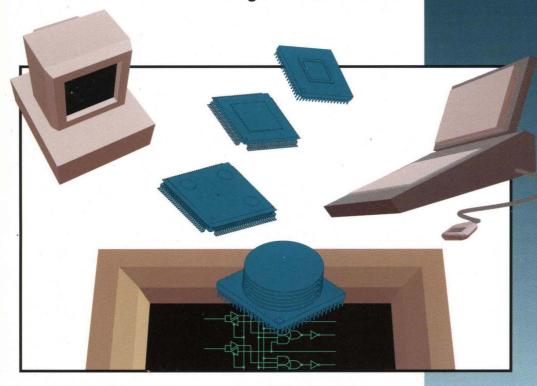
# FUJITSU

# **Channelless Gate Arrays**

1990 Data Book and Design Evaluation Guide



1990

FUĴITSU

Design Information
AU Series CMOS Gate Array Macrocell Library

CG21 Series CMOS Gate Array Macrocell Library

Sales Information





# **CMOS Channelless Gate Arrays**

1990 Data Book

Fujitsu Limited Tokyo, Japan Fujitsu Microelectronics, Inc. San Jose, California, U.S.A. Fujitsu Mikroelektronik GmbH Frankfurt, F.R. Germany

Fujitsu Microelectronics Pascific Asia PTE Limited Kowloon, Hong Kong

Copyright@ 1990 Fujitsu Microelectronics, Inc., San Jose, California

#### All Rights Reserved.

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete information sufficient for construction purposes is not necessarily given.

The information contained in this document has been carefully checked and is believed to be reliable. However, Fujitsu Microelectronics, Inc. assumes no responsibility for inaccuracies.

The information conveyed in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Fujitsu Limited, its subsidiaries, or Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. reserves the right to change products or specifications without notice.

No part of this publication may be copied or reproduced in any form or by any means, or transferred to any third party without prior written consent of Fujitsu Microelectronics, Inc.

This document is published by the Publications Department, Fuitsu Microelectronics, Inc., 3545 North First Street, San Jose, California, 95134-1804; U.S.A.

Printed in the U.S.A.Edition 2.0

Ethernet<sup>™</sup> is a registered trademark of Xerox Corporation. EtherStar<sup>™</sup> is a trademark of Fujitsu Microelectronics, Inc.

StarLANTM is a trademark of AT&T.

UNIX™ is a trademark of Bell Telephone Laboratories, Inc.

ViewCAD™ is a trademark of Fuiitsu Limited

X Window System™ is a trademark of Massachusetts Institute of Technology (MIT)

VERILOG™ is a trademark of Gateway Automation

LASAR™ is a trademark of Teradyne, Inc. HILO® is a registered trademark of GenRad, Inc.

IKOS™ is a trademark of IKOS Systems, Inc.

Synopsys<sup>TM</sup> Design Compiler<sup>TM</sup> is a trademark of Synopys Inc.

# Contents

Section 1 - Design Information	Preface . Fujitsu AS	C Products Listing		
Data Sheet: AU Series CMOS Gate Arrays   1-11	Section 1 – Desig	n Information		
Data Sheet: CG21 Series CMOS Gate Arrays   1-31    -31   Chapter 2   Steps Toward Design   1-49    -42   Chapter 3   Design Procedures   1-53    -53   Chapter 4   Design Considerations   1-65    -54   Chapter 5   Delay Estimation Principles   1-79    -75   Chapter 6   Quality and Reliability   1-99    -76   Chapter 7   Application Notes   1-115    -76   Developing Test Patterns that Work with the Physical Tester   1-117    -76   Selecting the Best Package for Your ASIC Design   1-123    -76   Section 2 - AU Series CMOS Gate Array Unit Cell Library    -76   Section 3 - CG21 Series CMOS Gate Array Unit Cell Library    -77   Selection 4 - Sales Information    -78   Integrated Circuits Corporate Headquarters - Worldwide   4-7    -78   FMI Sales Offices for North and South America   4-8    -79   FMI Representatives - USA   4-9    -70   FMI Representatives - Canada   4-11    -70   FMI Representatives - Mexico   4-11    -70   FMI Representatives - Puerto Rico   4-11    -70   FMI Represe	Chapter 1	Fujitsu CMOS Products		
Chapter 2         Steps Toward Design         1–49           Chapter 3         Design Procedures         1–53           Chapter 4         Design Considerations         1–65           Chapter 5         Delay Estimation Principles         1–79           Chapter 6         Quality and Reliability         1–99           Chapter 7         Application Notes         1–115           Developing Test Patterns that Work with the Physical Tester         1–117           Selecting the Best Package for Your ASIC Design         1–123           Section 3 – CG21 Series CMOS Gate Array Unit Cell Library           Section 4 – Sales Information           Introduction to Fujitsu         4–3           Integrated Circuits Corporate Headquarters – Worldwide         4–7           FMI Sales Offices for North and South America         4–8           FMI Representatives – USA         4–9           FMI Representatives – Canada         4–11           FMI Representatives – Mexico         4–11           FMI Representatives – Puerto Rico         4–11           FMI Representatives – Puerto Rico         4–11		Data Sheet: AU Series CMOS Gate Arrays		
Chapter 3 Design Procedures 1–53 Chapter 4 Design Considerations 1–65 Chapter 5 Delay Estimation Principles 1–79 Chapter 6 Quality and Reliability 1–99 Chapter 7 Application Notes 1–115 Developing Test Patterns that Work with the Physical Tester 1–117 Selecting the Best Package for Your ASIC Design 1–123  Section 2 – AU Series CMOS Gate Array Unit Cell Library  Section 3 – CG21 Series CMOS Gate Array Unit Cell Library  Section 4 – Sales Information Introduction to Fujitsu 4–3 Integrated Circuits Corporate Headquarters – Worldwide 4–7 FMI Sales Offices for North and South America 4–8 FMI Representatives – USA 4–9 FMI Representatives – Canada 4–11 FMI Representatives – Mexico 4–11 FMI Representatives – Puerto Rico 4–11 FMI Representatives – Puerto Rico 4–11		Data Sheet: CG21 Series CMOS Gate Arrays		
Chapter 4         Design Considerations         1–65           Chapter 5         Delay Estimation Principles         1–79           Chapter 6         Quality and Reliability         1–99           Chapter 7         Application Notes         1–115           Developing Test Patterns that Work with the Physical Tester         1–117           Selecting the Best Package for Your ASIC Design         1–123           Section 2 – AU Series CMOS Gate Array Unit Cell Library           Section 4 – Sales Information           Introduction to Fujitsu         4–3           Integrated Circuits Corporate Headquarters – Worldwide         4–7           FMI Sales Offices for North and South America         4–8           FMI Representatives – USA         4–9           FMI Representatives – Canada         4–11           FMI Representatives – Mexico         4–11           FMI Representatives – Puerto Rico         4–11	•	•		
Chapter 5 Delay Estimation Principles 1–79 Chapter 6 Quality and Reliability 1–99 Chapter 7 Application Notes 1–115 Developing Test Patterns that Work with the Physical Tester 1–117 Selecting the Best Package for Your ASIC Design 1–123  Section 2 – AU Series CMOS Gate Array Unit Cell Library  Section 3 – CG21 Series CMOS Gate Array Unit Cell Library  Section 4 – Sales Information Introduction to Fujitsu 4–3 Integrated Circuits Corporate Headquarters – Worldwide 4–7 FMI Sales Offices for North and South America 4–8 FMI Representatives – USA 4–9 FMI Representatives – Canada 4–11 FMI Representatives – Mexico 4–11 FMI Representatives – Puerto Rico 4–11 FMI Representatives – Puerto Rico 4–11	•	<b>y</b>		
Chapter 6 Quality and Reliability 1–99 Chapter 7 Application Notes 1–115 Developing Test Patterns that Work with the Physical Tester 1–117 Selecting the Best Package for Your ASIC Design 1–123  Section 2 – AU Series CMOS Gate Array Unit Cell Library  Section 3 – CG21 Series CMOS Gate Array Unit Cell Library  Section 4 – Sales Information Introduction to Fujitsu 4–3 Integrated Circuits Corporate Headquarters – Worldwide 4–7 FMI Sales Offices for North and South America 4–8 FMI Representatives – USA 4–9 FMI Representatives – Canada 4–11 FMI Representatives – Mexico 4–11 FMI Representatives – Puerto Rico 4–11 FMI Representatives – Puerto Rico 4–11	•	•		
Chapter 7 Application Notes	•	·		
Developing Test Patterns that Work with the Physical Tester 1–117 Selecting the Best Package for Your ASIC Design 1–123  Section 2 – AU Series CMOS Gate Array Unit Cell Library  Section 3 – CG21 Series CMOS Gate Array Unit Cell Library  Section 4 – Sales Information Introduction to Fujitsu 4–3 Integrated Circuits Corporate Headquarters – Worldwide 4–7 FMI Sales Offices for North and South America 4–8 FMI Representatives – USA 4–9 FMI Representatives – Canada 4–11 FMI Representatives – Mexico 4–11 FMI Representatives – Puerto Rico 4–11	•	•		
Section 2 – AU Series CMOS Gate Array Unit Cell Library  Section 3 – CG21 Series CMOS Gate Array Unit Cell Library  Section 4 – Sales Information  Introduction to Fujitsu 4–3 Integrated Circuits Corporate Headquarters – Worldwide 4–7 FMI Sales Offices for North and South America 4–8 FMI Representatives – USA 4–9 FMI Representatives – Canada 4–11 FMI Representatives – Mexico 4–11 FMI Representatives – Puerto Rico 4–11	Chapter 7	• •		
Section 2 – AU Series CMOS Gate Array Unit Cell Library  Section 3 – CG21 Series CMOS Gate Array Unit Cell Library  Section 4 – Sales Information  Introduction to Fujitsu 4–3 Integrated Circuits Corporate Headquarters – Worldwide 4–7 FMI Sales Offices for North and South America 4–8 FMI Representatives – USA 4–9 FMI Representatives – Canada 4–11 FMI Representatives – Mexico 4–11 FMI Representatives – Puerto Rico 4–11		· -		
Section 3 – CG21 Series CMOS Gate Array Unit Cell Library  Section 4 – Sales Information  Introduction to Fujitsu		Selecting the Best Package for Your ASIC Design		
Introduction to Fujitsu       4–3         Integrated Circuits Corporate Headquarters – Worldwide       4–7         FMI Sales Offices for North and South America       4–8         FMI Representatives – USA       4–9         FMI Representatives – Canada       4–11         FMI Representatives – Mexico       4–11         FMI Representatives – Puerto Rico       4–11				
Integrated Circuits Corporate Headquarters – Worldwide 4–7 FMI Sales Offices for North and South America 4–8 FMI Representatives – USA 4–9 FMI Representatives – Canada 4–11 FMI Representatives – Mexico 4–11 FMI Representatives – Puerto Rico 4–11	Section 3 – CG21	Series CMOS Gate Array Unit Cell Library		
FMI Sales Offices for North and South America       4–8         FMI Representatives – USA       4–9         FMI Representatives – Canada       4–11         FMI Representatives – Mexico       4–11         FMI Representatives – Puerto Rico       4–11	Section 4 – Sales	Information		
FMI Representatives – Canada       4–11         FMI Representatives – Mexico       4–11         FMI Representatives – Puerto Rico       4–11	Section 4 – Sales	Information n to Fujitsu		
FMI Representatives – Mexico	Section 4 – Sales Introductio	Information n to Fujitsu		
FMI Representatives – Puerto Rico	Section 4 – Sales Introductio Integrated FMI Sales	Information  n to Fujitsu		
·	Section 4 – Sales Introduction Integrated FMI Sales FMI Repre	Information n to Fujitsu		
	Section 4 – Sales Introductio Integrated FMI Sales FMI Repre	Information         n to Fujitsu       4–3         Circuits Corporate Headquarters – Worldwide       4–7         Offices for North and South America       4–8         sentatives – USA       4–9         sentatives – Canada       4–11		
FMI Distributors – USA 4–12	Section 4 – Sales Introduction Integrated FMI Sales FMI Repre	Information         n to Fujitsu       4–3         Circuits Corporate Headquarters – Worldwide       4–7         Offices for North and South America       4–8         sentatives – USA       4–9         sentatives – Canada       4–11         sentatives – Mexico       4–11		
FMI Distributors – Canada 4–16	Section 4 – Sales Introduction Integrated FMI Sales FMI Repre FMI Repre FMI Repre FMI Repre	Information         n to Fujitsu       4–3         Circuits Corporate Headquarters – Worldwide       4–7         Offices for North and South America       4–8         sentatives – USA       4–9         sentatives – Canada       4–11         sentatives – Mexico       4–11         sentatives – Puerto Rico       4–11		
FMG Sales Offices for Europe	Section 4 – Sales Introduction Integrated FMI Sales FMI Repre FMI Repre FMI Repre FMI Repre FMI Repre FMI Repre	Information         n to Fujitsu       4–3         Circuits Corporate Headquarters – Worldwide       4–7         Offices for North and South America       4–8         sentatives – USA       4–9         sentatives – Canada       4–11         sentatives – Mexico       4–11         sentatives – Puerto Rico       4–11         utors – USA       4–12		
FMG Distributors – Europe 4–18	Section 4 – Sales Introduction Integrated FMI Sales FMI Repre FMI Repre FMI Repre FMI Repre FMI Distrit FMI Distrit	Information         n to Fujitsu       4–3         Circuits Corporate Headquarters – Worldwide       4–7         Offices for North and South America       4–8         sentatives – USA       4–9         sentatives – Canada       4–11         sentatives – Mexico       4–11         sentatives – Puerto Rico       4–11         utors – USA       4–12         utors – Canada       4–16		
FMA Sales Offices for Asia and Australia 4–20	Section 4 – Sales Introduction Integrated FMI Sales FMI Repre FMI Repre FMI Repre FMI Repre FMI Distrit FMI Distrit FMG Sale FMG Distrit	Information         n to Fujitsu       4–3         Circuits Corporate Headquarters – Worldwide       4–7         Offices for North and South America       4–8         sentatives – USA       4–9         sentatives – Canada       4–11         sentatives – Mexico       4–11         sentatives – Puerto Rico       4–11         utors – USA       4–12         utors – Canada       4–16         s Offices for Europe       4–17         butors – Europe       4–18		
FMA Representatives – Asia	Section 4 – Sales Introduction Integrated FMI Sales FMI Repre FMI Repre FMI Repre FMI Distrit FMI Distrit FMG Sale FMG Distrit FMA Sale	Information         n to Fujitsu       4–3         Circuits Corporate Headquarters – Worldwide       4–7         Offices for North and South America       4–8         sentatives – USA       4–9         sentatives – Canada       4–11         sentatives – Mexico       4–11         sentatives – Puerto Rico       4–11         utors – USA       4–12         utors – Canada       4–16         s Offices for Europe       4–17         butors – Europe       4–18         c Offices for Asia and Australia       4–20		
FMA Distributors – Asia and Australia 4–22	Section 4 – Sales Introduction Integrated FMI Sales FMI Repres FMI Repres FMI Repres FMI Distrit FMI Distrit FMI Sales FMI Distrit FMI Sales FMI Distrit FMI DISTRIT FMI DISTRIT FMI DISTRIT FMI SALES FMI REPRES FMI REPRES	Information         n to Fujitsu       4–3         Circuits Corporate Headquarters – Worldwide       4–7         Offices for North and South America       4–8         sentatives – USA       4–9         sentatives – Canada       4–11         sentatives – Puerto Rico       4–11         sentatives – Puerto Rico       4–11         utors – USA       4–12         utors – Canada       4–16         s Offices for Europe       4–17         butors – Europe       4–18         c Offices for Asia and Australia       4–20         esentatives – Asia       4–21		

# Illustrations

Figures
1–1 The Basic Cell
1–2 The Basic Cell as a 2–input NAND Gate
1–3 Physical Construction of the Unit Cell NAND Gate
1–4 . Channeled Gate Array Chip Structure
1–5 Channelless Gate Array Chip Structure
1-6 Equivalent Gate Count vs. Processing Speed, Fujitsu CMOS Gate Array Technologies 1-9
1–7 Equivalent Gate Count, Fujitsu CMOS ASIC Technology Families
3–1 ASIC Design Flow with ViewCAD
3–2 Generic Workstation Design flow
3–3 . Post–Workstation Design Process
4–1 Hierarchical Organization of AU/CG21 Designs
4–2 Bus Driver Cell, B41
4–3 SSO–Generated Noise
4–4 SSO Pin Assignments
4–5 Scan Circuit Configuration
5–1 Delay Time vs. Loading Factor
5–2 . Delay Path Sample Circuit
5–3 Operating Environment Factors Influencing Delay
6-1 Quality Control Processes at Fujitsu 1-100
6–1 (Continuation) Quality Control Processes at Fujitsu
6–2 Distribution of Component Failure
6–3 . Example of Life Test Data on IC
6–4 Acceleration Rate vs. Junction Temperature
6–5 Digital IC Failures and Corrective Actions
Figures from Chapter 7, Application Notes
CMOS ASIC Test Patterns
1 Determining a Successful Test Cycle Length
2 Determining Preferred Cycle Length
3 Input to Input Skew
4 Input to Output Skew
ASIC Packaging Considerations
1 Package Size versus Pin Count
2 Minimizing Interconnect Length
3 Impact of Noise on Speed

	PLCC Package Construction (Front View)	
5	PLCC Lead Frame Construction (Top View)	
6	321-Pin Ceramic Pin Grid Array1-132	
7	Staggered Pin Grid Array Routing	
8	Flatpack Configurations	
9	Defect Caused by Difference in Thermal Coefficient of Expansion	
10	PLCC Package1–136	
11	Cross-Section of a Plastic Small-Outline J-Lead Package	
12	Surface Mount PGA         1–137	
13	Solder Pad Design for Surface Mount Pin Grid Arrays	
14	CMOS Output Buffer Model (Totem Pole)	
15	I/O Model, CMOS Input1–141	
16	I/O Model, TTL Input	
17	CMOS Basic Gate Structure: The Pull–up/Pull–down Network	
18	CMOS Basic Gate Structure: The Transmission Gate	
19	Electrical Model of Simultaneously Switching Outputs	
20	Effect of SSO Noise on Thresholds	
21	Variation in Inductance, Resistance, and Capacitance as a Function of Pin Position 1-147	
22	Measured Pin Capacitance by Package Position	
23	Self-Inductance in a Circuit	
24	Causes of Crosstalk	
25	Heat Flow through a Cavity-down Ceramic PGA with an Annular Fin Heat Sink 1-153	
Tables		
1-1		
	SuperMacro Implementations for CMOS ASIC	
4~1	SuperMacro Implementations for CMOS ASIC	
4–1 4–2	SuperMacro Implementations for CMOS ASIC	
4–1 4–2 4–3	SuperMacro Implementations for CMOS ASIC	
4–1 4–2 4–3 4–4	SuperMacro Implementations for CMOS ASIC 1–7  Basic Cells per Hierarchy Level 1–67  Recommended Maximum I/O Count per Block 1–67  Representative Value of Output Buffers 1–73	
4-1 4-2 4-3 4-4 5-1	SuperMacro Implementations for CMOS ASIC 1–7 Basic Cells per Hierarchy Level 1–67 Recommended Maximum I/O Count per Block 1–67 Representative Value of Output Buffers 1–73 Junction Temperature Coefficient of Load 1–74	
4-1 4-2 4-3 4-4 5-1 5-2	SuperMacro Implementations for CMOS ASIC 1–7 Basic Cells per Hierarchy Level 1–67 Recommended Maximum I/O Count per Block 1–67 Representative Value of Output Buffers 1–73 Junction Temperature Coefficient of Load 1–74 AC Parameters of Unit Cells 1–82	
4-1 4-2 4-3 4-4 5-1 5-2 5-3	SuperMacro Implementations for CMOS ASIC 1–7 Basic Cells per Hierarchy Level 1–67 Recommended Maximum I/O Count per Block 1–67 Representative Value of Output Buffers 1–73 Junction Temperature Coefficient of Load 1–74 AC Parameters of Unit Cells 1–82 Estimation Table for Metal Loading 1–83	
4-1 4-2 4-3 4-4 5-1 5-2 5-3	SuperMacro Implementations for CMOS ASIC 1–7  Basic Cells per Hierarchy Level 1–67  Recommended Maximum I/O Count per Block 1–67  Representative Value of Output Buffers 1–73  Junction Temperature Coefficient of Load 1–74  AC Parameters of Unit Cells 1–82  Estimation Table for Metal Loading 1–83  Package Thermal Resistance in °C/W 1–88	
4-1 4-2 4-3 4-4 5-1 5-2 5-3 5-4	SuperMacro Implementations for CMOS ASIC 1–7  Basic Cells per Hierarchy Level 1–67  Recommended Maximum I/O Count per Block 1–67  Representative Value of Output Buffers 1–73  Junction Temperature Coefficient of Load 1–74  AC Parameters of Unit Cells 1–82  Estimation Table for Metal Loading 1–83  Package Thermal Resistance in °C/W 1–88  Power Dissipation Calculation Factors 1–90	
4-1 4-2 4-3 5-1 5-2 5-3 5-4 5-6	SuperMacro Implementations for CMOS ASIC         1-7           Basic Cells per Hierarchy Level         1-67           Recommended Maximum I/O Count per Block         1-67           Representative Value of Output Buffers         1-73           Junction Temperature Coefficient of Load         1-74           AC Parameters of Unit Cells         1-82           Estimation Table for Metal Loading         1-83           Package Thermal Resistance in °C/W         1-88           Power Dissipation Calculation Factors         1-90           Input Buffer AC Power Dissipation (P <sub>ACIN</sub> ) Examples (in mW)         1-91	
4-1 4-2 4-3 5-1 5-2 5-3 5-4 5-6 5-7	SuperMacro Implementations for CMOS ASIC         1–7           Basic Cells per Hierarchy Level         1–67           Recommended Maximum I/O Count per Block         1–67           Representative Value of Output Buffers         1–73           Junction Temperature Coefficient of Load         1–74           AC Parameters of Unit Cells         1–82           Estimation Table for Metal Loading         1–83           Package Thermal Resistance in °C/W         1–88           Power Dissipation Calculation Factors         1–90           Input Buffer AC Power Dissipation (P <sub>ACIN</sub> ) Examples (in mW)         1–91           Output and Bidirectional Buffer AC Power Dissipation (P <sub>ACOUT</sub> ) Examples (in mW)         1–90	
4-1 4-2 4-3 5-1 5-2 5-3 5-4 5-6 5-7 5-8	SuperMacro Implementations for CMOS ASIC 1–7  Basic Cells per Hierarchy Level 1–67  Recommended Maximum I/O Count per Block 1–67  Representative Value of Output Buffers 1–73  Junction Temperature Coefficient of Load 1–74  AC Parameters of Unit Cells 1–82  Estimation Table for Metal Loading 1–83  Package Thermal Resistance in °C/W 1–88  Power Dissipation Calculation Factors 1–90  Input Buffer AC Power Dissipation (P <sub>ACIN</sub> ) Examples (in mW) 1–91  Output and Bidirectional Buffer AC Power Dissipation (P <sub>DCOUT</sub> ) Examples (in mW) 1–90  Output and Bidirectional Buffer DC Power Dissipation (P <sub>DCOUT</sub> ) Examples (in mW) 1–90	
4-1	SuperMacro Implementations for CMOS ASIC 1–7  Basic Cells per Hierarchy Level 1–67  Recommended Maximum I/O Count per Block 1–67  Representative Value of Output Buffers 1–73  Junction Temperature Coefficient of Load 1–74  AC Parameters of Unit Cells 1–82  Estimation Table for Metal Loading 1–83  Package Thermal Resistance in °C/W 1–88  Power Dissipation Calculation Factors 1–90  Input Buffer AC Power Dissipation (P <sub>ACIN</sub> ) Examples (in mW) 1–91  Output and Bidirectional Buffer AC Power Dissipation (P <sub>ACOUT</sub> ) Examples (in mW) 1–90  Output and Bidirectional Buffer DC Power Dissipation (P <sub>DCOUT</sub> ) Examples (in mW) 1–90  Internal Basic Cell Power Dissipation (P <sub>G</sub> ) Examples 1–91	
4-1	SuperMacro Implementations for CMOS ASIC  Basic Cells per Hierarchy Level	
4-1	SuperMacro Implementations for CMOS ASIC 1–7  Basic Cells per Hierarchy Level 1–67  Recommended Maximum I/O Count per Block 1–67  Representative Value of Output Buffers 1–73  Junction Temperature Coefficient of Load 1–74  AC Parameters of Unit Cells 1–82  Estimation Table for Metal Loading 1–83  Package Thermal Resistance in °C/W 1–88  Power Dissipation Calculation Factors 1–90  Input Buffer AC Power Dissipation (P <sub>ACIN</sub> ) Examples (in mW) 1–91  Output and Bidirectional Buffer AC Power Dissipation (P <sub>ACOUT</sub> ) Examples (in mW) 1–90  Output and Bidirectional Buffer DC Power Dissipation (P <sub>DCOUT</sub> ) Examples (in mW) 1–90  Internal Basic Cell Power Dissipation (P <sub>G</sub> ) Examples 1–91  RAM Macro Power Dissipation (P <sub>RAM</sub> ) Examples (in mW) 1–92  ROM Power Dissipation (P <sub>ROM</sub> ) Examples (in mW) 1–92	

5-13 . Single and Dual-Port RAM Columnar Configurations	1–95
5-14 . Calculated Parameters for Single-Port 256K x 8 Bit RAM	1–96
5-15 Delay Parameters for a Single-Port 256K x 8 Bit RAM (AU Series)	1–97
6-1a . Sampling Plan for Engineering Testing: Endurance Test	1–102
6-1b . Sampling Plan for Engineering Testing: Environmental and Mechanical Test	1–103
6-1c . Sampling Plan for Engineering Testing: Environmental and Mechanical Test (Optional) .	1–104
6-1d . Sampling Plan for Engineering Testing: Continuity Test	1–104
6–2 Determination of Coefficient	1–108
6-3 Product Defects Analysis	1–110
6-4 Relationship between Failure Causes and Analytical Test Methods	1–11
6-5 Sampling Plan for Reliability Testing	1–112
6-6 Example of Reliability Testing	1–113
6–7 Example of Electrical Testing	1–113
6-8 Example of Electrical Criteria	1–114
Tables from Chapter 7, Application Notes	
ASIC Packaging Considerations	
1 Considerations for Package Selection	1–124
2 Package Material Characteristics	1–128
3 Fujitsu Package Types	1–130
4 PGAs Available from Fujitsu	1–13
5 Comparison of Critical Features	1–138
6 ASIC CMOS Package Types and their Characteristics	1–140
7 Electrical Characteristics of Each Signal Type	1–14

#### **Preface**

Fujitsu Microelectronics introduced its first commercially available gate array, a bipolar chip called the B200, in 1974 (Fujitsu had been making them for internal use since 1972). Over the years it has been so popular that it is regarded as the world's most widely implemented gate array. Since that first array, Fujitsu has produced over 9000 successful bipolar and CMOS custom designs.

Fujitsu designs are successful because they are implemented using the most advanced design verification CAD systems available, allowing the production of chips with 90% cell utilization (more functional logic per chip than the industry standard) and one of the highest performance records in the industry.

This data book provides you with the information necessary to choose an application specific integrated circuit (ASIC) device using Fujitsu's advanced AU and CG21 channelless (sea-of-gates) CMOS gate array technologies. The data book describes Fujitsu's AU and CG21 gate arrays, explains their benefits and specifications, and outlines the process by which logic and circuit designers create a chip. The cell function (unit cell) libraries for the AU and CG21 technologies are included in the second and third sections of this volume. The first volume in this data book series provides the same information for Fujitsu's channeled gate arrays.

Fujitsu has pioneered and maintained a technological lead in the production of bipolar as well as CMOS ASIC devices; data books describing Fujitsu's other ASIC product families, as well as any other technical or sales-related information, may be obtained from any Fujitsu Technical Resource Center or Sales Office listed at the end of this book or by calling or writing Fujitsu Microelectronics Inc., 3545 North First Street, San Jose, CA 94135–1804, (408) 922–9000.

# **Fujitsu ASIC Products Listing**

#### **CMOS Channeled Gate Arrays Data Book**

#### UHB Series High Drive CMOS Gate Arrays — 1.5μ, 0.9 ns typical delay

Description	Name	Device Part Number
336 Gates, 58 I/O	C330UHB	MB625xxx
530 Gates, 64 I/O	C530UHB	MB624xxx
830 Gates, 74 I/O	C830UHB	MB623xxx
1,233 Gates. 88 I/O	C1200UHB	MB622xxx
1,724 Gates, 102 I/O	C1700UHB	MB621xxx
2,220 Gates, 115 I/O	C2200UHB	MB620xxx
3,066 Gates, 140 I/O	C3000UHB	MB606xxx
4,174 Gates, 155 I/O	C4100UHB	MB605xxx
6.000 Gates, 155 I/O	C6000UHB	MB604xxx
8.768 Gates, 188 I/O	C8700UHB	MB603xxx
12.734 Gates, 220 I/O	C12000UHB	MB602xxx

#### CG10 Series H

3,256 Gates, 108 I/O	CG10272	MBCG10272xxx
4,032 Gates, 123 I/O	CG10342	MBCG10342xxx
5,072 Gates, 148 I/O	CG10492	MBCG10492xxx
6,510 Gates, 163 I/O	CG10572	MBCG10572xxx
7,684 Gates, 163 I/O	CG10692	MBCG10692xxx
11,080 Gates, 188 I/O	CG10103	MBCG10103xxx
14,720 Gates, 220 I/O	CG10133	MBCG10133xxx

#### **CMOS Channelless Gate Arrays Data Book**

#### AU Series CMOS Series Gate Arrays — $1.2\mu$ , 0.6 ns typical delay

C10KAU	MB637xxx
C15KAU	MB636xxx
C20KAU	MB635xxx
C30KAU	MB634xxx
C40KAU	MB633xxx
C50KAU	MB632xxx
C75KAU	MB631xxx
C100KAU	MB630xxx
	C15KAU C20KAU C30KAU C40KAU C50KAU C75KAU

#### CG21 Series CMOS Series Gate Arrays — $0.8\mu$ , 370 ps typical delay

10,224 Gates, 108 I/O	CG21103	MBCG21103xxx
15,486 Gates, 142 I/O	CG21153	MBCG21153xxx
20,876 Gates, 155 I/O	CG21203	MBCG21203xxx
31,500 Gates, 178 I/O	CG21303	MBCG21303xxx
41,184 Gates, 220 I/O	CG21403	MBCG21403xxx
52,164 Gates, 245 I/O	CG21503	MBCG21503xxx
75,140 Gates, 284 I/O	CG21753	MBCG21753xxx
102,144 Gates, 332 I/O	CG21104	MBCG21104xxx

# Fujitsu ASIC Products Listing (Continued)

#### **BiCMOS Gate Arrays Data Book**

#### BC Series BiCMOS Gate Arrays — $1.5\mu/1.4\mu$ , 0.65 ns typical delay

Description	Name	Device Part Number
645 Gates, 52 I/O	BC400	MB211xxx
1,218 Gates, 72 I/O	BC800	MB212xxx
1,872 Gates, 96 I/O	BC1200	MB213xxx
3,240 Gates, 112 I/O	BC2000	MB214xxx

#### BC-H Series BiCMOS Gate Arrays — 1.0μ/0.5μ, 0.45 ns typical delay

4,312 Gates, 96 I/O	BC4000H	MB221xxx
8,160 Gates, 128 I/O	BC8000H	MB222xxx
11,968 Gates, 160 I/O	BC12000H	MB223xxx
16,720 Gates, 200 I/O	BC16000H	MB224xxx
7,920 Gates, 200 I/O with 40Kb RAM	BC8040HM	MB228xxx

#### **ECL Gate Arrays Data Book**

#### ET Series ECL Gate Arrays - 1.0µ, 220 ps typical delay

1.056 Gates, 64 I/O	ET750	MB121Kxxx
2,112 Gates, 88 I/O	ET1500	MB123Kxxx
4,224 Gates, 120 I/O	ET3000	MB125Kxxx
6,160 Gates, 120 I/O	ET4500	MB128Kxxx
2,640 Gates, 120 I/O with 4.6 Kb RAM	ET2004M	MB181/191xxx
2,640 Gates, 136 I/O, with 9.2 Kb RAM	ET2009M	MB182/192xxx
3,960 Gates, 136 I/O, with 4.6 Kb RAM	ET3004M	MB183/193xxx

#### H Series ECL Gate Arrays — 0.5μ, 100 ps typical delay

9,856 Gates, 200 I/O	ET10000H	MB147/157xxx
9,856 Gates, 300 I/O	E10000H	MB148/158xxx
4 928 Gates 200 I/O with 5 1Kh RAM	E5005HM	MB185/195xxx

#### Ultra High Performance ECL Gate Arrays 0.5µ, 75 ps typical delay

128 Gates, 23 /I/O	E128H	MB1800
32 Gates, 13 I/O	E32	MB1700
128 Gates 16 I/O	E128	MB1600

#### VH Series ECL Gate Arrays 0.4μ, 80 ps typical delay

38,948 Gates, 300 I/O	E30000VH	MB162/172xxx
13,440 Gates, 290 I/O, 40Kb RAM	E10040VHM	MB165/175xxx
13 440 Gates 294 I/O 160Kh BOM	F10160VHR	MB168/178xxx

#### **CMOS Standard Cell Data Book**

AU Series Standard Cells — 1.2µ, 0.6 ns typical delay

AS Series Standard Cells - 0.8 µ, 370 ps typical delay

# **Design Information**

Page			
1–3	Chapter	1	Fujitsu CMOS Products
1–11 1–31			heet: AU Series CMOS Gate Arrays heet: CG21 Series CMOS Gate Arrays
1–49	Chapter	2	Steps Toward Design
1–53	Chapter	3	Design Procedures
1-65	Chapter	4	Design Considerations
1-79	Chapter	5	Delay Estimation Principles
1-99	Chapter	6	Quality and Reliability
1-115	Chapter	7	Application Notes
1–117			Developing Test Patterns that Work with the Physical Tester
1–123			Selecting the Best Package for Your ASIC Design

#### Chapter 1 - Fujitsu CMOS Products

#### Contents of This Chapter

- 1.1 Introduction
- 1.2 CMOS Technology for ASICs
- 1.3 CMOS Gate Array Structure
- 1.4 Fujitsu's CMOS Gate Arrays

Data Sheet: AU Series CMOS Gate Arrays
Data Sheet: CG21 Series CMOS Gate Arrays

#### 1.1 Introduction

This section of the data book gives an overview of CMOS technology and introduces the CMOS channelless gate array technology families developed by Fujitsu to implement ASIC designs.

#### 1.2 CMOS Technology for ASICs

ASICs (Application Specific Integrated Circuits) are large scale integrated circuits that provide customers with made-to-order functions. These ICs implement the unique value designed into customer products by producing custom semiconductor designs that allow customers to take advantage of perceived market opportunities in a timely manner. The customized solutions offered by ASICs combine the power of personalized electronics and the advantage of increased system efficiency.

CMOS technology has long been chosen for ASIC applications because of its low power and high density characteristics. Advancing process technology and new production and fabrication techniques have now allowed device speed to increase to the point where it is competitive with bipolar devices. Fujitsu CMOS gate arrays are manufactured using advanced silicon gate technology utilizing two-layer and three-layer metal. This fabrication process yields parts that:

- a. require very low power dissipation (typically less than 500 mW per channeled array)
- b. operate at speeds equaling existing bipolar technologies
- c. feature higher gate densities than competing bipolar devices
- d. use a single power supply of 5 volts or less
- e. provide top-grade noise immunity and programmable logic levels compatible with TTL and CMOS logic families

#### 1.3 CMOS Gate Array Structure

Fujitsu CMOS gate arrays are configured in a matrix of basic cells in the center of the chip with input-output (I/O) cells on the device periphery. One basic cell is equivalent to a two-input NAND gate. The custom logic function is realized by interconnecting basic cells with double-layer metallization for the channeled and smaller channelless arrays and triple-layer metallization for channelless arrays of over 30K equivalent gates. Fujitsu's gate array products are fabricated using a twin-tub polysilicon CMOS process to produce high-speed, high-density arrays consisting of 300 to 100,000 basic cells.

#### 1.3.1 The Basic Cell

The basic cell of Fujitsu's CMOS gate array is a common building block consisting of one pair of P-channel and one pair of N-channel MOS transistors (represented by the broken-line box in Figure 1–1). Channelless arrays differ from the channeled arrays by the addition of four smaller N-channel transistors also shown in Figure 1–2. The four additional transistors are isolated from the P-and N-channel pairs, have no effect on them when the basic cells are configured as digital logic unit cells, and can be used as

an area to place the metalization that connects the unit cells. The basic cells are assembled in pairs on double-wide columns, and share common terminals of the two sets of four N-channel transistors.

The four additional N-channel transistors are used in conjunction with the "generic" portion of the basic cell to construct RAM and ROM compiled cell modules.

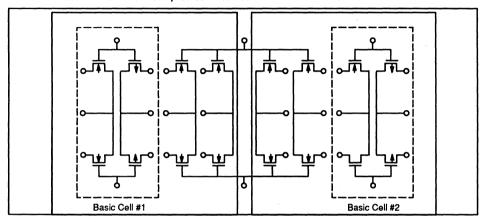


Figure 1-1. The Basic Cell

Since these are "generic" basic cells, no connections are shown to the power supply (+5 volts), to ground, or to the two common control gate terminals of the circuit. These connections are made as required during the metalization phase of the manufacturing process. The basic cell is the building block of all functions of the array and is often used as a unit to describe the size of an array or the complexity of a unit cell (logic function).

Figure 1–2 shows a schematic representation of the basic cell with the addition of the custom metalization required to convert the generic basic cell into a two-input NAND gate.

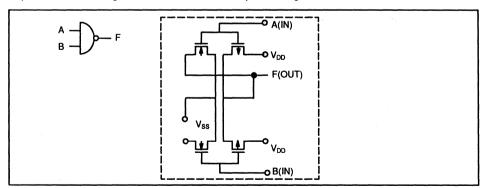


Figure 1-2. The Basic Cell as a 2-Input NAND Gate

#### 1.3.2 Basic Cell Construction

Basic cell construction varies somewhat among Fujitsu's CMOS technologies; however, an explanation based on AV technology provides a good model of how a basic cell is fabricated in any of the CMOS

families. In AV, the basic cell is constructed from an N-type silicon substrate upon which a P-well is deposited. The surface of the substrate is then covered with a thin layer of silicon dioxide (glass) and two strips of polysilicon are deposited perpendicular to the P-well and geometrically parallel. (Polysilicon is a silicon-based compound chemically altered so that it has good electrical conduction properties.) The polysilicon strips serve as the gate control elements of the basic cell and also as the two electrical interconnections between the sources of the P and N transistor pairs. See Figure 1–3.

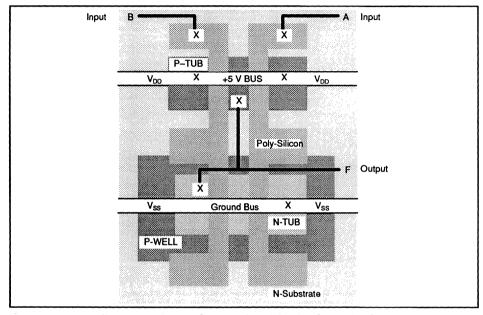


Figure 1-3. Physical Construction of the Unit Cell NAND Gate

The silicon dioxide layer is then stripped away from all areas of the substrate not protected by polysilicon. In two separate steps, the N-type and the P-type material of the twin tubs is diffused onto the substrate.

For the next step, N-type material is diffused or implanted into the P-well that was previously laid down. It straddles the two strips of polysilicon close to their ends. The polysilicon resists the diffusion, which results in the formation of three pads of N-type material separated by the two strips of polysilicon (self-aligned processing). The center pad of N-type material serves as a common drain terminal for both N-channel transistors. The outer pads are the separate source elements.

Then the P-type material is deposited on the the N-type substrate straddling the two polysilicon strips. Similarly the center pad of P-type material forms the common source connection for both P-channel transistors. The basic cell is then converted to a unit cell by application of a custom metalization pattern that connects (or wires) various points of the basic cell, or a number of basic cells, together. NO TAG shows the structure of a basic cell configured as a NAND gate after metalization (represented by the solid bold line connections) has been laid down.

Cell construction in the AU and CG21 technologies requires three layers of metal to be applied. Such layers are separated by an insulating layer of silicon dioxide. Interconnections between the metal layers are made by means of "vias" passing through the glass.

#### 1.3.3 Basic Cell Arrangement

Basic cells can be arranged in any of the following configurations:

- Unit cells
- b. User macros
- c. Compiled cells and super macros
- d. I/O buffer cells

#### 1.3.4 Unit Cells

Unit cells are the fundamental logic unit or function used for logic design, including digital logic gates, compiled cells, and I/O buffers.

#### 1.3.5 User Macros

User macros are composed of unit cells to form higher level logic block functions (e.g., shift register or decoder). Such blocks are user-defined and may contain any unit cell configuration.

#### 1.3.6 Compiled Cells and SuperMacros

Compiled cells and supermacros are MSI and LSI macros that perform memory functions (RAM and ROM) and such logic functions as adders and multipliers. Compiled cells are automatically generated by Fujitsu using proprietary compilers. Their building block approach and functional compatibility with common MSI and LSI devices can simplify construction of large and complicated designs. These cells are currently available for the AU and CG21 technologies; the status and design requirements of the super macros should be verified with a Fujitsu Sales Office or Technical Resource Center.

Selected compiled cells include:

- Dual-port RAM
- Triple-port RAM
- Single-port RAM
- ROM
- Multiplier
- Barrel shifter
- FIFO compiler

#### SuperMacros

Fujitsu's next step upward in ASIC functionality is embodied in the concept of supermacros. SuperMacros are large functional organizations implemented as an integral part of a chip. SuperMacros can be large-scale compiled cells or core cells, as well as generic or proprietary LSI functions. Reduction of board space, reduction of cost, and reduction of design cycle time, as well as extended functionality, reliability, performance, and security of design are all advantages of supermacros. Since supermacros are not bound to a particular technology, they may be migrated from one technology to another.

Fujitsu provides customers with gate and behavioral level models, macro symbols, and data sheets/specifications as well as kit parts in order to provide complete support from development to system integration. The supermacros listed below are the first to be developed for Fujitsu's CMOS supermacro library.

2843

3600

917

~500

1100

33

~3900

Compatible Device Technology **Gate Complexity** Universal Synchronous/Asynchronous Receiver/Transmitter (USART) 8251A UHB/AU/CG21 2900 Universal Asynchronous 8868 UHB/AU/CG21 TRD Receiver/Transmitter (UART) Programmable Interval Timer 8253 UHB/AU/CG21 5680 Programmable Peripheral Interface 8255A UHB/AU/CG21 784 - 1403<sup>1</sup> Programmable Interrupt Controller UHB/AU/CG21 8259 2205 Programmable DMA Controller 8237 UHB/AU/CG21 5100 Clock Generator/Driver 8284 UHB/AU/CG21 99 8288 UHB/AU/CG21 250 8254 Programmable Internal Timer UHB/AU/CG21 3500

UHB/AU/CG21

UHB/AU/CG21

UHB/AU/CG21

UHB/AU/CG21

UHB/AU/CG21

UHB/AU/CG21

UHB/AU/CG21

6845

87030<sup>2</sup>

87012<sup>2</sup>

2901

2902

2904

2910

Table 1-1, SuperMacro Implementations for CMOS ASIC

4-bit Arithmetic Logic Unit (ALU) Slice

Bus Controller

**CRT Controller** 

SCSI Protocol Controller

Status and Shift Control

12-bit Microprogram Controller

EtherNet Controller3

Carry Lookahead

#### 1.3.7 I/O (Input/Output) Buffer Cells

The I/O buffer cell is composed of both external and internal I/O cells. External I/O cells are located on the periphery of the gate array. Internal I/O cells are ordinary unit cells located in the main cell matrix of the gate array. There are a variety of I/O buffer designs including input, output, and bidirectional buffers.

Input buffers convert external voltage levels to internal CMOS levels. Input buffers include:

Low-drive input buffers with pull-up or pull-down resistance

Schmitt trigger input buffers

High-drive clock input buffers

Output buffers convert internal CMOS levels to external voltage levels and are available with 3.2 mA, 8 mA, 12 mA, and 24 mA current sink capability, and optional noise-limiting resistance (edge rate control). Output buffers include:

Output buffers with noise-limiting resistance

3-state output buffers

The bidirectional buffer is a combination of an input buffer and a 3-state output buffer in the same unit cell.

#### 1.3.8 Structure of the Chip

The arrangement of the basic cells on the chip differs according to the technology. The fundamental chip layout is a matrix of basic cells surrounded by a perimeter of I/O cells. In the channeled arrays, basic cells can be arranged in single columns, with the channels between the columns used for routing unit cell interconnections, as in AV, AVB, AVL, and AVM technologies, or in double columns, as in UHB technology. See Figure 1-4. In the channelless or sea-of-gates technologies (AU and CG21), the cells are positioned with no wiring channels between the double columns, allowing the wiring to go over the cells, rather than between the cells. See Figure 1-5.

<sup>1</sup>Several options are available (Mode 0 is 785 gates) 2Full-featured Fujitsu proprietary supermacro

<sup>&</sup>lt;sup>3</sup>Under consideration

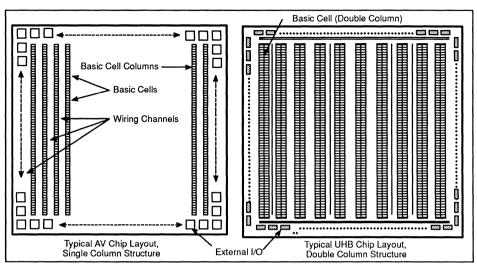


Figure 1-4. Channeled Gate Array Chip Structure

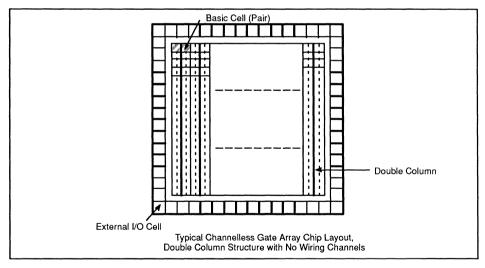


Figure 1-5 Channelless Gate Array Chip Structure

Larger gate arrays depart from the fundamental layout scheme by partitioning the basic cell matrix into four blocks. In some instances the designer may define the size of each block within certain limitations, while in other cases the block size is fixed. The purpose of chip partitioning is to improve speed performance by controlling wire length. Each block can be looked at as a small gate array, with four such gate arrays inside one package. (Smaller arrays exhibit less delay than larger ones.) In the AU and CG21 technologies, a block can be devoted to RAM or ROM for special applications requiring memory.

#### 1.4 Fujitsu's CMOS Gate Arrays

Fujitsu's channelless CMOS gate arrays are described in detail in the data sheet that follows at the end of this chapter. Complete information on Fujitsu's channeled CMOS gate array families is provided in a separate data book.

All offer the same high reliability, fast turnaround on design, simplified customer interface, full support by Fujitsu ViewCAD system design software if requested, full design support on other major CAE workstations, and a wide variety of packaging options.

The number of gates in relationship to the processing speed of each new CMOS technology is shown in Figure 1–6. Figure 1–7 shows in tabular form the equivalent gate count for each technology family.

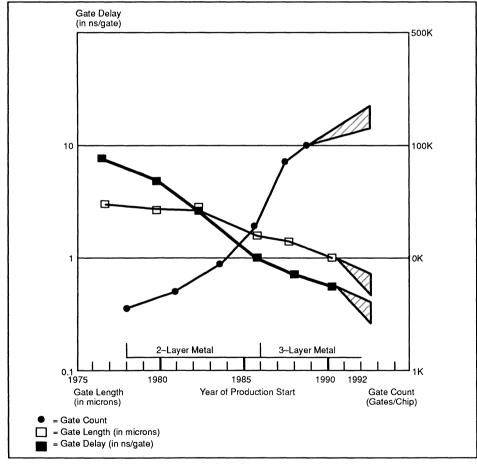


Figure 1–6. Equivalent Gate Count vs. Processing Speed, Fujitsu CMOS Gate Array Technologies

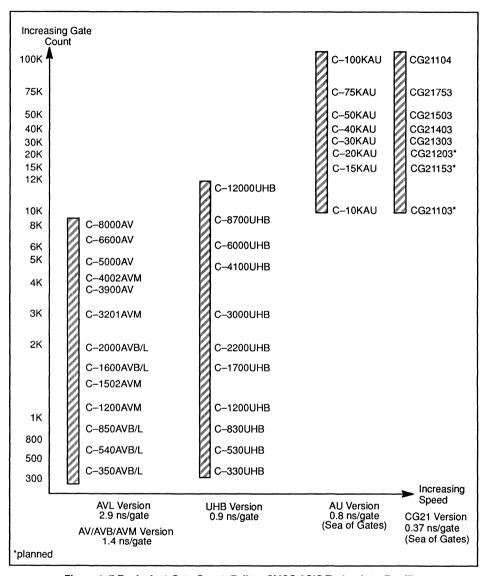


Figure 1–7 Equivalent Gate Count, Fujitsu CMOS ASIC Technology Families

AU Series CMOS Gate Arrays

# DESCRIPTION

The AU series of 1.2  $\mu$ m CMOS gate arrays, available in eight device types with from 10K to 100K gates, achieves the ultra fast speed of 0.6 ns per gate. Thanks to the channel-free structure of the AU gate array, AU basic cells can be used for logic cells, memory cells, or wiring area in order to implement the desired functions. The full utilization of the array surface and the three-layer metal interconnect technology produce a 75 percent maximum gate usability ratio.

The logic and I/O cells for the AU series are functionally compatible with Fujitsu's UHB series of gate arrays as well as with the new CG21 arrays to simplify upgrading. User-specifiable RAM and ROM configurations are also available. These gate arrays facilitate the implementation of large-scale devices such as computer and graphic processors on single chips.

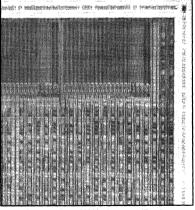
#### **FEATURES**

- 1.2 micron CMOS sea-of-gates technology
  - -3 layer metal interconnect for C30KAU to C100KAU
  - -2-layer metal interconnect for C30KAU to C20KAU
- · Ultra high speed
  - 0.8 ns/gate for 2-input NAND
  - 0.6 ns/gate for power 2-input NAND
- · High basic cell usage
  - 75% maximum for logic with RAM/ROM
  - 50% maximum for logic only
- High sink current capability
  - sink current up to 24 mA
- Minimum delay clock buffer true option

- · High current clock drivers
  - -Low-skew clock signal distribution
- · Extensive unit cell library (logic cell, RAM, ROM)
  - Unit cells functionally compatible with Fujitsu's UHB gate array series and new CG21 series
- Automatic test pattern generation optional
- On-chip pull-up/pull-down resistors
- High pin count plastic and ceramic packages
- High-density RAM and ROM compilers
  - up to 18K bit RAM compilation
  - up to 64K ROM compilation

#### PRODUCT FAMILY

Device	Part Number	BCs on Chip (2-input gate +4 N-ch Tr)	Usable BCs	Max Signal I/O
C-10KAU	MB637xxx	10,224		108
C-15KAU	MB636xxx	15,486	75% max. for Logic with	138
C-20KAU	MB635xxx	20,876	RAM,ROM	155
C-30KAU	MB634xxx	31,500	50% max. for Logic only	178
C-40KAU	MB633xxx	41,184	(Preliminary	220
C-50KAU	MB632xxx	52,164	values, to be upgraded)	245
C-75KAU	MB631xxx	75,140		300
C-100KAU	MB630xxx	102,144		332



Corner of 100KAU after metallization

Copywrite © 1990 by FUJITSU LIMITED and Fujitsu Microelectronics, Inc

# 51

#### **ELECTRICAL CHARACTERISTICS**

#### ABSOLUTE MAXIMUM RATINGS1

Rating		Symbol	Minimum	Maximum	Unit		
Supply Voltage		V <sub>DD</sub>	V <sub>SS</sub> <sup>2</sup> -0.5	6.0	V		
Input Voltage		nput Voltage		Vi	V <sub>SS</sub> <sup>2</sup> -0.5	V <sub>DD</sub> +0.5	V
Output Voltage		Vo	V <sub>SS</sub> <sup>2</sup> -0.5	V <sub>DD</sub> +0.5	V		
Storage Temperature	Ceramic Plastic	T <sub>stg</sub>	-65 -40	+150 +125	°C		
Temperature Under Bias	Ceramic Plastic	T <sub>bias</sub>	-40 -25	+125 +85	°C		

Notes: ¹Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
²V<sub>SS</sub> = 0 V.

#### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V <sub>DD</sub>	4.75	5.0	5.25	V
Input High Voltage for Normal Input	V <sub>IH</sub>	2.2	_	_	V
Input Low Voltage for Normal Input	V <sub>IL</sub>	_		0.8	V
Input High Voltage for CMOS Input	V <sub>IH</sub>	V <sub>DD</sub> x 0.7	_	_	ν
Input Low Voltage for CMOS Input	V <sub>IL</sub>	_	_	V <sub>DD</sub> x 0.3	V
Operating Temperature	TA	ó	_	70	°C

## CAPACITANCE ( $T_A = 25$ °C, $V_{DD} = V_I = VO$ , F = 1 MHZ)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Pin Capacitance	C <sub>IN</sub>	_	_	16	pF
Output Pin Capacitance	C <sub>OUT</sub>	_	_	16	ρF
I/O Pin Capacitance	C <sub>VO</sub>	_	_	16	pF

# **ELECTRICAL CHARACTERISTICS** (Continued)

#### DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Current	I <sub>DDS</sub>	Steady State <sup>1</sup>	_	_	0.2	mA
Output High Voltage for Normal Output (I <sub>OL</sub> = 3 mA)	V <sub>OH</sub>	1 <sub>OH</sub> = -2 mA	4.0	_	V <sub>DD</sub>	٧
Output High Voltage for Driver Output (I <sub>OL</sub> = 12 mA)	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	4.0	_	V <sub>DD</sub>	٧
Output Low Voltage for Normal Output	V <sub>OL</sub>	I <sub>OH</sub> = 3.2 mA	V <sub>SS</sub>	_	0.4	٧
Output Low Voltage for Driver Output	V <sub>OL</sub>	l <sub>OH</sub> = 12.0 mA	V <sub>SS</sub>		0.4	٧
Input High Voltage for Normal Input	V <sub>IH</sub>	_	2.2		_	٧
Input Low Voltage for Normal INput	V <sub>IL</sub>	_	_	_	0.8	٧
Input High Voltage for CMOS Input	V <sub>IH</sub>	_	V <sub>DD</sub> x 0.7	_	_	V
Input Low Voltage for CMOS Input	V <sub>IL</sub>		_	_	V <sub>DD</sub> x 0.3	٧
Input Leakage Current	ել	$V_I = 0V - V_{DD}$	-10	****	10	μΑ
Input Leakage Current	I <sub>LZ</sub>	3-state V <sub>I</sub> = 0V - V <sub>DD</sub>	-10		10	μΑ
Input Pull-up/Down Resistor	R <sub>P</sub>	V <sub>IH</sub> = V <sub>DD</sub> V <sub>OL</sub> = V <sub>SS</sub>	25	50	100	kΩ

Note:  ${}^{1}V_{IH} = V_{DD}$ ,  $V_{IL} = V_{SS}$ , and RAM inactive.

#### **AC CHARACTERISTICS**

(Recommended Operating Conditions unless otherwise noted)

Rating	Symbol	Minimum	Maximum <sup>2</sup>	Unit		
Propagation Delay Time	t <sub>PLH</sub>					
Propagation Delay Time	t <sub>PHL</sub>	(Typ) x 0.40 <sup>1</sup>	(Typ) x 1.60 <sup>1</sup>	ns		
	t <sub>PZL</sub>					
Enable Time	t <sub>PZH</sub>					
Disable Time	t <sub>PLZ</sub>					
	t <sub>PHZ</sub>					

Notes: ¹Values for post-layout simulation, with 0°C < Tj ≤ 70°C (Tj: Estimated Junction Temperature). 0.35 and 1.70 are used for pre-layout simulation.

<sup>2</sup>This value is determined by the junction temperature, which is a function of power dissipation, thermal resistance of the selected package, and operating environment (power supply voltage and ambient temperature). Please refer to Chapter 5 of this section or the Design Manual for the details.

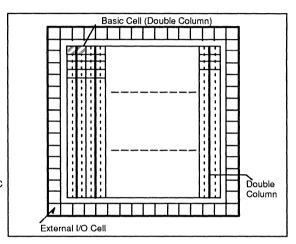
#### **CHIP STRUCTURE**

#### **CHIP LAYOUT**

On the CG21 gate array chip, the basic cells are configured in a matrix arranged in double parallel columns with no wiring channel between the double columns. External I/O cells are located around the basic cell matrix. Interconnection wires go over and across the columns of basic cells.

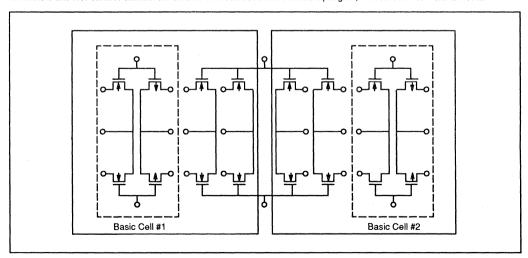
The structure of each device type is as follows:

C-10KAU	48 rows x 213 columns	= 10,224 BC
C-15KAU	58 rows x 267 columns	= 15,486 BC
C-20KAU	68 rows x 307 columns	= 20,876 BC
C-30KAU	84 rows x 375 columns	= 31,500 BC
C-40KAU	96 rows x 429 columns	= 41,184 BC
C-50KAU	108 rows x 483 columns	= 52,164 BC
C-75KAU	130 rows x 578 columns	= 75,140 BC
C-100KAU	152 rows x 672 columns	= 102,144 BC



#### **CELL STRUCTURE**

The basic cell is the structural element of the AU gate arrays. One basic cell consists of two pairs of P-channel and N-channel transistors and four small N-channel transistors. One basic cell can form a 2-input gate, 1 bit for RAM or 4 bits for ROM.



# **UNIT CELL AC CHARACTERISTICS**

(Representative Values for Respresentative Unit Cells)

		<u> </u>		Propagation Delays (in ns)					
Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Output Transition		NDI (Fan-out)				
ranction	1101110	Gate Count	Hansilion	1	2	3	4	5	
Inverter	V1N	1	L→H H→L	0.58 0.55	0.83 0.72	1.08 0.86	1.29 0.97	1.48 1.07	
Power Inverter	V2B	1	L → H H → L	0.39 0.39	0.52 0.52	0.66 0.66	0.77 0.74	0.87 0.80	
2-Input NAND	N2N	1	$L \rightarrow H$ $H \rightarrow L$	0.65 0.75	0.90 0.96	1.15 1.17	1.36 1.34	1.55 1.51	
Power 2-Input NAND	N2B	3	L → H H → L	1.07 1.22	1.20 1.28	1.34 1.34	1.45 1.39	1.55 1.43	
Power 2-Input NAND	N2K	2	L → H H → L	0.49 0.53	0.62 0.67	0.76 0.81	0.87 0.91	0.97 1.00	
3-Input NAND	N3N	2	L → H H → L	0.77 0.95	1.02 1.24	1.27 1.53	1.48 1.77	1.67 1.99	
Power 3-Input NAND	N3B	3	L → H H → L	1.22 1.44	1.35 1.50	1.49 1.56	1.60 1.61	1.70 1.65	
2-Input NOR	R2N	1	L → H H → L	0.94 0.60	1.38 0.75	1.82 0.89	2.19 1.00	2.53 1.10	
Power 2-Input NOR	R2B	3	L → H H → L	1.28 1.08	1.41 1.14	1.55 1.20	1.66 1.25	1.76 1.29	
Power 2-Input NOR	R2K	2	L → H H → L	0.66 0.50	0.87 0.59	1.08 0.69	1.25 0.77	1.42 0.84	
3-Input NOR	R3N	2	L → H H → L	1.56 0.64	2.19 0.81	2.82 0.95	3.35 1.06	3.84 1.16	
Power 3-Input NOR	R3B	3	L → H H → L	1.78 1.18	1.91 1.24	2.05 1.30	2.16 1.35	2.26 1.39	
4-Input NOR	R4N	2	L → H H → L	2.15 0.67	2.97 0.85	3.79 0.99	4.48 1.10	5.12 1.20	
Power 4-Input NOR	R4B	4	L → H H → L	2.19 1.15	2.32 1.21	2.46 1.27	2.57 1.32	2.67 1.36	
Non–SCAN Power D FF (CK→ Q)	FD2	7	L → H H → L	1.51 1.60	1.64 1.75	1.78 1.90	1.89 1.99	1.99 2.05	
SCAN 1-Input D FF with Clock Inhibit (CK $\rightarrow$ Q)	SDA	12	L → H H → L	2.74 2.59	2.87 2.72	3.01 2.86	3.12 2.93	3.22 2.97	

Note: Typical at V<sub>DD</sub> = 5 V and Tj = 25°C Estimated metal loading for C-30KAU (Level 4, Main Block)

## **INPUT BUFFER AC CHARACTERISTICS**

				Propagation Delays				
Unit Cell Function	Unit Cell Name			DI (Fan-ou	(Fan-out)			
ranotion				1	2	3	4	5
Input Buffer (True)	I2B	4	L → H H → L	0.93 1.55	0.99 1.61	1.05 1.67	1.10 1.72	1.14 1.76
Clock Input Buffer (True)	ILB	6	L → H H → L	1.82 2.48	1.84 2.50	1.86 2.52	1.87 2.53	1.89 2.55

Note: Typical at V<sub>DD</sub> = 5 V and Tj = 25°C Estimated metal loading for C-30KAU

## **OUTPUT BUFFER AC CHARACTERISTICS**

Unit Cell	Unit Cell	Faulusland	Output		Pro	pagation De	elays	
Function	Name	Equivalent Gate Count	Transition	C <sub>L</sub> = 10 pF	C <sub>L</sub> = 20 pF	C <sub>L</sub> = 30 pF	C <sub>L</sub> = 40 pF	C <sub>L</sub> = 50 pF
Output Buffer (True)	O2B	2	L → H H → L	1.93 2.56	2.40 3.59	2.87 4.62	3.34 5.65	3.81 6.68
Power Output Buffer (True)	O2L	2	$H \rightarrow H$ $H \rightarrow L$	2.18 2.37	2.50 2.71	2.82 3.05	3.14 3.39	3.46 3.73
3-state Output Buffer (True)	O4T	4	L → H H → L	2.79 3.63	3.26 4.66	3.73 5.69	4.20 6.72	4.67 7.75
Power 3-state Output Buffer (True)	O4W	4	L → H H → L	3.02 5.15	3.34 5.51	3.66 5.87	3.98 6.23	4.30 6.59

NOTE: Typical at V = 5 V and Tj = 25°C
Estimated metal loading for C-30KAU

# **AU CMOS Gate Array Package Options**

		DEVICE NAME								
Package Name	Package Material	C-10KAU	C-15KAU	C-20KAU	C-30KAU	C-40KAU	C-50KAU	C-75KAU	C-100KAU	
PGA-64	Ceramic	•	•	•	_			_	_	
PGA-88	Ceramic	•	•	•	_				_	
PGA-135	Ceramic	•	•	•	•	•	•	•	•	
PGA-179	Ceramic		-	•	•	•	•	•	•	
PGA-208	Ceramic	_		_	•	•	•	•	•	
PGA-256	Ceramic		_	_	_	•	•	•	•	
PGA-299	Ceramic	_					0	0	0	
PGA-321	Ceramic	-		_	_			0	0	
PGA-361	Ceramic		_	_	_	_		0	0	
PGA-401	Ceramic	_				_	_	_	0	
QFP-64	Plastic	•	•	•			_	_	_	
QFP-80	Plastic	•	•	•	-		_	_		
QFP-100	Plastic	•	•	•		_	_	_		
QFP-120	Plastic	•	•	•	•	•				
QFP-160	Plastic		•	•	•	•	_	_	_	
PLCC-68	Plastic	•	•	4	_		_	_	_	
PLCC-84	Plastic	•	•	•				_	_	
SDIP-64	Plastic	•	•	•		_	_	_	_	

Note:

• = Available

o = Under Development

-- = Not Available

# **AU CMOS Gate Array Package Descriptions**

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
SDIP-64	Plastic	None	70 mil Lead Pitch	None	C-20KAU C-15KAU C-10KAU	80 80 85	50 55 60
PLCC-68	Plastic	None	70 mil Lead Pitch Gull-wing	None	C-20KAU C-15KAU C-10KAU	50 55 60	35 40 40
PLCC-84	Plastic	None	30 mil Lead Pitch Gull-wing	None	C-20KAU C-15KAU C-10KAU	50 50 55	35 35 40
QFP-64	Plastic	None	100 mil Lead Pitch Gull-wing	None	C-20KAU C-15KAU C-10KAU	80 85 90	55 60 65
QFP-80	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	C-20KAU C-15KAU C-10KAU	80 85 90	55 60 65
QFP-100	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	C-20KAU C-15KAU C-10KAU	80 85 90	55 60 65
QFP-120	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	C-40KAU C-30KAU	65	40
					C-20KAU C-15KAU	70	50
					C-10K		
QFP-160	Plastic	None	0.65 mm Lead Pitch Gull-wing	Yes	C-40KAU C-30KAU	59	39
					C-20KAU C-15KAU	70	50
PGA-64	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C-10KAU C-15KAU C-20KAU	40	20
PGA-88	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C-10KAU C-15KAU C-20KAU	40	20
PGA-135	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	All AU	30	15
PGA-179	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C-30KAU- C-100KAU	25	13
					C-20KAU	30	15
PGA-208	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C-30KAU- C-100KAU	23	12

# AU CMOS Gate Array Package Descriptions (Continued)

Package -	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
PGA-256	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C-30KAU- C-100KAU	19	9
PGA-299	Ceramic	Down	100 mil Pin Pitch Through hole	Yes	C-50KAU- C-100KAU	19	9
PGA-321	Ceramic	Down	70 mil Stagger Through hole	Yes	C-75KAU- C-100KAU	22-24	11-13
PGA-361	Ceramic	Down	70 mil Stagger Through hole	Yes	C-75KAU- C-100KAU	22-24	11-13
PGA-401	Ceramic	Down	70 mil Stagger Through hole	Yes	C-100KAU	22-24	11-13

## **FUNCTIONAL INDEX OF UNIT CELL LIBRARY**

Note: The load unit (lu) is a normalized loading unit of capacitance representing the input load of an inverter without metal interconnection.

werter and Buff	er Family				
Unit Celi Name	Description		Basic Cells	Drive (Iu)	Polarity
V1N	Inverter		1	18	Neg
V2B	Power Inverter		1	36	Neg
V1L	Inverting Clock Buffer		2	55	Neg
B1N	True Buffer		1	18	Pos
BD3	True Delay Buffer	(> 5 ns)	5	18	Pos
BD4	Delay Cell	(> 4 ns)	4	6	Pos
BD5	Delay Cell	(>10 ns)	9	18	Pos
BD6	Delay Cell	(>22 ns)	17	18	Pos
Clock Buffer Fan	nily				
Unit Cell Name	Description		Basic Cells	Drive (lu)	Polarity
K1B	True Clock Buffer		2	36	Pos
K2B	Power Clock Buffer		3	55	Pos
КЗВ	Gated Clock (AND) Buffer		2	36	Pos
K4B	Gated Clock (OR) Buffer		2	36	Pos
K5B	Gated Clock (NAND) Buffer		3	36	Neg
KAB	Block Clock (OR) Buffer		. 3	55	Pos
KBB	Block Clock (OR x 10) Buffer		30	. 55	Pos
KDB	Block Clock (OR x 10) Buffer		32	55	Pos
KEB	Block Clock Buffer		23	55	Pos
NAND Family			•		
Unit Cell Name	Description		Basic Cells	Drive (lu)	
N2N	2-input NAND		1	18	
N2B	Power 2-input NAND		3	36	
N2K	Fast Power 2-input NAND		2	36	
N3N	3-input NAND		2	14	
N3B	Power 3-input NAND		3	36	
N4N	4-input NAND		2	10	
N4B	Power 4-input NAND		4	36	
N6B	Power 6-input NAND		5	36	
N8B	Power 8-input NAND		6	36	
N9B	Power 9-input NAND		8	36	1
NCB	Power 12-input NAND		10	36	
NGB	Power 16-input NAND		11	36	

# FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

NOR Family				
Unit Cell Name	Description	Basic Cells	Drive (lu)	
R2N	2-input NOR	1	14	
R2B	Power 2-input NOR	3	36	
R2K	Power 2-input NOR	2	36	
R3N	3-input NOR	2	10	
R3B	Power 3-input NOR	3	36	
R4N	4-input NOR	2	6	
R4B	Power 4-input NOR	4	36	
R6B	Power 6-input NOR	5	36	
R8B	Power 8-input NOR	6	36	
R9B	Power 9-input NOR	8	36	
RCB	Power 12-input NOR	10	36	
RGB	Power 16-input NOR	11	36	
AND Family				
Unit Cell Name	Description	Basic Cells	Drive (lu)	
N2P	Power 2-input AND	2	36	[
N3P	Power 3-input AND	3	36	
N4P	Power 4-input AND	3	36	
N8P	Power 8-input AND	6	36	
OR Family				
Unit Cell Name	Description	Basic Cells	Drive (lu)	
R2P	Power 2-input OR	2	36	
R3P	Power 3-input OR	3	36	
R4P	Power 4-input OR	3	36	
R8P	Power 8-input OR	6	36	
Exclusive NOR/0	OR Family (EXOR/EXNOR)			
Unit Cell Name	Description	Basic Cells	Drive (Iu)	Polarity
X1N	Exclusive NOR	3	18	Neg
X1B	Power Exclusive NOR	4	36	Neg
X2N	Exclusive OR	3	14	Pos
X2B	Power Exclusive OR	4	36	Neg
X3N	3-input Exclusive NOR	5	14	Neg
ХЗВ	Power 3-input Exclusive NOR	6	36	Neg
X4N	3-input Exclusive OR	5	14	Pos
X4B	Power 3-input Exclusive OR	6	36	Pos

# FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Unit Cell	- 1				1
Name		Description	Basic Cells	Drive (Iu)	1
D23		2-wide 2-AND 3-input AOI	2	14	<u> </u>
D14		2-wide 3-AND 4-input AOI	2	14	
D24	2-wide 2-AND 4-input AOI		2	14	
D34		3-wide 2-AND 4-input AOI	2	10	
D36		3-wide 2-AND 6-input AOI	3	10	
D44		2-wide 2-OR 2-AND 4-input AOI	2	10	
Note: AND	O-OR-Inve	rter unit cells are useful in implementing sum-of-pro	oducts (SOP) express	sions.	
OR-AND-In	verter Fa	amily (OAI)			
Unit Cell					
Name		Description	Basic Cells	Drive (lu)	
G23	I	2-wide 2-OR 3-input OAI	2	18	
G14		2-wide 3-OR 4-input OAI	2	10	
G24		2-wide 2-OR 4-input OAI	2	10	
G34		3-wide 2-OR 4-input OAI	2	10	
G44		2-wide 2-AND 2-OR 4-input OAI	2	14	
Note: OR-	AND-Inve	rter unit cells are useful in implementing product-of-	-sums (POS) express	sions.	
Multiplexe	Family				
Unit Cell Name	Туре	Description	Basic Cells	Drive (Iu)	Functio
Name					
T24*	4:1	Power 4, 2 ANDs into 4 NOR Multiplexer	6	36	SOP
	4:1 6:1	Power 4, 2 ANDs into 4 NOR Multiplexer Power 6, 2 ANDs into 6 NOR Multiplexer	6 10	36 36	SOP
T24*					
T24* T26*	6:1	Power 6, 2 ANDs into 6 NOR Multiplexer	10	36	SOP
T24* T26* T28*	6:1 8:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer	10 11	36 36	SOP SOP
T24* T26* T28* T32	6:1 8:1 2:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer	10 11 5	36 36 36	SOP SOP SOP
T24* T26* T28* T32 T33*	6:1 8:1 2:1 3:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer	10 11 5	36 36 36 36	SOP SOP SOP
T24* T26* T28* T32 T33* T34*	6:1 8:1 2:1 3:1 4:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer	10 11 5 7	36 36 36 36 36	SOP SOP SOP SOP
T24* T26* T28* T32 T33* T34* T42	6:1 8:1 2:1 3:1 4:1 2:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer	10 11 5 7 9 6	36 36 36 36 36 36	SOP SOP SOP SOP SOP
T24* T26* T28* T32 T33* T34* T42 T43	6:1 8:1 2:1 3:1 4:1 2:1 3:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer Power 3, 4 ANDs into 3 NOR Multiplexer	10 11 5 7 9 6	36 36 36 36 36 36 36	SOP SOP SOP SOP SOP SOP
T24* T26* T28* T32 T33* T34* T42 T43 T44	6:1 8:1 2:1 3:1 4:1 2:1 3:1 4:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer Power 3, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer	10 11 5 7 9 6 10	36 36 36 36 36 36 36 36	SOP SOP SOP SOP SOP SOP SOP
T24* T26* T28* T32 T33* T34* T42 T43 T44 T54	6:1 8:1 2:1 3:1 4:1 2:1 3:1 4:1 4:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer Power 3, 4 ANDs into 3 NOR Multiplexer Power 3, 4 ANDs into 4 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer Power 2, 2–3–4 ANDs into 4 NOR Multiplexer	10 11 5 7 9 6 10 11	36 36 36 36 36 36 36 36 36	SOP SOP SOP SOP SOP SOP SOP
T24* T26* T28* T32 T33* T34* T42 T43 T44 T54 U24*	6:1 8:1 2:1 3:1 4:1 2:1 3:1 4:1 4:1 4:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer Power 3, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer Power 2, 2–3–4 ANDs into 4 NOR Multiplexer Power 4, 2 OR into 4 NAND Multiplexer	10 11 5 7 9 6 10 11 10 6	36 36 36 36 36 36 36 36 36 36	SOP SOP SOP SOP SOP SOP SOP SOP SOP
T24* T26* T28* T32 T33* T34* T42 T43 T44 T54 U24* U26*	6:1 8:1 2:1 3:1 4:1 2:1 3:1 4:1 4:1 4:1 6:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer Power 3, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer Power 2, 2-3-4 ANDs into 4 NOR Multiplexer Power 4, 2 OR into 4 NAND Multiplexer Power 6, 2 OR into 6 NAND Multiplexer	10 11 5 7 9 6 10 11 10 6	36 36 36 36 36 36 36 36 36 36	SOP SOP SOP SOP SOP SOP SOP SOP SOP POS
T24* T26* T28* T32 T33* T34* T42 T43 T44 T54 U24* U26* U28*	6:1 8:1 2:1 3:1 4:1 2:1 3:1 4:1 4:1 4:1 4:1 6:1 8:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer Power 3, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer Power 4, 2 OR into 4 NOR Multiplexer Power 4, 2 OR into 4 NAND Multiplexer Power 6, 2 OR into 6 NAND Multiplexer Power 8, 2 OR into 8 NAND Multiplexer	10 11 5 7 9 6 10 11 10 6 9	36 36 36 36 36 36 36 36 36 36 36 36	SOP SOP SOP SOP SOP SOP SOP SOP POS POS
T24* T26* T28* T32 T33* T34* T42 T43 T44 T54 U24* U26* U28* U32	6:1 8:1 2:1 3:1 4:1 2:1 3:1 4:1 4:1 4:1 4:1 4:1 4:1 5:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer Power 3, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer Power 4, 2 ANDs into 4 NOR Multiplexer Power 2, 2-3-4 ANDs into 4 NOR Multiplexer Power 4, 2 OR into 4 NAND Multiplexer Power 6, 2 OR into 6 NAND Multiplexer Power 8, 2 OR into 8 NAND Multiplexer Power 8, 2 OR into 8 NAND Multiplexer Power 9, 3 OR into 2 NAND Multiplexer	10 11 5 7 9 6 10 11 10 6 9	36 36 36 36 36 36 36 36 36 36 36 36	SOP SOP SOP SOP SOP SOP SOP SOP POS POS
T24* T26* T28* T32 T33* T34* T42 T43 T44 T54 U24* U26* U28* U32 U33*	6:1 8:1 2:1 3:1 4:1 2:1 3:1 4:1 4:1 4:1 6:1 8:1 2:1 3:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 4 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer Power 3, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer Power 2, 2–3–4 ANDs into 4 NOR Multiplexer Power 4, 2 OR into 4 NAND Multiplexer Power 6, 2 OR into 6 NAND Multiplexer Power 8, 2 OR into 8 NAND Multiplexer Power 9, 3 OR into 2 NAND Multiplexer Power 3, 3 OR into 3 NAND Multiplexer	10 11 5 7 9 6 10 11 10 6 9 11 5	36 36 36 36 36 36 36 36 36 36 36 36 36	SOP SOP SOP SOP SOP SOP SOP SOP POS POS
T24* T26* T28* T32 T33* T34* T42 T43 T44 T54 U24* U26* U28* U32 U33* U34*	6:1 8:1 2:1 3:1 4:1 2:1 3:1 4:1 4:1 4:1 6:1 8:1 2:1 3:1 4:1	Power 6, 2 ANDs into 6 NOR Multiplexer Power 8, 2 ANDs into 8 NOR Multiplexer Power 2, 3 ANDs into 2 NOR Multiplexer Power 3, 3 ANDs into 3 NOR Multiplexer Power 4, 3 ANDs into 3 NOR Multiplexer Power 2, 4 ANDs into 2 NOR Multiplexer Power 3, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 3 NOR Multiplexer Power 4, 4 ANDs into 4 NOR Multiplexer Power 2, 2–3–4 ANDs into 4 NOR Multiplexer Power 4, 2 OR into 4 NAND Multiplexer Power 6, 2 OR into 6 NAND Multiplexer Power 8, 2 OR into 8 NAND Multiplexer Power 9, 3 OR into 2 NAND Multiplexer Power 3, 3 OR into 3 NAND Multiplexer Power 4, 3 OR into 3 NAND Multiplexer Power 4, 3 OR into 3 NAND Multiplexer	10 11 5 7 9 6 10 11 10 6 9 11 5 7	36 36 36 36 36 36 36 36 36 36 36 36 36	SOP

# FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Unit Celi Name	Туре	Description	Basic Cells	Drive (lu)	Selects	Outpu	ı	Bit Width
P24*	2:1	Data Selector	12	36	S, XS	a		4
T2E	2:1	Dual Selector	5	18	s	XQ		2
T2F	2:1	Selector	8	18	S	XQ		4
T2B*	2:1	Selector	2	18	S, XS	XQ		1
T2C*	2:1	Selector	4	18	S, XS	XQ		2
T2D*	2:1	Selector	2	14	S, XS	XQ		1
T5A*	4:1	Selector	5	9	S. XS	XQ.		1
V3A*	1:2	Selector	2	14	S, XS	XQ		1
V3B*	1:2	Dual Selector	4	14	S. XS	<u> </u>		2
Decoders Unit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Active Level Outputs	Enal	ole	
DE2	2:4	Decoder	5	18	Low			
DE3	3:8	Decoder	15	14	Low			
DE4	2:4	Decoder	8	14	Low	Low		
DE6	3:8	Decoder	30	18	Low	1 Higl 2 Low	h '	
Internal B Unit Cell Name	US UNIT	Description	Basic Cells	Drive (lu)	Bus Size	Enat	ole	
B11	<del>                                     </del>	us Driver	5	36	1	Low		
B21	2-bit B	us Driver	9	36	2	2 Low		
B41	4-bit B	us Driver	17	36	4	Low		
B81	8-bit B	us Driver	33	36	8	Low		
B12	1-bit B	lock Bus Driver	7	72	1	Low		
B22	2-bit B	lock Bus Driver	13	72	2	Low		
B42	<u> </u>	lock Bus Driver	25	72	4	Low		
Data Late	h Fami	ly					1	
Unit Cell Name		Description	Basic Cells	Drive (I	u) Enable	Bits	Output	Clear
YL2	Data	Latch with TM	5	36	High	1	a	<del>                                     </del>
YL4	Data	Latch with TM	14	36		4	a	<u> </u>
LTK	Data	Latch	4	18		1	Q, XQ	Async
LTL	Data	Latch with Clear	5	18	Low	1	Q, XQ	Async
LTM	Data	Latch with Clear	16	18	Low	4	Q, XQ	_
LT1	S-R	Latch with Clear	4	18	Low	1	Q, XQ	Async

Note: Y-type latches incorporate inhibit inputs and transparent mode (TM) to facilitate scan implementation.

18

Low

14

Data Latch

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Output	Clear	Preset	Clock inhibit
SDH	Scan D Flip-flop with 2:1 Multiplexed inputs	14	36	1	Q, XQ	Async	<b> </b>	Yes
SDJ	Scan D Flip-flop with 4:1 Multiplexed inputs	15	36	1	Q, XQ	Async		Yes
SDK	Scan D Flip-flop with 3:1 Multiplexed inputs	16	36	1	Q, XQ	Async	_	Yes
SJH	Scan J-K Flip-flop	16	36	1	Q, XQ	Async	_	Yes
SDD	Scan DFlip-flop with 2:1 Multiplexed inputs	16	36	1	Q, XQ	Async	Async	Yes
SDA	Scan 1-input D Flip-flop	12	36	1	Q, XQ			Yes
SDB	Scan 1-input D Flip-flop	42	36	4	Q, XQ			Yes
SHA	Scan 1-input D Flip-flop	68	18	8	Q, XQ	1 —	_	Yes
SHB	Scan 1-input D Flip-flop	62	18	8	Q	T		Yes
SHC	Scan 1-input D Flip-flop	62	18	8	XQ		_	Yes
SHJ	Scan D Flip-flop with 2:1 Multiplexed inputs	78	18	8	Q, XQ	_	-	Yes
SHK	Scan D Flip-flop with 3:1 Multiplexed inputs	88	18	8	Q, XQ		_	Yes
SFDM	Scan 1-input D Flip-flop	10	18	1	Q, XQ, SO	_		Yes
SFDO	Scan 1-input D Flip-flop	11	18	1	Q, XQ, SO	Yes		Yes
SFDP	Scan 1-input D Flip-flop	12	18	1	Q, XQ, SO	Yes	Yes	Yes
SFDR	Scan 4-input D Flip-flop	36	18	4	Q, XQ, SO	Yes		Yes
SFDS	Scan 4-input D Flip-flop	31	18	4	Q, XQ, SO	_		Yes
SFJD	Scan J-K D Flip-flop	14	18	1	Q, XQ, SO	_	_	Yes
Non S	Scan Filp-flop Family							
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs	Clear	Preset	Clock Edge
FDN	Non-Scan D Flip-flop with Set	7	18	1	Q, XQ		Async	Pos
FDM	Non-Scan D F	6	18	1	Q, XQ			Pos
FDO	Non-Scan D Flip-flop with Reset	7	18	1	Q, XQ	Async	-	Pos
FDP	Non-Scan D Flip-flop with Set and Reset	8	18	1	Q, XQ	Async	Async	Pos
FDQ	Non-Scan D Flip-flop	21	18	4	Q		_	Neg
FDR	Non-Scan D Flip-flop	26	18	4	Q	Async	_	Pos
FDS	Non-Scan D Flip-flop	20	18	4	Q			Pos
FD2	Non-Scan Power D Flip-flop	7	36	1	Q, XQ			Neg
FD3	Non-Scan Power D Flip-flop	8	36	1	Q, XQ		Async	Neg
	Non-Scan Power D Flip-flop	9	36	1	Q, XQ	Async	Async	Neg
FD4					2 1/2	A		
FD4 FD5	Non-Scan Power D Flip-flop	8	36	1 1	Q, XQ	Async		Neg
		12	36	1	Q, XQ Q, XQ	Async		Po

Note: Synchronous flip-flops may be constructed by adding a simple AND gate (such as N2P) to the input of a flip-flop to create a synchronous clear.

	y Counter Family									
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs <sup>1</sup>	Load	Clear	Enable	Carry In	Up/ Down
SC72	Scan Synchronous Binary				Q, XQ,					I
i	Counter with Parallel Load	62	36	4	CO (S)	Sync	_	Low	High	Up
SC8 <sup>2</sup>	Scan Synchronous Binary				Q, XQ,					
- 1	Counter with Parallel Load	66	36	4	CO (S)	Sync	_	High	Low	Down
C113	Non-Scan Flip-flop for Counter	11	18		Q, XQ	_		_	_	1=
C41	Non-Scan Binary									
1	Asynchronous Counter	24	18	4	Q, (A)		Async	l –	_	Up
C42	Non-Scan Binary			1						
	Synchronous Counter	32	18	4	a	_	Async	-	_	Up
C43	Non-Scan Binary									
	Synchronous Counter	48	18	4	Q, CO(S)	Sync	Async	High	High	Up
C45	Non-Scan Binary Synchronous									
	Counter	48	18	4	Q, CO	Sync	Sync	High	High	Up
C47	Non-Scan Binary Synchronous Counter	68	18	4	Q, CO	Async		Low	Low	Up/Dow
SC43 <sup>2</sup>	Scan synchronous Binary Counter	59	18	4	Q, CO	Sync	Async	High	High	Up
SC472	Scan synchronous Binary Counter	78	18	4	Q, CO	Async	_	Low	Low	Up/Dow

Notes:

(S), (A) indicate the counter is (S)ynchronous or (A)synchronous. Scan counters include clock inhibit and high drive ( $C_{DR} = 36 \text{ lu}$ ). For non-Scan counters  $C_{DR} = 18 \text{ lu}$  C11 may by used for purposes other than counters.

#### Shift Begister Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bit Width	Load	Outputs	Clock Polarity
FS1	Serial-in Parallel-out Shift						
l	Register	18	16	4	Serial-In only	Q-Parallel	Neg
FS2	Shift Register with						
- 1	Synchronous Load	30	16	4	Sync-High	Q-Parallel	Neg
FS3	Shift Register with						
	Asynchronous Load	34	18	4	Async-Low	Q-Parallel	Pos
SR1	Serial-in Parallel-out Shift						
- 1	Register with Scan	36	36	4	Serial-In only	Q-Parallel	Pos

### Datapath Operators (Adder, ALU, Parity)

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bit Width	Outputs	Carry In
MC4	Magnitude Comparator	42	18 (=) 10(<,>)	4	A>B, A=B, A <b< td=""><td>A&gt;B,A=B,ALB</td></b<>	A>B,A=B,ALB
A1A	1-bit Half Adder	5	36	1	S, CO	
A1N	1-bit Full Adder	8	18	1	S, CO	CI
A2N	2-bit Full Adder	16	14	2	S, CO	CI
A4H	4-bit Binary Full Adder w/Fast Carry	48	18(CO) 14(S)	4	s, co	CI
PE5	Even Parity Generator/Checker	12	36	5	EVEN, ODD	
PO5	Odd Parity Generator/Checker	12	36	5	ODD, EVEN	
PE8	Even Parity Generator/Checker	18	18	8	EVEN, ODD	
PO8	Odd Parity Generator/Checker	18	18	8	ODD, EVEN	<u> </u>
PE9	Even Parity Generator/Checker	22	18	9	EVEN, ODD	
PO9	Odd Parity Generator/Checker	22	18	9	ODD, EVEN	_

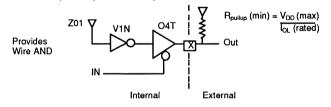
Miscella	aneous Cells					
Unit Cell		Basic				
Name	Description	Cells			Function	
Z00	0 Clip	0			Tie to V <sub>SS</sub>	
Z01	1 Clip	0			Tie to V <sub>DD</sub>	
Input B	uffer Family					
Unit Cell Name	- Description	Basic Cells	Drive (lu)	Logic Level	Туре	Input/ Output Polarity
I1B	Input Buffer	5	36	TTL	Signal	Invert
I1BU	I1B with Pull-up Resistance	5	36	TTL	Signal	Invert
I1BD	I1B with Pull-down Resistance	5	36	TTL	Signal	Invert
I2B	Input Buffer	4	36	TTL	Signal	True
I2BU	I2B with Pull-up Resistance	4	36	TTL	Signal	True
I2BD	I2B with Pull-down Resistance	4	36	ΠL	Signal	True
IKB	Clock Input Buffer	4	72	TTL	Clock	Invert
IKBU	Ikb With Pull-up Resistance	4	72	TTL	Clock	Invert
IKBD	IKB with Pull-down Resistance	4	72	TTL	Clock	Invert
ILB	Clock Input Buffer	6	72	TTL	Clock	True
ILBU	ILB with Pull-up Resistance	6	72	TTL	Clock	True
ILBD	ILB with Pull-down Resistance	6	72	TTL	Clock	True
I1C	CMOS Interface Input Buffer	5	36	CMOS	Signal	Invert
I1CU	I1C with Pull-up Resistance	5	36	CMOS	Signal	Invert
I1CD	I1C with Pull-down Resistance	5	36	CMOS	Signal	Invert
I2C	CMOS Interface Input Buffer	4	36	CMOS	Signal	True
I2CU	I2C with Pull-up Resistance	4	36	CMOS	Signal	True
I2CD	I2C with Pull-down Resistance	4	36	CMOS	Signal	True
I1S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	Invert
I1SU	I1S with Pull-up Resistance	8	18	CMOS	Schmitt	Invert
I1SD	I1S with Pull-down Resistance	8	18	CMOS	Schmitt	invert
128	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	True
I2SU	I2S with Pull-up Resistance	8	18	CMOS	Schmitt	True
I2SD	I2S with Pull-down Resistance	8	18	CMOS	Schmitt	True
IIR	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	Invert
I1RU	I1R with Pull-up Resistance	8	18	TTL	Schmitt	Invert
I1RD	I1R with Pull-down Resistance	8	18	TTL	Schmitt	Invert
I2R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	True
I2RU	I2R With Pull-up Resistance	8	18	TTL	Schmitt	True
I2RD	I2R with Pull-down Resistance	8	18	TTL	Schmitt	True
IKC	Clock Input Buffer	4	200	CMOS	Clock	Invert
IKCU	IKC with Pull-up Resistance	4	200	CMOS	Clock	Invert
IKCD	IKC with Pull-down Resistance	4	200	CMOS	Clock	Invert
ILC	Clock Input Buffer	6	200	CMOS	Clock	True
ILCU	IKC with Pull-up Resistance	6	200	CMOS	Clock	True
ILCD	IKC with Pull-down Resistance	6	200	CMOS	Clock	True

Note: A "U" suffixed to the name of an input buffer indicates pull-up resistance of  $50K\Omega$  (typical) and a "D" indicates a pull-down resistance of the equivalent value.

Output	Buffer Family						
Unit Cell Name	Description	Basic Cells	Drive (I <sub>OL</sub> )	Logic <sup>2</sup> Level	Туре	Edge Rate Control	Input/ Output Polarity
O1B	Output Buffer	3	3.2 mA	TTL/CMOS	Standard	No	Invert
O1L	Power Output Buffer	3	12 mA	TTL/CMOS	Standard	No	Invert
O1S	Power Output Buffer	5	12 mA	TTL/CMOS	Standard	Yes	Invert
O2B	Output Buffer	2	3.2 mA	TTL/CMOS	Standard	No	True
O2L	Power Output Buffer	2	12 mA	TTL/CMOS	Standard	No	True
O2S	Power Output Buffer	4	12 mA	TTL/CMOS	Standard	Yes	True
O44 <sup>1</sup>	3-state Output Buffer	4	3.2 mA	TTL/CMOS	3-state	No	True
O4W <sup>1</sup>	Power 3-state Output Buffer	4	12 mA	TTL/CMOS	3-state	No	True
O4S <sup>1</sup>	Power 3-state Output Buffer	5	12 mA	TTL/CMOS	3-state	Yes	True
O1R	Output Buffer	5	3.2 mA	TTL/CMOS	Standard	Yes	Invert
O2R	Output Buffer	4	3.2 mA	TTL/CMOS	Standard	Yes	True
O4R <sup>1</sup>	3-state Output Buffer	5	3.2 mA	TTL/CMOS	3-state	Yes	True
O2BF	Output Buffer	2	8 mA	TTL/CMOS	Standard	No	True
O2RF	Output Buffer	4	8 mA	TTL/CMOS	Standard	Yes	True
O4RF	3-state Output Buffer	5	8 mA	TTL/CMOS	3-state	Yes	True
O4TF	3-state Output Buffer	4	8 mA	TTL/CMOS	3-state	No	True

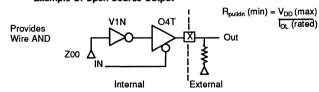
- Notes: 1. While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs
  - Totem pole outputs, such as these buffers have, can drive both TTL and CMOS levels. Voltage margins depend on actual source or sink current (see DC specifications).

### **Example of Open Drain Output**



In	X	Out
0 1	L Z	L

### **Example Of Open Source Output**



<u>In</u>	Х	Out
0	H Z	H

Bidirec	tional I/O Buffers (Buses)					
Unit Cell Name	Description	Basic Cells	Drive (I <sub>OL</sub> )	Logic Level	Edge Rate Control	Input/ Output Polarity
H6T	3-state Output and Input Buffer	8	3.2 mA	TTL	No	True
H6TU	H6T with Pull-up Resistance	8	3.2 mA	TTL	No	True
H6TD	H6T with Pull-down Resistance	8	3.2 mA	TTL	No	True
H6W	Power 3-state Output and Input Buffer	8	12 mA	TTL	No	True
H6WU	H6W with Pull-up Resistance	8	12 mA	TTL	No	True
H6WD	H6W with Pull-down Resistance	8	12 mA	TTL	No	True
H6C	3-state Output and	1				
	Interface Input Buffer	8	3.2 mA	CMOS	No	True
H6CU	H6C with Pull-up Resistance	8	3.2 mA	CMOS	No	True
H6CD	H6C with Pull-down Resistance	8	3.2 mA	CMOS	No	True
H6E	Power 3-state Output and	1				
	Interface Input Buffer	8	12 mA	CMOS	No	True
H6EU	H6E with Pull-up Resistance	8	12 mA	CMOS	No	True
H6ED	H6E with Pull-down Resistance	8	12 mA	смоѕ	No	True
H6S	3-state Output and Schmitt					
	Trigger Input Buffer	12	3.2 mA	CMOS	No	True
H6SU	H6S with Pull-up Resistance	12	3.2 mA	CMOS	No	True
H6SD	H6S with Pull-down Resistance	12	3.2 mA	CMOS	No	True
H6R	3-state Output and Schmitt					
	Trigger Input Buffer	12	3.2 mA	TTL	No	True
H6RU	H6R with Pull-up Resistance	12	3.2 mA	TTL	No	True
H6RD	H6R with Pull-down Resistance	12	3.2 mA	TTL	No	True
H8T	3-state Output and Input Buffer	9	3.2 mA	TTL	Yes	True
H8TU	H8T with Pull-up Resistance	9	3.2 mA	TTL	Yes	True
H8TD	H8T with Pull-down Resistance	9	3.2 mA	TTL	Yes	True
H8W	Power 3-state Output and Input Buffer	9	12 mA	TTL	Yes	True
H8WU	H8W with Pull-up Resistance	9	12 mA	TTL	Yes	True
H8WD	H8W with Pull-down Resistance	9	12 mA	TTL	Yes	True
H8C	3-state Output Buffer and					
	Interface Input Buffer	9	3.2 mA	CMOS	Yes	True
H8CU	H8C with Pull-up Resistance	9	3.2 mA	CMOS	Yes	True
H8CD	H8C with Pull-down Resistance	9	3.2 mA	CMOS	Yes	True

Note: A "U" suffixed to the name of a bidirectional buffer indicates a pull-up resistance of  $50\Omega$  (typical) and a "D" indicates a pull-down resistance of the equivalent value.

Bldirec	tional I/O Buffers (Buses) continue	d				
Unit Cell Name	Description	Basic Cells	Drive (I <sub>OL</sub> )	input Logic Level	Edge Rate Control	Input/ Output Polarity
H8E	Power 3-state Output Buffer and					
	Interface Input Buffer	9	12 mA	CMOS	Yes	True
H8EU	H8E with Pull-up Resistance	9	12 mA	CMOS	Yes	True
H8ED	H8E with Pull-down Resistance	9	12 mA	CMOS	Yes	True
H8S	3-state Output and Schmitt					
	Trigger Input Buffer	13	3.2 mA	CMOS	Yes	True
H8SU	H8S with Pull-up Resistance	13	3.2 mA	CMOS	Yes	True
H8SD	H8S with Pull-down Resistance	13	3.2 mA	CMOS	Yes	True
H8R	3-state Output and Schmitt					
	Trigger Input Buffer	13	3.2 mA	TTL	Yes	True
H8RU	H8R with Pull-up Resistance	13	3.2 mA	TTL	Yes	True
H8RD	H8R with Pull-down Resistance	13	3.2 mA	TTL	Yes	True
H6TF	3-state Output and Schmitt					
	Trigger Input Buffer	8	8 mA	TTL	No	True
H6TFU	H6TF with Pull-up Resistance	8	8 mA	TTL	No	True
H6TFD	H6TF with Pull-down Resistance	8	8 mA	TTL	No	True
H6CF	3-state Output and Input Buffer	8	8 mA	CMOS	No	True
H6CFU	H6CF with Pull-up Resistance	8	8 mA	CMOS	No	True
H6CFD	H6CF with Pull-down Resistance	8	8 mA	CMOS	No	True
H8TF	3-state Output and Input Buffer	9	8 mA	TTL	Yes	True
H8TFU	H8TF with Pull-up Resistance	9	8 mA	TTL	Yes	True
H8TFD	H8TF with Pull-down Resistance	9	8 mA	TTL	Yes	True
H8CF	3-state Output and Input Buffer	9	8 mA	CMOS	Yes	True
H8CFU	H8CF with Pull-up Resistance	9	8 mA	CMOS	Yes	True
H8CFD	H8CF with Pull-down Resistance	9	8 mA	CMOS	Yes	True
H8W2	3-state Output and Input Buffer	8	24 mA	TTL	Yes	True
H8W1	H8W2 with Pull-up Resistance	8	24 mA	TTL	Yes	True
H8W0	H8W2 with Pull-down Resistance	8	24 mA	TTL	Yes	True
H8E2	3-state Output and Input Buffer	8	24 mA	CMOS	Yes	True
H8E1	H8E2 with Pull-up Resistance	8	24 mA	CMOS	Yes	True
H8E0	H8E2 with Pull-down Resistance	8	24 mA	CMOS	Yes	True

Note: While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs, which includes all bidirectional buffers.

# DESCRIPTION

The CG21 series of 0.8 µm CMOS gate arrays are currently available in five device types with from 30K to 100K gates. Three more CG21 arrays, ranging from 10K to 20K gates, are now under development. These arrays achieve the ultra fast speed of 0.37 ps per gate. Thanks to the channel-free (sea-of-gates) structure of the CG21 gate array, CG21 basic cells can be used for logic cells, memory cells, or wiring area in order to implement the desired functions. The full utilization of the array surface and the three-layer metal interconnect technology produce a 75 percent maximum gate usability ratio.

The logic and I/O cells for the CG21 series are functionally compatible with Fujitsu's AU, UHB, and CG10 series of gate arrays to simplify upgrading. User-specifiable RAM and ROM configurations are also available. These gate arrays facilitate the implementation of large-scale devices such as computer and graphic processors on single chips.

#### **FEATURES**

- 0.8 micron CMOS sea-of-gates technology -3 laver metal interconnect
- Ultra high speed
  - 0.37 ns/gate for 2-input NAND with F/O = 2
  - 0.55 ns/gate for power 2-input NAND with F/O = 2
- High basic cell usage
  - 75% maximum for logic with RAM/ROM
  - 45% maximum for logic only
- · High sink current capability
  - sink current up to 12 mA, 24 mA planned
- Minimum delay clock buffer true option

- High current clock drivers
  - -Low-skew clock signal distribution
- Extensive unit cell library (logic cell, RAM, ROM) -Unit cells functionally compatible with Fuiltsu's AU. UHB, and CG10 gate array series
- Automatic test pattern generation optional
- On-chip pull-up/pull-down resistors
- High pin count plastic and ceramic packages
- High-density RAM and ROM compilers
  - up to 18K bit RAM compilation
  - up to 64K ROM compilation

### **PRODUCT FAMILY**

	Part	BCs on Chip (2-input gate		Max Signal	Available Pa	ckages <sup>1</sup>
Device	Number	+4 N-ch Tr)	Usable BCs	I/O	Plastic	Ceramic
CG21103	MBCG21103xxx <sup>3</sup>	10,224		108	SDIP-64, QFP-64, -80, -100, -120, PLCC-68, -84	PGA-64, 88, -135
CG21153	MBCG21153xxx <sup>3</sup>	15,486	75% max. for Logic with	142	SDIP-64, QFP-64, -80 -100, -120, -160, PLCC-68, -84	PGA-64, -88, -135
CG21203	MBCG21203xxx <sup>3</sup>	20,876	RAM,ROM	155	SDIP-64, QFP-64, -80, -100, -120, -160, PLCC-68, -84	PGA-64, -88, -135, -179
CG21303	MBCG21303xxx	31,500	45% max. for Logic only	178	QFP-120, -160	PGA-88, -135, -179, 208
CG21403	MBCG21403xxx	41,184	(Preliminary	220	QFP-120, -160 SQFP-176 <sup>2</sup> , -208 <sup>2</sup>	PGA-135, -179, 208, -256
CG21503	MBCG21503xxx	52,164	values, to be upgraded)	245	QFP-120, -160, -196 <sup>2</sup> SQFP-176 <sup>2</sup> , -208 <sup>2</sup>	PGA-135, -179, 208, -256, -299 <sup>2</sup>
CG21753	MBCG21753xxx	75,140		284	QFP-196 <sup>2</sup> , -232 <sup>2</sup> SQFP-176 <sup>2</sup> , -208 <sup>2</sup>	PGA-135, -179, 208, -256, -299 <sup>2</sup> , -321 <sup>2</sup> , -361 <sup>2</sup>
CG21104	MBCG21104xxx	102,144		332	QFP-196 <sup>2</sup> , -232 <sup>2</sup> SQFP-208 <sup>2</sup> , -256 <sup>2</sup>	PGA-135, -179, 208, -256, -299, -321 <sup>2</sup> , -361, -401 <sup>2</sup>

SDIP = Skinny dual in-line package, PGA = Pin grid array, QFP = Quad flat package, PLCC = Plastic leadless chip carrier, SQFP = Skinny quad flat package <sup>2</sup>Planned

<sup>3</sup>Under development

### **ELECTRICAL CHARACTERISTICS**

#### ABSOLUTE MAXIMUM RATINGS1

Rating		Symbol	Minimum	Maximum	Unit
Supply Voltage		V <sub>DD</sub>	V <sub>SS</sub> <sup>2</sup> -0.5	6.0	V
Input Voltage		Vı	V <sub>SS</sub> <sup>2</sup> -0.5	V <sub>DD</sub> +0.5	V
Output Voltage		Vo	V <sub>SS</sub> <sup>2</sup> -0.5	V <sub>DD</sub> +0.5	V
Storage Temperature	Ceramic Plastic	T <sub>stg</sub>	-65 -40	+150 +125	°C
Temperature Under Bias	Ceramic Plastic	T <sub>bias</sub>	-40 -25	+125 +85	°C

Notes: ¹Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
²V<sub>SS</sub> = 0 V.

#### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V <sub>DD</sub>	4.75	5.0	5.25	٧
Input High Voltage for Normal Input	V <sub>IH</sub>	2.2	_		V
Input Low Voltage for Normal Input	V <sub>IL</sub>	_		0.8	V
Input High Voltage for CMOS Input	V <sub>IH</sub>	V <sub>DD</sub> x 0.7		_	٧
Input Low Voltage for CMOS Input	V <sub>IL</sub>			V <sub>DD</sub> x 0.3	٧
Operating Temperature	T <sub>A</sub>	0		70	°C

### CAPACITANCE ( $T_A = 25$ °C, $V_{DD} = V_I = VO$ , F = 1 MHZ)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Pin Capacitance	C <sub>IN</sub>	_		16	pF
Output Pin Capacitance	C <sub>OUT</sub>	_	_	16	pF
I/O Pin Capacitance	C <sub>vo</sub>		_	16	pF

### **ELECTRICAL CHARACTERISTICS** (Continued)

#### DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Current	I <sub>DDS</sub>	Steady State <sup>1</sup>	_		0.2	mA
Output High Voltage for Normal Output (I <sub>OL</sub> = 3 mA or 8 mA)	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA	4.0	_	V <sub>DD</sub>	٧
Output High Voltage for Driver Output (I <sub>OL</sub> = 12 mA)	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	4.0	_	$V_{DD}$	٧
Output Low Voltage for Normal Output (I <sub>OL</sub> = 3 mA or 8 mA)	V <sub>OL</sub>	l <sub>OL</sub> = 3.2 mA or 8 mA	V <sub>SS</sub>	_	0.4	٧
Output Low Voltage for Driver Output (I <sub>OL</sub> = 12 mA)	V <sub>OL</sub>	I <sub>OL</sub> = 12.0 mA	V <sub>SS</sub>	_	0.4	٧
Input High Voltage for Normal Input	V <sub>IH</sub>	_	2.2	_	_	٧
Input Low Voltage for Normal INput	V <sub>IL</sub>	_	_		0.8	٧
Input High Voltage for CMOS Input	V <sub>IH</sub>	_	V <sub>DD</sub> x 0.7	_	_	٧
Input Low Voltage for CMOS Input	V <sub>IL</sub>	_	_	_	V <sub>DD</sub> x 0.3	٧
Input Leakage Current	և	$V_1 = 0V - V_{DD}$	-10	_	10	μΑ
Input Leakage Current	I <sub>LZ</sub>	3-state V <sub>I</sub> = 0V - V <sub>DD</sub>	-10	_	10	μА
Input Pull-up/Down Resistor	$R_P$	$V_{IH} = V_{DD}$ $V_{OL} = V_{SS}$	25	50	100	kΩ

Note:  ${}^{1}V_{IH} = V_{DD}$ ,  $V_{IL} = V_{SS}$ , and RAM inactive.

#### **AC CHARACTERISTICS**

(Recommended Operating Conditions unless otherwise noted)

Rating	Symbol	Minimum	Maximum <sup>1</sup>	Unit
Propagation Delay Time	t <sub>PLH</sub>			
1 Topagation Delay Time	t <sub>PHL</sub>			
E. II. E.	t <sub>PZL</sub>	]	(Typ) x 1.55 <sup>2</sup> (Typ) x 1.60 <sup>3</sup>	ns
Enable Time	t <sub>PZH</sub>	(Typ) x 0.40 <sup>2,3</sup>		
Di II Ti	t <sub>PLZ</sub>		(1)p) x 1.00	
Disable Time	t <sub>PHZ</sub>			

Notes: <sup>1</sup>This value is determined by the junction temperature, which is a function of power dissipation, thermal resistance of the selected package, and operating environment (power supply voltage and ambient temperature).

 $<sup>^2</sup>$ Values for post-layout simulation, with Tj  $\leq$  70 $^\circ$ C (Tj: Estimated Junction Temperature.) 0.35 and 1.70 are used for pre-layout simulation.

 $<sup>^3</sup>$ Values for post-layout simulation with Tj  $\leq$  60°C. 0.35 and 1.65 are used for pre-layout simulation.

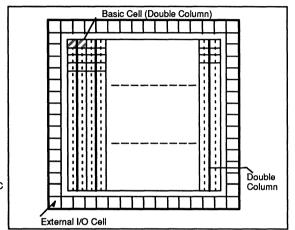
### **CHIP STRUCTURE**

#### **CHIP LAYOUT**

On the CG21 gate array chip, the basic cells are configured in a matrix arranged in double parallel columns with no wiring channel between the double columns. External I/O cells are located around the basic cell matrix. Interconnection wires go over and across the columns of basic cells.

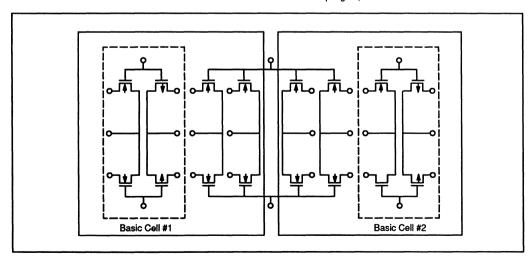
The structure of each device type is as follows:

CG21103	48 rows x 213 columns	= 10,224 BC
CG21153	58 rows x 267 columns	= 15,486 BC
CG21203	68 rows x 307 columns	= 20,876 BC
CG21303	84 rows x 375 columns	= 31,500 BC
CG21403	96 rows x 429 columns	= 41,184 BC
CG21503	108 rows x 483 columns	= 52,164 BC
CG21753	130 rows x 578 columns	= 75,140 BC
CG21104	152 rows x 672 columns	= 102,144 BC



### **CELL STRUCTURE**

The basic cell is the structural element of the CG21 gate arrays. One basic cell consists of two pairs of P-channel and N-channel transistors and four small N-channel transistors. One basic cell can form a 2-input gate, 1 bit for RAM or 4 bits for ROM.



3

## **Package Options**

					DEVIC	E NAME					
Package Name	Package Material	CG21103 (10K)	CG21153 (15K)	CG21203 (20K)	CG21303 (30K)	CG21403 (40K)	CG21503 (50K)	CG21703 (75K)	CG21104 (100K)	Number of V <sub>DD</sub> .	Number of V <sub>SS</sub> .
PGA-64	Ceramic	•	•	•		_	_	_	_	2 (2)	4 (2)
PGA-88	Ceramic	•	•	•					_	4 (4)	6 (4)
PGA-135	Ceramic	•	•	•	•	•	•	•	•	8	12
PGA-179	Ceramic	_	_	•	•	•	•	•	•	8	16
PGA-208	Ceramic	_	_		•	•	•	•	•	12	18
PGA-256	Ceramic	_	_	_	_	•	•	•	•	16	20
PGA-299	Ceramic	_			_	_	0	0	0	21	21
PGA-321	Ceramic	_	_	_	_	_	_	0	0	20	32
PGA-361	Ceramic	_	_	_	_	-	_	0	0	24	36
PGA-401	Ceramic		_			_	_		0	28	40
QFP-64	Plastic	•	•	•	_	_		_	_	2 (2)	4 (2)
QFP-80	Plastic	•	•	•	_	-	_	_		2 (2)	6 (4)
QFP-100	Plastic	•	•	•		_			_	4 (4)	8 (4)
QFP-120	Plastic	•	•	•	•	•	_	_		6 (4)	12 (8)
QFP-160	Plastic	_	•	•	•	•	_	_	-	8 (6)	14 (12)
QFP-196	Plastic	_					0	0	•	10	18
QFP-232	Plastic	_	_		_		_	0	•	14	20
QFP-176	Plastic	<u> </u>	_			0	0	0		8	16
QFP-208	Plastic	_	_	_		0	0	0	0	12	18
QFP-256	Plastic	_	_	_		_		_	0	16	20
PLCC-68	Plastic	•	•	•	_	_	_	_	_	2 (2)	4 (2)
PLCC-84	Plastic	•	•	•					_	4 (2)	6 (4)
SDIP-64	Plastic	•	•	•	_			_	_	2 (2)	4 (2)

Notes:

= Available

O = Under Development

- = Not Available

<sup>\*</sup>The values in parentheses show the number of  $V_{DD}$  and  $V_{SS}$  pins provided in the alternate pin assignment (U-type) packages, which have fewer  $V_{DD}/V_{SS}$  pins than in normally configured packages.

# **Package Descriptions**

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
SDIP-64	Plastic	None	70 mil Lead Pitch	None	CG21103* CG21153* CG21203*	80 80 85	50 55 60
PLCC-68	Plastic	None	70 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	50 55 60	35 40 40
PLCC-84	Plastic	None	30 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	50 50 55	35 35 40
QFP-64	Plastic	None	100 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP-80	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP100	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP-120	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	CG21303 CG21403 CG21503	65	40
					CG21103* CG21153* CG21203*	70	50
QFP-160	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	CG21303 CG21403 CG21503	59	39
					CG21153 CG21253	70	50
QFP-196**	Plastic	None	TBD Gull-wing	None	CG21503 CG21753 CG21104	TBD	TBD
QFP-232**	Plastic	None	TBD Gull-wing	None	CG21753 CG21104	TBD	TBD
QFP-176**	Plastic	None	TBD Gull-wing	None	CG21403 CG21503 CG21753	TBD	TBD
QFP-208**	Plastic	None	TBD Gull-wing	None	CG21403 CG21503 CG21753 CG21104	TBD	TBD
QFP-256**	Plastic	None	TBD Gull-wing	None	CG21104	TBD	TBD

Continued on next page

<sup>\*</sup> planned device \*\*package under development

# Package Descriptions (Continued)

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
PGA-64	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21103* CG21153* CG21203*	40	20
PGA-88	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21103* CG21153* CG21203* CG21303	40	20
PGA-135	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	All CG21	30	15
PGA-179	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21203* CG21303 CG21403 CG21503 CG21753 CG21104	30 25	15 13
PGA-208	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21303 CG21403 CG21503 CG21753 CG21104	23	12
PGA-256	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21403 CG21503 CG21753 CG21104	19	9
PGA-299	Ceramic	Down	100 mil Pin Pitch Through hole	Yes	CG21503 CG21753 CG21104	19	9
PGA-321	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21753 CG21104	22-24	11-13
PGA-361	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21753 CG21104	22-24	11-13
PGA-401	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21104	22-24	11-13

### **FUNCTIONAL INDEX OF UNIT CELL LIBRARY**

Note: The load unit (lu) is a normalized loading unit of capacitance representing the input load of an inverter without metal interconnection.

	fer Family	· · · · · · ·			
Unit Cell Name	Description	Bas	ic Cells	Drive (lu)	Polarity
V1N	Inverter		1	18	Neg
V2B	Power Inverter		1	36	Neg
B1N	True Buffer		1	18	Pos
BD3	True Delay Buffer (>	> 5 ns)	5	18	Pos
BD4	Delay Cell (>	> 4 ns)	4	6	Pos
BD5	Delay Cell (>	>10 ns)	9	18	Pos
BD6	Delay Cell (>	>22 ns)	17	18	Pos
ck Buffer Fan	nily				
Unit Cell Name	Description	Bas	ic Cells	Drive (Iu)	Polarity
K1B	True Clock Buffer		2	36	Pos
K2B	Power Clock Buffer		3	55	Pos
кзв	Gated Clock (AND) Buffer		2	36	Pos
K4B	Gated Clock (OR) Buffer		2	36	Pos
K5B	Gated Clock (NAND) Buffer		3	36	Neg
KAB	Block Clock (OR) Buffer		3	55	Pos
KBB	Block Clock (OR x 10) Buffer		30	55	Pos
KDB	Block Clock (OR x 10) Buffer		32	55	Pos
KEB	Block Clock Buffer		23	55	Pos
V1L	Inverting Clock Buffer		2	55	Neg
ND Family					
Unit Cell Name	Description	Bas	ic Cells	Drive (lu)	
N2N	2-input NAND		1	18	
N2B	Power 2-input NAND		3	36	
N2K	Fast Power 2-input NAND		2	36	1
N3N	3-input NAND		2	14	
N3B	Power 3-input NAND		3	36	
N4N	4-input NAND		2	10	
N4B	Power 4-input NAND		4	36	
N6B	Power 6-input NAND		5	36	
N8B	Power 8-input NAND		6	36	
N9B	Power 9-input NAND		8	36	1
NCB	Power 12-input NAND	1	10	36	

NOR Family				
Unit Cell Name	Description	Basic Cells	Drive (Iu)	
R2N	2-input NOR	1	14	
R2B	Power 2-input NOR	3	36	
R2K	Power 2-input NOR	2	36	
R3N	3-input NOR	2	10	
R3B	Power 3-input NOR	3	36	
R4N	4-input NOR	2	6	
R4B	Power 4-input NOR	4	36	
R6B	Power 6-input NOR	5	36	
R8B	Power 8-input NOR	6	36	
R9B	Power 9-input NOR	8	36	
RCB	Power 12-input NOR	10	36	
RGB	Power 16-input NOR	11	36	
AND Family			•	
Unit Cell Name	Description	Basic Cells	Drive (lu)	
N2P	Power 2-input AND	2	36	
N3P	Power 3-input AND	3	36	
N4P	Power 4-input AND	3	36	
N8P	Power 8-input AND	6	36	
OR Family				
Unit Cell Name	Description	Basic Cells	Drive (lu)	
R2P	Power 2-input OR	2	36	
R3P	Power 3-input OR	3	36	İ
R4P	Power 4-input OR	3	36	
R8P	Power 8-input OR	6	36	
Exclusive NOR/0	OR Family (EXOR/EXNOR)			
Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity
X1N	Exclusive NOR	3	18	Neg
X1B	Power Exclusive NOR	4	36	Neg
X2N	Exclusive OR	3	14	Pos
X2B	Power Exclusive OR	4	36	Neg
X3N	3-input Exclusive NOR	5	14	Neg
ХЗВ	Power 3-input Exclusive NOR	6	36	Neg
X4N	3-input Exclusive OR	5	14	Pos
X4B	Power 3-input Exclusive OR	6	36	Pos

Unit Cell Name	Description	Basic Cells	Drive (lu)
D23	2-wide 2-AND 3-input AOI	2	14
D14	2-wide 3-AND 4-input AOI	2	14
D24	2-wide 2-AND 4-input AOI	2	14
D34	3-wide 2-AND 4-input AOI	2	10
D36	3-wide 2-AND 6-input AOI	3	10
D44	2-wide 2-OR 2-AND 4-input AOI	2	10

Note: AND-OR-Inverter unit cells are useful in implementing sum-of-products (SOP) expressions.

### OR-AND-Inverter Family (OAI)

Unit Cell Name	Description	Basic Cells	Drive (lu)
G23	2-wide 2-OR 3-input OAI	2	18
G14	2-wide 3-OR 4-input OAI	2	10
G24	2-wide 2-OR 4-input OAI	2	10
G34	3-wide 2-OR 4-input OAI	2	10
G44	2-wide 2-AND 2-OR 4-input OAI	2	14

Note: OR-AND-Inverter unit cells are useful in implementing product-of-sums (POS) expressions.

#### **Multiplexer Family**

Unit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Function
T24*	4:1	Power 4, 2 ANDs into 4 NOR Multiplexer	6	36	SOP
T26*	6:1	Power 6, 2 ANDs into 6 NOR Multiplexer	10	36	SOP
T28*	8:1	Power 8, 2 ANDs into 8 NOR Multiplexer	11	36	SOP
T32	2:1	Power 2, 3 ANDs into 2 NOR Multiplexer	5	36	SOP
T33*	3:1	Power 3, 3 ANDs into 3 NOR Multiplexer	7	36	SOP
T34*	4:1	Power 4, 3 ANDs into 4 NOR Multiplexer	9	36	SOP
T42	2:1	Power 2, 4 ANDs into 2 NOR Multiplexer	6	36	SOP
T43	3:1	Power 3, 4 ANDs into 3 NOR Multiplexer	10	36	SOP
T44	4:1	Power 4, 4 ANDs into 4 NOR Multiplexer	11	36	SOP
T54	4:1	Power 2, 2-3-4 ANDs into 4 NOR Multiplexer	10	36	SOP
U24*	4:1	Power 4, 2 OR into 4 NAND Multiplexer	6	36	POS
U26*	6:1	Power 6, 2 OR into 6 NAND Multiplexer	9	36	POS
U28*	8:1	Power 8, 2 OR into 8 NAND Multiplexer	11	36	POS
U32	2:1	Power 2, 3 OR into 2 NAND Multiplexer	5	36	POS
U33*	3:1	Power 3, 3 OR into 3 NAND Multiplexer	. 7	36	POS
U34*	4:1	Power 4, 3 OR into 4 NAND Multiplexer	9	36	POS
U42	2:1	Power 2, 4 OR into 2 NAND Multiplexer	6	36	POS
U43	3:1	Power 3, 4 OR into 3 NAND Multiplexer	9	36	POS
U44	4:1	Power 4, 4 OR into 4 NAND Multiplexer	11	36	POS

Unit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Selects	Outpu	t	Bit Width
P24*	2:1	Data Selector	12	36	s, xs	1 a		4
T2E	2:1	Dual Selector	5	18	s	XQ		2
T2F	2:1	Selector	8	18	s	XQ		4
T2B*	2:1	Selector	2	18	s, xs	XQ		1
T2C*	2:1	Selector	4	18	S, XS	XQ		2
T2D*	2:1	Selector	2	14	S, XS	XQ		11
T5A*	4:1	Selector	5	9	S. XS	XQ		1
V3A*	1:2	Selector	2	14	s, xs	xq		1
V3B*	1:2	Dual Selector	4	14	S, XS	xq		2
Decoders Unit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Active Level Outputs	Enat	ole	
DE2	2:4	Decoder	5	18	Low			
DE3	3:8	Decoder	15	14	Low			
DE4	2:4	Decoder	8	14	Low	Low		
DE6	3:8	Decoder	30	18	Low	1 Higl 2 Low	;	
nternal B	us Unit	Cells			T	<del> </del>		
Unit Celi Name	Туре	Description	Basic Cells	Drive (lu)	Bus Size	Enat	ole	
B11	1-bit B	us Driver	5	36	1	Low		
B21	2-bit B	us Driver	9	36	2	Low		
B41	4-bit B	us Driver	17	36	4	Low		
B81	8-bit B	us Driver	33	36	8	Low		
B12	1-bit B	lock Bus Driver	7	72	1	Low		
B22	2-bit B	lock Bus Driver	13	72	2	Low		
B42	4-bit B	lock Bus Driver	25	72	4	Low		
Data Late	h Fami	ly				_		
Unit Cell Name		Description	Basic Cells	Drive (i	u) Enable	Bits	Output	Clear
YL2	Data	Latch with TM	5	36	High	1	a	T -
YL4	Data	Latch with TM	14	36	High	4	Q	
LTK	Data	Latch	4	18	Low	1	Q, XQ	Async
LTL	Data	Latch with Clear	5	. 18	Low	1	Q, XQ	Async
LTM	Data	Latch with Clear	16	18	Low	4	Q, XQ	<u> </u>
	100	Latch with Clear	4	18	Low	1	Q, XQ	Async
LT1	3-H	Lator With Clear			LOW		0, 10	Asylic

LT4 Data Latch 14 18 Low 4 Q, XQ —

Note: Y-type latches incorporate inhibit inputs and transparent mode (TM) to facilitate scan implementation.

Unit	Flip-flop Family (Positive-Edge Trigg							
Cell Name	Description	Basic Cells	Drive (lu)	Bits	Output	Clear	Preset	Clock Inhibit
SDH	Scan D Flip-flop with 2:1 Multiplexed inputs	14	36	1	Q, XQ	Async	_	Yes
SDJ	Scan D Flip-flop with 4:1 Multiplexed inputs	15	36	1	Q, XQ	Async	-	Yes
SDK	Scan D Flip-flop with 3:1 Multiplexed inputs	16	36	1	Q, XQ	Async		Yes
SJH	Scan J-K Flip-flop	16	36	1	Q, XQ	Async		Yes
SDD	Scan DFlip-flop with 2:1 Multiplexed inputs	16	36	1	Q, XQ	Async	Async	Yes
SDA	Scan 1-input D Flip-flop	12	36	1	Q, XQ	_	_	Yes
SDB	Scan 1-input D Flip-flop	42	36	4	Q, XQ	_		Yes
SHA	Scan 1-input D Flip-flop	68	18	8	Q, XQ	_		Yes
SHB	Scan 1-input D Flip-flop	62	18	8	Q	_	_	Yes
SHC	Scan 1-input D Flip-flop	62	18	8	XQ		_	Yes
SHJ	Scan D Flip-flop with 2:1 Multiplexed inputs	78	18	8	Q, XQ	_		Yes
SHK	Scan D Flip-flop with 3:1 Multiplexed inputs	88	18	8	Q, XQ		_	Yes
SFDM	Scan 1-input D Flip-flop	10	18	1	Q, XQ, SO		_	Yes
SFDO	Scan 1-input D Flip-flop	11	18	1	Q, XQ, SO	Yes		Yes
SFDP	Scan 1-input D Flip-flop	12	18	1	Q, XQ, SO	Yes	Yes	Yes
SFDR	Scan 4-input D Flip-flop	36	18	4	Q, XQ, SO	Yes	-	Yes
SFDS	Scan 4-input D Flip-flop	31	18	4	Q, XQ, SO	-		Yes
SFJD	Scan J-K D Flip-flop	14	18	1	Q, XQ, SO	_	_	Yes
Non S	Scan Flip-flop Family							
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs	Clear	Preset	Clock Edge
FDN	Non-Scan D Flip-flop with Set	7	18	1	Q, XQ		Async	Pos
FDM	Non-Scan D F	6	18	1	Q, XQ	_	_	Pos
FDO	Non-Scan D Flip-flop with Reset	7	18	1	Q, XQ	Async	_	Pos
FDP	Non-Scan D Flip-flop with Set and Reset	8	18	1	Q, XQ	Async	Async	Pos
FDQ	Non-Scan D Flip-flop	21	18	4	a		_	Neg
	Non-Scan D Flip-flop	26	18	4	Q	Async		Pos
FDR		20	18	4	Q	_	_	Pos
	Non-Scan D Flip-flop	- 20						
FDR FDS FD2	Non-Scan D Flip-flop Non-Scan Power D Flip-flop	7	36	1	Q, XQ			Neg
FDS FD2				1	Q, XQ Q, XQ		— Async	Neg Neg
FDS	Non-Scan Power D Flip-flop	7	36			— Async	Async Async	
FDS FD2 FD3	Non-Scan Power D Flip-flop Non-Scan Power D Flip-flop	7 8	36 36	1	Q, XQ			Neg

Note: Synchronous flip-flops may be constructed by adding a simple AND gate (such as N2P) to the input of a flip-flop to create a synchronous clear.

Unit	i								T	1
Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs <sup>1</sup>	Load	Clear	Enable	Carry In	Up/ Down
SC72	Scan Synchronous Binary				Q, XQ,					
	Counter with Parallel Load	62	36	4	CO(S)	Sync		Low	High	Up
SC8 <sup>2</sup>	Scan Synchronous Binary				Q, XQ,					
	Counter with Parallel Load	66	36	4	CO(S)	Sync		High	Low	Down
SC43 <sup>2</sup>	Scan synchronous Binary Counter	59	18	4	Q, CO	Sync	Async	High	High	Uρ
SC472	Scan synchronous Binary Counter	78	18	4	Q, CO	Async	_	Low	Low	UpDown
Non-	Scan Counter Family									
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs <sup>1</sup>	Load	Clear	Enable	Carry In	Up/ Down
C11 <sup>3</sup>	Non-Scan Flip-flop for Counter	11	18	_	Q, XQ		_	_	_	_
C41	Non-Scan Binary									
	Asynchronous Counter	24	18	4	Q, (A)		Async	_	l —	Up
C42	Non-Scan Binary									
	Synchronous Counter	32	18	4	Q	_	Async	_	l —.	Uр
C43	Non-Scan Binary									1
C43	Non-Scan Binary Synchronous Counter	48	18	4	Q, CO(S)	Sync	Async	High	High	Up
C43		48	18	4	Q, CO(S)	Sync	Async	High	High	Up
	Synchronous Counter	48 48	18	4	Q, CO(S) Q, CO	Sync	Async	High High	High High	Up

Notes:

- 1. (S), (A) indicate the counter is (S)ynchronous or (A)synchronous. 
  2. Scan counters include clock inhibit and high drive ( $C_{DR}$  = 36 lu). For non-Scan counters  $C_{DR}$  = 18 lu 3. C11 may by used for purposes other than counters.

Snitt H	egister Family						
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bit Width	Load	Outputs	Clock Polarity
FS1	Serial-in Parallel-out Shift						
	Register	18	16	4	Serial-In only	Q-Parallel	Neg
FS2	Shift Register with						
	Synchronous Load	30	16	4	Sync-High	Q-Parallei	Neg
FS3	Shift Register with						
	Asynchronous Load	34	18	4	Async-Low	Q-Parallel	Pos
SR1	Serial-in Parallel-out Shift						
	Register with Scan	36	36	4	Serial-In only	Q-Parallel	Pos
	l	1	•		- 1	1	1

Datapath	Operators (Adder, ALU, Parity)					
Unit Cell Name	Description	Basic Cells	Drive (iu)	Bit Width	Outputs	Carry In
MC4	Magnitude Comparator	42	18 (=) 10(<,>)	4	A>B, A=B, A <b< td=""><td>A&gt;B,A=B,ALB</td></b<>	A>B,A=B,ALB
A1A	1-bit Half Adder	5	36	1	S, CO	_
A1N	1-bit Full Adder	8	18	1	S, CO	CI
A2N	2-bit Full Adder	16	14	2	S, CO	CI
A4H	4-bit Binary Full Adder w/Fast Carry	18(CO) 14(S)	48	4	s, co	CI
PE5	Even Parity Generator/Checker	12	36	5	EVEN, ODD	_
PO5	Odd Parity Generator/Checker	12	36	5	ODD, EVEN	_
PE8	Even Parity Generator/Checker	18	18	8	EVEN, ODD	_
PO8	Odd Parity Generator/Checker	18	18	8	ODD, EVEN	_
PE9	Even Parity Generator/Checker	22	18	9	EVEN, ODD	
PO9	Odd Parity Generator/Checker	22	18	9	ODD, EVEN	
Miscellar	neous Cells					
Unit Cell		Basic				
Name	Description	Cells			Function	
Z00	0 Clip	0			Tie to Vss	
Z01	1 Clip	0		1	Tie to VDD	

Unit Cell Name	Description	Basic Cells	Drive (iu)	Logic Level	Туре	Input/ Output Polarity
I1B	Input Buffer	5	36	ΠL	Signal	Invert
I1BU	I1B with Pull-up Resistance	5	36	TTL	Signal	Invert
I1BD	I1B with Pull-down Resistance	5	36	TTL	Signal	Invert
I2B	Input Buffer	4	36	TTL	Signal	True
I2BU	I2B with Pull-up Resistance	4	36	TTL	Signal	True
I2BD	I2B with Pull-down Resistance	4	36	TTL	Signal	True
IKB	Clock Input Buffer	4	72	TTL	Clock	Invert
IKBU	Ikb With Pull-up Resistance	4	72	TTL	Clock	Invert
IKBD	IKB with Pull-down Resistance	4	72	TTL	Clock	Invert
ILB	Clock Input Buffer	6	72	TTL	Clock	True
ILBU	ILB with Pull-up Resistance	6	72	TTL	Clock	True
ILBD	ILB with Pull-down Resistance	6	72	TTL	Clock	True
I1C	CMOS Interface Input Buffer	5	36	CMOS	Signal	Invert
I1CU	I1C with Pull-up Resistance	5	36	CMOS	Signal	Invert
I1CD	I1C with Pull-down Resistance	5	36	CMOS	Signal	Invert
I2C	CMOS Interface Input Buffer	4	36	CMOS	Signal	True
I2CU	I2C with Pull-up Resistance	4	36	CMOS	Signal	True
I2CD	I2C with Pull-down Resistance	4	36	CMOS	Signal	True
118	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	Invert
I1SU	I1S with Pull-up Resistance	8	18	CMOS	Schmitt	Invert
I1SD	I1S with Pull-down Resistance	8	18	CMOS	Schmitt	Invert
12S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	True
I2SU	I2S with Pull-up Resistance	8	18	CMOS	Schmitt	True
I2SD	I2S with Pull-down Resistance	8	18	CMOS	Schmitt	True
I1R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	Invert
IIRU	I1R with Pull-up Resistance	8	18	TTL	Schmitt	Invert
I1RD	I1R with Pull-down Resistance	8	18	TTL	Schmitt	Invert
I2R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	True
I2RU	I2R With Pull-up Resistance	8	18	TTL	Schmitt	True
12RD	I2R with Pull-down Resistance	8	18	TTL	Schmitt	True
IKC	Clock Input Buffer	4	200	CMOS	Clock	Invert
IKCU	IKC with Pull-up Resistance	4	200	CMOS	Clock	Invert
IKCD	IKC with Pull-down Resistance	4	200	CMOS	Clock	Invert
ILC	Clock Input Buffer	6	200	CMOS	Clock	True
ILCU	IKC with Pull-up Resistance	6	200	CMOS	Clock	True
ILCD	IKC with Pull-down Resistance	6	200	CMOS	Clock	True

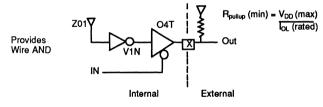
Note: A "U" suffixed to the name of an input buffer indicates pull-up resistance of 50KΩ (typical) and a "D" indicates a pull-down resistance of the equivalent value.

Unit Cell Name	Description	Basic Cells	Drive (I <sub>OL</sub> )	Logic <sup>2</sup> Level	Туре	Edge Rate Control	input/ Output Polarity
O1B	Output Buffer	3	3.2 mA	TTL/CMOS	Standard	No	Invert
O1L	Power Output Buffer	3	12 mA	TTL/CMOS	Standard	No	Invert
O1S	Power Output Buffer	5	12 mA	TTL/CMOS	Standard	Yes	Invert
O2B	Output Buffer	2	3.2 mA	TTL/CMOS	Standard	No	True
O2L	Power Output Buffer	2	12 mA	TTL/CMOS	Standard	No	True
O2S	Power Output Buffer	4	12 mA	TTL/CMOS	Standard	Yes	True
O4 <sup>1</sup>	3-state Output Buffer	4	3.2 mA	TTL/CMOS	3-state	No	True
O4W <sup>1</sup>	Power 3-state Output Buffer	4	12 mA	TTL/CMOS	3-state	No	True
O4S <sup>1</sup>	Power 3-state Output Buffer	5	12 mA	TTL/CMOS	3-state	Yes	True
O1R	Output Buffer	5	3.2 mA	TTL/CMOS	Standard	Yes	Invert
O2R	Output Buffer	4	3.2 mA	TTL/CMOS	Standard	Yes	True
O4R <sup>1</sup>	3-state Output Buffer	5	3.2 mA	TTL/CMOS	3-state	Yes	True
O2BF	Output Buffer	2	8 mA	TTL∕CMOS	Standard	No	True
O2RF	Output Buffer	4	8 mA	TTL/CMOS	Standard	Yes	True
O4RF	3-state Output Buffer	5	8 mA	TTL/CMOS	3-state	Yes	True
O4TF	3-state Output Buffer	4	8 mA	TTL/CMOS	3-state	No	True
O2S2	Output Buffer	3	24 mA	TTL/CMOS	Standard	Yes	True
O4S2	3-state Output Buffer	4	24 mA	TTL/CMOS	3-state	Yes	True

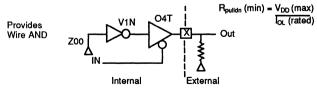
Notes: 1.While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs.

2.Totem pole outputs, such as these buffers have, can drive both TTL and CMOS levels. Voltage margins depend on actual source or sink current (see DC specifications).

#### **Example Of Open Drain Output**



#### **Example Of Open Source Output**



	tional I/O Buffers (Buses)					Ī .
Unit Celi Name	Description	Basic Cells	Drive (l <sub>OL</sub> )	Logic Level	Edge Rate Control	Input/ Output Polarity
Н6Т	3-state Output and Input Buffer	8	3.2 mA	TTL	No	True
H6TU	H6T with Pull-up Resistance	8	3.2 mA	TTL	No	True
H6TD	H6T with Pull-down Resistance	8	3.2 mA	TTL	No	True
H6W	Power 3-state Output and Input			<u> </u>		
	Buffer	8	12 mA	TTL	No	True
H6WU	H6W with Pull-up Resistance	8	12 mA	TTL	No	True
H6WD	H6W with Pull-down Resistance	8	12 mA	TTL	No	True
H6C	3-state Output and CMOS					
	Interface Input Buffer	8	3.2 mA	смоѕ	No	True
H6CU	H6C with Pull-up Resistance	8	3.2 mA	CMOS	No	True
H6CD	H6C with Pull-down Resistance	8	3.2 mA	CMOS	No	True
H6E	Power 3-state Output and CMOS					
	Interface Input Buffer	8	12 mA	CMOS	No	True
H6EU	H6E with Pull-up Resistance	8	12 mA	смоѕ	No	True
H6ED	H6E with Pull-down Resistance	8	12 mA	смоѕ	No	True
H6S	3-state Output and Schmitt					
	Trigger Input Buffer	12	3.2 mA	CMOS	No	True
H6SU	H6S with Pull-up Resistance	12	3.2 mA	CMOS	No	True
H6SD	H6S with Pull-down Resistance	12	3.2 mA	CMOS	No	True
H6R	3-state Output and Schmitt					
	Trigger Input Buffer	12	3.2 mA	TTL	No	True
H6RU	H6R with Pull-up Resistance	12	3.2 mA	TTL	No	True
H6RD	H6R with Pull-down Resistance	12	3.2 mA	ΠL	No	True
Н8Т	3-state Output and Input Buffer	9	3.2 mA	TTL	Yes	True
H8TU	H8T with Pull-up Resistance	9	3.2 mA	TTL	Yes	True
H8TD	H8T with Pull-down Resistance	9	3.2 mA	TTL	Yes	True
H8W	Power 3-state Output and Input					
	Buffer	9	12 mA	TTL	Yes	True
H8WU	H8W with Pull-up Resistance	9	12 mA	ΠL	Yes	True
H8WD_	H8W with Pull-down Resistance	9	12 mA	TTL	Yes	True
H8C	3-state Output Buffer and CMOS					
	Interface Input Buffer	9	3.2 mA	CMOS	Yes	True
H8CU	H8C with Pull-up Resistance	9	3.2 mA	CMOS	Yes	True
H8CD	H8C with Pull-down Resistance	9	3.2 mA	CMOS	Yes	True

Note: A "U" suffixed tol the name of a bidirectional buffer indicates a pull-up resistance of  $50\Omega$  (typical) and a "D" indicates a pull-down resistance of the equivalent value.

Unit Cell Name	Description	Basic Cells	Drive (I <sub>OL</sub> )	input Logic Level	Edge Rate Control	input/ Output Polarity
H8E	Power 3-state Output Buffer and					
	Interface Input Buffer	9	12 mA	CMOS	Yes	True
H8EU	H8E with Pull-up Resistance	9	12 mA	CMOS	Yes	True
H8ED	H8E with Pull-down Resistance	9	12 mA	CMOS	Yes	True
H8S	3-state Output and Schmitt					
	Trigger Input Buffer	13	3.2 mA	CMOS	Yes	True
H8SU	H8S with Pull-up Resistance	13	3.2 mA	CMOS	Yes	True
H8SD	H8S with Pull-down Resistance	13	3.2 mA	CMOS	Yes	True
H8R	3-state Output and Schmitt					
	Trigger Input Buffer	13	3.2 mA	TTL	Yes	True
H8RU	H8R with Pull-up Resistance	13	3.2 mA	TTL	Yes	True
H8RD	H8R with Pull-down Resistance	13	3.2 mA	TTL	Yes	True
H6TF	3-state Output and Schmitt					
	Trigger Input Buffer	8	8 mA	TTL	No	True
H6TFU	H6TF with Pull-up Resistance	8	8 mA	TTL	No	True
H6TFD	H6TF with Pull-down Resistance	8	8 mA	TTL	No	True
H6CF	3-state Output and Input Buffer	8	8 mA	CMOS	No	True
H6CFU	H6CF with Pull-up Resistance	8	8 mA	CMOS	No	True
H6CFD	H6CF with Pull-down Resistance	8	8 mA	CMOS	No	True
H8TF	3-state Output and Input Buffer	9	8 mA	TTL	Yes	True
H8TFU	H8TF with Pull-up Resistance	9	8 mA	TTL	Yes	True
H8TFD	H8TF with Pull-down Resistance	9	8 mA	TTL	Yes	True
H8CF	3-state Output and Input Buffer	9	8 mA	CMOS	Yes	True
H8CFU	H8CF with Pull-up Resistance	9	8 mA	CMOS	Yes	True
H8CFD	H8CF with Pull-down Resistance	9	8 mA	CMOS	Yes	True

### Chapter 2 - Steps Toward Design

#### **Contents of This Chapter**

- 2.1 Introduction
- 2.2 Choosing Fuiltsu as your ASIC Manufacturer
- 2.3 Choosing a Device
- 2.4 Choosing a Package
- 2.5 Technical Review
- 2.6 Design Interface Options

#### 2.1 Introduction

This section of the data book takes a look at the issues that must be considered before a design is ready to be entered on a computer-aided engineering (CAE) workstation.

#### 2.2 Choosing Fuiltsu as Your ASIC Manufacturer

The first step in implementing a given ASIC design is to choose the manufacturer that offers semi-conductor processes capable of actualizing the performance requirements of the IC. The manufacturer should also offer consistent and easily accessible customer support, timely transfer of the design into silicon, and a highly reliable end product.

The data sheet and supplementary information in Chapter 1 enable customers to determine whether their requirements fall within the broad range of Fujitsu's technical capability.

The second step is to discuss the design requirements with one of Fujitsu's Field Applications Engineers at either a Regional Sales Office or a Technical Resource Center. Regional Sales Office and Technical Resource Center addresses and telephone numbers are listed at the back of this volume. Fujitsu's Field Applications Engineers work with each customer to determine which technology would be most suitable for a given design, taking into account the factors outlined in more detail below.

Fujitsu's highly developed software tools, high-capacity manufacturing facilities (the largest in the world) and long history of excellence in the field (Fujitsu has been producing custom gate arrays commercially since 1974) enable customers to turn designs into highly reliable products in a cost-effective time frame.

#### 2.3 Choosing A Device

Speed is usually the deciding factor in choosing the technology for a design, but sometimes special requirements such as package availability, on-chip memory (available in the AU and CG21 technologies), or the necessity for battery power (a feature of the AVL technology) influence the final decision.

Usually the device type is a requirement of the design and is chosen before the package size is determined. The size of the package will depend on array size, partitioning, the number of power and ground pins required by the SSOs (simultaneously switching outputs) used in the design, and the high power drive buffers and clock inputs used in the design.

To determine the most suitable device within a given technology, the designer must determine the gate count and pinout requirements from the schematic diagram of the design to be implemented.

The functions in the schematic or logic block diagram may be described using standard logic functions, programmable logic, or Fulltsu's Unit Cell Library.

Gate counts are calculated in terms of how many basic cells make up each component function (unit cell). This number is given for each unit cell in the unit cell library for each technology. By adding up the number of basic cells used in each logic element in a design, a designer can arrive at a good first estimate of the design complexity.

In the double-column channelless array technologies (AU and CG21), unit cells may take up parts of two adjacent columns. It is recommended that no more than 50 percent of the basic cells in a channelless array be used; 75 percent may be used if memory is included on the chip. Respecting this limitation facilitates fully automated layout.

#### 2.4 Choosing a Package

Before the final choice of an array can be made, however, the choice of a package must be considered. The intended use of the IC generally determines the type of package used: packaging issues are discussed in detail in the application note "Choosing the Best Package for Your ASIC Design" included in Chapter 7 of Section 1 of this data book. The types of packages available for Fujitsu's CMOS channelless arrays are shown in the data sheet in Section 1 and in Appendix D of the AU Unit Cell Library (Section 2) and Appendix D of the CG21 Unit Cell Library (Section 3).

The size of the package chosen is regulated by the number of inputs and outputs required, the number of  $V_{SS}$  and  $V_{DD}$  pins required, and the number of simultaneously switching outputs (SSOs) included in the design.

#### Package Size vs. SSOs

The number of SSOs can influence the size of the package chosen because additional ground pins are sometimes required in a design that has more simultaneously switching outputs than is acceptable for a given package type. Simultaneously switching outputs are those that switch from a logic low or a high impedance (Z) to a logic high or from a logic high or Z state to a logic low within 20 nanoseconds of each other.

A general rule is to use one ground pin for each group of 10 simultaneously switching low power outputs or for 20 non-simultaneous outputs. Chapter 4 of Section 1 of this book and the Package Pin Assignments section of the Design Manuals cover pin requirement issues in more detail.

Although the Vss and VDD pins are preassigned in each package and cannot be changed, alternate packages are available offering varying numbers of power and ground pins.

#### 2.5 Technical Review

When the CMOS technology, the device, and the package have been decided upon, the customer and Fujitsu's Field Applications Engineer hold a technical review to ensure that all the information necessary to implement the design is available and to allow Fujitsu to derive a schedule and price.

#### 2.6 Design Interface Options

The next step is to determine which computer-aided engineering (CAE) workstation will be used to enter the design. The desired result of entering the design on a CAE workstation is the generation of a successful net list or Fujitsu Logic Description Language (FLDL) file and a list of test vectors or Fujitsu Test Description Language (FTDL) file. These two files (which may be generated on any of several different CAE workstation systems) enable Fujitsu's host mainframe to perform automated layout and rigorous test and simulation of the design.

Four popular dedicated CAE workstation systems (Valid, Mentor, Daisy, and the HP 9000) as well as several hardware-independent CAE packages support Fujitsu's design software. In addition, Fujitsu now offers design support on ViewCAD™, a computer-aided engineering system originated by Fujitsu for ASIC designs.

ViewCAD is written in the C programming language and runs on any UNIX™ platform that supports the X Window System™ (such as the Sun 3 or 4 series of workstations). It includes in one package all of the necessary functions for the design, simulation, and analysis of an ASIC design. ViewCAD makes use of a graphics-oriented interface that allows visual examination of all circuits, circuit test data, and simulation results. Its final product is the logic and test data description files (FLDL and FTDL) that are required by the host mainframe computer to process a design.



Through long experience, Fujitsu has found that by far the most efficient way to achieve a trouble-free end product is for customers to implement the design on a workstation themselves. This can be done:

- a. on CAD equipment that the customer is already using (Fujitsu provides cell library information files and the expertise to help write a conversion program to produce the FLDL and FTDL files if necessary)
- on one of the design systems that specifically support Fujitsu software (Daisy, Mentor, Valid, HP 9000) either at the customer's workplace or in one of the Technical Resource Centers
- on ViewCAD either on the customer's own Sun equipment or at a Technical Resource Center.

### Chapter 3 - Design Procedures

#### Contents of This Chapter

- 3.1 Introduction
- 3.2 ViewCAD Design Procedures
- 3.3 Generic Workstation Design Procedures
- 3.4 Post-Design Process
- 3.5 Post-Design Simulation and Test
- 3.6 Engineering Sample Testing
- 3.7 ATG and SCAN Testing

#### 3.1 Introduction

This section of the data book explains the steps necessary to implement an ASIC design in one of Fujitsu's CMOS technologies using a CAE (computer-aided engineering) workstation. Designs can be implemented with Fujitsu's ViewCAD design software or with one of the CAE systems or software applications that support Fujitsu designs.

#### 3.2 ViewCAD Design Procedures

Fujitsu developed the ViewCAD design software to complement a wide range of customer third party design tools. It includes:

- A schematic capture module utilizing the X Window System
- A logic design rule check module that screens for design violations in the areas of fanout and drive, gate count, I/O requirements, etc.
- · A test data or waveform entry module for test vector entry
- An interactive simulation module that replicates the Fujitsu mainframe for both functional and timing simulation
- Conversion modules to define the net list and test vectors in the FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Data Description Language) formats required by Fujitsu's host mainframe.

Figure 3–1 shows the ASIC design flow using ViewCAD. This design flow includes the use of schematic capture and test data generated on other workstations as well as on ViewCAD. The numbers on the left side of Figure 3–1 correspond to the numbers of the paragraphs below that explain the corresponding portion of the figure.

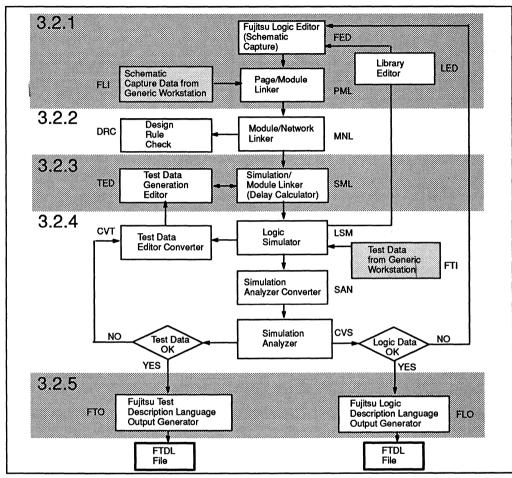


Figure 3-1. ASIC Design Flow with ViewCAD

#### 3.2.1 Schematic Capture

ViewCAD users accomplish logic circuit entry (schematic capture) through the Fujitsu Schematic Editor (FED) module. After running a setup utility requiring the entry of the design name, technology series, and package type, users can insert unit cells and connect them to create circuit diagrams and see a graphic representation of the resulting schematic. The Schematic Editor also provides a basic verification routine. If the schematic has already been entered in another CAE system, it can be converted to ViewCAD-compatible data by the FLDL-to-ViewCAD translator (FLI) module. A Library Editor (LED) module is available to specify design hierarchies, create user macros, and implement blocks in partitioned arrays. ViewCAD allows the user to go back and forth between LED and FED to facilitate the development of complex hierarchical designs.

The designer then uses a Page/Module Linker (PML) module to link pages, ensuring connectivity between the pages of the schematic.

#### 3.2.2 Logic Design Rule Check

DRC, ViewCAD's Design Rule Check module, examines the data files produced by the editor and page linker modules for conformity to the design rules of the CMOS technology in which the design is executed.

Subsequently a Module/Network Linker (MNL) is run on the PML file to expand macros and link the levels of the design hierarchy to prepare the data for the logic simulator.

#### 3.2.3 Circuit Test Data Entry

The designer then provides the Test Data Editor (TED) with test signals for the simulator. Like the schematic capture module, the test data generator displays the data graphically. It allows the user to create and modify signal data and to prepare the data for the simulator module by saving it in a format that the simulator understands. If test data has already been prepared on another CAE system, it can be converted to data usable to the Test Data Editor

The Simulation Module Linker (SML), which takes the output of the Module/Network Linker and generates the delay estimates for the logic simulator, is run before the logic simulator can be executed.

#### 3.2.4 Simulation and Analysis

The Logic Simulator Module (LSM) reads the data created by SML and combines it with the test information in the TED file to run a simulation of the design.

The Test Data Editor Converter (CVT) then converts the output of the simulation module (LSM) back into a TED file. It provides the path from the simulator back to TED so that output that was previously given an undefined value of "X" can be assigned actual simulated values.

The Simulation Analyzer Converter (CVS) translates the output of the logic simulator (LSM) into an acceptable format for the simulation analyzer.

The Simulation Analyzer Module (SAN) analyzes the output from the simulator to determine whether it performs as intended. SAN allows the user to display the simulation output and manipulate the display to help the user analyze the output.

#### 3.2.5 Data Conversion for Mainframe Interface

The last step in the implementation of an ASIC design on ViewCAD is the generation of the all-important FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Description Language) files.

After any design errors that may have been found by simulation and analysis have been corrected in the schematic capture module, the designer runs the Fujitsu Logic Language Output Generator (FLO) module to convert the schematic data into an FLDL file for use on Fujitsu's host mainframe.

If any errors in test data are discovered during the simulation analysis process, the test data can be sent back to the Test Data Editor Converter Module to be reconverted into a form that the test Data Editor understands (since the errors must be corrected in the Test Data Editor module). After error correction or if no errors are found, the designer sends the test data file to the Fujitsu Test Description Language Output Generator (FTO) module for conversion into an FTDL file for use on the mainframe.

#### 3.3 Generic Workstation Design Procedures

Fujitsu provides ASIC Design Software Kits for designers using some of the popular design tools on generic workstations. The kits offer support for Daisy, Mentor, Valid, and HP9000 and include:

- · Fujitsu symbol model libraries for the CAE system's schematic capture module
- · A Fujitsu logic design rule check module
- · Fujitsu timing model libraries for the system's simulator
- · A delay calculator module
- Conversion modules to define the net list and test vectors in the FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Description Language) formats required by host mainframe computer.

In addition, Fujitsu now offers FAME (Fujitsu's ASIC Management Environment), a menu-driven design management program that enables the user to select the technology, the approximate gate count and I/O, pinout, and the package requirements, and to create a design database that is referenced by the other modules to assure correct-by-construction design. FAME includes a test vector module that creates test vectors automatically for complex functions, assists in defining test groupings, cycle times, and strobe settings, and checks created test files against restrictions.

Fujitsu designs are also supported by several high-performance third party CAE tools. These include:

- Verilog-XL™ (Gateway Design Automation) mixed-mode system simulator
- LASAR™ Version 6 (Teradyne) design simulator and test program generator with fault simulation
- HILO® (GenRad) design verification, fault simulation, and test generation tools
- IKOS™ 800 logic validation hardware accelerator
- Synopsys<sup>™</sup> Design Compiler<sup>™</sup> interactive behavioral/logic synthesizer

Figure 3–2 shows a flowchart of the generic workstation-based design process. Because the function and file names used by each different CAE system may differ, generalized names for each operation are used rather than system-specific names in the following list of steps.

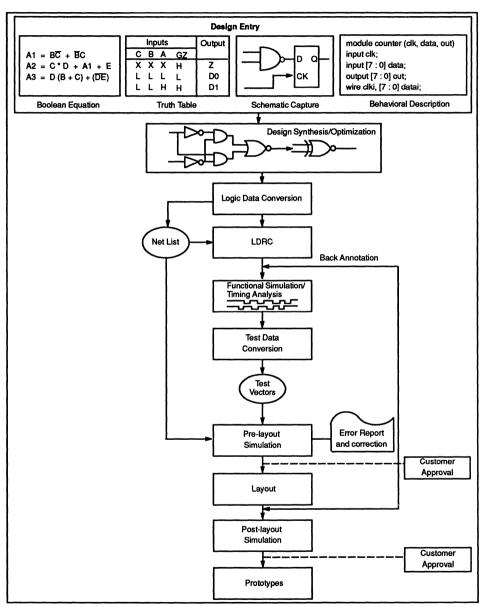


Figure 3-2. Generic Workstation Design Flow

#### 3.3.1 Design Entry

Design entry (schematic capture) is the first step in the generic design automation process. The designer can use the drawing editor program of the applicable workstation software and Fujitsu-supplied symbol

7

model libraries for schematic capture. In most of the Fujitsu-compatible CAE applications, as in ViewCAD, circuits can be defined as macros, for use as sub-parts of other circuits. Design entry can also be accomplished using Boolean equations, truth tables, or behavioral descriptions.

### 3.3.2 Logic Design Rule Check

The Logic Design Rule Check (LDRC) module is Fujitsu software, written specifically for each technology to check gate array designs. This program is run before simulation because it catches errors that, undetected under normal workstation design rules, often cannot be tolerated in a Fujitsu gate array. Even a seemingly small design flaw undetected prior to simulation may be severe enough to invalidate the functional simulation of the design and any test signal data that may be generated from as a result. LDRC checks that the design conforms to the logic design rules applicable to all Fujitsu designs, to those unique to a technology and to those required by the chosen package type. When hierarchy is used, LDRC checks for hierarchy violations.

In order to tailor the LDRC to a particular technology, device, and package, the customer enters required information via an LDRC Control File, which supplies the device and package name and sets the LDRC to output information in the form of a report either on all nets or on only nets that contain errors.

#### **LDRC Report**

When the LDRC is finished running, it produces a report containing the following information:

- a. errors, alarms, and warnings of detected violations
- b. chip information such as:

number of basic cells used vs. cells available

number of unit cells and of different unit cell types

total number of unit cell terminals vs. number of connected unit cell terminals

total number of nets

total number of external input, output, and bus terminals

package name

signal pins used and maximum number of signal pins available

loading unit check list (a list of the load units associated with each input and output signal)

Errors detected during LDRC can now be corrected before the Logic Simulation Program is run.

#### 3.3.3 Functional Simulation

The steps that make up the functional simulation process vary between workstations. For some workstations, functional simulation is all one step, while for others it is three separate steps:

- a. logic simulator data base file compilation
- b. delay calculation
- c. logic simulation

#### Logic Simulator Data Base File

The logic simulator data base file uses a Fujitsu-supplied library to apply behavioral characteristics such as component functions, delay parameters, loading factors, and minimum pulse width, set-up time, and hold time for flip-flops. These values are supplied by the Fujitsu libraries for the appropriate technology. Input stimulus to the circuit is supplied by the designer in the form of the Control File.

#### **Delay Calculator**

Fujitsu provides the program for performing the delay timing calculations. The execution of the program calculates the delay times unique to each net in accordance with the loading condition (fan-out and

hierarchy) in the schematic data file. These calculated delays are representative of pre-layout loading conditions.

The calculations for metal loading are based on the same look-up tables and load equations used in the Design Manual. These loads are subject to change after layout, reflecting the actual metal loads experienced.

#### **Logic Simulator**

The event-driven logic simulator evaluates the outputs of each gate as a function of its inputs and displays the results as either a waveform drawing or as a data file. Workstation simulations performed under the influence of the Delay Calculator are vitally important to verification of design functionality and to the creation of successful test vectors. Using in-circuit application stimulus from the Logic Simulator Data Base File, simulations are executed in minimum, nominal, and maximum modes, with timing checks enabled, to ensure that the design is responding as expected and is stable under all conditions. The results are written to a print-on-change file, which is a list of the signals that changed state, their new state, and the time at which they changed.

### 3.3.4 Logic Conversion (FLDL Generator)

Any errors found by the logic simulation process can be corrected at this point before Fujitsu's Logic Design Language generator (FLDLGEN) program is run on the schematic data file to create the FLDL file. The purpose of the FLDL file is to provide information to the host mainframe for automatic layout and logic simulation. An FLDL control file must be created by the customer containing the customer's name, the workstation type, the revision, the date, and the designer. The FLDLGEN program receives input from the FLDL control file and the schematic data base file created at schematic capture and amended if necessary according to the results of the LDRC and Logic Simulation. The FLDLGEN program can then create a Logic Description (FLDL) file that describes the customer's design for the mainframe software.

#### 3.3.5 Test Data Conversion (FTDL Generator)

The FTDL Generator (FTDLGEN) is a conversion program that translates the Logic Simulator's output file into Fujitsu's Test Description Language. In the process of doing this, it applies Fujitsu tester restrictions to the simulator results. If any signal or timing violations are detected, the operator is informed so that the necessary changes can be made to the data file. The final output file of the FTDL Generator becomes the FTDL File, that is, the test vectors for the mainframe simulator as well as for the LSI tester.

#### 3.4 Post-Design Process

At this point, the customer has gone as far as possible in designing a CMOS gate array on a CAE workstation. Now the design is transferred to the mainframe environment at one of the Technical Resource Centers for mainframe simulation on a Fujitsu M780 35 mips computer. Figure 3–3 describes the post-design process in flowchart form.

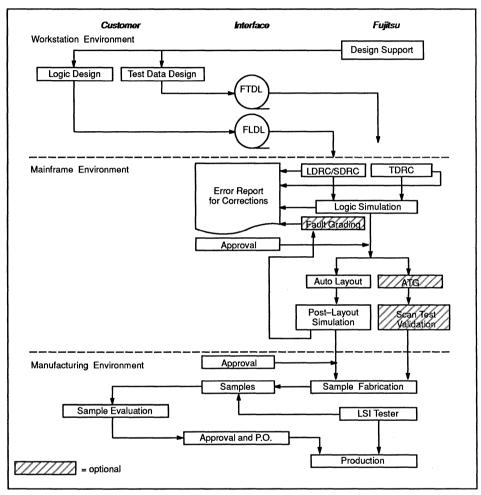


Figure 3-3. Post-workstation Design Process

# 3.5 Post Design Simulation and Testing

# 3.5.1 LDRC and TDRC

The FLDL and FTDL files are provided to a Technical Resource Center usually in the form of magnetic tape or floppy disk. On the mainframe, the FLDL is checked by the mainframe's Logic Design Rule Check (LDRC) to confirm the validity of the logic data and for formatting errors, unconnected inputs and outputs, loading conditions, etc. The FTDL file is checked by a similar mainframe program called the Test Data Rule Check (TDRC), which flags any violations of the published test data restrictions.

# 3.5.2 Pre-layout Simulation

After the LDRC and TDRC have been run successfully on the FLDL and FTDL, the mainframe pre-layout simulation can be performed. This is a logic simulation run at nominal, minimum, and maximum propagation delay times using estimated metalization capacitance values. If there is no discrepancy between simulation results and the expected outputs, the design is presumed to be correct. One of two simulators, LBS6 or ViewCAD, runs functional simulations and timing verification including the checking of set-up and hold time, pulse width, and removal times.

#### 3.5.3 Automatic Layout

After a successful pre-layout simulation has taken place and customer approval has been obtained, a proprietary Fujitsu mainframe application performs automatic placement and metal interconnection routing.

#### 3.5.4 Fault Grading

After post-layout simulation is completed, customers have the option of requesting that Fujitsu subject the test data to a process called fault grading. This CPU-intensive process analyzes the customer's circuit and test data to calculate the percentage of fault coverage. The input test data is analyzed to determine the adequacy of the stimulus patterns to detect any "stuck" (malfunctioning) nodes. The result, a report of all nodes not tested by the stimulus provided, is given to the customer. The customer then has the option of either changing the test vectors or acknowledging that the untested nodes are acceptable.

#### 3.5.5 Post-Layout Simulation

Post-layout simulation, also known as final validation, is again performed at nominal, minimum, and maximum propagation delay times, but using actual calculated capacitance based on the metal interconnection routing resulting from automatic layout.

#### 3.5.6 Sample Fabrication

After a successful post-layout simulation has been performed and customer approval has again been obtained, engineering samples of the array are fabricated for customer evaluation.

# 3.6 Engineering Sample Testing

#### 3.6.1 LSI Tester

Once sample chips have been fabricated, they are tested on the LSI Tester, a test instrument located at the manufacturing facility. Sample chips are tested with input test patterns and expected outputs obtained from the FTDL file.

One of the most important tasks of post-layout simulation is to validate the test vectors for later use on the LSI Tester. For this reason, simulation is executed under conditions adhering as closely as possible to the conditions imposed by the tester. A device that passes all phases of simulation is likely to pass the LSI tester.

The limitations of the LSI Tester places various restrictions upon test data. These restrictions must be respected when preparing the test data pattern and when creating the (stimulus) Control file for running workstation simulations. A "Summary of Test Data Restrictions" for AU Gate Array technology is included in the AU Design Manual.

Test data restrictions involve such issues at the numbers of test patterns acceptable for each test type, the minimum test cycle length, input signal timing, output strobe timing, bidirectional buffer simulation, input and output cycle timing, tester skew, and the treatment of data signals.

Tests performed on the LSI Tester include the function test, the delay test, the DC test, and the high impedance ("Z function") test. Specific data found in the AU Design Manual must be included in FTDL to perform each of these tests.

#### 3.6.2 Function Test

The function test guarantees the designed function of the gate array by exercising as many of the internal nodes as possible and detecting functional failures. Fujitsu requires the function test because it is the primary means of determining if an ASIC is functioning properly as it comes from manufacturing.

In the course of the function test, input signals are applied in accordance with customer timing specifications, using worst-case input voltage at a clock frequency not to exceed 16 MHz (a period of 63 ns). The dynamic performance of this test also partially verifies the AC characteristics of the device.

The function test may be run in multiple units (blocks), allowing changes to be made in the test vectors to assure thorough testing of the device. The transition from one block to the next requires that the device be powered off, adjustments made to the tester and pins regrouped as required. After all changes have been made, the test is restarted. For this reason, each test block must re-initialize the circuit.

# 3.6.3 Z-Function Test

The Z-Function test is administered in the last block(s) of the function test. Its purpose is limited to the verification of the high-impedance function of 3-state and bidirectional output buffers. The Z-function test is necessary only when there are two or more logic combinations that can generate the high-impedance state for a given I/O cell. The test can verify all these logic combinations. If only one logic combination generates the high-impedance condition, then the DC test is adequate.

### 3.6.4 DC Test

The DC test, as its name implies, verifies the DC characteristics of the array. It is not intended to check circuit functionality, but it can be used as a function test of 3-state circuits having only one signal path that generates the high-impedance condition.

The designer supplies the sequence of input signals and expected outputs in the FTDL. These test patterns must generate every possible state for every type of output and input buffer being used (high, low, and high-impedance).

The DC test applies the specified inputs to measure the following DC parameters:

- Steady state power supply current (I<sub>DDS</sub>)
- b. Output high voltage (VOH)
- c. Output low voltage (VOI)
- d. Input leakage current (III)
- e. High-impedance output leakage current (ILZ)

### 3.6.5 Delay Test

The delay test is optional. It is used to verify critical paths or as a means to characterize the device by performing this test on a small number of paths. The purpose of the test is to check that signal paths from various inputs of the chip to their respective outputs meet the customer's standards for minimum and/or maximum delay times. The paths may be sequential and/or combinatorial but only the propagation delay, not the toggle frequency, is measured.

# 3.7 ATG Testing and Scan Design

ATG testing is a special technique that supplements the customer's submitted test patterns (FTDL) to assure both Fujitsu and the customer of a highly reliable gate array by achieving a high degree of fault coverage. ATG testing is implemented by using scan design techniques described at the end of the Design Considerations Chapter. Scan test patterns (both applied input stimulus and expected outputs) are automatically generated by Fujitsu's Automatic Test Generator (ATG) software. ATG is offered by Fujitsu for partitioned arrays of the UHB technology and for all arrays in the channelless gate array technologies.

7

# Chapter 4 - Design Considerations

#### **Contents of This Chapter**

- 4.1 Introduction
- 4.2 Basic Cell Usage
- 4.3 Physical Design Consideration
- 4.4 Designing for Reliability and Testability
- 4.5 Clock Networks
- 4.6 Internal Bus Circuits
- 4.7 Transmission Gate Circuits
- 4.8 I/O Pin Assignments
- 4.9 Scan Test Technology
- 4.10 Compiled Cell Testing

# 4.1 Introduction

Chapter 4 gives an overview of the design hierarchy scheme and the logic and I/O design considerations with which designers need to be familiar in order to optimize a design in Fujitsu's chanelless CMOS Gate Array technologies. This chapter also covers design techniques necessary to implement automated scan path testing of logic circuits and automated testing of compiled cells.

#### 4.2 Basic Cell Usage

In order to benefit from fully automated layout, a designer may use no more than 50 percent of the actual cell count of an AU gate array, 45 percent for CG21 arrays, or 75 percent if the array includes memory or other compiled cells. The actual cell count is the number of basic cells used in the device. AU and CG21 gate arrays utilize internal basic cells as components for I/O buffers; this means that the number of inputs and outputs and therefore input and output buffers required can limit the number of basic cells available for logic design. The utilization guidelines are based on the following formula:

Basic cells available for unit cells and I/O cells = (total on-chip basic cells – compiled cell basic cells) x 50 percent for AU designs or x 45 percent for CG21 designs.

#### 4.3 Physical Design Considerations

In general, signal delays are caused by the signal having to travel through more gates or over longer distances, especially to enter a different block in gate arrays having block architecture (partitioned arrays) or through thicker interconnect wiring. Delay is proportional to length (and thickness) of interconnection metal along which the signal must travel. The following recommendations are therefore made to optimize overall design speed by minimizing the interconnect metal length and the use of thicker interconnection wiring.

# 4.3.1 Hierarchical Design

Devices that are partitioned allow the designer to control relative path lengths. AU and CG21 technologies, therefore, require a hierarchical design approach that divides the cells into blocks and the blocks into sub-blocks so that functional groups of unit cells are laid out in close proximity and signals have less far to travel. When it becomes necessary to link blocks, the use of high-power "high-drive" unit cells is recommended to drive signals in the inter-block metal.

The basic cells in the gate arrays are partitioned into as many as eight blocks. Additional blocks are required to accommodate RAM and ROM modules, when used. Blocks of basic cells used exclusively for digital logic gates can have as few as 4,500 basic cells or as many as 10,000.

The physical layout of all AU and CG21 gate arrays is similar. Required block partitioning is a function of software and is not a physical characteristic.

A hierarchical design method not only offers optimal control of path lengths, but also provides a convenient method of design. Hierarchical design allows the designer to divide the circuit into major macro functions and to follow a step-by-step approach in describing their interconnection.

The hierarchical structure is different for unit cells and compiled cells. Figure 4–1 illustrates the hierarchical structure of an AU or CG21 design.

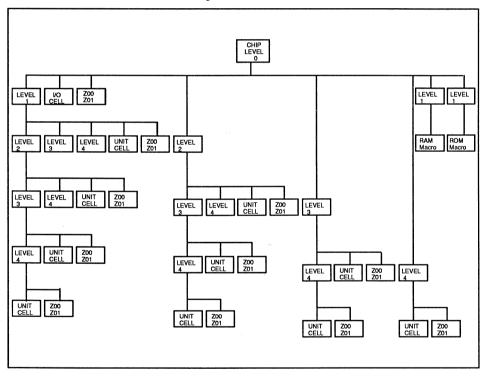


Figure 4-1. Hierarchical Organization of AU/CG21 Designs

#### 4.3.2 The Digital Logic Hierarchical Structure

The CHIP level is the highest level in the hierarchy and represents the entire chip. All I/O cells are defined immediately below the CHIP level, along with any clip cells they may require.

Level 1 blocks must be defined immediately beneath the CHIP level and cannot exceed eight in number (when used for digital logic). Neither unit cells nor compiled cells can be described immediately beneath the CHIP level.

Level 2 is defined beneath the Level 1 blocks, Level 3 beneath Level 2, etc. Levels must always be defined in numerical order. There is no limit to the number of Level 2, Level 3, or Level 4 blocks that may

be used (when defined below a higher block level). Unit cells may be defined beneath Levels 2, 3, or 4, but the lower in the hierarchy the unit cells are defined, the greater the designer's control of delay will be.

Any level may be the first defined under the CHIP level and any of the levels may be omitted; however, the more the designer deviates from the standard structure, the greater the differences between estimated pre-layout delay and actual post-layout delay will be.

The recommended number of basic cells for each hierarchical level is shown in Table 4–1. It is highly recommended that the designer adhere to the guidelines in this table since the tables of estimated metallization load for the cells are based on these block sizes. The basic cell level counts overlap from level to level. The designer may select either of the levels covered by the cell count, but must also use the appropriate table of estimated metallization load for delay calculations.

BLOCK under CHIP Basic Cell Count: Basic Cell Count: AU10K to AU20K AU30K to AU100K CG21103 to CG21203 CG21303 to CG21104 Level 1 4500 to 10,000\* 800 to 2500 Level 2 1800 to 5500 300 to 1200 Level 3 400 to 2200 80 to 500 Level 4 maximum 600 maximum 120

Table 4-1. Basic Cells per Hierarchy Level

# 4.3.3 The Compiled Cell Hierarchical Structure

Each compiled cell (RAM or ROM) must be defined under the level block which resides directly beneath the CHIP level (whether it is a Level 1, 2, 3, or 4). It must be the only cell beneath the level appropriate for the number of basic cells (as defined in Table 4–2) required for that particular compiled cell. The test circuit for a RAM or ROM block cannot be defined in the same block as the RAM or ROM itself. The test circuit should be defined in a block physically close to the RAM or ROM block.

In the CG21 technology, the reccomended number of cell I/Os per block is restricted as shown in Table 4–2. The numbers shown in parentheses in the table is the maximum number of unit cell outputs that can be connected to I/O unit cells (I/O buffers).

Block under CHIP	CG21103 to CG21303	CG21303 to CG21104	
Level 1	130 (70)	500 (140)	
Level 2	80 (50)	300 (90)	
Level 3	50 (90)	100 (60)	
Level 4	30 (20)	50 (30)	

Table 4-2. Recommended Maximum I/O Count per Block

<sup>\*</sup>Any block exceeding the recommended maximum of 10,000 basic cells must be designated Level 1.

# 4.4 Designing for Reliability and Testability

The following general considerations must be made to ensure maximum testability and therefore reliability of a design:

- a. External signal paths must be interfaced to the array by an I/O buffer.
- b. The outputs of a unit cell other than 3-state bus macros and transmission gates may not be wire-ANDed. Generally, if output functions must be tied together, they must be combined through a logic function.
- c. Only one I/O buffer cell can be connected to an external terminal.
- d. Inputs to the same cell may not be tied together.
- e. Unused inputs must be tied high or low, never left floating.
- f. At least one output of a unit cell must be connected.
- g. Functions such as one-shots and other monostable or astable circuits cannot be incorporated into a Fujitsu CMOS gate array. All logic state changes detected at the output of the array must be predictable for the purpose of test, and as such, be the direct result of changes of input stimulus. Series inverters must not be used for the purpose of creating a delay.
- Circuits incorporating sequential devices for instance, flip-flops, counters, shift registers, and so on must have a traceable method of initialization designed into the circuit, independent of feedback loops.
- i. No logic function should be incorporated within the array if it cannot be directly or indirectly set or initialized from a primary input. Designers have two choices for initialization:
  - 1. Supply an external signal for CLEAR, LOAD, etc.
  - Supply known inputs and allow time for them to propagate through the circuit. If the
    propagation method is used, UNKNOWN ("X" state) must be an acceptable output
    state until the initialization is completed.

The information contained in the following sections relates to more detailed aspects of gate array design.

#### 4.5 Clock Networks

A clock network is a circuit used for the efficient distribution of an external clock signal to the clock input of internal sequential and combinatorial unit cells. Skew is the differential delay of a signal as it proceeds through a system. In the context of gate arrays, skew is the effect of a common clock pulse being applied to sequential and combinatorial unit cells at different points in time, because the unit cells are located at different relative positions from the clock pulse origin.

Within a gate array, clock networks may utilize high-frequency and power (HFP), low frequency (LF), or low power (LP) input circuits. Clock networks should be optimized for both internal and inter-chip clock signal distribution applications to minimize skew and to assure high-speed, synchronized operation.

Optimization of clock networks is made possible by the use of the following:

- High-drive input buffers (also called clock input buffers) for HFP and LF input circuits
- Low-drive input buffers (also called data input buffers) for LP input circuits
- Dedicated unit cells (also called clock distribution buffers) driven by HFP, LF, and LP clock input circuits

Up to eight clock input buffers can be used per hierarchical block under the CHIP level and up to 16 clock buffers can be used per design.

#### 4.5.1 High-drive Input Buffers (Clock Input Buffers)

There are two types of high-drive input buffers used for HFP and LF input networks: IKB (an inverting clock input buffer) and ILB (a non-inverting clock input buffer). The IKB and ILB unit cells each have two variations: one incorporates a pull-up resistor on the unit cell input (IKBU and ILBU) and the other features a pull-down resistor (IKBD and ILBD). All have a CDR of 200 lu.

#### 4.5.2 Low-drive Input Buffers

Low-drive input buffers for LP input networks are also available with pull-up and pull-down resistors. Input buffers IB, I1C, I2B, and I2C have a  $C_{DR}$  of 36; input buffers I1S, I2S, I1R, I2R feature a Schmitt trigger input and a  $C_{DR}$  of 18.

## 4.5.3 Clock Distribution Buffers

Clock distribution buffers are used to minimize skew by isolating groups of loads from each other and to provide a facility for balancing one group of loads against another. Clock distribution buffers also provide additional drive capability to the clock signal.

Clock distribution buffers must be used immediately following high-drive input buffers in AU and CG21 gate array networks connected to the CK-input of any unit cell.

There are two categories of clock distribution buffer used in AU and CG21 designs: high-drive, with a  $C_{DR}$  of 55 and low-drive, with a  $C_{DR}$  of 36.

# **High-drive Clock Distribution Buffers**

There are five high-drive clock distribution buffers:

KAB - Block Clock Buffer

KBB - Block Clock (OR x 10) Buffer

KDB - Block Clock (OR x 10) Buffer

K2B - Power Clock Buffer

V1L - Inverting Clock Buffer

These high-drive clock distribution buffers are restricted to clock signal distribution applications.

These clock distribution buffers must be driven only by the following:

High-drive input buffers (clock input buffers)

Low-drive input buffers (data input buffers)

Schmitt trigger input buffers (maximum signal frequency 13 MHz)

HFP input networks must have KDB clock distribution buffers connected to the outputs of their high-drive input buffers (IKB and ILB) within certain limitations. The maximum number of KDB clock distribution buffers permitted per gate array is also limited by array size. These limitations are set out in full in the

appropriate Design Manual. Use of other clock distribution buffers is unlimited, regardless of the type of input network.

#### **Low-drive Clock Distribution Buffers**

There are four low-drive clock distribution buffers (C<sub>DR</sub> = 36):

K1B - Non-inverting Clock Buffer K3B - Gated (AND) Clock Buffer K4B - Gated (OR) Clock Buffer

K5B - Gated (NAND) Clock Buffer

Low-drive clock distribution buffers may be driven by the following:

High-drive input buffers(clock input buffers)
Low-drive input buffers (data input buffers)
Schmitt Trigger input buffers (maximum signal frequency of 13 MHz)
Any other unit cell, including high-drive or low-drive distribution buffers

Low-drive clock distribution buffers K1B, K3B, K4B, and K5B may be used in any application, clock or non-clock, that includes regular data signal buffering.

#### 4.6 Internal Bus Circuits

High-performance internal 3-state buses are a feature of AU and CG21 gate arrays using transmission gates for 3-state control. Bus terminator cells are provided to keep the 3-state bus from floating when not being driven. Fujitsu's design software automatically connects the bus terminator cells to the 3-state bus, where they serve to maintain the last logic level applied to the bus prior to the last bus driver's switching to its high-impedance state. This last logic level will be maintained until any bus driver begins to drive the bus line.

The following bus drivers are available:

B11 1-bit Bus Driver
B21 2-bit Bus Driver
B41 4-bit Bus Driver
B81 8-bit Bus Driver
B12 1-bit Block Bus Driver
B22 2-bit Block Bus Driver
B42 4-bit Block Bus Driver

Figure 4-2 shows a typical bus driver cell.

Overall, the total loading factor should be less than the output driving factor for any clock network design. Taking clock skew into consideration, it is recommended to limit the total input loading factor of clock input buffers to 16 lu (N  $_{\text{F/O}} \le 16$ ) and to limit the total input loading factor of clock buffers to 25 lu (N  $_{\text{F/O}} \le 25$ ).

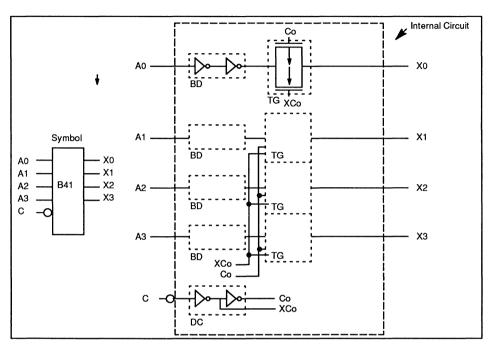


Figure 4-2 Bus Driver Cell, B41

A bus line and associated bus drivers B11, B21, B41, and B81 must reside within the same Level 1 block, immediately below the CHIP level in the design hierarchy. At this time, only a 3-state bus line driven by one of the Block Bus Drivers (B12, B21, and B41) can connect two different blocks. Capacitive loading on bus signal nets is calculated by adding the metal load per the net (N<sub>DI</sub>) and the load factor for all unit cell inputs and bus driver outputs connected to the net where:

```
N_{DI} = (number of unit cell inputs) + (Number of bus drivers – 1)

N_{F/O} = (sum of N_{F/O}s of all unit cells) + (sum of all bus driver Output Load Factors)
```

The total load driven by the output of a bus driver must not exceed 2CDB.

# 4.7 Transmission Gate Circuits

Transmission gates (TGs) allow the selection of two or more input signals, one at a time, to be extended to the TG output. Certain TGs have more than one output, facilitating the switching of one input of each of two or more groups to each of the respective group outputs. There are, for example, four outputs on the T2F TG. One input of four different input groups can be switched simultaneously to their respective group outputs. Selector terminals on the TGs allow direct control of the internal switches by the designer.

# 4.8 I/O Pin Assignments

# 4.8.1 Predetermined I/O Pin Locations

The locations of the following gate array pins are predetermined and cannot be changed:

V<sub>DD</sub> (+5 volts) V<sub>SS</sub> (Ground) Scan inputs and outputs

The maximum output low current ( $I_{OL}$ ) must not exceed 70 mA per  $V_{SS}$  pin output sink current. All  $V_{DD}$  and  $V_{SS}$  pins must be connected to power and ground.

If scan testing is included in the design see section 4.9 of this chapter., six scan test pins are assigned predetermined package pin locations.

When scan testing is to be employed, five of the six scan test pins must be dedicated to scan functions and cannot be used or multiplexed with any other signal in the design. If scan testing is not part of the design, the gate array pins otherwise reserved for the scan test pins can be used as inputs.

#### 4.8.2 General I/O Placement Recommendations

The following general parameters apply to the assignment of I/O pins:

- All V<sub>SS</sub> pins must be tied to ground.
- b. All V<sub>DD</sub> pins must be tied to 5 volts.
- c. Voltage and ground pins are predetermined by the package type and cannot be altered.
- d. Pins designated "No Connection" cannot be used.
- Additional V<sub>SS</sub> and V<sub>DD</sub> pins may not be assigned by the designer without first negotiating the change with Fuiltsu.
- f. Fujitsu recommends that the designer assign the pin numbers to the circuit in the \*ASSIGN or \*OPTION section of FLDL or submit the complete pin assignment table with the design. It is also possible to allow the Technical Resource Center to do the assignment automatically on the mainframe or manually from a customer-supplied form.

#### 4.8.3 Simultaneously Switching Outputs (SSOs)

Outputs are defined as switching simultaneously when they switch either from a logic low or a high-impedance state. to a logic high, or from a logic high or a high-impedance state to a logic low within 20 nanoseconds of each other. When an output switches, the gate array either sources current or sinks current, owing to the charge or discharge of the external capacitive load. This charge/discharge current flows through the self-inductance of the power and ground leads of the gate array, producing induced transient voltages across them.

Simultaneously switching outputs increase the momentary charge/discharge current flow at the gate array and cause noise in the form of momentary spikes or ringing in the power and ground lines. The greater the number of SSOs, the greater the noise produced. These spikes and ringing may appear as signals to the CMOS logic, and therefore must be avoided.

When the ground level is raised by the noise, the input threshold voltage of the gates is also raised, relatively, for the duration of the impulse (as illustrated in Figure 4–3). If  $V_{TH}$  rises, momentarily, above the  $V_{IHmin}$  level, a logic high with a level just above  $V_{IHmin}$  will be recognized as a low level for the duration of the spike. Similar problems are experienced when the ground level is depressed by the noise, affecting logic low levels close to  $V_{ILmax}$ .

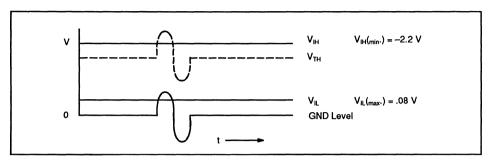


Figure 4-3. SSO-Generated Noise

The severity of the effect of SSOs is determined by:

- The number of SSOs
- . The density and distribution of SSOs in the package
- · The size of the load capacitance, being driven

The number of SSOs allowed in a package is restricted by the number of ground (Vss)pins available, the drive capability of the output buffers, and the location of ground pins on the package (See the Available Package and Pin Assignments section in the appropriate Design Manual). Representative values have been assigned to the effects of output buffers per single ground pin. Output buffers are capable of either 3.2mA or 12mA drive capability, and each may be selected with an optional noise-limiting resistance (NLR) value to minimize generated switching noise. The representative values are given in Table 4.3.

Output Buffer	Represenative Values (per Output)
Normal Drive with NLR (IO <sub>L</sub> = 3.2 mA)	7
High Drive with NLR (IO <sub>L</sub> = 8 mA)	12
High Drive with NLR (IO <sub>L</sub> = 12 mA)	14
High Drive with NLR (IO <sub>L</sub> = 24 mA)	26
Normal Drive with NLR (IO <sub>L</sub> = 3.2 mA)	10
High Drive with NLR (IO <sub>L</sub> = 8 mA)	16
High Drive with NLR (IO <sub>L</sub> = 12 mA)	20

Table 4-3. Representative Value of Output Buffers

The sum of the representaive values for each of the SSOs used in a design must not exceed 80 per Vss pin, regardless of the type of package used.

# 4.8.4 Maximum Load per Ground Pin

The maximum total output load per ground pin is limited as a function of the output switching frequency. The product of the output switching frequency in MHz. and the total output load in pF. per ground pin cannot exceed 12,700 pF x (frequency in MHz), at the maximum junction temperature,  $T_{jmax}$ , of 70°C. As the junction temperature increases, the allowable maximum load per ground pin decreases per the following formula:

 $C \times f \le (12,700 \times Kt.) pF \times (f_{IMHz1}/(number of ground pins))$ 

where C = the output load, in pF

5

f = the output switching frequency, in MHz

Kt = the junction temperature coefficient of load, a constant determined from Table 4–4.

Table 4-4. Junction Temperature Coefficient of Load

Tj( <sub>Max</sub> .) °C	Kt
70	1.0
85	0.7
100	0.5
125	0.3
150	0.2

# 4.8.5 Maximum Load per Output Pin

The maximum total output load per output pin is limited as a function of the output switching frequency. The product of the output switching frequency in MHz. and the total output load in pF. of any pin cannot exceed 1200 pF x  $f_{MHz}$ , at a maximum junction temperature,  $T_{j(max.)}$ , of 70°C. As the junction temperature increases, the allowable maximum load per output pin decreases per the following formula:

 $C \times f \le (1200 \times Kt.)pF \times (f_{IMHz1}/(number of ground pins)$ 

where

C = the output load, in pF

f = the output switching frequency, in MHz

Kt = the junction temperature coefficient of load, a constant determined from Table 4–2.

# 4.8.6 Pin Assignment Guidelines

The locations of all  $V_{SS}$  and  $V_{DD}$  pins are predetermined and fixed. Since the placement of SSOs on any package is critical, SSOs must be assigned within certain pin groups. Within these pin groups, other restrictions apply regarding the separation of SSOs from each other or their proximity to the  $V_{SS}$  pins.

As noted above, the total representative value of any SSO group shown in Table 4–4 must not exceed 80. The SSO pin groups differ between packages. The package outlines and designated grouping of SSO pins for specific devices are shown in the Available Packages and Pin Assignment section of the appropriate Design Manual.

As a general rule, however, the pins available for SSOs between two Vss pins are assigned as follows refer to Figure 4–4.

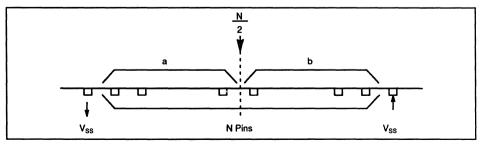


Figure 4-4. SSO Pin Assignments

- · Assume that N pins exist between adjacent VSS pins
- Find the center point on the package between the two V<sub>SS</sub> pins
- There are N/2 pins in the area between the center point and the first V<sub>SS</sub> pin (part A), and N/2 pins in the area between the center point and the second V<sub>SS</sub> pin (part B).
- The SSOs must be equally distributed between parts A and B, within ±1.

# 4.8.7 The Location of HFP Network Input Buffers

The placement of input buffers for HFP input networks is critical because of the special metalization required. Complete sets of tables in the Available Package and Pins Assignments section of the appropriate Design Manual cover the placement of HFP input buffers, reset, preset, and clear pin assignments.

# 4.8.8 SSO Pin Placement Summary

The following is a general summary of recommendations for the placement of pins.

- a. SSOs must be placed in close proximity to V<sub>SS</sub> pins.
- b. High-drive SSOs should be placed closer to V<sub>SS</sub> pins than normal-drive SSOs.
- Asynchronous inputs such as clocks, presets, and clears should be kept away from SSOs. It
  is preferable that these inputs be placed close to V<sub>SS</sub> pins, if available, and away from SSOs.
- d. Clock, preset, and clear inputs must not be placed on the corners of a package, especially when the array is packaged in a DIP.
- Output signals to be used as clock, preset, or clear for other devices must be kept away from SSOs and close to a V<sub>SS</sub> pin.
- f. SSOs should not be placed in the outer row of pins of PGA packages.

# 4.8.9 Test Pins

To facilitate testing, external pins should be provided whenever conditions warrant. The addition of supplementary test pins often allows the reduction of the overall test complexity for a circuit, thus reducing the number of test patterns required and the time necessary to determine functionality of the circuit.

# 4.9 Scan Test Technology

Scan testing is a supplementary, optional test technique that, when used in conjunction with the function and DC test required of the designer, allows greatly increased fault coverage. This increased fault coverage assures both Fujitsu and the designer of a highly reliable gate array.

# 4.9.1 Scan Test Design

The designer implements scan testing by arbitrarily connecting all the sequential logic elements to form an enormous shift register. This shift register can contain up to 3000 stages and is formed by connecting the Q-output of one stage to the dedicated scan input (SI) of the next. If the Q-output cannot be used for this purpose, then the XQ-output may be used, but an inverter must be placed between the XQ-output and the SI input of the following state in order that the data not be inverted.

To implement scan testing, designers use special scan-compatible unit cells for all sequential logic functions. With the use of the serial scan method, the difficult problem of testing a logic circuit containing both combinatorial and sequential logic is simplified to testing combinatorial logic and a shift register, as shown in Figure 4–5 below.

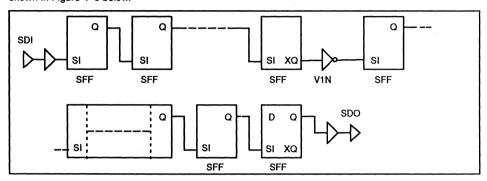


Figure 4-5. Scan Circuit Configuration

Dedicated scan inputs are also used to isolate elements that are not part of the scan test path. Some of these elements can also be tested during the scan test cycle by the use of an alternate scan test mode.

The scan chain design can be considered a data carrier with the ability to carry test input stimulus provided by the LSI tester deep into the design and to apply it to the unit cells under test. Once a unit cell has been tested, its output test result may be stored in the scan data chain and be carried out of the design for comparison to that which was expected. To the designer, can unit cells perform exactly the same as non-scan unit cells, the only difference being the provision of additional basic cells to facilitate the scan test.

Scan testing usually entails an extra 8 to 20% basic cell count, requires the use of seven extra I/O pins, and can cause some degree of propagation delay. Nevertheless, when absolute reliability is the issue, designers find that these considerations are within an acceptable range.

# 4.9.2 Test Pattern Generation

A circuit that is designed for scan testing in this way allows Fujitsu automatic test pattern generation (ATG) software to generate the scan test patterns automatically (both applied input stimulus and expected outputs). The ATG software uses the logic design data from the FLDL file as input from which it generates the test patterns for scan tests. The process requires that all sequential unit cells be of the scan type with the exception of data latches YL2 and YL4. Inclusion of non-scan sequential circuits constructed with combinatorial logic, (i.e., NAND-gate flip-flops, NOR-gate flip-flops, etc.), are discouraged in a scan design because they reduce the overall fault coverage attainable with scan testing. If their use is unavoidable, they must be disabled or isolated by one of the scan test signals discussed below during the ATG process and the scan test.

Scan testing is optional and is applicable only to digital logic unit cells. Compiled cells such as RAM and ROM are tested using a different technique, which is covered in section 4.10 of this chapter and in the Logic Design section of the appropriate Design Manual.

# 4.9.3 Scan Test Signals

Scan test implementation requires the assignment of a dedicated output pin and up to seven input pins, six of which are in predefined package locations. The package locations for these pins in each device type are shown in the Available Package and Pin Assignment section of the appropriate Design Manual.

#### Input Pins

#### Description

- XACK is the scan input, scan output (SISO) A-clock signal. It is generated by the LSI tester and is applied, inverted, to all scan devices at their A-clock input. It writes data from the unit cell's scan input to the master latch.
- 2. BCK is the SISO B-clock signal. It is generated by the LSI tester and is applied, inverted, to all scan devices at their B-clock input. It transfers data between the unit cell's master and slave latches (the output of the device).
- 3. XSM is the SISO mode signal. It is used for set-up of bidirectional buffers, bus drivers, and RAM. If bidirectional buffers or bus drivers are not used, then XSM is not required and need not be included in the design.
- 4. XTST is the scan test signal. It is used to reconfigure the array to make it suitable for scan test and to establish all conditions required for the use of FUjitsu's ATG software. This includes the isolation or removal of certain circuits unsuitable for scan testing, such as non-scan sequential functions and the asynchronous inputs of all sequential elements. (Since they are inaccessible to scan testing, these circuits and disabled functions must, therefore, be tested with user-prepared test patterns.)

XTST disengages all connections between RAM macro data outputs and RAM macro inputs by inserting scan flip-flops in the paths. It causes the internal compiled cell test circuit to select RAM and ROM address and enable lines and RAM wire enable inputs.

If all sequential functions utilize scan type unit cells, if no asynchronous functions are employed (including direct sets and clears), and if circuit isolation is not required, then XTST is not required and is not provided for.

- 5. XTCK is the TC mode clock signal. It is generated by the LSI tester. It is applied, inverted, to the IH-inputs of all sequential unit cells.
- 6. SDI is the serial data input port to the first device of the scan path from outside the chip. It is connected to the SI port of the unit cell. Test data entering the SI input subsequent devices in the scan path is derived either from the Q-Output of the immediately previous state or via an inverter from the XQ-output.

SDI is the only one of the scan test ports that may be used for another function. The designer may also use SDI as a principal input by paralleling the user input with the scan data input.

7. SDO is the serial data output port from the last device of the scan-configured shift register to the environment outside the chip. Test data from SDO is taken from the Q-output of the last stage (or from the XQ-output via an inverter) of the giant scan shift register. SDO is the only one of the scan test ports whose location is not fixed; SDO may be placed by the designer at any convenient location.

#### 4.9.4 Scan Test Modes

Scan testing consists of two modes of operation: SISO (Scan input/scan output) mode and TC (test clock) mode. Sequential logic is primarily addressed by SISO and combinatorial logic is addressed by TC; the two modes are alternated during the scan test.

### The SISO Mode

This mode causes all elements of the scan path to be written to and read from. In this mode of operation, the following occurs:

21

- a. The scan SISO path is activated by making XSM = 0
- b. The scan clocks XACK and BCK are supplied
- c. The data to be written is supplied to SDI serial data input
- d. The data is read out of SDO and compared with the expected values

These writing and reading operations are performed in parallel.

#### The TC Mode

This mode tests the array as a normally configured device, but the data is clocked by special clocks provided to the gate array by the LSI tester. In this mode of operation, the following occurs:

- a. The scan SISO path is disabled by making XSM = 1.
- b. All normal system clocks are disabled, forcing the clock inputs (CK) of all scan unit cells to a logic low.
- c. Input signals are applied to normal input pins principal inputs.
- d. The TC system clock, XTCK, is applied to the unit cells' IH-inputs.
- e. Output signals are read from normal output pins principal output and compared with the expected values.

The alternation of these two modes allows the correct functioning of logic elements not directly accessible from a principal input to be verified. The data scanned in is especially useful in providing control inputs to otherwise difficult-to-control internal logic. Prior to the input of the data to the scan path, some detectable faults can be observed externally by application of inputs to some non-scan external inputs. After data has been clocked into the scan path, other detectable faults can be observed externally. The remaining detectable faults are observable externally after the data has been clocked into the scan path, the TC system clock (XTCK) has been applied, and the resultant data shifted out of the scan path.

# 4.10 Compiled Cell Testing

Compiled cells (RAM and/or ROM) are tested by accessing the cell I/Os from principal inputs and principal outputs. Some designs may have the data inputs and outputs, the address lines, Read Enable, Write Enable, etc., connected directly to principal inputs and principal outputs, making the test of such macros very straightforward. In most designs, however, some or all of the above are embedded deep in the design, the input signals being derived either from other RAMs or ROMs or from the digital logic unit cells. To gain access to these RAM or ROM I/O ports, the designer must build test access circuits with input and output selectors around the macros.

With the test access circuits in place, Fujitsu prepares the test vectors for all RAM compiled cells.

In the case of ROM compiled cells, Fujitsu tests to determine that the permanently stored data pattern specified by the designer is properly stored and accessible. The designer, therefore, prepares all ROM test vectors.

Test signals from the LSI tester access the RAM and/or ROM macros through principal inputs and principal outputs, and are usually multiplexed with the designer's logic. The multiplexing is accomplished by means of the input selectors and output selectors. Input and output selectors allow the LSI tester to access the designer's logic or the compiled RAM or ROM cells individually to perform the appropriate tests.

Compiled cell testing can take place whether or not scan path testing has been implemented in the design and dedicated scan I/O pins assigned.

# **Chapter 5 – Delay Estimation Principles**

#### **Contents of This Chapter**

- 5.1 Introduction
- 5.2 Choosing Critical Paths
- 5.3 Load Units and Loading Guidelines
- 5.4 The Delay Equation
- 5.5 Estimating Gate Delay
- 5.6 Estimating Total Circuit Delay
- 5.7 Delay Calculations when Load Exceeds CDR
- 5.8 Clock Loading
- 5.9 Delay Multipliers
- 5.10 Calculation of Array Power Dissipation for Delay Multipliers
- 5.11 Calculating Delays for Test
- 5.12 Delay Parameters for Compiled Cells

# 5.1 Introduction

This section of the data book gives an overview of the delay estimation principles important to the design of an ASIC using Fujitsu's channelless CMOS gate array technologies. Included are the loading rules for AU and CG21 gate arrays and a demonstration of how to estimate the delay through a circuit. In addition to the basic delay equation, this chapter also considers the loading limitations for clock signals and the effects of the operating environment on typical delay figures.

# 5.2 Choosing Critical Paths

A critical path is a logic path whose timing requirements must be satisfied to ensure proper system function. In an ordinary synchronous circuit, data propagates from one register through combinatorial logic into another register. For the circuit to function properly, the sum of the clock-to-Q delay of the source register, the propagation delay through the logic, and the set-up time on the target register must be less than the worst-case system clock skew. Correct timing of the signal along the critical path guarantees that this condition is met.

Usually, the critical path is the one with the greatest number of gate levels. However, if such a path is speeded up by redesign, another, less complex path may become the new critical path.

For example, in a design in which a path has eight levels of gating, the designer may determine upon inspection that two groups of NAND-NAND structures can be changed to AND-OR inverter cells, an efficient CMOS implementation that noticeably increases the speed of the path. In this case, after applying DeMorgan's theorem and reducing the result, the designer finds that another path is now the critical path.

Since each logic state sensitizes different branches, logic paths must be analyzed using the inputs (rising or falling) that will actually be applied to them (since rising and falling delays are not equal) to determine the longest path that will be sensitized and ensure that it meets critical path requirements.

In this section, a path delay calculation is worked through to show how a designer can analyze each element of a Fujitsu CMOS circuit to make sure the design meets critical path requirements. In this example, the effect of a rising input on the sample circuit is calculated as it would be if this were a critical path and the rising input were forcing the transition of interest.

# 5.3 Load Units and Loading Guidelines

The Fujitsu CMOS load unit (lu) is the input capacitance of an inverter used as the basic unit for measurement and calculation of capacitive loads presented to unit cells within the gate array. Both the output drive factor of a unit cell and its input load factor are defined in terms of load units.

# 5.3.1 Output Drive Factor (CDR)

The output drive factor (C<sub>DR</sub>) is a parameter expressing the load driving capability of a unit cell. The output drive factor is provided in the Unit Cell Library for each unit cell in load units. Unit cells can drive loads greater than the output drive factor; however, the performance of CMOS circuits degrades exponentially with increased loading. If too great a load is driven, an exaggerated increase in delay through the unit cell may be experienced.

It is permissible for the load to exceed  $C_{DR}$  if the associated additional delays are anticipated and tolerable. Additional calculation factors are required to estimate delays of loads greater than  $C_{DR}$ . Figure 5–1 indicates the delays that may be generated when the load exceeds these guidelines.

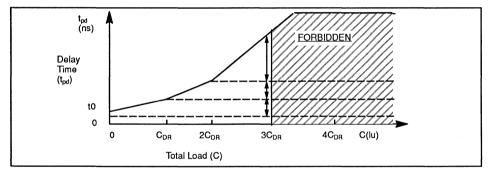


Figure 5-1. Delay Time vs. Loading Factor

# 5.3.2 Input Load Factor

The input load factor is the value in load units of the load placed on a network by the connection of the input of the unit cell in question. The input load factor for each unit cell is provided in the Unit Cell Library.

# 5.3.3 Total Input Load Factor (N<sub>F/O</sub>)

The total input load factor or fanout  $(N_{F/O})$  is the sum of the input load factor of each of the unit cells connected to the output of the unit cell in question.

# 5.3.4 Total Unit Cell Load

The delay factor of each unit cell is made up of two types of capacitive loading:

- a. Load capacitance inherent in the input of each cell it must drive  $(N_{F/O})$
- b. Load capacitance due to the metal interconnection of the unit cells  $(C_L)$

or 
$$C = N_{E/O} + C_{I}$$

#### 5.3.5 Number of Driven Inputs (NDI)

The total metal load ( $C_L$ ) depends on the number of driven inputs ( $N_{DI}$ ), that is, the number of other cells to which the output of the unit cell in question is connected. Given the value of  $N_{DI}$ , a value for  $C_L$  is available from the Estimation Tables for Metal Loading in Appendix C of the applicable Unit Cell Library (reprinted in Sections 2 and 3 of this Data Book). For each value of  $N_{DI}$ ,  $C_L$  varies according to hierarchical level of the cell in question (Level 1, Level 2 etc.) and to its functional logic block status as a main block or a subblock.

#### 5.3.6 Networks

A network or net is considered to be the metal wiring that connects the output of a unit cell to the input(s) of all unit cells that it is driving. Interconnect metal refers to the metal wiring, also called routing metal, that makes up each network. Networks that are not connected to any unit cell clock input are generally classified as data networks and are limited to a maximum load of 3  $C_{DR}$  or 72 lu. It is good design practice to limit loads on data networks to less than 2  $C_{DR}$  during the design phase, otherwise the load may exceed 3  $C_{DR}$  after chip layout.

A network that is connected to the clock input of any unit cell is classified as a clock network and is limited to a maximum load of  $C_{DR}$ . A prudent designer will limit loads on a clock network to much less than  $C_{DR}$ .

#### 5.3.7 Functional Logic Blocks

In the interest of optimizing critical paths and minimizing interconnect wiring length, logic is divided into functional logic blocks to facilitate unit cell output loading calculation. A block is regarded as a main block or a subblock with respect to a given signal net.

A main block has all of the following:

- · the complete network
- · the unit cell or block driving the network
- · all unit cells or blocks driven by the network

A subblock has some, but not all, of the above characteristics and is a component part of the main block.

The assignment of main block and subblock designations to segments of a circuit facilitates the notation of inter- and intra-hierarchical propagation of signals. The delay values given in the Estimation Tables for Metal Loading (appended to the Unit Cell Libraries) are different for main blocks and subblocks, owing to the difference in the estimated average path lengths encountered in each.

#### 5.4 The Delay Equation

The basic delay equation combines the AC parameters of a cell and its associated capacitive loads to estimate the delay time through the cell. The rise and fall time of a unit cell may not be symmetrical due to differences in the transconductivity of the N and P transistors as well as to differences in the arrangement of the transistors to form unit cells. The same equation is used with different variables for positive-going and negative-going signals at the unit cell output. These signal polarity variables must be considered separately.

$$t_{UP} = t_{OUP} + K_{CLUP}(N_{F/O} + C_L)$$
  
$$t_{dn} = t_{Odn} + K_{CLdn}(N_{F/O} + C_L)$$

where:

toxx is the circuit delay through the unit cell under no-load conditions (a value given in ns for each cell in the unit cell library).

KCLxx is the load derating constant or delay time per loading unit conversion factor (ns/pF) (a value defined for each unit cell in the unit cell library).

N<sub>F/O</sub> is the sum total of the input loads of all unit cells driven in the network (expressed in load units).

C<sub>L</sub> is the amount of loading, in load units, on the unit cell output due to interconnect metal (metal load).

# 5.5 Estimating Gate Delay

Figure 5–2 shows a sample circuit for the purposes of demonstrating how the total accumulated delay (tpd) through a short path is estimated.

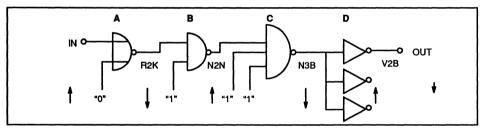


Figure 5-2. Delay Path Sample Circuit

Ordinarily a designer looks up the the specifications of each unit cell in the unit cell library of the applicable technology. For this example, however, all of the necessary specifications have been assembled in Table 5–1, using the values for AU technology.

Table 5-1. AC Parameters of Unit Cells

		Basic	Input	Output	Propag	Propagation Delay Time				
Cell	Cell	Cells	Load	Drive	t <sub>up</sub>		t <sub>dn</sub>			
Function	Name	Used	Factor	Factor	t <sub>o</sub>	K <sub>CL</sub>	t <sub>o</sub>	K <sub>CL</sub>		
2-Input NOR	R2K*	2	2	36	0.36	0.11	0.36	0.05		
2-Input NAND	N2N	1	1	18	0.30	0.13	0.45	0.11		
3-Input NAND	N3B*	3	1	36	1.03	0.07	1.36	0.03		
Inverter	V2B	1	2	36	0.20	0.07	0.20	0.04		
	ľ			ł		1	1	l .		

<sup>\*</sup> These are high drive cells that operate faster than their low drive equivalents under these circumstances.

The delays for rising  $(t_{up})$  and falling  $(t_{dn})$  edges of a pulse can differ widely. Digital pulses are either lengthened or shortened while passing through a unit cell. It is therefore important to calculate the pulse

width variations along the entire signal path to verify that pulse width is sufficient to pass through each gate.

In the example that follows, based on Figure 5–2, calculations are based on a rising pulse entering the input of unit cell A and changing state several times as it proceeds through the sample circuit. To find the total delay for the circuit, it would be necessary to calculate the values resulting from the opposite case, in which a falling pulse enters the circuit at unit cell A.

# 5.5.1 Delay Parameter for Rising Edge $(t_{up})$

The unit cell library shows that the delay time ( $t_0$ ) for an upward transitioning signal at the unit cell output ( $t_{up}$ ) for R2K, a 2-input NOR, is 0.36. It shows that the load/delay conversion factor for an upward transitioning signal ( $K_{Clup}$ ) for R2K is 0.11.

#### 5.5.2 Number of Fan-outs (NE/O)

The sample schematic in Figure 5–2 shows that the  $N_{F/O}$ , the number of cells that the R2K must drive, is one (an N2N). The unit cell library shows that the N2N has an input load factor of 1 lu.

# 5.5.3 Number of Driven Inputs (NDI) and Metal Load (CL)

The value for  $C_L$  is based on the number of inputs the cell in question must drive and is derived from the Estimation Tables for Metal Loading appended in this Data Book to each unit cell library. Table 5–2 is a sample metal load table for a 50KAU device at the sub-block level. Each technology and device has unique load/delay characteristics and the AU and CG21 technologies further divide loading values into main block values and subblock values and then into values for each hierarchical level. Since this sample circuit is very small, it will be assumed to be at a Level 4 in a subblock in the design hierarchy. Because the number of driven inputs (or  $N_{Dl}$ ) for R2K, N2N, and V2B in Table 5–2 is one, the amount of loading due to metallization ( $C_L$ ) is 1.0 lu. The NDI for N3B in Table 5–2 is three; therefore the  $C_L$  is 2.8.

Table 5–2. Estimation Table for Metal Loading C-50KAU (Subblock)

N <sub>DI</sub>		C <sub>L</sub> (I	lu)	
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	4.7	3.3	2.2	1.0
2	8.6	6.1	3.9	1.9
3	12.6	8.9	5.7	2.8
4	15.2	10.8	7.0	3.4
5	17.2	12.2	7.8	3.8
6	18.8	13.3	8.6	4.2
7	20.6	14.8	9.5	4.7
8	21.8	15.5	9.9	4.9
9	22.5	15.9	10.2	5.0
10	23.1	16.4	10.5	5.2
11	23.1	16.4	10.5	5.2
12	23.4	16.6	10.7	5.2
13	23.9	16.9	10.9	5.3
14	24.5	17.4	11.2	5.5
15	24.5	17.4	11.2	5.5
16 – 30	26.8	19.0	12.2	6.0
31 – 50	31.1	22.1	14.1	7.0
51 – 75	32.1	22.7	14.6	7.2
76 – 100	35.5	25,2	16.1	8.0

The value given for  $C_L$  in the Estimation Tables for Metal Loading is an estimate of the loading effect of the metalization capacitance on the output based on Fujitsu's careful statistical analysis of typical designs. Actual metal loading is based on the effect of the routing and therefore may vary from these estimates. To compensate for this uncertainty, Fujitsu incorporates a  $\pm 5\%$  variation into the prelayout delay multipliers. After routing, another set of simulations is run to verify the effect of the actual metal routing.

Additional metal loading tables in the Design Manual provide delay values for signals passing between exterior and interior I/O cells and for such signals routed through the heavier metal interconnect wiring required by high frequency signals.

# 5.6 Estimating Total Circuit Delay

Based on the values from Table 5-1 and Table 5-2, the propagation delay for R2K in the sample circuit is:

```
\begin{array}{llll} tdn \, (A) & = t_{Odn} & + & KCLdn \, (NF/O + CL) \\ tdn & = 0.36 & + & 0.05 \, (1 + 1.0) \\ tdn & = 0.36 & + & 0.05 \, (2.0) \\ tdn & = 0.36 & + & 0.10 \\ tdn & = 0.46 \\ tdn \, (A) & = 0.5 & (rounded up to the next 0.1 ns) \end{array}
```

The propagation delay for N2N, found by following the same procedure, is:

The propagation delay for N3B, found by following the same procedure, is:

```
\begin{array}{llll} tdn \ (C) & = \ todn & + & \ KCLdn \ (NF/O + CL) \\ tdn & = \ 1.36 & + & 0.03 \ (3 + 2.8) \\ tdn & = \ 1.36 & + & 0.03 \ (5.8) \\ tdn & = \ 1.36 & + & 0.174 \\ tdn & = \ 1.534 \\ tdn \ (C) & = \ 1.6 & \ (rounded \ up \ to \ the \ next \ 0.1 \ ns) \end{array}
```

The propagation delay for V2B, found by following the same procedure, is:

Therefore, the total delay for the sample circuit shown in Figure 5-2 is:

```
t_{pd} = t_{dn} (A) + t_{up} (B) + t_{dn} (C) + t_{up} (D)

t_{pd} = 0.5 + 0.6 + 1.6 + 0.4

t_{pd} = 3.1 \text{ ns}
```

# 5.7 Delay Calculations When Load Exceeds CDR

Fujitsu CMOS gate arrays are capable of driving loads beyond their published Output Drive Factor (*CDR*). It must be emphasized, however, that the delays that result from this practice are considerably increased. Unit cells may be loaded beyond their *CDRs* provided that the increased delay is acceptable.

Anticipation of the effects of loading beyond the published *CDR* requires recalculation of delay. The general formulas for loading beyond *CDR* are listed below; different delay equations must be used depending on the degree that the loading exceeds *CDR*.

The Sea-of-Gates technologies, AU2 and CG21, require two additional parameters to "fine-tune" calculations of unit cell delay under conditions of very light loads. These parameters, CDR2 and KCL2 are defined for some selected unit cells

CDR2: Initial output driving factor—if undefined, then CDR2 = 0)

KCL2: Initial delay time per load unit—if undefined, then KCL2 = 0)

When C is CDR or less:

tpd = t0 + KCL2 \* C

When C is between CDR2 and CDR:

tpd = t0 + KCL2 \* CDR2 + KCL \* (C - CDR2)

When C is between CDR and 2CDR:

tpd = t0 + KCL2 \* CDR2 + KCL \* (CDR - CDR2) + 1.5KCL \* (C - CDR)

When C is between 2CDR and 3CDR:

tpd = t0 + KCL2 \* CDR2 + KCL \* (CDR - CDR2) + 1.5KCL \* CDR + 3KCL \* (C - 2CDR)

### 5.8 Clock Loading

It is acceptable, though not a recommended design practice, to load the output of a unit cell that does not carry a clock signal beyond its Output Drive Factor (CDR). To ensure maximum clock accuracy, however, unit cells that output clock signals must never be loaded beyond CDR. Having different loading limitations for clock and non-clock unit cells can lead to "race conditions," in which the clock signal arrives at a flip-flop before the data signal set-up time has elapsed. It is therefore most important, when loading a unit cell beyond CDR, to modify the fundamental delay equation using the extra delay factors explained in the previous section.

# 5.9 Delay Multipliers

The delay times considered so far are typical delays derived from typical unit cell data. Typical data, however, does not take into account the environmental, thermal, and electrical variations of the real world operating environment. It is necessary, therefore, to simulate worst-case conditions during the simulation and test phases of circuit design. Revised estimates of delay under these harsher circumstances may be arrived at by multiplying the typical delay figures by delay multipliers.

#### 5.9.1 Operating Environment

The operating environment of the array can cause variations from the calculated typical delay figures. Influencing factors include ambient temperature, applied voltage, and variations in the manufacturing processes. Figure 5–3 shows how supply voltage and temperature affect the performance of a sample array when temperature or supply voltage varies beyond the published operating condition specifications for the device. The actual multipliers used depend on the device type.

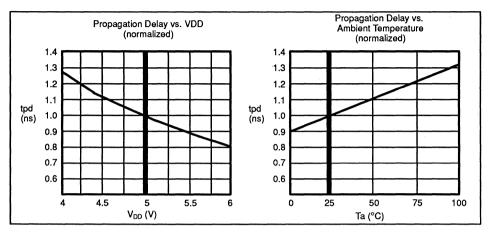


Figure 5-3. Operating Environment Factors Influencing Delay

Maximum and minimum pre-layout simulation delays are derived from delay multipliers applied to the calculated typical delays. Post-layout simulation delay multipliers are based on the capacitance of the actual metalization routing calculated as a function of the layout program.

# 5.9.2 Minimum and Maximum Delay Factors

Minimum/maximum delay factors for AU and CG21 technologies CMOS gate arrays are as follows:

winimum	maximum
5 V <u>+</u> 5%, <u>&gt;6</u> 0°C	5 V ±5%, <u>≤</u> 60°C
0.35	1.65
0.40	1.55
	<b>5 V ±5%, <u>&gt;6</u>0°C</b> 0.35

# 5.9.3 Factors Affecting Maximum Delay Multipliers

The normal operating temperatures of most arrays, however, will be in excess of 60°C and therefore the delay multipliers for maximum pre- and post-simulation delays must be scaled by junction temperature factors.

Junction temperature is a function of the power dissipated by the array, the thermal resistance of the package selected for the die, and the maximum ambient temperature. The power dissipated by the array becomes a serious consideration in AU and CG21 technology because the gate count and the operating speed of these gate arrays are appreciably higher than those of earlier, channeled arrays.

# 5

# 5.9.4 Calculating Junction Temperature (Tj)

The junction temperature of an array is determined by the following formula:

Junction Temperature (Tj) = 
$$T_{aMAX} + \theta ja * Pd$$
 (°C)

The factors affecting junction temperature are as follows:

 $T_{aMAX}$  = the maximum expected ambient temperature (°C)

- =  $\theta ja$  the thermal resistance of the package (°C/W)
- = pd the power dissipated by the array (W)

### **Maximum Ambient Temperature**

The maximum expected ambient temperature (Tamax) must be determined by the designer from the application.

# Package Thermal Resistance (θja)

The maximum junction temperatures for AU gate array packages are as follows:

Ceramic packages:

150°C

Plastic packages

ackages 125°C

The thermal resistance  $(\theta ja)$  of the chosen package type should be able to dissipate enough power so that the junction temperature (t) does not exceed the maximum junction temperature capability of the package.

Table 5-3 lists the thermal resistances of the larger AU and CG21 gate array PGA packages.

#### **Power Dissipation**

The method by which the designer determines the power dissipated by an array is discussed in the following section.

Table 5-3. Package Thermal Resistance in °C/W

Package	Part Number	Array Size	Air Flow (meters/sec.)		
			0	1	3
PGA-135	MB630K MB631K MB632K MB633K MB634K	C-100KAU C-75KAU C-50KAU C-40KAU C-30KAU	30	20	15
PGA-179	MB630K MB631K MB632K MB633K MB634K	C-100KAU C-75KAU C-50KAU C-40KAU C-30KAU	25	19	13
PGA-208	MB630K MB631K MB632K MB633K MB634K	C-100KAU C-75KAU C-50KAU C-40KAU C-30KAU	23	17	12
PGA-256	MB630K MB631K MB632K MB633K	C–100KAU C–75KAU C–50KAU C–40KAU	19	13	9
PGA-299	MB630K MB631K MB632K	C–100KAU C–75KAU C–50KAU	19	13	9
PGA-321	MB630K MB631K	C-100KAU C-75KAU	22 to 24	16 to 18	11 to 13
PGA-361	MB630K MB631K	C-100KAU C-75KAU	22 to24	16 to 18	11 to 13
PGA-401	MB630K	C-100KAU	22 to 24	16 to 18	11 to 13

# 5.10 Calculation of Array Power Dissipation (Pd) for Delay Multipliers

The worst-case power dissipation of the gate array is the sum of the power dissipations of the individual elemental groups of the array, multiplied by a factor (CV) determined by the power supply variation (tolerance). This factor, CV, is 1.10 for a 5 V  $\pm$ 5% tolerance power supply. The individual elemental groups of the design for which typical power dissipation must be calculated (in mW) are shown in Table 5–4.

Table 5-4. Power Dissipation Calculation Factors

Functional Group	Factor Name
I/O buffers	Pio
Internal logic gates	PG
RAM (compiled) cells	PRAM
ROM (compiled) cells	PROM

Typical power dissipation is calculated using the following formula:

$$P_T = P_{IO} + P_{G} + P_{RAM} + P_{ROM} (mW)$$

Worst case power dissipation:

$$Pd = P_T * CV (mW)$$

The formulas used to calculate each of these elements of typical power dissipation (*PT*) are listed in the following sections. A table showing values for a representative range of design elements is given following each formula.

# I/O Buffer Power Dissipation (PIO)

In the calculation of *PIo*, both AC power dissipation (*PAc*) and DC power dissipation (*PDc*) must be considered, as in the following formulation:

$$PIO = PAC + PDC (mW)$$

#### where

PAC is the active (or switching) power dissipation of an I/O buffer and PDC is the power dissipation of an I/O buffer caused by loads sourcing and sinking current external to the array.

#### Estimation of I/O Buffer AC Power Dissipation (PAC)

The AC power dissipation is proportional to the number of I/O buffers switching each cycle at the maximum switching frequency. A decimal factor representing the percentage of buffers switching in each cycle is indicated in the equations below by an asterisk.

In the formulas for the derivation of *PAc* shown below, 0.20 is used for the percentage of buffers switching in each cycle, reflecting Fujitsu's observation that in the average design, 20 percent of all buffers switch in each cycle. If every buffer switched at the system frequency, this factor would be 1.00.

The AC power dissipation of input buffers = 0.110 mW/MHz

PACIN (mW) = 
$$0.11 * (total input buffer count) * f * 0.20$$

where

f = the maximum system frequency 0.20 = fraction of buffers switching in each cycle

Table 5-5 shows a representative range of values for PACIN.

Table 5-5. Input Buffer AC Power Dissipation (PACIN) Examples (in mW)

Average Number		Average Input Frequency					
of Simultaneously Switching Inputs	1 MHz	5 MHz	10 MHz	20 MHz	30 MHz	40 MHz	
12	1	7	13	26	40	53	
25	3	14	28	55	83	110	
50	6	28	55	110	165	220	
75	8	41	83	165	248	330	
100	11	55	110	220	330	440	
125	14	69	138	275	413	550	
150	17	83	165	330	495	660	

The AC power dissipation of output and bidirectional buffers = 0.030 mW/MHz

where

f = the maximum system frequency

C = the output load capacitance in pF

0.20 = fraction of buffers switching in each cycle

Table 5–6 shows a representative range of values for  $P_{ACOUT}$ .

Table 5-6. Output and Bidirectional Buffer AC Power Dissipation (PACOUT) Examples (in mW)

Average Number		pF • MHz (per output)*							
of Simultaneously Switching Outputs	31	31 63 125 250 500 850							
6	5.58	11.34	22.50	45.00	90.00	153.00	216.00		
12	11.16	22.68	45.00	90.00	180.00	306.00	432.00		
25	23.25	47.25	93.75	187.50	375.00	637.50	900.00		
50	46.50	94.50	187.50	375.00	750.00	1275.00	1800.00		
75	69.75	141.75	281.25	562.50	1125.00	1912.50	2700.00		

<sup>\*</sup>pF \*MHz = SUM (loading for each pin in largest SSO group) \* SUM (toggle frequency of each output

# Estimation of I/O Buffer DC Power Dissipation (PDC)

The DC power dissipation of input buffers is so small as to be considered negligible and is not calculated.

The DC power dissipation of output and bidirectional buffers is determined by the following formula:

where the terms VOL and (VDD - VOH) are typically assumed to be 0.30V, when used for the determination of PDc. The terms tH and tL are decimal numbers determined by the duty cycle of the output waveform. They represent, respectively, the waveform's high and low periods.

Table 5-7 shows a representative range of values for PDCOUT.

Table 5-7. Output and Bidirectional Buffer DC Power Dissipation (PDCOUT) Examples\* (in mW)

Average Number	Output Drive Strength (I <sub>OL</sub> )				
of Outputs	3.2 mA	8 mA*	12 mA		
25	36	80	100		
50	72	160	200		
75	108	240	300		
100	144	320	400		
125	180	400	500		
150	216	480	600		
175	252	560	700		

<sup>\*</sup>assuming 50% duty cycle

# 5.10.2 Internal Gate Power Dissipation

The power dissipation of one internal basic cell is 0.010 mW/MHz.

$$PG = 0.010 * n * f * 0.20 (mW)$$

where

n = the total number of basic cells used for internal logic design, including internal basic cells for I/O buffers

f = the maximum system frequency

0.20 = factor reflecting Fujitsu's observation that in the average design, 20 percent of all buffers switch in each cycle.

Table 5-8 shows representative range of values for Pg.

Table 5-8. Internal Basic Cell Power Dissipation (PG) Examples

	System Clock Frequency					
Active Gates <sup>1</sup>	1 MHz	5 MHz	10 MHz	20 MHz	30 MHz	40 MHz
200	2	10	20	40	60	80
400	4	20	40	80	120	160
800	8	40	80	160	240	320
1600	16	80	160	320	480	640
3200	32	160	320	640	960	1280
6400	64	320	640	1280	1920	2560
12800	128	640	1280	2560	3840	5120
25600	256	1280	2560	5120	7680	10240
			}	,		

Note: Active Gate count is typically (Utilized gates)\* (Activity Factor) (usually 20%)

# 5.10.3 RAM Cell Power Dissipation

When the RAM enable input (RE) is at a logic high, the RAM is disabled and the power dissipated by the RAM (PRAM) = 0 mW.

When the RAM enable input is at a logic low, the RAM is enabled and power is dissipated by the RAM. Assuming that half of the address input terminals are switching at the RAM operating frequency *fRAM*, the power dissipation of a RAM cell is determined by the following formula:

$$PRAM = (0.63 + (0.008 * wp) + (0.036 + (0.045/c)) * bp * fRAM + (7.5) + 01.13/c) * bp * 1.2 mW$$

where

wp = the physical word length (in basic cells) of the RAM

c = the columnar structure of the RAM (how many physical words wide it is)

bp = the physical bit size (in basic cells)

Table 5–9 shows a representative range of values for PRAM where fRAM = 25 MHz and c = 2.

Table 5-9. RAM Macro Power Dissipation (PRAM) Examples

RAM Macro Power Estimate Table			
Bit Width			
4	8	16	
40.45	57.45	91.45	
43.65	60.65	94.65	
50.05	67.05	101.05	
62.85	79.85	113.85	
88.45	105.45	139.45	
139.65	156.65	190.65	
	4 40.45 43.65 50.05 62.85 88.45	Bit Width           4         8           40.45         57.45           43.65         60.65           50.05         67.05           62.85         79.85           88.45         105.45	

# 5.10.4 ROM Cell Power Dissipation

When the ROM enable input (RE) is at a logic high, the ROM is disabled and the power dissipated by the ROM (*PROM*) = 0 mW.

When the ROM enable input is at a logic low, the ROM is enabled and power is dissipated by the ROM. Assuming that half of the address input terminals are switching at the ROM operating frequency from, the power dissipation of a ROM cell is determined by the following formula:

$$PROM = (0.81 + (0.007 * Wp) + (0.001 + (0.200/c)) * bp * fROM$$

where

wp = the physical word length (in basic cells) of the ROM

c = the columnar structure of the ROM (how many physical words wide it is)

bp = the physical bit size (in basic cells)

Table 5–10 shows a representative range of values for PROM where fROM = 25 MHz and c = 2.

Table 5-10. ROM Power Dissipation (PROM) Examples (in mW)

Depth	ROM Macro Power Estimate Table  Bit Width			
	32	43.075	63.075	103.075
64	45.875	65.875	105.875	
128	51.475	71.475	111.475	
256	62.675	82.675	1222.675	
512	85.075	105.075	145.075	
1024	129.875	149.875	189.875	

# 5.10.5 Determination of Maximum Delay Multipliers

Once the maximum junction temperature of the array has been calculated, Table 5–11 must be consulted for the appropriate maximum delay multiplier.

Junction Pre-layout Post-layout Temperature 5 V+5% 5 V+10% 5 V+5% 5 V+10% (T)1.65 Ti ≤ 60°C 1.75 1.55 1.65 1.70 1.70 1.80 1.60 60°C <Tj ≤ 70°C 70°C <Ti < 80°C 1.75 1.85 1.65 1.75 1.80 1.90 1.70 1.80 80°C <Ti ≤ 90°C 90°C <Ti < 105°C 1.85 1.95 1.75 1.85 105°C <Tj < 120°C 1.90 2.00 1.80 1.90 120°C <Tj < 130°C 1.95 2.05 1.85 1.95 130°C <Tj ≤ 140°C 2.00 2.10 2.00 1.90 140°C <Tj ≤ 150°C 2.05 2.15 1.95 2.05

Table 5-11. Maximum Delay Multipliers

#### 5.10.6 Determination of Minimum Delay Multipliers

The minimum delay multipliers are almost exclusively dependent on the range of ambient temperature. For each ambient temperature range in which the gate array will be used, Table 5–12 shows the minimum delay multiplier. The power supply variation from 5 percent to 10 percent has no noticeable effect.

Lowest Ambient Pre-layout Post-layout Temperature 5 V±5% 5 V±10% 5 V±5% 5 V±10% (TA) 0.35 0.35 0.40 0.40 °C <TA<70°C 0.30 0.30 0.30 0.30 -20°C <TA<70°C 0.25 0.25 0.25 0.25 -40°C <TA<70°C 0.25 0.25 0.25 0.25 -40°C <TA<85°C -55°C <TA<125°C 0.20 0.20 0.25 0.25

Table 5-12, Minimum Delay Multipliers

#### 5.11 Calculating Delays for Test

# 5.11.1 Pre-layout Delay Calculations for Delay Test (AC Test)

The min/max delays for the delay test are determined by taking the sum of the typical delays and multiplying it by the appropriate minimum or maximum delay factor. The maximum delay figure must be rounded up to the next highest 0.1 ns, while the minimum delay figure must be rounded down to the next lowest 0.1 ns. The equation shown for typical delay calculation is repeated here and also shown in its modified form. The delay factors used are those for pre-layout in the AU and CG21 technologies. For simplicity's sake, the maximum delay multipliers in this example are unmodified by junction temperature factors. The figures used in this example are those derived from the delay calculations for the sample circuit in Figure 5–2 at the start of this chapter.

Typical delay:

$$tod = 0.5 + 0.6 + 1.6 + 0.4 = 3.1 \text{ ns}$$

Maximum delay (rounded up to 0.1 ns):

$$tod = (0.5 + 0.6 + 1.6 + 0.4) \times 1.65 = 5.115 = 5.2 \text{ ns}$$

Minimum delay (rounded down to 0.1 ns):

$$tod = (0.5 + 0.6 + 1.6 + 0.4) \times 0.35 = 1.085 = 1.1 \text{ ns}$$

# 5.11.2 Pre-layout Delay Calculations for DC Test, Function Test, and High Impedance Test

The minimum and maximum delays for these tests are determined by multiplying the typical delays for each cell individually by the delay factors. The resulting figures for both maximum and minimum delays are rounded up to the next 0.1 ns for each cell. The final figures for each unit cell of the path are totaled. The delay calculation used earlier is repeated here and is also shown calculated for the DC, Function, and High Impedance tests. The delay factors used are those for pre-layout in the AU and CG21 technologies.

Typical delay (rounded up to 0.1 ns):

$$tod = 0.5 + 0.6 + 1.6 + 0.4 = 3.1 \text{ ns}$$

Maximum delay (delay for each gate rounded up to the next 0.1 ns):

$$tpd = (0.5 \times 1.65) + (0.6 \times 1.65) + (1.6 \times 1.65) + (0.4 \times 1.65)$$
$$= 0.825 + 0.99 + 2.64 + 0.66$$
$$= 0.9 + 1.0 + 2.7 + 0.7 = 5.3 \text{ ns}$$

Minimum delay (delay for each gate rounded up to the next 0.1 ns):

$$tpd = (0.5 \times 0.35) + (0.6 \times 0.35) + (1.6 \times 0.35) + (0.4 \times 0.35)$$
$$= 0.175 + 0.21 + 0.56 + 0.14$$
$$= 0.2 + 0.3 + 0.6 + 0.2 = 1.3 \text{ ns}$$

Minimum/maximum delays are also calculated this way for minimum clock pulse width, minimum data set-up time, minimum data hold time, preset timing, and clear timing. The values of the maximum and minimum delay multipliers shown above apply to pre-layout calculations only; different factors are used for post-layout analysis.

# 5.12 Delay Parameters for Compiled Cells

#### 5.12.1 Compiled Cell Construction

The compiled cell is a RAM or a ROM that is automatically generated by Fujitsu-proprietary compilers. It is recommended that no more than four compiled cells be employed within a gate array. Since the compiled cell is a hardware macro, it is important that its dimensions allow it to be placed within the area of the basic cell matrix. It is also required that the remainder of the basic cell matrix be left as close to rectangular as possible (no T- or L-shapes) to facilitate the automatic routing of unit cell interconnections. Space must also be reserved along the outer edges of the macros for internal I/O cells. Unused address inputs of all compiled cells and unused data input terminals of RAM must be tied low to Z00 cells.

# 5.12.2 Compiled Cell Configuration

The macro's logic parameters must be converted to physical parameters in order that the macro be laid out in the most efficient manner. The resulting compiled cell, or macro, will be physically distributed across a number of columns of basic cells and, within limits, may be one, two, four, or eight words wide, regardless of the number of bits per word.

This columnar configuration (the width of the memory matrix in words) is referred to as the "c" value for the purposes of this discussion. This c value determines the physical (in basic cells) word and bit length (not logical length). In many cases, more than one value of c can be used, allowing alternate configurations of the macro. For example, Table 5–13 below shows the allowable c values for single- and dual-port RAM. For a 256 (word) x 8(bit) RAM, any value (c = 1 through c = 8) can be used.

 Number of Words
 Number of Bits/Word
 c Value

 4 to 256
 8 to 72
 1

 8 to 512
 4 to 36
 2

 16 to 1024
 2 to 18
 4

32 to 2048

Table 5-13. Single- and Dual-Port RAM Columnar Configurations

Procedures detailed in the Design Manual allow the size of the physical word, the size of the physical bit, the basic cell count, and the number of address lines needed to be derived from the c value. Table 5–14 below illustrates the calculated parameters for a single-port 256 x 8 RAM.

1 to 9

8

Table 5-14. Calculated Parameters for Single-Port 256 x 8 RAM

			c Value					
Parameter	Symbol	1	2	4	8	Unit		
Physical Word	wp	256	128	64	32	BC		
Number of Address Lines	t	8	8	8	8	units		
Physical Bit	bp	8	16	32	64	BC		
Total Basic Cells	_	6000	4592	4392	5016	ВС		
X-Dimension	×	20	28	44	76	ВС		
Y-Dimension	Y	300	164	98	66	ВС		
Power Dissipation	Р	89.9	158.2	302.5	595.0	mW		

The optimum configuration must be determined by the requirements of the design itself. As the table above shows, a macro configured with a smaller c value will use more basic cells but will require less power dissipation than a macro configured with a larger c value. The difference in power consumption at each end of the spectrum of possible configurations varies much more widely than does the difference in the number of basic cells used.

If the array design contains compiled cells, additional delay parameters, set out in full in the appropriate Design Manual, must be added to the basic delay equation explained in the previous section. Table 5–15 below shows the delay parameter for a single-port 245 x 8 RAM. As the table shows, the columnar configuration (c value) of a compiled cell has minimal influence on the basic delay times of the macro.

Read Operation

Table 5–15. Delay Parameters for a Single-Port 256 x 8 RAM (AU Series)

Symbol	Chosen Value of "c"				
Symbol	1	2	4	8	
t <sub>RC</sub>	21.72	21.44	21.41	21.37	
t <sub>AA</sub>	20.79	20.64	20.65	20.71	
t <sub>RA</sub>	19.79	19.71	19.68	19.83	
t <sub>OH</sub>	5.95	5.84	5.94	6.34	
t <sub>RH</sub>	2.85	2.86	2.87	2.90	
twc	21.72	21.44	21.41	21.37	
t <sub>RW</sub>	15.27	14.94	14.87	14.88	
t <sub>AW</sub>	18.57	18.24	18.17	18.18	
t <sub>AS</sub>	3.30	3.30	3.30	3.30	
t <sub>WP</sub>	11.82	10.94	10.54	10.38	
t <sub>DW</sub>	10.17	9.28	8.84	8.61	
twa	3.15	3.14	3.19	3.24	
t <sub>DH</sub>	3.59	3.66	3.81	4.11	
	taa traa toh trah twc traw taw tas twe tow	Symbol         1           t <sub>RC</sub> 21.72           t <sub>AA</sub> 20.79           t <sub>RA</sub> 19.79           t <sub>OH</sub> 5.95           t <sub>RH</sub> 2.85           t <sub>WC</sub> 15.27           t <sub>AW</sub> 18.57           t <sub>AS</sub> 3.30           t <sub>WP</sub> 11.82           t <sub>DW</sub> 10.17           t <sub>WR</sub> 3.15	Symbol         1         2           t <sub>RC</sub> 21.72         21.44           t <sub>AA</sub> 20.79         20.64           t <sub>RA</sub> 19.79         19.71           t <sub>OH</sub> 5.95         5.84           t <sub>RH</sub> 2.85         2.86           t <sub>WC</sub> 21.72         21.44           t <sub>RW</sub> 15.27         14.94           t <sub>AW</sub> 18.57         18.24           t <sub>AS</sub> 3.30         3.30           t <sub>WP</sub> 11.82         10.94           t <sub>DW</sub> 10.17         9.28           t <sub>WR</sub> 3.15         3.14	Symbol         1         2         4           t <sub>RC</sub> 21.72         21.44         21.41           t <sub>AA</sub> 20.79         20.64         20.65           t <sub>RA</sub> 19.79         19.71         19.68           t <sub>OH</sub> 5.95         5.84         5.94           t <sub>RH</sub> 2.85         2.86         2.87           t <sub>WC</sub> 21.72         21.44         21.41           t <sub>RW</sub> 15.27         14.94         14.87           t <sub>AW</sub> 18.57         18.24         18.17           t <sub>AS</sub> 3.30         3.30         3.30           t <sub>WP</sub> 11.82         10.94         10.54           t <sub>DW</sub> 10.17         9.28         8.84           t <sub>WR</sub> 3.15         3.14         3.19	

14.88 18.18 3.30 10.38 8.61 3.24 4.11

Frequency of Operation: 5MHz

All units are in ns

## Chapter 6 - Quality and Reliability

#### **Contents of This Chapter**

- 6.1 Introduction
- 6.2 Engineering Testing
- 6.3 In-process Inspection and Quality Control
- 6.4 Reliability Theory
- 6.5 Reliability Testing
- 6.6 Test Methods and Criteria

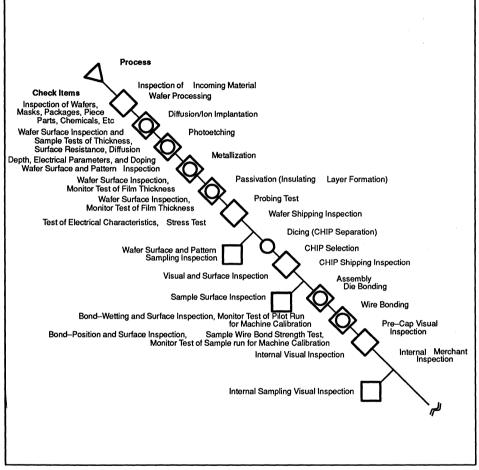
#### 6.1 Introduction

Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

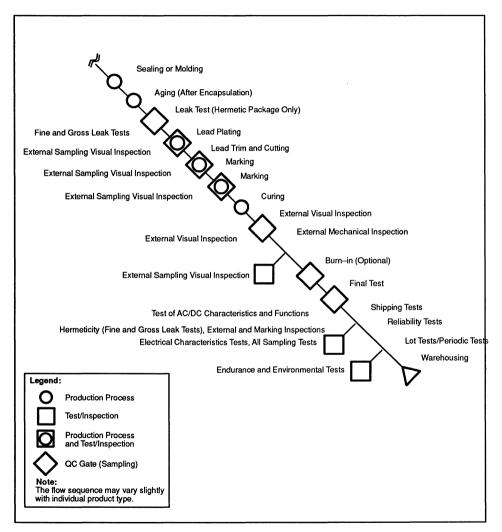
Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.



**Quality Control Processes at Fujitsu** 



Quality Control Processes at Fujitsu (Continued)

#### 6.2 Engineering Testing

Engineering testing is the heart of reliability and quality control. The reliability engineering department plans and performs most engineering testing. Whenever a device is developed, it must undergo engineering approval tests. After the device passes these tests, production engineering approval tests are performed on a representative sample of the device. All factors that could influence production of the device are examined. Only if all conditions are favorable and the device passes thorough testing, can the new device go into production.

Tables 6–1a through 6–1d show a sampling plan for engineering testing. These tests are in compliance with MIL-STD-883, Class B. When a change in production (e.g., a material change) is needed, engineering tests are performed on specific items for the change.

Since the representative samples tested must accurately reflect the reliability of the device, the following conditions must also be satisfied: the functions performed by the same basic circuit; the same processing techniques, materials, parts and packages used; and the same processing followed at the same factory.

Table 6-1a. Sampling Plan for Engineering Testing: Endurance Test

Test items	MIL-STD-883	LTPD* (%)	Acceptance number**	Note
High-temperature storage 150°C	1008 C	7	1	
High-temperature continuous operation	1005 D	7	1	
150°C or 125°C				
High-temperature continuous operation 125°C	1055 D	5	2	
Low-temperature continuous operation -55°C	(1055 C or D)	7	1	As applicable
High-temperature high-humidity storage	_	7	1	Plastic package only
85°C, 85% RH				
High-temperature high-humidity continuous	(1005 C or D)	7	1	Plastic package only
operation 85°C, 85% RH				

Lot test percent defects

<sup>\*\*</sup> Number of failures permitted per lot

Table 6–1b. Sampling Plan for Engineering Testing: Environmental and Mechanical Test

Test Items	MIL-STD-883	LTPD (%)	Acceptance number	Note
External visual inspection	2009	15	1	Same sample
Physical dimensions	2016	15	1	' ·
Radiophotography	2012	3 devices	0	
Internal visual inspection	2013	15	0	
Lead integrity: Tension Bending stress Lead fatigue	2004 A B B	15 15 15	0 0 0	Devices which failed in electrical characteristics test are acceptable to this test. Each test is performed on one third of the leads of each sample.
Resistance to soldering heat		7	1	Same sample
Temperature cycling	1010 C	7	1	1
Thermal shock	1011 A	7	1	
Vibration, variable-frequency	2007 A	<del></del>	· · · · · · · · · · · · · · · · · · ·	
Mechanical shock	2002 B	1 10	1 1	
Constant acceleration	2001 D	1 "		
Seal: (Fine and gross leak checks)	1014 A C 2015	7 7 40 devices	1 1	Hermetic package only  Devices which failed
	2000	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	·	in electrical characteristics test are acceptable to this test.
Solderability (260°C)	2003	15	1	Devices which failed in electrical characteristics test are acceptable to this test.
Solderability (230°C)	_	15	1	Devices which failed in electrical characteristics test are acceptable to this test.
Internal water-vapor content	1018	3 devices	0	Hermetic package only
Electrostatic discharge sensitivity	3015 A	15	1	
Pressure-Temperature-Humidity Storage (PTHS) 121°C, 2 atm.	_	15	1	Plastic package only

The following tests are performed only when required or when requested by the customer.

Table 6–1c. Sampling Plan for Engineering Testing: Environmental and Mechanical Test (Optional)

Test items	MIL-STD-883	LTPD (%)	Acceptance number	Note
Bond strength	2011 D (or C)	15	2 wires	34 wires/4 devices
Die shear strength	2019	3 devices	0	Hermetic package only
Moisture resistance	1004	15	0	
Salt atmosphere (corrosion)	1009 A	15	0	
Vibration fatigue	2005	15	0	
Immersion	1002 B	15	0	
SEM inspection of metallization	2018	3 devices	0	
Particle impact noise detection (PIND) test	2020 B	15	1	Hermetic package only
Lid torque	2024			Frit sealed package only, as applicable
Adhesion of lead finish	2025			As applicable

Table 6-1d, Sampling Plan for Engineering Testing: Continuity Test

Test item	MIL-STD-883	LTPD (%)	Acceptance number	Note
Continuity check	_	5	2	Plastic package only

#### 6.3 In-process Inspection and Quality Control

Every department involved in the manufacturing process is responsible for the quality-control inspection in its sphere of operation. In-process checks, sampling tests, and other inspections are assigned so that each department has certain allotted tasks for which it takes full responsibility. This total control system has rationalized overall operations dramatically.

### 6.3.1 In-process Checks (Including screening)

In-process checks are performed after each step critical to the next process in wafer processing and assembly. Defective or substandard products are weeded out at an early stage. Testing falls into the following three categories:

- (a) Probe testing, chip selection, and final testing. These are defined for each process.
- (b) Voluntary checks. These include inspection of the wafer surface after window opening (before the diffusion process) and inspection of the wafer surface after the metallization.
- (c) 100 percent screening. This includes the aging and visual inspection performed during wafer processing and assembly.

#### 6.3.2 In-process Sampling Test

The in-process sampling test is performed as a part of process quality control. The Manufacturing and QC departments check randomly drawn samples at key points in the manufacturing process to check process and facility conditions. This helps in maintaining product quality at the customary high level. The following items are checked in these sampling inspections or monitoring:

 (a) Surface resistance after diffusion, film thickness, evaporated or sputtered electrode thickness, and device characteristics

- (b) Product quality (checked by visual inspection of the chip surface)
- (c) Bonding machine calibration, visual inspection and bond strength after wire bonding, product appearance, marking permanency

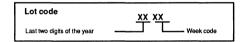
#### 6.3.3 In-process Inspection

The Manufacturing and QC departments perform stringent quality checks between major processes to ensure the highest quality. The following four types of inspections are performed:

- (a) Incoming materials, parts, and chemicals Inspection
- (b) Wafer shipping inspection
- (c) Chip shipping inspection
- (d) Shipping test

#### 6.3.4 Lot Configuration

A "lot" consists of the same devices produced over a stated period, having the same design and using the same processing techniques, materials, and production line. In addition to the Fujitsu logo, part number, and other markings, each device is marked with a lot code as shown below.



#### 6.4 Reliability Theory

#### 6.4.1 Estimating the Failure Rate

The graph of a component failure distribution is usually a downward–bowed curve, often called the bathtub curve (Figure 6–2). Life tests show that the instantaneous failure rate decreases with time and graphs as a straight line on a Weibull probability chart (Figure 6–3). Shape parameter m, which shows the instantaneous failure rate, is between 0.3 and 0.7. (In an exponential distribution, the instantaneous failure rate does not change and m = 1. As m becomes smaller than 1, the instantaneous failure rate decreases with time.)

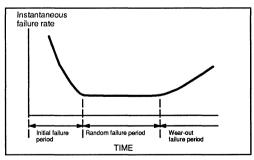


Figure 6-2. Distribution of Component Failure

Usually, the failure rates during the initial and random failure periods are the most important for semiconductors. Figure 6–3 shows an example of life test data graphed on a Weibull probability chart.

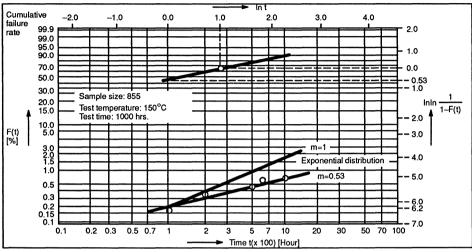


Figure 6-3. Example of Life Test Data on IC

#### 6.4.2 Accelerated Life Test

Modern applications require an extremely low failure rate for semiconductors. To guarantee such strict quality requirements, Fujitsu uses an accelerated life test. There is no fixed acceleration rate for semiconductors but, since semiconductor failure is usually caused by physical and chemical changes in materials, an acceleration rate can be calculated from the Arrhenius equation below for the progress speed of physical and chemical phenomena (assuming the R is proportional to the degradation speed):

 $R = A \exp(-Ea/kT)$ 

where:

R: Reaction rate

A: Proportionality constant

Ea: Activation energy

k: Boltzmann constant

T: Absolute temperature

The proportionality constant A corresponds to the component reliability. The activation energy,  $E_a$ , depends on the component's materials and their combination, but it ranges from 0.3 to 1.35 eV for semiconductors. This equation does not fit the data perfectly because it assumes that the failure rate is affected only by temperature when, in fact, there are many contributing factors. However, the equation does give a good rough fit. Using the equation on data from the accelerated life test, engineers can estimate and guarantee the field failure rate with reasonable accuracy.

The calculation method for the field failure rate is given below for Fujitsu semiconductor products. Although this method is not generally accepted yet, it has been found to be useful.

- Calculate the junction temperature (Tj(op)) for actual use from the temperature rise (Tj) and the ambient temperature (Ta) under an average load (do not use the worst–case load),Tj(op) = ΔTj + Ta.
- (2) Calculate the junction temperature (Tjt) for a life test. For a high-temperature storage test, Tjt equals Ta (the storage temperature). For a continuous operation test, the temperature rise

under load plus the ambient temperature (25°C except for high-temperature operation) for an operating temperature,  $Tjt = \Delta Tj + Ta$ .

(3) Calculate the acceleration rate (α) from the difference of Tj(op) and Tjt using Figure 6–4.

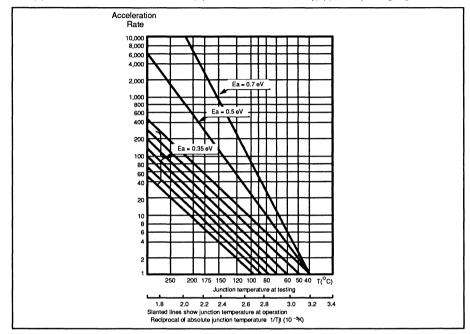


Figure 6-4. Acceleration Rate vs. Junction Temperature

(4) If planning reliability testing or calculating reliability in the field from data obtained in steps (1) to (3), determine the coefficient γ for the 60% confidence level in Table 6–2 from the number of defective units allowed or from the total number of failures found in the test.

Reliability = 
$$\frac{n}{\alpha NT}$$
 x  $\gamma$  x 10<sup>9</sup> [FIT]

#### where:

- N: Number of samples
- T: Total test time (hrs)
- n: Number of failed samples in test

No. of failures	Confidence level				
Tro. or railores	60%	90%			
0	(0.92)	(2.30)			
1	2.02	3.89			
2	1.55	2.66			
3	1.39	2.23			
4	1.31	2.00			
5	1.26	1.85			
6	1.22	1.76			
7	1.20	1.68			
8	1.18	1.62			
9	1.16	1.58			
10	1.15	1.54			

Table 6-2. Determination of Coefficient

The above equation applies only when n/N is equal to or less than 10% for the total test time, T. If n/N exceeds 10 percent, use the following method of calculation: divide the total test duration time, T, into subsections,  $\Delta ti$  (i = 1,2, . . . , m), so that for each  $\Delta ti$  the failure rate, (ni+1-ni)/(N-ni) (where ni is the cumulative number of failed samples for  $\Delta ti$ ), does not exceed 10 percent. Calculate (N-ni)  $\Delta ti$  for each time section  $\Delta ti$ . Calculate the summation  $\Sigma (N-ni)$   $\Delta ti$  for all the time sections in T. The summation  $\Sigma (N-ni)$   $\Delta ti$  must then be substituted for NT in the above equation.

#### 6.4.3 Failure and Causes

Circuit format differences, package types, and operating environments can change the mechanisms of IC failures, so it is difficult to foresee which factor will be the most important in a failure mechanism. Figure 6–5 shows specific electrical failures for ICs, their most common causes, and general corrective actions. Causes of IC failures are largely the same as for planar transistor failures, but the following problems are more common or specific to ICs:

- (a) Surface degradation
- (b) Flaws in an evaporated or sputtered metal film
- (c) Contact failures due to an increased number of wire bondings per package
- (d) Package failures due to an increased number of external leads

Table 6–3 lists failures with their most common causes, and Table 6–4 shows the relationship between operating environments and failure causes. Test items can be listed only if the failure cause can be pinpointed by the test.

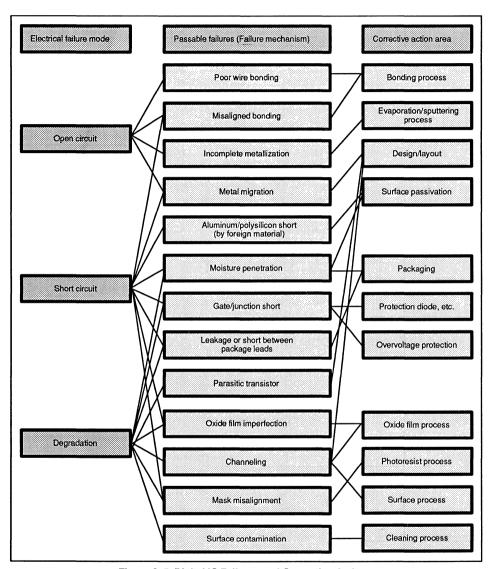


Figure 6-5. Digital IC Failures and Corrective Actions

Table 6-3. Process Defects Analysis

Defect Area	Defect mechanism	Frequency			Source		
71.00			Design	Factory Process Control	Manuf. Tech.	Operator Skill	User Application
Junction	Junction failure due to current crowding	High	•				•
(Internal)	Metal migration	Low	•	•	•	•	
Junction	Oxide film imperfection (Pinhole, crack, void, etc.)	Medium		•		•	
(Surface)	Impurity contamination	High	•	•		•	
	Metal peeling	Medium		•	•	•	
	Mask misalignment	Medium				•	
Inter-	Incomplete metallization	Medium		•	•	•	
connection	Improper metallization	Medium					
	Metal over-stress	High					•
	Aluminum corrosion	Medium		•	•	•	· · · · · · · · · · · · · · · · · · ·
	Aluminum migration	Medium	•			•	
	Bonding peel	High			•	•	
Wire	Purple plague	Medium	•		•	•	
	Wire over-stress	High				•	•
	Particle/wire short	Low				•	
	Leakage	Medium			•	•	
Package	Die bond failure	Low	•		•	•	
	Lead breakage	Medium			•		•
Others	Package corrosion	Medium	•	•	•		•
	Chip crack	Medium			•	•	•
	Seal contamination	Low		•	1	•	

Table 6-4. Relationship between Failure Causes and Analytical Test Methods

		Test										
Failure Cause	Solder- ability (2003.2)	Temper- ature Cycling (1010.2)	Thermal shock (1011.2)	Constant Acceleration (2001.2)	Mechanical shock (2002.2)	Vibration, variable frequency (2007.1)	Lead fatigue (2004.2)	Baro- metric pressure reduced (1001)	Moisture resistance (1004.2)	Salt atmos- phere (1009.2)	Vibration fatigue (2005.1)	Vibration noise (2006.1)
Bond integrity (Chip or wire)				•	•	•						
Cracked chip		•	•		•							•
Internal structural defect					•	•						
Contamination-/ contact-induced short		•			•	•						•
Wire or chip breakage					•	•						
Glass crack	•	•	•		•		•	•				
Lead fatigue contamination of junction (Surface)	•		•				•					•
Thermal fatigue		•										
Seal integrity		•										
Seal contamination				•	•	•						•
Leakage		•	•				•	•	•	•		
Package/material integrity		•	•		•			•	•	•		

#### 6.5 Reliability Testing

Reliability testing includes three types of tests—lot tests, periodic tests, and "occasional" tests. This section explains the details of each test in turn.

#### 6.5.1 Lot Tests

There are two types of lot tests, Group A and Group B. Group A and Group B tests are performed on items that are tested regularly, usually every week. Table 6–5 lists the specific lot tests.

Details of individual tests vary with the product under test, but all samples are selected at random from every weekly lot. Tests are not performed in any particular order unless specified, but are performed for each device type.

Note that the high-temperature storage and continuous-operation tests for Group B usually take 500 hours, although they may take only 168 hours in special cases. Good samples are returned to their lots after non-destructive testing. No-good samples and samples that have undergone destructive testing are destroyed.

#### 6.5.2 Periodic Tests

Particulars of the periodic tests are also listed in Table 6–5. There are two types of periodic tests: Group C tests and Group D tests. Group C tests are performed on items that are tested regularly, usually every 13 weeks. Group D tests include special reliability tests and very long life tests. The Group D tests are usually done once every 26 weeks.

Details of individual tests vary with the product under test, but all samples are selected at random. Tests are not performed in any particular order unless specified, but are performed for each device type. Note that the high-temperature storage and continuous-operation tests for Group C take 1000 hours and those for Group D take 3000 hours.

Table 6-5. Sampling Plan for Reliability Testing

C	0	Device classification		Dev	ice group 1	De	Device group 2		
Group	Subgroup	Test items			Sampling plan				
	A1	External visual i	nspection	100% test of sampled devices (All sampled device					
Α	A2		Function test		LTPD 5%	$A_c = 0$			
^	А3	Electrical	Static characteristics		LTPD 5%	$A_c = 0$			
	A4	Characteristics	Dynamic/Switching characteristics		LTPD 5%	A <sub>c</sub> = 0			
				Sample size	Acceptance number	Sample size	Acceptance number		
	B1	Physical dimens	ions	9	1	6	1		
	B2	Environmental	Resistance to solvant +temp-cycling	9	18	9	18		
		tests	Thermal shock test	9	18	9	18		
	В3		Mechanical environmental test	9	1	9	1		
	B4-I	Solderability (23	Solderability (230°C, 5s)1		1	3	1		
	B4-II	Solderability (26	Solderability (260°C, 5s)1		1	3	1		
	B5	Lead integrity <sup>1</sup>	Lead integrity <sup>1</sup>		1	3	1		
В		Pressure-tempe storage <sup>2</sup>	essure-temperature-humidity		13	3	13		
	B6	Pressure-tempe bias <sup>2</sup>	rature-humidity	9	17	3	17		
	B7		High-temperature storage	14	14	7	14		
	B8		Continuous operation	24	14	11	14		
	B9		High-humidity storage 85° C. 85% RH <sup>2</sup>	24	14	11	14		
	C1		High-temperature storage	14	1 <sup>5</sup>	7	1 <sup>5</sup>		
С	C2	Endurance	Continuous operation	24	1 <sup>5</sup>	11	1 <sup>5</sup>		
-	СЗ	test	High-humidity storage 85° C. 85% RH <sup>2</sup>	24	15	11	1 <sup>5</sup>		
	D1	]	High-temperature storage <sup>6</sup>	14		7	<del></del>		
D	D2		Continuous operation	24		11			
	D3	1	High-humidity storage 85° C, 85% RH <sup>2,6</sup>	24	_	11			

Test cycle: Group A and B for every weekly lot, Group C every 13 weeks, Group D every 26 weeks

Notes

\*\*Electrical reject devices can be used in this test.

\*\*These tests are performed on resin-sealed devices.

\*\*This test takes 96 hours.

\*\*These tests normally take 500 hours. But if no defects are found in the first 168 hours, the lot can be passed and the test may be terminated.

\*\*These tests take 1000 hours.

\*\*These tests take 3000 hours.

\*\*This test takes 48 hours.

\*\*This test takes 48 hours.

<sup>&</sup>lt;sup>7</sup>This test takes 48 hours. <sup>8</sup>These tests take 100 cycles.

#### 6.5.3 Occasional Tests

Occasional tests are performed on products whenever necessary. The tests are similar to periodic tests, but their details are specified by the QC/Reliability Engineering Division according to the purpose of the test.

#### 6.6 Test Methods and Criteria

The reliability of Fujitsu ICs is assured by severe environmental and endurance testing. Test methods are usually based on Japan Industrial Standards (JIS), the standards of the Electronic Industrial Association of Japan (EIAJ), and MIL standards.

Reliability tests are performed for two reasons. Firstly, they check or guarantee the reliability of a type or a lot according to specified standards. Secondly, they are used to determine the failure rate or mode. The most appropriate test method is chosen for each test, and test results are processed in the most suitable manner. Fujitsu usually performs the tests listed in Tables 6–6, 6–7, and 6–8.

Table 6-6. Example of Reliability Testing

Test items	MIL-STD-883	Condition		
Resistance to soldering heat		260°C, 10s		
Temperature cycling	1010 C	-65°C (30 min.) to 150°C (30 min.), 100 cycles		
Thermal shock	1011 A	0°C (5 min.) to 100°C (5 min.), 100 cycles		
Vibration, variable-frequency	2007 A	20 to 2,000Hz, 20G		
Mechanical shock	2002 B	1,500G, 0.5ms		
Constant acceleration	2001 E	30,000G, 1 min, Y1 only		
Fine leak <sup>1</sup>	1014 A <sub>1</sub>	Using compressed helium 99.5 psig, 4 hrs.		
Gross leak <sup>1</sup>	1014 C	Using fluorocarbon 75 psig, 1 hr., 125°C		
Solderability	_	230°C, 5s		
Solderability	2003	260°C, 5s		
Lead fatigue	2004 B2	0.25kgf, 90°, twice		
PTHS/PTHB <sup>2</sup>	_	121°C, 2 atm		
High-temperature storage	1008 C	150°C, 1,000 hrs.		
Continuous operation	1005 A to D	125°C, 1,000 hrs.		
High-humidity storage <sup>2</sup>	_	85°C,85%RH, 1,000 hrs.		

Notes: 1 Applies to hermetic packages. 2 Applies to plastic packages.

Table 6-7. Example of Electrical Testing

Circuit classification	Characteristics	Bipolar	MOS
Gates	DC	V <sub>OH,</sub> V <sub>OL</sub> , II <sub>H</sub> , II <sub>L</sub> , I <sub>CC</sub> (I <sub>EE</sub> )	V <sub>OH</sub> , V <sub>O</sub> L, I <sub>IH</sub> , I <sub>IL</sub> , I <sub>DD</sub> (I <sub>sub</sub> )
	AC	Function	Function
Flip-flops	DC	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , I <sub>IL</sub> , I <sub>OH</sub> , I <sub>CC</sub> (I <sub>EE</sub> )	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , I <sub>IL</sub> , I <sub>DD</sub> (I <sub>sub</sub> )
	AC	Function	Function
Shift registers	DC	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , IIL, I <sub>OH</sub> , I <sub>CC</sub> (I <sub>EE</sub> )	V <sub>OH</sub> , V <sub>OL</sub> , II <sub>H</sub> , I <sub>IL</sub> , I <sub>DD</sub> (I <sub>sub</sub> )
	AC	Function	Function
Memories	DC	V <sub>OH</sub> , V <sub>OL</sub> , II <sub>H</sub> , I <sub>IL</sub> , ICC (I <sub>EE</sub> )	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , II <sub>L</sub> , (I <sub>OH</sub> ),(I <sub>OL</sub> )
	AC	Function	I <sub>DD</sub> (I <sub>sub</sub> ) Function
Random-logic devices	DC	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , I <sub>IL</sub> , I <sub>CC</sub> (I <sub>EE</sub> )	$V_{OH, V_{OL}, I_{IH}, I_{IL}, (I_{OH}), (I_{OL})}$
	AC	Function	$I_{DD} (I_{Sub})$ Function
Analog devices	DC AC	V <sub>IO</sub> , I <sub>IO</sub> , I <sub>I,</sub> V <sub>OM</sub> , V <sub>OH</sub> ,V <sub>OL</sub> , A <sub>V</sub> , K <sub>E2</sub> , N <sub>E</sub>	_

Table 6-8. Example of Electrical Criteria

Parameter	Limit value (in multiples of the absolute value)		
	Upper	Lower	
V <sub>OH</sub>	_	L x 0.9	
V <sub>OL</sub>	U x 1.1	_	
I <sub>IH</sub>	U x 2 (No leak: U x 1.1)	_	
I <sub>L</sub>	U x 2 (Leak: U x 2	_	
юн lcc(l <sub>EE</sub> ) lcc (lsuв)	U x 2 (Leak: U x 2		

<sup>&</sup>quot;U" and "L" stand for the upper and lower limits

# **Chapter 7 – Application Notes**

### **Contents of This Chapter**

Developing Test Patterns That Work with the Physical Tester Selecting the Best Package for Your ASIC Design

## **CMOS ASIC**

# Developing Test Patterns That Work with the Physical Tester

by J. Scott Runner

Fujitsu Microelectronics, Inc.

Copyright© 1990 by Fujitsu Microelectronics, Inc.

#### Introduction

This application note briefly describes the process of developing test patterns for the simulation and test of Fujitsu CMOS ASIC designs. This information supplements testing information found in the Design Manual for the appropriate Fujitsu CMOS ASIC technology.

#### Tests to be Created

Fujitsu supports the following five types of test

- a. DC test
- b. Dynamic function test
- c. High impedance test (Z-function test)
- d. Delay test (AC test)
- e. Scan test (optional for certain Fujitsu technologies)

The DC test measures DC characteristics such as  $I_{DDS}$ ,  $V_{OH}$ ,  $I_{LI}$ , and  $I_{LZ}$ , while the function test screens for manufacturing faults (metal and transistor faults, principally). The Z-function test augments the DC test and is required for circuits in which one or more enable signals from a 3-state buffer can be generated by logic deeper than one gate of complexity within the ASIC device. The delay test may be used to verify critical timing paths that are necessary for proper system operation.

Scan test methods are used to simplify the [process of testing for manufacturing defects traditionally uncovered by the function test. Automatic test generation is supported in conjunction with scan testing in the UHB/CG10 and AU/CG21 technologies as an option.

#### Overview of Test Vector Creation

For each set of test patterns defined as a test block, the customer must specify input states and output states (in either vector or wave format), and the timing of inputs and outputs (with bidirectionals being considered both an input and an output). Many designers rely on one of the Fujitsu-supported CAE workstations when generating test vectors, easing the burden of test pattern development. In these cases, the customer creates input stimuli for the workstation simulator, which then generates a print-on-change file containing the resulting output response and the associated input stimulus previously defined by the designer. The print-on-change file is converted by Fujitsu's workstation software into FTDL (Fujitsu Test Description Language), which is the accepted test pattern description format regardless of the method by which patterns are created.

### **Developing the Tester Timing Information**

Whether or not the patterns are generated on the CAE workstation, it is necessary for the customer to generate in the FTDL file a Common Block file, containing administrative information and the test type, and a Test Block file, containing the timing information for all chip inputs and outputs by group (discussed further in the Design Manual). The definition of this overall timing is critical to the success of the test program itself. For example, input timing defines when input signals will transition, while output timing defines when outputs will be compared with their expected values or measured at a transition point.

The designer is responsible for specifying the following timing parameters for the Test Block, depending on the specific type of test:

- a. Test cycle
- b. Grouping of inputs and, if necessary, outputs and bidirectionals
- c. Delay-to-transition (DT) time for each input group of non-return to zero (NRZ) signals
- d. Propagation time (tp) and pulsewidth (Wp) times for the positive-going pulse (PP) and negative-going pulse (NP) for each input group of return to zero (RTZ) signals
- e.\* Delay-to-strobe time (STB) point for each output group
- f.\* DT and STB times for bidirectionals
- g.\*\* T time in the SPATH statement for AC tests

This timing is established for the entire test block and is invariant until another test block is invoked. Therefore, test pattern timing is periodic, that is, a group of inputs may only transition at the time specified in the Test Block, which is relative to the beginning of the test cycle. This delay to transition time for inputs is programmed for each input group with the  $t_p$  parameter in the FTDL INTIM or BUSTIM statement.

Similarly, common output groups are strobed, or sampled, periodically at a time determined by the test cycle and the delay-to-strobe time specified in the OUTTIM or BUSTIM statement, or the  $T_p$  parameter in the FTDL SPATH statement in the case of an AC test.

#### **Determining Input and Output Timing Parameters**

During the function test, outputs should stabilize before being strobed. Therefore, the minimum permissible test cycle programmed by the TIMING statement in the Test Block should be set with consideration of the maximum propagation delay from any input to any output, and the respective DT and STB times for those groups should be set far enough apart in time to assure that the outputs are stable under maximum

<sup>\*</sup>Specified in DC, function, and Z-function tests

<sup>\*\*</sup>Applicable only to AC tests.

conditions. Similarly, if the output is strobed before the transition, it must be stable under minimum delay conditions.

Test patterns are required to be invariant over minimum and maximum delay conditions. This is verified in simulation by scaling the typical delays by multipliers representing process, temperature, and power supply variations. Similarly, the strobed or expected output states must be identical under typical, maximum, and minimum conditions. If a propagation delay from input to output is greater than the test cycle defined, output states may not fulfill this requirement (see Figure 1). Furthermore, designers should be careful that glitches or short pulses do not occur anywhere within this minimum/maximum window (see Figure 2).

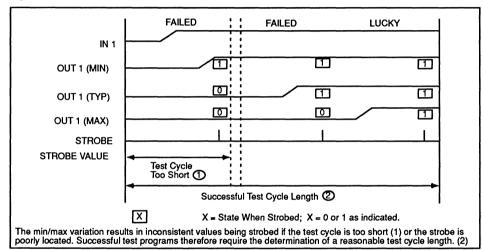


Figure 1. Determining a Successful Test Cycle Length

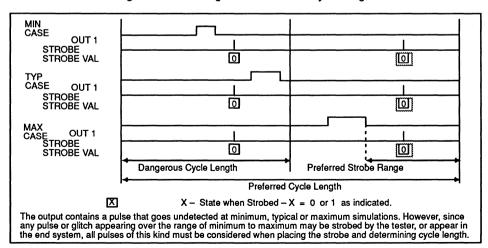


Figure 2. Determining Preferred Cycle Length

#### Generating Functional Input Stimulus Given Test Pattern Timing

One issue that must be considered when determining test pattern timing is the relationship between input signals, such as clock/data pairs, which must satisfy set-up and hold times. Other considerations guiding the timing definition are dependent on the particular circuit being tested, and on restrictions imposed by the tester. These restrictions are published in the Summary of Test Data Restriction section of Fujitsu's Design Manuals.

#### Tester Skew and its Compensation of Test Timing

The designer must pay particular attention to the issue of tester skew when determining input and output timing for Test Blocks; otherwise, the timing will not correctly represent the behavior of the device under test. Tester skew, specified for each technology in the Summary of Test Data Restrictions, is a result of the variation in the time at which a given signal generator triggers a transition or a comparator measures an output state. Several timings are affected by this skew.

#### Input-to-Input Skew

For the purpose of estimating the skew between two signal generators, (one driving data and the other driving its clock, for example), the driver skew, linearity of clocks, clock-to-clock skew, and jitter are collectively called driver accuracy, denoted tokerw.

In the case of data/clock pairs, the clocked data may fail either a set-up or hold time, depending on the direction of the skew. Therefore, when determining DT and  $t_p$  for data/clock pairs, the designer should adjust times to satisfy the following relationships (see Figure 3):

Set-up Time Criteria for Testing:  $(t_p(CLOCK) - DT(DATA)) >= t_S(MIN) + 2 * t_{DSKEW}$ Hold Time Criteria for Testing:  $(DT(DATA) - t_p(CLOCK)) >= t_H(MIN) + 2 * t_{DSKEW}$ 

Where  $t_S(MIN)$  and  $t_H(MIN)$  are the worst case set-up and hold times, respectively, sensitized from the internal circuit to the inputs,  $t_{DSKEW}$  is not directly specified in the Summary of Test Data Restriction; however,  $T_{ACC}$ , the overall system timing accuracy, is specified and can be substituted for  $t_{DSKEW}$  (see Section 7.2).

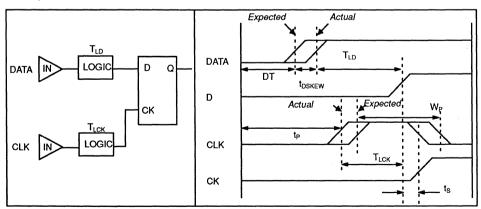


Figure 3. Input-to-Input Skew



#### Input-to-Output Skew

In addition to the skew incurred by the signal driver, skew is also introduced by the output comparator of the tester. This skew is dependent on the linearity of the strobe, pin-to-pin skew, skew between dual comparators, and the driver-to-comparator timing error. All factors are considered in the overall system timing accuracy, t<sub>ACC</sub>, which in turn affects output timing as shown in Figure 4.

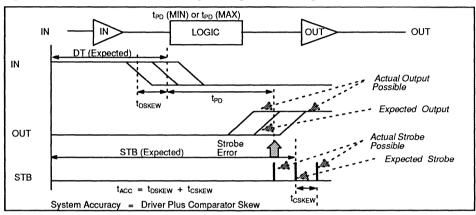


Figure 4. Input-to-Output Skew

#### Skew Effect on Input/Output Pairs - Minimum Delay Case

The STB (or T parameter in the SPATH statement) should expect an output transition at a time relative to the stimulated input transition dictated by

$$(STB - DT) > = t_{PD(MIN}) - t_{ACC}$$

where STB is the strobe point of the output under consideration, DT is the DT time of the stimulating input of interest, and  $t_{PD(MIN)}$  is the minimum propagation delay from this input to the strobed (or measured) output. In the case of the AC test, the quantity (STB - DT) should be replaced by the minimum T parameter in the SPATH statement. Note that if the path delay spans a test cycle boundary, STB should be set to STB plus the test cycle period.

#### Skew Effect on Input/Output Pairs - Maximum Delay Case

The complementary case occurs for maximum delay measurements, as described by

$$(STB - DT) \le t_{pd(MAX)}) + t_{ACC}$$

Note that these guidelines regarding the specification of test data timing as affected by tester skew apply to DC and Z-function tests as well. In these cases, the same rules apply as for the function test.

Again, for the specific values of  $t_{ACC}$ , and  $t_{DSKEW}$ , please refer to the Summary of Test Data Restrictions in the Fujitsu Design Manual for the appropriate technology. A designer interested in a methodical approach to the generation and verification of a good set of test vectors must consider the tester hardware on which it is running. Fujitsu has simplified designer responsibility by providing this information as part of the Test Block Information.

However, a lack of implementation and careful analysis of the timing characteristics of the circuit may result in a poor or unfeasible test, resulting in schedule delays or reduced device yield. Therefore, plan a test approach early, design for testability, and consider the effect and operation of the physical tester.



# **ASIC** Packaging Information

# Selecting the Best Package for Your ASIC Design

by J. Scott Runner

Fujitsu Microelectronics, Inc.

Copyright© 1990 by Fujitsu Microelectronics, Inc.

#### 1.0 Introduction

The widely varying degrees of complexity (gate count) of Fujitsu's CMOS and BiCMOS devices and the flexibility of their I/O configurations combine to produce devices that take advantage of the broad selection of packages available from Fujitsu. However, the requirements for package selection go far beyond pin count as the sole determinant of the best package. Selection issues include surface mount versus through-hole, plastic versus ceramic, and exotic versus conventional packaging. In fact, Fujitsu offers over 100 packages and 1000 package-die combinations from which to choose. Compounding the selection problem is the effect of increasingly faster outputs coupled with higher drive and wider bus structure, resulting in greater numbers of simultaneously switching outputs (and thereby greater amounts of noise).

The result is that designers are finding ASIC packaging implementation to be an increasingly complex task. This application note provides information about ASIC packaging that is meant to simplify the designer's task. It provides designers with a review of the various Fujitsu packages and their electrical, thermal, and mechanical characteristics, as well as some problem-solving strategies for their use. Sections 2.0 and 3.0 address system requirements and package availability; Sections 4.0 and 5.0 discuss noise and thermal issues.

#### 2.0 How System Requirements Affect Package Choice

Section 2.0 presents considerations involved in the selection of packages from a system designer's perspective. Table 1 lists issues a designer must consider when determining the optimal packaging for an ASIC design.

Table 1. Considerations for Package Selection

 Manufacturing and Cost
 Speed Requirements

 Board Integration
 Package and Interconnect Delays

 Double-sided Component Mounting
 The Effect of Package on Noise

 Number of Packages
 Thermal Considerations

Number of Packages
Package Outline Area
Power Density Limitations

Producibility Quality

Board Layout Package Quality and Reliability
Package Construction Number of Devices

Packaging Complexity Noise

Manufacturing Flow Thermal Considerations

#### 2.1 Manufacturing and Cost

The manufacturing-related factors discussed below, although not directly related to the design of the device or the number of power and ground pins it requires, are nonetheless important in the choice of an ASIC package.

#### 2.1.1 Board Area

One of the most important issues is the board area consumed by a circuit. Some of the factors affecting overall board density are:

Integration (gates per square inch of board)

Double-sided mounting capability (integration)

Number of packages

Package outline area

Additional board space required (for spacing, resistors, capacitors, probe areas, etc.)

Power density area (discussed in Section 5.0)

The critical issue in board area reduction, however, is overall integration. For example, surface mount devices (SMDs) can be densely mounted on both sides of the board, making them ideal for systems demanding high package integration. But a large design integrated into a few very large Sea-of-Gates arrays, even if packaged in large, through-hole packages, may well consume less board space than the same design using surface mount plastic J-leaded chip carriers (PLCCs). The PLCC version would require more space because the PLCCs, although small in outline, cannot house as large a die and therefore require the design to be partitioned into a greater number of devices.

Figure 1 illustrates the board area taken up by the outline of each kind of package Fujitsu offers, excluding any area around the package necessary for spacing, decoupling capacitors, series damping resistors, or solder pads.

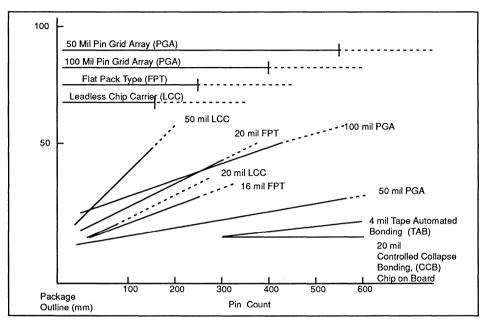


Figure 1. Package Size versus Pin Count

#### 2.1.2 Board Layout

Restrictions in board layout or construction must be identified and resolved early in the design process. For example, a design containing large buses (16 bits or 32 bits or more) must be split up to avoid too high a concentration of simultaneously switching outputs per ground pin. Splitting up the buses, however, may result in variations in signal trace length and require extra care in routing. Similarly, flatpacks, a form of SMDs, are a convenient way to support high pin counts in relatively inexpensive plastic packages. However, with pin pitches as narrow as 15 mils, they demand extremely accurate positioning of solder pads. Dense PGAs, on the other hand, provide a spacious 100-mil pin separation, but because of the number of rows of pins, normally require a large number of board layers.

#### 2.2 Producibility

Though some unusual packages may appear to promise ultra-high speed or dense integration or minimized component/board cost, the designer must always keep manufacturability in mind. The cost of a system is only partially dependent on materials and labor costs per unit; it is also highly dependent on the manufacturing yield of the end product. Therefore, design and production engineers must jointly consider the choice of package in order to guarantee that the chosen package conforms to existing (or purchasable) manufacturing equipment and that the manufacturing process can meet yield goals.

#### 2.3 Speed Requirements

The speed requirements of a system strongly affect package choice. If the interconnect lengths in the system (both inter- and intra-board) can be reduced, system speed may be increased. Reducing interconnect lengths may involve reducing the required number of packages, choosing packages with smaller outlines, changing to double-sided, modular, or piggy-backed mounting, using small form factors, reorganizing boards, and even changing the number of metal routing layers of the board. See Figure 2.

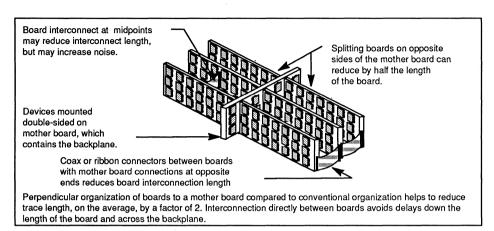


Figure 2. Minimizing Interconnect Length

#### 2.3.1 The Effect of Noise on Speed

There are various sources of noise that can affect an integrated circuit (IC), each with its own effect; all forms of noise influence signal speed, quality, and consequently, system reliability. Certain types of noise arise between a chip I/O and ground or power, while other forms of noise are coupled to the power rails and influence system power and ground lines, propagating noise throughout the entire system. Noise appears to an input buffer (receiver) relative to the receiver's ground. Any noise on this referenced signal is superimposed onto the incoming signal itself, as shown in Figure 3. The  $V_{\rm IH}$  or input threshold level of the receiver indicates when the input will switch, if the signal is stable at that level. Therefore, although the input voltage ordinarily would switch 4 ns after the driver switches, when the signal first crosses the threshold, the designer must assume it will not switch until it is stable; in this case at 8 ns, producing a loss of 4 ns due to noise.

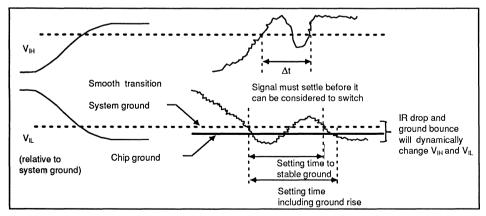


Figure 3. Impact of Noise on Speed

#### 2.3.2 Controlling Noise through Package Selection

Each form of noise is dependent not only on current or its first derivative with respect to time, but also on the real and imaginary components of impedance: resistance (R), inductance (L), and capacitance (C). One solution to noise can be to minimize the package L and R and to locate high drive pins where they will minimize L and R.

#### 2.3.3 The Effect of Thermal Characteristics on Speed

The speed performance of a CMOS or BiCMOS circuit degrades with temperature rise. Therefore, in very high speed systems, it is sometimes necessary to reduce the junction temperature (Tj) or die temperature as a way to improve speed. Certain packages offer better cooling properties than others, making them more suitable for high speed systems. Thermal issues are discussed in Section 5.0.

#### 2.4 Quality

Reliability refers to the defects or failures that appear during the lifetime of a device. Quality, on the other hand, refers to the frequency of occurrence of defects or faults in a device as a result of the manufacturing process. Quality defects are revealed by testing immediately after manufacturing, while reliability defects are revealed by special long-term or intensive test sequences or by time.

#### 2.4.1 How Package Type Affects Quality Testing

Conventional (through-hole) packages lend themselves to simplified testing because it is easy to access the leads in order to force a state (1 or 0) at a node and/or to observe the state of the node. These tests are performed with board-level in-circuit or functional testers. Such tests facilitate the manufacture of high-quality systems by ensuring proper connectivity and function.

Surface mount devices, however, generally provide poor probe access, and are known to occasionally possess faulty joints that make temporary connections during probe. Through-hole packages also have occasional bad solder joints, although their node access is fairly good.

#### 2.4.2 How Device Integration Affects Reliability

Total system reliability is related to the reliability of the individual devices and to their configurations. Systems may be configured as a series in which all devices are interdependent, in which case any one failure will cause overall system failure, or they may be configured in parallel, in which case all devices must fail for the system to fail. Parallel configuration is used in redundant or fault-tolerant systems.

The reliability of a system also depends on the reliability of the devices that comprise the system. The long-term reliability of a single device is defined as an inverse natural log function in a variable lambda, which is the failure rate of the device in the region of lifetime operation characterized by a constant failure rate. In the first hours of a device's life (the infant mortality period), the failure rate declines. The majority of a device's life is characterized by random failures (expressed as lambda), and the end of a device's life exhibits an increasing failure rate. Today's ICs, however, are designed so that we arout does not even begin to occur for at least several hundred years, and can be considered never to occur.

To understand how the partitioning of a system into circuits can affect the reliability of a system, consider a system in which N components are configured in series. Although the density of ASIC devices has increased by two orders of magnitude in the last decade, the reliability of the devices has remained roughly constant. Therefore, it can be assumed that the failure rate of each of the components is constant. The reliability of systems and subsystems in which components are series-dependent is the product of the individual reliability terms for each component. The reliability function of the system just described is therefore:

where

 $R(t)N = e - N\lambda t$ , t is the independent variable time, and  $\lambda$  is lambda, the failure rate.

Since all components have the same failure rate, the reliability function of the system is:

$$R(t)sys = e - N\lambda t$$

Because the number of packages affects the reliability more than the integration factor does, a designer's goal in constructing a reliable system should be to maximize integration and thereby reduce part count.

The disadvantage is that increased integration may in turn increase the package pin count, requiring a more complex package, which usually costs more than a simpler, smaller package. Additionally, the larger die sizes cost slightly more per gate than the smaller ones, although the total non-recurring engineering charges (NRE) would typically be lower.

#### 2.4.3 How Noise Affects Reliability

Even when Schmitt trigger input buffers are used to receive clock signals, noise may go beyond the hysteresis value of the input buffer and cause a counter to be incorrectly clocked or other circuit malfunction. Noise is in this sense a threat to reliability as well as to speed and must be considered in the package choice as well.

#### 2.4.4 How Thermal Issues Affect Reliability

While the junction temperature of a device affects its speed, it also affects reliability expressed as mean time between failures (MTBF) or the mean time a device will operate in a given environment before failure occurs. Figure 6–4 in the previous chapter, Quality and Reliability, illustrates this concept by plotting life test failures as a function of junction temperature. System reliability goals, then, restrict the desired maximum junction temperature in a manner that affects the choice of package according to its thermal characteristics, the chosen type of system thermal management (cooling), and the maximum allowable device power dissipation.

#### 2.4.5 How Package Material Affects Reliability

The different materials used in package construction each have distinct thermal and mechanical properties. The most common materials and their characteristics are listed in Table 2 below.

Package Type	Body Material	Thermal Coefficient of Expansion (ppm/5C)	Thermal Conductivity (W/m * 5C)	Dielectric Constant (K)
Ceramic	Al <sub>2</sub> O <sub>3</sub> (Alumina)	7.0	20	10
Plastic PGAs	Epoxy Fiberglass	14 – 18	0.16	4.5 – 5.0
Other plastic packages (DIP, PLCC, Flatpack)	Polyimide Epoxy	15 – 18	0.38	4.5 – 5.0

Table 2. Package Material Characteristics

To better understand the different characteristics of plastic and ceramic packages, it is helpful to know something about the way they are constructed. Packages provide electrical connection from the IC to the system and isolate the device from destructive elements of the environment. The choice of materials and construction of a package affect its final dimensions, thermal characteristics, and electrical characteristics, as well as device reliability. Fujitsu carefully determines the most appropriate manufacturing methods for a given package and then performs extensive qualification tests to determine its success.

The largest part of the package is the body, which houses the die. The die may be affixed to a lead frame, which physically supports the die and provides the leads that electrically connect the die to the system by means of bonding wires or tab leads. Alternatively, the die may be supported by a cavity on the body of the package or attached to the bottom of the body by a chip carrier.

The die is attached to the surface of the lead frame or to the metallized surface of the cavity or carrier with gold or silver paste, or eutectic. After the die is attached to the lead frame, cavity, or carrier and the bonding pads are bonded to the leads, the assembly is encapsulated. In plastic packages, an epoxy resin is molded around the assembly. In ceramic packages, a cap is sealed onto the lower part of the body or carrier using a frit glass or metal seal (the metal seal has a higher melting temperature than the glass). A solder seal can be used if the cap is metal.

To ensure that the device is completely isolated from its environment, the surface of the die is then coated with glass (SiO<sub>2</sub>) and then polyimide or other coating that prevents gas and moisture from coming in contact with the surface of the die. Figure 4 shows a frontal cross section of the structure of a PLCC package; Figure 5 provides a top view.

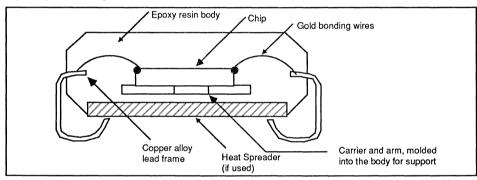


Figure 4. PLCC Package Construction (Front View)

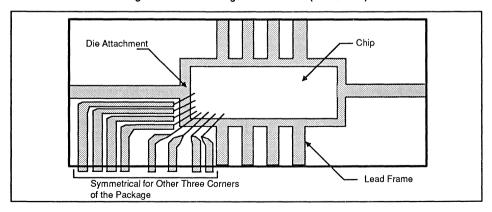


Figure 5. PLCC Lead Frame Construction (Top View)

Each of the various packaging methods has its advantages and disadvantages; for instance each body type and each type of seal has a different maximum case temperature. While plastic packages can tolerate tem-

peratures up to 125°C and high humidity levels with outstanding reliability, ceramic packages are the most reliable for harsh extremes of cold.

Each package type also responds differently to the thermal environment of the board to which the device is attached. Heat can cause thermal stress on the device when different materials expand at different rates, a particularly important factor when surface mount packages are involved.

Different packages also exhibit different electrical characteristics. As the speed and gate densities of CMOS devices rise, the avoidance of electrical parasitics in the form of package delays and noise becomes an increasingly important factor in choosing a package type.

Fujitsu's plastic PGA provides a good example of the tradeoffs involved in package construction. In 1986, Fujitsu introduced the plastic version of its ceramic PGA. The plastic configuration proved to have several advantages over the ceramic version. The body is formed from glass epoxy (VG-10) with an aluminum cap and an epoxy resin sealer. This combination of materials has the same rate of expansion as the PC boards onto which it is mounted; it is also less expensive than ceramic.

Ceramic PGAs have a hermetic seal of solder between the metal lid and the cavity, but plastic PGAs are sealed by filling the cavity with epoxy resin to form an inner seal, then placing a resin sheet over the inner seal to form an outer seal, and then securing an aluminum cap over the outer seal. The aluminum cap provides the necessary rigidity to support the fragile glass epoxy, as well as improving the thermal conductivity of the package.

Connections from the bonding wires to the pins are provided by copper traces designed to minimize mutual and self inductance. Because the plastic PGA is a large package, however, and generally houses a large die, the thermal coefficient of expansion (TCE) difference between the die and the cavity can exert stress on the bonding wires and the die attach. Table 3 lists the package types discussed in this section and the materials used to construct each type.

Table 3. Fujitsu Package Types

Package Type	Lead frame/ Metallization	Lead/Pad	Lead Finish	Cap Material	Body Material	Seal Material
Plastic DIP	le-Ni or Cu Alloy Lead frame	Same	Solder Dipped		Resin	Resin
Ceramic DIP	Tungsten Metallization	Kovar or Fe- Ni	Au/Sn Plated	Metal or Alu- minum	Laminated Alumina	Solder, Glass Frit
CERDIP	Fe-Ni Alloy Lead frame	Fe-Ni	Sn Plated	Alumina	Alumina	Glass Frit
Plastic Flatpack	Fe-Ni Alloy Lead frame	Same	Sn Plated		Resin	Resin
Ceramic Flatpack	Fe-Ni or Kovar Lead frame	Same	Au Plated	Metal or Alu- minum	Laminated Alumina	Solder or Glass Frit
Cerpack	Fe-Ni Alloy Lead frame	Same	Sn Plated and Solder Dipped	Alumina	Alumina	Glass Frit
Plastic PGA	Cu Conductor on Epoxy glass	Kovar	Ni Plated and Solder Dipped	Aluminum	Epoxy Glass	Resin
Ceramic PGA	Tungsten Metallization	Kovar	Au Plated and Solder Dipped	Metal or Alumina	Laminated Alumina	Glass Frit
Plastic LCC	Cu Alloy Lead frame	Same	Solder Plated		Resin	Resin
Ceramic LCC	Tungsten Metallization	Tungsten Metal Pad	Au Plated	Metal or Alu- mina	Laminated Alumina	Solder, Glass Frit

Note: All above packages are hermetic. Alumina is a ceramic. Solder is PbSn. Fe-Ni is ferrous (iron) nickel. Kovar is an alloy of cobalt, iron, and nickel. Bonding wires are gold in the case of molded packages (epoxy resin PLCCs, DIPs, Flatpacks) and gold or aluminum for the other cases. Cerpack is the ceramic flatpack equivalent of CERDIP.

#### 2.4.6 Package Qualification to Ensure Reliability

Fujitsu performs extensive six-month minimum qualification tests for every package-die combination. After such qualification is performed, the package die-combination is added to a package matrix in the Design Manual for the appropriate technology. The designer can be assured that Fujitsu has considered the issues presented here, as well as others, when releasing an approved package-die combination.

#### 3.0 Package Types

Very large scale integration (VLSI) ASIC devices are supported by a wide variety of packages, of both surface mount and through-hole types. Through-hole devices, including DIPs and PGAs, are a proven technology and are supported by widely available production equipment. The pins of these devices are inserted though holes in the PC board to form electrical contact with traces (usually copper) which are embedded in the board or applied to the surface and are routed to drilled pin holes. Solder applied by reflow or wave technique then completes the connection.

#### 3.1 Through-hole Packages

#### 3.1.1 Dual In-line Packages (DIPs)

DIPs have two rows of pins spaced 300 mils to 900 mils apart, with a pin spacing of 70 to 100 mils. Since the length of the package increases as each pair of pins is added, the size of a DIP tends to be unmanageable over 64 pins. The lead width and length of a DIP varies widely, causing variation in the input and output response of the device and thus, skew. Also, due to their high pin inductance, DIPs tend to be noisy, the degree of noise being a function of the location of outputs and sensitive inputs.

The DIP is relatively simple for manufacturing to support, thanks to a large installed base of well-proven equipment and is one of the least expensive packages available. Furthermore, DIPs, being well established, come in many JEDEC-approved options (see JEDEC Standard 95), and are available in both ceramic and plastic cases.

#### 3.1.2 Pin Grid Arrays (PGAs)

Although PGAs are usually through-hole (Fujitsu also offers SMD versions), they differ from DIPs in that pins are arranged in rows on all four sides. While the pin spacing is usually the same as for DIPs (70 to 100 mils), nesting the pins in rows permits a larger number of pins to be contained within a smaller area allowing PGAs to support high pin counts of more than 300 pins. See Table 4 for a list of Fujitsu PGAs.

Table 4. PGAs Available from Fujitsu

Package	Туре	Construction	Number of Pins
PGA – 64C, 64P	Through-hole	Ceramic/Plastic	64
PGA - 88C, 88P	Through-hole	Ceramic/Plastic	88
PGA - 135C, 135P	Through-hole	Ceramic/Plastic	135
PGA - 179C, 179P	Through-hole	Ceramic/Plastic	179
PGA - 208C	Through-hole	Ceramic	208
PGA - 256C	Through-hole	Ceramic	256
PGA - 256C	Surface	Ceramic	256
PGA - 299C	Through-hole	Ceramic	299
PGA - 321C	Staggered	Ceramic	321
PGA - 361C	Staggered	Ceramic	361
PGA - 401C	Staggered	Ceramic	401

Through-hole = 100 mil through-hole Surface = 50 mil surface mount PGA Staggered = 71 mil staggered PGA Although PGAs are generally easy to support from a manufacturing standpoint, they may also raise problems. The PC board designer may find it difficult to route signals to and from the inner rows of the PGA, since it has only 100 mils spacing between pins. Additionally, the large cluster of pins confined to a small area tends to create trace congestion and may require boards of up to six layers to be used to support the PGAs. Manufacturing engineers find the solder joints for the pins of inner rows are difficult to inspect, forcing them to rely on the results of "bed-of-nails" in-circuit testers, or sophisticated inspection techniques such as x-ray or infrared.

Although more expensive than DIPs, PGAs have come down in cost with the introduction of plastic PGAs (previous PGAs were usually ceramic). These plastic PGAs are generally constructed of G-10 glass-type epoxy with the traces routed through the epoxy the way they are routed on a typical PC board. (The electrical characteristics are, of course, tightly controlled). Although the reliability of plastic PGAs was initially in question, Fujitsu built them using special construction techniques employing metal lids and heat spreaders to provide rigidity and heat dissipation. Their excellent reliability history up to this point seems to indicate that plastic PGAs will continue to be popular. The widely-used epoxy thick-film substrate, once a quality and reliability concern, has the same TCE as the most common PC boards, and reduces the stress of expansion and contraction that is typically a concern with larger packages. (The distance of expansion per unit change in temperature increases with the size of the package.)

#### 3.1.3 Advances in Through-hole Packaging at Fujitsu

The demand for high pin-count plastic packages cannot be satisfied by merely increasing the number of pins a package supports. As size increases, so do the problems inherent in these lower-cost packages. These problems include greater lead inductance and thermal expansion mismatch between die and package. Ceramic flatpacks can support more pins than plastic packages, but they require special manufacturing capabilities, and are difficult to work with since they may have pin pitches down to 10 mils. Surface mount PGAs (discussed in Section 3.2) can support a large number of pins, but require difficult manufacturing processes.

Fujitsu's answer to these problems, for the customer who wants high levels of integration without the need for exotic manufacturing methods, is the staggered PGA, shown in Figure 6.

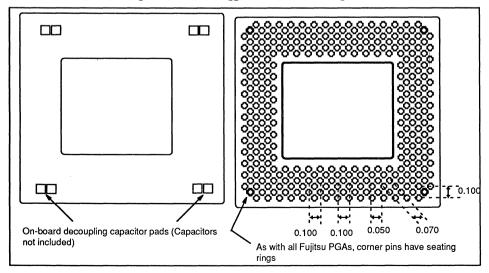


Figure 6. 321-Pin Ceramic Pin Grid Array

Figure 7 illustrates the footprint of the staggered PGA and the method for routing traces through the leads. Note that the routing is oblique, with the traces offset 45 degrees compared to traditional routing. At this angle, the lead spacing is 71 mils, providing the trace density available with standard through-hole devices, while reducing the package outline by approximately 40 percent.

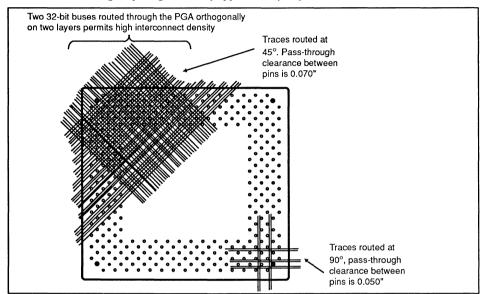


Figure 7. Staggered Pin Grid Array Routing

The lead configuration of a package affects the pin assignment of the ASIC device. For example, Figure 7 shows a situation in which a 32-bit address bus and a 32-bit data bus are routed through the device, with one offset 90 degrees from the other. If you assign consecutive bit significance to the bus, you will notice that the resulting pinout is quite different from an equivalent circuit packaged in a traditional orthogonal PGA. High drive buses can still be distributed around the ground pins, but the associated pads are not concentrated in one specific area of the die, reducing the concentration of SSOs, thereby reducing signal noise.

#### 3.2 Surface Mount Devices (SMDs)

The demands of military applications, space-constrained systems, and boards containing large numbers of memory devices were initially responsible for the development of surface mount technology (SMT). However, the accelerated push for physically reduced systems, the appearance of higher pin count ASICs, and the cost of pin grid arrays have encouraged many more designers to consider surface mount options. Easing the strain of the migration to SMT is the broader availability of pick and place, vapor phase soldering, and other necessary SMT equipment, as well as the availability of SMDs for an increasing percentage of devices on the boards. SMT for VLSI is gaining momentum due to the smaller board area consumption, smaller profile, and proven reliability.

#### 3.2.1 Flatpacks

Plastic flatpacks have been popular for years with manufacturers of peripherals in which the board area is constrained and height is restricted. And recently, the low cost of flatpacks (in plastic) has made them an attractive alternate to PGAs and even to DIPs in cases of higher pin count. As the following figures show,

flatpacks come in several lead type and location configurations. Figure 8a illustrates a small outline integrated circuit (SOIC), with gullwing leads on two sides, Figure 8b illustrates a quad flatpack (QFPT) with gullwing leads on four sides. Flatpacks with axial leads require special assembly, and are generally used only for ECL circuits in which leads may have to be trimmed and formed to tune impedance.

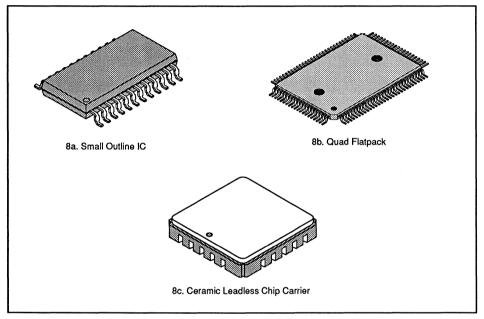


Figure 8. Flatpack Configurations

Because flatpacks feature pin pitches (pin spacing from center to center) down to 10 mils, they can support high pin counts within a small board area. However, the narrow pin spacing means that accuracy in device placement, pad size and placement, and solder paste application tolerance are all more critical. PC board designers also need to determine whether the true package dimensions are in metric or English dimensions, and, when converting between the systems of measure, ensure that enough precision is maintained so that pins on the end of large packages won't roll off due to inaccuracies in pad location.

Probing devices with fine pin pitches can be difficult because the pins do not pierce the bottom of the board, and if probes are <u>attached</u> to the leads, they can easily slip off and short adjacent leads.

# 3.2.2 Leadless Chip Carriers (LCCs)

Ceramic leadless chip carriers (CLCCs), such as the example shown in Figure 8c, have a long history in surface mount packaging. Ceramic packages perform well in high temperature environments, explaining their popularity in military applications. The term "chip carrier" comes from the process of mounting the die directly to a thick-film chip carrier, which also has pads for external connection on the opposite side of the substrate. This configuration differs from that of the PGA, in which the die is housed in the cavity of the package, or the flatpack, in which the die is held by the lead frame and molded with the package. CLCCs are available in pad counts ranging from 28 to 84 and beyond.

Pads, not leads, are located on the bottom of the carrier and are generally spaced at a 40-mil pitch (standard). Solder paste is applied to the pads on the board to which the device will be mounted, usually by screen printing, and the board is then vapor phase or infrared reflow soldered. Because the pads are lo-

cated beneath the package, they are typically very difficult to probe and are subject to manufacturing defects such as solder voiding (gas bubbles in solder formed during reflow).

The most challenging problem inherent to LCC devices relates to TCE mismatch between the chip carrier and the board to which it is mounted. As the temperature of boards and packages rises, the materials expand at different rates. This difference translates to mechanical shear force at the solder joint. This force temporarily deforms the leads of PLCCs and flatpacks, but CLCCs have no leads. Consequently, the force is directed at the solder joint, tending to promote thermal fractures, (shown in Figure 9).

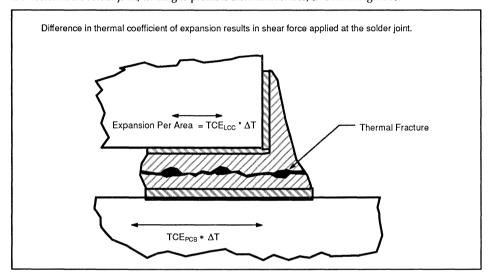


Figure 9. Defect Caused by Difference in Thermal Coefficient of Expansion

Even though CLCC SMDs cost more than equivalent plastic packages, their resistance to high temperatures, availability in hermetically sealed (moisture resistant) packages, and low profile of the CLCC SMDs make them very useful for applications in extreme environments. The TCE mismatch problem affecting LCCs is less severe when they are mounted to ceramic hybrids or PC boards, making their disadvantages acceptable in many circumstances.

# 3.2.3 Plastic J-leaded Chip Carriers (PLCCs)

If cost and TCE mismatch are a significant deterrent to the use of LCCs, leaded chip carriers may be more attractive. Though the chip is still mounted on a carrier (see Figure 10), the electrical connections of PLCCs are through pins that deform to absorb the TCE-induced thermal stress. Furthermore, while solvents used in the post-soldering cleaning process may be retained beneath the low profile of the CLCC and flatpack, the board offset of the PLCC permits it to remain free of these contaminants. In addition, the LCC in a plastic package costs less than the equivalent CLCC.

When more pins are necessary (in the 44-, 68-, 84-pin packages necessary for ASICs), the LCC is called a PLCC. It is also available in a ceramic body version; both are available in pin counts of 28 to 84 and beyond.

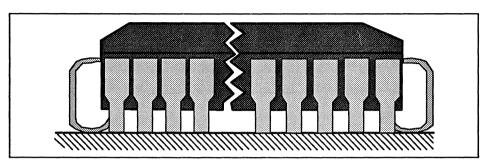


Figure 10. PLCC Package

This package is termed a small outline J-lead (SOJ) when its bent leads are located on only two sides (Figure 11). The leads are bent into the form of a J in order to permit it to be placed on top of the solder pad.

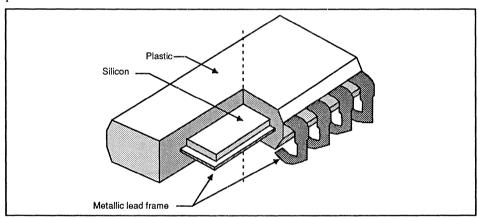


Figure 11. Cross-Section of a Plastic Small-Outline J-lead Package

On the list of drawbacks of the PLCC is its limited ability to withstand high case temperatures, and its unavailability as a hermetic package. It is nevertheless very well suited for industrial and commercial environments. With a 50-mil pin pitch and only slightly greater height and width, the profile of the PLCC is nearly equivalent to the corresponding CLCC.

#### 3.2.4 Advances in Surface Mounted Packages

While smaller process geometries themselves have few disadvantages, the associated increase in integration, speed, power, and particularly pin count place heavy burdens on packaging. The greatest challenges CMOS faces is supporting pin counts in excess of 300 in packages with low lead inductance, capacitance, and resistance.

To respond to these demands, Fujitsu has developed a clever solution in packaging to obtain the highest average pin density per board area yet achieved. This is accomplished with surface mount PGAs, which rely on narrow pin pitch (50 and even 25 mils) in a dense grid of multiple rows of pins. Since through-hole packages cannot effectively support pin pitches narrower than 70 mils, these PGAs must be surface mounted, though they still possess pins (see Figure 12).

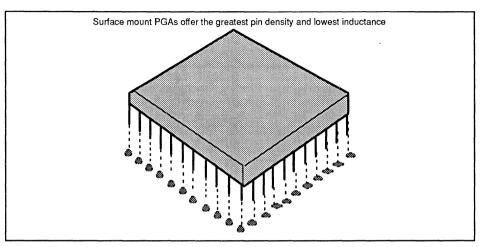


Figure 12. Surface Mount PGA

The surface mount technology also permits traces to run beneath the package leads, increasing available trace density. Figure 13 shows the solder pad design required by these high-pin-density packages.

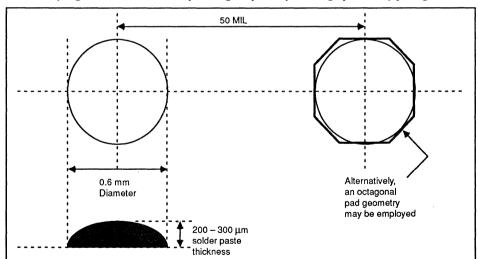


Figure 13. Solder Pad Design for Surface Mount Pin Grid Arrays

Table 5 provides an item-by-item comparison between PGAs, surface mount PGAs, and flatpacks of similar pin counts.

PACKAGE	TYPE	PIN PITCH	OUTLINE (MAX)	PIN DENSITY (Pins Per Sq Inch)
FPT - 160	Surface	25 mil	1.276" x 1.276" (1.63 sq ln)	98
PGA – 256	Through	100 mil	2" x 2" (4 sq ln)	64
PGA – 256	Surface	50 mil	1" x 1" (1 sq ln)	256
PGA – 321	Staggered	71 mil	1.72" x 1.72" (2.96 sq ln)	109
PGA – 401	Staggered	71 mil	1.922" x 1.922" (3.69 sq ln)	109

**Table 5. Comparison of Critical Features** 

The numerous electrical and mechanical advantages of surface-mount PGAs would seem to outweigh their disadvantages. However, the general state of high volume manufacturing has not kept pace with the rapid advances in semiconductor packaging. This is partly due to the requirement for state-of-the-art manufacturing equipment, which is quite expensive, and also to the need to maintain board yields with such complex devices. Therefore, in order to establish these packages as an attractive alternative, Fujitsu personnel are available to assist customers in the mounting and inspecting of these highly complex packages.

# 3.3 A Comparison of Through-hole and Surface Mount Devices

SMDs provide improved electrical performance and reduced system size and costs. Furthermore, with plastic flatpacks of up to 160 pins and beyond available, SMDs show promise in supporting the rapidly advancing gate size complexities and high pin count of today's ASIC products at a substantially lower cost than the large ceramic PGAs. However, as the manufacturing complexities that have just been reviewed indicate, surface mounting large ASIC devices may be difficult and risky, and the designer should be cautious in their use.

If board space constraints are not critical, if the economic impact of scaling down the end system is not great, if optimal electrical characteristics in packaging are not a critical concern, then through-hole packaging may be the best solution. On the other hand, if speed and integration requirements dictate the use of very dense gate arrays, PGAs or SMT PGAs provide both through-hole and surface mount alternatives.

#### 3.3.1 Socketing Surface Mount Devices

Some benefits of SMDs are available to manufacturers employing through-hole packages through the use of sockets for SMDs. Sockets are available for QFPTs, small outline packages (SOPs), CLCCs and PLCCs; however, the use of QFPT and SOP sockets is normally restricted to prototyping and burn-in, while low-cost, reliable production sockets are more commonly available for PLCCs and CLCCs. These production sockets house the SMD (they are tightly tailored to the specific package) in one of two ways. Flatpacks and LCCs use low/zero insertion force with a lid that closes down on the package. PLCCs use pressured socket contacts that drive a pin into the underside of the socket. Socket pins are arranged like those of PGAs: they are through-hole, they have 100-mil spacing (generally), and they are most commonly oriented in a grid of two rows.

One advantage of these sockets is that in applications where through-hole packaging is required and the choice of through-hole packages is limited to PGAs, a plastic SM package plus the production socket will cost less than the through-hole PGA. The scenario typically occurs when the required number of pins is between 40 and 84 for PLCCs and LCCs and up to 160 or more for the flatpacks.

Another significant reason to socket SMDs results from the manufacturing difficulties of SMDs that were presented earlier. ASIC devices are usually among the largest in the system, and the most vital and expensive. For the purpose of field maintenance, many companies feel it is more economical and reliable not to risk running an ASIC device through wave or reflow solder and risking stress fractures or other damage. Furthermore, the test probing difficulties alluded to earlier are alleviated with sockets, which usually provide easy access to the contacts. Often, once reliability of the system is proven, the boards are re-laid out with surface mount devices. Therefore, simply because a manufacturing facility isn't geared up for SMT does not mean that SMT devices cannot be used there.

#### 3.3.2 Noise Problems With Sockets

Sockets for SMDs are convenient for manufacturers not yet ready to go to SMT, or for initial prototyping where the device may frequently be removed. Socketing permits the user to gain many of the benefits of SMDs, such as reduced profile and support of high pin counts in plastic, while avoiding the drawbacks, such as special manufacturing equipment and lead probing difficulties. Unfortunately a major electrical advantage of SMDs, low pin inductance, is compromised when sockets are used. The primary result is greatly increased noise, which adversely affects overall speed and signal quality. In fact, a socketed SMD generally has a higher lead inductance than an equivalent through-hole PGA.

#### 3.4 Summary of the Packaging Alternatives

Having reviewed the package selection alternatives presented in Section 2.0 and the various tradeoffs between the packages discussed in this section and summarized in Table 6 below, the designer can weigh the benefits and limitations of the various packages and arrive at an optimal packaging scheme.

Table 6. ASIC CMOS Package Types and their Characteristics

Package Type		f Physical Insions	Electrical Characteristics <sup>1</sup>	Thermal Characteristics (°C/Watt)	Usable Gates³	Relative Cost (per Pin)
Through- Hole DIP	# Pins: Pin Pitch: Body Length: Body Width:	16 to 64 100 mils .75" to 2.3" .300" to .700"	R: Medium L: High C: Low	Ceramic/Plastic θJA <sup>2</sup> : 70 - 40/ 120 - 80	Up to 17K gates	1
Surface Mount SOIC	# Pins: Pin Pitch: Body Length: Body Width:	16 to 28 10 mils 50 to 70 mils .300" to .400"	R: Medium L: Medium C: Low	Ceramic/Plastic θJA <sup>2</sup> : 110 - 80/ 130 - 105	Up to 6500 gates	1
Surface Mount QFPT	# Pins: Pin Pitch: Body Width:	48 to 260 10 mils .65" to 1.7"	R: Medium L: Medium C: Low	Plastic θJA <sup>2</sup> : 95 - 60	Up to 17K gates	1
				Ceramic		
Surface Mount CLCC	# Pins: Pin Pitch: Body Width:	28 to 84 40 to 50 mils .45" to .97"	R: Medium L: Medium C: Medium	θJA²: 70 -45	Up to 25K gates	5
				Plastic		
Surface Mount PLCC	# Pins: Pin Pitch: Body Width:	28 to 84 50 mils .49" to 1.19"	R: Medium L: Medium C: Low	θJA²: 65 - 50	Up to 17K gates	1.05
			Ceramic/Plastic	Ceramic/Plastic		Ceramic/Plastic
Through- Hole PGA	# Pins: Pin Pitch: Body Width:	64 to 299 .100 mils, 70 mils 1.033" to 1.7"	R: Low/Low L: Low/Low C: High/Low	θJA <sup>2</sup> 40 - 19/ 46 - 38	Up to 75K gates	11/ 3.5-5

 ${}^{1}R$  = Resistance, L = Inductance, C = Capacitance  ${}^{2}Assuming$  Static Airflow

<sup>3</sup>Assuming 1.5µ CMOS Technology

#### 4.0 Electrical Considerations for the Assignment of Signal, Power, and Ground Pins

Driven by the continual demand for high speed systems, CMOS ASICs that exhibit output drive levels, rise and fall times, and propagation delays comparable to yesterday's ECL circuits are now being developed. Consequently, the problems intrinsic to ECL design (even thermal management) are now appearing in CMOS designs. These problems, based on noise and its effect on the device, are introduced in this section and possible solutions are discussed.

#### 4.1 Sources and Magnitude of Noise

CMOS circuits operate by charging and discharging node capacitances through pull-up or pull-down transistor networks constructed of P channel and N channel enhancement mode (normally off) MOSFET transistors. As a result, these circuits generate noise when switching. The following review of basic CMOS circuits and how they work explains this phenomenon in greater depth.

# 4.1.1 Basic CMOS Circuits

Figure 14 shows a CMOS totem pole output buffer, the typical implementation for CMOS circuits, while Figure 15 illustrates a CMOS-compatible input buffer, and Figure 16 depicts a CMOS input buffer configured to be TTL compatible.

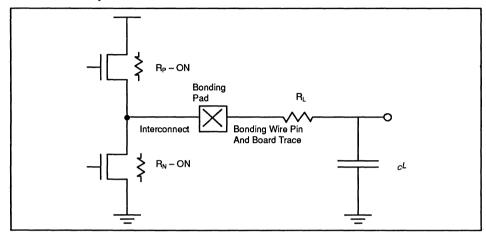


Figure 14. CMOS Output Buffer Model (Totem Pole)

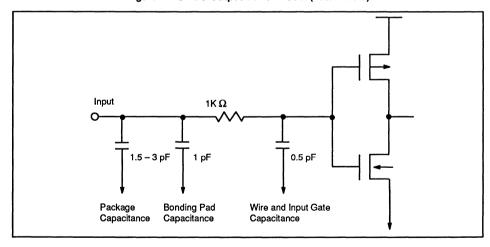


Figure 15. I/O Model, CMOS Input

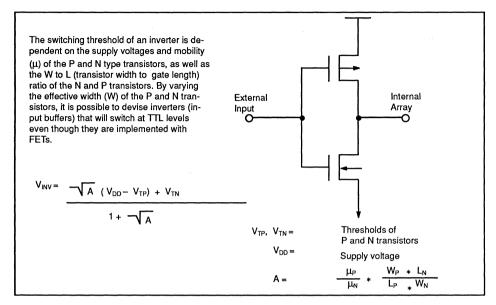


Figure 16. I/O Model, TTL Input

Internal CMOS circuits, such as the NAND gate shown in Figure 17 are typical of CMOS logic designs, which can be represented as a pull-up network and a pull-down network, each with its own logic and analog characteristics.

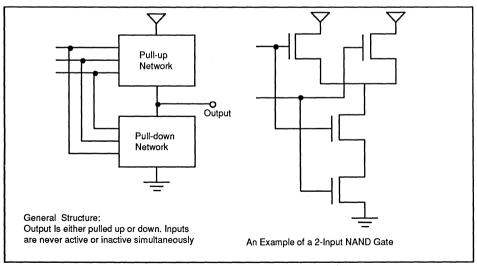


Figure 17. CMOS Basic Gate Structure: The Pull-up/Pull-down Network

The other type of element used in CMOS circuits is the transmission gate, or T-gate, which is useful for the efficient construction of multiplexers and sequential circuits (D-flops, latches, etc.) as shown in Figure 18.

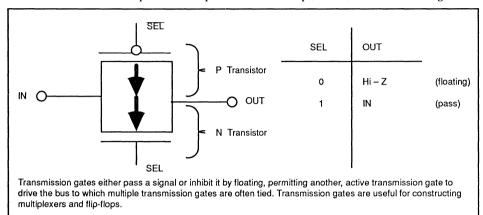


Figure 18. CMOS Basic Gate Structure: The Transmission Gate

#### 4.1.2 Output Switching Noise and Simultaneous Switching Outputs (SSOs)

The greatest source of noise in a CMOS circuit is the result of an output switching either high to low or low to high, particularly into or out of a high capacitive load. CMOS outputs drive two types of loads, either CMOS loads, which are high in capacitance but low in leakage current, or TTL loads, which are lower in capacitance but higher in leakage current. Therefore, the AC and DC currents that the buffers see when they switch depend greatly on the type of driven load and its capacitance. When this load discharges through the N-type transistor of the totem pole output, as illustrated in Figure 14, the effect is that of a capacitor discharging through resistance. Consequently, the initial current is high and decreases over time as the output node capacitance becomes charged. Similar currents may be observed when charging the node capacitance, as in the case of a low-to-high transition.

Figure 19 shows the characteristic resistance and capacitance of various parts of the output of an ASIC device.

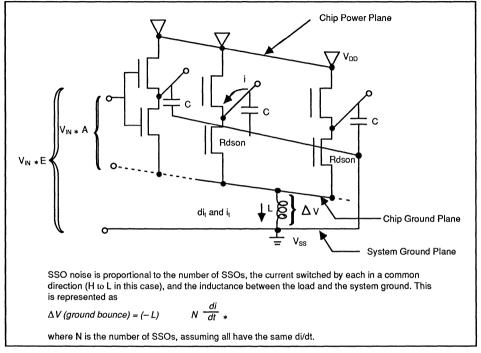


Figure 19. Electrical Model of Simultaneously Switching Outputs

Although small, the total inductance becomes a critical factor when discharging or charging output capacitance, since the instantaneous current (*i*) is high. Recall that the self-induced voltage in an inductance, (*L*) is expressed by

$$\Delta_{VINDUCED} = \frac{L * di}{dt}$$

where t is time and d is rate of change.

In a high-drive CMOS device driving high loads, such as 200 pF, through a voltage swing approaching 5 volts with a rise/fall time of < 2 ns, the instantaneous current may be

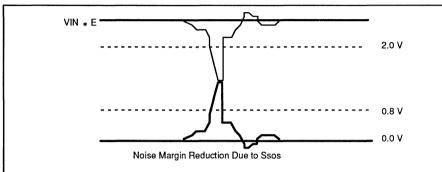
$$i = C + \frac{dv}{dt} \approx C + \frac{\Delta v}{\Delta t}$$
 (average over rise and fall time)

This induced voltage appears as noise on the receiving end of the signal as referenced to the ground. The current on a high-to-low transition is sunk into ground, causing the current to "bounce" or rise relative to other signals referenced to it. This ground bounce phenomenon may also apply to power on low-to-high transitions, yielding a similar noise problem.

Noise on signals may cause false triggering on the input buffer(s) being driven, or at least create a window of ambiguity in the time at which the driven input should switch (see Figure 20). Therefore, noise may result in degradation in speed resulting from adding settling time to a delay and may even result in

functional effects if false triggering occurs. Furthermore, if N multiple outputs under this condition switch simultaneously, the induced voltage is increased as a multiple of the number of outputs

$$nV = N \star L \star \frac{di}{dt}$$



- In this example, outputs switching H to L result in a ground bounce or rise in the chip ground relative to system ground.
- The rise appears as if the input signal voltage levels are reduced proportionally. If the bounce is too
  great, the input voltage is below V<sub>IH</sub> causing false triggering.
- In the L to H case, it is the low input levels (V<sub>II</sub>) that are affected.

Figure 20. Effect of SSO Noise on Thresholds

Not only inductance but also characteristic resistance can create noise problems. The following paragraphs summarize the types of noise that exist in CMOS systems and explain how packaging impacts this noise.

#### 4.1.3 Self-Induced Noise

Self-induced noise results when high-speed, high-drive outputs switch and introduce a spike on the signal relative to ground. The SSO effect, discussed previously, is an example of the level of self-induced noise that can occur. It is predicted by

$$\Delta V_{SI} = L \quad \frac{\Delta i}{\Delta t}$$

where L is the inductance between the pin and ground as well as the trace inductance.  $\Delta i$  is the instantaneous current and  $\Delta t$  is the fall/rise time.

#### 4.1.4 Mutually Induced Noise

Mutually induced noise (a form of crosstalk) occurs when a signal trace that has been running parallel to another for some distance switches, inducing a voltage into the adjacent wire. Since both inductive and capacitive coupling occur only during signal transition and propagation, the effect is additive, as the signal propagates down the trace. Resultant noise propagates in both the forward and backward directions down the line. The forward crosstalk has a pulse duration equal to the rise and fall of the signal, with an amplitude equal to the difference between the capacitive and inductive coupling. Backward crosstalk has a pulse duration equal to the transition time down the trace and an amplitude dependent on the sum of the inductive and capacitive coupling as well as the trace length.

# 4.1.5 Capacitive Coupled Noise

Another form of crosstalk resulting from mutual signal coupling, this noise occurs in proportion to the dielectric constant of the board, the distance of trace separation, and the trace length and width. Acting as two thin parallel plates, these traces couple switching current as integrated over time.

#### 4.1.6 Ringing on Signals

From basic circuit theory, the designer will recall that if the signal line impedance does not match the output impedance of the buffer, then the signal is not naturally dampened. If the impedance of the load is less than that of the buffer, the signal is over-damped and will have a slow rise/fall time. However, if the buffer possesses lower impedance, then the signal is under-damped and may ring, as illustrated by Figure 3. Typically, signal line impedances are in the range of 50 to 250  $\Omega$ , while in the past buffers possessed "on" resistances of 500  $\Omega$  to 2 K $\Omega$ . However, due to the need for higher current sourcing/sinking and faster switching speeds, "on" resistances of output buffers have come down to the 10- to 50-  $\Omega$  range, requiring the use of special termination techniques, discussed in the Fujitsu Application Note "Interfacing CMOS and BiCMOS VLSIs."

#### 4.1.7 iR Drop

Up to this point, the sources of noise discussed have depended on inductance or capacitance. Since the DC current that a ground pin may sink, or that a power supply pin may source can be significant, the familiar voltage drop across a resistor, as current passes through it, is also a source of noise. This iR drop is the phenomenon that limits the sum of source and sink currents through power and ground pins respectively. Ohm's Law describes the effect of this noise source in the following equation defining voltage rise or drop due to iR effects:

$$\Delta V = R \quad * \quad \sum_{n=0}^{N-1} i_n$$

where

R is the output pin-to-ground (sink) resistance, or power pin return-loop (source) resistance (including the "on" resistance of the respective N or P channel device) and

 $i_n$  is the current through the nth output pin connected to this common ground or power pin.

#### 4.1.8 Current Spiking or "Crowbar Noise"

As Figure 14 illustrated, a CMOS output buffer is constructed as a totem pole in which the output is taken from the common source (P type) and drain (N type) with the drain of the P type connected to power and the source of the N type connected to ground. When the input to the totem pole (the P and N gates) switches, the Miller capacitance of the gate causes the gates to charge or discharge at some specified time constant. It is possible that both transistors can be on, one in saturation and the other passing through the linear region, creating a current path between power and ground that can damage the device. This is less a concern for internal transistors than it is for the "beefy" transistors at the I/O. This current spiking can not only introduce noise on the power and ground planes, but may damage the device as well. For this reason, Fujitsu has taken precautions in the design of the CMOS output buffers to prevent this problem from occurring.

# 4.2 Recommended Strategy for Pin Assignment

The assignment of Clock, Scan, and other signals, as well as power and ground, to specific pins on the package affects electrical behavior (speed, noise, reliability, etc.), board manufacturing requirements, and device reliability. Therefore, optimal pin assignment strategies should consider the variables over which the user has control (placement of non-scan inputs, outputs and bi-directionals) and the variables over

which the vendor has control (power, ground and scan signal placement). Out of these relationships a method of placement can be developed, using the following approach:

- (a) Prioritize the signals whose placement is most critical.
- (b) Establish guidelines for the location of these signals, both in absolute position and relative to other signals.

#### 4.2.1 Prioritization of Signals for Placement

Noise minimization is used to establish signal prioritization. All of the various forms of noise discussed in the last section are dependent on either i or di/dt, and L, M, R, or C. The signals affect i and di/dt, while the package pin location affects L, R and C. Figure 21 provides an illustration of how electrical characteristics vary by pin position.

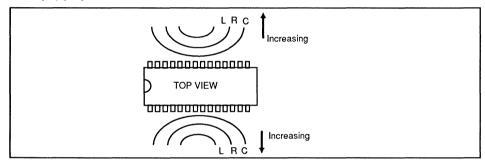


Figure 21. Variation in Inductance, Resistance, and Capacitance as a Function of Pin Position

In general, the further a pin's external contact is from the die connection, the greater its resistance, impedance, and capacitance. Therefore, signal prioritization is established according to current or its time derivative, while location is guided by package pin characteristics. Input signals are classified by their noise sensitivity. If a spike on an input could be disastrous (as with a clock), that signal should be carefully located. Table 7 classifies signal type by electrical characteristics.

Signal Type	Current Characteristics (General)
Ground	Highest i, DC, and di/dt
Power	High i, DC, and di/dt
High drive outputs	High di/dt
Clocks	Highest noise sensitivity
Low drive outputs	
Other Signals	

Table 7. Electrical Characteristics of Each Signal Type

# 4.2.2 Characteristics of Package Pins by Location

The inductance, capacitance, and resistance, all of which are critical to minimizing noise, are related not only to board construction, but also to the pin position on given packages, and the circuit to which the pins are bonded. The pin, lead frame, bonding wires, pads, and buffers (input, output or bi-directional) all influence the characteristic L, R, and C of the line. See Figure 22.

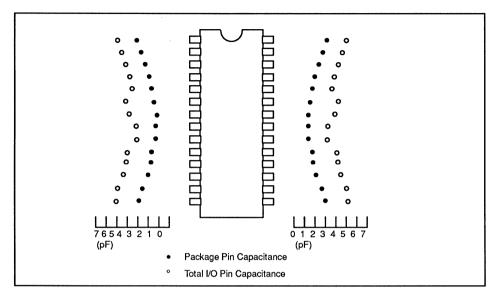


Figure 22. Measured Pin Capacitance by Package Position

#### 4.2.3 Relating Signal Type to Pin Location

Since power and ground pins demand a large DC current (i), iR drops are of great concern. Therefore, Fujitsu assigns power and ground to pins with minimum resistance (and inductance). High-drive outputs exhibit a large di/dt, resulting from high capacitive loading, so the best pins for these signals are those of minimum inductance. Furthermore, adjacent pins possess the greatest M, and thus couple the most M di/dt noise. This means that noise-sensitive inputs, such as clock inputs, should be isolated from pins that handle high di/dt, such as high-drive outputs.

#### 4.2.4 Minimizing iR Drops on Power and Ground Pins

Placement of ground pins is critical because noise on ground affects the voltage level of all signals referenced to it. For this reason, Fujitsu has preassigned power ( $V_{DD}$ ) and ground ( $V_{SS}$ ) signals for all packages in a given gate array family according to the electrically optimal locations. Preassigning power pins permits Fujitsu to develop load boards (which interface the packaged device to the tester) advanced enough to carry out high-speed functional testing of devices with high I/O count and to drive devices with relatively low noise. Fujitsu also took into consideration manufacturing issues such as adjacent pin shorting due to probes and package rotation. The predefined power and ground assignments for Fujitsu devices are found in the Package Pin Assignment Guide in the Design Manual for the appropriate gate array family, and are used in conjunction with the Package Matrix to determine pin assignment.

#### 4.2.5 Minimizing the Self-Inductance of a Signal

Fujitsu believes that an ASIC designer concerned about designing a mini-computer, PC, mainframe or other complex system should not have to be concerned with determining specific on-chip noise issues, particularly since board-level noise issues are demanding enough. Therefore, Fujitsu developed a straightforward grouping scheme for the placement of various types of signals relative to their distance from the nearest power and ground pins. As Figure 23 shows, the self-inductance associated with a given signal is

a function of the length of wire between it and its nearest ground (for a falling transition) or power (for a rising transition).

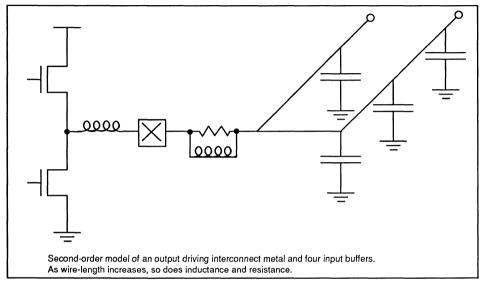


Figure 23. Self-inductance in a Circuit

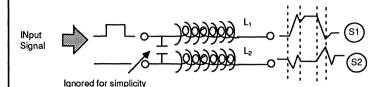
Since di/dt can vary greatly for outputs within a group, there are some general restrictions relating to SSOs and their total current to the number of grounds on the chip. This is done by summing representative values like those shown in Table 5–4 in Chapter 4, which are weighed depending on the IOL of the given output buffer. Notice that, if the output buffer employs noise limiting circuitry (edge rate grading) then di/dt is less and the representative value is also less, meaning more of these outputs can be supported per ground pin.

In summary, to ensure that the iR drops and the ground bounce effect (L di/dt) are within reasonable limitations, Fujitsu has established guidelines for determining the number of necessary grounds and defining the pinout.

#### 4.2.6 Placement of Clock and Asynchronous Clear/Preset Signals

In addition to causing the ground bounce and iR drops that can deteriorate an output signal's quality and alter the ground reference, output switching can also couple noise into adjacent sensitive inputs by mutual inductance, as shown in Figure 24. For that reason, the designer should ensure that clocks and asynchronous clear and preset signals are not placed near outputs, particularly high drive outputs. To further isolate inputs from noise, the designer should minimize the inductance (length) of the return loop from the input buffer to ground by placing this type of input near a ground pin. The mutual inductance of the input buffer itself can be minimized if it, and any outputs nearby, are not assigned to high inductance pins. As discussed in Section 4.2.1, the center pins of a DIP, flatpack, or PLCC possess the lowest L and R, as do the inner rows of PGAs, making them most suitable for  $V_{\rm DD}$ ,  $V_{\rm SS}$  and high drive outputs. But the edges of the package, while suitable for data signals, should be avoided when placing clock and other sensitive signals, as they exhibit a high mutual inductance and large iR drop.





Noise is introduced on the adjacent lead S2 as S1 is driven in a manner described by Faraday as

$$V_S = -M \frac{di}{dt} \frac{S1}{dt}$$

where M is the mutual inductance between the adjacent leads.

If S2 is also being driven, then the mutually induced noise is superimposed on the self induced noise already present, as described by

$$V_{S2} = -M \frac{di}{dt} + L_2 \frac{di}{dt} + S2$$

Figure 24. Causes of Crosstalk

## 4.3 Summary: Choosing the Package and Assigning the Pins

This discussion of noise as related to packaging and its effect on pinout should help the designer appreciate the care Fujitsu has taken to ensure that noise margins within the device are restricted to maximize system reliability. It should also provide the designer with a basis for establishing optimum pin assignments. A step-by-step procedure for choosing an optimal package and assigning pins to it follows.

#### 4.4 Package Selection Checklist

When selecting a package for an ASIC device, the designer should consider the following points:

- Define a subset of the Fujitsu packages that can be supported by your company's manufacturing capabilities.
- b. Estimate, as closely as possible, the gate and I/O counts of the circuit(s) to be packaged.
- c. Determine the number of power and ground pins required by considering the following:
  - Representative value limitations for SSOs
  - 2. Limitation of the sum of the sink current (I<sub>OL</sub>) per ground pin
  - Limitation of instantaneous current per ground pin to satisfy metal migration restrictions
- d. Using the package and pin assignment section of the Design Manual, determine the packages that satisfy the signal, power, and ground pin requirements of the circuit.
- e. Make sure that the electrical, mechanical, and thermal properties of the chosen packages are suitable for the application.
- f. Check the mechanical dimensions in Fujitsu's ASIC Package Catalog and the power and ground pin assignment tables and grouping charts in the appropriate package and pin assignment tables for the chosen technology. Please contact Fujitsu regarding pricing trade-offs when evaluating packages or partitioning the system.

#### 4.5 Pin Assignment Checklist

- a. Follow Fujitsu's pin assignments in the Package and Pin Assignment section of the Design Manuals. Although multiple pinouts of the same package may be offered in some cases, all power and ground signals indicated on the chosen package must be connected on the board.
- b. Assign input pins (in excess of 5 MHz) and high power output buffers ( $I_{OL} = 24$  mA) according to the appropriate pin assignment table.
- c. Place all high-drive (power and high power) outputs near ground pins; the higher the drive, the closer they should be placed. SSOs should be placed particularly close to ground pins.
- d. Place SSOs in groups belonging to given ground pins.
- e. Distance noise-sensitive signals such as clock and asynchronous clear and preset signals away from SSOs and high-drive outputs. Also, assign them to pins with low inductance and resistance, preferably near a ground, if one is available away from SSOs or high-drive outputs.
- f. Place SSOs on low inductance pins, such as those located on the inner rows and middle position of the PGAs.

These guidelines assist the designer in choosing the best package for the application, resulting in a device with reliable and predictable electrical performance and without harmful DC and AC effects on the system. There are other system interface issues such as device decoupling and termination that should be considered during design. These are discussed in Fujitsu's application note, "Interfacing CMOS and BiCMOS VLSIs."

#### 5.0 Thermal Issues in CMOS ASIC Packaging

CMOS has traditionally been associated with low power, one of the classic advantages it has over ECL. While ECL continually draws high current to supply its internal differential amplifiers and emitter-follower circuits, CMOS draws current primarily when it is switching. The total power dissipation of a CMOS device is dependent on the number of gates, the switching frequency, and the loading on the output of the gates. The revolution in CMOS technology that has resulted in densities of 100K gates has been accompanied by increases in all of the factors influencing power dissipation. Prior to 1985, when Fujitsu introduced the world's first 20,000 gate array, the C20000UH, CMOS gate arrays were not of sufficient integration density to warrant concerns about thermal control, but advancing CMOS technologies have forced this issue to the surface.

Because power is the product of current and voltage, power dissipation is important when defining the necessary power supply currents. Propagation delays and reliability of a device are also dependent on the temperature at which the die operates, as discussed in Sections 2.3.3 and 2.4.4. To ensure that speed and reliability requirements are satisfied, the designer needs to estimate the power dissipation of the device and, from this information, choose appropriate packages and system cooling techniques.

## 5.1 Estimation of Power Dissipation in CMOS Circuits

There are two constituent factors in the power dissipation of a semiconductor device: the DC power, which is dependent on the steady-state (quiescent) current, and the AC or dynamic power.

#### 5.1.1 Estimation of Dynamic (AC) Power Dissipation

CMOS circuits are constructed of FETs, which possess very small leakage currents. Therefore, CMOS possesses a low quiescent or steady-state current. CMOS dissipates power primarily while it is charging or discharging node capacitance, or drawing switching current, which occurs as a gate changes state. This can be modeled as the familiar pull-up/pull-down circuit discussed in Section 4.1, charging and discharging a node capacitance,  $C_L$  (shown in Figure 14). This model holds true whether the node is internal or off-chip.

The switching current is a result of charging and discharging the node capacitance which, for periodic signals, occurs twice a cycle: once while charging the capacitance, and once while discharging it. The energy involved in charging or discharging a capacitance is  $1/2(CLV^2)$ . The power is the energy divided by the period of time between successive changes (the clock period, T), multiplied by the two transitions that occur per cycle. Therefore, the dynamic or switching current of a CMOS circuit is defined as

$$Pd-dyn = 2 \qquad * \quad \frac{(C_L * V^2)}{2 * T} = (C_L * V^2) * f$$

where *V* is the supply voltage and *f* is the frequency of the given signal.

This is the power calculation for a single gate. The power dissipation for entire chip, however is much more complicated, since not all gates are simultaneously active. The degree of switching activity varies greatly within a circuit and depends on the nature of the circuits (synchronous sequential gates tend to switch concurrently, while combinatorial gates switch more randomly), the input stimulus (whether the circuit is stimulated at a periodic interval or asynchronously), and other design-dependent issues. Based on Fujitsu's experience, gate activity is on the average about 20 percent. This same figure is applied to the power estimation for output and input buffers.

## 5.1.2 Estimation of Quiescent (DC) Power Dissipation

There are two sources/sinks of DC current in a CMOS ASIC: the leakage current of the gates (gate leakage) and the DC current that flows through output and bidirectional buffers in output mode. The gate leakage in CMOS devices, even dense ones, is in the range of tens of microamperes, and is negligible. The DC current of the output buffers is the current that the buffer sources or sinks in steady state. This current level depends on the leakage currents of the driven loads, but for simplicity will be assumed to be equivalent to the IoL and IoH rating of the buffers. The DC power can be estimated for each output buffer by analyzing:

- a. the product of source current times the voltage difference from the power rail  $(V_{DD} V_{OH})$ , and
- b. the sink current times the low-level voltage  $(V_{OI})$ .

This calculation is valid provided the duty cycle, or the portion of the cycle in which the output is low versus the portion of the cycle in which the output is high, weighs the sum of the two components. The total DC power may be determined by extending this method to each output and bidirectional buffer.

#### 5.1.3 Estimation of Total Power Dissipation

The total power dissipation of a circuit is the sum of the DC and AC components. I/O buffers dissipate both DC and AC power when switching, while internal gates may be considered for the sake of simplicity, to dissipate only AC. The theory behind CMOS power dissipation is simple; however, the task of calculating the power dissipation can be tedious and prone to error. Therefore, Fujitsu has devised methods for estimating the power dissipation for each CMOS technology. These methods are presented in the Design Manual for the appropriate technology, available through the Field Applications Engineers at local Fujitsu Sales Offices or Technical Resource Centers.

#### 5.2 The Relationship Between Power Dissipation and Temperature

A device draws current through the power supply pins and the I/O buffers. As it does so, it dissipates thermal energy proportional to the power dissipated in the device. Assuming that the power dissipation of a device has been estimated as  $P_{\rm d}$ , using the method described in Section 5.1.1, how can one relate this power to the temperature of the die and the package, and also determine the warming effect on the surrounding environment?

The answer lies with two principles of heat transfer: conduction and convection. When an object is in a state of thermal equilibrium it is isothermal, seeing a constant temperature across its body. As the tem-

perature of one end of the object is raised by the introduction of energy, it is no longer in equilibrium; heat begins to flow from the warmer region to the cooler region through the process of conduction.

When a lake in winter is filled with water at a constant temperature, just above 32°F, it may still freeze. It will freeze at the surface, however, not the bottom. This is because heat is drawn from the water into the air through convection, the act of cooling by a gas.

These same mechanisms, conduction and convection, act upon a packaged semiconductor device and determine its junction temperature, the package or case temperature, and the warming effect on the surroundings.

#### 5.2.1 Determining the Junction Temperature of a Device

Figure 25 shows the paths through which heat flows in a packaged device. Each interface of materials with different properties of thermal conduction must be considered when determining the flow of heat from the die to the surroundings. The back side of the die is attached to a lead frame or slug, usually by means of a cutectic bond (material heat bonded with some conductive material, such as silver). Heat flows through this path from the die to the package, then from the package to the surrounding air.

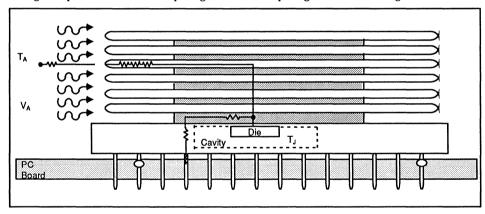


Figure 25. Heat Flow through a Cavity-down Ceramic PGA with an Annular Fin Heat Sink

From the die junction to the package, there is some associated thermal impedance (or resistance to the flow of heat). This impedance can be calculated, but may also be estimated in the following way. Operate a device and determine its power dissipation. Then, using some mechanism such as a thermal diode, whose forward bias voltage tracks linearly with temperature, determine the junction temperature. Then, after measuring the case temperature, determine the thermal impedance along the path from the die junction to the case (package body) using the following equation:

$$\theta jc = \frac{(Tc - Tj)}{P_d}$$

where  $T_c$  and  $T_i$  are the case and junction temperatures, respectively.

A similar procedure is followed when determining the thermal impedance between the junction and the ambient environment, except that the case temperature is replaced by the measurement of the ambient temperature

$$\theta ja = \frac{(Ta - Tj)}{P_d}$$

While  $\theta_{jc}$  relies on conduction as its cooling mechanism,  $\theta_{ja}$  reflects convective cooling. Therefore,  $\theta_{ja}$  varies with airflow and is specified at a given airflow, or as static (= 0).

Since thermal impedance depends on the heat conduction path between the die and some other interface, it can be modeled the same way as current flowing through real impedance or resistance. Therefore, as in circuit theory, when multiple interfaces are oriented in parallel, the thermal impedance is lowered. However, the situation is different from circuit theory in that when a very low impedance interface, such as a heat sink, is placed in the conduction path the flow capacity is increased, with the heat sink pulling heat out at a faster rate, lowering the thermal impedance.

#### 5.2.2 Using Thermal Impedance Data

Thermal impedance information and power dissipation information are used to estimate junction temperature and ambient temperature rise. Which impedance figure to use is based on how the device is to be cooled. If the device is air cooled (convective), then  $\theta_{ja}$  should be applied, while  $\theta_{jc}$  should be used if conductive techniques such as heat pipes or cold plates are employed. For example, the junction temperature may be obtained by multiplying the power dissipation of the device by the appropriate  $\Theta_{ja}$  and adding the ambient temperature. It is not surprising that this indicates that a small thermal impedance is desirable to achieve a low junction temperature.

Junction temperature is used to determine worst case delay multipliers and the package options for Fujitsu's CMOS AU (Sea-of-Gates) family. The junction temperature also indicates whether reliability goals are being met. The designer can trade off packages (which exhibit varying thermal impedances) with cooling techniques (such as varying the amount of airflow in a system) to achieve the desired junction temperature and consequently, worst case delay multiplier and reliability targets.

#### 5.3 Summary of Thermal Issues

Although thermal factors in CMOS design have not previously been an issue, the increased frequency and density of current generations of CMOS devices require such considerations to be made. This section has surveyed some of the issues involved in applying thermal analysis to CMOS devices and using the information gained from such analysis to determine the appropriate packaging and cooling techniques.

#### 6.0 Summary of the Note

As VLSI circuits increase in complexity, pin count and die size increase as well, placing greater demands on packaging, board layout, and manufacturing. Fujitsu has addressed these problems with exotic forms of packaging such as the surface mount PGA and the staggered PGA, while also stressing the importance of other surface mount packages. But simply making these packages available is not enough; Fujitsu must also provide the technical support necessary to ensure that these packages can be used successfully by our customers. Field Applications support in the local sales offices, technical information such as this Application Note, and packaging consultants at Fujitsu's San Jose headquarters all provide this support.

# F

#### References

Applications Engineering Staff. Points and Problems on Reliability and Mounting of Surface Mount ICs. Fujitsu Limited, 1988.

Hoshino, H. and K. Gotanda. Reliability of Surface Mount ICs. Fujitsu Limited, 1987.

Kane, Jim. Surface Mount Technology. Santa Clara: Fujitsu Microelectronics Inc.; August 1986.

Fujitsu Limited, Semiconductor Marketing. *Integrated Circuits Quality and Reliability*. Tokyo, Japan: Fujitsu Limited, 1984.

Mather, John C. "A Status Report on Multilayer Circuit Boards." *Proceedings, 30th Electronic Components Conference.* 1980, pp 302–306.

Vest, Roger. "How to Design a Fine Pitch Footprint." Nepcon East: 1988.

# **AU Series CMOS Gate Array** Unit Cell Library

Page	Contents
	Unit Call Consideration Information
2-2	Unit Cell Specification Information
1	Inverter and Buffer Family
2–15	NAND Family
2-29	NOR Family
2–43	AND Family
2–49	OR Family
2–55	EXNOR/EXOR Family
2–65	AND-OR-Inverter Family
2–73	OR-AND-Inverter Family
2–81	Multiplexer Family
2-103	Clock Buffer Family
2-117	Scan Flip-Flop (Positive Edge Type) Family
2–179	Non Scan Flip-Flop Family
2-207	Binary Counter Family
2-247	Adder and ALU Family
2–255	Data Latch Family
2–273	Shift Register Family
2–285	Parity Generator/Selector/Decoder Family
2–313	Bus Driver Family
2–323	Clip Cell Family
2–327	I/O Buffer Family
2–439	Single-Port RAM Specification
2-445	Dual-Port RAM Specification
2–451	Triple-Port-RAM Specification
2–457	ROM Specification
2–461	Appendix A: General AC Specifications
2–463	Appendix B: Hierarchical Structure
2–465	Appendix C: Estimation Tables for Metal Loading
2–473	Appendix D: Available Package Types
2–475	Appendix E: TTL 7400 Function Conversion Table
2–479	Appendix F: Alphanumeric Index of Unit Cells

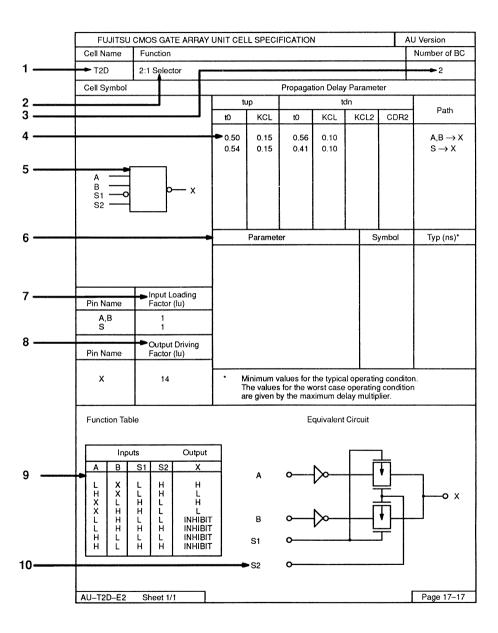
# **Unit Cell Specification Information**

This section contains specifications for all the unit cells available for the CG21 Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates. A basic cell contains one pair of P-channel and one pair of N-channel transistors (and two pairs of smaller N-channel resistors used for compiled cell construction).

# How to Read a Unit Cell Specification

The following paragraphs numbered 1–10 explain how the information given in the CG21 Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

- 1. The unit *cell name* appears in the upper left corner of the page.
- 2. The unit cell function is given on the same line as the unit cell name.
- 3. The *number of basic cells (BC)* or equivalent that make up the unit cell is shown in the upper right corner of the page.
- 4. Propagation delay parameters for the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t<sub>0</sub>) is given in ns. K<sub>CL</sub>, the delay constant for the cell (delay time per load unit) is given in ns/pF. K<sub>CL2</sub> and C<sub>DR2</sub> are a delay constant and an output driving factor used to calculate delay when a unit cell is loaded beyond its published output driving factor (C<sub>DR</sub>).
- 5. The cell symbol (logic symbol) is shown in the top left box under the cell name.
- Clock parameters (in ns) for unit cells such as flip-flops and counters that make use of clock signals
  are given in a table directly below the propagation delay parameters.
- 7. The input loading factor of each input of the unit cell are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
- The output drive factor of each output of the unit cell is shown directly under the input loading factor.
   The output drive factor is the maximum number of load units the unit cell can drive while performing at published specifications.
- 9. The function table (truth table), if applicable, is shown in a box at the lower left side of the page.
- The unit cell schematic, or equivalent circuit, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.



# Inverter, Buffer Family

Page	Unit Cell Name	Function	Basic Cells
2-7	V1N	Inverter	1
2–8	V2B	Power Inverter	1
2–9	V1L	Inverting Clock Buffer	2
2-10	B1N	True Buffer	1
2-11	BD3	Delay Cell	5
2-12	BD4	Delay Cell	4
2-13	BD5	Delay Cell	9
2-14	BD6	Delay Cell	17

FUITTSII	CMOS GATE A	RRAY II	NIT CEL	L SPECT	FICATIO	N		"Al	J" Version
Cell Name	Function		000		10.1110	·			Number of BC
V1N	Inverter								1
Cell Symbol				Prop	agation			er	
			t0	up KCL	t0	td KCL	n KCL2	CDR2	Path
			0.23	0.13	0.28	0.07	0.10	4	Path A → X
			0.23	0.13	0.20	0.07	0.10		
					1				
									ļ
	$\sim$ .								
Α	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	۲							
					1				
			Parame	ter			l s	ymbol	Typ(ns)*
								·	1
	T +						-		
Din Mana	Input Los	ading							
Pin Name A	Factor (	εu)					1		
A	1								
							1		
							1		
	Output D	riving					1		
Pin Name	Factor (	lu)							
X	18								
			. w			41	1		
			* Mini	mum val	ues for	tne ty	pical o	perat:	ing condition.
			are	values oiven h	for the y the m	worst	delaw m	mltin'	ng condition
			are	PTAGII D	y LITE III	av Till mill	четау п	атетр.	1101.
ATI TO I	Chart 1/1								Page 1-1
AU-V1N-E2	Sheet 1/1								Page 1-1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		7A"	J" Version Number of BC
Cell Name	Function							Number of RC
V2B	Power Inverter		P		n. 1 · · ·	D		1
Cell Symbol		t.	up up	agation	Delay td	raramet n	er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		0.20	0.07	0.20	0.04	0.07	7	$A \rightarrow X$
	·							
A	x x							
		Parame	ter			S	ymbol	Typ(ns)*
							-	
	Input Loading							
Pin Name	Factor (lu)							
A	2							
		ļ						
ļ	Output Driving							
Pin Name	Factor (lu)							
Х	36							
		* Mini	mum val	ues for	the tv	mical o	pperat	ing condition.
		The	values	for the	worst	case or	perati	ng condition
		are	given b	y the m	aximum	delay n	nultip	lier.
AU-V2B-E2	Sheet 1/1							Page 1-2

FULITSU C	MOS GATE ARRAY U	NIT CEL	T. SPECT	FICATIO	N		"AU	J" Version
Cell Name	Function	NII OLD	u biloi	TICKTIO	14			Number of BC
								2
V1L Coll Symbol	V1L Inverting Clock Buffer Cell Symbol Propagation Delay Parameter							
Cell Symbol		t	up	agation	td		er	1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.28	0.03	0.54	0.03			Path A → X
							l	
							}	
A —	> х						l	
A	/° x							
							l	
		D			L	L		7()%
		Parame	ter				ymbol	Typ(ns)*
						l		
	Input Loading							
Pin Name	Factor (lu)							
A	4							
								İ
D	Output Driving							
Pin Name X	Factor (lu)							
, and								
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati:	ng condition
	1	are	given b	y the m	naximum	delay n	urtip	lier.
AU-V1L-E2 S	Sheet 1/1							Page 1-3

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	Version
Cell Name	Function						1	Number of BC
								_
B1N	True Buffer		P		D-1	D		1
Cell Symbol			Prop	agation	Delay td		cer	7
		t0	up KCL	t0	KCL	n KCL2	CDR2	Path
		0.47	0.13	0.55	0.07	RODZ	ODKZ	Path A → X
	N ,							
Α	x		,					
		Parame	ter				Symbol	Typ(ns)*
						- 1		
						1		
						1		
	Input Loading							
Pin Name	Factor (lu)							
A	1					.		
						-		
						1		
						Ţ		
<b></b>	1 Out and Division							
Din Nama	Output Driving							
Pin Name X	Factor (lu)							
						1		
		* Mini	mum val	ues for	the ty	pical	operati	ng condition.
		The	values	for the	worst	case o	peratin	g condition
ļ		are	given b	y the m	naximum	delay	multipl	ier.
	•							
AU-B1N-E2	Sheet 1/1							Page 1-4

FULITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		П'А	U" Version
Cell Name	Function				• • • • • • • • • • • • • • • • • • • •		1 1	Number of BC
BD3	Delay Cell							
Cell Symbol	Delay Cell		Prop	agation	Delay	Paramet	er	5
			up		td	n		<u> </u>
		t0	KCL	t0 3.77	KCL	KCL2	CDR2	Path A → X
		4.27	0.13	3.77	0.10	0.11	4	$A \rightarrow X$
Α	x							
		Parame	tor		l	1 .	ymbol	Typ(ns)*
		rarame	rer				ymbol	Typ(IIS)"
· · ·	Input Loading							
Pin Name A	Factor (lu)							
	1							
	Output Driving							
Pin Name	Factor (lu)							
X	18							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	naximum	delay n	ultip	lier.
1								
1								
AU-BD3-E2	Sheet 1/1							Page 1-5
								1 0

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function					·····		Number of BC
BD4	Delay Cell							4
Cell Symbol		+1	Prop up	agation	Delay td	<u>Paramet</u> n	er	<del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		2.85	0.46	3.28	0.25	0.29	4	A + X
	_							1
Α	x							
								į
								T ()
		Parame	ter			-+ s	ymbol	Typ(ns)*
						-		
						1		1
Din Nama	Input Loading							
Pin Name A	Factor (lu)							
						1		
	Output Driving							
Pin Name X	Factor (lu)							
^								
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition
		The	values given h	for the	worst	case op delav m	erati ultir	ng condition
			011011	,				
1								
1								
]								
1								
AU-BD4-E2	Sheet 1/1							Page 1-6

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"Al	J" Version
Cell Name	Function	***************************************						Number of BC
BD5	Delay Cell	·						9
Cell Symbol			Prop	agation	Delay		er	<del></del>
		t0	up KCL	t0	KCL KCL	KCL2	CDR2	Path
		8.74	0.13	8.28	0.08	0.12	4	Path A → X
							i	
				ł				
Α	x							
Δ.	^							
				1				
		Parame	ter			S	ymbol	Typ(ns)*
						ļ		ł
						1		1
						}		
		İ				1		
						į		
	Input Loading	1				- 1		
Pin Name	Factor (lu)	1				1		
Α	1							
						1		
		İ				İ		
	Output Driving	1						
Pin Name	Factor (lu)							
X	18							1
		* Mini	mum val	ues for	the tw	nical o	nerat	ing condition.
		The	walues	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
		•						
								,
AU-BD5-E2	Sheet 1/1							Page 1-7

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
77.	2 2 2 2 2							
BD6 Cell Symbol	Delay Cell		Dron	agation	Dolass	Damamat		17
Cell Bymbol		tı	up	agation	td	n	<u>er</u>	1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		17.6	0.14	17.46	0.07	0.11	4	Path A → X
	$\sim$							
Α	x							
		Parame	ter	1	L	S	ymbol	Typ(ns)*
						1		
						1		
	Input Loading					-		
Pin Name	Factor (lu)							
A	1					İ		
D: 13	Output Driving							
Pin Name X	Factor (lu)							
^	10							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
1								
1								
								<del></del>
AU-BD6-E2	Sheet 1/1							Page 1-8

## **NAND Family**

Page	Unit Cell Name	Function	Basic Cells
2–17	N2N	2-input NAND	1
2–18	N2B	Power 2-input NAND	3
2–19	N2K	Power 2-input NAND	2
2–20	N3N	3-input NAND	2
2-21	N3B	Power 3-input NAND	3
2–22	N4N	4-input NAND	2
2–23	N4B	Power 4-input NAND	4
2-24	N6B	Power 6-input NAND	5
2–25	N8B	Power 8-input NAND	6
2–26	N9B	Power 9-input NAND	8
2–27	NCB	Power 12-input NAND	10
2–28	NGB	Power 16-input NAND	11

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"Al	U" Version
Cell Name	Function							Number of BC
				,				
N2N	2-input NAND						i	1
Cell Symbol		+-		agation	Delay		er	
		t0	up KCL	t0	KCL KCL	KCL2	CDR2	- Path
		0.30	0.13	0.45	0.11	RCDZ	CDRZ	Path A → X
		0.50	0.13	0.43	0.11			
A1								
A2	р—— х							
	_							
		Parame	ter			T s	ymbol	Typ(ns)*
						- 1		
						1		
	Tana Tanadian					l		
Pin Name	Input Loading Factor (lu)							
A	1							
••	1							
						ı		
						į		
	Output Driving							
Pin Name	Factor (lu)					l		
Х	18							
		* Mini	mum 1201	nos for	the tw	nical o	norat	ing condition.
		The	mum vai values	for the	worst	picai o	perati	ng condition
		are	varaes given b	v the m	aximum	delav m	ultip	lier.
	1		0					
				*				
AU-N2N-E2	Sheet 1/1							Page 2-1

FUJITSU Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		''A''	U" Version Number of BC
N2B Cell Symbol	Power 2-input N	AND	Prop	agation	Delay	Paramet	er	3
			up		td	n		
		t0 0.88	KCL 0.07	t0 1.14	0.03	KCL2	CDR2	Path A → X
		0.00	0.07	1.1	0.05			
A1	7							
A2	x							
		Parame	ter			S	ymbol	Typ(ns)*
						l		
Pin Namo	Input Loading					ļ		
Pin Name A	Factor (lu)					ŀ		
						ļ		
						ĺ		
	Output Driving							
Pin Name	Factor (lu)							
X	36							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the y the m	worst	case op	erati:	ng condition
		l are	Rivell D	y the m	a V T III U III	четаў П	штетр	1161.
AU-N2B-E2	Sheet 1/1							Page 2-2

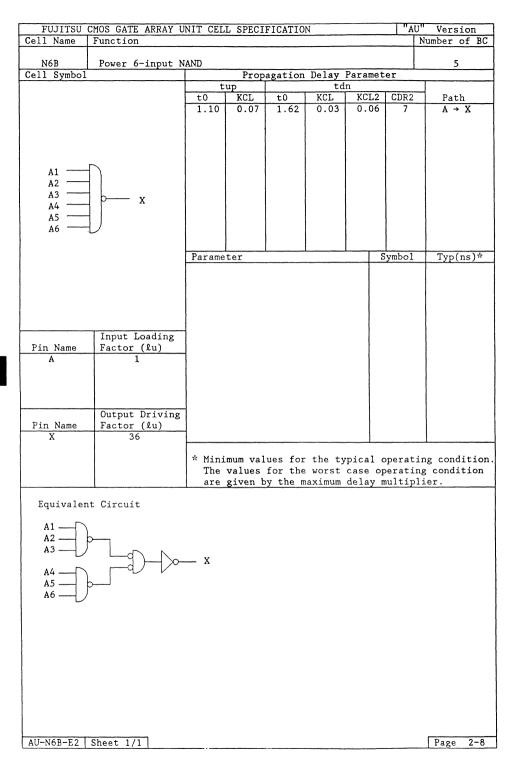
FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version	
Cell Name	Function							Number of B	С
Nor	D 0 10 11 11	ANTO						•	
N2K Cell Symbol	Power 2-input N	AND	Pron	agation	Delay	Paramot	er	2	_
CCII Bymbol		t	up Frop	agation	td	n	<u> </u>	<u> </u>	
		t0	KCL	t0	KCL	KCL2	CDR2		
		0.30	0.07	0.35	0.06	0.07	7	A - X	
									-
									1
									1
A1	·								
A2	, р—— х								- 1
								İ	
		Parame	ter			S	ymbol	Typ(ns)*	
						-			
						- 1			
						1			
	17								
Pin Name	Input Loading Factor (lu)					İ			ĺ
A	2								
						ŀ			
						l			
	Output Driving								
Pin Name	Factor (lu)					1			
X	36								
		4	,						
		" Mini	mum vai values	ues for	worst	picai o	perat	ing condition	n.
		are	given b	y the m	aximum	delav m	ultip	lier.	•
		•	-						
AU-N2K-E2	Sheet 1/1							Page 2-3	3

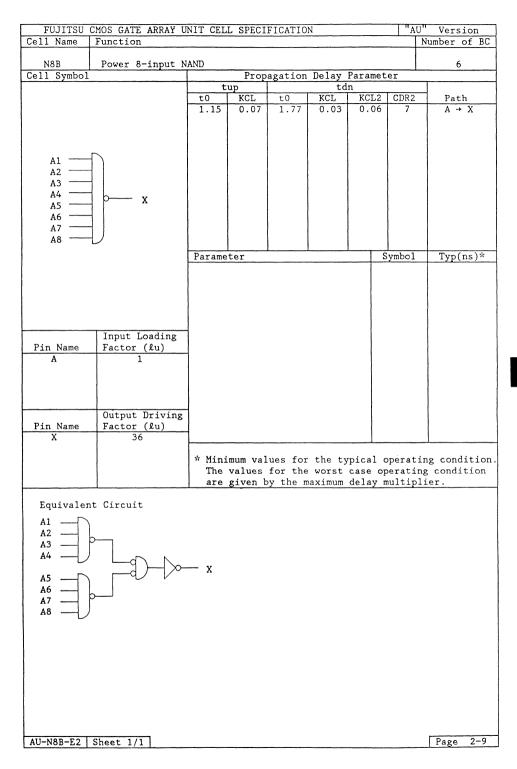
FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			AU"		ion
Cell Name	Function							N	umber d	of BC
								1	_	
N3N	3-input NAND		D		D-1 ::	D · · · ·			2	
Cell Symbol		+	up up	agation	Delay td	raramet	eI			
		t0	KCL	t0	KCL	KCL2	CDR	2	Pati	,
		0.42	0.13	0.55	0.15	ROBE	UDI.	-	Path A →	<u>x</u>
							ŀ			
A1	$\sim$						Ì			
A1 ————————————————————————————————————	b x									
A3	1									
113									1	
							l			
		Parame	ter			S	ymbo	1	Typ(1	ıs)*
	Input Loading									
Pin Name	Factor (lu)									
A	1									
	Output Driving									
Pin Name	Factor ((1))					İ				
X	Factor (lu)					ł				
									·	
		* Mini	mum val	ues for	the ty	pical o	pera	tin	g cond:	ition.
					worst					tion
		are	given b	y the m	aximum	delay n	ulti	pli	er.	
İ										
1										
AU-N3N-E2	Chast 1/1								Page	2-4
I MO-NON-EZ I	SHEEL I/I I								IIake	4

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
	Function							Number of BC
N3B	Power 3-innut M	AND						
N3B Cell Symbol	Power 3-input N	מאח	Prop	agation	Delav	Paramet	er	3
		tı	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		1.03	0.07	1.36	0.03			A + X
		ł						
	_							
A1	h							
A2 ————————————————————————————————————	р— х						1	
r) [								
							1	
							<u>L</u>	
		Parame	ter			S	ymbo1	Typ(ns)*
						}		
	T T 1:							
Pin Name	Input Loading Factor (lu)					ĺ		
Pin Name A	ractor (ku)							
	_					1		
						1		
						1		
	Output Driving							
Pin Name	Factor (lu)							
X	36							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		ine	values given h	for the y the m	worst	case op delav m	erati ultir	ng condition
	1	are	61 V C II L	, one m	· · · · · · · · · · · · · · · · · · ·			
AU-N3B-E2 S	hoot 1/1							Page 2-5
20 NODE 6	MEEL I/I							I Lage 4 J

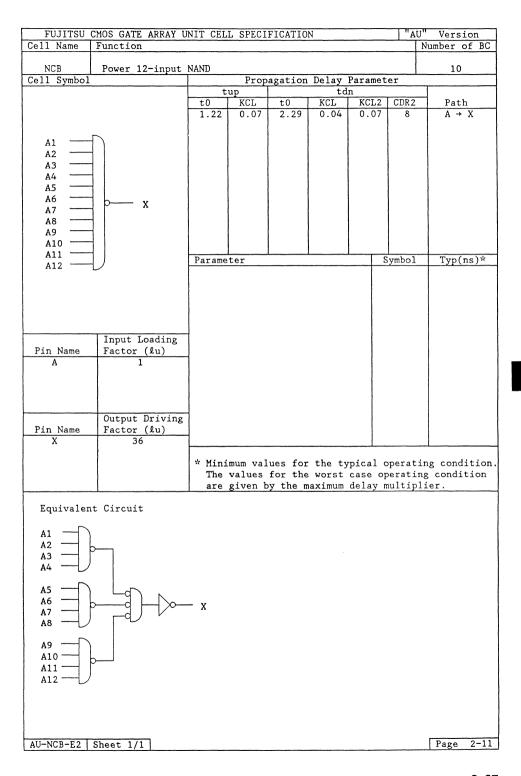
FUJITSU Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	J" Version Number of BC
N4N Cell Symbol	4-input NAND		Prop	agation	Delay	Paramet	er	2
			up		td	n		
		t0 0.50	KCL 0.13	t0 0.59	KCL 0.19	KCL2	CDR2	Path A → X
		0.50	0.15	0.55	0.15			n . n
								1
A1	<b>n</b>							]
A2	x							
A3	] )							
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name A	Factor (lu)							
	1							
į						Ì		
	Output Driving					ļ		
Pin Name X	Factor (lu)							
••					***************************************			L
		* Mini	mum val	ues for	the ty	pical c	perati	ing condition.
		are	values given b	y the m	aximum	delay m	ultipl	ng condition
								,
AU-N4N-E2	Sheet 1/1							Page 2-6

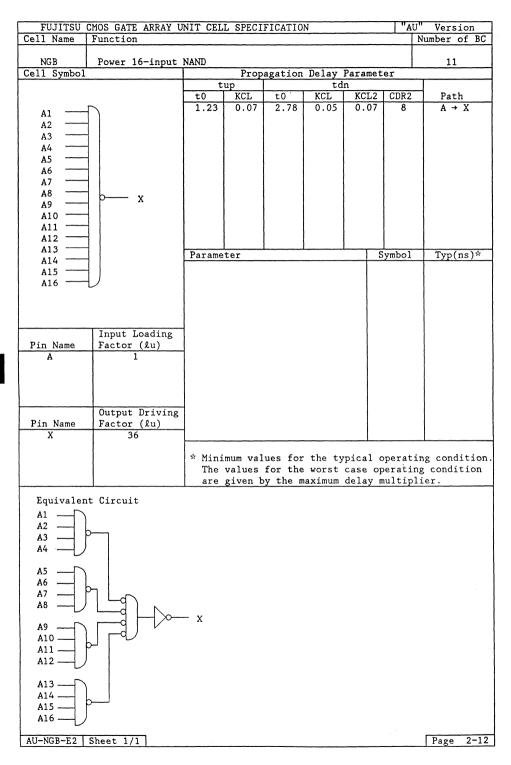
FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version	ı
Cell Name	Function			Number of	BC				
									- 1
N4B	Power 4-input N	IAND			D 1	D		4	
Cell Symbol		-		agation	td		er	<del></del>	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path	
		1.11	0.07	1.52	0.03	ROBE	OBKE	A + X	-
							l		
									1
								1	
							ì		
A1	1								
A2	<del>                                      </del>								
А3 ——	р—— х						l		
A4	$\cup$								
								1	
		1					l		
		Parame	ter			S	ymbol	Typ(ns)	*
		ļ							1
	Input Loading	1							
Pin Name	Factor (lu)	1				j			
A	1	1							
		ŀ							
	Output Driving	1							
Pin Name	Factor (lu)								
X	Factor (lu)								
		<b>.</b>	_	_					. 1
		* Mini	mum val	ues for	the ty	pical c	perat	ing conditi	lon.
		ine	varues given b	for the	worst	dolar m	erati w1+in	ng conditio	211
		are	given b	y the in	axillulli	deray n	штетр	iiei.	
									1
AU-N4B-E2	Sheet 1/1							Page 2-	-7





FILLITSU	MOS GATE ARRAY U	NIT CELL S	PECIFIC	ΔΤΙΟΝ			Π Δ	U" Version
	Function	TILL OUTIL B.	LUCIFIC				^	Number of BC
NOP	Davier O-innut N	I A NID						٥
N9B Cell Symbol	Power 9-input N	מאות	Propaga	tion	Delay:	Paramet	er	8
		tup			td	n.		
			CL t	.13	0.04	0.07	CDR2	Path A → X
A1								
A2								
A4								
A5	р—— x							
A6 ———								
A8	)							
A9 —		Parameter			1	S	ymbol	Typ(ns)*
}						l		
<u> </u>	Input Loading							
Pin Name	Factor (lu)					1		
A	1							
						İ		
	Output Driving					1		
Pin Name X	Factor (lu)							
^	36							
		* Minimum	values	for	the ty	pical c	perat	ing condition.
		are giv	ues for en by t	the he ma	worst ximum	case or delay m	eratı nultip	ng condition
- · ·								
Equivaler	nt Circuit							
A1 -								
A2								
A3 -								
A4 -		V						
A5 0		— x						
A7 —								
A8 A9								
AU-N9B-E2 S	Sheet 1/1							Page 2-10





## **NOR Family**

Page	Unit Cell Name	Function	Basic Cells
2–31	R2N	2-input NOR	1
2–32	R2B	Power 2-input NOR	3
2–33	R2K	Power 2-input NOR	2
2–34	R3N	3-input NOR	2
2–35	R3B	Power 3-input NOR	3
2–36	R4N	4-input NOR	2
2–37	R4B	Power 4-input NOR	4
2–38	R6B	Power 6-input NOR	5
2–39	R8B	Power 8-input NOR	6
2-40	R9B	Power 9-input NOR	8
2-41	RCB	Power 12-input NOR	10
2–42	RGB	Power 16-input NOR	11

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			u" Version
Cell Name	Function							Number of BC
R2N	2-input NOR							1
Cell Symbol	Inpac Non		Prop	agation	Delay	Paramet	er	1
			up		td	n		
		t0 0.32	KCL	t0 0.35	KCL 0.07	KCL2 0.09	CDR2	Path A → X
		0.32	0.23	0.33	0.07	0.09	4	ATA
	Δ							
A1 ——— A2 ———	x							
A2								
		Parame	ter			S	ymbo1	Typ(ns)*
						1		
Pin Name	Input Loading Factor (lu)							
A	1							
						1		
}	Output Driving							
Pin Name	Factor (lu)							
Х	14							
		* Mini	miim 17a1	ues for	the tw	nical c	norat	ing condition
		The	walues	for the	worst	case or	erati	ing condition
		are	given b	y the m	aximum	delay m	ultip	olier.
İ								
AU-R2N-E2	Sheet 1/1							Page 3-1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
DOD	D 0 ! ''	OB						
R2B Cell Symbol	Power 2-input N	UK	Pron	agation	Delass	Parame+		3
OEII DAMPOI		tı	up	agation	td	n n	e I	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.09	0.07	1.00	0.03			Path A → X
							1	
							}	
								į
۸۱	4						l	
A1 ————————————————————————————————————	р— х						1	
							l	
		Parame	ter			S	ymbol	Typ(ns)*
-								
	Input Loading							
Pin Name	Factor (lu)							
A	1							
						l		
						l		
	Output Driving					ļ		
Pin Name X	Factor (lu)	1						
^	30	<b></b>						
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay n	ultip	olier.
1								
1								
1								
AU-R2B-E2	Sheet 1/1							Page 3-2

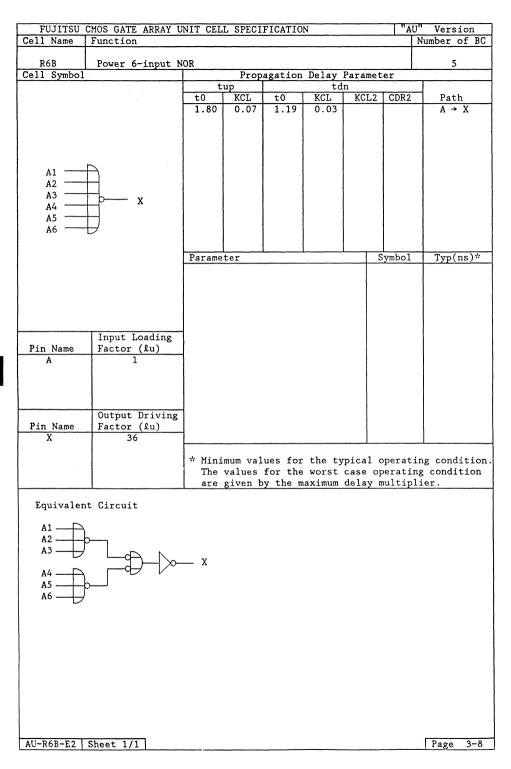
FUJITSU (	CMOS GATE ARRAY U. Function	NIT CEL	L SPECI	FICATIO	N			U" Version Number of BC
Cell Name	Function	·						Number of BC
R2K	Power 2-input N	OR	Dwan	<del></del>	Do 1 arr	Damamat		2
Cell Symbol		t	up Prop	agation	Delay td	raramet n	er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.36	0.11	0.36	0.05			A -> X
A1 -	A							
A2	_р х							
						•		
		Parame	ter			l s	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
Α	2					Ì		
	Output Driving					ļ		
Pin Name	Factor (lu)					1		
X	36							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
	1	are	given b	y the m	aximum	deray n	urtip	iler.
								!
AU-R2K-E2	Sheet 1/1							Page 3-3

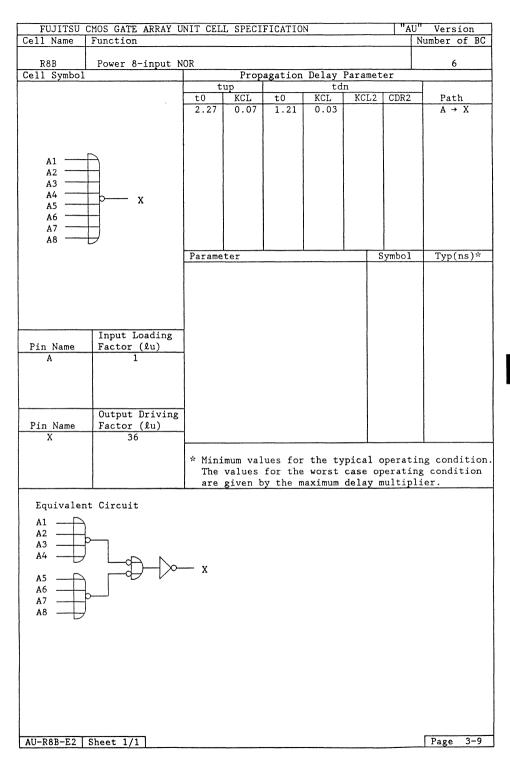
FUJITSU Cell Name	CMOS GATE ARRAY U Function	NIT CEL	L SPECI	FICATIO	N	······································	"Al	U" Version Number of BC
R3N Cell Symbol	3-input NOR		Prop	agation	Delay	Paramet	er	2
		t	up		td	n		
		t0 0.67	KCL 0.33	t0 0.37	KCL 0.07	KCL2 0.10	CDR2	Path A → X
A1	A							
A2 —— A3 ——	x							
					,			
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)					1		
A	1							
		ļ						
	Output Driving							
Pin Name X	Factor (lu)							
		* Mini The	mum val values	ues for for the	the ty worst	pical c case or	perat: erati	ing condit <mark>ion.</mark> ng condit <mark>ion</mark>
		are	given b	y the m	aximum	delay m	ultip	lier.
}								
İ								
AU-R3N-E2	Sheet 1/1							Page 3-4

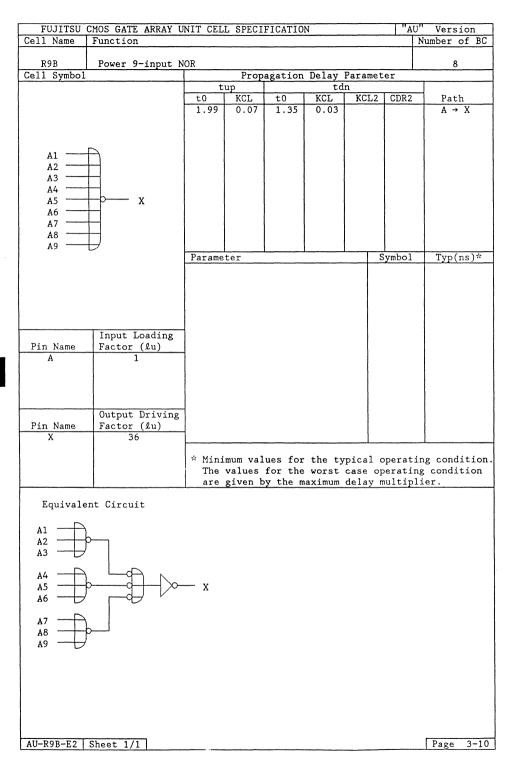
FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	" Version
Cell Name	Function							Number of BC
R3B	Power 3-input N	OR						3
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up KCL		td	n		Path
		t0 1.59	0.07	t0 1.10	KCL 0.03	KCL2	CDR2	Path A → X
		1	• • • • • • • • • • • • • • • • • • • •	1110	0.00			
	_							1
A1								
A2 A3	x							
113								
		Parame	ter			l s	ymbol	Typ(ns)*
		1224.110				—   <u> </u>	·	-75 ()
						ļ		
						l		
	<del></del>							
Din Nama	Input Loading Factor (lu)							1
Pin Name A	1	1						
	Output Driving	1						
Pin Name	Factor (lu)							
X	36							<b></b>
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
AU-R3B-E2	Sheet 1/1							Page 3-5

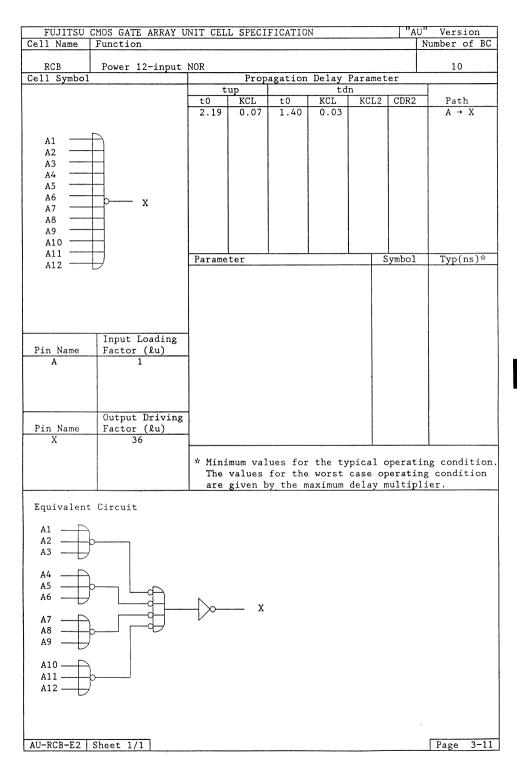
FUJITSU Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			U" Version Number of BC
R4N	4-input NOR							2
Cell Symbol	211000 11011		Prop	agation	Delay	Paramet	er	
			up		td KCL	n		D.+1
		t0 0.99	KCL 0.43	t0 0.37	0.07	KCL2 0.11	CDR2	Path A → X
	:	0.,,	0.15	0.57	0.07			
					ĺ			
	i							
					i			1
A1	A							
A2	—— x							
A3	<u> </u>							
A4								
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading					1		
Pin Name	Factor (lu)					1		
A	1					ł		
	Output Driving							
Pin Name	Factor (lu)							
X	6							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay n	ultip	lier.
1								
1								
ALL DAN DO T	Ch - + 1/1							Dec. 2.
AU-R4N-E2	Sheet 1/1							Page 3-6

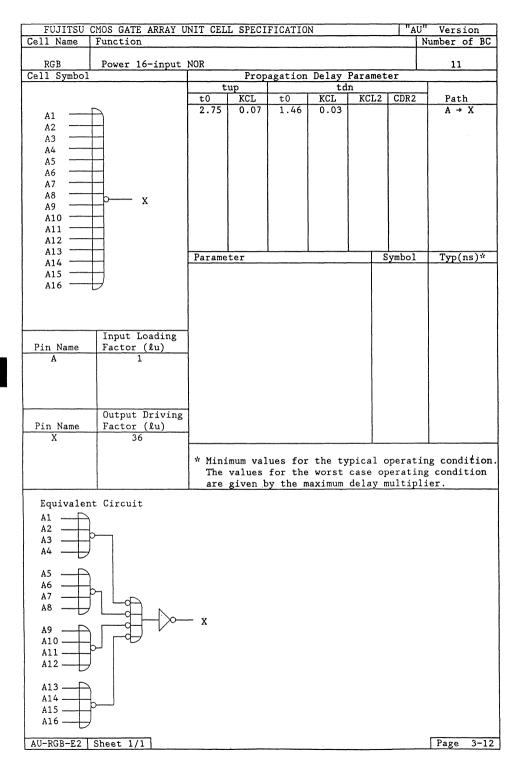
FUJITSU	CMOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	N		l "Aī	" Version
Cell Name	Function	NII ODD	<u> </u>	1011110				Number of BC
		0.0						
R4B Cell Symbol	Power 4-input N	OR	Prop	acation	Delay	Daramot		4
Cell Symbol		t	up FIOD	agacion	td			т
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		2.00	0.07	1.07	0.03			$A \rightarrow X$
	!		l					
							i	
A1	A							
A2	х							
A3	<u></u>							
A4							Ì	
								1
		Parame	ter			1 5	ymbol	Typ(ns)*
		Turumo				——— <u> </u>	7	
	Input Loading							1
Pin Name	Factor (lu)					- 1		
A	1							
		,						
n	Output Driving					ĺ		
Pin Name X	Factor (lu)	ł						
••								
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
	1	are	given b	y the m	aximum	delay n	multip.	iler.
AU-R4B-E2	Sheet 1/1							Page 3-7











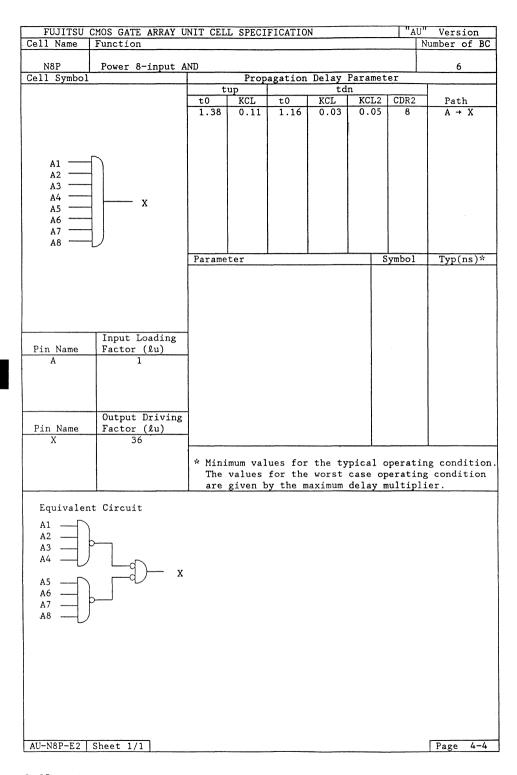
## **AND Family**

	Unit Cell		Basic
Page	Name	Function	Cells
245	N2P	Power 2-input AND	2
2-46	N3P	Power 3-input AND	3
2–47	N4P	Power 4-input AND	3
2-48	N8P	Power 8-input AND	6

FILITCII	CMOS GATE ARRAY U	NIT CEL	CDECT	EICATIO	NT.		"Al	J" Version
Cell Name	Function	NII CEL	L SPECI	FICATIO	IN		I A	Number of BC
N2P	Power 2-input A	ND						2
Cell Symbol			Prop	agation	Delay td	Paramet	er	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path
		0.81	0.07	0.69	0.03	0.05	7	A + X
							ļ	
A1	n							
A2	x							
			i					
								l
					<u> </u>	ļ	<u>L.,</u>	
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
A	1							
	Output Driving							
Pin Name X	Factor (lu)							
^	36							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
								1
AU-N2P-E2	Sheet 1/1							Page 4-1
114	222 2/2							

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		''A	U" Ver	sion
Cell Name	Function				<u></u>			Number	of BC
N3P	Power 3-input A	ND	D		D-1	D.m.c			3
Cell Symbol		t.	Prop up	agation	Delay td	raramet n	er	1	
		t0	KCL	t0	KCL	KCL2	CDR2	Pa	th → X
		1.06	0.07	0.86	0.03	0.05	7	A	→ X
	_							į	
A1 ————————————————————————————————————	1								
A3	·								
							İ	İ	
		Parame	ter				Symbol	Тур	(ns)*
	Input Loading								
Pin Name A	Factor (lu)								
•	•								
	Output Driving					1			
Pin Name X	Factor (lu)					ŀ			
^	30								
		* Mini	mum val	ues for	the ty	pical o	operat	ing cor	dition.
		are	values given b	for the	worst	case on delay r	perati multip	ng conc lier.	lition
			02.1011						
		,							<del>,</del>
AU-N3P-E2	Sheet 1/1							Page	e 4-2

FUJITSU C	MOS GATE AF	RAY UN	NIT CEL	L SPECI	FICATIO	N		"Al	J" Vers	ion
	Function								Number o	of BC
			_							
N4P Cell Symbol	Power 4-ir	iput Al	ND	Dron	agation	Dolor	Daramat		3	
Cell Symbol				up FIOD	agation	td		<u>e1</u>		
		t	t0	KCL	t0	KCL	KCL2	CDR2	Pati	1
		ļ	1.27	0.07	0.95	0.03	0.05	8	A →	X
		İ								
			ļ							1
			1							
_	_									
A1		1								
A2	— х									
A3	)									
234		1	Ì							
		ŀ	Parame	ter			T s	ymbol	Typ(:	15)%
		ŀ	Tarame	001				yb01	1,900	13)
							ļ			
		ļ					-			
		l							i	
		İ								
	Input Load	line								
Pin Name	Factor (li									
A	1									
							Ì			
							1			
		-					ŀ			
	Output Dr	iving								
Pin Name	Factor (lu									
X	36									
				_	_					
			* Mini	mum val	ues for	the ty	pical o	perat:	ing cond	ition.
		1	are	values given h	y the m	worst	delay m	ultin	ng condi	LION
	L		are	given b	y the in	aximum	delay iii	urcip.	itei.	
										ĺ
										Ì
AU-N4P-E2 S	heet 1/1								Page	4-3



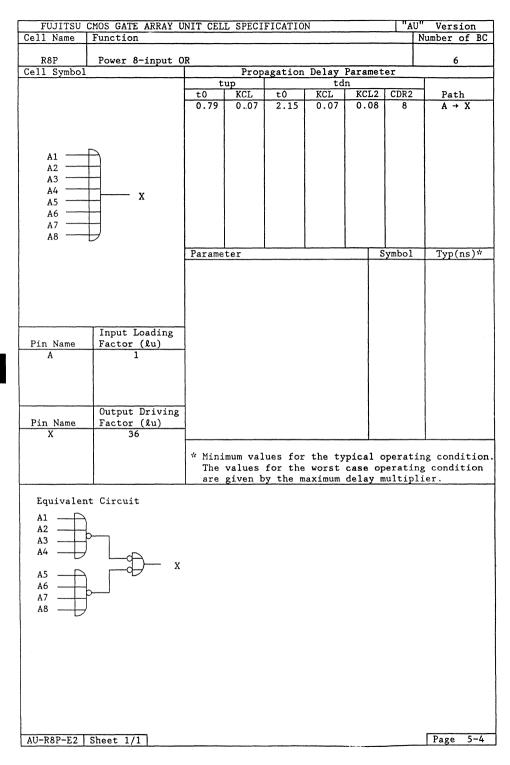
# **OR Family**

	Unit Cell		Basic
Page	Name	Function	Cells
2–51	R2P	Power 2-input OR	2
2–52	R3P	Power 3-input OR	3
2–53	R4P	Power 4-input OR	3
2-54	R8P	Power 8-input OR	6

FUJITSU C	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	J" Version
Cell Name	Function							Number of BC
R2P	Power 2-input 0	R						2
Cell Symbol			Prop	agation			er	
		t0	up	+0	td KCL	n KCL2	CDR2	- Doth
	•	0.63	KCL 0.07	t0 0.91	0.04	0.06	8	Path A → X
							1	
A1 ——	A							
A2 -	x							
							•	
		7				L		
		Parame	ter			S	ymbol	Typ(ns)*
1								
	Input Loading							
Pin Name	Factor (lu)							
A	1							
						İ		
	Output Driving							
Pin Name X	Factor (lu)							
		<b></b>						
		* Mini	mum val	ues for	the ty	rpical c	perati	ing condition.
								ng condition
	L	are	given b	y the m	aximum	delay ii	iurcip.	rier.
1								
AU DOD DO 1	01							[D 5 4
AU-R2P-E2	Sheet 1/1							Page 5-1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	J" Version
Cell Name	Function							Number of BC
202		n						•
R3P Cell Symbol	Power 3-input 0	K	Pron	agation	Delay	Parame+	er	3
Cell Symbol		t.	up	agation	td		61	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.72	0.07	1.47	0.05	0.07	8	A → X
					Ì		İ	
A1	A						Ì	
A2	<del>                                     </del>							
АЗ	$\forall$							
							1	
		Parame	ter	L	<u> </u>	T S	ymbol	Typ(ns)*
		102000					J	1 -3, -3, -3
						-		
	Input Loading	-						
Pin Name	Factor (lu)							
A	1							
	]							
-		l						
	Output Driving	{						
Pin Name	Factor (lu)							
X	36					į		
		* Mini	mum val	ues for	the ty	pical c	perati	ing condition.
		The	values	for the	worst	case or	eratir	ng condition
		are	given b	y the m	naximum	delay n	ultip	lier.
ľ								
AU-R3P-E2	Shoot 1/1							Page 5-2
I AUTADETLA	Dueel 1/1							I FARE J-4

בווזדפוו כ	MOS CATE APPAY II	NIT CEL	T CDECT	ETCATIO	NI.		111/4	U" Version			
Cell Name											
		D									
R4P Cell Symbol	Power 4-input 0	K .	Prop	agation	Delay 1	Paramete		3			
GCII Dymbol			up		td	n					
		t0	KCL	t0	KCL	KCL2 0.08	CDR2	Path A → X			
		0.72	0.07	2.02	0.06	0.08	8	$A \rightarrow X$			
						1					
A1	$\rightarrow$					1					
A2 —											
A3	x										
A4	$\forall$										
		Parame	ter	Ll			ymbol	Typ(ns)*			
		Tarame					,	1,10(113)			
						1					
Pin Name	Input Loading Factor (lu)										
A	1										
		ł				ļ					
	Output Driving					į					
Pin Name X	Factor (lu)										
^	36										
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.			
		The	values	for the	worst aximum	case op	erati	ng condition			
	1	are	given b	y the m	axımum	delay m	штетр	iiei.			
Ì											
1											
								:			
1											
AU-R4P-E2	Sheet 1/1							Page 5-3			



## **EXNOR/EXOR Family**

Page	Unit Cell Name	Function	Basic Cells
2–57	X1N	Exclusive NOR	3
2–58	X1B	Power Exclusive NOR	4
2–59	X2N	Exclusive OR	3
2-60	X2B	Power Exclusive OR	4
2-61	X3N	3-input Exclusive NOR	5
2-62	хзв	Power 3-input Exclusive NOR	6
2-63	X4N	3-input Exclusive OR	5
2-64	X4B	Power 3-input Exclusive OR	6

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	J" Version
Cell Name	Function							Number of BC
X1N	Exclusive NOR							3
Cell Symbol		t	Prop.	agation	Delay td		er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.93	0.23	0.77	0.11	0.13	4	$A \rightarrow X$
A1	÷				ĺ			
A2	_,0 х							
		Parame	ter			S	ymbol	Typ(ns)*
						1		
						1		
	Input Loading							
Pin Name A	Factor (lu)							
'n								
D: N	Output Driving							
Pin Name X	Factor (lu)							
		* W - 1	1		.1			: 1:+:
		" mini The	mum vai values	ues for for the	worst	case or	perati erati:	ing condition. ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
Equivalent	Circuit							
A1								
A2 -		_						
		<u>}</u>	— x					
AU-X1N-E2 S	Sheet 1/1							Page 6-1

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	"AU	
Cell Name	Function							Number of BC
X1B	Power Exclusive	NOR						4
Cell Symbol			Prop up	agation	Delay td		er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.19	0.07	1.42	0.04	0.07	7	A → X
A1 A2	x							
AZ T								
								T ( ) **
		Parame	ter				ymbol	Typ(ns)*
<del> </del>	Input Loading							
Pin Name	Factor (lu)							
A	2					1		
D: 11	Output Driving							
Pin Name X	Factor (lu)							
		o Ma_a	1		*			
		The	values	for the	worst	case op	eratir	ing condition.  ng condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
Equivalent	Circuit							
A1	<b></b>							
A2		7 1	\ <u></u>					
		= $$	<u> </u>	X				
AU-X1B-E2 S	Sheet 1/1							Page 6-2

וופדוווד ו	MOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		Ι"Δ1	U" Version
	Function	ОПП	L OIHOI.	. 10.1110				Number of BC
X2N	Exclusive OR							3
Cell Symbol	DACIUSIVE ON		Prop	agation	Delay	Paramet	er l	J
			up		td	n		
		t0 0.89	KCL 0.23	t0 0.94	KCL 0.11	KCL2 0.13	CDR2	Path A → X
A1 ———	$\rightarrow$							
A2	x							
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
A	2							
	Output Driving							
Pin Name	Factor (lu)							
X	14			-,				
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		are	values given b	for the	worst	case op delav m	perati nultip	ng condition lier.
		<u> </u>						
Equivalent	Circuit							
A1 A2	Þ———							
		P						
			— X					
AU-X2N-E2	Sheet 1/1							Page 6-3

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		"AU"	Version	n.
	Function	0111	. 01101	. 10//11/0	. 1			Number of	F BC
							<del>-  </del>		
X2B	Power Exclusive	OR						4	
Cell Symbol				agation	Delay	Paramet	er	·	
			up VCI	+0	td	n KCL2	CDP2	P.+.	
		t0 1.15	0.07	t0 1.31	0.04	0.06	CDR2	Path A → 1	
		1.15	0.07	1.31	0.04	0.00	,	A 7 4	•
A1 —	A								
A2	x				:			ļ	
		Parame	ter		L		ymbol	Typ(n:	5)%
		rarame	-C-1		·····		J001	1 yp(11:	<i>-</i> ) ·
	Input Loading								
Pin Name	Factor (lu)								
A	2								
		1							
	Output Driving								
Pin Name	Factor (lu)								
X	36								
		* Mini	mum val	ues for	the ty	pical o	perati	ng condi	tion.
								g condit	ion
		are	given b	y the m	axımum	иетау п	uitipl:	ier.	
Equivalen	t Circuit								
A1 -	b								
A2 -									
		b	>	X					
]									
1									
AU-X2B-E2	Sheet 1/1							Page	6-4
NO VED DE	DIIGED 1/1							1,486	

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		l "AU	" Vers	ion
Cell Name	Function							Number	of BC
X3N	3-input Exclusi	ve NOR						5	
Cell Symbol			Prop	agation	Delay	Paramet	er		
		t0	up KCL	t0	td KCL	n KCL2	CDR2	- Pat	h
		2.18	0.23	1.86	0.11	0.13	4	Pat A →	X
:									
A1	$\rightarrow$								
A2	х								
A3 ———	J								
		<u> </u>	<u> </u>				L., .,	- T	\
		Parame	ter			-   S	ymbol	Typ(	ns)"
1									
]									
Pin Name	Input Loading Factor (lu)								
A	2	1							
1						1			
		1							
Pin Name	Output Driving Factor (lu)	1				ļ			
X	18								
		* **			41- 4				
		The	mum vai values	for the	worst	case op	eratin	ng cond g condi	tion.
		are	given b	y the m	aximum	delay m	ultipl	ier.	
Equivalent	Circuit								
A2									
A3	]								
	₩ х								
A1	<del>"</del>								
	-								
AU-X3N-E2 S	Sheet 1/1							Page	6-5
MO NOW - DZ   C	JILCE L 1 / 1							11986	<u> </u>

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	J" Vers: Number o	ion
			- NOD						
X3B Cell Symbol	Power 3-input E	xclusiv	e NOK Prop	agation	Delay	Paramet	er	6	
		t0 t	up KCL	t0	td KCL	n KCL2	CDR2	Pati	
		2.11	0.07	2.71	0.04	0.07	7	Patl   A →	
	_								
A1	<b>_</b> "								
A2 —	x								
		Parame	ter			S	ymbol	Typ(1	ns)*
	T					1			
Pin Name	Input Loading Factor (lu)							}	
A	2					Ì			
						ł			
	Output Driving					Ì			
Pin Name X	Factor (lu)								
^	36								
		* Mini	mum val	ues for	the ty	pical c	perati	ing cond	ition.
		are	varues given b	for the y the m	worst	case op delay m	eratir ultipl	ng condí <sup>.</sup> lier.	tion
Fauturalan	t Circuit								
Equivalen	t Circuit								
A2 ————————————————————————————————————	<del></del>								
''		х							
A1									
AU-X3B-E2	Sheet 1/1							Page	6_4
AU-AJB-EZ	Dueer 1/1							rage	6-6

FUJITSU CI	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	Version
	Function							Number of BC
							1	
X4N	3-input Exclusi	ve OR						5
Cell Symbol				agation			er	T
		t0	up KCL	t0	KCL KCL	KCL2	CDR2	Path
		2.26	0.23	2.03	0.11	0.13	4	A + X
		2.20	0.23	2.03	0.11	0.13	•	
				1				1
A1 -	7							
A2	x							
A3 — 1	┦ .			ļ				
		Parame	ter			S	ymbol	Typ(ns)*
		i						
						1		
						İ		
						1		1
	Input Loading							
Pin Name	Factor (lu)							
A	2							
.,	-							
						İ		
						ĺ		
	Output Driving							
Pin Name	Factor (lu)					1		
X	14							
		* Mini	mum val	ues for	the ty	pical o	perati:	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
P	C::							
Equivalent	Circuit							
10								
A2								
A3								
	Щ							
	X							
A1								
AU-X4N-E2 S	heet 1/1							Page 6-7

FUJITSU C	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU"	
Cell Name	Function						1	Number of BC
X4B	Power 3-input E	xclusiv	e OR				1	6
Cell Symbol			Prop	agation			er	
		t0	up KCL	t0	KCL	n KCL2	CDR2	Path
		1.98	0.07	2.51	0.04	0.06	7	A + X
							l	
							ļ	
1 42	$\rightarrow$							
A1 A2	x							
A3 ———	$\frac{1}{2}$					ĺ		
							1	1
1		Parame	ter			S	ymbol	Typ(ns)*
						}		
	Input Loading	{						
Pin Name	Factor (lu)							
A	2	}						
-	Output Driving							
Pin Name	Factor (lu)							
X	36							<u> </u>
		* Mini	mum val	ues for	the tw	mical c	nerati	ng condition
		The	values	for the	worst	case or	erating	g condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultipl:	ier.
Equivalent	t Circuit							
A2 ————————————————————————————————————								
A3	<del></del>							
		X						
A1								
AU-X4B-E2	Sheet 1/1							Page 6-8

## **AND-OR-Inverter Family**

Page	Unit Cell Name	Function	Basic Cells
2–67	D23	2-wide 2-AND 3-input AOI	2
2-68	D14	2-wide 3-AND 4-input AOI	2
2-69	D24	2-wide 2-AND 4-input AOI	2
2-70	D34	3-wide 2-AND 4-input AOI	2
2–71	D36	3-wide 2-AND 6-input AOI	3
2-72	D44	2-wide 2-OR 2-AND 4-input AOI	2

בוווזדפון כ	MOS GATE ARRAY U	NIT CELL	SPECI	FICATIO	N		l "AU	" Version
	Function	NII ODD	D DILOI.	FICATIO	<u> </u>			Number of BC
700	0 11 0 11 0		~~					
D23 Cell Symbol	2-wide 2-AND 3-	input A	Prop	agation	Delay	Paramet		2
Cell Symbol		tı	up	agation	td		e1	T
		t0	KCL	t0	KCL	KCL2	LD2	Path
		0.59	0.23	0.55	0.11			A -> X
		0.30	0.18	0.30	0.07	0.10	4	B → X
A1	7							
A2	х							
ь								
	i	Parame	ter			S	ymbol	Typ(ns)*
						1		
	Input Loading							
Pin Name	Factor (lu)							
A B	1 1	}				1		
В	1							
						-		
	Output Driving							
Pin Name	Factor (lu)					l		
X	14							1
		& Mini	mum 1721	ues for	the tw	mical o	norati	ng condition.
		The	walues	for the	worst	case op	eratir	ng condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
								İ
AU-D23-E2 S	Sheet 1/1							Page 7-1

FUJITSU C	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	Ŋ		"A	U" Version
Cell Name	Function							Number of BC
D14	2-wide 3-AND 4-	innu+ A	OΤ					2
Cell Symbol	2-wide 3-AND 4-	Input A	Prop	agation	Delav	Paramet	er	14
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.72	0.23	0.56	0.15	0.17	4	A → X
		0.26	0.16	0.29	0.07	0.10	4	B → X
A1 -								
A2				ļ				
A3 —								
	x							
В								
1		Parame	ter			S	ymbol	Typ(ns)*
							*	
		[						
		]						
		İ						
		1						
	Input Loading	1				-		
Pin Name	Factor (lu)	1				- 1		
A B	1	l						
	1	l				İ		
		1				1		
Pin Nama	Output Driving							
Pin Name X	Factor (lu)	}						
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
	1	are	given b	y the m	axımum	delay m	uıtı	olier.
1								
AU-D14-E2	Sheet 1/1							Page 7-2
110 DI4 BZ	011060 1/1							11450 / 4

Number of BC   Propagation	FUJITSU C	MOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N		"AU	" Version
D24	Cell Name	Function		<u> </u>	1011110				Number of BC
Propagation Delay Parameter   To   KUL   To   KUL   To   KUL   To   Name   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   Factor (gu)   To   Name   To   Name   Factor (gu)   To   Name   To   Na			innut i	) T					
Tup to KCL to KCL CDR2 Path  0.43 0.18 0.50 0.11 RCL2 CDR2 Path  0.54 0.18 0.67 0.11 RA + X  B1	Cell Symbol	Z-Wide Z-AND 4-	input A	Prop	agation	Delay	Paramet	er	2
Pin Name Input Loading Factor (£u)  A 1 1  B 1 1  Whinimum values for the typical operating condition. The values for the maximum delay multiplier.	0011 0,		tı		-8001011	td	n		T
Parameter    Parameter   Symbol   Typ(ns)*	ļ		t0	KCL			KCL2	CDR2	
Pin Name   Input Loading   Factor (£u)    A									
Pin Name   Input Loading   Factor (£u)    Pin Name   Output Driving   Factor (£u)    X			0.54	0.18	0.67	0.11			$B \rightarrow X$
Pin Name   Input Loading   Factor (£u)    Pin Name   Output Driving   Factor (£u)    X					ĺ				
Pin Name   Input Loading   Factor (£u)    Pin Name   Output Driving   Factor (£u)    X			1						
Pin Name   Input Loading   Factor (£u)    Pin Name   Output Driving   Factor (£u)    X	_				- 1				
Pin Name   Input Loading   Factor (£u)   A									
Pin Name   Input Loading   Factor (£u)   A	A2	LA	i						
Pin Name   Input Loading   Factor (2u)	B1 —	, ×	l l						
Pin Name   Input Loading   Factor (£u)   A		_							1
Pin Name   Input Loading   Factor (£u)   A									
Pin Name   Input Loading   Factor (&u)   A	1		Parame	ter			S	ymbol	Typ(ns)*
Pin Name Factor (£u)  A 1 B 0 1  Pin Name Factor (£u)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (£u)  A 1 B 0 1  Pin Name Factor (£u)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (£u)  A 1 B 0 1  Pin Name Factor (£u)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (£u)  A 1 B 0 1  Pin Name Factor (£u)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (£u)  A 1 B 0 1  Pin Name Factor (£u)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							-		
A 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Pin Name						}		
Pin Name Factor (2u)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (Lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	В	1							
Pin Name Factor (Lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (Lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.		Output Driving	1						
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.							- 1		
The values for the worst case operating condition are given by the maximum delay multiplier.	X	14							
The values for the worst case operating condition are given by the maximum delay multiplier.			* Mini	mum val	ues for	the tv	pical c	perati	ng condition.
			The '	values	for the	worst	case op	eratir	ng condition
AU-D24-E2   Sheet 1/1			are	given b	y the m	aximum	delay m	ultipl	ier.
AU-D24-E2   Sheet 1/1									
AU-D24-E2   Sheet 1/1									
AU-D24-E2   Sheet 1/1									
AU-D24-E2   Sheet 1/1									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3	1								
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
AU-D24-E2   Sheet 1/1   Page 7-3									
1	AU-D24-E2 S	heet 1/1							Page 7-3

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
D34	3-wide 2-AND 4-	input A	OI					2
Cell Symbol			Prop	agation			er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.33	0.59	0.12	0 10	4	A → X
		0.50	0.28	0.35	0.07	0.10	4	B → X
		1 1						
A1								
A2 —								
	Th	1						
B1 B2	x							
BZ								
		]						
		Parame	ter			S	ymbol	Typ(ns)*
İ								
						l		
		[						
		l						
		[						
	Input Loading	i				l		
Pin Name	Factor (lu)							
A	1	]				İ		
В	1	l						
	Output Driving	1						
Pin Name	Factor (lu)	1						
X	10	i						
l		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the y the m	worst	case op	erati	ng condition
	L	are	given b	y the m	axillull	четау п	uitip	1161.
1								
1								
}								
1								
1								
1								
AU-D34-E2   S	Sheet 1/1							Page 7-/-
AU-D34-E2   S	Sheet 1/1							Page 7-4

FUJITSU C	MOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N		"AU	" Version
Cell Name	Function							Number of BC
D36	3-wide 2-AND 6-	input AC	Ι					3
Cell Symbol				agation	Delay		er	
		t0	KCL KCL	t0	td KCL	n KCL2	CDR2	Path
		0.62	0.23	0.58	0.11			A → X
		0.79	0.23	0.70 0.82	0.11	!		$\begin{array}{ccc} B \rightarrow X \\ C \rightarrow X \end{array}$
		0.7		0.02	0.111			
A1		l				!		
A2 —				Ì				
В1 —	<u>Б</u> .,			Ì				
B2 —	×							
C1 -				ļ				
C2				ļ				
		Paramet	ter			S	ymbol	Typ(ns)*
D: N	Input Loading							
Pin Name A	Factor (lu)							
В	1							
С	1							
Pin Name	Output Driving Factor (lu)							
X	10							
		* Minir	mum val	ues for	the tv	mical c	nerati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
AU-D36-E2 S	heet 1/1							Page 7-5

EUITTEU C	TMOC CATE ADDAY I	NITT CET	T CDECT	DICATIO	NT		7 11 11 1	U" Version
Cell Name	MOS GATE ARRAY U Function	NII CEL	L SPECI	FICATIO	in .		A	Number of BC
7								
D44	2-wide 2-OR 2-A	ND 4-in	put AOI					2
Cell Symbol				agation			er	
		t	up		td		anna	┥ 、, ,
		t0 0.83	KCL 0.33	t0 0.63	KCL 0.11	KCL2	CDR2	Path A → X
		0.83	0.33	0.51	0.11			$B \rightarrow X$
		0.79	0.23	0.39	0.07	0.09	4	$C \rightarrow X$
		)						
r								
A1 A2	7							
В —								
c	р— x							
								1
								Ì
							L.,.,	
		Parame	ter			-   S	ymbol	Typ(ns)*
		]						
		l						
		l				-		
	<b></b>	1				1		
Dim Nama	Input Loading					1		
Pin Name A	Factor (lu)	1				1		
В	1					)		
C	ī					Ì		
Din Nama	Output Driving							
Pin Name X	Factor (lu)	-						
,	10							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
}		The	values	for the	worst	case op	erati	ng condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultip	olier.
1								
1								
1								
AU-D44-E2	Sheet 1/1							Page 7-6

## **OR-AND-Inverter Family**

Page	Unit Cell Name	Function	Basic Cells
2–75	G23	2-wide 2-OR 3-input OAI	2
2-76	G14	2-wide 3-OR 4-input OAI	2
2–77	G24	2-wide 2-OR 4-input OAI	2
2-78	G34	3-wide 2-OR 4-input OAI	2
2-79	G44	2-wide 2-AND 2-OR 4-input OAI	2

Number of BC   C23   2-wide 2-OR 3-input OAI   2	FUJITSU CMOS GATE ARR	AY UNIT CEI	L SPECI	FICATIO	N		"AU"	Version
Propagation Delay Parameter   tdn	Cell Name   Function			1 1011110				
Propagation Delay Parameter   tdn	C22 2-114- 2 OF	2-innut 0	. T					2
Tup	Cell Symbol	3-input OF	Prop	agation	Delay	Paramet	er	2
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		t	up		td	n ·		
A1 A2 B  Parameter  Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Parameter  Parameter  Parameter  Symbol Typ(ns)*  Typ(ns)*  A						KCL2	CDR2	Path
Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (fu)  A							Ī	
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A		0.23	0.13	0.44	0.11			D 7 A
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A								
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A								]
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A	_	]						
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Pin Name Factor (Lu)  A								
Parameter Symbol Typ(ns)*  Pin Name Factor (Lu) A 1 B 1  Pin Name Factor (Lu) X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition		x						
Pin Name   Input Loading Factor (Lu)   A	В							
Pin Name   Input Loading Factor (Lu)   A								
Pin Name   Input Loading Factor (Lu)   A								
Pin Name   Input Loading Factor (Lu)   A		Parame	eter	L	l	1 8	ymbol	Typ(ns)*
Pin Name Factor (Lu)  A 1 B 1  Output Driving Factor (Lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition								
Pin Name Factor (Lu)  A 1 B 1  Output Driving Factor (Lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition								
Pin Name Factor (Lu)  A 1 B 1  Output Driving Factor (Lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition								
Pin Name Factor (Lu)  A 1 B 1  Output Driving Factor (Lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition								
Pin Name Factor (Lu)  A 1 B 1  Output Driving Factor (Lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition								
A B 1 B Output Driving Fin Name X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition	Input Loadi	.ng						J
B 1  Output Driving Factor (lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition								
Pin Name Factor (lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition								
Pin Name Factor (Lu) X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition	1							
Pin Name Factor (Lu) X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition								
Pin Name Factor (Lu) X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition								
X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition	Pin Name Factor (11)	'ing						
The values for the worst case operating condition	X 18							
The values for the worst case operating condition								_
are given by the maximum delay multiplier.		* Min:	imum val	ues for	the ty	pical c	peratir	ng condition.
The state of the s		are	values	ror the m	worst	case or delav m	erating multipli	s condition
			811011	<i>y</i> 0110 11	TO AT 2 III OIII	uoruj	.uzuzpzz	
								·
AU-G23-E2   Sheet 1/1   Page 8-1	AU-G23-E2 Sheet 1/1							Page 8-1

FULLTSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	" Version
Cell Name	Function	3111 000	D DI DOI	TIONITO				Number of BC
			-					
G14 Cell Symbol	2-wide 3-OR 4-i	nput OA	Prop	agation	Dolay	Daramat		2
Cell Bymbol		t	up	agation	t.d	n	<u> </u>	T
į		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.96	0.34	0.52	0.11			A → X
		0.20	0.13	0.52	0.11			. B → X
A1								
A2	_							
A3 —								
	у — х							
В	—U "							
					!			
		Parame	ter				ymbol	Typ(ns)*
		Tarane			,		,UI	135(113).
		Į.				-		
						-		
	Input Loading	1						
Pin Name	Factor (lu)	<u> </u>						
A	1							
В	1							
	ļ							
	Output Driving							
Pin Name X	Factor (lu)	4						
^	10							
		* Mini	mum val	ues for	the ty	pical c	perati	ing condition.
		The	values	for the	worst	case or	erati	ng condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultip	lier.
1								
1								
AU-G14-E2   S	Sheet 1/1							Page 8-2
								1

FUJITSU C	MOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N		"AU	
Cell Name	Function							Number of BC
G24	2-wide 2-OR 4-i	nput OAl	[					2
Cell Symbol			Prop	agation	Delay		er	
		to to	ip KCL	t0	td KCL	n KCL2	CDR2	Path
		0.40	0.23	0.56	0.11	KOBZ	CDRZ	A + X
		0.72	0.23	0.48	0.11			B → X
_							İ	
A1 A2	7~							
A2 D	」 > x							
B1 -								
B2 —								
		Paramet	er			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name A	Factor (lu)							
- B	1							
	Output Driving							
Pin Name X	Factor (lu)							
^	10							1
		* Minir	num val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst aximum	case or	eratin wltinl	g condition
		are	given b	y the n	IAXIIIUIII	delay n	uicipi	iei.
AII-CO/ FO I C	heat 1/1							D 9 2
AU-G24-E2 S	heet 1/1							Page 8-3

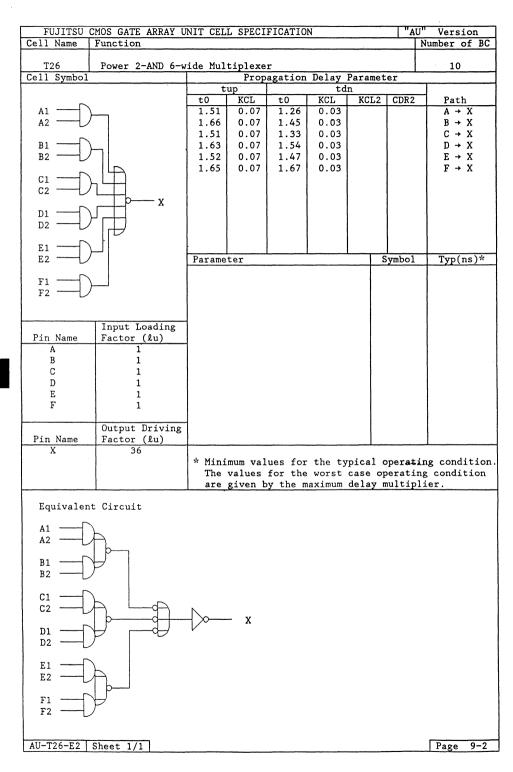
FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	V V		JA"	J" Version	
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "A Cell Name   Function							Number of BC		
G34	3-wide 2-OR 4-i	input OAI						2	
Cell Symbol	Symbol Propagation Delay Parameter tup tdn								
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		0.76	0.23	0.56	0.15			A + X	
		0.56	0.15	0.36	0.13			$B \rightarrow X$	
A1 —							1		
A2 -	7_						1		
	47								
B1	р— х								
B2							1		
		l i					ļ		
				Ì					
		Parame	ter			S	ymbol	Typ(ns)*	
						1			
		ĺ							
		]							
Dia Mana	Input Loading								
Pin Name A	Factor (lu)	-				ĺ			
B	1							}	
	_								
		]							
Pin Name	Output Driving Factor (lu)								
X	10	1				1			
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.	
		The	values	for the	worst	case or	erati	ng condition	
		are	given b	y the m	axımum	delay m	ultip	lier.	
AU-G34-E2   S	Sheet 1/1							Page 8-4	

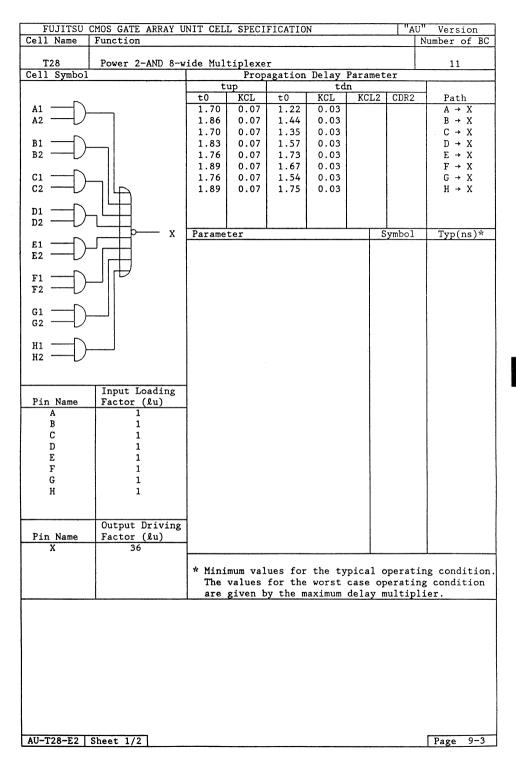
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version								
Cell Name Function								Number of BC
G44	2-wide 2-AND 2-OR 4-input OAI							2
Cell Symbol Propagation Delay Parameter tup tdn								T
	•	t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.59	0.23	0.69	0.15 0.15			$\begin{array}{c} A \rightarrow X \\ B \rightarrow X \end{array}$
		0.40	0.13	0.42	0.13			$C \rightarrow X$
A1 —	_							
A2	Dr			j				
B	□							
		Paramet	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
A B	1							
C	1					}		
	Output Driving							
Pin Name X	Factor (lu)							
^	14							
		* Minim	mum val	ues for	the ty	pical c	perat:	ing condition.
		The are	values given b	for the y the m	worst	case op delav m	erati: ultip	ng condition
	J	1 420	52.01. 2	<i>y</i> 0.10 1.1	<u> </u>	uoruj "	. штогр	
								ļ
AU-G44-E2   Sheet 1/1   Page 8-5								

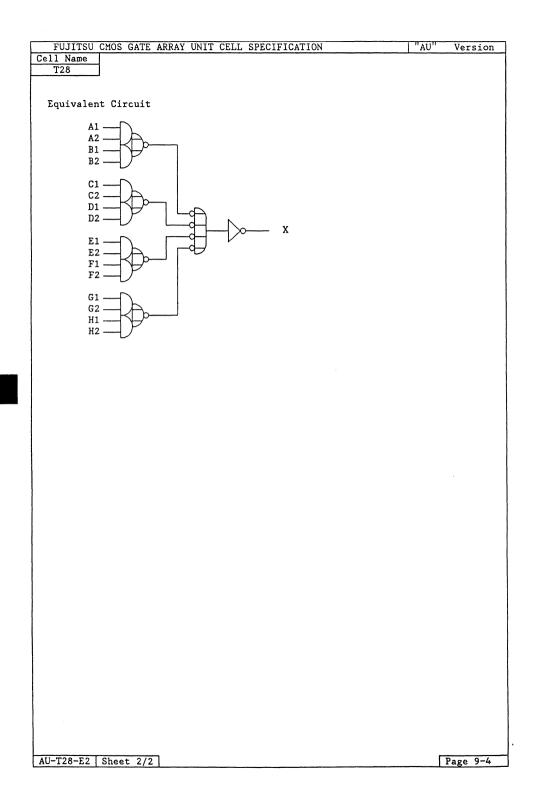
## **Multiplexer Family**

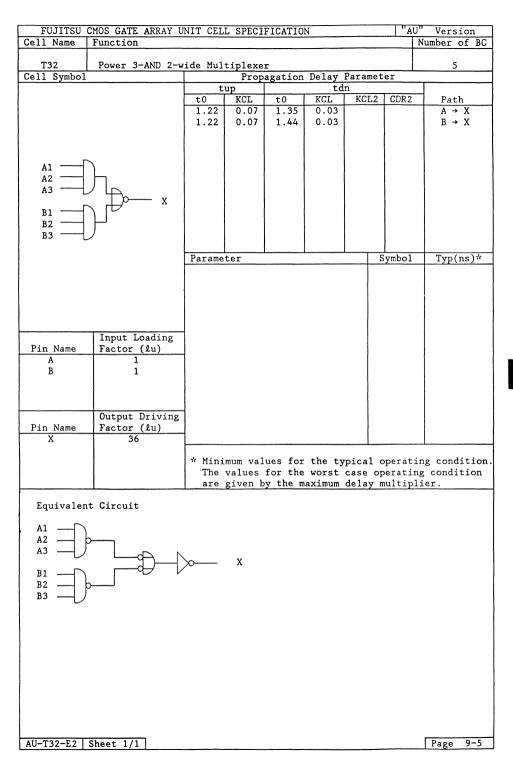
Page	Unit Cell Name	Function	Basic Cells
2-83	T24	Power 2-AND 4-wide Multiplexer	6
2–84	T26	Power 2-AND 6-wide Multiplexer	10
2–85	T28	Power 2-AND 8-wide Multiplexer	11
2–87	T32	Power 3-AND 2-wide Multiplexer	5
2–88	T33	Power 3-AND 3-wide Multiplexer	7
2–89	T34	Power 3-AND 4-wide Multiplexer	9
2–90	T42	Power 4-AND 2-wide Multiplexer	6
2–91	T43	Power 4-AND 3-wide Multiplexer	10
2-92	T44	Power 4-AND 4-wide Multiplexer	11
2-93	T54	Power 4–2–3–2 AND 4-wide Multiplexer	10
2-94	U24	Power 2-OR 4-wide Multiplexer	6
2–95	U26	Power 2-OR 6-wide Multiplexer	9
2–96	U28	Power 2-OR 8-wide Multiplexer	11
2–97	U32	Power 3-OR 2-wide Multiplexer	5
2–98	U33	Power 3-OR 3-wide Multiplexer	7
2–99	U34	Power 3-OR 4-wide Multiplexer	9
2-100	U42	Power 4-OR 2-wide Multiplexer	6
2-101	U43	Power 4-OR 3-wide Multiplexer	9
2-102	U44	Power 4-OR 4-wide Multiplexer	11

Name	PHILIPPH C	MOC CATT ADDAY II	NITT OF	CDECT	DIGATIO	,		1 11 4 1	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
T24									
Propagation Delay Parameter   Tup									
Tup									6
C									
1.44   0.07   1.41   0.03   C + X			t0	KCL			KCL2	CDR2	
1.27   0.07   1.31   0.03									
A1 A2 B1 B1 B2 C1 C2 D1 D2  Parameter  Symbol Typ(ns)*  Pin Name Factor (%u) A 1 B 1 C 1 D 1  Whinimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit A1 A2 B1 B2 C1 C1 C2 C1 C2 C1 C2 C1 C2 C1 C2 C1 C2 C1 C2 C1 C2 C1 C2 C2 C1 C2 C2 C3 C4 C4 C5 C5 C6 C7 C7 C8 C8 C8 C8 C8 C8 C8 C8 C8 C8 C8 C8 C8									
B1 B2 C1 C2 D1 D1 D2 Parameter  Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  A 1 B 1 C 1 D 1  Pin Name Factor (£u)  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit A1 A2 B1 B2 C1 C1 C2 D1 D2  X	A1 -	_			1				
Parameter    Symbol   Typ(ns)*	A2 —	'		ĺ					
Parameter    Symbol   Typ(ns)*	R1 —								
Pin Name   Input Loading   Pin Name   Factor (£u)   Parameter   Symbol   Typ(ns)*    A									
Pin Name Input Loading Factor (£u)  A	a:	x							
Pin Name   Input Loading   Factor (&u)   A		۲ <del>۱/</del> ۲							
Pin Name   Input Loading   Factor (£u)   A									
Pin Name   Input Loading   Factor (Ru)   A		ا ــــا	D				L		- m ( )
Pin Name Factor (lu)  A 1 B 1 C 1 D 1  Pin Name Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1 A2 B1 B2 C1 C1 C2 D1 D2  X	) DZ —		Parame	ter				ymbol	Typ(ns)*
Pin Name Factor (lu)  A 1 B 1 C 1 D 1  Pin Name Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1 A2 B1 B2 C1 C1 C2 D1 D2  X							1		
Pin Name Factor (lu)  A 1 B 1 C 1 D 1  Pin Name Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1 A2 B1 B2 C1 C1 C2 D1 D2  X									
Pin Name Factor (lu)  A 1 B 1 C 1 D 1  Pin Name Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1 A2 B1 B2 C1 C1 C2 D1 D2  X									
Pin Name Factor (lu)  A 1 B 1 C 1 D 1  Pin Name Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1 A2 B1 B2 C1 C1 C2 D1 D2  X									
A 1 B 1 C 1 D 1 D 1 Driving Pin Name Factor (&u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1 A2 B1 B2 C1 C2 D1 D2									
B 1 1 1 D 1 1 D 1 D 1 D 1 D 1 D 1 D 1 D		Factor (lu)							
Pin Name Factor (Au)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1		1					1		
Pin Name Factor (£u)  X  36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1  A2  B1  B2  C1  C2  D1  D2  * Minimum values for the typical operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the typical operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition. The values for the worst case operating condition.									
Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit A1 42 81 82 81	D	1							
Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit A1 42 81 82 81		Output Driving							
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1  A2  B1  B2  C1  C2  D1  D2		Factor (lu)							
The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1	X	36							
The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1			* Mini	mum val	ues for	the tv	pical o	perat:	ing condition.
Equivalent Circuit  A1 A2 B1 B2 C1 C2 D1 D2	The values for the worst case operating							ng condition	
A1 A2 B1 B2 X C1 C2 D1 D2			are	given b	y the m	aximum	delay m	ultip.	lier.
A1 A2 B1 B2 X C1 C2 D1 D2									
A2 B1 B2 C1 C2 D1 D2	Equivalent	Circuit							
B1 B2 C1 C2 D1 D2	A1								
D1 D2 X	A2 —	A							
D1 D2 X	R1								
C1 C2 D1 D2	1								
		x							
D1 D2									
D2 ——									
	D2	,							
AU-T24-E2   Sheet 1/1   Page 9-1	AU-T24-E2 S								

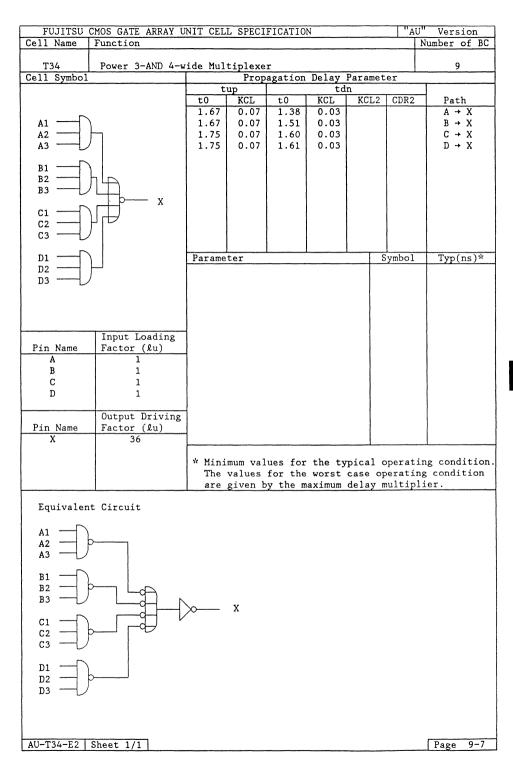


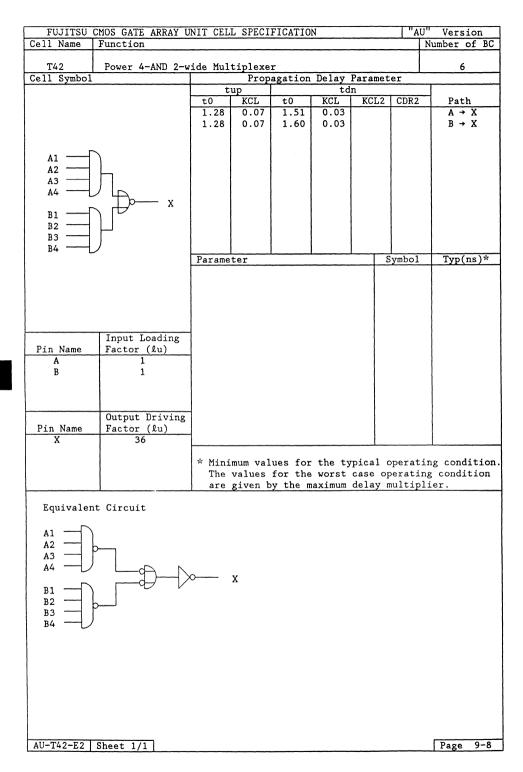


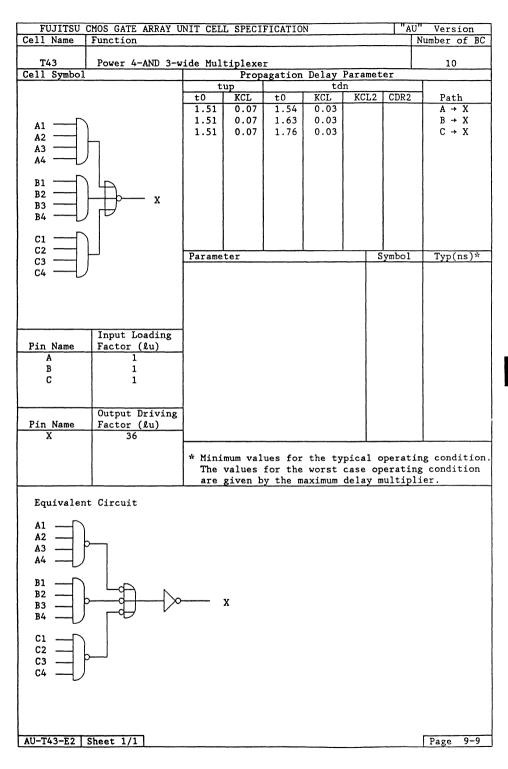


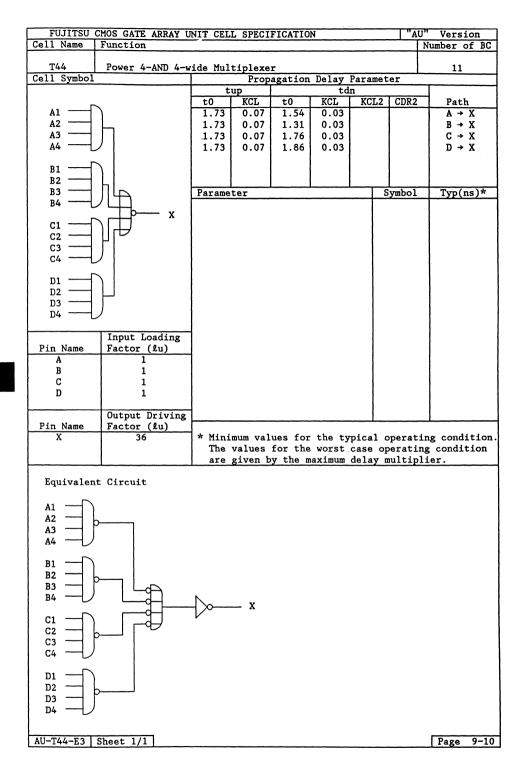


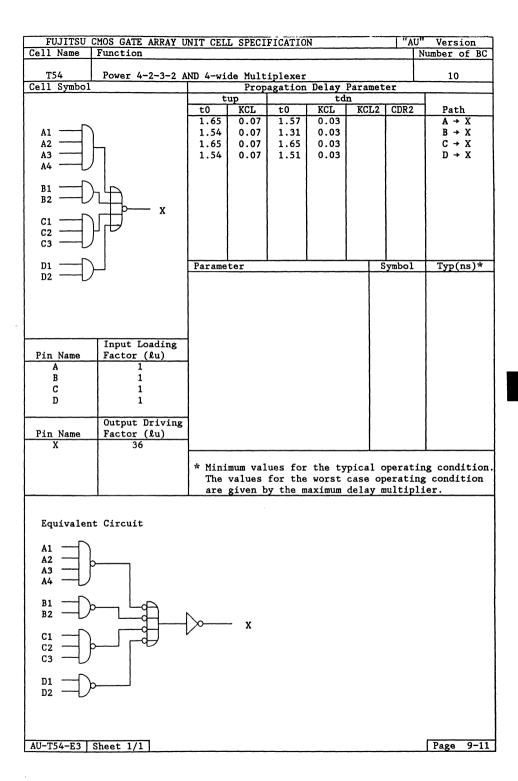
FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECT	FICATION	v v		l "Al	J" Version
Cell Name	Function	MIT OBB.	D DI BOI.	TIONTIO				Number of BC
1133	Dorrow 3 ANTO 2	M1					T	
T33 Cell Symbol	Power 3-AND 3-w	ide mul.	Prop	r agation	Delav	Paramet	er	7
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.40	0.07	1.33	0.03			$\begin{array}{c} A \rightarrow X \\ B \rightarrow X \end{array}$
		1.40	0.07	1.56	0.03			$C \rightarrow X$
A1 -								
A2 -	7				i			
A3 —								
B1	4							
B2	<del></del>							
B3								
C1 —								
C2	J							
C3 —		Parame	ter			S	ymbol	Typ(ns)*
l		ĺ				- 1		
l								
						-		
		ł				1		
	Input Loading							
Pin Name	Factor (lu)							
A	1	]						
B	1					1		
	1							
	Output Driving	1						
Pin Name X	Factor (lu)	ł						
^	36							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case op	erati:	ng condition
	1	are	given b	y the m	aximum	delay m	ultip	lier.
								<u></u>
AU-T33-E2   S	Sheet 1/1					·		Page 9-6





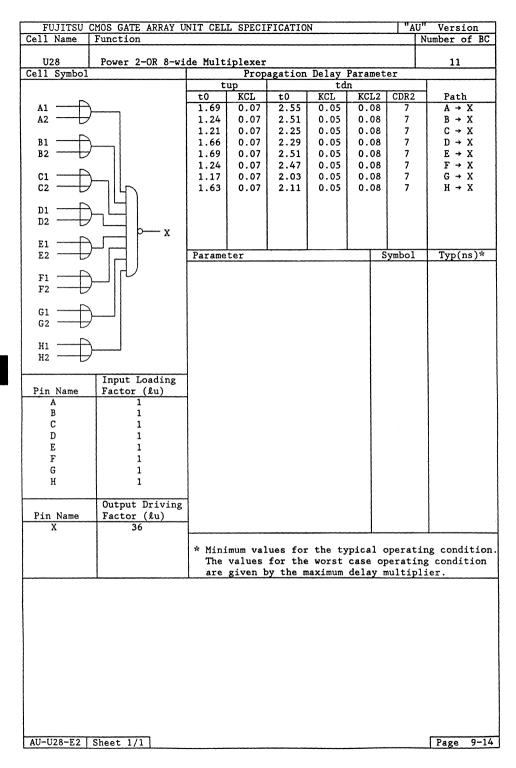






	CMOS GATE ARRAY U	NIT CELI	SPECI:	FICATIO	N		A	U" Version Number of BC
OCII Manie	r unccion							Hamber Of BC
U24	Power 2-OR 4-wi	de Mult:	<u>iplexe</u> r					6
Cell Symbol			Prop	agation			er	
		t0 t	IP KCL	t0	td KCL	n KCL2	CDR2	Path
		1.60	0.07	1.44	0.04	0.07	7	A + X
		1.15	0.07	1.40	0.04	0.07	7	$B \rightarrow X$
,,	_	1.52	0.07	1.43 1.36	0.04	0.07	7 7	$C \rightarrow X$
A1 A2		1.11	0.07	1.36	0.04	0.07		D + V
B1	7-17							
B2	′							
C1 —								
C2		ľ	'					
71 -		}						
D1 D2	)—	Paramet	ter			l s	ymbol	Typ(ns)*
						1		
						1		
						1		
	<b>.</b>							
Pin Name	Input Loading Factor (lu)					-		
A	1	1						
В	1					1		
C	1	ĺ						
D	1	İ						
	Output Driving					1		
Pin Name	Factor (lu)							
X	36							
		* Mini	num val	ues for	the tv	mical c	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
1								
111 1101 55								<u> </u>
AU-U24-E2	Sheet 1/1							Page 9-12

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version											
Cell Name	Function							Number of BC			
U26	Power 2-OR 6-wi	de Mult:						9			
Cell Symbol				agation	Delay		er				
		t0	up KCL	t0	td KCL	n KCL2	CDR2	Path			
A1 -		1.60	0.07	1.87	0.04	0.07	7	A + X			
A2		1.24	0.07	1.81 1.92	0.04	0.07	7	$\begin{array}{c c} B \to X \\ C \to X \end{array}$			
В1 ——		1.63	0.07	1.92	0.04	0.07	7	$D \rightarrow X$			
B2		1.31	0.07	2.07	0.04	0.07	7	E + X			
C1 —	147	1.68	0.07	2.07	0.04	0.07	7	F → X			
C2	ЦL										
D1 -	x										
D2											
E1 -											
E2	_	Parame	ter			S	ymbol	Typ(ns)*			
F1 —											
F2						Ì					
Pin Name	Input Loading Factor (lu)										
A	1										
B C	1 1					1					
D	1					1					
E	1										
F	1										
D. V	Output Driving										
Pin Name X	Factor (lu) 36					1					
		sh Mini				1					
								ng condition. g condition			
					aximum						
								ļ			
AII-1126-F2   C	AU-U26-E2   Sheet 1/1   Page 9-13										
NO 020-E2   3	neer 1/1							11456 7 13			



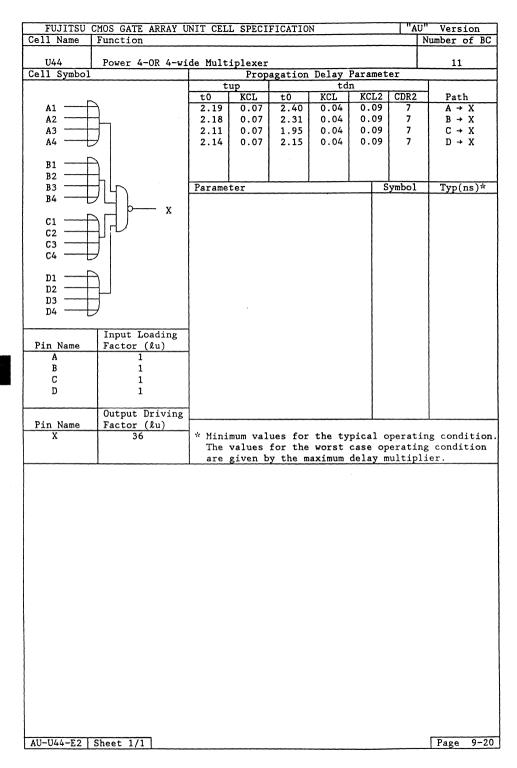
DUITMOU C	WOO OAME ARRAY !!	UTM ODT	. annar	n			1 11.	<del>,,, , , , , , , , , , , , , , , , , , </del>
	MOS GATE ARRAY U	NII CEL	L SPECI.	FICATIO	N		JA"	J" Version Number of BC
CEII Mame	runction							Mulliper Of BC
U32	Power 3-OR 2-wi	de Mult	iplexer					5
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.72	0.07	1.33	0.04	0.07	7	A → X
		1.69	0.07	1.31	0.04	0.07	7	B → X
A1								
A2								1
A3 -	[L							
_	ן >>— x							1
B1 —								
B2					}			1
B3 —								
								]
1		Parame	ter		I		ymbol	Typ(ns)*
		1				<del>-   -</del>		1-75(5)
1						1		
						ł		1
						ļ		1
	I 7					ł		
Pin Nama	Input Loading Factor (lu)					1		
Pin Name A	1							
В	1					1		
1 -	1							1
						1		1
						Ì		
	Output Driving	1						
Pin Name	Factor (lu)							
Х	36							
		w Mini	mm 1	use for	· +ha +	mical o	norat.	ing condition.
	[	The	mum vai valnes	for the	worst	case on	perati erati	ng condition
		are	given b	v the m	aximum	delay m	ultip:	lier.
	-L		8	-				
1								
1								
1								
								{
1								1
								l
1								ļ
								l
1								1
1								
1								
1								
1								
1								
AU-U32-E2	Sheet 1/1							Page 9-15

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	" Version
Cell Name	Function							Number of BC
U33	Power 3-OR 3-wi	de Mult	iplexer					7
Cell Symbol			Prop	agation			er	
		t0	up KCL	t0	td KCL	KCL2	CDR2	Path
1		1.83	0.07	1.83	0.04	0.09	7	A + X
		1.80 1.85	0.07 0.07	1.91 2.02	0.04	0.09	7	$\begin{array}{c} B \to X \\ C \to X \end{array}$
A1 -								
A2 A3	7							
B1 B2	—							
B3 -	T *							
C1								
C2								
C3 —		Parame	ter			S	ymbo1	Typ(ns)*
						İ		}
						9		
						}		
Pin Name	Input Loading Factor (lu)							
A	1							
B C	1							
	1							
								1
Pin Name	Output Driving Factor (lu)							
X	36							
		* Mini	mum val	ues for	the tv	pical c	perati	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip.	lier.
W 1100 Po 1								<u> </u>
AU-U33-E2   S	Sheet 1/1	·····						Page 9-16

FUJITSU CN	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	" Version	
Cell Name   I	Function							Number of E	3C
U34	Power 3-OR 4-wi	de Mult	inlever					9	
Cell Symbol	TOWEL J-OK 4-WI	ue muit	Prop	agation	Delay	Paramet	er	7	$\dashv$
-			up		td	n		Ι	
		t0 1.69	KCL 0.07	t0 2.39	KCL 0.05	0.08	CDR2	$\begin{array}{c c} & \text{Path} \\ \hline & A \rightarrow X \end{array}$	$\dashv$
_		1.71	0.07	2.40	0.05	0.08	7	$B \rightarrow X$	
A1 -		1.54	0.07	1.95	0.05	0.08	7	C → X	
A2 A3	7	1.69	0.07	2.15	0.05	0.08	7	$D \rightarrow X$	
AS C									
В1									
B2	147								
B3 —	☐								
C1 —									1
C2									
C3 —		Parame	ter		L		ymbol	Typ(ns)	-
D1 -		- arame					JUI	1,1,1,11,11	$\neg$
D2									l
D3 —									
		į							Ì
						1			
Di- N	Input Loading								ļ
Pin Name A	Factor (lu)					Ì			
В	ī							ĺ	
C	1								
D	1							1	
	Output Driving	1				1		l	
Pin Name	Factor (lu)					1			
X	36								$\dashv$
		* Mini	mum val	ues for	the ty	pical c	perati	ing condition	on.
		The	values	for the	worst	case op	eratir	ng condition	n
		are	given b	y the m	aximum	delay m	ultip	lier.	$\dashv$
									Ì
3									
									İ
AU-U34-E2   S	heet 1/1							Page 9-	17
007 112   0								1.000	لــــــــــــــــــــــــــــــــــــــ

FUJITSU C	MOS GATE ARRAY Function	UNIT CEL	L SPECI	FICATIO	N		"AU	" Versi Number o	ion of RC
									, , DO
U42 Cell Symbol	Power 4-OR 2-w	ide Mult	iplexer Prop	agation	Delay	Paramet	er	6	
			up		td	n		]	
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		2.08	0.07	1.37 1.31	0.04	0.07	7	A → B →	
		2.00	""	1.01			'		••
A1	4								
A2	_								
A3	1  _	Parame	ter			S	ymbol	Typ(r	ıs)*
A4 —	У х								
B1 -	1 [					-			
B2 B3	]								
B4 —	)								
						1			
						1			
	Input Loading	-							
Pin Name	Factor (lu)								
A	1								
В	1								
	Output Driving	_						ļ	
Pin Name	Factor (lu)	·							
Х	36	* Mini	mum val	ues for	the ty	pical c	perati	ng cond	ition
		The	values given b	for the	worst	case or	eratin ultipl	g condition	tion
	L	are	given b	y the n	IAXIIIIIII	deray ii	dicipi	101.	
1									
}									
AU-U42-E2 S	Sheet 1/1							Page	9-18

FUJITSU C	MOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	N		"A	U" Version
Cell Name	Function	NII CED	L BILCI.	I TORTTO	14			Number of BC
U43	Power 4-OR 3-wi	do W1+	inler-					9
Cell Symbol	rower 4-UK 3-WI	de Muit	Prop	agation	Delay	Paramet	er	9
			up		td	n		
		t0 2.06	KCL 0.07	t0 1.71	KCL 0.05	KCL2 0.07	CDR2	Path
		2.10	0.07	1.71	0.05	0.07	7	$B \rightarrow X$
A1 -	<i>†</i>	2.16	0.07	1.91	0.05	0.07	7	C → X
A2	<del></del>							
A3 A4	)							
B1	J 17	Parame	ter			S	ymbol	Typ(ns)*
B2 B3	}					ŀ		
B4	) p "							
C1 C2	]					ł		
C3						1		
C4 —	7					1		
						1		
Pin Name	Input Loading Factor (lu)					1		
A	1							
В	1					1		
С	1							
}								
	Output Driving	<b></b>						
Pin Name X	Factor (lu)	å Mini	mum val	ues for	the tw	nical c	norat	ing condition
-		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
1								
1								
}								
AU-U43-E2   S	Sheet 1/1							Page 9-19



## **Clock Buffer Family**

Page	Unit Cell Name	Function	Basic Cells
2-105	K1B	True Clock Buffer	2
2-106	K2B	Power Clock Buffer	3
2-107	кзв	Gated Clock (AND) Buffer	2
2-108	K4B	Gated Clock (OR) Buffer	2
2-109	K5B	Gated Clock (NAND) Buffer	3
2-110	KAB	Block Clock (OR) Buffer	3
2-111	KBB	Block Clock (OR x 10) Buffer	30
2-113	KDB	Block Clock (OR x 10) Buffer	32
2-115	KEB	Block Clock Buffer	23

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
K1B	True Clock Buff	er						2
Cell Symbol		4.	Prop	agation	Delay	Paramet	er	
		t0	up KCL	t0	td KCL	n KCL2	CDR2	Path
		0.58	0.07	0.69	0.03			Path   A → X
					,			
	_							
Α	У х							
	V							
	:							
			ļ			L		
		Parame	ter			S	ymbol	Typ(ns)*
						- 1		
Din Nome	Input Loading							
Pin Name A	Factor (lu)					İ		
						1		
n	Output Driving							
Pin Name X	Factor (lu)							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		are	varues given b	for the m	worst	delav m	eratı ultip	ng condition
		·	<u></u>					
Equivale	nt Circuit							
A>	x							
	V							
1								
1								
AU-K1B-E2	Sheet 1/1							Page 10-1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
wan.	Danier (11- D (	£						•
K2B Cell Symbol	Power Clock Buf	ier	Pron	agation	Delay	Paramot		3
Cell Symbol	·	t	up	agacion	td		<u> </u>	-T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.85	0.03	0.96	0.03			Path A → X
							İ	
							1	
							İ	
							ļ	
							1	
Α	x						Ì	
•	<b>"</b>							
				'				
		Parame	ter				Symbol	Typ(ns)*
						1		
	Input Loading					1		
Pin Name	Factor (lu)							
A	1	Ì						
		1				1		
	Output Driving	İ				1		
Pin Name	Factor (lu)					1		
Х	Factor (lu) 55							
ļ			_		_			
		* Mini	mum val	ues for	the ty	pical o	operat	ing condition.
								ng condition
l		I are	Progn D	y cite ii	naximum	uciay i	"ar crb	1101.
Equivaler	nt Circuit							
	-							
I								
A>	x							
1								
1								
l								
1								
	•							
1								
AU-K2B-E2	Sheet 1/1							Page 10-2

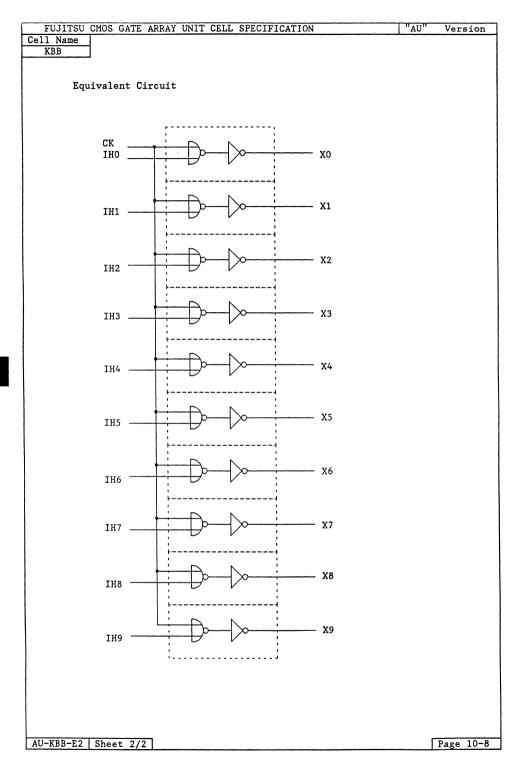
							111	m
FUJITSU C	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	" Version Number of BC
K3B Cell Symbol	Gated Clock (AN	D) Buff	er	agation	Delay	Paramo+	er	2
Sell Symbol		+	up	agacion	td	n aramet	<u> </u>	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.80	0.07	0.80	0.03			Path A → X
•								
					!			
							ŀ	
A1	\						l	
A2	)— x						į	
							l	
							•	
							1	
		Parame	ter			S	ymbol	Typ(ns)*
				***************************************	Tanada in Military			
						l		
								1
	Input Loading					1		
Pin Name	Factor (lu)					1		
A	1							
	_							
D:	Output Driving							
Pin Name X	Factor (lu)					1		1
^	36							.1
		* Mini	mum val	ues for	the tv	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratir	ng condition
		are	given b	y the m	aximum	delay n	ultipl	ier.
							-	
Equivalen	t Circuit							
A1	1							
A2 —	x ~							
1								
}								
ALL-Van Ea	Chast 1/1							Page 10-3
AU-K3B-E2	Sheet 1/1							rage 10-3

7,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,							7 11	.,,,
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			U" Version Number of BC
Cerr Mame	1 0110 0 1 011							TIGHINGI OT DC
K4B	Gated Clock (OR	) Buffe:	r					2
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t0	up KCL	t0	td KCL	KCL2	CDR2	Path
		0.63	0.07	0.91	0.04	0.06	8	A + X
								1
								1
A1	A							- {
A2	x							1
							L	
		Parame	ter			s	ymbol	Typ(ns)*
						į		
						1		
						İ		
<b> </b>	Input Loading					-		
Pin Name	Factor (lu)					ŀ		
A	1							
						1		
	Output Driving							
Pin Name	Factor (lu)							
Х	36							
		* Mini	ו פער מווח	nes for	the to	nical o	nerat	ing condition.
		The	walues	for the	worst	case or	erati	ng condition
	1.	are	given b	y the m	aximum	delay m	ultip	lier.
Fautralas	t Circuit							
Equivalen	COIICUIC							
A1 —								
A2 -	x —							
1								
1								
AU-K4B-E2	Sheet 1/1							Page 10-4

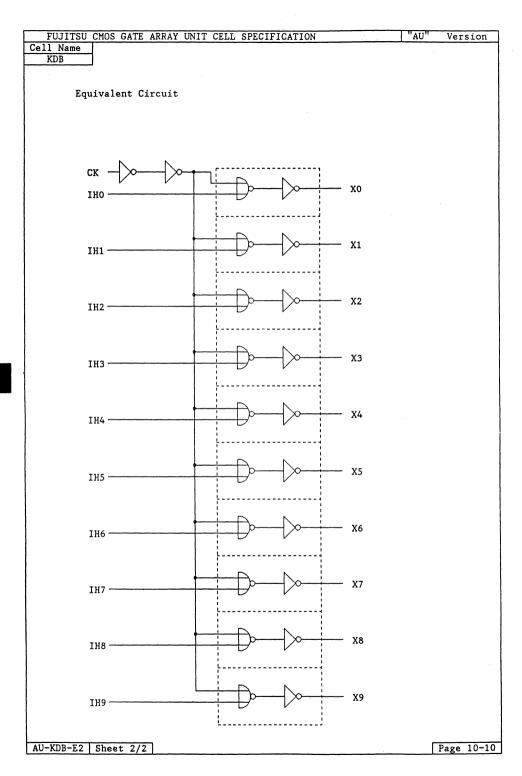
FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	" Version	
Cell Name									
								Number of BC	
K5B	Gated Clock (NA	ND) Buf	fer					3	
Cell Symbol				agation	Delay	Paramet	er		
		t0	up KCL	t0	KCL	n KCL2	CDR2	- Dath	
		0.91	0.07	1.19	0.03	ROLLZ	CDRZ	$\begin{array}{c c} Path \\ A \rightarrow X \end{array}$	
		0.51	0.07	1.17	0.05			^ ^	
								1	
A1	\							1	
A2	<i>р</i> — х								
								1	
		Parame	ter			T S	ymbol	Typ(ns)*	
		T d L d line					J01	13) (1.0)	
						1			
						1			
								1	
						İ			
		·				1			
D: 11	Input Loading								
Pin Name	Factor (lu)	ļ				1			
A	1	İ				l			
								1	
						1			
	Output Driving	1				1			
Pin Name	Factor (lu)								
Х	36							1	
			_	_			_		
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.	
	Ì	The	values	for the	worst	case op	eratin	g condition	
	L	are	given b	y the m	axımum	delay m	ultipi	ier.	
Equivalent	: Circuit								
nderagen									
A1	$\longrightarrow$ d $\longrightarrow$	— х						j	
A2 —	V V								
								ļ	
AU-K5B-E2 S	Sheet 1/1							Page 10-5	

FUJITSU ( Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		'A'	U" Version Number of BC
КАВ	Block Clock (OR	) Buffe	r					3
Cell Symbol			Prop	agation	Delay	Paramet	er	
	·		up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		0.87	0.03	1.48	0.03			A → X
								1
							1	
	_							
A1	x							
A2								
		Parame	ter			S	ymbol	Typ(ns)*
						1		
						1		
	Input Loading							
Pin Name	Factor (lu)							
A	1					l l		
						[		
						İ		
	Out Duly					1		]
Pin Nama	Output Driving Factor (lu)							
Pin Name X	55					İ		
'n	33							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
Equivalent	t Circuit							
Ì								
A1								
A2	x ~							
1								
	energy (March 1984) and the Company (March 1984)							
AU-KAB-E2	Sheet 1/1							Page 10-6

FUJITSU C	MOS GATE ARRAY U	NIT CELI	L SPECII	FICATIO	N		"AU	" Version
Cell Name	Function							Number of BC
KBB	Block Clock Buf	fer (OR	x 10)					30
Cell Symbol	DIOCK DIOCK DUI	101 (01.	Propa	agation	Delay	Paramet	er	
			р		td		appo	7,
		t0 1.07	KCL 0.03	t0 1.67	KCL 0.03	KCL2	CDR2	Path CK → X
		0.87	0.03	1.48	0.03		į	IH → X
		į	]	)				
ск —								
IHO —	xo	ĺ			ĺ			
IH1	X1	1						
IH2 IH3	X2 X3	l						
IH4	X4							
IH5	X5							
IH6 ————————————————————————————————————	X6 X7						Ì	
IH8	X8	Paramet	ter			S	ymbol	Typ(ns)*
IH9	Х9							
						- 1		
								1
	Input Loading							
Pin Name	Factor (lu)							
CK	10							
IH	1							
	Output Driving					ļ		
Pin Name	Factor (lu)							
X	55							
		* Minir	mum val	ues for	the tv	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
	1	are	given b	y the m	aximum	delay m	ultipl	ier.
								l
AU-KBB-E2 S	Sheet 1/2							Page 10-7
MU-NDB-EZ	oneer 1/2							rage 10-/



FULLTSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	J" Version
	Function	VII ODD	D DI DOI.	TORTIO				Number of BC
מתע	Pleak C11- P. C	· · · · · ·	10)					20
KDB Cell Symbol	Block Clock Buf	ter (OK	X IU)	agation	Delay	Paramet	er	32
ocii byanoti		t	up	agacion	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.90	0.04	2.80	0.02		l	CK → X
		0.90	0.04	1.85	0.02		İ	IH → X
ск —								
IHO —	X0						1	
IH1 ————————————————————————————————————	X1 X2							
IH3	— хз							
IH4	X4							
IH5 ——	X5 X6						}	
1H7 —	X7						ļ	
IH8	X8	Parame	ter			S	ymbol	Typ(ns)*
IH9	хэ					1		
						İ		
						1		
						İ		
	Input Loading							
Pin Name	Factor (lu)					- 1		
CK	1							
IH	1							
Din Nama	Output Driving							
Pin Name X	Factor (lu) 55							
		* Mini	mum val	ues for	the ty	pical c	perat:	ing condition.
		are	values given b	ior the m	aximum	delay m	peratio nultip	ng condition
	L		821011 2	<i>y</i> - 0.1.0 1.1.		dolay		
AU-KDB-E2 S	heet 1/2							Page 10-9



FUJITSU	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version										
Cell Name	Function Number of Bo										
KEB	Block Clock Buf	fer						23			
Cell Symbol			Prop	agation	Delay	Paramet	er				
			up		td						
		t0	KCL	t0	KCL	KCL2					
ск —	X0 X1 X1 X2 X3 X4 X5 X6 X6 X7	1.25	0.04	1.38	0.02	0.04	18				
Pin Name CK  Pin Name X	Input Loading Factor (lu)  6  Output Driving Factor (lu)  55										
		The		for the	worst	case or	erati	ing condition. Ing condition			

Note: The KEB is an equivalent of the KDB and the KBB, and it must be treated in the same manner as the KBB and the KDB in the logic circuit design.

AU-KEB-E2 | Sheet 1/2

Page 10-11

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version Cell Name KEB Equivalent Circuit X0 X1 X2 ХЗ X4 X5 X6 X7 X8 Х9 AU-KEB-E2 | Sheet 2/2 Page 10-12

## Scan Flip-flop (Positive Edge Type) Family

Page	Unit Cell Name	Function	Basic Cells
2-119	SDH	Scan 2-input D Flip-flop with Clear and Clock Inhibit	14
2-122	SDJ	Scan 4-input D Flip-flop with Clear and Clock Inhibit	15
2-125	SDK	Scan 6-input D Flip-flop with Clear and Clock Inhibit	16
2-128	SJH	Scan J-K Flip-flop with Clear and Clock Inhibit	16
2–131	SDD	Scan 2-input D Flip-flop with Clear, Preset, and Clock Inhibit	16
2-135	SDA	Scan 1-input D Flip-flop with Clock Inhibit	12
2-138	SDB	Scan 1-input 4-bit D Flip-flop with Clock Inhibit	42
2-142	SHA	Scan 1-input 8-bit D Flip-flop with Clock Inhibit	68
2–145	SHB	Scan 1-input 8-bit D Flip-flop with Clock Inhibit and Q Output	62
2–148	SHC	Scan 1-input 8-bit D Flip-flop with Clock Inhibit and XQ Output	62
2–151	SHJ	Scan 8-bit D Flip-flop with Clock Inhibit and 2-to-1 Data Multiplexer	78
2–154	SHK	Scan 8-bit D Flip-flop with Clock Inhibit and 3-to-1 Data Multiplexer	88
2–157	SFDM	Scan 1-input D Flip-flop with Clock Inhibit	10
2-160	SFDO	Scan 1-input D Flip-flop with Clear and Clock Inhibit	11
2–163	SFDP	Scan 1-input D Flip-flop with Clear, Preset, and Clock Inhibit	12
2-167	SFDR	Scan 4-input D Flip-flop with Clear and Clock Inhibit	36
2-171	SFDS	Scan 4-input D Flip-flop with Clock Inhibit	31
2-175	SFJD	Scan J-K Flip-flop with Clock Inhibit	14

Function								
<u>runetion</u>								Number of BC
SCAN 2-input DF	F with	Clear &	Clock-	Inhibit			1	14
	Propagation Delay Parameter							
	t							
	t0							Path
							7	CK, IH → Q
	1							CK, IH → X
	3.03	0.07	0.86	0.03	0.	07	7	CL → Q
	1	}						X
<u></u>								
		l						ł
b- vo								
م م	Parame	tor			L	5	vmho1	Typ(ns)*
<del>Q</del>								4.4
•								4.0
CL								
	Data Setup Time						tSD	3.0
	Data Hold Time						tHD	0.8
	Clear Pulse Width							4.0
								2.4
	Clear	Hold Ti	me				tINH	1.2
3						1		1
	1							l
1	1							
	1					1		}
	1							
	l					ĺ		
	1							
Output Driving	1							
						<b></b>		
36	* Mini	mum val	ues for	the tv	pica	1 0	perat	ing conditio
36								
	CL    Input Loading Factor (lu)  1	Clear   Clea	Prop   tup   t0   KCL   2.98   0.07   1.88   0.07   1.88   0.07   3.03   0.07     Clear Pulse W   Clock Pause T   Data Hold Tim   Clear Release   Input Loading Factor (lu)	Propagation  tup  t0 KCL t0  2.98 0.07 2.39  1.88 0.07 1.72  3.03 0.07 0.86   Parameter Clock Pulse Width Clock Pause Time  Data Setup Time Data Hold Time  Clear Pulse Width Clear Release Time  Clear Release Time  Clear Hold Time  Clear Hold Time  Output Driving Factor (lu)  Output Driving Factor (lu)  A Minimum values for The values for the	Propagation Delay   tup	Tup	Propagation Delay Paramet   tup	Propagation   Delay   Parameter

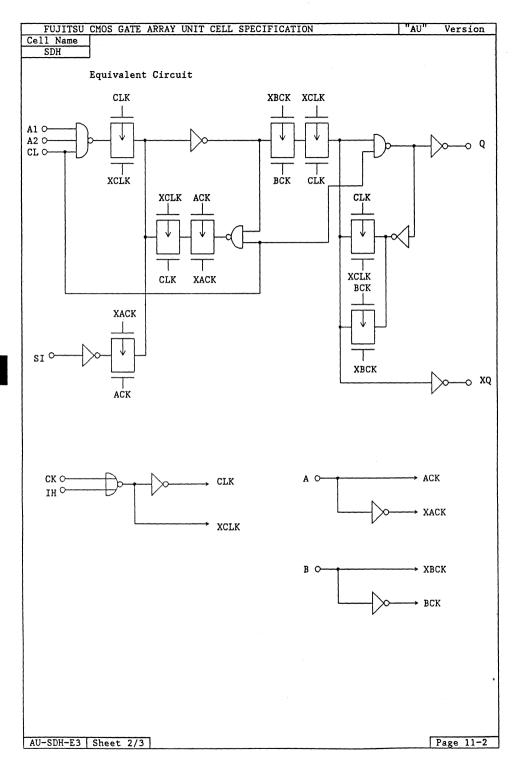
## Function Table

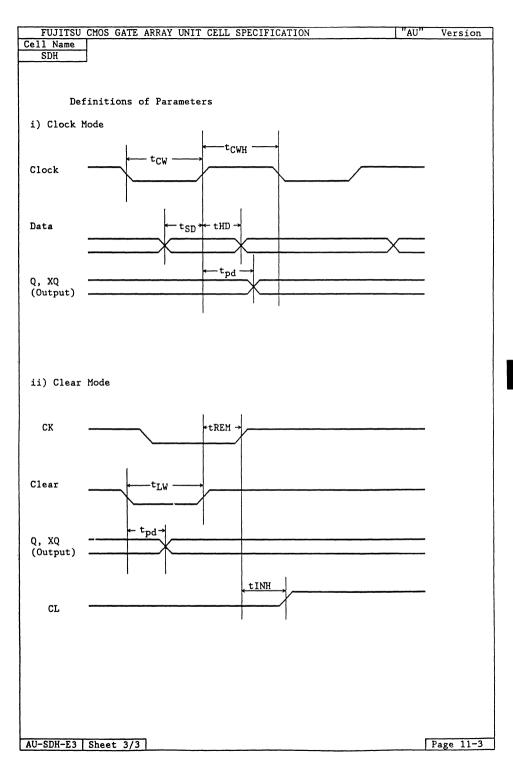
MODE		INPUT								
	CLK	CL	D	A	В	SI	Q	XQ		
CLEAR	Х	L	Х	Х	X	Х	L	н		
CLOCK	L→H	н	Dí	L	L	Х	Di	Di		
	Н	Н	Х	L	L	x	Q <sub>0</sub>	$XQ_0$		
SCAN	Н	Н	Х	L→H→L	Н	Si	Qo	XQο		
	Н	н	Х	L	н→∟→н	Х	Si	Si		

Note : CLK = CK + IH D = A1  $\times$  A2

AU-SDH-E3 | Sheet 1/3

Page 11-1





Col	FUJITSU		GATE A	RRAY U	NIT CEL	L SPEC	(FICATIO	ON			AU" Version Number of 1	
Cel	II Name	Func	11011								Number of i	ВС
	SDJ	SCA	N 4-in	put DF	F with	Clear 8	Clock-	-Inhibi	t		15	
Cel	ll Symbo	1					pagation	n Delay		neter		
į						up	l		dn Voi	O L CDD	<u> </u>	
					t0	KCL	t0 2.42	KCL 0.03	0.0		$\begin{array}{c c} \text{Path} \\ \text{CK,IH} \rightarrow 0 \end{array}$	
1					2.20	0.07	1.71		0.0		CK, IH → C	
	1				2.99	0.07	0.85	0.03	0.0		CL +	
	A1 -		Q		1 2.33	0.07	0.05	0.03	"		I	ΧQ
	A2 -	Ī				1	1	1	1			•
1	B1 -							1			1	
1	B2 -					1			1	ł	1	
l	ck —					1			1		ļ	
l	IH —							1		į		
1	sı —						l	1	1		ł	
1	Α		>− xQ		Parame	<u></u>	<u> </u>	Symbo	T ()			
1	В —		~ AQ			Pulse V	didth.			tCW	1 Typ(ns):	
1	,	<u> </u>				Pause '				tCWH	4.0	
1		CL										
l		02				etup T				tSD	3.6	
					Data F	lold Ti	ne			tHD	0.7	
1					<u></u>							
ļ						Pulse V				tLW tREM	4.0	
-		In	out Loa	ding		Hold T				tINH	1.2	
P:	in Name		ctor (l									
	A1,A2		1		1							
]	B1,B2	1	1						l			
Ì	CK	l	1									
	IH	1	1									
	CL SI	1	3 1									
	A,B	1	2						1			
1	,2	- 1	~									
		- 1							l			
			tput Dr									
P:	in Name	Fac	ctor (l	.u)	1							
	Q XQ	- 1	36 36								ting condition	
	ΛŲ		30							operat. y multij		11
						0	, ,,,,,,					
1	Function	n Table	9									
١.										_		
]	MODE			7.11	or mr			0	יחיו זרוי			
] [	MODE			INI	101			001	PUT	-{		
		CLK	CL	D	A	В	SI	Q	XQ			
	CLEAR	Х	L	х	Х	X	х	Ĺ	Н			
	CLOCK	L→H	н	Di	L	L	Х	Di	Di			
		н	Н	x	L	 L	X	Q <sub>0</sub>	XQ.	1		
		11	11					٧٥	~~0			

Note : CLK = CK + IH $D = (A1 \times A2) + (B1 \times B2)$ 

 $Q_{\,\boldsymbol{0}}$ 

Si

Page 11-4

 $XQ_{\,\textbf{0}}$ 

Si

SCAN

Н

Н

X

Х

 $L{\to}H{\to}L$ 

Н

L H→L→H

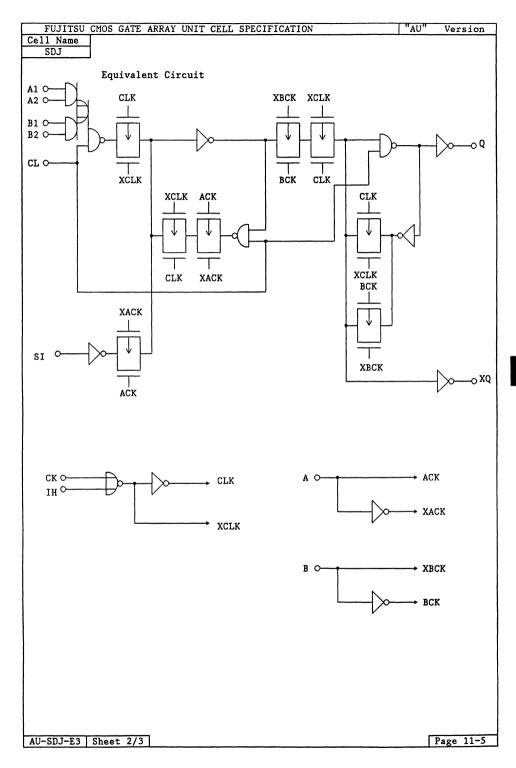
Si

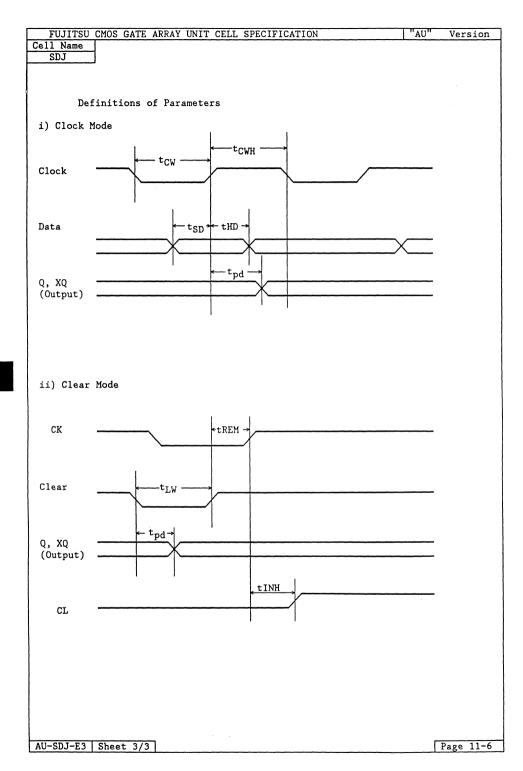
X

Н

Н

AU-SDJ-E3 | Sheet 1/3





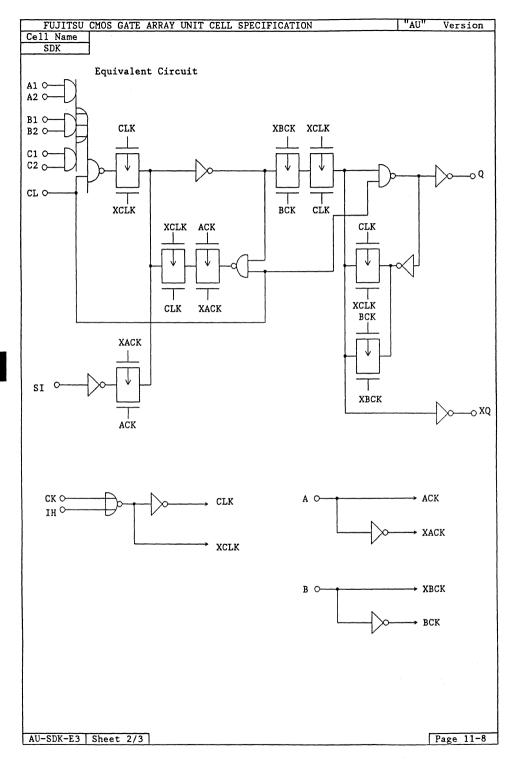
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			AU" Version
Cell Name	Function							Number of BO
SDK	SCAN 6-input DF	F with						16
Cell Symbol			Prop	agation	Delay		eter	
			up		td			
		t0	KCL	t0	KCL	KCL		
		2.96	0.07	2.40	0.03	0.0	7 7	CK, IH → Q
		1.86	0.07	1.73	0.05	0.1	0 7	CK, IH → X
A1 -	⊢ Q	2.99	0.07	0.82	0.03	0.0	7 7	CL → Q
A2 -	٧							X
B1 -								
B2		1					ł	1
C1								
C2 -		!		-			Ì	
C77								
CK _							İ	
IH —							-	
si —		Parame	ter				Symbol	Typ(ns)*
A ¬	р− <b>х</b> о	Clock	Pulse W	idth			tCW	4.4
в - С		Clock	Pause T	ime			tCWH	4.0
	P					<del></del>		
		Data S	etup Ti	me.			tSD	4.0
	CL	Data H	old Tim	e			tHD	0.4
		Clear	Pulse W	idth			tLW	4.0
		Clear	Release	Time			tREM	2.4
	Input Loading	Clear	Hold Ti	me			tINH	1.2
Pin Name	Factor (lu)							
A1,A2	1	1				- 1		
B1,B2	1							
C1,C2	1	1				1		
CK	1					1		
IH	1	1						
CL	3					İ		1
SI	1	l						
A,B	2							
,-								
	Output Driving	1				-		
Pin Name	Factor (lu)	<b></b>						
Q	36	* Mini	mum val	ues for	the tv	pical	operat	ting condition
χQ	36							ing condition
			given b					

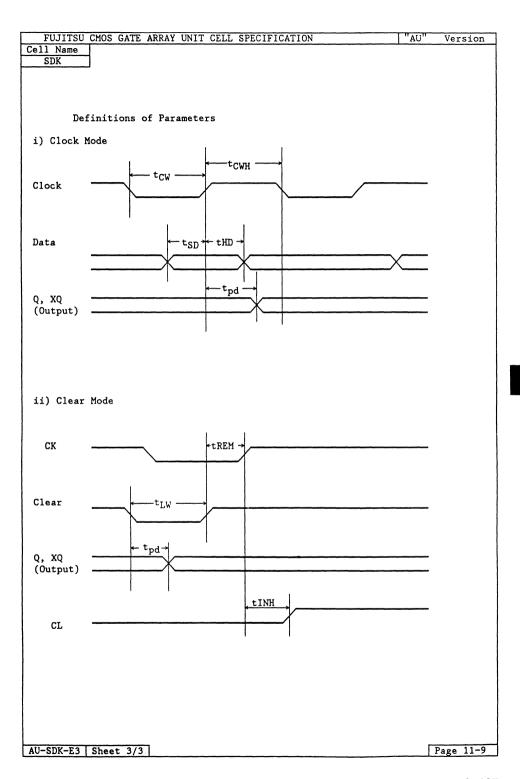
MODE			IN	PUT			OU.	rput -
	CLK	CL	D	A	В	SI	Q	XQ
CLEAR	Х	L	X	X	X	X.	. L	н
CLOCK	L→H	н	Di	L	L	Х	Di	Di
	Н	Н	Х	L	L	Х	Q <sub>0</sub>	$XQ_0$
SCAN	Н	Н	Х	L→H→L	Н	Si	Q <sub>0</sub>	ΧQο
	н	Н	Х	L	Н→L→Н	X	Sí	Si

Note : CLK = CK + IH  $D = (A1 \times A2) + (B1 \times B2) + (C1 \times C2)$ 

AU-SDK-E3 | Sheet 1/3

Page 11-7



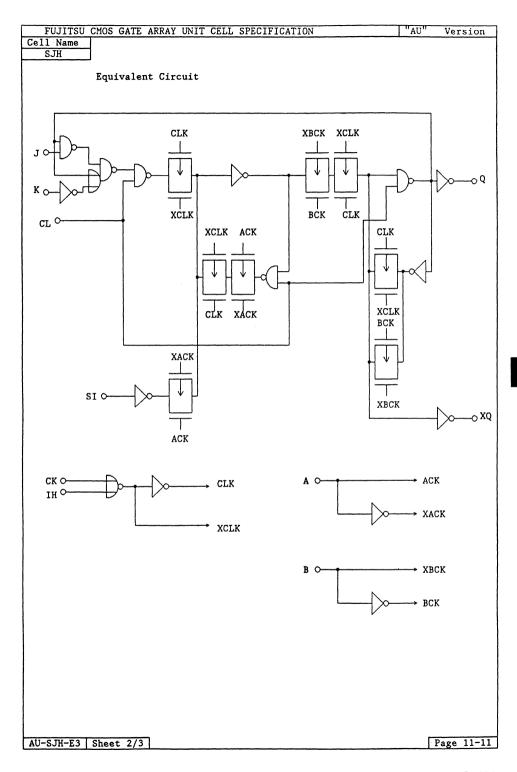


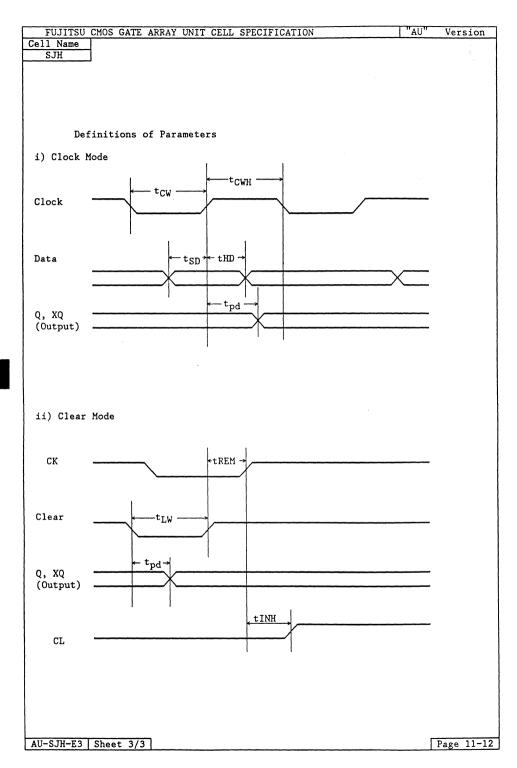
FUJITS	U CM	IOS G	ATE A	RRAY U	NIT CE	LL SPEC	IFICA	TIO	N		7.	"A	U"	Version
Cell Name		CMOS GATE ARRAY UNIT CELL SPECIFICATION Function											umber of BC	
SJH		SCAN	J-K	FF wit	h Clea	r & Clo	ck-In	hib:	it					16
Cell Symbo	01						pagat	ion	Delay		met	er		
						tup	+		to	ln KC	T O	anna	$\dashv$	D 1
1					t0 3.39	KCL 0.07	t0	70	0.03	0.		CDR2	-	$\frac{\text{Path}}{\text{CK,IH} \rightarrow \text{Q}}$
					1.89			73	0.05	0.		7	- 1	$CK,IH \rightarrow Q$ $CK,IH \rightarrow XQ$
					3.01			11	0.03	0.		7		CL → Q,
1 -									• • • • •		-		- 1	XQ
ј к-с		-	Q											
1 1					Param	eter					S	ymbol	$\dashv$	Typ(ns)*
CK						Pulse	Width					tCW	+	4.4
IH		1				Pause						tCWH	一	4.0
SI —														
в -d		p-	XQ		Data	Setup T	ime (	<u>J)</u>				tSD	_	3.6
- L	0				Data	Setup T	ime (	$\frac{K}{J,K}$				tSD	-	3.9
	Y	1.			Data	me (		tHD	$\dashv$	0.4				
1	·	EL			Clear	Width		tLW	$\dashv$	4.0				
1					Clear Pulse Width Clear Release Time							tREM	-	2.4
1						Hold T						tINH		1.2
			t Loa		1								1	
Pin Name		Fact	or (l	lu)	l									
J,K	- 1		1		İ								-	
CK													-	
CL	- 1		3		1								- }	
SI	- 1		1											
A,B	- 1		2											
,-	1				1									
				iving										
Pin Name		Fact	or (	lu)										
Q	l		36		* Mir	nimum va	lues	for	the ty	pica	1 0	perat	in	g condition.
XQ			36		The values for the worst case operati									
					are given by the maximum delay multip								)11	er.
Function	п Та	h1e												
					INPUT							T		
MODE														
	CI	LK	CL	J	K	<u>A</u>	В	<u>S</u>	I	Q		XQ		
	_	_	_						1					
CLEAR	>	<u> </u>	L	X	<u> </u>	X	<u> </u>	X		L		H		
		. 77	**					.,						
	L-	•п	Н	L	L	L	L	X		L_		<u>H</u>		
	L-	¥H	Н	н	Н	L	L	Х	- 1	н		L		
												-		
CLOCK	L-	+H	H	L	н	Ľ	L	Х		Q.	X	Q.		
	<u> </u>													
	L-	+H	H	Н	L	L	L	Х		$XQ_0$		Q <sub>0</sub>		
	<u> </u>					-								
	L 1	H	Н	X	X	L	L	Х		Q <sub>o</sub>	X	Q <sub>0</sub>		
SCAN	,	H	Н	X	X	L→H→L	Н		;		٠,			
SOMIN	<u> </u>			^		קבעבת	n	s		Q <sub>0</sub>		Q.		
	]	H	Н	X	X	L I	ł→L→H	X	<u> </u>	Si		Si		
1														

Note : CLK = CK + IH

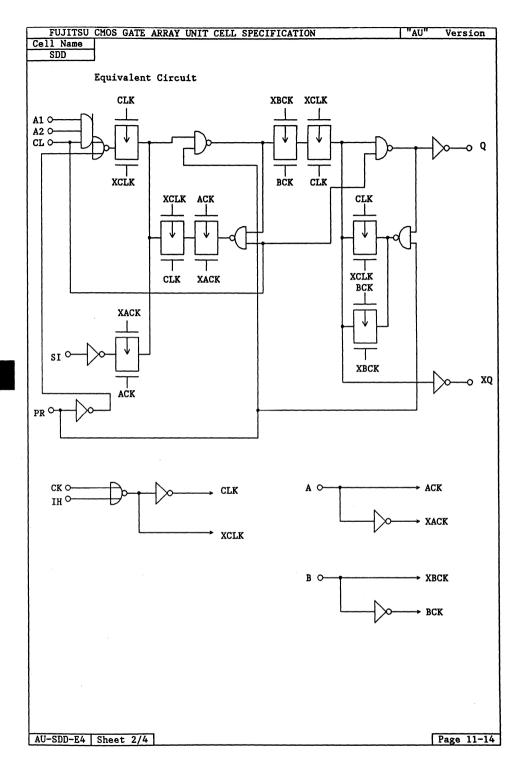
Page 11-10

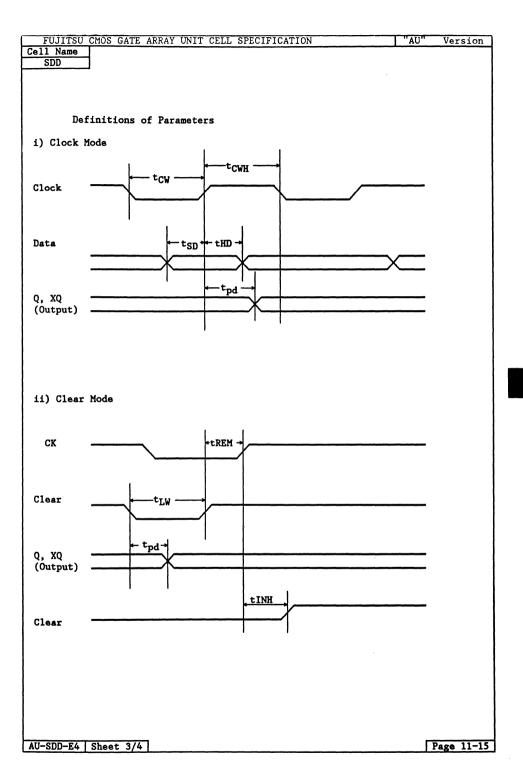
AU-SJH-E3 Sheet 1/3

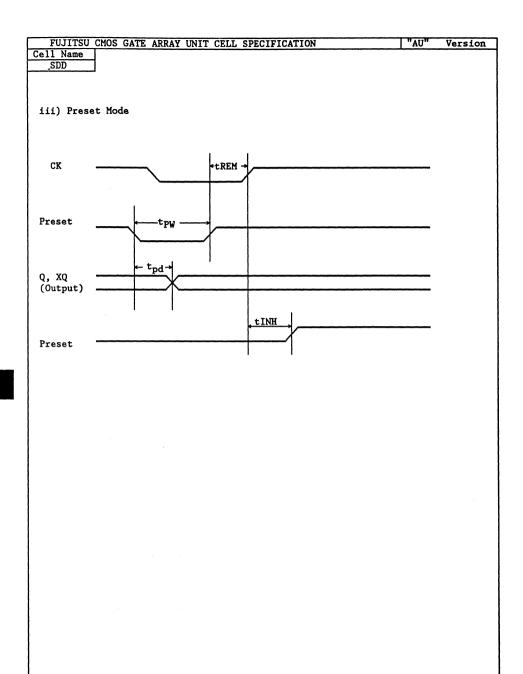




FUJIT	SU C	MOS G	ATE AR	RAY U	NIT CE	LL SPEC	IFICAT	ION			"/	AU" Version
Cell Nam	ie	Funct										Number of BC
SDD		SCAN	2-inp	ut DF	F with	Clear,	Prese	t & Clo	k-In	hibi	t	16
Cell Sym	bol					Pro		on Delay	Par			
					t0	tup   KCL	t0	KCL	dn	CL2	CDR2	Path
		PR			2.96	0.07				.07	7	CK, IH + Q
		,			2.12	0.07	1			.10	7	CK,IH → XQ
		هــ			3.60	0.07	0.8	2 0.03	3   0	.07	7	CL → Q,
A1 -	7	F	- Q		3.07	0.07	1.8	в 0.09	5   o	. 10	7	PR → Q,
A2 -			•				İ	1	ļ			XQ
CK -						1	1	1				
SI -	_				Param	eter				Ts	ymbol	Typ(ns)*
A -	-	b-	- xq		Clock	Pulse					tCW	4.4
В -	~ <u>_</u>		ΛQ		Clock	Pause	Time			_	tCWH	4.0
		Y			Data	Setup 1	ime			+	tSD	4.4
		CL				Hold Ti					tHD	0.8
					Class	Pulse	Width			-	+T 1/2	4.0
							e Time			╁	tLW tREM	2.4
			t Load			Hold 7					tINH	1.2
Pin Nam	ie	Fact	or (lu	)			111 1.1			_	+ DII	
A1,A2 CK		į	1 1				Width			+	tPW tREM	5.5
IH		1	1			t Hold					tINH	0.8
CL												
SI			1									
A,B			2		]							
		ł										
		Outp	ut Dri	ving								
Pin Nam	ne .		or (lu									
Q XQ		1	36 36									ing condition. ng condition
114			30					maximu				
Functi	on I	[able										
MODE	T				INPU	·			T	OUTT	ידיו זו	
HODE	$\vdash$	CLK	CL	PR	D	A	В	SI	Q	OUTF	XQ	
CLEAR		X	L L	н	x	X	x	X	L		Н	
PRESE	$\top$	х	н	L	Х	х	х	Х	н		L	
CLOCK		L→H	Н	н	Dí	L	L	х	D	i	Di	
		Н	Н	н	X	L	L	x	Q	0	XQ <sub>o</sub>	
SCAN		Н	Н	Н	Х	L→H→L	Н	Si	Q	0	XQ <sub>o</sub>	
		Н	Н	Н	Х	L	Н→Г→Н	х	s	i	Si	
CL/PR		Х	L	L	X	X	X Te : CL	X K = CK		ohit	ited	
						1101		D = A1				
AU-SDD-E	4 5	Sheet	1/4									Page 11-13







AU-SDD-E4 | Sheet 4/4

777.77.00											
Cell Name		MOS G Funct		RRAY U	NIT CEI	L SPECI	FICATIO	N		"A	U" Version Number of BC
Cell Name		runct	.1011								Number of BC
SDA	- }	SCAN	l 1-in	put DF	F with	Clock-I	nhibit				12
Cell Symb	001						agation		Parame	ter	
						up			dn Vor e	Loppo	
}					t0 2.55	KCL 0.07	t0 2.40	0.03	0.07	CDR2	$\begin{array}{c} \text{Path} \\ \text{CK,IH} \rightarrow \text{Q} \end{array}$
					1.87	0.07	1.74	0.05		7	CK, IH → XQ
										1	
	Г					1				1	
D -	7	1	— q								
CK -	-	}	•						İ	1	}
IH -	$\dashv$	l							1		]
SI										1	
A B	-d	F	yx −c		Parame	ter	ــــــــــــــــــــــــــــــــــــــ	Symbol	Typ(ns)*		
1					Clock Pulse Width						4.4
					Clock	Pause T	ime			tCWH	4.0
										+ OD	
					Data B	etup Ti Iold Tim	me			tSD	2.8
1					Data	ioid iiii				CILD	1.2
İ											1
	Input Loading								1		
Pin Name			or (l								
D		Tact	1	,u)							}
CK	1		1								
IH			1								
SI A,B	ı		1 2								
, , , , , , , , , , , , , , , , , , ,	1		2						Ì		
					ĺ				- 1		
	1				1				1		
		011++	nit De	iving	1						
Pin Name	,	Fact	or (l	u)	<b> </b>						
Q			36		* Mini	mum val	ues for	the t	ypical	operat	ing condition.
XQ	XQ 36										ng condition
<del></del>					are	given b	y the n	axımum	delay	multl	TIEI.
Function	on T	able									
							r		ı		
MODE				INPUT			דיים	PUT			
LIODE	-			111101			0.01	101			
	C	LK	D	A	В	SI	Q	XQ			
GT 007	-	. 11	ъ.			v	ъ.	<u></u>			
CLOCK	1	→H	Di	L	L	_X	Di	Di			
	1	Н	X	L	L	X	Q <sub>0</sub>	xQ,			
l <del> </del>	+							•			

Note : CLK = CK + IH

 $XQ_{o}$ 

Si

AU-SDA-E3 Sheet 1/3

X

X

L→H→L H

L H→L→H

Si

Х

 $Q_{\,0}$ 

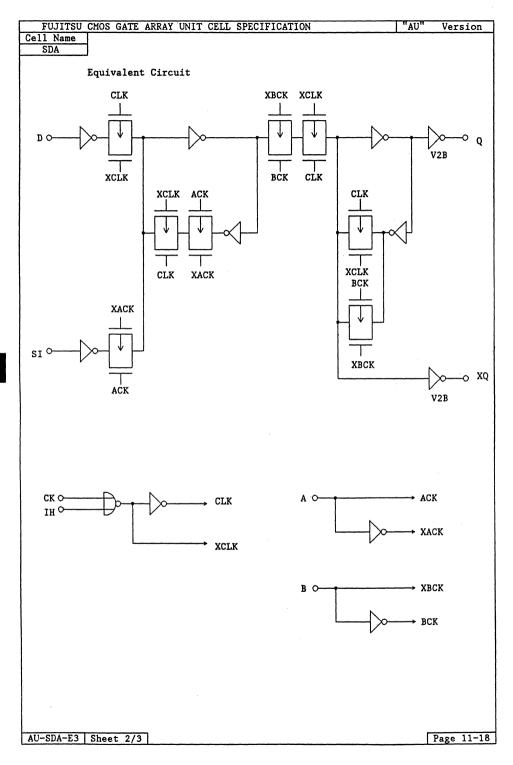
Si

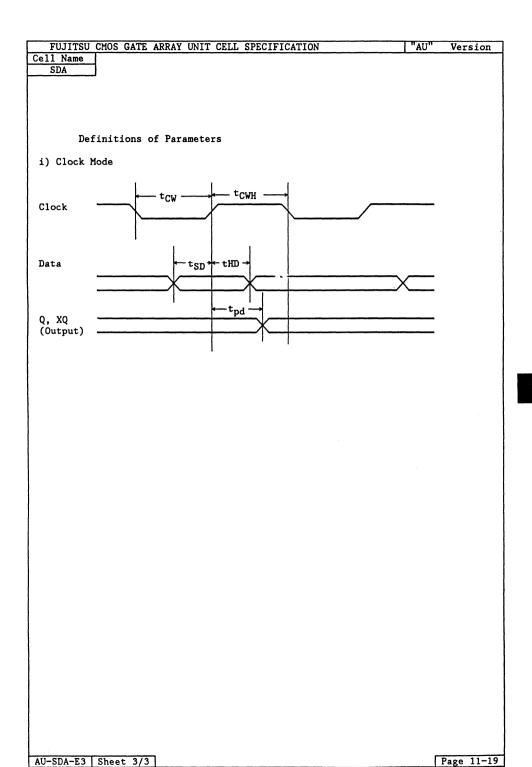
SCAN

Н

2-135

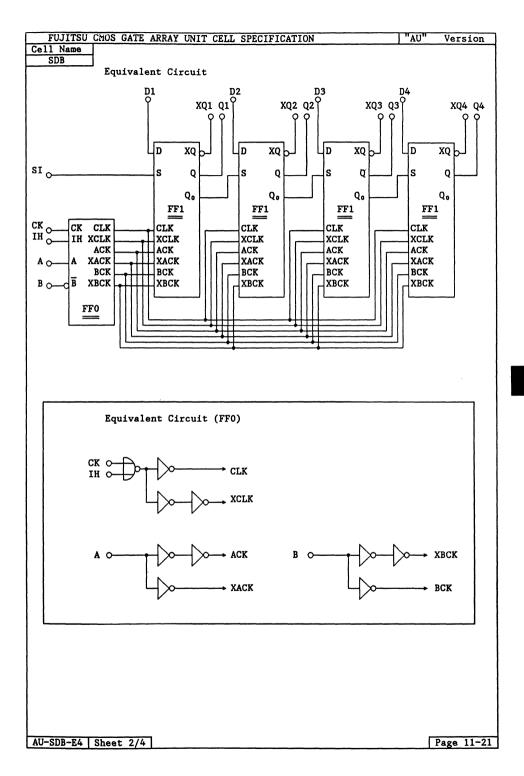
Page 11-17

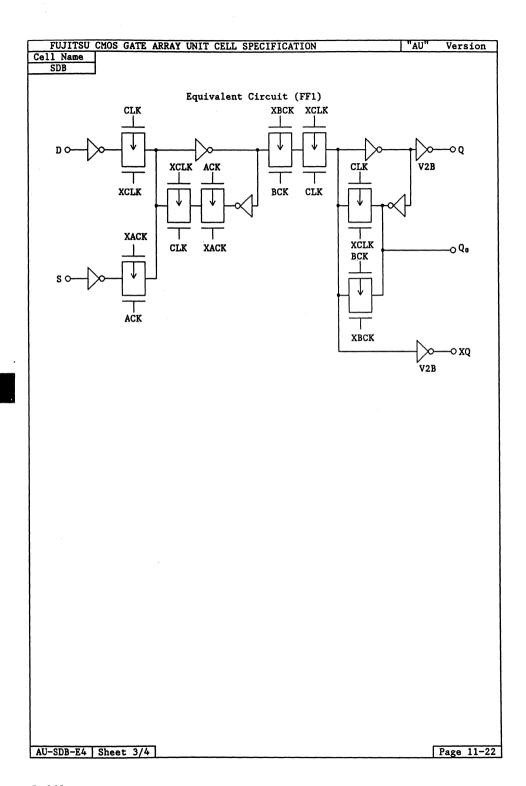


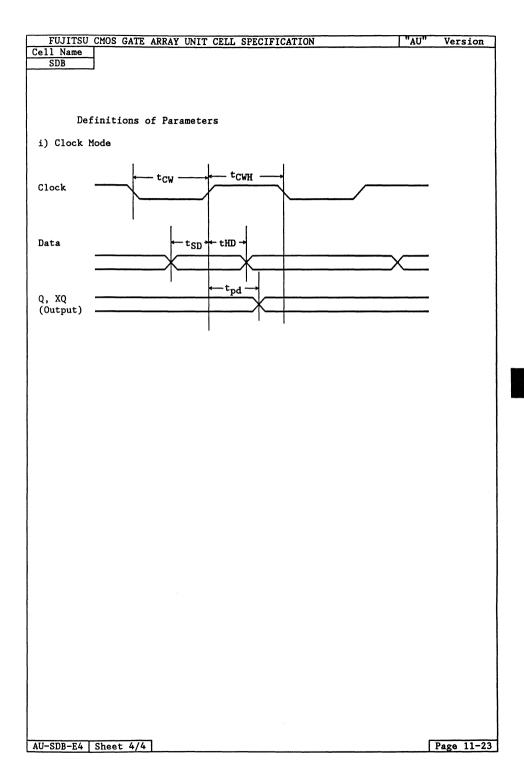


FILITS	I CMOS	CATE	ADDAY II	NIT CE	LL SPECI	ETCATION			т	"AU	" Version
Cell Name	Func	tion	ARRAI U	NII CE	T SPECT	FICATION	<u>'</u>		1		Number of BC
										$\top$	
SDB Cell Symbo	ol SCA	N 1-i	nput 4-	bit DF	F with C	lock-Inl agation	nibit Delay	Parer	neter		42
Gerr Bymb.	<u> </u>				tup	agacion	tdi		necer		T
				t0	KCL	t0	KCL	KCI		R2	Path
				3.39	0.07	3.15	0.03	0.0		7	CK, IH + Q
				2.60	0.07	2.66	0.05	0.1	10	7	CK, IH → XQ
						1					
		1			i i		l				
D1			Q1						1		1
D2 ——	4		XQ1 Q2						- 1		
D4	-	þ	XQ2		1						
ск —	4	_	Q3								
IH	-		XQ3	Parame		L	1		Symb	1	Tron (0.0)#
sı —	7	b	Q4 XQ4		Pulse W	idth		-	tCV		Typ(ns)*
A	<u>.</u>			Clock	Pause T	ime			tCV		4.0
1 5	`L	l		2	. m.				tSI		1.0
<b>[</b>				Data	Setup Ti Hold Tim		1.8				
				Data	ioid iiii	<u> </u>			tHI		
1				1				ı			1
	1 7	<del></del> T.a	ading	1				- 1			
Pin Name		tor (									
a		1						1			
CK		1		1				l			
IH SI		1 1		l							
A,B		2		}				i			1
				}				l			
1				Ì							
				1				- 1			
	Out	put D	riving	1				i			
Pin Name		tor (	lu)	·		_					
Q XQ	ļ	36 36		* Min	imum val	ues for	the ty	pica case	lope	rati	ng condition.  ng condition
<u>، ۲۷</u>	1	50		are	given b	v the m	worst aximum	dela <sup>.</sup>	opera v mul	tipl	ier.
					9						
Function	n Table										
					<del></del>	Γ		٦			
MODE			INPUT			OUT	PUT	1			
	CLK	Dn	A	В	SI On-1	02	YOn	1			
	CLIK	זוע	A	D	SI,Qn-1	Qn	XQn	1			
CLOCK	L→H	Di	L	L	X	Di	Di	_			
	и	v	т	L	v	050	XQn∘				
	Н	<u> </u>	L	п п	Х	Qn•	λίπο	-			
SCAN	н	X	L→H→L	H	Si	Qno	XQn∘				
	н	х	L	н→г→н	Х	Si	Si	1			
	· · · · · · · · · · · · · · · · · · ·										
						Note	: CLK =				
							n = 1	~ 4			

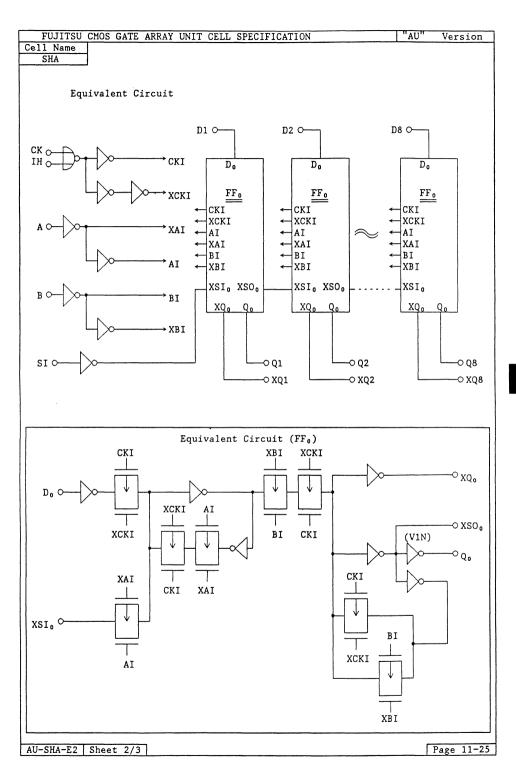
AU-SDB-E4 | Sheet 1/4

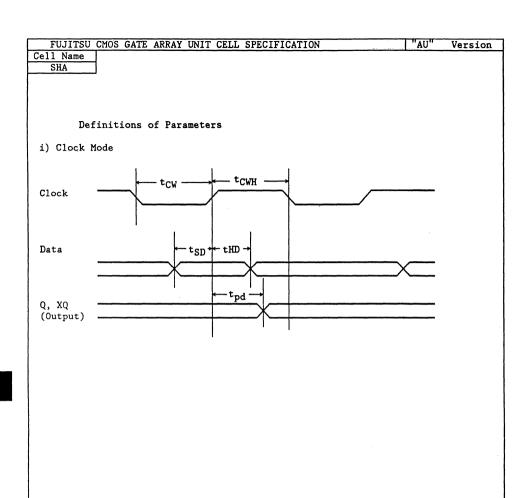






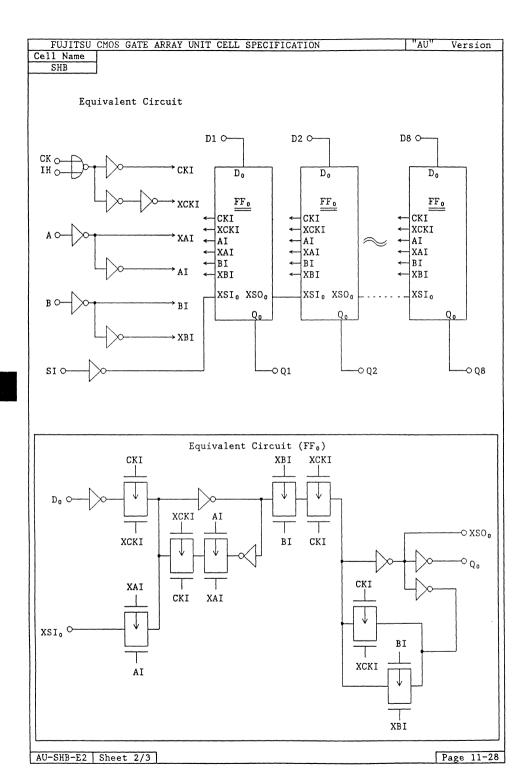
FILITSII C	MOS GATE ARRAY U	NIT CEL	T SPECT	FICATIO	N		Ι "Δ	U" Version
Cell Name	Function	NII CEL	L BIECI	FICALIO	14		^^	Number of BC
SHA	SCAN 1-input 8-	bit DFF				D		68
Cell Symbol		+	up up	agation	Delay td		eter	
		t0	KCL	t'0	KCL	KCL	2 CDR2	Path
		3.78	0.13	3.78	0.07	0.0		CK,IH → Q
D1	Q1	3.30	0.13	3.20	0.11	0.1	5 4	CK,IH → XQ
D2 ————————————————————————————————————	р—— XQ1							
D4	Q2 — XQ2						1	
D5	Q3						l	
D6	р хоз							
D7	Q4						1	
D8	р—— XQ4 —— Q5							
	р—— XQ5						ı	
	Q6							
CK	р— хо6	Parame	ter Pulse W	1.1+1.			Symbol	
IH SI	Q7 > XQ7		Pause T				tCW tCWH	5.8
A	— Q8			,				<del></del>
В —	P—— XQ8	Data S	etup Ti	me			tSD	1.5
	· · · · · · · · · · · · · · · · · · ·	Data H	old Tim	e			tHD	2.7
	Input Loading	•						ľ
Pin Name	Factor (lu)							
D	1					1		
CK	1					1		
IH SI	1 1							
A	1							
В	1	1						
	Out-ut Deini-	ł						
Pin Name	Output Driving Factor (lu)					1		
Q	18							
XQ	18	* Mini	mum val	ues for	the ty	pical	operat	ing condition.
		The	values	for the y the m	worst	case	operati	ng condition
	L	are	given b	y the m	aximum	delay	multip	ilei.
ł								
								<u></u>
AU-SHA-E2 S	Sheet 1/3							Page 11-24

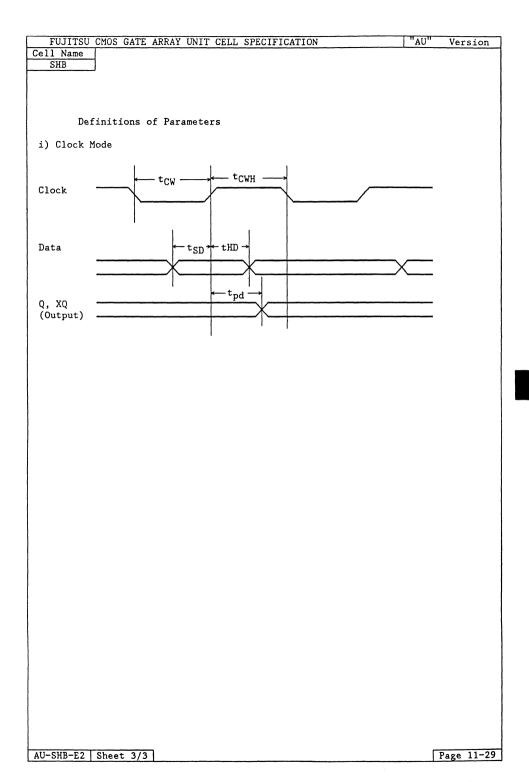




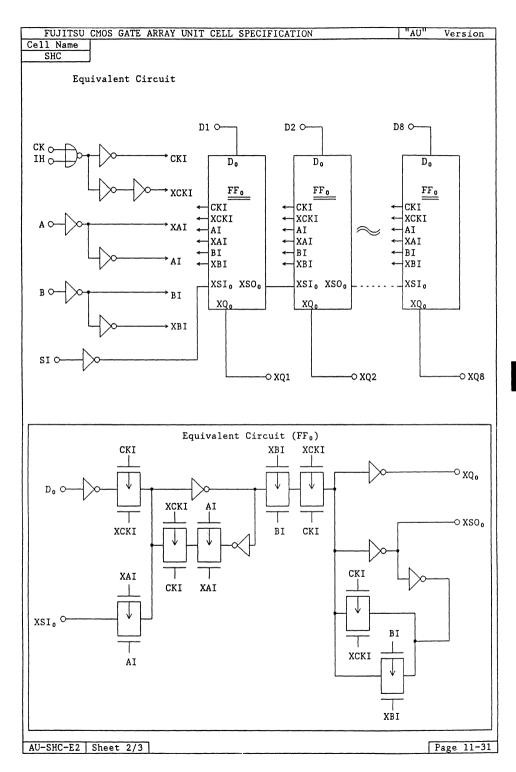
AU-SHA-E2 | Sheet 3/3

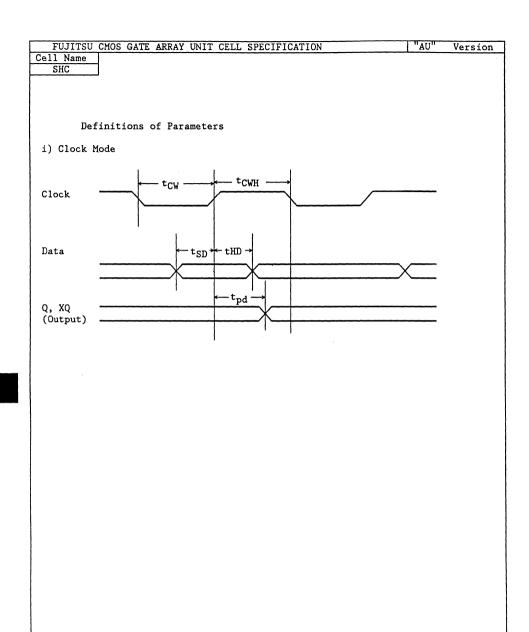
THITTSH C	MOS GATE ARRAY U	NIT CEL	T CDECT	FICATIO	NI.		ΠΔ1	U" Version
Cell Name	Function	NII CEL	D BLECT	FICATIO	-14			Number of BC
SHB	SCAN 1-input 8-	bit DFF	with C	lock-In	hibit &	Q Out	tput	62
Cell Symbol		+	up up	agation	Delay td		eter	<del></del>
		t0	KCL	t0	KCL	KCL	2   CDR2	Path
		3.46	0.13	3.54	0.07	0.08		CK,IH → Q
					}			
D1 ————————————————————————————————————	Q1 Q2				j			
D3	Q2 Q3							
D4	├ Q4				}			
D5	Q5					}		
D6	Q6 — Q7				)	1	j	
D8	Q8		ľ				1	
ck —	, ,						1	
IH —	1		<u> </u>	l	<u></u>	L		<u> </u>
sı —		Parame	ter Pulse W	idth			Symbol tCW	Typ(ns)* 5.8
A			Pause T				tCWH	4.4
в — ф_								
		Data S	etup Ti	me			tSD	1.6
		Data H	old Tim	ie			tHD	2.7
	Input Loading							
Pin Name	Factor (lu)							
D CK	1 1							
IH	1							
SI	1					1		
A	1					- 1		
В	1							
	Output Driving	1				1		
Pin Name	Factor (lu)							
Q	18					1		
		" Mini	mum vai	tes for	the ty	case (	operati operati	ing condition. ng condition
		are	given b	y the m	naximum	delay	multip	lier.
AU-SHB-E2	Sheet 1/3							Page 11-27
AU UND-EZ	Direct 1/3							lage II-2/





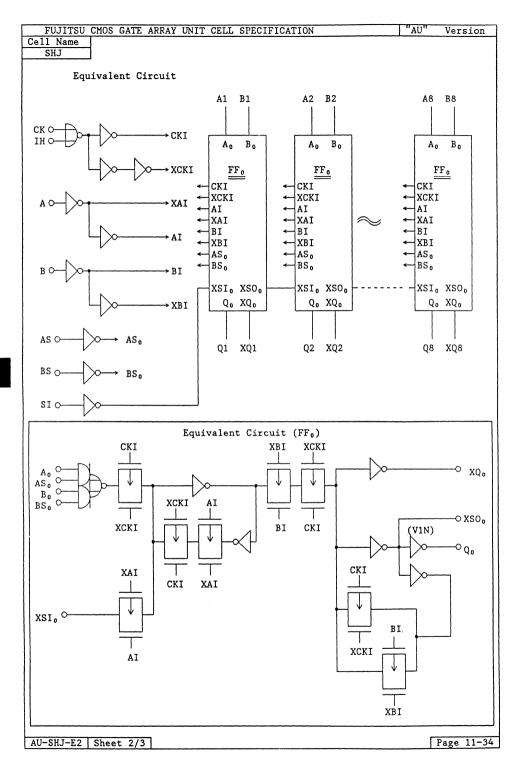
r FOLLETSH C	MOS GATE ARRAY U	NIT CEL	T. SPECT	FICATIO	N		Δ" Δ	U" Version
	Function	MII CEE.	L SILCI.	FICKITO				Number of BC
SHC	SCAN 1-input 8-	bit DFF	with C	lock-In	hibit &	XQ Ou	tput	62
Cell Symbol			Prop	agation	Delay	Parame	ter	
			up		td	n		
		t0	KCL	t0	KCL	KCL2		Path
		3.35	0.13	3.28	0.11	0.15	5 4	CK,IH → XQ
		1					l	į
D1	р—— хол	į į						
D2	р—— хог						1	
D3	р—— хоз Усу						l	
D4	P χQ4 P χQ5						1	
D6	~ xQ6						1	
D7	р—— ход						1	
D8	р—— xQ8	1					ì	
1							1	
CK:							1	1
IH -		Parame					Symbol	
SI		Clock	Pulse W	idth			tCW	5.8
A		Clock	Pause T	ime			tCWH	4.4
1 " 1								
]		Data S	etup Ti	me			tSD	1.6
		Data H	old Tim	<u>e</u>			tHD	2.7
<b></b>	Input Loading	4				1		
Pin Name	Factor (lu)	1						
D	1	1						
CK	1	İ				-		
IH	1	ł				1		
SI	1	1				l		
A	1							
В	1	1				1		
		]				1		
	Output Driving							Ì
Pin Name	Factor (lu)	<del> </del>						
XQ	18	# Mini	mum *** 1	nos for	the tu	mical	operat	ing condition
	1	The	mum vai values	for the	worst	case o	perati	ing condition
j		are	given b	y the m	aximum	delay	multip	olier.
					***************************************			
1								
1								
}								
1								
1								
1								
1								
1								
1								
AU-SHC-E2 S	Sheet 1/3							Page 11-30





AU-SHC-E2 | Sheet 3/3

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	
Cell Name	Function SCAN 8-bit DFF	with Cl	ook-Inh	ihi+				Number of BC
SHJ	& 2-to-1 Data M			IDIC				78
Cell Symbol				agation	Delay	Paramet	er	
		t	up	0	td			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.86	0.13	3.87	0.07	0.10	4	CK, IH → Q
		3.30	0.13	3.20	0.09	0.16	4	CK,IH → XQ
A1	Q1		ĺ				1	
B1 -	P—— XQ1						1	1
A2	Q2							
B2	○ XQ2						1	1
A3	Q3						l	1
B3 —	р—— хоз						1	
A4 ————————————————————————————————————	Q4 ————————————————————————————————————		1				1	
A5	Q5 Q5						1	
В5 —	xQ5		į				1	
A6	Q6						1	1 1
В6 —	⊳— xQ6						}	
A7	Q7						}	1
В7 —	þ x̂Q7						1	
A8	—— Q8							
В8	₽—— XQ8						1	
AS								1
BS —								
ск —								1
IH —								
si —				L	<u></u>	<del> </del>		
Α		Parame	ter Pulse W	2.34%			tCW	Typ(ns)*
в — ф			Pause T				tCWH	5.8
		CIUCK	rause 1	Tme			CCWII	<del>  •••</del>
		Data S	etup Ti	me			tSD	2.4
		Data H	old Tim	e			tHD	2.5
	Input Loading							
Pin Name	Factor (lu)							1
An, Bn	1							
(n=1~8)								
AS,BS	1							
CK	1							
IH	1					1		
SI	1 1							
A,B	1							1
<del></del>	Output Driving							
Pin Name	Factor (lu)							
Q	18							
χQ	18	* Mini	mum val	ues for	the ty	pical	operati	ing condition.
·		The	values	for the	worst	case o	peratir	ng condition
		are	given b	y the m	aximum	delay	multipl	lier.
-								
AU-SHJ-E2 S	Sheet 1/3							Page 11-33
·						<del></del>		

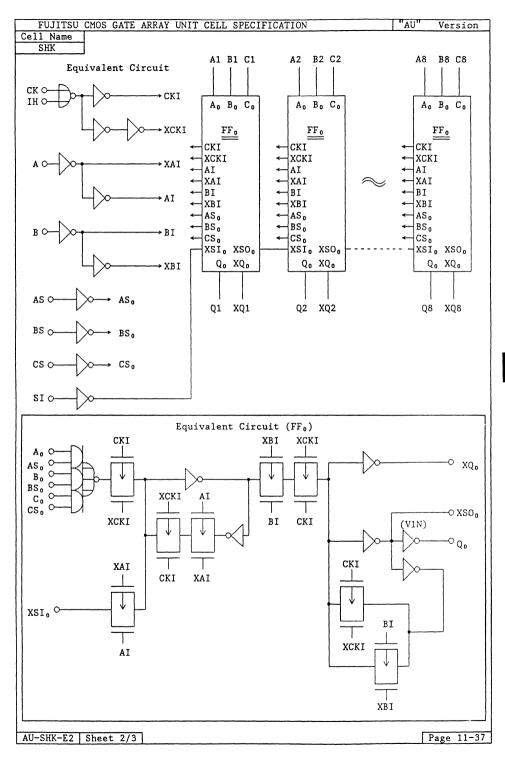


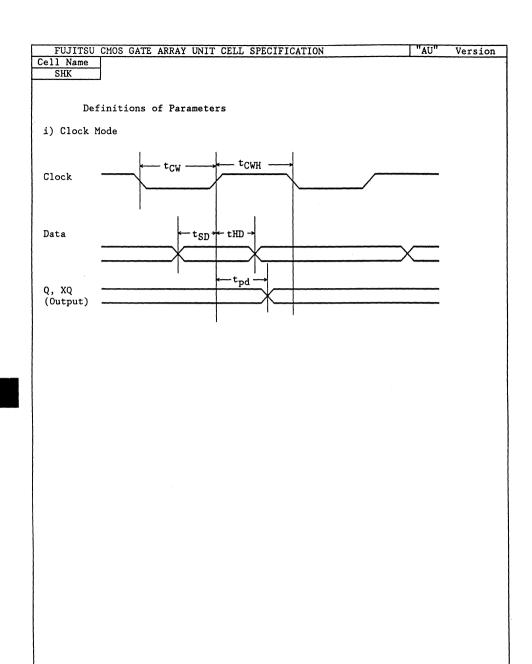
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version Cell Name SHJ Definitions of Parameters i) Clock Mode t<sub>CWH</sub> Clock Data -tHD t<sub>SD</sub>\* t<sub>pd</sub> -Q, XQ (Output)

AU-SHJ-E2 | Sheet 3/3

Page 11-35

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	
Cell Name	Function	1.1.61						Number of BC
SHK	SCAN 8-bit DFF			ibit			ł	0.0
Cell Symbol	& 3-to-1 Data M	ultiple	Pron	agation	Dolow	Paramot	<u></u> _	88
Cell Symbol		+	up	agation	td	n	ET	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
A1		3.71	0.13	3.68	0.07	0.08	4	CK, IH → Q
B1	Q1	3.27	0.13	3.20	0.11	0.15	4	CK, IH → XQ
C1	1	3.27	0.13	0.20	0.11	0.120	'	011,211
A2	р—— xq1						ļ	
B2	Q2						l	
C2	1						ł	
A3	р xq2							
В3	Q3						}	
C3	р xqз						ł	
A4	i i						}	
B4	Q4							
C4	р xq4						Ì	
A5	1 1							
B5	Q5						1	
A6	Þ χQ5						1	
B6	Q6						1	
C6	1						1	
A7	р—— XQ6							
В7	Q7							
C7	1 1							
A8	P XQ7						ł	
В8	Q8							
C8	р—— xQ8							
	, AQ0							
AS9								
BS ——							l	
cs — q								
CK		Damama	L			L	 	Typ(ns)*
IH —		Parame	Pulse W	id+h			ymbol tCW	5.8
A		Clock	Pause T	ime			tCWH	4.4
В —		OTOCK	Tause 1	TINE			20111	7.7
		Data S	etup Ti	me.			tSD	3.1
		Data H	old Tim	e			tHD	2.4
}								
	Input Loading							
Pin Name	Factor (lu)							
An, Bn, Cn	1							
(n=1~8)								
AS,BS,CS	1					1		
CK	1					İ		
IH	1							
SI	1							
A,B	1							
	Output Driving					-		
Pin Name	Factor (lu)							
Q	18	l						
xQ	18	* Mini	mum val	ues for	the tv	pical c	perat	ing condition.
1								ng condition
			given b					
1								
AU-SHK-E2 S	Sheet 1/3							Page 11-36

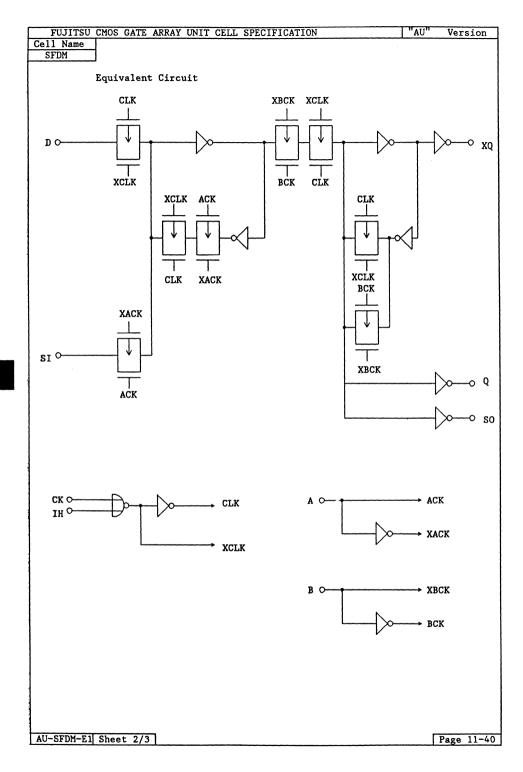


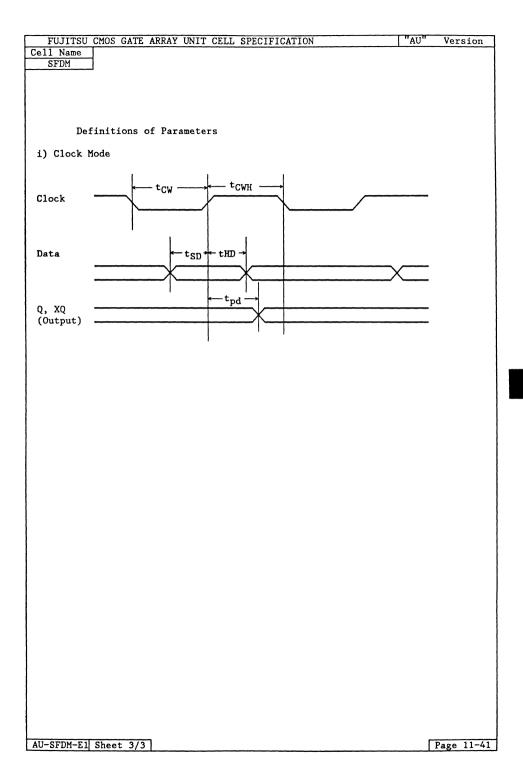


Page 11-38

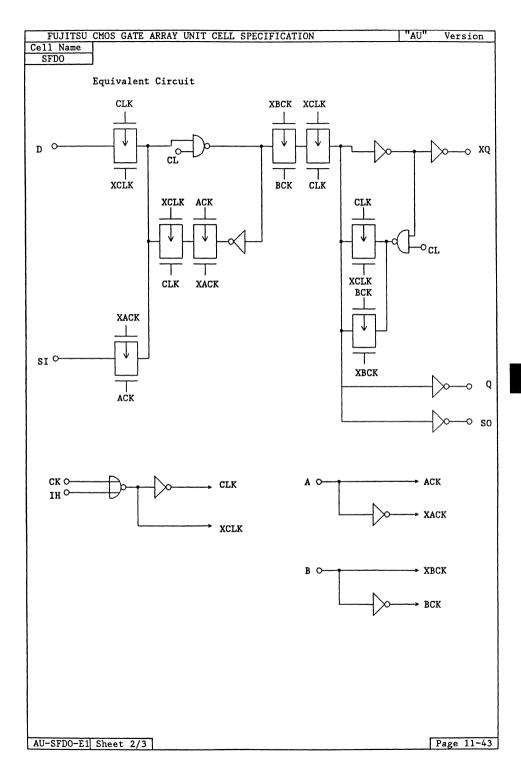
AU-SHK-E2 | Sheet 3/3

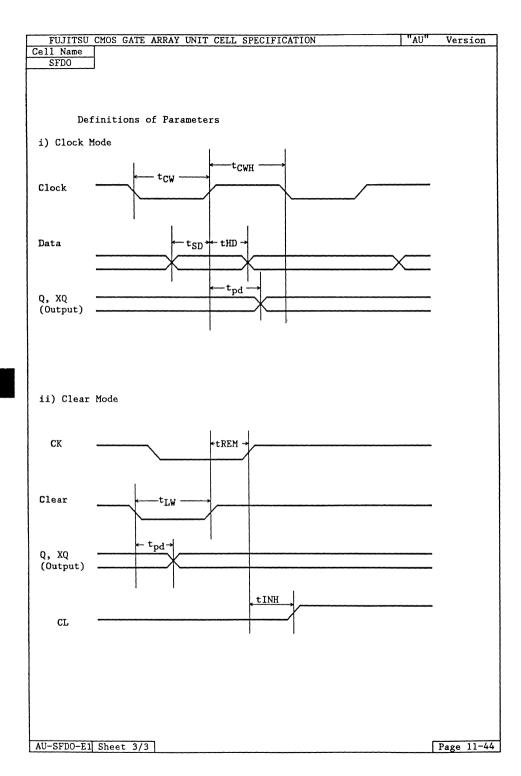
FILITSIL	MOS GATE ARRAY U	NIT CEL	T SDECT	FICATIO	N		Ι πΔ.	U" Version
Cell Name	Function	NII CEL	L SPECI	FICALIO	IN .		^A	Number of BC
SFDM	SCAN 1-input DF	F with	Clock-I	nhibit				10
Cell Symbol				agation			er	
		t0	up KCL	t0	td KCL	KCL2	CDR2	Path
		1.85	0.13	1.90	0.08	0.14	4	CK → Q
		2.35	0.13	2.31	0.07	0.08	4	CK → XQ
į							1	
							ţ	
D —	Q						ł	
1 1	— <b>4</b>						1	
CK	р—— <b>х</b> Q						ł	1
IH SI	so		1				1	
A	30					Ì	l	
В — ф						ŀ	1	
						j	}	
		Parame	ter	L	L	<u>ا</u> ا	ymbol	Typ(ns)*
1		Clock	Pulse W				tCW	4.0
1			Pause T				tCWH	4.0
		Data S	etup Ti Old Tim	me			tSD tHD	1.3
		рата н	1010 111	ie			THD	1.1
	Input Loading							
Pin Name	Factor (lu)							
D								
CK	1							
IH SI	1 2	l						i
A,B	2	1						
1,5	Output Driving							
Pin Name	Factor (lu)	}						
Q	18	<u></u>						
so	18	* Mini	.mum val	ues for	the ty	pical o	operat	ing condition.
		are	given b	or the m	WOIST	delay r	perati multin	ng condition
	1	are	given L	y the n	IAXIMUM	ueray i	uuicip	iller.
ļ								
l								
l								
1								
AU-SFDM-E1 S	Sheet 1/3							Page 11-39
								1 0



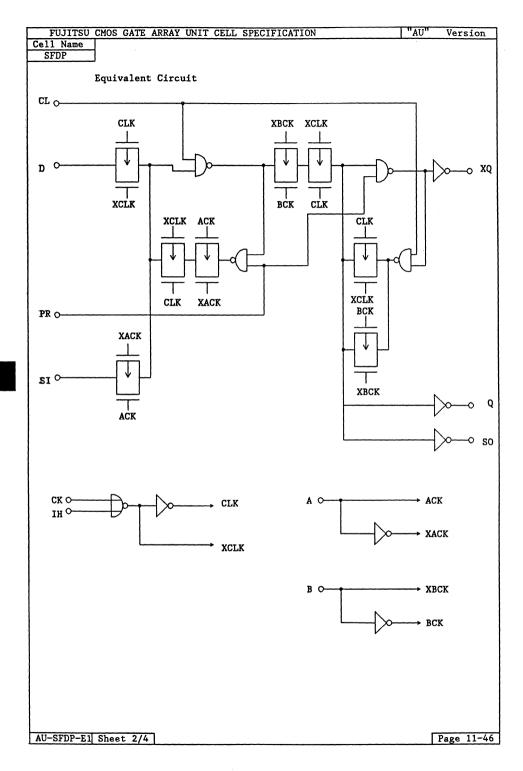


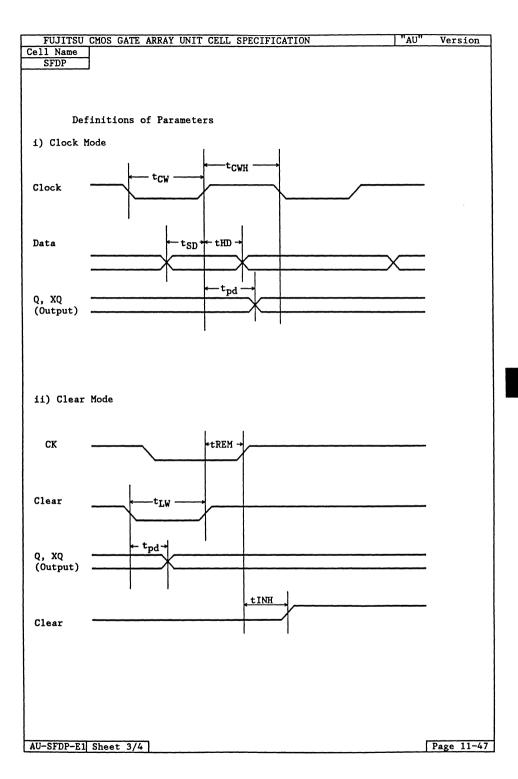
DUTTED O	MOC CATE ADDAY II	NITE OF	T CDECT	DICATIO	.,		1 WA	11" 171
Cell Name	MOS GATE ARRAY U Function	NIT CEL	L SPECI	FICATIO	N		- I A	U" Version Number of BC
Cell Name	r unc C10II							HOMBEL OF BC
SFDO	SCAN 1-input DF	F with	Clear a	nd Cloc	k Inhih	ít.		11
Cell Symbol	boan I Input bi	1 WICH	Prop	agation	Delay	Paramet	er.	
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
İ		2.14	0.14	2.04	0.09	0.15	4	CK → Q
į		2.37	0.13	2.62	0.07	0.08	4	CK → XQ
		2.51	0.13	2.18	0.09	0.15	4	CL + Q,XQ
								1
							l	
D —	Q						l	
CK -							}	
IH —	р—— <b>х</b> Q						}	
sı —	so						1	
A							l	
В ——	}							
-	<del>-                                    </del>		l					
1	1	Parame	ter	L		٠	Symbol	Typ(ns)*
	cr		Pulse W	idth			tCW	4.0
1		Clock	Pause T	ime			tCWH	4.0
1								
1		Data S	etup Ti	me			tSD	2.1
		Data H	lold Tim	ie			tHD	1.4
	Input Loading	Clear	Pulse W	idth			tLW	4.0
Pin Name	Factor (lu)	Clear	Release	Time			tREM	1.6
D	2	Clear	Hold Ti	me			tINH	3.9
CK,IH	1							
SI	2							
A,B	2 2	l						
CL	Output Driving	ł						
Pin Name	Factor (lu)	l						
Q	18	ł						
xQ	18							
so	18	* Mini	mum val	ues for	the ty	pical o	operat	ing condition.
1		The	values	for the	worst	case of	perati	ng condition
		are	given b	y the m	aximum	delay :	multip	lier.
1								
l								
ł								
1								
į .								
1								
1								
ALL CEDO DEL	35 4 - 1 / 6 - 1							<u> </u>
AU-SFDO-E1 S	oneet 1/3							Page 11-42

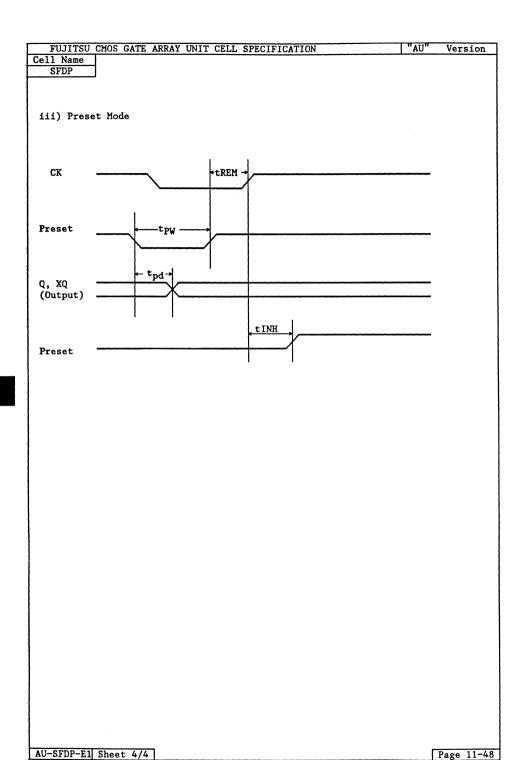




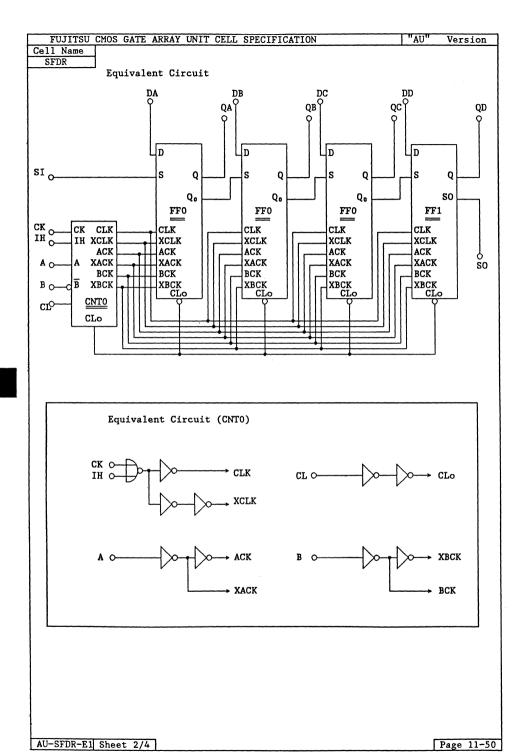
FILLITCH C	MOS GATE ARRAY U	NIT CET	CDECT	ETCATTO	NI		"A	U" Version
	Function	NII CEL	L SPECI	FICATIO	IN		^_	Number of BC
2022 11000								THE STATE OF BUILDING
SFDP	SCAN 1-input DF	F with	Clear,P	reset,a	nd Cloc	k Inhil	oit	12
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td	n		
	İ	t0	KCL	t0	KCL	KCL2		Path
1		2.16	0.14	2.03	0.09	0.15	4	CK → Q
	PR	2.86	0.13	2.62	0.07	0.08		CK → XQ
		2.91	0.13	2.15	0.09	0.15	4	CL + Q,XQ
	}	3.64	0.14	0.83	0.07	0.08	4	PR → Q,XQ
							l	
D	├ Q						j	
CK —	h vo							
IH —	р—— х <b>Q</b>							
si —	so						i	
Α —								1
в — ф	j						1	
_	<del>-</del>						1	
		Parame	ter			<del></del>	Symbol	Typ(ns)*
	cL		Pulse W	idth			tCW	4.0
			Pause T				tCWH	4.0
İ		OTOCK	14436 1	TIME			COMIT	7.0
		Data S	etup Ti	me			tSD	2.1
İ			old Tim			<del></del>	tHD	1.4
		Dava II		-		-+		
	Input Loading	Clear	Pulse W	idth			tLW	4.0
Pin Name	Factor (lu)	Clear	Release	Time			tREM	1.6
D	2		Hold Ti				tINH	3.9
CK, IH	1							
SI	2	Preset	Pulse	Width			tPW	4.9
A,B	2	Preset	Releas	e Time			tREM	0.8
CL,PR	2	Preset	Hold T	ime			tINH	4.9
	Output Driving							
Pin Name	Factor (lu)							
Q	18							
XQ	18							
S0	18							ing condition.
		The	values	for the	worst	case of	perati	ng condition
		are	given b	y the m	aximum	delay i	multip	lier.
AU-SFDP-E1 S	Sheet 1/4							Page 11-45

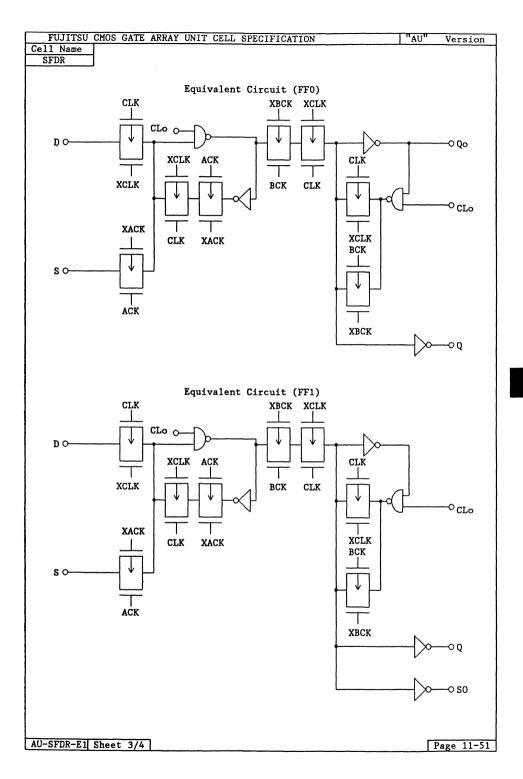






THAT TO CALL	MOG GAME ADDAY I	NITE OFF	Copper	Dra.mro	.,			U" Version
Cell Name	CMOS GATE ARRAY U Function	NIT CEL	L SPECI	FICATIO	N		A	U" Version Number of BC
CETT Mame	1 micción							rumber of bc
SFDR	SCAN 4-input DF	F with	Clear a	nd Cloc	k Inhih	it		36
Cell Symbol			Prop	agation	Delav	Parame	eter	
		t	up		td			
		t0	KCL	t0	KCL	KCL:	2 CDR2	
		2.98	0.14	3.00	0.09	0.1		CK → Q
Г		-	-	3.07	0.09	0.1	6 4	CL → Q
DA —	QA							
DB -	QB							
DC -	├── QC					1		
DD —	QD					}		
ск —						ł		
IН ——						ł	-	
si —	so					l	- }	
Α						ł	ł	
в — ф						l	ł	
Ĺ_	<del></del>					1	ł	1
		Parame	ter		L	'Т	Symbol	Typ(ns)*
	CL	Clock	Pulse W	idth			tCW	4.0
		Clock	Pause T	ime			tCWH	4.4
		Data S	teup Ti	me			tSD	0.9
		Data H	old Tim	e			tHD	2.0
	_							
	Input Loading	Clear	Pulse W	idth			tLW	4.0
Pin Name	Factor (lu)	Clear	Release	Time			tREM	2.3
D	2	Clear	Hold Ti	me			tINH	4.6
CK, IH	1							
SI	2							
A,B	1 1							
CL	Output Driving							
Pin Name	Factor (lu)							
Q	18							
so	18							
		* Mini	mum val	ues for	the tv	rpical	operat	ing condition.
								ng condition
		are	given b	y the m	aximum	delay	multip	olier.
				<del></del>				
AU-SFDR-E1	Sheet 1/4							Page 11-49

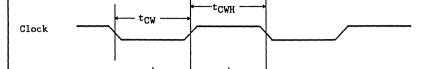




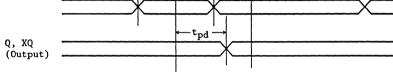
Definitions of Parameters

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

i) Clock Mode



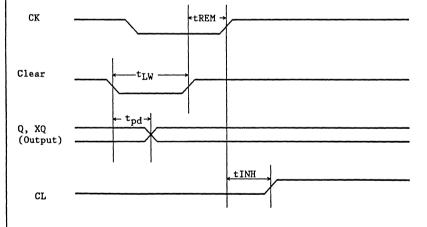
Data



tHD

tSD

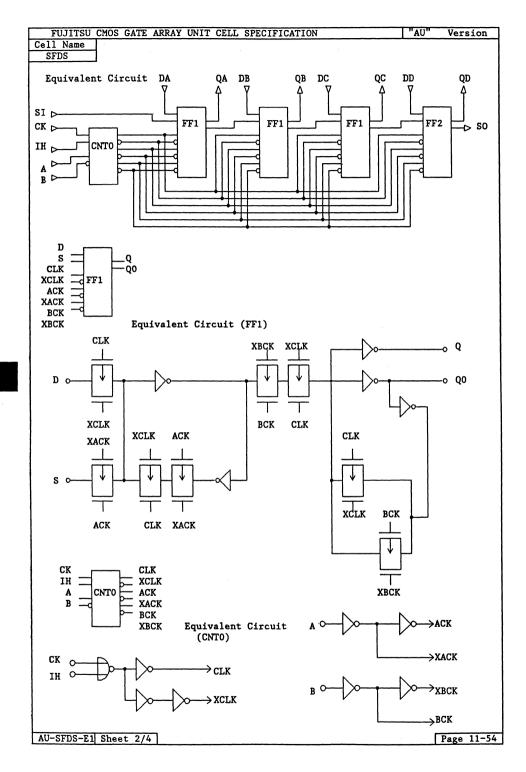
ii) Clear Mode

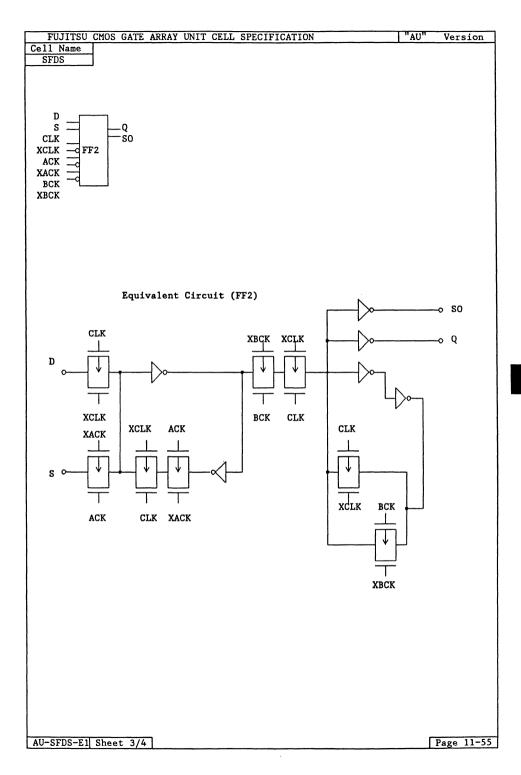


AU-SFDR-E1 Sheet 4/4

Page 11-52

FILITEII (	TMOC CATE ADDAY II	NITT CET	CDECT	ETCATIO	NI			"AU	Womaian
	CMOS GATE ARRAY U Function	NII CEL	L SPECI	FICATIO	IN				" Version Number of BC
SFDS	SCAN 4-input DF	F with	Clock I	nhibit				L	31
Cell Symbol				agation	Delay		neter	<u> </u>	<del></del>
			up KCL	t0	td KCL	n KCI	210	CDR2	- B-46
		t0 2.46	0.13	2.42	0.08	0.1		4	Path CK → QA~Q
		2.63	0.13	2.60	0.08	0.1		4	CK → QD
				2.00					(-
							- 1		İ
DA -	QA						- 1		
DB —	QB				'		- 1		
DD -	QC QD				ł		ł		
	QD .				i	ļ			
CK -									
IH —					1	l			1
SI —	so so					<u> </u>			
В ——		Parame	ter					mbo1	Typ(ns)*
" 1			Pulse W					CW	4.0
		Clock	Pause T	1me			t	CWH	4.0
		Data S	etup Ti	me			+	SD	0.0
		Data H	old Tim	e		_		HD	1.8
									, L, :
	Input Loading								
Pin Name	Factor (lu)								
D	2								
CK,IH	1 2								
SI A,B	1	i							
n,,,	1	ļ							
	Output Driving								
Pin Name	Factor (lu)								
Q	18								
so	18	4				•			
		* Mini	mum val	ues for	the ty	pica.	1 op	erati 	ng condition g condition
			varues given b						
	<u> </u>	arc	given b	y one a	MALMON		,		101.
	•								
1									
	····								
AU-SFDS-E1	Sheet 1/4								Page 11-53



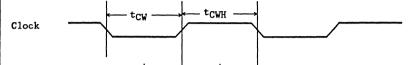


Page 11-56

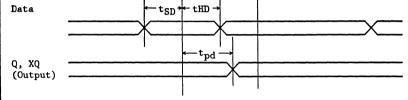
SFDS

Definitions of Parameters

i) Clock Mode

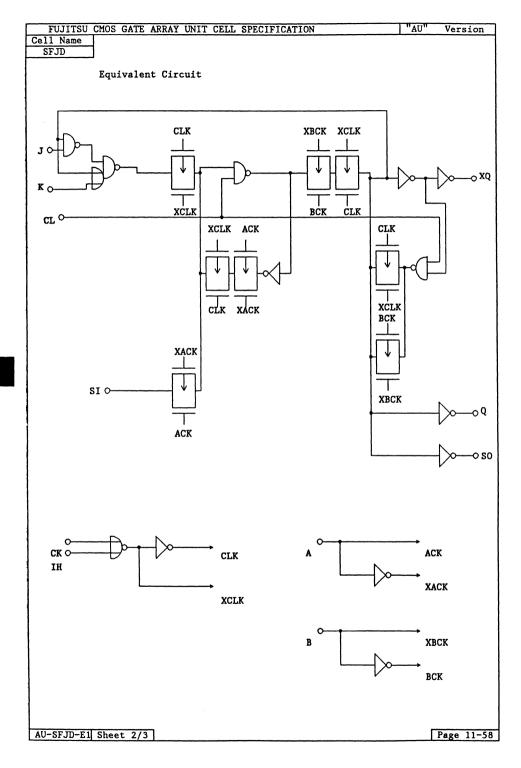


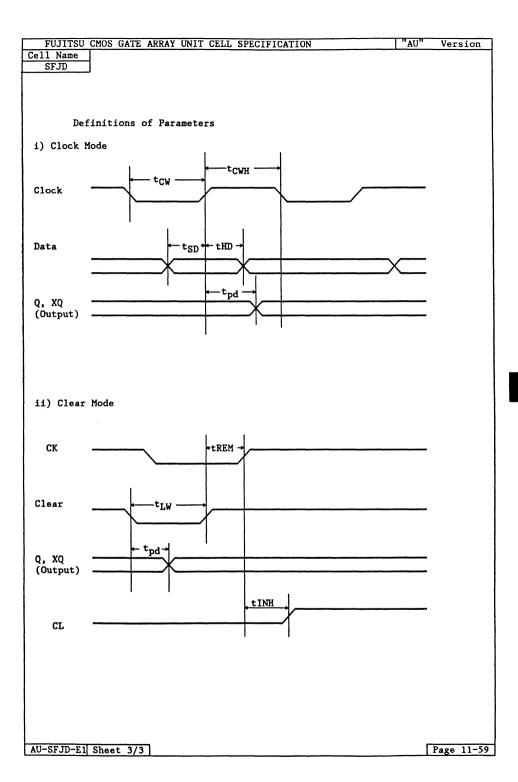
Data



AU-SFDS-E1 Sheet 4/4

FULLTSU C	MOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		"A1	U" Version
	Function	VIII ODD	B OI BOIL	TOMITO	·			Number of BC
SFJD	SCAN J-K FF wit	h Clock	Inhibi	t			i	14
Cell Symbol				agation	Delay		ter	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path
		2.59	0.14	2.40	0.10	0.16		CK → Q
		2.77	0.13	3.03	0.07	0.08		CK → XQ
		2.24	0.13	1.98	0.07	0.14	4	CL → Q,XQ
J —	├ Q							
к —	n vn						1	
CK -	о хо						1	
IH —								
SI —	so		1				1	
A							1	
В — 9_							1	
ļ	Ĭ	Parame	ter				Symbol	Typ(ns)*
	1	Clock	Pulse W	idth			tCW	4.0
	CL	Clock	Pause T	ıme			tCWH	4.0
		Data C	etup Ti	me (J)			tSD	3.0
		Data H	old Tim	e (J)			tHD	0.5
		Data II	OIG III	E (U)		-+		
	Input Loading	Data S	etup Ti	me (K)			tSD	2.6
Pin Name	Factor (lu)	Data H	old Tim	e (K)			tHD	0.1
J,K	1							
CK,IH	1	Clear	Pulse W	idth			tLW	4.0
SI	2	Clear	Release	Time			tREM	1.6
A,B	2	Clear	Hold Ti	me			tINH	3.5
CL	2 Output Driving	l						
Pin Name	Factor (lu)	ļ						
Q	18	l						
χQ	18							
so	18	* Mini	mum val	ues for	the ty	pical	operat	ing condition.
	]							ng condition
	<u> </u>	are	given b	y the m	aximum	delay	multip	lier.
1								
1								
1								
1								
1								
1								
1								
1								
}								1
AU-SFJD-E1 S	Sheet 1/3							Page 11-57





## Non Scan Flip-flop Family

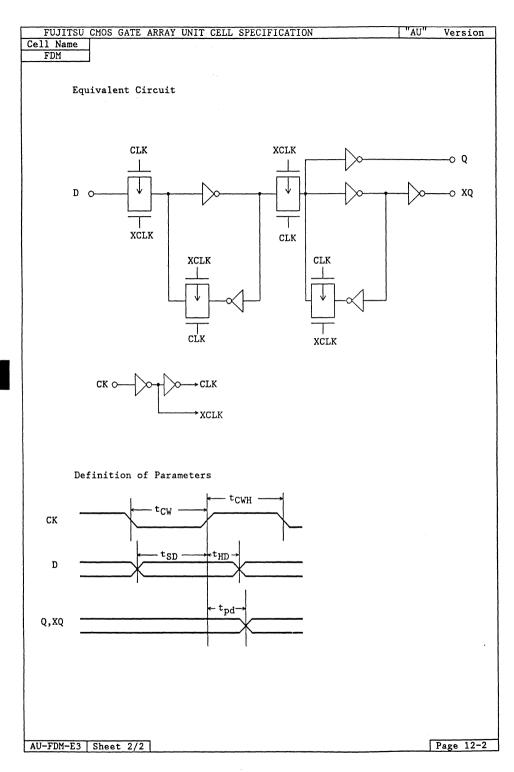
Page	Unit Cell Name	Function	Basic Cells
2-181	FDM	Non-Scan D Flip-flop	6
2-183	FDN	Non-Scan D Flip-flop with Set	7
2-185	FDO	Non-Scan D Flip-flop with Reset	7
2-187	FDP	Non-Scan D Flip-flop with Set and Reset	8
2-190	FDQ	Non-Scan 4-bit D Flip-flop	21
2-192	FDR	Non-Scan 4-bit D Flip-flop with Clear	26
2-195	FDS	Non-Scan 4-bit D Flip-flop	20
2-197	FD2	Non-Scan Power D Flip-flop	7
2-199	FD3	Non-Scan Power D Flip-flop with Preset	8
2-201	FD4	Non-Scan Power D Flip-flop with Clear and Preset	9
2-203	FD5	Non-Scan Power D Flip-flop with Clear	8
2–205	FJD	Non-Scan Positive Edge Clocked Power J–K Flip-flop with Clear	12

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
FDM	Non-SCAN DFF							6
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td	n		
ļ		t0	KCL	t0	KCL	KCL2	CDR2	
		1.40	0.13	1.44	0.07			CK → Q
	,	1.73	0.13	1.89	0.07			CK → XQ
р —— ск——	q xq							
		Parame					Symbol	
			Pulse W				tCW	4.0
l		Clock	Pause T	ime			tCWH	4.0
		Doto C	etup Ti				tSD	1.7
			old Tim				tHD	1.2
		Data II	OIG IIII				CIID	1.2
Pin Name D CK	Input Loading Factor (lu) 2 1							
Pin Name Q XQ	Output Driving Factor (lu) 18 18							
ΛŲ	10	The	values		worst	case or	erati	ing condition. ng condition plier.

## Function Table

Inputs	Outputs				
D CK	Q XQ				
H ↑ L ↑	H L L H				

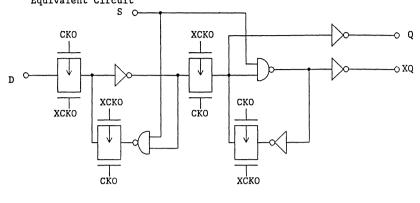
AU-FDM-E3 | Sheet 1/2



FUJITSU C	MOS GATE ARRAY L	NIT CEL	L SPECT	FICATIO	N		"A	U" Version
	Function		<u> D OIBOI</u>	1 1011110				Number of BC
FDN	Non-SCAN DFF wi	th SET						7
Cell Symbol			Prop up	agation	Delay td		er	
		t0 1.44 1.97	KCL 0.13 0.13	t0 1.40 1.94	KCL 0.07 0.07	KCL2 0.10	CDR2	CK → Q CK → XQ
D -	s q	1.79	0.13	0.86	0.07			$s \rightarrow q, xq$
ск —	р— хо							
		Parame	ter	L		ــــــ	ymbol	Typ(ns)*
			Pulse W	lidth			tCW	4.0
			Pause T				tCWH	4.0
		Data S	etup Ti	me			tSD	1.7
		Data H	old Tim	ie			tHD	1.2
	Input Loading	Sot Di	lse Wid	+ h			tSW	4.0
Pin Name	Factor (lu)	Set Re	lease T	ime (S)			tREM	0.3
D	2	Set Ho	ld Time				tINH	3.1
S CK	2 1							
Pin Name Q	Output Driving Factor (lu) 18	-						
XQ	18	The	values		worst	case of	perati	ing condition ng condition lier.
Function T	Table	_						
Inputs	Outputs							
S D C	CK Q XQ	_						
L X H H H L	X H L H L L H							

AU-FDN-E3 | Sheet 1/2

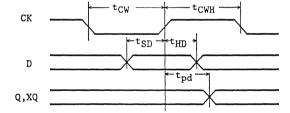
Equivalent Circuit

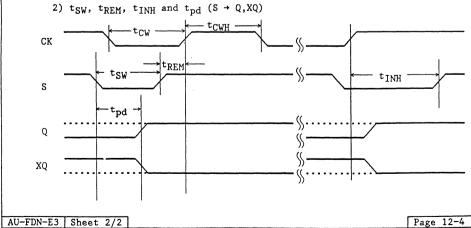


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

Definition of Parameters

1)  $t_{CW},\ t_{CWH},\ t_{SD},\ t_{HD}$  and  $t_{pd}$  (CK  $\rightarrow$  Q,XQ)



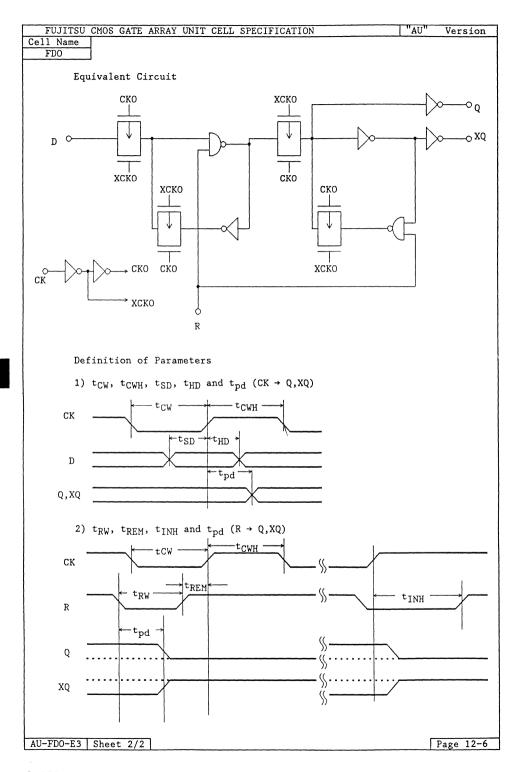


FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version	
Cell Name	Function							Number of BC	
FDO	Non-SCAN DFF wi	th RESE						7	
Cell Symbol				agation	Delay		er		
			up		td				
		t0	KCL	t0	KCL	KCL2	CDR2		
		1.55	0.13	1.43	0.08		ŀ	CK → Q	
		1.73	0.13	2.07	0.07			CK → XQ	
		1.60	0.13	1.31	0.08		l	$R \rightarrow Q, XQ$	
							l		
		1							
_ г		1					1	1	
D -	Q Q						1	Ì	
ск —							1		
1	р xq								
_	<del>-</del> <del>-</del> <del>-</del> <del>-</del> <del>-</del> -						1		
ł	•						<u> </u>		
	R	Parame					ymbol		
			Pulse W				tCW	4.0	
		Clock	Pause T	ime			tCWH	4.0	
1									
1			etup Ti				tSD	1.7	
		Data H	old Tim	e			tHD	1.2	
	γ								
	Input Loading		Pulse W				tRW	4.0	
Pin Name	Factor (lu)		Release		R)		tREM	0.8	
D	2	Reset	Hold Ti	me			tINH	2.7	
R	2	[						1	
CK	1	}				1			
1		1							
		1				1			
	Output Driving	1							
Pin Name	Factor (lu)								
Q	18								
XQ	18	1							
		* Minimum values for the typical operating condition.							
	The values for the worst case operating condition								
	<u></u>	are	given b	y the m	aximum	delay m	ultip	lier.	

## Function Table

I	nput	s	Ou	Outputs				
R	D	CK	Q	XQ				
L H H	X H L	X †	L H L	H L H				

AU-FDO-E3 | Sheet 1/2

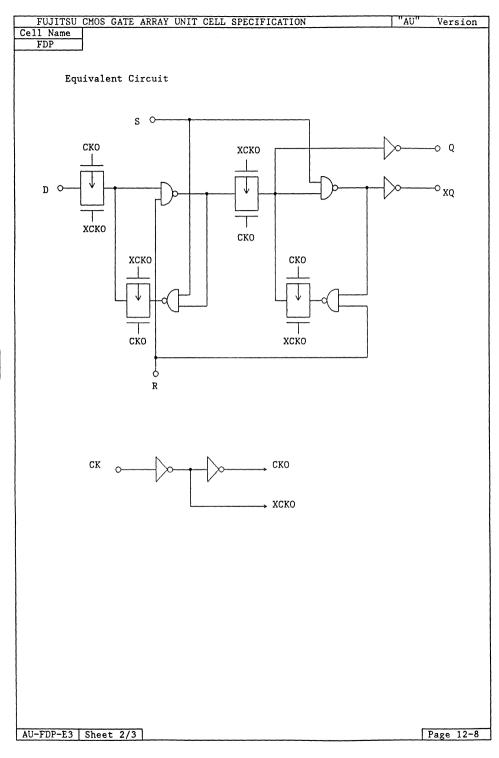


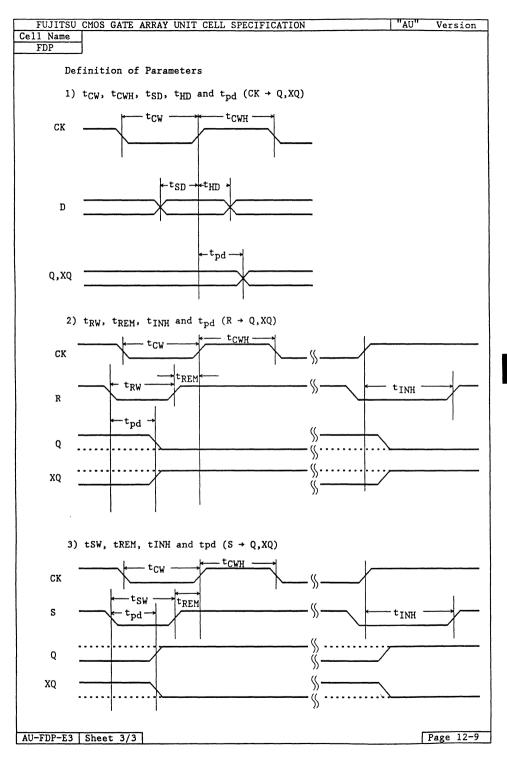
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version									
Cell Name	Function	Number of BC							
			·	***************************************					
FDP	Non-SCAN DFF wi	th Set	8						
Cell Symbol	1 Symbol Propagation Delay Parameter								
	tup tdn					<b>,</b>			
	t0	KCL	t0	KCL	KCL2	CDR2			
·s		1.57	0.13	1.41	0.08		ł	CK → Q	
		1.96	0.13		0.07		l	CK → XQ	
		1.79	0.13	1.27	0.08			$R \rightarrow Q, XQ$	
		2.03	0.13	0.81	0.07		1	$S \rightarrow Q, XQ$	
_		1					l	1	
D —									
ь	Q						}		
CK —		1						1	
	р xo	1					1	1	
L				İ			i		
	Y								
l R							]		
		Parameter				Is	ymbol	Typ(ns)*	
		Clock Pulse Width					tCW	4.0	
	Clock Pause Time t					tCWH	4.0		
	Data Setup Time tS					tSD	1.7		
		Data Hold Time					tHD	1.2	
	Input Loading						tSW	4.0	
Pin Name	Factor (lu)						tREM	0.3	
D	2	Set Ho	ld Time				tINH	3.1	
S	2								
						tRW	4.0		
CK	1						tREM	0.8	
	<del> </del>	Reset	Hold Ti	me			tINH	2.7	
D: 11	Output Driving								
Pin Name	Factor (lu)	4				1			
Q	18 18								
XQ	18	* Minimum values for the typical operating condition.							
		The values for the worst case operating condition.							
I	are given by the maximum delay multiplier.								
		are	graen p	y the m	avimmil	deray m	ur crp	11101.	

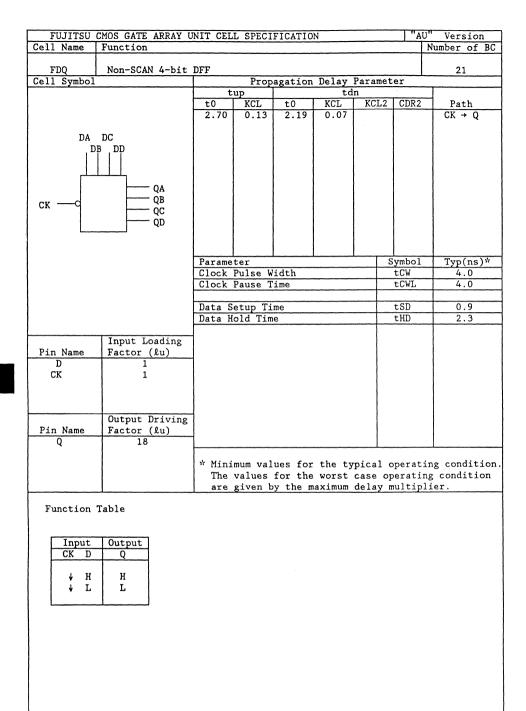
## Function Table

		Inpu	ts		Out	puts
	s	R	D	CK	Q	XQ
	Н	L	х	x	L	Н
1	L	H	Х	X	н	L
1	L	L	Х	X	Inhibited	
	H	H	Н	<b>↑</b>	н	L
	H	H	L	<b>↑</b>	L	H
					<u> </u>	

AU-FDP-E3 | Sheet 1/3

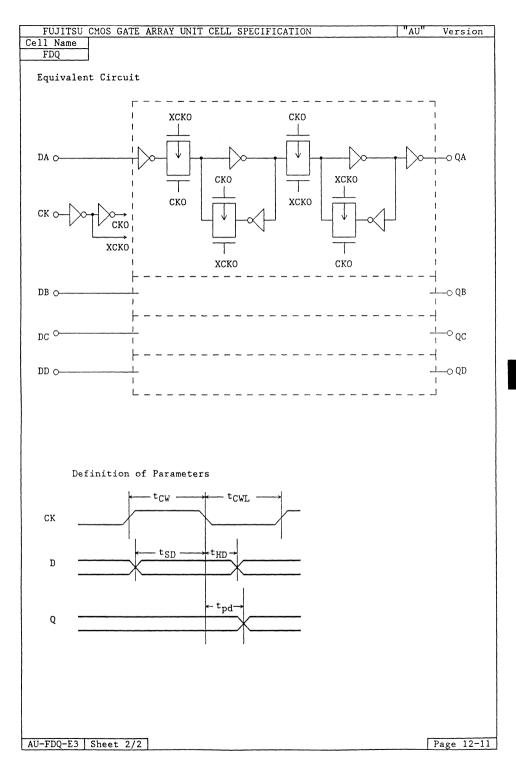






Page 12-10

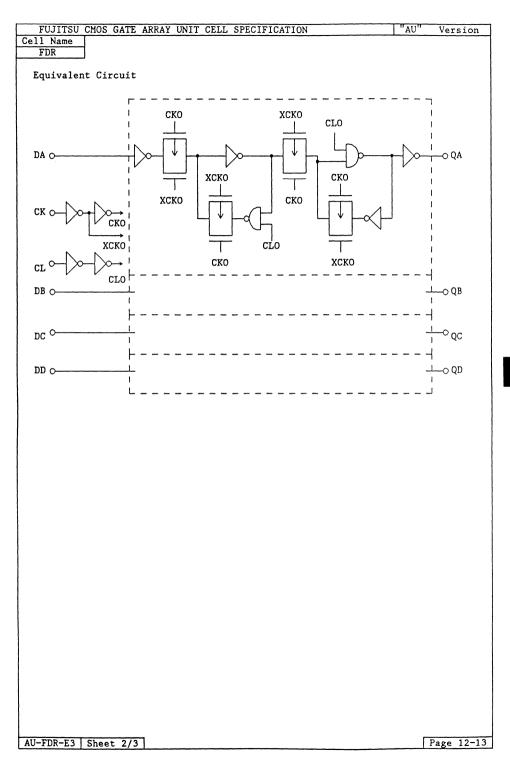
AU-FDQ-E3 | Sheet 1/2



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
FDR	Non-SCAN 4-bit	DFF wit						26
Cell Symbol				agation			ter	
			up		td		T	
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.11	0.13	2.90	0.07		1	CK → Q
70.4	7.0	-	-	1.75	0.07		1	CL → Q
DA							1	
ск —	QA QB QC QD		ter Pulse W Pause T				Symbol tCW tCWH	Typ(ns)* 4.0 4.0
		Data S	etup Ti	me			tSD	0.9
			old Tim				tHD	2.3
		- Dava A	010 111					
	Input Loading	Clear	Pulse W	idth			tLW	4.0
Pin Name	Factor (lu)		Release				tREM	1.2
D	1		Hold Ti				tINH	3.6
CK	1							
CL	1	}				1		
	Output Driving	1				1		
Pin Name	Factor (lu)					i		
Q	18			,				
	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

I	nputs	Output	
CK	D	CL	Q
X 1	X L H	L H H	L L H

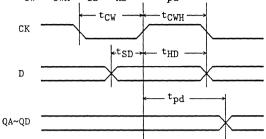
AU-FDR-E3 | Sheet 1/3



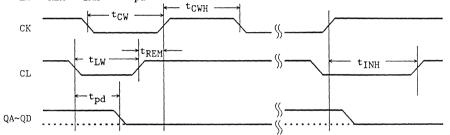
Page 12-14

Definition of Parameters

1)  $t_{\text{CW}},\ t_{\text{CWH}},\ t_{\text{SD}},\ t_{\text{HD}},\ \text{and}\ t_{\text{pd}}$  (CK+QA~QD)

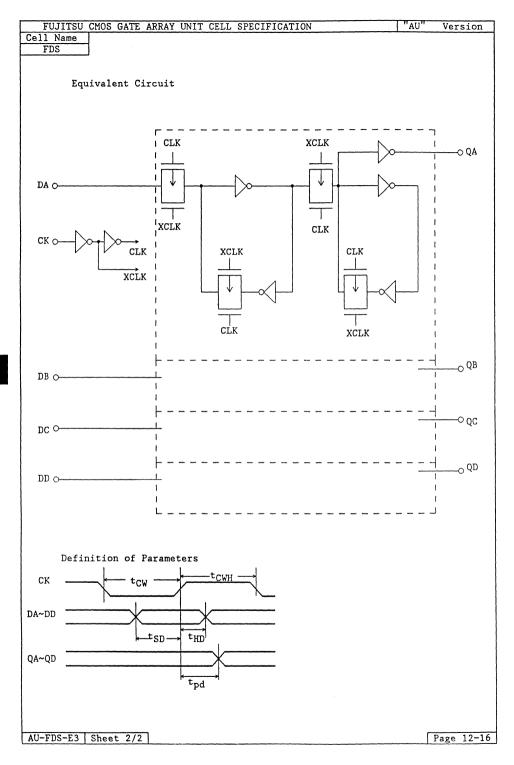


2)  $t_{LW},~t_{REM},~t_{INH}~and~t_{pd}~(CL \rightarrow QA \sim QD)$ 



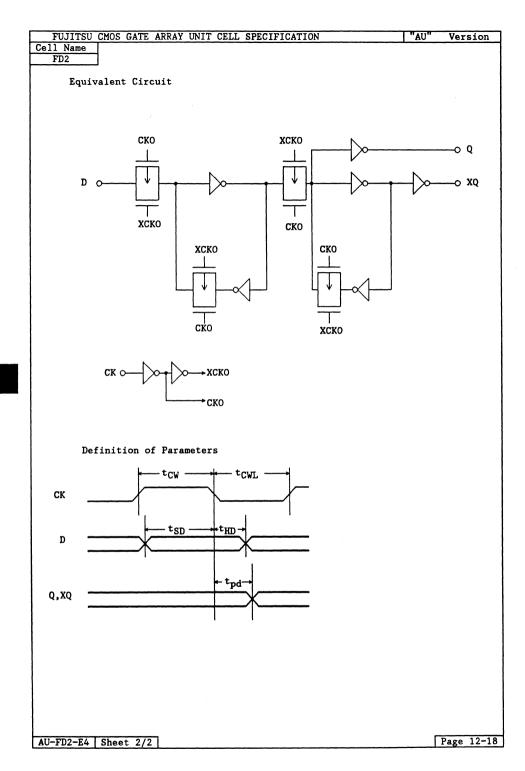
AU-FDR-E3 | Sheet 3/3

FUI	ITSU (	CMOS GATE ARRAY	INIT CFI	I. SPECT	FICATIO	N		Ι 11 Δ1	J" Version
Cell N		Function	ONTI CLL	I BILOI	FICALIO	14			Number of BC
FDS	rmb o 1	Non-SCAN 4-bit	DFF	D		Dalan	Damamat		20
Cell S	ymool		+ +	up Prop	agacion	Delay td		EI	
			t0	KCL	t0	KCL	KCL2	CDR2	Path
			2.43	0.13	1.96	0.07			CK → Q
								Ì	
	DA 1	DB DC DD							
				!					
	1	QA	į					1	
CK		QB QC							
O.K		☐ QD						ŀ	
			Parame	tor	L	L	1	ymbol	Typ(ns)*
				Pulse W	idth	·		tCW	4.0
				Pause T				tCWH	4.0
			Data S	etup Ti Old Tim	me			tSD tHD	0.9
			Data n	1010 1111	е			LUD	2.0
		Input Loading	7						
Pin N		Factor (lu)	_						
D CK		2	İ				}		
CK		1	-						
1			Ì						
		Output Driving	_				1		
Pin N	ame	Factor (lu)	3						
Q		18							
				_	_	_			
			* Mini	mum val	ues for	the ty	pical o	perat:	ing condition. ng condition
			are	given b	v the m	naximum	delay n	ultip	lier.
				<u></u>	· · · · · ·				
Func	tion '	Table							
Inp	uts	Outputs							
CK	D	Q							
	L	L							
	Н	н							
1									
AU-FDS	-E3	Sheet 1/2							Page 12-15



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
	Function							Number of BO
FD2	Non-SCAN Power	DFF						7
Cell Symbol				agation			eter	
			up		td		a Lanna	┥
		1.32	KCL 0.07	t0 1.38	KCL 0.04	KCI 0.0		Path CK → Q
		2.04	0.07	1.87	0.03	0.0		CK → XQ
						1	İ	
							- [	
D —	Q						İ	
ск-—		<u> </u>						
1	þ <b>x</b> Q						1	İ
L	`						İ	
							1	
							1	
		Parame	ter	L		<del>!                                    </del>	Symbol	Typ(ns)*
			Pulse W	idth		$\neg \neg$	tCW	4.0
			Pause T				tCW	4.0
		Data S	etup Ti old Tim	me		$-\!\!\!+$	tSD tHD	1.7
		Data II	Old IIm	<u> </u>		-+	<u>tin</u>	1.2
	Input Loading	1				[		1
Pin Name	Factor (lu)					- 1		
D	2					- 1		
CK	1	ļ						1
						- 1		
						1		1
	Output Driving	1						
Pin Name	Factor (lu)	1				l		
Q XQ	36 36							
AQ	]	* Mini	mum val	ues for	the to	roica1	operat	ing condition
		The	values	for the	worst	case	operati	ng condition
	<u> </u>	are	given b	y the m	aximum	delay	multip	lier.
Function 7	Table							
runction .	IADIC							
Inputs	Outputs							
CK 1	D Q XQ							
1.1.	.   .   .							
, , ,	H   H   L   L   L   H							
'   '								
·								

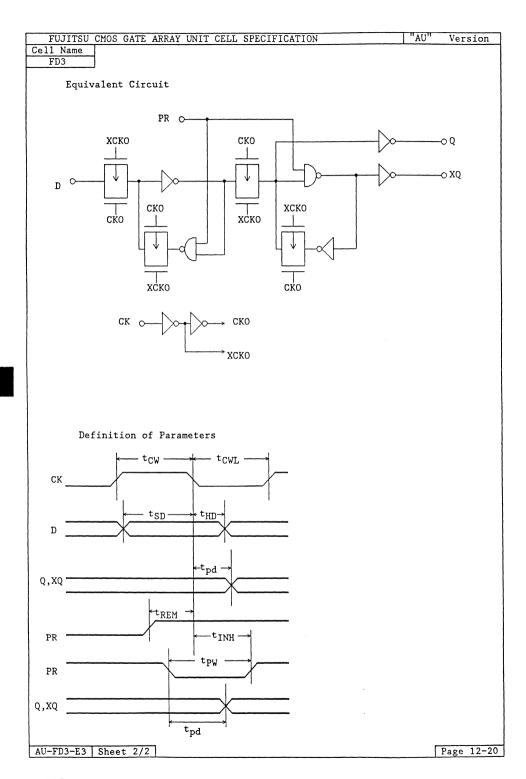
AU-FD2-E4 | Sheet 1/2 | Page 12-17



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		l "A	U" Version
Cell Name	Function							Number of BC
FD3	Non-SCAN Power	DFF wit						8
Cell Symbol		ļ		agation			er	<del></del>
			up		td		CDDO	⊣
		t0	KCL	t0	KCL	KCL2	CDR2	
PR		1.37	0.05	1.39	0.03	0.08	7	CK → Q
	PK	2.24	0.05	2.00	0.03	0.06	7 7	CK → XQ
D	Q	1.91	0.05	0.73	0.03	0.06		PR → Q,XQ
ск——	хо				,			
	Parameter Symbol Clock Pulse Width tCW Clock Pause Time tCWI					4.0		
		Clock Pause Time						4.0
			· m·				+ CD	<del></del>
			etup Ti old Tim			tSD	1.7	
		Data H	010 11m	e			LUD	1.2
	Input Loading	Preset	Pulse	Width			tPW	4.0
Pin Name	Factor (lu)	Preset	Releas	e Time			tREM	0.3
D	2	Preset	Hold T	ime			tINH	3.1
CK PR	1 2							
		1						
Pin Name	Output Driving Factor (lu)							
Q Q	36	1						
xQ	36							ing condition
								ng condition
	<u> </u>	are	given b	y the m	aximum	delay n	nultip	olier.

	Inputs	Outputs		
PR	CK	D	Q	XQ
L H H	X ↓	X H L	H H L	L L H

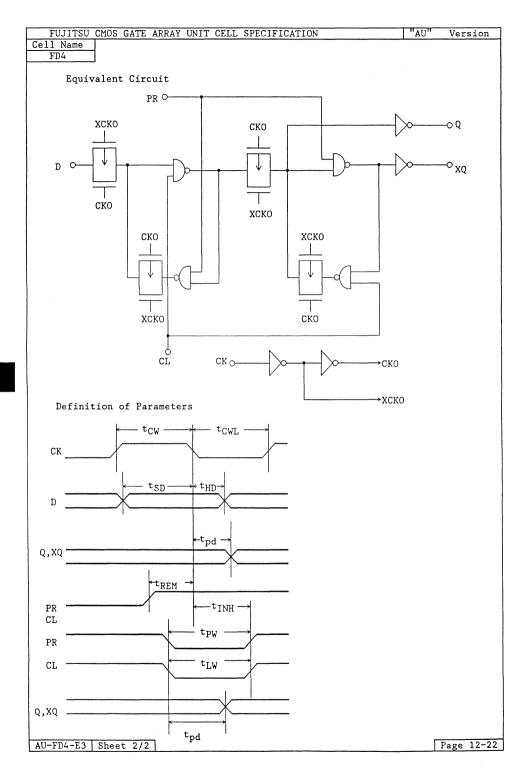
AU-FD3-E3 | Sheet 1/2



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
FD4	Non-SCAN Power	DEE wit	h Clear	and Pr	oset			9
Cell Symbol	NOII BOAN TOWEL	DII WIL		agation		Paramet	er	L
ocii bymboi		+	up	agacion	td	n		<del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.52	0.06	1.38	0.04	0.08	7	
ī	PR .	2.25	0.05		0.03	0.06	7	CK → XQ
-	1	1.98	0.05			0.08	7	CL → Q,XQ
		1.99	0.06	0.74	0.03	0.06	7	PR → Q,XQ
	<u>م</u>							, ,,,,
D	Q						1	
<b>5</b> 77.	`						1	
ск——			,				1	
ļ	р xo							
L	<del>_</del>							
							1	
(	CL							ļ
,	20						i	
		Parame	ter				ymbol	Typ(ns)*
		Clock Pulse Width					tCW	4.0
		Clock Pause Time					tCWL	4.0
			etup Ti				tSD	1.7
		Data H	old Tim	e			tHD	1.2
	<b>4</b>							
	Input Loading		Pulse				tPW	4.0
Pin Name	Factor (lu)		Releas				tREM	0.3
D	2	Preset	Hold T	ime			tINH	3.1
CK	1		D 1 1	1.1.1.			+T 1.7	
CL	2		Palse W				tLW	4.0
PR	2	Clear Release Time tREM Clear Hold Time tINH					0.8	
	Out-ut Duday	Clear	HOLD II	me			tINH	2.7
Din Name	Output Driving	ĺ						
Pin Name Q	Factor (lu)	-						
Q XQ	36	<b></b>						
ΛŲ	30	* Mini	miim 17.01	nes for	the +**	nical c	norat	ing condition
								ing condition
				y the m				
	<u> </u>	l are	Proci p	y che ili	antinuili	uciay I	14161	,1101 .

	Inp	Out	puts		
PR	CL	CK	D	Q	XQ
L H H	H L H H	X X *	X H L	H L H L	L H L H

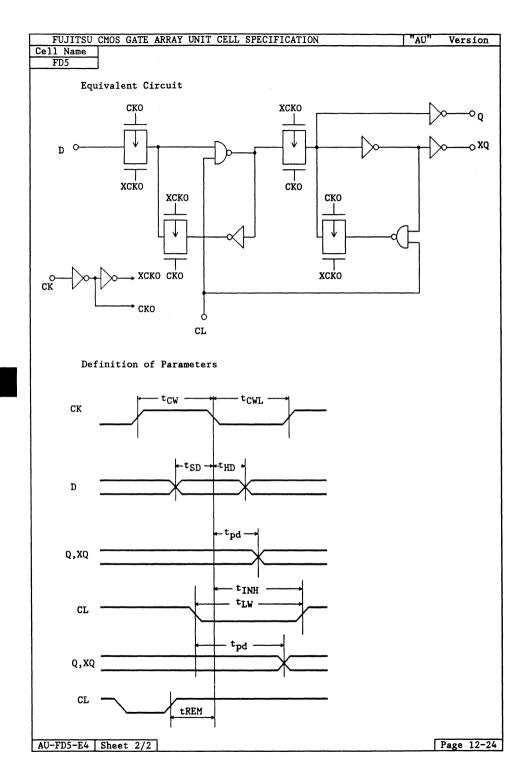
AU-FD4-E3 | Sheet 1/2



FULLTSU	CMOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		Ι "Δ	U" Version
Cell Name	Function	TITE ODD	D DI DOI	TIONITO	11			Number of BC
FD5	Non-SCAN Power	DFF wit	h CLEAR					8
Cell Symbol				agation	Delay	Param	eter	
		t	up		td			
1		t0	KCL	t0	KCL	KCL		
		1.51	0.07	1.37	0.04	0.0		CK → Q
		2.06	0.07	2.06	0.03	0.0		CK → XQ
		1.89	0.07	1.22	0.04	0.0	8 7	CL → Q,XQ
							}	
			1				1	
D —	Q							
Ск——								
1 "			İ					
1	р <del></del> хо		l					
	φ							
1	ı	İ			1			
1	CL							
		Parame					Symbol	
		Clock Pulse Width					tCW	4.0
		Clock Pause Time					tCWL	4.0
l		D					tSD	<del>-  </del>
ļ			etup Ti				tHD	1.7
		Data H	old Tim	е			THD	1.2
	Input Loading	C100=	Pulse W	1 d+ h			tLW	4.0
Pin Name	Factor (lu)		Release			-+	tREM	1.2
D D	Pactor (ku)		Hold Ti				tINH	3.6
СК	1	Clear	noru 11	шс			CTM	<del>  3.0</del>
CL	2							
CL CL						i		
								1
	Output Driving	1				i		
Pin Name	Factor (lu)	1				- 1		i
Q	36	1						
χQ	36							
		* Mini	mum val	ues for	the tv	pical	operat	ing condition.
								ing condition
are given by the maximum delay multiplier.								

	Input	Outputs		
CL	CK	D	Q	XQ
L H H	х +	X H L	L H L	H L H

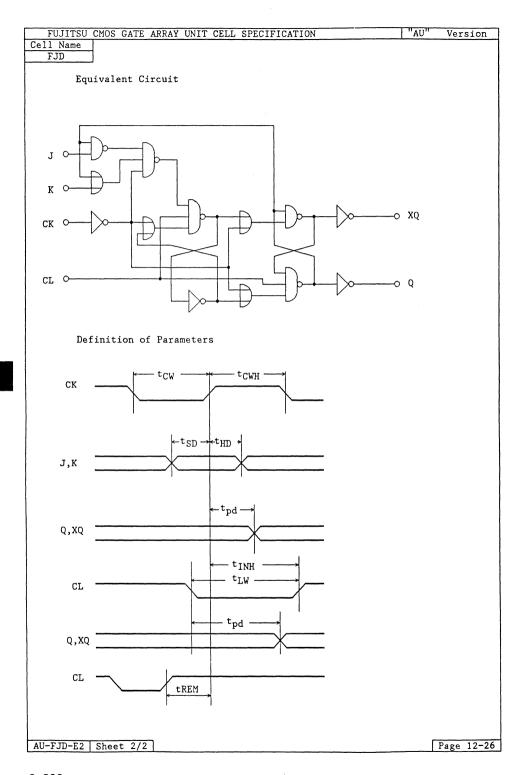
AU-FD5-E4 | Sheet 1/2



Number of BC   Number of BC	FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		Т "A	U" Version
FJD			····· ODD	<u>D DI BOI</u>	11011110	• `		1	
Tup			ve edge	clocke	d Power	JKFF w	ith Cle	ar	
CL	Cell Symbol				agation			er	
Symbol   Typ(ns)*									
Symbol   Typ(ns)*									
CL								1	
CK			•						
CK			1.92	0.07	1.03	0.04	0.07	′	$CL \rightarrow Q, XQ$
CK									
Clock Pulse Width   tCW   4.5	ск —								
Clock Pulse Width		CL	Parame	ter		· · · · · · · · · · · · · · · · · · ·	S	ymbol	Typ(ns)*
J,K Setup Time			Clock	Pulse W	idth			tCW	
J,K Hold Time			Clock Pause Time					tCWH	4.5
J,K Hold Time	]								
Input Loading   Factor (2u)   Clear Pulse Width   tLW   4.0									
Pin Name         Factor (lu)         Clear Release Time         tREM         2.0           CL         2         Clear Hold Time         tINH         3.6           K         1         CK         1           CK         1         Output Driving Factor (lu)         Factor (lu)           Q         36         36           XQ         36           XQ         * Minimum values for the typical operating condition.           The values for the worst case operating condition			J,K Ho	ld Time				tHD	1.0
Pin Name         Factor (lu)         Clear Release Time         tREM         2.0           CL         2         Clear Hold Time         tINH         3.6           K         1         CK         1           CK         1         Output Driving Factor (lu)         Factor (lu)           Q         36         36           XQ         36           XQ         * Minimum values for the typical operating condition.           The values for the worst case operating condition	<b> </b>	Input Inadina	Class	D. 1 !/	i al + la			+T 1.7	4.0
CL 2 Clear Hold Time tINH 3.6  I 1	Pin Name								
J 1 1 1 1 CK 1 1									
K 1 1		-							
Pin Name Factor (lu)  Q 36  XQ 36  * Minimum values for the typical operating condition. The values for the worst case operating condition	K	1							
Pin Name Factor (Lu)  Q 36  XQ 36  * Minimum values for the typical operating condition.  The values for the worst case operating condition	CK	1							
Pin Name Factor (Lu)  Q 36  XQ 36  * Minimum values for the typical operating condition.  The values for the worst case operating condition							1		
Q 36 XQ 36  * Minimum values for the typical operating condition. The values for the worst case operating condition		Output Driving	]						
XQ 36  * Minimum values for the typical operating condition. The values for the worst case operating condition			]						
* Minimum values for the typical operating condition. The values for the worst case operating condition		l .							
The values for the worst case operating condition	XQ	36							
The values for the worst case operating condition are given by the maximum delay multiplier.									
are given by the maximum delay multiplier.			The	values	for the	worst	case op	erati	ng condition
		<u></u>	are	given b	y the m	aximum	delay m	ultip	lier.

	Inp	uts		Outputs
CL	CK	J	K	Q XQ
L H H H	X † †	X L L H	X L H L	L H Q <sub>0</sub> XQ <sub>0</sub> L H H L XQ <sub>0</sub> Q <sub>0</sub>

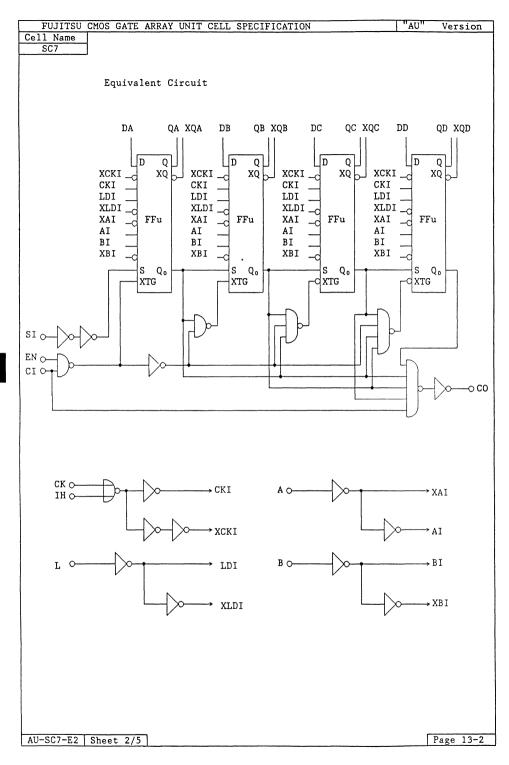
AU-FJD-E2 | Sheet 1/2

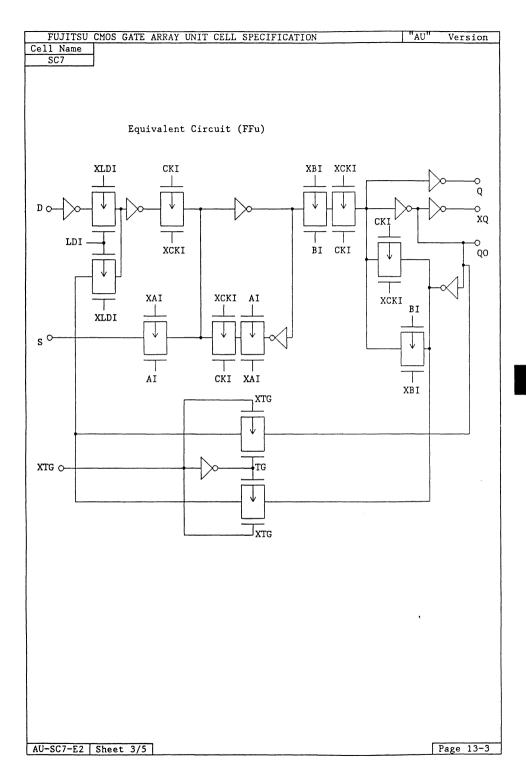


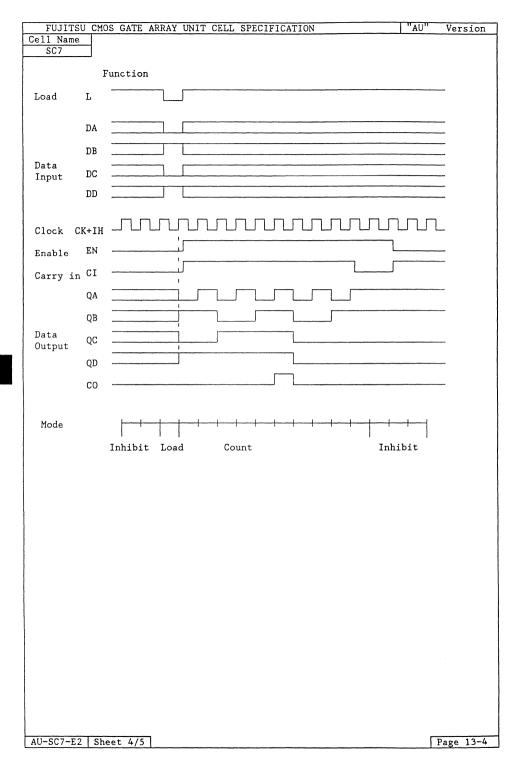
# **Binary Counter Family**

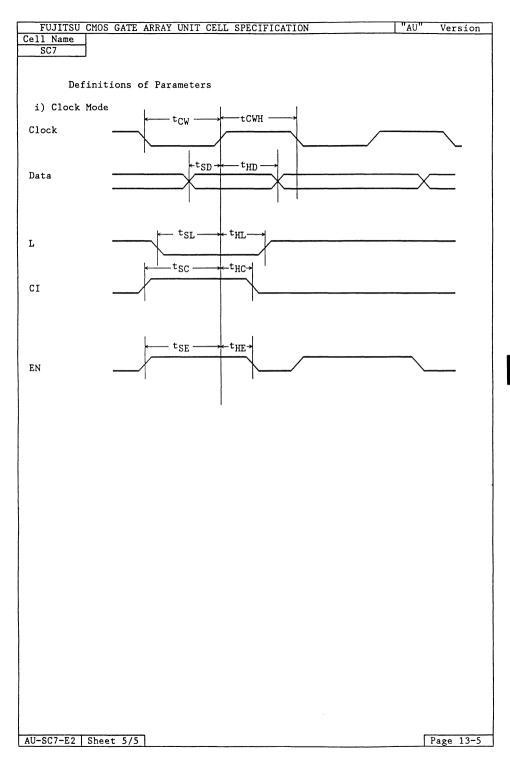
Page	Unit Cell Name	Function	Basic Cells
2–209	SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62
2–214	SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load 66	
2-219	C11	Non-Scan Flip-Flop for Counter	11
2-221	C41	Non-Scan 4-bit Binary Asynchronous Counter	24
2-224	C42	Non-Scan 4-bit Binary Synchronous Counter	32
2-227	C43	Non-Scan 4-bit Binary Synchronous Up Counter	48
2-231	C45	Non-Scan 4-bit Binary Synchronous Up Counter	48
2-235	C47	Non-Scan 4-bit Binary Synchronous Up/Down Counter	68
2–239	SC43	Scan 4-bit Synchronous Binary Up Counter with Asynchronous Clear	59
2-243	SC47	Scan 4-bit Synchronous Binary Up/Down Counter	78

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	U" Version
Cell Name								
SCAN 4-bit Synchronous Binary SC7 Up Counter with Parallel Load 62							(0)	
SC7 Cell Symbol	op counter with	Parall	el Load	agation	Dolor	Daramo	<u> </u>	62
Cell Symbol		+-	up	agation	td		rei	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.64	0.07	2.44	0.05	0.12		CK, IH → Q
		4.63	0.07	4.27	0.05	0.12	1	CK,IH → XQ
		6.24	0.07	4.19	0.03	_	-	CK,IH → CO
DA -		1.60	0.07	0.08	0.03	_	-	CI → CO
DB -	QA						1	
DC —	P—— XQA							1
DD -	QB VOD						ı	
CV	р—— хов						Į.	
CK —	P—— QC	i l						
L —	QD QD							
cı —	⇒—— xQD	Parame					Symbol	Typ(ns)*
EN -	1		Pulse W				tCW	5.8
sı —	co	CTOCK	Pause T	тше			tCWH	5.8
Α		Data S	etup Ti	me			tSD	1.6
В — 9			old Tim				tHD	2.7
		<del></del>						
		Load S	etup Ti	me			tSL	5.1
		Load H	old Tim	e			tHL	2.9
	<b>,</b>							
Dia Na	Input Loading	CI Setup Time					tSC tHC	5.8
Pin Name D	Factor (lu)	Ru) CI Hold Time						2.2
CK	1	EN Setup Time						5.8
IH	1	EN Hol		tSE tHE	2.2			
L	1							
CI	2					l		
EN	1					-		
SI	1					l		
A,B	1					1		
-	Output Driving					ı		
Pin Name	Factor (lu)							
Q	36							
XQ	36							
CO	36							ing condition.
		The values for the worst case operating condition are given by the maximum delay multiplier.						
	L	are	given b	y the m	axımum	delay	multip	iier.
1								
AU-SC7-E2   S	Sheet 1/5							Page 13-1
NO 001 12   3	meer 1/3							l rage 13 1

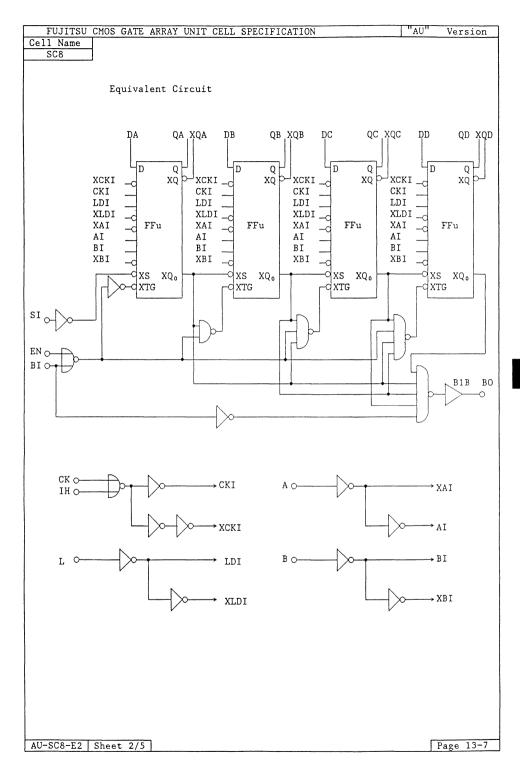


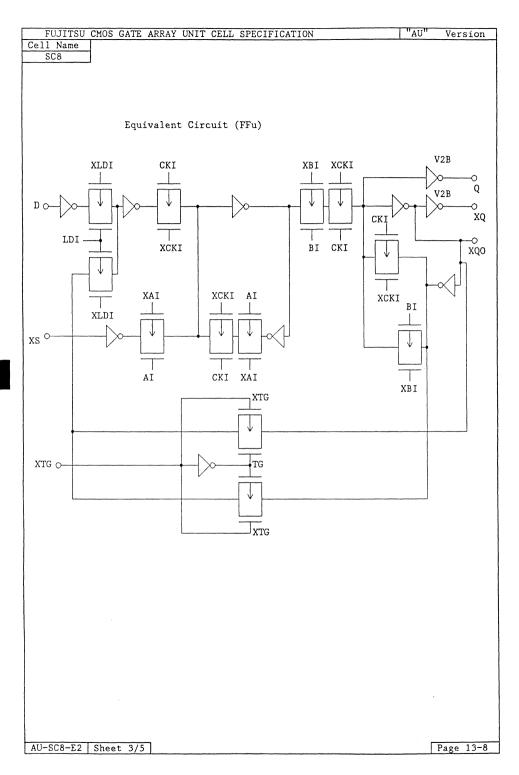


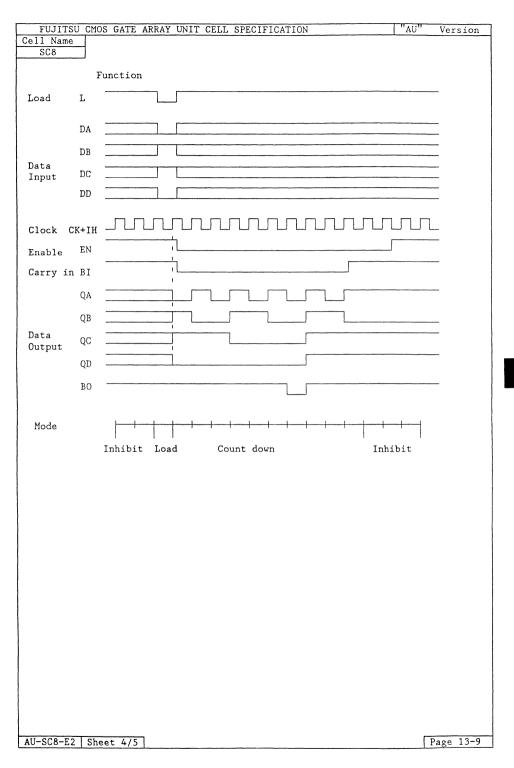


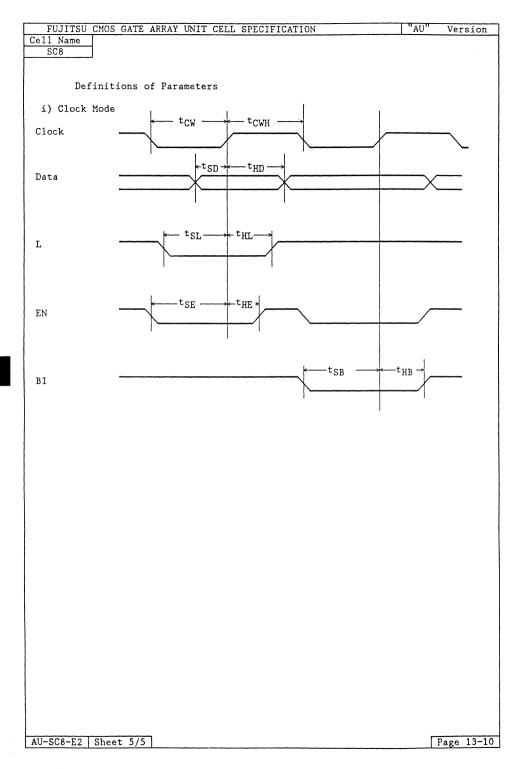


FUJITSU C	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		T"A	U" Version	
Cell Name	Function							Number of BC	
	SCAN 4-bit Sync	hronous	Binary						
SC8	Down Counter wi	th Para	llel Lo	ad				66	
Cell Symbol	Cell Symbol Propagation Delay Parameter tup tdn								
		t0	up KCL	t0	KCL	n KCL2	CDR2	Path	
		2.70	0.06	2.55	0.05	0.11	7	CK, IH → Q	
		3.52	0.05	3.46	0.03	0.11	'	CK,IH → XQ	
		5.13	0.07	6.70	0.03			CK, IH → BO	
DA		1.19	0.07	1.82	0.03			BI → BO	
DB -	QA VQA								
DC -	QB QB						<b> </b>		
DD -	р								
CK -	QC								
IH —	P xQC						l	1	
L —o	QD YOR	Parame	ter	L		S	ymbol	Typ(ns)*	
BI ——	р хор	Clock	Pulse W				tCW	5.5	
si —	b во	Clock	Pause T	ime			tCWH	5.5	
A			- + · · · · · · · · · · · · · · · · · ·				+CD	1	
в ——		Data S	etup Ti old Tim	me			tHD	1.6	
		Data n	<u> </u>				CIID		
		Load S	etup Ti	me			tSL	5.1	
		Load H	old Tim	е			tHL	2.9	
Dia Nama	Input Loading		up Time				tSE tHE	6.5	
Pin Name D	Factor (lu)	EN Hold Time						1.5	
CK CK	1	BI Setup Time t					tSB	6.5	
IH	1	BI Hold Time					tHB	1.5	
L	1								
BI	2							}	
EN SI	1 1								
A,B	1								
1 ","	1					1			
	Output Driving	1							
Pin Name	Factor (lu)	j				- 1			
Q	36								
XQ BO	36 36	* M:	mum *** 1	1105 for	the +	nicol -	no==+	ing condition.	
100	]							ng condition.	
		are	given b	y the m	aximum	delay n	ultip	lier.	
	· · · · · · · · · · · · · · · · · · ·	·							
1									
1									
1									
AU-SC8-E2	Sheet 1/5							Page 13-6	
.10 000 12	011066 1/3							11060 13 0	



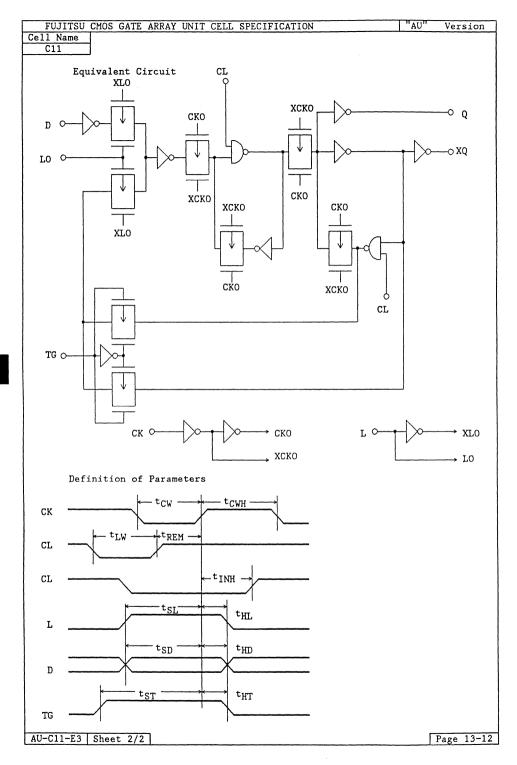






C	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version											
Ce	Cell Name Function Number									Number of BC		
	C11 Non-SCAN Flip-Flop for Counter 11									11		
Ce	11 Sy	mbol						agation			er	
l							up		td		GDDA	
Ì						t0 1.52	KCL 0.13	t0 1.40	KCL 0.08	KCL2	CDR2	Path CK → Q
						2.03	0.13	2.38	0.08			CK → VQ
						2.10	0.13	1.39	0.08			CL → Q,XQ
İ							0.120	1.00				32 4,
į		Г										
	D -	$\neg$										
	L -		Ī	—— Q		1						
	CK -		[								1	
	OIL	į	1								ł	
ļ	TG -		þ	— х	Q							
}			- 1									
į			9			Parame					ymbol	
1			1				Pulse W				tCW tCWH	4.0
			CL			Clock	Pause T	ıme			tcwn	4.0
						Clear	Pulse W	lidth			tLW	4.0
							Release				tREM	0.8
						Clear Hold Time					tINH	0.4
				t Loa								
P	in Na	me	Fact	or (l	u)	Load Setup Time (CK)					tSL	1.9
	L TG			2		Load Hold Time (CK)					tHL	0.4
1	CL		ł	2		Data S	Data Setup Time (CK)					2.0
1	D,CK 1				Data Hold Time (CK) tH						0.4	
,	de Na	<b></b>	Outp	ut Dr	iving		up Time			tST	2.4	
F	in Na Q	me	ract	or (l	<u>u)</u>	TG Hold Time (CK) tHT 0.0						
	ΧQ			18		<b></b>						
1	•					* Minimum values for the typical operating condition.						
			}			The values for the worst case operating condition are given by the maximum delay multiplier.						
<u> </u>			L			are	given b	y the m	aximum	delay m	ultip	olier.
1	Funct	ion T	abla									
	1 dile t	1011 1	abic									
			1				7					
	L	D	TG	CL	CK	Q(Q <sub>0</sub> )	-					
	<b></b>	<b></b> -		-		-	-					
	Х	Х	X	L	X	L	1					
	н	н	х	н	<b>1</b>	н						i
		-				"						
	н	L	Х	Н	1	L						
	١.	١	١.	٠	,							
	L	Х	L	Н	<b>↑</b>	Q(Q <sub>0</sub> )						
	L	x	н	н	<b>^</b>	$\overline{\mathbb{Q}}(\overline{\mathbb{Q}_o})$						!
	L	"	l .			((40)						:
1												

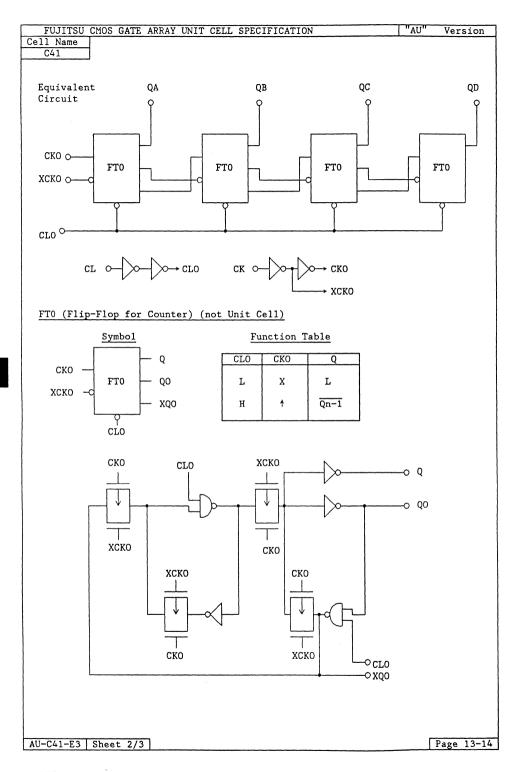
AU-C11-E3 | Sheet 1/2



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function Number of BC							
C41 Cell Symbol	Non-SCAN 4-bit Binary Asynchronous Counter 24 Propagation Delay Parameter							
Cell Symbol				agation	Delay td		er	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path
		1.60	0.11	1.49	0.08	- 10002	- ODKZ	CK → QA
		2.94	0.11	2.63	0.08	_	_	CK → QB
		4.11	0.11	3.80	0.08	_	_	CK → QC
		5.28	0.11	4.96	0.08	_	] _	CK → QD
_		-	-	3.35	0.08	_	_	CL → Q
ск ——	——— QA ——— QB ——— QC ——— QD							
L		Parame					ymbol	Typ(ns)*
	Y	Clock Pulse Width					tCW	4.0
	1	Clock Pause Time					tCWH	4.0
	CL	Clock Tadse Time						
		Clear Pulse Width					tLW	4.0
		Clear Release Time					tREM	1.7
	Input Loading	Clear	Hold Ti	me			tINH	5.4
Pin Name	Factor (lu)							
CK CL	1 1							
OD.	1							
	Output Driving	1						
Pin Name	Factor (lu)							
Q	18							
		* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.						
	J	are	Erven D	y the in	antillulli	ueray II	итстр	1101.

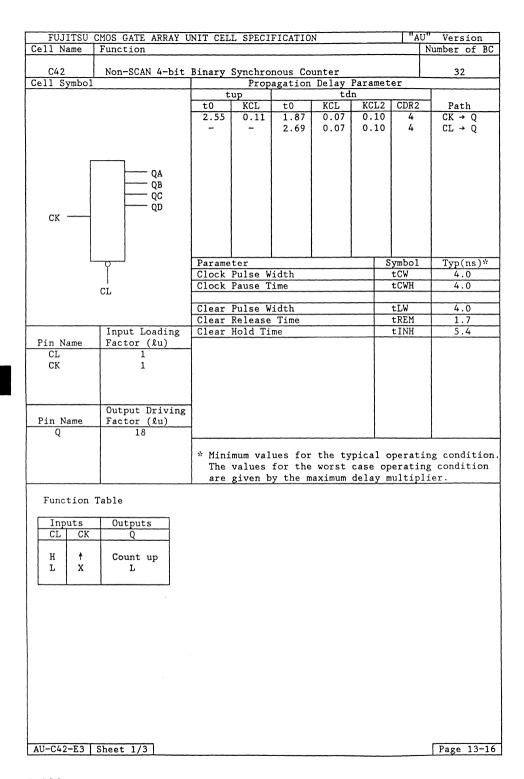
AU-C41-E3 | Sheet 1/3

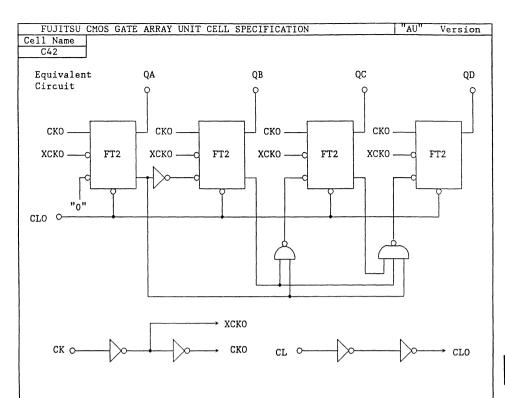
Inp	uts	Outputs				
CL	CK	Q				
H L	↑ X	Count up L				



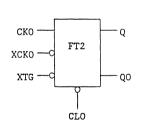
"AU" FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION Version Cell Name C41 Definition of Parameters -t<sub>REM</sub>→  $t_{INH}$ 

AU-C41-E3 | Sheet 3/3







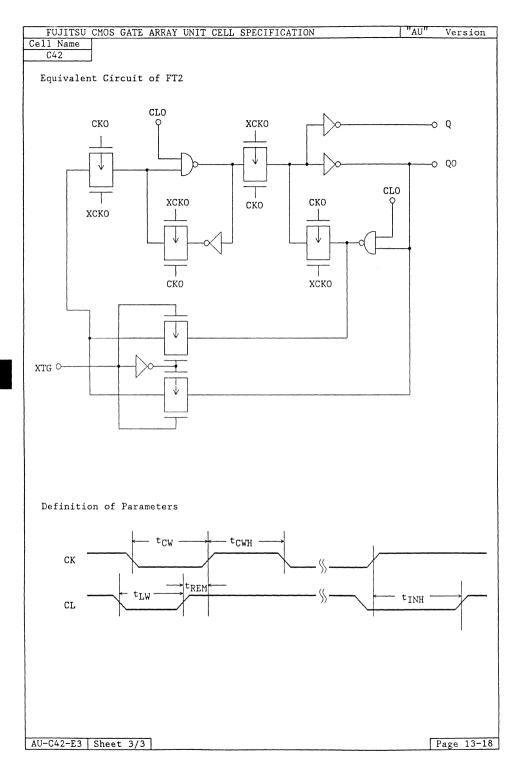


Symbol

Function Table

	Inputs							
CLO	XTG	Q(Q0)						
L	х	Х	L					
н	н	<b>↑</b>	Qn-1					
н	L	<b>↑</b>	Qn−1					

AU-C42-E3 | Sheet 2/3

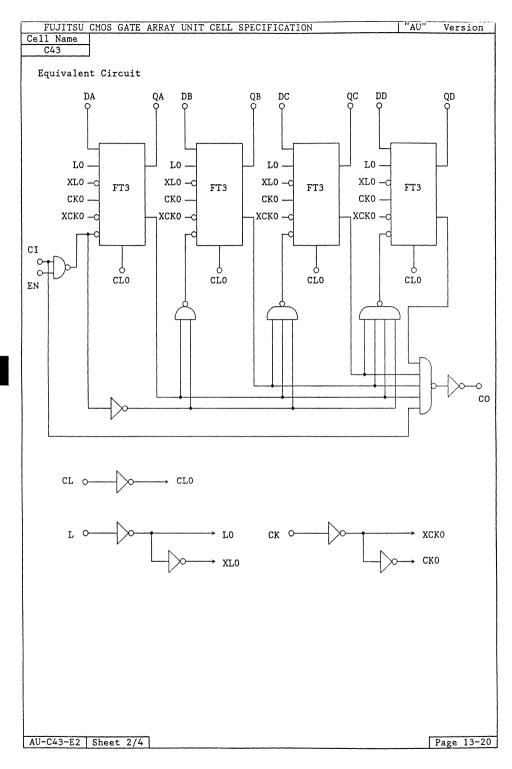


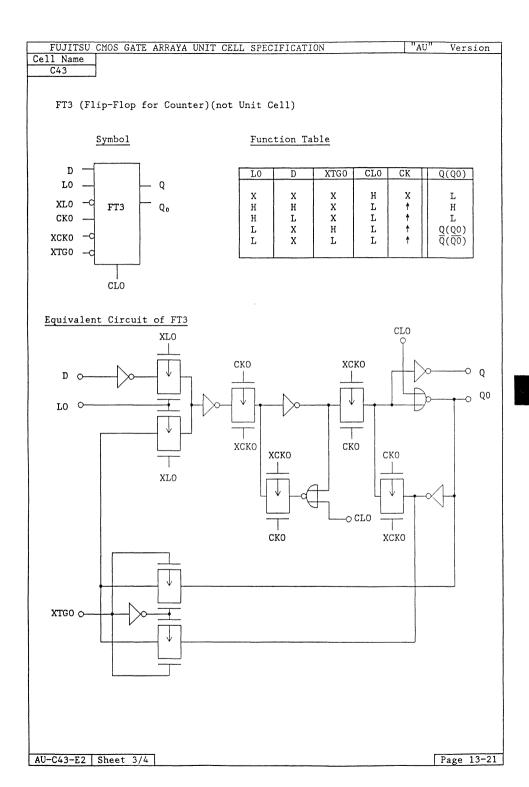
FUJITSU	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version								
Cell Name	Function							Number of BC	
C43	Non-SCAN 4-bit Binary Synchronous Up Counter 48								
Cell Symbol			Prop	agation	Delay	Paramet	er		
		t	up		td				
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		2.37	0.13	1.92	0.07			CK → Q	
		4.48	0.13	2.85	0.07		1	CK → CO	
		1.28	0.13	0.65	0.07		1	CI → CO	
		-	-	3.11	0.07		1	CL → Q	
Г		-	-	2.11	0.07			CL → CO	
DA -	QA						1		
DB —	├ QB						1		
DC -	QC								
DD —	QD								
L							1		
ск —							i		
EN —							l		
ci —	co						1		
"		Parame	ter			<u> </u>	Symbol	Typ(ns)*	
	Ī	Clock Pulse Width					tCW	4.0	
	1	Clock Pause Time					tCWH	5.4	
	CL	Data S	etup Ti	me		tSD	2.1		
			old Tim			tHD	2.4		
		Load S	etup Ti	me		tSL	3.6		
	Input Loading		old Tim				tHL	1.1	
Pin Name	Factor (lu)		up Time				tSC	3.5	
D	1		d Time				tHC	0.8	
L,EN	1		up Time				tSE	3.5	
CK,CL	1		d Time				tHE	0.8	
CI	2		Pulse W				tLW	4.5	
			Release				tREM	1.6	
	Output Driving	Clear	Hold Ti	me			tINH	6.7	
Pin Name	Factor (lu)								
Q	18								
CO	18				***************************************				
		* Minimum values for the typical operating condition.  The values for the worst case operating condition							
	are given by the maximum delay multiplier.								

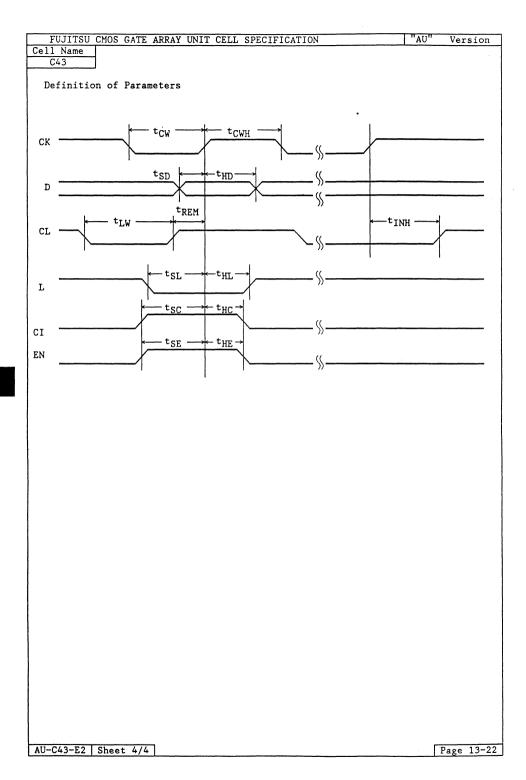
		Outputs				
CL	L	D	EN	CI	CK	Q
L H H H H	X L H H	X H X X X	X X X L H	X X X L X H	X † X X	L H L No Counting No Counting Count up

Note: The CO output produces a high level output data when the counter overflows.

AU-C43-E2 | Sheet 1/4







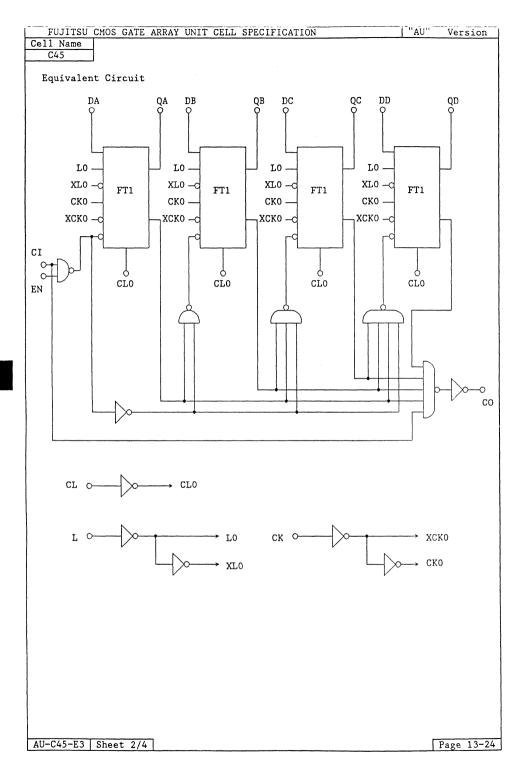
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
	Function							Number of BC
C45	Non-SCAN 4-bit	Binary	Synchro	nous Up	Counte	r		48
Cell Symbol				agation			er	
		t	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.14	0.11	1.50	0.07	0.11	4	CK → Q
		4.06	0.14	2.26	0.07			CK → CO
		1.53	0.14	1.09	0.07		1	CI → CO
							1	
DA ————————————————————————————————————	QA QB QC QD CD	Clock Data S Data H	Pulse W Pause T etup Ti old Tim	ime me e		2	Symbol tCW tCWH tSD tHD	4.0 4.0 3.1 1.7
	Input Loading		etup Ti				tSL tHL	4.0
Pin Name	Factor (lu)		up Time				tSC	5.3
D	1		d Time				tHC	1.6
L,EN	1		up Time				tSE	5.3
CK,CL	1		d Time				tHE	1.6
CI	2		Setup T	ime			tSR	3.1
	_		Hold Ti				tHR	1.6
	Output Driving	32552						
Pin Name	Factor (lu)					ł		
Q	18							
co	18							
		The		for the	worst	case or	erati	ing condition ng condition blier.

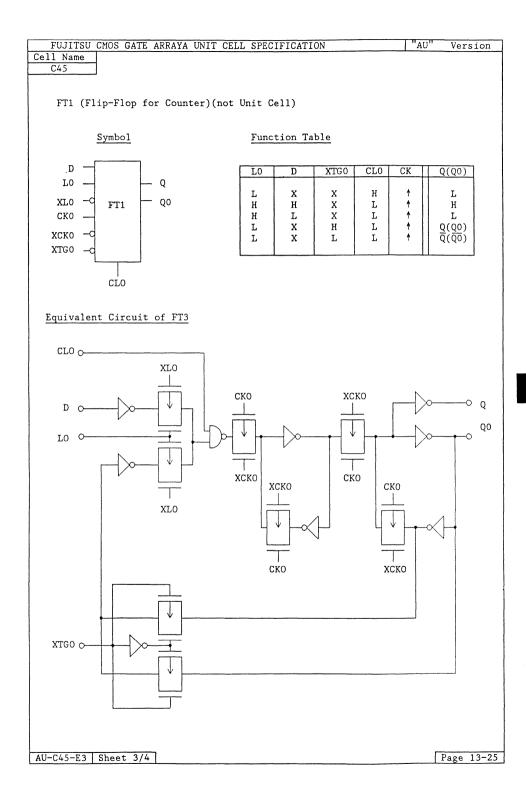
		Inp	uts			Outputs
CL	L	D	EN	CI	CK	Q
L H H H	X L H H	X H L X X	X X X L H	X X X L X H	† † X X	L H L No Counting No Counting Count up

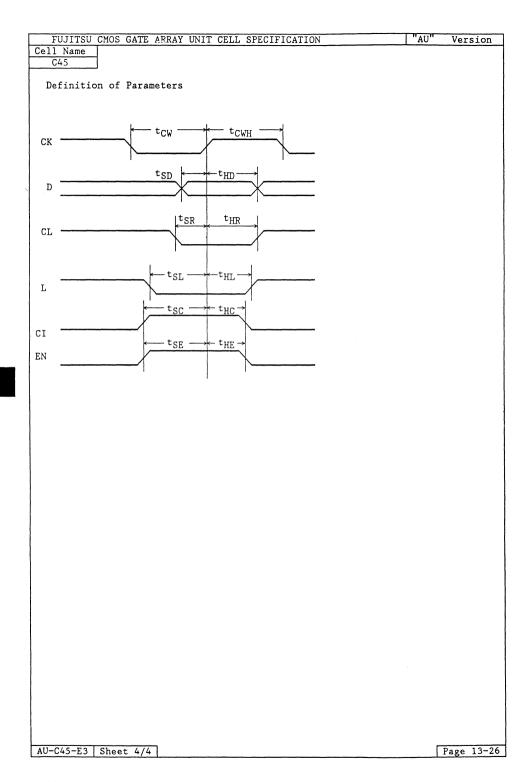
Note : The CO output produces a high level output data when the counter overflows.

AU-C45-E3 | Sheet 1/4

Page 13-23







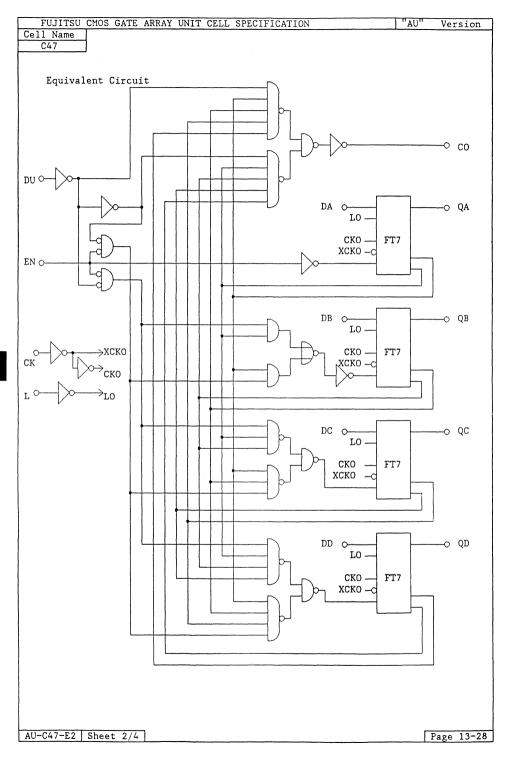
FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
C47 Cell Symbol	Non-SCAN 4-bit	Binary		nous Up agation				68
Cell Symbol				<del></del>				
		t0	up KCL	t0	td KCL	KCL2	CDR2	
		3.19	0.13	2.87	0.13	0.20	4 4	Path CK → Q
		4.33	0.13	4.90	0.13	0.20	7	CK → CO
		4.01	0.03	4.43	0.07	0.20	4	L → Q
		1.98	0.13	2.41	0.13	0.20	-	DU → CO
_		1.90	0.03	2.41	0.07			DO 7 CO
DA ————————————————————————————————————	QA QB QC QD QD	Clock	Pulse W Pause T	ime			Symbol tCW tCWH	4.5
			etup Ti				tSD	0.6
	_	Data H	old Tim	е			tHD	1.5
	Input Loading							
Pin Name	Factor (lu)		up Time				tSU	4.3
D	1	DU Hol	d Time			-	tHU	0.7
L	2	F)1 G	m.				- CF	+ , , -
DU	1		up Time				tSE	4.0
CK EN	1 3	EN Hol	a lime				THE	1.0
EN	3	C1	Release	T:			tREM	1 0
	Output Deducts		<u>Kelease</u> Hold Ti				tINH	1.9
Pin Name	Output Driving Factor (lu)	Clear	noid II	me			LINH	8.9
Q	18	Load P	ulse Wi	dth			tLW	4.0
co	18	The		for the	worst	case o	perati	ing condition ng condition lier.

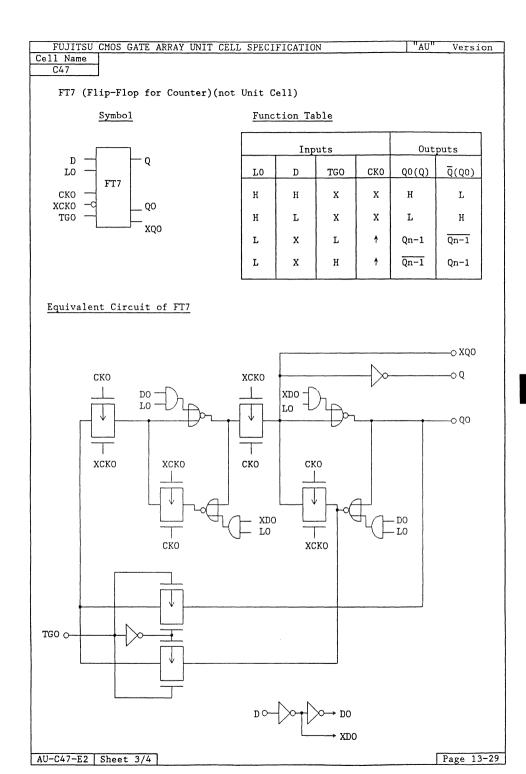
		Inp	uts		Outputs
Q	L	EN	Q		
H L X X	L L H H	X X H L	X X X L H	X X †	H L No Counting Count Up Count Down

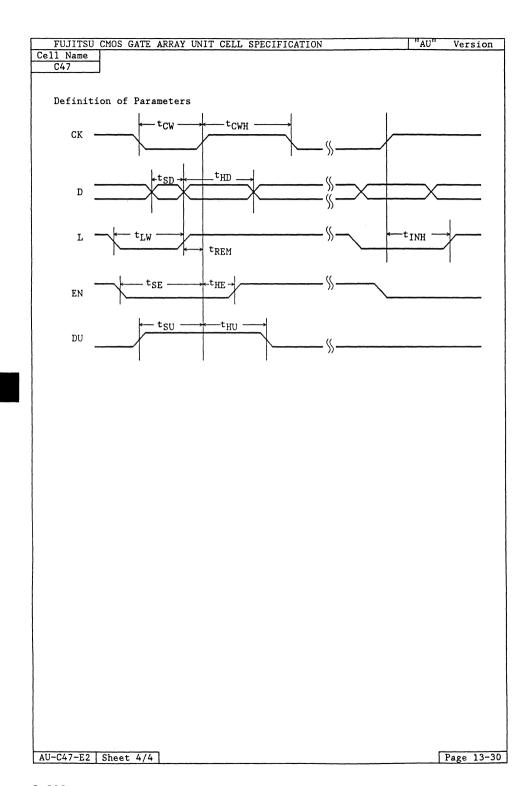
Note : The CO output produces a low level output pulse when the counter overflows or underflows.

AU-C47-E2 Sheet 1/4

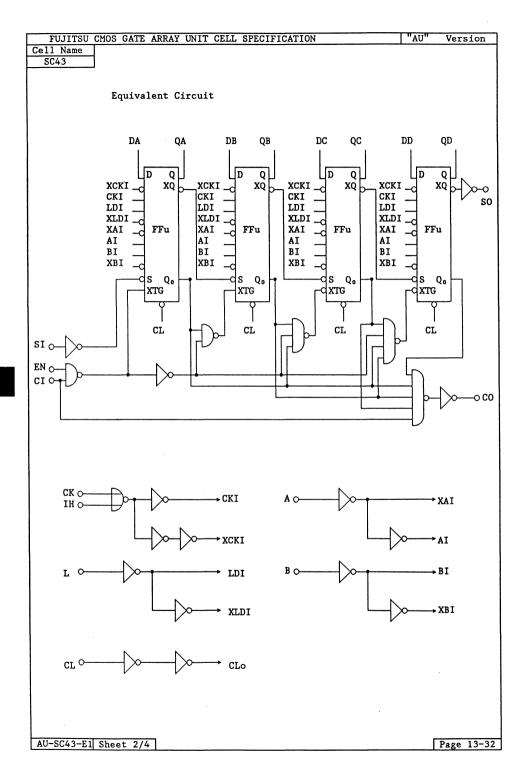
Page 13-27

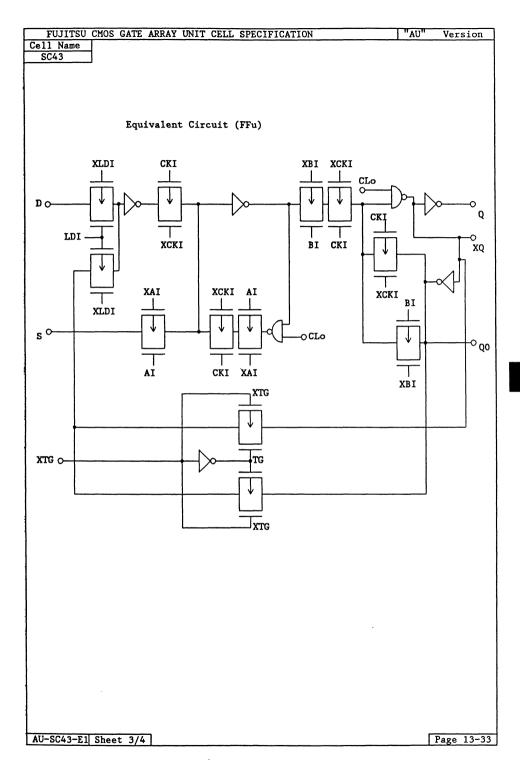


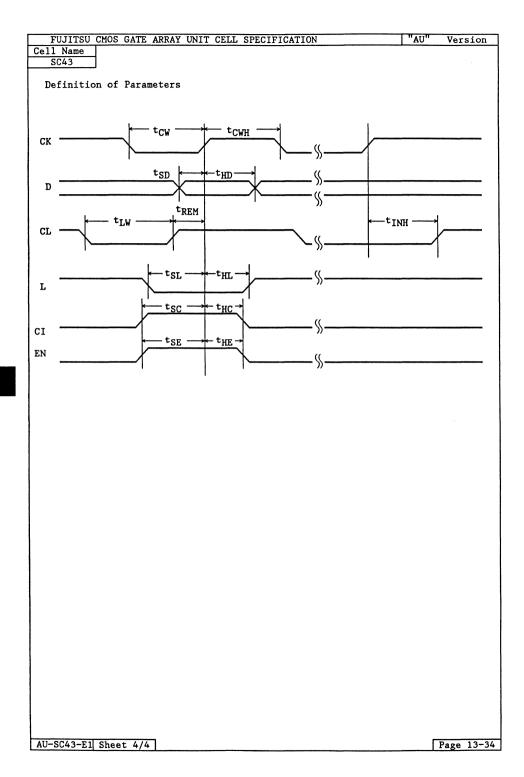




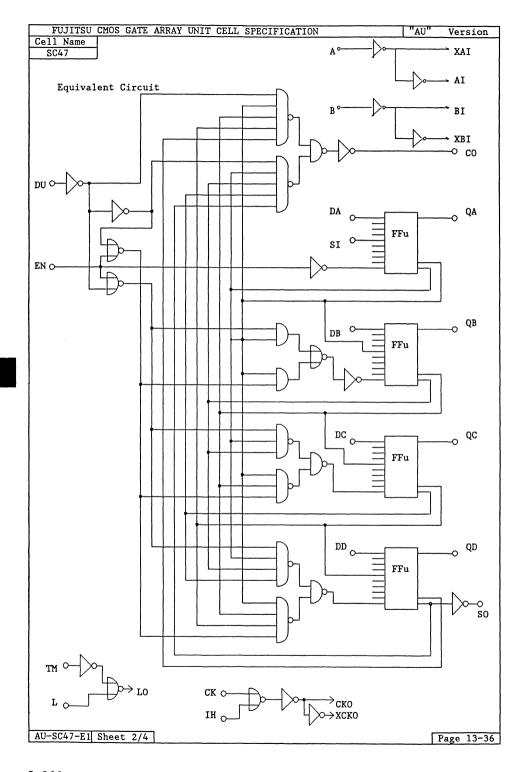
SCAN 4		FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version Cell Name Function Number of BC											
SC43 with A	-bit Sync	hronous	Rinary	Un Cou	nter				Number of BC				
	Asynchrono			op cou	11001				59				
1		t			td								
		t0	KCL	t0	KCL	KCI	L2	CDR2	Path				
		3.42	0.13	3.29	0.07	0.1	10	4	CK → Q				
l —		4.12	0.13	4.40	0.07	0.1	10	4	CK → CO				
DA	QA	-	-	2.09	0.07	0.1	10	4	CL → Q				
DB	QB	1.46	0.13	1.00	0.07	0.1		4	CI → CO				
DC —	QC	-	-	2.86	0.07	0.1	10	4	CL → CO				
DD	QD												
CK							- 1						
IH —							- [		1				
L													
cī —	— co						- 1						
EN —	00												
si —	— so						- 1						
A		Parama	ter			Ь	!	ymbol	Typ(ne)%				
B — d		Parame	Pulse W	idth				tCW	Typ(ns)* 4.1				
			Pause T					ECWH	5.9				
I		Data S	etup Ti	me				tSD	1.6				
CL CL		Data H	old Tim	e e				tHD	1.7				
		Load S	etup Ti	me.				tSL	2.4				
		Load H	old Tim	e				EHL	2.0				
Input	Loading	CI Set	up Time					tSC	3.2				
	r (lu)	CI Hol	d Time					tHC	1.4				
D	2		up Time		·		tSE		3.2				
CK,IH	1	EN Hol	d Time				tHE		1.4				
L,CL,SI	1	Clear Pulse Width						tLW	5.0				
EN	1	Clear Release Time						tREM	1.2				
A,B,CI	2							tINH	4.6				
	t Driving	į											
	r (lu)												
1 ' 1	18												
	18	l	_	_			_		l				
S0	18								ng condition.				
1									g condition				
		are	given b	y the m	aximum	dela	y m	ultipl	ier.				
İ													
ì													
1													
									ì				
AU-SC43-E1 Sheet 1									Page 13-31				

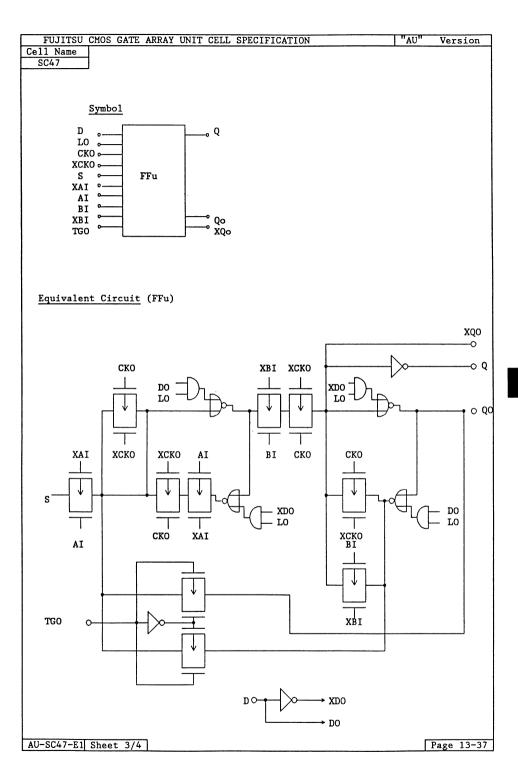


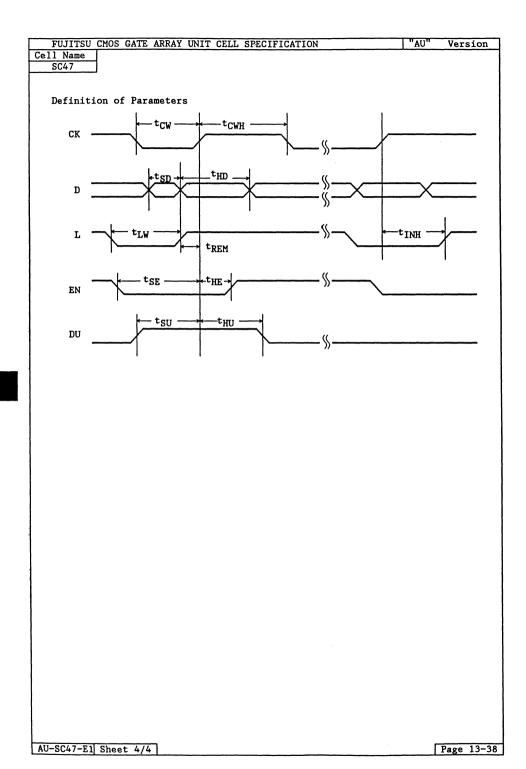




FILITSII C	MOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		Π'Δ	U" Version
	Function	MII ODD	D BILCI	FICATIO				Number of BC
3322								.,
SC47	SCAN 4-bit Sync	hronous	Binary	Up/Down	n Count	er		78
Cell Symbol			Prop	agation	Delay	Paramet	er	<del> </del>
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.60	0.13	3.76	0.15	0.20	4	CK → Q
_		4.90	0.13	6.96	0.07		l	CK → CO
DA	QA	1.88	0.13	2.35	0.07		l	DU → CO
DB	Qв							
DC	—— Qc							į į
DD	—— QD							
	1						1	
CK		ŀ						
IH —							l	
L							ļ.	
TM							ŀ	
EN -	þ co							
עם —							l	
si —	so	Parame	tor	لــــــا		1 6	ymbol	. Typ(ns)*
A				idth (H	7	<del> -</del>	tCWH	8.8
В — ф		Clock	Pause T	ime (L			tCWL	7.3
		Data	etup Ti	we (n	,		tSD	10.7
		Data H	old Tim	<u>ш</u> е			tHD	1.7
		EN So+	up Time				tSE	6.3
			d Time				tHE	0.6
	Input Loading	DII Tee	ut Setu	n Time			tSU	7.1
Pin Name	Factor (lu)	DII Tee	ut Hold	Time			tHU	0.4
D D	2	Tood D	ulse Wi	d+h			tLW	15.4
ľ		Load P	elease	Time			tREM	2.9
CK,IH,TM,L	1 3		old Tim					12.2
EN DU A D		Load H	010 11m	ie			tINH	12.2
DU,A,B	1							
SI	2	ł						
D: 11	Output Driving							
Pin Name	Factor (lu)							
Q	18							
SO SO	18		1					
co	18							ing condition.
1	Ì							ing condition
	l	are	given b	y the m	aximum	delay r	nultip	olier.
1								
1								
1								
1								
1								
1								
İ								
1								
AU-SC47-E1 S								



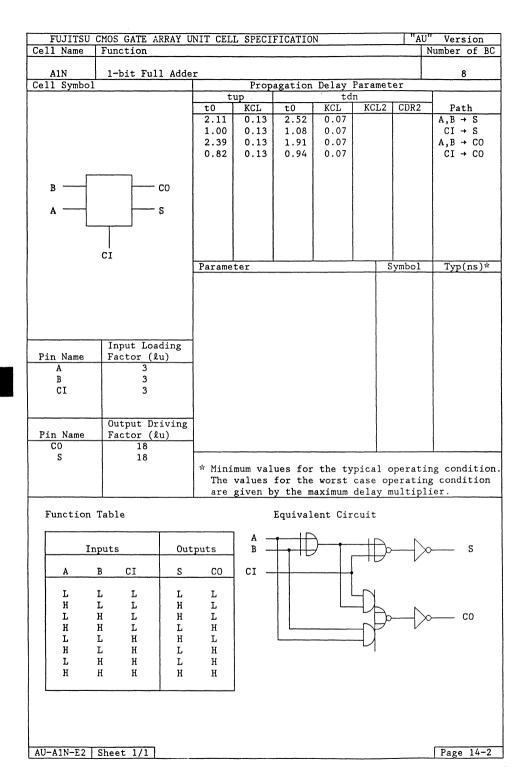




# **Adder and ALU Family**

Page	Unit Cell Name	Function	Basic Cells
2-249	A1A	1-bit Half Adder	5
2-250	A1N	1-bit Full Adder	8
2-251	A2N	2-bit Full Adder	16
2-253	A4H	4-bit Binary Full Adder with Fast Carry	48

DULTIMOU O	WOG GARE A	20.437. 77	urm one		DIGAMIC			11.	TT!!! T7 .
	MOS GATE A	U YAX	NII CEL	L SPECI	r ICATIO	IA		J A	U" Version Number of BC
A1A Cell Symbol	1-bit Hal	E Adde	r	Pron	agation	Delay	Paramet	er	5
Jell Symbol			t	up	agacion	td			
			t0	KCL	t0	KCL	KCL2	CDR2	
			0.98	0.07	1.15	0.03			$A \rightarrow S$ $B \rightarrow S$
			0.90	0.07	1.00	0.03			A → CO
			1.02	0.07	0.92	0.03		ļ	B → CO
В	C	)							
Α	s								
^^									
			Parame	ter			S	ymbol	Typ(ns)*
	Input Loa								
Pin Name A	Factor (1	u)	-						
B	2								
	Output Dr								
Pin Name CO	Factor (1		-						
s	36								
			* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
			The	values given b	or the	worst	delav m	erati nultir	ng condition
			are given by the maximum delay multiplier.						
Function T	Table				Equival	ent Cir	cuit		
			1	Α —		•	$\overline{A}$		
A F	3 CO	S	1	В		1	-		>>— s
l L I	L	L	1						, 5
L	f L	H							
HI		H L	1				$\rightarrow$		>>— co
	, L	ш						V	
			-						
AU-A1A-E2 S	Sheet 1/1								Page 14-1

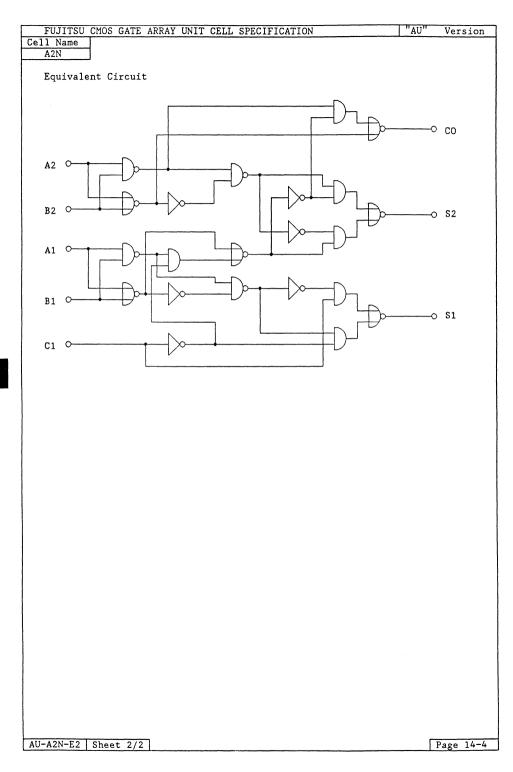


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version										
Cell Name	Function							Number of BC		
A2N	2-bit Full Adde	r						16		
Cell Symbol		Propagation Delay Parameter								
			up KCL	t0	KCL	n KCL2	CDR2	D-45		
		t0 2.28	0.23	2.25	0.11	KUL2	CDK2	Path A1 → C0		
		2.28	0.23	2.23	0.11			B1 → C0		
		1.27	0.23	1.09	0.11	0.10	4	A2 → CO		
		1.18	0.23	1.09	0.07	0.10	4	B2 → C0		
		2.23	0.23	2.07	0.11	0.10	7	CI → CO		
В2	co	2.38	0.18	2.20	0.11			A1 → S1		
A2		2.38   0.18   2.20   0.11   2.38   0.18   2.20   0.11								
В1 —	s2	0.95	0.18	0.95	0.11		Ì	B1 → S1 CI → S1		
A1	S1	2.26	0.18	2.20	0.11			A1 → S2		
L		2.49	0.18	2.36	0.11			A2 → S2		
		2.17	0.18	2.25	0.11		l	B1 → S2		
		2.49	0.18	2.36	0.11			B2 → S2		
	CI	2.21	0.18	2.02	0.11		l	CI → S2		
		Parame	ter			S	ymbol	Typ(ns)*		
						1				
	Input Loading					i				
Pin Name	Factor (lu)									
A,B	2					ļ				
CI	2					1				
								1		
	Output Driving					1		1		
Pin Name	Factor (lu)									
S	14									
co	14									
00	1	* Mini	mum val	ues for	the tv	pical c	perat	ing condition.		
	* Minimum values for the typical operating condition.  The values for the worst case operating condition									
			given b							

	Inpi	ıts				Out	puts		
				(	CI = I		(	CI = F	ł
A1	B1	A2	B2	S1	S2	CO	S1	S2	CO
							1		
L	L	L	$_{ m L}$	L	L	L	H	L	L
Н	L	L	L	H	L	L	L	H	L
L	H	L	L	Н	L	L	L	H	$_{ m L}$
Н	H	L	L	L	Н	L	н	Н	L L L
L	L	H	L	L	Н	L	н	Н	L
Н	L	H	L	н	н	L	L	L	H
L	H	H	L	н	H	L	L	L	H
н	H	H	L	L	L	H	н	L	H
L	L	L	H	L	H	L	н	H	L
Н	L	L	H	н	H	L	L	L	H
L	H	L	H	н	Н	L	L	L	Н
Н	Н	L	Н	L	${f L}$	Н	н	L	H
L	L	H	Н	L	L	Н	н	L	Н
Н	L	Н	Н	Н	L	Н	L	H	Н
L	H	н	н	н	L	н	L	Ĥ	Н
н	Н	Н	Н	L	H	Н	н	H	Н
									••

AU-A2N-E2 | Sheet 1/2

Page 14-3



FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N N		"AU	J" Version
Cell Name	Function							Number of BC
А4Н	4-bit Binary Fu	11 Adde	r with	Fast Ca	rry			48
Cell Symbol			Prop	agation	Delay :	Paramet	er	
		tup tdn						
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.95	0.18	1.31	0.11			CI → S1
		2.12	0.23	2.46	0.11			CI → S2
		2.43	0.23	2.39	0.11			CI → S3
B4	co	2.51	0.23	2.83	0.11			CI → S4
A4	S4	2.30	0.13	2.57	0.07			CI → CO
В3 —								
A3	S3	3.05	0.18	2.71	0.11			A1,B1 → S1
B2		2.54	0.23	2.47	0.11			A1,B1 → S2
A2	S2	2.74	0.23	3.08	0.11			A1,B1 → S3
B1		3.00	0.23	3.14	0.11			A1,B1 → S4
A1	s1	2.64	0.13	3.03	0.07		ł	A1,B1 → CO
L	<del></del> _						l	
		2.47	0.23	2.70	0.11		1	A2,B2 → S2
		2.93	0.23	2.88	0.11			A2,B2 → S3
	CI	2.99	0.23	3.24	0.11			A2,B2 → S4
		3.10	0.13	3.07	0.07			A2,B2 → CO
	Input Loading	2.25	0.23	2.28	0.11			A3,B3 → S3
Pin Name	Factor (lu)	3.07	0.23	3.23	0.11		ł	A3,B3 → S4
A	2	3.04	0.13	3.06	0.07		l	A3.B3 → CO
В	2	_ , , ,		- 700	- / - /			,
ČI	2	2.32	0.18	2.41	0.07	0.10	4	A4,B4 → S4
	_	2.93	0.13	2.81	0.07			A4,B4 → CO
	Output Driving	_ /• •					l	,
Pin Name	Factor (lu)							
CO	18							
\$1,83,84	14							
S2	18							

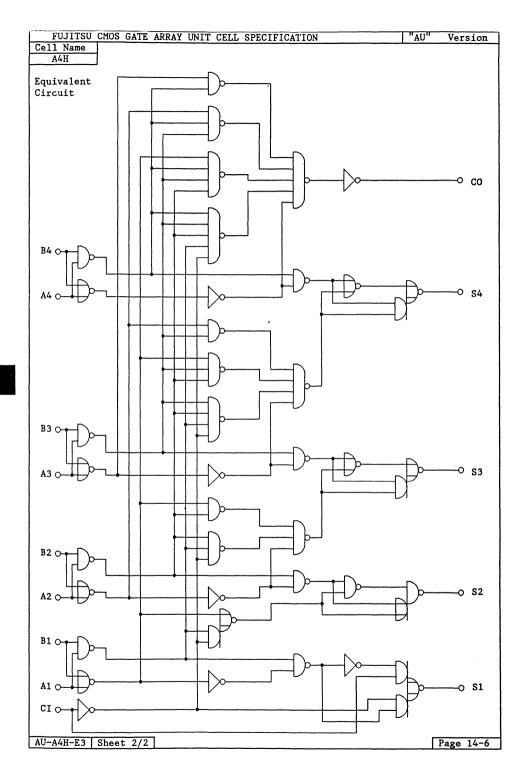
AU-A4H-E3 Sheet 1/2

г					Ι		TITO	PUT		
1		INP	TU		CI	= L		CI	= 1	ī
						= <u>T</u>	;		$= \frac{1}{1}$	ī — —
	A1_	B1_	A2_	B2_	<u>s</u> 1	<u>S2</u>	C2_	<u>S1</u>	<u>S2</u>	C2_
L	A3	В3	Ā4	B4	<u>8</u> 3	S4	CO		S4	CO
١	_	_	-	_			_	۱	_	-
1	L	L	L	L	L	L	L	Н	L	L
1	H	L	L	L	Н	L	L	L	H	L
1	L	H	${f L}$	L	Н	L	L	L	H	L
1	H	H	L	L	L	H	L	H	H	L
1	L	L	H	L	L	H	L	Н	H	L
1	H	L	H	L	н	Н	L	L	L	H
ı	L	H	H	L	н	H	L	L	L	H
ŀ	H	H	Н	L	L	L	Н	н	L	Н
1	L	L	L	H	L	Н	L	н	Н	L
1	H	Ĺ	Ĺ	Н	н	Н	Ĺ	L	L	H
ł	L	H	Ĺ	H	н	H	L	Ĺ	Ĺ	н
1	н	Н	Ĺ	Н	L	L	Н	н	Ĺ	Н
ı	L	L	Н	H	L	L	Н	н	Ĺ	Н
1										
1	H	L	H	H	H	L	H	L	H	H
1	L	H	H	Н	Н	L	H	L	H	Н
1	H	H	H	Н	L	Н	H	H	H	H
L					1					

#### Note:

Input conditions at A1, A2, B1, B2 and CI are used to determine outputs S1 and S2 and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4 and CO.

Page 14-5



# **Data Latch Family**

Page	Unit Cell Name	Function	Basic Cells
2–257	YL2	1-bit Data Latch with TM	5
2-259	YL4	4-bit Data Latch with TM	14
2-261	LTK	Data Latch	4
2-263	LTL	1-bit Data Latch with Clear	5
2-265	LTM	4-bit Data Latch with Clear	16
2-268	LT1	S-R Latch with Clear	4
2-270	LT4	4-bit Data Latch	14

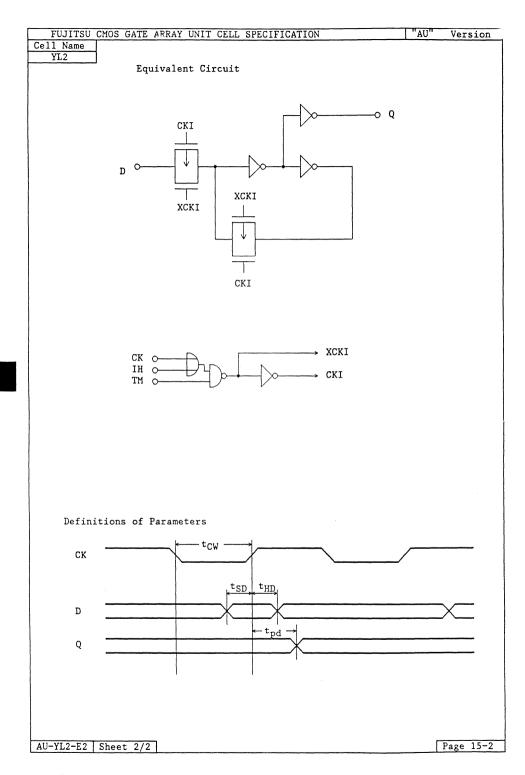
	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A"	
Cell Name	Function	Number of BO						
YL2		it Data Latch with TM						
Cell Symbol								
			up		td		anna	┙.
		t0	KCL	t0	KCL 0.03	KCL2	CDR2	Path
		2.19 0.93	0.07	2.25	0.03			CK,IH → Q D → O
		0.93	0.07	1.03	0.03			D 7 Q
D — C IH — C	Q Q							
		Parame	ter			l s	ymbol	Typ(ns)*
		Tarame					<i>y</i> 201	135(115)
		Clock	Pulse W	idth			tCW	5.5
		Data S	etup Ti	me			tSD	2.6
		Data H	old Tim	e			tHD	2.0
	Input Loading	ĺ						
Pin Name	Factor (lu)							
D	2	1						
CK	1							
IH	1							
TM	1							
	Output Driving					1		
Pin Name	Factor (lu)	]						
Q	36							
		The		for the	worst	case op	erati	ing condition

The TM terminal must be kept LOW during the SCAN Mode.

### Function Table

Input				Output	Mode
TM	IH	H CK D		Q	node
L	X	X	D	D	SCAN
Н	Н	X	X	Q <sub>o</sub>	
Н	Х	Н	X	Q <sub>0</sub>	LATCH
Н	L	L	D	D	

Page 15-1



FULITSII (	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version							
YL4 Cell Symbol	4-bit Data Latch with TM 14							
Cell Symbol Propagation Delay Parameter tup tdn								
		to	KCL	t0	KCL	KCL2	CDR2	Path
		2.67	0.07	2.75	0.03			CK,IH → Q
		0.88	0.07	1.03	0.03			$D \rightarrow Q$
ı		[						
D1 —								
D2 —	Q1 Q2	,						
D3 —	$ \frac{Q^2}{Q^3}$							
D4	<b>⊢</b>							
ск —								
IH —								
TM -							1	
L						}	ł	
		Parame	ter			1 5	Symbol	Typ(ns)*
		Clock Pulse Width (CK)					tCW	5.8
					(5)			
		Data Setup Time (D)  Data Hold Time (D)					tSD tHD	1.5
		Data H	old lim	<u>e</u>	(1)		LID	3.2
	Input Loading	1						
Pin Name	Factor (lu)					1		
D	2							
CK	1							
IH TM	1 1							
1m	1					ĺ		
	Output Driving	1						
Pin Name	Factor (lu)							
Q	36							
		S. M	<b>_</b>					
								ing condition. ng condition
					aximum			
	<del></del>		0-1011	, ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,				

## Note:

The TM terminal must be kept LOW during the SCAN Mode.

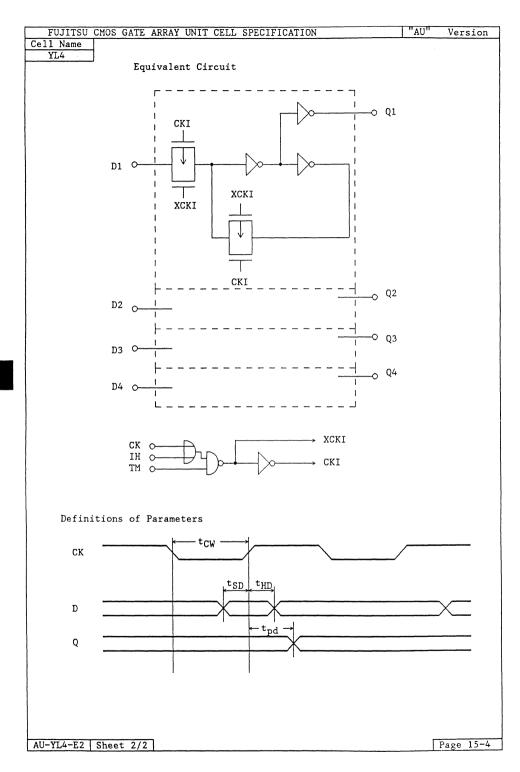
## Function Table

	Input				Output	Mode
	TM	IH	CK	Dn	Qn	node
ĺ	L	X	X	D	D	SCAN
	Н	Н	X	Х	Qno	
	H	X	н	Х	Qno	LATCH
	H	L	L	D	D	

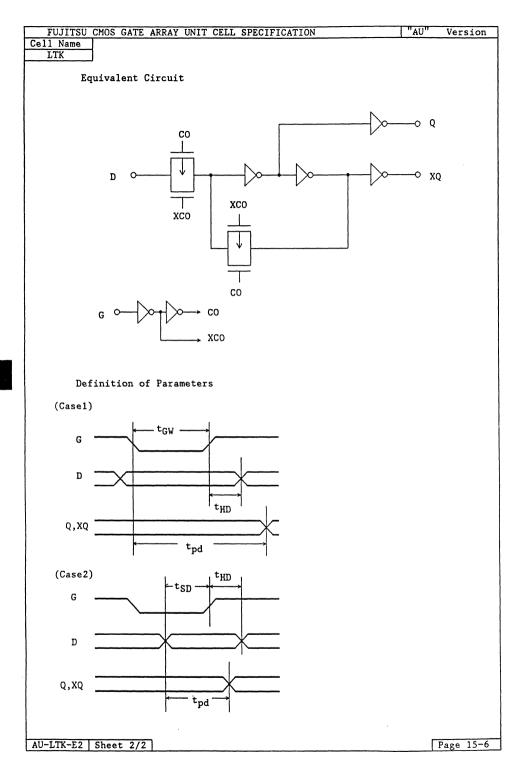
 $n = 1 \sim 4$ 

AU-YL4-E2	Sheet 1/2
-----------	-----------

Page 15-3



FUJITSU C	MOS GATE ARRAY I	NIT CELL SPECIFICATION	"AU" Version					
	Function	WIT ORDER STEETITION	Number of BC					
LTK	Doto Istah		,					
Cell Symbol	Data Latch	Propagation Delay Param	neter 4					
		tup tdn						
		t0 KCL t0 KCL KCI 0.83 0.13 0.92 0.07	$\begin{array}{c cccc}  & CDR2 & Path \\ \hline  & D \rightarrow Q \end{array}$					
		1.16 0.13 1.31 0.07	$D \rightarrow XQ$					
		1.40 0.13 1.46 0.07	$G \rightarrow Q$					
		1.70   0.13   1.87   0.07	G → XQ					
D	Q							
G								
1	р— xq							
		Parameter	Symbol Typ(ns)*					
		G Input Pulse Width	tGW 4.0					
		Data Setup Time Data Hold Time	tSD 1.3 tHD 1.9					
		Data Hord Time	CHD 1.5					
	-							
Pin Name	Input Loading Factor (lu)							
D	2							
G	1							
	Output Driving							
Pin Name Q	Factor (lu)							
xQ	18							
		* Minimum values for the typical	operating condition.					
		The values for the worst case operating condition are given by the maximum delay multiplier.						
		are given by the maximum deray	marcipiler.					
Function 7	<b>Table</b>							
Inputs	Outputs							
D G	Q XQ							
хн	Q <sub>o</sub> XQ <sub>o</sub>							
H L	H L							
LL	L H							
			<u></u>					
AU-LTK-E2 S	Sheet 1/2		Page 15-5					

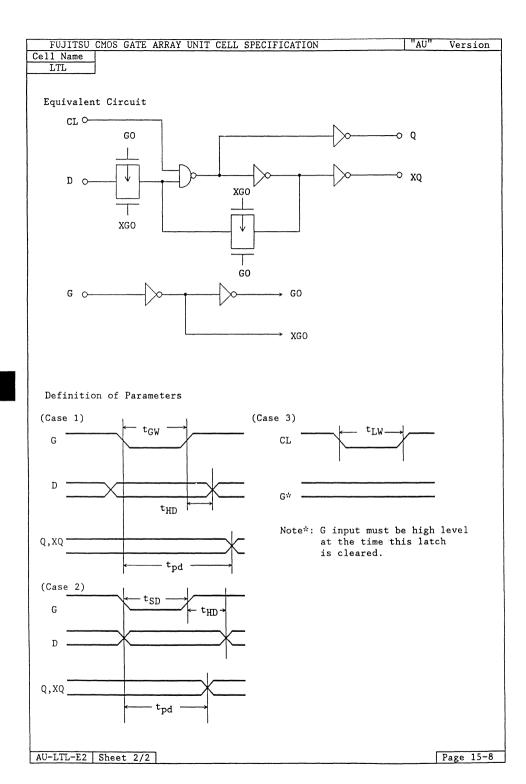


	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
LTL	1-bit Data Latch with Clear							5
Cell Symbol		I		agation	Delay :	Paramet	er	<del></del>
		t	up		td			
		t0	KCL	t0	KCL	KCL2	LD2	Path
		1.11	0.13	0.68	0.07			CL → Q,X0
		0.95	0.13	0.98	0.07			$D \rightarrow Q$
		1.22	0.13	1.37	0.07		ĺ	$D \rightarrow XQ$
		1.57	0.13		0.07		Ì	$G \rightarrow Q$
		1.78	0.13	2.01	0.07		ł	G → XQ
D	Q							
	4							
G — 9								
	þ— χο							
L								
	Ĭ							
	CL	D				1 6		T () %
		Parameter Symbol G Input Pulse Width tGW					ymbol	Typ(ns)*
		G Inpu	t Pulse	width			LGW	4.0
		Data S	etup Ti	mo			tSD	1.1
			old Tim				tHD	0.4
		Dava II	014 11					
		Clear	Pulse W	idth			tLW	4.0
	Input Loading							
Pin Name	Factor (lu)							
D	2							
G	1							
$\mathtt{CL}$	1					İ		
· · · · · · · · · · · · · · · · · · ·	I	1						
D: 17	Output Driving							
Pin Name	Factor (lu)	1						
Q	18							
XQ	10	W Mind	mum 11c1	fc-	+ho +	niaal -	nonet	ing condition
								ng condition
					aximum			
	<u></u>	1 416	Prveii D	J CITE III	avinail.	uciay II	41 61 6	,1101+

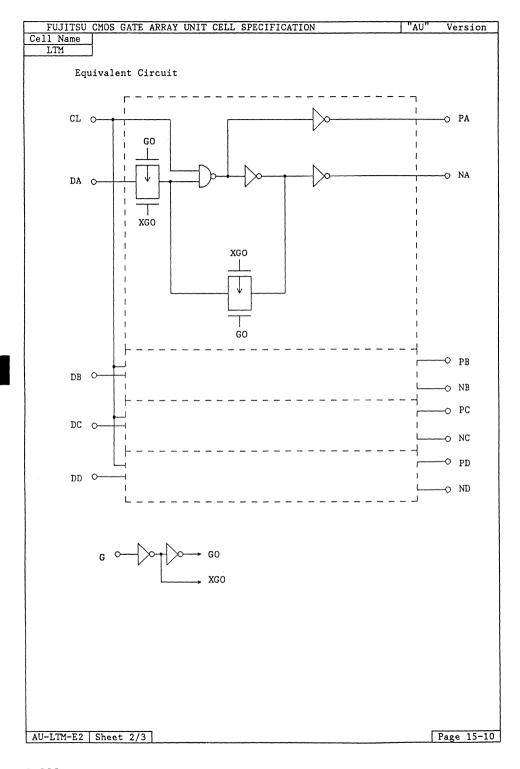
Inputs	Out	puts
CL D G	Q	XQ
L X H H X H H H L H L L	L Q <sub>0</sub> H L	H XQ。 L H

AU-LTL-E2 | Sheet 1/2

Page 15-7



FILITSILC	MOS GATE ARRAY U	INIT CEL	I SDECT	FICATIO	NI .		Π'Α	U" Version	
	Function	MII CLL	L SIECI.	FICATIO			1 2	Number of BC	
		,	<b>61</b>						
LTM Cell Symbol	4-bit Data Late	h with		agation	Delay	Paramet	er	16	
Jerr Bymber		t	up	agacion	td		<u> </u>		
DA —— DB —— DC —— DD —— G ——		t0 1.23 0.98 1.28 2.09 2.19	KCL 0.13 0.13 0.13 0.13 0.13	t0 0.78 1.03 1.43 1.96 2.52	KCL 0.07 0.07 0.07 0.07 0.07	KCL2	CDR2	Path  CL → P,N  D → P  D → N  G → P  G → N	
	ND								
		Parame	ter			S	ymbol	Typ(ns)*	
	CL		t Pulse	Width			tGW	4.0	
	OL	Clear	Pulse W	idth			tLW	4.0	
								1.3	
				Data Setup Time         tSD           Data Hold Time         tHD					
		Data II	014 11				-	1.9	
Pin Name	Input Loading Factor (lu)					Ì			
D	2	1							
G CL	1 4	}							
CL	+								
ļ	0.1.1.2	1							
Pin Name	Output Driving Factor (lu)								
P	18	]							
N	18	The		for the	worst	case op	erati	ing condition. ng condition lier.	
Function T	Cable								
Inputs	Outputs								
CL D G	PN								
L X H H X H H H L H L I	P <sub>o</sub> N <sub>o</sub>								
AU-LTM-E2   S	Sheet 1/3							Page 15-9	



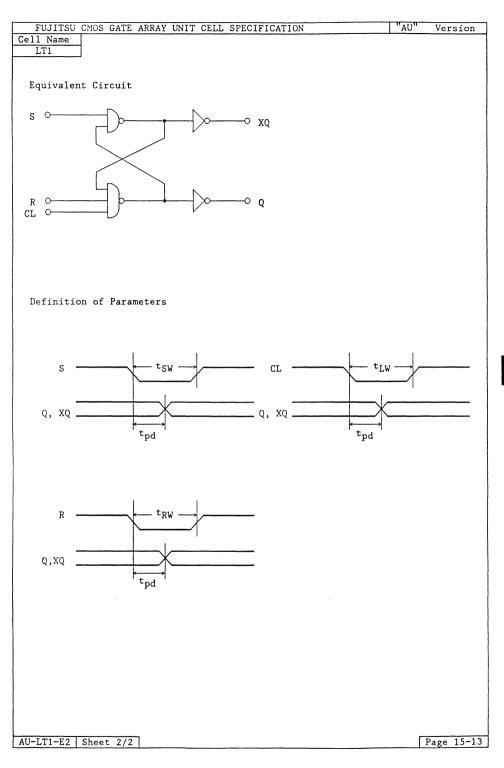
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version Cell Name LTM Definition of Parameters (Case1) G D tHD P,N (Case2) G  $\mathsf{t}_{\mathtt{SD}}$  $\mathtt{t}_{HD}$ P,N (Case3) CL ₩G P,N Note \*: G input must be high level at the time this latch is cleared. AU-LTM-E2 | Sheet 3/3 Page 15-11

FUJITSU C	MOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	N		T "A	U" Version
	Function			1011110				Number of BC
LT1	S-R Latch with	CLEAR						4
Cell Symbol			Prop	agation	Delay	Paramet	er	W
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.41	0.13	0.71	0.07		ļ	$S \rightarrow Q, XQ$
		1.25	0.13	0.83	0.07		1	$R \rightarrow Q, XQ$
		1.15	0.13	0.74	0.07		1	CL → Q,XQ
s —	Q							
R —d	xQ							
	CL	Parame	tor			١	Symbol	Typ(ns)*
						tSW	4.0	
		1000 10	100 1110					
		Reset Pulse Width					tRW	4.0
							tLW	
		Clear	Pulse W	idth	th			4.0
	Input Loading	-						
Pin Name	Factor (lu)							
S	1	1				1		
R	1							
CL	1							
	Output Driving	1						
Pin Name	Factor (lu)					1		
Q	18							
XQ	18							
		* Minimum values for the typical operating condition.						
		The values for the worst case operating condition are given by the maximum delay multiplier.						
	1	are	given b	y the m	aximum	delay	nultip	lier.

I:	nputs		Outputs		
CL	S	R	Q	XQ	
L H H H	H H H L	H H L H L	L Q <sub>0</sub> L H Inhi	H XQ <sub>0</sub> H L ibited	

AU-LT1-E2 | Sheet 1/2

Page 15-12

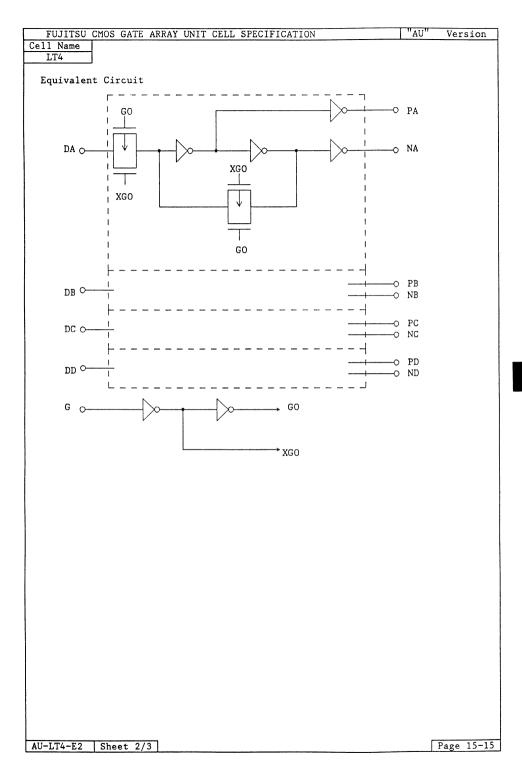


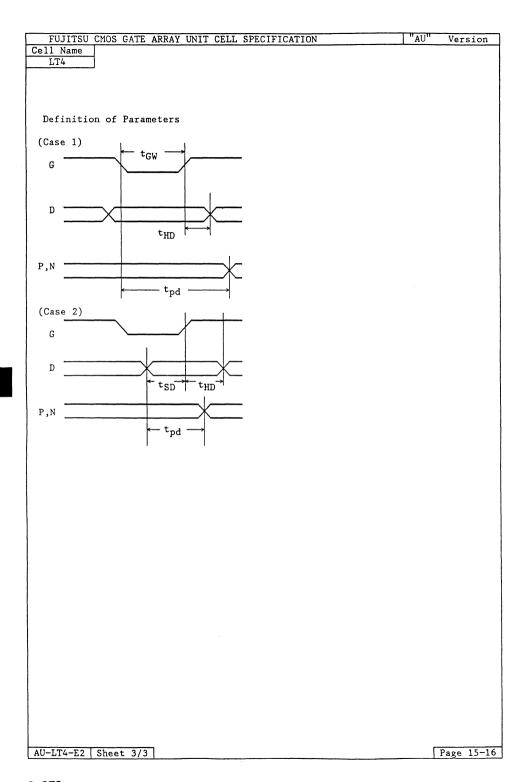
	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		''A	U" Version
Cell Name	Function							Number of BO
LT4	4-bit Data Latc	h						14
Cell Symbol				agation	Delay		er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.00	0.13	1.83	0.07			G → P
		2.00	0.13 0 13	2.44 0.95	0.07		1	$G \rightarrow N$ $D \rightarrow P$
		1.12	0.13	1.28	0.07			$D \rightarrow P$
DA -	PA	1.12	0.13	1.20	0.07			D - N
DB —	b— NA	l					1	
DC —	PB						j	
DD —	p— NB							
G —d	PC							
6 -9	р— ис							
j	PD							
	р— ND						1	
<u> </u>	<del></del>	Parame				1 6	ymbol	Typ(ns)*
			t Pulse	Width			tGW	4.0
		O Impu	t Turse	WIGGII				<del></del>
		Data S	etup Ti	me			tSD	1.3
		Data H	old Tim	е			tHD	1.9
						- 1		
	Input Loading	}						
Pin Name	Factor (lu)					1		
D	2							
G	1							
n	Output Driving	1						
Pin Name P	Factor (lu)	}						
N N	18							
11		* Mini	mum val	ues for	the tv	nical c	nerat	ing condition
		* Minimum values for the typical operating condition.  The values for the worst case operating condition						
		are given by the maximum delay multiplier.						

Inpu	ıts	Outp	uts
D	G	P	N
H L H L	H H L	Po Po H L	No No L H

AU-LT4-E2 Sheet 1/3

Page 15-14





## **Shift Register Family**

Page	Unit Cell Name	Function	Basic Cells
2-275	FS1	4-bit Serial-in Parallel-out Shift Register	18
2-277	FS2	4-bit Shift Register with Synchronous Load	30
2-279	FS3	4-bit Shift Register with Asynchronous Load	34
2-282	SR1	4-bit Serial-in Parallel-out Shift Register with Scan	36

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			U" Version
	Function	000	D OI BOI	11011110	··		1 1	Number of BC
FS1	4-bit Serial-in	Parall	el-out	Shift R	egister			18
Cell Symbol				agation			ter	
		t	up		td			
		t0	KCL	t0	KCL	KCL2		Path
sd —c	QA QB QC QD	1.94	0.13	2.51	0.07	0.10	4	CK → Q
							Symbol tCW	Typ(ns)* 4.0
		SD Setup Time					tSSD	0.5
			d Time				tHSD	0.2
		35	_ 110				3	
		Clock		C ≤ 1	6 lu		tCWL*	* 4.7
	Input Loading	Pause	16	C ≦ 1 < C ≦ 3 < C ≦ 4	2 lu		tCWL*	
Pin Name	Factor (lu)	Time	32	< C ≦ 4	8 lu		tCWL*	* 8.8
SD CK	1 1	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
Pin Name Q	Output Driving Factor (lu)	** The value of tCWL depends on the load(C) connected to the output terminals, QA, QB, QC and QD.						

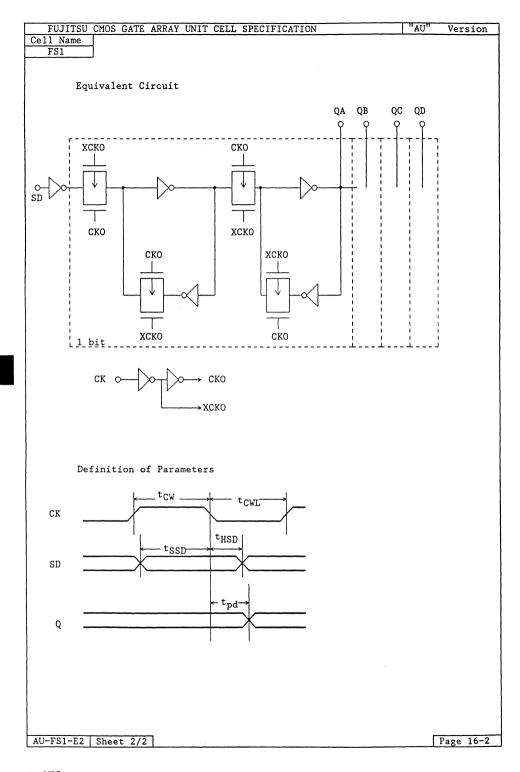
	Inputs		Outputs					
ļ	SD	CK	QA	QB	QC	QD		
	SD	<b>+</b>	SD	QAn	QBn	QCn		

Note:  $\cdot$ SD = H or L

'QAn, QBn and QCn are levels of QA, QB and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

AU-FS1-E2 | Sheet 1/2

Page 16-1



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A"	U" Version
Cell Name	Function							Number of BC
FS2	4-bit Shift Regi	ster wi				<b>D</b>		30
Cell Symbol			Propagation Delay Parameter tup tdn					
]		t0	KCL	t0	KCL	KCL:	2   CDR2	- D. +1
		1.86	0.13	2.51	0.07	0.10		Path CK → Q
PA PB PC PD CK CL	QA — QB — QC — QD			2.51	0.07	0.10		
ь	Parame	ter Pulse W	. 141			Symbol tCW	Typ(ns)*	
				lath			TUW	4.0
		SD Setup Time					tSSD	2.3
		SD Hold Time					tHSD	1.0
		Load Setup Time					tSL	3.5
		Load H	old Tim	e			tHL	0.4
		D Catu	- Ti				tSP	2.9
		P Setu P Hold	Time				tHP	1.2
	Input Loading	1 11010	111116				CIII	1.4
Pin Name	Factor (lu)	Clock	1	C ≤ 1	6 Lu		tCWL*	* 4.7
CK	1	Pause	16	< C ≤ 3	2 lu		tCWL*	
SD	ī	Time	32	< C ≦ 3 < C ≦ 4	8 lu		tCWL*	
L	1							
P	1	* Min	imum va	lues fo	r the t	ypica	l opera	ting con-
								ase operating
	Output Driving	con	dition	are giv	en by t	he max	ximum d	elay
Pin Name	Factor (lu)	mu1	tiplier					
Q	16	]						
				of tCWL to the				d(C) A, QB, QC and

	Inp	uts		Outputs				
SD	L	P	CK	QA	QB	QC	QD	
SD	L	х	<b>→</b>	SD	QAn	QBn	QCn	
х	н	P	<b>+</b>	PA	РВ	PC	PD	

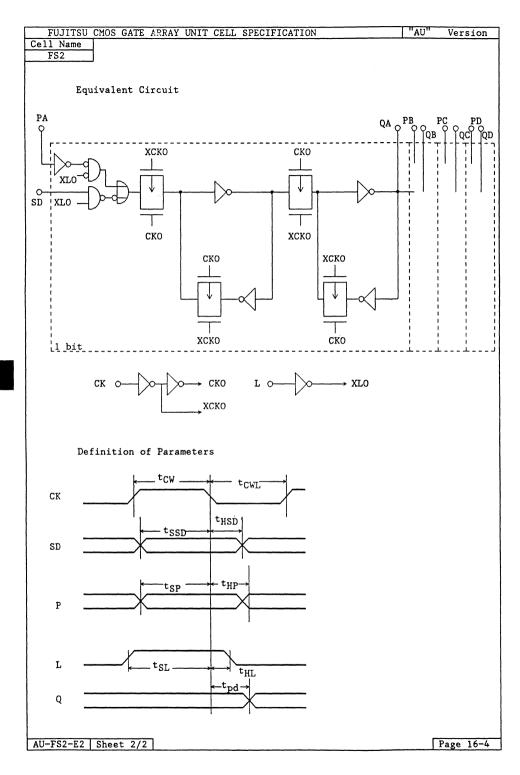
Note:  $\cdot$ SD = H or L

·QAn, QBn and QCn are levels of QA, QB and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

 $\cdot P$  represents PA, PB, PC and PD.

AU-FS2-E2 | Sheet 1/2

Page 16-3

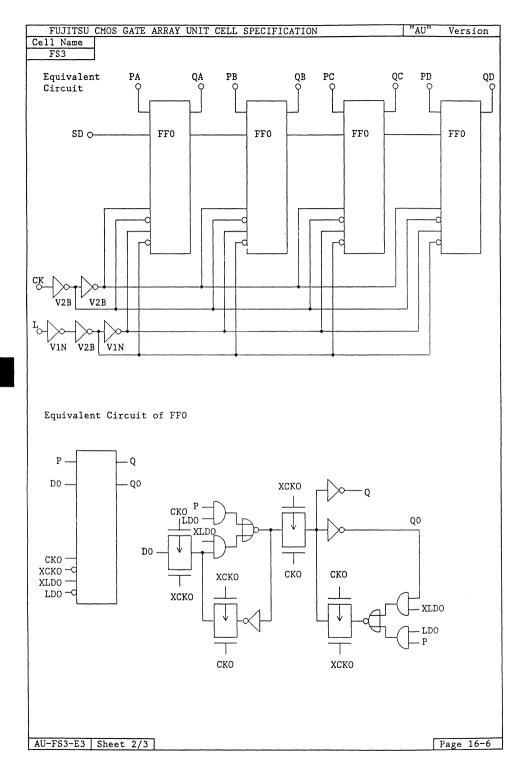


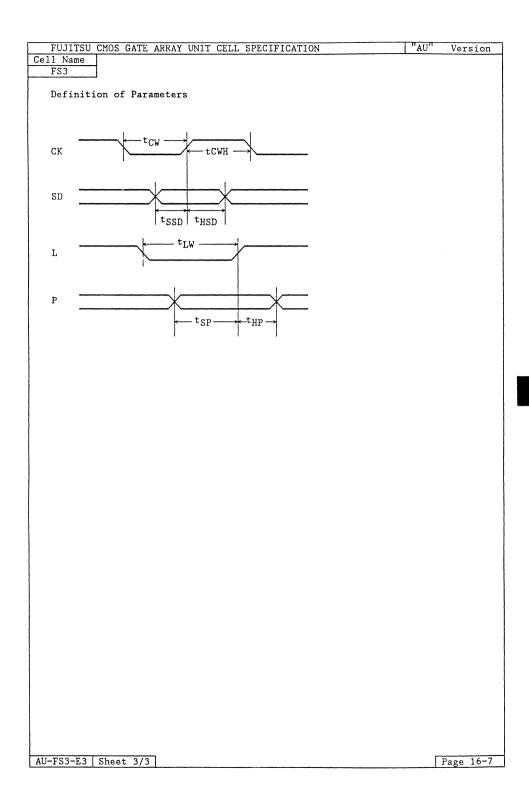
	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		[ "A	U" Version
Cell Name	Function							Number of BC
FS3	4-bit Shift Regi	ster wi				D		34
Cell Symbol				agation	Delay td		ter	
		t0	up KCL	t0	KCL	KCL2	T CDR2	Path
		1.83	0.14	1.70	0.09	KODZ	CDRZ	CK → Q
		3.71	0.14	2.80	0.09		1	L → Q
		1.63	0.14	2.42	0.09			$P \rightarrow Q$
PA ————————————————————————————————————	QA — QB — QC — QD	Clock Load P SD Set	Pulse W Pause T ulse Wi up Time	ime dth			Symbol tCW tCWH tLW	Typ(ns)* 4.0 4.0 5.0 0.8
		SD Hol	d Time				tHSD	1.4
	Input Loading	P Setu	p Time				tSP	0.3
Pin Name	Factor (lu)	P Hold	Time				tHP	1.9
CK	2							
SD	2							
L	1							
P	2							
Pin Name Q	Output Driving Factor (lu)							
		The	values		worst	case o	perati	ing condition of the co
Function	Table							

	Inp	Output		
L	P	SD	CK	Q
L L H	L H X X	X X L H	X X †	L H L H

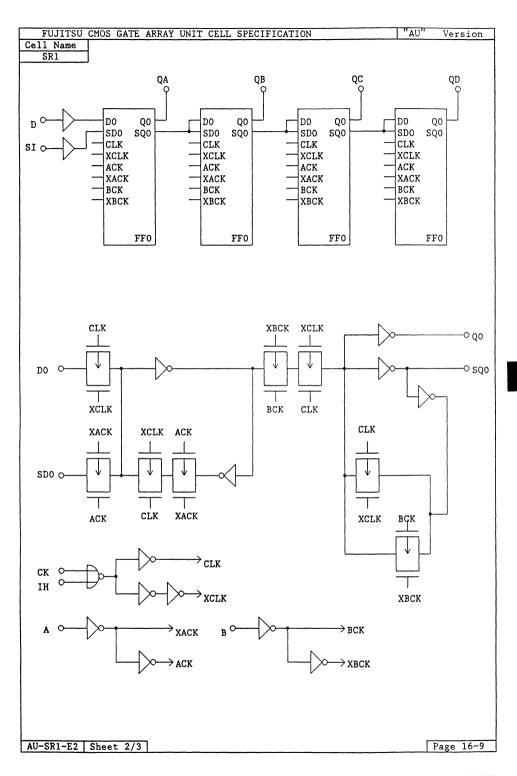
AU-FS3-E3 | Sheet 1/3

Page 16-5





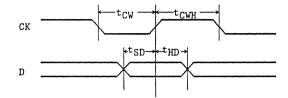
FUJITSU CMOS GAT		NIT CEL	L SPECI	FICATIO	N		JA"	
Cell Name Function	n							Number of BC
SR1 4-bit S	erial-in	Paralle	1-out S	hift Re	gister	with SC	AN	36
Cell Symbol				agation			er	
		t0	up KCL	t0	td KCL	KCL2	CDR2	Path
		2.62	0.07	2.70	0.06	0.09	7	CK → Q
		2.07	0.07	2.32	0.06	0.09	7	B → Q
						i I	1	
				İ			1	
D _	QA						1	
1	QB							
CK —	QC						1	
IH —	QD							
A -							}	
в —				1				1
		Darrie	<u></u>					T ()
		Parame	ter Pulse W	idth			tCW	Typ(ns)* 4.4
		Clock	Pause T	Ime			tCWH	4.5
		Data S	Pause T etup Ti	me			tSD	2.7
		Data H	old Tim	е			≉HD	1.2
Input	Loading							
Pin Name Factor								
D	1							
CK IH	1 1							
SI	1							
A,B	1							
	Driving							
Pin Name Factor	(lu) 36							
		* Mini	mum val	ues for	the ty	pical o	operat:	ing condition.
		The	values	for the	worst	case of	perati	ng condition
		are	given c	y the m	aximum	delay r	nultip.	lier.
AU-SR1-E2   Sheet 1,	/3							Page 16-8



"AU" Version

Cell Name SR1

Definitions of Parameters

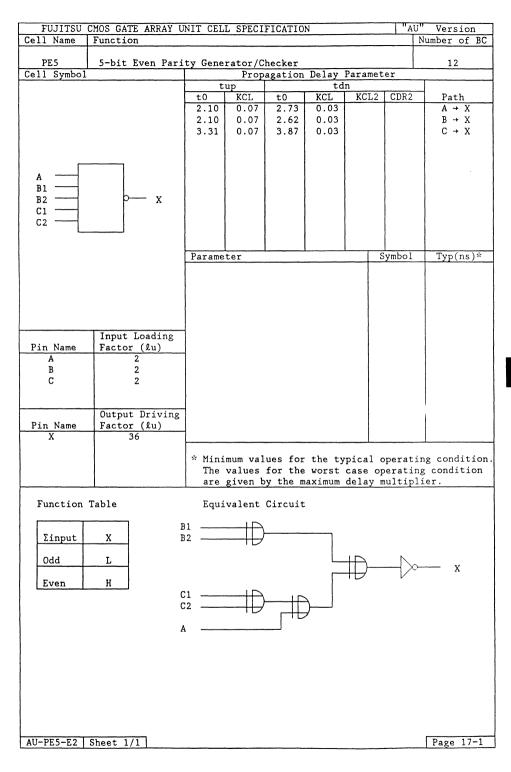


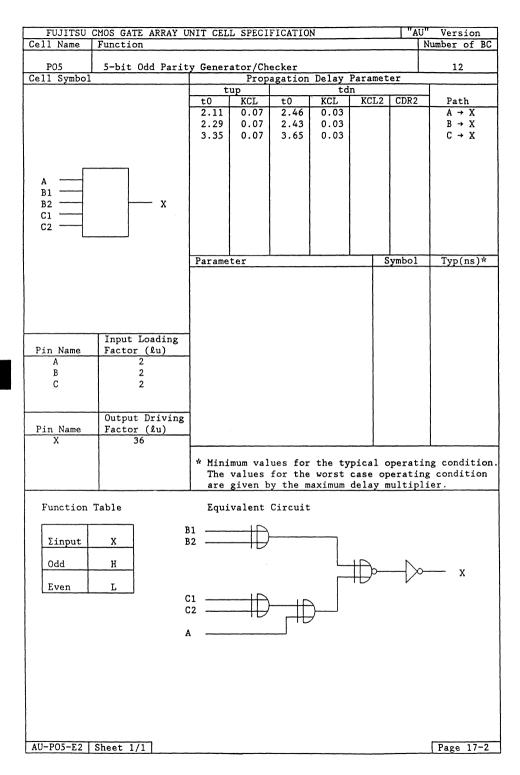
2

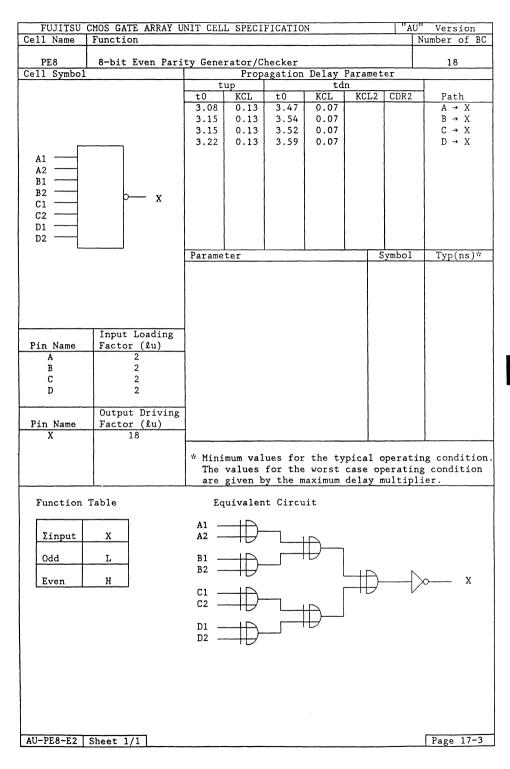
AU-SR1-E2 | Sheet 3/3

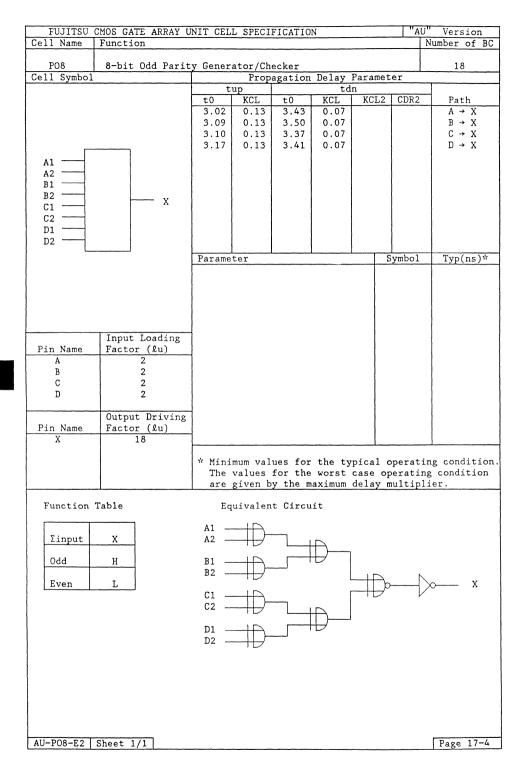
# Parity Generator/Selector/Decoder Family

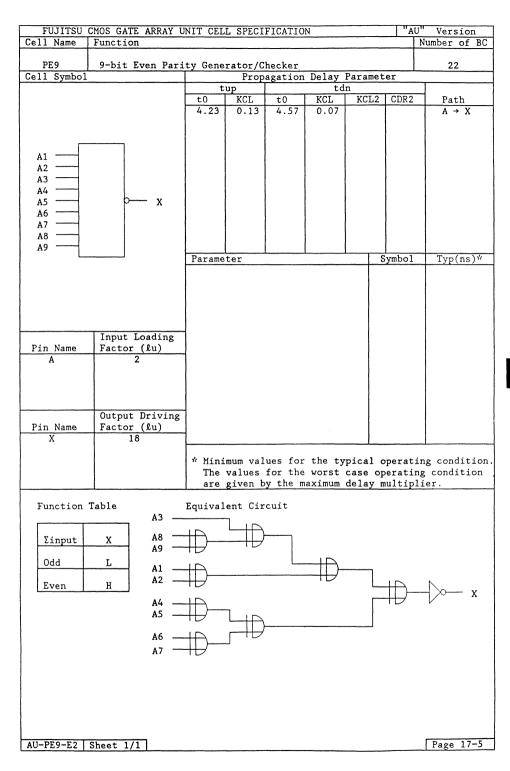
Page	Unit Cell Name	Function	Basic Cells
Parity Ger	nerators/Ch	eckers	
2-287	PE5	5-bit Even Parity Generator/Checker	12
2-288	PO5	5-bit Odd Parity Generator/Checker	12
2-289	PE8	8-bit Even Parity Generator/Checker	18
2-290	PO8	8-bit Odd Parity Generator/Checker	18
2-291	PE9	9-bit Even Parity Generator/Checker	22
2–292	PO9	9-bit Odd Parity Generator/Checker	22
Data Sele	ctor		
2–293	P24	4-wide 2:1 Data Selector	12
Decoders			
2-294	DE2	2:4 Decoder	5
2-295	DE3	3:8 Decoder	15
2-297	DE4	2:4 Decoder with Enable	8
2–298	DE6	3:8 Decoder with Enable	30
Selectors			
2-300	T2B	2:1 Selector	2
2-301	T2C	Dual 2:1 Selector	4
2-303	T2D	2:1 Selector	2
2-304	T2E	Dual 2:1 Selector	5
2-305	T2F	2:1 Selector	8
2-307	T5A	4:1 Selector	5
2-309	V3A	1:2 Selector	2
2–310	V3B	Dual 1:2 Selector	4
Magnitude	e Comparat	or	
2-311	MC4	4-bit Magnitude Comparator	42

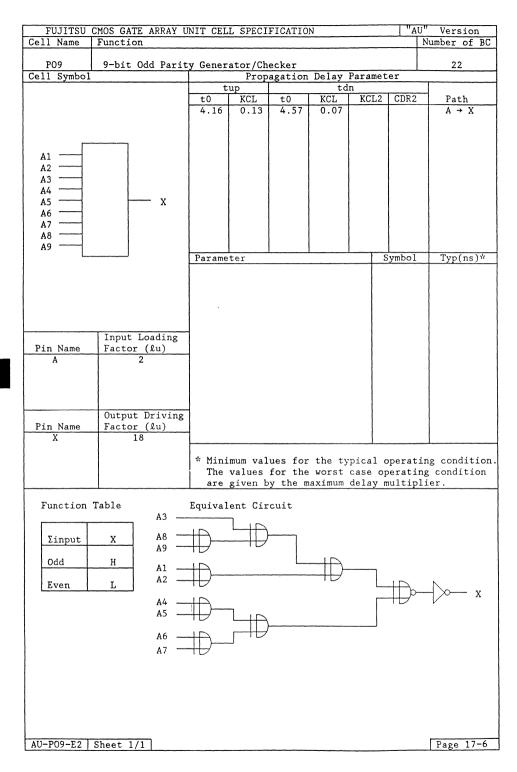


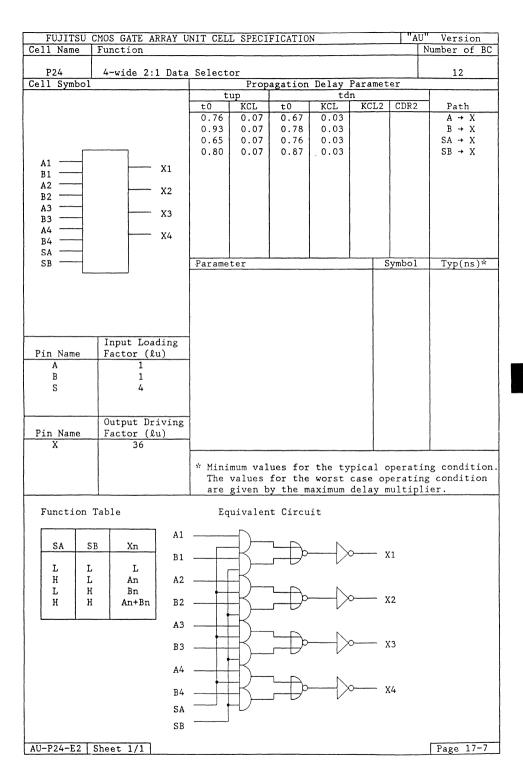


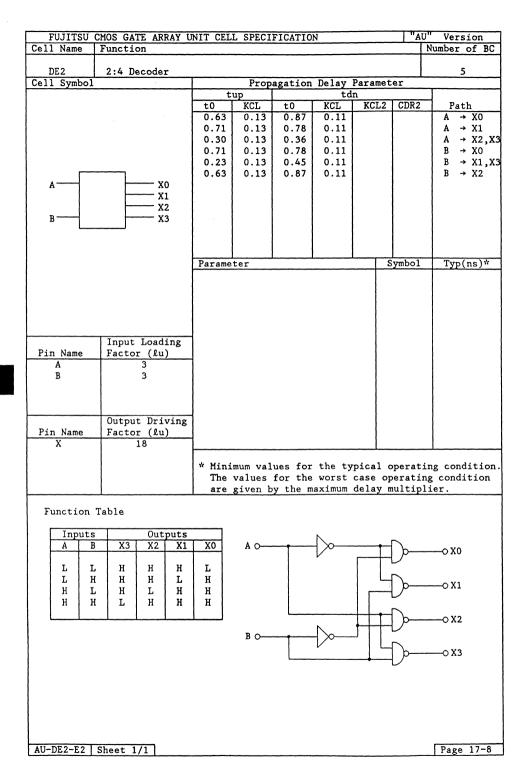








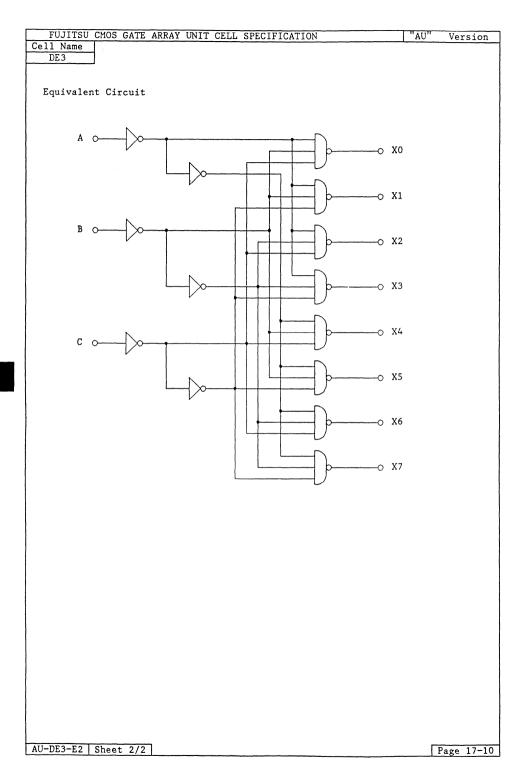




	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	
Cell Name	Function							Number of BC
DE3	3:8 Decoder							15
Cell Symbol				agation	Delay		er	
			up		td		anna	4
		t0 1.15	KCL 0.13	t0 1.34	0.15	KCL2	CDR2	Path A → X0~X3
		1.13	0.13	1.34	0.15		1	$A \rightarrow X0 \sim X3$ $A \rightarrow X4 \sim X7$
		1.93	0.13	1.38	0.15		l	$B \rightarrow X0 \sim X3$
		1.87	0.13	1.99	0.15			$B \rightarrow X4 \sim X7$
1	xo	0.99	0.13	1.43	0.15			C → X0~X3
A	x1	1.79	0.13	2.64	0.15		ļ	C → X4~X7
	x2	1	0.15	2.01	0.15		ļ	1
_	x3							
В —	X4	i l					İ	
1	X5	1					ŀ	
c —	X6							
1	X7							
<b>L</b>							L	
		Parame	ter			S	ymbol	Typ(ns)*
						1		
						l		
						1		
						1		
		l				İ		
	Input Loading	1						
Pin Name	Factor (lu)	<u> </u>						
A	1							
В	1							
C	1							
		]						
	Output Driving	1				1		
Pin Name	Factor (lu)					1		
X	14							
						_ / 1		
								ing condition
			values given b					ng condition
	1	l are	Riven p	y the m	aximum	ueray II	in r c i b i	TET.

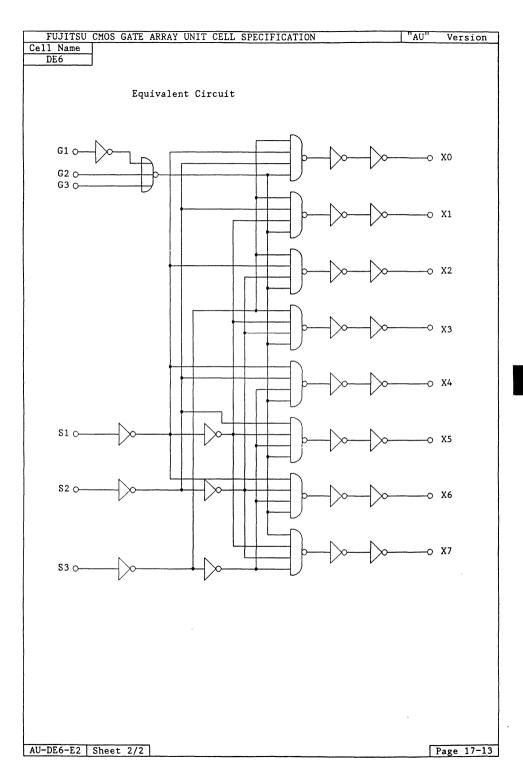
In	puts	5				Outp	uts			
A	В	С	X0	X1	X2	Х3	Х4	X5	Х6	X7
L	L	L	L	н	н	н	Н	Н	Н	Н
Ĺ	$_{ m L}$	H	н	L	H	H	H	H	H	H
Ĺ.	Н	L	н	H	L	H	H	H	Н	Н
_	Н	Н	н	H	H	L	H	Н	H	Н
H	L	L	н	Н	H	H	L	H	H	Н
Ŧ	L	Н	н	H	H	H	H	L	Н	Н
H	H	L	Н	H	Н	H	H	H	L	Н
H	Н	H	Н	H	H	H	H	H	H	L

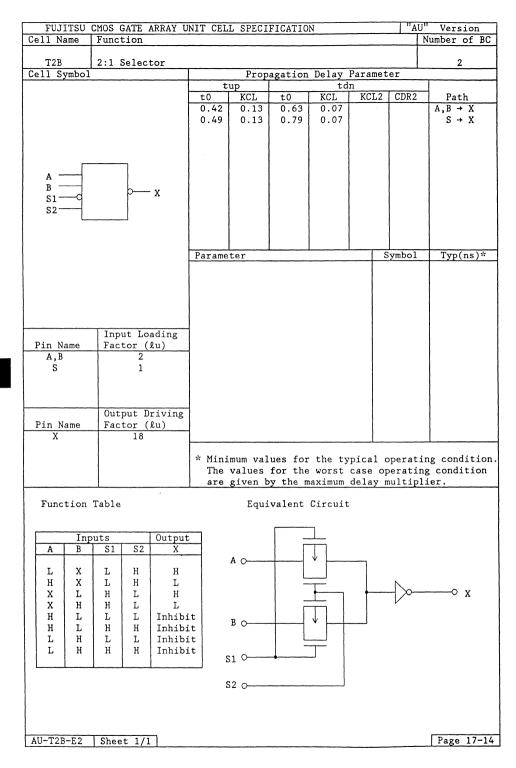
AU-DE3-E2 | Sheet 1/2 | Page 17-9

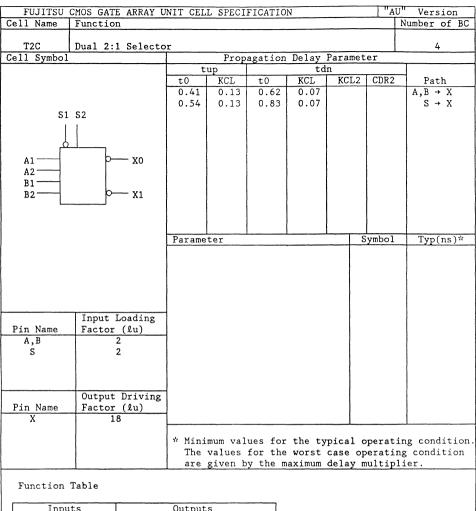


	וופדוווים	CMOS CATE ADDAY I	NIT CELL EDECIFICATION	"AU" Version
DE4	Cell Name		THE CELL SPECIFICATION	Number of BC
Propagation Delay Parameter   Tunum values for the typical operating condition   The values for the worst case operating condition are given by the maximum delay multiplier.   Function Table			1 7 11	
Tup		2:4 Decoder wit		
Description   Top   Top   Top   Top	Jerr Bymbor		tup tdn	
Description   Continue				
Pin Name   Input Loading   Factor (\$\mathbb{L}\$)   Factor (\$\mathbb{L}\$)   Factor (\$\mathbb{L}\$)   Function Table   Function				
B X2 X2 X1 X0  Fin Name Factor (Ru)  A 3 B 3 G 1  Pin Name Factor (Ru)  X 14  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table Equivalent Circuit  G A B X3 X2 X1 X0 H X X H H H H L H L L L H H H H L H L L L H H H H				
Pin Name   Input Loading   Parameter   Symbol   Typ(ns)*    Parameter   Symbol   Typ(ns)*   Pa				
B X2 X2 X1 X0  Fin Name Factor (Ru)  A 3 B 3 G 1  Pin Name Factor (Ru)  X 14  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table Equivalent Circuit  G A B X3 X2 X1 X0 H X X H H H H L H L L L H H H H L H L L L H H H H	_			
Parameter    Parameter   Symbol   Typ(ns)*	Α	р xo		
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u)  A 3 B 3 G 1  Pin Name Factor (£u)  X 14  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Equivalent Circuit  G A B X3 X2 X1 X0 H X X H H H H L L L L H H H H L L L L H H H H	В —	1.		
Pin Name   Input Loading   Factor (Lu)   A   B   S   S   S   S   S   S   S   S   S	G —d			
Pin Name   Input Loading   Factor (&u)    A				
Pin Name   Input Loading   Factor (&u)    A				
Pin Name   Factor (Lu)   A   3   B   3   G   1    Pin Name   Factor (Lu)	1		Parameter	Symbol Typ(ns)*
Pin Name   Factor (Lu)   A   3   B   3   G   1    Pin Name   Factor (Lu)				
Pin Name   Factor (Lu)   A   3   B   3   G   1    Pin Name   Factor (Lu)				
Pin Name   Factor (Lu)   A   3   B   3   G   1    Pin Name   Factor (Lu)				
Pin Name   Factor (Lu)   A   3   B   3   G   1    Pin Name   Factor (Lu)				
A B 3 G 1  Pin Name Factor (Lu)  X 14  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table Equivalent Circuit  G A B X3 X2 X1 X0 H X X H H H H H L L L L H H H H L H L L L H H H H		Input Loading		
B G 1  Pin Name Output Driving Factor (£u)  X 14  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table Equivalent Circuit  G A B X3 X2 X1 X0  H X X H H H H H  L L L L H H H H L  L L L H H H H		Factor (lu)		
G 1  Pin Name Factor (Lu)  X 14  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table Equivalent Circuit  G A B X3 X2 X1 X0  H X X H H H H H  L L L H H H H L H  L L L H H H H	5			
Pin Name   Factor (Lu)		1		
Pin Name   Factor (Lu)				
* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Equivalent Circuit  G A B X3 X2 X1 X0 H X X H H H H H L L L L H H H H L L L L H H H H		Output Driving		
* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Equivalent Circuit  G A B X3 X2 X1 X0 H X X H H H H A L L L L H H H H L L L L H H H H L H L H L H				
The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Equivalent Circuit  G A B X3 X2 X1 X0  H X X H H H H H  L L L L H H H H L  L L H H H H	, x	14		
are given by the maximum delay multiplier.    Function Table   Equivalent Circuit				
Function Table Equivalent Circuit  G A B X3 X2 X1 X0  H X X H H H H H  L L L H H H H L  L L H H H H				
G A B X3 X2 X1 X0  H X X H H H H A  L L L H H H H L H  L H L H L H H H  L H L H				
H X X H H H H L L L L H H H L H L H L H	Function	Table	Equivalent	Circuit
H X X H H H H L L L L H H H L H L H L H				
L L L H H H L L L L L H L L L L L L L L	G A	B X3 X2	X1 X0 G	
L L L H H H L L H L H L H L H L H L H L		х н н	н н А	xo
L   H L   H L H H       L	1 1 1			<del>                                      </del>
	1 [ 1		ľ	LT     X1
		l l	1	<del>       </del> U
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	•			X2
B			В — — — — — — — — — — — — — — — — — — —	<del>                                     </del>
			V	
X3				b x3
			L	——U
AU-DE4-E2   Sheet 1/1   Page 17-11	AU-DE4-E2	Sheet 1/1		Page 17-11

Γ	FUJI	rsu cmo	OS G	ATE	ARRAY	UN	IT CEL	L SPI	CIF	ICAT	ION				".	AU"	Version
Ce]	1 Nar		unct														umber of BC
	DE6	Ι,	2.0	Dooo	do= .	.:+h	Enabl	•									30
Ce l	1 Syr		3.0	Deco	uer v	1	Eliabi		ора	gati	on D	elay	Para	met	er		
						T	t	up				to	ln				
							t0	KCI		t0		KCL	K	L2	CDR	2	Path
							2.44	0.1		2.6	- 1	0.07 0.07	1				$G \rightarrow X$ $S \rightarrow X$
							2.51	0.1		2.0		0.07					b / k
				7													
1	31	1			X0				1		l			l			
	32 — 33 —				· X1 · X2						ı						
					- X3								1				
	51 — 52 —	$\Box$		-	- X4				l								
I	33				X5												
					- X6 - X7								1	-			
		L		ل	Λ/												
							Parame	ter						S	ymbo	1	Typ(ns)*
						1								1			
						_								1			
D-	in Nar	mo   :	Inpu Fact	t Lo or (	ading	3								1			
	G	iie i	ract	1	λu)	-											
	S	İ		1										1			
		1				1											
		- 1	Outr	out D	rivi	ng											
P:	in Na	me ]	Fact	or (	lu)	_								1			
	Х	1		18		F								1			
1						.	* Mini	י חנוח	valu	ies f	or t	he ty	zpic:	al o	pera	tin	g condition.
		- 1					The	value	es f	or t	he w	orst	cas	е ор	erat	ing	condition
<u> </u>							are	give	n by	the	max	imum	dela	ay m	ulti	pli	er.
١,	Funct	ion Tal	hle														
	unct	1011 1d	216														
[			$\neg \top$														
	G1	G2+G	3	S3	S2	S1	X7	X6	X5	X4	Х3	X2	X1	X0	4		
	х	Н		х	х	х	н	Н	н	н	Н	н	Н	Н			
	L	X		X	X	X	Н	Н	Н	Н	Н	Н	Н	Н			
		_		_	_	_											
	H H	L L		L L	L L	L H	H	H H	H H	H H	H	H H	H L	L H			
	H	L		L	H	н L	H	H H	H H	H	H H	H L	H	H H			
	н	L		Ĺ	Н	H	H	н	H	Н	L	н	н	Н	1		
	Н	L		Н	L	L	Н	Н	H	L	H	H	H	Н			
	H H	L L		H H	L H	H L	H	H L	L H	H H	H H	H H	H H	H H			
	H	L		н Н	н Н	H	L	H	H	н Н	n H	н Н	н Н	н Н			
Ι.															_		
1																	
AU	-DE6-	E2 Sh	eet	1/2	]												Page 17-12



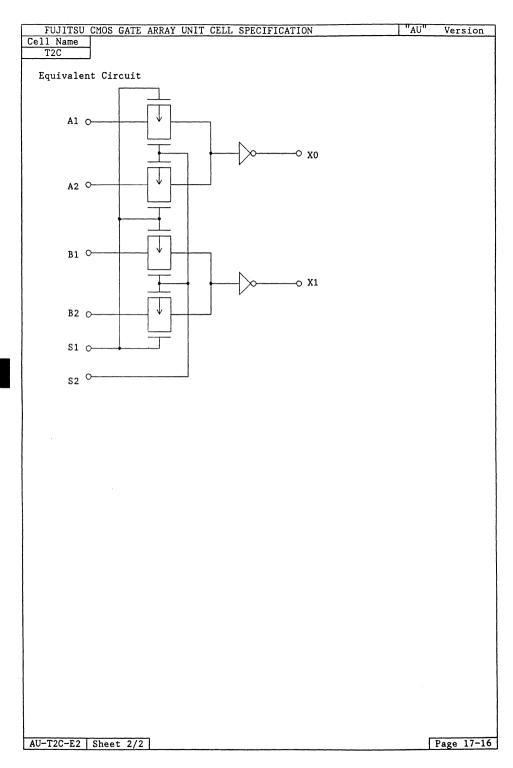


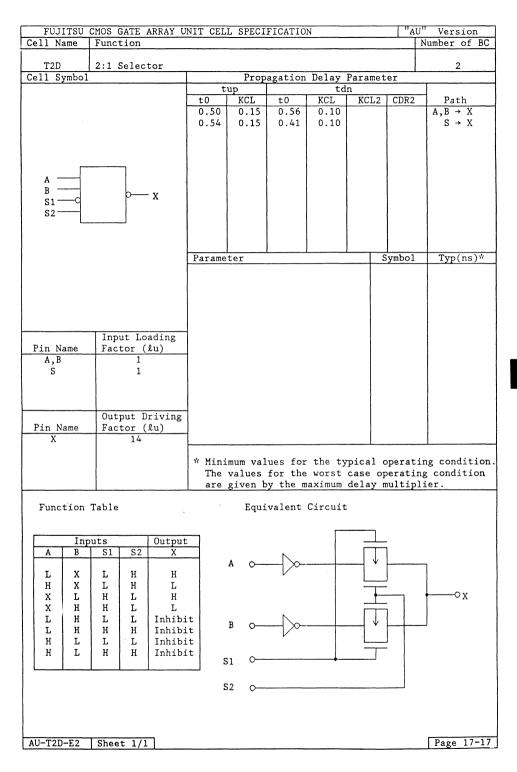


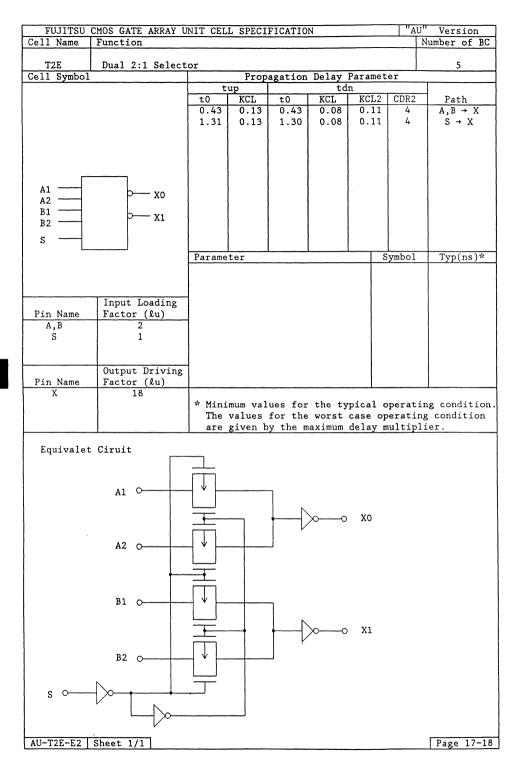
	Inp	uts	Outputs						
A:	l,B1	A2,B2	S1	S2	X0	X1			
	_								
	L	X	L	H	H	Н			
	H	Х	L	H	L	L			
	X	L	Н	L	Н	Н			
1	X	н	н	L	L	L			
	L	н	L	L	Inhibit	Inhibit			
1	H	L	L	L	Inhibit	Inhibit			
1	L	н	н	н	Inhibit	Inhibit			
ł	H	L	н	н	Inhibit	Inhibit			

AU-T2C-E2 | Sheet 1/2

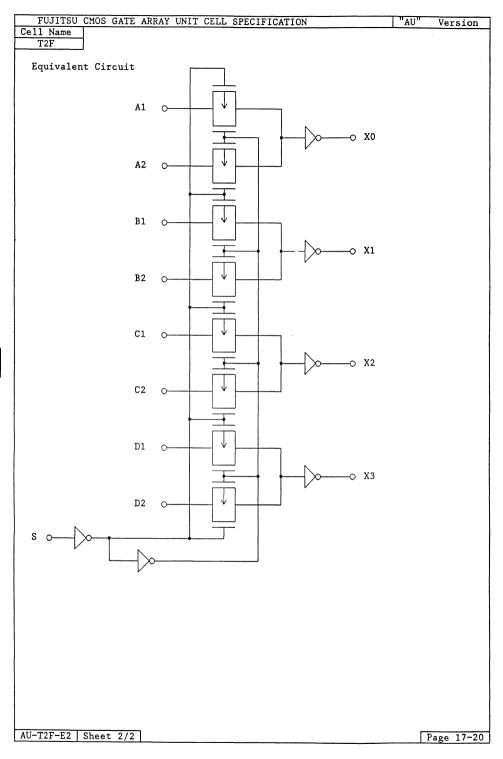
Page 17-15







FUJITSU CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	J" Version Number of BC
T2F 2:1 Selector Cell Symbol		Prop	agation	Delay	Paramet	er	8
CCII Bymbol	Propagation Delay Parameter tup tdn					-	
	t0	KCL	t0	KCL	KCL2	CDR2	Path
	0.43	0.13	0.43	0.08	0.11	4	A,B,
	1.31	0.13	1.30	0.08	0.11	4	$C,D \rightarrow X$ $S \rightarrow X$
		0.120	2.00				
A1 ————————————————————————————————————							
R1 —							
B2 —— X1							
C1 ————————————————————————————————————							
n1 ——							
D2 — X3							
s	Parama	+		İ		ymbol	Typ(ps)%
	Parame	rer				ymboi	Typ(ns)*
					ŀ		
Input Loading Pin Name Factor (lu)							
Pin Name Factor (lu) A,B,C,D 2							1
S 1							
Output Driving							
Pin Name Factor (lu) X 18							
X 18							
	* Mini	mum val	ues for	the ty	pical c	perat:	ing condition.
	The	values	for the	worst	case or	erati	ng condition
	are	given b	y the m	aximum	delay m	nultip.	lier.
•							
							Page 17-19



FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
	4:1 Selector							5
Cell Symbol				agation	Delay	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.80	0.19	0.80	0.13			A,B → X
S1 0	2 S3 S4	0.80	0.19	0.67	0.13			S1~4 → X
1	1 1 1	0.45	0.19	0.43	0.13			S5~6 → X
۰. ح								
A1								
A2	- v							
B1	р х							
B2								
۔								
	1							
S5	) C4							
33	20	Parame	tor			1 8	ymbol	Typ(ns)*
		rarame	rei				ymboi	Typ(IIS)"
						į		
	Input Loading							
Pin Name	Factor (lu)							
A,B	1							
, 2 S	ī							
_	_							
	Output Driving	1						
Pin Name	Factor (lu)					l.		
X	9	1						
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition
								ng condition
					naximum			

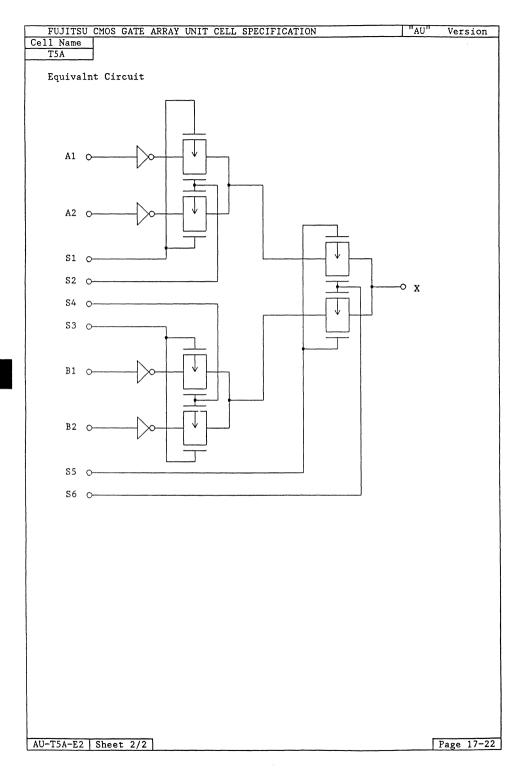
#### Function Table

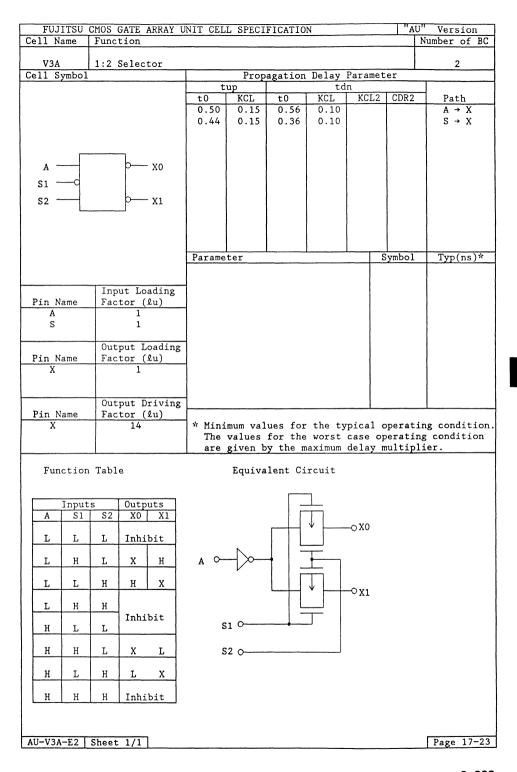
	Inputs										
A1	A2	B1	B2	S1	S2	S3	S4	S5	S6	X	
L H	L H	L H	L H	L H H	H H L L	L L H H	H H L L	L L L H H	H H H L L L	H L H L H L	

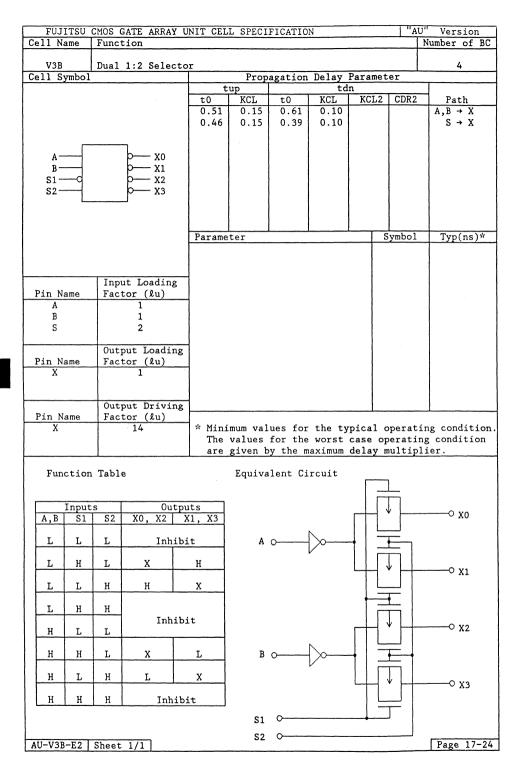
A1 $\neq$ A2  $\rightarrow$  S1=S2 or S5=S6 Inhibit B1 $\neq$ B2  $\rightarrow$  S3=S4 or S5=S6 Inhibit A1,A2 $\neq$ B1,B2 or S5=S6 Inhibit

AU-T5A-E2 | Sheet 1/2

Page 17-21





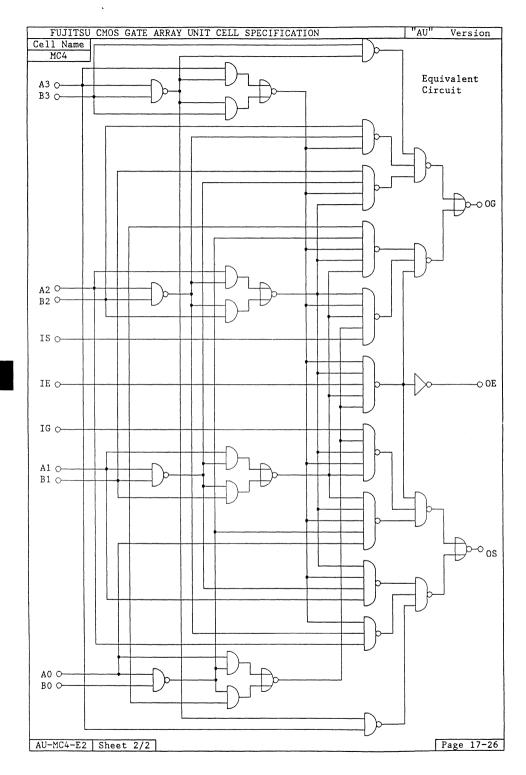


Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"Al	U" Version Number of BC
Cell Name	Function							Number of BC
MC4	4-bit Magnitude	Compar	ator					42
Cell Symbol				agation	Delay	Paramet	er	
			up		td			
l		t0	KCL	t0	KCL	KCL2	CDR2	Path
		4.23	0.23	5.06	0.07	0.09	4	A → OS
		4.31	0.23	4.97	0.07	0.09	4	B → OS
B2		1.89	0.23	2.23 1.93	0.07	0.09	4	IE → OS IG → OS
A3 B3 ==================================		4.15	0.23	5.23	0.07	0.09	4	A → OG
A1 B1		4.22	0.23	5.14	0.07	0.09	4	B → OG
AO BO		1.80	0.23	2.39	0.07	0.09	4	IE → OG
AU		1.71	0.23	1.85	0.07	0.09	4	IS → OG
IG-	OG	4.55	0.13	3.49	0.07	0.10	4	A → OE
IE-	OE	4.47	0.13	3.56	0.07	0.10	4	B → OE
IS-	os	1.71	0.13	1.15	0.07	0.10	4	IE → OE
							}	
		Denie				L .	ymbol	T () *
		Parame	ter				ymbol	Typ(ns)*
						Į.		
		}						
	Input Loading	]						
Pin Name	Factor (lu)	1						
A	3							
B IE	3 1							
IG	1	1						
IS	1							
1	1							
	Output Driving	1						
Pin Name	Factor (lu)							
OE	18							
OG	10				41	1		
OS	10							ing condition. ng condition
					aximum			
	_l	1 216	9 T V C11 D	, circ ii	CALTINGIII	uciay II		

#### Function Table

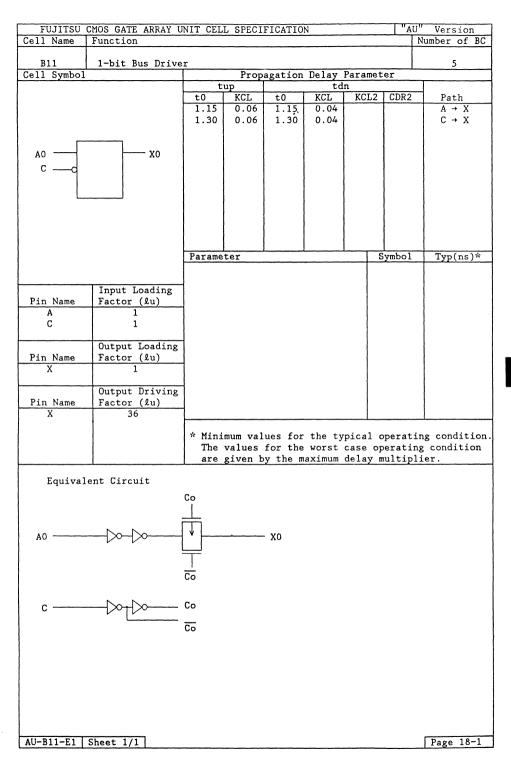
	Comparin	g Inputs		Casca	ding In	puts		Outputs	
	40.00		10.70	IG	IS	IE	OG (A)	OS	OE
A3,B3	A2,B2	A1,B1	AO,BO	(A>B)	(A <b)< td=""><td>(A=B)</td><td>(A&gt;B)</td><td>(A<b)< td=""><td>(A=B)</td></b)<></td></b)<>	(A=B)	(A>B)	(A <b)< td=""><td>(A=B)</td></b)<>	(A=B)
A3>B3	х	x	x	x	х	х	н	L	L
A3 <b3< td=""><td>X</td><td>x</td><td>X</td><td>X</td><td>X</td><td>Х</td><td>L</td><td>н</td><td>L</td></b3<>	X	x	X	X	X	Х	L	н	L
A3=B3	A2>B2	X	x	X	Х	Х	н	L	L
A3=B3	A2 <b2< td=""><td>X</td><td>X</td><td>Х</td><td>X</td><td>X</td><td>L</td><td>Н</td><td>L</td></b2<>	X	X	Х	X	X	L	Н	L
A3=B3	A2=B2	A1>B1	X	Х	Х	Х	Н	L	L
A3=B3	A2=B2	A1 <b1< td=""><td>X</td><td>Х</td><td>Х</td><td>Х</td><td>L</td><td>Н</td><td>L</td></b1<>	X	Х	Х	Х	L	Н	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	Н	L	L
A3=B3	A2=B2	A1=B1	A0 <b0< td=""><td>X</td><td>X</td><td>X</td><td>L</td><td>H</td><td>L</td></b0<>	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	AO=BO	Х	X	H	L	L	H
A3=B3	A2=B2	A1=B1	AO=BO	H	L	L	Н	L	L
A3=B3	A2=B2	A1=B1	AO=BO	L	Н	L	L	H	L
A3=B3	A2=B2	A1=B1	AO=BO	H	Н	L	L	L	L
A3=B3	A2=B2	A1=B1	AO=BO	L	L	L	Н	H	L
						1	l	l	

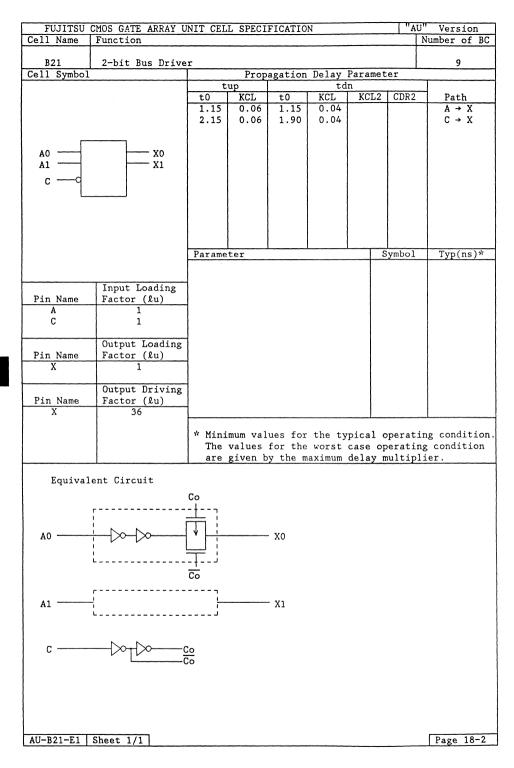
AU-MC4-E2 | Sheet 1/2 | Page 17-25

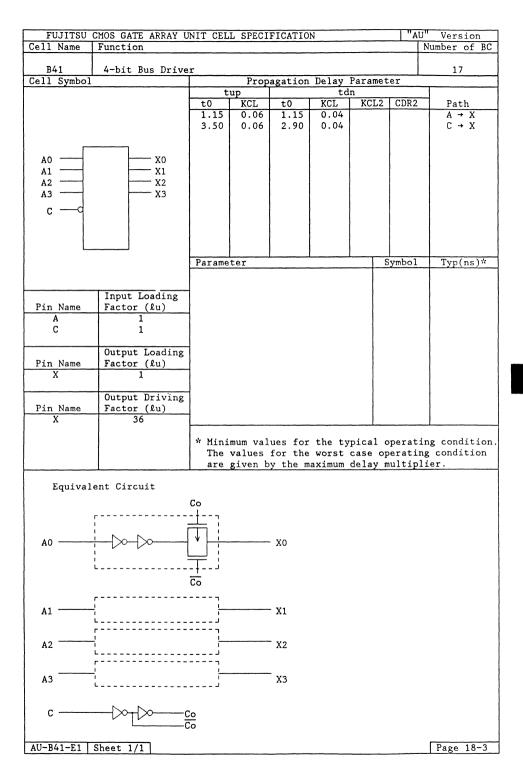


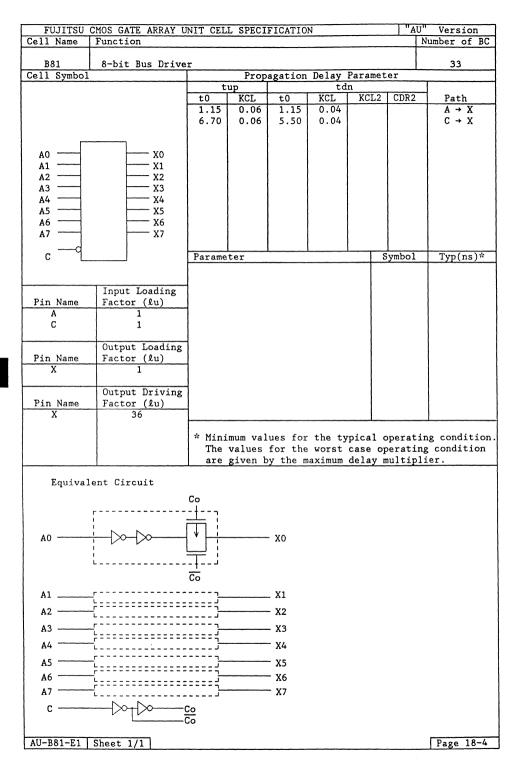
## **Bus Driver Family**

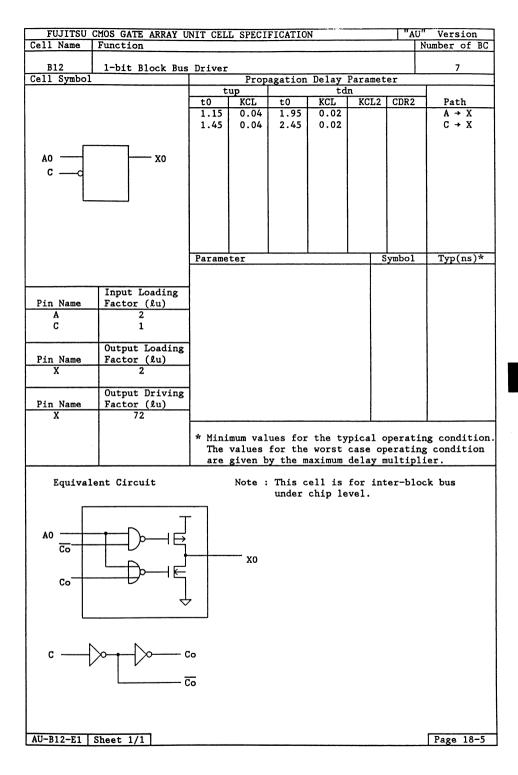
Page	Unit Cell Name	Function	Basic Cells
·			
2–315	B11	1-bit Bus Driver	5
2-316	B21	2-bit Bus Driver	9
2-317	B41	4-bit Bus Driver	17
2-318	B81	8-bit Bus Driver	33
2–319	B12	1-bit Block Bus Driver	7
2-320	B22	2-bit Block Bus Driver	13
2-321	B42	4-bit Block Bus Driver	25

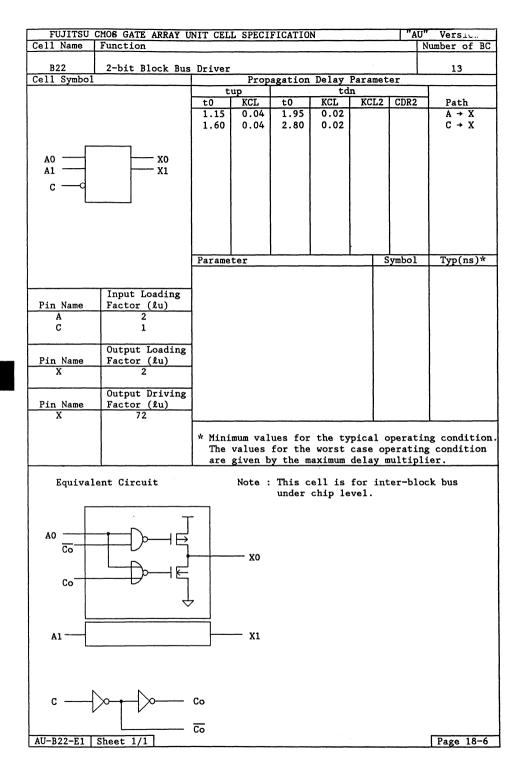


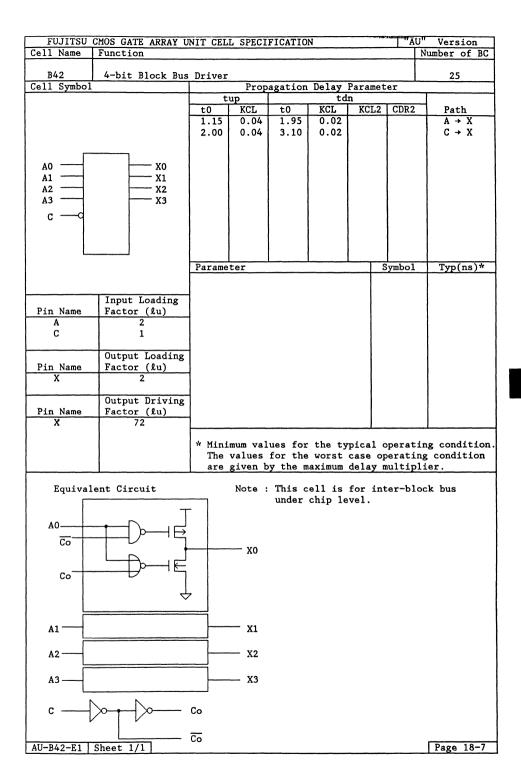












# **Clip Cell Family**

Page	Unit Cel Name	1	Function	Basic Cells
2-325	Z00	0 Clip		0
2-326	Z01	1 Clip		0

FUJITSU Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	J" Version Number of BC
Z00	0 Clip							0
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t0	up KCL	t0	td KCL	n KCL2	CDR2	Path
		LU	KCL	10	KCL	KCDZ	CDRZ	rath
	X							
	$\downarrow$							
	$\triangle$							
	:						<u> </u>	
		Parame	ter			S	ymbol	Typ(ns)*
						ł		
						1		
Din Nama	Input Loading Factor (lu)							
Pin Name	ractor (ku)							
						ļ		
- ·	Output Driving							
Pin Name X	Factor (lu)							
						l		
		* Mini	mum val	ues for	the ty	pical o	perat:	ing condition. ng condition
		are	given b	y the m	aximum	delay m	ultip.	lier.
1								
1								
AU-700-F1	<u> </u>							Page 19-1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	
Cell Name	Function							Number of BC
Z01	1 Clip							0
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
				1				
				Ì				
				1				
[								1
				1	ì			
	abla							
	$\bigvee$	i	1	1	Ì	· ·		-
					1			
			1	l				
	X		ļ	1				
			l		ļ			
		Parame	ter			S	ymbol	Typ(ns)*
ļ								
į								
	Input Loading					1		
Pin Name	Factor (lu)							
	j							
	1							
	Output Driving					į		
Pin Name	Factor (lu)							1
Х	200							
İ		* Mini	mum 1701	was for	tho to	nical c	norat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	naximum	delay n	ultip	lier.
		L						
Ì								
AU-201-E1	Sheet 1/1							Page 19-2

# I/O Buffer Family

Page	Unit Cell Name	Function	Basic Cells
2-331	I1B	Input Buffer (Inverter)	5
2-332	I1BU	I1B with Pull-up Resistance	5
2-333	I1BD	I1B with Pull-down Resistance	5
2-334	I2B	Input Buffer (True)	4
2-335	I2BU	12B with Pull-up Resistance	4
2-336	I2BD	I2B with Pull-down Resistance	4
2-337	IKB	Clock Input Buffer (Inverter)	4
2-338	IKBU	IKB with Pull-up Resistance	4
2-339	IKBD	IKB with Pull-down Resistance	4
2-340	ILB	Clock Input Buffer (True)	8
2-341	ILBU	ILB with Pull-up Resistance	8
2-342	ILBD	ILB with Pull-down Resistance	8
2-343	I1C	CMOS Interface Input Buffer (Inverter)	5
2-344	I1CU	I1C with Pull-up Resistance	5
2-345	I1CD	I1C with Pull-down Resistance	8 5 5 4 4
2-346	12C	CMOS Interface Input Buffer (True)	4
2-347	I2CU	I2C with Pull-up Resistance	4
2-348	I2CD	I2C with Pull-down Resistance	4
2-349	I1S	Schmitt Trigger Input Buffer (CMOS Type, Inverter)	8
2-350	I1SU	I1S with Pull-up Resistance	8
2-351	I1SD	I1S with Pull-down Resistance	8
2-352	128	Schmitt Trigger Input Buffer (CMOS Type, True)	8
2-353	I2SU	I2S with Pull-up Resistance	8
2-354	I2SD	I2S with Pull-down Resistance	8
2-355	I1R	Schmitt Trigger Input Buffer	8
2-356	I1RU	I1R with Pull-up Resistance	8
2-357	I1RD	I1R with Pull-down Resistance	8
2-358	I2R	Schmitt Trigger Input Buffer (TTL Type, True)	8
2-359	I2RU	I2R with Pull-up Resistance	8
2-360	I2RD	I2R with Pull-down Resistance	8
2-361	O1B <sup>1</sup>	Output Buffer (Inverter)	3
2-362	O1L <sup>2</sup>	Power Output Buffer (Inverter)	3
2-363	O1R1	Output Buffer (Inverter) with Noise Limit Resistance	5
2-364	O1S <sup>2</sup>	Power Output Buffer (Inverter) with Noise Limit	
		Resistance	5
2-365	O2B <sup>1</sup>	Output Buffer (True)	3
2-366	O2L <sup>2</sup>	Power Output Buffer (True)	3
2-367	02R1	Output Buffer (True) with Noise Limit Resistance	4
2-368	O2S <sup>2</sup>	Power Output Buffer (True) with Noise Limit Resistance	4
2–369	O4R <sup>1</sup>	3-state Output Buffer (True) with Noise Limit Resistance	5
2–370	O4S <sup>2</sup>	Power 3-state Output Buffer (True) with Noise Limit	5
2-371	O4T <sup>1</sup>	Resistance 3-state Output Buffer (True)	6
2-372	O4W <sup>2</sup>	Power 3-state Output Buffer (True)	6
2-373	H6T <sup>1</sup>	3-state Output and Input Buffer (True)	8
2-374	H6TU <sup>1</sup>	H6T with Pull-up Resistance	8
2–375	H6TD <sup>1</sup>	H6T with Pull-down Resistance	8

<sup>1.</sup> I<sub>OL</sub> = 3.2 mA 2. I<sub>OL</sub> = 12 mA

## I/O Buffer Family (Continued)

Page	Unit Cell Name	Function	Basic Cells
2-376	H6W <sup>2</sup>	Power 3-state Output and Input Buffer (True)	8
2-377	H6WU <sup>2</sup>	H6W with Pull-up Resistance	8
2-378	H6W <sub>D</sub> 2	H6W with Pull-down Resistance	8
2–379	H6C <sup>1</sup>	3-state Output and CMOS Interface Input Buffer	
		(True)	8
2–380	H6CU <sup>1</sup>	H6C with Pull-up Resistance	8
2–381 2–382	H6CD <sup>1</sup> H6E <sup>2</sup>	H6C with Pull-down Resistance Power 3-state Output and CMOS Interface Input	8
2-302	пос-	Buffer (True)	8
2-383	H6EU <sup>2</sup>	H6E with Pull-up Resistance	8
2–384	H6ED <sup>2</sup>	H6E with Pull-down Resistance	8
2-385	H6S <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer	-
		(CMOS Type, True)	12
2-386	H6SU <sup>1</sup>	H6S with Pull-up Resistance	12
2–387	H6SD <sup>1</sup>	H6S with Pull-down Resistance	12
2–388	H6R <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer	
		(TTL Type, True)	12
2-389	H6RU <sup>1</sup>	H6R with Pull-up Resistance	12
2–390 2–391	H6RD <sup>1</sup> H8T <sup>1</sup>	H6R with Pull-down Resistance 3-state Output with Noise Limit Resistance and	12
2-391	пот	Input Buffer (True)	9
2-392	H8TU¹	H8T with Pull-up Resistance	9
2-393	H8TD1	H8T with Pull-down Resistance	9
2-394	H8W <sup>2</sup>	Power 3-state Output with Noise Limit Resistance and	-
		Input Buffer (True)	9
2-395	H8WU <sup>2</sup>	H8W with Pull-up Resistance	9
2-396	H8W <sub>D</sub> 2	H8W with Pull-down Resistance	9
2–397	H8C <sup>1</sup>	3-state Output Buffer with Noise Limit Resistance	
		and CMOS Interface Input Buffer (True)	9
2-398	H8CU <sup>1</sup>	H8C with Pull-up Resistance	9
2–399 2–400	H8CD <sup>1</sup> H8E <sup>2</sup>	H8C with Pull-down Resistance	9
2-400	HOE	Power 3-state Output Buffer with Noise Limit Resistance and CMOS Interface Input Buffer (True)	9
2-401	H8EU <sup>2</sup>	H8E with Pull-up Resistance	9
2-402	H8ED <sup>2</sup>	H8E with Pull-down Resistance	9
2-403	H8S <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer	
		(CMOS Type, True) with Noise Limit Resistance	13
2-404	H8SU <sup>1</sup>	H8S with Pull-up Resistance	13
2-405	H8SD <sup>1</sup>	H8S with Pull-down Resistance	13
2-406	H8R <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer	
		(TTL Type, True) with Noise Limit Resistance	13
2-407	H8RU <sup>1</sup>	H8R with Pull-up Resistance	13
2–408 2–409	H8RD <sup>1</sup> IKC	H8R with Pull-down Resistance	13
2-410	IKCU	CMOS Interface Clock Input Buffer (Inverter) IKC with Pull-up Resistance	4 4
2-410	IKCD	IKC with Pull-down Resistance	4
2-411	ILC	CMOS Interface Clock Input Buffer (True)	6
- 712	120	Since interact clock input ballet (1140)	3
1.	I <sub>OI</sub> = 3.2 mA		
2.	$l_{OL} = 12 \text{ mA}$		
3.	$I_{OL} = 8 \text{ mA}$		

### I/O Buffer Family (Continued)

Page	Unit Cell Name	Function	Basic Cells
2-413	ILCU	ILC with Pull-up Resistance	6
2-414	ILCD	ILC with Pull-down Resistance	6
2-415	O2BF <sup>3</sup>	Output Buffer	3
2-416	O2RF <sup>3</sup>	Output Buffer with Noise Limit Resistance	4
2-417	O4TF <sup>3</sup>	3-state Output Buffer (True)	6
2-418	O4RF <sup>3</sup>	3-state Output Buffer (True) with Noise Limit	
		Resistance	5
2-419	H6TF <sup>3</sup>	3-state Output and Input Buffer (True)	8
2-420	H6TFU <sup>3</sup>	H6TF with Pull-up Resistance	8
2-421	H6TFD <sup>3</sup>	H6TF with Pull-down Resistance	8
2-422	H6CF <sup>3</sup>	3-state Output and CMOS Interface Input Buffer	8
2-423	H6CFU <sup>3</sup>	H6CF with Pull-up Resistance	8
2-424	H6CFD <sup>3</sup>	H6CF with Pull-down Resistance	8
2-425	H8TF <sup>3</sup>	3-state Output with Noise Limit Resistance	•
		and Input Buffer True)	9
2-426	H8TFU <sup>3</sup>	H8TF with Pull-up Resistance	9
2-427	H8TFD <sup>3</sup>	H8TF with Pull-down Resistance	9
2-428	H8CF <sup>3</sup>	3-state Output Buffer with Noise Limit Resistance	-
		and CMOS Interface Input Buffer (True)	9
2-429	H8CFU <sup>3</sup>	H8CF with Pull-up Resistance	9
2-430	H8CFD <sup>3</sup>	H8CF with Pull-down Resistance	9
2-431	O2S2 <sup>4</sup>	Output Buffer with Noise Limit Resistance	3
2-432	O4S24	3-state Output Buffer (True) with Noise Limit Resistance	
2-433	H8W2 <sup>4</sup>	3-state Output and Input Buffer with Noise Limit	•
00	1.0112	Resistance and Input Buffer (TTL, True)	8
2-434	H8E2 <sup>4</sup>	3-state Output and Input Buffer with Noise Limit	·
	1.022	Resistance and Input Buffer (TTL, True)	8
2-435	H8W1 <sup>4</sup>	3-state Output and Input Buffer with Noise Limit	•
		Resistance and Input Buffer (TTL, True) with	
		Pull-up Resistance	8
2-436	H8E1 <sup>4</sup>	3-state Output and Input Buffer) with Noise Limit	·
		Resistance and Input Buffer (CMOS, True) with	
		Pull-up Resistance	8
2-437	H8WO <sup>4</sup>	3-state Output and Input Buffer with Noise Limit	Ü
2 707	110110	Resistance and Input Buffer (TTL, True) with	
		Pull-down Resistance	8
2-438	H8EO <sup>4</sup>	3-state Output and Input Buffer with Noise Limit	·
2 400	HOLO	Resistance and Input Buffer (CMOS, True) with	
		Pull-down Resistance	8
		i un-down neolotande	O
1.	$I_{OL} = 3.2 \text{ mA}$		
2.	$I_{OL} = 12 \text{ mA}$		
3.	$I_{OL} = 8 \text{ mA}$		
4.	$I_{OL} = 24 \text{ mA}$		

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
I1B Input Buffer (Inverter)						5		
Cell Symbol				agation	Delay	Paramet	er	
		t0	up KCL	t0	td KCL	n KCL2	CDR2	Path
		1.28	0.03	1.23	0.03	RODE	ODICE	X + IN
	_							
х —	>>— IN							
		Parame	ter			S	ymbol	Typ(ns)*
						l		
	1							
Pin Name	Input Loading Factor (lu)							
TIII Name	ractor (ku)							
						j		
	Output Driving					1		
Pin Name	Factor (lu)					İ		
IN	36							
		" mini	mum vai values	ues for	worst	picai c	perat erati	ing condition. ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
		<del></del>	<del></del>	<del> </del>				
AU-I1B-E2	Sheet 1/1							Page 20-1

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	" Version
	Function							Number of BC
	Input Buffer (Inverter)							
I1BU	I1BU with Pull-up Resistance						5	
Cell Symbol				agation	Delay		er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.28	0.03	1.23	0.03			X → IN
							1	
							1	
х —	>> IN							
Λ							1	
							1	
		Parame	ter	L			ymbol	Typ(ns)*
	,							1
								-
						1		
	Input Loading							
Pin Name	Factor (lu)							
	0					- 1		
Din Name	Output Driving					- 1		
Pin Name	Factor (lu)	-						
IN	30	<b></b>						
		* Mini	רפיזי חווח	nes for	the tw	nical 4	nerati	ing condition.
		The	walnes	for the	worst	Case Of	perati	ng condition
		are	given h	v the m	aximum	delav r	nultip	lier.
	A		<u></u>					
1								
1								
1								
AU-I1BU-E2	Sheet 1/1							Page 20-2

PHILIPPIN	ONOC CAME ADDAY U	NITT OF	T ADDAT	DIGIMIO	NT		I II A T	, III
Cell Name	CMOS GATE ARRAY U Function	NII CEL	L SPECI	FICATIO	'N		JA"	J" Version Number of BC
Input Buffer (Inverter)								TARRIDET OF DC
I1BD	with Pull-down R	esistan	, ce	ŀ	5			
Cell Symbol		2213 can	Pron	agation	Delav	Paramet	er	
0011 0701		t	up	180000	td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.28	0.03	1.23	0.03			X → IN
					ļ			
					l		]	
						ļ		
				·		Ì		
							]	
						ļ		
.,	<u></u>						1	
х —	→ IN				ļ			
							1	
					]	ļ		
		Parame	ter	L	I	<u>'                                    </u>	ymbol	Typ(ns)*
							-	'' '
								1
		}						
	T							
Die News	Input Loading					- 1		
Pin Name	Factor (lu)					1		
						1		
		1				ļ		
						1		
	Output Driving							
Pin Name	Factor (lu)					1		
IN	36							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
	L	are	given b	y the m	naximum	delay m	ultip	lier.
								j
								İ
								1
								ļ
								ĺ
AU-I1BD-E2	Sheet 1/1							Page 20-3
	·							

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version Number of BC
								4
I2B Cell Symbol	Input Buffer (T	True) Propagation Delay Parameter						
		up		td	n			
		t0 0.85	KCL 0.03	t0 1.47	KCL 0.03	KCL2	CDR2	Path X → IN
1								
х —	IN							
		Parame	ter			S	ymbol	Typ(ns)*
						l		
Pin Name	Input Loading Factor (lu)							
		1						
	Output Driving	1						
Pin Name IN	Factor (lu)	}						
l IN	36							
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition. ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
1								
AU-I2B-E2	Sheet 1/1							Page 20-4

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	J" Version
Cell Name	Function							Number of BC
	Input Buffer (T	rue)						
I2BU with Pull-up Resistance						4		
Cell Symbol		<u>.</u>		agation	Delay	<u>raramet</u>	er	
		t0	up KCL	t0	td KCL	KCL2	CDR2	ᅴ <sub>Pa+h</sub>
		0.85	0.03	1.47	0.03	KODZ	ODKZ	Path X → IN
		0.05	0.03	1.77	0.05			
		İ						
			1					
	<b>,</b> ,,,							
х —	IN							
		Parame	ter			S	ymbol	Typ(ns)*
						1		
						-		
	Input Loading							
Pin Name	Factor (lu)							
						i		
						1		
	Output Driving							
Pin Name	Factor (lu)							
IN	36							
		* Mini	mum val	ues for	the ty	pical o	perat:	ing condition.
		The	values	for the	worst	case op	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip.	lier.
AU-I2BU-E2	Sheet 1/1							Page 20-5

		AY UNIT CELL SPECIFICATION "						
Cell Name	Function							Number of BC
		rue)					1	
I2BD	with Pull-down R	esistan	ce					4
Cell Symbol			Prop	agation	Delay		er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path X → IN
		0.85	0.03	1.47	0.03			X → IN
		1						
l 1	<b></b>							
х —	→ IN							
•							l	
							1	1
					L	L	٠	<del>    _   </del>
		Parame	ter			s	ymbol	Typ(ns)*
								1
	I T . T 1:							
Din Nama	Input Loading							
Pin Name	Factor (lu)							1
						- 1		
	Out-ut Deisies							1
Din Nama	Output Driving Factor (lu)							
Pin Name IN	36					1		]
114	30							
		ok Mini	mum 3791	ues for	the tw	mical c	norati	ng condition.
		The	walnes	for the	worst	Case or	peratin	g condition
		are	given b	v the m	aximum	delay m	nultipl	ier.
	<u> </u>	410	STYON 2	<i>y</i> •110 11		uciu,		
1								
i								
1								
AU-T2BD-E2	Sheet 1/1							Page 20-6

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	J" Version		
Cell Name	Function			Number of BC						
IKB	Clock Input Buff	er (In	verter)				L	4		
Cell Symbol				agation			er			
			up		td		anna	┥		
		t0	KCL	t0	KCL	KCL2	CDR2	Path X → CI		
		2.05	0.01	1.88	0.01			X → C1		
							j			
							1			
							l			
x	>>— сі									
							į			
		Parame	ter		<u> </u>	1 5	ymbol	Typ(ns)*		
	Input Loading					Ì				
Pin Name	Factor (lu)									
						- 1				
						1				
Din Nama	Output Driving					į				
Pin Name CI	Factor (lu)									
01	200									
		* Mini	mum val	ues for	the tv	pical c	perat	ing condition.		
		The	values	for the	worst	case or	erati	ng condition		
		are	given b	y the m	aximum	delay n	nultip:	lier.		
	•									
AU-IKB-E1	Sheet 1/1							Page 20-7		

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
	Function							Number of BC
TV	Clock Input Buff	er (In	verter)					
IKBU Cell Symbol	with Pull-up Res	istance	Pron	agation	Delay	Paramet	or	4
Cell Symbol		+	up	agation	td	n n	61	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.05	0.01	1.88	0.01			Path X → CI
							]	
							1	
1 .								
x —	>> cī						İ	
1								
							Į.	
]		Parame	ter	L		l s	ymbol	Typ(ns)*
1	:							1
						1		
1								
	Input Loading							
Pin Name	Factor (lu)							
		`						
		1						
	Output Driving	ì						
Pin Name	Factor (lu)	}						
CI	200							
			_	_				
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		Ine	values	y the m	worst	delay m	erati mltin	ng condition
		are	given t	y the n	IAXIIIUIII	deray ii	iurcip	riter.
1								
AU-IKBU-E1	Sheet 1/1							Page 20-8

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	.U" Version
Cell Name	Function							Number of BC
	Clock Input Buff	er (In	verter)					
IKBD	with Pull-down R							4
Cell Symbol			Prop	agation	Delay	Paramet	er	*
		tı	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.05	0.01	1.88	0.01			X → CI
		ļ					İ	
			i					
			l					
			1				1	
			1				1	
х	>>— cī						l	
Λ .	0 01						i	
							1	
		Dom					I rrmh - 1	Tran ( = = ) **
		Parame	rer			<del></del>	Symbol	Typ(ns)*
								i i
				•				
	T							
<b>.</b>	Input Loading					1		
Pin Name	Factor (lu)					1		
						- 1		
						1		
						1		
	Output Driving					ŀ		1
Pin Name	Factor (lu)					,		
CI	200							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
								ng condition
		are	given b	y the m	aximum	delay n	nultip	olier.
AU-IKBD-E1	Sheet 1/1							Page 20-9

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"/	\U"	
Cell Name	Function							N	umber of BC
ILB	Clock Input Buff	er (Tr	)					1	8
Cell Symbol	Clock Input Bull	er (11	Prop	agation	Delav	Paramet	er		
		tı	up		td	n			
		t0	KCL	t0	KCL	KCL2	CDR2	2	Path
		1.09	0.01	1.49	0.01				X → CI
							l		
							l		
							l		
	_	İ			'				
х —	CI	,	'						
						İ			
		Parame	ter	L	L	<u> </u>	ymbo.	1	Typ(ns)*
							7		-35(7
		:							
						1			
	Input Loading								
Pin Name	Factor (lu)	1							
		<u> </u>				-			}
						1			
[	İ	İ							
	Output Driving	ł							
Pin Name	Factor (Lu)					į			
CI	Factor (lu)	1							
1		The	mum val	for the	the ty	rpical o	pera	tin ino	ng condition. condition
		are	given h	y the m	aximum	delay	nulti	pli	er.
l									
1									
1									
AU-ILB-E2	Chart 1/1								Page 20-10
I WO-ITR-F7	SHEET I/I								rage 20-10

FILITTEIL	CMOS GATE AR	DAY INITY	TELL COECT	FICATIO	N		"AU	Version
Cell Name	Function		Number of BC					
COLL HAME	Clock Input	Buffer	(True)					
ILBU	with Pull-u	n Resistan	TT ME)				- 1	8
Cell Symbol		v vestera	Pror	agation	Delay	Paramet	er	
Cell Symbol			tup	I	td	n aramet	-CT	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.0		1.49	0.01	RODZ	ODKZ	X → CI
		1	0.01	1.47	0.01			1 " "
			l l				İ	1
		1	1					
		i	l					
		- 1		1			İ	
		- 1	1	1				
		1		1			1	
х		.		Į.				
Α	C1	.	İ	1				1
		1	1	1				1
		ı	- 1	1			1	
		1	1	1	1		1	
		To		<u> </u>	L	L	rrmb = 1	+ Transcall
		rar	ameter			<del> `</del>	ymbol	Typ(ns)*
		1						
		1				- 1		
		1						
		1						
		1				- 1		
	T					- 1		1
	Input Load	ling						1
Pin Name	Factor (lu	1)						
		1				İ		
	Output Dr	lving						
Pin Name	Factor (lu	1)				1		
CI	200							
		1.						
		* M	inimum va	lues for	the ty	rpical o	operati	ng condition.
	i	Т	he values	for the	worst	case of	peratin	g condition
		a	re given	by the m	naximum	delay r	nultipl	ier.
1								
ļ								
ŀ								
1								
1								
l								
1								
AU-ILBU-E2	Sheet 1/1							Page 20-11
	1 1/1							1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function Clock Input Buff	er (Tr	ue)					Number of BC
ILBD	with Pull-down R	esistan	ce					8
Cell Symbol				agation			er	
		t0	up KCL	t0	td KCL	n KCL2	CDR2	Path
		1.09	0.01	1.49	0.01		222	Path X + CI
							l	
į								
ļ								
								'
х —	сі							
^								İ
		Parame	ter	L		l s	ymbol	Typ(ns)*
Ì						ŀ		
l						- 1		
ļ	T T T 17	ł						
Pin Name	Input Loading Factor (lu)							1
T III Made	Tactor (xu)	1						
		ļ						
	-	1						
	Output Driving	1						
Pin Name	Factor (lu)					Í		
CI	200	<b></b>						
1		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case of	erati	ing condition
		are	given b	y the m	axımum	deray n	uiti	olier.
				•				
AU-TLBD-E2	Sheet 1/1							Page 20-12

FUJITSU	CMOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		"A	U" Version
Cell Name	Function	000	<u> </u>	1 1011110	.,			Number of BC
					_	·		
I1C	CMOS Interface I	nput Bu	ffer (	Inverte	r)			5
Cell Symbol		ļ <u>.</u>		agation	Delay		er	
		t0	up KCL	t0	td KCL	n KCL2	CDR2	⊢ թ I
		0.65	0.03	0.29	0.03	KCLZ	CDRZ	Path X → IN
		0.05	0.03	0.25	0.03			1 1 1 1
	<u> </u>							
х	>> IN							
		Parame	ter	L	l	1	ymbol	Typ(ns)*
		Larame	CCT				, m.DO1	1JP(IIS)"
						ļ		
	<del></del>	Į						
<b>.</b>	Input Loading							
Pin Name	Factor (lu)	ļ						
		1						
		1						
	Output Driving	1						
Pin Name	Factor (lu)	]						
IN	36	L						
			m,,m1	f	+hc +	nical :		ina condition
	1	The	mum Val	ues IOT	tne ty	hical (	perat	ing condition. ng condition
		are	given h	v the m	aximum	delav m	nultin	lier.
		,	9 D	, 11			<u>-</u>	
ĺ								ļ
AU-I1C-E3	Sheet 1/1			_				Page 20-13

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			AU"	Version
Cell Name	Function							N	umber of BC
	CMOS Interface I			Inverte	r)			Г	
I1CU	with Pull-up Res								5
Cell Symbol			Prop	agation			er		
			up		td				
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.65	0.03	0.29	0.03		1		X → IN
							1		
							1		
,	_						1		
х	> IN								
ا									
							<u></u>		
		Parame	ter			S	ymbo	1	Typ(ns)*
1									
						1			
						- 1			
						1			
	Input Loading					1			
Pin Name	Factor (lu)								
1 III Hame	1 20001 (20)								
	1								
ļ									
						-			
	Output Driving								
Pin Name	Factor (lu)								
IN	36					l			
			_						
		" Mini	mum val	ues for	tne ty	pical c	pera	tin	g condition.
1		The	values	ior the	worst	case of	erat.	rus Tus	condition
	<u> </u>	are	given b	y the m	aximum	четау п	ultl	PII	er.
1									
1									
1									
1									
1									
1									
i									
1									
1									
	•								
1									
AU-I1CU-E3	Sheet 1/1								Page 20-14

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	
	Function							Number of BC
	CMOS Interface I			Inverte	r)		ļ	-
I1CD Cell Symbol	with Pull-down R	esistan	Prop	agation	Delay	Paramet	er	5
ocii bymboi		tı	up	agation	td		<u> </u>	- 1
		t0	KCL	t0	KCL	KCL2	CDR2	Path X → IN
		0.65	0.03	0.29	0.03			X → IN
1								
x	→ IN							1
•							ļ	
								1
						į		
		Parame	ter			S	ymbo1	Typ(ns)*
								1
	Input Loading							1
Pin Name	Factor (lu)							
	i e							
	Output Driving							
Pin Name IN	Factor (lu)							
111	] 30							
		* Mini	mum val	ues for	the ty	pical c	perat:	ing condition.
		The	values	for the	worst	case or	erati	ng condition
<u> </u>	<u> </u>	are	given b	y the m	aximum	delay m	ultip.	lier.
1								
ĺ								
1								
AU-I1CD-E3	Sheet 1/1							Page 20-15

	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION								n
Cell Name	Function							Number of	
T20	CMOC T-+	D	<i>EE</i> /m	N				,	
I2C Cell Symbol	CMOS Interface I	nput Bu	Pron	rue)	Delay	Paramet	er	4	
CCII Dymbol		t	up ITOP	-8a c 1 O II	td			T	
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
!		0.74	0.03	1.07	0.03			Path X → I	N
							ļ	ļ	
								i	
	_							]	
х	IN								
								ĺ	
						i			
		Parame	ter			S	ymbol	Typ(ns	)*
						1			
								-	
n	Input Loading								
Pin Name	Factor (lu)							}	
								1	
	1011								
Pin Name	Output Driving Factor (lu)							1	
IN	36								
		* Mini	mum val	ues for	the ty	pical c	perat	ing condit	ion.
		The	values	for the	worst	case or	erati	ng conditi	.on
	1	l are	given b	y the m	axımum	deray n	uuıtır	olier.	
1									
}									
1									
AU-I2C-E2	Sheet 1/1							Page 20	)-16

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
T00"	CMOS Interface I	nput Bu	ffer					
I2CU Cell Symbol	with Pull-up Res	istance	(True)	agation	Delaw	Parame+	er	4
Serr Symbor		t.ı	up up	agacion	td	n n		T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.74	0.03	1.07	0.03			X → IN
							1	
							l	
		}						
							i	
х —	IN							
<b></b>	<u></u>						1	
							l	
		لـــــا		L		L		
		Parame	ter			—   S	ymbol	Typ(ns)*
						J		
n	Input Loading							
Pin Name	Factor (lu)							
						Ì		
	Output Driving					- 1		
Pin Name	Factor (lu)							
IN	36							
		* Mini	mum val	ues for	the tw	nical o	nerat	ing condition.
	1	The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
AU-I2CU-E2	Sheet 1/1							Page 20-17

FUJITSU C	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU"								
Cell Name	Function							AU" Version Number of BC	
	CMOS Interface I	nput Bu	ffer						
	with Pull-down R	esistan	ce (Tru	e)				4	
Cell Symbol				agation	Delay		er		
			up		td		GDE :		
		t0	KCL	t0	KCL	KCL2	CDR2		
		0.74	0.03	1.07	0.03			X → IN	
							}		
							1		
							-		
							İ		
							1		
							1		
ا ن	711								
х —	IN							1	
							1		
							1	1	
							]		
		Parame	ter	L	L	ء ا	ymbo]	l Typ(ns)*	
		1 GI AIII C					. <u>,</u>		
<b>!</b>						1			
						1			
						1			
						İ		1	
	Input Loading					l			
Pin Name	Factor (lu)					į			
						ļ			
						1			
ļ						1			
	Output Driving					ļ			
Pin Name	Factor (lu)								
IN	36								
		1							
		* Mini	mum val	ues for	the ty	pical o	opera	ting condition	
	}	The	values	for the	worst	case of	perat:	ing condition	
		are	given b	y the m	naximum	delay r	nulti	plier.	
l									
İ									
1									
1									
AU-T2CD-F2	Shoot 1/1							Page 20-18	

FILTER	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version									
Cell Name	Function	NII CEL	L SPECI	FICATIO	N		AC	Number of BC		
CCII Hame	Schmitt Trigger	Input R	uffer	<del></del>				TIGHIDET OF DO		
IIS	(CMOS Type, Inve	rter)					- 1	8		
Cell Symbol			Prop	agation	Delay	Paramet	er			
			up		td	n				
		t0	KCL	t0	KCL	KCL2	CDR2	Path		
		3.12	0.13	2.15	0.07			X → IN		
1							ļ			
							}	1 1		
								i		
ļ										
	_							1		
x	√√ IN									
	- III									
Ì								1		
				'						
[										
		Parame	ter			. 8	ymbol	Typ(ns)*		
1										
								1		
1								1		
1								1		
<u> </u>	Input Loading									
Pin Name	Factor (lu)									
	120002 (20)							1		
								1		
h	Output Driving					1				
Pin Name IN	Factor (lu)									
111	10									
1		* Mini	mum val	ues for	the tv	pical c	perati	ing condition.		
	1	The	values	for the	worst	case or	eratir	ng condition		
		are	given b	y the m	naximum	delay n	ultipl	ier.		
}										
1								1		
1										
1										
1								1		
1										
Į.										
1										
1										
AU-I1S-E2	Sheet 1/1							Page 20-19		

FUJITSU C	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU"								
Cell Name	Function .								Version umber of BC
	Schmitt Trigger	Input B	uffer						
IISU	(CMOS Type, Inve	rter) w	ith Pul	1-up Re	sistanc	e ·		L	8
Cell Symbol				agation			eter		
			up		td		0 1 055		<b>.</b>
		t0	KCL	t0	KCL	KCL:	2 CDR	2	Path X → IN
		3.12	0.13	2.15	0.07		İ		X → 1N
							1		
							- 1		
							1		
х —	√√ IN								
^ _	J) VIII						1		
							1		
							1		r
Parameter Symbol								1	Typ(ns)*
					+			-55 (115)	
						1			
						1			
						1			
	Input Loading								
Pin Name	Factor (lu)								
						İ			
						1			
						ì			
						1			
	Output Driving								
Pin Name	Factor (lu)					l			
IN	18								
		* Mini	mum val	ues for	the ty	pical	opera	tin	g condition.
		The	values	for the	worst	case	operat	ing	condition
	<u> L</u>	are	given b	y the m	aximum	delay	multi	pli	er.
1									
1									
1									
1									
1									
I									
1									
1									
AU-I1SU-E2	Sheet 1/1								Page 20-20

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	
Cell Name	Function Schmitt Trigger	Input R	uffor					Number of BC
IISD	(CMOS Type, Inve	rter) w	ith Pul	l-down l	Resista	nce		8
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.12	0.13	2.15	0.07			X → IN
								1
х —	ır>>>— in							
								}
								1
		Parame	ter			S	ymbol	Typ(ns)*
						1		
	:							,
	Input Loading							
Pin Name	Factor (lu)							
						1		
	Output Driving					i		
Pin Name	Factor (lu)					1		
IN	18							
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		ine	values	for the y the m	WOIST	case op	eratin	g condition
		are	PTAGII D	J CITE III	CATION!	uciay II	GI CIPI	
AU-I1SD-E2	Sheet 1/1							Page 20-21

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU								U" Version Number of BC		
Cell Name	Function									
	Schmitt Trigger	Input B	uffer							
I2S	(CMOS Type, True	) -						- 8		
Cell Symbol			Prop	agation	Delay	Parame	ter			
		t	up		td					
		t0	KCL	t0	KCL	KCL2	CDR2	Path		
		1.99	0.13	2.47	0.08			Path X → IN		
		1.,,	0.15	2.77	0.00					
l							1			
ļ										
۱ ،	_					1	1			
x —	IN │									
						i				
							1			
		D		L	L	<b>I</b>	<u> </u>	T ( )-E		
		Parame	ter				Symbol	Typ(ns)*		
								]		
]						}				
ĺ										
ł						1				
						1				
	Input Loading							ļ		
Pin Name	Factor (lu)									
	140001 (24)									
ļ										
ŀ						1				
1										
								1		
1	Output Driving					- 1		}		
Pin Name	Factor (lu)									
IN	18					- 1				
		* Mini	mum val	ues for	the tv	roical	operat	ing condition.		
		The	values	for the	worst	Case (	nerati	ng condition		
		270	given b	or the m	avimum	dalaw	multin	lior		
	L.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	are	given b	y che ii	Idaliiuiii	delay	marcip	1161.		
Ļ										
1										
1										
1										
1										
1										
1										
1										
AU-I2S-E2   S	Shoot 1/1							Page 20-22		
1 NO 140 E4   3	コルモモレ エノエ !							I FARE ZUTZZ		

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		JA"	J" Version
Cell Name	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I2SU	(CMOS Type, True	) with :	Pull-up	Resist	ance			8
Cell Symbol				agation	Delay		er	
	İ		up		td		appe	<b>-</b>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
	İ	1.99	0.13	2.47	0.08			
								1
X .	IN							
, <u> </u>	~							
		Parame	ter			S	ymbol	Typ(ns)*
						1		
						1		
	I T							
D4 N	Input Loading							
Pin Name	Factor (lu)							
								}
	Output Driving							
Pin Name	Factor (lu)							
IN	18							
				_				
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati:	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
	•							
1								
AU-I2SU-E2	Sheet 1/1							Page 20-23

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I2SD	(CMOS Type, True	) with	Pull-do	wn Resi	stance			8
Cell Symbol				agation			er	
			up		td		anna	┦ , .
		t0	KCL	t0	KCL	KCL2	CDR2	Path X → IN
		1.99	0.13	2.47	0.08			X → IN
	,						l	
							1	
							ļ	
							İ	
х —	IN							
							Ì	
					1		<b>!</b>	ļ.
							1	ı
				L	L	L	<u></u>	
		Parame	ter			S	ymbol	Typ(ns)*
	•					ļ		
	Input Loading							
Pin Name	Factor (lu)					i		
								İ
								ļ
<b>.</b>	Output Driving							1
Pin Name	Factor (lu)							
IN	18	<b></b>						
		* Mini	mum 1721	nos for	the to	mical c	nerat	ing condition.
		The	walnes	for the	worst	case or	perati	ng condition
		are	given b	y the m	naximum	delay m	ultip	lier.
	<u> </u>		<u></u>				<u>-</u> -	
1								
1								
1								
1								
1								
1								
All-12SD-F2	Sheet 1/1							Page 20-24

FUJITSU (	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version								
Cell Name	Function							Number of BC	
I1R	Schmitt Trigger (TTL Type, Inver	Input B	uffer					g.	
Cell Symbol	(III Type, Inver	terj	Prop	agation	Delav	Paramet	er l	8	
······································		t	up		td	n			
		t0	KCL	t0	KCL	KCL2	CDR2	Path X → IN	
		3.59	0.13	1.89	0.07			X → IN	
	C 2								
х —	IN IN								
								1	
		Parame	ter			S	ymbol	Typ(ns)*	
						ļ			
						-			
Din Nama	Input Loading Factor (lu)								
Pin Name	ractor (ku)								
						1			
	1								
	Outros Delevino								
Pin Name	Output Driving Factor (lu)					ļ			
IN	18					- 1			
		* Mini	mum val	ues for	the ty	pical o	perat.	ing condition.	
		The	values	for the y the m	worst	case op	erati	ng condition	
	<u> </u>	are	given b	y the m	axillidili	delay iii	штетр	iiei.	
								}	
AU-I1R-E2 S	Sheet 1/1							Page 20-25	

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "A									Version
Cell Name	Function							N	umber of BC
	Schmitt Trigger	Input B	uffer					T	
I1RU	(TTL Type, Inver	ter) wi	th Pull	-up Res	istance				8
Cell Symbol			Prop	agation	Delay	Parame	ter		
			up		td	n			
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		3.59	0.13	1.89	0.07				X → IN
							1		
							1		
							1		
х	IJ>>>─ IN								
						1	1		
1									
1						<u> </u>	1		
		Parame	ter				Symbo	1	Typ(ns)*
	Input Loading					1			
Pin Name	Factor (lu)								
						1			
{									
						Ì			)
						1			
	Output Driving								
Pin Name	Factor (lu)								
IN	18								<u> </u>
		* Mini	mum val	ues for	the ty	pical	opera	tin	g condition.
		The	values	for the	worst	case o	perat	ing	condition
	1	are	given b	y the m	aximum	delay	multi	pli	er.
1									
]									
]									
1									
1									
1									
[									
1									
ļ									
1									
1									
1									
1									
1									
1									
							0		
AU-I1RU-E2	Sheet 1/1								Page 20-26

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"Al	J" Version
Cell Name	Function		5 01 1101	1 1011110	••			Number of BC
	Schmitt Trigger	Input B	uffer					
I1RD	(TTL Type, Inver	ter) wi	th Pull	-down R	esistan	ce		8
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0	KCL	tO ·	KCL	KCL2	CDR2	Path X → IN
		3.59	0.13	1.89	0.07		ļ	$X \rightarrow IN$
							1	
							ľ	
							[	
							İ	
v	711			ľ			l	
х —	IN							
ĺ	•							
		Parame	ter			S	ymbol	Typ(ns)*
							<i>y</i>	- JF(112)
						1		
	Input Loading							
Pin Name	Factor (lu)							
		i i						
						[		1
	1							
n	Output Driving					ŀ		
Pin Name IN	Factor (lu)	}						
IN	18							
		& Mini	mum 1	was for	+ho +v	nical c		ing condition.
ĺ		The	mum vai	for the	worst	pical c	operat.	ng condition.
		are	varues viven h	y the m	avimum	delay m	ultin	lier
	<u> </u>	arc	given i	y the in	CATIOUI.	ucray n	dicip	1101.
1								
l								
1								
1								
I								
AU-I1RD-E2	Sheet 1/1							Page 20-27

FUJITSU	CMOS GATE ARRAY U	NIT CEL	Version					
Cell Name	Function						1	Number of BC
	Schmitt Trigger		uffer	1				
I2R	(TTL Type, True)							8
Cell Symbol			Prop	agation			er	<del>,                                     </del>
		t t	up	+6	td		CDDO	, n
		t0	KCL	t0	KCL	KCL2	CDR2	Path X → IN
		1.79	0.13	2.98	0.11			X → IN
							1	1
								1
							1	1
								1
	j							1
	_						1	1
х —	IN I							
·							1	}
							1	
			<u> </u>		L		<u></u>	m ( )
		Parame	ter				ymbol	Typ(ns)*
						ł		
						-		
						Ì		
	Input Loading					-		
Pin Name	Factor (lu)							
						}		
						1		
	1							
D2- N	Output Driving					-		
Pin Name IN	Factor (lu)							
I	10	<b></b>						1
		* Mini	mum val	ues for	the to	pical d	perati	ng condition.
		The	values	for the	worst	case or	erating	g condition
		are	given b	y the m	aximum	delay r	nultipl	ler.
	<del></del>							
1								
1								
1								
1								
1								
1								
AU-I2R-E2	Choo+ 1/1							Page 20-28
1 40-174-57	DREET I/II							T FAVE /UT/O

FUJITSU (	CMOS GATE ARRAY U	"A	U" Version					
Cell Name	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I 2RU	(TTL Type, True)	with P	ull-up	Resista	nce			8
Cell Symbol			Prop	agation	Delay		er	
			up		td		L arn-	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.79	0.13	2.98	0.11		ĺ	X → IN
		}						
v	CT TV	ĺ					l	
х	IN IN							
·							1	
		Parame	ter	L		1 9	ymbol	Typ(ns)*
		. a. ame					,	1,7,0(113)
						1		
	Input Loading							
Pin Name	Factor (lu)							
								1
	Output Driving							
Pin Name	Factor (lu)					- 1		
IN	18							
				_				
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
	1	are	given b	y the m	aximum	delay n	nultip	lier.
1								
1								
AU-I2RU-E2	Sheet 1/1							Page 20-29

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		" <i>E</i>	AU"	Version
Cell Name	Function							Nı	umber of BC
	Schmitt Trigger	Input B	uffer						
I2RD	(TTL Type, True)	with P	ull-dow	n Resis	tance				8
Cell Symbol			Prop	agation	Delay		er		
			up		td	n		[	
		t0	KCL	t0	KCL	KCL2	CDR2	2	Path X → IN
		1.79	0.13	2.98	0.11		l	1	$X \rightarrow IN$
								ŀ	
							}	1	
							1	1	
							ļ		
								- 1	
							1	- 1	
v	7.,						1	- 1	
х —	IN IN							- 1	
}							ŀ	- 1	
							1	- 1	
								- 1	
		Parame	ter		I	<u> </u>	ymbo]	-	Typ(ns)*
		Tarame	rer			<del></del>	'y moo	-	135(112)
						ľ			
						l			
1	,								
1									
	Input Loading							- 1	
Pin Name	Factor (lu)					- 1		- 1	
	155555							l	
								-	
						1		İ	
						1		- 1	
								- 1	
	Output Driving								
Pin Name	Factor (lu)								
IN	18							i	
		* Mini	mum val	ues for	the ty	pical o	perat	tin;	g condition.
		The	values	for the	worst	case or	erat:	ing	condition
		are	given b	y the m	aximum	delay n	ultip	<u>pli</u>	er.
1									
1									
1									
1									
1									
1									
1									
AU-I2RD-E2	Sheet 1/1							-	Page 20-30

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATION			JA"	J" Version
	Function							Number of BC
			_					
	Output Buffer (I	nverter			D. 1 D			3
Cell Symbol				agation	Delay P	aramete	Ι	<del></del>
		t0	up KCL	t0	KCL	KCL2	CDR	2 Path
		1.60	0.047	1.63	0.103	RODZ	ODICA	OT → X
		(4.42)	0.017	(7.81)				0
		` 1		` ′				
1	_							
от —	>> x						ł	1
•				1				
							1	1
							L	
		Parame	ter			Sy	mbol	Typ(ns)*
						1		
						ŀ		
	Input Loading					1		1
Pin Name	Factor (lu)							
OT	2							
						1		
								1
	Output Driving							
Pin Name	Factor (lu)							
			_	•				
								ing condition.
				for the y the ma				ng condition
	L	are	green p	y the ma	XIIIUM Q	eray mu	п.1р.	1161.

Note: 1. The unit of K<sub>CL</sub> is ns/pF.

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-01B-E1 | Sheet 1/1 | Page 20-31

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N			U" V	ersio	n
Cell Name	Function	000	<u> </u>	11011110					er of	
			·-,····							
O1L	Power Output Buf	fer (In							3	
Cell Symbol				agation			er			
		to	up KCL	t0	td KCL	KCL2	CDR2	$\dashv$	Path	
		2.00	0.032	2.13	0.034	ROBZ	ODINZ		$T \rightarrow X$	
		(3.92)		(4.17)			1			
							1			
							ł			
								1		
ОТ —	>>─ x									
							l			
							1			
		Parame	ter			\	ymbol	. 7	yp(ns	)*
ļ						į		-		
						1				
	Input Loading	1				1		Ì		
Pin Name	Factor (lu)					- 1		-		
OT	2					Ì				
								1		
	Output Driving	1						İ		
Pin Name	Factor (lu)					1		1		
		* Mini	miim 12a1	ues for	the tw	mical (	nerat	ino c	ondit	ion
				for the						
				y the m						
		, -								
Note: 1. The unit of K <sub>CL</sub> is ns/pF.										
2. 0	2. Output load capacitance of 60 pF is used for Fujitsu's									
	ogic simulation.		P.		·		-			
3. T	3. The parameters in parentheses are the values applied to the simulation.									

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION			"AU	
Cell Name	Function							Number of BC
	Output Buffer (I						İ	
O1R	with Noise Limit	Resist						5
Cell Symbol			Prop	agation			r	
			up		tdn			<u> </u>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.75	0.047	6.60	0.103		l	OT → X
		(6.57)		(12.78)				
					Ì		l	
			i	1			i	
	<u> </u>			1	1	ł	1	
				}	į	ł	l	
OT	× x			1		1		
ľ						ļ		
l						ŀ		
1					l	1		
		Parame	ter	L	L	Sv	mbol	Typ(ns)*
1		Tarame				1 5,	IIIDO I	135(113)
1		1						
1								
		l						į
	Input Loading	1						
Pin Name	Factor (lu)	ł						
OT	1	1						
1								
		1						
	Output Driving	1						
Pin Name	Factor (lu)							ļ
		1						1 .
1		* Mini	mum val	ues for	the typ	ical or	erati	ng condition.
		The	values	for the	worst c	ase ope	ratin	g condition
		are	given b	y the ma	ximum d	lelay mu	ltipl	ier.
Note: 1. T	The unit of $K_{ m CL}$ is	ns/pF.						
1								
	output load capaci	tance o	f 60 pF	'is used	for Fu	ijitsu's	;	
1	ogic simulation.							

3. The parameters in parentheses are the values applied to the simulation.

AU-01R-E1 | Sheet 1/1

FILITEII (	CMOS GATE ARRAY U	NIT CET	T CDECT	FICATION			"AU"	Version
Cell Name	Function	ATT CEP	L SPECT	FICALION				Number of BC
OCII Manie	Power Output Buf	fer (In	verter					tumber of BC
018	with Noise Limit							5
Cell Symbol			Prop	agation	Delay P	aramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		4.35	0.033	8.69	0.046			OT → X
		(6.33)		(11.45)				
	_				ŀ			
OT	, "							
OT	× x							
		Parame	ter	L		Sv	mbo1	Typ(ns)*
						ļ		
						1		
	Input Loading							
Pin Name	Factor (lu)							
OT	1							
	Output Driving							
Pin Name	Factor (lu)							
1 111 Name	1140001 (24)							
		<b></b>						
		* Mini	mum val	ues for	the tyr	oical or	erati	ng conditi <b>on</b> .
								g condition
				y the ma				
		•						

Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  is ns/pF.

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

DUTTELL	CMOC CATE ADDAY IT	NIT CEL	T CDECT	FICATION			l "Al	U" Version
Cell Name	CMOS GATE ARRAY U	NII CEL	L SPECI	FICALION			L A	Number of BC
CETT MAME	ruiction							MUNDET OF BC
02В	Output Buffer (T	rue)						3
Cell Symbol			Prop	agation	Delay P	aramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR	
		0.78	0.047	1.15	0.103			OT + X
		(3.60)		(7.33)			l	
					1		1	
							ł	
ł							)	
			ł					
	$\wedge$		1			}		
от	→ x		ĺ			1		į
					ĺ			
			İ					
			<u> </u>			<u> </u>	<u> </u>	
		Parame	ter			Sy	mbo1	Typ(ns)*
		1						
		İ				İ		
	Input Loading	1						
Pin Name	Factor (lu)	l				- 1		ì
OT	6					- 1		
						1		
l						1		
								1
	Output Driving	1				[		1
Pin Name	Factor (lu)					ļ		
Tak Numb	140001 (24)	1				j		i
		* Mini	mum val	ues for	the typ	oical or	erat	ing condition.
		The	values	for the	worst o	ase ope	erati	ng condition
		are	given h	y the ma	ximum c	lelay mu	ıltip	lier.
Note: 1. T	The unit of $\mathtt{K}_{\operatorname{CL}}$ is	ns/pF.						
	hitmit load ac		£ 60 -1	. da nesi	1 for P-		_	
	Output load capaci logic simulation.	LLANCE C	or on br	rs used	I TOT PU	เป็นกลา	•	
1 ,	rogic simularion.							

- 3. The parameters in parentheses are the values applied to the simulation.

AU-02B-E2 | Sheet 1/1 Page 20-35

FUJITSU ( Cell Name	CMOS GATE ARRAY U Function	NIT CELL SPECI	FICATIO	N		"A	U" Version Number of BC
O2L	Power Output Buf	for (True)					
Cell Symbol	rower output bur	Prop	agation			er	3
		tup t0 KCL	t0	td KCL	n KCL2	CDR2	Path
		0.89 0.032	1.26	0.034			OT + X
		(2.81)	(3.30)				
	$\sim$						
от —	> x						
		Parameter	L		S	ymbo1	Typ(ns)*
							į į
	Input Loading						
Pin Name OT	Factor (lu)				l		
01	•						
Pin Name	Output Driving Factor (lu)						
							ing condition.
	1	The values are given b					ng condition
Note: 1 T	he unit of Ver is						
	he unit of K <sub>CL</sub> is						
2. 0	utput load capaci ogic simulation.	tance of 60 pl	is use	d for F	ujitsu'	S	
1	he parameters in	naranthaeae a	a tha "	ra11166 a	nnlied	to +h	ne simulation
3. 1	" harameters III	beremeneses at			hhrred		SIMOISTIVII.
AU-02L-E2	Sheet 1/1						Page 20-36

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION			"AU	
Cell Name	Function							Number of BC
	Output Buffer (T						l	
O2R	with Noise Limit	Resist						4
Cell Symbol				agation			r	
			up		tdn			_
		t0	KCL	t0	KCL	KCL2	CDR2	
		3.68	0.047	6.07	0.103		}	OT → X
		(6.50)		(12.25)			l	
							1	
			:				İ	
							ì	
							}	-
			i				}	
							1	
OT -	x		ļ				1	-
							l	1
							l	
							l	
		Parame	ter			Sy	mbol	Typ(ns)*
						į		
						1		
						}		
	<del></del>							
l <u>.</u>	Input Loading							
Pin Name	Factor (lu)					- 1		
OT	2					l		
	1					- 1		į
	l							
						}		
	Outros Design							
D:	Output Driving							
Pin Name	Factor (lu)							
	1	<u> </u>						
		* W	1		41- 4	1		na sanditian
								ng condition.
								ng condition
	1	are	given b	y the ma	ximum d	eray mu	пттрі	161.

Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  is ns/pF.

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

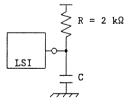
FILITSII	CMOS GATE ARRAY U	NIT CEL	I. SPECT	FICATION			"AU	" Version
Cell Name	Function	0011	- 0.101	TIONITON			1 7	Number of BC
JOIL Hame	Power Output Buf	fer (Tr	ne)		<del></del>			THE OF THE
02S	with Noise Limit							4
Cell Symbol		Vestar		agation	Delay D	aramoto	<u></u>	-
CELL DAMPOI		+	up	agacion	tdn			1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		4.40	0.033	8.48	0.046	TOT 2	CDKZ	Path OT → X
			0.033					01 7 A
		(6.38)		(11.24)			ĺ	
				ļ		}		
				ļ				
						ŀ		
				1	1		j	1
	_			ŀ	1	İ	}	
					1	1	1	
OT	x			1	1			
				1	1	1	1	
				ì				
				1				
		Parame	ter			Sy	mbol	Typ(ns)*
1								
1								
								}
}								1
	Input Loading							ł
Pin Name	Factor (lu)							
TO	2							•
						1		
						Ì		
								Ì
1								
	Output Driving							
Pin Name	Factor (lu)							
1 111 Name	ractor (ku)					-		
}		<b></b>						
		& W	1	£	+ha +	daal -		ina aanditis-
		" mini	mum val	ues for	the typ	orcal of	erat:	ing condition.
								ng condition
		are	given b	y the ma	ximum c	ielay mu	iltip.	ner.
] ,, ,	m :							
Note: 1. 7	The unit of $\mathtt{K}_{ extsf{CL}}$ is	ns/pF.						
	Output load capaci	tance o	of 60 pF	is used	i for Fu	ijitsu's	5	
] ]	logic simulation.							
1								
3. 7	The parameters in	parenth	ieses ar	e the va	ılues ap	plied t	to the	e simulation.
1								
1								
1								
1								
1								
1								
1								
1								

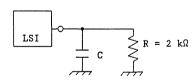
Page 20-38

AU-02S-E1 Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATION	١		"A	U"	Version	
Cell Name	Function							Nι	umber of	ВC
	Tri-state Output	Buffer	(True	)					1	
04R	with Noise Limit	Resist							5	
Cell Symbol			Pro	pagation	Delay P	aramete	r			
		t	up		tdn					
		t0	KCL	t0	KCL	KCL2	CDR	2	Path	_
		3.35	0.047		1			-	OT → X	
		(6.41)		(12.96)	)		ŀ	- 1		
				1						
1				į.						
OT	, v			i						
ОТ	х х									
i				ł						
	С			}						
	C									
			L →	7.	J	$Z \rightarrow L$		+		_
		t0	_ <u>_</u>	KCL	t0		CL	$\dashv$	$C \rightarrow X$	
		2.0	0		6.62		105			
		(13.5		*	(13.45	)				
					`	´				
						1				
	Input Loading									
Pin Name	Factor (lu)			į		1				
OT	2									
С	2 .		Н →			Z → H				
		t0		KCL	t0		CL			
		3.2	-		3.40		048	- 1		
	Output Driving	(13.5	7)	*	(13.45	)				
Pin Name	Factor (lu)									
								ŀ		
								ŀ		
	1	ı	1	i		1				

\* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and Zh are as follows:





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of  $K_{\rm CL}$  is ns/pF.

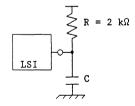
- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

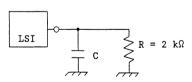
AU-04R-E1 | Sheet 1/1

FILLECTI	CMOS GATE ARRAY U	NIT CET	CDEC	TETCATION	.1		"Al	7 11	Version
Cell Name	Function	NII CEL	L SPEC	JIF ICALIO	<u> </u>		1 4		mber of BC
Cell Name	Power Tri-state	Output	Ruffor	(True)			+	110	mber or bc
048	with Noise Limit			(IIue)			- 1		5
Cell Symbol	WICH NOISE BINIE	- KCDIBC		pagation	Delay P	aramete	r		
5511 57551		t	up	Jugueton	tdn			Т	
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		4.06	0.033					十	OT + X
		(6.21)		(11.63)	)		÷		
		` ′		(				-	
				1			l		
				i					
				- [				١	
OT	x			-					
	M							- 1	
				ł			ļ	1	
	-			İ					
	С			ı					
					<u> </u>	7	<u> </u>	+	
			L →			$Z \rightarrow L$	CL	4	C . V
		t0 3.5	<del>.  </del>	KCL	t0 8.36		046	$\dashv$	$C \rightarrow X$
		(16.8		*	(11.35		040		
		(10.0	0)		(11.33	'			
			1	İ					
	Input Loading		- 1	1					
Pin Name	Factor (lu)		1					- 1	
OT	2	1	1	1					
С	2		Η →	Z		$Z \rightarrow H$		$\neg$	
1		t0		KCL	t0		CL		
		4.0			4.30	4	033		
	Output Driving	(16.8	0)	*	(11.35	)			
Pin Name	Factor (lu)		1			- 1			
			- 1						
			1					- 1	
	1		- 1	1		- 1		- 1	

\* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



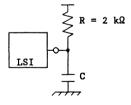


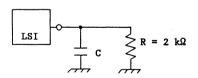
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at  ${\tt HZ}$  and  ${\tt ZH}$ .
- Note: 1. The unit of  $K_{\rm CL}$  is ns/pF.
  - Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-04S-E1 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPEC	CIFICATION	N		"A		Version
Cell Name	Function							Νι	umber of BC
04T	Tri-state Output	Buffer	(True	:)					6
Cell Symbol				pagation			r		
			up	+	tdn		CDD	ᅱ	D
		t0 1.08	KCL 0.047	t0	KCL 0.103	KCL2	CDR	4	Path OT → X
		(4.14)		(8.65)				١	01 7 X
		(4.14)		(0.05)	Ί Ι			ı	
				1				- 1	
•								- 1	
								- 1	
от —	<b>x</b>						1	- 1	
							1	١	
	С						l	l	
			L →			$Z \rightarrow L$		_	
		t0	_	KCL	t0 2.44		CL 105		$C \rightarrow X$
		1.8 (13.8		*	(9.27	1	103	- 1	
		(13.0	"		().2/	'			
			- 1						
	Input Loading		ļ					ı	
Pin Name	Factor (lu)		į					- 1	
OT C	6 2		<u>H</u> →	7		$Z \rightarrow H$		$\dashv$	
· ·		t0		KCL	t0		CL	$\dashv$	
		3.7	7		1.23		048	$\dashv$	
	Output Driving	(13.8	9)	*	(9.27	)		- 1	
Pin Name	Factor (lu)	l	- 1						
			- 1					-	
			- 1						
		<b>!</b>				- }			

\* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:





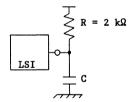
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

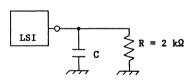
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-04T-E2 | Sheet 1/1

FILLTEIL C	CMOS GATE ARRAY U	NIT CET	CDEC	TETCATTO	NT		I WA	U" Version
	Function	NII CEL	L SPEC	IFICATIO	<u> </u>		^A	Number of BC
Cell Name	runction							Number of BC
	Power Tri-state	Output	Buffer	(True)				6
Cell Symbol				pagation			er	
	;		up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.49	0.032		0.036			OT → X
		(3.57)		(4.68)			l	
							1	1
							1	1
1	_		l			1	l	
		ł		1			l	
от —	x						i	
l	7	}						1
		<u> </u>	}			ł		
1	C		ł			l	1	
	C		l					
	•		L →	1 7		$Z \rightarrow I$		
		t0	<del></del>	KCL	t0		KCL	$ c \rightarrow x$
		2.6	2	KOD	2.5		0.036	- "
		(15.8		*	(4.8			ļ
		(13.0	,		. (***	"		
}			l					
	Input Loading	1	- 1					1
Pin Name	Factor (lu)							
OT	6	1			l			
С	2		H →	Z		$Z \rightarrow I$	H	
		t0		KCL	tO		KCL	
	<u> </u>	4.4			1.4		0.033	
	Output Driving	(15.8	30)	*	(4.8	37)		
Pin Name	Factor (lu)	j			1			
								Ī
		1	1					
	1	1						





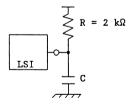
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

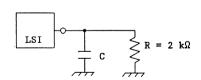
Note: 1. The unit of KCL is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-04W-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPE	CIFICATIO	ON			"A1	Ū"	Versio	on.
Cell Name	Function								Nu	mber of	
н6Т	Tri-state Output	& Inpu								10	
Cell Symbol			Pro	opagatio			mete:	r			
			up			dn			$\Box$		
		t0	KCL		KCL		CL2	CDR	2	Path	
		0.85	0.03						- 1	$X \rightarrow I$	
		1.08	0.04			3			- 1	OT → X	ζ
	1	(5.08)		(10.7	1)				- 1		
IN	<b>-</b> < h			ł							
	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \					-			- 1		
om				1					- 1		
OT	x .			ł					- 1		
				ł	1				- 1		
				ł					- [		
				Į.	1						
	С			ŧ		İ			- 1		
			L →		<del>,</del>		→ L		-		
		t0	_ <u> </u>	KCL		0		CL	$\dashv$	C →	х
		1.8	_	KCL		44		105	$\dashv$	U 7	Λ
		(17.0		ric	(11.		١ ٠.	103	- 1		
		(17.0	١ (٥		(11.	37)					
			- 1		İ						
	Input Loading		- 1		1		ĺ				
Pin Name	Factor (lu)										
OT	6		ı								
C	2		H →	7.	<del> </del>	7.	→ H		ᅱ		
-	_	t0	<del></del>	KCL	† †	0		CL	ᅥ		
		3.7	7			23		048	$\neg$		
	Output Driving	(17.0		*	(11.		'				
Pin Name	Factor (lu)	,=	1		`==.						
IN	36						1				
			- 1								
					1						
			1		1		1		- 1		

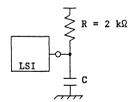


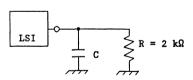


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6T-E3 | Sheet 1/1

FUITSU	CMOS GATE ARRAY U	NIT CEL	I. SPEC	IFICATIO	N		"AU	ŢĦ.	Vers	ion
	Function	011	D DI DO	11 1011110					mber	
0011	Tri-state Output	& Inpu	t Buffe	er (True	<u> </u>		+			01 20
H6TU	with Pull-up Res			. (	,		- 1		10	
Cell Symbol				pagation	Delay P	aramete	r			
		t	up	1	tdn		=	$\neg$		
		t0	KCL	t0	KCL	KCL2	CDR2	7	Pat	h
		0.85	0.03	1.47				7		IN
		1.08	0.047	1.95					OT →	X
	_	(5.08)		(10.71			l	ı		
in ——	_/_	`		1	1		İ			
IN							ł	ı		
							1			
от —	> x				1					
	Y		ł					- [		
		'					1	1		
	1						l	1		
	C		[				l	- [		
								$\perp$		
			L → :			$Z \rightarrow L$				
		t0		KCL	t0		CL		C →	X
		1.8			2.44		105	-		
		(17.0	0)	n't	(11.37	)				
			- 1							
	Input Loading									
Pin Name	Factor (lu)									
OT	6					L		_		
C	2		Η → .			$Z \rightarrow H$		4		
	į	t0		KCL	t0		CL	4		
<u></u>	ļ	3.7			1.23		048			
Dia Nam	Output Driving	(17.0	(0)	*	(11.37	,				
Pin Name	Factor (lu)					- 1				
IN	36		1			1				
	1		l					1		
ı		ı	ŀ		l	- 1		1		

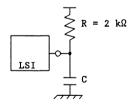


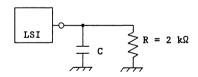


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6TU-E3 | Sheet 1/1

CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	I		"AU	J" Version
Function							Number of BC
Tri-state Output	& Inpu	t Buffe	r (True)				
			` ′				10
		Prop	agation	Delay Pa	aramete	r	
	t	up	1	tdn			
	t0	KCL	t0	KCL	KCL2	CDR	Path
	0.85	0.03	1.47	0.03			X → IN
	1.08	0.047	1.95	0.103			OT → X
	(5.08)		(10.71)	1			i
				i i			
$\backslash$			1	1			i
<b>X</b>							
ΓÝ							
							1
1				1			
C							
				l			
			KCL				C → X
		-	Ī			105	1
	(17.0	0)	*	(11.37	)		
			ļ.				
					ł		
_							
2							
			KCL				_
			. 1			048	l l
	[ (17.0	0)	37	(11.37	)		
36	ı	- 1	- 1		ı		I
1 30	1		l		i		l
	Function Tri-state Output with Pull-down R  C  Input Loading Factor (lu)  6 2  Output Driving Factor (lu)	Function Tri-state Output & Inpu with Pull-down Resistan  t t0 0.85 1.08 (5.08)  t0 1.8 (17.0  Input Loading Factor (£u) 6 2 t0 3.7 Output Driving Factor (£u) Factor (£u)	Function  Tri-state Output & Input Buffe with Pull-down Resistance  Prop  tup  t0 KCL  0.85 0.03 1.08 0.047 (5.08)   L + 2  t0  1.86 (17.00)  Input Loading Factor (&\ellu)  6 2 H + 2  t0  3.77 Output Driving Factor (&\ellu)  Factor (&\ellu)  Factor (&\ellu)  Factor (&\ellu)	Function  Tri-state Output & Input Buffer (True) with Pull-down Resistance  Propagation  tup t0 KCL t0 0.85 0.03 1.47 1.08 0.047 1.95 (5.08) (10.71)   X  C  L + Z t0 KCL 1.86 (17.00) *  Input Loading Factor (Lu) 6 2 H + Z t0 KCL 3.77 Output Driving Factor (Lu)  Factor (Lu)  Output Driving Factor (Lu)  Factor (Lu)  A True  Resistance  Propagation  **  **CL 1.86 (17.00) *  **  **CL 3.77 (17.00) *  **  **CL 3.77 Output Driving Factor (Lu)  **  **CL 3.77 Output Driving Factor (Lu)  **  **CL 3.77 Output Driving Factor (Lu)  **  **CL 3.77 Output Driving Factor (Lu)  **  **  **CL 3.77 Output Driving Factor (Lu)  **  **  **  **  **  **  **  **  **	Tri-state Output & Input Buffer (True) with Pull-down Resistance  Propagation Delay P.  tup tdn to KCL t0 KCL 0.85 0.03 1.47 0.03 1.08 0.047 1.95 0.103 (5.08) (10.71)   L + Z t0 KCL t0 1.86 2.44 (17.00) * (11.37  Input Loading Factor (lu) 6 2 H + Z t0 KCL t0 3.77 1.23 Output Driving Factor (lu) Factor (lu)  Output Driving Factor (lu) (17.00) * (11.37	Function  Tri-state Output & Input Buffer (True) with Pull-down Resistance  Propagation Delay Paramete  tup tdn  t0 KCL t0 KCL KCL2  0.85 0.03 1.47 0.03 1.08 0.047 1.95 0.103 (5.08) (10.71)  L + Z Z + L  t0 KCL t0 KCL  1.86 (17.00) * (11.37)  Input Loading Factor (lu)  6 2 H + Z Z + H  t0 KCL t0 KCL  1.37 0.00  Input Loading Factor (lu)  6 2 H + Z Z + H  t0 KCL t0 KCL  1.23 0.  Output Driving Factor (lu)  Output Driving Factor (lu)  Factor (lu)  Very contact to KCL  1.23 0.	Function  Tri-state Output & Input Buffer (True) with Pull-down Resistance  Propagation Delay Parameter tdn tup t tdn to KCL KCL2 CDR:  0.85 0.03 1.47 0.03 1.08 0.047 1.95 0.103 (5.08) (10.71)  X  C  L + Z

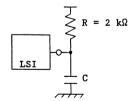


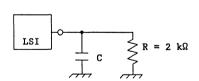


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6TD-E3 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U" Version
Cell Name	Function							Number of BC
H6W	Power Tri-state	Output	& Input	Buffer	(True)			10
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	The second secon
1		0.85	0.03	1.47			1	X → IN
		1.49	0.032	2.34	0.036		l	OT → X
	1	(4.21)		(5.40)			l	
IN	<b>-</b> < h						ł	
	N 71						1	
от	x —							
"							l	ŀ
l							1	į
l	İ						Ì	
	С						j	
			L → 2			Z → I		
1		t0		KCL	t0		KCL	c → x
		2.6			2.5		0.036	
		(19.8	0)	*	(5.5	9)		
	Input Loading	1						
Pin Name	Factor (lu)							
OT	6	ì				ì		1
C	2		H → 2	?.		$Z \rightarrow I$	Ŧ	-
		t0		KCL	t0		KCL	
		4.4	7		1.4	4 (	0.033	
	Output Driving	(19.8	0)	*	(5.5	9)		
Pin Name	Factor (lu)					İ		
IN	36					- 1		
			İ					
		L			l			

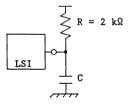


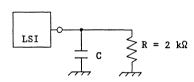


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6W-E3 Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N		"AU	J" Version
Cell Name	Function							Number of BC
	Power Tri-state	Output	& Inpu	t Buffer	(True)			
H6WU	with Pull-up Res	istance						10
Cell Symbol			Pro	pagation	Delay	Paramet	er	
		t	up	1	td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.85	0.03	1.47	0.03			X → IN
		1.49	0.032	2.34	0.036		Į.	OT → X
		(4.21)	į	(5.40)			1	İ
IN							1	
III	. 🔰							1
							1	
от —	<b>X</b>		1	1			1	
	M		1	1			1	
		}	l			ł	ì	
	1		İ			l	<u> </u>	
	C		ĺ	1			į .	
			1	1				
			L →			Z → I		
		t0		KCL	t0		KCL	_ c → x
		2.6			2.5		0.036	
		(19.8	0)	n'r	(5.5	9)		
			ł					
						Ì		
	Input Loading	Ì	-					
Pin Name	Factor (lu)		1			- 1		
OT	6							
С	2		Η →			Z → 1		
		t0		KCL	t0		KCL	
		4.4			1.4		0.033	
	Output Driving	(19.8	(0)	*	(5.5	9)		1
Pin Name	Factor (lu)	]				- 1		1
IN	36					ł		ı
	j	]						
		l	- 1			1		

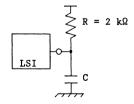


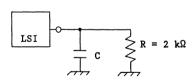


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the  ${\tt simulation}.$

AU-H6WU-E3 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"Al		ersion
Cell Name	Function							Numb	er of BC
	Power Tri-state	Output	& Input	Buffer	(True)				
H6WD	with Pull-down R	esistan							10
Cell Symbol			Prop	agation	Delay	Paramet	er		
		t	up		td				
		t0	KCL	t0	KCL	KCL2	CDR2		Path
		0.85	0.03	1.47	0.03				X → IN
		1.49	0.032	2.34	0.036		l	0	$T \rightarrow X$
	_	(4.21)		(5.40)				1	
IN			1					Ì	
III	$\sim$		1					1	
							1	1	
ОТ ——	x							1	
	V							- {	
			ĺ				l	ļ	
	1						l	į	
	С							ļ	
			$L \rightarrow 2$			Z → I			
		t0		KCL	t0		KCL		C → X
		2.6	- 1		2.5		.036	1	
		(19.8	0)	*	(5.5	9)		-	
			1			- 1			
								ı	
	Input Loading		l			1		-	
Pin Name	Factor (lu)		1			}			
OT	6							_	
С	2		H → 2			$Z \rightarrow I$			
		t0		KCL	t0		KCL	_	
	<u> </u>	4.4		_	1.4		0.033	- 1	
	Output Driving	(19.8	(0)	o'c	(5.5	9)		-	
Pin Name	Factor (lu)							1	
IN	36	1				i		1	
		ĺ			1	1		1	
						1			
		İ							

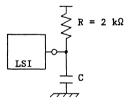


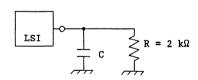


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6WD-E3 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	N		JA"	J" Version
Cell Name	Function							Number of BC
н6С	Tri-state Output	& CMOS	Interf	ace Inp	ut Buffer	(True	)	10
Cell Symbol			Prop	agation	Delay Pa	ramete	r	
			up		tdn		<b>,</b>	
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.74	0.03	1.07			1	X → IN
		1.08	0.047	1.95	0.103			OT → X
	1	(5.08)		(10.71)	)		1	
IN	<b>-</b> < h							
	N 71							ì
от	x							
01	^ ^			l	1 1		1	1
	ļ			l			1	
	С	1			1 1			}
					1 1		ļ	
			$L \rightarrow Z$			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		1.8			2.44		.105	
		(17.0	0)	*	(11.37)	1		
						-		
				i				
	Input Loading							
Pin Name	Factor (lu)	ł						
OT C	6 2	ļ	H → 2	,		$Z \rightarrow H$		
C	2	to	n 7 /	KCL	t0		CL	$\dashv$
		3.7	7	KCD	1.23		048	
	Output Driving	(17.0		*	(11.37)		J +U	}
Pin Name	Factor (lu)	\=			()			
IN	36	j				-		
								-
		1						
						- 1		1





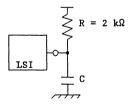
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

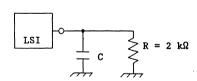
Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H6C-E3 | Sheet 1/1

FILITSII	CMOS GATE ARRAY U	NIT CEL	T. SPEC	TETCATIO	N		l "AU	" Version
Cell Name	Function	000	D DI DO	11 10/1110				Number of BC
0011 (10111)	Tri-state Output	& CMOS	Inter	face Inp	ut Buffe	r (True		THE STATE OF DO
H6CU	with Pull-up Res			-uoop		_ (	1	10
Cell Symbol				pagation	Delay P	aramete	r	
		t	up	T	tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.74	0.03	1.07	0.03			X → IN
		1.08	0.047				1	OT → X
	1	(5.08)		(10.71	)		1	
IN	<b>─</b>			İ			1	
	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \			1			1	
om							1	
OT -	x						i	İ
				İ				
	С						1	
							į	1
			L →	7.		$Z \rightarrow L$	<b></b>	
		t0	<del></del>	KCL	t0		CL	$\neg c \rightarrow x$
		1.8	6		2.44		.105	
		(17.0	0)	*	(11.37	)		ļ
		'	1					
	Input Loading							
Pin Name	Factor (lu)	!	- 1					
OT	6							
С	2		Η →			$Z \rightarrow H$		_
		t0		KCL	t0		CL	_
	10.4 1 B / /	3.7		*	1.23		048	
Din Nome	Output Driving Factor (lu)	(17.0	ا رن	^	(11.37	,		
Pin Name IN	36	ł	1					
11	30							
ĺ			1					
ļ								





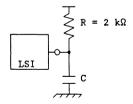
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

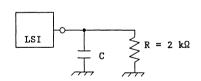
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H6CU-E3 | Sheet 1/1

FILLTEIL	CMOS GATE ARRAY U	NITE CEL	T CDEC	TETCATIO			T"AU	J" Version
Cell Name	Function	NII CEL	L SPEC	JIF ICAL LOI	<u> </u>			Number of BC
Cell Name	Tri-state Output	S. CMOS	Tatas	face Inn	ıt Duffe	r (True		Muliber of BC
H6CD	with Pull-down R			Tace Inp	ut buile	ı (ırue	'	10
Cell Symbol			Pro	pagation	Delay P	aramete	r	
		t	up	T	tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	2 Path
		0.74	0.03	1.07	0.03			X → IN
		1.08	0.047					OT → X
	1	(5.08)		(10.71)				1
IN —	<b>─</b>							
111	$\sqrt{}$							
								1
OT	x							
	V			}				
				į				
	_			ı			l	
	С							
			L		L		L	
			L →			Z + L	OT.	┥ 。
		t0		KCL	t0		CL	c → x
		1.8		*	2.44		.105	
		(17.0	0)	,,	(11.37	)		İ
			- 1			- 1		
	Input Loading		ļ			-		
Pin Name	Factor (lu)		l			1		1
OT	factor (ku)							1
C	2	<u> </u>	H →	7		$Z \rightarrow H$		_
C		t0	- n -	KCL	t0		CL	_
		3.7	7	VOT	1.23		048	-{
	Output Driving	(17.0		*	(11.37			
Pin Name	Factor (lu)	(2	7		(11.07	<b>′</b>		
IN	36		1			1		1
. <del></del>								
						1		

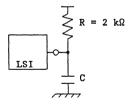


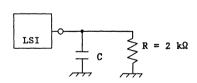


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6CD-E3 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"Al		
Cell Name	Function							Number of BC	
	Power Tri-state	Output	& CMOS	Interfa	ce				
H6E	Input Buffer (Tr	ue)						10	
Cell Symbol			Propagation Delay Parameter						
		t	up		td				
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		0.74	0.03	1.07				X → IN	
		1.49	0.032	2.34	0.036		l	OT → X	
	4	(4.21)		(5.40)					
IN	<b>─</b> < h								
714	, 7	l							
		1							
ОТ	x +	1						i	
	M	1					į		
		]	Ì						
	_								
	C	1	}				l	l l	
			<u></u>	L			L		
			L → Z			$Z \rightarrow L$		┥	
		t0		KCL	t0		KCL	C → X	
		2.6			2.5		.036	ļ	
		(19.8	0)	*	(5.5	9)			
		1				i			
	1	1				l			
Dia Nama	Input Loading					1			
Pin Name									
	Factor (lu)	ł	i			- 1		1	
OT	6			,					
		10	H → Z		+0	Z → H			
OT	6	t0		KCL	t0		KCL		
OT	6 2	4.4	7	KCL	1.4	4 0			
OT C	6 2 Output Driving		7			4 0	KCL		
OT C Pin Name	6 2 Output Driving Factor (lu)	4.4	7	KCL	1.4	4 0	KCL		
OT C	6 2 Output Driving	4.4	7	KCL	1.4	4 0	KCL		
OT C Pin Name	6 2 Output Driving Factor (lu)	4.4	7	KCL	1.4	4 0	KCL		

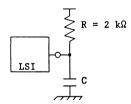


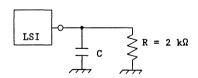


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

AU-H6E-E3 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A1	U" Version
Cell Name	Function					***************************************	<u> </u>	Number of BC
	Power Tri-state	Output	& CMOS	Interfa	ce			
H6EU	Input Buffer (Tr						1	10
Cell Symbol				agation		Paramet	er	
		t	up	T T	td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.74	0.03	1.07	0.03			X + IN
		1.49	0.032	2.34	0.036		ĺ	OT → X
ı		(4.21)		(5.40)				
<b></b>		` ′		` ′				
IN ——							J	
	$\setminus$ 1						1	1
от	> x							
			1					
			l			ł	l	l
	i							
	С		ļ	1				
						ļ	1	
			L + 2	:		$Z \rightarrow I$	,	
		t0		KCL	t0		KCL	C → X
		2.6	2		2.5	3 0	0.036	
		(19.8	(0)	ric	(5.5	9)		İ
			- 1					
						- 1		1
	Input Loading							
Pin Name	Factor (lu)		ł			- 1		
OT	6							
С	2		H → Z	:		Z → H	Ţ	
		t0		KCL	t0		KCL	
		4.4	.7		1.4	4 0	0.033	
	Output Driving	(19.8	(0)	**	(5.5	9)		1
Pin Name	Factor (lu)		1			-		
IN	36		1					
İ						[		[
						l		1
	1		- 1		1	1		

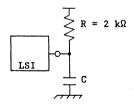


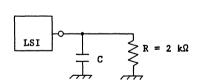


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6EU-E3 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N		"A"	U" Version
Cell Name	Function							Number of BC
	Power Tri-state	Output	& CMOS	Interfa	ce			
H6ED	Input Buffer (Tr	ue) wit	h Pull	-down Re	sistanc	е		10
Cell Symbol				pagation			er	
		t	up	T	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.74	0.03	1.07	0.03			X + IN
		1.49	0.032	2.34	0.036			OT → X
	4	(4.21)		(5.40)				į.
IN	<u> </u>			1			l	
111	$\sim$							
1				1				1
ОТ	x -							
	LY I						ļ	
							ĺ	1
	ı			1				ì
	C			1				1
			L→			$Z \rightarrow I$		
		t0		KCL	t0		KCL	C → X
•		2.6			2.5		0.036	1
		(19.8	0)	*	(5.5	9)		1
			1					
1	Input Loading		i					
Pin Name	Factor (lu)		1					1
TO	6		L_					_
C	2		Н →			Z → H		_
•		t0		KCL	t0		KCL	_
		4.4			1.4		0.033	l
l	Output Driving	(19.8	0)	**	(5.5	9)		1
Pin Name	Factor (lu)		- 1					l
IN	36		1					
						1		
		Į				- 1		
	1				İ			





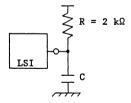
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

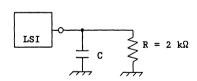
Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H6ED-E3 Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATION	1		"A	U"	Version
Cell Name	Function							Νι	umber of BC
	Tri-state Output	& Schm	itt Tr	igger In	out Buff	er			
H6S	(CMOS Type, True								14
Cell Symbol			Pro	pagation	Delay P	aramete	r		
		t	up	1	tdn				
İ		t0	KCL	t0	KCL	KCL2	CDR	2	Path
	!	1.99	0.13	2.47					X → IN
		1.08	0.047	1.95	0.103			- 1	$OT \rightarrow X$
	4	(5.08)		(10.71)	)	1		- 1	
IN	— II							- 1	
114				1	ł			- 1	
			İ	1				- 1	
OT -	> x						}	- 1	
	Y						}	- }	
							j	ļ	
	1						Ì	ļ	
	С						Ì	- [	
			L →			$Z \rightarrow L$			
		t0		KCL	t0		CL		$C \rightarrow X$
		1.8			2.44		.105		
		(17.0	0)	*	(11.37	)		- 1	
			- 1			1			
			- 1			1			
	Input Loading		i						
Pin Name	Factor (lu)								
OT	6								
С	2		Н →			Z → H			
	İ	t0		KCL	t0		CL		
	<u> </u>	3.7			1.23		048		
	Output Driving	(17.0	0)	*	(11.37	)		-	
Pin Name	Factor (lu)	1						- 1	
IN	18	]	)					- 1	
		1	J					- 1	
		1						1	
	i .	ı	1			1		- 1	

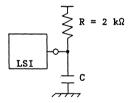


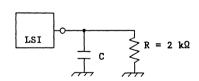


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6S-E3 Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N		"A	U"	Version
Cell Name	Function							N	umber of BC
	Tri-state Output	& Schm	itt Tr	igger In	out Buff	er			
H6SU	(CMOS Type, True								14
Cell Symbol			Pro	pagation	Delay P	aramete	r		
		t	up	Τ	tdn			$\neg$	
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		1.99	0.13	2.47	0.08				X → IN
		1.08	0.047	1.95	0.103			1	$OT \rightarrow X$
	4	(5.08)		(10.71			l	- 1	
IN	$-\sqrt{\pi}$							- 1	
114							1	- 1	
				1				1	
от —	x							- 1	
	M							ı	
				ļ			1	- 1	
	-			1	1		1	- 1	
	С			1				ļ	
					ــــــــــــــــــــــــــــــــــــــ	بـــــــــــــــــــــــــــــــــــــ	L		
		t0	L →	KCL	t0	$Z \rightarrow L$	CL		C → X
		1.8		KCT	2.44		105		C → X
		(17.0		*	(11.37		.103		
		(17.0	ן ני		(11.5/	'		- 1	
			-						
	Input Loading		1			1		ı	
Pin Name	Factor (lu)	1	ł						
OT	6		}					- 1	
C	2		H →	Z		$Z \rightarrow H$			
		t0		KCL	t0	K	CL		
		3.7	7		1.23	0.	048		
	Output Driving	(17.0	0)	*	(11.37	)		į	
Pin Name	Factor (lu)		1						
IN	18	1							
			- 1						
		1	1			1			
	1	1	- 1			1			





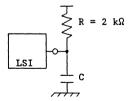
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

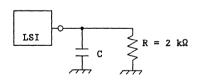
Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H6SU-E3 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	N		l "At	Jn	Version
Cell Name	Function	000	<u>D DI DOI</u>	11011110			<u> </u>		mber of BC
	Tri-state Output	& Schm	itt Tri	gger In	out Buffe:	r			
H6SD	(CMOS Type, True								14
Cell Symbol					Delay Pa	ramete	r		
		t	up	T	tdn			T	
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		1.99	0.13	2.47	0.08			T	X → IN
		1.08	0.047	1.95	0.103		j	- 1	$OT \rightarrow X$
		(5.08)		(10.71)					
IN	$-\sqrt{\pi}$			ļ			l	- 1	
114					1			- 1	
				1				-	
от —	x -			1					
	M			1				- 1	
							l	- 1	
					1 1		l	ı	
	С			ł			l	1	
				İ					
			$L \rightarrow Z$			$Z \rightarrow L$			
		t0		KCL	t0		CL	_	$C \rightarrow X$
		1.8			2.44	0	.105	į	
		(17.0	0)	3'0	(11.37)	1		1	
			- 1			1		1	
				1		-		- {	
	Input Loading			1		-		- 1	
Pin Name	Factor (lu)		ļ	ļ		1		1	
OT	6					L		_	
C	2		H → 2			$Z \rightarrow H$		_	
		t0		KCL	t0		CL	4	
	ļ	3.7	- 1		1.23	0.	048	- 1	
D. 11	Output Driving	(17.0	(1)	*	(11.37)	-		1	
Pin Name	Factor (lu)		1			1		- 1	
IN	18					1			
				į		- 1			
						1			
ı	I	1	1	j		1		- 1	

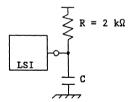


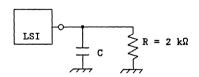


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

AU-H6SD-E3 Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATION	I		l "Al	U" Version
Cell Name	Function	000	<u> </u>	11011111	·		1	Number of BC
	Tri-state Output	& Schm	itt Tri	gger Int	out Buff	er		
H6R	(TTL Type, True)						- 1	14
Cell Symbol			Prop	agation	Delay P	aramete	r	
		t	up	l	tdn			
		t0	KCL	t0	KCL	KCL2	CDR	2 Path
		1.79	0.13	2.98	0.11			X → IN
		1.08	0.047	1.95	0.103			OT → X
	4	(5.08)		(10.71)	)			l
IN	<i>&lt;1</i> √h			}	1			
211				1				
				1				
OT -	x				1			
	Y							
	C							
	C			Ì	1			
	,		$L \rightarrow 2$	<del>!</del>		$Z \rightarrow L$	L	
		t0		KCL	t0		CL	⊢ c → x
		1.8		KOD	2.44		.105	
		(17.0	-	*	(11.37			
		(2	,	1	(22.0.	'		
	Input Loading					1		
Pin Name	Factor (lu)		1			-		
OT	6							
С	2		H → Z			Z → H		
		t0		KCL	t0		CL	
	<u> </u>	3.7			1.23		048	
	Output Driving	(17.0	0)	*	(11.37	)		1
Pin Name	Factor (lu)			1		- 1		}
								•
IN	18	ŀ	i	ì		į		
	18					ĺ		

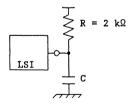


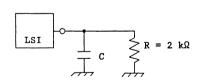


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6R-E3 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATION			JA"	J" Version
Cell Name	Function							Number of BC
	Tri-state Output	& Schm	itt Tr	igger Inp	ut Buff	er		
H6RU	(TTL Type, True)	with P	ull-up	Resistan	ce		1	14
Cell Symbol			Pro	pagation	Delay P	aramete	r	
		t	up	1	tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.79	0.13	2.98	0.11			X → IN
		1.08	0.047	1.95	0.103			OT → X
	*	(5.08)		(10.71)				
T).		` ′		1 '				
IN			i	1	]			1
	$\setminus$ 1				1			
от	> x			1				
	V							
					1			
	ı							
	С							
	· ·							-
			L →	7.	L	$Z \rightarrow L$	L	
		t0		KCL	t0		CL	d c → x
		1.8	6		2.44		.105	7
		(17.0		*	(11.37			
		(2/10	,	1	(22.0)	<b>'</b>		1
				1				
*	Input Loading			1		- 1		
Pin Name	Factor (lu)					1		
OT	6		- 1	1				
Ċ	2		Η →	$\frac{1}{z}$		Z → H		
J	1	t0	<del></del> -	KCL	t0		CL	
		3.7	7		1.23		048	7
	Output Driving	(17.0		o'c	(11.37			
Pin Name	Factor (lu)	(2	-/		(5/	´		
IN	18			İ		1		1
						1		
	1		1	i		1		1
								l .

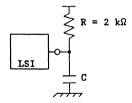


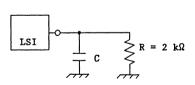


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6RU-E3 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A1	U" Version
	Function						<del></del>	Number of BO
	Tri-state Output	& Schm	itt Tri	gger In	put Buff	er		
H6RD	(TTL Type, True)	with P	ull-dow	m Resis	tance			14
Cell Symbol			Prop	agation	Delay P		r	
<b>i</b>			up		tdn			
}	'	t0	KCL	t0	KCL	KCL2	CDR	
		1.79	0.13	2.98			Ì	X → IN
,		1.08 (5.08)	0.047	1.95			1	OT → X
	<i>(</i> €)	(3.00)		(10.71	1			
IN —	<b>─</b> <~\/ h				1		}	
	<u> </u>							
от —	> <b>→</b> x						}	
	P						ļ	
				i				
							ļ	
	С						İ	į .
]			$L \rightarrow 2$	<del>,</del>	ــــــــــــــــــــــــــــــــــــــ	$Z \rightarrow L$	L	
		t0	<u> </u>	KCL	t0		CL	$ c \rightarrow x$
		1.8	6	NOD	2.44		.105	
		(17.0		*	(11.37			
		,	·			`		
			1			1		
	Input Loading					1		
Pin Name	Factor (lu)	1				1		
OT C	6 2	<u> </u>	H → 2	,		$Z \rightarrow H$		
"		to	-11 -7 -4	KCL	t0		CL	-
1		3.7	7		1.23		048	-
	Output Driving	(17.0		*	(11.37			
Pin Name	Factor (lu)				-	- 1		1
IN	18		1	,		1		
1								
1		1	- [					
1	I	1	1			- 1		1

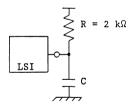


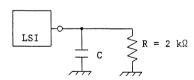


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6RD-E3 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U"	Version
Cell Name	Function							N.	umber of BC
	Tri-state Output	with N	oise Li	mit Res	istance				
Т8Н	& Input Buffer (	True)						L	9
Cell Symbol			Prop	agation	Delay Pa	ramete	r		
			up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.85	0.03	1.47	0.03				$X \rightarrow IN$
		3.35	0.047	6.26	0.103				$OT \rightarrow X$
		(7.35)		(15.02)					
IN									
III									
					1				
OT	<b>X</b>							ĺ	
					1 1				
					1 1				
	С				1				
					l				
			L → 2			$Z \rightarrow L$			
		t0		KCL	t0	K	CL		$C \rightarrow X$
		2.0	0		6.62	0.	105		
		(16.9	5)	*	(15.55)	ļ		ı	
	Input Loading								
Pin Name	Factor (lu)								
OT	2								
С	2		H → Z			$Z \rightarrow H$			
		t0		KCL	t0		CL		
		3.2	-		3.40	- 1	048		
	Output Driving	(16.9	5)	*	(15.55)				
Pin Name	Factor (lu)								
IN	36								
		1							
				-					

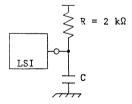


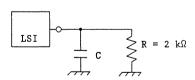


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the  ${\tt simulation.}$

AU-H8T-E2 | Sheet 1/1

							1 11	<b></b>
	CMOS GATE ARRAY U	NIT CEL	L SPEC	CIFICATIO	N		"AU	
Cell Name	Function							Number of BC
	Tri-state Output	_with N	oise I	Limit Res	istance			
H8TU	& Input Buffer (	True) w	ith Pu	ıll-up Re	sistance			9
Cell Symbol				opagation			r	·
			up		tdn			<b>↓</b>
		t0	KCL		KCL	KCL2	CDR2	
		0.85	0.03					X → IN
		3.35	0.04					OT → X
	1	(7.35)		(15.02	기			
IN	<b>&lt;</b> h						ì	
	7			1				
077	J ,,,			1				
OT -	x			1				
				1				1
					1			1
				İ	1			
	С			1				
			L →			$Z \rightarrow L$	L	
		t0		KCL	t0		CL	$c \rightarrow x$
		2.0	<u> </u>	KOL	6.62		105	- "
}		(16.9		*	(15.55		103	
Ì		(10.)	١,		(15.55	, I		
			1					
	Input Loading							
Pin Name	Factor (lu)	-						
OT	2	İ						
c	2		Н →	Z		$Z \rightarrow H$		1
	1 -	t0	$-\dot{-}$	KCL	t0		CL	7
1		3.2	0		3,40		048	1
	Output Driving	(16.9		*	(15.55			
Pin Name	Factor (lu)	`~~.,	-/		(22.55	<b>′</b>		
IN	36	1	1					
1		1						





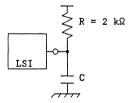
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

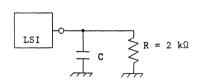
Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8TU-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	ı .		"A	U" Version
Cell Name	Function	I ODD	D DIDO.	110111101	`		1	Number of BC
	Tri-state Output	with N	oise L	mit Resi	stance			
нвтр	& Input Buffer (					ce	- 1	9
Cell Symbol			Pro	pagation	Delay P	aramete	r	
		t	up	T	tdn			
		t0	KCL	t0	KCL	KCL2	CDR	2 Path
		0.85	0.03	1.47	0.03			X → IN
		3.35	0.047	6.26	0.103			OT → X
		(7.35)		(15.02)				
*		` ′		` '				
IN —				İ				į.
					1			
то то	> x				1 1			
				ļ	1			Ì
				ł				
	1			1	1			1
	С		1	ļ				
				l	1			
			L → 2	Z		$Z \rightarrow L$		
		t0		KCL	t0	K	CL	C → X
		2.0	0		6.62	0.	105	7
		(16.9	5)	*	(15.55	)		İ
			1		`	´		
				ļ				
	Input Loading	1		1		1		
Pin Name	Factor (lu)			- 1				
OT	2	1				1		
С	2		H → 2	Z		Z → H		
		t0	T	KCL	t0	K	CL	
		3.2	0		3.40	0.	048	
	Output Driving	(16.9	5)	*	(15.55	)		
Pin Name	Factor (lu)	,		1	•	·		1
IN	36	1	1			- 1		
	1	l	1			1		1





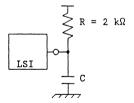
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

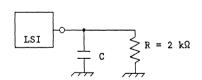
Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8TD-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPEC	FICATION	Į.		"Al	
Cell Name	Function							Number of BC
	Power Tri-state	Output	with No	oise Limi	it Resis	tance		
H8W	& Input Buffer (	True)						9
Cell Symbol			Prop	pagation	Delay P	aramete	r	
		t	up	T	tdn			
		t0	KCL	t0	KCL	KCL2	CDR	2 Path
		0.85	0.03	1.47	0.03			X → IN
		4.06	0.033	8.64	0.046			OT → X
	4	(6.87)		(12.55)	)			
IN	<b>─</b>			į.				
714	$\backslash \mathcal{N}$			1				
				1				1
OT TO	x							
Ì	7						ļ	
	1			[				
	C			į.				
			L → 2			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		3.5		. 1	8.36		046	
		(21.0	9)	*	(12.27	)		
			- 1	1				
	<del></del>		- 1					
D' - M	Input Loading		l	l				
Pin Name	Factor (lu)		- [	ļ				
OT C	2 2		H → ;	,		$Z \rightarrow H$		_
C	2	+0	_ n → /	KCL	+0		CL	
		t0 4.0	$\overline{}$	VCT	±0 4.30		033	
	Output Driving		- 1	*			033	
Din Name		(21.0	"	.*	(12.27	'		
Pin Name	Factor (lu)		- 1	l				
	1 30	ı	1	i i		i		ı
IN	1	l	i	į				1
IN				l				





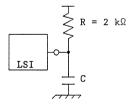
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

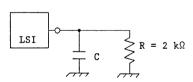
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8W-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	J	*****	"AU	Ţ#	Version
Cell Name	Function	000	<u> </u>	1 10111101			Ť		mber of BC
	Power Tri-state	Output	with No	ise Limi	t Resist	ance			
H8WU	& Input Buffer (								9
Cell Symbol					Delay Pa	ramete	r		
		t	up		tdn			$\neg$	
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.85	0.03	1.47	0.03				$X \rightarrow IN$
		4.06	0.033	8.64	0.046			- 1	OT → X
	1	(6.87)		(12.55)	)				
IN	<b>-</b> < h '				1				
				Į					
	\				1				
от —	x x						ļ		
	Y				1 1		1	- 1	
					1 1			-	
					1		}	-	
	С				1 1		İ	-	
			$L \rightarrow 2$	<del> </del>	JL	$Z \rightarrow L$	L	+	
		t0	<u> </u>	KCL	t0		CL		C → X
		3.5	0	KCL	8.36		046	$\dashv$	C - A
		(21.0	,	*	(12.27)		040		
		(21.0	<sup>-</sup> /		(12.27)				
	Input Loading								
Pin Name	Factor (lu)			ŀ					
OT	2			-					
С	2		H → Z	2		Z → H		$\neg$	
		t0	T	KCL	t0	K	CL		
		4.0	0		4.30	0.	033		
	Output Driving	(21.0	9)	*	(12.27)				
Pin Name	Factor (lu)								
IN	36			İ					
	1								

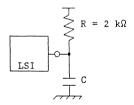


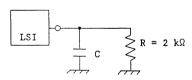


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8WU-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N N		"A	U"	Version
Cell Name	Function							Nı	umber of BC
	Power Tri-state	Output	with No	oise Lim	it Resis	tance			
H8WD	& Input Buffer (	True) w	ith Pu	11-down	Resistan	ce			9
Cell Symbol			Pro	pagation	Delay P	aramete	r		
		t	up	T	tdn			T	
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.85	0.03	1.47	0.03			T	X → IN
ı		4.06	0.033	8.64	0.046		1	1	$OT \rightarrow X$
ı	4	(6.87)		(12.55)	)		1		
IN -	<u> </u>			1				-	
TIA	$\sqrt{N}$			1				- 1	
				1					
ОТ —	x						}	1	
	M							ŀ	
					1		1	1	
	-			1	1			1	
	С						l	Į	
					1	L	<u> </u>	_	
			L →			$Z \rightarrow L$	TOT		
		t0 3.5		KCL	t0		CL	-	$C \rightarrow X$
			- 1	*	8.36	1 .	046		
		(21.0	9)	*	(12.27	)			
			1					- 1	
	T+ T3:	-							
Dán Nama	Input Loading		1					1	
Pin Name	Factor (lu)	1							
OT C	2 2	<u> </u>	H →	7		$Z \rightarrow H$			
		10		KCL	+0		KCL	$\dashv$	
		t0 4.0	<del>-  -</del>	VCT	t0 4.30		.033	$\dashv$	
	Output Driving	(21.0	- 1	*	(12.27		.033		
Pin Name	Factor (lu)	(21.0	ا (د		(12.2/	,			
IN	36	{	1			1		١	
114	]							1	
								-	
	I .	1							

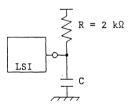


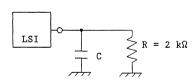


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8WD-E2 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATION	N		"AL	J" Version
Cell Name	Function							Number of BC
	Tri-state Output	Buffer	with h	Noise Li	nit Resis	tance	1	
H8C	& CMOS Interface	Input	Buffer	(True)				9
Cell Symbol			Prop	pagation	Delay Pa	ramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
	*	0.74	0.03	1.07				X → IN
		3.35	0.047	6.26			]	OT → X
	1	(7.35)		(15.02)				
IN	<b>─</b>						1	
±11	<u> </u>							
OT -	x						1	
	VΥ			1	1			
					1			
	1			1				
	С						ĺ	
				1	1		L	
			L → :			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		2.0	- 1		6.62		.105	
		(16.9	5)	**	(15.55)			
			- 1	i		1		
			- 1					
	Input Loading							
Pin Name	Factor (lu)							
TO	2							_
С	2		H → 1			$Z \rightarrow H$	.O.T	
		t0		KCL	t0		CL	-
	1 D	3.2		*	3.40		048	
Din Name	Output Driving	(16.9	ا رد	*	(15.55)			
Pin Name IN	Factor (lu)		1			1		
IN	30					1		
			1					
	1	ſ	1			1 .		1

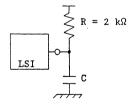


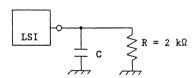


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8C-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U"	Version
Cell Name	Function		<del></del>				1	Νι	mber of BC
	Tri-state Output	Buffer	w/ Nois	se Limit	Resista	nce &			
H8CU	CMOS Interface In	put Buf	fer (Tr	ue) w/	Pull-up	Resista	nce		9
Cell Symbol			Prop	pagation	Delay P	aramete	r		
			up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.74	0.03	1.07	1			- 1	$X \rightarrow IN$
		3.35	0.047	6.26			1		$OT \rightarrow X$
	1	(7.35)		(15.02	)		1	1	
IN	—< h						1	- 1	
				1			1	- 1	
							1	- 1	
от —	x			1					
	V	ŀ		1			1	- 1	
				1			1	į	
	, ~		Ì	l				ĺ	
	С		ļ				ł	Ì	
			$L \rightarrow 2$	7	J	$Z \rightarrow L$	<u> </u>	+	
		t0	<u> </u>	KCL	t0		CL	$\dashv$	C → X
		2.0	10	KOD	6.62		0.105	$\dashv$	0 , A
		(16.9		*	(15.55	1	05	- 1	
		(10.)	"		(13.33	.			
								-	
	Input Loading	1	}					- [	
Pin Name	Factor (lu)	1	1					-	
OT	2	1		į				-	
С	2		H → 2	Z		$Z \rightarrow H$		$\neg$	
		t0		KCL	t0	ŀ	CL	$\neg$	
		3.2	.0		3.40	0.	048		
	Output Driving	(16.9	5)	*	(15.55	)			
Pin Name	Factor (lu)	}						- [	
IN	36	1	- 1			- 1			
			1			1		Í	
		1	1						
	1	1	1			- 1		- 1	





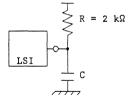
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

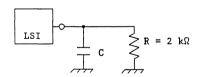
Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8CU-E2 | Sheet 1/1

FILITTEIL	CMOS GATE ARRAY U	NIT CET	T CDFC	TETCATIO	N.		l "AU	J" Version
Cell Name	Function	MII OED	L SEEC	TETORITO	<u> </u>			Number of BC
ocii Name	Tri-state Output	Ruffer	w/ Noi	se Limit	Resistan	nce & C		14dinber Of BO
HSCD	Interface Input B							9
Cell Symbol		(		pagation				
OCII Dymbo.	·	+	up	pagacion	tdn	ar ame ee		T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.74	0.03	1.07		ROBE	ODITZ	X → IN
		3.35	0.047		0.103			OT → X
		(7.35)		(15.02	1 1			
		(,,,,,,		(13.02	1 1			
IN —								
	N 1							
от	→ x							
01	· ·				1 1			
		İ		1				
	1	1	ļ	1	1 1			
	С	ļ	İ	İ				
	ŭ			1	1			
		<b></b>	L →	7.		$Z \rightarrow L$		
		t0	<u> </u>	KCL	t0		CL	d c → x
		2.0	0		6.62		.105	-
		(16.9	- 1	*	(15.55)			
		(201)	-/		(	´		
		1						
	Input Loading	1						
Pin Name	Factor (lu)		1			- 1		
OT	2	1						
C	2		H →	Z		$Z \rightarrow H$		7
		t0		KCL	t0	K	CL	
		3.2	.0		3.40	0.	048	
	Output Driving	(16.9		*	(15.55)	)		
Pin Name	Factor (lu)	1			•			
IN	36	1						
		1	j					j
	1	1				İ		

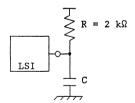


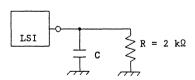


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8CD-E2 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N		"AU	Version
Cell Name	Function						1	Number of BO
	Power Tri-state	Output	Buffer	w/ Nois	e Limit R	esistanc	e	
H8E	& CMOS Interface	Input	Buffer	(True)			- 1	9
Cell Symbol		-	Pro	pagation	Delay Pa	rameter		
		t	up		tdn			
	1	t0	KCL	t0	KCL	KCL2	CDR:	Path
	!	0.74	0.03	1.07	0.03			X - IN
		4.06	0.033	8.64	0.046			OT → X
	4	(6.87)		(12.55	)			
IN	<b>─</b>			ļ				
III				ł				
ОТ	<b>→</b> x							ì
	Y			l	i I			1
								1
	1		ŀ	1				
	С	, i		1	1 1			
								1
			L →			$Z \rightarrow L$		_
		t0		KCL	t0	KCI		C → X
		3.5			8.36	0.04	+6	1
		(21.0	9)	*	(12.27)			
								1
			-					1
		Į.						
								4
C	2		_ н →		1			4
				VCT				4
	Output Deduction	1	- 1	*			3	
Din Name		(21.0	ן נפי	•	(12.2/)	-		
		1				1		
TIA	30				}	1		1
		1	1					
Pin Name OT C Pin Name IN	Input Loading Factor (lu)  2 2 2  Output Driving Factor (lu)  36	t0 4.0 (21.0	- 1	Z KCL *	t0 4.30 (12.27)	Z → H   KCI   0.03		

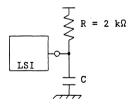


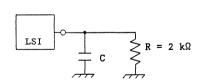


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

AU-H8E-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N		"AU"	
Cell Name	Function							umber of BC
	Power Tri-state 0							
H8EU	CMOS Interface In	put Buf	fer (Ti	rue) w/	Pull-up R	esistan	ce	9
Cell Symbo	1		Prop	pagation	Delay Pa	rameter		
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.74	0.03	1.07	0.03			X → IN
		4.06	0.033	8.64	0.046			$OT \rightarrow X$
		(6.87)		(12.55	)			
IN				ł	1 1			
IN	$\mathcal{N}$							
ОТ	-  >- <b>-</b> x							
	V .							
				1	i			
	į			1				
	C <sup>.</sup>							
				ł				
			L → 2	Z		Z + L		
		t0		KCL	t0	KC	L	C → X
		3.5	0		8.36	0.0	46	
		(21.0	9)	**	(12.27)			
		(==::	1		(,	1		
			- 1					
	Input Loading							
Pin Name	Factor (lu)							
OT	2	1						
C	2		H → :	7.		$Z \rightarrow H$		
U	"	t0		KCL	t0	KC	'T.	
		4.0	<del>.  </del>	VOT	4.30	0.0		
	Output Driving	(21.0		n/c	(12.27)		-55	
Pin Name	Factor (lu)	(21.0	<sup>-</sup> /		(12.2/)			
IN IN	36					1		
114	30	1			ļ			
		l	j j					





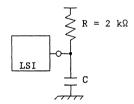
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

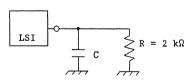
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8EU-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPEC	FICATIO	N	,	"AU'		
Cell Name	Function							Number	of I
	Power Tri-state O								
H8ED	CMOS Interface In	put Buf	fer (T	ue) w/	Pull-down	Resist	ance	9	
Cell Symbo			Proj	pagation	Delay Par	ameter			
			up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR2		
		0.74	0.03	1.07	1 1		}	X →	
		4.06	0.033	8.64				OT →	X
	· /	(6.87)		(12.55	)		l	1	
IN —	<b>─</b> < h						l	1	
	, 7	1		İ					
				1	1			1	
то то	- x	1 1		i	1			1	
	V			1				1	
				ļ	1		ļ	Į.	
	_						l		
	С	1 1					ĺ		
		لـــــا		<u></u>	إـــــا		l	ļ	
		10	L →	KCL		Z → L   KC	т	l c→	v
		t0 3.5		KCL	t0 8.36	0.0		∪ →	Х
			- 1	*	(12.27)	0.0	146		
		(21.0	9)	^	(12.27)	ĺ			
		ļ	ı			-		1	
	Input Loading	1	1			1			
Pin Name	Factor (lu)		1			1		1	
OT	2	1	İ			1			
C	2		Η →	7		Z → H		-	
U		t0		KCL	t0	KC	T.	1	
		4.0	<del>.  </del>	VOTI	4.30	0.0		1	
	Output Driving	(21.0	- 1	**	(12.27)	0.0	, , , ,		
Pin Name	Factor (lu)	(21.0			(12.27)	1			
IN	36	1							
	""		}					1	
	1	1				- 1			
		1	1		1	1		1	

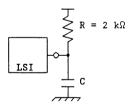


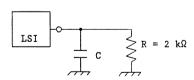


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

AU-H8ED-E2 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U"	Version
Cell Name	Function							Nu	mber of BC
	Tri-state Output	& Schm	itt Tri	gger In	put Buff	er			
H8S	(CMOS Type, True								13
Cell Symbol					Delay P		er		· · · · · · · · · · · · · · · · · · ·
		t	up	T	tdn			Т	
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		1.99	0.13	2.47	0.08				X → IN
		3.35	0.047	6.26	0.103			H	$OT \rightarrow X$
ı		(7.35)		(15.02	)	İ		- 1	
in —								ı	
IN						•	İ	1	
OT	→ x					ĺ			
								1	
							1	ł	
	1					1	1		
	C					1		1	
			L → 2			$Z \rightarrow L$			
		t0		KCL	t0		KCL		$C \rightarrow X$
		2.0			6.62		. 105	-	
		(16.9	5)	*	(15.55	)			
								- 1	
	Input Loading								
Pin Name	Factor (lu)								
TO	2							_	
С	2		H → Z			Z <b>→</b> H			
		t0		KCL	t0		KCL		
		3.2	- 1		3.40		.048		
	Output Driving	(16.9	5)	*	(15.55	)			
Pin Name	Factor (lu)								
IN	18								
	1								
	I	I	1		l	- 1		ı	

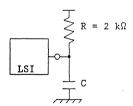


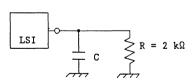


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of  $85\ pF$  is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8S-E2 | Sheet 1/1

FILITEII	CMOS GATE ARRAY U	NITT CET	T CDE	CIPICATI	ONI			JA"	1111	Version
Cell Name	Function	NII CEL	L SPE	CIFICATI	UN			1 4		ber of BC
Cell Name	Tri-state Output	& Schmi	tt Tr	igger In	nut Ruf	fer(C	MOS	Type	ITUII	iber of bo
H8SU	True) w/ Noise L									13
Cell Symbo		IMILO INC		opagatio						
5522 5755	_	t	up	Jugusta		dn		<del>-</del>	$\top$	
		t0	KCL	t0	KCI	, F	CL2	CDR	2	Path
		1.99	0.13	2.4	7 0.08				$\top$	X → IN
		3.35	0.04	7 6.2	6 0.10	3 .				$OT \rightarrow X$
1	4	(7.35)		(15.0	2)	ì			- 1	
IN	<i>──</i> < <i>ॼ</i> Ь									
111					1				- 1	
					1	İ				
ОТ	- x				1	-			1	
-	V								İ	
į.					1	ı			1	
Ì									-	
	С	i				- 1			-	
İ			L →	7	ㅜㅗ		→ L	L	+	······································
1		t0	<del></del>	KCL	<del>                                     </del>	:0		CL	$\dashv$	C → X
		2.0	0	ROB		62		105	$\dashv$	0 · 1.
		(16.9	1	*	(15		"			
			-		\	,				
			ł							
	Input Loading								1	
Pin Name	Factor (lu)		-				l		-	
OT	2						<u> </u>			
C	2		Η →				→ H			
1		t0		KCL		:0		CL	_	
	Out out Duty	3.2		*		40	1 0.	048		
Pin Name	Output Driving Factor (lu)	(16.9	ا (د	*	(12	.55)				
IN	18				1		1			
111	10		1							
							1			
			1						- 1	

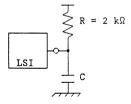


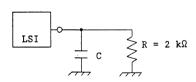


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8SU-E2 | Sheet 1/1

בווזדפוו	CMOS GATE ARRAY U	NIT CEI	CDEC	TETCATION	ī		"AU"	Version
	Function	NII CEL	L SILC.	IFICATIO	<u> </u>			Number of BC
COII Maile	Tri-state Output	& Schmi	tt Tri	gger Inni	t Buffer	(CMOS		Tambel Of Do
H8SD	True) w/ Noise L							13
Cell Symbol		IMIO NO			Delay Pa			
GOII DJDO.		t	up	T T	tdn		Ξ	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.99	0.13	2.47				X + IN
		3.35	0.047	6.26	0.103			OT → X
		(7.35)		(15.02)				1
TN		` ′		` '				
IN —	. "							
					1 1			
от	→ x							
	V				1			
				1	1			
	'			1	1			
	С			1	1			·
				<u> </u>	<u> </u>			
			L→			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		2.0		_ 1	6.62	0.	105	
		(16.9	5)	*	(15.55)			
				İ				
				ļ				
<b>.</b>	Input Loading		1	}		-		
Pin Name	Factor (lu)			1		-		
OT	2		Н →			$Z \rightarrow H$		4
С	2	1.	H →				CT	4
		t0		KCL	t0		CL	4
	Out-ut Duis	3.2	-	*	3.40	0.	048	
Din Nor-	Output Driving	(16.9	ا (د	^	(15.55)			
Pin Name IN	Factor (lu)					-		
114	10					- 1		1
			- 1					
			1					
		l						1

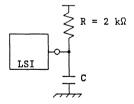


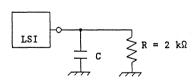


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8SD-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATION	N		"A	U"	Version
Cell Name	Function							Νι	mber of BC
	Tri-state Output	& Schm	itt Tr	igger In	out Buff	er			
H8R	(TTL Type, True)								13
Cell Symbol			Pro	pagation	Delay P	aramete	r		
		t	up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		1.79	0.13	2.98					$X \rightarrow IN$
ı		3.35	0.047				İ	-	$OT \rightarrow X$
	1	(7.35)		(15.02)	)(			- [	
in —	<i>&lt;</i> √ <i>T</i>  ¬						l	- 1	
	<u> </u>							-	
om -									
OT -	x								
				ļ				- 1	
		· .		1				-	
	C							ı	
	·							1	
			L →	7.		$Z \rightarrow L$	1	$\dashv$	
		t0	_ <del>-</del>	KCL	t0		CL	$\dashv$	$C \rightarrow X$
		2.0	0		6.62	0.	105	$\neg$	
		(16.9	5)	**	(15.55	)		I	
		,			•	`			
								- 1	
	Input Loading		ı			- [		-	
Pin Name	Factor (lu)					- 1		- }	
OT	2							_	
С	2		Н →			$Z \rightarrow H$		_	
		t0		KCL	t0	The second second second	CL	_	
	LOUIS DUICE	3.2	-	*	3.40	1	048		
Din Nama	Output Driving	(16.9	ارد	н	(15.55	,			
Pin Name IN	Factor (lu)		-	İ		1			
TIA	10					1		1	
	}		1					1	

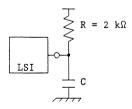


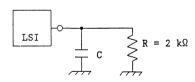


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8R-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	N .		"A		Version
Cell Name	Function							Nı	umber of BC
ĺ	Tri-state Output								
H8RU	True) w/ Noise Li	mit Res							13
Cell Symbo	1			agation	Delay Pa	ramete	r		
			up		tdn			_	
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		1.79	0.13	2.98	0.11				$X \rightarrow IN$
		3.35	0.047	6.26	0.103		1	- [	$OT \rightarrow X$
	1	(7.35)		(15.02)	)			- 1	
IN -	—< <i>I</i> h				1		1	ı	
	7								
				1					
ОТ	- x								
	VY			i	} }			- 1	
					1 1				
	-								
	C							1	
				l	11		L	_	
			L → Z			$Z \rightarrow L$	OT	_	0 . 11
		t0		KCL	t0		CL	-	$C \rightarrow X$
		2.0	- 1	*	6.62		105		
		(16.9	ا (د	"	(15.55)	'		- 1	
								- 1	
	T					ı		١	
Pin Name	Input Loading			I					
OT OT	Factor (lu)					1		ı	
C	2 2		H → Z	,		$Z \rightarrow H$		$\dashv$	
C		t0	n 7 2	KCL	t0		CL	$\dashv$	
		3.2	0	VOT	3,40		048	$\dashv$	
	Output Driving	(16.9		*	(15.55)	1	040		
Pin Name	Factor (lu)	(10.9	<sup>3</sup> /		(13.33)	'		ļ	
IN	18								
711	10					1		- 1	
	1		i			- 1		- 1	

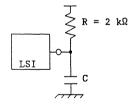


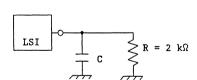


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8RU-E2 Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPE	CIFICATIO	N .		l "AU'	' Version
Cell Name	Function				·			Number of BC
	Tri-state Output	& Schmi	tt Tr	igger Inp	ut Buffe	r(TTL T		
H8RD	True) w/ Noise Li							13
Cell Symbo				opagation				
		t	up	1	tdn			T Total
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.79	0.13		0.11		· · · · · · · · · · · · · · · · · · ·	X → IN
		3.35	0.04				Ì	OT → X
		(7.35)		(15.02	)	<b>\</b>	l	
	\tau_{\tau_{\text{\tin}\text{\ti}\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\tin}\text{\texi}}\\ \tittt{\text{\text{\text{\text{\text{\texi}\til\text{\tex{\text{\text{\text{\text{\text{\texi}\text{\texi}\tint{\text{\text{\text{\text{\texi}\text{\text{\texi}\text{\texit{\text{\	( , , , ,		,	1		1	
IN —				ļ		İ		
				l	1		Ì	1
от	-		ŀ	l		ľ		
	P			İ			İ	
				1		1	1	1
	1					<b>\</b>		1
	С					Į	l	
			L →	Z		$Z \rightarrow L$		
		t0		KCL	t0	K	CL	1 c → x
		2.0	0		6.62	0.	105	7
		(16.9	5)	n'e	(15.55	o 1		İ
					,	´		
			l					
	Input Loading	1	1					
Pin Name	Factor (lu)		1					1
OT	2	1						]
С	2		H →	Z		Z → H		
		t0		KCL	. t0		CL	
		3.2	.0		3.40	0.	048	
	Output Driving	(16.9	5)	*	(15.55	5)		
Pin Name	Factor (lu)	]				-		1
IN	18					1		1
1			į.					
					1	[		
	1	1	1			- 1		1





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8RD-E2 | Sheet 1/1

FILITTEIL	CMOS GATE ARRAY U	NITT CEL	CDECT	FICATIO	NI .		"AU	" Version
Cell Name	Function	NII CEL	L SPECI	FICATIO	N			Number of BC
IKC	CMOS Interface C	lock In	put Buf	fer(Inv	erter)			4
Cell Symbol		<u> </u>		agation	Delay td	Paramet	er	
		t0	up KCL	t0	KCL	KCL2	CDR2	- Poth
		1.70	0.01	1.62	0.01	KULZ	CDKZ	Path X → CI
		1.,,	0.01	1.02	"""		ì	" "
							ŀ	
							İ	1
								1
	<u> </u>						l	1
х —	→— cī	1					l	
								1
								1
		Parame	ter			T S	ymbol	Typ(ns)*
		1414					,	+ -7F(7
İ								
		<u>j</u>						1
	Input Loading	1						1
Pin Name	Factor (lu)	1				j		
		ŀ						
						- 1		
						-		
	Output Driving	1				- 1		
Pin Name	Factor (lu)	1						
CI	200	1						
}	1							
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case of	peratin	ng condition
	<u> </u>	are	given b	y the m	aximum	delay n	nultipl	ier.
1								
1								
								İ
								i
1								
AU-IKC-E1	Sheet 1/1							Page 20-79

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"A	U"	Version
Cell Name	Function								umber of BC
	CMOS Interface C	lock In	put Buf	fer(Inv	erter)				
IKCU	with Pull-up Res	istance						<u></u>	4
Cell Symbol				agation			er		
		t0	up KCL	t0	td KCL	n KCL2	CDR2	-1	Path
		1.70	0.01	1.62	0.01	TOU2	ODICZ	-	X → CI
								١	
								- 1	
								- 1	
								- 1	
х	<b>∞</b> — сі							- 1	•
Α.	01							l	
							Ì	١	
							}	- 1	
							<u> </u>		
		Parame	ter		-	S	ymbol	Ц	Typ(ns)*
						İ		l	
	Input Loading								
Pin Name	Factor (lu)								
	1							- 1	
	1	1							
	Output Driving	1							
Pin Name	Factor (lu)								
CI	200								
					. 41.				
		" Mini	mum val	ues for	tne ty	pical o	perat	tin irr	g condition. condition
		are	values given h	or the	aximum	delay n	nılti.	riig riig	er.
		, are	PTACH F	, one ii	·~VTIIIIII	ccray i			· · ·
ļ									
AU-IKCU-E1	Sheet 1/1								Page 20-80

FUJITSU (	MOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N		"AU	" Version
Cell Name	Function						1	Number of BC
THEN	CMOS Interface C	lock In	out Buf	fer(Inv	erter)			,
IKCD Cell Symbol	with Pull-down R	esistan	Dron	agation	Dolor	Daramat		4
Cell bymbol		tı	up rrop	agation	td		er	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.70	0.01	1.62	0.01			X → CI
		1					1	1
х	>> c1							1
	<b>.</b> 0.							
		Parame	ter			S	ymbol	Typ(ns)*
						- 1		1
						1		
		į.				- 1		
	Input Loading	1						
Pin Name	Factor (lu)							
								1
		}						
						1		
	Output Driving	l				ļ		
Pin Name	Factor (lu)	1						l
CI	200	1				ļ		
	į	* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
								g condition
	<u></u>	are	given b	y the m	aximum	delay n	ultipl	ier.
AU-IKCD-E1	Sheet 1/1							Page 20-81

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			U" Version
Cell Name	Function							Number of BC
ILC	CMOS Interfere	look T-	nu+ D	for (T	٥)			_
Cell Symbol	CMOS Interface C	TOCK III	Pron	agation	Delav	Paramet	er	6
		t	up	3-3-011	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path X + CI
		1.53	0.01	2.12	0.01		1	X + CI
							1	<b>j</b>
							}	[
								1
							1	
							1	
	<u> </u>						İ	1
х —	CI						1	l l
							ļ	
							ļ	
							<u> </u>	
		Parame	ter			- 1	Symbol	Typ(ns)*
								1
1								
1								
						Ì		
Pin Name	Input Loading Factor (lu)					1		
1111 Hame	Tactor (zu)					1		
}								
		ł				i		
	1							
ļ	Output Driving	}				Ì		
Pin Name	Factor (lu)							
CI	200							
				_				
		The	mum val	ues for	the ty	rpical o	operat	ting condition. ing condition
ĺ		are	given h	v the n	naximum	delav i	multi:	olier.
			8					
					•			
1								
1								
1								
1								
1								
AU-ILC-E1	Sheet 1/1							Page 20-82

FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"AU	" Version
Cell Name	Function						T	Number of BC
	CMOS Interface C	lock In	put Buf	fer(Tru	e)			
ILCU	with Pull-up Res			•	•		Ì	6
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td		***************************************	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.53	0.01	2.12	0.01			X + CI
		1.50	0.02					" "
			1			•		
								1
							l	
								1
	•							1
								1
1	_		1				l	
х —	> cı							i i
1								i i
			<b> </b>				1	l i
			l				į	1
		Parame	ter				ymbol	Typ(ns)*
						- 1		
						-		
	Input Loading							1
Pin Name	Factor (lu)					i		
I III Mame	Tactor (24)							
	1					- 1		
	1							
	<del> </del>					- 1		
n	Output Driving							
Pin Name	Factor (lu)					1		
CI	200							
				_				
		" Mini	lmum val	ues for	the ty	pical o	operat:	ing condition.
		The	values	for the	worst	case of	perati	ng condition
		are	given b	y the n	naximum	delay r	nultip	lier.
1								
								( n 00 00
AU-ILCU-E1	Sheet 1/1							Page 20-83

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			AU"	
Cell Name	Function							N	umber of BC
	CMOS Interface C	lock In	put Buf	fer(Tru	e)				
ILCD	with Pull-down R	esistan	се						6
Cell Symbol				agation	Delay		eter		
			up		td		0 1 05-	<u>,</u>	<b>.</b>
		t0	KCL	t0	KCL	KCL	2 CDF	(2	Path
		1.53	0.01	2.12	0.01		- 1		X → CI
							ı	l	
							1		
							- 1		
							- 1		
							1		
							- 1		
v	77						- 1		
х —	CI CI						- 1		
							1		
							1		
		Parame	ter		L	<del></del>	Symbo	<u>. 1</u>	Typ(ns)*
		rarame	CET			-+	Оушос	-	Typ(ns)
						- 1			
						1			
	Input Loading					1			
Pin Name	Factor (lu)								
	1					1			
						1			
Ì						1			}
ļ						1			1
						1			1
	Output Driving					1			1
Pin Name	Factor (lu)								1
CI	200								l
		* Mini	mum val	ues for	the ty	pical	oper	atin	g condition.
		The	values	for the	worst	case	opera	ting	condition
ļ		are	given b	y the m	naximum	delay	mult	ipli	er.
1									
1									
ĺ									
1									
1									
1									
1									
1									
1									
1									
1									
1									
1									
1									
1									
AU-TI-CD-F1	Sheet 1/1								Page 20-84
1 170 THON-PT	1 011000 1/1								1 10KG 20 04

FUJITSU (	UJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version									
Cell Name	Function								N	umber of BC
O2BF	Output Buffer (I	OL=8mA,	True)							3
Cell Symbol				agation			nete	r		
			up		tdn					
		t0	KCL	t0	KCL	K	CL2	CDR	2	Path
		0.86	0.047	1.09	0.052				- 1	OT → X
		(3.68)		(4.21)					- 1	
									- 1	
									- 1	
									- 1	
	_									
от	x									
"	^ 1								- 1	
		Parame	<u> </u>		L	Щ,	S17	mbol	$\dashv$	Typ(ns)*
1		rarame	rer				Зу	шоот	-	Typ(IIS)
}										
										,
	Input Loading									
Pin Name	Factor (lu)									
OT	6	1								
ļ										
	Output Driving									
Pin Name	Factor (lu)	İ								
							L			
		+ M:-:	v.a1	was for	+ha +	400	1		- 4	a condition
										g condition. condition
				y the ma						
Note: 1. T	he unit of K $_{ m CL}$ is	ns/pF.								
, ,	utput load capaci	tance c	v€ 60 n¥	lie neod	l for Fu	44+	en'e	,		
	ogic simulation.	.cance C	, 00 pr	13 4360	. LOL FU	.,	5 u 5			
·	J									
3. Т	he parameters in	parenth	eses ar	e the va	lues ap	pli	ed t	o th	16	simulation.

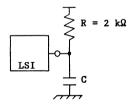
AU-02BF-E2 Sheet 1/1

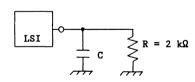
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION											
Output Buffer (IOL=8mA, True)   with Noise Limit Resistance	FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION						
Victor   V	Cell Name									N	umber of BC
Propagation Delay Parameter   tup   tdn											
Tup   Tdn		with Noise Limit	Resist								4
The values for the typical operating condition  The values for the typical operating condition  The values for the worst case operating condition	Cell Symbol			Prop	agation	Delay P	arai	nete	r		
OT  A  Parameter  Parameter  Symbol Typ(ns)*  Pin Name  Factor (\$\mathbb{l}\	•										
Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  OT  Pin Name Factor (lu)  Whinimum values for the typical operating condition The values for the worst case operating condition							K	CL2	CDR	2	
Parameter Symbol Typ(ns)*  Pin Name Factor (Lu)  OT 2  Minimum values for the typical operating condition The values for the worst case operating condition											OT → X
Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  OT 2  Minimum values for the typical operating condition The values for the worst case operating condition			(6.57)		(10.57)						
Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  OT 2  Minimum values for the typical operating condition The values for the worst case operating condition											
Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  OT 2  Minimum values for the typical operating condition The values for the worst case operating condition										- 1	
Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  OT 2  Minimum values for the typical operating condition The values for the worst case operating condition											
Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  OT 2  Minimum values for the typical operating condition The values for the worst case operating condition											
Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  OT 2  Minimum values for the typical operating condition The values for the worst case operating condition											
Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  OT 2  Minimum values for the typical operating condition The values for the worst case operating condition											
Pin Name   Input Loading   Factor (lu)   OT   2    Pin Name   Output Driving   Factor (lu)   * Minimum values for the typical operating condition   The values for the worst case operating condition	OT -	x									
Pin Name   Input Loading   Factor (lu)   OT   2    Pin Name   Output Driving   Factor (lu)   * Minimum values for the typical operating condition   The values for the worst case operating condition											
Pin Name   Input Loading   Factor (lu)   OT   2    Pin Name   Output Driving   Factor (lu)   * Minimum values for the typical operating condition   The values for the worst case operating condition											
Pin Name   Input Loading   Factor (lu)   OT   2    Pin Name   Output Driving   Factor (lu)   * Minimum values for the typical operating condition   The values for the worst case operating condition											
Pin Name   Input Loading   Factor (lu)   OT   2    Pin Name   Output Driving   Factor (lu)   * Minimum values for the typical operating condition   The values for the worst case operating condition											
Pin Name Factor (lu)  OT 2  Output Driving Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition			Parame	ter				Sy	mbol		Typ(ns)*
Pin Name Factor (lu)  OT 2  Output Driving Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition							ı				
Pin Name Factor (lu)  OT 2  Output Driving Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition							1				
Pin Name Factor (lu)  OT 2  Output Driving Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition											
Pin Name Factor (lu)  OT 2  Output Driving Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition							- 1				
Pin Name Factor (lu)  OT 2  Output Driving Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition							Į				
Pin Name Factor (lu)  OT 2  Output Driving Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition											
OT 2  Pin Name Cutput Driving Factor (Lu)  * Minimum values for the typical operating condition The values for the worst case operating condition							ļ				
Pin Name Output Driving Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition											
Pin Name Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition	OT	2									
Pin Name Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition											
Pin Name Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition			t				- 1				
Pin Name Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition											
Pin Name Factor (lu)  * Minimum values for the typical operating condition The values for the worst case operating condition							- 1				
* Minimum values for the typical operating condition The values for the worst case operating condition											
The values for the worst case operating condition	Pin Name	Factor (lu)									
The values for the worst case operating condition											
The values for the worst case operating condition		1									
are given by the maximum delay multiplier.											
		1	are	given b	y the ma	ximum d	ela	y mu	ltip	11	er.

Note: 1. The unit of  $K_{\rm CL}$  is ns/pF.

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

	CMOS GATE ARRAY U	NIT CELL	SPECI	FICATION	Ŋ				Version
Cell Name	Function							Νι	umber of BC
04TF	Tri-state Output	Buffer	(IOL=8	mA, Tru	e)				6
Cell Symbol				agation	Delay P		r		
		tuj			tdn				
		1.21	KCL 0.047	t0 2.09	KCL 0.052	KCL2	CDR	2	Path OT → X
		(4.27)	0.047	(5.47)				- 1	01 <del>7</del> X
		(4.27)		(3.47)	Ί Ι			I	
								- 1	
	_			}				- 1	
OTT	,,							- 1	
от —	x			İ				- 1	
	C			l				- 1	
		<u> </u>		<u></u>	<u> </u>		L	_	
		t0	L + Z	KCL	t0	$Z \rightarrow L$	CL	-	C → X
		2.55		KOL	2.32		054	$\neg$	U , A
		(15.20		*	(5.83				
								- 1	
	<del></del>								
Pin Name	Input Loading Factor (lu)								
OT	Factor (ku)	1							
Č	2		H → Z	3		$Z \rightarrow H$		$\neg$	
		t0		KCL	t0		CL		
		3.56			1.37		048		
Die Nee	Output Driving	(15.20	)	*	(5.83	)			
Pin Name	Factor (lu)	-							
		1	- 1						
			- 1						
	1	1							





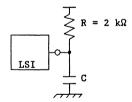
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

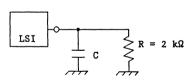
Note: 1. The unit of  $K_{\mbox{CL}}$  is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-04TF-E2 Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	1		"A	U" Version
Cell Name	Function				<del></del>		Ī	Number of BC
	Tri-state Output	Buffer	(IOL=8	mA, True	∍)			
O4RF	with Noise Limit	Resist			-			5
Cell Symbol			Prop	agation	Delay Pa	ramete	r	
			up	<u> </u>	tdn			
		t0	KCL	t0	KCL	KCL2	CDR	
		3.42	0.047	7.64				OT → X
		(6.48)		(11.28)	)			1
				1	1			
				<b>,</b>	1 1			1
	$\sim$				1 1			-
от	x			İ	1 1			ł
01	<b>⋄</b>			1	1 1			ł
				}	1 1			1
	i			ļ	1			İ
	С				1 1			<b>!</b>
	-							
		· · · · · · · · · · · · · · · · · · ·	L + 2	Ż		$Z \rightarrow L$		
		t0		KCL	t0	K	CL	c → x
		2.6	9		7.72	0.	056	
		(15.3	7)	*	(11.36)			
			- 1			- 1		i
			- 1					1
	Input Loading		ļ	1				1
Pin Name	Factor (lu)		1					
OT	2			<del>,</del>				
С	2		H → 2			Z → H	-	
		t0 2.9		KCL	t0 3.58		CL	
	Output Driving	(15.3	-	*	(11.36)		047	
Pin Name	Factor (lu)	(13.3	"	"	(11.30)			1
IIII Name	ractor (ku)		- 1					
			1			1		
			[			- 1		
	i .	l .						





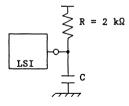
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

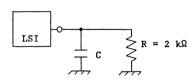
Note: 1. The unit of KCL is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-04RF-E1 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	٧		"A		Version
Cell Name	Function							N	umber of BC
H6TF	Tri-state Output	& Inpu							10
Cell Symbol				agation	Delay Pa	ramete	r		
			up		tdn			_	
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.85	0.03	1.47	0.03		İ	Ì	X → IN
		1.21	0.047	2.09	0.052		ł	- 1	$OT \rightarrow X$
	1	(5.21)		(6.51)	ן ו'			- 1	
IN ——	<b>-</b> < h ∣				1 1			- 1	
	N 71						1	- {	
от —	<b>X</b>		į		]				
<b>.</b>	Λ " I			1			1		
					1 1		ł	- 1	
	ı							- 1	
	C				1				
			L → 2			$Z \rightarrow L$			
		t0		KCL	t0		CL	_	C → X
		2.5			2.32		054		
		(19.1	0)	*	(6.91)	)		Į	
			ļ						
	Input Loading		l			- 1			
Pin Name	Factor (lu)	ŀ	- 1						
OT	6	1							
C	2		H → 2	2		Z + H			
	1	t0		KCL	t0	K	CL		
		3.5	6		1.37	0.	048		,
	Output Driving	(19.1	0)	*	(6.91)	) [			
Pin Name	Factor (lu)		ł						
IN	36		j						
		1	1						
	1	1		1					

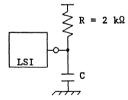


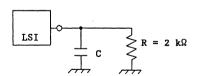


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6TF-E2 Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPEC	FICATION	1	·	"A	U"	Version
Cell Name	Function							Nı	umber of B
	Tri-state Output	& Inpu	t Buffe	er (IOL=8	BmA, Tru	e)			
H6TFU	with Pull-up Res	istance							10
Cell Symbol			Prop	pagation	Delay P	aramete	r		
		t	up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.85	0.03	1.47	0.03				X → IN
		1.21	0.047	2.09	0.052			- 1	$OT \rightarrow X$
		(5.21)		(6.51)	)			- 1	
IN					1 1		l	- 1	
TIN							1	- 1	
								- 1	
от —	> <b>→</b> x			1	1		1	- 1	
				1			Ì	- 1	
				1			1	- 1	
	ı			1			1	- 1	
	C			}				- 1	
				1					
			L → 2			$Z \rightarrow L$			
		t0		KCL	t0		CL		$C \rightarrow X$
	,	2.5	5		2.32	0.	054		
		(19.1	0)	*	(6.91	)		ı	
						`			
			1			- 1		Į	
	Input Loading			į		-			
Pin Name	Factor (lu)								
OT	6								
С	2		H → 2	Z		$Z \rightarrow H$			
		t0		KCL	t0		CL		
		3.5	6		1.37	0.	048		
	Output Driving	(19.1	.0)	*	(6.91	)		- 1	
Pin Name	Factor (lu)	l						- 1	
IN	36	1	- 1			- 1		- 1	
			l			1		- 1	
			- 1	į		1			
	1	l	į.			1			

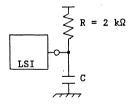


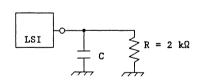


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H6TFU-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPEC	CIFICATION	N			u"	
Cell Name	Function							Z	umber of BC
	Tri-state Output	& Inpu	t Buff	fer (IOL=	BmA, Tru	e)			
H6TFD	with Pull-down R	esistan						L	10
Cell Symbol			Pro	opagation			r		
			up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.85	0.03	_					$X \rightarrow IN$
		1.21	0.047						$OT \rightarrow X$
	1	(5.21)		(6.51	)				
IN	<b>-</b> <- \f		ĺ	]					
				1					
OT	x						İ	- 1	
	ΓY			1				- 1	
	-		ľ	1			l	- 1	
•	С			İ	İ				
			L	i	<u> </u>	L		_	
			L →			$Z \rightarrow L$			
		t0		KCL	t0		CL		C → X
		2.5		*	2.32	1	054	- }	
		(19.1	0)	ж	(6.91	)			
ı			- 1	į					
	T		-						
Dia Nama	Input Loading			1		1			
Pin Name OT	Factor (lu)	1							
C	6 2	<b></b>	H →	7		$Z \rightarrow H$			
·	2	to	n →	KCL	+0		CL		
	1	3.5	4	VOT	t0 1.37		048		
	Output Driving	(19.1		75	(6.91		040		
Pin Name	Factor (lu)	(19.1	٠,		(0.91	'		l	
IN IN	36	1	1						
111	] 30		i						
	I		1						





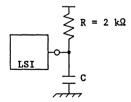
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

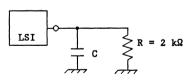
Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H6TFD-E2 | Sheet 1/1

FILITSII	CMOS GATE ARRAY U	NIT CEL	r corc	TETCATIO	N			U"	Version
Cell Name	Function	NII CEL	L SFEC	IFICALIO			1-7		umber of BC
	Tri-state Output	& CMOS	Inter	face Inn	ut Buffe	r			AMBEL OF BO
H6CF	(IOL=8mA, True)	G 0110D	111001	race imp	Dallo	•			8
Cell Symbol	, , , , , , , , , , , , , , , , , , , ,		Pro	pagation	Delay P	aramete	r	_	
		t	up	T-	tdn			7	
		t0	KCL	t0	KCL				Path
		0.74	0.03	1.07	0.03				X → IN
		2.39	0.047	4.30	0.051		l	- 1	$OT \rightarrow X$
	4	(6.39)		(8.64	)		ŀ	- 1	
IN	<b>-</b> √h							1	
	, 기				1		1	١	
					1		ł	- 1	
от —	x						1	I	
	ΓŢ I						İ	ı	
								- 1	
	c				ì				
	U				1			- 1	
			L →	7.	<u> </u>	$Z \rightarrow L$	L	-	<del></del>
		t0		KCL	t0		CL	$\dashv$	c → x
		2.6	3		3.93		.051	$\dashv$	
		(18.7		*	(8.27			- 1	
		(				1		-	
			- 1					- [	
	Input Loading		Ì						
Pin Name	Factor (lu)		1			1			
OT	4								
С	2		Н →			Z → H		_	
		t0		KCL	t0		CL	$\dashv$	
	Outros Dudasia	3.4		*	2.50		047	ı	
Pin Name	Output Driving Factor (lu)	(18.7	ا (2	•	(8.27	'		ı	
IN IN	36		1.					- 1	
714	30		-						
			}			1		1	
l	1		1			i		1	





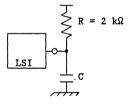
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

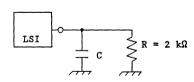
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

AU-H6CF-E1 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N N		T"AU	J" T	Versio	n.
Cell Name	Function								oer of	
	Tri-state Output	& CMOS	Inter	face Inp	ut Buffer	:				
H6CFU	with Pull-up Res	istance	(IOL=	BmA. Tru	e)		ł		8	
Cell Symbol					Delay Pa	ramete	r			
		t	up	T	tdn			1		
		t0	KCL	t0	KCL	KCL2	CDR	2	Path	
İ		0.74	0.03	1.07	0.03				X + I	N
		2.39	0.047	4.30	0.051			- 1	X ← TC	
		(6.39)		(8.64	)			-		
IN —		<u> </u>			i l					
IN	$\sim$ $\sim$ $\sim$			1	1 1					
					1			1		
OT	x -			1	1 1					
	M				1 1			-		
					1 1					
	1 ,				1 1			1		
	С	1			1		l			
							L			
			L →			$Z \rightarrow L$		_		
		t0		KCL	t0		CL	_	C →	X
		2.6			3.93		.051	-		
		(18.7	2)	ric	(8.27)	)				
			}			-				
	<del></del>		i							
	Input Loading		j			1				
Pin Name	Factor (lu)	1	1			1				
OT	4	ļ						4		
С	2		Η →			$Z \rightarrow H$		-		
		t0		KCL	t0		CL	$\dashv$		
	Outros Dudas	3.4		*	2.50		047	1		
Din Nama	Output Driving	(18.7	4)	ж	(8.27)	'		1		
Pin Name IN	Factor (lu)	{	1					ı		
TIM	30	1				1		-		
		1	1			1				
			1			1		-		
	1	1	í			1		1		





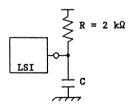
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

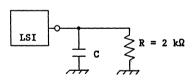
Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

AU-H6CFU-E1 | Sheet 1/1

FILITSII	CMOS GATE ARRAY U	NIT CET	T CDEC	TETCATION	<del>,</del>		T"AU	" Version	
Cell Name	Function	MII CED	L SPEC	IFICALION	<u> </u>			Number of BC	
OCII MUMO	Tri-state Output	& CMOS	Inter	face Inn	t Buffe			Number of bo	
H6CFD	with Pull-down R					•	1	8	
Cell Symbol	WION I GIII GOWN N	esistan		pagation		aramoto	<del></del>		
GGII DJEEGI		+	up	Pagacion	tdn		-	T	
İ		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		0.74	0.03	1.07			1 32.00	X + IN	
		2.39	0.047		0.051		1	OT → X	
		(6.39)		(8.64)			l	"	
		(0.0)		(0.0.)	1		1		
IN —				1			l		
I	N 1	l	ŀ	1			ļ		
от	> <b>→</b> x		1	1			l		
	7	l	1	1					
į			l	1			l		
į	1								
	С		l	1		1	ì		
l	•	l	Ì	1		1	į		
			L +	Z		$Z \rightarrow L$	·		
		to		KCL	t0		CL	c → x	
		2.6	3		3.93	(	0.051	7	
1		(18.7	2)	*	(8.27	)		ì	
		<b>'</b>			•	<b>^</b>		1	
			- 1			- 1		1	
	Input Loading	]	1			- 1		1	
Pin Name	Factor (lu)	1	1			- 1		1	
OT	4	1	- 1			- 1			
C	2		H →	Z		$Z \rightarrow H$		7	
	1	t0	T	KCL	t0		KCL	7	
l		3.4	0		2.50	0.	.047	7	
	Output Driving	(18.7	(2)	*	(8.27	) [		1	
Pin Name	Factor (lu)	]	1					1	
IN	36	1	- 1					1	
l			- 1					1	
1	1		- 1					1	
	1		1					1	

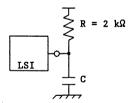


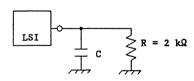


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

AU-H6CFD-E1 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	١		JA"	
Cell Name	Function							Number of B
	Tri-state Output	with N	oise Li	mit Resi	istance			
H8TF	& Input Buffer (	IOL=8mA					1	9
Cell Symbol			Prop	agation	Delay Pa	aramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR	2 Path
		0.85	0.03	1.47	0.03			X + IN
		3.42	0.047	7.64	0.056			OT → X
	4	(7.42)		(12.40)	ol i			
IN					1 1			
IN	$\sim$			1				
					1 1			1
от —	<b>X</b>							
	<b>▶</b>				1 1			
				1	1			
	l l							
	C			1	1 1			
	-			Į.	1 1			
			$L \rightarrow 2$			$Z \rightarrow L$		
		t0		KCL	t0	K	CL	C → X
		2.6	9		7.72	0.	056	
		(19.6	9)	*	(12.48)	)		
		(2)	~	ļ	(	´		
		1		- 1				ŀ
	Input Loading	1		}				1
Pin Name	Factor (lu)	l		l		i		
OT	2	i		1		l		1
Č	2		H → Z			Z → H		-
•	1 -	t0	<del></del>	KCL	t0		CL	-
	!	2.9	0		3.58		047	-1
	Output Driving	(19.6		*	(12.48			1
Pin Name	Factor (lu)	`	7		(22.40	´		
IN	36	1	l					1
		1	- 1					1
	}		l					ı
	1		- 1					l





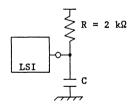
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

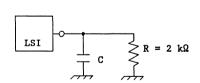
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8TF-E1 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CEL	I. SPEC	IFICATIO	N .		"Al	J" Version
	Function	MII ODD	D OLDO	11 1011110			<del>- "</del>	Number of BC
	Tri-state Output	with N	oise I	imit Res	istance			
H8TFU	& Input Buffer(I	OL=8mA,	True)	with Pu	11-up Re	sistano	:е	9
Cell Symbol				pagation				
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR	
		0.85	0.03	1.47				X → IN
1		3.42	0.047				1	OT → X
	4	(7.42)		(12.40)	)		1	1
IN —	-<- h			1	1		l	
	\ \ \			l	1			
077					1			
OT -	x							
,	<b>_</b>			l	1			
				1	1			
	C			1				
	C				1		l	
1			L →	7		$Z \rightarrow L$	1	
		t0	<u> </u>	KCL	t0		CL	⊢ c → x
	•	2.6	9	NOD	7.72		056	-
		(19.6		*	(12.48			
1		(27.1	7		(	<b>'</b>		
						1		
	Input Loading					1		
Pin Name	Factor (lu)							
TO	2							
С	2		Η →			$Z \rightarrow H$		
		t0		KCL	t0		CL	
		2.9	-		3.58		.047	
l	Output Driving	(19.6	9)	*	(12.48	(i)		
Pin Name	Factor (lu)	l	1					
IN	36					l		
						ł		
		1				- 1		
I	į.	ı	- 1			1		ı

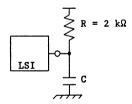


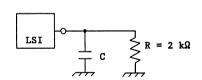


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8TFU-E1 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPE	CIFIC	ATION			"A	U"		
Cell Name	Function								Νι	umber of	BC
	Tri-state Output	with N	oise :	Limit	Resi	stance					
H8TFD	& Input Buffer(I	OL=8mA,								9	
Cell Symbol				opaga	tion	Delay P		r			
			up			tdn					
		t0	KCL		t0	KCL	KCL2	CDR	2	Path	
		0.85	0.03		1.47				١	X + II	
		3.42	0.04		7.64	0.056			ı	$OT \rightarrow X$	
	1	(7.42)		(1	2.40)				- 1		
IN	<b></b> < h ∣			- 1					l		
	_ 7										
om				- 1					- 1		
от —	x +			1					- 1		
	νĭ			- 1					- 1		
				ł					- 1		
	,							l	- 1		
	С			- 1					ļ		
					—т	L	$Z \rightarrow L$	L			
		t0	L →	KCI		t0		CL		C → :	<b>y</b>
		2.6	<u>a</u>	KOL		7.72		056	_		••
		(19.6	- 1	*		(12.48		050			
		(17.0	"			(12.40	<b>'</b>				
					- 1						
	Input Loading										
Pin Name	Factor (lu)				į		1				
OT	2		- 1		1						
C	2		H →	· Z			$Z \rightarrow H$				
_		t0		KCI		t0	T I	CL			
		2.9	0			3.58		047			
	Output Driving	(19.6	9)	*	ı	(12.48	)				
Pin Name	Factor (lu)	`				-					
IN	36	1	1								
			l						Ì		
	1	İ	- 1		-		- 1				





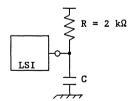
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

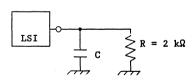
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8TFD-E1	Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N N		"AU	Wersion
Cell Name	Function					·		Number of BC
	Tri-state Output	Buffer	with	Noise Li	mit Resi	stance		
H8CF	& CMOS Interface	Input	Buffer	(IOL=8m	A, True)		- 1	9
Cell Symbol				pagation		aramete	r	
		t	up	T	tdn			1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.74	0.03	1.07	0.03			X → IN
		3.42	0.047	7.64	0.056			OT → X
	4	(7.42)		(12.40	)			
IN	<u> </u>			1	1			
114	$\sim$							
от —	<b>x</b>			1			1	
	M							
				1				į
	1						1	l
	С			1	į.		1	i
			L →			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		2.6	9		7.72		0.056	
		(19.6	9)	*	(12.48	)		1
			}					ì
			- 1			1		1
	Input Loading		1					
Pin Name	Factor (lu)					- 1		1
OT	2							
C	2		Η →	Z		Z → H		
		t0		KCL	t0		CL	
		2.9	-		3.58		047	
	Output Driving	(19.6	9)	*	(12.48	)		
Pin Name	Factor (lu)		ı			- 1		
IN	36	1	1			- 1		
			1			- 1		1
	1				l	- 1		1

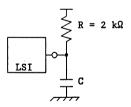


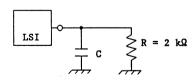


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\text{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

AU-H8CF-E1 | Sheet 1/1

FUJITSU	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version											
	Function	000	<u> </u>				Ť	Number of BC				
	Tri-state Output	Buffer	w/ Nois	e Limit	Resista	nce						
	& CMOS Interface	Input B	uffer(I	OL=8mA.	True)							
H8CFU	w/ Pull-up Resist	ance	- , -	,	,			9				
Cell Symbol	L		Prop	agation	Delay P	aramete	r					
		t	up		tdn							
		t0	KCL	t0	KCL	KCL2	CDR	2 Path				
		0.74	0.03	1.07	0.03			X → IN				
		3.42	0.047	7.64	0.056			OT → X				
	4	(7.42)		(12.40)								
IN	<b>─</b> ✓ Ь											
OT — X												
				1								
				ļ								
	С			l			1					
				<u> </u>								
			$L \rightarrow Z$			$Z \rightarrow L$		_				
		t0		KCL	t0		CL	C → X				
		2.6			7.72		0.056					
		(19.6	9)	*	(12.48	)						
				ŀ		- 1		1				
	Input Loading			1		1						
Pin Name	Factor (lu)					-		İ				
OT	2							_				
С	2	<u> </u>	H → Z			Z → H		4				
	į	t0		KCL	t0		CL	_				
	<del> </del>	2.9		*	3.58		047					
D:- N	Output Driving	(19.6	9)	*	(12.48	,		1				
Pin Name IN	Factor (lu)		ļ	1								
IN	36			i				1				
i						- 1		-				
				l		-						
		L	1			1						





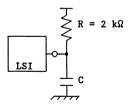
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

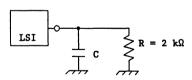
Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8CFU-E1 | Sheet 1/1

FUJITSU	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AU" Version											
Cell Name	Function				<u>`                                      </u>			Number of BC				
	Tri-state Output	Buffer	w/ Nois	e Limit	Resista	nce						
	& CMOS Interface		uffer(1	OL=8mA,	True)							
H8CFD	w/ Pull-down Resi	stance						9				
Cell Symbo	l			agation			r					
			up	1	tdn KCL	KCL2	CDR2					
		t0 0.74	KCL 0.03	1.07	0.03	KCLZ	CDRZ	Path X → IN				
	3.42	0.03	7.64	0.056		l	OT + X					
		(7.42)		(12.40)				01 7 %				
		(,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		(12.40)	Ί .							
IN — I												
OT — X												
	-				1							
	С											
1		ļ	$L \rightarrow 2$	, ,	L	$Z \to L$						
		t0	<del> </del>	KCL	t0		CL	⊢ c → x				
		2.6	9		7.72		.056					
		(19.6	9)	*	(12.48	)						
		· .		]	-			,				
	Input Loading											
Pin Name	Factor (lu)	Į										
OT C	2 2		H → 2	,		Z → H		_				
'	. 2	to	_ <del>n → '</del>	KCL	t0		CL					
1		2.9	0	KCT	3.58		047	-				
	Output Driving	(19.6		*	(12.48							
Pin Name	Factor (lu)	`	- /		(==:-0	1						
IN	36	1										
		1										
l			-			- 1						
		L										





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

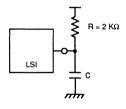
AU-H8CFD-E1 | Sheet 1/1

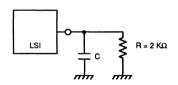
FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION			<i>" AU "</i> \	/ers	ion
Cell Name	Function									Number of BC
02S2	Output Buffer (IC with Noise Limit	DL=24m Resista	nA, True ince	<del>)</del>						3
Cell	l Symbol			Pro	pagation D	elay Pa	ram	eter		
			ıp			dn				Path
		3.60	KCL 0.024	7.69	0.041	KCL	2	CDR2		OT to X
		(5.04)		(10.15)						
от	x									
		Paramete	er				S	ymbol		Typ (ns) *
						İ				
						1				
									1	
	Input Loading									
Pin Name	Factor (lu)					ł				
ОТ	2								l	
						l			l	
	Output Driving					1				
Pin Name	Factor (Iu)					İ				
ļ		* Minimu	m values fo	r the typical	loperating	conditio	n.			
		The val	ues for the					given by th	e ma	aximum delay
		multiplie	er. 							
Note: 1. The	e unit of KcL is ns/pF.									
	tput load capacitance	of 60 pFi	s used fo	r Fuiitsu's	s logic sin	nulatio	n.			
1	e parameters in parent									
0	c parameters in parent	noses an	t the vale	ics applic	u to the s	milaia		•		

AU-02S2-E1

Sheet 1/1

FUJIT	SU CMOS GATE AR	TINU YAF	CELL S	PECIFICA	ATION		" AU "\	
Cell Name	Function							Number of BC
O4S2	Tri-state Outpu with Noise Lim			4mA, Tr	rue)			4
Cell	Symbol			Proj	ameter			
		tı				dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
от —	×	3.60 (5.16)	0.024	7.90 (10.56)	0.041			OT to X
	C		L to Z			Z to L		a :
		t O		KCL	t O		KCL	C to X
		3.82 (18.72)	)	•	8.12 (10.85		0.042	
Pin Name	Input Loading Factor (lu)	]						
от	2 2				<b></b>			
С	2	10	H to Z	KCL	10	Z to F	KCL	
				KOL				
Pin Name	Output Driving Factor (lu)	6.43 (18.72		•	3.83 (10.85		0.024	

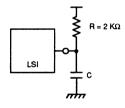


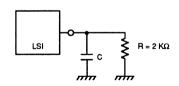


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL is ns/pF.
  - 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-O4S2-E1 Sheet 1/1

	ISU CMOS GATE AR	RAY UNIT	CEL	L SF	PECIFICA	ATION		" AU " V	
Cell Name	Function								Number of B
H8W2	Tri-state Outpo with Noise Lim	ut & Inpu it Resista	t Buf ance	ffer and	(IOL=2 d Input	4mA) Buffer (	TTL,	True)	8
Ce	II Symbol	1				pagation D			
		tu				Path			
		t O	KCI	L	t O	KCL	KCL	CDR2	
	1	0.85 3.60 (5.86)	0.0		1.47 7.90 (11.39)	0.03 0.041			X to IN OT to X
ot	×								
			L to	٥Z			Z to		
		t 0			KCL	10		KCL	C to X
		3.82 (22.50			*	8.12 (11.69		0.042	
Pin Name	Input Loading Factor (lu)	]							
οτ	2 2	<u></u>		o Z			Z to		
С	2	10	H 1		KCL	10		KCL	
Pin Name	Output Driving Factor (lu)	6.43 (22.50			*	3.83 (11.69		0.024	
IN	36								





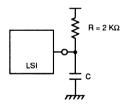
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

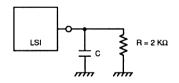
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

AU-H8W2-E1 Sheet 1/1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELI	_ SF	PECIFICA	ATION		Ť	" AU " \	ersion	
Cell Name	Function									. N	umber of BC
H8E2	Tri-state Outpu with Noise Limi						СМС	DS, T	rue)		8
Cel	l Symbol				Prop	pagation D	elay P	arame	ter		
		tup			tdn						Path
		t O	KCI	-	t 0	KCL	KCI	12	CDR2		
		0.74 3.60 (5.86)	0.0		1.07 7.90 (11.39)	0.03 0.041					to IN T to X
ot ——	×										
	C										
			L to	L to Z			Z t			_	
		10			KCL	t 0			KCL	C	to X
		3.82 (22.50)			•	8.12 (11.69)		0	.042		
Pin Name	Input Loading Factor (lu)										
OT C	2 2					ļ		D H			
C	4	t 0 KCL				10	210		KCL		
		<b></b>			NOL	<b></b>					
Pin Name	Output Driving Factor (lu)	6.43 (22.50			•	3.83 (11.69		0	.024		
IN	36										

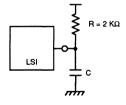


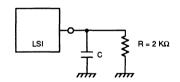


- (a) Measurement of tpd at LZ and ZL:
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8E2-E1 Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELL S	PECIFIC	ATION		" AU " \	/ersion		
Cell Name	Function							Number of BC		
H8W1	Tri-state Output with Noise Limit with Pull-up Res	Resistan				ſL, Tru	ıe)	8		
Ce	ell Symbol	T		Pro	pagation D	elay Para	meter			
		tup tdn								
		t O	KCL	t O	KCL	KCL2	CDR2	Path		
	1	0.85 3.60 (5.86)	0.03 0.024	1.47 7.90 (11.39)	0.03 0.041			X to IN OT to X		
от	×									
			L to Z		<u> </u>	Z to L		Q		
		3.82 (22.50)		*	8.12 (11.69	2	0.042	C to X		
Pin Name	Input Loading Factor (lu)	]								
от	2 2									
С	2	10	H to Z	KCL	10	Z to F	KCL			
		6.43		NUL	3.83		0.024			
Pin Name	Output Driving Factor (lu)	(22.50)	)	•	(11.69	))				
IN	36									
			- 1		1	- 1				

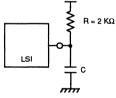


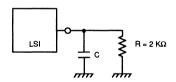


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8W1-E1 Sheet 1/1

	<u> ISU CMOS GATE AR</u>	RAY UNIT	CELLS	PECIFICA	ATION		" AU " Ve		
Cell Name	Function							Number of	
H8E1	Tri-state Output with Noise Limit with Pull-up Res	Resistan				MOS, T	rue)	8	
Ce	II Symbol			Proj	pagation D	elay Parar	neter		
		tup tdn							
		10	KCL	t O	KCL	KCL2	CDR2	Path	
	1	0.74 3.60 (5.86)	0.03 0.024	1.07 7.90 (11.39)	0.03 0.041			X to IN OT to X	
ot	×								
	· ·		L to Z			Z to L			
		10		KCL	10		KCL	C to X	
		3.82 (22.50		•	8.12 (11.69)		0.042		
Pin Name	Input Loading Factor (lu)	]							
OT C	2 2		H to Z		ļ	Z to H			
J	-	t O	102	KCL	10		KCL		
		6.43			3.83		0.024		
Pin Name	Output Driving Factor (lu)	(22.50		*	(11.69		0.024		
IN	36								
Measur	values are subject to e ement circuits of prop /L, HZ and ZH are as	agation de		ndition.					

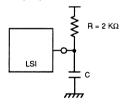


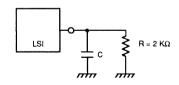


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8E1-E1 | Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELL S	SPECIFICA	ATION		" AU "\	/ersion
Cell Name	Function							Number of B
H8W0	Tri-state Output with Noise Limit I with Pull-down F	Resistan	ce and	(IOL=24r I Input Bu	nA) ⊔ffer (T⊓	L, Tru	e)	8
Ce	II Symbol							
		tu				in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
	4	0.85 3.60 (5.86)	0.03 0.024	1.47 7.90 (11.39)	0.03 0.041			X to IN OT to X
ОТ								
			L to Z			Z to L		
		3.82		KCL	8.12		KCL 0.042	C to X
		(22.50)		•	(11.69)		5.5.1	
Pin Name	Input Loading Factor (lu)	]						
от	2 2							
С	2	10	H to Z	KCL	to	Z to H	KCL	
		<del></del>		NOL				
Pin Name	Output Driving Factor (lu)	6.43 (22.50		•	3.83 (11.69		0.024	
IN	36							



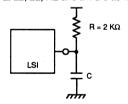


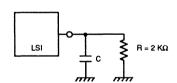
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8W0-E1 | Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELL	SP	ECIFICA	ATION		" AU " \	ersion
Cell Name	Function								Number of B
H8E0	Tri-state Output with Noise Limit I with Pull-down F	Resistan	ce ar				MOS,	True)	8
Ce	ell Symbol				Prop	pagation D	elay Pa	rameter	
		tı.	ıp				dn		Path
		t 0	KCL		t O	KCL	KCL	2 CDR2	raui
		0.74 3.60 (5.86)	0.03 0.02	24	1.07 7.90 (11.39)	0.03 0.041			X to IN OT to X
IN	$\preceq$								
от	×								
	· ·		L to	Z			Z to	L	
		t O			KCL	t 0		KCL	C to X
		3.82 (22.50			•	8.12 (11.69		0.042	
Pin Name	Input Loading Factor (lu)	]							
от	2 2	<u> </u>	H to				Z to	1.1	
С	2	10	H to		KCL	t O	- <u>/ 10</u>	KCL	
		6.43				3.83	, +	0.024	
Pin Name	Output Driving Factor (lu)	(22.50			•	(11.69		0.024	
IN	36	1							

\* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

AU-H8E0-E1 Sheet 1/1

# SINGLE-PORT RAM SPECIFICATION

## **FEATURES**

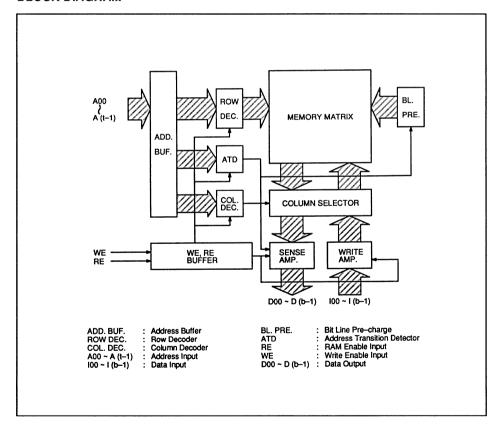
- · Configurable size
- Non-clocked static RAM
- 1 address 1 Read/Write port

# **SPECIFIC PARAMETERS**

Word size range: 4 to 2K words

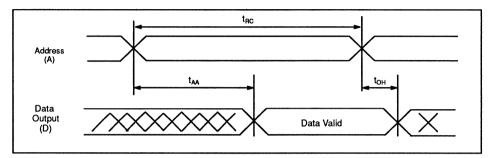
• Bit size range: 1 to 72 bits

# **BLOCK DIAGRAM**

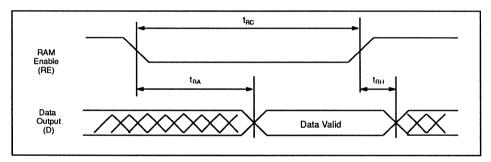


# **TIMING DIAGRAMS**

# READ CYCLE<sup>1</sup>



Read Cycle: Address Controlled<sup>2</sup>



Read Cycle: RE Controlled<sup>3</sup>

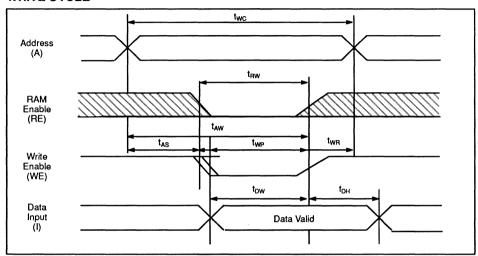
Notes: <sup>1</sup>WE is High for Read Cycle.

<sup>2</sup>RE is Low for Address Controlled Read Cycle.

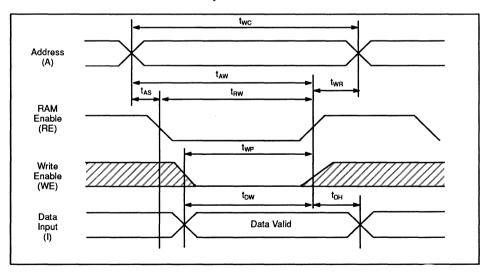
<sup>3</sup>Address must be valid prior to or coincident with RE transition Low.

# TIMING DIAGRAMS (Continued)

## WRITE CYCLE<sup>1</sup>



Write cycle: WE Controlled<sup>2</sup>



Write cycle: RE Controlled3

Notes: <sup>1</sup>The Data Output (D) is invalid in the Write mode. <sup>2</sup>WE must be high during address transitions. <sup>3</sup>RE must be high during address transitions.

# **CELL SYMBOL AND CELL SPECIFICATION**

FUJIT	SU CMOS GATE ARRAY	UNIT CEL	L SPECI	FICATION	V			A	U Version
Cell Name	Function							$\Box$	Number of BC
RAMxx	Single Port SRAM (w	word x b	bit)						1
Cell Symb	ool			Propaga	tion Delay	/ Parar	neter		
		tı	h		tı	dn			Path
101	D01	to	K <sub>CL</sub>	to	K <sub>CL</sub>	K <sub>CL</sub>	<sub>2</sub> C <sub>1</sub>	OR2	raui
102 —	D02	٠	0.07	٠	0.04	0.07	7		$\begin{array}{c} A \rightarrow D \\ RE \rightarrow D \end{array}$
A00 =	. 🗼								
A (t-1)									
	Input Loading	Parameter Symb						bol	Typ (ns) **
Pin Name	Factor (lu)	Read C	ycle Time	)			. t <sub>RC</sub>		
A4*** 14***	1 1	Addres	s Access	Time			t <sub>AA</sub>		
WE RE	1	RAM E	nable Acc	ess Time			t <sub>RA</sub>		
	•	Output	Hold from	Address	Change		tон		
		Output	Hold from	RAM En	able Cha	nge	t <sub>RH</sub>		
		Write C	ycle Time	)			t <sub>WC</sub>		
		RAM E	nable to E	nd of Wr	ite		t <sub>RW</sub>		
		Addres	s Valid to	End of W	rite		t <sub>AW</sub>		
Pin Name	Output Driving Factor (Iu)		s Setup ti				tas		
Fill Name	ractor (Iu)	Write P	ulse Widt	h 			t <sub>WP</sub>		
D4***	36	Data S	etup Time				t <sub>DW</sub>		
			ecovery	Time			t <sub>WR</sub>		
			old Time				t <sub>DH</sub>		L
		**	pages. Minimum The value the maxim The value are given on the foll Pin Name	values for s for the value delay indicate in the Recowing page	r the typic worst case multiplied and here de ad Mode ges.	al oper e opera r. epend o and Wi	rating co ating co on bit-w rite Mod	ondition ord o	on the following ion. on are given by organization and alay Time Tables and with two char-

# **BASIC DELAY TIME**

### Read Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t <sub>RC</sub>	Read Cycle Time	c=1: 0.0024*w + 0.0044*b + 21.07 c=2: 0.0010*w + 0.0110*b + 21.10 c=4: 0.0006*w + 0.0176*b + 21.12 c=8: 0.0003*w + 0.0341*b + 21.02	ns
t <sub>AA</sub>	Address Access Time	c=1: 0.0024*w + 0.0044*b + 20.14 c=2: 0.0010*w + 0.0110*b + 20.30 c=4: 0.0006*w + 0.0176*b + 20.36 c=8: 0.0003*w + 0.0341*b + 20.36	ns
t <sub>RA</sub>	RAM Enable Access Time	c=1: 0.0051*w + 0.0140*b + 18.29 c=2: 0.0006*w + 0.0077*b + 19.49 c=4: 0.0003*w + 0.0143*b + 19.49 c=8: 0.0002*w + 0.0286*b + 19.55	ns
t <sub>OH</sub>	Output Hold from Address Change	c = 1: 0.0018 * w + 0.0140 * b + 5.38 c = 2: 0.0009 * w + 0.0286 * b + 5.38 c = 4: 0.0004 * w + 0.0572 * b + 5.38 c = 8: 0.0002 * w + 0.1140 * b + 5.38	ns
t <sub>RH</sub>	Output Hold from RAM Enable Change	c = 1:       0.0010 * b + 2.84         c = 2:       0.0020 * b + 2.84         c = 4:       0.0040 * b + 2.84         c = 8:       0.0079 * b + 2.84	ns

### Example

To find the delay time for the read-mode parameters for a single-port RAM of 512 words, 16 bits, and c = 4:

```
\begin{array}{lll} t_{RC} & = & 0.0006 \, ^*w \, + \, 0.0176 \, ^*b \, + \, 21.12 \\ & = & 0.0006 \, ^*512 \, + \, 0.0176 \, ^*16 \, + \, 21.12 \\ & = & 21.71 \, \text{ns} \\ \\ t_{AA} & = & 0.0006 \, ^*w \, + \, 0.0176 \, ^*b \, + \, 20.36 \\ & = & 0.0006 \, ^*512 \, + \, 0.0176 \, ^*16 \, + \, 20.36 \\ & = & 20.95 \, \text{ns} \\ \\ t_{RA} & = & 0.0003 \, ^*w \, + \, 0.0143 \, ^*b \, + \, 19.49 \\ & = & 0.0003 \, ^*512 \, + \, 0.0143 \, ^*16 \, + \, 19.49 \\ & = & 19.87 \, \text{ns} \\ \\ t_{OH} & = & 0.0004 \, ^*w \, + \, 0.0572 \, ^*b \, + \, 5.38 \\ & = & 0.0004 \, ^*512 \, + \, 0.0572 \, ^*16 \, + \, 5.38 \\ & = & 6.50 \, \text{ns} \\ \\ t_{RH} & = & 0.0040 \, ^*b \, + \, 2.84 \\ & = & 0.0040 \, ^*16 \, + \, 2.84 \\ & = & 2.90 \, \text{ns} \\ \end{array}
```

## **BASIC DELAY TIME** (Continued)

#### Write Mode

Symbol	Parameter	Equation (Typical Value)	Unit
twc	Write Cycle Time	c = 1: 0.0024 * w + 0.0044 * b + 21.07 c = 2: 0.0010 * w + 0.0110 * b + 21.10 c = 4: 0.0006 * w + 0.0176 * b + 21.12 c = 8: 0.0003 * w + 0.0341 * b + 21.02	ns
t <sub>RW</sub>	RAM Enable to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 14.63 c = 2: 0.0010 * w + 0.0066 * b + 14.63 c = 4: 0.0006 * w + 0.0110 * b + 14.63 c = 8: 0.0003 * w + 0.0220 * b + 14.63	ns
t <sub>AW</sub>	Address Valid to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 17.93 c = 2: 0.0010 * w + 0.0066 * b + 17.93 c = 4: 0.0006 * w + 0.0110 * b + 17.93 c = 8: 0.0003 * w + 0.0220 * b + 17.93	ns
t <sub>AS</sub>	Address Setup Time	c = 1:     3.30       c = 2:     3.30       c = 4:     3.30       c = 8:     3.30	ns
t <sub>WP</sub>	Write Pulse Width	c = 1: 0.0070 * w + 0.0022 * b + 10.01 c = 2: 0.0035 * w + 0.0044 * b + 10.01 c = 4: 0.0018 * w + 0.0088 * b + 10.01 c = 8: 0.0009 * w + 0.0176 * b + 10.01	ns
t <sub>DW</sub>	Data Setup Time	c = 1: 0.0070 * w 8.38 c = 2: 0.0035 * w 8.38 c = 4: 0.0018 * w 8.38 c = 8: 0.0009 * w 8.38	ns
t <sub>wR</sub>	Write Recovery Time	c = 1: 0.0011 * b + 3.14 c = 2: 0.0044 * b + 3.14 c = 4: 0.0066 * b + 3.14 c = 8: 0.0121 * b + 3.14	ns
t <sub>DH</sub>	Data Hold Time	c = 1:       0.0094*b + 3.51         c = 2:       0.0187*b + 3.51         c = 4:       0.0374*b + 3.51         c = 8:       0.0748*b + 3.51	ns

#### Example

To find the delay time for the write-mode parameters for a single-port RAM of 512 words, 16 bits, and c=4:

```
t_{RC} = 0.0006 * w + 0.0176 * b + 21.12
                                                   t_{WP} = 0.00 * w + 0.0088 * b + 10.01
     = 0.0006 * 512 + 0.0176 * 16 + 21.12
                                                        = 0.0018 * 512 + 0.0088 * 16 + 10.01
     = 21.71 ns
                                                        = 11.07 ns
                                                   t_{DW} = 0.0018 * w + 8.38
t_{RW} = 0.0006 * w + 0.0110 * b + 14.63
     = 0.0006 * 512 + 0.0110 * 16 + 14.63
                                                        = 0.0018 * 512 + 8.38
     = 15.11 ns
                                                        = 9.30 ns
t_{AW} = 0.0006 * w + 0.0110 * b + 17.93
                                                   t_{WR} = 0.0066 * b + 3.14
     = 0.0006 * 512 + 0.0110 * 16 + 17.93
                                                        = 0.0066 * 16 + 3.14
     = 18.41 ns
                                                        = 3.25 ns
                                                   t_{DH} = 0.0347 * b + 3.51
t_{AW} = 3.30 \text{ ns}
                                                         = 0.0347 * 16 + 3.51
                                                        = 4.11 ns
```

### **DUAL-PORT RAM SPECIFICATION**

### **FEATURES**

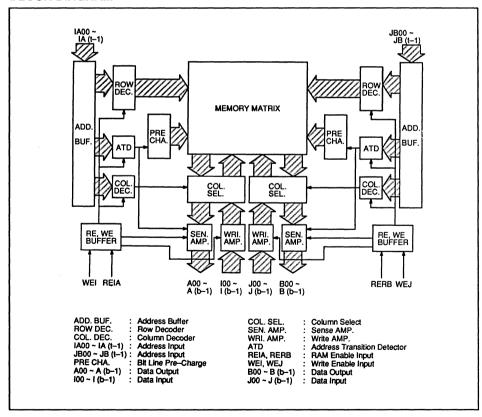
- Configurable size
- Non-clocked Static RAM
- 2 address 2 Read/Write port

#### SPECIFIC PARAMETERS

Word size range: 4 to 2K words

· Bit size range: 1 to 72 bits

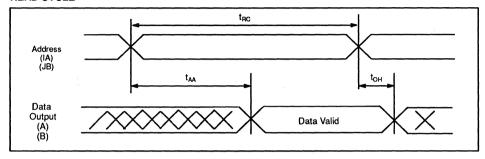
### **BLOCK DIAGRAM**



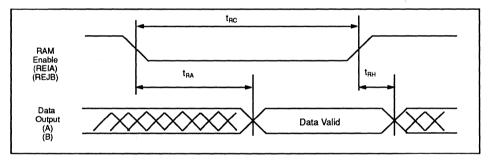
### **TIMING DIAGRAMS**

Only when both ports are in READ mode can one address be accessed by two ports in one cycle.

### **READ CYCLE<sup>1</sup>**



Read Cycle: Address Controlled<sup>2</sup>



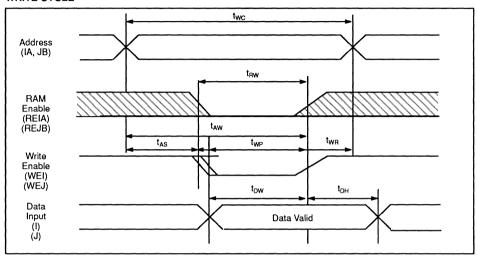
Read Cycle: RE Controlled<sup>3</sup>

Notes: ¹WE is High for Read Cycle.
2RE is Low for Address Controlled Read Cycle.

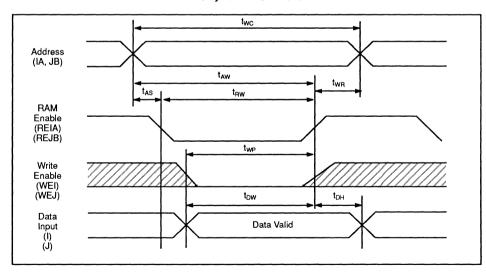
<sup>3</sup>Address must be valid prior to or coincident with RE transition Low.

## TIMING DIAGRAMS (Continued)

#### WRITE CYCLE<sup>1</sup>



Write cycle: WE Controlled<sup>2</sup>



Write cycle: RE Controlled3

Notes: <sup>1</sup>The Data Output (D) is invalid in the Write mode. <sup>2</sup>WE must be high during address transitions. <sup>3</sup>RE must be high during address transitions.

## **CELL SYMBOL AND CELL SPECIFICATION**

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION AU Version							U Version		
Cell Name	Cell Name Function						T	Number of BC	
RAMxx	DUAL Port Static RA	M (w word x b bit)						T	1
Cell Symb	ool			Propaga	tion Delay	/ Parar	neter		
J., J		tı	ıb		te	dn			D-4
	A00 A01	ţ	K <sub>CL</sub>	Ş	K <sub>CL</sub>	K <sub>CL</sub>	CDI	R2	Path
J(b-1) J00 J01 J(b-1) IA00 IA01 IA(1-1) JB00 JB01 JB(1-1) REIA REJB REJB WEJ WEJ WEJ	A (b-1) B800 B01 B (b-1)	•	0.07	•	0.04	0.07	7		A → A JB → B REIA →A REJB →B
	Input Loading		Paramet	er.	<u> </u>	L	Symt	hol	Typ (ns) **
Pin Name	Factor (lu)	Bead C	ycle Time				t <sub>RC</sub>		130 (110)
J***	1		s Access				t <sub>AA</sub>		
IA***	1	<del>-</del>					t <sub>RA</sub>		
JB*** RE	1	<del> </del>					tон		1
WE	1	Output	Hold fron	RAM En	able Cha	nge	t <sub>RH</sub>		
		Write Cycle Time two							
		RAM Enable to End of Write t <sub>RW</sub>							1
				End of W			t <sub>AW</sub>		
	Output Driving	Addres	s Setup ti	me			tas		
Pin Name	Factor (lu)	Write P	ulse Widt	h			t <sub>WP</sub>		
Α***	00	Data S	etup Time				t <sub>DW</sub>		
B***	36 36		ecovery				twR		
ļ		Data H	old Time				t <sub>DH</sub>		
		Refer to the Read Mode and Write Mode Tables on the following pages.      Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.      The values to be indicated here depend on bit-word organization and are given by the Read Mode and Write Mode Delay Time Tables on the following pages.      Pin Name  When b or t ≤ 10, these pin names are described with two characters: e.g., A9.				ion. on are given by vord organiza- Mode Delay			

### **BASIC DELAY TIME**

#### Read Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t <sub>RC</sub>	Read Cycle Time	c=1: 0.0024*w + 0.0044*b + 22.07 c=2: 0.0010*w + 0.0110*b + 22.10 c=4: 0.0006*w + 0.0176*b + 22.12 c=8: 0.0003*w + 0.0341*b + 22.02	ns
t <sub>AA</sub>	Address Access Time	c=1: 0.0024*w + 0.0044*b + 21.14 c=2: 0.0010*w + 0.0110*b + 21.30 c=4: 0.0006*w + 0.0176*b + 21.36 c=8: 0.0003*w + 0.0341*b + 21.36	ns
t <sub>RA</sub>	RAM Enable Access Time	c=1: 0.0051 * w + 0.0140 * b + 19.29 c=2: 0.0006 * w + 0.0077 * b + 20.49 c=4: 0.0003 * w + 0.0143 * b + 20.49 c=8: 0.0002 * w + 0.0286 * b + 20.55	ns
t <sub>OH</sub>	Output Hold from Address Change	c=1: 0.0018*w + 0.0140*b + 5.38 c=2: 0.0009*w + 0.0286*b + 5.38 c=4: 0.0004*w + 0.0572*b + 5.38 c=8: 0.0002*w + 0.1140*b + 5.38	ns
t <sub>RH</sub>	Output Hold from Ram Enable Change	c = 1:       0.0010 * b + 2.84         c = 2:       0.0020 * b + 2.84         c = 4:       0.0040 * b + 2.84         c = 8:       0.0079 * b + 2.84	ns

#### Example

To find the delay time for the write-mode parameters for a dual-port RAM of 512 words, 16 bits, and c = 4:

```
\begin{array}{lll} t_{RC} & = & 0.0006 \ ^*w + 0.0176 \ ^*b + 22.12 \\ & = & 0.0006 \ ^*512 + 0.0176 \ ^*16 + 22.12 \\ & = & 22.71 \ ns \\ \\ t_{AA} & = & 0.0006 \ ^*w + 0.0176 \ ^*b + 21.36 \\ & = & 0.0006 \ ^*512 + 0.0176 \ ^*16 + 21.36 \\ & = & 21.95 \ ns \\ \\ t_{RA} & = & 0.0003 \ ^*w + 0.0143 \ ^*b + 20.49 \\ & = & 0.0003 \ ^*512 + 0.0143 \ ^*16 + 20.49 \\ & = & 20.87 \ ns \\ \\ t_{OH} & = & 0.0004 \ ^*w + 0.0572 \ ^*b + 5.38 \\ & = & 0.0004 \ ^*512 + 0.0572 \ ^*16 + 5.38 \\ & = & 6.50 \ ns \\ \\ t_{RH} & = & 0.0040 \ ^*b + 2.84 \\ & = & 0.0040 \ ^*16 + 2.84 \\ & = & 2.90 \ ns \\ \end{array}
```

### **BASIC DELAY TIME (Continued)**

#### Write Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t <sub>wc</sub>	Write Cycle Time	c = 1: 0.0024 * w + 0.0044 * b + 22.07 c = 2: 0.0010 * w + 0.0110 * b + 22.10 c = 4: 0.0006 * w + 0.0176 * b + 22.12 c = 8: 0.0003 * w + 0.0341 * b + 22.02	ns
t <sub>RW</sub>	RAM Enable to End of Write	c = 1: 0.0024 *w + 0.0033 *b + 15.63 c = 2: 0.0010 *w + 0.0066 *b + 15.63 c = 4: 0.0006 *w + 0.0110 *b + 15.63 c = 8: 0.0003 *w + 0.0220 *b + 15.63	ns
t <sub>AW</sub>	Address Valid to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 18.93 c = 2: 0.0010 * w + 0.0066 * b + 18.93 c = 4: 0.0006 * w + 0.0110 * b + 18.93 c = 8: 0.0003 * w + 0.0220 * b + 18.93	ns
tas	Address Setup Time	c = 1:     3.30       c = 2:     3.30       c = 4:     3.30       c = 8:     3.30	ns
t <sub>WP</sub>	Write Pulse Width	c = 1: 0.0070 * w + 0.0022 * b + 11.01 c = 2: 0.0035 * w + 0.0044 * b + 11.01 c = 4: 0.0018 * w + 0.0088 * b + 11.01 c = 8: 0.0009 * w + 0.0176 * b + 11.01	ns
t <sub>DW</sub>	Data Setup Time	c = 1: 0.0070 * w 9.38 c = 2: 0.0035 * w 9.38 c = 4: 0.0018 * w 9.38 c = 8: 0.0009 * w 9.38	ns
t <sub>WR</sub>	Write Recovery Time	c = 1:     0.0011 * b + 3.14       c = 2:     0.0044 * b + 3.14       c = 4:     0.0066 * b + 3.14       c = 8:     0.0121 * b + 3.14	ns
t <sub>DH</sub>	Data Hold Time	c = 1:     0.0094 * b + 3.51       c = 2:     0.0187 * b + 3.51       c = 4:     0.0374 * b + 3.51       c = 8:     0.0748 * b + 3.51	ns

#### Example

To find the delay time for the write-mode parameters for a dual-port RAM of 512 words, 16 bits and c = 4:

```
t_{WC} = 0.0006 * w + 0.0176 * b + 22.12
                                                   t_{WP} = 0.0018 * w + 0.0088 * b + 11.01
     = 0.0006 * 512 + 0.0176 * 16 + 22.12
                                                         = 0.0018 * 512 + 0.0088 * 16 + 11.01
     = 22.71 ns
                                                         = 12.07 ns
t_{RW} = 0.0006 * w + 0.0110 * b + 15.63
                                                   t_{DW} = 0.0018 * w + 9.38
     = 0.0006 * 512 + 0.0110 * 16 + 15.63
                                                         = 0.0018 * 512 + 9.38
     = 16.11 ns
                                                         = 10.30 ns
t_{AW} = 0.0006 * w + 0.0110 * b + 18.93
                                                   t_{WR} = 0.0066 * b + 3.14
     = 0.0006 * 512 + 0.0110 * 16 + 18.93
                                                         = 0.0066 * 16 + 3.14
     = 19.41 ns
                                                         = 3.25 ns
                                                    t_{DH} = 0.0347 * b + 3.51
t_{AS} = 3.30 \, \text{ns}
                                                         = 0.0347 * 16 + 3.51
                                                         = 4.11 ns
```

## TRIPLE-PORT RAM SPECIFICATION

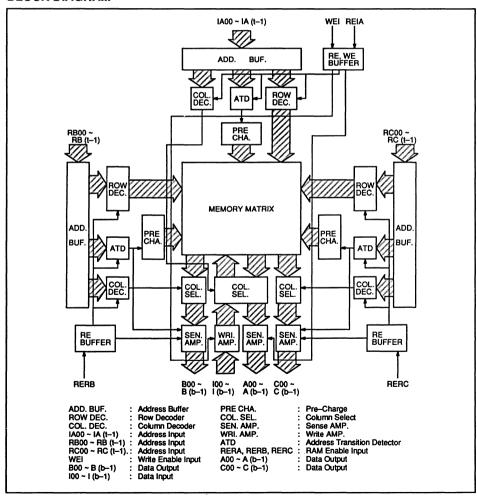
## **FEATURES**

- · Configurable word/bit organization
- Non-clocked static RAM
- 3 addresses 2 Read ports and 1 Read/Write port

#### SPECIFIC PARAMETERS

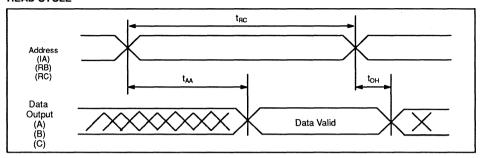
- Word size range: 4 to 2048 words
- · Bit size range: 2 to 72 bits
- Total bit size range: 64 to 18K bits

### **BLOCK DIAGRAM**

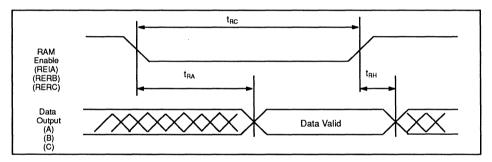


#### **TIMING DIAGRAMS**

### READ CYCLE<sup>1</sup>



Read Cycle: Address Controlled<sup>2</sup>



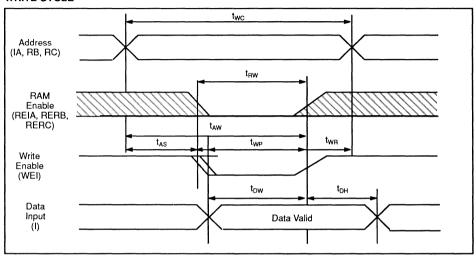
Read Cycle: RE Controlled<sup>3</sup>

Notes: <sup>1</sup>WEI is High for Read Cycle. <sup>2</sup>RE is Low for Address Controlled Read Cycle.

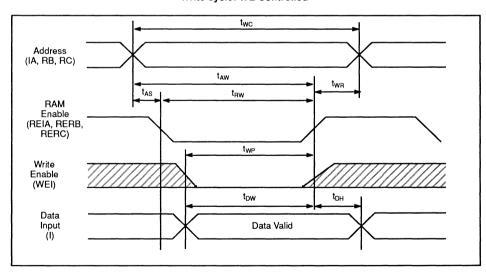
<sup>3</sup>Address must be valid prior to or coincident with RE transition Low.

### TIMING DIAGRAMS (Continued)

### WRITE CYCLE<sup>1</sup>



Write cycle: WE Controlled<sup>2</sup>



Write cycle: RE Controlled<sup>3</sup>

Notes: <sup>1</sup>The Data Output (A) is invalid in the Write mode. <sup>2</sup>WE must be high during address transitions. <sup>3</sup>RE must be high during address transitions.

## **CELL SYMBOL AND CELL SPECIFICATION**

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION AU Version							U Version		
Cell Name	Function							Number of BC	
RAMxx	RAMxx Triple Port Static RAM (			// (w word x b bit)					
Cell Symbo	ol			Propaga	tion Dela	/ Paran	neter		
I 100 —		tı	dr		t	dn		Path	
1 101 -	A01	ŧ <sub>o</sub>	K <sub>CL</sub>	to	K <sub>CL</sub>	K <sub>CL2</sub>	C <sub>DR2</sub>	1 441	
I (b-1)	A (b-1) B001 B (b-1) C C01 C (b-1)	•	0.07	٠	0.04	0.07	7	$\begin{array}{ccc} \text{IA} & \rightarrow & \text{A} \\ \text{RB} & \rightarrow & \text{B} \\ \text{RC} & \rightarrow & \text{C} \\ \text{REIA} & \rightarrow & \text{A} \\ \text{RERB} & \rightarrow & \text{B} \\ \text{RERC} & \rightarrow & \text{C} \end{array}$	
<u> </u>	Input Loading		Paramet	er	L	<u> </u>	Symbol	Typ (ns) **	
Pin Name	Factor (lu)	Read C	ycle Time	)	.,		t <sub>RC</sub>		
<sub>A</sub>	1	Address Access Time					t <sub>AA</sub>		
RB RC	1	RAM E	nable Acc	ess Time			t <sub>RA</sub>		
RE	į	Output	Hold from	Address	Change		tон		
WE	1	Output Hold from RAM Enable Change					t <sub>RH</sub>		
		Write C	ycle Time	)			twc		
] ]		RAM E	nable to	nd of Wr	ite		t <sub>RW</sub>		
		Addres	s Valid to	End of W	rite		t <sub>AW</sub>		
	Output Driving	Addres	s Setup ti	ne			t <sub>AS</sub>		
Pin Name	Factor (lu)	Write P	ulse Widt	h			t <sub>WP</sub>		
A	36	Data Se	etup Time	)			t <sub>DW</sub>		
BC	36	Write R	ecovery 7	Time			t <sub>WR</sub>		
	36		old Time				t <sub>DH</sub>	L	
		Refer to the Read Mode and Write Mode Tables on the following pages.      Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.      The values to be indicated here depend on bit-word organization and are given by the Read Mode and Write Mode Delay Time Tables on the following pages.      Pin Name  When b or t ≤ 10, these pin names are described with two characters: e.g., A9.							

### **BASIC DELAY TIME**

#### Read Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t <sub>RC</sub>	Read Cycle Time	c = 1: 0.0024 * w + 0.0044 * b + 22.27 c = 2: 0.0010 * w + 0.0110 * b + 22.30 c = 4: 0.0006 * w + 0.0176 * b + 22.32 c = 8: 0.0003 * w + 0.0341 * b + 22.22	ns
t <sub>AA</sub>	Address Access Time	c=1: 0.0024 * w + 0.0044 * b + 21.34 c=2: 0.0010 * w + 0.0110 * b + 21.50 c=4: 0.0006 * w + 0.0176 * b + 21.56 c=8: 0.0003 * w + 0.0341 * b + 21.56	ns
t <sub>RA</sub>	RAM Enable Access Time	c = 1: 0.0051 * w + 0.0140 * b + 19.44 c = 2: 0.0006 * w + 0.0077 * b + 20.69 c = 4: 0.0003 * w + 0.0143 * b + 20.69 c = 8: 0.0002 * w + 0.0286 * b + 20.75	ns
t <sub>он</sub>	Output Hold from Address Change	c = 1: 0.0018 * w + 0.0140 * b + 5.38 c = 2: 0.0009 * w + 0.0286 * b + 5.38 c = 4: 0.0004 * w + 0.0572 * b + 5.38 c = 8: 0.0002 * w + 0.1140 * b + 5.38	ns
t <sub>RH</sub>	Output Hold from RAM Enable Change	c = 1:       0.0010 * b + 2.84         c = 2:       0.0020 * b + 2.84         c = 4:       0.0040 * b + 2.84         c = 8:       0.0079 * b + 2.84	ns

### Example

To find the delay time for the write-mode parameters for a triple-port RAM of 512 words, 16 bits, and c = 4:

```
\begin{array}{lll} t_{RC} & = & 0.0006 * w + 0.0176 * b + 22.32 \\ & = & 0.0006 * 512 + 0.0176 * 16 + 22.32 \\ & = & 22.91 \ ns \ (typ) \\ \\ t_{AA} & = & 0.0006 * w + 0.0176 * b + 21.56 \\ & = & 0.0006 * 512 + 0.0176 * 16 + 21.56 \\ & = & 22.15 \ ns \ (typ) \\ \\ t_{RA} & = & 0.0003 * w + 0.0143 * b + 20.69 \\ & = & 0.0003 * 512 + 0.0143 * 16 + 20.69 \\ & = & 21.08 \ ns \ (typ) \\ \\ t_{OH} & = & 0.0004 * w + 0.0572 * b + 5.38 \\ & = & 0.0004 * 512 + 0.0572 * 16 + 5.38 \\ & = & 0.50 \ ns \ (typ) \\ \\ t_{RH} & = & 0.0040 * b + 2.84 \\ & = & 0.0040 * 16 + 2.84 \\ & = & 2.91 \ ns \ (typ) \\ \end{array}
```

### **BASIC DELAY TIME (Continued)**

#### Write Mode

Symbol	Parameter	Equation (Typical Value)	Unit
twc	Write Cycle Time	c=1: 0.0024*w + 0.0044*b + 22.27 c=2: 0.0010*w + 0.0110*b + 22.30 c=4: 0.0006*w + 0.0176*b + 22.32 c=8: 0.0003*w + 0.0341*b + 22.22	
t <sub>RW</sub>	RAM Enable to End of Write	c=1: 0.0024*w + 0.0033*b + 15.63 c=2: 0.0010*w + 0.0066*b + 15.63 c=4: 0.0006*w + 0.0110*b + 15.63 c=8: 0.0003*w + 0.0220*b + 15.63	ns
t <sub>AW</sub>	Address Valid to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 18.93 c = 2: 0.0010 * w + 0.0066 * b + 18.93 c = 4: 0.0006 * w + 0.0110 * b + 18.93 c = 8: 0.0003 * w + 0.0220 * b + 18.93	ns
t <sub>AS</sub>	Address Setup Time	c = 1:     3.30       c = 2:     3.30       c = 4:     3.30       c = 8:     3.30	ns
t <sub>WP</sub>	Write Pulse Width	c = 1: 0.0070 * w + 0.0022 * b + 11.01 c = 2: 0.0035 * w + 0.0044 * b + 11.01 c = 4: 0.0018 * w + 0.0088 * b + 11.01 c = 8: 0.0009 * w + 0.0176 * b + 11.01	ns
t <sub>DW</sub>	Data Setup Time	c = 1: 0.0070 * w 9.38 c = 2: 0.0035 * w 9.38 c = 4: 0.0018 * w 9.38 c = 8: 0.0009 * w 9.38	ns
t <sub>WR</sub>	Write Recovery Time	c = 1:     0.0011 * b + 3.34       c = 2:     0.0044 * b + 3.34       c = 4:     0.0066 * b + 3.34       c = 8:     0.0121 * b + 3.34	ns
t <sub>DH</sub>	Data Hold Time	c = 1:       0.0094 * b + 3.51         c = 2:       0.0187 * b + 3.51         c = 4:       0.0374 * b + 3.51         c = 8:       0.0748 * b + 3.51	ns

#### Example

To find the delay time for the write-mode parameters for a triple-port RAM of 512 words, 16 bits and c = 4:

```
t_{WC} = 0.0006 * w + 0.0176 * b + 22.32
                                                     t_{WP} = 0.0018 * w + 0.0088 * b + 11.01
     = 0.0006 * 512 + 0.0176 * 16 + 22.32
                                                           = 0.0018 * 512 + 0.0088 * 16 + 11.01
     = 22.91 ns (typ)
                                                          = 12.08 \text{ ns (typ)}
                                                     t_{DW} = 0.0018 * w + 9.38
t_{RW} = 0.0006 * w + 0.0110 * b + 15.63
                                                           = 0.0018 * 512 + 9.38
     = 0.0006 * 512 + 0.0110 * 16 + 15.63
     = 16.12 ns (typ)
                                                          = 10.31 ns (typ)
t_{AW} = 0.0006 * w + 0.0110 * b + 18.93
                                                     t_{WR} = 0.0066 * b + 3.34
     = 0.0006 * 512 + 0.0110 * 16 + 18.93
                                                           = 0.0066 * 16 + 3.34
     = 19.42 ns (typ)
                                                          = 3.45 ns (typ)
                                                     t<sub>DH</sub> = 0.0347 * b + 3.51
t_{AS} = 3.30 \text{ ns (typ)}
                                                           = 0.0347 * 16 + 3.51
                                                           = 4.11 ns (typ)
```

## **ROM SPECIFICATION**

### **FEATURES**

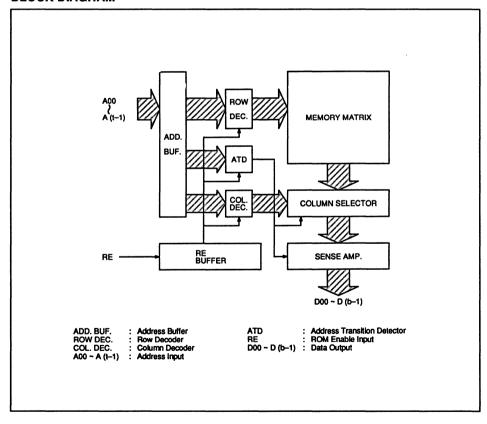
- Configurable size
- Non-clocked static ROM

### **SPECIFIC PARAMETERS**

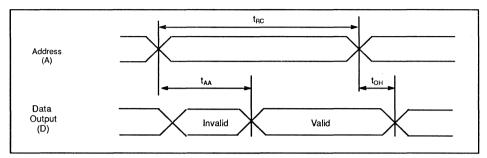
Word size range: 16 to 2K words

• Bit size range: 4 to 64 bits

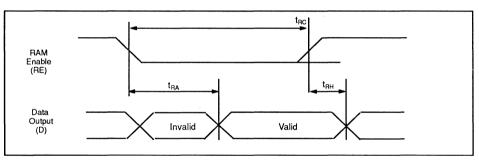
### **BLOCK DIAGRAM**



### **TIMING DIAGRAMS**



Address Control<sup>1</sup>



RE Control<sup>2</sup>

Notes: ¹ROM Enable (RE) must be Low in the address control ²In RE control, the address must be validated before ROM Enable (RE) becomes low.

### **CELL SYMBOL AND CELL SPECIFICATION**

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						Α	U Version		
Cell Name								Number of BC	
ROMxx	k b bit)							1	
Cell Symi	ool			Propaga	tion Delay	/ Parar	neter		
A00 —	D00	tı	dr		to	dn			Path
A01 A02	D01	t <sub>o</sub>	K <sub>CL</sub>	to	K <sub>CL</sub>	K <sub>CL</sub>	<sub>2</sub> C <sub>D</sub>	R2	7 441
		٠	0.07	•	0.04	0.07	7		$\begin{array}{c} A \rightarrow D \\ RE \rightarrow D \end{array}$
A (t – 2) ——————————————————————————————————	D (b – 2) D (b – 1)								
	Input Loading		Paramet	L er	L		Sym	bol	Typ (ns) **
Pin Name	Factor (lu)	Read Cycle Time					t <sub>RC</sub>		
A***		Address Access Time					t <sub>AA</sub>		
RE		RAM Enable Access Time					t <sub>RA</sub>		
		Output Hold from Address Change					ŧон		
		Output Hold from RAM Enable Change					t <sub>RH</sub>		
Pin Name	Output Driving Factor (Iu)								
D***	36								
		* Refer to the Read Mode and Write Mode Tables on pages.  * Minimum values for the typical operating condition. The values for the worst case operating condition a			on.				
the maximum delay multiplier. The values indicated here depend on bit-word organiz are given in the Read Mode Delay Time Table on the f page.									
		Pin Name When b or t ≤ 10, these pin names are described with two characters: e.g., A9.							

### **BASIC DELAY TIME**

#### Read Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t <sub>RC</sub>	Read Cycle Time	c = 4: 33.12 c = 8: 33.02	ns
t <sub>AA</sub>	Address Access Time	c = 4: 0.0161 * w + 0.0226 * b + 16.85 c = 8: 0.0080 * w + 0.0258 * b + 17.81	ns
t <sub>RA</sub>	RAM Enable Access Time	c = 4: 0.0173 * w + 0.0290 * b + 16.55 c = 8: 0.0091 * w + 0.0487 * b + 16.63	ns
t <sub>OH</sub>	Output Hold from Address Change	c = 4: 0.0194 * b + 4.36 c = 8: 0.0258 * b + 4.40	ns
t <sub>RH</sub>	Output Hold from RAM Enable Change	c = 4: 0.0194 * w + 6.76 c = 8: 0.0258 * w + 6.61	ns

### Example

To find the delay time for the Read-mode for a ROM of 512 words, 16 bits, and c = 4:

```
\begin{array}{lll} t_{RC} & = & 33.12 \\ \\ t_{AA} & = & 0.0161 * w + 0.0226 * b + 16.85 \\ & = & 0.0161 * 512 + 0.0226 * 16 + 16.85 \\ & = & 25.46 \, \text{ns} \\ \\ t_{RA} & = & 0.0173 * w + 0.0290 * b + 16.55 \\ & = & 0.0173 * 512 + 0.0290 * 16 + 16.55 \\ & = & 25.88 \, \text{ns} \\ \\ t_{OH} & = & 0.0194 * b + 4.36 \\ & = & 0.0194 * 16 + 4.36 \\ & = & 4.67 \, \text{ns} \\ \\ t_{RH} & = & 0.0194 * b + 6.76 \\ & = & 0.0194 * 16 + 6.76 \\ & = & 7.07 \, \text{ns} \\ \end{array}
```

# **Appendix A: General AC Specifications**

#### Simulation Delay Specifications

(Recommended Operating Conditions, Ta = 0 to 70°C,  $V_{DD} = 5 V_{\pm}5\%$ 

Delay Multipliers	Min.	Max.
Pre-layout Simulation	0.35	t <sub>maxB</sub>
Post-layout Simulation	0.40	t <sub>maxA</sub>

Junction Temperate	ure (Tj)	tmaxB	tmaxA
Tj <u>≤</u>	60°C	1.65	1.55
60°C <tj td="" ≤<=""><td>70°C</td><td>1.70</td><td>1.60</td></tj>	70°C	1.70	1.60
70°C <tj td="" ≤<=""><td>80°C</td><td>1.75</td><td>1.65</td></tj>	80°C	1.75	1.65
80°C <tj td="" ≤<=""><td>90°C</td><td>1.80</td><td>1.70</td></tj>	90°C	1.80	1.70
90°C <tj td="" ≤<=""><td>105°C</td><td>1.85</td><td>1.75</td></tj>	105°C	1.85	1.75
105°C <tj td="" ≤<=""><td>120°C</td><td>1.90</td><td>1.80</td></tj>	120°C	1.90	1.80
120°C <tj <u="">≤</tj>	130°C¹	1.95	1.85
130°C <tj td="" ≤<=""><td>140°C²</td><td>2.00</td><td>1.90</td></tj>	140°C²	2.00	1.90
140°C <tj <u="">≤</tj>	150°C²	2.05	1.95

**NOTES:** 1. This condition cannot be applied to devices in some plastic packages. If this condition is required for devices in plastic, please consult Fujitsu.

2. This condition cannot be applied to devices in plastic packages. If this condition is required even for ceramic packages, please consult Fujitsu.

Tj is determined by the following formula:

$$Ti = T_{aMAX} + \theta ia \times Pd (^{\circ}C)$$

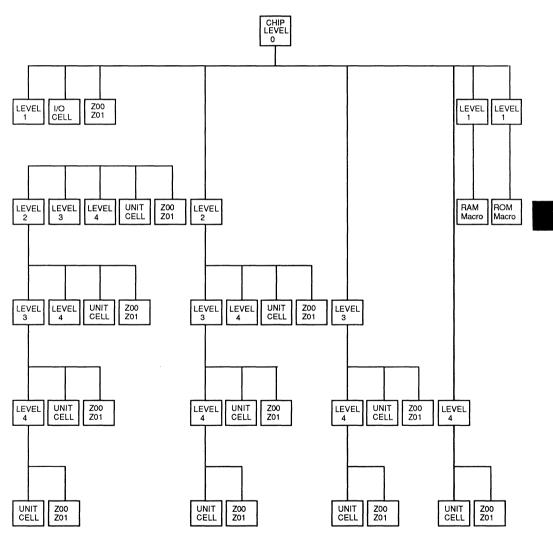
where

Pd: Power dissipation (W)

θja: Thermal Resistance (°C/W). This value is determined for each package.

Tamax: Maximum Ambient Termperature (°C)

# **Appendix B: Hierarchical Structure**



# Appendix C: Estimation Tables for Metal Loading

## C-10KAU (Main Block)

	C <sub>L</sub> (lu)					
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4	
1	4.1	2.8	1.8	1.1	0.6	
2	6.2	4.3	2.7	1.7	0.8	
3	8.3	5.7	3.7	2.3	1.1	
4	9.7	6.7	4.3	2.7	1.3	
5	10.7	7.4	4.7	2.9	1.5	
6	11.6	8.0	5.1	3.2	1.6	
7	12.7	8.8	5.6	3.5	1.7	
8	13.2	9.1	5.8	3.6	1.8	
9	13.5	9.3	6.0	3.7	1.8	
10	13.9	9.6	6.1	3.8	1.9	
11	13.9	9.6	6.1	3.8	1.9	
12	14.1	9.7	6.2	3.9	1.9	
13	14.3	9.9	6.3	3.9	1.9	
14	14.6	10.1	6.5	4.0	2.0	
15	14.6	10.1	6.5	4.0	2.0	
16 – 30	15.8	10.9	7.0	4.3	2.2	
31 – 50	18.1	12.5	8.0	5.0	2.5	
51 – 75	18.6	12.8	8.2	5.1	2.5	
76 –100	20.5	14.1	9.1	5.6	2.8	

### C-10KAU (Sub Block)

O-TOKAO (GGD DIOCK)						
	C <sub>L</sub> (lu)					
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4		
1	1.9	1.2	0.7	0.4		
2	3.4	2.1	1.3	0.6		
3	4.8	3.1	1.9	0.9		
4	5.8	3.7	2.3	1.1		
5	6.5	4.1	2.5	1.3		
6	7.1	4.5	2.8	1.4		
7	7.9	5.0	3.1	1.5		
8	8.2	5.2	3.2	1.6		
9	8.4	5.4	3.3	1.6		
10	8.7	5.5	3.4	1.7		
11	8.7	5.5	3.4	1.7		
12	8.8	5.6	3.5	1.7		
13	9.0	5.7	3.5	1.7		
14	9.2	5.9	3.6	1.8		
15	9.2	5.9	3.6	1.8		
16 – 30	10.0	6.4	3.9	2.0		
31 – 50	11.6	7.4	4.6	2.3		
51 – 75	11.9	7.6	4.7	2.3		
76 – 100	13.2	8.5	5.2	2.6		

## C-15KAU (Main Block)

	C <sub>L</sub> (lu)					
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4	
1	5.1	2.8	1.8	1.1	0.6	
2	7.7	4.3	2.7	1.7	0.8	
3	10.4	5.7	3.7	2.3	1.1	
4	12.1	6.7	4.3	2.7	1.3	
5	13.4	7.4	4.7	2.9	1.5	
6	14.4	8.0	5.1	3.2	1.6	
7	15.8	8.8	5.6	3.5	1.7	
8	16.4	9.1	5.8	3.6	1.8	
9	16.9	9.3	6.0	3.7	1.8	
10	17.3	9.6	6.1	3.8	1.9	
11	17.3	9.6	6.1	3.8	1.9	
12	17.6	9.7	6.2	3.9	1.9	
13	17.8	9.9	6.3	3.9	1.9	
14	18.3	10.1	6.5	4.0	2.0	
15	18.3	10.1	6.5	4.0	2.0	
16 – 30	19.7	10.9	7.0	4.3	2.2	
31 – 50	22.6	12.5	8.0	5.0	2.5	
51 – 75	23.2	12.8	8.2	5.1	2.5	
76 –100	25.6	14.1	9.1	5.6	2.8	

## C-15KAU (Sub Block)

	C <sub>L</sub> (lu)					
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4		
1	1.9	1.2	0.7	0.4		
2	3.4	2.1	1.3	0.6		
3	4.8	3.1	1.9	0.9		
4	5.8	3.7	2.3	1.1		
5	6.5	4.1	2.5	1.3		
6	7.1	4.5	2.8	1.4		
7	7.9	5.0	3.1	1.5		
8	8.2	5.2	3.2	1.6		
9	8.4	5.4	3.3	1.6		
10	8.7	5.5	3.4	1.7		
11	8.7	5.5	3.4	1.7		
12	8.8	5.6	3.5	1.7		
13	9.0	5.7	3.5	1.7		
14	9.2	5.9	3.6	1.8		
15	9.2	5.9	3.6	1.8		
16 – 30	10.0	6.4	3.9	2.0		
31 – 50	11.6	7.4	4.6	2.3		
51 – 75	11.9	7.6	4.7	2.3		
76 – 100	13.2	8.5	5.2	2.6		

## C-20KAU (Main Block)

	C <sub>L</sub> (lu)					
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4	
1	5.9	2.8	1.8	1.1	0.6	
2	8.9	4.3	2.7	1.7	0.8	
3	11.9	5.7	3.7	2.3	1.1	
4	13.9	6.7	4.3	2.7	1.3	
5	15.4	7.4	4.7	2.9	1.5	
6	16.6	8.0	5.1	3.2	1.6	
7	18.2	8.8	5.6	3.5	1.7	
8	18.9	9.1	5.8	3.6	1.8	
9	19.4	9.3	6.0	3.7	1.8	
10	19.9	9.6	6.1	3.8	1.9	
11	19.9	9.6	6.1	3.8	1.9	
12	20.2	9.7	6.2	3.9	1.9	
13	20.5	9.9	6.3	3.9	1.9	
14	21.0	10.1	6.5	4.0	2.0	
15	21.0	10.1	6.5	4.0	2.0	
16 – 30	22.7	10.9	7.0	4.3	2.2	
31 – 50	26.0	12.5	8.0	5.0	2.5	
51 <i>–</i> 75	26.7	12.8	8.2	5.1	2.5	
76 –100	29.4	14.1	9.1	5.6	2.8	

### C-20KAU (Sub Block)

	C <sub>L</sub> (lu)					
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4		
1	1.9	1.2	0.7	0.4		
2	3.4	2.1	1.3	0.6		
3	4.8	3.1	1.9	0.9		
4	5.8	3.7	2.3	1.1		
5	6.5	4.1	2.5	1.3		
6	7.1	4.5	2.8	1.4		
7	7.9	5.0	3.1	1.5		
8	8.2	5.2	3.2	1.6		
9	8.4	5.4	3.3	1.6		
10	8.7	5.5	3.4	1.7		
11	8.7	5.5	3.4	1.7		
12	8.8	5.6	3.5	1.7		
13	9.0	5.7	3.5	1.7		
14	9.2	5.9	3.6	1.8		
15	9.2	5.9	3.6	1.8		
16 – 30	10.0	6.4	3.9	2.0		
31 – 50	11.6	7.4	4.6	2.3		
51 – 75	11.9	7.6	4.7	2.3		
76 – 100	13.2	8.5	5.2	2.6		

## C-30KAU (Main Block)

	C <sub>L</sub> (lu)					
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4	
1	9.9	7.8	5.5	3.5	1.7	
2	14.9	11.6	8.3	5.3	2.6	
3	20.0	15.6	11.1	7.1	3.5	
4	23.4	18.3	13.0	8.3	4.1	
5	25.9	20.3	14.4	9.2	4.6	
6	27.9	21.9	15.5	9.9	4.9	
7	30.6	23.9	17.0	10.9	5.4	
8	31.8	24.9	17.6	11.3	5.6	
9	32.6	25.5	18.1	11.6	5.7	
10	33.4	26.2	18.6	11.9	5.9	
11	33.4	26.2	18.6	11.9	5.9	
12	33.9	26.5	18.8	12.0	6.0	
13	34.4	26.9	19.1	12.2	6.1	
14	35.2	27.6°	19.6	12.5	6.2	
15	35.2	27.6	19.6	12.5	6.2	
16 – 30	38.1	29.9	21.2	13.5	6.7	
31 – 50	43.6	34.2	24.2	15.5	7.7	
51 – 75	44.9	35.1	24.9	15.9	7.9	
76 –100	49.3	38.6	27.3	17.5	8.7	

## C-30KAU (Sub Block)

	C <sub>L</sub> (lu)					
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4		
1	4.7	3.3	2.2	1.0		
2	8.6	6.1	3.9	1.9		
3	12.6	8.9	5.7	2.8		
4	15.2	10.8	7.0	3.4		
5	17.2	12.2	7.8	3.8		
6	18.8	13.3	8.6	4.2		
7	20.6	14.8	9.5	4.7		
8	21.8	15.5	9.9	4.9		
9	22.5	15.9	10.2	5.0		
10	23.1	16.4	10.5	5.2		
11	23.1	16.4	10.5	5.2		
12	23.4	16.6	10.7	5.2		
13	23.9	16.9	10.9	5.3		
14	24.5	17.4	11.2	5.5		
15	24.5	17.4	11.2	5.5		
16 – 30	26.8	19.0	12.2	6.0		
31 – 50	31.1	22.1	14.1	7.0		
51 – 75	32.1	22.7	14.6	7.2		
76 – 100	35.5	25.2	16.1	8.0		

## C-40KAU (Main Block)

	C <sub>L</sub> (lu)				
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	11.3	7.8	5.5	3.5	1.7
2	17.0	11.6	8.3	5.3	2.6
3	22.8	15.6	11.1	7.1	3.5
4	26.7	18.3	13.0	8.3	4.1
5	29.6	20.3	14.4	9.2	4.6
6	31.9	21.9	15.5	9.9	4.9
7	34.9	23.9	17.0	10.9	5.4
8	36.3	24.9	17.6	11.3	5.6
9	37.3	25.5	18.1	11.6	5.7
10	38.2	26.2	18.6	11.9	5.9
11	38.2	26.2	18.6	11.9	5.9
12	38.7	26.5	18.8	12.0	6.0
13	39.3	26.9	19.1	12.2	6.1
14	40.3	27.6	19.6	12.5	6.2
15	40.3	27.6	19.6	12.5	6.2
16 – 30	43.6	29.9	21.2	13.5	6.7
31 – 50	49.9	34.2	24.2	15.5	7.7
51 – 75	51.3	35.1	24.9	15.9	7.9
76 – 100	56.3	38.6	27.3	17.5	8.7

### C-40KAU (Sub Block)

	C <sub>L</sub> (lu)					
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4		
1	4.7	3.3	2.2	1.0		
2	8.6	6.1	3.9	1.9		
3	12.6	8.9	5.7	2.8		
4	15.2	10.8	7.0	3.4		
5	17.2	12.2	7.8	3.8		
6	18.8	13.3	8.6	4.2		
7	20.6	14.8	9.5	4.7		
8	21.8	15.5	9.9	4.9		
9	22.5	15.9	10.2	5.0		
10	23.1	16.4	10.5	5.2		
11	23.1	16.4	10.5	5.2		
12	23.4	16.6	10.7	5.2		
13	23.9	16.9	10.9	5.3		
14	24.5	17.4	11.2	5.5		
15	24.5	17.4	11.2	5.5		
16 – 30	26.8	19.0	12.2	6.0		
31 – 50	31.1	22.1	14.1	7.0		
51 – 75	32.1	22.7	14.6	7.2		
76 – 100	35.5	25.2	16.1	8.0		

## C-50KAU (Main Block)

	C <sub>L</sub> (lu)				
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	12.7	7.8	5.5	3.5	1.7
2	19.1	11.6	8.3	5.3	2.6
3	25.7	15.6	11.1	7.1	3.5
4	30.1	18.3	13.0	8.3	4.1
5	33.3	20.3	14.4	9.2	4.6
6	35.9	21.9	15.5	9.9	4.9
7	39.3	23.9	17.0	10.9	5.4
8	40.9	24.9	17.6	11.3	5.6
9	41.9	25.5	18.1	11.6	5.7
10	43.0	26.2	18.6	11.9	5.9
11	43.0	26.2	18.6	11.9	5.9
12	43.5	26.5	18.8	12.0	6.0
13	44.2	26.9	19.1	12.2	6.1
14	45.3	27.6	19.6	12.5	6.2
15	45.3	27.6	19.6	12.5	6.2
16 – 30	49.0	29.9	21.2	13.5	6.7
31 – 50	56.1	34.2	24.2	15.5	7.7
51 – 75	57.7	35.1	24.9	15.9	7.9
76 – 100	63.3	38.6	27.3	17.5	8.7

### C-50KAU (Sub Block)

	C <sub>L</sub> (lu)				
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4	
1	4.7	3.3	2.2	1.0	
2	8.6	6.1	3.9	1.9	
3	12.6	8.9	5.7	2.8	
4	15.2	10.8	7.0	3.4	
5	17.2	12.2	7.8	3.8	
6	18.8	13.3	8.6	4.2	
7	20.6	14.8	9.5	4.7	
8	21.8	15.5	9.9	4.9	
9	22.5	15.9	10.2	5.0	
10	23.1	16.4	10.5	5.2	
11	23.1	16.4	10.5	5.2	
12	23.4	16.6	10.7	5.2	
13	23.9	16.9	10.9	5.3	
14	24.5	17.4	11.2	5.5	
15	24.5	17.4	11.2	5.5	
16 – 30	26.8	19.0	12.2	6.0	
31 – 50	31.1	22.1	14.1	7.0	
51 – 75	32.1	22.7	14.6	7.2	
76 – 100	35.5	25.2	16.1	8.0	

## C-75KAU (Main Block)

·	C <sub>L</sub> (lu)					
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4	
1	15.2	7.8	5.5	3.5	1.7	
2	22.8	11.6	8.3	5.3	2.6	
3	30.6	15.6	11.1	7.1	3.5	
4	35.9	18.3	13.0	8.3	4.1	
5	39.7	20.3	14.4	9.2	4.6	
6	42.9	21.9	15.5	9.9	4.9	
7	46.9	23.9	17.0	10.9	5.4	
8	48.8	24.9	17.6	11.3	5.6	
9	50.1	25.5	18.1	11.6	5.7	
10	51.4	26.2	18.6	11.9	5.9	
11	51.4	26.2	18.6	11.9	5.9	
12	52.0	26.5	18.8	12.0	6.0	
13	52.8	26.9	19.1	12.2	6.1	
14	54.1	27.6	19.6	12.5	6.2	
15	54.1	27.6	19.6	12.5	6.2	
16 – 30	58.6	29.9	21.2	13.5	6.7	
31 – 50	67.0	34.2	24.2	15.5	7.7	
51 – 75	68.9	35.1	24.9	15.9	7.9	
76 – 100	75.7	38.6	27.3	17.5	8.7	

### C-75KAU (Sub Block)

	C <sub>L</sub> (lu)				
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4	
1	4.7	3.3	2.2	1.0	
2	8.6	6.1	3.9	1.9	
3	12.6	8.9	5.7	2.8	
4	15.2	10.8	7.0	3.4	
5	17.2	12.2	7.8	3.8	
6	18.8	13.3	8.6	4.2	
7	20.6	14.8	9.5	4.7	
8	21.8	15.5	9.9	4.9	
9	22.5	15.9	10.2	5.0	
10	23.1	16.4	10.5	5.2	
11	23.1	16.4	10.5	5.2	
12	23.4	16.6	10.7	5.2	
13	23.9	16.9	10.9	5.3	
14	24.5	17.4	11.2	5.5	
15	24.5	17.4	11.2	5.5	
16 – 30	26.8	19.0	12.2	6.0	
31 – 50	31.1	22.1	14.1	7.0	
51 – 75	32.1	22.7	14.6	7.2	
76 – 100	35.5	25.2	16.1	8.0	

## C-100KAU (Main Block)

			C. (lu)		
j	ļ		C <sub>L</sub> (lu)	<b>,</b>	
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	17.7	7.8	5.5	3.5	1.7
2	26.5	11.6	8.3	5.3	2.6
3	35.6	15.6	11.1	7.1	3.5
4	41.8	18.3	13.0	8.3	4.1
5	46.2	20.3	14.4	9.2	4.6
6	49.9	21.9	15.5	9.9	4.9
7	54.6	23.9	17.0	10.9	5.4
8	56.8	24.9	17.6	11.3	5.6
9	58.2	25.5	18.1	11.6	5.7
10	59.7	26.2	18.6	11.9	5.9
11	59.7	26.2	18.6	11.9	5.9
12	60.5	26.5	18.8	12.0	6.0
13	61.4	26.9	19.1	12.2	6.1
14	62.9	27.6	19.6	12.5	6.2
15	62.9	27.6	19.6	12.5	6.2
16 – 30	68.1	29.9	21.2	13.5	6.7
31 – 50	77.9	34.2	24.2	15.5	7.7
51 – 75	80.1	35.1	24.9	15.9	7.9
76 – 100	88.0	38.6	27.3	17.5	8.7

### C-100KAU (Sub Block)

	C <sub>L</sub> (lu)				
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4	
1	4.7	3.3	2.2	1.0	
2	8.6	6.1	3.9	1.9	
3	12.6	8.9	5.7	2.8	
4	15.2	10.8	7.0	3.4	
5	17.2	12.2	7.8	3.8	
6	18.8	13.3	8.6	4.2	
7	20.6	14.8	9.5	4.7	
8	21.8	15.5	9.9	4.9	
9	22.5	15.9	10.2	5.0	
10	23.1	16.4	10.5	5.2	
11	23.1	16.4	10.5	5.2	
12	23.4	16.6	10.7	5.2	
13	23.9	16.9	10.9	5.3	
14	24.5	17.4	11.2	5.5	
15	24.5	17.4	11.2	5.5	
16 – 30	26.8	19.0	12.2	6.0	
31 – 50	31.1	22.1	14.1	7.0	
51 – 75	32.1	22.7	14.6	7.2	
76 – 100	35.5	25.2	16.1	8.0	

# Appendix D: AU CMOS Gate Array Available Package Types

		DEVICE NAME							
Package Name	Package Material	C-10KAU	C-15KAU	C-20KAU	C-30KAU	C-40KAU	C-50KAU	C-75KAU	C-100KAU
PGA-64	Ceramic	•	•	•					
PGA-88	Ceramic	•	•	•					
PGA-135	Ceramic	•	•	•	•	•	•	•	•
PGA-179	Ceramic	_	_	•	•	•	•	•	•
PGA-208	Ceramic	_	_	_	•	•	•	•	•
PGA-256	Ceramic			_		•	•	•	•
PGA-299	Ceramic	<del>-</del>	_				0	0	0
PGA-321	Ceramic							0	0
PGA-361	Ceramic	_						0	0
PGA-401	Ceramic		_		_	_		_	0
QFP-64	Plastic	•	•	•					
QFP-80	Plastic	•	•	•					
QFP-100	Plastic	•	•	•					
QFP-120	Plastic	•	•	•	•	•			
QFP-160	Plastic	_	•	•	•	•	_	_	
PLCC-68	Plastic	•	•	•					_
PLCC-84	Plastic	•	•	•				_	
SDIP-64	Plastic	•	•	•		_	_		_

Note:

- = Available
- o = Under Development
- = Not Available

# Appendix E: TTL 7400 Function Conversion Table

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7400	Quad 2-input NAND	4 x N2N	4
7401	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7402	Quad 2-input NOR	4 x R2N	4
7403	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7404	Hex Inverter	6 x VIN	6
7405	Hex Inverter, Open Collector Outputs	R6B	5
7406	Hex Inverter/Buffer, Open Collector Outputs	R6B	5
7407	Hex Buffer, Open Collector Outputs	2 x N3N into R2N	5
7408	Quad 2-input AND	4 x N2P	8
7409	Quad 2-input AND, Open Collector Outputs	N8P	6
7410	Triple 3-input NAND	3 x N3N	6
7411	Triple 3-input AND	3 x N3P	9
7412	Triple 3-NAND, Open Collector Outputs	T33	7
7413	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7414	Hex Schmitt Trigger Inverter	6 x l1R	48
7415	Triple 3-input AND, Open Collector Outputs	N8P to N2P	8
7418	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7419	Hex Schmitt Trigger Inverter	6 x I1R	48
7420	Dual 4-input NAND	2 x N4N	4
7421	Dual 4-input AND	2 x N4P	6
7422	Dual 4-input NAND, Open Collector Outputs	2 x N4N + N2P	6
7423	Expanded Dual 4-input NOR with Strobe	R4P to D23 + R4P to R2N	9
7424	Quad Schmitt Trigger 2-input NAND	8 x I2R + 4 x N2N	68
7425	Dual 4-input NOR with Strobe	2 x (R4P + R2N)	8
7426	Quad 2-input NAND, High Voltage Output	4 x N2N	4
7427	Triple 3-input NOR	3 x R3N	6
7428	Quad 2-input NOR Buffer	4 x R2N	4
7430	8-input NAND	N8B	6
7432	Quad 2-input OR	4 x R2P	8
433	Quad 2-input NOR Buffer, Open Collector		_
	Outputs	4 x R2N + N4P	7
7434	Hex Noninverter	6 x B1N	6
7435	Hex Noninverter with Open Collector Outputs	2 x N3N into R2N	5
7437	Quad 2-input NAND Buffer	4 x N2B	12
7438/9	Quad 2-input NAND Buffer, Open Collector	A NON NAD	_
	Outputs	4 x N2N + N4P	7
7440	Dual 4-input NAND Buffer	2 x N4B (N4N if not power)	8(4)
7442	BCD to Decimal Decoder	4 x V2B + 10 x N4N	24
7443	EX3 to Decimal Decoder	4 x V2B + 10 x N4N	24
444	4 to 10 Line Decoder	4 x V2B + 10 x N4N	24
445	BCD to Decimal Decoder/driver (30V)	4 x V2B + 10 x N4N	24
446	BCD to 7-segment Decoder/Driver (30V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7447	BCD to 7-segment Decoder/Driver (15V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
448	BCD to 7-segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53 53
7449 7450	BCD to 7-segment, Open Collector Outputs	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P D36 + D24	53 5
7450	Dual 2-input, 2-wide AOI (One Expandable)		5 4
7451 7452	AOI	2 x D24 N3N + D36 + V1N into N3N	8
7452 7453	Expandable 4-wide AND-OR	D36 + D23 into N2P	7
453	Expandable 4-wide AOI 4-wide AOI	2 x N3N + 2 x N2N + N4N + V1N	9
454 7455	2-wide 4-input AOI		6
7455 7460		T42 2 x N4P	6
	Dual 4-input Expander		
7461 7462	Triple 3-input Expander	3 x N3P	6 8
7462 7464	4-wide AND-OR Expander 4-2-3-2 AOI	2 x N3N + 2 x N2N + N4N T54	8 10
7464 7465	4-2-3-2 AOI (Open Collector)	T54	10
400	4-2-3-2 AUI (UDER CORECTOR)	104	10

# Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7470	AND-gated positive-edge JK FF with Preset		
7470	and Clear	3 x V1N + 2 x N3N + N2N + R2N + FJD	. 21
	or:	FD4 + 2 x N2N + R2N + V1N + R2P + D24	17
7471	AND-gated RS M/S FF with Preset	TOT I EXILET THE THE TOET	• • • • • • • • • • • • • • • • • • • •
, .	and Clear	FD4 + 2 x N3N + 2 x D23 + 2 x V1N	19
	or:	LT1+ 2 x N4N + N2P	10
7472	AND-gated JK M/S FF with Preset		
	and Clear	V1N + 2 x N3N + N2N + R2N + FJD	19
	or:	FD4 + N3P + N3N + V1N + D24	17
7473	Dual JK FF with Clear	2 x FJD	24
7474	Dual positive-edge D-FF with Preset and		
	Clear	2 x FDP	16
7475	4-bit Bistable Latch	LTM	16
7476	Dual JK FF with Preset and Clear	2 x (FJD + N2N + R2N + V1N)	30
7477	4-bit Bistable Latch	LTM	16
7478	Dual JK FF with Preset and Common	2 x (FJD + N2N + R2N + V1N)	30
	Clear and Clock		
7480	Gated Full Adder	A1N	8
7482	2-bit Binary Full Adder	A2N	16
7483	4-bit Binary Full Adder with Fast Carry	A4H	48
7484	4-bit Magnitude Comparator	MC4	42
7486	Quad 2-input XOR	4 x X2N	12
7487	4-bit True/Complement Zero/One Element	4 x N2N + V1N + 4 x N2N	17
7489	64-bit (16 x 4) Memory	2 x DE6 + V1N + 16 x LT4	298
		+ 5 x (V2B + T5A) + 10 x V2B	
7490	Decade Counter	2 x (FDP + FDO + N2P + N2N + R2N) + V1N	39
	(Different Implementation)	4 x N2P + 2 x R2P + N2N + C41 + LT1	41
7491	8-bit Shift Register	2 x FDS + V1N	41
7492	Divide-by-12 Counter	4 x FDO + 2 x V1N + 2 x R2N + N2N	33
7493	4-bit Binary Counter	C41 + N2N (for the resets)	25
7494	4-bit Shift Register, 2 asynchronous Presets	FS3	34
	4-bit Shift Register, 2 asynchronous		
	Presets, Full Implementation	4 x FDP + 4 x D24 + 2 x V1N	42
7495	4-bit Parallel-access Shift Register	FS2 + D24 + 2 x V1N	34
7496	5-bit Shift Register	5 x FDP + 5 x N2N + V1N(clock)	46
7497	Synch 6-bit Binary Rate Multiplier	FDR + 2 x FDO + 3 x V1N + 2 x N2N	122
		+ 2 x N3N + 2 x N4N + 5 x N6B + 3 x N8B	
7.100	4100 . 01 . 00 . 0	+ R2B + X2N + 5 x X1B.	
7498	4-bit Data Selector/Storage Register	FDQ + T2F + 4 x V1N	33
7499	4-bit Universal Shift Register	FS2 + LTK + 2 x D24 + 4 x V1N	42
74100	8-bit Bistable Latch	2 x YL4 + 2 x V1N	30
74101	AO-gated JK Negative-Edge FF,	EDO MAN O DOA	45
74400	with Preset	FD3 + V1N + 3 x D24	15
74102	AND-gated JK Negative-Edge FF with	EDA DOA NOD NON	40
74400	Preset and Clear	FD4 + D24 + N3P + N3N	16
74103	Dual JK FF with Clear	2 x FJD + 2 x V1N (for clock)	26 22
74106	or:	2 x (FD5 + D24 + V1N)	22
74100	Dual JK Negative-Edge FF with Preset and Clear	2 × (ED4 + D24 + V4N)	24
74107	and Clear Dual JK FF with Clear	2 x (FD4 + D24 + V1N) 2 x (FJD + 2 x V1N)	24 22
74107		2 x (FJU + 2 x V IIV)	22
74100	Dual JK Negative-Edge FF with Preset and Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74109	Dual JK Positive-Edge FF with Preset and	2 x (1 D4 + D24 + VIN)	24
74109	Clear	2 × (EDB + V1N + D24)	22
74110		2 x (FDP + V1N + D24)	. 22
/4110	AND-gated JK M/S FF with Data Lockout	EDD - D24 - N2D - N2N	15
74111	Dual JK M/S FF with Data Lockout	FDP + D24 + N3P + N3N	15 22
74111		2 x (FDP + D24 + V1N)	22
14112	Dual JK Negative-Edge FF with Preset and Clear	2 × (ED4 + D24 + V1N)	24
	and Olean	2 x (FD4 + D24 + V1N)	24

# Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74113	Dual JK Negative-Edge FF with Preset	2 x (FD3 + D24 + V1N)	22
74114	Dual JK Negative-Edge FF with Preset and	0(ED4 D04 V(4N)	0.4
74440	Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74116	Dual 4-bit Latch with Clear	2 x LTM	32
74120	Dual Pulse Synchronizer/Driver	2 x (N2P + LT1 + 4 x N3N + 2 x N2N + 2 x V1N)	36
74125	Quad Bus Buffer with 3-state Output	B41	9 13
74126	Quad Bus Buffer with 3-state Output	B41 + 4 x V1N	68
74132 74133	Quad 2-input NAND Schmitt Trigger 13-input NAND	4 x (2 x I2R + N2N) 2 x N4N + N3N + N2N into R4P	10
74133 74134	12-input NAND with 3-state Outputs	NCB + O4R	15
74134 74135	Quad 3-input EXOR/EXNOR	4 x X4N	20
74135 74136		4 X A4IN	20
74136	Quad 2-input EXOR with Open-Collector	A v VON - DAN	14
74107	Outputs 3-line to 8-line Decoder with Address	4 x X2N + R4N	14
74137	Latch	3 x LTK into DE6	42
74138	3-line to 8-line Decoder with Enable	DE6	30
74139	Dual 2-line to 4-line Decoder	2 x DE4	16
74139	BCD-to-Decimal Decoder	4 x V2B + 10 x N4N	24
74141	BCD-to-decimal Decoder	4 x V2B + 10 x N4N 4 x V1N + 10 x N4N	24
74145 74147	10-line to 4-line BCD Priority Encoder	3 x N4N + 3 x N3N + 2 x N2N + 2 x N2P	36
74147	TO-line to 4-line BOD Phonty Encoder	+ 3 x R2N + R4N + 13 x V1N	36
74148	C. line to 2. line Octol Drierity Encoder	N9B + 2 x N2N + R2P + R4N + 4 x N3N	40
74146	8-line to 3-line Octal Priority Encoder	+ 2 x N4N + G44 + 12 x V1N	40
74150	1-to-16 Multiplexer	DE3 + 2 x U28 + D24 + 2 x V1N	41
74150	1–to–16 Multiplexer  1–to–8 Multiplexer with Strobe	DE3 + 2 x 028 + D24 + 2 x V IN DE3 + U28 + N2N + V1N	28
		DE3 + U28 + N2N + VIN	
74152 74153	1-to-8 Multiplexers	DE2 + 2 x U24 + 2 x R2N	26
	Dual 4-line to 1-line Selector/Multiplexer		19
74154	4-line to 16-line Decoder/Demultiplexer	2 x DE6 + V1N	61 50
74155	or:	2 x DE4 + N2P + 16 x R2P	50
74155	Dual 2-line to 4-line Decoder/Demultiplexer (Totem Pole)	8 x N3N + 2 x R2N + 5 x V1N	23
74156	Dual 2-line to 4-line Decoder/Demultiplexer		
	(Open Collector)	8 x N3N + 2 x R2N + 5 x V1N	23
74157	Quad 2-line to 1-line multiplexer	T2F + 4 x R2N + B1N	13
74158	Quad 2-line to 1-line multiplexer		
	(Inverter Data Outputs)	4 x D24 + V1N + 2 x R2N	11
74159	4-line to 16-line Demultiplexer	2 x DE6 + V1N (without open collector)	50
74160	Synchronous 4-bit Counter	4 x C11 + K1B + 2 x V2B + V1N + B1N+	62
	(Decimal with Direct Clear)	N2K + 2 x R3N + R4N + 3 x R2N + N2N	
74161	Synchronous 4-bit Counter (Binary		
	with Direct Clear)	C43	48
74162	Synchronous 4-bit Counter		
	(Decimal with Synchronous Clear)	C45 + D36 + N3P + 2 x R2N + B1N	57
74163	Synchronous 4-bit Counter (Binary		
	with Synchronous Clear)	C45	48
74164	8-bit Parallel Output Serial Shift		
	Register, Asynchronous Clear	2 x FDR + N2P	54
74165	8-bit Shift Register	2 x FDS + 8 x D24 + 11 x V1N + K4B + R2P	71
74166	8-bit Shift Register	2 x FDR + 8 x D24 + 10 x V1N + K4B	80
74168	4-bit Up/Down Synchronous Counter		
	(Decade)	4 x C11 + 4 x T32 + 7 x N2N + 2 x N3N + R2N + 7 x V2B + K1B	85
74169	4-bit Up/Down Synchronous Counter		
	(Binary)	C47	68
74170	4-by-4 Register File	4 x (YL4 + B1N + V1N + U24) + 2 x DE4	104
74171	Quad D-FF with Clear	FDR + 4 x V1N	30
74172	16-bit (8 x 2) Register File	3 x DE6 + 4 x FDS + 16 x (N2N + G34 +	348
17116	IO MI (O X Z) Neglatel I lie	+ V1N + 2 x R2P + 4 x U28) + 2 x V1N + 2 x R2P	340
		, T Z X 1 (2) + 4 X O 20 / + 2 X T 1 (4 + 2 X 1 (2)	

# **Appendix E: TTL 7400 Function Conversion Table** (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74173	4-bit D-type Register		
	(3-state Output)	FDR + 2 x R2N + B41 + 6 x V1N + K1B + 4 x D24	53
74174	Hex D-FF (Single Output)	FDR + 2 x FDO	40
74175	Quad D-FF (with Clear)	FDR + 4 x V1N	30
74176	Presettable Decade/Binary Counter	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74177	Presettable Binary Counter	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74178	4-bit Universal Shift Register	FS2	30
74179	4-bit Universal Shift Register		•
	(Direct Clear)	FS2 + 9 x N2N + B1N	40
74180	9-bit Odd/Even Parity Checker	PO8 + 2 x D24 + V1N	23
74181	ALU/Function Generator	5 x V1N + 5 x T32 + 4 x D36 + 8 x X2N + 3 x T54 +	20
14101	ALON Unclion denerator	N6B + N4B + 2 x N2N + 2 x N4P	113
74182	Look-ahead Carry Generator	R4P + 2 x V1N + 2 x T44 + T33 + D24	36
74182 74183	Dual Carry-save Full Adder	144 + 2 x V 1 N + 2 x 144 + 133 + D24 2 x A1N	16
4103	Duai Carry-save Full Adder	ZXAIN	16
74184	BCD-to-binary Code Converter	These devices are ROM based	
74185	Binary-to-BCD Code Converter	These devices are ROM based	
74190	Synch Up/Down Counter (BCD)	4 x FDP + 4 x X2N + K1B + 3 x V1N + 3 x N3N	
	-,	+ 9 x N2N + 2 x T32 + T43	
74191	Synch Up/Down Counter (Binary)	C47	68
74192	Up/Down Dual Clock Counter (BCD)	4 x C11 + 4 x V2B + N6B + 2 x N3N + R2N	79
74102	oproduit buai clock counter (Bob)	+ T32 + T42 + T43	,,
74193	Up/Down Dual Clock Counter (Binary)	4 x C11 + 2 x N6B + 4 x V2B + R2N + D24 + T32 + T42	72
74194	4-bit Bidirectional Universal Shift Register	FDR + 6 x V1N + R2N + 4 x D36 + D23 + B1N	48
74195	4-bit Parallel Access Shift Register	FS2 + D24 + 2 x V1N	34
74196	Preset Decade/Binary Counter/Latch	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74197	Preset Binary Counter/Latch	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74198	8-bit Bidirectional Universal Shift Register	2 x FDR + D24 + 10 x V1N + R2N + 8 x D36	89
74199	8-bit Bidirectional Universal Shift	2 X 1 DN + D24 + 10 X V 114 + 1(2)4 + 0 X D00	03
4133	Register (JK Serial Input)	2 x FS2 + D24 + 3 x V1N + B1N + R2N + 8 x N2P	83
		2 x FDR + 7 x D24 + T33 + 11 x V1N + R2N	85
74246	or:	2 X FDH + 7 X D24 + 133 + 11 X V IN + H2N	85
74246	BCD-to-7-Segment Decoder/Driver		
	(30V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74247	BCD-to-7-Segment Decoder/Driver		
	(15V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74248	BCD-to-7-Segment Decoder/Driver		
	(Internal Pull-up)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74249	BCD-to-7-Segment Decoder/Driver		
	(Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74260	Dual 5-input NOR	2 x R6B	10
74265	Quad Complementary Output Element	B1N + V1N	
74266	Quad 2-EXNOR, Open Collector	4 x X1N	12
74273	Octal D-type FF with Clear	2 x FDR	52
74276	Quad J-K FF	4 x (FDP + V1N + D24) + 2 x B1N	46
	BCD-to-7-Segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53

# **Appendix F: Alphanumeric Index of Unit Cells**

Name	Function	Page No.
A1A	1-bit Half Adder	2-249
A1N	1-bit Full Adder	2-250
A2N	2-bit Full Adder	2-251
A4H	4-bit Binary Full Adder with Fast Carry	2-253
BD3	Delay Cell	2–11
BD4	Delay Cell	2–12
BD5	Delay Cell	2–13
BD6	Delay Cell	2-14
B1N	True Buffer	2-10
B11	1-bit Bus Driver	2–315
B12	1-bit Block Bus Driver	2–319
B21	2-bit Bus Driver	2–316
B22	2-bit Block Bus Driver	2-320
B41	4-bit Bus Driver	2–317
B42	4-bit Block Bus Driver	2-321
B81	8-bit Bus Driver	2–318
C11	Non-Scan Flip-flop for Counter	2-219
C41	Non-Scan 4-bit Binary Asynchronous Counter	2-221
C42	Non-Scan 4-bit Binary Synchronous Counter	2-224
C43	Non-Scan 4-bit Binary Synchronous Up Counter	2-227
C45	Non-Scan 4-bit Binary Synchronous Up Counter	2-231
C47	Non-Scan 4-bit Binary Synchronous Up/Down Counter	2-235
DE2	2:4 Decoder	2-294
DE3	3:8 Decoder	2-295
DE4	2:4 Decoder with Enable	2-297
DE6	3:8 Decoder with Enable	2-298
D14	2-wide 3-AND 4-Input AOI	2–68
D23	2-wide 2-AND 3-Input AOI	2-67
D24	2-wide 2-AND 4-Input AOI	2-69
D34	3-wide 2-AND 4-Input AOI	2–70
D36	3-wide 2-AND 6-Input AOI	2–71
D44	2-wide 2-OR 2-AND 4-Input AOI	2-72
FDM	Non-Scan D Flip-flop	2–181
FDN	Non-Scan D Flip-flop with Set	2–183
FDO	Non-Scan D Flip-flop with Reset	2–185
FDP	Non-Scan D Flip-flop with Set and Reset	2–187
FDQ	Non-Scan 4-bit D Flip-flop	2–190
FDR	Non-Scan 4-bit D Flip-flop with Clear	2–192
FDS	Non-Scan 4-bit D Flip-flop	2–195
FD2	Non-Scan Power D Flip-flop	2–197

Name	Function	Page No.
FD3	Non-Scan Power D Flip-flop with Preset	2-198
FD4	Non-Scan Power D Flip-flop with Clear and Preset	2-201
FD5	Non-Scan Power D Flip-flop with Clear	2-203
FJD	Non-Scan Positive Edge Clocked Power J-K FK with Clear	2-205
FS1	4-bit Serial-in Parallel-out Shift Register	2-275
FS2	4-bit Shift Register with Synchronous Load	2–277
FS3	4-bit Shift Register with Asynchronous Load	2–279
G14	2-wide 3-OR 4-Input OAI	2–76
G23	2-wide 2-OR 3-Input OAI	2–75
G24	2-wide 2-OR 4-Input OAI	2–77
G34	3-wide 2-OR 4-Input OAI	2–78
G44	2-wide 2-AND 2-OR 4-Input OAI	2–79
H6C	3-state Output (I <sub>OL</sub> = 3.2 mA) and CMOS Interface Input Buffer (True)	2–379
H6CD	H6C with Pull-down Resistance	2–381
H6CF	3-state Output and CMOS Interface Input Buffer (I <sub>OL</sub> = 8 mA,True)	2-422
H6CFD	H6CF with Pull-down Resitance	2-424
H6CFU	H6CF with Pull-up Resistance	2–423
H6CU	H6C with Pull-up Resistance	2–380
H6E	Power 3-state Output (I <sub>OL</sub> = 12 mA) and CMOS Interface Input Buffer (True)	2–382
H6ED	H6E with Pull-down Resistance	2-384
H6EU	H6E with Pull-up Resistance	2–383
H6R	3-state Output (I <sub>OL</sub> = 3.2 mA) and Schmitt Trigger Input Buffer	
	(TTL type, True)	2–388
H6RD	H6R with Pull-down Resistance	2–390
H6RU	H6R with Pull-up Resistance	2–389
H6S	3-state Output (I <sub>OL</sub> = 3.2 mA) and Schmitt Trigger Input Buffer (CMOS type, True)	2–385
H6SD	H6S with Pull-down Resistance	2–387
H6SU	H6S with Pull-up Resistance	2–386
H6T	3-state Output (I <sub>OL</sub> = 3.2 mA) and Input Buffer (True)	2–373
H6TD	H6T with Pull-down Resistance	2–375
H6TF	3-state Output and Input Buffer (I <sub>OL</sub> = 8 mA, True)	2–419
H6TFD	H6TF with Pull-down Resistance	2–421
H6TFU	H6TF with Pull-up Resistance	2–420
H6TU	H6T with Pull-up Resistance	2–374
H6W	Power 3-state Output (I <sub>OL</sub> = 12 mA) and Input Buffer (True)	2–376
H6WD	H6W with Pull-down Resistance	2–378
H6WU	H6W with Pull-up Resistance	2–377
H8C	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA) with Noise Limit Resistance and CMOS	0.007
LIGOD	Interface Input Buffer (True)	2–397
H8CD	H8C with Pull-down Resistance	2–399

Name	Function	Page No.
H8CF	3-state Output Buffer with Noise Limit Resistance and CMOS	
	Interface Input Buffer (I <sub>OL</sub> = 8 mA, True)	2-428
H8CFD	H8CF with Pull-down Resistance	2-430
H8CFU	H8CF with Pull-up Resistance	2-429
H8CU	H8C with Pull-up Resistance	2-398
H8E	Power 3-state Output Buffer (I <sub>OL</sub> = 12 mA) with Noise Limit Resistance and CMOS Interface Input Buffer (True)	2–400
H8ED	H8E with Pull-down Resistance	2-402
H8EU	H8E with Pull-up Resistance	2-401
H8E2	3-state Output with Noise Limit Resistance and Input Buffer, (CMOS, True)	2-436
H8E1	H8E2 with Pull-up Resistance	2-437
H8E0	H8E2 with Pull-down Resistance	2-438
H8R	3-state Output and Schmitt Trigger Input Buffer (TTL type, True)	
	with Noise Limit Resistance	2-406
H8RD	H8R with Pull-down Resistance	2-408
H8RU	H8R with Pull-up Resistance	2-407
H8S	3-state Output and Schmitt Trigger Input Buffer (CMOS type, True)	
	with Noise Limit Resistance	2–403
H8SD	H8S with Pull-down Resistance	2–405
H8SU	H8S with Pull-up Resistance	2-404
H8T	3-state Output with Noise Limit Resistance and Input Buffer (True)	2–391
H8TD	H8T with Pull-down Resistance	2–393
H8TF	3-state Output with Noise Limit Resistance and Input Buffer	2–425
H8TFD	(I <sub>OL</sub> = 8 mA, True) H8TF with Pull-down Resistance	2–425 2–427
H8TFU		2–42 <i>1</i> 2–426
H8TU	H8TF with Pull-up Resistance	2–392
H8W	H8T with Pull-up Resistance	2–392 2–394
H8WD	Power 3-state Output with Noise Limit Resistance and Input Buffer (True) H8W with Pull-down Resistance	2–394 2–396
H8WU		2–396 2–395
H8W2	H8W with Pull-up Resistance	2–393 2–433
H8W1	3-state Output with Noise Limit Resistance and Input Buffer, (TTL, True) H8W2 with Pull-up Resistance	2–433 2–434
H8W0	H8W2 with Pull-down Resistance	2–435
IKB	Clock Input Buffer (Inverter)	2–337
IKBD	IKB with Pull-down Resistance	2–339
IKBU		2–338
IKC	IKB with Pull-up Resistance CMOS Interface Clock Input Buffer (Inverter)	2–409
IKCD	,	2-409
IKCU	IKC with Pull-down Resistance	2–411 2–410
ILB	IKC with Pull-up Resistance	2–410 2–340
	Clock Input Buffer (True)	2-340 2-342
ILBD	ILB with Pull-down Resistance	2–342 2–341
ILBU	ILB with Pull-up Resistance	2-341

Name	Function	Page No.
ILC	CMOS Interface Clock Input Buffer (True)	2-412
ILCD	ILC with Pull-down Resistance	2-414
ILCU	ILC with Pull-up Resistance	2-413
I1B	Input Buffer Inverter	2–331
I1BD	I1B with Pull-down Resistance	2–333
I1BU	I1B with Pull-up Resistance	2–332
I1C	CMOS Interface Input Buffer (Inverter)	2–343
I1CD	I1C with Pull-down Resistance	2–345
I1CU	I1C with Pull-up Resistance	2–344
I1R	Schmitt Trigger Input Buffer (TTL Type, Inverter)	2–355
I1RD	I1R with Pull-down Resistance	2–354
I1RU	I1R with Pull-up Resistance	2–356
I1S	Schmitt Trigger Input Buffer (CMOS Type, Inverter)	2–349
I1SD	I1S with Pull-down Resistance	2–351
I1SU	I1S with Pull-up Resistance	2–350
I2B	Input Buffer (True)	2–334
I2BD	I2B with Pull-down Resistance	2–336
I2BU	I2B with Pull-up Resistance	2–335
I2C	CMOS Interface Input Buffer (True)	2–346
12CD	I2C with Pull-down Resistance	2–348
I2CU	I2C with Pull-up Resistance	2–347
I2R	Schmitt Trigger Input Buffer (TTL Type, True)	2–358
I2RD	I2R with Pull-down Resistance	2–360
I2RU	I2R with Pull-up Resistance	2–359
128	Schmitt Trigger Input Buffer (CMOS Type, True)	2–352
I2SD	I2S with Pull-down Resistance	2–354
I2SU	I2S with Pull-up Resistance	2–353
KAB	Block Clock (OR) Buffer	2–110
KBB	Block Clock Buffer(OR x 10)	2–111
KDB	Block Clock Buffer(OR x 10)	2–113
KEB	Block Clock Buffer	2–115
K1B	True Clock Buffer	2–105
K2B	Power Clock Buffer	2–106
КЗВ	Gated Clock (AND) Buffer	2–107
K4B	Gated Clock (OR) Buffer	2–108
K5B	Gated Clock (NAND) Buffer	2–109
LTK	Data Latch	2–261
LTL	1-bit Data Latch with Clear	2-263
LTM	4-bit Data Latch with Clear	2–265
LT1	S-R Latch with Clear	2–268
LT4	4-bit Data Latch	2–270
MC4	4-bit Magnitude Comparator	2–311
2-482		

Name	Function	Page No.
NCB	Power 12-Input NAND	2-27
NGB	Power 16-Input NAND	2-28
N2B	Power 2-Input NAND	2–18
N2K	Power 2-Input NAND	2-19
N2N	2-Input NAND	2–17
N2P	Power 2-Input AND	2–45
N3B	Power 3-Input NAND	2–21
N3N	3-Input NAND	2-20
N3P	Power 3-Input AND	2–46
N4B	Power 4-Input NAND	2-23
N4N	4-Input NAND	2–22
N4P	Power 4-Input AND	2–47
N6B	Power 6-Input NAND	2-24
N8B	Power 8-Input NAND	2–25
N8P	Power 8-Input AND	2-48
N9B	Power 9-Input NAND	2–26
O1B	Output Buffer (I <sub>OL</sub> = 3.2 mA Inverter)	2–361
O1L	Power Output Buffer (I <sub>OL</sub> = 12 mA Inverter)	2–362
O1R	Output Buffer (I <sub>OL</sub> = 3.2 mA Inverter) with Noise Limit Resistance	2–363
O1S	Power Output Buffer (I <sub>OL</sub> = 12 mA Inverter) with Noise Limit Resistance	2–364
O2B	Output Buffer (I <sub>OL</sub> = 3.2 mA, True)	2–365
O2BF	Output Buffer (I <sub>OL</sub> = 8 mA, True)	2–415
O2L	Power Output Buffer (I <sub>OL</sub> = 12 mA, True)	2–366
O2R	Output Buffer (I <sub>OL</sub> = 3.2 mA, True) with Noise Limit Resistance	2–367
O2RF	Output Buffer (I <sub>OL</sub> = 8 mA, True)with Noise Limit Resistance	2–416
O2S	Power Output Buffer (I <sub>OL</sub> = 12 mA, True) with Noise Limit Resistance	2–368
O2S2	Output Buffer (I <sub>OL</sub> = 12 mA, True) with Noise Limit Resistance	2-431
O4R	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA, True) with Noise Limit Resistance	2–369
O4RF	3-state Output Buffer (I <sub>OL</sub> = 8 mA, True) with Noise Limit Resistance	2–418
O4S	Power 3-state Output Buffer (I <sub>OL</sub> = 12 mA, True) with Noise Limit Resistance	2–370
O4S2	3-state Output Buffer (I <sub>OI</sub> = 24 mA, True) with Noise Limit Resistance	2–432
040L	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA, True)	2–371
O4TF	3-state Output Buffer (I <sub>OL</sub> = 8 mA, True)	2–417
04W	Power 3-state Output Buffer (I <sub>OL</sub> = 12 mA, True)	2-372
PE5	5-bit Even Parity Generator/Checker	2–287
PE8	8-bit Even Parity Generator/Checker	2–289
PE9	9-bit Even Parity Generator/Checker	2–291
PO5	5-bit Odd Parity Generator/Checker	2–288
PO8	8-bit Odd Parity Generator/Checker	2–290
PO9	9-bit Odd Parity Generator/Checker	2–292
P24	4-wide 2:1 Data Selector	2–293
	. 1100 E.1 Data 00100101	0.40

Name	Function	Page No.
RCB	Power 12-Input NOR	2-41
RGB	Power 16-Input NOR	2-42
R2B	Power 2-Input NOR	2-32
R2K	Power 2-Input NOR	2–33
R2N	2-Input NOR	2–31
R2P	Power 2-Input OR	2–51
R3B	Power 3-Input NOR	2–35
R3N	3-Input NOR	2–34
R3P	Power 3-Input OR	2–52
R4B	Power 4-Input NOR	2–37
R4N	4-Input NOR	2–36
R4P	Power 4-Input OR	2–53
R6B	Power 6-Input NOR	2–38
R8B	Power 8-Input NOR	2–39
R8P	Power 8-Input OR	2–54
R9B	Power 9-Input NOR	2-40
SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	2-209
SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	2-214
SC43	Scan 4-bit Synchronous Binary Up Counter with Asynchronous Clear	2-239
SC47	Scan 4-bit Synchronous Binary Up/Down Counter	2-243
SDA	Scan 1-Input D Flip-flop with Clock Inhibit	2–135
SDB	Scan 1-Input 4-bit D Flip-flop with Clock Inhibit	2–138
SDD	Scan 2-Input D Flip-flop with Clear, Preset, and Clock Inhibit	2–131
SDH	Scan 2-Input D Flip-flop with Clear and Clock Inhibit	2–119
SDJ	Scan 4-Input D Flip-flop with Clear and Clock Inhibit	2–122
SDK	Scan 6-Input D Flip-flop with Clear and Clock Inhibit	2-125
SFDM	Scan 1-Input D Flip-flop with Clock Inhibit	2–157
SFDO	Scan 1-Input D Flip-flop with Clear and Clock Inhibit	2-160
SFDP	Scan 1-Input D Flip-flop with Clear, Preset, and Clock Inhibit	2-163
SFDR	Scan 4-Input D Flip-flop with Clear and Clock Inhibit	2–167
SFDS	Scan 4-Input D Flip-flop with Clock Inhibit	2–171
SFJD	Scan J-K Flip-flop with Clock Inhibit	2–175
SHA	Scan 1-Input 8-bit D Flip-flop with Clock Inhibit	2–142
SHB	Scan 1-Input 8-bit D Flip-flop with Clock Inhibit and Q Output	2–145
SHC	Scan 1-Input 8-bit D Flip-flop with Clock Inhibit and XQ Output	2–148
SHJ	Scan 8-bit D Flip-flop with Clock Inhibit and 2-to-1 Data Multiplexer	2-151
SHK	Scan 8-bit D Flip-flop with Clock Inhibit and 3-to-1 Data Multiplexer	2-154
SJH	Scan J–K Flip-flop with Clear and Clock Inhibit	2–128
SR1	Scan 4-bit Serial-in Parallel-out Shift Register with Scan	2-282
T2B	2:1 Selector	2–300
T2C	Dual 2:1 Selector	2–301
T2D	2:1 Selector	2–303
2-484		

Name	Function	Page No.
T2E	Dual 2:1 Selector	2–304
T2F	2:1 Selector	2–305
T24	Power 2-AND 4-wide Multiplexer	2–83
T26	Power 2-AND 6-wide Multiplexer	2–84
T28	Power 2-AND 8-wide Multiplexer	2–85
T32	Power 3-AND 2-wide Multiplexer	2–87
T33	Power 3-AND 3-wide Multiplexer	2–88
T34	Power 3-AND 4-wide Multiplexer	2–89
T42	Power 4-AND 2-wide Multiplexer	2–90
T43	Power 4-AND 3-wide Multiplexer	2–91
T44	Power 4-AND 4-wide Multiplexer	2–92
T54	Power 4-2-3-2 AND 4-wide Multiplexer	2–93
T5A	4:1 Selector	2–307
U24	Power 2-OR 4-wide Multiplexer	2–94
U26	Power 2-OR 6-wide Multiplexer	2–95
U28	Power 2-OR 8-wide Multiplexer	2–96
U32	Power 3-OR 2-wide Multiplexer	2–97
U33	Power 3-OR 3-wide Multiplexer	2–98
U34	Power 3-OR 4-wide Multiplexer	2–99
U42	Power 4-OR 2-wide Multiplexer	2–100
U43	Power 4-OR 3-wide Multiplexer	2–101
U44	Power 4-OR 4-wide Multiplexer	2–102
V1L	Inverting Clock Buffer	2–9
V1N	Inverter	2–7
V2B	Power Inverter	2–8
V3A	1:2 Selector	2–309
V3B	Dual 1:2 Selector	2–310
X1B	Power Exclusive NOR	2–58
X1N	Exclusive NOR	2–57
X2B	Power Exclusive OR	2–60
X2N	Exclusive OR	2–59
ХЗВ	Power 3-Input Exclusive NOR	2–62
X3N	3-Input Exclusive NOR	2–61
X4B	Power 3-Input Exclusive OR	2–64
X4N	3-Input Exclusive OR	2–63
YL2	1-bit Data Latch with TM	2–257
YL4	4-bit Data Latch with TM	2–259
Z00	0 Clip	2–325
Z01	1 Clip	2–326

**CG21 Series CMOS Gate Array Unit Cell Library** 

Page	Contents
3–2	Unit Cell Specification Information
3–5	Inverter and Buffer Family
3–15	NAND Family
3–29	NOR Family
3–43	AND Family
3-49	OR Family
3–55	EXNOR/EXOR Family
3–65	AND-OR-Inverter Family
3–73	OR-AND-Inverter Family
3–81	Multiplexer Family
3-103	Clock Buffer Family
3-119	Scan Flip-flop (Positive Edge Type) Family
3–181	Non Scan Flip-flop Family
3–209	Scan Counter Family
3–229	Non-scan Counter Family
3–251	Adder and ALU Family
3–259	Data Latch Family
3–277	Shift Register Family
3–289	Parity Generator/Selector/Decoder Family
3–317	Bus Driver Family
3–327	Clip Cell Family
3–331	I/O Buffer Family
3-437	Appendix A: General AC Specifications
3-439	Appendix B: Hierarchical Structure
3-441	Appendix C: Estimation Tables for Metal Loading
3-447	Appendix D: Available Package Types
3-449	Appendix E: TTL 7400 Function Conversion Table
3–453	Appendix F: Alphanumeric Index of Unit Cells

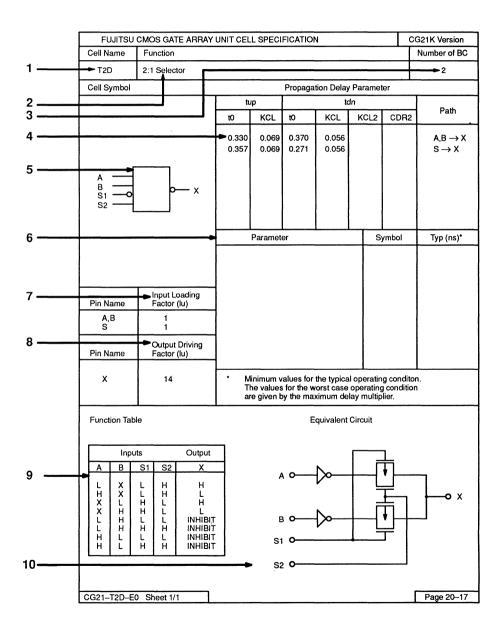
### **Unit Cell Specification Information**

This section contains specifications for all the unit cells available for the CG21 Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates. A basic cell contains one pair of P-channel and one pair of N-channel transistors (and two pairs of smaller N-channel resistors used for compiled cell construction).

#### How to Read a Unit Cell Specification

The following paragraphs numbered 1–10 explain how the information given in the CG21 Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

- 1. The unit *cell name* appears in the upper left corner of the page.
- 2. The unit cell function is given on the same line as the unit cell name.
- 3. The *number of basic cells (BC)* or equivalent that make up the unit cell is shown in the upper right corner of the page.
- 4. Propagation delay parameters for the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t<sub>0</sub>) is given in ns. K<sub>CL</sub>, the delay constant for the cell (delay time per load unit) is given in ns/pF. K<sub>CL2</sub> and C<sub>DR2</sub> are a delay constant and an output driving factor used to calculate delay when a unit cell is loaded beyond its published output driving factor (C<sub>DR</sub>).
- 5. The cell symbol (logic symbol) is shown in the top left box under the cell name.
- Clock parameters (in ns) for unit cells such as flip-flops and counters that make use of clock signals
  are given in a table directly below the propagation delay parameters.
- 7. The input loading factor of each input of the unit cell are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
- 8. The output drive factor of each output of the unit cell is shown directly under the input loading factor. The output drive factor is the maximum number of load units the unit cell can drive while performing at published specifications.
- 9. The function table (truth table), if applicable, is shown in a box at the lower left side of the page.
- The unit cell schematic, or equivalent circuit, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.



3

### Inverter, Buffer Family

Page	Unit Cell Name	Function	Basic Cells
3–7	V1N	Inverter	1
3–8	V2B	Power Inverter	1
3–9	B1N	True Buffer	1
3–10	BD3	Delay Cell	5
3–11	BD4	Delay Cell	4
3–12	BD5	Delay Cell	9
3-13	BD6	Delay Cell	17

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG21F	C " Version
Cell Name	Function							Number of BC
V1N	Inverter							1
Cel	i Symbol			Pro		elay Param	eter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
		0.137	0.060	0.203	0.039	0.056	4	A to X
		0.107	0.000	0.200	0.000	0.000		71.0
			1					
Α ——	> ×							
		İ						
		Paramete	er				Symbol	Typ (ns) *
		1						
						- 1		
						İ		
Pin Name	Input Loading	1						
Pin Name	Factor (lu)	ļ						
Α	1	]						
		İ						
		i						
	Output Driving	ł						
Pin Name	Factor (lu)							
х	18							
		* Minimu	m values fo	r the typical	operating o	condition.	aivon by th	e maximum delay
		multiplie		worst case	operating o	ondition are	given by u	e maximum delay
		<u> </u>						
C21-V1N-E0	Sheet 1/1							Doct 4.4
								Page 1-1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21F	( " Version
Cell Name	Function							Number of BC
V2B	Power Inverter							1 1
Cell	l Symbol			Pro	pagation D	elay Paran	neter	
		t O	лр KCL	t O	KCL	In KCL2	CDR2	Path
}		0.119	0.032	0.145	0.023	0.039	7	A to X
							]	
1						ł		
A	> ×					ĺ		
	V							
						l		
		Paramete	er				Symbol	Typ (ns) *
						- 1		
		}						
	·							
		1				ł		
Pin Name	Input Loading Factor (lu)							
A	2					ļ		
						1		
						- 1		
	Output Driving					1		
Pin Name	Factor (lu)							
×	36							
]		* Minimu The val	m values foues for the	r the typical worst case	operating operating o	condition. ondition are	given by th	e maximum delay
		multipli						-
	L	L						
1								
C21-V2B-E0	Sheet 1/1							Page 1 2
								Page 1-2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version							" Version	
Cell Name							Number of BC	
B1N	True Buffer							1
Cell	l Symbol			Proj	pagation D		neter	
		t O	IP KCL	t O	KCL	in KCL2	CDR2	Path
		0.310	0.060	0.363	0.039		33.12	A to X
							1 1	
					ļ			
ı								
Α	> ×							
					<u> </u>			
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading							
	Factor (lu)							
A	1							
Pin Name	Output Driving							
	Factor (lu)							
Х	18	* Minimu	m values fo	r the typical	operating	20ndition		
		The val	ues for the	worst case	operating o	ondition are	given by the	maximum delay
		multiplie	er.					
	L							
C21-B1N-E0	Sheet 1/1							Page 1-3
								i age i-o

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name Function								Number of BC
BD3	Delay Cell							5
	Symbol			Prot	pagation D	elav Param	eter	
	- Cymuu	tu	ıp	,		in		Doth
		t O	KCL	t O	KCL	KCL2	CDR2	Path
		2.818	0.060	2.488	0.056	0.062	4	A to X
					Ì			
	<b>\</b>							
Α	×							
		Paramete	).		L	L	Symbol	Typ (ns) *
		Taramete	1				Symbol	136 (113)
							1	
Pin Name	Input Loading							
	Factor (lu)							
A	'							
Dia Nama	Output Driving							
Pin Name	Factor (lu)							
×	18		<del></del>					
			m values fo				e given by the	maximum delay
		multiplie					,	,
		L						
İ								
C21-BD3-E0	Sheet 1/1							Dog 1 4
								Page 1-4

FUNITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION   **GG27K* Version   *GE17K* Version		CHICHOS CATE ADI	DAY LIAU	CCLLC	DECIEIO	ATION		* CC011	C" Vorsion
Parameter   Propagation Delay Parameter   Path	Cell Name	Function	HAY UNI	CELLS	PECIFICA	ATION		CGZII	
Cell Symbol  To KOL to KOL KOL2 CDR2    1.881   0.211   2.165   0.140   0.162   4		1							
Pin Name Input Loading Factor (Iu)  X  6  **Melimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21-BD4-E0** Sheet 1/1		1	<del></del>		Pro	nagation D	elay Daran	eter	
Pin Name Input Loading Factor (iu)  A 4  Pin Name Output Driving Factor (iu)  X 6  Minimum values for the lypical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.		Symbol	t	ıp	F10			ietei	5.4
Pin Name Input Loading Factor (tu)  A 4  Pin Name Output Driving Factor (the Mark of the Mark of the Worst case operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0 Sheet 1/1								CDR2	
Pin Name Input Loading Factor (tu)  A 4  Pin Name Coutput Driving Factor (tu)  X 6  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0 Sheet 1/1			1.881	0.211	2.165	0.140	0.162	4	A to X
Pin Name Input Loading Factor (tu)  A 4  Pin Name Coutput Driving Factor (tu)  X 6  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0 Sheet 1/1			1				1		
Pin Name Input Loading Factor (tu)  A 4  Pin Name Coutput Driving Factor (tu)  X 6  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0 Sheet 1/1				•					
Pin Name Input Loading Factor (tu)  A 4  Pin Name Coutput Driving Factor (tu)  X 6  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0 Sheet 1/1					•				
Pin Name Input Loading Factor (tu)  A 4  Pin Name Coutput Driving Factor (tu)  X 6  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0 Sheet 1/1			ł	ł		ł			
Pin Name Input Loading Factor (tu)  A 4  Pin Name Coutput Driving Factor (tu)  X 6  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0 Sheet 1/1									
Pin Name Input Loading Factor (tu)  A 4  Pin Name Output Driving Factor (tu)  **Y 6  ** Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21-BD4-E0   Sheet 1/1	Δ								
Pin Name   Input Loading Factor (tu)    A		^ ^				}			
Pin Name   Input Loading Factor (fu)    A									
Pin Name   Input Loading Factor (fu)    A			}			<u> </u>			
Pin Name Output Driving Factor (lu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0   Sheet 1/1			Paramete	er				Symbol	Typ (ns) *
Pin Name Output Driving Factor (lu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0   Sheet 1/1									
Pin Name Output Driving Factor (lu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0   Sheet 1/1							- 1		
Pin Name Output Driving Factor (lu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0   Sheet 1/1									
Pin Name Output Driving Factor (lu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0   Sheet 1/1							İ	Ì	
Pin Name Output Driving Factor (lu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0   Sheet 1/1		Input Loading	1				1		
Pin Name Cutput Driving Factor (lu)  X 6 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0 Sheet 1/1	Pin Name	Factor (lu)					1		
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21-BD4-E0   Sheet 1/1	Α	4					- 1		
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21-BD4-E0   Sheet 1/1							- 1		
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21-BD4-E0** Sheet 1/1**			1						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21-BD4-E0** Sheet 1/1**			4						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-BD4-E0 Sheet 1/1	Pin Name	Factor (lu)					ı		
The values for the worst case operating condition are given by the maximum delay multiplier.	X								
C21-BD4-E0 Sheet 1/1			* Minimu	m values fo	r the typical	operating of	condition.	alisaa bir th	a mavimum dalau
C21-BD4-E0 Sheet 1/1					worst case	operating o	onation are	given by u	e maximum delay
C21-BD4-E0 Sheet 1/1		<u> </u>	L						
C21-BD4-E0 Sheet 1/1									
C21-BD4-E0 Sheet 1/1									
C21-BD4-E0 Sheet 1/1									
C21-BD4-E0 Sheet 1/1									
C21-BD4-E0 Sheet 1/1									
C21-BD4-E0   Sheet 1/1									
C21-BD4-E0   Sheet 1/1	1								
C21-BD4-E0   Sheet 1/1									!
C21-BD4-E0   Sheet 1/1									
C21-BD4-E0   Sheet 1/1									
C21-BD4-E0   Sheet 1/1									
C21-BD4-E0   Sheet 1/1									
C21-BD4-E0   Sheet 1/1									
C21-BD4-E0   Sheet 1/1									:
021-004-C0   Olicet I/1	CO1_BD4_EA	Sheet 1/1							
Page 1–5	UZ1-004-00	Office 1/1							Page 1-5

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function		<del></del>					Number of BO
BD5	Delay Cell							9
	l Symbol	Τ		Pro	pagation D	elay Daran	neter	
	reymoor	tu	ıρ			in	10.00	
		t O	KCL	t O	KCL	KCL2	CDR2	Path
• •		5.769	0.060	5.465	0.045	0.067	4	A to X
		l					1 1	
			1					
						1	1 1	
							1 1	
Α	x				İ	}		
^	^				ĺ		1 1	
					į			
					ļ			
		Dawn made	<u> </u>	L	<u>L</u>	<u> </u>	Cumbal	Tun (na) t
		Paramete	er				Symbol	Typ (ns) *
						- 1		
							i	
		1						
							İ	
		4				1	1	•
Pin Name	Input Loading Factor (lu)						1	
Α .	1	1				1	1	
^		1				1		
		1						
						- 1		
	Output Driving	┨				- 1		
Pin Name	Factor (lu)	1				- [		
X	18							
		* Minimu	m values fo	r the typical	l operating	condition.		
		The val		worst case	operating c	ondition are	given by the	maximum delay
		Indiapik	JI.					
	<u> </u>							
C21-BD5-E0	Sheet 1/1							Page 1 6
								Page 1-6

	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
BD6	Delay Cell							17
	   Symbol	1		Pro	pagation D	elay Param	neter	
		tı			to	dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		11.616	0.064	11.524	0.039	0.062	4	A to X
		ļ						
}								
	<b>\</b> ,							
A	x							
1		Paramete	<u> </u>	l	L	<u>Ц</u>	Symbol	Typ (ns) *
		raramete	71				Symbol	Typ (IIs)
ļ						j	)	
							1	
							1	
		]				j		
Pin Name	Input Loading	]						
	Factor (lu)	ł					1	
A	1	1						
		[				I	1	
		1					1	
	Output Driving	1						
Pin Name	Factor (lu)	<u> </u>					[	
X	18	ļ				L		
		* Minimur	n values fo	r the typical	operating o	condition.	aiven by the	maximum delay
		multiplie		WOISI Case	operating o	onanion are	given by and	maximum delay
			·					
C21-BD6-E0	Sheet 1/1							
								Page 1-7

### **NAND Family**

Page	Unit Cell Name	Function	Basic Cells
3–17	N2N	2-input NAND	1
3–18	N2B	Power 2-input NAND	3
3–19	N2K	Power 2-input NAND	2
3–20	N3N	3-input NAND	2
3–21	N3B	Power 3-input NAND	3
3–22	N4N	4-input NAND	2
3–23	N4B	Power 4-input NAND	4
3–24	N6B	Power 6-input NAND	5
3–25	N8B	Power 8-input NAND	6
3–26	N9B	Power 9-input NAND	8
3–27	NCB	Power 12-input NAND	10
3–28	NGB	Power 16-input NAND	11

	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
N2N	2-input NAND							1
Cell	Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	ln KCL2	CDR2	Path
		0.179	0.060	0.326	0.062			A to X
							]	
A1	_							
A2	)×							
		Paramete	er				Symbol	Typ (ns) *
						1		
	Input Loading							
Pin Name	Factor (lu)							
Α	1							
Pin Name	Output Driving							
×	Factor (lu)							
		* Minimur	n values fo	r the typical	operating o	condition.		4-1
		The vali multiplie		worst case	operating o	ondition ar	e given by the	maximum delay
C21-N2N-E0	Sheet 1/1							1
								Page 2-1

CITUT	SU CMOS GATE ARE	דוואו ו עמ	CELLS	PECIFIC	ATION		" CG21K	" Version
Cell Name	Function	TAT UNIT	OLLL 3	LOIFIC	ATION		CGZIK	Number of BC
N2B	Power 2-input N	IAND						3
Cel	l Symbol			Pro	pagation D	elay Paran	neter	
			ıp			dn		Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	A to V
		0.581	0.032	0.753	0.017		1	A to X
					Ì			
					ŀ			
A1	<b>√</b> "							
A2	<b>)</b> >── ×							
		İ						
		Paramete	<u> </u>		L	L	Symbol	Typ (ns) *
		Paramete	#				Symbol	Typ (IIS)
		ĺ						
Pin Name	Input Loading							
	Factor (lu)					Ì		
Α	1							
		1				- 1	1	
							Ī	
	Output Driving					l		
Pin Name	Factor (lu)							
X	36							
		* Minimu	m values fo	r the typical	operating of	condition. ondition are	aiven by the	maximum delay
		multiplie	er.	Worst oaso	operating o	onanon ar	given by alc	maximom colay
	<u> </u>	l						
i								
								•
C21-N2B-E0	Sheet 1/1							T B 0.0
								Page 2-2

	SU CMOS GATE ARF	TUALI VAS	CELLS	PECIFIC	ATION		" CG21	K " Version
Cell Name	Function	TAT UNIT	OLLL 3	LOIFIO	ATION		CGZT	Number of BC
N2K	Power 2-input N	IAND						2
Cel	l Symbol			Pro	pagation D		neter	
		t O	JP KCL	t O	KCL to	In KCL2	CDR2	Path
		0.179	0.032	0.254	0.034	0.039	7	A to X
A1 ——— A2 ———	Do ×							
			L			L	<u></u>	T (= ) •
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
Α	2					1		
Pin Name	Output Driving Factor (lu)							
X	36	* Minimu The val multiplie		r the typical worst case	operating o	condition. ondition are	given by th	ne maximum delay
	0							
C21-N2K-E0	Sheet 1/1							Page 2–3

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG21	K " V	ersion/
Cell Name	Function								Number of BC
N3N	3-input NAND								2
Cel	Symbol			Pro	pagation D		meter		
		t O	KCL	t O	KCL	n KCL2	CDR2		Path
		0.250	0.060	0.399	0.084	KULZ	CDRZ	-	A to X
		0.230	0.000	0.533	0.004				Alox
								1	
A1	^						1		
A1 ——— A2 ———	b x								
Аз ——									
							1		
							1		
	,	Paramete	er				Symbol		Typ (ns) *
						1			
	Input Loading					- 1		l	
Pin Name	Factor (lu)					l			
A	1								
						1			
						1		1	
Pin Name	Output Driving Factor (lu)					1			
Х	14								
		* Minimu	m values fo	r the typical	operating o	condition.			
		The val		worst case	operating o	ondition a	re given by th	ne ma	ximum delay
	<u> </u>								
C21-N3N-E0	Sheet 1/1							$\neg$	Page 2-4
									F 40H 2-4

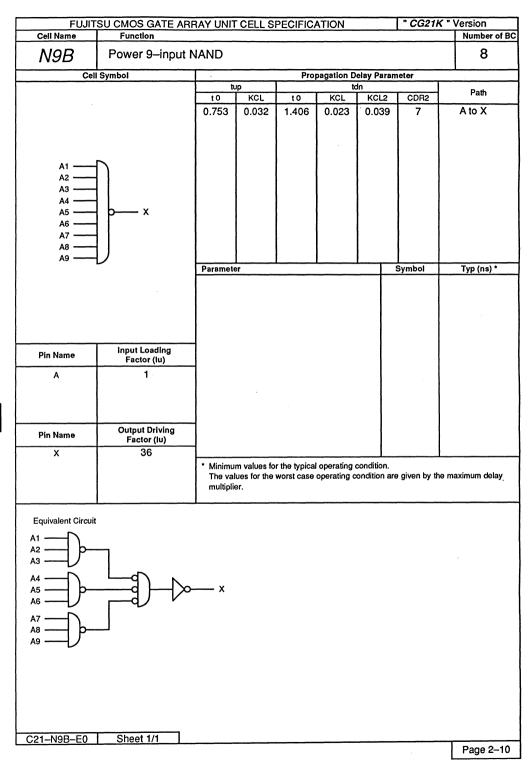
FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		T " CG21F	("\	/ersion
Cell Name	Function								Number of BC
N3B	Power 3-input N	IAND							3
	l Symbol	r		Dro	pagation D	elev Dere	meter		
. Cei	i Symbol	t	J <b>p</b>	Pro		in Paran	erei		
		t O	KCL	t O	KCL	KCL2	CDR2		Path
		0.680	0.032	0.898	0.017				A to X
		]							
				'			1 .		
							1 1		
	<b>~</b>								
A1 ——— A2 ———	Ъ— ×	Ì					!		
A3 — ) — ^									
				]					
		Paramete	lj er			└──Т	Symbol		Typ (ns) *
			*						
						- 1			
•		ĺ			•	1			
		Ì				ł	1		
Pin Name	Input Loading Factor (lu)					- 1			
A	1	1				- 1			
İ		j				1			
į									
						- 1	{		
Pin Name	Output Driving Factor (lu)					ı			ļ
×	36								
		* Minimu	m values for	the typical	operating of	ondition.			
		The val	ues for the v	worst case	operating o	ondition ar	e given by th	e ma	ximum delay
	•	multiplie	ar.						
•									
C21-N3B-E0	Sheet 1/1								
		•						L	Page 2–5

FILIIT	SU CMOS GATE ARF	TIMIT VAS	CELLS	PECIFIC	ATION		" CG21K	" Version
Cell Name	Function	IAT OINT	OLLL 3	LOII 107	ATION		<u> </u>	Number of BC
N4N	4-input NAND							2
Cel	Symbol			Pro	pagation D	elay Paran	neter	
			ıp		to	dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		0.298	0.060	0.428	0.106		<b>1</b>	A to X
					[			
					İ .	j	1 1	
						l		
						Ì	1 1	
A1							1 1	
A2	р—— х						1 1	
Аз ——							<b>!</b>	
A4 ——						ļ		
						l		
				L	L	L	<u> </u>	
		Paramete	er				Symbol	Typ (ns) *
							1	
							1	
							}	
						l		
						ļ	į	
Pin Name	Input Loading Factor (lu)							
Α	1					i		
^	•							
						1	İ	
						- 1		
	Outsid Delutes					- 1	1	
Pin Name	Output Driving Factor (lu)					ı		
X	10						1	
		* Minimu	m values fo	r the typical	operating	condition.		
		The val	ues for the	worst case	operating o	ondition are	given by the	maximum delay
		multiplie	er.					
C21-N4N-E0	Sheet 1/1							
32 LO								Page 2-6

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL SI	PECIFICA	ATION		] * C	G21K	" Version
Cell Name	Function								Number of BC
N4B	Power 4-input N	IAND							4
Cell	Symbol			Pro	pagation D		rameter		
		t O	IP KCL	t O	KCL	In KCL	o I cr	DR2	Path
		0.733	0.032	1.003	0.017	KOL	<del>\ \</del>	112	A to X
		000	0.002		0.017		- 1		
							į		
						1			
	•						İ		
A1	$\bigcap$					Ì	İ		
A2 A3									
A4	J						ı		
'									
		Paramete	er				Symb	ol	Typ (ns) *
						1			
								j	
						- 1			
Pin Name	Input Loading								
Α	Factor (lu)							-	
^	•								
						- 1			
Pin Name	Output Driving								
X	Factor (lu)								
^	36	* Minimu	m values for	r the typical	operating o	condition	············		
		The val	ues for the	worst case	operating o	ondition	are give	n by the	maximum delay
		multiplie	er.						
		L							
C21-N4B-E0	Sheet 1/1								Dags 0. 7
									Page 2-7

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function						·	Number of BC
N6B	Power 6-input N	IAND						5
Cell	Symbol			Proj	pagation D	elay Param	neter	
			p			in		Path
A1 A2 A3	x	0.726	ксL 0.032	1.069	0.017	0.034	7	A to X
A4 ————————————————————————————————————								
		Paramete	r			٠ .	Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
Α	1					- 1		
Pin Name	Output Driving Factor (lu)							
х	36	Minimul The val multiplie		r the typical worst case	operating o	condition. ondition are	given by the	maximum delay
Equivalent Circuit A1 A2 A3 A4 A5 A6		x						
C21-N6B-E0	Sheet 1/1			<del>,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,</del>		· · · · · ·		Page 2–8

FUET	CH CMCC CATE ADD	TIMI VAC	CELLO	DEOIEIO	ATION		" CC21V	"Varaian
Cell Name	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K"  I Name Function							Number of BC
N8B	Power 8-input NAND						6	
Cell	Symbol	Propagation Delay Parameter						
		t O	IP KCL	t O	KCL	in KCL2	CDR2	Path
		0.759	0.032	1.168	0.017	0.034	7	A to X
		0.700	0.002		0.017	0.00	'	
A1	$\Gamma$							
A2								
A3 ———							[ ]	
A5	р ×						!!!	
A6								
A7 ————————————————————————————————————	)							
1		Paramete	).		l	<del></del>	Symbol	Typ (ns) *
		- ununion	·•				,	.,,,,
}						1		
							1	
						į	Į.	
		1				ļ		
Pin Name	Input Loading Factor (lu)							
Α	1	1				i		
		1				- 1		
Pin Name	Output Driving Factor (lu)	l						
x	36							
				the typical				
		The value multiplie		worst case	operating o	ondition are	given by the	maximum delay
Equivalent Circuit								
A1 A2								
A3 — —								
A4								
A5								
A6								
A8 ——								
C21-N8B-E0	Sheet 1/1		ŧ					
<u> </u>								Page 2-9



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version								" Version	
Cell Name								Number of BC	
NCB	Power 12-input NAND							10	
Cel	Propagation Delay Parameter								
		t O	KCL	t O	KCL	In KCL2	CDR2	Path	
		0.805	0.032	1.512	0.023	0.039	8	A to X	
		0.000	0.002	1.512	0.020	0.000	"	71.0 7	
							] ]		
A1	Ŋ						}		
A2		ļ					1		
A3 ———									
A5									
A6	l b х								
A7 ———		]					1		
A9 —									
A10					İ				
A11		Paramete	r		L	<u> </u>	Symbol	Typ (ns) *	
A12	D .								
						1	İ		
						ĺ	İ		
							Ì		
	<b>,</b>	1					İ		
Pin Name	Input Loading Factor (lu)	ĺ							
A	1					İ			
_ ^	'					Ì	ĺ		
Pin Name	Output Driving	Ì				İ	l		
	Factor (lu)					1	- 1		
X	36								
		Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay							
		multiplier.							
	<u> </u>	l							
Equivalent Circuit									
1 -									
A1 A2									
A3 — P	7								
A4 ————————————————————————————————————									
A5	La, .								
$ \begin{array}{c c} A6 & & & \\ A7 & & & \\ \end{array} $									
A7	$\vdash \triangleleft \vee$								
A9 —									
A10 ————————————————————————————————————									
A12 ——   F									
A12 ————————————————————————————————————									
C21-NCB-E0	Sheet 1/1								
								Page 2-11	

ELLIN	CHICKOS GATE ADD	THALLVAG	CELL S	DECIEIC	ATION		" CG21K	" Varsian
Cell Name	ITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" \ Function							Number of BC
NGB	Power 16-input NAND						11	
								-L
		tu			to	dn		Path
		t 0 0.812	KCL 0.032	1.835	0.028	KCL2 0.039	CDR2 8	A to X
A1 ————————————————————————————————————	> x	Paramete		1.835	0.028		Symbol	Typ (ns) *
A16 ————————————————————————————————————	Input Loading Factor (Iu)							
Pin Name X	Output Driving Factor (lu) 36							
^	30	Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						maximum delay
A1 ————————————————————————————————————	Sheet 1/1	×						Page 2–12

### **NOR Family**

Page	Unit Cell Name	Function	Basic Cells
3–31	R2N	2-input NOR	1
3–32	R2B	Power 2-input NOR	3
3–33	R2K	Power 2-input NOR	2
3–34	R3N	3-input NOR	2
3–35	R3B	Power 3-input NOR	3
3–36	R4N	4-input NOR	2
3–37	R4B	Power 4-input NOR	4
3–38	R6B	Power 6-input NOR	5
3–39	R8B	Power 8-input NOR	6
3–40	R9B	Power 9-input NOR	8
3–41	RCB	Power 12-input NOR	10
3–42	RGB	Power 16-input NOR	11

ELLIIT	SH CMOS CATE ADI	ZAV LINII	CELLS	DECIEIO	ATION		" CG21k	" Version
Cell Name	SU CMOS GATE ARE Function	IAT UNI	OLLL S	LOIFIU	TION		I CGZ IN	Number of BC
R2N	2-input NOR							1
Cell	Symbol			Pro		elay Param	neter	
		t O	KCL	t O	KCL	dn KCL2	CDR2	Path
		0.191	0.106	0.254	0.039	0.050	4	A to X
A1 A2	A2 Input Loading		er				Symbol	Typ (ns) *
Pin Name	Factor (lu)							
A	1							
Pin Name	Output Driving Factor (lu)							
X	14	* Minimu The val multipli		r the typical worst case	operating o	condition. condition are	given by the	e maximum delay
C21-R2N-E0	Sheet 1/1							<del></del>
C21-R2N-E0	Sheet 1/1							Page 3-1

	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
R2B	Power 2-input N	IOH						3
Cell	Symbol			Pro	pagation D		eter	
		t O	JP KCL	t O	KCL	n KCL2	CDR2	Path
		0.720	0.032	0.660	0.017			A to X
A1	× *							
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu) 1							
Pin Name X	Output Driving Factor (lu) 36	* Minimu	m values fo	r the typical	operating o	condition.		
		The val multipli	ues for the	worst case	operating c	ondition are	given by the	e maximum delay
C21-R2B-E0	Sheet 1/1	A						Page 3-2

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
R2K	Power 2-input N	NOR						2
Cell	l I Symbol	Γ		Pro	pagation D	elay Parai	meter	
			ıp		to	n		Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	A to X
		0.214	0.051	0.261	0.028			AIOA
					l			
	_							
A1 ——— A2 ———	Ď∞— ×							
AZ -								
					İ			
		Paramete	er				Symbol	Typ (ns) *
						1		
Pin Name	Input Loading Factor (lu)							
Α	2	i						
	~							
Pin Name	Output Driving Factor (lu)							
×	36	1						
		* Minimu	m values fo	r the typical	operating of	condition.		
		The val		worst case	operating c	ondition ar	e given by the	maximum delay
		mulaphe	JI.					
C21-R2K-E0	Sheet 1/1							
								Page 3–3

FILIT	SU CMOS GATE ARF	TIMIT YAS	CELLS	PECIFICA	ATION		" CG21k	( " Version
Cell Name	Function	IAI CIVII	OLLLO	LOII 107	111011		OGZ	Number of BC
R3N	3-input NOR							2
Cell	Symbol			Proj	pagation D		neter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
A1 ——— A2 ——— A3 ———	<b>&gt;</b> — x	0.399	0.151	0.268	0.039	0.056	4	A to X
ı		Paramete	er			<u> </u>	l Symbol	Typ (ns) *
	Input Loading							
Pin Name	Factor (lu)							
A	1						-	
Pin Name	Output Driving Factor (lu)							
х	10	* Minimu The val multiplie		r the typical worst case	operating o	condition. ondition are	e given by th	e maximum delay
C21-R3N-E0	Sheet 1/1			,, <del></del>		,		Page 3–4

FILUT	CHICHOS CATE ADI	DAY LINUT	CELLO	DECIFIC	ATION		" CG211	/ " \/o	mion
Cell Name	SU CMOS GATE ARE	TAT UNIT	CELL SI	PECIFICA	ATION		CGZ11		lumber of BC
R3B	Power 3-input N	NOR							3
Cell	Symbol			Pro	pagation D		neter		
		t O	IP KCL	t O	KCL	ln KCL2	CDR2		Path
		1.050	0.032	0.726	0.017	KOLZ	ODINZ	A	to X
			0.002	0	0.0				
			·						
A1	A						}		
A2	├×						Ì		
АЗ ——	D								
		Paramete				L .	Symbol	T	yp (ns) *
		- unumer	<u>.                                    </u>			<del></del>	.,	•	, p ()
		İ							
	r	1							
Pin Name	Input Loading Factor (lu)								
Α	1	1							
		Ì							
Pin Name	Output Driving Factor (lu)					ĺ			
x	36	ļ			<u></u>				
		* Minimu	m values for	r the typical	operating o	xondition.	given by th	o mavin	num delav
		multiplie		WOISt Case	operating o	onomon are	given by a	o maxii	nom ociay
		<u> </u>							
C21-R3B-E0	Sheet 1/1							٠.	2000 0 5
									Page 3-5

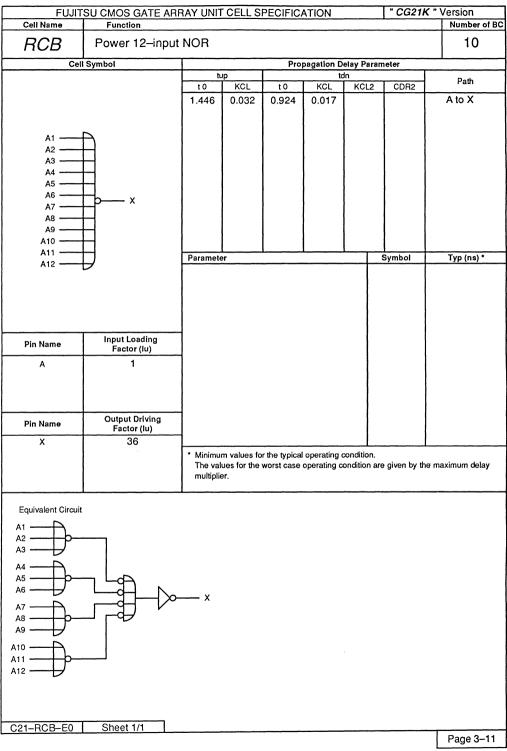
FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL S	PECIFICA	ATION		" CG21F	( " Version
Cell Name	Function							Number of BC
R4N	4-input NOR							2
Cel	l Symbol			Proj	pagation D		neter	
		t O	JP KCL	t O	KCL	ln KCL2	CDR2	Path
A1 A2 A3	<b>&gt;</b> ×	0.589	0.197	0.268	0.039	0.062	4	A to X
A4	<del>D</del>							
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading							
	Factor (lu)	-				1		
Α								
Pin Name	Output Driving Factor (lu)	1						
X	6	* Minimu The val multiplie		r the typical worst case	operating o	condition. condition are	given by th	e maximum delay
	Sheet 1/1							
C21-R4N-E0								

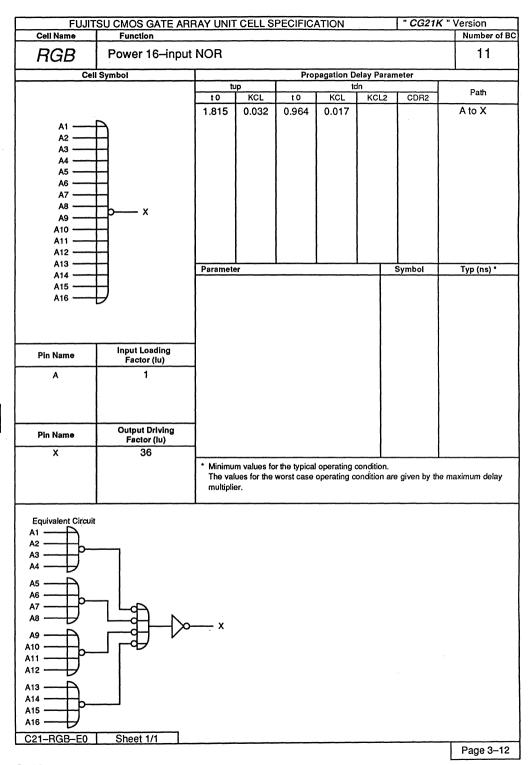
FILIIT	SU CMOS GATE ARF	" Version						
Cell Name	Function	IAT CIVIT	OLLL O	LOII 107	TION		002	Number of BC
R4B	Power 4-input N	IOR						4
Cel	Symbol			Prop	pagation D		eter	
			ib KCI	••		ln KCI 2	CDDa	Path
A1 ————————————————————————————————————	×	1.320	KCL 0.032	0.706	0.017	KCL2	CDR2	A to X
Pin Name	Input Loading Factor (lu)							
A	1							
Pin Name	Output Driving Factor (lu)							
X	36	* Minimu The val multiplie		r the typical worst case	operating o	condition. ondition are	given by the	e maximum delay
C21-R4B-E0	Sheet 1/1							
JE1 1170 EU								Page 3-7

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function		02220	2011 101				Number of BC
R6B	Power 6-input N	IOR						5
Cell	Symbol							
		t O	IP KCL	t O	KCL	in KCL2	CDR2	Path
A1 ————————————————————————————————————	A2 ————————————————————————————————————		0.032	0.786	0.017		Symbol	A to X
Pin Name	Input Loading							
Pin Name X	Output Driving Factor (Iu) 36	* Minimu The val multiplic	ues for the	r the typical worst case	operating o	condition.	e given by the	maximum delay
Equivalent Circuit A1 A2 A3 A4 A5 A6		— х						
C21-R6B-E0	Sheet 1/1							T Day of
								Page 3–8

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K											
Cell Name	Function	IAT UNIT	OLLL S	LOIFICA	TION			Number of BC			
R8B	Power 8-input N	IOR						6			
Ce	Il Symbol			Pro	pagation D		neter				
		t O	KCL	t O	KCL	fn KCL2	CDR2	Path			
A1 A2	Ð	1.498	0.032	0.799	0.017			A to X			
A3 ————————————————————————————————————	A3 ————————————————————————————————————		er				Symbol	Typ (ns) *			
	Input Loading										
Pin Name	Factor (lu)						1				
A	1										
Pin Name	Output Driving Factor (lu)										
Х	36	* Minimul The val multiplie	ues for the	r the typical worst case	operating o	∞ndition. ondition are	given by the	e maximum delay			
Equivalent Circuit A1 A2 A3 A4 A5 A6 A7 A8		x									
C21-R8B-E0	Sheet 1/1							Page 3–9			

FILIT	SU CMOS GATE ARF	TIALL VA	CELLS	DECIEIC	ATION		" CG21K	" Version
Cell Name	Function Function	IAT UNIT	OLLL 3	r LOIFIO	ATION		OUZIK	Number of BC
R9B	Power 9-input N	IOR						8
Cell	l Symbol			Proj	pagation D		neter	
		t O	KCL	t O	KCL to	in KCL2	CDR2	Path
		1.314	0.032	0.891	0.017	NOLE	OBITE	A to X
								·
					1			
					į			
A1	<b>P</b> 1							
A2 ——— A3 ———								
A4	<del>-</del>							
A5 ——— A6 ———	×							
A7							1	
A8	H					İ		
A9 ——	$\Theta$	Paramete	r		<u> </u>	<u> </u>	Symbol	Typ (ns) *
	Input Loading							
Pin Name	Factor (lu)							
A	1							
						1		
							.	
	Output Driving					ł		
Pin Name	Factor (lu)					- 1		
Х	36						<u> </u>	
		* Minimu The val	m values fo	r the typical worst case	l operating o	condition.	aiven by the	maximum delay
		multipli			oporating o	01101110111011	y g	
	L	L						
Equivalent Circuit								
A1 —								
A2 — — —	7							
A3 —								
A4 A5	~	x						
A6		^						
A7 ——	1							
A8 — — — —								
A9 —								
C21-R9B-E0	Sheet 1/1							Page 3-10
								raye 3-10





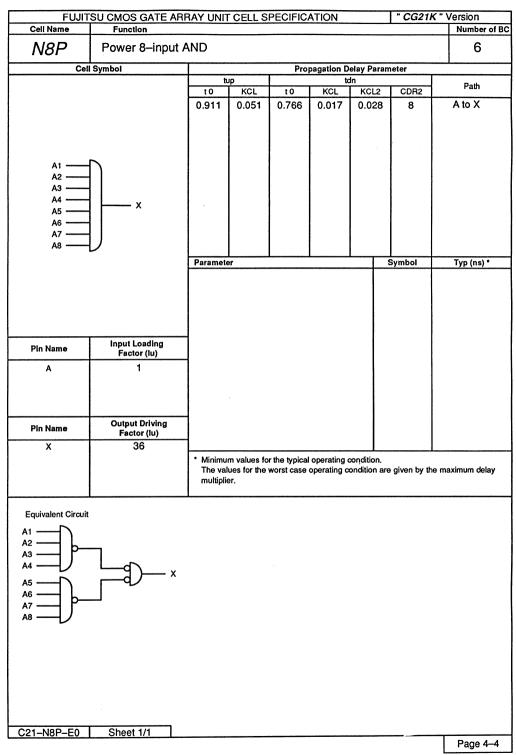
## **AND Family**

	Unit Cell		Basic
Page	Name	Function	Cells
3-45	N2P	Power 2-input AND	2
3–46	N3P	Power 3-input AND	3
3–47	N4P	Power 4-input AND	3
3–48	N8P	Power 8-input AND	6

FUJIT	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function			N				Number of Bo
N2P	Power 2-input	AND						2
Cel	l Symbol	I		Pro	pagation D	elay Param	neter	
			ip			in		Path
		t 0	KCL	t0	KCL	KCL2	CDR2	A to X
		0.535	0.032	0.456	0.017	0.028	′	Alox
		1						
							i i	
	_							
A1	)—x	1						
A2	V							
		1	·				1	
		Paramete	er				Symbol	Typ (ns) *
						1		
Pin Name	Input Loading	1						
	Factor (lu)	4						
Α	1							
		1						
	Output Driving	1					ł	
Pin Name	Factor (lu)							
x	36	ļ						
		* Minimu The val	m values fo	r the typical worst case	operating o	condition. ondition are	aiven by the	maximum delay
		multipli			operating o	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	g	
		<u> </u>						
C21-N2P-E0	Sheet 1/1							
(:ソ1ーNソピードロ								

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFICA	ATION		" CG21k	( " Version
Cell Name	Function							Number of BC
N3P	Power 3-input A	ND						3
Cell	Symbol			Proj	pagation D		neter	
		t O	KCL	t O	KCL	In KCL2	CDR2	Path
A1 ————————————————————————————————————	D ×	0.700	0.032	0.568	0.017	0.028	7	A to X
					L	<u> </u>	<u> </u>	
ļ.		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
Α	1							
Pin Name	Output Driving							
×	Factor (lu)					l		
^	30	* Minimu The val multiplie	ues for the	r the typical worst case	operating o	condition. ondition ar	e given by th	e maximum delay
C21-N3P-E0	Chast 1th							
UZI-NSP-EU	Sheet 1/1							Page 4-2

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL SI	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
N4P	Power 4-input A	ND						3
Cell	Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
A1 A2 A3	×	0.838	0.032	0.627	0.017	0.028	8	A to X
A4							1 1	
'							1 1	
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
Α	1							ļ
Pin Name	Output Driving Factor (Iu)							
X	36						L	
		* Minimur The valumultiplie		r the typical worst case	operating o	condition. ondition are	e given by the	maximum delay
C21-N4P-E0	Sheet 1/1							
021-1441-LU	Check I/I		· · · · · · · · · · · · · · · · · · ·					Page 4-3



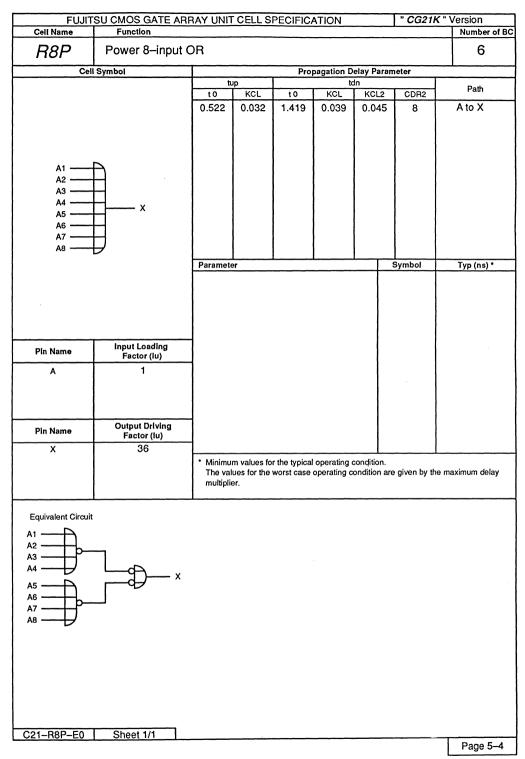
## **OR Family**

	Unit Cell		Basic
Page	Name	Function	Cells
3-51	R2P	Power 2-input OR	2
3–52	R3P	Power 3-input OR	3
3–53	R4P	Power 4-input OR	3
3-54	R8P	Power 8-input OR	6

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
R2P	Power 2-input 0	OR						2
Cel	l Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
		0.416	0.032	0.601	0.023	0.034	8	A to X
A1 ——— A2 ———	<b>)</b> —×	Paramete	<b>27</b>				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)						ĺ	
A	1	1				İ	ļ	
	·							
Pin Name	Output Driving Factor (lu)							
X	36	* Minimui The val multiplie		r the typical worst case	operating o	condition. ondition are	given by the	e maximum delay
C21-R2P-E0	Sheet 1/1							Page 5–1

FUJIT	SU CMOS GATE ARI	TINU YAF	CELLS	PECIFICA	ATION		" CG211	K" V	ersion/
Cell Name	Function								Number of BC
R3P	Power 3-input (	OR							3
Cel	l Symbol			Pro	pagation D		neter		
		t O	KCL	t O	KCL to	n KCL2	CDR2		Path
		0.475	0.032	0.970	0.028	0.039	8		A to X
		l							
		i			ŀ				
		İ					1		
A1	4						1	ĺ	
A2	<del>                                     </del>						1		
A3 ——	Ð								
		Paramete	<u> </u>	L	<u> </u>	L	Symbol		Tun (na) t
		Paramete	71				Symbol	-	Typ (ns) *
						1			
		l							
		İ							
Din Nama	Input Loading	İ							
Pin Name	Factor (lu)	1							
Α	1	İ							
		ļ							
Pin Name	Output Driving	1							
×	Factor (lu)	1				1			
		* Minimu	m values fo	r the typical	operating	condition.			
		The val		worst case	operating o	ondition ar	e given by the	ne ma	ximum delay
	1								
C21-R3P-E0	Sheet 1/1								
· · · · · · · · · · · · · · · · · · ·								- 1	Page 5-2

	ISU CMOS GATE AR	RAY UNIT	CELL SI	PECIFICA	ATION		" CG21F	( " Version
Cell Name	Function							Number of B
R4P	Power 4-input	OR						3
Ce	li Symbol	T		Proj	pagation D	elay Param	neter	
			ıp		to	ln		Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	A to X
		0.475	0.032	1.333	0.034	0.045	8	AIUA
					•		1	
					Ì			
A1	A							
A2 A3	<u> </u>				ĺ			
A4 ——	<del>D</del>				l			
		Paramete	er				Symbol	Typ (ns) *
		]				l		
						İ		
Pin Name	Input Loading	1						
	Factor (lu)	4				l		
Α	1						i	
	Output Driving	-				j		
Pin Name	Factor (lu)	]						
×	36	ļ				L		
		* Minimu	m values for	r the typical worst case	operating of	ondition. Ondition are	aiven by th	e maximum delay
		multiplie			-p		. <b>.</b>	<b>.</b>
· · · · · · · · · · · · · · · · · · ·	<u></u>	<u> </u>						
C21-R4P-E0	Sheet 1/1							



## **EXNOR/EXOR Family**

Page	Unit Cell Name	Function	Basic Cells
3–57	X1N	Exclusive NOR	3
3-58	X1B	Power Exclusive NOR	4
3–59	X2N	Exclusive OR	3
3-60	X2B	Power Exclusive OR	4
361	X3N	3-input Exclusive NOR	5
3-62	ХЗВ	Power 3-input Exclusive NOR	6
3-63	X4N	3-input Exclusive OR	5
3-64	X4B	Power 3-input Exclusive OR	6

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFICA	ATION		" CG21k	(" Version
Cell Name	Function							Number of BC
X1N	Exclusive NOR							3
Cel	Symbol			Proj	pagation D		neter	
		t O	IP KCL	t O	KCL	ln KCL2	CDR2	Path
		0.614	0.106	0.508	0.062	0.073	4	A to X
A1 ————————————————————————————————————	<b>}</b> ∘—×	Paramete		0.508	0.062		Symbol	Typ (ns) *
Pin Name	Input Loading							
A	Factor (lu)					l	l	
Pin Name  X  Equivalent Circuit A1	Output Driving Factor (Iu) 18	* Minimur The val multiplie	ues for the	r the typical	operating o	condition. condition are	given by the	e maximum delay
A2 C21-X1N-E0	Sheet 1/1	x						Page 6–1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name X1B	Function Power Exclusive	NOR				<del></del>		Number of BC
	Symbol			Pro	pagation D	elav Parar	neter	
		tu			to	ln		Path
A1 ——	Po— ×	0.786	кс <u>ь</u> 0.032	0.937	0.023	0.039	7 7	A to X
A2	Po *	Paramete	r				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
Α	2							
Pin Name	Output Driving Factor (lu)							
X	36	* Minimur The valu multiplie	ues for the	r the typical worst case	operating o	condition.	e given by the	maximum delay
Equivalent Circuit A1 A2		<b>&gt;</b>	×					
C21-X1B-E0	Sheet 1/1		and the second second second second second second second second second second second second second second seco					Page 6–2

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	( " Version
Cell Name	Function							Number of BC
X2N	Exclusive OR							3
Cel	l Symbol			Pro	pagation D		neter	
		10	KCL	t O	KCL	in KCL2	CDR2	Path
		0.588	0.106	0.621	0.062	0.073	4	A to X
A1 ————————————————————————————————————	<b>)</b> ——×							
		Paramete	er				Symbol	Typ (ns) *
	T							
Pin Name	Input Loading Factor (lu)							
Α	2							
Pin Name	Output Driving Factor (lu)							
X	14	* Minimu The val multiplie		r the typical worst case	operating o	condition. condition are	given by th	e maximum delay
Equivalent Circuit A1 A2		- x						
C21-X2N-E0	Sheet 1/1							T n
								Page 6-3

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA	ATION		" CG21K	' Version
Cell Name	Function							Number of BC
X2B	Power Exclusive	OR						4
	   Symbol			Proj	pagation D	elay Paran	neter	
			ip		to	ln		Path
	,	t 0 0.759	KCL 0.032	t 0 0.865	KCL 0.023	KCL2 0.034	CDR2	A to X
		0.759	0.032	0.865	0.023	0.054	'	Alox
	,						l . l	
]				·				
A1 ——	<b>&gt;</b> —×							
A2 —	₽ <b>—</b> ^							
								:
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A	2							
	2.4.2.4					İ		
Pin Name	Output Driving Factor (lu)							
х	36							
		* Minimu	m values fo	r the typical worst case	operating o	condition. ondition are	given by the	maximum delay
		multiplie			- <b>,</b>		<b>.</b>	······································
		L	· · · · · · · · · · · · · · · · · · ·					
Equivalent Circuit								
A1 TO								
A2 + 1	L	N						
	- $           -$		- X					
	<del></del>							
C21-X2B-E0	Sheet 1/1							T = - :
								Page 6-4

								<del></del>
FUJIT Cell Name	SU CMOS GATE ARF	RAY UNII	CELL SI	PECIFICA	ATION		" CG211	( " Version Number of BC
		io NOD						
X3N	3-input Exclusiv	e NOR						5
Cell	Symbol			Pro	pagation D		eter	
		t O	KCL	t O	KCL	In KCL2	CDR2	Path
		1.439	0.106	1.228	0.062	0.073	4	A to X
			0.700		0.002	0.070		
A1 —	A							
A2 —	├-b ×							
A3 ——	$\Theta$	1						
		Paramete	r				Symbol	Typ (ns) *
		1				- 1	į	1
		ì				Ì		
						l		Ì
		•						
	Input Loading	1				1		j
Pin Name	Factor (lu)					1		
A	2							
		1						
	Control Dalata	1						
Pin Name	Output Driving Factor (lu)							
x	18							
		* Minimu	n values for	the typical	operating of	ondition.	ماه بنظ مصنات	e maximum delay
		multiplie		worst case	operating o	ondition are	given by th	e maximum delay
		<u> </u>						
Equivalent Circuit								
A2 A3								
	10							
A1	11_b x							
	10							
C21-X3N-E0	Sheet 1/1							Page 6 F
								Page 6-5

FILIT	SUCMOS GATE ARE	ZAY LINIT	CELLS	PECIFICA	ATION		" CG21K	" Version
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG2 Cell Name Function					- OGZ III	Number of BC		
X3B	Power 3-input Exclusive NOR					6		
Cell Symbol				Proj	pagation D		neter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
		1.393	0.032	1.789	0.023	0.039	7	A to X
A1 ————————————————————————————————————	*	Paramete		1.709	0.023		Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A	2							
	Output Driving							
Pin Name	Factor (lu)							
X	36	* Minimu The val multipli		r the typical worst case	operating o	condition. ondition are	given by the	maximum delay
Equivalent Circuit A2 A3 A1	₩ ×							
C21-X3B-E0	Sheet 1/1			.,				Page 6-6

FILLET	CHICHOC CATE AD	DAY LINIT	CCLLC	DECITIO	ATION		" CC214	C" Vorsion
Cell Name	ISU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K"					Number of BC		
X4N	3-input Exclusive OR					5		
Cel	l Symbol	I		Pro		elay Paran	eter	
			JP KOL	10	KCL to	dn L KOLO	ODDO	Path
		1.492	0.106	t 0 1.340	0.062	0.073	CDR2	A to X
		1.452	0.100	1.540	0.002	0.073		Alox
		Ì						
A1 —	A		]			j		
A2 ————————————————————————————————————	×							
		Paramete	er		L		Symbol	Typ (ns) *
						1		
Pin Name	Input Loading	1						
	Factor (lu)	-				j		
A	2					1		
		_						
Pin Name	Output Driving Factor (lu)	1						
x	14	-						
		* Minimu	m values fo	r the typical	operating of	condition.		
		The val		worst case	operating o	ondition are	given by the	e maximum delay
Equivalent Circuit								
A2 —								
A3 — —								
L	<del>1D</del> ×							
A1	<del>-11/</del> ^							

C21-X4N-E0	Sheet 1/1

Cell Symbol  Cell Symbol  Propagation Delay Parameter  tup  to  10 KCL 10 KCL KCL2 CDR2  1.307 0.032 1.657 0.023 0.034 7 A  Parameter  Pin Name  Input Loading Factor (lu)  A 2  Pin Name  Output Driving Factor (lu)  X 36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit  A2  Equivalent Circuit  A2	rsion
Cell Symbol  Tropagation Delay Parameter  tup tdn  1.307 0.032 1.657 0.023 0.034 7 A  Parameter  Parameter  Symbol  Ty  Parameter  Pin Name Input Loading Factor (tu)  A 2  Pin Name Output Driving Factor (tu)  X 36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit  A2	Number of BC
Pin Name Input Loading Factor (tu)  A 2  Pin Name Output Driving Factor (tu)  X 36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.	6
Pin Name Input Loading Factor (lu)  A 2  Pin Name Output Driving X  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.	
Parameter  Parameter  Symbol  Ty  Pin Name  Input Loading Factor (lu)  A  2  Pin Name  Output Driving Factor (lu)  X  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit  A2	Path
Plin Name Input Loading Factor (lu)  A 2  Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit  A2	A to X
Pin Name Input Loading Factor (Iu)  A 2  Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit  A2	
Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit  A2	Гур (ns) *
Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit  A2	
Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit A2	
Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit  A2	
X     36      * Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit  A2	
The values for the worst case operating condition are given by the maxim multiplier.  Equivalent Circuit	
A2 — <del>                                    </del>	mum delay
A3 — H X	
C21–X4B–E0 Sheet 1/1	Page 6–8

## **AND-OR-Inverter Family**

	Unit Cell		Doolo
Page	Name	Function	Basic Cells
3–67	D23	2-wide 2-AND 3-input AOI	2
3-68	D14	2-wide 3-AND 4-input AOI	2
3-69	D24	2-wide 2-AND 4-input AOI	2
3-70	D34	3-wide 2-AND 4-input AOI	2
3–71	D36	3-wide 2-AND 6-input AOI	3
3–72	D44	2-wide 2-OR 2-AND 4-input AOI	2

FILIT	SU CMOS GATE ARF	TIMIT VA	CELLS	PECIFICA	ATION		" CG211	(" Version
Cell Name	Function	AT UNIT	OLLL SI	LOIFIU	TION		1 00211	Number of BC
D23	2-wide 2-AND	3_innut	AOI					2
		- Input						
Cell	Symbol			Pro	pagation D	elay Param In	neter	
		t O	IP KCL	t O	KCL	KCL2	CDR2	Path
		0.351 0.179	0.106 0.083	0.399 0.218	0.062 0.039	0.056	4	A to X B to X
A1 A2 B	<b>Т</b> р-— х							
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (Iu)							
A B	1							
_	Output Driving							
Pin Name	Factor (lu)							
Х	14							
							given by th	e maximum delay
C21-D23-E0	Sheet 1/1							
021-020-E0	Oneet I/T							Page 7-1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function	1711 01111	OLLLO	2011 107	111014			Number of BC
D14	2-wide 3-AND	4–input	AOI					2
Cel	Symbol			Proj	pagation D		neter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
A1 A2 A3 B	×	0.429 0.155	0.106 0.073	0.406 0.210	0.084 0.039	0.095 0.056	4 4	A to X B to X
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A B	1							
Pin Name	Output Driving Factor (lu)							
х	14						given by the	maximum delay
C21-D14-E0	Sheet 1/1							
<u> </u>	<u> </u>							Page 7–2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Ve											
Cell Name	Function				THOIT			Number of BC			
D24	2-wide 2-AND	4—input	AOI					2			
Cell	Symbol			Proj	pagation D		neter				
		t O	KCL	t O	KCL	in KCL2	CDR2	Path			
A1 ————————————————————————————————————	×	0.256 0.322	0.083 0.083	0.363 0.486	0.062 0.062			A to X B to X			
		Paramete	L		L	L	Symbol	Typ (ns) *			
		raiamete					Symbol	Typ (IIS)			
Pin Name	Input Loading Factor (lu)										
A B	1										
Pin Name	Output Driving Factor (lu)										
X	14	Minimul     The val     multiplie	ues for the	r the typical worst case	operating o	condition. condition are	e given by the	maximum delay			
C21-D24-E0	Sheet 1/1							Page 7–3			

FUJIT	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version										
Cell Name	Function							Number of BC			
D34	3-wide 2-AND	4–input	AOI					2			
Cell	Symbol			Pro	pagation D		neter				
		t O	IP KCL	t O	KCL	fn KCL2	CDR2	Path			
		0.548 0.298	0.151 0.128	0.428 0.254	0.067 0.039	0.056	4	A to X B to X			
A1 A2 B1 B2	×										
		Paramete	er				Symbol	Typ (ns) *			
Pin Name	Input Loading Factor (lu)										
A B	1										
Pin Name	Output Driving Factor (lu)										
X	10						e given by th	ne maximum delay			
C21-D34-E0	Sheet 1/1							Page 7–4			

Cell Name	rsion	CG21K"\		J	ATION	CIFIC	I SE	r C.F	RAY LINI	MOS GATE ARE	ITS	FULID
Cell Symbol Propagation Delay Parameter    tup   tdn	Number of BC	OGZ / K	L	`	ATIO	_011 10		0.	1711 0111		Ĭ	Cell Name
tup   tdn	3							AO	6-input	-wide 2-AND		D36
10 KCL 10 KCL KCL2 CDR2  0.369 0.106 0.421 0.062 0.470 0.106 0.508 0.062 0.560 0.106 0.595 0.062		er			pagatio	Pro				ool	ell S	Cel
0.369 0.106 0.421 0.062 0.470 0.106 0.508 0.062 0.560 0.106 0.595 0.062	Path	CDB3			T KC	• 0	<del>,  </del>					
B1	to X to X to X			52 52	0.00	0.421 0.508	06 06	0.	0.369 0.470		\	
C1 C2 C2 C3 C3 C3 C3 C3 C3 C3 C3 C3 C3 C3 C3 C3										L .,	<u> </u>	
			-	- 1	l		}			ρ x	Γ.	1 1-
Parameter Symbol 1											لر	
	yp (ns) *	nbol	s	1	·			er	Paramet			
Pin Name Input Loading Factor (Iu)										Factor (lu)		
A 1 1 C 1 1 C 1 C 1 C 1 C 1 C C C C C C										1 1 1		A B C
Pin Name Cutput Driving Factor (lu)									1		T	Pin Name
X 10      * Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the maximultiplier.	mum delay	ven by the ma	ndition. ndition are	ting co	l opera operati	he typica orst case	ues for or the v	lues i	The va	10		x
C21-D36-E0   Sneet 1/1										Sheet 1/1	7	C21-D36-E0

Cell Name	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K" V												
Cell Symbol   Symbol   Propagation Delay Parameter   Path		Function							Number of BC				
To   KCL   10   KCL   KCL2   CDR2   Path			-AND 4-	-input A			-		2				
10	Cel	l Symbol			Proj			neter					
D.494   0.151   0.457   0.062   0.050   A to X					10			CDB2	Path				
Pin Name Input Loading Factor (tu)  A 1 1 C 1  Pin Name Soutput Driving Factor (tu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-D44-E0 Sheet 1/1		6	0.494 0.494	0.151 0.151	0.457 0.370	0.062 0.062			B to X				
Pin Name Input Loading Factor (fu)  A 1 1		<u>М</u> —×											
Pin Name Input Loading Factor (fu)  A 1 1			L	L			L						
Pin Name   Factor (lu)			Paramete	er				Symbol	Typ (ns) *				
Pin Name   Factor (lu)								-					
Pln Name Output Driving Factor (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-D44-E0 Sheet 1/1	Pin Name	Factor (lu)											
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21-D44-E0   Sheet 1/1	В	1 1											
Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–D44–E0 Sheet 1/1	Pin Name	Output Driving Factor (lu)											
C21-D44-E0   Sheet 1/1	X	10	The val	ues for the	r the typical worst case	operating o	condition. ondition are	e given by th	ne maximum delay				
C21-D44-E0   Sheet 1/1													
I Page 7–6	U21-D44-E0	Sneet 1/1							Page 7-6				

## **OR-AND-Inverter Family**

Page	Unit Cell Name	Function	Basic Cells
3–75	G23	2-wide 2-OR 3-input OAI	2
3–76	G14	2-wide 3-OR 4-input OAI	2
3-77	G24	2-wide 2-OR 4-input OAI	2
3–78	G34	3-wide 2-OR 4-input OAI	2
3-79	G44	2-wide 2-AND 2-OR 4-input OAI	2

3

Cell Name	FUJIT	SU CMOS GATE ARE	RAY LINIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Name   Call Symbol   Name   Call Symbol   Name   Call Symbol   Name   Call Symbol   Name   Call Symbol   Name   Call Symbol   Name   Call Symbol   Name   Call Symbol   Name   Call Symbol   Name   Call Symbol   Name	Cell Name	Function		0222				1	Number of BC
Pin Name   Input Loading Factor (Iu)   X   18   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	G23	2-wide 2-OR 3-	-input C	Al					2
Pin Name Input Loading Factor (Iu)  A 1 1 18  Pin Name Output Driving Factor (Iu)  X 18  * Minimum values for the typical operating condition are given by the maximum delay multiplier.  * Minimum values for the worst case operating condition are given by the maximum delay multiplier.	Cel	l Symbol			Proj			neter	
Pin Name Input Loading Factor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					•0			LCDBa	Path
Pin Name Input Loading Factor (lu)  A 1 1 B 1  Pin Name Output Driving Factor (lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–G23–E0 Sheet 1/1	A2 —————	<u>_</u>	0.345	0.106	0.319	0.062	ROLE	COTTE	
Pin Name Input Loading Factor (lu)  A 1 1 B 1  Pin Name Output Driving Factor (lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–G23–E0 Sheet 1/1							l	1 1	
Pin Name Input Loading Factor (lu)  A 1 1 B 1  Pin Name Output Driving Factor (lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–G23–E0 Sheet 1/1			Paramete	er	L	L	<del>'                                    </del>	Symbol	Typ (ns) *
Pin Name Output Driving Factor (Iu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–G23–E0 Sheet 1/1									
Pin Name	Pin Name	Input Loading Factor (lu)							
Pin Name	A	1					ĺ		
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–G23–E0 Sheet 1/1		Output Driving							
The values for the worst case operating condition are given by the maximum delay multiplier.	X								
C21-G23-E0   Sheet 1/1			The val	ues for the				e given by the	a maximum delay
Page 8-1	C21-G23-E0	Sheet 1/1							Page 8-1
Page 8–1									Page 8-1

FUJIT	SU CMOS GATE ARI	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of B
G14	2-wide 3-OR 4	–input C	ΑI					2
	l I Symbol	T		Pro	pagation D	elay Paran	neter	L
			ıp		to	in		Path
		t0	KCL	t 0	KCL	KCL2	CDR2	
		0.571 0.119	0.156 0.060	0.377 0.377	0.062 0.062			⊶A to X B to X
		0.119	0.000	0.577	0.002			Вюх
		1					1	
_		l	İ				ļ . j	
A1 -			ŀ					
A2 A3	7		į					
	Ъ <u> </u>			}		i	1	
В	<b>−</b> レ							
		1		l				
		Paramete	er				Symbol	Typ (ns) *
		1					1	
							Į	
							ł	
	Input Loading	-			*	ļ		
Pin Name	Factor (lu)	]				l	l	
A B	1							
ь	'	İ				- 1		
	Output Driving	4						
Pin Name	Factor (lu)						1	
×	10							
		* Minimu	m values fo	r the typical	l operating	condition.	i b tb.	maximum delay
		multipli		WOISI Case	operating c	ondition an	e given by an	maximum delay
	<u> </u>	<u> </u>						
	Sheet 1/1							
C21-G14-E0								

Cell Name  G24  2-wide 2-OR 4-input OAI  Cell Symbol  Propagation Delay Parameter    10   KCL   10   KCL   CDR2   Path	FILIT	SUCMOS GATE ARE	RAY LINIT	CELLS	PECIFIC	ATION		" CG21	K" Version
Cell Symbol   Propagation Delay Parameter   Day   Da	Cell Name	Function	IAT OIT	OLLEG	LOITIO	ATION		OGZII	Number of BC
Pin Name Input Loading Factor (tu)  X  10  VIL 10  ROLL KOL2 ODR2  Path  0.429 0.106 0.348 0.062  Path  10  Path  10  ROLL 10  ROLL KOL2 ODR2  A to X  B to X  Parameter  Pin Name Factor (tu)  A 1  Pin Name Output Driving Factor (tu)  X  10  * Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum de multiplier.			-input C	ΙΑ					
Parameter  Parameter	Cel	Symbol			Pro			neter	
Perameter  Pin Name Input Loading Factor (tu)  A 1  Pin Name Output Driving Pactor (tu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.								CDBa	Path
Pin Name Input Loading Factor (lu)  A 1 1 B 1 1  Pin Name Output Driving Factor (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.	A2 ————————————————————————————————————	})—×	0.238	0.106	0.406	0.062			
Pln Name Input Loading Factor (iu)  Pln Name Output Driving Factor (iu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum demultiplier.			Paramete	L er	L	L	<u> </u>	Symbol	Typ (ns) *
Pin Name Output Driving Factor (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.									
Pin Name Output Driving Factor (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.	Pin Name	Input Loading Factor (lu)							
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.	A B	1							
• Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.	Pin Name	Factor (lu)							
C21_G24_F0   Sheet 1/1	•		The val	ues for the	r the typical worst case	operating c	condition.	given by th	e maximum delay
Page 8	C21-G24-E0	Sheet 1/1							Page 8–3

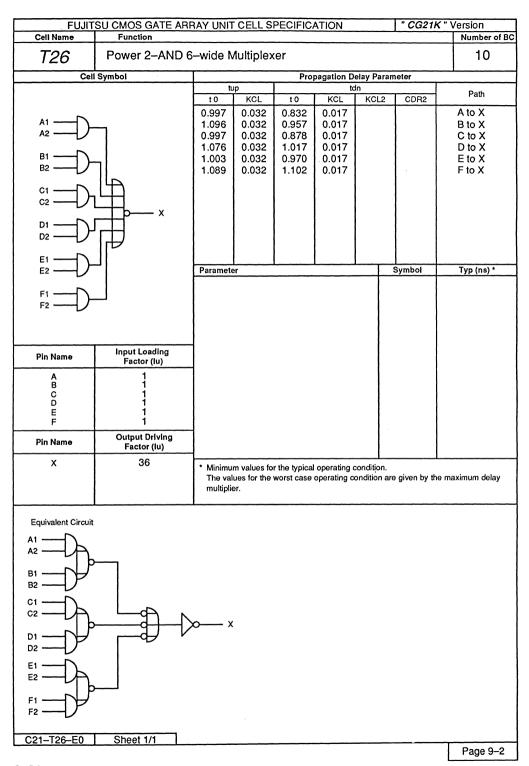
FUJIT	SU CMOS GATE ARF	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" V											
Cell Name	Function							Number of BC					
G34	3-wide 2-OR 4-	-input O	Al					2					
Cell	Symbol			Pro	pagation D		neter						
		t O	IP KCL	t O	KCL	in KCL2	CDR2	Path					
		0.452	0.106	0.406	0.084		1 1	A to X					
		0.333	0.069	0.261	0.073		1 1	B to X					
			:										
A1	٦												
	<b>九</b>												
B1 ————————————————————————————————————	ן א −×						1 1						
		Paramete	<u> </u> er	l	L	I	Symbol	Typ (ns) *					
						1							
	_						1						
Pin Name	Input Loading Factor (lu)						1						
A	1						1						
A B	i												
	Output Driving					}							
Pin Name	Factor (lu)												
×	10												
		The val	m values fo lues for the	r the typical worst case	operating o	condition. ondition ar	e given by the	maximum delay					
		multiplie	er.										
		l											
]													
. C21-G34-E0	Sheet 1/1												
								Page 8-4					

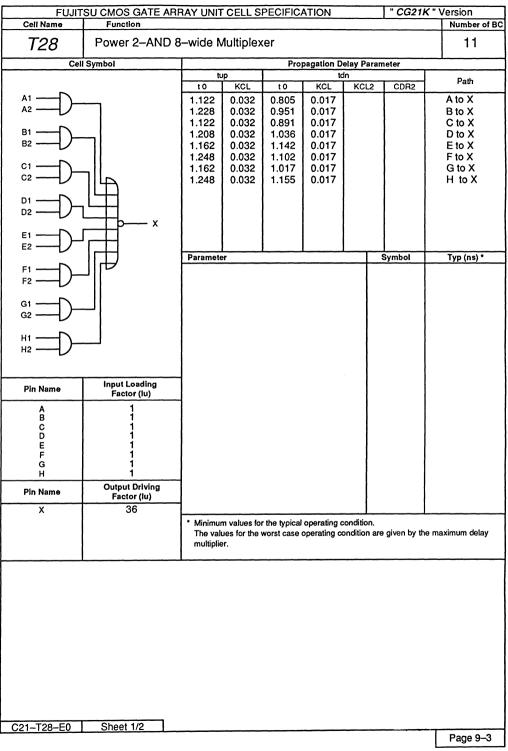
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Ve											
Cell Name	Function		OLLL O	2011 107	111011			Number of BC			
G44	2-wide 2-AND 2	2-OR 4	–input C	DAI				2			
Cell	Symbol			Proj		elay Paran	neter				
		t O	KCL	t O	KCL	n KCL2	CDR2	Path			
A1 A2 B C	<u>Dr</u> D—×	0.351 0.208 0.238	0.106 0.106 0.060	0.500 0.363 0.305	0.084 0.084 0.062	ROLE	CUMZ	A to X B to X C to X			
		Paramete	l er			<del>'                                    </del>	Symbol	Typ (ns) *			
Pin Name	Input Loading Factor (lu)										
A B C	1 1										
Pin Name	Output Driving Factor (lu)										
X	14	* Minimu The val multiplie		r the typical worst case	operating o	ondition. ondition are	given by the	maximum delay			
001 011 50	Shoot 1/4										
C21-G44-E0	Sheet 1/1						<del></del>	Page 8–5			
								9000			

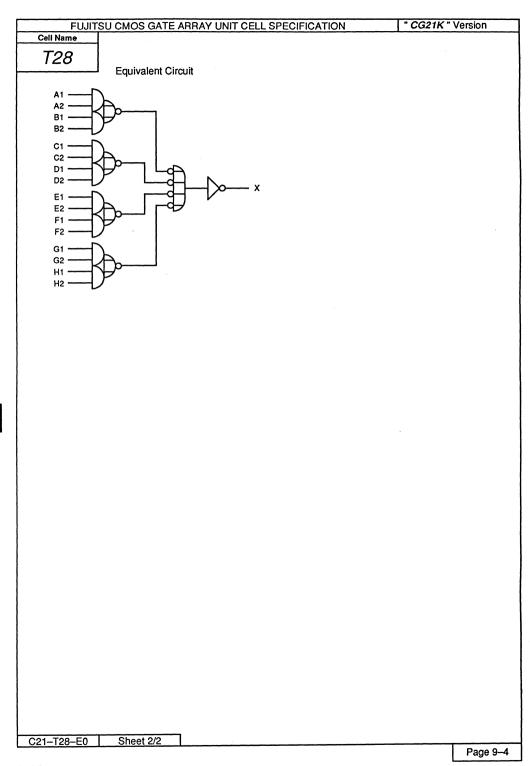
## **Multiplexer Family**

Page	Unit Cell Name	Function	Basic Cells
3–83	T24	Power 2-AND 4-wide Multiplexer	6
3-84	T26	Power 2-AND 6-wide Multiplexer	10
3–85	T28	Power 2-AND 8-wide Multiplexer	11
3-87	T32	Power 3-AND 2-wide Multiplexer	5
3–88	T33	Power 3-AND 3-wide Multiplexer	7
3-89	T34	Power 3-AND 4-wide Multiplexer	9
3–90	T42	Power 4-AND 2-wide Multiplexer	6
3-91	T43	Power 4-AND 3-wide Multiplexer	10
3–92	T44	Power 4-AND 4-wide Multiplexer	11
3–93	T54	Power 4–3–3–2 AND 4-wide Multiplexer	10
3–94	U24	Power 2-OR 4-wide Multiplexer	6
3–95	U26	Power 2-OR 6-wide Multiplexer	9
3–96	U28	Power 2-OR 8-wide Multiplexer	11
3–97	U32	Power 3-OR 2-wide Multiplexer	5
3–98	U33	Power 3-OR 3-wide Multiplexer	7
3–99	U34	Power 3-OR 4-wide Multiplexer	9
3-100	U42	Power 4-OR 2-wide Multiplexer	6
3-101	U43	Power 4-OR 3-wide Multiplexer	9
3-102	U44	Power 4-OR 4-wide Multiplexer	11

	COLLONGO CATE ADO	2437 1 15117	. 0511 0	DEOIE10	171011		" CC041	("Namaian
Cell Name	SU CMOS GATE ARF	AAY UNII	CELL S	PECIFICA	ATION		CG211	K" Version Number of BC
T24	Power 2–AND 4	-wide N	/lultiplex	er				6
Cel	l Symbol			Pro	pagation D	elay Paran	neter	
			Jp VOL			dn L KOLO	0000	Path
		0.858 0.951	0.032 0.032	0.805 0.931	0.017 0.017	KCL2	CDR2	A to X B to X
		0.838	0.032	0.865	0.017			C to X
A1	٦	0.911	0.032	0.997	0.017			D to X
B1 —								
B2 ————————————————————————————————————	└┼ <b>├</b> ── ×					ł		
C1 C2	T							
D1 —		! 				<u> </u>		
D2		Paramete	er			-   -	Symbol	Typ (ns) *
	r							
Pin Name	Input Loading Factor (Iu)							
A B	1							
CD	1							
Pin Name	Output Driving Factor (lu)							
×	36	l						L
		* Minimu The val multipli		r the typical worst case	operating o	condition. condition are	given by the	ne maximum delay
	<u> </u>	L						
Equivalent Circuit								
A1 A2								
B1 —	, 							
B2 —		о х	•					
C1 C2								
01 —								
D2 —								
								÷
C21-T24-E0	Sheet 1/1							Page 9–1
								Page 9-1



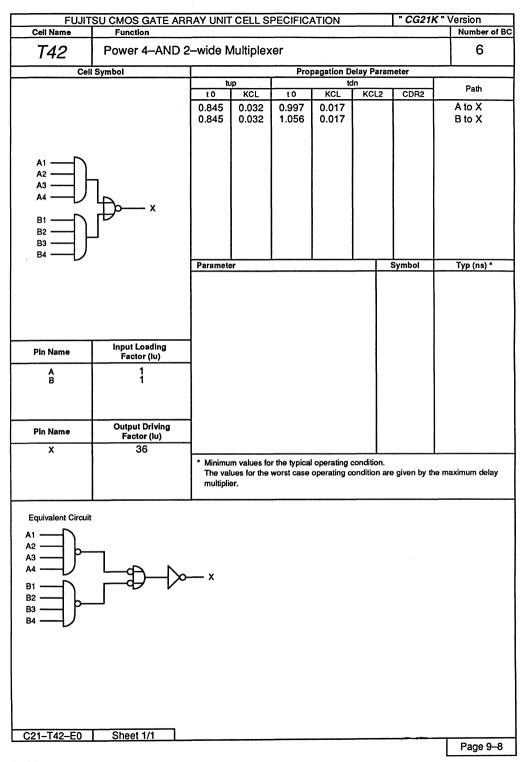




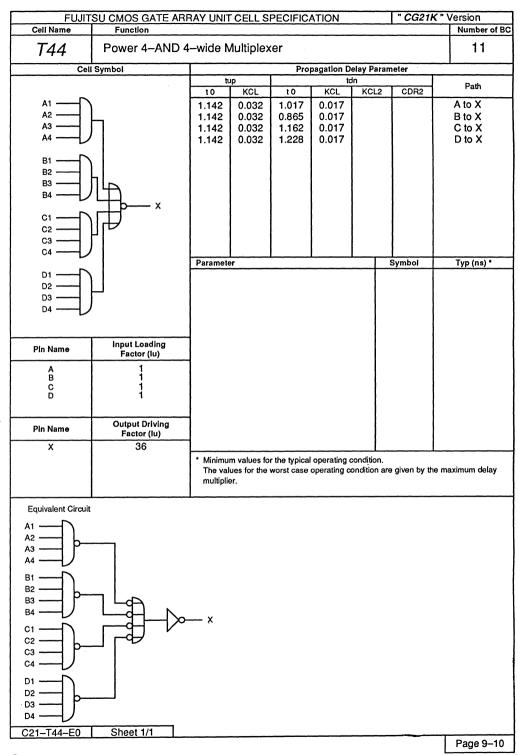
	OLLOWOO OATE ADD		. 0511. 0	DEOLEIO	ATION		" 0004	/ # \/a-raia-r
Cell Name	SU CMOS GATE ARF	AY UNII	CELLS	PECIFICA	ATION		- CG211	K " Version Number of BC
T32	Power 3-AND 2	-wide N	Aultiplex	er				5
Cell	l   Symbol	T		Pro	pagation D	elay Param	eter	
		tı	ηp			dn nt		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		0.805 0.805	0.032 0.032	0.891 0.951	0.017 0.017			A to X B to X
A1 A2 A3 B1 B2 B3	x							
		Paramete	er			:	Symbol	Typ (ns) *
	Input Loading							
Pin Name	Factor (lu)							
A B	1							
Pin Name	Output Driving Factor (lu)							
X	36	* Minimu The val multiplie		r the typical worst case	operating o	condition. ondition are	given by th	e maximum delay
Equivalent Circuit								
A1 A2 A3 B1 B2 B3		x						
C21-T32-E0	Sheet 1/1							Dog O. F
								Page 9–5

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
T33	Power 3-AND 3	-wide N	/lultiplex	er				7
	   Symbol	T	neter					
			ρ		to	in		Path
		t0	KCL	t 0	KCL 0.017	KCL2	CDR2	A to X
		0.924 0.924	0.032	0.878 0.944	0.017 0.017			B to X
		0.924	0.032	1.030	0.017			C to X
A1 ——						}		
A2	7	l	l		/			
A3 ——		İ	•			}		
В1 ——			1					
B2 — -			ł					
B3 — ✓	H					ł	1	
C1 —		I	l					
	J							
C3 —		Paramete	er				Symbol	Typ (ns) *
		1				-		
							į	
	Input Loading	1						
Pin Name	Factor (lu)	]					ļ	
A B	1					1		
C	1							
		ŧ					ŧ	
	0.44.0.5.5	ļ					l	
Pin Name	Output Driving Factor (lu)						ĺ	
X	36							
		* Minimu	m values fo	r the typical	operating o	condition.		
	'	The val		worst case	operating o	ondition are	given by the	maximum delay
				···				
ļ								
C21-T33-E0	Sheet 1/1							Page 0.6
								Page 9–6

ELUT	SU CMOS GATE ARF	TIMITY	CELLS	DECIEIC	ATION		" CG21F	C" Va	reion
Cell Name	Function	TAT UNII	OELL 3	FECIFICA	ATION		CGZII		Number of BC
T34	Power 3–AND 4	-wide N	<i>f</i> ultiplex	er					9
Cell	Symbol			Pro	pagation D		neter		
		t O	p KCL	t O	KCL	In KCL2	CDR2		Path
		1.102	0.032	0.911	0.017	KULZ	CDRZ	Α	to X
_		1.102	0.032	0.997	0.017				to X
A1		1.155	0.032	1.056	0.017				to X
A2 —		1.155	0.032	1.063	0.017			D	to X
B1	١								
B2 ————————————————————————————————————	η <b>ί</b> Α								
	ЧЪ— х								
C1 —							]		
C2 —									
~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	}								
D1 —		Paramete	er				Symbol	T	yp (ns) *
D2 —	<b>-</b>								
						1			
						Ì			
	Input Loading								
Pin Name	Factor (lu)	}							
A	1					1			
B C	1 1								
Ď	i								
Pin Name	Output Driving Factor (lu)								
×	36								
		* Minimu	m values fo	r the typical	operating of	ondition.			
		The val	ues for the	worst case	operating o	ondition are	given by th	e maxir	num delay
		multiplie	er.						
		-				1			
Equivalent Circuit									
A1 —									
A2									
B1 B2 D-	_   ~								
В3 —									
C1 —		— x							
C2 — þ—									
C3 ——/									į
D1									
D2 — )—									
D3 ————————————————————————————————————									
C21-T34-E0	Sheet 1/1								
J21 104 LU	011000 1/1								Page 9–7
								L	



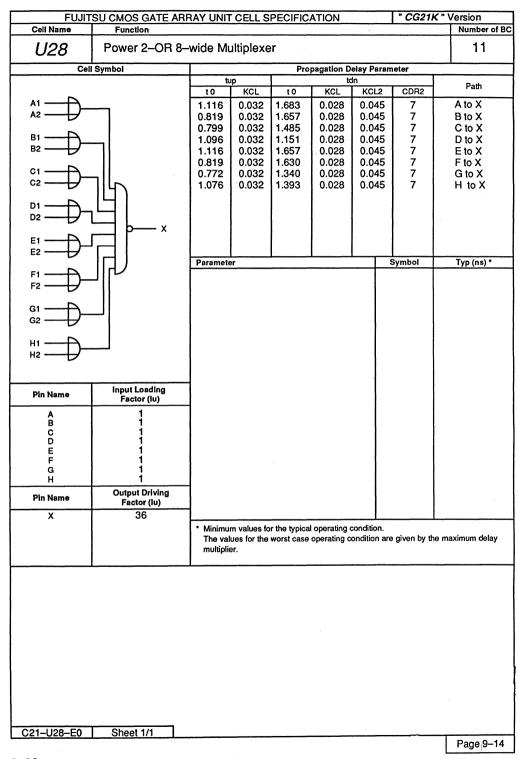
FULL	CH CHOC CATE ADD	) A) /	OFIL C	חבטובוס	ATION		" 00011	("Marajam
Cell Name	SU CMOS GATE ARF	TAY UNII	GELL SI	PECIFICA	ATION		CGZIK	" Version Number of BC
T43	Power 4–AND 3	–wide N	/lultiplex	er				10
Cell	Symbol	Propagation Delay Parameter						
			ıp			ln KOLO	0000	Path
		t 0 0.997	ксь 0.032	t 0 1.017	ксL 0.017	KCL2	CDR2	A to X
i		0.997	0.032	1.076	0.017			B to X
A1		0.997	0.032	1.162	0.017			C to X
A2 — _	_						[ [	
A3								
A4							1	
В1 ——		ļ .					1	
B2	—— ×						1	
B3							1	
B4 ————————————————————————————————————								
C1 ——								
C2		Paramete	er				Symbol	Typ (ns) *
C3								
							i	
							Ì	
							1	
Pin Name	Input Loading Factor (lu)					l	l	
A	1					ı	ł	
A B C	1 1	ļ						
	•					- [		
						į	i	
Pin Name	Output Driving							
×	Factor (lu) 36					l		
^	30	Minimu	m values for	r the typical	operating of	condition		
		The val	ues for the				given by the	e maximum delay
		multiplie	er.					
	<u> </u>	l						
Equivalent Circuit								
A1								
A2 b	-							
A3	l							
B1 ————————————————————————————————————	<u></u> — ₽							
B3 P	— <del>9</del> — />	— x						
B4 ——								
C1 —								
C2								
C3 — — — — — — — — — — — — — — — — — — —								
004 F40 F6	Chaot 4.14							
C21-T43-E0	Sheet 1/1							Page 9–9
								3-91



I CILIIT	SU CMOS GATE ARF	AV LINIT	CELL S	DECIEIC	ATION		" CG21K	' Vorsion
Cell Name	Function	WALL OINT	JLLL 3	LOIPIO	TION		1 COZIA	Number of BC
T54	Power 4-2-3-2	AND 4-	-wide M	ultiplexe	er			.10
Cell	Symbol	Propagation Delay Parameter					neter	
		t O	KCL	t O	KCL	ln KCL2	CDR2	Path
A1 ————————————————————————————————————		1.089 1.017 1.089 1.017	0.032 0.032 0.032 0.032	1.036 0.865 1.089 0.997	0.017 0.017 0.017 0.017	ROLZ	ODAZ	A to X B to X C to X D to X
C1 — C2 — C3 — D1 — D1	×	Paramete	er				Symbol	Typ (ns) *
D2 ——								
Pin Name	input Loading Factor (lu)						ļ	
A B C D	1 1 1							
Pin Name	Output Driving Factor (lu)						1	
×	36					- 1		
							given by the	maximum delay
Equivalent Circuit A1 A2 A3 A4 B1 B2 C1 C2 C3 D1 D2 C21—T54—E0	Sheet 1/1	— х						
								Page 9-11

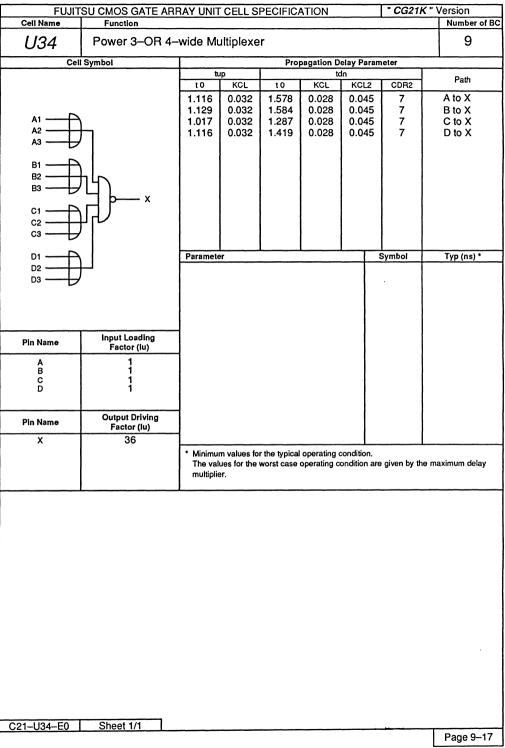
FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
U24	Power 2–OR 4–	wide Mu	ultiplexe	r				6
Cell	Symbol		I					
		t O	KCL	CDR2	Path			
		1.056	0.032	t 0 0.951	0.023	0.039	7	A to X
		0.759	0.032	0.924	0.023	0.039	7	B to X
1		1.003 0.733	0.032 0.032	0.944 0.898	0.023 0.023	0.039 0.039	7 7	C to X D to X
A1 —	<b>—</b>	0.700	0.002	0.000	0.020	0.005	'	DIOX
A2 ————	•							
B1 -	5 L							
B2 — 1	ЧЬ—×							
C1 —	건)							
C2 —		•						
D1 —	$\sqcup$	<u> </u>	<u> </u>		L	L.,		
D2 —	•	Paramete	er			<del></del>	Symbol	Typ (ns) *
							l	
	Input Loading							
Pin Name	Factor (lu)							
A B	1							
C	1					İ		
	•							
Pin Name	Output Driving	Ì						
X	Factor (lu)							
^	30	* Minimu	m values fo	r the typical	operating of	condition.		
		The val	ues for the				given by the	maximum delay
		multiplie	71.					
C21-U24-E0	Sheet 1/1							
								Page 9-12

	per of BC
Cell Symbol   Propagation Delay Parameter	9
Cell Symbol   Propagation Delay Parameter	
10   KCL   10   KCL   KCL2   CDR2   Path	
1.056   0.032   1.234   0.023   0.039   7   A to 2	h
Name   Input Loading Factor (lu)   Parameter   Symbol   Typ (n   D   D   D   D   D   D   D   D   D	Κ
B1	
Di	X
Parameter   Symbol   Typ (n   F1   F2   F2   F3   F3   F3   F3   F3   F3	
D1	`
Parameter   Symbol   Typ (n   F1   F2   F2   F3   F3   F3   F3   F3   F3	
Parameter   Symbol   Typ (n   F1   F2   F2   F3   F3   F3   F3   F3   F3	
Parameter   Symbol   Typ (n   F1   F2   F2   F3   F3   F3   F3   F3   F3	
Parameter   Symbol   Typ (n   F1   F2   F2   F3   F3   F3   F4   F4   F4   F4   F4	
F2	ns) *
F2	
Factor (Iu)  A 1 B 1 C 1 D 1 E 1	
Factor (Iu)  A 1 B 1 C 1 D 1 E 1	
Factor (Iu)  A 1 B 1 C 1 D 1 E 1	
B 1 1   D 1	
C 1 1	
E   1	
Dia Name Output Driving	
Factor (lu)	
Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum of the values for the worst case operating condition.	delav
multiplier.	uciay
C21-U26-E0 Sheet 1/1	
Page	9–13



EILUT	SU CMOS GATE ARF	TIMIT VA	CELLS	PECIFICA	ATION		" CG214	C" Version
Cell Name	Function	IAT UNIT	JLLL 3	LOIFIO	TION		00211	Number of BC
U32	Power 3-OR 2-	wide Mu	ultiplexe	r				5
Cell	Symbol	Propagation Delay Parame						
			ıр KCL	t O	KCL to	n KCL2	CDR2	Path
		1.135 1.116	0.032 0.032	0.878 0.865	0.023 0.023	0.039 0.039	7 7	A to X B to X
A1 A2 A3 B1 B2 B3	×	Paramete	er				Symbol	Typ (ns) *
	!	, uramete					-,	.35 (119)
Pin Name	Input Loading Factor (lu)							
A B	1							
Pin Name	Output Driving Factor (lu)							
X	36	* Minimu The val multiplie		r the typical worst case	operating o	condition. ondition ar	e given by th	e maximum delay
004 1100 50	Sheet 1/1							
C21-U32-E0	SHEEL I/I							Page 9-15

	FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Symbol   Propagation Delay Parameter   To   KCL   to   KCL   CDR2   Path   T.208   0.032   1.208   0.023   0.050   7   B to X   T.221   0.032   1.333   0.023   0.050   7   B to X   T.221   0.032   1.333   0.023   0.045   7   C to X   Typ (ns) *	Cell Name								Number of BC
Name   Input Loading Factor (lu)   Parameter   Symbol   Typ (ns)*	<i>U33</i>	Power 3–OR 3–	wide Mu	ultiplexe					7
1.208   0.032   1.208   0.023   0.050   7   A to X	Cell	Symbol			Pro	neter			
1.208   0.032   1.208   0.023   0.050   7   A to X					••			CDB2	Path
A2 A3 B1 B2 B3 C1 C2 C3 Parameter Symbol Typ (ns)*  Pin Name Input Loading Factor (lu) A 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	A1 ——		1.208 1.188	0.032 0.032	1.208 1.261	0.023 0.023	0.050 0.050	7 7	B to X
Pin Name Input Loading Factor (lu)  A 1 1 C 1  Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay	A2 A3 B1 B2	x							
Pin Name Input Loading Factor (lu)  A 1 1	C1 —								
Pin Name Input Loading Factor (lu)  A 1 B 1 C 1  Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay			Paramete	er			<u>'                                    </u>	Symbol	Typ (ns) *
Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay									
Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay	Pin Name	Input Loading Factor (lu)							
Factor (lu)  X  36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay	A B C	1							
Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay.	Pin Name	Output Driving Factor (lu)							
	x	36	The val	ues for the				given by the	maximum delay
C21-U33-E0 Sheet 1/1	C21-U33-E0	Sheet 1/1							Page 9–16



CUNT	CHICKOS CATE ADD	DAV LINIT	CELLS	DECIFIC	ATION		" CG21	K" Version
Cell Name	SU CMOS GATE ARE	TAT UNII	CELL S	FECIFIC/	ATION		CGZT	Number of BC
U42	Power 4–OR 2–	wide Mu	ultiplexe	r				6
Cel	Symbol	ľ		Pro	pagation D	elay Paran	neter	
			ıp			in Kala	T 0000	Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	A to V
		1.373 1.340	0.032 0.032	0.904 0.865	0.023 0.023	0.039	7 7	A to X B to X
		1.540	0.032	0.005	0.023	0.003	′	Blox
~								
A1 A2					1		1	
A3 —		<b>.</b>				1		
A4	Г.							
	] )>×	1		·		1	ì	
B1 -		l					Į.	
B2 B3		l			l	ł		
B4 —						1	1	
		Paramete	er				Symbol	Typ (ns) *
							_	
						-		
		}						
		ļ						
						1		
Pin Name	Input Loading	1				1		
	Factor (lu)	İ				ļ		
A B	1	Ì						
_	•							
Pin Name	Output Driving Factor (lu)							
X	36					Ì		
		* Minimu	m values fo	r the typical	operating	condition.		
		The val	ues for the				e given by th	ne maximum delay
i		multiplie	er.					
		L						
C21-U42-E0	Sheet 1/1							Doc 0 40
								Page 9-18

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version									
Cell Name Function							1 0027	Number	of BC
U43	Power 4-OR 3-wide Multiplexer							9	
Cell Symbol		Propagation Delay Parameter							
		t O	IP KCL	t O	KCL	fn KCL2	CDR2	Path	
		1.360	0.032	1.129	0.028	0.039	7	A to X	
		1.386	0.032	1.195	0.028	0.039	7	B to X	
A1 —		1.426	0.032	1.261	0.028	0.039	7	C to X	
A2						•	ļ		
A3					1		į	ļ	
A4 - D									
B1 —	7								
B2									
B3 B4	$\mathcal{U}$								
C1 ————————————————————————————————————									
C2 ————————————————————————————————————		Paramete	er				Symbol	Typ (ns) 1	
C4 —						l			
Pin Name	Input Loading	1							
	Factor (lu)	4							
A B	1								
Ç	i								
	Output Driving	1							
Pin Name	Factor (lu)								
X	36	<u></u>							
Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum.							ne maximum dels	av.	
multiplier.							y given by a	io maximam dele	-17
		1							
		•							
C21 1142 E0	Sheet 1/1								
C21-U43-E0	SHEEL I/I							Page 9-	-19

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL SI	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
U44	Power 4-OR 4-	wide Mu	ıltiplexe	r				11
Cell	Symbol			Prop	pagation D	elay Param	eter	
		t 0	p KCL	t O	KCL to	ln KCL2	CDR2	Path
A1 —		1.446	0.032	1.584	0.023	0.050	7	A to X
A2 A3		1.439	0.032	1.525	0.023	0.050	7	B to X
A4		1.393 1.413	0.032 0.032	1.287 1.419	0.023 0.023	0.050 0.050	7 7	C to X D to X
В1 —								
B2								
B3	J 7/							
B4 ————————————————————————————————————	Ы—×							
C1 -								
C2 ————————————————————————————————————	7							
C4 —		D			L	L.,	Symbol	Typ (ns) *
D1 —		Paramete	71			<del>-   '</del>	Syllibol	Typ (IIS)
D2							l	
D3 D4								
							l	
· · ·	Input Loading							
Pin Name	Factor (lu)					-		
A B	1							
CD	1							
Pin Name	Output Driving Factor (lu)							
×	36	1						
	9	* Minimu	m values fo	r the typical	operating	condition.		
		The val		worst case	operating c	ondition are	given by the	e maximum delay
		<u> </u>						
C21-U44-E0	Sheet 1/1							Dec: 0.00
								Page 9–20

# **Clock Buffer Family**

Page	Unit Cell Name	Function	Basic Cells
3–105	K1B	True Clock Buffer	2
3-106	K2B	Power Clock Buffer	3
3-107	КЗВ	Gated Clock (AND) Buffer	2
3-108	K4B	Gated Clock (OR) Buffer	2
3-109	K5B	Gated Clock (NAND) Buffer	3
3-110	KAB	Block Clock (OR) Buffer	3
3–111	KBB	Block Clock (OR x 10) Buffer	30
3–113	KDB	Block Clock (OR x 10) Buffer	32
3–115	KEB	Block Clock Buffer	23
3–117	VIL	Inverting Clock Buffer	2

FILIT	SU CMOS GATE AR	RAV LINIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function Function	HAT ONL	OLLLO	LOII 107	TION		00277	Number of BC
K1B	True Clock Buff	er						2
Cel	Symbol			Pro	pagation D		neter	
		t O	IP KCL	t O	KCL td	n KCL2	CDR2	Path
		0.383	0.032	0.456	0.017			A to X
Α ——	У х	Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
Α	1	-				ļ		
Pin Name X	Output Driving Factor (Iu) 36	* Minimu	m values fo	the typical	operating c	ondition.		
		The value multiplie	ues for the	worst case	operating or	ondition are	given by the	maximum delay
Equivalent Circuit								
C21-K1B-E0	Sheet 1/1							

FUJIT	SU CMOS GATE ARE	RAY UNIT CELL SPECIFICATION " CG21K							'ersion
Cell Name	Function								Number of BC
K2B	Power Clock Bu	ffer							3
Cel	Symbol			Pro	pagation D	elay Paran	eter		
			ıb			in			Path
		t O	KCL	t O	KCL	KCL2	CDR2		
1	!	0.561	0.014	0.634	0.017				X of A
		1							
							İ		
		l							
A	>×	1							
	<b>√</b>	İ							
					<u> </u>				
	•	Paramete	er				Symbol		Typ (ns) *
						ļ			
						l			
•		}							
Pin Name	Input Loading								
	Factor (lu)	Ì							
Α	1								
		Ì							
						1		i	
Pin Name	Output Driving	}						l	
×	Factor (lu) 55	l						l	
^	33	* Minimu	m values fo	r the typica	operating of	ondition.		l	
		The val	ues for the	worst case	operating c	ondition are	given by th	e ma	ximum delay
		multiplie					,		•
	l	<u> </u>							
Familia 1 - 2 Ot 1									
Equivalent Circuit									
A1	— <b>d</b> >—−×								
į									
004 1/05 50	Object 414								
C21-K2B-E0	Sheet 1/1							т	Page 10-2

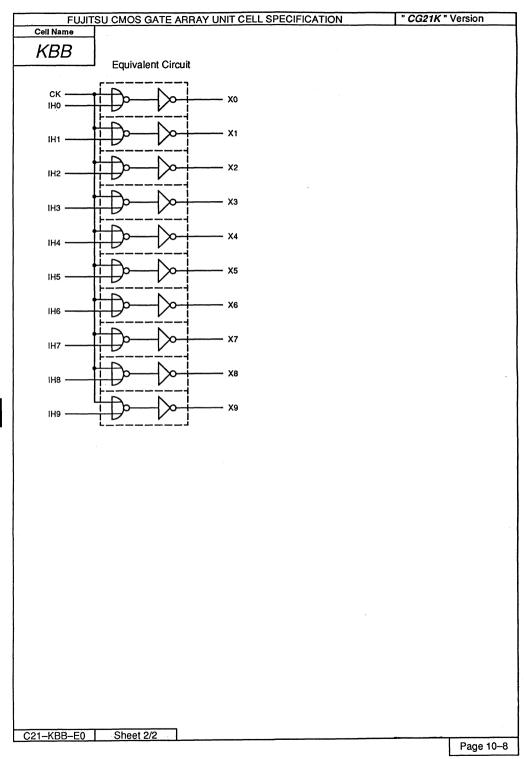
CILIIT	SH CMOS CATE ADI	DAY LIAUT	CELLO	DECIEIC	ATION		" CG211	C" Version
Cell Name	SU CMOS GATE ARE	TAT UNI	CELLS	PECIFICA	ATION		CGZII	Number of BC
КЗВ	Gated Clock (Al	ND) Buff	fer					2
Cell	Symbol			Pro	pagation D		neter	
		t O	JP KCL	t O	KCL to	ln KCL2	CDBA	Path
		0.528	0.032	0.528	0.017	KULZ	CDR2	A to X
A1 ————————————————————————————————————	D×							
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
Α	1							
Pin Name	Output Driving							
х	Factor (lu)	1						
^	00	Minimu     The val     multiplie	ues for the	r the typical worst case	operating o	condition.	e given by th	e maximum delay
Equivalent Circuit								
A1	x							
C21-K3B-E0	Sheet 1/1							Dogo 40.0
								Page 10-3

FUJIT	SU CMOS GATE ARF	CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version										
Cell Name	Function							Number of BC				
K4B	Gated Clock (Of	R) Buffe	r					2				
	l I Symbol	<u> </u>		Pro	pagation D	elay Param	neter					
			ıδ			in		Path				
		t0	KCL	t 0	KCL	KCL2	CDR2	A to X				
A1 A2	<b>┣</b> —×	0.416	0.032	0.601	0.023	0.034	8	7.07				
					ĺ							
		Paramete	l ∋r		L	<del>'                                    </del>	Symbol	Typ (ns) *				
	Pin Name Input Loading											
Pin Name	Input Loading Factor (lu)											
A	1											
Pin Name	Output Driving Factor (lu)											
X	36	* Minimu The val multiplie		r the typical worst case	operating o	condition. ondition are	given by the	maximum delay				
Equivalent Circuit A1 A2	x											
C21-K4B-E0	Sheet 1/1							7				
								Page 10-4				

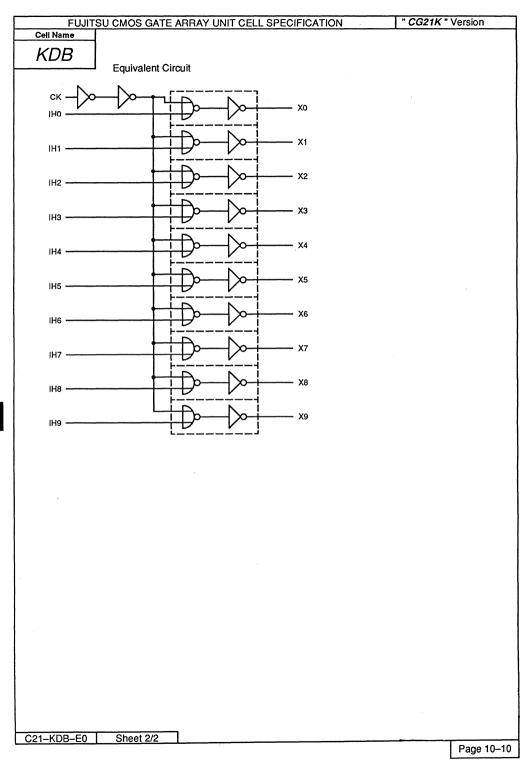
FULIIT	SU CMOS GATE ARF	TIMIT YAS	CELLS	PECIFIC	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
K5B	Gated Clock (NA	AND) Bu	uffer					3
Cell	Symbol			Pro	pagation D		eter	
		t O	KCL	t O	KCL	ln KÇL2	CDR2	Path
A1	)•—×	0.601	0.032	0.786	0.017	KOLZ	CDR2	A to X
							<u> </u>	
		Paramete	er				Symbol	Typ (ns) *
	Lava Ladia							
Pin Name	Input Loading Factor (lu)							
A	1							
Pin Name	Output Driving Factor (lu)							
х	36	* Minimu The val multiplie	ues for the	r the typical worst case	operating o	condition. condition are	given by the	e maximum delay
Equivalent Circuit								
A1	<b>-</b> ♦ <b>-</b> ->-	x						
C21-K5B-E0	Sheet 1/1							Page 10-5

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG21F	(" Version
Cell Name	Function							Number of BC
KAB	Block Clock (OF	l) Buffer						3
Cel	Symbol			Pro	pagation D	elay Paran	neter	
		tu				in		Path
A1 A2	<b>D</b> ×	t 0 0.574	KCL 0.014	0.977	0.017	KCL2	CDR2	A to X
Pin Name	Input Loading Factor (lu)							
А	1							
Pin Name	Output Driving Factor (lu)							
X	55	* Minimui The val multiplie	ues for the	r the typica worst case	l operating o	condition. condition are	e given by th	e maximum delay
Equivalent Circuit A1 A2	×							
C21-KAB-E0	Sheet 1/1							Page 10-6
								Faye 10-0

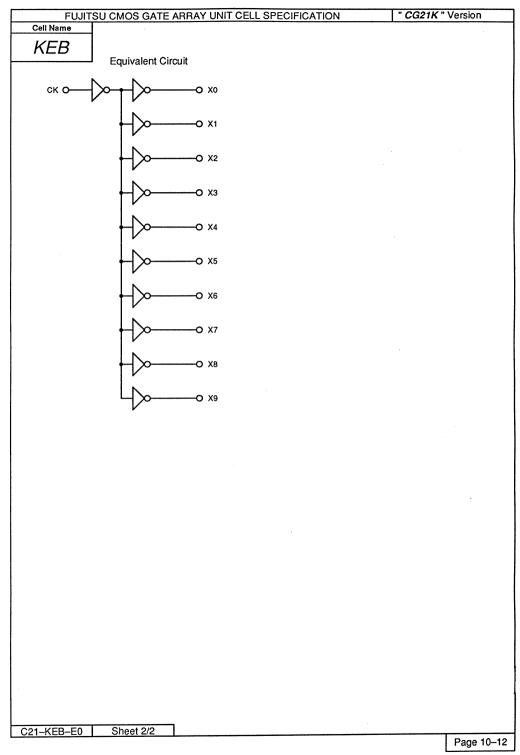
ELLIT	SU CMOS CATE ADD	AV LINIT	CELL S	DECISIO	ATION		" CG21K	" Version
Cell Name	SU CMOS GATE ARF	MT UNII	OELL SI	CUITIU	ATION		CGZIK	Number of BC
KBB	Block Clock Buff	er (OR	x 10)					30
Cell	Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
		0.706 0.574	0.014 0.014	1.102 0.977	0.017 0.017	KOLZ	CDR2	CK to X IH to X
CK ————————————————————————————————————	— X0 — X1 — X2 — X3 — X4 — X5 — X6 — X7							
IH8	X8 X9	Paramete	er				Symbol	Typ (ns) *
Pin Name CK IH	Input Loading Factor (lu) 10 1							
Pin Name	Output Driving Factor (lu)							
х	55	* Minimui The val multiplie	ues for the	r the typical worst case	operating o	condition.	given by the	maximum delay
								İ
C21-KBB-E0	Sheet 1/2							
								Page 10-7



FUJIT	SU CMOS GATE ARE	RAY UNIT	CFLLS	PECIFICA	ATION		" CG21K	(" Version
Cell Name	Function						1	Number of BC
KDB	Block Clock Buff	fer (OR	x 10)					32
Cell	Symbol			Proj	pagation D		neter	
		t O	KCL	t O	KCL	n KCL2	CDR2	Path
		1.254 0.594	0.019 0.019	1.848 1.221	0.011 0.011			CK to X IH to X
CK ————————————————————————————————————	X0 X1 X2 X3 X4 X5 X6 X7 X8 X9	Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
CK IH	1							
Pin Name	Output Driving							
X X	Factor (lu) 55					İ		
^	33	* Minimui The vali multiplie	ues for the	r the typical worst case	operating o	condition. ondition are	e given by th	e maximum delay
C21-KDB-E0	Sheet 1/2							
								Page 10-9



FUJIT	SU CMOS GATE ARE	RAY LINIT	CELLS	PECIFIC	ATION		" CG21	K " Version
Cell Name	Function	1711 01111	OLLLO	1 2011 107	111011			Number of BC
KEB	Block Clock Buff	fer						23
Cel	l Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	dn KCL2	CDDA	Path
		0.825	0.019	0.911	0.011	0.023	18	CK to X
ск ——	X0							
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
ск	6							
Pin Name	Output Driving Factor (lu)							
X	55	* Minimu The val multiplie	ues for the	r the typical worst case	operating o	condition.	given by th	ne maximum delay
C21-KEB-E0	Sheet 1/2							
								Page 10-11



FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG21I	C" Version
Cell Name	Function							Number of BO
V1L	Inverting Clock	Buffer						2
Cel	Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	In KCL2	CDR2	Path
		0.167	0.014	0.392	0.017			A to X
Α	<b>&gt;</b> ×	Paramete	er				Symbol	Typ (ns) *
Din Name	Input Loading							
Pin Name	Factor (lu)	_						
	4 Output Driving							
Pin Name	Factor (iu)							
x	55	* Minimu The val multiplie		r the typical worst case	operating o	condition. ondition are	given by th	e maximum delay
						٠		
C21-V1L-E0	Sheet 1/1							

# Scan Flip-flop (Positive Edge Type) Family

Page	Unit Cell Name	Function	Basi Cells
3–121	SDH	Scan 2-input D Flip-flop with Clear and Clock Inhibit	14
3-124	SDJ	Scan 4-input D Flip-flop with Clear and Clock Inhibit	15
3–127	SDK	Scan 6-input D Flip-flop with Clear and Clock Inhibit	16
3-130	SJH	Scan J-K Flip-flop with Clear and Clock Inhibit	16
3–133	SDD	Scan 2-input D Flip-flop with Clear, Preset, and Clock Inhibit	16
3–137	SDA	Scan 1-input D Flip-flop with Clock Inhibit	12
3–140	SDB	Scan 1-input 4-bit D Flip-flop with Clock Inhibit	42
3–144	SHA	Scan 1-input 8-bit D Flip-flop with Clock Inhibit	68
3–147	SHB	Scan 1-input 8-bit D Flip-flop with Clock Inhibit and Q Output	62
3–150	SHC	Scan 1-input 8-bit D Flip-flop with Clock Inhibit and XQ Output	62
3–153	SHJ	Scan 8-bit D Flip-flop with Clock Inhibit and 3-to-1 Data Multiplexer	78
3–156	SHK	Scan 8-bit D Flip-flop with Clock Inhibit and 3-to-1 Data Multiplexer	88
3-159	SFDM	Scan 1-input D Flip-flop with Clock Inhibit	10
3-162	SFDO	Scan 1-input D Flip-flop with Clear and Clock Inhibit	11
3–165	SFDP	Scan 1-input D Flip-flop with Clear, Preset, and Clock Inhibit	12
3–169	SFDR	Scan 4-input D Flip-flop with Clear and Clock Inhibit	36
3–173	SFDS	Scan 4-input D Flip-flop with Clock Inhibit	31
3–177	SFJD	Scan J-K Flip-flop with Clock Inhibit	14

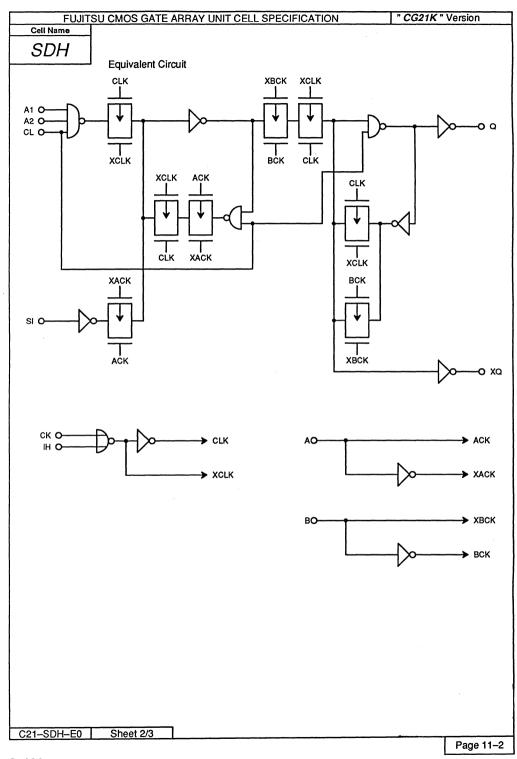
FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFIC.	ATION		" CG211	K " Version
Cell Name	Function							Number of BC
SDH	SCAN 2-input	DFF with	Clear &	& Clock-	-Inhibit			14
Cel	l Symbol	1		Pro	pagation D	elay Paran	neter	
		tı	ıρ			dn		Path
		10	KCL	t O	KCL	KCL2	CDR2	
		1.967	0.032	1.575	0.017	0.039	7	CK, IH to Q
		1.241	0.032	1.135	0.028	0.056	7	CK, IH to XQ
		2.000	0.032	0.568	0.017	0.039	7	CL to Q, XQ
				1	1	1	1	
		1	1			ĺ		
A1 —	<b>├</b> ─ °		İ	İ	1			
A2			!			l		
ск —		1			l	ł		
и	i i		1		i	1		
sı ——	Ì			1	ł	l		
Α	b— хо		ļ		ļ			
в — ф	7 ~~		l	}	1	İ		
_	<del>ბ</del>	<u></u>	L	<u> </u>	L	L	<u></u>	
		Paramete					Symbol	Typ (ns) *
	CL		ulse Wid				tcw	3.2 2.5
	01	Clock P	ause Tim	ie			t cwn	2.5
		Data Se	etup Time	· · · · · · · · · · · · · · · · · · ·			tsD	2.2
			old Time				t HD	0.6
		- Data in						
	Input Loading	Clear P	ulse Widt	h			tLW	2.5
Pin Name	Factor (lu)	Clear R	elease Ti	me			t REM	1.8
A1, A2	1	Clear H	old Time				t inn	0.9
ĊК	1					I		
IH CL	1 3	1						
SI	1 1	1						
A, B	2							
	Output Driving	1						
Pin Name	Factor (lu)							
Q	36	1						L
ΧQ	36				operating o		aivon hy th	e maximum delay
	1	multiplic		worst case	operating o	ondition are	given by th	io maximum delay

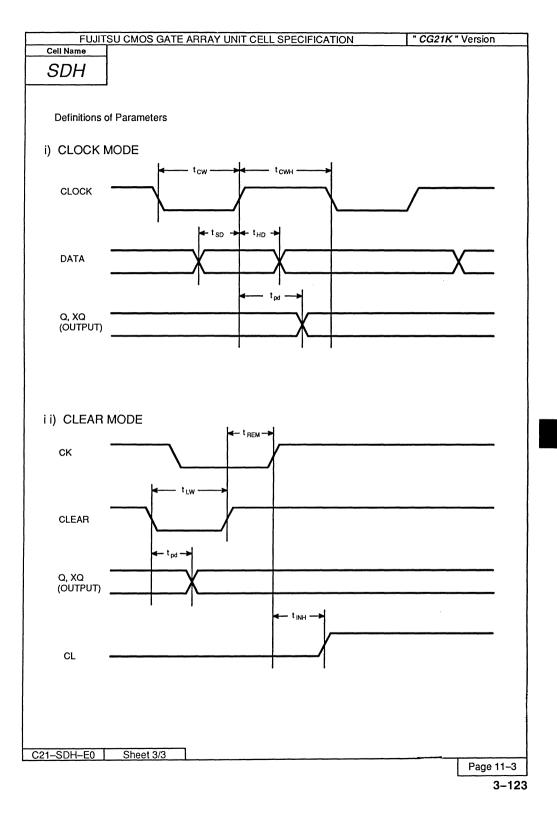
MODE			IN	PUT			ОИТ	PUT
MODE	CLK	CL	D	Α	В	SI	Q	XQ
CLEAR	Х	L	х	х	Х	Х	L	Н
CLOCK	L to X	Н	Di	L	L	Х	Di	Di
CLOCK	Н	Н	х	L	L	Х	Q <sub>0</sub>	XQο
0041	Н	н	х	L to H to L	Η.	Si	Q <sub>0</sub>	XQ <sub>0</sub>
SCAN	Н	Н	х	LHt	o L to	нх	Si	Si

multiplier.

Note : CLK = CK + IH  $D = A1 \times A2$ 

C21-SDH-E0	Sheet 1/3





	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	K"\	Version
Cell Name	Function								Number of BC
SDJ	SCAN 4-input [	OFF with		15					
Cel	l Symbol			neter		<u> </u>			
		tup tdn						Path	
		t O	KCL	t O	KCL	KCL2	CDR2		
		1.452 1.248 1.974	0.032 0.032 0.032	1.597 1.129 0.561	0.017 0.028 0.017	0.039 0.056 0.039	7 7 7	c	CK, IH to Q CK, IH to XQ CL to Q, XQ
A1 ————————————————————————————————————	a ха								
_	<del></del>	Paramete	er				Symbol		Typ (ns) *
		Clock P		t cw		3.2			
	CL	Clock P	ause Tim	ie			t cwn		2.5
	OL	<u> </u>						_	2.7
			tup Time			<del></del>	t <sub>SD</sub>		0.5
		Data Ho		t HD	-	0.5			
	Input Loading	Clear P	ulse Widt	h			tıw	-	2.5
Pin Name	Factor (lu)		elease Ti				t REM		1.8
A1, A2	1		old Time				t inh		0.9
61, 82 CK IH CL SI A, B	1 1 1 3 1 2								
Pin Name	Output Driving Factor (lu)	]							
Q XQ	36 36						e given by th	e ma	aximum delay

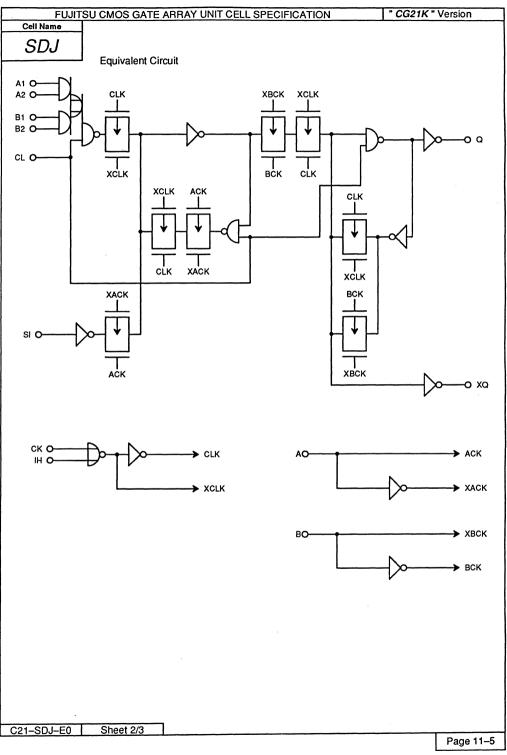
MODE				OUTPUT				
MODE	CLK	CL	D	Α	В	SI	Q	XQ
CLEAR	Х	L	х	х	Х	Х	L	Н
CLOCK	L to H	Н	Di	L	L	Х	Di	Di
CLOCK	Н	Н	Х	L	L	X	Q <sub>0</sub>	XQο
SCAN	Н	Н	х	L to H to L	Н	Si	Q <sub>0</sub>	XQο
SCAN	Н	Н	Х	L Ht	o L to	нх	Si	Si

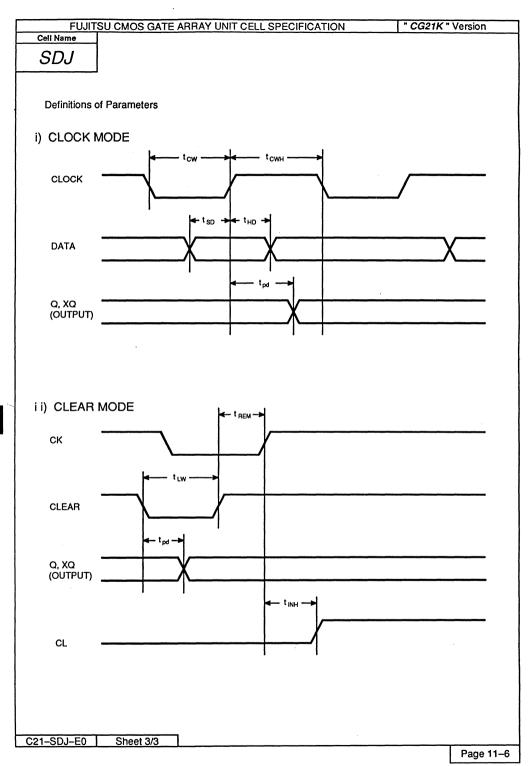
Note : CLK = CK + IH

 $D = (A1 \times A2) + (B1 \times B2)$ 

C21-SDJ-E0	Sheet 1/3
021-3DJ-LU	SHEEL 1/3

Page 11-4





	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21	K"\	
Cell Name	Function								Number of BC
SDK	SCAN 6-input [	OFF with	Clear &	& Clock-			16		
Cel	l Symbol	1		Pro	pagation D	elay Parar	neter		
		tı	η		to	dn			Path
		t 0	KCL	t 0	KCL	KCL2	CDR2		raui
A1 ————————————————————————————————————	— a	1.954 1.228 1.974	0.032 0.032 0.032	1.584 1.142 0.541	0.017 0.028 0.017	0.039 0.056 0.039	7 7 7	C	EK, IH to Q EK, IH to XQ EL to Q, XQ
В — q		Paramete	er		<u> </u>		Symbol	<del>                                     </del>	Typ (ns) *
i L		Clock P	ulse Wid	th			t <sub>CW</sub>		3.2
	7	Clock P	ause Tim	ne			t cwH		2.5
ł	CL		etup Time				t <sub>SD</sub>	<u> </u>	2.9
		Data Ho	old Time				t HD	<u> </u>	0.3
			1 1100					<u> </u>	- 0.5
Pin Name	Input Loading		ulse Widt				tLW	<u> </u>	2.5
	Factor (lu)		elease Ti	me			t REM	├	1.8 0.9
A1, A2 B1, B2 C1, C2		Clear H	old Time				t inn		0.9

CL SI A, B

Pin Name

Q XQ

MODE			11	IPUT			OUT	PUT
MODE	CLK	CL	D	Α	В	SI	Q	XQ
CLEAR	Х	L	Х	×	х	Х	L	н
CLOCK	L to H	Н	Di	L	L	Х	Di	Di
CLOCK	Н	Н	х	L	L	Х	Qo	XQ₀
00411	Н	Н	Х	L to H to L	Н	Si	Qo	XQο
SCAN	Н	Н	Х	LHt	o L to	нх	Si	Si

multiplier.

11312

Output Driving Factor (lu)

36 36

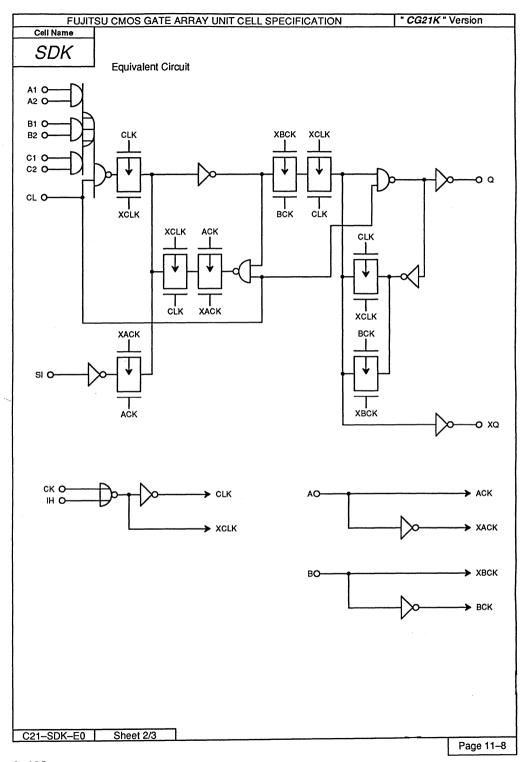
Note : CLK = CK + IH

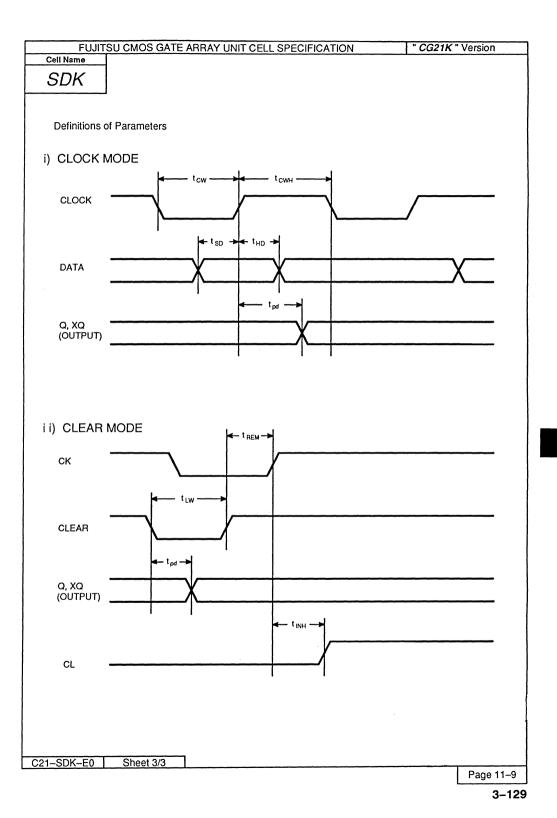
 $D = (A1 \times A2) + (B1 \times B2) + (C1 \times C2)$ 

Minimum values for the typical operating condition.
 The values for the worst case operating condition are given by the maximum delay

C21-SDK-E0 Sheet 1/3

Page 11-7





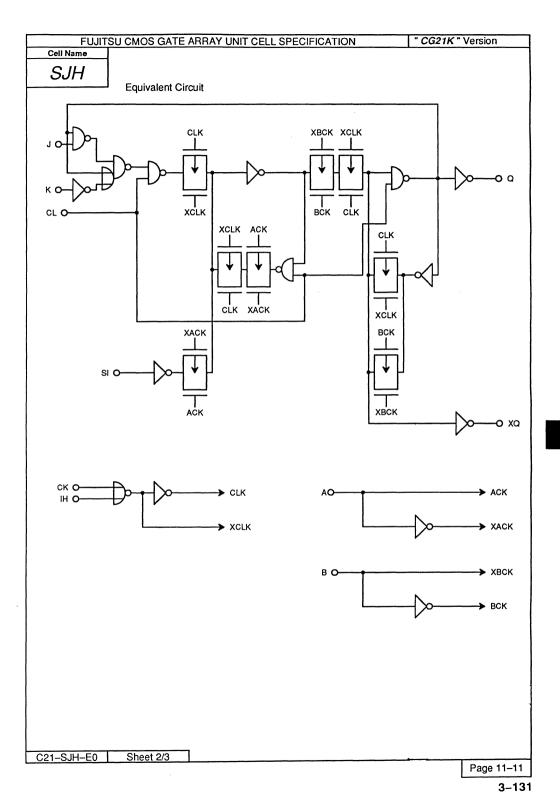
				E ARI	RAY UNI	TCE	LL S	PECIFICA	ATION			" CG21	K"	Version
Cell Name	е	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION Function												Number of E
SJH		SCA	N J–K	FF v	vith Clea	ar &	Clo	ck–Inhib	oit					16
	Cell	Symbol					aram	eter						
												dn		
					t O	-	CL	t O	KCL	KCI	_	CDR2		Path
					2.238		032	1.782	0.017	0.03		7		CK, IH to Q
					1.248		032	1.142	0.028	0.0		7		CK, IH to XQ
					1.987	1 0.0	032	0.733	0.017	0.03	39	7	(	CL to Q, XQ
						1.								
J					1	1								
к —	<b>-</b> d	-	— a		1	1								
	7	- 1				1								
ск — IH —		1												
si		1			1	1								
A	_				1					l				
В —	-d	p-	— xa		1	l								
		لح												
		Ī		Paramet						Symbol			Typ (ns) *	
		CL		Clock F							t cw		3.2	
				Clock F	ause	e Tim	<u>e</u>			t cwH			2.5	
				Data S	Timo	7 D		t sp		2.7				
						Data Setup Time (J) Data Setup Time (K)								2.9
					Data H				t <sub>SD</sub>	_	0.3			
Pin Name			t Loadin											
r iii itaiiic		Fa	ctor (lu)		Clear Pulse Width							t LW		2.5
J,K			1		Clear Release Time							t REM		1.8
CK IH			1		Clear Hold Time							t INH	_	0.9
CL			3		ł									
SI A, B			1 3 1 2		ļ									
Λ, Β			-		İ									
D' N		Outr	out Drivi	ng	1								ŀ	
Pin Name			ctor (lu)										L	
Q XQ			36 36					the typical				alisa a bis A		
XQ			36		nultipli		or the v	worst case	operating c	onditio	n are	given by th	e m	aximum delay
					1110100	٠								
Function Ta	able													
				INPUT				OU	TPUT	1				
MODE						D.				ł				
	CL		J	K	Α	В	SI	_ <u> </u>	XQ	1				
CLEAR	X	L	Х	Х	X	X	Х	L	н					
	L to	н н	L	L	L	L	X	L	Н	1				
	L to	н н	н	Н	L	L	Х	Н	L	1				
CLOCK	L to	н н	L	Н	L	L	X	Q <sub>0</sub>	XQ <sub>0</sub>					
	L to	н н	Н	L	L	L	х	XQ <sub>0</sub>		1				
	Н	Н	×	×	L	L	Х	Q <sub>0</sub>	XQ₀	1				
	Н		X		to H to L		Si	Q <sub>0</sub>	XQ <sub>0</sub>					
SCAN						·		<del></del>		1				

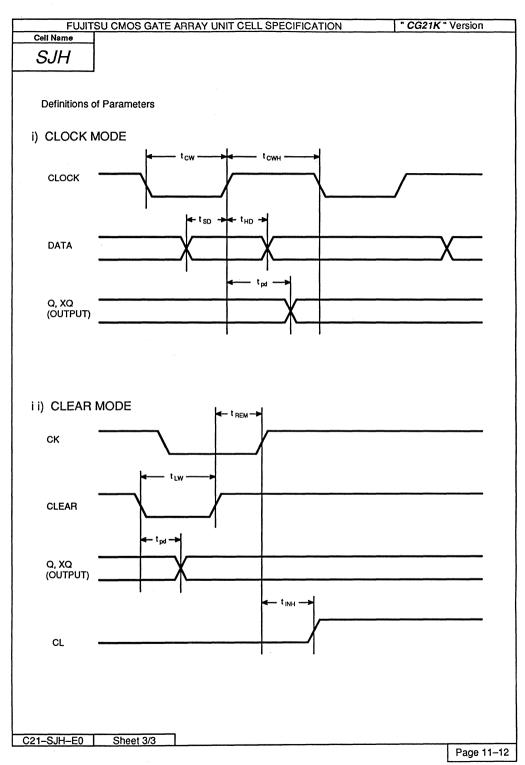
Note : CLK = CK + IH

L H to L to H X

C21-SJH-E0 Sheet 1/3

Page 11-10





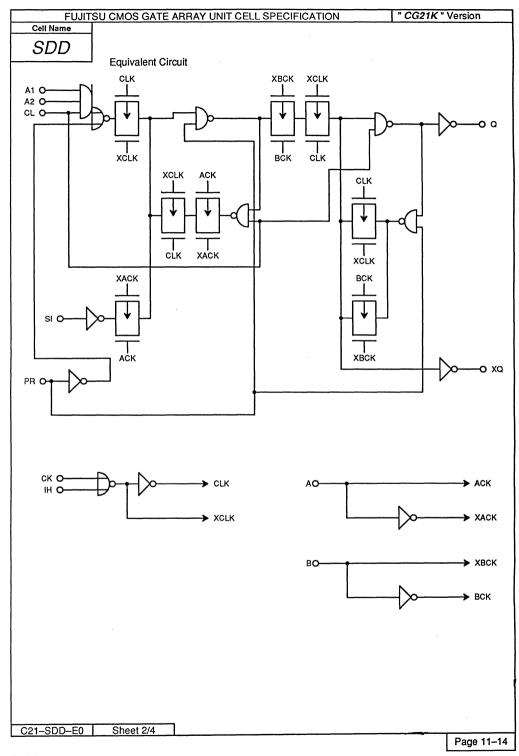
FULIIT	SU CMOS GATE AR	RAY LINIT	CELLS	PECIFIC	ATION		" CG	21K	" Version
Cell Name	Function	11/11 01111	OLLL O	1 2011 107	VIIIOI V				Number of BC
SDD	SCAN 2-input [	OFF with	Clear,	Preset 8	& Clock-	–Inhil	bit		16
Cel	l Symbol	Τ		Pro	rameter				
		tı	ıρ	tdn					Path
		t O	KCL	t O	KCL	KCL	2 CDF	12	
A1	1.954 1.399 2.376 2.026	0.032 0.032 0.032 0.032	1.703 1.129 0.541 1.241	0.017 0.028 0.017 0.028	0.03 0.05 0.03 0.05	56 7 39 7		CK, IH to Q CK, IH to XQ CL to Q, XQ PR to Q, XQ	
CK ————————————————————————————————————	SI — XO		er				Symbol		Typ (ns) *
	CL	Clock Pulse Width							3.2
	OL .	Clock Pause Time							2.5
			tup Time				t <sub>SD</sub>		3.2 0.6
		Data Ho		t HD	-	0.6			
	Input Loading	Clear P	ulse Widt	h			tLW		2.5
Pin Name	Factor (lu)		elease Ti			$\neg \neg$	t REM	$\neg$	1.8
A1. A2	1		old Time				t inh		0.9
ćк	1								
IH CL	1 3		Pulse Wid				t pw		4.0
PR	3 3 1		Release 1				t REM		2.2
SI		Preset I	Hold Time	·			t inh	_	0.6
A, B	2					- 1			
Pin Name	Output Driving Factor (lu)					l		$\bot$	
a xa	36 36		ues for the		operating o			by the	maximum delay

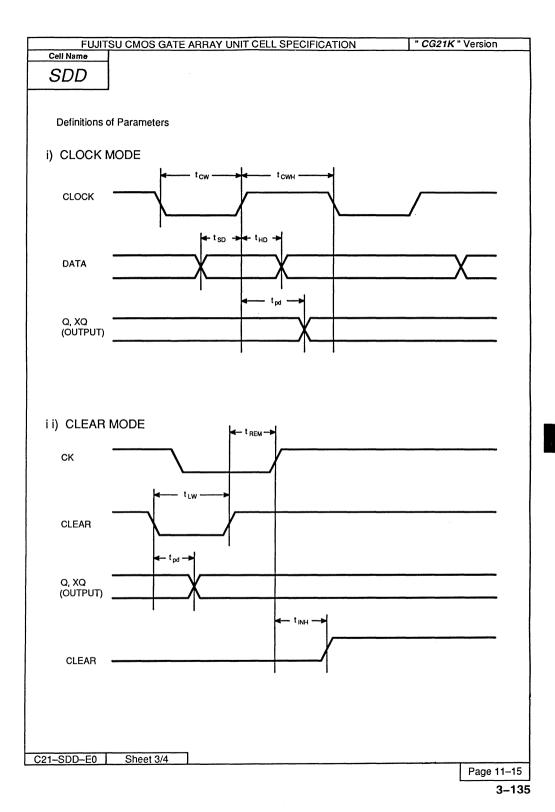
MODE				INPU	Т			OUT	PUT
MODE	CLK	CL	PR	D	Α	В	SI	Q	XQ
CLEAR	Х	L	Н	Х	Х	х	х	L	Н
PRESET	Х	Н	L	Х	х	х	х	Н	L
	L to H	Н	н	Di	L	L	х	Di	Di
CLOCK	н	Н	Н	Х	L	L	х	Q <sub>0</sub>	XQ₀
20411	Н	Н	Н	Х	L to H t	L H	Si	Q <sub>0</sub>	XQο
SCAN	н	Н	Н	Х	L	H to L to	нх	Si	Si
CL/PR	Х	L	L	Х	Х	Х	х	Proh	ibited

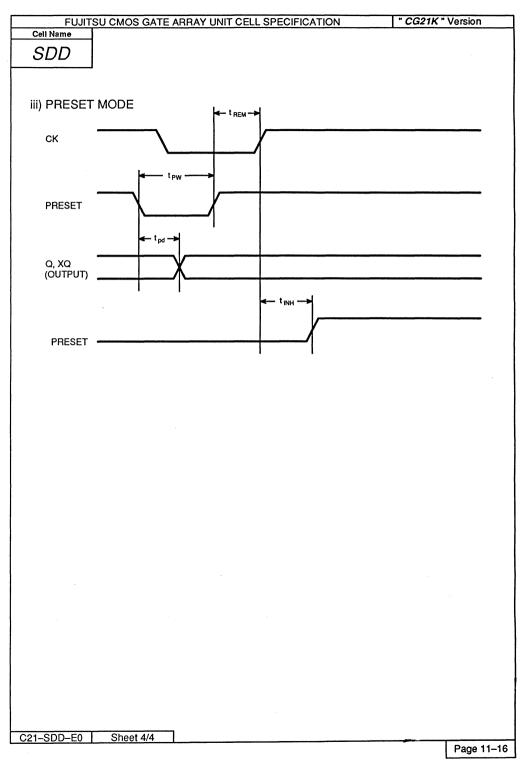
Note : CLK = CK + IH D = A1 x A2

C21-SDD-E0 Sheet 1/4

Page 11-13





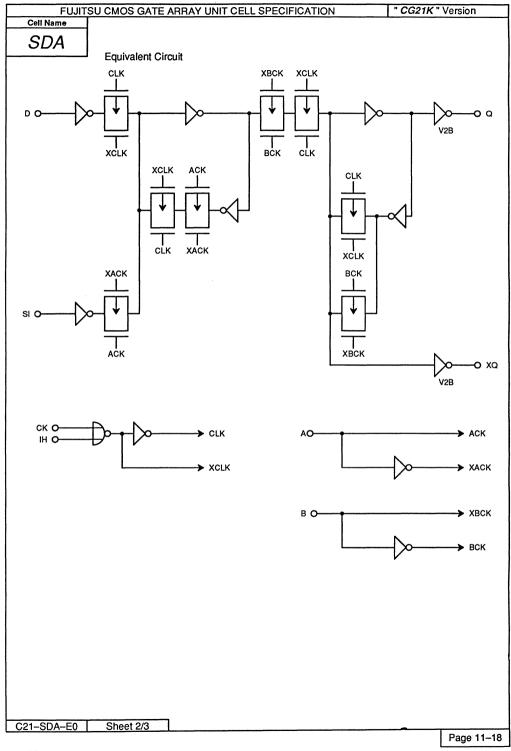


	JITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" V							
Cell Name	Function						Number of B	
SDA	SCAN 1-input DFF with Clock-Inhibit						12	
Cel	l Symbol							
	tı	tup tdn					Path	
		t O	KCL	t 0	KCL	KCL2	CDR2	
		1.683	0.032	1.584	0.017	0.039	7	CK, IH to Q
		1.234	0.032	1.149	0.028	0.056	7	CK, IH to XQ
D ————————————————————————————————————	— a э— ха	Clock P	er ulse Widt ause Tim etup Time	e			Symbol tow towh	Typ (ns) * 3.2 2.5 2.1 0.9
Pin Name	Input Loading Factor (lu)	1						
D CK IH SI A, B	1 1 1 1 1 2						-	
Pin Name	Output Driving Factor (lu)							
Q XQ	Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the maximum delay multiplier.							

MODE			OUTPUT				
	CLK	D	Α	В	SI	Q	XQ
CLOCK	L to H	Di	L	L	Х	Di	Di
	н	Х	L	L	Х	Q <sub>0</sub>	XQ <sub>0</sub>
SCAN	н	х	L to H to L	Н	Si	Q <sub>0</sub>	XQ <sub>0</sub>
	н	X	LHt	L to	НХ	Si	Si

Note : CLK = CK + IH

C21	-SDA	\-E0_	Sheet	1/3_



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

Cell Name

SDA

Definitions of Parameters

i) CLOCK MODE

CLOCK

DATA

Q, XQ
(OUTPUT)

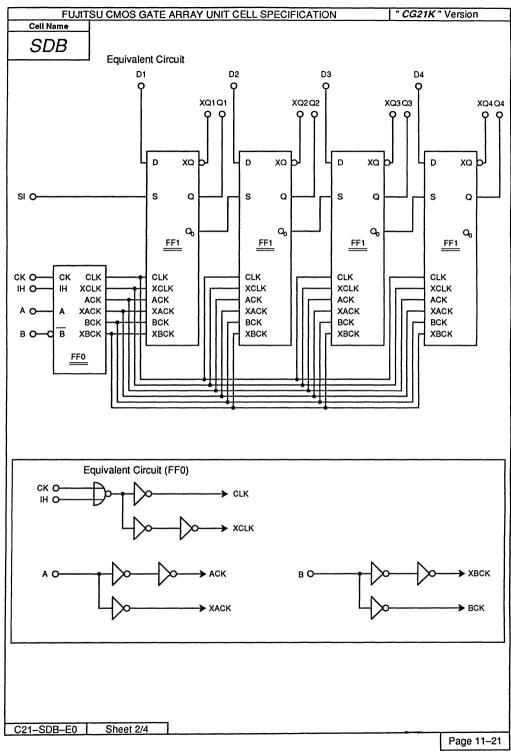
C21-SDA-E0 Sheet 3/3

. F	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version												
Cell Name			ction	- 71111	AT OINT	OLLEO	LOII 107	ATION			002.	•	Number of BC
SDB	?	SCA	N 1-inp	out 4-	- bit DF	F with (	Clock-Ir	nhibit					42
	Cell S	ymbol					Pro	pagation D		aram	eter		
				- }	t O	ıр KCL	t O	KCL	in KCL	2	CDR2		Path
				ŀ	2.238	0.032	2.079	0.017	0.03	_	7		K, IH to Q
					1.716	0.032	1.756	0.028	0.05		7		K, IH to XQ
D1 — D2 — D3 — D4 — CK — IH — SI — A — B —	D2 — XQ1 D3 — Q2 D4 — Q2 CK — Q3 CK — Q4 SI — Q4 A — XQ4					er ulse Wid ause Tin					Symbol t cw t cwn		Typ (ns) * 4.0 2.5
				t	Olocki	4436 1111					CWH		
						etup Time old Time				_	t <sub>SD</sub>		1.3 2.0
Pin Name D CK IH SI A, B		Fa	t Loading ctor (lu) 1 1 1 1 2 out Driving ctor (lu)										
Q		ra										l	
хã			36 36			ues for the		operating o			given by th	ne ma	aximum delay
Function Ta	able										***************************************	-	
MODE			INPU	т		тио	PUT						
MODE	CLK	Dn	Α	В 8	SI, Qn-1	Q	XQn						
сьоск	L to H	Di X	L L	L	X	Di Qn <sub>0</sub>	Di XQn <sub>0</sub>						
	Н		L to H to L		Si	Qn <sub>0</sub>	XQn <sub>0</sub>						
SCAN	Н			to L to I		Si	Si						
						Note : CLK	= CK + IH = 1 ~ 4						

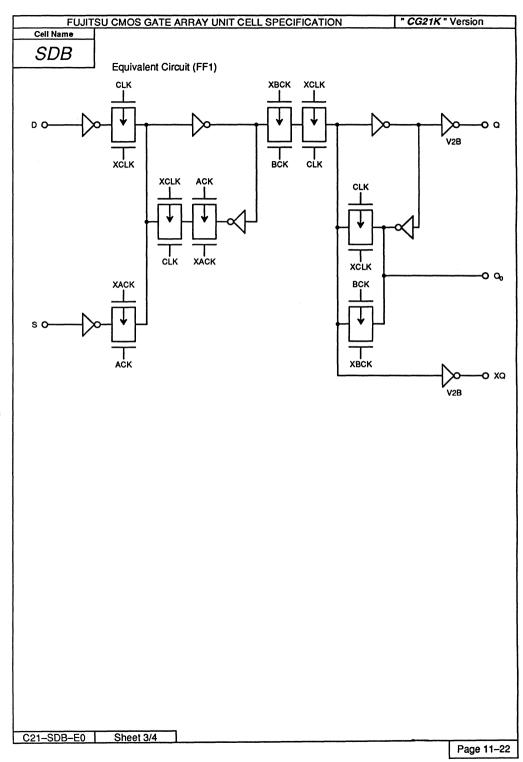
n = 1 ~ 4

C21-SDB-E0 Sheet 1/4

Page 11-20



3-141



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

Cell Name

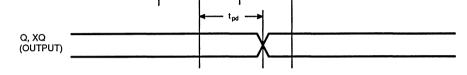
SDB

Definitions of Parameters

i) CLOCK MODE

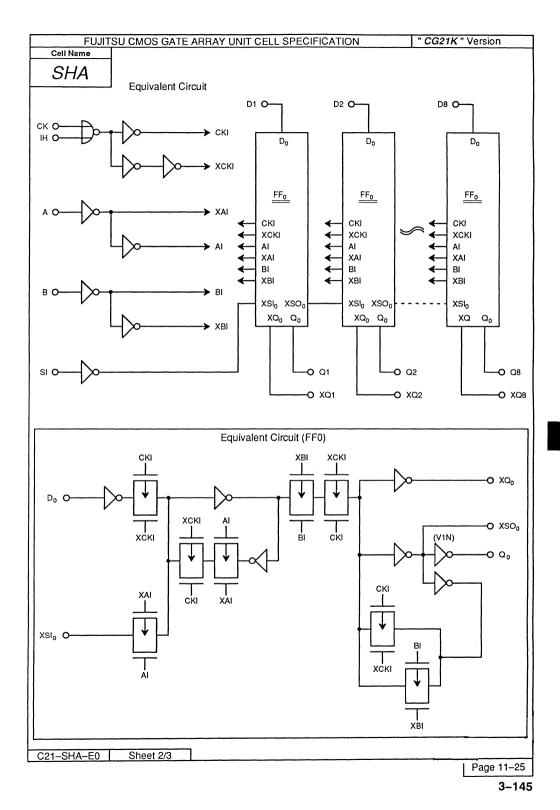
CLOCK

DATA

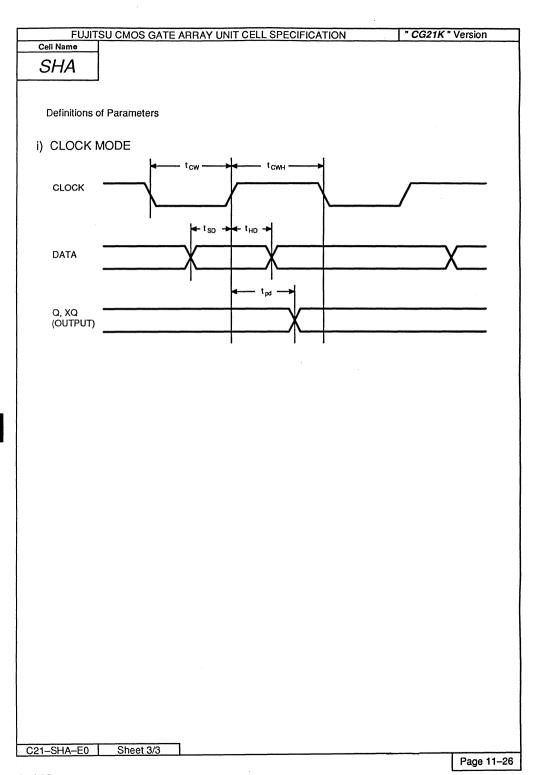


C21-SDB-E0 Sheet 4/4

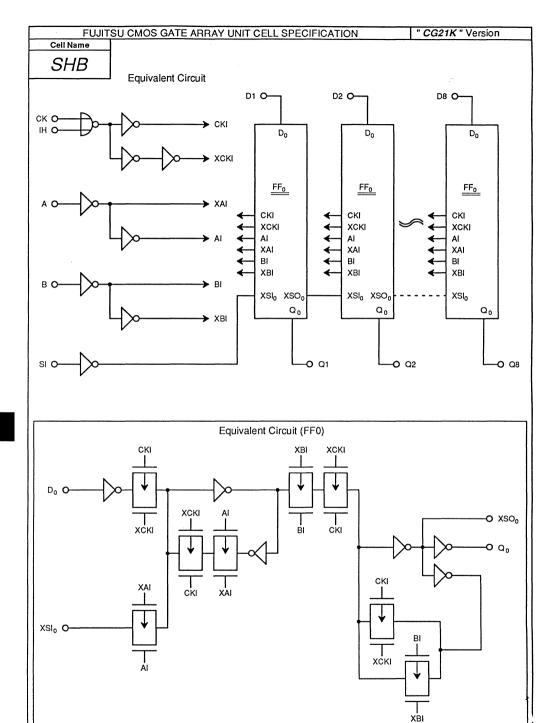
FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21k	" Version
Cell Name	Function							Number of BC
SHA	SCAN 1-input 8	-bit DF	F with C					68
Cell	l Symbol			Pro	pagation D		meter	
		t O	KCL	t O	KCL	ln KCL2	CDR2	Path
D1 ————————————————————————————————————	O1 O— XO1 —— Q2 O— XQ2 —— Q3 O— XQ3 —— Q4 O— XQ4 —— Q5 O— XQ5 O— XQ5	2.495 2.178	0.060 0.060	2.495 2.112	0.039 0.062	0.045 0.084		CK, IH to Q CK, IH to XQ
ск —	р—— хо <sub>б</sub>						1 1	
IH ————————————————————————————————————	Q7 D XQ7	Paramete					Symbol	Typ (ns) *
) A	Q8		ulse Widt				t cw	4.2
в — d	D XQ8	Clock P	ause Tim	e			t cwH	3.2
		Data Se	1.1					
		Data Ho	2.0					
Pin Name	Input Loading Factor (lu)							
D CK IH SI A B	1 1 1 1 1							
Pin Name	Output Driving Factor (lu)							
Q XQ	18 18		ues for the v	r the typical worst case			re given by the	e maximum delay
C21-SHA-E0	Sheet 1/3							I Bread St
								Page 11-24







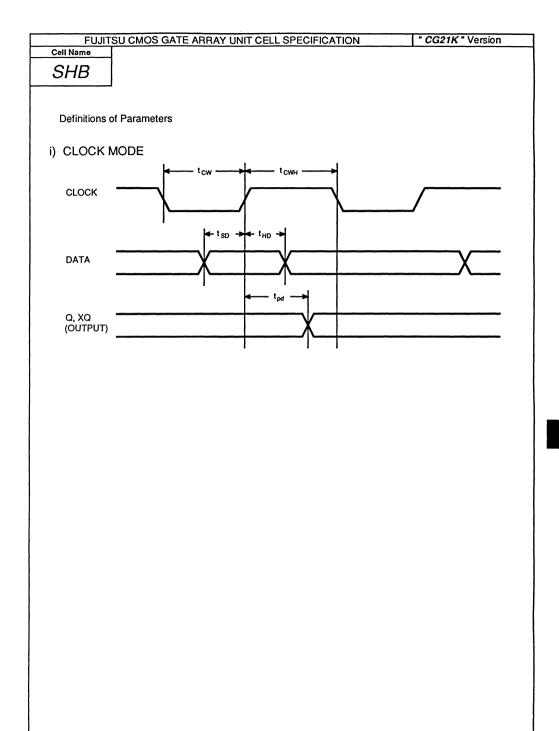
	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFIC	ATION		" CG21	K"∨	
Cell Name	Function		<del></del>					_	Number of BC
SHB	SCAN 1-input 8	B-bit DF	F with C	lock-In	hibit & 0	Q Outp	ut		62
Cel	l Symbol	1		Pro	pagation D	elay Parai	neter		
			ıp			dn			Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	<u> </u>	
		2.284	0.060	2.337	0.039	0.045	4	١٠	K, IH to Q
Г				Ì					
D1 ————————————————————————————————————	Q1 Q2			ĺ	ł	i	1		
D3 —	Q2 Q3								
D4	Q4				l				
D5	Q5								
D6 ———	Q6 Q7								
D8 ——	Q8								
ск —		·	1		ĺ				
IH —		}							
sı ——		Paramete	er	L	·		Symbol	<del>                                     </del>	Typ (ns) *
Å 📆		Clock P	ulse Widt				tcw		4.2
L		Clock P	ause Tim	ne			t cwH		3.2
		Data Se	etup Time				t <sub>SD</sub>	-	1.2
			old Time				t HD		2.0
	·								
Pin Name	Input Loading Factor (lu)								
D	1	1							
CK IH									
SI	1								
A B						1			
	Output Driving	1							
Pin Name	Factor (lu)								
Q	18				operating o		o givon by th	.a ma	ximum delay
		multiplie		WOISI Case	operating o	oridition ar	e given by a	ic ma	Aimon delay
		<u> </u>							
•									
			,						
C21-SHB-E0	Sheet 1/3								
								T	Page 11–27
								L	3–14
									J 14



Page 11-28

C21-SHB-E0

Sheet 2/3

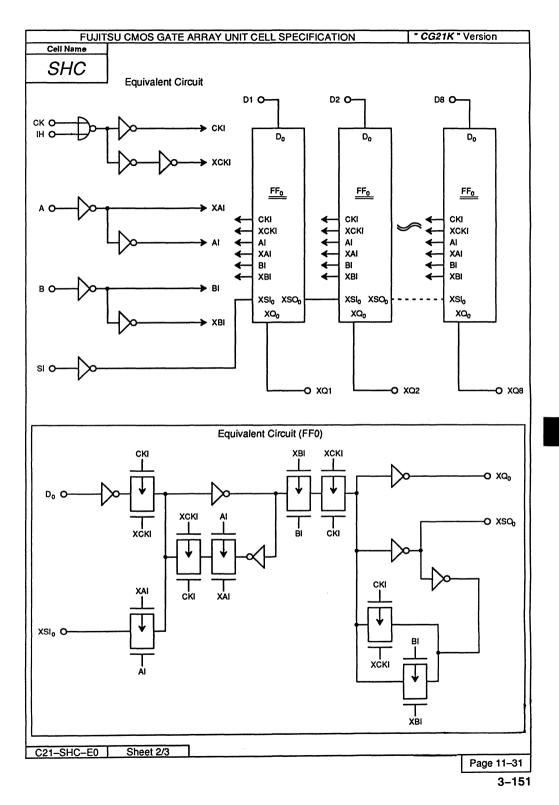


C21-SHB-E0

Sheet 3/3

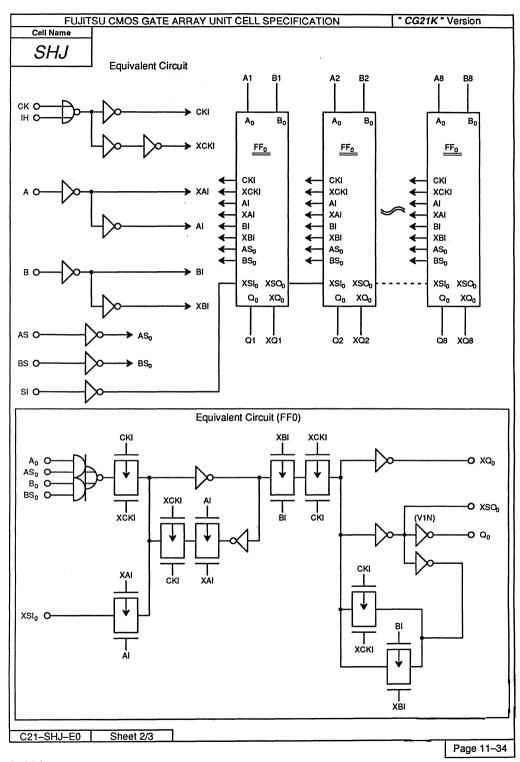
Page 11-29

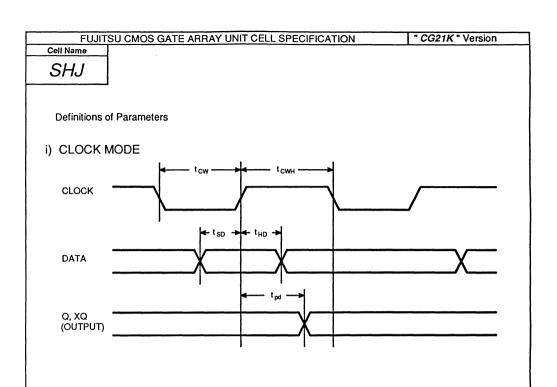
	SU CMOS GATE ARE	RAY LIMIT	CELLS	PECIFICA	ATION		" CG21F	<" '	Version
Cell Name	Function	1711 01111	OLLL O	2011 107	111011		1 002	•	Number of BC
SHC	SCAN 1-input 8	-bit DF	F with C	lock-In	hibit & X	(Q Out	out		62
Cell	l Symbol			Pro	pagation D	elay Paran	neter		
			ıp			dn			Path
ı		10	KCL	t O	KCL	KCL2	CDR2	L.,	
1		2.211	0.060	2.165	0.062	0.084	4		CK, IH to XQ
		l.				ł			
D1	р хоı					l			
D2	þ xo2					l			
D3	р— хоз					ļ			
D4	D	l					1		
D6	b xae								
D7	D XQ7					l	į i		
D8 ——	þ xos								
ск —			Ì			ł			
IH			Ì			]			
SI —		Paramete	l	L	L	<u>'                                     </u>	Symbol		Typ (ns) *
A			ulse Wid	h			tcw	_	4.2
в — q_			ause Tim				t cwn		3.2
1									
ı		Data Se	etup Time old Time				t <sub>SD</sub>	┡	1.2 2.0
Ì		Dala no	-	2.0					
	Input Loading	1							
Pin Name	Factor (lu)	1				ŀ			
D	1							1	
CK IH	1 1							١	
SI	i								
A B		l				- 1			
		]							
Pin Name	Output Driving Factor (lu)								
XQ	18	* Minimu	m values fo	r the typical	operating	condition.			
ı				worst case	operating c	ondition an	e given by th	e m	aximum delay
		multipli	er.						
	L	L							······································
2									
CO1 CUC FO	Choot 4/2								
C21-SHC-E0	Sheet 1/3							$\neg$	Page 11-30



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K " Version Cell Name SHC **Definitions of Parameters** i) CLOCK MODE t<sub>CWH</sub> CLOCK DATA Q, XQ (OUTPUT) C21-SHC-E0 Sheet 3/3 Page 11-32

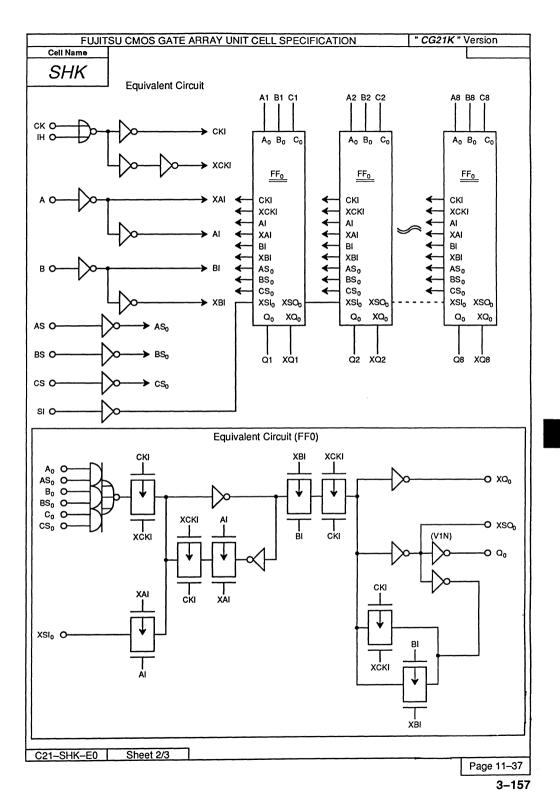
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version											
Cell Name	Function							Nu	mber of BC		
SHJ	SCAN 8-bit DFI	with C	lock–Inł				-		78		
Cell	l Symbol			Proj	pagation D		neter				
			p			ln	T		Path		
F		t0 KCL		t O	KCL	KCL2	CDR2				
A1	Q1	2.548	0.060	2.554	0.039	0.056	4		H to Q		
B1	p xq1	2.178	0.060	2.112	0.050	0.089	4	CK, I	H to XQ		
A2	Q2						1	l			
B2	D XQ2						1				
A3	Q3						1	ĺ			
В3	р хоз						ļ	1			
A4	Q4	1					ļ				
B4	b x04						İ	l			
A5	Q5 VO5						İ				
B5	р—— хо <sub>5</sub>						1	1			
A6	Q6						ļ	ļ			
B6	р— хо <sub>6</sub>							ŀ			
A7	Q7						ł	1	İ		
B7 ——	р—— хот	Paramete	i	L	L	L	l Symbol	T	ns) *		
A8	Q8 D		ulse Widt	·h					4.2		
B8	p— xus						t cw		3.2		
as —d		Clock P	ause Tim	ie			t cwh		3.2		
вs <b>— с</b>		Data Co	tun Timo						1 0		
ск —		Data He	tup Time	t sp							
ІН ——		Dala Fic	nu mne	t HD		1.5					
SI		į.									
Α						1		[			
B —− <b>q</b>	1					- 1		i			
						ł		l			
		1						i			
Pin Name	Input Loading										
	Factor (lu)					1					
An, Bn	1	l				ļ		ŀ			
(n=1~8)	1					- 1					
AS, BS CK	1					1		l			
IH	1					ł					
SI	1	1				- 1		{			
A, B	1	1				- 1					
Di- N	Output Driving	1									
Pin Name	Factor (lu)	<del>                                     </del>						l			
Q	18 18				operating o		aiuan bu 4	o meula-	m dolo:		
XQ	18	nultiplie		worst case (	operating of	oridition are	given by the	н шахіті	ini delay		
i		musupile	•••								
		L									
CO1 CILL EA 1	Shoot 1/2										
C21-SHJ-E0	Sheet 1/3							Des	10 11 22		
								Pag	je 11–33		



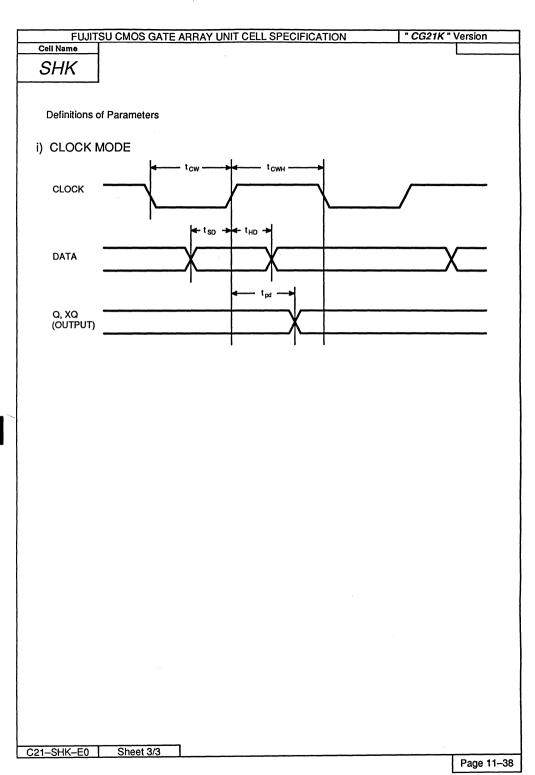


C21-SHJ-E0 Sheet 3/3

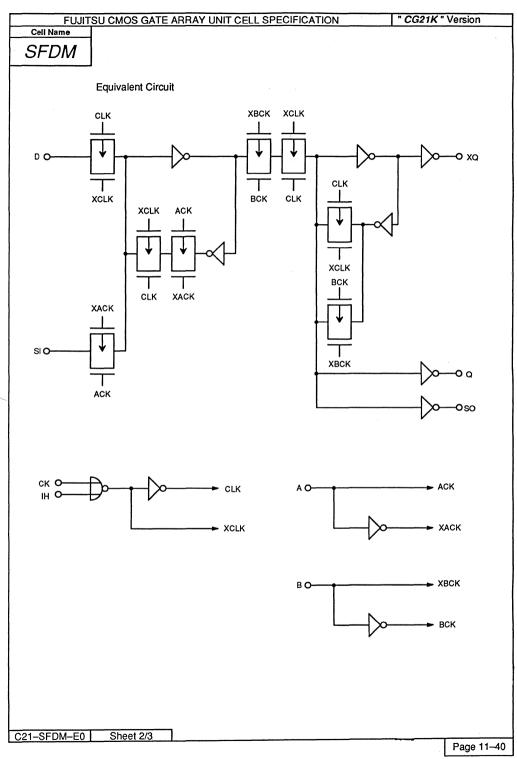
	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21F	(" Version
Cell Name	Function							Number of BC
SHK	SCAN 8-bit DFF	with C	lock–Ini				-	88
Cell	Symbol	tu		Proj	pagation D	elay Para In	ameter	
		t O	KCL	t O	KCL	KCL2	CDR2	Path
A1 ————————————————————————————————————	— Q1  — XQ1  — Q2  — XQ2  — Q3  — XQ3  — Q4  — XQ4	2.449 2.158	0.060 0.060	2.429 2.112	0.039 0.062	0.045 0.084	5 4	CK, IH to Q CK, IH to XQ
A5 ————————————————————————————————————	Q5							
C5 -	D XQ5	Paramete	er				Symbol	Typ (ns) *
A6	Q6	Clock P	ulse Widt	h			t <sub>CW</sub>	4.2
B6 —		Clock P	ause Tim	ie			t cwn	3.2
C6 —	р хоє	Data Se	etup Time				t <sub>SD</sub>	2.3
В7 —	Q7	Data Ho	old Time				t <sub>HD</sub>	1.8
C7	р хол							
A8 ————————————————————————————————————	Q8					l		
C8 ——	b xas							
AS —C BS —C CS —C CK								
SI ————————————————————————————————————								
Pin Name	Input Loading							
An, Bn, Cn	Factor (lu)	1						
(n=1 ~ 8) AS, BS, CS CK IH	1 1							
SI A, B	1							
Pin Name	Output Driving Factor (lu)							
Q XQ	18 18		ues for the	r the typical worst case				ne maximum delay
		Lance Later Control						
C21-SHK-E0	Sheet 1/3							Page 11–36

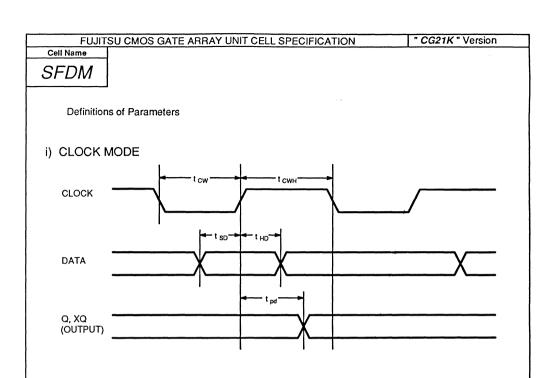






Cell Name   Function   SFDM   SCAN 1-input DFF with Clock-Inhibit   10	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Vers											
Cell Symbol   Symbol   Typ (ng)				<u> </u>					Number of BC			
To   KCL   10   KCL   KCL2   CDR2   Path			FF with	Clock-					10			
10   KCL   10   KCL   CDR2   Path	Cell	Symbol			Pro			meter				
1.221   0.060   1.254   0.045   0.078   4   CK to C					• • •			Longo	Path			
CK   H   SO   SO   Parameter   Symbol   Typ (ns)*   Clock Pulse Width   tow   2.5   Clock Pause Time   town   2.5   Data Setup Time   tso   1.0   Data Hold Time   Tho   0.8    Plin Name   Factor (tu)   DCK   1   H   1   1   SI   2   2   A, B   2   2   A, B   18   18    Plin Name   Factor (tu)   Coulput Driving Factor (tu)   Coulput Dr	-		1.221	0.060	1.254	0.045	0.078	4				
Clock Pulse Width tow 2.5 Clock Pause Time tow 2.5  Data Setup Time tso 1.0 Data Hold Time the the O.8  Pin Name Factor (tu)  D C C T T T T T T T T T T T T T T T T T	CK IH SI A	<b>р</b> —— хо	Poramot	:				Sumbal	Tun (ne) *			
Clock Pause Time town 2.5    Data Setup Time   town   1.0					h							
Pin Name   Input Loading Factor (lu)    D   2   CK   1   IH   1   1   SI   2   2   A, B   2   Pin Name   SO   18   SO   18   18    - Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			Clock P	ause Tim	ie							
Pin Name   Input Loading Factor (lu)    D   2   CK   1   IH   1   SI   2   A, B   2   A, B   18   SO   18   SO   18    * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.												
Pin Name   Input Loading Factor (lu)    D			Data Se									
Pin Name Factor (lu)  D CK II III SI SI SI A, B D Output Driving Factor (lu)  O SO 18 18 18  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			Data Figure 1 thb 1 0.0									
C21-SFDM-E0   Sheet 1/3	D CK IH SI A, B Pin Name	2 1 1 2 2 2  Output Driving Factor (lu)  18 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the ma										
OZI-OI DIN-EU   Gricet 170	C21_SEDM_E0	Sheet 1/3										
Page 11–39	OZITOI DIVITED	Officer 1/0						* <u></u>	Page 11-39			



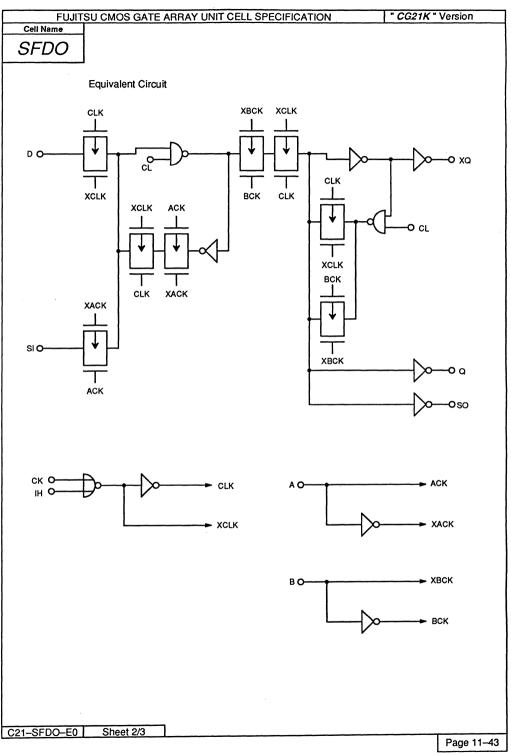


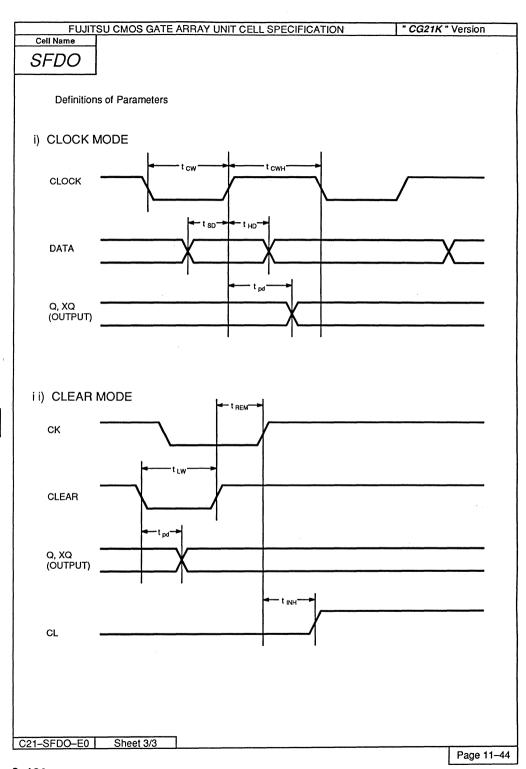
C21-SFDM-E0

Sheet 3/3

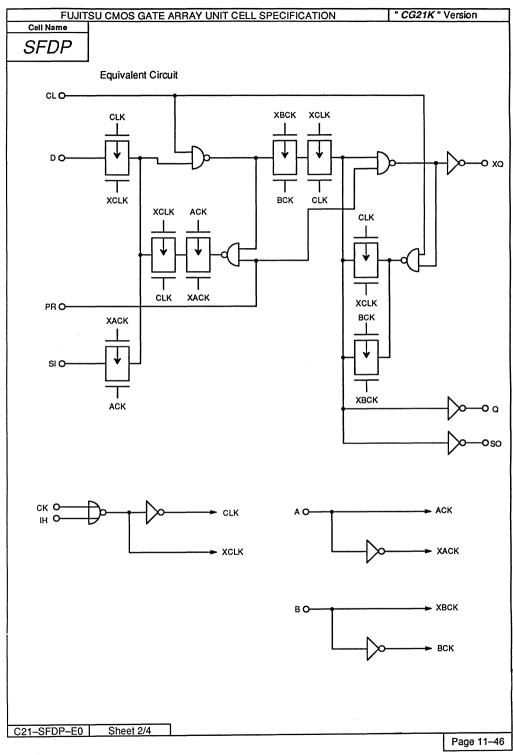
3-161

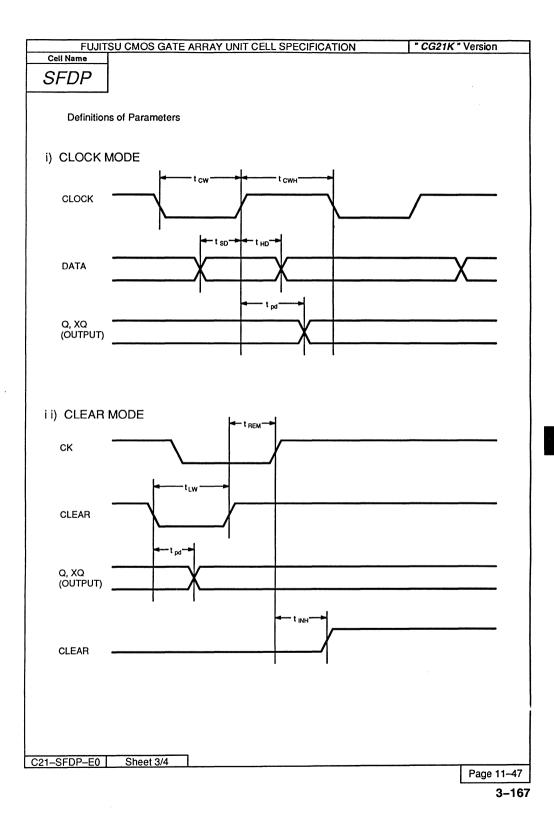
Cell Name   Function   SFDO   SCAN 1-input DFF with Clear and Clock Inhibit   11	FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Symbol   Propagation Delay Parameter   Usp   Ito   KCL   Ito   KCL   KCL2   CDR2   Path   Ito   KCL   Ito   KCL   KCL2   CDR2   Path   Ito   KCL   Ito   KCL   KCL2   CDR2   Path   Ito   Ito   KCL   Ito   KCL   KCL2   CDR2   Path   Ito   Ito   KCL   Ito   It									Number of BC
To   KCL   10   KCL   KCL   CDR2   Path	SFDO	SCAN 1-input D	FF with	Clear	and Clo	ck Inhibi	t		11
1.0   KCL   1.0   KCL   KCD   KCD   CORP   Fath	Celi	Symbol			Pro			neter	
1.413   0.064   1.347   0.050   0.084   4   CK to O								0000	Path
Pin Name	CK —— IH —— SI —— A ——	р хо	1.413 1.564	0.064 0.060	1.347 1.729	0.050 0.039	0.084 0.045	4 4	CK to XQ
Pin Name		7					ĺ		
Pin Name		1							
Clock Pause Time		CL							
Data Setup Time									
Pin Name   Input Loading Factor (lu)   Clear Pulse Width   t.t.w   2.5   D			CIOCK P	ause IIII	t CWH	2.3			
Pin Name   Input Loading   Clear Pulse Width   t Lw   2.5			Data Se	1.6					
Pin Name    Factor (lu)   Clear Release Time   t REM   1.2			Data Ho	ld Time				t <sub>HD</sub>	1.1
Pin Name    Factor (lu)   Clear Release Time   t REM   1.2	ļ	Innut I and Inn	Cloar P	ulco Widt	h			+	25
CL Clear Hold Time t INH 2.9    Clear Hold Time	Pin Name	Factor (lu)	Clear R	elease Ti	me				
Pin Name Factor (lu)  Q 18 XQ 18 SO 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-SFDO-E0 Sheet 1/3	D	2	Clear H	old Time					
C21-SFDO-E0   Sheet 1/3	SI A, B CL Pin Name	Output Driving Factor (lu) 18 18	The val	ues for the				given by the	naximum delay
Page 11–42	C21_SFDQ_F0	Sheet 1/3							
1 1 440 11 36	021-31-DO-E0	SHEEL I/S							Page 11-42

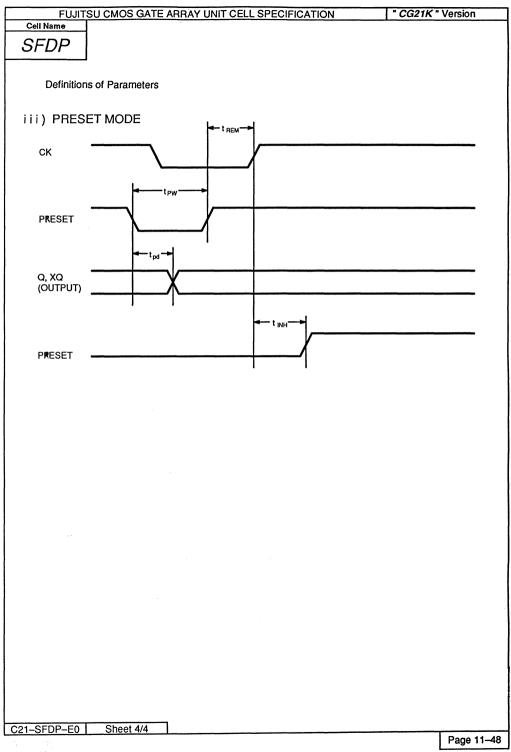




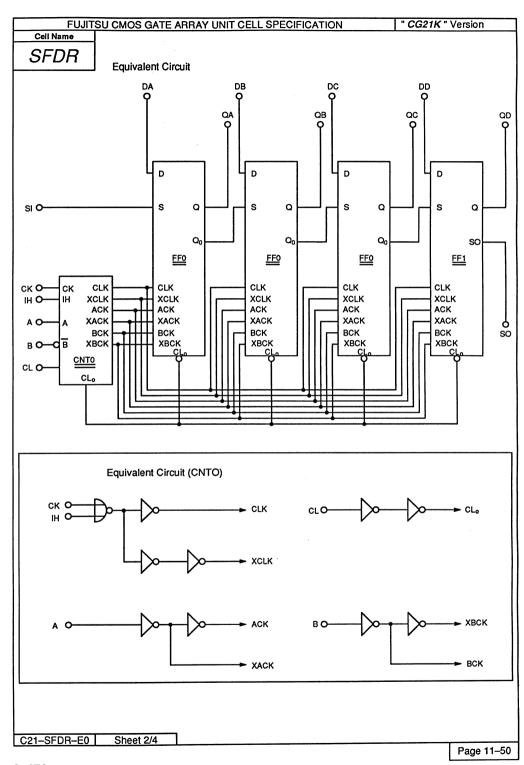
Cell Name   Function   SFDP   SCAN 1-input DFF with Clear, Preset, and Clock Inhibit   12	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version										
Cell Symbol   Not										Number of BC	
To   KCL   10   KCL   KCL   CDR2   Path			FF with	Clear,						12	
10   KCL   10   KCL   KCL2   CORP   Path	Cel	l Symbol			Proj			neter			
1.426					t O			CDR2		Path	
Clock Pulse Width	CK	- a - xa	1.426 1.888 1.921	0.064 0.060 0.060	1.340 1.729 1.419	0.050 0.039 0.050	0.084 0.045 0.084	4 4 4	0	K to XQ L to Q,XQ	
Clock Pulse Width			Dozomoto	<u> </u>		<u> </u>	<u> </u>	Cumbal		Tun (na) t	
Clock Pause Time		ĊL			h						
Data Setup Time											
Pin Name   Input Loading Factor (lu)   Clear Pulse Width   1 tuw   2.5											
Pin Name   Input Loading Factor (lu)   Clear Pulse Width   1 tuw   2.5											
Pin Name  D Clear Release Time Clear Hold Time			Data Ho	ola i ime				I HD			
Pin Name   Factor (Iu)   Clear Release Time   t nem   1.2   D   2   Clear Hold Time   t nm   2.9   CK, IH   1   SI   2   A, B   2   Preset Pulse Width   t pw   3.6   CL, PR   2   Preset Release Time   t nem   0.6   Preset Release Time   t nem   0.6   Preset Release Time   t nm   3.6    Preset Hold Time   t nm   3.6    Output Driving   Factor (Iu)   3.6    O		Input Loading	Clear P	ulse Widt	h			t <sub>LW</sub>		2.5	
CK, IH SI A, B CL, PR 2 Preset Pulse Width Preset Hold Time 1 NAME Preset Hold Time 1 NAME  A 18 A 2 A 18 A 3.6 A 18 A 18 A 3.6 6 A 3.6 A 3	Pin Name		Clear R	elease Ti							
Preset Hold Time tinh 3.6  Plin Name Factor (tu)  Q 18 XQ 18 SO 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-SFDP-E0 Sheet 1/4		2	Clear H	old Time	t INH		2.9				
Preset Hold Time tinh 3.6  Plin Name Factor (tu)  Q 18 XQ 18 SO 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-SFDP-E0 Sheet 1/4		2	Procet I	Pulsa Wic	lth			t ow		3.6	
Preset Hold Time tinh 3.6  Plin Name Factor (tu)  Q 18 XQ 18 SO 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21-SFDP-E0 Sheet 1/4	A, B	2									
Pin Name    Sector (lu)	CL, PR	2						3.6			
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  * Minimum values for the typical operating condition are given by the maximum delay multiplier.  **C21-SFDP-E0** Sheet 1/4**		Factor (lu)									
C21-SFDP-E0   Sheet 1/4	XQ	18	The val	ues for the v	the typical worst case	operating o	condition.	given by th	e ma	ıximum delay	
I Page 11_45 I	C21-SFDP-E0	Sheet 1/4								Page 11_45	
Page 11–45										Page 11–45	

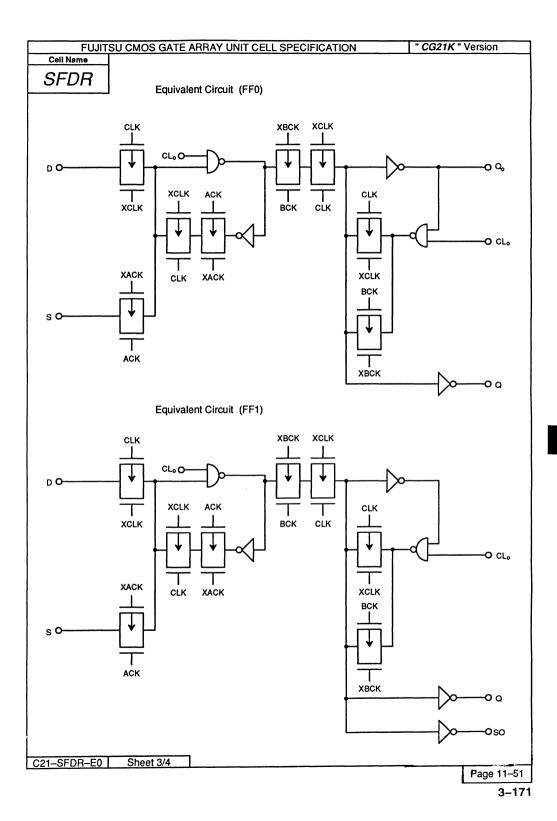


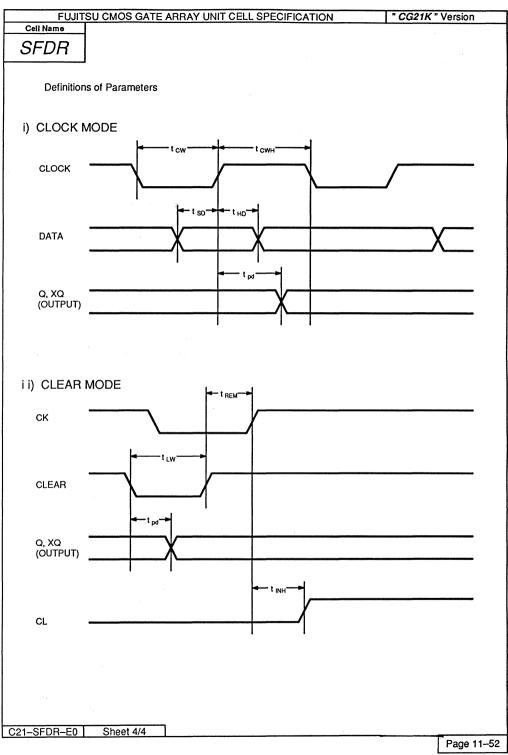




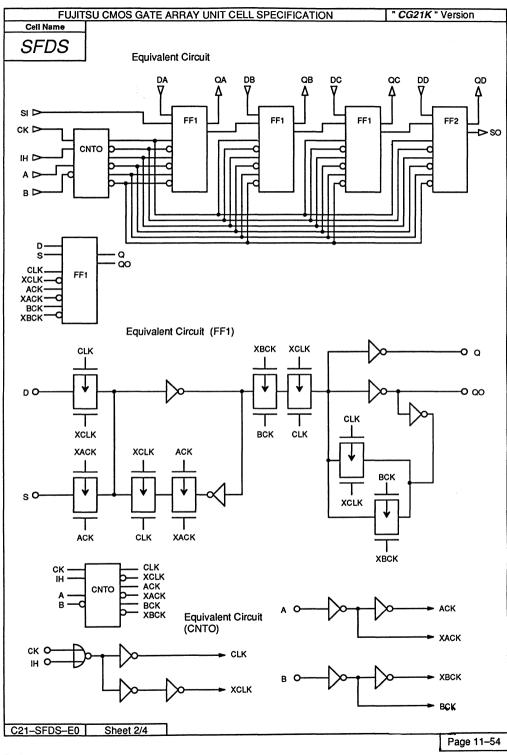
Cell Name  SFDR  Cell  DA ———————————————————————————————————	Function  SCAN 4—input E  Symbol  OA OB OC OD SO  CL  Input Loading Factor (lu)  2 1 2 1 1	Parameter Clock Pa Clock Pa Data Set Data Ho Clear Pu Clear Ho	KCL 0.064 0.	Prop t 0 1.980 2.026	ck Inhibi pagation D. tc KCL 0.050 0.050	elay Param In KCL2 0.084 0.089	Symbol tew temperature to the temperature	Path CK to Q CL to Q  Typ (ns) * 2.5 3.2  0.7 1.5  2.5 1.7 3.4
DA DB DC DD CK IH SI DC CK, IH SI A DC CK, IH SI A, B CL Pin Name	Symbol  OA OB OC OD SO  Input Loading Factor (Iu)	Parameter Clock Pt Clock Pa Data Set Data Ho Clear Pt Clear Re	KCL 0.064 0.	Prop t 0 1.980 2.026	pagation Detection KCL	elay Param In KCL2 0.084 0.089	CDR2 4 4 4 tcw tcw tthD tthU trem	Path  CK to Q  CL to Q  Typ (ns) *  2.5  3.2  0.7  1.5  2.5  1.7
DA —— DB —— DC —— DD —— CK —— IH —— SI —— A —— C  Pin Name  CK, IH SI A, B CL  Pin Name	OA OB OC OD OC	Parameter Clock Pt Clock Pt Data Set Data Ho Clear Pt Clear Re	rulse Widtause Time	10 1.980 2.026	KCL 0.050	NCL2 0.084 0.089	CDR2 4 4 4 tcw tcw tthD tthU trem	Typ (ns)* 2.5 3.2 0.7 1.5
DB — DC — DD — CK — IH — SI — D — CK, IH SI A, B — CL — Pin Name — Q	OB OC OD OC	Parameter Clock Pt Clock Pt Data Set Data Ho Clear Pt Clear Re	rulse Widtause Time	1.980 2.026	KCL 0.050	0.084 0.089	Symbol tcw tcwh tsD thD	Typ (ns)* 2.5 3.2 0.7 1.5
DB — DC — DD — CK — IH — SI — D — CK, IH SI A, B — CL — Pin Name — Q	OB OC OD OC	Parameter Clock Pt Clock Pt Data Set Data Ho Clear Pt Clear Re	rulse Widt ause Time Id Time	1.980 2.026	0.050	0.084	Symbol tcw tcwh tsD thD	Typ (ns) * 2.5 3.2 0.7 1.5 2.5 1.7
DB — DC — DD — CK — IH — SI — D — CK, IH SI A, B — CL — Pin Name — Q	OB OC OD OC	Clock Pa Clock Pa Data Set Data Ho Clear Pu Clear Re	ulse Widt ause Time tup Time Id Time ulse Widt elease Ti	h			t cw t cwh t sp t hp t lw t rem	2.5 3.2 0.7 1.5 2.5
D CK, IH SI A, B CL Pin Name	Input Loading Factor (lu)	Data Ser Data Ho Clear Pu Clear Re	tup Time Id Time Ilse Widt elease Ti	h			t sd t hd t lw t rem	0.7 1.5 2.5 1.7
D CK, IH SI A, B CL Pin Name	Factor (lu)	Clear Pu	ld Time Ilse Widt elease Ti	h			t <sub>HD</sub>	1.5 2.5 1.7
D CK, IH SI A, B CL Pin Name	Factor (lu)	Clear Pu	ld Time Ilse Widt elease Ti	h			t <sub>HD</sub>	1.5 2.5 1.7
D CK, IH SI A, B CL Pin Name	Factor (lu)	Clear Re	elease Ti				t REM	1.7
D CK, IH SI A, B CL Pin Name	Factor (lu)	Clear Re	elease Ti				t REM	1.7
D CK, IH SI A, B CL Pin Name								
CK, IH SI A, B CL Pin Name	1 2							
	Output Driving Factor (lu)  18 18		es for the		operating co		given by th	e maximum delay
C21–SFDR–E0 ↓								Page 11–49

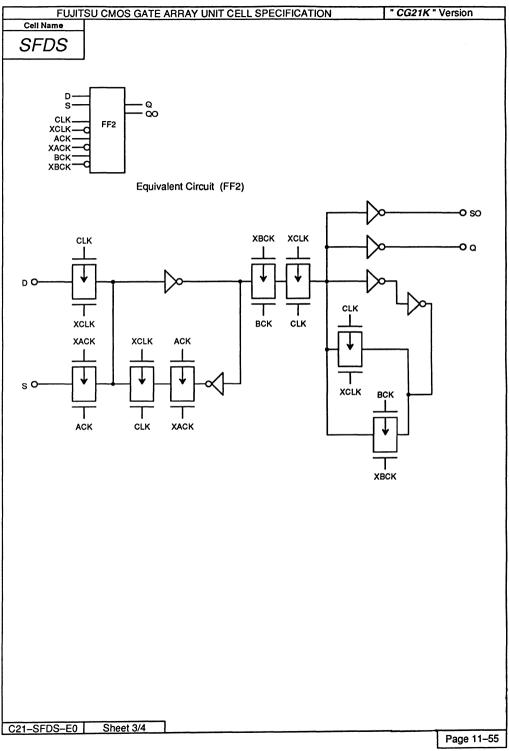


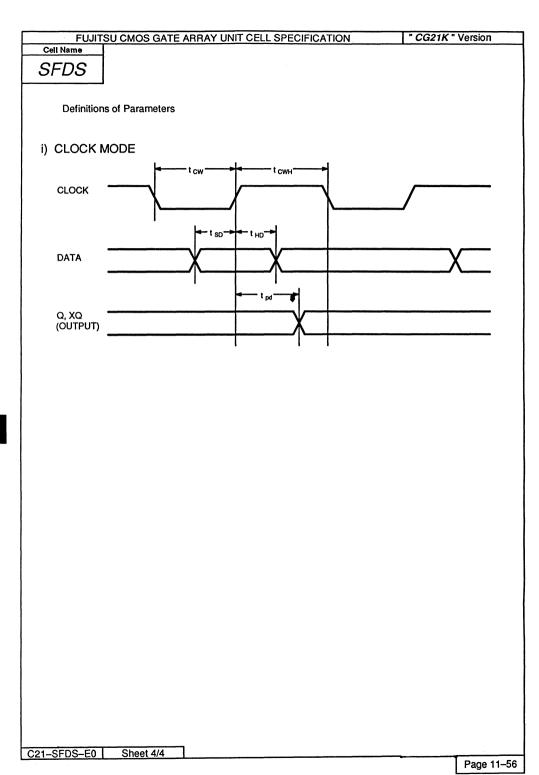




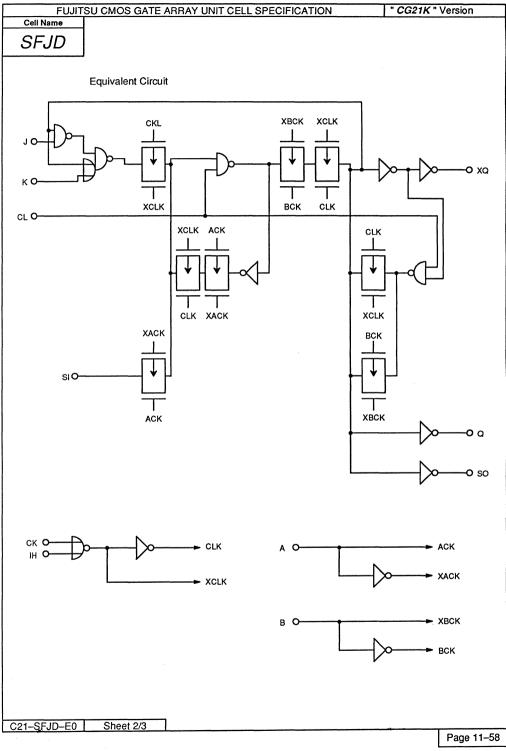
FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFIC/	ATION		" CG21	K"\	/ersion
Cell Name	Function								Number of BC
SFDS	SCAN 4-input E	FF with	Clock I	nhibit					31
Cell	Symbol			Proj	pagation D		ameter	<del></del>	
		t O	IP KCL	t O	KCL	n KCL2	CDR2	1	Path
F		1.624 1.736	0.060 0.060	1.597 1.716	0.045 0.045	0.073	3 4		( to QA~QC ( to QD
DA	OA OB OC OD SO								
ı		Paramete		-			Symbol	┼	Typ (ns) * 2.5
		Clock P	ulse Widt ause Tim	e			t cw	1	3.2
							t sp		
		Data Se	-	0.0 1.3					
		Data Ho	old Time				t HD	L	1.3
Pin Name  D CK, IH SI A, B	Factor (Iu)  2 1 2 1 1 Output Driving Factor (Iu) 18								
so	18						are given by the	he ma	aximum delay
C21-SFDS-E0	Sheet 1/4		,						
021-SFDS-E0	Sneet 1/4							$\neg$	Page 11-53
								L	2 172

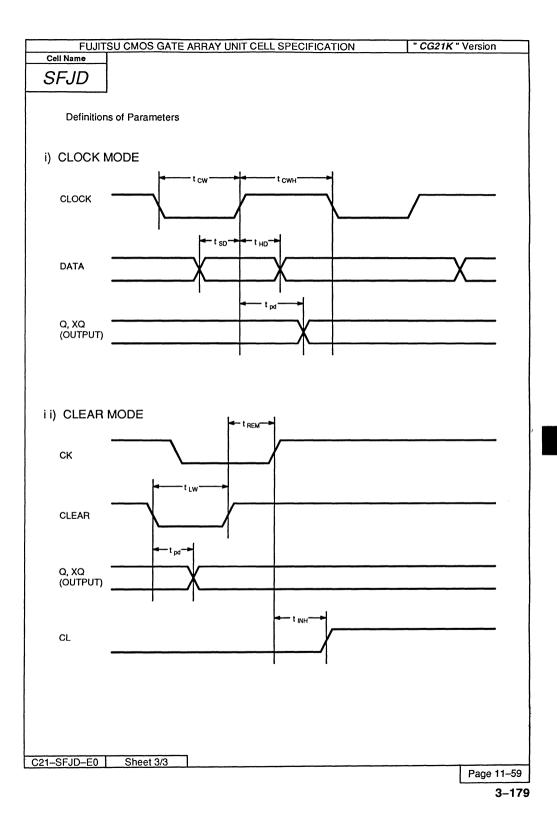






Cell Name SFJD	SU CMOS GATE ARE Function SCAN J–K FF w							" Version Number of
SEID	SCAN I KEEN		Number of					
0100	SCAN J-K FF W	ith Cloc	k Inhibit					14
Cel	l Symbol			Pro	pagation D		neter	
		t 0	KCL	t O	KCL	In KCL2	CDR2	Path
Ј	a xa so	1.710 1.828 1.479	0.064 0.060 0.060	1.584 2.000 1.307	0.056 0.039 0.039	0.089 0.045 0.078	4 4 4	CK to Q CK to XQ CL to Q,XQ
		Paramete					Symbol	Typ (ns) *
	CL		ulse Widt				tow	2.5
		Clock P	ause Tim	ie			t cwh	2.5
		Data So	tup Time	(J)			t <sub>SD</sub>	2.2
		Data Ho	old Time	(J)			t HD	0.4
m	Input Loading	Data Se	tup Time	(K)			t <sub>SD</sub>	1.9
Pin Name	Factor (lu)	Data Ho	old Time	(K)		t <sub>HD</sub>	0.1	
J, K CK, IH	1 1 2 2 2	Clear Pi	ulse Widt	h		t <sub>LW</sub>	2.5	
SI A, B	2	Clear R	elease Ti			t REM	1.2	
ĊL CL	2	Clear H	old Time			L_	t INH	2.6
Pin Name Q XQ SO	Output Driving Factor (lu) 18 18 18	* Minimur The valu multiplie		r the typical worst case	operating o	condition.	e given by the	e maximum delay
C21-SFJD-E0	Sheet 1/3						· ·	Dan 11 F
								Page 11-5

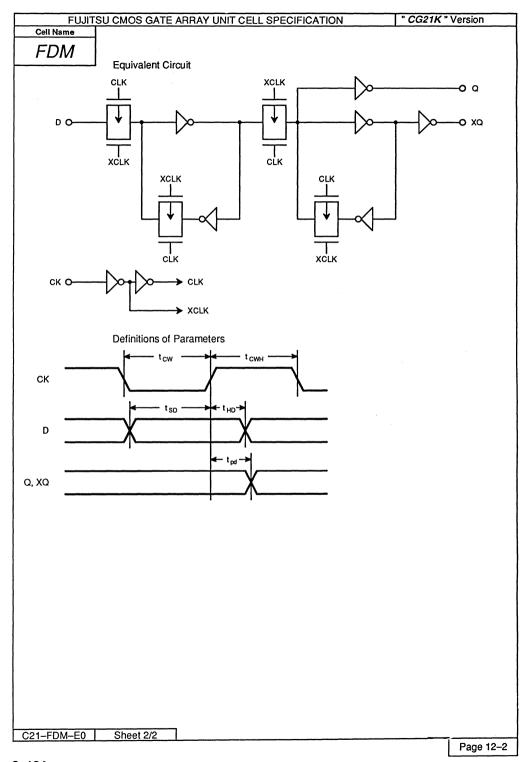




# Non Scan Flip-Flop Family

Page	Unit Cell Name	Function	Basic Cells
3–183	FDM	Non-Scan D FF	6
3-185	FDN	Non-Scan D FF with Set	7
3–187	FDO	Non-Scan D FF with Reset	7
3-189	FDP	Non-Scan D FF with Set and Reset	8
3-192	FDQ	Non-Scan 4-bit D FF	21
3-194	FDR	Non-Scan 4-bit D FF with Clear	26
3–197	FDS	Non-Scan 4-bit D FF	20
3–199	FD2	Non-Scan Power D FF	7
3-201	FD3	Non-Scan Power D FF with Preset	8
3–203	FD4	Non-Scan Power D FF with Clear and Preset	9
3–205	FD5	Non-Scan Power D FF with Clear	8
3–207	FJD	Non-Scan Positive Edge Clocked Power J-K FF with Clear	12

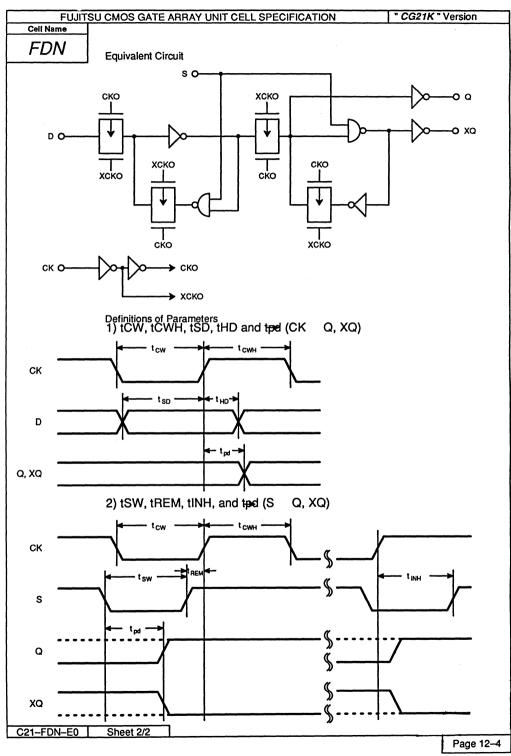
FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	( " Version
Cell Name	Function							Number of BC
FDM	Non-SCAN DF	F						6
Cel	Symbol			Pro	pagation D		neter	
			lb KOI			ln KOLO	CDR2	Path
		0.924	KCL	t 0 0.951	ксL 0.039	KCL2	CDH2	CK to Q
		1.142	0.060 0.060	1.248	0.039			CK to XQ
D —	a							
ск ——	1		1	İ				
	<b>р</b> — ха	Ì						
<u> </u>		l		l			1	
				L				
		Paramete					Symbol	Typ (ns) *
		Clock P	ulse Wid	<u>th</u>			tcw	2.5 2.5
		Clock	ause Tim	ie			t cwH	2.3
		Data Se	etup Time	)			t sp	1.3
		Data Ho	old Time				t <sub>HD</sub>	0.9
	Input Loading	┨						
Pin Name	Factor (lu)					•		
D	2 1	1						
СК	1	1						
		1						
		j						
Pin Name	Output Driving	}						
Q	Factor (lu)	4						
χα	18 18	Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay.						
		multiplie	er.					
Function Table								
Inputs	Outputs							
D CK	Q XQ							
н 1	H L							
L T	LH							
C21-FDM-E0	Sheet 1/2							
								Page 12–1



FUJIT	SUCM	CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version									
Cell Name		nction			OLLLO		THOIT		1 002	Number of BC	
FDN	Nor	-SCAN	1 DFF	with S	ET					7	
Cel	l Symbol					Pro	pagation D		neter		
					ip			in	1 0000	Path	
				10 0.051	KCL	t 0	KCL	KCL2	CDR2	CK to Q	
				0.951 1.300 1.182	0.060 0.060 0.060	0.924 1.281 0.568	0.039 0.039 0.039	0.056	4	CK to XQ S to Q, XQ	
ск ——											
				Paramete					Symbol	Typ (ns) *	
				Clock P	ulse Widt	<u>h</u>			tcw	2.5 2.5	
				Clock Pause Time					t cwn	2.5	
				Data Se	tup Time				tsp	1.3	
				Data Hold Time t <sub>HD</sub>					t <sub>HD</sub>	0.9	
	T	ut Loading		Set Pulse Width					tsw	2.5	
Pin Name		actor (lu)	3		ease Tim	e (S)			t REM	0.3	
D		2		Set Hold					t inn	2.3	
S CK		2 2 1									
									:		
Pin Name	l Gu	tput Drivin actor (lu)	g								
χQ		18 18			ues for the		operating o		given by th	e maximum delay	
Function Table	Function Table										
Inputs	Inputs Outputs			1							
S D	ск			]							
L X	Х	Н	L	ļ							
н н	1			}							
H L	1	L	Н								

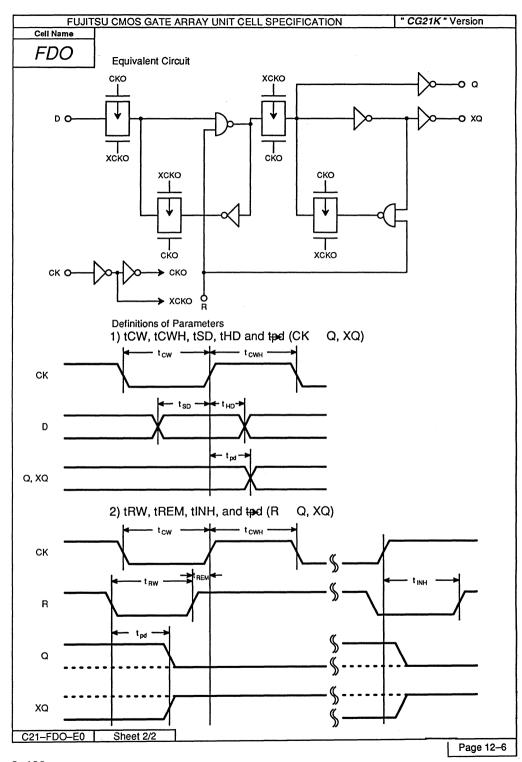
C21-FDN-E0 | Sheet 1/2

Page 12-3



FILIT	SUCM	CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version										
Cell Name		nction		OLLEG	. 2011 10	111011		1	Number of BC			
FDO	Non	-SCAN DI	F with R	ESET					7			
Cel	l Symbol				Pro	pagation D	elay Paran	neter				
				Jp			dn		Path			
			10	KCL	t0	KCL	KCL2	CDR2				
			1.023 1.142 1.056	0.060 0.060 0.060	0.944 1.366 0.865	0.045 0.039 0.045			CK to Q CK to XQ R to Q, XQ			
О — О СК — ХО												
	Ř		Paramete					Symbol	Typ (ns) *			
				ulse Wid				tcw	2.5			
			Clock P	ause Tim	ie			t cwn	2.5			
			Data Se	Data Setup Time					1.3			
				Data Hold Time					0.9			
Pin Name		ut Loading	Reset F	Reset Pulse Width t Reset Release Time (R) t Re					2.5			
		actor (lu)	Heset F	Reset Release Time (R) Reset Hold Time					0.6 2.0			
D R CK		2 2 1	Hesett	iola Time				t inh	<b>L.</b> 0			
Pin Name	Out	tput Driving										
Q XQ	F	18 18 18						given by the	e maximum delay			
Function Table												
Inputs		Outputs										
R D	СК	Q XQ										
L X	х	L H										
н н	<b>↑</b>	НЬ										
H L												

$C_2$	'1-	Fυ	$\mathcal{O}_{-1}$	=0	l Sneet	1/2
_						



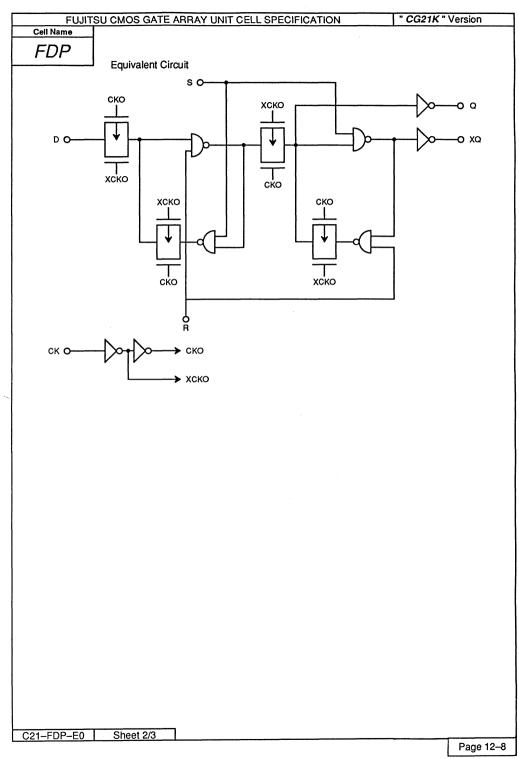
	ISU CMOS GATE AR	RAY UNIT	r cell s	PECIFIC	ATION		" CG21	<i>K</i> " Version
Cell Name	Function							Number of BC
FDP	Non-SCAN DF	F with S	et and F	Reset				8
Cel	ll Symbol	T		Pro	pagation D	elay Para	meter	<del></del>
		tı	up		to	dn		Path
		t O	KCL	t 0	KCL	KCL2	CDR2	Pain
р ——	1.036 1.294 1.182 1.340	0.060 0.060 0.060 0.060	0.931 1.320 0.838 0.535	0.045 0.039 0.045 0.039			CK to Q CK to XQ R to Q, XQ S to Q, XQ	
	Ř	Parameter					Symbol	Typ (ns) *
		Clock Pulse Width					t <sub>CW</sub>	2.5
		Clock Pause Time					t cwn	2.5
								ļ
			etup Time	!			t <sub>SD</sub>	1.3
ļ		Data Ho	old Time				t HD	0.9
		<u> </u>						
Pin Name	Input Loading		se Width				t sw	2.5
	Factor (lu)		ease Tim	<u>e (S)</u>			t REM	0.3
D	2 2 2	Set Hole	d Time				t inn	2.3
S R	2							25
l ck	1 1		Pulse Wid				t RW	2.5
			Release T				t REM	0.6 2.0
		Reset F	lold Time				t INH	2.0
Pin Name	Output Driving Factor (lu)	_						
a xa	18 18						re given by th	L ne maximum delay

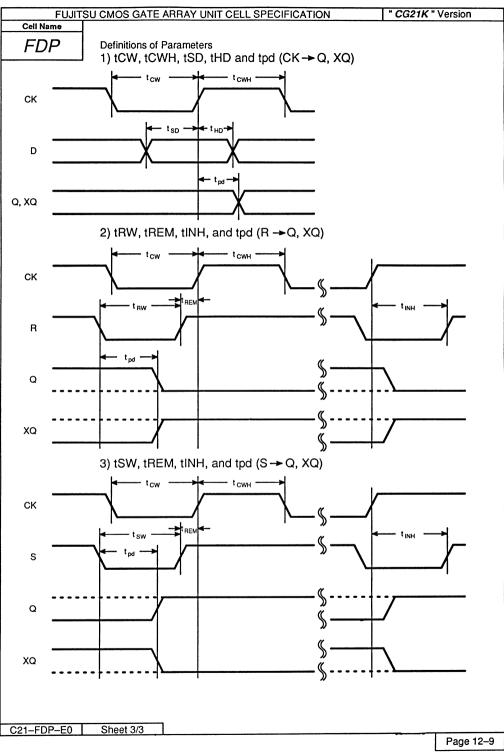
multiplier.

## Function Table

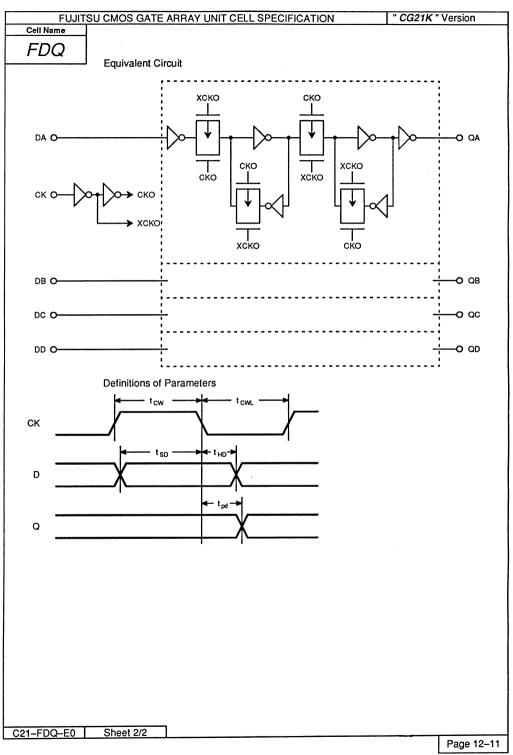
		Inp	uts		Ou	tputs
	s	R	D	ск	Q	XQ
ſ	Н	L	х	х	L	Н
l	L	Н	x	х	Н	L
1	L	L	x	х	Inhi	bited
1	н	н	н	1	Н	L
L	н	н	L	1	L	н

C21-FDP-E0 Sheet 1/3

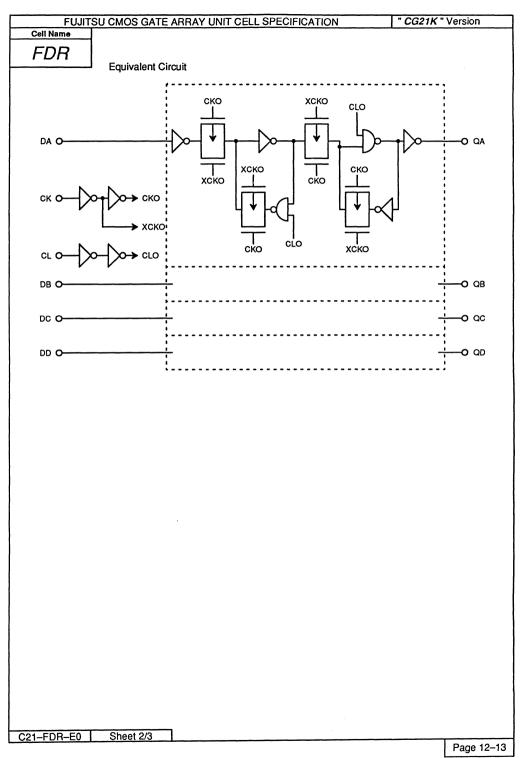


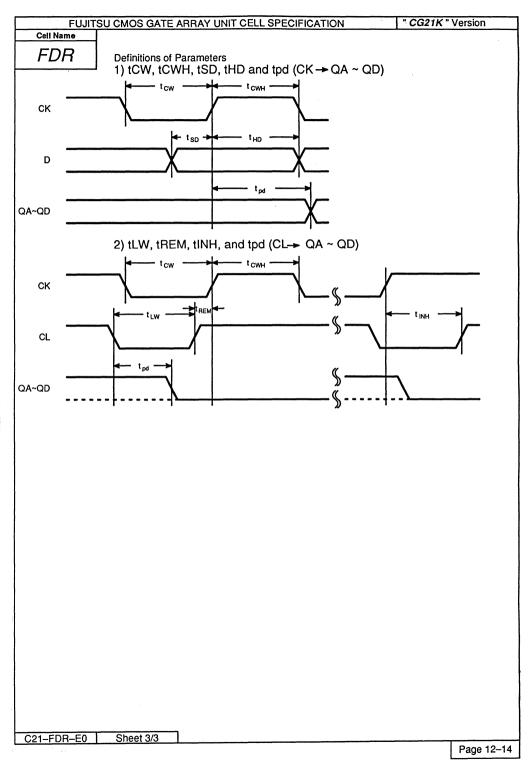


	ITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version									
Cell Name		CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K" V Function								
								Number of BC		
FDQ	Non-SCAN 4-b	it DFF						21		
	   Symbol	т	<del></del>	Dro	pagation D	olav Parom	neter	L		
Cen	ТЭУШЬОГ	tı tı	ıp	F101		in raian	ietei			
		t O	KCL	t O	KCL	KCL2	CDR2	Path		
		1.782	0.060	1.446	0.039			CK to Q		
				'						
		Í					1 1			
DAD	BDCDD									
	III									
		1								
	QA	ŀ								
	QB QB	İ								
ск — ф	— ac	ŀ								
	QD									
ļ <u>L</u>										
		Paramete	er	L	<u> </u>	<u> </u>	Symbol	Typ (ns) *		
			ulse Wid				tcw	2.5		
			ause Tim				t cwL	2.5		
		Data Se	etup Time old Time				t sp	0.7 1.7		
1		Data H	na rine				t <sub>HD</sub>	1.7		
	Input Loading	1				- 1				
Pin Name	Factor (lu)	J								
D	1	]				l	1			
ск	1	1				1				
		1								
	Output Driving	1								
Pin Name	Factor (lu)									
Q	18									
		* Minimu	m values fo	r the typical	operating of	condition.				
			maximum delay							
		multiplie	JI.							
Function Table										
Input	Output									
	<del></del>									
CK D	°									
↓ н	Н									
	[									
C21-FDQ-E0	Sheet 1/2									
								Page 12-10		



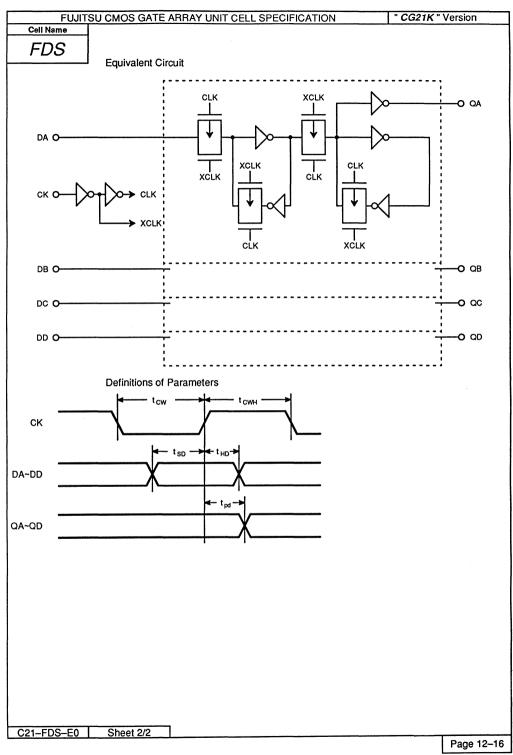
<u></u>	Cell Name	•	F	Function								Number of BC
	FDR	<b>?</b>	No	n–SC	AN 4-b	it DFF v	vith CLE	AR				26
		Cell	Symbo	ol				Proj	pagation D		eter	
						tu •••	KCL	• • •	to		CDDO	Path
						t0		t0 1.914	KCL	KCL2	CDR2	CK to Q
						1.393	0.060	1.155	0.039 0.039			CL to Q
1								100	0.003			OL 10 Q
1		DADI	BDCD	)								
			- 1 1									
		Γ''		٦							1 1	
					QA QB							
	ск —	-{			QC							
				1	QD							
1			0	J								
1			Ī									
			CL			Paramete	r	L			Symbol	Typ (ns) *
						Clock P	ulse Widt	h			tcw	2.5
1							ause Tim				t cwH	2.5
1							tup Time				t <sub>SD</sub>	0.7 1.7
						Dala no	na rime				1 HD	1.,
<b>—</b>	Di .:	Т	Ir	nput Load	ding	Clear P	ulse Widt	h	t <sub>LW</sub>	2.5		
	Pin Name	•		Factor (		Clear R	elease Ti	me	t REM	0.9		
	D			1		Clear H	old Time		t inn	2.7		
1	CK CL		į									
	OL	ı		•								
ĺ		i										
	Din Name		0	Output Dr	iving							
	Pin Name	<u> </u>		Factor (	lu)		1					
	Q			18								
Ì						* Minimu	n values fo	r the typical	operating o	ondition.		
1		İ				The val		worst case	operating o	ondition are	given by the i	maximum delay
		l				manupile						
											· · · · · · · · · · · · · · · · · · ·	<u> </u>
1	Function Ta	elde										
[		Inpu	ts		Output	l						
	CV				Q							
	СК	D		CL								
	Х	Х		L	L							
	1	L		н	L							
	1	н		н	н							
1 1	•	<u>''</u>			.,	I						
1												
L												
C	21-FDR-	-E0	S	heet 1/3	3							
												Page 12-12



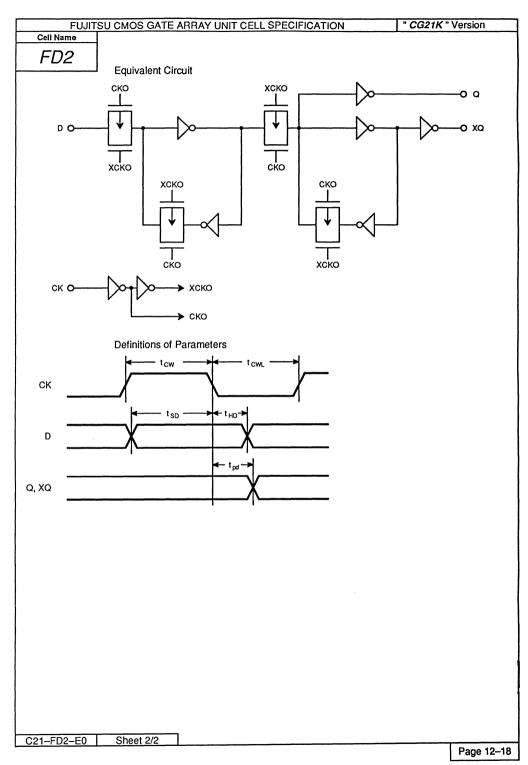


F	UJIT	SU CMOS G	J CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" V Function							
Cell Name		Function								Number o
FDS		Non-SC	AN 4-b	it DFF						20
	Cell	Symbol				Pro	pagation D		meter	
				t O	ıр KCL	t O	KCL	in KCL2	CDR2	Path
	DADI	BDCDD		1.604	0.060	1.294	0.039	NOLE	GBITE	CK to Q
СК — — — — — — — — — — — — — — — — — — —										
				Parameter					Symbol	Typ (ns) *
				Clock Pulse Width Clock Pause Time					t cw	2.5
				Clock P	ause iin	<u>e</u>			t cwn	2.5
				Data Se	tup Time				tsD	0.7
				Data Ho	ld Time				t <sub>HD</sub>	1.5
Pin Name		Input Loa Factor (	ding lu)							
D CK		2								
Pin Name		Output Dr Factor (								
Q		18		ues for the		operating o		e given by th	e maximum delay	
Function Tal	ole									
Inpu	ıts	Outputs								
ск	D	Q								
↑ ↑	L	T T								

C2.	I–FD	S-E0	Sheet 1/2



	LUITS	II CMOS G	ATF ARE	RAY LINIT	CELLS	PECIFICA	ATION		" CG211	C" Ver	rsion
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" VG Cell Name Function										Number of BC	
FD2		Non-SC	AN Pov	ver DFF							7
	Cell S	Symbol				Pro	pagation D	elay Paran	neter		
					ip			dn			Path
				0.871	KCL	t0	KCL	0.045	CDR2		K to Q
				1.347	0.032 0.032	0.911 1.234	0.023 0.017	0.045	7 7		K to XQ
				1.047	0.002	1.201	0.017	0.004	'	Ú	it to AQ
				1	'				İ		
							ł	1			
							1				
D —		c	)								
							[				
ск —	٦٩			İ			l				
	ŀ	р— х	Q	į.							
				]							
				Paramete		L	L	L	Symbol	T.	yp (ns) *
					ulse Widt	h			t <sub>CW</sub>		2.5
					ause Tim				t CWL		2.5
				Data Setup Time Data Hold Time					t <sub>SD</sub>		1.3 0.9
					na mne				( HD		0.0
Pin Name		Input Loa		1							
		Factor (	lu)								
D CK		2 1									
		•									
		Output Dr	t. da a	}							
Pin Name	•	Factor	iving (lu)	1							
Q		36 36	<u> </u>	Ĺ							
XQ	- 1	36		* Minimum values for the typical operating condition.							
				The values for the worst case operating condition are given by the maximum delay multiplier.							
				munipher.							
Function Ta	able										
Inp	outs	Out	puts								
СК	D	Q	XQ	]							
	Н	н	L	1							
	L	L	н								
			L	j							
1											
C21-FD2-	F0 T	Sheet 1/2	2 ]								
021-102-	<u> 1</u>	CCO. 17								P	age 12–17
										L	

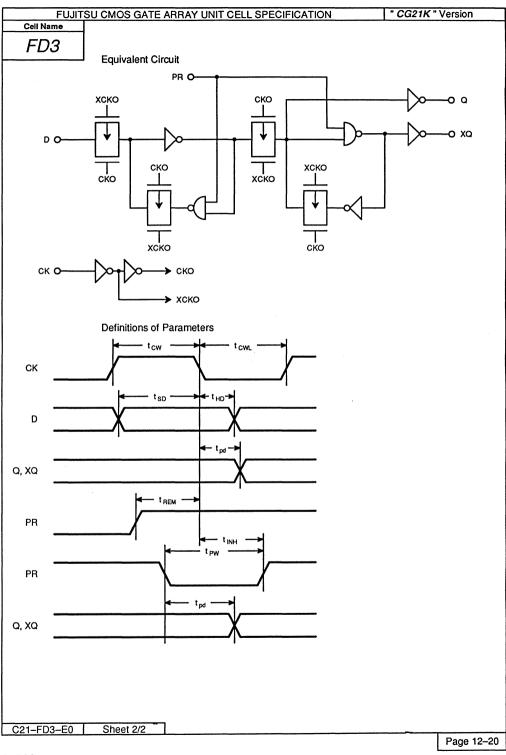


	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	K" Version
Cell Name	Function							Number of B
FD3	Non-SCAN Po	wer DFF	with Pr					8
Cel	l Symbol			Pro	pagation D	elay Parar	neter	
			ıp qı			in	,	Path
		t 0	KCL	t O	KCL	KCL2	CDR2	
D ————————————————————————————————————	PR	0.904 1.479 1.261	0.023 0.023 0.023	0.918 1.320 0.482	0.017 0.017 0.017	0.045 0.034 0.034	7 7 7	CK to Q CK to XQ PR to Q, XQ
		Parameter					Symbol	Typ (ns) *
		Clock Pulse Width					tcw	2.5 2.5
		Clock Pause Time					t CWL	2.5
		Data Setup Time					t <sub>SD</sub>	1.3
		Data Hold Time					t HD	0.9
Pin Name	Input Loading	Preset Pulse Width					t pw	2.5
	Factor (lu)		Release 7				t REM	0.3
D CK PR	2 1 2	Preset	Hold Time				t inh	2.3
Pin Name	Output Driving Factor (lu)							
Q XQ	36 36						e given by th	e maximum delay

#### Function Table

	Inputs	Outputs			
PR	ск	D	a	ΧQ	
L	х	х	Н	L	
н	↓	н	н	L	
н	↓	L	L	н	

C21-FD3-E0 Sheet 1/2



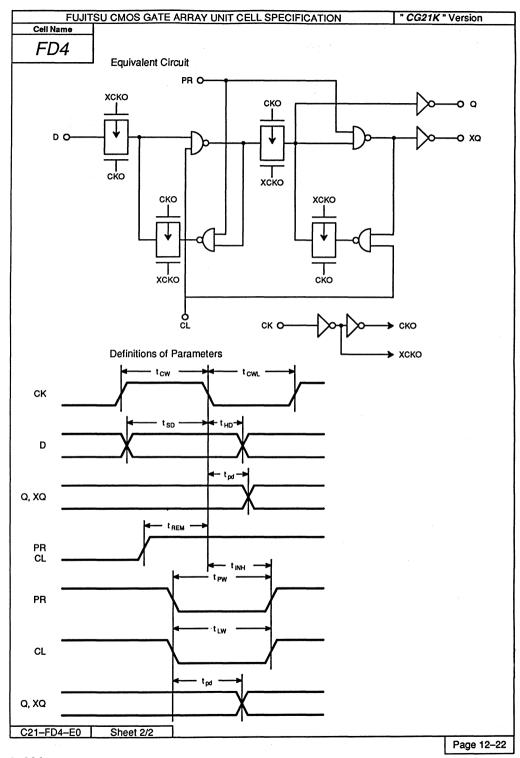
CILIET CHARLES	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version								
Cell Name	Function	TAT UNII	CELLS	PECIFICA	ATION		LUZI	^ `	Number of BC
FD4	Non-SCAN Pov	ver DFF	with Cl						9
Cell	l Symbol	Propagation Delay Parameter							
			tup tdn					-	Path
		t0	KCL	t 0	KCL	KCL2		١.,	3// 0
		1.003	0.028	0.911	0.023	0.045			CK to Q
İ		1.485	0.023 0.023	1.439 0.772	0.017 0.023	0.034		1	CK to XQ
		1.314	0.023	0.772	0.023	0.04			CL to Q, XQ
	PR	1.517	0.020	0.405	0.017	0.05-	'   '	'	PR to Q, XQ
]	1						1	1	
l	<u></u>						1		
	。								
	,				l		İ		
ск <i>-</i>		•			}		}	1	
1	b хо						ļ		
<u> </u>					İ				
•	Y	1							
	CL	Paramete			L	<u> </u>	Symbol	╀	Typ (ns) *
	CL		ulse Widt	h		<del></del>	t cw	-	2.5
			ause Tim			+	t CWL	1	2.5
ļ		Glook Fadoo Filino					LOHE	<b>†</b>	
		Data Setup Time					t <sub>SD</sub>		1.3
		Data Hold Time					t HD		0.9
Pin Name	Input Loading	Preset Pulse Width					t pw	<u> </u>	2.5
7 111 1121110	Factor (lu)	Preset Release Time					t REM		0.3
D	2	Preset Hold Time					t inh	├	2.3
CK CL	2 1 2 2	Clear	ilaa Mid	14			<b>A</b>	-	2.5
PR	2		<u>ulse Wid</u> elease Ti			-+	t LW	┼	0.6
			old Time	me		<del></del>	t REM t INH	┼	2.0
	Output Driving	Cicai i i	Old Tillio				LINM	<del>                                     </del>	
Pin Name	Factor (lu)								
a	36	1				- 1		1	
χã	36	Minimus	m values for	r the typical	operating of	ondition			
								he ma	aximum delay
		multiplier.							

### Function Table

	Inp	Out	puts		
PR	CL	ск	D	σ	ΧQ
L	Н	х	х	Н	L
н	L	×	×	L	н
н	н	↓	н	н	L
н	н	↓	L	L	н

C21-FD4-E0 Sheet 1/2

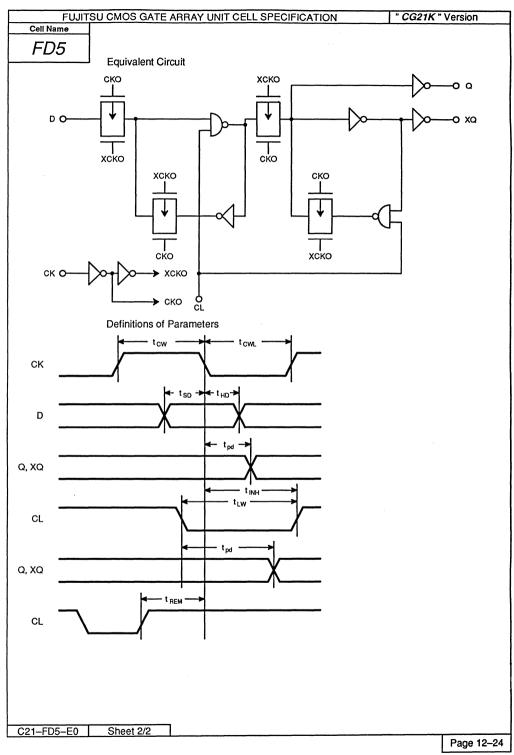
Page 12-21



FUJI	TSU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	( " Version		
Cell Name	Function							Number of BC		
FD5	Non-SCAN Pov	wer DFF	with Cl	EAR				8		
Ce	Cell Symbol			Propagation Delay Parameter						
			ιp qι			dn		Path		
		t 0	KCL	t O	KCL	KCL2				
		0.997	0.032	0.904	0.023	0.045		CK to Q		
		1.360	0.032	1.360	0.017	0.034		CK to XQ		
		1.248	0.032	0.805	0.023	0.045	5 7	CL to Q, XQ		
		Ì	<b> </b>	ĺ	1	[	1 1			
		1				1	1 1			
		ŀ			l	l	] [			
□ —	。		Ì		l		1			
0-	q	i				ĺ	1 1			
ск ——ф		ł	}			l	1 1			
	b— хо	}	1				1 1			
L										
	Ĭ	1				ì	1 1			
	CL	Paramete	L		L	۳	Symbol	Typ (ns) *		
	OL		ulse Widt	h			t cw	2.5		
			ause Tim				t cwL	2.5		
		O IO OIL I	abou imi							
		Data Se	etup Time				t <sub>SD</sub>	1.3		
		Data Hold Time					t HD	0.9		
Pin Name	Input Loading		ulse Wid				t LW	2.5		
	Factor (lu)		elease Ti	me			t REM	0.9 2.7		
D CK	2	Clear H	old Time				t inh	2.1		
CL	2	İ				1	İ			
		1					1			
		)				ļ				
Di- N	Output Driving	1				- 1	İ			
Pin Name	Factor (lu)					- 1	ł			
Q	36 36							<u> </u>		
XQ	36			r the typical						
		1		worst case	operating o	ondition a	are given by the	e maximum delay		
		multiplie	er.							
	<u> </u>	l								
Function Table										
i uncuon rable										

	Inputs	Outputs				
CL	ск	D	Q	XQ		
L	х	×	L	н		
н	1	н	н	L		
н	↓	L	L	н		

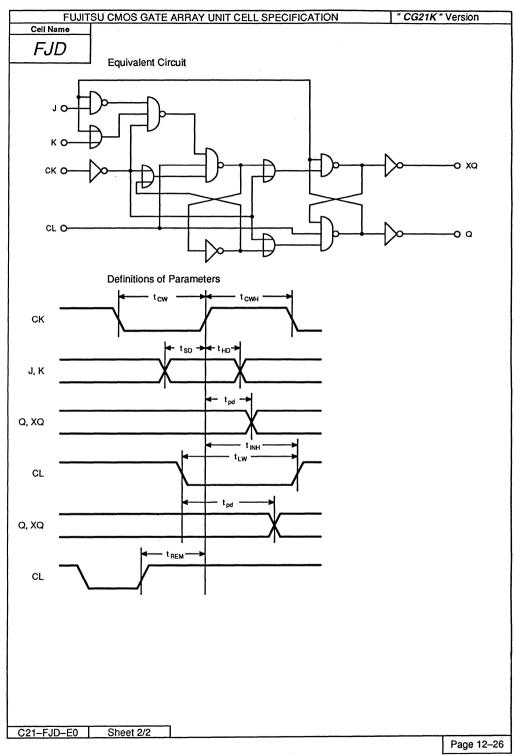
C21-FD5-E0 | Sheet 1/2



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION   " CG2	Path  CK to Q CK to XQ CL to Q, XQ						
Cell Symbol   Propagation Delay Parameter	Path  CK to Q  CK to XQ						
tup tdn  t0 KCL t0 KCL KCL2 CDR2  2.323 0.032 1.564 0.023 0.039 7  2.343 0.032 1.314 0.023 0.039 7	CK to Q CK to XQ						
t0 KCL t0 KCL KCL2 CDR2 2.323 0.032 1.564 0.023 0.039 7 2.343 0.032 1.314 0.023 0.039 7	CK to Q CK to XQ						
2.323	CK to Q CK to XQ						
1.267   0.032   0.680   0.023   0.039   7	CL to Q, XQ						
	}						
	1						
CK							
K — p— xq							
CL Parameter Symbol	Typ (ns) *						
Clock Pulse Width tow	3.3						
Clock Pause Time town	3.3						
J, K Setup Time t <sub>SD</sub>	1.5						
J, K Hold Time t <sub>HD</sub>	0.8						
Pin Name Input Loading Clear Pulse Width tuw	2.5						
Pin Name Input Loading Clear Pulse Width t <sub>LW</sub> Factor (Iu) Clear Release Time t <sub>REM</sub>	1.5						
CL 2 Clear Hold Time tinh	2.7						
l K l 1 l							
CK 1							
Oct. 4 District							
Pin Name Cutput Driving Factor (Iu)							
Q 36 XQ 36	<u> </u>						
Minimum values for the typical operating condition.	will inform values for the typical operating condition.						
multiplier.	The values for the worst case operating condition are given by the maximum delay multiplier.						
Function Table							
Inputs Outputs							
CL CK J K Q XQ							
L H X X L H							
н ↑ ∟ ∟   Q0 хQ0							
.   н ↑ ∟ н   ∟ н							

C21-FJD-E0 Sheet 1/2

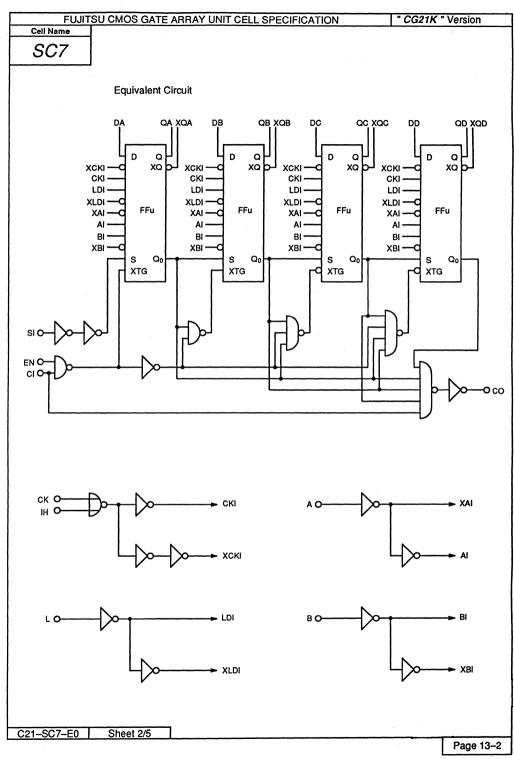
Page 12-25

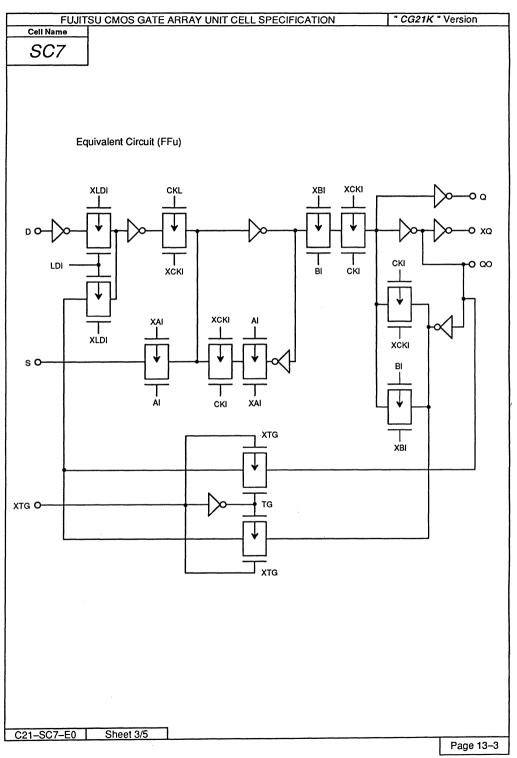


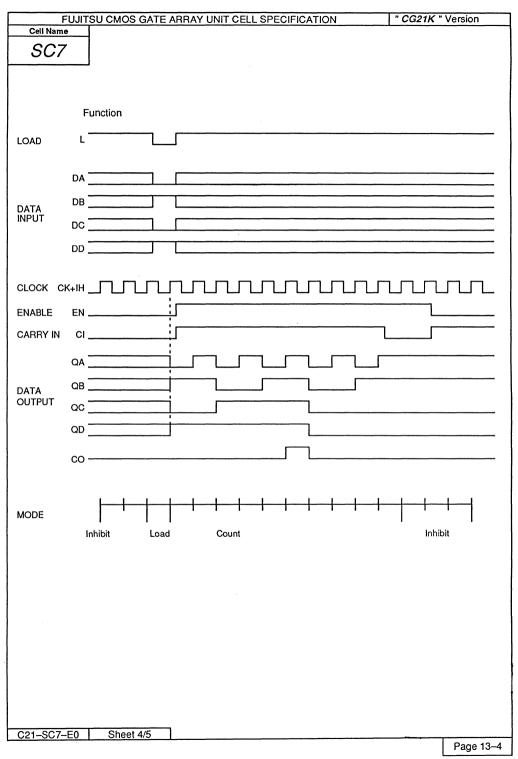
# **Scan Counter Family**

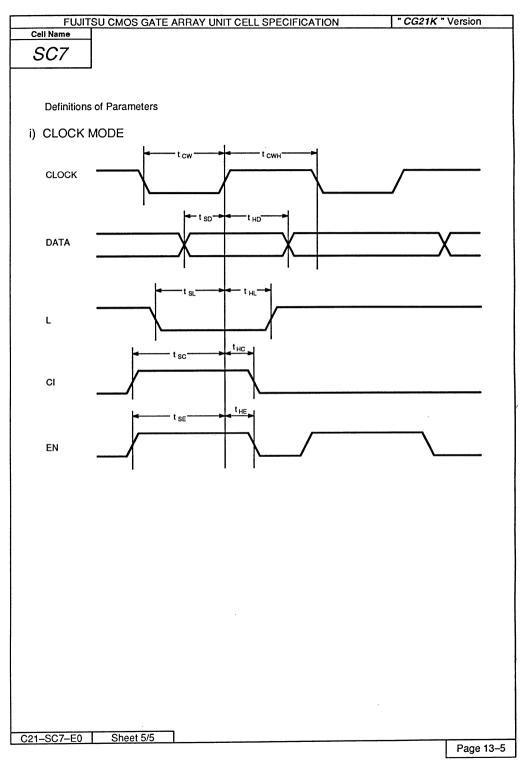
Page	Unit Cell Name	Function	Basic Cells
3–211	SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62
3–216	SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66
3–221	SC43	Scan 4-bit Synchronous Binary Up Counter with Asynchronous Clear	59
3-225	SC47	Scan 4-bit Synchronous Binary Up/down Counter	78

	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA	ATION		" CG211	K "	Version
Cell Name	Function		D'						Number of BC
SC7	SCAN 4-bit Syr Up Counter with	icnronol	i i oca is binar	у					62
	Symbol	T Tarane	LUau	Droi	pagation D	olav Dan			L
Çeli	Symbol	t	ip	F10)		in Par	ameter	Г	
		t0 KCL t0 KCL KCL2					CDR2		Path
		1.743	0.032	1.611	0.028	0.067			CK,IH to Q
		3.056	0.032	2.818	0.028	0.067	7 7		K,IH to XQ
_	<del></del>	4.119	0.032	2.766 0.053	0.017 0.017	-	-	C	K,IH to CO
DA	QA	1.056	0.032	-	1	CI to CO			
DB DC	D XQA	ł .							
DD -	QB	1					1		
ск—	о— хав — ас							ł	
н	— чс Б— хос								
"L—d	QD	Paramete	er				Symbol	$\vdash$	Typ (ns) *
CI —	þ xad		ulse Widt				t cw		4.2
EN	co	Clock P	ause Tim	ie			t cwn	<u> </u>	4.2
sı		Data Se	tup Time				t sp	├	1.2
А — d	Ì		old Time				t HD	$\vdash$	2.0
- L							- 110		
			etup Time	)	·		t st		3.7
		Load Ho	old Time			-+	t HL	⊢	2.1
	Input Loading	CI Setu	o Time			-+	t sc		4.2
Pin Name	Factor (lu)	CI Hold					t HC		1.6
D	1	ENION						<u> </u>	4.2
CK IH	1	EN Sett	p Time			-+	t se t he	-	1.6
L	1 1 2 1	LIVITOR	7 11110				· nc		<u>::</u>
CI EN	1	l							
SI	1								
A,B		4							
Pin Name	Output Driving Factor (lu)								
Q	36	1							
XQ	36 36	* Minimu	n values for	r the typical	operating of	condition			
co	30	The val	ues for the v					ne m	aximum delay
		multiplie	er.						
		<u> </u>							
C21-SC7-E0	Sheet 1/5								Page 13–1

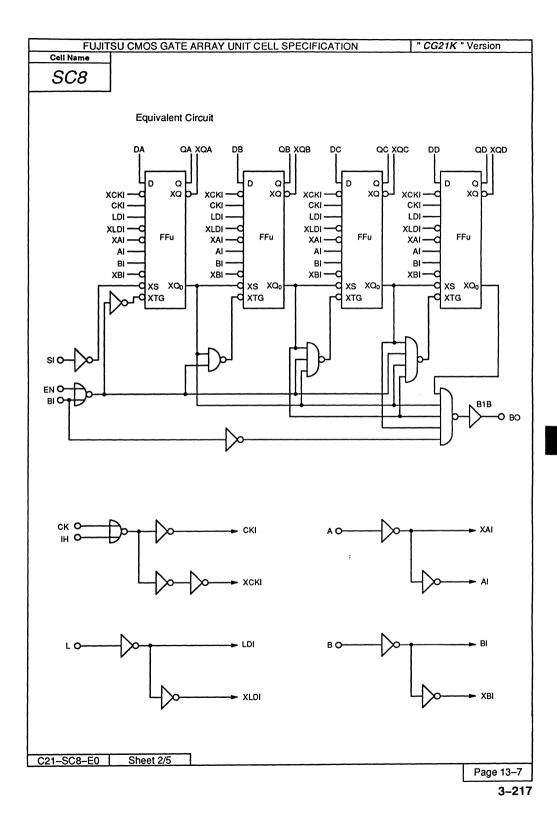


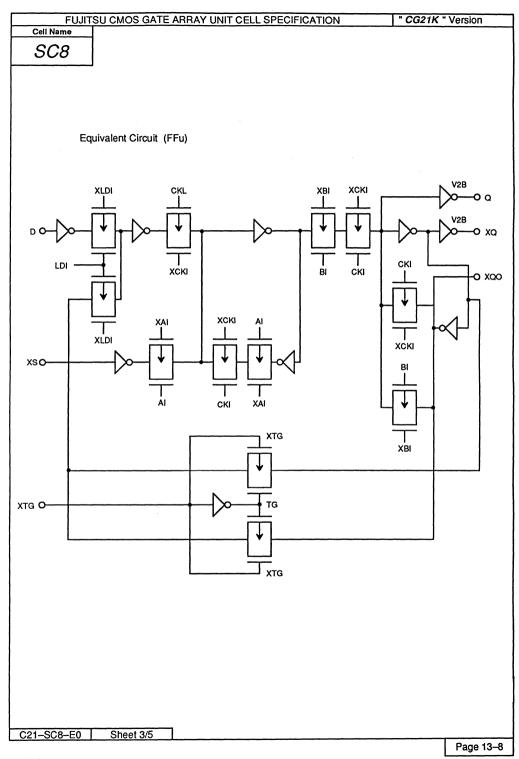


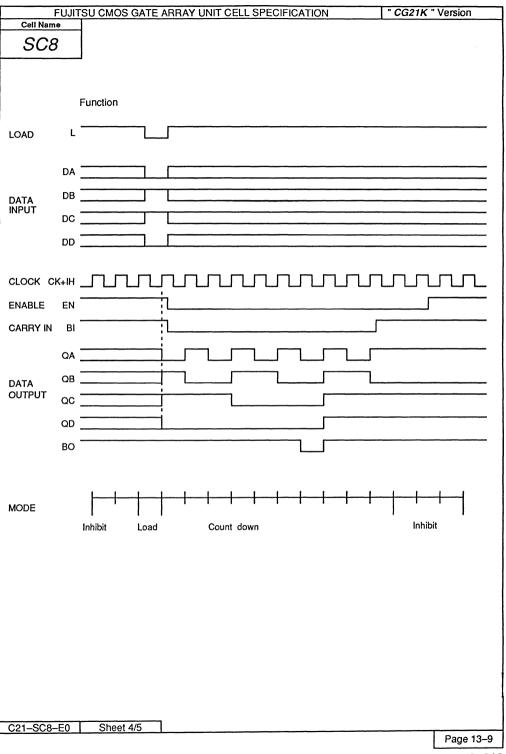


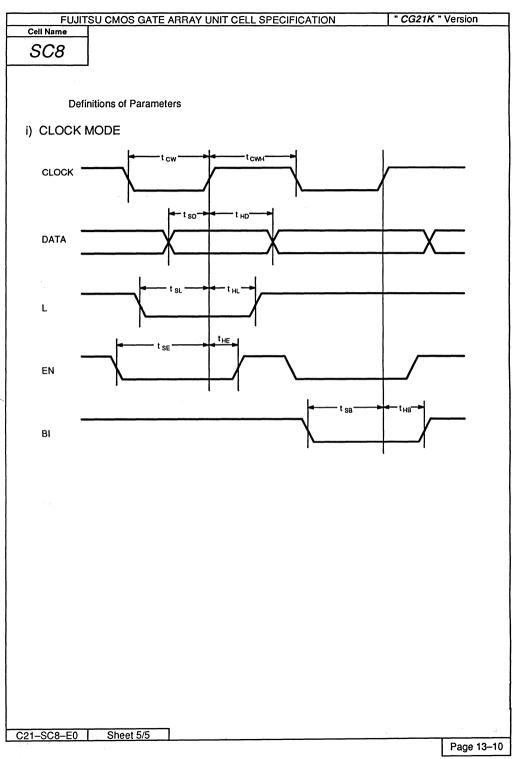


FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	K " V	ersion
Cell Name	Function		-						Number of BC
SC8	SCAN 4-bit Syn Down Counter w								66
Cel	Symbol			Pro	pagation D	elay Para	meter		
		t O	KCL	t O	KCL to	dn KCL2	CDR2		Path
DA	— QA D— XQA — QB D— XQB — QC D— XQC	1.782 2.323 3.386 0.786	0.028 0.023 0.032 0.032	1.683 2.284 4.422 1.201	0.028 0.017 0.017 0.017	0.062	7	Cł Cł	K,IH to Q K,IH to XQ K,IH to BO BI to BO
l "ï—d	QD	Paramete	r		L	<u> </u>	Symbol		Typ (ns) *
ві — а	D XQD		ulse Widt	h			tcw		4.0
EN ——q			ause Tim				t cwn		4.0
SI -	р— во								
A			tup Time				t sp		2.0
B —q_		Data Ho	old Time				t HD		2.0
		Load Se	etup Time	·			t st		3.7
			old Time				t HL		2.1
Pin Name	Input Loading Factor (lu)	EN Sett	ID Time				t se		4.8 1.1
_		EN Hold	rime				t HE		1.1
D CK	1	BI Setu	Time				t sB		4.8
IH L	1	BI Hold					t HB		1.1
BI EN SI A,B	2 1 1								
Pin Name	Output Driving Factor (lu)								
a XB	36 36 36		ues for the		operating o		re given by th	e ma	ximum delay
C21-SC8-E0	Sheet 1/5							_	Desc to o
								L	Page 13–6



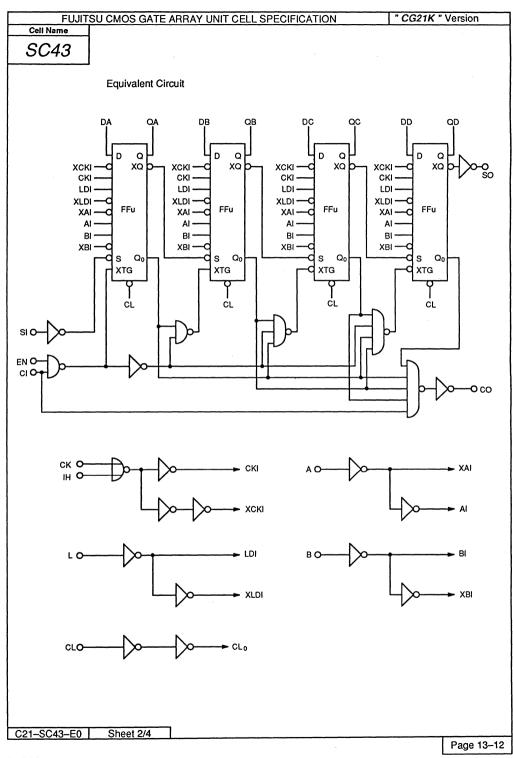


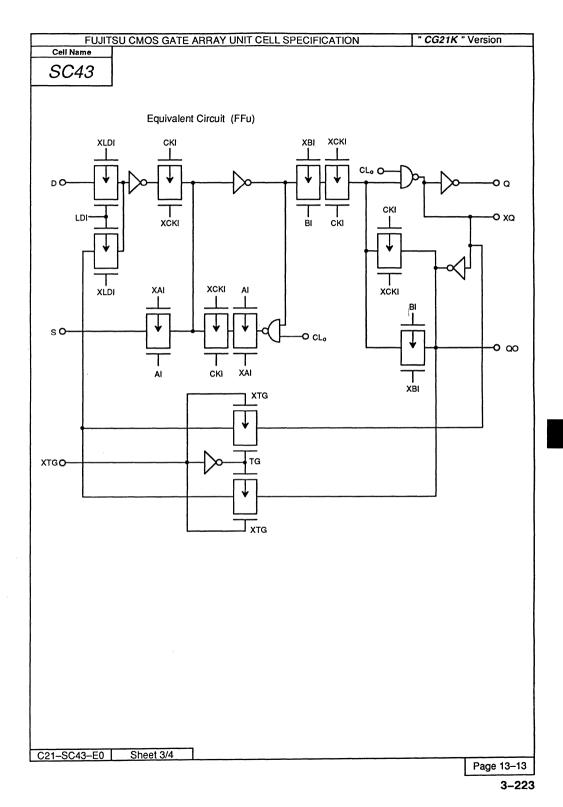


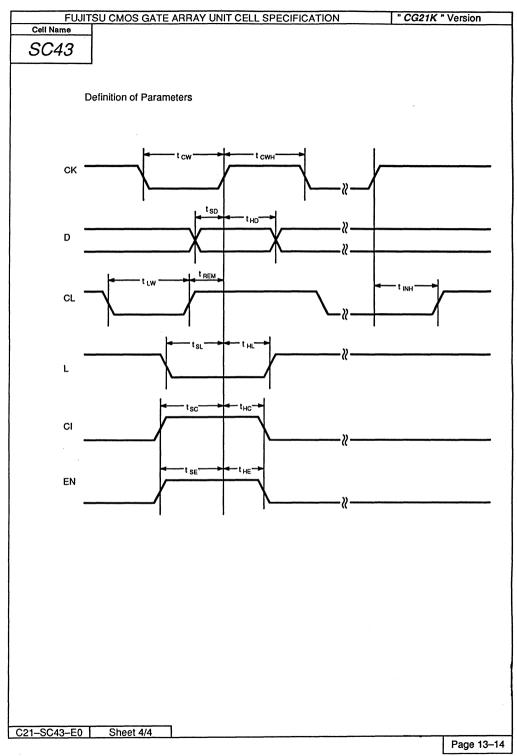


FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG211	K " Version
Cell Name	Function							Number of BC
SC43	SCAN 4-bit Syr with Asynchrono			y Up Co	ounter			59
Cel	l Symbol	Propagation Delay Param					meter	
			ıρ			in		Path
1		t0	KCL	t 0	KCL	KCL2	CDR2	
DA — DB — DC — DD — CK — CI — EN — SI — A	— QA — QB — QC — QD	2.257 2.719 - 0.964 -	0.060 0.060 - 0.060 -	2.172 2.904 1.380 0.660 1.888	0.039 0.039 0.039 0.039 0.039	0.056 0.056 0.056 0.056 0.056	4 4 4 4	CK to Q CK to CO CL to Q CI to CO CL to CO
B—d		Paramete	L			L	Symbol	Typ (ns) *
L	<del></del>		ulse Widt	h			tcw	3.0
			ause Tim		~		t cwH	4.3
	CL		tup Time				t <sub>SD</sub>	1.2
		Data Ho	old Time				t HD	1.3
		Load Se	etup Time				t <sub>SL</sub>	1.8
	· · · · · · · · · · · · · · · · · · ·		old Time				t <sub>HL</sub>	1.5
,	Input Loading	CI Setu				_	tsc	2.4
Pin Name	Factor (lu)	CI Hold					t HC	1.1
D CK, IH	2	EN Setu EN Hold					t se t HE	2.4 1.1
L, CL, SI	l i		ulse Widt	h			tıw	3.7
EN	1 2	Clear R	0.9					
A, B, CI	2	Clear H	3.4					
Pin Name	Output Driving Factor (lu)						t INH	
Q CO SO	18 18 18	* Minimur The valu multiplie	e maximum delay					

C21-SC43-E0 | Sheet 1/4





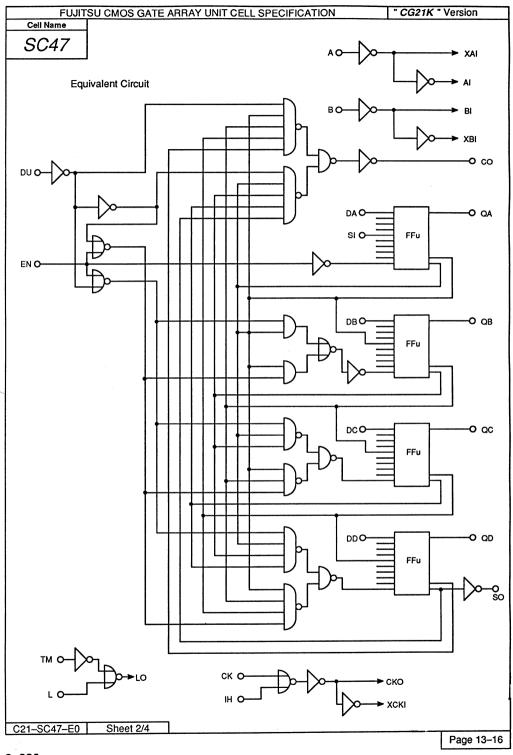


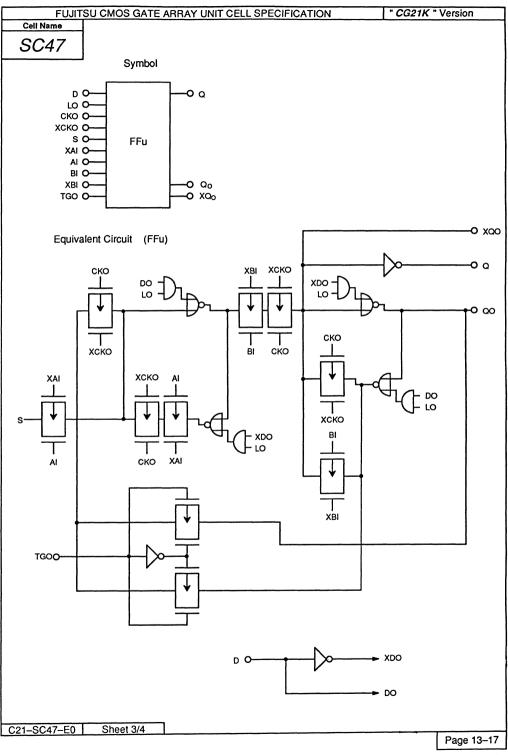
FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
SC47	SCAN 4-bit Syn	chronou	us Binar	y Up/Do	own Cou	unter		78
Cell	Symbol			Pro	pagation D	elay Paran	neter	
			Jp			dn		Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	
DA ————————————————————————————————————	——— QA ——— QB ———— QC ———— QD	2.376 3.234 1.241	0.060 0.060 0.060	2.482 4.594 1.551	0.084 0.039 0.039	0.112	4	CK to Q CK to CO DU to CO
CK IH C	> co so	Paramete					Symbol	Typ (ns) *
A			ulse Widt	h (H)			tow	3.0
			ause Tim				t cwH	4.3
		Data Se	tup Time				t <sub>SD</sub>	1.2
			old Time	t <sub>HD</sub>	1.3			
		EN Setu	Ip Time		t sE	2.4		
	Input Loading		it Setup 7	ime	t HE	1.1 1.1		
Pin Name	Factor (lu)	DU Inpu	t Hold Ti	me			t <sub>HU</sub>	2.4
D	2 1	Load Pu	ılse Widtl	t <sub>LW</sub>	3.7			
CK, IH, TM, L	1		<u>elease Ti</u>	me		t REM	0.9	
EN DU, A, B	3 1	Clear H	old Time				t INH	3.4
Si	2						Ì	
Pin Name	Output Driving Factor (lu)							
Q	18							
so co	18 18						given by the	maximum delay

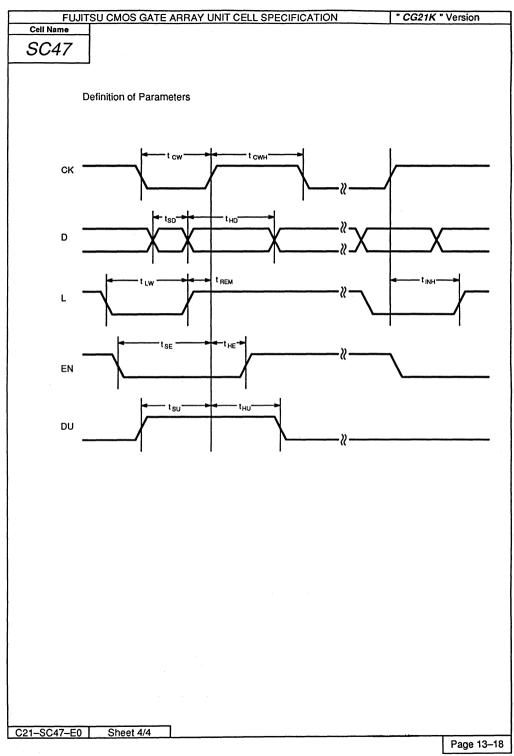
C21-SC47-E0

Sheet 1/4

Page 13-15







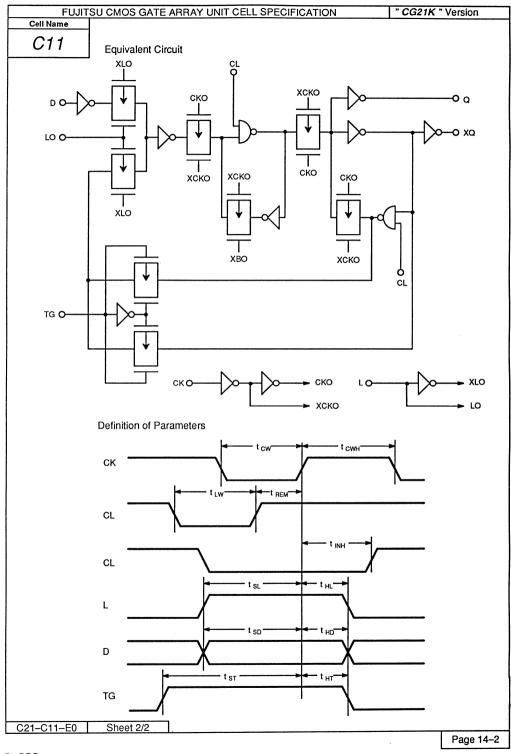
# **Non-Scan Counter Family**

Page	Unit Cell Name	Function	Basic Cells
3-231	C11	Non-Scan Flip-Flop for Counter	11
3-233	C41	Non-Scan 4-bit Binary Asynchronous Counter	24
3-236	C42	Non-Scan 4-bit Binary Synchronous Counter	32
3-239	C43	Non-Scan 4-bit Binary Synchronous Up Counter	48
3-243	C45	Non-Scan 4-bit Binary Synchronous Up Counter	48
3-247	C47	Non-Scan 4-bit Binary Synchronous Up/Down Counter	68

FUJI	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFICA	ATION		" CG21F	( " Version
Cell Name	Function							Number of BO
C11	Non-SCAN Flip	Flop fo	r Count	er				11
Ce	I Symbol	T		Pro	pagation D	elay Paran	neter	······································
		tı	ıþ			in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	raui
D	— a >— ха	1.003 1.340 1.386	0.060 0.060 0.060	0.924 1.571 0.918	0.045 0.045 0.045			CK to Q CK to XQ CL to Q,XQ
L	CL	Parameter Symb Clock Pulse Width tow Clock Pause Time town						Typ (ns) * 2.5 2.5
		Cloar P	ulse Widt	h			t <sub>LW</sub>	2.5
			elease Ti				t REM	0.6
			old Time	1110			t INH	0.3
Pin Name	Input Loading							
i ili Mallie	Factor (lu)		etup Time		CK)		t <sub>SL</sub>	1.4
L		Load Ho	old Time	(	CK)		t HL	0.3
ΤĠ	2 2 2	D-4- C-	ton Time a		(014)			1.5
CL	2		etup Time		CK)		t <sub>SD</sub>	0.3
D,CK	1	Data no	na rime		UN)		t HD	0.3
	Output Driving	TG Setu	ın Time	1	CK)		t <sub>ST</sub>	1.8
Pin Name	Factor (lu)	TG Hold			CK)		tHT	0.0
Q XQ	18 18	* Minimu	m values for		l operating o			e maximum delay

-	L	D	TG	CL	СК	Q (Q <sub>0</sub> )
	х	х	х	L	х	L
i	Н	Н	Х	Н	1	Н
	Н	L	Х	Н	1	L
	L	Х	L	Н	1	Q (Q <sub>0</sub> )
	L	Х	Н	Н	1	Q (Q <sub>0</sub> )
						1

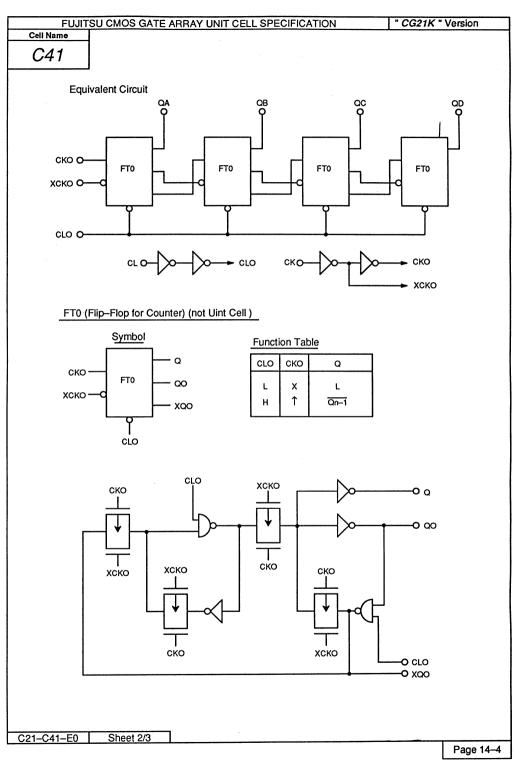
C2.	1-C11	-E0	Sheet	1/2_



	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFIC	ATION		" CG211	K " Version
Cell Name	Function							Number of BC
C41	Non-SCAN 4-	oit Binary	Asyncl	hronous	Counte	er		24
Cell	Symbol			Pro	pagation D	elay Paran	neter	
		tup tdn						Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		1.056	0.051	0.984	0.045	-	- 1	CK to QA
		1.941	0.051	1.736	0.045	-	- 1	CK to QB
<del></del>	2.713	0.051	2.508	0.045	-	-	CK to QC	
	3.485	0.051	3.274	0.045	-	-	CK to QD	
1	ав	-	-	2.211	0.045	-	- 1	CL to Q
ì	<u></u> − ac					ŀ		
l l	QD							
ск								
i		1		İ				
L	<del>p                                    </del>			<u> </u>		L		
		Paramete				Symbol	Typ (ns) *	
	CL	Clock Pulse Width					t cw t cwh	2.5
		Clock P	Clock Pause Time					2.5
		Class D	ula a NA/: alk	<u> </u>				2.5
			ulse Widt elease Ti				t LW	1.3
			old Time	me			t INH	4.0
	Input Loading	Clear	old Tillle				INH	4.0
Pin Name	Factor (lu)							
		┪						
ск	1							
CL	1	1						
		ł						
		1						
	Output Driving	1						
Pin Name	Factor (lu)							
		1						
a	18	* Minimu	m values for	r the typical	operating of	condition		
							aiven by th	e maximum delay
1		multiplie					. g y u	
		1 '						

Inp	uts	Output
CL	СК	a
Н	1	Count up
L	X	L

C21-C41-E0 | Sheet 1/3



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K" Version

Cell Name

C41

Definition of Parameters

CK

CK

CL

TRIM

TREM

CL

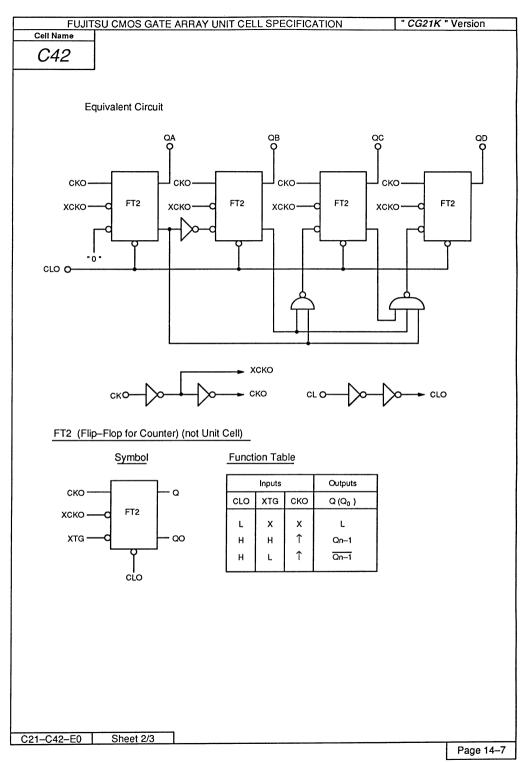
C21-C41-E0 Sheet 3/3

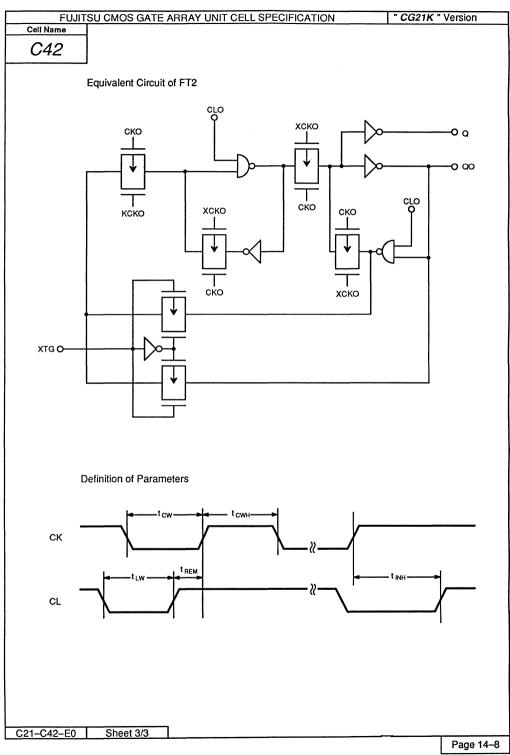
Page 14-5

F	UJITS	SU CMOS GATE	ARR	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	K " V	ersion
Cell Name		Function									Number of BC
C42		Non-SCAN	4–bi	t Binary	/ Synch	ronous	Counter	•			32
	Cell	Symbol		Propagation Delay Parameter							
					ip			in Kolo	1 0000	l	Path
				1.683 -	0.051 -	1.234 1.776	0.039 0.039	0.056 0.056	3 4		K to Q L to Q
ск—	— QA — QB — QC — QD										
	,	Y	Ì	Paramete	er	L		<u> </u>	Symbol	<del></del>	Typ (ns) *
		1	l	Clock P	ulse Wid	h			t cw		2.5
	,	CL		Clock P	ause Tim	ne			t cwn		2.5
			}	Ole el D		11.				ļ	0.5
			ŀ	Clock P	ulse Wid elease Ti	in			t LW		1.3
			}	Clear H	old Time	me			t REM t INH	4.0	
Pin Name		Input Loading Factor (lu)								•	
CK		1									
Pin Name		Output Driving Factor (lu)									
Q		18		Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						imum delay	
Function	n Tal	ble									
Inpu	uts	Outputs									
CL	СК	Q									
Н	1	Count up									
	X	L									

Page 14-6

C21-C42-E0 Sheet 1/3





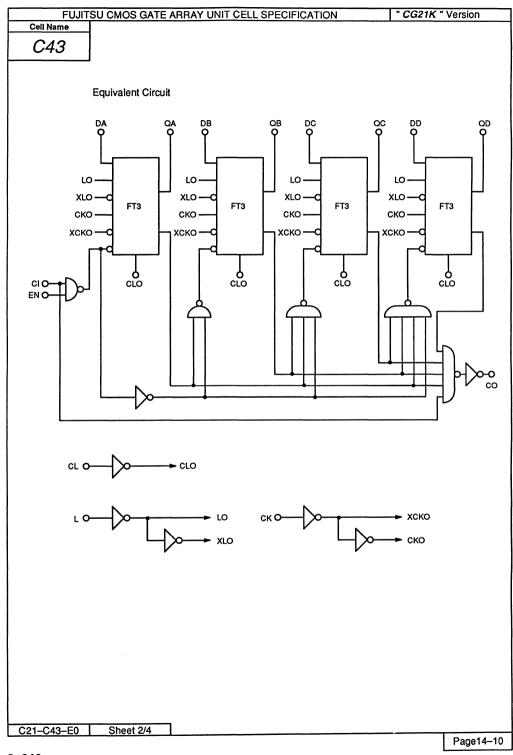
	SU CMOS GATE AR	U CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K"								
Cell Name	Function	unction								
C43	Non-SCAN 4-	bit Binar	y Synch	ronous	Up Cou	nter		48		
Cel	Symbol			Pro	pagation D	elay Paran	neter			
		tup tdn						D-4		
		t 0	KCL	t 0	KCL	KCL2	CDR2	Path		
DA — DB — DC — DD — C — C K — EN — CI		1.564 2.957 0.845 —	0.060 0.060 0.060 - -	1.267 1.881 0.429 2.053 1.393	0.039 0.039 0.039 0.039 0.039			CK to Q CK to CO CI to CO CL to Q CL to CO		
		Paramete					Symbol	Typ (ns) *		
	CL	Clock Pulse Width					t <sub>CW</sub>	2.5		
			ause Tim				t cwn	4.0		
			etup Time				t <sub>SD</sub>	1.6		
			old Time				t HD	1.8		
			etup Time	<u> </u>			t <sub>SL</sub>	2.7		
			old Time				t HL	0.8		
Pin Name	Input Loading	CI Setu					t sc	2.6		
	Factor (lu)	CI Hold					t HC	0.6		
D	4	EN Setu					t se	2.6		
L,EN	1	EN Hold					t HE	0.6		
CK,CL	1		<u>ulse Widt</u>				t <sub>LW</sub>	3.3		
CI	2		<u>elease Ti</u>	me			t REM	1.2		
		Clear H	old Time				t inn	4.9		
Pin Name	Output Driving Factor (lu)	-								
Q CO	18 18						e given by th	e maximum delay		

		Outputs				
CL	L	D	EN	CI	СК	Q
L	Х	х	х	Х	х	L
н	L	Н	х	Х	1	н
Н	L	L	X	Х	1	L
н	Н	Х	Х	L	Х	No Counting
н	Н	Х	L	Х	Х	No Counting
Н	Н	х	Ή	Н	1	Count up

Note: The CO output produces a high level output data when the counter overflows.

C21-C43-E0	Sheet 1/4
------------	-----------

Page14-9

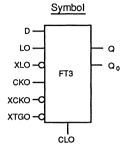


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version

Cell Name

C43

FT3 (Flip-Flop for Counter) (not Unit Cell)

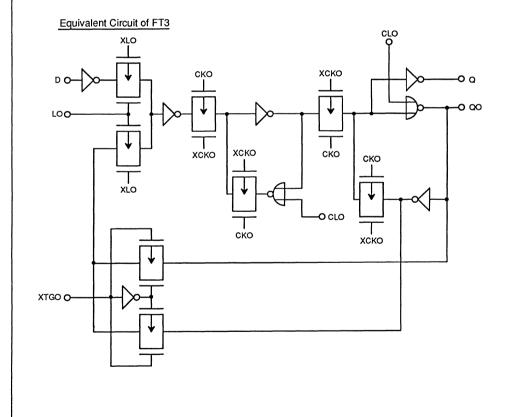


Sheet 3/4

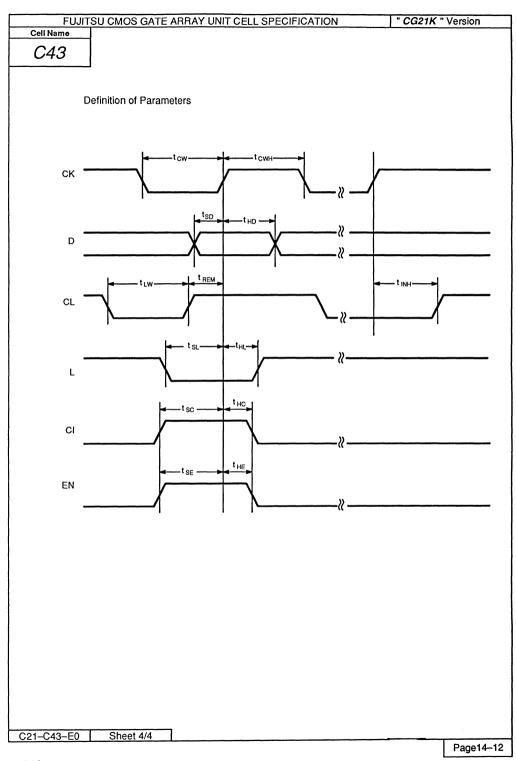
C21-C43-E0

Function Table

LO	D	XTGO	CLO	ск	Q (QO)
×	х	х	н	х	L
н	н	х	L	1	н
н	L	х	L	1	L
L	х	н	L	1	Q (QO)
L	х	L	L	1	Q (QO)



Page14-11

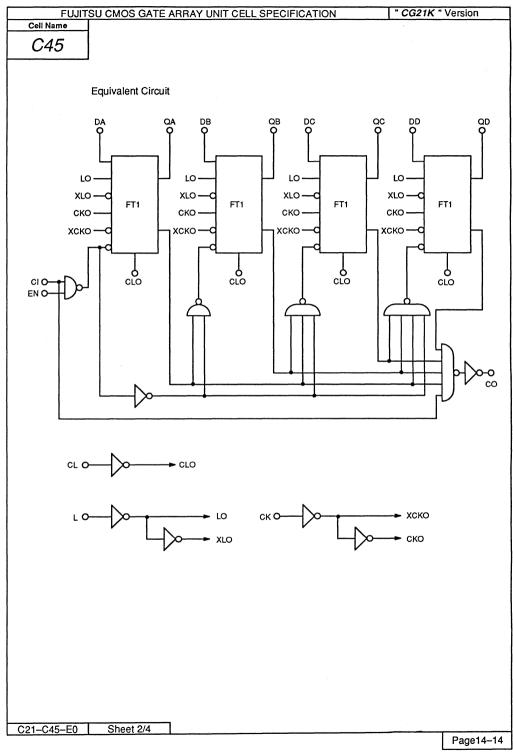


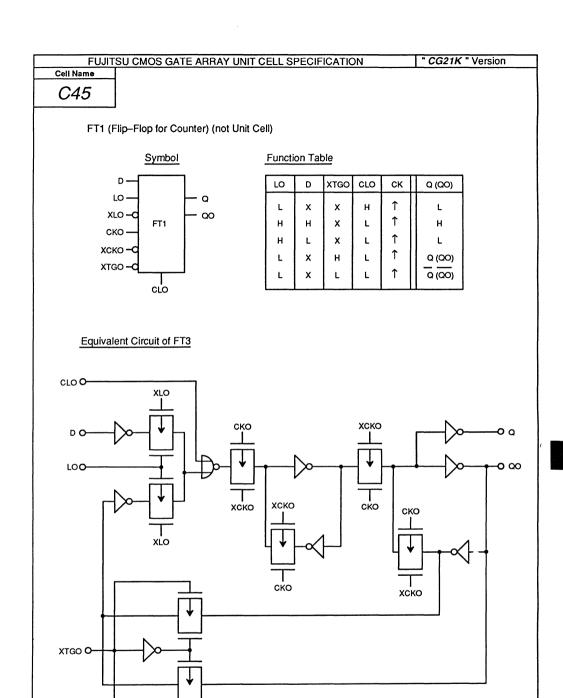
FUJIT	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K"					( " Version		
Cell Name	Function					Number of BC		
C45	Non-SCAN 4-bit Binary Synchronous Up Counter						48	
Cel		Propagation Delay Parameter						
		tup tdn						Path
		t 0	KCL	t O	KCL	KCL2	CDR2	
DA — QA DB — QB DC — QC DD — QD L — C CK — EN — CO		1.413 2.680 1.010	0.051 0.064 0.064	0.990 1.492 0.720	0.039 0.039 0.039	0.062	4	CK to Q CK to CO CI to CO
	CL			Parameter				Typ (ns) *
				Clock Pulse Width				2.5
92		Clock Pause Time					t cw	2.5
		Data Setup Time					t <sub>SD</sub>	2.3
		Data Hold Time					t <sub>HD</sub>	1.3
		Load Setup Time					t <sub>SL</sub>	2.9
			Load Hold Time					1.3
Pin Name	Input Loading	CI Setup Time					t sc	3.9
	Factor (lu)	CI Hold Time					t HC	1.2
l D	1	EN Setup Time					t se	3.9
L,EN	1 1	EN Hold Time					t HE	1.2
CK,CL							tsa	2.3
CI	2	Clear H	old Time				t HR	1.2
Pin Name	Output Driving Factor (lu)	- -						
co	18 18	<ul> <li>Minimum values for the typical operating condition.</li> <li>The values for the worst case operating condition are given by the maximum delay multiplier.</li> </ul>					e maximum delay	

		Outputs				
CL	L	D	EN	CI	СК	Q
L	х	х	Х	х	1	L
Н	L	н	Х	Х	1	Н
Н	L	L	Х	х	1	L
н	н	х	Х	L	Х	No Counting
Н	Н	Х	L	Х	Х	No Counting
Н	Н	Х	Н	Н	1	Count up

Note: The CO output produces a high level output data when the counter overflows.

C21-C45-E0	Sheet 1/4
UZ 1-U43-EU	311661 1/4

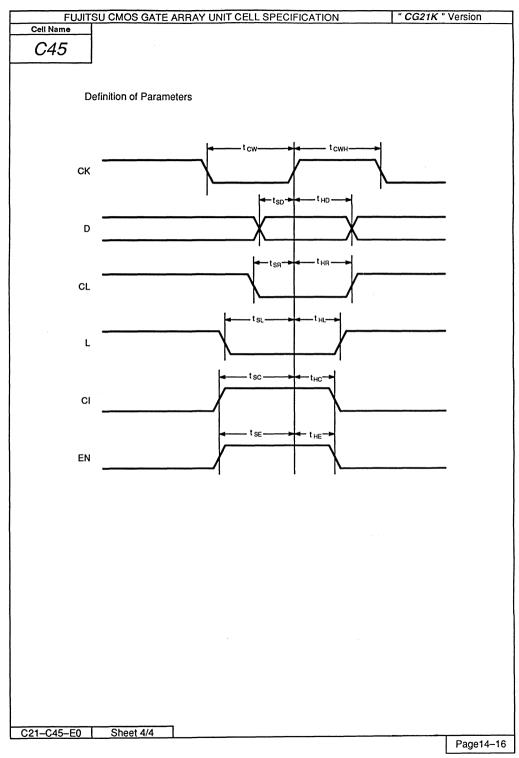




C21-C45-E0

Sheet 3/4

Page14-15 3-245



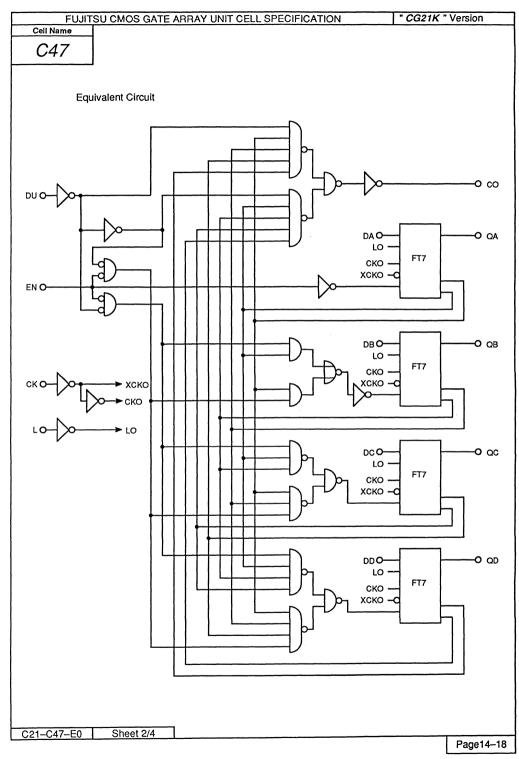
	SU CMOS GATE AF	RAY UNIT	CELLS	PECIFICA	ATION		" CG211	K " Version	
Cell Name	Function							Number of	
C47	Non-SCAN 4-	bit Binary	/ Synch	ronous	Up/Dow	n Cou	unter	68	
Cel	l Symbol			Pro	pagation D	elay Para	meter		
			tup tdn					Path	
		10	KCL	t O	KCL	KCL2	CDR2		
		2.106	0.060	1.894	0.073	0.112	. 4	CK to Q	
_		2.858	0.041	3.234	0.039			CK to CO	
DA	QA	2.647	0.060	2.924	0.073	0.112	4	L to Q	
DB——	ов	1.307	0.041	1.591	0.039			DU to CO	
DC-	ac	1							
DD	QD						1		
ر—q									
ск	ł						1		
ENq	h								
DU	p co								
_									
		Paramete				_	Symbol t <sub>CW</sub>	Typ (ns) *	
			Clock Pulse Width					3.3	
		Clock P	Clock Pause Time					5.3	
		Data Se	tup Time			—— <del>[</del>	t <sub>SD</sub>	0.5	
		Data Ho					t HD	1.1	
		- Julia III							
Pin Name	Input Loading	DU Setu					t su	3.2	
Pin Name	Factor (lu)	DU Hold	d Time				t HU	0.5	
Þ	1	EN Setu	ın Tima				t <sub>SE</sub>	2.9	
L DU	2	EN Hold				-+	t HE	0.8	
CK	1 1	2.47101	, , ,,,,,,					U.U	
EN	3	Load Re	elease Tir	ne			t REM	1.4	
Pin Name	Output Driving	Load Ho	old Time				t inn	6.5	
	Factor (lu)	<del> </del>							
a	18		ılse Widtl			L	t LW	2.5	
co	18	The val	Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the maximum delay multiplier.						

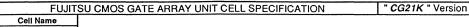
1			Inputs			Outputs
	Q	L	EN	DU	СК	Q
	Н	L	х	х	х	Н
	L	L	х	х	Х	L .
	Х	Н	Н	Х	1	No Counting
	Х	н	L	L	1	Count Up
	X	Н	L	Н	1	Count Down

Note: The CO output produces a low level output pulse when the counter overflows or underflows.

C21-C47-E0	Sheet 1/4

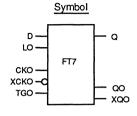
Page14-17





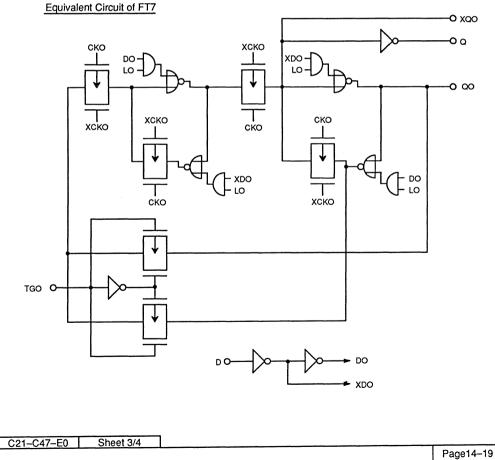
C47

FT7 (Flip-Flop for Counter) (not Unit Cell)

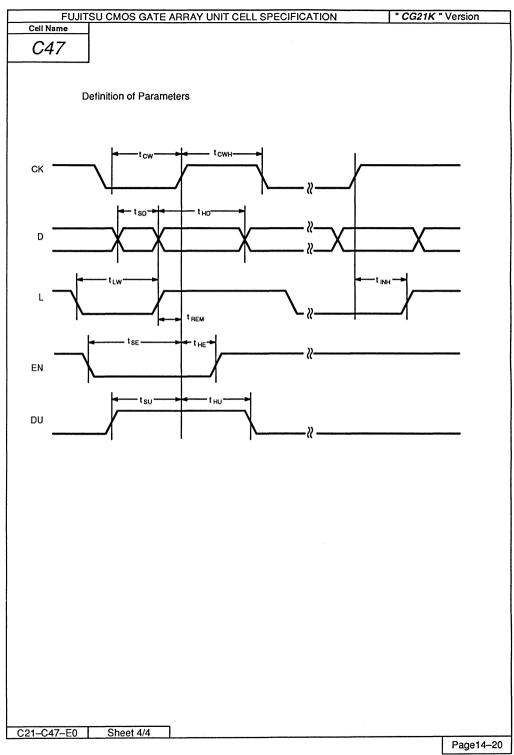


Function Table

	In	puts		Outputs			
LO	D	TGO	ско	QO(Q)	<u>a</u> (ao)		
н	н	х	х	н	L		
н	L	х	х	L	н		
L	х	L	1	Qn-1	Qn-1		
L.	х	Н	1	Qn-1	Qn-1		



\_\_\_\_\_



# **Adder and ALU Family**

	Unit Cell		Basic
Page	Name	Function	Cells
3–253	A1A	1-bit Half Adder	5
3-254	A1N	1-bit Full Adder	8
3–255	A2N	2-bit Full Adder	16
3-257	A4H	4-bit Binary Full Adder with Fast Carry	48

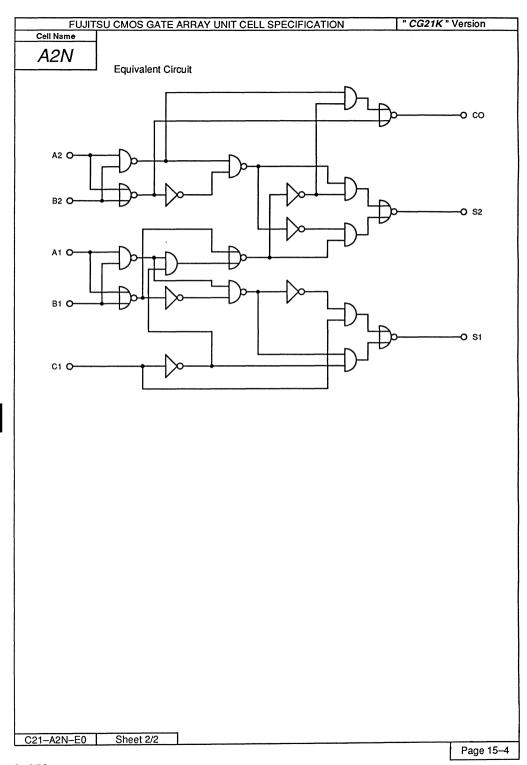
FILE	ITSII	CMOS G	ATE ARE	TIMI I VAS	CELLS	PECIFIC	MOLTA		" CG21K	" Version
Cell Name	1130	Function	AIE ARF	MI UNII	VELL S	EUIFIU	ATION		CGZIK	Number of BC
A1A	1	1-bit Hal	f Adder	•						5
C	ell Syı	mbol				Pro	pagation D		eter	
				t O	KCL	t O	KCL	In KCL2	CDR2	Path
В ——				0.647 0.574 0.594 0.673	0.032 0.032 0.032 0.032	0.759 0.772 0.660 0.607	0.017 0.017 0.017 0.017	ROLZ	CONZ	A to S B to S A to CO B to CO
'										
				Paramete	<u> </u>	L	L	L	Symbol	Typ (ns) *
	<del></del>		T.							
Pin Name		Input Load Factor (I	iing u)							
A B		2								
Pin Name		Output Dri Factor (								
CO S		36 36		* Minimu The val multiplie	ues for the	r the typical worst case	operating o	condition. ondition are	given by the	maximum delay
Function Table						Equivalent	Circuit			
A	В	со	s					-P	Α.	
L	L	L	L		-			7	$\sim$	)—— S
L	Н	L	н							
Н	L	L	н				14	b—	\_	со
н	Н	н	Ł							
C21-A1A-E0	T	Sheet 1/1								I possess
										Page 15-1

FILID	SU CMOS G	ATE ARE	RAY LINIT	CELLS	PECIFIC	ATION		" CG21K	" Version
Cell Name	Function	ATE AIN	1711 01111	OLLE O	LOILIO	THOIT			Number of BC
A1N	1-bit Ful	l Adder							8
Cel	i Symbol				Pro	pagation D		eter	
			10	IP KCL	t O	KCL	n KCL2	CDR2	Path
B					1.663 0.713 1.261 0.621	0.039 0.039 0.039 0.039			A, B to S CI to S A, B to CO CI to CO
	ĊI		Paramete	er	L		٠	Symbol	Typ (ns) *
Pin Name A B CI	A 3 B 3								
Pin Name	Output Dr Factor (								
co s	18 18		Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
Function Table					Equivalent	Circuit			
Inp	uts	Out	puts	_	- 1	$\mathbb{H}$		1 1	•
A E	3 CI	S	со	E	' <b>    †</b>		<del>-11</del>	~~\ V	s
L	L	L	L	С	, 44		↓		
) н і	. L	н	L			1			
		Н	L				-1		
Н н		L	н			L	一小	7سم	<u></u> co
		н	L				—\ф	ィーヤ	,
		L	н		L		-U		
		L	н						
		Н	н						
C21-A1N-E0	Sheet 1/	1 7		•					
									Page 15-2

FUJIT	SU CMOS GATE AR	<u>RAY UNIT</u>	CELL S	PECIFIC/	AHON		" CG211	(" Version
Cell Name	Function							Number of E
A2N	2-bit Full Adde	r						16
Cel	l Symbol		Propagation Delay Paran					
			tup tdn					Path
		t O	KCL	t O	KCL	KCL2	CDR2	1 401
	1.505	0.106	1.485	0.062	_		A1 to CO	
		1.446	0.106	1.518	0.062	-		B1 to CO
		0.838	0.106	0.720	0.039	0.056	4	A2 to CO
	0.779	0.106	0.720	0.039	0.056	4	B2 to CO	
	1.472	0.106	1.366	0.062	_		CI to CO	
B2 ——	1.571	0.083	1.452	0.062	_		A1 to S1	
A2		1.571	0.083	1.452	0.062	_	Í I	B1 to S1
B1	S2	0.627	0.083	0.627	0.062	_		CI to S1
A1	1.492	0.083	1.452	0.062	-		A1 to S2	
L	1.644	0.083	1.558	0.062	_	1	A2 to S2	
	1.432	0.083	1.485	0.062	_		B1 to S2	
	CI	1.644	0.083	1.558	0.062			B2 to S2
	OI	1.459	0.083	1.333	0.062	-		CI to S2
		Paramete	Parameter				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A, B	2 2	1				1		
ĊI	2	1				1		
		1						
						-		
	Output Driving	$\exists$				- 1		
Pin Name	Factor (lu)							
S	14	1				ļ		
co	14						given by th	e maximum delay

		Inputs				Ou	tputs		
		inputs			CI = L			CI = H	
Α	1 B1	A2	B2	S1	S2	CO	S1	S2	co
L	. L	L	L	L	L	L	Н	L	L
H	l L	L	L	Н	L	L	L	Н	L
L	. н	L	L	Н	L	L	L	Н	L
H	І Н	L	L	L	н	L	Н	Н	L
L	. L	Н	L	L	Н	L	Н	Н	L
H	l L	Н	L	н	Н	L	L	L	Н
L	. н	Н	L	н	н	L	L	L	Н
H	н н	Н	L	L	L	Н	Н	L	Н
L	. L	L	Н	L	Н	L	н	Н	L
l H	L	L	н	н	Н	L	L	L	Н
L	. н	L	Н	Н	Н	L	L	L	Н
[ н	Н	L	Н	L	L	Н	Н	L	Н
L	. L	Н	Н	L	L	Н	н	L	Н
<b>!</b> н	L	н	н	н	L	Н	L	Н	Н
1 6	Н	Н	н	н	L	Н	L	Н	Н
Н	н	Н	Н	L	Н	Н	Н	H	Н

C21-A2N-E0	Sheet 1/2



FUJI Cell Name	SU CMOS GATE ARI	RAY UNIT	CELL S	PECIFIC	ATION		" CG211	( " Version Number of BC
A4H	4-bit Binary Ful	l Adder	with Fas	st Carry				48
Ce	I Symbol	T		Pro	pagation D	elay Param	neter	
			tup tdn				Path	
		t O	KCL	t O	KCL	KCL2	CDR2	
B4 ————————————————————————————————————	CO S4 S3 S2 S1	0.627 1.399 1.604 1.657 1.518 2.013 1.677 1.809 1.980 1.743	0.083 0.106 0.106 0.106 0.060 0.083 0.106 0.106 0.106 0.060	0.865 1.624 1.578 1.868 1.696 1.789 1.630 2.033 2.073 2.070	0.062 0.062 0.062 0.062 0.039 0.062 0.062 0.062 0.062 0.063			CI to S1 CI to S2 CI to S3 CI to S4 CI to CO A1, B1 to S1 A1, B1 to S2 A1, B1 to S3 A1, B1 to S4 A1, B1 to CO
	CI	1.630 1.934 1.974 2.046	0.106 0.106 0.106 0.060	1.782 1.901 2.139 2.026	0.062 0.062 0.062 0.039			A2, B2 to S2 A2, B2 to S3 A2, B2 to S4 A2, B2 to CO
Pin Name	Input Loading Factor (lu)	1.485 2.026 2.007	0.106 0.106 0.060	1.505 2.132 2.020	0.062 0.062 0.039			A3, B3 to S3 A3, B3 to S4 A3, B3 to CO
B CI	2 2 2	1.531 1.934	0.083 0.060	1.591 1.855	0.039 0.039	0.056	4	A4, B4 to S4 A4, B4 to CO
Pin Name								
CO S1, S3, S4 S2	18 14 18							

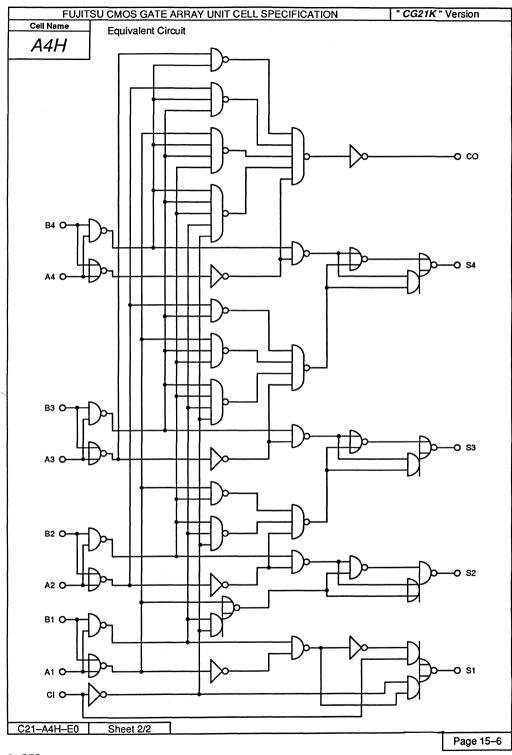
-					Outputs						
		Inp	uts			CI = L			CI = H		
- 1						C2 = L		C2 = H			
-	A1	B1	A2	B2	S1	S2	C2	S1	S2	C2	
- 1	А3	В3	A4	B4	S3	S4	co	S3	S4	co	
ı	L	L	L	L	L	L	L	Н	L	L	
	н	L	L	L	Н	L	L	L	Н	L	
	L	н	L	L	Н	L	L	L	Н	L	
	н	Н	L	L	L.	н	L	н	Н	L	
	L	L	Н	L	L	н	L	Н	Н	L	
	Н	L	Н	L	Н	Н	L	L	L	Н	
- 1	L	Н	н	L	Н	Н	L	L	L	Н	
Į	Н	Н	Н	L	L	L	н	н	L	Н	
- 1	L	L	L	Н	L	Н	L	н	Н	L	
- 1	Н	L	L	н	н	Н	L	L	L	Н	
	L	н	L	н	н	н	L	L	L	н	
١	Н	Н	L	н	L	L	Н	Н	L	Н	
	L	L	Н	н	L	L	н	н	L	Н	
	Н	L	Н	н	н	L	н	L	Н	Н	
	Ë	H	н	Н	н	L	н	L	н	Н	
	H	Н	Н	Н	L	Н	Н	н	Н	Н	
C	21–A4H	l–E0	Sh	neet 1/2							

### Note:

Input conditions at A1, A2, B1, B2 and CI are used to determine outputs S1 and S2 and the value of the internal carry C2.

The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4 and CO.

Page 15-5



# **Data Latch Family**

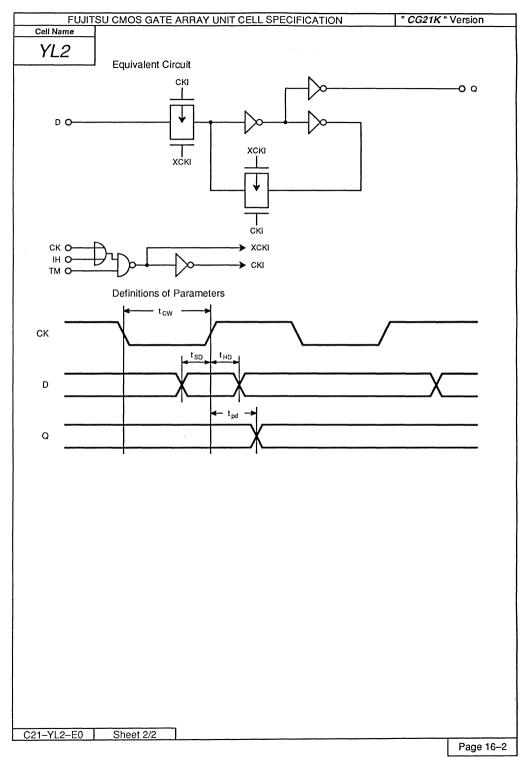
Page	Unit Cell Name	Function	Basic Cells
3-261	YL2	1-bit Data Latch with TM	5
3-263	YL4	4-bit Data Latch with TM	14
3-265	LTK	Data Latch	4
3–267	LTL	1-bit Data Latch with Clear	5
3-269	LTM	4-bit Data Latch with Clear	16
3-272	LT1	S-R Latch with Clear	4
3-274	LT4	4-bit Data Latch	14

E11117	ISU CMOS GATE AR	DAV LINIT	CELLS	DECIEIC	ATION		" CG21F	(" Va	reion	
Cell Name	Function	INAT CIVIT	OLLLO	LOITIO	TION		T COL !!		Number of BC	
YL2	1-bit Data Latc	h with TI	M						5	
Ce	I Symbol	T		Proj	pagation D	elay Paran	neter			
		tı	IP KCL		to	in			Path	
				t O	KCL	KCL2	CL2 CDR2		Path	
		1.446	0.032	1.485	0.017				, IH to Q	
		0.614	0.032	0.680	0.017		1 1	D t	o Q	
			l							
_							1			
D —	°									
ск ——ф							1			
IH ——							1			
тм ——ф										
			Ì							
			L							
		Paramete		Symbol	7	yp (ns) *				
		Clock P	h		tcw		4.0			
		CIOCK	uise wiat	<u> </u>			1 CW		7.0	
		Data Se	etup Time				t <sub>SD</sub>		1.9	
		Data Ho	Data Hold Time						1.5	
		4				İ				
Pin Name	Input Loading Factor (lu)									
D	2 1	7								
CK	1 1					- 1				
IH TM						ł				
						-				
Pin Name	Output Driving	1								
	Factor (lu)	1								
Q	36					L				
					operating of					
			The values for the worst case operating condition are given by the maximum delay multiplier.							
Nana .										
Note :	nal must be kept LOW durin	a the SCAN	Modo							
me nvitemii	iai iliusi be kepi LOW dulli	y ale SCAN	WIGGE.							

	Inj	out	Output	Mode		
TM	IH	СК	D	a	iviode	
L	Х	Х	D	D	SCAN	
н	Н	Х	Х	Q <sub>0</sub>		
н	х	Н	х	Q <sub>0</sub>	LATCH	
Н	L	L	D	D		

C21-YL2-E0	Sheet 1/2

Page 16-1



	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	K"\	
Cell Name	Function								Number of BC
YL4	4-bit Data Latch	with Ti	M						14
Cel	Symbol			Proj	pagation D	elay Paran	neter		
		ıρ			in	,	l	Path	
	t O	KCL	t O	KCL	KCL2	CDR2			
		1.762 0.581	0.032 0.032	1.815 0.680	0.017 0.017				K, IH to Q to Q
D1	Q1								
D2 ————————————————————————————————————	Q2 Q3								
D4	Q4								
ск — с									
тм ——ф									
		Paramete	r			L	l Symbol		Typ (ns) *
		1 diamen	·				Cymoo.	_	1,75 (1.15)
		Clock P	ulse widt	h (CK)			t <sub>CW</sub>		4.2
		Data Se	tup Time	(D)			t sp	<u> </u>	1.1 2.4
		Data Ho	old Time	(D)			t <sub>HD</sub>		2.4
Pin Name	Input Loading Factor (lu)								
D CK	2	1							
I CK						ŀ			
ТМ	1								
		1				-			
Pin Name	Output Driving Factor (lu)								
Q	36	L							
			ues for the	r the typical worst case			given by th	ie ma	aximum delay

# Note:

The TM terminal must be kept LOW during the SCAN Mode.

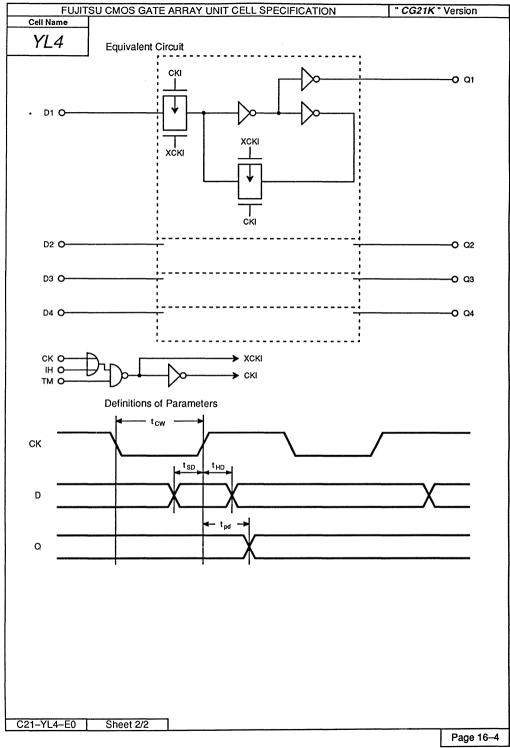
## Function Table

	In	out	Output	Mode		
TM	IH	I CK Dn		Qn	Wiode	
L	Х	Х	D	D	SCAN	
Н	Н	Х	Х	Qn <sub>0</sub>		
н	х	н	Х	Qn <sub>0</sub>	LATCH	
н	L	L	D	D		

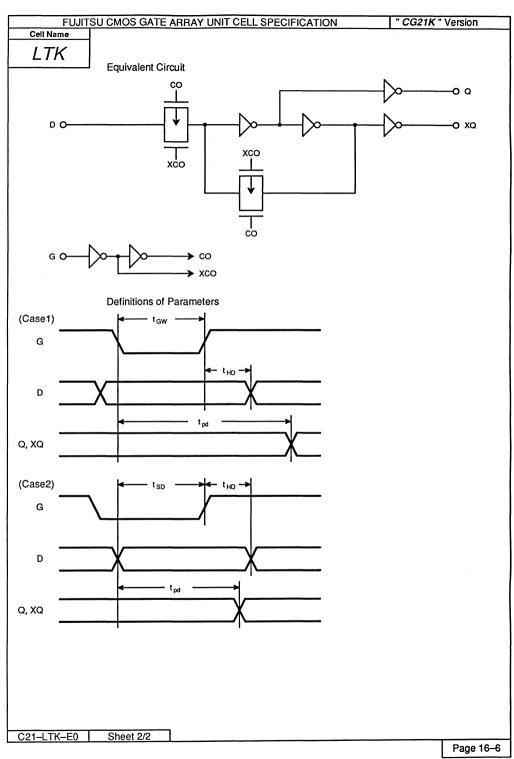
n = 1 ~ 4

C21-YL4-E0	Sheet 1/2

Page 16-3



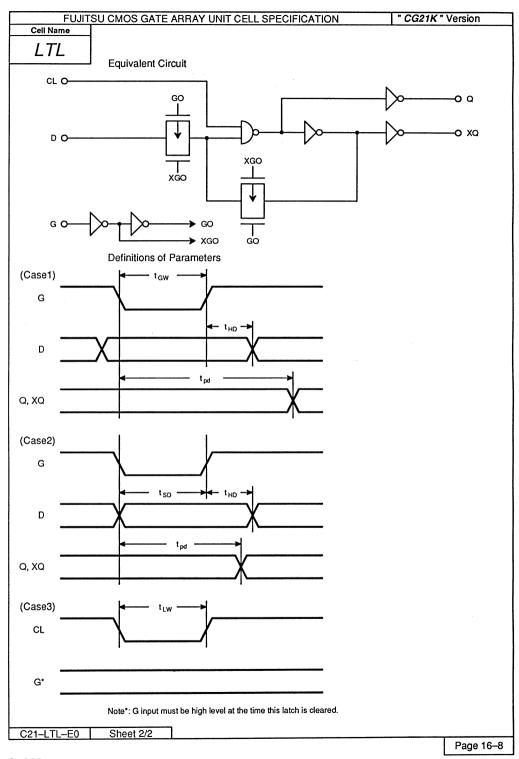
FUJIT	SU CMOS GATE AR	RAY UNIT	CFLLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function Function	nat ONL	OLLL 3	r LOITIO	TION		OGZIK	Number of BC
LTK	Data Latch							4
Cel	Symbol	1	Propagation Delay Parameter					
		t O	KCL	t O	KCL to	In KCL2	CDR2	Path
		0.548 0.766	0.060 0.060	0.607 0.865	0.039 0.039	KCLZ	CDR2	D to Q D to XQ
		0.924	0.060	0.964 1.234	0.039			G to Q G to XQ
			0.000	1.201	0.000			G 10 AG
G —d								
L.	b— xa							
		Paramete	er .				Symbol	Typ (ns) *
			Pulse W	idth			t GW	2.5
		Data S	etup Time				t <sub>SD</sub>	1.0
		Data H	old Time				t HD	1.4
Pin Name	Input Loading Factor (lu)							
D G	2 1					İ		
Pin Name	Output Driving Factor (lu)							
a xa	18 18	* Minimu	m values fo	r the typical	operating o	condition.		
		The val		worst case	operating o	ondition are	given by the	maximum delay
Function Table								
Inputs	Outputs							
D G	Q XQ							
х н	Q <sub>0</sub> XQ <sub>0</sub>							
нь	H L							
L L	L H							
C21-LTK-E0	Sheet 1/2							
								Page 16-5



	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	C" Version	
Cell Name	Function							Nun	nber of BC
LTL	1-bit Data Latc	h with Cl	ear						5
Cel	l Symbol			Pro	pagation D	elay Paran	neter		
						ln	,	Pa	ath
		10	KCL	t O	KCL	KCL2	CDR2		
D ————————————————————————————————————	о — хо	0.733 0.627 0.805 1.036 1.175	0.060 0.060 0.060 0.060 0.060	0.449 0.647 0.904 1.017 1.327	0.039 0.039 0.039 0.039 0.039			CL to CD to CD to XG to CG to X	Q Q
	CL	Paramete	Parameter					Тур	(ns) *
		G Input	G Input Pulse Width					2	.5
		1					t <sub>SD</sub>		.8
			Data Setup Time Data Hold Time						.3
		Data H	old Time				t <sub>HD</sub>		.0
		Clear P	Clear Pulse Width					2	:.5
Pin Name	Input Loading Factor (lu)								
D G CL	2 1 1								
Pin Name	Output Driving Factor (lu)								
Q XQ	18 18	Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the maximum of multiplier.							n delay

	Inputs	Out	Outputs			
CL	D	G	Q	XQ		
L	х	Н	L	Н		
н	X	Н	Q <sub>0</sub>	$XQ_0$		
н	Н	L	н	L		
н	L	L	L	Н		

C21-LTL-E0	Sheet 1/2
UZI-LIL-EU I	311661 1/2

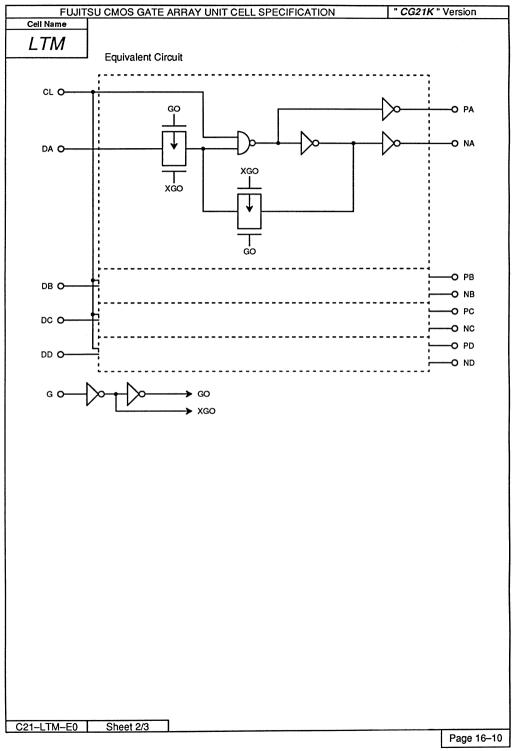


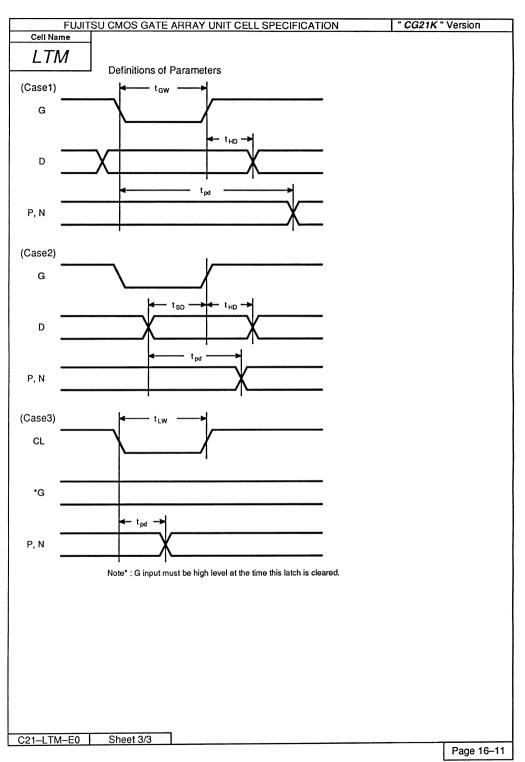
	FULIIT	SILCM	OS GATE	ARR	AY UNIT	CELLS	PECIFICA	ATION		" CG21	IK"	Version
Cell Nar			nction	. 7 (1 (1)	17 (1 OIVI	OLLLO	1 2011 107	111011				Number of BC
LTN	1	4bi	it Data l	atch.	with CI	ear						16
	Cel	Symbol					Pro	pagation D	elay Par	ameter		
						ip			in		4	Path
					t 0	KCL	t 0	KCL	KCL2	CDR2	+-	
DA PA			0.812 0.647 0.845 1.380 1.446	0.060 0.060 0.060 0.060 0.060	0.515 0.680 0.944 1.294 1.663	0.039 0.039 0.039 0.039 0.039				CL to P, N D to P D to N G to P G to N		
DB — DC — DD — G —	DC —— PB —— NB —— PC											
		Y		- 1	Paramete		-111-			Symbol t GW	+	Typ (ns) *
í		CL		ł	G Input	G Input Pulse Width					+	2.5
		<b>V</b> L		Ì	Clear Pulse Width					t LW		2.5
				-		tup Time				t <sub>SD</sub>	+-	1.0
Pin Nam D G CL	ne		ut Loading actor (lu) 2 1 4									
Pin Nam	ne		tput Driving actor (lu)									
P N			18 18			ues for the		operating o			the ma	aximum delay
Function 1	Table											
	Inputs		Outpo	its	7							
CL	D	G	Р	N	1							
L	Х	н	L	Н	1							
н	X	Н	Po	$N_0$				,				
н	н	L	н	L								
Н	L	L	L	н								
· · · · · · · · · · · · · · · · · · ·		en en en en en en en en en en en en en e	•		_							

Sheet 1/3

C21-LTM-E0

Page 16-9

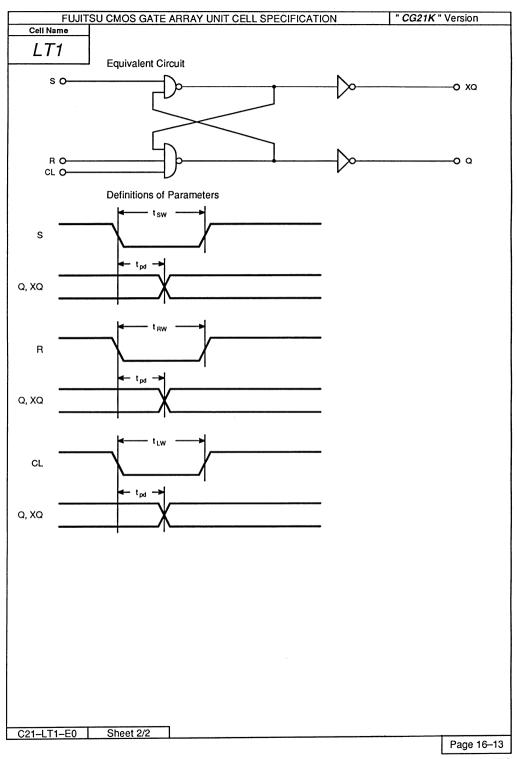




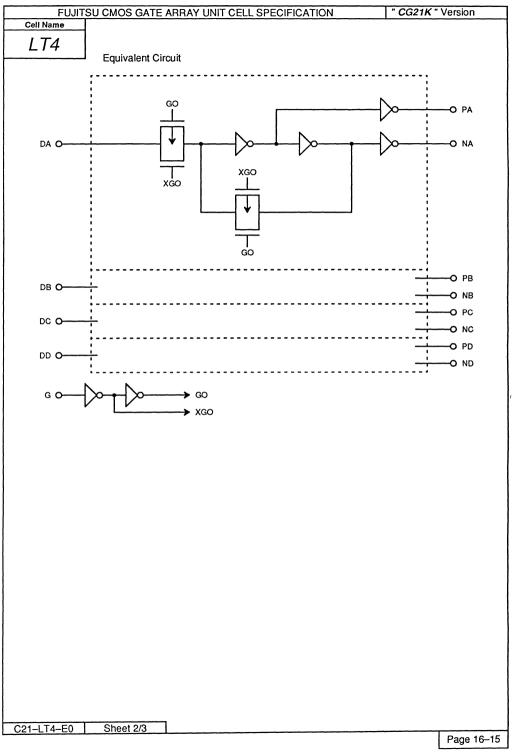
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version						/ersion					
Cell Name		nction			<u> </u>						Number of BC
LT1			with (	CLEAR							4
Cell	Symbol					Pro	pagation D		meter		
				t O	KCL	t O	KCL	In KCL2	CDR2		Path
s — Q Q XQ				0.931 0.825 0.759	0.060 0.060 0.060	0.469 0.548 0.489	0.039 0.039 0.039	KOLL	OUTE	F	S to Q, XQ I to Q, XQ CL to Q, XQ
	İ										
	CL			Paramete					Symbol		Typ (ns) *
				Set Puls	se Width				t sw	<u> </u>	2.5
					V. 1 VA (*-1						2.5
				Reset Pulse Width					t RW	$\vdash$	2.5
			Clear Pulse Width					t <sub>LW</sub>	┢	2.5	
				Olour Falos Width							
Pin Name	Pin Name Input Loading Factor (lu)										
S R CL	1										
Pin Name	Out	tput Drivi actor (lu)	ng )								
Q XQ		18 18								L	
XQ		10		* Minimui The vali multiplie	ues for the	r the typical worst case	operating o	condition. ondition a	re given by th	e ma	aximum delay
Function Table							-				
Inputs		Out	puts	7							
CL S	R	Q	XQ	]							
LH	н	L	Н								
н н	н	Q <sub>0</sub>	XQ <sub>0</sub>								
н н	L	L	н								
Н Г	н	Н	L								
Н	Ľ		bited								
	_	Linni	UILEU	J							

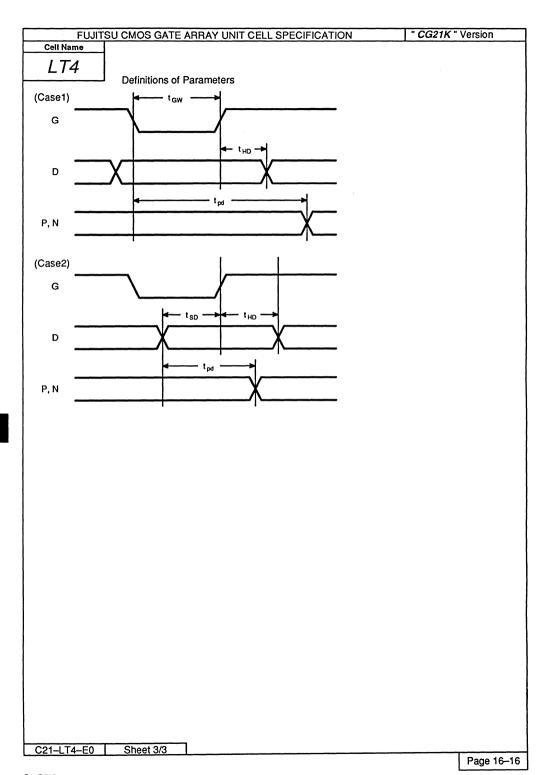
Page 16-12

C21-LT1-E0 | Sheet 1/2



Cell Name	FILIT	SUCMOS GATE ARI	RAY LINIT	CELLS	PECIFICA	ATION		" CG21K	" Version
14   14   14   14   15   15   15   15								Number of BC	
Du	LT4	4-bit Data Latch							
10   KGL   10   KGL   CDR2   Path	Cell	Symbol			Proj			neter	
1.320								CDR2	Path
DB DC PB PB NB PC PB NB PC PC PD NC P			1.320 0.555	0.060 0.060	1.611 0.627	0.039 0.039			G to N D to P
Cal-LT4-E0   Sheet 1/3   She	DB ————————————————————————————————————	O							
Data Setup Time tso 1.0 Data Hold Time tso 1.4  Pin Name Input Loading Factor (Iu)  Plin Name Output Driving Factor (Iu)  P 18 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs D G P N H H Po No L H Po No H L H L L L H  C21-LT4-E0 Sheet 1/3					dth				
Pin Name   Input Loading Factor (tu)    Pin Name   Output Driving Factor (tu)    Pin Name   P									
Pin Name Input Loading Factor (tu)  Pin Name Output Driving Factor (tu)  Pin Name Factor (tu)  Pin Name Sector (tu)  Pin Name Factor (tu)  Pin Name Output Driving Factor (tu)  Pin Name Factor (tu)  Pin Name Output Signature (to the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  D G P N  H H Po No  L H Po No  H L H L  L L H  C21-LT4-E0 Sheet 1/3			Data Se	etup Time					
Pin Name			Dala no	old Time				r HD	1.9
Pin Name	D. M.	Input Loading							
Pin Name Pin Name Pin Name Pin 18 N 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs D G P N H H P O N O L H P O N O L H L L L L H  C21-LT4-E0 Sheet 1/3		Factor (lu)	]						
Function Table  Function Table  Function Table  Inputs Outputs D G P N H H Po No L H Po No H L H L L L H  C21-LT4-E0 Sheet 1/3	D G	1							
Function Table  Function Table    Inputs	Pin Name	Factor (lu)							
Inputs	P N	18 18	The val	ues for the				e given by the	maximum delay
D G P N H H P <sub>0</sub> N <sub>0</sub> L H P <sub>0</sub> N <sub>0</sub> H L H L L L H	Function Table								
H H P <sub>0</sub> N <sub>0</sub> L H P <sub>0</sub> N <sub>0</sub> H L H L L L H	Inputs	Outputs							
L H P <sub>0</sub> N <sub>0</sub> H L H L L L H	D G	P N							
H L H L L L H	н н	P <sub>0</sub> N <sub>0</sub>							
C21-LT4-E0 Sheet 1/3	LH	P <sub>0</sub> N <sub>0</sub>							
C21-LT4-E0 Sheet 1/3	Н ь	H L							
C21-LT4-E0 Sheet 1/3	LLL	LH							
C21-LT4-E0   Sheet 1/3   Page 16-14									
	U21-L14-E0	Sneet 1/3							Page 16-14





# **Shift Register Family**

Page	Unit Cell Name	Function	Basic Cells
3–279	FS1	4-bit Serial-in Parallel-out Shift Register	18
3-281	FS2	4-bit Shift Register with Synchronous Load	30
3-283	FS3	4-bit Shift Register with Asynchronous Load	34
3-286	SR1	4-bit Serial-in Parallel-out Shift Register with Scan	36

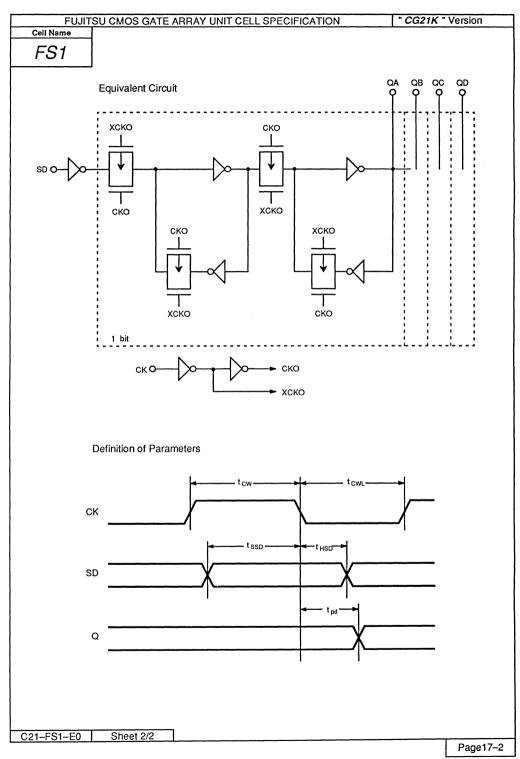
	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFIC.	ATION		" CG21K	( " Version
Cell Name	Function							Number of BC
FS1	4-bit Serial-in	4-bit Serial-in Parallel-out Shift Register						
Cel	l Symbol			Pro	pagation D	elay Paran	neter	
		tı	ıb			dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
SD — C	1.281	0.060	1.657	0.039	0.056	4	CK to Q	
		Parameter					Symbol	Typ (ns) *
		Clock Pulse Width					t <sub>CW</sub>	2.5
		SD Setup Time					t ssD	0.4
		SD Hold Time					t HSD	0.2
		Clock C ≤16 lu					t cwt**	3.4
	Input Loading	Clock C ≤ 16 lu Pause 16 < C ≤ 32 lu					t cwt**	5.0
Pin Name	Factor (lu)	Time		< C ≤48			t cwt**	6.4
SD CK	1 1	* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum de multiplier.						maximum delay
Pin Name	Output Driving Factor (lu)				the load(c) nals, QA, QI	3, QC and	QD.	
Q	16							

Inp	outs	Outputs					
SD	СК	QA	QB	QC	QD		
SD	<b>→</b>	SD	QAn	QBn	QCn		

NOTE: • SD = H or L

 QAn, QBn and QCn are levels of QA, QB, and QC respectively, before the falling edge of CK, i.e.
 bit shift by the falling edge of CK.

C21-FS1-E0	Sheet 1/2
------------	-----------



	SU CMOS GATE AF	RRAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of I
FS2	4-bit Shift Re	4-bit Shift Register with Synchronous Load						30
Cel	Symbol			Pro	pagation D	elay Paran	neter	
		tı	ıρ			dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		1.228	0.060	1.657	0.039	0.056	4	CK to Q
PA PB PC PD CK C	PB — QB — QC — QD — QD — SD — CK — C		er ulse Widt up Time d Time	h			Symbol t cw t ssp t hsp	Typ (ns) * 2.5 1.7 0.8
		Load Setup Time					t <sub>SL</sub>	2.6
			Load Hold Time					0.3
	•							
		P Setup					t SP	2.1
Pin Name	Input Loading Factor (lu)	P Hold	Time				t <sub>HP</sub>	0.9
CK	1	Clock		C ≦16	lu		t cwL**	3.4
SD	į į	Pause		< C ≦32			t cwL**	5.0
L P	1	Time	32	< C ≦48	lu		t cwL**	6.4
Pin Name	Output Driving Factor (lu)	Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  "The value of tcwl_depends on the load(c)						

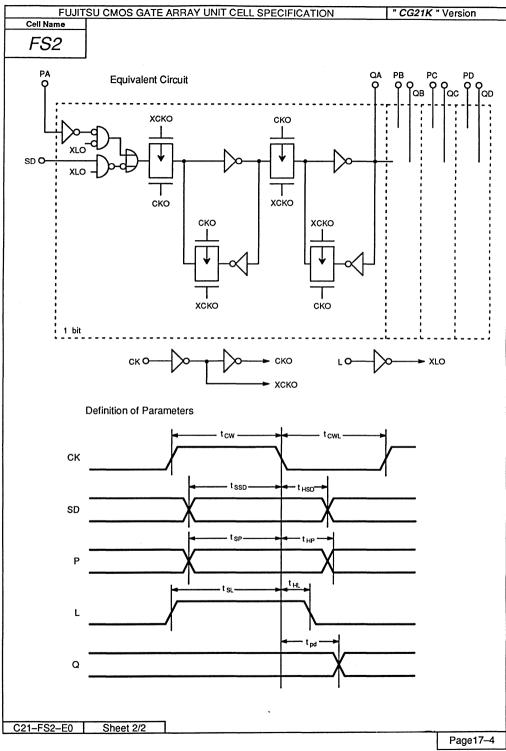
		Inp	outs		Outputs				
S	D	L	Р	СК	QA	QB	QC	QD	
s	D	L	×	<b>↓</b>	SD	QAn	QBn	QCn	
	×	Н	Р	<b>↓</b>	PA	РВ	PC	PD	

NOTE: • SD = H or L

- QAn, QBn and QCn are levels of QA, QB, and QC respectively, before the falling edge of CK, i.e.
   bit shift by the falling edge of CK.
- P represents PA, PB, PC and PD.

C21-FS2-E0	Sheet 1/2
------------	-----------

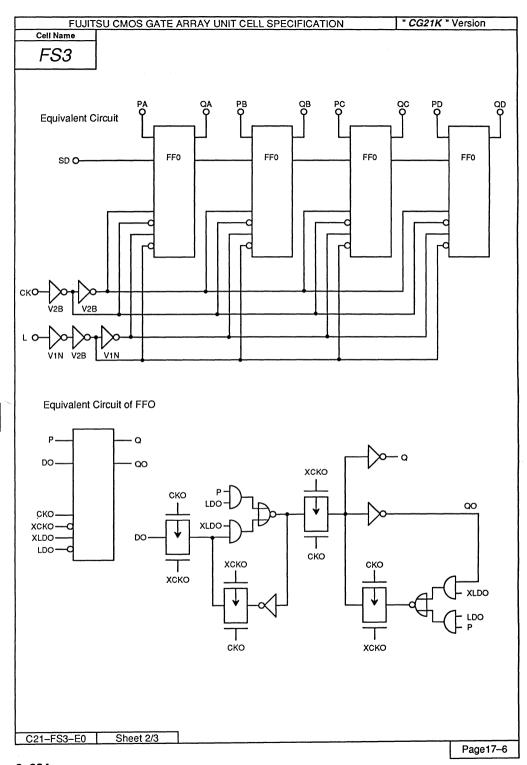
Page17-3

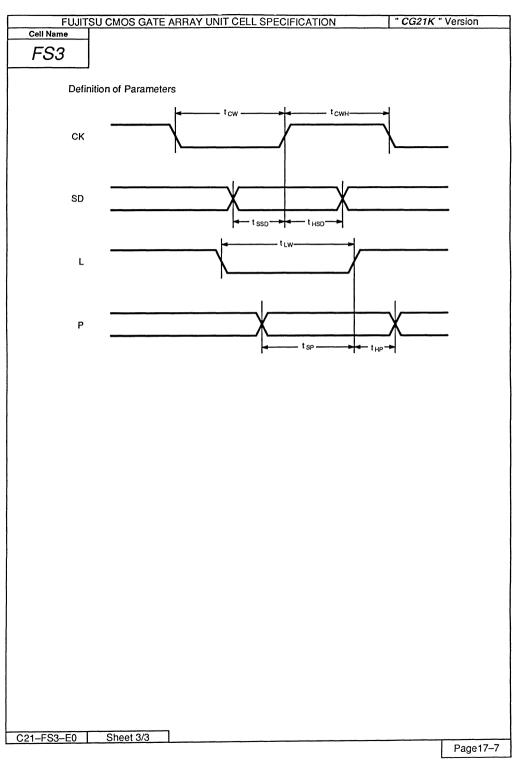


	ISU CMOS GATE AF	RAY UNIT	CELL S	PECIFIC	ATION		" CG21K	( " Version		
Cell Name	Function							Number of BC		
FS3	4-bit Shift Reg	ister with	ster with Asynchronous Load							
Се	II Symbol	T		Pro	elay Paran	neter	<u>-</u>			
		tı	ιp		to	in		Path		
		t O	KCL	t O	KCL	KCL2	CDR2	Pain		
PA — PB — PC — PD — SD — CK — C	PB — QB — QC PD — QD SD — CK — QD		0.064 0.064 0.064	1.122 1.848 1.597	0.050 0.050 0.050			CK to Q L to Q P to Q		
		Paramete					Symbol	Typ (ns) *		
		Clock Pulse Width					tcw	2.5		
		Clock P	ause Tim	e			t cwH	2.5		
		Load Pu	ulse Widtl	1			t <sub>LW</sub>	3.7		
		SD Setu					t ssp	0.6		
Pin Name	Input Loading Factor (lu)	SD Hold	d Time				t HSD	1.1		
	1	P Setup	Time			-+	tsp	0.3		
CK SD	2	P Hold					t <sub>HP</sub>	1.4		
L P	2 2 1 2									
Pin Name	Output Driving Factor (lu)									
Q	18		ues for the		operating o		given by the	e maximum delay		

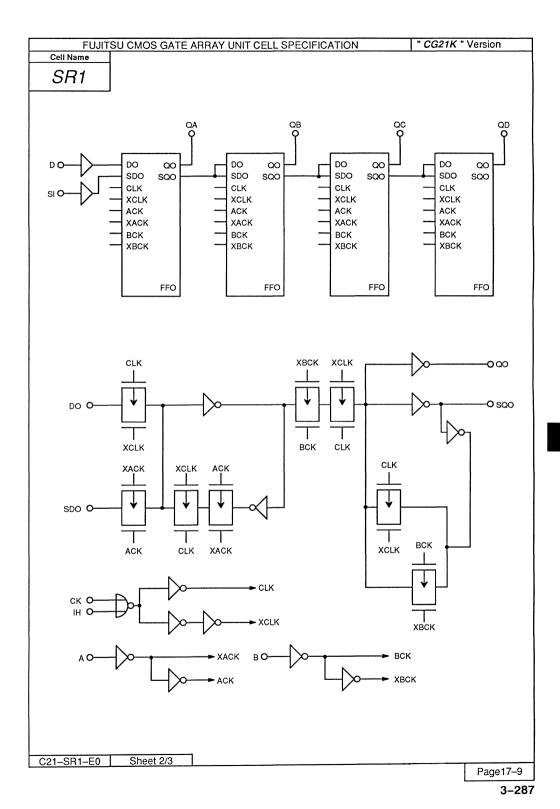
	Inp	Outputs		
L	Р	SD	α	
L	L	х	х	L
L	Н	х	Х	н
н	Х	L	1	L
Н	Х	Н	1	Н

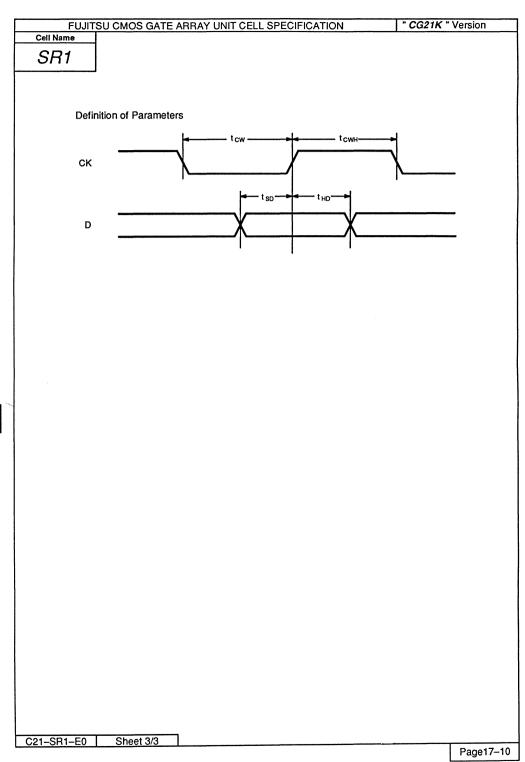
C21-FS3-E0 | Sheet 1/3





FILIT	SU CMOS GATE ARE	TIMI VAC	CELLS	PECIFIC	ATION		" CG21k	( " Version	
Cell Name	Function	TAT UNIT	OELL 3	r LOII-IO	ATION		CGZII	Number of BC	
SR1	4-bit Serial-in F	Parallel-	out Shif	t Regist	er with	SCAN	***************************************	36	
Cel	Symbol	Propagation Delay Parameter							
		tup tdn							
□ □	QA	1.729	0.032	1.782	0.034	0.050	7 7	CK to Q	
CK————————————————————————————————————	— QB — QC — QD	Paramete	er er				Symbol	Typ (ns) *	
			ulse Wid	th			tcw	2.5	
		Clock P	ause Tim	ie .			t cwn	3.3	
		Data Se	etup Time				t <sub>SD</sub>	2.0	
		Data Ho	old Time				t HD	0.9	
Pin Name	Input Loading								
Pin Name	Factor (lu)								
D CK IH SI A,B	1 1 1 1								
Pin Name	Output Driving Factor (lu)								
Q	36	Minimu     The val     multiplie		r the typical worst case	operating o	condition. ondition a	are given by th	e maximum delay	
C21-SR1-E0	Sheet 1/3								
C21-3H1-EU	J SHEEL 1/3							Page17-8	
								L . ugo . , o	





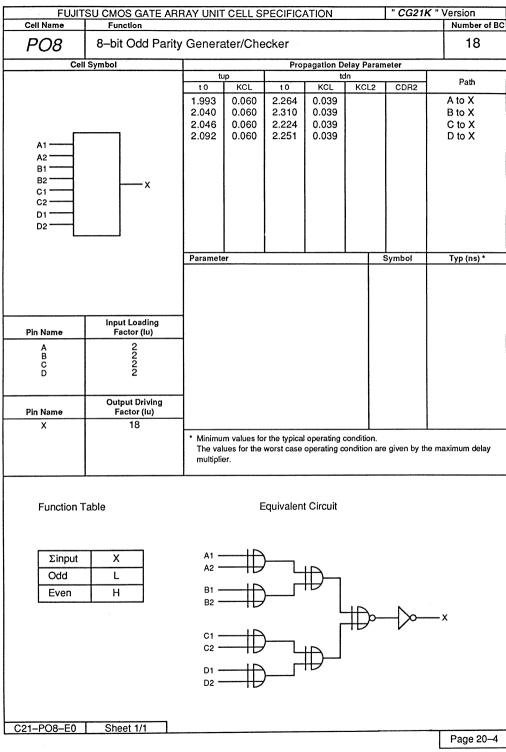
# Parity Generator/Selector/Decoder Family

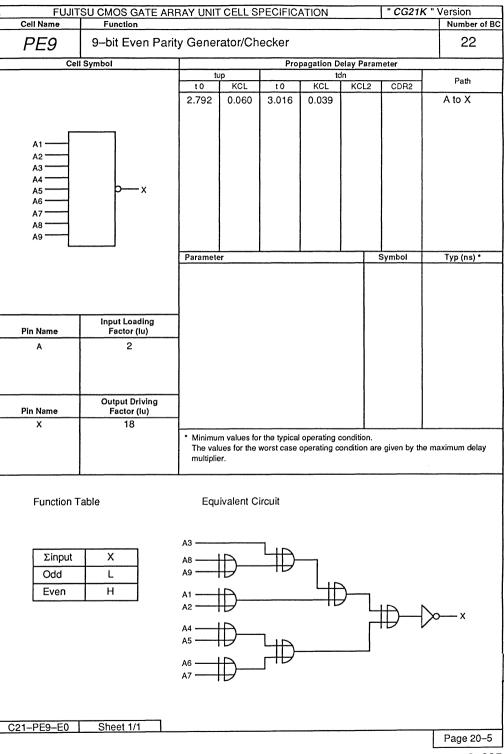
Page	Unit Cell Name	Function	Basic Cells
Parity Ge	nerators/Ch	neckers	
3-291	PE5	5-bit Even Parity Generator/Checker	12
3–292	PO5	5-bit Odd Parity Generator/Checker	12
3-293	PE8	8-bit Even Parity Generator/Checker	18
3–294	PO8	8-bit Odd Parity Generator/Checker	18
3–295	PE9	9-bit Even Parity Generator/Checker	22
3–296	PO9	9-bit Odd Parity Generator/Checker	22
Data Sele	ctor		
3–297	P24	4-wide 2:1 Data Selector	12
Decoders	;		
3–298	DE2	2:4 Decoder	5
3–299	DE3	3:8 Decoder	15
3–301	DE4	2:4 Decoder with Enable	8
3–302	DE6	3:8 Decoder with Enable	30
Selectors	;		
3-304	T2B	2:1 Selector	2
3–305	T2C	Dual 2:1 Selector	4
3–307	T2D	2:1 Selector	2
3-308	T2E	Dual 2:1 Selector	5
3–309	T2F	2:1 Selector	8
3–311	T5A	4:1 Selector	5
3–313	V3A	1:2 Selector	2
3–314	V3B	Dual 1:2 Selector	4
Magnitud	e Comparat	or	
3–315	MC4	4-bit Magnitude Comparator	42

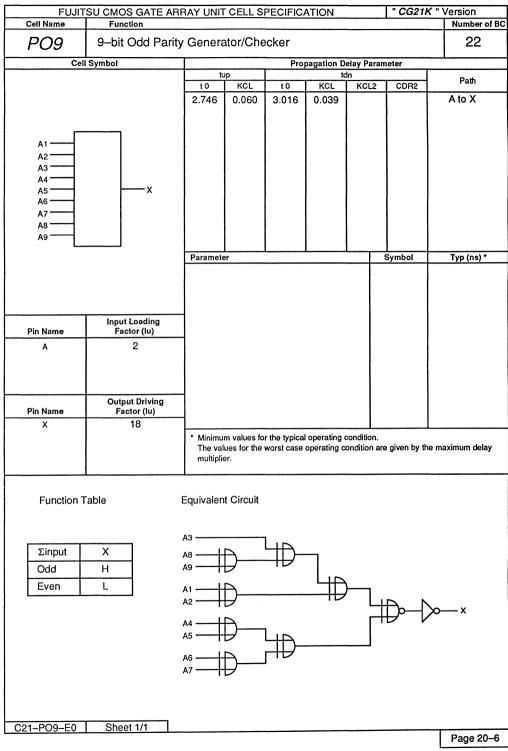
CILIIT	SU CMOS GATE ARF	TIMI VA	CELLS	PECIFICA	ATION		" CG211	K " Version
Cell Name	Function	AT UNIT	CELL S	PECIFICA	ATION		CGZ11	Number of B
PE5	5-bit Even Parit	y Gener	ator/Ch	ecker				12
Cell	Symbol			neter				
			ip			l KCIS	CDBs	Path
A	р—-х	1.386 1.386 2.185	0.032 0.032 0.032	1.802 1.729 2.554	0.017 0.017 0.017	KCL2	CDR2	A to X B to X C to X
C2								
		Paramete			l	L	Symbol	Typ (ns) *
		Paramete	71 				Symbol	Typ (IIs)
Pin Name	Input Loading Factor (lu)							
Α	2					1		
B C	2 2 2							
	Output Driving							
Pin Name	Factor (lu)							
Х	36							
		* Minimul The val multiplie	ues for the	r the typical worst case	operating o	condition. ondition are	given by th	e maximum delay
Function T	able		E	quivalent	t Circuit			
		B1 —	- 10	_				
Σinput	X	B2 -	-+	)				
Odd	L				Ĺ	44	N	
Even	Н				Г	+	√v—	-x
		C1 — C2 —	1					
		A -						
						•		
C21-PE5-E0	Sheet 1/1							Page 20-1
								3_20

		ταν ιικιίΤ	CELLS	PECIFICA	MOITA	4	" CG21K "	Version
Cell Name	SU CMOS GATE ARF Function	IATE OINT	JLLL O		TION			Number of BC
PO5	5-bit Odd Parity	Genera	ator/Che	ecker		,		12
Cell	Symbol			neter				
		t O	KCL	t O	KCL	ln KCL2	CDR2	Path
		1.393 1.512	0.032 0.032	1.624 1.604	0.017 0.017	KOLE	ODAZ	A to X B to X
		2.211	0.032	2.409	0.017			C to X
B1	x							
C1 C2								
		Paramete	er		l	L	Symbol	Typ (ns) *
	•		***************************************					·
						į		
						ļ		
						1		
Pin Name	Input Loading Factor (Iu)							
A B	2							
C	2 2 2							,
						l		
	Output Driving							
Pin Name X	Factor (lu) 36							
,	00	* Minimu	m values fo	r the typical	operating of	condition.		
		The val		worst case	operating c	ondition are	given by the m	naximum delay
Function T	able		Е	quivalent	t Circuit			
Σinput	X							
Odd	Н		31 ———	#)-		_		
Even	L					''		
							$\sim$	— x
		(	C1	AH-	_11	'	•	
			C2	+1	$\mathcal{AD}$			
			Α					
			••					
CO1 PO5 50	Sheet 1/1							
C21-PO5-E0	SHEEL I/I							Page 20-2

			- 05:1: 0				l " 000444	
Cell Name	SU CMOS GATE ARE	RAY UNII	CELLS	PECIFICA	ATION		" CG21K	" Version Number of BC
PE8	5-bit Even Parit	y Gener	ator/Ch	ecker				18
Cell	l Symbol			Pro	pagation D		neter	
		t O	IP KCL	t O	KCL to	ln KCL2	CDR2	Path
A1 ————————————————————————————————————	р—-х	2.033 2.079 2.079 2.125	0.060 0.060 0.060 0.060	2.290 2.337 2.323 2.370	0.039 0.039 0.039 0.039	KOLZ	CUNZ	A to X B to X C to X D to X
		Paramete		L			Symbol	Typ (ns) *
	Input Loading							
Pin Name	Factor (lu)					ł		
A B C D	2 2 2 2							
Pin Name	Output Driving Factor (lu)							
X	18		ues for the v		operating co		given by the	maximum delay
Function T	able able		E	quivalent	Circuit			
Σinput Odd Even	X L H	A1 - A2 - B1 - B2 - C1 - C2 - D1 - D2 -		)—( )—( )—(		#)-	<b></b> >	— x
UZ1-FE0-EU ]	Sileet I/I							Page 20-3
								3_293







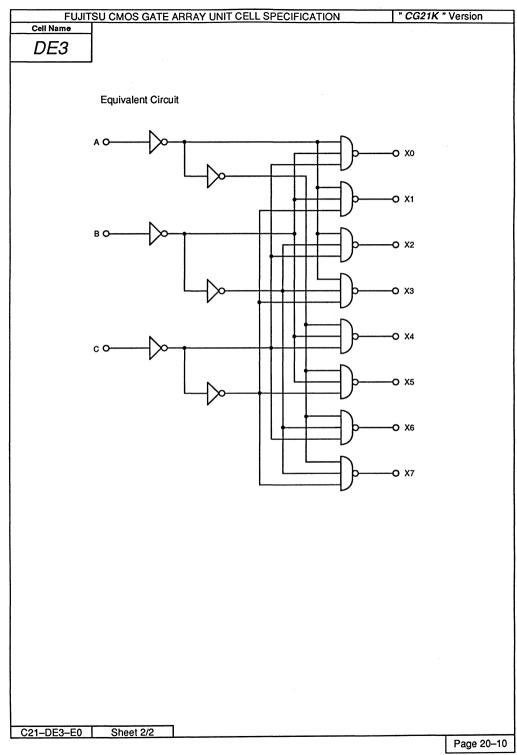
Cell Name	FUJI	TSU CMOS GATE ARF	RAY UNIT	CFLLS	PECIFICA	ATION	 " CG21k	( " Version
Cell Symbol   Delay Parameter   Delay Parameter   Delay Parameter   Delay Parameter   Delay Parameter   Delay Record   Delay Parameter   Delay Record   Delay Parameter   Delay Record   Delay Parameter   Delay Record   Delay Parameter   Delay Record   Delay Re							 	Number of BC
To   KoL   10   KoL   KoL   CDR2   Path	P24	4-wide 2 : 1 Dat	ta Selec	tor				12
10   KCL   10   KCL   CDR2   Path	Се	II Symbol			Pro		neter	
O.514   O.032   O.515   O.017   SA to X   SA					t O		 CDR2	Path
Pin Name Input Loading Factor (lu)  A 1 1	L.	x <sub>1</sub>	0.614 0.429	0.032 0.032	0.515 0.502	0.017 0.017		B to X SA to X
Pin Name   Input Loading   Factor (lu)   A	A2 ————————————————————————————————————	хз				:		
Pin Name Factor (tu)  A 1 B 1 S 4  Pin Name Output Driving Factor (tu)  X 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table Equivalent Circuit  SA SB Xn L L L L H Bn H H An+Bn  A1 A2 A3 A4 A4 A4 A5 A5 B5 A1 A2 A3 A3 A4 A4 A4 A5 A5 A5 A5 A5 A5 A5 A5 A5 A5 A5 A5 A5	1		Paramete	er			Symbol	Typ (ns) *
Pin Name Pin Name Pin Name Pin Name Sactor (lu)  X  36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Equivalent Circuit  A1 B1 B1 B2 B2 B2 B3 B3 B3 B3 B3 B3 B3 B3 B3 B3 B3 B3 B3	Pin Name	Factor (lu)						
Pin Name  X  36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Equivalent Circuit  SA SB Xn L L L An L H Bn H H An+Bn  A2 B2 B2 A3 B3 B3 A4 B4 B4 SA SB SB  C21-P24-E0   Sheet 1/1	В	1						
Function Table  Equivalent Circuit  SA SB Xn L L L An L H Bn H H An+Bn  A1 A2 A3 A3 A4 A4 A4 A5A A5B A7 A8 A7 A8 A8 A8 A8 A8 A8 A8 A8 A8 A8 A8 A8 A8	Pin Name							
SA SB Xn  L L L  H L An  L H Bn  H H An+Bn  A1  B1  A2  A3  B3  A4  B4  SA  SB  C21-P24-E0 Sheet 1/1	x	36	The val	ues for the			given by the	e maximum delay
L L L H Bn H H An+Bn	Function	Table		Equiv	alent Circ	cuit		
	L H L	L L L An H Bn H An+Bn		B1 ————————————————————————————————————			xo	
	C21-P24-E0	Sheet 1/1					 	Page 20–7

Cell Name   Function   " CG21.	Number of BC
Cell Symbol   Propagation Delay Parameter     tup   tdn     t0	5
tup         tdn           10         KCL         10         KCL         KCL         KCL2         CDR2           0.416         0.060         0.574         0.062         0.062         0.469         0.060         0.515         0.062         0.062         0.198         0.060         0.238         0.062         0.062         0.060         0.	
t0         KCL         t0         KCL         KCL         KCL2         CDR2           0.416         0.060         0.574         0.062         0.062         0.469         0.060         0.515         0.062         0.062         0.198         0.060         0.238         0.062         0.062         0.060	
0.416	Path
0.469   0.060   0.515   0.062   0.198   0.060   0.238   0.062	A to X0
	A to X1
	A to X2,X3
0.469   0.060   0.515   0.062   0.152   0.062   0.152   0.060   0.297   0.062	B to X0
0.152   0.060   0.297   0.062   0.416   0.060   0.574   0.062	B to X1,X3 B to X2
A    X0	
B — X2 X3	
Parameter Symbol	Typ (ns) *
Input Loading Pin Name Factor (lu)	
<u></u>	
A 3 3	
Output Driving	
Pin Name Factor (Iu)	
X 18 * Minimum values for the typical operating condition.	L
The values for the worst case operating condition are given by the	ne maximum delay
multiplier.	
Function Table Equivalent Circuit	
Inpute Outpute	
Inputs Outputs A O	—o xo
A B X3 X2 X1 X0	- A0
L   H   H   H   L   H	—O X1
H H L H H H H	—О X2
ВО	
	—o <sub>хз</sub>
C21-DE2-E0 Sheet 1/1	
	Page 20-8

	SU CMOS GATE ARI	RAY UNIT	CELLS	PECIFICA	ATION		" CG211	K " Version
Cell Name	Function							Number of BC
DE3	3:8 Decoder							15
Cel	l Symbol			Pro	pagation D	elay Para	meter	
ì			JP			dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		0.759	0.060	0.885	0.084	l		A to X0~X3
				1.287	0.084	1	1	A to X4~X7
i —		0.706	0.060 0.060	0.911 1.314	0.084			B to X0~X3 B to X4~X7
	xo	1.234 0.654	0.060	0.944	0.084			C to X0~X3
A —	X1	1.182	0.060	1.743	0.084	1	Ì	C to X4~X7
1	X2	1.102	0.000	1.,, 40	0.004			0107477
В —	X3				ŀ	ŀ	ŀ	
1	X4 X5					1	l	
	ç — X5				i			
"	× X6 × X7					İ	1	
Í			1			1	ł	
		Paramete	l	l	l	<u> </u>	Symbol	Typ (ns) *
		Taramet	·-				<u> </u>	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
						1		
								1
1								
	Input Loading	1				- 1		
Pin Name	Factor (lu)							
Α	1	1				- 1		
B	li					- 1		į
c	1 1							
						į		
	Output Driving							
Pin Name	Factor (lu)	-						
l x	14							L
		* Minimum values for the typical operating condition.						
	1	The values for the worst case operating condition are given by the maximum delay multiplier.						
1	I	"""						

	Inputs			Outputs							
Α	В	С	X0	X1	X2	ХЗ	X4	X5	X6	X7	
L L L H H H	L H H L H			H L H H H H H	H $H$ $H$ $H$ $H$ $H$	H $H$ $L$ $H$ $H$ $H$	H H H L H H	H H H H L H H	H H H H H L H		

C21-DE3-E0 Sheet 1/2

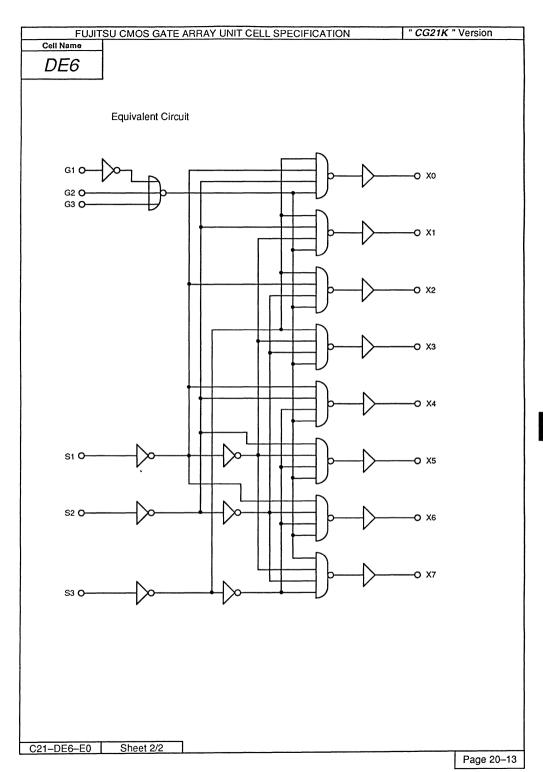


	FILIC	rsu c	MOS	SATE	ARR	AY LINIT	CELLS	PECIFICA	ATION		" CG21F	C" Version
Cell N			Functio		., ., .	/ ( ) ( ) ( ) ( )	OLLLO	I LOII 107	111011			Number of BC
DE	4	2	: 4 De	code	r wit	h Enab	ole					8
	Ce	II Symb	ol					Pro	pagation D		neter	
					}	t O	KCL	t O	KCL	In KCL2	CDR2	Path
A B	=			– X0 – X1		0.627 0.456 0.568	0.060 0.060 0.060	0.772 0.588 0.601	0.084 0.084 0.084			G to X A to X B to X
G	<u> </u>			- X2 - X3		Paramete	er				Symbol	Typ (ns) *
Pin Na	ame		nput Lo Factor	ading (lu)								
A B G			3 3 1									
Pin Na		7	Output I	Oriving	一							
X	·		14			* Minimur The value	ues for the	r the typical worst case	operating o	condition. ondition are	e given by th	e maximum delay
Fun	ction Ta	ble							Equivale	ent Circui	t	
							G G		>			
G H	A X	В	Х3 Н	X2 H	X1 H	Х0 Н	Α	<del></del>	, >>		- -	xo
L L L	L L H	L H L	H H H L	H L H	H H H	L Н Н					D-	X1
<b>L</b>	L						В		>-			— x2 — x3
C21-DE	4-E0	8	heet 1	/1								<del></del>
												Page 20–11

Cell Name	SU CMOS GATE AR	HAY UNII	CELL S	PECIFICA	ATION		CGZIK	" Version Number of E
DE6	3:8 Decoder v	vith Enab	ole					30
Cel	l Symbol			Pro	pagation D	elay Para	ameter	
			JD			in		Path
		10	KCL	t 0	KCL	KCL2	CDR2	0.1- V
		1.611 1.525	0.060 0.060	3.142 1.736	0.039 0.039			G to X S to X
G1————————————————————————————————————	X0 X1 X2 X3 X4 X5 X6 X7	Paramete	er				Symbol	Typ (ns) *
Pin Name G	Input Loading Factor (lu) 1							
S Pin Name	1 Output Driving Factor (lu)	_						
X	18	* Minimu The val multipli	lues for the	r the typical worst case	operating o	condition.	are given by the	maximum delay

G1	G2+G3	S3	S2	S1	X7	Х6	X5	X4	ХЗ	X2	X1	X0
X	H X	X	×	X	H H	Н	H H	H H	H H H	H H	H H	H H
H	L	L	Ĺ	Н	Н	Н	Н	Н	Н	Н	L	Н
H	L L	L L	H	L H	H	H	H H	H	H L	L H	H	H H
H	L	H H	L	L H	H	H H	H L	L H	H H	H	H	H H
Н	Ĺ	H	H H	L H	Н	L	H	H	H	H	H	H H
H	L	П	П	n 		П	''	•••		•••	•••	''

C21-DE6-E0 Sheet 1/2



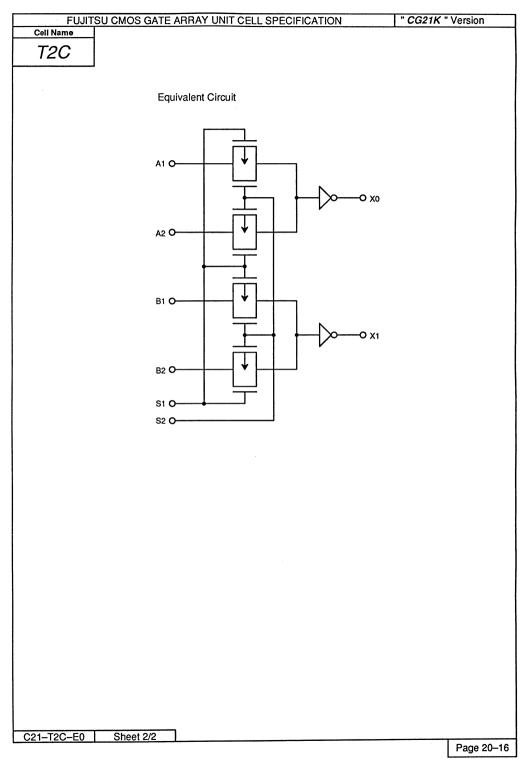
3-303

	CITIIT	SILC	408 G	ATE ADD	DAV LINI	T CELL S	PECIFIC	ATION		" CG211	K " Version
Cell Na			unction		IAT UNI	1 OLLE O	I LOII IO	ATION		1 00277	Number of BC
T21	 R	2:	1 Sel	ector							2
		Symbo			Γ	·····	Dra	pagation D	olay Para	neter	
	Cei	. Symbo	<u> </u>		<b></b>	tup	1		dn Paran	10101	n. d
					10	KCL	t 0	KCL	KCL2	CDR2	Path
					0.277 0.324	0.060	0.416	0.039			A,B to X S to X
					0.524	0.000	0.522	0.003			310 X
A -			1		•						
B -			L .	J							
S1 —	<b>-</b> d		J—.	X		1					
S2 —			]					l			
					Parame	ler	L	<u> </u>	L	] Symbol	Typ (ns) *
											. 75 ()
									l		
		In	put Loa	ding							
	Pin Name Factor (lu)										
	A,B 2 S 1										
	s 1								ļ		
		0	utput Di	iving					ļ		
Pin Na	me		Factor	(lu)					İ		
×			18		* Minim	um values fo	r the typical	l operating (	condition.		
					The va	lues for the				given by th	e maximum delay
					multipl	ier.					
Fund	tion Ta	ble						Equivale	nt Circuit		
I —	In	oute		Output	10		-				
A	Тв	outs S1	S2	Output	-			근	=		
		31	32	<del>  ^</del>	$\dashv$	А	$\longrightarrow$	↓		_	
L	H	L	Н	H				L			
H	H	L	H	L H			- 1	コ			оо х
x	H	H	L	L	- 1		-		=		
L	H	L	L	Inhibi Inhibi		5	<u>-</u>	↓			
L	L	L	"	Inhibi		В	$\overline{}$				
Н	L	Н	Н	Inhibi	t	64			-		
						S1					
						S2	J				
C21-T2	3–E0	<u>S</u>	neet 1/	1							Page 20-14
											1 ago 20 14

	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
T2C	Dual 2:1 Selec	tor						4
Cel	Symbol			Pro	pagation D	elay Paran	neter	
			JP			in		Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	
		0.271	0.060	0.409	0.039			A,B to X
		0.357	0.060	0.548	0.039			S to X
SIS	2	ļ						
			:					
ے ا		i						
A1 —	b— x₀							
A2	Γ							
B1 ——			•					
B2	þ x1	1						
		Paramete	er		·		Symbol	Typ (ns) *
		Ì						
		1					1	
	Input Loading	1					l	
Pin Name	Factor (lu)						ŀ	
A,B	2 2					l		
s	2	ł					1	
						1		
							1	
ļ	Outros Delade	-					ŀ	
Pin Name	Output Driving Factor (lu)							
		1						
X	18	* Minimu	m values fo	r the typical	operating of	condition		
							given by the	maximum delay
		multiplie			, 8			
1	l	i i						

Inp	outs			Outputs	
A1 , B1	A2 , B2	S1	S2	X0	X1
L H X L H L	X X L H H L H L		IIJJJII	H L H L Inhibit Inhibit Inhibit	H L H L Inhibit Inhibit Inhibit

C21-T2C-E0   Shee	ł	1/	2	
-------------------	---	----	---	--



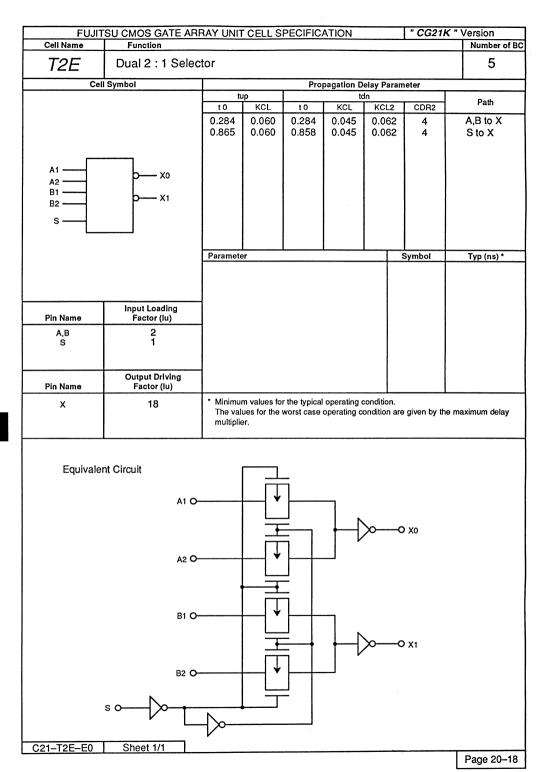
					TE ARE	RAY UNIT	CELLS	PECIFICA	ATION			" CG2	1K "	Version
	eli Name			nction										Number of B
-	T2D	'	2:1	Sele	ctor									2
		Cell	Symbol					Proj	pagation D		aram	eter		
							ıp			dn			1	Path
	A ————————————————————————————————————					0.330 0.357	0.069 0.069	0.370 0.271	0.056 0.056	КС	LZ	CDR2		A,B to X S to X
	<b>01</b>	L				Paramete	er				S	Symbol		Typ (ns) *
P	Pin Name Input Loading Factor (Iu)  A,B 1 S 1													
Pi	in Name	•	Out F	tput Driv actor (Iu	ving u)	* Minimu	m values for	r the typical	operating congressing	conditio	on.	given by	the m	aximum delay
						multiplie		worst case	operating of	OTTORIO		given by		
i	Functio	on Tab	ole						Equivale	nt Cir	cuit			
ļ	Γ	In	nute		Outp	uts				Г				
	A B S1 S2 L X L H				X	X A O O								
	H X L H L H X L H L H X H H L L L Inhi H L L Inhi H L L Inhi H L L Inhi H L L Inhi H L L H H Inhi				oit oit	\$	в О	<b>&gt;</b> —					——• х	

S2 O-

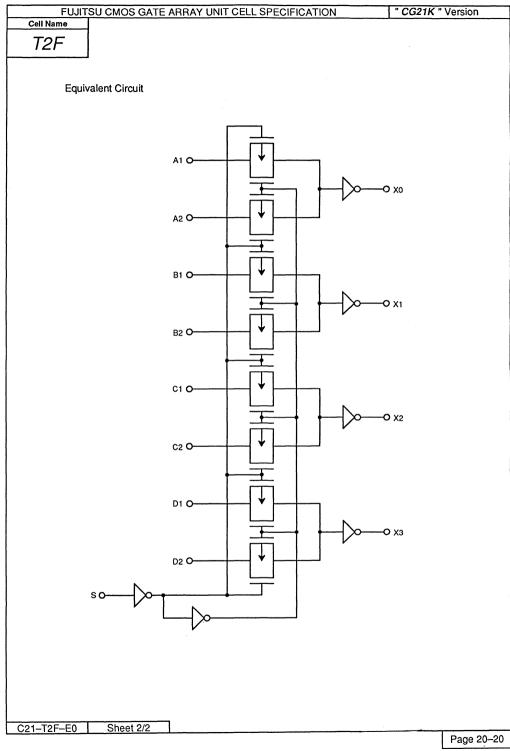
C21-T2D-E0

Sheet 1/1

## Page 20–17 3–307



EL US	CU ONOS SATE ADI	2 424 1 1417	OFIL O	DEOISIO	ATION		L # 0004	· 11 1	· · · · · · · · · · · · · · · · · · ·
Cell Name	SU CMOS GATE ARE	HAY UNII	CELLS	PECIFICA	ATION		" CG211	_	Number of BC
T2F	2:1 Selector								8
Cel	l Symbol	I		Pro	pagation D	elay Paran	neter		1
			IP KCL	40		dn KCL2	0000		Path
		0.284	0.060	t 0 0.284	KCL 0.045	0.062	CDR2	_	,B,C,D to X
		0.865	0.060	0.858	0.045	0.062	4	ı ^	S to X
A1 ————————————————————————————————————	D—— X0 D—— X1 D—— X2 D—— X3								
	**************************************	Paramete	er		l	<u> </u>	l Symbol		Typ (ns) *
Pin Name	Input Loading Factor (lu)								
A,B,C,D S	2 1								
Pin Name	Output Driving Factor (Iu)								
x	18						given by th	e ma	aximum delay
C21 T25 50	Shoot 1/2								
C21-T2F-E0	Sheet 1/2	·						Т	Page 20-19
								L	1 aye 20-19

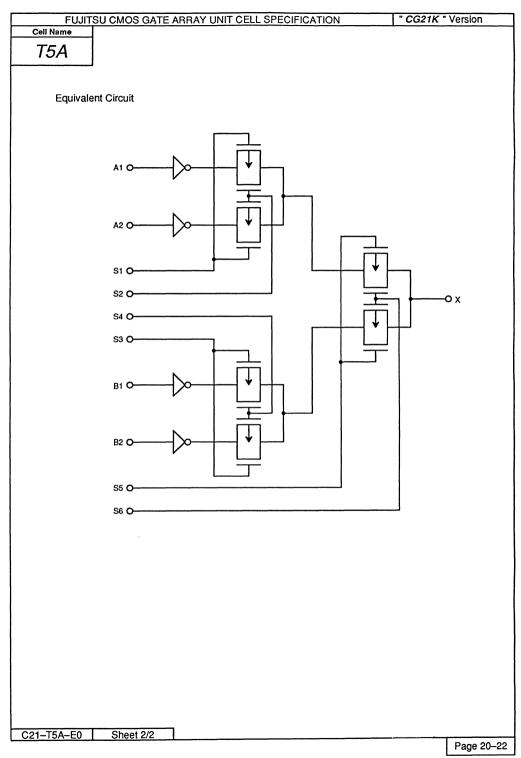


FUJI	TSU CMOS GATE AR	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of E
T5A	4:1 Selector							5
Ce	II Symbol			Pro	pagation De	elay Parar	neter	
		tı	ıρ		td			Path
		t O	KCL	t 0	KCL	KCL2	CDR2	
A1 ————————————————————————————————————	S2 S3 S4	0.528 0.528 0.297	0.087 0.087 0.087	0.528 0.442 0.284	0.073 0.073 0.073			A,B to X S1~4 to X S5~6 to X
\$5	30	Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)					1		
A,B S	1 1							
Pin Name	Output Driving Factor (lu)	]						
X	9		ues for the		operating o		e given by the	e maximum delay

				Inp	uts					Output
A1	A2	B1	B2	S1	S2	S3	S4	S5	S6	Х
L H	LH	L H	L H	LLHH	H H L L	ココエエ	X		IIIIII	H L H L H L

A1 $\neq$ A2 to S1=S2 or S5=S6 Inhibit B1 $\neq$ B2 to S3=S4 or S5=S6 Inhibit A1,A2 $\neq$ B1,B2 or S5=S6 Inhibit

C21-	-T5A-I	=n i	Sheet 1/2



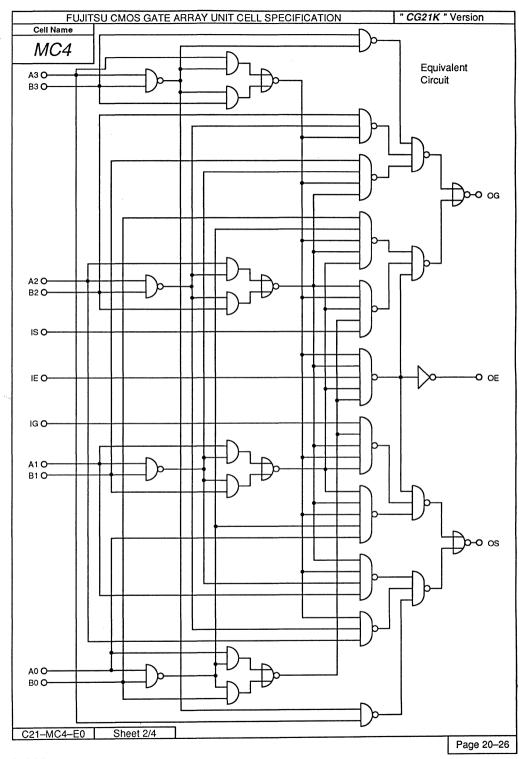
	FUJIT	SU CM	OS GA	TE ARI	RAY UNIT	CELL S	PECIFICA	ATION		" CG21	K"Ve	ersion
Cell Nam			nction									Number of BC
V3A	<u> </u>	1:2	Sele	ctor								2
	Cell	Symbol					Pro	pagation D		neter		
					t O	JP KCL	t O	KCL	In KCL2	CDR2		Path
					0.330 0.291	0.069 0.069	0.370 0.238	0.056 0.056				A to X S to X
					0.23	0.000	0.200	0.000				3 to 7.
Α	$\neg \Box$		x	0								
S1 —	-d											
S2	_	6	x	1								
	L											
		1		I	Paramete	er				Symbol	<u> </u>	Typ (ns) *
Pin Nam	e		ut Load actor (li									
A S			1									
Di- No-			out Load		-							
	Pin Name Factor (Iu)											
.,	×   '											
Pin Nam	е		put Driv actor (le		* Minimu	m values fo	r the typical	operating of	condition		<u> </u>	
x			14		The val	ues for the	worst case	operating o	ondition ar	e given by th	he max	imum delay
Functi	on Tal	ole			Equivalent Circuit							
	Inpu	te .	Out	puts				_				
A	S1	S2	XO	X1					1			
	L	L	<b></b>	nibit					_  ↓		<b>)</b> X0	
	H	1		Н								
	<u>                                    </u>	<u>-</u>   H	Н	X		A O-	<del>- </del> >	1	上			
L	Н	Н						Ц	$\Box$	<u> </u>	) X1	
Н	L	L	Int	nibit								
Н	Н	L	х	L	\$1 O							
Н	L	Н	L	Х		·	•					
Н	Н	Н	Inh	nibit								
		1										
C21-V3A	-E0	She	et 1/1			,						
											L	Page 20-23

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version											K " Version		
	Cell Na			Function				Number of BC					
	V3B Dual 1 : 2 Select							4					
Cell Symbol							Pro	pagation D	elay Paran In	neter			
					t O	KCL	CDR2	Path					
	A — — X0					0.337     0.069     0.403     0.056       0.304     0.069     0.258     0.056					A,B to X S to X		
	B —										Typ (ns) *		
			Ī	nput Loading	Paramete	Parameter Symbol							
	Pin Name Factor (Iu)  A 1												
	B S			1 2									
	Outpu Pin Name Fac			utput Loading Factor (lu)									
	X			1									
	Pin Name X			Output Driving Factor (Iu) 14	The val	Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the maximum delay multiplier.							
Function Table							Equiva	alent Circ	uit				
l		Inputs		Outp	outs	]			.   [	IJ			
	A,B	S1	S2	X0, X2	X1, X3				—-О ХО				
	L	L	L	Inh	ibit	A 0							
	L	Н	L	Х	Н	_				<b>+</b>  - -	O X1		
	L	L	Н	Н	X					<del> </del>			
	L H H Inhibit			bit						O X2			
										—~ ^2			
	Н	Н	L	X	L		ВО			丰十			
H L H L				X	_					——О хз			
	Н	Н	Н	Inh	ibit	S1 O							
							S2 <b>O</b> -		-				
C2	1-V3	B-E0	[ 5	Sheet 1/1									
Page 20–24													

FUJIT	SU CMOS GATE AR			" CG21F	" Version					
Cell Name	Function								Number of B	
MC4	4-bit Magnitude	e Compa	Comparator						42	
Cel	Symbol		Propagation Delay Parameter							
		tup tdn							Path	
		t O	KCL	t 0	KCL	KCL		CDR2		
		2.792	0.106	3.340	0.039	0.05	1	4	A to OS	
		2.845	0.106	3.280	0.039	0.05		4	B to OS	
		1.248	0.106	1.472	0.039	0.05		4	IE to OS	
A3_B3		1.023	0.106	1.274	0.039	0.05	1	4 4	IG to OS A to OG	
Λ2 <sup>B2</sup>	İ	2.739	0.106 0.106	3.452 3.393	0.039 0.039	0.05		4 4	B to OG	
A1 B1		1.188	0.106	1.578	0.039	0.05		4	IE to OG	
AO BO		1.129	0.106	1.221	0.039	0.0		4	IS to OG	
1		3.003	0.060	2.304	0.039	0.05		4	A to OE	
IG ——	og	2.950	0.060	2.350	0.039	0.05	1	4	B to OE	
IE OE		1.129	0.060	0.759	0.039	0.05	1	4	IE to OE	
ıs <del></del>	os os									
L.										
	Parameter						ymbol	Typ (ns) *		
	Input Loading	1								
Pin Name	Factor (lu)	4				l				
Α	3									
В	3	!								
IE IG	1					ı		İ		
IG IS	1									
13	'									
	Output Driving	7								
Pin Name	Factor (lu)	_								
OE	18	<u></u>								
OG	10	* Minimum values for the typical operating condition.								
os	10	The values for the worst case operating condition are given by the maximum delay								
		multiplie	er.							

	Compari	ng Inputs		Cas	cading In	puts	Outputs			
A3, B3	A2, B2	A1, B1	A0, B0	IG (A>B)	IS (A <b)< td=""><td>IE (A=B)</td><td>OG (A&gt;B)</td><td>OS (A<b)< td=""><td>OE (A=B)</td></b)<></td></b)<>	IE (A=B)	OG (A>B)	OS (A <b)< td=""><td>OE (A=B)</td></b)<>	OE (A=B)	
A3>B3 A3 <b3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3</b3 	X X X A2>B2 A2 <b2 A2=B2 A2=B2 A2=B2 A2=B2 A2=B2 A2=B2 A2=B2 A2=B2</b2 	X X X X A1>B1 A1=B1 A1=B1 A1=B1 A1=B1 A1=B1	X X X X X X A0>B0 A0=B0 A0=B0 A0=B0 A0=B0 A0=B0	X X X X X X X H L	X X X X X X X L H	X X X X X X H L	. H L H L H L L H L L H			

C21-MC4-E0 Sheet 1/2

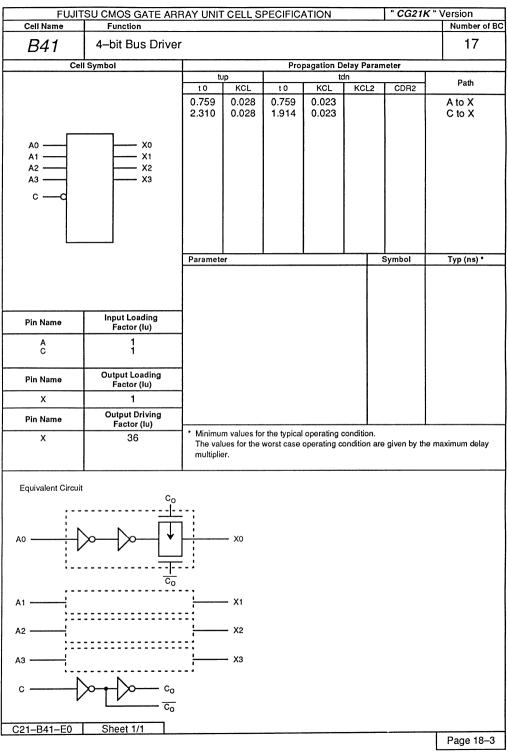


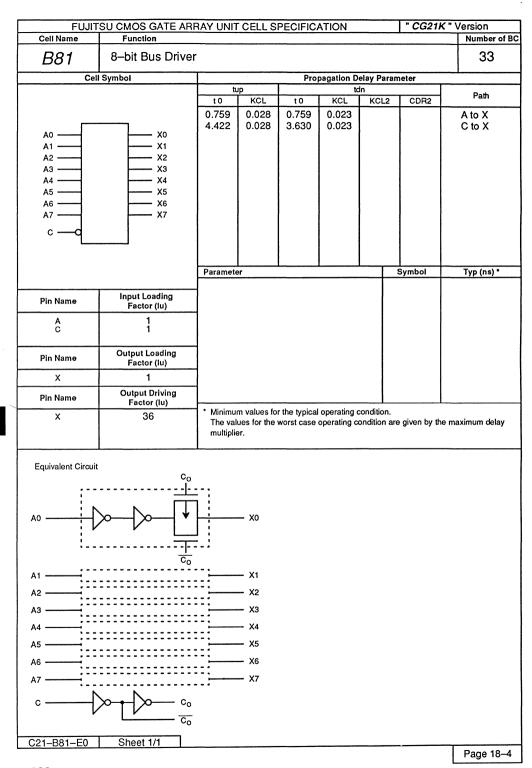
## **Bus Driver Family**

Page	Unit Cell Name	Function	Basic Cells
rage	Name	Tanction	Cella
3–319	B11	1-bit Bus Driver	5
3–320	B21	2-bit Bus Driver	9
3–321	B41	4-bit Bus Driver	17
3–322	B81	8-bit Bus Driver	33
3-323	B12	1-bit Block Bus Driver	7
3–324	B22	2-bit Block Bus Driver	13
3-325	B42	4-bit Block Bus Driver	25

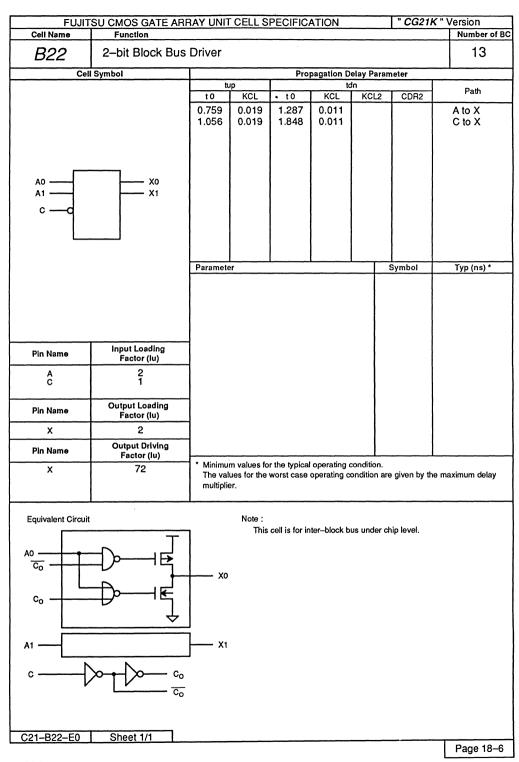
FILLET	CU CHOC CATE ADD	AV LINUT	OFIL O	DEOLEIO.	ATION		" CC244	(" Version
Cell Name	SU CMOS GATE ARF	TAT UNIT	CELL S	PECIFICA	ATION		CG21K	Number of BC
B11	1-bit Bus Driver							5
Cell	Symbol			Proj	pagation D		eter	
		t O	KCL	t O	KCL to	ln KCL2	CDR2	Path
A0 ————————————————————————————————————	хо	0.759 0.858	0.028 0.028	0.759 0.858	0.023 0.023			A to X C to X
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)						ĺ	
A C	1							
Pin Name	Output Loading Factor (lu)					-		
×	1					İ		
Pin Name	Output Driving Factor (lu)							
х	36	* Minimur The value multiplie	ues for the	the typical worst case	operating o	condition. condition are	given by the	e maximum delay
Equivalent Circuit	c <sub>o</sub>							
A0	$\longrightarrow$ $\longrightarrow$ $\bigcirc$ $\bigcirc$ $\bigcirc$ $\bigcirc$ $\bigcirc$ $\bigcirc$ $\bigcirc$ $\bigcirc$ $\bigcirc$ $\bigcirc$		— xo					
c ———	c <sub>o</sub>							
C21-B11-E0	Sheet 1/1		·····					Page 18–1

CI III	SU CMOS GATE ARF	DAV LINIT	CELLS	PECIFIC	ATION		" CG21K	' Version		
Cell Name	Function	IAT UNII	OLLL 3	LOIFICA	TION		UGZIK	Number of BC		
B21	2-bit Bus Driver							9		
Cel	l Symbol		neter	1						
		t O	IP KCL	t O	KCL	n KCL2	CDR2	Path		
		0.759	0.028	0.759	0.023	ROLZ	CDRZ	A to X		
		1.419	0.028	1.254	0.023			C to X		
l —										
A0	X0 X1									
c —d										
1 0 9										
		Paramete	l er	l	1	L	Symbol	Typ (ns) *		
1										
	Input Loading									
Pin Name	Factor (lu)									
A C	1									
C	1									
Pin Name	Output Loading									
	Factor (lu)									
X	1									
Pin Name	Output Driving Factor (lu)									
×	36	* Minimu	m values fo	r the typical worst case	operating o	condition. andition are	aiven by the	maximum delay		
		multiplie		WOISt Case	operating o	orianion are	givein by the	maximum colay		
Equivalent Circuit										
	c <sub>o</sub>									
:		-:								
Αο	<u>~_</u> \ <u>~</u> _ ↓	1	— X0							
~			,,,							
:		- :								
	$\frac{1}{C_0}$									
A1 ———— X1										
"	······································									
0	>									
	<u>c₀</u>									
	-0									
C21-B21-E0	Sheet 1/1							Dent 40.0		
								Page 18-2		





FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version										
Cell Name	Function	., (1 OINII	VLLE OI					Number of BC		
B12	1-bit Block Bus	Driver						7		
Cel	l Symbol			Pro	pagation D		neter			
		t O	IP KCL	t O	KCL	fn KCL2	CDR2	Path		
A0	—— хо	0.759 0.957	0.019 0.019	1.287 1.617	0.011 0.011			A to X C to X		
		Paramete	er				Symbol	Typ (ns) *		
Pin Name	Input Loading Factor (lu)									
A C	2 1									
Pin Name	Output Loading Factor (lu)									
X	2									
Pin Name	Output Driving Factor (lu)						l			
X	72	The val	ues for the	r the typical worst case	operating o	condition. ondition are	given by the	e maximum delay		
Equivalent Circuit  Note:  This cell is for inter-block bus under chip level.  Co  Co  Co  Co  Co  Co  Co  Co  Co  C										
C21-B12-E0	Sheet 1/1							Page 18–5		



FILIT	SU CMOS GATE ARF	TIMILVAC	CELLS	DECIFIC	ATION		" CG21K	(" Version
Cell Name	Function Function	IAT OINT	VLLL 3	LOIFIO	TION		00218	Number of BC
B42	4-bit Block Bus	Driver						25
Cel	Symbol	<b></b>		Pro	pagation D		eter	
		t 0	KCL	t O	KCL	in KCL2	CDR2	Path
A0	xo	0.759 1.320	0.019 0.019	1.287 2.046	0.011 0.011		93.12	A to X C to X
A1 ————————————————————————————————————	X1 X2 X3	Paramete	<b>2</b> F				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A C	2							
Pin Name	Output Loading Factor (lu)							
X	2 Output Driving							
Pin Name X	Factor (Iu) 72		ues for the	r the typical worst case			given by the	e maximum delay
Equivalent Circuit  A0  Co		xo	Note : This	cell is for in	ter-block b	us under ch	iip level.	
c <sub>o</sub>								
A1 ——		X1						
A2	X2							
c	$c_o \over c_o$	хз						
C21-B42-E0	Sheet 1/1							Page 18-7
								1 496 10 17

## **Clip Cell Family**

Page	Unit Cel Name	I	Function	Basic Cells
3-329	Z00	0 Clip		0
3-330	Z01	1 Clip		0

FULIIT	SU CMOS GATE ARE	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K									
Cell Name	Function	0.111	32220					Number of BC			
<i>Z</i> 00	0 Clip							0			
Cell	Symbol			Prop	pagation D		neter				
		t O	KCL	t O	KCL to	in KCL2	CDR2	Path			
2	×										
		Paramete	er				Symbol	Typ (ns) *			
	Input Loading										
Pin Name	Factor (lu)					1					
Pin Name X	Output Driving Factor (lu) 200	* Minimu	an value fo	a sho shuring							
		The val		r the typical worst case (	operating o	ondition ar	e given by the	maximum delay			
C21-Z00-E0	Sheet 1/1							Page 19–1			
								raye 19-1			

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	K " V	/ersion
Cell Name	Function								Number of BC
Z01	1 Clip								0
Cel	l Symbol			Prop	pagation D		neter		
		t O	KCL	t O	KCL	in KCL2	0000		Path
7	V x		KOL	20	NOL	ROLE	CDR2		
	^								
		Paramete	er				Symbol		Typ (ns) *
	·								
Pin Name	Input Loading Factor (lu)							1	
Pin Name X	Output Driving Factor (lu) 200								
		* Minimu The val multiplie	ues for the	r the typical worst case	operating o	condition. ondition are	e given by th	ne ma	ximum delay
C21-Z01-E0	Sheet 1/1								Page 19–2
									Page 10_2

## I/O Buffer Family

Page	Unit Cell Name	Function	Basic Cells
3-335	I1B	Input Buffer (Inverter)	5
3-336	I1BU	I1B with Pull-up Resistance	5
3-337	I1BD	I1B with Pull-down Resistance	5
3-338	I2B	Input Buffer (True)	4
3-339	I2BU	I2B with Pull-up Resistance	4
3-340	I2BD	I2B with Pull-down Resistance	4
3-341	IKB	Clock Input Buffer (Inverter)	4
3–342	IKBU	IKB with Pull-up Resistance	4
3–343	IKBD	IKB with Pull-down Resistance	4
3–444	IKC	CMOS Interface Clock Input Buffer (Inverter)	4
3–445	IKCU	IKC with Pull-up Resistance	4
3-446	IKCD	IKC with Pull-down Resistance	4
3–347	ILB	Clock Input Buffer (True)	8
3-348	ILBU	ILB with Pull-up Resistance	8
3-349	ILBD	ILB with Pull-down Resistance	8
3-350	ILC	CMOS Interface Clock Input Buffer (True)	6
3-351	ILCU	ILC with Pull-up Resistance	6
3-352	ILCD	ILC with Pull-down Resistance	6 5 5 5
3-353	I1C	CMOS Interface Input Buffer (Inverter)	5
3–354 3–355	I1CU I1CD	I1C with Pull-up Resistance I1C with Pull-down Resistance	5
3–356	12C	CMOS Interface Input Buffer (True)	4
3–356	I2CU	I2C with Pull-up Resistance	4
3–358	12CD	I2C with Pull-down Resistance	4
3–359	120D	Schmitt Trigger Input Buffer (CMOS Type, Inverter)	8
3–360	IISU	I1S with Pull-up Resistance	8
3–361	11SD	I1S with Pull-down Resistance	8
3–362	125	Schmitt Trigger Input Buffer (CMOS Type, True)	8
3-363	12SU	I2S with Pull-up Resistance	8
3–364	I2SD	I2S with Pull-down Resistance	8
3–365	I1R	Schmitt Trigger Input Buffer (TTL Type, Inverter)	8
3–366	I1RU	I1R with Pull-up Resistance	8
3–367	I1RD	I1R with Pull-down Resistance	8
3–368	I2R	Schmitt Trigger Input Buffer (TTL Type, True)	8
3-369	I2RU	I2R with Pull-up Resistance	8
3-370	I2RD	I2R with Pull-down Resistance	8
3-371	O1B <sup>1</sup>	Output Buffer (Inverter)	3
3-372	O1BF <sup>2</sup>	Output Buffer (Inverter)	3
3-373	O1L <sup>3</sup>	Power Output Buffer (Inverter)	3
3-374	O1R <sup>1</sup>	Output Buffer (Inverter) with Noise Limit Resistance	5
3–375	O1RF <sup>2</sup>	Output Buffer (Inverter) with Noise Limit Resistance	5
3–376	O1S <sup>3</sup>	Power Output Buffer (Inverter) with Noise Limit	
		Resistance	5
3–377	O2B <sup>1</sup>	Output Buffer (True)	3 3 3
3–378	O2BF <sup>2</sup>	Output Buffer	3
3–379	O2L <sup>3</sup>	Power Output Buffer (True)	
3–380	02R1	Output Buffer (True) with Noise Limit Resistance	4
3–381	O2RF <sup>2</sup>	Output Buffer with Noise Limit Resistance	4
1.	$I_{OL} = 3.2 \text{ mA}$		
2.	$I_{OL} = 8 \text{ mA}$		
3.	$I_{OL} = 12 \text{ mA}$		

## I/O Buffer Family (Continued)

Page	Unit Cell Name	Function	Basic Cells
3-382	O2S <sup>3</sup>	Power Output Buffer (True) with Noise Limit Resistance	4
3-383	O4T <sup>1</sup>	3-state Output Buffer (True)	6
3-384	O4TF <sup>2</sup>	3-state Output Buffer (True)	6
3-385	O4W <sup>3</sup>	Power 3-state Output Buffer (True)	6
3-386	O4R <sup>1</sup>	3-state Output Buffer (True) with Noise Limit	
		Resistance	5
3–387	O4RF <sup>2</sup>	3-state Output Buffer (True) with Noise Limit Resistance	5
3–388	O4S <sup>3</sup>	Power 3-state Output Buffer (True) with Noise Limit Resistance	5
3-389	H6T <sup>1</sup>	3-state Output and Input Buffer (True)	8
3–390	H6TU	H6T with Pull-up Resistance	8
3–391	H6TD <sup>1</sup>	H6T with Pull-down Resistance	8
3–392	H6TF <sup>2</sup>	3-state Output and Input Buffer (True)	8
3–393	H6TFU <sup>2</sup>	H6TF with Pull-up Resistance	8
3–394	H6TFD <sup>2</sup>	H6TF with Pull-down Resistance	8
3–395	H6W <sup>3</sup>	Power 3-state Output and Input Buffer (True)	8
3–396	H6WU <sup>3</sup>	H6W with Pull-up Resistance	8
3–397	H6WD3	H6W with Pull-down Resistance	8
3–398	H6C <sup>1</sup>	3-state Output and CMOS Interface Input Buffer	o
0 000	1100	(True)	8
3-399	H6CU1	H6C with Pull-up Resistance	8
3–400	H6CD1	H6C with Pull-down Resistance	8
3-401	H6CF <sup>2</sup>	3-state Output and CMOS Interface Input Buffer	8
3-402	H6CFU <sup>2</sup>	H6CF with Pull-up Resistance	8
3-403	H6CFD <sup>2</sup>	H6CF with Pull-down Resistance	8
3-404	H6E <sup>3</sup>	Power 3-state Output and CMOS Interface Input	0
0-404	TIOL	Buffer (True)	8
3-405	H6EU <sup>3</sup>	H6E with Pull-up Resistance	8
3-406	H6ED3	H6E with Pull-down Resistance	8
3-407	H6S <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer	Ü
0 407	1100	(CMOS Type, True)	12
3-408	H6SU <sup>1</sup>	H6S with Pull-up Resistance	12
3-409	H6SD1	H6S with Pull-down Resistance	12
3-410	H6R <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer	12
0 4.0	11011	(TTL Type, True)	12
3-411	H6RU <sup>1</sup>	H6R with Pull-up Resistance	12
3-412	H6RD1	H6R with Pull-down Resistance	12
3-413	H8T1	3-state Output with Noise Limit Resistance and	12
0 410	1.01	Input Buffer (True)	9
3-414	H8TU <sup>1</sup>	H8T with Pull-up Resistance	9
3-415	H8TD1	H8T with Pull-down Resistance	9
3-416	H8TF <sup>2</sup>	3-state Output with Noise Limit Resistance	3
0 410	11011	and Input Buffer True)	9
3-417	H8TFU <sup>2</sup>	H8TF with Pull-up Resistance	9
3–418	H8TFD <sup>2</sup>	H8TF with Pull-down Resistance	9
3-419	H8W <sup>3</sup>	Power 3-state Output with Noise Limit Resistance and	3
0 410		Input Buffer (True)	9
1. lo	= 3.2 mA		
	= 8 mA		
	= 12 mA		
O.	-		

## I/O Buffer Family (Continued)

Page	Unit Cell Name	Function	Basic Cells
3-420	H8WU <sup>3</sup>	H8W with Pull-up Resistance	9
3-421	H8WD <sup>3</sup>	H8W with Pull-down Resistance	9
3-422	H8C <sup>1</sup>	3-state Output Buffer with Noise Limit Resistance	
		and CMOS Interface Input Buffer (True)	9
3-423	H8CU <sup>1</sup>	H8C with Pull-up Resistance	9 9
3–424	H8CD <sup>1</sup>	H8C with Pull-down Resistance	9
3–425	H8CF <sup>2</sup>	3-state Output Buffer with Noise Limit Resistance	
	_	and CMOS Interface Input Buffer (True)	9
3–426	H8CFU <sup>2</sup>	H8CF with Pull-up Resistance	9
3–427	H8CFD <sup>2</sup>	H8CF with Pull-down Resistance	9
3–428	H8E <sup>3</sup>	Power 3-state Output Buffer with Noise Limit	
		Resistance and CMOS Interface Input Buffer (True)	9
3-429	H8EU <sup>3</sup>	H8E with Pull-up Resistance	9 9
3–430	H8ED <sup>3</sup>	H8E with Pull-down Resistance	9
3–431	H8S <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer	
		(CMOS Type, True) with Noise Limit Resistance	13
3–432	H8SU <sup>1</sup>	H8S with Pull-up Resistance	13
3–433	H8SD <sup>1</sup>	H8S with Pull-down Resistance	13
3–434	H8R <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer	
		(TTL Type, True) with Noise Limit Resistance	13
3–435	H8RU <sup>1</sup>	H8R with Pull-up Resistance	13
3–436	H8RD <sup>1</sup>	H8R with Pull-down Resistance	13
1. 2. 3.	I <sub>OL</sub> = 3.2 mA I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 12 mA		

FILIIT	SH CMOS GATE ARE	ARRAY UNIT CELL SPECIFICATION " CG21K" \							
Cell Name	Function	INT OINT	OLLLO	LOII 107	111011		OGZII	Number of BC	
I1B	Input Buffer (Inv	erter)						5	
Cel	Symbol			Pro		elay Param	eter		
		t O	IP KCL	t O	KCL	n KCL2	CDR2	Path	
x[	>o— in	0.845	0.014	0.812	0.017	NOLZ	COME	X to IN	
		Paramete	r				Symbol	Typ (ns) *	
Pin Name	Input Loading Factor (lu)					1	1		
Pin Name	Output Driving Factor (lu)								
IN	36	* Minimui The vali multiplie		the typical worst case	operating o	condition. ondition are	given by the	maximum delay	
COL MD FO	Sheet 1/1								
C21-I1B-E0	SHEEL I/I							Page 21-1	

FILIIT	SU CMOS GATE ARE	RAY LINIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function	1711 OI111	OLLL O	LOII 107	111011		002	Number of BC
	Input Buffer (Inv	verter)						
I1BU	with Pull-up Res	sistance	•					5
Cell	Symbol			Pro	pagation D	elay Param	neter	
		tı	ıp		to	ln		Dath
		t O	KCL	t O	KCL	KCL2	CDR2	Path
		0.845	0.014	0.812	0.017			X to IN
1							j j	
	_						l 1	
x —	>> <u></u> IN							
							i i	
	:	Paramete			L	٠ .	Symbol	Typ (ns) *
			-				7	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
1							- 1	
							l	
							ŀ	
		İ				1	ŀ	
Pin Name	Input Loading Factor (lu)							
T III TABILIO	7 40.01 (10)							
						- 1	[	
							Ì	
							1	
	Output Driving							
Pin Name	Factor (lu)							
IN	36						<u>l</u> .	
		* Minimu	m values for	r the typical	operating of	condition.	aivon hu tho	maximum delay
	:	multiplie		WOISI Case	operating o	ondition are	given by the	maximum oelay
1								
1								
1								
1								
1								
1								
l								
C21-I1BU-E0	Sheet 1/1							
								Page 21-2

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL SI	PECIFICA	ATION		" CG21F	( " Version
Cell Name	Function							Number of BC
I1BD	Input Buffer (Inv	/erter)						5
	with Pull-down I	Resistar	nce					
Cell	l Symbol			Pro	pagation D		neter	
		t O	IP KCL	t O	KCL	n KCL2	CDR2	Path
		0.845	0.014	0.812	0.017	KOLL	OBINE	X to IN
		0.043	0.014	0.012	0.017			7.10
1	<u> </u>							
×—	>→ IN							
-			,					
							1	
		Paramete	-r				Symbol	Typ (ns) *
		Turumote	<u>"</u>				,	.,,, (,
						- 1		
						İ		
	Input Loading							
Pin Name	Factor (lu)					- 1		
						İ		
						1		
	Output Driving							
Pin Name	Factor (lu)							
IN	36							
114	00	* Minimur	m values for	the typical	operating o	ondition.		
		The value multiplie		worst case	operating o	ondition are	given by the	e maximum delay
		manaphe						
C21-I1BD-E0	Sheet 1/1							Page 21–3

	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFIC.	ATION		" CG21	K " V	'ersion
Cell Name	Function								Number of BC
I2B	Input Buffer (Tr	ue)							4
Cel	l Symbol			Pro	pagation D		neter		
			JD			in	r		Path
		t 0	KCL	t0	KCL	KCL2	CDR2	<u> </u>	
		0.561	0.014	0.970	0.017			1	X to IN
			1			}	1	1	
							l		
								İ	
							İ		
							İ		
x	>— IN							1	
				2			ŀ		
							İ	l	
							İ		
,		Paramete	er			_	Symbol	<u> </u>	Typ (ns) *
		l				1		1	
						l		l	
								İ	
								i	
	Input Loading	ł							
Pin Name	Factor (lu)							l	
		1						1	
								1	
	,							l	
	Output Driving	1						l	
Pin Name	Factor (lu)	1						1	
IN	36	• 14:-:		- 41 - 4 - 1 - 1				L	
		The val	m values fo	r the typical worst case	operating o	condition. ondition ar	e given by th	ne ma	ximum delay
		multiplie							•
	<u> </u>	<u></u>							
C21-l2B-E0	Sheet 1/1								
UZ 1-12B-EU	SHEEL I/I							Т	Page 21-4

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
I2BU	Input Buffer (Tru	ne)						4
	with Pull-pu Res	sistance						
Cell	Symbol	*1	ıp	Proj	pagation D	elay Parai In	neter	
		t O	KCL	t O	KCL "	KCL2	CDR2	Path
		0.561	0.014	0.970	0.017			X to IN
							1	
				· ·			1 1	
					İ			
x	IN							
L								
							1	
							1	
		Paramete	er				Symbol	Typ (ns) *
						ł	İ	
							İ	
	Input Loading						l	
Pin Name	Factor (Iu)							
	0.4.1011							
Pin Name	Output Driving Factor (Iu)							
IN	36							
	00	* Minimu	m values fo	r the typical	operating o	condition.		
	,	The val		worst case	operating o	ondition ar	e given by the	maximum delay
		шопри	···					
C21-I2BU-E0	Sheet 1/1							
								Page 21-5

	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFIC/	ATION		" CG211	K " \	
Cell Name	Function								Number of BC
IODD	Input Buffer (Tri	ne)							4
I2BD	with Pull-down I	Resistar	nce					ı	4
	Symbol			Pro	pagation D	elav Par	ameter	1	
Cen	. 07.11001	ħ	ıp	I		in		Γ	
		t O	KCL	t O	KCL	KCL2	CDR2		Path
		0.561	0.014	0.970	0.017			<del>                                     </del>	X to IN
	i	0.501	0.014	0.970	0.017		1	1	X to iii
								ł	
1								l	
								1	
_									
x	>— IN							l	
L					•			1	
								l	
								l	
		Paramete	er				Symbol		Typ (ns) *
			_						
								1	
						1		1	
								1	
Dia Massa	Input Loading							1	
Pin Name	Factor (lu)								
						ļ		1	
						1		l	
								l	
	Output Datata							1	
Pin Name	Output Driving Factor (lu)					- 1		1	
IN	36							Ь	
		* Minimu	m values fo	r the typical	operating o	condition.	are given by th	na ma	vimum dolav
		ne vai multiplie		worst case	operating c	J. 10111011 8	are given by tr	ie ma	Annum delay
		monuplie	<b>-1.</b>						
		L							
004 1055 55	Chart 4/4								
C21-I2BD-E0	Sheet 1/1							$\neg \tau$	Page 21 6
								- 1	Page 21–6

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	( " Version
Cell Name	Function							Number of BC
IKB	Clock Input Buffe	er (Inve	erter)					4
Cell	Symbol			Proj	pagation D		meter	
		t O	IP KCL	t O	KCL	ln KCL2	CDR2	Path
		1.540	0.004	1.020	0.004	KOLE	OBITE	X to CI
			0.00		0.00		1	
							1	
						i		
_								
× ——	<b>&gt;</b> 0— cı							
L							1	
		D			L	L	Sumb at	Tim (no) \$
		Paramete	<del>;</del> r				Symbol	Typ (ns) *
						- [		
						ŀ		
Pin Name	Input Loading Factor (lu)							
						- 1		
						- 1		
						l		
Pin Name	Output Driving Factor (lu)							
CI	200							
Ci	200	* Minimu	m values fo	r the typical	operating o	condition.		
		The val multiplie		worst case	operating o	ondition ar	e given by th	e maximum delay
C21-IKB-E0	Sheet 1/1							
<u></u>								Page 21-7

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	K " Version
Cell Name	Function							Number of BC
IKBU	Clock Input Buff with Pull-up Res	er (Inve sistance	erter)					4
Cel	Symbol			Pro	pagation D		neter	
			ıp			dn KOLO	1 0000	Path
		1.540	KCL	t 0	KCL	KCL2	CDR2	X to CI
		1.540	0.004	1.020	0.004			X 10 C1
	_							
	<b>O</b> CI		1					
		Paramete	er	L	L	<u> </u>	Symbol	Typ (ns) *
						l		
		l						
		l						
		ł				1		
Pin Name	Input Loading Factor (lu)					ļ		
		1						
	Output Driving	]						
Pin Name	Factor (lu)					1		
CI	200	* Minimu	m values fo	r the typical	operating of	condition		
		The val	ues for the	worst case	operating o	ondition ar	e given by th	e maximum delay
		multiplie	er.					
	L	l						
COL INDIL EQ	Choot 1/1							
C21-IKBU-E0	Sheet 1/1							Page 21-8

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function	<del></del>					<u> </u>	Number of BC
IKBD	Clock Input Buffe with Pull-down I	er (Inve Resistar	erter) nce					4
Cel	l Symbol	T		Pro	pagation D	elay Paran	eter	····
		tu			to	ln		Path
		t O	KCL	t 0	KCL	KCL2	CDR2	
		1.540	0.004	1.020	0.004			X to CI
					1		1	
_							1	
x —	>> cı							
		Paramete		L	L	٠	Symbol	Typ (ns) *
		Turumoto					,	.,,, (,
Pin Name	Input Loading Factor (Iu)							
Pili Name	racior (iu)	1						
		[						
	Output Driving	ĺ						
Pin Name	Factor (lu)							
CI	200						1	
		* Minimu	m values fo	r the typical	operating o	condition.	airea bu the	e maximum delay
		multiplie		worst case	operating o	Jilulion are	given by the	maximum delay
		in one pine	···					
C21-IKBD-E0	Sheet 1/1							Page 21–9
								i Page 21-9

FUJIT	JITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K"								
Cell Name	Function								Number of BC
IKC	CMOS Interface	Clock I	nput Bu	ffer (Inv	erter)				4
Cel	l Symbol			Pro	pagation D	elay Para	meter		
		t O	IP KCL	t O	KCL to	In KCL2	CDR2		Path
		1.310	0.004	0.980	0.004		35.12		X to CI
								l	
۱ ۲									
	OI								
								İ	
		Paramete	er				Symbol		Typ (ns) *
						İ		İ	
Pin Name	Input Loading Factor (lu)								
7 III Hallie	1 40.01 (10)								
								İ	
Pin Name	Output Driving Factor (lu)								
CI	200								
0.		* Minimu	m values fo	r the typical	operating o	condition.	are given by th	m	vimum dolav
		multiplie		worst case	operating o	ondition a	are given by a	10 1116	ixiiiidiii delay
	L	<u> </u>							
C21-IKC-E0	Sheet 1/1								
L CZ I-INC-EU	SHEEL I/I							Т	Page 21-10

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function	.,	ULLE U			<del></del>		Number of BC
	CMOS Interface	Clock I	nput Bu	ffer (Inv	erter)			4
IKCU	with Pull-up Res	sistance		`	•			4
Cell	Symbol			Pro	pagation D	elay Param	neter	
			ıρ			ln		Path
		t 0	KCL	t O	KCL	KCL2	CDR2	
		1.310	0.004	0.980	0.004			X to CI
					l			
							1	
							ĺ	
×—	<b>&gt;</b> → cı				l			
					ļ .			j
		Paramete	er				Symbol	Typ (ns) *
	Input Loading						1	
Pin Name	Factor (lu)							
						- [		
	Output Driving							
Pin Name	Factor (lu)							
CI	200							
O.	200	* Minimu	m values for	r the typical	operating o	condition.		
				worst case	operating o	ondition are	given by the	maximum delay
		multiplie	er.					
	0114"							
C21-IKCU-E0	Sheet 1/1							T Bago 24 44
								Page 21-11

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Ve								/ersion	
Cell Name	Function	17 (1 0 (1)	OLLL O	2011 101	111011			Ť	Number of BC
	CMOS Interface	Clook I	nout Bu	ffor (Inv	ortor)				
IKCD	with Dull daws	Dociotor	nput bu	nei (iiiv	errer)			- 1	4
	with Pull-down	Resistar	ice						
Cell	Symbol			Proj	pagation D		neter		
			qı			in			Path
		t O	KCL	t O	KCL	KCL2	CDR2		
		1.310	0.004	0.980	0.004		1		X to CI
							1		
							1		
							1		
							<u> </u>		
					ĺ		1		
							1		
1	<b>\</b> .		1				1		
x —	>> cı								
							1		
							1		
							1		
		B	L		l	<b>L</b>	Cumbal		Tun (na) *
		Paramete	er				Symbol		Typ (ns) *
								İ	
						1			
	Input Loading								
Pin Name	Factor (lu)	l				1			
		1						ŀ	
		i						į	
		Į.							
						1		l	
	Output Driving	1				- [		l	
Pin Name	Factor (lu)								
CI	200	1							
CI	200	* Minimu	m values fo	r the typical	operating of	condition.			
		The val	ues for the	worst case	operating o	ondition ar	e given by th	ne ma	ximum delay
		multiplie					-		_
C21-IKCD-E0	Sheet 1/1								
OE1-IIIOD-LU	1 011000 1/1								Page 21-12

	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	K "∖	
Cell Name	Function							$\Box$	Number of BC
ILB	Clock Input Buffe	er (True	e)						8
Cell	Symbol			Pro	pagation D		neter		
		t O	KCL	t O	KCL	In KCL2	CDR2		Path
		0.560	0.004	1.330	0.004		- OBINE		X to CI
							1		
					1			l	
							j		
							}	l	
×—	CI CI								
L							l l	Ì	
							}		
		Paramete	er				Symbol		Typ (ns) *
								•	
								l	
						Ì			
Pin Name	Input Loading Factor (lu)								
Fill Name	ractor (lu)					- 1			
						1			
						1			
						- 1			
	Output Driving					- 1			
Pin Name	Factor (lu)					- [			
CI	200	* Minimu	m values fo	r the typical	operating of	condition.		L	
		The val	ues for the	worst case	operating o	ondition ar	e given by th	ne ma	ximum delay
		multiplie	er. 						
C21-ILB-E0	Sheet 1/1								
								- 1	Page 21-13

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG21F	K " V	'ersion
Cell Name	Function								Number of BC
II DU	Clock Input Buffe	er (True	9)						8
ILBU	with Pull-up Res	sistance	,						0
Cell	Symbol			Pro	pagation D	elav Para	meter	1	
	. 0,	tu	מו			in			
		t0	KCL	t O	KCL	KCL2	CDR2		Path
		0.560	0.004		0.004		100.11		X to CI
		0.560	0.004	1.330	0.004		1 1		X 10 C1
							1		
							į		
							1		
							1 1		
							1		
							1 1		
x	<b>&gt;</b> cı								
" L							1 1		
							1 1		
						}	1		
							1 1		
							1 1		
		Paramete	r				Symbol		Typ (ns) *
						1			
						i			
						- 1			
						1			
						- 1			
	Input Loading								
Pin Name	Factor (lu)					l			
						1			
						ı			
						ĺ		1	
						ļ		ŀ	
						1			
	Output Driving					- 1			
Pin Name	Factor (lu)					l			
CI	200							<u> </u>	
		* Minimu	n values fo	r the typical	operating of	condition.			
				worst case	operating o	ondition ar	e given by th	e ma	ximum delay
		multiplie	er.						
		L							
C21-ILBU-E0	Sheet 1/1								
021-1200-20	0.1001.1/1								Page 21-14

ELLITCH CMOS CATE ADDAY UNIT CELL SPECIFICATION 1" CG21K" Vorsi								V " Varaian	
FUJI I	UJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" V								
Cell Name	Function Clock Input Buffor (True)							Number of BC	
ILBD	Clock input Buff	Clock Input Buffer (True)							
	with Pull-down I	<b>Resistar</b>	nce				8		
Cell	Symbol			Pro	pagation D		meter		
			ıp			in		Path	
		t 0	KCL	t O	KCL	KCL2	CDR2		
		0.560	0.004	1.330	0.004		l	X to CI	
					ļ		l		
							1		
					i				
							J		
			į				l.		
1	<b>\</b>						1		
x	>— cı								
_					l				
							1		
		Paramete			<u> </u>	<u> </u>	Symbol	Typ (ne) *	
		Paramete	er				Symbol	Typ (ns) *	
						1			
						- 1			
						- 1			
						- 1			
	Input Loading								
Pin Name	Factor (lu)					]			
						1			
						]			
						1			
						ļ			
	Output Driving					-			
Pin Name	Factor (lu)					ı			
CI	200							L	
		* Minimu	n values for	r the typical	operating of	ondition.			
		The values for the worst case operating condition are given by the man							
		multiplie	er.						
004 11 55 52	Chaot 414								
C21-ILBD-E0	Sheet 1/1							Page 21-15	
								3-349	

FUJIT	ITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K"						/ersion		
Cell Name	Function							Number of BC	
ILC	CMOS Interface	Clock Input Buffer (True)							6
Cel	Symbol	Propagation Delay Parameter							<u> </u>
			ıp			in			Path
		t O	KCL	t 0	KCL	KCL2	CDR2	<u> </u>	
		0.880	0.004	1.550	0.004		1	l	X to CI
		1				ł	1		
					ļ	i			
								l	
l ,1	CI					l			
×	Cl				ļ	l			
		Danamata			<u> </u>		Symbol		Tum (m =) #
		Paramete	÷r				Symbol	-	Typ (ns) *
						1			
						l			
		Ì				į			
						j			
	Input Loading								
Pin Name	Factor (lu)					l			
						1			
						1			
	i					Ì			
	Output Driving								
Pin Name	Factor (lu)					1			
CI	200							L	
		* Minimu	m values fo	r the typical	operating o	condition.	o aivon hy th	o ma	vimum dalav
		The values for the worst case operating condition are given by the ma multiplier.							Millioni delay
		l							
C21-ILC-E0	Sheet 1/1								
UE I-ILU-LU	i Oncor I/I							T	Page 21-16

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							" CG21	K " Version		
Cell Name	Function Function							Number of BC		
	CMOS Interface	Clock I	nout Bu	ffer (Tri						
ILCU	with Pull-up Res	sistance	6							
	Symbol		Propagation Delay Parameter							
- Cen	-,	tu	ıp			in				
		t O	KCL	t O	KCL	KCL2	CDR2	Path		
		0.880	0.004	1.550	0.004			X to CI		
							· '			
							1			
							ł			
							i			
_							İ			
x—	cı						l			
^ L	<b>/</b>						1			
							1			
								l		
		Paramete	er				Symbol	Typ (ns) *		
								į		
						1				
	Input Loading									
Pin Name	Factor (lu)					j				
						l				
						ŀ				
						- 1				
						l				
	0.41.0.4.4					]				
Pin Name	Output Driving Factor (lu)									
CI	200	* Minimu	m values fo	r the tynical	onerating (	condition		·		
		<ul> <li>Minimum values for the typical operating condition.</li> <li>The values for the worst case operating condition are given by the maximum delay</li> </ul>								
	multiplier.									
	01									
C21-ILCU-E0	Sheet 1/1							Page 21–17		
								3-351		

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K" Ve							Version				
Cell Name	Function	THAT DIVIT CELE SPECIFICATION   COZIN V						Number of BC			
	CMOS Interface	Clock I	nnut Ru	ffor /Tr	(۵)						
ILCD		OIUUK I	nput bu	1101 (110	10)			6			
	with Pull-down I	nesistar	ice					l			
Cel	Symbol			Pro	pagation D						
		tı				dn			Path		
		t O	KCL	t O	KCL	KCL2	CDR2	<u> </u>			
		0.880	0.004	1.550	0.004	1			X to CI		
					1			1			
					1	<b>!</b>					
					1	l		1			
						1		1			
			i			1		ĺ			
_					1	1					
\ ×—-[	cı				l			l			
^ L					1	١		1			
								İ			
					1	1		1			
						1					
					<u> </u>			L			
		Paramete	r				Symbol		Typ (ns) *		
						1		1			
						-		l			
								1			
	Input Loading							l			
Pin Name	Factor (lu)							l			
								l			
						1					
						}					
	Output Driving							l			
Pin Name	Factor (lu)					1					
CI	200							L			
!		* Minimu	n values fo	r the typical	operating	condition.	ua alica e terror				
		The vali multiplie		worst case	operating c	ondition a	re given by th	ie ma	aximum delay		
		mulupile									
	L	L									
C21-ILCD-E0	Sheet 1/1							Т	Page 21–18		
									ころいき ノリーバ		

FUJIT	SU CMOS GATE ARE	CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" V						
Cell Name	Function							Number of BC
I1C	CMOS Interface	Input B	uffer (I	nverter)			5	
Cell	Symbol			Pro	pagation D		eter	
		tu	p KCL	t O	KCL	n KCL2	CDR2	Path
		t 0			0.017	NCL2	CDRZ	X to IN
		0.387	0.014	0.210	0.017			X 10 114
1								
x —	>> IN							
•								
		Paramete	er .			<del></del>	Symbol	Typ (ns) *
		,					,	
	r							
Pin Name	Input Loading Factor (lu)							
T III Maine	1 20101 (10)							
	Output Driving							
Pin Name	Factor (lu)							
IN	36	* Minimu	m valuas fai	r the tunical		L		
	<ul> <li>Minimum values for the typical operating condition.</li> <li>The values for the worst case operating condition are given by the ma</li> </ul>							e maximum delay
		multiplie	er.					
	L	L						
C21-I1C-E0	Sheet 1/1							
021-110-EU	SHEELI/I							

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFIC/	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
I1CU	CMOS Interface with Pull-up Res	Input B	uffer (Ir	rverter)				5
Cell	l Symbol			Proj	pagation D	elay Parai	neter	
			ıρ		to	In		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		0.387	0.014	0.210	0.017			X to IN
							1 1	
						ŀ	1	
						l		
						l		
							1 1	
_								
x —	>> cı							
L						l		
							1	
		Paramete		L	L	<u> </u>	Symbol	Typ (ns) *
							-,	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
							İ	
	Input Loading						-	
Pin Name	Factor (lu)							
-								
	Output Driving					1		
Pin Name	Factor (lu)					i		
IN	36							
	"	* Minimu	m values fo	r the typical	operating o	condition.		
				worst case	operating o	ondition ar	e given by the	maximum delay
		multiplie	er.					
	L							
C21-I1CU-E0	Sheet 1/1							
								Page 21-20

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFICA	ATION		П	" CG21K	("	Version
Cell Name	Function								_	Number of BC
I1CD	CMOS Interface with Pull-down	Input B Resista	uffer (I	nverter)						5
Cell	Symbol				pagation D	elay Pa	ram	eter		
			р		to	in				Path
		t O	KCL	t O	KCL	KCL	2	CDR2		
		0.387	0.014	0.210	0.017		l			X to IN
			·			]	Ì			
							- 1			
						•				
							- }	1		
J1	>> IN					l				
×—	IN IN						-			
						i				
							١			
						l	- 1			
		Paramete	:r			ЧТ	— <u>ե</u>	ymbol		Typ (ns) *
						一十		,	_	71.5.7
						j				
	Input Loading							į		
Pin Name	Factor (lu)									
		1								
Pin Name	Output Driving Factor (lu)									
IN	36	* Minimu	m values fo	r the typical	operating of	condition	n.			
		The val	ues for the	worst case	operating o	ondition	are	given by the	e m	aximum delay
		multiplie	er.							
		L								
C21-I1CD-E0	Sheet 1/1									
OZ I-ITOD-LU	Once I/I									Page 21-21
									L	-

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG211	K " Version
Cell Name	Function			Number of BC				
I2C	CMOS Interface	Input B	uffer (T	rue)				4
Cel	l Symbol			Pro	pagation D		meter	
			ip			in	T 0000	Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	X to IN
		0.489	0.014	0.706	0.017	İ		A 10 IN
						1		
۲ ا	_						ŗ	
x	N N						1	
			1					
		Paramete	L	L	L	L	Symbol	Typ (ns) *
		Faramete	71				Cymoor	1,75 (1.3)
						1		
						- 1		
Die Nesse	Input Loading	ĺ						
Pin Name	Factor (lu)							
						- 1		
						ŀ		
						1		
	Output Driving					1		İ
Pin Name	Factor (lu)	]				i		
IN	36	ļ						l
		* Minimu	m values fo	r the typical worst case	operating o	condition. ondition as	re aiven by th	ne maximum delay
		multiplie			oporag o		- g, -	,
	<u> </u>	L						
1								
C21-I2C-E0	Sheet 1/1							1 =
								Page 21-22

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K " Version		
Cell Name	Function								Number of BC
IOCII	CMOS Interface	Input B	uffer					$\Box$	4
I2CU	with Pull-up Res	sistance	(True)						4
Cell	Symbol		· · · · · · · · · · · · · · · · · · ·		pagation D	elay Paran	neter		
		tu		[		ln			Deth
		t O	KCL	t O	KCL	KCL2	CDR2	1	Path
		0.489	0.014	0.706	0.017				X to IN
								İ	
								ļ	
_								Ì	
×——	> IN							1	
^ L	<b>/</b> "'								
								İ	
								l	
					l			L	
		Paramete	r				Symbol		Typ (ns) *
								1	
								1	
								1	
	Input Loading							}	•
Pin Name	Factor (lu)							ŀ	
	· · · · · · · · · · · · · · · · · · ·							ļ	
						- 1		Ì	
Pin Name	Output Driving Factor (lu)								
								l	
IN	36	* Minimus	m valuas fai	r the tunical	operating of	L		L	
		The value	ues for the	worst case	operating o	ondition are	aiven by th	e max	imum delay
		multiplie					• ,		•
C21-I2CU-E0	Sheet 1/1	·					.,		
								L	Page 21-23
									3-357

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	( " Version	
Cell Name	Function							Number of	вс
I2CD	CMOS Interface with Pull-down f	Input B Resistar	uffer nce ( <b>7</b> rı	ne)				4	
Cel	Symbol			Pro	pagation D	elay Para	meter		
		tu				in		Path	
		t 0	KCL	t 0	KCL	KCL2	CDR2		
		0.489	0.014	0.706	0.017			X to IN	
					•				
_					į				
x	)—IN					l			
^ レ									
	•								
		Paramete	er		L	<b>—</b> ——	Symbol	Typ (ns) *	
								. , , , , , , , , , , , , , , , , , , ,	
						- 1			
						1			
						- 1			
	Input Loading								
Pin Name	Factor (lu)								
						1			
	Output Driving					l			
Pin Name	Factor (lu)					l			
IN	36								
		* Minimu	n values for	r the typical	operating o	condition.	re aiven hy th	e maximum delay	
		multiplie		WOIST 5000	operating o	J. 10111011 C	. o g o o ,	o maximum colay	
		<u> </u>							
C21-I2CD-E0	Sheet 1/1								
021-1200-LU	Once I/I							Page 21-2	4
								, -	

			. 0.51.1.0	0501510			T " 0004	< 11 \ / '		
FUJ Cell Name	Function	RAY UNII	RAY UNIT CELL SPECIFICATION " CG21K"							
I1S	Schmitt Trigger (CMOS Type, Ir	Input Bu	ıffer					Number of		
C	ell Symbol			Pro	pagation D	elay Par	ameter			
	-		ıρ			dn		Path		
		t 0	KCL	t 0	KCL	KCL2	CDR2			
		2.059	0.060	1.419	0.039			X to IN		
		1			1					
		İ								
x	<i>₽</i> >>− IN				ŀ					
					1					
						Ì				
		Paramete	er				Symbol	Typ (ns) *		
	1	-								
Pin Name	Input Loading Factor (lu)									
		1								
						- 1				
	Output Driving					1				
Pin Name	Factor (lu)									
IN	18									
		* Minimu The val	m values fo	r the typical worst case	operating o	condition andition	are given by th	e maximum delay	,	
		multiplie		WOIDE GUDG	operating o	0110111011	are given by a	a		
		<u> </u>								
004 40 50	Choot 4/4									
C21-I1S-E0	Sheet 1/1							Page 21-	25	

FILIT	SU CMOS GATE ARE	RAY LINIT	CELLS	PECIFICA	ATION		" CG21k	" Version
Cell Name	Function	1711 01111	OLLL O	LOII 107	111011		, our	Number of BC
	Schmitt Trigger	Input Bu	ıffer					
l1SU	Schmitt Trigger (CMOS Type, In	verter)	with Pull	l–up Re	sistance	Э		8
Cell	Symbol				pagation D		neter	
			JD			dn		Path
		10	KCL	t 0	KCL	KCL2	CDR2	
		2.059	0.060	1.419	0.039			X to IN
		l				1		
		1				i		
x	IN IN						<b>i</b>	
"								
		Paramete	!i			<u>'                                    </u>	Symbol	Typ (ns) *
						-		
		1						
		İ				1		
	Input Loading	1					1	,
Pin Name	Factor (lu)							
						1	i	
		1				l		
	Output Driving					ļ		
Pin Name	Factor (lu)	1						
IN	18							
			m values for				aiven by the	a maximum delay
		multiplie		Worst case	operating o	oridition are	, given by an	o maximum ociay
1								
C21-I1SU-E0	Sheet 1/1							
UZ1-113U-EU	Olicet I/I							Page 21-26

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		$\neg$	" CG21F	(")	Version
Cell Name	Function									Number of BC
I1SD	Schmitt Trigger I (CMOS Type, In	nput Bu verter) v	iffer with Pul	–down	Resista	nce				8
Cell	Symbol	<u> </u>		Proj	pagation D	elay Pa	rame	eter		L
		tı			to	n				Path
		t 0	KCL	t O	KCL	KCL	2	CDR2		
		2.059	0.060	1.419	0.039	İ	- 1			X to IN
						1	1			
						l	ł			
							- 1			
						l	1			
_						l	- 1			
x	<i>σ</i> >>ο— IN						- 1			
						ļ				
						<b>\$</b>	- 1			
						l				
		Paramete	L			<b>!</b> —т		ymbol		Typ (ns) *
		Paramete						yiiiboi		Typ (IIS)
						- 1				
						İ				
	PM									
Din Name	Input Loading Factor (lu)					İ				
Pin Name	ractor (Iu)					1				
						l				
						ļ				
						İ				
						l				
	Output Driving									
Pin Name	Factor (lu)					l				
IN	18									
		* Minimu	m values fo	the typical	operating o	condition	n.	-1		
		The val		worst case	operating o	ondition	are	given by th	e ma	aximum delay
		manuphe								
C21-I1SD-E0	Sheet 1/1									
									- 1	Page 21-27

	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFIC/	NOITA		" CG21	K " Version
Cell Name	Function							Number of BC
I2S	Schmitt Trigger I (CMOS Type, Tr	nput Bu ue)	iffer					8
Cell	Symbol			Proj	pagation D		ameter	
			lb KCI	••		in KCI 3	Longo	Path
		10	KCL	t 0	KCL 0.045	KCL2	CDR2	X to IN
		1.314	0.060	1.630	0.045			A 10 114
_								
x	IN							
						L		
		Paramete	er				Symbol	Typ (ns) *
	Input Loading							
Pin Name	Factor (lu)						4	
						1		
	Output Driving							
Pin Name	Factor (lu)							
IN	18	* Minimu	m values fo	r tha train-I	anoretice :			L
		The val	ues for the	worst case	operating o	ondition	are given by th	e maximum delay
		multiplie					- •	·
	l							
C21-I2S-E0	Sheet 1/1							
021-120-LU	1 011000 1/1							Page 21–28

	SU CMOS GATE ARF	RAY UNIT	CELL SI	PECIFICA	ATION		" CG211	K " Version
Cell Name	Function							Number of BC
I2SU	Schmitt Trigger I (CMOS Type, Tr	Input Burue) with	iffer 1 Pull–ui	o Resist	tance			8
Cell	Symbol			Pro	pagation D	elay Parar	neter	
		tu				ln KOLO	0000	Path
		t 0 1.314	KCL 0.060	t 0 1.630	KCL 0.045	KCL2	CDR2	X to IN
		1.314	0.000	1.030	0.045			710111
x	σ> IN							
^ 5								
		Paramete	r				Symbol	Typ (ns) *
							•	
Pin Name	Input Loading Factor (lu)							
riii Name	ractor (lu)							
						ļ		
	Output Driving							
Pin Name	Factor (lu)							
IN	18	* Minimur	m values for	the typical	operating of	ondition.		
		The val	ues for the v	worst case	operating o	onditión an	e given by th	e maximum delay
		multiplie	er.					
C21-I2SU-E0	Sheet 1/1							
UZ 1-123U-EU	OHEEL I/ I							Page 21-29

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFIC/	ATION		" CG21F	( " Version
Cell Name	Function							Number of BC
I2SD	Schmitt Trigger I	nput Bu	iffer	own D-	oiotono			8
	(CMOS Type, Tr	ue) witr	i Pull—a	own He	sistance	<del>,</del>		
Cel	Symbol			Proj	pagation D		ameter	
	2	t O	KCL	t O	KCL	in KCL2	CDR2	Path
		1.314	0.060	1.630	0.045			X to IN
					****			
x	IN							
			İ					
		Paramete	er				Symbol	Typ (ns) *
						- 1		
						- 1		
						ļ		
						- 1		
						j	}	
	Input Loading							
Pin Name	Factor (lu)					-		
						- 1		
	:					- 1		
						- 1		
	Output Driving					1		
Pin Name	Factor (lu)							
IN	18							
		* Minimu	m values to	r the typical	operating o	condition	are given by th	e maximum delay
		multiplie		WOISE CASC	operating o	01101110111	alo giron by an	o maximom colay
C21-I2SD-E0	Sheet 1/1							Deer 04 00
								Page 21-30

FILHT	SU CMOS GATE ARF	RAY LINIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function	,, ()(1)	JEEL OI					Number of BC
	Schmitt Trigger	Input Bu	ıffer					
I1R	(TTL Type, Inve	rter)						8
Cel	Symbol			Pro		elay Paran	neter	
		t O	IP KCL	t O	KCL	dn KCL2	CDR2	Path
		2.370	0.060	1.248	0.039	NOL2	CDR2	X to IN
		2.370	0.000	1.240	0.059			X 10 114
					İ	l		
	>						1	
\ \ \	D IN				l	}	<b>!</b>	
						l	i i	
							1	
		Paramete			l	L .	Symbol	Typ (ns) *
			·			<del>-  -</del>	,	-75 (3.6)
						1		
							ŀ	
	Input Loading							
Pin Name	Factor (lu)							
							İ	
	•							
	Output Driving							
Pin Name	Factor (lu)							
IN	18							
"•	,,,	* Minimu	m values for	the typical	operating	condition.		
		The val		worst case	operating o	ondition are	given by the	maximum delay
		aiupiie						
1								
}								
C21-I1R-E0	Sheet 1/1							Page 21 21
								Page 21-31

	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFIC/	ATION		" CG211	( " Version
Cell Name	Function							Number of I
I1RU	Schmitt Trigger I (TTL Type, Inver	Input Buffer ter) with Pull-up Resistance						8
Cell	Symbol			ameter				
			ıb		to	in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		2.370	0.060	1.248	0.039			X to IN
						1		
						l		
						İ		
						l		
_						l		
x	Ø IN							
						l		
						l		
						1		
		Paramete	er				Symbol	Typ (ns) *
						1		
						- 1		
						1		
						- 1		
						- 1		
	Input Loading							
Pin Name	Factor (lu)							
						- 1		
						1		
	Output Driving							
Pin Name	Factor (lu)					i		
IN	18							<u> </u>
,,,,		* Minimu	m values fo	r the typical	operating of	condition		
		The val multiplie		worst case	operating o	ondition	are given by th	e maximum delay
		типри	<b>51.</b>					
<u> </u>		L						
C21-I1RU-E0	Sheet 1/1							
<u> </u>								Page 21-3

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG21k	( " Version
Cell Name	Function							Number of BC
I1RD	Schmitt Trigger (TTL Type, Inve	Input Burter) with	iffer n Pull-d	own Re	sistance	9		8
Cel	Symbol			Pro	pagation D	elay Paraı	neter	
			ıp		to	in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		2.370	0.060	1.248	0.039			X to IN
							1	
					ļ	1		
					l			
					İ	l		
_								
x	Ø>>>→ IN						1.	
L								
		Paramete					Symbol	Typ (ns) *
		1 4/4/1/1000	·				C)GC.	1,75 (110)
							1	
							1	
							1	
	Input Loading							
Pin Name	Factor (lu)							
							1	
	Output Driving							
Pin Name	Factor (lu)					İ		
IN	18							
114	10		n values for					
				worst case	operating o	ondition ar	e given by the	e maximum delay
		multiplie	er.					
C21-I1RD-E0	Sheet 1/1							
OLI-IIID-LU	Chect i/i							Page 21-33

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG211	K " Version
Cell Name	Function							Number of BC
I2R	Schmitt Trigger (TTL Type, True	Input Bu )	ıffer					8
Cel	Symbol	Í		Pro	pagation D	elay Paran	neter	
			ıρ		to	n		Path
		t0	KCL	t O	KCL	KCL2	CDR2	
		1.182	0.060	1.967	0.062			X to IN
					1			
					İ			
					i			
_								
x	<i>б</i> >— IN							
					1			
					İ			
					l			
				<u> </u>	<u> </u>	<u> </u>		
		Paramete	er		***************************************		Symbol	Typ (ns) *
								•
	Input Loading							
Pin Name	Factor (lu)							
						l		
						- 1		
Pin Name	Output Driving Factor (lu)					ı		
						1		
IN	18	* Minimu	m values fo	r the typical	operating	condition.		
		The val	ues for the	worst case	operating o	ondition are	given by th	e maximum delay
		multiplie	er.					
		•						
004 105 55	Observation 1							
C21-I2R-E0	Sheet 1/1							Page 21_34

Coll Name   Function   Number of BC	CITIT	SHICMOS GATE ADD	TIMI I VAS	CELLS	PECIFIC	ATION		" CG21k	" Version
Schmitt Trigger Input Buffer (TTL Type, True) with Pull—up Resistance   Seminary   TTL Type, True) with Pull—up Resistance   Seminary   TTL Type, True) with Pull—up Resistance   Seminary   Ttl True   Ttl Tru	College	T Eurotice	TAT UNIT OLLE OF CONTOATION						
Cell Symbol    No   10   KCL   10   KCL   KCL   CDR2   Path	Cell Name							Number of	
Cell Symbol    No   10   KCL   10   KCL   KCL   CDR2   Path	IDRII	Schmitt Trigger	input Bu	itter					lα
Cell Symbol    No   10   KCL   10   KCL   KCL   CDR2   Path		(TTL Type, True	) with P						
To   KCL   10   KCL   KCL   COR2   Path	Cel				Pro	pagation D	elay Par	ameter	
Parameter  Parameter  Symbol Typ (ns)  Parameter  Symbol Typ (ns)  Pin Name   Input Loading Factor (tu)  Pin Name   Table   Ta						to	in		Doth
Parameter Symbol Typ (ns) *  Parameter Symbol Typ (ns) *  Pin Name Factor (tu)  Pin Name Practor (tu)  1 8  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–12RU–E0 Sheet 1/1			t O	KCL	t 0	KCL	KCL2	CDR2	Pan
Parameter Symbol Typ (ns) *  Parameter Symbol Typ (ns) *  Pin Name Factor (tu)  Pin Name Practor (tu)  1 8  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–12RU–E0 Sheet 1/1			1.182	0.060	1.967	0.062			X to IN
Pin Name Input Loading Factor (lu)  Pin Name Sector (lu)  IN 18  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–12RU—E0 Sheet 1/1	ļ						l	1	
Pin Name Input Loading Factor (lu)  Pin Name Sector (lu)  IN 18  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–12RU—E0 Sheet 1/1	1						l	i l	
Pin Name Input Loading Factor (lu)  Pin Name Sector (lu)  IN 18  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–12RU—E0 Sheet 1/1							1		
Pin Name Input Loading Factor (lu)  Pin Name Sector (lu)  IN 18  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–12RU—E0 Sheet 1/1	ĺ			l				1 1	
Pin Name Input Loading Factor (lu)  Pin Name Sector (lu)  IN 18  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–12RU—E0 Sheet 1/1					1	l	l	l l	
Pin Name Input Loading Factor (lu)  Pin Name Sector (lu)  IN 18  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–12RU—E0 Sheet 1/1									
Pin Name Input Loading Factor (lu)  Pin Name Sector (lu)  IN 18  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–12RU—E0 Sheet 1/1	1 1	<b>&gt;</b>							
Pin Name   Input Loading Factor (lu)    Pin Name   Gutput Driving Factor (lu)    IN   18   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	x —	D IN		,					
Pin Name   Input Loading Factor (lu)    Pin Name   Gutput Driving Factor (lu)    IN   18   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					i		İ		
Pin Name   Input Loading Factor (lu)    Pin Name   Gutput Driving Factor (lu)    IN   18   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name   Input Loading Factor (lu)    Pin Name   Gutput Driving Factor (lu)    IN   18   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.				•				ł l	
Pin Name   Input Loading Factor (lu)    Pin Name   Gutput Driving Factor (lu)    IN   18   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name   Input Loading Factor (lu)    Pin Name   Gutput Driving Factor (lu)    IN   18   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			Paramete		L	L	<u> </u>	Symbol	Typ (ns) *
Pin Name			Turumen					0,0.	1,75 ()
Pin Name									
Pin Name	1								
Pin Name									
Pin Name									
Pin Name									
Pln Name Output Driving Factor (tu)  1N 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C21–I2RU–E0 Sheet 1/1							ļ		
Pin Name IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21–I2RU–E0   Sheet 1/1	Pin Name	Factor (lu)							
Pin Name IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21–I2RU–E0   Sheet 1/1									
Pin Name IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21–I2RU–E0   Sheet 1/1									
Pin Name IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21–I2RU–E0   Sheet 1/1									
Pin Name IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21–I2RU–E0   Sheet 1/1									
Pin Name IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21–I2RU–E0   Sheet 1/1									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C21–I2RU–E0**   Sheet 1/1**	Din None	Output Driving							
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.  **C21-I2RU-E0** Sheet 1/1**	Pin Name	ractor (IU)							
The values for the worst case operating condition are given by the maximum delay multiplier.	IN	18							
C21-I2RU-E0   Sheet 1/1			* Minimu	m values to	r the typical	operating of	condition.	ana missaa huu th	a mayimum dalau
C21-I2RU-E0 Sheet 1/1					worst case	operating o	oridition a	are given by u	a maximum delay
C21–l2RU–E0 Sheet 1/1			manapine	21.					
C21- 2RU-E0   Sheet 1/1   Page 21-35			L						
C21- 2RU-E0   Sheet 1/1   Page 21-35									
C21-I2RU-E0 Sheet 1/1	ļ								
C21-I2RU-E0   Sheet 1/1   Page 21-35									
C21–I2RU–E0 Sheet 1/1 Page 21–35									
C21–I2RU–E0 Sheet 1/1 Page 21–35									
C21–I2RU–E0 Sheet 1/1 Page 21–35									
C21–I2RU–E0 Sheet 1/1 Page 21–35									
C21-I2RU-E0 Sheet 1/1 Page 21-35									
C21-I2RU-E0   Sheet 1/1   Page 21-35									
C21-I2RU-E0   Sheet 1/1   Page 21-35									
C21–I2RU–E0 Sheet 1/1 Page 21–35									
C21–I2RU–E0   Sheet 1/1   Page 21–35									
C21–I2RU–E0   Sheet 1/1   Page 21–35									
C21–I2RU–E0   Sheet 1/1   Page 21–35									
C21–I2RU–E0   Sheet 1/1   Page 21–35									
C21–I2RU–E0   Sheet 1/1   Page 21–35									
C21-I2RU-E0   Sheet 1/1   Page 21-35									
C21–I2RU–E0 Sheet 1/1 Page 21–35									
Page 21–35	C21-I2RU-E0	Sheet 1/1							
									Page 21-3

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL SI	PECIFIC/	ATION		" CG21I	K " \	/ersion
Cell Name	Function								Number of BC
I2RD	Schmitt Trigger I (TTL Type, True	Input Bu ) with Pi	ıffer ull–dow	n Resist	tance				8
Cell	Symbol			Pro	pagation D	elay Para	meter		
			ip		tc	ln			Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	<u> </u>	
		1.182	0.060	1.967	0.062				X to IN
x	in								
	-								
		<u> </u>				<u> </u>	Sumb -1	<u> </u>	Tun (no) *
		Paramete	er				Symbol	<u> </u>	Typ (ns) *
5: 11	Input Loading					}			
Pin Name	Factor (lu)								
	Output Driving								
Pin Name	Factor (lu)								
IN	18							<u> </u>	
		* Minimu	m values for	r the typical	operating o	condition.	re aiven by th	ne ma	ximum delay
		multiplie			operating t		y u	ma	Joint
		l							
C21-I2RD-E0	Sheet 1/1							_	Page 21-36
								ı	rage 21-36

FUUT	CH CHOC CATE ADD	DAY LINUT	OFIL O	DEOLEIO	ATION		I " CC211	" Version
Cell Name	SU CMOS GATE ARF	TAY UNIT	CELL S	PECIFICA	ATION		LGZIN	Number of BC
	runction							Number of BC
01B	Output Buffer (I	nverter)						3
Cel	Symbol			Pro	pagation D	elay Paran	neter	
		tı	ıρ			dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	raui
от —	<b>&gt;</b> ~×	0.790 (2.47)	0.028	1.060 (4.24)	0.053		Symbol	OT to X
		Taramete					- Jillooi	135 (113)
Pin Name OT	Input Loading Factor (Iu) 2							
		]				j		
Pin Name	Output Driving Factor (lu)							
		* Minimui The val multiplie	ues for the	r the typical worst case	operating o	condition. ondition are	given by the	e maximum delay
2. Ou	e unit of KcL is ns/pF. tput load capacitance of parameters in parent						ո.	

C21-O1B-E0   Shee
-------------------

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL SI	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
O1BF	Output Buffer (I	OL=8m/	A, Inver	ter)				4
Cell	Symbol							
		tı			pagation D to	in		Path
,		t O	KCL	t O	KCL	KCL2	CDR2	Pan
		0.830 (2.51)	0.028	1.070 (3.47)	0.040			OT to X
от —	<b>&gt;</b> -x	Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
ОТ	2							
Pin Name	Output Driving Factor (lu)							
							given by the	e maximum delay

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

CUUT	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version								
Cell Name	Function	TAT UNIT	CELL S	PECIFICA	ATION		CGZTI	Number of B	
	Function								
O1L	Power Output B	uffer (In	verter)					3	
Cel	Symbol								
			J <b>p</b>			in		Path	
		t O	KCL	t 0	KCL	KCL2	CDR2		
		0.900	0.020	1.240	0.026	l	į .	OT to X	
		(2.10)		(2.80)		1	1		
					i '	l			
						1			
						ł	1		
_						ł			
					1		1		
от —	>>—×				l .	İ			
L					Í	l	1		
						l			
						1			
		Paramete	er				Symbol	Typ (ns) *	
						1			
						- 1			
						- 1			
						- 1			
	Input Loading					- 1			
Pin Name	Factor (lu)					- 1			
OT	2					l			
•	_					j			
						1			
						j			
	Output Driving								
Pin Name	Factor (lu)					- 1			
	<u> </u>								
		* Minimur	m values fo	r the typical	operating of	condition			
		The val	ues for the					e maximum delay	
		multiplie	er.						

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21K	' Version
Cell Name	Function							Number of BC
01R	Output Buffer (I	nverter)						5
	with Noise Limit	Resista	nce					<u> </u>
Cell	l Symbol	ļ		Proj	pagation D		neter	
		t O	KCL	t O	KCL	ln KCL2	CDR2	Path
		1.730	0.036	4.540	0.081	KOLE	ODITE.	OT to X
		(3.89)	0.000	(9.40)	0.001			0.107
		` ′		, ,				
							1 1	
			1				1	
							1	
от-	>>—×		!					
L			l					
			1		1			
			l				1	:
		Paramete	er				Symbol	Typ (ns) *
							1	
							l	
						- 1		
						1		
						1	İ	
Die Neuer	Input Loading					1		
Pin Name	Factor (lu)							
ОТ	1					l		
						1		
						1	]	
						1		
Pin Name	Output Driving Factor (lu)	l				1	1	
T III TAUNIC	1 40(0) (14)	i				1	1	
		* Minimu	m values fo	r the typical	operating of	condition.	·····	
		The val	ues for the				given by the i	maximum delay
		multipli	er.					
	l	L						<u></u>
Note: 1. The	e unit of KcL is ns/pF.							
2. 00	tput load capacitance	of 60 pF	is used fo	r Fujitsu's	s logic sir	nulation.		
3. In	e parameters in parent	neses ar	e me vall	ies applie	to the s	oiiiuiali0i	11.	
C21-O1R-E0	Sheet 1/1							
								Page 21-40

	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFIC/	ATION		" CG21F	( " Version
Cell Name	Function							Number of BC
O1RF	Output Buffer (I with Noise Limit	OL=8m/ Resista	A, Invert nce	ter)				5
Cell	Symbol			Pro	pagation D	elay Paran	neter	
		tu	ıp			ln		Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	raui
от —	<b>&gt;</b> ~x	1.780 (3.94)	0.036	5.690 (8.57)	0.048		Symbol	OT to X
Pin Name OT Pin Name	Input Loading Factor (lu) 1 Output Driving Factor (lu)	• Minimur The vall multiplie		r the typical worst case (	operating o	condition.	given by th	e maximum delay
	<u> </u>							

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-O1	RF-E0	I Sheet 1/1

FUUT	OIL OLIOO OATE ADD			DEOUTIO	. T.O		L # 000414	n 1 / 1
Cell Name	SU CMOS GATE ARE	KAY UNII	CELLS	PECIFICA	ATION		" CG21K	
Cell Name								Number of BC
<i>01S</i>	Power Output B with Noise Limit	Resista	nce					5
Cel	l Symbol			Pro	pagation D	elay Paran	neter	
		tup tdn						
		t O	KCL	t O	KCL	KCL2	CDR2	Path
		2.040	0.024	6.720	0.040		l l	OT to X
		(3.48)	1	(9.12)			1 1	
			1			1	1	
						l	1 1	
			ł					
						l	1	
1			Ì				] [	
от —	>>—×		ĺ			1	l	
L								
				ŀ			1 1	
		Paramete	er		<u> </u>	·	Symbol	Typ (ns) *
						- 1		
						- 1		
		ŀ				1		
	Input Loading					ļ		
Pin Name	Factor (lu)					ſ		
ОТ	1					l		
01	'					1		
							1	
	0.410.1.1							
Pin Name	Output Driving Factor (lu)					1		
		* Minimur	m values fo	r the typical	operating of	condition		
		The val	ues for the	worst case	operating o	ondition are	given by the	maximum delay
		multiplie			-		•	•

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG21k	( " Version
Cell Name	Function							Number of BC
O2B	Output Buffer (1	Γrue)						3
Cel	Symbol			Pro	pagation D	elay Parai	neter	
		tı.			Path			
		t O	KCL	t O	KCL	KCL2	CDR2	
		0.500	0.028	0.820	0.053		1	OT to X
		(2.18)		(4.00)	1		1 1	
						l		
						Ì		
							1 1	
[	` "							
от	x	·						
V								
							1	
		Paramete	L	L		Ц	Symbol	Typ (ns) *
		raramete	-1				Cymbol	195 (113)
	Input Loading					1	i	
Pin Name	Factor (lu)							
ОТ	6							
							i	
	Output Driving							
Pin Name	Factor (lu)					l		
		* Minimur	m values for	r the typical	operating of	condition.		
				worst case	operating o	ondition ar	e given by the	e maximum delay
		multiplie	er.					
		<u></u>						

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-O2B-E0 Sheet 1/1

EIIIT	JJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version							/ersion		
Cell Name	Function	IAT CIVIT	OLLLO	LOITIO	ATION				`	Number of BC
O2BF	Output Buffer (IC	DL=8mA	=8mA, True)							3
Cel	Symbol		· · · · · · · · · · · · · · · · · · ·	Pro	pagation D	elav Pa	rame	eter		
		tı.	ıp	l		dn				D-4
		t O	KCL	t O	KCL	KCL	2	CDR2		Path
		0.560	0.048	0.850	0.040		Ī			OT to X
		(2.24)		(3.25)	İ		- 1	- 1		
						l				
				1	1	1				
<b>\</b>				ļ	1		- 1			
от-	<u>&gt;</u> х						- 1			
							Ì			
					l		- 1			
				Ì	l	]				
		Paramete	<u> </u>	L	L	$\vdash$	닏.	ymbol		Typ (ns) *
		Paramete	71 					yiiiooi		Typ (IIs)
						1				
		İ				ı				
						- 1				
	r					1		İ		
Din Name	Input Loading									
Pin Name	Factor (lu)									
ОТ	6					ŀ				
						1				
						l				
						- 1				
	Output Driving									
Pin Name	Factor (lu)	l				I				
		<del></del>								
		The val	m values to	r the typical	operating o	condition	٦. عدم ہ	aiven hy th	e ma	ximum delay
		multiplie		110101 0000	oporating o	0110111011	u.o	g		iximum colay
Note: 4 Th	a unit of Kou is no/all									
	e unit of KcL is ns/pF.									
2. Ou	tput load capacitance	of 60 pF i	is used fo	r Fujitsu'	s logic sir	mulatio	n.			
3 Th	e parameters in parent	heses ar	e the valu	ies applie	ed to the	simula	tion.			
]	- p									

Page 21-44

C21-O2BF-E0 | Sheet 1/1

	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFIC	ATION		" CG21K '	
Cell Name	Function						<u></u>	Number of BC
O2L	Power Output B	uffer (T	rue)					3
Cel	l Symbol			neter				
			lb KCI			in KCLD	Loppo	Path
		0.640	KCL 0.020	1.020	0.026	KCL2	CDR2	OT to X
		(1.84)	0.020	(2.58)	0.026	ĺ		01107
		(	ł	(2.00)	l	Ì		
		ł						
					l	]		
				İ				
	_					l		
от —	<u>&gt;—</u> х		İ			1		
		i	Ì	ŀ				
		i		l		l	1	
		l						
		Paramete	L	L		Ц	Symbol	Typ (ns) *
		1 0.0	<u></u>				<del> </del>	.,,,
		]						
	Input Loading							
Pin Name	Factor (lu)	ł				İ		
OT	6							
	Output Driving	ł						
Pin Name	Factor (lu)	1						
		<u> </u>						
		* Minimu	m values fo	r the typical	operating o	condition.		
		The val		worst case	operating o	ondition ar	e given by the r	naximum delay
		,,,ouple						
Note: 1 Th	e unit of KcL is ns/pF.							
			ia waad t-	e Enliter?	o logio sir	mulation		
I	tput load capacitance							
3. The	e parameters in parent	theses ar	e the valu	ies applie	ed to the	simulatio	n.	

C21-O2L-E0

Sheet 1/1

FUJIT	SU CMOS GATE ARE	GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version						
Cell Name	Function	Number of BC						
O2R	Output Buffer (	rue)						4
	with Noise Limit	Resista	ince					
Cel	Symbol			Pro	pagation D		neter	
		t O	JP KCL	t O	KCL	in KCL2	CDR2	Path
		1.510	0.036	4.400	0.081			OT to X
		(3.67)	0.000	(9.26)	0.00		1 1	
		, ,	1	, ,			1 1	
					1			
		ŀ		ì			1 1	
		l	ł		l			
۱ ۲		1			1			
от	x			1	l		1 1	
			1			l		
			l		l	1	1 1	
		l		<b>!</b>				
			L	<u> </u>	<u> </u>	l		
ĺ		Paramete	er				Symbol	Typ (ns) *
						1	1	
							ĺ	
		1				1		
	Input Loading					l	ļ	
Pin Name	Factor (lu)						j	
OT	2	1						
	_							
		1						
		}						
	Output Driving	1						
Pin Name	Factor (lu)	l				1		
		<u> </u>						
		* Minimu	m values fo	r the typical	l operating of	condition. ondition ar	e given by the I	maximum delay
		multipli			operating o	oridition di	o given ey ale i	
		<u> </u>						
Note: 1. Th	e unit of KCL is ns/pF.							
1	tput load capacitance		ic used fo	vr Fuiiteu'	e logic eir	mulation		
3. Th	e parameters in paren	theses ar	e the valu	ues applie	ed to the	sımulatio	n.	
l								

Page 21-46

C21-O2R-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BO
CODE	Output Buffer (IC	DL=8mA	A, True)					4
<i>02RF</i>	with Noise Limit	Resista	nce					4
Cell	Symbol			Pro	pagation D	elay Param	eter	
		tu	Path					
		t 0	KCL	t 0	KCL	KCL2	CDR2	Paul
		1.570	0.036	5.600	0.048			OT to X
		(3.73)		(8.48)			1	
<b>N</b>								
от ——	<u>&gt;</u> х							
•								
		Paramete			l	L	Symbol	Typ (ns) *
		Paramete	·r				Symbol	Typ (ns)
						j		
							ŀ	
							ļ	
	Input Loading							
Pin Name	Factor (lu)	ļ						
OT	2	l					l	
						1		
		ł				ļ		
	Output Driving	1						
Pin Name	Factor (lu)	ĺ					Ì	
		1						
		* Minimu	n values for	r the typical	operating of	condition.		
		The val	ues for the	worst case	operating o	ondition are	given by the	e maximum delay
		multiplie	er.					
		L						

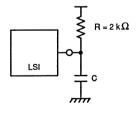
- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

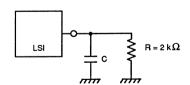
C21-	O2RF-E	:0 l	Sheet	1/1

	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG21F	( " Version
Cell Name	Function							Number of BC
<i>02S</i>	Power Output Bi	uffer (T	rue)					4
	with Noise Limit	Resista	nce					
Cell	Symbol			Pro	pagation D		neter	
		tup tdn						
		t 0	KCL	t 0	KCL	KCL2	CDR2	OT 4- V
		1.820	0.024	6.560	0.040			OT to X
		(3.26)		(8.96)				
		1	'					
							[ [	
от —	>×							
L								
		Paramete				L	Symbol	Typ (ns) *
		Paramete	žI				Syllibol	Typ (IIS)
						ļ		
Pin Name	Input Loading Factor (lu)							
		ł						
ОТ	2	l				- 1		
						İ		
						1		
Pin Name	Output Driving Factor (lu)					1		
rii Name	ractor (lu)	l						
		* Minimu	m values fo	r the typical	operation (			L
		The val	ues for the	worst case	operating o	ondition are	given by th	e maximum delay
		multiplie						·
		l						

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJIT	SU CMOS GATE ARF	U CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version							
Cell Name	Function							Number of BC	
O4T	Tri-state Output	Buffer	(True)					6	
Cell	Symbol			Pro	pagation D	elay Par	ameter		
		tu			to			Path	
		t O	KCL	t O	KCL	KCL2	CDR2		
		0.710 (2.53)	0.028	1.460 (4.91)	0.053			OT to X	
1									
от	×								
ŕ	1								
	· ·								
			L to Z	<u>.                                    </u>		Z to			
		t O		KCL.	t O		KCL	C to X	
		2.00	0		1.55	0	0.055		
		(15.00	0)	*	(5.13	)			
Pin Name	Input Loading Factor (lu)								
OT C	6 2								
С	2	H to Z Z to H							
		t0		KCL	t 0		KCL		
Pin Name	Output Driving Factor (lu)	2.60 (15.00		*	0.74 (5.13		0.028		

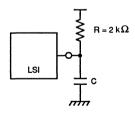


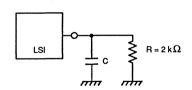


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL is ns/pF.
  - 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

COL CAT EC	Sheet 1/1
C21-O4T-E0	SHEEL I/I

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL	SPECIFIC	ATION		" CG21k	( " Version	
Cell Name	Function							Number of BC	
O4TF	Tri-state Outp	ut Buffer	(IOL:	₌8mA, Trι	ie)			6	
Cell	Symbol		Propagation Delay Parameter						
		tı				in		Path	
		t O	KCL		KCL	KCL	2 CDR2		
от —	×	0.750 (2.57)	0.02	(4.08)	0.040	Z to		OT to X	
		t O	t O		t O		KCL	C to X	
			0	KCL *	1.65 (4.32	0	0.041		
Pin Name	input Loading Factor (lu)								
от	6 2				ļ				
С	۷	t 0		KCL	10	Z to	KCL		
			_	NOL	<del> </del>		0.028		
Pin Name	Output Driving Factor (Iu)	2.60 (15.80		*	0.75 (4.32		0.026		





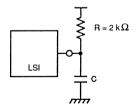
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

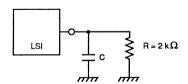
Note: 1. The unit of KcL is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

004	OAT	F F0	Choot 4/4
U21	-O4 I	F-E0	Sheet 1/1

		SU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K" Version									
Cell Name	Function	Function								Number of B	
04W	Power Tri-state	Power Tri-state Output Buffer (True)								6	
Cel	Symbol				Pro	pagation D	elay Pa	arame	eter		
			ıp				in				Path
		t 0	КС		t O	KCL	KCI	2	CDR2		
от х		0.860 (2.16)	0.02	20	1.580 (3.47)	0.029					OT to X
		L to Z				Z to L					
		t O			KCL	t O		KCL			C to X
		2.800 (16.70)			*	1.550 (3.50)		0	0.030		
Pin Name	Input Loading Factor (lu)	]									
OT C	6 2			- 7		Z to H					
C	2	t O	H to Z		KCL	t O	1		KCL		
		3.30	<u> </u>			0.80	_		0.020		
Pin Name	Output Driving Factor (lu)	(16.70			*	(3.50					

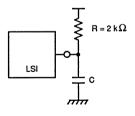


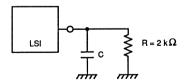


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL is ns/pF.
  - 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21	_04W-	-F0	Sheet	1/1

	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K"								
Cell Name		Function							
O4R		Tri-state Output Buffer (True) with Noise Limit Resistance							
Cel	l Symbol	T		Pro	pagation D	elay Pa	rameter		
		tu				in		Path	
		t O	KCL	t O	KCL	KCL	2 CDR2		
от х		1.570 (3.91)	0.03	6 4.720 (9.99)	0.081			OT to X	
			L to		Z to L				
		t O		KCL	t O		KCL	C to X	
		2.100 (14.20		*	4.600 (9.87)		0.081		
Pin Name	Input Loading Factor (lu)	]							
от	2 2				ļ	Z to	.,,		
c 2		10	H to	KCL	10		KCL		
		<b> </b>		NOL	<del> </del>				
Pin Name	Output Driving Factor (lu)	1.900 (14.20		*	1.60 (9.87		0.036		





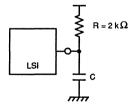
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

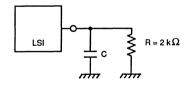
Note: 1. The unit of KCL is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-O4B-F0	Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version									" Version
Cell Name	Function								Number of BC
O4RF		Tri-state Output Buffer (IOL=8mA, True) with Noise Limit Resistance							
Ce	li Symbol	1			Pro	pagation D	elay Pa	arameter	<del></del>
		tı	ıp			to			Path
		t O	KCI	_	t O	KCL	KCI	2 CDR2	
от ——	×	1.730 (4.07)	0.03		5.950 (9.07)	0.048			OT to X
	C	L to Z			Z to L				<b>6. 1</b>
		10		KCL		t O		KCL	C to X
			0		* 5.650 (8.97)			0.051	
Pin Name	Input Loading Factor (lu)								
от	2 2							<u></u>	
С	2	H to Z			KCL	10	Z to	KCL	
		t 0			NUL				
Pin Name	Output Driving Factor (lu)	2.656 (16.10			*	1.60 (8.97		0.036	

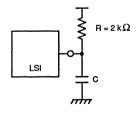


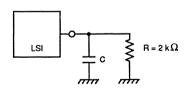


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL is ns/pF.
  - 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21	-04	RF-	E0	Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version							Version			
Cell Name	Function									Number of BC
O4S	Power Tri-state	Power Tri-state Output Buffer (True) with Noise Limit Resistance								5
Cel	l Symbol				Proj	pagation D	elay Pa	rameter		
		tu	р			to	in			Path
		t O	KCL	<u> </u>	t O	KCL	KCL	2 C[	DR2	
от	x c	2.170 (3.73)	0.02		6.900 (9.50)	0.040				OT to X
		L to Z				Z to L				
		t O		KCL		t O		KCL		C to X
		2.500 (16.80			*	6.75 (9.42		0.04	11	
Pin Name	Input Loading Factor (lu)									
от	2 2	H to Z Z to H								
C	4	H to Z			(CL	t O	2 10	KCI		
			$\overline{}$			1.80	<del>,  </del>	0.02		
Pin Name	Output Driving Factor (lu)	3.500 (16.80			*	(9.42		0.02	:5	
	l	l								





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

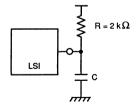
Note: 1. The unit of KcL is ns/pF.

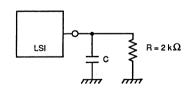
- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-O4S-E0	Sheet 1/1
UZ1-U43-EU	Sileet I/I

CITUT	SH CMOS GATE ADI	DAV LINII	CEL	1 8	DECIFIC	MOLTA		" CG211	C" Version
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K"  Cell Name Function								Number of BC	
H6T									10
Cell	Symbol				Pro	pagation D	elay Pa	rameter	
			ıρ				ln		Path
		t O	КС	:L	t O	KCL	KCL	.2 CDR2	raui
		0.561 0.710 (3.09)	0.0		0.970 1.460 (5.97)	0.017 0.053			X to IN OT to X
IN									
от									
	С	L to Z							
		t O			KCL	t O		KCL	C to X
		2.000 (19.20			*	1.55 (6.23		0.055	
Pin Name	Input Loading Factor (lu)	]							
от	6 2	<u> </u>		<u>L_</u>			Z to		
С		10	Н	to Z	KCL	t O	2 to	KCL	
		<b></b>		-	or		$\overline{}$		
Pin Name	Output Driving Factor (lu)	2.60 (19.2			•	0.74 (6.23		0.028	

36





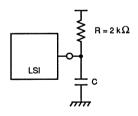
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

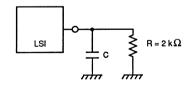
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H6T-	-F0 l	Sheet 1/1

FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL	SF	PECIFICA	ATION		Т	" CG21F	<" ∨	ersion
Cell Name	Function										Number of BC
H6TU	Tri-state Outpu with Pull-up Re			er	(True)						10
Cel	Symbol				Pro	pagation D	elay Pa	arame	eter		
		tı	ıp				ln				Path
		t O	KCL		t O	KCL	KCI	2	CDR2		
от х		0.561 0.710 (3.09)	0.01 0.02		0.970 1.460 (5.97)	0.017 0.053					X to IN OT to X
			L to	17			Z to				
ı		10			KCL	t O			KCL		C to X
			2.000 (19.20)		*	1.550 (6.23)		0.055			
Pin Name	Input Loading Factor (lu)										
OT C	6 2	<u> </u>	H to	7			Z to	. H			
		t O	1		KCL	t O			KCL		
			<del>,                                    </del>			0.74		-	0.028		
Pin Name	Output Driving Factor (lu)		2.600 (19.20)		*	(6.23					
IN	36										

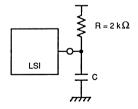


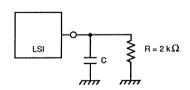


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H6TU-E0   Sheet 1/1	
-------------------------	--

			_							
FUJIT	SU CMOS GATE ARI	RAY UNIT	CEL	L SI	PECIFICA	ATION		" CG21	Κ"	Version
Cell Name	Function									Number of BC
H6TD	Tri-state Output with Pull-down	t & Input Resistar	Buff nce	fer	(True)					10
Cel	Symbol	T			Pro	pagation D	elay Pa	arameter		<u> </u>
		tu	р			tc	ln			Path
		t O	t 0 KCL		t O	KCL	KCL	2 CDR2		raui
	4	0.561 0.710 (3.09)	0.01		0.970 1.460 (5.97)	0.017 0.053				X to IN OT to X
и <b></b>	×									
	C	L to Z				Z to L			1	
		t O			KCL	t O		KCL	l	C to X
		2.000 (19.20)			*	1.550 (6.23)		0.055		
Pin Name	Input Loading Factor (lu)									
οŢ	6 2			_					ł	
С	2	t O	Ht	o Z	KCL	10	Z to	KCL	1	
					NOL				ł	
Pin Name	Output Driving Factor (lu)	2.600 (19.20)			*	0.740 (6.23)		0.028		
IN	36									





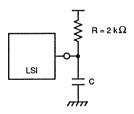
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

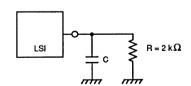
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-	HATD-	-F0	Sheet 1/1

FUJII	SU CMOS GATE AR	ATION		" CG21k	( " Version			
Cell Name	Function							Number of B
H6TF	Tri-state Outp	ut & Inpu	t Buffe	r (IOL=8	mA, Tru	ie)		10
Cell	l Symbol			Pro	pagation D	elay Pa	rameter	
			p		to			Path
		t 0	KCL	t O	KCL	KCL	2 CDR2	
		0.561 0.750 (3.13)	0.014 0.028		0.017 0.040			X to IN OT to X
IN		:						
от								
	С	<b> </b>	L to Z	<u>-</u>		Z to	L L	
		t O		KCL	t O	Ī	KCL	C to X
		2.200 (20.10)		*	1.650 (5.14)		0.041	
Pin Name	Input Loading Factor (lu)							
ОТ	6 2							
С	2		H to 2		<u> </u>	Z to		
		t O		KCL	t0		KCL	
Pin Name	Output Driving Factor (lu)	(20.10		*	0.75 (5.14	-	0.028	
IN	36							





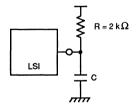
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

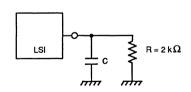
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H6TF-E0	Sheet 1/1

	CU CMOS CATE ADI	DANG LINUT	· CELI		DECIFIC	ATION			" CG21	K" Vorsian
Cell Name	SU CMOS GATE ARE	TAY UNII	UELL	_ 51	-ECIFIC	ATION		i	UG211	K" Version Number of BC
H6TFU	Tri-state Outpu with Pull-up Re	it & Inpu	t Buf	fer	(IOL=8	mA, Tr	ıe)			10
Cel	l Symbol				Pro	pagation D	elay P	aram	eter	
		tı	р				dn n			Path
			KCL	-	t 0	KCL	KCI	L2	CDR2	Path
		0.561 0.750 (3.13)	0.01 0.02		0.970 1.480 (4.88)	0.017 0.040				X to IN OT to X
OT X										
			L to				Z t	٥L		
				KCL	t0		KCL		C to X	
			2.200 (20.10)		*	1.650 (5.14)		(	0.041	
Pin Name	Input Loading Factor (lu)									
от	6 2	ļ						L		
С	2	10	H to		KCL	10	Z to	ЭН	KCL	
					NOL		$\overline{}$	<del>                                     </del>		
Pin Name	Output Driving Factor (lu)	2.600 (20.10			*	0.75( (5.14			0.028	
IN	36									





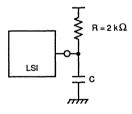
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

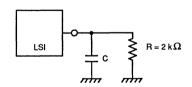
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21	I_H	6TFI	I_F0	Sheet 1/1

CILIIT	SU CMOS GATE ARE	THALLYA	CEL	1 01	DECIFIC /	ATION		1 " CC	201K"	Version
Cell Name	Function	TAY UNIT	CEL	L 01	PECIFICA	ATION		1 00	12 I K	Number of BC
H6TFD	Tri-state Outpu with Pull-down	t & Inpu Resista	t But	ffer	(IOL=8	mA, Tru	ie)			10
Cel	l Symbol				Prop	pagation D	elay Pa	arameter		
		tu	р			to	in			Path
		t O	KC	L	t O	KCL	KCI	2 CDF	R2	Patn
	1			)14 )28	0.970 1.480 (4.88)	0.017 0.040				X to IN OT to X
OT X										
	· ·		Lt	o Z			Z t	o L		
		t O			KCL	t 0		KCL		C to X
		2.200 (20.10)			*	1.650 (5.14)		0.041		
Pin Name	Input Loading Factor (lu)									
OT C	6 2			to Z			Z to	. U		
O		t O		0 2	KCL	t O		KCL	-	
		2.600				0.75	<u>,                                    </u>	0.028		
Pin Name	Output Driving Factor (lu)	(20.10			*	(5.14	-	0.020		
IN	36									





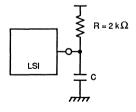
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

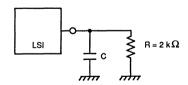
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H6TFD-E0 Sheet 1/1

	TSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K"											
Cell Name	Function							Number of B				
H6W	Power Tri-state	Output	& Inpi	ut Buffer	(True)			10				
Cel	l Symbol	T		Pro	pagation D	elay Pa	rameter					
		tı				In		Path				
		t O	KCL	t O	KCL	KCL	2 CDR2					
OT X		0.561 0.860 (2.56)	0.014 0.020		0.017 0.029			X to IN OT to X				
	C	10	L to	Z KCL	to	Zto	KCL	C to X				
		2.800 (21.00)		*	1.55 (4.10	0.030		0.07				
Pin Name	Input Loading Factor (lu)											
от	6 2		H to	<del></del>		l						
С	2	10	H 10	KCL	to	- 210	KCL					
				*	0.80		0.020					
Pin Name	Output Driving Factor (lu)		3.300 (21.00)		(4.10		0.020					
IN	36											

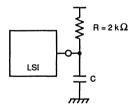


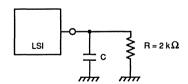


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H6W-E0	Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL	SPECIFIC	ATION		" CG211	K" Version
Cell Name	Function							Number of BC
H6WU	Power Tri-state with Pull-up Re	Output sistance	& Inpu	t Buffer	(True)			10
Cel	l Symbol			Pro	pagation D	elay Par	ameter	
			p			in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
OT X		0.561 0.860 (2.56)	0.014 0.020		0.017 0.029			X to IN OT to X
			L to 2			Z to l		
		t0		KCL	t0		KCL	C to X
		2.800 (21.00)		•	1.550 (4.10)		0.030	
Pin Name	Input Loading Factor (lu)							
от	6 2			7		<del></del>	1	
С	2	10	H to	KCL	to	Z to I	KCL	!
				NOL				
Pin Name	Output Driving Factor (lu)	3.300 (21.00		*	0.800 (4.10)		0.020	
IN	36							

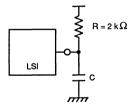


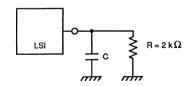


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H6WU-E0 Sheet 1/1

FUJI	ISU CMOS GATE AF	RAY UNIT	CELL	SPECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of B
H6WD	Power Tri-state with Pull-down	Output Resistar	& Inpu	it Buffer	(True)			10
Ce	II Symbol			Pro	pagation De	elay Para	meter	
		tı			td			Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		0.561 0.860 (2.56)	0.014 0.020		0.017 0.029			X to IN OT to X
IN	×							
	С		L to		Z to L			-
		t O		KCL	t O		KCL	C to X
		2.800 (21.00		•	1.550 (4.10)		0.030	
Pin Name	Input Loading Factor (lu)							
ОТ	6 2							
С	2	<u> </u>	H to		<del> </del>	Z to H		
		t O		KCL	t O		KCL	
Pin Name	Output Driving Factor (lu)	3.300 (21.00		•	0.800 (4.10)		0.020	
IN	36	7	1					

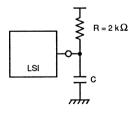


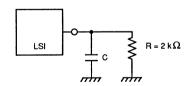


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-	H6WI	)_F0	Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL	SPECIFICA	ATION		" CG21K	( " Version		
Cell Name	Function	`						Number of BC		
H6C	Tri-state Outp	ut & CMC	OS Inte	rface Inc	out Buffe	er (Tr	ue)	10		
Cel	l Symbol		Propagation Delay Parameter							
		tu		t O		in		Path		
		t O			KCL	KCL	2 CDR2			
		0.489 0.710 (3.09)	0.014 0.028	0.706 1.460 (5.97)	0.017 0.053			X to IN OT to X		
от х										
	O	<u> </u>	L to Z		t O	Z to	KCL	C to X		
		2.000 (19.20		*	1.550 (6.23)		0.055	0.10 X		
Pin Name	Input Loading Factor (lu)									
ΟT	6 2									
С	2	10	H to Z		t O	Z to	KCL			
				KCL			0.028			
Pin Name	Output Driving Factor (lu)		2.600 (19.20)		0.740 (6.23		0.020			
IN	36									

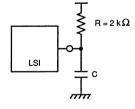


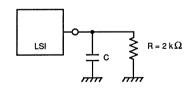


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H6C-	FO	Sheet 1/1

	SU CMOS GATE ARI	RAY UNIT	CEL	<u>L SI</u>	PECIFICA	ATION			CG21K	" Version
Cell Name	Function	+ 0. 0140	O 1-		· I		/T	· · - \		Number of BC
H6CU	Tri-state Outpu with Pull-up Re	esistance	)5 II	iter	race inp	out Bume	er (ı	rue)		10
Cel	l Symbol				Pro	pagation D		aramete	r	
	·	tu					ln			Path
		t O	КС	_	t O	KCL	KCI		DDR2	
		0.489 0.710 (3.09)	0.0		0.706 1.460 (5.97)	0.017 0.053				X to IN OT to X
IN	$ \rightarrow $									
от	×									
	С	J	L to Z				Z t			
		t O		KCL		t O		KCL		C to X
		2.000 (19.20)			*	1.550 (6.23)		0.0	)55	
Pin Name	Input Loading Factor (lu)									
ОТ	6 2			Ļ		<u> </u>				
С	2	t O	H to 2		KCL	t O	Z to		CL	
				<del>                                     </del>	NOL.	<del></del>				
Pin Name	Output Driving Factor (lu)		2.600 (19.20)		*	0.740 (6.23)		0.0	128	
IN	36									

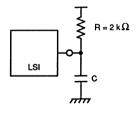


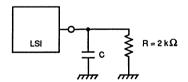


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H6CU-E0 Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CEL	L SI	PECIFICA	ATION		Т	" CG21K	" Version
Cell Name	Function									Number of BC
H6CD	Tri-state Outpu with Pull-down	t & CMC Resista	OS In nce	ter	face Inp	out Buffe	er (T	rue)	)	10
Cel	l Symbol		Propagation Delay Parameter							
		tı	ıρ				n			Path
		t O	KC	L_	t O	KCL	KC	2	CDR2	raui
	4	0.710   0.028		0.706 1.460 (5.97)	0.017 0.053				X to IN OT to X	
IN	×									
	· ·	+0	L to Z		KCI	Z to L		KCI	C to X	
		2.000 (19.20)			*	1.550 (6.23)		0.055		0.0 %
Pin Name	Input Loading Factor (lu)									
OT C	6 2	<u> </u>		o Z			71	L		
C		10	- 1	0 2	KCL	10			KCL	
		2.600				0.740		_	0.028	
Pin Name	Output Driving Factor (lu)	(19.20			*	(6.23)			7.020	
iN	36									

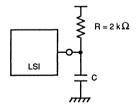


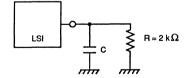


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H6CD-E0 Sheet 1/1

FUJIT	SU CMOS GATE AP	RAY UNIT	CELL	_ SPECIFIC.	ATION		" CG21K	" Version
Cell Name	Function							Number of B
H6CF	Tri-state Outp (IOL=8mA, Tru	ut & CM( ie)	OS In	terface In	out Buffe	er		8
Cell	Symbol	T		Pro	pagation D	elay Pa	rameter	
		tı	ıp	T		in .	1	
		t O	KCL	. t0	KCL	KCL	2 CDR2	Path
IN ————————————————————————————————————	×	0.489 0.750 (3.13)	0.01 0.02		0.017 0.040			X to IN OT to X
	C		L to	Z		Z to	L	
		t O	t0 KC		t O		KCL	C to X
		2.200 (20.10		*	* (5.14		0.041	
Pin Name	Input Loading Factor (lu)							
OT	4 2		H to	. 7		L Z to	<del></del>	
С	4	10	H 10	KCL	t 0		KCL	
			<del></del>		0.75		0.028	
Pin Name	Output Driving Factor (lu)		2.600 (20.10)		(5.14		0.026	
IN	36							

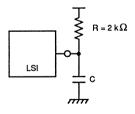


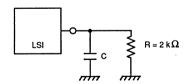


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H6CF-	-F0 l	Sheet 1/1

FUJIT	SU CMOS GATE ARI	RAY UNIT	CEL	LS	PECIFICA	ATION		" CG21F	( " Version
Cell Name	Function								Number of BC
H6CFU	Tri-state Outpu with Pull-up Re						∍r		8
Cel	l Symbol				Pro	pagation D	elay Pa	rameter	
		tup					ln		Path
		t O			t O	KCL	KCL	2 CDR2	raui
			0.0 <sup>2</sup>		0.706 1.480 (4.88)	0.040			X to IN OT to X
OT X									
		<u></u>	L t	o Z	KCL		Z to		C to X
		t O			KUL,	t0		KCL	Ctox
		(20.10			*	1.650 (5.14)		0.041	
Pin Name	Input Loading Factor (lu)								
OT C	4 2	<u> </u>	t 0				Z to	u	
· ·		10			KCL	t O	- <u>- 10</u>	KCL	
	[	2.600				0.75	<del>,  </del>	0.028	
Pin Name	Output Driving Factor (lu)	(20.10	-		*	(5.14		0.020	
IN	36								

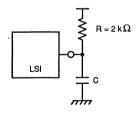


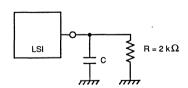


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H6FU-E0 Sheet 1/1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELI	SI	PECIFICA	ATION		" CG21F	(" Version
Cell Name	Function								Number of BC
H6CFD	Tri-state Outpu with Pull-down				L=8mA	True)			8
Cel	ll Symbol				Pro	pagation D	elay Par	rameter	
			ıρ			to			Path
		t O			t 0	KCL	KCL2	CDR2	
IN	<b>-</b> ∕1₁	0.489 0.750 (3.13)	0.01 0.02		0.706 1.480 (4.88)	0.017 0.040			X to IN OT to X
от[	×								
		l	L to	5 Z	KCL	t O	Z to	KCL	C to X
		2.200 (20.10)			*	1.650 (5.14)		0.041	C 10 X
Pin Name	Input Loading Factor (lu)								
οτ	4 2	<u> </u>	H to				Z to		
С	'	10	H 10	0 2	KCL	t O	2 10	KCL	
			$\overline{}$		NOL	0.750	$\overline{}$	0.028	
Pin Name	Output Driving Factor (lu)		2.600 (20.10)		*	(5.14		0.020	
IN	36								





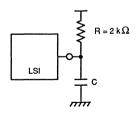
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

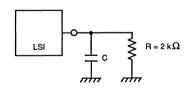
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H6CFD-E0	Sheet 1/1
02 1-11001 D-L0	Oneet 1/1

	TSU CMOS GATE AR	RAY UNIT	CELL	SPECIFIC.	ATION		" CG21K	" Version		
Cell Name	Function							Number of B		
H6E	Power Tri-stat	e Output rue)	& CN	IOS Inter	face			10		
Ce	II Symbol	1		Pro	pagation D	elay Para	meter			
		tu	ip		to		Path			
		t O	KCL	t O	KCL	KCL2	L2 CDR2	Paul		
IN	~		~ 1		0.014 0.020		0.017			X to IN OT to X
	ċ		L to							
		t0	t O		t0	KCL		C to X		
		2.800 (21.00		*	1.550 (4.10)		0.030			
Pin Name	Input Loading Factor (lu)	1								
οτ	6 2		H to	<del></del>	ļ	Z to H				
С	-	10	H 10	KCL	10		KCL			
				1,02	0.800		0.020			
Pin Name	Output Driving Factor (lu)		3.300 (21.00)		(4.10		0.020			
IN	36									





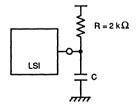
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

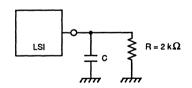
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H6E-	E0 '	Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CEL	L SI	PECIFICA	ATION			" CG211	(" Version
Cell Name	Function	Function					Number of BC			
H6EU	H6EU Power Tri-state Output & CMOS Interface Input Buffer (True) with Pull-up Resistance						10			
Cel	l Symbol				Pro	pagation D	elay P	aram	eter	
			ıp				n			Path
		t O	KC	<u> </u>	t O	KCL	KC	L2	CDR2	
IN	×	0.489 0.860 (2.56)	0.01		0.706 1.580 (4.05)	0.017 0.029				X to IN OT to X
	c		Lt	o Z	KCL	t O	Z t		KCL	C to X
		2.800 (21.00			•	1.550 (4.10)			0.030	
Pin Name	Input Loading Factor (lu)									
οτ	6 2			o Z			7.	o H		
С	۲ ۲	10		<u> </u>	KÇL	t O		<u>Г</u>	KCL	
		<b></b>					·		0.020	
Pin Name	Output Driving Factor (lu)	3.300 (21.00			*	0.800 (4.10)			0.020	
IN	36									

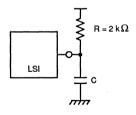


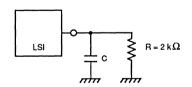


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21	-H6FU-	-F0	l Sheet 1/1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL	SPECIFIC	ATION		" CG211	K " Version
Cell Name	Function					Number of BC		
H6ED	Power Tri-state Output & CMOS Interface Input Buffer (True) with Pull-down Resistance					10		
Cel	l Symbol			Pro	pagation D	elay Pa	rameter	
		tu			tc			Path
		t O	KCL	t O	KCL	KCL	2 CDR2	
in ——		0.489 0.860 (2.56)	0.014 0.020		0.017 0.029			X to IN OT to X
от	от х			Z KCL	to	Z to	L	C to X
		2.800 (21.00)		*	1.550 (4.10)		0.030	
Pin Name	Input Loading Factor (Iu)							
OT C	6 2	ļ	H to	7	<b></b>	Z to	u	
		t O	- T	KCL	10	- T	KCL	
Pin Name	Output Driving Factor (lu)	3.300 (21.00)		*	0.800 (4.10)		0.020	
IN	36							





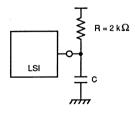
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

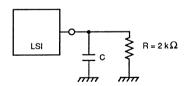
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-F	16ED-E0	Sheet 1/1	

FUJIT	SU CMOS GATE ARI	RAY UNIT	CEL	LSI	PECIFICA	ATION		" CG21I	<b>(</b> " Version
Cell Name	Function							Number of BC	
H6S	Tri-state Outpu (CMOS Type, 7	Tri-state Output & Schmitt Trigger Input Buffer (CMOS Type, True)						14	
Cel	Symbol				Proj	pagation D	elay Pai	rameter	
			ıp				n		Path
		t 0	КС		t 0	KCL	KCL2	CDR2	
IN	×	1.314 0.710 (3.09)	0.00		1.630 1.460 (5.97)	0.045 0.053			X to IN OT to X
	C	L to Z			KCL	Z to L		L KCL	C to X
					KUL.		-	0.055	Clox
		2.00 (19.2			•	1.55 (6.23		0.033	
Pin Name	Input Loading Factor (lu)								
OT C	6 2	ļ	ш	to Z			Z to	ш	
O		t O		0 2	KCL	t O		KCL	
		2.60	0			0.74	10	0.028	
Pin Name	Output Driving Factor (lu)	(19.2			*	(6.2		0.020	
IN	18								

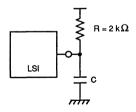


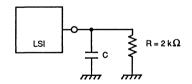


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

$\overline{C}$	1_H6S_F0	Sheet 1/1

Cell Name	TSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K" \ Function						" Version Number of B			
	Tri state Outside Only in Triangle In the Control of the Control o									
H6SU	(CMOS Type, True) with Pull-up Resistance						14			
Ce	II Symbol				Pro	pagation D		arame	ter	
			tup				n			Path
		t 0	КС		t O	KCL	KCI	12	CDR2	V 1 . 101
		1.314 0.710	0.06		1.630 1.460	0.045 0.053				X to IN OT to X
		(3.09)	0.02	28	(5.97)	0.053	İ			OITOX
		(3.03)			(3.51)					
IN —	<i>_</i>							1	1	
114							1			
	×							- 1		
от—	^									
	Ý			Ì				l		
	1									
	C			. Z			71	<u>-                                    </u>		
		t O			KCL.	. 10			KCL	C to X
		2.000			. 1,550		0.055		.055	
		(19.20			•	(6.23)		ľ		
	T	4								
Pin Name	Input Loading Factor (lu)	Ì						1		
ОТ	<del></del>	1						1		
Ċ.	6 2		Н	to Z			Ζt	οН		
		t 0			KCL	t O			KCL	
		2.600				0.740		0	.028	
Pin Name	Output Driving Factor (lu)	(19.20	)			(6.23)	)			
IN	18	7								
	1	1		ı				ı	i	

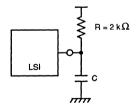


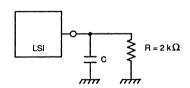


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H6SU-E0 Sheet 1/1

	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K" Version							
Cell Name	Function							Number of B
H6SD Tri-state Output & Schmitt Trigger Input Buffer (CMOS Type, True) with Pull-down Resistance						14		
Ce	I Symbol	T			pagation D		arameter	
		tı	ıρ			in		Path
		t O	KCL	t O	KCL	KCI	2 CDR2	raui
IN	×	1.314 0.710 (3.09)	0.060 0.028		0.045 0.053			X to IN OT to X
	С		L to	I Z KCL	Z to L			
		10	t 0		t O	KCL		CtoX
		2.00 (19.2		*	1.55 (6.2		0.055	
Pin Name	Input Loading Factor (lu)							
OT C	6 2		H to	7	<del> </del>	Z to	N H	1
U	1	10	- 11.60	KCL	10		KCL	1
	Output Driving	2.60		*	0.74 (6.2	10	0.028	
Pin Name	Factor (lu)	] ''''	, I		, ,	-,		
IN	18							





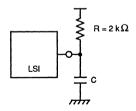
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

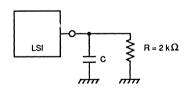
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H6SD-E0	Sheet 1/1

FUJIT	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG21K" Version						" Version	
Cell Name	Function					Number of B		
H6R	Tri-state Output & Schmitt Trigger Input Buffer (TTL Type, True)					14		
Cel	I Symbol	T		Pro	pagation D	elay Pa	rameter	
		tı	ıp qı		to			Path
		t O	KCL	t O	KCL	KCL	2 CDR2	
	_	1.182 0.710 (3.09)	0.060 0.028	1.967 1.460 (5.97)	0.062 0.053			X to IN OT to X
OT X			L to Z			Z to		
		10		KCL	10	- 210	KCL	C to X
		2.000		*	1.550 (6.23)		0.055	0.07
Pin Name	Input Loading Factor (lu)							
от	6 2			,	<b></b>	Z to		
С	4	10	t 0 KCL				KCL	
				NOL	0.740	$\overline{}$	0.028	
Pin Name	Output Driving Factor (lu)	2.600 (19.20		*	0.740 (6.23)		0.020	
IN	18							





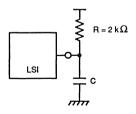
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

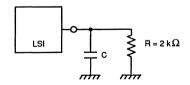
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H6R-E0	Sheet 1/1

FUJIT	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG21K" Version										
Cell Name	Function							Number of B			
H6RU	Tri-state Outpu (TTL Type, Tru	it & Schi e) with F	mitt Tri Pull–up	gger Inp Resista	ut Buffe nce	r		14			
Cel	Cell Symbol			Propagation Delay Parameter							
			ıb		Path						
		t O	KCL	t O	KCL	KCL2	CDR2				
OT X		1.182 0.710 (3.09)	0.060 0.028	1.967 1.460 (5.97)	0.062 0.053			X to IN OT to X			
	C	L to Z				Z to	L				
		t 0		KCL	t O		KCL	C to X			
			)	*	1.550 (6.23)		0.055				
Pin Name	Input Loading Factor (lu)										
от	6 2		H to 2			Z to					
С	2	t O	1 10 2	KCL	t O	- Z 10	KCL				
				NOL							
Pin Name	Output Driving Factor (lu)	2.600 (19.20	)	*	0.740 (6.23)		0.028				
IN	18										

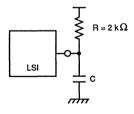


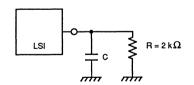


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

001	LIODIL	E0	Ob 4 4 /4
UZ 1-	-H6RU-	-=0	Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CEL	L SI	PECIFICA	ATION			" CG21K	" Version
Cell Name	Function									Number of BC
H6RD	Tri-state Outpo (TTL Type, Tru	ut & Sch e) with F	mitt <sup>-</sup> Pull–	Trig dow	ger Inpi vn Resis	ut Buffe stance	r			14
Cell	T T	Propagation Delay Parameter								
			ıρ		tdn					Path
		t O	кс	L	t O	KCL	KCI	L2	CDR2	
IN	×	1.182 0.710 (3.09)	0.02		1.967 1.460 (5.97)	0.062 0.053				X to IN OT to X
	C	L to Z Z to L				0 L				
		t O			KCL.	t O		KCL		C to X
			)		*	1.550 (6.23		C	).055	
Pin Name	Input Loading Factor (lu)									
OT C	6 2			o Z		<b> </b>	7.	οН		
	_	t0		0 2	KCL	t O		<u> </u>	KCL	
						0.740		_	0.028	
Pin Name	Output Driving Factor (lu)	2.600 (19.20			*	(6.23				
IN	18									





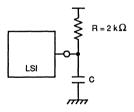
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

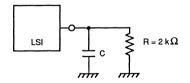
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H6RD-E0	Sheet 1/1

Cell Name H8T Cell Sy	Function Tri-state Outpu & Input Buffer (Tymbol	t with No Frue)  to 0.561 1.570 (4.63)		t 0 0.970	oagation Do			Number of BC
Cell Sy	& Input Buffer (7	tue) to 0.561 1.570	р КСL 0.014	t 0 0.970	pagation De to KCL	n		
	ymbol	0.561 1.570	KCL 0.014	t 0 0.970	to KCL	n		Path
IN ———	$\triangle$	0.561 1.570	KCL 0.014	0.970	KCL		2 CDR2	Path
IN	<u></u>	0.561 1.570	0.014	0.970		KCL2	2 CDR2	
IN<	<u></u>	1.570			0.017			<del></del>
OT X				(11.61)	0.081			X to IN OT to X
			L to Z			Z to		
		t O	1 10 2	KCL	to KCL			C to X
			)))	*	4.600 (11.49		0.081	
Pin Name	Input Loading Factor (lu)							
OT C	2		H to 2	,		Z to	н	
١ .	-	t O	11.02	KCL	t O	<del>- 1</del>	KCL	
		1.900	<u>,                                    </u>	*	1.600	$\overline{}$	0.036	
Pin Name	Output Driving Factor (lu)	(18.10		•	(11.49		0.000	
IN	36							

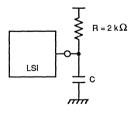


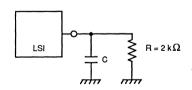


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21_L	IST_FO	Sheet 1/1

FUJIT	SU CMOS GATE ARI	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	(" Version
Cell Name	Function							Number of BC
H8TU	Tri-state Outpu & Input Buffer (	it with N True) wi	oise Li th Pull-	mit Resis -up Resi	stance stance			9
Cel								
			ıp		to			Path
		t O	KCL	t O	KCL	KCL2	CDR2	
	4	0.561 1.570 (4.63)	0.014 0.036	0.970 4.720 (11.61)	0.017 0.081			X to IN OT to X
OT X								
		L to Z			Z to L		4	
		t O		KCL	t O		KCL	C to X
			)	*	4.600 (11.49		0.081	
Pin Name	Input Loading Factor (lu)							
OT C	2 2		H to Z			Z to F	<del>,</del>	
	-	1 to	H 10 Z	KCL	to	2.01	KCL	
		1.900			1.600		0.036	
Pin Name	Output Driving Factor (lu)	(18.10		*	(11.49		0.030	
IN	36							





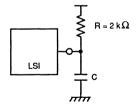
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

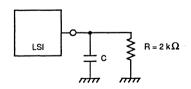
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H8T	U-E0	Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL	SPI	ECIFIC/	ATION		_	" CG21F	C" Version	
Cell Name	Function	Function								Number o	of BC
H8TD	Tri-state Outpu & Input Buffer (	ut with N True) wi	oise I th Pu	_imi II–d	it Resis Iown R	stance esistan	ce			9	
Ce	I Symbol		Propagation Delay Parameter								
			ıρ				n			Path	
		t O	KCL	.	t 0	KCL	KCI	L2	CDR2		
		0.561 1.570 (4.63)	0.01 0.03	6	0.970 4.720 (11.61)	0.017 0.081				X to IN OT to X	
ot ——	×										
	С		L to Z					۰L			
		t O			(CL	t 0		KCL		C to X	
			)		* 4.0 (11				0.081		
Pin Name	Input Loading Factor (lu)										
OT	2 2		H to	-			7.	о Н			
С		10	n (0		KCL	t 0		<del>-</del>	KCL		
		<b></b>	-		,00			<del>                                     </del>	0.036		
Pin Name	Output Driving Factor (lu)	1.900 (18.10			•	1.600 (11.49			0.036		
IN	36										

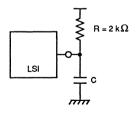


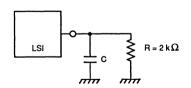


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8T	rD-F0 L	Sheet 1/1

EI III	SU CMOS GATE ARE	DAV LINIT	CELL	CDECIEIC	ATION		1 " CG211	C" Version			
Cell Name	Function	TAT UNII	CELL	SPECIFICA	TION		CGZ11	Number of BC			
H8TF	Tri-state Output with Noise Limit Resistance & Input Buffer (IOL=8mA, True)							9			
Cel	Cell Symbol			Propagation Delay Parameter							
		tu				in		Path			
		t O	KCL	t O	KCL	KCL2	2 CDR2				
		0.561 1.730 (4.79)	0.014 0.036		0.017 0.048			X to IN OT to X			
OT X											
	_	L to Z			Z to		_				
		t O		KCL	t0		KCL	C to X			
			8	*	5.650 (9.99)		0.051				
Pin Name	Input Loading Factor (lu)										
OT C	2 2		H to	7		Z to	ш				
	-	t0		KCL	t O	- i	KCL				
		2.650	<u>,                                    </u>		1.60	0	0.036				
Pin Name	Output Driving Factor (lu)	(20.90		*	(9.99		0.000				
IN	36										





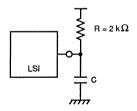
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

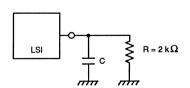
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-	Н8	TF	-E0	Sheet 1/1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CEL	L SI	PECIFICA	ATION		" CG211	K" Version
Cell Name	Function								Number of BC
H8TFU	Tri-state Outpu & Input Buffer (						Resist	ance	9
Cel	Symbol				Prop	pagation D	elay Par	rameter	
		tı.					ln		Path
		t O	КС		t O	KCL	KCL2	CDR2	
	1	0.561 1.730 (4.79)	0.0		0.970 5.950 (10.03)	0.017 0.048			X to IN OT to X
ot ——	×								
			LI	o Z			Z to		
		t O			KCL.	t O		KCL	C to X
		2.100 (20.90)			*	5.650 (9.99)		0.051	
Pin Name	Input Loading Factor (lu)								
OT	2 2			<u> </u>			L		
С	2	10	H	to Z	KCL	t O	Z to	H KCL	
		2.650	`		NOL	1.600	$\overline{}$	0.036	
Pin Name	Output Driving Factor (lu)	(20.90			*	(9.99)		0.030	
IN	36								

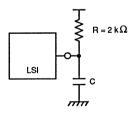


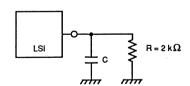


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21		Ľ	T		1		Λ	Sheet 1/1
121	-	ПC		Γŧ	J	_	v	

FUJIT	SU CMOS GATE AR	RAY UNIT	CEL	L SI	PECIFICA	ATION		Т	" CG211	K"Ve	ersion
Cell Name	Function						_				Number of BC
H8TFD	Tri-state Outpu & Input Buffer (	it with N IOL=8m	oise A, Tı	Lin rue	nit Resis ) with P	stance ull–dow	n Re	sist	tance		9
Cel	Symbol				Prop	pagation D	elay Pa	ram	eter		
			p				in				Path
		t O	KCI		t 0	KCL	KCL	.2	CDR2		
	_1	0.561 1.730 (4.79)	0.01 0.03		0.970 5.950 (10.03)	0.017 0.048					X to IN OT to X
от	×										
		10	L to	o Z	KCL	t O	Z to	<u>L</u>	KCL	؍ ا	C to X
		2.100	•		*	5.65( (9.99)	- 1	(	0.051		J 10 X
Pin Name	Input Loading Factor (lu)										
OT	2 2		<u>l</u>	- 7			Z to	. 11			
С	<b>4</b>	10	H 1	0 2	KCL	t O		, п	KCL		
		2.650	$\overline{}$		NOL	1.600	$\overline{}$		0.036	1	
Pin Name	Output Driving Factor (lu)	(20.90			*	(9.99)		(	J.U36		
IN	36										





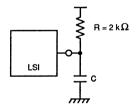
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

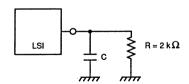
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-	-H8TFD-	-FOI	Sheet 1/1

	<u>SU CMOS GATE AR</u>	RAY UNIT	CELI	<u>L S</u> F	PECIFICA	NOITA			" CG21F	<b>("</b> Version
Cell Name	Function									Number of B
H8W	Power Tri-stat & Input Buffer	e Output True)	with	No	ise Lim	it Resis	tanc	е		9
Cell	Symbol		Propagation Delay Parameter							
		tı				to				Path
		t 0	KCI	_	t O	KCL	KC	L2	CDR2	гаш
ot			0.01 0.02		0.970 6.900 (10.30)	0.017 0.040				X to IN OT to X
	C		L to				Zt	٥L		0. V
		t O			KCL	t O		-	KCL	C to X
		2.500 (20.90	5)		•	6.750 (10.24			0.041	
Pin Name	Input Loading Factor (lu)	1								
OT C	2 2		H to	- 7			7.	<u>L</u> о Н		
٠	2	10	- H (C		KCL	t O		<u> </u>	KCL	
			$\overline{}$			1.80	`	╁	0.025	
Pin Name	Output Driving Factor (lu)	3.500 (20.90			*	(10.2			0.025	
IN	36				:					

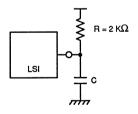


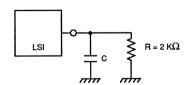


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21	-H8	W-	FO	Sheet 1/1	

FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL	SPECIFICA	ATION		" CG21K	( " Version
Cell Name	Function							Number of BC
H8WU	Power Tri-state & Input Buffer (	Output True) wi	with I th Pul	Noise Lim I–up Resi	it Resis stance	tance	)	9
Cell	Symbol	T		Pro	pagation D	elay Pa	rameter	
		tu				in		Path
		t O	KCL	t O	KCL	KCL	2 CDR2	
IN ————————————————————————————————————	×	0.561 2.170 (4.21)	0.014 0.024		0.017 0.040			X to IN OT to X
	С	10	L to	Z KCL	t0	Z to	L KCL	C to X
		2.500		*	6.750 (10.24	)	0.041	Clox
Pin Name	Input Loading Factor (lu)	1						
οτ	2 2		H to	7	ļ	Z to	<u>.</u>	
С	_	10		KCL	to		KCL	
							0.025	
Pin Name	Output Driving Factor (lu)	3.500 (20.90		*	1.800 (10.24		0.025	
IN	36							

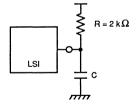


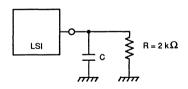


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8WU-E0 Sheet 1/1

	SU CMOS GATE AR	DAT UNIT	CELL	. 35601510.	ATION		LGZIA	( " Version
Cell Name	Function							Number of BC
H8WD	Power Tri-stat & Input Buffer	e Output (True) wi	with th Pu	Noise Lim Il-down R	nit Resis Sesistan	tance ce	9	9
Cell	Symbol	T		Pro	pagation D	elay Pa	rameter	
		tı.	ıp		to	dn .		Path
		t O	KCL	t 0	KCL	KCL	2 CDR2	
		0.561 2.170 (4.21)	0.01 0.02		0.017 0.040			X to IN OT to X
OT	×							
	C		L to	Z		Z to	) L	
		t O		KCL	t O		KCL	C to X
		2.500 (20.90		*	6.750 (10.24		0.041	
Pin Name	Input Loading Factor (lu)							
OT C	2 2		H to	. 7	<u> </u>			
C	2	10		KCL	10	- Z 10	KCL	
		3.500	_		1.800	$\overline{}$	0.025	
Pin Name	Output Driving Factor (lu)	(20.90		•	(10.24		0.025	
IN	36							

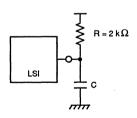


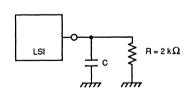


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8WD-E0 I	Sheet 1/1

FUJI	<u>TSU CMOS GATE AR</u>	RAY UNIT	CELLS	PECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
H8C	Tri-state Outpo & CMOS Interf	ut Buffer ace Inpu	with N t Buffe	oise Lim r (True)	it Resist	ance	l	9
Ce	II Symbol	T			pagation D	elay Pa	rameter	
		tı	ıp		to	In		Path
		t O	KCL	t O	KCL	KCL	2 CDR2	raui
		0.489 1.570 (4.63)	0.014 0.036	0.706 4.720 (11.61)	0.017 0.081			X to IN OT to X
IN	× ×							
	° c		L to Z			Z to		
		t 0	<del>- 11-</del>	KCL	t O	Ť	KCL	C to X
		2.100 (18.10		*	4.60 (11.4		0.081	
Pin Name	Input Loading Factor (lu)							
от	2 2		H to Z			Z to	<del></del>	
С	4	10	H 10 Z	KCL	t O		KCL	
		1.90	<del>.  </del>		1.60		0.036	
Pin Name	Output Driving Factor (lu)	(18.1)		*	(11.4		0.036	
IN	36							





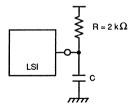
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

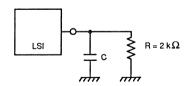
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-	-H8C-E	EO	Sheet 1/1

FUJI	<u>TSU CMOS GATE AR</u>	RAY UNIT	CELI	L SP	ECIFICA	ATION			" CG21K	" Version
Cell Name	Function									Number of B
H8CU	Tri-state Outp CMOS Interfac	ut Buffer e Input E	w/ N Buffei	oise r (Tı	e Limit rue) w/	Resista Pull-up	nce &	& sista	nce	9
Ce	il Symbol				Proj	pagation D	elay Pa	arame	ter	
,			ıp				in			Path
		10	KCI		t 0	KCL	KCI	2	CDR2	
	4	0.489 1.570 (4.63)	0.01 0.03	36	0.706 4.720 (11.61)	0.017 0.081				X to IN OT to X
ot	×									
	С	ļ	L to				Z to			
		t0	Ť		KCL	t O			KCL	C to X
		2.100 (18.10			*	4.600 (11.49			0.081	
Pin Name	Input Loading Factor (lu)	]								
от	2 2							L		
С	2	t O	H to		KCL	t O	Z to		KCL	
					NOL					
Pin Name	Output Driving Factor (lu)	1.900			*	1.600 (11.49			0.036	
IN	36									

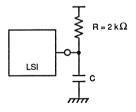


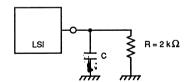


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

G21-	-H80	:U-	FO I	Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION									" CG21K" Version		
Cell Name	Function								Number of	f BC	
H8CD	Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-down Resistance								9		
Cel	l Symbol				Pro	agation D	elay Pa	aram	eter		
		tup t 0 KCL			tdn					Path	
			KCL		t 0	KCL	KCL2		CDR2		
IN —		0.489 1.570 (4.63)	0.01 0.03	6	0.706 4.720 (11.61)	0.017 0.081				X to IN OT to X	
от	от х		L to	7			Z to				
					T		KCL	t O		J L	KCL
		2.100 (18.10)			*	4.600 (11.49)		ı	0.081		
Pin Name	Input Loading Factor (lu)										
OT C	2 2	2				Н					
Ŭ	_	t O			KCL	t0		KCL			
						1.600 (11.49)		0.036			
Pin Name	Output Driving Factor (lu)	1.900 (18.10)			*			0.000			
IN	36										

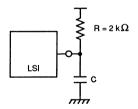


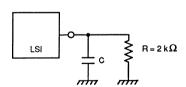


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8CD-E0 Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG2									" CG21F	(" Version
Cell Name	Function								Number of BO	
H8CF	Tri-state Output Buffer with Noise Limit Resistance & CMOS Interface Input Buffer (IOL=8mA, True)								9	
Cel	l Symbol	1			Prop	agation D	elay P	arame	eter	
			tup		tdn					Path
		t 0 KCL			t 0	KCL	KCL2 CDR2		CDR2	
	0.489 1.730 (4.79)	0.01 0.03	6	0.706 5.950 10.03)	0.017 0.048				X to IN OT to X	
и — и то	×									
		L to Z				Z to L				
		t O		KCL		t O		KCL	C to X	
			2.100 (20.30)		•	5.650 (9.99)		C	).051	
Pin Name	Input Loading Factor (lu)									
OT C	2 2	H to Z Z to H				Н				
	_	t O		KCL		t O		KCL		
		2.650				1.600		0	0.036	
Pin Name	Output Driving Factor (lu)	(20.30	(20.30)		•	(9.99)				
IN	36									

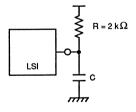


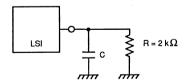


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8CF-E0 Sheet 1/1

EILIIT	CHICHOS CATE ADS	DAY LINIT	· CEL		DECITIO	ATION			" CC211	(" Version	
Cell Name	SU CMOS GATE ARE	TAT UNIT	UEL	L 3	LECIPIO/	ATION			CGZII		er of BC
H8CFU	Tri-state Output Interface Input Bu	Buffer w uffer (IO	/ Noi L=8n	se nA,	Limit Ro	esistano v/ Pull–i	e & up R	CM esis	IOS stance	Nume	
Cel	l Symbol	T									
		tu	ıp			to	in			D-4	
		t O	KC	L	t O	KCL	KCI	.2	CDR2	Pati	1
		0.489 1.730 (4.79)	0.01 0.03		0.706 5.950 (10.03)	0.017 0.048				X to II OT to	
от —	×										
		10	L to	o Z	KCL	t O	Zt	O L	KCL	C to >	,
	i i		2.100 (20.30)		*	5.650 (9.99)		(	0.051	0107	`
Pin Name	Input Loading Factor (lu)										
от	2 2							<u></u>			
С	2	H to Z				t O	Z to	ЭН	KCL		
1		10			KCL			<del> </del>			
Pin Name	Output Driving Factor (lu)	2.650 (20.30)			*	1.600 (9.99)		'	0.036		
IN	36										

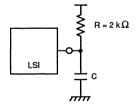


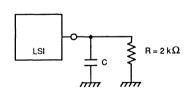


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8CFU-E0 Sheet 1/1

	ISU CMOS GATE AR	RAY UNII	CELL	SPECIFICA	ATION		CG21K	" Version			
Cell Name	Function							Number of B			
H8CFD	Tri-state Output Interface Input B							e 9			
Ce	Il Symbol		Propagation Delay Parameter								
		tı	ıp			dn		Path			
		t O	KCL	t 0_	KCL	KCL2	CDR2	raui			
IN	×	0.489 1.730 (4.79)	0.014 0.036		0.017 0.048			X to IN OT to X			
	c		L to	Z KCL	t O		KCL	C to X			
		2.100 (20.30		*	5.65( (9.99)	- 1	0.051				
Pin Name	Input Loading Factor (lu)										
от	2 2		H to	7		Z to h	,				
С	2	10	H to	KCL	t O		KCL				
			$\leftarrow$	NOL							
Pin Name	Output Driving Factor (lu)	2.650 (20.30		*	1.60 (9.99)	-	0.036				
IN	36										

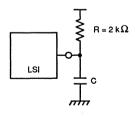


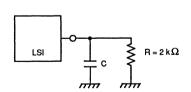


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21_H8CFD	-F0	Sheet 1	/1

FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL	SPECIFIC	ATION		" CG21k	(" Version
Cell Name	Function							Number of BC
H8E	Power Tri-state & CMOS Interfa	Output ace Inpu	Buffe t Buffe	r w/ Noise r (True)	e Limit I	Resis	tance	9
Cel	l Symbol			Pro	pagation D	elay Pa	rameter	
		tı	ıp		to	dn		Path
		t O	KCL	t O	KCL	KCL	2 CDR2	raui
	4	0.489 2.170 (4.21)	0.014 0.024		0.017 0.040			X to IN OT to X
от —	×							
		L to Z				Z to		0.1- 1/
		tO		KCL	t 0		KCL	C to X
		2.500 (20.90		*	6.75 (10.2		0.041	
Pin Name	Input Loading Factor (lu)							
OT C	2 2	<u></u>	H to Z			Z to	н	
J	_	t O		KCL	t O		KCL	
		3.50	0		1.80	0	0.025	
Pin Name	Output Driving Factor (lu)	(20.9		•	(10.2		0.020	
IN	36							





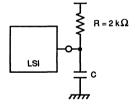
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

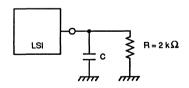
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H8E-E0	Sheet 1/1

	SU CMOS GATE AR	RAY UNIT	CEL	L S	PECIFIC/	ATION			" CG21K	(" Version
Cell Name	Function									Number of I
H8EU	Power Tri-stat CMOS Interfac	e Output e Input E	Buff Buffe	fer r (T	w/ Noise rue) w/	e Limit F Pull–up	Resis Res	stan sista	ce & ance	9
Cel	l Symbol									
		tı	ıρ			to	ln			Path
		t O	KC	L	t 0	KCL	KCI	2	CDR2	raui
IN	×	0.489 2.170 (4.21)	0.0		0.706 6.900 (10.30)	0.017 0.040				X to IN OT to X
		L to Z			t O	Z to	- I	KCL	C to X	
		2.500 (20.90			*	6.750 (10.24)		(	0.041	C 10 X
Pin Name	Input Loading Factor (lu)									
οT	2 2						لب			
С	2	H to Z		0 Z	KCL	t O	Z to	Н	KCL	
		t 0			NOL					
Pin Name	Output Driving Factor (lu)	3.500 (20.90			*	1.800 (10.24			0.025	
IN	36									

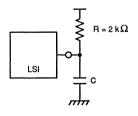


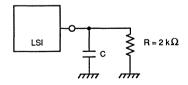


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8EU-E0 Sheet 1/1

FILIT	SU CMOS GATE ARE	RAY LINIT	CFL	LSI	PECIFICA	ATION			" CG21I	K"\	Version
Cell Name	Function	17 (T OT (T)	<u> </u>		2011 107	111011		1	002	<u> </u>	Number of BC
H8ED	Power Tri-state CMOS Interface	Output Input E	Buff Buffe	ier r (T	w/ Noise rue) w/	e Limit f Pull–do	Resis	star Res	nce & sistance		9
Cel	I Symbol	Propagation Delay Parameter									
		tu					in				Path
		t O	KC	L	t 0	KCL	KC	L2	CDR2		rauı
	4	0.489 2.170 (4.21)	0.02		0.706 6.900 (10.30)	0.017 0.040					X to IN OT to X
OT X											
		L to Z					Zt	٥L			
		t 0			KCL	t0		<b> </b>	KCL		C to X
		2.500 (20.90			*	6.750 (10.24)		'	0.041		
Pin Name	Input Loading Factor (lu)										
OT C	2 2			- 7			7.	<u> </u>			
	4	t 0			KCL	t O	21	Г	KCL		
					I.OL			-			
Pin Name	Output Driving Factor (lu)	3.500 (20.90			*	1.800 (10.24			0.025		
IN	36										





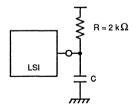
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

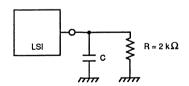
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C21-H8ED-E0 Sheet 1/1

FUJII	SU CMOS GATE AR	RAY UNII	CELL	SPECIFICA	ATION_		" CG21K	" Version			
Cell Name	Function							Number of B			
H8S	Tri-state Outp (CMOS Type,	ut & Sch True) wit	mitt T h Noi:	rigger Inpo se Limit R	ut Buffe esistan	r ce		13			
Cell	Symbol		Propagation Delay Parameter								
		tı	tup tdn								
		t O	KCL	t O	KCL	KCL2	CDR2	Path			
IN ————————————————————————————————————	×	1.314 1.570 (4.63)	0.060 0.036		0.045 0.081			X to IN OT to X			
	C		L to	Z		Z to L					
		t O		KCL	t O		KCL	C to X			
		2.10 (18.10		*	4.600 (11.49)		0.081				
Pin Name	Input Loading Factor (lu)										
OT	2 2			_							
С	2	10	H to	KCL	t O	Z to H	KCL				
				NOL							
Pin Name	Output Driving Factor (lu)	1.90		*	1.60 (11.4		0.036				
IN	18										

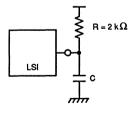


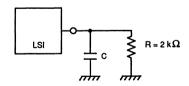


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21_H8S_F0	Sheet 1/1

	ISU CMOS GATE AR	MAT UNI	CELL	SPECIFICA	ATION		CGZII	C" Version			
Cell Name	Function							Number of B			
H8SU	Tri-state Outp , True) w/ Nois	ut & Sch e Limit F	mitt Tr lesista	igger Inp ince w/ P	ut Buffe ull–up F	r (CM Resista	OS Type ance	13			
Ce	I Symbol		Propagation Delay Parameter								
		tı	ıp		to	Jn .		Path			
		t O	KCL	t O	KCL	KCL2	CDR2	1.001			
IN	×	1.314 1.570 (4.63)	0.060 0.036		0.045 0.081			X to IN OT to X			
		to	L to	Z KCL	to	Z to	KCL	C to X			
		2.100 (18.10		•	4.60 (11.49		0.081				
Pin Name	Input Loading Factor (lu)										
от	2 2	<u> </u>	H to			Z to					
С	2	10	H 10	KCL	to	Z 10	KCL				
				NOL		$\overline{}$	***************************************				
Pin Name	Output Driving Factor (lu)	1.900		•	1.600 (11.49		0.036				
IN	18										





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8SU-E0 | Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELLS	SPECIFICA	ATION		" CG21K	" Version
Cell Name	Function							Number of BC
H8SD	Tri-state Outpo , True) w/ Nois	ut & Sch e Limit F	mitt Tri Resistar	gger Inp nce w/ P	ut Buffe ull–dow	r (CMO n Resis	S Type tance	13
Cel	Symbol			Pro	pagation D	elay Paran	neter	
			ıp qı	<u> </u>		in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		1.314 1.570 (4.63)	0.060 0.036	1.630 4.720 (11.61)	0.045 0.081			X to IN OT to X
OT —	×							
			L to Z		<u></u>	Z to L	1401	0 t- V
		t O		KCL	t O		KCL	C to X
		2.100 (18.10		*	4.60 (11.49		0.081	
Pin Name	Input Loading Factor (lu)	1						
от	2 2							
С	c 2		H to Z			Z to H	1401	
		10		KCL	t O		KCL	
	0.4.4845	1.900	).		1.600	)	0.036	

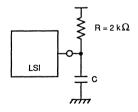
(18.10)

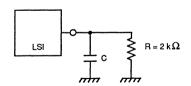
**Output Driving** 

Factor (lu)

Pin Name

IN



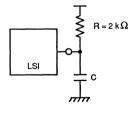


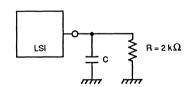
(11.49)

- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21	-HRSD-	FΛ	Sheet 1/1

	TSU CMOS GATE AR	( " Version Number of E							
Cell Name	Function	Function							
H8R	Tri-state Outp (TTL Type, Tru	Tri-state Output & Schmitt Trigger Input Buffer (TTL Type, True) with Noise Limit Resistance							
Ce	II Symbol	T	Propagation Delay Parameter						
	tup tdn					Path			
		t O	KCL	t O	KCL	KCL2	CDR2	Pain	
IN	×	1.182 1.570 (4.63)	0.060 0.036		0.062 0.081			X to IN OT to X	
	C	-	L to a	 Z		Z to	L		
		t O		KCL	t O		KCL	C to X	
		2.100 (18.10		•	4.60 (11.49		0.081		
Pin Name	Input Loading Factor (lu)	]							
OT	2 2	<u> </u>	H to	7	Z to H				
С	1 2	10	H to	KCL	10		KCL		
		1,900		1102	1.600	<del></del>	0.036		
Pin Name	Output Driving Factor (lu)	(18.10		*	(11.49		0.036		
IN	18								

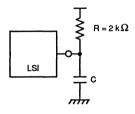


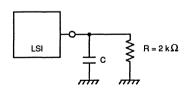


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8R-E0 Sheet 1/1

	SU CMOS GATE AF	(" Version						
Cell Name	Function							Number of B
H8RU	Tri-state Outp True) w/ Noise	ut & Schi Limit Re	mitt Trig	gger Inpo e w/ Pul	ut Buffe II–up Re	r (TTL sistan	Type, ce	13
Cel	Symbol			Pro	pagation D	elay Para	meter	
			ip.		to			Path
		t O	KCL	t O	KCL	KCL2	CDR2	
	4	1.182 1.570 (4.63)	0.060 0.036	1.967 4.720 (11.61)	0.062 0.081			X to IN OT to X
OT X								
		L to Z Z to L t 0 KCL t 0						
		10			t O		KCL	C to X
		2.100 (18.10		*	4.600 (11.49		0.081	
Pin Name	Input Loading Factor (lu)							
OT C	2 2	<b> </b>	H to Z			Z to H		
	_	t O	1 102	KCL	t O	21011	KCL	
		1.900			1.600		0.036	
Pin Name	Output Driving Factor (lu)	(18.10		*	(11.49		3.000	
IN	18							

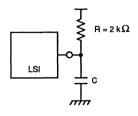


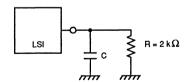


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

$\overline{c}$	21.	-H8RI	I_F0	Sheet 1/1

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL	SF	PECIFICA	ATION		" CG21	IK"	Version
Cell Name	Function									Number of BC
H8RD	Tri-state Output & Schmitt Trigger Input Buffer (TTL Type, True) w/ Noise Limit Resistance w/ Pull-down Resistance									13
Cel	l Symbol				Prop	pagation D	elay Pa	rameter		
		tı					ln			Path
		t O	KCL		t O	KCL	KCL	2 CDR2	↓_	
ла <del>—</del> Т		1.182 1.570 (4.63)	0.06 0.03		1.967 4.720 (11.61)	0.062 0.081				X to IN OT to X
от			L to				Z to			0. V
		t 0			KCL	t O		KCL	4	C to X
		2.100 (18.10			*	4.600 (11.49		0.081		
Pin Name	Input Loading Factor (lu)									
οT	2 2			. 7			Z to	U	-	
С		H to Z			KCL	t O	- Z 10	KCL	1	
		1.900	_			1.600		0.036	1	l
Pin Name	Output Driving Factor (lu)	(18.10			*	(11.49		0.036		
IN	18									·





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C21-H8RD-E0 | Sheet 1/1

### **Appendix A: General AC Specifications**

#### **Simulation Delay Specifications**

(Recommended Operating Conditions, Ta = 0 to 70°C, V<sub>DD</sub> = 5 V±5%

Delay Multipliers	Min.	Max.
Pre-layout Simulation	0.35	t <sub>maxB</sub>
Post-layout Simulation	0.40	t <sub>maxA</sub>

Junction Temperature (Tj)	tmaxB	tmaxA
Tj ≤ 60°C	1.65	1.55
60°C <tj 70°c<="" td="" ≤=""><td>1.70</td><td>1.60</td></tj>	1.70	1.60
70°C <tj 80°c<="" td="" ≤=""><td>1.75</td><td>1.65</td></tj>	1.75	1.65
80°C <tj 90°c<="" td="" ≤=""><td>1.80</td><td>1.70</td></tj>	1.80	1.70
90°C <tj 105°c<="" td="" ≤=""><td>1.85</td><td>1.75</td></tj>	1.85	1.75
105°C <tj 120°c<="" td="" ≤=""><td>1.90</td><td>1.80</td></tj>	1.90	1.80
120°C <tj 130°c¹<="" td="" ≤=""><td>1.95</td><td>1.85</td></tj>	1.95	1.85
130°C <tj 140°c²<="" td="" ≤=""><td>2.00</td><td>1.90</td></tj>	2.00	1.90
140°C <tj 150°c²<="" td="" ≤=""><td>2.05</td><td>1.95</td></tj>	2.05	1.95

NOTES: 1. This condition cannot be applied to devices in some plastic packages. If this condition is required for devices in plastic, please consult Fujitsu.

2. This condition cannot be applied to devices in plastic packages. If this condition is required even for ceramic packages, please consult Fujitsu.

Tj is determined by the following formula:

$$Ti = T_{aMAX} + \theta ia \times Pd (^{\circ}C)$$

where

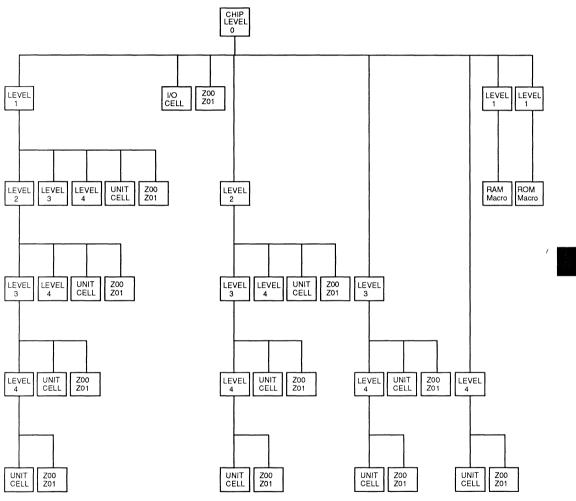
Тамах: Maximum Ambient Termperature (°C)

Thermal Resistance (°C/W). This value is determined for each package. θja: Pd:

Power dissipation (W). Please refer to Chapter 5 of Section 1 of this Data Book or the CG21

Design Manual for details.

### **Appendix B: Hierarchical Structure**



### **Appendix C: Estimation Tables for Metal Loading**

CG21303 (30K-gate-device) (Main Block)

	C <sub>L</sub> (lu)						
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4		
1	12.3	9.7	6.8	4.3	2.1		
2	18.5	14.4	10.3	6.6	3.2		
3	24.8	19.3	13.8	8.8	4.3		
4	29.0	22.7	16.1	10.3	5.1		
5	32.1	25.2	17.8	11.4	5.7		
6	34.6	27.1	19.2	12.3	6.1		
7	37.9	29.6	21.1	13.5	6.7		
8	39.4	30.9	21.8	14.0	6.9		
9	40.4	31.6	22.4	14.4	7.1		
10	41.4	32.5	23.0	14.7	7.3		
11	41.4	32.5	23.0	14.7	7.3		
12	42.0	32.8	23.3	14.9	7.4		
13	42.6	33.3	23.7	15.1	7.6		
14	43.6	34.2	24.3	15.5	7.7		
15	43.6	34.2	24.3	15.5	7.7		
16 – 30	47.2	37.0	26.3	16.7	8.3		
31 – 50	54.0	42.4	30.0	19.2	9.5		
51 – 75	55.6	43.5	30.9	19.7	9.8		
76 –100	61.1	47.8	33.8	21.7	10.8		

#### CG21303 (30K-gate-device) (Sub Block)

	C <sub>L</sub> (lu)					
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4		
1	5.8	4.1	2.7	1.2		
2	10.7	7.6	4.8	2.4		
3	15.6	11.0	7.1	3.5		
4	18.8	13.4	8.7	4.2		
5	21.3	15.1	9.7	4.7		
6	23.8	16.5	10.7	5.2		
7	25.2	18.3	11.8	5.8		
8	27.0	19.2	12.3	6.1		
9	27.9	19.7	12.6	6.2		
10	28.6	20.3	13.0	6.4		
11	28.6	20.3	13.0	6.4		
12	29.0	20.6	13.3	6.4		
13	29.6	20.9	13.5	6.6		
14	30.4	21.6	13.9	6.8		
15	30.4	21.6	13.9	6.8		
16 – 30	33.2	23.5	15.1	7.4		
31 – 50	38.5	27.4	17.5	8.7		
51 – 75	39.8	28.1	18.1	8.9		
76 – 100	44.00	31.2	19.9	9.9		

### 2

## **Appendix C: Estimation Tables for Metal Loading (Continued)**

#### CG21403 (40K-gate-device) (Main Block)

	C. /lu\						
			C <sub>L</sub> (lu)	<b>,</b>			
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4		
1	14.0	9.7	6.8	4.3	2.1		
2	21.1	14.4	10.3	6.6	3.2		
3	28.2	19.3	13.8	8.8	4.3		
4	33.1	22.7	16.1	10.3	5.1		
5	36.7	25.2	17.8	11.4	5.7		
6	39.5	27.1	19.2	12.3	6.1		
7	43.2	29.6	21.1	13.5	6.7		
8	45.0	30.9	21.8	14.0	6.9		
9	46.2	31.6	22.4	14.4	7.1		
10	47.3	32.5	23.0	14.7	7.3		
11	47.3	32.5	23.0	14.7	7.3		
12	47.9	32.8	23.3	14.9	7.4		
13	48.7	33.3	23.7	15.1	7.6		
14	49.9	34.2	24.3	15.5	7.7		
15	49.9	34.2	24.3	15.5	7.7		
16 – 30	54.0	37.0	26.3	16.7	8.3		
31 – 50	61.8	42.4	30.0	19.2	9.5		
51 – 75	63.6	43.5	30.9	19.7	9.8		
76 – 100	69.8	47.8	33.8	21.7	10.8		

### CG21403 (40K-gate-device) (Sub Block)

T T T T T T T T T T T T T T T T T T T	i i i i i i i i i i i i i i i i i i i							
	C <sub>L</sub> (lu)							
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4				
1	5.8	4.1	2.7	1.2				
2	10.7	7.6	4.8	2.4				
3	15.6	11.0	7.1	3.5				
4	18.8	13.4	8.7	4.2				
5	21.3	15.1	9.7	4.7				
6	23.3	16.5	10.7	5.2				
7	25.5	18.3	11.8	5.8				
8	27.0	19.2	12.3	6.1				
9	27.9	19.7	12.6	6.2				
10	28.6	20.3	13.0	6.4				
11	28.6	20.3	13.0	6.4				
12	29.0	20.6	13.3	6.4				
13	29.6	20.9	13.5	6.6				
14	30.4	21.6	13.9	6.8				
15	30.4	21.6	13.9	6.8				
16 – 30	33.2	23.5	15.1	7.4				
31 – 50	38.5	27.4	17.5	8.7				
51 – 75	39.8	28.1	18.1	8.9				
76 – 100	44.0	31.2	19.9	9.9				

### **Appendix C: Estimation Tables for Metal Loading (Continued)**

#### CG21503 (50K-gate-device) (Main Block)

	C <sub>L</sub> (lu)					
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4	
1	15.7	9.7	6.8	4.3	2.1	
2	23.7	14.4	10.3	6.6	3.2	
3	31.8	19.3	13.8	8.8	4.3	
4	37.3	22.7	16.1	10.3	5.1	
5	41.3	25.2	17.8	11.4	5.7	
6	44.5	27.1	19.2	12.3	6.1	
7	48.7	29.6	21.1	13.5	6.7	
8	50.7	30.9	21.8	14.0	6.9	
9	51.9	31.6	22.4	14.4	7.1	
10	53.3	32.5	23.0	14.7	7.3	
11	53.3	32.5	23.0	14.7	7.3	
12	53.9	32.8	23.3	14.9	7.4	
13	54.8	33.3	23.7	15.1	7.6	
14	56.1	34.2	24.3	15.5	7.7	
15	56.1	34.2	24.3	15.5	7.7	
16 – 30	60.7	37.0	26.3	16.7	8.3	
31 – 50	69.5	42.4	30.0	19.2	9.5	
51 – 75	71.5	43.5	30.9	19.7	9.8	
76 <b>–</b> 100	78.4	47.8	33.8	21.7	10.8	

#### CG21503 (50K-gate-device) (Sub Block)

	C <sub>L</sub> (lu)					
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4		
1	5.8	4.1	2.7	1.2		
2	10.7	7.6	4.8	2.4		
3	15.6	11.0	7.1	3.5		
4	18.8	13.4	8.7	4.2		
5	21.3	15.1	9.7	4.7		
6	23.3	16.5	10.7	5.2		
7	25.5	18.3	11.8	5.8		
8	27.0	19.2	12.3	6.1		
9	27.9	19.7	12.6	6.2		
10	28.6	20.3	13.0	6.4		
11	28.6	20.3	13.0	6.4		
12	29.0	20.6	13.3	6.4		
13	29.6	20.9	13.5	6.6		
14	30.4	21.6	13.9	6.8		
15	30.4	21.6	13.9	6.8		
16 – 30	33.2	23.5	15.1	7.4		
31 – 50	38.5	27.4	17.5	8.7		
51 – 75	39.8	28.1	18.1	8.9		
76 – 100	44.0	31.2	19.9	9.9		

## **Appendix C: Estimation Tables for Metal Loading (Continued)**

#### CG21753 (75-gate-device) (Main Block)

r	T				
			C <sub>L</sub> (lu)		
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	18.8	9.7	6.8	4.3	2.1
2	28.2	14.4	10.3	6.6	3.2
3	37.9	19.3	13.8	8.8	4.3
4	44.5	22.7	16.1	10.3	5.1
5	49.2	25.2	17.8	11.4	5.7
6	53.2	27.1	19.2	12.3	6.1
7	58.1	29.6	21.1	13.5	6.7
8	60.5	30.9	21.8	14.0	6.9
9	62.1	31.6	22.4	14.4	7.1
10	63.7	32.5	23.0	14.7	7.3
11	63.7	32.5	23.0	14.7	7.3
12	64.4	32.8	23.3	14.9	7.4
13	65.4	33.3	23.7	15.1	7.6
14	67.0	34.2	24.3	15.5	7.7
15	67.0	34.2	24.3	15.5	7.7
16 – 30	72.6	37.0	26.3	16.7	8.3
31 – 50	83.0	42.4	30.0	19.2	9.5
51 – 75	85.4	43.5	30.9	19.7	9.8
76 – 100	93.8	47.8	33.8	21.7	10.8

#### CG21753 (75-gate-device) (Sub Block)

<u></u>				
,	C <sub>L</sub> (lu)			
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	5.8	4.1	2.7	1.2
2	10.7	7.6	4.8	2.4
3	15.6	11.0	7.1	3.5
4	18.8	13.4	8.7	4.2
5	21.3	15.1	9.7	4.7
6	23.3	16.5	10.7	5.2
7	25.5	18.3	11.8	5.8
8	27.0	19.2	12.3	6.1
9	27.9	19.7	12.6	6.2
10	28.6	20.3	13.0	6.4
11	28.6	20.3	13.0	6.4
12	29.0	20.6	13.3	6.4
13	29.6	20.9	13.5	6.6
14	30.4	21.6	13.9	6.8
15	30.4	21.6	13.9	6.8
16 – 30	33.2	23.5	15.1	7.4
31 – 50	38.5	27.4	17.5	8.7
51 – 75	39.8	28.1	18.1	8.9
76 – 100	44.0	31.2	19.9	9.9

### **Appendix C: Estimation Tables for Metal Loading (Continued)**

#### CG21104 (100K- gate-device) (Main Block)

			C <sub>L</sub> (lu)		
NDI	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	21.9	9.7	6.8	4.3	2.1
2	32.8	14.4	10.3	6.6	3.2
3	44.1	19.3	13.8	8.8	4.3
4	51.8	22.7	16.1	10.3	5.1
5	57.2	25.2	17.8	11.4	5.7
6	61.8	27.1	19.1	12.3	6.1
7	67.6	29.6	21.1	13.5	6.7
8	70.4	30.9	21.8	14.0	6.9
9	72.1	31.6	22.4	14.4	7.1
10	74.0	32.5	23.0	14.7	7.3
11	74.0	32.5	23.0	14.7	7.3
12	75.0	32.8	23.3	14.9	7.4
13	76.1	33.3	23.7	15.1	7.6
14	77.9	34.2	24.3	15.5	7.7
15	77.9	34.2	24.3	15.5	7.7
16 – 30	84.4	37.0	26.3	16.7	8.3
31 – 50	96.5	42.4	30.0	19.2	9.5
51 – 75	99.2	43.5	30.9	19.7	9.8
76 – 100	109.0	47.8	33.8	21.7	10.8

#### CG21104 (100K- gate-device) (Sub Block)

		C <sub>L</sub> (1	lu)	
NDI	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	5.8	4.1	2.7	1.2
2	10.7	7.6	4.8	2.4
3	15.6	11.0	7.1	3.5
4	18.8	13.4	8.7	4.2
5	21.3	15.1	9.7	4.7
6	23.3	16.5	10.7	5.2
7	25.5	18.3	11.8	5.8
8	27.0	19.2	12.3	6.1
9	27.9	19.7	12.6	6.2
10	28.6	20.3	13.0	6.4
11	28.6	20.3	13.0	6.4
12	29.0	20.6	13.3	6.4
13	29.6	20.9	13.5	6.6
14	30.4	21.6	13.9	6.8
15	30.4	21.6	13.9	6.8
16 – 30	33.2	23.5	15.1	7.4
31 – 50	38.5	27.4	17.5	8.7
51 – 75	39.8	28.1	18.1	8.9
76 – 100	44.00	31.2	19.9	9.9

## Appendix D: Available Package Types

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
SDIP-64	Plastic	None	70 mil Lead Pitch	None	CG21103* CG21153* CG21203*	80 80 85	50 55 60
PLCC-68	Plastic	None	70 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	50 55 60	35 40 40
PLCC-84	Plastic	None	30 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	50 50 55	35 35 40
QFP-64	Plastic	None	100 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP-80	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP-100	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP-120	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	CG21303 CG21403 CG21503	65	40
					CG21103* CG21153* CG21203*	70	50
QFP-160	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	CG21303 CG21403 CG21503	59	39
					CG21153 CG21253	70	50
QFP-196**	Plastic	None	TBD Gull-wing	None	CG21503 CG21753 CG21104	TBD	TBD
QFP-232**	Plastic	None	TBD Gull-wing	None	CG21753 CG21104	TBD	TBD
QFP-176**	Plastic	None	TBD Gull-wing	None	CG21403 CG21503 CG21753	TBD	TBD
QFP-208**	Plastic	None	TBD Gull-wing	None	CG21403 CG21503 CG21753 CG21104	TBD	TBD
QFP-256**	Plastic	None	TBD Gull–wing	None	CG21104	TBD	TBD

Continued on next page

<sup>\*</sup> planned device \*\*package under development

## Appendix D: Available Package Types (Continued)

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
PG <b>A</b> -64	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21103* CG21153* CG21203*	40	20
PGA-88	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21103* CG21153* CG21203* CG21303	40	20
PGA-135	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	All CG21	30	15
PGA-179	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21203* CG21303 CG21403 CG21503 CG21753 CG21104	30 25	15 13
PGA-208	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21303 CG21403 CG21503 CG21753 CG21104	23	12
PGA-256	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21403 CG21503 CG21753 CG21104	19	9
PGA-299	Ceramic	Down	100 mil Pin Pitch Through hole	Yes	CG21503 CG21753 CG21104	19	9
PGA-321	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21753 CG21104	22-24	11-13
PGA-361	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21753 CG21104	22-24	11-13
PGA-401	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21104	22-24	11-13

## **Appendix E: TTL 7400 Function Conversion Table**

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
Name		Dusic Octio	Ociis
7400	Quad 2-input NAND	4 x N2N	4
7400	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7401			4
	Quad 2-input NOR	4 x R2N	
7403	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7404	Hex Inverter	6 x VIN	6
7405	Hex Inverter, Open Collector Outputs	R6B	5
7406	Hex Inverter/Buffer, Open Collector Outputs	R6B	5
7407	Hex Buffer, Open Collector Outputs	2 x N3N into R2N	5
7408	Quad 2-input AND	4 x N2P	8
7409	Quad 2-input AND, Open Collector Outputs	N8P	6
7410	Triple 3-input NAND	3 x N3N	6
7411	Triple 3-input AND	3 x N3P	9
7412	Triple 3-NAND, Open Collector Outputs	T33	7
7413	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7414	Hex Schmitt Trigger Inverter	6 x l 1R	48
7415	Triple 3-input AND, Open Collector Outputs	N8P to N2P	8
7413 7418		2 x (4 x I2R to N4N)	68
	Dual 4-input NAND, Schmitt Trigger		48
7419	Hex Schmitt Trigger Inverter	6 x l1R	
7420	Dual 4-input NAND	2 x N4N	4
7421	Dual 4-input AND	2 x N4P	6
7422	Dual 4-input NAND, Open Collector Outputs	2 x N4N + N2P	6
7423	Expanded Dual 4-input NOR with Strobe	R4P to D23 + R4P to R2N	9
7424	Quad Schmitt Trigger 2-input NAND	8 x I2R + 4 x N2N	68
7425	Dual 4-input NOR with Strobe	2 x (R4P + R2N)	8
7426	Quad 2-input NAND, High Voltage Output	4 x N2N	4
7427	Triple 3-input NOR	3 x R3N	6
7428	Quad 2-input NOR Buffer	4 x R2N	4
7430	8-input NAND	N8B	6
7432	Quad 2-input OR	4 x R2P	8
7433	Quad 2-input NOR Buffer, Open Collector	4 × 1121	Ŭ
7433	Outputs	4 x R2N + N4P	7
7434	4	6 x B1N	6
	Hex Noninverter	- · · · · · · · · · · · · · · · · · · ·	5
7435	Hex Noninverter with Open Collector Outputs	2 x N3N into R2N	-
7437	Quad 2-input NAND Buffer	4 x N2B	12
7438/9	Quad 2-input NAND Buffer, Open Collector		
	Outputs	4 x N2N + N4P	7
7440	Dual 4-input NAND Buffer	2 x N4B (N4N if not power)	8(4
7442	BCD to Decimal Decoder	4 x V2B + 10 x N4N	24
7443	EX3 to Decimal Decoder	4 x V2B + 10 x N4N	24
7444	4 to 10 Line Decoder	4 x V2B + 10 x N4N	24
7445	BCD to Decimal Decoder/driver (30V)	4 x V2B + 10 x N4N	24
7446	BCD to 7-segment Decoder/Driver (30V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7447	BCD to 7—segment Decoder/Driver (15V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7448	BCD to 7–segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7449	BCD to 7–segment, Open Collector Outputs	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7449 7450		D36 + D24	5
	Dual 2-input, 2-wide AOI (One Expandable)		4
7451	AOI	2 x D24	
7452	Expandable 4-wide AND-OR	N3N + D36 + V1N into N3N	8
7453	Expandable 4-wide AOI	D36 + D23 into N2P	7
7454	4-wide AOI	2 x N3N + 2 x N2N + N4N + V1N	9
7455	2-wide 4-input AOI	T42	6
7460	Dual 4-input Expander	2 x N4P	6
7461	Triple 3-input Expander	3 x N3P	6
7462	4-wide AND-OR Expander	2 x N3N + 2 x N2N + N4N	8
7464	4-2-3-2 AOI	T54	10
7465	4-2-3-2 AOI (Open Collector)	T54	10

## Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7470	AND-gated positive-edge JK FF with Preset		
	and Clear	3 x V1N + 2 x N3N + N2N + R2N + FJD	21
	or:	FD4 + 2 x N2N + R2N + V1N + R2P + D24	17
7471	AND-gated RS M/S FF with Preset	TOTTE X HERT TILLET THE TOET	
7471	and Clear	FD4 + 2 x N3N + 2 x D23 + 2 x V1N	19
	or:	LT1+ 2 x N4N + N2P	10
7472	AND-gated JK M/S FF with Preset	LITTE A 19414 T NEF	10
14/2	and Clear	V1N + 2 x N3N + N2N + R2N + FJD	19
	or:	FD4 + N3P + N3N + V1N + D24	17
7473	Dual JK FF with Clear	2 x FJD	24
7474	Dual positive-edge D-FF with Preset and	2 × 1 0 D	24
1414	Clear	2 x FDP	16
7475	4-bit Bistable Latch	LTM	16
7475	Dual JK FF with Preset and Clear	2 x (FJD + N2N + R2N + V1N)	30
7477	4-bit Bistable Latch	LTM	16
7477	Dual JK FF with Preset and Common	2 x (FJD + N2N + R2N + V1N)	30
7470	Clear and Clock	2 x (F00 + N2N + H2N + V IN)	30
7480	Gated Full Adder	A1N	8
7480 7482	2-bit Binary Full Adder	AIN A2N	8 16
7482	4-bit Binary Full Adder with Fast Carry	A4H	48
7483 7484		MC4	
	4-bit Magnitude Comparator		42
7486	Quad 2-input XOR	4 x X2N	12
7487	4-bit True/Complement Zero/One Element	4 x N2N + V1N + 4 x N2N	17
7489	64-bit (16 x 4) Memory	2 x DE6 + V1N + 16 x LT4	298
~		+ 5 x (V2B + T5A) + 10 x V2B	
7490	Decade Counter	2 x (FDP + FDO + N2P + N2N + R2N) + V1N	39
	(Different Implementation)	4 x N2P + 2 x R2P + N2N + C41 + LT1	41
7491	8-bit Shift Register	2 x FDS + V1N	41
7492	Divide-by-12 Counter	4 x FDO + 2 x V1N + 2 x R2N + N2N	33
7493	4-bit Binary Counter	C41 + N2N (for the resets)	25
7494	4-bit Shift Register, 2 asynchronous Presets	FS3	34
	4-bit Shift Register, 2 asynchronous		
	Presets, Full Implementation	4 x FDP + 4 x D24 + 2 x V1N	42
7495	4-bit Parallel-access Shift Register	FS2 + D24 + 2 x V1N	34
7496	5-bit Shift Register	5 x FDP + 5 x N2N + V1N(clock)	46
7497	Synch 6-bit Binary Rate Multiplier	FDR + 2 x FDO + 3 x V1N + 2 x N2N	122
		+ 2 x N3N + 2 x N4N + 5 x N6B + 3 x N8B	
		+ R2B + X2N + 5 x X1B.	
7498	4-bit Data Selector/Storage Register	FDQ + T2F + 4 x V1N	33
7499	4-bit Universal Shift Register	FS2 + LTK + 2 x D24 + 4 x V1N	42
74100	8-bit Bistable Latch	2 x YL4 + 2 x V1N	30
74101	AO-gated JK Negative-Edge FF,		
	with Preset	FD3 + V1N + 3 x D24	15
74102	AND-gated JK Negative-Edge FF with		
	Preset and Clear	FD4 + D24 + N3P + N3N	16
74103	Dual JK FF with Clear	2 x FJD + 2 x V1N (for clock)	26
	or:	2 x (FD5 + D24 + V1N)	22
74106	Dual JK Negative-Edge FF with Preset		
	and Clear	2 x (FD4 + D24 + V1N)	24
74107	Dual JK FF with Clear	2 x (FJD + 2 x V1N)	22
74108	Dual JK Negative-Edge FF with Preset	·	
	and Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74109	Dual JK Positive-Edge FF with Preset and	•	
	Clear	2 x (FDP + V1N + D24)	22
74110	AND-gated JK M/S FF with Data	•	
	Lockout	FDP + D24 + N3P + N3N	15
74111	Dual JK M/S FF with Data Lockout	2 x (FDP + D24 + V1N)	22
74112	Dual JK Negative-Edge FF with Preset	, · · · · · /	
	and Clear	2 x (FD4 + D24 + V1N)	24
		=, = =	

## Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74113 74114	Dual JK Negative-Edge FF with Preset Dual JK Negative-Edge FF with Preset and	2 x (FD3 + D24 + V1N)	22
	Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74116	Dual 4-bit Latch with Clear	2 x LTM	32
74120	Dual Pulse Synchronizer/Driver	2 x (N2P + LT1 + 4 x N3N + 2 x N2N + 2 x V1N)	36
74125	Quad Bus Buffer with 3-state Output	B41	9
74126	Quad Bus Buffer with 3-state Output	B41 + 4 x V1N	13
74132	Quad 2-input NAND Schmitt Trigger	4 x (2 x I2R + N2N)	68
74133 74134	13-input NAND 12-input NAND with 3-state Outputs	2 x N4N + N3N + N2N into R4P NCB + O4R	10 15
74134	Quad 3-input EXOR/EXNOR	4 x X4N	20
74136	Quad 2-input EXOR with Open-Collector Outputs	4 x X2N + R4N	14
74137	3-line to 8-line Decoder with Address	4 X AZN + N4N	14
1,413,	Latch	3 x LTK into DE6	42
74138	3-line to 8line Decoder with Enable	DE6	30
74139	Dual 2-line to 4-line Decoder	2 x DE4	16
74141	BCD-to-Decimal Decoder	4 x V2B + 10 x N4N	24
74145	BCD-to-decimal Decoder	4 x V1N + 10 x N4N	24
74147	10-line to 4-line BCD Priority Encoder	3 x N4N + 3 x N3N + 2 x N2N + 2 x N2P	36
1	•	+ 3 x R2N + R4N + 13 x V1N	
74148	8-line to 3-line Octal Priority Encoder	N9B + 2 x N2N + R2P + R4N + 4 x N3N + 2 x N4N + G44 + 12 x V1N	40
74150	1-to-16 Multiplexer	DE3 + 2 x U28 + D24 + 2 x V1N	41
74151	1-to-8 Multiplexer with Strobe	DE3 + U28 + N2N + V1N	28
74152	1-to-8 Multiplexers	DE3 + U28	26
74153	Dual 4-line to 1-line Selector/Multiplexer	DE2 + 2 x U24 + 2 x R2N	19
74154	4-line to 16-line Decoder/Demultiplexer or:	2 x DE6 + V1N 2 x DE4 + N2P + 16 x R2P	61 50
74155	Dual 2-line to 4-line Decoder/Demultiplexer (Totem Pole)	8 x N3N + 2 x R2N + 5 x V1N	23
74156	Dual 2-line to 4-line Decoder/Demultiplexer (Open Collector)	8 x N3N + 2 x R2N + 5 x V1N	23
74157	Quad 2-line to 1-line multiplexer	T2F + 4 x R2N + B1N	13
74158	Quad 2-line to 1-line multiplexer		
	(Inverter Data Outputs)	4 x D24 + V1N + 2 x R2N	11
74159	4-line to 16-line Demultiplexer	2 x DE6 + V1N (without open collector)	50
74160	Synchronous 4-bit Counter	4 x C11 + K1B + 2 x V2B + V1N + B1N+	62
74161	(Decimal with Direct Clear) Synchronous 4-bit Counter (Binary	N2K + 2 x R3N + R4N + 3 x R2N + N2N	
74100	with Direct Clear)	C43	48
74162	Synchronous 4-bit Counter (Decimal with Synchronous Clear)	C45 + D36 + N3P + 2 x R2N + B1N	57
74163	Synchronous 4-bit Counter (Binary with Synchronous Clear)	C45	48
74164	8-bit Parallel Output Serial Shift	a v EDD . NOD	£.4
74165	Register, Asynchronous Clear 8-bit Shift Register	2 x FDR + N2P 2 x FDS + 8 x D24 + 11 x V1N + K4B + R2P	54 71
74165	8-bit Shift Register	2 x FDS + 8 x D24 + 11 x V IN + K4B + H2P 2 x FDR + 8 x D24 + 10 x V1N + K4B	80
74168	4-bit Up/Down Synchronous Counter	2 X FUT + 0 X U24 + 10 X V IN + N4D	60
74100	(Decade)	4 x C11 + 4 x T32 + 7 x N2N + 2 x N3N + R2N + 7 x V2B + K1B	85
74169	4-bit Up/Down Synchronous Counter	TO TEST TIME	
1	(Binary)	C47	68
74170	4-by-4 Register File	4 x (YL4 + B1N + V1N + U24) + 2 x DE4	104
74171	Quad D-FF with Clear	FDR + 4 x V1N	30
74172	16-bit (8 x 2) Register File	3 x DE6 + 4 x FDS + 16 x (N2N + G34 +	348
		+ V1N + 2 x R2P + 4 x U28) + 2 x V1N + 2 x R2P	

### Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74173	4-bit D-type Register		
	(3-state Output)	FDR + 2 x R2N + B41 + 6 x V1N + K1B + 4 x D24	53
74174	Hex D-FF (Single Output)	FDR + 2 x FDO	40
74175	Quad D-FF (with Clear)	FDR + 4 x V1N	30
74176	Presettable Decade/Binary Counter	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74177	Presettable Binary Counter	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74178	4-bit Universal Shift Register	FS2	30
74179	4-bit Universal Shift Register		
	(Direct Clear)	FS2 + 9 x N2N + B1N	40
74180	9-bit Odd/Even Parity Checker	PO8 + 2 x D24 + V1N	23
74181	ALU/Function Generator	5 x V1N + 5 x T32 + 4 x D36 + 8 x X2N + 3 x T54 +	
		N6B + N4B + 2 x N2N + 2 x N4P	113
74182	Look-ahead Carry Generator	R4P + 2 x V1N + 2 x T44 + T33 + D24	36
74183	Dual Carry-save Full Adder	2 x A1N	16
74184	BCD-to-binary Code Converter	These devices are ROM based	
74185	Binary-to-BCD Code Converter	These devices are ROM based	
74190	Synch Up/Down Counter (BCD)	4 x FDP + 4 x X2N + K1B + 3 x V1N + 3 x N3N	
74100	Synon oproduit counter (Dob)	+ 9 x N2N + 2 x T32 + T43	
74191	Synch Up/Down Counter (Binary)	C47	68
74192	Up/Down Dual Clock Counter (BCD)	4 x C11 + 4 x V2B + N6B + 2 x N3N + R2N	79
	-p	+ T32 + T42 + T43	
74193	Up/Down Dual Clock Counter (Binary)	4 x C11 + 2 x N6B + 4 x V2B + R2N + D24 + T32 + T42	72
74194	4-bit Bidirectional Universal Shift Register	FDR + 6 x V1N + R2N + 4 x D36 + D23 + B1N	48
74195	4-bit Parallel Access Shift Register	FS2 + D24 + 2 x V1N	34
74196	Preset Decade/Binary Counter/Latch	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74197	Preset Binary Counter/Latch	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74198	8-bit Bidirectional Universal Shift Register	2 x FDR + D24 + 10 x V1N + R2N + 8 x D36	89
74199	8-bit Bidirectional Universal Shift		
	Register (JK Serial Input)	2 x FS2 + D24 + 3 x V1N + B1N + R2N + 8 x N2P	83
	or:	2 x FDR + 7 x D24 + T33 + 11 x V1N + R2N	85
74246	BCD-to-7-Segment Decoder/Driver		
	(30V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74247	BCD-to-7-Segment Decoder/Driver	A MANA AA MANA AA MANA A MAD D MAD	
74040	(15V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74248	BCD-to-7-Segment Decoder/Driver	A MAN. AA NON. AO NON. A NOD. O NOD.	
74040	(Internal Pull-up)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74249	BCD-to-7-Segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74060	(Open Collector)	2 x R6B	10
74260 74265	Dual 5-input NOR Quad Complementary Output Element	2 X H6B B1N + V1N	10
74265 74266	Quad Complementary Output Element Quad 2–EXNOR, Open Collector	4 x X1N	12
74266	Octal D-type FF with Clear		12 52
74273	Quad J–K FF	2 x FDR 4 x (FDP + V1N + D24) + 2 x B1N	46
74276	BCD-to-7-Segment Decoder/Driver	4 x (FDP + V1N + D24) + 2 x B1N 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	46 53
14341	BOD-to-7-Segment Decoder/Driver	4 A V 114 + 11 A 14214 + 10 A 14314 + 4 A 143P + 3 X 142P	

## Appendix F: Alphanumeric Index of Unit Cells

Name	Function	Page No.
A1A	1-bit Half Adder	3–253
A1N	1-bit Full Adder	3–254
A2N	2-bit Full Adder	3-255
A4H	4-bit Binary Full Adder with Fast Carry	3–257
BD3	Delay Cell	3–10
BD4	Delay Cell	3–11
BD5	Delay Cell	3–12
BD6	Delay Cell	3–13
B1N	True Buffer	3–9
B11	1-bit Bus Driver	3–319
B12	1-bit Block Bus Driver	3–323
B21	2-bit Bus Driver	3–320
B22	2-bit Block Bus Driver	3–324
B41	4-bit Bus Driver	3–321
B42	4-bit Block Bus Driver	3-325
B81	8-bit Bus Driver	3–322
C11	Non-Scan Flip-flop for Counter	3–231
C41	Non-Scan 4-bit Binary Asynchronous Counter	3-233
C42	Non-Scan 4-bit Binary Synchronous Counter	3–236
C43	Non-Scan 4-bit Binary Synchronous Up Counter	3–239
C45	Non-Scan 4-bit Binary Synchronous Up Counter	3–243
C47	Non-Scan 4-bit Binary Synchronous Up/Down Counter	3–247
DE2	2:4 Decoder	3–248
DE3	3:8 Decoder	3–299
DE4	2:4 Decoder with Enable	3–301
DE6	3:8 Decoder with Enable	3–302
D14	2-wide 3-AND 4-Input AOI	3–68
D23	2-wide 2-AND 3-Input AOI	3–67
D24	2-wide 2-AND 4-Input AOI	369
D34	3-wide 2-AND 4-Input AOI	3–70
D36	3-wide 2-AND 6-Input AOI	3–71
D44	3-wide 2-OR 2-AND 4-Input AOI	3–72
FDM	Non-Scan D Flip-flop	3–183
FDN	Non-Scan D Flip-flop with Set	3–185
FDO	Non-Scan D Flip-flop with Reset	3–187
FDP	Non-Scan D Flip-flop with Set and Reset	3–189
FDQ	Non-Scan 4-bit D Flip-flop	3–192
FDR	Non-Scan 4-bit D Flip-flop with Clear	3–194
FDS	Non-Scan 4-bit D Flip-flop	3–197
FD2	Non-Scan Power D Flip-flop	3–199
FD3	Non-Scan Power D Flip-flop with Preset	3–201

Name	Function	Page No.
FD4	Non-Scan Power D Flip-flop with Clear and Preset	3-203
FD5	Non-Scan Power D Flip-flop with Clear	3-205
FJD	Non-Scan Positive Edge Clocked Power J-K FK with Clear	3-207
FS1	4-bit Serial-in Parallel-out Shift Register	3-279
FS2	4-bit Shift Register with Synchronous Load	3-281
FS3	4-bit Shift Register with Asynchronous Load	3-283
G14	2-wide 3-OR 4-Input OAI	3–76
G23	2-wide 2-OR 3-Input OAI	3–75
G24	2-wide 2-OR 4-Input OAI	3–77
G34	3-wide 2-OR 4-Input OAI	3–78
G44	2-wide 2-AND 2-OR 4-Input OAI	3–79
H6C	3-state Output (I <sub>OL</sub> = 3.2 mA) and CMOS Interface Input Buffer (True)	3–398
H6CD	H6C with Pull-down Resistance	3–400
H6CF	3-state Output and CMOS Interface Input Buffer (I <sub>OL</sub> = 8 mA,True)	3–401
H6CFD	H6CF with Pull-down Resitance	3–403
H6CFU	H6CF with Pull-up Resistance	3-402
H6CU	H6C with Pull-up Resistance	3–399
H6E	Power 3-state Output (I <sub>OL</sub> = 12 mA) and CMOS Interface Input Buffer (True)	3-404
H6ED	H6E with Pull-down Resistance	3–406
H6EU	H6E with Pull-up Resistance	3-405
H6R	3-state Output (I <sub>OL</sub> = 3.2 mA) and Schmitt Trigger Input Buffer (TTL type, True)	3–410
H6RD	H6R with Pull-down Resistance	3–412
H6RU	H6R with Pull-up Resistance	3-411
H6S	3-state Output (I <sub>OL</sub> = 3.2 mA) and Schmitt Trigger Input Buffer (CMOS type, True)	3–407
H6SD	H6S with Pull-down Resistance	3-409
H6SU	H6S with Pull-up Resistance	3–408
H6T	3-state Output (I <sub>OL</sub> = 3.2 mA) and Input Buffer (True)	3–389
H6TD	H6T with Pull-down Resistance	3–391
H6TF	3-state Output and Input Buffer (I <sub>OL</sub> = 8 mA, True)	3–392
H6TFD	H6TF with Pull-down Resistance	3–394
H6TFU	H6TF with Pull-up Resistance	3–393
H6TU	H6T with Pull-up Resistance	3–390
H6W	Power 3-state Output (I <sub>OL</sub> = 12 mA) and Input Buffer (True)	3–395
H6WD	H6W with Pull-down Resistance	3–397
H6WU	H6W with Pull-up Resistance	3–396
H8C	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA) with Noise Limit Resistance and CMOS Interface Input Buffer (True)	3–422
H8CD	H8C with Pull-down Resistance	3-424
H8CF	3-state Output Buffer with Noise Limit Resistance and CMOS	- ·-·
	Interface Input Buffer (I <sub>OL</sub> = 8 mA, True)	3-425
H8CFD	H8CF with Pull-down Resistance	3-427
H8CFU	H8CF with Pull-up Resistance	3-426

Name	Function	Page No.
H8CU	H8C with Pull-up Resistance	3-423
H8E	Power 3-state Output Buffer (I <sub>OL</sub> = 12 mA) with Noise Limit Resistance and	
	CMOS Interface Input Buffer (True)	3-428
H8ED	H8E with Pull-down Resistance	3-430
H8EU	H8E with Pull-up Resistance	3-429
H8R	3-state Output and Schmitt Trigger Input Buffer (TTL type, True)	
	with Noise Limit Resistance	3–434
H8RD	H8R with Pull-down Resistance	3–436
H8RU	H8R with Pull-up Resistance	3–435
H8S	3-state Output and Schmitt Trigger Input Buffer (CMOS type, True) with Noise Limit Resistance	0.404
H8SD	H8S with Pull-down Resistance	3–431 3–433
H8SU		3–433 3–432
H8T	H8S with Pull-up Resistance	3–432 3–413
H8TD	3-state Output with Noise Limit Resistance and Input Buffer (True) H8T with Pull-down Resistance	3-415 3-415
H8TF	3-state Output with Noise Limit Resistance and Input Buffer (I <sub>OI</sub> = 8 mA, True)	3–415 3–416
H8TFD	H8TF with Pull-down Resistance	3–418
H8TFU	H8TF with Pull-up Resistance	3–416 3–417
H8TU	H8T with Pull-up Resistance	3–417
H8W	Power 3-state Output with Noise Limit Resistance and Input Buffer (True)	3-414
H8WD	H8W with Pull-down Resistance	3–421
H8WU	H8W with Pull-up Resistance	3–420
IKB	Clock Input Buffer (Inverter)	3-341
IKBD	IKB with Pull-down Resistance	3–343
IKBU	IKB with Pull-up Resistance	3–342
IKC	CMOS Interface Clock Input Buffer (Inverter)	3–344
IKCD	IKC with Pull-down Resistance	3–346
IKCU	IKC with Pull-up Resistance	3–345
ILB	Clock Input Buffer (True)	3–347
ILBD	ILB with Pull-down Resistance	3–349
ILBU	ILB with Pull-up Resistance	3–348
ILC	CMOS Interface Clock Input Buffer (True)	3–350
ILCD	ILC with Pull-down Resistance	3–352
ILCU	ILC with Pull-up Resistance	3–351
I1B	Input Buffer Inverter	3–335
I1BD	I1B with Pull-down Resistance	3–337
I1BU	I1B with Pull-up Resistance	3–336
I1C	CMOS Interface Input Buffer (Inverter)	3–353
I1CD	I1C with Pull-down Resistance	3–355
I1CU	I1C with Pull-up Resistance	3-354
I1R	Schmitt Trigger Input Buffer (TTL Type, Inverter)	3–365
I1RD	I1R with Pull-down Resistance	3–367

Name	Function	Page No.
I1RU	I1R with Pull-up Resistance	3–366
I1S	Schmitt Trigger Input Buffer (CMOS Type, Inverter)	3–359
I1SD	I1S with Pull-down Resistance	3–360
I1SU	I1S with Pull-up Resistance	3–361
I2B	Input Buffer (True)	3–338
I2BD	I2B with Pull-down Resistance	3–340
I2BU	I2B with Pull-up Resistance	3–339
I2C	CMOS Interface Input Buffer (True)	3–356
I2CD	I2C with Pull-down Resistance	3–358
I2CU	I2C with Pull-up Resistance	3–357
I2R	Schmitt Trigger Input Buffer (TTL Type, True)	3–368
I2RD	I2R with Pull-down Resistance	3–370
I2RU	I2R with Pull-up Resistance	3–369
128	Schmitt Trigger Input Buffer (CMOS Type, True)	3–362
I2SD	I2S with Pull-down Resistance	3–364
I2SU	I2S with Pull-up Resistance	3–363
KAB	Block Clock (OR) Buffer	3–110
KBB	Block Clock Buffer(OR x 10)	3–111
KDB	Block Clock Buffer(OR x 10)	3–113
KEB	Block Clock Buffer	3–115
K1B	True Clock Buffer	3–105
K2B	Power Clock Buffer	3–106
K3B	Gated Clock (AND) Buffer	3–107
K4B	Gated Clock (OR) Buffer	3–108
K5B	Gated Clock (NAND) Buffer	3–109
LTK	Data Latch	3–265
LTL	1-bit Data Latch with Clear	3–267
LTM	4-bit Data Latch with Clear	3–269
LT1	S-R Latch with Clear	3–272
LT4	4-bit Data Latch	3–274
MC4	4-bit Magnitude Comparator	3–315
NCB	Power 12-Input NAND	3–27
NGB	Power 16-Input NAND	3–28
N2B	Power 2-Input NAND	3–18
N2K	Power 2-Input NAND	3–19
N2N	2-Input NAND	3–17
N2P	Power 2-Input AND	3–45
N3B	Power 3-Input NAND	3–21
N3N	3-Input NAND	3–20
N3P	Power 3-Input AND	3–46
N4B	Power 4-Input NAND	3–23

Name	Function	Page No.
N4N	4-Input NAND	3–22
N4P	Power 4-Input AND	3-47
N6B	Power 6-Input NAND	3-24
N8B	Power 8-Input NAND	3–25
N8P	Power 8-Input AND	3-48
N9B	Power 9-Input NAND	3–26
O1B	Output Buffer (I <sub>OL</sub> = 3.2 mA, Inverter)	3–371
O1BF	Output Buffer (I <sub>OL</sub> = 8 mA, Inverter)	3–372
O1L	Power Output Buffer (I <sub>OL</sub> = 12 mA, Inverter)	3–373
O1R	Output Buffer (I <sub>OL</sub> = 3.2 mA, Inverter) with Noise Limit Resistance	3–374
O1RF	Output Buffer (I <sub>OL</sub> = 8 mA, Inverter) with Noise Limit Resistance	3–375
018	Power Output Buffer (I <sub>OL</sub> = 12 mA, Inverter) with Noise Limit Resistance	3–376
O2B	Output Buffer (I <sub>OL</sub> = 3.2 mA, True)	3–377
O2BF	Output Buffer (I <sub>OL</sub> = 8 mA, True)	3–378
O2L	Power Output Buffer (I <sub>OL</sub> = 12 mA, True)	3–379
O2R	Output Buffer (I <sub>OL</sub> = 3.2 mA, True) with Noise Limit Resistance	3–380
O2RF	Output Buffer (I <sub>OL</sub> = 8 mA, True)with Noise Limit Resistance	3–381
O2S	Power Output Buffer (I <sub>OL</sub> = 12 mA, True) with Noise Limit Resistance	3–382
O4R	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA, True) with Noise Limit Resistance	3–386
O4RF	3-state Output Buffer (I <sub>OL</sub> = 8 mA, True) with Noise Limit Resistance	3–387
O4S	Power 3-state Output Buffer (I <sub>OL</sub> = 12 mA, True) with Noise Limit Resistance	3–388
O4T	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA, True)	3–383
O4TF	3-state Output Buffer (I <sub>OL</sub> = 8 mA, True)	3–384
O4W	Power 3-state Output Buffer (I <sub>OL</sub> = 12 mA, True)	3–385
PE5	5-bit Even Parity Generator/Checker	3–291
PE8	8-bit Even Parity Generator/Checker	3-293
PE9	9-bit Even Parity Generator/Checker	3-295
PO5	5-bit Odd Parity Generator/Checker	3-292
PO8	8-bit Odd Parity Generator/Checker	3-294
PO9	9-bit Odd Parity Generator/Checker	3–296
P24	4-wide 2:1 Data Selector	3–297
RCB	Power 12-Input NOR	3–41
RGB	Power 16-Input NOR	3-42
R2B	Power 2-Input NOR	3–32
R2K	Power 2-Input NOR	3–33
R2N	2-Input NOR	3–31
R2P	Power 2-Input OR	3–51
R3B	Power 3-Input NOR	3–35
R3N	3-Input NOR	3–34
R3P	Power 3-Input OR	3–52
R4B	Power 4-Input NOR	3–37

١	lame	Function	Page No.
F	R4N	4-Input NOR	3–36
F	R4P	Power 4-Input OR	3-53
F	R6B	Power 6-Input NOR	3–38
F	R8B	Power 8-Input NOR	3–39
F	R8P	Power 8-Input OR	3–54
F	R9B	Power 9-Input NOR	3–40
S	SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	3–211
S	SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	3–216
S	SC43	Scan 4-bit Synchronous Binary Up Counter with Asynchronous Clear	3–221
S	SC47	Scan 4-bit Synchronous Binary Up/Down Counter	3–225
S	SDA	Scan 1-Input D Flip-flop with Clock Inhibit	3–137
S	SDB	Scan 1-Input 4-bit D Flip-flop with Clock Inhibit	3–140
S	SDD	Scan 2-Input D Flip-flop with Clear, Preset, and Clock Inhibit	3–133
S	SDH	Scan 2-Input D Flip-flop with Clear and Clock Inhibit	3–121
S	SDJ	Scan 4-Input D Flip-flop with Clear and Clock Inhibit	3–124
S	SDK	Scan 6-Input D Flip-flop with Clear and Clock Inhibit	3–127
S	SFDM	Scan 1-Input D Flip-flop with Clock Inhibit	3–159
S	SFDO	Scan 1-Input D Flip-flop with Clear and Clock Inhibit	3–162
S	SFDP	Scan 1-Input D Flip-flop with Clear, Preset, and Clock Inhibit	3–165
S	SFDR	Scan 4-Input D Flip-flop with Clear and Clock Inhibit	3–169
S	SFDS	Scan 4-Input D Flip-flop with Clock Inhibit	3–173
S	SFJD	Scan J-K Flip-flop with Clock Inhibit	3–177
S	SHA	Scan 1-Input 8-bit D Flip-flop with Clock Inhibit	3–144
S	SHB	Scan 1-Input 8-bit D Flip-flop with Clock Inhibit and Q Output	3–147
5	SHC	Scan 1-Input 8-bit D Flip-flop with Clock Inhibit and XQ Output	3–150
5	SHJ	Scan 8-bit D Flip-flop with Clock Inhibit and 2-to-1 Data Multiplexer	3–153
	SHK	Scan 8-bit D Flip-flop with Clock Inhibit and 3-to-1 Data Multiplexer	3–156
5	SJH	Scan J–K Flip-flop with Clear and Clock Inhibit	3–130
5	SR1	Scan 4-bit Serial-in Parallel-out Shift Register with Scan	3–286
٦	Г2B	2:1 Selector	3–304
٦	ſ2C	Dual 2:1 Selector	3–305
٦	ſ2D	2:1 Selector	3–307
٦	Γ2E	Dual 2:1 Selector	3–308
٦	ſ2F	2:1 Selector	3–309
٦	Г24	Power 2-AND 4-wide Multiplexer	3–83
7	Г26	Power 2-AND 6-wide Multiplexer	3–84
٦	Г28	Power 2-AND 8-wide Multiplexer	3–85
	Г32	Power 3-AND 2-wide Multiplexer	3–87
7	Г33	Power 3-AND 3-wide Multiplexer	3–88
٦	Г34	Power 3-AND 4-wide Multiplexer	3–89
٦	Г42	Power 4-AND 2-wide Multiplexer	3–90

Name	Function	Page No.
T43	Power 4-AND 3-wide Multiplexer	3–91
T44	Power 4-AND 4-wide Multiplexer	3–92
T54	Power 4-2-3-2 AND 4-wide Multiplexer	3–93
T5A	4:1 Selector	3–311
U24	Power 2-OR 4-wide Multiplexer	3–94
U26	Power 2-OR 6-wide Multiplexer	3–95
U28	Power 2-OR 8-wide Multiplexer	3–96
U32	Power 3-OR 2-wide Multiplexer	3–97
U33	Power 3-OR 3-wide Multiplexer	3–98
U34	Power 3-OR 4-wide Multiplexer	3–99
U42	Power 4-OR 2-wide Multiplexer	3–100
U43	Power 4-OR 3-wide Multiplexer	3–101
U44	Power 4-OR 4-wide Multiplexer	3–102
V1L	Inverting Clock Buffer	3–117
V1N	Inverter	37
V2B	Power Inverter	3–8
V3A	1:2 Selector	3–313
V3B	Dual 1:2 Selector	3–314
X1B	Power Exclusive NOR	3–58
X1N	Exclusive NOR	3–57
X2B	Power Exclusive OR	3–60
X2N	Exclusive OR	3–59
X3B	Power 3-Input Exclusive NOR	3–62
X3N	3-Input Exclusive NOR	3–61
X4B	Power 3-Input Exclusive OR	3–64
X4N	3-Input Exclusive OR	3–63
YL2	1-bit Data Latch with TM	3–261
YL4	4-bit Data Latch with TM	3–263
Z00	0 Clip	3–329
Z01	1 Clip	3–330

### Sales Information

Page	Contents
4-3	Introduction to Fujitsu
4–7	Integrated Circuits Corporate Headquarters - Worldwide
4-8	FMI Sales Offices for North and South America
4-9	FMI Representatives – USA
4-11	FMI Representatives - Canada
4-11	FMI Representatives – Mexico
4-11	FMI Representatives – Puerto Rico
4-12	FMI Distributors – USA
4-16	FMI Distributors - Canada
4-17	FMG Sales Offices for Europe
4-18	FMG Distributors – Europe
4-20	FMA Sales Offices for Asia and Australia
4-21	FMA Representatives - Asia and Australia
4-22	FMA Distributors - Asia and Australia

### Introduction to Fujitsu

#### **Fujitsu Limited**

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly-owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

### Introduction to Fujitsu (Continued)

#### Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to three marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The Advanced Products Division (APD) is responsible for the complete product development cycle, from design through operations support and worldwide marketing and sales. Products are the result of both internal development and external relationships, such as joint development agreements, technology licenses, and joint ventures. The SPARC™ RISC processor was developed by both APD and Sun Microsystems, Inc.

In addition to designing and selling a full line of SPARC processors and peripheral chips, APD also designed and is selling the EtherStar™ LAN controller — the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of APD's cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs, FETs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD).

Memory and programmable devices marketed by ICD include the following:

DRAMs and DRAM Modules
EPROMS
EEPROMS
NOVRAMS
CMOS masked ROMS
CMOS SRAMS and CMOS SRAM Modules
BiCMOS SRAMS
Bipolar PROMS
ECL RAMS
STRAMS (self-timed RAM)
Hi-Rel PROMS and SRAMS
Ultra High-speed ECL/ECL—TTL Translator Circuits
Linear ICs and Transistors

### Introduction to Fujitsu (Continued)

ASIC products offered by ICD include the following:

CMOS, ECL, and BiCMOS gate arrays CMOS standard cells Design Software Support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose Gresham Dallas Chicago Atlanta Boston

Microcomputer and communications products offered by ICD include the following:

4-bit MCUs
8- and 16-bit MPUs
SCSI and controllers
DSPs
Prescalers
PLLs
Memory Cards

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, the Gresham Manufacturing Division began manufacturing ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, Fujitsu Components of America, markets connectors, keyboards, plasma displays, relays, and hybrid ICs.

#### Fujitsu Mikroelektronik GmbH (European Sales Operation)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a wholly-owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Europe. The wide range of ICs, LSI memories, microprocessors, and ASIC products are noted throughout Europe for design excellence and unmatched reliability. Branch offices are located in Munich, London, Paris, Stockholm, and Milan.

### Introduction to Fujitsu (Continued)

#### Fujitsu Microelectronics Ireland, Ltd. (European Production Operation)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in the suburbs of Dublin, as Fujitsu's European Production Center for integrated circuits. FME assembles DRAMs, EPROMs, and other LSI memory products.

#### Fujitsu Microelectronics, Ltd. (European ASIC Design Operation)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with highly sophisticated CAD systems to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

#### Fujitsu Microelectronics Asia PTE Ltd. (Asian/Oceanian Sales Operation)

Fujitsu Microelectronics Asia PTE Ltd. (FMA) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

### Integrated Circuits Corporate Headquarters — Worldwide

#### International Corporate Headquarters

**FUJITSU LIMITED** 

Marunouchi Headquarters 6-1, Marunouchi 1-chome Chiyoda-ku, Tokyo 100 Japan Tel: (03) 216-3211 Telex: 781-22833

FAX: (03) 213-7174

For integrated circuits marketing information please contact the following:

#### **Headquarters for Japan**

#### **FUJITSU LIMITED**

Integrated Circuits and Semiconductor Marketing Furukawa Sogo Bldg.
6–1, Marunouchi 2–chome
Chiyoda–ku, Tokyo 100
Japan
Tel: (03) 216-3211
Telex: 781–2224361
FAX: (03) 211-3987

#### **Headquarters for North and South America**

FUJITSU MICROELECTRONICS, INC.

Integrated Circuits Division 3545 North First Street San Jose, CA 95134-1804 USA Tel: (408) 922-9000

Telex: 910-338-0190 FAX: (408) 432-9044

### **Headquarters for Europe**

#### FUJITSU MIKROELEKTRONIK GmbH

Lyoner Strasse 44–48 Arabella Centre 9. OG D–6000 Frankfurt 71 Federal Republic of Germany Tel: (069) 66320 Telex: 441963 FAX: (069) 6632122

#### Headquarters for Asia and Australia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED

06-04/06-07 Plaza by the Park No. 52 Bras Basah Road Singapore 0718 Tel: (65) 336-1600 Telex: 55573 FAX: (65) 336-1609

# Fujitsu Microelectronics, Inc. (FMI) Sales Offices for North and South America

#### **NORTHERN CALIFORNIA**

Fujitsu Microelectronics, Inc. 10600 N. De Anza Blvd. Suite 225 Cupertino, CA 95014

Cupertino, CA 95014 Tel: (408) 996–1600 FAX: (408) 725–8746

#### **SOUTHERN CALIFORNIA**

Fujitsu Microelectronics, Inc. Century Centre 2603 Main Street Suite 510 Irvine, CA 92714 Tel: (714) 724–8777 FAX: (714) 724–8778

#### COLORADO (Denver)

Fujitsu Microelectronics, Inc. 5445 DTC Parkway Suite 300 Englewood, CO 80111 Tel: (303) 740–8880 FAX: (303) 740–8988

#### **GEORGIA** (Atlanta)

Fujitsu Microelectronics, Inc. 3500 Parkway Lane Suite 210 Norcross, GA 30092 Tel: (404) 449–8539 FAX: (404) 441–2016

#### ILLINOIS (Chicago)

Fujitsu Microelectronics, Inc. One Pierce Place Suite 910 Itasca, IL 60143–2681 Tel: (708) 250–8580 FAX: (708) 250–8591

#### MASSACHUSETTS (Boston)

Fujitsu Microelectronics, Inc. 75 Wells Avenue Suite 5 Newton Center, MA 02159–3251 Tel: (617) 964–7080 FAX: (617) 964–3301

#### MINNESOTA (Minneapolis)

Fujitsu Microelectronics, Inc. 3460 Washington Drive Suite 209 Eagan, MN 55122–1303 Tel: (612) 454–0323 FAX: (612) 454–0601

#### **NEW JERSEY (Mt. Laurel)**

Fujitsu Microelectronics, Inc. Horizon Corporate Center 3000 Atrium Way Suite 100 Mt. Laurel, NJ 08054 Tel: (609) 727–9700 FAX: (609) 727–9797

#### NEW YORK (Hauppauge)

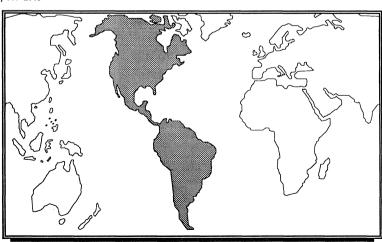
Fujitsu Microelectronics, Inc. 601 Veterans Memorial Highway Suite P Hauppauge, NY 11788–1054 Tel: (516) 361–6565 FAX: (516) 361–6480

#### **OREGON** (Portland)

Fujitsu Microelectronics, Inc. 5285 SW Meadows Road Suite 222 Lake Oswego, OR 97035–9998 Tel: (503) 684–4545 FAX: (503) 684–4547

#### **TEXAS (Dallas)**

Fujitsu Microelectronics, Inc. 14785 Preston Road Suite 670 Dallas, TX 75240 Tel: (214) 233–9394 FAX: (214) 386–7917



### FMI Representatives — USA

For product information, contact your nearest Representative.

#### Alabama

The Novus Group, Inc. 2905 Westcorp Blvd. Suite 120 Huntsville, AL 35805 Tel: (205) 534–0044 FAX: (205) 534–0186

#### Arizona

Aztech Component Sales Inc. 15230 N 75th Street Suite 1031 Scottsdale, AZ 85260 Tel: (602) 991–6300 FAX: (602) 991–0563

#### California

Harvey King, Inc. 6393 Nancy Ridge Drive San Diego, CA 92121 Tel: (619) 587–9300 FAX: (619) 587–0507

Infinity Sales, Inc. 4500 Campus Drive Suite 300 Newport Beach, CA 92660 Tel: (714) 833–0300 FAX: (714) 833–0303

Norcomp 3350 Scott Blvd., Suite 24 Santa Clara, CA 95054 Tel: (408) 727-7707 FAX: (408) 986-1947

Norcomp 2140 Professional Drive Suite 200 Roseville, CA 95661 Tel: (916) 782–8070 FAX: (916) 782–8073

Sonika Electronica of America 925 Hale Place Suite A-8 Chula Vista, CA 92013 Tel: (619) 482-8700 FAX: (619) 482-7598

#### Colorado

Front Range Marketing 3100 Arapahoe Road Suite 404 Boulder, CO 80303 Tel: (303) 443–4780 FAX: (303) 447–0371

#### Connecticut

Conntech Sales, Inc. 182 Grand Street Suite 318 Waterbury, CT 06702 Tel: (203) 754–2823 FAX: (203) 573–0538

#### Florida

Semtronic Associates, Inc. 657 Maitland Avenue Altamonte Springs, FL 32701 Tel: (407) 831–8233 FAX: (407) 831–2844 Semtronic Associates. Inc.

1467 S. Missouri Avenue Clearwater, FL 33516 Tel: (813) 461–4675 FAX: (813) 442–2234

Semtronic Associates, Inc. 3471 NW 55th Street Ft. Lauderdale, FL 33309 Tel: (305) 731–2484 FAX: (305) 731–1019

#### Georgia

The Novus Group, Inc. 6115-A Oakbrook Pkwy Norcross, GA 30093 Tel: (404) 263-0320 FAX: (404) 263-8946

#### Idaho

Cascade Components 2710 Sunrise Rim Road Suite 130 Boise, ID 83705 Tel: (208) 343–9886 FAX: (208) 343–9887

#### Illinois

Beta Technology 1009 Hawthorn Drive Itasca, IL 60143 Tel: (708) 256–9586 FAX: (708) 256–9592

#### Indian

Fred Dorsey & Associates 3518 Eden Place Carmel, IN 46032 Tel: (317) 844–4842 FAX: (317) 844–4843

#### lowa

Electromec Sales 1500 2nd Avenue Suite 205 Cedar Rapids, IA 52403 Tel: (319) 362–6413 FAX: (319) 362–6535

#### Kansas

Rothkopf & Associates, Inc. 1948 E. Santa Fe Suite H Olathe, KS 66062 Tel: (913) 829–8897 FAX: (913) 829–1664

#### Maryland

Arbotek Associates 102 W. Joppa Road Towson, MD 21204 Tel: (301) 825-0775 FAX: (301) 337-2781

#### Massachusetts

Mill-Bern Associates 2 Mack Road Woburn, MA 01801 Tel: (617) 932-3311 FAX: (617) 932-0511

#### Michigan

Greiner Associates, Inc. 15324 E. Jefferson Avenue Suite 12 Grosse Point Park, MI 48230 Tel: (313) 499–0188 FAX: (313) 499–0665

## Λ

### FMI Representatives — USA (Continued)

#### Minnesota

Electromec Sales 1601 E Highway 13 Suite 200 Burnsville, MN 55337 Tel: (612) 894–8200 FAX: (612) 894–9352

#### Missouri

Rothkopf & Associates, Inc. 8721 Manchester Road St. Louis, MO 63144 Tel: (314) 961–4485 FAX: (314) 961–4736

#### **New Jersey**

BGR Associates Evesham Commons 525 Route 73 Suite 100 Marlton, NJ 08053 Tel: (609) 983–1020 FAX: (609) 983–1879

Technical Applications & Marketing 91 Clinton Road Suite 1D Fairfield, NJ 07006 Tel: (201) 575–4130 FAX: (201) 575–4563

#### **New York**

Quality Components 3343 Harlem Road Buffalo, NY 14225 Tel: (716) 837–5430 FAX: (716) 837–0662 Quality Components 116 Fayette Street Manlius, NY 13104 Tel: (315) 682–8885 FAX: (315) 682–2277

Quality Components 2318 Titus Ave. Rochester, NY 14622 Tel: (716) 342–7229 FAX: (716) 342–7227

#### North Carolina

The Novus Group, Inc. 1026 Commonwealth Court Cary, NC 27511 Tel: (919) 460-7771 FAX: (919) 460-5703

#### Ohio

Spectrum ESD 3947 Ray Court Road Morrow, OH 45152 Tel: (513) 899–3260 FAX: (513) 899–3260

Spectrum ESD 8925 Galloway Trail Novelty, OH 44072 Tel: (216) 338–5226 FAX: (216) 338–3214

#### Oregon

L-Squared Limited 15234 NW Greenbrier Pkwy Beaverton, OR 97006 Tel: (503) 629-8555 FAX: (503) 645-6196

#### Texas

Technical Marketing, Inc. 3320 Wiley Post Road Carrollton, TX 75006 Tel: (214) 387–3601 FAX: (214) 387–3605

Technical Marketing, Inc. 2901 Wilcrest Drive Suite 139 Houston, TX 77042 Tel: (713) 783–4497 FAX: (713) 783–5307

Technical Marketing, Inc. 1315 Sam Bass Circle Suite B–3 Round Rock, TX 78681 Tel: (512) 244–2291 FAX: (512) 338–1596

#### Washington

L-Squared Limited 105 Central Way Suite 203 Kirkland, WA 98033 Tel: (206) 827–8555 FAX: (206) 828–6102

#### Wisconsin

Beta Technology 9401 W Beloit Street Suite 304C Milwaukee, WI 53227 Tel: (414) 543–6609 FAX: (414) 543–9288

### FMI Representatives — Canada, Mexico and Puerto Rico

#### Canada

5468 Dundas Street W. Suite 206 Islington, Ontario M9B 6E3 Tel: (416) 236–2355 FAX: (416) 236–3387

Pipe-Thompson Limited

Pipe-Thompson Limited RR2 North Gower Ottawa, Ontario K0Z 2T0 Tel: (613) 258–4067 FAX: (613) 258–7649

#### Mexico

Solano Electronica Ermita 1039-10 Colonia Chapalita Guadalajara, JAL. 45042 Tel: (36) 47-4250 FAX: (36) 473433 Solano Electronicas

Thiers 100 Colonia Anzures Mexico City, D.F. 11590 Tel: (55) 31–5915 FAX: (55) 31–5915

#### **Puerto Rico**

Semtronic Associates Mercantil Plaza Building Suite 816 Hato Rey, Puerto Rico 00918 Tel: (809) 766–0700

#### FMI Distributors — USA

#### Alabama

Marshall Industries 3313 S. Memorial Highway Suite 121 Huntsville, AL 35801 (205) 881–9235

Repton Electronics 4950 Corporate Drive Suite 105C Huntsville, AL 35805 (205) 722–9565

#### Arizona

Insight Electronics 1515 W. University Drive Suite 103 Tempe, AZ 85281 (602) 829–1800

Sterling Electronics 3501 E. Broadway Road Phoeniz, AZ 85040 (602) 268–2121

Marshall Industries 9830 S. 51st Street Suite B121 Phoenix, AZ 85044 (602) 496–0290

#### California

Insight Electronics 28035 Dorothy Drive Suite 220 Agoura, CA 91301 (818) 707–2100

Insight Electronics 15635 Alton Parkway Suite 120 Irvine, CA 92718 (714) 727–2111

Insight Electronics 6885 Flanders Drive Suite G San Diego, CA 92126 (619) 587–9757

Marshall Industries 9710 Desoto Ave. Chatsworth, CA 91311 (818) 407–4100

Marshall Industries 9674 Telstar Ave. El Monte, CA 91731 (818) 459–5500 Marshall Industries One Morgan Irvine, CA 92718 (714) 458–5308

Marshall Industries 336 Los Coches Street Milpitas, CA 95035 (408) 942-4600

Marshall Industries 3039 Kilgore Ave. Rancho Cordova, CA 95670 (916) 635–9700

Marshall Industries 10105 Carroll Canyon Road San Diego, CA 92131 (619) 578-9600

Merit Electronics 2070 Ringwood Avenue San Jose, CA 95131 (408) 434-0800

Sterling Electronics 55310 Derry Unit X Agoura, CA 91301 (818) 707–0911

Sterling Electronics 9410 Topanga Canyon Rd. Chatsworth, CA 91311 (818) 407–8850

Sterling Electronics 1342 Bell Avenue Tustin, CA 92680 (714) 259–0900

Western Microtechnology 28720 Roadside Dr. Suite 175 Agoura Hills, CA 91301 (818) 356-0180

Western Microtechnology 1637 North Brian Orange, CA 92667 (714) 637–0200

Western Microtechnology 6837 Nancy Ridge Drive San Diego, CA 92121 (619) 453–8430

Western Microtechnology 12900 Saratoga Ave. Saratoga, CA 95070 (408) 725–1660

#### Colorado

Marshall Industries 12351 N. Grant Road Suite A Thornton, CO 80241 (303) 451-8383

Sterling Electronics 8200 South Akron Street Suite 111 Englewood, CO 80112 (303) 792-3939

#### Connecticut

Marshall Industries 20 Sterling Drive Wallingford, CT 06492 (203) 265–3822

Milgray Electronics 326 W. Main Street Milford, CT 06460 (203) 795-0711

Western Microtechnology, Inc. 731 Main Street Suite B2 Lantern Ridge Monroe, CT 06468 (203) 452-0533

#### Florida

Marshall Industries 380 S. Northlake Blvd Suite 1024 Altamonte Springs, FL 32701 (407) 767–8585

Marshall Industries 2700 W. Cypress Creek Rd. Suite C 106 Ft. Lauderdale, FL 33309 (305) 977–4880

Marshall Industries 2840 Sherer Drive St. Petersburg, FL 33716 (813) 573–1399

Milgray Electronics 1850 Lee Road Suite 104 Winter Park, FL 32789 (407) 647–5747

### FMI Distributors — USA (Continued)

#### Florida (Continued)

Reptron Electronics 33320 N.W. 53rd Street Suite 206 Ft. Lauderdale, FL 33309 (305) 735–1112

Reptron Electronics 14501 McCormick Drive Tampa, FL 33626 (813) 855–2351

#### Georgia

Marshall Industries 5300 Oakbrook Pkwy Suite 146 Norcross, GA 30093 (404) 923–5750

#### Georgia

Milgray Electronics 3000 Northwoods Parkway Suite 270 Norcross, GA 30071 (404) 446–9777

Reptron Electronics 3040 H Business Park Drive Norcross, GA 30071 (404) 446–1300

#### Illinois

Classic Components 3336 Commercial Ave. Northbrook, IL 60062 (312) 272–9650

Marshall Industries 50 E. Commerce Dr. Suite I Schaumburg, IL 60173 (312) 490–0155

Milgray Electronics 3223 N. Wilkey Road Arlington Heights, IL 60004 (312) 253–1573

Reptron Electronics 1000 E. State Hwy Suite K Schaumburg, IL 60173 (312) 882–1700

#### Indiana

Marshall Industries 6990 Corporate Drive Indianapolis, IN 46278 (317) 297–0483

#### Kansas

Marshall Industries 10413 W. 84th Terrace Lenexa, KS 66214 (913) 492–3121

Milgray Electronics 6901 W. 63rd Street Overland Park, KS 66202 (913) 236–8800

#### Maryland

Marshall Industries 2221 Broadbirch Suite G Silver Springs, MD 20910 (301) 622–1118

Milgray Electronics 9801 Broken Land Parkway Columbia, MD 21045 (301) 995–6169

Vantage Components, Inc. 6925-R Oakland Mills Road Columbia, MD 21045 (301) 720-5100

#### Massachusetts

Interface Electronic Corp. 228 South Street Hopkinton, MA 01748 (617) 435–6858

Marshall Industries 33 Upton Drive Wilmington, MA 01887 (508) 658-0810

Milgray Electronics 187 Ballardvale Street Wilmington, MA 01887 (508) 657–5900

Vantage Components, Inc. 200 Bulfinch Drive Andover, MA 01810 (508) 687-3900

Western Microtechnology 20 Blanchard Road 9 Corporate Place Burlington, MA 01803 (617) 273–2800

#### Michigan

Marshall Industries 31067 Schoolcraft Rd. Livonia, MI 48150 (313) 525–5850

#### Michigan

Reptron Electronics 34403 Glendale Livonia, MI 48150 (313) 525–2700

#### Minnesota

Marshall Industries 3955 Annapolis Lane Plymouth, MN 55447 (612) 559–2211

Reptron Electronics 5929 Baker Road Minnetonka, MN 55345 (612) 938–0000

#### Missouri

Marshall Industries 3377 Hollenberg Drive Bridgeton, MO 63044 (314) 291–4650

#### **New Jersey**

Marshall Industries 101 Fairfield Road Fairfield, NJ 07006 (201) 882–0320

Marshall Industries 158 Gaither Drive Mt. Laurel, NJ 08054 (609) 234–9100

Milgray Electronics 3002 Greentree Exec. Campus Suite B Marlton, NJ 08053 (609) 983–5010

Vantage Components, Inc. 23 Sebago Street P.O. Box 2939 Clifton, NJ 07013 (201) 777–4100

Western Microtechnology, Inc. 387 Passaic Avenue Fairfield, NJ 07006 (201) 882-4999

#### **New Mexico**

Sterling Electronics 3450-D Pan American Freeway Albuquerque, NM 87107 (505) 884-1900

### FMI Distributors — USA (Continued)

#### **New York**

Marshall Industries 275 Oser Avenue Hauppauge, NY 11788 (516) 273–2424

Marshall Industries 129 Brown Street Johnson City, NY 13790 (607) 798–1611

#### **New York**

Marshall Industries 1280 Scottsville Road Rochester, NY 14624 (716) 235–7620

Mast Distributors 95 Oser Avenue P.O. Box 12248 Hauppauge, NY 11788 (516) 273–4422

Micro Genesis 90–10 Colin Drive Holbrook, NY 11741 (516) 472–6000

Milgray Electronics 77 Schmitt Blvd. Farmingdale, NY 11735 (516) 420–9800

Milgray Electronics 1200 A Scottsville Rd. Rochester, NY 14624 (716) 235–0830

Vantage Components, Inc. 1041-G West Jericho Turnpike Smithtown, NY 11787 (516) 543–2000

#### **North Carolina**

Marshall Industries 5224 Greens Dairy Road Raleigh, NC 27604 (919) 878–9882

Reptron Electronics 5954-A Six Fork Road Raleigh, NC 27609 (214) 783-0800

#### Ohio

Marshall Industries 3520 Park Center Drive Dayton, OH 45414 (513) 898-4480

Marshall Industries 30700 Bain Bridge Road Unit A Solon, OH 44139 (216) 248–1788

Milgray Electronics 6155 Rockside Road Cleveland, OH 44131 (216) 447–1520

Reptron Electronics 404 E. Wilson Bridge Road Suite A Worthington, OH 43085 (614) 436–6675

#### Oklahoma

Radio Inc. 1000 South Main Tulsa, OK 74119 (918) 587-9123

#### Oregon

Marshall Industries 9705 S.W. Gemin Drive Beaverton, OR 97005 (503) 644–5050

Western Microtechnology 1800 N.W. 169th Place Suite B300 Beaverton, OR 97006 (503) 629–2082

#### Pennsylvania

Interface Electronic Corp. 7 Great Valley Parkway Malvern, PA 19355 (215) 889-2060

Marshall Industries 701 Alpha Drive Pittsburg, PA 15237 (412) 788-0441

#### Texas

Insight Electronics, Inc. 1778 Plano Road Suite 320 Richardson, TX 75081 (214) 783–0800

Marshall Industries 8504 Cross Park Drive Austin, TX 78754 (512) 837–1991

Marshall Industries 2045 Chenault Carrollton, TX 75006 (214) 233–5200

Marshall Industries 2635 South Highway 77 Harlingen, TX 78550 (512) 421-4621

Marshall Industries 7250 Langtry Houston, TX 77040 (713) 895–9200

Milgray Electronics 16610 N. Dallas Pkwy Suite 1300 Dallas, TX 75248 (214) 248–1603

Reptron Electronics 3410 Midcourt Carrollton, TX 75006 (214) 702-9373

Western Microtechnology, Inc. 18333 Preston Road Suite 460 Dallas, TX 75252 (214) 248-3775

Western Microtechnology, Inc. 2500 Wilcrest, 3rd Floor Houston, TX 77042 (713) 954-4850

### FMI Distributors — USA (Continued)

#### Utah

Marshall Industries 466 Lawndale Drive Suite C Salt Lake City, UT 84115 (801) 485–1551

Milgray Electronics 4190 S. Highland Drive Suite 102 Salt Lake City, UT 84124 (801) 272–4999

#### Washington

Insight Electronics, Inc. 12002 115th Avenue, NE Kirkland, WA 98034 (206) 820-8100 Marshall Industries 11715 N. Creek Parkway Suite 112 Bothell, WA 98011 (206) 486–5747

Western Microtechnology 14636 N.E. 95th Street Redmond, WA 98052 (206) 881–6737

#### Wisconsin

Classic Components 2925 S. 160th Street New Berlin, WI 53151 (414) 786–5300 Marsh Electronics 1563 S. 101st Street Milwaukee, WI 53214 (414) 475–6000

Marshall Industries 20900 Swenson Drive Suite 150 Waukesha, WI 53186 (414) 797–8400

### FMI Distributors — Canada

#### **British Columbia**

ITT Industries 3455 Gardner Court Burnaby, B.C. V5G 4J7 (604) 291–1227

Space Electronics 1695 Boundry Road Vancouver, B.C. V5K 4X7 (604) 294–1166

#### Ontario

ITT Industries 300 North Rivermede Road Concord, ON L4K 2Z4 (416) 736–1114 Marshall Industries 4 Paget Road Unit 10 & 11 Framton, ON L6T 5G3 (416) 458–8046

Milgray Electronics 150 Consumers Road Suite 502 Willowdale, ON M2J 4R4 (416) 756–4481

#### Quebec

Marshall Industries 3869 Sources Blvd Suite 207 D.D.O., QUE H9B 2A2 (514) 683–9440

Space Electronics 5651 Rue Ferrier Street Montreal, QUE H4P 2K5 (514) 697–8676

### Fujitsu Mikroelektronik GmbH (FMG) Sales Offices for Europe

#### France

Fuiitsu Immeuble le Trident 3-5. Voie Felix Eboue F-94024 Creteil Cedex Tel: (1)4-207-8200 Telex: 262861 FAX: (1)4-207-7933

#### F.R. Germany

Fujitsu Mikroelektronik GmbH Lyoner Strasse 44-48 Arabella Center 9, OG D-6000 Frankfurt am Main 71 Tel: (69)66320 Telex: 411963 FAX: (69)66321

Fujitsu Mikroelektronik GmbH Am Joachimsberg 10-12 D-7033 Herrenberg

Tel: (07032) 4085 FAX: (07032) 4088 Fujitsu Mikroelektronik GmbH Carl-Zeiss-Ring 11

D-8045 Ismaning bei Munchen Tel: (89)960-9440 Telex: 8974464 FAX: (89)960-9442

#### Italy

Fujitsu Microelectronics Italia S.R.L. Centro Direzionale Milanofiori Strada 4 - Palazzo A/2 I-20094 Milano Tel: (39)(2)824-6170/176 Telex: 318546

#### Netherlands

Fujitsu Benelux Europalaan 6/B 5623 LJ Eindhoven Tel: (31)44-7440 Telex: 59265 FAX: (31)44-4158

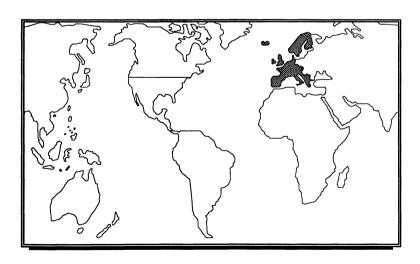
FAX: (39)(2)824-6189

#### Sweden

Fujitsu Microelectronics Ltd. Torggatan 8 17154 Solna Tel: (8)764-6365 Telex: 13411 FAX: (8)28-0345

#### **United Kingdom**

Fujitsu Microelectronics Ltd. Hargrave House Belmont Road Maidenhead Berkshire SL6 6NE Tel: (0628)76100 Telex: 848955 FAX: (0628)781484



### FMG Distributors — Europe

#### Austria

Eljapex Handelsges. MBH Eitnergasse 6 1232 Wien Tel: (222)861531 Telex: 112344 FAX: (222)863211200

MHV/EBV Elektronik Diefenbachgasse 35/6 1150 Wien

Tel: (222)838519 Telex: 134946 FAX: (222) 838530

#### Belgium

Eriat SA 83, Rue des Fraisiers 4410 Herstal Vottem Tel: (41)271993 Telex: 41782 FAX: (41)278085

MHV/EBV Elektronik Excelsiorlaan 35 Avenue Excelsion 35 1930 Zaventem Tel: (2)7209936 Telex: 62590 FAX: (2)7208152

#### Denmark

Nordisk Elektronik AS Transformervej 17 2730 Herlev Tel: (2)842000 Telex: 35200 FAX: (2)921552

#### Finland

Gadelius OY Kaupintie 18 00440 Helsinki Tel: (90)5626644 Telex: 121274 FAX: (90)5626196 Aspecs OY Myyrmaentie 2 A 01600 Vantaa Helsinki Tel: (90)5668686

#### France

D P A 12, Avenue des Pres 78 180 Montigny le Bretonneux Tel: (1)30575040 Telex: 689423 FAX: (1)30571863

Microram 6, Rue le Corbusier Silic 424 94583 Rungis Cedex Tel: (1)46868170 Telex: 2265909 FAX: (1)45605549

#### Germany Eliapex GmbH

Felsenauerstr. 18 7890 Waldshut-Tiengen Tel: (07751)2035 Telex: (07751)6603 Micro Halbleiter GmbH Jagerweg 10 8012 Ottobrunn Tel: (089)6096068

Telex: 5213807

FAX: (089)6093758

#### Italy

Unidis Group Bologna Malpassi SRL Via Baravelli, 1 40012 Calderara di Reno Tel: (051)727252 Telex: 583118 FAX: (051)727515 Unidis Group Torino PCM SnC Via Piave 54/B 10099 Rivoli Tel: (011)9532256 FAX: (011)9534238

#### Netherlands

MHV/EBV Elektronik Planetenbaan 2 3606 AK-Maarssenbroek Tal: (3465)62353 Telex: 76089 FAX: (3465)64277 P & T Electronics B.V. Esse Baan 77 P.O. Box 329 2908 LJ Capelle A/D ljssel

Tel: 104501444 Telex: 26096 FAX: 104507092

#### Norway

Odin Electronics AS Postboks 72 Edv. Griegsvei 2 1472 Fjellhamar Tel: (02)703730 Telex: 19732 FAX: (02)700310

#### Republic of Ireland

FAX: (61)363141

Allied Semiconductors International Ltd. Unit 1 Distribution Park Shannon Industrial Estate Shannon Co. Clare Tel: (61)61777 Telex: 70358

### FMG Distributors — Europe (Continued)

#### Spain

Comelta S.A. Pedro IV-84, 5 PI 08005 Barcelona Tel: (93)3007712 Telex: 51934 FAX: (93)3005156

Comelta S.A. Emilio Munoz 41 Nave 1-1-2 28037 Madrid Tel: (1)7543001 Telex: 42007 FAX: (1)7542151

#### Sweden

Martinsson Elektronik AB Box 9060 Instrumentvagen 16 12609 Hagersten Tel: (8)7440300 Telex: 13077 FAX: (8)7443403

#### Switzerland

Eljapex AG Hardstrasse 72 5430 Wettingen Tel: (56)275777 Telex: 826300 FAX: (56)261486

#### United Kingdom

Hawke Components Amotex House 45 Hanworth Road Sunbury on Thames Middlesex TW16 5DA Tel: (0197)97799 Telex: 923592

FAX: (9327)87333 Pronto Electronic Systems Ltd. City Gate House 399/425 Eastern Avenue Gants Hills Ilford

Essex IG2 6LR Tel: (15)546222 Telex: 8954213 FAX: (15)183222

# Fujitsu Microelectronics Asia PTE Limited (FMA) Sales Offices for Asia and Australia

#### Taiwan

Fujitsu Microelectronics Pacific Asia TW Branch Ltd. 1906 No. 333 Keelung Road Sec.1 Taipei 10548 Taiwan, Republic of China Tel: (02) 757–6548

Telex: 17312 FMPTPI FAX: (02) 757–6571

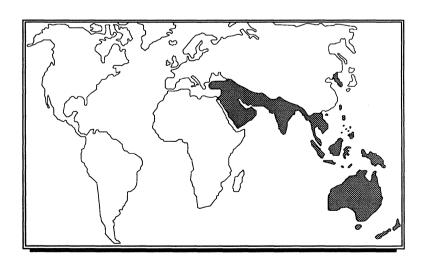
#### Singapore

FAX: 336-1609

Fujitsu Electronics PTE Ltd. #06-04/07 Plaza by the Park 52 Bras Basah Road 05-301/2, The Plaza Singapore 0718 Tel: (65) 336-1600 Telex: 55573 FESPL

#### Hong Kong

Fujitsu Microelectronics Pacific Asia Ltd. 618–617, Tower B New Mandarin Plaza 14 Science Museum Road TST East, Kowloon Hong Kong Tel: 723–0393 FAX: 721–6555



### FMA Representatives — Asia and Australia

#### Australia

Pacific Microelectronics PTY Ltd. Unit A20, Central Park 4 Central Avenue P.O. Box 189 Thornleigh NSW 2120 Australia Tel: (2)481–0065

Telex: 24844460 FAX: (2) 484–4460

#### Korea

KML Corporation 3/F Bangbae Station Bldg. 981–15 Bangbae 3–Dong Shucho-gu, Seoul, Korea Tel: (2)588–2011 Telex: K25981 KMLCORP FAX: (2)588–2017

### FMA Distributors — Asia

#### Hong Kong

Famint (HK) Ltd. Room 1502,15/F No. 111 Leighton Road Causeway Bay, Hong Kong

Tel: 5-760130 / 5-760146

FAX: 5-765619

#### Singapore

Cony Electronics (S) PTE Ltd. 10 Jalan Besar 03–25 Sim Lim Tower Singapore 0820 Tel: 296–2111 Telex: CONY RS34808 FAX: 296–0339

Famint Electronics PTE Ltd. 01–302, The Plaza 7500 A Beach Road Singapore 0719 Tel: 298–4566

Telex: RS37295 FAMINT

FAX: 297-2597

#### Taiwan

Eplus Corporation, Ltd. 11F-8, No. 20 Min Chuin West Road Taipei, Taiwan Tel: (2) 536-3250 FAX: (2) 581-6309

Famint (Taiwan) Co., Ltd. Room 113, 10/F Chang An East Road Taipei, Taiwan Republic of China Tel: (02) 5051963 FAX: (02) 5080385



- Design Information
- AU Series CMOS Gate Array Macrocell Library
- 3 CG21 Series CMOS Gate Array Macrocell Library
- 4. Sales Information

### **FUJITSU LIMITED**

Marunouchi Headquarters 6-1, Marunouchi 1-chome Chiyoda-ku, Tokyo 100, Japan Tel: (03) 216-3211

Telex: 781-22833 FAX: (03) 213-7174

For further information, please contact:

### Japan

FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg.
6-1, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100, Japan
Tel: (03) 216-3211
Telex: 781-2224361
FAX: (03) 211-3987

### Europe

FUJITSU MIKROELEKTRONIK GmbH Lyoner Strasse 44-48 Arabella Centre 9. 0G D-6000 Frankfurt 71 Federal Republic of Germany Tel: (49) (069) 66320 Telex: 441-963 FAX: (069) 663-2122

#### Asia

FUJITSU MICROELECTRONICS ASIA PTE. LTD. 06-04/06-07 Plaza By the Park No. 52 Bras Basah Road Singapore 0718 Tel: (65) 336-1600 Telex: 55573 FAX: (65) 336-1609

#### North and South America

FUJITSU MICROELECTRONICS, INC. Integrated Circuits Division 3545 North First Street San Jose, CA 95134-1804 USA Tel: (408) 922-9000 Telex: 910-338-0190 FAX: (408) 432-9044