MOS Memory Products

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FUJITSU

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MOS Memory Products

1989 Data Book

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Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete information sufficient for construction purposes is not necessarily given.

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Overview

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Fujitsu's MOS Memory Products

Introduction

Fujitsu manufactures a wide range of integrated circuits that includes linear products, microprocessors, telecommunications circuits, ASICs, high-speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and both static and dynamic memories.

The MOS memory product line offers devices for use in a wide range of applications. These memories are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

DRAMs

Fujitsu manufactures a complete family of leading technology dynamic random access memories for the data processing, telecom, and industrial markets. This family consists of the highest density devices currently available with a broad selection of organizations, access modes, and packages.

MOS Application-Specific Memories

Our application-specific memories include a CMOS dual-port RAM that has two separate I/O ports, a CMOS cache buffer RAM that offers a two-byte width data path, and a CMOS TAG RAM that enhances memory performance of cache-based systems.

MOS RAM Modules

Fujitsu manufacturers a complete family of reliable CMOS dynamic and static RAM memory modules for those applications requiring high density and large memory storage capability. Fujitsu's family of memory modules are pin compatible with Jedec standards.

High-speed CMOS SRAMs

Fujitsu's high-speed CMOS static RAMs offer the advantages of low power dissipation, low cost, and high performance. Features includes TTL compatibility and a separate chip select pin that simplifies multipackage systems design.

Application-Specific Static Memories

To address the system needs of cache memory chips, Fujitsu's application-specific memory line includes both cache TAG RAM and high-speed static RAM, as well as port RAMS for multiprocessor systems. Additionally, Fujitsu will be offering control chips for memory transfers between CPU, main, and cache memories.

Low-Power CMOS SRAMs

These low-power static random access memories are ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. The memories utilize asynchronous circuitry and may be maintained in any state for an indefinite period of time.

NMOS Erasable PROMs

Fujitsu currently offers 64K density EPROMs in NMOS technology to allow our customers with NMOS designs the time to change over to the newer CMOS technology.

CMOS Erasable PROMs

This family includes densities from 64K to 1 Mbit and is suited for applications with extremely low power consumption. The line is available in standard CERDIPs and surface mount packages with windows. New product development is expanding the offering to higher densities and to speeds under 100 ns.

CMOS One-Time PROMs

These products have the programming features of the EPROMS but are much more cost effective since they are not reprogrammable and come in plastic packages. All devices are available in standard DIPs and several are offered in flat packages and leaded chip carriers.

Fujitsu's MOS Memory Products (Continued)

CMOS EEPROMs

These user-programmable, electrically erasable products are used for systems that require in-system reprogrammability. Such applications include digital instrumentation, industrial controls, and systems such as point-of-sale terminals. The features include latched addresses, self-timed write cycles, and write-protect circuitry.

NMOS Non-Volatile RAMs

Fujitsu's NMOS non-volatile RAMs combine a high-speed static RAM with an EEPROM to provide read and write capability together with non-volatile storage. These RAMs are used in systems that require volatile memory that can be change at fast microprocessor speed. The features include an unlimited recall endurance and a 10-year data retention store.

CMOS Mask ROMs

These factory-programmed devices are available in densities from 258K to 48Mbits and are ideal for problem-free designs in high-volume production. These products are not reprogrammable and come in plastic packages. New product development will increase the density offering to 8Mbits and beyond.

Alphanumeric Index of MOS Memory Products

Alphanumeric Index of MOS Memory Products (Continued)

Section 1

NMOS DRAMs

Page	Device	Maximum Access Time (ns)	Capacity	Package Options			Sealing Method
1-3	MB81256-10	100	262144 bits	16-pin	Plastic	DIP	Plastic
	MB81256-12	120	(262144w x 1b)	16-pin	Ceramic	DIP	Metal
	MB81256-15	150		16-pin	Ceramic	DIP	CERDIP
				16-pin	Plastic	ZIP	Plastic
				18-pad	Plastic	LCC	Plastic
				18-pad	Ceramic	LCC	Frit Glass
1-25	MB81256-80	80	262144 bits	16-pin	Plastic	DIP	Plastic
			(262144w x 1b)	16-pin	Ceramic	DIP	Metal
				16-pin	Plastic	ZIP	Plastic
				18-pad	Plastic	LCC	Plastic
1-45	MB81257-10	100	262144 bits	16-pin	Plastic	DIP	Plastic
	MB81257-12	120	(262144w x 1b)	16-pin	Ceramic	DIP	Metal
	MB81257-15	150		16-pin	Ceramic	DIP	CERDIP
				16-pin	Plastic	ZIP	Plastic
				18-pad	Plastic	LCC	Plastic
				18-pad	Ceramic	LCC	Frit Glass
1-69	MB81257-80	80	262144 bits	16-pin	Plastic	DIP	Plastic
			(262144w x 1b)	16-pin	Ceramic	DIP	Metal
				16-pin	Plastic	ZIP	Plastic
				18-pad	Plastic	LCC	Plastic
1-93	MB81464-10	100	262144 bits	18-pin	Plastic	DIP	Plastic
	MB81464-12	120	(65536w x 4b)	18-pin	Ceramic	DIP	Metal
	MB81464-15	150		18-pad	Plastic	LCC	Plastic
				20-pin	Plastic	ZIP	Plastic

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FUJITSU

MOS 262144-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 81256-10
MB 81256-12
MB 81256-15

December 1985
Edition 4.1

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY

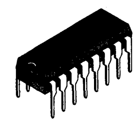
The Fujitsu MB 81256 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permits the MB 81256 to be housed in a standard 16 pin DIP/ZIP and 18 pad LCC. Pin-out conform to the JEDEC approved pin out. Additionally, the MB 81256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability. The MB 81256 also features "page mode" which allows high speed random access to up to 512 bits within a same row.

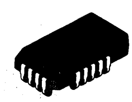
The MB 81256 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply torelance is very wide. All inputs are TTL compatible.

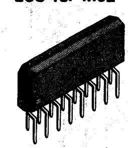
- 262,144 x 1 RAM, 16 pin DIP and ZIP/18 pad LCC
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row access time,
  - 100 ns max. (MB 81256-10)
  - 120 ns max. (MB 81256-12)
  - 150 ns max. (MB 81256-15)
- Cycle time,
  - 200 ns min. (MB 81256-10)
  - 220 ns min. (MB 81256-12)
  - 260 ns min. (MB 81256-15)
- Page cycle time,
  - 100 ns max. (MB 81256-10)
  - 120 ns max. (MB 81256-12)
  - 145 ns max. (MB 81256-15)
- Single +5V Supply, ±10% tolerance
- Low power,
  - 385 mW max. (MB 81256-10)
  - 358 mW max. (MB 81256-12)
  - 314 mW max. (MB 81256-15)
  - 25 mW max. (standby)
- 256 refresh cycles every 4ms
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- High speed Read-while-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD}, are eliminated
- Output unlatched at cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-pin Ceramic (Seam Weld) DIP (Suffix: -C)
  Standard 16-pin Ceramic (Cerdip) DIP (Suffix: -Z)
  Standard 16-pin Plastic DIP (Suffix: -P)
  Standard 18-pad Ceramic LCC (Suffix: -TV)
  Standard 18-pin plastic LCC (Suffix: -PV)
  Standard 16-pin Plastic ZIP (Suffix. -PSZ)



PLASTIC PACKAGE
DIP-16P-M03



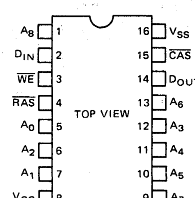
PLASTIC PACKAGE
LCC-18P-M02

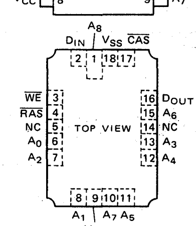


PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 17
DIP-16C-A04: See Page 18
DIP-16C-C04: See Page 19
LCC-18C-F04: See Page 24

PIN ASSIGNMENT





Pin assignment for ZIP: See Page 21

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	–1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	–1 to +7	V
Storage temperature	Ceramic	T_{STG}	–55 to +150	°C
	Plastic		–55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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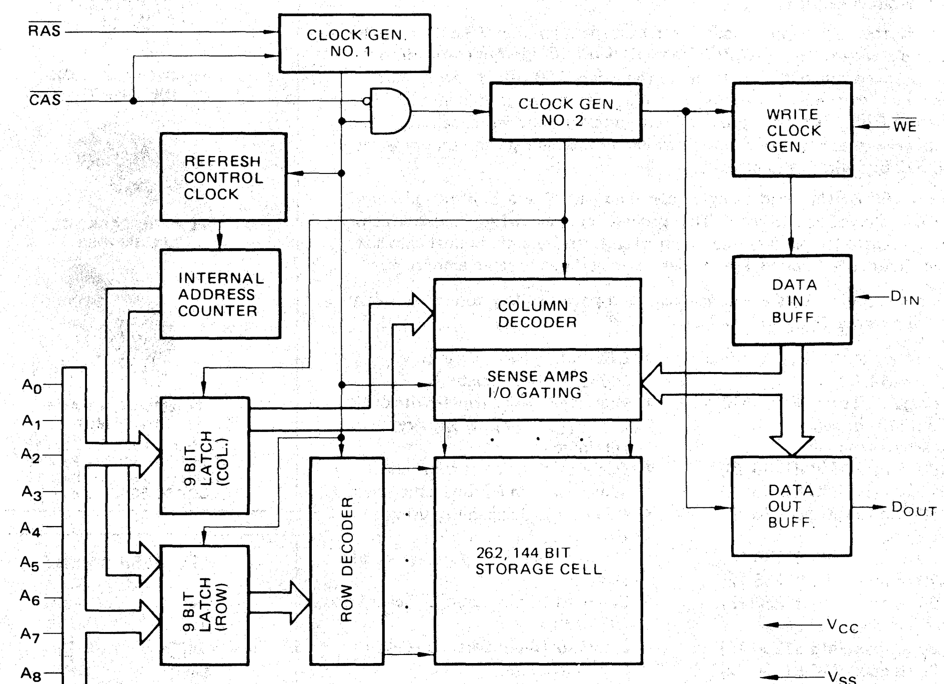
Fig. 1 — MB 81256 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		10	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value Min	Value Typ	Value Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	MB 81256-10	I_{CC1}			70	mA
	MB 81256-12				65	
	MB 81256-15				57	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$=V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81256-10	I_{CC3}			60	mA
	MB 81256-12				55	
	MB 81256-15				50	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = Min.)	MB 81256-10	I_{CC4}			35	mA
	MB 81256-12				30	
	MB 81256-15				25	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81256-10	I_{CC5}			65	mA
	MB 81256-12				60	
	MB 81256-15				55	
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10		10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output high Voltage (I_{OH} = -5.0 mA)		V_{OH}	2.4			V

NOTE * : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	MB 81256-10		MB 81256-12		MB 81256-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4		4	ms
Random Read/Write Cycle Time		t_{RC}	200		220		260		ns
Read-Write Cycle Time		t_{RWC}	200		220		260		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	85		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	55		60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		20		ns
Write Command Set Up Time	10	t_{WCS}	0		0		0		ns
Write Command Pulse Width		t_{WP}	15		20		25		ns
Write Command Hold Time		t_{WCH}	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		40		45		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	15		20		25		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		25		30		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter NOTES	Symbol	MB 81256-10		MB 81256-12		MB 81256-15		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)	t_{RPC}	20		20		20		ns
Page Mode Read/Write Cycle Time	t_{PC}	100		120		145		ns
Page Mode Read-Write Cycle Time	t_{PRWC}	100		120		145		ns
Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	40		50		60		ns
Refresh Counter Test Cycle Time 11	t_{RTC}	330		375		430		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width 11	t_{TRAS}	230	10000	265	10000	320	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time 11	t_{CPT}	50		60		70		ns

Notes:

1 An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.

2 AC characteristics assume t_T = 5 ns.

3 V_{IH} (min) and V_{IL} (max) are refrence levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).

4 Assumes that $t_{RCD} \leqq t_{RCD}$ (max.) If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

5 Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).

6 Measured with a load equivalent to 2 TTL loads and 100 pF.

7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

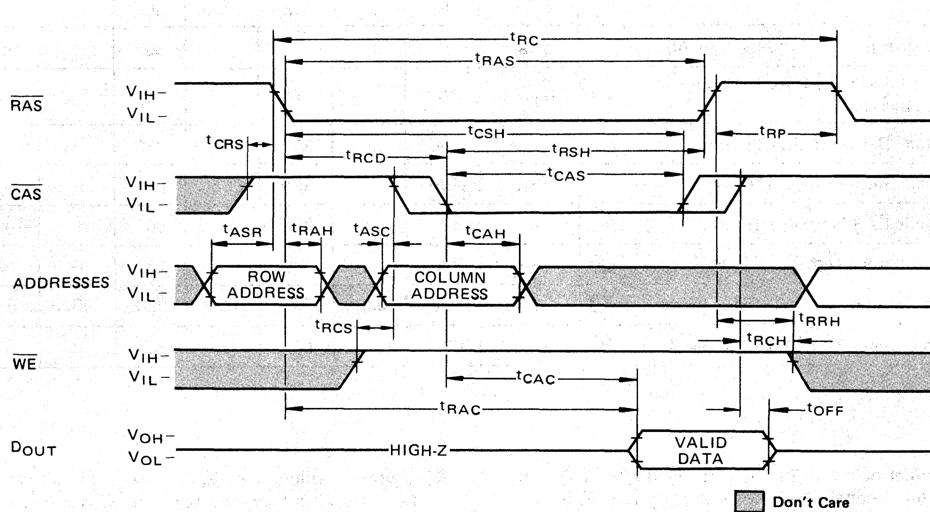
8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5ns) + t_{ASC} (min).

9 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

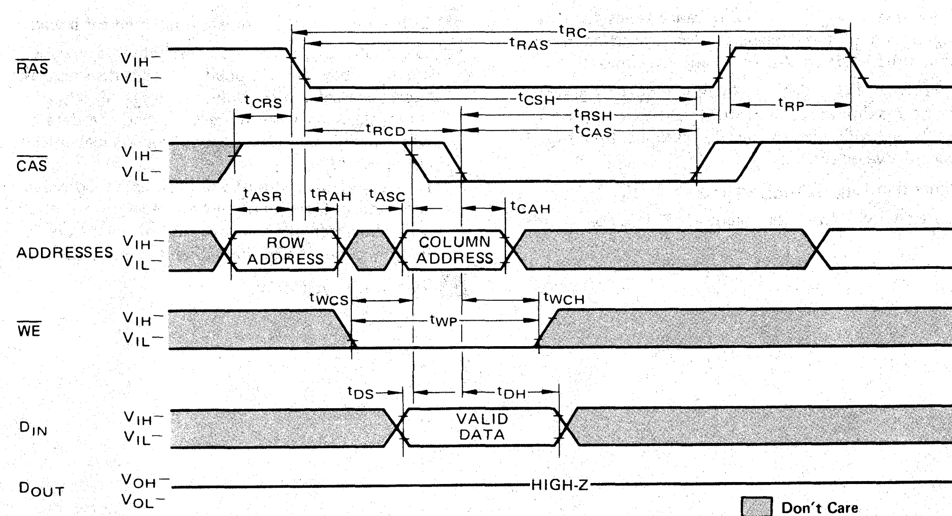
10 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
If $t_{CWD} \geqq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

11 Test mode cycle only.

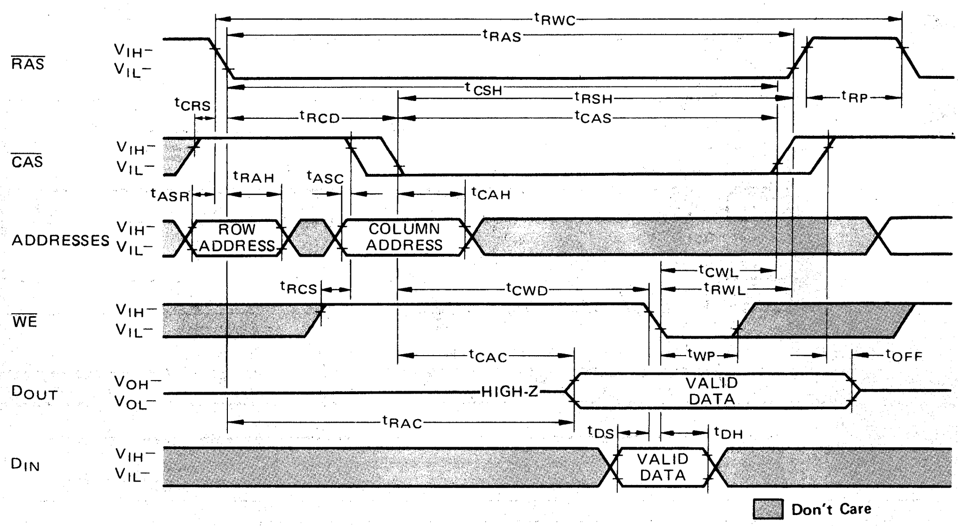
Read Cycle



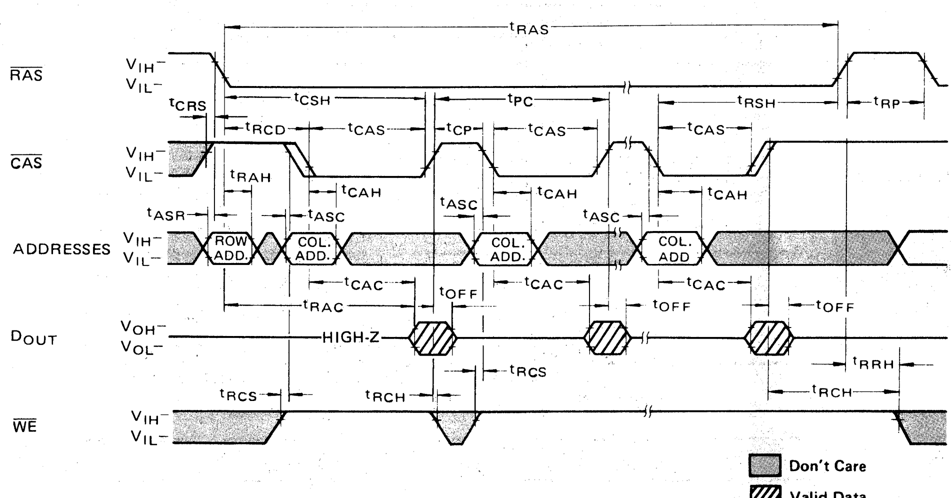
Write Cycle (Early Write)

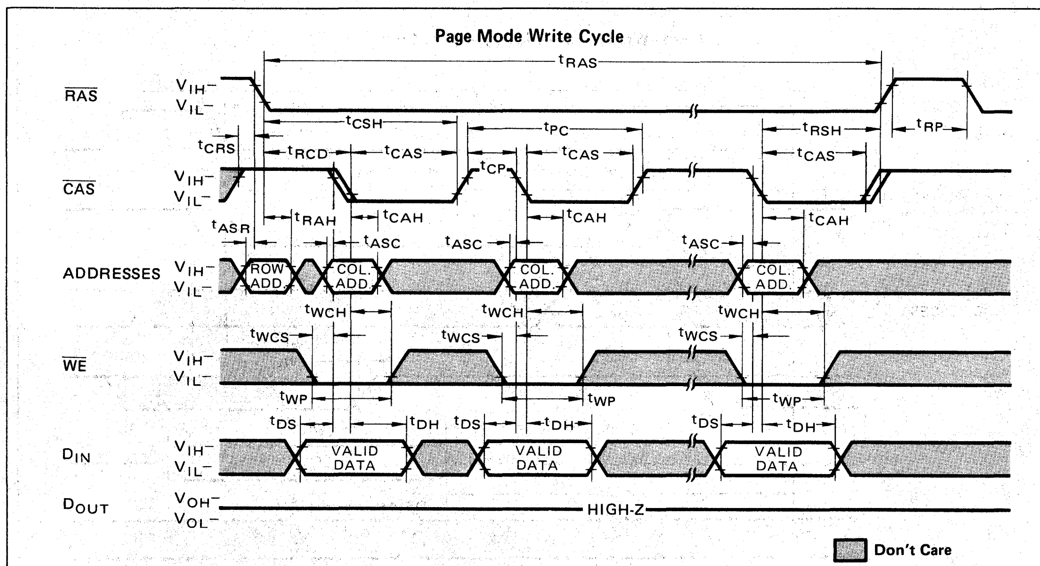


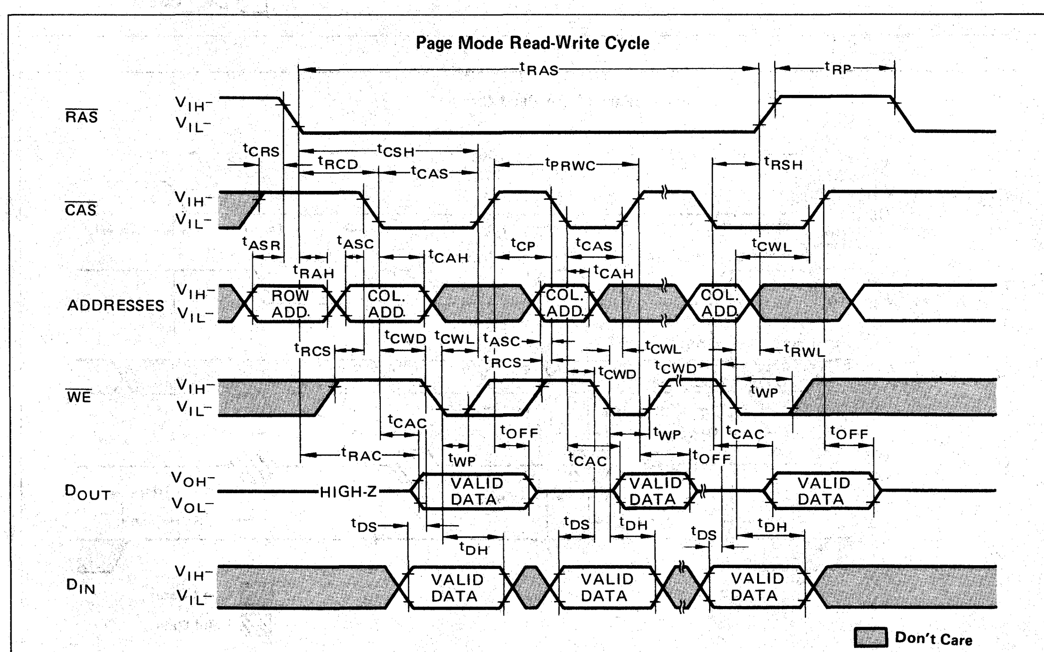
Read–Write/Read–Modify–Write Cycle



Page Mode Read Cycle

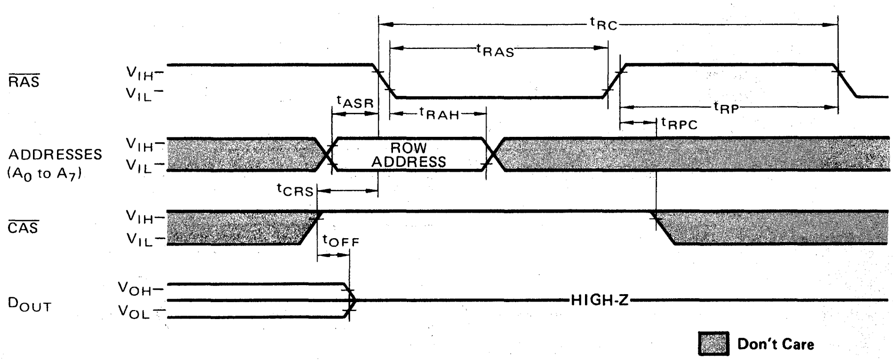



Page Mode Write Cycle
RAS
CAS
ADDRESSES
WE
DIN
DOUT
ROW ADD.
COL. ADD.
VALID DATA
HIGH-Z
Don't Care


Page Mode Read-Write Cycle
RAS
CAS
ADDRESSES
WE
DOUT
DIN
ROW ADD.
COL. ADD.
VALID DATA
HIGH-Z
Don't Care

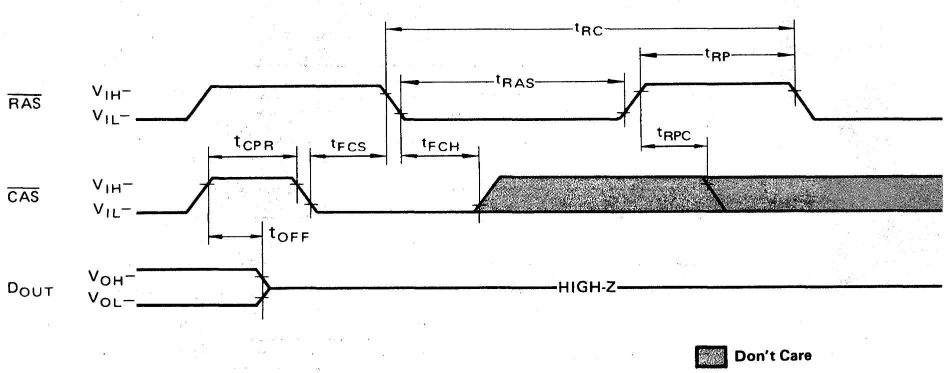
$\overline{RAS}$-only Refresh cycle

NOTE: $\overline{WE}$, D_{IN} = Don't care, A_8 = V_{IH} or V_{IL}

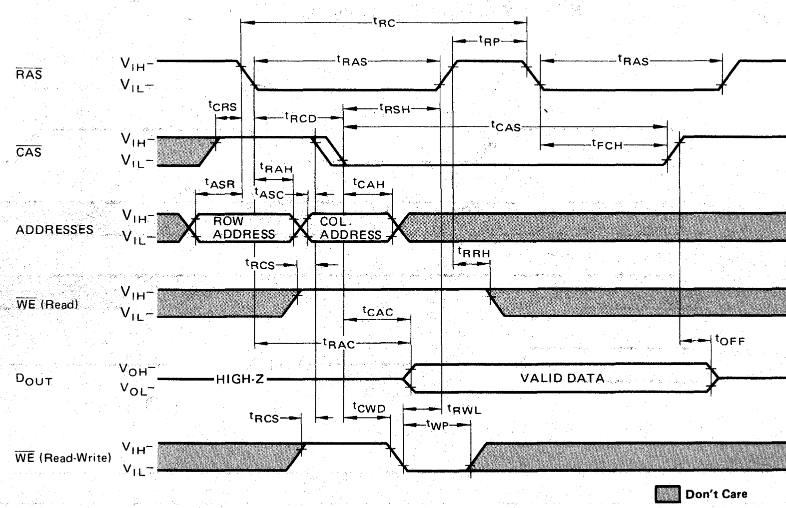


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

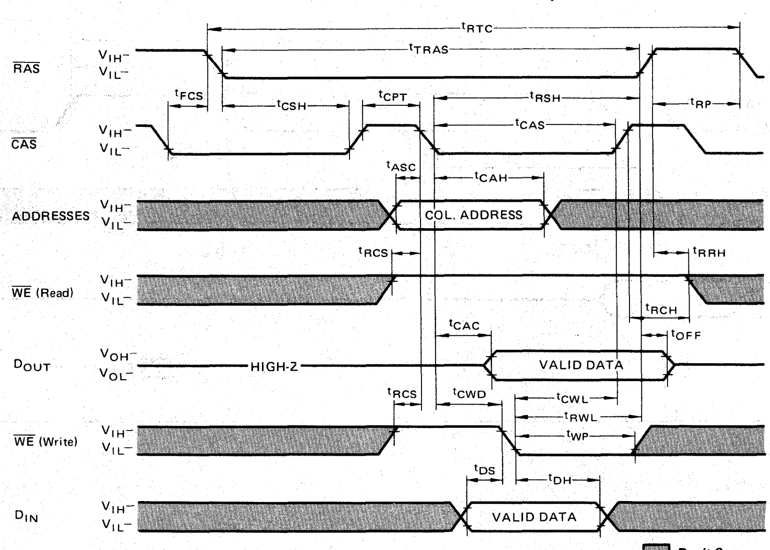
NOTE: Address, $\overline{WE}$, D_{IN} = Don't care



Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement

The MB 81256 has improved circuitry that eases timing requirements for high speed access operations. The MB 81256 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81256 has the minimal hold time of Address (t_{CAH}), WE (t_{WCH}) and D_{IN} (t_{DH}). The MB 81256 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirements that are referenced to RAS nonrestrictive and deleted them from the data sheet, these include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and WE as well as t_{CWD} (CAS to WE Delay) are not ristricted by t_{RCD}.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81256. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe (RAS). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe (CAS). All row addresses must be stable on or before the falling edge of RAS. CAS is internally inhibited (or "gated") by RAS to permit triggering of CAS as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-address.

Write Enable:

The read mode or write mode is selected with the WE input. A high on WE selects read mode; low selects write mode. The data input is disable when read mode is selected.

Data input:

Data is written into the MB 81256 during a write or read-write cycle. The later falling edge of WE or CAS is a strobe for the Data In (D_{IN}) register. In a write cycle, if WE is brought low before CAS, D_{IN} is strobed by CAS, and the set-up and hold times are referenced to CAS. In a read-write cycle, WE can be delayed after CAS has been low and CAS to WE Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by WE, and set-up and hold times are referenced to WE.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until CAS is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of RAS when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of CAS when the transition occurs after t_{RCD} (max). Data remain valid until CAS is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle

The MB 81256 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of WE when CAS goes low. When WE is low during CAS transition to low, the MB 81256 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when WE goes low after t_{CWD} following CAS transition to low, the MB 81256 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle (t_{RWC} = t_{RC}) is possible with the MB 81256.

Page Mode:

Page-mode operation permits strobing the row-address into the MB 81256 while maintaining RAS at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of RAS is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4ms. The MB 81256 offers the following 3 types of refresh.

RAS-only Refresh;

RAS-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless CAS is brought low.
Strobing each of 256 row-addresses (A_0 to A_7) with RAS will cause all bits in each row to be refreshed. Further RAS-only refresh results in a substantial reduction in power dissipation. During RAS-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

CAS-before-RAS Refresh;

CAS-before-RAS refreshing available on the MB 81256 offers an alternate refresh method. If CAS is held "low" for the specified period (t_{FCS}) before RAS goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next CAS-before-RAS refresh operation.

Hidden Refresh;

A hidden refresh cycle may takes place while maintaining the latest valid data at the output by extending CAS active time.
For the MB 81256 a hidden refresh is a CAS-before-RAS refresh cycle. The internal refresh address counters provide the refresh addresses, as in a normal CAS-before-RAS refresh cycle.

CAS-before-RAS Refresh Counter Test Cycle:

A special timing sequence using CAS-

before-$\overline{\text{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh activated circuitry.
After the $\overline{\text{CAS}}$-befor-$\overline{\text{RAS}}$ refresh operation, if $\overline{\text{CAS}}$ goes to high and then goes to low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled.
This is shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and column address (9 bits) to be accessed can be defined as follows:

*A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.

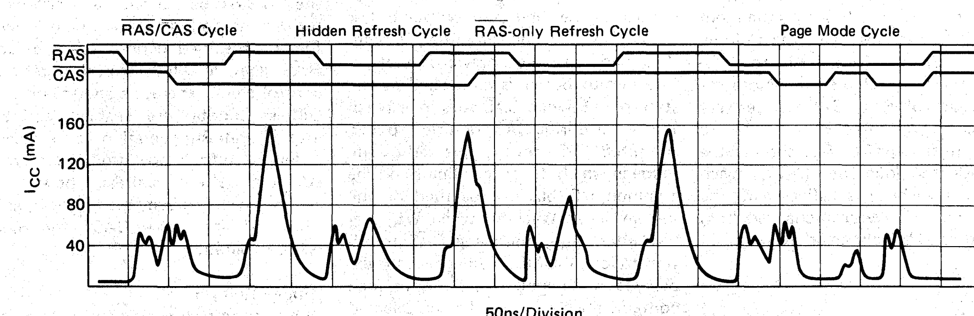
*A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{\text{CAS}}$.

Suggested $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Procedure

The timing as shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test cycles is used for the following operations:

(1) Initialize the internal refresh address counter by using eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles.
(2) Throughout the test, use the same column address, and keep RA8 high.
(3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
(4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
(5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
(6) Complement the test pattern and repeat step 3), 4) and 5).

Fig. 2 – CURRENT WAVEFORM (V_{CC}=5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

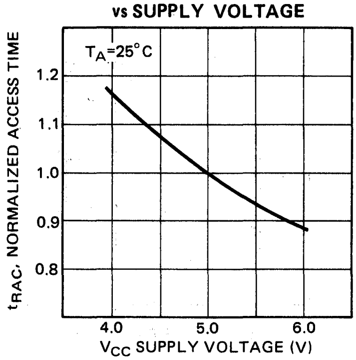


Fig. 4 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

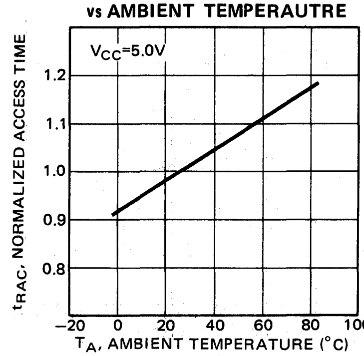


Fig. 5 – OPERATING CURRENT vs CYCLE RATE

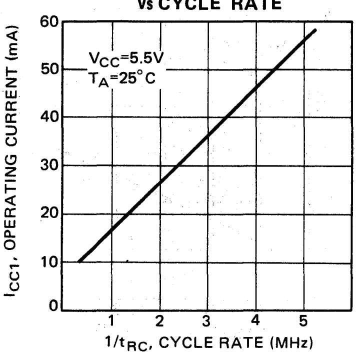


Fig. 6 – OPERATING CURRENT vs SUPPLY VOLTAGE

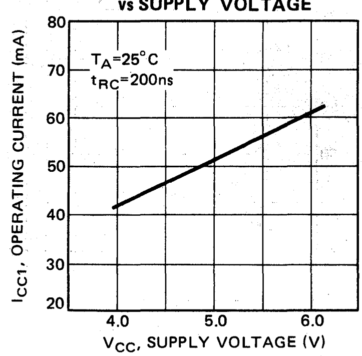


Fig. 7 – OPERATING CURRENT vs AMBIENT TEMPERATURE

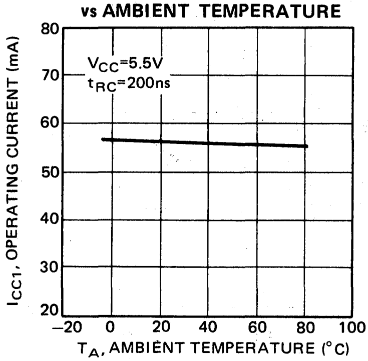


Fig. 8 – STANDBY CURRENT vs SUPPLY VOLTAGE

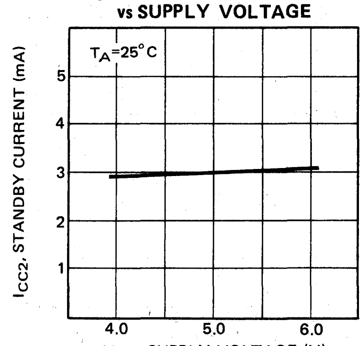


Fig. 9 — STANDBY CURRENT vs AMBIENT TEMPERATURE

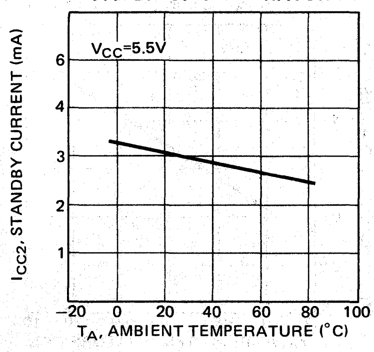


Fig. 10 — REFRESH CURRENT 1 vs CYCLE RATE

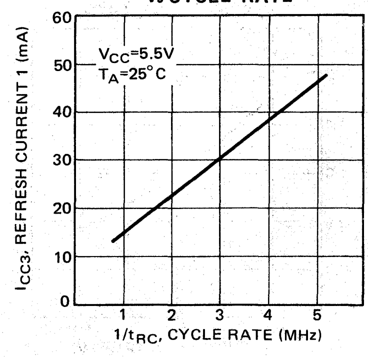


Fig. 11 — REFRESH CURRENT 1 vs SUPPLY VOLTAGE

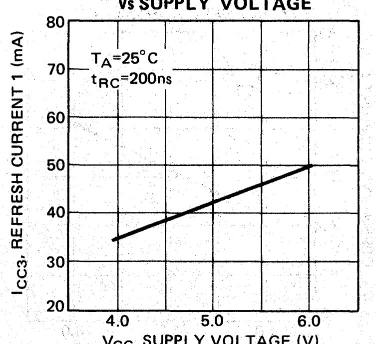


Fig. 12 — PAGE MODE CURRENT vs CYCLE RATE

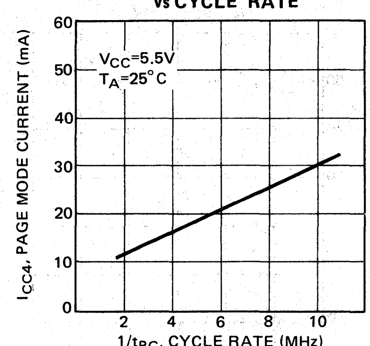


Fig. 13 — PAGE MODE CURRENT vs SUPPLY VOLTAGE

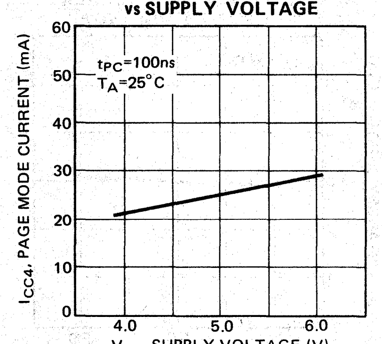


Fig. 14 — REFRESH CURRENT 2 vs CYCLE RATE

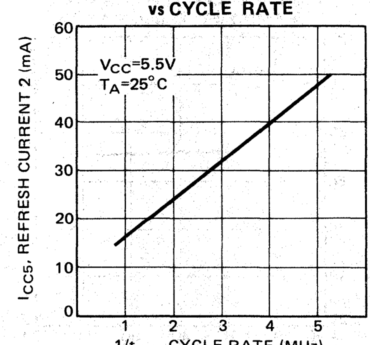


Fig. 15 — REFRESH CURRENT 2 vs SUPPLY VOLTAGE

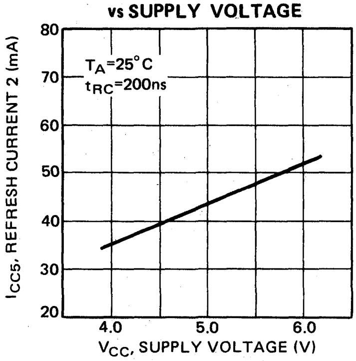


Fig. 16 — ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

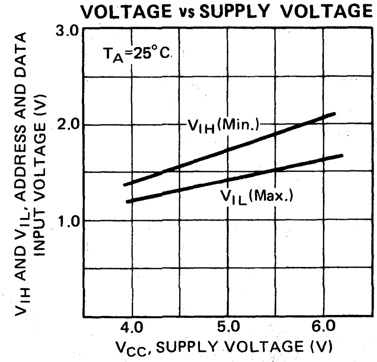


Fig. 17 — ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

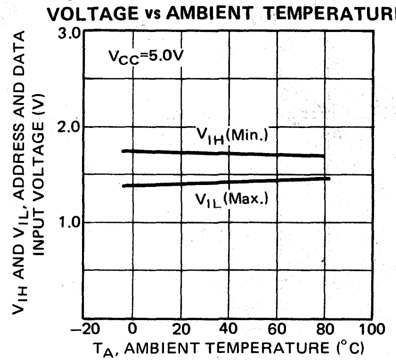


Fig. 18 — $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

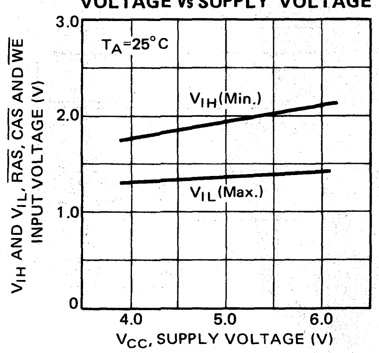


Fig. 19 — $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

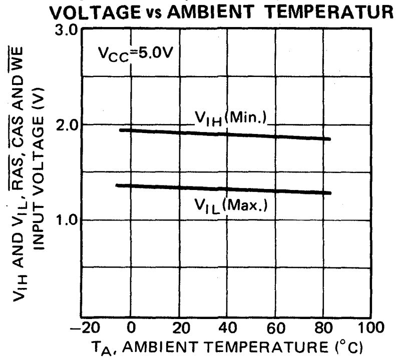


Fig. 20 — ACCESS TIME vs LOAD CAPACITANCE

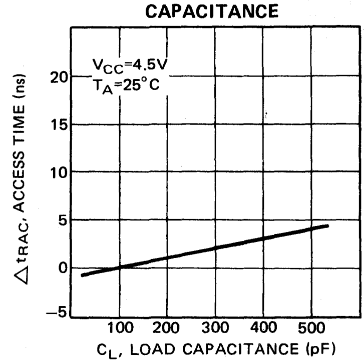


Fig. 21 – OUTPUT CURRENT vs OUTPUT VOLTAGE

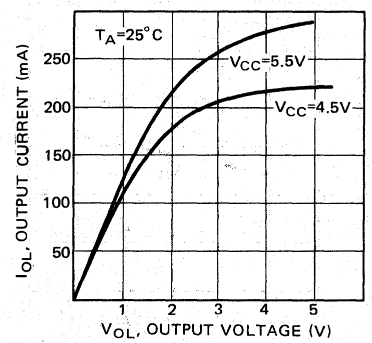


Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

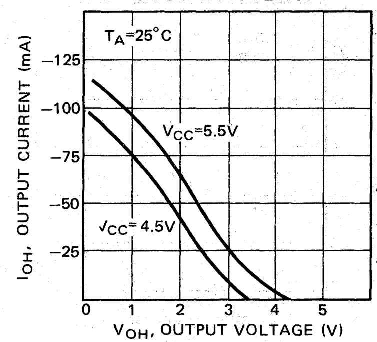


Fig. 23 – CURRENT WAVEFORM DURING POWER UP

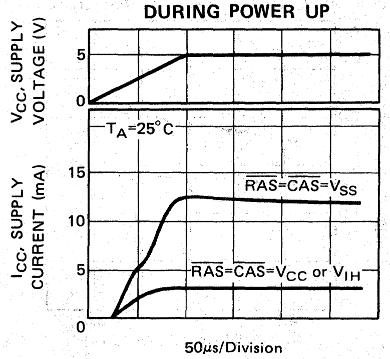
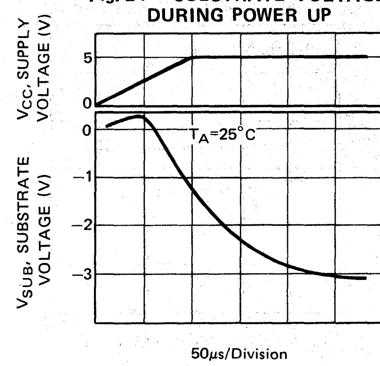
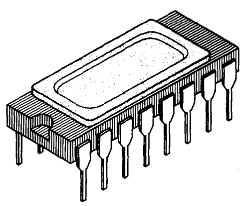


Fig. 24 – SUBSTRATE VOLTAGE DURING POWER UP



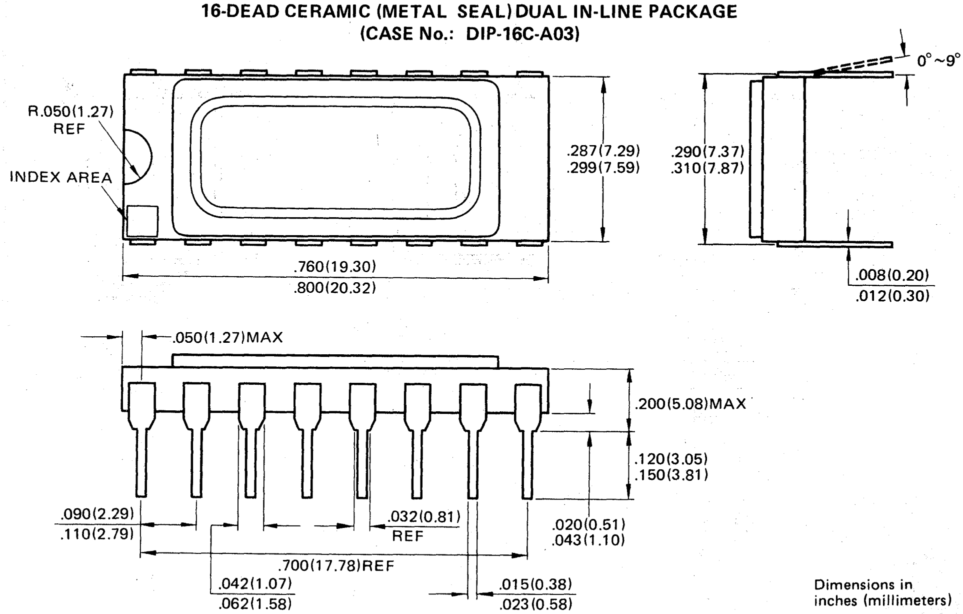
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A03

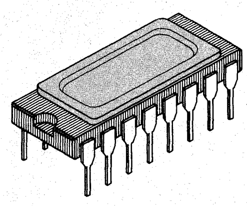
16-DEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A03)



Dimensions in inches (millimeters)

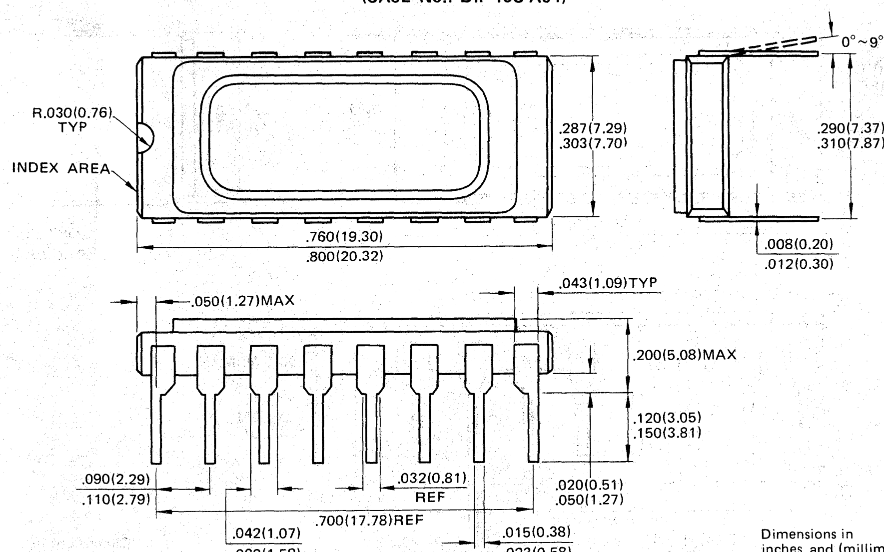
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A04

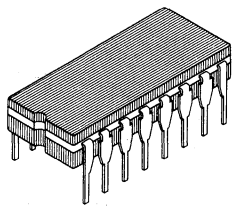
16-LEAD SEAM WELD DIP PACKAGE
(CASE No.: DIP-16C-A04)



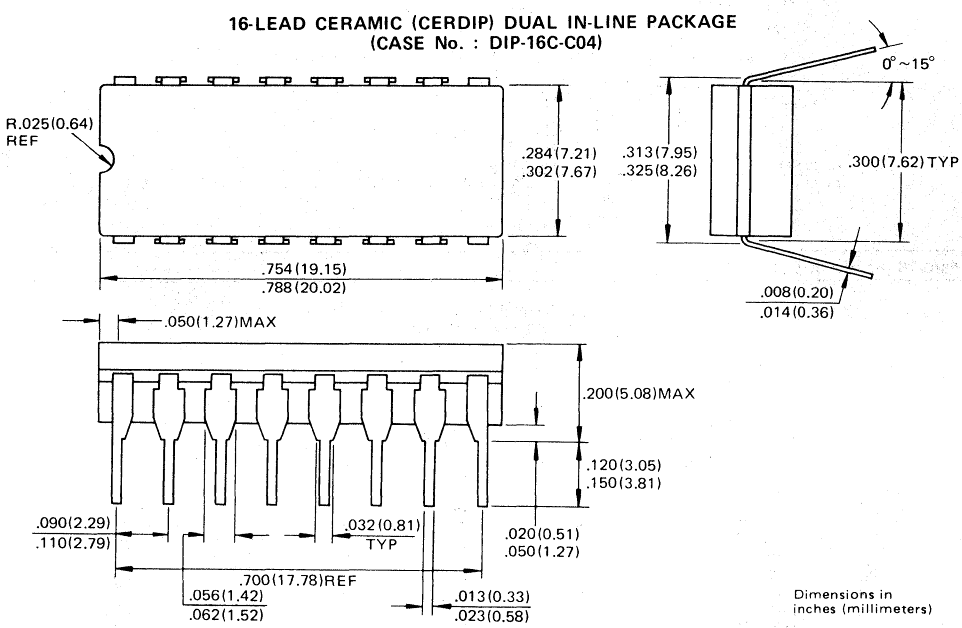
Dimensions in
inches and (millimeters)

PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -Z)

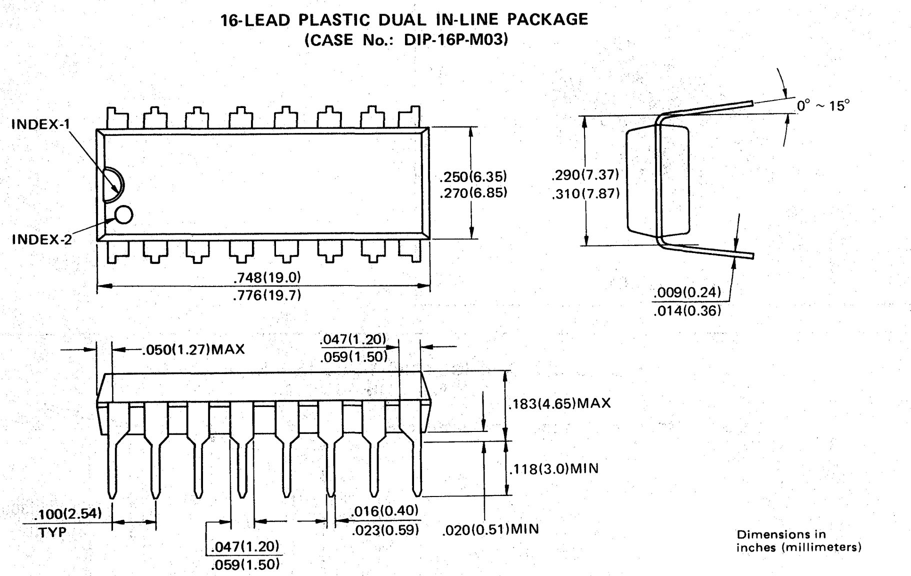


DIP-16C-C04

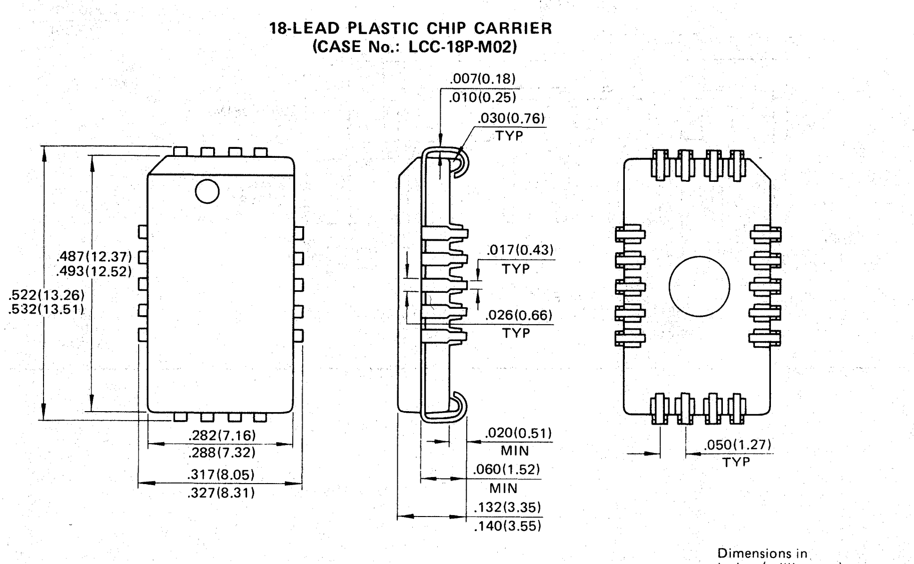


PACKAGE DIMENSIONS

Standard 16-pin Plastic DIP (Suffix: -P)



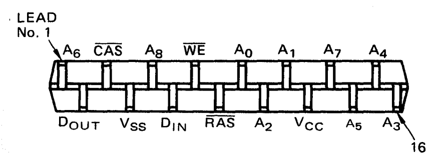
Standard 18-pin Plastic LCC (Suffix: -PV)



PACKAGE DIMENSIONS

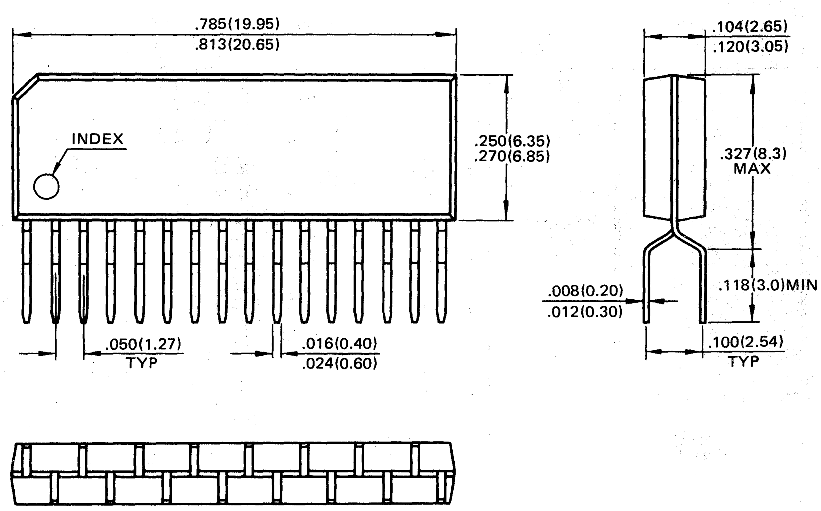
Standard 16-pin Plastic ZIP (Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

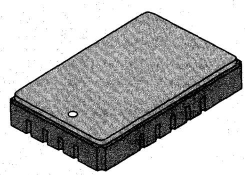
16 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE (CASE No.: ZIP-16P-M01)



Dimensions in inches (millimetres)

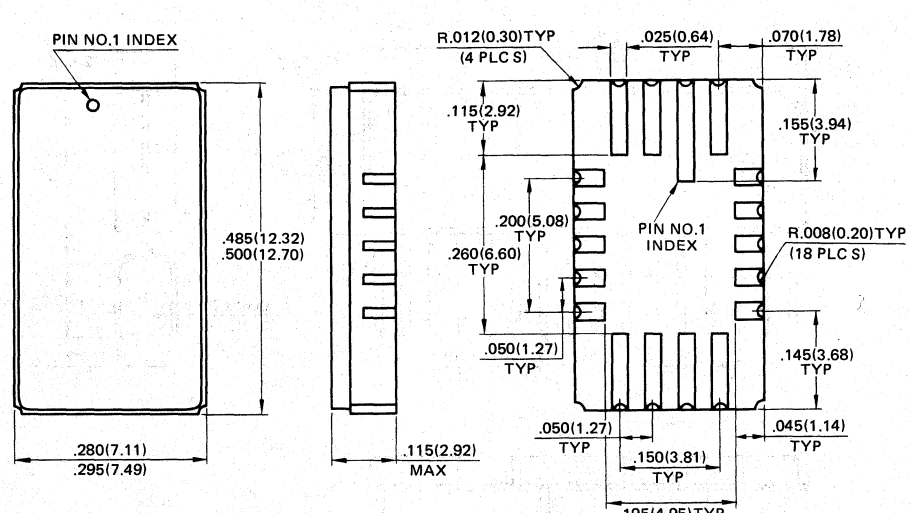
PACKAGE DIMENSIONS

Standard 18-pad Ceramic LCC (Suffix: -TV)



LCC-18C-F04

18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F04)



Dimension in inches (millimeters).

*Shape of Pin 1 index: Subject to change without notice

FUJITSU

MOS 262144-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 81256-80

1

March 1987
Edition 1.0

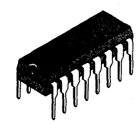
262,144-BIT DYNAMIC RANDOM ACCESS MEMORY

The Fujitsu MB 81256 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

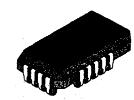
Multiplexed row and column address inputs permits the MB 81256 to be housed in a standard 16 pin DIP/ZIP and 18 pad LCC. Pin-out conform to the JEDEC approved pin out. Additionally, the MB 81256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability. The MB 81256 also features "page mode" which allows high speed random access to up to 512 bits within a same row.

The MB 81256 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

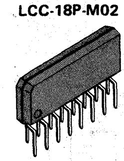
Clock timing requirements are noncritical, and power supply torelance is very wide. All inputs are TTL compatible.



PLASTIC PACKAGE
DIP-16P-M03



PLASTIC PACKAGE
LCC-18P-M02

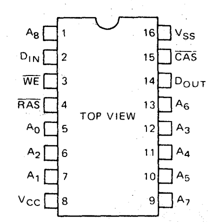


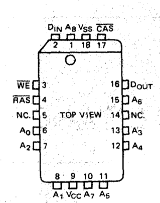
PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 17
DIP-16C-A04: See Page 18

- 262,144 x 1 RAM, 16 pin DIP and ZIP/18 pad LCC
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row access time (t_{RAC}), 80ns max. (MB 81256-80)
- Randam cycle time (t_{RC}), 175ns min. (MB 81256-80)
- Page mode cycle time (t_{PC}), 100ns min. (MB 81256-80)
- Single +5V supply, ±10% tolerance
- Lower power, 385mW max. (MB 81256-80) 25mW max. (standby)
- 256 refresh cycles every 4ms
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- High speed Read-while-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD}, are eliminated
- Output unlatched at cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-pin Plastic DIP (Suffix: -P)
- Standard 18-pin Plastic LCC (Suffix: -PD)
- Standard 16-pin Plastic ZIP (Suffix: -PSZ)
- Standard 16-pin Ceramic DIP (Suffix: -C)

PIN ASSIGNMENT





Pin assignment for ZIP: See Page 22

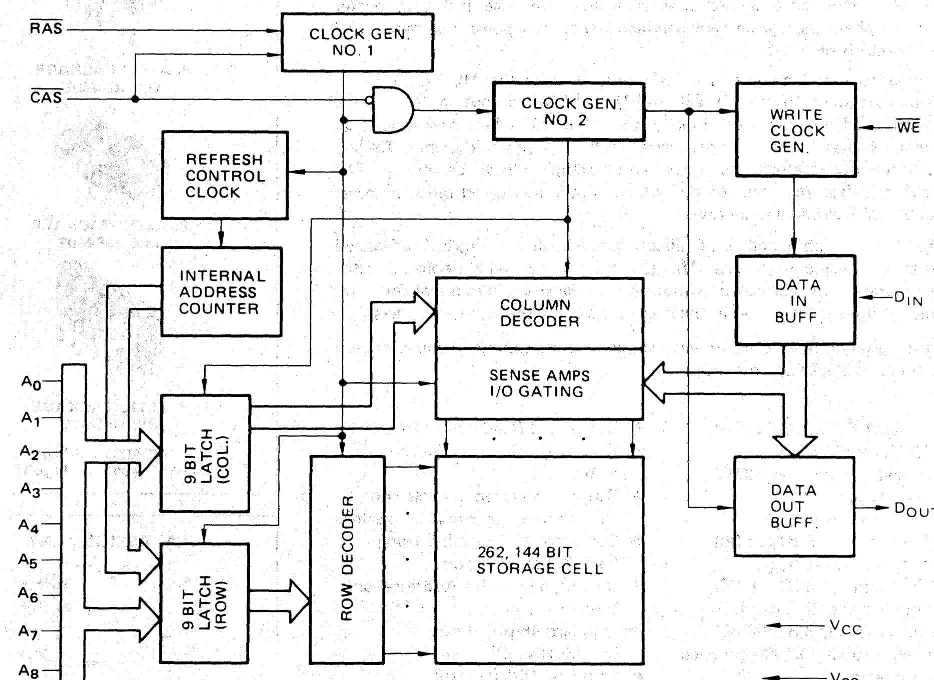
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 81256 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		10	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	MB 81256-80	I_{CC1}			70	mA
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81256-80	I_{CC3}			60	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = Min.)	MB81256-80	I_{CC4}			35	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81256-80	I_{CC5}			65	mA
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	−10		10	µA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	−10		10	µA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0mA)		V_{OH}	2.4			V

NOTE* : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
Time between Refresh		t_{REF}		4	ms
Random Read/Write Cycle Time		t_{RC}	175		ns
Read-Write Cycle Time		t_{RWC}	180		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		80	ns
Access Time from $\overline{CAS}$	4 6	t_{CAC}		45	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	ns
Transition Time		t_T	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	85	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	50		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	50	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	85		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	35	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		ns
Row Address Set Up Time		t_{ASR}	0		ns
Row Address Hold Time		t_{RAH}	10		ns
Column Address Set Up Time		t_{ASC}	0		ns
Column Address Hold Time		t_{CAH}	15		ns
Read Command Set Up Time		t_{RCS}	0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		ns
Write Command Set Up Time	10	t_{WCS}	0		ns
Write Command Pulse Width		t_{WP}	15		ns
Write Command Hold Time		t_{WCH}	15		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		ns
Data In Set Up Time		t_{DS}	0		ns
Data In Hold Time		t_{DH}	15		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	15		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		ns

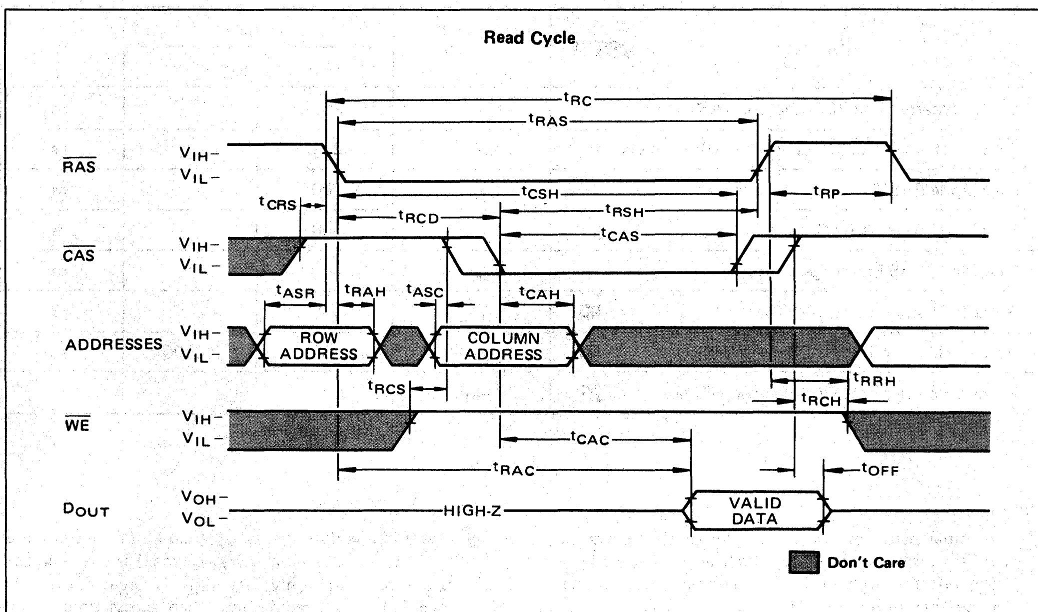
AC CHARACTERISTICS

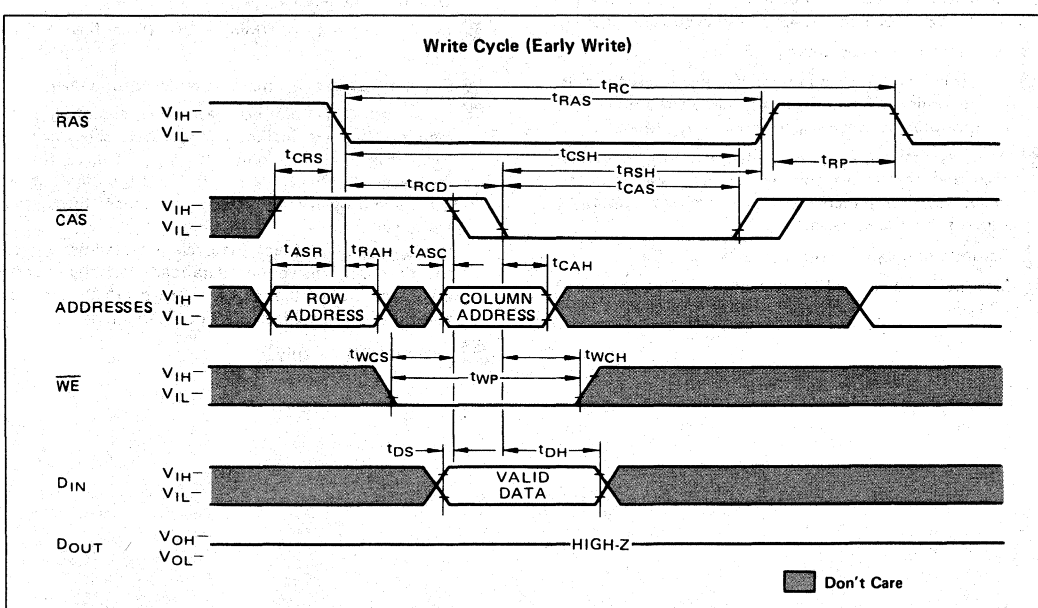
(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		ns
Page Mode Read/Write Cycle Time		t_{PC}	100		ns
Page Mode Read-Write Cycle Time		t_{PRWC}	100		ns
Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	40		ns
Refresh Counter Test Cycle Time	11	t_{RTC}	330		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	11	t_{TRAS}	230	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	11	t_{CPT}	50		ns

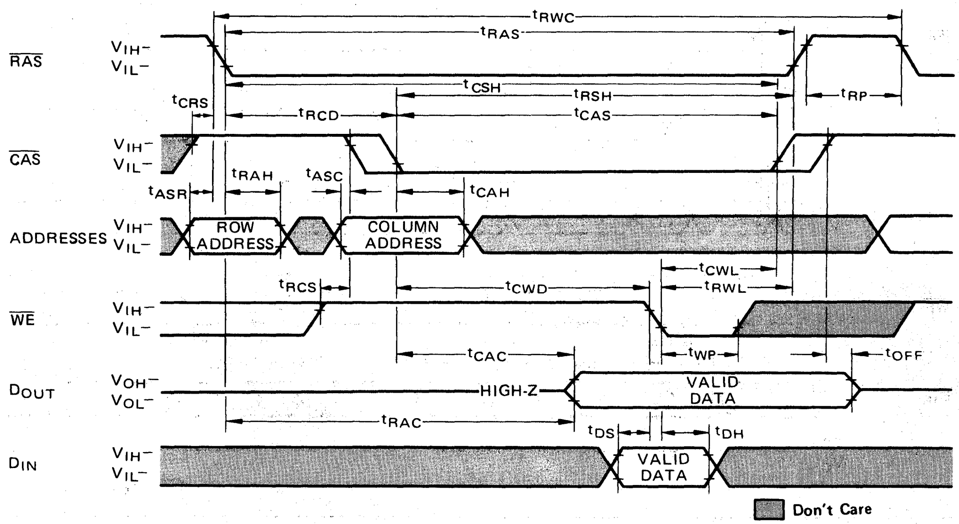
Notes:

1. An initial pause of 200 µs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are refrence levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.) If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5ns) + t_{ASC} (min).
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
    If $t_{CWD} \geqq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
11. Test mode cycle only.

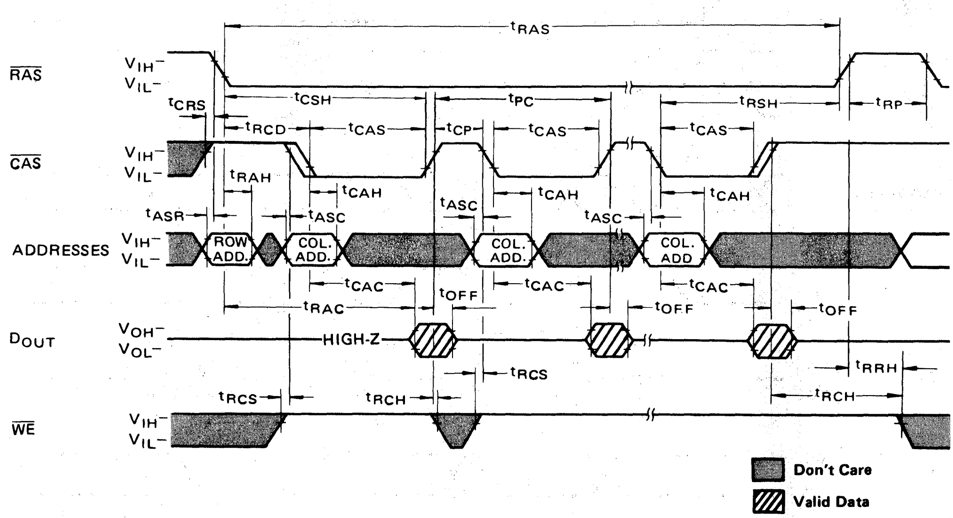

Read Cycle
tRC
tRAS
RAS
VIH–
VIL–
tCRS
tCSH
tRP
tRCD
tRSH
tCAS
CAS
VIH–
VIL–
tASR
tRAH
tASC
tCAH
ADDRESSES
VIH–
VIL–
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
tRCH
WE
VIH–
VIL–
tCAC
tRAC
tOFF
DOUT
VOH–
VOL–
HIGH-Z
VALID DATA
Don't Care


Write Cycle (Early Write)
tRC
tRAS
RAS
VIH–
VIL–
tCRS
tCSH
tRP
tRSH
tRCD
tCAS
CAS
VIH–
VIL–
tASR
tRAH
tASC
tCAH
ADDRESSES
VIH–
VIL–
ROW ADDRESS
COLUMN ADDRESS
tWCS
tWCH
WE
VIH–
VIL–
tWP
tDS
tDH
DIN
VIH–
VIL–
VALID DATA
DOUT
VOH–
VOL–
HIGH-Z
Don't Care

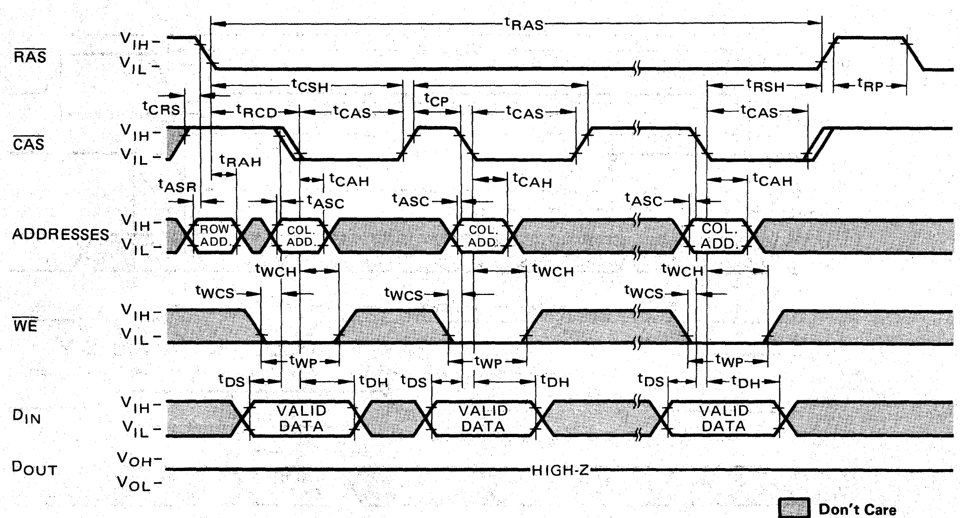
Read–Write/Read–Modify–Write Cycle



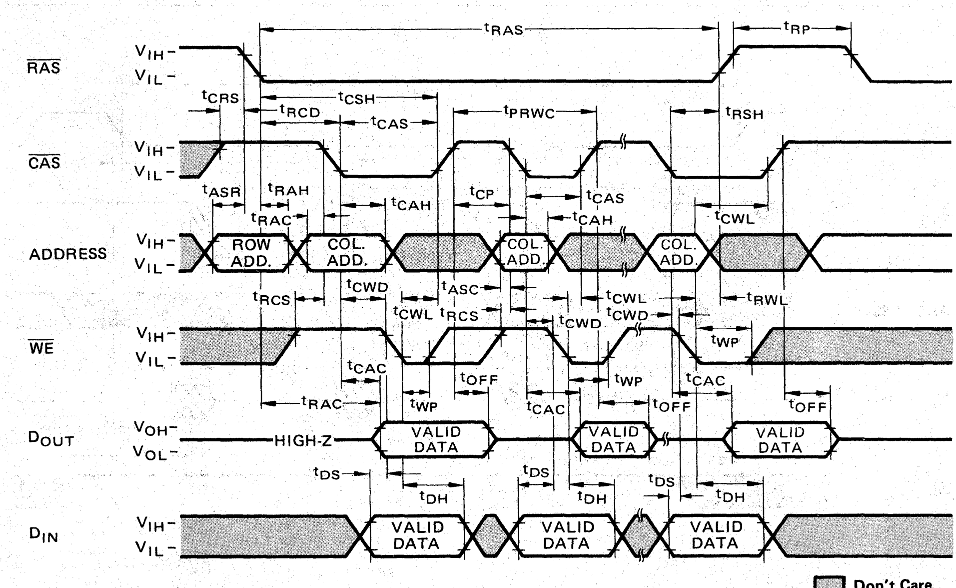
Page Mode Read Cycle



Page Mode Write Cycle (Early Write)

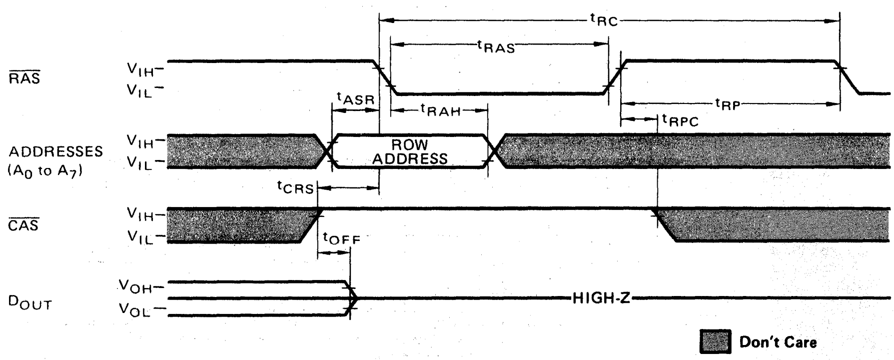


Page Mode Read-Write Cycle



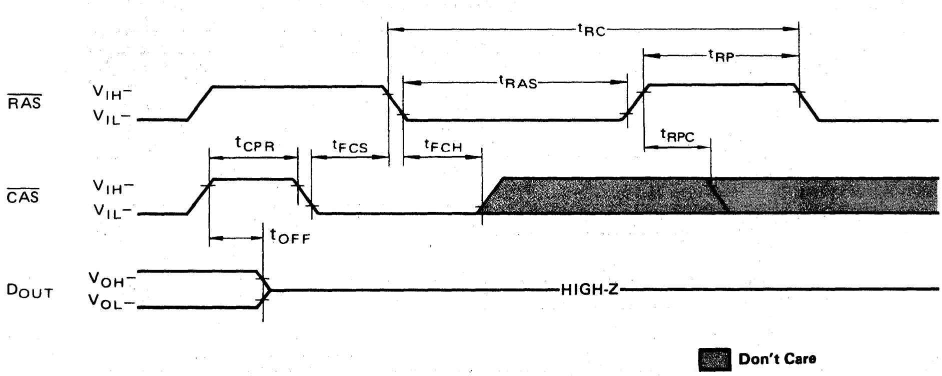
$\overline{RAS}$-only Refresh cycle

NOTE: $\overline{WE}$, D_{IN} = Don't care, A_8 = V_{IH} or V_{IL}

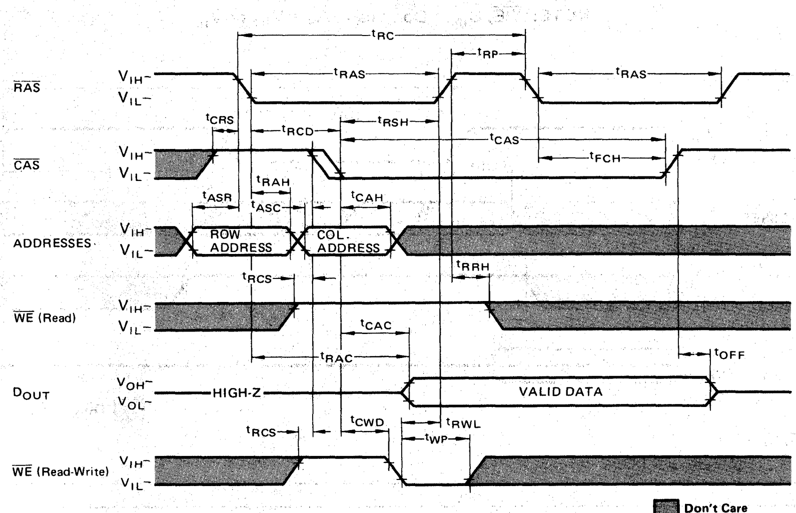


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

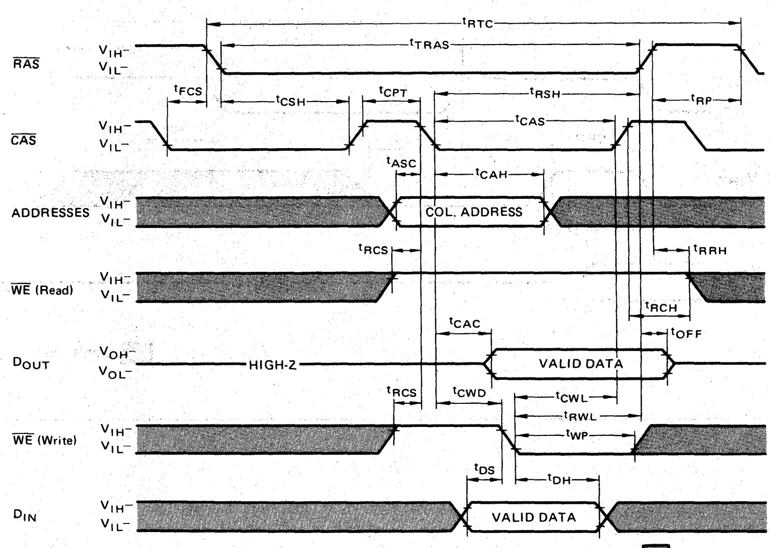
NOTE: Address, $\overline{WE}$, D_{IN} = Don't care



Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement
The MB 81256 has improved circuitry that eases timing requirements for high speed access operations. The MB 81256 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81256 has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 81256 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ nonrestrictive and deleted them from the data sheet, these include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Address Inputs:
A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81256. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-address.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode; low selects write mode. The data input is disable when read mode is selected.

Data input:
Data is written into the MB 81256 during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be delayed after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle
The MB 81256 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MB 81256 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB 81256 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle is possible with the MB 81256.

Page Mode:
Page-mode operation permits strobing the row-address into the MB 81256 while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4ms. The MB 81256 offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh;
$\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low.
Strobing each of 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81256 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh;
A hidden refresh cycle may takes place while maintaining the latest valid data at the output by extending $\overline{CAS}$ active time.
For the MB 81256 a hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counters provide the refresh addresses, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-

before-$\overline{\text{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh activated circuitry.
After the $\overline{\text{CAS}}$-befor-$\overline{\text{RAS}}$ refresh operation, if $\overline{\text{CAS}}$ goes to high and then goes to low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled.
This is shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and column address (9 bits) to be accessed can be defined as follows:

*A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.

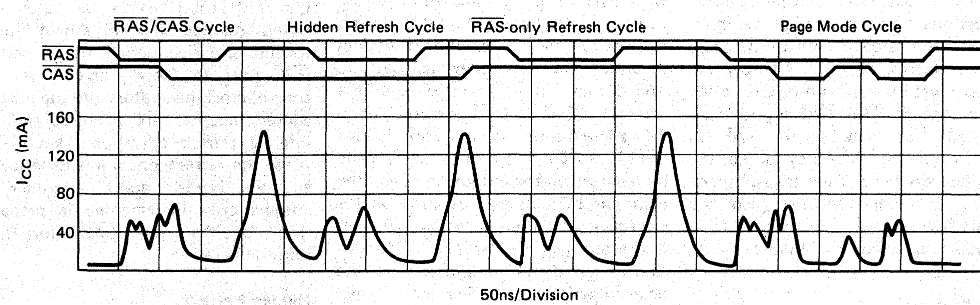
*A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{\text{CAS}}$.

Suggested $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Procedure

The timing as shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test cycles is used for the following operations:

(1) Initialize the internal refresh address counter by using eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles.
(2) Throughout the test, use the same column address, and keep RA8 high.
(3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
(4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
(5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
(6) Complement the test pattern and repeat step 3), 4) and 5).

Fig. 2 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

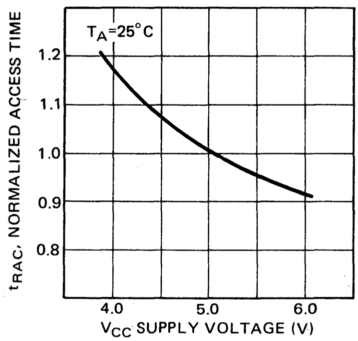


Fig. 4 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

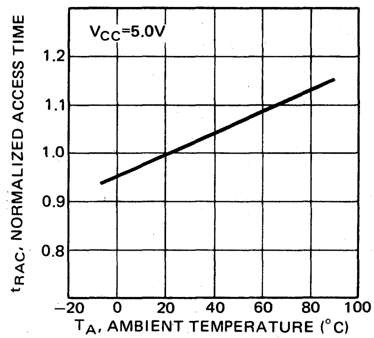


Fig. 5 – OPERATING CURRENT vs CYCLE RATE

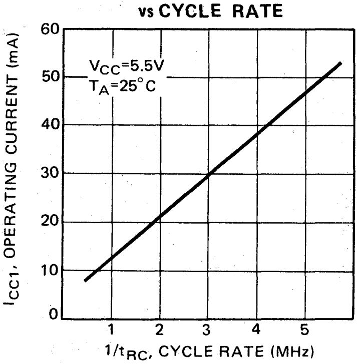


Fig. 6 – OPERATING CURRENT vs SUPPLY VOLTAGE

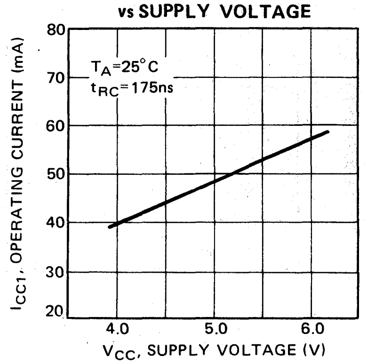


Fig. 7 – OPERATING CURRENT vs AMBIENT TEMPERATURE

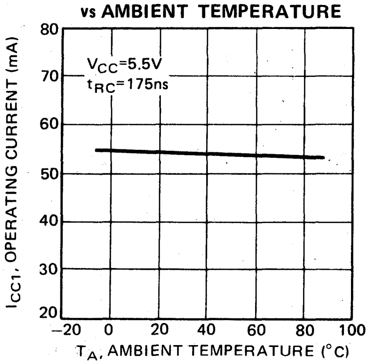


Fig. 8 – STANDBY CURRENT vs SUPPLY VOLTAGE

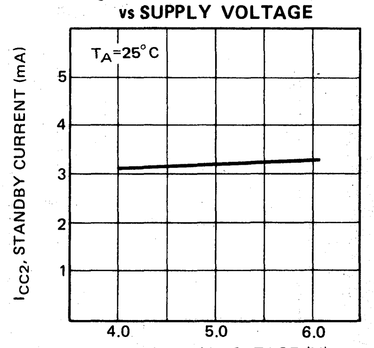


Fig. 9 — STANDBY CURRENT vs AMBIENT TEMPERATURE

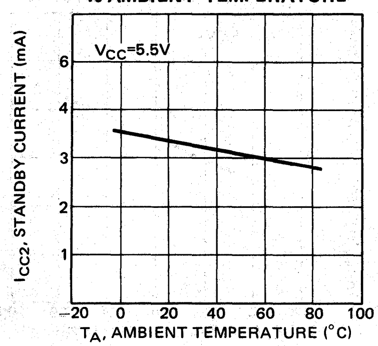


Fig. 10 — REFRESH CURRENT 1 vs CYCLE RATE

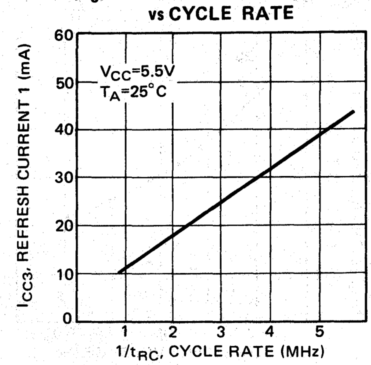


Fig. 11 — REFRESH CURRENT 1 vs SUPPLY VOLTAGE

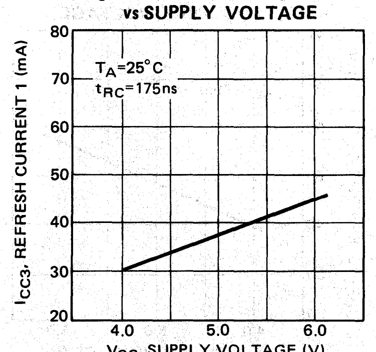


Fig. 12 — PAGE MODE CURRENT vs CYCLE RATE

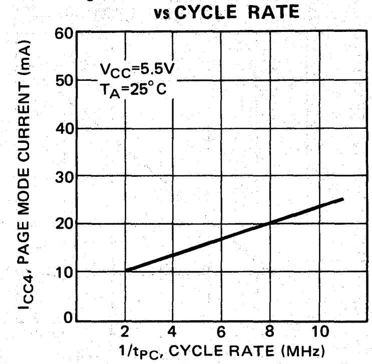


Fig. 13 — PAGE MODE CURRENT vs SUPPLY VOLTAGE

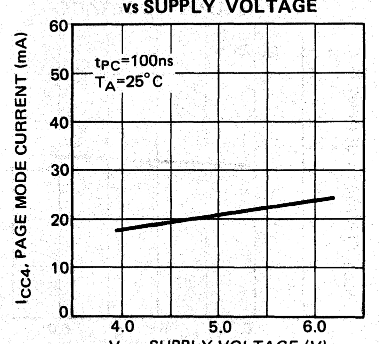


Fig. 14 — REFRESH CURRENT 2 vs CYCLE RATE

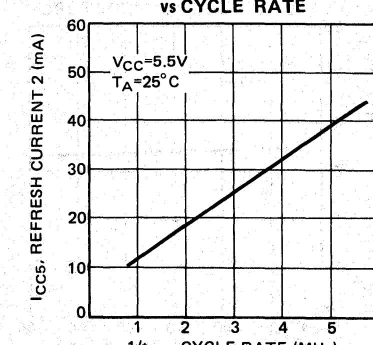


Fig. 15 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

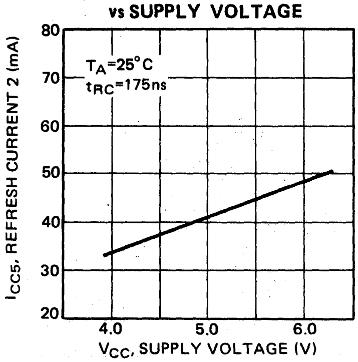


Fig. 16 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

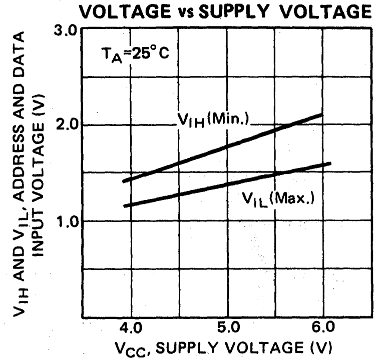


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

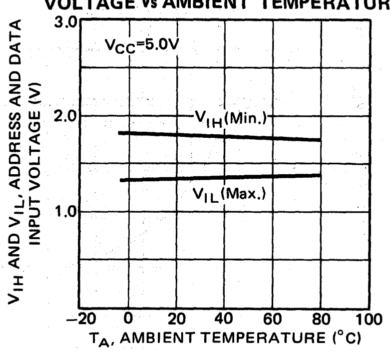


Fig. 18 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

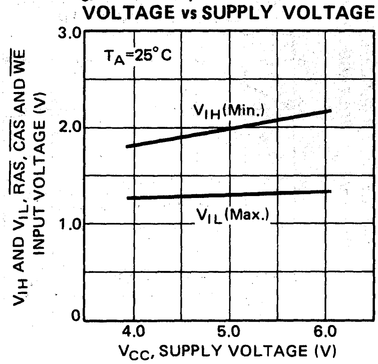


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

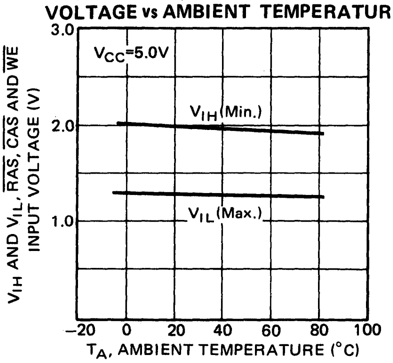


Fig. 20 – ACCESS TIME vs LOAD CAPACITANCE

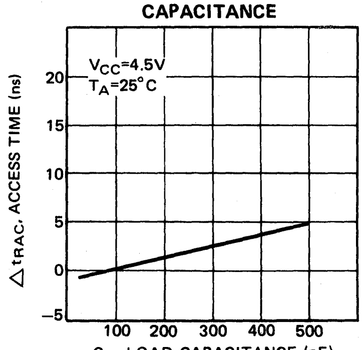


Fig. 21 — OUTPUT CURRENT vs OUTPUT VOLTAGE

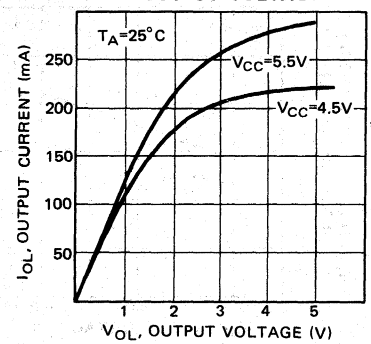


Fig. 22 — OUTPUT CURRENT vs OUTPUT VOLTAGE

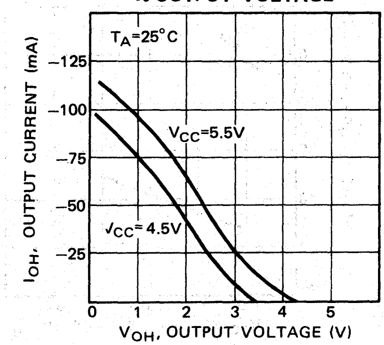


Fig. 23 — CURRENT WAVEFORM DURING POWER UP

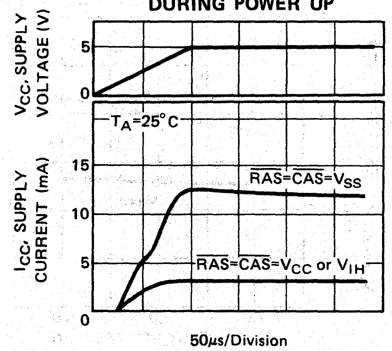
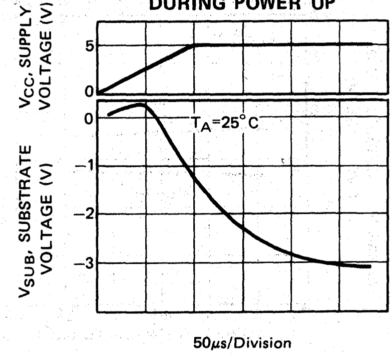
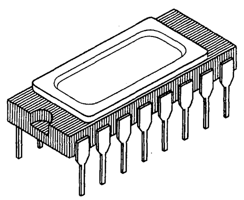


Fig. 24 — SUBSTRATE VOLTAGE DURING POWER UP



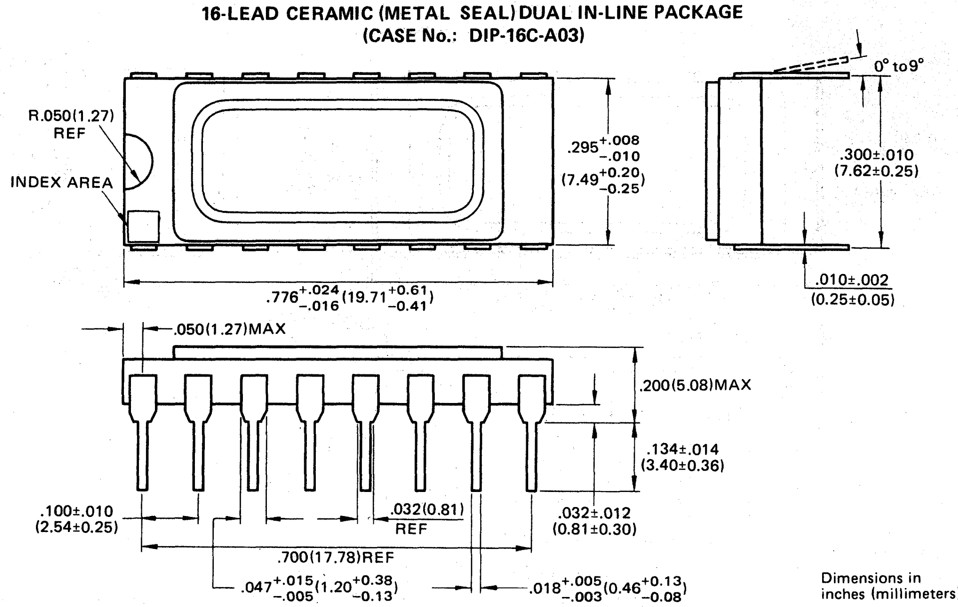
PACKAGE DIMENSIONS

(Suffix: -C)



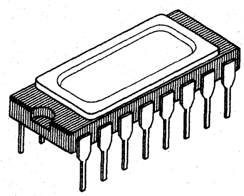
DIP-16C-A03

16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A03)

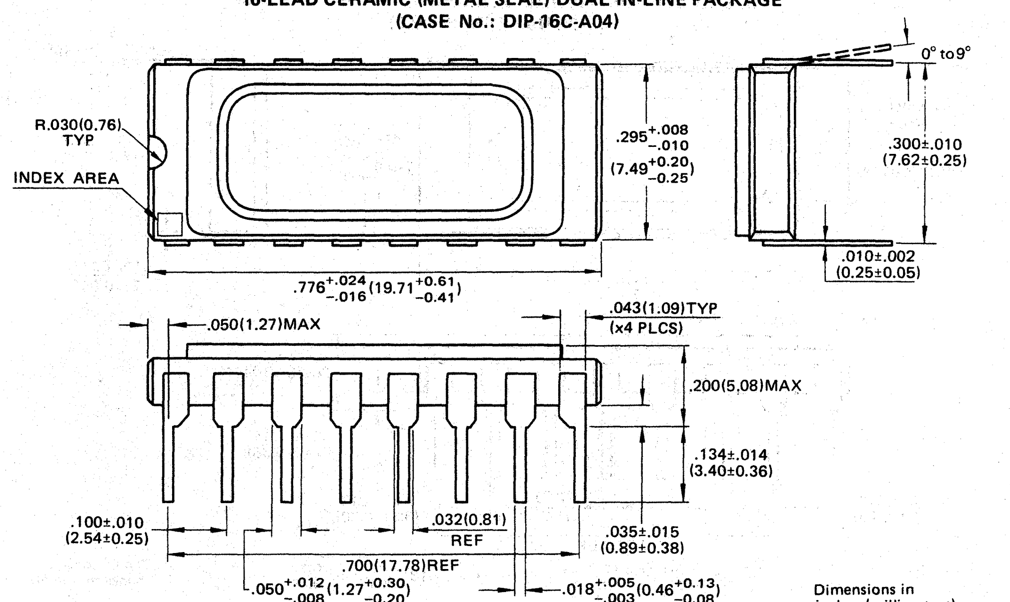


PACKAGE DIMENSIONS

(Suffix: -C)



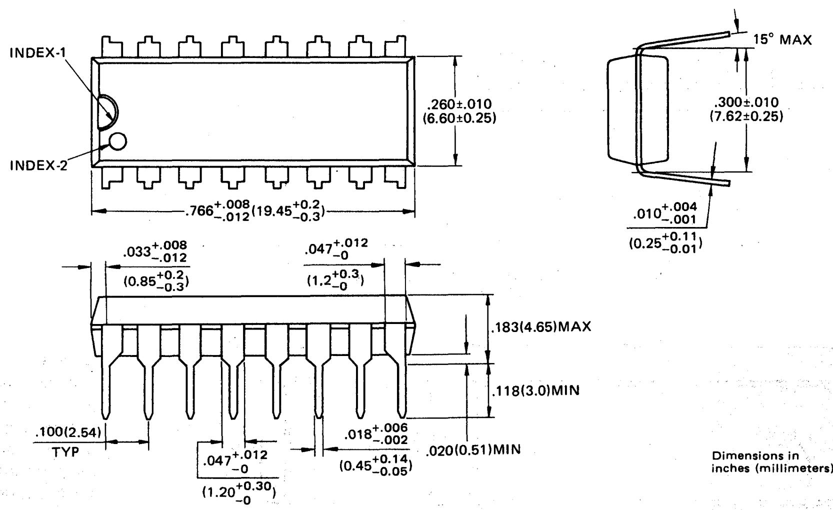
DIP-16C-A04



PACKAGE DIMENSIONS

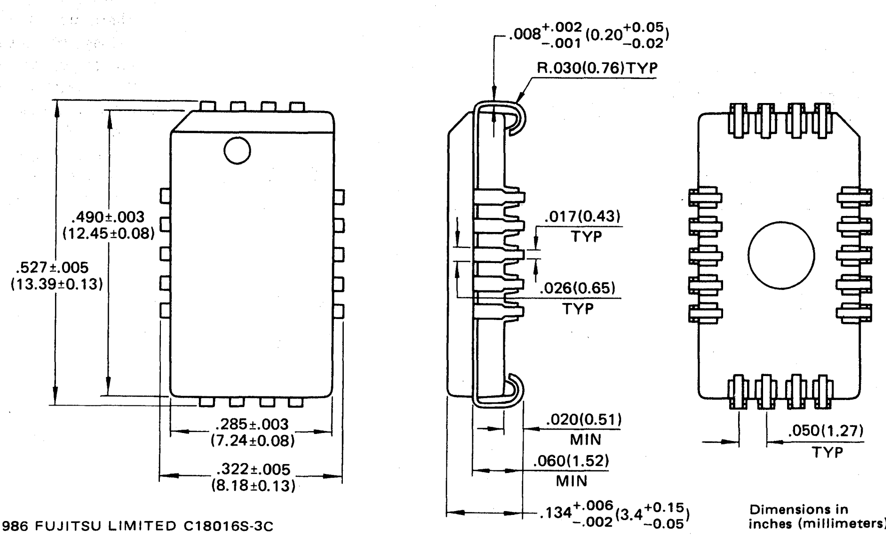
(Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



(Suffix: -PD)

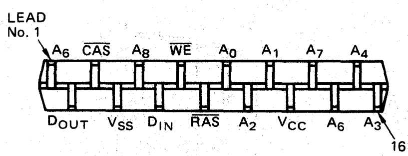
18-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-18P-M02)



PACKAGE DIMENSIONS

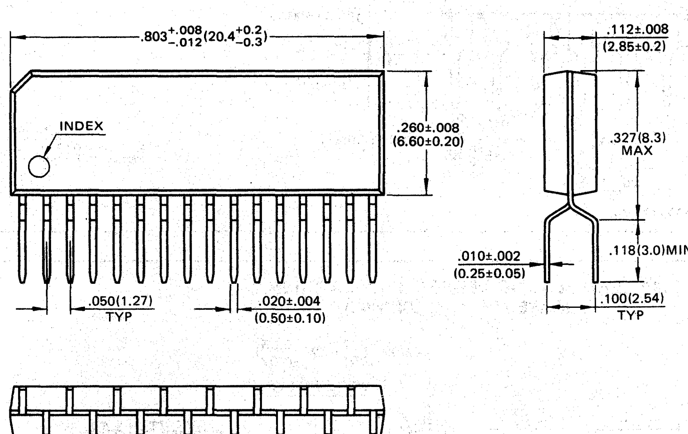
(Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

16 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-16P-M01)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

MOS 262144-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 81257-10
MB 81257-12
MB 81257-15

September 1985
Edition 4.0

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY

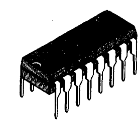
The Fujitsu MB 81257 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 81257 to be housed in a standard 16 pin DIP/ZIP and 18 pad LCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MB 81257 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$" refresh provides an on-chip refresh capability that is an upward compatible version of MB 8266A. The MB 81257 also features "Nibble Mode" which allows high speed serial access to up to 4 bits of data.

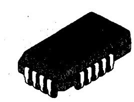
The MB 81257 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

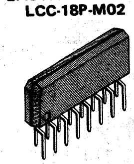
- 262,144 x 1 RAM, 16 pin DIP and ZIP/18 pad LCC
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row access time,
  100 ns max. (MB 81257-10)
  120 ns max. (MB 81257-12)
  150 ns max. (MB 81257-15)
- Cycle time,
  200 ns min. (MB 81257-10)
  220 ns min. (MB 81257-12)
  260 ns min. (MB 81257-15)
- Nibble cycle time,
  45 ns max. (MB 81257-10)
  50 ns max. (MB 81257-12)
  60 ns max. (MB 81257-15)
- Single +5V Supply, ±10% tolerance
- Low power,
  385 mW max. (MB 81257-10)
  358 mW max. (MB 81257-12)
  314 mW max. (MB 81257-15)
  25 mW max. (standby)
- 256 refresh cycles every 4ms
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, $\overline{\text{RAS}}$-only, Hidden refresh capability
- High speed Read-white-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} are eliminated
- Output unlatched at cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-pin Ceramic (Seam Weld) DIP (Suffix:-C)
  Standard 16-pin Ceramic (Cerdip) DIP (Suffix: -Z)
  Standard 16-pin Plastic DIP (Suffix: -P)
  Standard 18-pad Ceramic LCC (Suffix: -TV)
  Standard 18-pin Plastic LCC (Suffix: -PV)
  Standard 16-pin Plastic ZIP (Suffix: -PSZ)



PLASTIC PACKAGE
DIP-16-M03



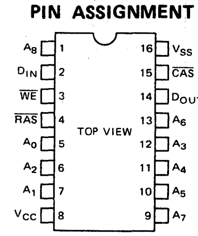
PLASTIC PACKAGE
LCC-18P-M02

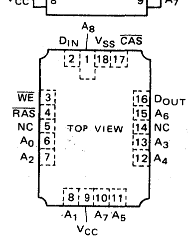


PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 19
DIP-16C-A04: See Page 20
DIP-16C-C04: See Page 21
LCC-18C-F04: See Page 24

PIN ASSIGNMENT





Pin assignment for ZIP: See page 23

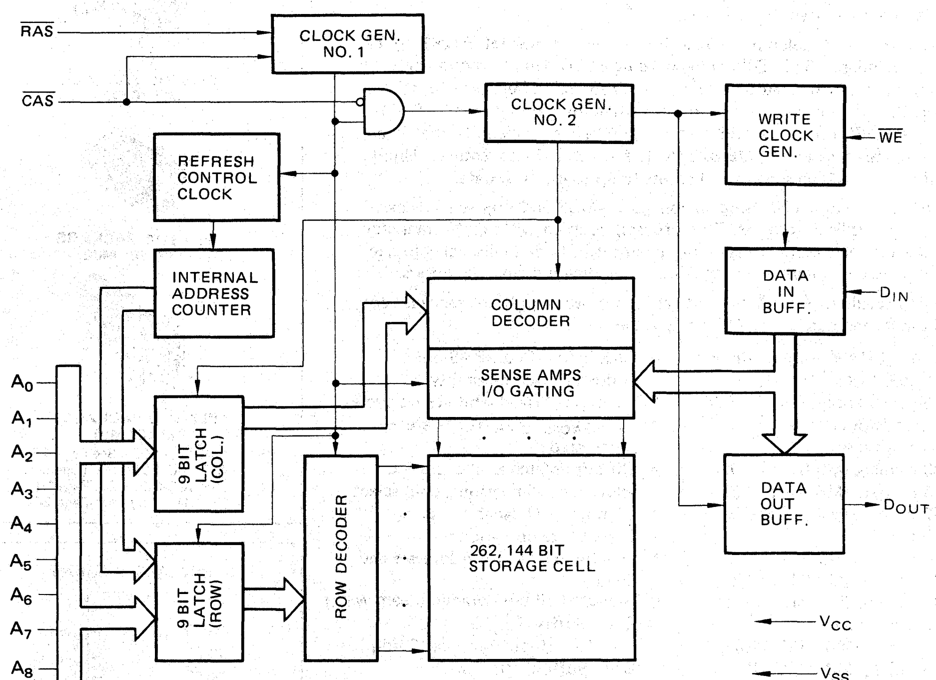
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	–1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	–1 to +7	V
Storage temperature	Ceramic	T_{STG}	–55 to +150	°C
	Plastic		–55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 81257 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		8	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	MB 81257-10	I_{CC1}			70	mA
	MB 81257-12				65	
	MB 81257-15				57	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81257-10	I_{CC3}			60	mA
	MB 81257-12				55	
	MB 81257-15				50	
NIBBLE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = Min.)	MB 81257-10	I_{CC4}			22	mA
	MB 81257-12				20	
	MB 81257-15				18	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81257-10	I_{CC5}			65	mA
	MB 81257-12				60	
	MB 81257-15				55	
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10		10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output high Voltage (I_{OH} = -5.0 mA)		V_{OH}	2.4			V

NOTE * : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB 81257-10		MB 81257-12		MB 81257-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4		4	ms
Random Read/Write Cycle time		t_{RC}	200		220		260		ns
Read-Write Cycle Time		t_{RWC}	200		220		260		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	85		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	55		60		75		ns
$\overline{CAS}$ Pulse width		t_{CAS}	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		20		ns
Write Command Set Up Time	10	t_{WCS}	0		0		0		ns
Write Command Pulse Width		t_{WP}	15		20		25		ns
Write Command Hold Time		t_{WCH}	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		30		25		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	15		20		25		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		25		30		ns

AC CHARACTERISTICS

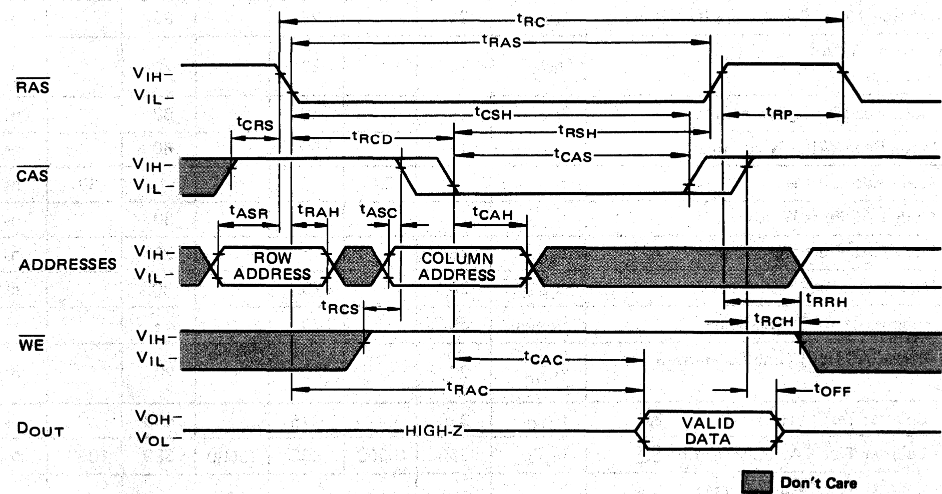
(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 81257-10		MB 81257-12		MB 81257-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		20		20		ns
Nibble Mode Read/Write Cycle Time		t_{NC}	45		50		60		ns
Nibble Mode Read-Write Cycle Time		t_{NRWC}	45		50		60		ns
Nibble Mode Access Time		t_{NCAC}		20		25		30	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	20		25		30		ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	15		15		20		ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	20		25		30		ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	35		40		45		
Nibble Mode $\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$		t_{RNH}	20		20		20		ns
Refresh Counter Test Cycle Time	11	t_{RTC}	330		375		430		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	11	t_{TRAS}	230	10000	265	10000	320	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	11	t_{CPT}	50		60		70		ns

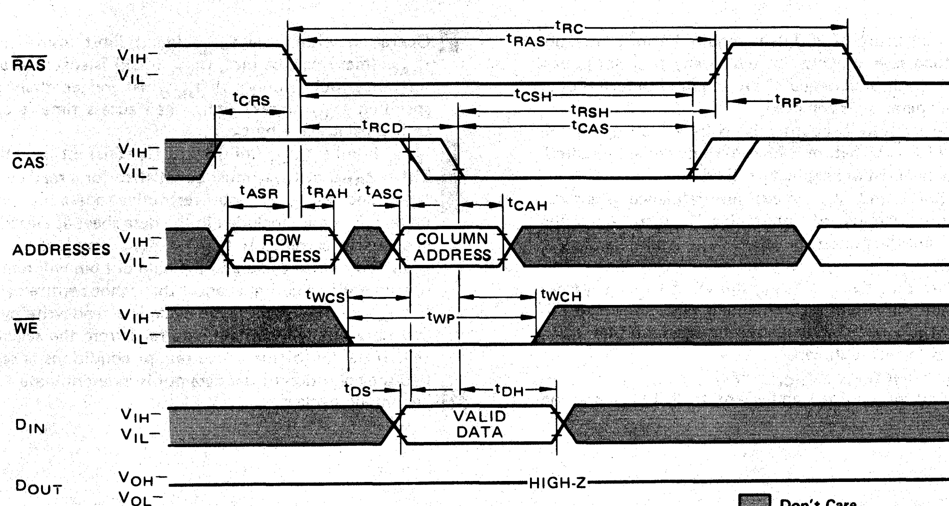
Notes:

1. An initial pause of 200 μs is required after power up. And then several cycles (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume $t_T = 5$ ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
11. Test mode cycle only.

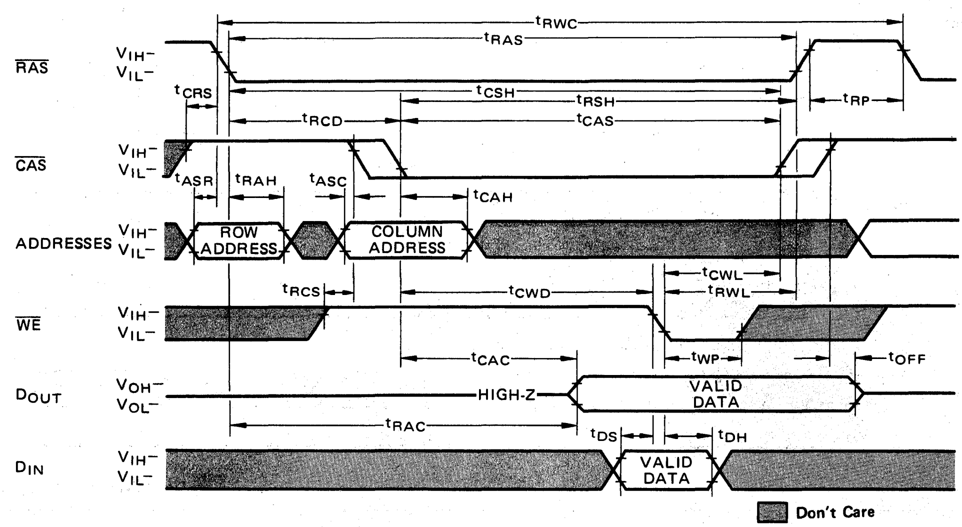
Read Cycle



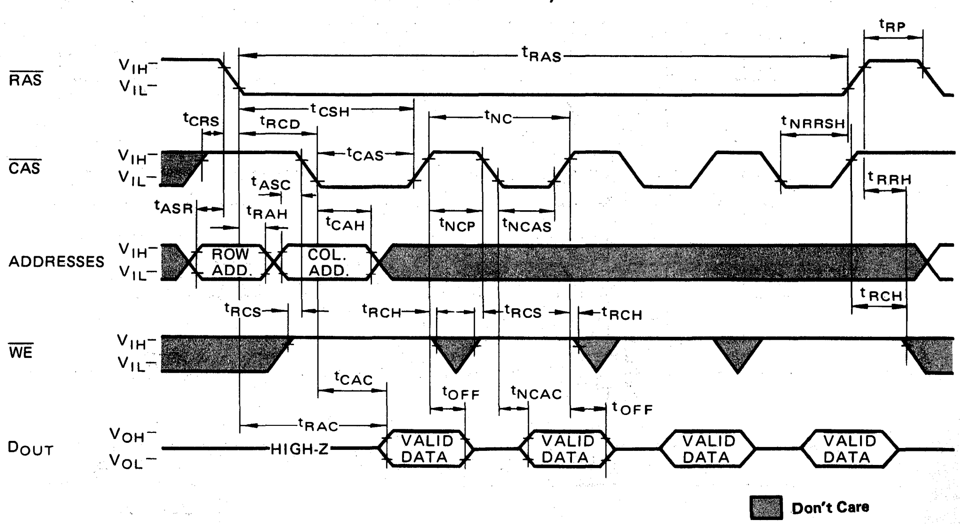
Write Cycle (Early Write)



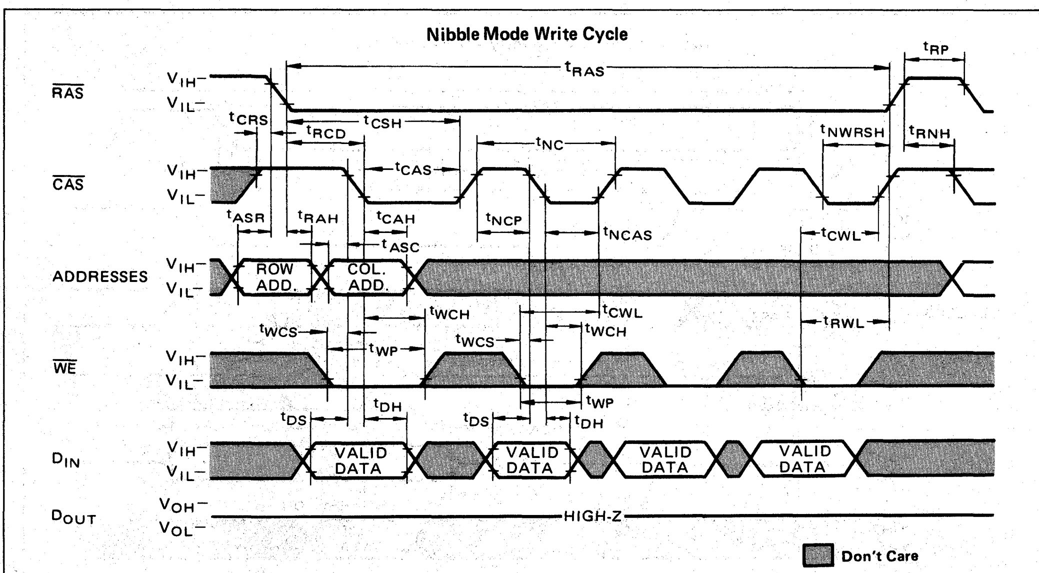
Read–Write/Read–Modify–Write Cycle

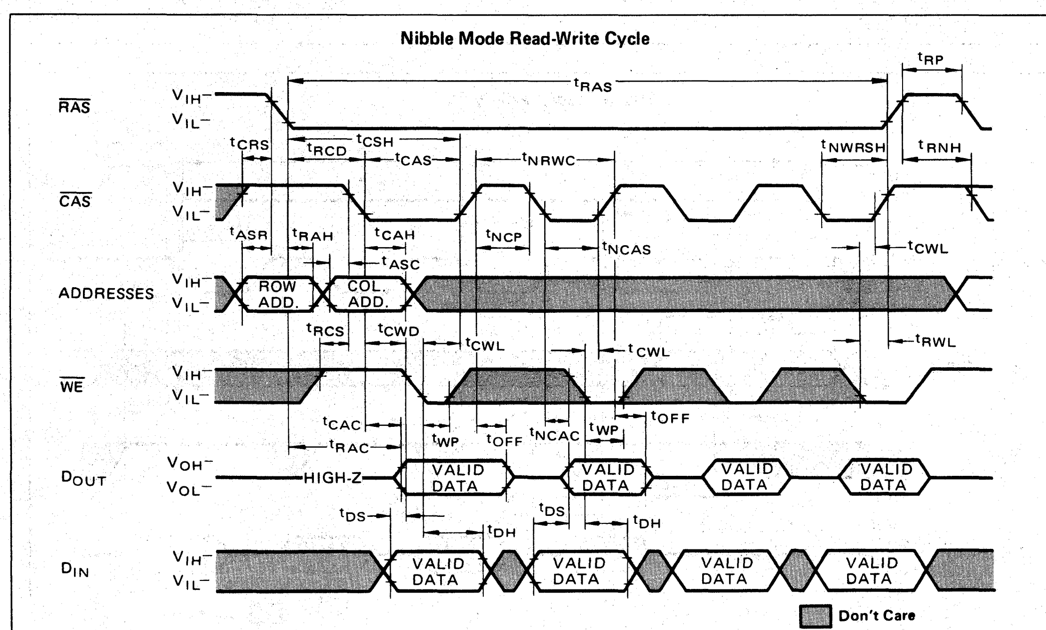


Nibble Mode Read Cycle



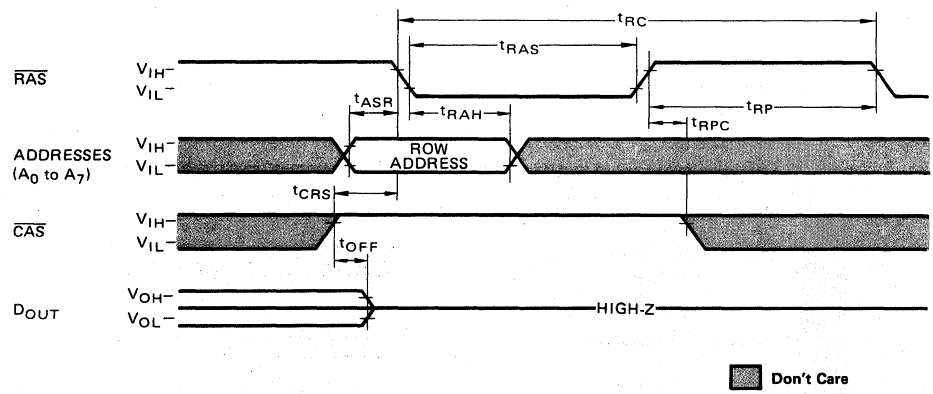
1


Nibble Mode Write Cycle
RAS
CAS
ADDRESSES
WE
DIN
DOUT
VIH
VIL
VOH
VOL
tRAS
tRP
tCRS
tCSH
tRCD
tNWRSH
tRNH
tNC
tCAS
tASR
tRAH
tCAH
tNCP
tNCAS
tCWL
tASC
ROW ADD.
COL. ADD.
tWCH
tRWL
tWCS
tWP
tDH
tDS
VALID DATA
HIGH-Z
Don't Care


Nibble Mode Read-Write Cycle
RAS
CAS
ADDRESSES
WE
DOUT
DIN
VIH
VIL
VOH
VOL
tRAS
tRP
tCRS
tCSH
tRCD
tCAS
tNRWC
tNWRSH
tRNH
tASR
tRAH
tCAH
tNCP
tNCAS
tCWL
tASC
ROW ADD.
COL. ADD.
tRCS
tCWD
tRWL
tCAC
tRAC
tWP
tOFF
tNCAC
HIGH-Z
VALID DATA
tDS
tDH
Don't Care

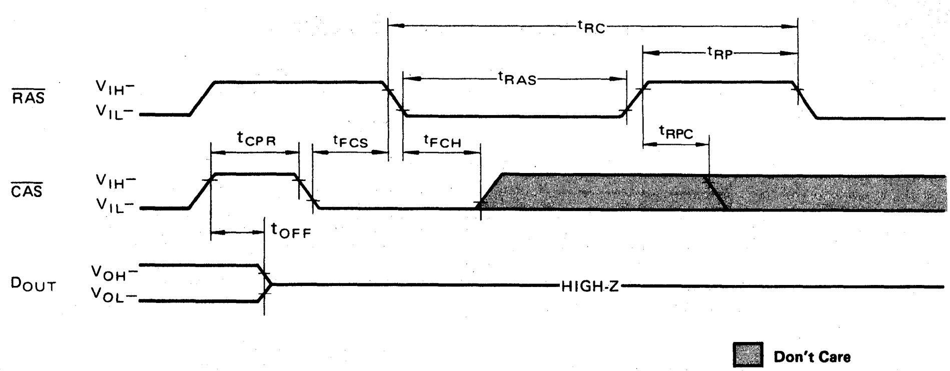
$\overline{RAS}$-only Refresh Cycle

NOTE: $\overline{WE}$, D_{IN} = Don't care, A_8 = V_{IH} or V_{IL}

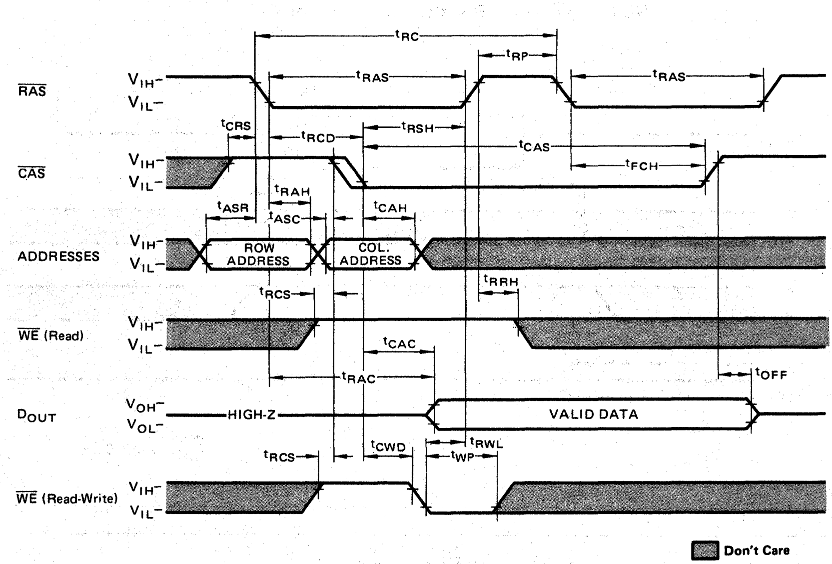


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

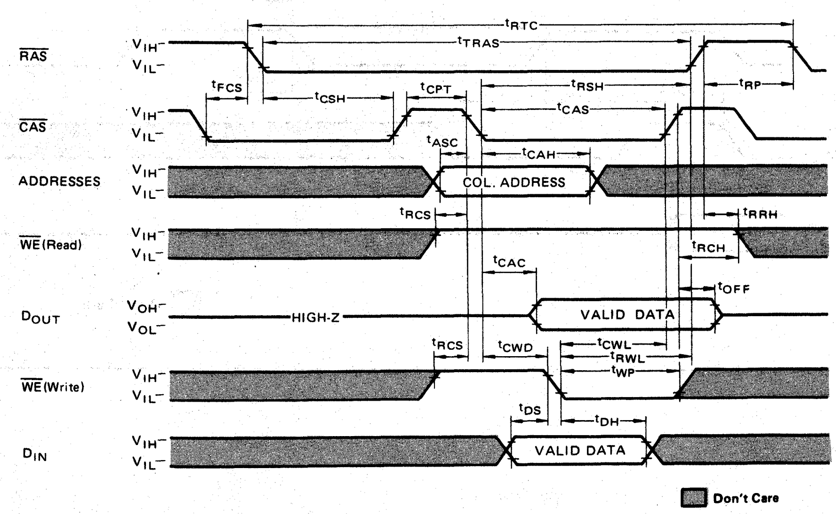
NOTE: Address, $\overline{WE}$, D_{IN} = Don't care



Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement

The MB 81257 has improved circuitry that eases timing requirements for high speed access operations. The MB 81257 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81257 has the minimal hold times of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 81257 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirement that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81257. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode, low selects write mode. The data input is disabled when read mode is selected.

Data Input:

Data is written into the MB 81257 during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be delayed after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.) Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle, the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle

The MB 81257 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings, described in the previous section. The output buffer is controlled by the sate of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MB 81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB 81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle (t_{RWC} = t_{RC}) is possible with the MB 81257.

Nibble Mode:

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1).

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of the D_{OUT} pin is determined by the first normal access cycle.

The data output is controlled only by the $\overline{WE}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} >$ t_{WCS} (min) is met, the data output will remain high impedance state throughout the succeeding nibble cycle regardless of the $\overline{WE}$ state. Whereas, when $t_{CWD} >$ t_{CWD} (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{WE}$ state. The write operation is done during the period in which the $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit).

See Fig. 2.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 ms.

The MB 81257 offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh;

The $\overline{RAS}$ only refresh aboids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses (A_0 to A_7) with RAS will cause all bits in each row to be refreshed. Further RAS-only refresh results in a substantial reduction in power dissipation. During RAS-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

CAS-before-RAS Refresh;
CAS-before-RAS refreshing available on the MB 81257 offers an alternate refresh method. If CAS is held low for the specified period (t_{FCS}) before RAS goes to low, on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next CAS-before-RAS refresh operation.

Hidden Refresh;
A hidden refresh cycle may takes place while maintaining latest valid data at the output by extending the CAS active time. For the MB 81257, a hidden refresh cycle is CAS-before-RAS refresh.

The internal refresh address counters provide the refresh addresses, as in a normal CAS-before-RAS refresh cycle.

CAS-before-RAS Refresh Counter Test Cycle:
A special timing sequence using CAS-before-RAS counter test cycle provides a convenient method of verifying the functionality of CAS-before-RAS refresh activated circuitry. After the CAS-before-RAS refresh operation, if CAS goes to high and goes to low again while RAS is held low, the read and write operation are enabled. This is shown in the CAS-before-RAS counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

*A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.
*A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of CAS.

Suggested CAS-before-RAS Counter Test Procedure
The timing, as shown in the CAS-before-RAS Counter Test Cycle, is used for the following operations:

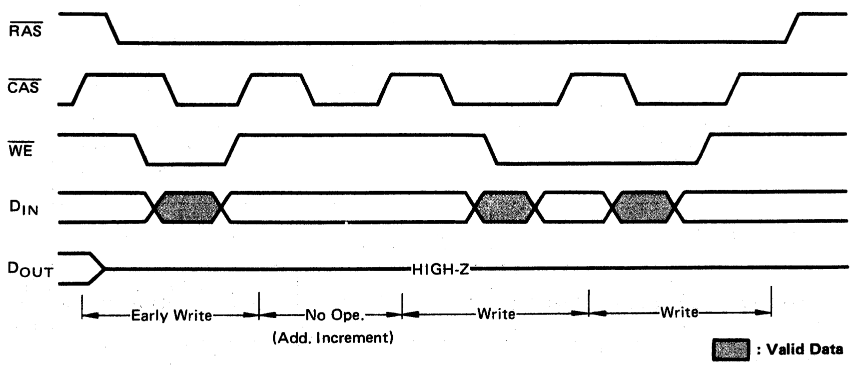
1) Initialize the internal refresh address counter by using eight CAS-before-RAS refresh cycles.
2) Throughout the test, use the same column address, and keep RA8 high.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

Table 1 – NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

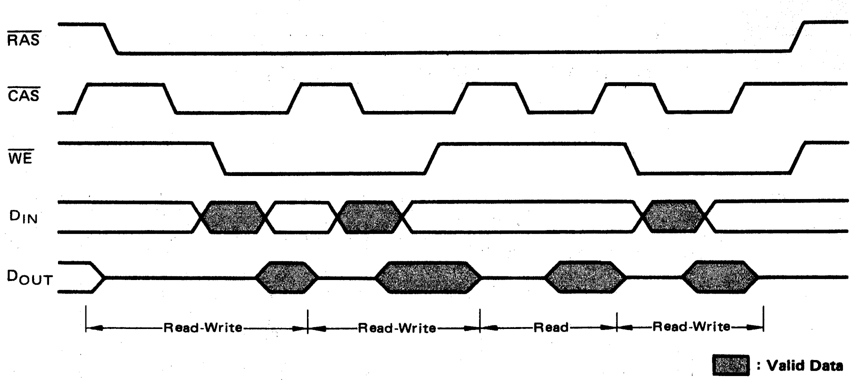
SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
RAS/CAS (normal mode)	1	0	10101010	0	10101010	input addresses
toggle CAS (nibble mode)	2	1	10101010	0	10101010	generated internally
toggle CAS (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle CAS (nibble mode)	4	1	10101010	1	10101010	generated internally
toggle CAS (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Fig. 2 — Nibble Mode

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)

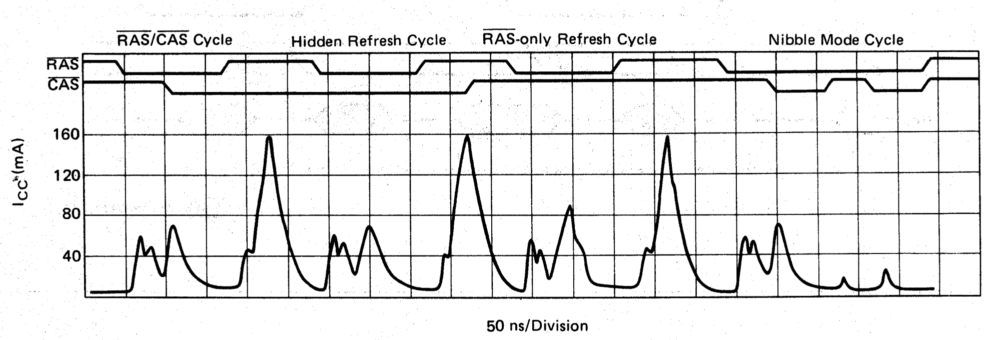


1

Table-2 FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geqq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write ($t_{WCS} \leqq t_{WCS}$ (min) or $t_{CWD} \geqq t_{CWD}$ (min))
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.

Fig. 3 — CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 4 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

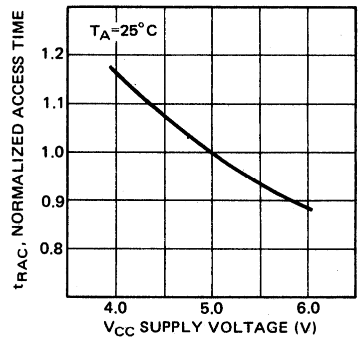


Fig. 5 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

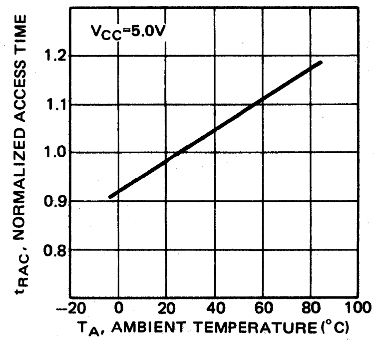


Fig. 6 – OPERATING CURRENT vs CYCLE RATE

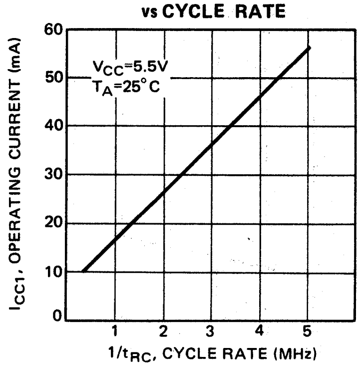


Fig. 7 – OPERATING CURRENT vs SUPPLY VOLTAGE

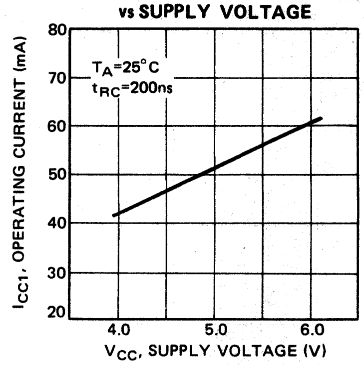


Fig. 8 – OPERATING CURRENT vs AMBIENT TEMPERATURE

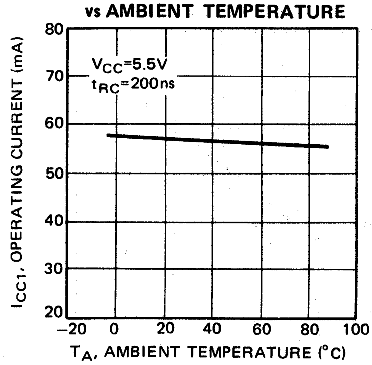


Fig. 9 – STANDBY CURRENT vs SUPPLY VOLTAGE

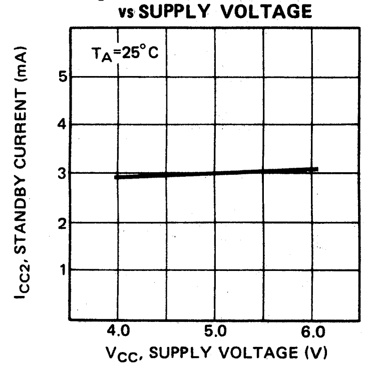


Fig. 10 – STANDBY CURRENT vs AMBIENT TEMPERATURE

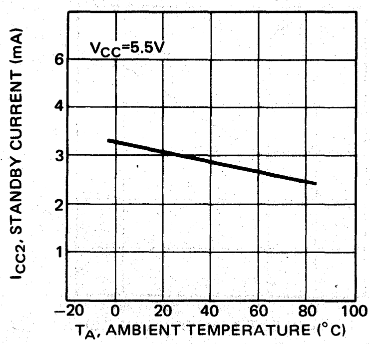


Fig. 11 – REFRESH CURRENT 1 vs CYCLE RATE

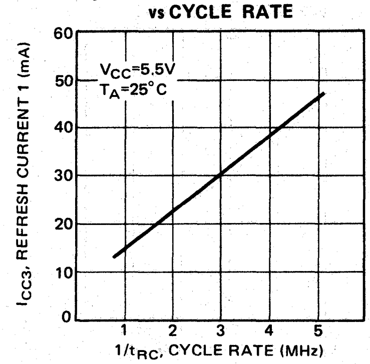


Fig. 12 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

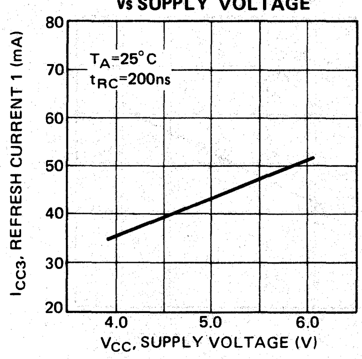


Fig. 13 – NIBBLE MODE CURRENT vs CYCLE RATE

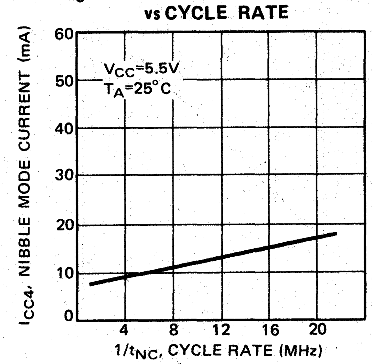


Fig. 14 – NIBBLE MODE CURRENT vs SUPPLY VOLTAGE

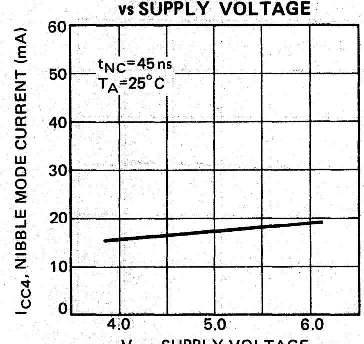


Fig. 15 – REFRESH CURRENT 2 vs CYCLE RATE

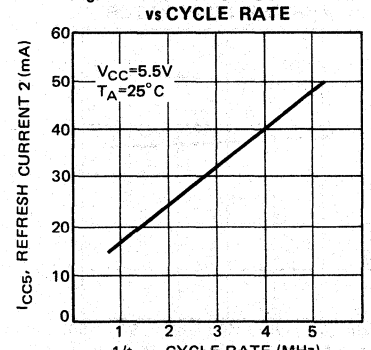


Fig. 16 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

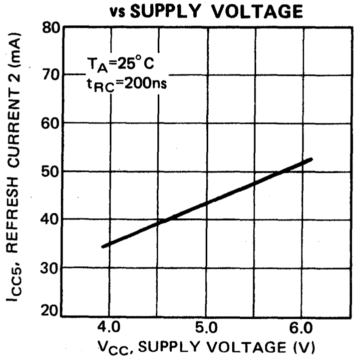


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

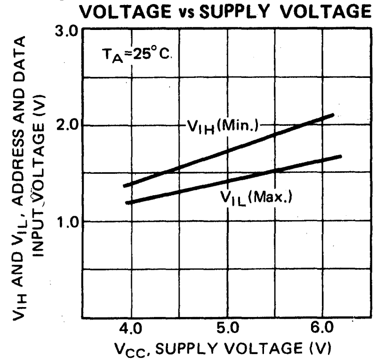


Fig. 18 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

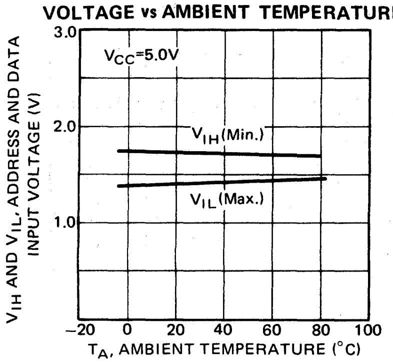


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

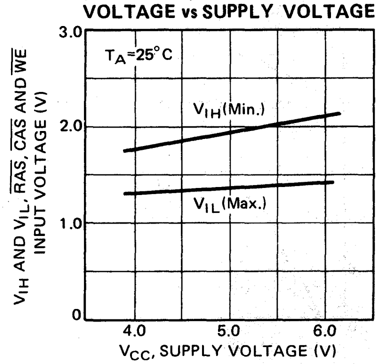


Fig. 20 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

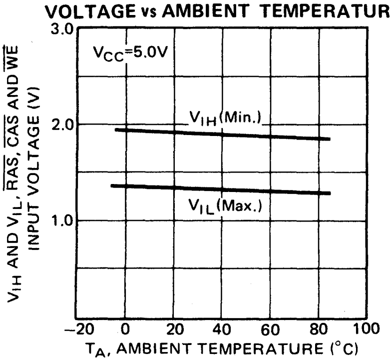


Fig. 21 – ACCESS TIME vs LOAD CAPACITANCE

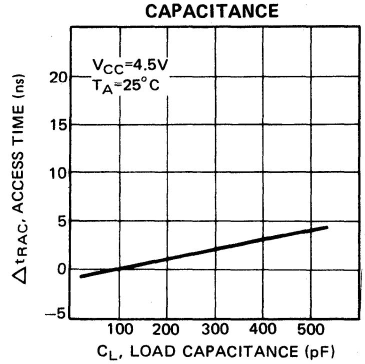


Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

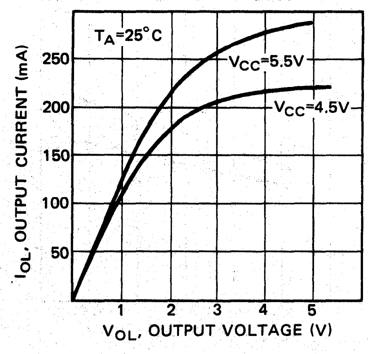


Fig. 23 – OUTPUT CURRENT vs OUTPUT VOLTAGE

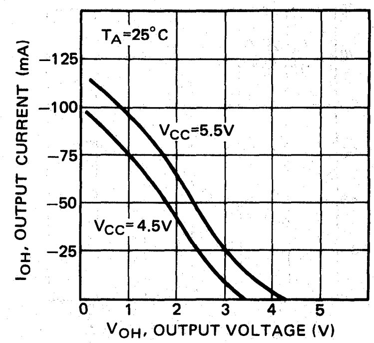


Fig. 24 – CURRENT WAVEFORM DURING POWER UP

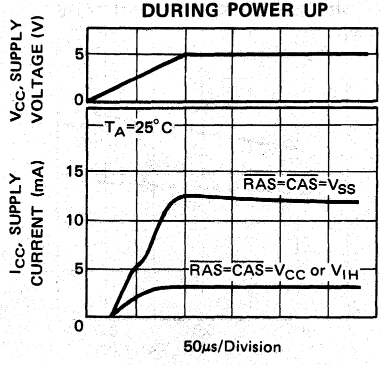
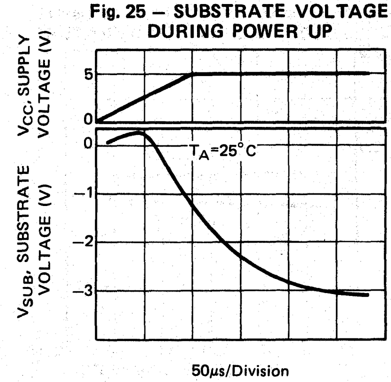
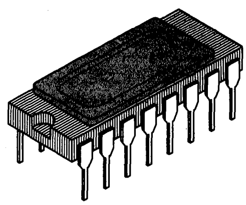


Fig. 25 – SUBSTRATE VOLTAGE DURING POWER UP



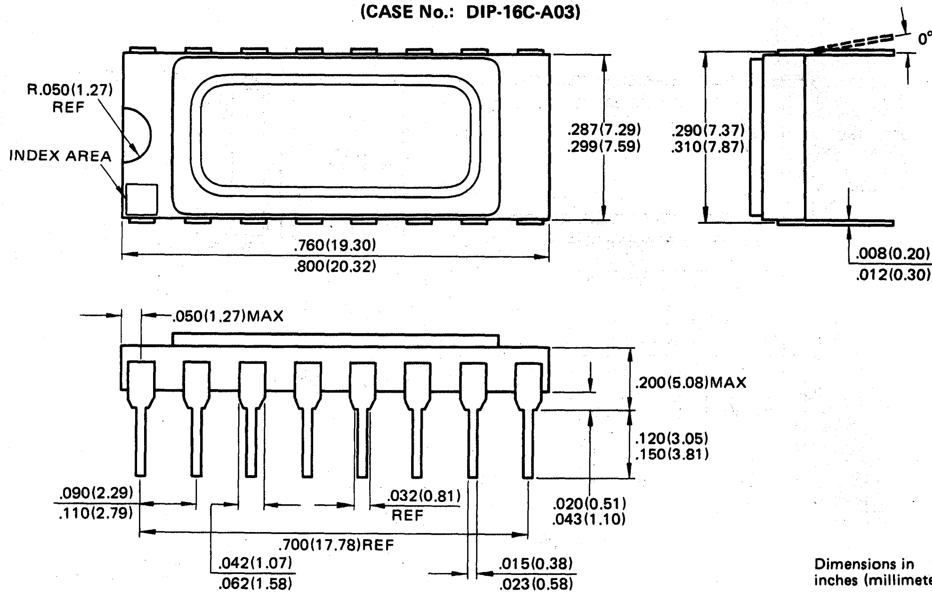
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A03

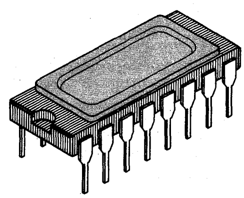
16-DEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A03)



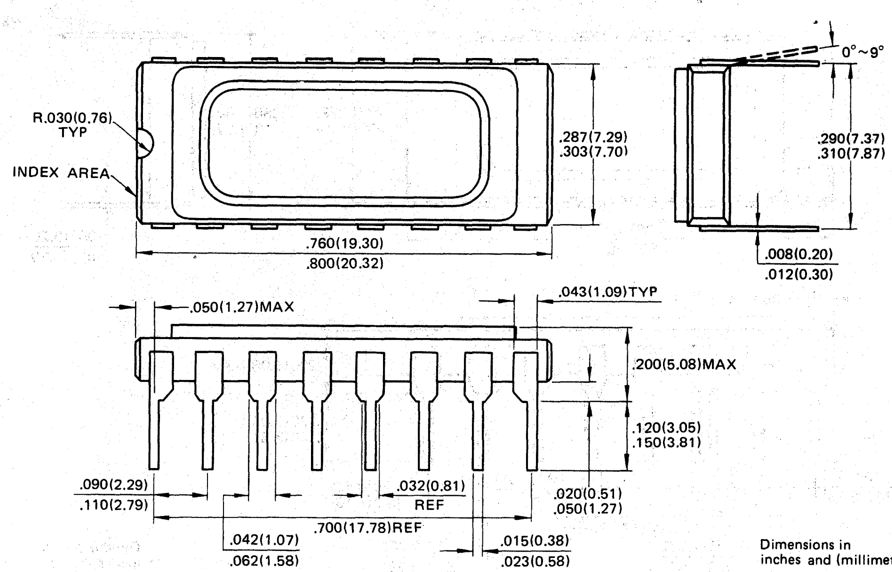
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)

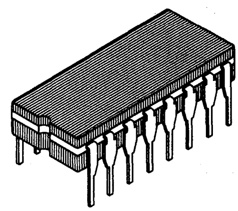


DIP-16C-A04



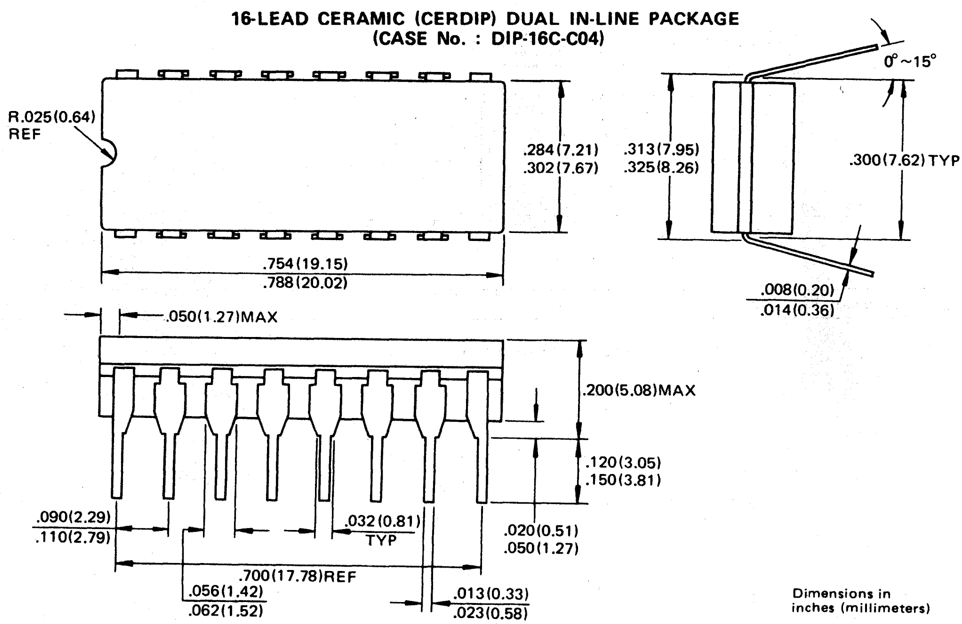
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -Z)



DIP-16C-C04

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C04)

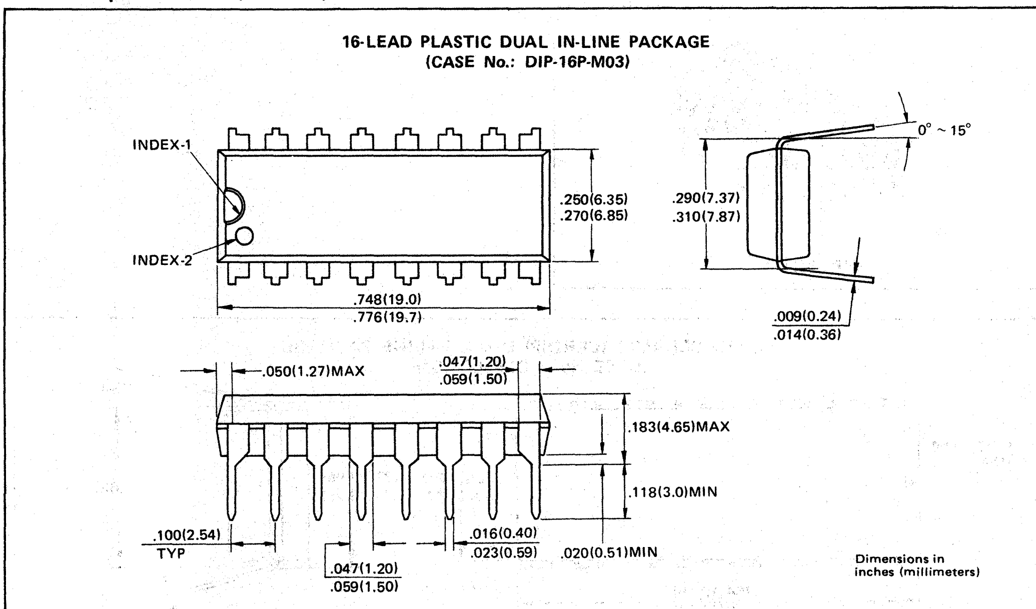


Dimensions in inches (millimeters)

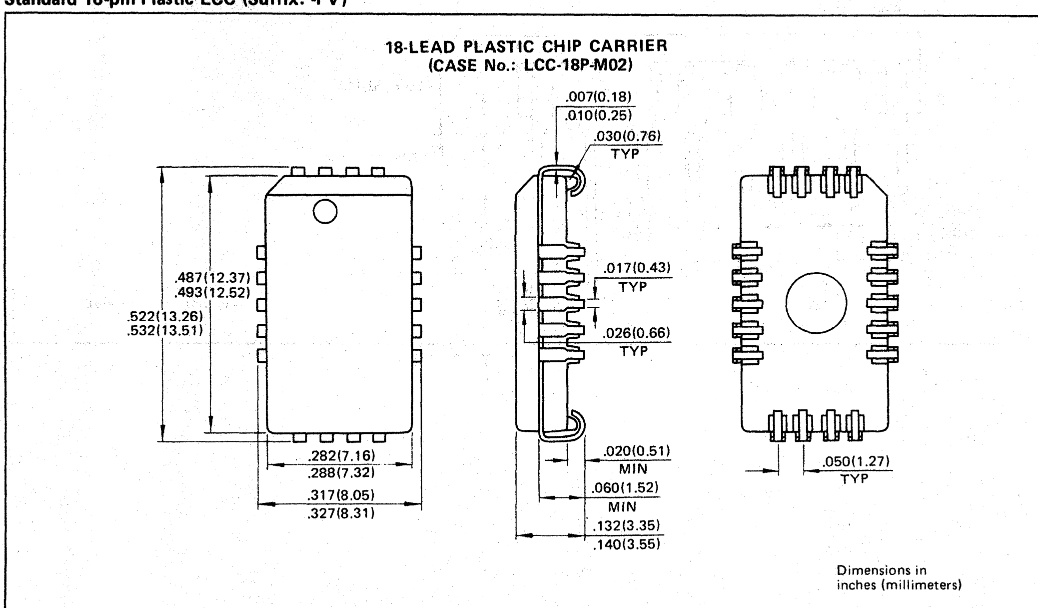
1

PACKAGE DIMENSIONS

Standard 16-pin Plastic DIP (Suffix: -P)



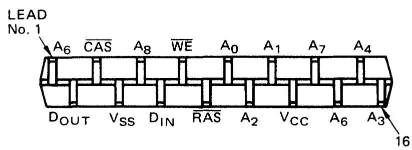
Standard 18-pin Plastic LCC (Suffix: -PV)



PACKAGE DIMENSIONS

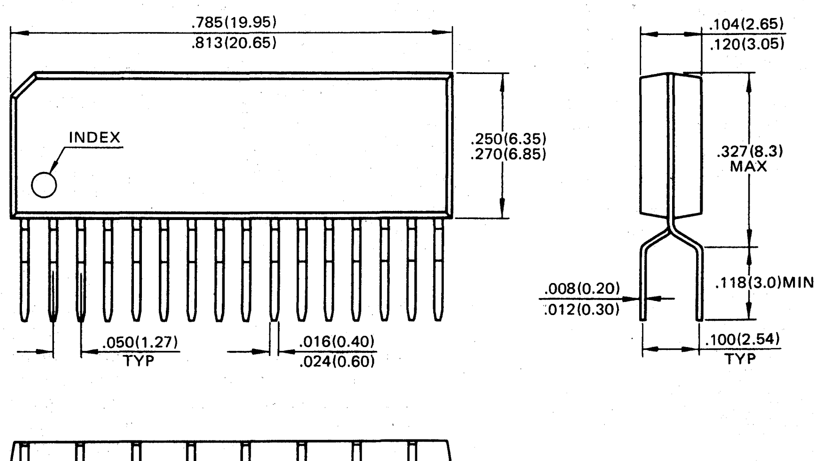
Standard 16-Pin Plastic ZIP(Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

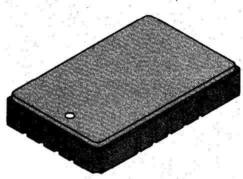
16 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-16P-M01)



Dimensions in
inches (millimetres)

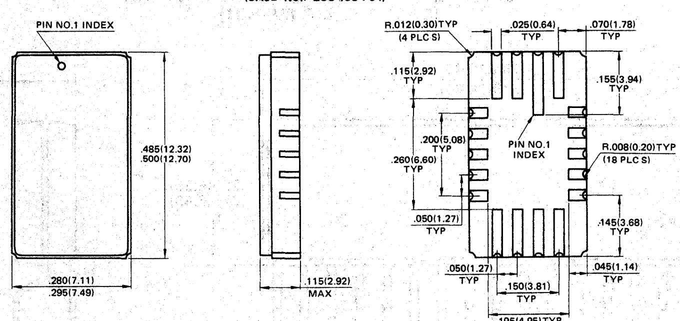
PACKAGE DIMENSIONS

Standard 18-pin Ceramic LCC (Suffix: -TV)



LCC-18C-F04

18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F04)



*Shape of Pin 1 index: Subject to change without notice

Dimension in inches (millimeters).

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

MOS 262144-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 81257-80

March 1987
Edition 1.0

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY

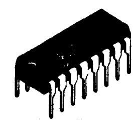
The Fujitsu MB 81257 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 81257 to be housed in a standard 16 pin DIP/ZIP and 18 pad LCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MB 81257 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability that is an upward compatible version of MB 8266A. The MB 81257 also features "Nibble Mode" which allows high speed serial access to up to 4 bits of data.

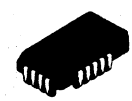
The MB 81257 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

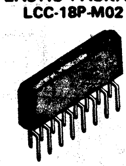
- 262,144 x 1 RAM, 16 pin DIP and ZIP/18 pad LCC
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row access time (t_{RAC}), 80ns max. (MB 81257-80)
- Randam cycle time (t_{RC}), 175ns min. (MB 81257-80)
- Nibble Mode cycle time (t_{NC}), 45ns min. (MB 81257-80)
- Single +5V supply, ±10% tolerance
- Lower power, 385mW max. (MB 81257-80) 25mW max. (standby)
- 256 refresh cycles every 4ms
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- High speed Read-white-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD}, are eliminated
- Output unlatched at cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-pin Plastic DIP (Suffix: -P)
- Standard 18-pin Plastic LCC (Suffix: -PD)
- Standard 16-pin Plastic ZIP (Suffix: -PSZ)
- Standard 16-pin Ceramic DIP (Suffix: -C)



PLASTIC PACKAGE
DIP-16P-M03



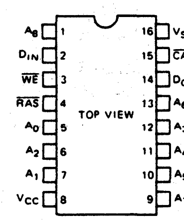
PLASTIC PACKAGE
LCC-18P-M02

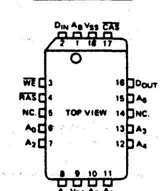


PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 19
DIP-16C-A04: See Page 20

PIN ASSIGNMENT





Pin assignment for ZIP: See page 23

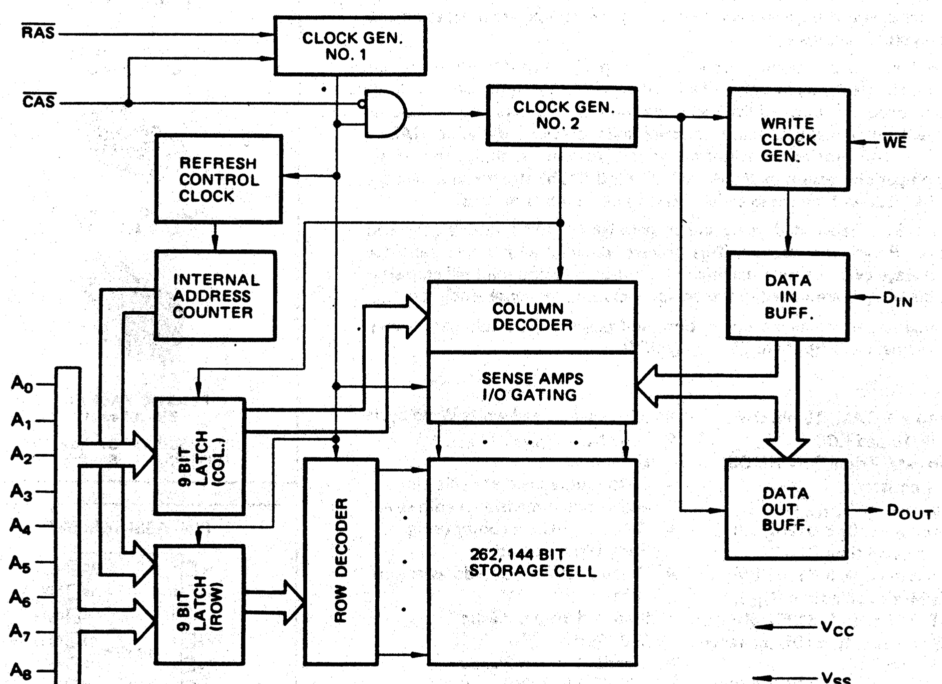
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 81257 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		10	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.)	MB 81257-80	I_{CC1}			70	mA
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81257-80	I_{CC3}			60	mA
NIBBLE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = Min.)	MB 81257-80	I_{CC4}			22	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81257-80	I_{CC5}			65	mA
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10		10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = -5.0mA)		V_{OH}	2.4			V

NOTE* : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
Time between Refresh		t_{REF}		4	ms
Random Read/Write Cycle Time		t_{RC}	175		ns
Read-Write Cycle Time		t_{RWC}	180		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		80	ns
Access Time from $\overline{CAS}$	4 6	t_{CAC}		45	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	ns
Transition Time		t_T	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	85	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	50		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	50	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	85		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	35	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		ns
Row Address Set Up Time		t_{ASR}	0		ns
Row Address Hold Time		t_{RAH}	10		ns
Column Address Set Up Time		t_{ASC}	0		ns
Column Address Hold Time		t_{CAH}	15		ns
Read Command Set Up Time		t_{RCS}	0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		ns
Write Command Set Up Time	10	t_{WCS}	0		ns
Write Command Pulse Width		t_{WP}	15		ns
Write Command Hold Time		t_{WCH}	15		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		ns
Data In Set Up Time		t_{DS}	0		ns
Data In Hold Time		t_{DH}	15		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	15		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		ns
Nibble Mode Read/Write Cycle Time		t_{NC}	45		ns
Nibble Mode Read-Write Cycle Time		t_{NRWC}	45		ns
Nibble Mode Access Time		t_{NCAC}		18	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	20		ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	15		ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	20		ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	35		ns
Nibble Mode $\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$		t_{RNH}	20		ns
Refresh Counter Test Cycle Time	11	t_{RTC}	330		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	11	t_{TRAS}	230	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	11	t_{CPT}	50		ns

Notes:

1 An initial pause of 200 μs is required after power up. And then several cycles (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.

2 AC characteristics assume t_T = 5 ns.

3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).

4 Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

5 Assumes that $t_{RCD} \geqq t_{RCD}$ (max).

6 Measured with a load equivalent to 2 TTL loads and 100 pF.

7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

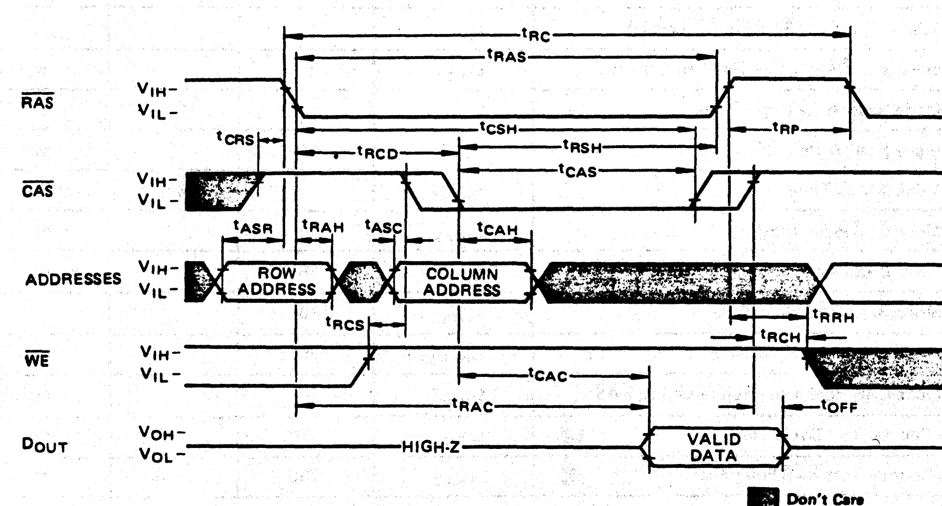
8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)

9 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

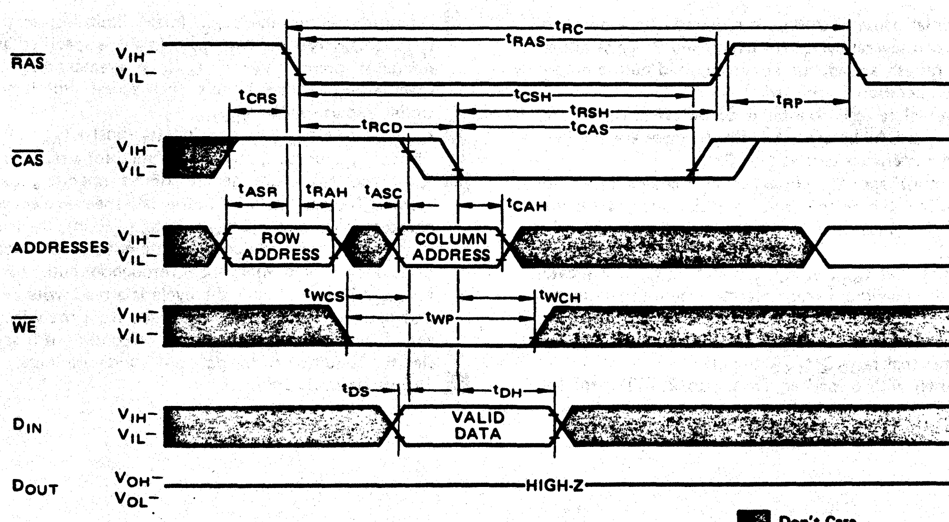
10 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

11 Test mode cycle only.

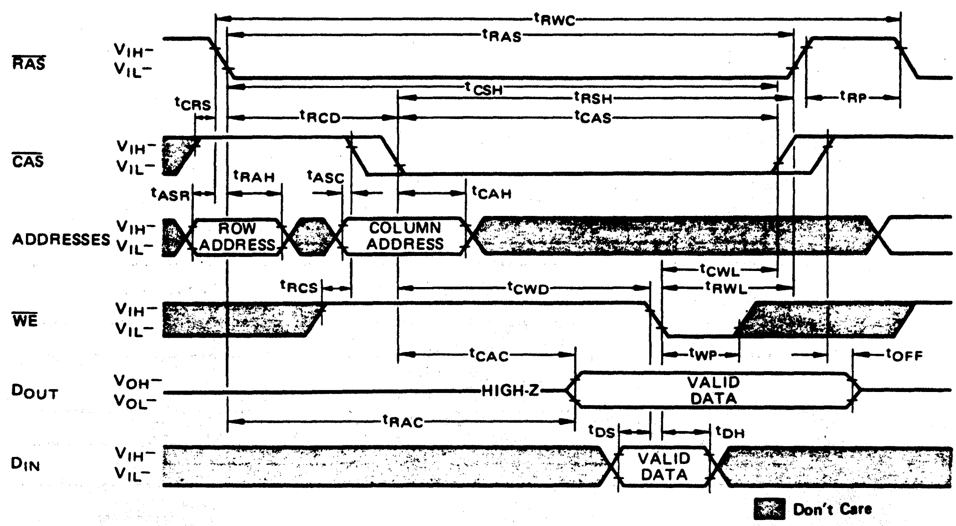
Read Cycle



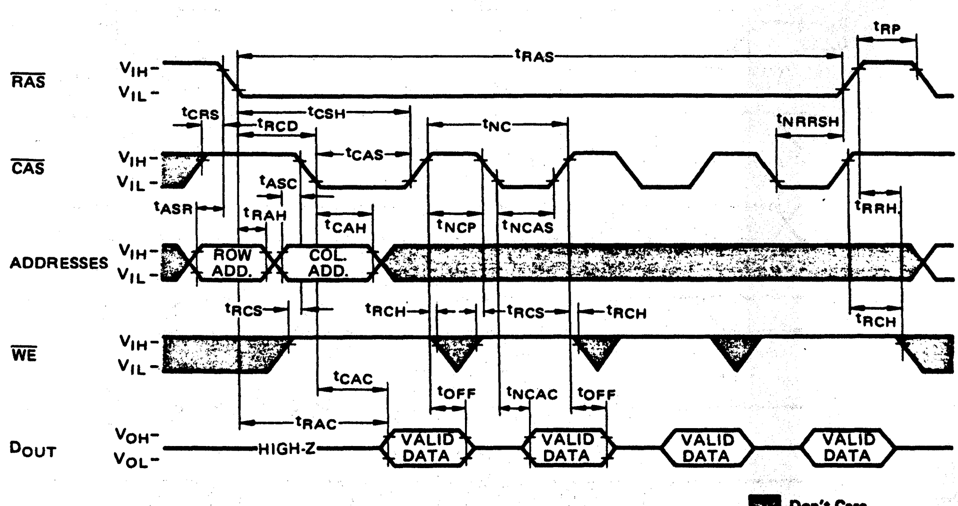
Write Cycle (Early Write)



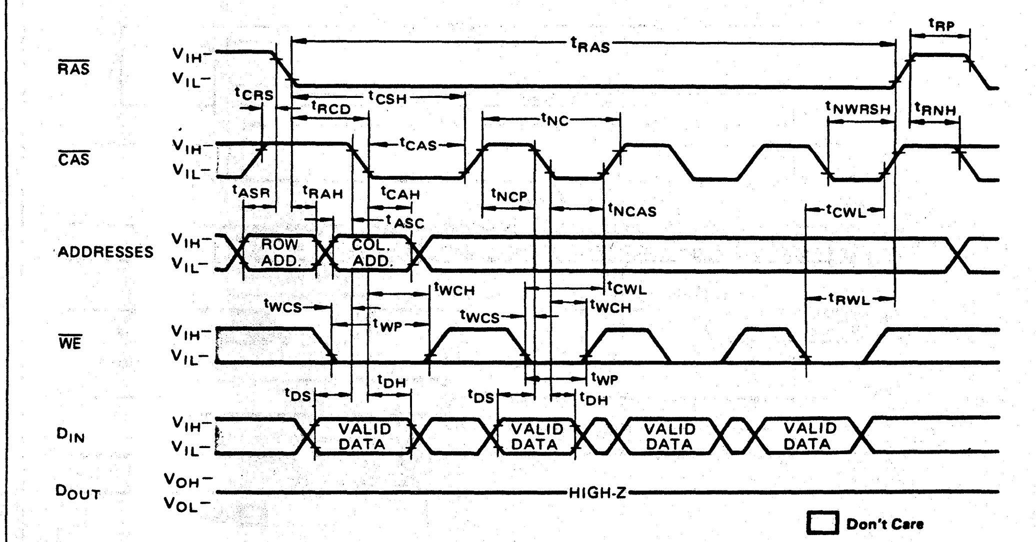
Read–Write/Read–Modify–Write Cycle



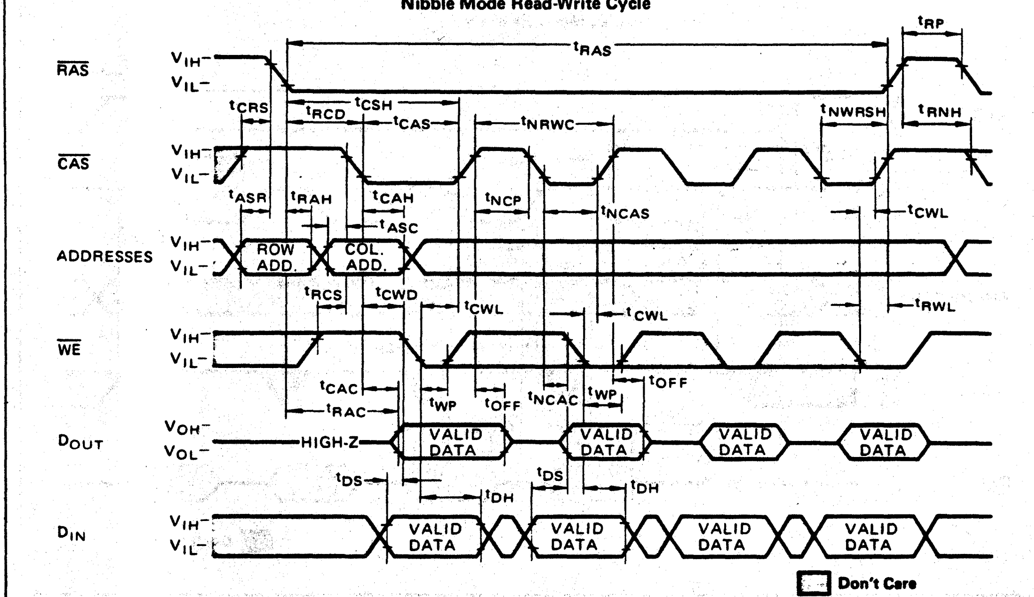
Nibble Mode Read Cycle



Nibble Mode Write Cycle (Early Write)

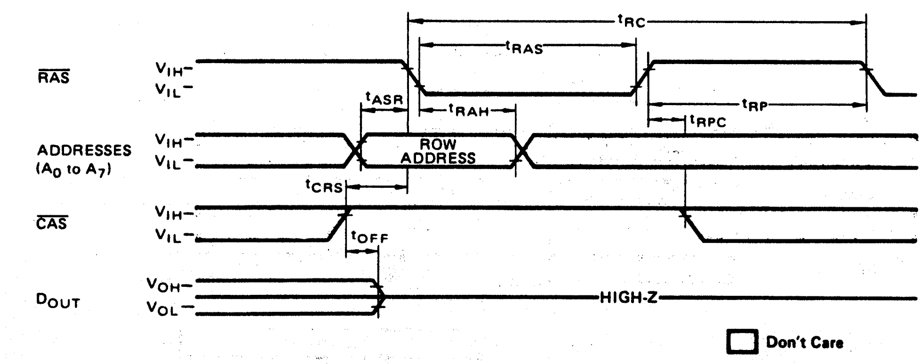


Nibble Mode Read-Write Cycle



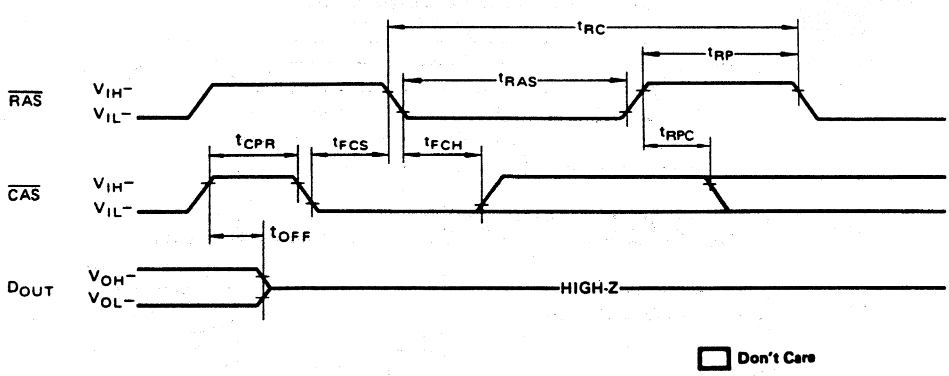
$\overline{RAS}$-only Refresh cycle

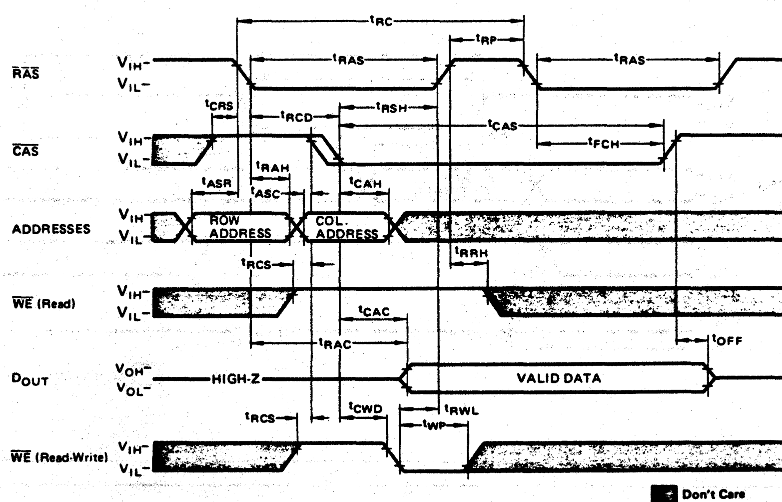
NOTE: $\overline{WE}$, D_{IN} = Don't care, A_8 = V_{IH} or V_{IL}

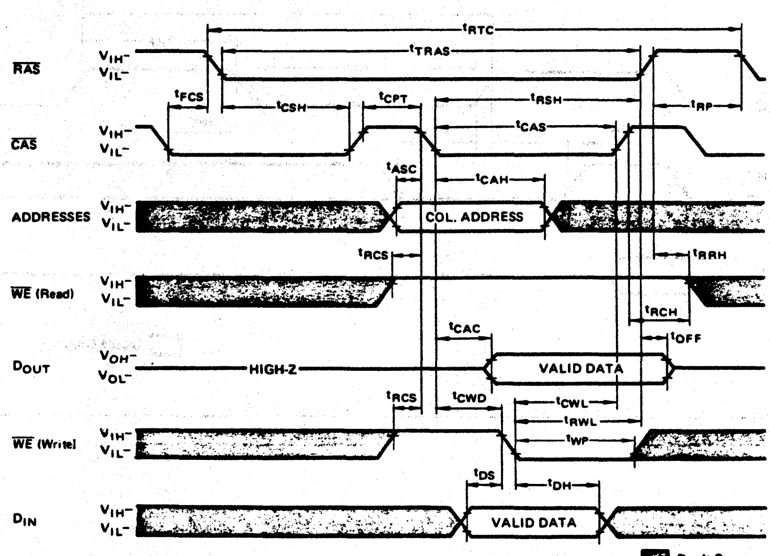


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE: Address, $\overline{WE}$, D_{IN} = Don't care




Hidden Refresh Cycle
RAS
CAS
ADDRESSES
WE (Read)
DOUT
WE (Read-Write)
VIH
VIL
VOH
VOL
tRC
tRP
tRAS
tCRS
tRCD
tRSH
tCAS
tFCH
tRAH
tASR
tASC
tCAH
ROW ADDRESS
COL. ADDRESS
tRCS
tRRH
tCAC
tRAC
tOFF
HIGH-Z
VALID DATA
tCWD
tRWL
tWP
Don't Care


CAS-before-RAS Refresh Counter Test Cycle
RAS
CAS
ADDRESSES
WE (Read)
DOUT
WE (Write)
DIN
VIH
VIL
VOH
VOL
tRTC
tTRAS
tFCS
tCSH
tCPT
tRSH
tRP
tCAS
tASC
tCAH
COL. ADDRESS
tRCS
tRRH
tRCH
tCAC
tOFF
HIGH-Z
VALID DATA
tCWD
tCWL
tRWL
tWP
tDS
tDH
Don't Care

DESCRIPTION

Simple Timing Requirement

The MB 81257 has improved circuitry that eases timing requirements for high speed access operations. The MB 81257 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81257 has the minimal hold times of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 81257 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirement that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81257. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode; low selects write mode. The data input is disabled when read mode is selected.

Data Input:

Data is written into the MB 81257 during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be delayed after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.) Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle, the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle

The MB 81257 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings, described in the previous section. The output buffer is controlled by the sate of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MB 81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB 81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle is possible with the MB 81257.

Nibble Mode:

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1).

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of the D_{OUT} pin is determined by the first normal access cycle.

The data output is controlled only by the $\overline{WE}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} >$ t_{WCS} (min) is met, the data output will remain high impedance state throughout the succeeding nibble cycle regardless of the $\overline{WE}$ state. Whereas, when $t_{CWD} >$ t_{CWD} (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{WE}$ state. The write operation is done during the period in which the $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit).

See Fig. 2.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 ms.

The MB 81257 offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh;

The $\overline{RAS}$ only refresh aboids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses (A_0 to A_7) with $\overline{\text{RAS}}$ will cause all bits in each row to be refreshed. Further $\overline{\text{RAS}}$-only refresh results in a substantial reduction in power dissipation. During $\overline{\text{RAS}}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh;

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing available on the MB 81257 offers an alternate refresh method. If $\overline{\text{CAS}}$ is held low for the specified period (t_{FCS}) before $\overline{\text{RAS}}$ goes to low, on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation.

Hidden Refresh;

A hidden refresh cycle may takes place while maintaining latest valid data at the output by extending the $\overline{\text{CAS}}$ active time. For the MB 81257, a hidden refresh cycle is $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh.

The internal refresh address counters provide the refresh addresses, as in a normal $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle.

CAS-before-RAS Refresh Counter Test Cycle:

A special timing sequence using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh activated circuitry. After the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation, if $\overline{\text{CAS}}$ goes to high and goes to low again while $\overline{\text{RAS}}$ is held low, the read and write operation are enabled. This is shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

- *A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.
- *A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{\text{CAS}}$.

Suggested $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Procedure

The timing, as shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Cycle, is used for the following operations:

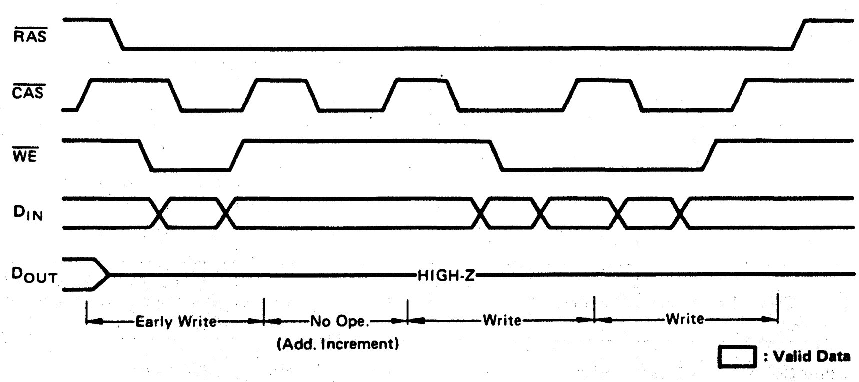
1) Initialize the internal refresh address counter by using eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles.
2) Throughout the test, use the same column address, and keep RA8 high.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

Table 1 – NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{\text{RAS}}$/$\overline{\text{CAS}}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{\text{CAS}}$ (nibble mode)	2	1	10101010	0	10101010	generated internally
toggle $\overline{\text{CAS}}$ (nibble mode)	3	0	10101010	1	10101010	
toggle $\overline{\text{CAS}}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{\text{CAS}}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Fig. 2 — Nibble Mode

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)

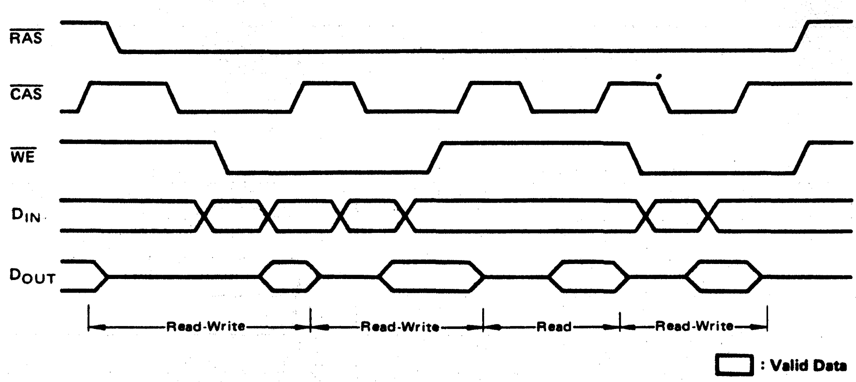
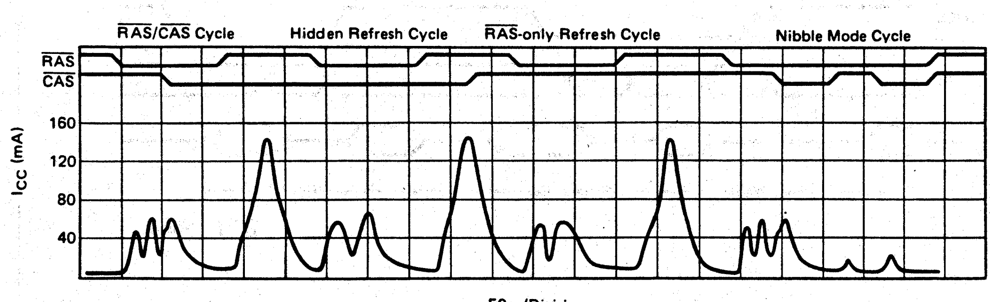


Table-2 FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write ($t_{CWD} \geq t_{CWD}$ (min))
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.

Fig. 3 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 4 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

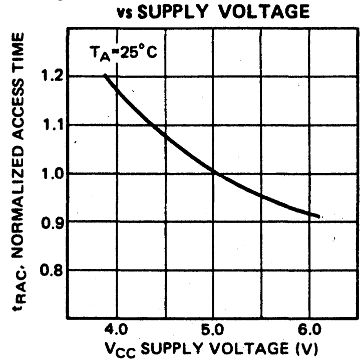


Fig. 5 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

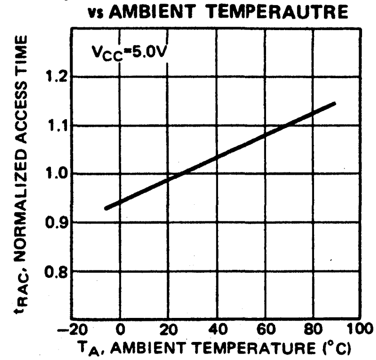


Fig. 6 – OPERATING CURRENT vs CYCLE RATE

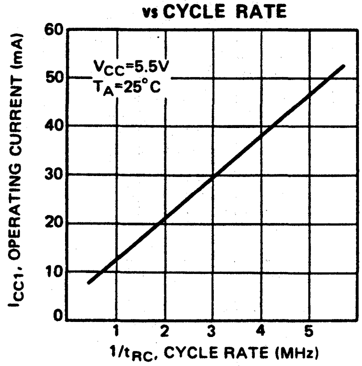


Fig. 7 – OPERATING CURRENT vs SUPPLY VOLTAGE

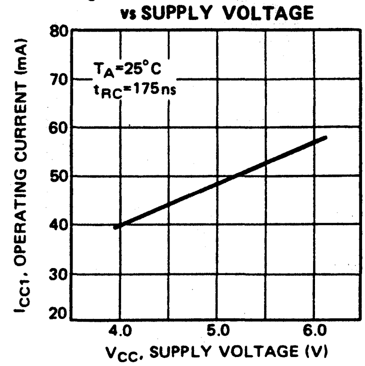


Fig. 8 – OPERATING CURRENT vs AMBIENT TEMPERATURE

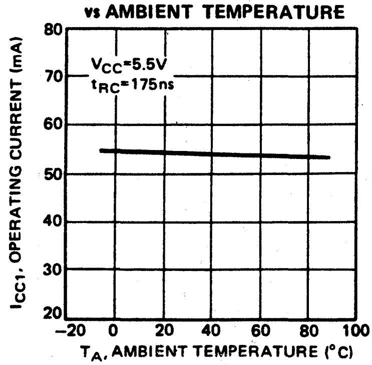


Fig. 9 – STANDBY CURRENT vs SUPPLY VOLTAGE

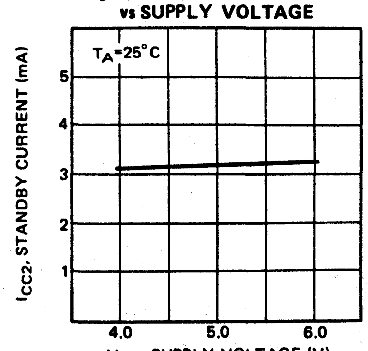


Fig. 10 – STANDBY CURRENT vs AMBIENT TEMPERATURE

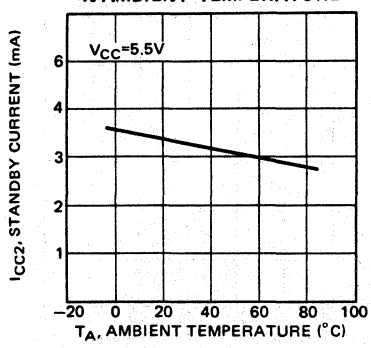


Fig. 11 – REFRESH CURRENT 1 vs CYCLE RATE

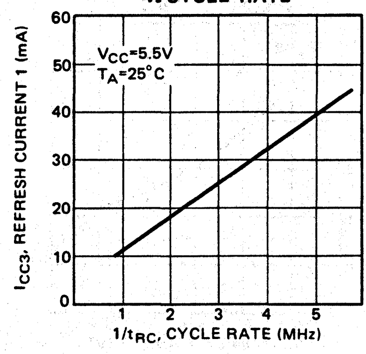


Fig. 12 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

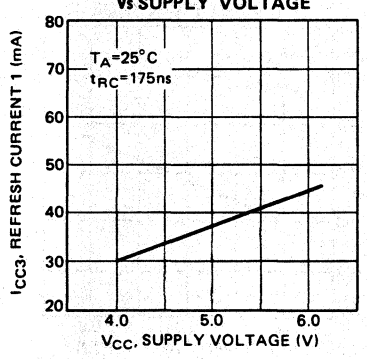


Fig. 13 – NIBBLE MODE CURRENT vs CYCLE RATE

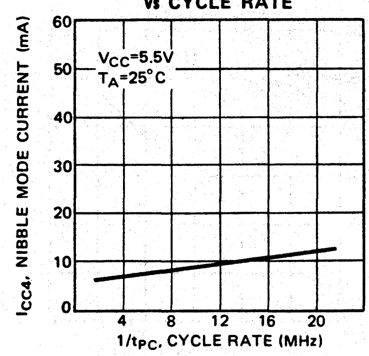


Fig. 14 – NIBBLE MODE CURRENT vs SUPPLY VOLTAGE

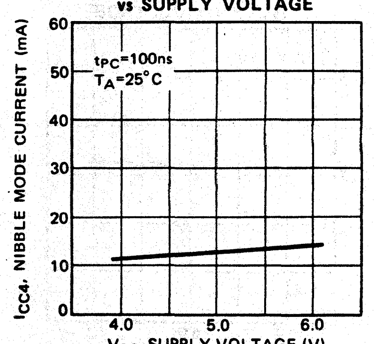


Fig. 15 – REFRESH CURRENT 2 vs CYCLE RATE

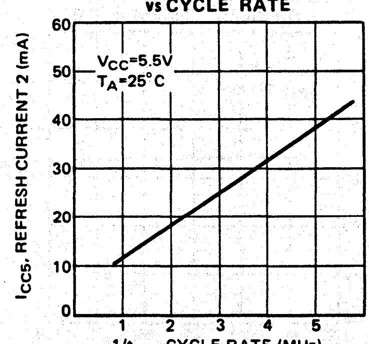


Fig. 16 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

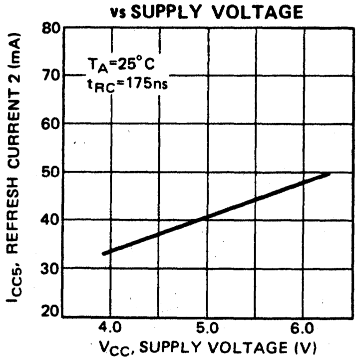


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

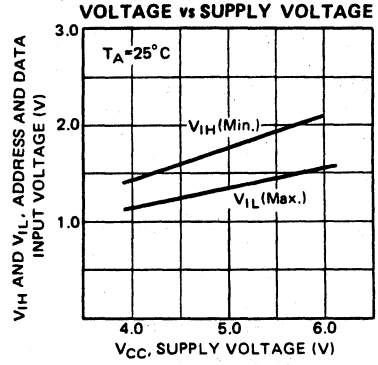


Fig. 18 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

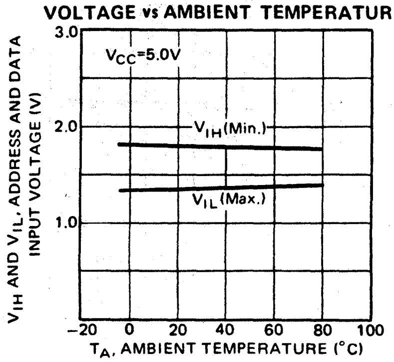


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

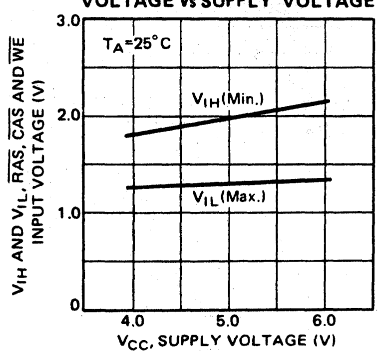


Fig. 20 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

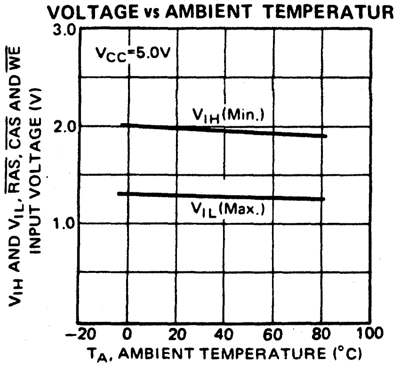


Fig. 21 – ACCESS TIME vs LOAD CAPACITANCE

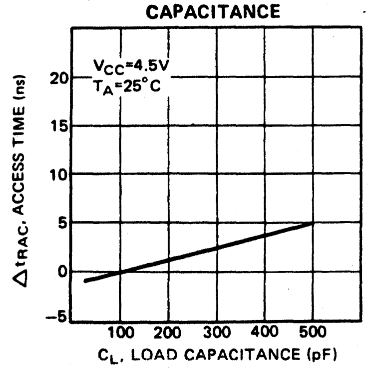


Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

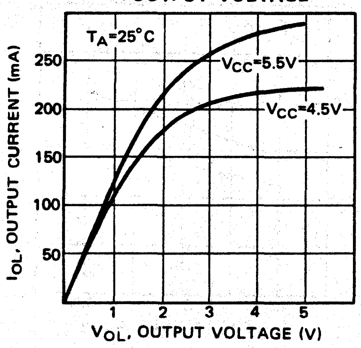


Fig. 23 – OUTPUT CURRENT vs OUTPUT VOLTAGE

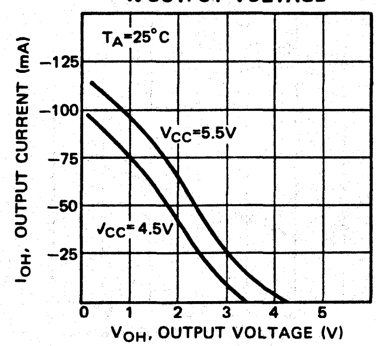
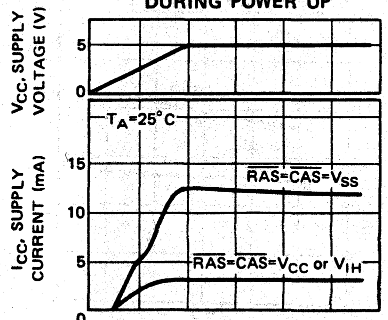
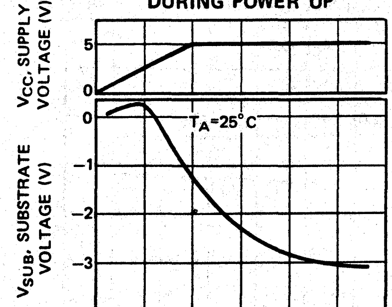


Fig. 24 – CURRENT WAVEFORM DURING POWER UP



50μs/Division

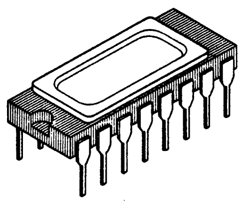
Fig. 25 – SUBSTRATE VOLTAGE DURING POWER UP



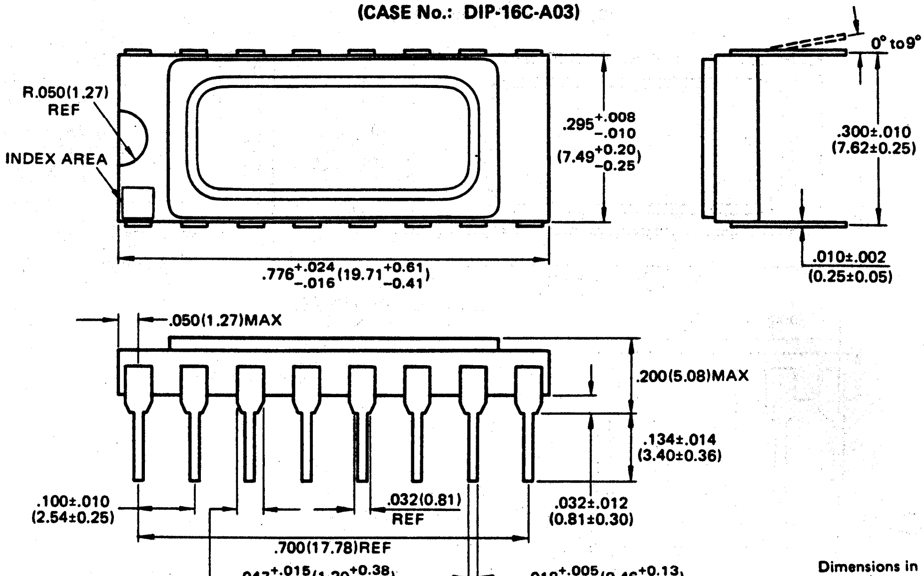
50μs/Division

PACKAGE DIMENSIONS

(Suffix: -C)

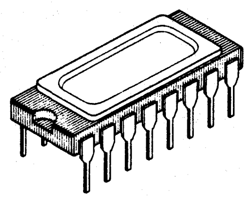


DIP-16C-A03



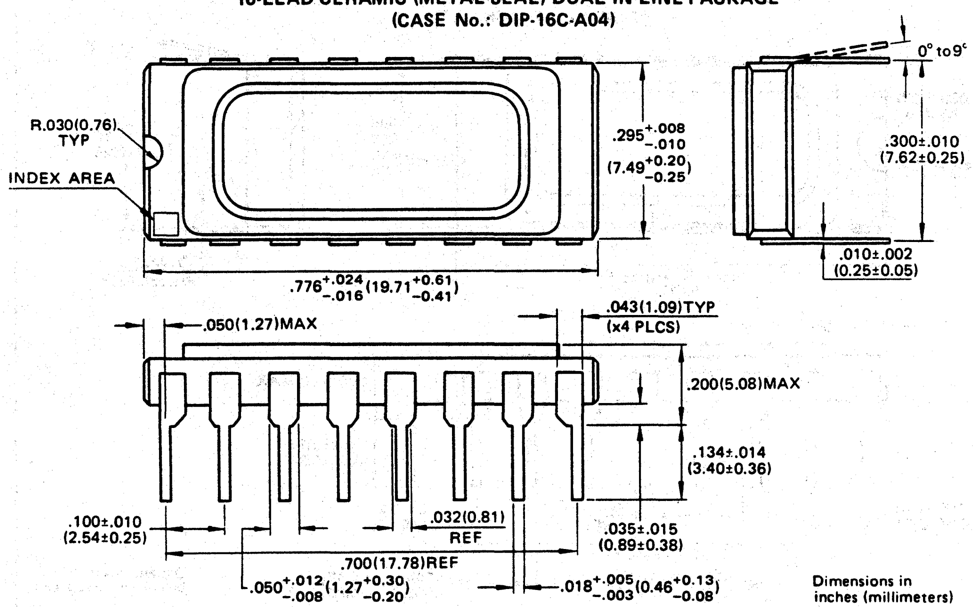
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-16C-A04

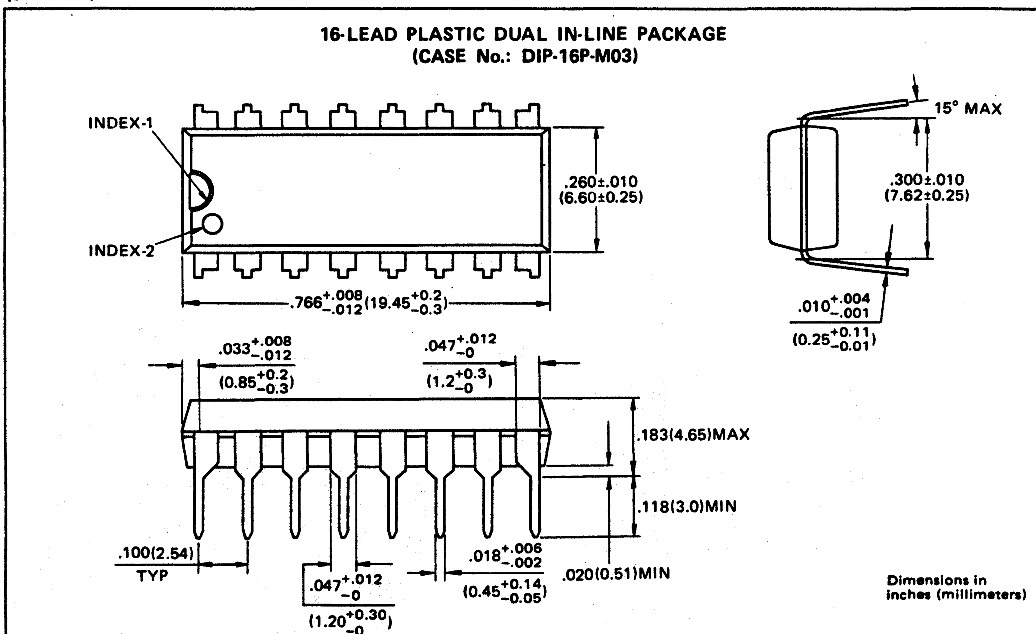
16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A04)



Dimensions in inches (millimeters)

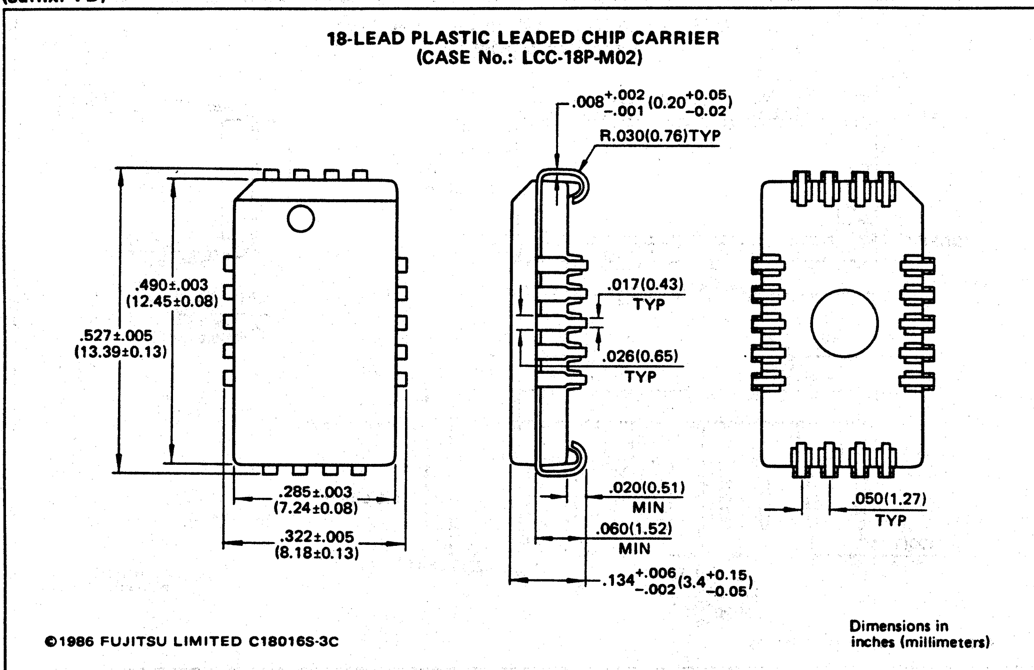
PACKAGE DIMENSIONS

(Suffix: -P)



PACKAGE DIMENSIONS

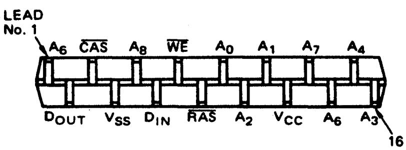
(Suffix: -PD)



PACKAGE DIMENSIONS

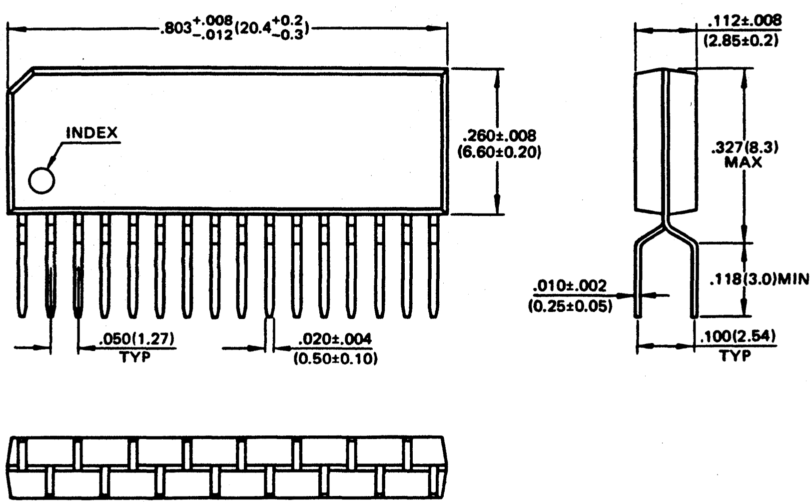
(Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

16 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-16P-M01)



Dimensions in inches (millimeters)

FUJITSU

MOS 262144-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 81464-10
MB 81464-12
MB 81464-15

June 1987
Edition 4.0

65,536 x 4 DYNAMIC RANDOM ACCESS MEMORY

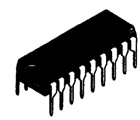
The Fujitsu MB 81464 is fully decoded, dynamic random access memory organized as 65,536 words by 4-bits. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and system memory for microprocessor unit where low power dissipation and compact layout is required.

The multiplex row and column address inputs permit the MB 81464 to be housed in a standard 18 pin DIP, 18 pin PLCC, and 20 pin ZIP. Additionally the MB 81464 offers new functional enhancements that make it more versatile than previous dynamic RAMs. The "$\overline{CAS}$-before-$\overline{RAS}$" refresh cycle is provided an on chip refresh capability. MB 81464 also features "page mode" which allows high speed random access to up 256 bits within a same row.

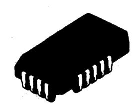
The MB 81464 is fabricated using silicon gate NMOS and Fujitsu's advanced "Triple Layer Polysilicon" process technology. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

The clock timing requirements are non critical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

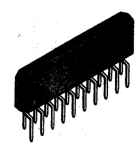
- 65,536 x 4 DRAM, 18 pin DIP, 18 pin PLCC, and 20 pin ZIP.
- Silicon gate, Triple Poly NMOS, single transistor cell.
- Row access time (t_{RAC}),
  - 100 ns max. (MB 81464-10)
  - 120 ns max. (MB 81464-12)
  - 150 ns max. (MB 81464-15)
- Cycle time (t_{RC}),
  - 200 ns min. (MB 81464-10)
  - 220 ns min. (MB 81464-12)
  - 260 ns min. (MB 81464-15)
- Page cycle time (t_{PC}),
  - 100 ns min. (MB 81464-10)
  - 120 ns min. (MB 81464-12)
  - 145 ns min. (MB 81464-15)
- Single +5V supply, 10% tolerance Low power,
  - 385 mW max. (MB 81464-10)
  - 358 mW max. (MB 81464-12)
  - 314 mW max. (MB 81464-15)
  - 27.5 mW max. (Standby)
- On chip substrate bias generator for high performance
- All inputs/outputs are TTL compatible
- 4 ms/256 refresh cycles
- Early write or $\overline{OE}$ controlled write capacity
- "$\overline{CAS}$-before-$\overline{RAS}$", $\overline{RAS}$-only and hidden refresh capability
- Read write capability
- On chip latches for addresses and DQs.
- Compatible with µPD41254, HM50464, and TM4464
- Stanadard 18-pin Ceramic (Metal Seal) DIP (Suffix: -C)
- Standard 18-pin Plastic DIP: (Suffix: -P)
- Standard 18 pin PLCC (Suffix: -PD)
- Standard 20 pin ZIP (Suffix: -PSZ)



PLASTIC PACKAGE
DIP-18P-M03



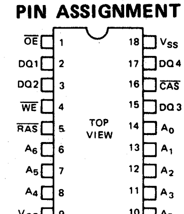
PLASTIC PACKAGE
LCC-18P-M02

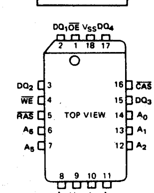


PLASTIC PACKAGE
ZIP-20P-M01

DIP-18C-A01: See Page 22

PIN ASSIGNMENT





Pin assignment for ZIP: See page 21

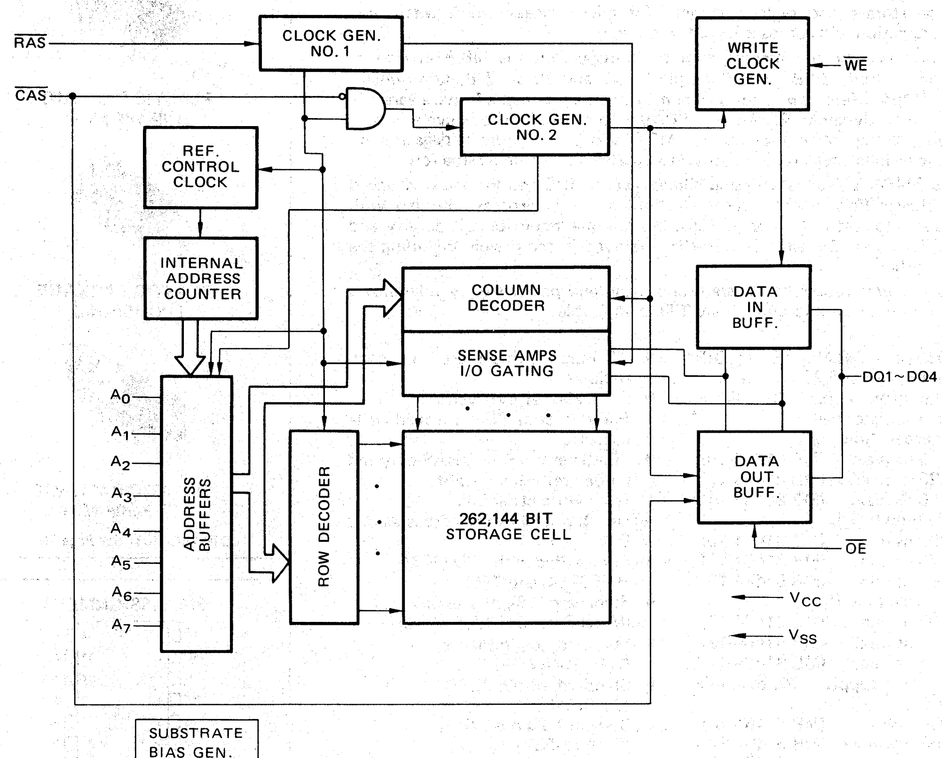
ABSOLUTE MAXIMUM RATING (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	–1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	–1 to +7	V
Storage temperature	Ceramic	T_{STG}	–55 to +150	°C
	Plastic		–55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 81464 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance A_0 to A_7	C_{IN1}	—	7	pF
Input Capacitanct $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	10	pF
Data I/O Capacitance (DQ1 to DQ4)	C_{DQ}	—	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to 70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	–	6.5	V	
Input Low Voltage, all inputs except DQ	V_{IL}	-2.0	–	0.8	V	
Input Low Voltage, DQ	V_{ILD}*	-1.0	–	0.8	V	

* The device will withstand undershoots to the -2.0 V level with a maximum pulse width of 20 ns at the -1.5 V level.

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81464-10	I_{CC1}			70	mA
	MB 81464-12				65	
	MB 81464-15				57	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}			5.0	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81464-10	I_{CC3}			60	mA
	MB 81464-12				55	
	MB 81464-15				50	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling; t_{PC} = min)	MB 81464-10	I_{CC4}			40	mA
	MB 81464-12				35	
	MB 81464-15				30	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81464-10	I_{CC5}			65	mA
	MB 81464-12				60	
	MB 81464-15				55	
INPUT LEAKAGE CURRENT any input ($0V \leqq V_{IN} \leqq 5.5V$, $4.5V \leqq V_{CC} \leqq 5.5V$, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0 V \leqq V_{OUT} \leqq 5.5 V$)		$I_{DQ(L)}$	-10		10	μA
OUTPUT LEVEL Output High Voltage (I_{OH} = -5 mA)		V_{OH}	2.4			V
OUTPUT LEVEL Output Low Voltage (L_{OL} = 4.2 mA)		V_{OL}			0.4	V

* : I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
I_{CC} is dependent on input low voltage level V_{ILD}, $V_{ILD} > -0.5$ V.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB 81464-10		MB 81464-12		MB 81464-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4		4	ms
Random Read/Write Cycle Time		t_{RC}	200		220		260		ns
Read-Modify-Write Cycle Time		t_{RWC}	270		305		345		ns
Page Mode Cycle Time		t_{PC}	100		120		145		ns
Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	170		195		225		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		50		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	80		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	50		60		75		ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	40		50		60		ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	30		32		35		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	50	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	10		15		20		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		0		ns
Write Command Set Up Time	10	t_{WCS}	–5		–5		–5		ns
Write Command Hold Time		t_{WCH}	25		30		35		ns
Write Command Pulse Width		t_{WP}	25		30		35		ns
Write Command to $\overline{RAS}$ Lead Time	10	t_{RWL}	35		40		45		ns

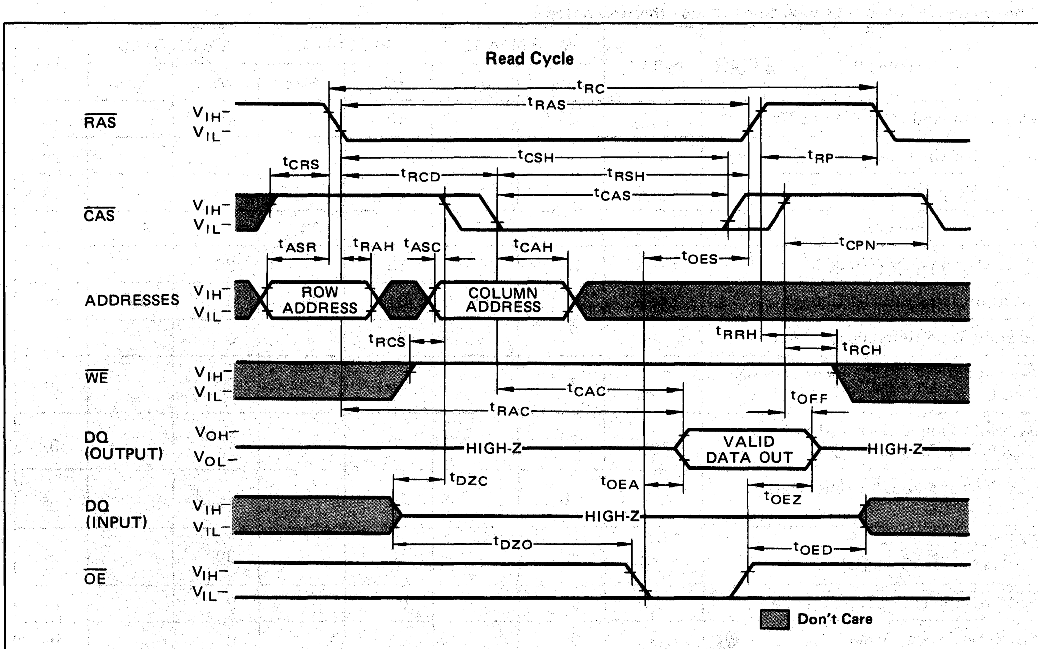
AC CHARACTERISTICS (cont'd)

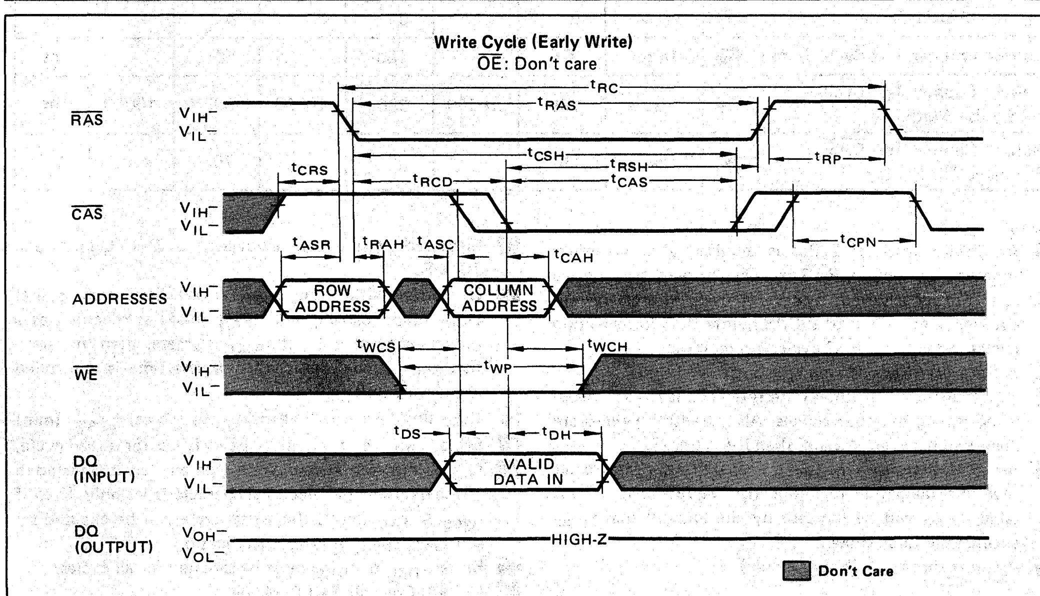
(At recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 81464-10		MB 81464-12		MB 81464-15		Unit
			Min	Max	Min	Max	Min	Max	
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		40		45		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	25		30		35		ns
Access Time from $\overline{OE}$		t_{OEA}		27		30		40	ns
$\overline{OE}$ to Data In Delay Time		t_{OED}	25		25		30		ns
Output Buffer Turn Off Delay from $\overline{OE}$		t_{OEZ}	0	25	0	25	0	30	ns
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$		t_{OEH}	0		0		0		ns
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)		t_{FCS}	20		20		20		ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)		t_{FCH}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time (Refresh cycles)		t_{RPC}	10		10		10		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycles)		t_{CPR}	30		30		30		ns
$\overline{OE}$ to $\overline{RAS}$ in active Set Up Time		t_{OES}	0		0		0		ns
D_{IN} to $\overline{CAS}$ Delay Time	11	t_{DZC}	0		0		0		ns
D_{IN} to $\overline{OE}$ Delay Time	11	t_{DZO}	0		0		0		ns
Refresh Counter Test Cycle Time	12	t_{RTC}	375		430		505		ns
Refresh Counter Test Cycle $\overline{RAS}$ Pulse Width	12	t_{TRAS}	285	10000	330	10000	395	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	12	t_{CPT}	50		60		70		ns

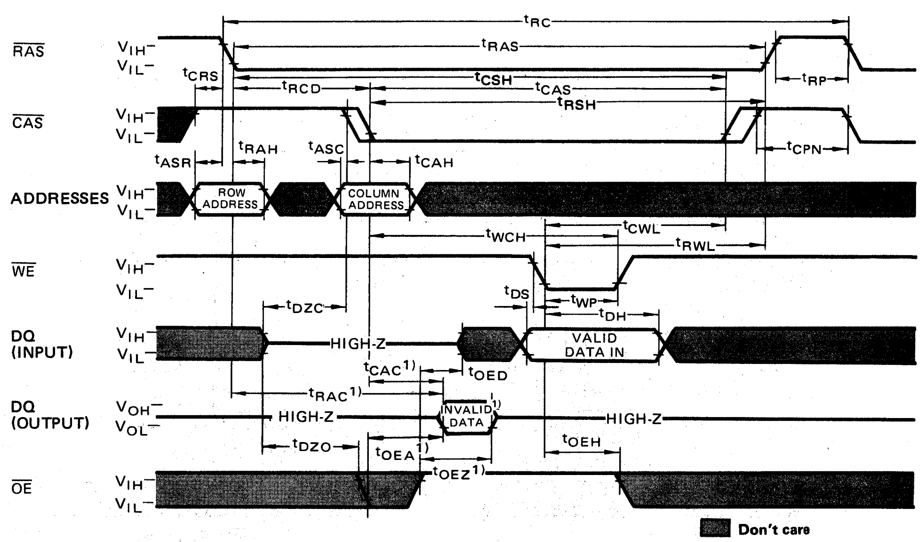
Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. Even if $t_{WCS} \leqq t_{WCS}$(min), the write cycle can be excuted by satisfying t_{RWL} or t_{CWL} specification.
11. Either t_{DZC} or t_{DRO} must be satisfied for all cycles.
12. Refresh Counter Test Cycle only.

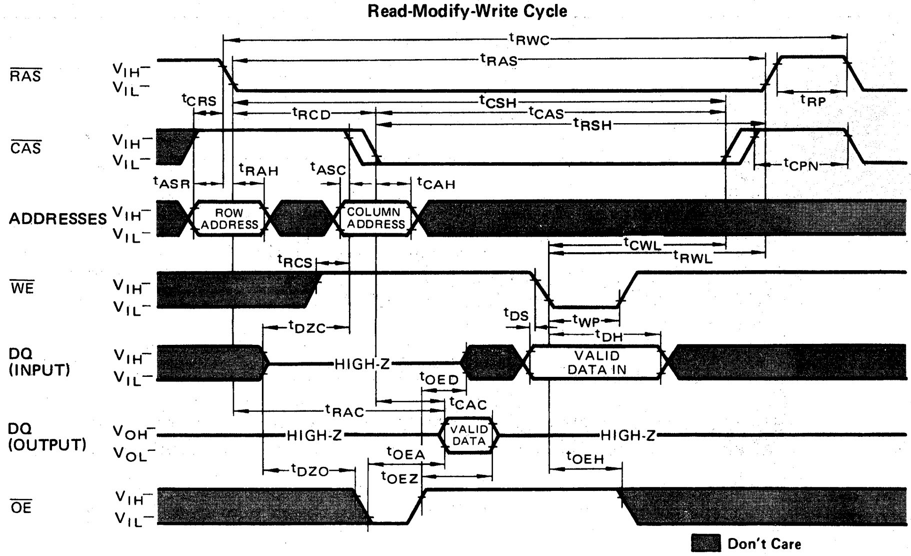

Read Cycle
tRC
tRAS
RAS
VIH
VIL
tCRS
tCSH
tRCD
tRSH
tCAS
tRP
CAS
tASR
tRAH
tASC
tCAH
tOES
tCPN
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
tRCH
WE
tCAC
tRAC
tOFF
DQ (OUTPUT)
VOH
VOL
HIGH-Z
VALID DATA OUT
tDZC
tOEA
tOEZ
DQ (INPUT)
tDZO
tOED
OE
Don't Care


Write Cycle (Early Write)
OE: Don't care
tRC
tRAS
RAS
VIH
VIL
tCRS
tCSH
tRSH
tRCD
tCAS
tRP
CAS
tASR
tRAH
tASC
tCAH
tCPN
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tWCS
tWCH
tWP
WE
tDS
tDH
DQ (INPUT)
VALID DATA IN
DQ (OUTPUT)
VOH
VOL
HIGH-Z
Don't Care

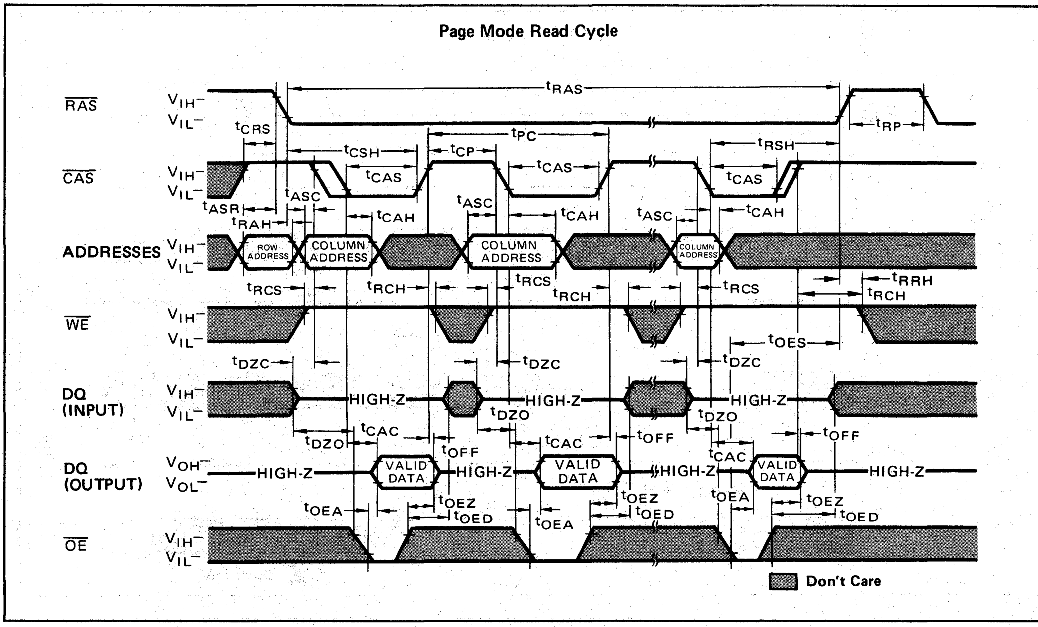
$\overline{OE}$ Write Cycle

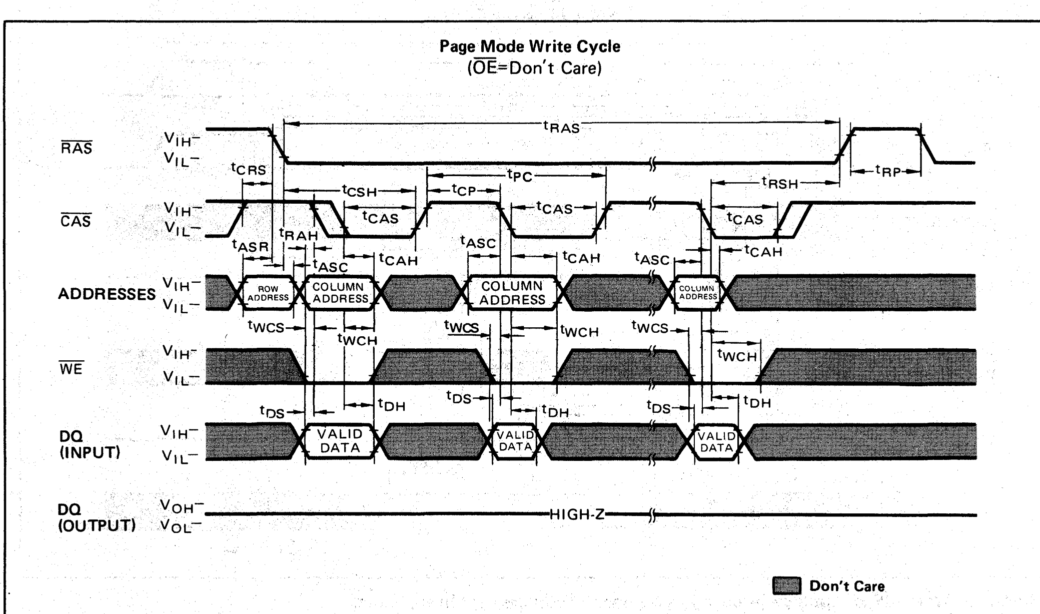


Read-Modify-Write Cycle

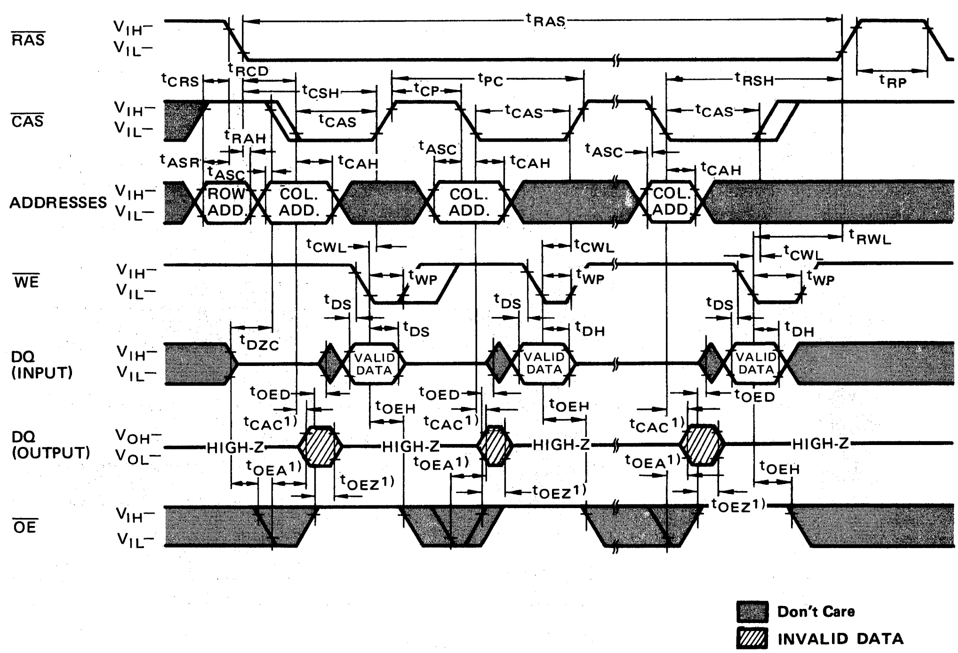


Note: 1) When $\overline{OE}$ is kept high through a cycle, the DQ pins are kept high-Z state.


Page Mode Read Cycle
RAS
CAS
ADDRESSES
WE
DQ (INPUT)
DQ (OUTPUT)
OE
ROW ADDRESS
COLUMN ADDRESS
HIGH-Z
VALID DATA
Don't Care

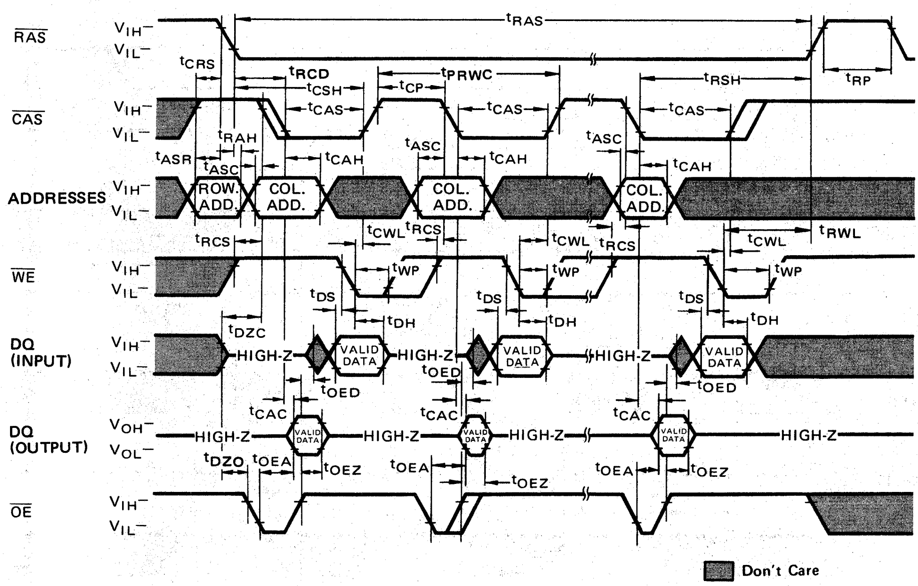

Page Mode Write Cycle
(OE=Don't Care)
RAS
CAS
ADDRESSES
WE
DQ (INPUT)
DQ (OUTPUT)
ROW ADDRESS
COLUMN ADDRESS
VALID DATA
HIGH-Z
Don't Care

Page Mode $\overline{OE}$ Write Cycle

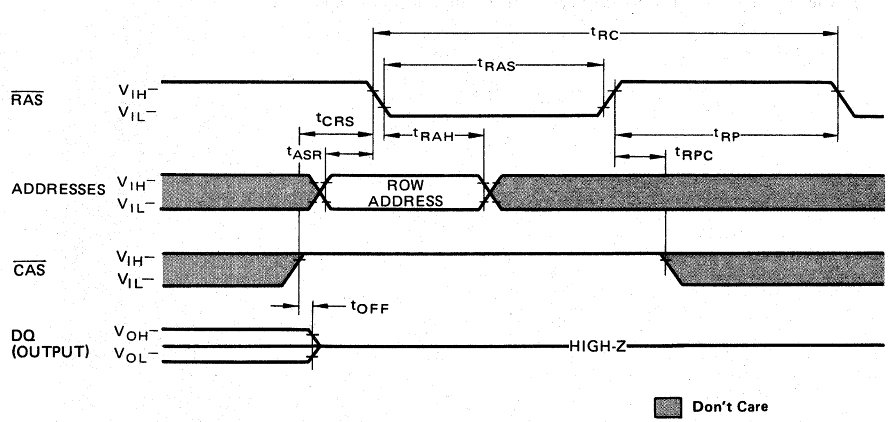


Note: 1) When $\overline{OE}$ is kept high through a cycle, the DQ pins are kept high-Z state.

Page Mode Read Modify-Write Cycle

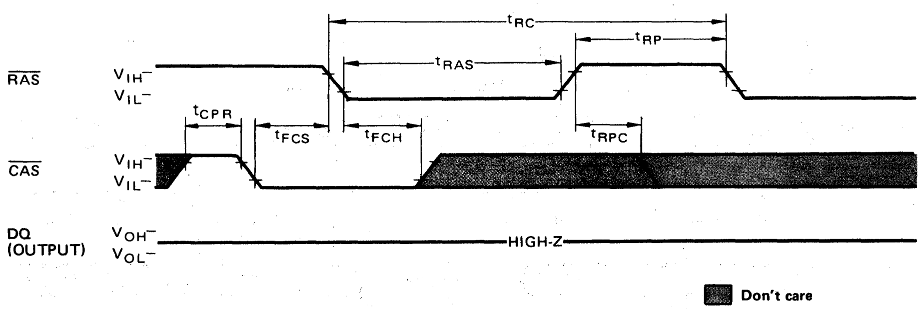


$\overline{RAS}$-Only Refresh Cycle
($\overline{WE}$, $\overline{OE}$=Don't Care)

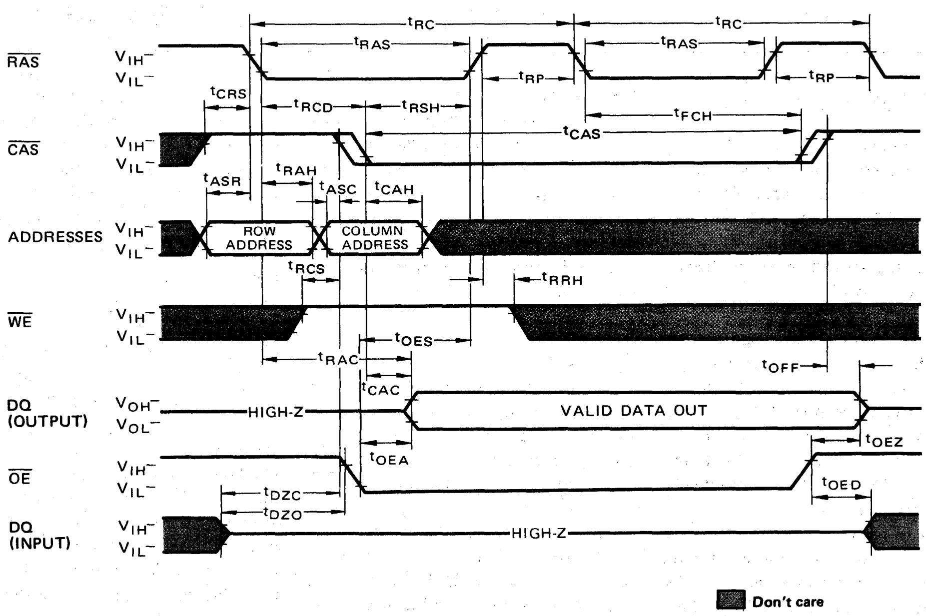


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

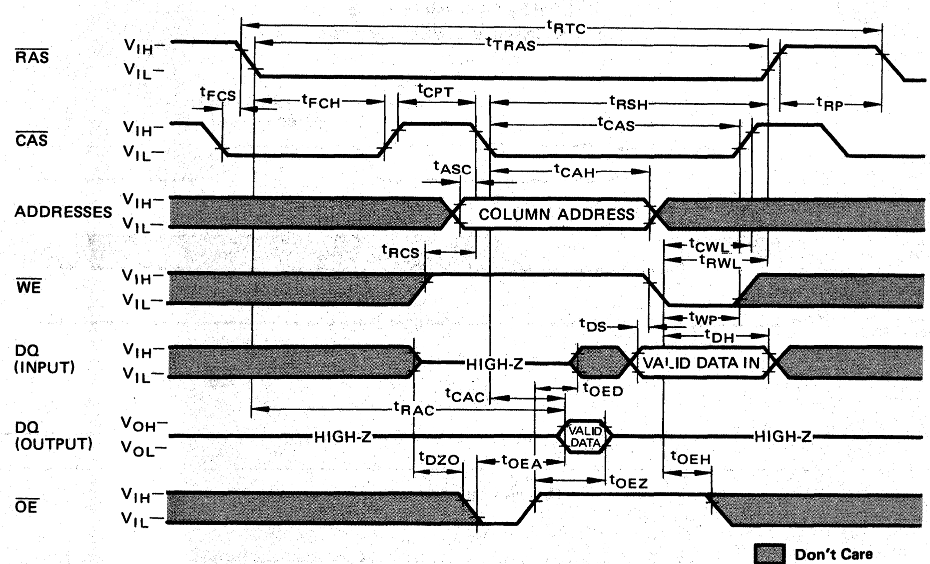
NOTE: Addresses, $\overline{WE}$, $\overline{OE}$ = Don't care



Hidden Refresh Cycle



Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode parallel 4 bits of 262,144 storage cell locations within the MB 81464.

Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins (A_0 through A_7) and latched with the Column Address Strobe ($\overline{CAS}$).

The row and column address inputs must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the Write Enable ($\overline{WE}$) input. A high on $\overline{WE}$ selects read mode and low selects write mode. The data inputs are disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data-outs will remain in the high-impedance state allowing a write cycle.

Data Pins:

Data Inputs;

Data are written during a write or read-modify-write cycle. The later falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed by $\overline{CAS}$ with setup and hold times referenced to $\overline{CAS}$. In a read-modify-write cycle, thus the data will be strobed by $\overline{WE}$ with set-up and hold times referenced to $\overline{WE}$.

In a read-modify-write cycle, $\overline{OE}$ must be low after t_{DZO} to change the data pins from input mode to output mode and then $\overline{OE}$ must be changed to low before t_{OED} to return the data pins to input mode. In an early write cycle, data pins are in input mode regardless of the status of $\overline{OE}$.

Data Outputs;

The three-state output buffers provide direct TTL compatibility with a fan out of two standard TTL loads. Data-out are the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle, the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied. The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ and $\overline{OE}$ are low. In a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high brings the outputs into the high impedance state.

Output Enable:

The $\overline{\text{OE}}$ controls the impedance of the output buffers. In the high state on $\overline{\text{OE}}$, the output buffers are high impedance state. In the low state on $\overline{\text{OE}}$, the output buffers are low impedance state. But in early write cycle, the output buffers are in high impedance state even if $\overline{\text{OE}}$ is low. In the page mode read cycle, $\overline{\text{OE}}$ can be allowed low through the cycle. In the page mode early write cycle, $\overline{\text{OE}}$ can be allowed high throughout the cycle. In the page mode read-modify-write or delayed write cycle, $\overline{\text{OE}}$ must be changed from low to high with t_{OED}.

Page Mode:

Page Mode operation permits strobing the row-address into the MB 81464 while maintaining $\overline{\text{RAS}}$ at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{\text{RAS}}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh;

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 through A_7) at least every four milliseconds.

The MB 81464 offeres the following three types of refresh.

$\overline{\text{RAS}}$-Only Refresh:

$\overline{\text{RAS}}$-only refresh avoids any output during refresh because the output bufuers are in the high impedance state unless $\overline{\text{CAS}}$ is brought low. Strobing each of 256 row-addresses with $\overline{\text{RAS}}$ will cause all bits in each row to be refreshed.

Further $\overline{\text{RAS}}$-only refresh results in a substantial reduction in power dissipation.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh;

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing available on the MB 81464 offers an alternate refresh method. If $\overline{\text{CAS}}$ is held low for the specified period (t_{FCS}) before $\overline{\text{RAS}}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and a internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{\text{CAS}}$ active time.

In MB 81464, hidden refresh means $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh and the internal refresh addresses from the counter are used to refresh addresses i.e., it doesn't need to apply refresh addresses, because $\overline{\text{CAS}}$ is always low when $\overline{\text{RAS}}$ goes to low in the cycle.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh activated circuitry. After the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation, if $\overline{\text{CAS}}$ goes to high and goes to low again while $\overline{\text{RAS}}$ is held low, the read and write operation are enabled. This is shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

*A ROW ADDRESS – All bits are defined by the refresh counter.

*A COLUMN ADDRESS – All the bits A_0 to A_7 are defined by latching levels on A_0 to A_7 at the second falling edge of $\overline{\text{CAS}}$.

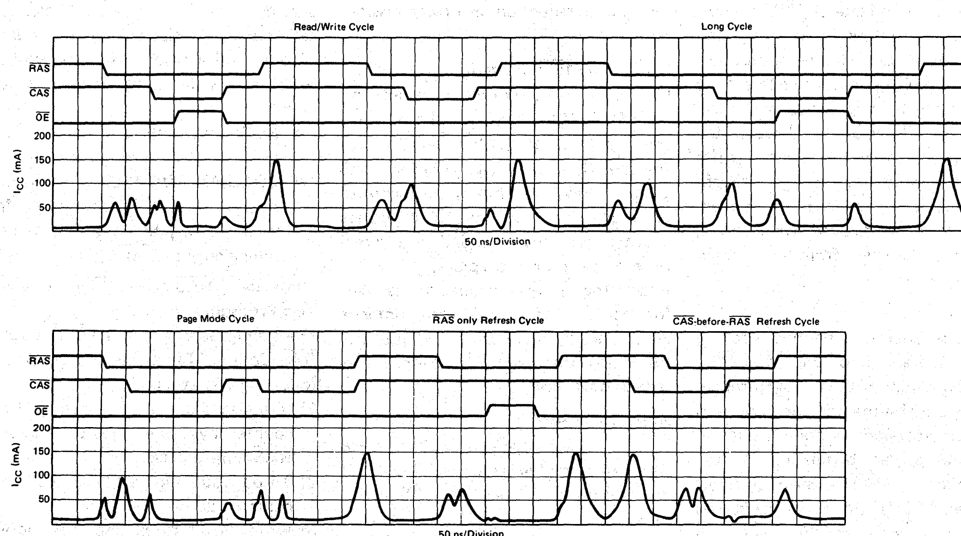
Suggested $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Procedure

The timing, as shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Cycle, is used for the following operations:

1) Initialize the internal refresh address counter by using eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

1

Fig. 2 — CURRENT WAVEFORM (V_{CC} = 5.5 V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 — NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

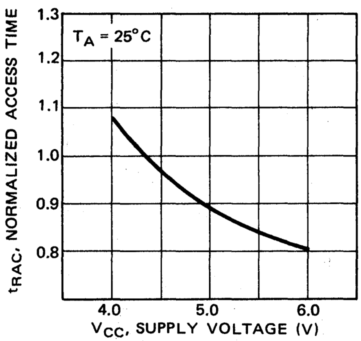


Fig. 4 — NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

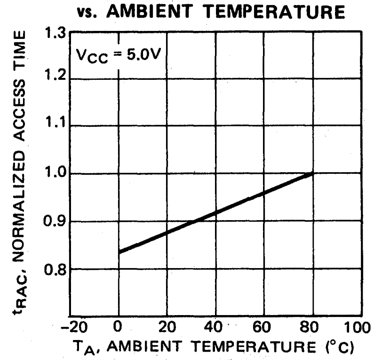


Fig. 5 — OPERATING CURRENT vs. CYCLE RATE

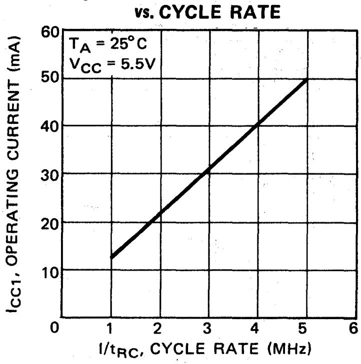


Fig. 6 — OPERATING CURRENT vs. SUPPLY VOLTAGE

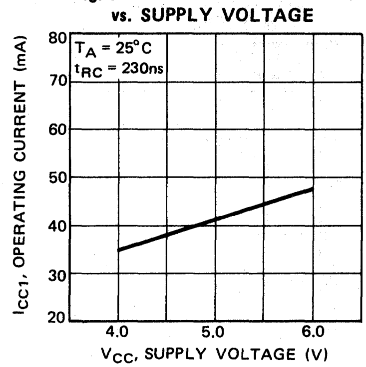


Fig. 7 — OPERATING CURRENT vs. AMBIENT TEMPERATURE

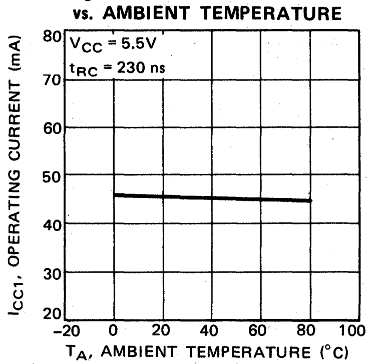


Fig. 8 — STANDBY CURRENT vs. SUPPLY VOLTAGE

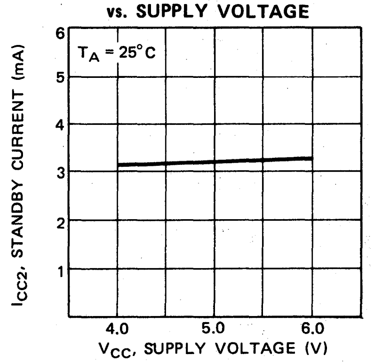


Fig. 9 — STANDBY CURRENT vs. AMBIENT TEMPERATURE

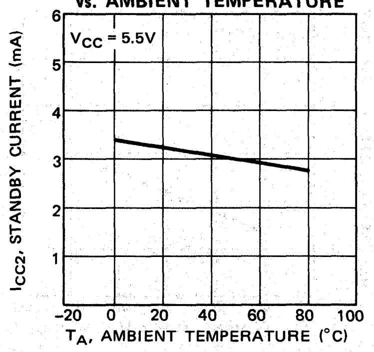


Fig. 10 — REFRESH CURRENT 1 vs. CYCLE RATE

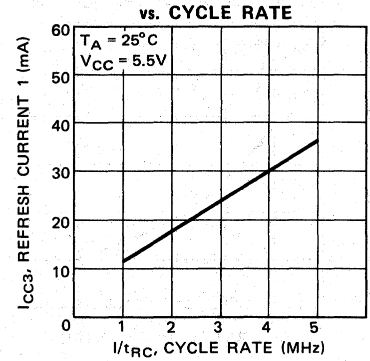


Fig. 11 — REFRESH CURRENT 1 vs. SUPPLY VOLTAGE

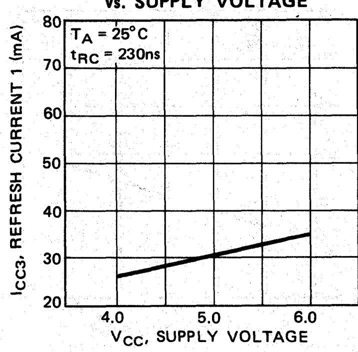


Fig. 12 — PAGE MODE CURRENT vs. CYCLE RATE

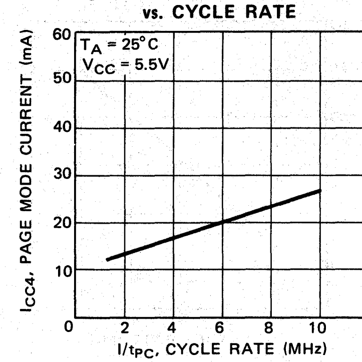


Fig. 13 — PAGE MODE CURRENT vs. CYCLE RATE

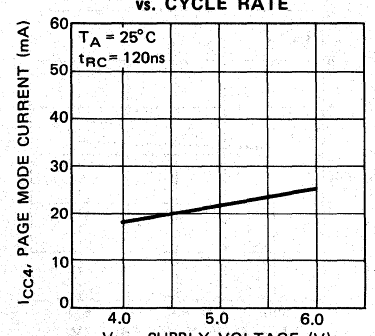


Fig. 14 — REFRESH CURRENT 2 vs. CYCLE RATE

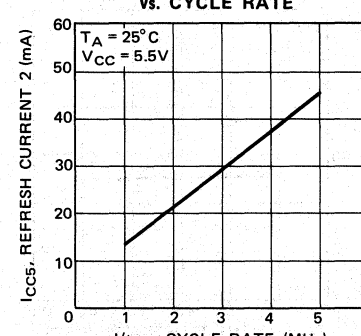


Fig. 15 — REFRESH CURRENT 2 vs. SUPPLY VOLTAGE

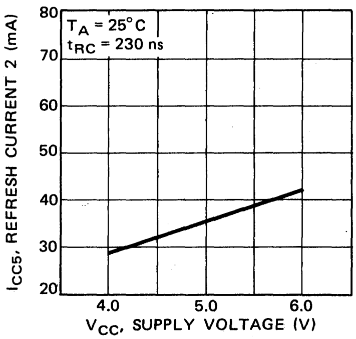


Fig. 16 — ADDRESS AND DATA INPUT VOLTAGE vs. SUPPLY VOLTAGE

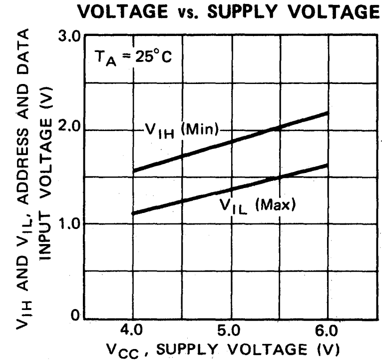


Fig. 17 — ADDRESS AND DATA INPUT VOLTAGE vs. AMBIENT TEMPERATURE

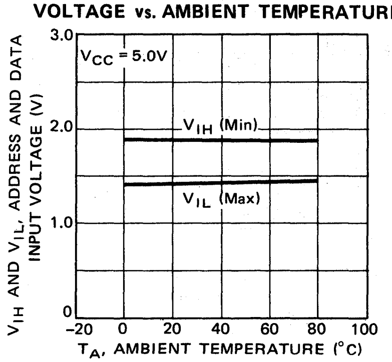


Fig. 18 — $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. SUPPLY VOLTAGE

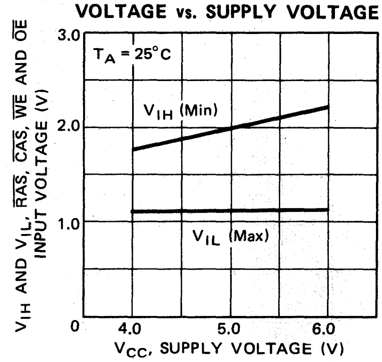


Fig. 19 — $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. AMBIENT TEMPERATURE

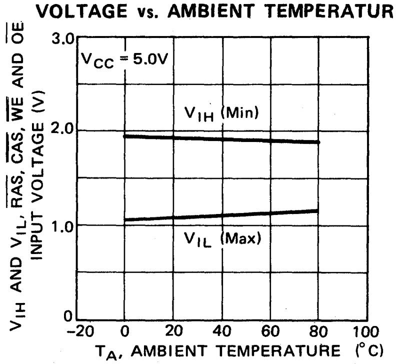


Fig. 20 — ACCESS TIME vs. LOAD CAPACITANCE

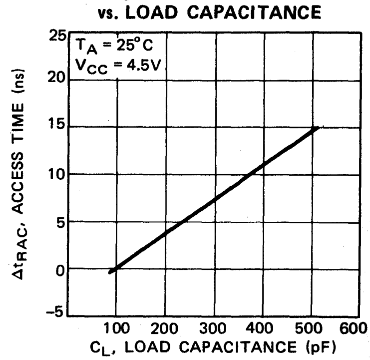


Fig. 21 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

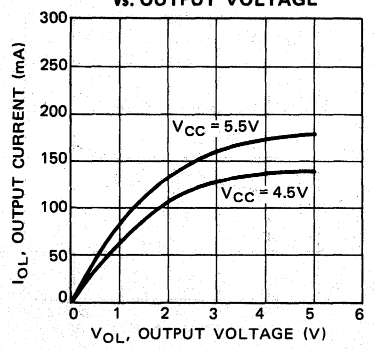


Fig. 22 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

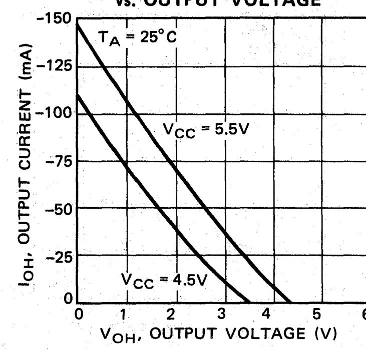


Fig. 23 – SUBSTRATE VOLTAGE DURING POWER UP

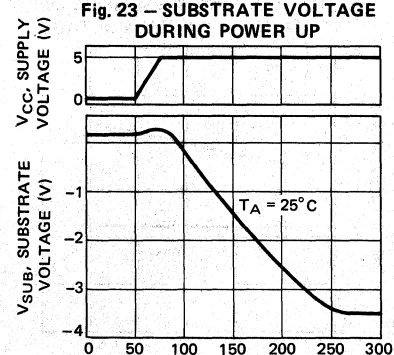
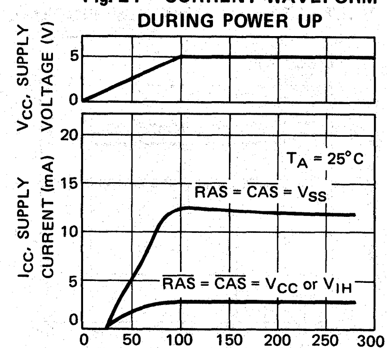
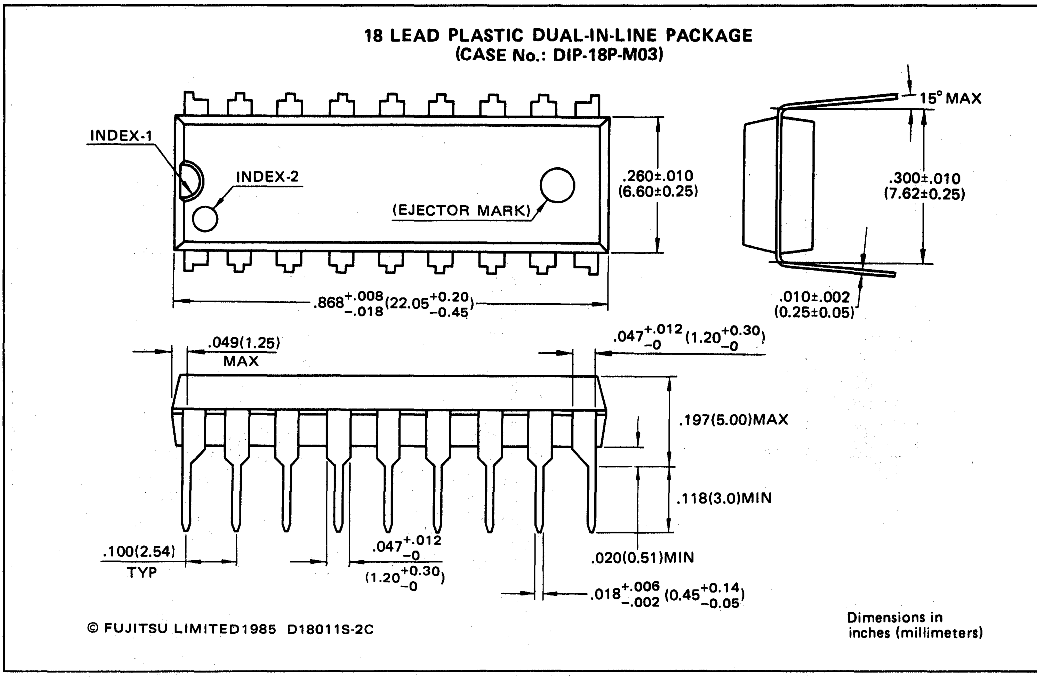


Fig. 24 – CURRENT WAVEFORM DURING POWER UP



PACKAGE DIMENSIONS

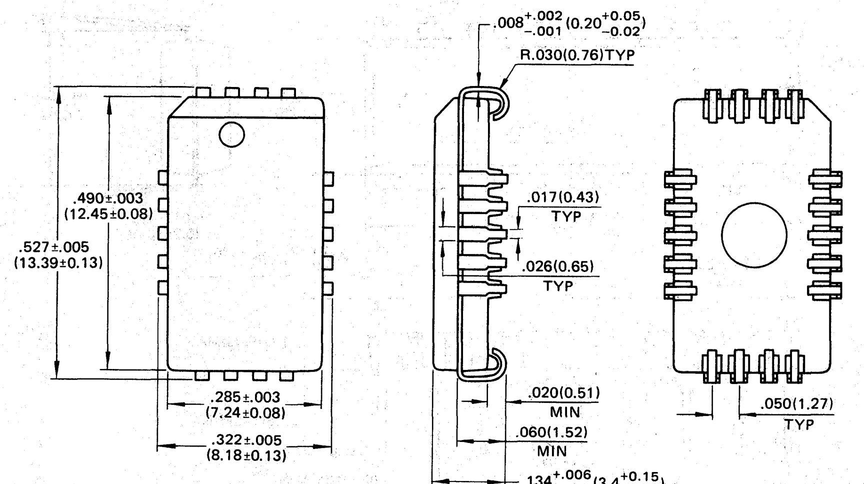
(Suffix: -P)



PACKAGE DIMENSIONS

(Suffix: -PD)

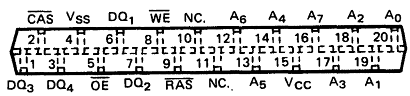
18-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-18P-M02)



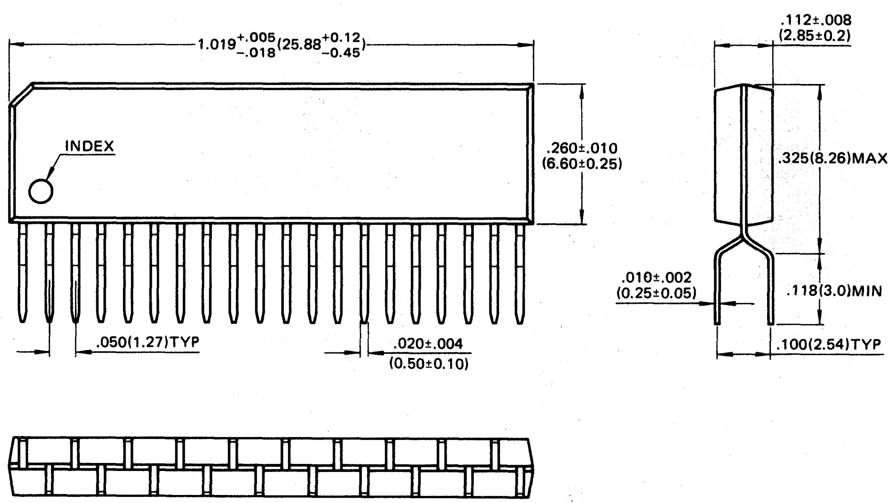
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PSZ)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE (CASE NO.: ZIP-20P-M01)

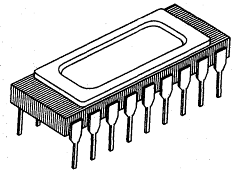


 Z20001S-3C

Dimensions in inches (millimeters)

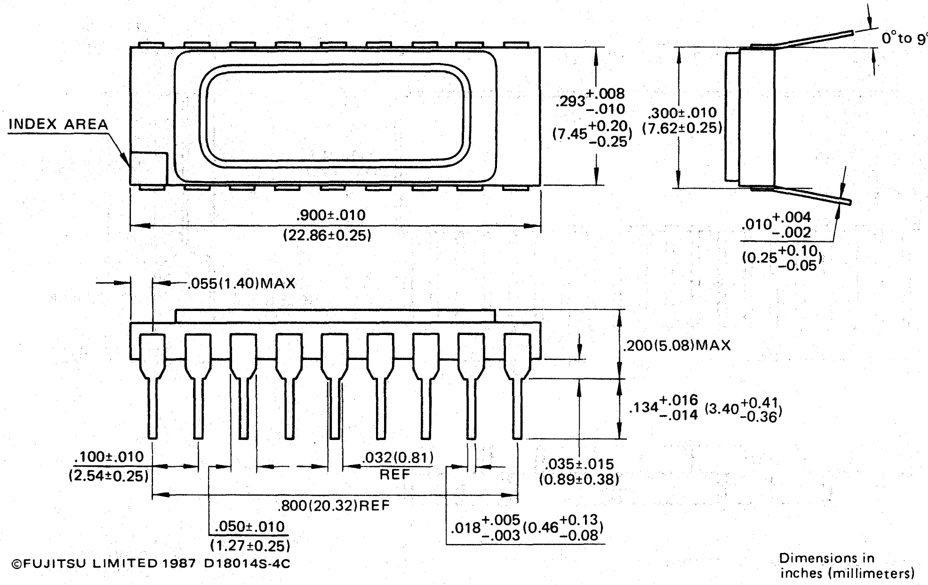
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-18C-A01

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

Section 2

CMOS DRAMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options			Sealing Method
2-3	MB81C258-10	100	262144 bits	16-pin	Plastic	DIP	Plastic
	MB81C258-12	120	(262144w x 1b)	18-pad	Plastic	LCC	Plastic
	MB81C258-15	150					
2-25	MB81C466-10	100	262144 bits	18-pin	Ceramic	DIP	Metal
	MB81C466-12	120	(65536w x 4b)	18-pin	Plastic	DIP	Plastic
	MB81C466-15	150		20-pin	Plastic	ZIP	Plastic
2-41	MB81C1000-70	70	1048576 bits	18-pin	Ceramic	DIP	Metal
	MB81C1000-80	80	(1048576w x 1b)	18-pin	Plastic	DIP	Plastic
	MB81C1000-10	100		20-pin	Plastic	ZIP	Plastic
	MB81C1000-12	120		26-pad	Plastic	LCC	Plastic
2-61	MB81C1001-70	70	1048576 bits	20-pin	Plastic	ZIP	Plastic
	MB81C1001-80	80	(1048576w x 1b)	18-pin	Ceramic	DIP	Metal
	MB81C1001-10	100		18-pin	Plastic	DIP	Plastic
	MB81C1001-12	120		26-pad	Plastic	LCC	Plastic
2-81	MB81C1002-85	85	1048576 bits	18-pin	Ceramic	DIP	Metal
	MB81C1002-10	100	(1048576w x 1b)	18-pin	Plastic	DIP	Plastic
	MB81C1002-12	120		20-pin	Plastic	DIP	Plastic
				26-pad	Plastic	LCC	Plastic
2-105	MB81C1003-85	85	1048576 bits	18-pin	Ceramic	DIP	Metal
	MB81C1003-10	100	(1048576w x 1b)	18-pin	Plastic	DIP	Plastic
	MB81C1003-12	120		20-pin	Plastic	ZIP	Plastic
				26-pad	Plastic	LCC	Plastic
2-123	MB81C4256-85	85	1048576 bits	20-pin	Ceramic	DIP	Metal
	MB81C4256-10	100	(262144w x 4b)	20-pin	Plastic	DIP	Plastic
	MB81C4256-12	120		20-pin	Plastic	ZIP	Plastic
				26-pad	Plastic	LCC	Plastic
2-147	MB81C4257-85	85	1048576 bits	20-pin	Ceramic	DIP	Metal
	MB81C4257-10	100	(262144w x 4b)	20-pin	Plastic	DIP	Plastic
	MB81C4257-12	120		20-pin	Plastic	ZIP	Plastic
				26-pad	Plastic	LCC	Plastic
				26-pad	Ceramic	LCC	Metal

CMOS DRAMs
(Continued)

Page	Device	Maximum Access Time(ns)	Capacity	Package Options		Sealing Method
2-175	MB81C4258-85	85	1048576 bits	20-pin Plastic	ZIP	Plastic
	MB81C4258-10	100	(262144w x 4b)	26-pad Plastic	LCC	Plastic
	MB81C4258-12	120		20-pin Ceramic	DIP	Metal
				20-pin Plastic	DIP	Plastic
2-199	MB81C4259-85	85	1048576 bits	20-pin Ceramic	DIP	Metal
	MB81C4259-10	100	(262144w x 4b)	20-pin Plastic	DIP	Plastic
	MB81C4259-12	120		20-pin Plastic	ZIP	Plastic
				26-pad Ceramic	LCC	Metal
				26-pad Plastic	LCC	Plastic
2-225	MB814100-80	80	4194304 bits	18-pin Plastic	DIP	Plastic
	MB814100-10	100	(4194304w x 1b)	20-pin Plastic	ZIP	Plastic
	MB814100-12	120		26-pad Plastic	LCC	Plastic

FUJITSU

262144 BIT CMOS STATIC COLUMN DYNAMIC RAM

MB81C258-10
MB81C258-12
MB81C258-15

2

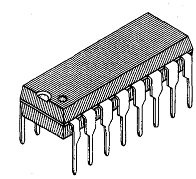
October 1988
Edition 3.0

262,144 x 1 BIT CMOS STATIC COLUMN DYNAMIC RAM

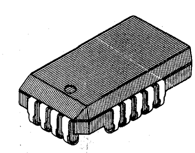
The Fujitsu MB 81C258 is CMOS static column dynamic random access memory, SC-DRAM, which is organized as 262144 word by 1 bit. This SC-DRAM is designed for high speed, high performance applications such as main frame memory, buffer memory, and video memory, and for applications to battery backed-up systems where very low power dissipation and compact layout is required.

The advantage of SC-DRAM is achieving the static mode operation such as read, write and read-modify-write cycles in spite of dynamic RAM and the fast read and write operation can be performed by this mode.

The MB 81C258 is fabricated using silicon gate CMOS process. Since the CMOS circuit dissipates very small power, it can be easily used in battery backed-up application system such as hand held computer.
The MB 81C258 is pin compatible with HM 51258.
All inputs and outputs are TTL compatible.



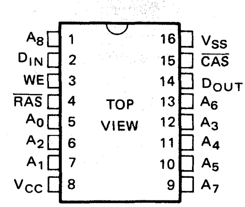
PLASTIC PACKAGE
DIP-16P-M03

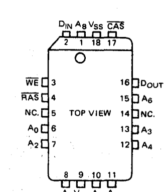


PLASTIC PACKAGE
LCC-18P-M02

- 262144 x 1 SC-DRAM, 16-pin DIP/18-pin PLCC
- Silicon-gate, CMOS, single transistor cell
- Row Access Time (t_{RAC}),
  100 ns max. (MB 81C258-10)
  120 ns max. (MB 81C258-12)
  150 ns max. (MB 81C258-15)
- Random Cycle Time (t_{RC}),
  200 ns min. (MB 81C258-10)
  230 ns min. (MB 81C258-12)
  260 ns min. (MB 81C258-15)
- Address Access Time (t_{AA}),
  45 ns max. (MB 81C258-10)
  55 ns max. (MB 81C258-12)
  70 ns max. (MB 81C258-15)
- Static Mode Cycle Time (t_{SC}),
  50 ns min. (MB 81C258-10)
  60 ns min. (MB 81C258-12)
  75 ns min. (MB 81C258-15)
- Low Power Dissipation
  330 mW max. (MB 81C258-10)
  275 mW max. (MB 81C258-12)
  248 mW max. (MB 81C258-15)
  11 mW max. (TTL level input)
  1.65 mW max. (CMOS level input)
- Single 5V supply, ±10% tolerance
- 32 ms/256 refresh cycles
- $\overline{RAS}$-Only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden refresh capability
- Standard 16-pin Plastic DIP (Suffix: -P)
- Standard 18-pin Plastic LCC (Suffix: -PD)

PIN ASSIGNMENT





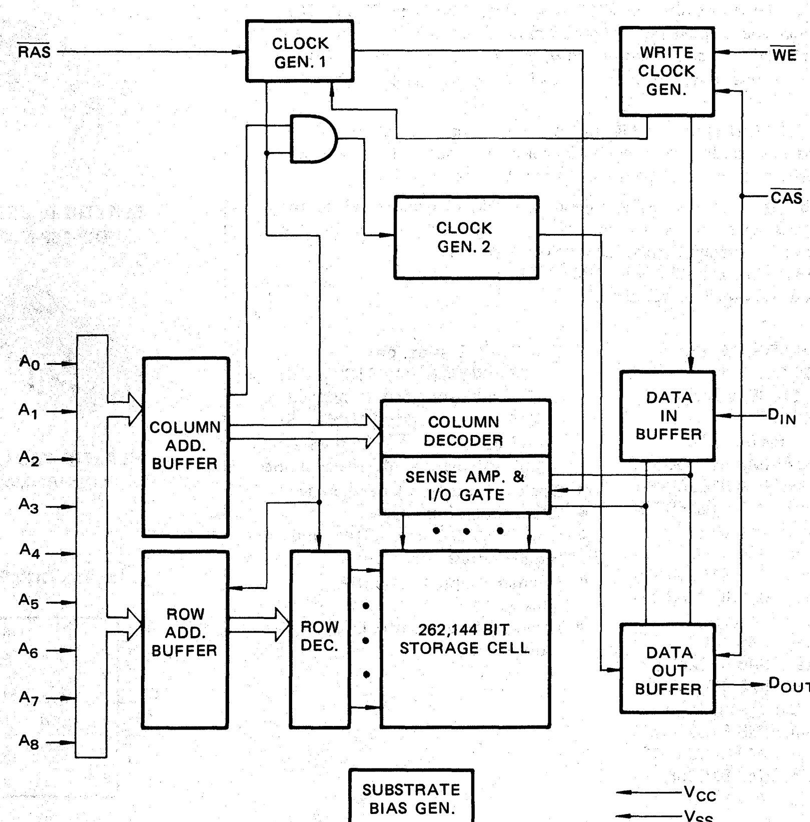
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-1 to +7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit output current		50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_8 and D_{IN}	C_{IN1}	—	7	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	10	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	7	pF

2

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input High Voltage, all inputs	V_{IH}	2.4	–	6.5	V	
Input Low Voltage, all inputs	V_{IL}	-1.0	–	0.8	V	

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

Parameter		Conditions	Symbol	Values		Unit
				Min	Max	
Operating Current* (Average power supply current)	MB81C258-10	$\overline{CAS}$ = V_{IL} or V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	I_{CC1}	–	60	mA
	MB81C258-12			–	50	
	MB81C258-15			–	45	
Standby Current (Power supply current)	TTL level	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	I_{CC2}	–	2.0	mA
	CMOS level	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC}-0.2V		–	0.3	
Static Mode Current*	MB81C258-10	$\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, $\overline{RAS}$ cycling; t_{SC} = min.	I_{CC3}	–	40	mA
	MB81C258-12			–	35	
	MB81C258-15			–	30	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current* (Average power current)	MB81C258-10	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	I_{CC4}	–	55	mA
	MB81C258-12			–	45	
	MB81C258-15			–	40	
Input Leakage Current		0V ≦ V_{IN} ≦ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V; pins not under test = 0V	$I_{I(L)}$	-10	10	μA
Output Leakage Current		0V ≦ V_{OUT} ≦ 5.5V; Data out disabled	$I_{O(L)}$	-10	10	
Output High Voltage		I_{OH} = -5mA	V_{OH}	2.4	–	V
Output Low Voltage		I_{OL} = 4.2mA	V_{OL}	–	0.4	

NOTE: *; I_{CC} depends on the output load operating speed. The specified values are with the output pin open.

AC CHARACTERISTICS

(At Recommended operating conditions unless otherwise noted) Notes 1, 2

Parameter	NOTES	Symbol	MB 81C258-10		MB 81C258-12		MB 81C258-15		Unit
			Min	Max	Min	Max	Min	Max	
Time Between Refresh		t_{REF}	–	32	–	32	–	32	ms
Random Read/Write Cycle Time		t_{RC}	200	–	230	–	260	–	ns
Read-Modify-Write Cycle Time		t_{RWC}	245	–	285	–	325	–	ns
Access Time from $\overline{RAS}$	3 5	t_{RAC}	–	100	–	120	–	150	ns
Access Time from $\overline{CAS}$		t_{CAC}	–	25	–	30	–	35	ns
Output Buffer Turn off Delay Time		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
Column Address Access Time	4 5	t_{AA}	–	45	–	55	–	70	ns
Output Hold Time from Column Address Change		t_{AOH}	5	–	5	–	5	–	ns
Access Time from $\overline{WE}$ Precharge		t_{WPA}	–	25	–	30	–	35	ns
Access Time Relative to last Write	6	t_{ALW}	–	90	–	110	–	140	ns
Write Latched Data Hold Time		t_{WOH}	0	–	0	–	0	–	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90	–	100	–	100	–	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	65	100000	75	100000	95	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	25	–	30	–	35		ns
$\overline{CAS}$ Pulse Width (Read)		t_{CAS}	25	100000	30	100000	35	100000	ns
$\overline{CAS}$ Pulse Width (Write)		t_{CAS}	15	100000	20	100000	25	100000	ns
$\overline{CAS}$ Hold Time (Read)		t_{CSH}	100	–	120	–	150	–	ns
$\overline{CAS}$ Hold Time (Write)		t_{CSH}	80	–	95	–	115	–	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	25	75	25	90	30	115	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	20	–	25	–	30	–	ns
Row Address Set Up Time		t_{ASR}	0	–	0	–	0	–	ns
Row Address Hold Time		t_{RAH}	15	–	15	–	20	–	ns
Column Address Set Up Time	7	t_{ASC}	0	–	0	–	0	–	ns
Column Address Hold Time	7	t_{CAH}	20	–	25	–	30	–	ns
$\overline{RAS}$ to Column Address Delay Time	8 9	t_{RAD}	20	55	20	65	25	80	ns
Column Address Hold Time Reference to $\overline{RAS}$		t_{AR}	100	–	120	–	150	–	ns
Write Address Hold Time Referenced to $\overline{RAS}$		t_{AWR}	80	–	90	–	110	–	ns
Read Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	–	55	–	70	–	ns
Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time	10	t_{AHR}	15	–	15	–	20	–	ns

2

AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) Notes 1, 2

Parameter NOTES	Symbol	MB 81C258-10		MB 81C258-12		MB 81C258-15		Unit
		Min	Max	Min	Max	Min	Max	
Last Write to Column Address Delay Time 11 12	t_{LWAD}	20	45	20	55	25	70	ns
Column Address Hold Time Referenced to Last Write	t_{AHLW}	90	–	110	–	140	–	ns
Read Command Set Up Time Referenced to $\overline{CAS}$	t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time Referenced to $\overline{RAS}$ 13	t_{RRH}	10	–	10	–	10	–	ns
Read Command Hold Time Referenced to $\overline{CAS}$ 13	t_{RCH}	0	–	0	–	0	–	ns
$\overline{WE}$ Pulse Width	t_{WP}	15	–	20	–	25	–	ns
$\overline{WE}$ Inactive Time	t_{WI}	15	–	20	–	25	–	ns
Write Command Hold Time	t_{WCH}	15	–	20	–	25	–	ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	–	30	–	35	–	ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	–	30	–	35	–	ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time 14	t_{RWD}	100	–	120	–	150	–	ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	–	30	–	35	–	ns
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	45	–	55	–	70	–	ns
$\overline{RAS}$ to Second Write Delay Time	t_{RSWD}	105	–	125	–	155	–	ns
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	80	–	95	–	115	–	ns
$\overline{RAS}$ Precharge Time from Last Write	t_{RPLW}	135	–	155	–	165	–	ns
Write Set Up Time for Output Disable 14	t_{WS}	0	–	0	–	0	–	ns
Write Hold Time for Output Disable 14	t_{WH}	0	–	0	–	0	–	ns
D_{IN} Set Up Time	t_{DS}	0	–	0	–	0	–	ns
D_{IN} Hold Time	t_{DH}	20	–	25	–	30	–	ns
D_{IN} Hold Time Reference to $\overline{RAS}$	t_{DHR}	80	–	90	–	110	–	ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCS}	20	–	25	–	30	–	ns

2

AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) Notes 1, 2

Parameter	NOTES	Symbol	MB 81C258-10		MB 81C258-12		MB 81C258-15		Unit
			Min	Max	Min	Max	Min	Max	
Refresh Hold Time for CAS Referenced to RAS (CAS-before-RAS cycle)		t_{FCH}	20	–	25	–	30	–	ns
CAS Precharge Time (CAS-before-RAS cycle)		t_{CPR}	20	–	25	–	30	–	ns
RAS Precharge Time to CAS Active Time (Refresh cycles)		t_{RPC}	20	–	20	–	20	–	ns
Static Mode Read/Write Cycle Time		t_{SC}	50	–	60	–	75	–	ns
Static Mode Read-Modify-Write Cycle Time		t_{SRWC}	95	–	115	–	145	–	ns
Static Mode CAS Precharge Time		t_{CP}	15	–	20	–	25	–	ns
Refresh Counter Test Cycle Time	15	t_{RTC}	440	–	520	–	610	–	ns
Refresh Counter Test RAS Pulse Width	15	t_{TRAS}	340	10000	410	10000	500	10000	ns
Refresh Counter Test CAS Precharge Time	15	t_{CPT}	50	–	60	–	70	–	ns
Refresh Counter Test CAS to Col. Address Delay Time	15	t_{CADT}	–	100	–	120	–	150	ns
Refresh Counter Test Access Time from CAS	15	t_{CACT}	–	135	–	165	–	205	ns
Refresh Counter Test CAS to WE Delay Time	15	t_{CWDT}	135	–	165	–	205	–	ns

NOTES:

1 An Initial pause (RAS = CAS = V_{IH}) of 200 µs is required after power-up followed by any 8 RAS-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.

2 AC characteristics assume t_T = 5ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8V, V_{OH} = 2.4V, and V_{OL} = 0.4V.

3 Assumes that $t_{RAD} \leq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.

4 Assumes that $t_{RAD} \geq t_{RAD}$ (max).

5 Measured with a load equivalent to 2 TTL loads and 100pF.

6 Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.

7 Write Cycle Only.

8 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

9 t_{RAD} (min) = t_{RAH} (min) + t_T (t_T = 5ns)

10 t_{AHR} is specified to latch column address by the rising edge of RAS.

11 Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.

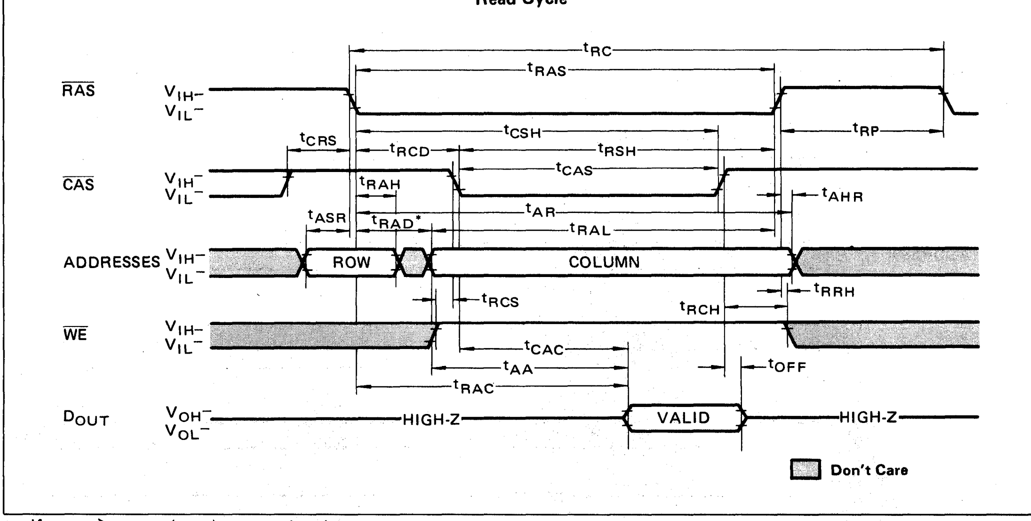
12 t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T = 5ns).

13 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

14 t_{WS}, t_{WH}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. It $t_{RWD} \geq t_{RWD}$ (min), The data output will contain data read from the selected cell.

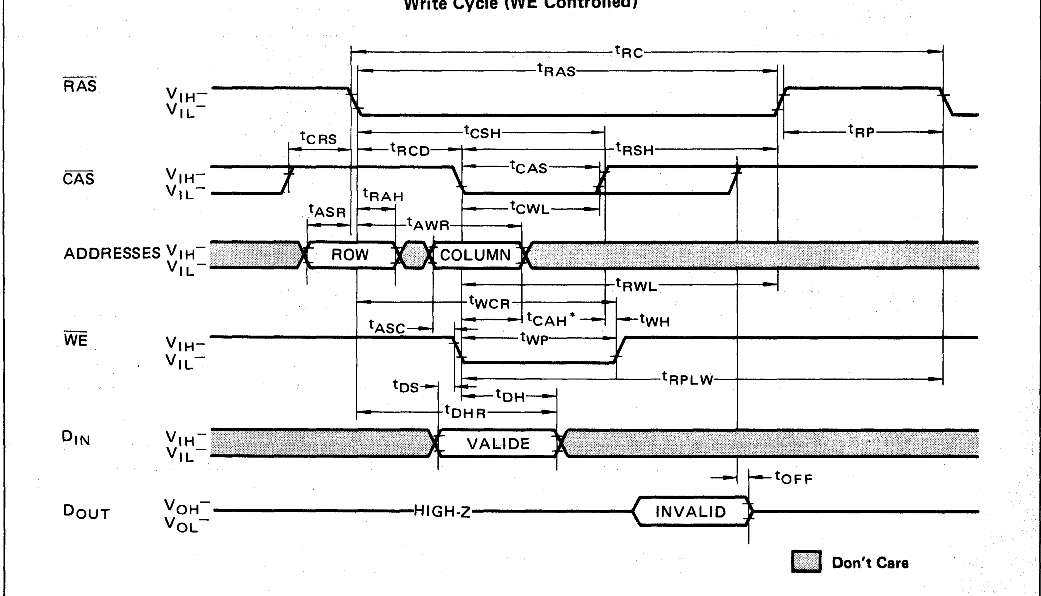
15 CAS-before-RAS refresh counter test cycle only.

Read Cycle



*; If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA}.

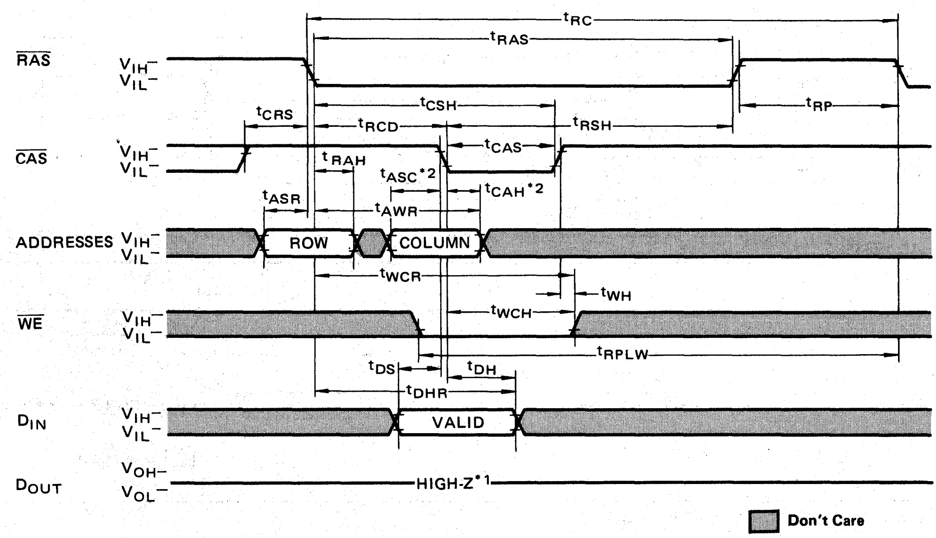
Write Cycle (WE Controlled)



*; Write Cycle only.

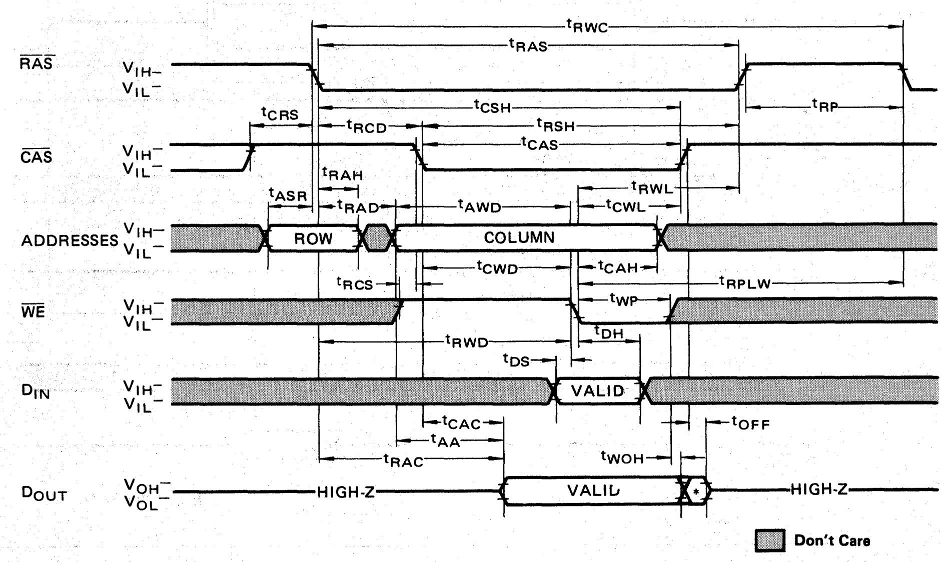
2

Write Cycle ($\overline{CAS}$ Controlled)



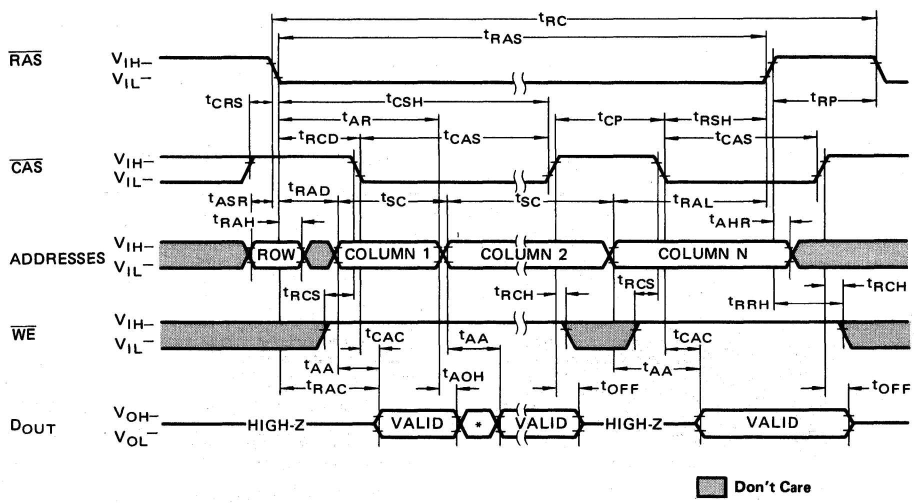
*1; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.
*2; Write Cycle only.

Read-Modify-Write Cycle



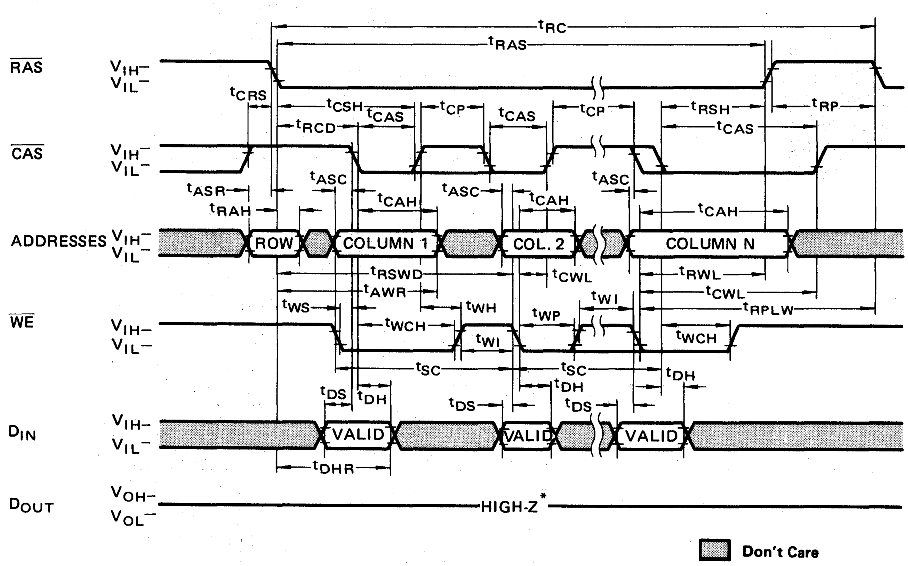
*; Invalid Data

Static Mode Read Cycle



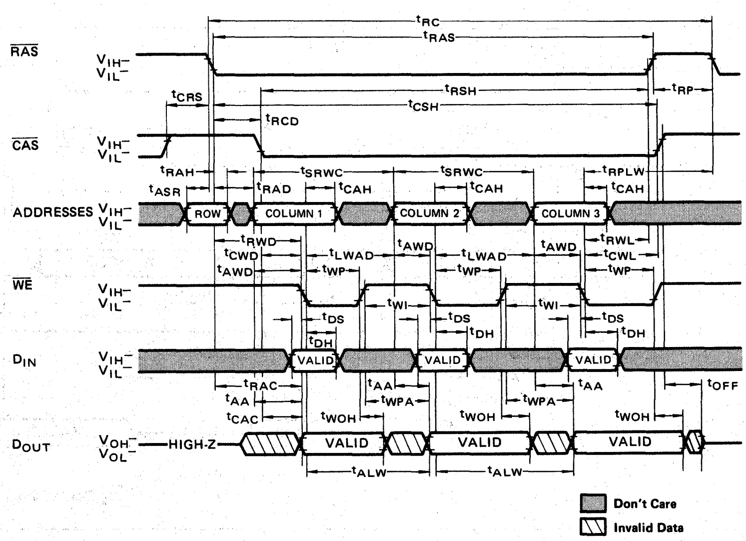
*; Invalid Data.

Static Mode Write Cycle

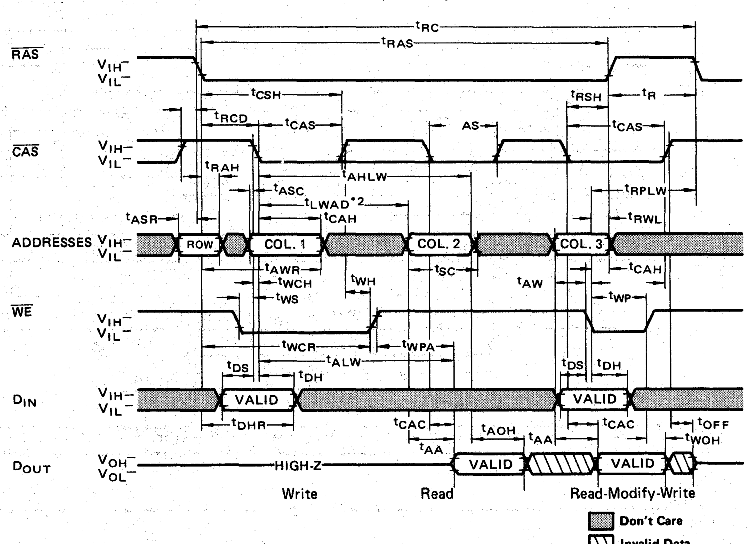


*; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.

Static Mode Read-Modify-Write



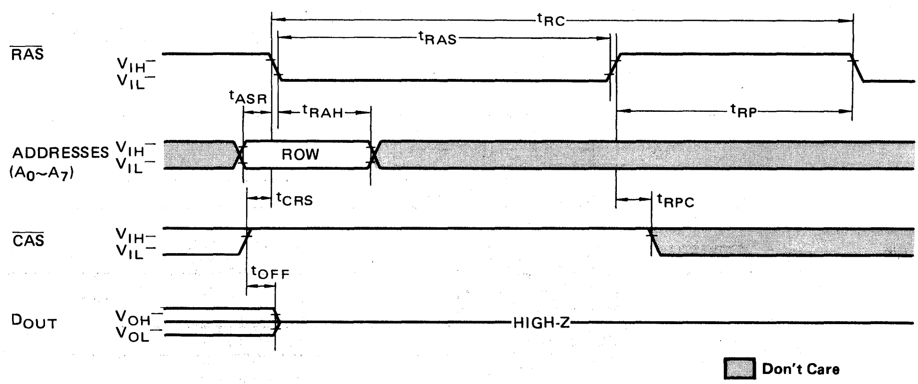
Static Mode Mixed Cycle[*1]



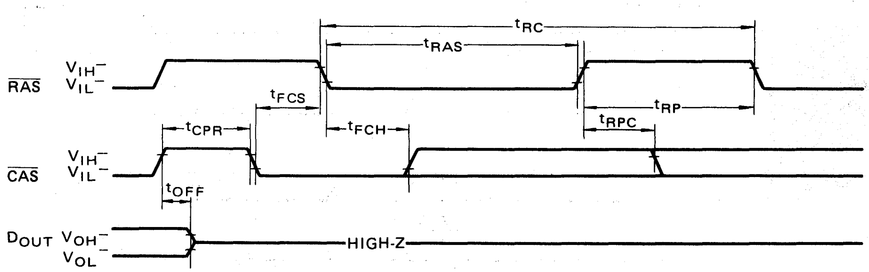
*1; This is an example of static mode mixed cycle.
*2; If t_{LWAD} is satisfied its min/max value, $t_{ALW} = t_{SC}$ (min) + t_{AA} (max)

2

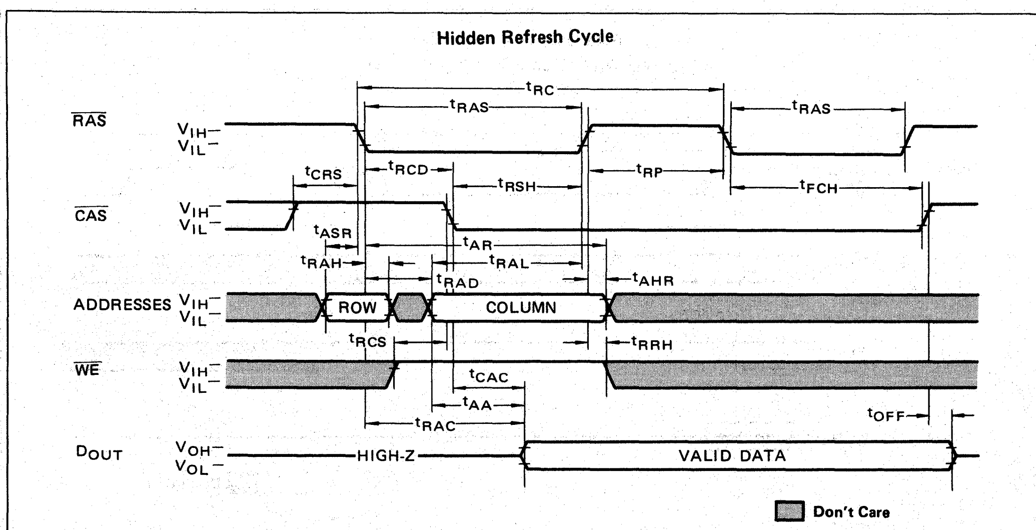
$\overline{RAS}$-Only Refresh Cycle
(Note; $\overline{WE}$, D_{IN} = Don't Care, A_8 = V_{IH} or V_{IL})

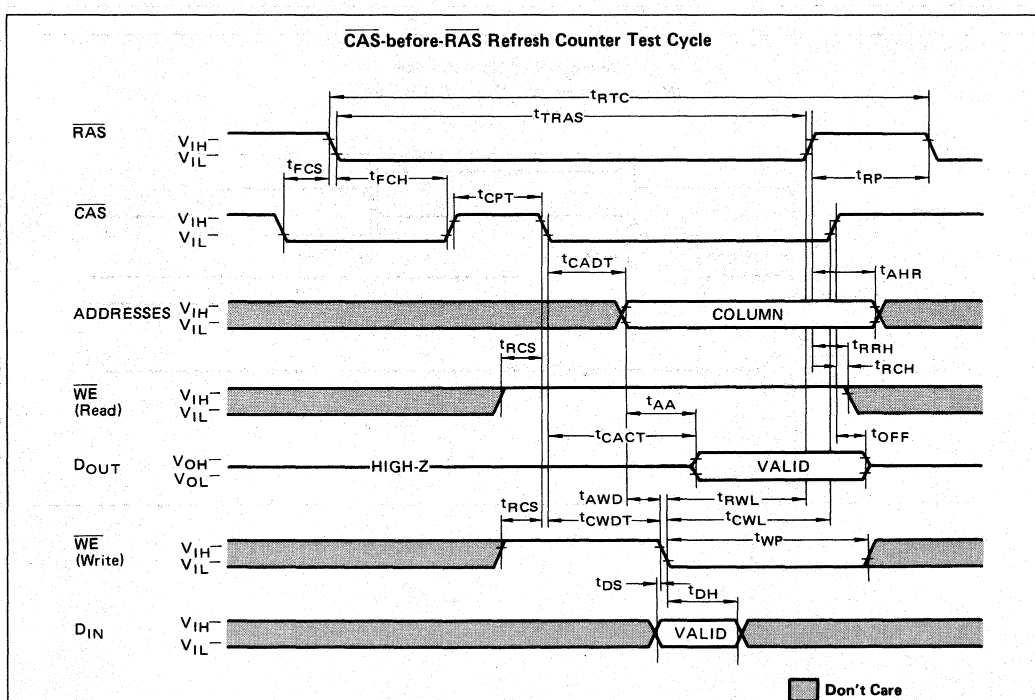


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle
(Note; Address, $\overline{WE}$, D_{IN} = Don't Care)



2


Hidden Refresh Cycle
RAS
CAS
ADDRESSES
WE
DOUT
ROW
COLUMN
HIGH-Z
VALID DATA
Don't Care


CAS-before-RAS Refresh Counter Test Cycle
RAS
CAS
ADDRESSES
WE (Read)
DOUT
WE (Write)
DIN
COLUMN
HIGH-Z
VALID
Don't Care

DESCRIPTION

Address Inputs:
A total of eighteen binary input address bits are required to decode any one of the 262,144 storage cells within the MB 81C258. Nine row address bits are established on the address input pins (A_0 to A_8) and latched with the Row Address Strobe (RAS). The nine column address bits are established on the address input pins (A_0 to A_8) after the Row Address Hold Time has been satisfied. In read cycle, the column address are not latched by the Column Address Strobe (CAS), so the column address must be stable until the output becomes valid. In write cycle, the column addresses are latched by the later falling edge of CAS or WE.

Write Enable:
Read or Write cycle is selected with the WE inputs. A high on WE selects read cycle and low selects write cycle. The write operation is asserted on the later falling edge of CAS or WE (Both CAS and WE are low). The time period of the write operation is determined by internal circuit, thus next write operation will be inhibited during the write operation.

Data Input:
Data is written into the MB 81C258 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of CAS or WE.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is in high impedance state until CAS is brought low. In a read cycle, the access time is determined by the following conditions:
1. t_{RAC} from the falling edge of RAS.
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of CAS.

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC}=t_{RCD}+t_{CAC}$ or $t_{RAC}=t_{RAD}+t_{AA}$.
Data output remains valid while the column address inputs are kept constant. However, when CAS goes high, the output returns to high impedance state. In the static mode, the output data is internally latched by the later falling edge of CAS or WE and remains valid internally until either returns to high.

Static Mode:
The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, CAS can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.
1. Static mode read cycle;
   In a static mode read cycle, the access time is t_{RAC} from the falling edge of RAS or t_{AA} from the column address input. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle,
   In a static mode write cycle, the data is written into the cell triggered by the later falling edge of CAS or WE. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle.
3. Static mode read-modify-write cycle;
   In the static mode read-modify-write cycle, WE goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of CAS. The data and column address inputs are strobed and latched by the falling edge a of WE.
4. Static mode mixed cycle,
   In the static mode, read, write, and read-modify-write cycles can be mixed in any order.

In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.
1. t_{ALW} from the falling edge of WE at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of WE at the read cycle.
4. t_{CAC} from the falling edge of CAS.

Refresh:
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7) at least every 4ms.

The MB 81C258 offers the following three types of refresh.
1. RAS only refresh;
   The RAS-only refresh avoids any output during refresh because the output buffer is high impedance state due to CAS high. Strobing of each 256 row address (A_0 to A_7) with RAS will cause all bits in each row to be refreshed. During RAS-only refresh cycle, (either V_{IH} or V_{IL}) is permitted to A_8.
2. CAS-before-RAS refresh;
   CAS-before-RAS refreshing available on the MB 81C258 offers an alternate refresh method. If CAS is held low for the specified period (t_{FCS}) before RAS goes low, on chip refresh control clock generator and the internal refresh address counter are enabled, and an internal refresh operation is executed. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next CAS-before-RAS refresh.
3. Hidden refresh;
   A hidden refresh cycle will be executed while maintaining latest valid data at the output pin by extending the CAS low time. For the MB 81C258, a hidden refresh cycle is CAS-before-RAS refresh. The internal refresh address counter provides the refresh address, as in a normal CAS-before-RAS refresh cycle.

CAS-before-RAS refresh counter Test:
A special timing sequence using CAS-before-RAS refresh counter test cycle provides a convenient method of verifying the function of CAS-before-RAS refresh activated circuitry. After the CAS-before -RAS refresh cycle, if CAS goes to high and goes to low again while RAS is held low, the read and read-modify-write cycles are enabled according to the state of WE. This is shown in the CAS-before-RAS counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed is shown below.
ROW ADDRESS — Bits A_0 to A_7 are provided by the refresh counter. The

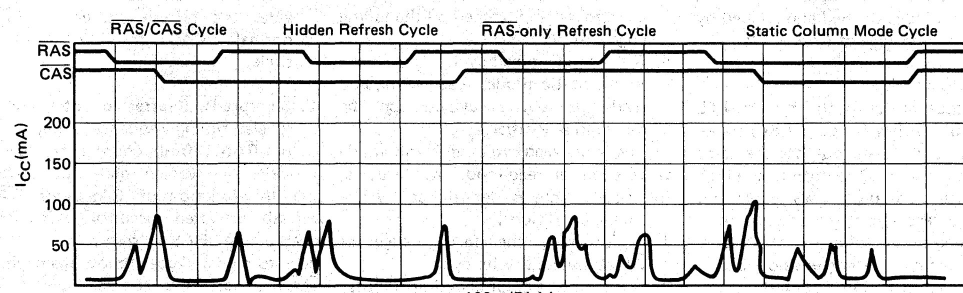
bits A_8 is set high internally.

COLUMN ADDRESS – All the bits A_0 to A_8 are provided by externally after t_{CADT}.

The recommended procedure of $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle is shown below. The timing of $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle should be used.

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Using a write cycle, write 0s to all 256 row addresses.
4) Using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle in read-modify-write mode, read the 0 written in step 3), and simultaneously write a 1 to the same cell. This step is repeated 256 row address generated by internal refresh address counter.
5) Using a normal read cycle, read back the 1s written in step 4), from all 256 locations.
6) Complement the test pattern and repeat step 3), 4), and 5).

Fig. 2 — CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 — NORMALIZED ACCESS TIME (t_{RAC}) vs SUPPLY VOLTAGE

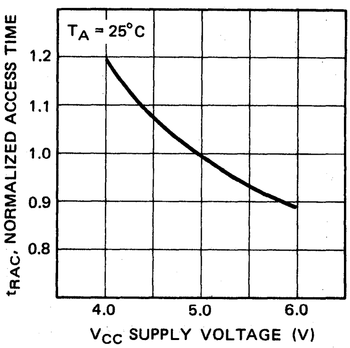


Fig. 4 — NORMALIZED ACCESS TIME (t_{RAC}) vs AMBIENT TEMPERATURE

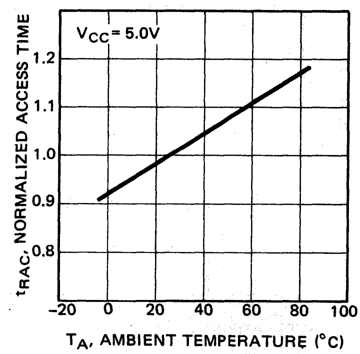


Fig. 5 — NORMALIZED ACCESS TIME (t_{AA}) vs SUPPLY VOLTAGE

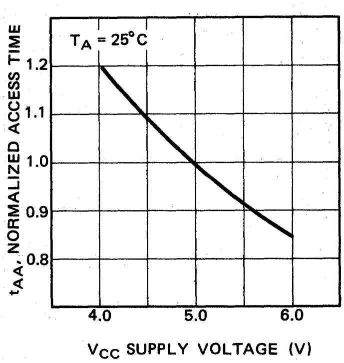


Fig. 6 — NORMALIZED ACCESS TIME (t_{AA}) vs AMBIENT TEMPERATURE

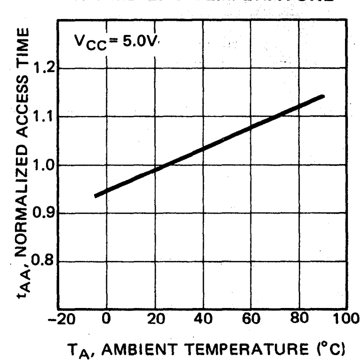


Fig. 7 — OPERATING CURRENT vs CYCLE RATE

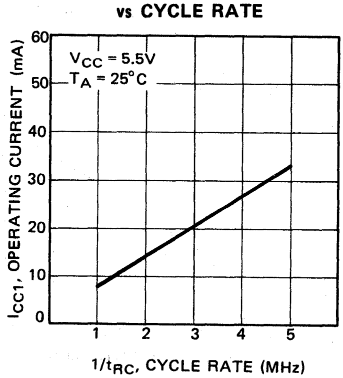


Fig. 8 — OPERATING CURRENT vs SUPPLY VOLTAGE

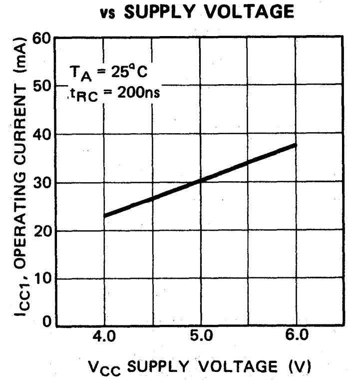


Fig. 9 – OPERATING CURRENT vs AMBIENT TEMPERATURE

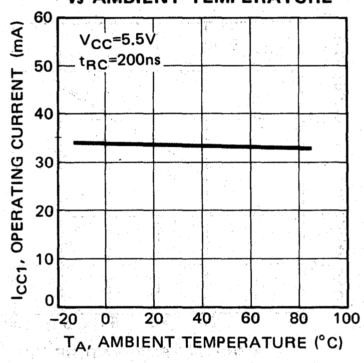


Fig. 10 – TTL STANDBY CURRENT vs SUPPLY VOLTAGE

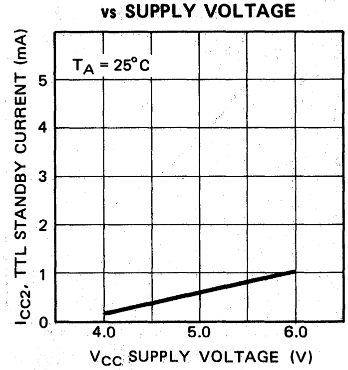


Fig. 11 – CMOS STANDBY CURRENT vs SUPPLY VOLTAGE

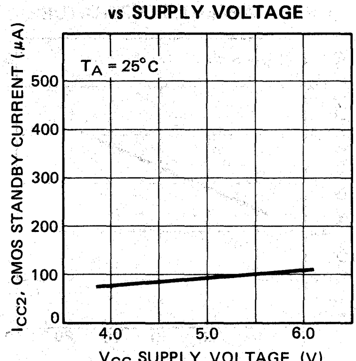


Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

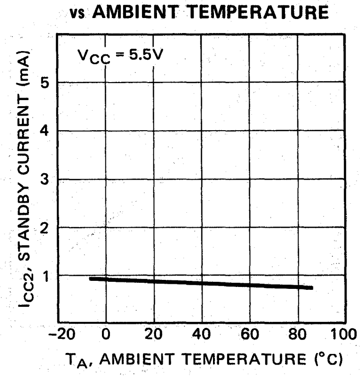


Fig. 13 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

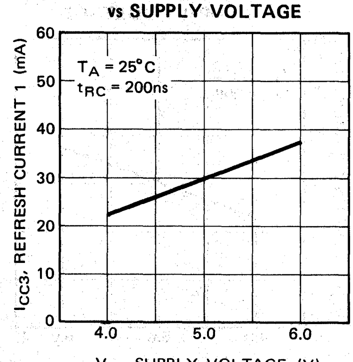


Fig. 14 – REFRESH CURRENT 1 vs CYCLE RATE

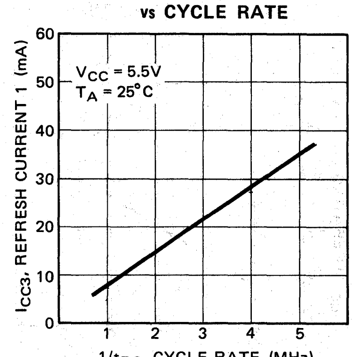


Fig. 15 – STATIC COLUMN MODE CURRENT vs CYCLE RATE

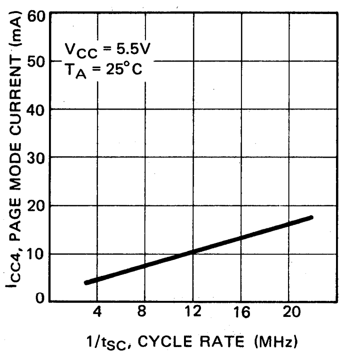


Fig. 16 – STATIC COLUMN MODE CURRENT vs SUPPLY VOLTAGE

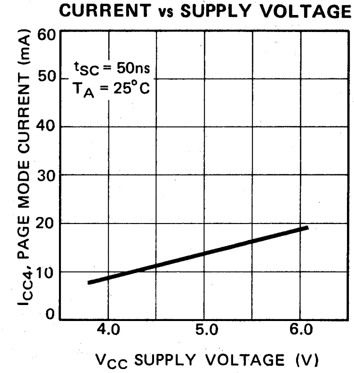


Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

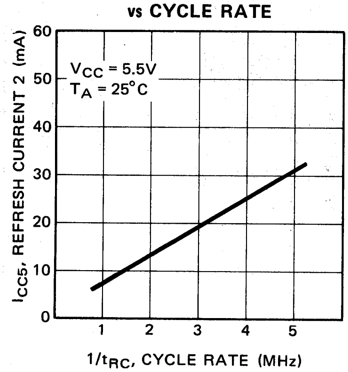


Fig. 18 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

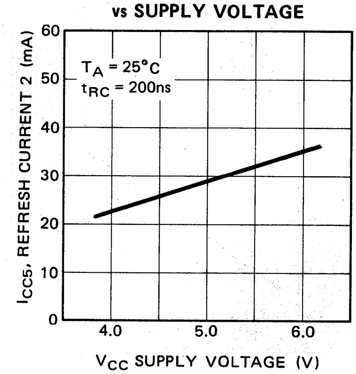


Fig. 19 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

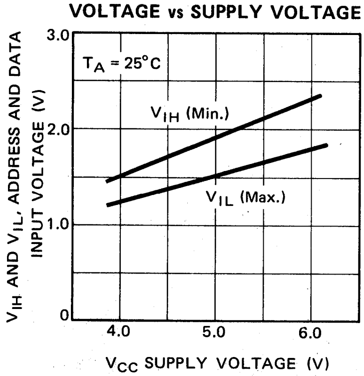
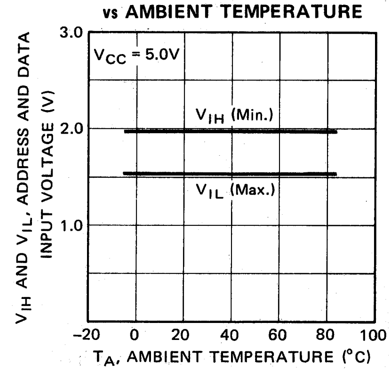


Fig. 20 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



2

Fig. 21 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

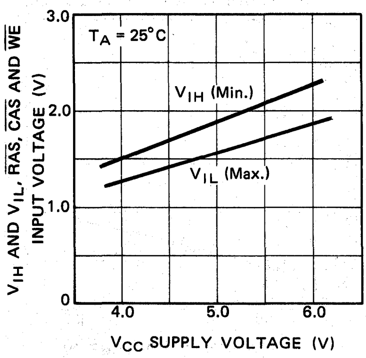


Fig. 22 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

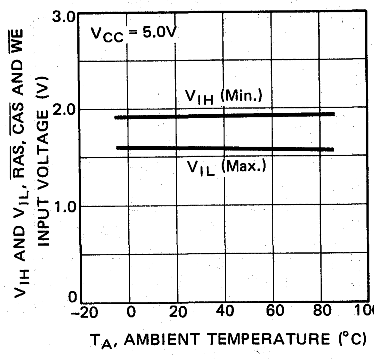


Fig. 23 – ACCESS TIME (t_{RAC}) vs LOAD CAPACITANCE

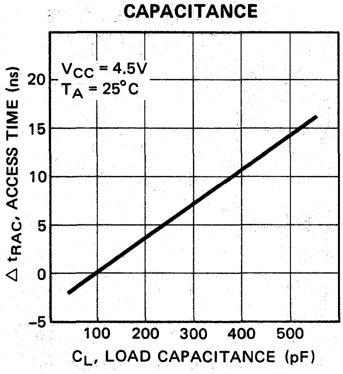


Fig. 24 – ACCESS TIME (t_{AA}) vs LOAD CAPACITANCE

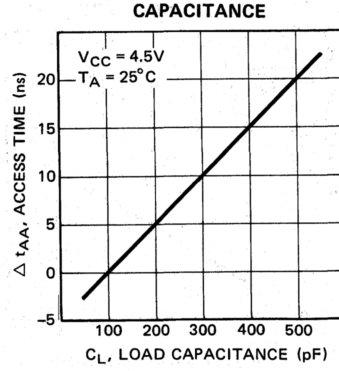


Fig. 25 – OUTPUT CURRENT vs OUTPUT VOLTAGE

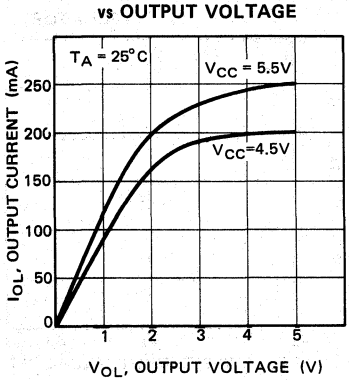


Fig. 26 – OUTPUT CURRENT vs OUTPUT VOLTAGE

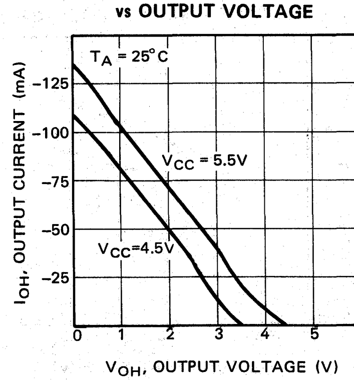


Fig. 27 — CURRENT WAVEFORM DURING POWER UP (1)

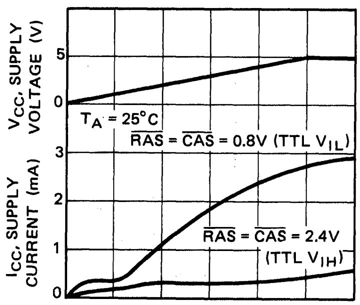
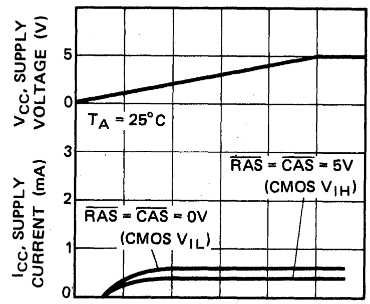


Fig. 28 — CURRENT WAVEFORM DURING POWER UP (2)



FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data	
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output
Standby	H	H	X	X	X	X	High-Z
Read Cycle	L	L	H	Valid	Valid	X	Valid
Write Cycle	L	L	L	Valid	Valid	Valid	High-Z*1
Static Mode Read Cycle	L	L	H	Valid*2	Valid	X	Valid
Static Mode Write Cycle	L	L	L	Valid*2	Valid	Valid	High-Z*1
Static Mode Mixed Cycle	L	L	L/H	Valid*2	Valid	Valid	High-Z or Valid
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	X	X	High-Z

X: Don't Care H: High level L: Low level

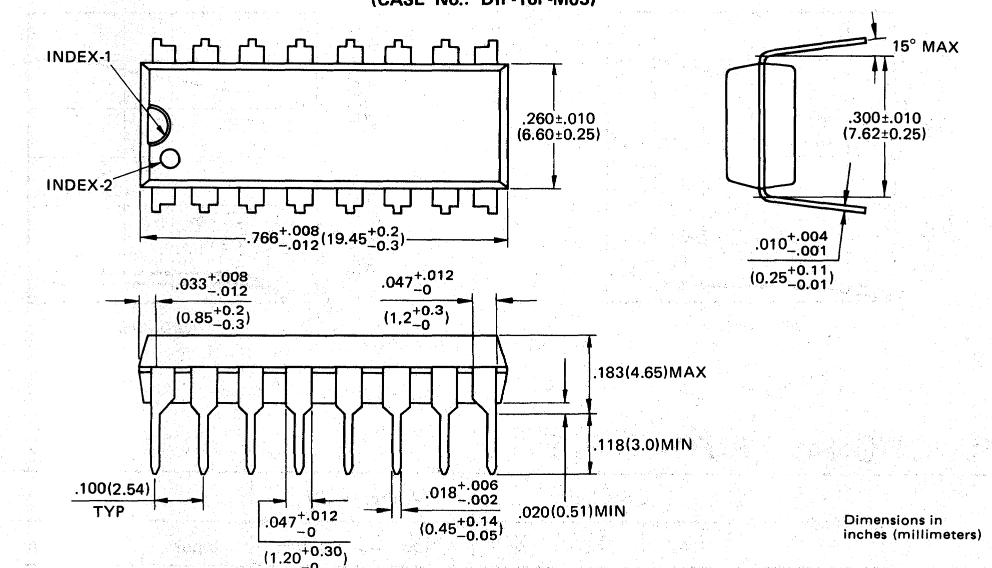
Note: *1: If $t_{WS} < t_{WS(min)}$ and $t_{WH} < t_{WH(min)}$, the data output become invalid.
*2: After first cycle, row address is not necessary.

2

PACKAGE DIMENSIONS

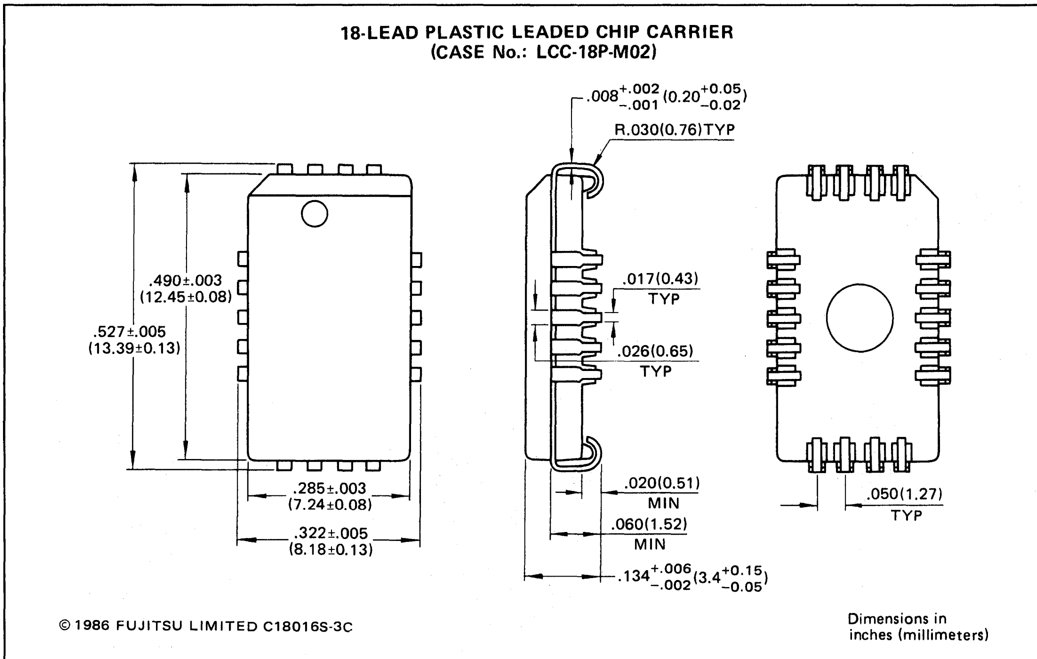
(Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



PACKAGE DIMENSIONS

(Suffix: -PD)



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262144 BIT CMOS STATIC COLUMN DYNAMIC RAM

MB 81C466-10
MB 81C466-12
MB 81C466-15

March 1987
Edition 2.0

65,536 x 4 BIT CMOS STATIC COLUMN DYNAMIC RANDOM ACCESS MEMORY

The Fujitsu MB 81C466 is static column dynamic random access memory, SC-DRAM, which is organized as 65536 word by 4 bits. This SC-DRAM is designed for high speed, high performance applications such as main frame memory, buffer memory, and video memory, and for applications to battery backed-up systems where very low power dissipation and compact layout is required.

The advantage of SC-DRAM is achieving the static mode operation such as read, write and read-modify-write cycles in spite of dynamic RAM and the fast read and write operation can be performed by this mode.

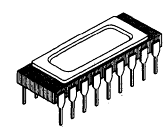
The MB 81C466 is fabricated using silicon gate CMOS process. Since the CMOS circuit dissipates very small power, it can be easily used in battery backed-up application system such as hand held computer.
The MB 81C466 is pin compatible with Intel's 51C259.
All inputs and outputs are TTL compatible.

- 65536 x 4 SC-DRAM, 18-pin DIP/ 20-pin ZIP
- Silicon-gate, CMOS, single transistor cell
- Row Access Time (t_{RAC}),
  100 ns max. (MB 81C466-10)
  120 ns max. (MB 81C466-12)
  150 ns max. (MB 81C466-15)
- Random Cycle Time (t_{RC}),
  200 ns min. (MB 81C466-10)
  230 ns min. (MB 81C466-12)
  260 ns min. (MB 81C466-15)
- Address Access Time (t_{AA}),
  45 ns max. (MB 81C466-10)
  55 ns max. (MB 81C466-12)
  70 ns max. (MB 81C466-15)
- Static Mode Cycle Time (t_{SC}),
  50 ns min. (MB 81C466-10)
  60 ns min. (MB 81C466-12)
  75 ns min. (MB 81C466-15)
- Low Power Dissipation
  385 mW max. (MB 81C466-10)
  330 mW max. (MB 81C466-12)
  275 mW max. (MB 81C466-15)
  11 mW max. at standby with TTL level input
  1.65 mW max. at standby with CMOS level input
- Single 5V supply ±10% tolerance
- Internal write period control
- On chip latches for address and data inputs
- 32ms/256 refresh cycle
- $\overline{RAS}$-Only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden refresh capability
- Standard 18-pin ceramic (Metal seal) DIP (Suffix: -C)
- Standard 18-pin Plastic DIP (Suffix: -P)
- Standard 20-Pin Plastic ZIP (Suffix: -PSZ)

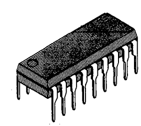
ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} relative to V_{SS}		V_{CC}	−1 to +7	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit output current			50	mA

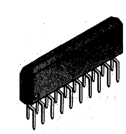
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



CERAMIC PACKAGE
DIP-18C-A01

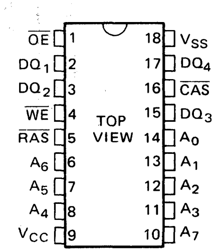


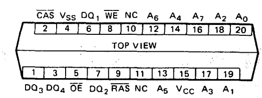
PLASTIC PACKAGE
DIP-18P-M01



PLASTIC PACKAGE
ZIP-20P-M01

PIN ASSIGNMENT





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application cf any voltage higher than maximum rated voltages to this high impedance circuit.

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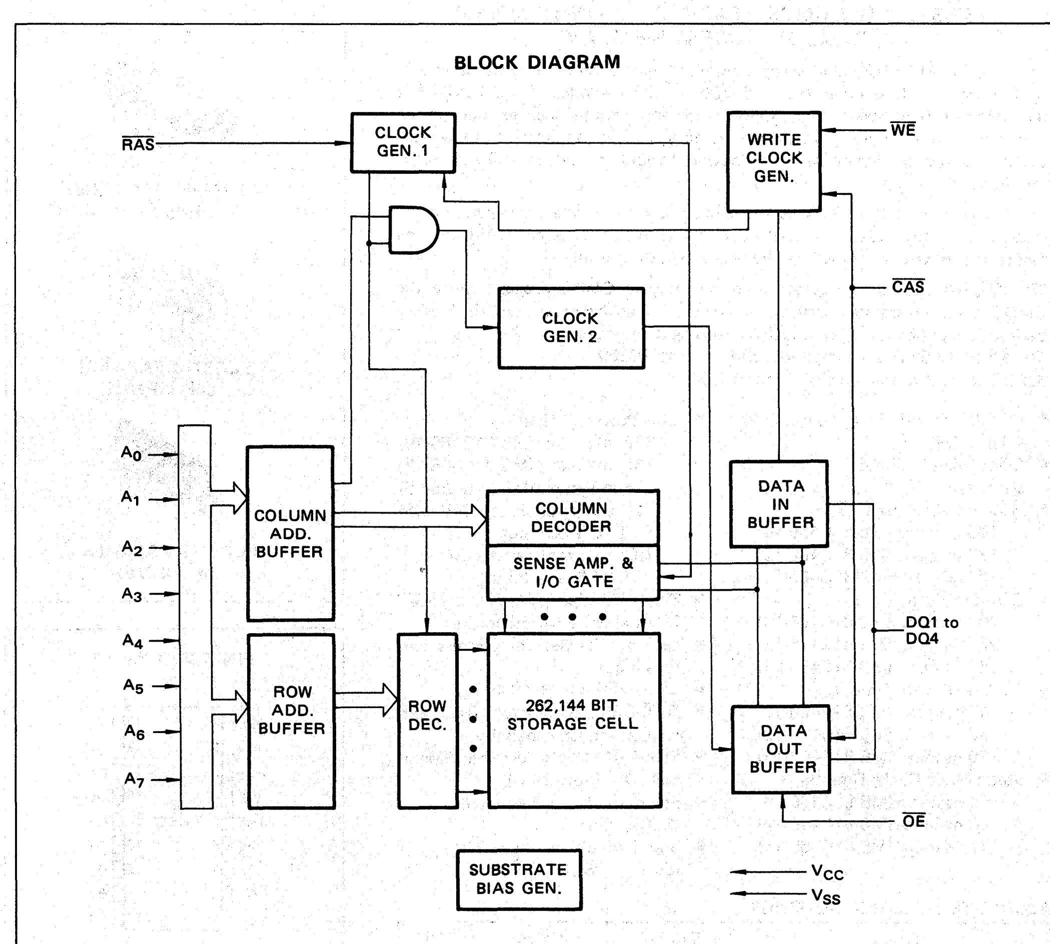

CAPACITANCE (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_7	C_{IN1}		7	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}		10	pF
Input/Output Capacitance, DQ_1 to DQ4	C_{IO}		7	pF

2

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IN}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING/REFRESH CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81C466-10	I_{CC1}			70	mA
	MB 81C466-12				60	
	MB 81C466-15				50	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	TTL Level	I_{CC2}			2	mA
	CMOS Level				0.3	
STATIC MODE OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, $\overline{WE}$ or Address = cycling; t_{SC} = min)	MB 81C466-10	I_{CC3}			50	mA
	MB 81C466-12				40	
	MB 81C466-15				35	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81C466-10	I_{CC4}			65	mA
	MB 81C466-12				55	
	MB 81C466-15				45	
INPUT LEAKAGE CURRENT, ALL INPUTS (V_{IN} = 0V to 5.5V, V_{CC} = 5V, V_{SS} = 0V, all other inputs not under test = 0V)		$I_{I(L)}$	−10		10	μA
INPUT/OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{DQ(L)}$	−10		10	μA
OUTPUT LEVEL, OUTPUT LOW VOLTAGE (I_{OL} = 4.2mA)		V_{OL}			0.4	V
OUTPUT LEVEL, OUTPUT HIGH VOLTAGE (I_{OH} = −5.0 mA)		V_{OH}	2.4			V

NOTE *; I_{CC} is depended on the output loading and cycle rate. The specified values are obtained with the output open.

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AC CHARACTERISTICS

(At Recommended operating conditions unless otherwise noted) NOTE 1,2

Parameter	NOTE	Symbol	MB 81C466-10 Min	MB 81C466-10 Max	MB 81C466-12 Min	MB 81C466-12 Max	MB 81C466-15 Min	MB 81C466-15 Max	Unit
Time Between Refresh		t_{REF}		32		32		32	ms
Random Read/Write Cycle Time		t_{RC}	200		230		260		ns
Read-Modify-Write Cycle Time		t_{RWC}	270		315		360		ns
Access Time from $\overline{RAS}$	3 5	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5	t_{CAC}		25		30		35	ns
Output Buffer Turn off Delay Time		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
Column Address Access Time	5	t_{AA}		45		55		70	ns
Output Hold Time from Column Address Change		t_{AOH}	5		5		5		ns
Access Time from $\overline{WE}$ Precharge		t_{WPA}		25		30		35	ns
Access Time Relative to Last Write	6	t_{ALW}		90		110		140	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90		100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	65	100000	75	100000	95	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	25		30		35		ns
$\overline{CAS}$ Pulse Width (Read)		t_{CAS}	25	100000	30	100000	35	100000	ns
$\overline{CAS}$ Pulse Width (Write)		t_{CAS}	15	100000	20	100000	25	100000	ns
$\overline{CAS}$ Hold Time (Read)		t_{CSH}	100		120		150		ns
$\overline{CAS}$ Hold Time (Write)		t_{CSH}	80		95		115		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	25	75	25	90	30	115	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	20		25		30		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	15		15		20		ns
Column Address Set Up Time	7	t_{ASC}	0		0		0		ns
Column Address Hold Time	7	t_{CAH}	20		25		30		ns
$\overline{RAS}$ to Column Address Delay Time	8 9	t_{RAD}	20	55	20	65	25	80	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	100		120		150		ns
Write Address Hold Time Referenced to $\overline{RAS}$		t_{AWR}	80		90		110		ns
Read Address to $\overline{RAS}$ Lead Time		t_{RAL}	45		55		70		ns
Column Address Hold Time Reference to $\overline{RAS}$ Rising Time	10	t_{AHR}	15		15		20		ns
Last Write to Column Address Delay Time	11 12	t_{LWAD}	20	45	20	55	25	70	ns
Column Address Hold Time Reference to Last Write		t_{AHLW}	90		110		140		ns

AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) NOTE 1,2

Parameter NOTE	Symbol	MB 81C466-10		MB 81C466-12		MB 81C466-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Command Set Up Time Referenced to $\overline{\text{CAS}}$	t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{\text{RAS}}$ [13]	t_{RRH}	10		10		10		ns
Read Command Hold Time Referenced to $\overline{\text{CAS}}$ [13]	t_{RCH}	0		0		0		ns
$\overline{\text{WE}}$ Pulse Width	t_{WP}	15		20		25		ns
$\overline{\text{WE}}$ Inactive Time	t_{WI}	15		20		25		ns
Write Command Hold Time	t_{WCH}	15		20		25		ns
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	25		30		35		ns
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	25		30		35		ns
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time [14]	t_{RWD}	125		150		185		ns
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{CWD}	50		60		70		ns
Column Address to $\overline{\text{WE}}$ Delay Time	t_{AWD}	70		85		100		ns
$\overline{\text{RAS}}$ to Second Write Delay Time	t_{RSWD}	105		125		155		ns
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{WCR}	80		95		115		ns
$\overline{\text{RAS}}$ Precharge Time from Last Write	t_{RPLW}	135		155		165		ns
Write Set Up Time for Output Disable [14]	t_{WS}	0		0		0		ns
Write Hold Time for Output Disable [14]	t_{WH}	0		0		0		ns
D_{IN} Set Up Time	t_{DS}	0		0		0		ns
D_{IN} Hold Time	t_{DH}	20		25		30		ns
D_{IN} Hold Time Referenced to $\overline{\text{RAS}}$	t_{DHR}	80		90		110		ns
Access Time from $\overline{\text{OE}}$	t_{OEA}		25		30		35	ns
OE to Data In Delay Time	t_{OED}	20		25		30		ns
Output Buffer Turn off Delay Time from $\overline{\text{OE}}$	t_{OEZ}	0	20	0	25	0	30	ns
$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{RAS}}$ [15]	t_{OEHR}	20		20		20		ns
$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{CAS}}$ [15]	t_{OEHC}	20		20		20		ns
Refresh Set Up Time for $\overline{\text{CAS}}$ Referenced to $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{FCS}	20		25		30		ns
Refresh Hold Time for $\overline{\text{CAS}}$ Referenced to $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{FCH}	20		25		30		ns
$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{CPR}	20		25		30		ns
$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh cycles)	t_{RPC}	20		20		20		ns

AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) NOTE 1,2

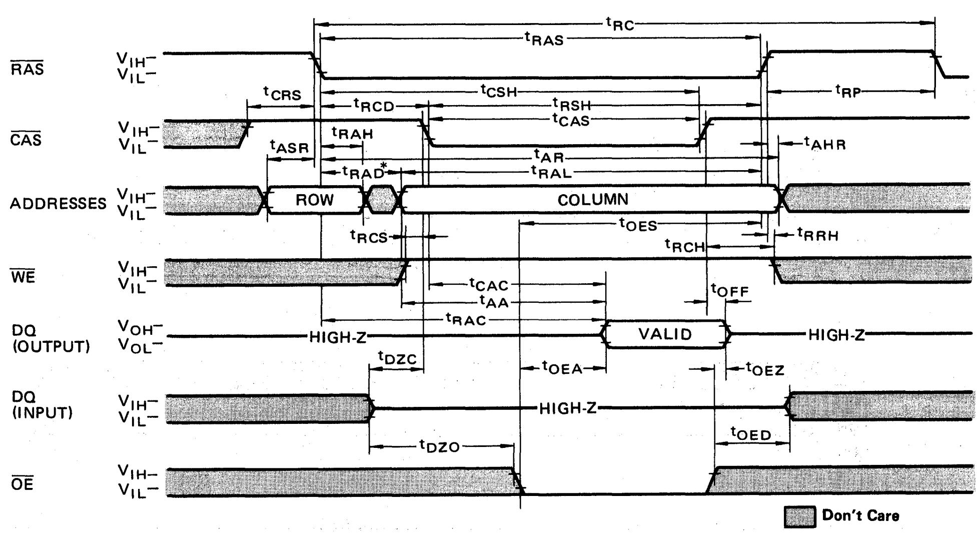
Parameter	NOTE	Symbol	MB 81C466-10		MB 81C466-12		MB 81C466-15		Unit
			Min	Max	Min	Max	Min	Max	
Static Mode Read/Write Cycle Time		t_{SC}	50		60		75		ns
Static Mode Read-Modify-Write Cycle Time		t_{SRWC}	120		145		180		ns
Static Mode $\overline{CAS}$ Precharge Time		t_{CP}	15		20		25		ns
$\overline{OE}$ to $\overline{RAS}$ Inactive Set Up Time		t_{OES}	25		30		35		ns
D_{IN} to $\overline{CAS}$ Delay Time	16	t_{DZC}	0		0		0		ns
D_{IN} to $\overline{OE}$ Delay Time	16	t_{DZO}	0		0		0		ns
Refresh Counter Test Cycle Time	17	t_{RTC}	465		550		645		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	17	t_{TRAS}	365	10000	440	10000	535	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	17	t_{CPT}	50		60		70		ns
Refresh Counter Test $\overline{CAS}$ to Column Address Delay Time	17	t_{CADT}		100		120		150	ns
Refresh Counter Test Access Time from $\overline{CAS}$	17	t_{CACT}		135		165		205	ns
Refresh Counter Test $\overline{CAS}$ to $\overline{WE}$ Delay Time	17	t_{CWDT}	135		165		205		ns

NOTES:

1. An Initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8, V_{OH} = 2.4V, and V_{OL} = 0.4V.
3. Assumes that $t_{RAD} \leqq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.
4. Assumes that $t_{RAD} \geqq t_{RAD}$ (max).
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. Assumes that $t_{LWAD} \leqq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
7. Write Cycle only.
8. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
9. t_{RAD} (min) = t_{RAH} (min) + t_T (t_T = 5ns)
10. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
11. Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
12. t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T = 5ns).
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WS}, t_{WH}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geqq t_{WS}$ (min) and $t_{WH} \geqq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. It $t_{RWD} \geqq t_{RWD}$ (min). The data output will contain data read from the selected cell.
15. Either t_{OEHR} or t_{OEHC} is satisfied, output is disabled.
16. Either t_{DZC} or t_{DZO} must be satisfied.
17. $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

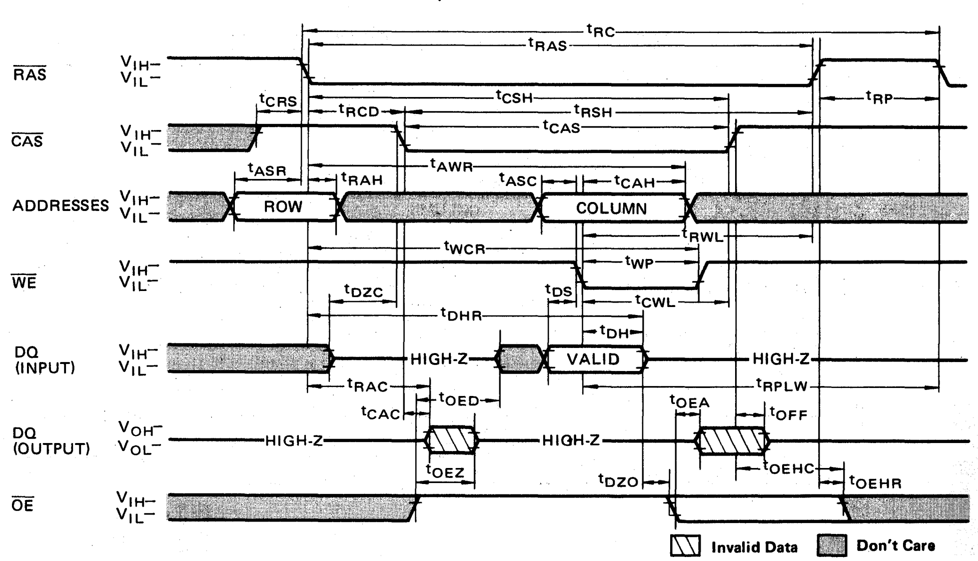
2

Read Cycle



*; If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA}.

Write Cycle (WE Controlled)



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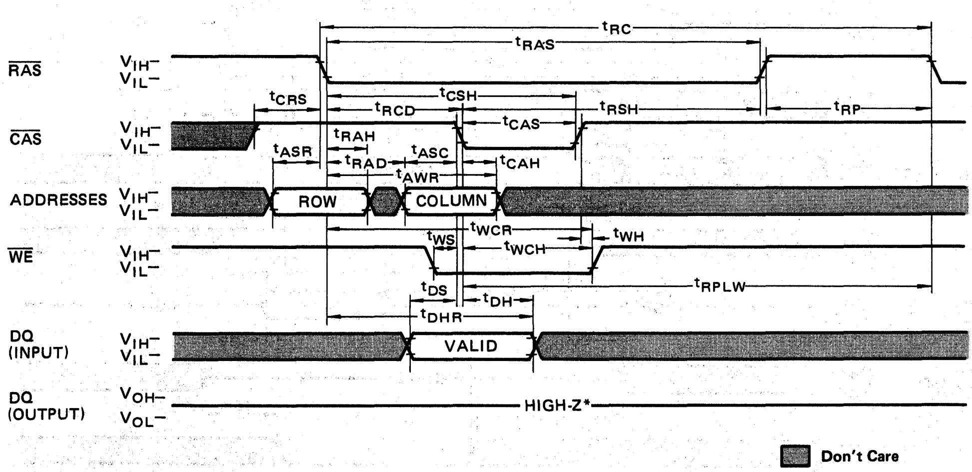
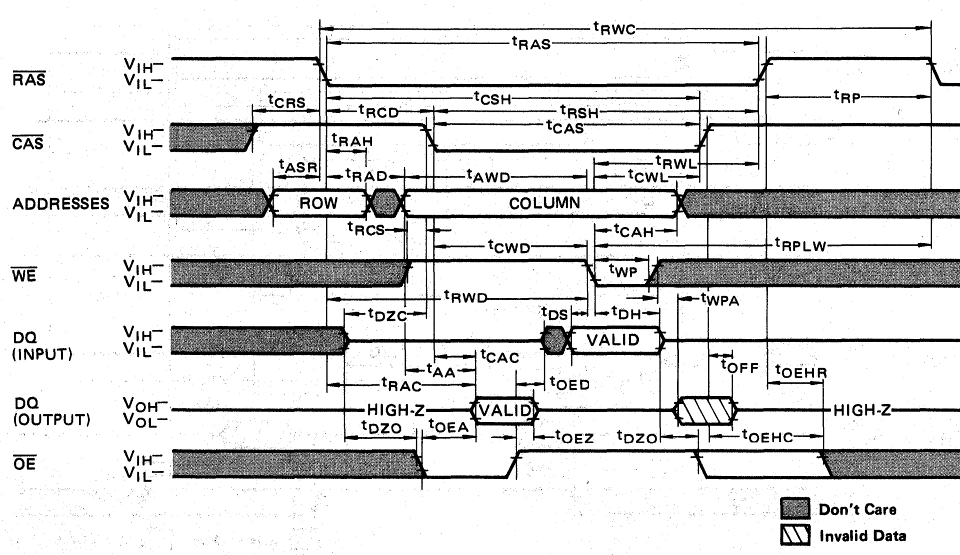
Write Cycle ($\overline{CAS}$ Controlled)
$\overline{OE}$; Don't Care

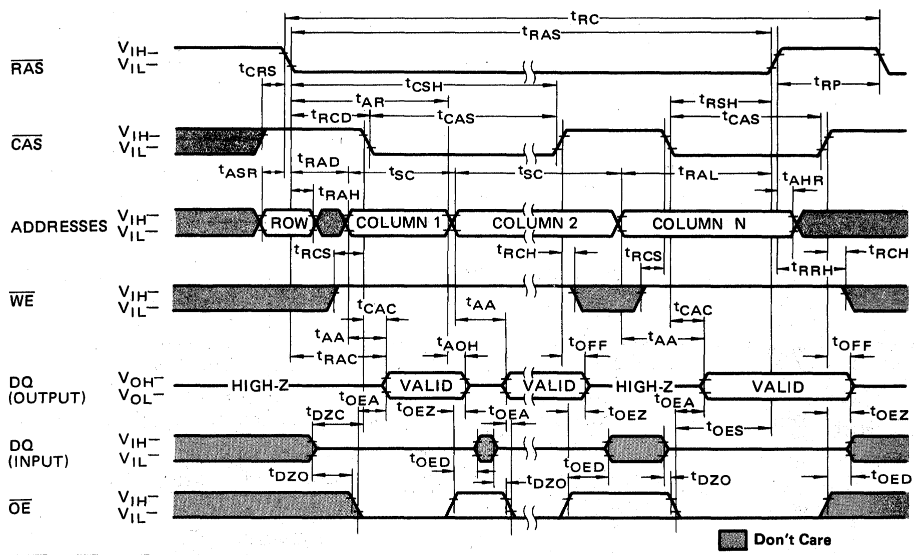


*; If $\overline{OE}$ is kept high through a cycle or $t_{WS} \geqq t_{WS}$ (min) and $t_{WH} \geqq t_{WH}$ (min) are met, DQ pins are kept high impedance state.

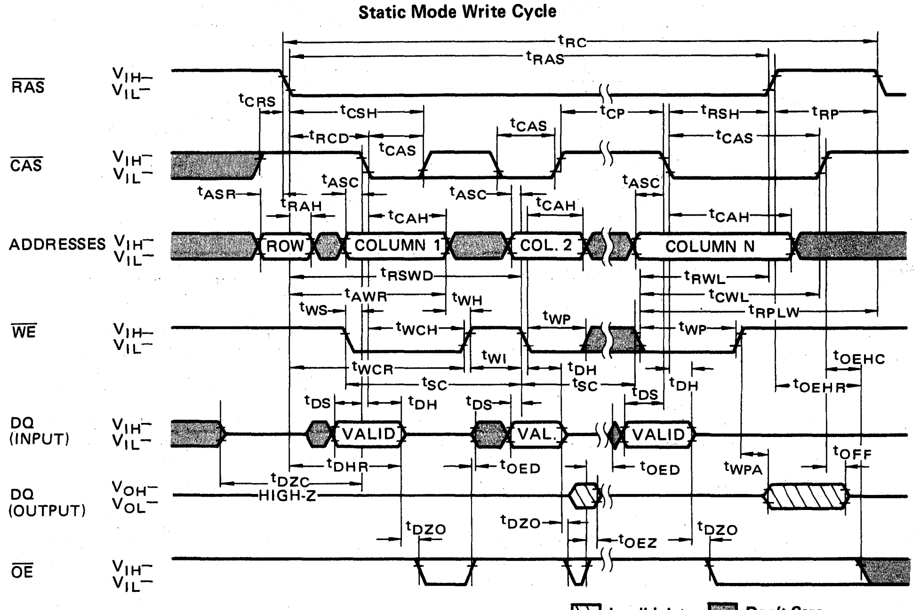
Read-Modify-Write Cycle



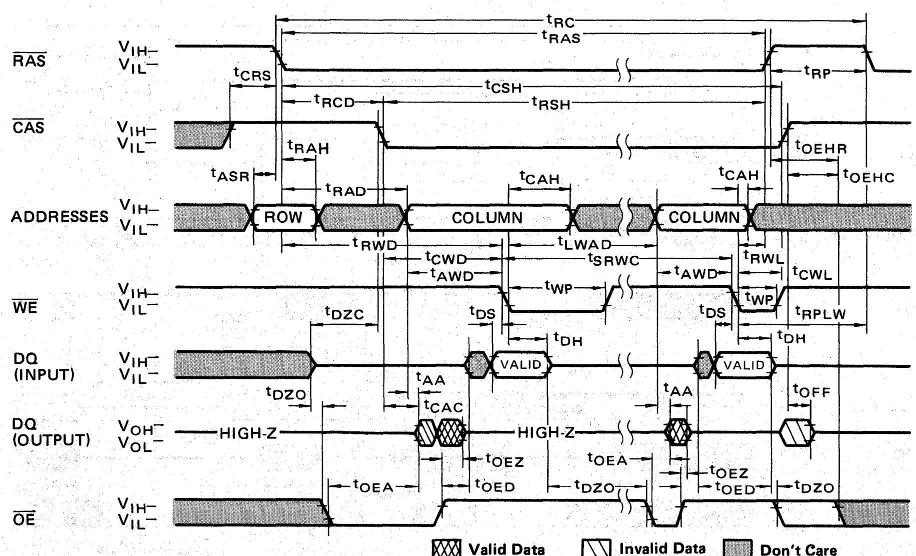
Static Mode Read Cycle



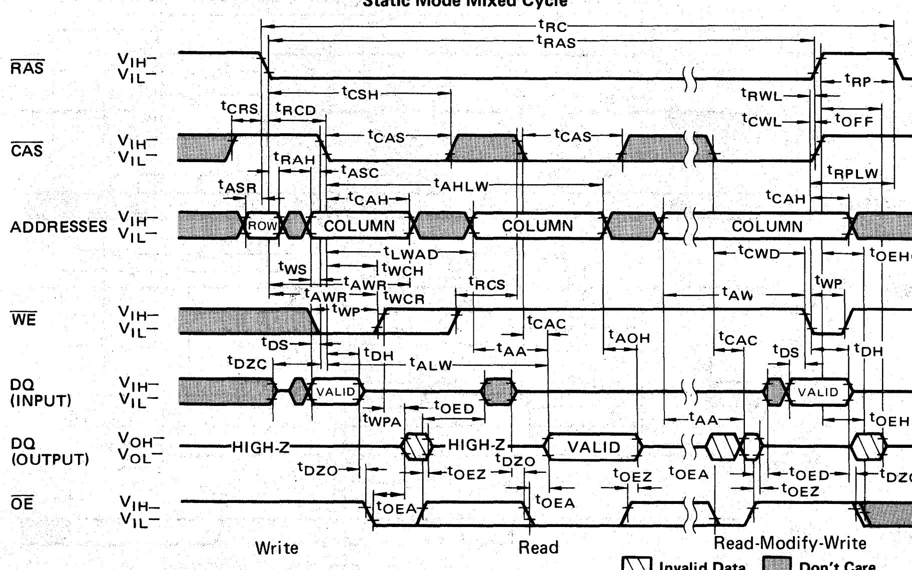
Static Mode Write Cycle



Static Mode Read-Modify-Write Cycle



Static Mode Mixed Cycle



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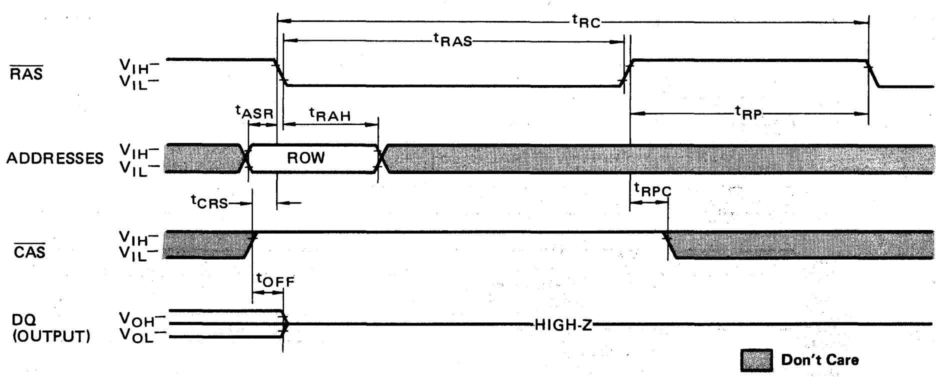
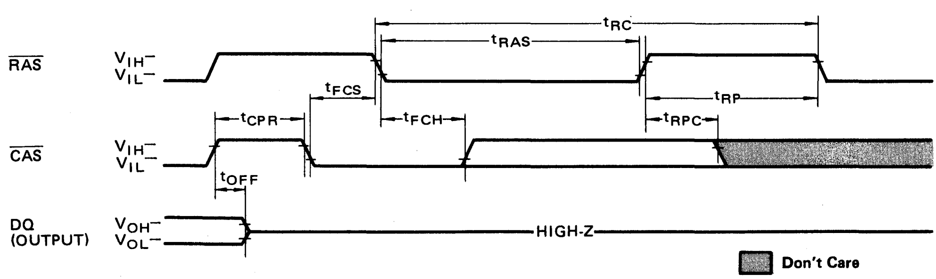
$\overline{RAS}$-Only Refresh Cycle
(Note; $\overline{WE}$, $\overline{OE}$, D_{IN} = Don't Care)



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)
(Note; Address, $\overline{WE}$, $\overline{OE}$, D_{IN} = Don't Care)



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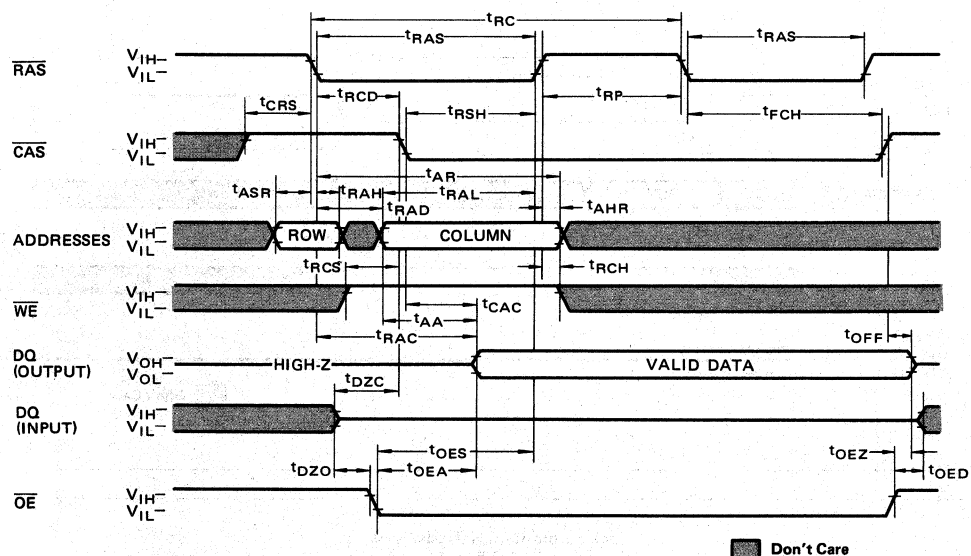
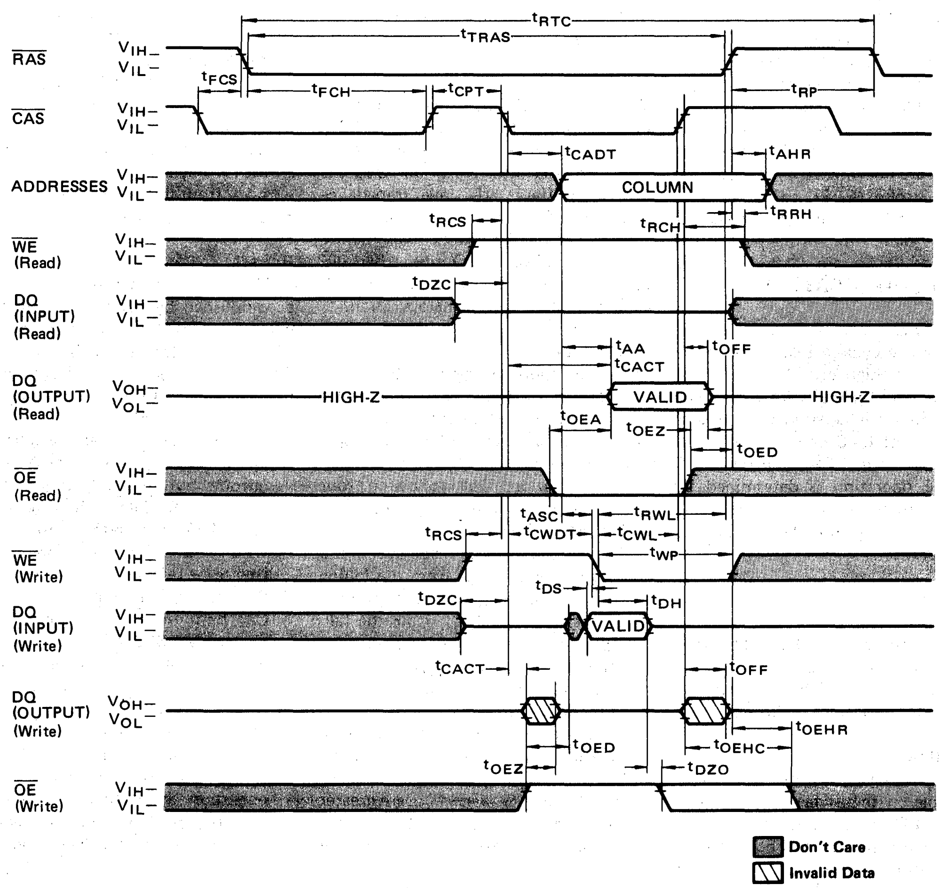
Hidden Refresh Cycle



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:
A total of sixteen binary input address bits are required to decode parallel 4 bits of the 262,144 storage cells within the MB 81C466. Eight row address bits are established on the address input pins (A_0 to A_7) and latched with the Row Address Strobe (RAS). The eight column address bits are established on the address input pins (A_0 to A_7) after the Row Address Hold Time has been satisfied. In read cycle, the column addresses are not latched by the Column Address Strobe (CAS), so the column address must be stable until the output becomes valid. In write cycle, the column addresses are latched by the later falling edge of CAS or WE.

Write Enable:
Read or Write cycle is selected with the WE inputs. A high on WE selects read cycle and low selects write cycle. The write operation is asserted on the later falling edge of CAS or WE (Both CAS and WE are low). The time period of the write operation is determined by internal circuit, thus the next write operation will be inhibited during the write operation.

Data Pins:
Data Inputs;
Data are written into the MB 81C466 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of CAS or WE.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is in high impedance state until CAS is brought low. In a read cycle, the access time is determined by the following conditions:

1. t_{RAC} from the falling edge of RAS.
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of CAS.
4. t_{OEA} from the falling edge of OE.

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC}=t_{RCD}+t_{CAC}$ or $t_{RAC}=t_{RAD}+t_{AA}$.
Data output remains valid while the column address inputs are kept constant. However, when either CAS or OE goes high, the output returns to a high impedance state. In the static write cycle (CAS controlled), if both $t_{WS} \geqq t_{WS}$ (min) and $t_{WH} \geqq t_{WH}$ (min) are met, data pins are input mode regardless of the state of OE.

Output Enable:
The OE controls the impedance of the output buffers. In the high state on OE, the output buffers are high impedance state. In the low state on OE, the output buffers are low impedance state. In the write cycle (WE controlled), the OE must be high before the data applied to DQ pins. When WE controlled write cycles is not used, OE can be low throughout the operation.

Static Mode:
The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, CAS can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.

1. Static mode read cycle;
   In a static mode read cycle, the access time is t_{RAC} from the falling edge of RAS or t_{AA} from the column address input or t_{OEA} from the falling edge of OE. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle;
   In a static mode write cycle, the data is written into the cell triggered by the later falling edge of CAS or WE. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle. The OE must be high before the data are applied to DQ pins.
3. Static mode read-modify-write cycle;
   In the static mode read-modify-write cycle, WE goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of CAS. The data and column address inputs are strobed and latched by the falling edge of WE. The OE must be high before the data are applied to DQ pins.
4. Static mode mixed cycle;
   In the static mode, read, write, and read-modify-write cycles can be mixed in any order.

In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.

1. t_{ALW} from the falling edge of WE at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of WE at the read cycle.
4. t_{CAC} from the falling edge of CAS.
5. t_{OEA} from the falling edge of OE.

Refresh:
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7) at least every 4ms.
The MB 81C466 offers the following three types of refresh.

1. RAS only refresh;
   The RAS-only refresh avoids any outputs during refresh because the outputs buffers are high impedance state due to CAS-high. Strobing of each 256 row address (A_0 to A_7) with RAS will cause all bits in each row to be refreshed.
2. CAS-before-RAS refresh;
   CAS-before-RAS refreshing available on the MB 81C466 offers an alternate refresh method. If CAS is held low for the specified period (t_{FCS}) before RAS goes low, on chip refresh control clock generator and the internal refresh address counter are enabled, and an internal refresh operation is executed. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next CAS-before-RAS refresh.
3. Hidden refresh;
   A hidden refresh cycle will be executed while maintaining latest valid data at the output pin by extending the CAS low time. For the MB 81C466, a hidden refresh cycle is CAS-before-RAS refresh. The internal refresh address counter provides the refresh address, as in a normal CAS-before-RAS refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh counter Test:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the function of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and read-modify-write cycles are enabled according to the state of $\overline{WE}$. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (8 bits) and a column address (8 bits), to be accessed is shown below.

ROW ADDRESS – All bits A_0 to A_7 are provided by the refresh counter.

COLUMN ADDRESS – All the bits A_0 to A_7 are provided by externally after t_{CADT}.

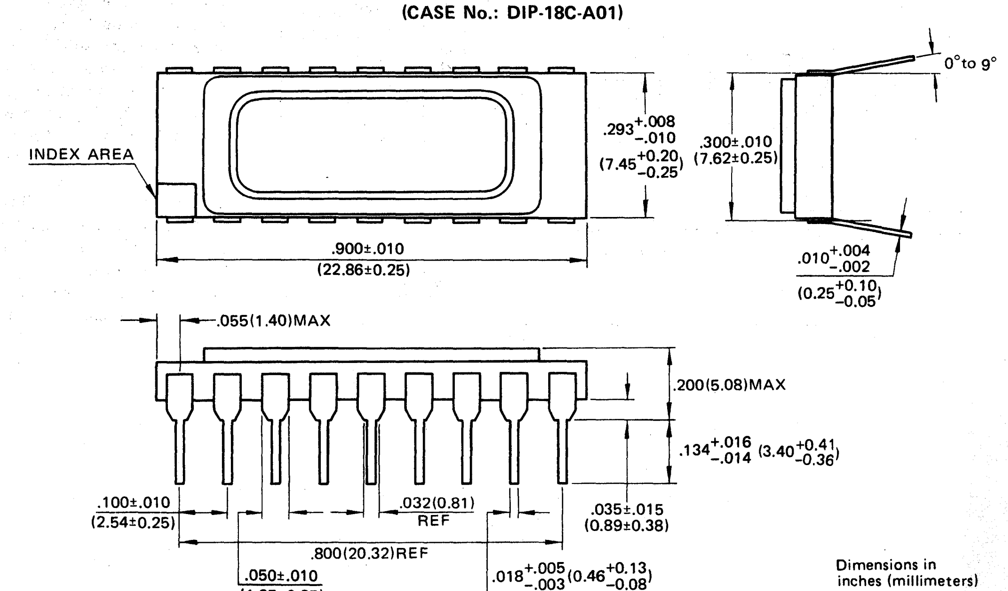
The recommended procedure of $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test is shown below. The timing of $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle should be used.

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Using a write cycle, write 0s to all 256 row addresses.
4) Using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle in read-modify-write mode, read the 0 written in step 3), and simultaneously write a 1 to the same cell. This step is repeated 256 row address generated by internal refresh address counter.
5) Using a normal read cycle, read back the 1s written in step 4), from all 256 locations.
6) Complement the test pattern and repeat step 3), 4), and 5).

PACKAGE DIMENSIONS

(Suffix: -C)

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)

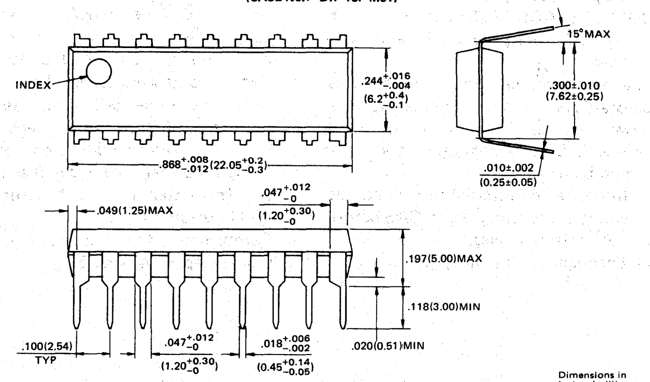


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

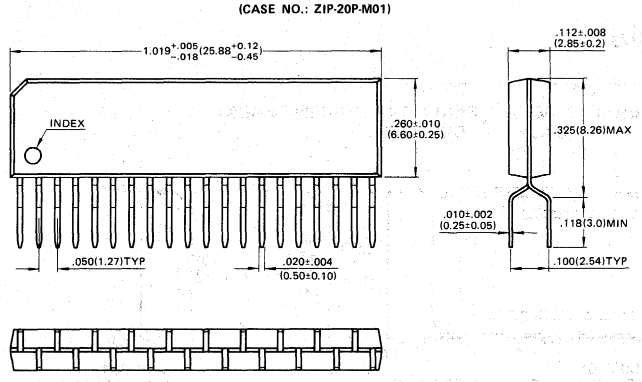
(Suffix: -P) (Suffix: -PSZ)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-18P-M01)



Dimensions in inches (millimeters)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE NO.: ZIP-20P-M01)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

CMOS 1048576-BIT FAST PAGE DYNAMIC RAM

MB81C1000-70
MB81C1000-80
MB81C1000-10
MB81C1000-12

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September 1988
Edition 1.0

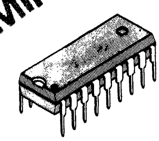
PRELIMINARY

CMOS 1,048,576 x 1 BIT FAST PAGE MODE DYNAMIC RAM

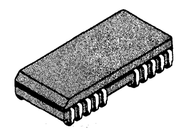
The Fujitsu MB81C1000 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1000 has been designed for mainframe memories, buffer memories, and video image memories requiring highspeed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very lower power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1000 high α-ray soft error immunity and long refresh time.
Since the CMOS circuits are used for peripheral circuits, low power dissipation and high speed operation are realized.

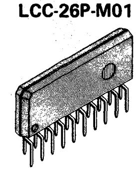
This specification is applied to "BC" version revised with intent to realize faster access time. So faster speed version (70ns and 80ns) are available on this chip.



PLASTIC PACKAGE
DIP-18P-M04



PLASTIC PACKAGE
LCC-26P-M01



PLASTIC PACKAGE
ZIP-20P-M02

DIP-18C-A01: See Page 19

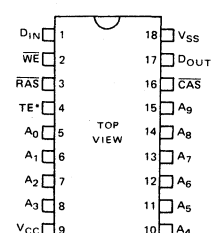
PRODUCT LINE

Parameter	MB81C1000 -70	MB81C1000 -80	MB81C1000 -10	MB81C1000 -12
Row Access time	70ns max.	80ns max.	100ns max.	120ns max.
Random Cycle Time	140ns min.	155ns min.	180ns min.	210ns min.
Column Address Time	43ns max.	45ns max.	50ns max.	60ns max.
Column Access Time	25ns max.	25ns max.	30ns max.	35ns max.
Fast Page Mode Cycle Time	53ns min.	55ns min.	60ns min.	70ns min.
Low Power Dissipation • Operating current	413mW max.	385mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level)/5.5mW max. (CMOS level)			

FEATURES

- 1,048,576 word x 1bit organization
- Silicon Gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

PIN ASSIGNMENT



*: Test Enable (will be available)

Pin Assignment For SOJ: See Page 17

Pin Assignment For ZIP: See Page 18

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} Relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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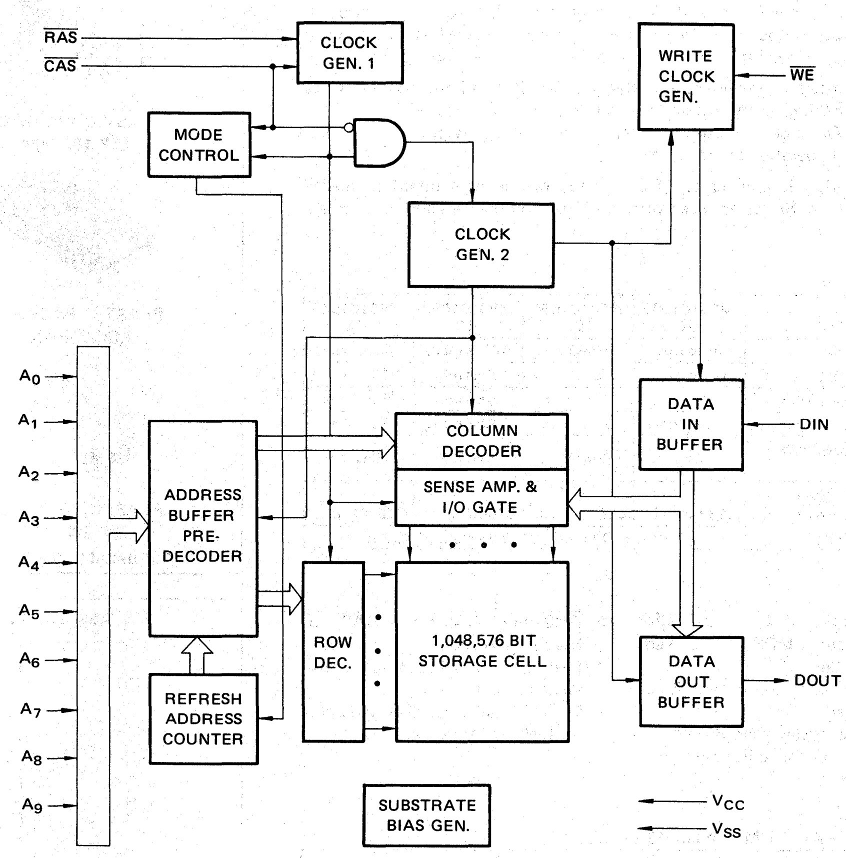
Fig. 1 – BLOCK DIAGRAM



CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance, A_0 to A_9, D_{IN}	C_{IN1}		5	pF
Input Capacitance, $\overline{RAS}$ $\overline{CAS}$, $\overline{WE}$	C_{IN2}		5	pF
Output Capacitance, D_{OUT}	C_{OUT}		5	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Ambient Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input High Voltage, All inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, All inputs	V_{IL}	−2.0		0.8	V	

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DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

Parameter		Conditions	Symbol	Values		Unit
				Min	Max	
Operating Current* (Average power Supply current)	MB81C1000-70	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	I_{CC1}		75	mA
	MB81C1000-80				70	
	MB81C1000-10				60	
	MB81C1000-12				50	
Standby Current (Power supply current)	TTL level	$\overline{RAS} = \overline{CAS} = V_{IH}$	I_{CC2}		2.0	mA
	CMOS level	$\overline{RAS} = \overline{CAS} \geqq V_{CC} - 0.2V$			1.0	
Refresh Current 1* (Average power supply current	MB81C1000-70	$\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min	I_{CC3}		70	mA
	MB81C1000-80				65	
	MB81C1000-10				55	
	MB81C1000-12				45	
Fast Page Mode Current*	MB81C1000-70	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = min	I_{CC4}		47	mA
	MB81C1000-80				45	
	MB81C1000-10				40	
	MB81C1000-12				33	
Refresh Current 2* (Average power current)	MB81C1000-70	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	I_{CC5}		70	mA
	MB81C1000-80				65	
	MB81C1000-10				55	
	MB81C1000-12				45	
Input Leakage Current		$0V \leqq V_{IN} \leqq 5.5V$, $4.5V \leqq V_{CC} \leqq 5.5V$, V_{SS} = 0V; pins not under test = 0V	$I_{I(L)}$	-10	10	μA
Output Leakage Current		$0V \leqq V_{OUT} \leqq 5.5V$; Data out disabled	$I_{O(L)}$	-10	10	
Output High Voltage		I_{OH} = -5mA	V_{OH}	2.4		V
Output Low Voltage		I_{OL} = 4.2mA	V_{OL}		0.4	

NOTE: *; I_{CC} depends on the output load conditions and cycle rate. The specified values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
I_{CC4} is specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter NOTE	Symbol	MB81C1000-70		MB81C1000-80		MB81C1000-10		MB81C1000-12		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh	t_{REF}		8.2		8.2		8.2		8.2	ms
2	Random Read/Write Cycle Time	t_{RC}	140		155		180		210		ns
3	Read-Modify-Write Cycle Time	t_{RWC}	167		182		210		245		ns
4	Access Time from $\overline{RAS}$ 4 7	t_{RAC}		70		80		100		120	ns
5	Access Time from $\overline{CAS}$ 5 7	t_{CAC}		25		25		30		35	ns
6	Access Time from Column Address 6 7	t_{AA}		43		45		50		60	ns
7	Output Data Hold Time	t_{OH}	7		7		7		7		ns
8	Output Buffer Turn on Delay Time	t_{ON}	5		5		5		5		ns
9	Output Buffer Turn Off Delay Time 8	t_{OFF}		25		25		25		25	ns
10	Transition Time	t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time	t_{RP}	60		65		70		80		ns
12	$\overline{RAS}$ Pulse Width	t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time	t_{RSH}	25		25		30		35		ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		0		0		ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time 9 10	t_{RCD}	20	45	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width	t_{CAS}	25		25		30		35		ns
17	$\overline{CAS}$ Hold Time	t_{CSH}	70		80		100		120		ns
18	$\overline{CAS}$ Precharge Time ($\overline{C}$-B-$\overline{R}$ Cycle) 15	t_{CPN}	15		15		15		15		ns
19	Row Address Set Up Time	t_{ASR}	0		0		0		0		ns
20	Row Address Hold Time	t_{RAH}	10		12		15		15		ns
21	Column Address Set Up Time	t_{ASC}	0		0		0		0		ns
22	Column Address Hold Time	t_{CAH}	15		15		15		20		ns
23	$\overline{RAS}$ to Column Address Delay Time 11	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	43		45		50		60		ns
25	Read Command Set Up Time	t_{RCS}	0		0		0		0		ns

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AC CHARACTERISTICS (Cont'd)

(At recommended operating conditions unless otherwise noted.) Notes 1,2,3

No.	Parameter	NOTE	Symbol	MB81C1000-70		MB81C1000-80		MB81C1000-10		MB81C1000-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
26	Read Command Hold Time Referenced to $\overline{RAS}$	12	t_{RRH}	0		0		0		0		ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	12	t_{RCH}	0		0		0		0		ns
28	Write Command Set Up Time	13	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time		t_{WCH}	15		15		15		20		ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15		15		15		20		ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22		22		25		30		ns
32	Write Commnd to $\overline{CAS}$ Lead Time		t_{CWL}	17		17		20		25		ns
33	D_{IN} Set Up Time		t_{DS}	0		0		0		0		ns
34	D_{IN} Hold time		t_{DH}	15		15		15		20		ns
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	13	t_{RWD}	70		80		100		120		ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	13	t_{CWD}	25		25		30		35		ns
37	Column Address to $\overline{WE}$ Delay Time	13	t_{AWD}	43		45		50		60		ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0		0		0		0		ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0		0		0		0		ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15		15		15		20		ns
41	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}		43		45		50		60	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	53		55		60		70		ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	75		77		85		100		ns
52	Access Time from $\overline{CAS}$ Precharge	7 14	t_{CPA}		53		55		60		70	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15		15		15		15		ns

NOTES:

1. An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

2. AC characteristics assume t_T = 5 ns.

3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 2 and 3.

5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA}\text{-}t_{CAC}\text{-}t_T$, access time is t_{CAC}.

6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA}\text{-}t_{CAC}\text{-}t_T$, access time is t_{AA}.

7. Measured with a load equivalent to two TTL loads and 100 pF.

8. t_{OFF} is specified that output buffer changes to high impedance state.

9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

10. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).

11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

13. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restructive operating parameter. They are included in the data sheet as the electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin.
    If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear at the D_{OUT} pin, and write operation can be executed by satisfing t_{RWL}, t_{CWL}, and t_{RAL} specifications.

14. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).

15. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only

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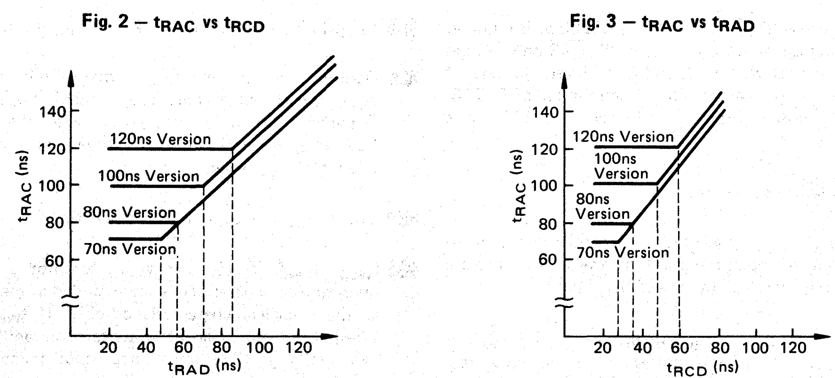
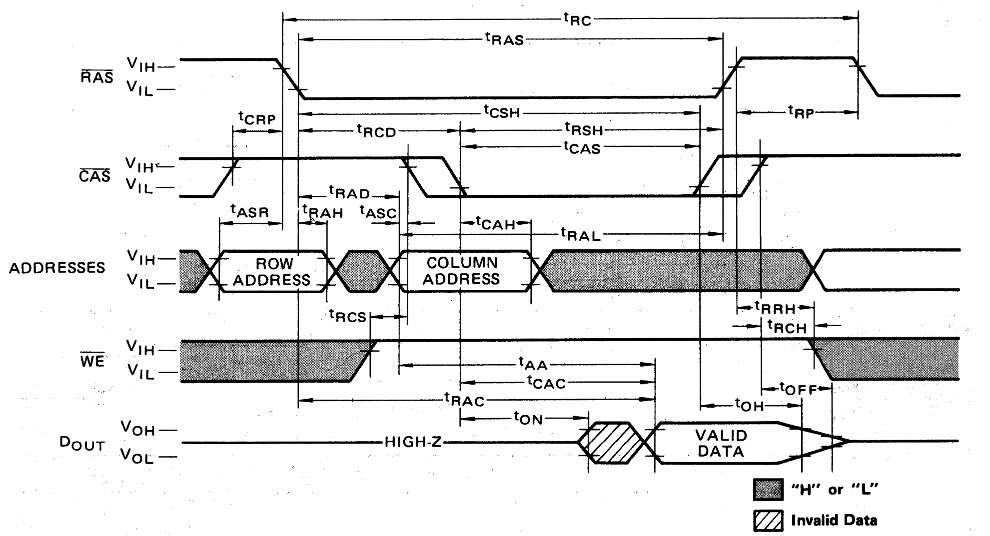


FUNCTIONAL TRUTH TABLE

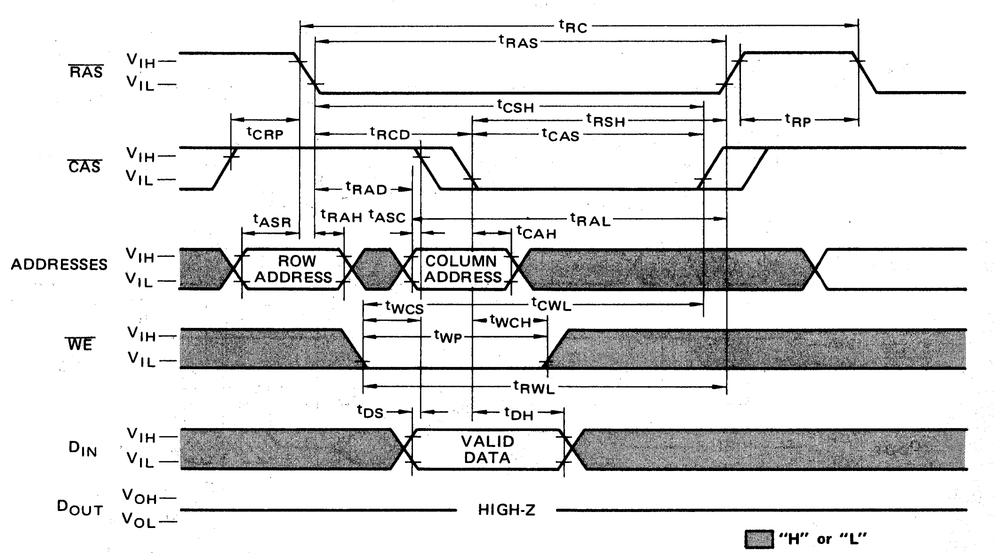
Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	–	–	–	High-Z	–	
Read Cycle	L	L	H	Valid	Valid	–	Valid	○ *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	○ *	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	Valid	Valid	X→ Valid	Valid	○ *	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	–	–	High-Z	○	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	L	L	X	–	–	–	High-Z	○	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	–	–	–	Valid	○	Previous data is kept.

X; "H" or "L"
*; It is impossible in fast page mode.

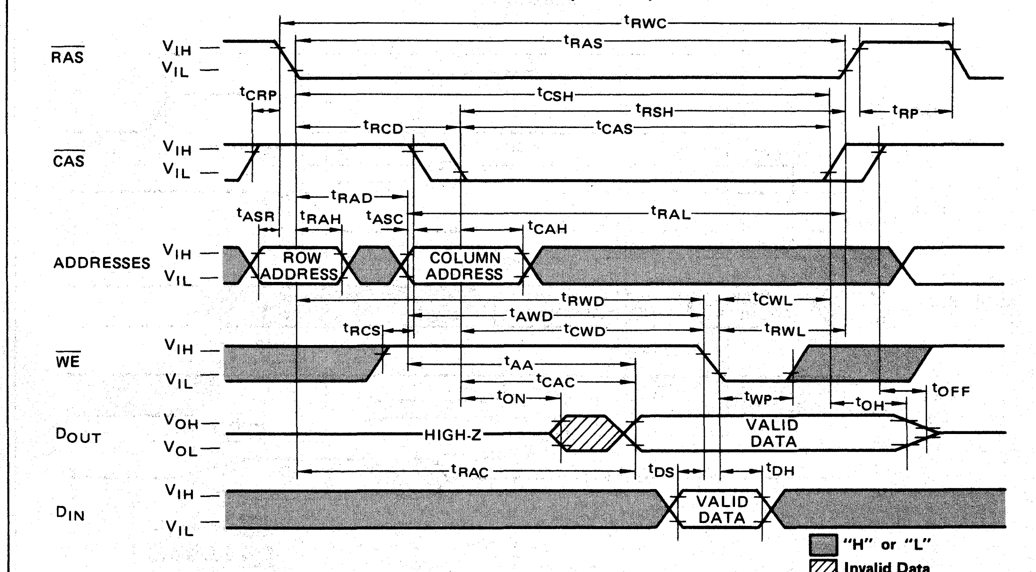
Read Cycle



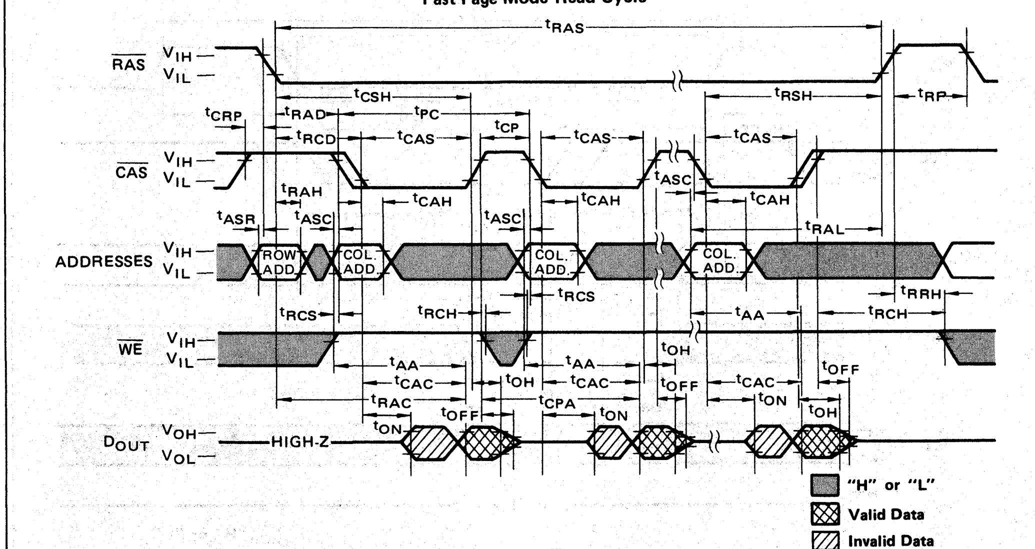
Write Cycle (Early Write)



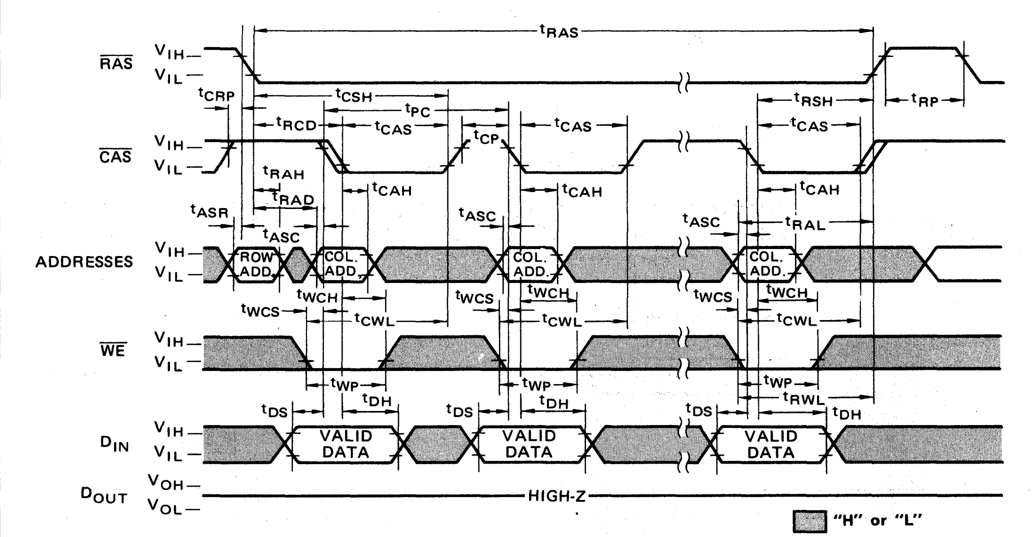
Read-Write/Read-Modify-Write Cycle



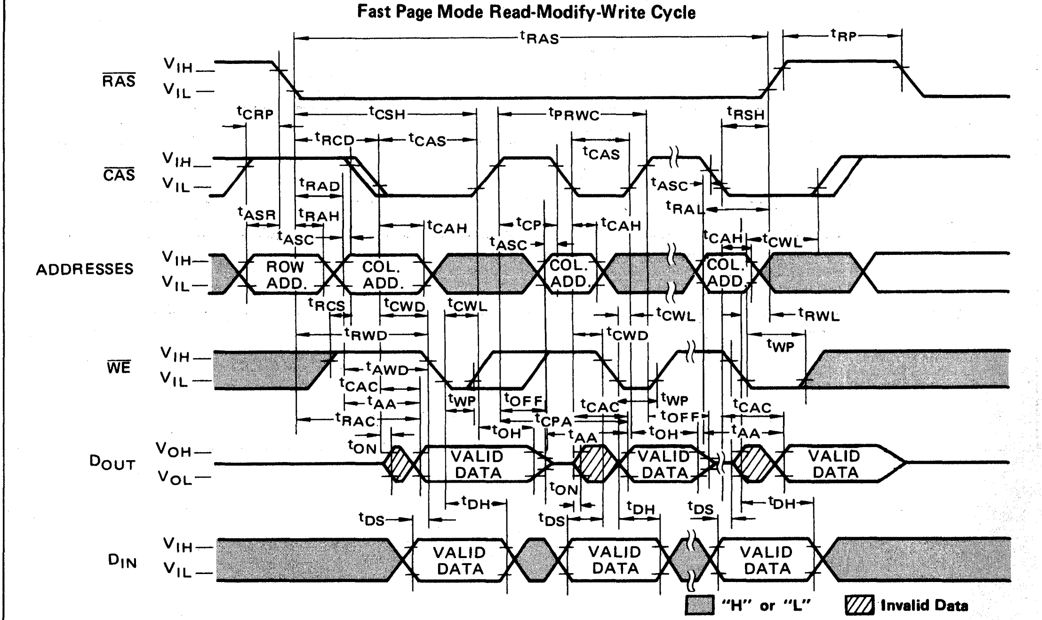
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)

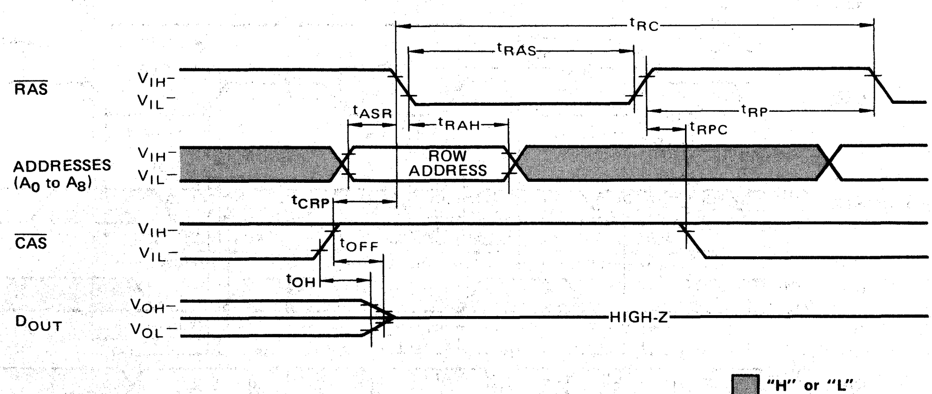


Fast Page Mode Read-Modify-Write Cycle



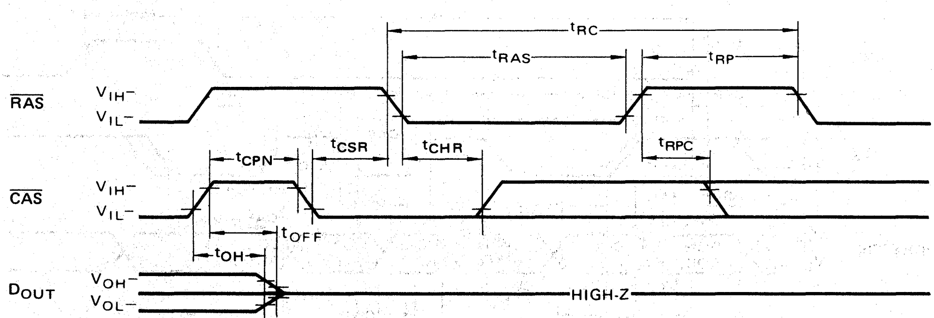
$\overline{RAS}$-only Refresh Cycle

NOTE: $\overline{WE}$, D_{IN} = "H"or"L", A_9 = V_{IH} or V_{IL}

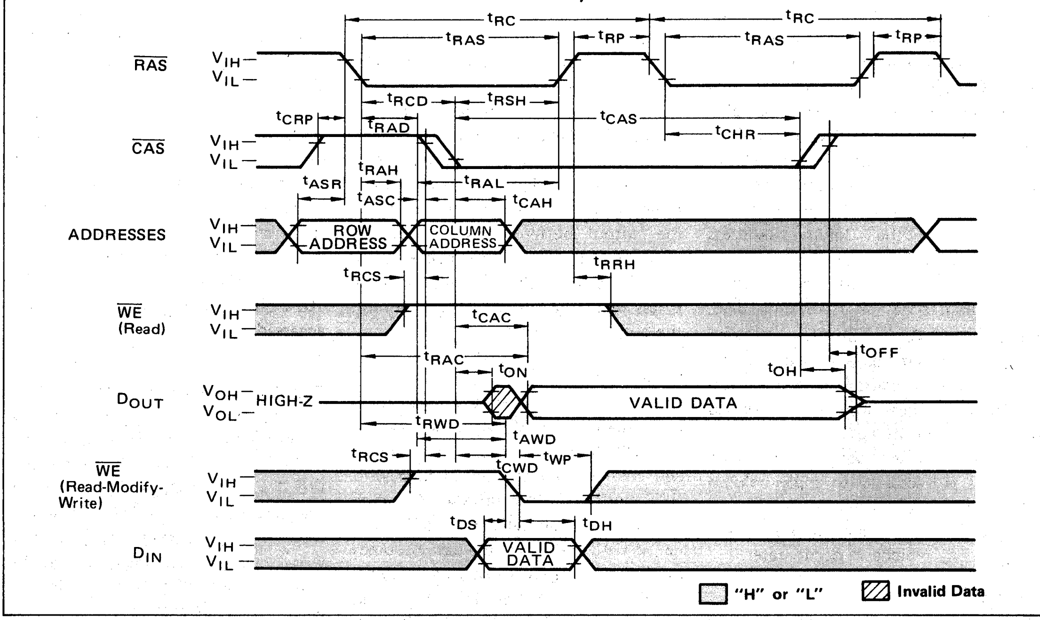


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

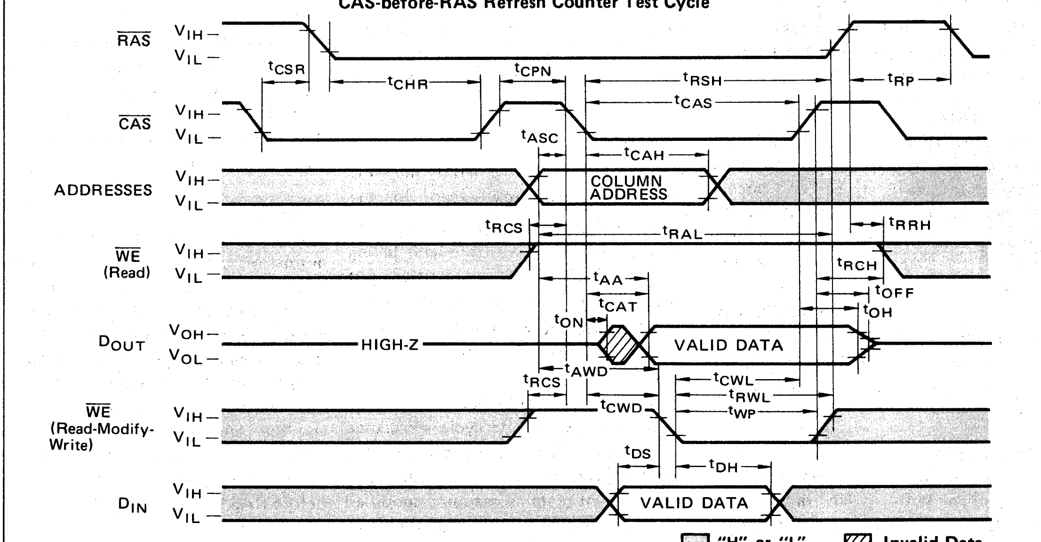
NOTE: Address, $\overline{WE}$, D_{IN} = "H"or"L"



Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:
A total of twenty binary input address bits are required to decode any one of the 1,048,576 storage cells whthin the MB 81C1000. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe ($\overline{RAS}$). The ten column address bits are established on the address input pins (A_0 to A_9) and latched with the Column Address Strobe ($\overline{CAS}$). All row and column address must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min) + t_T.
Therefore, to get valid data within t_{RAC}, it is necessary to apply column address within t_{RAD} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occur later.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. Data input is ignored during read cycle. Data output is high impedance state during write cycle.

Data Input:
Data is written into the MB 81C1000 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-modify-write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is high impedance state until $\overline{CAS}$ is brought low. In a read or read-modify-write cycle, the output becomes valid after t_{RAC} from the falling edge of $\overline{CAS}$ when t_{RCD} (max) is satisfied or after t_{CAC} when t_{RCD} is longer than t_{RCD} (max). The data output remains valid until $\overline{CAS}$ returns to high with t_{OH} and becomes high impedance state after t_{OFF}. In an early write cycle, the output buffer is high impedance state during the entire cycle. In a delayed write cycle, if t_{RWD} or t_{CWD} is less than t_{RWD} (min) or t_{CWD} (min), the output is invalid.

Read Cycle:
The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output is remain valid with $\overline{CAS}$ "L", i.e., if $\overline{CAS}$ goes "H", the data becomes invalid with t_{OH}. During read cycle, the D_{IN} pin is "H" or "L". The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), or Column address input (t_{AA}). If t_{RCD} ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}.

Write Cycle:
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and D_{IN} pin. The data on D_{IN} pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL} and t_{RAL} must be satisfied the specifications.

Read-Modify-Write Cycle:
The read-modify-write cycle is executed by changing $\overline{WE}$ high to low after the data appears on the D_{OUT} pin. After the current data is readout, modified data can be re-written into the same address quickly.

Fast Page Mode Read Cycle:
The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H". Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. So power consumption and cycle time are reduced. During fast page mode, the access time is t_{CAC}, t_{AA}, or t_{CPA}, whichever occur later. Any of the 1024 bits belonging to each row can be accessed.

Fast Page Mode Write Cycle:
The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$. The data on D_{IN} pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, t_{CWL} must be satisfied. Any of the 1024 bits belonging to each row can be accessed.

Fast Page Mode Read-Modify-Write Cycle:
During fast page mode, the read-modify-write cycle can be executed by changing $\overline{WE}$ high to low after the data appears at the D_{OUT} pin as well as normal cycle. Any of the 1024 bits belonging to each row can be accessed.

Refresh:
The refresh of DRAM is executed by normal read, write or read-modity-write cycle, i.e., the cells on the one row line are refreshed by executing one of three cycles. 1024 row address must be refreshed every 8.2 ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB 81C1000 also has three types of refresh modes, $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and Hidden refresh.

1. $\overline{\text{RAS}}$-Only Refresh;
The $\overline{\text{RAS}}$-only refresh is executed by keeping $\overline{\text{RAS}}$ "L" and keeping $\overline{\text{CAS}}$ "H" through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$-only refresh, the D_{OUT} pin is kept high impedance state.

2. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh;
The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is executed by bringing $\overline{\text{CAS}}$ "L" before $\overline{\text{RAS}}$. By this timing combination, the MB 81C1000 executes $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh. The row address input is not necessary because it is generated internally.

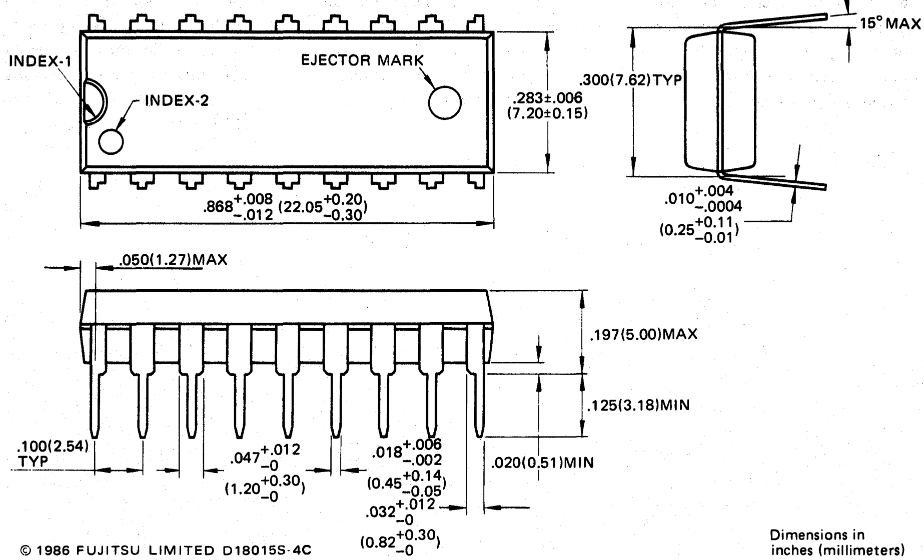
3. Hidden Refresh;
The Hidden refresh is executed by keeping $\overline{\text{CAS}}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{\text{CAS}}$ is kept low continusely from previous cycle, followed refresh cycle should be $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh.

2

PACKAGE DIMENSIONS

(Suffix: -P)

18 LEAD PLASTIC DUAL-IN-LINE PACKAGE (CASE No.: DIP-18P-M04)



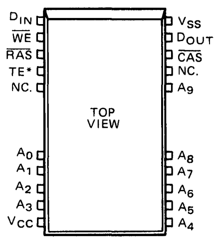
Dimensions in inches (millimeters)

2

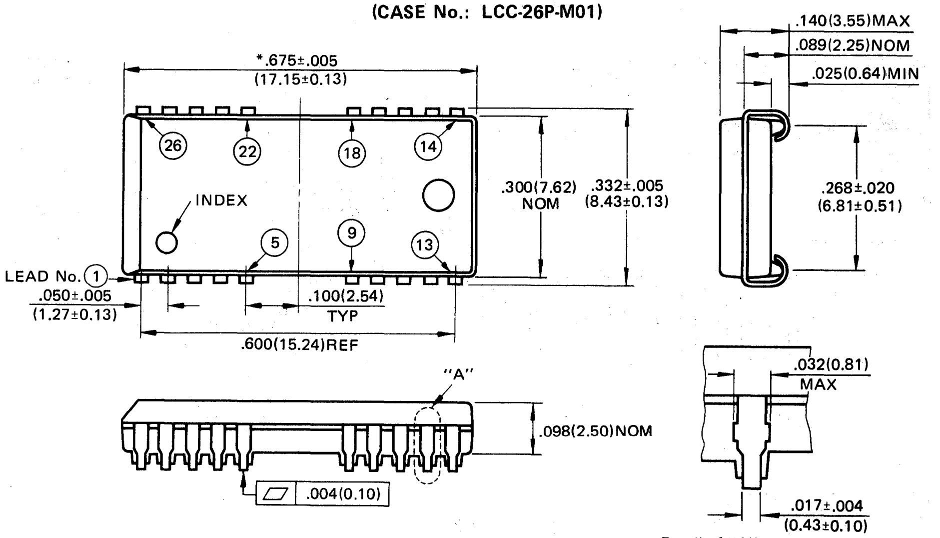
PACKAGE DIMENSIONS

(Suffix: -PJ)

PIN ASSIGNMENT



26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M01)



Detail of "A" part

NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package. Foot-print compatible with "SOJ-26", LCC-26C-A01)

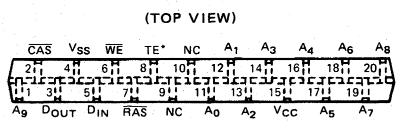
Dimensions in inches (millimeters)

2

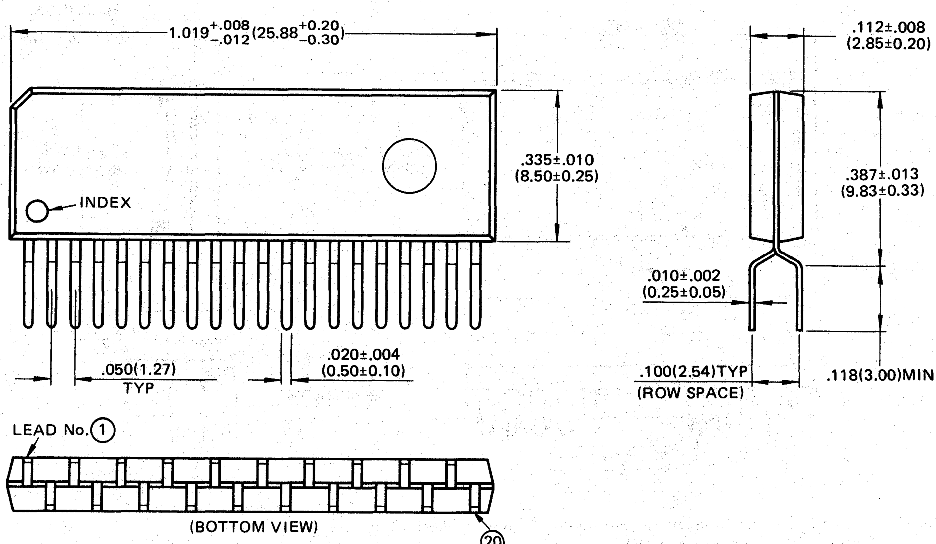
PACKAGE DIMENSIONS

(Suffix: -PSZ)

PIN ASSIGNMENT



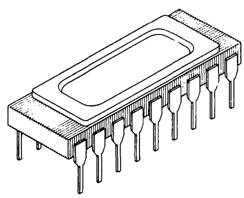
20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)



Dimensions in inches (millimeters)

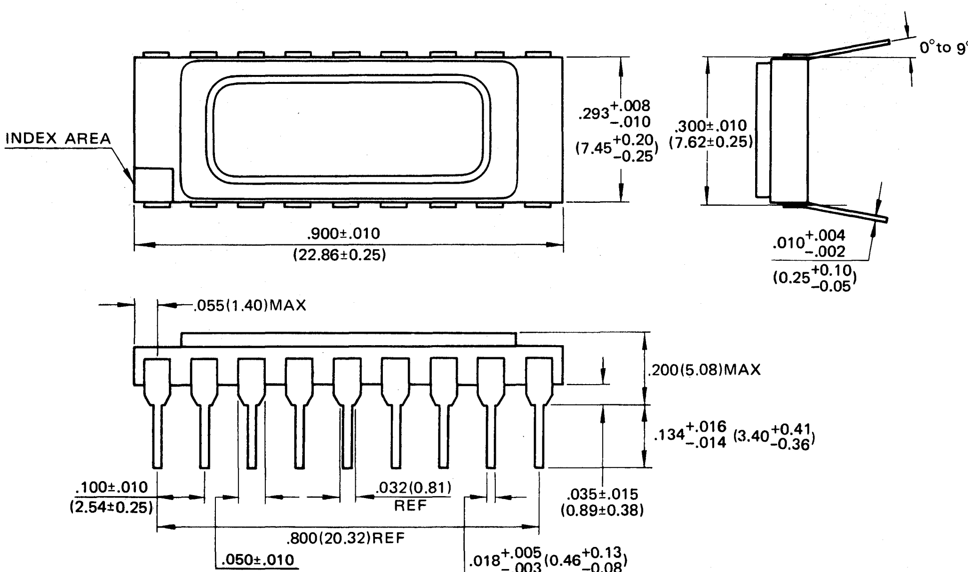
PACKAGE DIMENSIONS

(Suffix :-C)



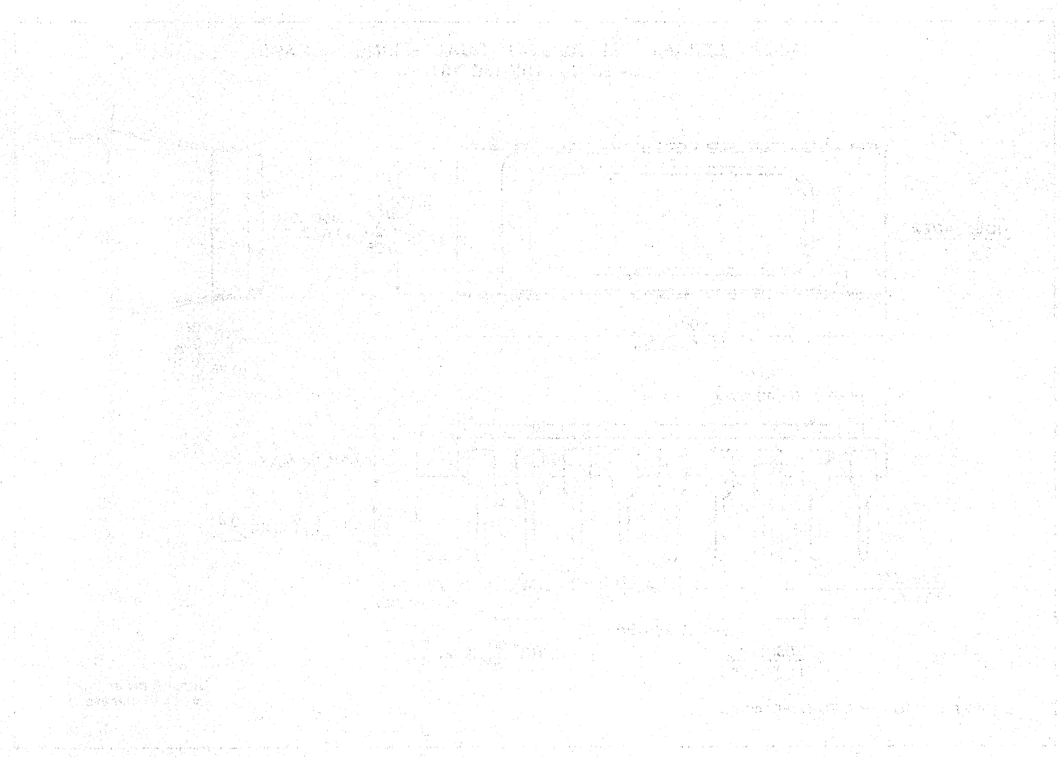
DIP-18C-A01

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



Dimensions in inches (millimeters)

2



FUJITSU

CMOS 1048576 BIT NIBBLE DYNAMIC RAM

MB81C1001-70
MB81C1001-80
MB81C1001-10
MB81C1001-12

2

PRELIMINARY

September 1988
Edition 1.0

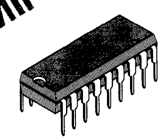
CMOS 1,048,576 x 1 BIT NIBBLE MODE DYNAMIC RAM

The Fujitsu MB81C1001 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1001 has been designed for mainframe memories, buffer memories, and video image memories requiring highspeed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very lower power dissipation.

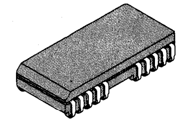
Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1001 high α-ray soft error immunity and long refresh time.

Since the CMOS circuits are used for peripheral circuits, low power dissipation and high speed operation are realized.

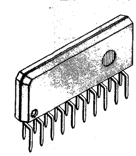
This specification is applied to "BC" version revised with intent to realize faster access time. So faster speed version (70ns and 80ns) are available on this chip.



PLASTIC PACKAGE
DIP-18P-M04



PLASTIC PACKAGE
LCC-26P-M01



PLASTIC PACKAGE
ZIP-20P-M02

DIP-18C-A01: See Page 19

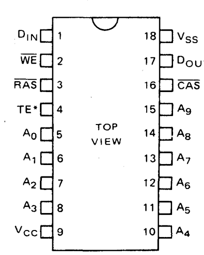
PRODUCT LINE

Parameter	MB81C1001 -70	MB81C1001 -80	MB81C1001 -10	MB81C1001 -12
Row Access Time	70ns max.	80ns max.	100ns max.	120ns max.
Random Cycle Time	140ns min.	155ns min.	180ns min.	210ns min.
Column Address Time	43ns max.	45ns max.	50ns max.	60ns max.
Column Access Time	25ns max.	25ns max.	30ns max.	35ns max.
Nibble Mode Cycle Time	50ns min.	50ns min.	55ns min.	60ns min.
Low Power Dissipation • Operating current	413mW max.	385mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level)/5.5mW max. (CMOS level)			

FEATURES

- 1,048,576 word x 1bit organization
- Silicon Gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2ms
- Common I/O capability by using early write
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance.

PIN ASSIGNMENT



*: Test Enable (will be available)

Pin Assignment
For SOJ: See Page 17
Pin Assignment
For ZIP: See Page 18

ABSOLUTE MAXIMUM RATINGS (See NOTE)

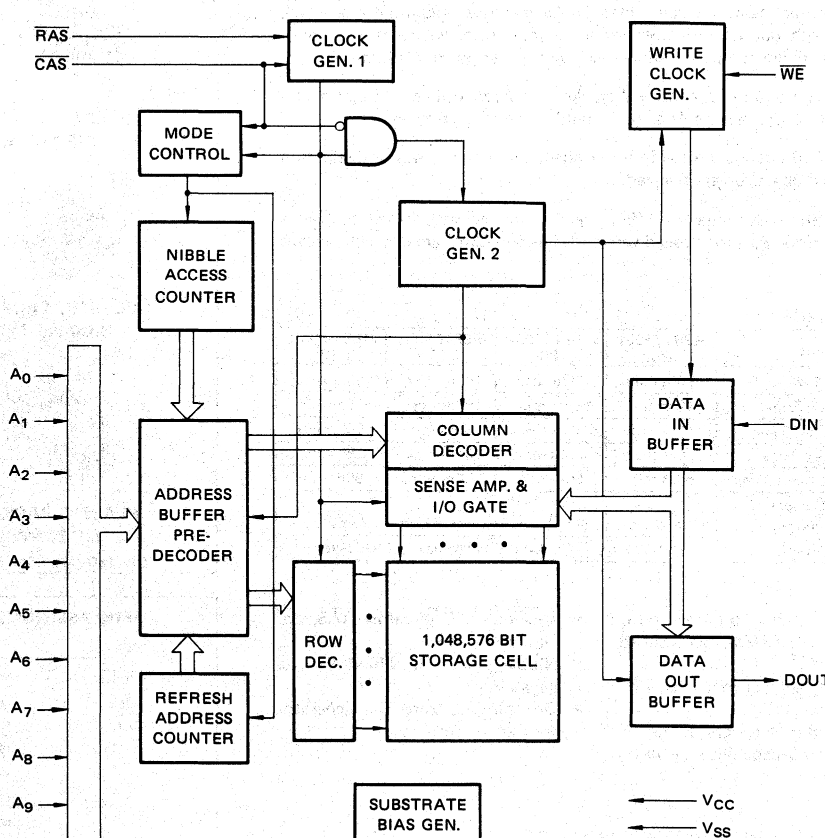
Rating		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} Relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – BLOCK DIAGRAM



CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance, A_0 to A_9, D_{IN}	C_{IN1}		5	pF
Input Capacitance, $\overline{RAS}$ $\overline{CAS}$, $\overline{WE}$	C_{IN2}		5	pF
Output Capacitance, D_{OUT}	C_{OUT}		5	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input High Voltage, All inputs	V_{IH}	2.4	–	6.5	V	
Input Low Voltage, All inputs	V_{IL}	-2.0	–	0.8	V	

2

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

Parameter		Conditions	Symbol	Values		Unit
				Min	Max	
Operating Current* (Average power supply current)	MB81C1001-70	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	I_{CC1}		75	mA
	MB81C1001-80				70	
	MB81C1001-10				60	
	MB81C1001-12				50	
Standby Current (Power supply current)	TTL level	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	I_{CC2}		2.0	mA
	CMOS level	$\overline{RAS}$ = $\overline{CAS}$ $\geqq V_{CC}-0.2V$			1.0	
Refresh Current 1* (Average power supply current)	MB81C1001-70	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	I_{CC3}		70	mA
	MB81C1001-80				65	
	MB81C1001-10				55	
	MB81C1001-12				45	
Nibble Mode Current*	MB81C1001-70	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min	I_{CC4}		45	mA
	MB81C1001-80				45	
	MB81C1001-10				35	
	MB81C1001-12				25	
Refresh Current 2* (Average power current)	MB81C1001-70	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	I_{CC5}		70	mA
	MB81C1001-80				65	
	MB81C1001-10				55	
	MB81C1001-12				45	
Input Leakage Current		$0V \leqq V_{IH} \leqq 5.5V$, $4.5V \leqq V_{CC} \leqq 5.5V$, V_{SS} = 0V; pins not under test = 0V	$I_{I(L)}$	-10	10	µA
Output Leakage Current		$0V \leqq V_{OUT} \leqq 5.5V$; Data out disabled	$I_{O(L)}$	-10	10	
Output High Voltage		I_{OH} = -5mA	V_{OH}	2.4		V
Output Low Voltage		I_{OL} = 4.2mA	V_{OL}		0.4	

NOTE: * I_{CC} depends on the output load conditions and cycle rate. The specified values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1,2,3

No.	Parameter NOTE	Symbol	MB81C1001-70		MB81C1001-80		MB81C1001-10		MB81C1001-12		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh	t_{REF}		8.2		8.2		8.2		8.2	ms
2	Random Read/Write Cycle Time	t_{RC}	140		155		180		210		ns
3	Read-Modify-Write Cycle Time	t_{RWC}	167		182		210		245		ns
4	Access Time from $\overline{RAS}$ [4] [7]	t_{RAC}		70		80		100		120	ns
5	Access Time from $\overline{CAS}$ [5] [7]	t_{CAC}		25		25		30		35	ns
6	Access Time from Column Address [6] [7]	t_{AA}		43		45		50		60	ns
7	Output Data Hold Time	t_{OH}	7		7		7		7		ns
8	Output Buffer Turn on Delay Time	t_{ON}	5		5		5		5		ns
9	Output Buffer Turn Off Delay Time [8]	t_{OFF}		25		25		25		25	ns
10	Transition Time	t_{T}	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time	t_{RP}	60		65		70		80		ns
12	$\overline{RAS}$ Pulse Width	t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time	t_{RSH}	25		25		30		35		ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		0		0		ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time [9] [10]	t_{RCD}	20	45	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width	t_{CAS}	25		25		30		35		ns
17	$\overline{CAS}$ Hold Time	t_{CSH}	70		80		100		120		ns
18	$\overline{CAS}$ Precharge Time ($\overline{C}$-B-$\overline{R}$ Cycle) [15]	t_{CPN}	15		15		15		15		ns
19	Row Address Set Up Time	t_{ASR}	0		0		0		0		ns
20	Row Address Hold Time	t_{RAH}	10		12		15		15		ns
21	Column Address Set Up Time	t_{ASC}	0		0		0		0		ns
22	Column Address Hold Time	t_{CAH}	15		15		15		20		ns
23	$\overline{RAS}$ to Column Address Delay Time [11]	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	43		45		50		60		ns
25	Read Command Set Up Time	t_{RCS}	0		0		0		0		ns

2

AC CHARACTERISTICS (Cont'd)

(At recommended operating conditions unless otherwise noted.) Notes 1,2,3

No.	Parameter NOTE	Symbol	MB81C1001-70		MB81C1001-80		MB81C1001-10		MB81C1001-12		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
26	Read Command Hold Time Referenced to RAS [12]	t_{RRH}	0		0		0		0		ns
27	Read Command Hold Time Referenced to CAS [12]	t_{RCH}	0		0		0		0		ns
28	Write Command Set Up Time [13]	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time	t_{WCH}	15		15		15		20		ns
30	WE Pulse Width	t_{WP}	15		15		15		20		ns
31	Write Command to RAS Lead Time	t_{RWL}	22		22		25		30		ns
32	Write Commnd to CAS Lead Time	t_{CWL}	17		17		20		25		ns
33	D_{IN} Set Up Time	t_{DS}	0		0		0		0		ns
34	D_{IN} Hold time	t_{DH}	15		15		15		20		ns
35	RAS to WE Delay Time [13]	t_{RWD}	70		80		100		120		ns
36	CAS to WE Delay Time [13]	t_{CWD}	25		25		30		35		ns
37	Column Address to WE Delay Time [13]	t_{AWD}	43		45		50		60		ns
38	RAS Precharge Time to CAS Active Time (Refresh Cycles)	t_{RPC}	0		0		0		0		ns
39	CAS Set Up Time for CAS-before-RAS Refresh	t_{CSR}	0		0		0		0		ns
40	CAS Hold Time for CAS-before-RAS Refresh	t_{CHR}	15		15		15		20		ns
41	Access Time from CAS (Counter Test Cycle)	t_{CAT}		43		45		50		60	ns
50	Nibble Mode Read/Write Cycle Time	t_{NC}	50		50		55		60		ns
51	Nibble Mode Read-Modify-Write Cycle Time	t_{NRWC}	67		67		75		85		ns
52	Access Time from CAS Precharge [7] [14]	t_{NPA}		45		45		50		55	ns
53	Nibble Mode CAS Precharge Time	t_{NCP}	15		15		15		15		ns

NOTES:

1 An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

2 AC characteristics assume t_T = 5 ns.

3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

4 Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 2 and 3.

5 If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA}$-t_{CAC}-t_T, access time is t_{CAC}.

6 If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA}$-t_{CAC}-t_T, access time is t_{AA}.

7 Measured with a load equivalent to two TTL loads and 100 pF.

8 t_{OFF} is specified that output buffer changes to high impedance state.

9 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

10 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).

11 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

12 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

13 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restructive operating parameter. They are included in the data sheet as the electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin.
If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear at the D_{OUT} pin, and write operation can be executed by satisfing t_{RWL}, t_{CWL}, t_{RAL} specifications.

14 t_{NPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{NCP} is long, t_{NPA} is longer than t_{NPA} (max).

15 Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only

Fig. 2 — t_{RAC} vs t_{RCD}

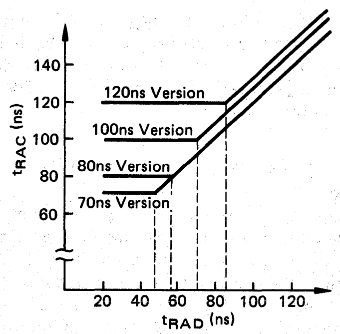
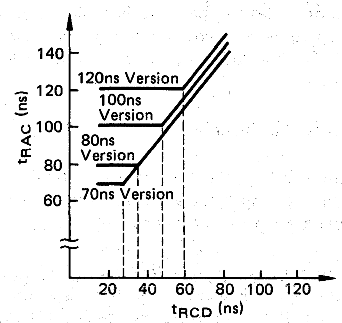


Fig. 3 — t_{RAC} vs t_{RAD}



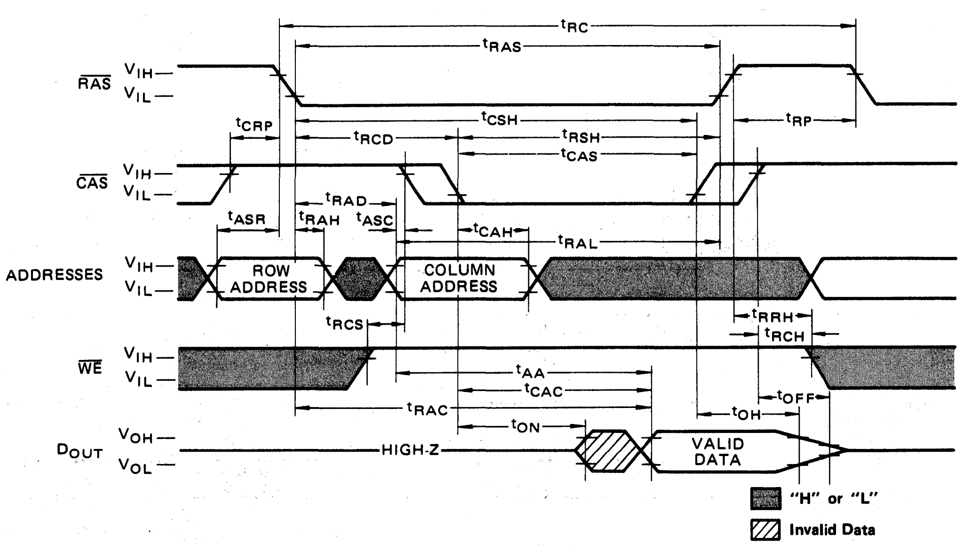
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	–	–	–	High-Z	–	
Read Cycle	L	L	H	Valid	Valid	–	Valid	○ *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	○ *	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	Valid	Valid	X→ Valid	Valid	○ *	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	–	–	High-Z	○	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	L	L	X	–	–	–	High-Z	○	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H→L	L	X	–	–	–	Valid	○	Previous data is kept.

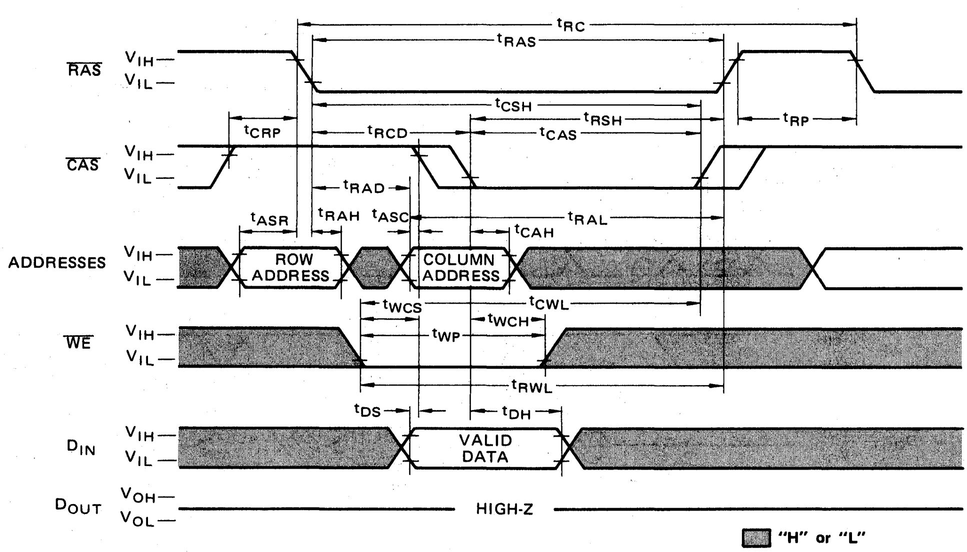
X; "H" or "L"
* ; It is impossible in nibble mode.

2

Read Cycle

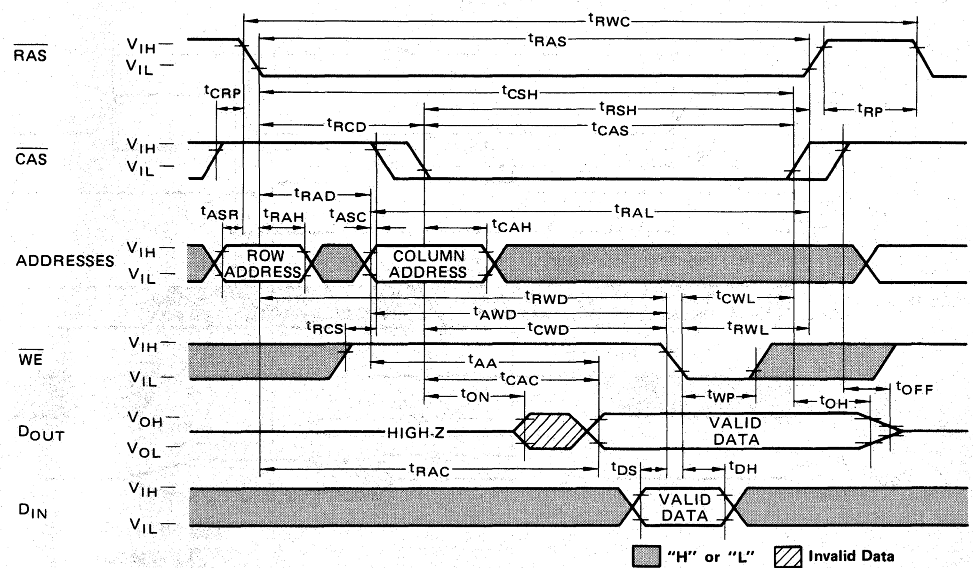


Write Cycle (Early Write)

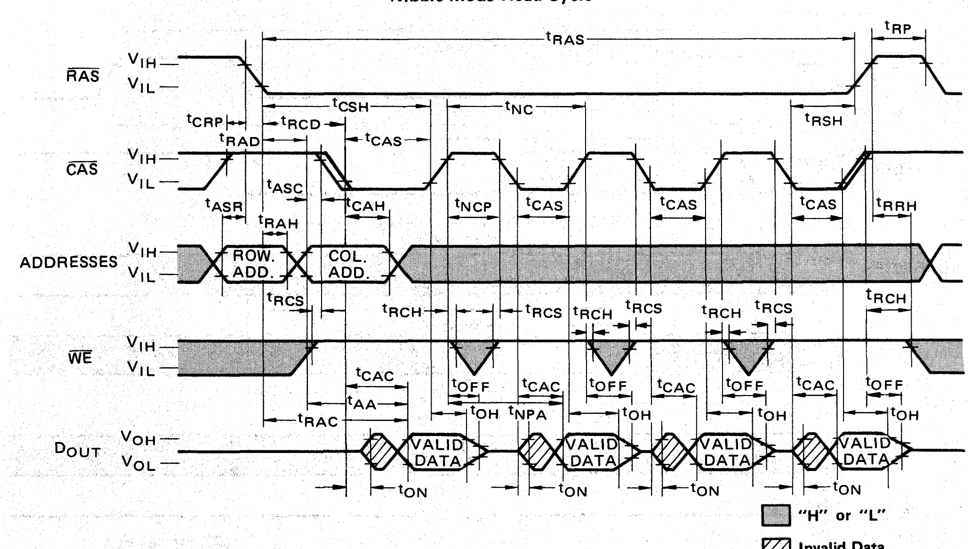


2

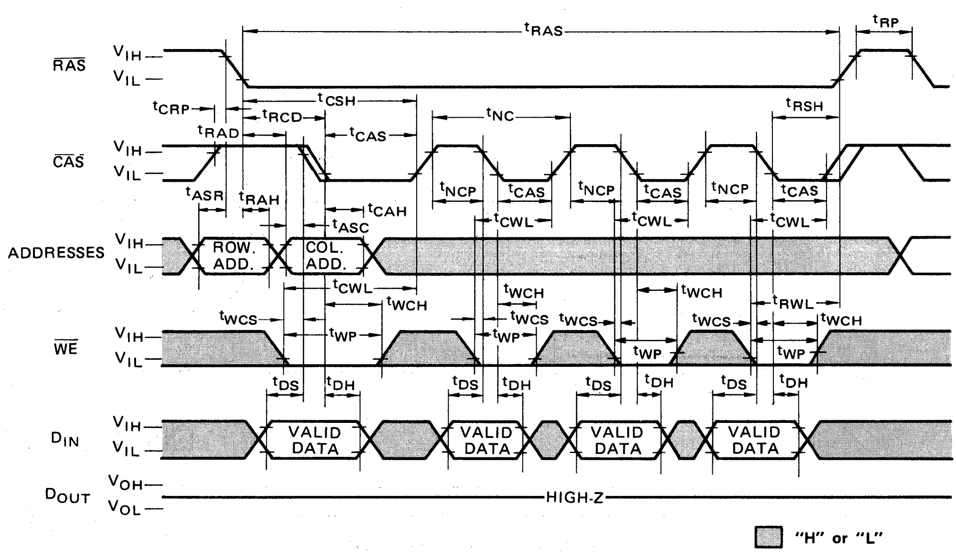
Read-Write/Read-Modify-Write Cycle



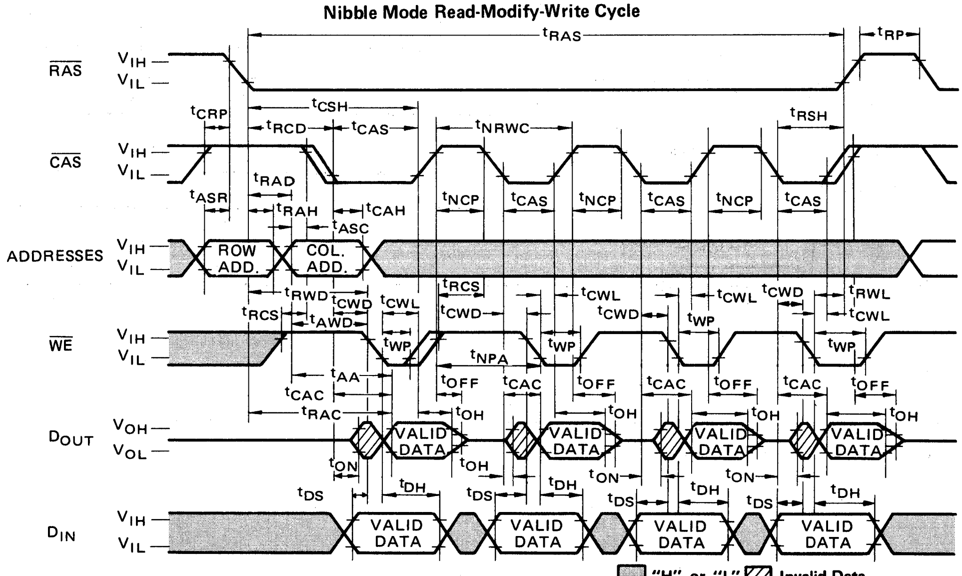
Nibble Mode Read Cycle



Nibble Mode Write Cycle (Early Write)

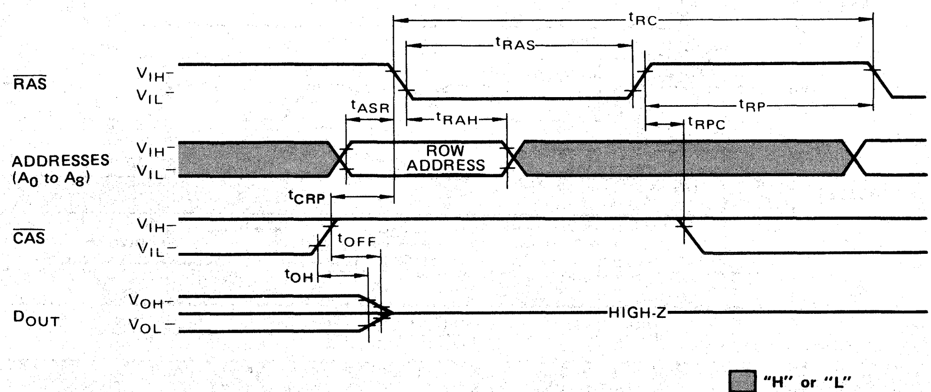


Nibble Mode Read-Modify-Write Cycle



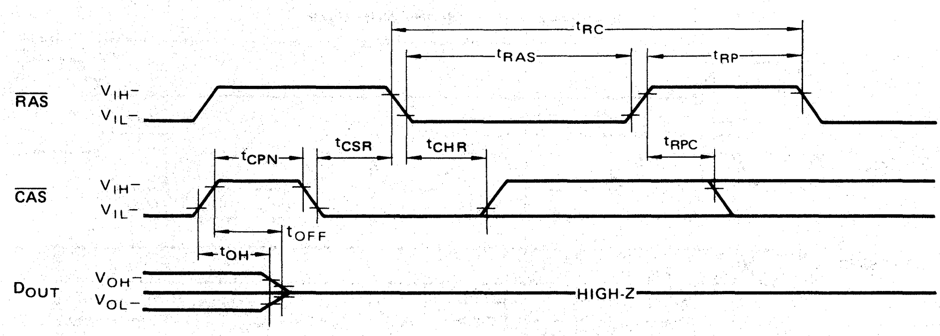
$\overline{RAS}$-Only Refresh Cycle

NOTE: $\overline{WE}$, D_{IN} = "H"or"L", A_9 = V_{IH} or V_{IL}

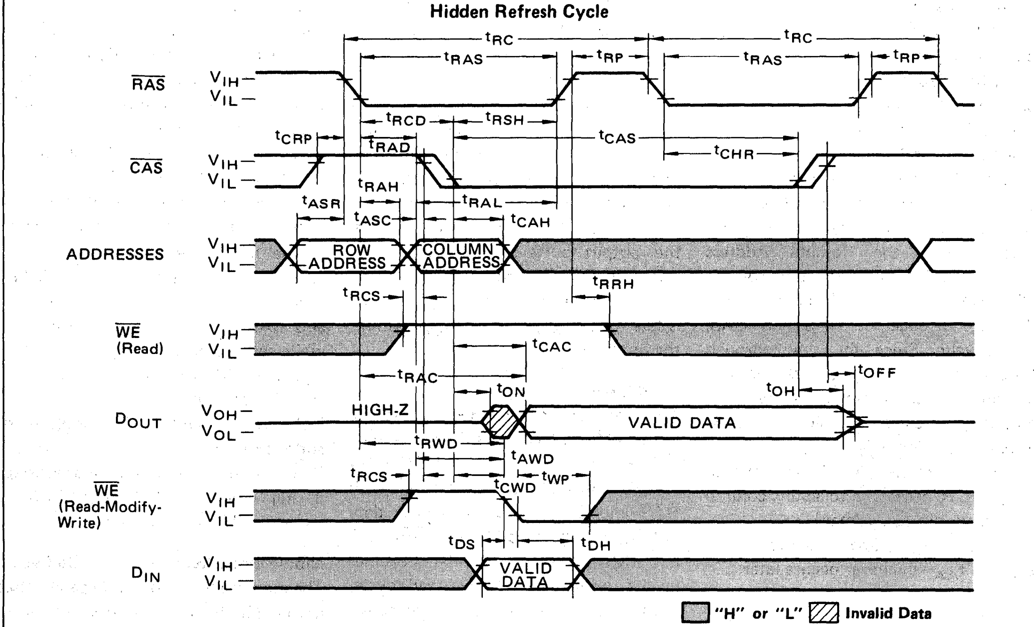


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

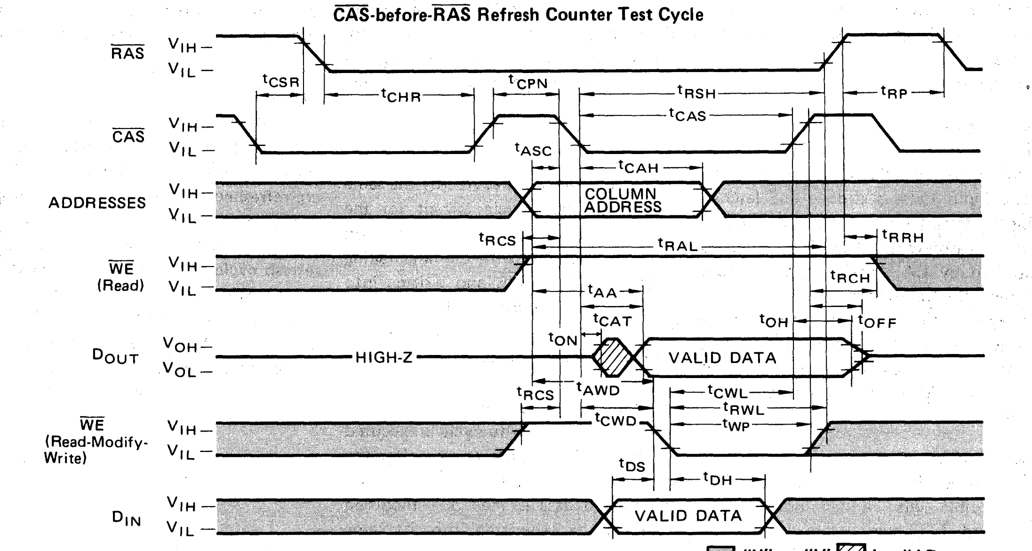
NOTE: Address, $\overline{WE}$, D_{IN} = "H"or"L"



Hidden Refresh Cycle



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:
A total of twenty binary input address bits are required to decode any one of the 1,048,576 storage cells within the MB 81C1001. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe ($\overline{RAS}$). The ten column address bits are established on the address input pin (A_0 to A_9) and latched with the Column Address Strobe ($\overline{CAS}$). All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min) + t_T.
Therefore, to get valid data within t_{RAC}, it is necessary to apply column address within t_{RAD} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occure later.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. Data input is ignored during read cycle. Data output is high impedance state during write cycle.

Data Input:
Data is written into the MB 81C1001 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-modify-write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is high impedance state until $\overline{CAS}$ is brought low. In a read or read-modify-write cycle, the output becomes valid after t_{RAC} from the falling edge of $\overline{CAS}$ when t_{RCD} (max) is satisfied or after t_{CAC} when t_{RCD} is longer than t_{RCD} (max). The data output remains valid until $\overline{CAS}$ returns to high with t_{OH} and becomes high impedance state after t_{OFF}. In an early write cycle, the output buffer is high impedance state during the entire cycle. In a delayed write cycle, if t_{RWD} or t_{CWD} is less than t_{RWD} (min) or t_{CWD} (min), the output is invalid.

Read Cycle:
The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" through-out the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output is remain valid with $\overline{CAS}$ "L", i.e., if $\overline{CAS}$ goes "H", the data becomes invalid with t_{OH}. During read cycle, the D_{IN} pin is "Don't Care". The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), or Column address input (t_{AA}). If t_{RCD} ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}.

Write Cycle:
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and D_{IN} pin. The data on D_{IN} pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL} and t_{RAL} must be satisfied the specifications.

Read-Modify-Write Cycle:;
The read-modify-write cycle is executed by changing $\overline{WE}$ high to low after the data appears at the D_{OUT} pin. After the current data is read out, modified data can be re-written into the same address quickly.

Nibble Read/Write Cycle:
Nibble mode allows high speed serial read, write, or read-modify-write access of 2, 3, or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 9 row and 9 column addresses. The 2 bits of addresses (RA9 and CA9) are used to select one of four nibble bits for initial access. After the first bits is accessed by normal mode, the remaining nibble bits can be accessed by toggling $\overline{CAS}$ "H" then "L". Toggling $\overline{CAS}$ causes RA9 and CA9 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access.
Refer to the table 1 for nibble mode address sequence.
If more than four bits are accessed during nibble mode, the address sequence will begin to repeat.

Nibble Mode Read-Modify-Write Cycle:
The read-modify-write cycle can be used during nibble mode as well as normal mode operation. During the nibble mode, all combinations of read, write, and read-modify-write cycle can be applied as well as normal mode operation.

Refresh:
The refresh of DRAM is executed by normal read, write or read-modify-write cycle, i.e., the cells on the one row line are refreshed by executing one of three cycles. 1024 row address must be refreshed every 8.2 ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB 81C10001 also has three types of refresh modes, $\overline{RAS}$-Only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and Hidden refresh.

1. **$\overline{\text{RAS}}$-Only Refresh;**
The $\overline{\text{RAS}}$-Only refresh is executed by keeping $\overline{\text{RAS}}$ "L" and keeping $\overline{\text{CAS}}$ "H" through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$-Only refresh, the D_{OUT} pin is kept high impedance state.

2. **$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh;**
The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is executed by bringing $\overline{\text{CAS}}$ "L" before $\overline{\text{RAS}}$. By this timing combination, the MB 81C1001 executes $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh. The row address input is not necessary because it is generated internally.

3. **Hidden Refresh;**
The Hidden refresh is executed by keeping $\overline{\text{CAS}}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{\text{CAS}}$ is kept low continuousely from previous cycle, followed refresh cycle should be $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh.

Table 1 — NIBBLE MODE ADDRESS SEQUENCE

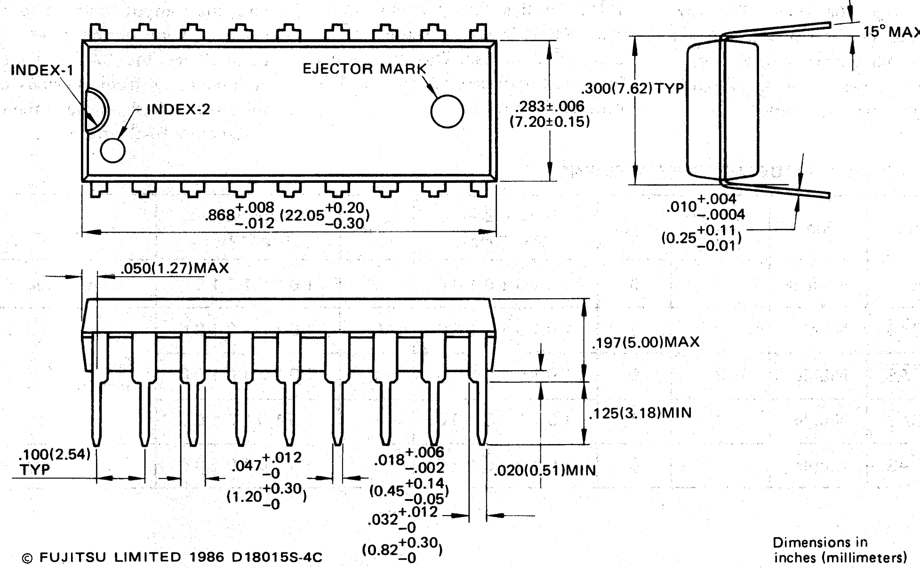
Sequence	Mode	Nibble bit	RA_9	Row address ($A_8 \sim A_0$)	CA_9	Column address ($A_8 \sim A_0$)	
$\overline{\text{RAS}}$/$\overline{\text{CAS}}$	Normal	1	0	101010100	0	101010100	Input address
Toggle $\overline{\text{CAS}}$	Nibble	2	1	101010100	0	101010100	
Toggle $\overline{\text{CAS}}$	Nibble	3	0	101010100	1	101010100	Generated Internally
Toggle $\overline{\text{CAS}}$	Nibble	4	1	101010100	1	101010100	
Toggle $\overline{\text{CAS}}$	Nibble	1	0	101010100	0	101010100	Sequence repeats

2

PACKAGE DIMENSIONS

(Suffix: -P)

18 LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M04)



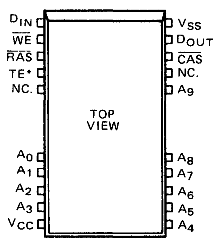
Dimensions in inches (millimeters)

2

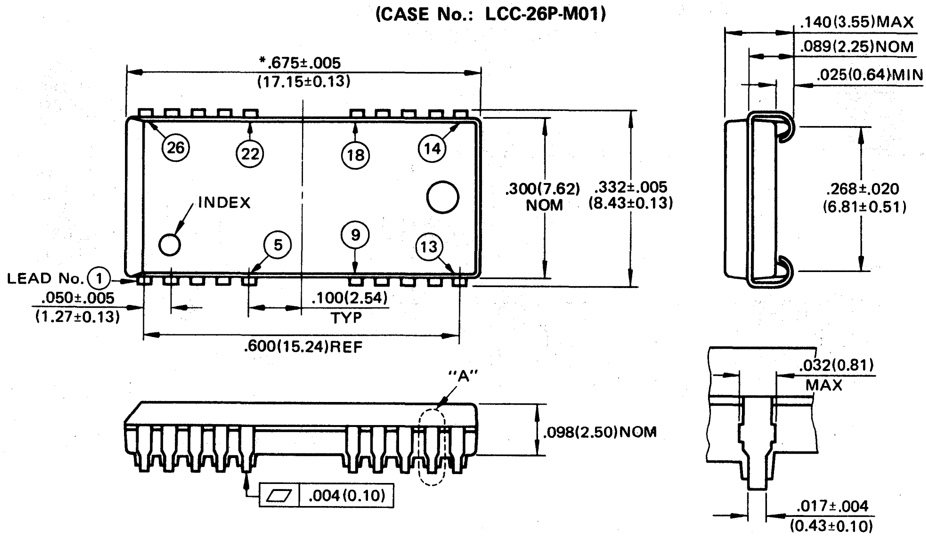
PACKAGE DIMENSIONS

(Suffix: -PJ)

PIN ASSIGNMENT



26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M01)



NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package. Foot-print compatible with "SOJ-26", LCC-26C-A01)

Dimensions in inches (millimeters)

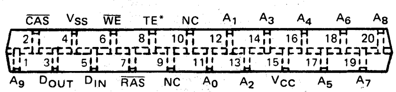
2

PACKAGE DIMENSIONS

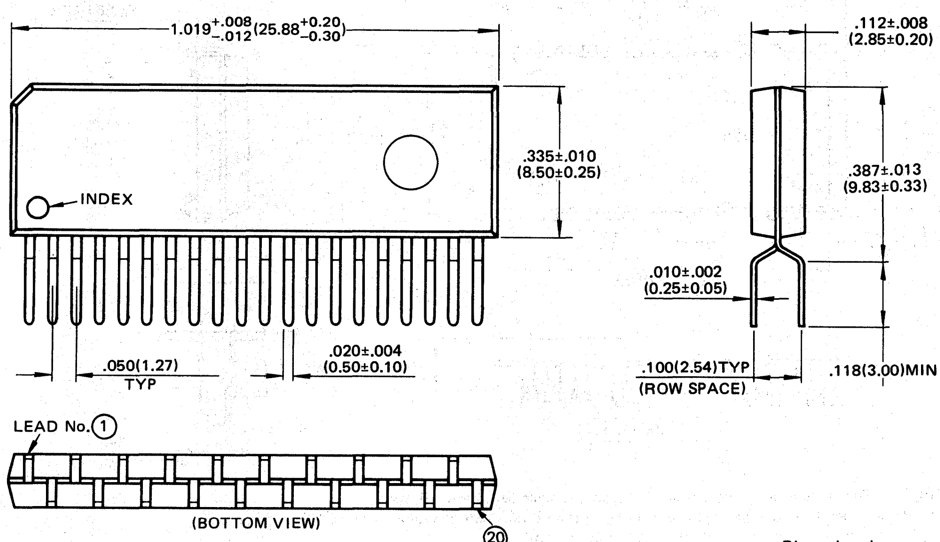
(Suffix:-PSZ)

PIN ASSIGNMENT

(TOP VIEW)



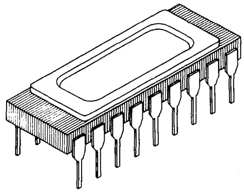
20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)



Dimensions in
inches (millimeters)

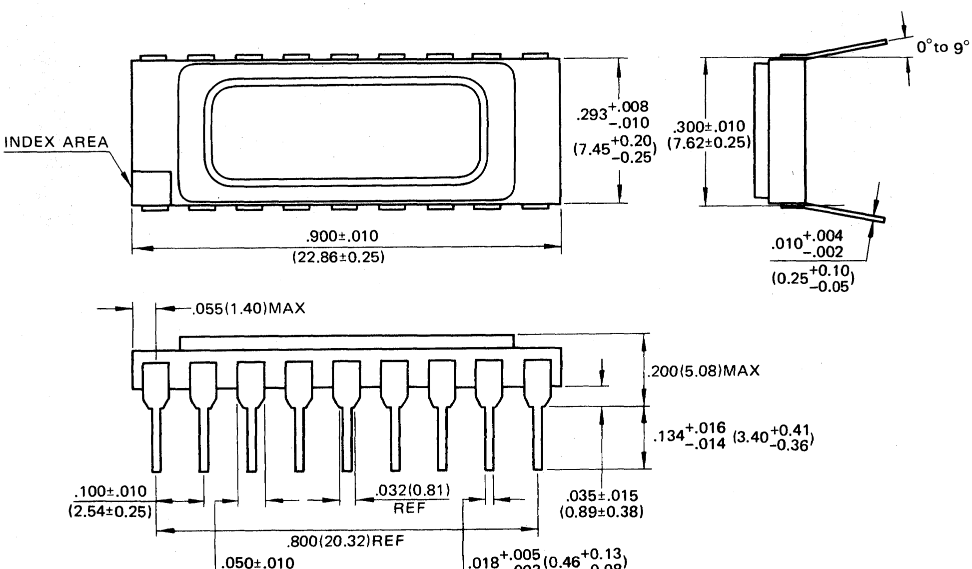
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-18C-A01

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



Dimensions in
inches (millimeters)

FUJITSU

CMOS 1,048,576 BIT STATIC COLUMN DYNAMIC RAM

MB81C1002-85
MB81C1002-10
MB81C1002-12

December 1988
Edition 1.0

CMOS 1,048576 X 1 BIT Static Column Mode Dynamic RAM

The Fujitsu MB81C1002 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1002 has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1002 High α-ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

The CMOS standby current is about one-fifth that of the conventional NMOS DRAM, so large-capacity memory systems shuch as semiconductor disks with less power and battery backup becomes possible, i.e., low standby current makes the RAM applicable as non-volatile memories.

DIP-18P-M04

DIP-18C-A01

LCC-26P-M01

ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C1002-85	MB81C1002-10	MB81C1002-12
Row Access Time	85ns max.	100ns max.	120ns max.
Random Cycle Time	160ns min.	180ns min.	210ns min.
Column Address Time	50ns max.	50ns max.	60ns max.
Column Access Time	25ns max.	30ns max.	35ns max.
Static Column Mode Cycle Time	55ns min.	55ns min.	65ns min.
Low Power Dissipation			
• Operating current	358mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level) /5.5mW max. (CMOS level)		

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Static column Mode, Read-Modify-Write capacity
- On chip substrate bias generator for high performance

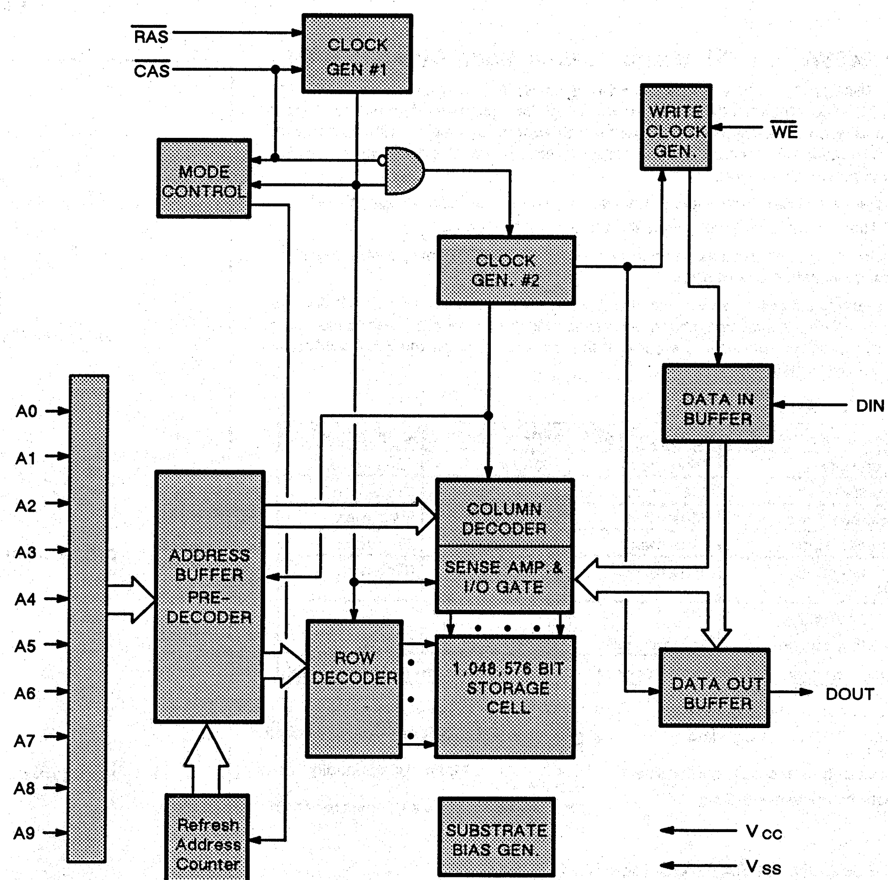
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		--	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB81C1002 DYNAMIC RAM—BLOCK DIAGRAM

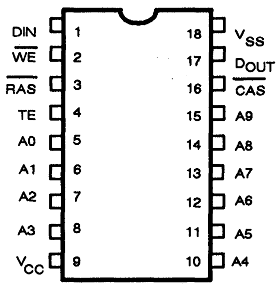


CAPACITANCE (T_A = 25°C, f = 1MHz)

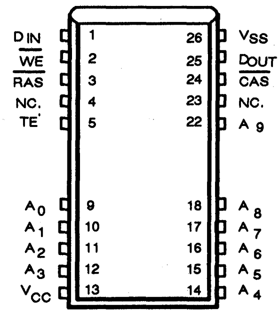
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

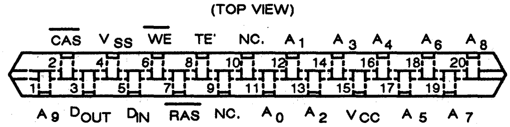
18-Pin DIP:
(TOP VIEW)



26-Pin SOJ:
(TOP VIEW)



20-Pin ZIP:
(TOP VIEW)



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available)
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

(All voltages referenced to ground; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	VSS	0	0	0	
Input High Voltage, all inputs	VIH	2.4	—	6.5	V
Input Low Voltage, all inputs	VIL	-2.0	—	0.8	V

Note: Undershoots of up to -2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0-through-A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Data is written into the MB81C1002 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-modify-write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

STATIC COLUMN MODE OF OPERATION

The static column mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static column mode, $\overline{RAS}$ can be kept low throughout static column mode operation. The following four cycles are allowed in the static column mode.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Conditions	Values			Unit
				Min	Typ	Max	
Output high voltage		V_{OH}	IOH = -5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V $\leq$ VIN $\leq$ 5.5V; 4.5V $\leq$ VCC $\leq$ 5.5V; VSS=0V;All other pins under test =0V	-10	—	10	µA
Output leakage current		$I_{O(L)}$	0V $\leq$ VOUT $\leq$ 5.5V; Data out disabled	-10	—	10	
Operating current (Average power supply current)	MB81C1002-85	ICC_1 (Note)	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	65	mA
	MB81C1002-10					60	
	MB81C1002-12					50	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	2.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ $\geq$ VCC-0.2V			1.0	
Refresh current #1 (Average power supply current)	MB81C1002-85	ICC_3 (Note)	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC} = min	—	—	60	mA
	MB81C1002-10					55	
	MB81C1002-12					45	
Static column mode current	MB81C1002-85	ICC_4 (Note)	$\overline{RAS}$ = $\overline{CAS}$ =VIL cycling; t_{SC} = min	—	—	30	mA
	MB81C1002-10					30	
	MB81C1002-12					23	
Refresh current #2 (Average power supply current)	MB81C1002-85	ICC_5 (Note)	$\overline{RAS}$ cycling ; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	60	mA
	MB81C1002-10					55	
	MB81C1002-12					45	

Note: ICC depends on output load conditions, input levels, and cycle rates; the value of ICC is also a function of the input low voltage level with VILD $\geq$ -0.5V. All specified values are measured with the output open.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB81C1002-85		MB81C1002-10		MB81C1002-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	Time Between Refresh	t_{REF}	—	8.2	—	8.2	—	8.2	ms	—
2	Random Read/Write Cycle Time	t_{RC}	160	—	180	—	210	—	ns	—
3	Read-Modify-Write Cycle Time	t_{RWC}	190	—	210	—	245	—	ns	—
4	Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	4,7
5	Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	30	—	35	ns	7
6	Column Address Access Time	t_{AA}	—	50	—	50	—	60	ns	6,7
7	Output Hold Time	t_{OH}	7	—	7	—	7	—	ns	—
8	Output Buffer Turn on Delay Time	t_{ON}	5	—	5	—	5	—	ns	—
9	Output Buffer Turn off Delay Time	t_{OFF}	—	25	—	25	—	25	ns	8
10	Transition Time	t_{T}	3	50	3	50	3	50	ns	—
11	$\overline{RAS}$ Precharge Time	t_{RP}	65	—	70	—	80	—	ns	—
12	$\overline{RAS}$ Pulse Width	t_{RAS}	85	100000	100	100000	120	100000	ns	—
13	$\overline{RAS}$ Hold Time	t_{RSH}	25	—	30	—	35	—	ns	—
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0	—	0	—	0	—	ns	—
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	60	25	70	25	85	ns	9,10
16	$\overline{CAS}$ Pulse Width	t_{CAS}	25	—	30	—	35	—	ns	—
17	$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	—
18	$\overline{CAS}$ Precharge Time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{CPN}	15	—	15	—	15	—	ns	19
19	Row Address Set Up Time	t_{ASR}	0	—	0	—	0	—	ns	—
20	Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	—
21	Column Address Set Up Time	t_{ASC}	0	—	0	—	0	—	ns	5
22	Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	—
23	$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	35	20	50	20	60	ns	11
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	50	—	60	—	ns	—
25	Read Command Set Up Time	t_{RCS}	0	—	0	—	0	—	ns	—
26	Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	12
27	Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	12
28	Write Command Hold Time	t_{WCH}	20	—	20	—	25	—	ns	—
29	$\overline{WE}$ Pulse Width	t_{WP}	15	—	15	—	20	—	ns	—
30	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	—
31	Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	—
32	DIN Set Up Time	t_{DS}	0	—	0	—	0	—	ns	—
33	DIN Hold Time	t_{DH}	20	—	20	—	25	—	ns	—

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB81C1002-85		MB81C1002-10		MB81C1002-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
34	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{RWD}	85	—	100	—	120	—	ns	13, 18
35	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{CWD}	25	—	30	—	35	—	ns	13
36	Column Address to $\overline{\text{WE}}$ Delay Time	t_{AWD}	50	—	50	—	60	—	ns	13
37	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh Cycles)	t_{RPC}	0	—	0	—	0	—	ns	—
38	$\overline{\text{CAS}}$ Set Up Time for $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh	t_{CSR}	0	—	0	—	0	—	ns	—
39	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh	t_{CHR}	15	—	15	—	20	—	ns	—
40	Access Time from $\overline{\text{CAS}}$ (Counter Test Cycle)	t_{CAT}	—	50	—	50	—	60	ns	—
50	Static Column Mode Read/Write Cycle Time	t_{SC}	55	—	55	—	65	—	ns	—
51	Static Column Mode Read-Modify-Write Cycle Time	t_{SRWC}	95	—	95	—	115	—	ns	—
52	Static Column Mode $\overline{\text{CAS}}$ Precharge Time	t_{CP}	15	—	15	—	15	—	ns	—
53	Access Time Relative to Last Write	t_{ALW}	—	90	—	90	—	110	ns	14
54	Access Time from $\overline{\text{WE}}$ Precharge	t_{WPA}	—	30	—	30	—	35	ns	—
55	Output Hold Time for Column Address Change	t_{AOH}	10	—	10	—	10	—	ns	—
56	Write Latched Data Hold Time	t_{WOH}	0	—	0	—	0	—	ns	—
57	Column Address Hold Time Referenced to $\overline{\text{RAS}}$ Rising Time	t_{AHR}	15	—	15	—	15	—	ns	15
58	Last Write to Column Address Delay Time	t_{LWAD}	25	40	25	40	30	50	ns	16, 17
59	Column Address Hold Time Referenced to Last Write	t_{AHLW}	83	—	95	—	120	—	ns	—
60	$\overline{\text{RAS}}$ to Second Write Delay Time	t_{RSWD}	85	—	100	—	120	—	ns	—
61	$\overline{\text{WE}}$ Inactive Time	t_{WI}	15	—	15	—	20	—	ns	—
62	Write Set Up Time for Output Disable	t_{WS}	0	—	0	—	0	—	ns	18
63	Write Hold Time for Output Disable	t_{WH}	0	—	0	—	0	—	ns	18

2

Notes:

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=VIH) of 200µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max), and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 2 and 3.
5. Assumes that write cycle only.
6. If $t_{RAD} \geqq t_{RAD}$ (max), access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{CWD} \geqq t_{CWD}$ (min), $t_{RWD} \geqq t_{RWD}$ (min), and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read modify-write cycle and data from the selected cell will apper at the DOUT pin.
If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the DOUT pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
14. Assumes that $t_{LWAD} \leqq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{AWL} will be increased by the amount that t_{LWAD} exceeds the value shown.
15. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
16. Operation within the t_{LWAD} (max) limit insures that t_{AWL} (max) can be met. t_{LWAD}(max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
17. t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T=5ns).
18. t_{WS}, t_{WH} and t_{RWD} are specified as a reference point only. If $t_{WS} \geqq t_{WS}$(min) and $t_{WH} \geqq t_{WH}$(min), the data output pin will remain High-Z state through entire cycle. If it $t_{RWD} \geqq t_{RWD}$(min), the data output will contain data read from the selected cell.
19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only

Fig. 2 – t_{RAC} vs. t_{RCD}

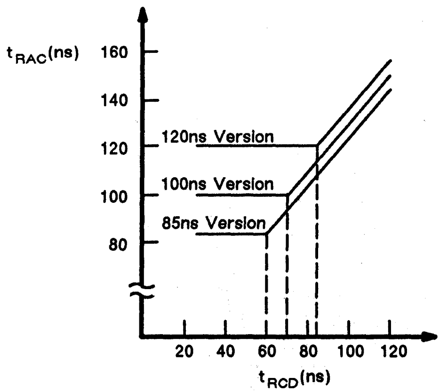
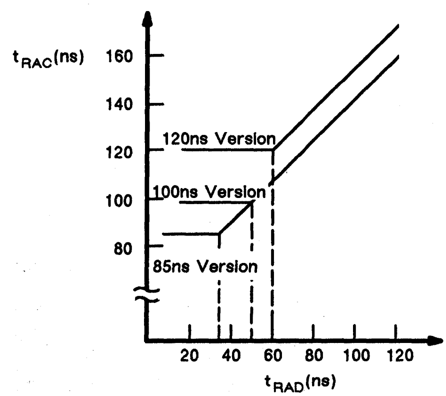


Fig. 3 – t_{RAC} vs. t_{RAD}



FUNCTIONAL TRUTH TABLE

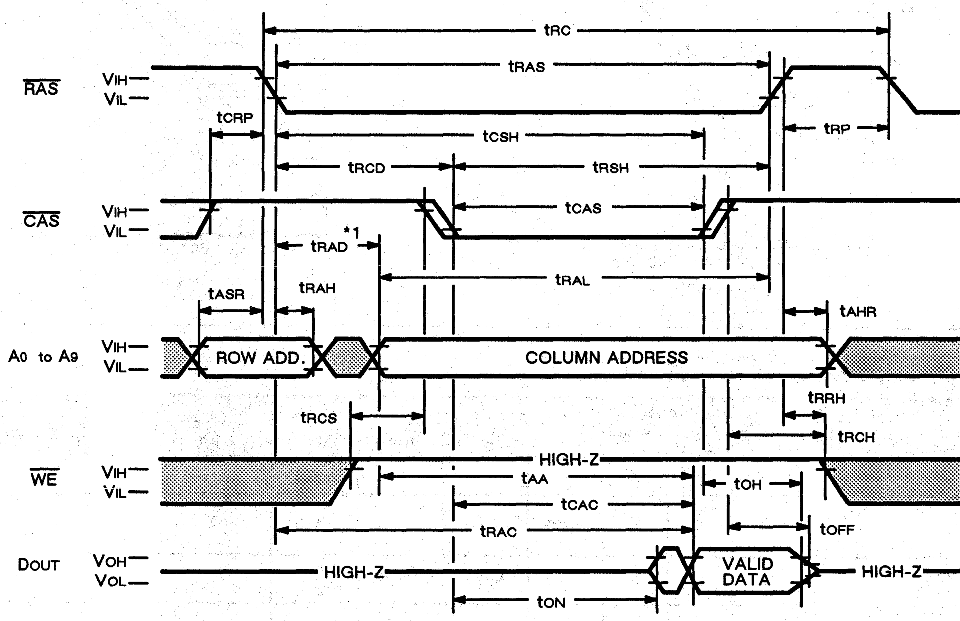
Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	O	$t_{RCS} \geq t_{RCS}$(min) $t_{RCH} \geq t_{RCH}$(min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	*1 High-Z	O	$t_{WS} \geq t_{WS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	Valid	Valid	X→ Valid	Valid	O	$t_{CWD} \geq t_{CWD}$(min)
Static Column Mode Read Cycle	L	L	H	*2 Valid	Valid	—	Valid	X	$t_{RCS} \geq t_{RCS}$(min) $t_{RCH} \geq t_{RCH}$(min)
Static Column Mode Write Cycle	L	L	L	*2 Valid	Valid	Valid	*1 High-Z	X	
Static Column Mode Read-Modify-Write Cycle	L	L	H→L	*2 Valid	Valid	X→ Valid	Valid	X	$t_{CWD} \geq t_{CWD}$(min)
Static Column Mode Mixed Cycle	L	L	L/H	*2 Valid	Valid	Valid	High-Z or Valid	X	
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	—	—	High-Z	O	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	O	
Hidden Refresh Cycle	H→L	L	X	—	—	—	Valid	O	Previous data is kept

Notes:
X : "H" or "L"
*1: If $t_{WS} < t_{WS}$ (min) and $t_{WH} < t_{WH}$ (min), the data output become invalid.
*2: After first cycle, row address is not necessary.

2

TIMING DIAGRAMS

Fig. 4 – READ CYCLE



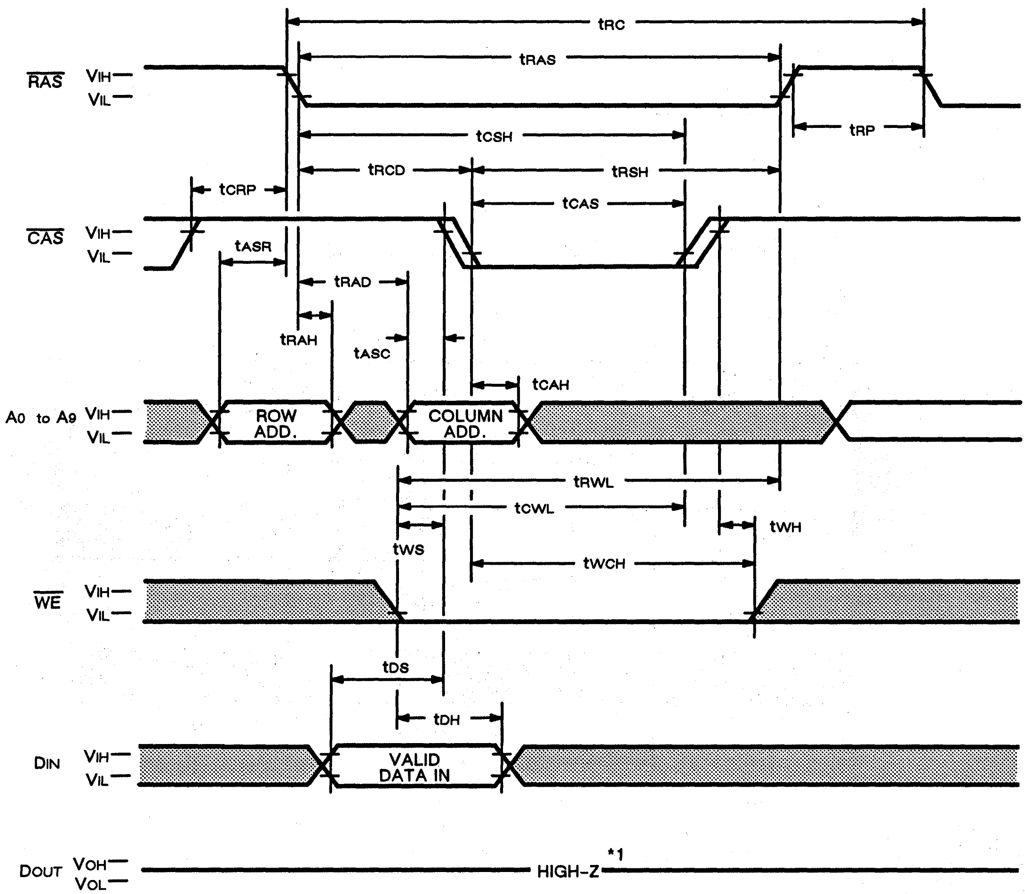
*1; If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occur later.

"H" or "L"

DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" through out the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remain valid with $\overline{CAS}$ "L", i.e., if $\overline{CAS}$ goes "H", the data becomes invalid with t_{OH}. During read cycle, the DIN pin is "H" or "L". The acces time is determined by $\overline{RAS}$(t_{RAC}), $\overline{CAS}$(t_{CAC}), or Column address input(t_{AA}). If t_{RCD} ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC} or t_{AA} whichever occur later.

Fig. 5 - WRITE CYCLE (Early Write)



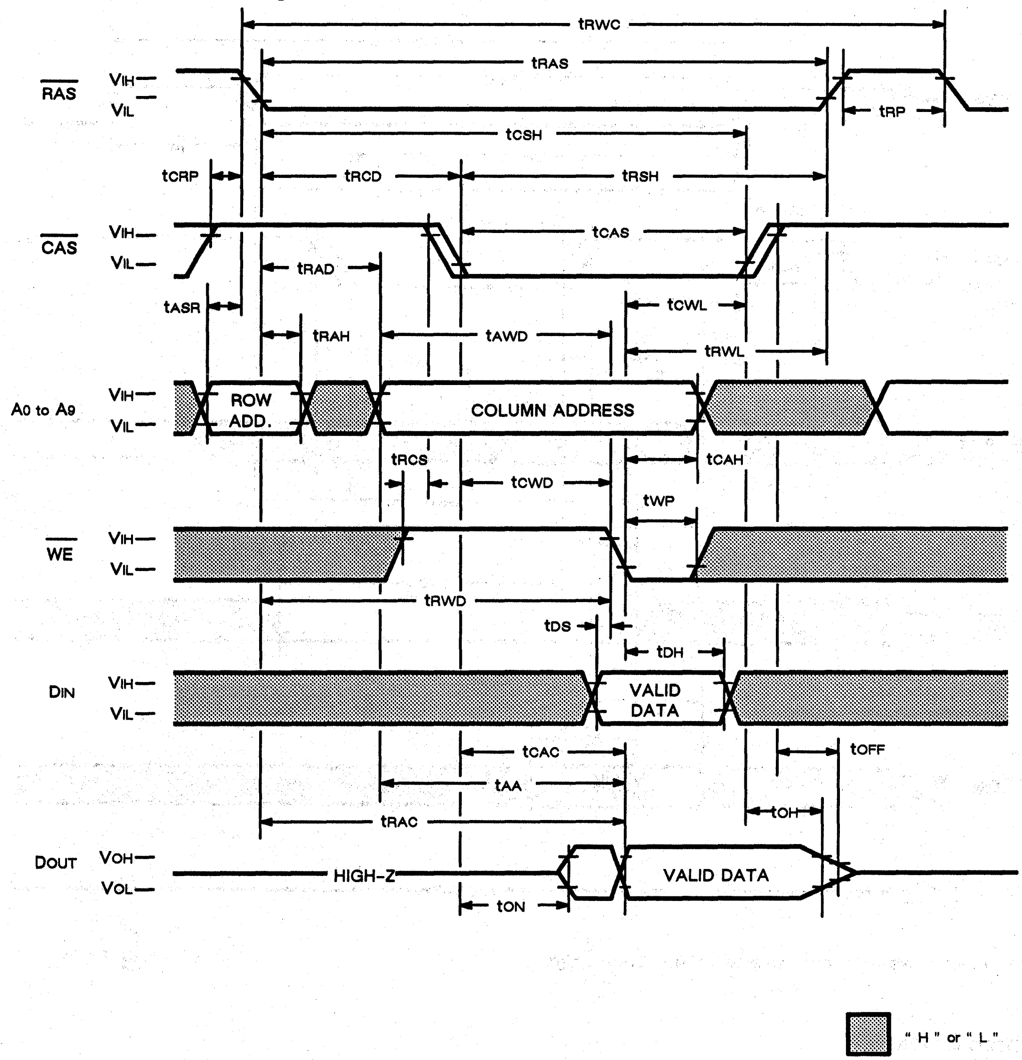
*1; If tWS ≥ tWS (min) and tWH ≥ tWH (min), DOUT is high-Z.

DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pin. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL, tCWL and tRAL must be satisfied the specifications.

2

Fig. 6 – READ WRITE/READ-MODIFY-WRITE CYCLE

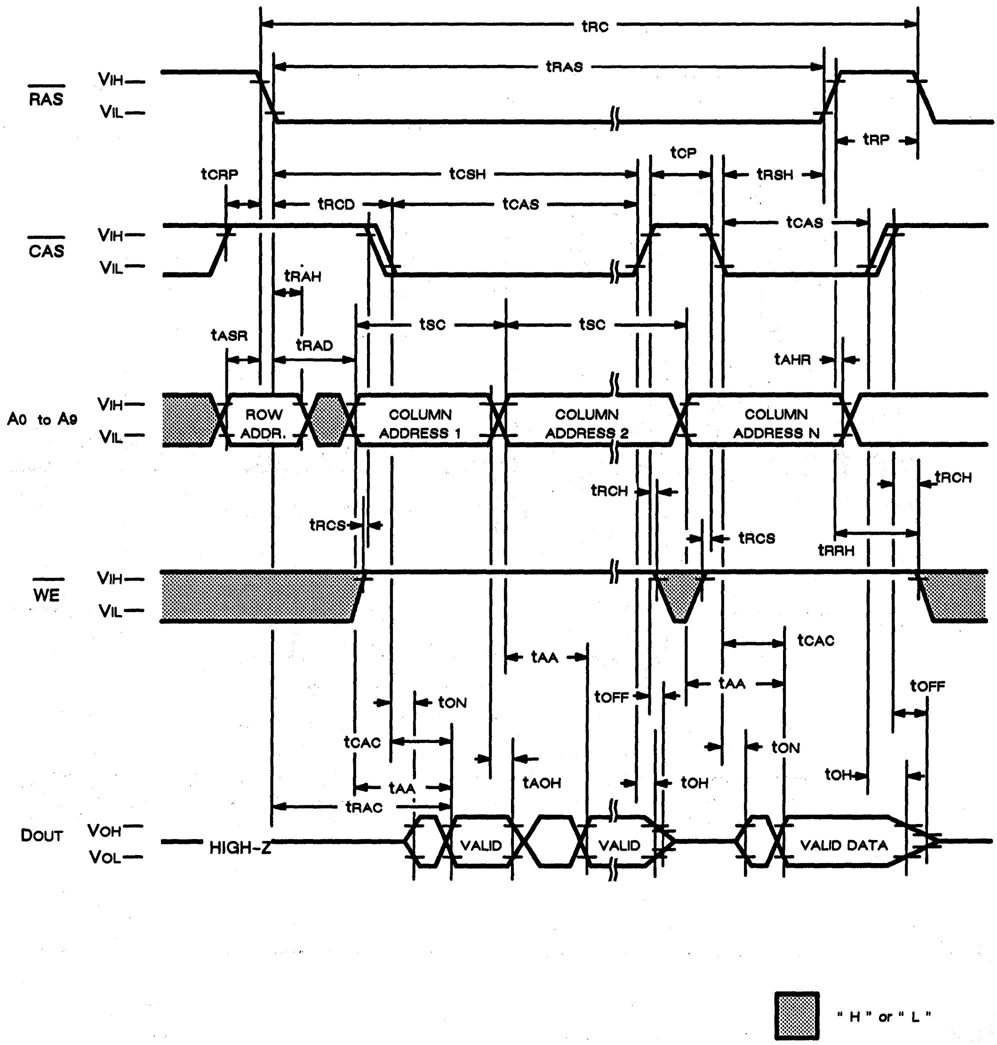


DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DOUT pin. This new data is written into the same address as read out.

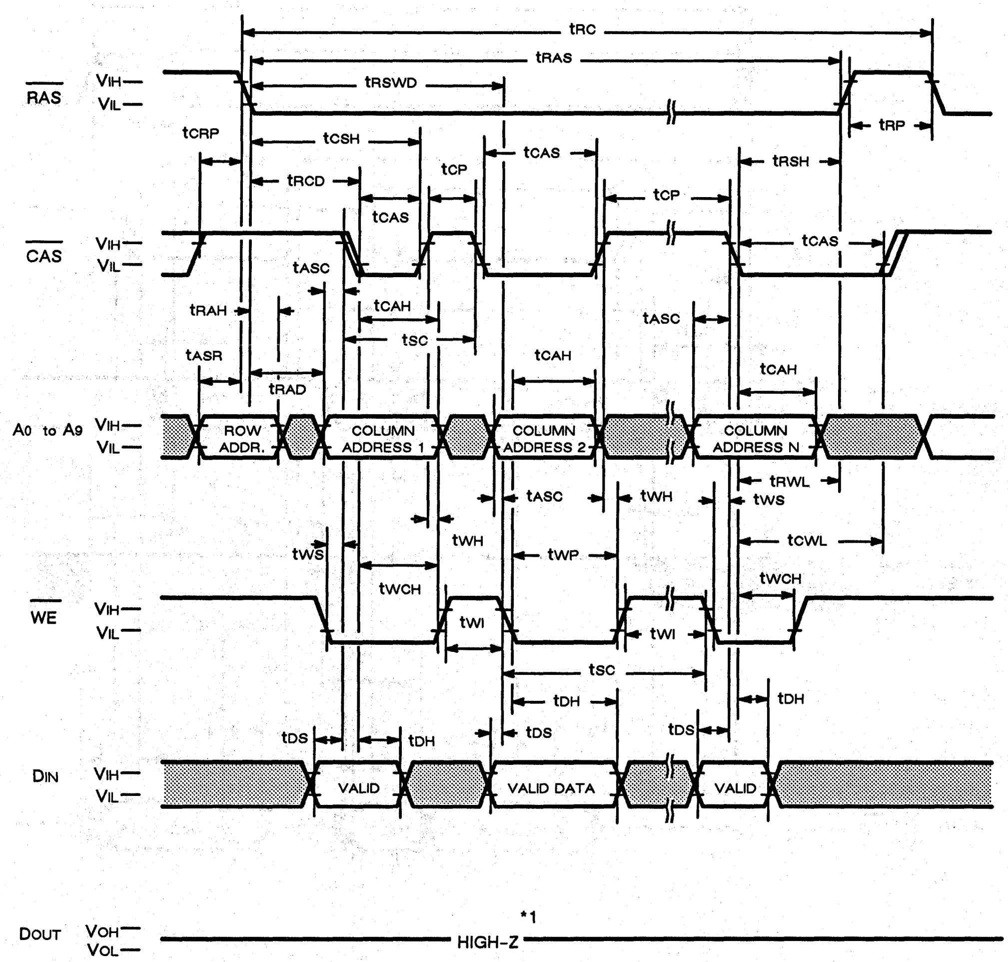
2

Fig. 7 – STATIC COLUMN MODE READ CYCLE



2

Fig. 8 – STATIC COLUMN MODE WRITE CYCLE



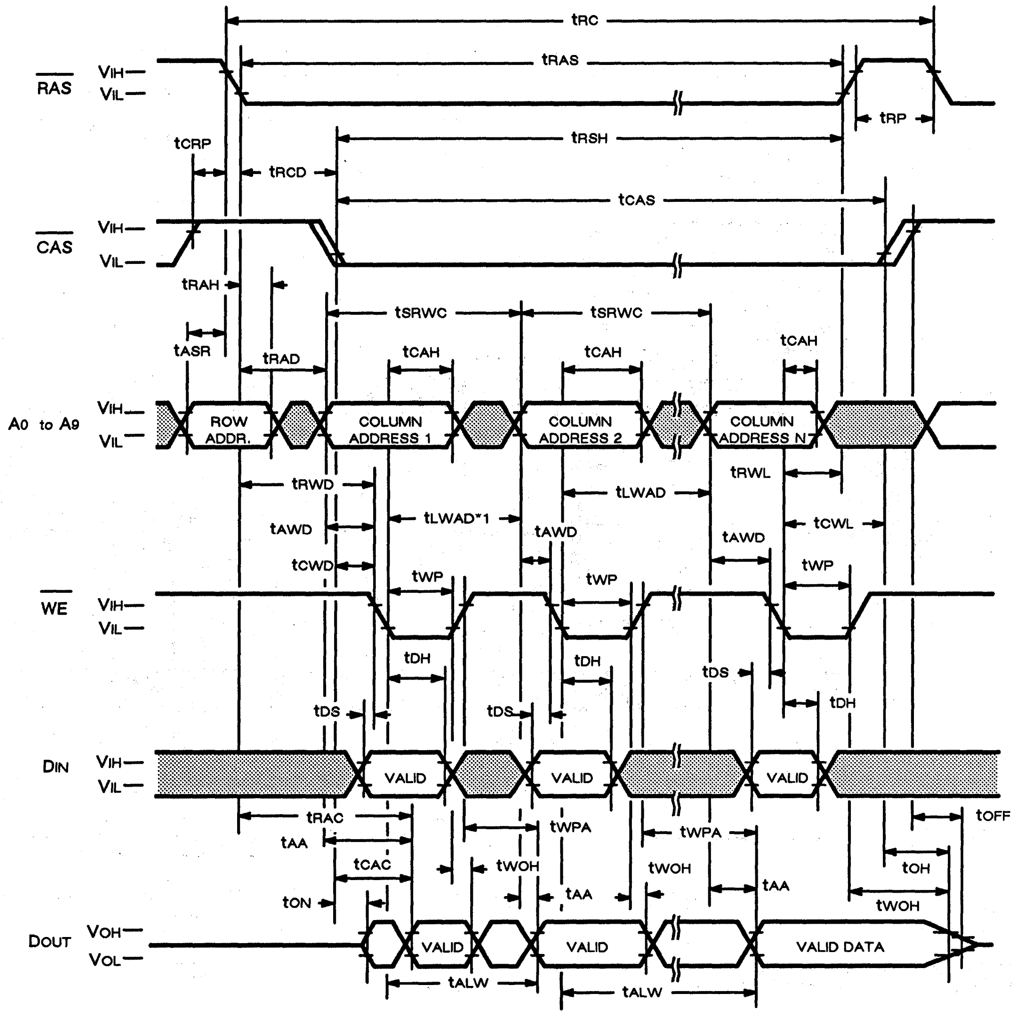
*1; If tWS ≥ tWS (min) and tWH ≥ tWH (min), DOUT is high-Z.

DESCRIPTION

In a static column mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both tWS and tWH are greater than their minimum limits, the data output pin is kept high impedance state through the static column mode write cycle.

2

Fig. 9 – STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



*1; If tLWAD (min) ≦ tLWAD ≦ tLWAD (max), tALW = tSC (min) + tAA (max).

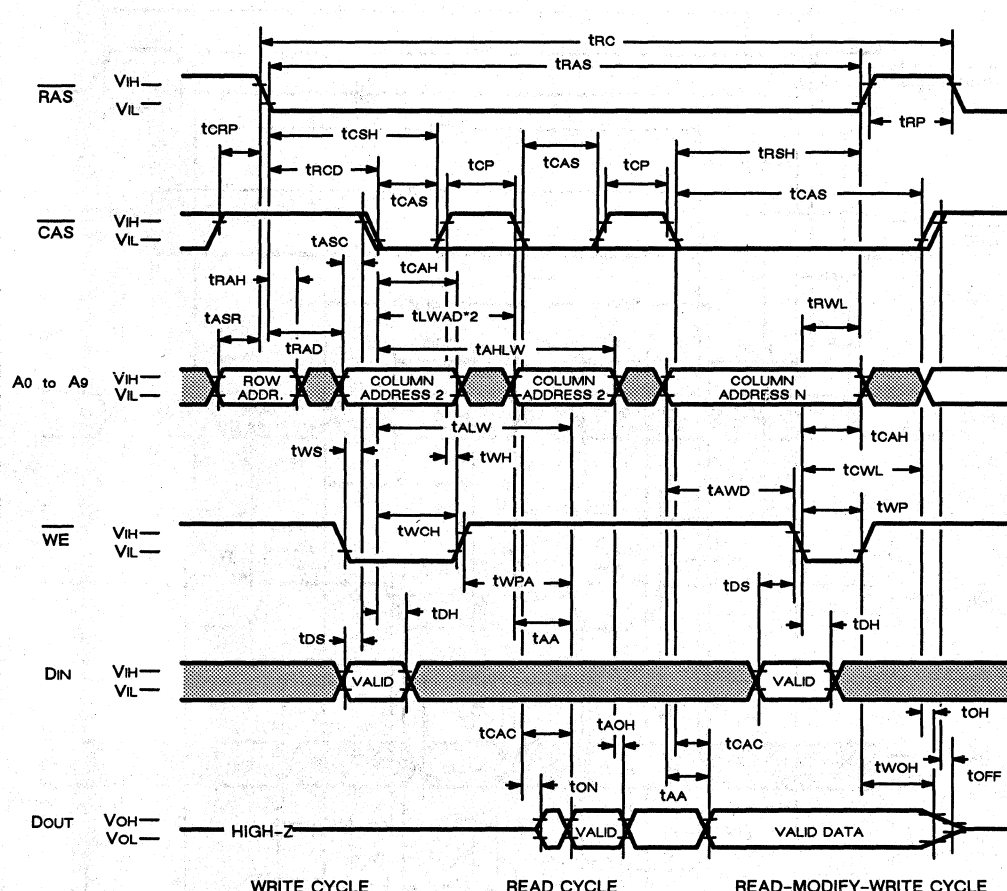
" H " or " L "

DESCRIPTION

In the static column mode read-modify-write cycle, $\overline{WE}$ goes low after tAWD from the column address inputs and tCWD from the falling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge of $\overline{WE}$.

2

Fig. 10 – STATIC COLUMN MODE MIXED CYCLE *1



*1; This is an example of static column mode mixed cycle.
*2; If tLWAD is satisfied its min/max value, tALW = tSC (min) + tAA (max)

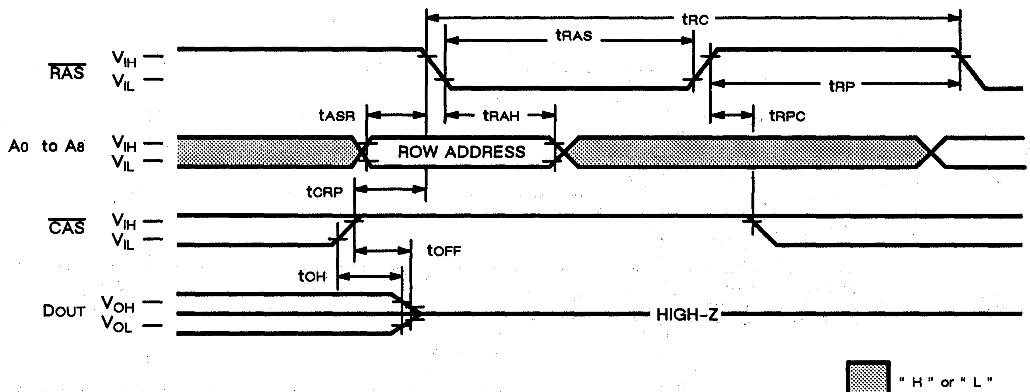
DESCRIPTION

In the static column mode, read, write, and read-modify-write cycles can be mixed in any order.
In the next read cycle of static column mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.

1. tALW from the falling edge of WE or CAS at previous write cycle.
2. tAA from the column address inputs.
3. tWPA from the rising edge of WE at the read cycle.
4. tCAC from the falling edge of CAS.

2

Fig. 11 – $\overline{\text{RAS}}$-ONLY REFRESH CYCLE
NOTE: A9, $\overline{\text{WE}}$, DIN = " H " or " L "

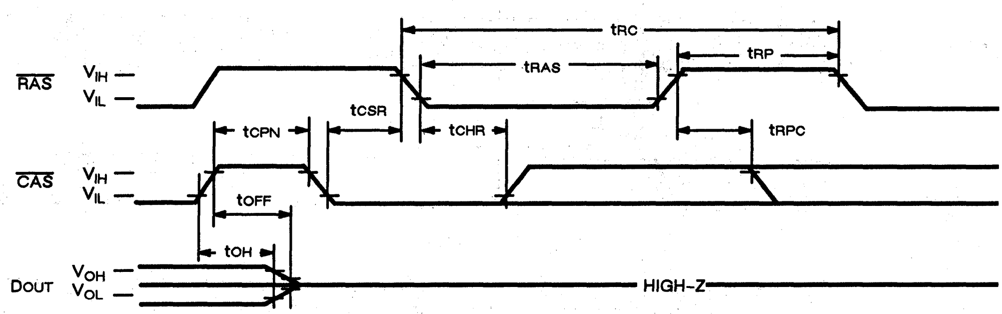


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, and hidden refresh.

$\overline{\text{RAS}}$-only refresh is performed by keeping $\overline{\text{RAS}}$ Low and $\overline{\text{CAS}}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$-only refresh, DOUT pin is kept in a high-impedance state.

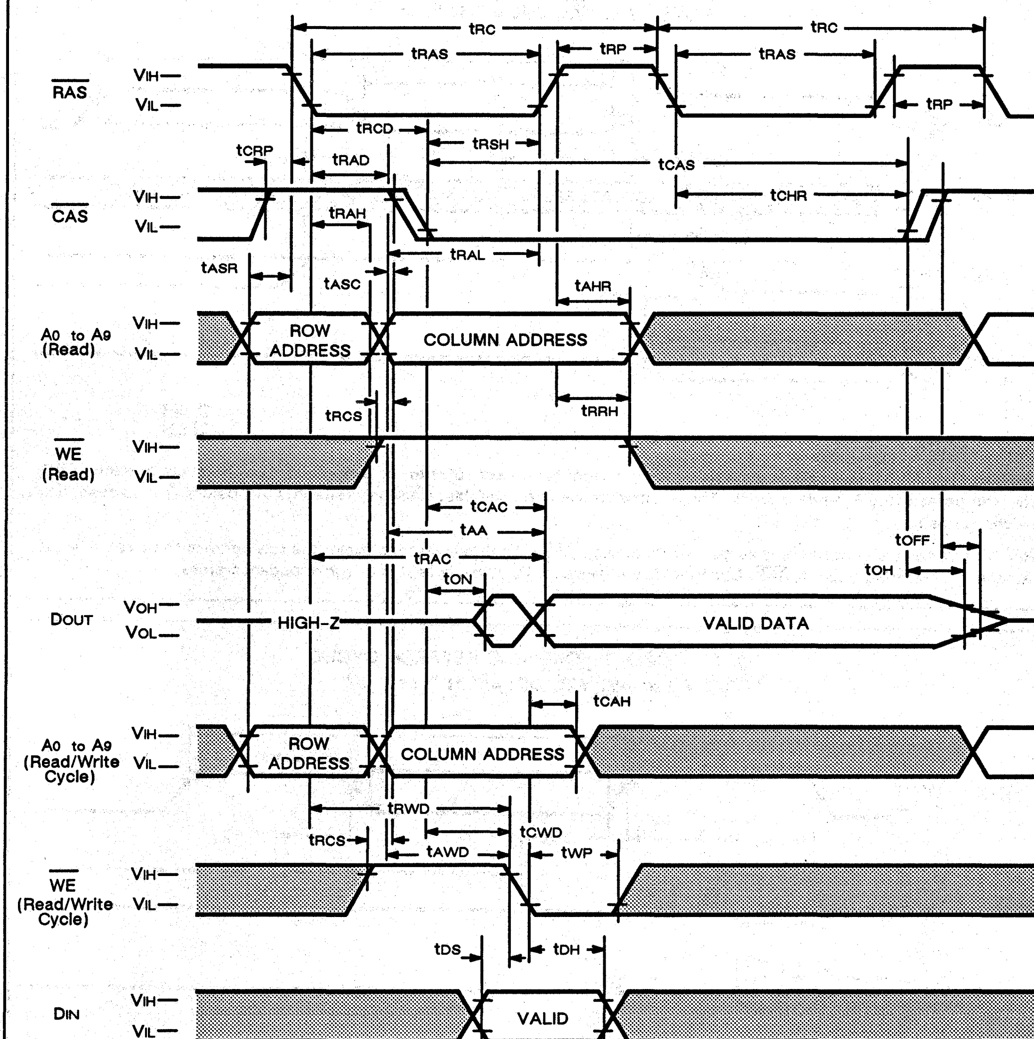
Fig. 12 – $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{\text{WE}}$, DIN = " H " or " L "



DESCRIPTION

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held Low for the specified setup time (t_{CSR}) before $\overline{\text{RAS}}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation.

Fig. 13 – HIDDEN REFRESH CYCLE

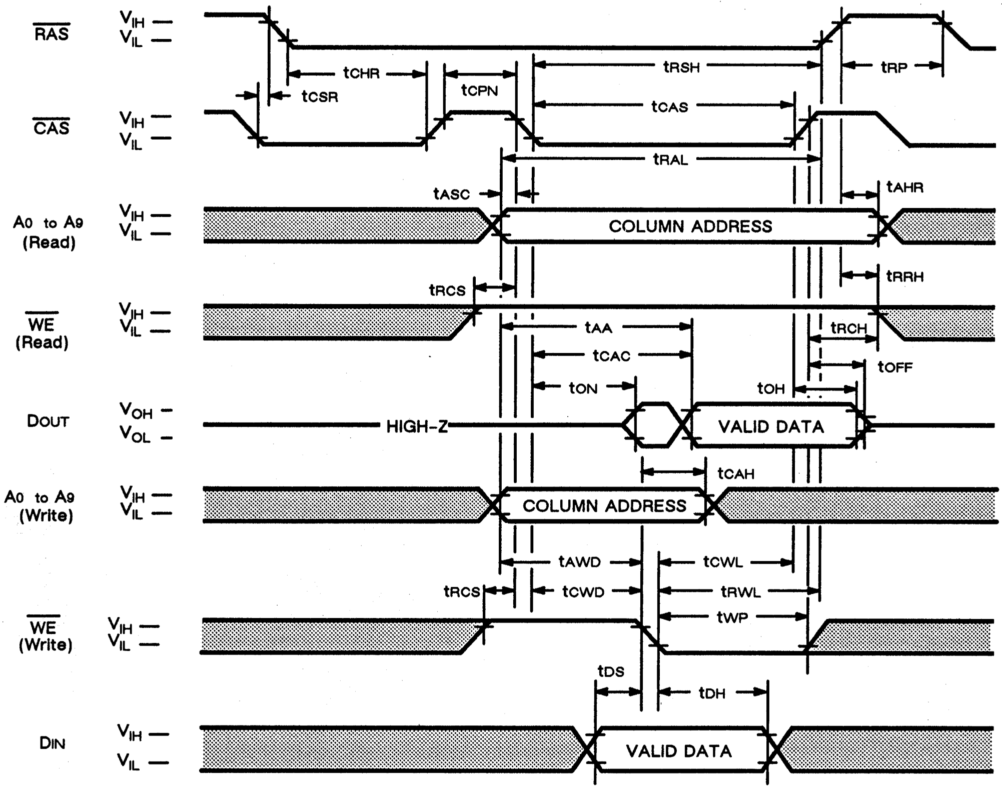


" H " or " L "

DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 14 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



"H" or "L"

DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A9 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A9 are defined by latching levels on A0–A9 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle is designed for use with the following procedures:

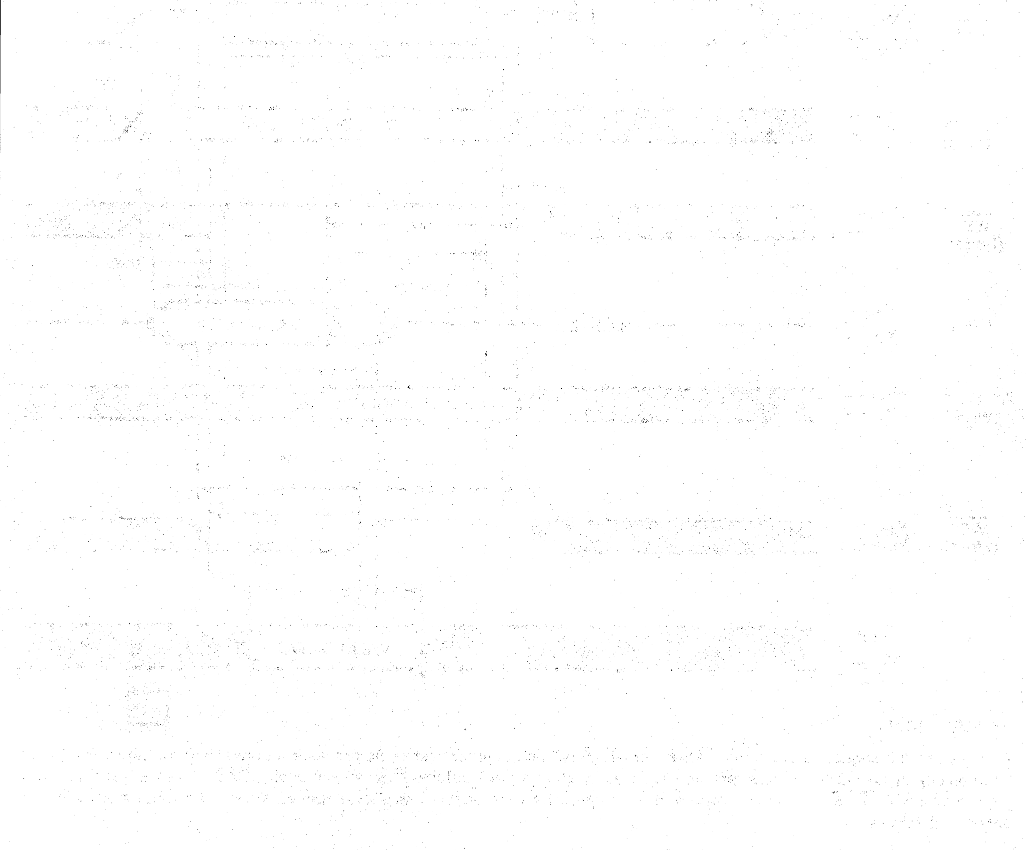
1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.
4) Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read-write cycles. Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3, 4, and 5.

2

PACKAGE DIMENSIONS

(Suffix: -P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-18P-M04))



PACKAGE DIMENSIONS (Continued)

(Suffix: -C)

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER (SOJ-26)
(CASE No.: LCC-26P-M01)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PSZ)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)

2

FUJITSU

CMOS 1048576 BIT SERIAL ACCESS DYNAMIC RAM

MB81C1003-85
MB81C1003-10
MB81C1003-12

2

PRELIMINARY

October 1988
Edition 1.0

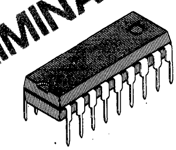
CMOS 1,048,576 x 1 BIT SERIAL ACCESS MODE DYNAMIC RAM

The Fujitsu MB81C1003 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1003 has been designed for mainframe memories, buffer memories, and video image memories requiring highspeed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very lower power dissipation.

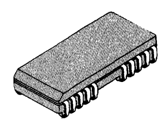
Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1003 high α-ray soft error immunity and long refresh time.

Since the CMOS circuits are used for peripheral circuits, low power dissipation and high speed operation are realized.

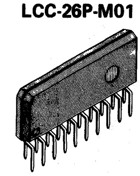
The CMOS standby current is about one fifth that of the conventional NMOS DRAM, so large capacity memory systems with less power and battery backup becomes possible, i.e., low standby current makes the RAM applicable as non-volatile memories.



PLASTIC PACKAGE
DIP-18P-M04



PLASTIC PACKAGE
LCC-26P-M01

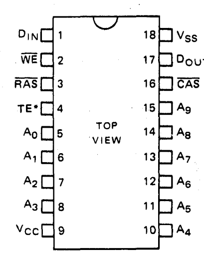


PLASTIC PACKAGE
ZIP-20P-M02

DIP-18C-A01: See Page 16

- 1,048,576 x 1 CMOS DRAM, 18-pin DIP, 26-pin SOJ, and 20-pin ZIP
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- Row Access Time (t_{RAC}),
  85 ns max. (MB81C1003-85)
  100 ns max. (MB81C1003-10)
  120 ns max. (MB81C1003-12)
- Random Cycle Time (t_{RC}),
  160 ns min. (MB81C1003-85)
  180 ns min. (MB81C1003-10)
  210 ns min. (MB81C1003-12)
- Column Access Time (t_{CAC}),
  25 ns max. (MB81C1003-85)
  30 ns max. (MB81C1003-10)
  35 ns max. (MB81C1003-12)
- Serial Access Mode Cycle Time (t_{SA}),
  60 ns min. (MB81C1003-85)
  60 ns min. (MB81C1003-10)
  70 ns min. (MB81C1003-12)
- Single 5V±10% Supply
- Low Power Dissipation
  358 mW max. (MB81C1003-85)
  330 mW max. (MB81C1003-10)
  275 mW max. (MB81C1003-12)
  11 mW max. (TTL level input)
  5.5 mW max. (CMOS level input)
- 512 refresh cycles every 8.2 ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Early Write and Delayed Write
- Common I/O capability by using early write

PIN ASSIGNMENT



*: Test Enable (will be available)

Pin Assignment For SOJ: See Page 14
Pin Assignment For ZIP: See Page 15

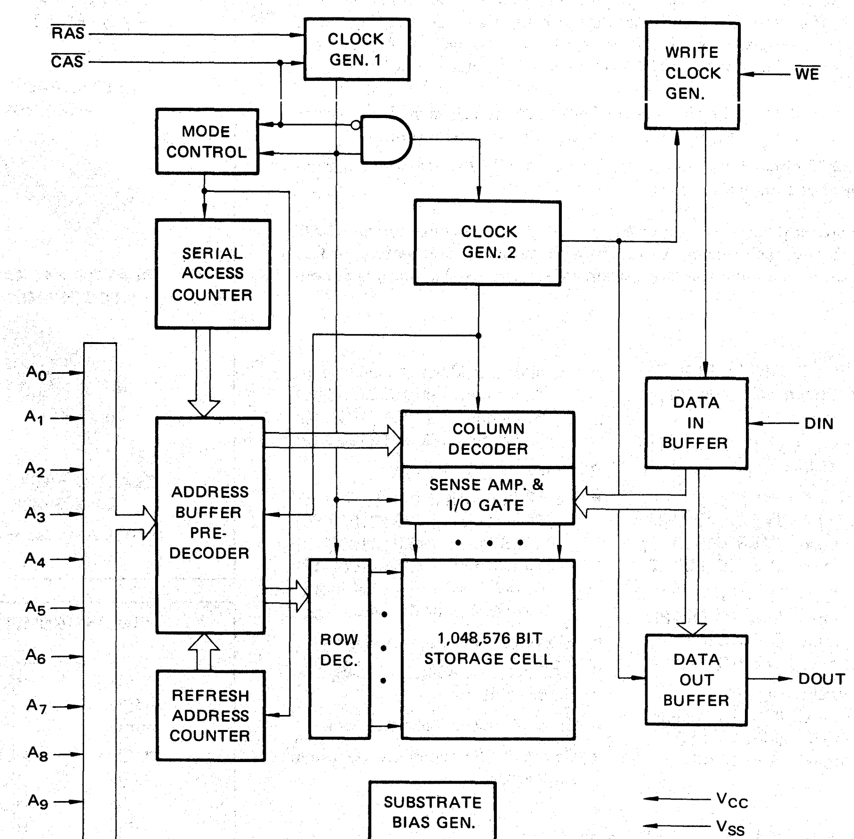
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} Relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM



CAPITANCE

(T_A = 25°C)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance, A_0 to A_9, D_{IN}	C_{IN1}		5	pF
Input Capacitance, $\overline{RAS}$ $\overline{CAS}$, $\overline{WE}$	C_{IN2}		5	pF
Output Capacitance, D_{OUT}	C_{OUT}		5	pF

2

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0		
Input High Voltage, All inputs	V_{IH}	2.4	–	6.5	V	
Input Low Voltage, All inputs	V_{IL}	-2.0	–	0.8	V	

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

Parameter		Conditions	Symbol	Values		Unit
				Min	Max	
Operating Current* (Average power supply current)	MB81C1003-85	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	I_{CC1}	–	65	mA
	MB81C1003-10			–	60	
	MB81C1003-12			–	50	
Standby Current (Power supply current)	TTL level	$\overline{RAS} = \overline{CAS} = V_{IH}$	I_{CC2}	–	2.0	mA
	CMOS level	$\overline{RAS} = \overline{CAS} \geqq V_{CC}$-0.2V		–	1.0	
Refresh Current 1* (Average power supply current	MB81C1003-85	$\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min	I_{CC3}	–	60	mA
	MB81C1003-10			–	55	
	MB81C1003-12			–	45	
Serial Access Mode Current*	MB81C1003-85	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{SA} = min	I_{CC4}	–	40	mA
	MB81C1003-10			–	40	
	MB81C1003-12			–	33	
Refresh Current 2* (Average power current)	MB81C1003-85	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	I_{CC5}	–	60	mA
	MB81C1003-10			–	55	
	MB81C1003-12			–	45	
Input Leakage Current		0V $\leqq V_{IN} \leqq$ 5.5V, 4.5V $\leqq V_{CC} \leqq$ 5.5V, V_{SS} = 0V; All other pins not under test = 0V	$I_{I(L)}$	-10	10	µA
Output Leakage Current		0V $\leqq V_{OUT} \leqq$ 5.5V; Data out disabled	$I_{O(L)}$	-10	10	
Output High Voltage		I_{OH} = -5mA	V_{OH}	2.4	–	V
Output Low Voltage		I_{OL} = 4.2mA	V_{OL}	–	0.4	

NOTE: *; I_{CC} depends on the output load conditions and cycle rate. The specified values are with the output open.

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1,2,3

No.	Parameter	NOTE	Symbol	MB81C1003-85		MB81C1003-10		MB81C1003-12		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}		8.2		8.2		8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	160		180		210		ns
3	Read-Modify-Write Cycle Time		t_{RWC}	190		210		245		ns
4	Access Time from $\overline{RAS}$	4 7	t_{RAC}		85		100		120	ns
5	Access Time from $\overline{CAS}$	5 7	t_{CAC}		25		30		35	ns
6	Access Time from Column Address	6 7	t_{AA}		50		50		60	ns
7	Output Data Hold Time		t_{OH}	7		7		7		ns
8	Output Buffer Turn On Delay Time		t_{ON}	5		5		5		ns
9	Output Buffer Turn Off Delay Time	8	t_{OFF}		25		25		25	ns
10	Transition Time		t_T	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	65		70		80		ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	85	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25		30		35		ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0		0		0		ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	9 10	t_{RCD}	22	60	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25		30		35		ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	85		100		120		ns
18	$\overline{CAS}$ Precharge Time ($\overline{C}$-B-$\overline{R}$ Cycle)	15	t_{CPN}	15		15		15		ns
19	Row Address Set Up Time		t_{ASR}	0		0		0		ns
20	Row Address Hold Time		t_{RAH}	12		15		15		ns
21	Column Address Set Up Time		t_{ASC}	0		0		0		ns
22	Column Address Hold Time		t_{CAH}	15		15		20		ns
23	$\overline{RAS}$ to Column Address Delay Time	11	t_{RAD}	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	45		50		60		ns
25	Read Command Set Up Time		t_{RCS}	0		0		0		ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	12	t_{RRH}	0		0		0		ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	12	t_{RCH}	0		0		0		ns
28	Write Command Set Up Time	13	t_{WCS}	0		0		0		ns
29	Write Command Hold Time		t_{WCH}	15		15		20		ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15		15		20		ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25		25		30		ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		20		25		ns
33	D_{IN} Set Up Time		t_{DS}	0		0		0		ns

2

AC CHARACTERISTICS (continued)

(At recommended operating conditions unless otherwise noted.) Notes 1,2,3

No.	Parameter NOTE	Symbol	MB81C1003-85 Min	MB81C1003-85 Max	MB81C1003-10 Min	MB81C1003-10 Max	MB81C1003-12 Min	MB81C1003-12 Max	Unit
34	D_{IN} Hold Time	t_{DH}	15		15		20		ns
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time 13	t_{RWD}	85		100		120		ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time 13	t_{CWD}	25		30		35		ns
37	Column Address to $\overline{WE}$ Dealy Time 13	t_{AWD}	50		50		60		ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)	t_{RPC}	0		0		0		ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CSR}	0		0		0		ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	15		15		20		ns
41	Access Time from $\overline{CAS}$ (Counter Test Cycle)	t_{CAT}		50		50		60	ns
50	Serial Access Mode Read/Write Cycle Time	t_{SA}	60		60		70		ns
51	Serial Access Mode Read-Modify-Write Cycle Time	t_{SARW}	85		85		100		ns
52	Access Time from $\overline{CAS}$ Precharge 7 14	t_{SPA}		60		60		70	ns
53	Serial Access Mode $\overline{CAS}$ Precharge Time	t_{SCP}	15		15		15		ns

NOTES:

1 An initial pause ($\overline{RAS}=\overline{CAS}=V_{IH}$) of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

2 AC characteristics assume t_T = 5 ns.

3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

4 Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 2 and 3.

5 If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA}$-t_{CAC}-t_T, access time is t_{CAC}.

6 If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA}$-t_{CAC}-t_T, access time is t_{AA}.

7 Measured with a load equivalent to two TTL loads and 100 pF.

8 t_{OFF} is specified that output buffer changes to high impedance state.

9 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

10 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).

11 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

12 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

13 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restructive operating parameter. They are included in the data sheet as the electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin.
If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear at the D_{OUT} pin, and write operation can be executed by satisfing t_{RWL}, t_{CWL}, t_{RAL} specifications.

14 t_{SPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{SCP} is long, t_{SPA} is longer than t_{SPA}(max).

15 Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 — t_{RAC} vs t_{RCD}

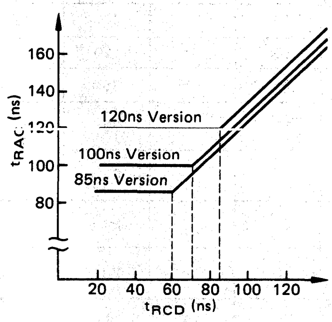
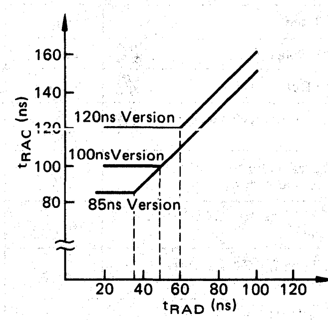


Fig. 3 — t_{RAC} vs t_{RAD}

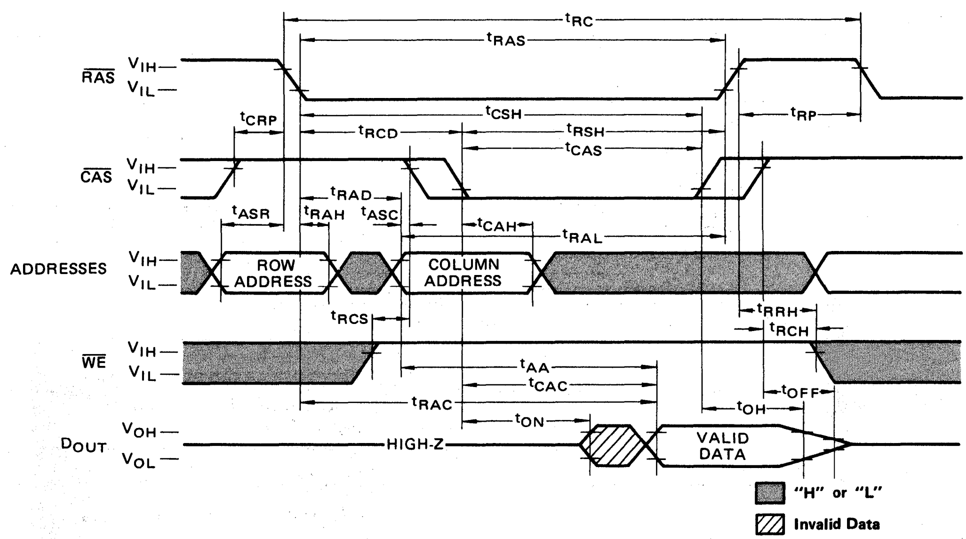


FUNCTIONAL TRUTH TABLE

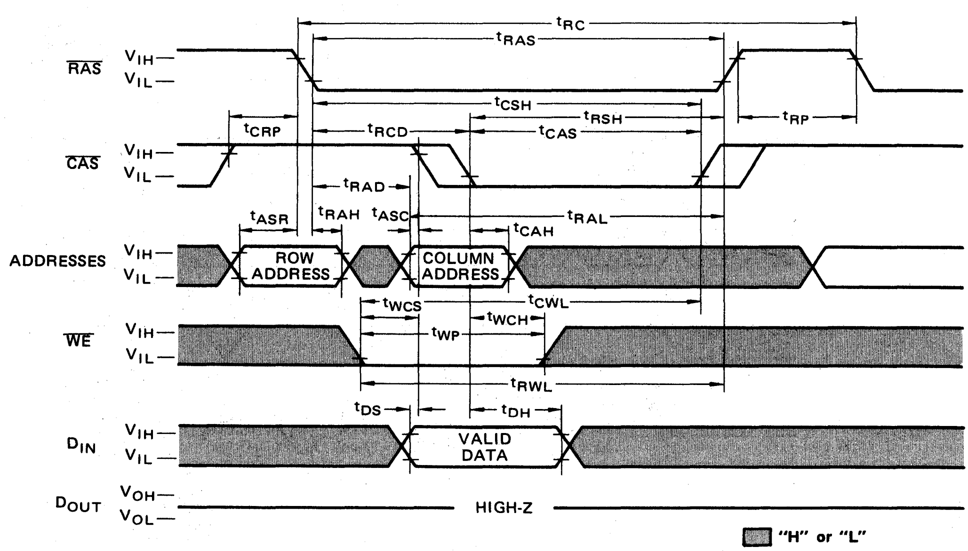
Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	–	–	–	High-Z	–	
Read Cycle	L	L	H	Valid	Valid	–	Valid	○ *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	○ *	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	Valid	Valid	X→ Valid	Valid	○ *	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	–	–	High-Z	○	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	L	L	X	–	–	–	High-Z	○	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	–	–	–	Valid	○	Previous data is kept.

X; "H" or "L"
* ; It is impossible in serial access mode.

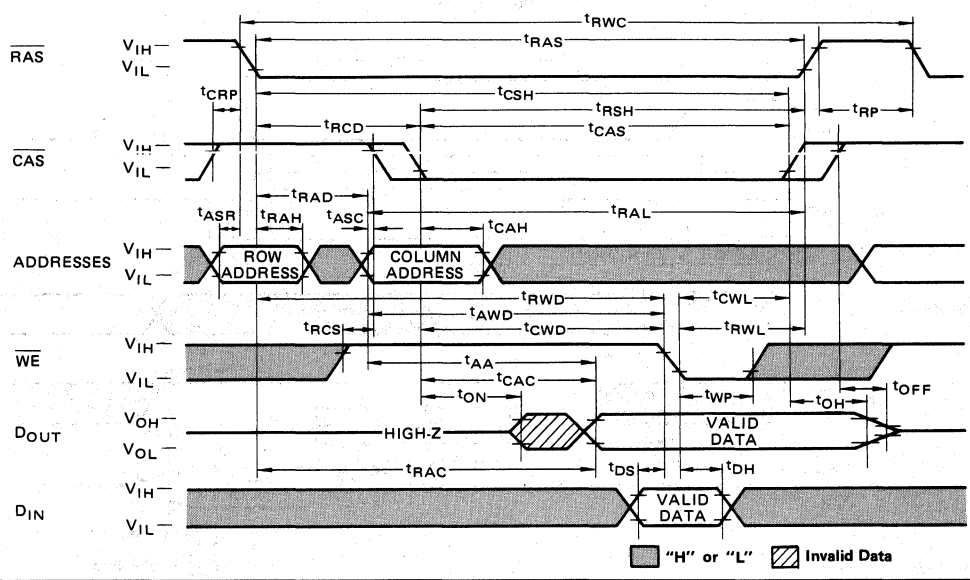
Read Cycle



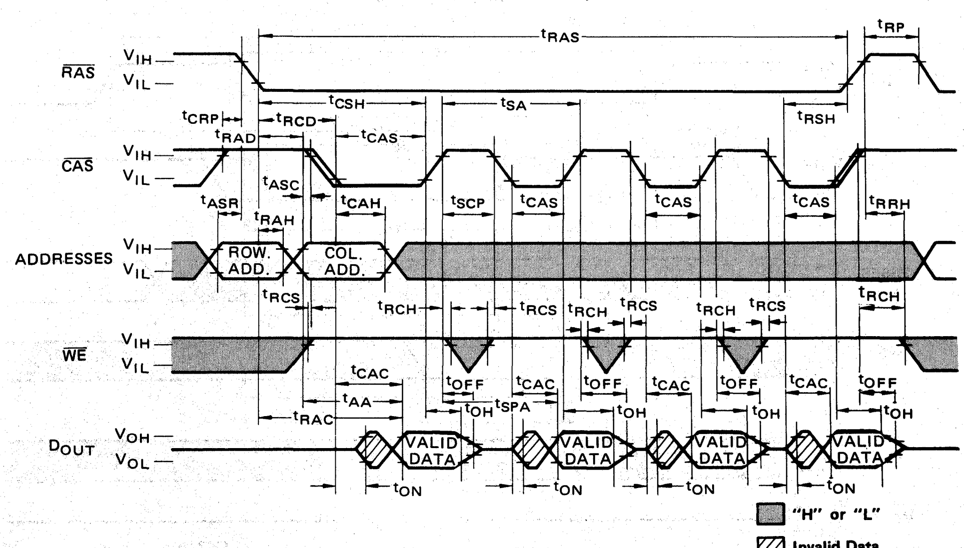
Write Cycle (Early Write)



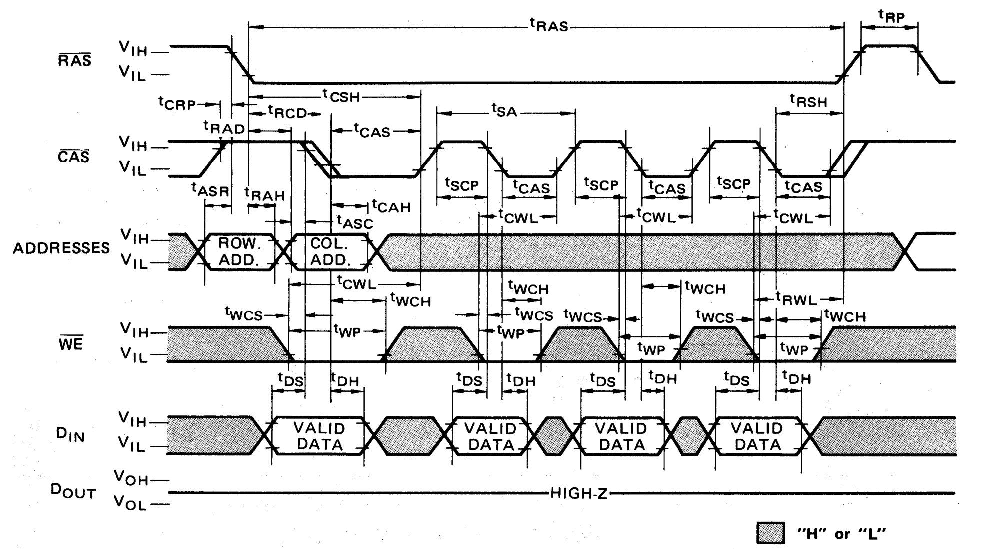
Read-Write/Read-Modify-Write Cycle



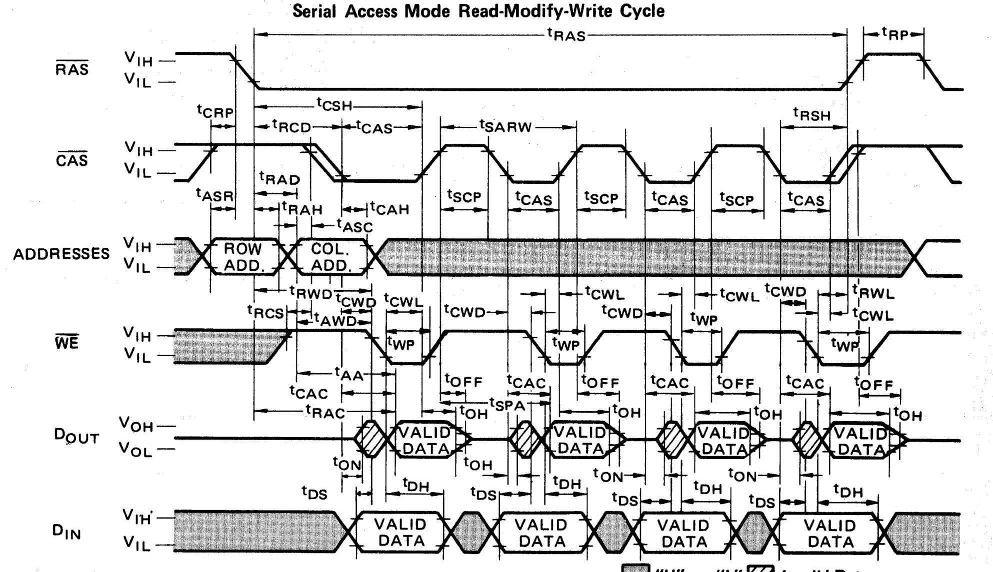
Serial Access Mode Read Cycle



Serial Access Mode Write Cycle (Early Write)



Serial Access Mode Read-Modify-Write Cycle



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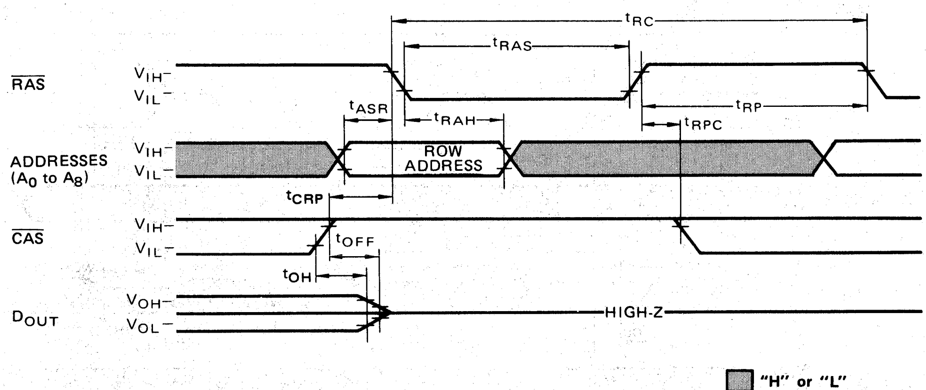
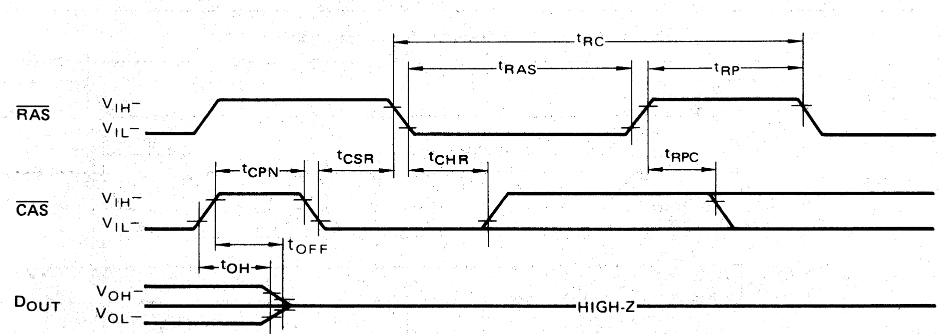
$\overline{RAS}$-Only Refresh Cycle

NOTE: A_9 $\overline{WE}$, D_{IN} = "H" or "L"



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE: Address, $\overline{WE}$, D_{IN} = "H" or "L"



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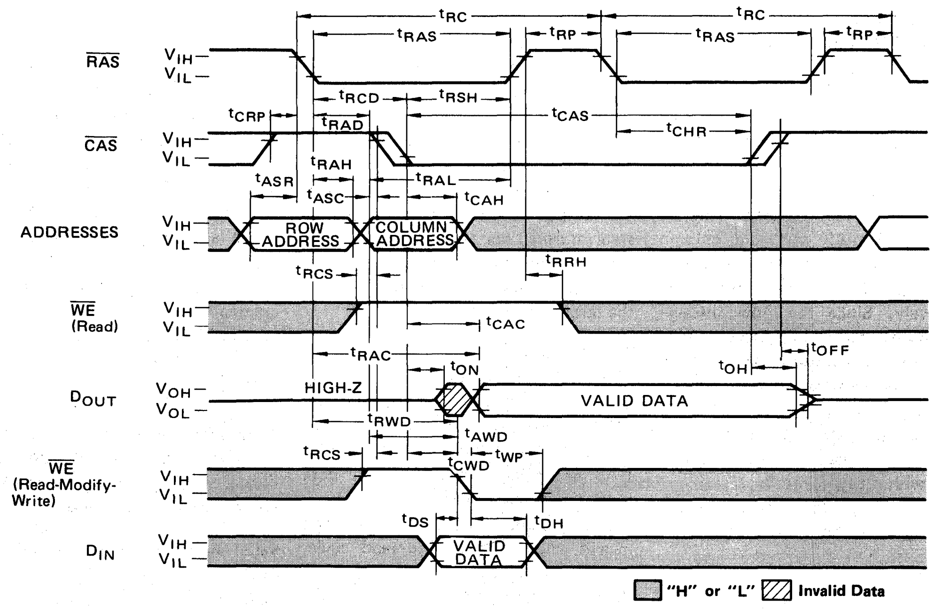
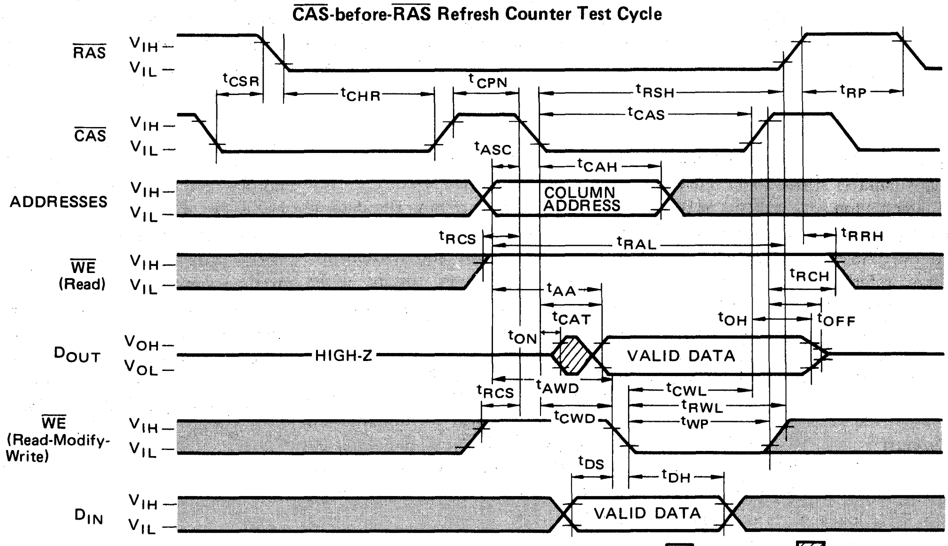
Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



2

DESCRIPTION

Address Inputs:
A total of twenty binary input address bits are required to decode any one of the 1,048,576 storage cells within the MB81C1003. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe ($\overline{RAS}$). The ten column address bits are established on the address input pin (A_0 to A_9) and latched with the Column Address Strobe ($\overline{CAS}$). All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min) + t_T.
Therefore, to get valid data within t_{RAC}, it is necessary to apply column address within t_{RAD} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occure later.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. Data input is ignored during read cycle. Data output is high impedance state during write cycle.

Data Input:
Data is written into the MB81C1003 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-modify-write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is high impedance state until $\overline{CAS}$ is brought low. In a read or read-modify-write cycle, the output becomes valid after t_{RAC} from the falling edge of $\overline{CAS}$ when t_{RCD} (max) is satisfied or after t_{CAC} when t_{RCD} is longer than t_{RCD} (max). The data output remains valid until $\overline{CAS}$ returns to high with t_{OH} and becomes high impedance state after t_{OFF}. In an early write cycle, the output buffer is high impedance state during the entire cycle. In a delayed write cycle, if t_{RWD} or t_{CWD} is less than t_{RWD} (min) or t_{CWD} (min), the output is invalid.

Read Cycle:
The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" through-out the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output is remain valid with $\overline{CAS}$ "L", i.e., if $\overline{CAS}$ goes "H", the data becomes invalid with t_{OH}. During read cycle, the D_{IN} pin is "Don't Care". The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), or Column address input (t_{AA}). If t_{RCD} ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}.

Write Cycle:
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and D_{IN} pin. The data on D_{IN} pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL}, and t_{RAL} must be satisfied tne specifications.

Read-Modify-Write Cycle:
The read-modify-write cycle is executed by changing $\overline{WE}$ high to low after the data appears at the D_{OUT} pin. After the current data is read out, modified data can be re-written into the same address quickly.

Serial Access Mode Read/Write Cycle:
Serial Access mode allows high speed serial read, write or read-modify-write access of 2 to 1024 bits of data. The bits of data that may be accessed during serial access mode are determined by the 10 row addresses. The remaining 10 bits of addresses (CA_0 to CA_9) are used to select one of 1024 serieal access bits for initial access. After the first bits is accessed by normal mode, the remaining serial access bits can be accessed by toggling $\overline{CAS}$ "H" then "L". Toggling $\overline{CAS}$ causes CA_0 to CA_9 to be incremented internally while all other address bits are held constant and makes the next serial access bit available for access.
Refer to the table 1 for serial access mode address sequence.
If more than 1024 bits are accessed during serial access mode, the address sequence will begin to repeat.

Serial Access Mode Read-Modify-Write Cycle:
The read-modify-write cycle can be used during serial access mode as well as normal mode operation. During the serial access mode, all combinations of read, write, and read-modify-write cycle can be applied as well as normal mode operation.

Refresh:
The refresh of DRAM is executed by normal read, write or read-modify-write cycle, i.e., the cells on the one row line are refreshed by executing one of three cycles. 1024 row address must be refreshed every 8.2 ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB81C1003 also has three types of refresh modes, $\overline{RAS}$-Only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and Hidden refresh.

1. $\overline{\text{RAS}}$-Only Refresh;
The $\overline{\text{RAS}}$-Only refresh is executed by keeping $\overline{\text{RAS}}$ "L" and keeping $\overline{\text{CAS}}$ "H" through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$-Only refresh, the D_{OUT} pin is kept high impedance state.

2. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh;
The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is executed by bringing $\overline{\text{CAS}}$ "L" before $\overline{\text{RAS}}$. By this timing combination, the MB81C1003 executes $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh. The row address input is not necessary because it is generated internally.

3. Hidden Refresh;
The Hidden refresh is executed by keeping $\overline{\text{CAS}}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{\text{CAS}}$ is kept low continuousely from previous cycle, followed refresh cycle should be $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh.

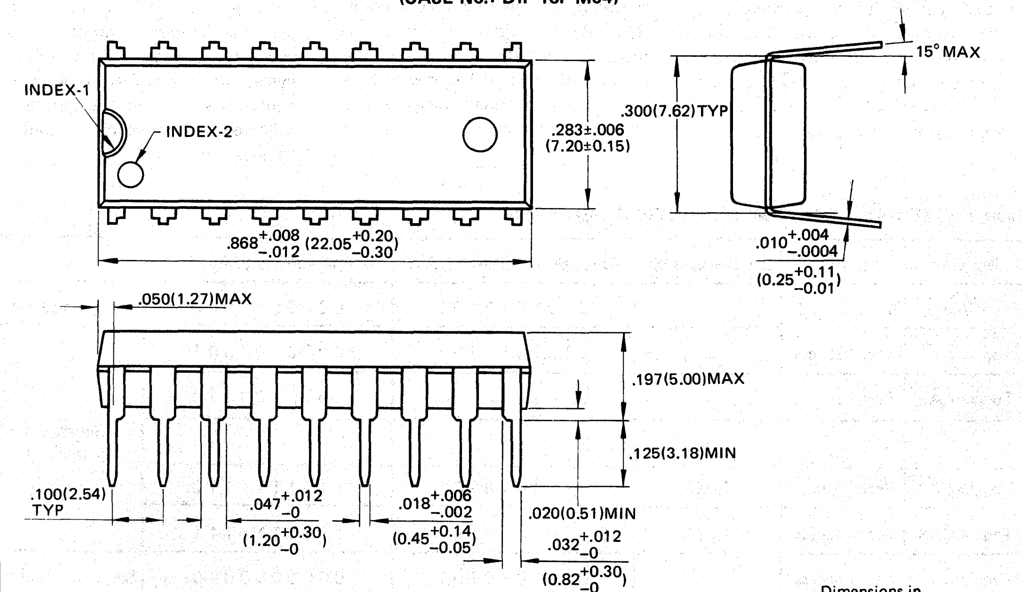
Table 1 — SERIAL ACCESS MODE ADDRESS SEQUENCE

Sequence	Mode	Serial access bit	Row address (RA_9~RA_0)	Column address (CA_9~CA_0)	
$\overline{\text{RAS}}$/$\overline{\text{CAS}}$	Normal mode	1	0 1 0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0 0	Input address
Toggle $\overline{\text{CAS}}$	Serial access	2	0 1 0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0 1	Generated Internally
Toggle $\overline{\text{CAS}}$	Serial access	3	0 1 0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 1 0	
⋮	⋮	⋮	⋮	⋮	
Toggle $\overline{\text{CAS}}$	Serial access	1,023	0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 1 0	
Toggle $\overline{\text{CAS}}$	Serial access	1,024	0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 1 1	
Toggle $\overline{\text{CAS}}$	Serial access	1	0 1 0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0 0	Sequence repeats

2

PACKAGE DIMENSIONS

(Suffix: -P)



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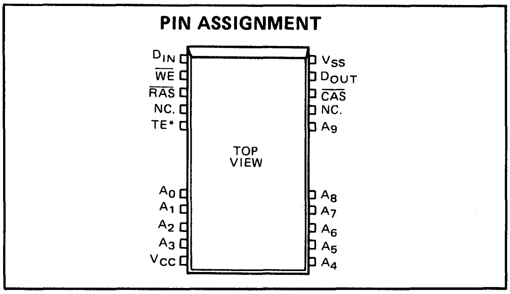
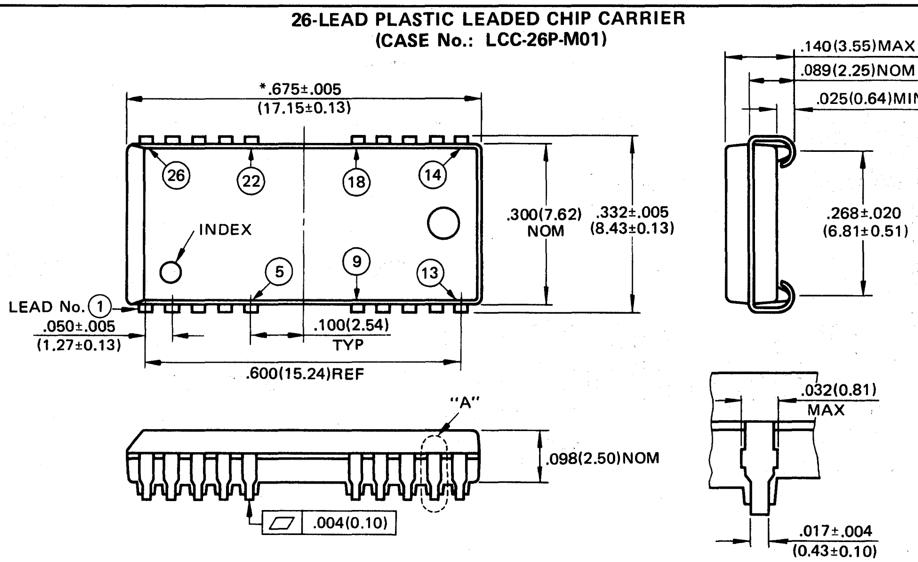
PACKAGE DIMENSIONS (continued)

(Suffix: -PJ)





NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package. Foot-print compatible with "SOJ-26", LCC-26C-A01)

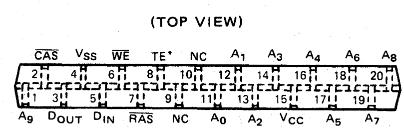
Dimensions in inches (millimeters)

2

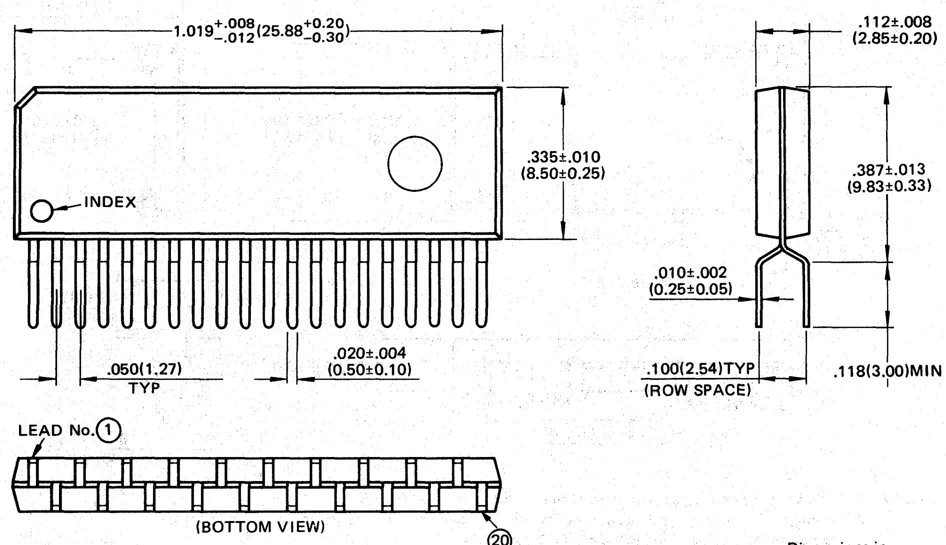
PACKAGE DIMENSIONS (continued)

(Suffix:-PSZ)

PIN ASSIGNMENT



20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)

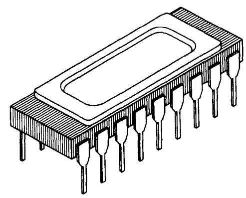


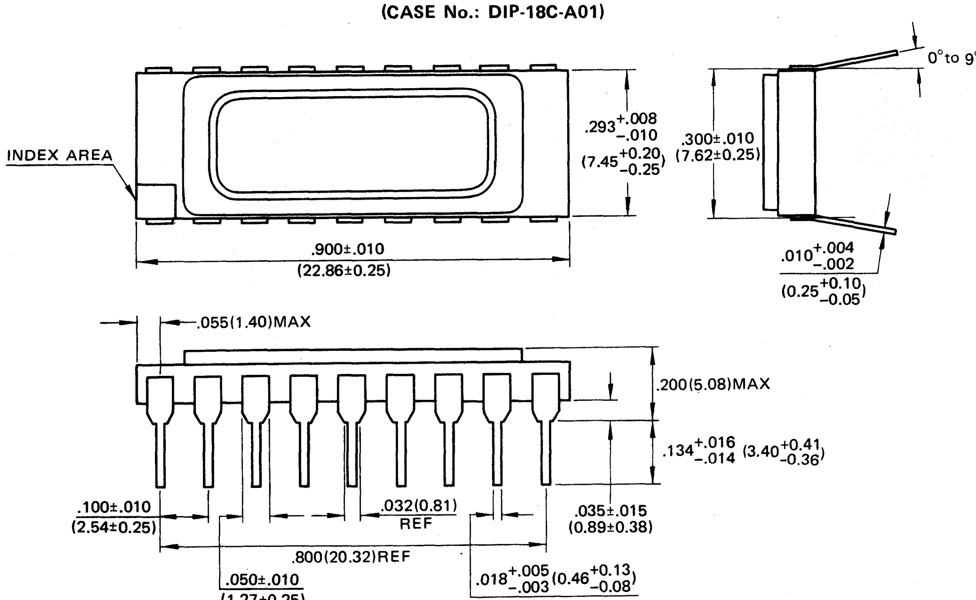
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (continued)

(Suffix: -C)


DIP-18C-A01



Dimensions in inches (millimeters)

FUJITSU

CMOS 1,048,576 BIT FAST PAGE DYNAMIC RAM

MB81C4256-85
MB81C4256-10
MB81C4256-12

2

December 1988
Edition 1.0

CMOS 262,144 x 4 BIT Fast Page Mode DYNAMIC RAM

The Fujitsu MB81C4256 is a fully decoded CMOS Dynamic RAM (DRAM) that contains 1,048,576 memory cells accessible in 4-bit increments. The MB81C4256 features a "fast page" mode of operation whereby high-speed random access of up to 512-bits of data within the same row can be selected. The MB81C4256 DRAM is ideally suited for mainframes, buffers, hand-held computers, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81C4256 is only about one-fifth that of a conventional NMOS DRAM, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81C4256 is fabricated using silicon gate CMOS and Fujitsu's advanced triple-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81C4256 are not critical and all inputs are TTL compatible.

DIP-20P-M03

DIP-20C-A03

LCC-26P-M01

ZIP-20P-M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PRODUCT LINE & FEATURES

Parameter	MB81C4256-85	MB81C4256-10	MB81C4256-12
Row Access Time	85ns max.	100ns max.	120ns max.
Random Cycle Time	160ns min.	180ns min.	210ns min.
Column Address Time	50ns max.	50ns max.	60ns max.
Column Access Time	25ns max.	30ns max.	35ns max.
Fast Page Mode Cycle Time	60ns min.	60ns min.	70ns min.
Low Power Dissipation			
• Operating current	358mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level) /5.5mW max. (CMOS level)		

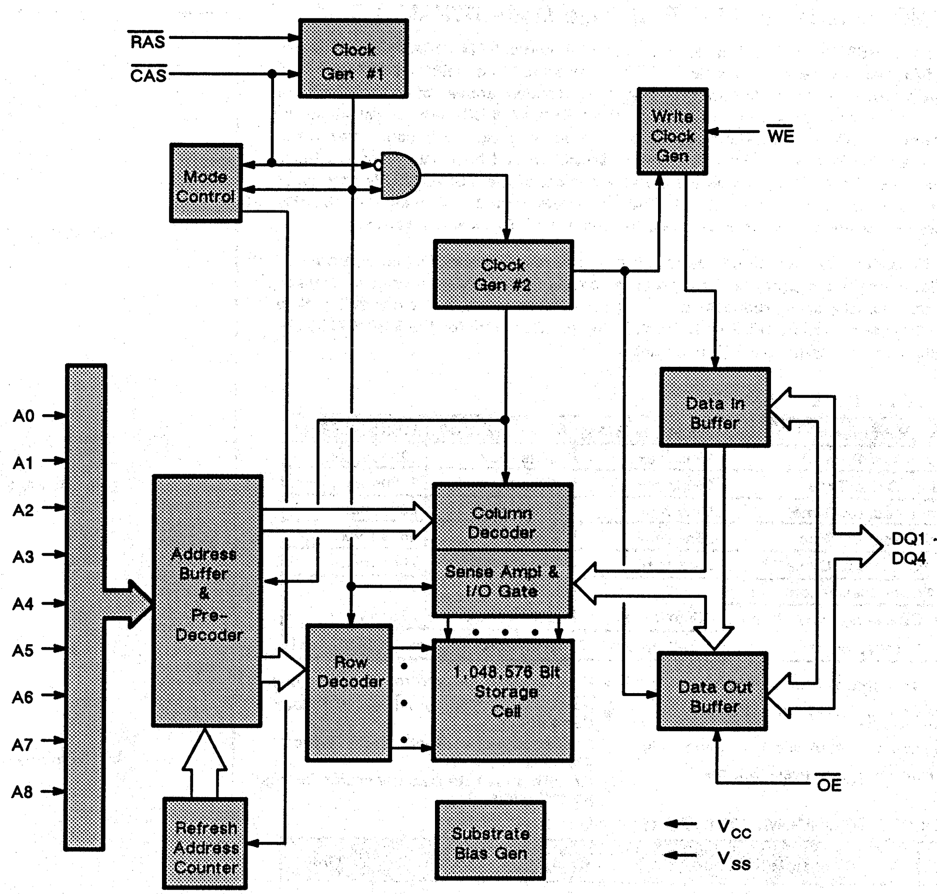
- 262,144 words x 4 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write or $\overline{OE}$ controlled write capacity
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capacity
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		--	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB81C4256 DYNAMIC RAM – BLOCK DIAGRAM

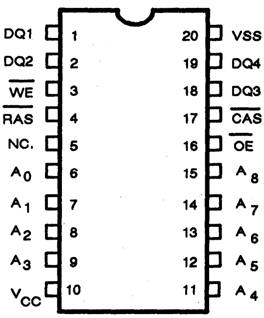


CAPACITANCE (T_A= 25°C, f = 1MHz)

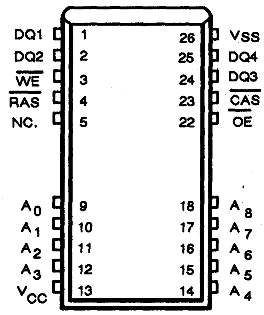
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

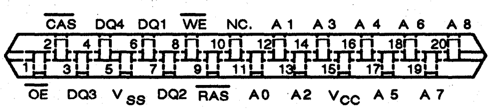
18-Pin DIP:
(TOP VIEW)



26-Pin SOJ:
(TOP VIEW)



20-Pin ZIP:
(TOP VIEW)



Designator	Function
DQ1 to DQ4	Data Input.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A8	Address Inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

(All voltages referenced to ground; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	VSS	0	0	0	
Input High Voltage, all inputs	VIH	2.4	—	6.5	V
Input Low Voltage, all inputs	VIL	-2.0	—	0.8	V
Input Low Voltage, DQ(Note)	VILD	-1.0	—	0.8	V

Note: Undershoots of up to -2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0-through-A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways--an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data (DQ1-DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

t_{RAC}: from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

t_{CAC}: from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

t_{AA} : from column address input when t_{RAD} is greater then t_{RAD} (max).

t_{OEA}: from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} .

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 512-bits can be accessed and, when multiple MB 81C4256s are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready-modify-write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value Min	Value Typ	Value Max	Unit
Output High Voltage		V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output Low Voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input Leakage Current (Any Input)		$I_{I(L)}$	0 V ≤ V_{IN} ≤ 5.5 V; 4.5 V ≤ V_{CC} ≤ 5.5 V; Vss = 0 V; All other pins not under test = 0V	-10	—	10	µA
Output Leakage Current		$I_{DQ(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V; Data out disabled	-10	—	10	µA
Operating Current (Average Power Supply Current)	MB81C4256-85	I_{CC1} (Note)	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	65	mA
	MB81C4256-10					60	
	MB81C4256-12					50	
Standby Current (Power Supply Current)	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2 V			1.0	
Refresh Current #1 (Average Power Supply Current)	MB81C4256-85	I_{CC3} (Note)	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	60	mA
	MB81C4256-10					55	
	MB81C4256-12					45	
Fast Page Mode Current	MB81C4256-85	I_{CC4} (Note)	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling t_{PC} = min	—	—	40	mA
	MB81C4256-10					40	
	MB81C4256-12					33	
Refresh Current #2 (Average Power Supply Current)	MB81C4256-85	I_{CC5} (Note)	$\overline{RAS}$ cycling $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	60	mA
	MB81C4256-10					55	
	MB81C4256-12					45	

Note: Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
Icc depends on the input low voltage level VIL, VIL>–0.5V.

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB81C4256-85		MB81C4256-10		MB81C4256-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	Time Between Refresh	t_{REF}	—	8.2	—	8.2	—	8.2	ms	—
2	Random Read/Write Cycle Time	t_{RC}	160	—	180	—	210	—	ns	—
3	Read-Modify-Write Cycle Time	t_{RWC}	220	—	240	—	275	—	ns	—
4	Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	4,7
5	Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	30	—	35	ns	5,7
6	Access Time from Column Address	t_{AA}	—	50	—	50	—	60	ns	6,7
7	Output Hold Time	t_{OH}	7	—	7	—	7	—	ns	—
8	Output Buffer Turn On Delay Time	t_{ON}	5	—	5	—	5	—	ns	—
9	Output Buffer Turn off Delay Time	t_{OFF}	—	25	—	25	—	25	ns	8
10	Transition Time	t_T	3	50	3	50	3	50	ns	—
11	$\overline{RAS}$ Precharge Time	t_{RP}	65	—	70	—	80	—	ns	—
12	$\overline{RAS}$ Pulse Width	t_{RAS}	85	100000	100	100000	120	100000	ns	—
13	$\overline{RAS}$ Hold Time	t_{RSH}	25	—	30	—	35	—	ns	—
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0	—	0	—	0	—	ns	—
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	60	25	70	25	85	ns	9,10
16	$\overline{CAS}$ Pulse Width	t_{CAS}	25	—	30	—	35	—	ns	—
17	$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	—
18	$\overline{CAS}$ Precharge Time (Normal)	t_{CPN}	15	—	15	—	15	—	ns	17
19	Row Address Set Up Time	t_{ASR}	0	—	0	—	0	—	ns	—
20	Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	—
21	Column Address Set Up Time	t_{ASC}	0	—	0	—	0	—	ns	—
22	Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	—
23	$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	35	20	50	20	60	ns	11
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	50	—	60	—	ns	—
25	Read Command Set Up Time	t_{RCS}	0	—	0	—	0	—	ns	—
26	Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	12
27	Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	12
28	Write Command Set Up Time	t_{WCS}	0	—	0	—	0	—	ns	15
29	Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	—
30	$\overline{WE}$ Pulse Width	t_{WP}	15	—	15	—	20	—	ns	—
31	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	—
32	Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	—
33	DIN set Up Time	t_{DS}	0	—	0	—	0	—	ns	—
34	DIN Hold Time	t_{DH}	15	—	15	—	20	—	ns	—

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB81C4256-85		MB81C4256-10		MB81C4256-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
35	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	t_{RPC}	0	—	0	—	0	—	ns	—
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before $\overline{RAS}$ Refresh	t_{CSR}	0	—	0	—	0	—	ns	—
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before $\overline{RAS}$ Refresh	t_{CHR}	15	—	15	—	20	—	ns	—
38	Access Time from $\overline{OE}$	t_{OEA}	—	22	—	25		30	ns	7
39	Output Buffer Turn Off Delay from $\overline{OE}$	t_{OEZ}	—	25	—	25	—	25	ns	8
40	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data	t_{OEL}	10	—	10	—	10	—	ns	—
41	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	0	—	0	—	0	—	ns	13
42	$\overline{OE}$ to Data In Delay Time	t_{OED}	25	—	25	—	25	—	ns	
43	DIN to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	14
44	DIN to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	14
45	Access Time from $\overline{CAS}$ (Counter Test Cycle)	t_{CAT}	—	50	—	50	—	60	ns	—
50	Fast Page Mode Read/Write Cycle Time	t_{PC}	60	—	60	—	70	—	ns	—
51	Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	115	—	115	—	130	—	ns	—
52	Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	60	—	60	—	70	ns	7.16
53	Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	15	—	15	—	15	—	ns	—

Notes:

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=VIH) of 200μs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max). If $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min)
11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. Assumes that $t_{WCS} < t_{WCS}$ (min)
14. Either t_{DZC} or t_{DZO} must be satisfied.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is shortened, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

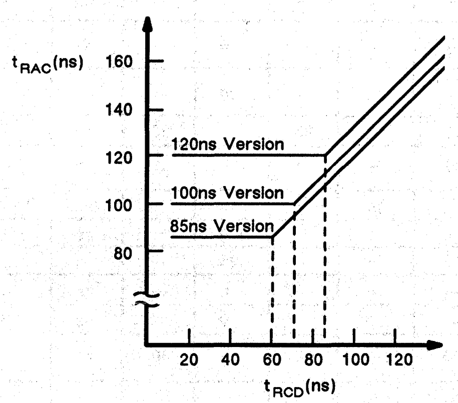
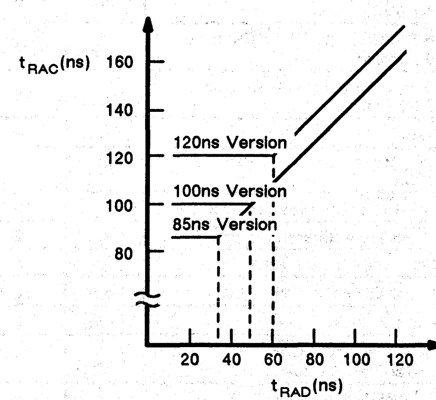


Fig. 3 – t_{RAC} vs. t_{RAD}



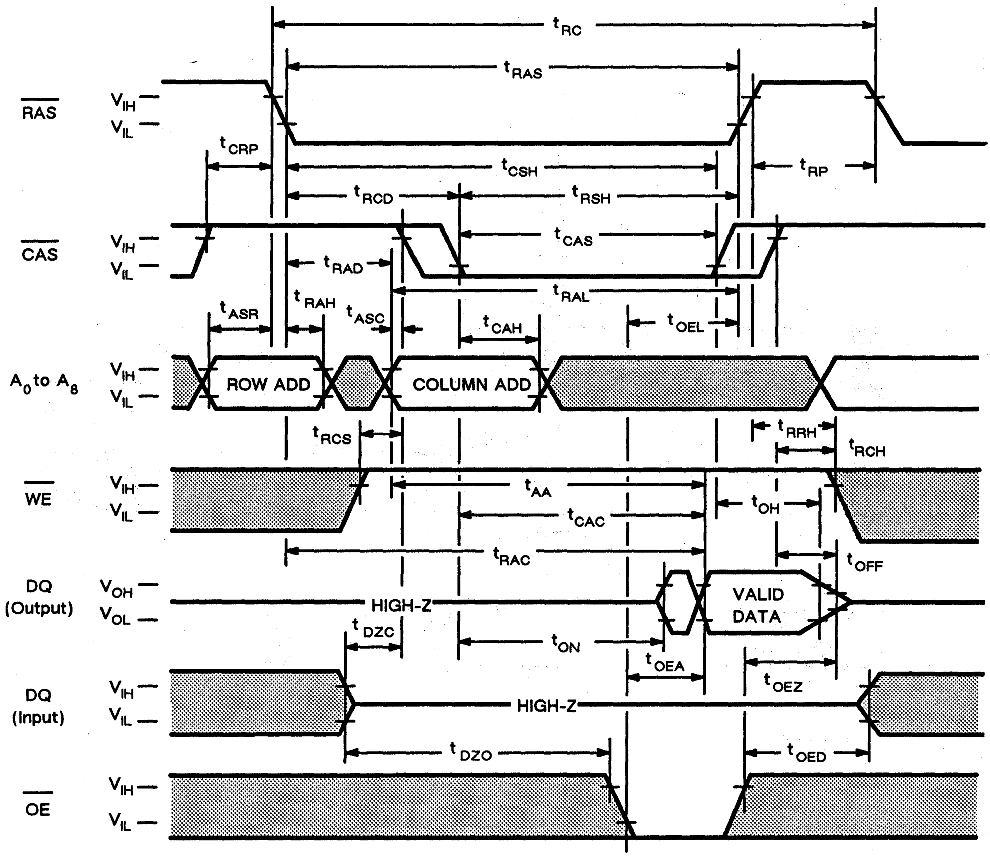
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	○ *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	○ *	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	○ *	
$\overline{RAS}$-only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	○	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High-Z	○	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh Cycle	H→L	L	X	L	—	—	—	Valid	○	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

TIMING DIAGRAMS

Fig. 4 - READ CYCLE



"H" or "L"

DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and, with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), $\overline{OE}$, (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

- If $t_{RCD} > t_{RCD}$ (max), access time = t_{CAC}.
- If $t_{RAD} > t_{RAD}$ (max), access time = t_{AA}.
- If $\overline{OE}$ is brought Low after t_{RAC} t_{CAC}, or t_{AA} (which ever occurs later), access time = t_{OEA}.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

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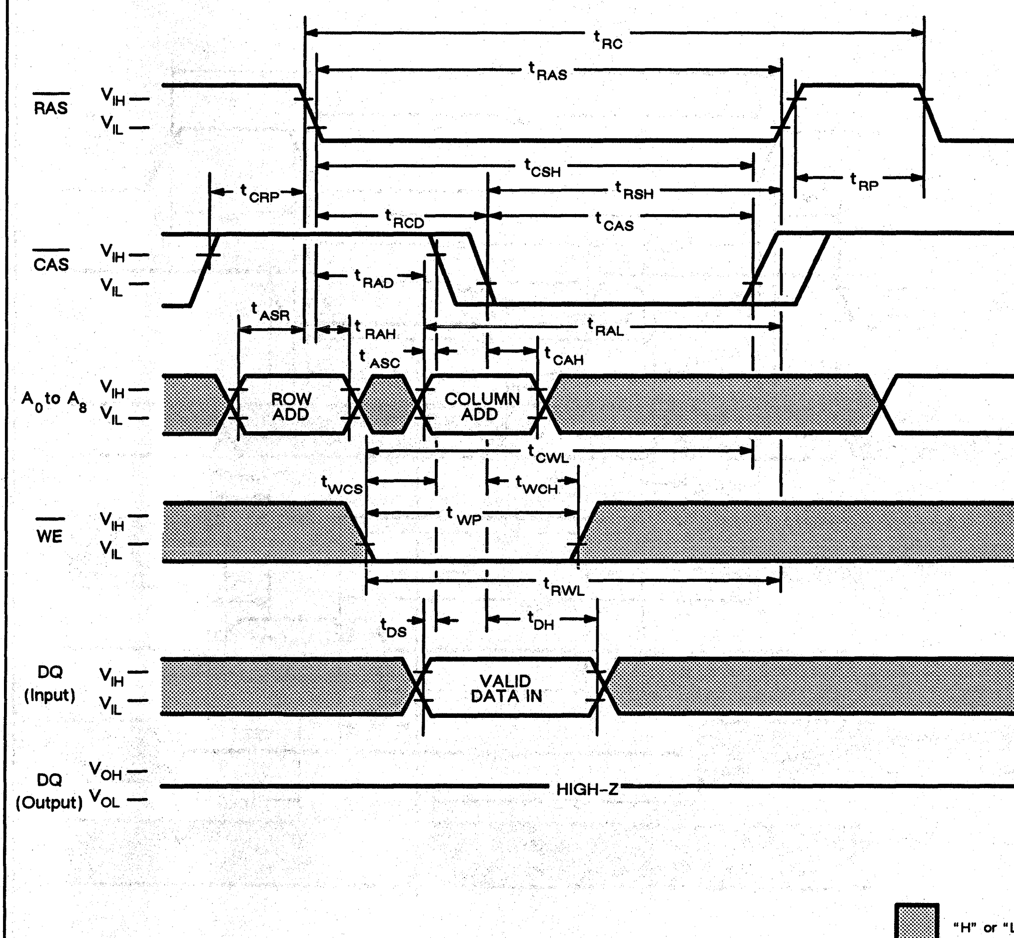
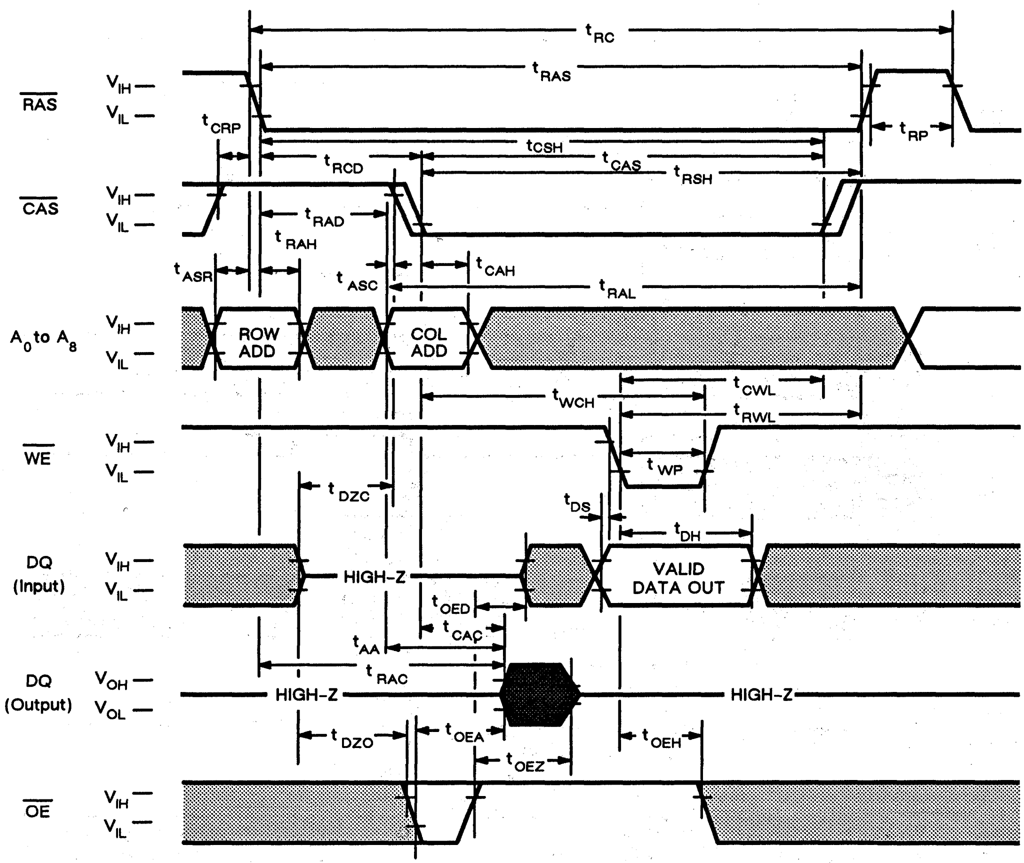
Fig. 5 — EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways — early write, $\overline{OE}$ write (delayed write), or read-modify-write. During all write cycles, timing parameters t_{RWL}, t_{CWL} and t_{RAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins is latched with the falling edge of $\overline{CAS}$ and written into memory.

Fig. 6 — $\overline{OE}$ (DELAYED WRITE CYCLE)

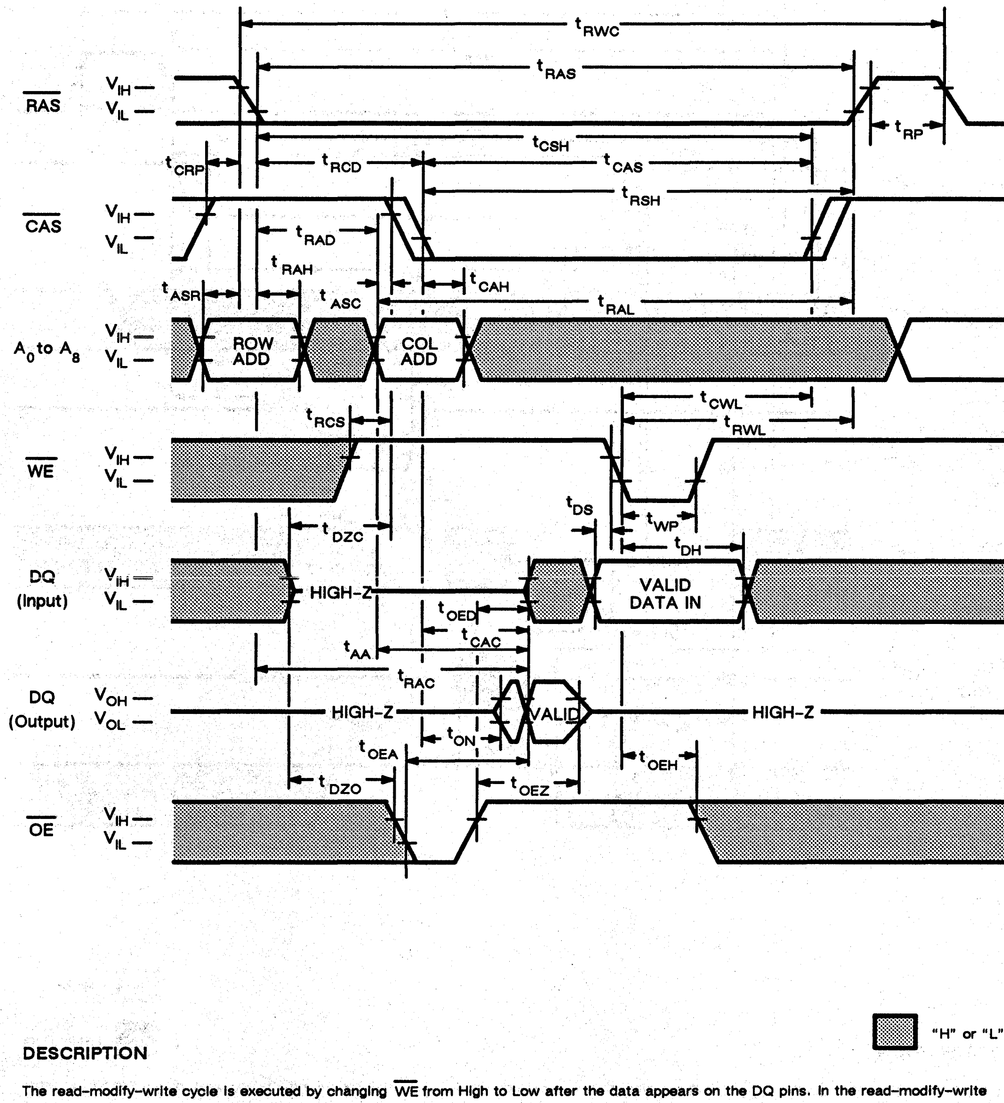


DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_{DS}$).

2

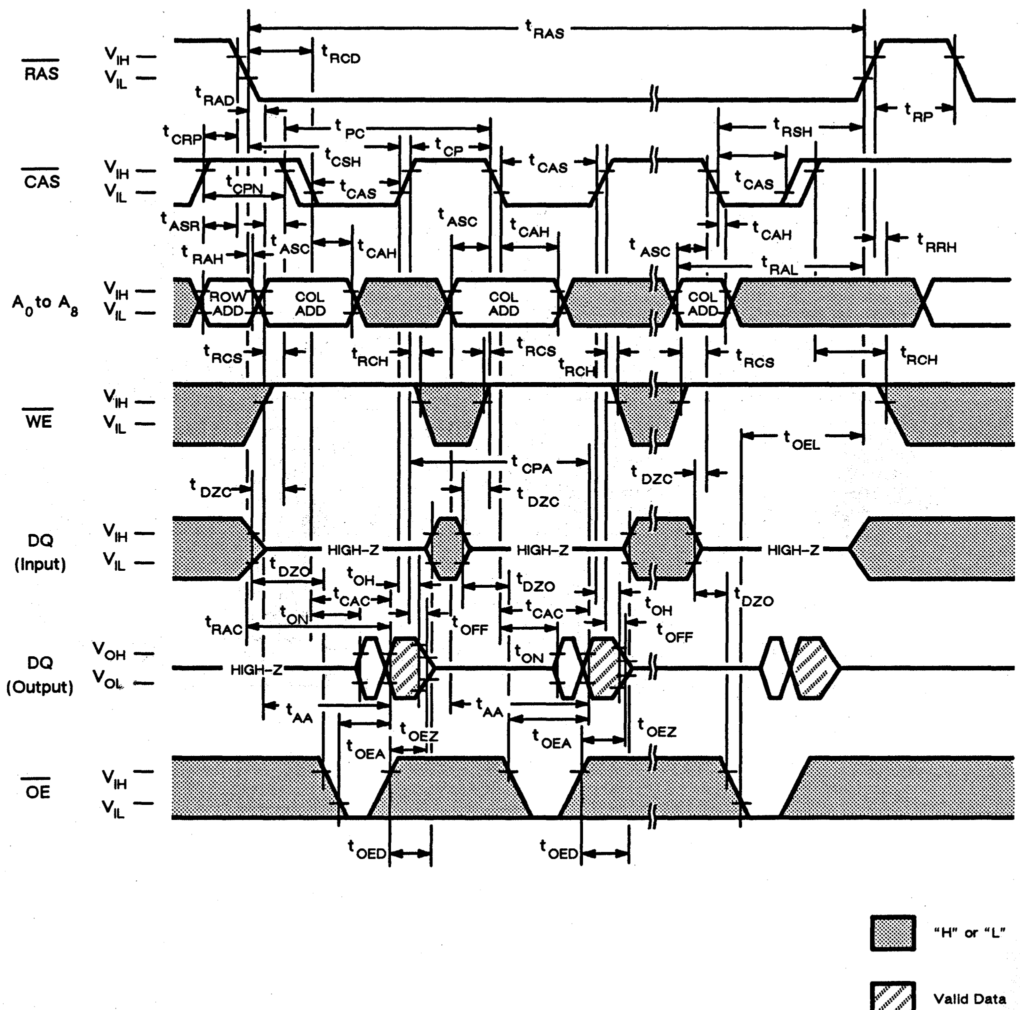
Fig. 7 — READ-MODIFY-WRITE-CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

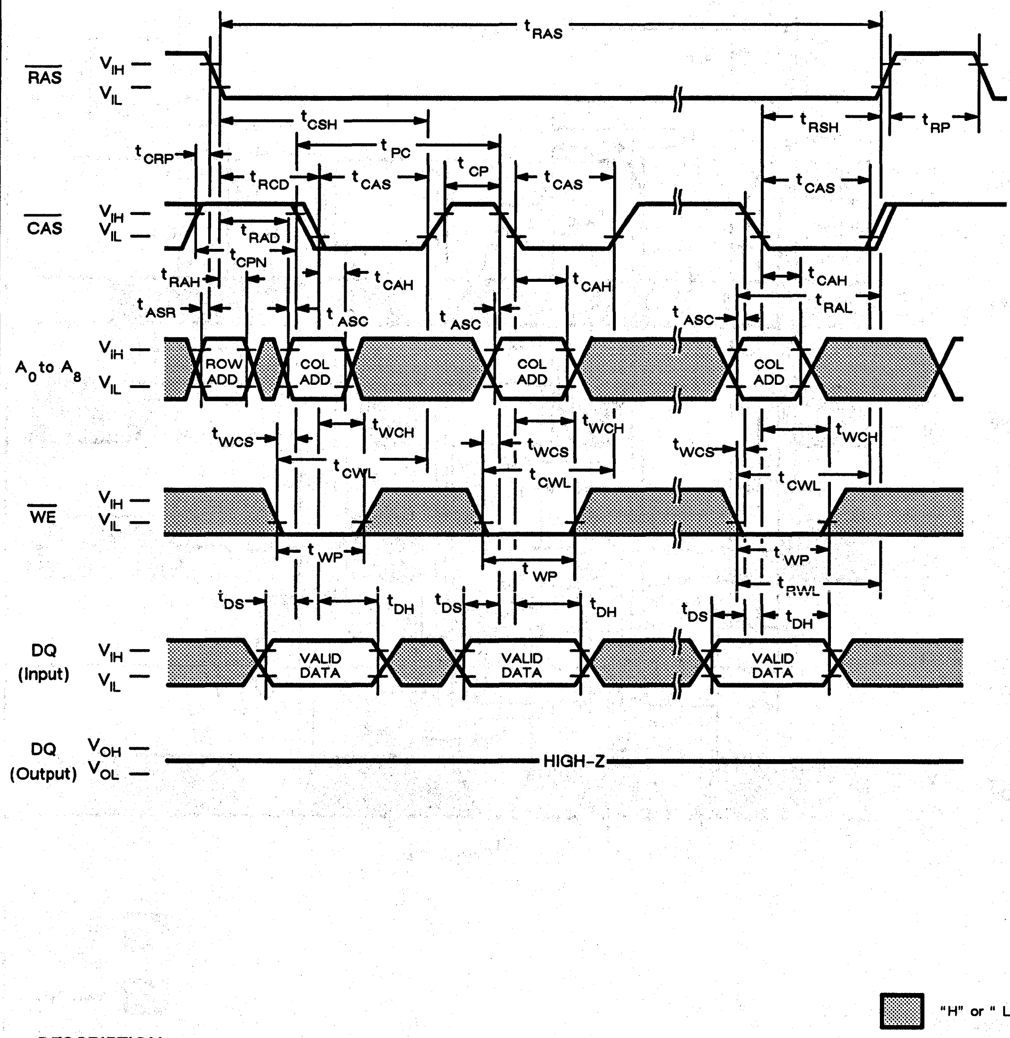
Fig. 8 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining RAS at a Low level and WE at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occuring.

Fig. 9 — FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")

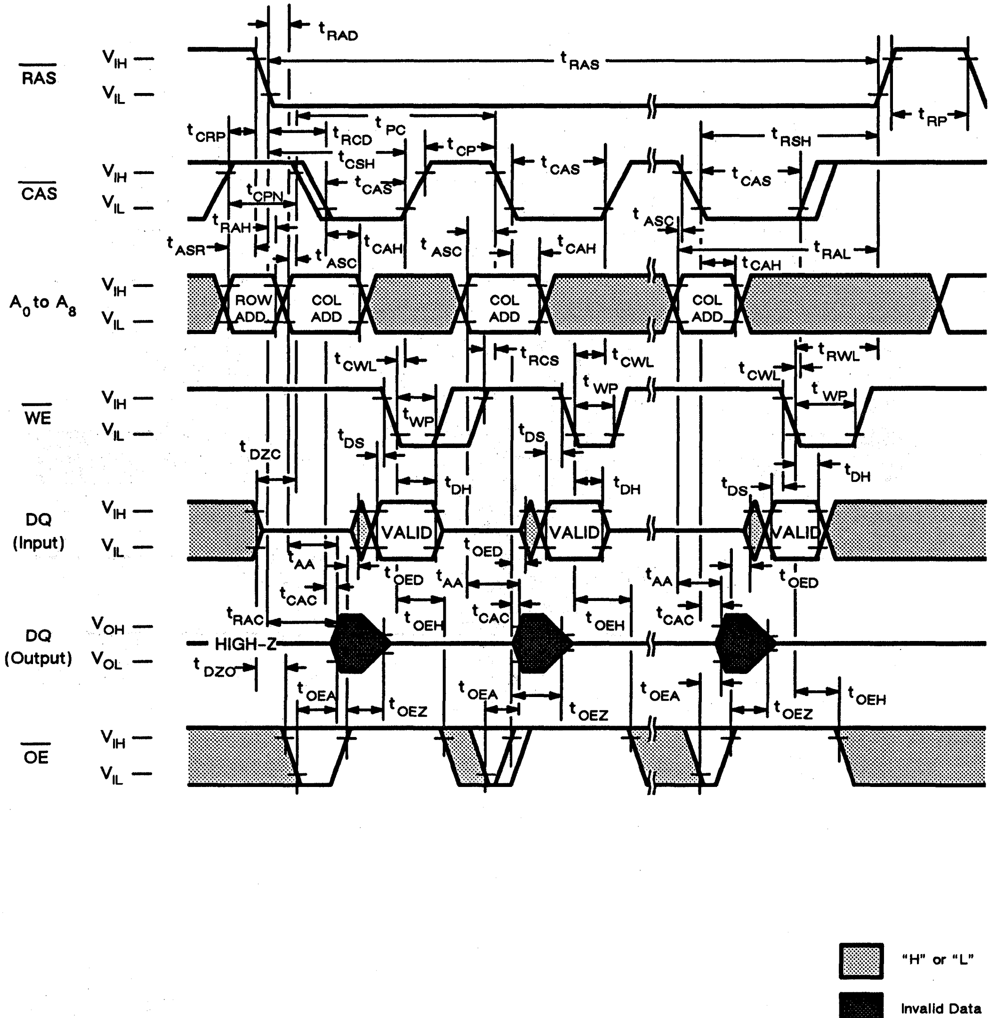


DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, t_{CWL} must be satisfied.

2

Fig. 10 — FAST PAGE MODE $\overline{OE}$ WRITE CYCLE

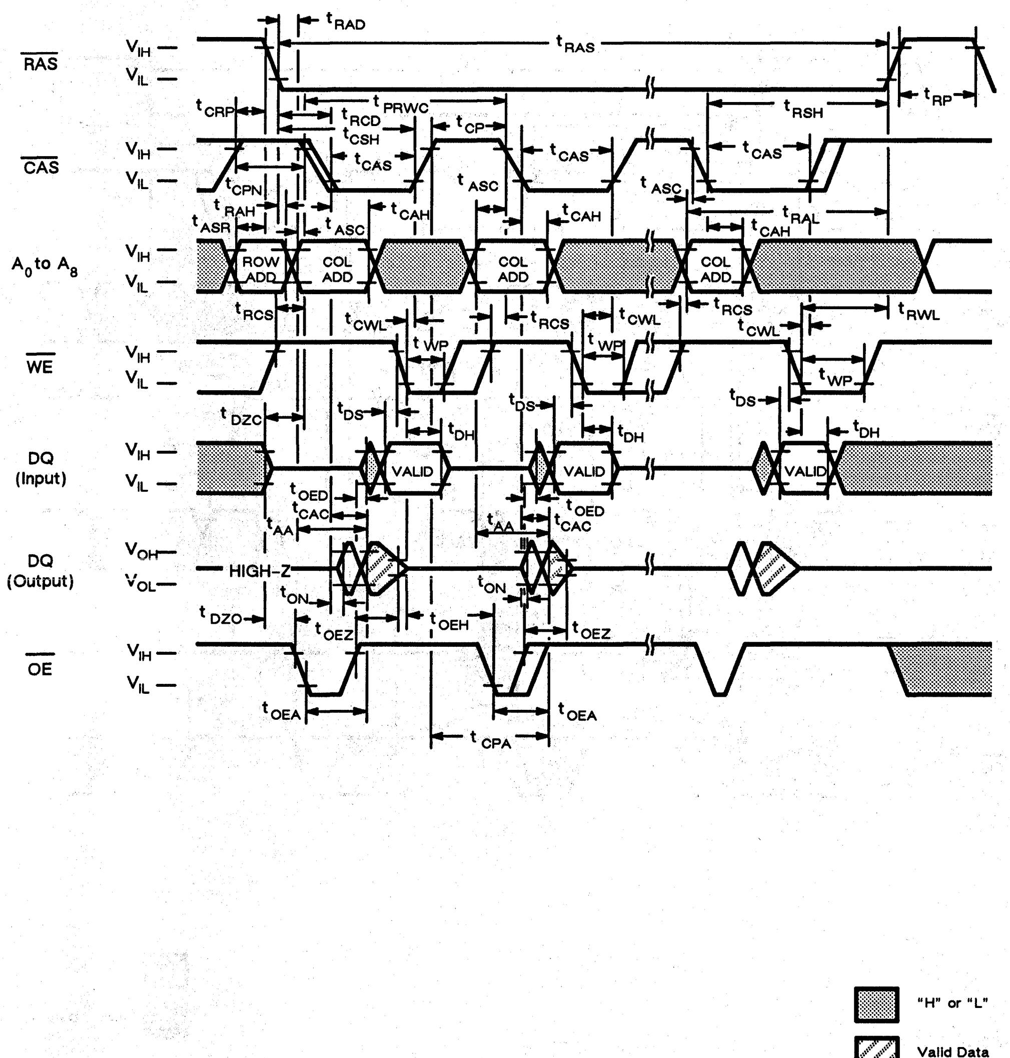


DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_{DS}$).

2

Fig. 11 – FAST PAGE MODE READ-MODIFY-WRITE CYCLE

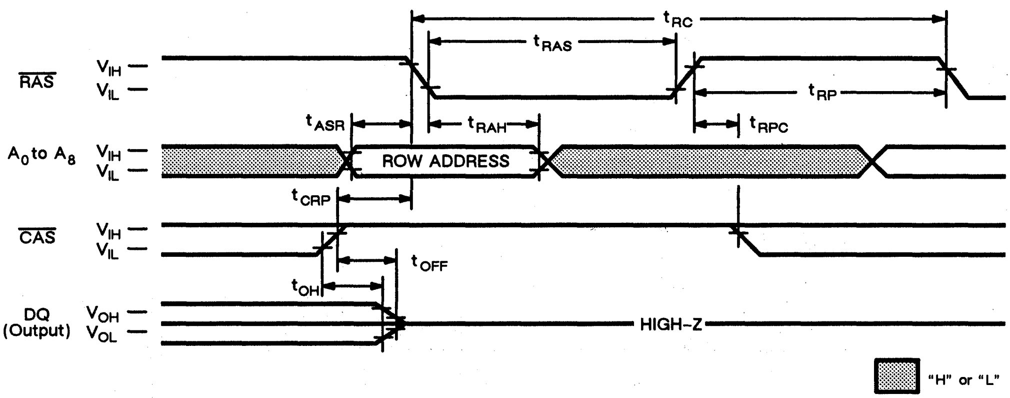


DESCRIPTION

During fast page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

2

Fig. 12 — $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

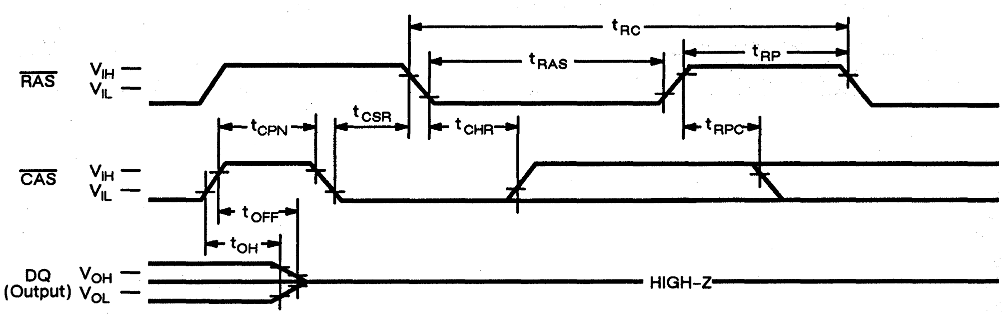


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

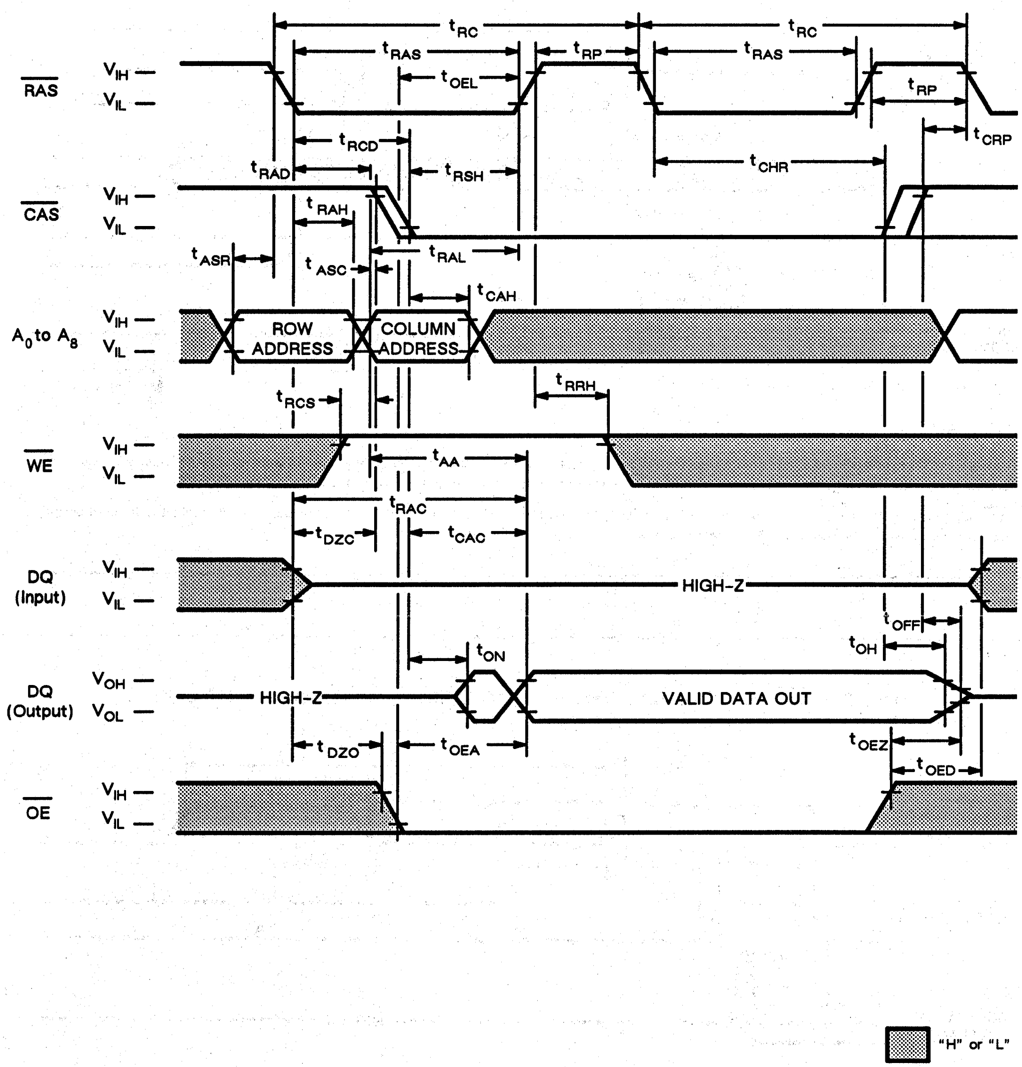
Fig. 13 — $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")



DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

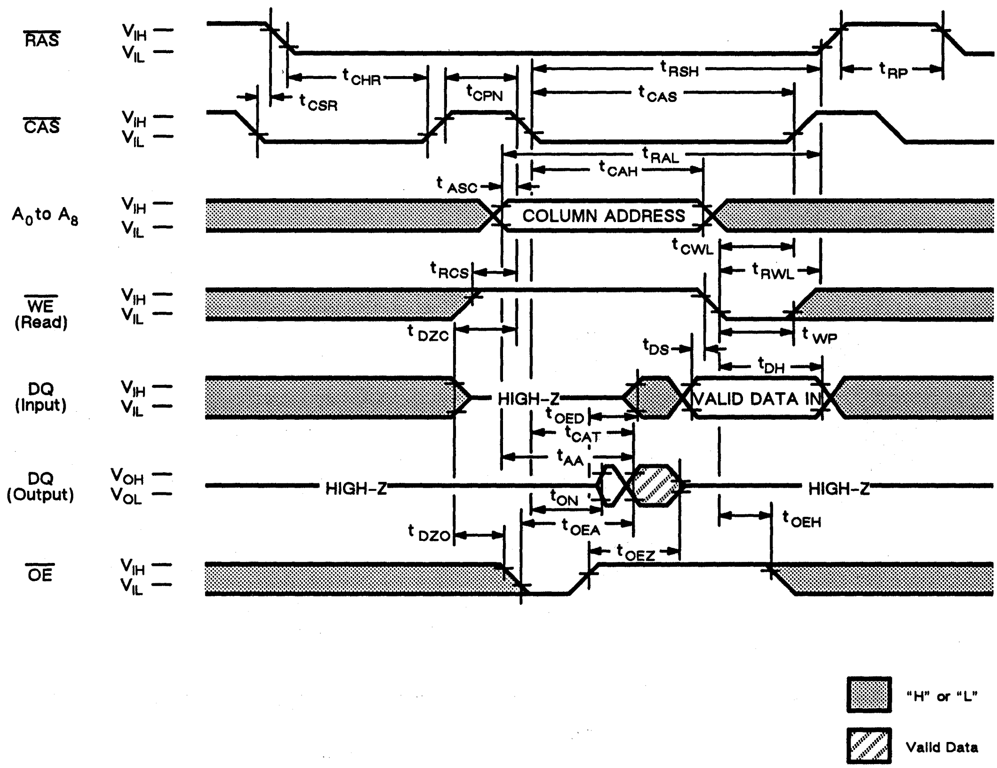
Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on–chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$ –before– $\overline{RAS}$ refresh capability.

Fig. 15 — $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above, Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle is designed for use with the following procedures:

- Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
- Use the same column address throughout the test.
- Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.
- Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read-write cycles. Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
- Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.
- Complement test pattern and repeat procedures 3, 4, and 5.

PACKAGE DIMENSIONS

(Suffix : –P)

20–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20P–M03)

PACKAGE DIMENSIONS (Continued)

(Suffix : -C)

20-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-A03)

2

PACKAGE DIMENSIONS (Continued)

(Suffix : -PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER (SOJ-26)
(CASE No.: LCC-26P-M01)

PACKAGE DIMENSIONS (Continued)

(Suffix : -PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)

2

FUJITSU

CMOS 1,048,576 BIT NIBBLE DYNAMIC RAM

MB81C4257-85 MB81C4257-10 MB81C4257-12

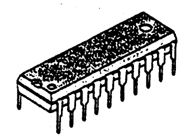
2

CMOS 262,144 X 4 BIT Nibble DYNAMIC RAM

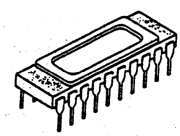
TS009-H87Z
December 1987

The Fujitsu MB81C4257 is a fully decoded CMOS Dynamic RAM (DRAM) that contains 1,048,576 memory cells accessible in 4-bit increments. The MB81C4257 features a nibble mode of operation whereby the user can serially access up to four bits of data at very high speed. The MB81C4257 DRAM is ideally suited for mainframes, buffers, hand-held computers, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81C4257 is only about one-fifth that of a conventional NMOS DRAM, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

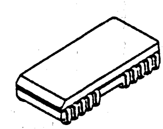
The MB81C4257 is fabricated using silicon gate CMOS and Fujitsu's advanced triple-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81C4257 are not critical and all inputs are TTL compartible.



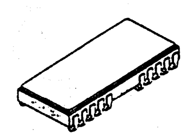
DIP-20P-M03



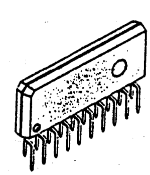
DIP-20C-A03



LCC-26P-M01



LCC-26C-A01



ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C4257-85	MB81C4257-10	MB81C4257-12
Row Access Time	85ns max.	100ns max.	120ns max.
Random Cycle Time	160ns min.	180ns min.	210ns min.
Column Address Time	50ns max.	50ns max.	60ns max.
Column Access Time	25ns max	30ns max.	35ns max.
Nibble Mode Cycle Time	60ns min.	60ns min.	70ns min.
Low Power Dussipation			
• Operating current	358mA max.	330mA max.	275mA max.
• Standby current	11mW max.(TTL level)/5.5mW max.(CMOS level)		

- On-chip latches for both address and data
- TTL compatible inputs and outputs
- Three-dimensional stacked capacitor memory cells
- 512 refresh cycles every 8.2ms
- RAS only, CAS-before-RAS, or Hidden refresh
- Both early and delayed (OE) write

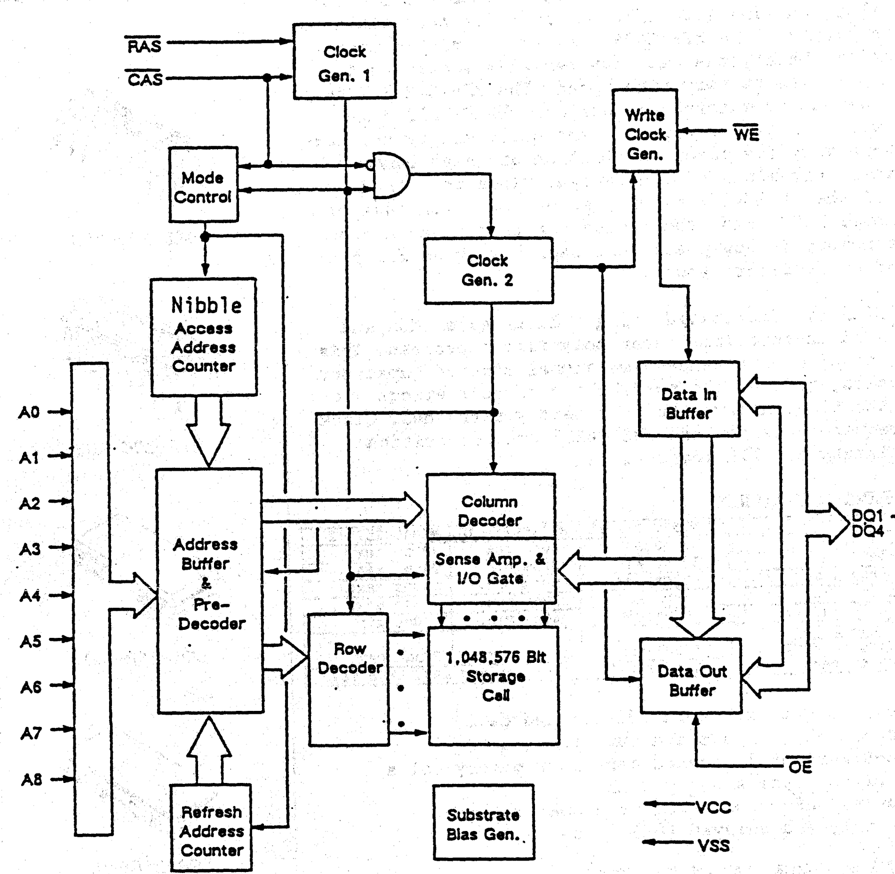
ABSOLUTE MAXIMUM RATINS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} Relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB81C4257 DYNAMIC RAM – BLOCK DIAGRAM



CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}		5	pF
Input Capacitance, RAS, CAS, WE, OE	C_{IN2}		5	pF
Input/Output Capacitance, (DQ1~DQ4)	C_{DQ}		6	pF

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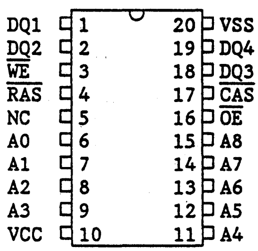
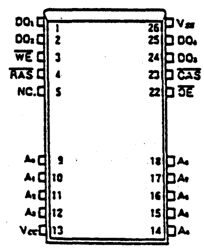
MB81C4257-85
MB81C4257-10
MB81C4257-12

PIN ASSIGNMENTS AND DESCRIPTIONS

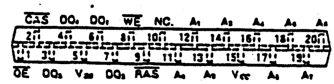
20–Pin DIP:
(TOP VEIW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	:	**Function**
DQ1 ~ DQ2 DQ3 ~ DQ4	:	When $\overline{\text{WE}}$ is Low, DQ1~DQ4 serve as data inputs; when $\overline{\text{WE}}$ is High, these pins provide output data.
$\overline{\text{WE}}$	:	When active Low, the write mode is enabled, when High, the read mode is enabled.
$\overline{\text{RAS}}$	:	Row address strobe.
NC	:	No connection.
A0 ~ A3 A4 ~ A8	:	Address inputs.
VCC	:	+5 volt power supply.
$\overline{\text{OE}}$	:	When active Low, enables output pins DQ1~DQ4
$\overline{\text{CAS}}$	:	Column address strobe.
VSS	:	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Volate	VCC	4.5	5.0	5.5	V	0°C to +70°C
	VSS	0	0	0		
Input High Voltage, all inputs	VIH	2.4		6.5	V	
Input Low Voltage, all inputs	VIL	-2.0		0.8	V	
Input Low Voltage, DQ	VILD*	-1.0	–	0.8	V	

* The device will withstand undershoots to the –2.0 level with a maximum pulse width of 20 ns at the –1.5 V level.

FUNCTIONAL OPERATION

Address Inputs;

Eighteen binary input address bits are required to select any 4 of 262,144 cell locations within the MB81C4257. Nine row address bits are placed onto the input pins(A0 to A8) and latched with the Row Address Strobe ($\overline{RAS}$) signal. Nine column address bits are then placed onto the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the address latch is flow through latch, address information at address pins are automatically latched as column address after tRAH(min)+tT. If tRAD ≥ tRAD(min) access time is t_{CAC} or t_{AA} whichever occur later.

Write Enable:

The read or write mode is determined by the $\overline{WE}$ input. If $\overline{WE}$=high, a read cycle is selected. If $\overline{WE}$=low, a write mode is selected. Data input is ignored during read mode.

Data Input:

Data are written to the MB81C4257 during a write (early write or $\overline{OE}$ write) or read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, is a strobe for the input data latch. In an early write cycle, data on DQ pins are strobed by $\overline{CAS}$, and the setup and hold times are referenced to $\overline{CAS}$ due to the $\overline{WE}$ is set low before $\overline{CAS}$. In a delayed write or read-write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus data on DQ pins are strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffers are three-state TTL-compatible with a fan-out of two standard TTL loads. Data Out are the same polarity as Data In. The outputs are in high impedance state until $\overline{CAS}$ goes low. In a read or read-write cycle, the outputs become valid after;

1) t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD}(max) is satisfied
2) t_{CAC} from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}(max)
3) tAA from column address input when tRAD is greater than tRAD(max).
4) tOEA from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought "L" after tRAC, tCAC, or tAA.

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to "H". In an early write cycle, the output buffers are in high impedance state during the entire cycle.

FUNCTIONAL OPERATION

Nibble Mode of Operation:

In the nibble mode of operation, the user can serially access from one to four bits of data and perform high-speed read, write, or read-modify-write operations. During the nibble mode, the accessed bits of data are determined by row address zero(0) and column address one(1). For initial access, address bits CA0 and CA1 are used to select one of four nibble bits. After the first bit accessed by this method, all remaining bits are accessed by simply toggling the column address strobe ($\overline{CAS}$) from High to Low. Each High-to-Low transition of $\overline{CAS}$ intermally increments CA0 and CA1 and provides access to the next nibble bit.

If more than four bits are accessed during the nibble mode, the address sequence shown in table 1 will repeat. Timing diagrams showing $\overline{RAS}$, $\overline{CAS}$, address, and read/write relationships are shown in Figures 6 through 10. AC parameters for each nibble mode of operation are shown in subsequent timing diagrams (Figures11 through 14).

Table 1 - NIBBLE MODE ADDRESS SEQUENCE

Sequence	Nibble Bit	Row Address.	Row CA0	Column Address	Col CA1	Remarks
$\overline{RAS}$/$\overline{CAS}$ (Normal mode)	1	101010101	0	101010101	0	Input address
Toggle $\overline{CAS}$ (Nibble mode)	2	101010101	1	101010101	0	Internally generated address
Toggle $\overline{CAS}$ (Nibble mode)	3	101010101	0	101010101	1	Internally generated address
Toggle $\overline{CAS}$ (Nibble mode)	4	101010101	1	101010101	1	Internally generated address
Toggle $\overline{CAS}$ (Nibble mode)	1	101010101	0	101010101	0	Sequence repeats

2

DC CHARACTERISTICS

(Recommendec operating conditions unless otherwise noted.)

Parameter		Symbol	Value Min	Value Typ	Value Max	Unit
OPERATING CURRENT* Average power supply current (RAS, CAS cycling;tRC=min)	MB81C4257-85	ICC1			65	mA
	MB81C4257-10				60	
	MB81C4257-12				50	
STANDBY CURRENT Power supply current	TTL level RAS=CAS=VIH	ICC2			2.0	mA
	CMOS level RAS=CAS≥VCC-0.2V				1.0	
REFRESH CURRENT 1* Average power supply current (CAS =VIH RAS cycling;tRC=min)	MB81C4257-85	ICC3			60	mA
	MB81C4257-10				55	
	MB81C4257-12				45	
NIBBLE MODE CURRENT * (RAS = V_{IL}, CAS = cycling; tNC= min)	MB81C4257-85	ICC4			40	mA
	MB81C4257-10				40	
	MB81C4257-12				33	
REFRESH CURRENT 2* Average power supply current (CAS-before-RAS; tRC = min)	MB81C4257-85	ICC5			60	mA
	MB81C4257-10				55	
	MB81C4257-12				45	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V≤VIN ≤5.5 V, 4.5≤VCC≤5.5V, VSS=0V, all other pins not under test=0V)		$I_{I(L)}$	-10		10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤VOUT≤5.5V)		IDQ(L)	-10		10	µA
OUTPUT LEVELS Output high voltage (I_{OH} =-5mA)		VOH	2.4			V
Output low voltage(IOL=4.2mA)		VOL			0.4	V

*: ICC depends on the output load conditions, input levels, and cycle rate.
The specified values are obtained with the output open.
ICC also depends in input low voltage level, VILD, VILD≥-0.5V.

C CHARACTERISTICS

At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB81C4257-85		MB81C4257-10		MB81C4257-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	Time Between Refresh	tREF		8.2		8.2		8.2	ms	
2	Random Read/Write Cycle Time	tRC	160		180		210		ns	
3	Read-Modify-Write Cycle Time	tRWC	220		240		275		ns	
4	Access Time from RAS	tRAC		85		100		120	ns	4,7
5	Access Time from CAS	tCAC		25		30		35	ns	5,7
6	Access Time from Column Address	tAA		50		50		60	ns	6,7
7	Output Hold Time	tOH	7		7		7		ns	
8	Output Buffer Turn On Delay Time	tON	5		5		5		ns	
9	Output Buffer Turn off Delay Time	tOFF		25		25		25	ns	8
10	Transition Time	tT	3	50	3	50	3	50	ns	
11	RAS Precharge Time	tRP	65		70		80		ns	
12	RAS Pulse Width	tRAS	85	100000	100	100000	120	100000	ns	
13	RAS Hold Time	tRSH	25		30		35		ns	
14	CAS to RAS Precharge Time	tCRP	0		0		0		ns	
15	RAS to CAS Delay Time	tRCD	22	60	25	70	25	85	ns	9,10
16	CAS Pulse Width	tCAS	25		30		35		ns	
17	CAS Hold Time	tCSH	85		100		120		ns	
18	CAS Precharge Time(Normal)	tCPN	15		15		15		ns	
19	Row Address Set Up Time	tASR	0		0		0		ns	
20	Row Address Hold Time	tRAH	12		15		15		ns	
21	Column Address Set Up Time	tASC	0		0		0		ns	
22	Column Address Hold Time	tCAH	15		15		20		ns	
23	RAS to Column Address Delay Time	tRAD	17	35	20	50	20	60	ns	11
24	Column Address to RAS Lead Time	tRAL	45		50		60		ns	
25	Read Command Set Up Time	tRCS	0		0		0		ns	
26	Read Command Hold Time Referenced to RAS	tRRH	0		0		0		ns	12
27	Read Command Hold Time Referenced to CAS	tRCH	0		0		0		ns	12
28	Write Command Set Up Time	tWCS	0		0		0		ns	15
29	Write Command Hold Time	tWCH	15		15		20		ns	
30	WE Pulse Width	tWP	15		15		20		ns	
31	Write Command to RAS Lead Time	tRWL	25		25		30		ns	
32	Write Command to CAS Lead Time	tCWL	20		20		25		ns	
33	DIN set Up Time	tDS	0		0		0		ns	
34	DIN Hold Time	tDH	15		15		20		ns	

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MB81C4257-85
MB81C4257-10
MB81C4257-12

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AC CHARACTERISTICS - Continued -

(At Recommended operating conditions unless otherwise noted)   Note 1, 2, 3

No.	Parameter	Symbol	MB81C4256-85		MB81C4256-10		MB81C4256-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
35	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	tRPC	0		0		0		ns	
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	tCSR	0		0		0		ns	
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before $\overline{RAS}$ Refresh	tCHR	15		15		20		ns	
38	Access Time from $\overline{OE}$	tOEA		22		25		30	ns	7
39	Output Buffer Turn Off Delay from $\overline{OE}$	tOEZ		25		25		25	ns	8
40	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data	tOEL	10		10		10		ns	
41	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	tOEH	0		0		0		ns	13
42	$\overline{OE}$ to Data In Dealy Time	tOED	25		25		25		ns	
43	DIN to $\overline{CAS}$ Delay Time	tDZC	0		0		0		ns	14
44	DIN to $\overline{OE}$ Delay Time	tDZO	0		0		0		ns	14
45	Access Time from $\overline{CAS}$ (Counter Test Cycle)	tCAT		50		50		60	ns	
50	Nibble Mode Read/Write Cycle Time	tNC	60		60		70		ns	
51	Nibble Mode Read-Modify-Write Cycle Time	tNRWC	115		115		130		ns	
52	Access Time from Nibble Mode $\overline{CAS}$ Precharge	tNPA		60		60		70	ns	7,1[illegible]
53	Nibble Mode $\overline{CAS}$ Precharge Time	tNCP	15		15		15		ns	

Notes;

1. An Initial pause($\overline{RAS}$=$\overline{CAS}$=VIH) of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T=5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amout that tRCD exceeds the value shown. Refer to Fig.2 and 3.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$(max). If $t_{ASC} \geq t_{AA}-t_{CAC}-t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$(max) and $t_{ASC} \leq t_{AA}-t_{CAC}-t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance sate.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max)is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max)limit, access time is controlled exclusively by t_{CAC} or tAA.
10. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min)
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only; If t_{RAD} is greater than the specified t_{RAD}(max) limit, access time is controlled exclusively by t_{CAC} or tAA.
12. Either t_{RRH} or t_{RCH} must be satisfed for a read cycle.
13. Assumes that $t_{WCS} < t_{WCS}$(min).
14. Either t_{DZC} or t_{DZO} must be satisfied.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$(min) the data output pin will remain High-Z state through entire cycle.
16. tNPA is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ From "L" to "H"). Therefore, if tNCP is short, tCAC is longer than tCAC(max).

Fig. 2 – tRAC vs. tRCD

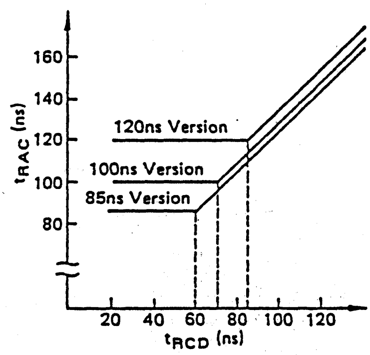
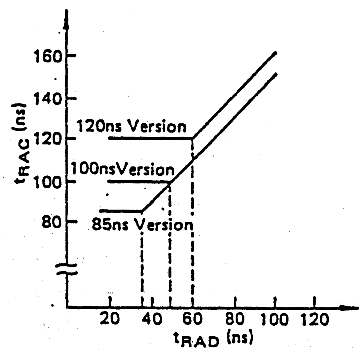


Fig. 3 – tRAC vs. tRAD

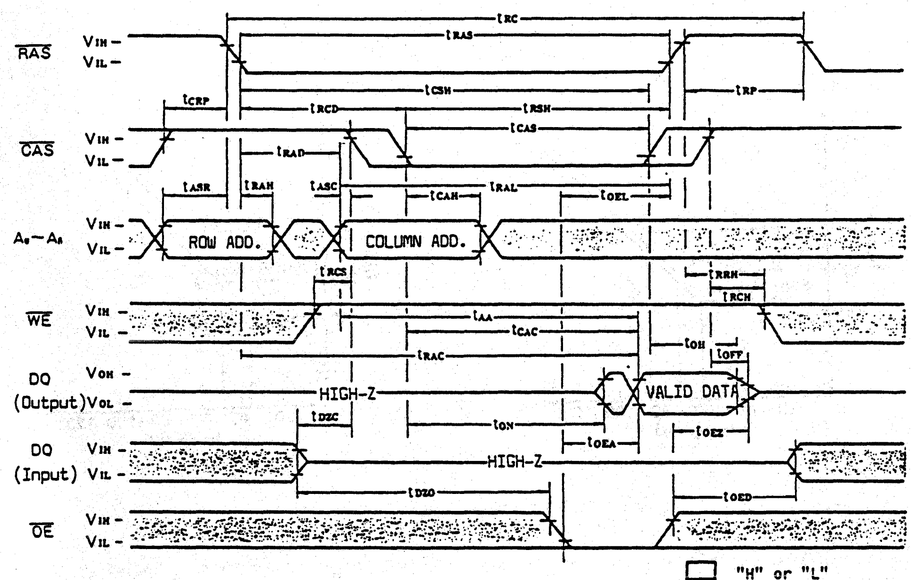


FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	RAS	CAS	WE	OE	Row	Column	Input	Output		
Standby	H	H	X	X	–	–	–	High-Z	–	
Read Cycle	L	L	H	L	Valid	Valid	–	Valid	○ *	tRCS≥tRCS(min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	○ *	tWCS≥tWCS(min)
Read-Modify-Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	○ *	
RAS-only Refresh Cycle	L	H	X	X	Valid	–	–	High-Z	○	
CAS-before-RAS Refresh Cycle	L	L	X	X	–	–	–	High-Z	○	tCSR≥tCSR(min)
Hidden Refresh Cycle	H→L	L	X	L	–	–	–	Valid	○	Previous data is kept.

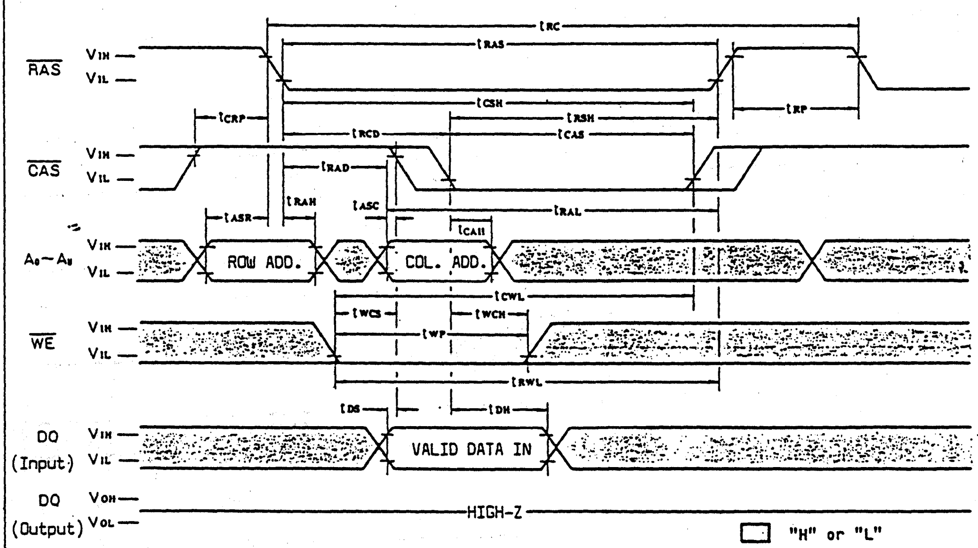
X; "H" or "L"
*; It is impossible in Nibble Mode

Read Cycle

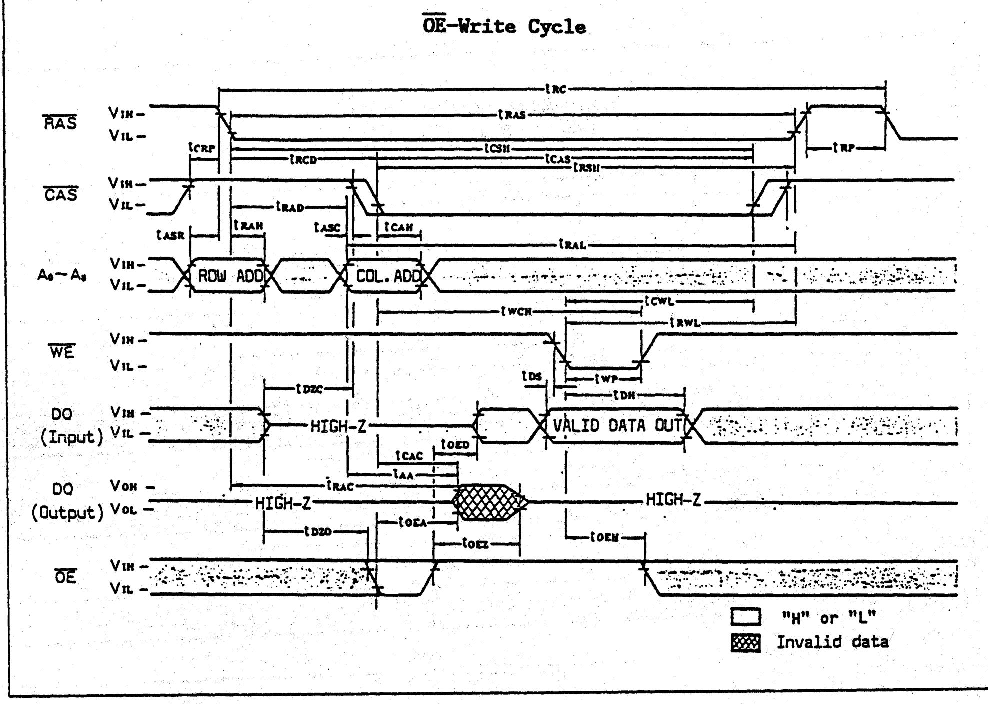


Read Cycle;
The read cycle is executed by keeping both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ "L" and keeping $\overline{\text{WE}}$ "H" throughout the cycle. The row and column addresses are latched with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, respectively. The data outputs remain valid with $\overline{\text{CAS}}$ "L" or $\overline{\text{OE}}$ "L", i.e., if $\overline{\text{CAS}}$ goes "H" or $\overline{\text{OE}}$ goes "H", the data becomes invalid with tOH. The access time is determined by $\overline{\text{RAS}}$(tRAC), $\overline{\text{CAS}}$(tCAC), $\overline{\text{OE}}$(tOEA) or Column address input(tAA). If tRCD($\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time) is greater than the specification, the access time is tCAC. If tRAD is greater than the specification, the access time is tAA. And if $\overline{\text{OE}}$ is brought "L" after tRAC, tCAC, or tAA, whichever occurs later, the access time is tOEA.

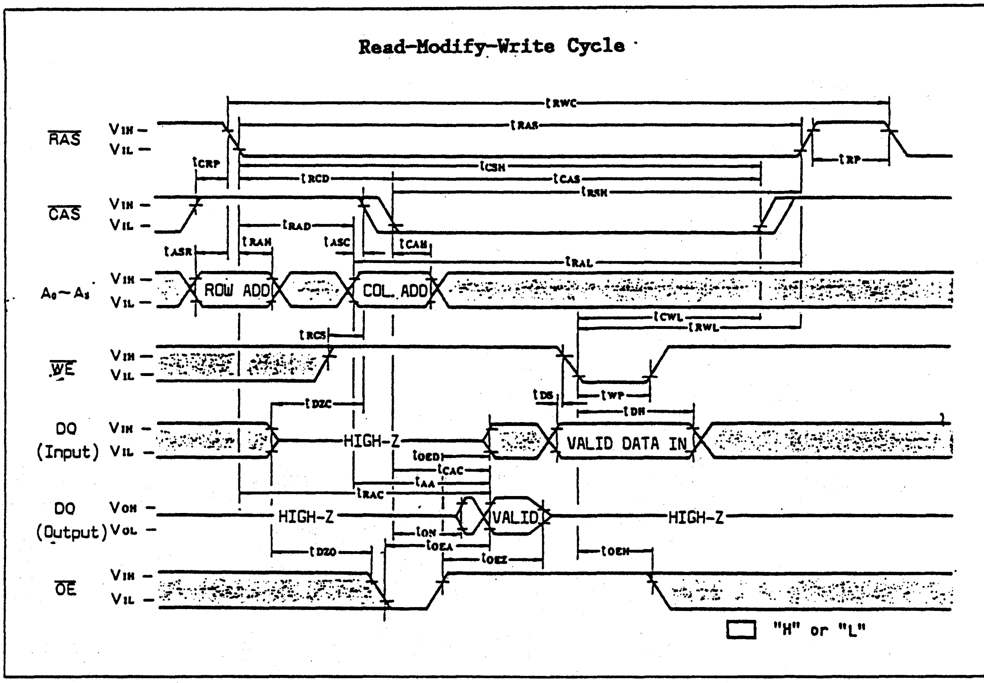
Write Cycle (Early Write)
($\overline{OE}$: "H" or "L")



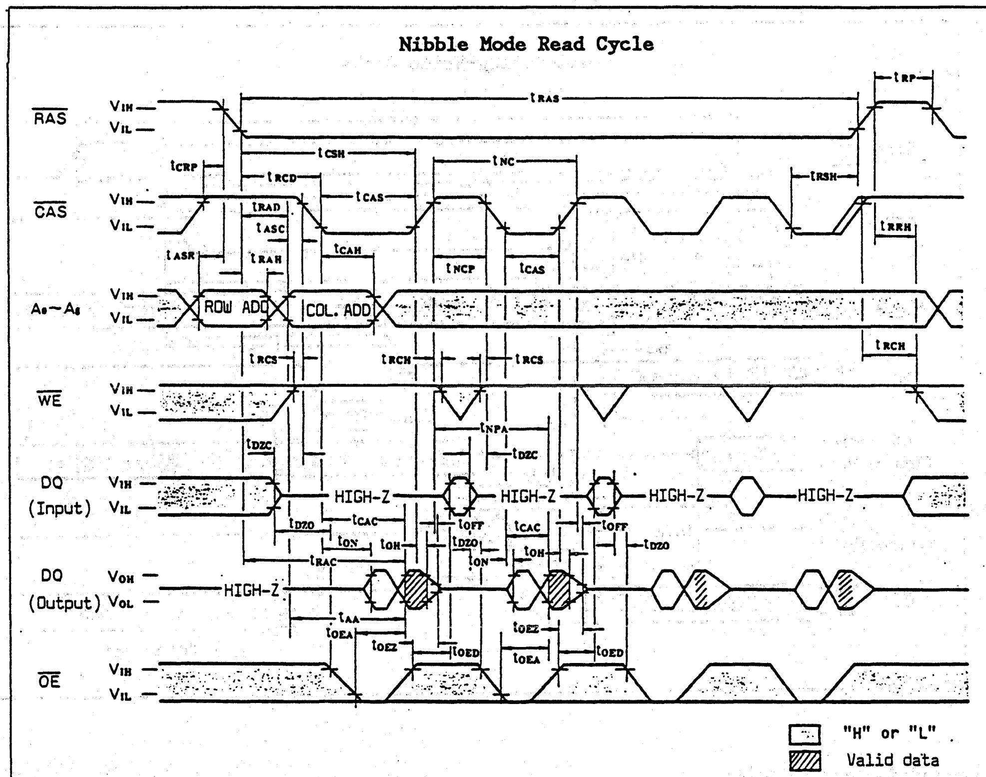
Early-Write Cycle;
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and $\overline{OE}$ pin. There are three types of write cycles, early-write, $\overline{OE}$-write(delayed write), and read-modify-write cycles. During all write cycles, tRWL, tCWL and tRAL must be satisfied.
In an early write cycle, tWCS is satisfied, data on DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory, and $\overline{OE}$ is a "don't care" signal.



OE-Write Cycle;
In the OE write cycle, tWCS is not satisfied, the data on DQ pins is latched on the falling edge of WE and written into memory, and OE must be changed from "L" to "H" before WE goes "L" with tOED+tDS.

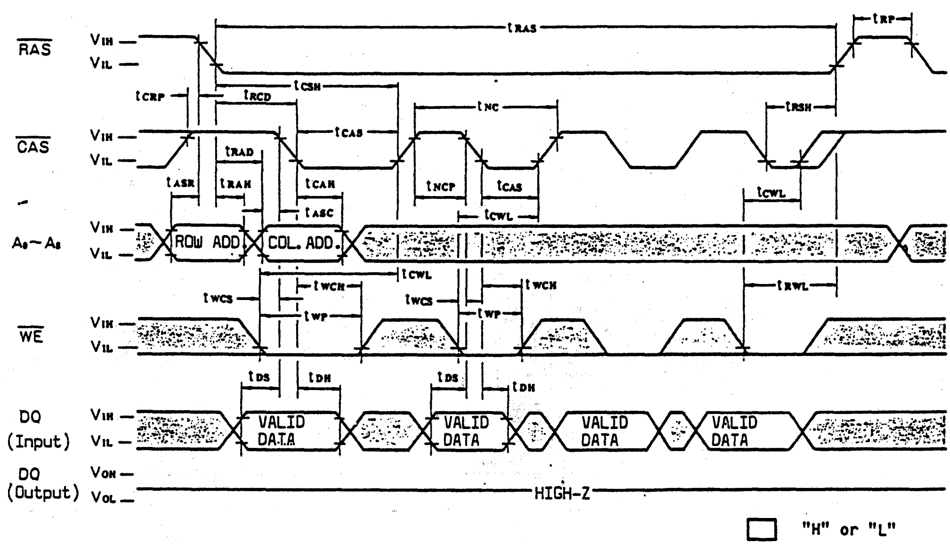


Read-Modify-Write Cycle;
The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from "L" to "H" after the memory access time.



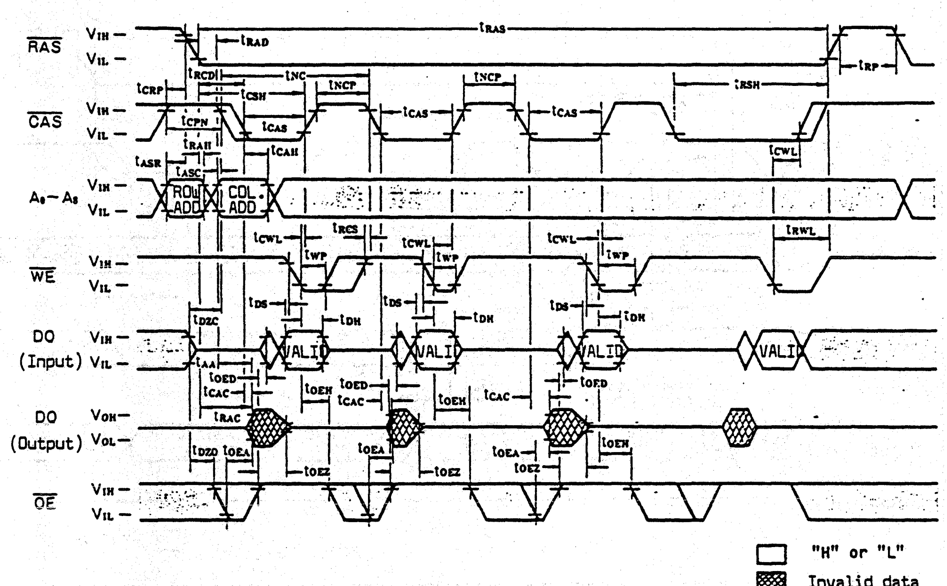
Nibble Read/Write Cycle;
Nibble mode allows high speed serial read, write, or read-modify-write access of 2, 3, or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 9 row and 9 column addresses. The 2 bits of addresses(RA9 and CA9) are used to select one of four nibble bits for initial access. After the first bits is accessed by normal mode, the remaining nibble bits can be accessed by toggling $\overline{CAS}$ "H" then "L". Toggling $\overline{CAS}$ causes RA9 and CA9 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. If more than four bits are accessed during nibble mode, the address sequence will begin to repeat.

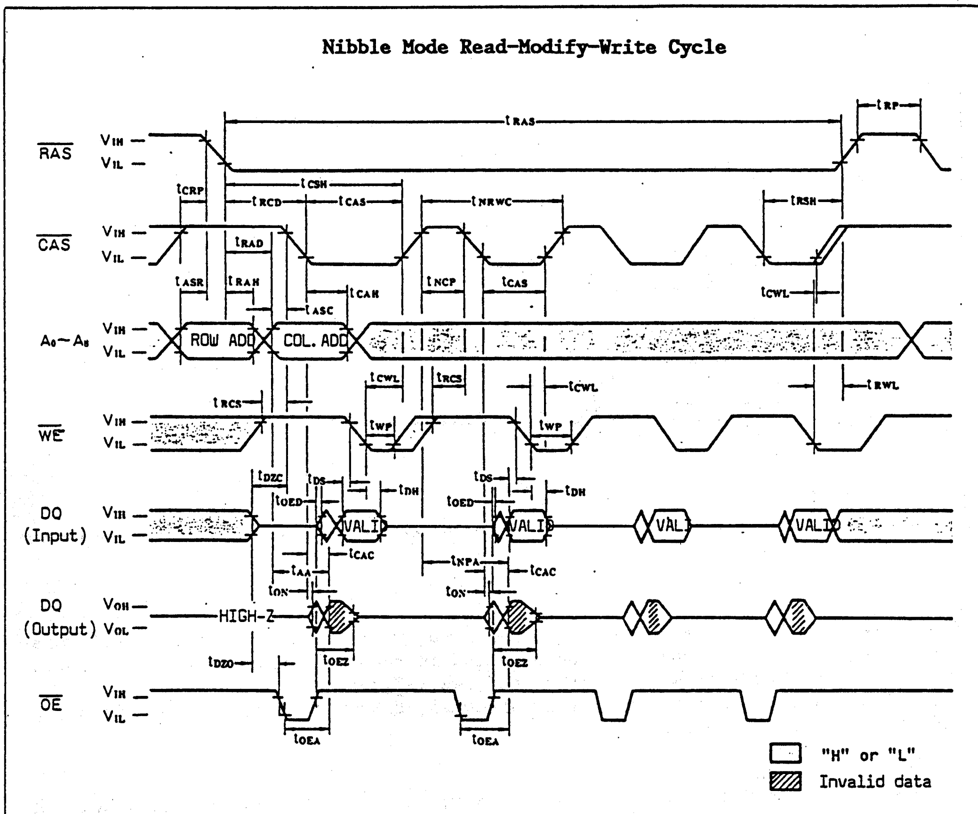
Nibble Mode Write Cycle
($\overline{OE}$; "H" or "L")

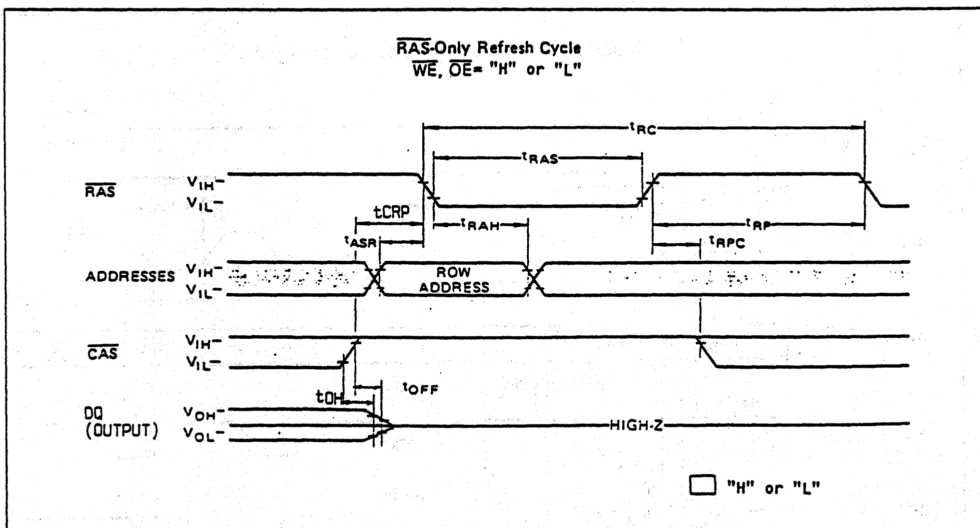


2

Nibble Mode OE-Write Cycle



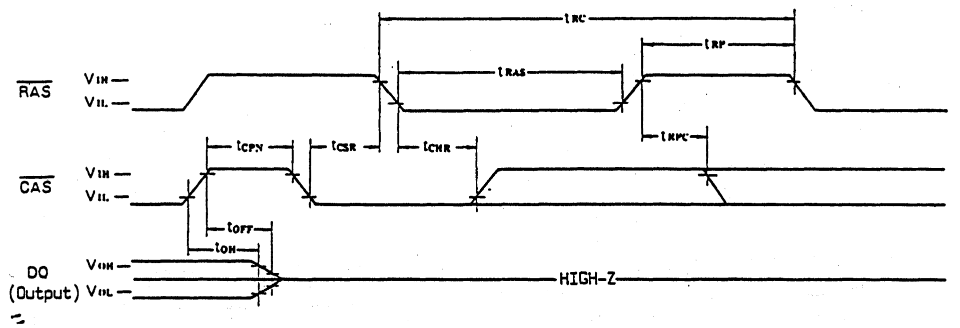

Nibble Mode Read-Modify-Write Cycle
RAS
CAS
A0~A8
WE
DQ (Input)
DQ (Output)
OE
VIH
VIL
VOH
VOL
tRAS
tRP
tCRP
tCSH
tRCD
tCAS
tNRWC
tRSH
tRAD
tASR
tRAH
tCAH
tASC
tNCP
tCWL
ROW ADD
COL. ADD
tRCS
tWP
tRWL
tDZC
tDS
tDH
tOED
VALID
tCAC
tAA
tNPA
tON
HIGH-Z
tDZO
tOEZ
tOEA
"H" or "L"
Invalid data



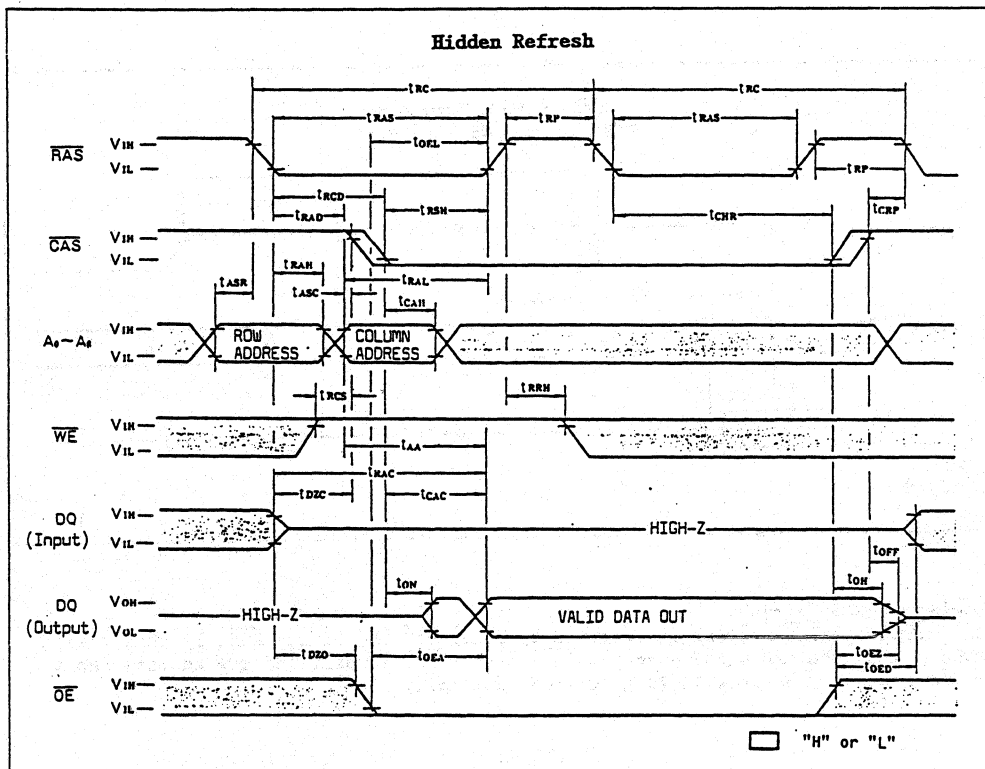
Refresh;
The refresh of DRAM is executed by normal read, write or read-modify write cycle, i.e., the cells on the one row line are also refreshed by executing one of three cycles. 512 row address must be refreshed every 8.2ms period.
The MB81C4257 has three types of refresh modes, $\overline{RAS}$-Only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and Hidden refresh.

$\overline{RAS}$-Only Refresh;
The $\overline{RAS}$ only refresh is executed by keeping $\overline{RAS}$ "L" and $\overline{CAS}$ "H" throughout the cycle. The row address to be refreshed is latched on the faling edge of $\overline{RAS}$. During $\overline{RAS}$-Only refresh, the DQ pins are kept in a high impedance state.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle
NOTE: Addresses, $\overline{WE}$, $\overline{OE}$ = "H" or "L"

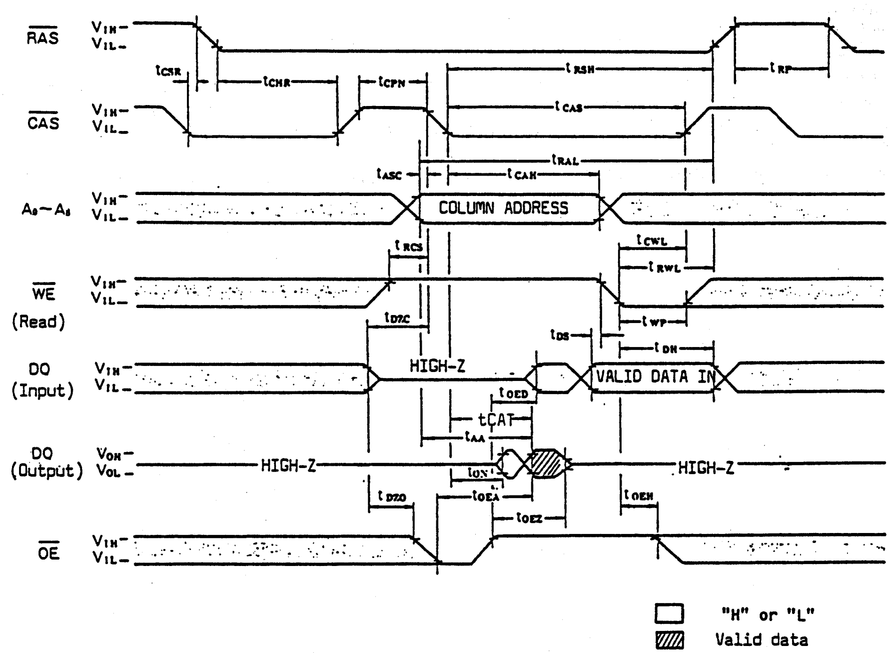


$\overline{CAS}$-before-$\overline{RAS}$ Refresh;
The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bring $\overline{CAS}$ "L" before $\overline{RAS}$. By this timing combination, the MB81C4257 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.



Hidden Refresh;
The Hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next $\overline{CAS}$-before-$\overline{RAS}$ Refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle;
A special timing sequence using $\overline{CAS}$-beore-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, if $\overline{CAS}$ makes a transtiion from "H" to "L" while $\overline{RAS}$ is held "L", read and write operation are enabled. This is shown in $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits) to be accessed are defined as follows.

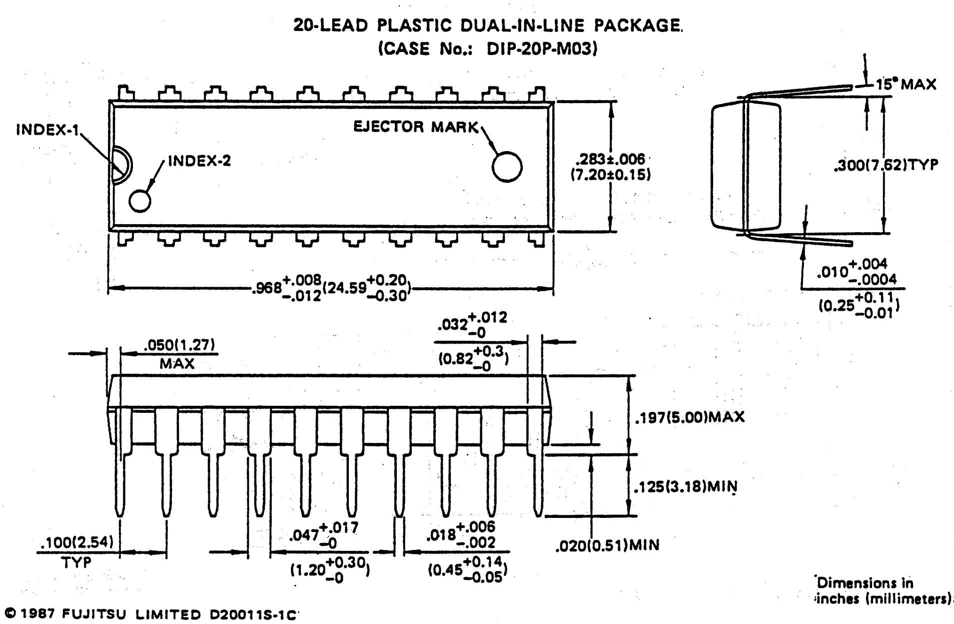
ROW ADDRESS -- Bits A0 to A8 are defined by the on chip refresh counter.
COLUMN ADDRESS -- All bits A0 to A8 are defined by latching levels on A0 to A8 at the second falling edge of $\overline{CAS}$.

2

Recommended $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle;
The timing, shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter Test Cycle, is used with the following procedures.

1) Initialize the internal refresh address counter circuitry by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Write "0"s to all 512 row addresses at the same column address by using normal early write cycles.
4) Read "0" written in step 3) and check, and simultaneously write "1" to the same address by using internal refresh counter test read-write cycles. This step is repeated 512 times with the address generated by internal refresh address counter.
5) Read and check data written in step 4) by using normal read cycle for all 512 locations.
6) Complement the test pattern and repeat step 3), 4), and 5).

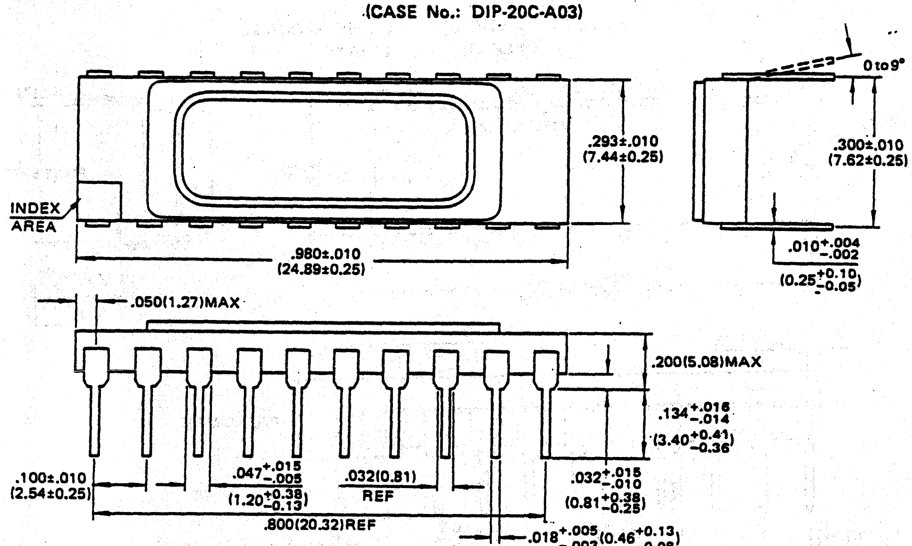
PACKAGE DIMENSIONS



2

PACKAGE DIMENSIONS

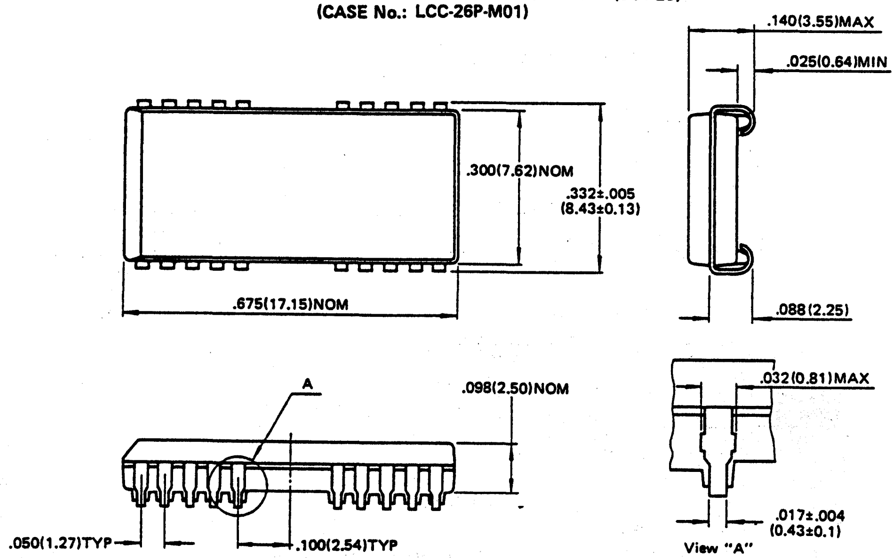
20-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-A03)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

26-LEAD PLASTIC LEADED CHIP CARRIER (SOJ-26)
(CASE No.: LCC-26P-M01)



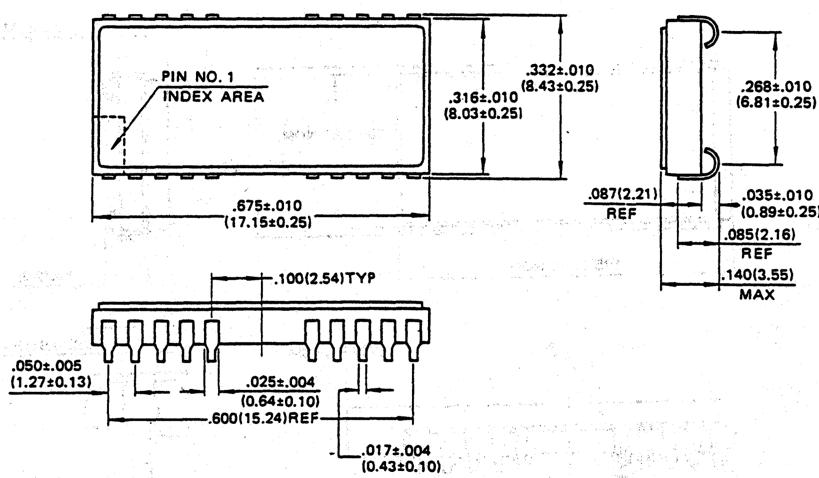
NOTE : Although this package has 20 leads only, its pin positions are the same as that of 26-lead package. Foot-print compatible with "SOJ-26", LCC-26C-A01)

Dimensions in inches (millimeters)

2

PACKAGE DIMENSIONS

26-LEAD CERAMIC LEADED CHIP CARRIER
(CASE No.: LCC-26C-A01)

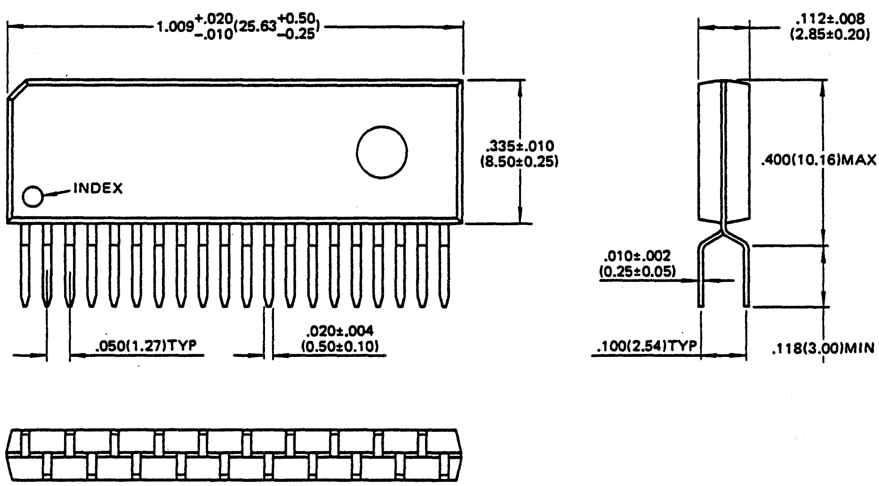


NOTE : Although this package has 20 leads only, its pin positions are the same as that of 26-lead package. Foot-print compatible with "SOJ-26", LCC-26P-A01

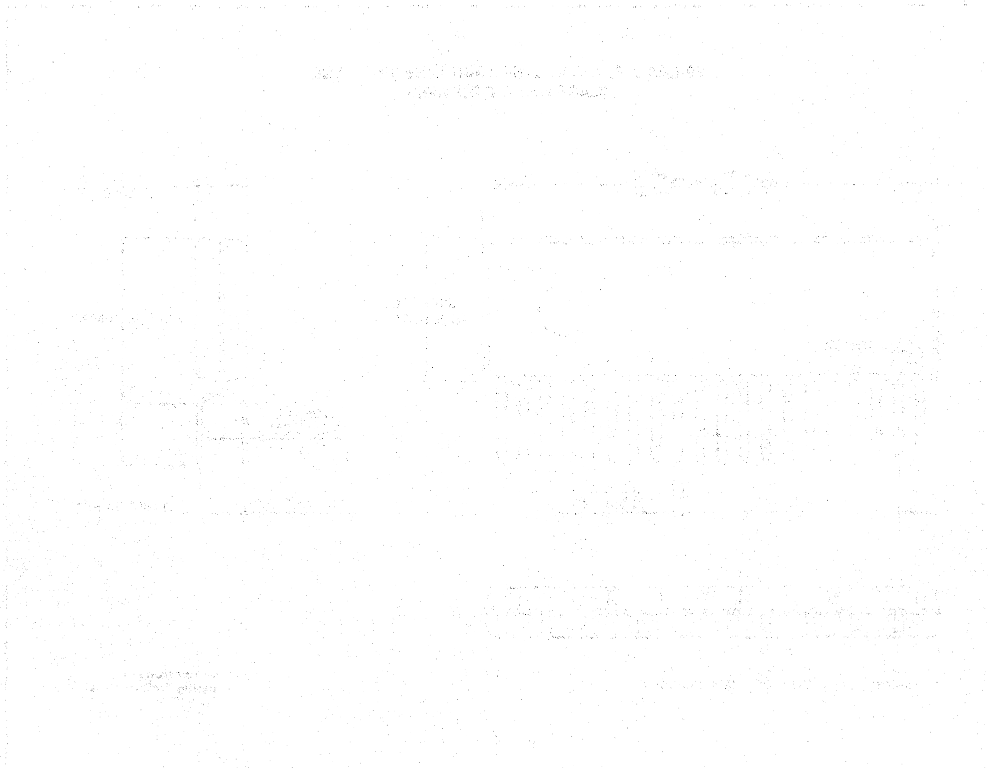
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)



Dimensions in inches (millimeters)



FUJITSU

CMOS 1,048,576 BIT STATIC COLUMN DYNAMIC RAM

MB81C4258-85
MB81C4258-10
MB81C4258-12

December 1988
Edition 1.0

CMOS 262,144 x 4 BIT Static Column Mode Dynamic RAM

The Fujitsu MB81C4258 is a fully decoded CMOS Dynamic RAM (DRAM) that contains 1,048,576 memory cells accessible in 4-bit increments. The MB81C4258 features a "static column" mode of operation whereby high-speed random access of up to 512-bits of data within the same row can be selected. The MB81C4258 DRAM is ideally suited for mainframes, buffers, hand-held computers, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81C4258 is only about one-fifth that of a conventional NMOS DRAM, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81C4258 is fabricated using silicon gate CMOS and Fujitsu's advanced triple-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81C4258 are not critical and all inputs are TTL compatible.

DIP-20P-M03

DIP-20C-A03

LCC-26P-M01

ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C4258-85	MB81C4258-10	MB81C4258-12
Row Access Time	85 ns max	100 ns max	120 ns max
Random Cycle Time	160 ns min	180 ns min	210 ns min
Column Address Time	50 ns max	50 ns max	60 ns max
Column Access Time	25 ns max	30 ns max	35 ns max
Static Column Mode Cycle Time	55 ns min	55 ns min	65 ns min
Low Power Dissipation • Operating Current	358 mW max	330 mW max	275 mW max
• Standby Current	11 mW max (TTL level)/5.5 mW max (CMOS level)		

- 262,144 words x 4 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Static column Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

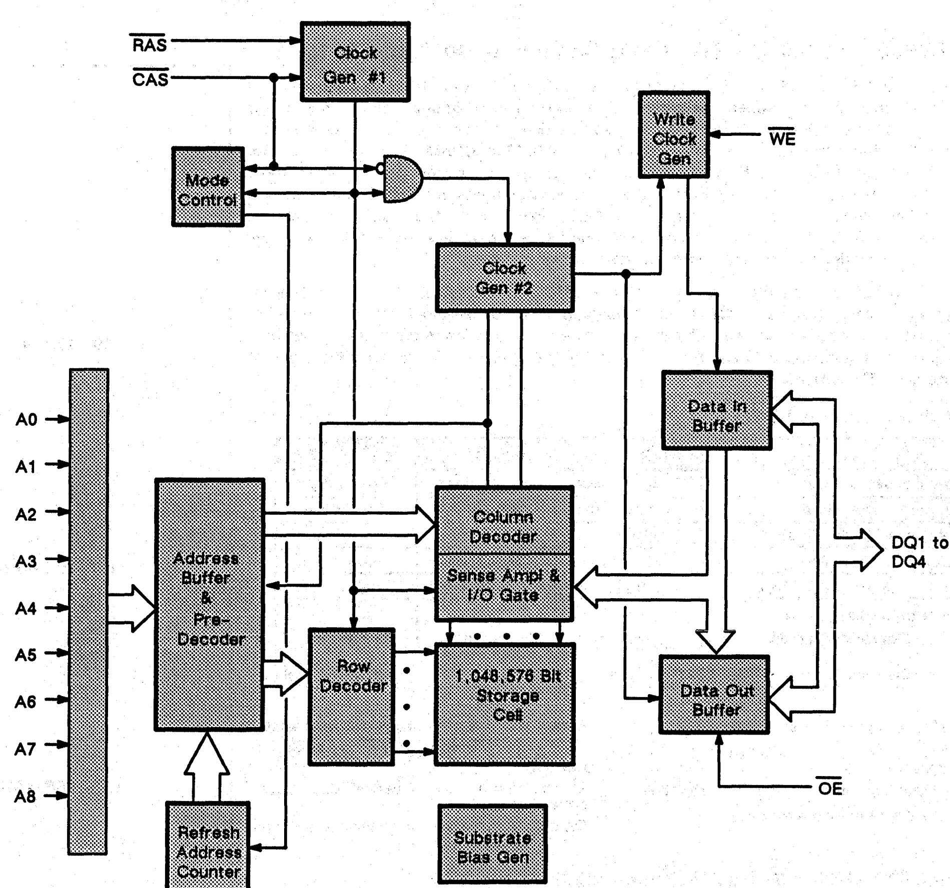
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		--	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB81C4258 DYNAMIC RAM—BLOCK DIAGRAM

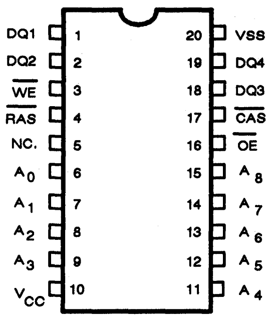


CAPACITANCE (TA = 25°C, f = 1 MHz)

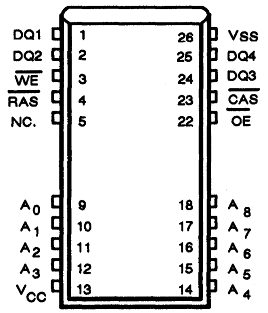
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 To A8	C_{IN1}	—	5	pF
Input Capacitance, RAS, CAS, WE, OE	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 To DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

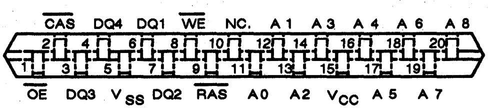
18-Pin DIP:
(TOP VIEW)



26-Pin SOJ:
(TOP VIEW)



20-Pin ZIP:
(TOP VIEW)



Designator	Function
DQ	Data Input.
WE	Write Enable.
RAS	Row address strobe.
NC	No connection.
A0 to A8	Address Inputs.
VCC	+5 volt power supply.
OE	Output enable.
CAS	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

(All voltages referenced to ground; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	
Input High Voltage, All Inputs	VIH	2.4	—	6.5	V
Input Low Voltage, All Inputs	VIL	-2.0	—	0.8	V
Input Low Voltage, DQ	VILD (Note)	-1.0	—	0.8	V

Note: Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0-through-A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH}(min) + t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.
- t_{CAC}: from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}(max).
- t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max).
- t_{OEA}: from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

STATIC COLUMN MODE OF OPERATION

The static column mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static column mode, $\overline{RAS}$ can be kept low throughout static column mode operation. The following four cycles are allowed in the static column mode.

2

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Output High Voltage		V_{OH}	I_{OH} = -5 mA	2.4	—	—	V
Output Low Voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input Leakage Current (Any Input)		$I_{I(L)}$	0 V ≤ V_{IN} ≤ 5.5 V; 4.5 V ≤ V_{CC} ≤ 5.5 V; V_{SS} = 0 V; All other pins not under test = 0V	-10	—	10	µA
Output Leakage Current		$I_{DQ(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V; Data out disabled	-10	—	10	µA
Operating Current (Average Power Supply Current)	MB81C4258-85	I_{CC1} (Note)	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	65	mA
	MB81C4258-10					60	
	MB81C4258-12					50	
Standby Current (Power Supply Current)	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} -0.2 V			1.0	
Refresh Current #1 (Average Power Supply Current)	MB81C4258-85	I_{CC3} (Note)	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	60	mA
	MB81C4258-10					55	
	MB81C4258-12					45	
Static Column Mode Current	MB81C4258-85	I_{CC4} (Note)	$\overline{RAS}$ = $\overline{CAS}$ = V_{IL}; t_{SC} = min	—	—	30	mA
	MB81C4258-10					30	
	MB81C4258-12					23	
Refresh Current #2 (Average Power Supply Current)	MB81C4258-85	I_{CC5} (Note)	$\overline{RAS}$ cycling $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	60	mA
	MB81C4258-10					55	
	MB81C4258-12					45	

Note: I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
I_{CC} depends on the input low voltage level V_{IL}, V_{IL}>-0.5V.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) * Notes 1, 2, 3

No.	Parameter	Symbol	MB81C4258-85		MB81C4258-10		MB81C4258-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	Time Between Refresh	t_{REF}	—	8.2	—	8.2	—	8.2	ms	—
2	Random Read/Write Cycle Time	t_{RC}	160	—	180	—	210	—	ns	—
3	Read-Modify-Write Cycle Time	t_{RWC}	220	—	240	—	275	—	ns	—
4	Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	4,7
5	Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	30	—	35	ns	7
6	Column Address Access Time	t_{AA}	—	50	—	50	—	60	ns	6,7
7	Output Hold Time	t_{OH}	7	—	7	—	7	—	ns	—
8	Output Buffer Turn on Delay Time	t_{ON}	5	—	5	—	5	—	ns	—
9	Output Buffer Turn off Delay Time	t_{OFF}	—	25	—	25	—	25	ns	8
10	Transition Time	t_T	3	50	3	50	3	50	ns	—
11	$\overline{RAS}$ Precharge Time	t_{RP}	65	—	70	—	80	—	ns	—
12	$\overline{RAS}$ Pulse Width	t_{RAS}	85	100000	100	100000	120	100000	ns	—
13	$\overline{RAS}$ Hold Time	t_{RSH}	25	—	30	—	35	—	ns	—
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0	—	0	—	0	—	ns	—
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	60	25	70	25	85	ns	9,10
16	$\overline{CAS}$ Pulse Width	t_{CAS}	25	—	40	—	45	—	ns	—
17	$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	—
18	$\overline{CAS}$ Precharge Time (C-B-R cycle)	t_{CPN}	15	—	15	—	15	—	ns	21
19	Row Address Set Up Time	t_{ASR}	0	—	0	—	0	—	ns	—
20	Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	—
21	Column Address Set Up Time	t_{ASC}	0	—	0	—	0	—	ns	5
22	Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	—
23	$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	35	20	50	20	60	ns	11
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	50	—	60	—	ns	—
25	Read Command Set Up Time	t_{RCS}	0	—	0	—	0	—	ns	—
26	Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	12
27	Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	12
28	Write Command Hold Time	t_{WCH}	20	—	20	—	25	—	ns	—
29	$\overline{WE}$ Pulse Width	t_{WP}	15	—	15	—	20	—	ns	—
30	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	—
31	Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	—
32	DIN Set Up Time	t_{DS}	0	—	0	—	0	—	ns	—
33	DIN Hold Time	t_{DH}	20	—	20	—	25	—	ns	—

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) * Notes 1, 2, 3

No.	Parameter	Symbol	MB81C4258-85		MB81C4258-10		MB81C4258-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
34	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycle)	t_{RPC}	0	—	0	—	0	—	ns	—
35	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CSR}	0	—	0	—	0	—	ns	—
36	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	15	—	15	—	20	—	ns	—
37	Access Time from $\overline{OE}$	t_{OEA}	—	22	—	25	—	30	ns	7
38	Output Buffer Turn off Dealy from $\overline{OE}$	t_{OEZ}	—	25	—	25	—	25	ns	8
39	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data	t_{OEL}	10	—	10	—	10	—	ns	—
40	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	0	—	0	—	0	—	ns	13
41	$\overline{OE}$ to Data In Delay Time	t_{OED}	25	—	25	—	25	—	ns	—
42	DIN to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	14
43	DIN to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	14
44	Access Time from $\overline{CAS}$ (Counter Test Cycle)	t_{CAT}	—	50	—	50	—	60	ns	—
50	Static Column Mode Read/Write Cycle Time	t_{SC}	55	—	55	—	65	—	ns	—
51	Static Column Mode Read-Modify-Write Cycle Time	t_{SRWC}	120	—	120	—	145	—	ns	—
52	Access Time Relative to Last Write	t_{ALW}	—	90	—	90	—	110	ns	15
53	Access Time from $\overline{WE}$ Precharge	t_{WPA}	—	30	—	30	—	35	ns	—
54	Output Hold Time for Column Address Change	t_{AOH}	10	—	10	—	10	—	ns	—
55	Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time	t_{AHR}	15	—	15	—	15	—	ns	16
56	Last Write to Column Address Delay Time	t_{LWAD}	25	40	25	40	30	50	ns	17, 18
57	Column Address Hold Time Referenced to Last Write	t_{AHLW}	83	—	95	—	120	—	ns	—
58	$\overline{RAS}$ to Second Write Delay Time	t_{RSWD}	85	—	100	—	120	—	ns	—
59	$\overline{WE}$ Inactive Time	t_{WI}	15	—	15	—	20	—	ns	—
60	Write Set Up Time for Output Disable	t_{WS}	0	—	0	—	0	—	ns	19
61	Write Hold Time for Output Disable	t_{WH}	0	—	0	—	0	—	ns	19
62	$\overline{OE}$ Hold Time Referenced to $\overline{RAS}$	t_{OEHR}	20	—	20	—	20	—	ns	20
63	$\overline{OE}$ Hold Time Referenced to $\overline{CAS}$	t_{OEHC}	20	—	20	—	20	—	ns	20

2

Notes:

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5 ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Figs. 2 and 3.
5. Assumes that write cycle only.
6. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} and t_{OEZ} are specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is co ntrolled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min)
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. Assumes that $t_{WS} \leq t_{WS}$ (min)
14. Either t_{DZC} or t_{DZO} must be satisfied.
15. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
16. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
17. Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
18. t_{LWAD} (min) = t_{CAH} (min)+ t_T(t_T − 5 ns).
19. t_{WS} and t_{WH} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High-Z state through entire cycle.
20. Either t_{OEHR} or t_{OEHC} is satisfied.
21. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.$\overline{CAS}$-before $\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

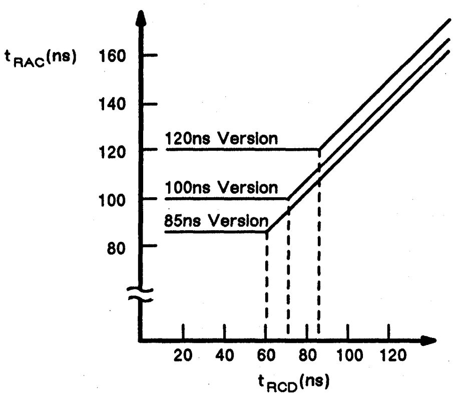
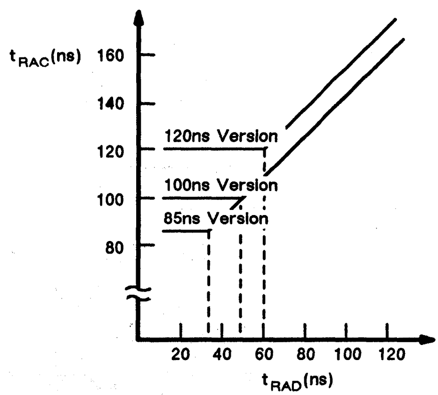


Fig. 3 – t_{RAC} vs. t_{RAD}



FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	O	$t_{RCS} \geq t_{RCS}(min)$ $t_{RCH} \geq t_{RCH}(min)$
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	*1 High-Z	O	$t_{WS} \geq t_{WS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	O	
Static Column Mode Read Cycle	L	L	H	L	*2 Valid	Valid	—	Valid	X	$t_{RCS} \geq t_{RCS}(min)$ $t_{RCH} \geq t_{RCH}(min)$
Static Column Mode Write Cycle	L	L	L	H	*2 Valid	Valid	Valid	*1 High-Z	X	
Static Column Mode Read-Modify-Write Cycle	L	L	H→L	L→H	*2 Valid	Valid	Valid	Valid	X	
Static Column Mode Mixed Cycle	L	L	L/H	L/H	*2 Valid	Valid	Valid	High-Z or Valid	X	
$\overline{RAS}$-only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	O	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High-Z	O	
Hidden Refresh Cycle	H→L	L	X	L	—	—	—	Valid	O	Previous data is kept

Notes:

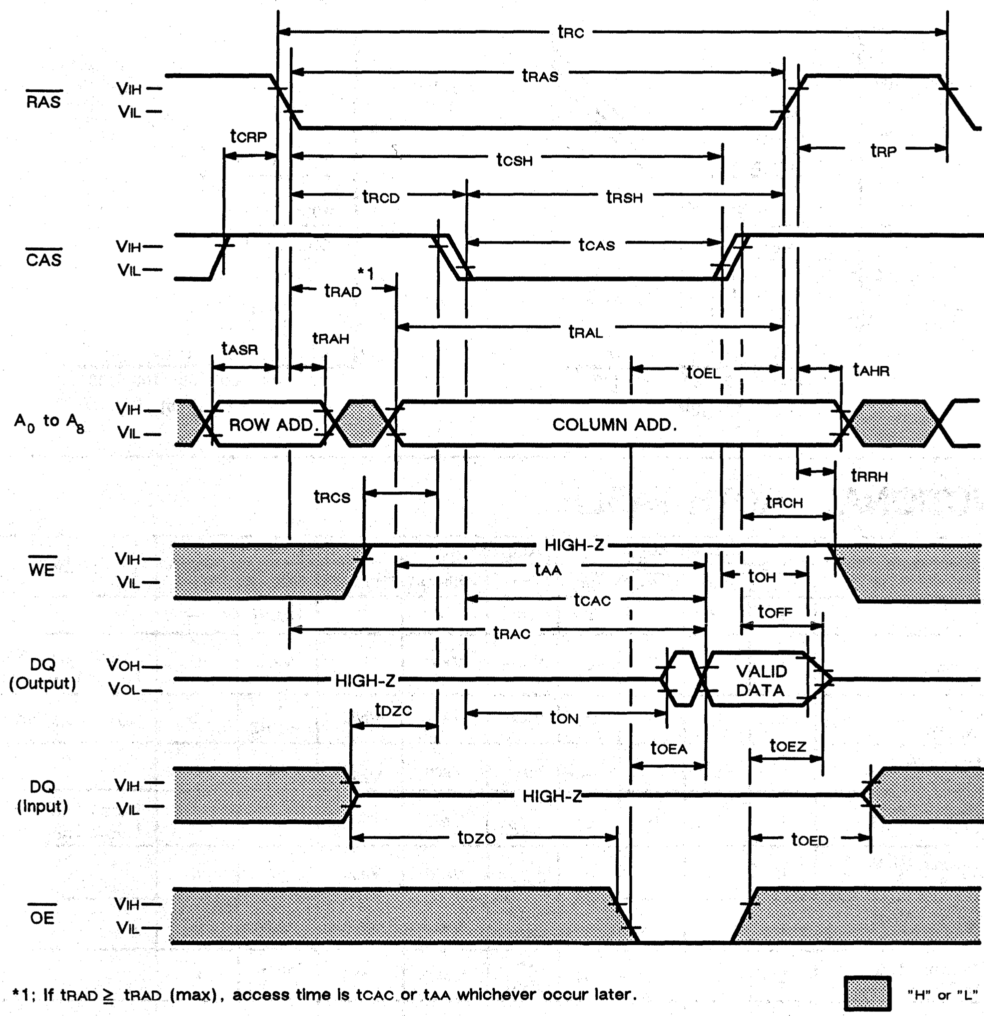
X : "H" or "L"

*1: If tWS < tWS (min) and tWH < tWH (min), the data output become invalid.

*2: After first cycle, row address is not necessary.

2

Fig. 4 – READ CYCLE



*1: If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occur later.

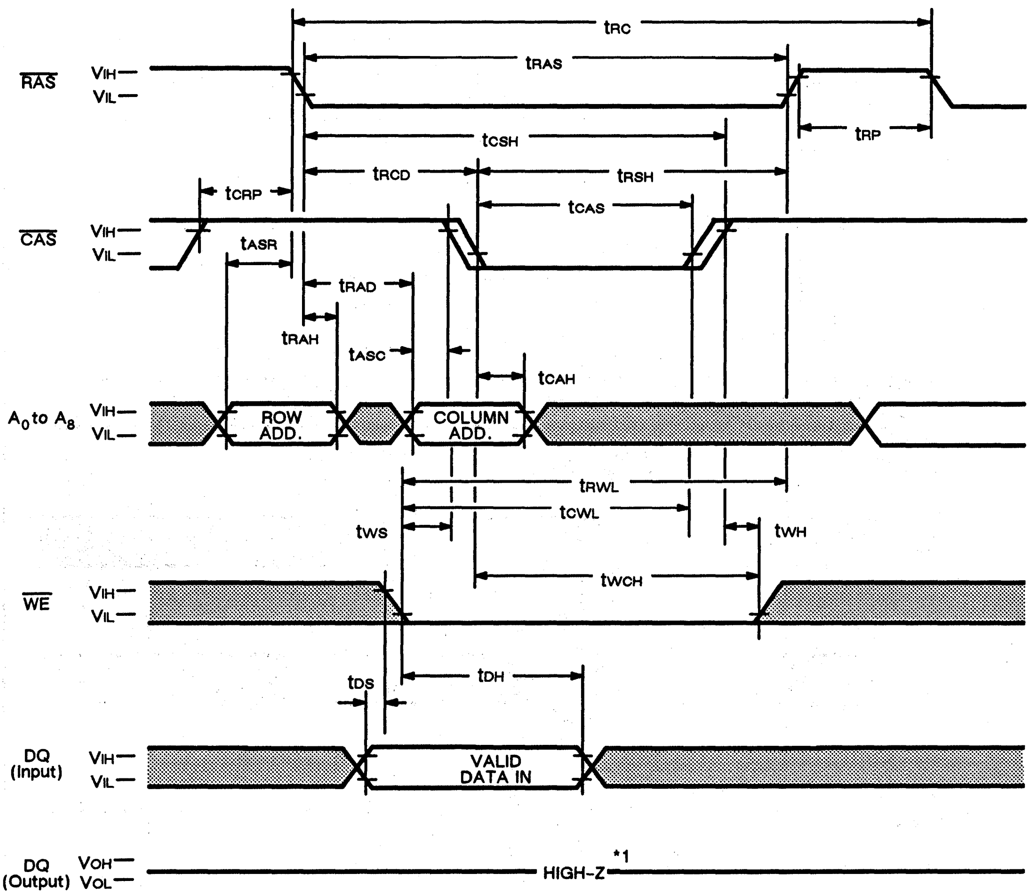
DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and, with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), $\overline{OE}$, (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

- If $t_{RCD} > t_{RCD}$ (max), access time = t_{CAC}.
- If $t_{RAD} > t_{RAD}$ (max), access time = t_{AA}.
- If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (which ever occurs later), access time = t_{OEA}.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

Fig. 5 - EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



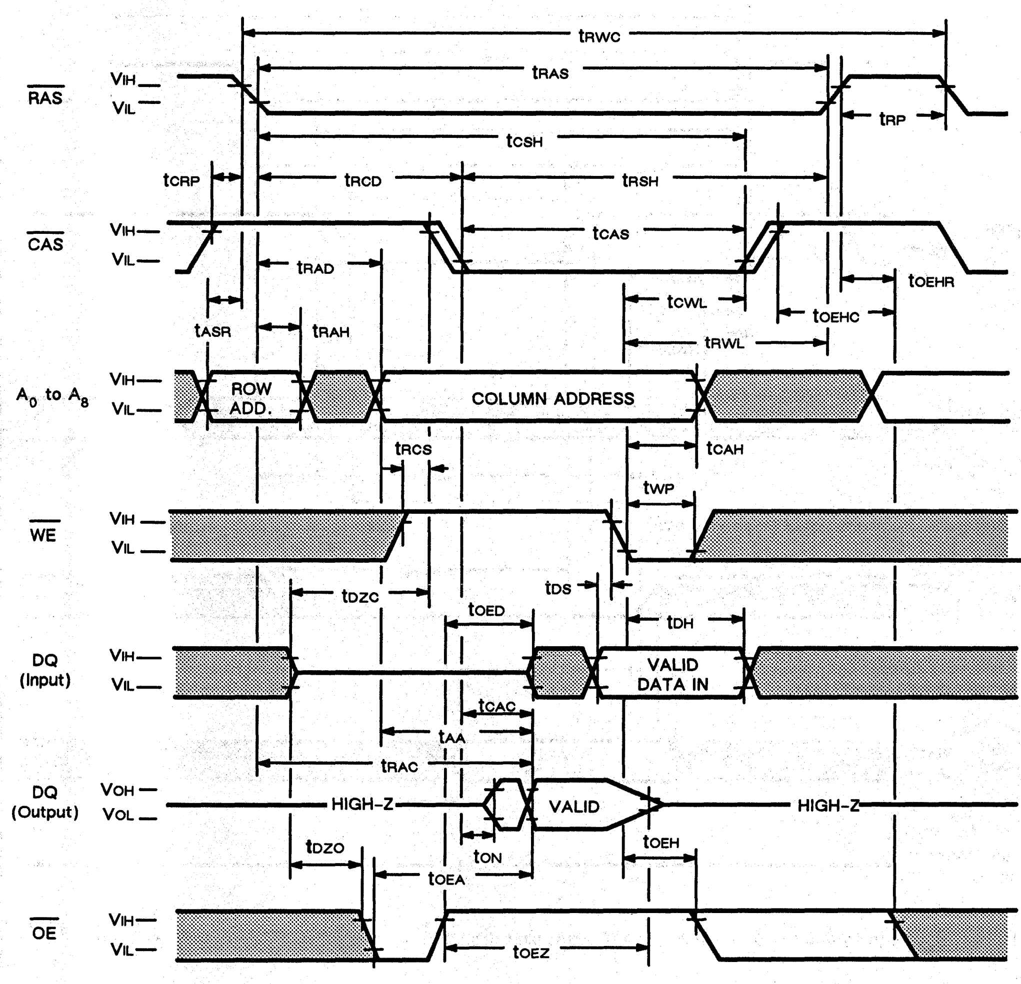
*1; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), DQ (Output) pin is high-Z.

DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways—early write, $\overline{OE}$ write (delayed write), or read-modify-write. During all write cycles, timing parameters t_{RWL}, t_{CWL} and t_{RAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins is latched with the falling edge of $\overline{CAS}$ and written into memory.

2

Fig. 6 – READ-MODIFY-WRITE-CYCLE

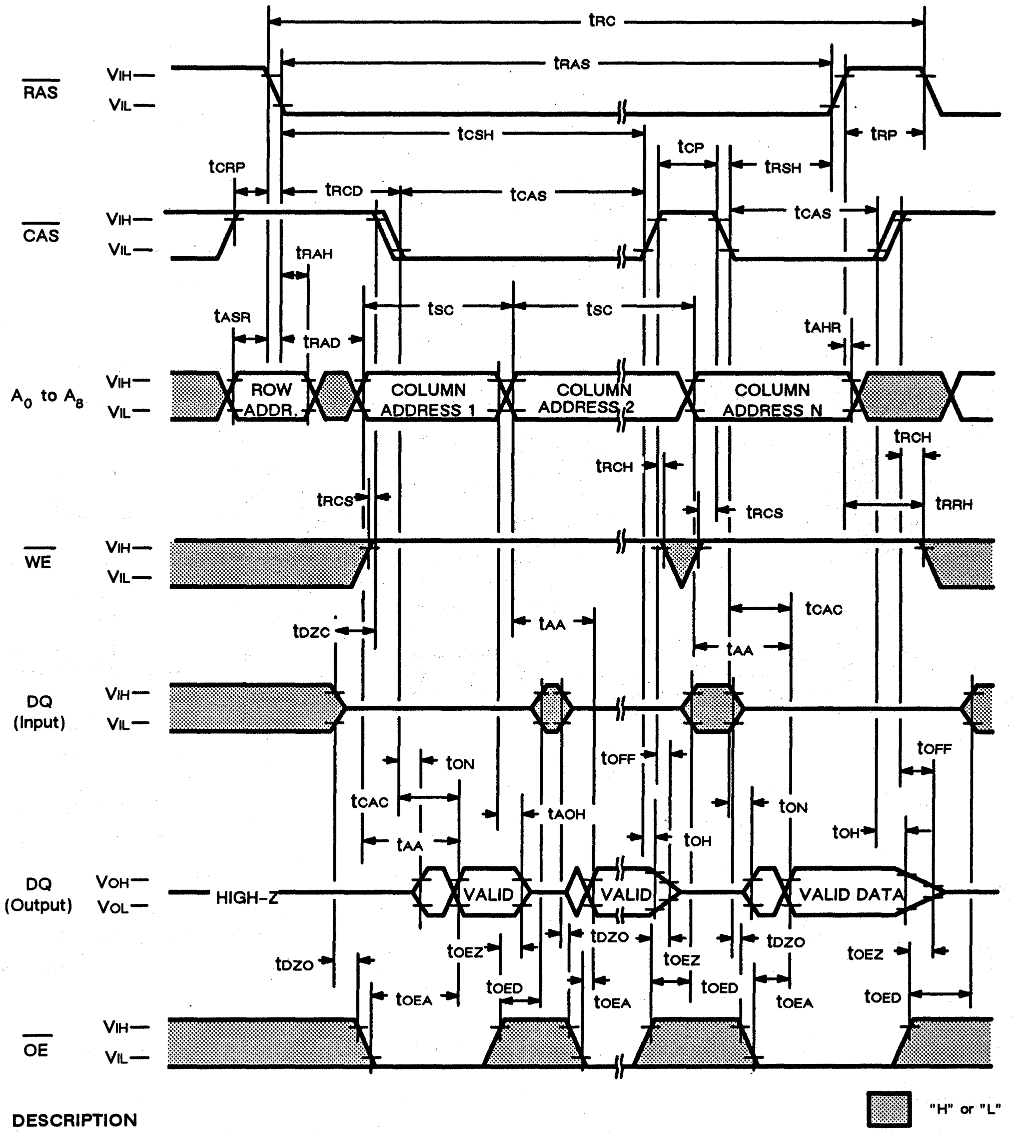


"H" or "L"

DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 7 – STATIC COLUMN MODE READ CYCLE

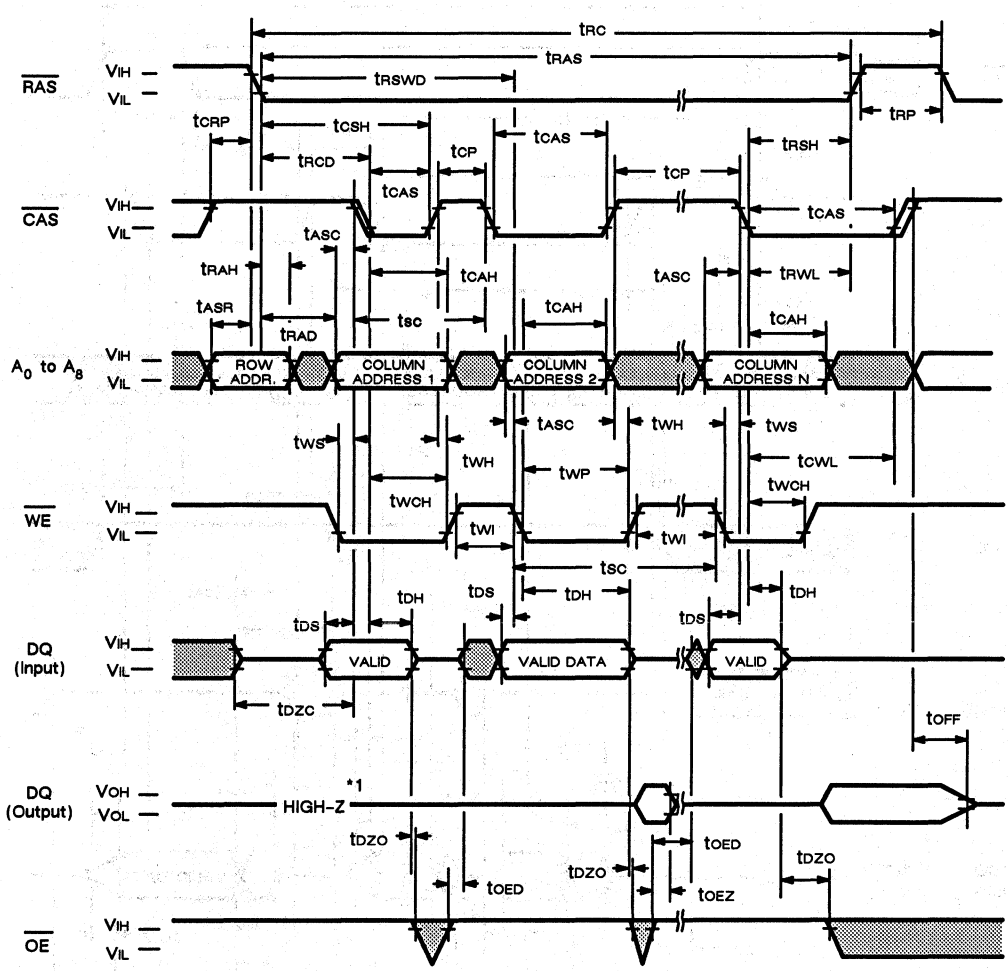


DESCRIPTION

In a static column mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input or t_{OEA} from the falling edge of $\overline{OE}$. The data remains valid for a time t_{AOH} after the column address is changed.

2

Fig. 8 – STATIC COLUMN MODE WRITE CYCLE ($\overline{OE}$ = "H " or "L")

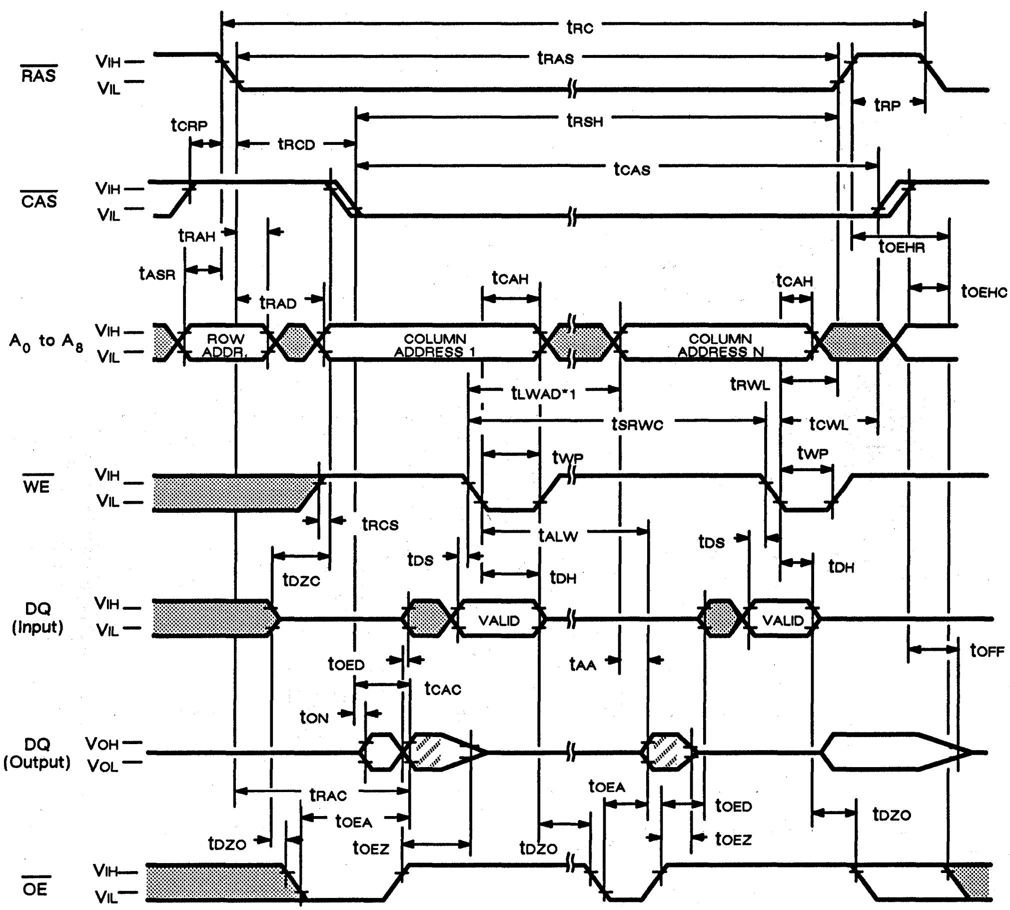


*1; If tWS ≥ tWS (min) and tWH ≥ tWH (min), DQ (Output) pin is high-Z.

DESCRIPTION

In a static column mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both tWS and tWH are greater than their minimum limits, the data output pin is kept high impedance state through the static column mode write cycle. The OE must be high before the data are applied to DQ pins.

Fig. 9 – STATIC COLUMN MODE READ–MODIFY–WRITE CYCLE



*1; If tLWAD (min) ≦ tLWAD ≦ tLWAD (max), tALW = tSC (min) + tAA (max).

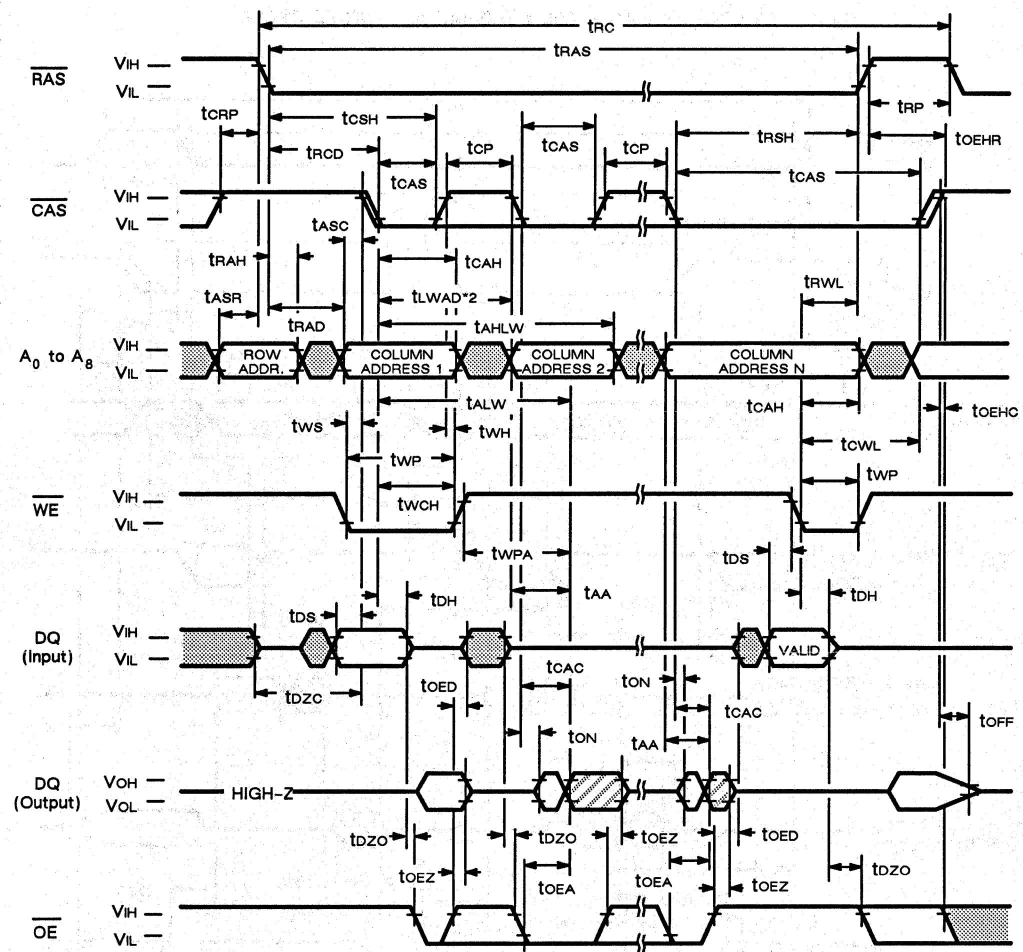
"H" or "L"

Valid Data

DESCRIPTION

In the static column mode read-modify-write cycle, $\overline{WE}$ goes low after tAWD from the column address inputs and tCWD from the falling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge of $\overline{WE}$. The $\overline{OE}$ must be high before the data are applied to DQ pins.

Fig. 10 - STATIC COLUMN MODE MIXED CYCLE *1



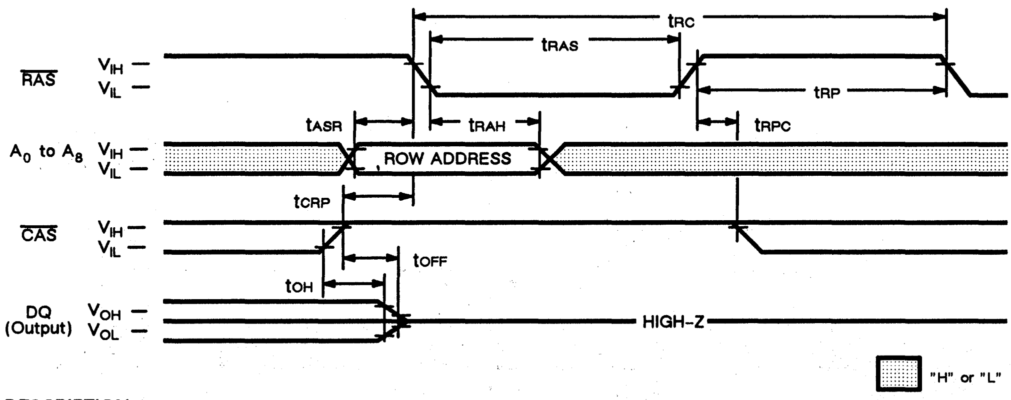
*1; This is an example of static column mode mixed cycle.
*2; If tLWAD is satisfied its min/max value, tALW = tSC (min) + tAA (max)

DESCRIPTION

In the static column mode, read, write, and read-modify-write cycles can be mixed in any order.
In the next read cycle of static column mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.

1. tALW from the falling edge of $\overline{WE}$ or $\overline{CAS}$ at previous write cycle.
2. tAA from the column address inputs.
3. tWPA from the rising edge of $\overline{WE}$ at the read cycle.
4. tCAC from the falling edge of $\overline{CAS}$
5. tOEA from the falling edge of $\overline{OE}$

Fig. 11 – $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

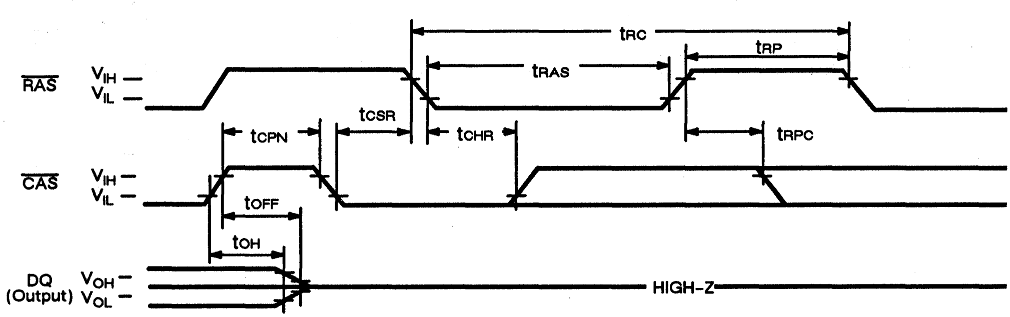


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available; $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

Fig. 12 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (A0 to A9 = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

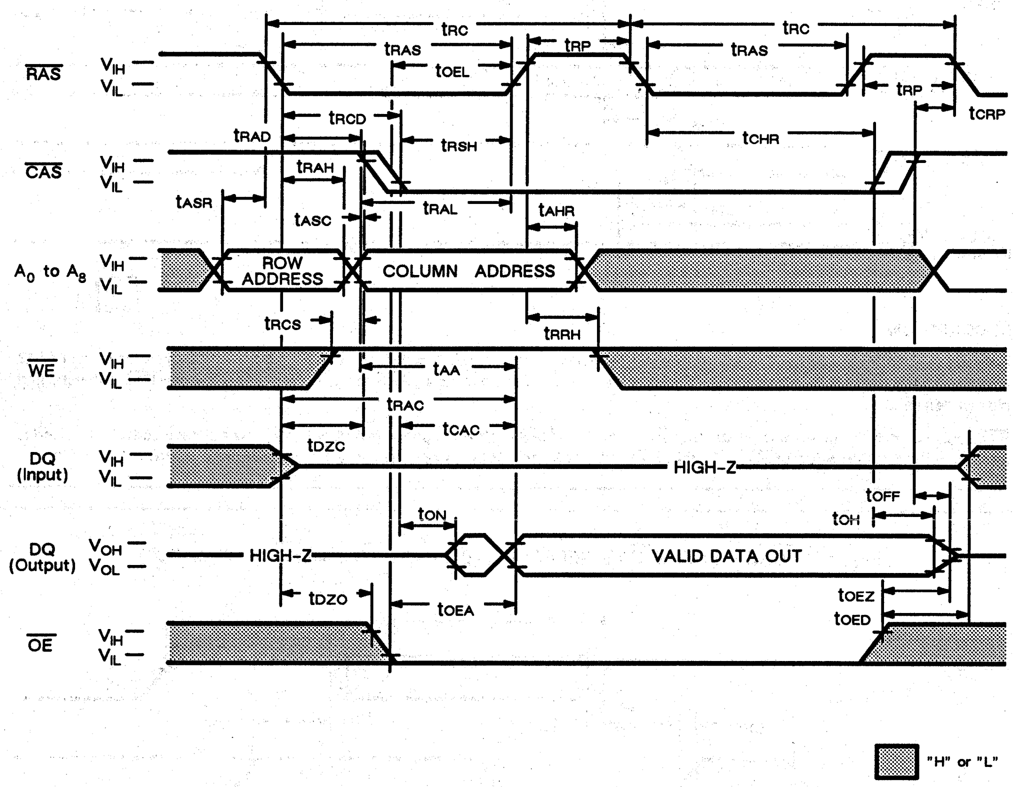


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

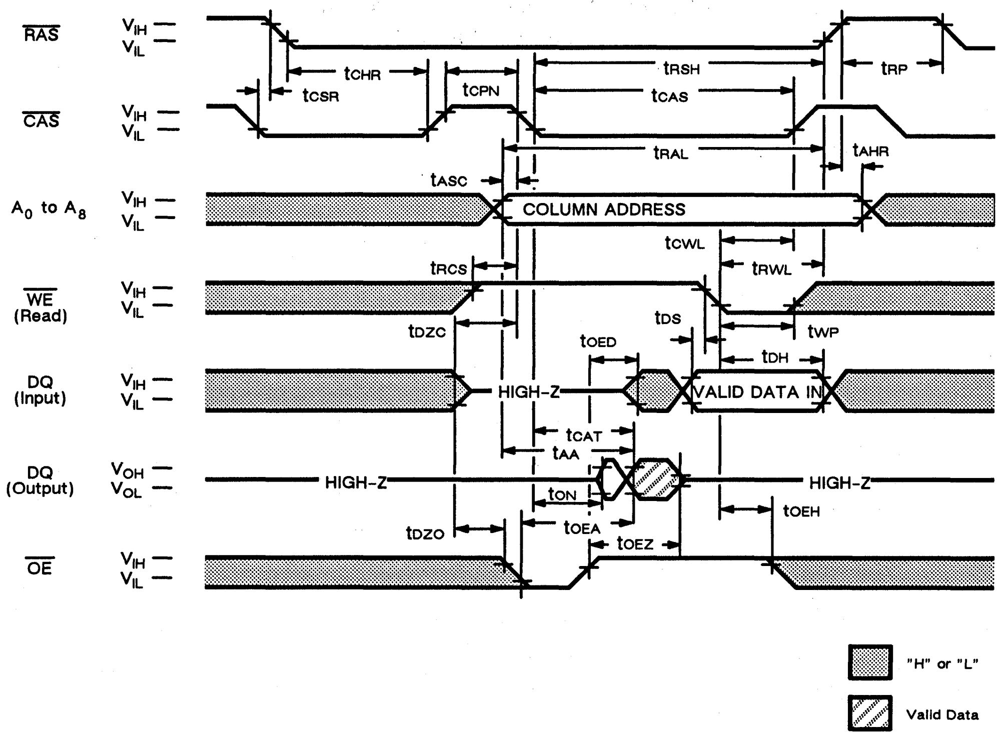
Fig. 13 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 14 – $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh circuitry. If, after a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle. $\overline{\text{CAS}}$ makes a transition from High to Low while $\overline{\text{RAS}}$ is held Low, read and write operations are enabled as shown above, Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{\text{CAS}}$.

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Cycle is designed for use with the following procedures:

1) Initialize the internal refresh address counter by using eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.
4) Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read-write cycles. Repeat this procedure 5.2 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3, 4, and 5.

2

PACKAGE DIMENSIONS

(Suffix : -P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M03)

PACKAGE DIMENSIONS (Continued)

(Suffix : –C)

20–LEAD CERAMIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20C–A03)

2

PACKAGE DIMENSIONS (Continued)

(Suffix : -PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER (SOJ-26)
(CASE No.: LCC-26P-M01)

PACKAGE DIMENSIONS (Continued)

(Suffix : -PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)

2

FUJITSU

CMOS 1,048,576 BIT SERIAL ACCESS DYNAMIC RAM

MB81C4259-85 MB81C4259-10 MB81C4259-12

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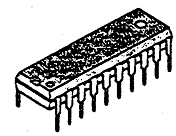
CMOS 262,144 X 4 BIT Serial Access DYNAMIC RAM

TS026-C886
June 1988

The Fujitsu MB81C4259 is a fully decoded CMOS Dynamic RAM (DRAM) that contains 1,048,576 memory cells accessible in 4-bit increments. The MB81C4259 features a serial access mode of operation whereby the user can serially access up to 1024 bits of data at very high speed. The MB81C4259 DRAM is ideally suited for mainframes, buffers, hand-held computers, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81C4259 is only about one-fifth that of a conventional NMOS DRAM, the device can be used as a nonvolatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81C4259 is fabricated using silicon gate CMOS and Fujitsu's advanced triple-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81C4259 are not critical and all inputs are TTL compartible.



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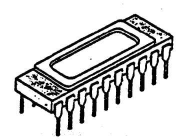

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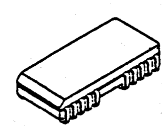

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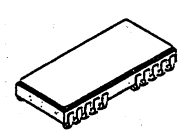

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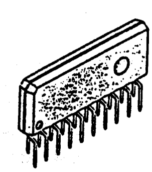


ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C4259-85	MB81C4259-10	MB81C4259-12
Row Access Time	85ns max.	100ns max.	120ns max.
Random Cycle Time	60ns min.	180ns min.	210ns min.
Column Address Time	50ns max.	50ns max.	60ns max.
Column Access Time	25ns max	30ns max.	35ns max.
Serial Access Mode Cycle Time	60ns min.	60ns min.	70ns min.
Low Power Dussipation			
• Operating current	358mA max.	330mA max.	275mA max.
• Standby current	11mW max.(TTL level)/5.5mW max.(CMOS level)		

- On-chip latches for both address and data
- TTL compatible inputs and outputs
- Three-dimensional stacked capacitor memory cells
- 512 refresh cycles every 8.2ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh
- Both early and delayed ($\overline{OE}$) write

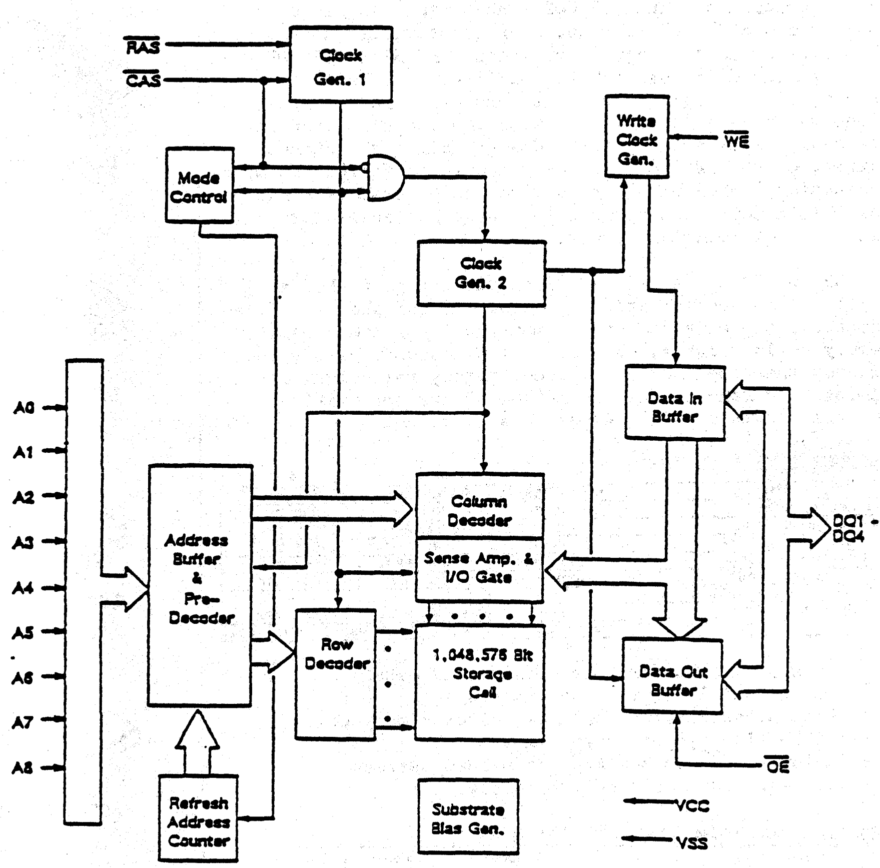
ABSOLUTE MAXIMUM RATINS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} Relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 - MB81C4259 DYNAMIC RAM - BLOCK DIAGRAM



CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}		5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}		5	pF
Input/Output Capacitance, (DQ1~DQ4)	C_{DQ}		6	pF

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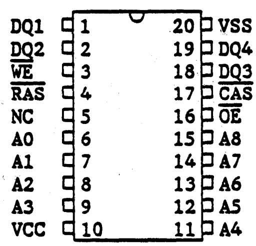
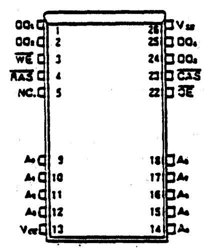
PIN ASSIGNMENTS AND DESCRIPTIONS

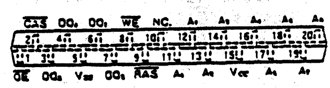
20-Pin DIP:
(TOP VEIW)



26-Pin SOJ:
(TOP VIEW)



20-Pin ZIP:
(TOP VIEW)



Designator		Function
DQ1 ~ DQ2 DQ3 ~ DQ4	:	When WE is Low, DQ1~DQ4 serve as data inputs; when WE is High, these pins provide output data.
WE	:	When active Low, the write mode is enabled, when High, the read mode is enabled.
RAS	:	Row address strobe.
NC	:	No connection.
A0 ~ A3 A4 ~ A8	:	Address inputs.
VCC	:	+5 volt power supply.
OE	:	When active Low, enables output pins DQ1~DQ4
CAS	:	Column address strobe.
VSS	:	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Volate	VCC	4.5	5.0	5.5	V	0°C to +70°C
	VSS	0	0	0		
Input High Voltage, all inputs	VIH	2.4		6.5	V	
Input Low Voltage, all inputs	VIL	-2.0		0.8	V	
Input Low Voltage, DQ	VILD*	-1.0	-	0.8	V	

* The device will withstand undershoots to the -2.0 level with a maximum pulse width of 20 ns at the -1.5 V level.

FUNCTIONAL OPERATION

Address Inputs;

Eighteen binary input address bits are required to select any 4 of 262,144 cell locations within the MB81C4259. Nine row address bits are placed onto the input pins(A0 to A8) and latched with the Row Address Strobe ($\overline{RAS}$) signal. Nine column address bits are then placed onto the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the address latch is flow through latch, address information at address pins are automatically latched as column address after tRAH(min)+tT. If tRAD ≥ tRAD(min) access time is t_{CAC} or t_{AA} whichever occur later.

Write Enable:

The read or write mode is determined by the $\overline{WE}$ input. If $\overline{WE}$=high, a read cycle is selected. If $\overline{WE}$=low, a write mode is selected. Data input is ignored during read mode.

Data Input:

Data are written to the MB81C4259 during a write (early write or $\overline{OE}$ write) or read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, is a strobe for the input data latch. In an early write cycle, data on DQ pins are strobed by $\overline{CAS}$, and the setup and hold times are referenced to $\overline{CAS}$ due to the $\overline{WE}$ is set low before $\overline{CAS}$. In a delayed write or read-write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus data on DQ pins are strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.
As MB81C4259 has I/O common pins, so in case of delayed write and read-modify-write, input/output data should be controlled by $\overline{OE}$.

Data Output:

The output buffers are three-state TTL-compatible with a fan-out of two standard TTL loads. Data Out are the same polarity as Data In. The outputs are in high impedance state until $\overline{CAS}$ goes low. In a read or read-write cycle, the outputs become valid after;

1) t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD}(max) is satisfied
2) t_{CAC} from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}(max)
3) tAA from column address input when tRAD is greater than tRAD(max).
4) tOEA from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought "L" after tRAC, tCAC, or tAA.

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to "H". In an early write cycle, the output buffers are in high impedance state during the entire cycle.

FUNCTIONAL OPERATION

Serial Access Mode of Operation:

In the serial access mode of operation, the user can serially access (2 ~ 512) x 4 bits of data and perform high-speed read, write, or read-modify-write operations. During the serial access mode, the bits of data that may be accessed are determined by nine bits of row addresses. For initial access, address bits CA0 to CA8 are used to select one of 512 serial access bits. After the first bit are accessed by this method, all remaining bits are accessed by simply toggling the column address strobe ($\overline{CAS}$) from High to Low. Each High-to-Low transition of $\overline{CAS}$ internally increments CA0 to CA8 and provides access to the next serial access bit. If more than 512 bits are accessed during the serail access mode, the address sequence shown in table 1 will repeat.

Table 1 - SERIAL ACCESS MODE ADDRESS SEQUENCE

Sequence	Serial Access Bit	Row Add. (RA8~RA0)	Col. Add. (CA8~CA0)	Remarks
$\overline{RAS}$/$\overline{CAS}$ (Normal mode)	1	101010101	000000000	Input address
Toggle $\overline{CAS}$ (Serial Access mode)	2	101010101	000000001	Internally generated address
Toggle $\overline{CAS}$ (Serial Access mode)	3	101010101	000000010	Internally generated address
• •	• •	• •	• •	• •
Toggle $\overline{CAS}$ (Serial Access mode)	511	101010101	111111110	Internally generated address
Toggle $\overline{CAS}$ (Serial Access mode)	512	101010101	111111111	Internally generated address
Toggle $\overline{CAS}$ (Serial Access mode)	1	101010101	000000000	Sequence repeats

DC CHARACTERISTICS

(Recommendec operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average power supply current (RAS, CAS cycling;tRC=min)	MB81C4259-85	ICC1			65	mA
	MB81C4259-10				60	
	MB81C4259-12				50	
STANDBY CURRENT Power supply current	TTL level RAS=CAS=VIH	ICC2			2.0	mA
	CMOS level RAS=CAS≥VCC-0.2V				1.0	
REFRESH CURRENT 1* Average power supply current (CAS =VIH RAS cycling;tRC=min)	MB81C4259-85	ICC3			60	mA
	MB81C4259-10				55	
	MB81C4259-12				45	
SERIAL ACCESS MODE CURRENT* (RAS = V_{IL}, CAS = cycling; tSA= min)	MB81C4259-85	ICC4			40	mA
	MB81C4259-10				40	
	MB81C4259-12				33	
REFRESH CURRENT 2* Average power supply current (CAS-before-RAS; tRC = min)	MB81C4259-85	ICC5			60	mA
	MB81C4259-10				55	
	MB81C4259-12				45	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V≤VIN ≤5.5 V, 4.5V≤VCC≤5.5V, VSS=0V, all other pins not under test=0V)		$I_{I(L)}$	-10		10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤VOUT≤5.5V)		IDQ(L)	-10		10	µA
OUTPUT LEVELS Output high voltage (I_{OH} =-5mA)		VOH	2.4			V
Output low voltage(IOL=4.2mA)		VOL			0.4	V

*: ICC depends on the output load conditions, input levels, and cycle rate.
The specified values are obtained with the output open.
ICC also depends in input low voltage level, VILD, VILD≥-0.5V.

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AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB81C4259-85		MB81C4259-10		MB81C4259-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	Time Between Refresh	tREF		8.2		8.2		8.2	ms	
2	Random Read/Write Cycle Time	tRC	160		180		210		ns	
3	Read-Modify-Write Cycle Time	tRWC	220		240		275		ns	
4	Access Time from RAS	tRAC		85		100		120	ns	4,7
5	Access Time from CAS	tCAC		25		30		35	ns	5,7
6	Access Time from Column Address	tAA		50		50		60	ns	6,7
7	Output Hold Time	tOH	7		7		7		ns	
8	Output Buffer Turn On Delay Time	tON	5		5		5		ns	
9	Output Buffer Turn off Delay Time	tOFF		25		25		25	ns	8
10	Transition Time	tT	3	50	3	50	3	50	ns	
11	RAS Precharge Time	tRP	65		70		80		ns	
12	RAS Pulse Width	tRAS	85	100000	100	100000	120	100000	ns	
13	RAS Hold Time	tRSH	25		30		35		ns	
14	CAS to RAS Precharge Time	tCRP	0		0		0		ns	
15	RAS to CAS Delay Time	tRCD	22	60	25	70	25	85	ns	9,10
16	CAS Pulse Width	tCAS	25		30		35		ns	
17	CAS Hold Time	tCSH	85		100		120		ns	
18	CAS Precharge Time(Normal)	tCPN	15		15		15		ns	17
19	Row Address Set Up Time	tASR	0		0		0		ns	
20	Row Address Hold Time	tRAH	12		15		15		ns	
21	Column Address Set Up Time	tASC	0		0		0		ns	
22	Column Address Hold Time	tCAH	15		15		20		ns	
23	RAS to Column Address Delay Time	tRAD	17	35	20	50	20	60	ns	11
24	Column Address to RAS Lead Time	tRAL	45		50		60		ns	
25	Read Command Set Up Time	tRCS	0		0		0		ns	
26	Read Command Hold Time Referenced to RAS	tRRH	0		0		0		ns	12
27	Read Command Hold Time Referenced to CAS	tRCH	0		0		0		ns	12
28	Write Command Set Up Time	tWCS	0		0		0		ns	15
29	Write Command Hold Time	tWCH	15		15		20		ns	
30	WE Pulse Width	tWP	15		15		20		ns	
31	Write Command to RAS Lead Time	tRWL	25		25		30		ns	
32	Write Command to CAS Lead Time	tCWL	20		20		25		ns	
33	DIN set Up Time	tDS	0		0		0		ns	
34	DIN Hold Time	tDH	15		15		20		ns	
35	RAS precharge Time to CAS Active Time	tRPC	0		0		0		ns	

AC CHARACTERISTICS - Continued -

(At Recommended operating conditions unless otherwise noted) Note 1, 2, 3

No.	Parameter	Symbol	MB81C4259-85		MB81C4259-10		MB81C4259-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
36	CAS Set Up Time for CAS-before-RAS Refresh	tCSR	0		0		0		ns	
37	CAS Hold Time for CAS-before RAS Refresh	tCHR	15		15		20		ns	
38	Access Time from OE	tOEA		22		25		30	ns	7
39	Output Buffer Turn Off Delay from OE	tOEZ		25		25		25	ns	8
40	OE to RAS Lead Time for Valid Data	tOEL	10		10		10		ns	
41	OE Hold Time Referenced to WE	tOEH	0		0		0		ns	13
42	OE to Data In Dealy Time	tOED	25		25		25		ns	
43	DIN to CAS Delay Time	tDZC	0		0		0		ns	14
44	DIN to OE Delay Time	tDZO	0		0		0		ns	14
45	Access Time from CAS (Counter Test Cycle)	tCAT		50		50		60	ns	
50	Serial Access Mode Read/Write Cycle Time	tSA	60		60		70		ns	
51	Serial access Mode Read-Modify-Write Cycle Time	tSARW	115		115		130		ns	
52	Access Time from Serial Access Mode CAS Precharge	tSPA		60		60		70	ns	7,16
53	Serial Access Mode CAS Precharge Time	tSCP	15		15		15		ns	

Notes;

1. An Initial pause(RAS=CAS=VIH) of 200µs is required after power-up followed by any 8 RAS-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
2. AC characteristics assume t_T=5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} (or tRAD) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amout that tRCD exceeds the value shown. Refer to Fig.2 and 3.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$(max). If $t_{ASC} \geq t_{AA}-t_{CAC}-t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$(max) and $t_{ASC} \leq t_{AA}-t_{CAC}-t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max)is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$limit, access time is controlled exclusively by t_{CAC} or tAA.
10. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min)
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only; If t_{RAD} is greater than the specified t_{RAD}(max) limit, access time is controlled exclusively by t_{CAC} or tAA.
12. Either t_{RRH} or t_{RCH} must be satisfed for a read cycle.
13. Assumes that $t_{WCS} < t_{WCS}$(min).
14. Either t_{DZC} or t_{DZO} must be satisfied.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$(min) the data output pin will remain High-Z state through entire cycle.
16. tSPA is access time from the selection of a new column address (that is caused by changing CAS From "L" to "H"). Therefore, if tSCP is long, tSPA is longer than tSPA(max).
17. Assume that CAS-before-RAS Refresh cycle and CAS-before-RAS counter test cycle only.

Fig. 2 – tRAC vs. tRCD

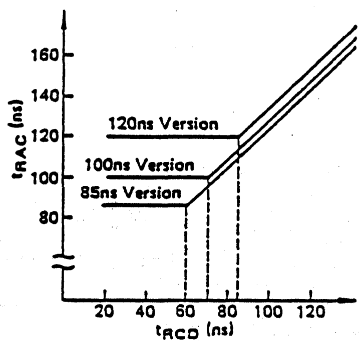
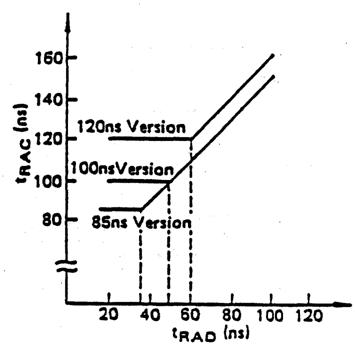


Fig. 3 – tRAC vs. tRAD

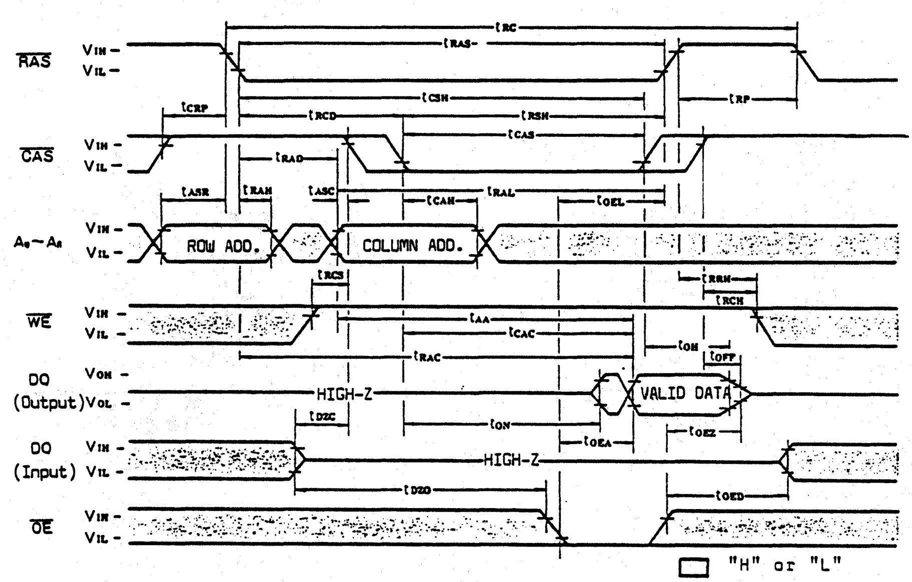


FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	RAS	CAS	WE	OE	Row	Column	Input	Output		
Standby	H	H	X	X	-	-	-	High-Z	-	
Read Cycle	L	L	H	L	Valid	Valid	-	Valid	○ *	tRCS≥tRCS(min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	○ *	tWCS≥tWCS(min)
Read-Modify-Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	○ *	
RAS-only Refresh Cycle	L	H	X	X	Valid	-	-	High-Z	○	
CAS-before-RAS Refresh Cycle	L	L	X	X	-	-	-	High-Z	○	tCSR≥tCSR(min)
Hidden Refresh Cycle	H→L	L	X	L	-	-	-	Valid	○	Previous data is kept.

X; "H" or "L"
*; It is impossible in Nibble Mode

Read Cycle

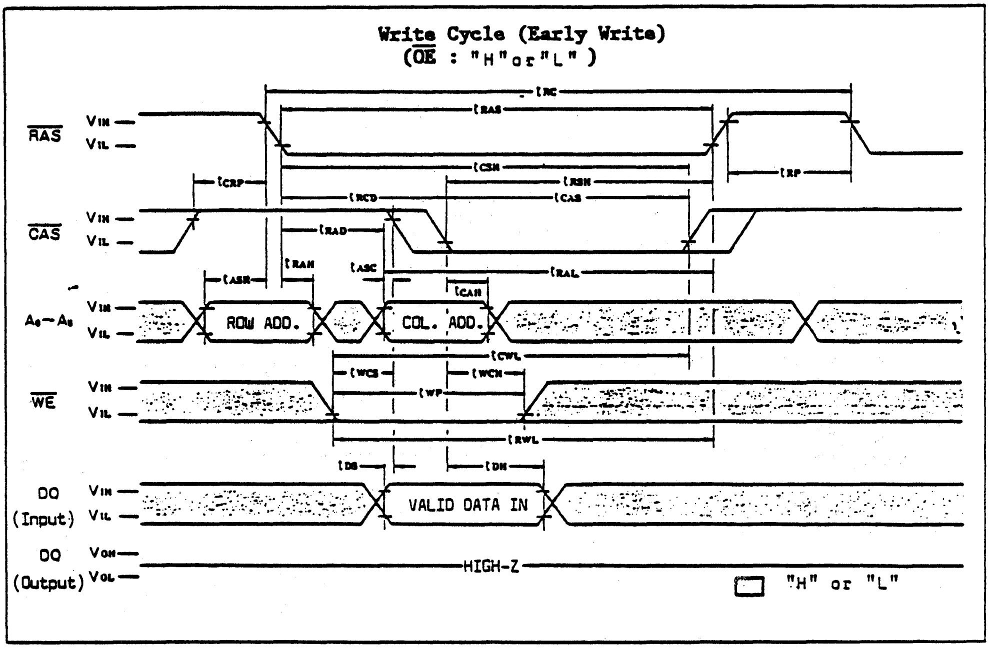


DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and, with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), $\overline{OE}$, (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

- If $t_{RCD} > t_{RCD}$ (max), access time = t_{CAC}.
- If $t_{RAD} > t_{RAD}$ (max), access time = t_{AA}.
- If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (which ever occurs later), access time = t_{OEA}.

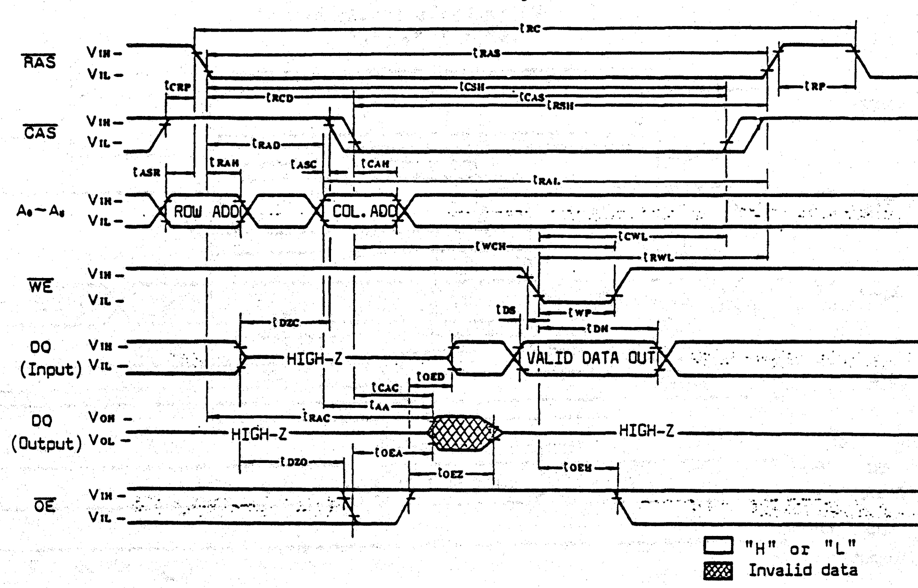
However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H or L" signal. A write cycle can be implemented in either of three ways—early write, $\overline{OE}$ write (delayed write), or read-modify-write. During all write cycles, timing parameters tRWL, tCWL, tRAL, and tCAL must be satisfied. In the early write cycle shown above twcs satisfied, data on the DQ pins is latched with the falling edge of $\overline{CAS}$ and written into memory.

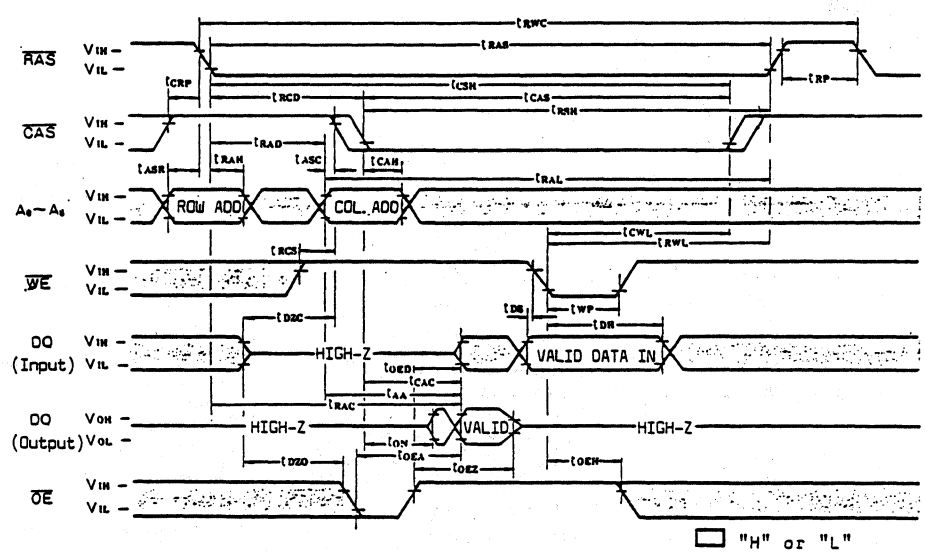
$\overline{OE}$-Write Cycle



DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, twcs is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High befor $\overline{WE}$ goes Low (t_{OED} + t_{DS}).

Read Write/Read-Modify-Write Cycle



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

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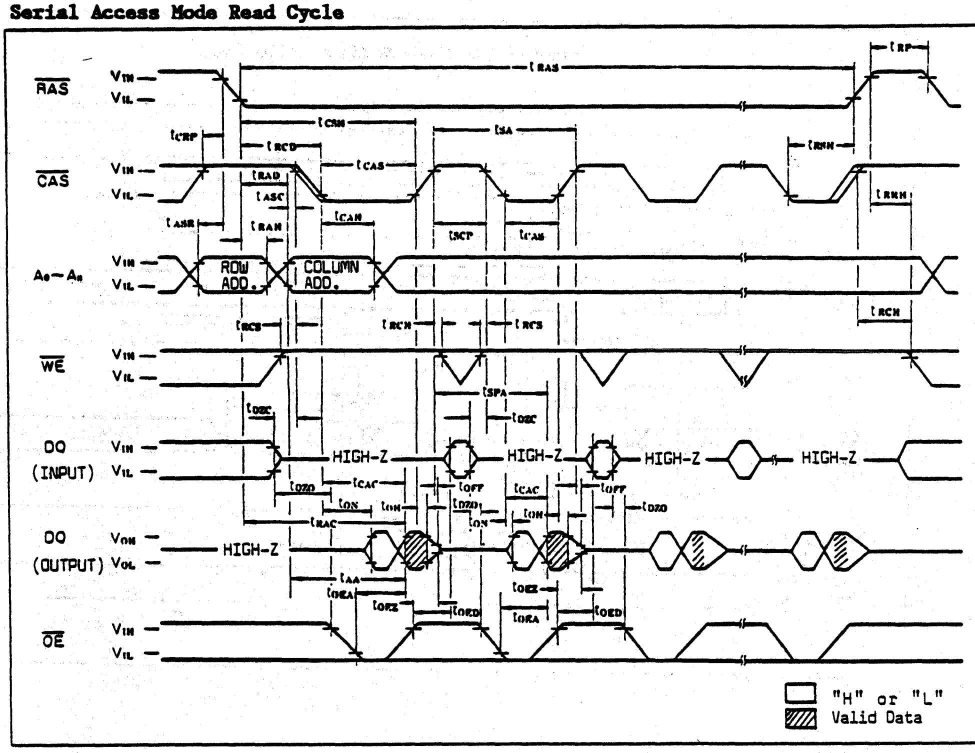
Serial Access Mode Read Cycle

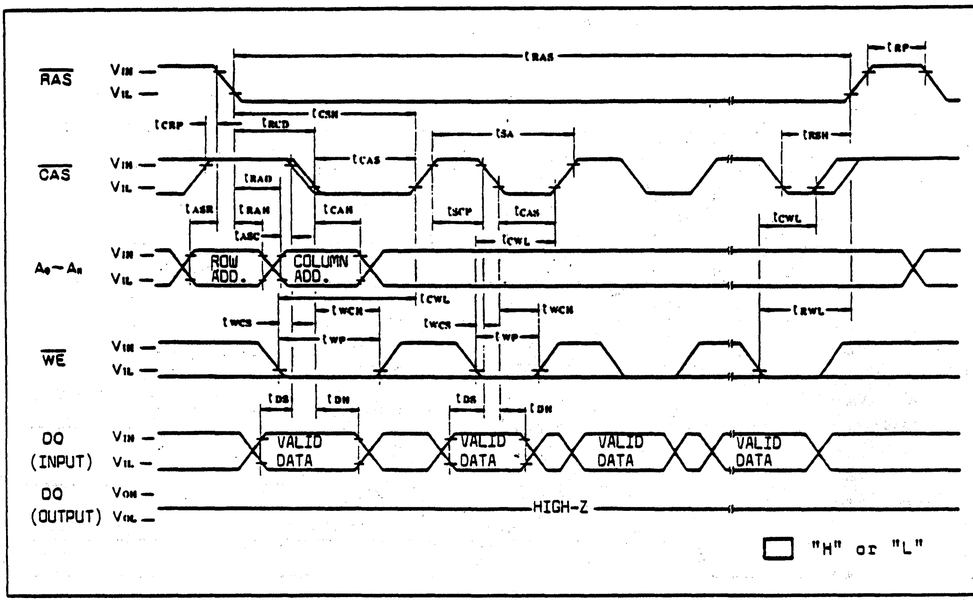


DESCRIPTION

The serial access mode read cycle can be executed after normal cycle with holding $\overline{RAS}$="L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$="H".

Data are not refreshed during serial access mode cycle. Therefore, pay attention that refresh requirment must be kept.

Serial Access Mode Write Cycle (Early-Write)



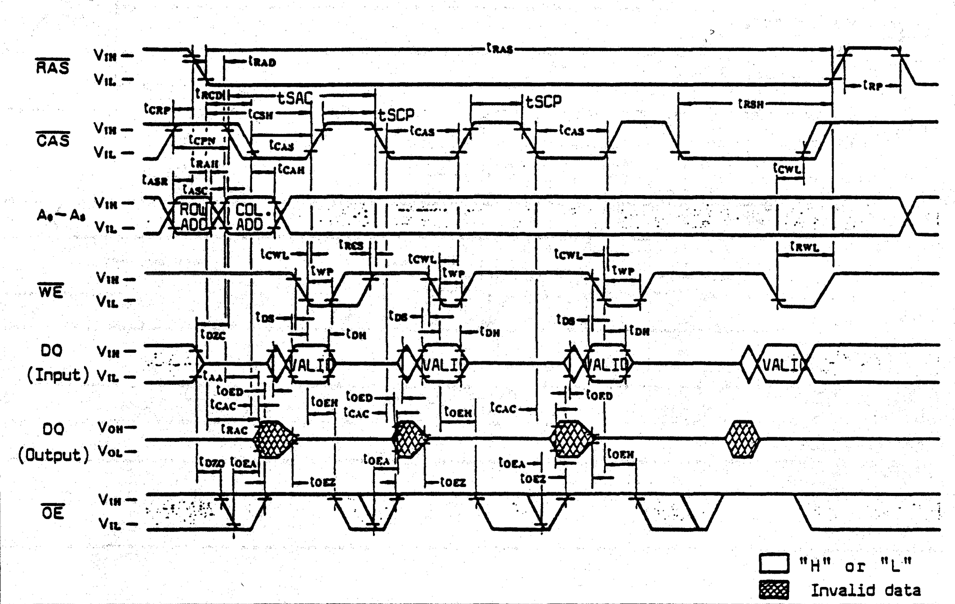
DESCRIPTION

The serial access mode write cycle is executed by the same manner as serial read cycle except for teh state of WE (e.i., WE="L").

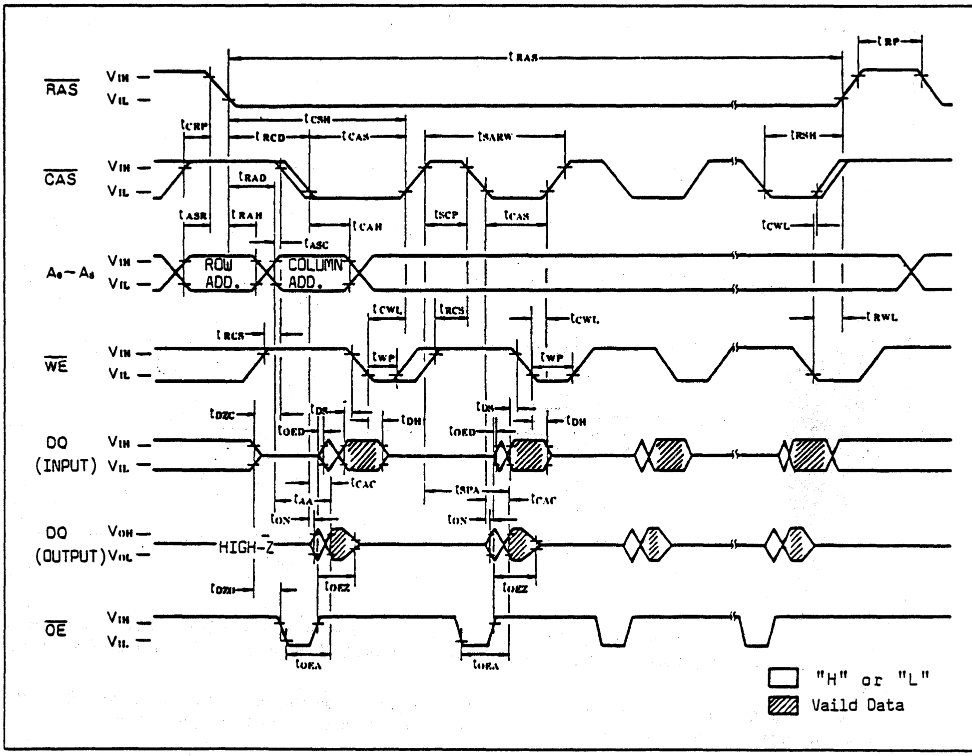
If write operation begins, input data is latched with the later falling edge of CAS or WE. (If write operation is executed by CAS control, it is possible to keep WE="L" during the continuous serial access mode write cycle.)

Data are not refreshed during serial access mode cycle. Therefore, pay attention that refresh requirment must be kept.

Serial Access Mode $\overline{OE}$-Write Cycle

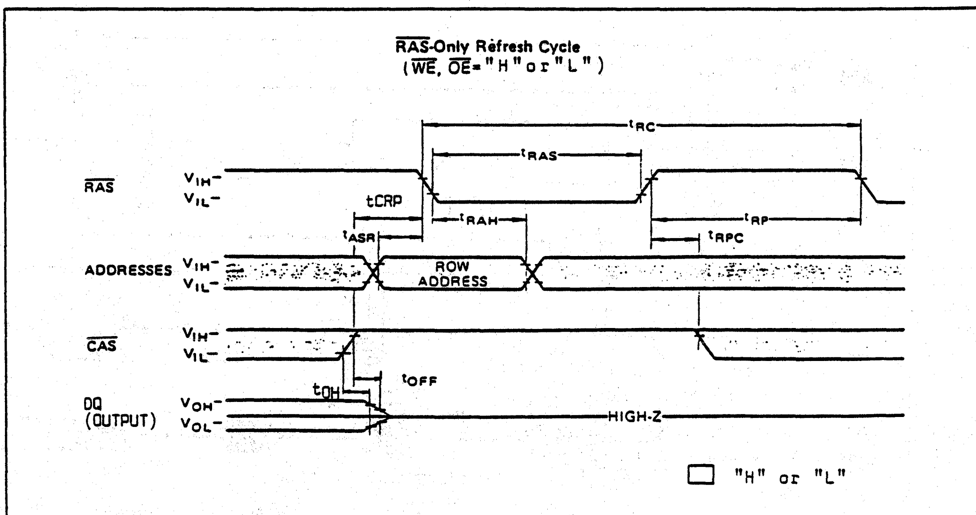


Serial Access Mode Read-Modify-Write Cycle



DESCRIPTION

The read-modify-write cycle can be used during serial access mode as well as normal mode operation. During the serial access mode, all combinations of read, write, and read-modify-write cycle can be applied as well as normal mode operation.



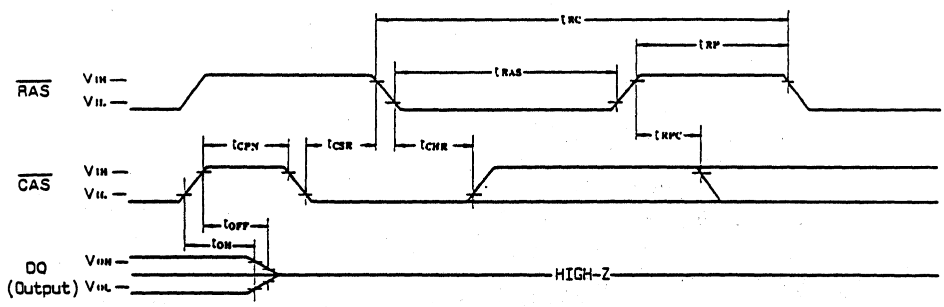
DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available; RAS-only refresh, CAS-before-RAS refresh, and hidden refresh.

RAS-only refresh is performed by keeping RAS Low and CAS High throughout the cycle; the row address to be refreshed is latched on the falling edge of RAS. During RAS-only refresh, DQ pins are kept in a high-impedance state.

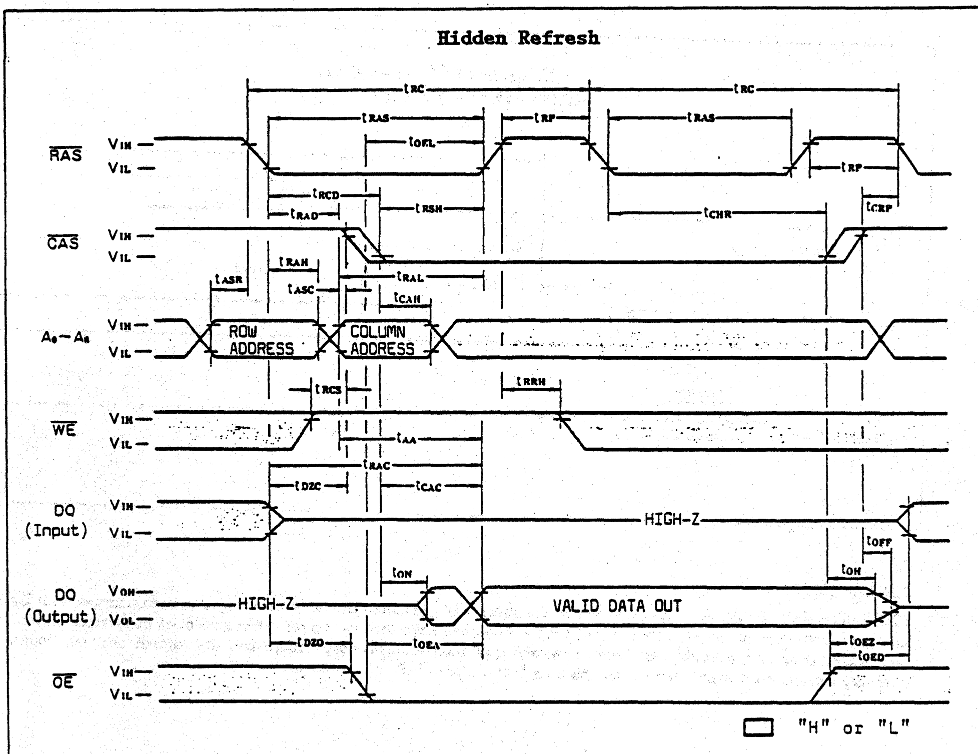
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE: Addresses, $\overline{WE}$, $\overline{OE}$ = "H" or "L"



DESCRIPTION

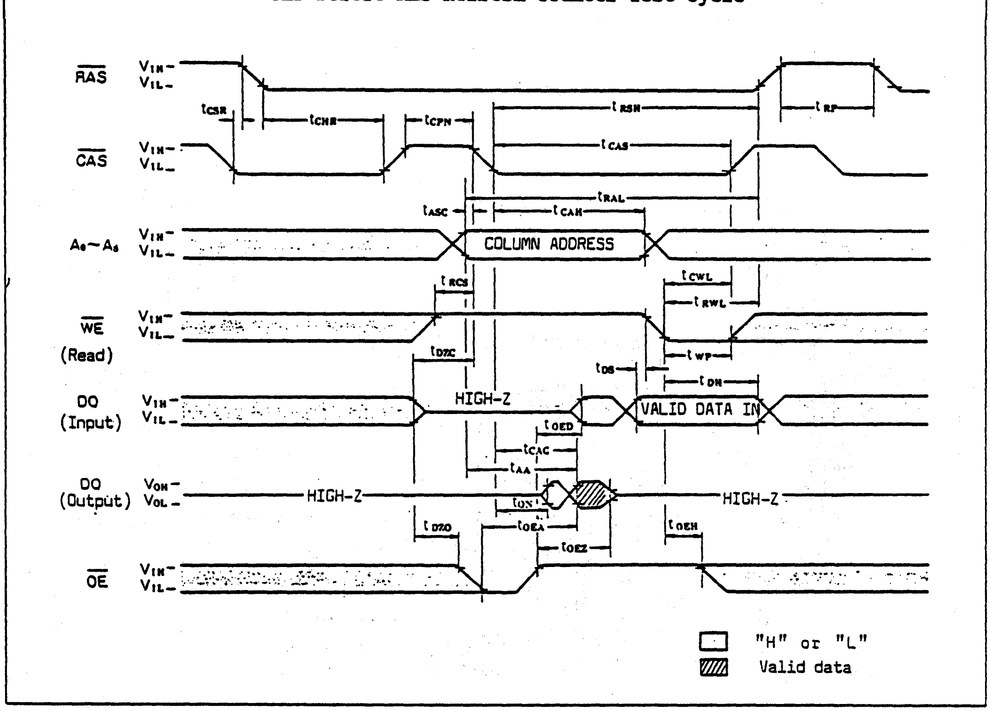
$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

A special timing sequence using the CAS-before-RAS refresh counter test cycle provides a convenient method to verify the functionality of CAS-before-RAS refresh circuitry. If, after a CAS-before-RAS refresh cycle. CAS makes a transition from High to Low while RAS is held Low, read and write operations are enabled as shown above, Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of CAS.

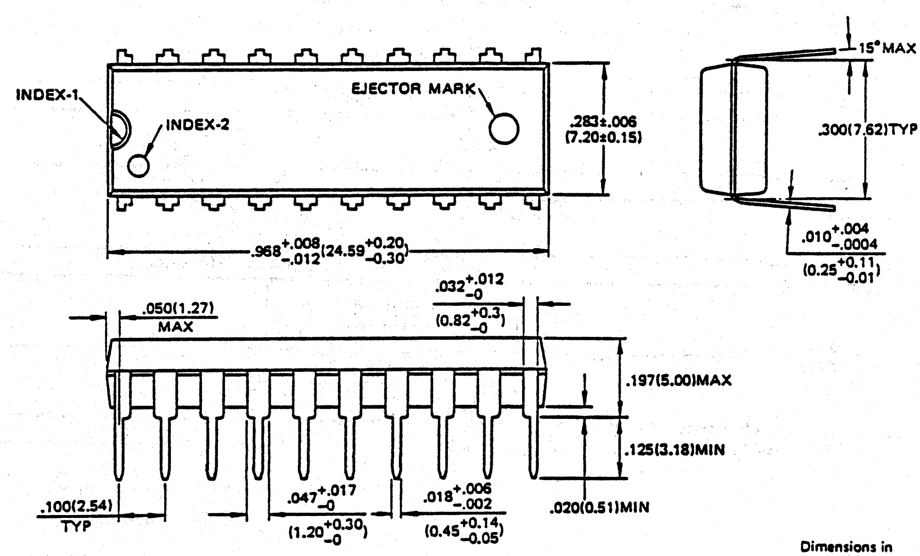
The CAS-before-RAS Counter Test Cycle is designed for use with the following procedures:

1. **Initialize the internal refresh address counter by using eight CAS-before-RAS refresh cycles.**
2. **Use the same column address throughout the test.**
3. **Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.**
4. **Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read-write cycles. Repeat this procedure 5.2 times with addresses generated by the internal refresh address counter.**
5. **Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.**
6. **Complement test pattern and repeat procedures 3, 4, and 5.**

2

PACKAGE DIMENSIONS

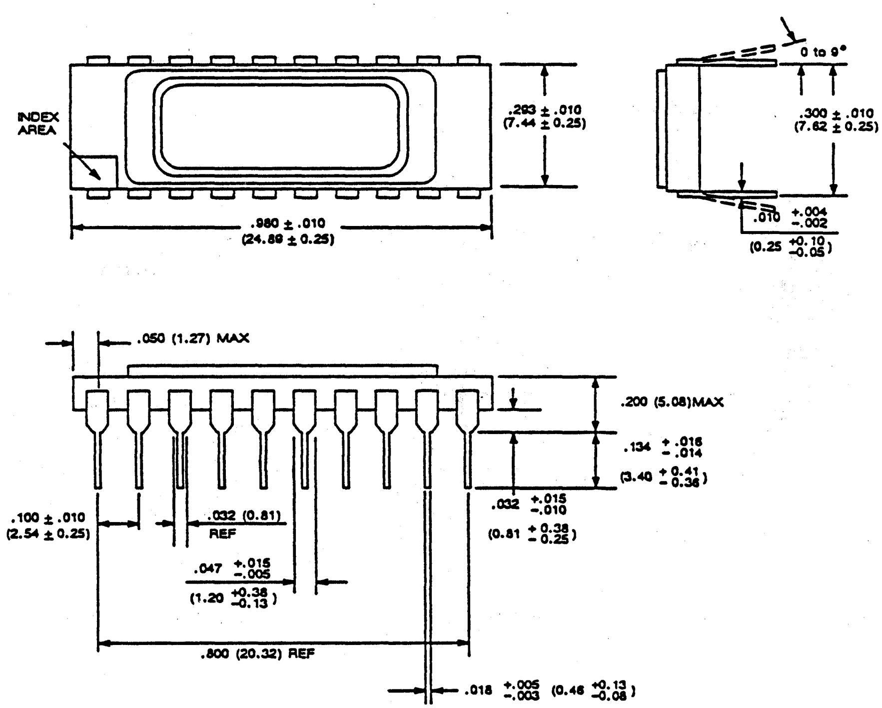
20-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20P-M03)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

20-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-A03)

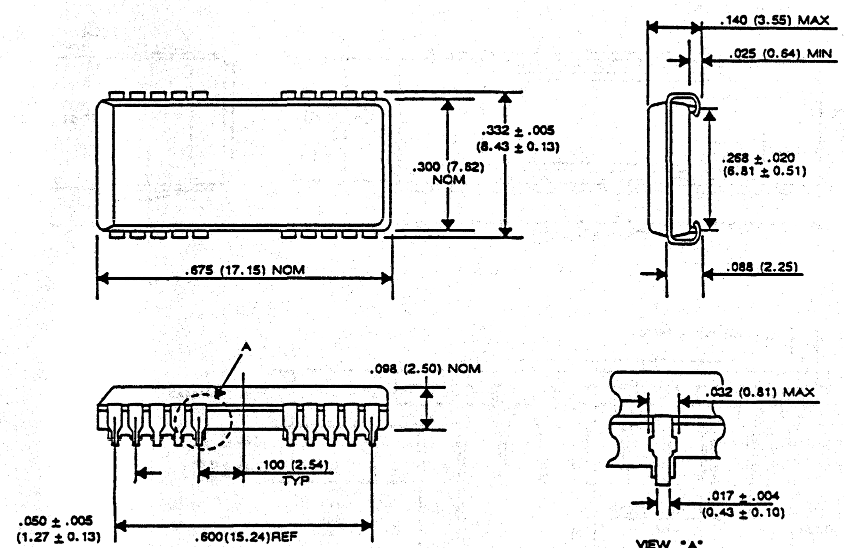


Dimensions in
inches (millimeters)

D20012S-2C

PACKAGE DIMENSIONS (Continued)

26-LEAD PLASTIC LEADED CHIP CARRIER (SOJ-26)
(CASE No.: LCC-26P-M01)



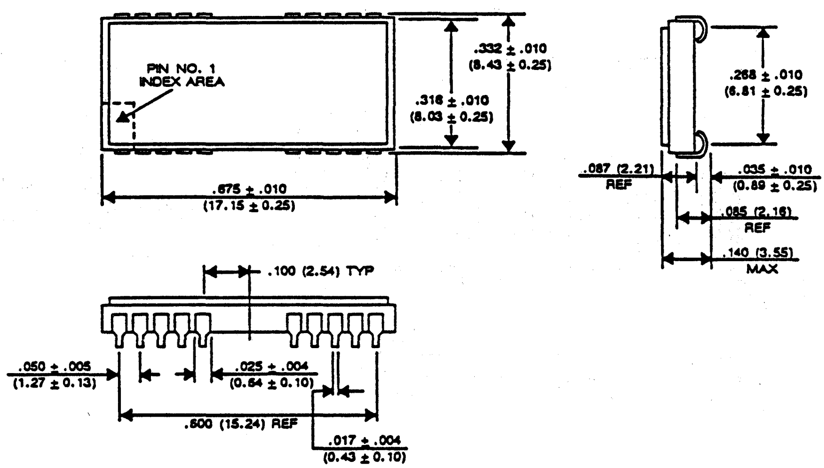
NOTE: Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
Foot-print compatible with "SOJ-26" , LCC-26C-A01.

Dimensions in
inches (millimeters)

C26003S-4C

PACKAGE DIMENSIONS (Continued)

26-LEAD CERAMIC LEADED CHIP CARRIER
(CASE No.: LCC-26C-A01)



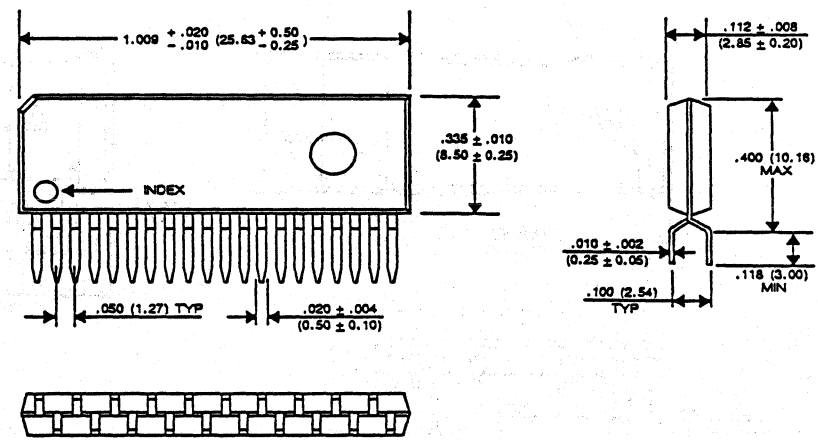
NOTE: Although this package has 20 leads only, its pin positions are the same as that of 26-lead package. Foot-print compatible with "SOJ-26", LCC-26C-A01.

Dimensions in
inches (millimeters)

C26004S-3C

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)



Dimensions in
Inches (millimeters)

Z20002S-2C

FUJITSU

CMOS 4,194,304 BIT FAST PAGE MODE DYNAMIC RAM

MB814100-80
MB814100-10
MB814100-12

2

CMOS 4,194,304 x 1 BIT FAST PAGE MODE DYNAMIC RAM

TS035-A886
June 1988

The Fujitsu MB814100 is CMOS fully decoded dynamic RAM organized as 4,194,304 words x 1 bit. The MB814100 has been designed for mainframe memories, buffer memories, and video image memories requiring highspeed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.
Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB814100 high α-ray soft error immunity and long refresh time.
Since the CMOS circuits are used for peripheral circuits, low power dissipation and high speed operation are realized.

TARGET SPEC

T.B.D.

PLASTIC DIP 18-PIN
(DIP-18P-MXX)

T.B.D.

PLASTIC SOJ 26-PIN
(LCC-26P-MXX)

T.B.D.

PLASTIC ZIP 20-PIN
(ZIP-20P-MXX)

PRODUCT LINE & FEATURES

Parameter	MB814100-80	MB814100-10	MB814100-12
Row Access Time	80ns max.	100ns max.	120ns max.
Random Cycle Time	155ns min.	180ns min.	210ns min.
Column Address Time	45ns max.	50ns max.	60ns max.
Column Access Time	25ns max.	30ns max.	35ns max.
Fast Page Mode Cycle Time	55ns min.	60ns min.	70ns min.
Low Power Dissipation			
• Operating current	413mA max.	358mA max.	303mA max.
• Standby current	11mW max.(TTL level)/5.5mW max.(CMOS level)		

- On-chip latches for both address and data
- TTL compatible inputs and outputs
- Three-dimensional stacked capacitor memory cells
- 1024 refresh cycles every 16.4ms
- RAS only, CAS-before-RAS, or Hidden refresh

ABSOLUTE MAXIMUM RATINGS (See NOTE)

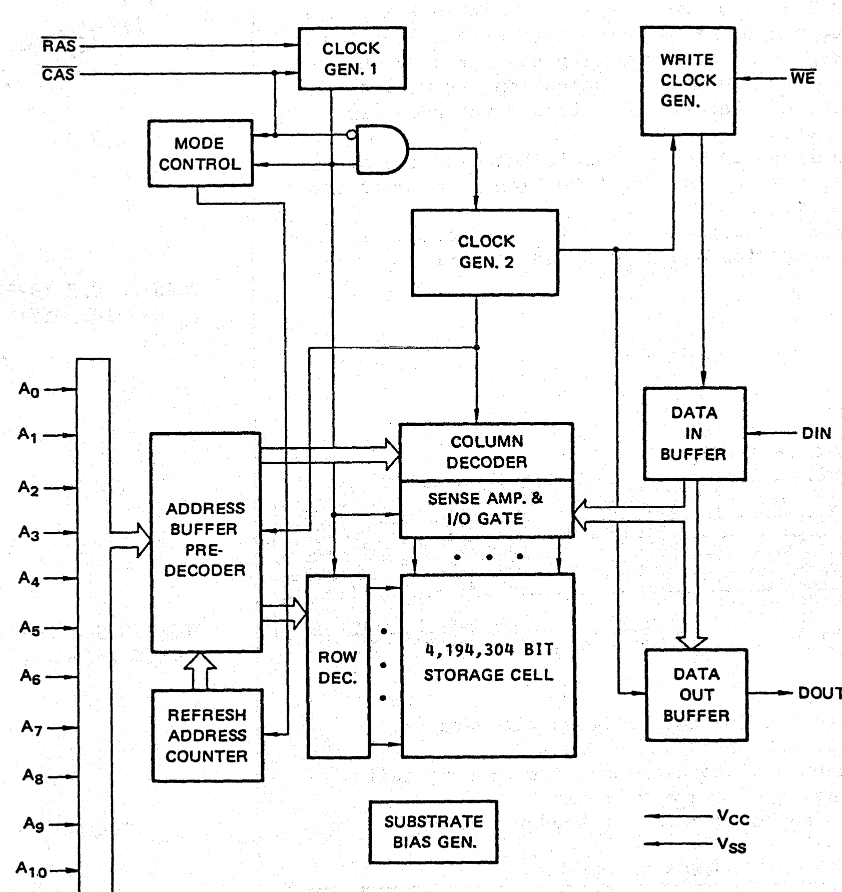
Rating		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} Relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB814100 DYNAMIC RAM – BLOCK DIAGRAM

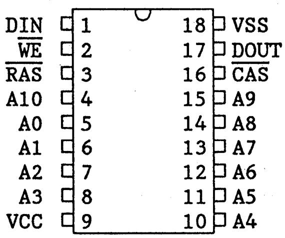


CAPACITANCE (TA=25°C, f=1MHz)

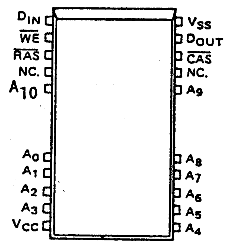
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10, D_{IN}	C_{IN1}		5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		5	pF
Output Capacitance, DOUT	C_{OUT}		5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

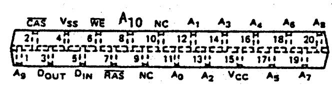
18–Pin DIP:
(TOP VEIW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	:	**Function**
DIN	:	Data Input
DOUT	:	Data Output
WE	:	When active Low, the write mode is enabled, when High, the read mode is enabled.
RAS	:	Row address strobe.
NC	:	No connection.
A0 ~ A10	:	Address inputs.
VCC	:	+5 volt power supply.
CAS	:	Column address strobe.
VSS	:	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

(All voltages referenced to ground; TA=0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Volate	VCC	4.5	5.0	5.5	V
	VSS	0	0	0	
Input High Voltage, all inputs	VIH	2.4		6.5	V
Input Low Voltage, all inputs	VIL	-2.0		0.8	V

2

FUNCTIONAL OPERATION

Address Inputs;

A total of twenty-two binary input address bits are required to decode any one of the 4,194,304 storage cells within the MB814100. Eleven row address bits are established on the address input pins (A0 to A10) and latched with the Row Address Strobe ($\overline{RAS}$). The eleven column address bits are established on the address input pins(A0 to A10) and latched with the Column Address Strobe($\overline{CAS}$). All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively.
Since the flow through type address latches are used, address information at address pins are automatically latched as column address after tRAH (min)+ tT.
If tRAD ≥ tRAD(max), access time is tCAC or tAA whichever occurs later.

Write Enable:

Read or Write mode is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write mode. Data input is ignored during read mode.

Data Input:

Data is written into the MB814100 during write or read-modify-write cycle. The input data is strobed and latched by the latter falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-modify-write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read or read-modify-write cycle, the output becomes valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD}(max) is satisfied or after tCAC from the falling edge of $\overline{CAS}$ when t_{RCD} is longer than t_{RCD}(max) or t_{AA} from column address input when t_{RAD} is greater than t_{RAD}(max). The data output remains valid until $\overline{CAS}$ returns to high. In an early write cycle, the output buffer is in a high impedance state during the entire cycle. In a delayed write cycle, if t_{RWD} or t_{CWD} is less than t_{RWD}(min) or t_{CWD}(min), the output is invalid.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Conditions	Symbol	Value Min	Value Max	Unit
Operating Current* (Average power supply current)	MB814100-80	$\overline{RAS}$&$\overline{CAS}$ cycling; tRC=min	ICC1	–	75	mA
	MB814100-10			–	65	
	MB814100-12			–	55	
Standby Current (Power supply current)	TTL level	$\overline{RAS}$=$\overline{CAS}$=VIH	ICC2	–	2.0	mA
	CMOS level	$\overline{RAS}$=$\overline{CAS}$≥VCC-0.2V		–	1.0	
Refresh Current 1* (Average power supply current)	MB814100-80	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling;tRC=min	ICC3	–	75	mA
	MB814100-10			–	65	
	MB814100-12			–	55	
Fast Page Mode Current*	MB814100-80	$\overline{RAS}$=VIL, $\overline{CAS}$ cycling;tPC=min	ICC4	–	50	mA
	MB814100-10			–	45	
	MB814100-12			–	40	
Refresh Current 2* (Average power supply current)	MB814100-80	$\overline{CAS}$-before-$\overline{RAS}$ tRC=min	ICC5	–	75	mA
	MB814100-10			–	65	
	MB814100-12			–	55	
Input Leakage Current		0V≤VIN≤5.5V, 4.5V≤VCC≤5.5V, VSS=0V;pins not under test=0V	$I_{I(L)}$	-10	10	µA
Output Leakage Current		0V≤VOUT≤5.5V; Data out disabled	$I_{O(L)}$	-10	10	µA
Output High Voltage		IOH=-5mA	VOH	2.4		V
Output Low Voltage		IOL=4.2mA	VOL		0.4	V

*: ICC depends on the output load conditions and cycle rate. The specified values are obtained with the output open.

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) * Notes 1, 2, 3

No.	Parameter	Symbol	MB814100-80		MB814100-10		MB814100-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	Time Between Refresh	tREF		16.4		16.4		16.4	ms	
2	Random Read/Write Cycle Time	tRC	155		180		210		ns	
3	Read-Modify-Write Cycle Time	tRWC	185		210		245		ns	
4	Access Time from $\overline{RAS}$	tRAC		80		100		120	ns	4,7
5	Access Time from $\overline{CAS}$	tCAC		25		30		35	ns	5,7
6	Column Address Access Time	tAA		45		50		60	ns	6,7
7	Output Hold Time	tOH	5		5		5		ns	
8	Output Buffer Turn on Delay Time	tON	5		5		5		ns	
9	Output Buffer Turn off Delay Time	tOFF		25		25		25	ns	8
10	Transition Time	tT	3	50	3	50	3	50	ns	
11	$\overline{RAS}$ Precharge Time	tRP	65		70		80		ns	
12	$\overline{RAS}$ Pulse Width	tRAS	80	100000	100	100000	120	100000	ns	
13	$\overline{RAS}$ Hold Time	tRSH	25		30		35		ns	
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	0		0		0		ns	
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	22	55	25	70	25	85	ns	9,10
16	$\overline{CAS}$ Pulse Width	tCAS	25		30		35		ns	
17	$\overline{CAS}$ Hold Time	tCSH	80		100		120		ns	
18	$\overline{CAS}$ Precharge Time ($\overline{C}$-B-$\overline{R}$ Cycle)	tCPN	15		15		15		ns	15
19	Row Address Set Up Time	tASR	0		0		0		ns	
20	Row Address Hold Time	tRAH	12		15		15		ns	
21	Column Address Set Up Time	tASC	0		0		0		ns	
22	Column Address Hold Time	tCAH	15		15		20		ns	
23	$\overline{RAS}$ to Column Address Delay Time	tRAD	17	35	20	50	20	60	ns	11
24	$\overline{RAS}$ to Column Address Lead Time	tRAL	45		50		60		ns	
25	Read Command Set Up Time	tRCS	0		0		0		ns	
26	Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0		0		0		ns	12
27	Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0		0		0		ns	12
28	Write Command Set Up Time	tWCS	0		0		0		ns	13
29	Write Command Hold Time	tWCH	15		15		20		ns	
30	$\overline{WE}$ Pulse Width	tWP	15		15		20		ns	
31	Write Command to $\overline{RAS}$ Lead Time	tRWL	25		25		30		ns	
32	Write Command to $\overline{CAS}$ Lead Time	tCWL	20		20		25		ns	

AC CHARACTERISTICS - CONTINUED -

(At Recommended operating conditions unless otherwise noted) Note 1, 2, 3

No.	Parameter	Symbol	MB814100-80		MB814100-10		MB814100-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
33	DIN Set Up Time	tDS	0		0		0		ns	
34	DIN Hold Time	tDH	15		15		20		ns	
35	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	tRWD	80		100		120		ns	13
36	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tCWD	25		30		35		ns	13
37	Column Address to $\overline{\text{WE}}$ Delay Time	tAWD	45		50		60		ns	13
38	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time(Refresh cycles)	tRPC	0		0		0		ns	
39	$\overline{\text{CAS}}$ Set Up Time for $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh	tCSR	0		0		0		ns	
40	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$-before -$\overline{\text{RAS}}$ Refresh	tCHR	15		15		20		ns	
41	$\overline{\text{WE}}$ Set Up Time from $\overline{\text{RAS}}$	tWSR	0		0		0		ns	
42	$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$	tWHR	15		15		20		ns	
51	Fast Page Mode Read/Write Cycle Time	tPC	55		60		70		ns	
52	Fast Page Mode Read-Modify-Write Cycle Time	tPRWC	80		85		100		ns	
53	Access Time from $\overline{\text{CAS}}$ Precharge	tCPA		55		60		70	ns	7,14
54	Fast Page Mode $\overline{\text{CAS}}$ Precharge Time	tCP	15		15		15		ns	

NOTES ;

1. An Initial pause($\overline{\text{RAS}}$=$\overline{\text{CAS}}$=VIH) of 200μs is required after power-up followed by any 8 $\overline{\text{RAS}}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
2. AC characteristics assume t_T=5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that tRCD≦tRCD(max), tRAD≦tRAD(max). If tRCD(or tRAD) is greater than the maximum recommended value shown in this table, tRAC will be increased by the amount that tRCD (or tRAD) exceeds the value shown.
5. If $t_{RCD} \geqq t_{RCD}(max)$, $t_{RAD} \geqq t_{RAD}(max)$ and $t_{ASC} \geqq t_{AA}-t_{CAC}-t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geqq t_{RAD}(max)$ and $t_{ASC} \geqq t_{AA}-t_{CAC}-t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min)
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only; If t_{RAD} is greater than the specified t_{RAD}(max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min), and $t_{AWD} \geq t_{AWD}$(min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{OUT} pin, and write operation can be executed by satisfing t_{RWL}, t_{CWL} and t_{RAL} specifications.
14. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
15. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Fig. 2 – tRAC vs. tRCD

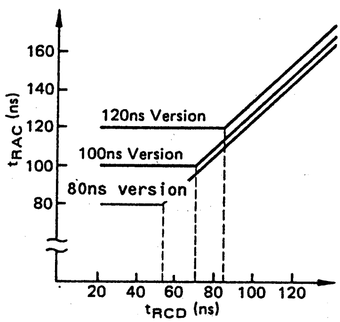
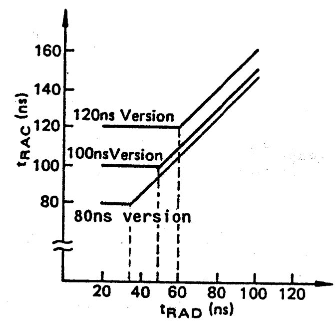


Fig. 3 – tRAC vs. tRAD

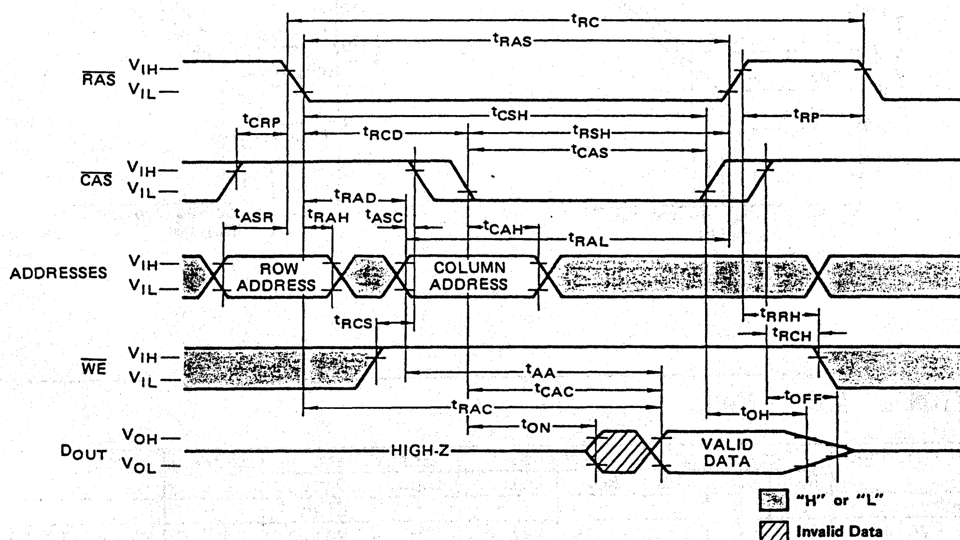


FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	–	–	–	High-Z	–	
Read Cycle	L	L	H	Valid	Valid	–	Valid	○ *	tRCS≥tRCS(min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	○ *	tWCS≥tWCS(min)
Read-Modify-Write Cycle	L	L	H→L	Valid	Valid	X→ Valid	Valid	○ *	
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	–	–	High-Z	○	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	H	–	–	–	High-Z	○	tCSR≥tCSR(min)
Hidden Refresh Cycle	H→L	L	H	–	–	–	Valid	○	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

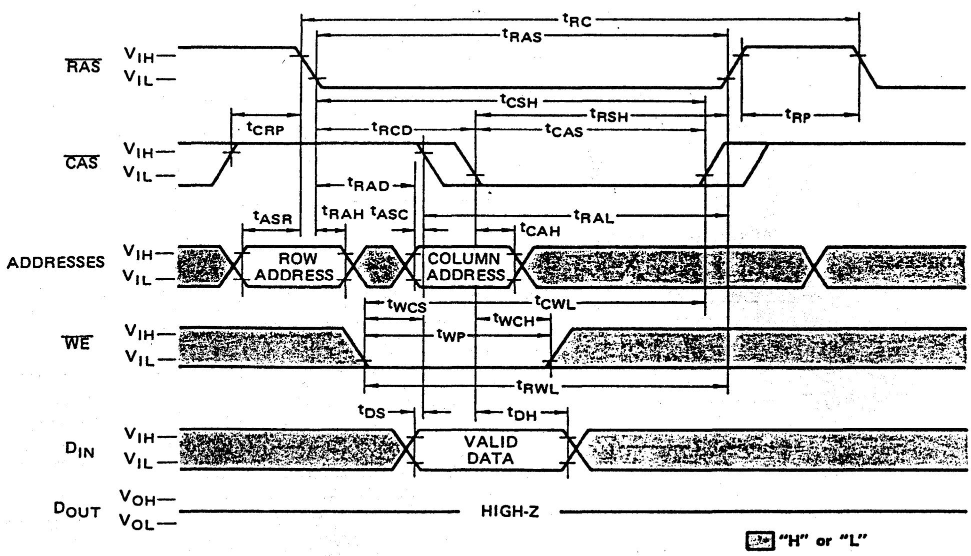
Read Cycle



Description

Read Cycle;
The read cycle is executed by keeping both RAS and CAS "L" and keeping WE "H" throughout the cycle. The row and column addresses are latched with RAS and CAS, respectively. The data outputs remain valid with CAS "L", i.e., if CAS goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by RAS(tRAC), CAS(tCAC), or Column address input(tAA). If tRCD(RAS to CAS delay time) is greater than the specification, the access time is tCAC. If tRAD is greater than the specification, the access time is tAA.

Write Cycle (Early Write)

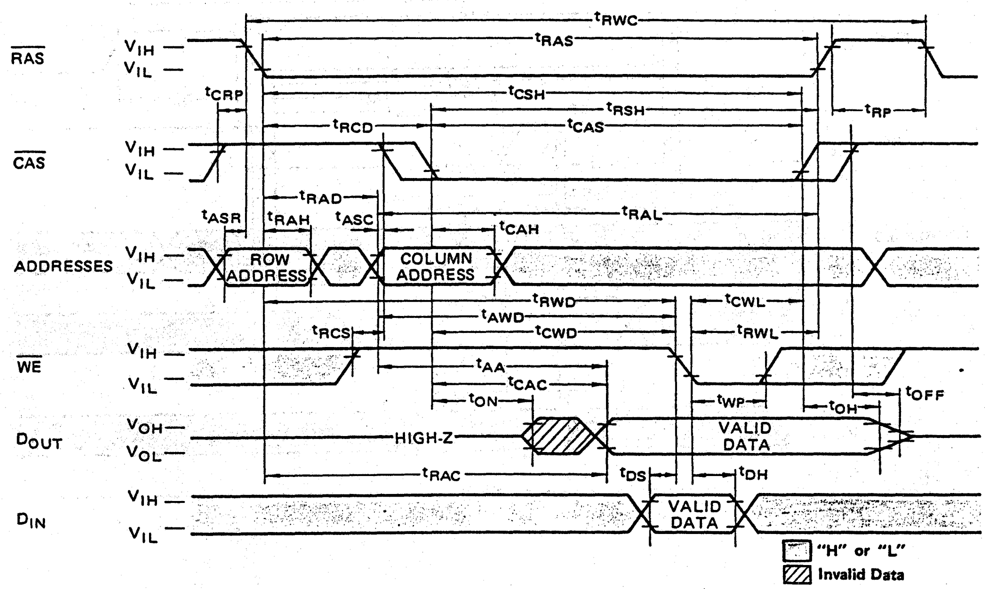


Description

Write Cycle;
The write cycle is executed by the same manner as read cycle except for the state of WE and DIN pins. The data on DIN pin is latched with the latter falling edge of CAS or WE and written into memory. In addition, during write cycle, tRWL, and tRAL must be satisfied the specifications.

2

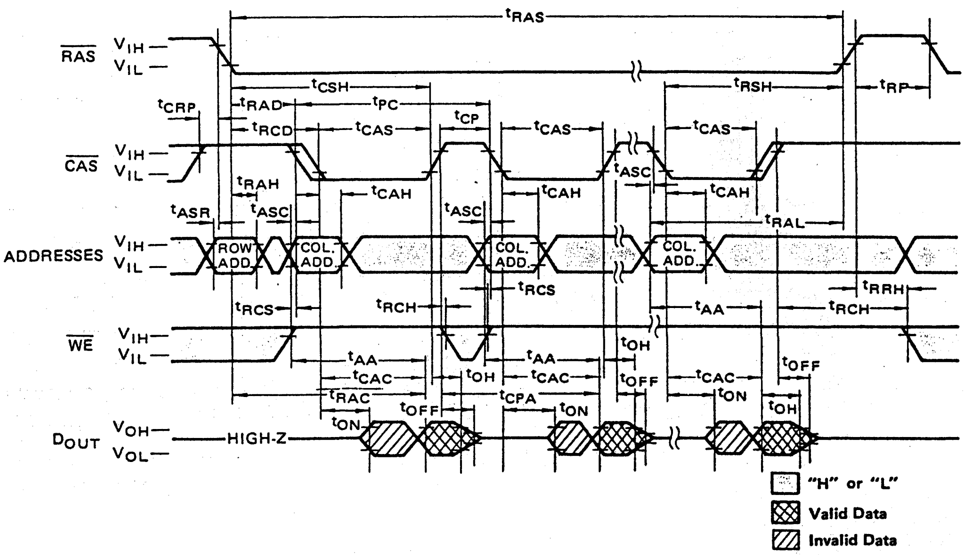
Read-Write/Read-Modify-Write Cycle



Description

Read-Modify-Write Cycle;
The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be re-written into the same address quickly.

Fast Page Mode Read Cycle

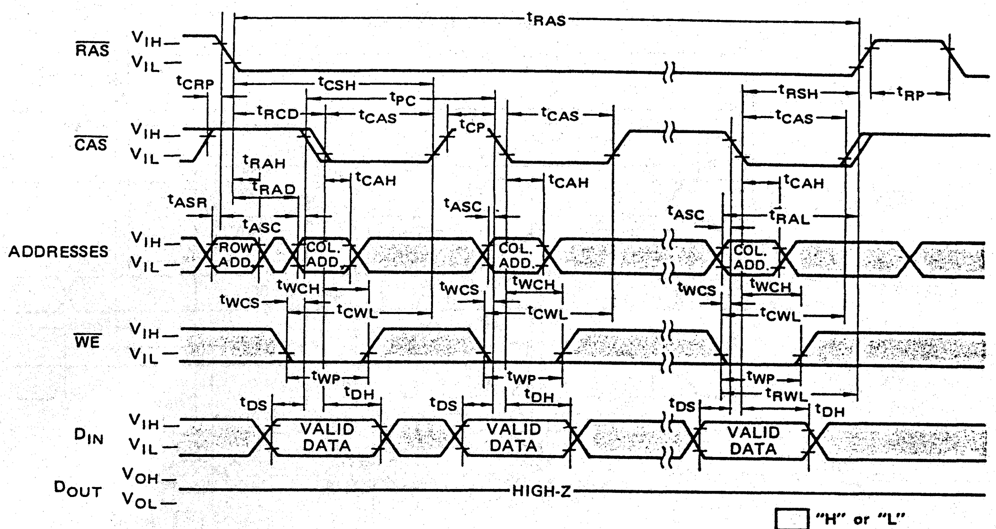


Description

Fast Page Mode Read Cycle;

The fast page mode read cycle is executed after normal cycle with holding RAS "L", applying column address and CAS, and keeping WE "H". Once an address is selected normally using the RAS and CAS, other addresses in the same row can be selected by only changing the column address and applying the CAS. So power consumption and cycle time are reduced.
During fast page mode, the access time is tCAC, tAA, or tCPA, whichever occurs later. Any of the 2048 bits belonging to each row can be accessed.

Fast Page Mode Write Cycle (Early Write)

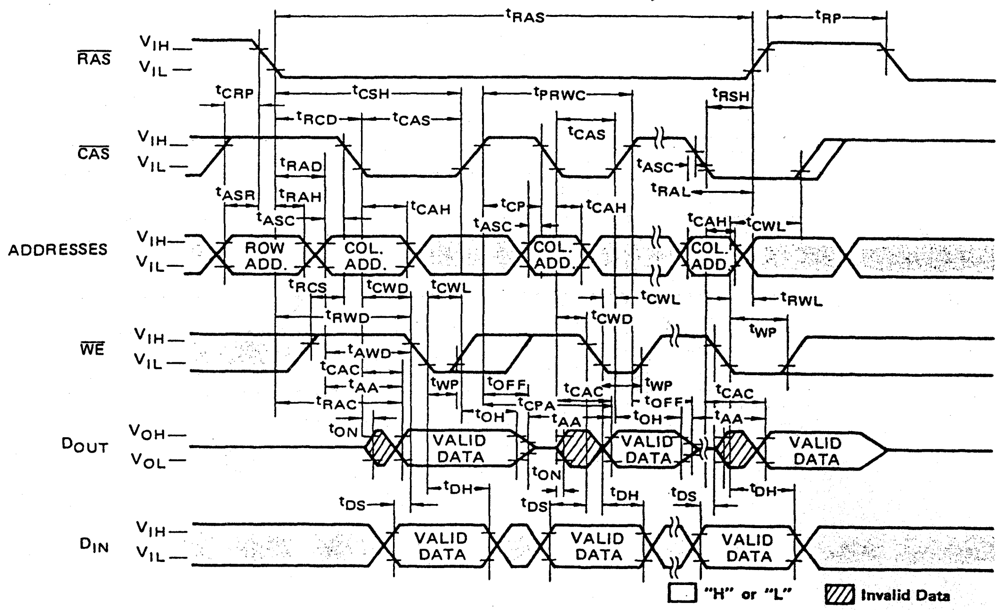


Description

Fast Page Mode Write Cycle;

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of WE. The data on DIN pin is latched with the falling edge of CAS and written into the memory. During fast page mode write cycle, tCWL must be satisfied. Any of the 2048 bits belonging to each row can be accessed.

Fast Page Mode Read-Modify-Write Cycle



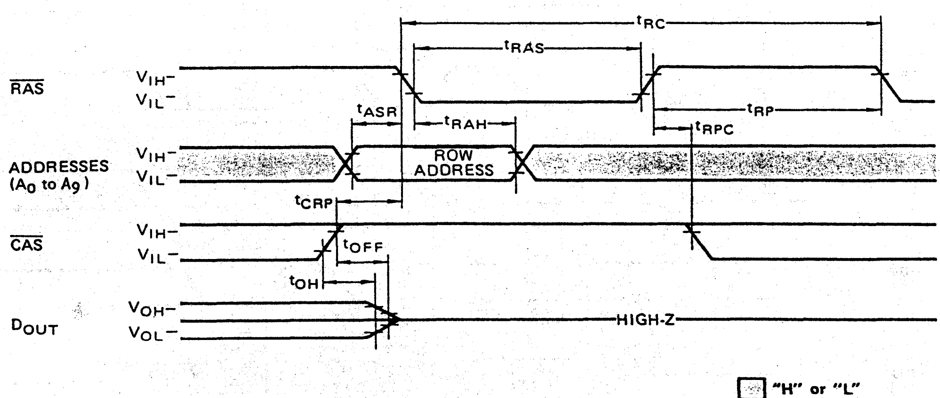
Description

Fast Page Mode Read-Modify-Write Cycle;

During fast page mode, the read-modify-write cycle can be executed by changing $\overline{WE}$ high to low after the data appears at DOUT pin as well as normal cycle. Any of the 2048 bits belonging to each row can be accessed.

2

$\overline{RAS}$-only Refresh Cycle
NOTE: $\overline{WE}$, D_{IN} = Don't care, A_{10}= V_{IH} or V_{IL}

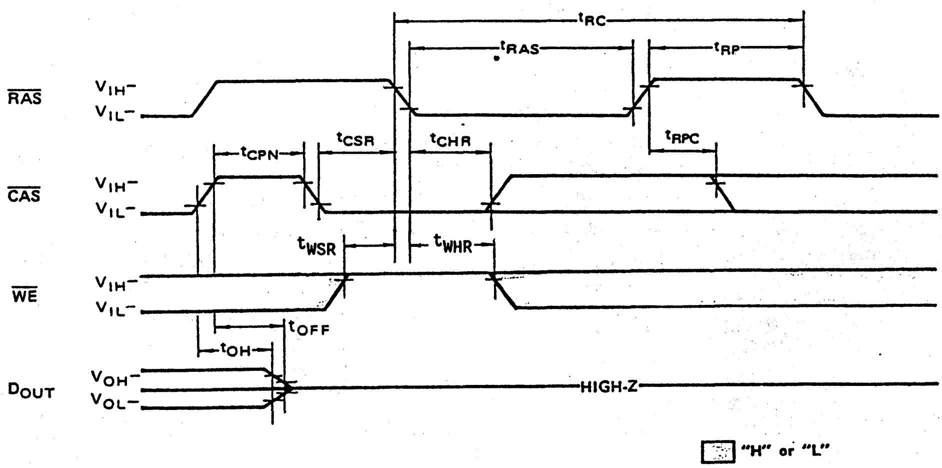


Description

Refresh;
The refresh of DRAM is executed by normal read, write or read-modify-write cycle, i.e., the cells on the one row line are also refreshed by executing one of three cycles. 2048 row address must be refreshed every 16.4ms period. Durign the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-written to the cell. The MB814100 has three types of refresh modes, RAS-Only refresh, CAS-before-RAS refresh, and Hidden refresh.

$\overline{RAS}$-Only Refresh;
The RAS only refresh is executed by keeping $\overline{RAS}$ "L" and $\overline{CAS}$ "H" throughout the cycle. The row address to be refreshed is latched on the falling edge of RAS. During RAS-Only refresh, the DOUT pin is kept in a high impedance state.

CAS-before-RAS Refresh Cycle
NOTE: Address, D_{IN} = Don't care



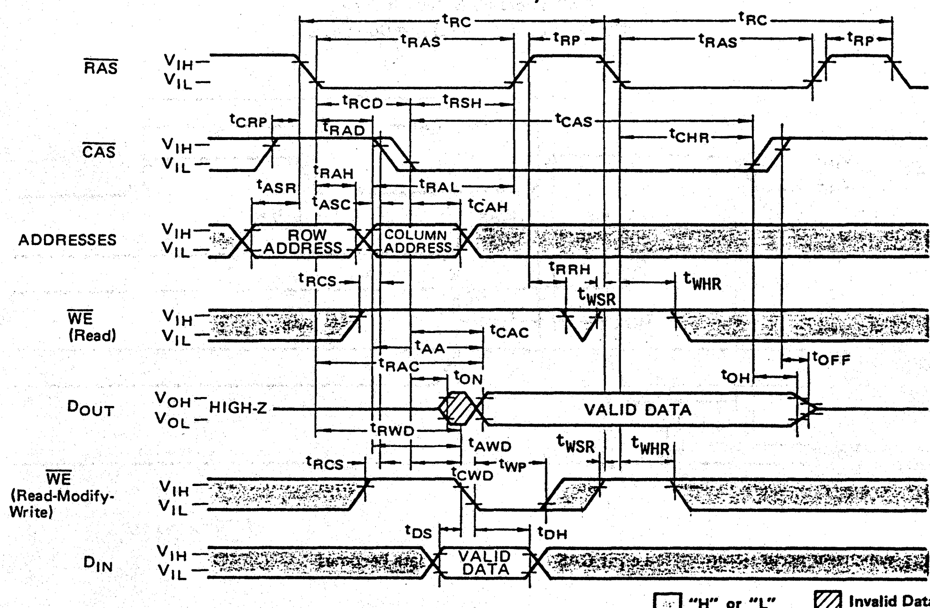
Description

CAS-before-RAS Refresh;

The CAS-before-RAS refresh is executed by bring CAS "L" before RAS. By this timing combination, the MB814100 executes CAS-before-RAS refresh. The row address input is not necessary because it is generated internally.

2

Hidden Refresh Cycle



Description

Hidden Refresh;
The Hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the CAS is kept low continuously from previous cycle, followed refresh cycle should be CAS-before-RAS refresh.

2

Section 3

MOS Application-Specific RAMs

3

FUJITSU

262144-BIT DUAL PORT DYNAMIC RANDOM ACCESS MEMORY

MB81461-12 MB81461-15

July 1987
Edition 3.0

3

262,144 BIT DUAL PORT DRAM

The Fujitsu MB 81461 is a fully decoded dual port NMOS dynamic random access memory organized as 65,536 words by 4 bits dynamic RAM port and 256 words by 4 bits serial access memory (SAM) port.

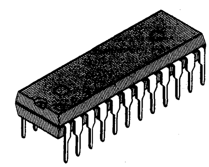
The DRAM port is identical to the Fujitsu MB 81464 with four bits parallel random access I/O while the SAM port is designed as four 256 bit registers each operating as a serial I/O. The four serial registers operate in parallel with each other during SAM port operation. Internal interconnects give the device the capability to transfer data bi-directionally between the DRAM memory array and the SAM data registers.

The MB 81461 offers complementely asynchronous access of both the DRAM and SAM ports except when data is transfered between them internally.

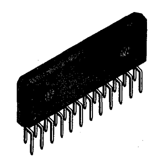
The design is optimized for high speed and performance which makes the MB 81461 the most efficient solution for implementing the frame buffer of a bit mapped video display system. Multiplexed row and column address inputs permit the MB 81461 to be housed in a 400 mil wide 24 pin DIP and ZIP. Pin outs conformed to the JEDEC approved pin out.

The MB 81461 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple Layer Polysilicon process technology. This process coupled with single transistor memory storage cells permits maximum circuit density and minimum chip size. All inputs and outputs are TTL compatible.

- Dual port organization
  64K x 4 Dynamic RAM port (DRAM)
  256 x 4 Serial Access Memory port (SAM)
- 24 pin DIP and ZIP package
- Silicon-gate, Triple Poly NMOS, single transistor cell
- DRAM Port
  Access Time (t_{RAC}),
  120ns max. (MB 81461-12)
  150ns max. (MB 81461-15)
  Cycle Time (t_{RC}),
  230ns min. (MB 81461-12)
  260ns min. (MB 81461-15)
- SAM Port
  Access Time (t_{SAC}),
  40 ns max. (MB 81461-12)
  60 ns max. (MB 81461-15)
  Cycle Time (t_{SC}),
  40ns min. (MB 81461-12)
  60ns min. (MB 81461-15)
- Single +5V power supply, ±10% tolerance
- Power Dissipation
  DRAM; Act/SAM; Stby
  523mW max. (MB 81461-12)
  468mW max. (MB 81461-15)
  DRAM; Stby/SAM; Act
  275mW max. (MB 81461-12)
  220mW max. (MB 81461-15)
  DRAM; Stby/SAM; Stby
  110mW max.
- Bi-directional Data Transfer between DRAM and SAM
- Fast serial access asynchronous to DRAM except transfer operation
- Real Time Read Transfer Capability
- Page Mode capability
- Bit Masked Write Mode capability
- 256 refresh cycles every 4ms
- RAS-only, CAS-before-RAS and Hidden refresh capability
- Delayed write and Read-Modify-Write capability
- Standard 24 pin plastic DIP (Suffix; -P)
- Standard 24 pin plastic ZIP (Suffix; -PSZ)

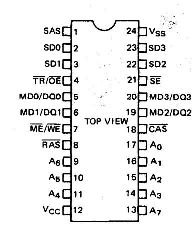


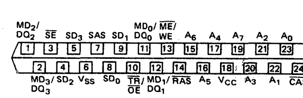
PLASTIC PACKAGE
DIP-24P-M04



PLASTIC PACKAGE
ZIP-24P-M02

PIN ASSIGNMENT





BOTTOM VIEW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

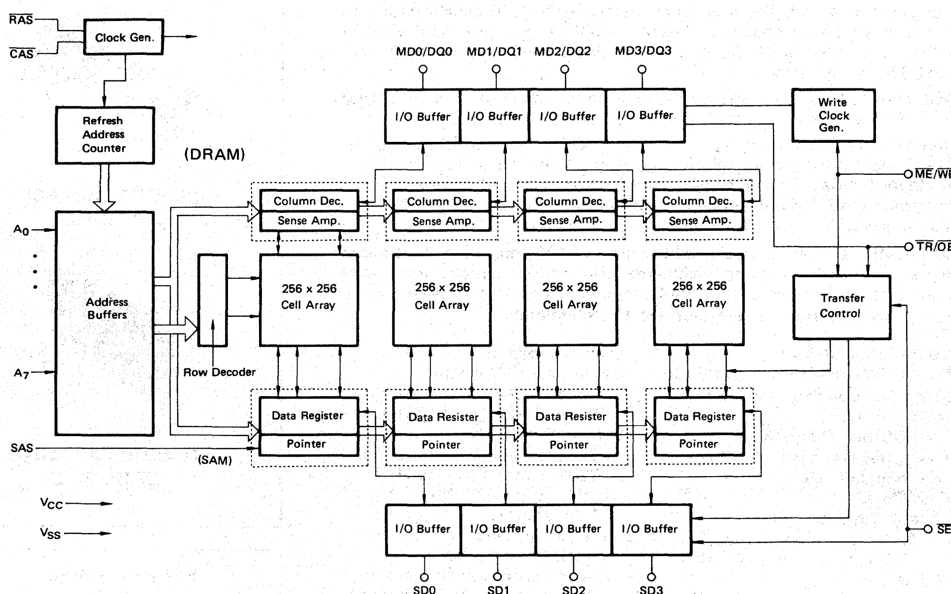
Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-1 to +7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit output current	—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Fig. 1 — BLOCK DIAGRAM OF MB 81461 and PIN DESCRIPTION

Block Diagram



Pin Description

Pin Number		Symbol	Parameter	Mode
DIP	ZIP			
1	7	SAS	Serial Access Memory Strobe	Input
2,3,22,23	8,9,4,5	SD0 to SD3	Serial Data I/O	I/O
4	10	$\overline{TR}/\overline{OE}$	Transfer Enable/ Output Enable	Input
5,6,19,20	11,12,1,2	MD0/DQ0 to MD3/DQ3	Mask Data/Data I/O	I/O
7	13	$\overline{ME}/\overline{WE}$	Mask Mode Enable/Write Enable	Input
8	14	$\overline{RAS}$	Row Address Strobe	Input
17, 16, 15 14, 11, 10 9, 13	23,22,21, 20,17,16, 15,19	A_0 to A_7	Address Input	Input
12	18	V_{CC}	Supply Voltage +5 V	Power Supply
18	24	$\overline{CAS}$	Column Address Strobe	Input
21	3	$\overline{SE}$	Serial port Enable	Input
24	6	V_{SS}	Ground	Power Supply

DESCRIPTION

DRAM OPERATION

RAS;

This pin is used to strobe eight row-address inputs from A0 to A7 pins and is used to select the operation mode of subsequent cycle, such as DRAM operation or transfer operation (by TR/OE and bit mask write cycle or not (by ME/WE and MD0/DQ0 to MD3/DQ3). Since RAS = "L" is the active condition of circuit, to maintain RAS = "H" (standby condition) is effective to save power dissipation.

CAS;

This pin is used to strobe eight column address inputs at the falling edge. CAS pin has the function to enable and disable the output at "L" and "H" respectively during the read operation.
Another function of CAS is to select "early write" mode conditioned by ME/WE = "L".

ME/WE;

This pin is used to select read or write cycle. ME/WE = "L" select write mode and ME/WE = "H" select read mode. This pin is also used to enable bit mask write cycle. If ME/WE = "L" at the falling edge of RAS, bit mask write is enabled.

TR/OE;

This pin is used to select Transfer operation or not at the falling edge of RAS, TR/OE = "H" enables DRAM operation and TR/OE = "L" enables Transfer operation between DRAM and SAM. After the falling of RAS with t_{YH}, this pin is used for output enable.
The TR/OE controls the impedance of the output buffers. TR/OE = "H" forces the output buffers at high impedance state. TR/OE = "L" leads the output buffers at low impedance state. But in early write cycle, the output buffers are high impedance state even if TR/OE is low.

A0 to A7;

These are multiplexed address input pins and used to select 4 bits of 262,144 memory cell locations in parallel within the MB 81461. The eight row address inputs are strobed by RAS and followed eight column address inputs are strobed by CAS. These are used to select the start address of serial access memory also.

MD0/DQ0 to MD3/DQ3

These are common I/O pins of DRAM port. I/O mode is as specified for each function mode in the truth table.

Data Outputs:

The output buffers have three-state capability "H", "L" and "High-Z". To get valid output data on the pins, one of the read operations is selected such as "read" or "read-modify-write" mode. During a refresh cycle, either RAS-only or CAS-before-RAS mode is selected, output buffers are set in "High-Z" state.

Data inputs:

These are used as data input pins when a data write mode such as "Early-Write", "Delayed Write" or "Read-modify-Write" is selected. In any of the above cases, these pins are set at "High-Z" state to enable data-in without any bus conflict.
In any operation mode, read, write, refresh, transfer and their combined functions, output states "H", "L", "High-Z" are set by control signals RAS, CAS, ME/WE and/or TR/OE. When "Bit mask write" mode is set, these pins are used as a control signal for write inhibit with MDi/DQi = "L" on the selected bit i.

Page Mode;

The page mode operation is to strobe the column address by CAS while RAS is maintained at "L" through all the successive memory operations if the row address doesn't change. This mode can save power dissipation and get the faster access time due to the elimination of RAS falling edge function.

Refresh;

Refresh of the DRAM cells is performed for every 256 rows per every 4 milliseconds.
The MB 81461 offers the following three types of refresh.

1) RAS-Only refresh; The RAS-Only refresh is performed with CAS="H" condition. Strobing every 256 row addresses with RAS will complete all bits of memory cell to be refreshed while all outputs are invalid due to "High-Z" state. Further RAS-only refresh saves the power dissipation substantially.
2) CAS-before-RAS refresh; The CAS-before-RAS refresh offers an alternate refresh method. If CAS is set low for the specified period (t_{FCS}) before the falling edge of RAS, refresh control clock generator and refresh address counter are enabled, and an refresh operation is performed. After the refresh operation is performed, the refresh address counter is incremented automatically for the next CAS-before-RAS refresh.
3) Hidden refresh; The hidden refresh is performed by maintaining the valid data of last read cycle at MD/DQ pins while extending CAS low. The hidden refresh is equivalent to CAS-before-RAS refresh because CAS stays low when RAS goes to low in the next cycle.

Bit Mask Write;

This mode is used when some of the bits should be inhibited to be written into cells. The bit mask write mode is executed by setting ME/WE = "L" at the falling edge of RAS during write mode (early, delayed write or read-modify-write cycle). The bits to be masked (or inhibited to write) is determined by MD/DQ state at the falling edge of RAS, for example, if MD0/DQ0 and ME/WE are both low at the falling edge of RAS, the data on MD0/DQ0 pin is not written into the cell during the cycle. Refer to the Fig. 2.

EXAMPLE OF BIT MASK WRITE OPERATION

Falling edge of RAS						Function
TR/OE	ME/WE	MD0/DQ0	MD1/DQ1	MD2/DQ2	MD3/DQ3	
H	H	X	X	X	X	Write enable
	L	H	L	H	L	Write enable for DQ0 and DQ2 Write disable for DQ1 and DQ3

X: Don't Care

FUNCTIONAL TRUTH TABLE FOR DRAM OPERATION

RAS	CAS	ME/WE	TR/OE	ADDRESSES	MD0/DQ0 to MD3/DQ3	Function
H	H	X	X	X	X	Standby
L	L	H	H→L	Valid	Valid Data Out	Read
L	L	L*	H→X	Valid	Valid Data In	Early Write
L	L	H→L	H → X → H	Valid	Valid Data In	Delayed Write
L	L	H→L	H→L→H	Valid	Valid Data Out → Valid Data In	Read-Modify-Write
L	H	X	H→X	Row address	High-Z	RAS-Only Refresh
H→L	L	X	H→X	X	High-Z	CAS-before-RAS Refresh

*: If ME/WE = "L" at the falling edge of RAS, bit mask write mode is enabled.

TRANSFER OPERATION:

The transfer operation is featured in the MB 81461B. This mode is used to transfer simultaneously 256x4 data from DRAM to SAM or from SAM to DRAM. The direction of transfer is determined by the state of ME/WE at the falling edge of RAS. ME/WE="H" defines the transfer from DRAM to SAM (Read Transfer Cycle) and ME/WE="L" defines the transfer from SAM to DRAM (Write Transfer Cycle).

I/O mode of SD0 to SD3 determined while the transfer operation is set (TR/OE="L") conjunctioned with ME/WE state.

After Read Transfer Cycle, please apply two or more SAS Clock.

TR/OE;

This pin is used to enable transfer operation at the falling edge of RAS.

ME/WE;

This pin is used to select the direction of transfer at the falling edge of RAS.

A0 to A7;

These pins are used to select the row address of DRAM port to be transfered from or to, and the start address of SAM port for the serial read or write operation. The row address is strobed by RAS and the start address is strobed by CAS.

Pseudo Write Transfer:

To start serial write cycle, the SD pins must be set in input mode. To do this, write transfer cycle should be executed. The pseudo write transfer cycle is to change the SD pins into input mode without data transfer from SAM to DRAM. Refer to Fig. 3.

Refresh during transfer cycle;

DRAM and SAM are refreshed during transfer cycle as shown below.

1) Read transfer cycle:
   During read transfer cycle, the selected row address of DRAM to be transfered to SAM is refreshed. SAM data are kept by applying 256 SAS clocks within 4 ms after the read transfer cycle.
2) Write transfer cycle:
   During write transfer cycle, the new data are written from SAM to DRAM and this row address should be refreshed within 4 ms.
   But SAM data are not refreshed during write transfer cycle. Therefore, the SAM refresh (applying 256 SAS clocks within 4 ms) must be executed. Especially, when the write transfer cycle is executed continuously, 256 SAS clock should be applied within 4 ms.

SERIAL ACCESS OPERATION:

The MB 81461 has 256 words by 4 bits Serial Acess Memory (SAM) corresponding to 64K words by 4 bits DRAM and the fast serial read/write access is achieved by SAM architecture. Read or write cycle is determined when the last read or write transfer operation is executed. If the last transfer operation was read transfer, the serial read cycle is performed until the next write or pseudo write transfer cycle is executed. On the other hand, if the last transfer operation was write or pseudo write or pseudo write transfer, the serial write cycle is performed. In the serial write operation, 256 words by 4 bits data stored in the SAM can be transfered to DRAM under SE="L" condition, and SE="H" condition disables data transfer from SAM to DRAM. The serial access operation can be done asynchronously from DRAM port.

SAS;

This pin is used as a shift clock for SAM port. The serial access is triggered by the rising edge of SAS. In the write cycle, the data of the SD pins are strobed by the rising edge of SAS and written into the selected cell. In the read cycle, output data become valid after t_{SAC} from the rising edge of SAS and the data remain valid until the next cycle is defined. The SAS clock increments the SAM address automatically. When the SAM address exceeds #255 (Most Significant Address) it returnes to #0 (Least Significant Address).

$\overline{SE}$;
This pin is used to enable serial access operation by bit to bit. $\overline{SE}$ = "H" disables serial access operation. In the serial read operation, this pin is used for output enable, i.e., $\overline{SE}$ = "H" leads SD pins to "High-Z" state. $\overline{SE}$ = "L" leads SD pins to valid data with specified access time. In the serial write operation, this pin works as write enable control pin.

SD0 to SD3;
These are used as data input/output pins for SAM port. Input or output mode is determined by last occured transfer operation, if last transfer operation was read transfer mode, they are output mode. If the write transfer mode was set, SD pins are enabled to write data into SAM.

Refresh;
Since the SAM is constructed by dynamic circuitry, the refresh is necessary to maintain the data in it. The refresh of SAM must be done by 256 cycles of SAS clock/4ms in either output or input mode. $\overline{SE}$ = "H" allows refresh of SAM with SD pins at "High-Z" state.

Real Time Read Transfer;
This feature is applicable to obtain valid data continuously when row address is changed without any timing loss from the last bit of previous row to the first bit of new row. Data transfer from DRAM to SAM is triggered by rising edge of $\overline{TR}/\overline{OE}$ after the preparation of internal circuit for this operation, while SAM port can continue read operation asynchronously from the above mentioned internal move. Once $\overline{TR}/\overline{OE}$ returns to "H" with the restricted timing specification t_{TSL} and t_{TSD} refered to SAS clock, SD pins can get the valid output data continuously as shown in Fig. 4. The key issue to achieve this feature is to apply SAS clock continuously with the timing consideration to the rising edge of $\overline{TR}/\overline{OE}$.

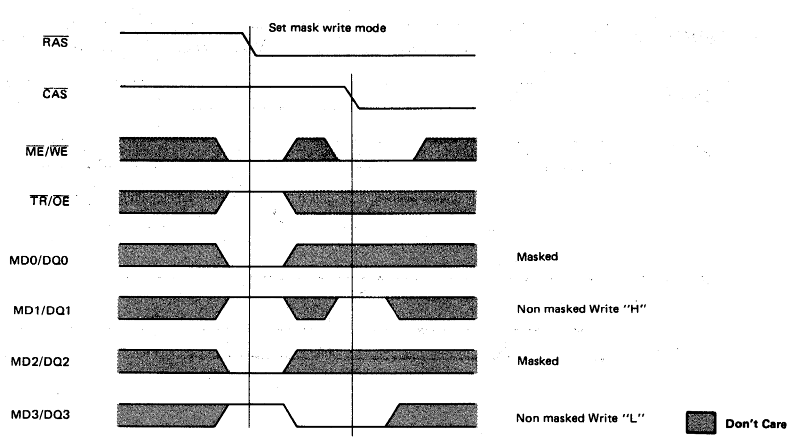
FUNCTIONAL TRUTH TABLE FOR SERIAL ACCESS (Asynchronous from DRAM port)

Falling edge of $\overline{RAS}$		SAS	$\overline{SE}$	SD0 to SD3	Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$				
H	X	Clock	L	Input/Output*	Sequential access enable
		Clock	H	Input/Output*	Sequential access disable

*: The read or write operation of SAM port is pre-determined by the last occurred transfer cycle. Input mode is for write operation. Output mode is for read operation.

X; Don't Care

Fig. 2 — EXAMPLE OF BIT MASK WRITE OPERATION



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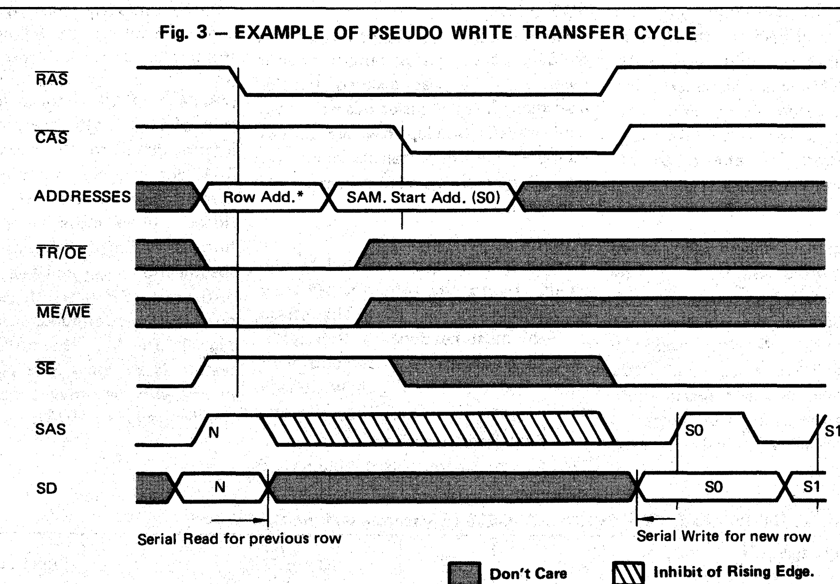
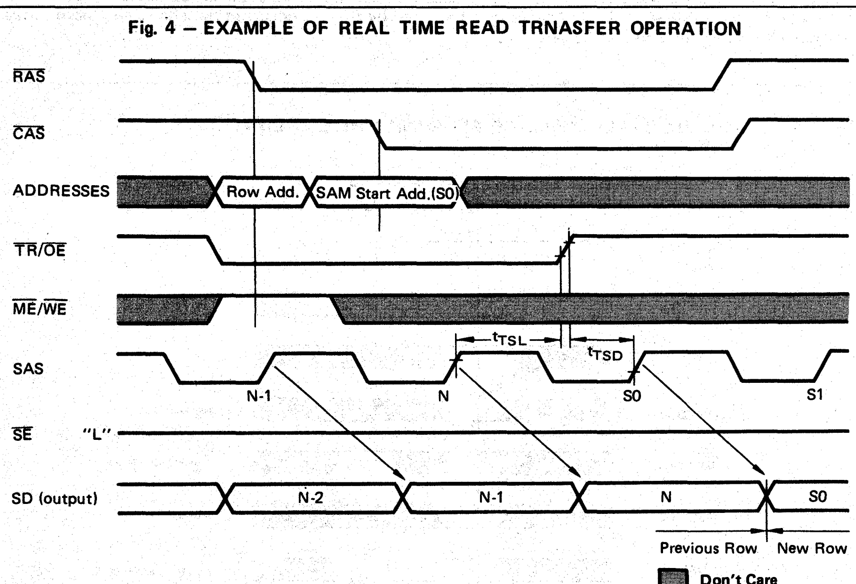


*The DRAM data of this row address are refreshed during pseudo write transfer cycle.



3

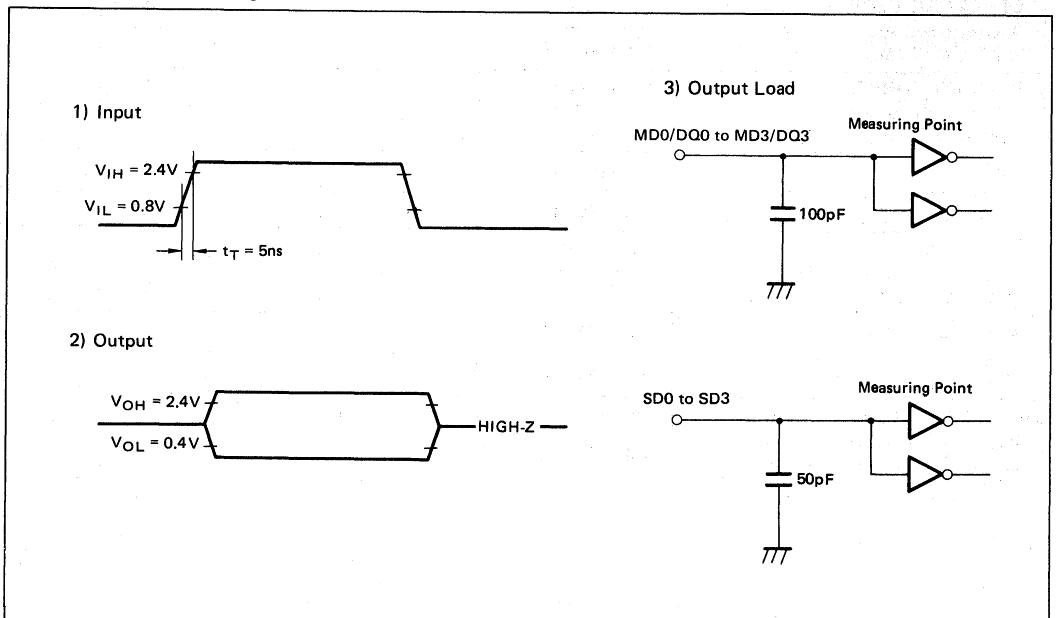
RECOMMENDED OPERATING CONDITIONS
(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4		6.5	V	
Input Low Voltage	V_{IL}	-2.0		0.8	V	

CAPACITANCE (T_A=25°C)

Paramter	Symbol	Typ	Max		Unit
			DIP	ZIP	
Input Capacitance (A0 to A7)	C_{IN1}		7	8	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{SE}$, $\overline{TR}/\overline{OE}$)	C_{IN2}		10	12	pF
Input Capacitance (SAS)	C_{IN3}		7	7	pF
Input/Output Capacitance (MD0/DQ0 to MD3/DQ3)	C_{IO1}		7	8	pF
Input/Output Capacitance (SD0 to SD3)	C_{IO2}		7	8	pF

AC TEST CONDITIONS



3

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
SAM STANDBY $\overline{SE} = V_{IH}$, SAS = V_{IL}					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC1}		95	mA
	MB 81461-15			85	
STANDBY CURRENT Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}		20	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC3}		77	mA
	MB 81461-15			70	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = cycling, t_{PC} = min)	MB 81461-12	I_{CC4}		50	mA
	MB 81461-15			45	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461-12	I_{CC5}		77	mA
	MB 81461-15			70	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC6}		110	mA
	MB 81461-15			100	
SAM ACTIVE $\overline{SE} = V_{IL}$, t_{SC} = min					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC7}		130	mA
	MB 81461-15			110	
STANDBY CURRENT Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	MB 81461-12	I_{CC8}		50	mA
	MB 81461-15			40	
REFRESH CURRENT 1* Average power supply current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC9}		112	mA
	MB 81461-15			95	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, t_{PC} = min)	MB 81461-12	I_{CC10}		85	mA
	MB 81461-15			70	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461-12	I_{CC11}		112	mA
	MB 81461-15			95	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC12}		145	mA
	MB 81461-15			125	

3

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, $V_{CC}=5.5V$, $V_{SS}=0V$, all other pins not under test=0V)	$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH}=-5mA/-2mA for DQi/SDi) Output low voltage (I_{OL}=4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1 2 3

Parameter NOTES	Symbol	MB 81461-12		BM 81461-15		Unit
		Min	Max	Min	Max	
Time between Refresh (RAM/SAM)	t_{REF}		4		4	ms
Random Read/Write Cycle Time	t_{RC}	230		260		ns
Read-Modify-Write Cycle Time	t_{RWC}	305		345		ns
Page Mode Cycle Time	t_{PC}	120		145		ns
Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	195		225		ns
Access Time from $\overline{RAS}$ 4 6	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$ 5 6	t_{CAC}		60		75	ns
Output Buffer Turn Off Delay	t_{OFF}	0	25	0	35	ns
Transition Time	t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90		100		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	120	60000	150	60000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	60		75		ns

AC CHARACTERISTICS

Parameter	Notes	Symbol	MB 81461-12 Min	MB 81461-12 Max	MB 81461-15 Min	MB 81461-15 Max	Unit
CAS Precharge Time (Normal cycle)		t_{CPN}	40		50		ns
CAS Precharge Time (Page mode only)		t_{CP}	50		60		ns
CAS Precharge Time (CAS-before-RAS)		t_{CPR}	25		30		ns
CAS Pulse Width		t_{CAS}	60	60000	75	60000	ns
CAS Hold Time		t_{CSH}	120		150		ns
RAS to CAS Delay Time	7 8	t_{RCD}	22	60	25	75	ns
CAS to RAS Set Up Time		t_{CRS}	10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		ns
Column Address Hold Time		t_{CAH}	20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to RAS	9	t_{RRH}	20		20		ns
Read Command Hold Time Referenced to CAS	9	t_{RCH}	0		0		ns
Write Command Set Up Time		t_{WCS}	-5		-5		ns
Write Command Hold Time		t_{WCH}	30		35		ns
Write Command Pulse Width		t_{WP}	30		35		ns
Write Command to RAS Lead Time		t_{RWL}	40		45		ns
Write Command to CAS Lead Time		t_{CWL}	40		45		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	30		35		ns
Access Time from TR/OE	6	t_{OEA}		35		40	ns
TR/OE to Data In Delay Time		t_{OED}	25		30		ns

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AC CHARACTERISTICS

Parameter NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
		Min	Max	Min	Max	
Output Buffer Turn Off Delay from $\overline{TR}/\overline{OE}$	t_{OEZ}	0	25	0	30	ns
$\overline{TR}/\overline{OE}$ Hold Time Referenced to $\overline{ME}/\overline{WE}$	t_{OEH}	0		0		ns
$\overline{TR}/\overline{OE}$ to $\overline{RAS}$ inactive Set Up Time	t_{OES}	0		0		ns
Data In to $\overline{CAS}$ Delay Time 16	t_{DZC}	0		0		ns
Data In to $\overline{TR}/\overline{OE}$ Delay Time 16	t_{DZO}	0		0		ns
Refresh Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCS}	25		30		ns
Refresh Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCH}	25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{RPC}	20		20		ns
Serial Clock Cycle Time	t_{SC}	40	50000	60	50000	ns
Access Time from SAS 10	t_{SAC}		40		60	ns
Access Time from $\overline{SE}$ 10	t_{SEA}		40		50	ns
SAS Precharge Time	t_{SP}	10		20		ns
SAS Pulse Width	t_{SAS}	10		20		ns
$\overline{SE}$ Precharge Time	t_{SEP}	25		45		ns
$\overline{SE}$ Pulse Width	t_{SE}	25		45		ns
Serial Data Out Hold Time after SAS High	t_{SOH}	10		10		ns
Serial Output Buffer Turn Off Delay from $\overline{SE}$	t_{SEZ}	0	25	0	30	ns
Serial Data In Set Up Time 11	t_{SDS}	0		0		ns
Serial Data In Hold Time 11	t_{SDH}	20		25		ns

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AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12 Min	MB 81461-12 Max	MB 81461-15 Min	MB 81461-15 Max	Unit
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{TS}	0		0		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{RTH}	90		110		ns
Write Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time	12	t_{RTHW}	12		15		ns
Transfer Command ($\overline{TR}$) to $\overline{CAS}$ Hold Time		t_{CTH}	30		35		ns
Transfer Command ($\overline{TR}$) to SAS Lead Time		t_{TSL}	5		10		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Lead Time		t_{TRL}	130		140		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Delay Time		t_{TRD}	−65		−50		ns
First SAS Edge to Transfer Command Delay Time		t_{TSD}	25		35		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Set Up Time		t_{WSR}	0		0		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Hold Time		t_{RWH}	12		15		ns
Mask Data (MD) to $\overline{RAS}$ Set Up Time		t_{MS}	0		0		ns
Mask Data (MD) to $\overline{RAS}$ Hold Time		t_{MH}	35		45		ns
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	12	t_{SDZ}	10	60	10	75	ns
Serial Output Buffer Turn On Delay from $\overline{RAS}$	13	t_{SRO}	0		0		ns
SAS to $\overline{RAS}$ Set Up Time	11	t_{SRS}	40		60		ns
$\overline{RAS}$ to SAS Delay Time	12	t_{SRD}	30		45		ns
Serial Data Input to $\overline{SE}$ Delay Time		t_{SZE}	0		0		ns
Serial Data Input Delay from $\overline{RAS}$	12	t_{SDD}	60		75		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Serial Data Input to $\overline{RAS}$ Delay Time	13	t_{SZS}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Set up Time	14	t_{ESR}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	14	t_{REH}	12		15		ns
Serial Write Enable Set up Time	11	t_{SWS}	20		30		ns
Serial Write Enable Hold Time	11	t_{SWH}	80		120		ns
Serial Write Disable Set Up Time	11	t_{SWIS}	20		30		ns
Serial Write Disable Hold Time	11	t_{SWIH}	40		60		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{YS}	0		0		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{YH}	12		15		ns
Time between Transfer	15	t_{REFT}		4		4	ms

NOTES;

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 transfer, and 8 SAS cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycle are required
2. AC characteristics assume
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Measured with a load equivalent to 2 TTL loads and 50pF.
11. Input mode only
12. Write transfer and pseuso write transfer only.
13. Read transfer only in the case that the previous transfer was write transfer.
14. Pseudo write transfer only.
15. If t_{REFT} is not satisfied, 8 transfer and 8 SAS cycles before proper device operation is needed.
16. Either t_{DZC} or t_{DZO} must be satisfied.

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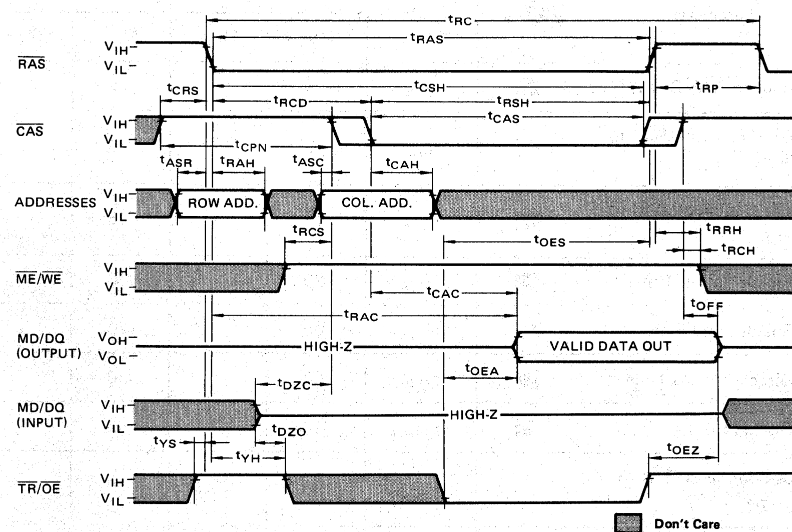
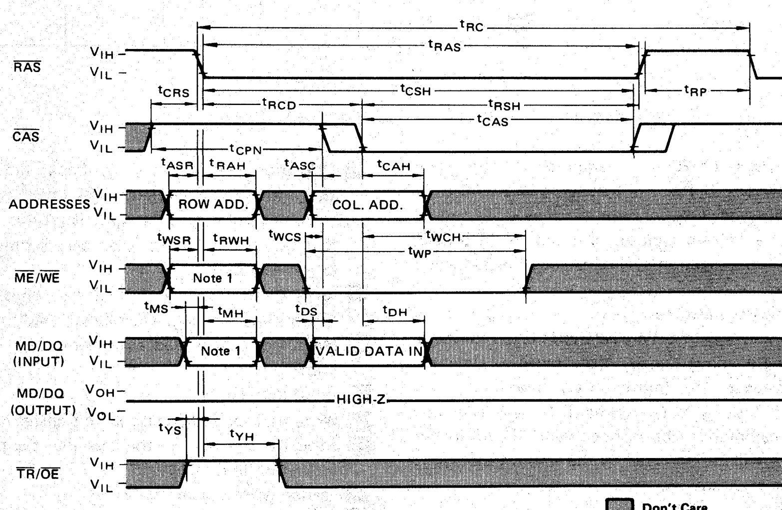
READ CYCLE

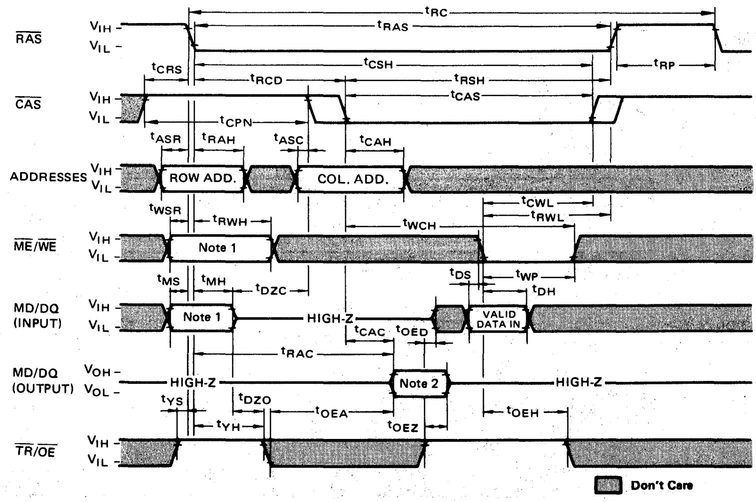


WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

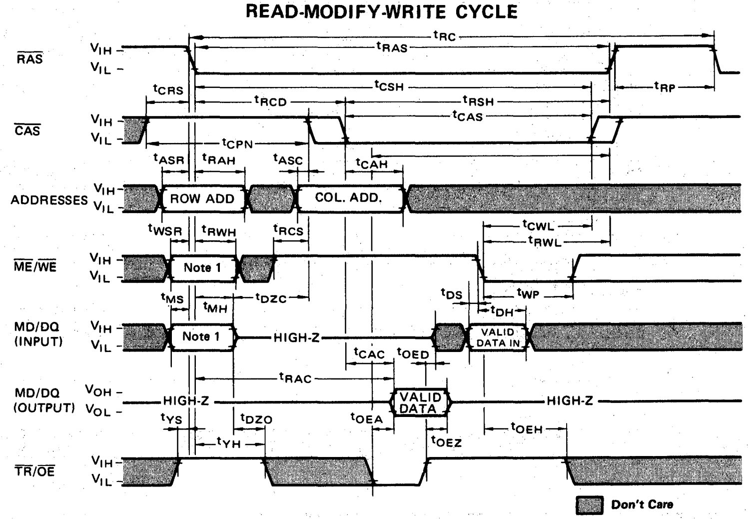
DELAYED WRITE CYCLE



Note 1) When ME/WE = "H", all data on the MD/DQ can be written into the cell.
When ME/WE = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of RAS.

Note 2) When TR/OE is kept "H" through a cycle, the MD/DQ are kept High-Z state.

READ-MODIFY-WRITE CYCLE



Note 1) When ME/WE = "H", all data on the MD/DQ can be written into the cell.
When ME/WE = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of RAS.

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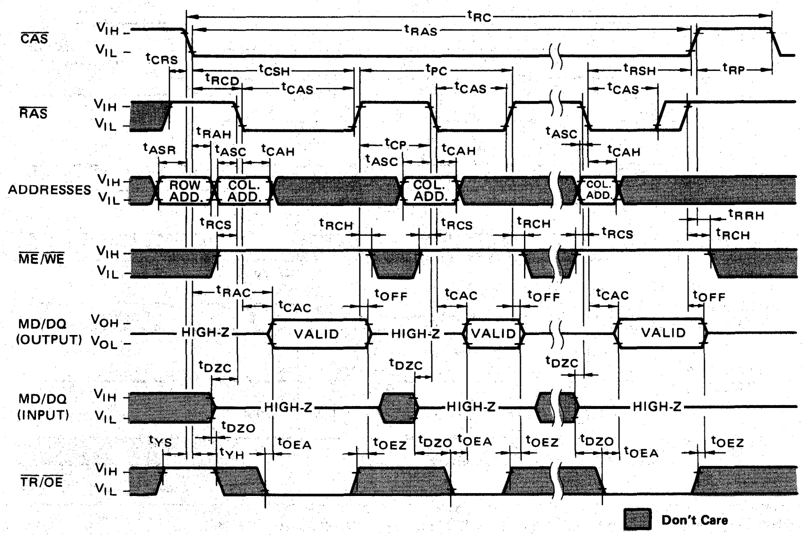
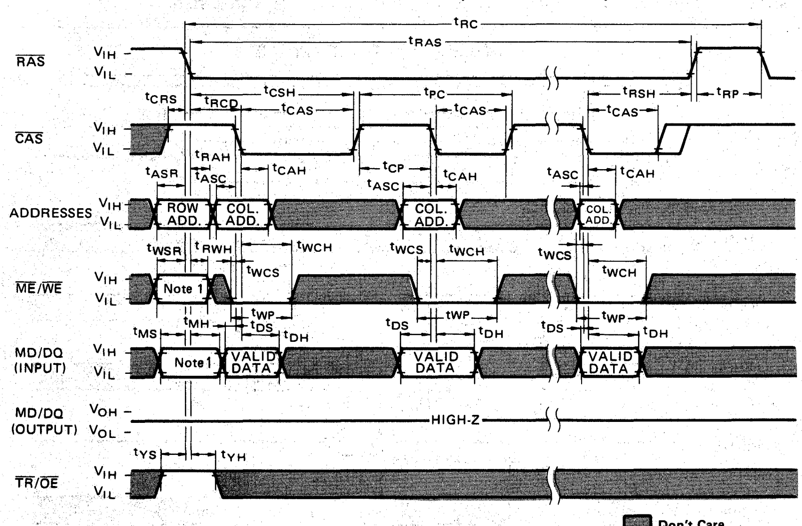
PAGE MODE READ CYCLE

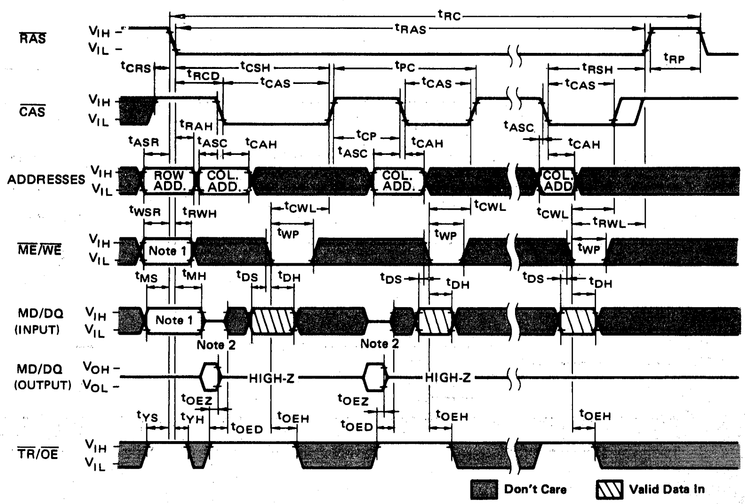


PAGE MODE WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

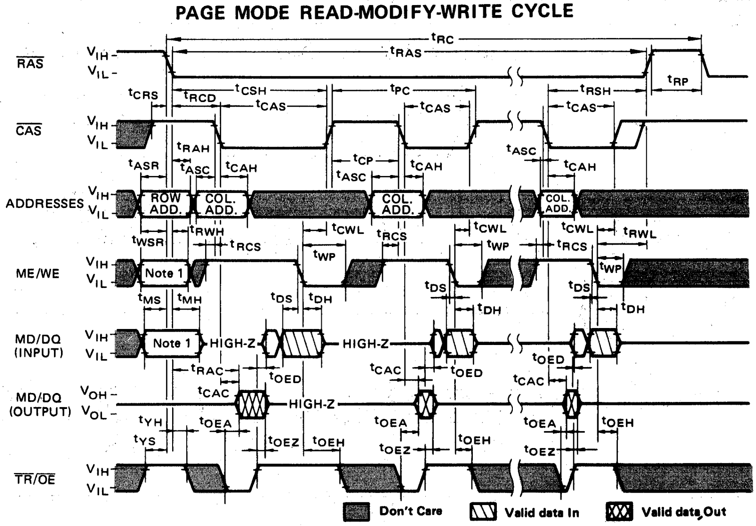
PAGE MODE DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

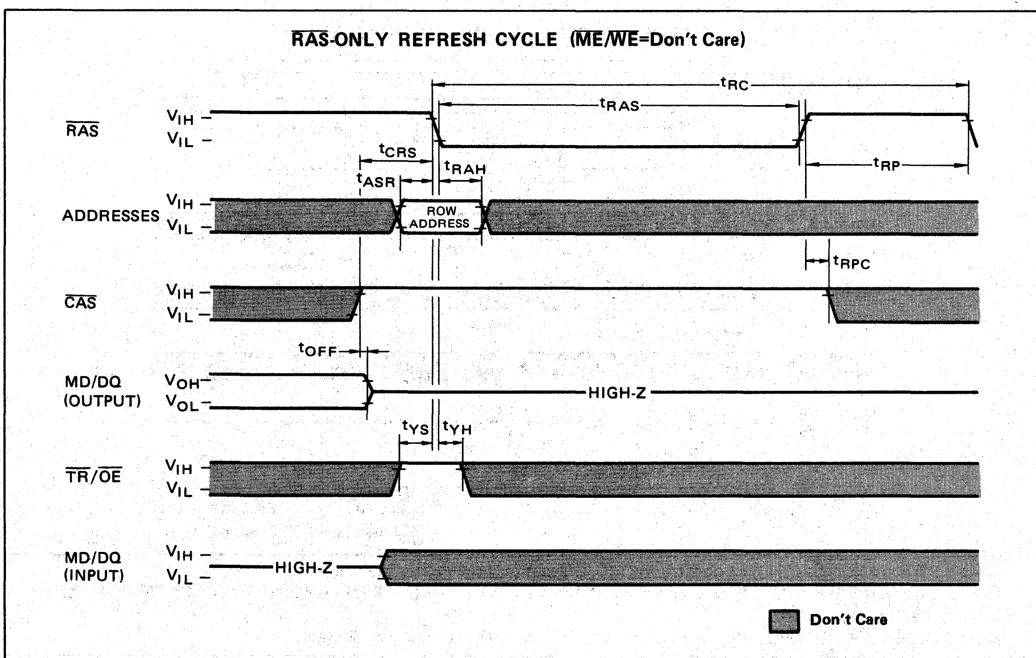
Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

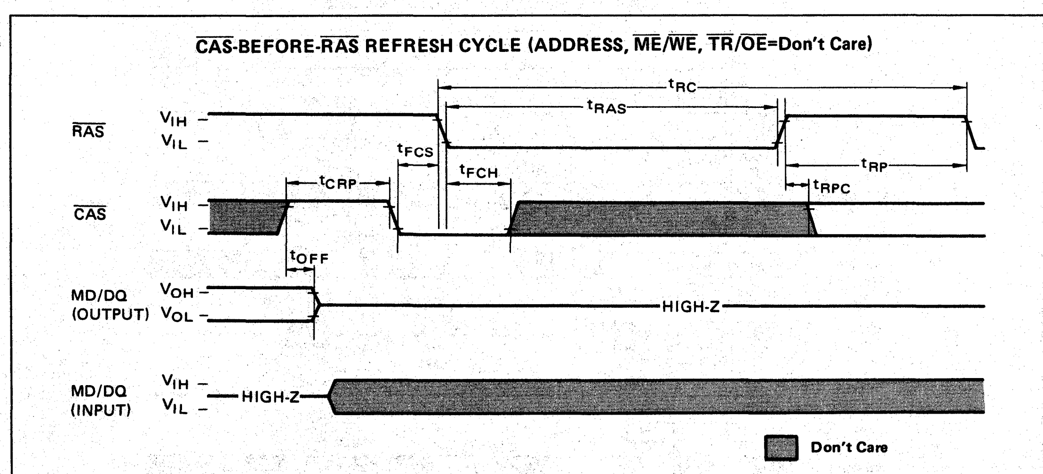
PAGE MODE READ-MODIFY-WRITE CYCLE



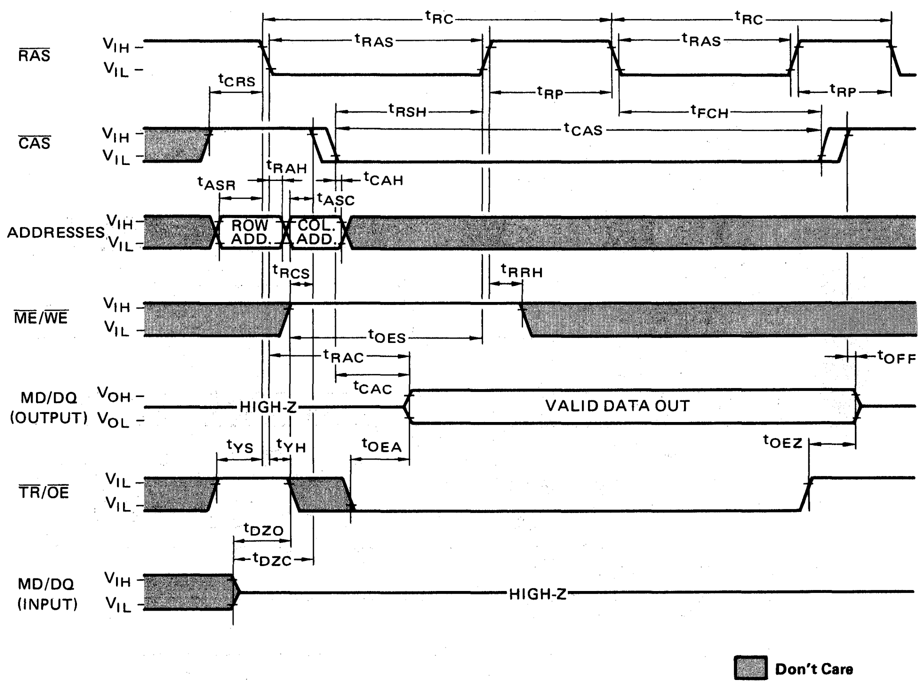
Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

3


RAS-ONLY REFRESH CYCLE (ME/WE=Don't Care)
tRC
tRAS
RAS
VIH
VIL
tCRS
tRAH
tASR
tRP
ADDRESSES
ROW ADDRESS
tRPC
CAS
tOFF
MD/DQ (OUTPUT)
VOH
VOL
HIGH-Z
tYS
tYH
TR/OE
MD/DQ (INPUT)
HIGH-Z
Don't Care


CAS-BEFORE-RAS REFRESH CYCLE (ADDRESS, ME/WE, TR/OE=Don't Care)
tRC
tRAS
RAS
VIH
VIL
tFCS
tRP
tFCH
tCRP
tRPC
CAS
tOFF
MD/DQ (OUTPUT)
VOH
VOL
HIGH-Z
MD/DQ (INPUT)
HIGH-Z
Don't Care

HIDDEN REFRESH CYCLE



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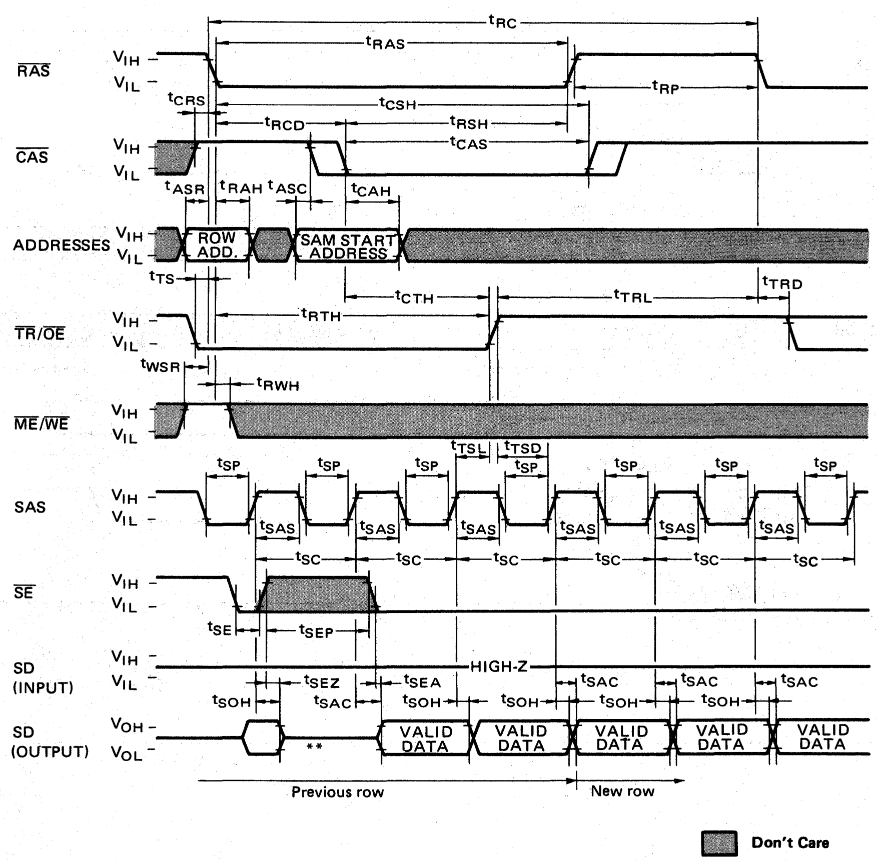
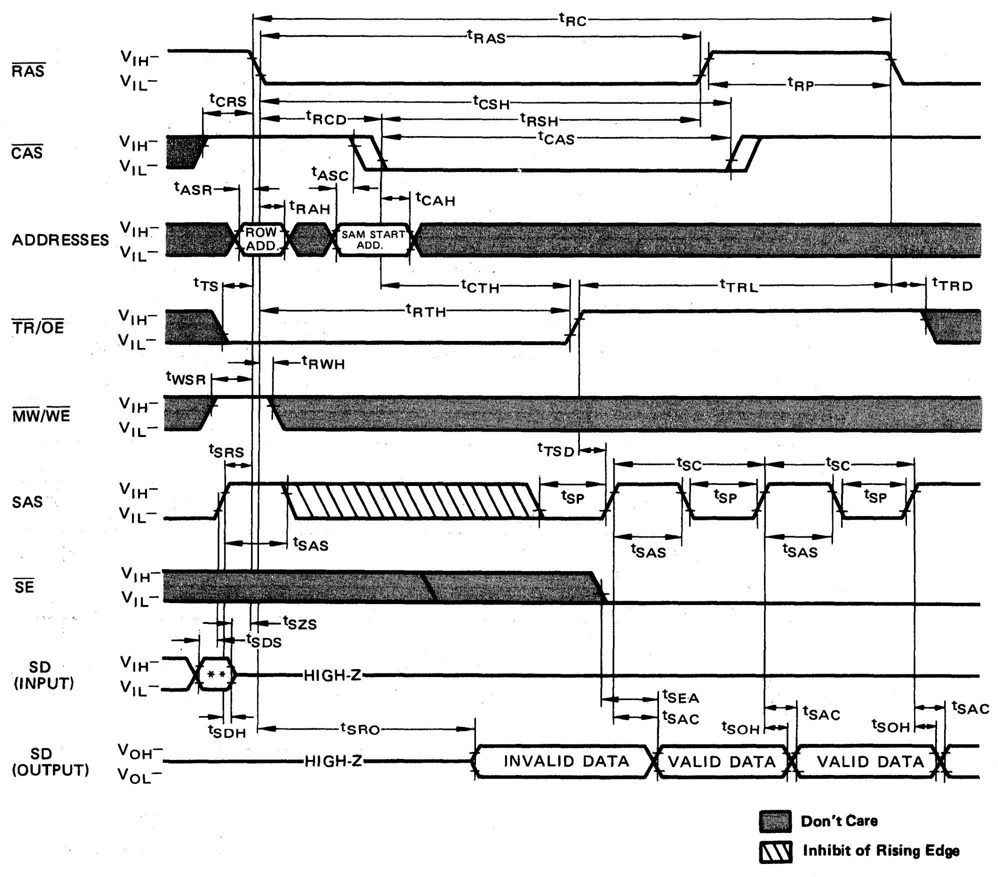
READ TRANSFER CYCLE* (MD/DQ = Don't Care)



*: In the case that the previous transfer is read transfer.
**: If $\overline{SE}$ is low, the valid data will appear within t_{SAC} or t_{SEA}.

READ TRANSFER CYCLE* (MD/DQ = Don't Care)



*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is low and the previous cycle is serial write cycle, this should be valid data input.

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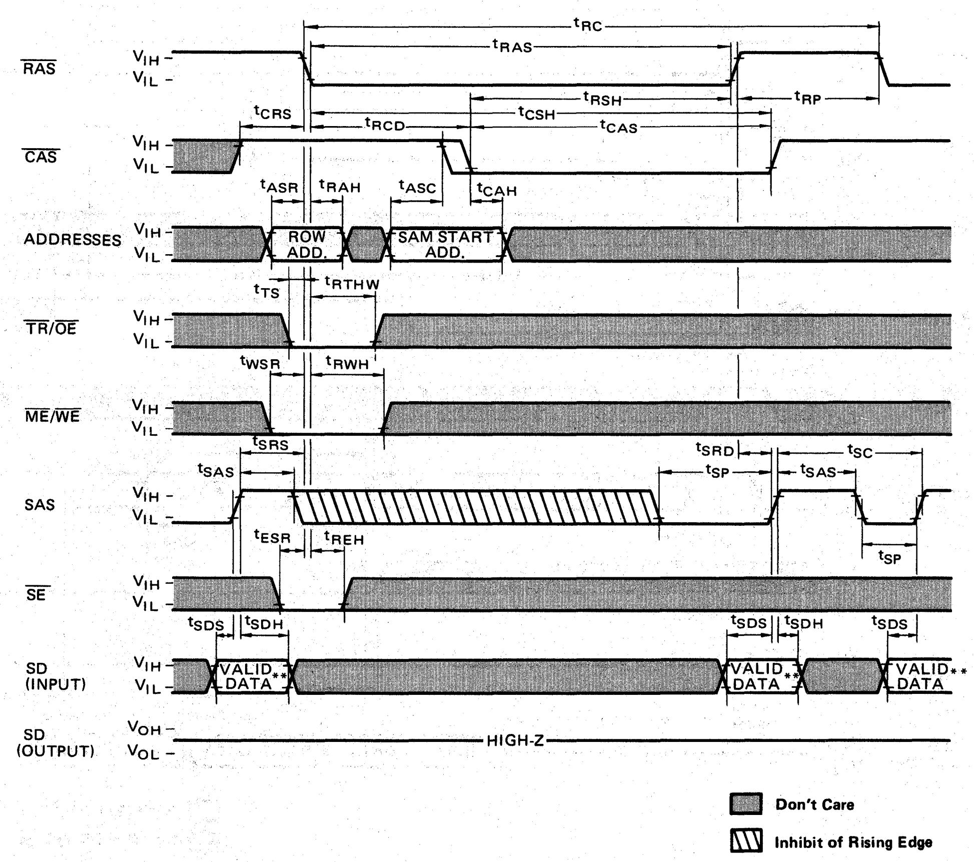
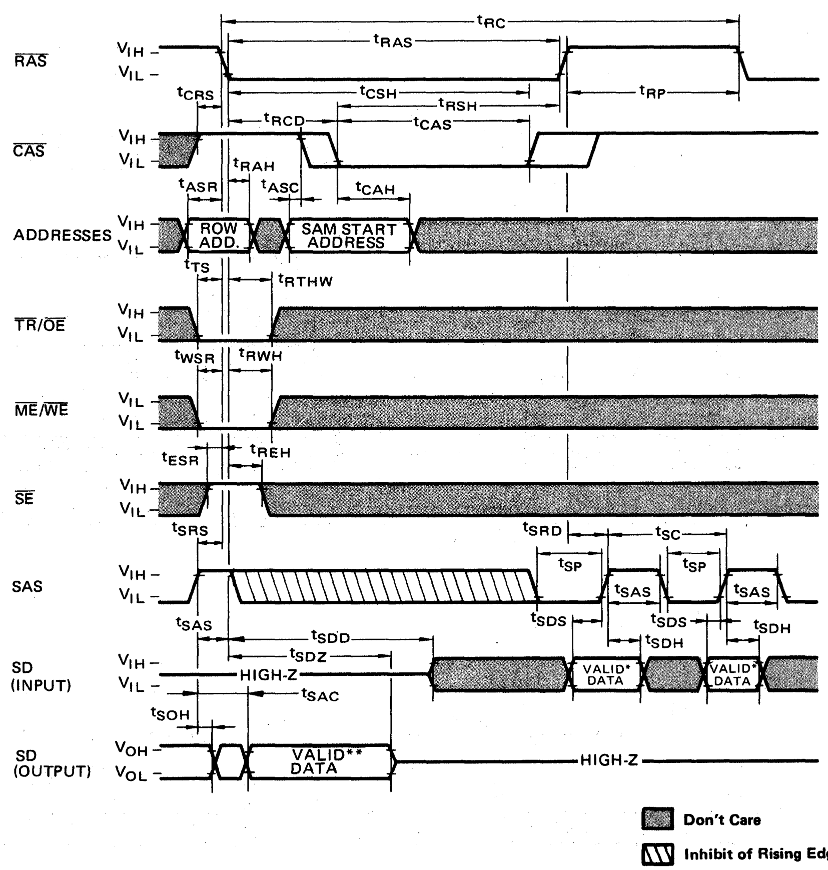
WRITE TRANSFER CYCLE* (MD/DQ = Don't Care)



*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is high these data are not written into the SAM.

PSEUDO WRITE TRANSFER CYCLE (MD/ DQ = Don't Care)



*: If $\overline{SE}$ is high, these data are not written into SAM.
**: If $\overline{SE}$ is high, SD (SD0 to SD3) are in High-Z state after t_{SEZ}.
If $\overline{SE}$ becomes low, the valid data will appear meeting t_{SAC} and t_{SEA}.

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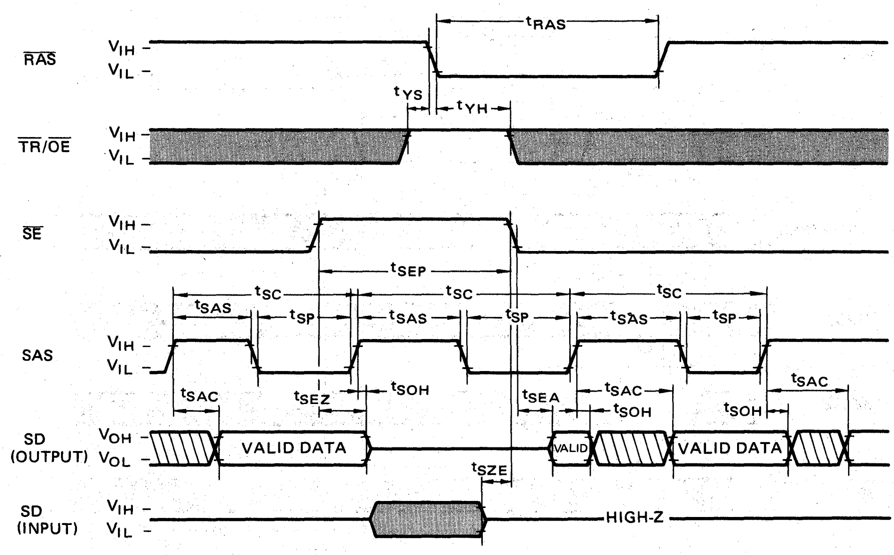
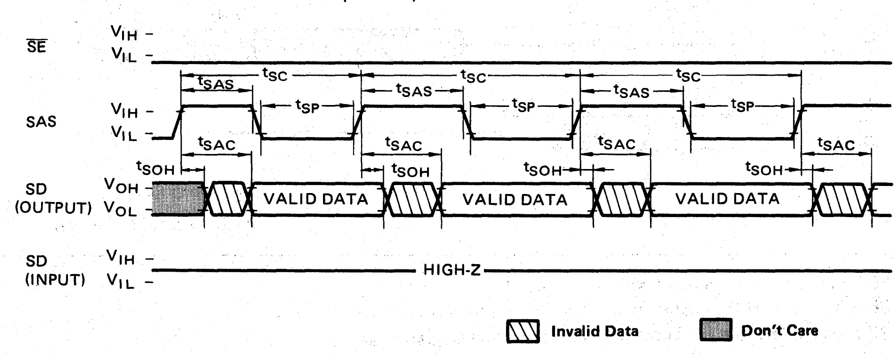
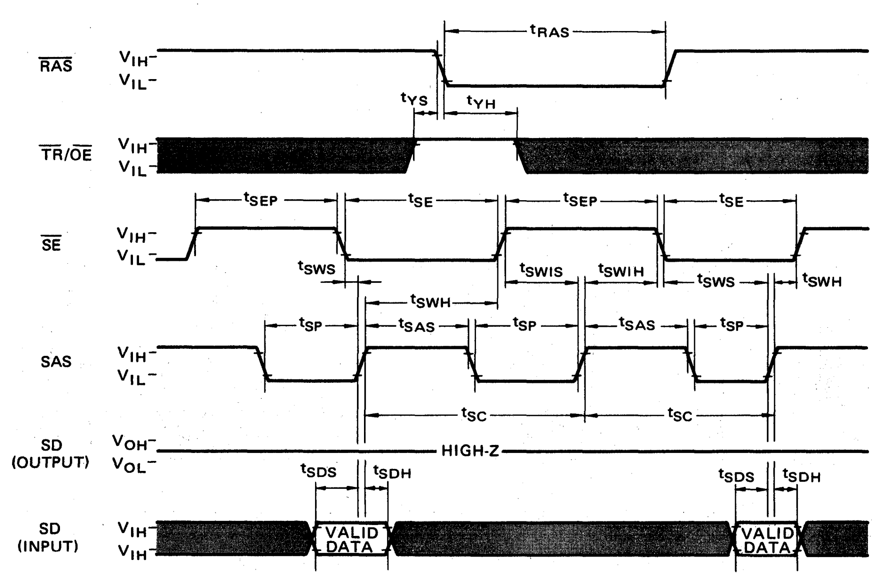
SERIAL READ CYCLE



In the case of $\overline{SE}$="L" while the operation;



SERIAL WRITE CYCLE



In the case of $\overline{SE}$="L" while the operation;

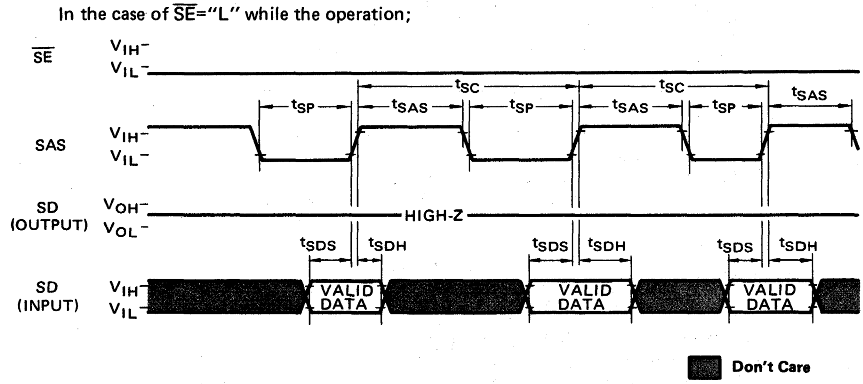


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Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

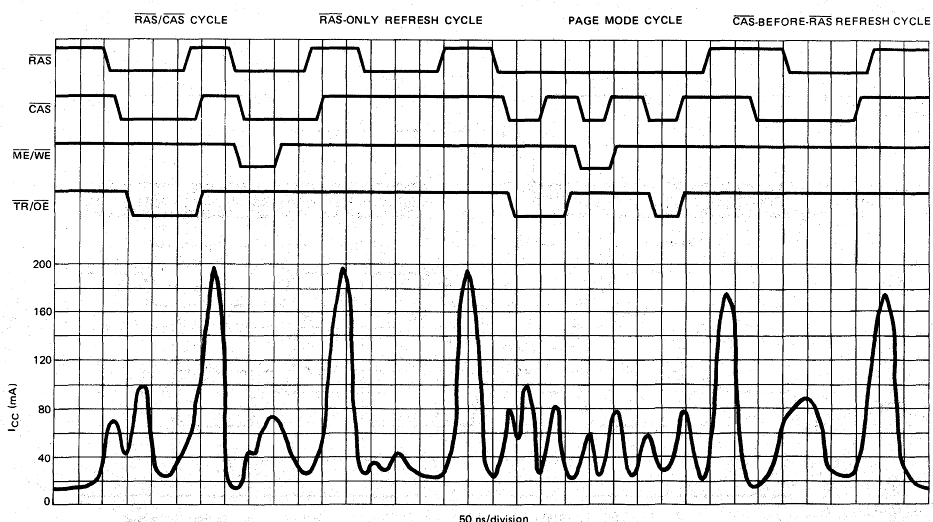
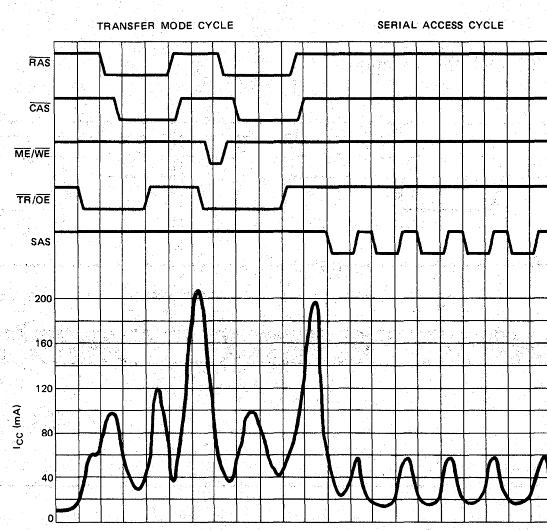


Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C) (cont'd)



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TYPICAL CHARACTERISTICS CURVES

Fig. 6 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

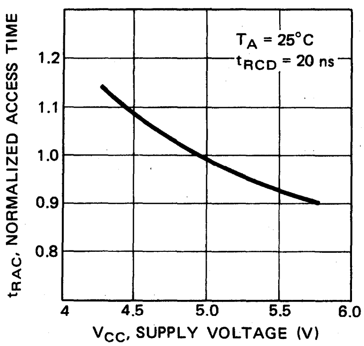

Fig. 7 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

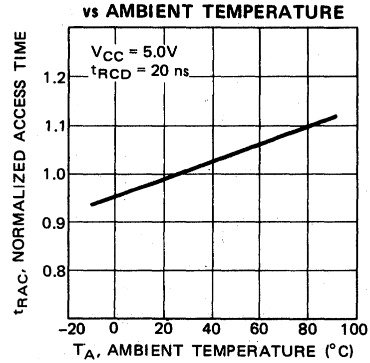

Fig. 8 – OPERATING CURRENT vs CYCLE RATE

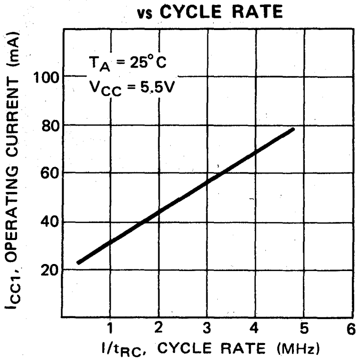

Fig. 9 – OPERATING CURRENT vs SUPPLY VOLTAGE

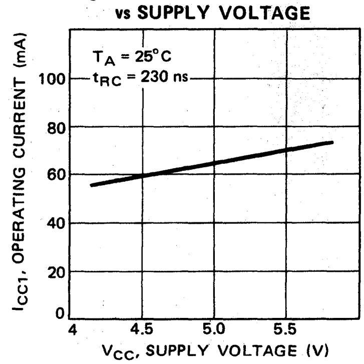

Fig. 10 – OPERATING CURRENT vs AMBIENT TEMPERATURE

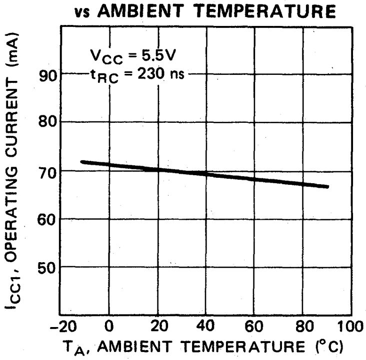

Fig. 11 – STANDBY SURRENT vs SUPPLY VOLTAGE

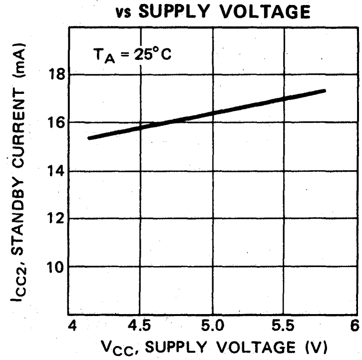

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Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

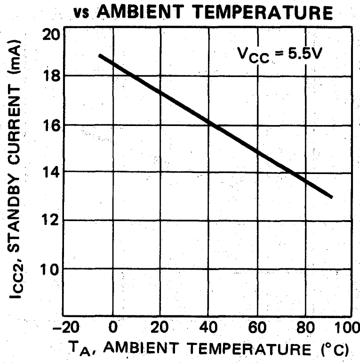

Fig. 13 – REFRESH CURRENT 1 vs CYCLE RATE

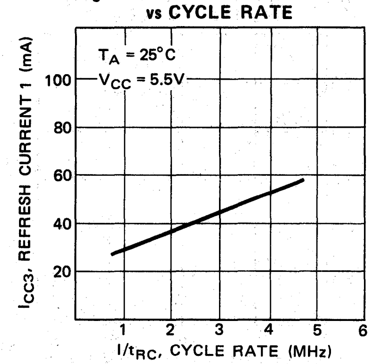

Fig. 14 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

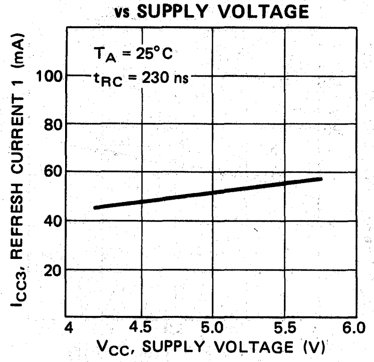

Fig. 15 – PAGE MODE CURRENT vs CYCLE RATE

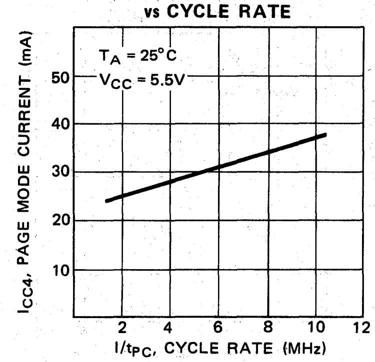

Fig. 16 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

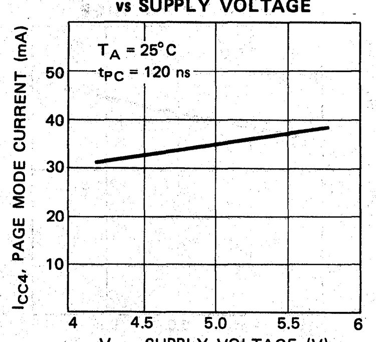

Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

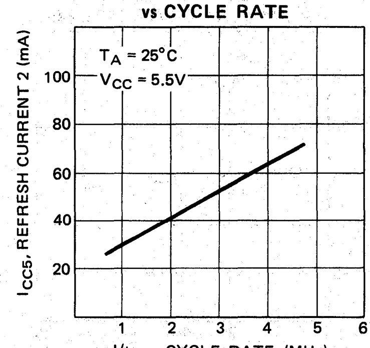

Fig. 18 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

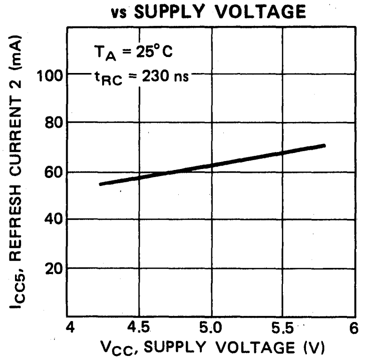

Fig. 19 – TRANSFER MODE CURRENT vs CYCLE RATE

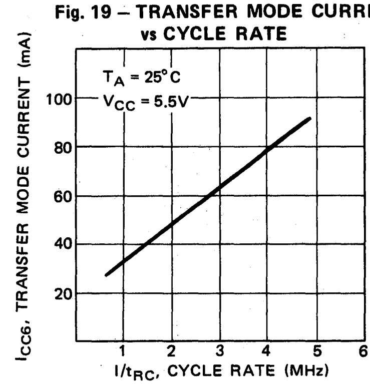

Fig. 20 – TRANSFER MODE CURRENT vs SUPPLY VOLTAGE

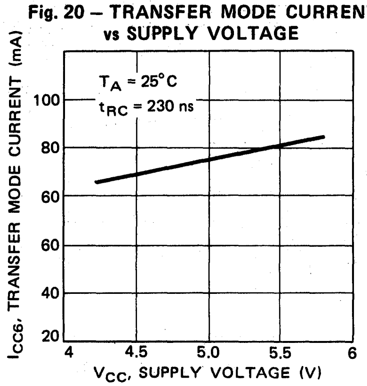

Fig. 21 – RAM STANDBY/SAM ACTIVE CURRENT vs CYCLE RATE

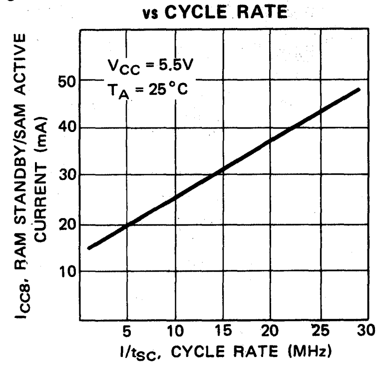

Fig. 22 – RAM STANDBY/SAM ACTIVE CURRENT vs SUPPLY VOLTAGE

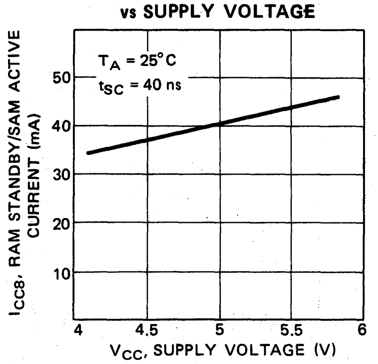

Fig. 23 – RAM STANDBY/SAM ACTIVE CURRENT vs AMBIENT TEMPERATURE

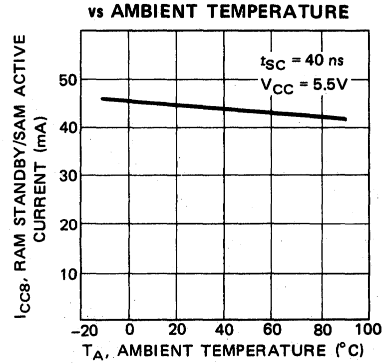

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Fig. 24 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

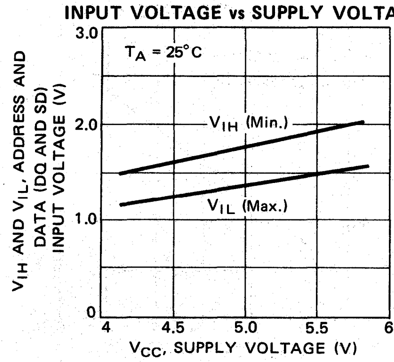


Fig. 25 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

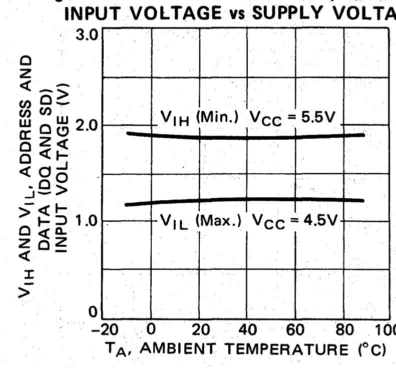


Fig. 26 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs SUPPLY VOLTAGE

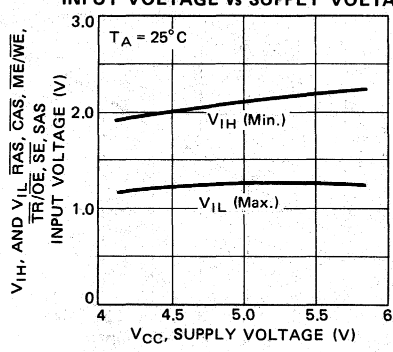


Fig. 27 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs AMBIENT TEMPERATURE

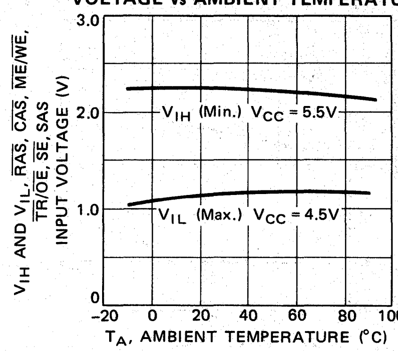


Fig. 28 – ACCESS TIME (RAM) vs LOAD CAPACITANCE

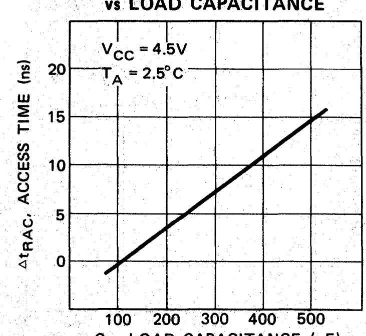


Fig. 29 – ACCESS TIME (SAM) vs LOAD CAPACITANCE

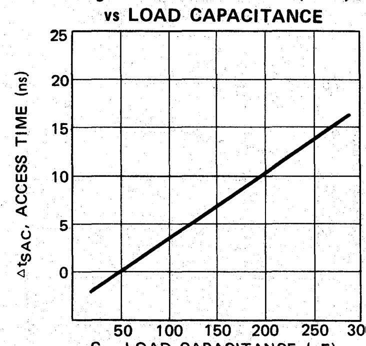


Fig. 30 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

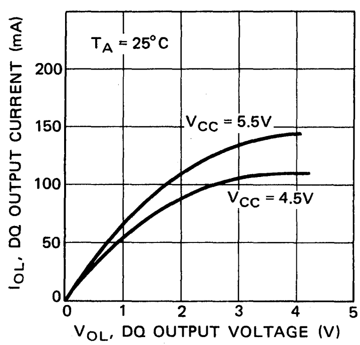


Fig. 31 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

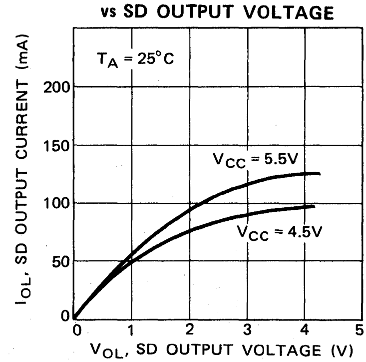


Fig. 32 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

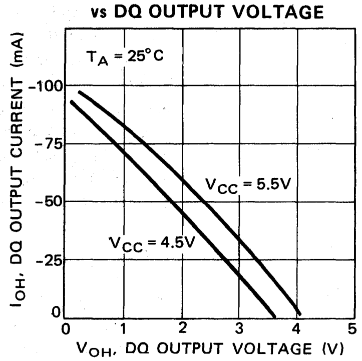


Fig. 33 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

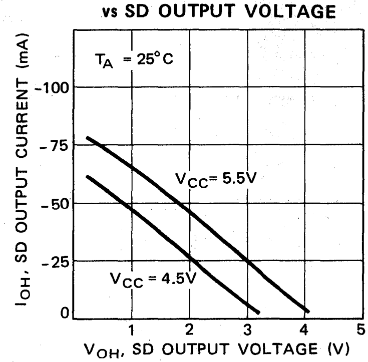
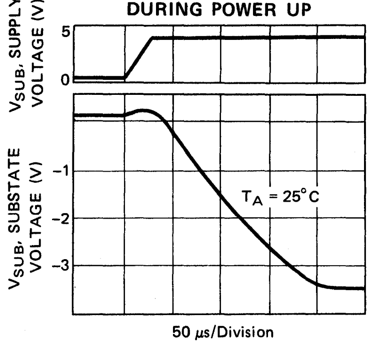


Fig. 34 – SUBSTRATE VOLTAGE DURING POWER UP

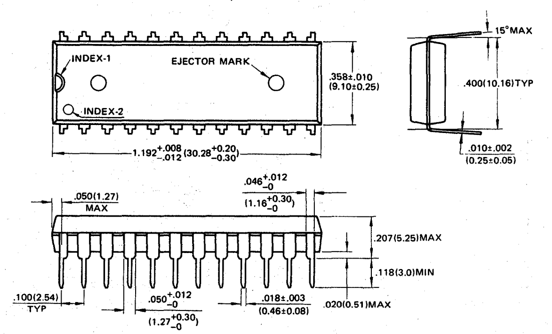


3

PACKAGE DIMENSIONS

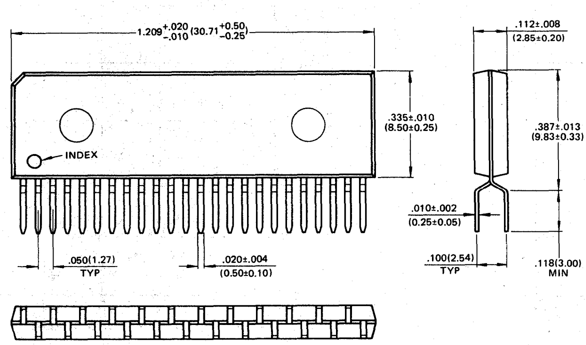
PLASTIC DIP (Suffix: -P) PLASTIC ZIP (Suffix: -PSZ)

24-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-24P-M04)



Dimensions in
inches (millimeters)

24-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-24P-M02)



Dimensions in
inches (millimeters)

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FUJITSU

262144-BIT DUAL PORT DYNAMIC RANDOM ACCESS MEMORY

MB81461B-12
MB81461B-15

July 1987
Edition 1.0

262, 144 BIT DUAL PORT DRAM

The Fujitsu MB 81461B is a fully decoded dual port NMOS dynamic random access memory organized as 65,536 words by 4 bits dynamic RAM port and 256 words by 4 bits serial access memory (SAM) port.

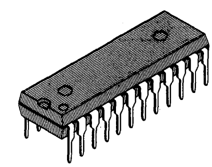
The DRAM port is identical to the Fujitsu MB 81464 with four bits parallel random access I/O while the SAM port is designed as four 256 bit registers each operating as a serial I/O. The four serial registers operate in parallel with each other during SAM port operation. Internal interconnects give the device the capability to transfer data bi-directionally between the DRAM memory array and the SAM data registers.

The MB 81461B offers complementely asynchronous access of both the DRAM and SAM ports except when data is transfered between them internally. The design is optimized for high speed and performance which makes the MB 81461B the most efficient solution for implementing the frame buffer of a bit mapped video display system. Multiplexed row and column address inputs permit the MB 81461B to be housed in a 400 mil wide 24 pin DIP and ZIP. Pin outs conformed to the JEDEC approved pin out.

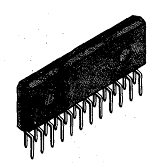
The MB 81461B is fabricated using silicon gate NMOS and Fujitsu's advanced Triple Layer Polysilicon process technology. This process coupled with single transistor memory storage cells permits maximum circuit density and minimum chip size. All inputs and outputs are TTL compatible.

Some of the transfer cycle timing specification are different from MB 81461.

- Dual port organization
  64K x 4 Dynamic RAM port (DRAM)
  256 x 4 Serial Access Memory port (SAM)
- 24 pin DIP and ZIP package
- Silicon-gate, Triple Poly NMOS, single transistor cell
- DRAM Port
  Access Time (t_{RAC}),
  120ns max. (MB 81461B-12)
  150ns max. (MB 81461B-15)
  Cycle Time (t_{RC}),
  230ns min. (MB 81461B-12)
  260ns min. (MB 81461B-15)
- SAM Port
  Access Time (t_{SAC}),
  40 ns max. (MB 81461B-12)
  60 ns max. (MB 81461B-15)
  Cycle Time (t_{SC}),
  40ns min. (MB 81461B-12)
  60ns min. (MB 81461B-15)
- Single +5V power supply, ±10% tolerance
- Power Dissipation
  DRAM; Act/SAM; Stby
  523mW max. (MB 81461B-12)
  468mW max. (MB 81461B-15)
  DRAM; Stby/SAM; Act
  275mW max. (MB 81461B-12)
  220mW max. (MB 81461B-15)
  DRAM; Stby/SAM; Stby
  110mW max.
- Bi-directional Data Transfer between DRAM and SAM
- Fast serial access asynchronous to DRAM except transfer operation
- Real Time Read Transfer Capability
- Page Mode capability
- Bit Masked Write Mode capability
- 256 refresh cycles every 4ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability
- Delayed write and Read-Modify-Write capability
- Standard 24 pin plastic DIP (Suffix; -P)
- Standard 24 pin plastic ZIP (Suffix; -PSZ)

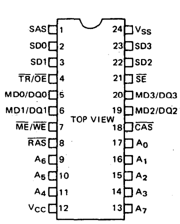


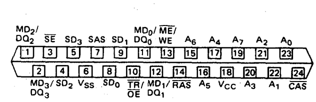
PLASTIC PACKAGE
DIP-24P-M04



PLASTIC PACKAGE
ZIP-24P-M02

PIN ASSIGNMENT





BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-1 to +7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit output current	—	50	mA

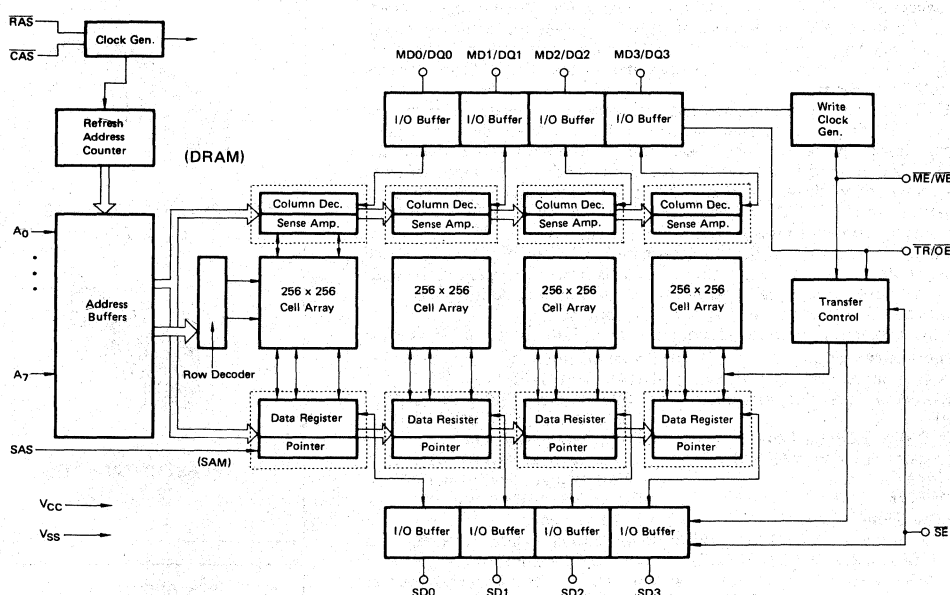
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 — BLOCK DIAGRAM OF MB 81461B and PIN DESCRIPTION

Block Diagram



Pin Description

Pin Number		Symbol	Parameter	Mode
DIP	ZIP			
1	7	SAS	Serial Access Memory Strobe	Input
2,3,22,23	8,9,4,5	SD0 to SD3	Serial Data I/O	I/O
4	10	$\overline{TR}/\overline{OE}$	Transfer Enable/ Output Enable	Input
5,6,19,20	11,12,1,2	MD0/DQ0 to MD3/DQ3	Mask Data/Data I/O	I/O
7	13	$\overline{ME}/\overline{WE}$	Mask Mode Enable/Write Enable	Input
8	14	$\overline{RAS}$	Row Address Strobe	Input
17, 16, 15 14, 11, 10 9, 13	23,22,21, 20,17,16, 15,19	A_0 to A_7	Address Input	Input
12	18	V_{CC}	Supply Voltage +5 V	Power Supply
18	24	$\overline{CAS}$	Column Address Strobe	Input
21	3	$\overline{SE}$	Serial port Enable	Input
24	6	V_{SS}	Ground	Power Supply

DESCRIPTION

DRAM OPERATION

$\overline{RAS}$;

This pin is used to strobe eight row-address inputs from A0 to A7 pins and is used to select the operation mode of subsequent cycle, such as DRAM operation or transfer operation (by $\overline{TR}/\overline{OE}$ and bit mask write cycle or not (by $\overline{ME}/\overline{WE}$ and MD0/DQ0 to MD3/DQ3). Since $\overline{RAS}$ = "L" is the active condition of circuit, to maintain $\overline{RAS}$ = "H" (standby condition) is effective to save power dissipation.

$\overline{CAS}$;

This pin is used to strobe eight column address inputs at the falling edge. $\overline{CAS}$ pin has the function to enable and disable the output at "L" and "H" respectively during the read operation.
Another function of $\overline{CAS}$ is to select "early write" mode conditioned by $\overline{ME}/\overline{WE}$ = "L".

$\overline{ME}/\overline{WE}$;

This pin is used to select read or write cycle. $\overline{ME}/\overline{WE}$ = "L" select write mode and $\overline{ME}/\overline{WE}$ = "H" select read mode. This pin is also used to enable bit mask write cycle. If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write is enabled.

$\overline{TR}/\overline{OE}$;

This pin is used to select Transfer operation or not at the falling edge of $\overline{RAS}$, $\overline{TR}/\overline{OE}$ = "H" enables DRAM operation and $\overline{TR}/\overline{OE}$ = "L" enables Transfer operation between DRAM and SAM. After the falling of $\overline{RAS}$ with t_{YH}, this pin is used for output enable.
The $\overline{TR}/\overline{OE}$ controls the impedance of the output buffers. $\overline{TR}/\overline{OE}$ = "H" forces the output buffers at high impedance state. $\overline{TR}/\overline{OE}$ = "L" leads the output buffers at low impedance state. But in early write cycle, the output buffers are high impedance state even if $\overline{TR}/\overline{OE}$ is low.

A0 to A7;

These are multiplexed address input pins and used to select 4 bits of 262,144 memory cell locations in parallel within the MB81461B The eight row address inputs are strobed by $\overline{RAS}$ and followed eight column address inputs are strobed by $\overline{CAS}$. These are used to select the start address of serial access memory also.

MD0/DQ0 to MD3/DQ3

These are common I/O pins of DRAM port. I/O mode is as specified for each function mode in the truth table.

Data Outputs:

The output buffers have three-state capability "H", "L" and "High-Z". To get valid output data on the pins, one of the read operations is selected such as "read" or "read-modify-write" mode. During a refresh cycle, either $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ mode is selected, output buffers are set in "High-Z" state.

Data inputs:

These are used as data input pins when a data write mode such as "Early-Write", "Delayed Write" or "Read-modify-Write" is selected. In any of the above cases, these pins are set at "High-Z" state to enable data-in without any bus conflict.
In any operation mode, read, write, refresh, transfer and their combined functions, output states "H", "L", "High-Z" are set by control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$ and/or $\overline{TR}/\overline{OE}$. When "Bit mask write" mode is set, these pins are used as a control signal for write inhibit with MDi/DQi = "L" on the selected bit i.

Page Mode;

The page mode operation is to strobe the column address by $\overline{CAS}$ while $\overline{RAS}$ is maintained at "L" through all the successive memory operations if the row address doesn't change. This mode can save power dissipation and get the faster access time due to the elimination of $\overline{RAS}$ falling edge function.

Refresh;

Refresh of the DRAM cells is performed for every 256 rows per every 4 milliseconds.
The MB81461B offers the following three types of refresh.

1) $\overline{RAS}$-Only refresh; The $\overline{RAS}$-Only refresh is performed with $\overline{CAS}$="H" condition. Strobing every 256 row addresses with $\overline{RAS}$ will complete all bits of memory cell to be refreshed while all outputs are invalid due to "High-Z" state. Further $\overline{RAS}$-only refresh saves the power dissipation substantially.
2) $\overline{CAS}$-before-$\overline{RAS}$ refresh; The $\overline{CAS}$-before-$\overline{RAS}$ refresh offers an alternate refresh method. If $\overline{CAS}$ is set low for the specified period (t_{FCS}) before the falling edge of $\overline{RAS}$, refresh control clock generator and refresh address counter are enabled, and an refresh operation is performed. After the refresh operation is performed, the refresh address counter is incremented automatically for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3) Hidden refresh; The hidden refresh is performed by maintaining the valid data of last read cycle at MD/DQ pins while extending $\overline{CAS}$ low. The hidden refresh is equivalent to $\overline{CAS}$-before-$\overline{RAS}$ refresh because $\overline{CAS}$ stays low when $\overline{RAS}$ goes to low in the next cycle.

Bit Mask Write;

This mode is used when some of the bits should be inhibited to be written into cells. The bit mask write mode is executed by setting $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$ during write mode (early, delayed write or read-modify-write cycle). The bits to be masked (or inhibited to write) is determined by MD/DQ state at the falling edge of $\overline{RAS}$, for example, if MD0/DQ0 and $\overline{ME}/\overline{WE}$ are both low at the falling edge of $\overline{RAS}$, the data on MD0/DQ0 pin is not written into the cell during the cycle. Refer to the Fig. 2.

EXAMPLE OF BIT MASK WRITE OPERATION

Falling edge of RAS						Function
TR/OE	ME/WE	MD0/DQ0	MD1/DQ1	MD2/DQ2	MD3/DQ3	
H	H	X	X	X	X	Write enable
	L	H	L	H	L	Write enable for DQ0 and DQ2 Write disable for DQ1 and DQ3

X: Don't Care

FUNCTIONAL TRUTH TABLE FOR DRAM OPERATION

RAS	CAS	ME/WE	TR/OE	ADDRESSES	MD0/DQ0 to MD3/DQ3	Function
H	H	X	X	X	X	Standby
L	L	H	H→L	Valid	Valid Data Out	Read
L	L	L*	H→X	Valid	Valid Data In	Early Write
L	L	H→L	H → X → H	Valid	Valid Data In	Delayed Write
L	L	H→L	H→L→H	Valid	Valid Data Out → Valid Data In	Read-Modify-Write
L	H	X	H→X	Row address	High-Z	RAS-Only Refresh
H→L	L	X	H→X	X	High-Z	CAS-before-RAS Refresh

*: If ME/WE = "L" at the falling edge of RAS, bit mask write mode is enabled.

TRANSFER OPERATION:

The transfer operation is featured in the MB 81461B. This mode is used to transfer simultaneously 256x4 data from DRAM to SAM or from SAM to DRAM. The direction of transfer is determined by the state of ME/WE at the falling edge of RAS. ME/WE="H" defines the transfer from DRAM to SAM (Read Transfer Cycle) and ME/WE="L" defines the transfer from SAM to DRAM (Write Transfer Cycle).

I/O mode of SD0 to SD3 determined while the transfer operation is set (TR/OE="L") conjunctioned with ME/WE state.

After Read Transfer Cycle, please apply two or more SAS Clock.

TR/OE;

This pin is used to enable transfer operation at the falling edge of RAS.

ME/WE;

This pin is used to select the direction of transfer at the falling edge of RAS.

A0 to A7;

These pins are used to select the row address of DRAM port to be transfered from or to, and the start address of SAM port for the serial read or write operation. The row address is strobed by RAS and the start address is strobed by CAS.

Pseudo Write Transfer:

To start serial write cycle, the SD pins must be set in input mode. To do this, write transfer cycle should be executed. The pseudo write transfer cycle is to change the SD pins into input mode without data transfer from SAM to DRAM. Refer to Fig. 3.

Refresh during transfer cycle;

DRAM and SAM are refreshed during transfer cycle as shown below.

1) Read transfer cycle:
   During read transfer cycle, the selected row address of DRAM to be transfered to SAM is refreshed. SAM data are kept by applying 256 SAS clocks within 4 ms after the read transfer cycle.
2) Write transfer cycle:
   During write transfer cycle, the new data are written from SAM to DRAM and this row address should be refreshed within 4 ms.
   But SAM data are not refreshed during write transfer cycle. Therefore, the SAM refresh (applying 256 SAS clocks within 4 ms) must be executed. Especially, when the write transfer cycle is executed continuously, 256 SAS clock should be applied within 4 ms.

SERIAL ACCESS OPERATION:

The MB 81461B has 256 words by 4 bits Serial Acess Memory (SAM) corresponding to 64K words by 4 bits DRAM and the fast serial read/write access is achieved by SAM architecture. Read or write cycle is determined when the last read or write transfer operation is executed. If the last transfer operation was read transfer, the serial read cycle is performed until the next write or pseudo write transfer cycle is executed. On the other hand, if the last transfer operation was write or pseudo write or pseudo write transfer, the serial write cycle is performed. In the serial write operation, 256 words by 4 bits data stored in the SAM can be transfered to DRAM under SE="L" condition, and SE="H" condition disables data transfer from SAM to DRAM. The serial access operation can be done asynchronously from DRAM port.

SAS;

This pin is used as a shift clock for SAM port. The serial access is triggered by the rising edge of SAS. In the write cycle, the data of the SD pins are strobed by the rising edge of SAS and written into the selected cell. In the read cycle, output data become valid after t_{SAC} from the rising edge of SAS and the data remain valid until the next cycle is defined. The SAS clock increments the SAM address automatically. When the SAM address exceeds #255 (Most Significant Address) it returnes to #0 (Least Significant Address).

$\overline{\text{SE}}$;
This pin is used to enable serial access operation by bit to bit. $\overline{\text{SE}}$ = "H" disables serial access operation. In the serial read operation, this pin is used for output enable, i.e., $\overline{\text{SE}}$ = "H" leads SD pins to "High-Z" state. $\overline{\text{SE}}$ = "L" leads SD pins to valid data with specified access time. In the serial write operation, this pin works as write enable control pin.

SD0 to SD3;
These are used as data input/output pins for SAM port. Input or output mode is determined by last occured transfer operation, if last transfer operation was read transfer mode, they are output mode. If the write transfer mode was set, SD pins are enabled to write data into SAM.

Refresh;
Since the SAM is constructed by dynamic circuitry, the refresh is necessary to maintain the data in it. The refresh of SAM must be done by 256 cycles of SAS clock/4ms in either output or input mode. $\overline{\text{SE}}$ = "H" allows refresh of SAM with SD pins at "High-Z" state.

Real Time Read Transfer;
This feature is applicable to obtain valid data continuously when row address is changed without any timing loss from the last bit of previous row to the first bit of new row. Data transfer from DRAM to SAM is triggered by rising edge of $\overline{\text{TR}}/\overline{\text{OE}}$ after the preparation of internal circuit for this operation, while SAM port can continue read operation asynchronously from the above mentioned internal move. Once $\overline{\text{TR}}/\overline{\text{OE}}$ returns to "H" with the restricted timing specification t_{TSL} and t_{TSD} refered to SAS clock, SD pins can get the valid output data continuously as shown in Fig. 4. The key issue to achieve this feature is to apply SAS clock continuously with the timing consideration to the rising edge of $\overline{\text{TR}}/\overline{\text{OE}}$.

FUNCTIONAL TRUTH TABLE FOR SERIAL ACCESS (Asynchronous from DRAM port)

Falling edge of $\overline{\text{RAS}}$		SAS	$\overline{\text{SE}}$	SD0 to SD3	Function
$\overline{\text{TR}}/\overline{\text{OE}}$	$\overline{\text{ME}}/\overline{\text{WE}}$				
H	X	Clock	L	Input/Output*	Sequential access enable
		Clock	H	Input/Output*	Sequential access disable

*: The read or write operation of SAM port is pre-determined by the last occurred transfer cycle. Input mode is for write operation. Output mode is for read operation.

X; Don't Care

Fig. 2 – EXAMPLE OF BIT MASK WRITE OPERATION

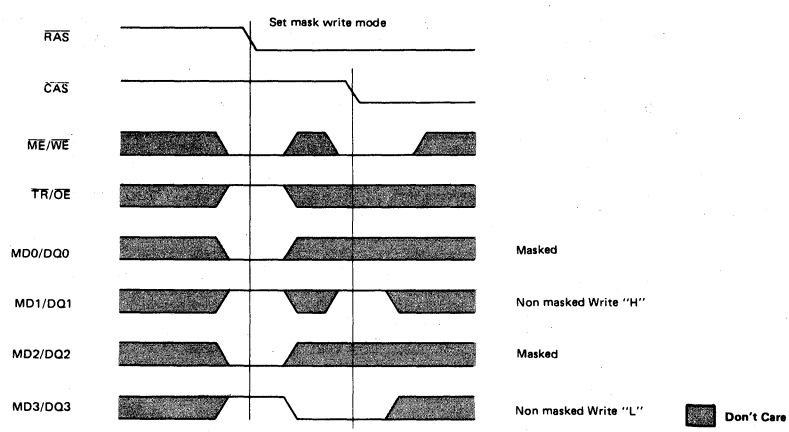


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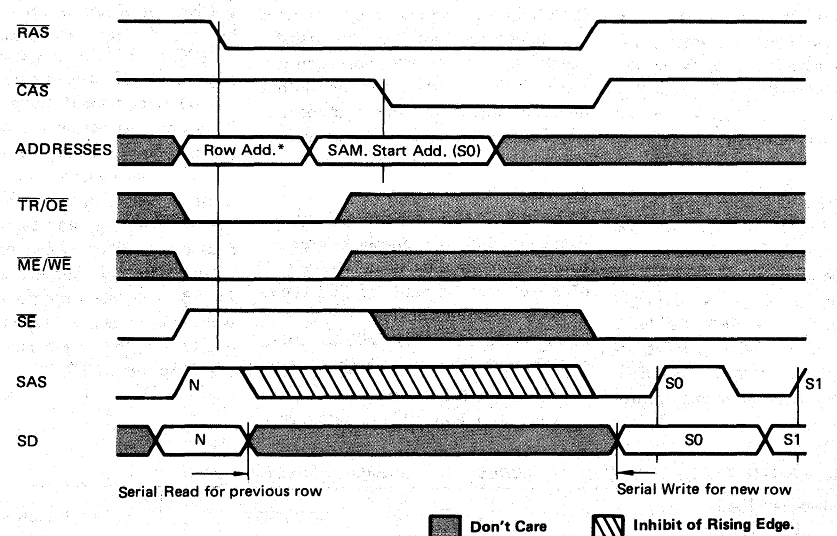
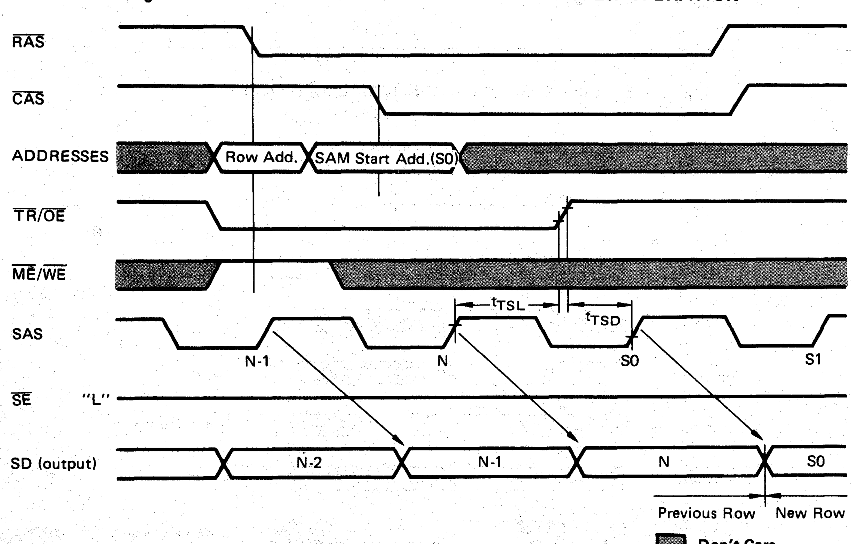
Fig. 3 — EXAMPLE OF PSEUDO WRITE TRANSFER CYCLE



*The DRAM data of this row address are refreshed during pseudo write transfer cycle.

Fig. 4 — EXAMPLE OF REAL TIME READ TRNASFER OPERATION



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RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

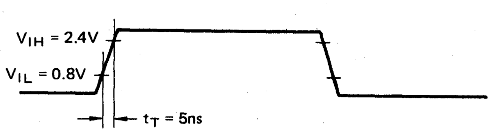
Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4		6.5	V	
Input Low Voltage	V_{IL}	-2.0		0.8	V	

CAPACITANCE (T_A=25°C)

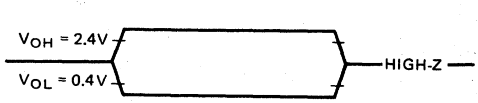
Paramter	Symbol	Typ	Max		Unit
			DIP	ZIP	
Input Capacitance (A0 to A7)	C_{IN1}		7	8	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{SE}$, $\overline{TR}/\overline{OE}$)	C_{IN2}		10	12	pF
Input Capacitance (SAS)	C_{IN3}		7	7	pF
Input/Output Capacitance (MD0/DQ0 to MD3/DQ3)	C_{IO1}		7	8	pF
Input/Output Capacitance (SD0 to SD3)	C_{IO2}		7	8	pF

AC TEST CONDITIONS

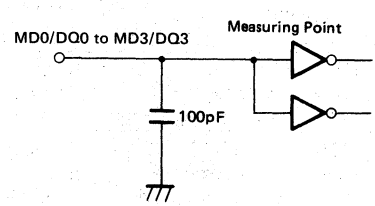
1) Input

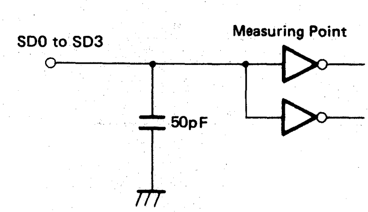


2) Output



3) Output Load





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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
SAM STANDBY $\overline{SE} = V_{IH}$, SAS = V_{IL}					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC1}		95	mA
	MB 81461B-15			85	
STANDBY CURRENT Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}		20	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC3}		77	mA
	MB 81461B-15			70	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = cycling, t_{PC} = min)	MB 81461B-12	I_{CC4}		50	mA
	MB 81461B-15			45	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461B-12	I_{CC5}		77	mA
	MB 81461B-15			70	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC6}		110	mA
	MB 81461B-15			100	
SAM ACTIVE $\overline{SE} = V_{IL}$, t_{SC} = min					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC7}		130	mA
	MB 81461B-15			110	
STANDBY CURRENT Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	MB 81461B-12	I_{CC8}		50	mA
	MB 81461B-15			40	
REFRESH CURRENT 1* Average power supply current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC9}		112	mA
	MB 81461B-15			95	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, t_{PC} = min)	MB 81461B-12	I_{CC10}		85	mA
	MB 81461B-15			70	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461B-12	I_{CC11}		112	mA
	MB 81461B-15			95	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC12}		145	mA
	MB 81461B-15			125	

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, $V_{CC}=5.5V$, $V_{SS}=0V$, all other pins not under test=0V)	$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH}=-5mA/-2mA for DQi/SDi) Output low voltage (I_{OL}=4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1 2 3

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Time between Refresh (RAM/SAM)		t_{REF}		4		4	ms
Random Read/Write Cycle Time		t_{RC}	230		260		ns
Read-Modify-Write Cycle Time		t_{RWC}	305		345		ns
Page Mode Cycle Time		t_{PC}	120		145		ns
Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	195		225		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	25	0	35	ns
Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	120	60000	150	60000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	60		75		ns

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AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
CAS Precharge Time (Normal cycle)		t_{CPN}	40		50		ns
CAS Precharge Time (Page mode only)		t_{CP}	50		60		ns
CAS Precharge Time (CAS-before-RAS)		t_{CPR}	25		30		ns
CAS Pulse Width		t_{CAS}	60	60000	75	60000	ns
CAS Hold Time		t_{CSH}	120		150		ns
RAS to CAS Delay Time	7 8	t_{RCD}	22	60	25	75	ns
CAS to RAS Set Up Time		t_{CRS}	10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		ns
Column Address Hold Time		t_{CAH}	20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to RAS	9	t_{RRH}	20		20		ns
Read Command Hold Time Referenced to CAS	9	t_{RCH}	0		0		ns
Write Command Set Up Time		t_{WCS}	-5		-5		ns
Write Command Hold Time		t_{WCH}	30		35		ns
Write Command Pulse Width		t_{WP}	30		35		ns
Write Command to RAS Lead Time		t_{RWL}	40		45		ns
Write Command to CAS Lead Time		t_{CWL}	40		45		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	30		35		ns
Access Time from TR/OE	6	t_{OEA}		35		40	ns
TR/OE to Data In Delay Time		t_{OED}	25		30		ns

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AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12 Min	MB 81461B-12 Max	MB 81461B-15 Min	MB 81461B-15 Max	Unit
Output Buffer Turn Off Delay from $\overline{TR}/\overline{OE}$		t_{OEZ}	0	25	0	30	ns
$\overline{TR}/\overline{OE}$ Hold Time Referenced to $\overline{ME}/\overline{WE}$		t_{OEH}	0		0		ns
$\overline{TR}/\overline{OE}$ to $\overline{RAS}$ inactive Set Up Time		t_{OES}	0		0		ns
Data In to $\overline{CAS}$ Delay Time	16	t_{DZC}	0		0		ns
Data In to $\overline{TR}/\overline{OE}$ Delay Time	16	t_{DZO}	0		0		ns
Refresh Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCS}	25		30		ns
Refresh Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCH}	25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	20		20		ns
Serial Clock Cycle Time		t_{SC}	40	50000	60	50000	ns
Access Time from SAS	10	t_{SAC}		40		60	ns
Access Time from $\overline{SE}$	10	t_{SEA}		40		50	ns
SAS Precharge Time		t_{SP}	10		20		ns
SAS Pulse Width		t_{SAS}	10		20		ns
$\overline{SE}$ Precharge Time		t_{SEP}	25		45		ns
$\overline{SE}$ Pulse Width		t_{SE}	25		45		ns
Serial Data Out Hold Time after SAS High		t_{SOH}	10		10		ns
Serial Output Buffer Turn Off Delay from $\overline{SE}$		t_{SEZ}	0	25	0	30	ns
Serial Data In Set Up Time	11	t_{SDS}	0		0		ns
Serial Data In Hold Time	11	t_{SDH}	20		25		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{TS}	0		0		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{RTH}	90		110		ns
Write Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time	12	t_{RTHW}	12		15		ns
Transfer Command ($\overline{TR}$) to $\overline{CAS}$ Hold Time		t_{CTH}	30		35		ns
Transfer Command ($\overline{TR}$) to SAS Lead Time		t_{TSL}	5		10		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Lead Time	17	t_{TRRL}	25		35		ns
Transfer Command ($\overline{TR}$) Hold Time from $\overline{RAS}$	17	t_{TRRH}	25		35		ns
First SAS Edge to Transfer Command Delay Time		t_{TSD}	25		35		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Set Up Time		t_{WSR}	0		0		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Hold Time		t_{RWH}	12		15		ns
Mask Data (MD) to $\overline{RAS}$ Set Up Time		t_{MS}	0		0		ns
Mask Data (MD) to $\overline{RAS}$ Hold Time		t_{MH}	35		45		ns
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	12	t_{SDZ}	10	60	10	75	ns
Serial Output Buffer Turn On Delay from $\overline{RAS}$	13	t_{SRO}	0		0		ns
SAS to $\overline{RAS}$ Set Up Time	11	t_{SRS}	40		60		ns
$\overline{RAS}$ to SAS Delay Time	12	t_{SRD}	30		45		ns
Serial Data Input to $\overline{SE}$ Delay Time		t_{SZE}	0		0		ns
Serial Data Input Delay from $\overline{RAS}$	12	t_{SDD}	60		75		ns

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AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Serial Data Input to $\overline{RAS}$ Delay Time	13	t_{SZS}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Set up Time	14	t_{ESR}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	14	t_{REH}	12		15		ns
Serial Write Enable Set up Time	11	t_{SWS}	20		30		ns
Serial Write Enable Hold Time	11	t_{SWH}	80		120		ns
Serial Write Disable Set Up Time	11	t_{SWIS}	20		30		ns
Serial Write Disable Hold Time	11	t_{SWIH}	40		60		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{YS}	0		0		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{YH}	12		15		ns
Time between Transfer	15	t_{REFT}		4		4	ms

NOTES:

1. An initial pause of 200μs is required after power-up followed by any 8 RAS, 8 transfer, and 8 SAS cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycle are required.
2. AC characteristics assume.
3. V_{IH} (min) and L_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Measured with a load equivalent to 2 TTL loads and 50pF.
11. Input mode only
12. Write transfer and pseuso write transfer only.
13. Read transfer only in the case that the previous transfer was write transfer.
14. Pseudo write transfer only.
15. If t_{REFT} is not satisfied, 8 transfer and 8 SAS cycles before proper device operation is needed.
16. Either t_{DZC} or t_{DZO} must be satisfied.
17. This timing specification is different from that of MB 81461.

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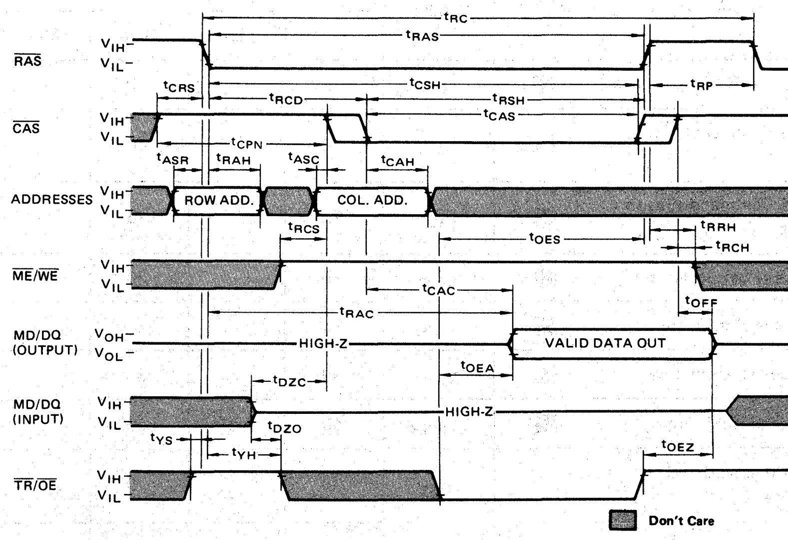
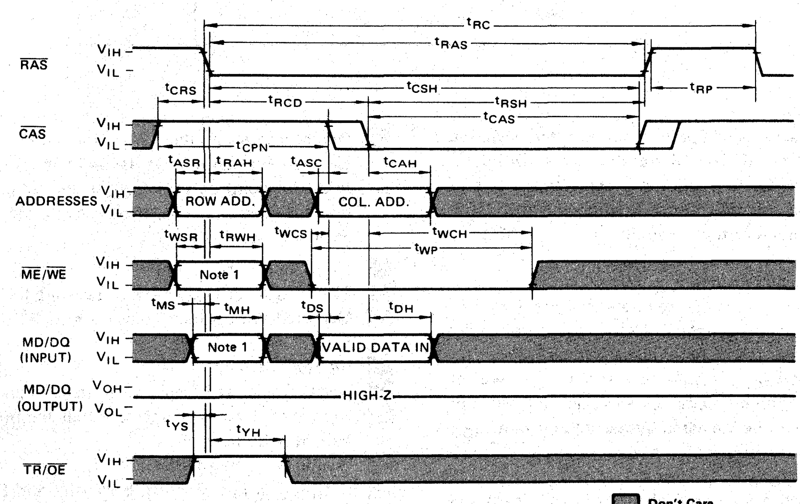
READ CYCLE

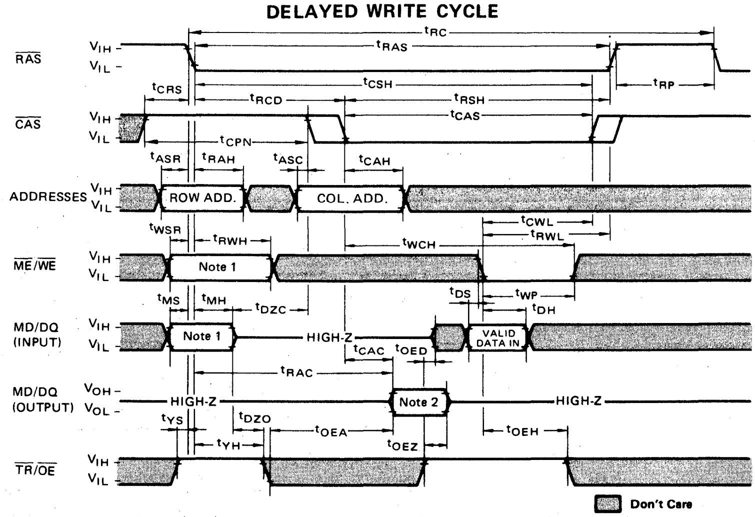


WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

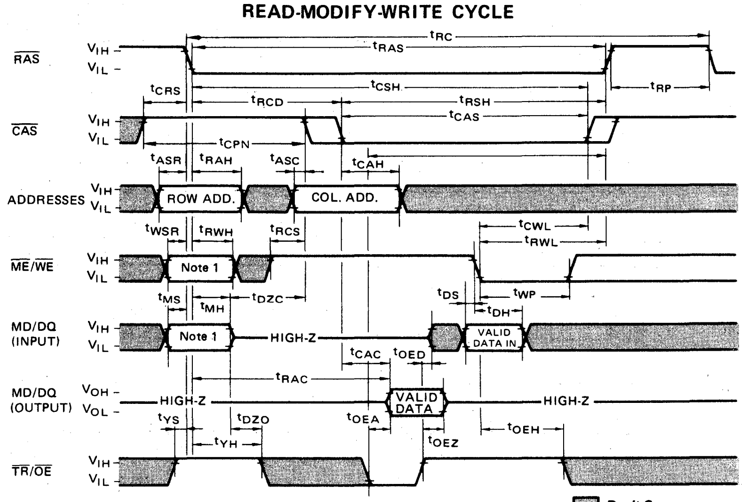
DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

READ-MODIFY-WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

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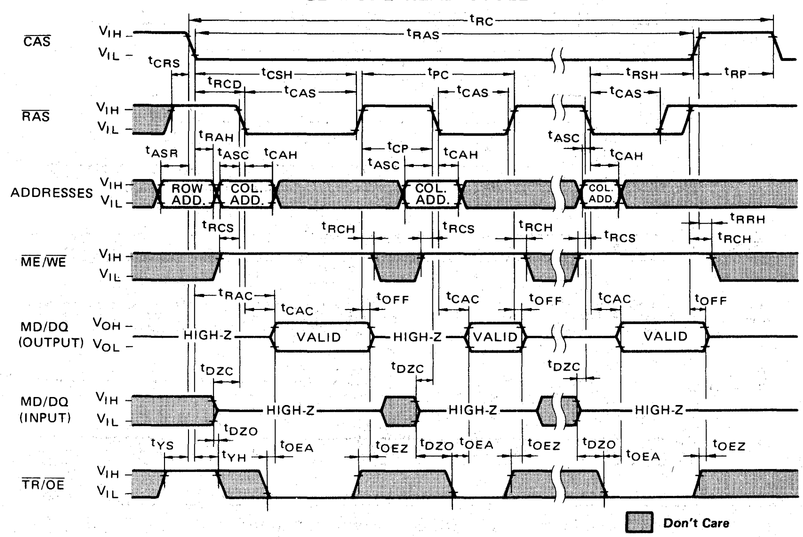
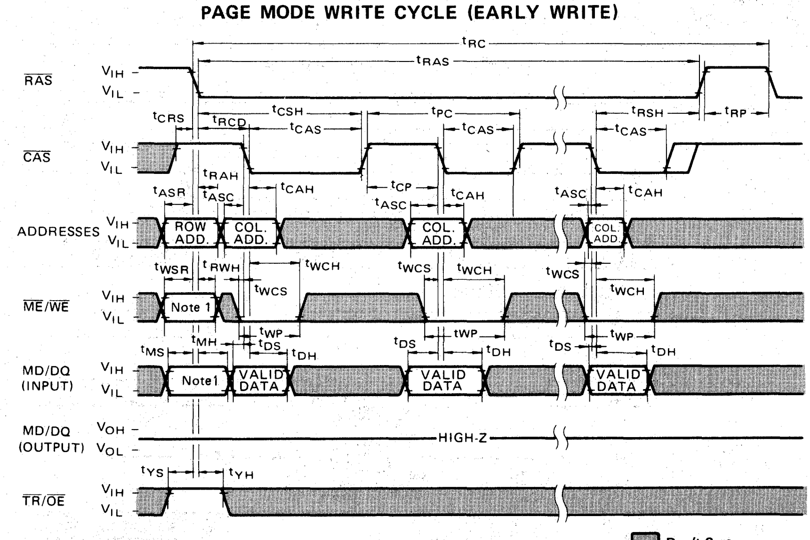
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

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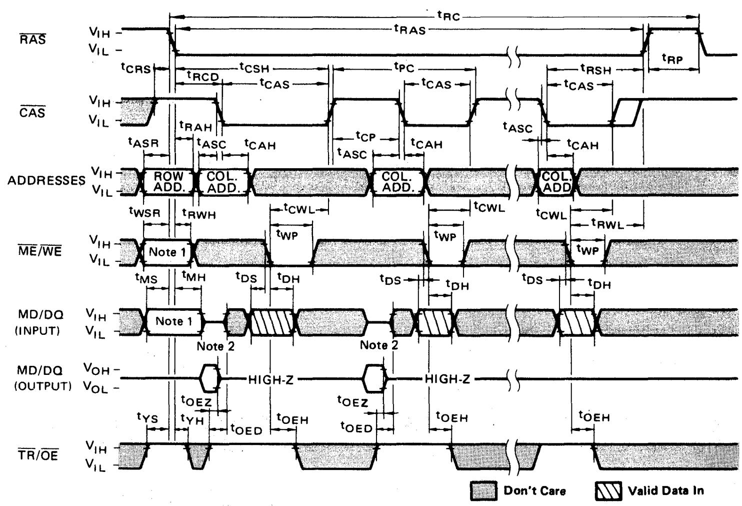
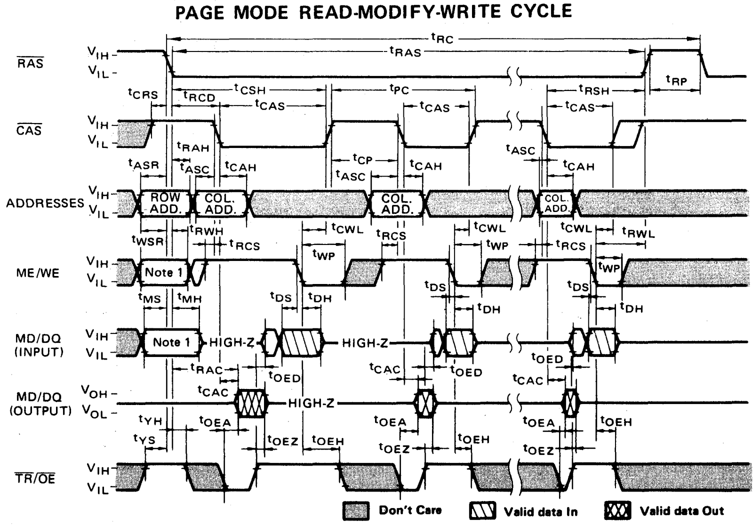
PAGE MODE DELAYED WRITE CYCLE



Note 1) When ME/WE = "H", all data on the MD/DQ can be written into the cell.
When ME/WE = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of RAS.

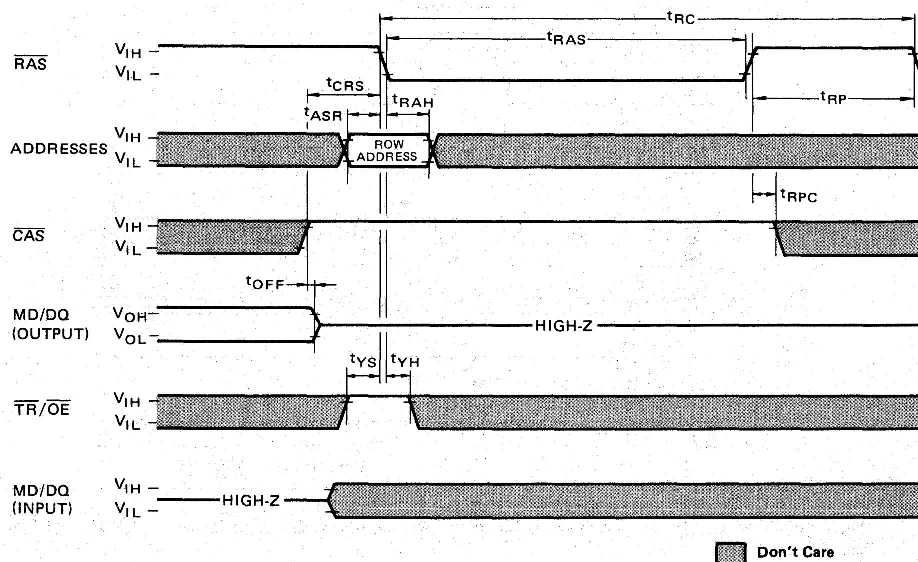
Note 2) When TR/OE is kept "H" through a cycle, the MD/DQ are kept High-Z state.

PAGE MODE READ-MODIFY-WRITE CYCLE

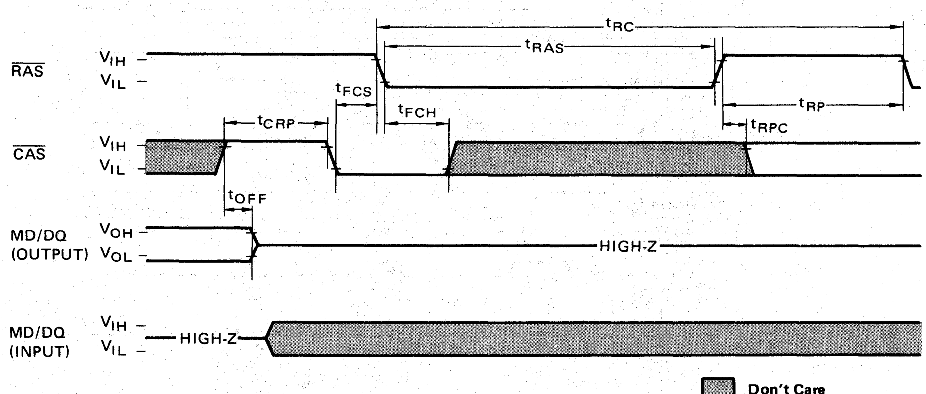


Note 1) When ME/WE = "H", all data on the MD/DQ can be written into the cell.
When ME/WE = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of RAS.

RAS-ONLY REFRESH CYCLE (ME/WE=Don't Care)



CAS-BEFORE-RAS REFRESH CYCLE (ADDRESS, ME/WE, TR/OE=Don't Care)



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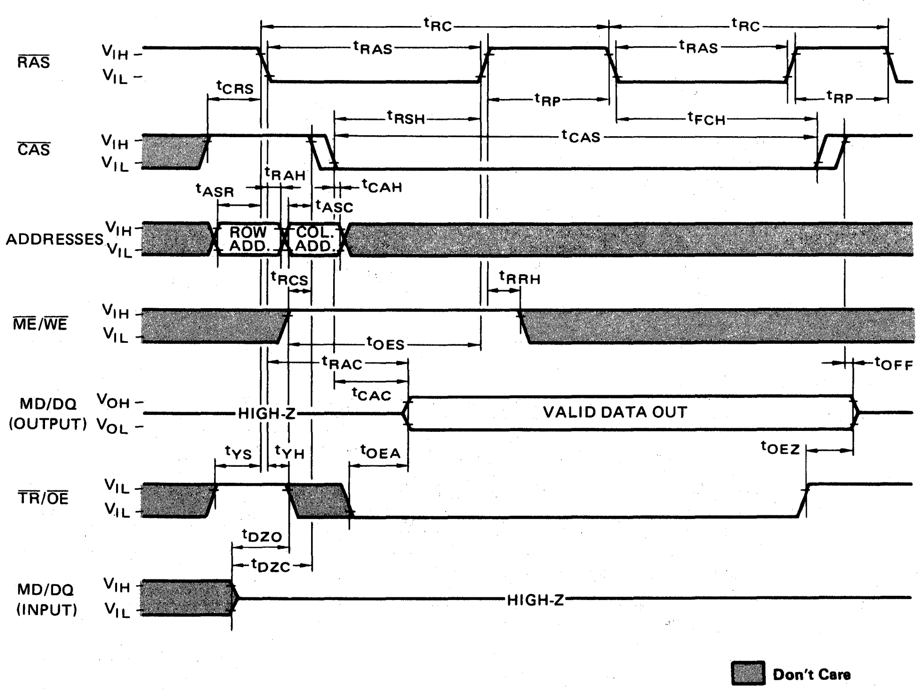
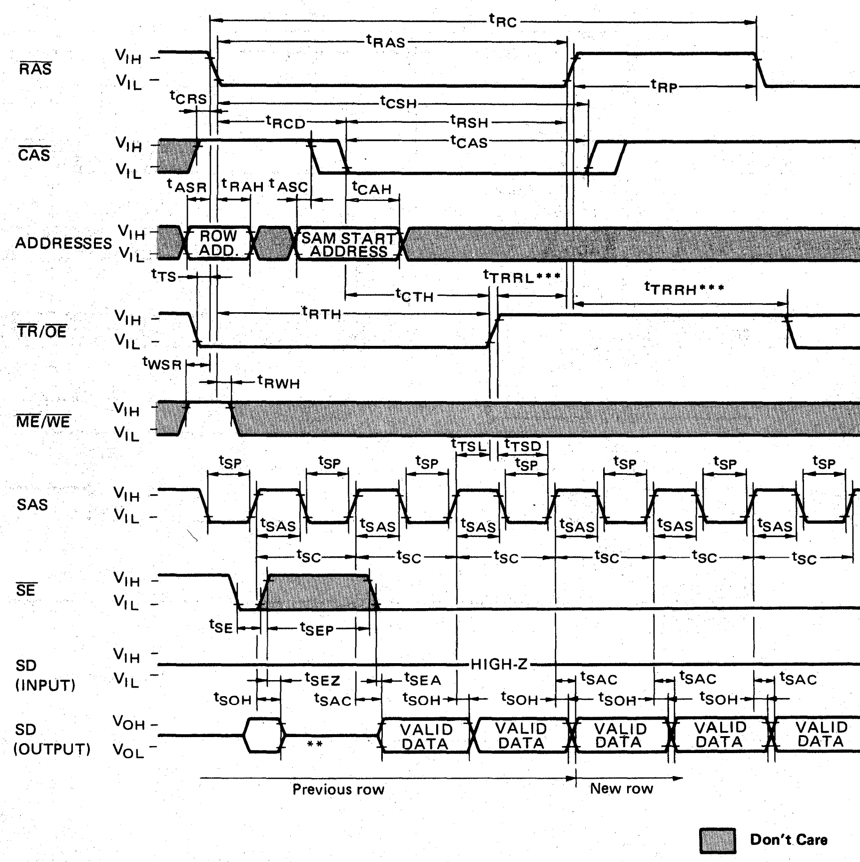
HIDDEN REFRESH CYCLE



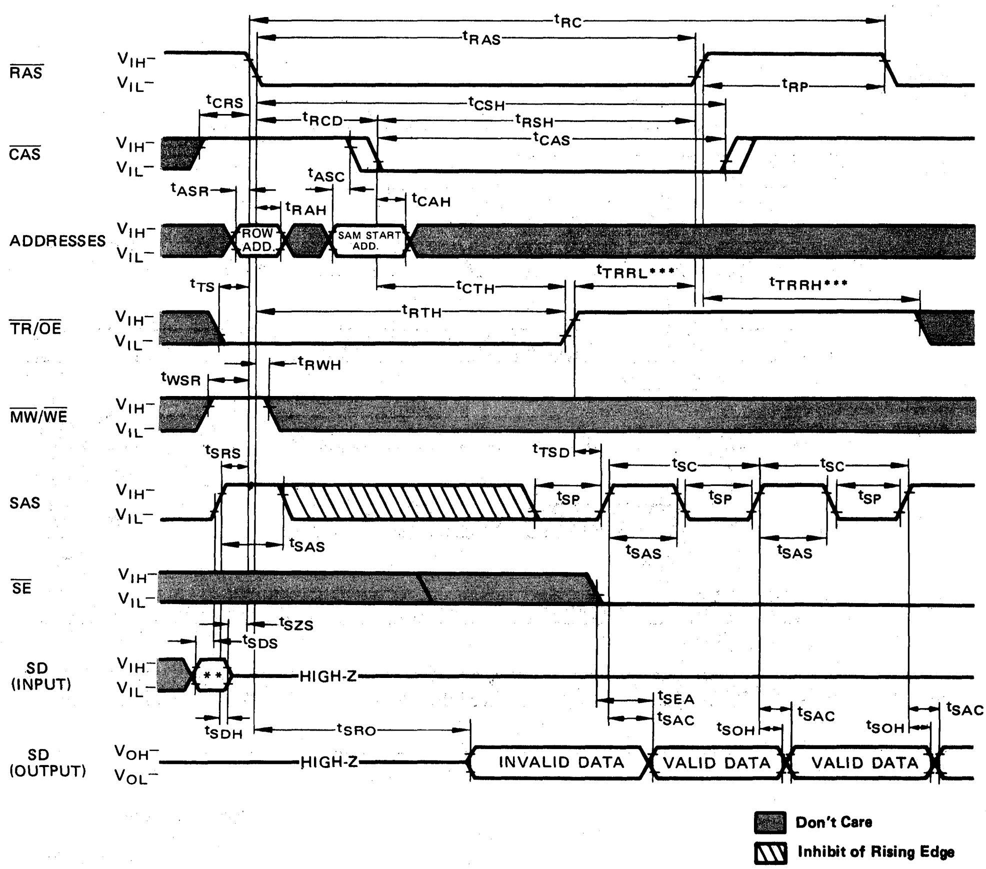
3

READ TRANSFER CYCLE* (MD/DQ = Don't Care)

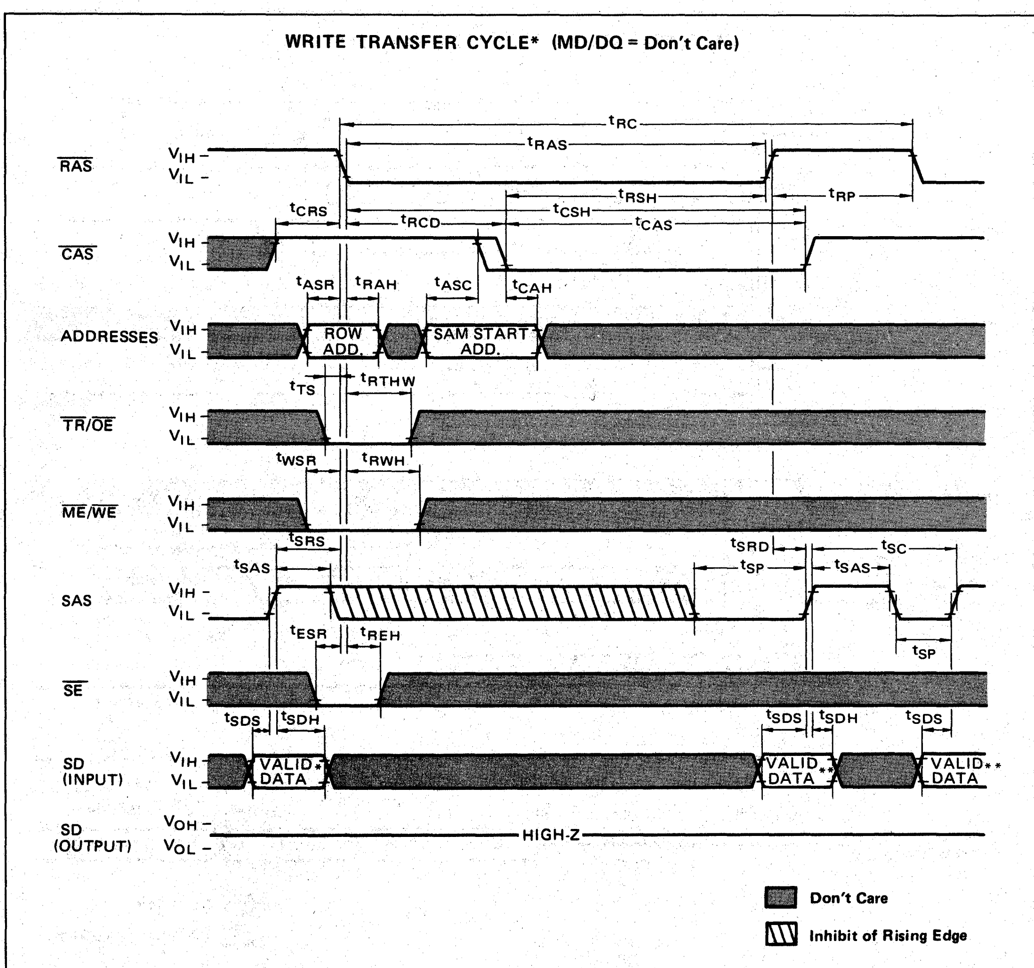


*: In the case that the previous transfer is read transfer.
**: If $\overline{SE}$ is low, the valid data will appear within t_{SAC} or t_{SEA}.
***: These parameters are different from that of MB 81461.

READ TRANSFER CYCLE* (MD/DQ = Don't Care)

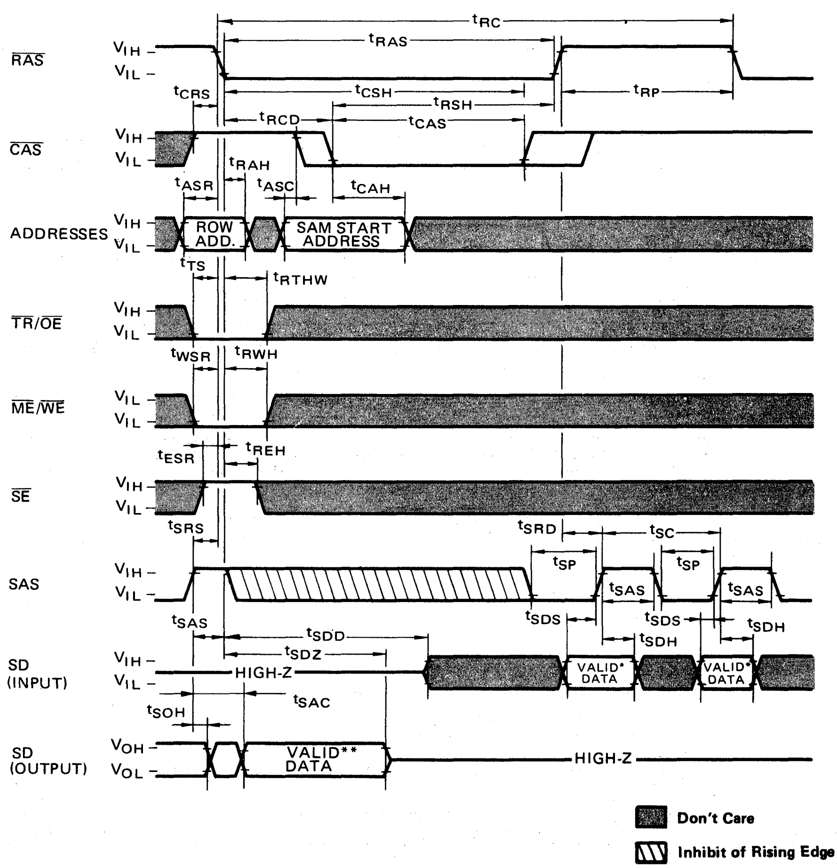


*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is low and the previous cycle is serial write cycle, this should be valid data input.
***; These parameters are different from that of MB 81461.



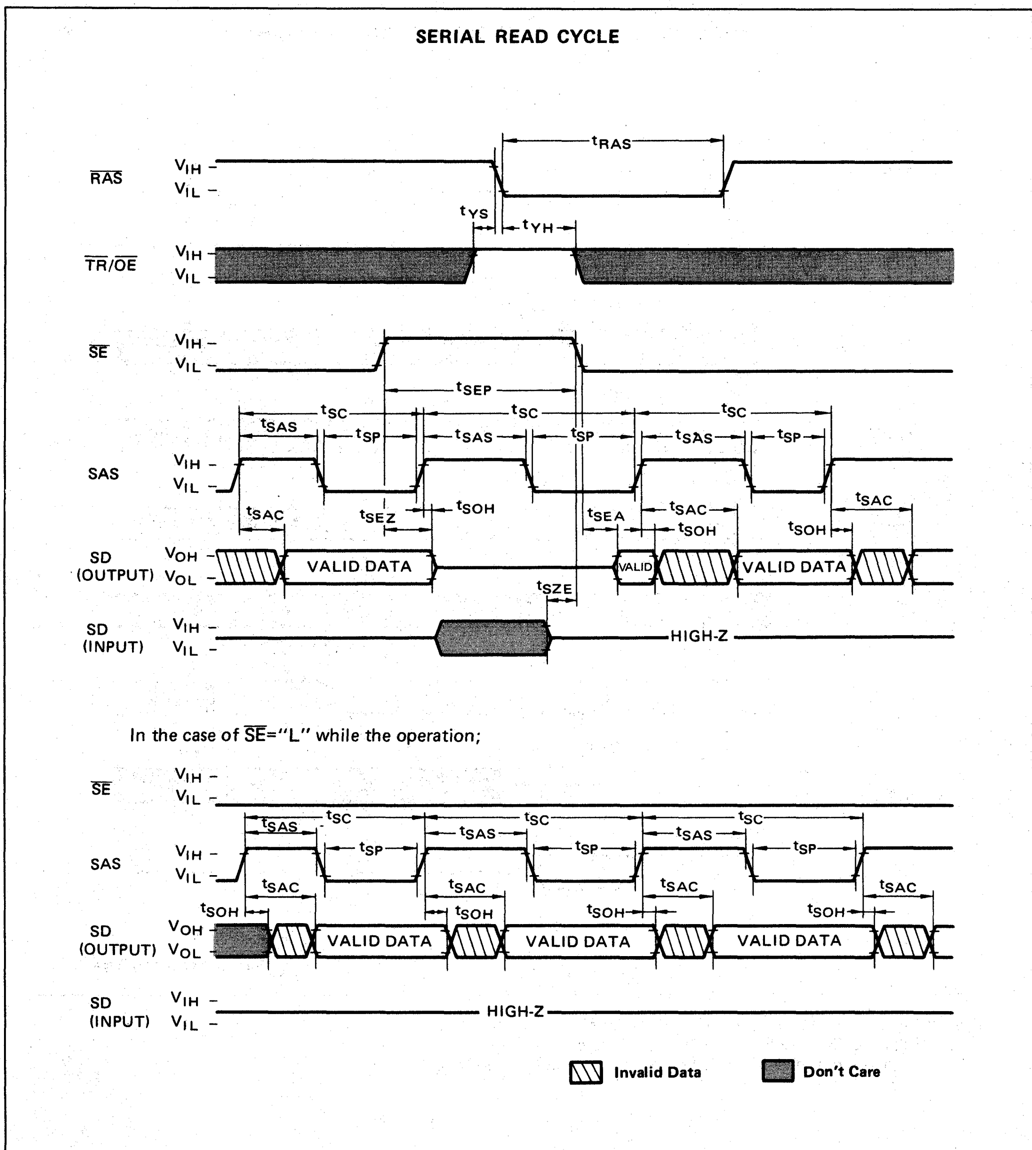
*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is high these data are not written into the SAM.

PSEUDO WRITE TRANSFER CYCLE (MD/ DQ = Don't Care)



*: If $\overline{SE}$ is high, these data are not written into SAM.
**: If $\overline{SE}$ is high, SD (SD0 to SD3) are in High-Z state after t_{SEZ}.
If $\overline{SE}$ becomes low, the valid data will appear meeting t_{SAC} and t_{SEA}.

3


SERIAL READ CYCLE
RAS
TR/OE
SE
SAS
SD (OUTPUT)
SD (INPUT)
VIH
VIL
VOH
VOL
tRAS
tYS
tYH
tSEP
tSC
tSAS
tSP
tSAC
tSEZ
tSOH
tSEA
tSZE
VALID DATA
VALID
HIGH-Z
In the case of SE="L" while the operation;
Invalid Data
Don't Care

SERIAL WRITE CYCLE

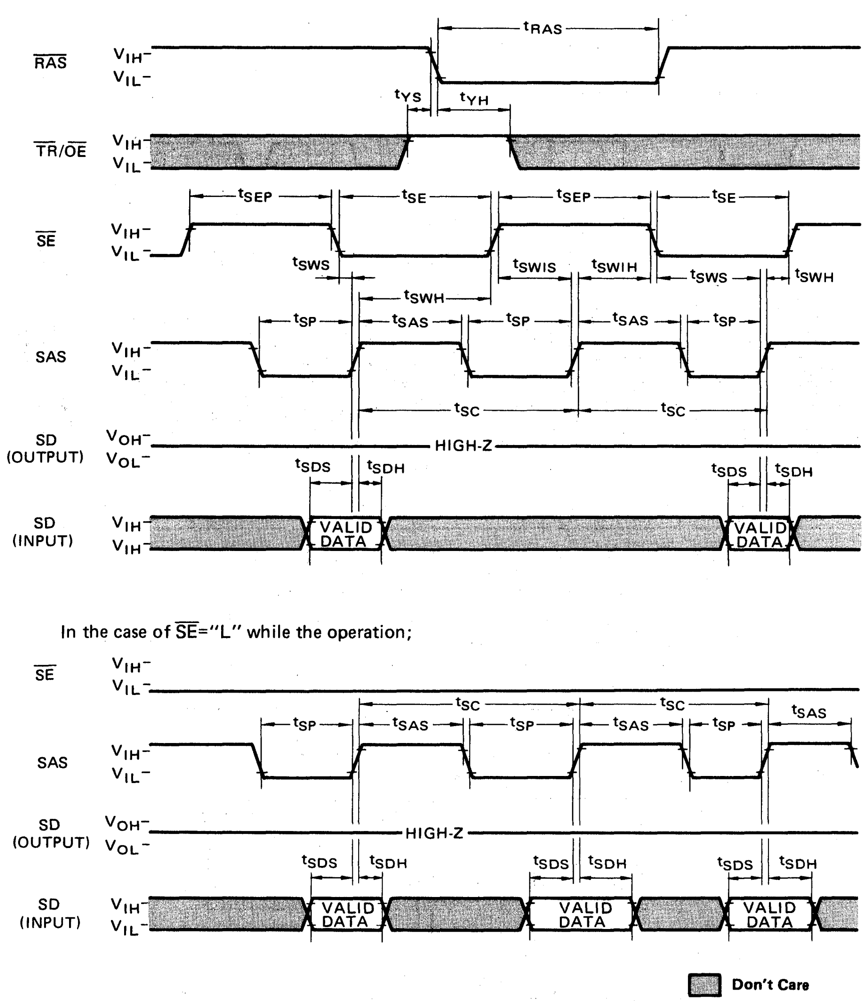


Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

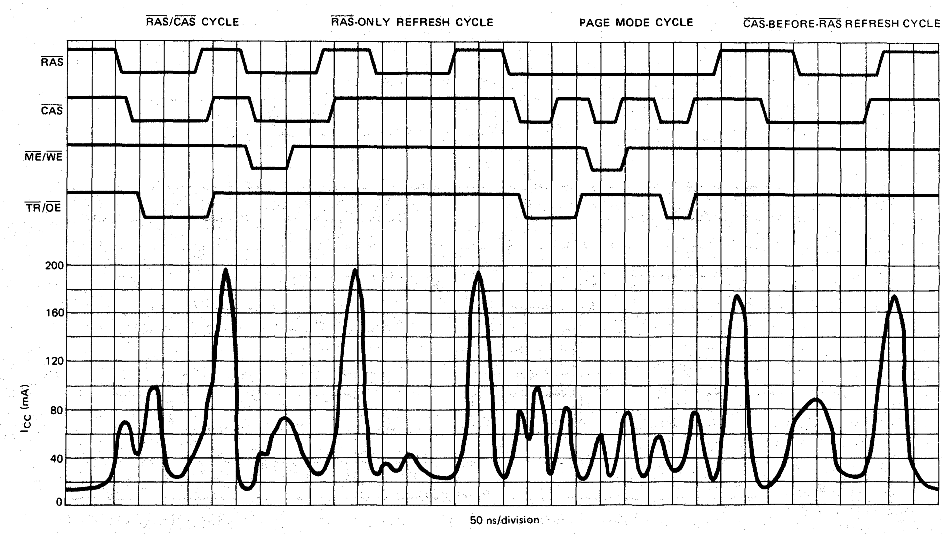
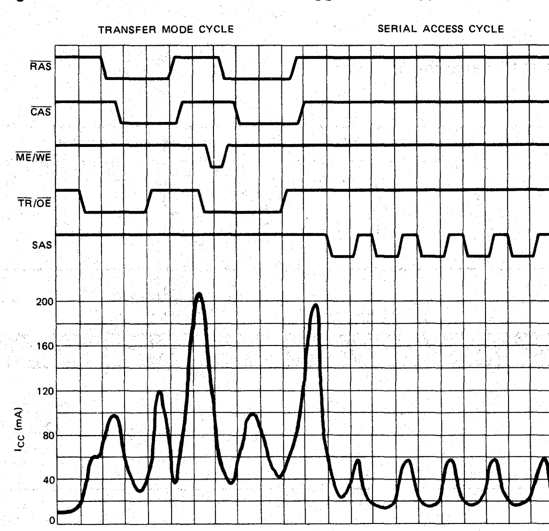


Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C) (cont'd)



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

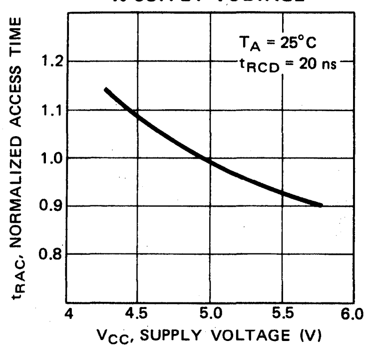


Fig. 7 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

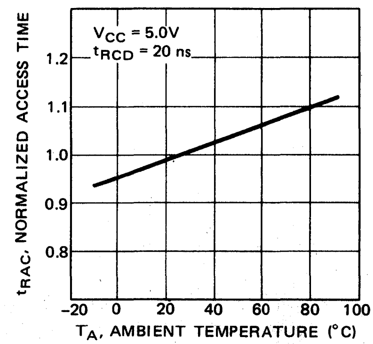


Fig. 8 – OPERATING CURRENT vs CYCLE RATE

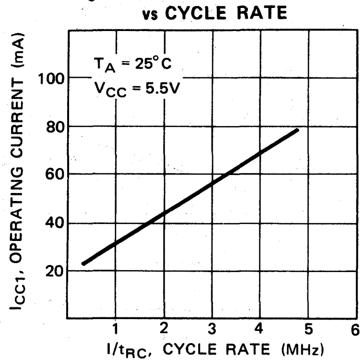


Fig. 9 – OPERATING CURRENT vs SUPPLY VOLTAGE

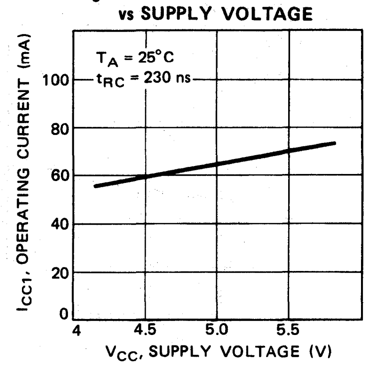


Fig. 10 – OPERATING CURRENT vs AMBIENT TEMPERATURE

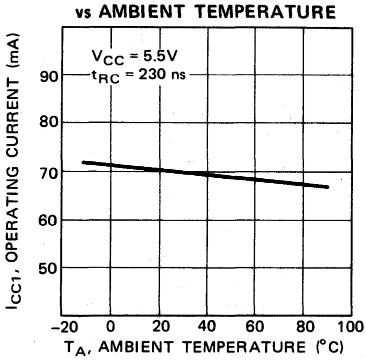


Fig. 11 – STANDBY SURRENT vs SUPPLY VOLTAGE

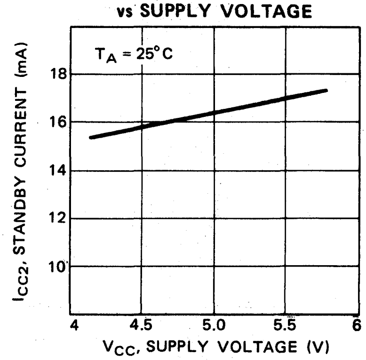


Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

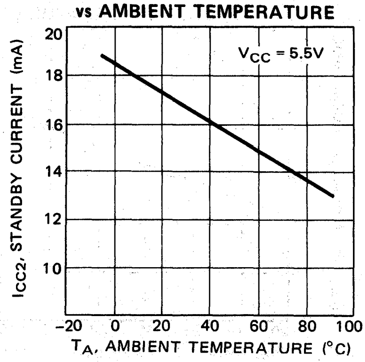


Fig. 13 – REFRESH CURRENT 1 vs CYCLE RATE

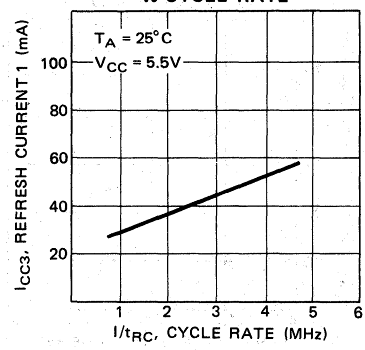


Fig. 14 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

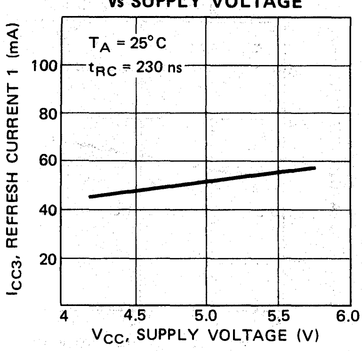


Fig. 15 – PAGE MODE CURRENT vs CYCLE RATE

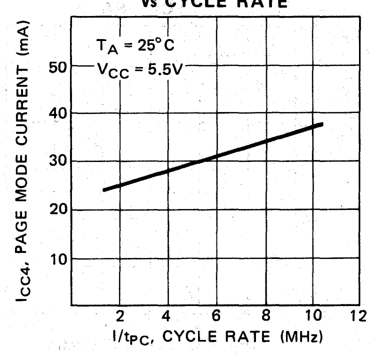


Fig. 16 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

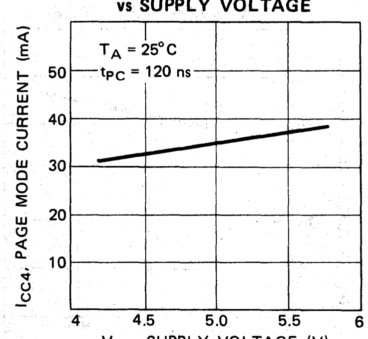


Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

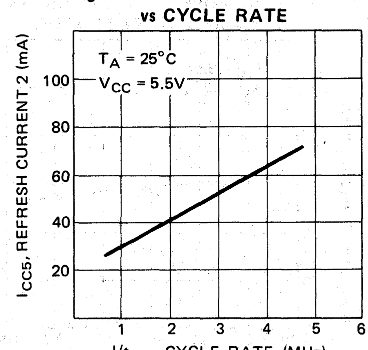


Fig. 18 — REFRESH CURRENT 2 vs SUPPLY VOLTAGE

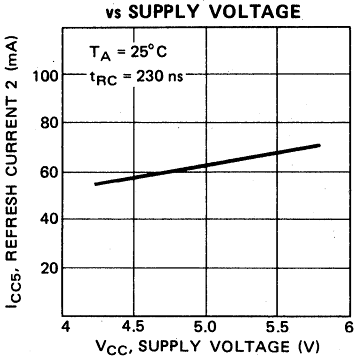


Fig. 19 — TRANSFER MODE CURRENT vs CYCLE RATE

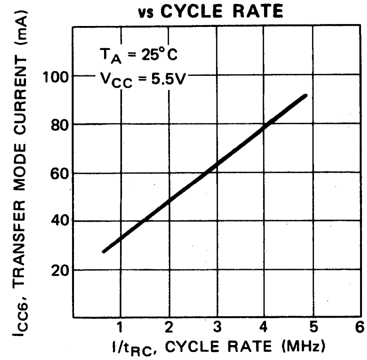


Fig. 20 — TRANSFER MODE CURRENT vs SUPPLY VOLTAGE

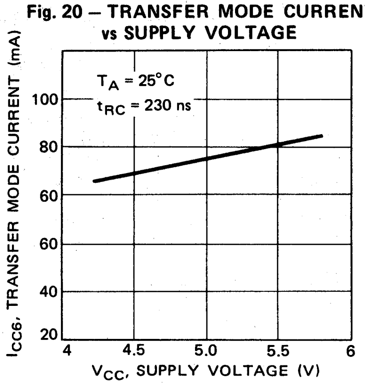


Fig. 21 — RAM STANDBY/SAM ACTIVE CURRENT vs CYCLE RATE

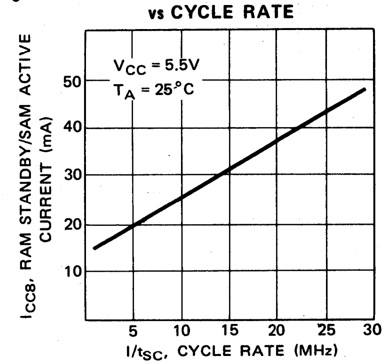


Fig. 22 — RAM STANDBY/SAM ACTIVE CURRENT vs SUPPLY VOLTAGE

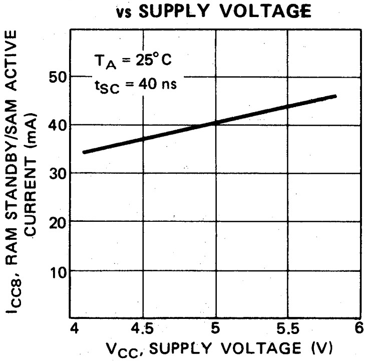


Fig. 23 — RAM STANDBY/SAM ACTIVE CURRENT vs AMBIENT TEMPERATURE

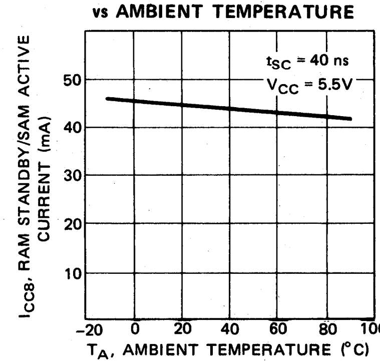


Fig. 24 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

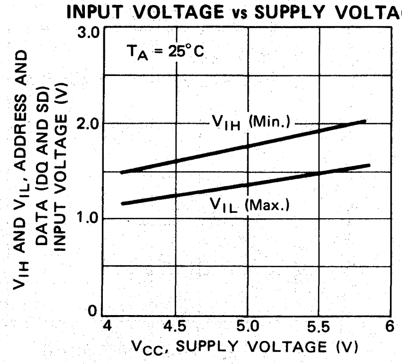


Fig. 25 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

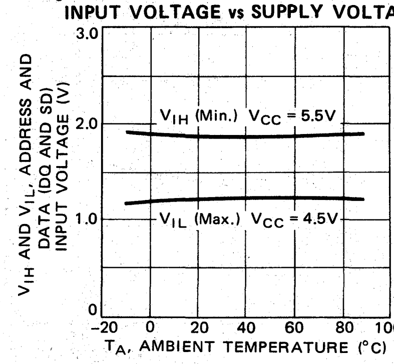


Fig. 26 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs SUPPLY VOLTAGE

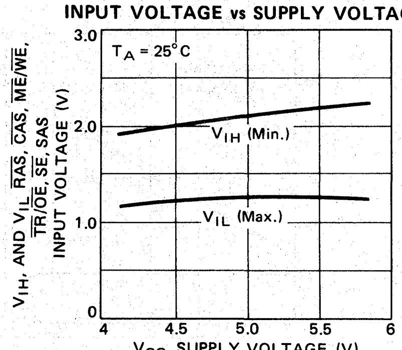


Fig. 27 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPU VOLTAGE vs AMBIENT TEMPERATURE

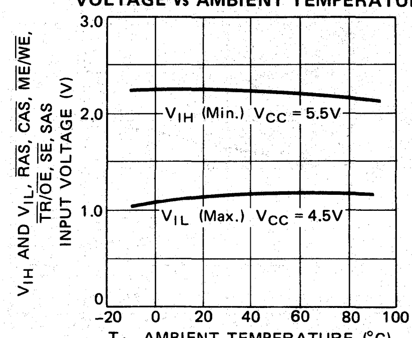


Fig. 28 – ACCESS TIME (RAM) vs LOAD CAPACITANCE

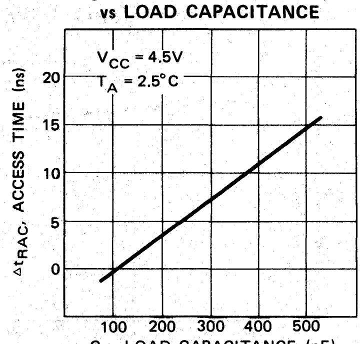


Fig. 29 – ACCESS TIME (SAM) vs LOAD CAPACITANCE

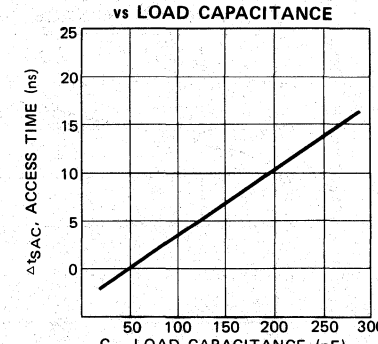


Fig. 30 — DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

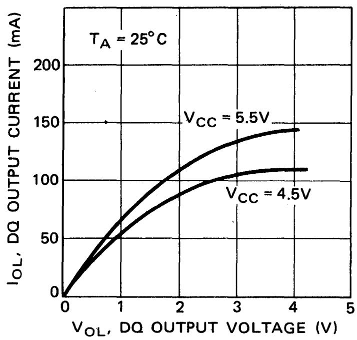


Fig. 31 — SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

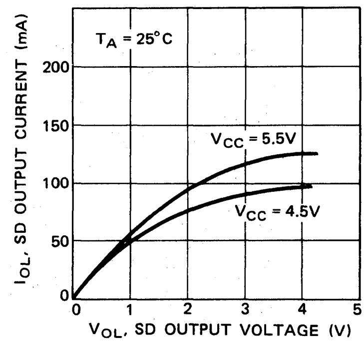


Fig. 32 — DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

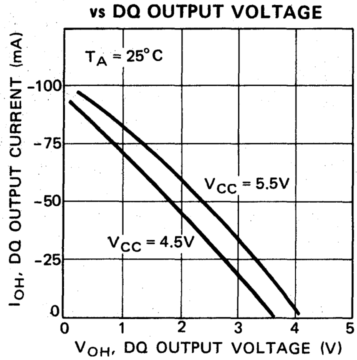


Fig. 33 — SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

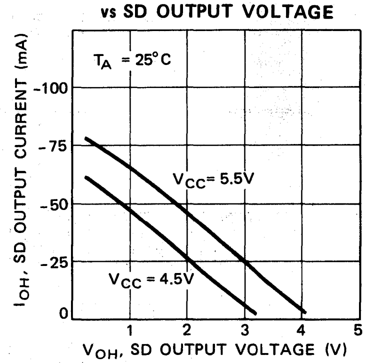
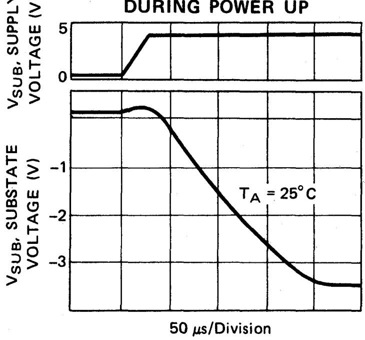


Fig. 34 — SUBSTRATE VOLTAGE DURING POWER UP

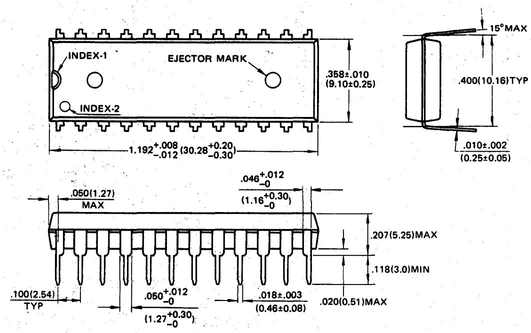


3

PACKAGE DIMENSIONS

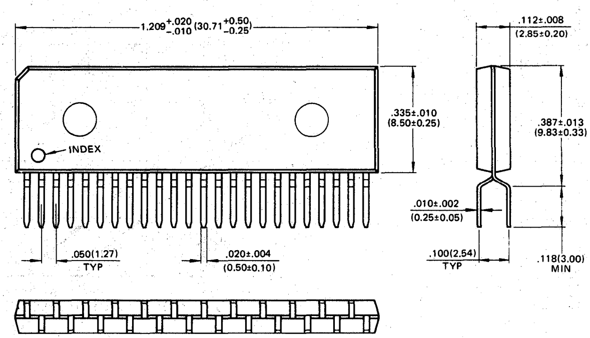
PLASTIC DIP (Suffix: -P) PLASTIC ZIP (Suffix: -PSZ)

24-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-24P-M04)



Dimensions in inches (millimeters)

24-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-24P-M02)



Dimensions in inches (millimeters)

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FUJITSU

1,048,576 BIT DUAL PORT CMOS DYNAMIC RANDOM ACCESS MEMORY

MB81C4251-10
MB81C4251-12
MB81C4251-15

July 1988
Edition 1.0

ADVANCE INFORMATION

262,144 x 4 BIT DUAL PORT CMOS DYNAMIC RAM

The Fujitsu MB81C4251 is a fully decoded dual port CMOS dynamic random access memory organized as 262,144 words by 4 bits dynamic RAM port and 512 words by 4 bits serial access memory (SAM) port. The MB81C4251 is ideally suited for mainframes, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design.

Multiplexed row and column address inputs permit the MB81C4251 to be housed in a 400mil wide 28 pin DIP, SOJ and ZIP. Pin outs conformed to the JEDEC approved pinout.

The MB81C4251 features a Bit Masked Write operation whereby the user can inhibit writing to particular bits.

The MB81C4251 is fabricated using silicon gate CMOS and Fujitsu's advanced triple-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time between memory refreshes.

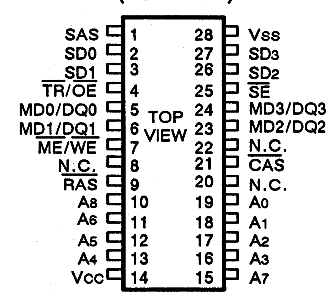
- Dual port organization
  262,144 words x 4 bits (DRAM port)
  512 words x 4 bits (SAM port)
- Silicon gate CMOS,1 transistor cell
- DRAM Port
  - Access Time (tRAC),
    - 100ns max. (MB81C4251-10)
    - 120ns max. (MB81C4251-12)
    - 150ns max. (MB81C4251-15)
  - Cycle Time (tRC)
    - 180ns min. (MB81C4251-10)
    - 210ns min. (MB81C4251-12)
    - 260ns min. (MB81C4251-15)
- SAM Port
  - Access Time (tSAC),
    - 30ns max. (MB81C4251-10)
    - 40ns max. (MB81C4251-12)
    - 60ns max. (MB81C4251-15)
  - Cycle Time (tSC)
    - 30ns min. (MB81C4251-10)
    - 40ns min. (MB81C4251-12)
    - 60ns min. (MB81C4251-15)
- TTL-compatible all inputs and outputs
- 512 refresh cycles every 8.2ms
- Bi-directional data transfer capability
- Fast serial access asynchronous to DRAM except transfer operation
- Addressable start location (TAP) on serial shift register
- Realtime Read Transfer capability
- Bit Masked Write Mode capability
- I/O switch by transfer cycle
- Fast Page Mode. Read-Modify-Write capability
- Single +5V power supply, ±10% tolerance
- Power Dissipation
  - DRAM;Act/SAM;Stby
    - 450mW max. (MB81C4251-10)
    - 400mW max. (MB81C4251-12)
    - 350mW max. (MB81C4251-15)
  - DRAM;Stby/SAM;Act
    - 330mW max.(MB81C4251-10)
    - 280mW max.(MB81C4251-12)
    - 250mW max.(MB81C4251-15)
  - DRAM;Sty/SAM;Stby
    - 22mW max.

PLASTIC DIP 28-PIN
DIP-28P-MXX

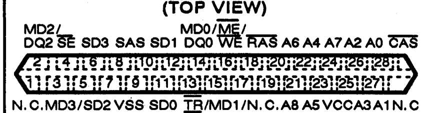
PLASTIC ZIP 28-PIN
ZIP-28P-MXX

PLASTIC SOJ 28-PIN
LCC-28P-MXX

PIN ASSIGNMENT
(TOP VIEW)



28-Pin ZIP
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Section 4

MOS RAM Modules

4

Page	Device	Maximum Access Time(ns)	Capacity	Package Options
4-3	MB85225-12 MB85225-15	120 150	2097152 bits (262144w x 8b)	30-pin Plastic SIP
4-17	MB85227-10 MB85227-12 MB85227-15	100 120 150	2359296 bits (262144w x 9b)	30-pin Plastic SIP
4-31	MB85230-10 MB85230-12	100 120	8388608 bits (1048576w x 8b)	30-pin Plastic SIP
4-49	MB85235-10 MB85235-12	100 120	9437184 bits (1048576w x 9b)	30-pin Plastic SIP
4-65	MB85240-10 MB85240-12	100 120	2359296 bits (262144w x 9b)	30-pin Plastic SIP
4-81	MB85402-30 MB85402-40	30 40	262144 bits (16384w x 16b)	36-pin Ceramic DIP/SIP
4-89	MB85403A-40 MB85403A-50	40 50	2097152 bits (262144w x 8b)	44-pin Ceramic TSIP
4-97	MB85410-30 MB85410-40	30 40	524288 bits (65536w x 8b)	60-pin Plastic ZIP
4-105	MB85414-30 MB85414-40	30 40	524288 bits (16384w x 32b)	64-pin Plastic ZIP
4-113	MB85420-40 MB85420-50	40 50	2097152 bits (262144w x 8b)	60-pin Plastic ZIP

4

FUJITSU

MOS 262144 × 8 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

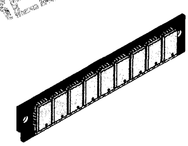
MB 85225-12
MB 85225-15

April 1986
Edition 1.0

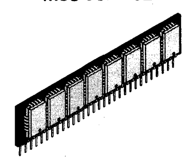
262,144 x 8-BIT DYNAMIC RANDOM ACCESS MEMORY SIP MODULE

The Fujitsu MB 85225 is a fully decoded, 262,144 words x 8-bits NMOS-dynamic random access memory composed of eight 256K DRAM chips (MB 81256 x 8). Assembling eight PLCC chips on a 30 pin plastic Single-In Line Package (SIP), this RAM module is optimized for the application where high-density and large capacity of storage memory is needed.

The electrical characteristics of the MB 85225 are quite same as the original MB 81256; each timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

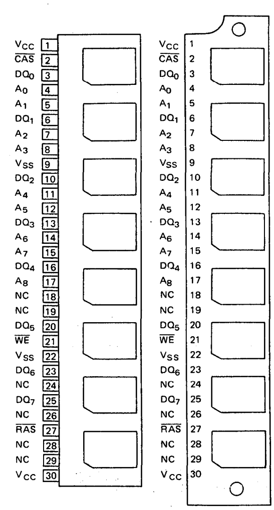


PLASTIC PACKAGE
MSS-30P-P02



PLASTIC PACKAGE
MSP-30P-P03

PIN ASSIGNMENT



- 262,144 x 8 DRAM 30-pin Plastic SIP (MB 81256 x 8)
- Row access time (t_{RAC}),
  120 ns max. (MB 85225-12)
  150 ns max. (MB 85225-15)
- Cycle time (t_{CAC}),
  230 ns min. (MB 85225-12)
  260 ns min. (MB 85225-15)
- Page Cycle Time (t_{PC}),
  120 ns min. (MB 85225-12)
  150 ns min. (MB 85225-15)
- Single +5 V supply, ±10% tolerance
- Low power (active),
  2860 mW max. (MB 85225-12)
  2508 mW max. (MB 85225-15)
  198 mW max. (Standby)
- 4 ms/256 refresh cycles capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability
- Page Mode Capability
- On-chip latches for Addresses and Data-in
- Standard 30-pad Plastic Leaded SIP (Suffix: PDPS)
- Standard 30-pin Plastic Leadless SIP (Suffix: PDPB)

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	–1 to +7	V
Storage temperature	T_{STG}	–55 to +125	°C
Power dissipation	P_D	8.0	W
Short circuit output current	–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 — FUNCTIONAL BLOCK DIAGRAM

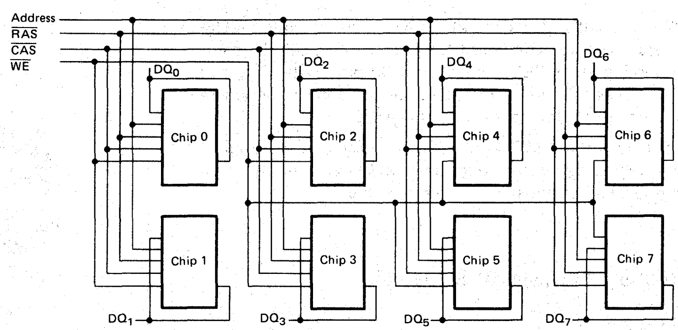
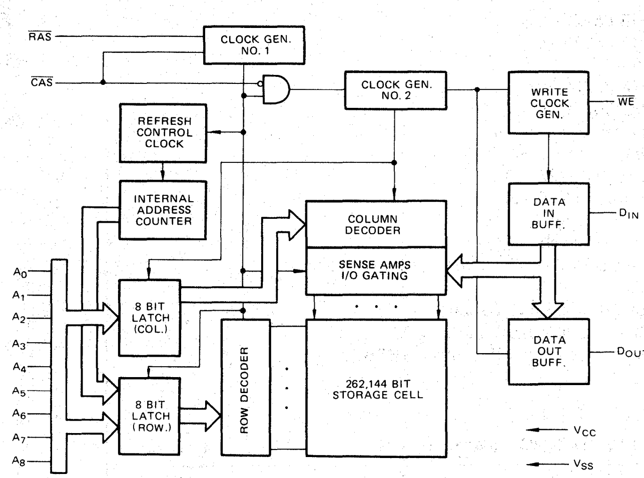


Fig. 2 — BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8	C_{IN1}	—	TBD	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	TBD	pF
Input/Output Capacitance, DQ_0 to DQ_7	C_{IO}	—	TBD	pF

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RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C*
Input High Voltage	V_{IH}	2.4	–	6.5	V	
Input Low Voltage	V_{IL}	-1.0	–	0.8	V	

Note * : Maximum ambient temperature is permissible under certain conditions.
See the derating curve Fig. 3 for normal cycle, and Fig. 4 for page mode cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	MB 85225-12	I_{CC1}		520	mA
	MB 85225-15			456	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		36	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 85225-12	I_{CC3}		440	mA
	MB 85225-15			400	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = Min.)	MB 85225-12	I_{CC4}		240	mA
	MB 85225-15			200	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 85225-12	I_{CC5}		480	mA
	MB 85225-15			440	
INPUT LEAKAGE CURRENT (Except for DQ pins) Input leakage current, any input ($0 \leqq V_{IN} \leqq 5.5$ V, V_{CC} = 5.5 V, V_{SS} = 0 V, all other pins not under test = 0 V)		$I_{I(L)}$	–80	80	μA
OUTPUT LEAKAGE CURRENT (DQ pins) (Data out is disabled, $0 \text{ V} \leqq V_{OUT} \leqq 5.5$ V) DQ pins are high impedance state.		$I_{O(L)}$	–10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = –5 mA) Output low voltage (I_{OL} = 4.2 mA)		V_{OH} V_{OL}	2.4	 0.4	V

Note 1) : I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

4

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB 85225-12		MB 85225-15		Unit
			Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4	ms
Random Read/Write Cycle Time	4	t_{RC}	230		260		ns
Access Time from $\overline{RAS}$	5 6	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$	6 7	t_{CAC}		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	0	30	ns
Transition Time		t_{T}	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	8 9	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	20		20		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		ns
Column Address Hold Time		t_{CAH}	20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	10	t_{RCH}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	10	t_{RRH}	20		20		ns
Write Command Set Up Time		t_{WCS}	0		0		ns
Write Command Pulse Width		t_{WP}	20		25		ns
Write Command Hold Time		t_{WCH}	20		25		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$-cycle)		t_{FCS}	25		30		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$-cycle)		t_{FCH}	25		30		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

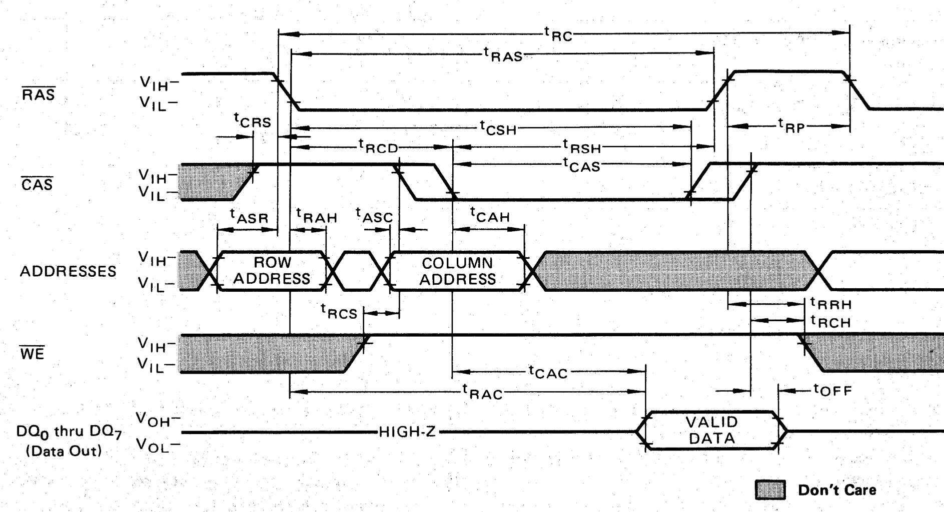
Parameter NOTES	Symbol	MB-85225-12		MB-85225-15		Unit
		Min	Max	Min	Max	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycle)	t_{RPC}	20		20		ns
Page Mode Read/Write Cycle Time 11	t_{PC}	120		150		ns
Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	50		65		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	25		30		ns

Notes:

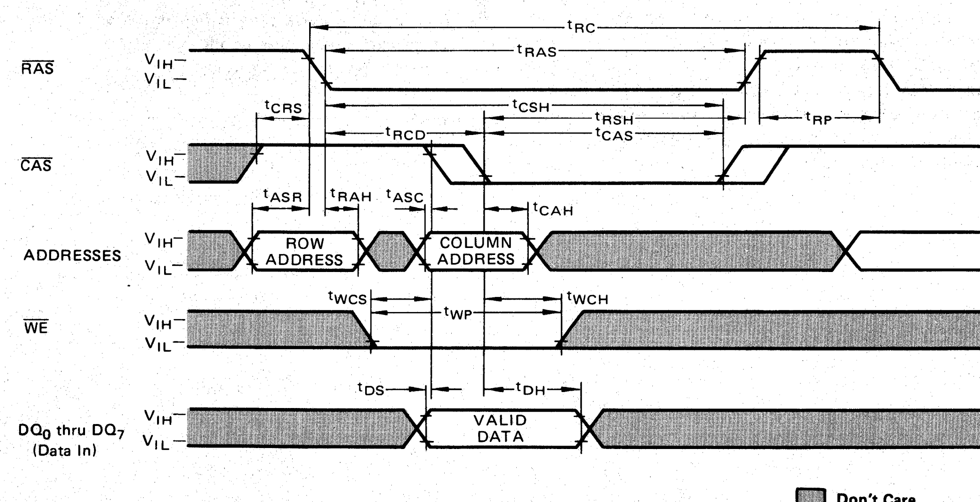
1. An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are refrence levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. The minimum cycle time is dependent on the ambient temperature and cooling conditions.
   See Fig. 3 for durating curve.
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
8. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The minimum cycle time is dependent on the ambient temperature and cooling conditions.
    See Fig. 4 for derating curve.

4

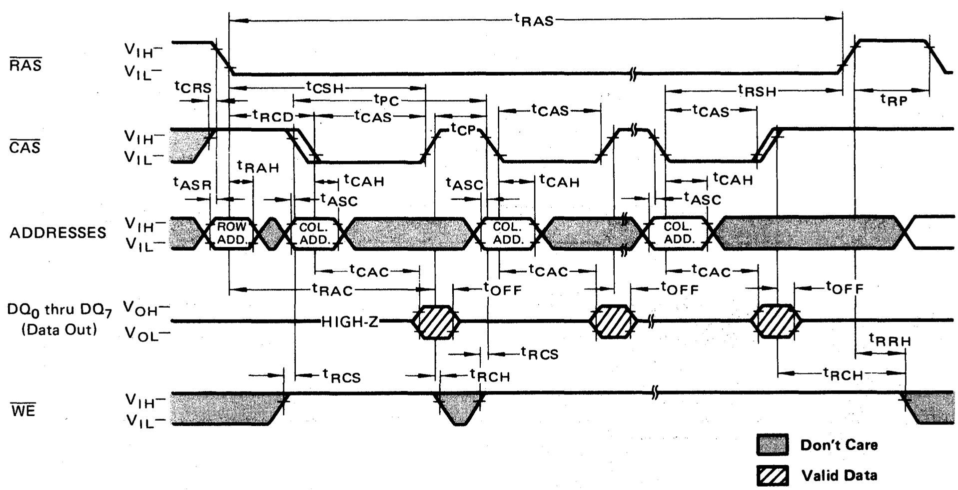
Read Cycle



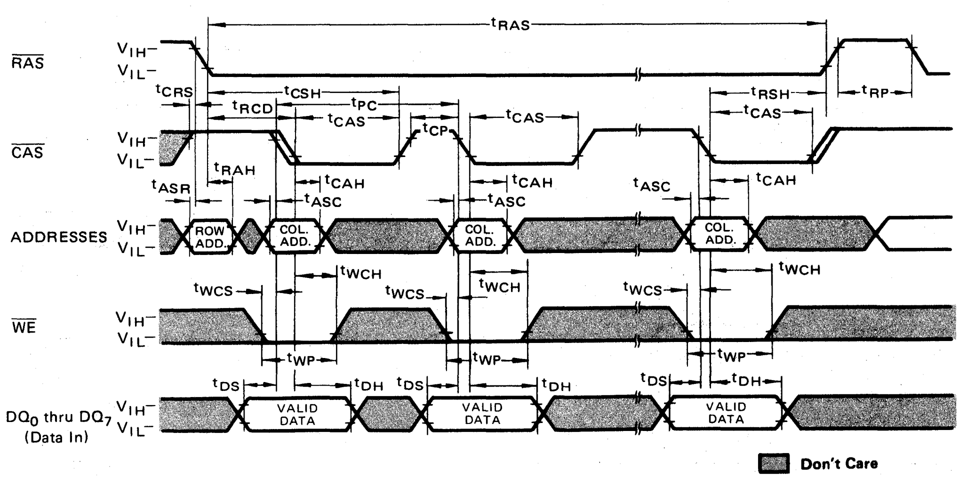
Write Cycle (Early Write)



Page Mode Read Cycle



Page Mode Write Cycle



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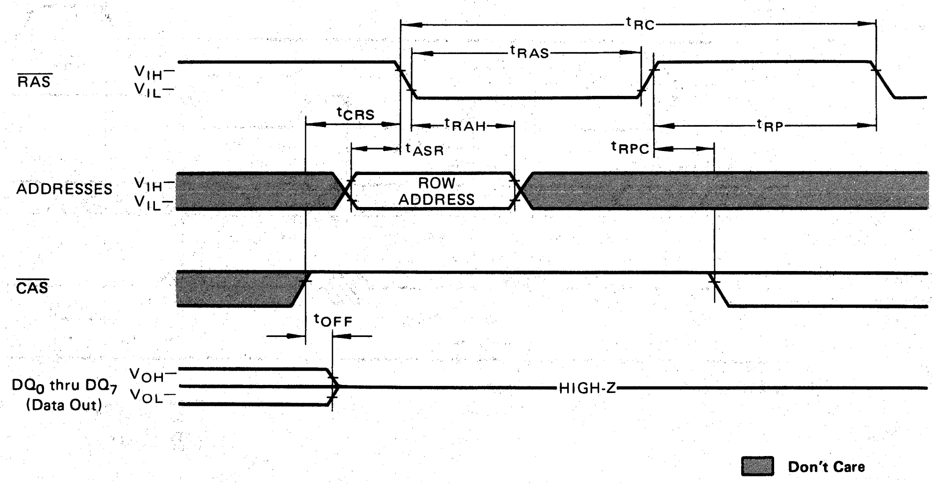
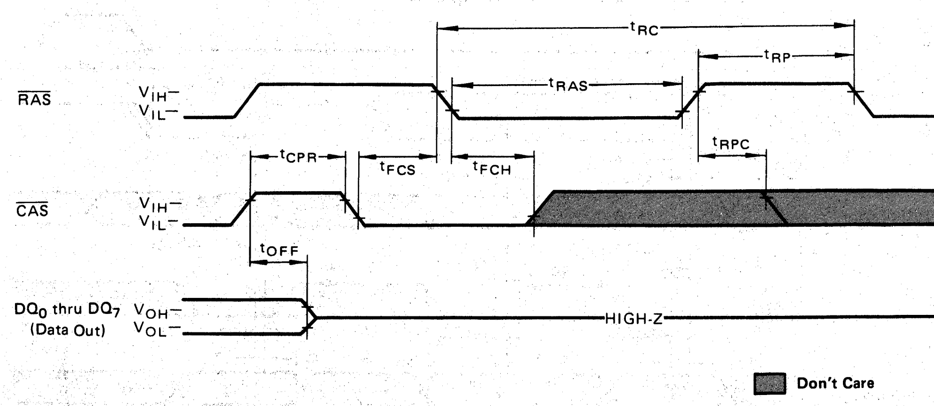
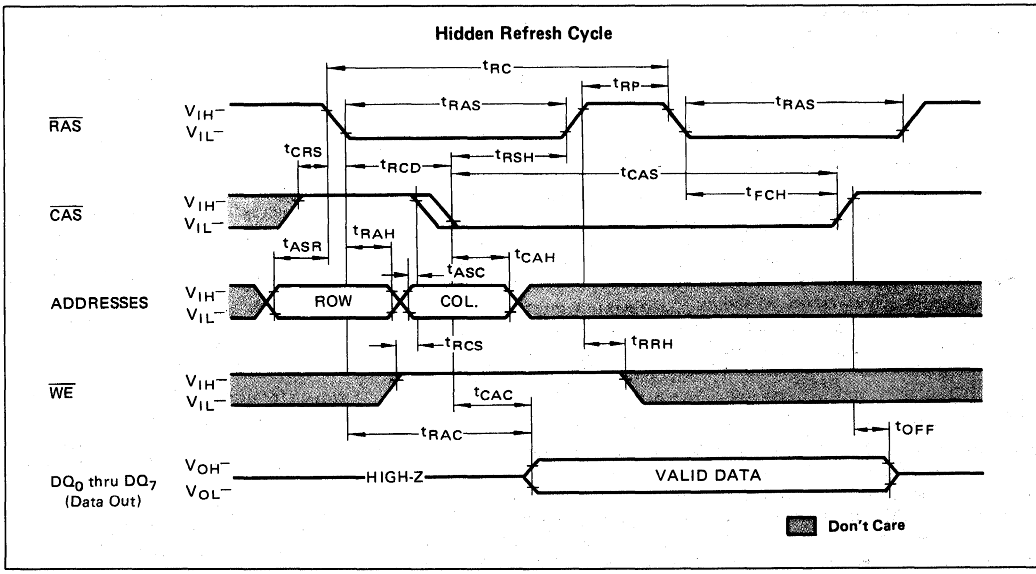
$\overline{RAS}$-only Refresh cycle
NOTE: $\overline{WE}$ = Don't care



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle
NOTE: Address, $\overline{WE}$ = Don't care





FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQ_0 to DQ_7	Function
H	H	Don't Care	High-Z	Standby
L	L	H	Valid Data Out[1)]	Read cycle
L	L	L	Valid Data In[2)]	Write cycle
L	L[3)]	Don't Care	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh cycle
L	H	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle

Notes 1) : DQ Pins are output mode.
2) : DQ pins are input mode.
3) : $t_{FCS} \geqq t_{FCS}$ (min).

DESCRIPTION

Simple Timing Requirement:
The MB 85225 has imporved circuitry that eases timing requirements for high speed access operations. The MB 85225 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 85225 has the minimal hold times of address (t_{CAH}), WE (t_{WCH}) and D_{IN} (t_{DH}). The provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirement that are referenced to RAS non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, and t_{DHR}. As a result, the hold times of the column address, DQ (input) and WE are not restricted by t_{RCD}.

Address Inputs:
A total of eighteen binary input address bits are required to decode parallel 8 bits data of 2,097,152 storage cells within the MB 85225.
Nine row address bits are established on the input pins (A_0 through A_8) and latched with RAS.
Nine column address bits are established on the input pins and latched with CAS. All input addresses must be stable on or before the falling edge of RAS. CAS is internally inhibited by RAS to permit triggering of CAS as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable:
The read mode or write mode is selected with the WE input. A high on the WE selects read mode, low selects write mode. Data inputs are disabled when read mode is selected.

Data Pins:
The input and output terminal of each LCC is directly connected on the mother board to save the number of I/O pins. The write cycle should be early write cycle in order to avoid data conflict between output data and input data.

Data Input:
The 8-bit data are written into the MB 85225 through the DQ pins (DQ_0 ~ DQ_7) during a write (early write) cycle. The falling edge of CAS is strobe for the data input register.
The set up and hold times are referenced to CAS.

Data Output:
The output buffer of each chips are three state TTL compatible with a fan out of two standard TTL loads.
The output are in high impedance state until CAS is brought low. In a read cycle, the output is valid after t_{RAC} from the falling edge of RAS when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of CAS when the transistion occurs after t_{RCD} (max). Data remain valid until CAS is returned to a high level.

Page-Mode:
Page-mode operation permits strobing the row-address into the MB 85225 while maintaining RAS at low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of RAS is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each 256 row address (A_0 through A_7 of the at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8.
The MB 85225 offers the following three types of refresh.

1) RAS-Only Refresh;
RAS Only refresh avoids any output during refresh because the output buffer is in high impedance state unless CAS is brought low. Strobing each of 256 row addresses with RAS will cause all bits in each row to be refreshed.
2) CAS-before-RAS Refresh;
CAS-before-RAS refresh available on the MB 85225 offers an alternate refresh method. If CAS is held low for the specified period (t_{FCS}) before RAS goes to low, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next CAS-before-RAS refresh operation. So, by performing 256 cycles for CAS-before-RAS refresh, all bits in a module are refreshed.
3) Hidden Refresh;
Hidden refresh may take place while maintaining latest valid data at the output by extending CAS active time. In MB 85225 hidden refresh means CAS-before-RAS refresh and the internal refresh address are used, that is no external refresh address is needed.

Notice for using
The MB 85225 is a SIP (Single-In-Line-Package) module which is composed of eight MB 81256 DRAMs housed in plastic LCC, and assembled on the multilayer epoxy printed circuit board. Furthermore, as the MB 85225 is a very high-speed memory, the timing windows to strobe address WE and D_{IN} signals are very short (Approx. 5 ns). Therefore, it is very sensitive even to very sharp noise.
From above reasons, special care should be taken for using the MB 85225.
The following notices are recommended;

1. Provide a capacitor of approx. a few μF for each module, though the MB 85225 has eight decoupling capacitors of 0.22 μF on the each modules.
2. Remove noise, riging, overshoot and undershoot from the address, control and DQ lines, so that the MB 85225 won't latch wrong signals due to the noise induction between signal lines and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. Provide an appropriate dumping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

Fig. 3 – MB 85225 DERATING CURVE
(Normal Cycle)

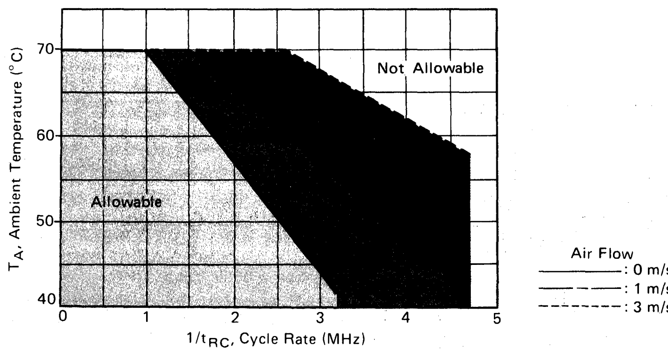
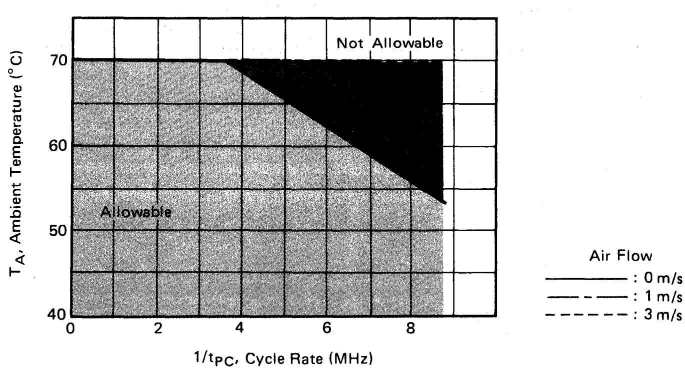


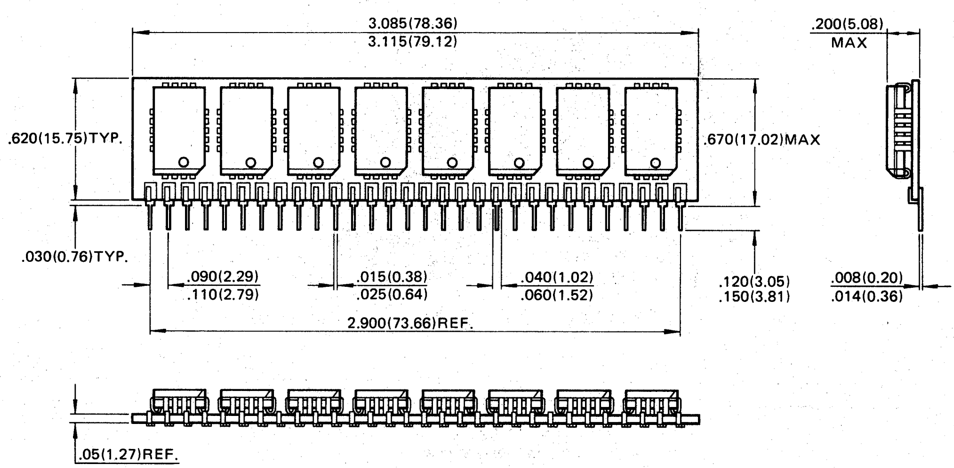
Fig. 4 – MB 85225 DERATING CURVE
(Page Mode Cycle)



4

PACKAGE DIMENSIONS

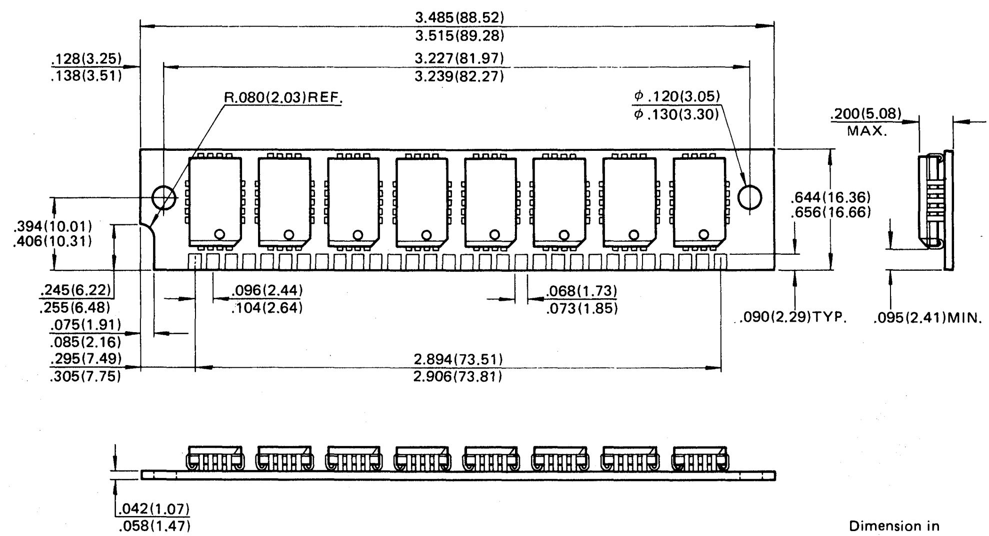
30-LEAD PLASTIC MULTI SINGLE PACKAGE
(CASE No.: MSP-30P-P03)



Dimension in inches(millimeters).

PACKAGE DIMENSIONS

30-LEAD PLASTIC SINGLE PACKAGE
(CASE No.: MSS-30P-P02)



Dimension in inches(millimeters).

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

4

FUJITSU

262144×9 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

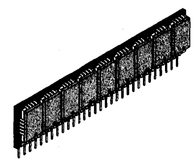
MB85227-10 MB85227-12 MB85227-15

December 1987
Edition 2.0

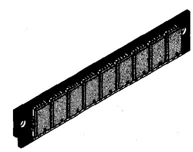
262,144 x 9-BIT DYNAMIC RANDOM ACCESS MEMORY SIP MODULE

This Fujitsu MB85227 is a fully decoded, 262,144 words x 9 bits NMOS dynamic random access memory composed of nine 256K DRAM chips (MB81256 x 9). Assembling nine PLCC chips on a 30 pin PCB, this RAM module is optimized for the applications where high-density and large capacity of storage memory with parity bit is needed.
The electrical characteristics of the MB85227 are the same as the original MB81256; each timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

- 262,144 x 9 DRAM, 30-pin SIP (MB81256 x 9)
- Row access time (t_{RAC}),
  100 ns max. (MB85227-10)
  120 ns max. (MB85227-12)
  150 ns max. (MB85227-15)
- Cycle time (t_{RC}),
  200 ns min. (MB85227-10)
  220 ns min. (MB85227-12)
  260 ns min. (MB85227-15)
- Page Cycle Time (t_{PC}),
  100 ns min (MB85227-10)
  120 ns min (MB85227-12)
  150 ns min. (MB85227-15)
- Single +5V supply, ±10% tolerance
- Low power (active)
  3465 mW max. (MB85227-10)
  3213 mW max. (MB85227-12)
  2822 mW max. (MB85227-15)
  226 mW max. (Standby)
- 4 ms/256 refresh cycles capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability
- Page Mode Capability
- On-chip latches for Addresses and Data-in
- Leaded and Leadless types are available
- Compatible with TM4256EL9/TM4256EU9 and MH25609J
- Standard Leaded Epoxy SIP (Suffix: PDPS)
- Standard Leadless Epoxy SIM (Suffix: PDPB)

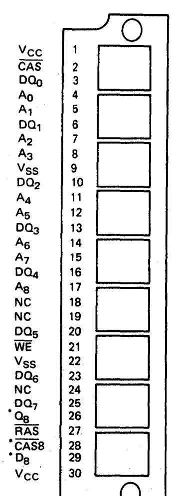


PLASTIC PACKAGE
MSP-30P-P02



PLASTIC PACKAGE
MSS-30P-P01

PIN ASSIGNMENT



*; For parity bit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{STG}	−55 to 125	°C
Power dissipation	P_D	4.5	W
Short circuit output current	—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – FUNCTIONAL BLOCK DIAGRAM

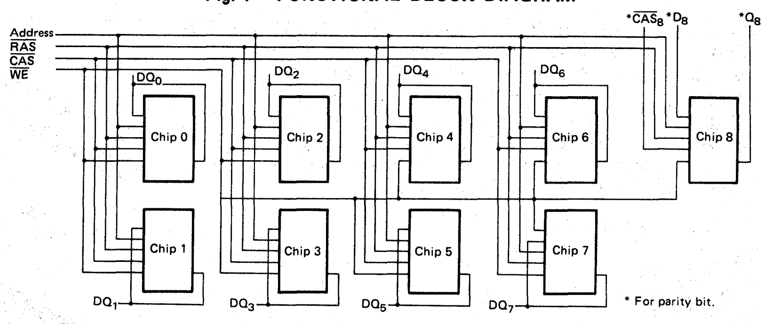
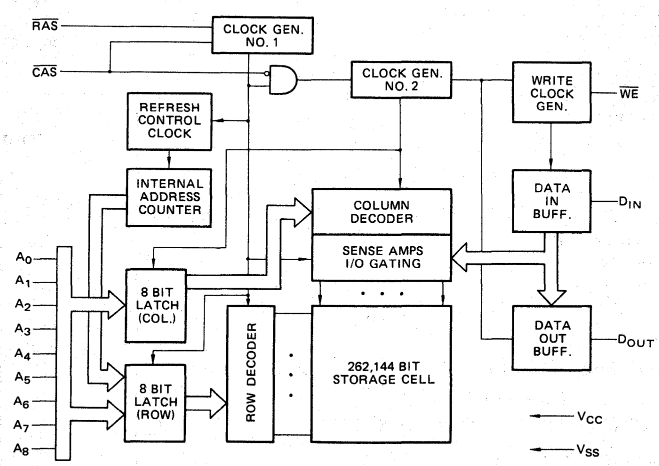


Fig. 2 – BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_8	C_{IN1}		75	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}		80	pF
Input Capacitance, $\overline{CAS}$	C_{IN3}		70	pF
Input Capacitance, $\overline{WE}$	C_{IN4}		55	pF
Input Capacitance, $\overline{CAS8}$	C_{IN5}		10	pF
Input Capacitance, D_8	C_{IN6}		7	pF
I/O Capacitance, DQ_0 to DQ_7	C_D		17	pF
Output Capacitance, Q_8	C_O		12	pF

4

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C*
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	–	6.5	V	
Input Low Voltage	V_{IL}	−2.0	–	0.8	V	

Note * : Maximum ambient temperature is permissible under certain conditions.
See the derating curve Fig. 3 for normal cycle, and Fig. 4 for page mode cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$, $\overline{CAS8}$ cycling; t_{RC} = Min.)	MB85227-10	I_{CC1}		630	mA
	MB85227-12			585	
	MB85227-15			513	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{CAS8}$ = V_{IH})		I_{CC2}		41	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$ = V_{IH}; t_{RC} = Min.)	MB85227-10	I_{CC3}		540	mA
	MB85227-12			495	
	MB85227-15			450	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, $\overline{CAS8}$ cycling; t_{PC} = Min.)	MB85227-10	I_{CC4}		315	mA
	MB85227-12			270	
	MB85227-15			225	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB85227-10	I_{CC5}		585	mA
	MB85227-12			540	
	MB85227-15			495	
INPUT LEAKAGE CURRENT (Except for DQ_0 to DQ_7) Input Leakage Current, Any Input ($0 \leqq V_{IN} \leqq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)1}$ ($\overline{CAS8}$, D8)	−10	10	μA
		$I_{I(L)2}$ (Others)	−90	90	
DQ and Q8 LEAKAGE CURRENT (Data out is disabled, $0V \leqq V_{OUT} \leqq 5.5V$) Each DQ is high impedance		$I_{O(L)}$	−10	10	μA
OUTPUT LEVELS Output High Voltage (I_{OH} = −5 mA) Output Low Voltage (I_{OL} = −4.2 mA)		V_{OH} V_{OL}	2.4	0.4	V

Note 1): I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

4

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB85227-10		MB85227-12		MB85227-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4		4	ms
Random Read/Write Cycle Time	4	t_{RC}	200		220		260		ns
Access Time from $\overline{\text{RAS}}$	5 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{\text{CAS}}$	6 7	t_{CAC}		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{\text{RAS}}$ Precharge Time		t_{RP}	85		90		100		ns
$\overline{\text{RAS}}$ Pulse Width		t_{RAS}	105	100000	120	100000	150	100000	ns
$\overline{\text{RAS}}$ Hold Time		t_{RSH}	55		60		75		ns
$\overline{\text{CAS}}$ Pulse Width		t_{CAS}	55	100000	60	100000	75	100000	ns
$\overline{\text{CAS}}$ Hold Time		t_{CSH}	105		120		150		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delat Time	8 9	t_{RCD}	20	50	22	60	25	75	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Set Up Time		t_{CRS}	10		10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	10	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	10	t_{RRH}	20		20		20		ns
Write Command Set Up Time		t_{WCS}	0		0		0		ns
Write Command Pulse Width		t_{WP}	15		20		25		ns
Write Command Hold Time		t_{WCH}	15		20		25		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	15		20		25		ns
Refresh Set Up Time for $\overline{\text{CAS}}$ Referenced to $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)		t_{FCS}	20		20		20		ns
Refresh Hold Time for $\overline{\text{CAS}}$ Referenced to $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)		t_{FCH}	20		25		30		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB85227-10		MB85227-12		MB85227-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time (Refresh cycles)		t_{RPC}	20		20		20		ns
Page Mode Read/Write Cycle Time	11	t_{PC}	100		120		150		ns
Page Mode $\overline{\text{CAS}}$ Precharge Time		t_{CP}	40		50		65		ns
$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)		t_{CPR}	20		25		30		ns
Write Command to $\overline{\text{RAS}}$ Lead Time	12	t_{RWL}	40		50		60		ns
Write Command to $\overline{\text{CAS}}$ Lead Time	12	t_{CWL}	40		50		60		ns
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	12	t_{CWD}	15		20		25		ns
Read-Write Cycle Time	12	t_{RWC}	200		220		260		ns

Notes:

1. An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are refrence levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time is dependent on the ambient temperature and cooling conditions.
   See Fig. 3 for durating curve.
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
8. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The minimum cycle time is dependent on the ambient temperature and cooling conditions.
    See Fig. 4 for derating curve.
12. Only for parity bit.

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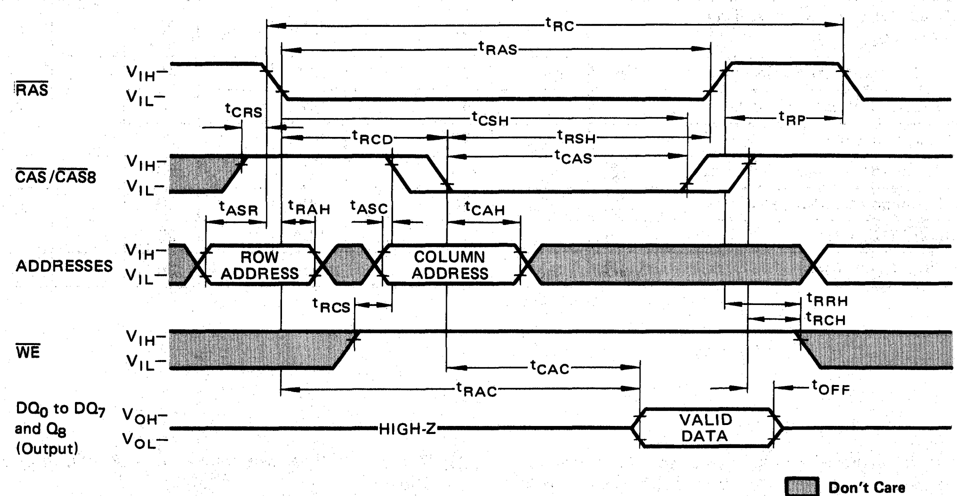
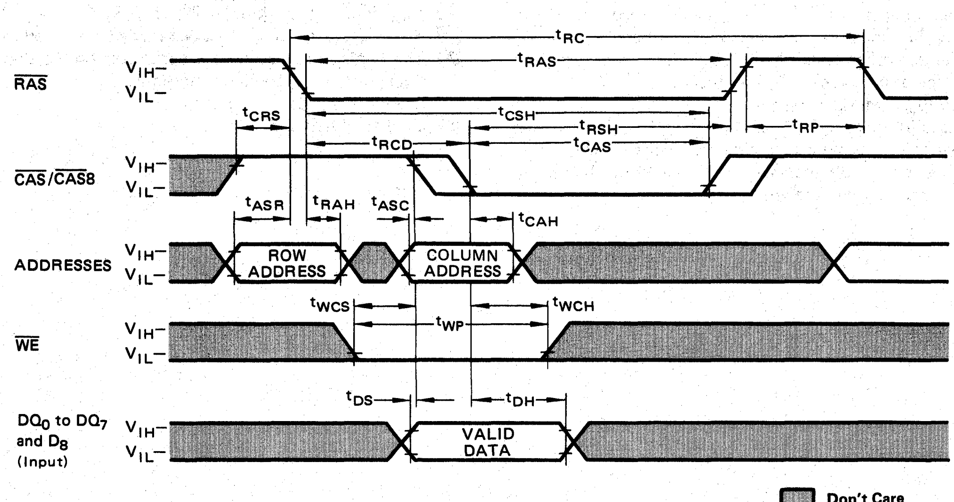
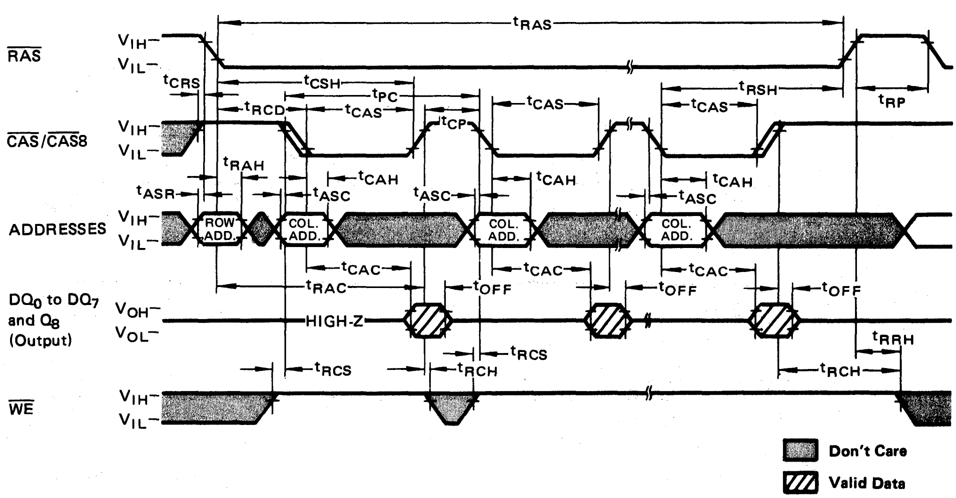
Read Cycle



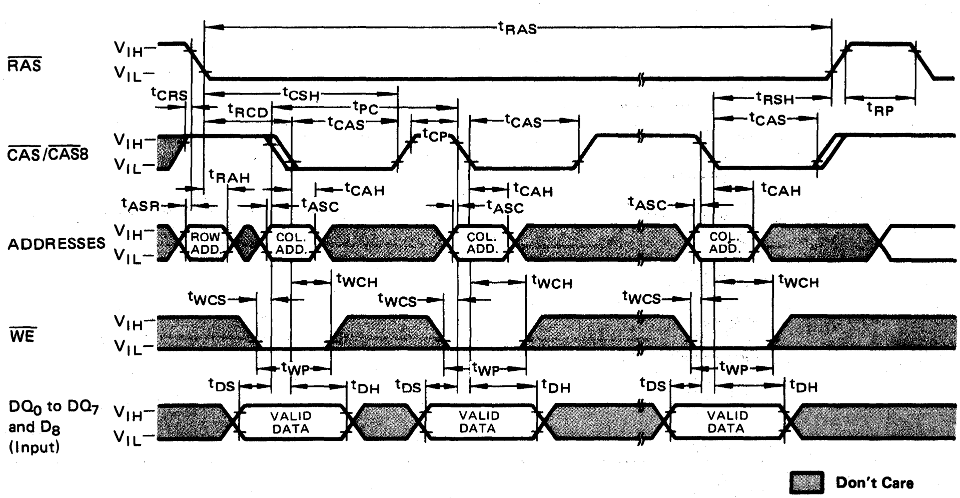
Write Cycle



Page Mode Read Cycle

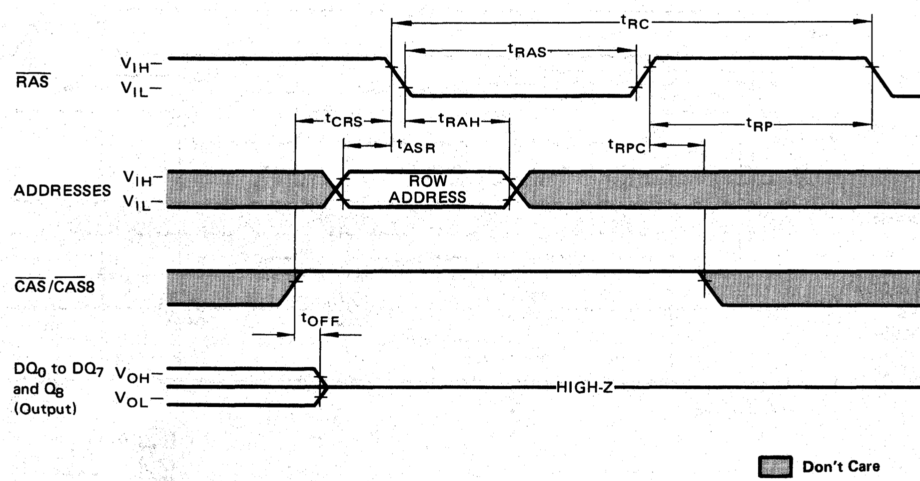


Page Mode Write Cycle



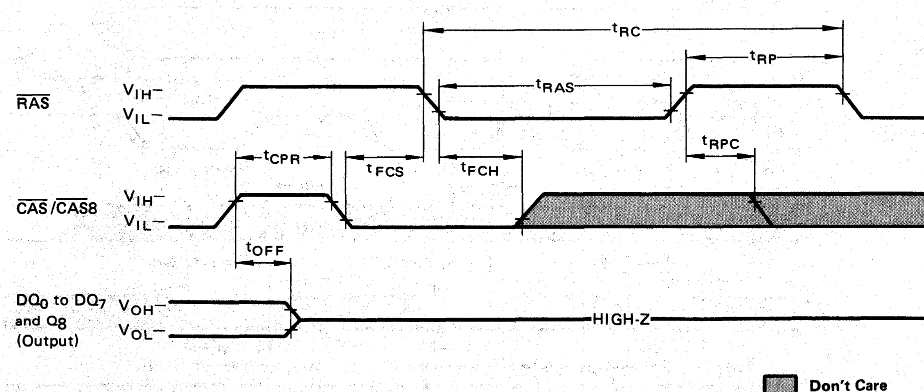
$\overline{RAS}$-only Refresh Cycle

NOTE: $\overline{WE}$, and D_8 = Don't Care

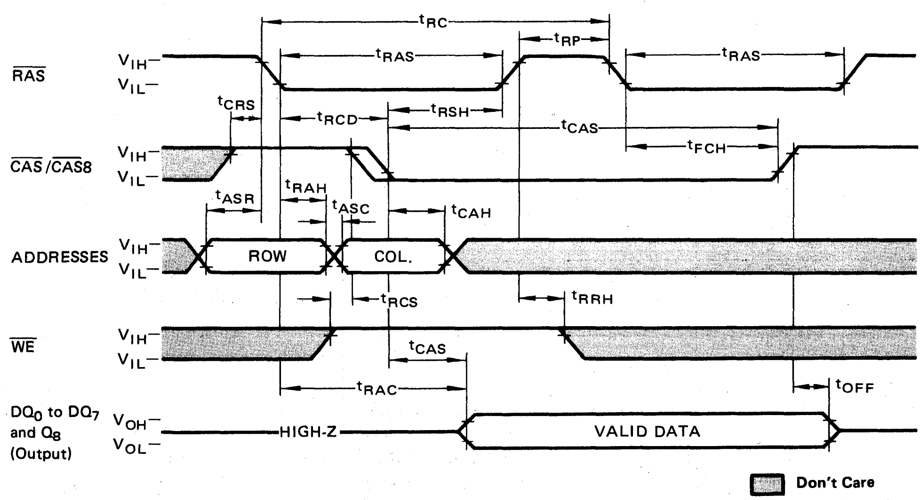


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

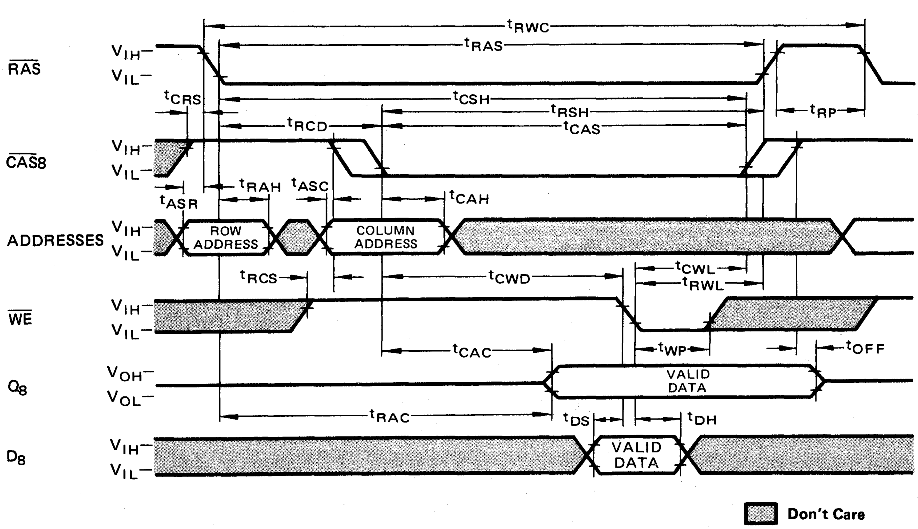
NOTE: Address, $\overline{WE}$, and D_8 = Don't Care



Hidden Refresh Cycle



Read—Write/Read—Modify—Write Cycle*



* ; Only for parity bit.

FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$ and $\overline{CAS_8}$	$\overline{WE}$	DQ_0 to DQ_7, D_8 and Q_8	Function
H	H	Don't Care	High-Z	Standby
L	L	H	Valid Data Out[1)]	Ready cycle
L	L	L	Valid Data In[2)]	Write cycle
L	L[3)]	Don't Care	High-Z	$\overline{CAS}$-before $\overline{RAS}$ Refresh cycle
L	H	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle
L	H ($\overline{CAS}$) L ($\overline{CAS_8}$)	H → L[4)]	High-Z (DQ_0 to DQ_7) Valid Data In (D_8) Valid Data Out (Q_8)	$\overline{RAS}$-only Refresh cycle (Except for Pairyt bit) Read-Write/Read-Modify-Write (Parity bit)

Notes: 1): DQ Pins are output mode.
2): DQ pins are input mode.
3): $t_{FCS} \geqq t_{FCS}$ (min)
4): $t_{CWD} \geqq t_{CWD}$ (min)

DESCRIPTION

Simple Timing Requirement:
The MB 85227 has improved circuitry that eases timing requirements for high speed access operations. The MB 85227 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 85227 has the minimal hold times of address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 85227 provides higher throughput in interleaved memory system applications. Fujitsu has made timing requirement that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, and t_{DHR}. As a result, the hold times of the column address, D_{IN} and $\overline{WE}$ are not restricted by t_{RCD}.

Address Inputs:
A total of eighteen binary input address bits are required to decode any 9 bits data of 2359296 storage cells within the MB 85227.
Nine row address bits are established on the input pin (A_0 through A_8) and latched with $\overline{RAS}$.
Nine columns address bits are established on the input pins and latched with $\overline{CAS}$ and $\overline{CAS8}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ and $\overline{CAS8}$ are internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ and $\overline{CAS8}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on the $\overline{WE}$ selects read mode, low selects write mode. Data inputs are disabled when read mode is selected.

Data Pins:
The input and output pins of each PLCC except for parity bit are directly connected on the mother board to minimized the number of I/O pins. The write cycle should be early write cycle in order to avoid data conflict between output data and input data. However, it is possible to execute read-modify-write cycle on the parity bit because the input & output of parity bit are separated.

Data Input:
The 9 bits data are written through the DQ pins (DQ_0 to DQ_7 and D_8) during write (early write) cycle.
The falling edge of $\overline{CAS}$ and $\overline{CAS8}$ are triggered for the data input register. The set up and hold times are referenced to $\overline{CAS}$ and $\overline{CAS8}$.

Data Output:
The output buffer of each chips are three state TTL compatible with a fan out of two standard TTL loads.
The outputs are in high impedance state until $\overline{CAS}$ and $\overline{CAS8}$ are brought low. In a read cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ and $\overline{CAS8}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ and $\overline{CAS8}$ are returned to a high level.

Page-Mode:
Page-mode operation permits strobing the row-address into the MB 85227 while maintaining $\overline{RAS}$ at low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each 256 row address (A_0 through A_7 of the at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8.
The MB 85227 offers the following three types of refresh.

1) $\overline{RAS}$-only Refresh;
   $\overline{RAS}$ Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ and $\overline{CAS8}$ are brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB 85227 offers an alternate refresh method. If $\overline{CAS}$ and $\overline{CAS8}$ are held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter on each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. So, by performing 256 cycles for $\overline{CAS}$-before-$\overline{RAS}$ refresh, all bits in a module are refreshed.
3) Hidden Refresh;
   Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ and $\overline{CAS8}$ active time. In MB 85227, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh address and used, that is no external refresh address is needed.

Notice for using MB 85227
The MB 85227 is a SIP (Single-In-Line-Package) module which is composed of nine MB 81256 DRAMs housed in plastic LCC, and assembled on the epoxy printed circuit board. Generally the multilayer PCB board has large wiring capacitance. This disadvantage causes relatively noise induction between signal lines and power supply lines (V_{SS} or V_{CC}).
Furthermore, as the MB 85227 is a very high-speed memory, the timing windows to strobe address $\overline{WE}$ and D_{IN} signals are very short (Approx. 5 ns). Therefore, it is very sensitive even to very sharp noise.
From the above reasons, special care should be taken for use the MB 85227. The following notices are recommended;

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DESCRIPTION

1. Provide a externally capacitor of approx. a few μF each module, the MB 85227 has the nine decoupling capacitors (0.22 μF on each module 0.22 μF x 9).
2. Remove noise, riging, overshoot and undershoot from the address, clocks and DQ lines, so that the MB 85227 won't latch wrong signals due to the noise induction between signal lines and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. Provide an appropriate dumping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

Fig. 3 — MB 85227 DERATING CURVE (Normal Cycle)

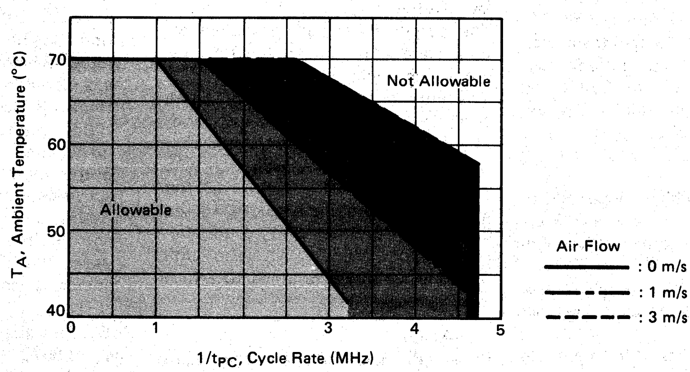
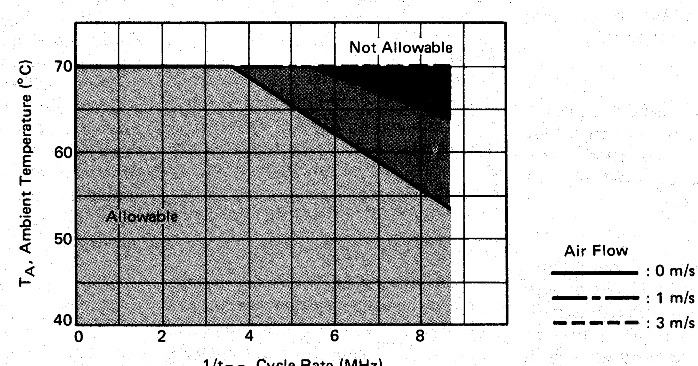


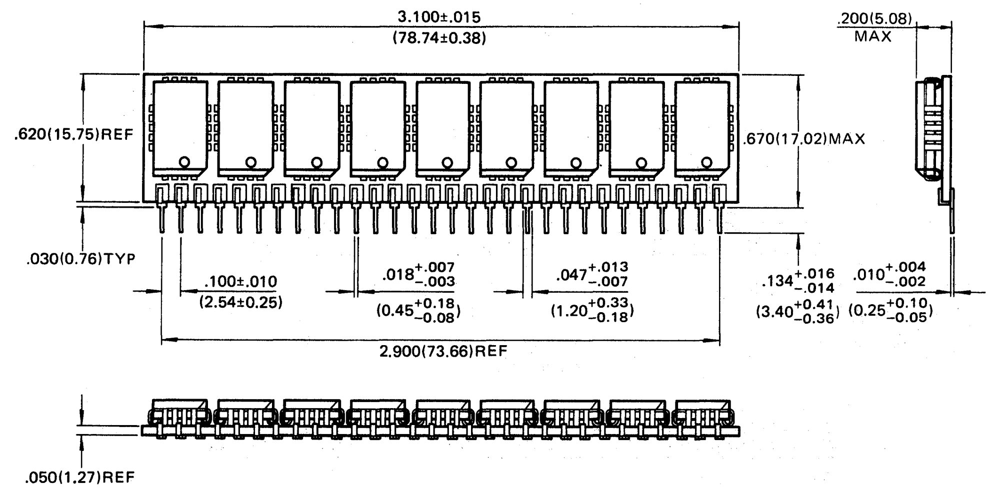
Fig. 4 — MB 85227 DERATING CURVE (Page Mode Cycle)



4

PACKAGE DIMENSIONS

30-LEAD SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSP-30P-P02)



Dimensions in
inches (millimeters)

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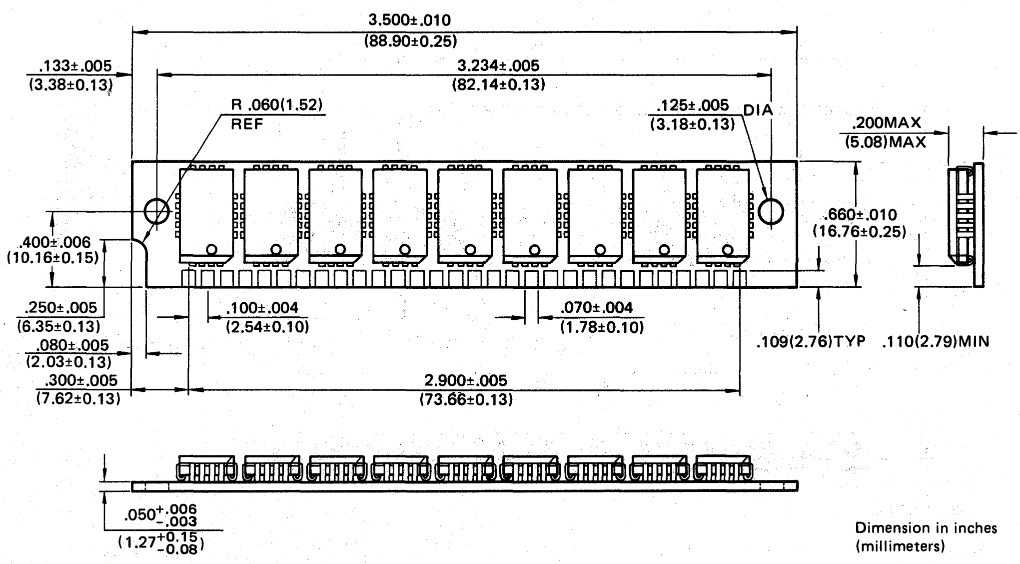
PACKAGE DIMENSIONS

**30-PAD PLASTIC SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSS-30P-P01)**



Dimension in inches (millimeters)

FUJITSU

1,048,576 × 8 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

MB85230-10
MB85230-12

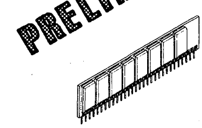
May 1988
Edition 1.0

1M x 8 BIT DYNAMIC RANDOM ACCESS MEMORY SIP MODULE

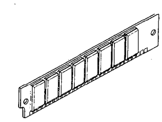
PRELIMINARY

The Fujitsu MB85230 is a fully decoded, dynamic CMOS random access memory modulew with eight MB81C1000, in 26-pin SOJ packages, and eight .22µF decoupling capacitor under the each memory, mounted on a 30-pin SIP or a 30-pad SIMM module. Organized as 1,048,576 x 8-bit words, the MB85230 PCB module is optimized for those applications requiring high density and large memory storage capability. The operation and electrical characteristics of the MB85230 are the same as the MB81C1000 devices which feature a Fast Page mode operation.

- 1,048,576 x 8 DRAM, 30-pin SIP and SIMM
- Row access time (t_{RAC}):
  100 ns max. (MB85230-10)
  120 ns max. (MB85230-12)
- Cycle time (t_{RC}):
  180 ns min. (MB85230-10)
  210 ns max. (MB85230-12)
- Column access time (t_{CAC}):
  30 ns max. (MB85230-10)
  35 ns max. (MB85230-12)
- Fast Page mode cycle time (t_{PC}):
  60 ns max. (MB85230-10)
  70 ns max. (MB85230-12)
- Dual +5V supply, ±10% tolerance
- Low power:
  Active = 2640 mW max. (MB85230-10)
  2200 mW max. (MB85230-12)
  Standby = 44 mW max. (CMOS level)
- Refresh:
  - 8.2 ms / 512 refresh cycle
  - "$\overline{RAS}$-only", "$\overline{CAS}$-before-$\overline{RAS}$" and "Hidden" refresh capabilities
- TTL compatible inputs and outputs
- Leaded and Leadless type are available.
- JEDEC standard (30-pin SIP) pin assignment



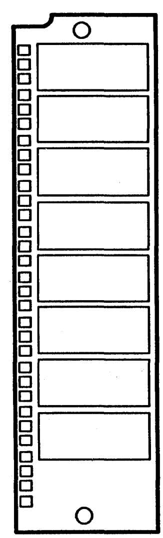
MSP-30P-P05



MSS-30P-P04

PIN ASSIGNMENT

VCC	1
$\overline{CAS}$	2
DQ0	3
A0	4
A1	5
DQ1	6
A2	7
A3	8
VSS	9
DQ2	10
A4	11
A5	12
DQ3	13
A6	14
A7	15
DQ4	16
A8	17
A9	18
NC	19
DQ5	20
$\overline{WE}$	21
VSS	22
DQ6	23
NC	24
DQ7	25
NC	26
$\overline{RAS}$	27
NC	28
NC	29
VCC	30



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	8.0	W
Short circuit output current	—	50	mA

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Fig. 1 – BLOCK DIAGRAM

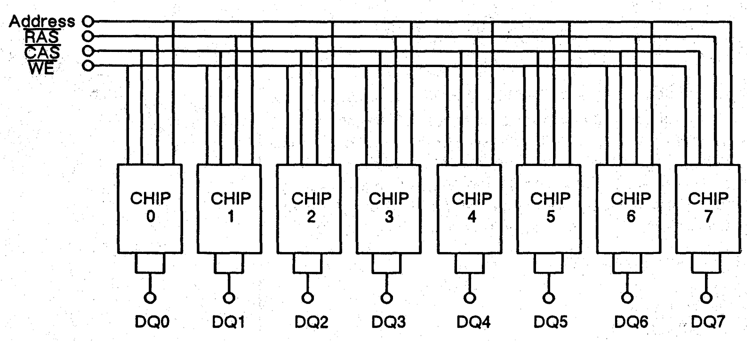
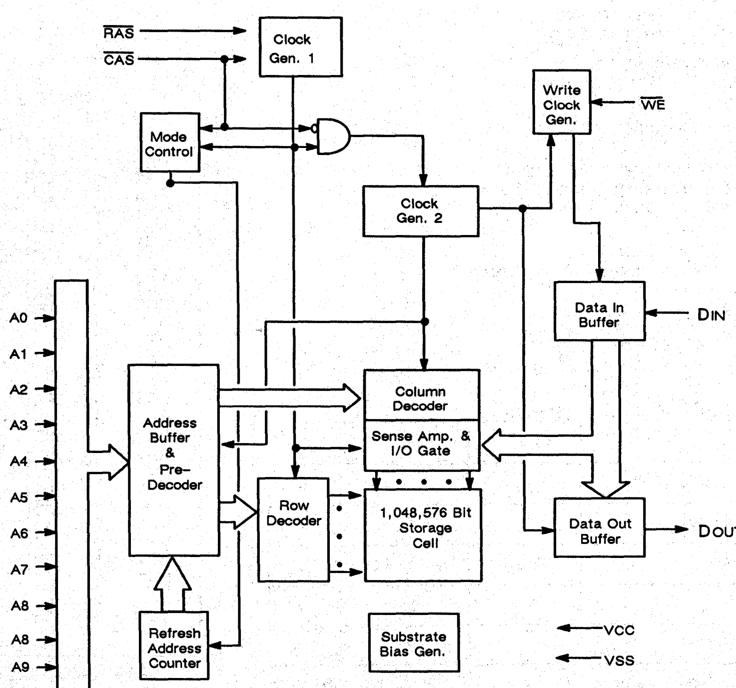


Fig. 2 – BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Value		Unit
		Typ	Max	
Address Input Capacitance	C_{IN1}		56	pF
$\overline{RAS}$ pin Capacitance	C_{IN2}		47	pF
$\overline{CAS}$ pin Capacitance	C_{IN3}		49	pF
$\overline{WE}$ pin Capacitance	C_{IN4}		46	pF
DQ pin Capacitance	C_{DQ}		14	pF

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RECOMMENDED OPERATING CONDITIONS

(Referenced to Vss)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input High Level	V_{IH}	2.4		6.5	V
Input Low Level, all inputs all DQs	V_{IL1} V_{IL2}	-2.0 -1.0 *1		0.8 0.8	V V
Operating Temperature	T_A	0	25	70 *2	V

Note: *1 The device will withstand undershoots to the -2.0V level with a maximum pulse width of 20ns at the -1.5V level.
*2 Maximum ambient temperature is permissible under certain conditions.

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value Min	Value Typ	Value Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}=min.)	-10	I_{CC1}			480	mA
	-12				400	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	TTL	I_{CC2}			16	mA
	CMOS				8	
REFRESH CURRENT 1 Average Power Supply Current ($\overline{CAS}$=V_{IH}; $\overline{RAS}$=min cycling)	-10	I_{CC3}			440	mA
	-12				360	
FAST PAGE CURRENT Average Power Supply Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$=min cycling)	-10	I_{CC4}			320	mA
	-12				264	
REFRESH CURRENT 2 Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC}=min)	-10	I_{CC5}			440	mA
	-12				360	
INPUT LEAKAGE CURRENT		I_{IL}	-30		30	µA
OUTPUT LEAKAGE CURRENT		I_{OL}	-10		10	µA
OUTPUT HIGH LEVEL (I_{OH}=-5MA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=4.2mA)		V_{OL}			0.4	V

Note: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(At recommended operating conditions otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85230-10 Min.	MB85230-10 Max.	MB85230-12 Min.	MB85230-12 Max.	Unit
Time Between Refresh		t_{REF}		8.2		8.2	ms
Random Read/Write Cycle Time	4	t_{RC}	180		210		ns
Access Time from $\overline{RAS}$	5,8	t_{RAC}		100		120	ns
Access Time from $\overline{CAS}$	6,8	t_{CAC}		30		35	ns
Access Time from Column Address	7,8	t_{AA}		50		60	ns
Output Data Hold Time		t_{OH}	7		7		ns
Output Buffer Turn On Delay Time		t_{ON}	5		5		ns
Output Buffer Turn Off Delay Time	9	t_{OFF}		25		25	ns
Input Transition Time		t_{T}	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	70		80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	100000	120	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	30		35		ns
$\overline{CAS}$ to RAS Precharge Time		t_{CRP}	0		0		ns
$\overline{RAS}$ to CAS Delay Time	10,11	t_{RCD}	25	70	25	85	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	30		35		ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		ns
Row Address Setup Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	15		15		ns
Column Address Setup Time		t_{ASC}	0		0		ns
Column Address Setup Time		t_{CAH}	15		20		ns
$\overline{RAS}$ to Column Address Delay Time	12	t_{RAD}	20	50	20	60	ns
Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	50		60		ns
Read Command Setup Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0		0		ns
Write Command Setup Time	14	t_{WCS}	0		0		ns
Write Command Hold Time		t_{WCH}	15		20		ns
$\overline{WE}$ Pulse Width		t_{WP}	15		20		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25		30		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		25		ns
DIN Setup Time		t_{DS}	0		0		ns
DIN Hold Time		t_{DH}	15		20		ns
Fast Page Mode Read/Write Cycle Time		t_{PC}	60		70		ns
Access Time from $\overline{CAS}$ Precharge	8,15	t_{CPA}		60		70	ns
Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15		15		ns

4

AC CHARACTERISTICS (Continued)

(At recommended operating conditions otherwise noted.) Notes 1, 2, 3

Parameter NOTES	Symbol	MB85230-10		MB85230-12		Unit
		Min.	Max.	Min.	Max.	
$\overline{CAS}$ Precharge Time	t_{CPN}	15		15		ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	t_{RPC}	0		0		ns
$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CSR}	0		0		ns
$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	15		20		ns

NOTES:

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200 µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T=5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time depends upon the ambient temperature and cooling condition. See Fig. 3 and 4.
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 5 and 6.
6. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA}-t_{CAS}-t_T$, access time is t_{CAC}.
7. If $t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \geq t_{AA}-t_{CAS}-t_T$, access time is t_{AA}.
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. t_{OFF} is specified that output buffer changes to high impedance state.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RAC} (max) is specifies as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAS} or t_{AA}.
11. t_{RCD} (min) = t_{RAH} (min) $+2t_T + t_{ASC}$ (min).
12. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WCS} is specified as a reference point only and must be satisfied for a write cycle.
15. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from V_{IL} to V_{IH}.). Therefore, if t_{CP} is short, t_{CAC} is longer than t_{CAC} (max).

Fig. 3 – MB85230 DERATING CURVE (Normal Cycle)

T.B.D.

Fig. 4 – MB85230 DERATING CURVE (Fast Page Mode Cycle)

T.B.D.

Fig. 5 – t_{RAC} vs t_{RCD}

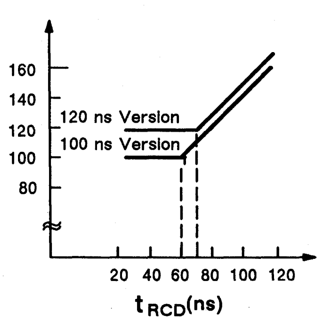
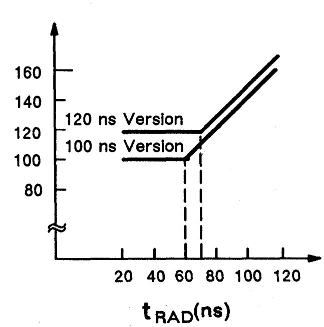
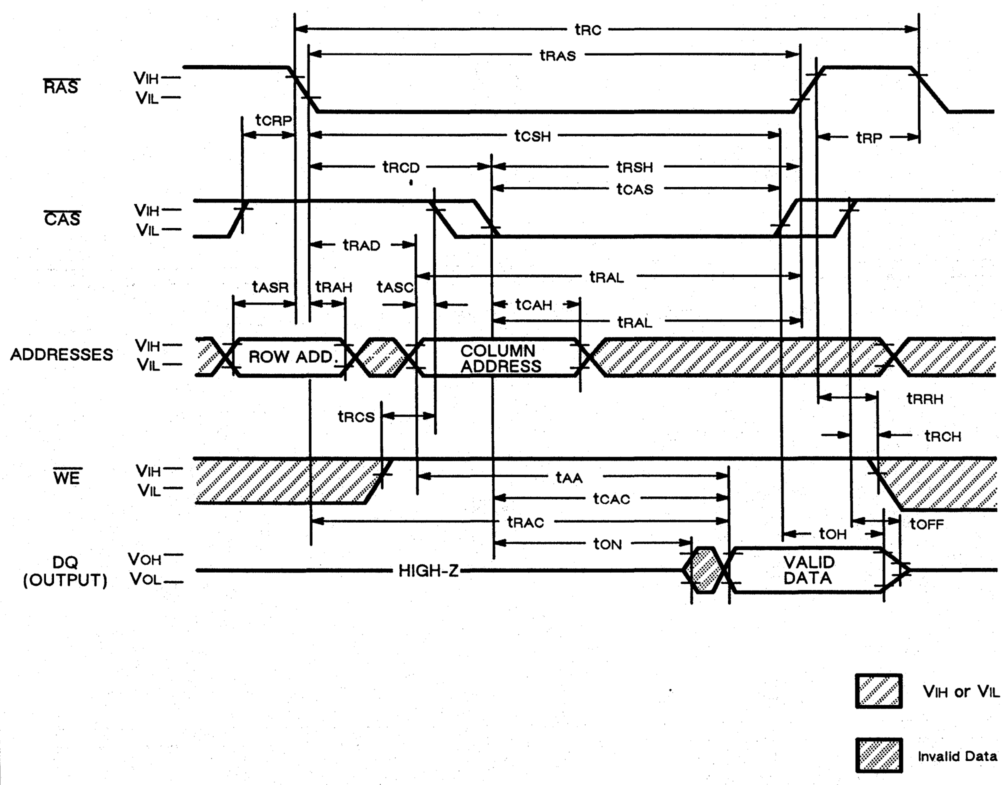


Fig. 6 – t_{RAC} vs t_{RAD}

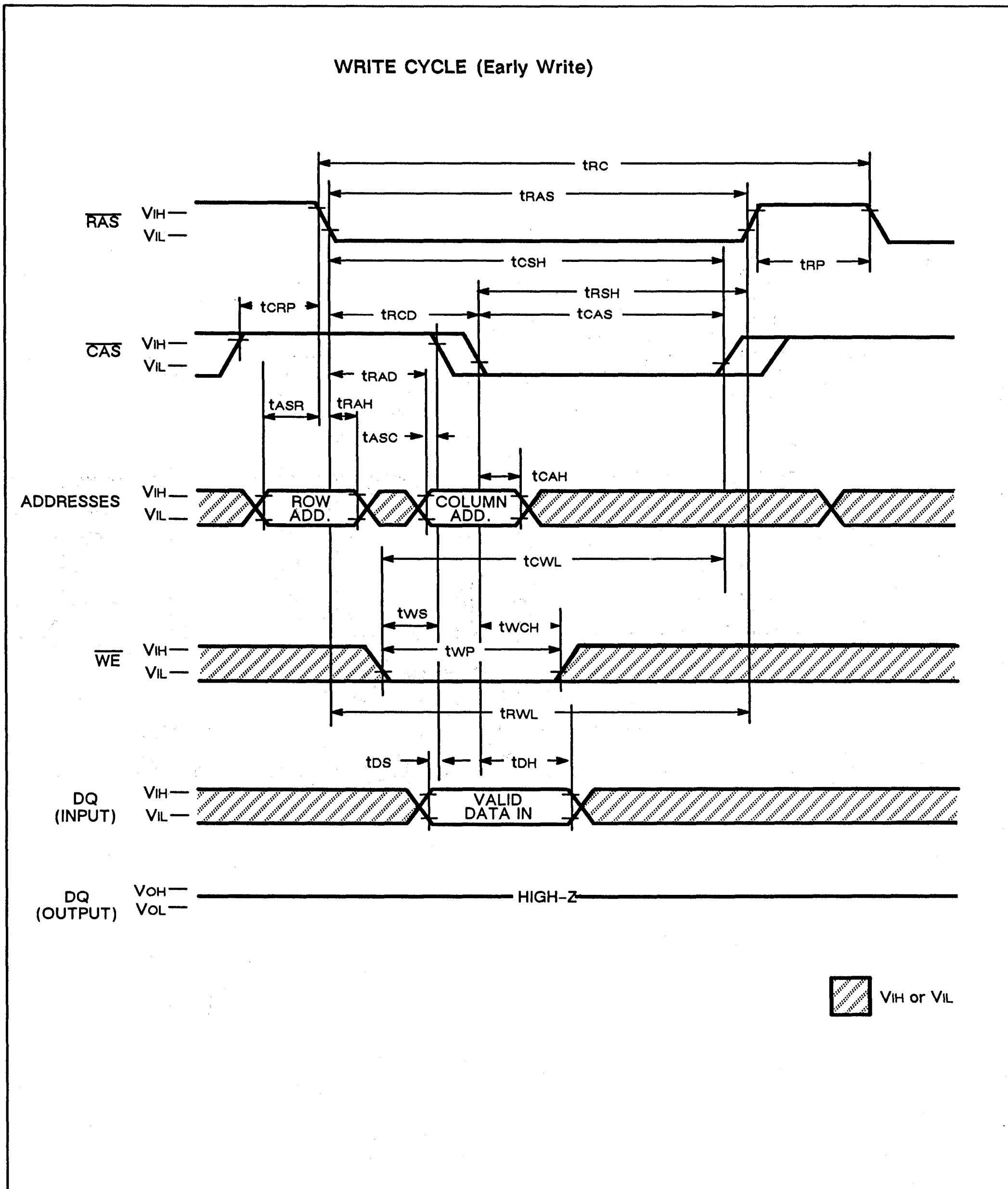


4

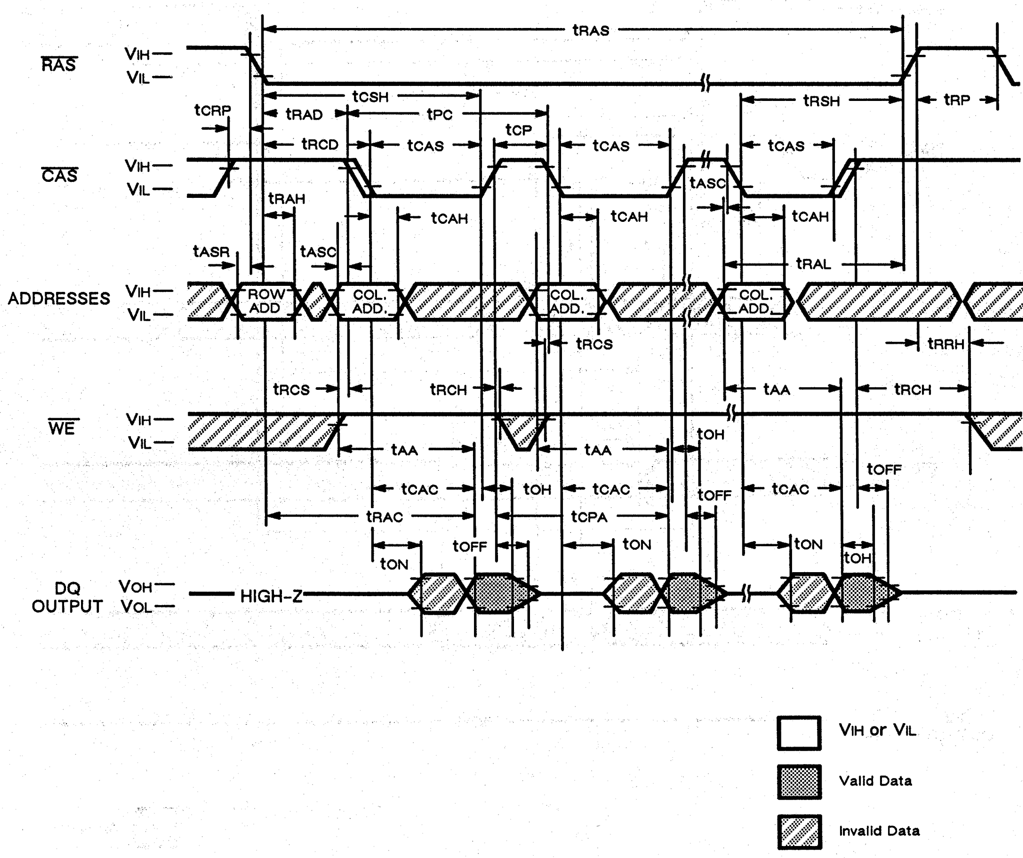
READ CYCLE


tRC
tRAS
RAS
VIH
VIL
tCRP
tCSH
tRP
tRCD
tRSH
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
ADDRESSES
ROW ADD.
COLUMN ADDRESS
tRRH
tRCS
tRCH
WE
tAA
tCAC
tRAC
tOH
tOFF
tON
DQ (OUTPUT)
VOH
VOL
HIGH-Z
VALID DATA
VIH or VIL
Invalid Data

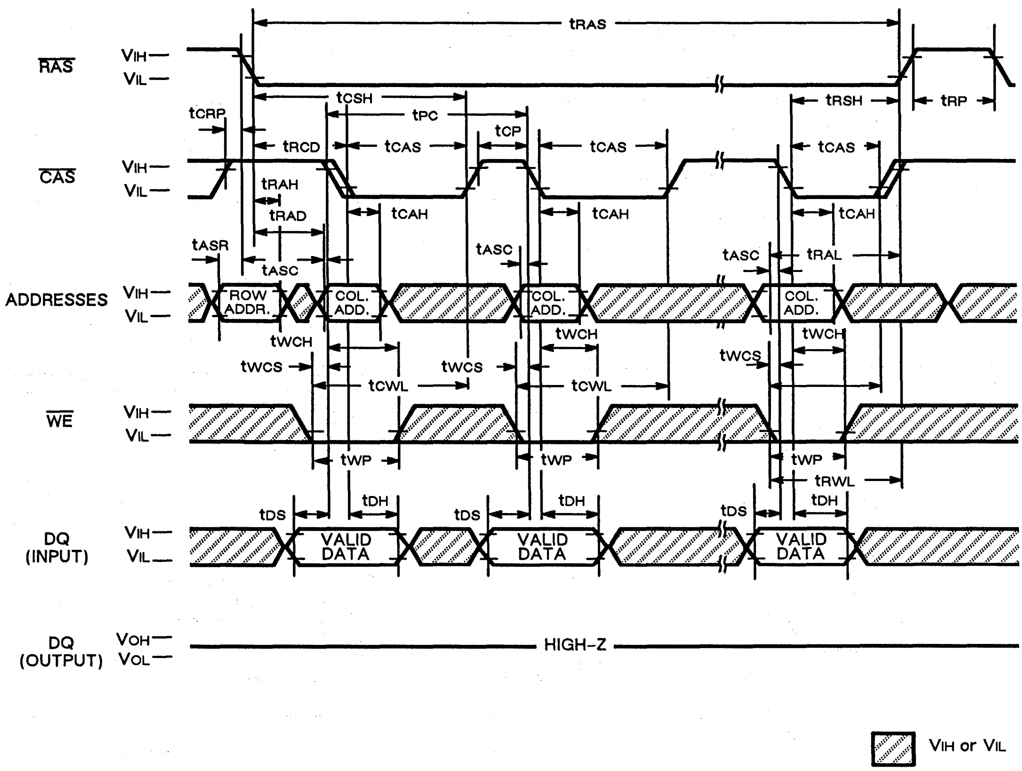
4


WRITE CYCLE (Early Write)
tRC
tRAS
tCSH
tRP
tRSH
tCRP
tRCD
tCAS
tRAD
tASR
tRAH
tASC
tCAH
RAS
CAS
ADDRESSES
WE
DQ (INPUT)
DQ (OUTPUT)
VIH
VIL
VOH
VOL
ROW ADD.
COLUMN ADD.
tCWL
tWS
tWCH
tWP
tRWL
tDS
tDH
VALID DATA IN
HIGH-Z
VIH or VIL

FAST PAGE MODE READ CYCLE



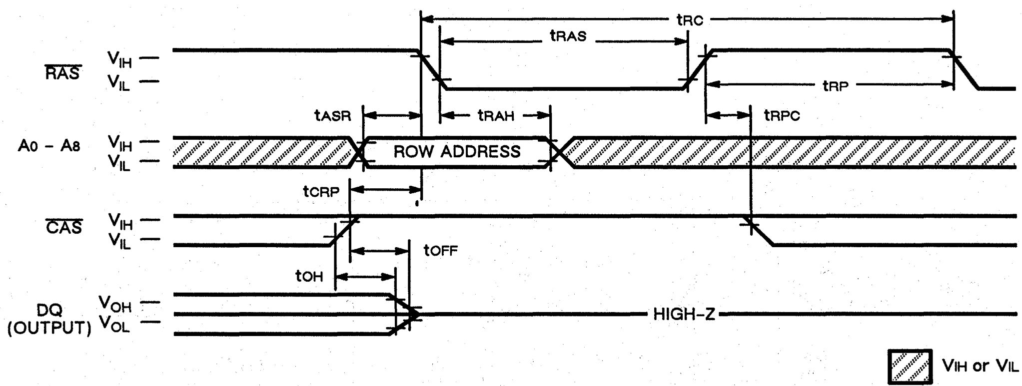
FAST PAGE MODE WRITE CYCLE



4

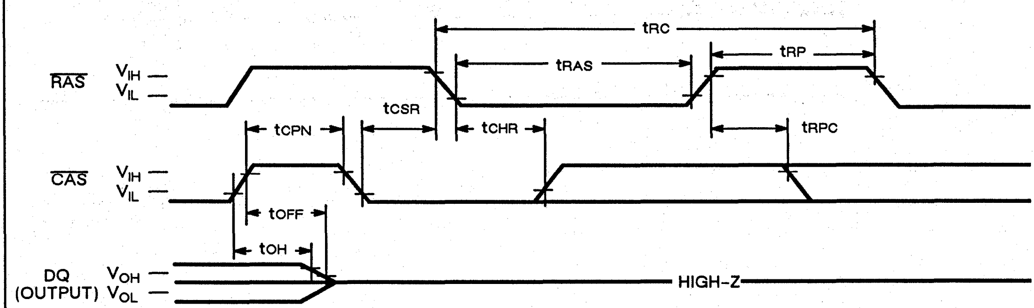
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

NOTE : $\overline{\text{WE}}$, DQ(Input)=Don't care, A9 = VIH or VIL

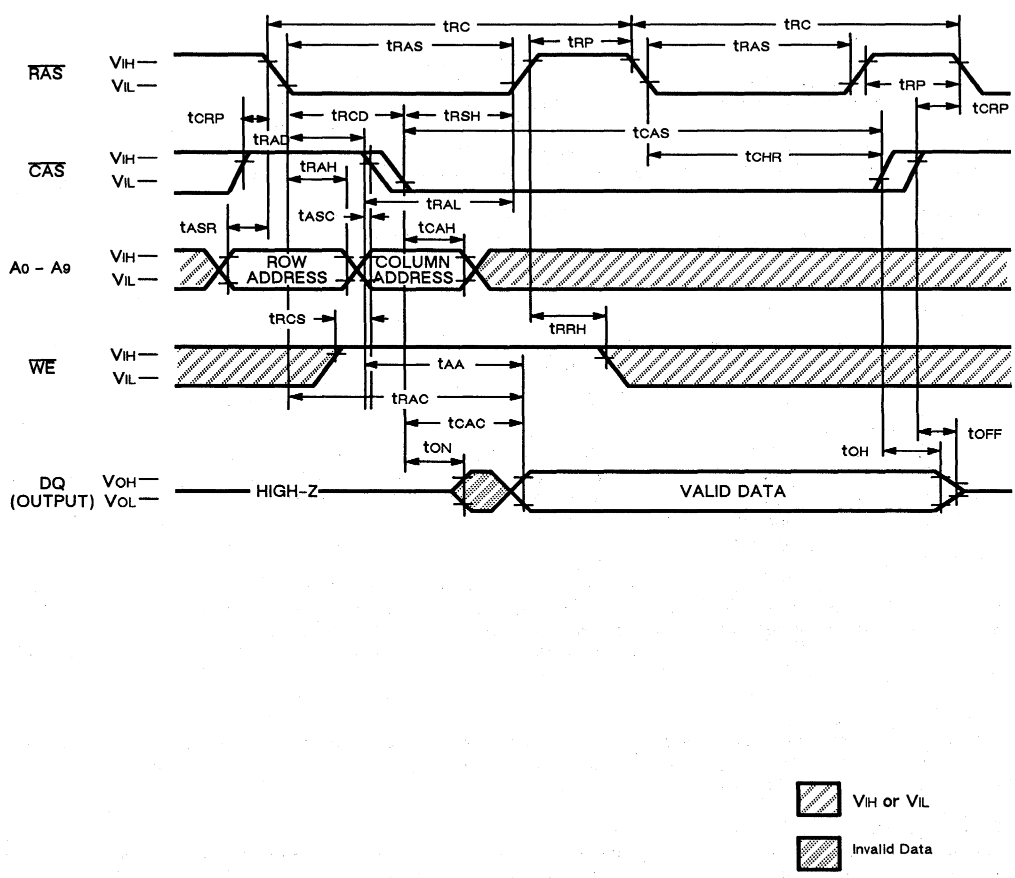


$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

NOTE: ADDRESS, $\overline{\text{WE}}$, DIN = Don't Care



HIDDEN REFRESH CYCLE



DESCRIPTION

Block Analysis:

As shown in Fig. 1 and Fig. 2, the MB85230 is composed of eight MB81C1000, and the memory selection of the each MB81C1000 consists of a 1024-by-1024 cell matrix.
Operational modes of the device are shown in the FUNCTIONAL TRUTH TABLE below.

Address Inputs:

A total of twenty binary input address bits are required to decde any 8-bit of the 8,388,608 storage cells within the MB85230. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe, $\overline{RAS}$. The ten column address bits are established on the address input pins(A_0 to A_9) and latched with the Column Address Strobe, $\overline{CAS}$. All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min)+ t_T. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occurs later.

Write Enable:

Read or Write mode is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write mode.

Data Input/Output:

1. **Data Input;**
   In write cycle, the 8-bit data is written into the MB85230 during write cycle through each DQ pins. Each input data is strobed and latched by falling edge of $\overline{CAS}$, and $\overline{WE}$ must be brought to V_{IL} before falling edge of $\overline{CAS}$, data input strobed by $\overline{CAS}$, and setup and hold times are referenced to $\overline{CAS}$.

2. **Data Output;**
   The output buffers on each chip are three state TTL compatible with a fan out of 2 TTL loads. Output data has the same porality as input data. The outputs are in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid within t_{CAC} or t_{AA} whichever occurs later after falling edge of $\overline{CAS}$.
   The data output remans valid until $\overline{CAS}$ returns to high.

Read Cycle:

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}=V_{IL}$ and keeping $\overline{WE}=V_{IH}$ throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The output data is remain valid with $\overline{CAS}=V_{IL}$, i.e., if $\overline{CAS}$ goes V_{IH}, the data becomes invalid with t_{OH}. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$(t_{CAC}), or Column address input (t_{AA}). If t_{RCD}($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}.

Write Cycle:

The write cycle is executed is executed by the same manner as read cycle except for the state of $\overline{WE}$. The 8-bit data on DQ pins are latched with the falling edge of $\overline{CAS}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL}, and t_{RAL} must be satisfied the specifications.

Fast Page Mode Read Cycle:

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}=V_{IL}$, applying column address and $\overline{CAS}$, and keeping $\overline{WE}=V_{IH}$. Since the row address during fast page mode cycle is latched by normal cycle, the cycle time is reduced. During this mode, the access time is t_{CAC}, t_{AA}, or t_{CPA}, whichever occur later. Any of the 1024 bits belonging to each internal row address can be accessed.

Fast Page Mode Write Cycle:

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of WE. The data on each DQ is latched with the falling edge of $\overline{CAS}$ and written into the memory. During this write cycle, t_{CWL} must be satisfied. Any of 1024 bits belonging to each internal row address can be accessed.

DESCRIPTION (Continued)

Refresh:
The refresh of DRAM is executed by normal read and write cycle, i.e., the cells on each one row line, A_0 through A_8 except for A_9, are refreshed by one of two cycles. Each 512 row address must be refreshed every 8.2ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB85230 also has three types of refresh modes, $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden refresh.

1. **$\overline{RAS}$-only Refresh;**
   The $\overline{RAS}$-only refresh is executed by keeping $\overline{RAS}=V_{IL}$ and keeping $\overline{CAS}=V_{IH}$ through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During this refresh, the DQ pins are kept high impedance state.

2. **$\overline{CAS}$-before-$\overline{RAS}$ Refresh;**
   The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}=V_{IL}$ before $\overline{RAS}$. By this combination, the MB85230 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

3. **Hidden Refresh;**
   The hidden refresh is execute dby keeping $\overline{CAS}=V_{IL}$ to next cycle during read mode, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept V_{IL} continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data I/O	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column		
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	Cells are not refreshed.
Read (Normal)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min)
Read (Fast Page)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min) Cells are not refreshed.
Write (Normal)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min)
Write (Fast Page)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min) Cells are not refreshed.
$\overline{RAS}$-only Refresh	V_{IL}	V_{IH}	X	Valid	X	High-Z	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	V_{IL}	V_{IL}	X	X	X	High-Z	$t_{CRS} \geq t_{CRS}$ (min)
Hidden Refresh	V_{IL} *	V_{IL}	V_{IH}	X	X	Output Valid	Previous data is kept.

Note: X: Don't Care
*; $\overline{RAS}$ puts V_{IH} at once.

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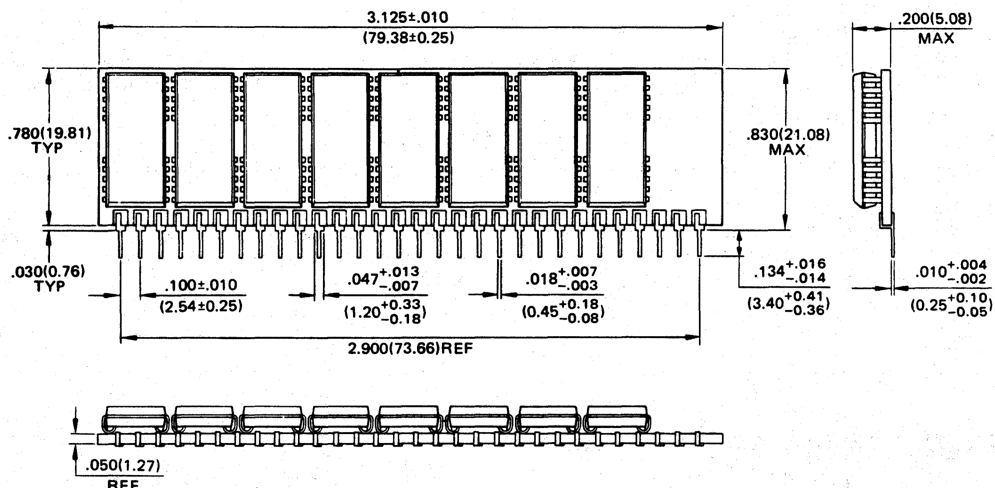
PACKAGE DIMENSIONS

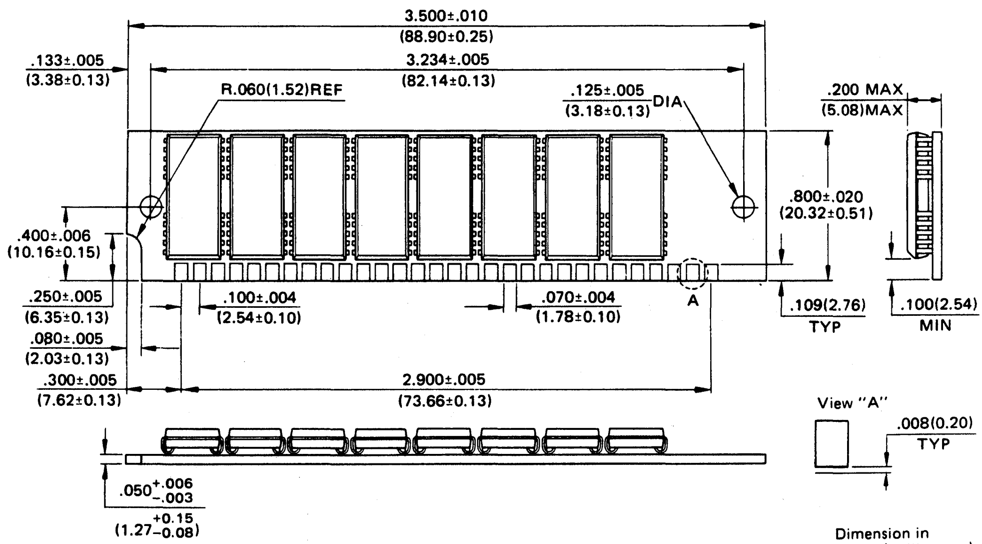
30-LEAD PLASTIC SINGLE-IN-LINE PACKAGE MODULE
(CASE No.: MSP-30P-P05)



Dimension in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

**30-PAD PLASTIC SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSS-30P-P04)**



Dimension in inches (millimeters)

4

FUJITSU

1M x 9 DRAM MODULE

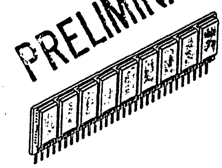
MB85235-10
MB85235-12

1,048,576 x 9 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

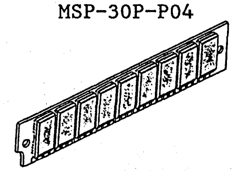
TS028-B87Z
Dec. 1987

PRELIMINARY

The Fujitsu MB85235 is a fully decoded, dynamic CMOS random access memory module with eight MB81C1000, in 26-pin SOJ packages, and nine .22µF decoupling capacitors under the each memory, mounted on a 30-pin SIP or a 30-pad SIMM module. Organized as 1,048,576 x 9-bit words, the MB85235 PCB module is optimized for those applications requiring high density and large memory storage capability. The operation and electrical characteristics of the MB85235 are the same as the MB81C1000 devices which feature a Fast Page mode operation.



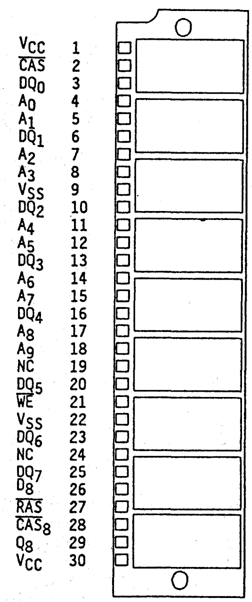
PLASTIC PACKAGE
MSP-30P-P04



PLASTIC PACKAGE
MSS-30P-P03

- 1,048,576 x 9 DRAM, 30-pin SIP and SIMM
- RAS access time (t_{RAC}):
  - 100 ns max. (MB85235-10)
  - 120 ns max. (MB85235-12)
- Cycle time (t_{RC}):
  - 180 ns min. (MB85235-10)
  - 210 ns max. (MB85235-12)
- Column access time (t_{CAC}):
  - 30 ns max. (MB85235-10)
  - 35 ns max. (MB85235-12)
- Fast Page mode cycle time (t_{PC}):
  - 60 ns max. (MB85235-10)
  - 70 ns max. (MB85235-12)
- Dual +5V supply, ±10% tolerance
- Low power:
  - Active = 2970 mW max. (MB85235-10)
  - 2475 mW max. (MB85235-12)
  - Standby = 49.5 mW max. (CMOS level)
- Refresh:
  - 8.2 ms / 512 refresh cycle
  - "RAS-only", "CAS-before-RAS" and "Hidden" refresh capability
- Fast Page Mode Read and Write capability
- Leaded and Leadless type are available.
- JEDEC standard (30 pin SIP) pin assignment

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	9.0	W
Short circuit output current	—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 - BLOCK DIAGRAM

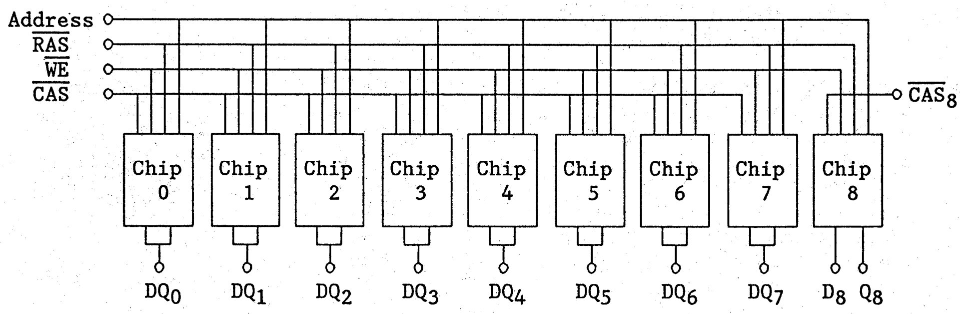
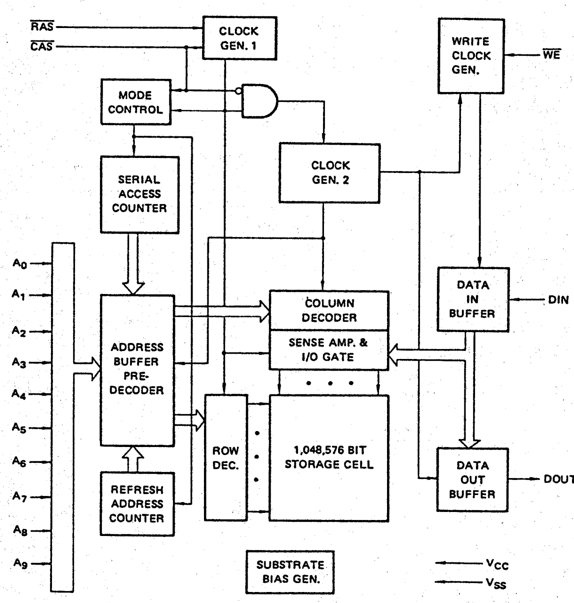


Fig. 2 - BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_9	C_{IN1}	–	60	pF
Input Capacitance, RAS	C_{IN2}	–	49	pF
Input Capacitance, CAS	C_{IN3}	–	49	pF
Input Capacitance, WE	C_{IN4}	–	48	pF
Input Capacitance, CAS_8	C_{IN5}	–	9	pF
Input Capacitance, D_8	C_D	–	7	pF
I/O Capacitance, DQ_0 to DQ_7	C_{DQ}	–	14	pF
Output Capacitance, Q_8	C_O	–	10	pF

4

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input High Level, all inputs	V_{IH}	2.4		6.5	V
Input Low Level, all inputs all DQs	V_{IL1} V_{IL2}	-2.0 -1.0*1		0.8 0.8	V V
Operating Temperature Range	T_A	0	25	70*2	°C

Note: *1 The device will withstand undershoots to the -2.0V level with a maximum pulse width of 20ns at the -1.5V level.
*2 Maximum ambient temperature is permissible under certain conditions.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}=min.)	MB85235-10	I_{CC1}			540	mA
	MB85235-12				450	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	TTL level	I_{CC2}			18	mA
	CMOS level				9	
REFRESH CURRENT 1 Average Power Supply Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$=min cycling)	MB85235-10	I_{CC3}			495	mA
	MB85235-12				405	
FAST PAGE MODE CURRENT Average Power Supply Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$=min cycling)	MB85235-10	I_{CC4}			360	mA
	MB85235-12				297	
REFRESH CURRENT 2 Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC}=min)	MB85235-10	I_{CC5}			495	mA
	MB85235-12				405	
INPUT LEAKAGE CURRENT, all inputs		I_{IL1}	-30		30	µA
INPUT LEAKAGE CURRENT, $\overline{CAS}_8$ and D_8		I_{IL2}	-10		10	µA
OUTPUT LEAKAGE CURRENT		I_{OL}	-10		10	µA
OUTPUT HIGH LEVEL (I_{OH}=-5mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=4.2mA)		V_{OL}			0.4	V

Note: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85235-10 Min	MB85235-10 Max	MB85235-12 Min	MB85235-12 Max	Unit
Time Between Refresh		t_{REF}		8.2		8.2	ms
Random Read/Write Cycle Time	4	t_{RC}	180		210		ns
Access Time from RAS	5,8	t_{RAC}		100		120	ns
Access Time from CAS	6,8	t_{CAC}		30		35	ns
Access Time from Column Address	7,8	t_{AA}		50		60	ns
Output Data Hold Time		t_{OH}	10		10		ns
Output Buffer Turn On Delay Time		t_{ON}	5		5		ns
Output Buffer Turn Off Delay Time	9	t_{OFF}		25		25	ns
Input Transition Time		t_T	3	50	3	50	ns
RAS Precharge Time		t_{RP}	70		80		ns
RAS Pulse Width		t_{RAS}	100	100000	120	100000	ns
RAS Hold Time		t_{RSH}	30		35		ns
CAS to RAS Precharge Time		t_{CRP}	0		0		ns
RAS to CAS Delay Time	10,11	t_{RCD}	20	70	20	85	ns
CAS Pulse Width		t_{CAS}	30		35		ns
CAS Hold Time		t_{CSH}	100		120		ns
Row Address Setup Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	15		15		ns
Column Address Setup Time		t_{ASC}	0		0		ns
Column Address Setup Time		t_{CAH}	15		20		ns
RAS to Column Address Delay Time	12	t_{RAD}	20	50	20	60	ns
Column Address to RAS Lead Time		t_{RAL}	50		60		ns
Read Command Setup Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to RAS	13	t_{RRH}	0		0		ns
Read Command Hold Time Referenced to CAS	13	t_{RCH}	0		0		ns
Write Command Setup Time	14	t_{WCS}	0		0		ns
Write Command Hold Time		t_{WCH}	15		20		ns
WE Pulse Width		t_{WP}	15		20		ns
Write Command to RAS Lead Time		t_{RWL}	25		30		ns
Write Command to CAS Lead Time		t_{CWL}	20		25		ns
DIN Setup Time		t_{DS}	0		0		ns
DIN Hold Time		t_{DH}	15		20		ns
Fast Page Mode Read/Write Cycle Time		t_{PC}	60		70		ns
Access Time from CAS Precharge	8,15	t_{CPA}		60		70	ns
Fast Page Mode CAS Precharge Time		t_{CP}	15		15		ns
CAS Precharge Time		t_{CPN}	15		15		ns
RAS Precharge Time to CAS Active Time (Refresh Cycles)		t_{RPC}	0		0		ns
CAS Setup Time for CAS-before-RAS Refresh		t_{CSR}	0		0		ns
CAS Hold Time for CAS-before-RAS Refresh		t_{CHR}	15		20		ns

AC CHARACTERISTICS (Cont'd)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter NOTES	Symbol	MB85235-10		MB85235-12		Unit
		Min	Max	Min	Max	
Read-Modify-Write Cycle Time 16	t_{RWC}	210		245		ns
Fast Page Mode Read-Modify-Write Cycle Time 16	t_{PRWC}	85		100		ns
RAS to WE Delay Time 14,16	t_{RWD}	100		120		ns
CAS to WE Delay Time 14,16	t_{CWD}	30		35		ns
Column Address to WE delay Time 14,16	t_{AWD}	50		60		ns

NOTES;

1. An initial pause ($\overline{RAS}=\overline{CAS}/\overline{CAS_8}=V_{IH}$) of 200 µs is required after power-up followed by any 8 $\overline{RAS}$-only cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T=5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time depends upon the ambient temperature and cooling condition. See Fig.4.
5. Assumes that $t_{RCD} \le t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
6. If $t_{RCD} \ge t_{RCD}$ (max), $t_{RAD} \ge t_{RAD}$ (max), and $t_{ASC} \ge t_{AA}-t_{CAC}-t_T$, access time is t_{CAC}.
7. If $t_{RAD} \ge t_{RAD}$ (max), $t_{ASC} \ge t_{AA}-t_{CAC}-t_T$, access time is t_{AA}.
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. t_{OFF} is specified that output buffer changes to high impedance state.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
11. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).
12. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are specified as a reference point only. If $t_{WCS} \ge t_{WCS}$ (min), the cycle is early write cycle and the output pins will maintain high impedance(High-Z) state throughout the entire cycle. If $t_{RWD} \ge t_{RWD}$ (min), $t_{CWD} \ge t_{CWD}$ (min), and $t_{AWD} \ge t_{AWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the output pins.
   If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear at the output pins, and write operation can be executed by satisfing t_{RWL}, t_{CWL}, and t_{RAL} specifications.
15. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}/\overline{CAS_8}$ from V_{IL} to V_{IH}.). Therefore, if t_{CP} is short, t_{CAC} is longer than t_{CAC} (max).
16. For parify bit only.

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Fig.3 - DERATING CURVE (Normal Cycle)

T.B.D.

Fig.4 - DERATING CURVE (Fast Page Mode Cycle)

T.B.D.

Fig.5 - t_{RAC} vs t_{RCD}

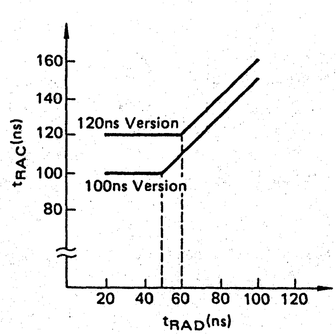
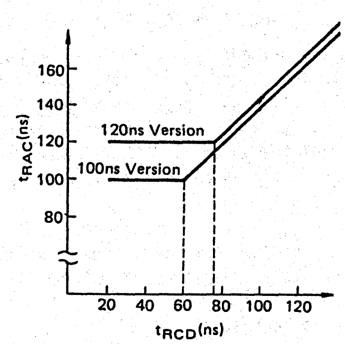
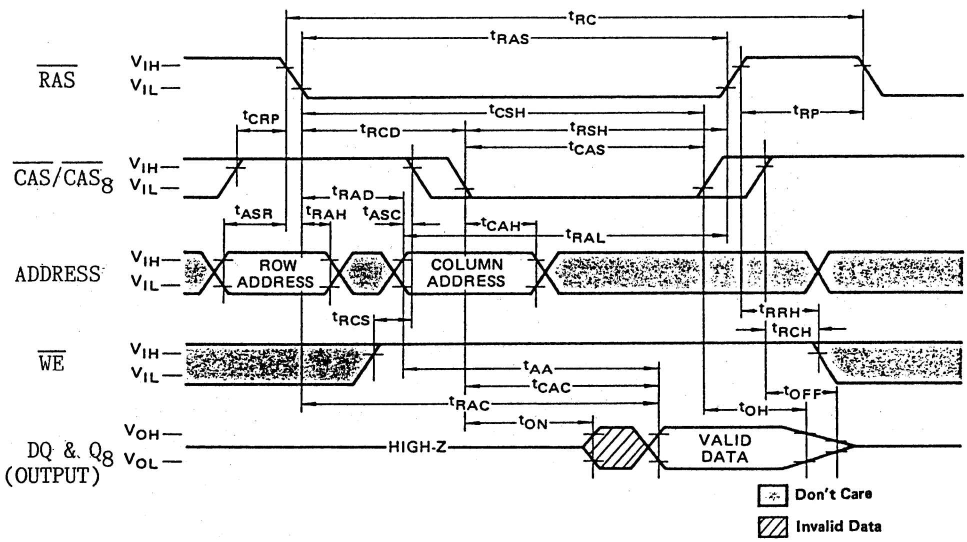


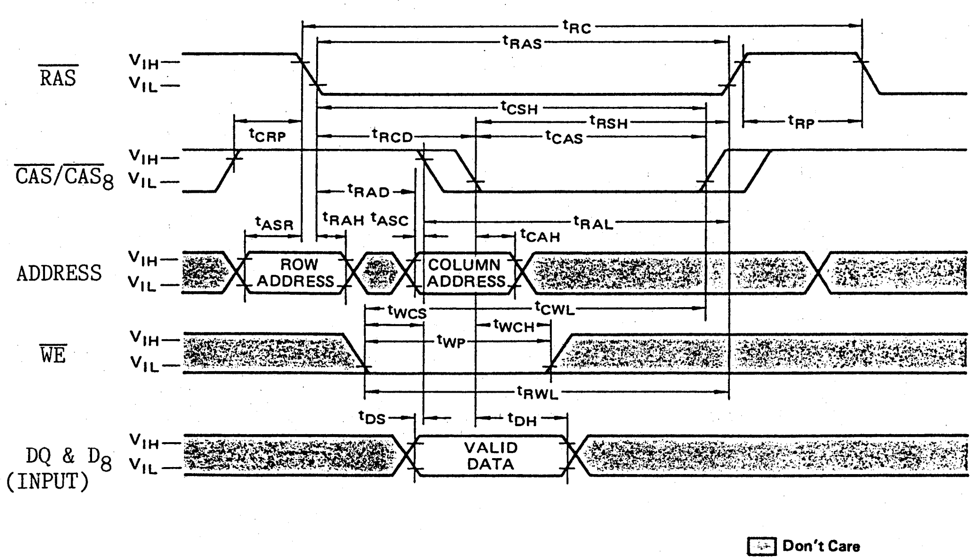
Fig.6 - t_{RAC} vs t_{RAD}



Read Cycle



Write Cycle (Early Write)



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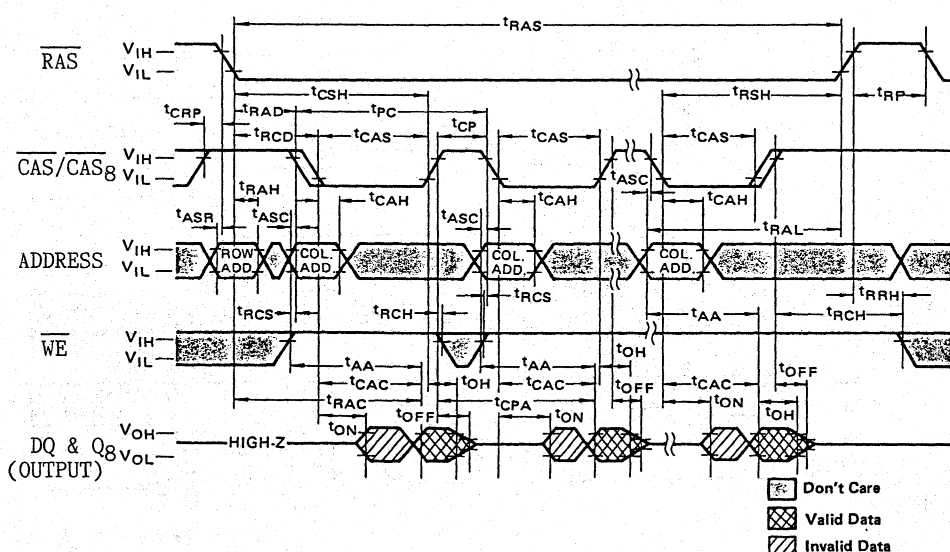
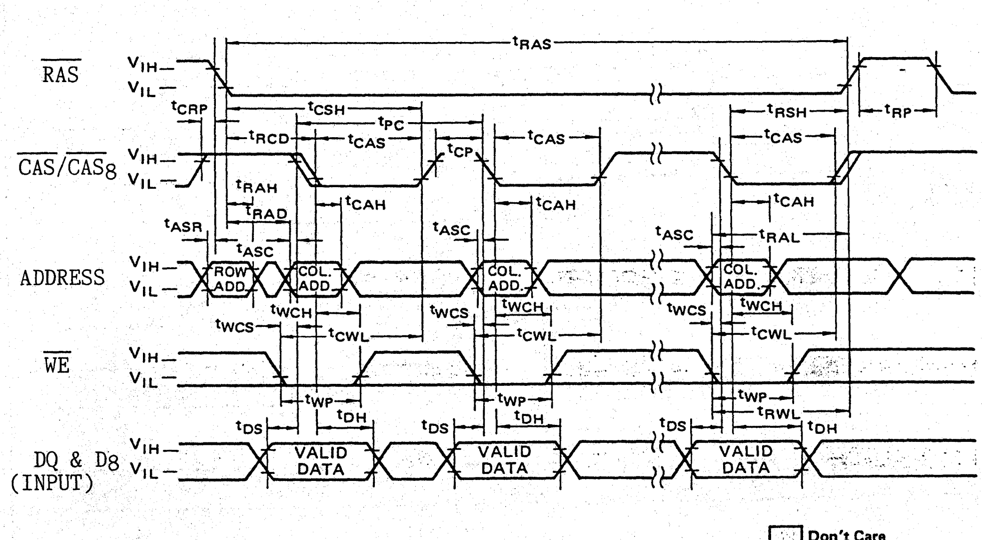
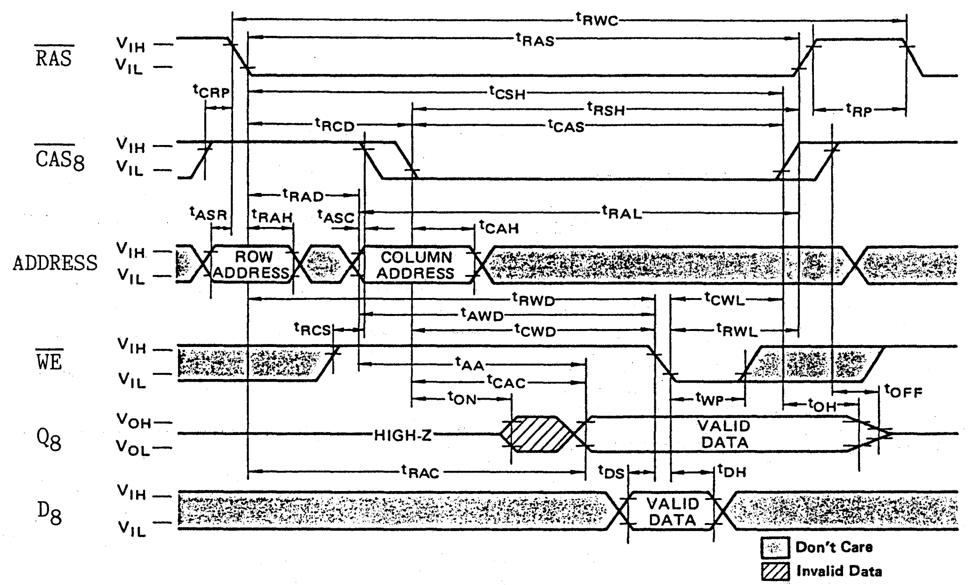
Fast Page Mode Read Cycle



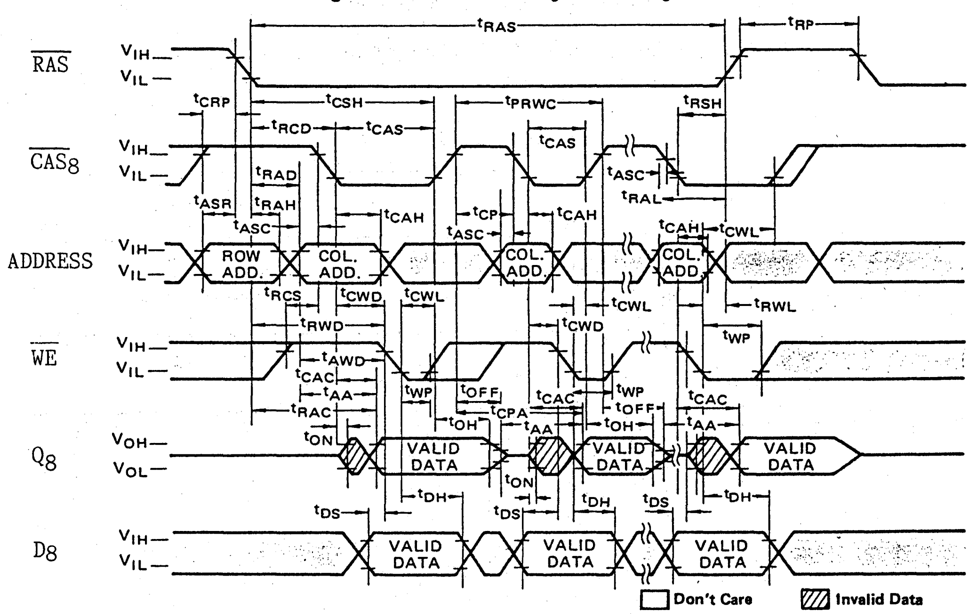
Fast Page Mode Write Cycle



Read-Modify-Write Cycle



Fast Page Mode Read-Modify-Write Cycle



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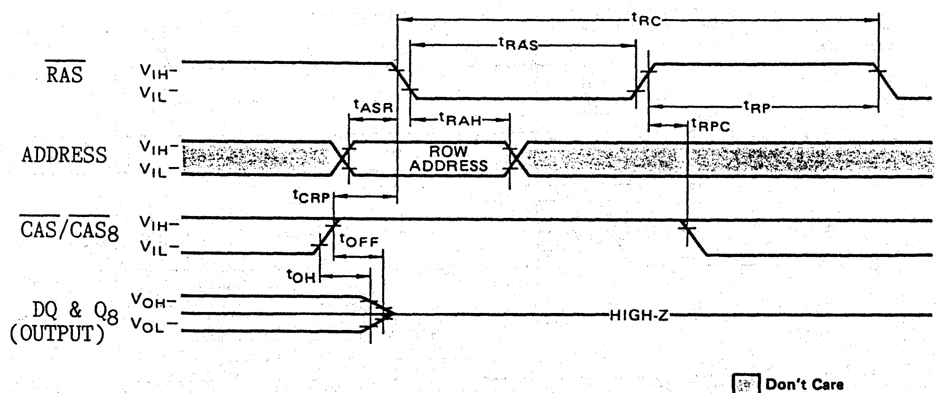
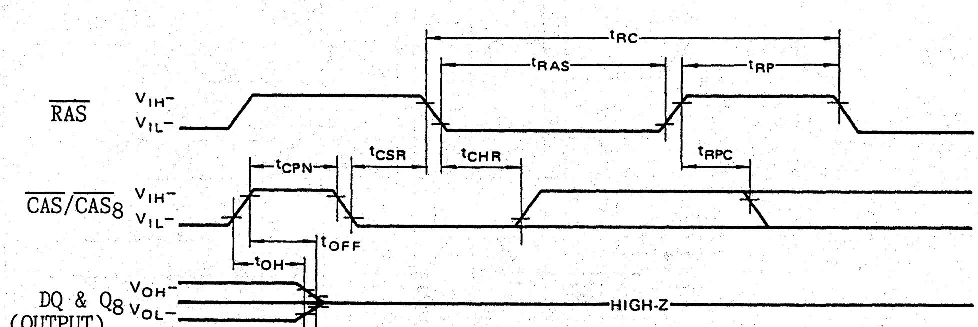
$\overline{RAS}$-only Refresh Cycle

NOTE : $\overline{WE}$, D, DQ(Input)=Don't care, A_9=V_{IH} or V_{IL}

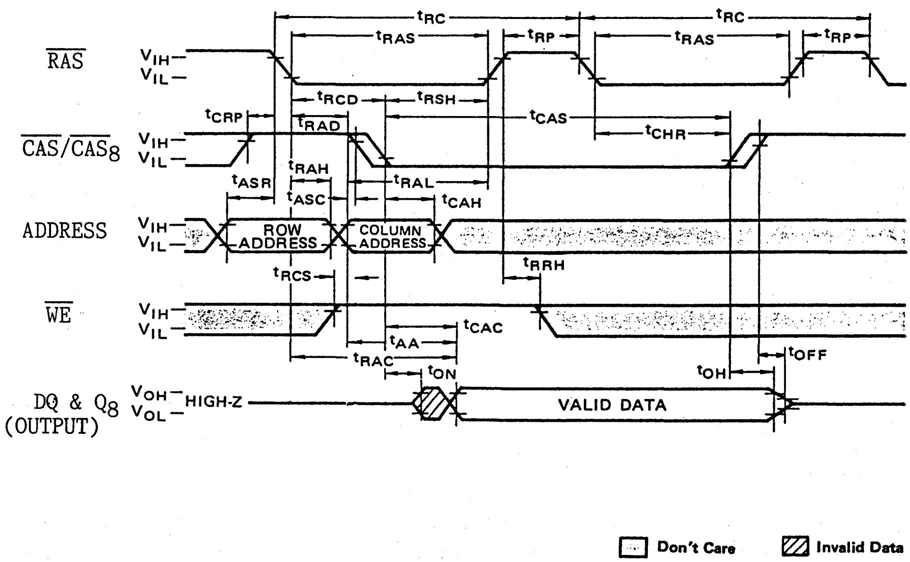


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE : Address, $\overline{WE}$, D, DQ(Input)=Don't care



Hidden Refresh Cycle



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DESCRIPTION

Block Analysis:
As shown in Fig. 1 and Fig. 2, the MB85235 is composed of nine MB81C1000, and the memory selection of the each MB81C1000 consists of a 1024-by-1024 cell matrix. Operational modes of the device are shown in the FUNCTIONAL TRUTH TABLE below.

Address Inputs:
A total of twenty binary input address bits are required to decode any 9-bit of the 9,437,184 storage cells within the MB85235. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe, $\overline{RAS}$. The ten column address bits are established on the address input pins(A_0 to A_9) and latched with the Column Address Strobe, $\overline{CAS}/\overline{CAS_8}$. All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}/\overline{CAS_8}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min)+ t_T. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occurs later.

Write Enable:
Read or Write mode is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write mode.

Data Input/Output:
1. **Data Input;**
   In write cycle, the 9-bit data is written into the MB85235 during write cycle through each DQ and D pin. Each input data is strobed and latched by falling edge of $\overline{CAS}/\overline{CAS_8}$ and $\overline{WE}$ must be brought to V_{IL} before falling edge of $\overline{CAS}/\overline{CAS_8}$, data input is strobed by $\overline{CAS}/\overline{CAS_8}$, and setup and hold times are referenced to $\overline{CAS}/\overline{CAS_8}$.
2. **Data Output;**
   The output buffers on each chip are three state TTL compatible with a fan out of 2 TTL loads. Output data has the same porality as input data. The outputs are in high impedance state until $\overline{CAS}$ and $\overline{CAS_8}$ are brought low. In a read cycle, the output becomes valid within t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD}(max) is satisfied. In the meanwhile when either t_{RCD} or t_{RAD}, or both, are equal or greater than their maximum value, the output data becomes valid within t_{CAC} or t_{AA} whichever occurs later after falling edge of $\overline{CAS}/\overline{CAS_8}$. The data output remains valid until $\overline{CAS}$ and $\overline{CAS_8}$ return to high.

Read Cycle:
The read cycle is executed by the falling edge of both $\overline{RAS}$ and $\overline{CAS}/\overline{CAS_8}$, and keeping $\overline{WE}$ to high throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}/\overline{CAS_8}$ respectively. The valid data will appear at the DQ and Q pins after determined by $\overline{RAS}$(t_{RAC}), $\overline{CAS}$(t_{CAC}), or Column address input(t_{AA}). If t_{RCD}($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}. The output data becomes invalid after $\overline{CAS}/\overline{CAS_8}$ is brought high, with a delay time of t_{OH}, and the DQ and Q pins return to the high impedance with t_{OH}.

Write Cycle:
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$. The 9-bit data on DQ and D pins are latched with the falling edge of $\overline{CAS}/\overline{CAS_8}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL}, and t_{RAL} must be satisfied the specifications.

DESCRIPTION (Continued)

Fast Page Mode Read Cycle:
The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ low, applying column address and $\overline{CAS}/\overline{CAS_8}$, and keeping $\overline{WE}$ high. Since the row address during fast page mode cycle is latched by normal cycle, the cycle time is reduced. During this mode, the access time is t_{CAC}, t_{AA}, or t_{CPA}, whichever occur later. Any of the 1024 bits belonging to each internal row address can be accessed.

Fast Page Mode Write Cycle:
The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$. The data on each DQ and D are latched with the falling edge of $\overline{CAS}/\overline{CAS_8}$ and written into the memory. During this write cycle, t_{CWL} must be satisfied. Any of 1024 bits belonging to each internal row address can be accessed.

Refresh:
The refresh of DRAM is executed by normal read and write cycle, i.e., the cells on each one row line, A_0 through A_8 except for A_9, are refreshed by one of two cycles. Each 512 row address must be refreshed every 8.2ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB85231 also has three types of refresh modes below.

1. **$\overline{RAS}$-only Refresh;**
   The $\overline{RAS}$-only refresh is executed by keeping $\overline{RAS}$ low, and $\overline{CAS}/\overline{CAS_8}$ remains high through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During this refresh, the data pins are kept high impedance state.

2. **$\overline{CAS}$-before-$\overline{RAS}$ Refresh;**
   The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}/\overline{CAS_8}$ low before $\overline{RAS}$ brought low. By this combination, the MB85235 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

3. **Hidden Refresh;**
   The hidden refresh is executed by keeping $\overline{CAS}/\overline{CAS_8}$ low to next cycle during read mode, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ and $\overline{CAS_8}$ are kept low continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

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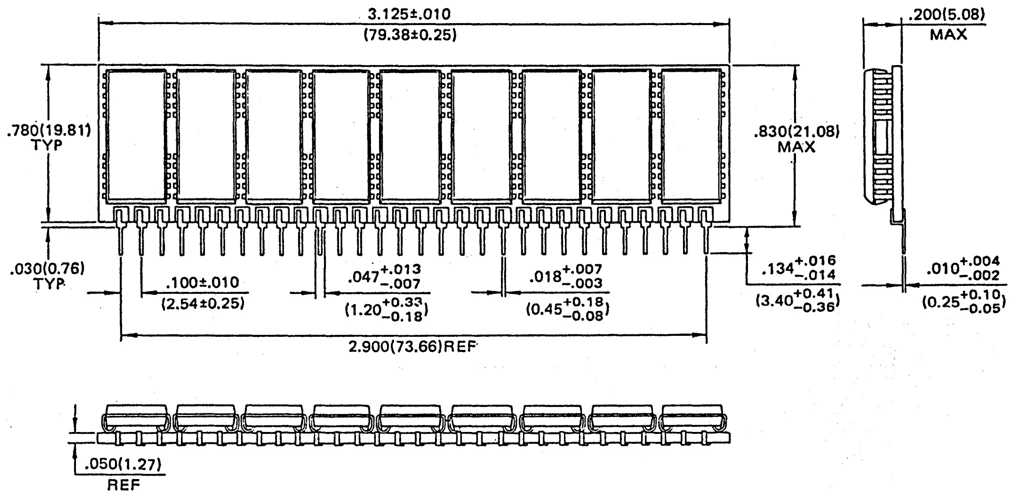
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data I/O	Note
	$\overline{RAS}$	$\overline{CAS}$(8)	$\overline{WE}$	Row	Column		
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	Cells are not refreshed.
Read (Normal)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min)
Read (Fast Page)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min) Cells are not refreshed.
Write (Normal)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min)
Write (Fast Page)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min) Cells are not refreshed.
$\overline{RAS}$-only Refresh	V_{IL}	V_{IH}	X	Valid	X	High-Z	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	V_{IL}	V_{IL}	X	X	X	High-Z	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh	V_{IL} *	V_{IL}	V_{IH}	X	X	Output Valid	Previous data is kept.

Note: X; Either V_{IH} or V_{IL}.
*; $\overline{RAS}$ puts V_{IH} at once.

PACKAGE DIMENSIONS
(Suffix: PJPS)

30-LEAD PLASTIC SINGLE-IN-LINE PACKAGE MODULE
(CASE No.: MSP-30P-P04)



Dimension in inches (millimeters)

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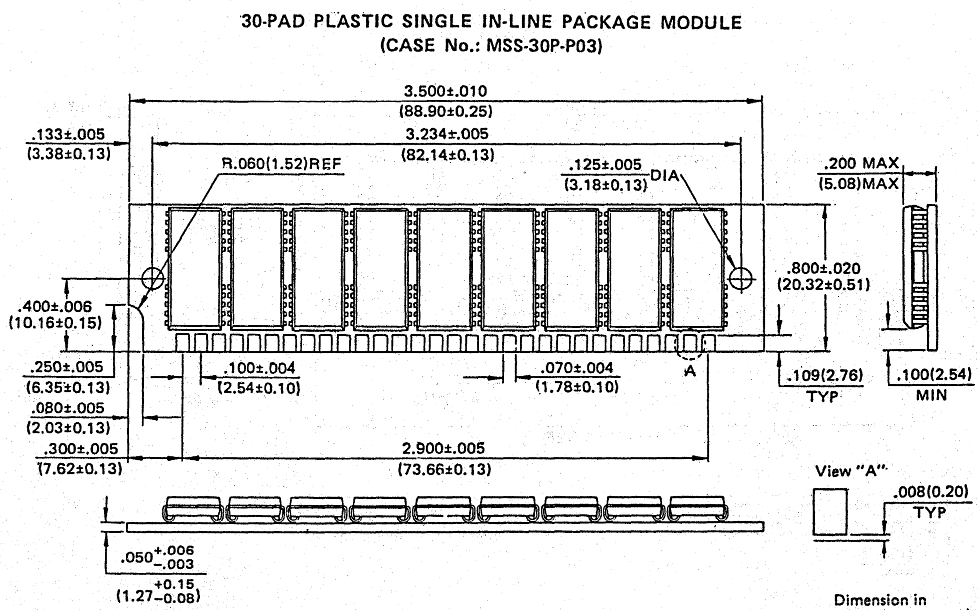
PACKAGE DIMENSIONS
(Suffix: PJPB)



FUJITSU

262144×9 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

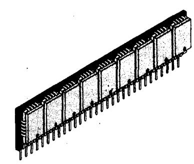
MB85240-10
MB85240-12

December 1987
Edition 1.0

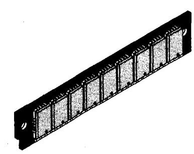
262,144 x 9 BIT CMOS STATIC COLUMN RANDOM ACCESS MEMORY

This Fujitsu MB85240 is a fully decoded, 262,144 words x 9 bits CMOS static column random access memory composed of nine 256k SCRAM chips (MB81C258x9). This module is designed for high speed, high performance applications such as main frame memory, buffer memory, and video memory, and for applications to battery backed-up systems where very low power dissipation and compact layout is required. The electrical characteristics of the MB85240 are quite same as the original MB81C258; each timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

- 262,144 x 9 SCRAM MODULE, 30-pin SIP and socket type
- Row Access Time (t_{RAC})
  - 100 ns max. (MB85240-10)
  - 120 ns max. (MB85240-12)
- Random Cycle Time (t_{RC})
  - 200 ns min. (MB85240-10)
  - 230 ns min. (MB85240-12)
- Address Access Time (t_{AA})
  - 45 ns max. (MB85240-10)
  - 55 ns max. (MB85240-12)
- Static Mode Cycle Time (t_{SC})
  - 50 ns min. (MB85240-10)
  - 60 ns min. (MB85240-12)
- Low Power Dissipation
  - 2970 mW max. (MB85240-10)
  - 2475 mW max. (MB85240-12)
    - 99 mW max. standby with TTL level input
    - 15 mW max. standby with CMOS level input
- +5V supply, ±10% tolerance
- 32ms/256 refresh cycles capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability

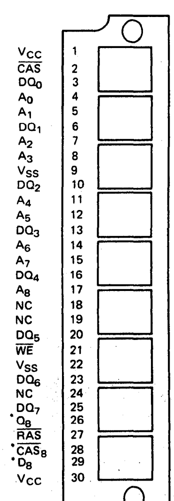


PLASTIC PACKAGE
MSP-30P-P02



PLASTIC PACKAGE
MSS-30P-P01

PIN ASSIGNMENT



* ; For parity bit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	9.0	W
Short circuit output current	–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — FUNCTIONAL BLOCK DIAGRAM

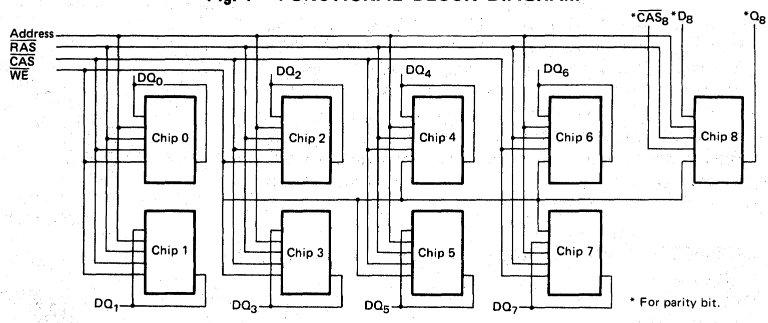
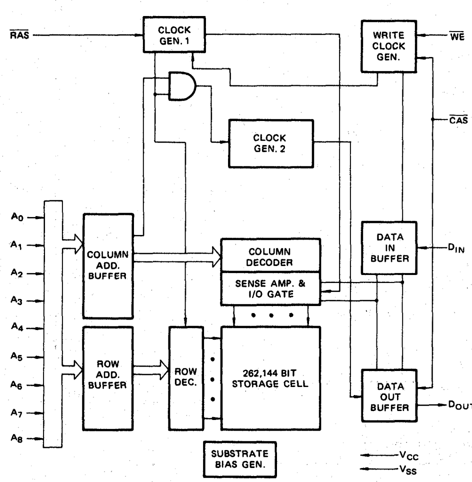


Fig. 2 — BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_8	C_{IN1}		80	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}		88	pF
Input Capacitance, $\overline{CAS}$	C_{IN3}		70	pF
Input Capacitance, $\overline{WE}$	C_{IN4}		49	pF
Input Capacitance, $\overline{CAS_8}$	C_{IN5}		11	pF
Input Capacitance, D_8	C_{IN6}		7	pF
I/O Capacitance, DQ_0 to DQ_7	C_{DQ}		15	pF
Output Capacitance, Q_8	C_O		11	pF

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RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C*
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	–	6.5	V	
Input Low Voltage	V_{IL}	-1.0	–	0.8	V	

Note * : Ambient temperature is dependent on cycle time and cooling conditions.
See the derating curve Fig. 3 for normal cycle, and Fig. 4 for static mode cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING/REFRESH CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB85240-10	I_{CC1}		540	mA
	MB85240-12			450	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	TTL Level	I_{CC2}		18	mA
	CMOS Level			2.7	
STATIC MODE OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, $\overline{WE}$ or Address = cycling; t_{SC} = min)	MB85240-10	I_{CC3}		360	mA
	MB85240-12			315	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$ refresh; t_{RC} = min)	MB85240-10	I_{CC4}		495	mA
	MB85240-12			405	
INPUT LEAKAGE CURRENT, ALL INPUTS (V_{IN} = 0V to 5.5V, V_{CC} = 5V, V_{SS} = 0V, all other inputs not under test = 0V)		$I_{I(L)1}$ ($\overline{CAS_8}$, D_8)	-10	10	μA
		$I_{I(L)2}$ (Others)	-30	30	
OUTPUT LEAKAGE CURRENT Each output is high impedance (Data is disable, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output High Voltage (I_{OH} = -5 mA) Output Low Voltage (I_{OL} = 4.2 mA)		V_{OH} V_{OL}	2.4	0.4	V

Note 1): I_{CC} is dependent on the output loading and cycle time. Output pins are open.

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2

Parameter	NOTE	Symbol	MB85240-10		MB85240-12		Unit
			Min	Max	Min	Max	
Time between Refresh		t_{REF}	–	32	–	32	ms
Random Read/Write Cycle Time		t_{RC}	200	–	230	–	ns
Read-Modify-Write Cycle Time	15	t_{RWC}	245	–	285	–	ns
Access Time from $\overline{RAS}$	3 5	t_{RAC}	–	100	–	120	ns
Access Time from $\overline{CAS}$		t_{CAC}	–	25	–	30	ns
Output Buffer Turn Off Delay Time		t_{OFF}	0	25	0	25	ns
Transition Time		t_T	3	50	3	50	ns
Column Address Access Time	4 5	t_{AA}	–	45	–	55	ns
Output Hold Time from Column Address Change		t_{AOH}	5	–	5	–	ns
Access Time from $\overline{WE}$ Precharge	15	t_{WPA}	–	25	–	30	ns
Access Time Relative to Last Write	6 15	t_{ALW}	–	90	–	110	ns
Write latched Output Hold Time	15	t_{WOH}	0	–	0	–	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90	–	100	–	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	65	100000	75	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	25	–	30	–	ns
$\overline{CAS}$ Pulse Width (Read)		t_{CAS}	25	100000	30	100000	ns
$\overline{CAS}$ Pulse Width (Write)		t_{CAS}	15	100000	20	100000	ns
$\overline{CAS}$ Hold Time (Read)		t_{CSH}	100	–	120	–	ns
$\overline{CAS}$ Hold Time (Write)		t_{CSH}	80	–	95	–	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	25	75	25	90	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	20	–	25	–	ns
Row Address Set Up Time		t_{ASR}	0	–	0	–	ns
Row Address Hold Time		t_{RAH}	15	–	15	–	ns
Column Address Set Up Time	7	t_{ASC}	0	–	0	–	ns
Column Address Hold Time	7	t_{CAH}	20	–	25	–	ns
$\overline{RAS}$ to Column Address Delay Time	8 9	t_{RAD}	20	55	20	65	ns
Column Address Hold Time Reference to $\overline{RAS}$		t_{AR}	100	–	120	–	ns
Write Address Hold Time Referenced to $\overline{RAS}$		t_{AWR}	80	–	90	–	ns

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AC CHARACTERISTICS (Cont'd)

(Recommended operating conditions unless otherwise noted.) Note 1, 2

Parameter	NOTE	Symbol	MB85240-10		MB85240-12		Unit
			Min	Max	Min	Max	
Read Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	–	55	–	ns
Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time	10	t_{AHR}	15	–	15	–	ns
Last Write to Column Address Delay Time	11 12 15	t_{LWAD}	25	45	30	55	ns
Column Address Hold Time Referenced to Last Write		t_{AHLW}	90	–	110	–	ns
Read Command Set Up Time Referenced to $\overline{CAS}$		t_{RCS}	0	–	0	–	ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	10	–	10	–	ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0	–	0	–	ns
$\overline{WE}$ Pulse Width		t_{WP}	15	–	20	–	ns
$\overline{WE}$ Inactive Time		t_{WI}	15	–	20	–	ns
Write Command Hold Time		t_{WCH}	15	–	20	–	ns
Write Command to $\overline{RAS}$ Lead Time	15	t_{RWL}	25	–	30	–	ns
Write Command to $\overline{CAS}$ Lead Time	15	t_{CWL}	25	–	30	–	ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time	14 15	t_{RWD}	100	–	120	–	ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	–	30	–	ns
Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	45	–	55	–	ns
$\overline{RAS}$ to Second Write Delay Time		t_{RSWD}	105	–	125	–	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	80	–	95	–	ns
Write Set Up Time for Output Disable	14	t_{WS}	0	–	0	–	ns
Write Hold Time for Output Disable	14	t_{WH}	0	–	0	–	ns
D_{IN} Set Up Time		t_{DS}	0	–	0	–	ns
D_{IN} Hold Time		t_{DH}	20	–	25	–	ns
D_{IN} Hold Time Reference to $\overline{RAS}$		t_{DHR}	80	–	90	–	ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20	–	25	–	ns

4

AC CHARACTERISTICS (Cont'd)

(Recommended operating conditions unless otherwise noted.) Note 1, 2

Parameter NOTES	Symbol	MB85240-10		MB85240-12		Unit
		Min	Max	Min	Max	
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCH}	20	–	25	–	ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	20	–	25	–	ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)	t_{RPC}	20	–	20	–	ns
Static Mode Read/Write Cycle Time	t_{SC}	50	–	60	–	ns
Static Mode Read-Modify-Write Cycle Time 15	t_{SRWC}	95	–	115	–	ns
Static Mode $\overline{CAS}$ Precharge Time	t_{CP}	15	–	20	–	ns

NOTES:

1 An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

2 AC characteristics assume t_T = 5ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8V, V_{OH} = 2.4V, and V_{OL} = 0.4V.

3 Assumes that $t_{RAD} \leq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.

4 Assumes that $t_{RAD} \geq t_{RAD}$ (max).

5 Measured with a load equivalent to 2 TTL loads and 100pF.

6 Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.

7 Write Cycle Only.

8 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

9 t_{RAS} (min) = t_{RAH} (min) + t_T (t_T = 5ns)

10 t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.

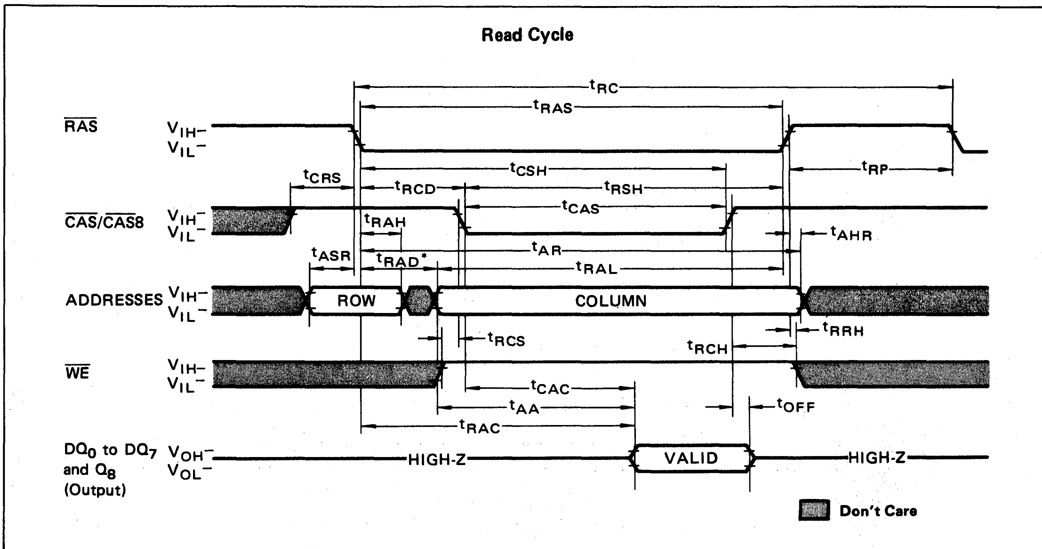
11 Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.

12 t_{LWAD} (min) = t_{AHW} (min) + t_T (t_T = 5ns)

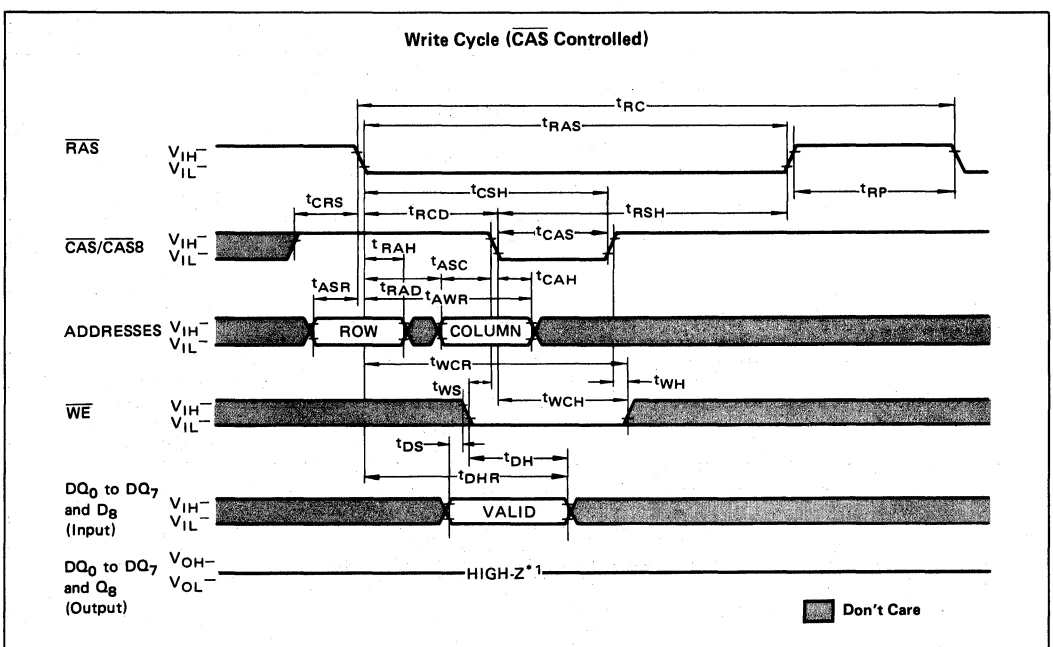
13 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

14 t_{WS}, t_{WH}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. It $t_{RWD} \geq t_{RWD}$ (min). The data output will contain data read from the selected cell.

15 Parity bit only.



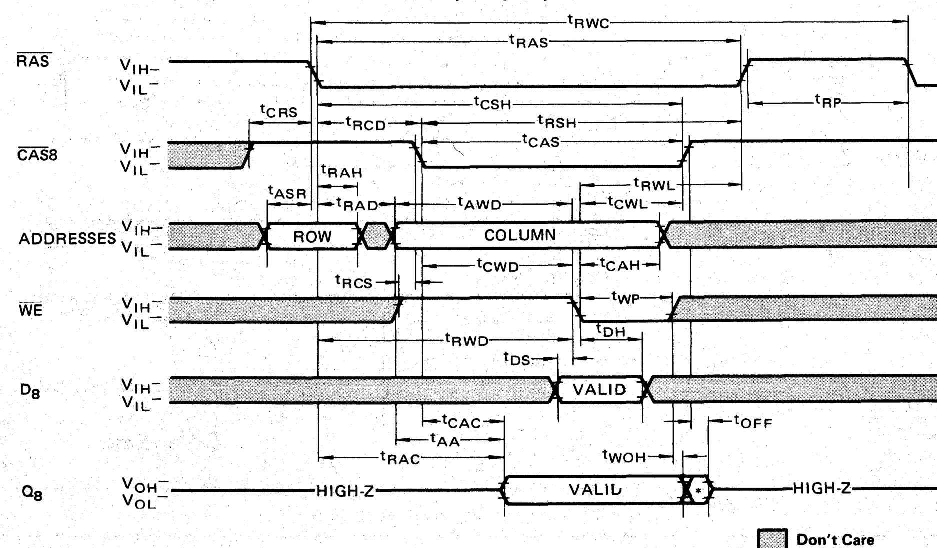
*; If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA}



*; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.

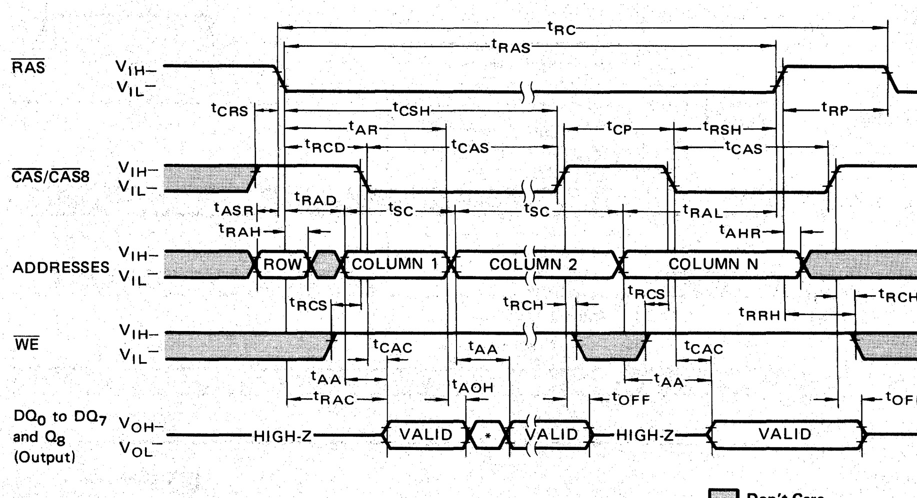
4

Read-Modify-Write Cycle
(Note; Only for parity bit.)



*; Invalid Data

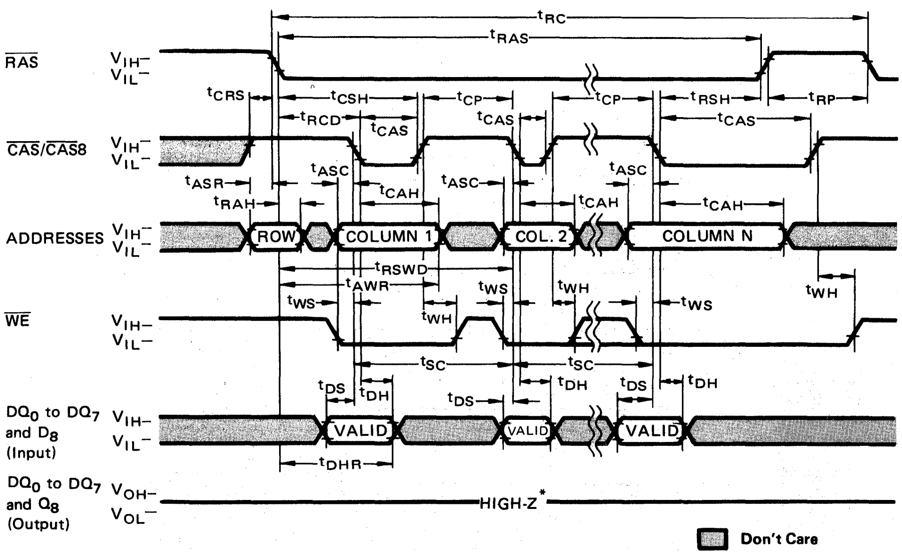
Static Mode Read Cycle



*; Invalid Data.

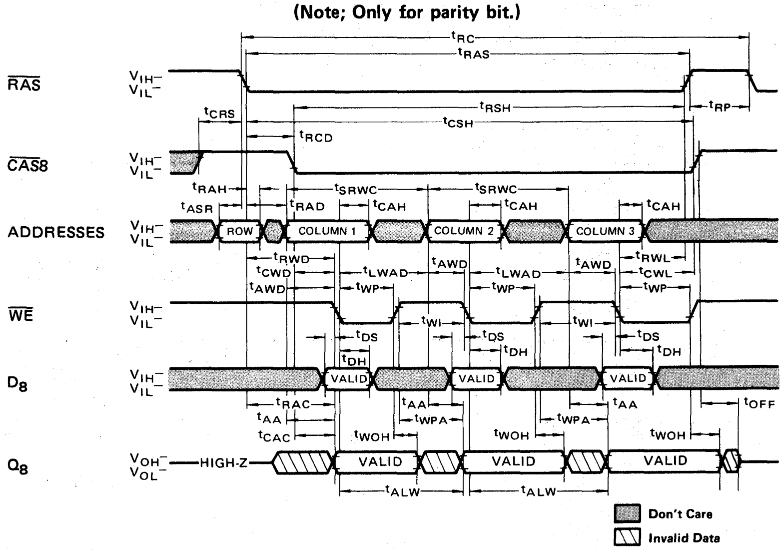
4

Static Mode Write Cycle



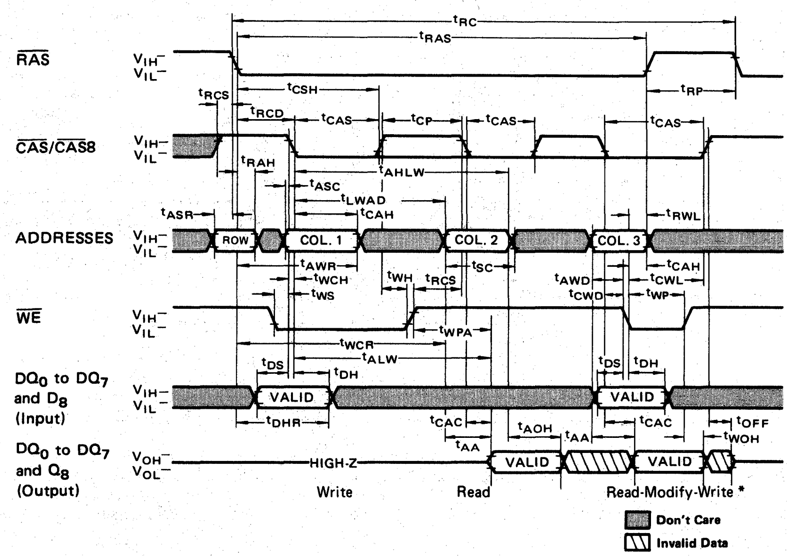
*; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.

Static Mode Read-Modify-Write
(Note; Only for parity bit.)



4

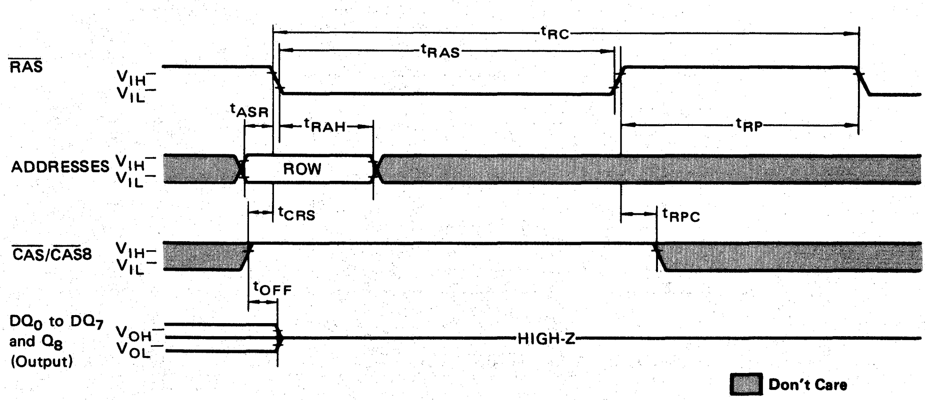
Static Mode Mixed Cycle



*; Only for parity bit.

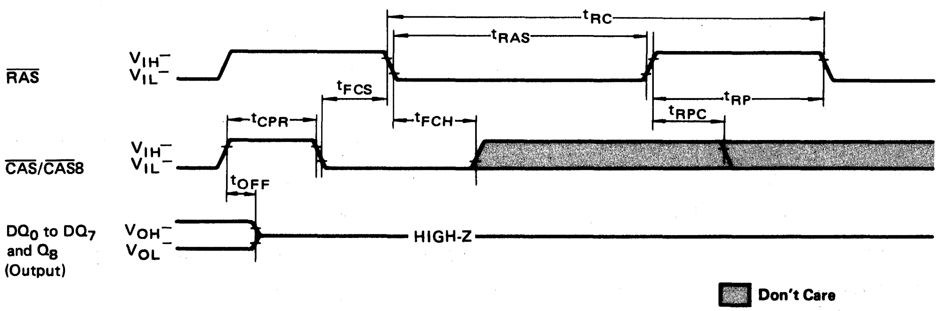
RAS-Only Refresh Cycle

(Note; WE, D_{IN} = Don't Care, A_8 = V_{IH} or V_{IL})

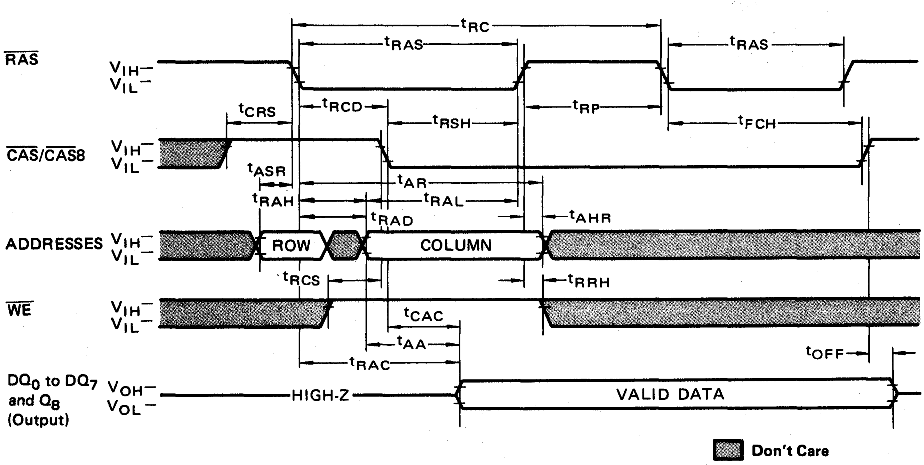


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

(Note; Address, $\overline{WE}$, D_{IN} = Don't Care)



Hidden Refresh Cycle



FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$ and $\overline{CAS_8}$	$\overline{WE}$	DQ_0 to DQ_7, D_8 and Q_8	Function
H	H	Don't Care	High-Z	Standby
L	L	H	Valid Data Out[1)]	Ready cycle
L	L	L	Valid Data In[2)]	Write cycle
L	L[3)]	Don't Care	High-Z	$\overline{CAS}$-before $\overline{RAS}$ Refresh cycle
L	H	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle
L	H ($\overline{CAS}$) L ($\overline{CAS_8}$)	H → L[4)]	High-Z (DQ_0 to DQ_7) Valid Data In (D_8) Valid Data Out (Q_8)	$\overline{RAS}$-only Refresh cycle (Except for Pairyt bit) Read-Write/Read-Modify-Write (Parity bit)

Notes: 1): DQ Pins are output mode.
2): DQ pins are input mode.
3): $t_{FCS} \geqq t_{FCS}$ (min)
4): $t_{CWD} \geqq t_{CWD}$ (min)

DESCRIPTION

Address Inputs:
A total of eighteen binary input address bits are required to decode any one of the 262,144 storage cells within each MB81C258. Nine row address bits are established on the address input pins (A_0 to A_8) and latched with the Row Address Strobe ($\overline{RAS}$). The nine column address bits are established on the address input pins (A_0 to A_8) after the Row Address Hold Time (t_{RAH}) has been satisfied. In read cycle, the column address are not latched by the Column Address Strobe ($\overline{CAS}$), so the column address must be stable until the output becomes valid. In write cycle, the column address are latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. The write operation is asserted on the later falling edge of $\overline{CAS}$ or $\overline{WE}$ (Both $\overline{CAS}$ and $\overline{WE}$ are low). The time period of the write operation is determined by internal circuit, thus next write operation will be inhibited during the write operation.

Data Input:
Data is written into the MB85240 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Data Output:
Each output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. Each output is in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the access time is determined by the following conditions:
1. t_{RAC} from the falling edge of $\overline{RAS}$.
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of $\overline{CAS}$.

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC} = t_{RCD} + t_{CAC}$ or $t_{RAC} = t_{RAD} + t_{AA}$.
Data outputs remain valid while the column address inputs are kept constant. However, when $\overline{CAS}$ goes high, the output returns to high impedance state.

Static Mode:
The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, $\overline{CAS}$ can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.
1. Static mode read cycle;
   In a static mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle;
   In a static mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle.
3. Static mode read-modify-write cycle;
   In the static mode read-modify-write cycle, $\overline{WE}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge a of $\overline{WE}$.
4. Static mode mixed cycle;
   In the static mode, read, write, and read-modify-write cycles can be mixed in any order.

In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.
1. t_{ALW} from the later falling edge of $\overline{CAS}$ or $\overline{WE}$ at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of $\overline{WE}$ at the read cycle.
4. t_{CAC} from the falling edge of $\overline{CAS}$.

Refresh:
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7) at least every 32ms.
The MB85240 offers the following three types of refresh.
1. $\overline{RAS}$-only refresh;
   The $\overline{RAS}$-only refresh avoids any output during refresh because each output buffer is high impedance state due to $\overline{CAS}$ high. Strobing of each 256 row address (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB85240 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes low, on chip refresh control clock generator and the internal refresh address counter are enabled, and an internal refresh operation is executed. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3. Hidden refresh;
   A hidden refresh cycle will be executed while maintaining latest valid output datas at the DQ pins by extending the $\overline{CAS}$ low time. For the MB85240, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh. The internal refresh address counter provides the refresh address, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Notice for using MB8520
The MB85240 is a SIP (Single-In-Line-Package) module which is composed of nine MB81C258 DRAMs housed in plastic LCC, and assembled on the epoxy printed circuit board. Generally the multilayer PCB board has large wiring capacitance. This disadvantage causes relatively noise induction between signal lines and power supply lines (V_{SS} or V_{CC}).
Furthermore, as the MB85240 is a very high-speed memory, the timing windows to strobe address $\overline{WE}$ and D_{IN} signals are very short (Approx. 10ns). Therefore, it is very sensitive even to very sharp noise.
From the above reasons, special care should be taken for use the MB85240. The following notices are recommended;

4

DESCRIPTION

1. Provide a externally capacitor of approx. a few μF each module, the MB85240 has the nine decoupling capacitors (0.22 μF on each SCRAM 0.22 μF x 9).
2. Remove noise, riging, overshoot and undershoot from the address, clocks and DQ lines, so that the MB85240 won't latch wrong signals due to the noise induction between signal lines and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. Provide an appropriate dumping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

Fig. 3 — MB85240 DERATING CURVE

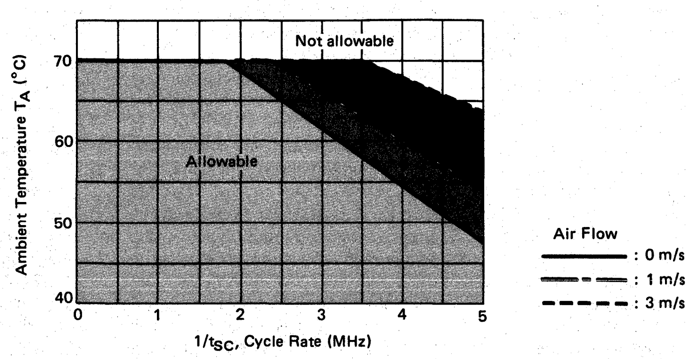
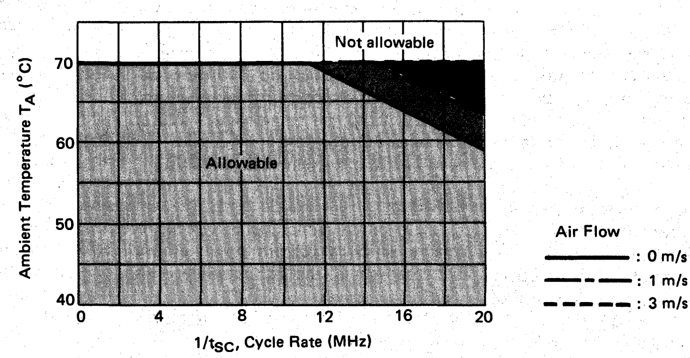
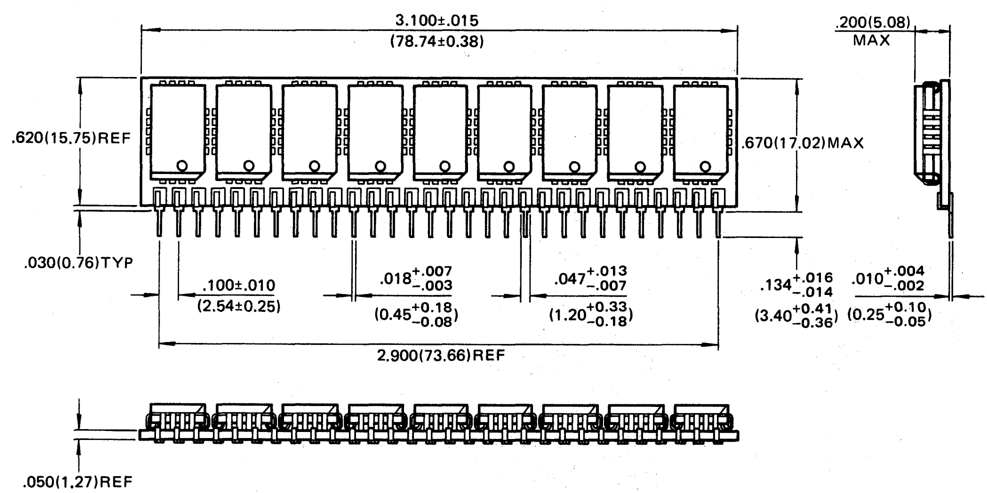


Fig. 4 — MB85240 DERATING CURVE



PACKAGE DIMENSIONS

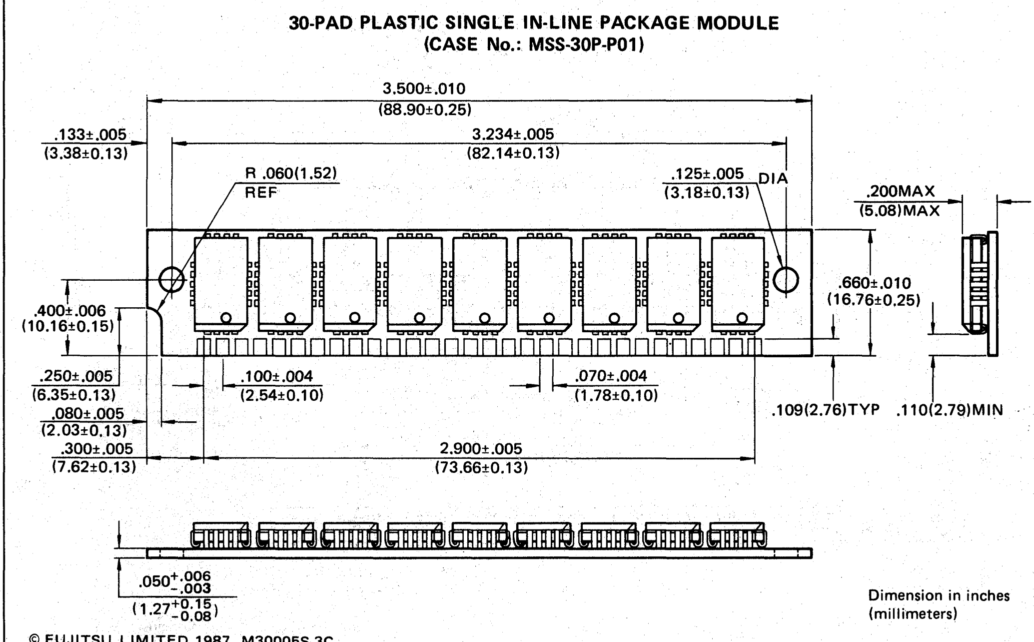
30-LEAD SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSP-30P-P02)



Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS



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FUJITSU

16K x 16 CMOS SRAM MODULE

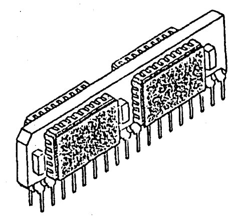
MB85402-30
MB85402-40

TS255-B88Y
Nov. 1988

CMOS 16,384 Words x 16-Bit STATIC RANDOM ACCESS MEMORY MODULE

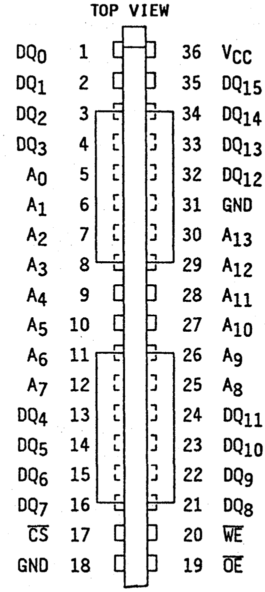
The Fujitsu MB85402 is a fully decoded, CMOS Static random access memory module comprised of four MB81C75 devices mounted on a 36-pin ceramic board. Organized as four 16K x 4 devices, the MB85402 is optimized for those applications requiring high speed, high performance, low power and high density.
A separate output enable function provides maximum control for those systems where bus contention may be a problem.

- Organized as 16,384 x 16-bit Words
- Memory : MB81C75, 4 pcs
- Access Time : 30 ns max (MB85402-30)
  40 ns max (MB85402-40)
- Low Power Dissipation
  Standby: 220 mW max (CMOS level)
  440 mW max (TTL level)
  Active : 1760 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- TTL Compatible Input/Output Pins
- 3-State Output
- 36-Pin 100 MIL Ceramic DIP/SIP



CERAMIC PACKAGE
MTP-36C-C01

PIN ASSIGNMENT
TOP VIEW



ABSOLUTE MAXIMUM RATING (See **NOTE**.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	4.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM

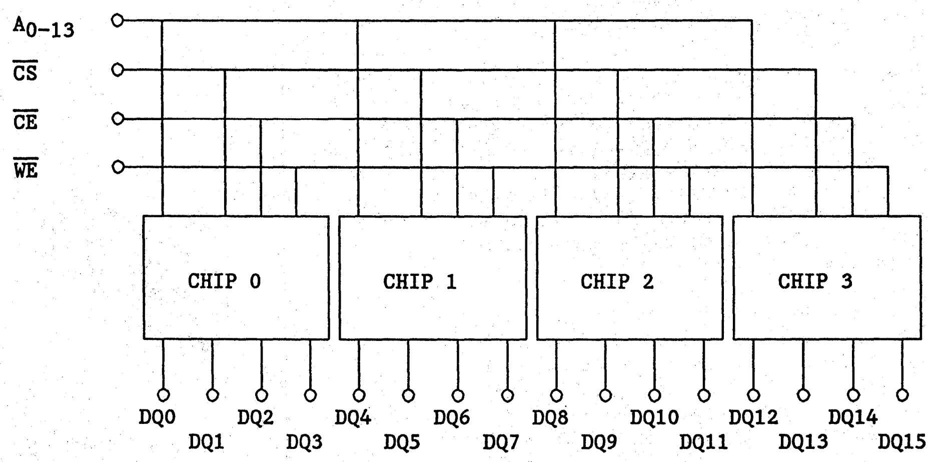
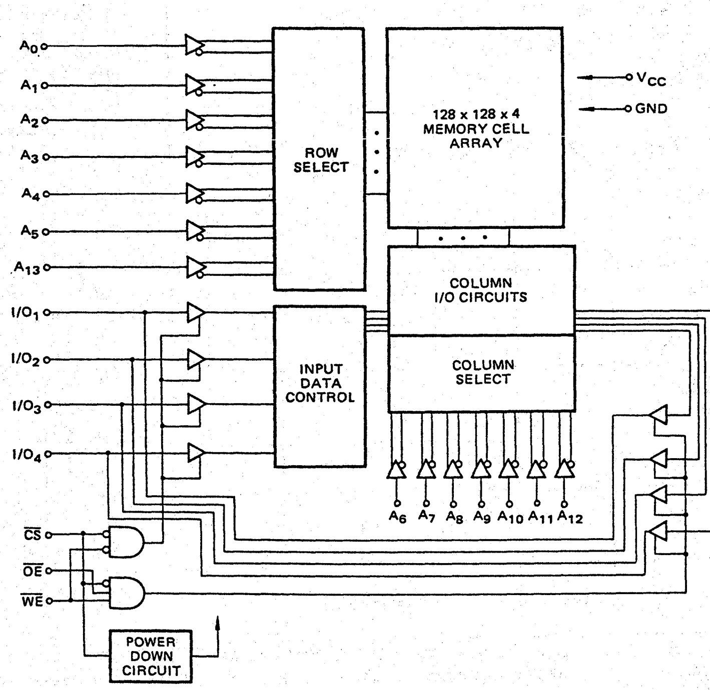


Fig. 2 – BLOCK DIAGRAM for EACH MEMORY



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input1Capacitance (V_{IN}=0V)	C_{IN}		50	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		15	pF

FUNCTIONAL TRUTH TABLE

MODE	ADDRESS	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
STANDBY	DON'T CARE	V_{IH}	DON'T CARE	DON'T CARE	HIGH-Z	STANDBY
READ	VALID	V_{IL}	V_{IH}	V_{IL}	D_{OUT}	ACTIVE
OUTPUT DESABLE	VALID	V_{IL}	V_{IH}	V_{IH}	HIGH-Z	ACTIVE
WRITE	VALID	V_{IL}	V_{IL}	DON'T CARE	D_{IN}	ACTIVE

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

4

DC CHARACTERISTICS

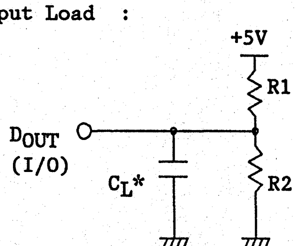
(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
INPUT LEAKAGE CURRENT (V_{IN}=0V to V_{CC})		I_{LI}	-40		40	µA
OUTPUT LEAKAGE CURRENT ($\overline{CS}$=V_{IH}, V_{OUT}=0V to V_{CC})		I_{LO}	-10		10	µA
STANDBY POWER SUPPLY CURRENT	CMOS level	I_{SB1}			40	mA
	TTL level	I_{SB2}			80	mA
ACTIVE POWER SUPPLY CURRENT ($\overline{CS}$=V_{IL}, I_{OUT}=0mA, V_{IN}=0V or V_{CC})		I_{CC1}			240	mA
OPERATING POWER SUPPLY CURRENT (I_{OUT}=0mA, t_{CYCLE}=Min.)		I_{CC2}			320	mA
INPUT HIGH LEVEL		V_{IH}	2.2		6.0	V
INPUT LOW LEVEL*[1]		V_{IL}	-0.5		0.8	V
OUTPUT HIGH LEVEL (I_{OH}=-4mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=8mA)		V_{OL}			0.4	V

Note: *[1] -2.0V level with a maximum pulse width of 20ns.

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels : 0V to 3.0V
- Input Rise and Fall Times : 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels : 1.5V (Input and Output)
- Output Load :



	R1	R2	C_L
Load I	480Ω	255Ω	30pF
Load II	480Ω	255Ω	5pF

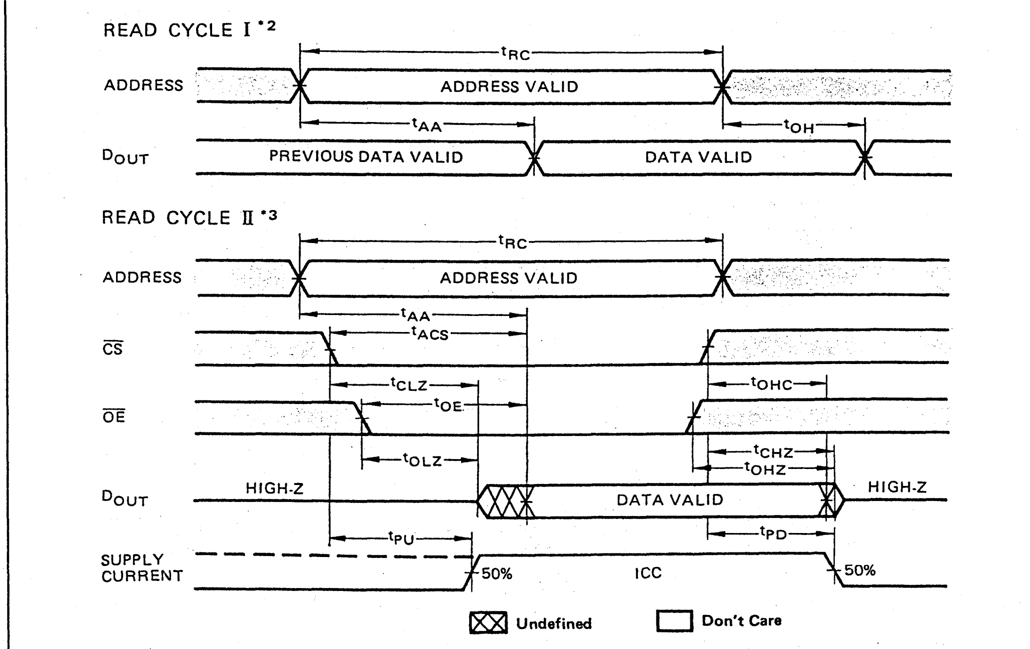
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB85402-30		MB85402-40		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	30		40		ns
Address Access Time *2	t_{AA}		30		40	ns
CS Access Time *3	t_{ACS}		30		40	ns
OE Access Time *3	t_{OE}		13		15	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from CS	t_{OHC}	3		3		ns
CS to Output Low-Z *4*5	t_{CLS}	5		5		ns
OE to Output Low-Z *4*5	t_{OLZ}	0		0		ns
CS to Output High-Z *4*5	t_{CHZ}		13		15	ns
OE to Output High-Z *4*5	t_{OHZ}		13		15	ns
Power Up from CS	t_{PU}	0		0		ns
Power Down from CS	t_{PD}		25		30	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}=V_{IL}$, $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

4

AC CHARACTERISTICS

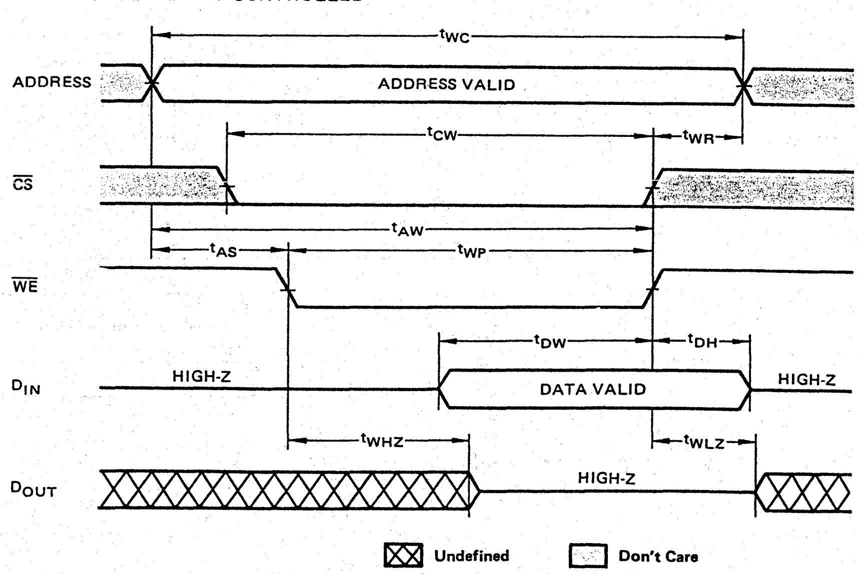
(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85402-30		MB85402-40		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	30		40		ns
Address Valid to End of Write	t_{AW}	25		35		ns
CS to End of Write	t_{CW}	25		35		ns
Data Valid to End of Write	t_{DW}	13		17		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	25		35		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	2		2		ns
Output High-Z from $\overline{WE}$ *3*4	t_{WHZ}		13		15	ns
Output Low-Z from WE *3*4	t_{WLZ}		25		35	ns

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE I: $\overline{WE}$ CONTROLLED*1*2



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

*3 Transition is measured at the point of ±500mV from steady state voltage.

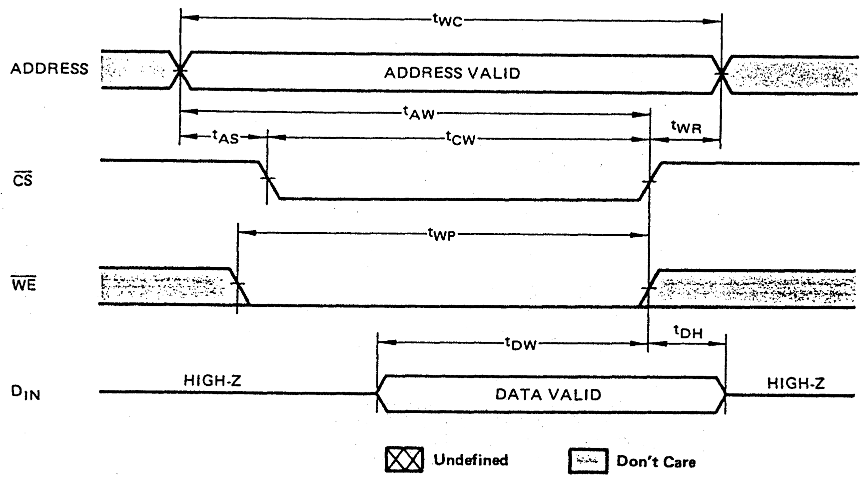
*4 This parameter is specified with Load II in Fig. 2.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1 *2

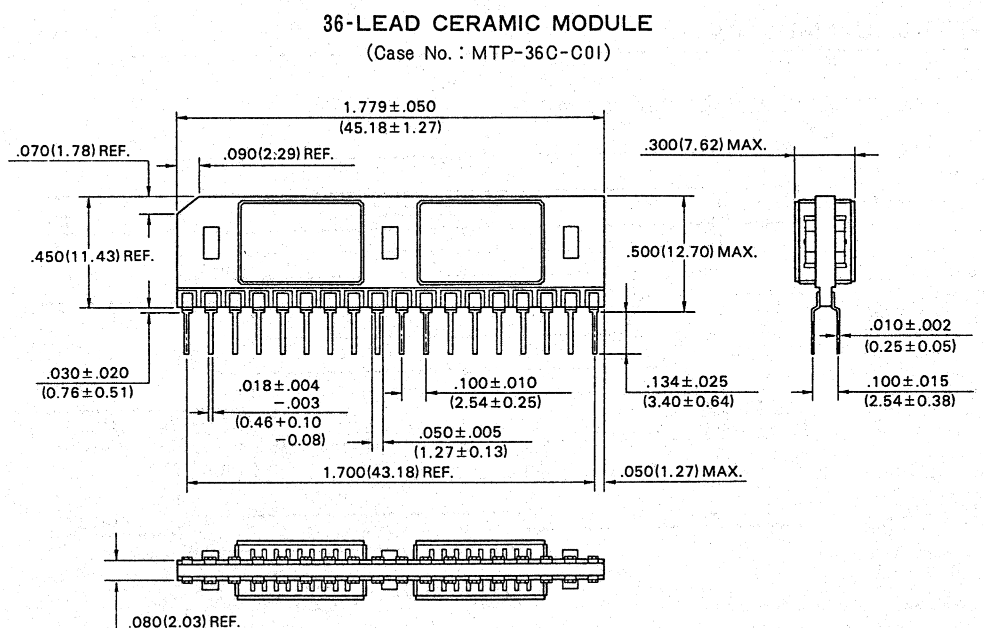


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

4

PACKAGE DIMENSIONS
(Suffix: CVCT)



NOTE
1. Dimension in inches and (millimeters).

FUJITSU

256K x 8 CMOS SRAM MODULE

MB85403A-40
MB85403A-50

TS261-A88Y
Nov. 1988

CMOS 262,144 Words x 8-Bit STATIC RANDOM ACCESS MEMORY MODULE

PRELIMINARY

The Fujitsu MB85403A is a fully decoded, CMOS static random access memory module consists of eight MB81C81A devices mounted on a 44-pin ceramic board. Organized as eight 256K x 1 devices, the MB85403 is optimized for those applications requiring high speed, high performance, large memory storage, and high density.

- Organized as 262,144 x 8-bit Words
- Memory : MB81C81A, 8 pcs
- Access Time : 40 ns max (MB85403A-40)
  50 ns max (MB85403A-50)
- Low Power Dissipation
  Standby: 660 mW max (CMOS level)
  1320 mW max (TTL level)
  Active : 5280 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- Dual Chip Select (x8 or x4 organization)
- TTL Compatible Input/Output Pins
- 3-State Output
- 44-Pin 100 MIL Ceramic Twin SIP (TSIP)

CERAMIC PACKAGE
MTP-44C-C02

PIN ASSIGNMENT
TOP VIEW

GND	1	44	VCC
DOUT0	2	43	DOUT7
DIN0	3	42	DIN7
A16	4	41	A0
A17	5	40	A1
A13	6	39	A2
GND	7	38	A3
DOUT1	8	37	DOUT6
DIN1	9	36	DIN6
A12	10	35	A4
A11	11	34	A7
NC	12	33	/WE
/CSA	13	32	/CSB
DOUT2	14	31	DOUT5
DIN2	15	30	DIN5
A14	16	29	GND
A15	17	28	A6
A10	18	27	A5
A9	19	26	A8
DOUT3	20	25	DOUT4
DIN3	21	24	DIN4
VCC	22	23	GND

ABSOLUTE MAXIMUM RATING (See NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – BLOCK DIAGRAM

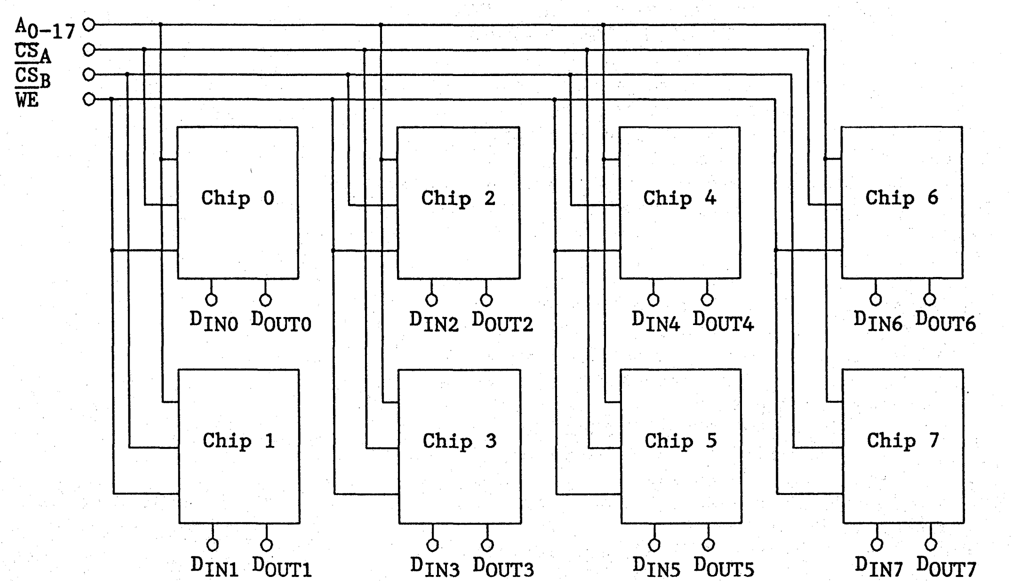
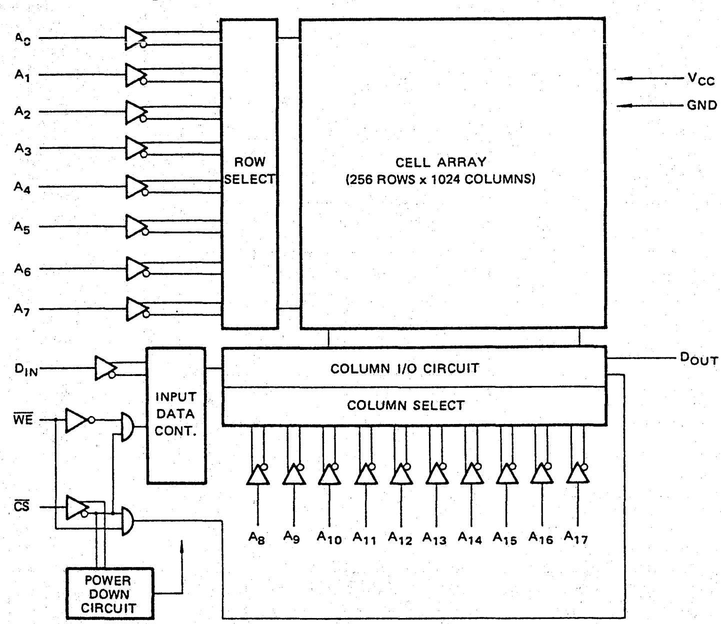


Fig. 2 – BLOCK DIAGRAM for EACH MEMORY



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (except $\overline{CS}_A$, $\overline{CS}_B$)	C_{IN}		100	pF
Input Capacitance ($\overline{CS}_A$+$\overline{CS}_B$)	$C_{\overline{CS}}$		120	pF
Output Capacitance	C_{OUT}		20	pF

FUNCTIONAL TRUTH TABLE

MODE	ADDRESS	$\overline{CS}_A$	$\overline{CS}_B$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	DON'T CARE	V_{IH}	V_{IH}	DON'T CARE	HIGH-Z	HIGH-Z	STANDBY
WRITE	VALID	V_{IL}	V_{IL}	V_{IL}	D_{IN}	HIGH-Z	ACTIVE
READ	VALID	V_{IL}	V_{IL}	V_{IH}	HIGH-Z	D_{OUT}	ACTIVE

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

DC CHARACTERISTICS

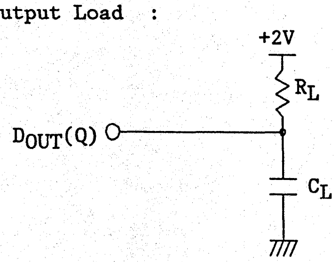
(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value Min	Value Typ	Value Max	Unit
INPUT LEAKAGE CURRENT (V_{IN}=0V to V_{CC})		I_{LI}	-80		80	µA
OUTPUT LEAKAGE CURRENT ($\overline{CS}$=V_{IH}, V_{OUT}=0V to V_{CC})		I_{LO}	-50		50	µA
STANDBY POWER SUPPLY CURRENT	CMOS level	I_{SB1}			120	mA
	TTL level	I_{SB2}			240	mA
ACTIVE POWER SUPPLY CURRENT ($\overline{CS}$=V_{IL}, I_{OUT}=0mA)	MB85403A-40	I_{CC}			960	mA
	MB85403A-50				800	
PEAK POWER ON SUPPLY CURRENT ($\overline{CS}$=Lower of V_{CC}, or V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level *[1]		V_{IL}	-0.5		0.8	V
OUTPUT HIGH LEVEL (I_{OH}=-4mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=16mA)		V_{OL}			0.4	V

Note: *[1] -3.0V min. for pulse width less than 20ns.

Fig. 3 – AC TEST CONDITIONS

- Input Pulse Levels : 0.6V to 2.4V
- Input Rise and Fall Times : 5ns
- Timing Reference Levels : V_{IL}/V_{OL}=0.8V, V_{IH}/V_{OH}=2.2V
- Output Load :



	R_L	C_L
Load I	100Ω	30pF
Load II	100Ω	5pF

4

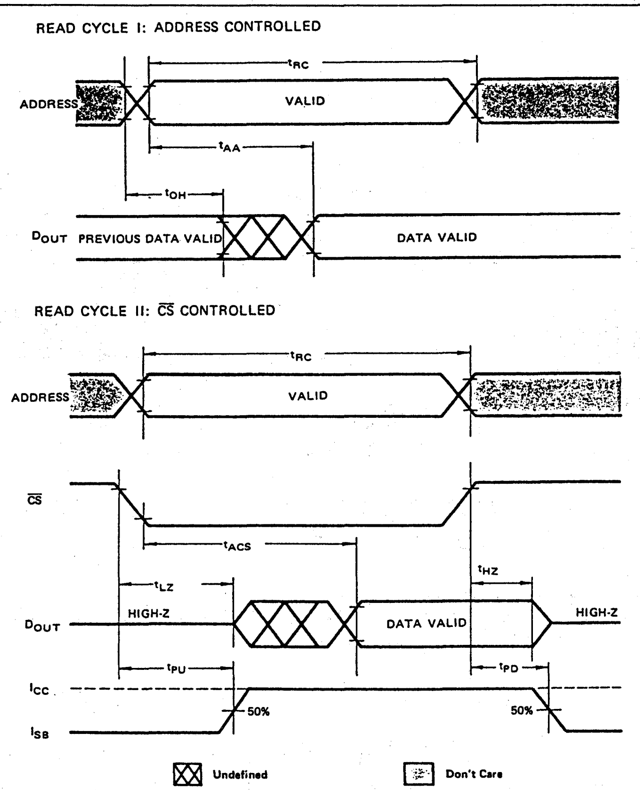
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB85403A-40		MB85403A-50		Unit
		Min	Max	Min	Max	
Read Cycle Time *2	t_{RC}	40		50		ns
Address Access Time	t_{AA}		40		50	ns
CS Access Time *3	t_{ACS}		40		50	ns
Output Hold from Address Change	t_{OH}	5		5		ns
CS to Output Low-Z *4*5	t_{LZ}	5		5		ns
CS to Output High-Z *4*5	t_{HZ}	0	25	0	30	ns
Power Up from CS	t_{PU}	0		0		ns
Power Down from CS	t_{PD}		40		50	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 WE is high during Read cycle.
*2 Device is continuously selected, $\overline{CS}=V_{IL}$.
*3 Address valid prior to or coincident with CS transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 3.

4

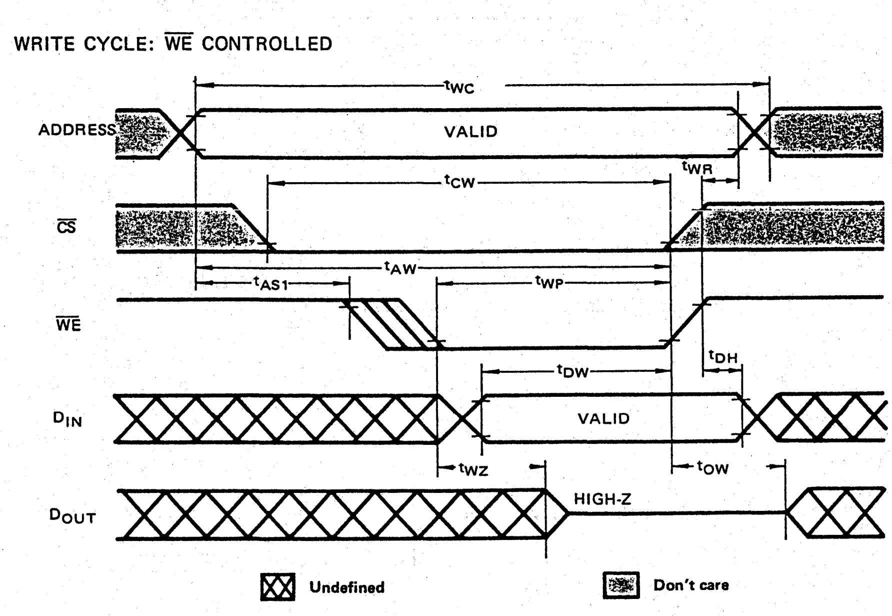
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85403A-40		MB85403A-50		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	40		50		ns
Address Valid to End of Write	t_{AW}	35		45		ns
CS to End of Write	t_{CW}	35		45		ns
Data Valid to End of Write	t_{DW}	25		30		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	25		30		ns
Address Setup Time	t_{AS1}	5		5		ns
	t_{AS2}	0		0		ns
Write Recovery Time	t_{WR}	5		5		ns
Output High-Z from $\overline{WE}$ *3*4	t_{WZ}	0	25	0	30	ns
Output Low-Z from $\overline{WE}$ *3*4	t_{OZ}	0		0		ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

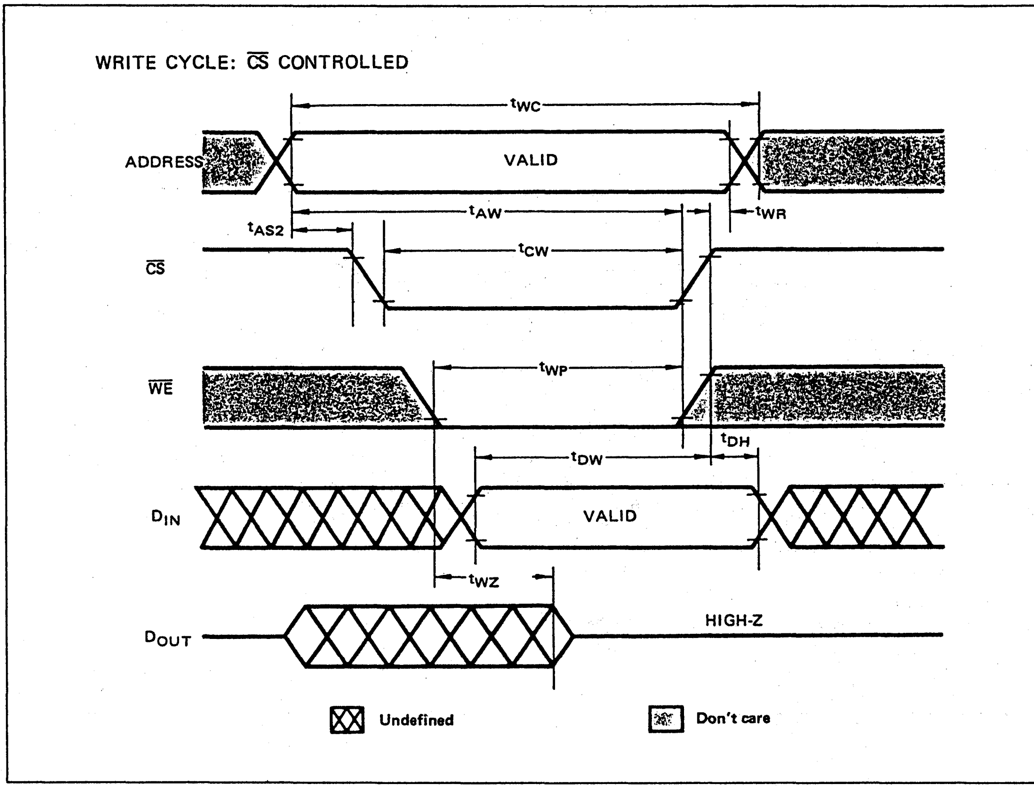
*3 Transition is measured at the point of ±500mV from steady state voltage.

*4 This parameter is specified with Load II in Fig. 3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

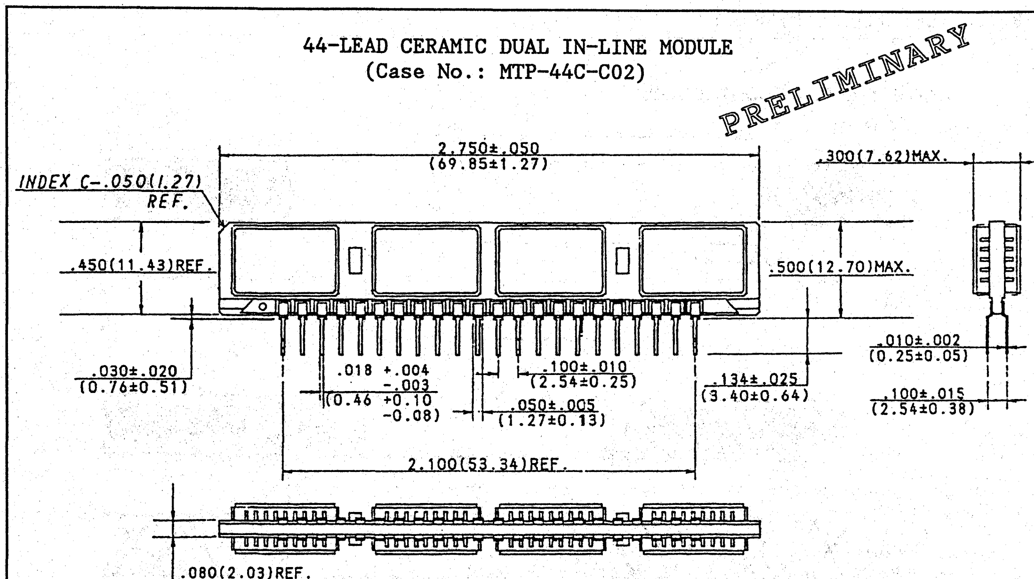


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 All write cycle are determined from last address transition to the first address transition of the next address.

4

PACKAGE DIMENSIONS
(Suffix: CVCT)

44-LEAD CERAMIC DUAL IN-LINE MODULE
(Case No.: MTP-44C-C02)



NOTE
1. Dimension in inches and (millimeters).

FUJITSU

64K x 8 CMOS SRAM MODULE

MB85410-30
MB85410-40

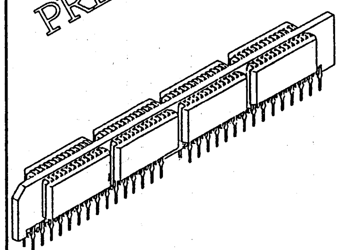
TS250-B88Y
Nov. 1988

CMOS 65,536 Words x 8-Bit HIGH SPEED STATIC RANDOM ACCESS MEMORY MODULE

The Fujitsu MB85410 is a fully decoded, CMOS static random access memory module consists of eight MB81C71A devices mounted on a 60-pin plastic board.
Organized as eight 64K x 1 devices, the MB85410 is optimized for those applications requiring high speed, high performance, large memory storage, and high density.

- Organized as 65,536 x 8-bit Words
- Memory : MB81C71A, 8 pcs
- Access Time : 30 ns max (MB85410-30)
  40 ns max (MB85410-40)
- Low Power Dissipation
  Standby: 440 mW max (CMOS level)
  880 mW max (TTL level)
  Active : 3200 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- Dual Chip Select (x8 or x4 organization)
- TTL Compatible Input/Output Pins
- 3-State Output
- Decoupling Capacitor : .22μF, 8 pcs
- 60-Pin Plastic(FR-4) ZIP

PRELIMINARY



PLASTIC PACKAGE
MZP-60P-P02

ABSOLUTE MAXIMUM RATING (See **NOTE**.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-45 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT
TOP VIEW

PD0(GND)	2	1	VSS
NC	4	3	PD1(OPEN)
VCC	6	5	NC
D0	8	7	D1
Q0	10	9	Q1
A0	12	11	NC
A2	14	13	A1
A4	16	15	A3
A6	18	17	A5
VSS	20	19	A7
D2	22	21	D3
Q2	24	23	Q3
$\overline{WE}$	26	25	VCC
NC	28	27	NC
$\overline{CS1}$	30	29	NC
NC	32	31	$\overline{CS2}$
NC	34	33	NC
VCC	36	35	NC
D4	38	37	D5
Q4	40	39	Q5
A8	42	41	VSS
A10	44	43	A9
A12	46	45	A11
A14	48	47	A13
NC	50	49	A15
D6	52	51	D7
Q6	54	53	Q7
NC	56	55	VCC
NC	58	57	NC
VSS	60	59	NC

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

4

Fig. 1 - BLOCK DIAGRAM

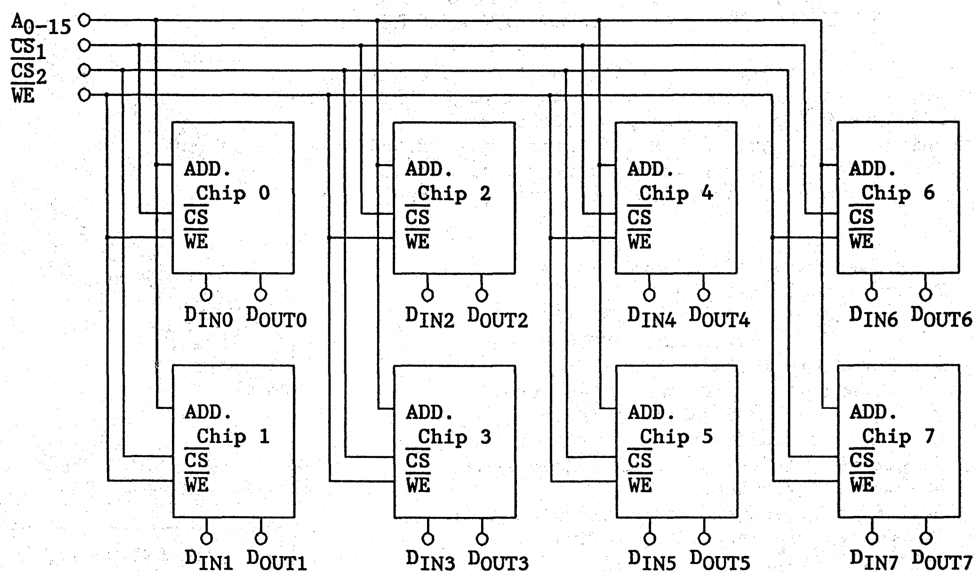
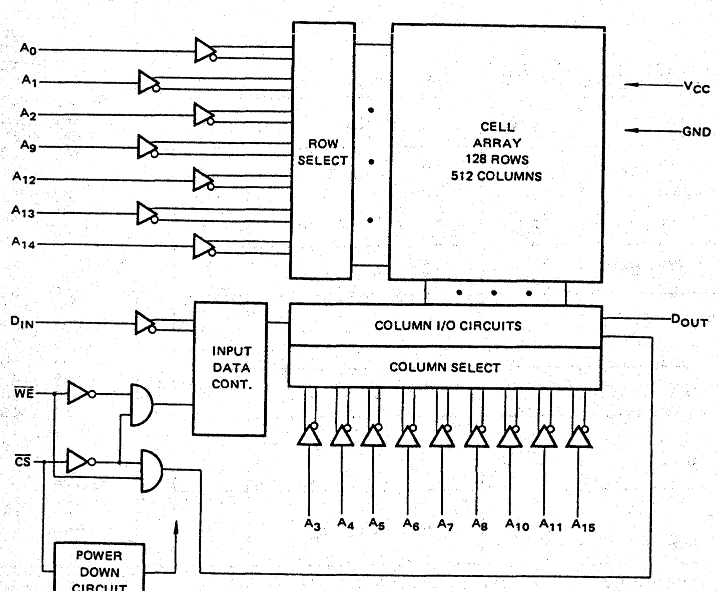


Fig. 2 - BLOCK DIAGRAM for EACH MEMORY



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, ADDRESS and $\overline{WE}$	C_{IN1}		80	pF
Input Capacitance, $\overline{CS}_1$ and $\overline{CS}_2$	C_{IN2}		40	pF
Input Capacitance, D_{IN}	C_{IN3}		10	pF
Output Capacitance, D_{OUT}	C_{OUT}		10	pF

FUNCTIONAL TRUTH TABLE

MODE	ADDRESS	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	DON'T CARE	V_{IH}	V_{IH}	DON'T CARE	HIGH-Z	HIGH-Z	STANDBY
WRITE	VALID	V_{IL}	V_{IL}	V_{IL}	D_{IN}	HIGH-Z	ACTIVE
READ	VALID	V_{IL}	V_{IL}	V_{IH}	HIGH-Z	D_{OUT}	ACTIVE

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

4

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

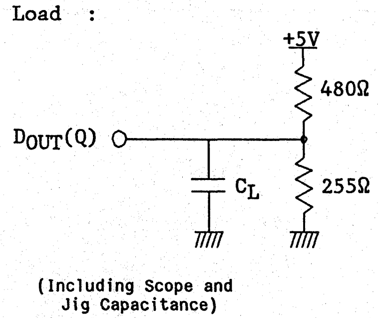
Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
INPUT LEAKAGE CURRENT (V_{IN}=0V to V_{CC})		I_{LI}	-80		80	µA
OUTPUT LEAKAGE CURRENT ($\overline{CS}$=V_{IH}, V_{OUT}=0V to V_{CC})		I_{LO}	-10		10	µA
STANDBY POWER SUPPLY CURRENT	CMOS level	I_{SB1}			80	mA
	TTL level	I_{SB2}			160	mA
ACTIVE POWER SUPPLY CURRENT ($\overline{CS}$=V_{IL}, I_{OUT}=0mA)		I_{CC}			640	mA
PEAK POWER ON SUPPLY CURRENT ($\overline{CS}$=Lower of V_{CC}, or V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level *1		V_{IL}	-0.5		0.8	V
OUTPUT HIGH LEVEL (I_{OH}=-4mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=16mA)		V_{OL}			0.4	V

Note: *1 -2.0V min. for pulse width less than 20ns.

Fig. 3 – AC TEST CONDITIONS

- Input Pulse Levels : 0.6V to 2.4V
- Input Rise and Fall Times : 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels : 1.5V (Input and Output)

- Output Load :



	C_L
Load I	30pF
Load II	5pF

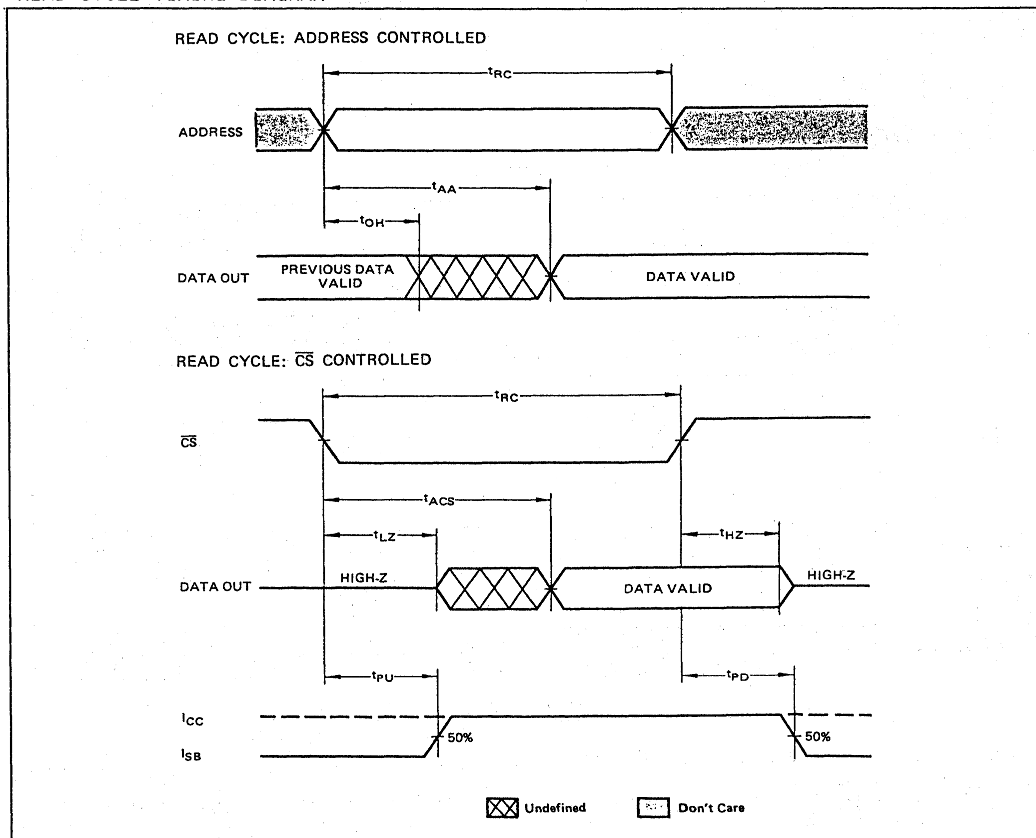
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB85410-30		MB85410-40		Unit
		Min	Max	Min	Max	
Read Cycle Time *1	t_{RC}	30		40		ns
Address Access Time	t_{AA}		30		40	ns
CS Access Time *2	t_{ACS}		30		40	ns
Output Hold from Address Change	t_{OH}	5		5		ns
CS to Output Low-Z *3*4	t_{LZ}	5		5		ns
CS to Output High-Z *3*4	t_{HZ}	0	10	0	15	ns
Power Up from CS	t_{PU}	0		0		ns
Power Down from CS	t_{PD}		20		30	ns

READ CYCLE TIMING DIAGRAM



Note: *1 Device is continuously selected, $\overline{CS}=V_{IL}$.
*2 Address valid prior to or coincident with $\overline{CS}$ transition low.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 3.

4

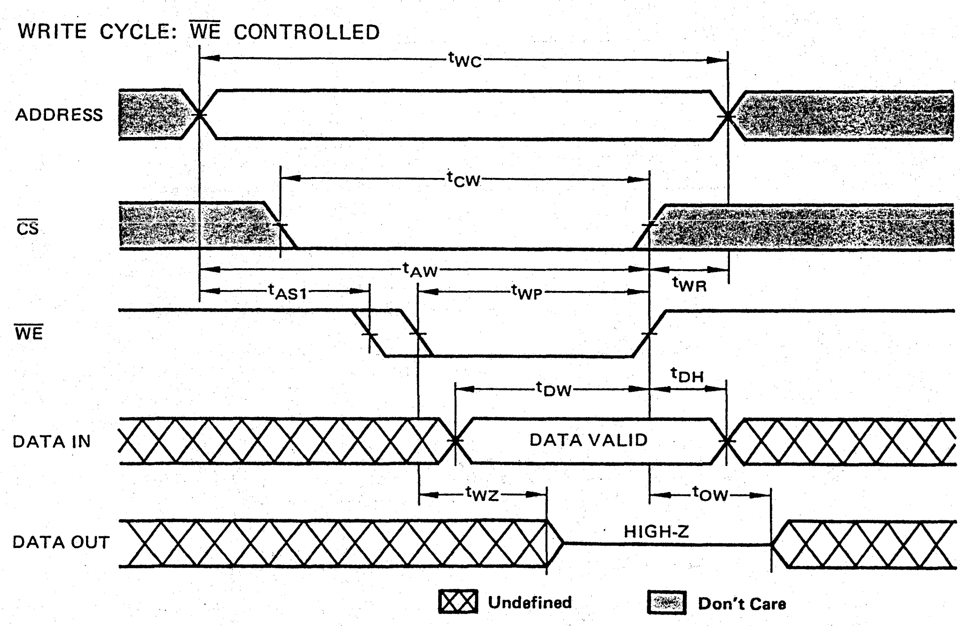
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85410-30		MB85410-40		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	30		40		ns
Address Valid to End of Write	t_{AW}	25		35		ns
CS to End of Write	t_{CW}	25		35		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	20		30		ns
Data Valid to End of Write	t_{DW}	15		20		ns
Address Setup Time	t_{AS1}	0		0		ns
	t_{AS2}	0		0		ns
Write Recovery Time	t_{WR}	2		2		ns
Output High-Z from WE *3*4	t_{WZ}	0	10	0	15	ns
Output Low-Z from WE *3*4	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If CS goes high simultaneously with WE high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

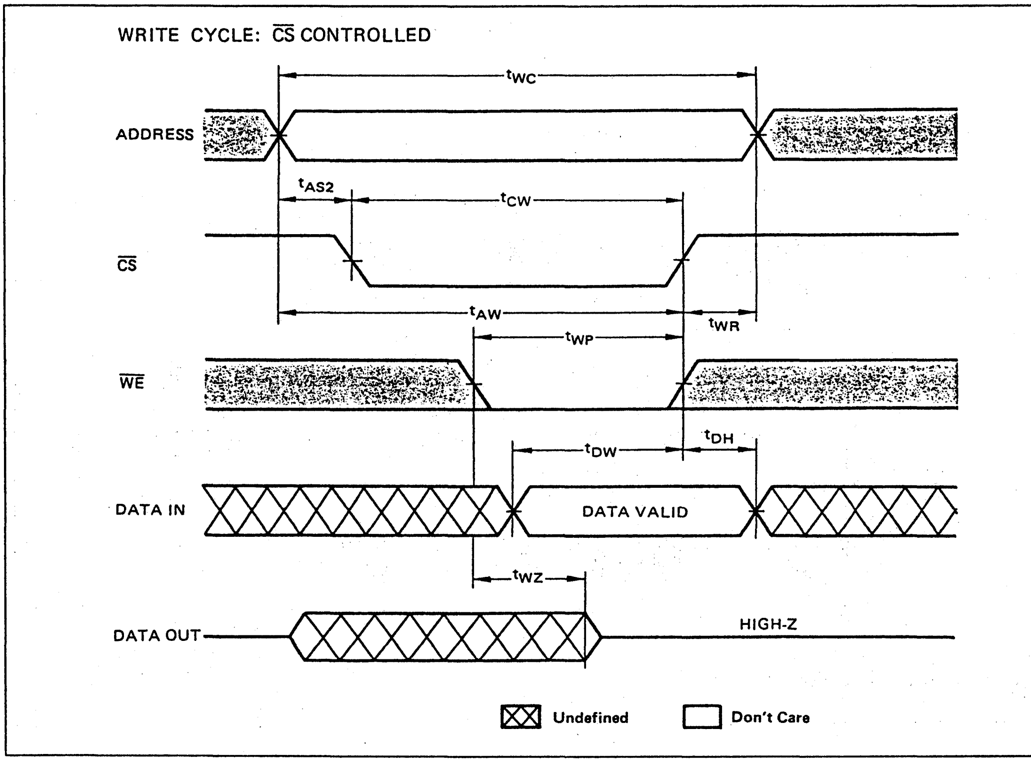
*3 Transition is measured at the point of ±500mV from steady state voltage.

*4 This parameter is specified with Load II in Fig. 3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

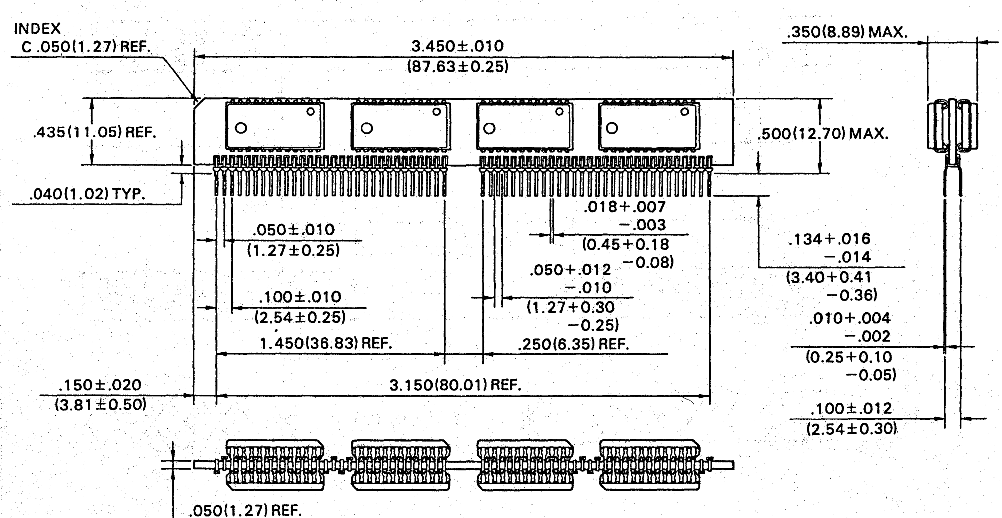
WRITE CYCLE TIMING DIAGRAM



4

PACKAGE DIMENSIONS
(Suffix: PJPZ)

60-LEAD PLASTIC MODULE
(Case No.: MZP-60P-P02)



NOTES
1. Dimension in inches and (millimeters).
2. Pin No. 1; Back side

FUJITSU

16K x 32 CMOS SRAM MODULE

MB85414-30
MB85414-40

TS260-A88Y
Nov. 1988

CMOS 16,384 Words x 32-Bit HIGH SPEED STATIC RANDOM ACCESS MEMORY MODULE

PRELIMINARY

The Fujitsu MB85414 is a fully decoded, CMOS static random access memory module consists of nine MB81C75A devices mounted on a 64-pin plastic board.
Organized as eight 16K x 4 devices, the MB85414 is optimized for those applications requiring high speed, high performance, wide word width, and high density.

- Organized as 16,384 x 32-bit Words
- Optional organization as 32,768 x 16-bit
- Memory : MB81C75A, 8 pcs
- Access Time : 30 ns max (MB85414-30)
  40 ns max (MB85414-40)
- Low Power Dissipation
  Standby: 440 mW max (CMOS level)
  880 mW max (TTL level)
  Active : 3520 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- TTL Compatible Input/Output Pins
- 3-State Output
- Decoupling Capacitor : .22µF, 8 pcs
- 64-Pin Plastic(FR-4) ZIP

PLASTIC PACKAGE
MZP-64P-P01

PIN ASSIGNMENT

TOP VIEW

PD0(GND)	2	1	VSS
DQ0	4	3	PD1(OPEN)
DQ1	6	5	DQ4
DQ2	8	7	DQ5
DQ3	10	9	DQ6
VCC	12	11	DQ7
A6	14	13	A7
A10	16	15	A5
A3	18	17	A11
DQ8	20	19	DQ12
DQ9	22	21	DQ13
DQ10	24	23	DQ14
DQ11	26	25	DQ15
$\overline{WE}$	28	27	VSS
NC	30	29	NC
$\overline{CS1}$	32	31	$\overline{CS2}$
$\overline{CS3}$	34	33	$\overline{CS4}$
NC	36	35	NC
VSS	38	37	$\overline{OE}$
DQ16	40	39	DQ20
DQ17	42	41	DQ21
DQ18	44	43	DQ22
DQ19	46	45	DQ23
A1	48	47	A2
A9	50	49	A4
A0	52	51	A13
A12	54	53	VCC
DQ24	56	55	A8
DQ25	58	57	DQ28
DQ26	60	59	DQ29
DQ27	62	61	DQ30
VSS	64	63	DQ31

ABSOLUTE MAXIMUM RATING (See **NOTE.**)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-45 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 - BLOCK DIAGRAM

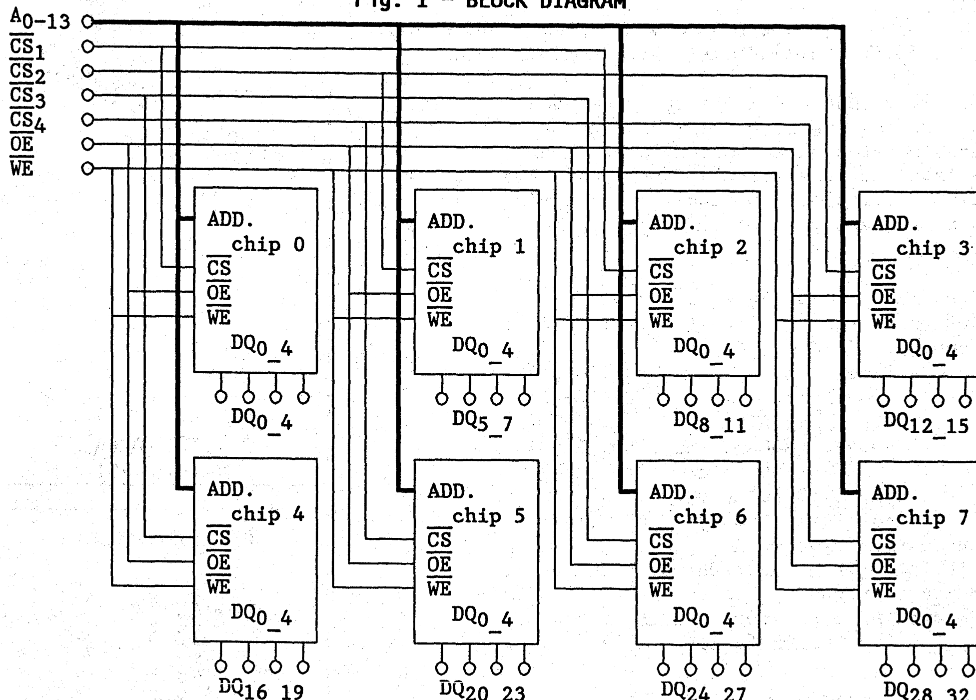
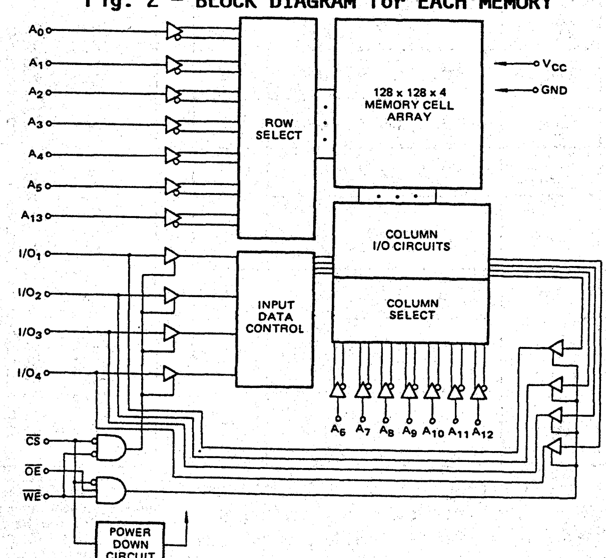


Fig. 2 - BLOCK DIAGRAM for EACH MEMORY



4

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, ADDRESS	C_{IN1}		80	pF
Input Capacitance, $\overline{CS}$	C_{IN2}		30	pF
Input Capacitance, $\overline{WE}$ and $\overline{OE}$	C_{IN3}		80	pF
Input Capacitance, I/O	$C_{I/O}$		12	pF

FUNCTIONAL TRUTH TABLE

MODE	ADDRESS	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
STANDBY	X	V_{IH}	X	X	HIGH-Z	STANDBY
OUTPUT DISABLE	VALID	V_{IL}	V_{IH}	V_{IH}	HIGH-Z	ACTIVE
WRITE	VALID	V_{IL}	V_{IL}	X	HIGH-Z	ACTIVE
READ	VALID	V_{IL}	V_{IH}	V_{IL}	D_{OUT}	ACTIVE

X can be either V_{IH} or V_{IL}.

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

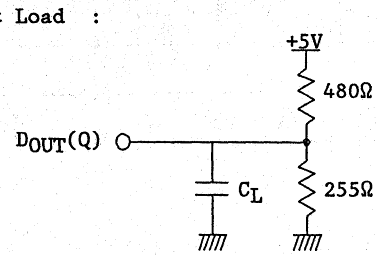
Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
INPUT LEAKAGE CURRENT (V_{IN}=0V to V_{CC})		I_{LI}	-80		80	µA
OUTPUT LEAKAGE CURRENT ($\overline{CS}$=V_{IH}, V_{OUT}=0V to V_{CC})		I_{LO}	-10		10	µA
STANDBY POWER SUPPLY CURRENT	CMOS level	I_{SB1}			80	mA
	TTL level	I_{SB2}			160	mA
ACTIVE POWER SUPPLY CURRENT ($\overline{CS}$=V_{IL}, I_{OUT}=0mA)		I_{CC1}			480	mA
OPERATING SUPPLY CURRENT (Cycle=Min., I_{OUT}=0mA)		I_{CC2}			640	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level *[1]		V_{IL}	-0.5		0.8	V
OUTPUT HIGH LEVEL (I_{OH}=-4mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=8mA)		V_{OL}			0.4	V

Note: *[1] -2.0V min. for pulse width less than 20ns.

Fig. 3 – AC TEST CONDITIONS

- Input Pulse Levels : 0V to 3V
- Input Rise and Fall Times : 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels : 1.5V (Input and Output)

- Output Load :



(Including Scope and Jig Capacitance)

	C_L
Load I	30pF
Load II	5pF

4

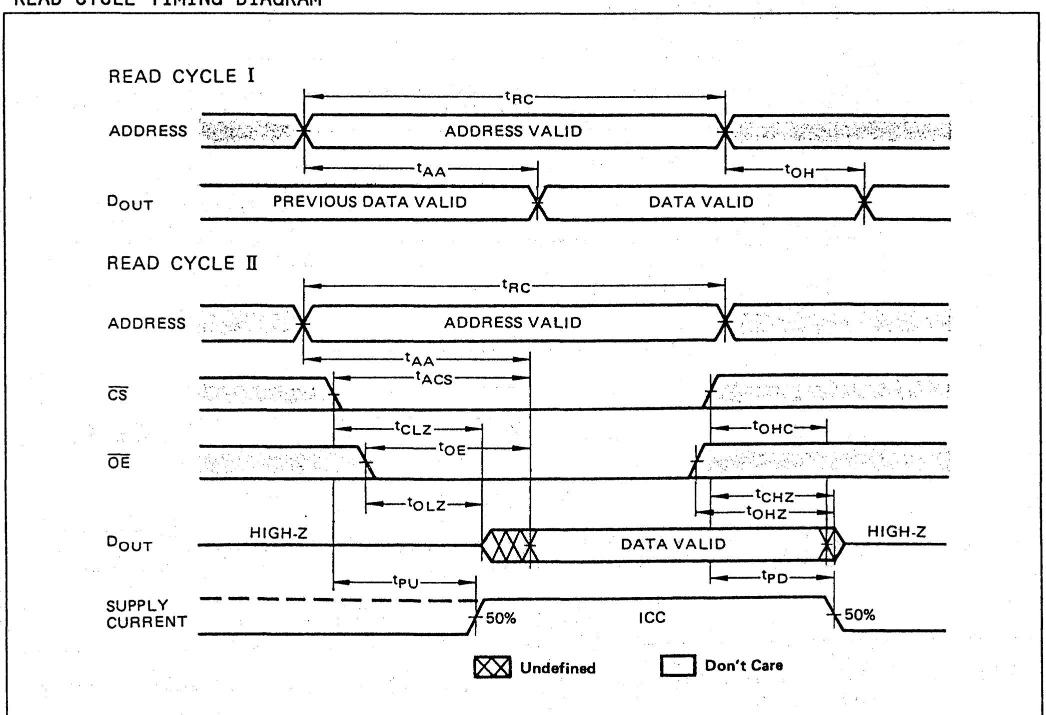
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB85414-30		MB85414-40		Unit
		Min	Max	Min	Max	
Read Cycle Time *1	t_{RC}	30		40		ns
Address Access Time	t_{AA}		30		40	ns
CS Access Time *2	t_{ACS}		30		40	ns
OE Access Time *2	t_{OE}		15		20	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from Output Disable	t_{OHC}	3		3		ns
CS to Output Low-Z *3*4	t_{CLZ}	5		5		ns
OE to Output Low-Z *3*4	t_{OLZ}	0		0		ns
CS to Output High-Z *3*4	t_{CHZ}		10		15	ns
OE to Output High-Z *3*4	t_{OHZ}		10		15	ns
Power Up from CS	t_{PU}	0		0		ns
Power Down from CS	t_{PD}		20		30	ns

READ CYCLE TIMING DIAGRAM



Note: *1 Device is continuously selected, $\overline{CS}=V_{IL}$.
*2 Address valid prior to or coincident with $\overline{CS}$ transition low.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 3.

4

AC CHARACTERISTICS

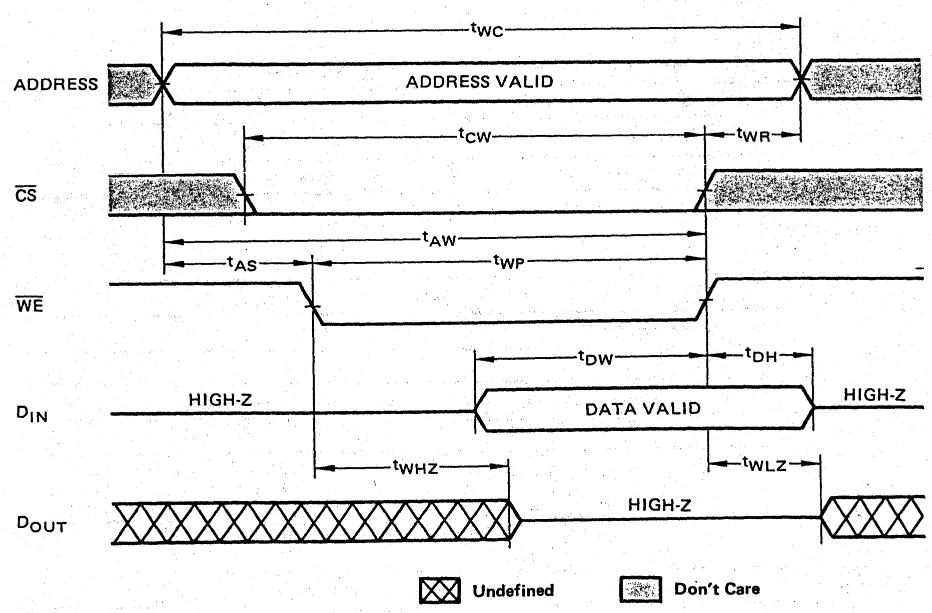
(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85414-30		MB85414-40		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	30		40		ns
Address Valid to End of Write	t_{AW}	25		35		ns
CS to End of Write	t_{CW}	25		35		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	20		30		ns
Data Valid to End of Write	t_{DW}	15		20		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	2		2		ns
Output High-Z from WE *3*4	t_{WHZ}		10		15	ns
Output Low-Z from WE *3*4	t_{WLZ}	0	20	0	30	ns

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE I: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

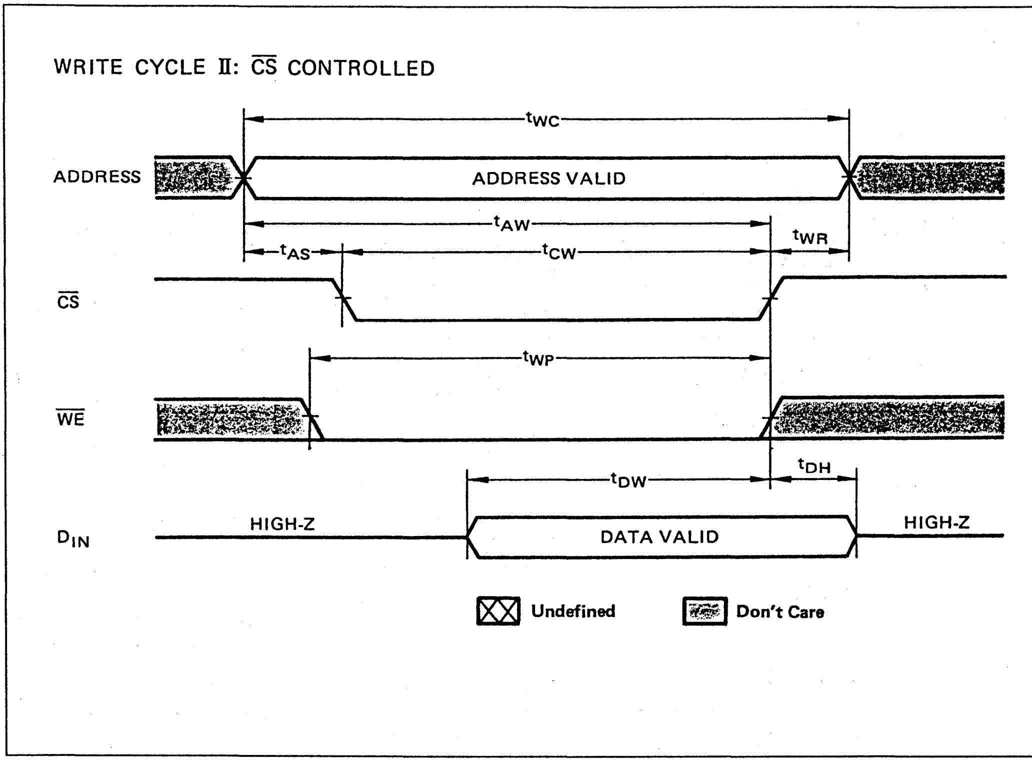
*3 Transition is measured at the point of ±500mV from steady state voltage.

*4 This parameter is specified with Load II in Fig. 3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

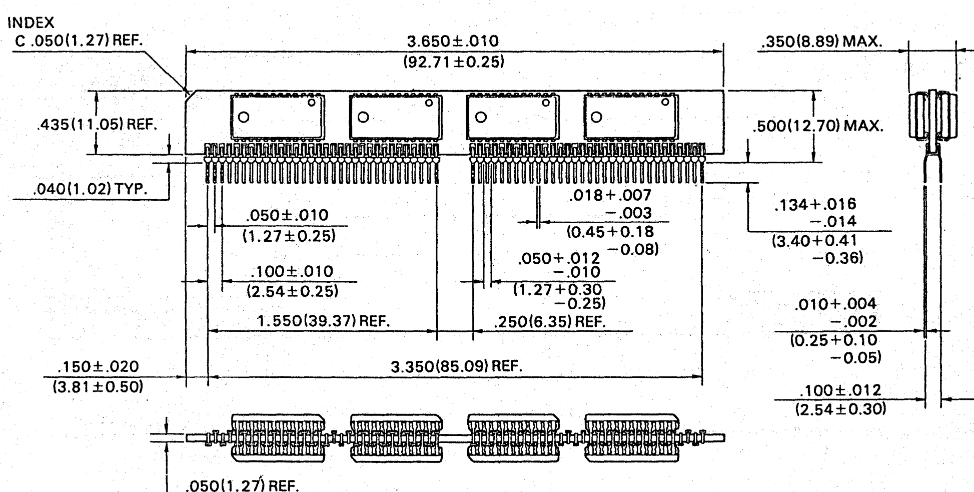
WRITE CYCLE TIMING DIAGRAM



4

PACKAGE DIMENSIONS
(Suffix: PJPZ)

64-LEAD PLASTIC MODULE
(Case No.: MZP-64P-P01)



NOTES
1. Dimension in inches and (millimeters).
2. Pin No. 1; Back side.

FUJITSU

256K x 8 CMOS SRAM MODULE

MB85420-40
MB85420-50

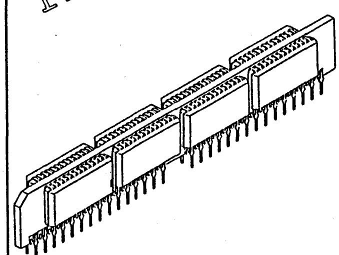
TS251-B88Y
Nov. 1988

CMOS 262,144 Words x 8-Bit HIGH SPEED STATIC RANDOM ACCESS MEMORY MODULE

PRELIMINARY

The Fujitsu MB85420 is a fully decoded, CMOS static random access memory module consists of eight MB81C81A devices mounted on a 60-pin plastic board.
Organized as eight 256K x 1 devices, the MB85420 is optimized for those applications requiring high speed, high performance, large memory storage, and high density.

- Organized as 262,144 x 8-bit Words
- Memory : MB81C81A, 8 pcs
- Access Time : 40 ns max (MB85420-40)
  50 ns max (MB85420-50)
- Low Power Dissipation
  Standby: 660 mW max (CMOS level)
  1320 mW max (TTL level)
  Active : 5280 mW max (MB85420-40)
  4400 mW max (MB85420-50)
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- Dual Chip Select (x8 or x4 organization)
- TTL Compatible Input/Output Pins
- 3-State Output
- Decoupling Capacitor : .22μF, 8pcs
- 60-Pin Plastic(FR-4) ZIP
- Upgrade version of MB85410



PLASTIC PACKAGE
MZP-60P-P02

ABSOLUTE MAXIMUM RATING (See NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-45 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT
TOP VIEW

PD0(OPEN)	2	1	VSS
NC	4	3	PD1(GND)
VCC	6	5	NC
D0	8	7	D1
Q0	10	9	Q1
A	12	11	NC
A	14	13	A
A	16	15	A
A	18	17	A
VSS	20	19	A
D2	22	21	D3
Q2	24	23	Q3
$\overline{WE}$	26	25	VCC
A	28	27	A
$\overline{CS1}$	30	29	NC
NC	32	31	$\overline{CS2}$
NC	34	33	NC
VCC	36	35	NC
D4	38	37	D5
Q4	40	39	Q5
A	42	41	VSS
A	44	43	A
A	46	45	A
A	48	47	A
NC	50	49	A
D6	52	51	D7
Q6	54	53	Q7
NC	56	55	VCC
NC	58	57	NC
VSS	60	59	NC

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – BLOCK DIAGRAM

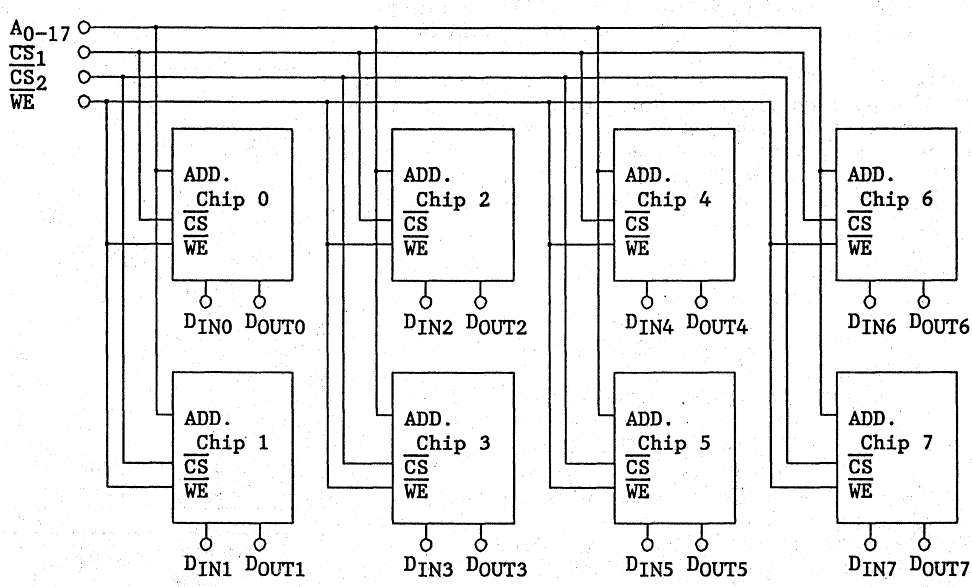
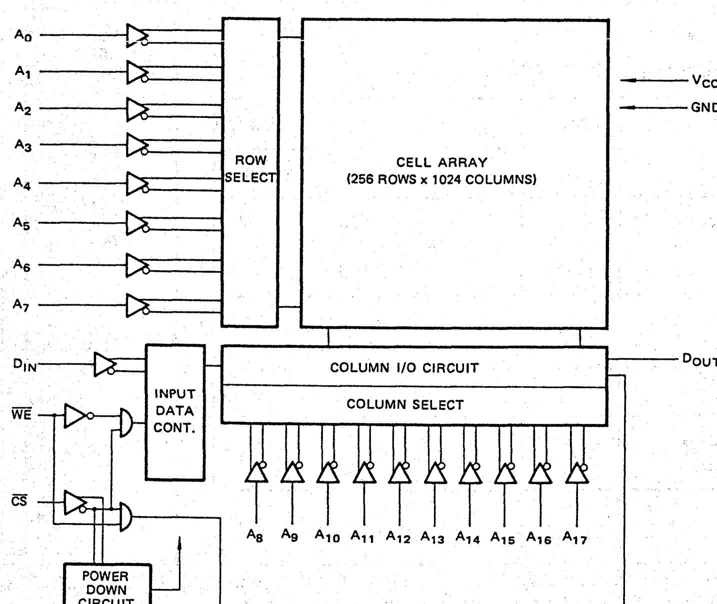


Fig. 2 – BLOCK DIAGRAM for EACH MEMORY



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, ADDRESS and $\overline{WE}$	C_{IN1}		70	pF
Input Capacitance, $\overline{CS}_1$ and $\overline{CS}_2$	C_{IN2}		45	pF
Input Capacitance, D_{IN}	C_{IN3}		9	pF
Output Capacitance, D_{OUT}	C_{OUT}		12	pF

FUNCTIONAL TRUTH TABLE

MODE	ADDRESS	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	DON'T CARE	V_{IH}	V_{IH}	DON'T CARE	HIGH-Z	HIGH-Z	STANDBY
WRITE	VALID	V_{IL}	V_{IL}	V_{IL}	D_{IN}	HIGH-Z	ACTIVE
READ	VALID	V_{IL}	V_{IL}	V_{IH}	HIGH-Z	D_{OUT}	ACTIVE

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

4

DC CHARACTERISTICS

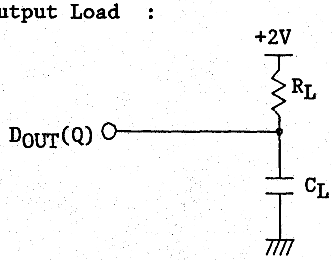
(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value Min	Value Typ	Value Max	Unit
INPUT LEAKAGE CURRENT (V_{IN}=0V to V_{CC})		I_{LI}	-80		80	μA
OUTPUT LEAKAGE CURRENT ($\overline{CS}=V_{IH}$, V_{OUT}=0V to V_{CC})		I_{LO}	-50		50	μA
STANDBY POWER SUPPLY CURRENT	CMOS level	I_{SB1}			120	mA
	TTL level	I_{SB2}			240	mA
ACTIVE POWER SUPPLY CURRENT ($\overline{CS}=V_{IL}$, I_{OUT}=0mA)	MB85420-40	I_{CC}			960	mA
	MB85420-50				800	mA
PEAK POWER ON SUPPLY CURRENT ($\overline{CS}$=Lower of V_{CC}, or V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level *[1]		V_{IL}	-0.5		0.8	V
OUTPUT HIGH LEVEL (I_{OH}=-4mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=16mA)		V_{OL}			0.4	V

Note: *[1] -3.0V min. for pulse width less than 20ns.

Fig. 3 – AC TEST CONDITIONS

- Input Pulse Levels : 0.6V to 2.4V
- Input Rise and Fall Times : 5ns
- Timing Reference Levels : V_{IL}/V_{OL}=0.8V, V_{IH}/V_{OH}=2.2V
- Output Load :



	R_L	C_L
Load I	100Ω	30pF
Load II	100Ω	5pF

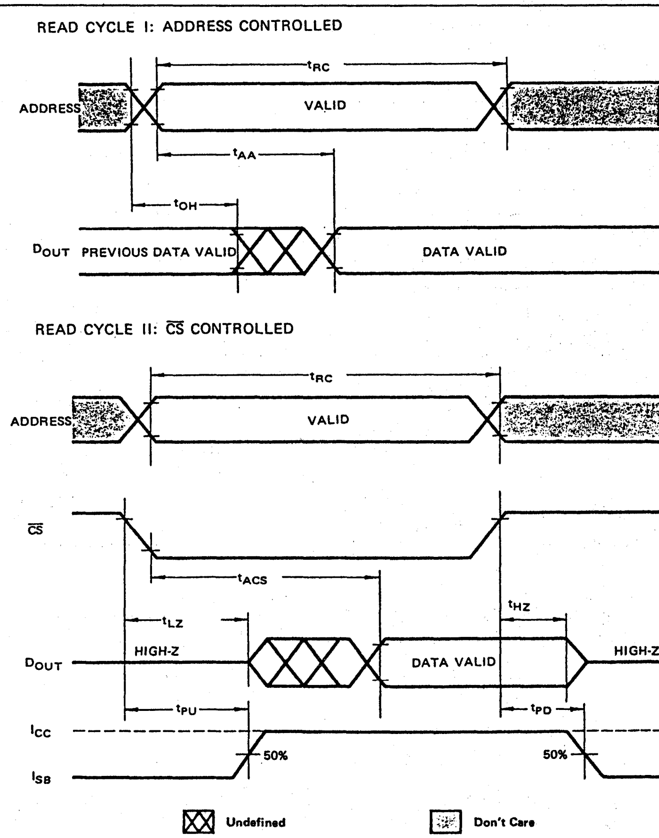
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB85420-40		MB85420-50		Unit
		Min	Max	Min	Max	
Read Cycle Time *1	t_{RC}	40		50		ns
Address Access Time	t_{AA}		40		50	ns
CS Access Time *2	t_{ACS}		40		50	ns
Output Hold from Address Change	t_{OH}	5		5		ns
CS to Output Low-Z *3*4	t_{LZ}	5		5		ns
CS to Output High-Z *3*4	t_{HZ}	0	20	0	25	ns
Power Up from CS	t_{PU}	0		0		ns
Power Down from CS	t_{PD}		40		50	ns

READ CYCLE TIMING DIAGRAM



Note: *1 Device is continuously selected, $\overline{CS}=V_{IL}$.
*2 Address valid prior to or coincident with $\overline{CS}$ transition low.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 3.

4

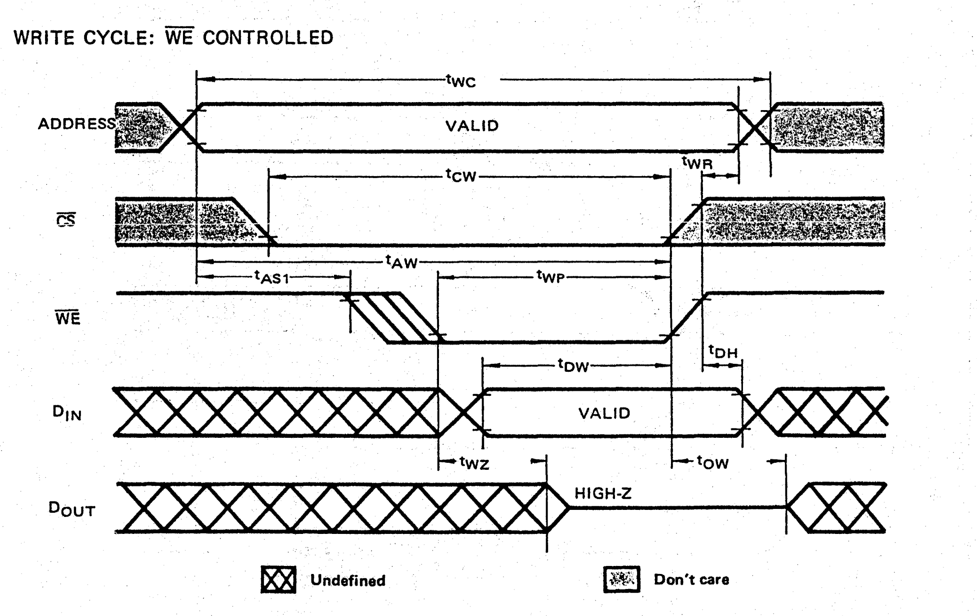
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85420-40		MB85420-50		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	40		50		ns
Address Valid to End of Write	t_{AW}	35		45		ns
CS to End of Write	t_{CW}	35		45		ns
Data Valid to End of Write	t_{DW}	20		25		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	30		35		ns
Address Setup Time	t_{AS1}	5		5		ns
	t_{AS2}	0		0		ns
Write Recovery Time	t_{WR}	5		5		ns
Output High-Z from WE *3*4	t_{WZ}	0	20	0	25	ns
Output Low-Z from WE *3*4	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

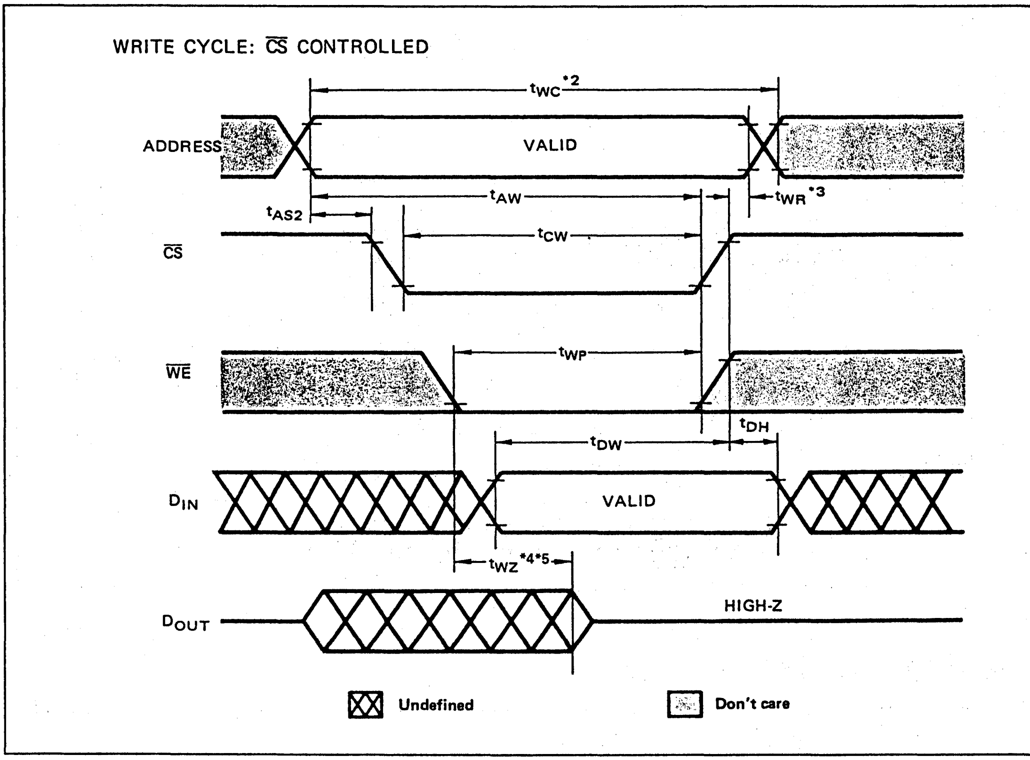
*3 Transition is measured at the point of ±500mV from steady state voltage.

*4 This parameter is specified with Load II in Fig. 3.

AC CHARACTERISTICS (Continued)

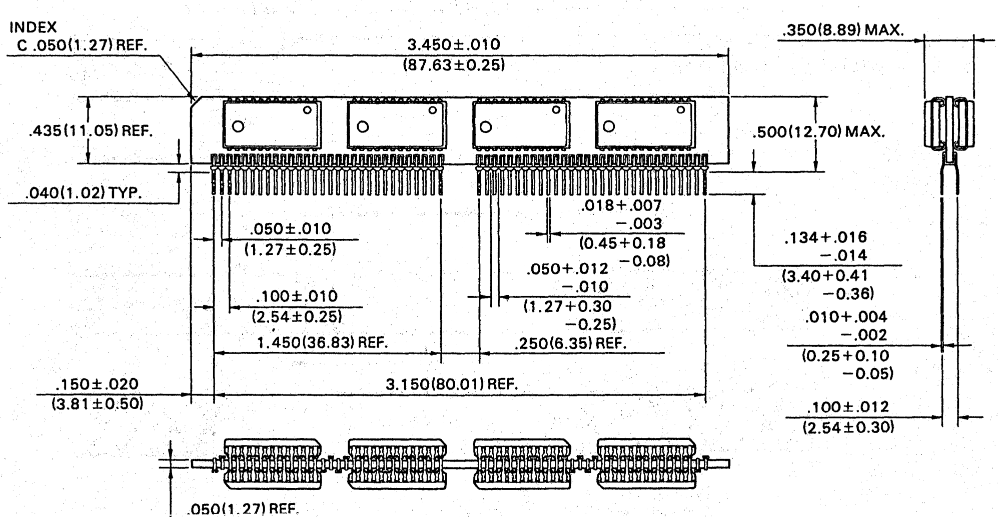
(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM



PACKAGE DIMENSIONS
(Suffix: PJPZ)

60-LEAD PLASTIC MODULE
(Case No.: MZP-60P-P02)



NOTES
1. Dimension in inches and (millimeters).
2. Pin No.1; Back side

Section 5

High-Speed CMOS SRAMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options	Sealing Method
5-3	MB81C67-35	35	16384 bits	20-pin Ceramic DIP	CERDIP
	MB81C67-45	45	(16384w x 1b)	20-pad Ceramic LCC	Frit Glass
	MB81C67-55	55		20-pin Plastic DIP	Plastic
5-15	MB81C68A-25	25	16384 bits	20-pin Ceramic DIP	CERDIP
	MB81C68A-30	30	(4096w x 4b)	20-pin Plastic DIP	Plastic
	MB81C68A-35	35		20-pin Plastic ZIP	Plastic
5-27	MB81C69A-25	35	16384 bits	20-pin Ceramic DIP	CERDIP
	MB81C69A-30	45	(4096w x 4b)	20-pin Plastic DIP	Plastic
	MB81C69A-35	55			
5-39	MB81C71-45	45	65536 bits	22-pin Ceramic DIP	Metal
	MB81C71-55	55	(65536w x 1b)	22-pad Ceramic LCC	Metal
				22-pin Plastic DIP	Plastic
5-49	MB81C71A-25	25	65536 bits	22-pin Plastic DIP	Plastic
	MB81C71A-35	35	(65536w x 1b)	24-pad Plastic LCC	Plastic
5-61	MB81C74-25	25	65536 bits	22-pin Plastic DIP	Plastic
	MB81C74-35	35	(16384w x 4b)	22-pad Ceramic LCC	Metal
5-71	MB81C75-25	25	65536 bits	24-pin Plastic DIP	Plastic
	MB81C75-35	35	(16384w x 4b)	24-pad Plastic LCC	Plastic
5-83	MB81C78A-35	35	65536 bits	28-pin Plastic DIP	Plastic
	MB81C78A-45	45	(8192w x 8b)	28-pin Plastic FPT	Plastic
				32-pad Ceramic LCC	Metal
5-97	MB81C79A-35	35	73728 bits	28-pin Plastic DIP	Plastic
	MB81C79A-45	45	(8192w x 9b)	28-pin Plastic FPT	Plastic
				32-pad Ceramic LCC	Metal
5-111	MB82B79-15	15	73728 bits	32-pin Plastic DIP	Plastic
	MB82B79-20	20	(8192w x 9b)	32-pin Plastic FPT	Plastic
5-121	MB81C81A-35	35	262144 bits	24-pin Plastic DIP	Plastic
	MB81C81A-45	45	(262144w x 1b)	24-pin Ceramic DIP	Metal
				24-pad Ceramic LCC	Metal
				24-pad Plastic LCC	Plastic
5-133	MB81C84A-35	35	262144 bits	24-pin Plastic DIP	Plastic
	MB81C84A-45	45	(65536w x 4b)	24-pad Plastic LCC	Plastic
5-141	MB81C86-55	55	262144 bits	28-pin Ceramic DIP	Metal
	MB81C86-70	70	(65536w x 4b)	32-pad Ceramic LCC	Metal
5-149	MB8289-25	25	262144 bits	32-pin Plastic DIP	Plastic
	MB8289-35	35	(32768w x 9b)	32-pin Plastic FPT	Plastic

5

FUJITSU

CMOS 16384-BIT STATIC RANDOM ACCESS MEMORY

MB 81C67-35
MB 81C67-45
MB 81C67-55

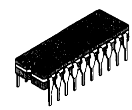
March 1986
Edition 2.0

16,384 WORDS x1 BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY

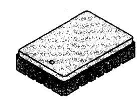
The Fujitsu MB 81C67 is 16,384 words x 1 bit static random access memory fabricated with a CMOS silicon gate process. All pins are TTL compatible and a single 5 volts power supply is required.

For ease of use, chip select ($\overline{CS}$) permits the selection of an individual package when outputs are OR-tied, and automatically power down the MB 81C67. All devices offer the advantages of low power dissipation, low cost, and high performance.

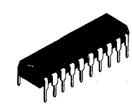
- Organization: 16,384 words x 1 bit
- Static operation: No clocks or refresh required
- Fast access time: 35 ns max. (MB 81C67-35)
  45 ns max. (MB 81C67-45)
  55 ns max. (MB 81C67-55)
- Single +5 V supply, ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- Standard 20-pin DIP package (Suffix: CZ, Suffix: P)
- Standard 20-pad Leadless Chip Carrier (Suffix: TV)
- Pin compatible with Fujitsu MB 8167A



CERAMIC PACKAGE
CERDIP
DIP-20C-C03

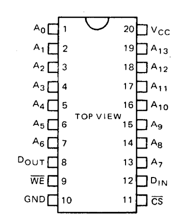


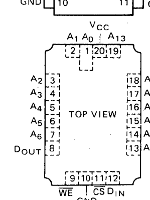
CERAMIC PACKAGE
LCC-20C-F01



PLASTIC PACKAGE
DIP-20P-M01

PIN ASSIGNMENT





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	-3.5 to +7.0	V
Output Voltage on any pin with respect to GND		V_{OUT}	-0.5 to +7.0	V
Output Current		I_{OUT}	±50	mA
Power Dissipation		P_D	1.2	W
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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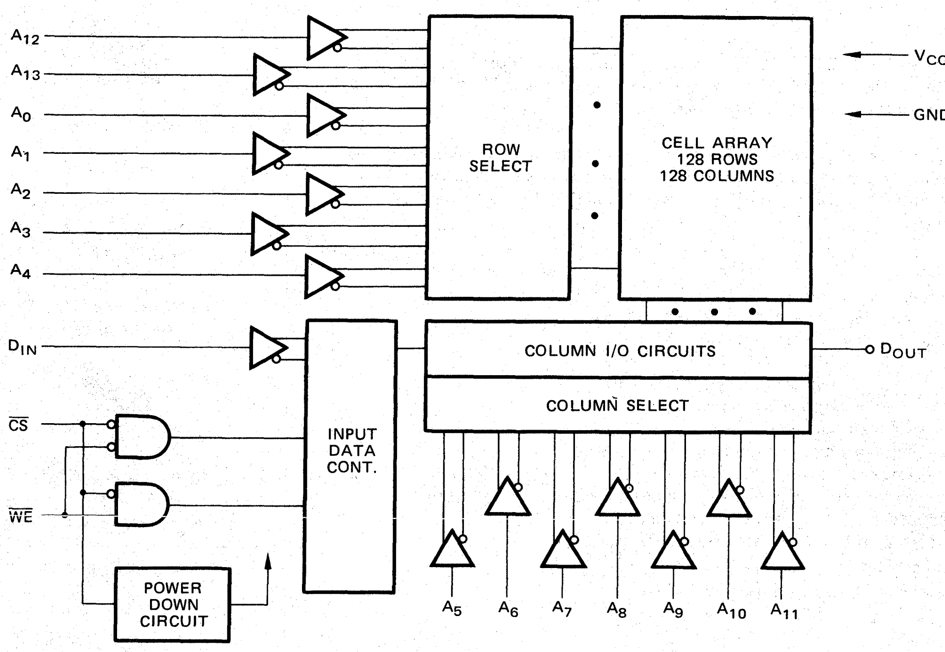
Fig. 1 – MB 81C67 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-3.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

*-3.0V Min. for pulse width less than 20ns. (V_{IL} Min = -1.0 V at DC level)

DC CHARACTERISTICS

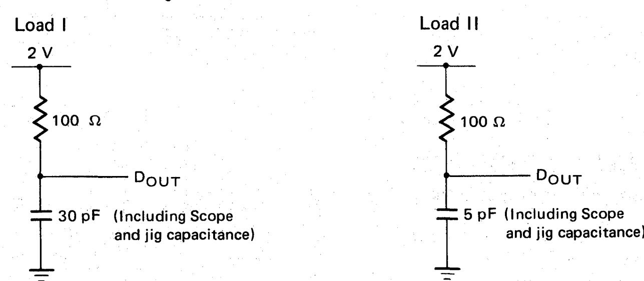
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	-2.0		2.0	μA
Output Leakage Current	$\overline{CS} = V_{IH}$, V_{OUT} = 0 V to V_{CC}	I_{LO}	-2.0		2.0	μA
Active Supply Current	$\overline{CS} = V_{IL}$, I_{OUT} = 0 mA $V_{IN} = V_{IL}$ or V_{IH}	I_{CC1}		25	40	mA
Operating Supply Current	$\overline{CS} = V_{IL}$, I_{OUT} = 0 mA Cycle = Min, C_L = 0 pF	I_{CC2}		35	60	mA
Standby Supply Current	$\overline{CS} \geqq V_{CC} - 0.2$ V $V_{IN} \geqq V_{CC} - 0.2$ V or $V_{IN} \leqq 0.2$ V	I_{SB1}		2	15	mA
Standby Supply Current	$\overline{CS} = V_{IH}$	I_{SB2}		15	25	mA
Output Low Voltage	I_{OL} = 16 mA	V_{OL}			0.4	V
Output High Voltage	I_{OH} = -4 mA	V_{OH}	2.4			V

AC TEST CONDITIONS

Input Pulse Levels :	0.6 V to 2.4 V
Input Pulse Rise And Fall Times :	5 ns
Timing Measurement Reference Levels :	Input : 1.5 V Output : 1.5 V

Output Load : Fig. 2



(For t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

AC CHARACTERISTICS

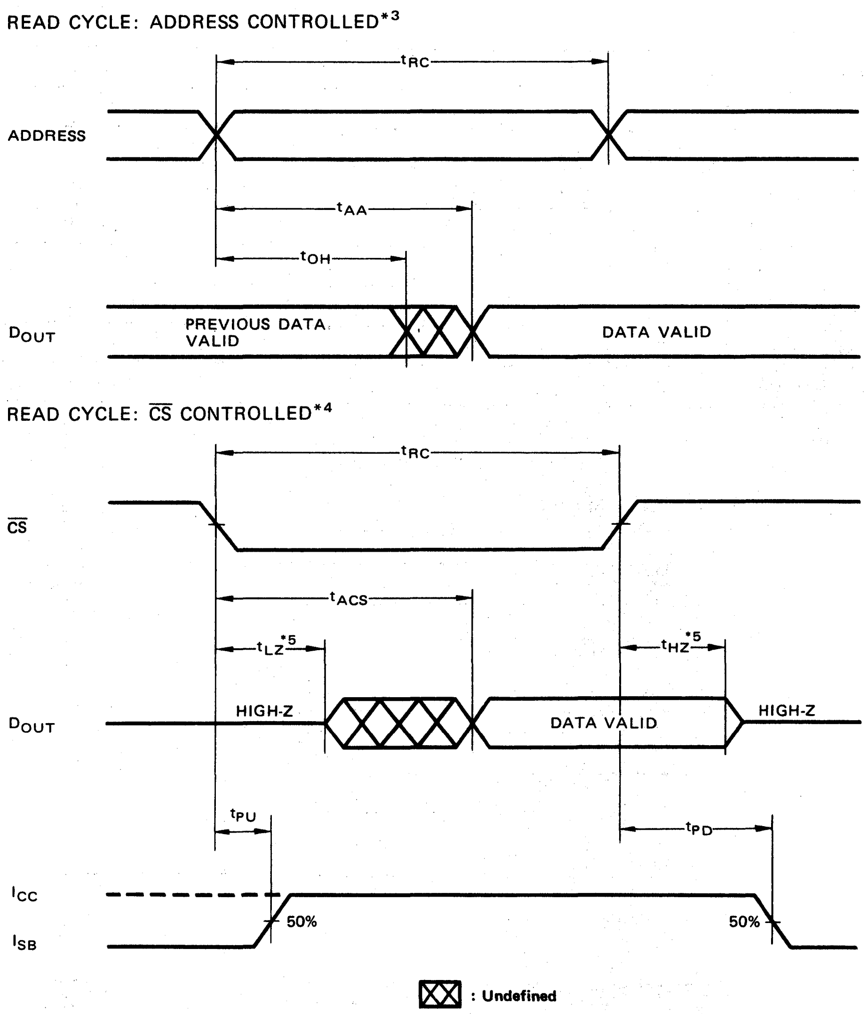
(Recommended operating conditions unless otherwise noted.)

READ CYCLE[*1]

Parameter	Symbol	MB 81C67-35		MB 81C67-45		MB 81C67-55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time [*2]	t_{RC}	35		45		55		ns
Address Access Time [*3]	t_{AA}		35		45		55	ns
Chip Select Access Time [*4]	t_{ACS}		35		45		55	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low-Z [*5]	t_{LZ}	5		5		5		ns
Chip Deselection to Output in High-Z [*5]	t_{HZ}	0	25	0	25	0	30	ns
Chip Selection to Power Up	t_{PU}	0		0		0		ns
Chip Deselection to Power Down	t_{PD}		30		40		50	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle are determined from the last address transition to the first address transition of the next address.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

READ CYCLE TIMING DIAGRAM*1*2



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle are determined from the last address transition to the first address transition of the next address.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

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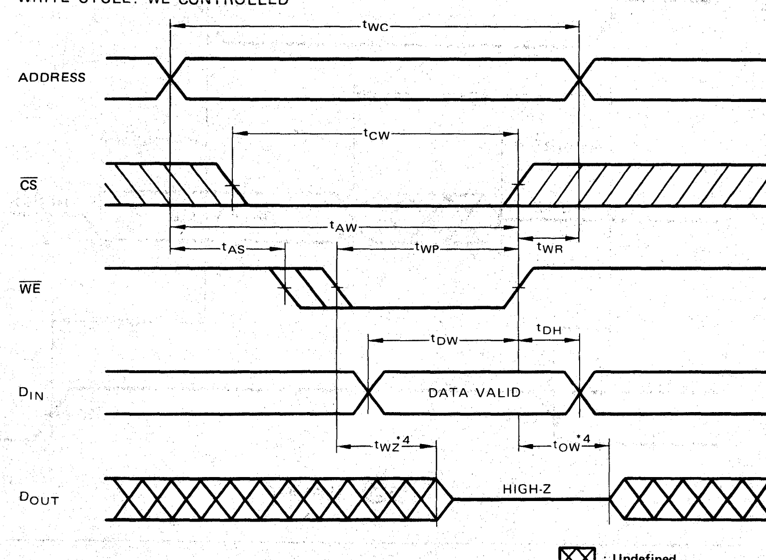
WRITE CYCLE[*1*2]

Parameter	Symbol	MB 81C67-35		MB 81C67-45		MB 81C67-55		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time[*3]	t_{WC}	35		45		55		ns
Chip Selection to End of Write	t_{CW}	30		35		50		ns
Address Valid to End of Write	t_{AW}	30		35		50		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Valid to End of Write	t_{DW}	20		20		25		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Output in High-Z[*4]	t_{WZ}	0	25	0	25	0	30	ns
Output Active from End of Write[*4]	t_{OW}	0	25	0	25	0	30	ns

WRITE CYCLE TIMING DIAGRAM[*1*2]

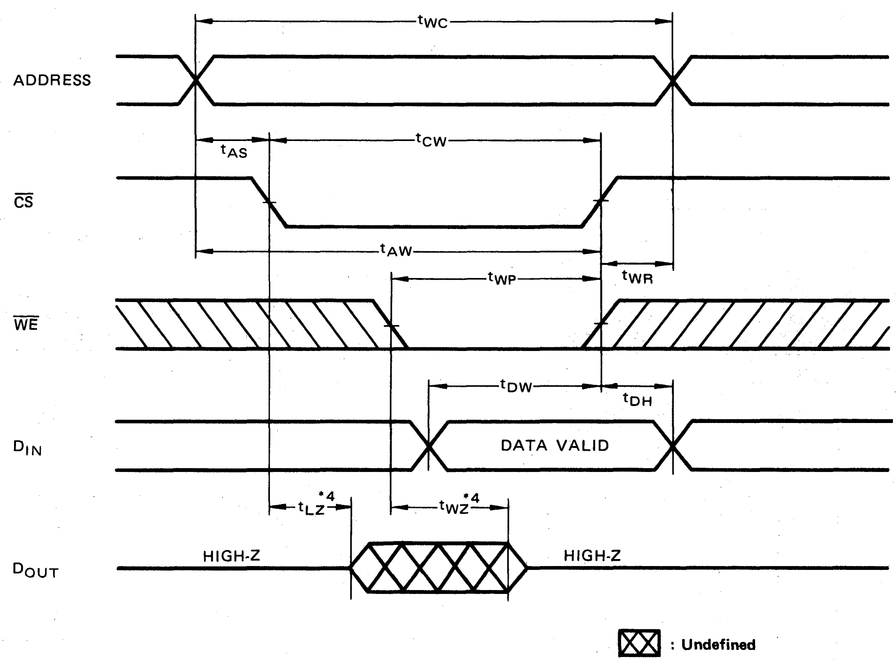
WRITE CYCLE: $\overline{WE}$ CONTROLLED[*3]



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle are determined from the last address transition to the first address transition of next address.
*4 Transition is measured at the point of ±500mV from steady state voltage.

WRITE CYCLE TIMING DIAGRAM[*1*2]

WRITE CYCLE: $\overline{CS}$ CONTROLLED[*3]



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transistion.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle are determined from the last address transistion to the first address transition of next address.
*4 Transition is measured at the point of ±500mV from steady state voltage.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

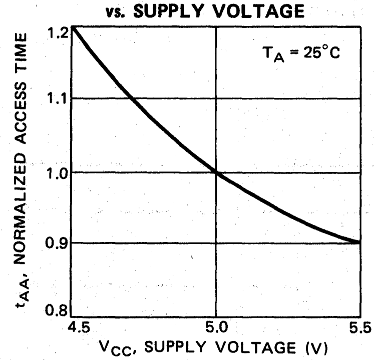


Fig. 4 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

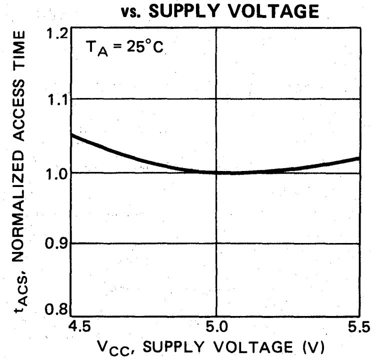


Fig. 5 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

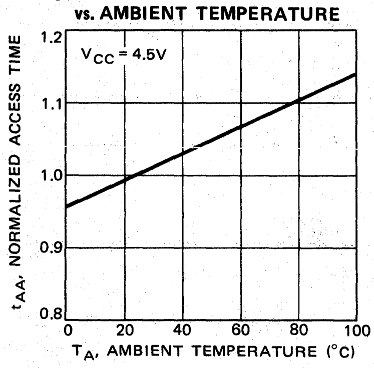


Fig. 6 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

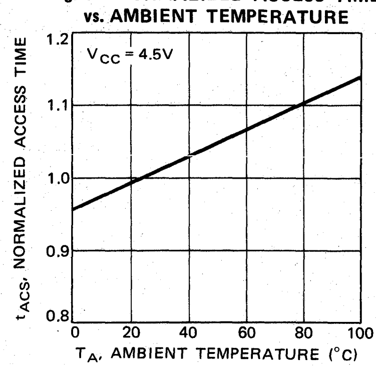


Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

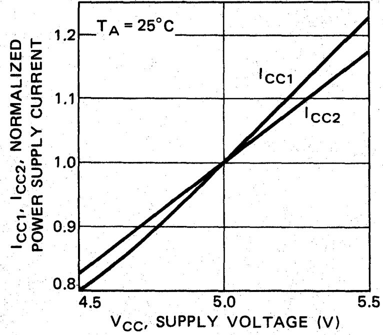


Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

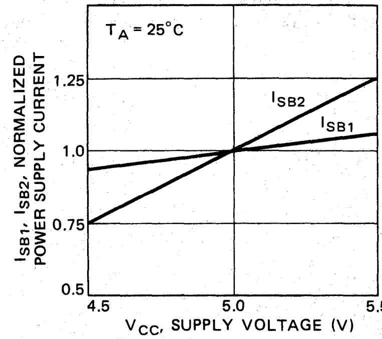


Fig. 9 — NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

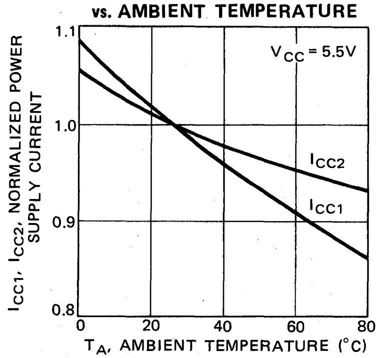


Fig. 10 — NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

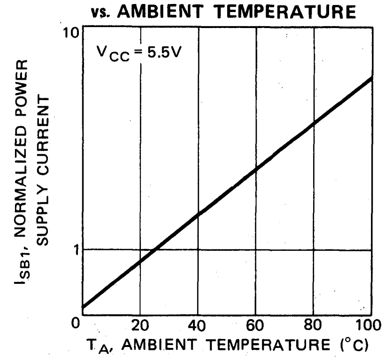


Fig. 11 — NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

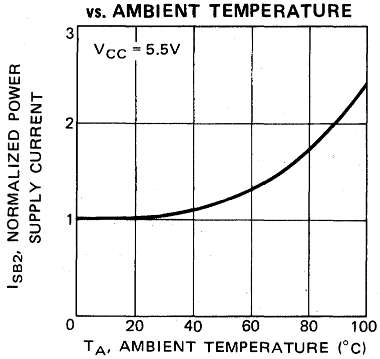


Fig. 12 — OUTPUT VOLTAGE vs. OUTPUT CURRENT

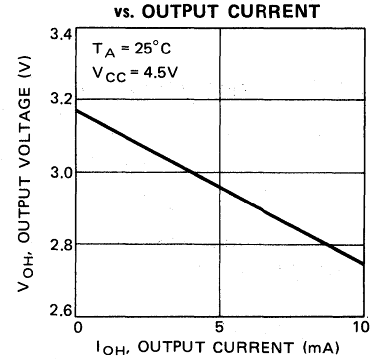


Fig. 13 — OUTPUT VOLTAGE vs. OUTPUT CURRENT

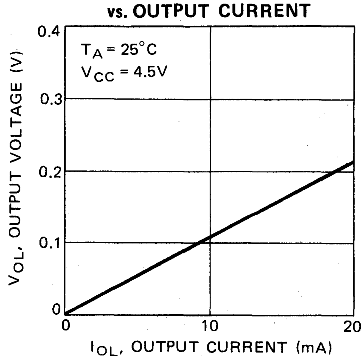


Fig. 14 — NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

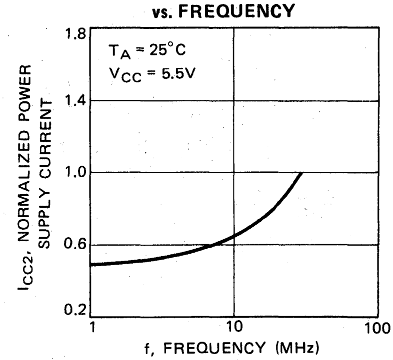


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Fig. 15 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

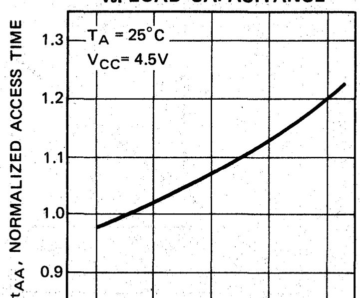
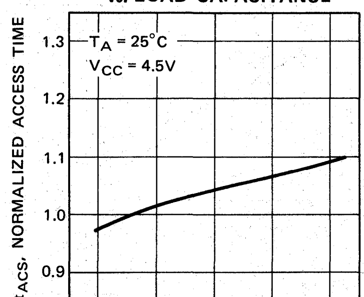


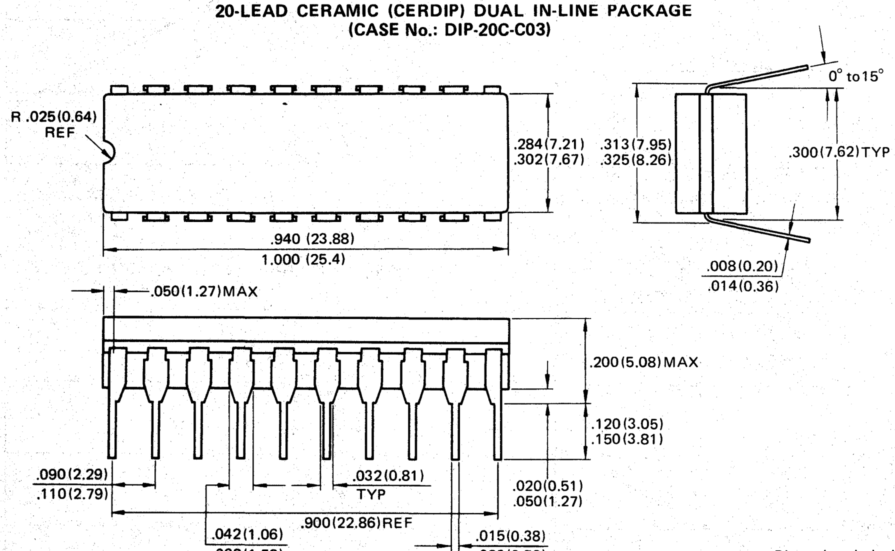
Fig. 16 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

(Suffix: CZ)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE (CASE No.: DIP-20C-C03)

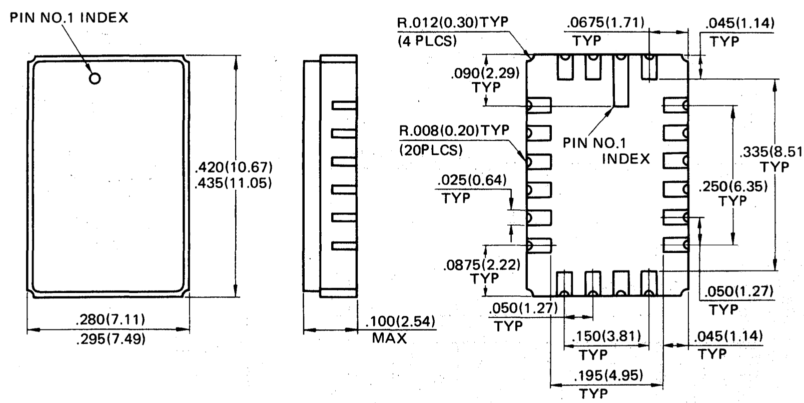


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: TV)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



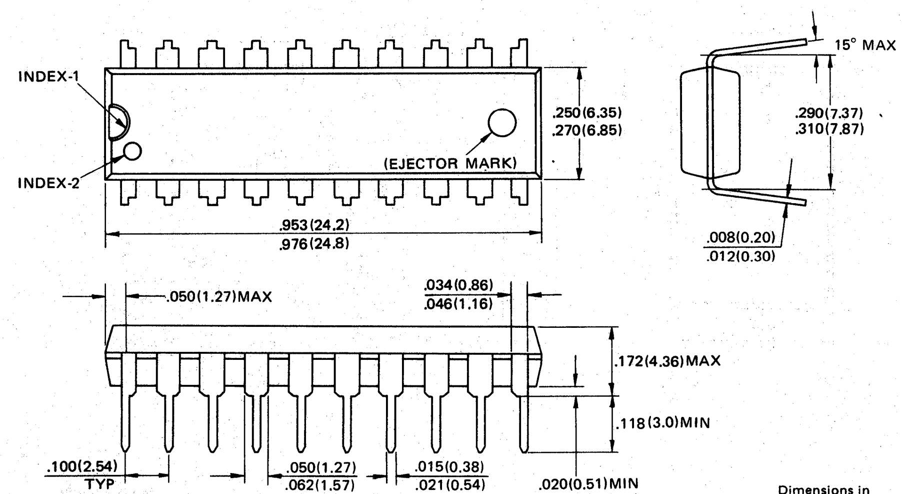
Dimension in
inches (millimeters)

5

PACKAGE DIMENSIONS

(Suffix: P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

CMOS 16384-BIT STATIC RANDOM ACCESS MEMORY

MB81C68A-25
MB81C68A-30
MB81C68A-35

January 1988
Edition 2.0

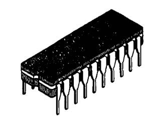
4K x 4 (16,384-BIT) STATIC RANDOM ACCESS MEMORY WITH SUPER HIGH SPEED AND AUTOMATIC POWER DOWN

The Fujitsu MB 81C68A is 4096 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and all pins are TTL compatible and a single 5 volts power supply is required.

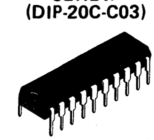
A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS}$, the other deselected packages automatically power down.

All devices offer the advantages of low power dissipation, low cost, and high performance.

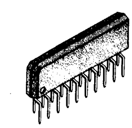
- Organization: 4096 words x 4 bits
- Static operation: No clocks or timing strobe required
- Fast access time: $t_{AA} = t_{ACS}$ = 25 ns max. (MB 81C68A-25)
  $t_{AA} = t_{ACS}$ = 30 ns max. (MB 81C68A-30)
  $t_{AA} = t_{ACS}$ = 35 ns max. (MB 81C68A-35)
- Low power consumption: 385 mW max. (Active)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 20-pin DIP (Suffix -P(plastic)/Suffix: -Z(cerdip))
- Standard 20-pad LCC (Suffix: -TV)
- Standard 20-pin ZIP (Suffix: -PSZ)



CERAMIC PACKAGE
CERDIP
(DIP-20C-C03)



PLASTIC PACKAGE
(DIP-20P-M01)



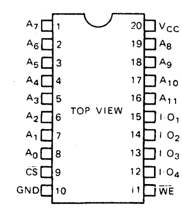
PLASTIC PACKAGE
(ZIP-20P-M01)

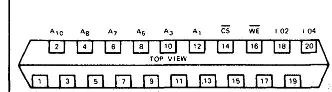
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7	V
Input Voltage on Any Pin with respect to GND		V_{IN}	-3.5 to +7	V
Output Voltage on Any I/O Pin with respect to GND		V_{OUT}	-0.5 to +7	V
Output current		I_{OUT}	±20	mA
Power dissipation		P_D	1.0	W
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	CERAMIC	T_{STG}	-65 to +150	°C
	PLASTIC		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

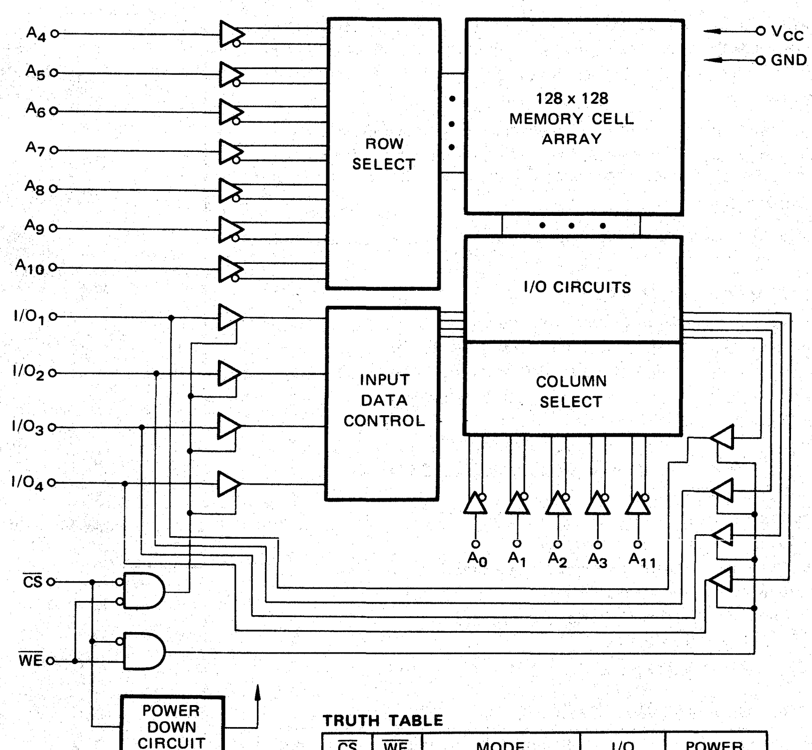
PIN ASSIGNMENT





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 81C68A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		6	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	$C_{I/O}$		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

Note: * –2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = –0.5V at DC level)

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DC CHARACTERISTICS

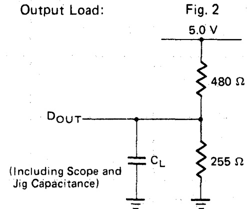
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	-10		10	µA
Output Leakage Current	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}	I_{LO}	-10		10	µA
Active (DC) Supply Current	I_{OUT} = 0 mA $\overline{CS}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH}	I_{CC1}		25	50	mA
Operating Supply Current	$\overline{CS}$ = V_{IL} I_{OUT} = 0 mA, Cycle = Min	I_{CC2}		40	70	mA
Standby Supply Current	$\overline{CS}$ = V_{CC} – 0.2V, $V_{IN} \leqq$ 0.2V or $V_{IN} \geqq V_{CC}$ – 0.2V	I_{SB1}		0.5	15	mA
Standby Supply Current	$\overline{CS}$ = V_{IH}	I_{SB2}		10	25	mA
Output Low Voltage	I_{OL} = 8 mA	V_{OL}			0.4	V
Output High Voltage	I_{OH} = -4 mA	V_{OH}	2.4			V

AC TEST CONDITION

Input Pulse Levels:	0 V to 3.0 V
Input Pulse Rise and Fall Times:	5 ns (Transient Time between 0.8 V and 2.2 V)
Timing Reference Levels:	Input : 1.5 V Output: 1.5 V

Output Load: Fig. 2



C_L = 30 pF
C_L = 5 pF for t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

AC CHARACTERISTICS

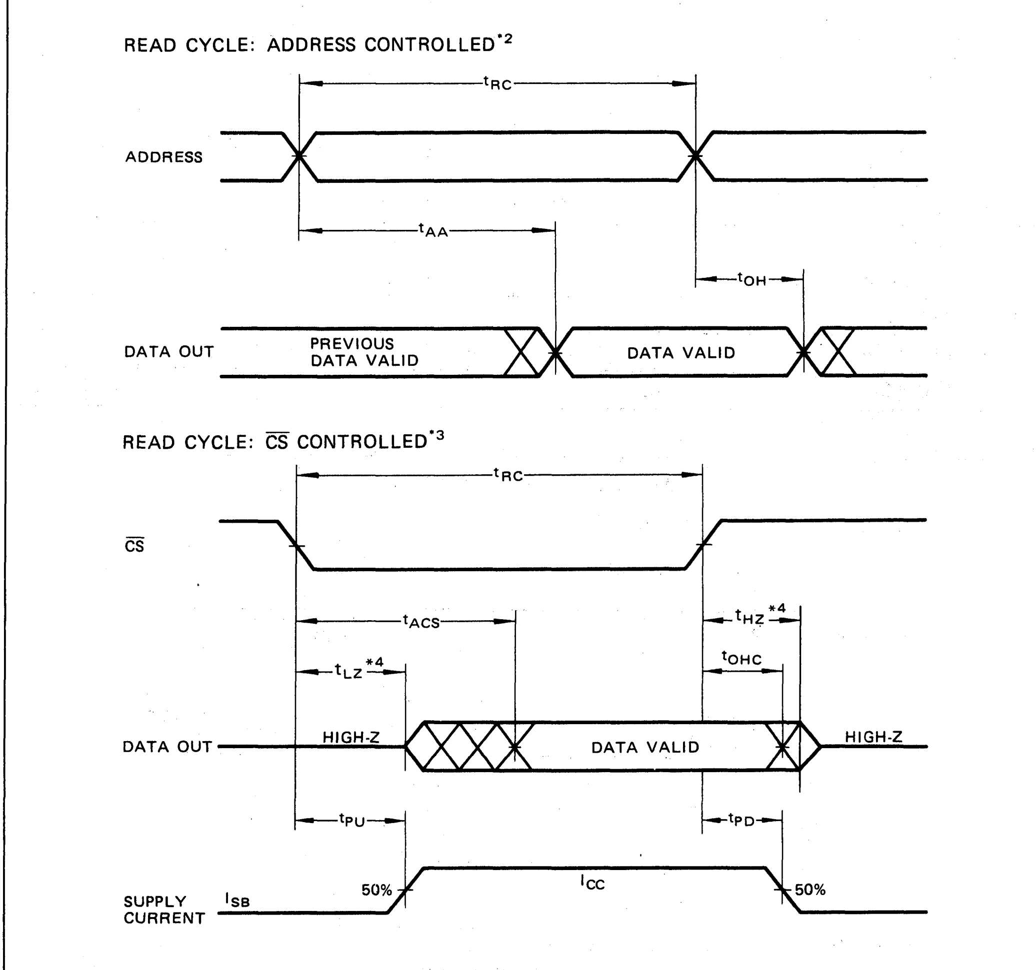
(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 81C68A-25		MB 81C68A-30		MB 81C68A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		30		35		ns
Address Access Time*2	t_{AA}		25		30		35	ns
Chip Select Access Time*3	t_{ACS}		25		30		35	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Output Hold from $\overline{CS}$	t_{OHC}	0		0		0		ns
Chip Selection to Output in Low-Z*4	t_{LZ}	5		5		5		ns
Chip Deselection to Output in High-Z*4	t_{HZ}		10		13		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		0		ns
Power Down from $\overline{CS}$	t_{PD}		20		25		30	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS} = V_{IL}$
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is specified at the point of ±500 mV from steady state voltage.

READ CYCLE TIMING DIAGRAM*1



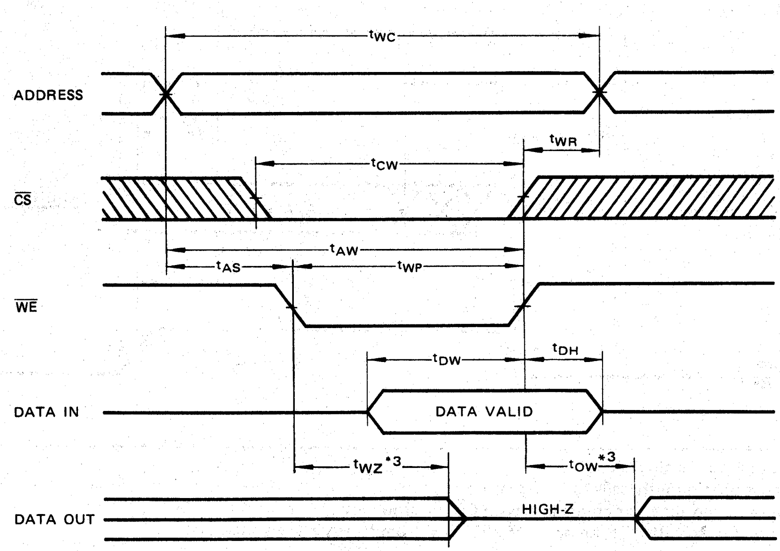
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS} = V_{IL}$
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is specified at the point of ±500 mV from steady state voltage.

WRITE CYCLE[*1*2]

Parameter	Symbol	MB 81C68A-25		MB 81C68A-30		MB 81C68A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		30		35		ns
Chip Selection to End of Write	t_{CW}	20		25		30		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Setup Time	t_{DW}	13		15		15		ns
Write Recovery Time	t_{WR}	2		2		2		ns
Data Hold Time	t_{DH}	0		0		0		ns
Output High-Z from $\overline{WE}$ *3	t_{WZ}		10		13		15	ns
Output Low-Z from $\overline{WE}$ *3	t_{OW}	5		5		5		ns

WRITE CYCLE TIMING DIAGRAM

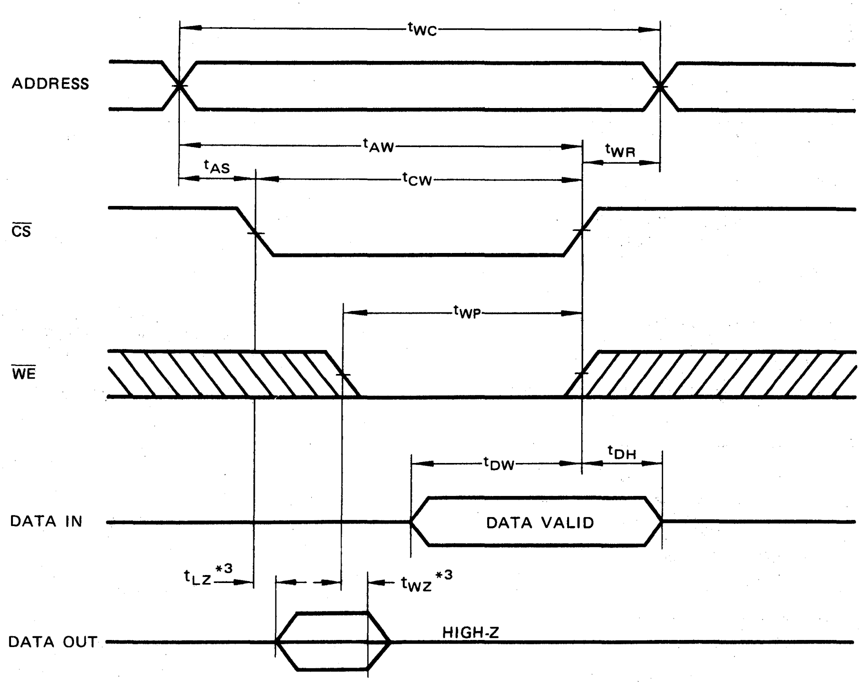
WRITE CYCLE: $\overline{WE}$ CONTROLLED[*1*2]



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
*3 Transition is specified at the point of ±500 mV from steady state voltage.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED*1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
*3 Transition is specified at the point of ±500 mV from steady state voltage.

5

TYPICAL CHARACTERISTICS CURVES

Fig. 3 OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

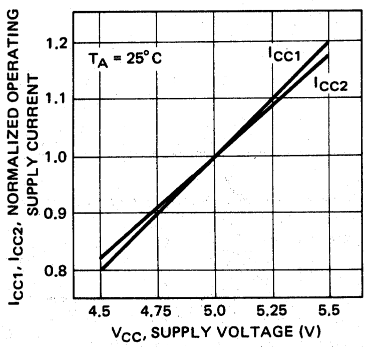


Fig. 4 OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

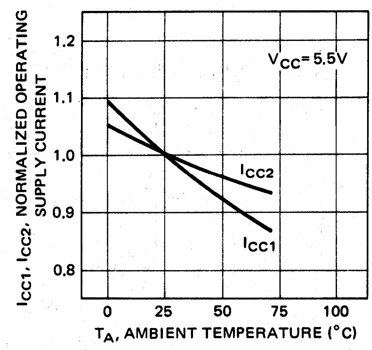


Fig. 5 STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

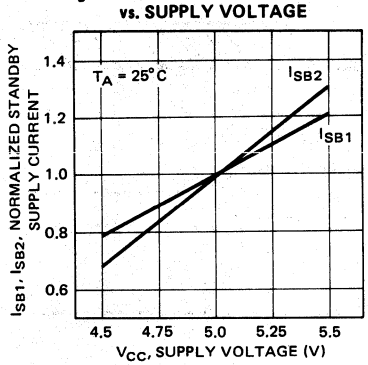


Fig. 6 STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

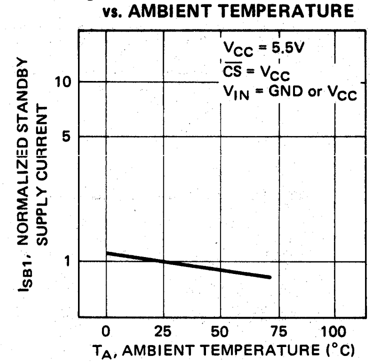


Fig. 7 STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

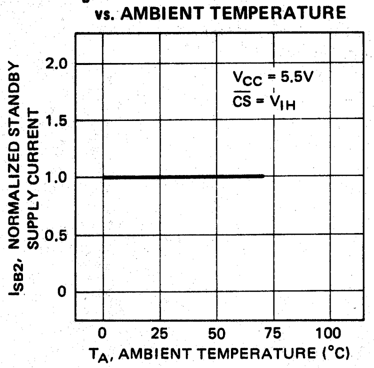
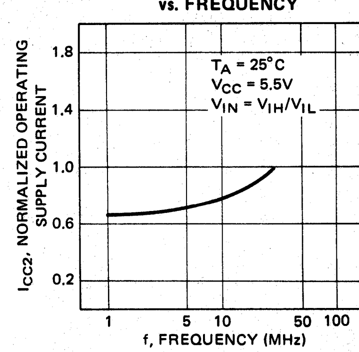


Fig. 8 OPERATING SUPPLY CURRENT vs. FREQUENCY



TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 9 "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

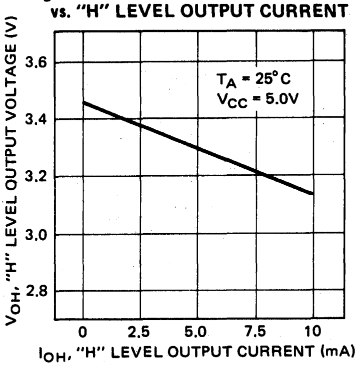


Fig. 10 "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

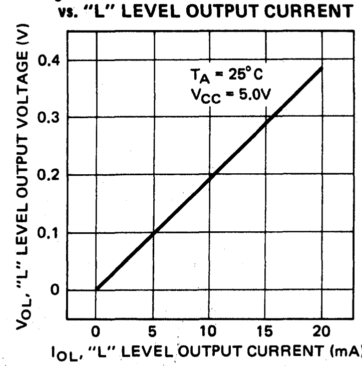


Fig. 11 ACCESS TIME vs. SUPPLY VOLTAGE

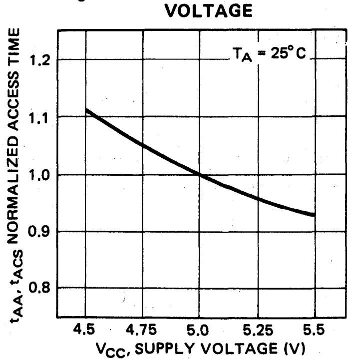


Fig. 12 ACCESS TIME vs. AMBIENT TEMPERATURE

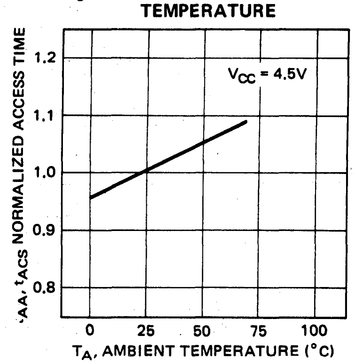
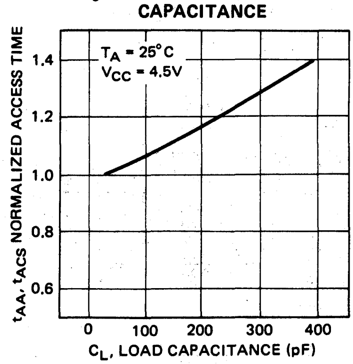


Fig. 13 ACCESS TIME vs. LOAD CAPACITANCE

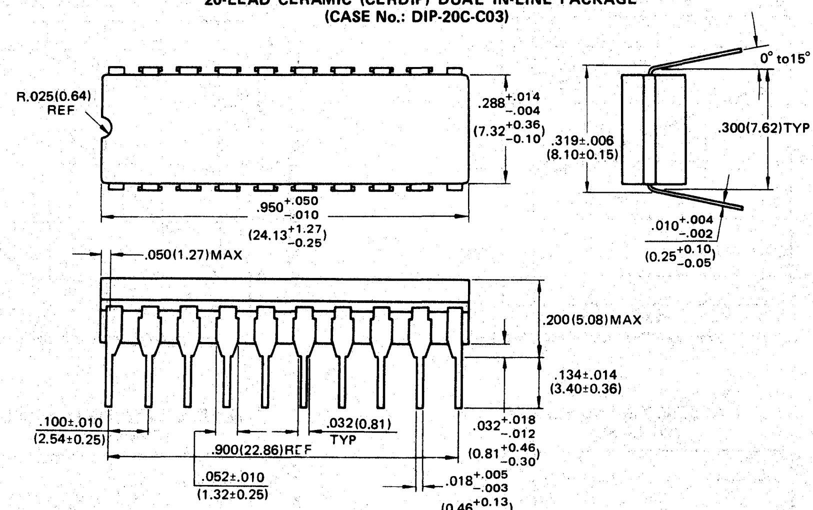


5

PACKAGE DIMENSIONS

(Suffix: -Z)

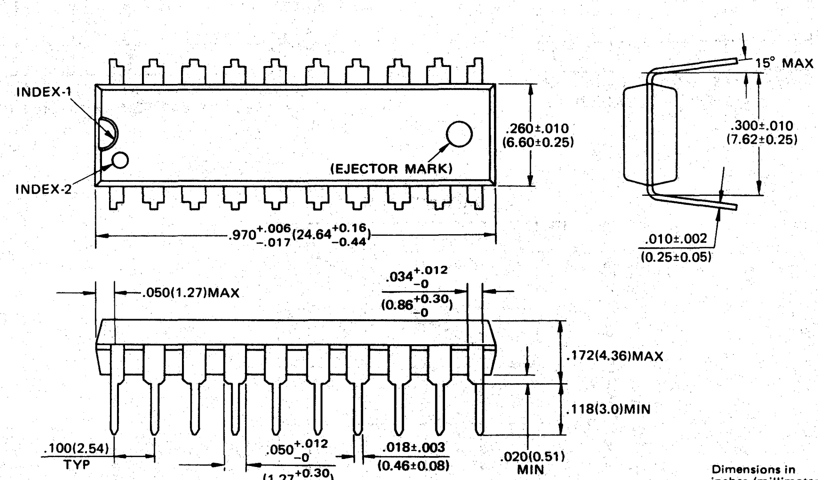
20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimensions in inches (millimeters)

(Suffix: -P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



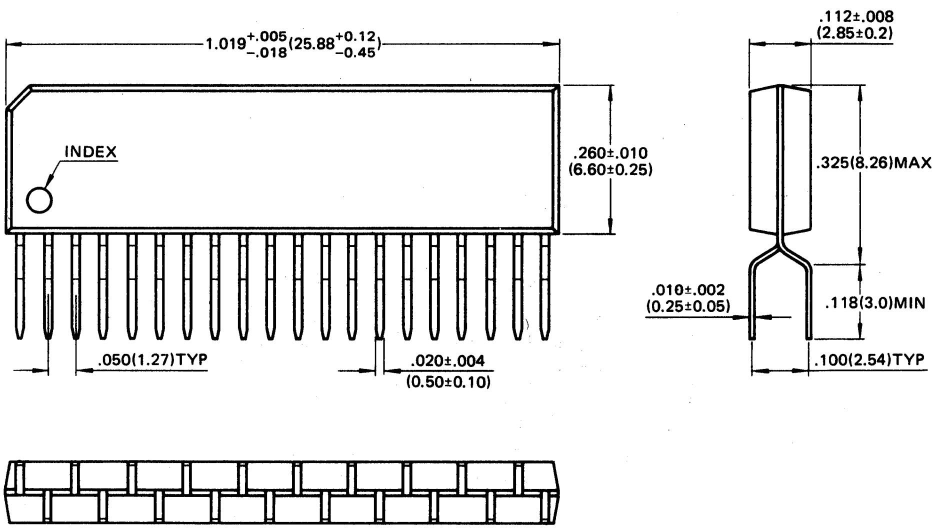
Dimensions in inches (millimeters)

5

PACKAGE DIMENSIONS

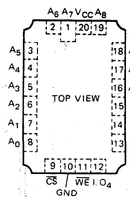
(Suffix: -PSZ)

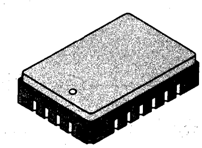
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE NO.: ZIP-20P-M01)



Dimensions in inches (millimeters)

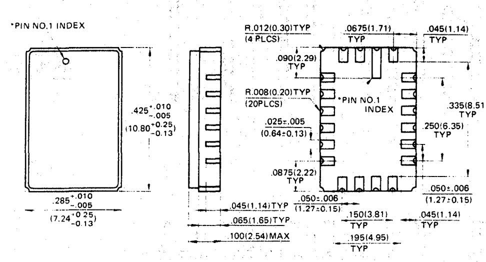
(Suffix: -TV)





CERAMIC PACKAGE
LCC
(LCC-20C-F01)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



* Shape of PIN NO. 1 INDEX: Subject to change without notice

Dimension in inches (millimeters)

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FUJITSU

CMOS 16384-BIT STATIC RANDOM ACCESS MEMORY

MB81C69A-25
MB81C69A-30
MB81C69A-35

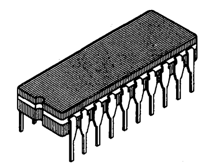
January 1988
Edition 2.0

4K x 4 (16,384-BIT) STATIC RANDOM ACCESS MEMORY WITH SUPPER HIGH SPEED

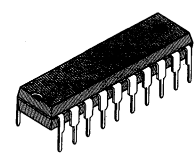
The Fujitsu MB 81C69A is 4096 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and all pins are TTL compatible and a single 5 volts power supply is required.

A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied.

All devices offer the advantages of low power dissipation, low cost, and high performance.



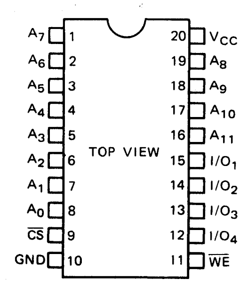
CERAMIC PACKAGE CERDIP (DIP-20C-C03)



PLASTIC PACKAGE (DIP-20P-M01)

- Organization: 4096 words x 4 bits
- Static operation: No clocks or timing strobe required
- Fast access time: t_{AA} = 25 ns max, t_{ACS} = 15 ns max (MB 81C69A-25)
  t_{AA} = 30 ns max, t_{ACS} = 18 ns max (MB 81C69A-30)
  t_{AA} = 35 ns max, t_{ACS} = 20 ns max (MB 81C69A-35)
- Low power consumption: 385 mW max. (Active)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion
- All inputs and outputs have protection against static charge
- Standard 20-pin DIP (Suffix: -P(plastic)/Suffix: -Z(cerdip))
- Standard 20-pad LCC (Suffix: -TV)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

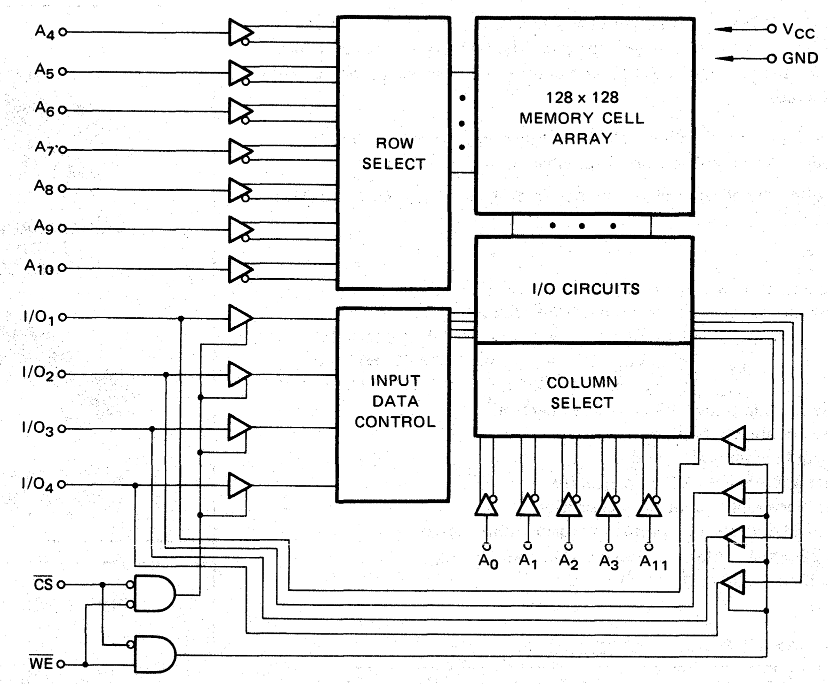
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	–0.5 to +7	V
Input Voltage on Any Pin with respect to GND		V_{IN}	–3.5 to +7	V
Output Volage on Any I/O Pin with respect to GND		V_{OUT}	–0.5 to +7	V
Output current		I_{OUT}	±20	mA
Power dissipation		P_D	1.0	W
Temperature under Bias		T_{BIAS}	–10 to +85	°C
Storage Temperature	CERAMIC	T_{STG}	–65 to +150	°C
	PLASTIC		–45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 – MB 81C69A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O
H	X	NOT SELECTED	HIGH-Z
L	L	WRITE	D_{IN}
L	H	READ	D_{OUT}

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		6	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	$C_{I/O}$		7	pF

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

Note: * –2.0 V Min. for pulse width less than 20 ns. (V_{IL} Min. = –0.5 V at DC level)

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

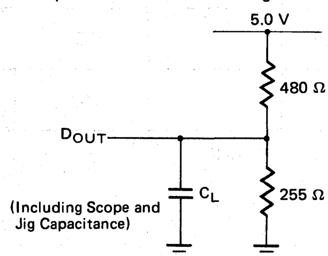
Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}	-10		10	µA
Output Leakage Current	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}	I_{LO}	-10		10	µA
Active Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA V_{IN} = V_{IL} or V_{IH}	I_{CC1}		25	50	mA
Operating Supply Current	$\overline{CS}$ = V_{IL} I_{OUT} = 0 mA, Cycle = Min	I_{CC2}		40	70	mA
Output Low Voltage	I_{OL} = 8 mA	V_{OL}			0.4	V
Output High Voltage	I_{OH} = -4 mA	V_{OH}	2.4			V

5

AC TEST CONDITION

Input Pulse Levels: 0 V to 3.0 V
Input Pulse Rise and Fall Times: 5 ns (Transient Time between 0.8 V and 2.2 V)
Timing Reference Levels: Input : 1.5 V
Output: 1.5 V

Output Load: Fig. 2



C_L = 30 pF
C_L = 5 pF for t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

AC CHARACTERISTICS

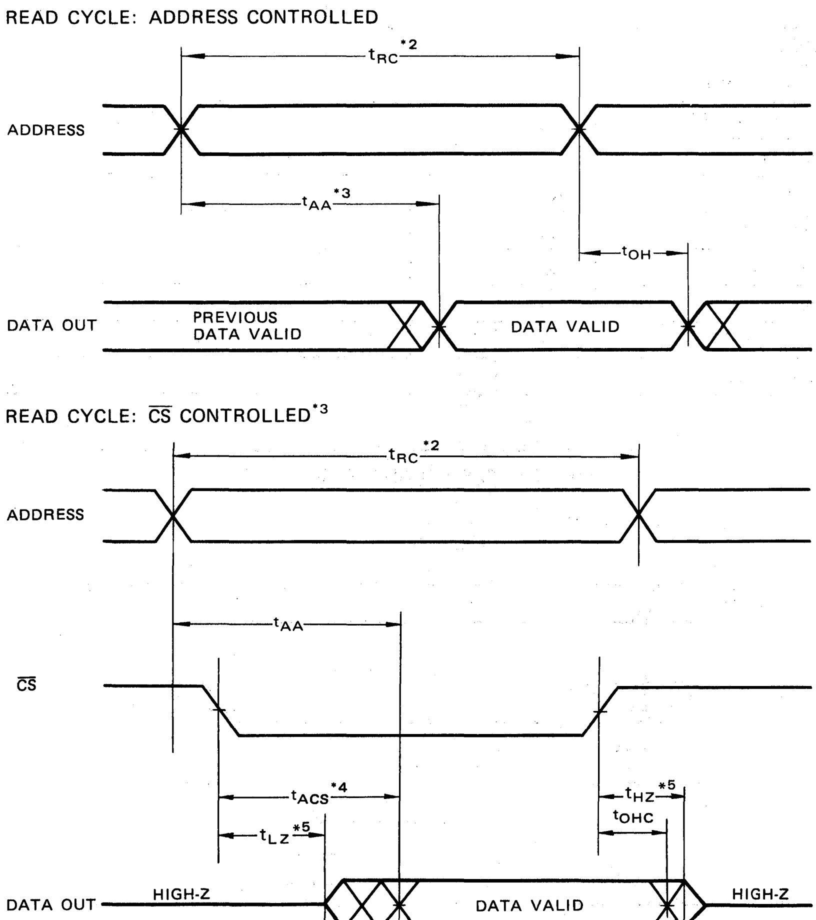
(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 81C69A-25		MB 81C69A-30		MB 81C69A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	25		30		35		ns
Address Access Time*3	t_{AA}		25		30		35	ns
Chip Select Access Time*4	t_{ACS}		15		18		20	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Output Hold from $\overline{CS}$	t_{OHC}	0		0		0		ns
Chip Selection to Output in Low-Z*5	t_{LZ}	0		0		0		ns
Chip Deselection to Output in High-Z*5	t_{HZ}		10		13		15	ns

Note: *1 $\overline{WE}$ is high for Raed cycle.
*2 All read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified at the point of ±500mV from steady state Voltage with Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM*1



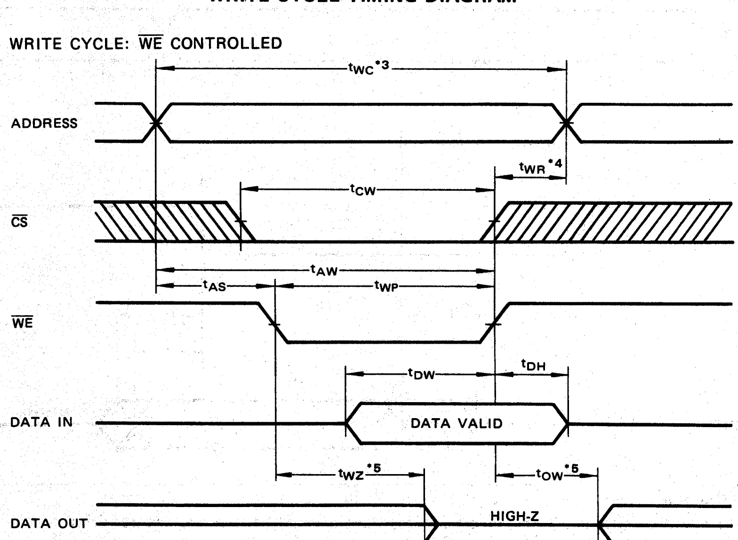
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified at the point of ±500 mV from steady state voltage with Lead II in Fig. 2.

5

WRITE CYCLE *1*2

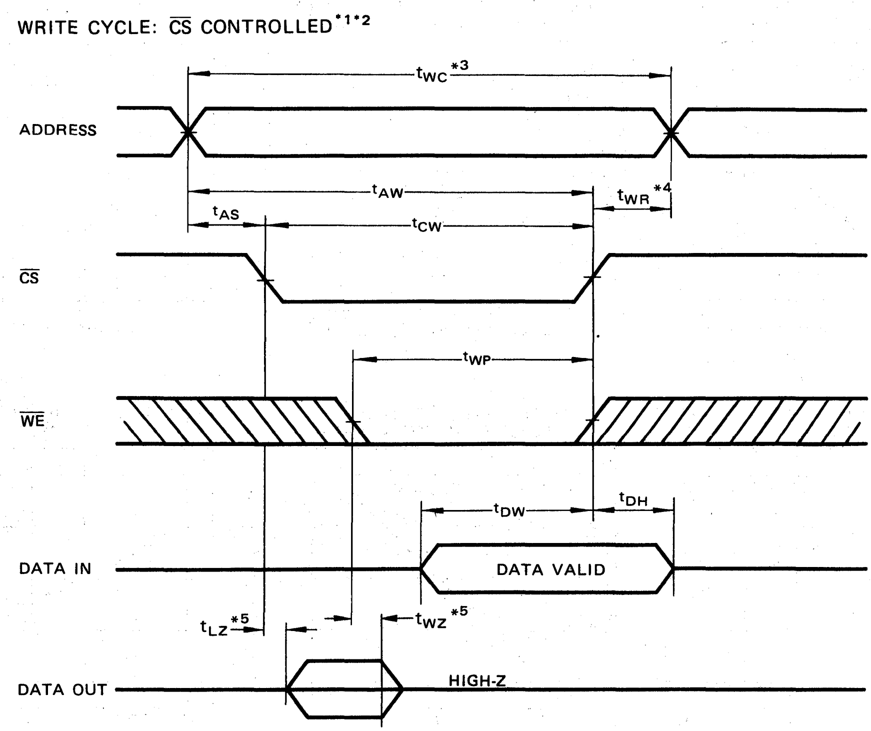
Parameter	Symbol	MB 81C69A-25		MB 81C69A-30		MB 81C69A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	25		30		35		ns
Chip Selection to End of Write	t_{CW}	20		25		30		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Setup Time	t_{DW}	13		15		15		ns
Write Recovery Time *4	t_{WR}	2		2		2		ns
Data Hold Time	t_{DH}	0		0		0		ns
Output High-Z from $\overline{WE}$*5	t_{WZ}		10		13		15	ns
Output Low-Z from $\overline{WE}$*5	t_{OW}	5		5		5		ns

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 If $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simulatneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified at the point of ±500mV from steady state voltage, with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified at the point of ±500mV from steady state voltage with Load II in Fig. 2.

5

TYPICAL CHARACTERISTICS CURVES

Fig. 3 OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

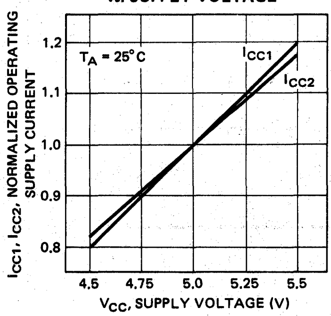


Fig. 4 OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

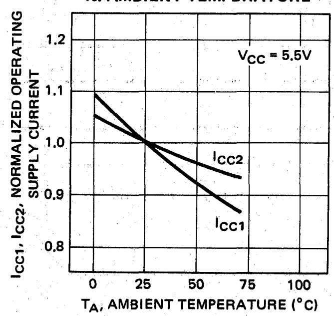


Fig. 5 OPERATING SUPPLY CURRENT vs. FREQUENCY

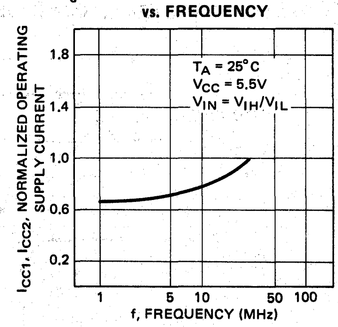


Fig. 6 "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

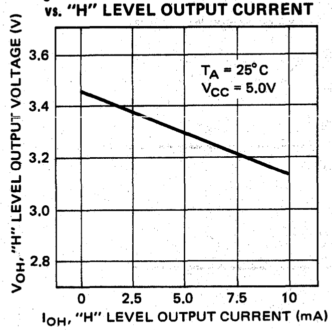


Fig. 7 "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

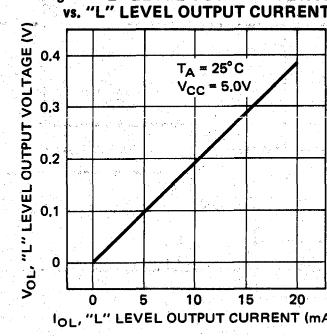


Fig. 8 ACCESS TIME vs. SUPPLY VOLTAGE

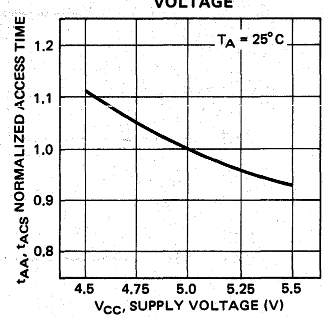


Fig. 9 ACCESS TIME vs. AMBIENT TEMPERATURE

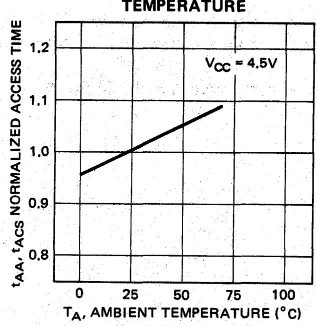
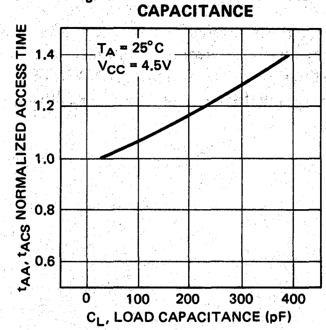
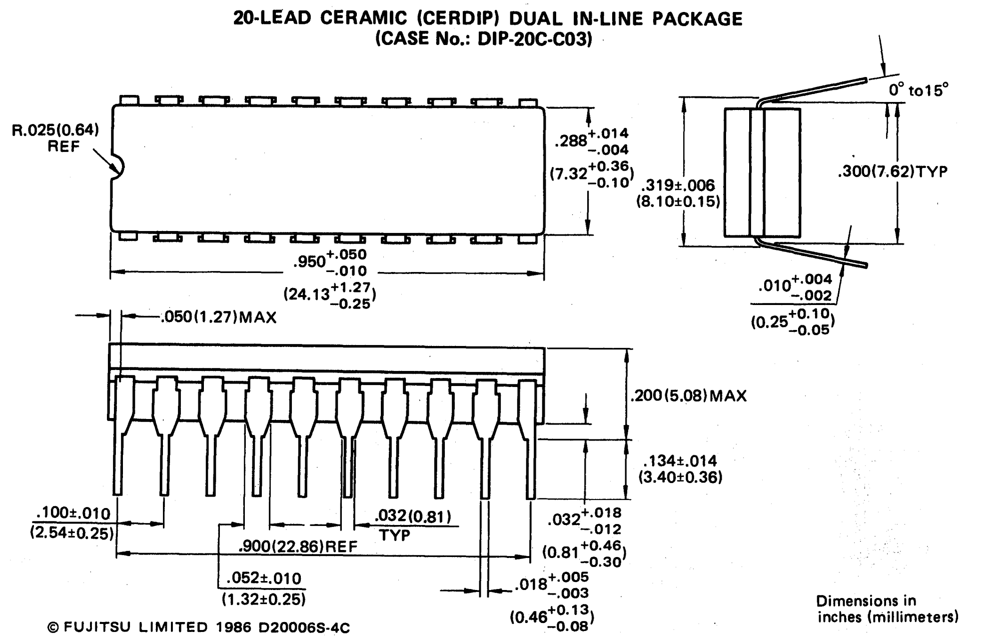


Fig. 10 ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

CERAMIC DIP (Suffix: -Z)



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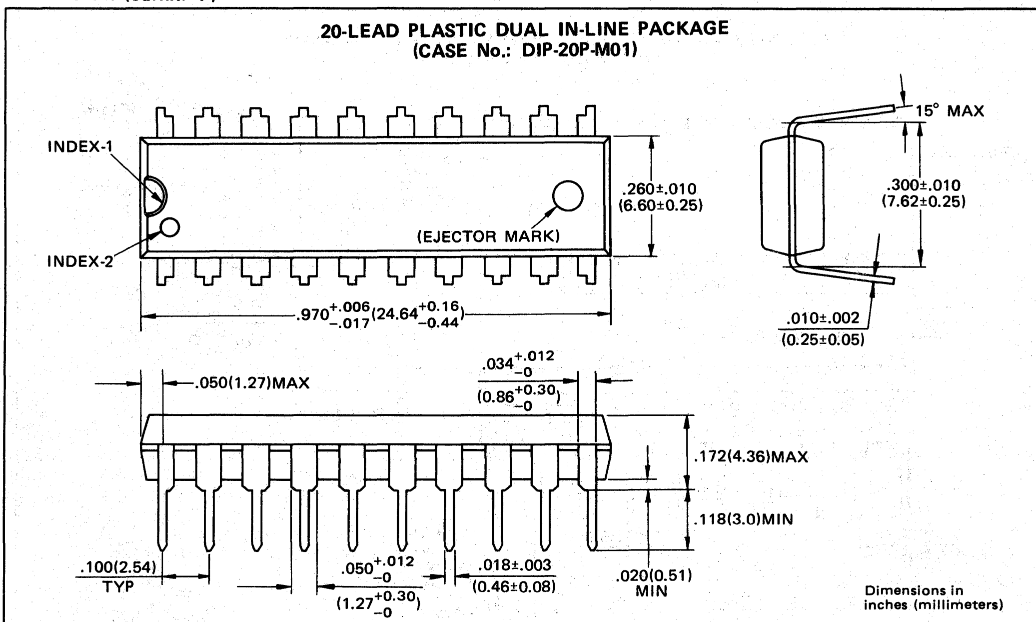
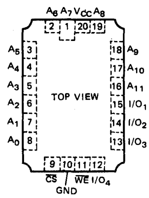
PACKAGE DIMENSIONS

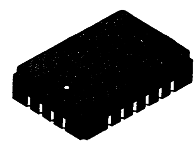
PLASTIC DIP (Suffix: -P)



PACKAGE DIMENSIONS

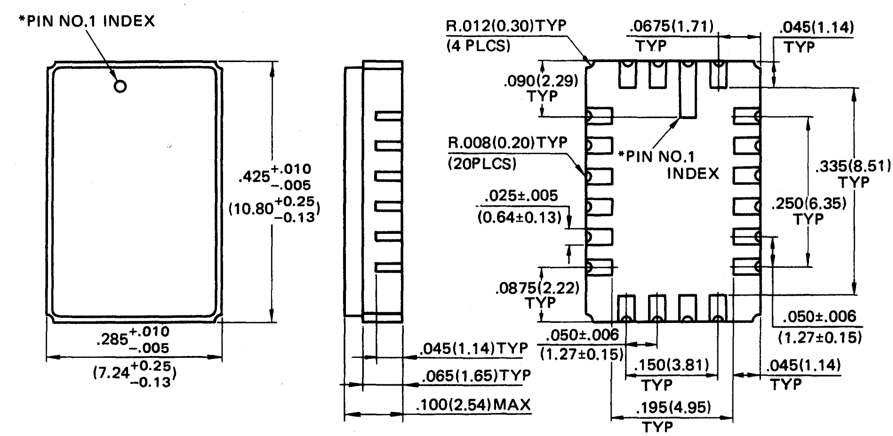
CERAMIC LCC (Suffix: -TV)





CERAMIC PACKAGE
(LCC-20C-F01)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



Dimension in inches (millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

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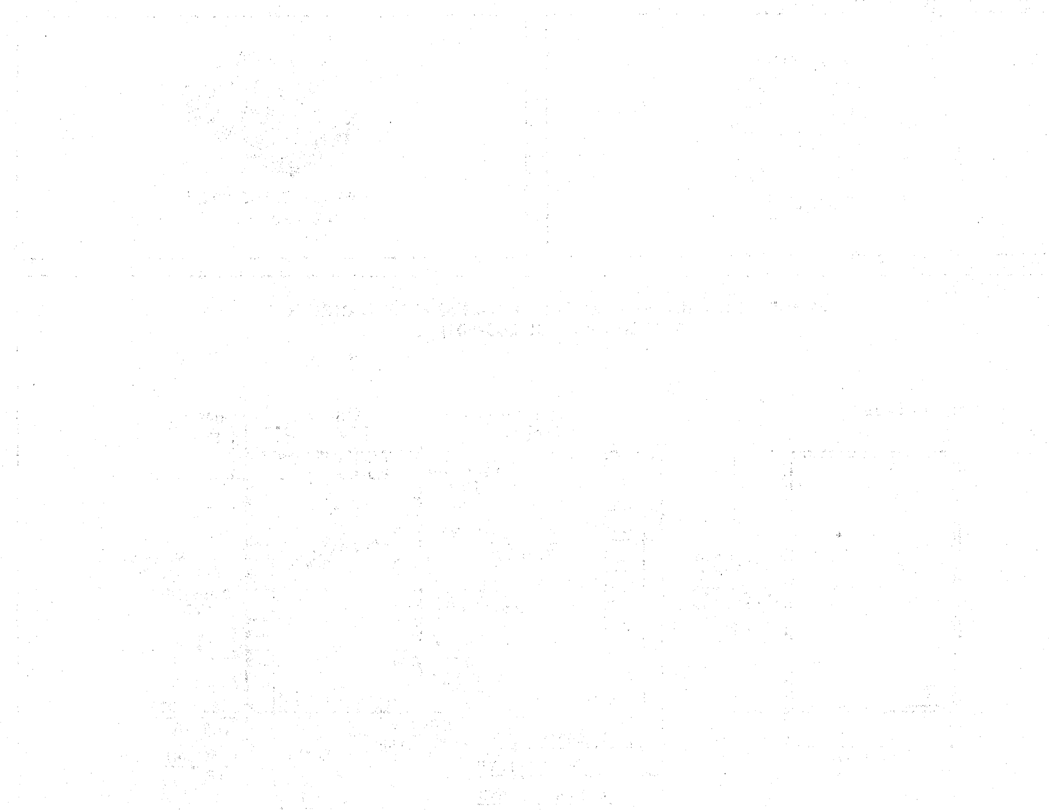


FUJITSU

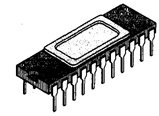
CMOS 65536-BIT STATIC RANDOM ACCESS MEMORY

MB 81C71-45
MB 81C71-55

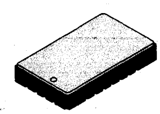
August 1986
Edition 2.0

65,536 WORDS X 1 BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY

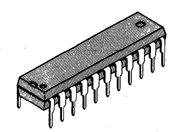
The Fujitsu MB 81C71 is 65,536 words x 1 bit static random access memory fabricated with a CMOS technology.
It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.
The MB 81C71 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.
MB 81C71 is compatible with TTL logic families in all respects; input, output and a single +5 V supply.



CERAMIC PACKAGE
DIP-22C-A02



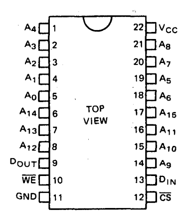
CERAMIC PACKAGE
LCC-22C-A01

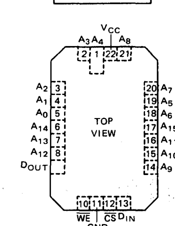


PLASTIC PACKAGE
DIP-22P-M04

- Organization : 65,536 words x 1 bit
- Static operation : No clocks or refresh required
- Fast access time : 45 ns max. (MB 81C71-45)
  55 ns max. (MB 81C71-55)
- Single +5 V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- Standard 300mil width 22-pin Dual In-Line package (Suffix:C) (Suffix:P)
- Standard 22-pad LCC (Suffix:CV)

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	-3.5 to +7	V
Output Voltage on any pin with respect to GND		V_{OUT}	-0.5 to +7	V
Output Current		I_{OUT}	±50	mA
Power Dissipation		P_D	1.0	W
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMAM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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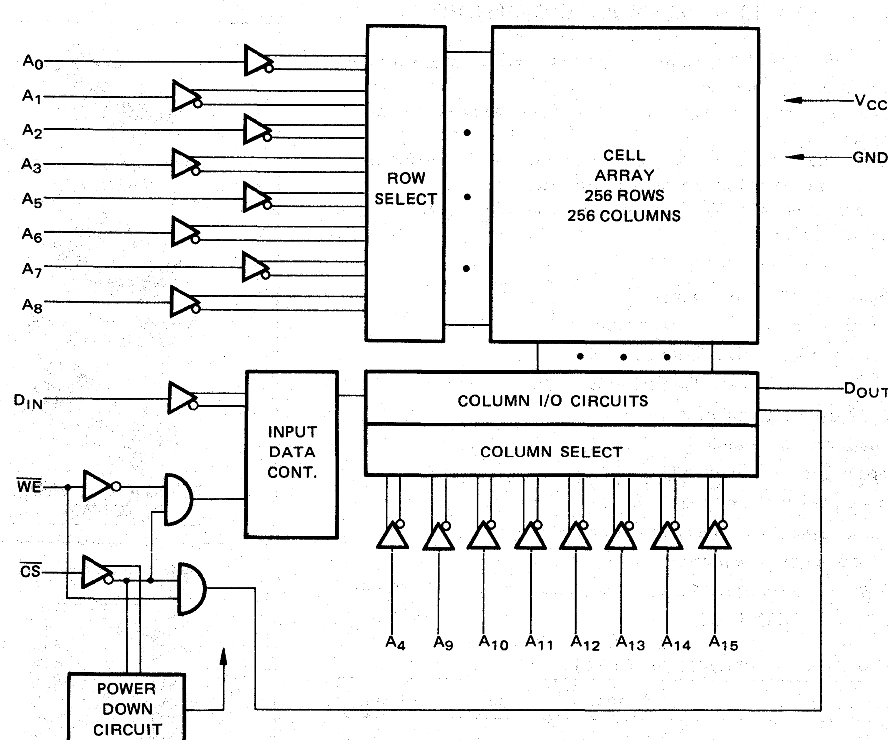
Fig. 1 — MB 81C71 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0V)	$C_{\overline{CS}}$		8	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.5*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -3.0V Min, for pulse width less than 20ns. (V_{IL} Min = -0.5V at DC Level)

DC CHARACTERISTICS

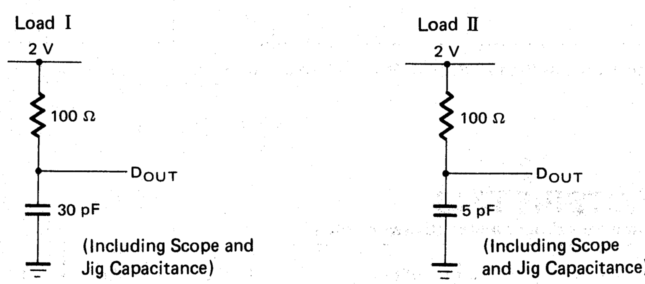
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0V to V_{CC} V_{CC} = Max.	I_{LI}	–10	0.01	10	μA
Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to 4.5V V_{CC} = Max.	I_{LO}	–50	0.1	50	μA
Operating Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max. I_{OUT} = 0 mA Cycle = Min.	I_{CC}		50	80	mA
Standby Current	V_{CC} = Min. to Max. $\overline{CS}$ = V_{CC} –0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} –0.2V	I_{SB1}		2	15	mA
Standby Current	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}	I_{SB2}		12	25	mA
Output Low Voltage	I_{OL} = 16 mA	V_{OL}			0.45	V
Output High Voltage	I_{OH} = –4 mA	V_{OH}	2.4			V
Peak Power on Current	V_{CC} = 0V to V_{CC} Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.	I_{PO}			30	mA

AC TEST CONDITIONS

Input Pulse Levels:	0.6 V to 2.4 V
Input Pulse Rise And Fall Times:	5 ns
Timing Measurement Reference Levels:	Input : 1.5 V
	Output: 1.5 V

OUTPUT LOAD: **Fig. 2**



(For t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

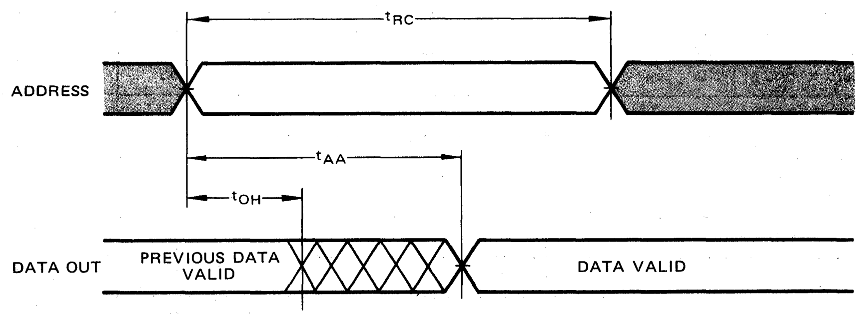
READ CYCLE *1

Parameter	Symbol	MB 81C71-45		MB 81C71-55		Unit
		Min	Max	Min	Max	
Read Cycle Time *2	t_{RC}	45		55		ns
Address Access Time *3	t_{AA}		45		55	ns
Chip Select Access Time *4 *5	t_{ACS}		45		55	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Chip Selection to Output in Low-Z *6 *7	t_{LZ}	5		5		ns
Chip Deselection to Output in High-Z *6 *7	t_{HZ}	0	25	0	30	ns
Chip Selection to Power Up Time	t_{PU}	0		0		ns
Chip Deselection to Power Down Time	t_{PD}		35		40	ns

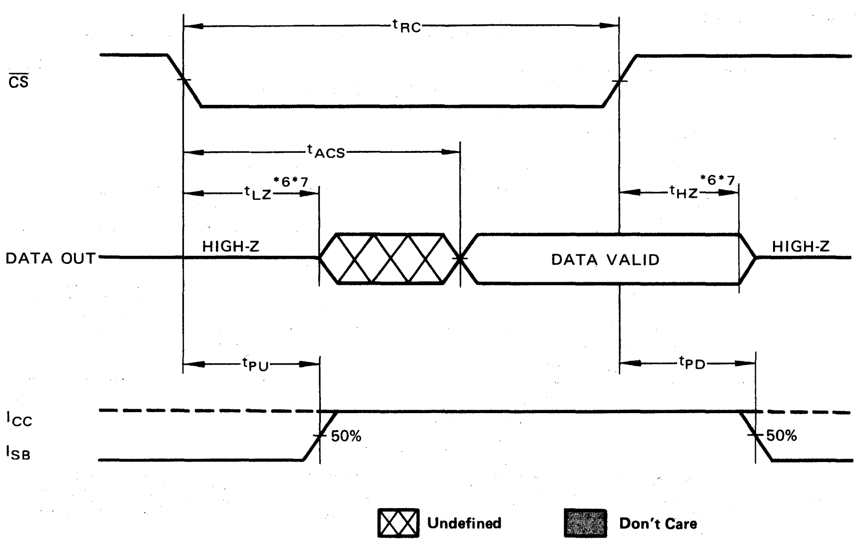
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage.
*7 This parameter is measured with specified loading Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM*1*2

READ CYCLE: ADDRESS CONTROLLED*3



READ CYCLE: $\overline{CS}$ CONTROLLED*4*5



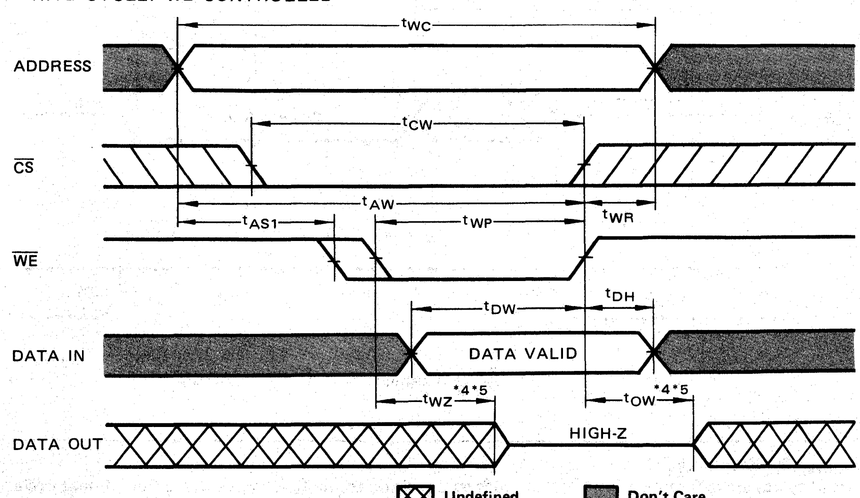
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage.
*7 This paramater is measured with specified loading Load II in Fig. 2.

WRITE CYCLE *1*2

Parameter	Symbol	MB 81C71-45		MB 81C71-55		Unit
		Min	Max	Min	Max	
Write Cycle Time *3	t_{WC}	45		55		ns
Chip Selection to End of Write	t_{CW}	40		50		ns
Address Valid to End of Write	t_{AW}	40		50		ns
Address Setup Time	t_{AS1}	5		5		ns
Address Setup Time	t_{AS2}	0		0		ns
Write Pulse Width	t_{WP}	30		35		ns
Data Valid to End of Write	t_{DW}	25		30		ns
Write Recovery Time	t_{WR}	5		5		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *4*5	t_{WZ}	0	25	0	30	ns
Output Active from End of Write *4*5	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM *1*2

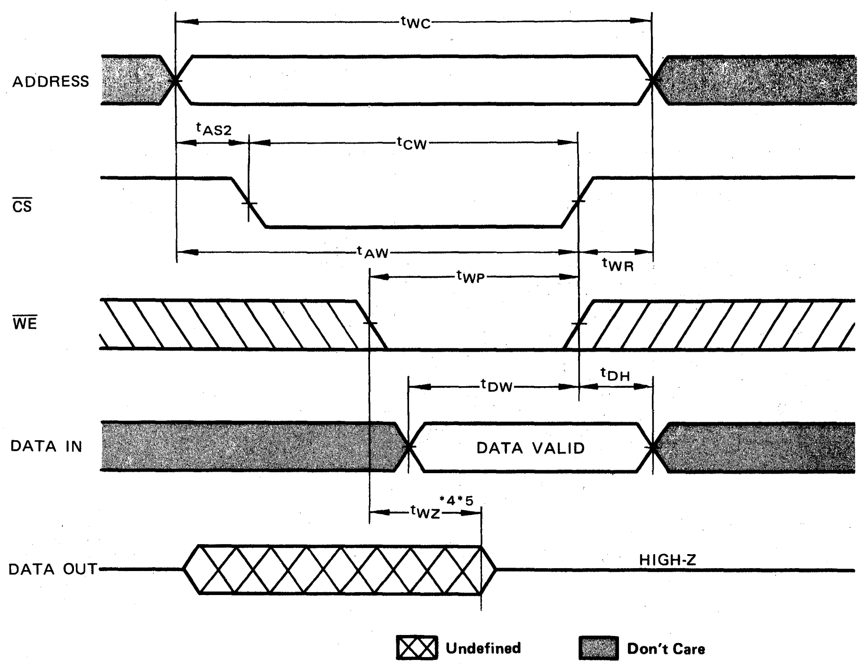
WRITE CYCLE: $\overline{WE}$ CONTROLLED *3



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified loading II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM*1*2

WRITE CYCLE: $\overline{CS}$ CONTROLLED*3



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified loading II in Fig. 2.

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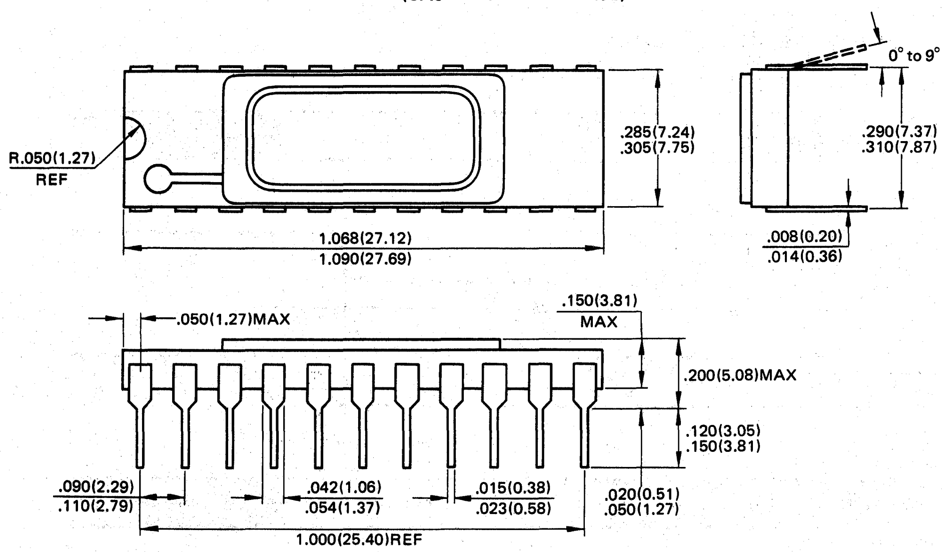
PACKAGE DIMENSIONS

(Suffix: -C)

22-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-22C-A02)

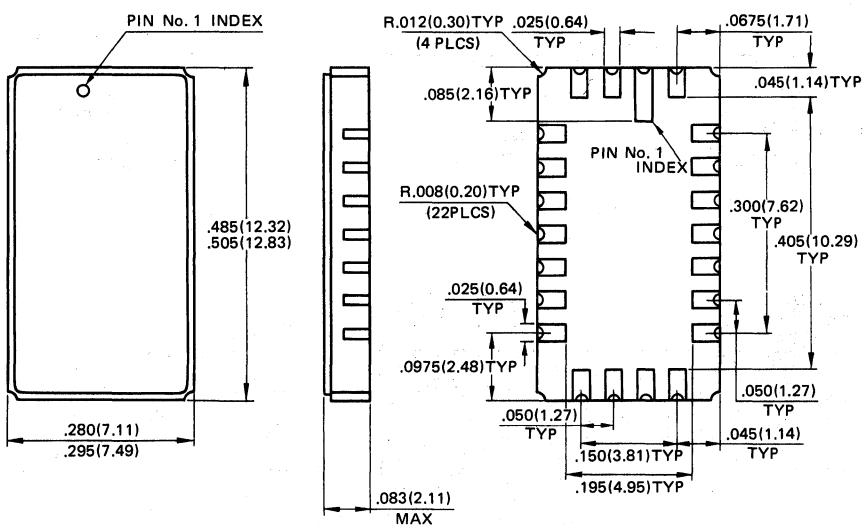


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -CV)

22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



Dimensions in inches (millimeters)

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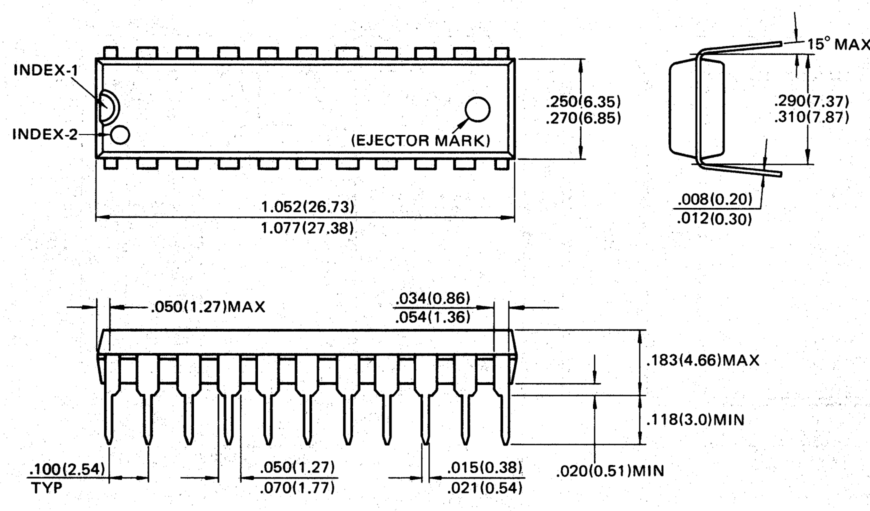
PACKAGE DIMENSIONS

(Suffix: -P)

22-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-22P-M04)



Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

CMOS 65,536-BIT STATIC RANDOM ACCESS MEMORY

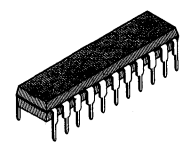
MB81C71A-25
MB81C71A-35

February 1988
Edition 2.0

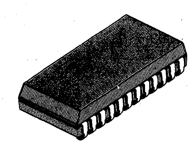
65,536 WORDS X 1 BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY

The Fujitsu MB 81C71A is 65,536 words x 1 bit static random access memory fabricated with a CMOS technology.
It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.
The MB 81C71A is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.
MB 81C71A is compatible with TTL logic families in all respects; input, output and a single +5 V supply.

- Organization : 65,536 words x 1 bit
- Static operation : No clocks or refresh required
- Fast access time : $t_{AA} = t_{ACS}$ = 25 ns (MB 81C71A-25)
  $t_{AA} = t_{ACS}$ = 35 ns (MB 81C71A-35)
- Single +5 V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- Standard 22-pin DIP (300 mil) (Suffix: P)
- Standard 22-pad LCC (Suffix: CV)
- Standard 24-pin SOJ (300 mil) : (Suffix : PJ)

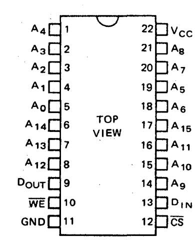


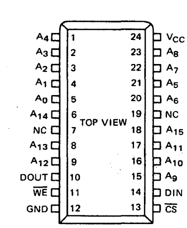
PLASTIC PACKAGE
DIP-22P-M04



PLASTIC PACKAGE
LCC-24P-M01

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	-3.5 to +7	V
Output Voltage on any pin with respect to GND		V_{OUT}	-0.5 to +7	V
Output Current		I_{OUT}	±50	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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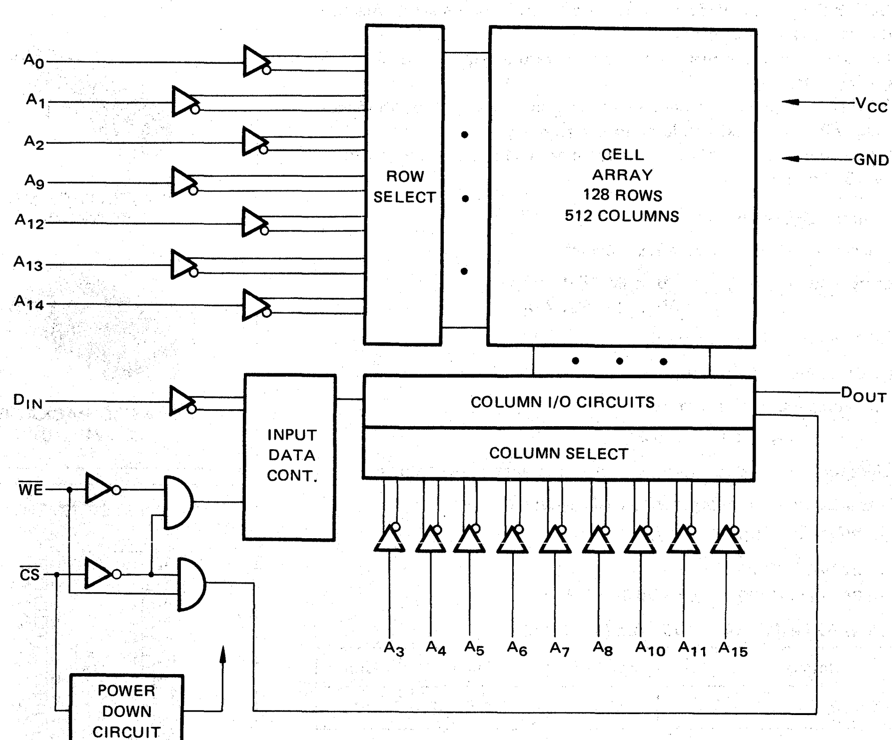
Fig. 1— MB 81C71A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance (V_{IN} = 0 V)	C_{IN}		7	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -2.0 V Min, for pulse width less than 20 ns. (V_{IL} Min = -0.5 V at DC Level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Leakage Current	V_{IN} = 0 V to V_{CC} V_{CC} = Max.	I_{LI}	-10		10	μA
Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0 V to 4.5 V V_{CC} = Max.	I_{LO}	-10		10	μA
Operating Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max. D_{OUT} = Open, Cycle = Min.	I_{CC}			80	mA
Standby Current	V_{CC} = Min. to Max. $\overline{CS} \geqq V_{CC}$ -0.2 V $V_{IN} \leqq$ 0.2 V or $V_{IN} \geqq V_{CC}$ -0.2 V	I_{SB1}			10	mA
Standby Current	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}	I_{SB2}			20	mA
Output Low Voltage	I_{OL} = 16 mA	V_{OL}			0.45	V
Output High Voltage	I_{OH} = -4 mA	V_{OH}	2.4			V
Peak Power on Current	V_{CC} = 0 V to V_{CC} Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.	I_{PO}			30	mA

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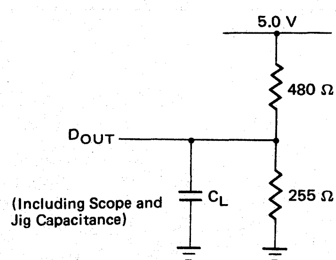
Fig. 2 — AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise And Fall Times: 5 ns
- Timing Measurement Reference Levels: Input : 1.5 V
  Output: 1.5 V
- Output Load:



Load I: C_L = 30 pF
Load II: C_L = 5 pF for t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 81C71A-25		MB 81C71A-35		Unit
		Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	25		35		ns
Address Access Time*3	t_{AA}		25		35	ns
Chip Select Access Time*4 *5	t_{ACS}		25		35	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Chip Selection to Output in Low-Z*6 *7	t_{LZ}	5		5		ns
Chip Deselection to Output in High-Z*6 *7	t_{HZ}	0	10	0	15	ns
Chip Selection to Power Up Time	t_{PU}	0		0		ns
Chip Deselction to Power Down time	t_{PD}		20		30	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$ = V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage.
*7 This parameter is measured with specified loading Load II in Fig. 2.

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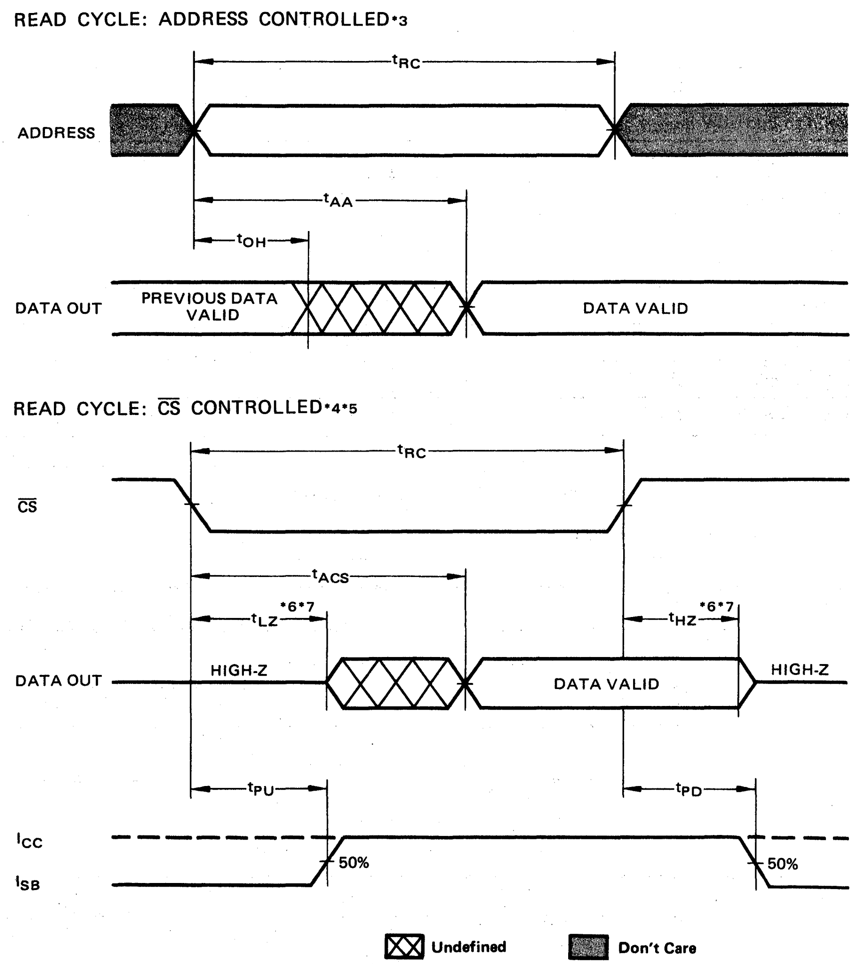
READ CYCLE TIMING DIAGRAM*1*2



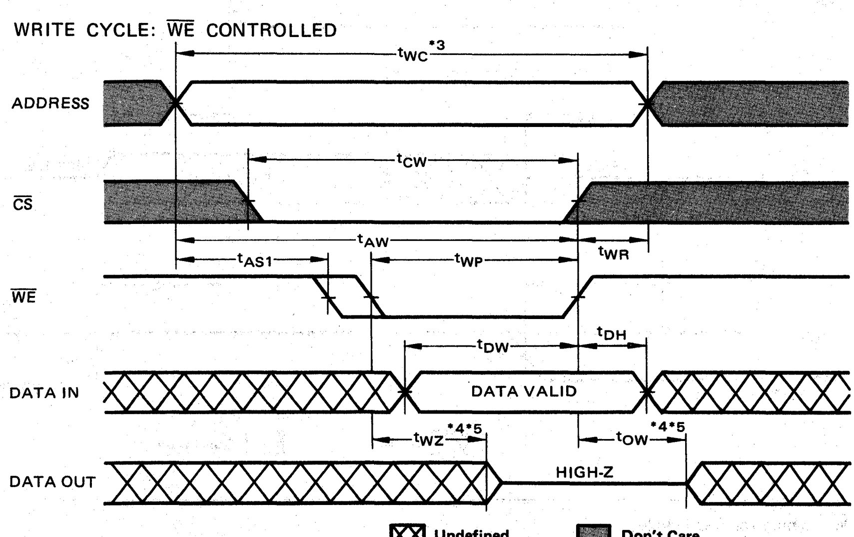
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage.
*7 This parameter is measured with specified loading Load II in Fig. 2.

5

WRITE CYCLE*1*2

Parameter	Symbol	MB 81C71A-25		MB 81C71A-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	25		35		ns
Chip Selection to End of Write	t_{CW}	20		30		ns
Address Valid to End of Write	t_{AW}	20		30		ns
Address Setup Time	t_{AS1}	0		0		ns
Address Setup Time	t_{AS2}	0		0		ns
Write Pulse Width	t_{WP}	20		30		ns
Data Valid to End of Write	t_{DW}	15		20		ns
Write Recovery Time	t_{WR}	2		2		ns
Data Hold Time	t_{DH}	2		2		ns
Write Enable to Output in High-Z*4*5	t_{WZ}	0	10	0	15	ns
Output Active from End of Write*4*5	t_{OW}	0		0		ns

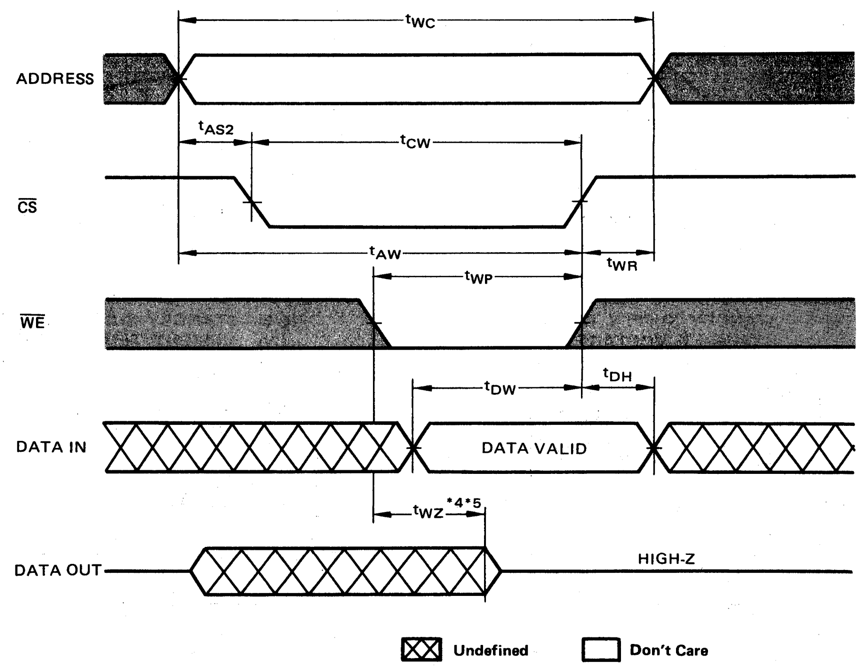
WRITE CYCLE TIMING DIAGRAM*1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1*2

WRITE CYCLE: $\overline{CS}$ CONTROLLED *3



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

5

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

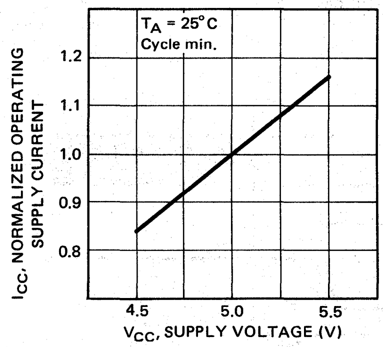


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

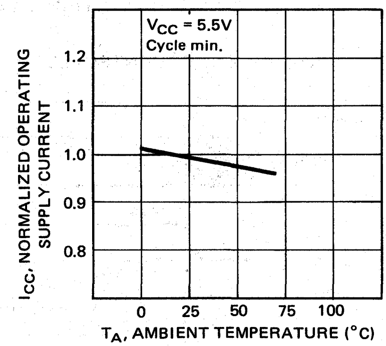


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

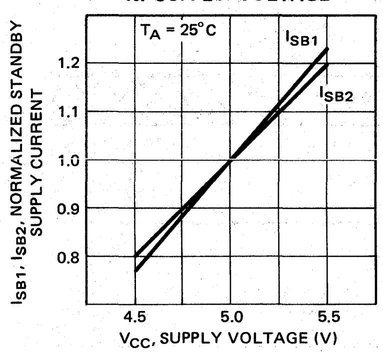


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

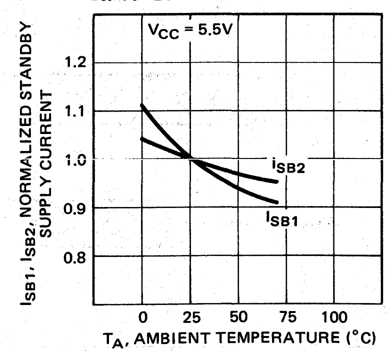
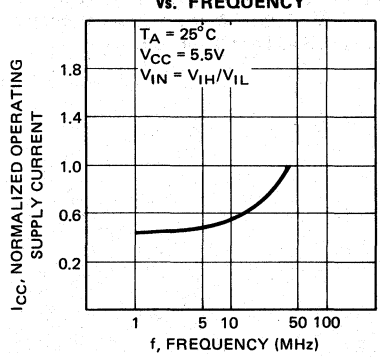


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

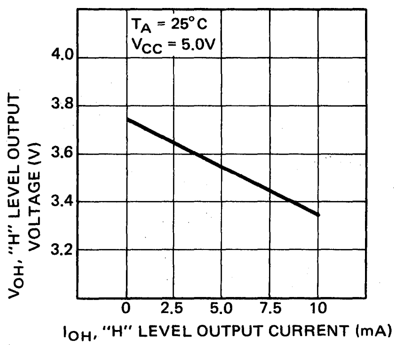


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

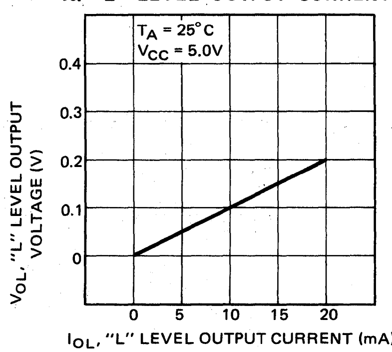


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

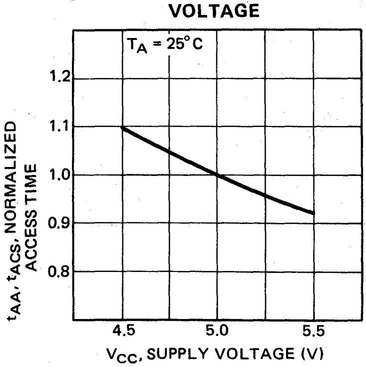


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

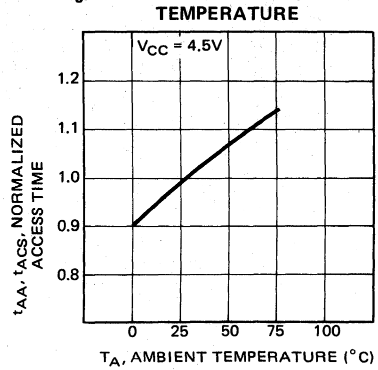
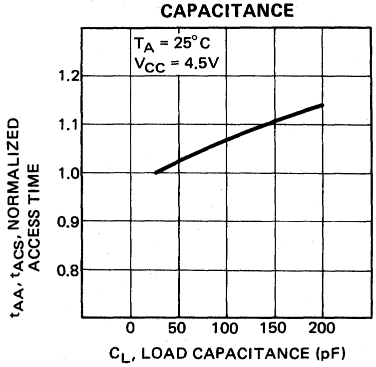


Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE



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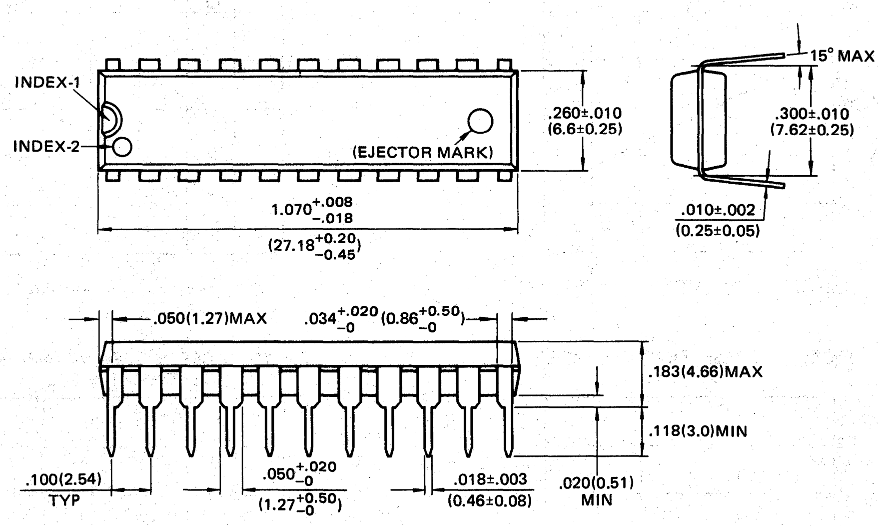
PACKAGE DIMENSIONS

(Suffix: -P)

22-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-22P-M04)



Dimensions in inches (millimeters)

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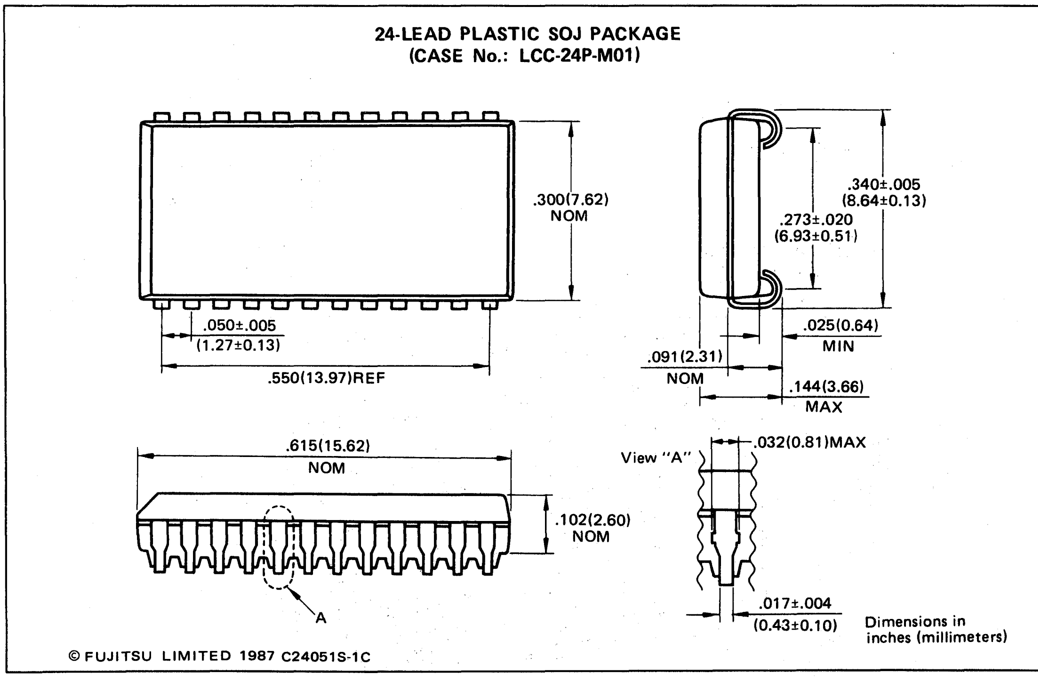
PACKAGE DIMENSIONS

(Suffix: -PJ)



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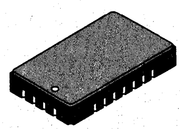
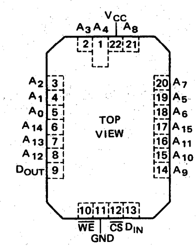
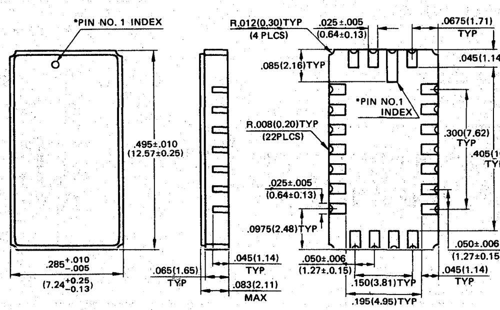
PACKAGE DIMENSIONS
(Suffix: -CV)



CERAMIC PACKAGE
LCC-22C-A01



22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in inches (millimeters)

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FUJITSU

CMOS 65,536-BIT STATIC RANDOM ACCESS MEMORY

MB81C74-25
MB81C74-35

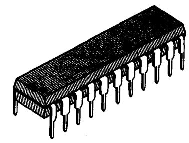
December 1987
Edition 2.0

16K x 4 BIT (65,536-BIT) HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

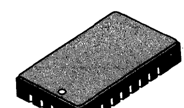
The Fujitsu MB 81C74 is a 16,384-words by 4-bits static random access memory fabricated with a CMOS silicongate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volts power supply is required.

The MB 81C74 is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 16,384 words x 4 bits
- Fast access time: $t_{AA} = t_{ACS}$ = 25 ns max. (MB 81C74-25)
  $t_{AA} = t_{ACS}$ = 35 ns max. (MB 81C74-35)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply ±10% tolerance
- Low power standby: 440 mW max. (Active)
  55 mW max. (Standby, CMOS level)
  110 mW max. (Standby, TTL level)
- Standard 22-pin DIP (300 mil): Suffix: P
- Standard 22-pad LCC : Suffix: CV

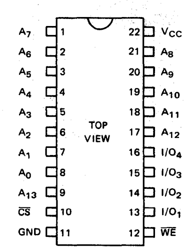


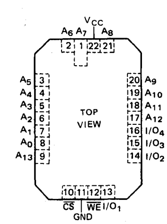
PLASTIC PACKAGE
DIP-22P-M04



CERAMIC PACKAGE
LCC-22C-A01

PIN ASSIGNMENT





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

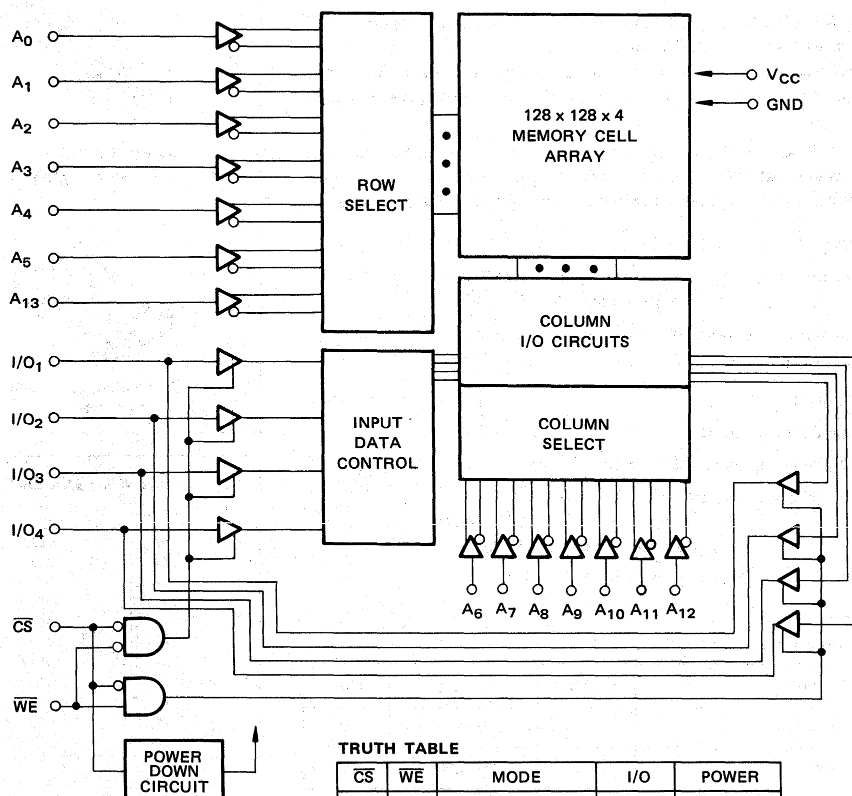
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage		V_{IN}	-3.5 to +7.0	V
Output Voltage		V_{OUT}	-0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5

Fig. 1 – MB 81C74 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			7	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*1		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

*1 −2.0 V Min. for pulse width less than 20 ns. (V_{IL} min. = −0.5 V at DC level)

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DC CHARACTERISTICS

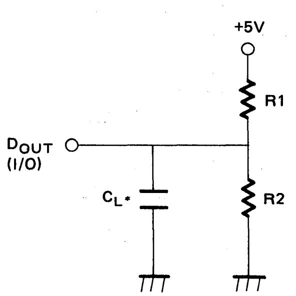
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current	I_{SB1}		10	mA	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$
	I_{SB2}		20	mA	$\overline{CS} = V_{IH}$
Active Supply Current	I_{CC1}		60	mA	I_{OUT} = 0 mA, $\overline{CS} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}
Operating Supply Current	I_{CC2}		80	mA	Cycle = Min., I_{OUT} = 0 mA
Input Leakage Current	I_{LI}	−10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	−10	10	μA	$\overline{CS} = V_{IH}$, $V_{I/O}$ = 0V to V_{CC}
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −4 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 mA

Note: All voltages are referenced to GND

Fig. 2 — AC TEST CONDITIONS

- Output Load



- Input Pulse Levels: 0 V to 3.0 V
- Input Pulse Rise & Fall Times: 5 ns (Transient between 0.8 V and 2.2 V)
- Timing Reference Levels: Input: 1.5 V; Output: 1.5 V

* Including Scope and Jig Capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30 pF	except t_{CLZ}, t_{CHZ}, t_{WLZ}, and t_{WHZ}
Load II	480Ω	255Ω	5 pF	t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}

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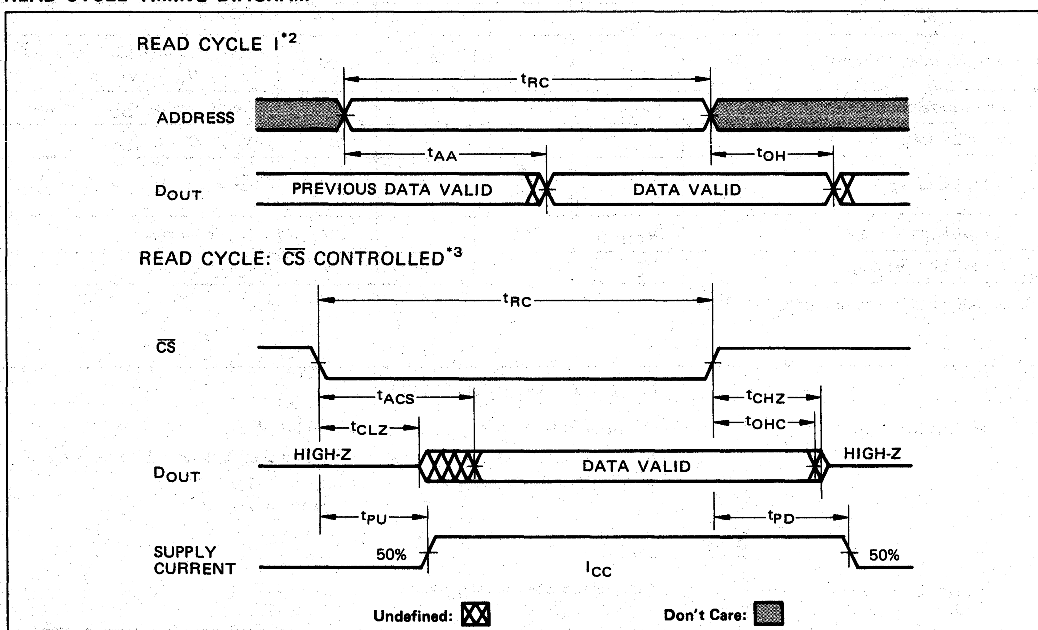
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 81C74-25		MB 81C74-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time*2	t_{AA}		25		35	ns
$\overline{CS}$ Access Time*3	t_{ACS}		25		35	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	3		3		ns
Chip Selection to Output Low-Z*4*5	t_{CLZ}	5		5		ns
Chip Deselection to Output High-Z*4*5	t_{CHZ}		10		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		20		30	ns

READ CYCLE TIMING DIAGRAM*1



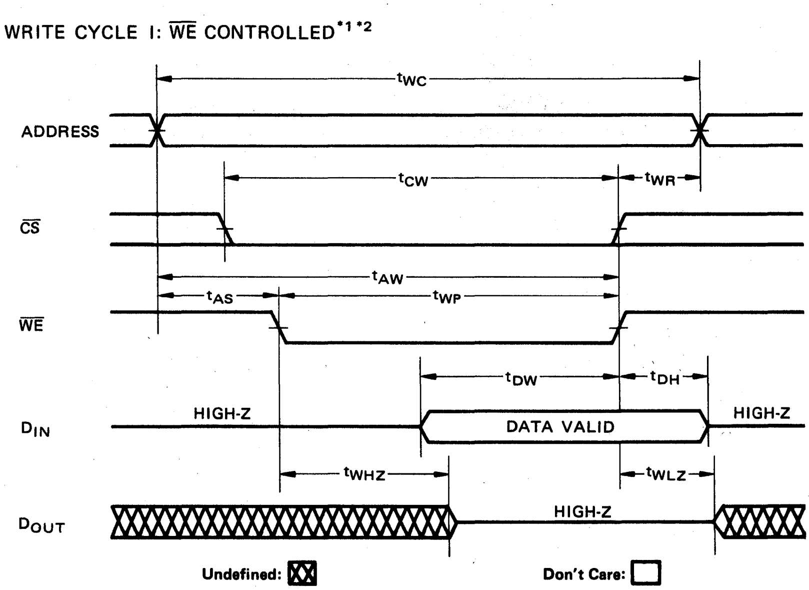
Note:

*1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500 mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE[*1]

Parameter	Symbol	MB 81C74-25		MB 81C74-35		Unit
		Min	Max	Min	Max	
Write Cycle Time[*2]	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	20		30		ns
Chip Select to End of Write	t_{CW}	20		30		ns
Data Valid to End of Write	t_{DW}	13		17		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	20		30		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	2		2		ns
Output High-Z from $\overline{WE}$[*3*4]	t_{WHZ}		10		15	ns
Output Low-Z from $\overline{WE}$[*3*4]	t_{WLZ}	0	10	0	15	ns

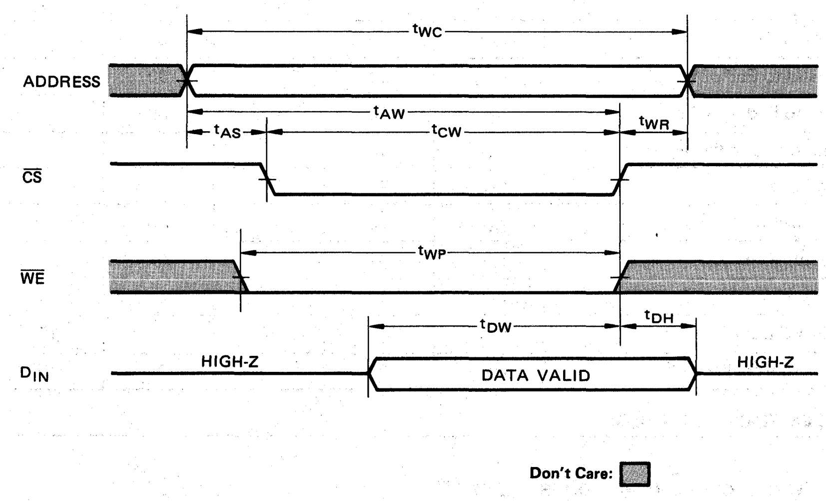
WRITE CYCLE TIMING DIAGRAM



Note:
*1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500 mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.

5

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1 *2



Note:

*1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 — OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

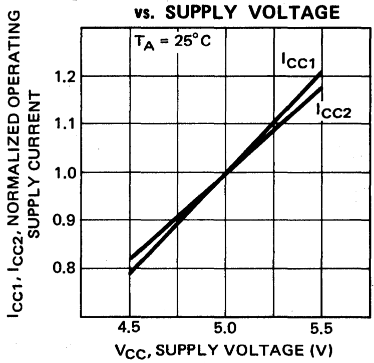


Fig. 4 — OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

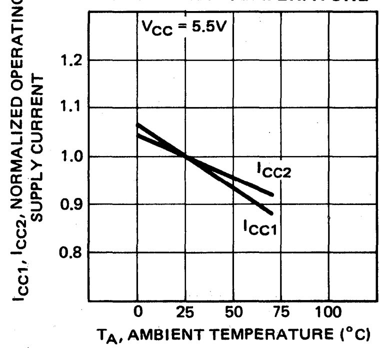


Fig. 5 — STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

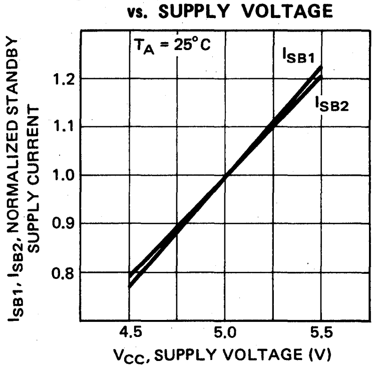


Fig. 6 — STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

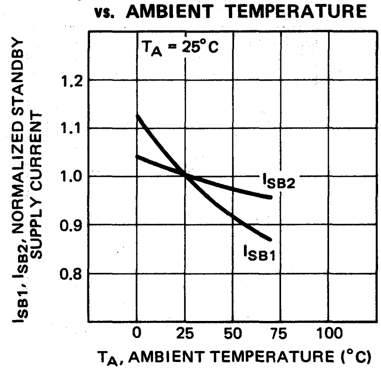
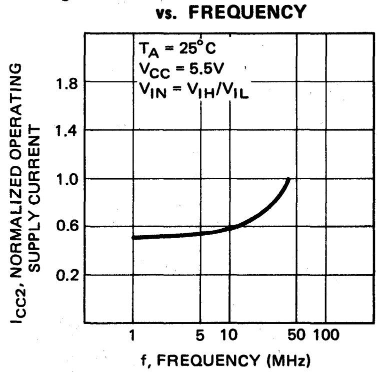


Fig. 7 — OPERATING SUPPLY CURRENT vs. FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 — "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

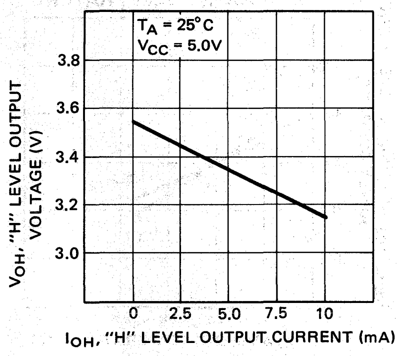


Fig. 9 — "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

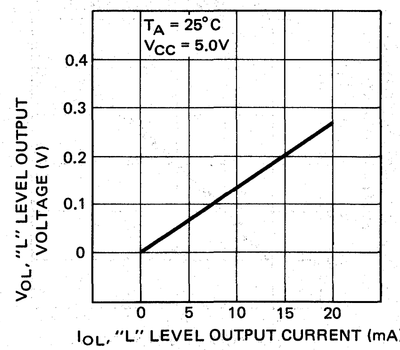


Fig. 10 — ACCESS TIME vs. SUPPLY VOLTAGE

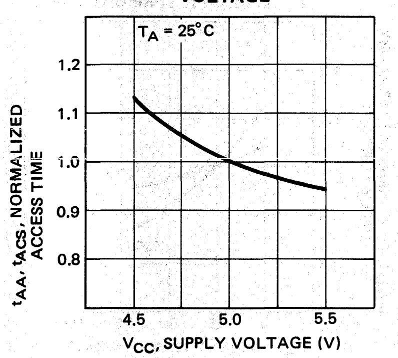


Fig. 11 — ACCESS TIME vs. AMBIENT TEMPERATURE

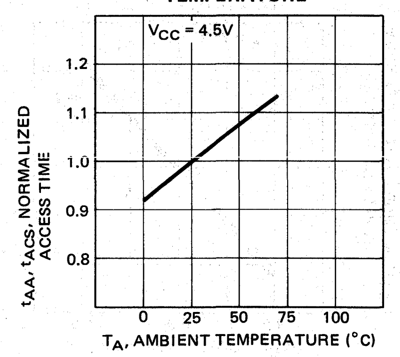
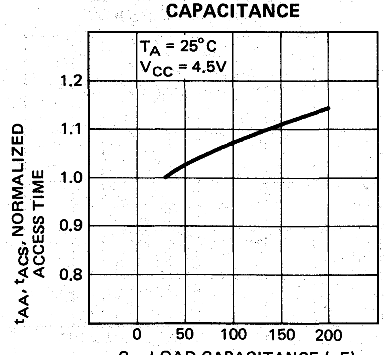


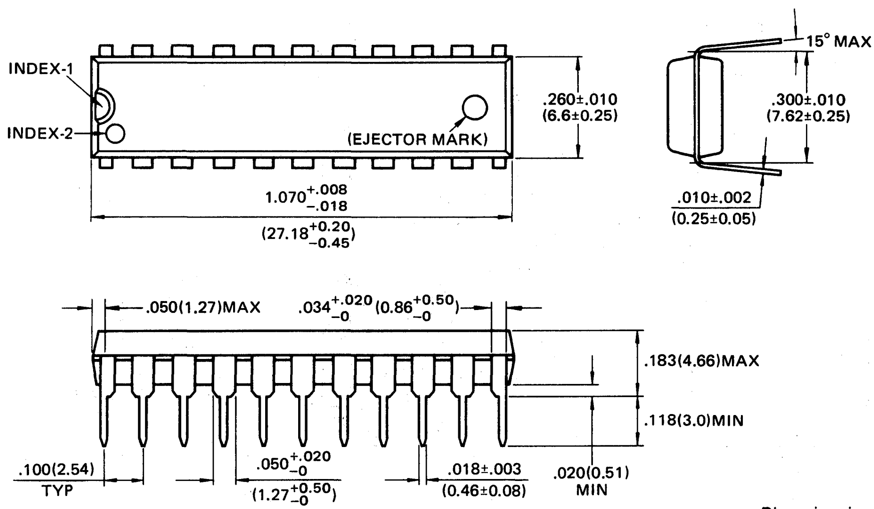
Fig. 12 — ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

(Suffice: -P)

22-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-22P-M04)



Dimensions in inches (millimeters)

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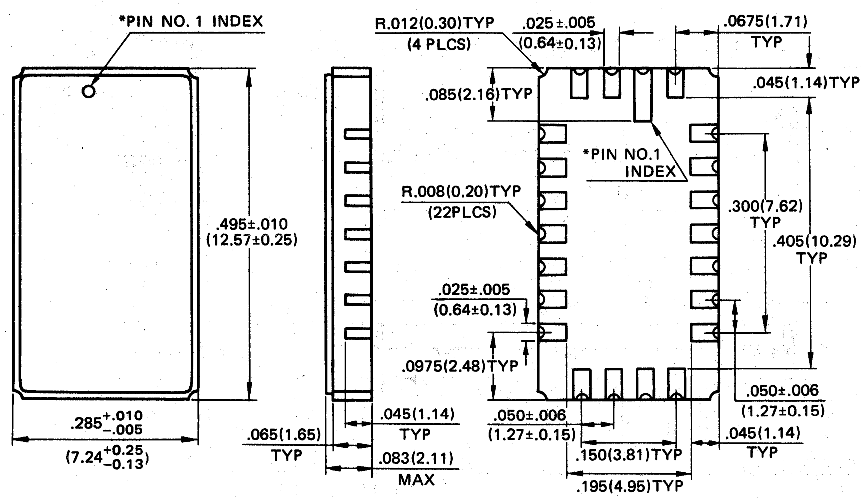
PACKAGE DIMENSIONS

(Suffice: -CV)

22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in inches (millimeters)

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FUJITSU

CMOS 65,536-BIT STATIC RANDOM ACCESS MEMORY

MB81C75-25 MB81C75-35

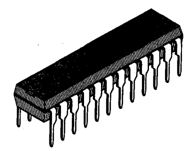
February 1988
Edition 2.0

16K x 4 BIT (65,536-BIT) HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

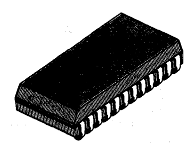
The Fujitsu MB 81C75 is a 16,384-words by 4-bits static random access memory fabricated with a CMOS silicongate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volts power supply is required.

The MB 81C75 is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization : 16,384 words x 4 bits
  Fast access time : t_{AA} = t_{ACS} = 25 ns max. (MB 81C75-25)
  t_{OE} = 10 ns max.
  t_{AA} = t_{ACS} = 35 ns max. (MB 81C75-35)
  t_{OE} = 15 ns max.
- Completely static operation : No clock required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5 V power supply ±10% tolerance
- Low power standby : 440 mW max. (Active)
  55 mW max. (Standby, CMOS level)
  110 mW max. (Standby, TTL level)
- Standard 24-pin DIP (300 mil) : Suffix: P
- Standard 28-pad LCC : Suffix: CV
- Standard 24-pin SOJ (300 mil) : Suffix : PJ

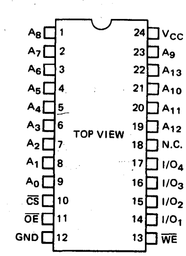


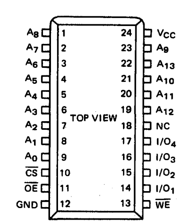
PLASTIC PACKAGE
DIP-24P-M03



PLASTIC PACKAGE
LCC-24P-M01

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

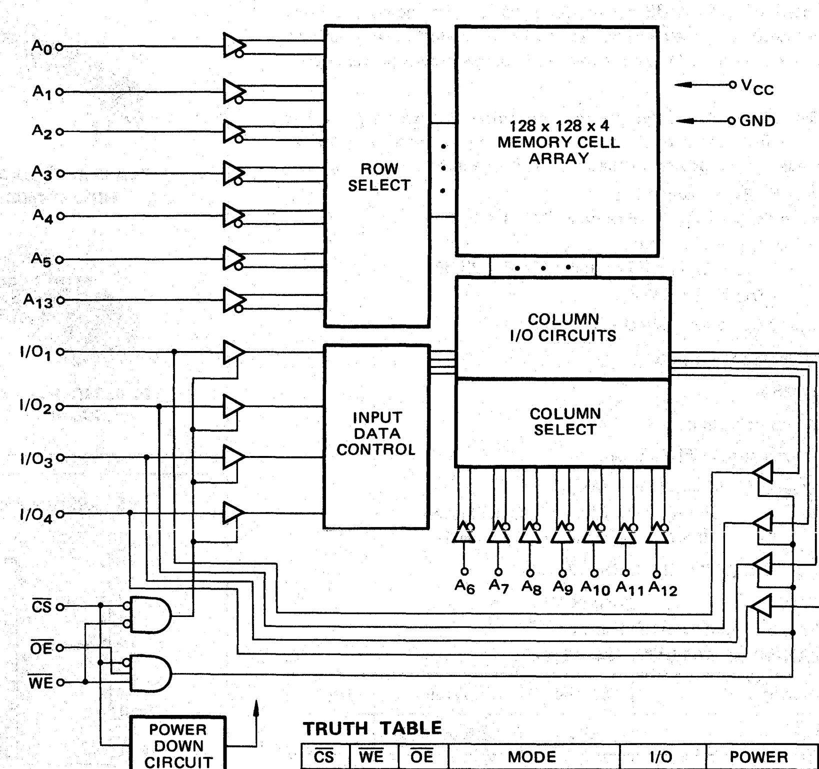
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage		V_{IN}	-3.5 to +7.0	V
Output Voltage		V_{OUT}	-0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 — MB 81C75 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O	POWER
H	X	X	NOT SELECTED	HIGH-Z	STANDBY
L	H	H	OUTPUT DESABLE	HIGH-Z	ACTIVE
L	H	L	READ	D_{OUT}	ACTIVE
L	L	X	WRITE	D_{IN}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
I/O Capacitance ($V_{I/O}$ = 0 V)	$C_{I/O}$			7	pF
Input Capacitance (V_{IN} = 0 V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -2.0 V Min, for pulse width less than 20 ns. (V_{IL} Min = -0.5 V at DC Level)

DC CHARACTERISTICS

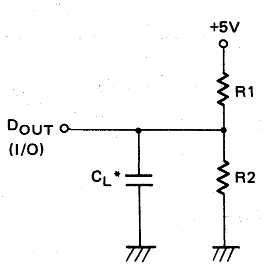
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	Value		Unit
			Min	Max	
Standby Supply Current	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V	I_{SB1}		10	mA
	$\overline{CS} = V_{IH}$	I_{SB2}		20	
Active Supply Current	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}, $I_{OUT} = 0$ mA	I_{CC1}		60	mA
Operating Supply Current	Cycle = Min., $I_{OUT} = 0$ mA	I_{CC2}		80	
Input Leakage Current	$V_{IN} = 0$ V to V_{CC}	I_{LI}	-10	10	μA
Output Leakage Current	$\overline{CS} = V_{IH}$, $V_{I/O} = 0$ V to V_{CC}	$I_{LI/O}$	-10	10	μA
Output High Voltage	$I_{OH} = -4$ mA	V_{OH}	2.4		V
Output Low Voltage	$I_{OL} = 8$ mA	V_{OL}		0.4	V

Note: All voltages are referenced to GND

Fig. 2 – AC TEST CONDITIONS

- Output Load



* Including Scope and Jig Capacitance

- Input Pulse Levels: : 0 V to 3.0 V
- Input Pulse Rise & Fall Times : 5 ns (Transient between 0.8 V and 2.2 V)
- Timing Reference Levels : Input : 1.5 V
  : Output : 1.5 V

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30 pF	except t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}, t_{OLZ} and t_{OHZ}
Load II	480Ω	255Ω	5 pF	t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}, t_{OLZ} and t_{OHZ}

5

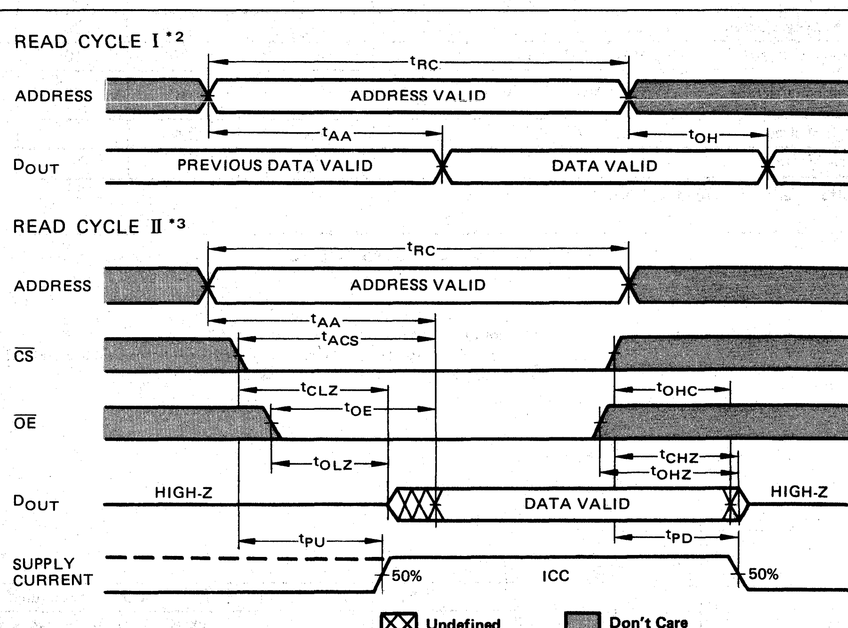
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 81C75-25		MB 81C75-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time*2	t_{AA}		25		35	ns
$\overline{CS}$ Access Time*3	t_{ACS}		25		35	ns
$\overline{OE}$ Access Time*3	t_{OE}		10		15	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	3		3		ns
$\overline{CS}$ to output Low-Z*4*5	t_{CLZ}	5		5		ns
$\overline{OE}$ to Output in Low-Z*4*5	t_{OLZ}	0		0		ns
$\overline{CS}$ to Output High-Z*4*5	t_{CHZ}		10		15	ns
$\overline{OE}$ to Output High-Z*4*5	t_{OHZ}		10		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Dwown from $\overline{CS}$	t_{PD}		20		30	ns

READ CYCLE TIMING DIAGRAM*1

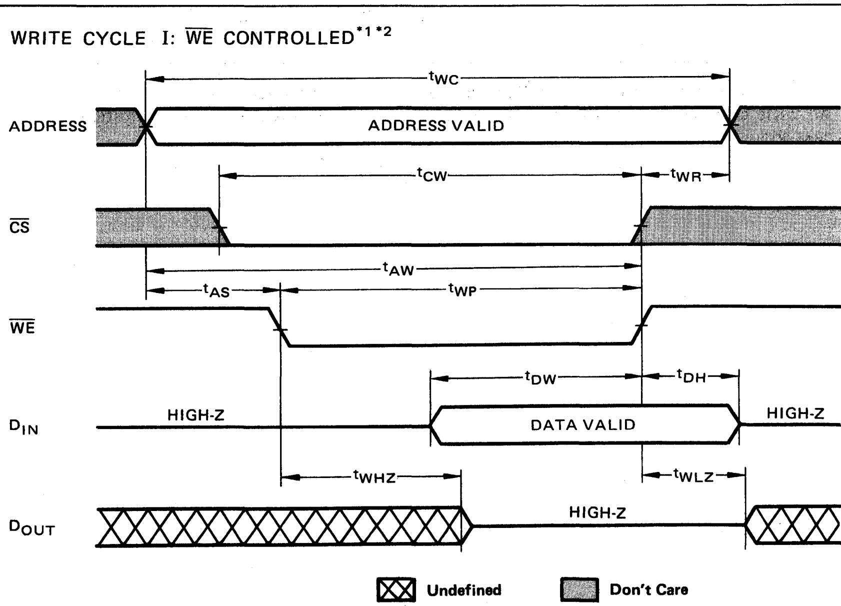


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}=V_{IL}$, $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE*1

Parameter	Symbol	MB 81C75-25		MB 81C75-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	20		30		ns
Chip Select to End of Write End of Write	t_{CW}	20		30		ns
Data Valid to End of Write	t_{DW}	13		17		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	20		30		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	2		2		ns
Output High-Z from $\overline{WE}$*3*4	t_{WHZ}		10		15	ns
Output Low-Z from $\overline{WE}$*3*4	t_{WLZ}	0	20	0	30	ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.

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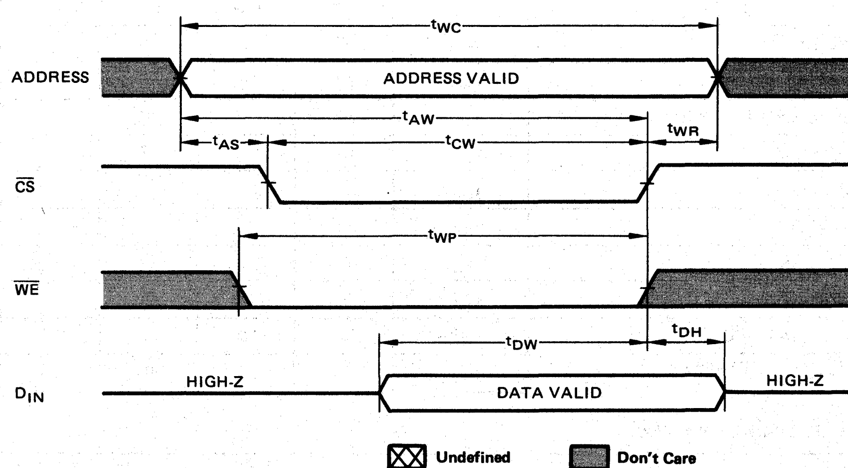
WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1 *2



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.

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TYPICAL CHARACTERISTICS CURVES

Fig. 3 — OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

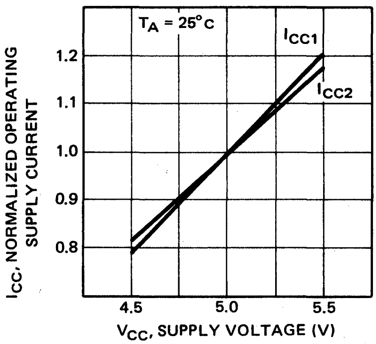


Fig. 4 — OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

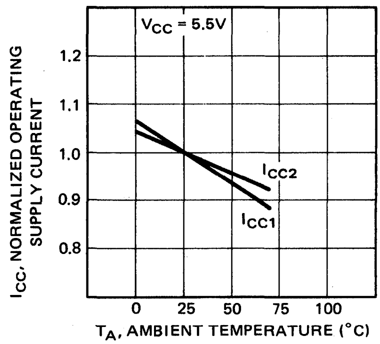


Fig. 5 — STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

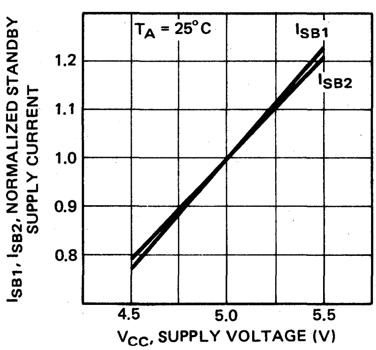


Fig. 6 — STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

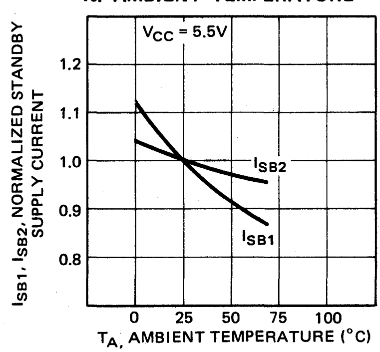
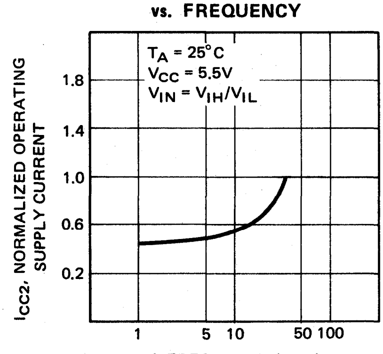


Fig. 7 — OPERATING SUPPLY CURRENT vs. FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 — "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

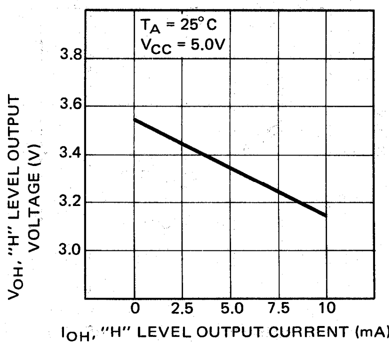


Fig. 9 — "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

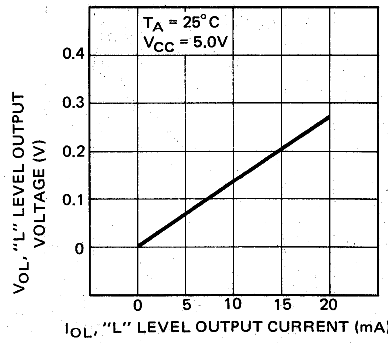


Fig. 10 — ACCESS TIME vs. SUPPLY VOLTAGE

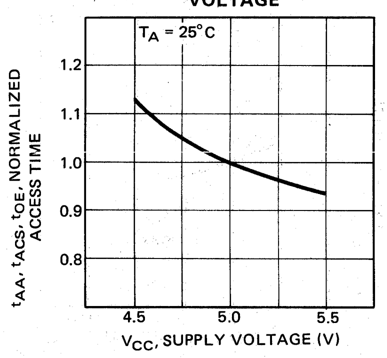


Fig. 11 — ACCESS TIME vs. AMBIENT TEMPERATURE

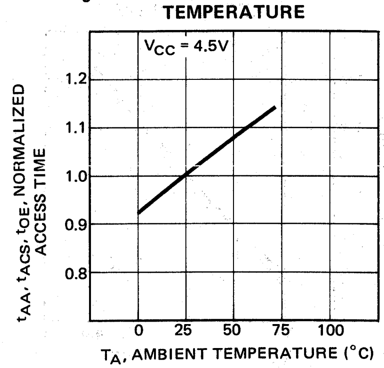
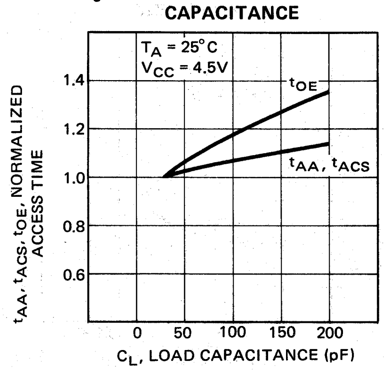


Fig. 12 — ACCESS TIME vs. LOAD CAPACITANCE

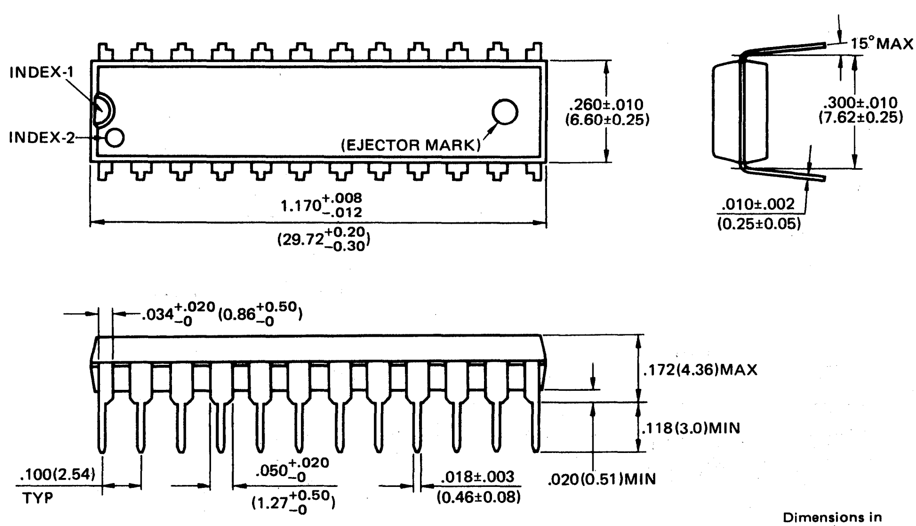


5

PACKAGE DIMENSIONS

(Suffix: P)

24-LEADS PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)

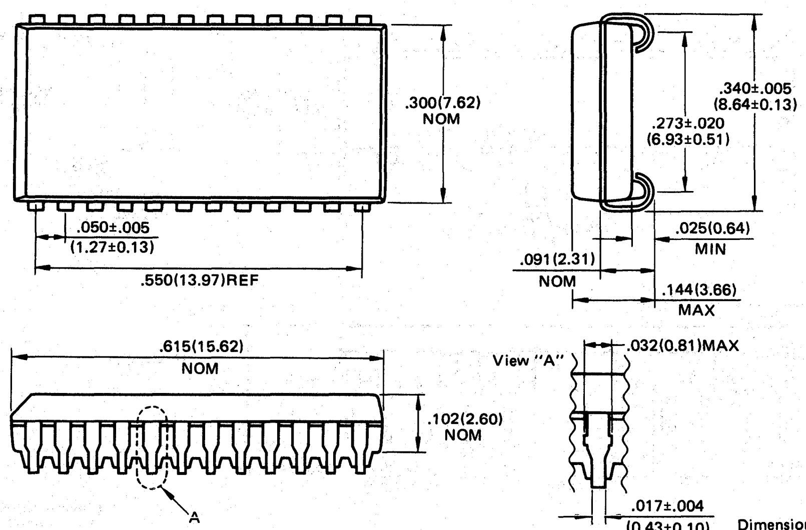


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

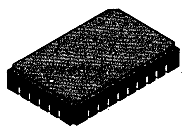
(Suffix: -PJ)

24-LEAD PLASTIC SOJ PACKAGE
(CASE No.: LCC-24P-M01)

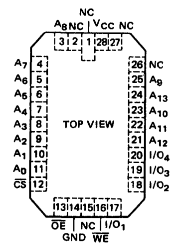


Dimensions in inches (millimeters)

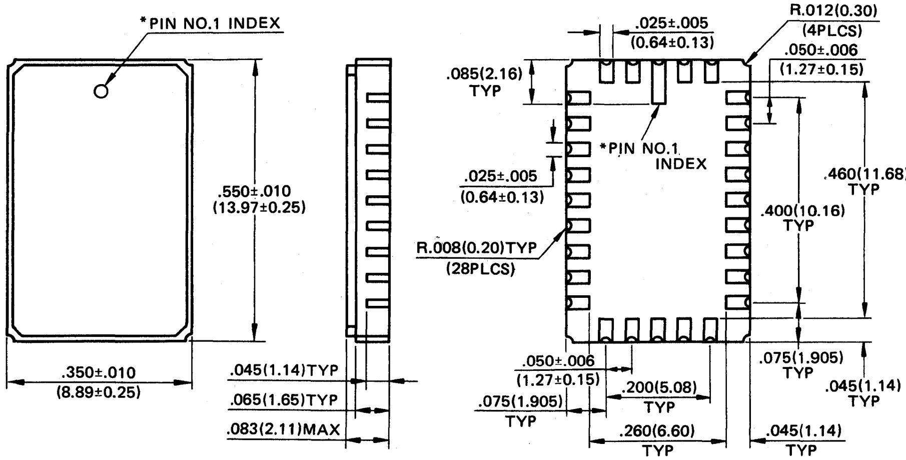
PACKAGE DIMENSIONS
(Suffix: CV)



CERAMIC PACKAGE
LCC-28C-A03



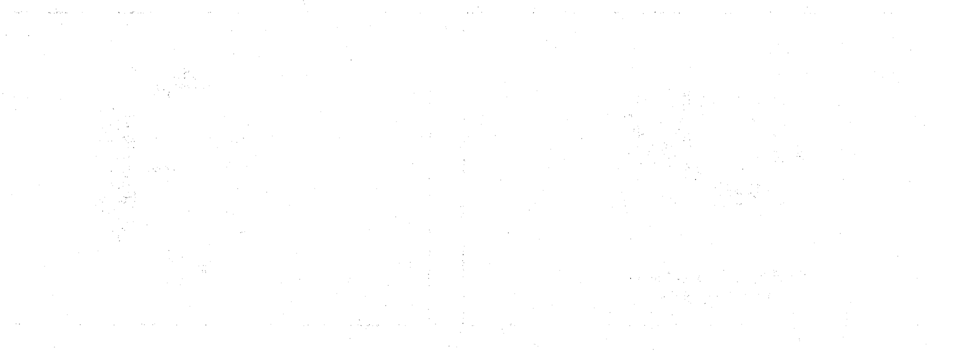
28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A03)

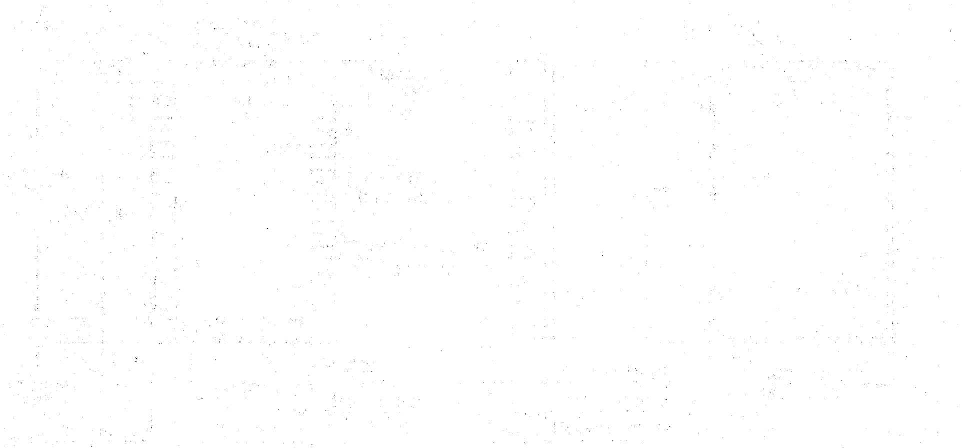


*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in inches and (millimeters)

5





FUJITSU

CMOS 65536-BIT STATIC RANDOM ACCESS MEMORY

MB81C78A-35
MB81C78A-45

November 1987
Edition 2.0

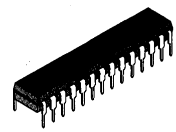
64K-BIT (8192x8) HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB 81C78A is 8192 words x 8 bits static random access memory fabricated with a CMOS process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single 5 volts power supply is required.

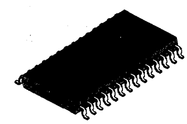
A separate chip select ($\overline{CS}_1$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS}_1$, the other deselected packages automatically power down.

All devices offer the advantages of low power dissipation, low cost, and high performance.

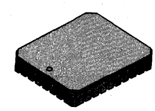
- Organization: 8192 words x 8 bits
- Static operation: No clock or timing strobe required
- Fast access time: $t_{AA} = t_{ACS1}$ = 35 ns max. (MB 81C78A-35)
  $t_{AA} = t_{ACS1}$ = 45 ns max. (MB 81C78A-45)
- Low power consumption: 495 mW max. (Operating)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5V supply, ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 28-pin Plastic DIP package (Suffix: -P-SK)
- Standard 28-pin Bend type Plastic Flat package (Suffix: -PF)
- Standard 32-pad Leadless Chip Carrier (Suffix: -CV)



PLASTIC PACKAGE
DIP-28P-M04

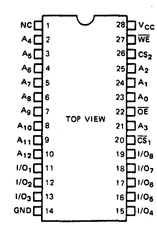


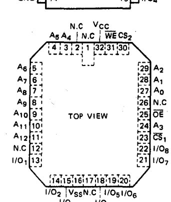
PLASTIC PACKAGE
FPT-28P-M02



CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

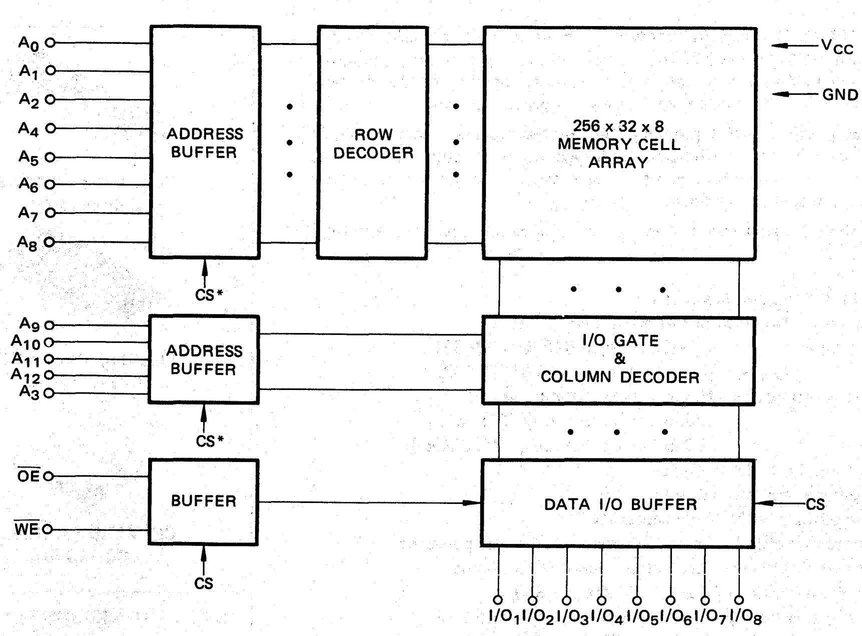
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	-3.5 to +7	V
Output Voltage on any I/O with respect to GND		V_{OUT}	-0.5 to +7	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	PLASTIC	T_{STG}	-40 to +125	°C
	CERAMIC		-65 to +150	

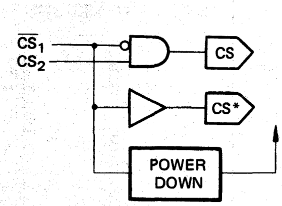
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 — MB 81C78A BLOCK DIAGRAM





TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V) ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN} = 0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	pF

5

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.5V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{LO}	-10	10	μA	$\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, V_{OUT} = 0V to V_{CC}
Operating Supply Current	I_{CC}		90	mA	$\overline{CS_1} = V_{IL}$ I/O = Open, Cycle = Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC} = Min to Max. $\overline{CS_1} = V_{CC}-0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$
	I_{SB2}		25	mA	$\overline{CS_1} = V_{IH}$
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC} = 0V to V_{CC} Min. $\overline{CS_1}$ = Lower of V_{CC} or V_{IH} Min.

5

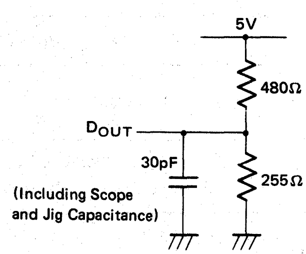
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V

Fig. 2

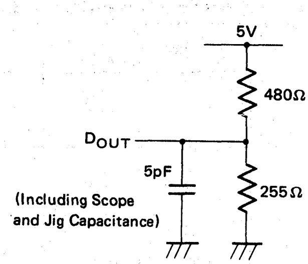
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



5

AC CHARACTERISTICS

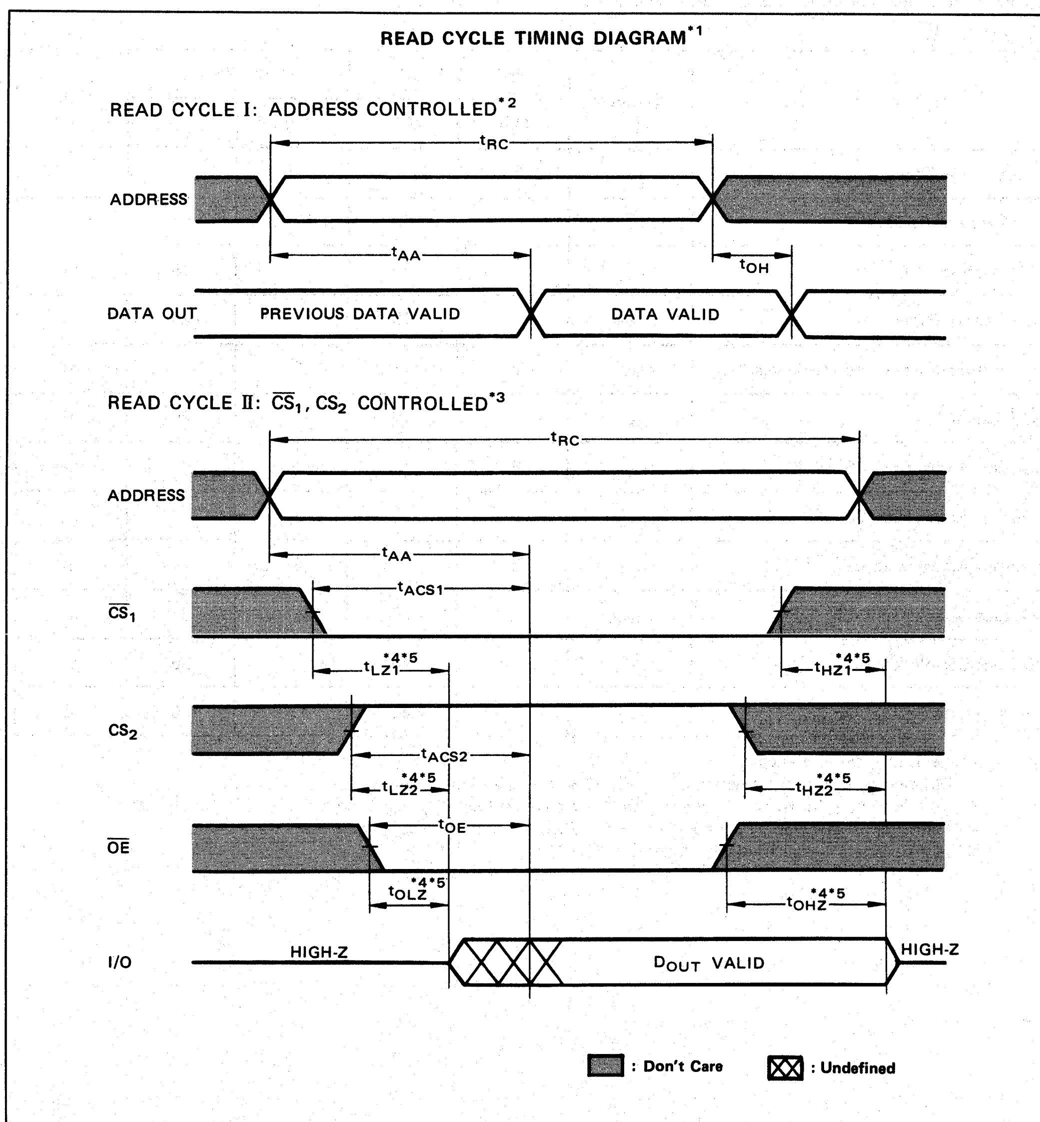
(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 81C78A-35		MB81C78A-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time*2	t_{AA}		35		45	ns
$\overline{CS}_1$ Access Time*3	t_{ACS1}		35		45	ns
CS_2 Access Time*3	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		15		20	ns
Output Active from $\overline{CS}_1$ *4*5	t_{LZ1}	5		5		ns
Output Active from CS_2 *4*5	t_{LZ2}	3		3		ns
Output Active from $\overline{OE}$*4*5	t_{OLZ}	3		3		ns
Output Disable from $\overline{CS}_1$ *4*5	t_{HZ1}		20		25	ns
Output Disable from CS_2 *4*5	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$*4*5	t_{OHZ}		20		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

5



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE[*1]

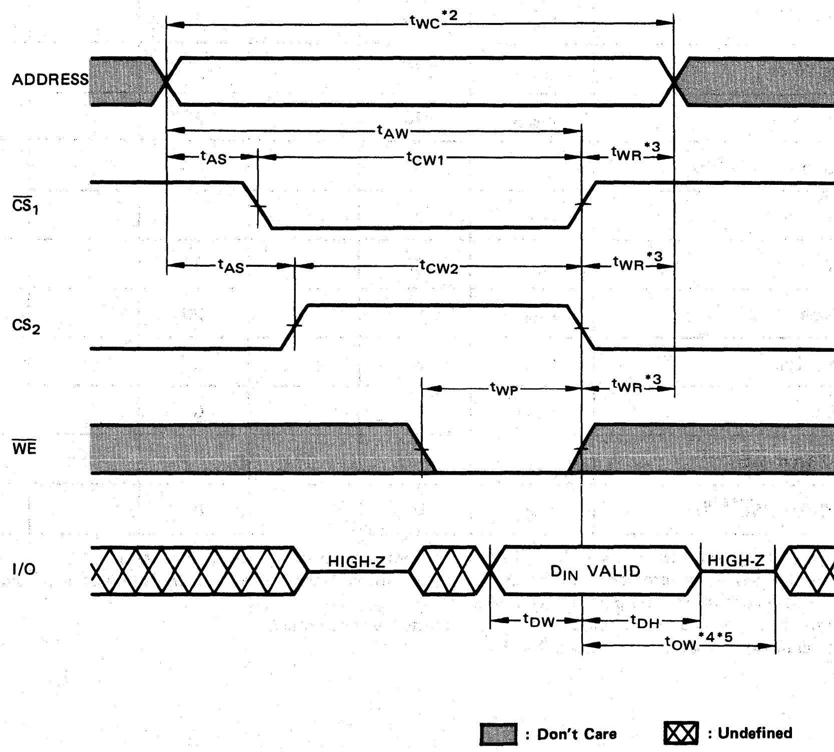
Parameter	Symbol	MB 81C78A-35		MB81C78A-45		Unit
		Min	Max	Min	Max	
Write Cycle Time[*2]	t_{WC}	35		45		ns
$\overline{CS}_1$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time[*3]	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$[*4*5]	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$[*4*5]	t_{OW}	0		0		ns

Note: *1 If $\overline{CS}_1$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

5

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE I: $\overline{CS}_1$, CS_2 CONTROLLED

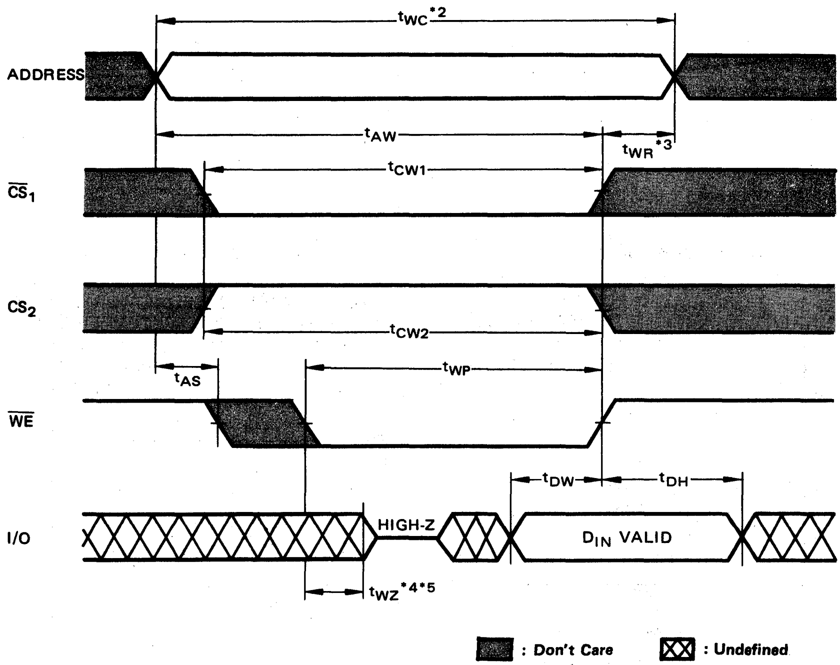


Note: *1 If $\overline{OE}$, $\overline{CS}_1$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycle are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

5

WRITE CYCLE TIMING DIAGRAM[*1]

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS}_1$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

5

Fig. 3 — NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

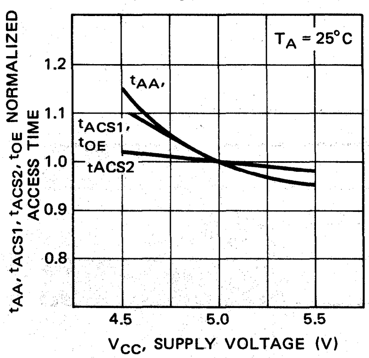


Fig. 4 — NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

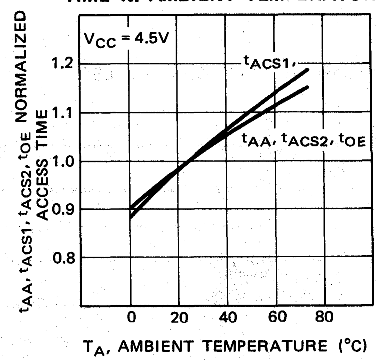


Fig. 5 — NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

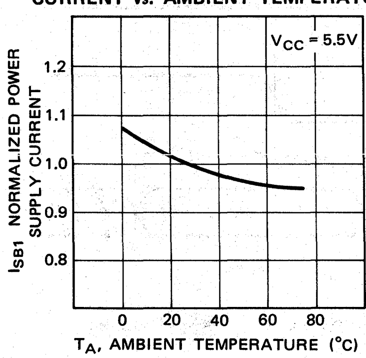


Fig. 6 — NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

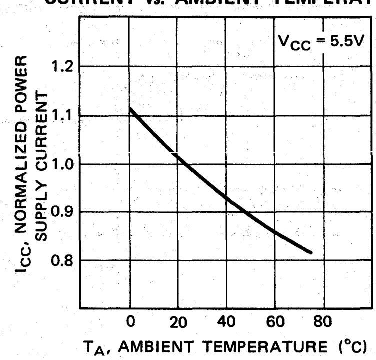


Fig. 7 — NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

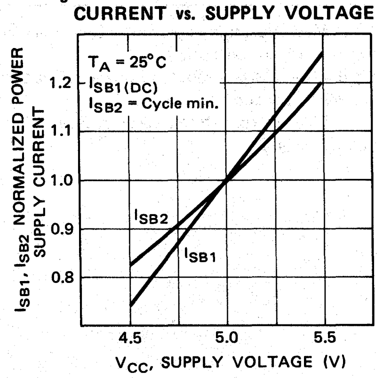


Fig. 8 — NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

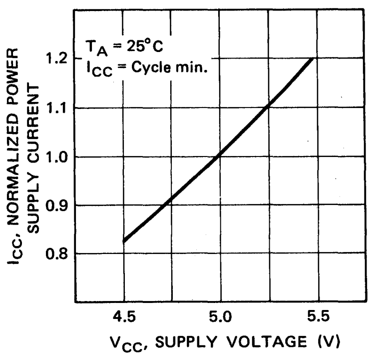


Fig. 9 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

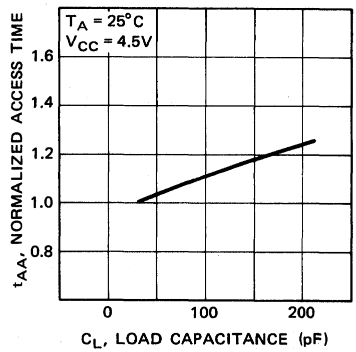


Fig. 10 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

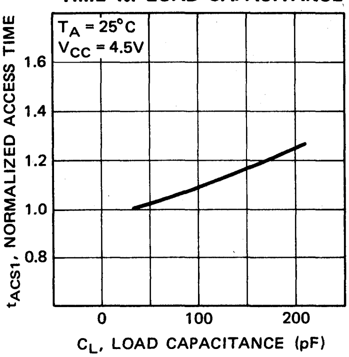


Fig. 11 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

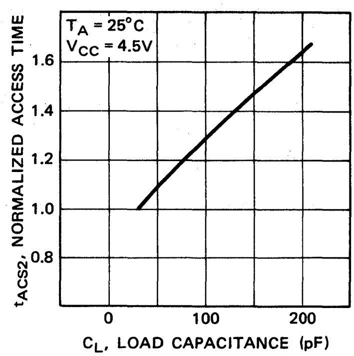
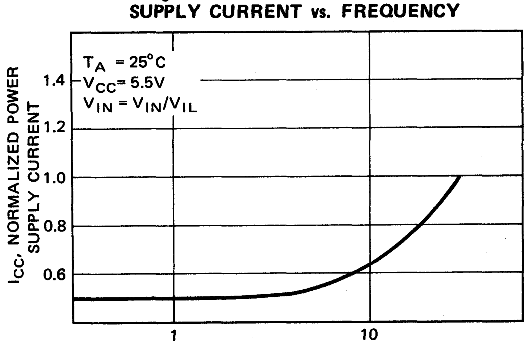


Fig. 12 — NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY



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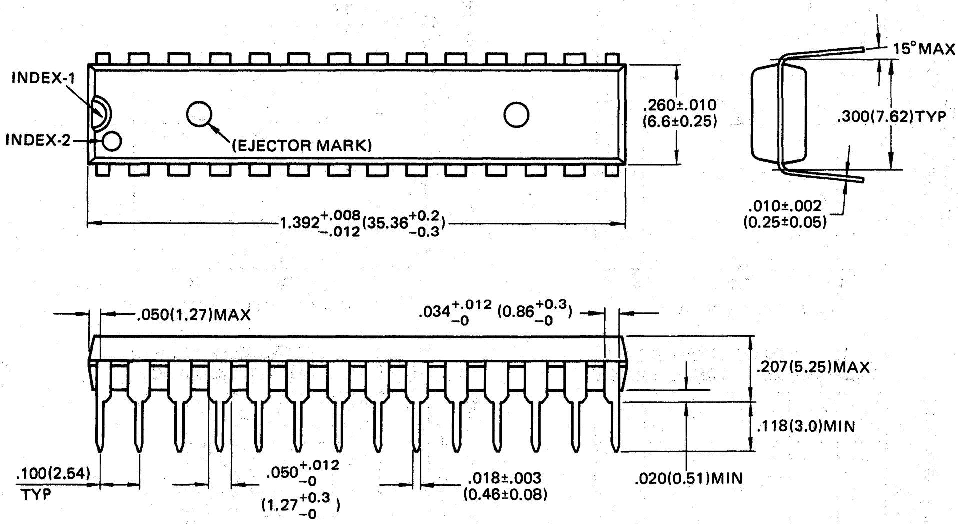
PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

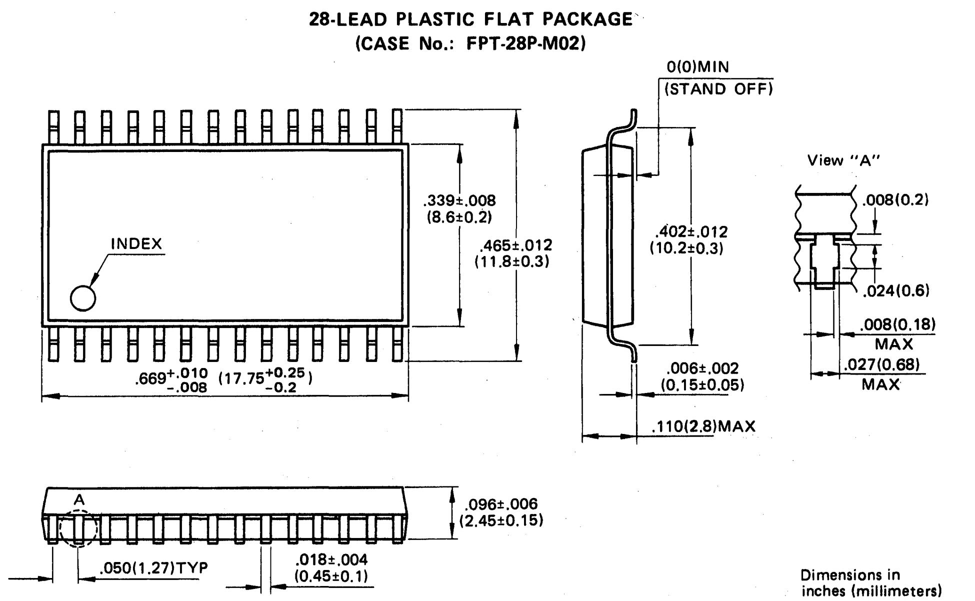
28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: -PF)



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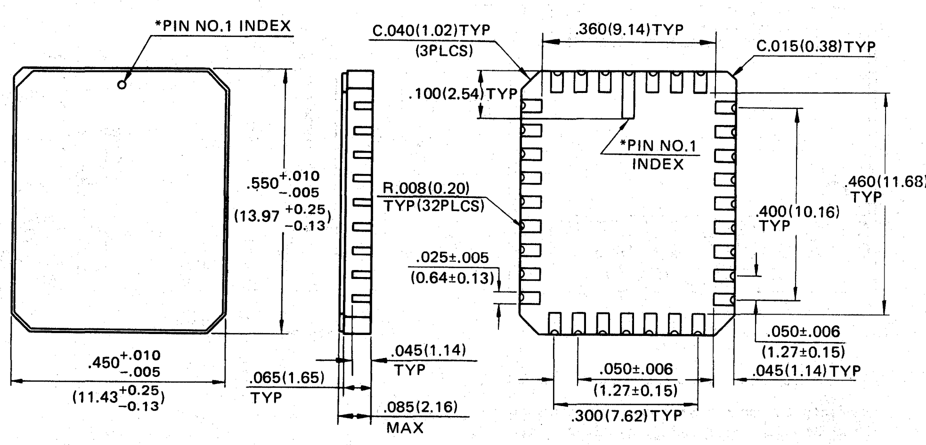
PACKAGE DIMENSIONS

CERAMIC LCC (Suffix: -CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches
(millimeters)

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FUJITSU

CMOS 73728-BIT STATIC RANDOM ACCESS MEMORY

MB81C79A-35
MB81C79A-45

November 1987
Edition 2.0

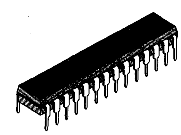
72K-BIT (8192x9) HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB 81C79A is 8192 words x 9 bits static random access memory fabricated with a CMOS process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single 5 volts power supply is required.

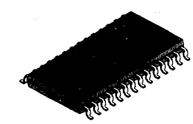
A separate chip select ($\overline{CS}_1$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS}_1$, the other deselected packages automatically power down.

All devices offer the advantages of low power dissipation, low cost, and high performance.

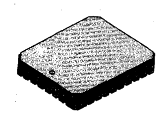
- Organization: 8192 words x 9 bits
- Static operation: No clock or timing strobe required
- Fast access time: $t_{AA} = t_{ACS1}$ = 35 ns max. (MB 81C79A-35)
  $t_{AA} = t_{ACS1}$ = 45 ns max. (MB 81C79A-45)
- Low power consumption: 495 mW max. (Operating)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5V supply, ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 28-pin Plastic DIP package (Suffix: -P-SK)
- Standard 28-pin Bend type Plastic Flat package (Suffix: -PF)
- Standard 32-pad Leadless Chip Carrier (Suffix: -CV)



PLASTIC PACKAGE
DIP-28P-M04

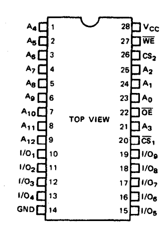


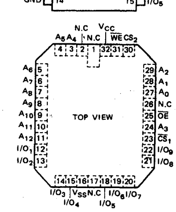
PLASTIC PACKAGE
FPT-28P-M02



CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT





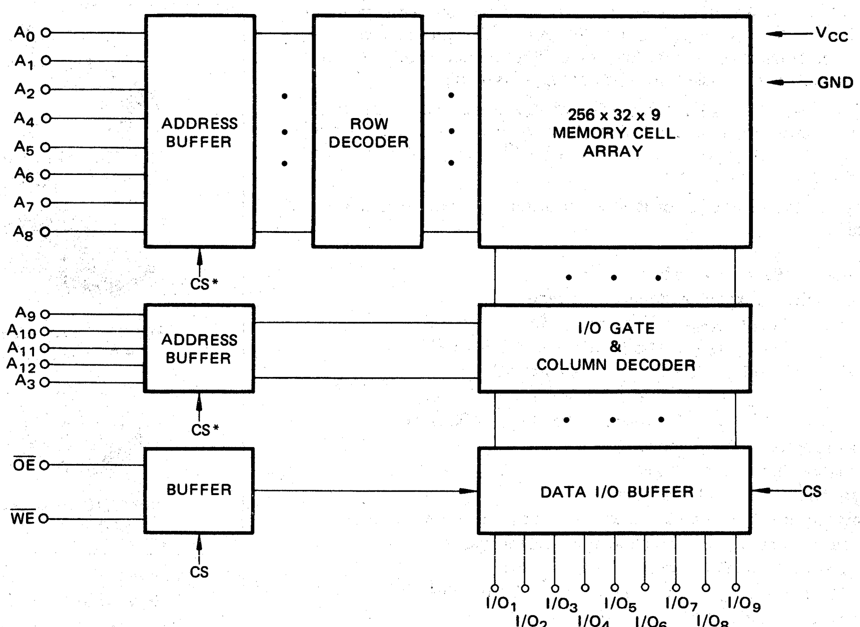
ABSOLUTE MAXIMUM RATINGS (See NOTE)

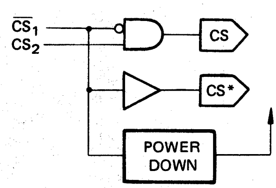
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	–0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	–3.5 to +7	V
Output Voltage on any I/O with respect to GND		V_{OUT}	–0.5 to +7	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	–10 to +85	°C
Storage Temperature	PLASTIC	T_{STG}	–40 to +125	°C
	CERAMIC		–65 to +150	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 81C79A BLOCK DIAGRAM





TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V) ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN} = 0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.5V at DC level)

5

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{LO}	-10	10	μA	$\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, V_{OUT} = 0V to V_{CC}
Operating Supply Current	I_{CC}		90	mA	$\overline{CS_1} = V_{IL}$ I/O = Open, Cycle = Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC} = Min to Max. $\overline{CS_1} = V_{CC}-0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$
	I_{SB2}		25	mA	$\overline{CS_1} = V_{IH}$
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC} = 0V to V_{CC} Min. $\overline{CS_1}$ = Lower of V_{CC} or V_{IH} Min.

5

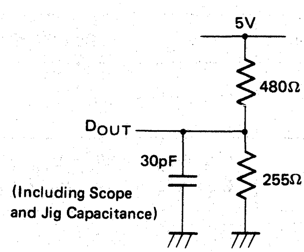
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V

Fig. 2

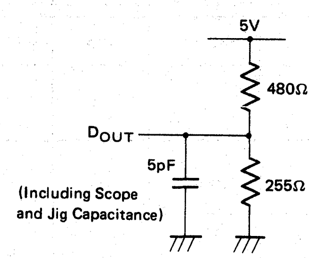
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE[*1]

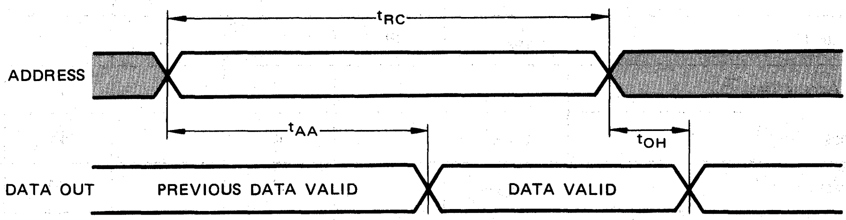
Parameter	Symbol	MB 81C79A-35		MB 81C79A-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time[*2]	t_{AA}		35		45	ns
$\overline{CS}_1$ Access Time[*3]	t_{ACS1}		35		45	ns
CS_2 Access Time[*3]	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		15		20	ns
Output Active from $\overline{CS}_1$[*4*5]	t_{LZ1}	5		5		ns
Output Active from CS_2[*4*5]	t_{LZ2}	3		3		ns
Output Active from $\overline{OE}$[*4*5]	t_{OLZ}	3		3		ns
Output Disable from $\overline{CS}_1$[*4*5]	t_{HZ1}		20		25	ns
Output Disable from CS_2[*4*5]	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$[*4*5]	t_{OHZ}		20		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

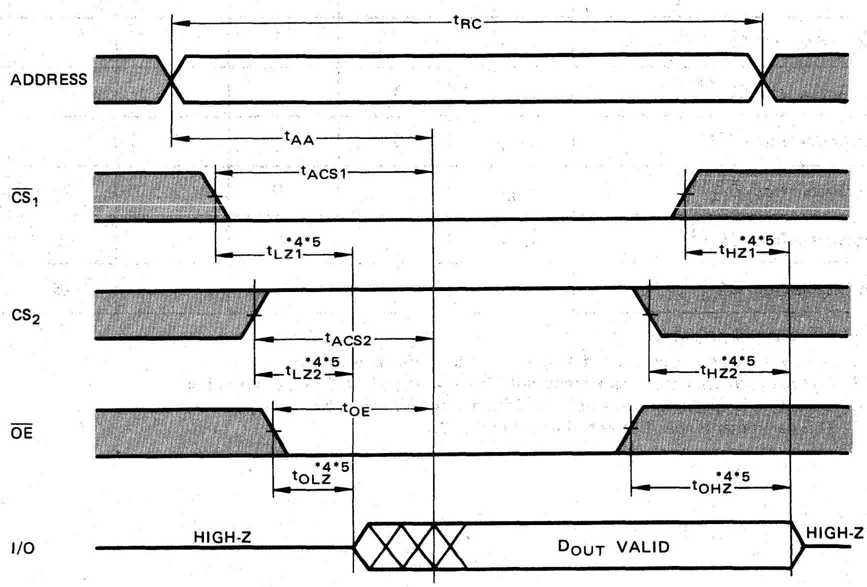
5

READ CYCLE TIMING DIAGRAM*1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS}_1$, CS_2 CONTROLLED*3



⊠ : Undefined ▩ : Don't Care

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE[*1]

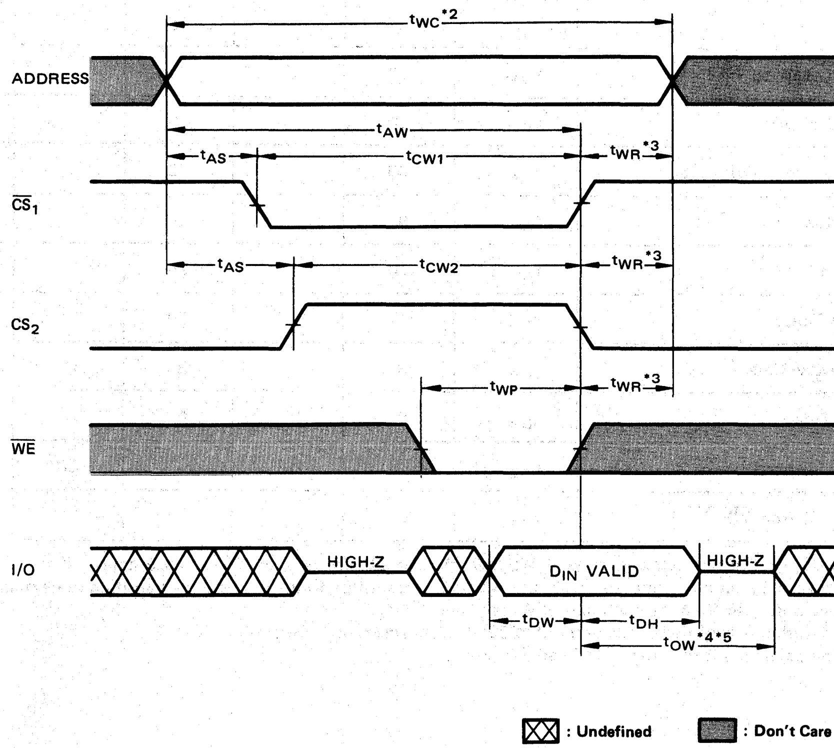
Parameter	Symbol	MB 81C79A-35		MB 81C79A-45		Unit
		Min	Max	Min	Max	
Write Cycle Time[*2]	t_{WC}	35		45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time[*3]	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$[*4*5]	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$[*4*5]	t_{OW}	0		0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

5

WRITE CYCLE TIMING DIAGRAM*1

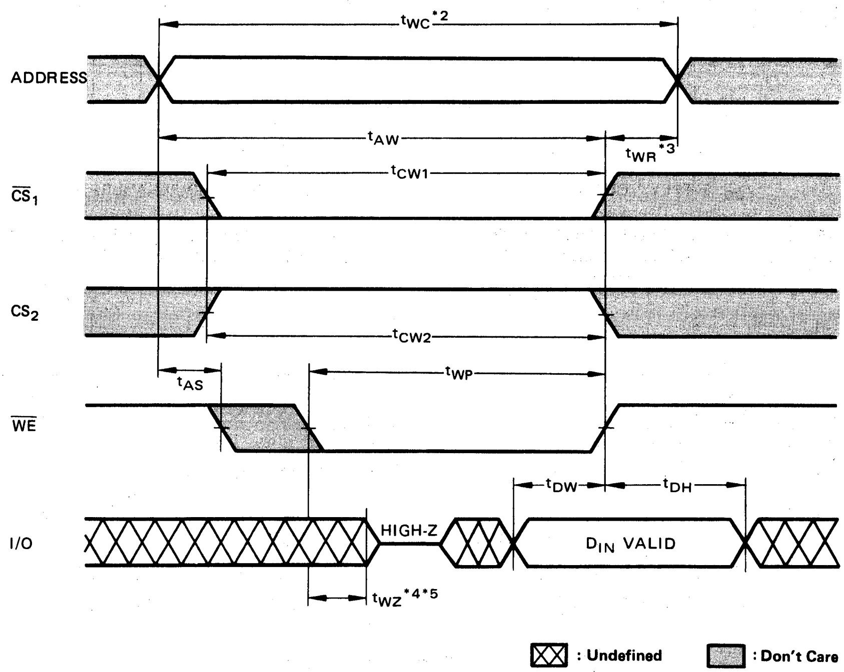
WRITE CYCLE I: $\overline{CS_1}$, CS_2 CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycle are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

Fig. 3 — NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

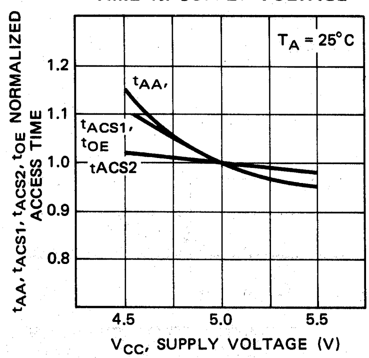


Fig. 4 — NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

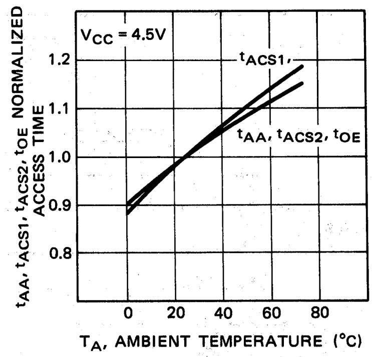


Fig. 5 — NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

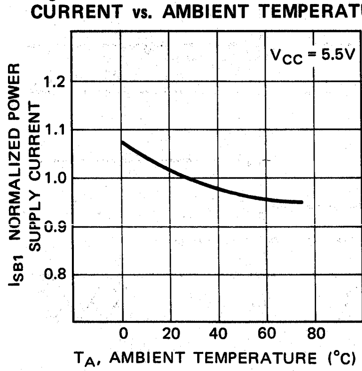


Fig. 6 — NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

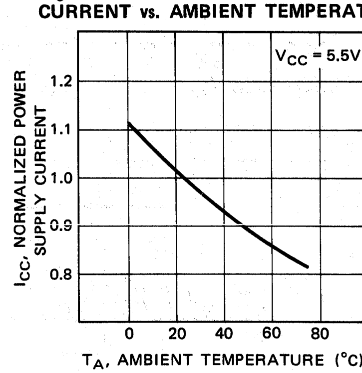


Fig. 7 — NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

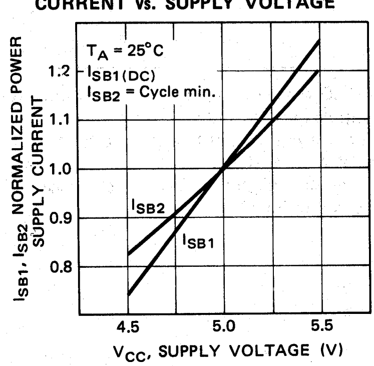


Fig. 8 — NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

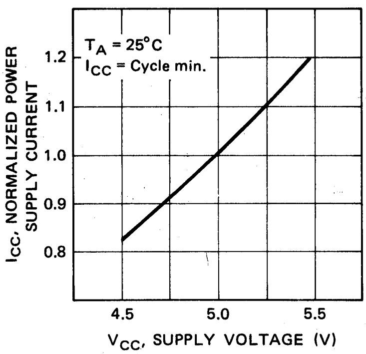


Fig. 9 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

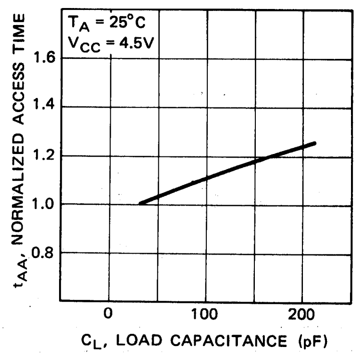


Fig. 10 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

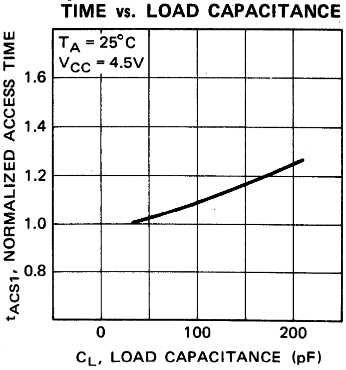


Fig. 11 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

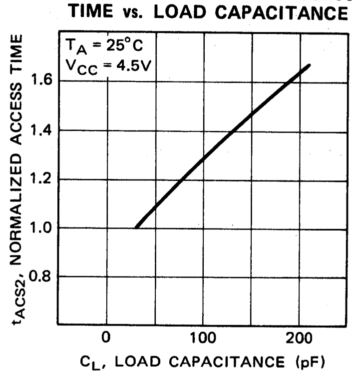
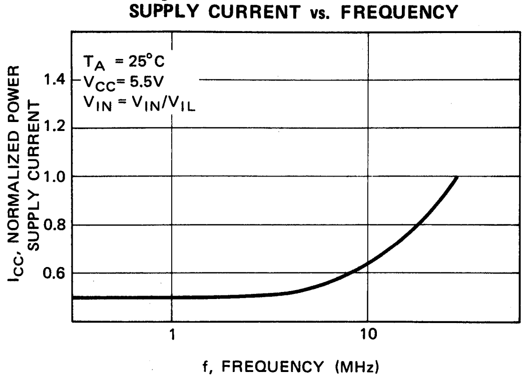


Fig. 12 — NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

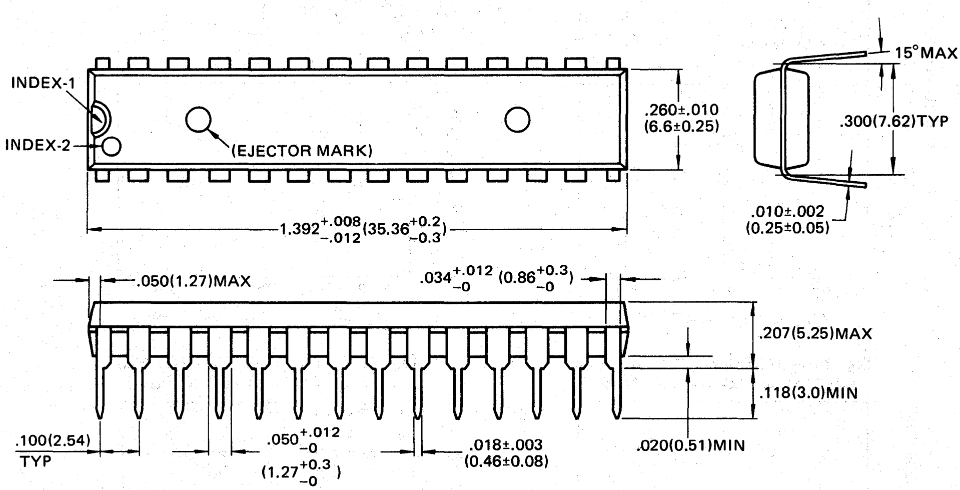


5

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)

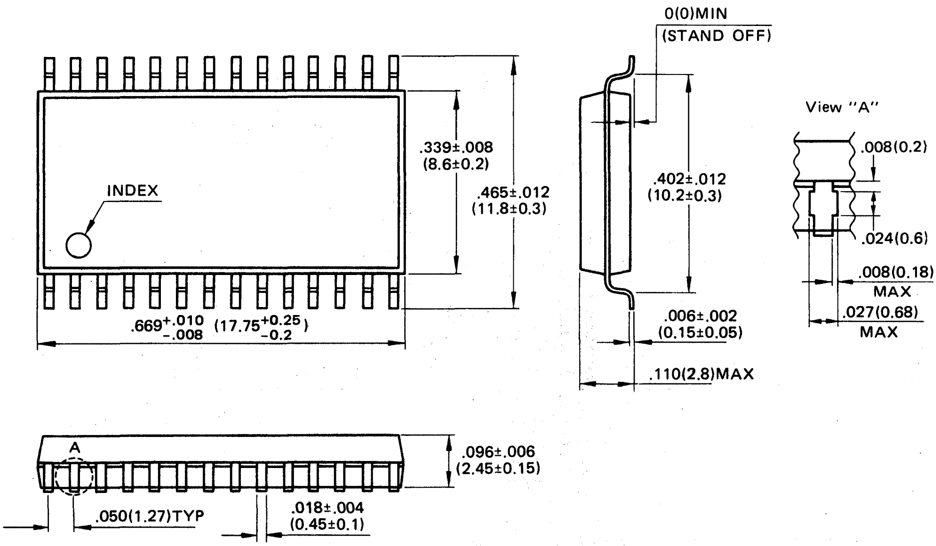


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: -PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



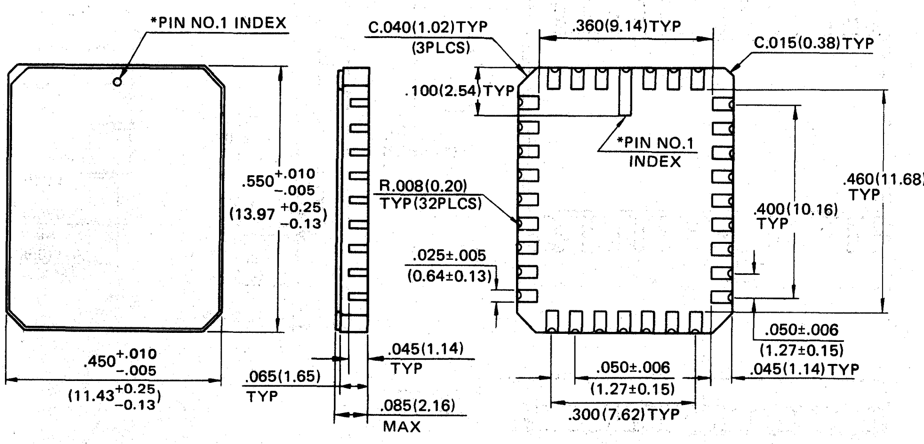
Dimensions in
inches (millimeters)

5

PACKAGE DIMENSIONS

CERAMIC LCC (Suffix: -CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches
(millimeters)

FUJITSU

CMOS 73,728-BIT BI-CMOS STATIC RANDOM ACCESS MEMORY

MB82B79-15 MB82B79-20

TS248-C88X
October 1988

72K-BIT(8192 x 9) Bi-CMOS HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

ADVANCE INFO.

The Fujitsu MB82B79 is a 8,192-words by 9-bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower and high speed, peripheral circuits consist of Bi-CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors.

MB82B79 has 300mil plastic DIP and plastic flat (SOIC) as package option. The memory utilizes asychronous circuitly and requires +5V power supply. All pins are TTL compatible.

The MB82B79 is ideally suited for use in large computer and other applications where fast access time, large -apacity and ease of use are required.
All devices offer the advantages of low power dissipation, low cost high performance.

PLASTIC PACKAGE
DIP-32P-M02

PLASTIC PACKAGE
FPT-32P-M02

- 8,192 words x 9 bits organization
- Fast access time:
  tAA=tACS1=15ns max./tACS2=tOE= 8ns max.(MB82B79-15)
  tAA=tACS1=20ns max./tACS2=tOE=10ns max.(MB82B79-20)
- Bi-CMOS peripheral
- TTL compatible inputs/outputs
- Completely static operation: No clock required
- Three-state output
- Common data input/output
- Single=5V(±10%) power supply with low current drain
  - Active operation = 120mA max.
  - Standby operation = 15 mA max.(CMOS level)
  - Standby operation = 25 mA max.(TTL level)
- Standard 32-pin plastic DIP package : Suffix -P-SK
- Standard 32-pin plastic flat package: Suffix -PF

PIN ASSIGNMENT

(TOP VIEW)

A3	1	32	VCC
A2	2	31	A4
A1	3	30	A5
A0	4	29	A6
A12	5	28	A7
A11	6	27	A8
A10	7	26	A9
NC	8	25	NC
NC	9	24	CS1
OE	10	23	WE
CS2	11	22	I/09
I/01	12	21	I/08
I/02	13	20	I/07
I/03	14	19	I/06
I/04	15	18	I/05
GND	16	17	GNDQ

ABSOLUTE MAXIMUM RATINGS (See Note)

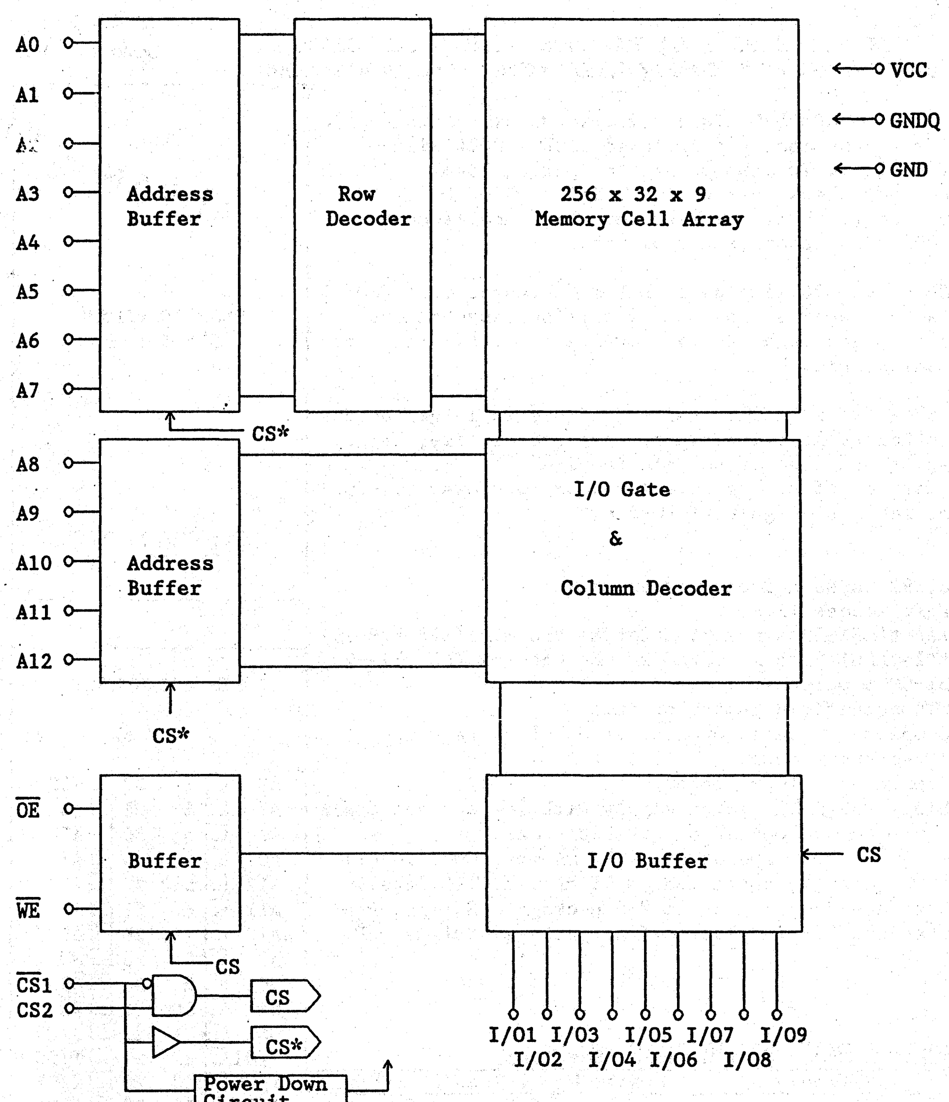
Rating	Symbol	Values	Unit
Supply Voltage	VCC	-0.5 to +7.0	V
Input Voltage	VIN	-3.5 to +7.0	V
Output Voltage	VI/O	-0.5 to +7.0	V
Output Current	IOUT	±20	mA
Power Dissipation	PD	1.0	W
Temperature Under Bias	TBIAS	-10 to +85	°C
Storage Temperature Range	TSTG	-40 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 - MB82B79 BLOCK DIAGRAM



CAPACITANCE(Ta=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			8	pF
Input Capacitance(VIN=0V) (/CS1, CS2, /WE, /OE)	CI1			7	pF
Input Capacitance(VIN=0V) (Other inputs)	CI2			6	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A12	Address input.	$\overline{WE}$	Write Enable.
I/01 to I/09	Data input/output.	VCC	Power Supply(+5V±10%)
$\overline{CS1}$	Chip Select 1.	GND	Ground.
CS2	Chip Select 2.	GNDQ	Ground for output.
$\overline{OE}$	Output Enable.	NC	No Connection.

TRUTH TABLE

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	I/O pin	Power Supply Current
X	H	X	X	Standby	High-Z	Standby
X	L	L	X	Not selected	High-Z	Active
H	L	H	H	Dout disable	High-Z	Active
H	L	H	L	Read	Data out	Active
L	L	H	X	Write	Data in	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

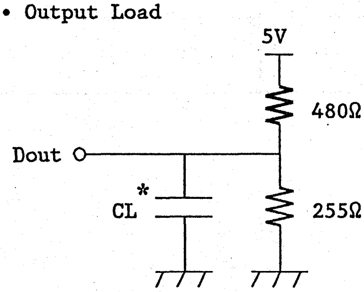
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	VIN=GND to VCC VCC=max.	ILI	-10	10	μA
Output Leakage Current	VI/O=GND to VCC $\overline{\text{CS1}}$=VIH or CS2=VIL or $\overline{\text{WE}}$=VIL or $\overline{\text{OE}}$=VIH	ILI/O	-10	10	μA
Operating Supply Current	$\overline{\text{CS1}}$=VIL, I/O=Open Cycle=min.	ICC		120	mA
Standby Supply Current	VCC=min. to max. $\overline{\text{CS1}}$=VCC-0.2V, VIN≤0.2V or VIN≥VCC-0.2V	ISB1		15	mA
Standby Supply Current	$\overline{\text{CS1}}$=VIH	ISB2		25	mA
Input High Voltage		VIH	2.2	6.0	V
Input Low Voltage		VIL	*1 -0.5	0.8	V
Output High Voltage	IOH=-4mA	VOH	2.4		V
Output Low Voltage	IOL=8mA	VOL		0.4	V
Peak Power-on Current *2	VCC=GND to 4.5V $\overline{\text{CS1}}$=Lower of VCC or VIH min.	IPO		50	mA

Note: *1 -2.0V min. for pulse width less than 20ns.
*2 The $\overline{\text{CS1}}$ input should be connected to VCC to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 3ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: VIL=0.8V, VIH=2.2V
- Output: VOL=0.8V, VOH=2.2V
- Output Load



* Including Scope and jig capacitance

	CL	Parameters measured
Load I	30pF	except tLZ, tHZ, tOW, tOLZ and tOHZ
Load II	5pF	tLZ, tHZ, tOW, tOLZ and tOHZ

AC CHARACTERISTICS

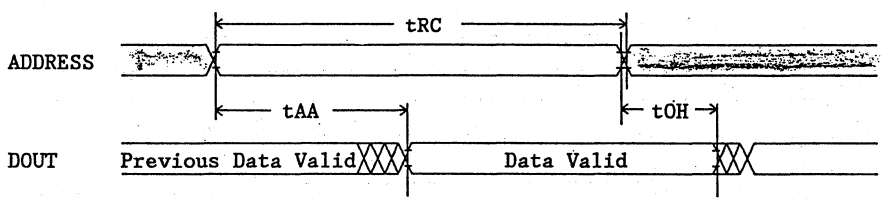
(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

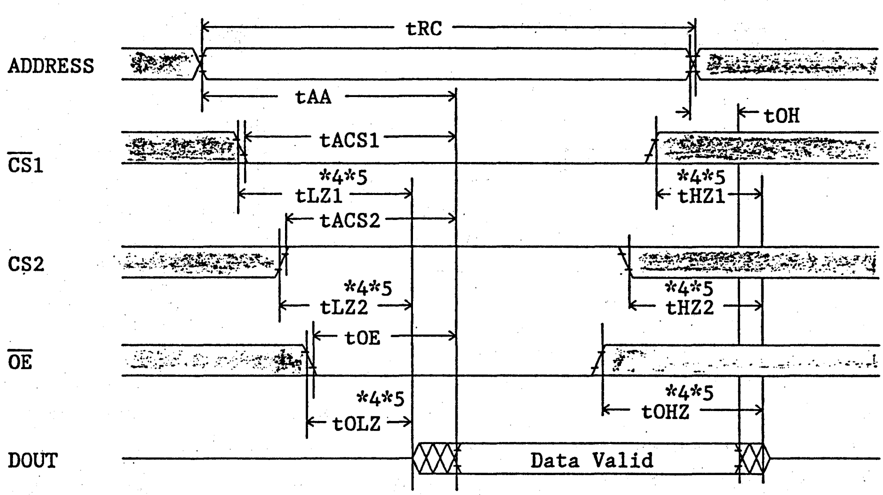
Parameter	Symbol	MB82B79-15		MB82B79-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15		20		ns
Address Access Time *2	tAA		15		20	ns
/CS1 Access Time *3	tACS1		15		20	ns
CS2 Access Time	tACS2		8		10	ns
/OE Access Time	tOE		8		10	ns
Output Hold from Address Change	tOH	3		3		ns
Output Low-Z from /CS1 *4*5	tLZ1	3		3		ns
Output Low-Z from CS2 *4*5	tLZ2	2		2		ns
Output Low-Z from /OE *4*5	tOLZ	2		2		ns
Output High-Z from /CS1 *4*5	tHZ1		8		10	ns
Output High-Z from CS2 *4*5	tHZ2		8		10	ns
Output High-Z from /OE *4*5	tOHZ		8		10	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE I: ADDRESS CONTROLLED *3 ($\overline{CS1}$=$\overline{OE}$="L")



READ CYCLE II: $\overline{CS1}$, CS2 CONTROLLED *4



:Don't care :Undefined

Note: *1 /WE is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE *1

Parameter		Symbol	MB82B79-15		MB82B79-20		Unit
			Min	Max	Min	Max	
Write Cycle Time		tWC	15		20		ns
Address Valid to End of Write		tAW	10		15		ns
/CS1 to End of Write		tCW1	10		15		ns
CS2 to End of Write		tCW2	6		8		ns
Data Setup Time		tDW	7		10		ns
Data Hold Time		tDH	3		3		ns
Write Pulse Width		tWP	8		10		ns
Write Recovery Time *2	/CS1,/WE	tWR1	3		3		ns
	CS2	tWR2	5		5		ns
Address Setup Time	/CS1,/WE	tAS1	0		0		ns
	CS2	tAS2	2		2		ns
Output Low-Z from /WE *3*4		tOW	0		0		ns
Output High-Z from /WE *3*4		tWZ		8		10	ns

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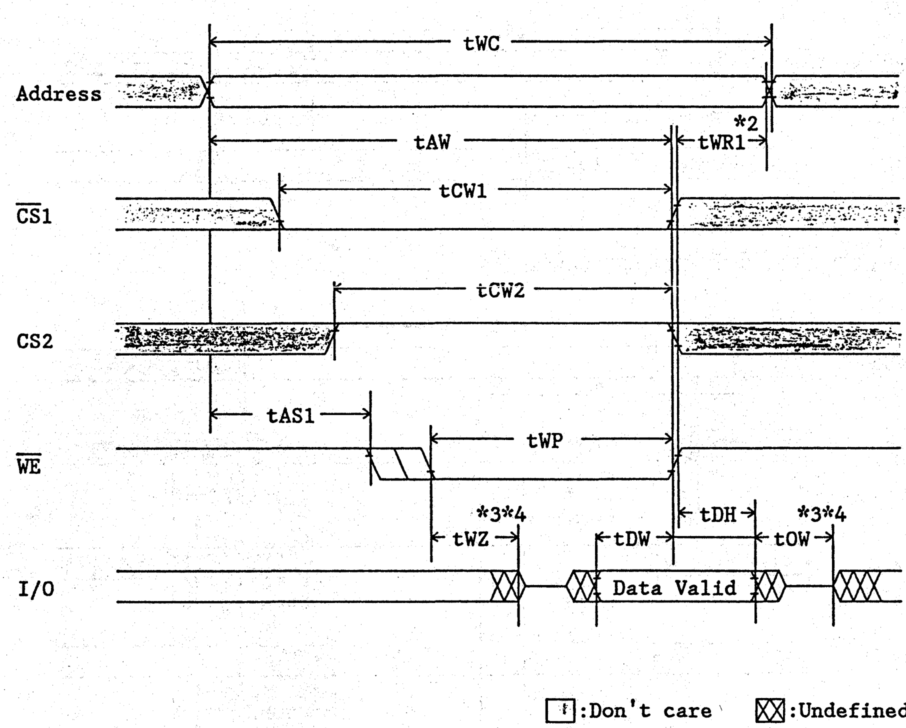
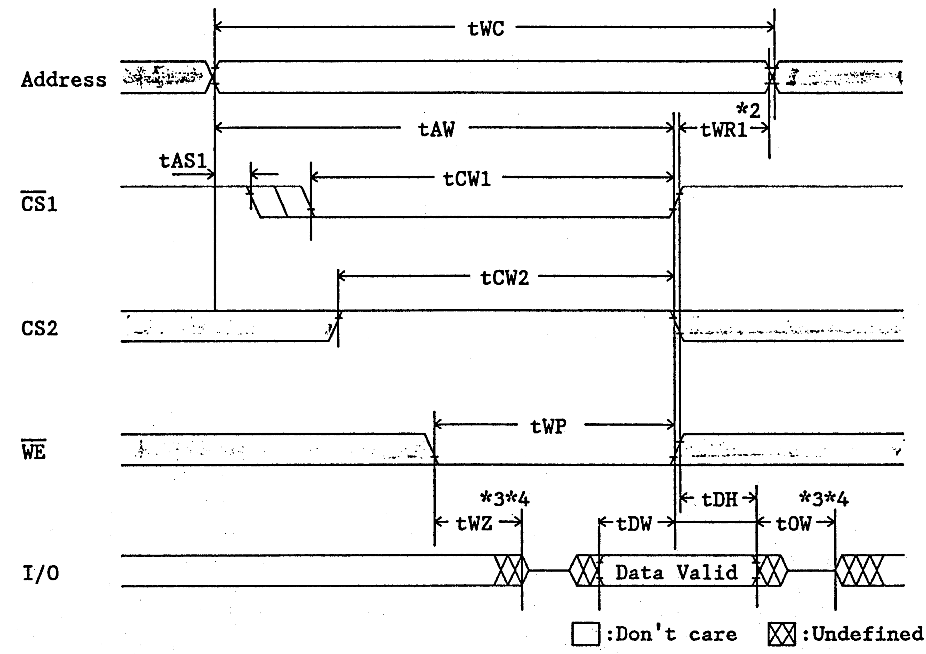
WRITE CYCLE TIMING DIAGRAM *1

WRITE CYCLE I: $\overline{WE}$ CONTROLLED

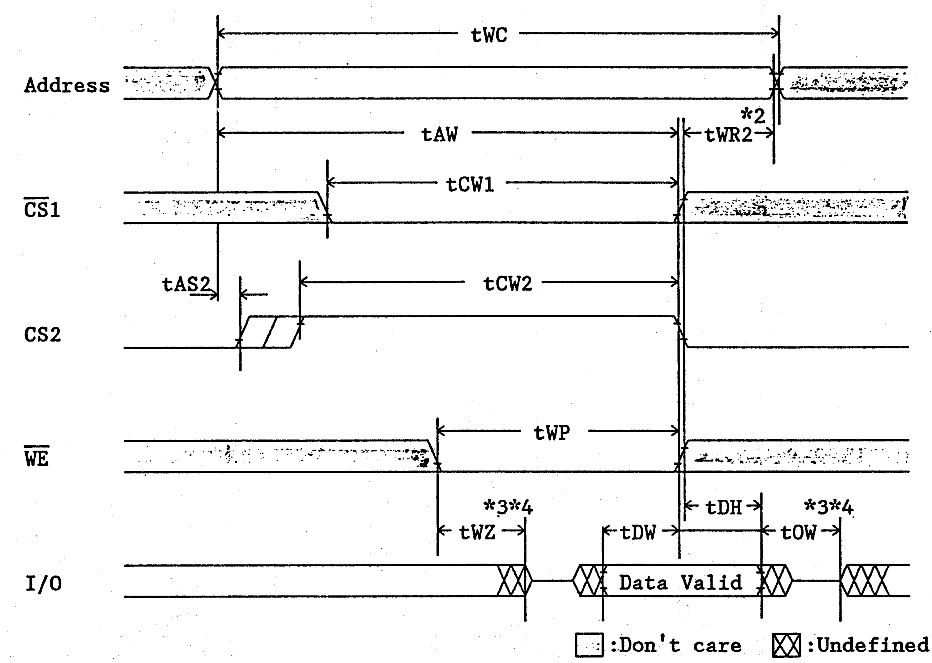


Note: *1 If $\overline{CS1}$, $\overline{OE}$ and CS2 are in the READ Mode during this period, I/O pins are in the out put state so that the input signals of opposite phase to the outputs must not be applied.
*2 tWR is defined from the end point of WRITE Mode.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE II: $\overline{CS1}$ CONTROLLED



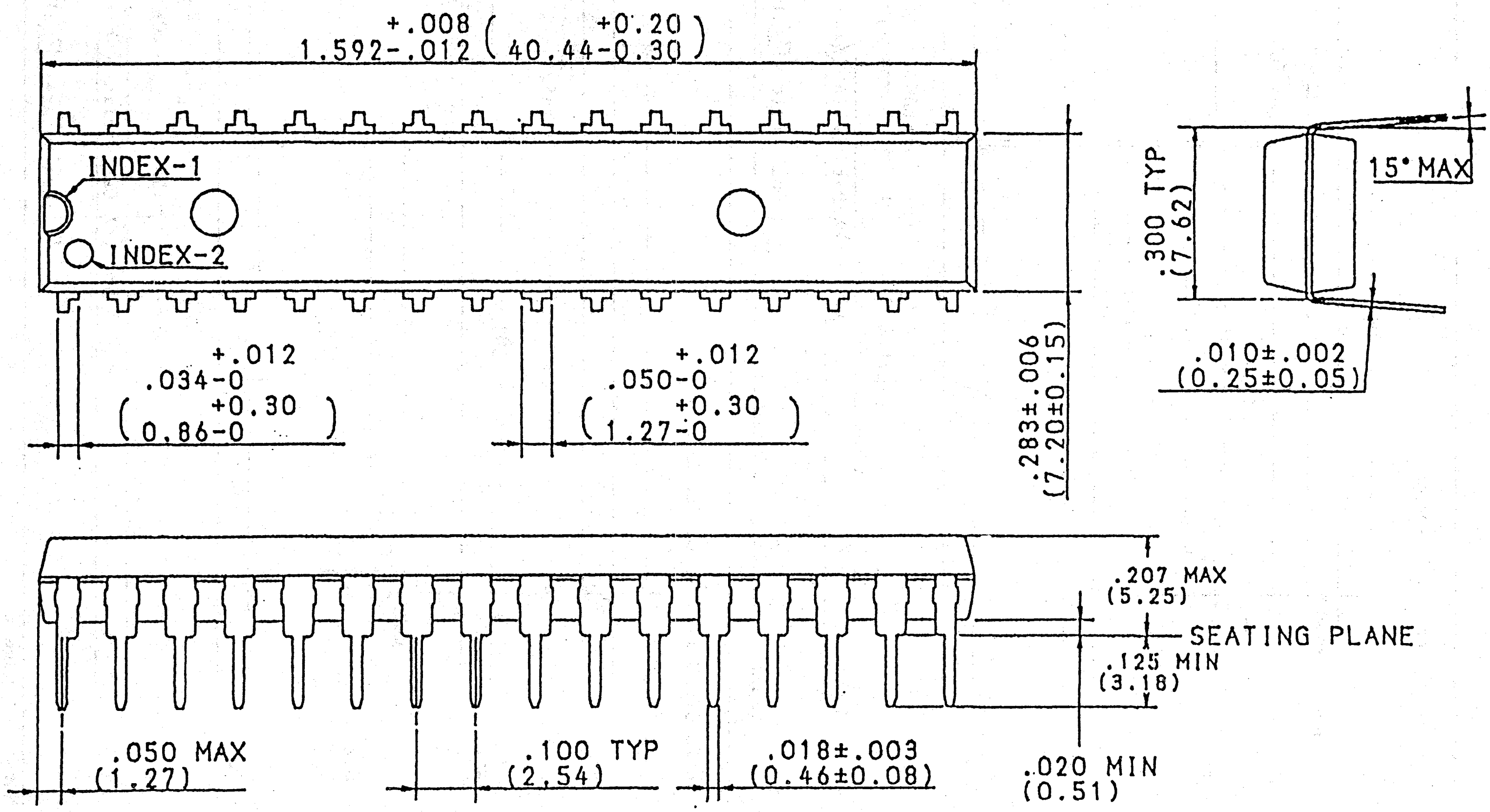
WRITE CYCLE III: $\overline{WE}$ CONTROLLED



Note: See page 6

32 LEAD PLASTIC DUAL-IN-LINE PACKAGE.

(CASE No DIP-32P-M02)
Dimensions in inches(millimeters).

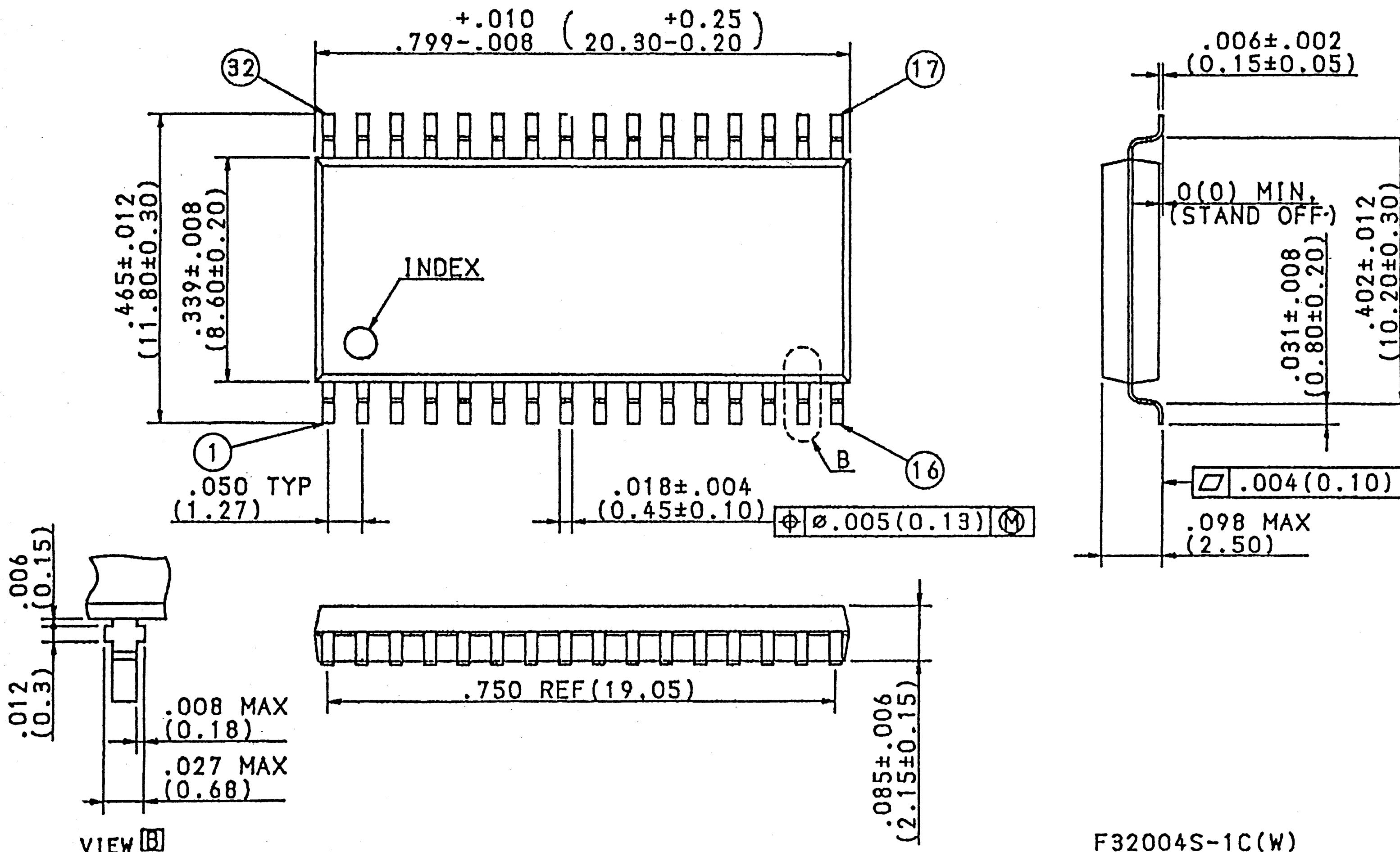


D32009S-1C(W).

FUJITSU LIMITED

32 PINS PLASTIC FLAT PACKAGE.

(CASE No FPT-32P-M02)
Dimensions in inches(millimeters)



F32004S-1C(W)

FUJITSU LIMITED

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FUJITSU

CMOS 262,144 BIT STATIC RANDOM ACCESS MEMORY

MB81C81A-35
MB81C81A-45

May 1988
Edition 1.0

262,144 WORDS x 1 BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY

The Fujitsu MB81C81A is 262,144 words x 1 bit static random access memory fabricated with a CMOS technology.

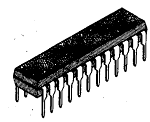
Since MB81C81A consists of NMOS cells and CMOS peripherals, it is packaged in 300 mil DIP and reached low power dissipation such as 550 mW.

It uses fully static circuitry and therefore requires no clocks or refreshing to operate.

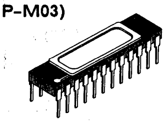
The MB81C81A is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.

MB81C81A is compatible with TTL logic families in all respects; input, output and a single +5 V supply.

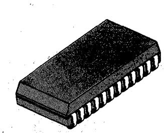
- Organization: 262,144 words x 1 bit
- Static operation: No clocks or refresh required
- Fast access time: 35 ns max. (MB81C81A-35)
  45 ns max. (MB81C81A-45)
- Single +5V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- 300 mil width 24-pin Dual In-Line Package
  (Suffix: Plastic DIP; P-SK, Ceramic DIP; C-SK)
  24 pad LCC (Suffix: CV)
  24 pad SOJ (Suffix: PJ)



PLASTIC PACKAGE
(DIP-24P-M03)



CERAMIC PACKAGE
(DIP-24C-A08)



PLASTIC PACKAGE
(LCC-24P-M01)

LCC-24C-A02, See page 11

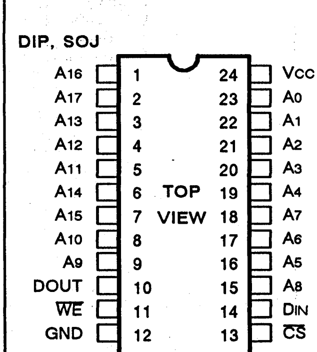
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		VCC	-0.5 to +7	V
Input Voltage on any pin with to GND		VIN	-3.5* to +7	V
Output Voltage on any pin with to GND		VOUT	-0.5 to +7	V
Output Current		IOUT	±20	mA
Power Dissipation		PD	1.0	W
Temperature under Bias		TBIAS	-10 to +85	°C
Storage Temperature	CERAMIC	TSTG	-65 to +150	°C
	PLASTIC		-45 to +125	

* DC: min. = -0.5 V

NOTE:
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

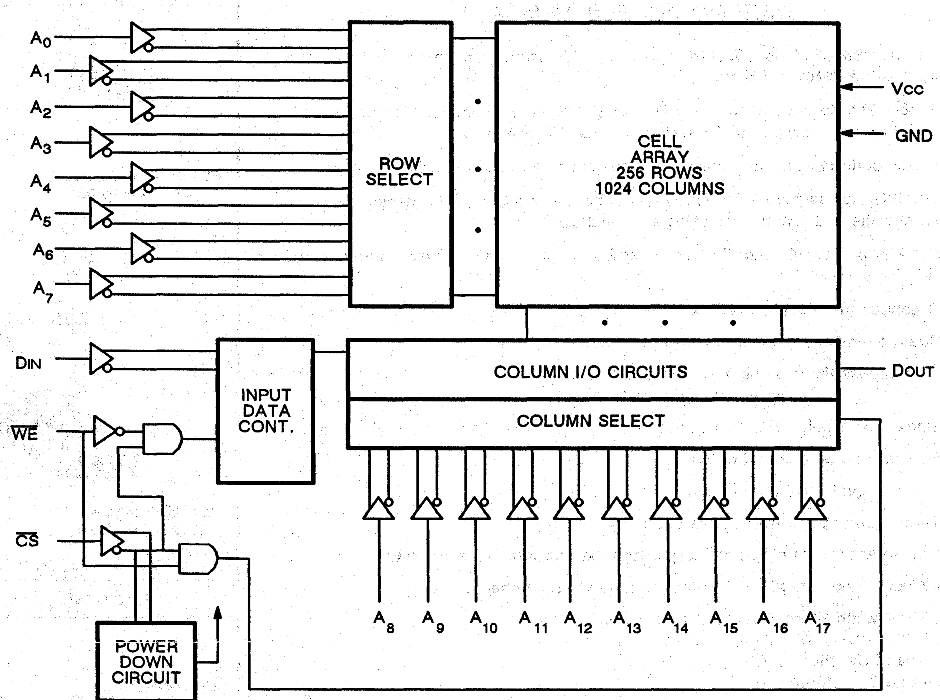
PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 — MB81C81A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	DOUT	Active

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		8	pF
Output Capacitance (VOUT = 0 V)	COUT		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.5*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -3.0 V Min. for pulse width less than 20 ns.

5

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition		Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC} V_{CC} = Max.		I_{LI}	-10		10	µA
Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0 V to 4.5 V V_{CC} = Max.		I_{LO}	-50		50	µA
Power Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA V_{CC} = Max. Cycle = Min.	MB81C81A-45	I_{CC}			100	mA
		MB81C81A-35				120	
Standby Current	$\overline{V_{CC}}$ = Min. to Max. CS ≥ V_{CC} -0.2 V V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} - 0.2 V		I_{SB1}			15	mA
	$\overline{V_{CC}}$ = Min. to Max. CS = V_{IH}		I_{SB2}			30	
Output Low Voltage	I_{OL} = 16 mA		V_{OL}			0.4	V
Output High Voltage	I_{OH} = -4 mA		V_{OH}	2.4			V
Peak Power on Current*1	$\overline{V_{CC}}$ = 0 to V_{CC} Min. CS = Lower of V_{CC} or V_{IH} Min.		I_{PO}			30	mA

*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

5

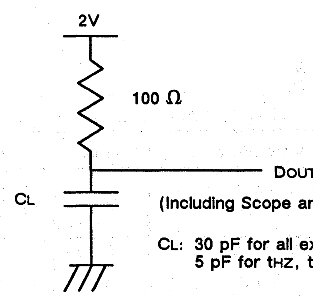
AC TEST CONDITIONS

Input Pulse Levels: 0.6 V to 2.4 V

Input Pulse Rise and Fall Times: 5 ns

Timing Measurement Reference Levels: Input: V_{IL} = 0.8 V/V_{IH} = 2.2 V
Output: V_{OL} = 0.8 V/V_{OH} = 2.2 V

Output Load: Fig. 2



(Including Scope and Jig)

C_L: 30 pF for all except t_{HZ}, t_{WZ}, t_{LZ} and t_{OW}.
5 pF for t_{HZ}, t_{WZ}, t_{LZ} and t_{OW}.

AC CHARACTERISTICS

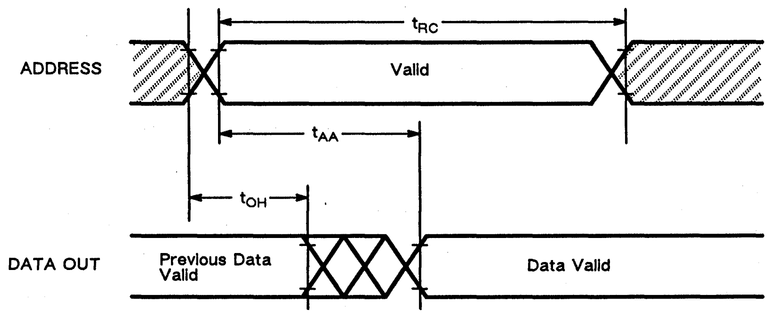
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C81A-35		MB81C81A-45		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
Read Cycle Time *1	t_{RC}	35		45		ns
Address Access Time	t_{AA}		35		45	ns
Chip Select Access Time *2	t_{ACS1}		35		45	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Chip Selection to Output in Low-Z *3	t_{LZ}	5		5		ns
Chip Deselection to Output in High-Z *3	t_{HZ}	0	20	0	25	ns
Chip Selection to Power Up time	t_{PU}	0		0		ns
Chip Deselection to Power Down	t_{PD}		35		45	ns

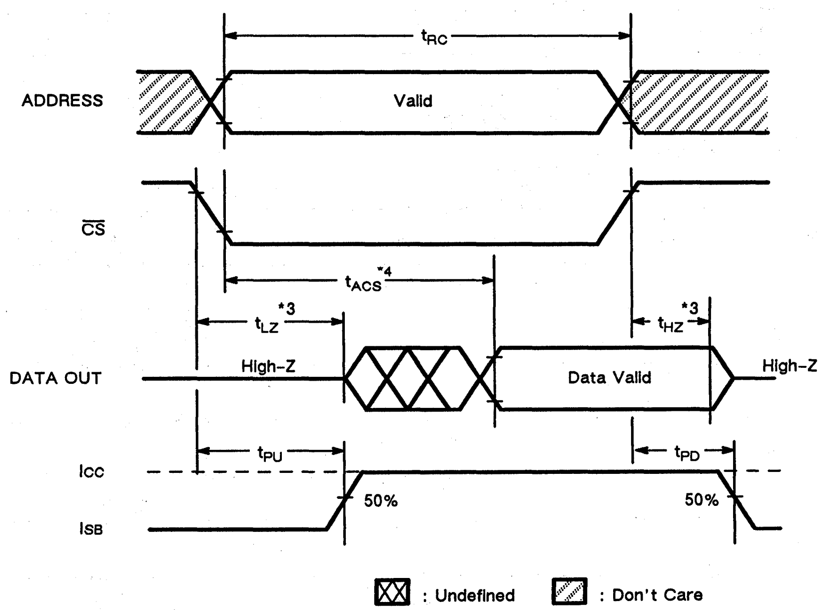
*1 All Read cycles are determined from the last valid address transitioning to the first address transitioning of next cycle.
*2 Addesses valid prior to or coincident with $\overline{CS}$ transition low.
*3 Transition is measured at the point of ±500 mV from steady state voltage with specified load in Figure 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *2



READ CYCLE: $\overline{CS}$ CONTROLLED *2



*1 $\overline{CS}$ is Low.
*2 $\overline{WE}$ is high for Read cycles.
*3 transition is measured at ±500mV from steady state voltage with specified load in Fig. II.
*4 Addresses valid prior to or coincident with $\overline{CS}$ transition low.

5

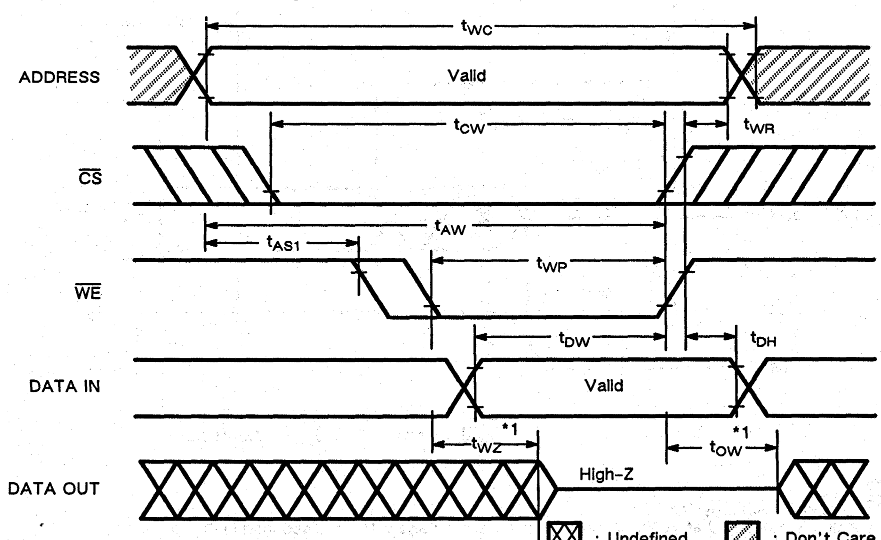
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C81A-35		MB81C81A-45		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
Write Cycle Time	t_{WC}	35		45		ns
Chip Selection to End of Write	t_{CW}	30		40		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS1}	5		5		ns
Address Setup Time	t_{AS2}	0		0		ns
Write Pulse Width	t_{WP}	25		30		ns
Data Valid to End of Write	t_{DW}	20		25		ns
Write Recovery Time	t_{WR}	5		5		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *1	t_{WZ}	0	20	0	25	ns
Output Active from End of Write *1	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM

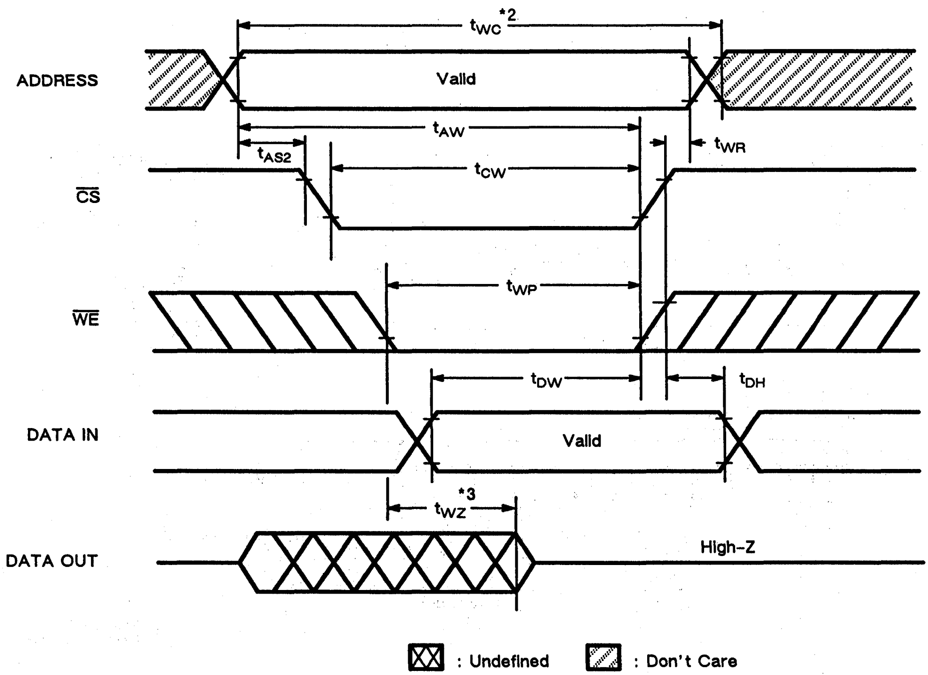
WRITE CYCLE: $\overline{WE}$ CONTROLLED *2



*1 Transition is measured at the point of ±500 mV from steady state voltage.
*2 $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1

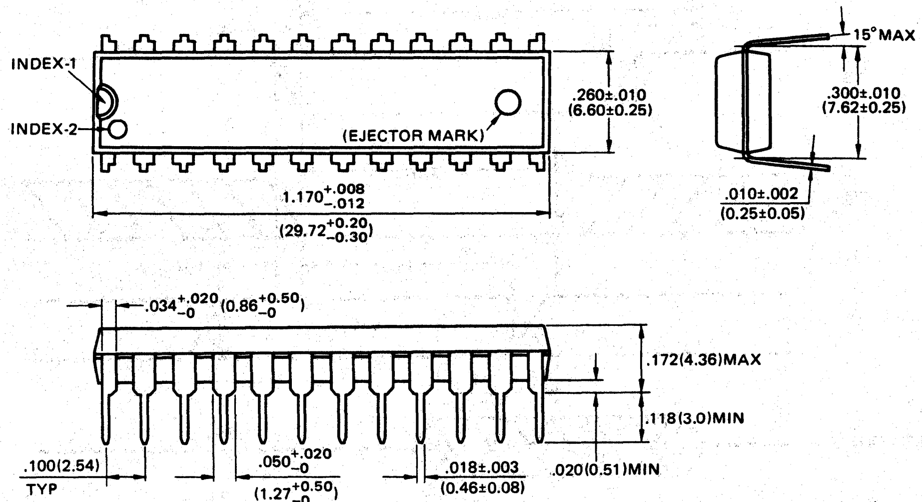


*1 $\overline{CS}$ OR $\overline{WE}$ must be high during address transitions.
*2 All write cycle are determined from last valid address transitioning to the first address transitioning of next cycle.
*3 Transition is measured at ±500mV from steady state voltage with specified load in Fig. II.

5

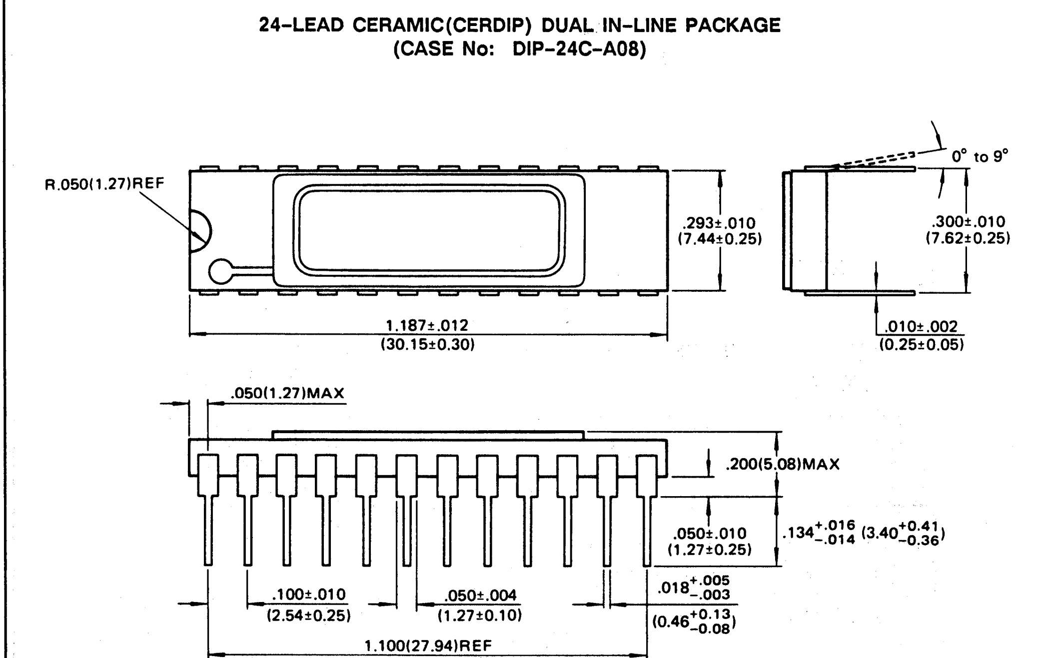
PACKAGE DIMENSIONS

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)



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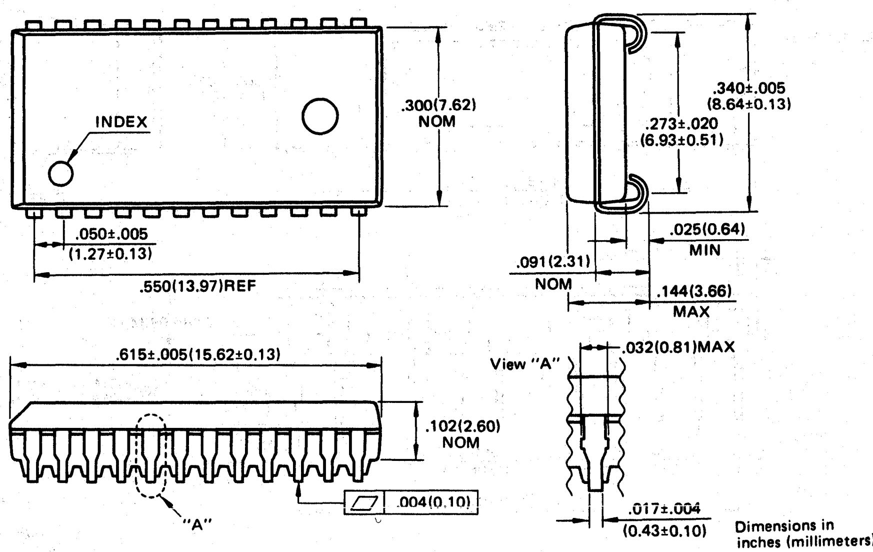
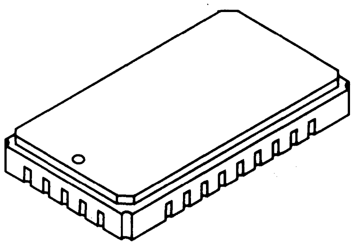
PACKAGE DIMENSIONS (Continued)

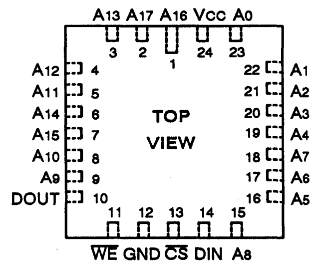
24-LEAD CERAMIC(CERDIP) DUAL IN-LINE PACKAGE
(CASE No: LCC-24P-M01)



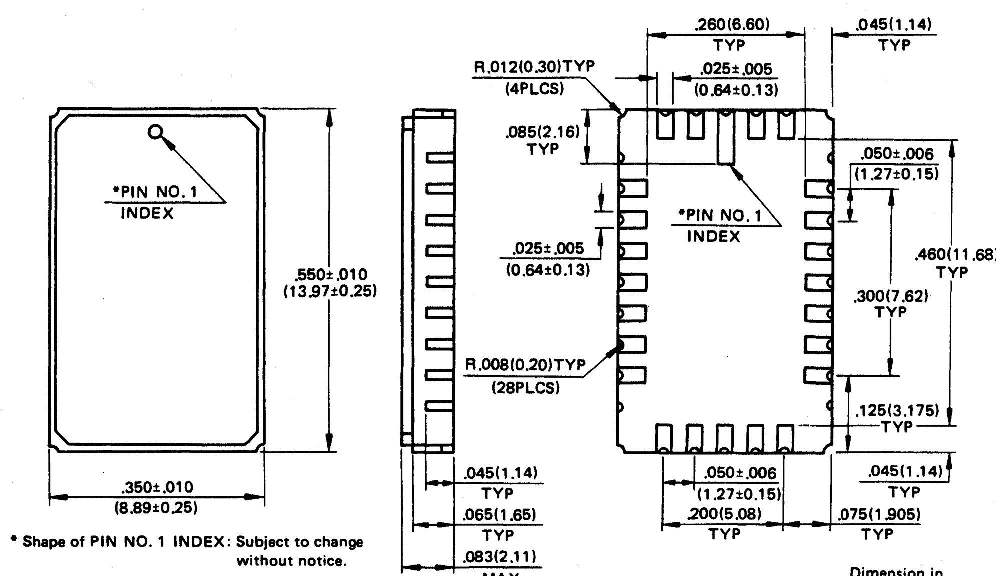
PACKAGE DIMENSIONS (Continued)



CERAMIC PACKAGE
(LCC-24C-A02)



24-LEAD CERAMIC LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

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FUJITSU

CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

MB81C84A-35 MB81C84A-45

April 1988
Edition 2.0

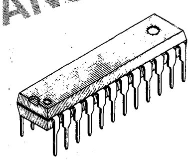
ADVANCE INFO.

64K x 4 BIT(262, 144-BIT) HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

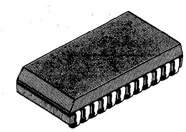
The Fujitsu MB81C84A is a 65,536-words by 4-bits static random access memory fabricated with a CMOS silicon-gate process. To make power dissipation lower, peripheral circuits consist of CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors. MB81C84A has 300mil plastic DIP and 300mil plastic small outline J-lead (SOJ) as package option. The memory utilizes asynchronous circuitly and requires +5V power supply. All pins are TTL compatible.

The MB81C84A is ideally suited for use in large computer systems and other applications where fast access time, large capacity and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 65,536 words x 4 bits
  Fast access time: $t_{AA} = t_{ACS} = 35$ ns max. (MB81C84A-35)
  $t_{AA} = t_{ACS} = 45$ ns max. (MB81C84A-45)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 660 mW max. (Active)
  165 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Standard 24-pin PLASTIC DIP package (300mil) : Suffix -P-SK
- Standard 24-pin PLASTIC SOJ package (300mil) : Suffix -PJ

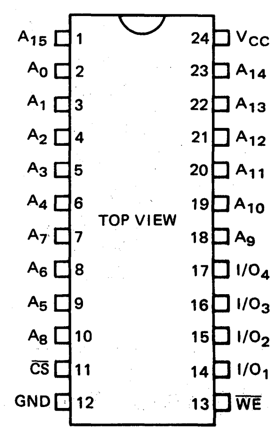


PLASTIC PACKAGE (DIP-24P-M03)



PLASTIC PACKAGE (LCC-24P-M01)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.0 to +7.0	V
Output Voltage	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	-45 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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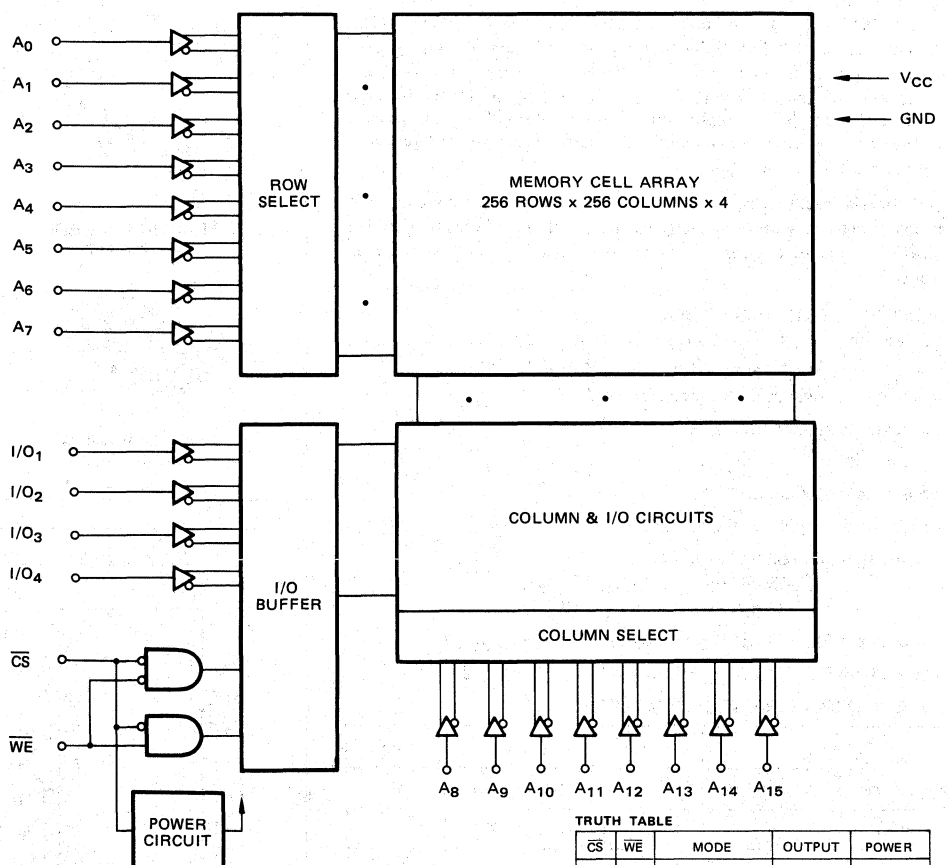
Fig. 1 – MB81C84A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance ($V_{I/O}$ = 0V)	C_{OUT}			8	pF
Input Capacitance ($V_{\overline{CS}}$ = 0V)	$C_{\overline{CS}}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

RECOMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−2.0*1		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

*1 −2.0 V Min. for pulse width less than 20 ns. (V_{IL} min. = −0.5 V at DC level)

DC CHARACTERISTICS

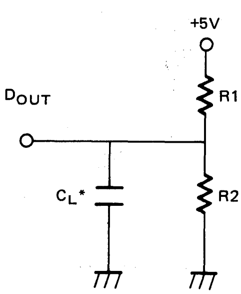
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current	I_{SB1}		30	mA	$\overline{CS}$ = V_{IH}, V_{IN} = GND or V_{CC}
Standby Supply Current	I_{SB2}		15	mA	$\overline{CS} \geq V_{CC}$ −0.2V, V_{IN} = GND or V_{CC}
Operating Supply Current	I_{CC}		120	mA	Cycle = Min., I_{OUT} = 0mA, $\overline{CS}$ = V_{IL}
Input Leakage Current	I_{LI}	−10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	−50	50	μA	$\overline{CS}$ = V_{IH}, V_{OUT} = 0 to V_{CC}
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −4 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 mA

Note: All voltages are referenced to GND

Fig. 2 — AC TEST CONDITIONS

- Output Load



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5 ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
  Output: V_{OL} = 0.8V, V_{OH} = 2.2V

* Including Scope and Jig Capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30 pF	except t_{LZ}, t_{HZ}, t_{WZ}, and t_{OW}
Load II	480Ω	255Ω	5 pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}

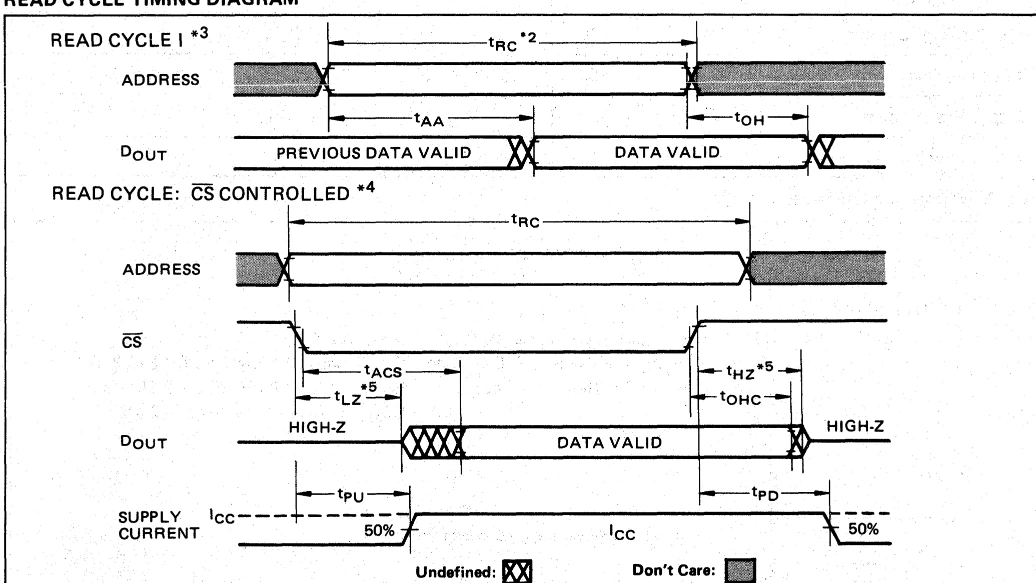
5

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB81C84A-35		MB81C84A-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time	t_{AA}	35	35		45	ns
Chip Selection Access Time	t_{ACS}		35		45	ns
Output Hold from Address Change	t_{OH}	0		0		ns
Output Hold from Chip Selection	t_{OHC}	0		0		ns
Chip Selection to Output Low-Z	t_{LZ}	5		5		ns
Chip Deselection to Output High-Z	t_{HZ}	0	20	0	25	ns
Power Up from Chip Selection	t_{PU}	0		0		ns
Power Down from Chip Selection	t_{PD}		35		35	ns

READ CYCLE TIMING DIAGRAM *1

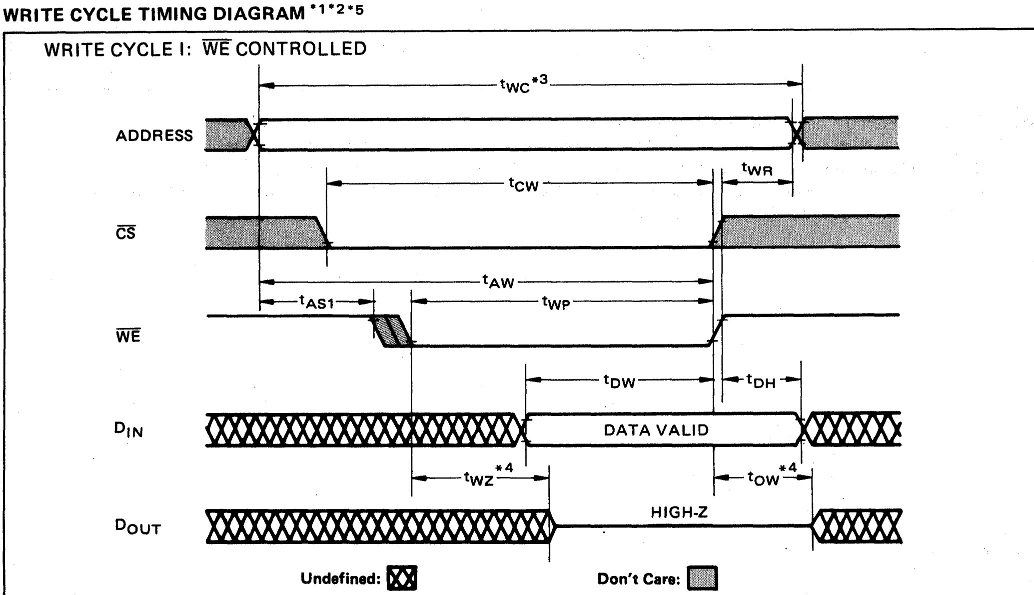


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*3 Device is continously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at ±500mV from steady state voltage with specified load in Fig. 2.

WRITE CYCLE

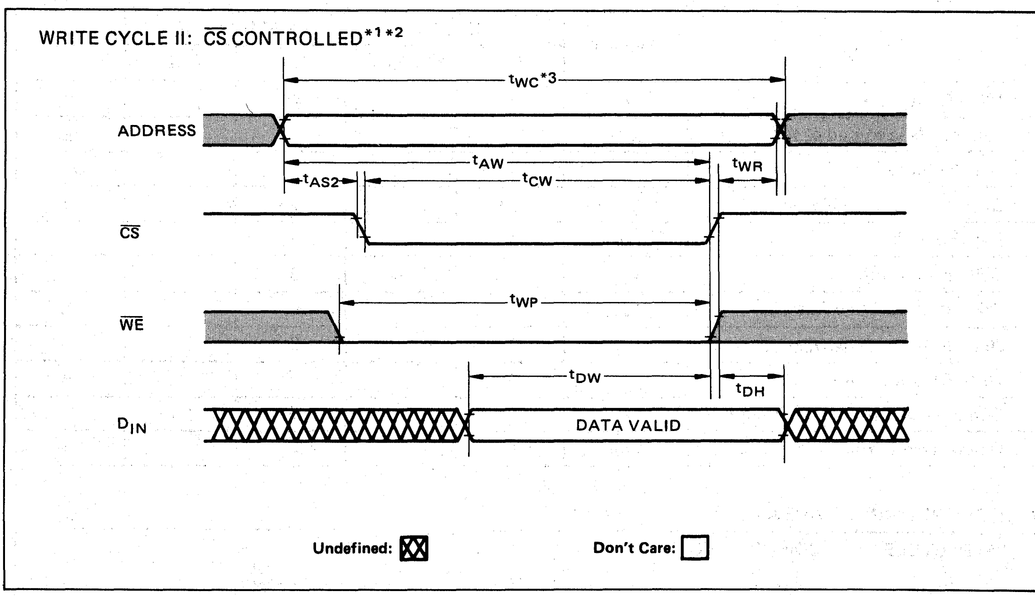
Parameter	Symbol	MB81C84A-35		MB81C84A-45		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	35		45		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Chip Select to End of Write	t_{CW}	30		40		ns
Data Valid to End of Write	t_{DW}	20		25		ns
Data Hold Time	t_{DH}	5		5		ns
Write Pulse Width	t_{WP}	25		35		ns
Address Setup Time from $\overline{WE}$	t_{AS1}	5		5		ns
Address Setup Time from $\overline{CS}$	t_{AS2}	0		0		ns
Write Recovery Time	t_{WR}	5		5		ns
Output High-Z from Write Enable	t_{WZ}	0	20	0	25	ns
Output Low-Z from Write Enable	t_{OW}	5		5		ns

WRITE CYCLE TIMING DIAGRAM *1*2*5



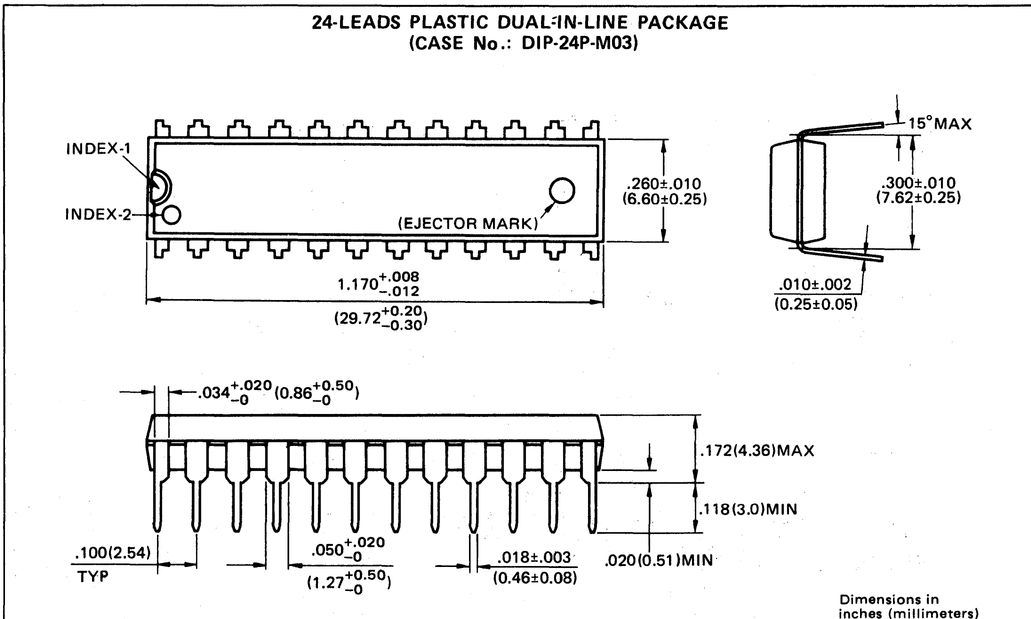
Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load in Fig. 2.
*5 If $\overline{CS}$ is in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

5



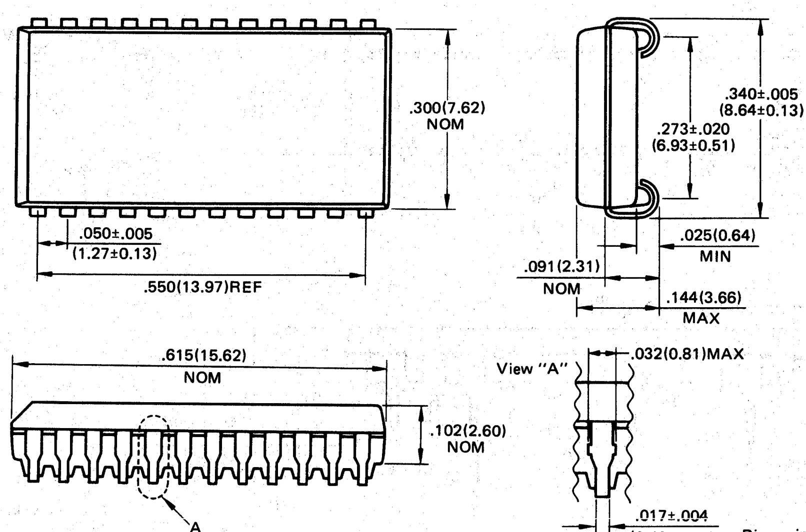
Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle timings are referenced from the last valid address to the first transitioning address.
*4 If $\overline{CS}$ is in the READ mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

PACKAGE DIMENSIONS



PACKAGE DIMENSIONS (continued)

24-LEAD PLASTIC SOJ PACKAGE
(CASE No.: LCC-24P-M01)



Dimensions in inches (millimeters)

FUJITSU

CMOS 262,144-BIT STATIC RANDOM ACCESS MEMORY

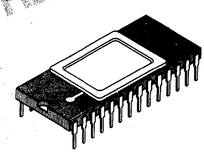
MB 81C86-55
MB 81C86-70

September 1986
Edition 1.0

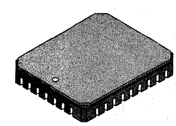
64K x 4 BIT(262,144-BIT) HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB 81C86 is a 65,536-words by 4-bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower, peripheral circuits consist of CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors. The memory utilizes asynchronous and requires single +5V power supply. All pins are TTL compatible.

The MB 81C86 is ideally suited for use in large computer systems and other applications where fast access time, large capacity and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.



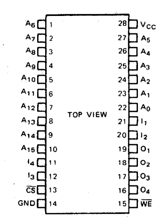
CERAMIC PACKAGE
DIP-28C-A07

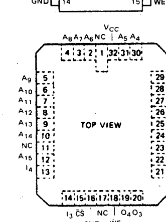


CERAMIC PACKAGE
LCC-32C-A02

- Organization: 65,536 words x 4 bits
- Fast access time: $t_{AA} = t_{ACS}$ = 55 ns max. (MB 81C86-55)
  $t_{AA} = t_{ACS}$ = 70 ns max. (MB 81C86-70)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state output
- Separate data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 550 mW max. (Active)
  55 mW max. (Standby)
- Standard 28-pin DIP: (Suffix: -C)
- Standard 32-pad LCC: (Suffix: -CV)

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–3.0 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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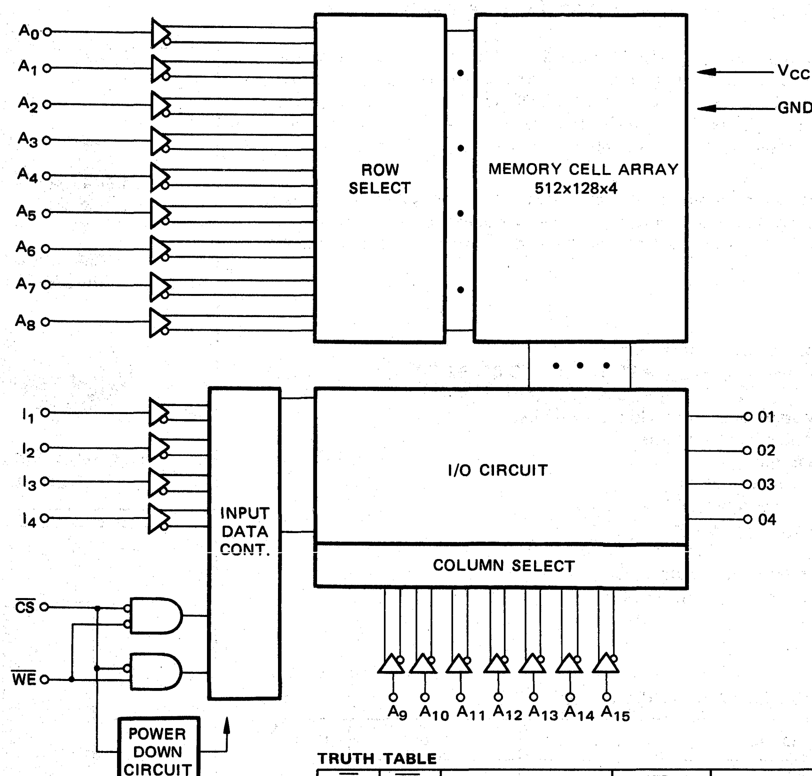
Fig. 1 — MB 81C86 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			8	pF
Input Capacitance ($V_{\overline{CS}}$ = 0V)	$C_{\overline{CS}}$			7	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-3.0*1		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

*1 -3.0 V Min. for pulse width less than 20 ns. (V_{IL} min. = -0.5 V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current	I_{SB}		10	mA	$\overline{CS} = V_{IH}$ V_{IN} = 0 V to V_{CC}
Operating Supply Current	I_{CC}		100	mA	Cycle = Min., I_{OUT} = 0 mA $\overline{CS} = V_{IL}$
Input Leakage Current	I_{LI}	-5	5	μA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-5	5	μA	$\overline{CS} = V_{IH}$ V_{OUT} = 0 V to V_{CC}
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 mA
Peak Power-on Current	I_{PO}		40	mA	V_{CC} = 0V to V_{CC} MAX. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.

Note: All voltages are referenced to GND

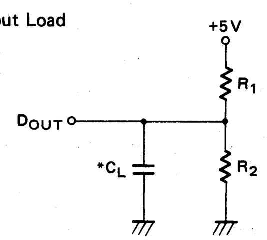
Fig. 2 — AC TEST CONDITIONS

Input Pulse Levels: 0.6V to 2.4V

Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)

Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
Output: V_{OL} = 0.8V, V_{OH} = 2.2V

Output Load



*Including Scope and Jig Capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, and t_{OW}
Load II	480Ω	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}

5

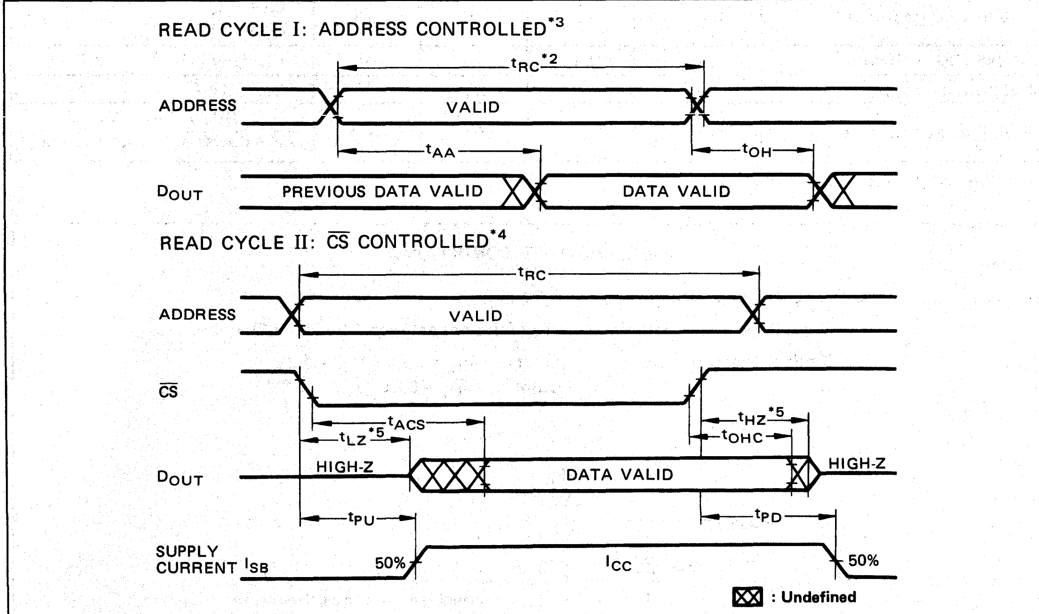
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 81C86-55		MB 81C86-70		Unit
		Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	55		70		ns
Address Access Time*3	t_{AA}		55		70	ns
$\overline{CS}$ Access Time*4	t_{ACS}		55		70	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	5		5		ns
Chip Selection to Output Low-Z *5	t_{LZ}	10		10		ns
Chip Deselection to Output High-Z*5	t_{HZ}	5	25	5	25	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		40		40	ns

READ CYCLE TIMING DIAGRAM*1

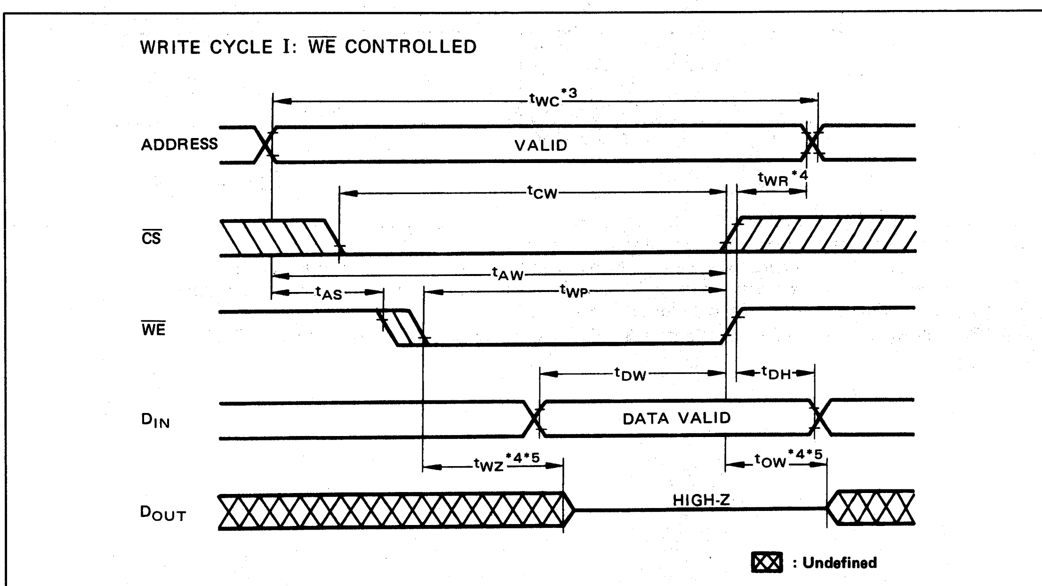


Note:
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified ±500mV from steady state voltage with specified load II in Fig. 2.

WRITE CYCLE*1*2

Parameter	Symbol	MB 81C86-55		MB 81C86-70		Unit
		Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	55		70		ns
Address Valid to End of Write	t_{AW}	45		50		ns
Chip Select to End of Write	t_{CW}	45		50		ns
Data Valid to End of Write	t_{DW}	25		30		ns
Data Hold Time	t_{DH}	5		5		ns
Write Pulse Width	t_{WP}	30		35		ns
Address Setup Time	t_{AS}	5		5		ns
Write Recovery Time*4	t_{WR}	5		5		ns
Output High-Z from $\overline{WE}$*5	t_{WZ}	0	25	0	25	ns
Output Low-Z from $\overline{WE}$*5	t_{OW}	5	30	5	35	ns

WRITE CYCLE TIMING DIAGRAM*1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified ±500mV from steady state voltage with specified load II in Fig. 2.

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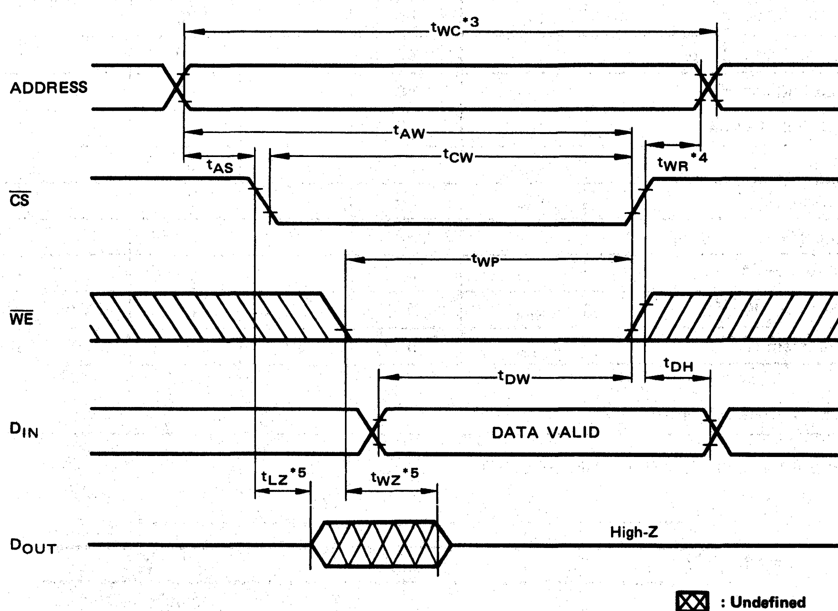
WRITE CYCLE II: $\overline{CS}$ CONTROLLED[*1*2]

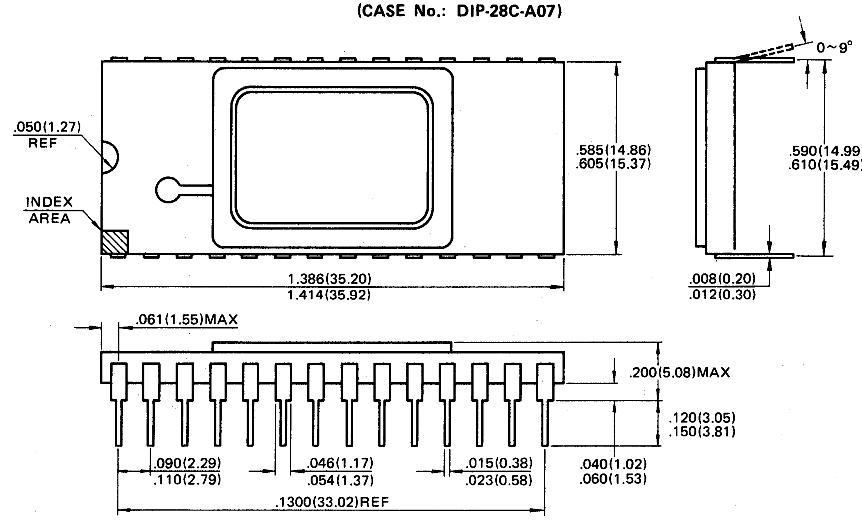


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle timings are referenced from the last valid address to the first transitioning address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified ±500mV from steady state voltage with specified Load II in Fig.2.

PACKAGE DIMENSIONS

(Suffix: -C)

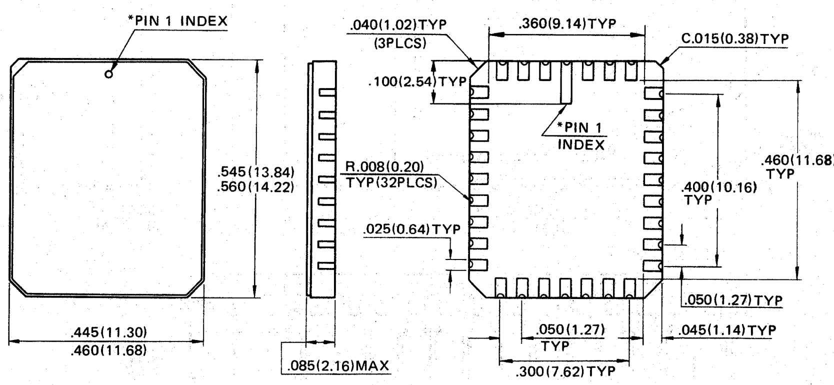
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A07)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS
(Suffix: -CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches
(millimeters)

*Shape of Pin 1 index : Subject to change without notice

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

MB8289-25 MB8289-35

32K x 9-BIT STATIC RANDOM ACCESS MEMORY WITH AUTO MATIC POWER DOWN

TS253-A888
August 1988

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

The Fujitsu MB8289 is 32768 words x 9 bits high speed static random access memory fabricated with CMOS technology.
To obtain smaller chip, cell consists of NMOS transistors and resistors therefore this device is assembled in 300 mil DIP and has such small power dissipation as 550mW max.
All pins are TTL compatible and single 5 volt power supply is required.

A separate chip select ($\overline{CS}_1$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS}_1$ the other deselected packages automatically power down.
All devices offer the advantages of low power dissipation, low cost, and high performance.

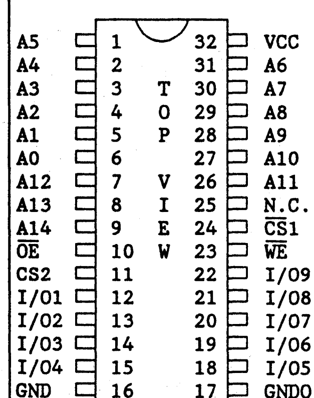
PLASTIC PACKAGE (DIP-32P-M02)

PLASTIC PACKAGE (FPT-32P-M02)

5

- Organization : 32768 words x 9 bits
- Static operation : no clocks or timing strobe required
- Fast access time : $t_{AA}=t_{ACS1}$=25nsmax, t_{ACS2}=14nsmax(MB8289-25)
  $t_{AA}=t_{ACS1}$=35nsmax, t_{ACS2}=15nsmax(MB8289-35)
- Low power consumption : 660mW max. (Operating) for 25ns
  550mW max. (Operating) for 35ns
  138mW max. (TTL Standby)
  83mW max. (CMOS Standby)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 32-pin DIP package(300 mil) : (Suffix: P-SK)
- Standard 32-pin FPT package (450mil) : (Suffix: PF)

PIN ASSIGNMENT



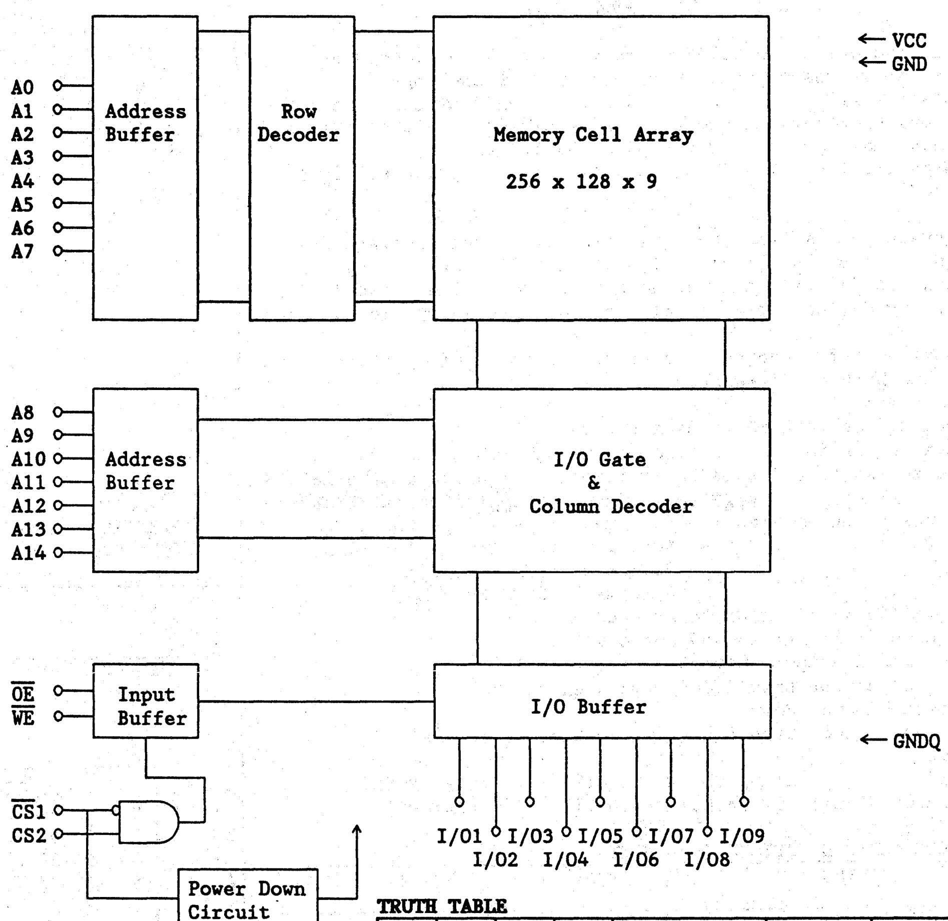
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +7	V
Input Voltage on any pin with respect to GND	VIN	-3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	VOUT	-0.5 to +7	V
Output Current	IOUT	±20	mA
Power dissipation	PD	1.0	W
Temperature Under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-45 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB8289 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O,PE STATE
H	X	X	X	STANDBY	ISB	HIGH-Z
L	L	X	X	DESELECT	ICC	HIGH-Z
L	H	H	H	DOUT DISABLE	ICC	HIHG-Z
L	H	H	L	READ	ICC	DOUT
L	H	L	X	WRITE	ICC	DIN

CAPACITANCE (T_A= 25°C, f= 1MHz)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance (CS1,CS2,OE,WE)	VIN=0V	CI1			8	pF
Input Capacitance (Other Input)	VIN=0V	CI2			7	pF
I/O Capacitance	VI/O=0V	CI/O			8	pF

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0	--	70	°C

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

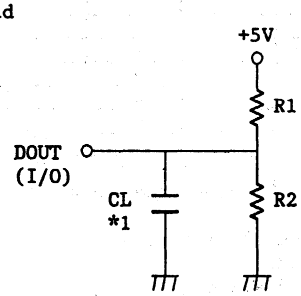
Parameter		Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current		ISB1	--	15	mA	CS1≥VCC-0.2V VIN≥VCC-0.2V or VIN≤0.2V
		ISB2	--	25	mA	VIN≤0.2V /CS1=VIH
Operating Supply Current	25ns	ICC	--	120	mA	IOUT=0mA, CS1=VIL Cycle=Min.
	35ns			100		
Input Leakage Current		ILI	- 5	5	µA	VIN=0V to VCC
Output Leakage Current		ILI/O	- 5	5	µA	$\overline{CS1}$=VIH or CS2=VIL or $\overline{WE}$=VIL or $\overline{OE}$=VIH, VI/O=0 V to VCC
Input Low Voltage *1		VIL	-2.0	0.8	V	
Input High Voltage		VIH	2.2	6.0	V	
Output High Voltage		VOH	2.4	--	V	IOH=-4 mA
Output Low Voltage		VOL	--	0.4	V	IOL=8mA

*1 -2.0 V Min. for pulse width less than 20 ns.(VIL min. =-0.5 V at DC level)
Note : All voltages are referenced to GND.

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise & Fall Times: 3ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input : VIL=0.8V, VIH=2.2V
  Output: VOL=0.8V, VOH=2.2V

- Output Load



*1 Including Scope and Jig Capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30 pF	except tLZ, tHZ, tWZ, tOW, tOLZ and tOHZ
Load II	480Ω	255Ω	5 pF	tLZ, tHZ, tWZ, tOW, tOLZ, and tOHZ

5

AC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted)
READ CYCLE *1

Parameter	Symbol	MB8289-25		MB8289-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	25		35		ns
Address Access Time *2	tAA		25		35	ns
CS1 Access Time *3	tACS1		25		35	ns
CS2 Access Time *3	tACS2		14		15	ns
OE Access Time	tOE		12		14	ns
Output Hold from Address Change	tOH	3		3		ns
Output Active from CS1 *4*5	tLZ1	5		8		ns
Output Active from CS2 *4*5	tLZ2	2		3		ns
Output Active from OE *4*5	tOLZ	2		3		ns
Output Disable from CS1*4*5	tHZ1	1	15	1	15	ns
Output Disable from CS2*4*5	tHZ2	1	15	1	15	ns
Output Disable from OE *4*5	tOHZ	1	15	1	15	ns

Note *1 $\overline{\text{WE}}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{\text{CS1}}$=VIL, CS2=VIH and $\overline{\text{OE}}$=VIL.
*3 Address valid prior to or coincident with $\overline{\text{CS1}}$ transition low, CS2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

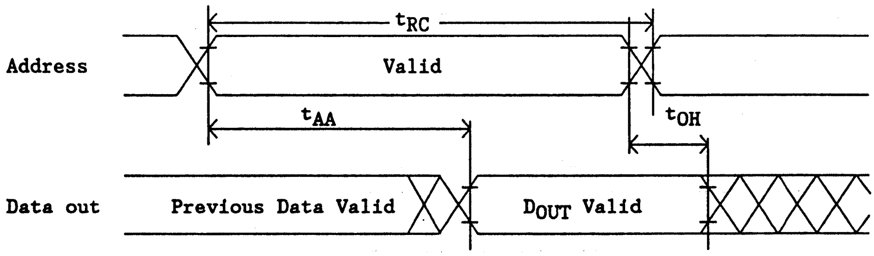
WRITE CYCLE #1

Parameter	Symbol	MB8289-25		MB8289-35		Unit
		Min	Max	Min	Max	
Write Cycle Time #2	tWC	25		35		ns
Address Valid to End of Write	tAW	18		28		ns
CS1 to End of Write	tCW1	16		26		ns
CS2 to End of Write	tCW2	13		20		ns
Data Setup Time	tDW	8		12		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	15		20		ns
Write Recovery Time #3	tWR	0		0		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from WE #4#5	tOW	0		0		ns
Output High-Z from WE #4#5	tWZ	0	8	0	14	ns

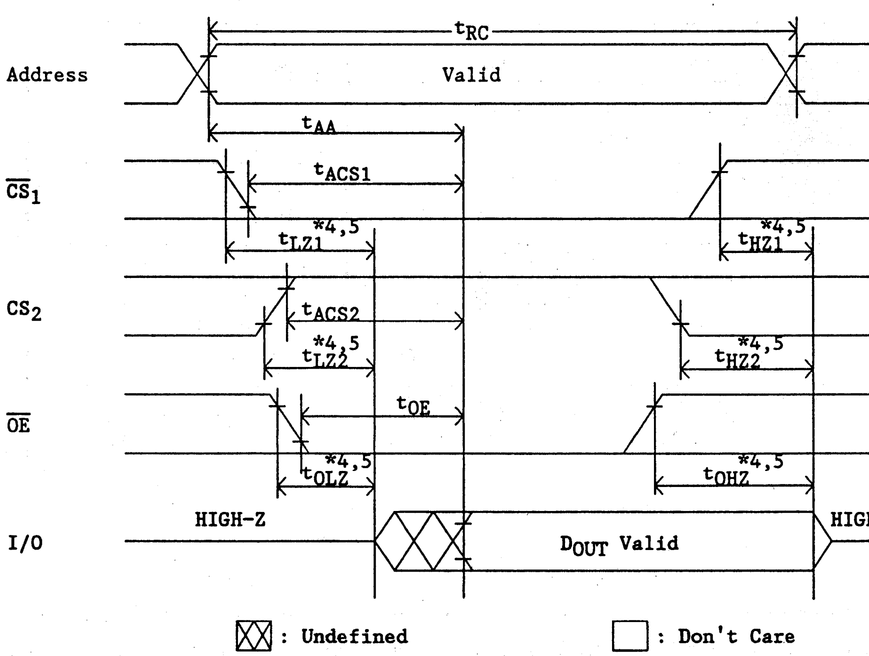
Note #1 If $\overline{\text{CS}}$ goes high simultaneously with $\overline{\text{WE}}$ high, the output remains in high impedance state.
#2 All Write Cycles are determined from the last address transition to the first address transition of next address.
#3 tWR is defined from the end point of Write Mode.
#4 Transition is specified at the point of ±500mV from steady state voltage.
#5 This parameter is specified with Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM *1

READ CYCLE : ADDRESS CONTROLLED *2



READ CYCLE : $\overline{CS}1$, CS2 CONTROLLED *3



Note *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS}1$=VIL, CS2=VIH and $\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}1$ tarnsition low, CS2 transition high.
*4 Transition is specified at the point of ±500mV from stead state voltage.
*5 This parameter is specified with Load II in Fig. 2.

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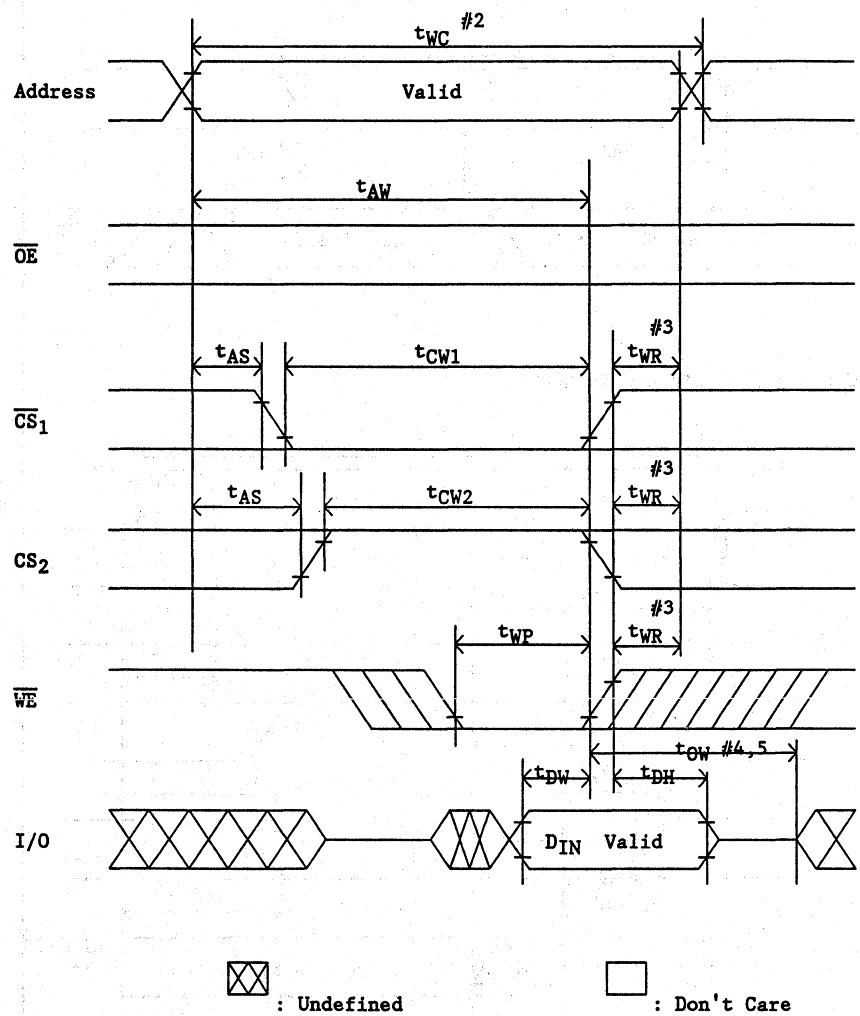
WRITE CYCLE TIMING DIAGRAM #1

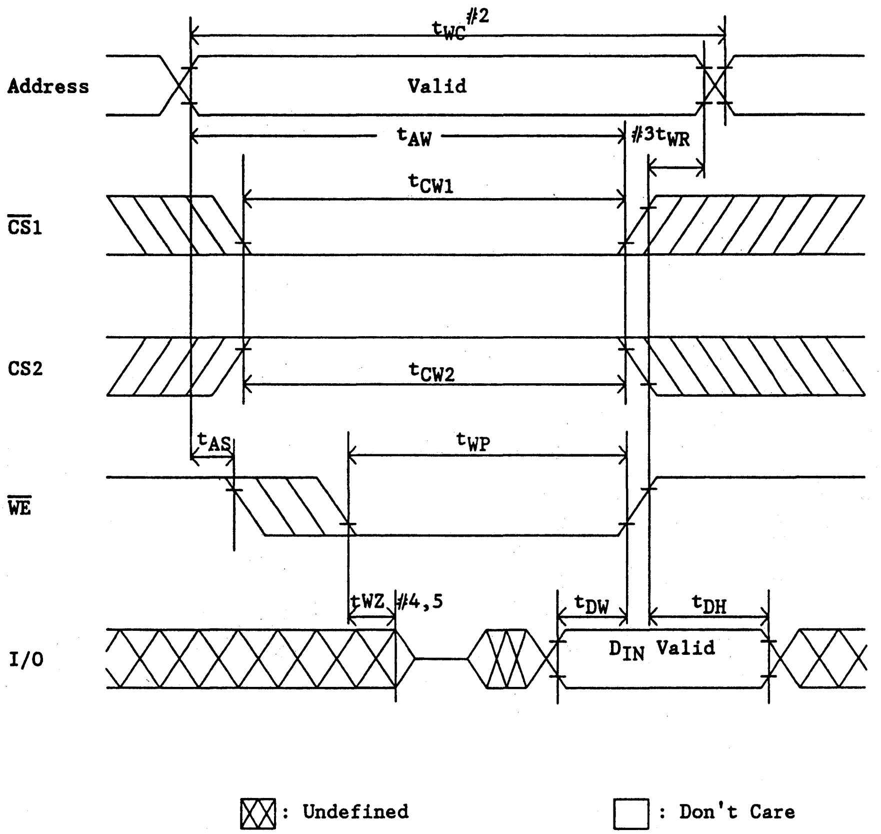
WRITE CYCLE No.1 ($\overline{CS}_1$,CS_2 Controlled)



Note #1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
#2 All Write Cycles are determined from the last address transition to the first address transition of next address.
#3 tWR is defined from the end point of Write Mode.
#4 Transition is specified at the point of $\pm$500mV from steady state voltage.
#5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM #1

WRITE CYCLE No.2 ($\overline{WE}$ Controlled)



Note #1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

#2 All Write Cycles are determined from the last address transition to the first address transition of next address.

#3 tWR is defined from the end point of Write Mode.

#4 Transition is specified at the point of $\pm$500mV from steady state voltage.

#5 This parameter is specified with Load II in Fig. 2.

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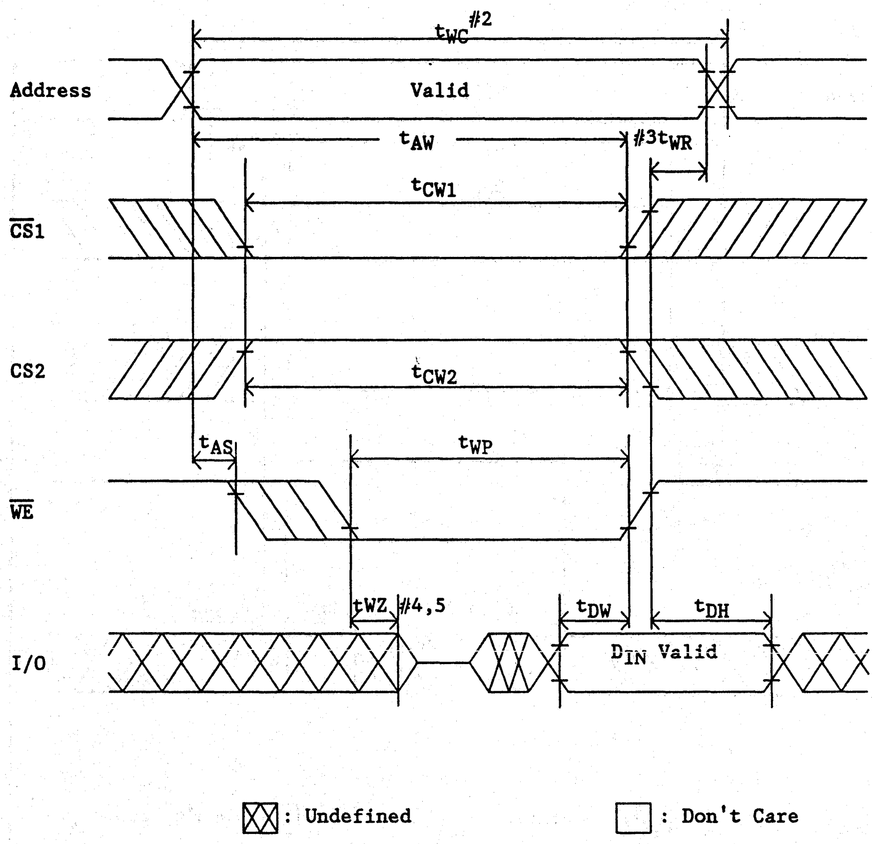
WRITE CYCLE TIMING DIAGRAM #1

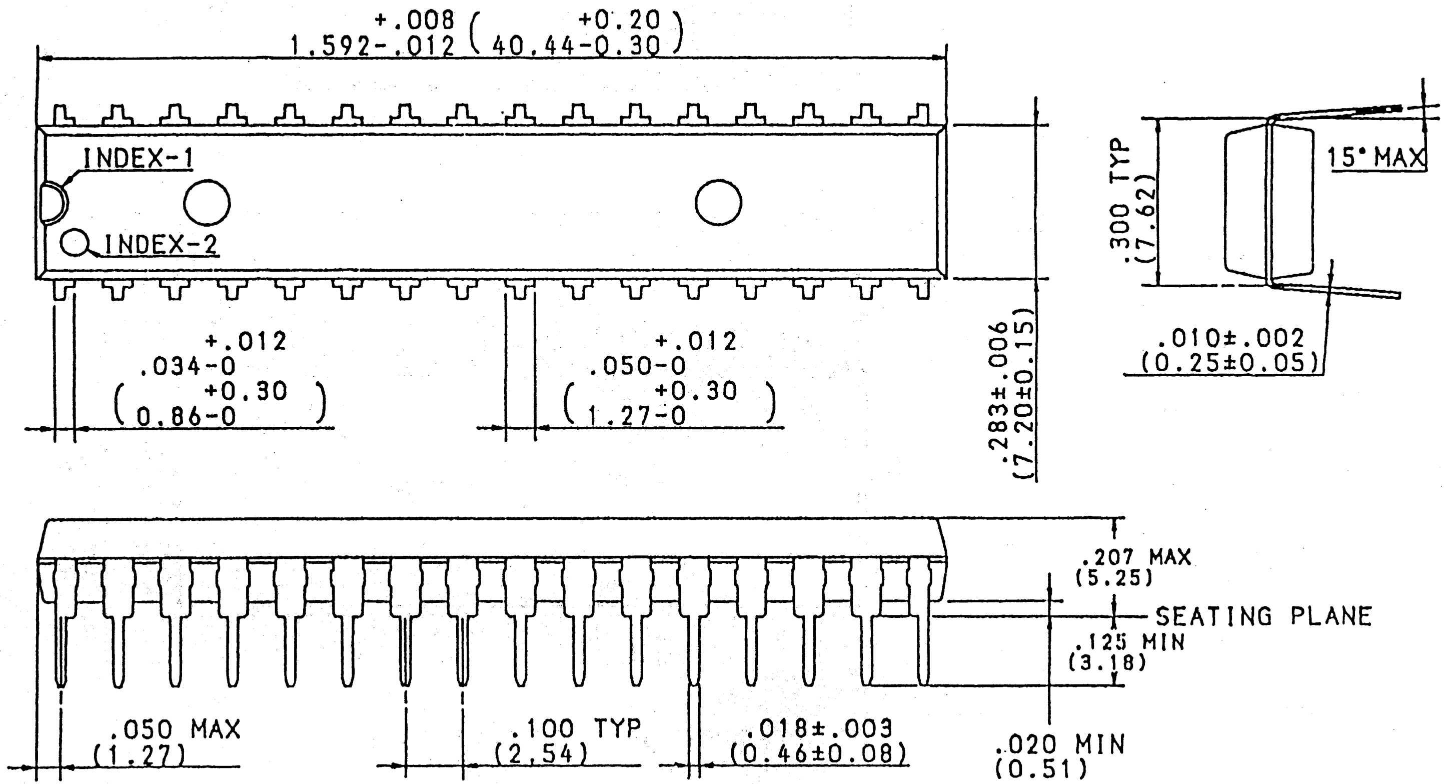
WRITE CYCLE No.2 ($\overline{WE}$ Controlled)



Note #1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
#2 All Write Cycles are determined from the last address transition to the first address transition of next address.
#3 tWR is defined from the end point of Write Mode.
#4 Transition is specified at the point of ±500mV from steady state voltage.
#5 This parameter is specified with Load II in Fig. 2.

32 LEAD PLASTIC DUAL-IN-LINE PACKAGE.

(CASE No DIP-32P-M02)
Dimensions in inches(millimeters).



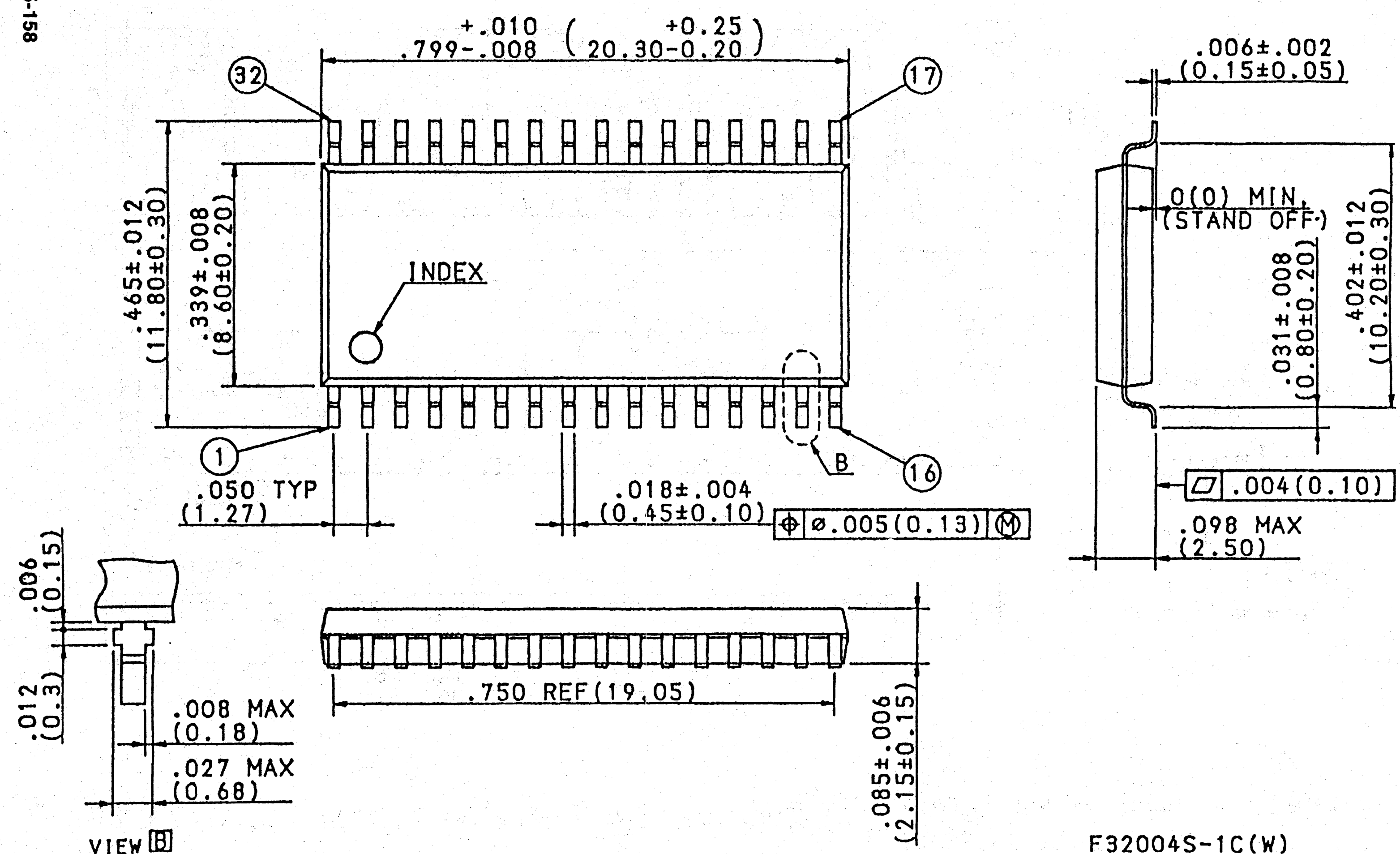
D32009S-1C(W).

FUJITSU LIMITED

(CASE No FF -32P-M02

Dimensions in inches(millimeters

32 PINS PLASTIC FLAT PACKAGE.



F32004S-1C(W)

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Section 6

Low-Power CMOS SRAMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options	Sealing Method
6-3	MB8464A-80	80	65536 bits	28-pin Plastic DIP	Plastic
	MB8464A-80L	80	(8192w x 8b)	28-pin Plastic FPT	Plastic
	MB8464A-80LL	80		32-pad Ceramic LCC	Metal
	MB8464A-10	100			
	MB8464A-10L	100			
	MB8464A-10LL	100			
	MB8464A-15	150			
	MB8464A-15L	150			
	MB8464A-15LL	150			
6-15	MB84256-10L	100	262144 bits	28-pin Plastic DIP	Plastic
	MB84256-10L	100	(32768w x 8b)	28-pin Plastic FPT	Plastic
	MB84256-10LL	100		32-pad Ceramic LCC	Metal
	MB84256-12	120			
	MB84256-12L	120			
	MB84256-12LL	120			
	MB84256-15	150			
	MB84256-15L	150			
	MB84256-15LL	150			
6-25	MB84256A-70	70	262144 bits	28-pin Plastic DIP	Plastic
	MB84256A-70L	70	(32768w x 8b)	28-pin Plastic FPT	Plastic
	MB84256A-70LL	70			
	MB84256A-10	100			
	MB84256A-10L	100			
	MB84256A-10LL	100			
	MB84256A-12	120			
	MB84256A-12L	120			
	MB84256A-12LL	120			
	MB84256A-15	150			
	MB84256A-15L	150			
	MB84256A-15LL	150			
6-35	MB841000-80	80	1048576 bits	32-pin Plastic DIP	Plastic
	MB841000-80L	80	(131072w x 8b)	32-pin Plastic FPT	Plastic
	MB841000-10	100			
	MB841000-10L	100			
6-37	MB84F256-25	250	262144 bits	28-pin Plastic DIP	Plastic
			(32768w x 8b)	28-pin Plastic FPT	Plastic

6

6

FUJITSU

CMOS 65536-BIT STATIC RANDOM ACCESS MEMORY

MB 8464A-80/80L/80LL
MB 8464A-10/10L/10LL
MB 8464A-15/15L/15LL

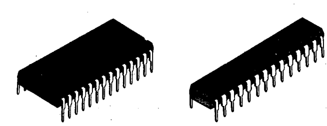
March 1987
Edition 2.0

8,192 WORDS x 8 BIT CMOS STATIC RAM WITH LOW POWER AND DATA RETENTION

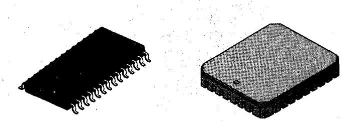
The Fujitsu MB 8464A is a 8192-word by 8-bit static random access memory fabricated with a CMOS sillicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volts power supply is required.

The MB 8464A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

- Organization: 8192 words x 8 bits
- Fast access time: 80 ns max. (MB 8464A-80/80L/80LL)
  100 ns max. (MB 8464A-10/10L/10LL)
  150 ns max. (MB 8464A-15/15L/15LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 11mW max. (MB 8464A-80/10/15)
  0.55mW max. (MB 8464A-80L/10L/15L)
  0.55mW max. (MB 8464A-80LL/10LL/15LL)
- Data retention current: 1mA max. (MB 8464A-80/10/15)
  25μA max. (MB 8464A-80L/10L/15L)
  2μA max. at 0°C to 40°C (MB 8464A-80LL/10LL/15LL)
- Data retention: 2.0V min.
- Standard 28-pin DIP (300mil width) (Suffix: P-SK)
  (600mil width) (Suffix: P)
- Standard 28-pin bend-type Flat package (450mil width) (Suffix: PF)
- Standard 32-pad LCC (Suffix: CV)

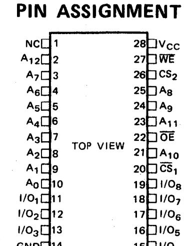


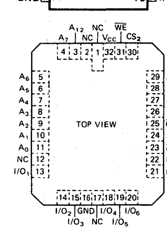
PLASTIC PACKAGE DIP-28P-M02   PLASTIC PACKAGE DIP-28P-M04



PLASTIC PACKAGE FPT-28P-M02   CERAMIC PACKAGE LCC-32C-A02

PIN ASSIGNMENT





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage		V_{IN}	-0.5* to V_{CC}+0.5	V
Output Voltage		V_{OUT}	-0.5 to V_{CC}+0.5	V
Temperature Under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature Range	CERAMIC	T_{STG}	-65 to +150	°C
	PLASTIC		-45 to +125	

*-2.0V for pulse width less than 20ns.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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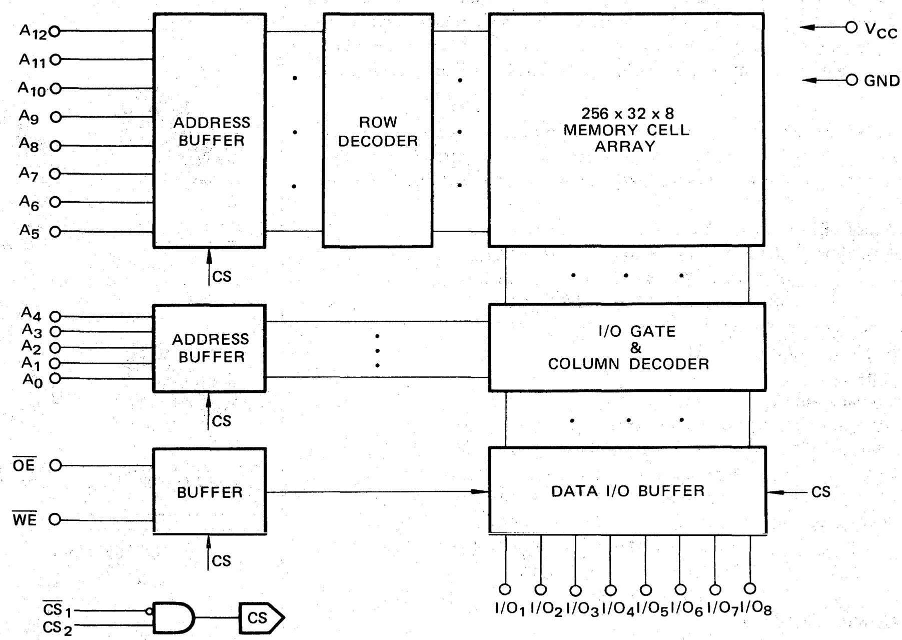
Fig. 1 – MB 8464A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I_{SB}	HIGH-Z
X	L	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	L	H	READ	I_{CC}	D_{OUT}
L	H	X	L	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

*-2.0 V Min for pulse width less than 20 ns. (V_{IL} Min. = −0.3 V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB 8464A-80/10/15		MB 8464A-80L/80LL 10L/10LL/15L/15LL			Unit	Test Condition
		Min	Max	Min	Typ	Max		
Standby Supply Current	I_{SB1}		2		1μA	0.1	mA	$CS_2 \leq 0.2V$, $\overline{CS_1} \geq V_{CC}-0.2V$ ($CS_2 \leq 0.2V$ or $CS_2 \geq V_{CC}-0.2V$)
	I_{SB2}		3			3	mA	$\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$
Active Supply Current	I_{CC1}		50			50	mA	$\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = 0mA$
Operating Supply Current	I_{CC2}		60			60	mA	Cycle = Min., Duty = 100% $I_{OUT} = 0mA$
Input Leakage Current	I_{LI}	−1	1	−1		−1	μA	$V_{IN} = 0V$ to V_{CC}
Output Leakage Current	$I_{LI/O}$	−2	2	−2		2	μA	$V_{I/O} = 0V$ to V_{CC} $\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Output High Voltage	V_{OH}	2.4		2.4			V	$I_{OH} = -1.0mA$
Output Low Voltage	V_{OL}		0.4			0.4	V	$I_{OL} = 2.1mA$

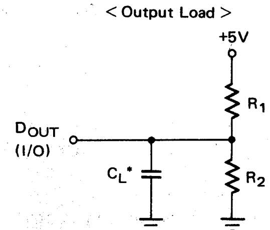
Note: All voltages are referenced to GND

Fig. 2 — AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise and Fall Times: 5ns (Transient Time between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
  Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load:

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100 pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8KΩ	990Ω	5 pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

< Output Load >



*Including jig and stray capacitance

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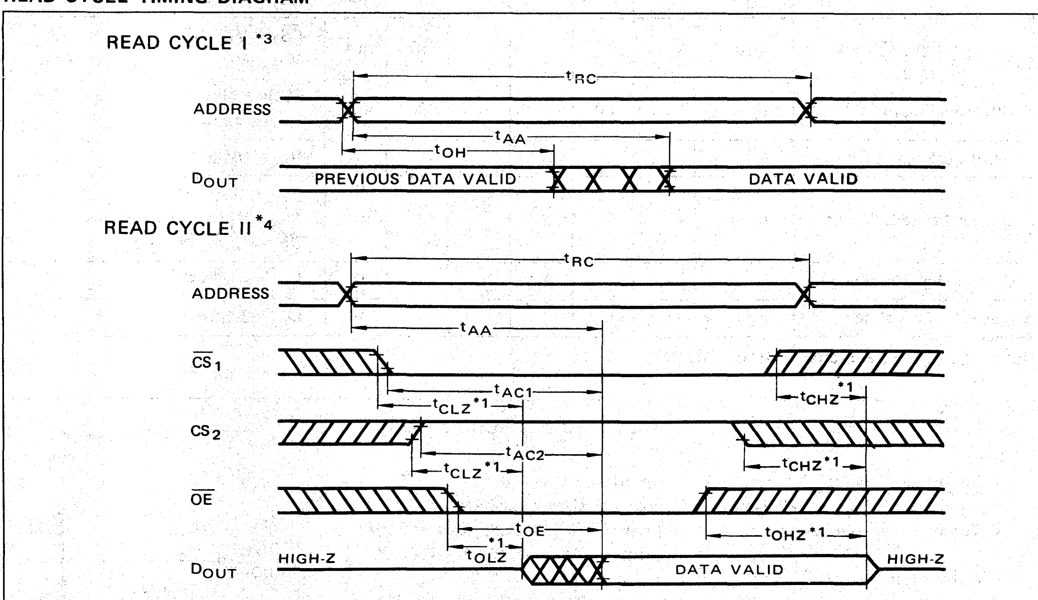
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE

Parameter	Symbol	MB 8464A-80/80L/80LL		MB 8464A-10/10L/10LL		MB 8464A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80		100		150		ns
Address Access Time	t_{AA}		80		100		150	ns
$\overline{CS}_1$ Access Time	t_{AC1}		80		100		150	ns
CS_2 Access Time	t_{AC2}		80		100		150	ns
Output Enable to Output Valid	t_{OE}		35		45		55	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Select to Output Low-Z *1	t_{CLZ}	10		10		10		ns
Output Enable to Output Low-Z *1	t_{OLZ}	5		5		5		ns
Chip Select to Output High-Z *1	t_{CHZ}		35		35		40	ns
Output Enable to Output High-Z *1	t_{OHZ}		30		35		40	ns

READ CYCLE TIMING DIAGRAM *2



Note: *1 Transition is measured at the point of ±500mV from steady state voltage.
*2 $\overline{WE}$ is high for Read Cycle.
*3 Device is continuously selected, $\overline{CS}_1 = \overline{OE} = V_{IL}$, $CS_2 = V_{IH}$.
*4 Address vaild prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.

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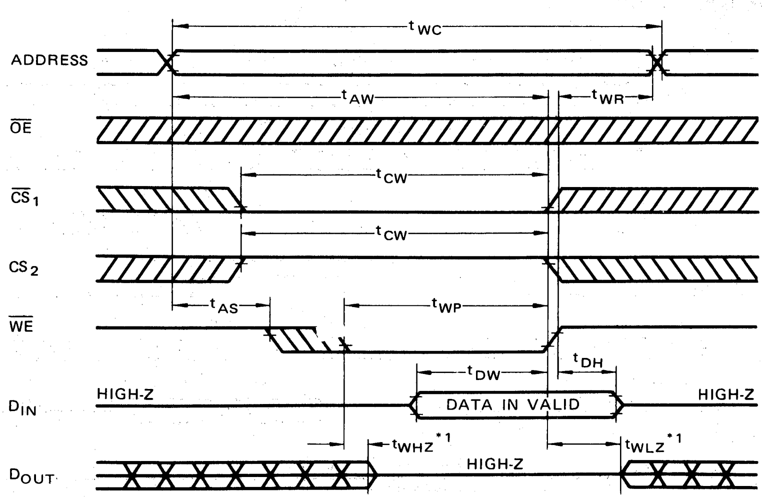
WRITE CYCLE

Parameter	Symbol	MB 8464A-80/80L/80LL		MB 8464A-10/10L/10LL		MB 8464A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	80		100		150		ns
Address Valid to End of Write	t_{AW}	60		80		100		ns
Chip Select to End of Write	t_{CW}	60		80		100		ns
Data Valid to End of Write	t_{DW}	30		35		40		ns
Data Hold Time	t_{DH}	5		5		5		ns
Write Pulse Width	t_{WP}	60		70		90		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time	t_{WR}	10		10		10		ns
Write Enable to Output Low-Z*1	t_{WLZ}	5		5		5		ns
Write Enable to Output High-Z*1	t_{WHZ}		30		35		40	ns

WRITE CYCLE TIMING DIAGRAM *2



Note: *1 Transition is measured at the point of ±500mV from steady state voltage.
*2 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

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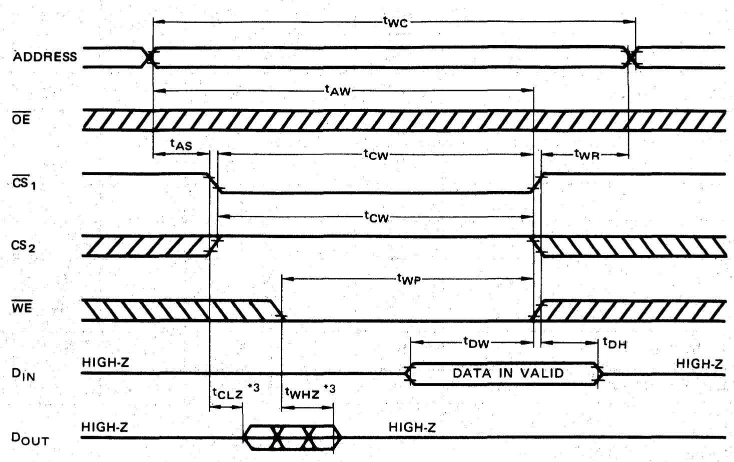
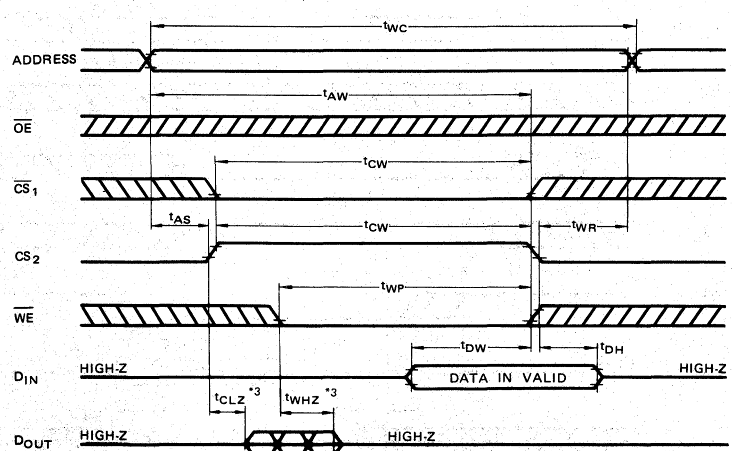
WRITE CYCLE II: $\overline{CS_1}$ CONTROLLED*1



WRITE CYCLE III: CS_2 CONTROLLED*2



Note: *1 If $\overline{OE}$, CS_2 and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{OE}$, $\overline{CS_1}$ and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3 Transition is measured at the point of ± 500mV from steady state voltage.

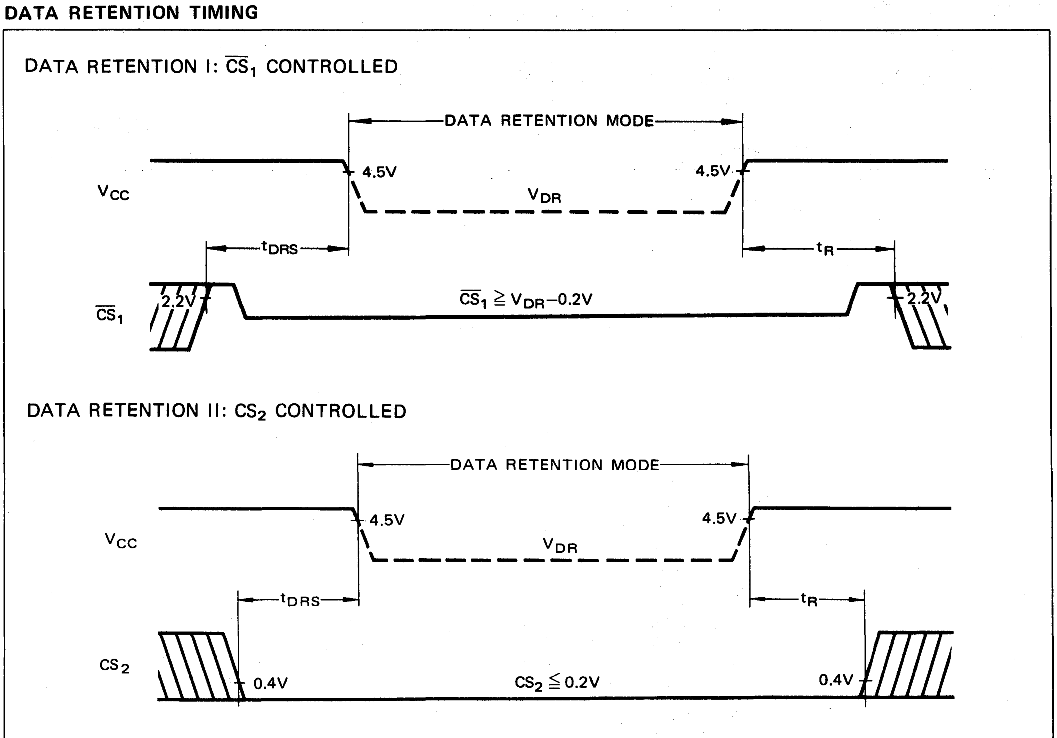
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current*2	Standard	I_{DR}			1.0	mA
	L-Version			1.0	25	μA
	LL-Version*3			1.0	2.0	μA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *2 CS_2 controlled: V_{DR} = 3.0V, $CS_2 \leqq 0.2V$
$\overline{CS}_1$ controlled: V_{DR} = 3.0V, $\overline{CS}_1 \geqq V_{DR}-0.2V$ ($CS_2 \leqq 0.2V$ or $CS_2 \geqq V_{DR}-0.2V$)
*3 V_{DR}=3.0V, T_A=0°C to 40°C

DATA RETENTION TIMING



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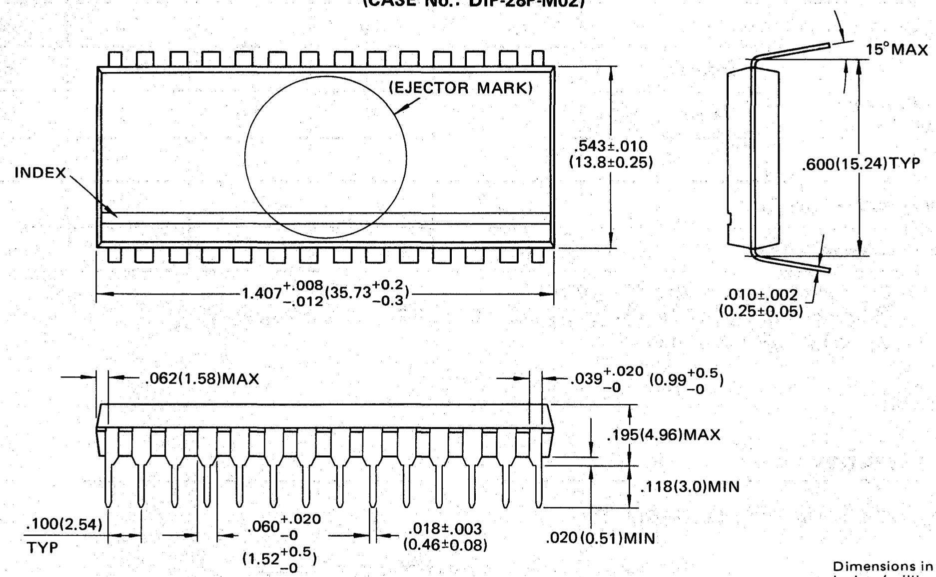
PACKAGE DIMENSIONS

(Suffix: P)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M02)

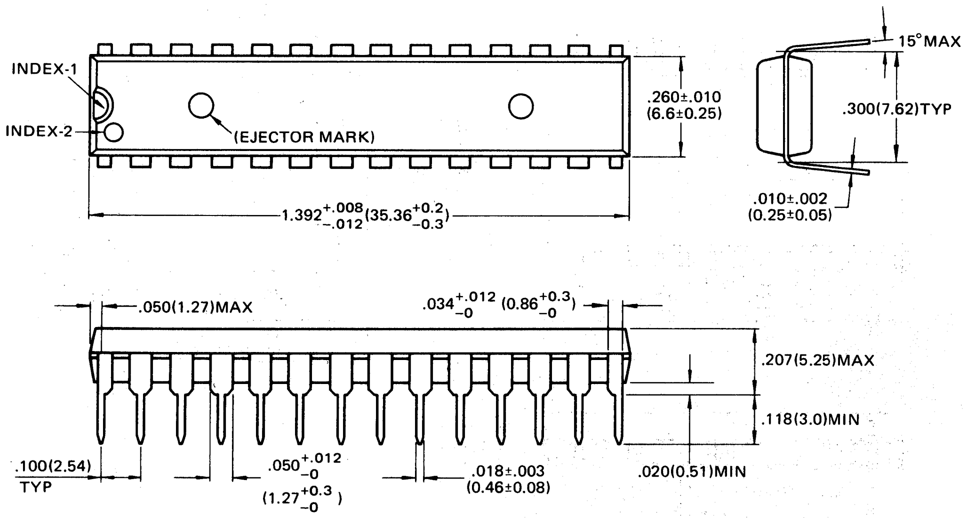


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: P-SK)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)



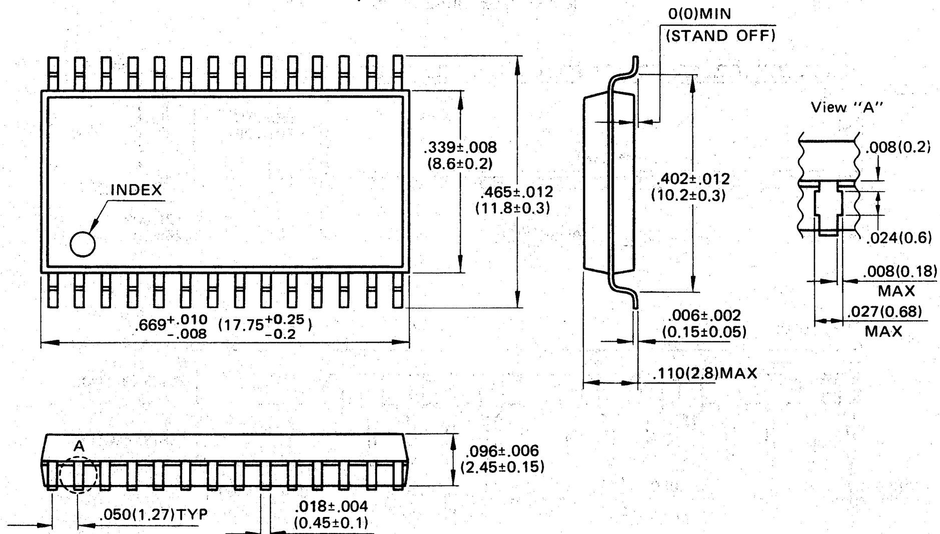
Dimensions in inches (millimeters)

6

PACKAGE DIMENSIONS

(Suffix: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



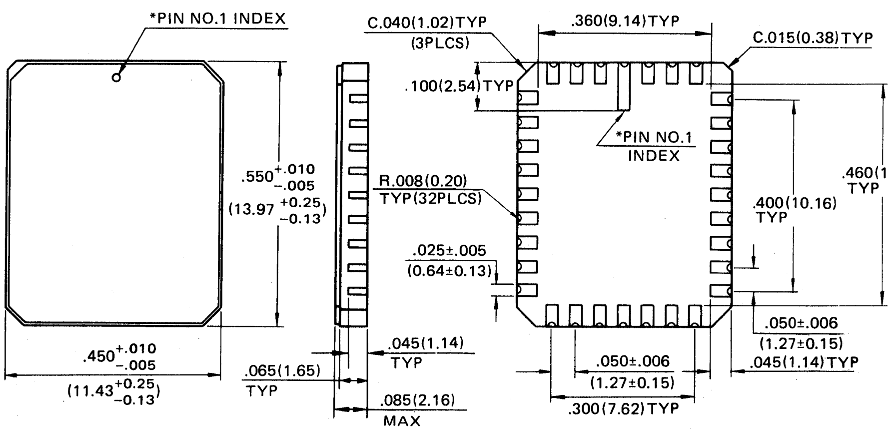
Dimensions in
inches (millimeters)

6

PACKAGE DIMENSIONS

(Suffix: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches (millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

6

FUJITSU

CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

MB 84256-10/10L/10LL
MB 84256-12/12L/12LL
MB 84256-15/15L/15LL

August 1986
Edition 2.0

256K-BIT (32,768 x 8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW POWER

The Fujitsu MB 84256 is a 32,768-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronouse circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volts power supply is required.

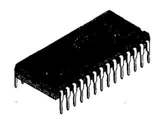
The MB 84256 is ideally suited for use in microprocesser systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

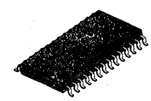
- Organization: 32,768 x 8 bits
- Fast access time: 100 ns max. (MB 84256-10/10L/10LL)
  120 ns max. (MB 84256-12/12L/12LL)
  150 ns max. (MB 84256-15/15L/15LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state outputs
- Single +5V power supply, ±10% tolerance
- Low power standby:
  CMOS level: 5.5 mW max. (MB 84256-10/12/15)
  0.55 mW max. (MB 84256-10L/10LL/12L/12LL/15L/15LL)
  TTL level: 16.5 mW max. (MB 84256-10/10L/10LL/12/12L/12LL/15/15L/15LL)
- Data retention: 2.0V
- Standard 28-pin DIP (600 mil) (Suffix: -P)
- Standard 28-pin Bend-type Plastic Flat Package (450 mil) (Suffix: -PF)
- Standard 32-pad LCC (Suffix: -CV)

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC}+0.5	V
Output Voltage		V_{OUT}	−0.5 to V_{CC}+0.5	V
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	CERAMIC	T_{STG}	−65 to +150	°C
	PLASTIC		−40 to +125	

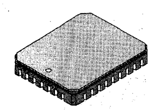
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





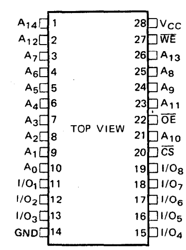
PLASTIC PACKAGE DIP-28P-M02

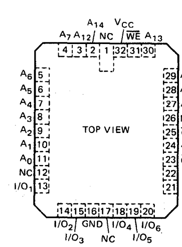
PLASTIC PACKAGE FPT-28P-M02



CERAMIC PACKAGE LCC-32C-A02

PIN ASSIGNMENT

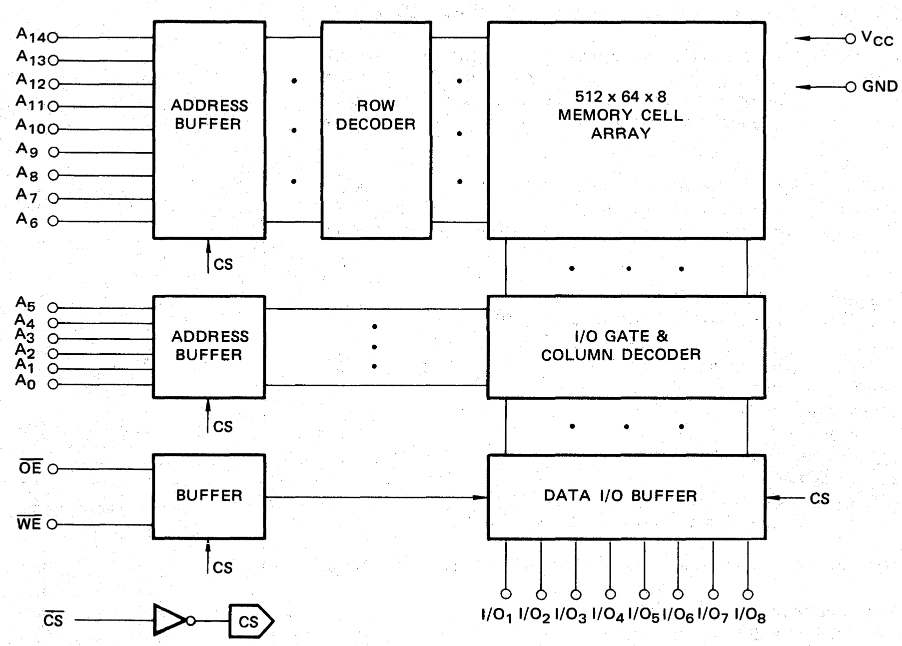




This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

Fig. 1 — MB 84256 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	DOUT DISABLE	I_{CC}	HIGH-Z
L	L	H	READ	I_{CC}	D_{OUT}
L	X	L	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0 *		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

* -2.0 V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.3 V at DC level)

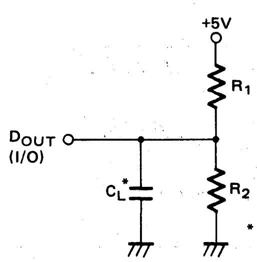
DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	MB 84256-10/12/15		MB 84256-10L/10LL/ 12L/12LL/15L/15LL		Unit	Test Conditions
		Min	Max	Min	Max		
Standby Supply Current	I_{SB1}		1		0.1	mA	$\overline{CS} \geq V_{CC}-0.2V$
	I_{SB2}		3		3		$\overline{CS} = V_{IH}$
Active Supply Current	I_{CC1}		45		45	mA	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL} I_{OUT} = 0 mA
Operating Supply Current	I_{CC2}		70		70		Cycle = Min., Duty = 100%, I_{OUT} = 0 mA
Input Leakage Current	I_{LI}	-1	1	-1	1	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	-1	1	-1	1	μA	$V_{I/O}$ = 0V to V_{CC}, $\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Output High Voltage	V_{OH}	2.4		2.4		V	I_{OH} = -1.0 mA
Output Low Voltage	V_{OL}		0.4		0.4	V	I_{OL} = 2.1 mA

Note: All voltages are referenced to GND

Fig. 2 — AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V; Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load

* Including Jig and stray capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 84256-10/ 10L/10LL		MB 84256-12/ 12L/12LL		MB 84256-15/ 15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time*2	t_{AA}		100		120		150	ns
$\overline{CS}$ Access Time*3	t_{ACS}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		40		50		60	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns
Chip Select to Output Low-Z*4*5	t_{CLZ}	10		10		10		ns
Output Enable to Output Low-Z*4*5	t_{OLZ}	5		5		5		ns
Chip Select to Output High-Z*4*5	t_{CHZ}		40		40		50	ns
Output Enable to Output High-Z*4*5	t_{OHZ}		40		40		50	ns

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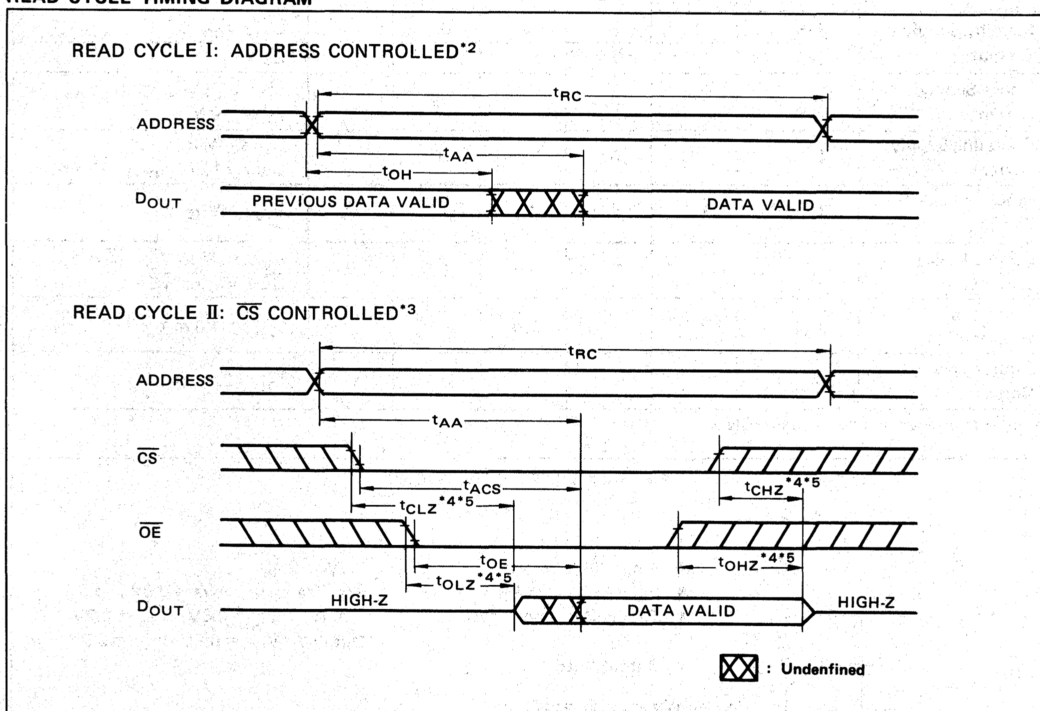
READ CYCLE TIMING DIAGRAM*1



Note:
*1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS} = \overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

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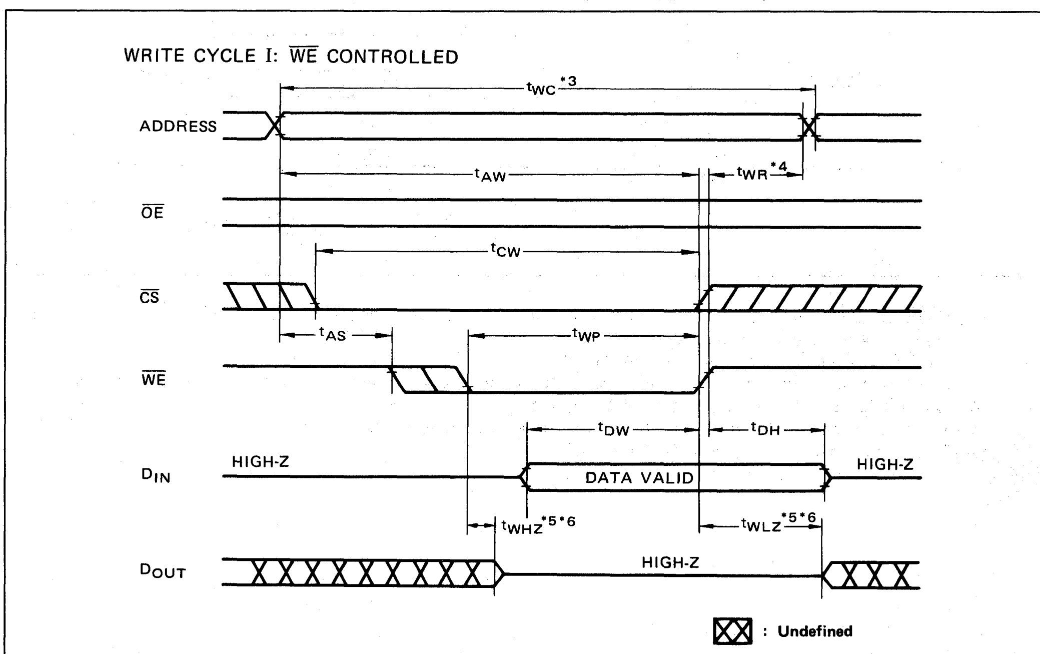
WRITE CYCLE*1 *2

Parameter	Symbol	MB 84256-10/ 10L/10LL		MB 84256-12/ 12L/12LL		MB 84256-15/ 15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	100		120		150		ns
Address Valid to End of Write	t_{AW}	80		85		100		ns
Chip Select to End of Write	t_{CW}	80		85		100		ns
Data Valid to End of Write	t_{DW}	40		45		50		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Pulse Width	t_{WP}	60		70		90		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time*4	t_{WR}	5		5		5		ns
$\overline{WE}$ to Output Low-Z*5 *6	t_{WLZ}	5		5		5		ns
$\overline{WE}$ to Output High-Z*5 *6	t_{WHZ}		40		40		50	ns

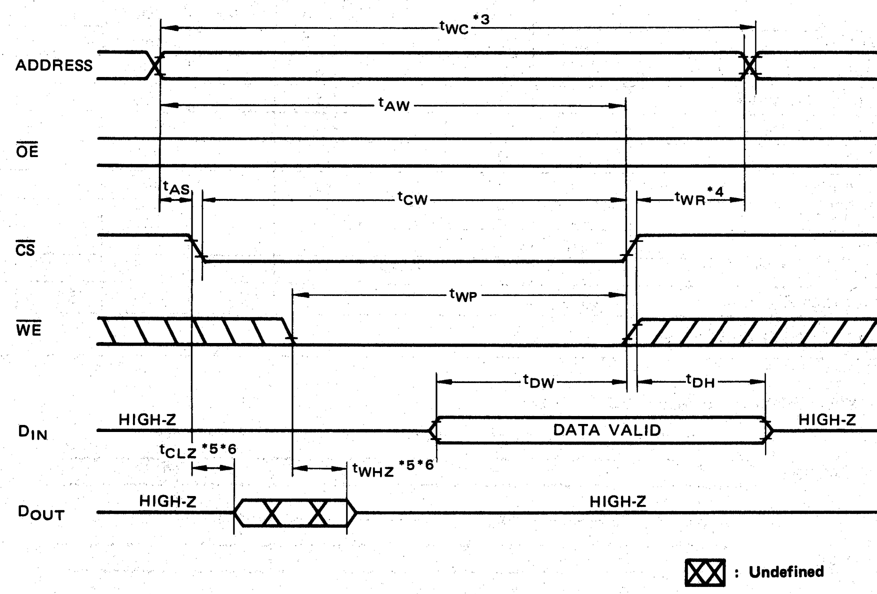
WRITE CYCLE TIMING DIAGRAM*1 *2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined form last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is specified with Load II in Fig. 2.

6

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is specified with Load II in Fig. 2.

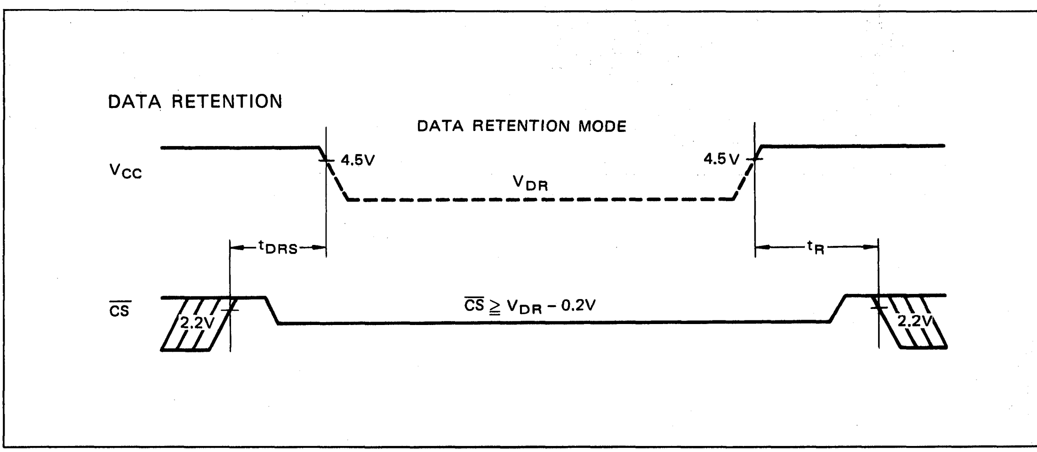
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Data Retention Supply Voltage*1		V_{DR}	2.0	5.5	V
Data Retention*2 Supply Current	Standard	I_{DR}		1	mA
	L-Version			50	μA
	LL-Version*3			5	
Data Retention Setup Time		t_{DRS}	0		ns
Operation Recovery Time		t_R	t_{RC}		ns

Note: *1 $\overline{CS} \geq V_{DR}-0.2V$
*2 $V_{DR} = 3.0V$, $\overline{CS} \geq V_{DR}-0.2V$
*3 $V_{DR} = 3.0V$, $T_A = 40°C$

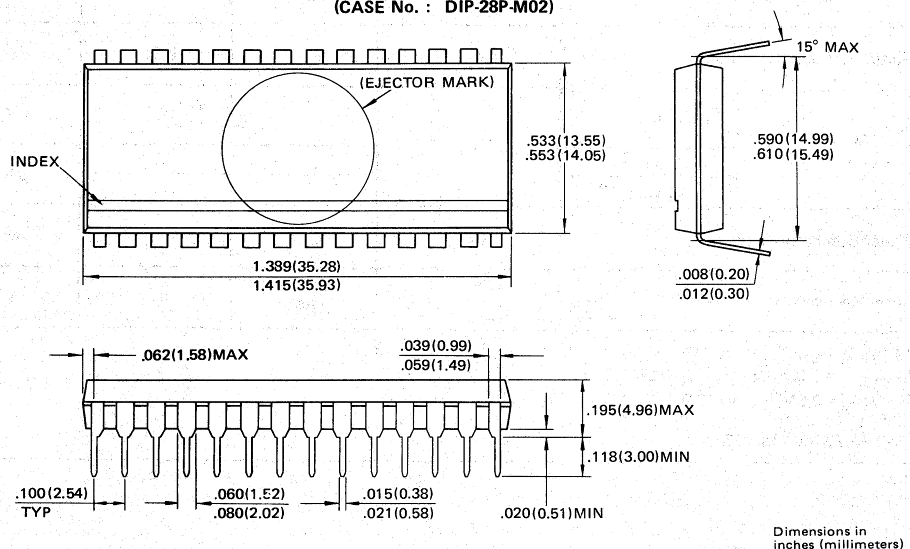
DATA RETENTION TIMING



PACKAGE DIMENSIONS

(Suffix: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



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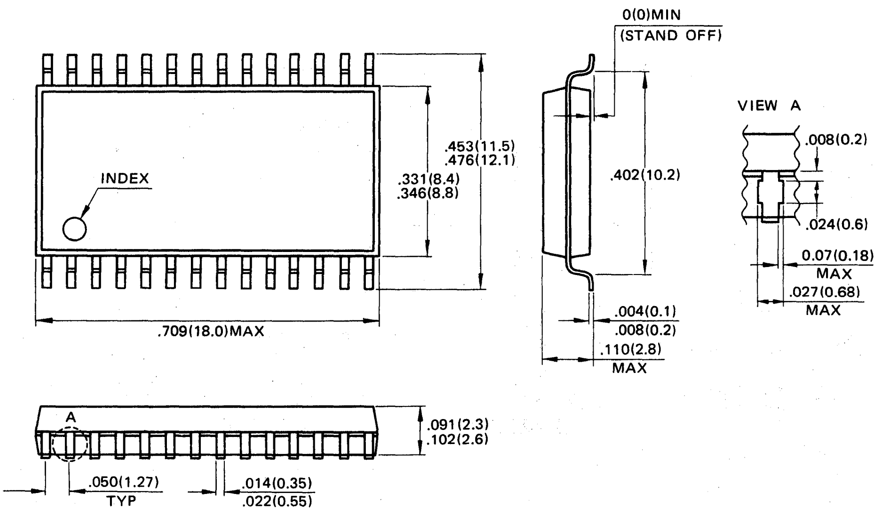
PACKAGE DIMENSIONS

(Suffix: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



Detail of "A" part

Dimensions in inches (millimeters)

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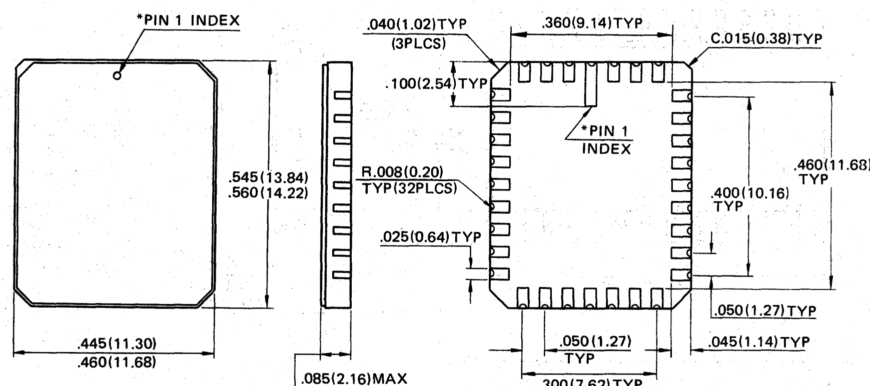
PACKAGE DIMENSIONS

(Suffix: CV)

**32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)**



Dimensions in inches
(millimeters)

*Shape of Pin 1 index : Subject to change without notice

FUJITSU

CMOS 262,144-BIT STATIC RANDOM ACCESS MEMORY

MB84256A-70/70L/70LL
MB84256A-10/10L/10LL
MB84256A-12/12L/12LL
MB84256A-15/15L/15LL

TS256-B889
Sept. 1988

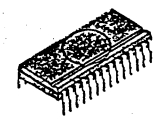
256K-BIT (32,768x8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW POWER

PRELIMINARY

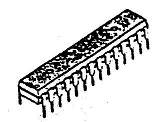
The Fujitsu MB84256A is a 32,768-word by 8-bit static random access memory fabricated with a CMOS sillicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The MB84256A is ideally suited for use in microprocesser systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

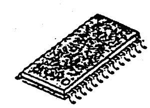
- Organization : 32,768 x 8 bits
- Fast access time : 70 ns max. (MB84256A-70/70L/70LL)
  100 ns max. (MB84256A-10/10L/10LL)
  120 ns max. (MB84256A-12/12L/12LL)
  150 ns max. (MB84256A-15/15L/15LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three state outputs
- Single +5V power supply, ±10% tolerance
- Low power standby :
  CMOS level: 5.5 mW max. (MB84256A-70/10/12/15)
  0.55 mW max. (MB84256A-70L/70LL/10L/10LL/12L/12LL/15L/15LL)
  TTL level: 16.5 mW max. (MB84256A-70/70L/70LL/10/10L/10LL/12/12L/12LL/15/15L/15LL)
- Data retention: 2.0V min.
- Standard 28-pin DIP (600mil) (Suffix: P)
- Standard 28-pin DIP (300mil) (Suffix: P-SK)
- Standard 28-pin Bend-type FPT (450mil) (Suffix: PF)



PLASTIC PACKAGE
DIP-28P-M02



PLASTIC PACKAGE
DIP-28P-M04



PLASTIC PACKAGE
FPT-28P-M02

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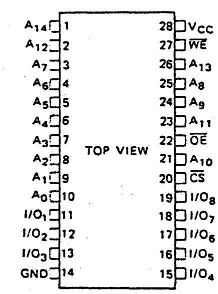
PIN ASSIGNMENT



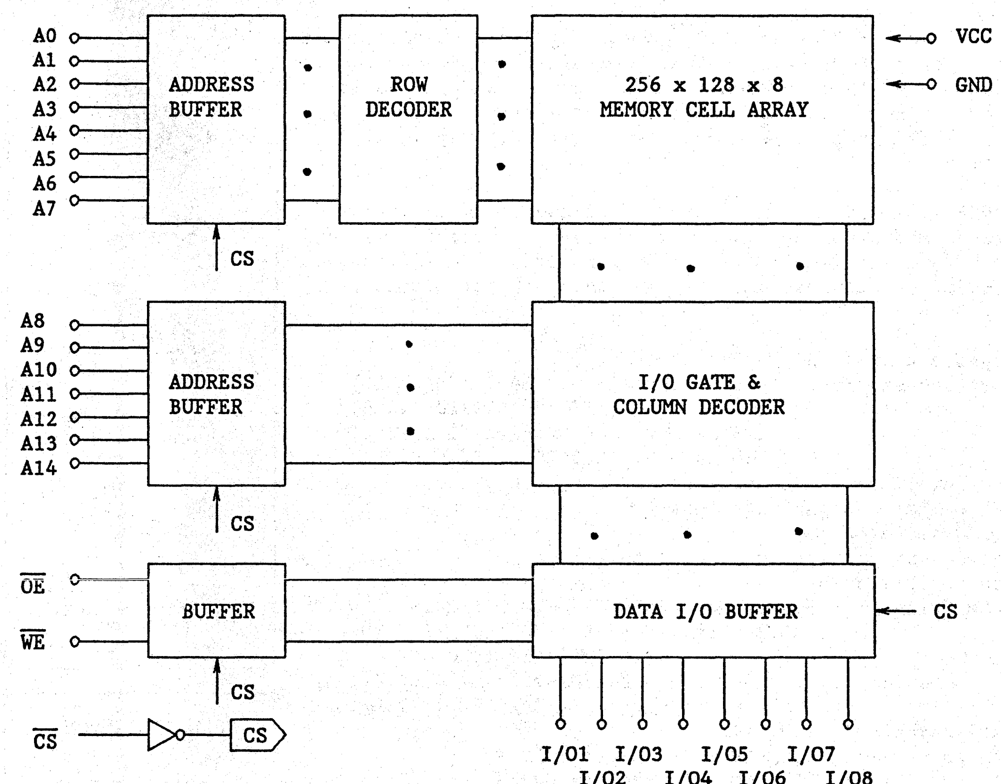
ABSOLUTEMAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +7.0	V
Input Voltage	VIN	-0.5 to VCC+0.5	V
Output Voltage	VI/O	-0.5 to VCC+0.5	V
Temperature under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-40 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB84256A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	ISB	High-Z
L	H	H	DOUT Disable	ICC	High-Z
L	L	H	Read	ICC	DOUT
L	X	L	Write	ICC	DIN

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			8	pF
Input Capacitance (VIN=0V)	CIN			7	pF

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

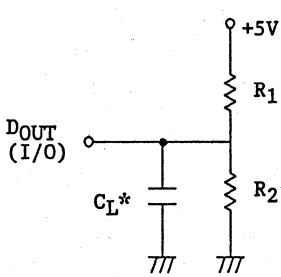
DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	MB84256A-70/10/12/15		MB84256A-70L/70LL/10L/10LL/12L/12LL/15L/15LL		Unit	Test Condition
		Min	Max	Min	Max		
Standby Supply Current	ISB1		1		0.1	mA	CS≥VCC-0.2V
	ISB2		3		3	mA	CS=VIH
Active Supply Current	ICC1		55		55	mA	VIN=VIH or VIL CS=VIL, IOUT=0mA
Operating Supply Current -70	ICC2		80		80	mA	Cycle=Min. Duty=100% IOUT=0mA
Operating Supply Current -10/12/15			70		70		
Input Leakage Current	ILI	-1	1	-1	1	μA	VIN=0V to VCC
Output Leakage Current	ILI/O	-1	1	-1	1	μA	VI/O=0V to VCC CS=VIH OE=VIH or WE=VIL
Input High Voltage	VIH	2.2	VCC +0.3	2.2	VCC +0.3	V	
Input Low Voltage	VIL	-3.0 *	0.8	-3.0 *	0.8	V	
Output High Voltage	VOH	2.4		2.4		V	IOH=-1.0mA
Output Low Voltage	VOL		0.4		0.4	V	IOL=2.1mA

Note: All voltages are referenced to GND.
*: -3.0V min. for pulse width less than 20 ns. (VIL min. = -0.3V at DC level.)

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times:
  5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels
  Input: VIL=0.8V, VIH=2.2V
  Output: VOL=0.8V, VOH=2.0V
- Output Load

* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load1	1.8KΩ	990Ω	100pF	except tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ
Load2	1.8KΩ	990Ω	5pF	tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ

6

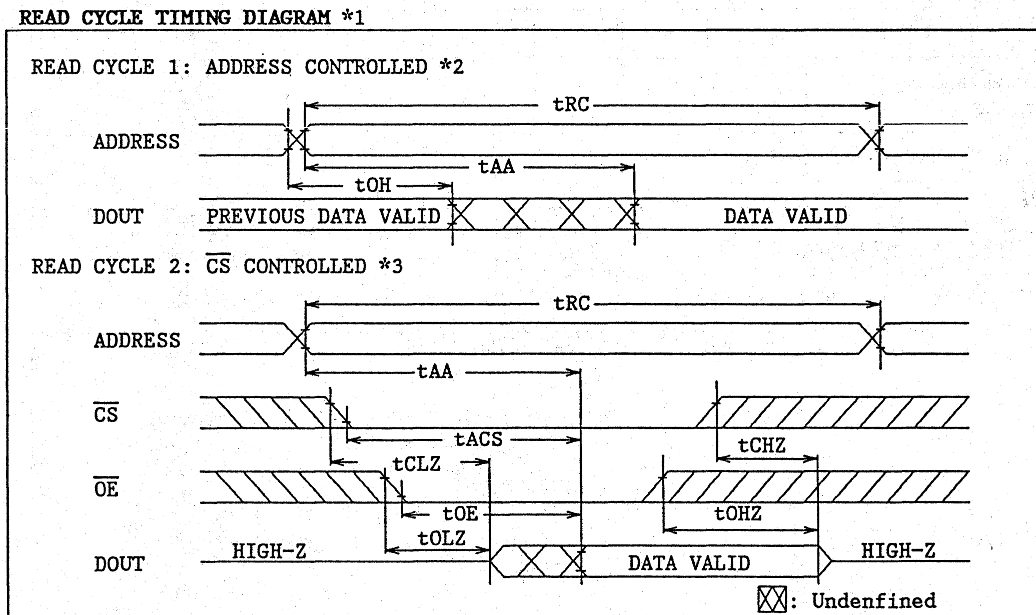
AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB84256A-70/70L/70LL		MB84256A-10/10L/10LL		MB84256A-12/12L/12LL		MB84256A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	70		100		120		150		ns
Address Access Time *2	tAA		70		100		120		150	ns
$\overline{CS}$ Access Time *3	tACS		70		100		120		150	ns
Output Enable to Output Valid	tOE		35		40		50		60	ns
Output Hold from Address Change	tOH	20		20		20		20		ns
Chip Select to Output Low-Z *4*5	tCLZ	10		10		10		10		ns
Output Enable to Output Low-Z *4*5	tOLZ	5		5		5		5		ns
Chip Select to Output High-Z *4*5	tCHZ		25		40		40		50	ns
Output Enable to Output High-Z *4*5	tOHZ		25		40		40		50	ns

READ CYCLE TIMING DIAGRAM *1



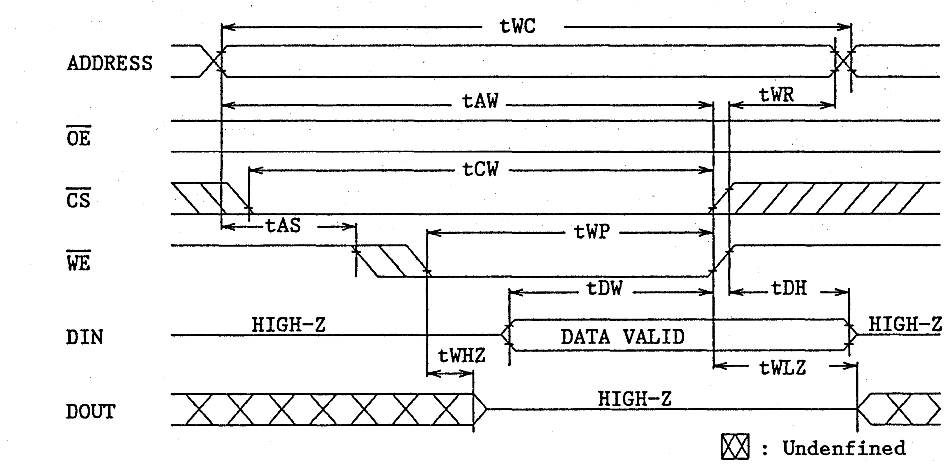
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load 2 in Fig. 2.

WRITE CYCLE *1*2

Parameter	Symbol	MB84256A-70/70L/70LL		MB84256A-10/10L/10LL		MB84256A-12/12L/12LL		MB84256A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time *3	tWC	70		100		120		150		ns
Address Valid to End of Write	tAW	50		80		85		100		ns
Chip Select to End of Write	tCW	50		80		85		100		ns
Data Valid to End of Write	tDW	25		40		45		50		ns
Data Hold Time	tDH	0		0		0		0		ns
Write Pulse Width	tWP	50		60		70		90		ns
Address Setup Time	tAS	0		0		0		0		ns
Write Recovery Time *4	tWR	5		5		5		5		ns
$\overline{WE}$ to Output Low-Z *5*6	tWLZ	5		5		5		5		ns
$\overline{WE}$ to Output High-Z *5*6	tWHZ		25		40		40		50	ns

WRITE CYCLE TIMING DIAGRAM *1*2

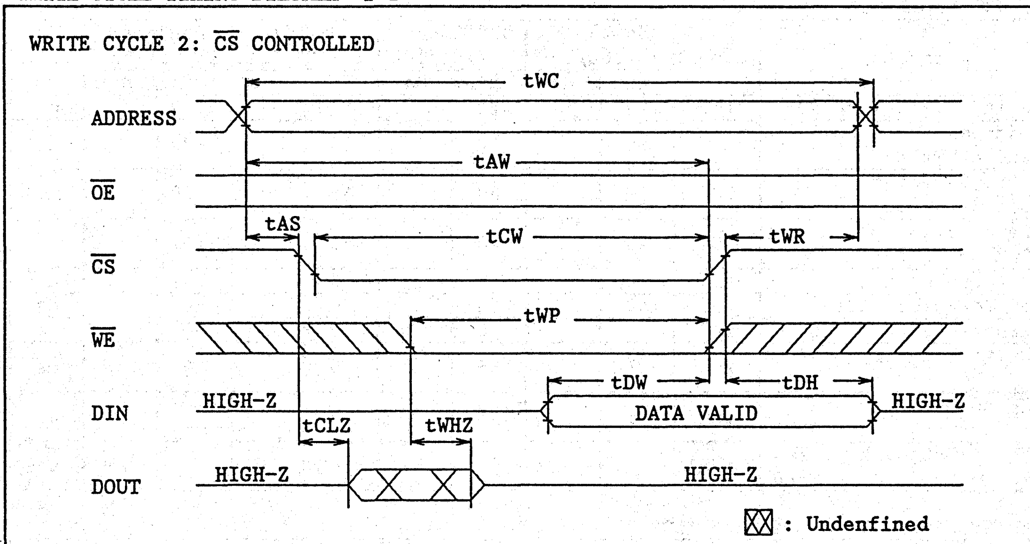
WRITE CYCLE 1: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 tWR is defined from the end point of WRITE Mode.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is specified with Load 2 in Fig. 2.

6

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 If OE, CS are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage.

*6 This parameter is specified with Load 2 in Fig. 2.

6

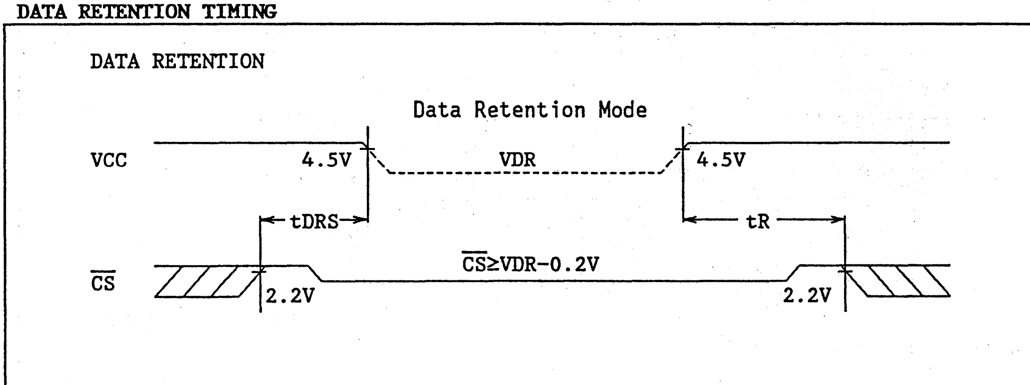
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage *1		VDR	2.0		5.5	V
Data Retention Supply Current *2	MB84256A-70/10/12/15	IDR			1.0	mA
	MB84256A-70L/10L/12L/15L			1.0	50	µA
	MB84256A-70LL/10LL/12LL/15LL			1.0	5.0 *3	
Data Retention Setup Time		tDRS	0			ns
Operation Recovery Time		tR	tRC			ns

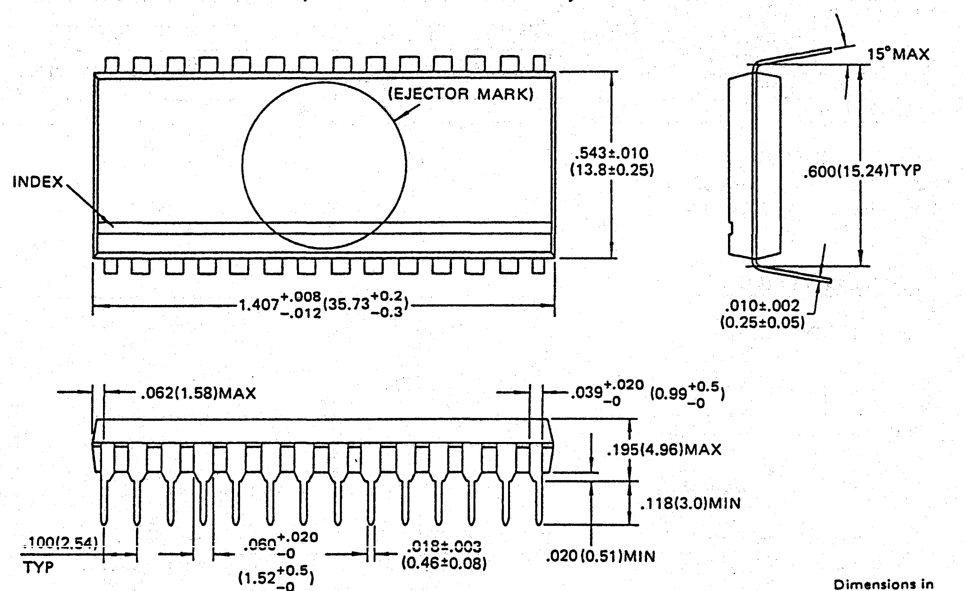
Note: *1 $\overline{CS}$≥VDR−0.2V
*2 VDR=3.0V, $\overline{CS}$≥VDR−0.2V
*3 VDR=3.0V, TA=40°C

DATA RETENTION TIMING



PACKAGE DIMENSIONS
(Suffix: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M02)



Dimensions in inches (millimeters)

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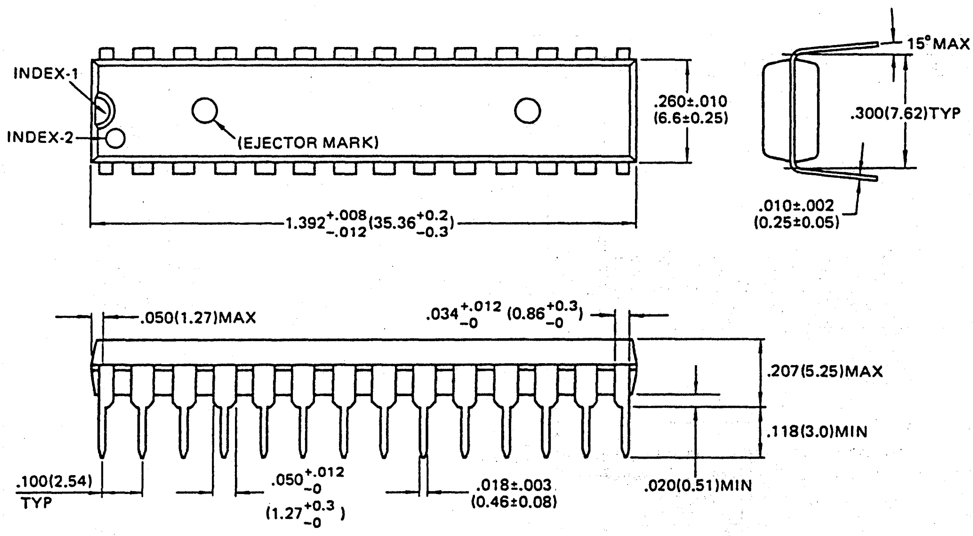
PACKAGE DIMENSIONS
(Suffix: P-SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)



Dimensions in inches (millimeters)

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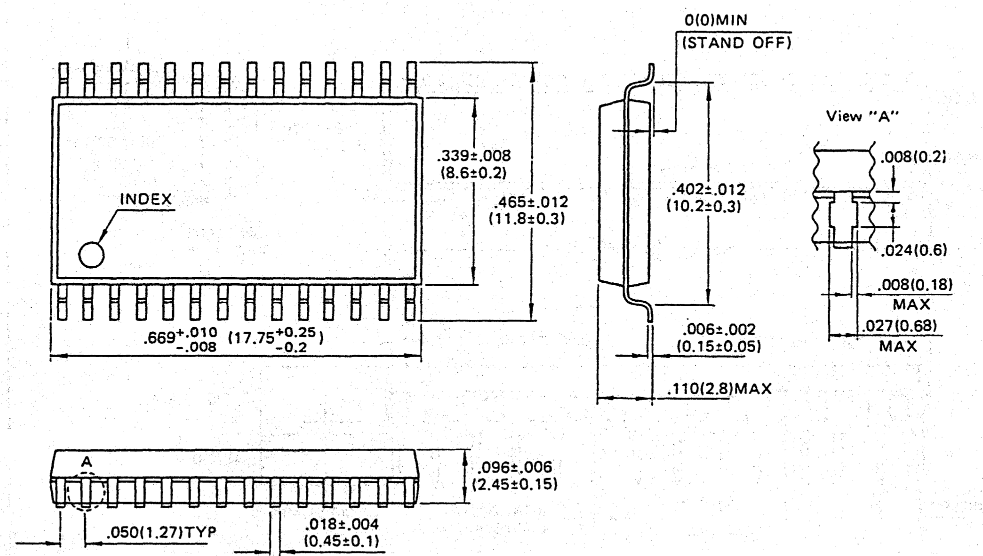
PACKAGE DIMENSIONS
(Suffix: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



Dimensions in
inches (millimeters)

6

FUJITSU

1M BIT CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOWER POWER

MB841000-80/80L
MB841000-10/10L

August 1988
Edition 1.0

1M BIT (131,072 x 8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW LOWER

The Fujitsu MB841000 is a 131,072-words x 8-bits static random access memory fabricated with a CMOS silicon-gate process. To make power dissipation lower, peripheral circuits consist of CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors. The memory utilizes asynchronous circuitry. All pins are TTL compatible, and a single +5V power supply is required.

The MB841000 has 32-pin 600mil plastic DIP and 32-pin 525 mil plastic FPT as package option.

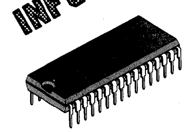
The MB841000 is ideally suited for use in microprocessor systems and other applications where fast access time, and ease of use are required. For example, since data retention voltege(VDR) is 2.0V min., MB841000 can be used as non volatile memory by battery back-up. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 131,072 x 8 bits
- Fast access time: $t_{AA}=t_{AC1}=t_{AC2}$=80ns max. / t_{OE}=35ns max. (MB841000-80/80L)
  $t_{AA}=t_{AC1}=t_{AC2}$=100ns max. / t_{OE}=40ns max. (MB841000-10/10L)
- TTL compatible inputs/outputs
- Three-state outputs
- Single +5V power supply, ±10% tolerance
- Low power dissipation :

	Standard (MB841000-80/10)	Low-power version (MB841000-80L/10L)
Active :	440 mA max.	440 mA max.
Standby (TTL Level) :	16.5 mW max.	16.5 mW max.
Standby (CMOS Level) :	11 mW max.	1.1 mW max.

- Data retention voltage : 2.0V min.
- Standard 32-pin PLASTIC DIP(600mil) : Suffix -P
- Standard 32-pin PLASTIC SOJ(525mil): Suffix -PF
- JEDEC Standard Pin assignment

ADVANCE INFORMATION



PLASTIC PACKAGE
(DIP-32P-M01)

TBD

PLASTIC PACKAGE
(FPT-32P-MXX)

PIN ASSIGNMENT (TOP VIEW)

|---|---|---|---|
NC	1	32	Vcc
A16	2	31	A15
A14	3	30	CS2
A12	4	29	$\overline{WE}$
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CS1}$
A0	12	21	I/08
I/01	13	20	I/07
I/02	14	19	I/06
I/03	15	18	I/05
GND	16	17	I/04

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

FUJITSU

CMOS 262,144-BIT STATIC RANDOM ACCESS MEMORY

MB84F256-25

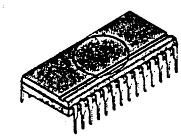
TS258-B88Y
Nov. 1988

256K-BIT (32,768x8) FULL CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION

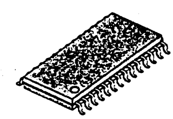
PRELIMINARY

The Fujitsu MB84F256 is a 32,768-word by 8-bit static random access memory. Fabricated with full CMOS circuit, MB84F256 realizes extremely low data retention current compared with that of MB84256, which can allows MB84F256 to use non volatile memory using a back up battery.

The MB84F256 features minimum voltage of 1.1V operation to utilize single lithium battery.
The device suits for application where, low and wide supply voltage and low power comsumption are required.



PLASTIC PACKAGE
DIP-28P-M02



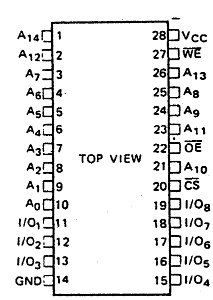
PLASTIC PACKAGE
FPT-28P-M02

- Organization : 32,768 x 8 bits
- Fast access time : 250 ns max. (VCC=4.0V to 5.5V)
  2000 ns max. (VCC=2.2V to 3.6V)
  5000 ns max. (VCC=1.1V to 1.8V)
- Completely static operation: No clock required
- TTL compatible inputs/outputs (at +5V power supply)
- Three state outputs
- Single power supply (+1.5V, +3.0V, +5.0V)

- Low power dissipation
  Standby : 0.18 mW max. (VCC=1.1V to 1.8V)
  1.8 mW max. (VCC=2.2V to 3.6V)
  11.0 mW max. (VCC=4.0V to 5.5V)
  Active : 9.0 mW max. (VCC=1.1V to 1.8V)
  72.0 mW max. (VCC=2.2V to 3.6V)
  220 mW max. (VCC=4.0V to 5.5V)

- Data retention: 1.1V min.
- Standard 28-pin DIP (600mil) (Suffix: P)
- Standard 28-pin Bend-type FPT (450mil) (Suffix: PF)

PIN ASSIGNMENT



ABSOLUTEMAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +7.0	V
Input Voltage	VIN	-0.5 to VCC+0.5	V
Output Voltage	VI/O	-0.5 to VCC+0.5	V
Temperature under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-40 to +125	°C

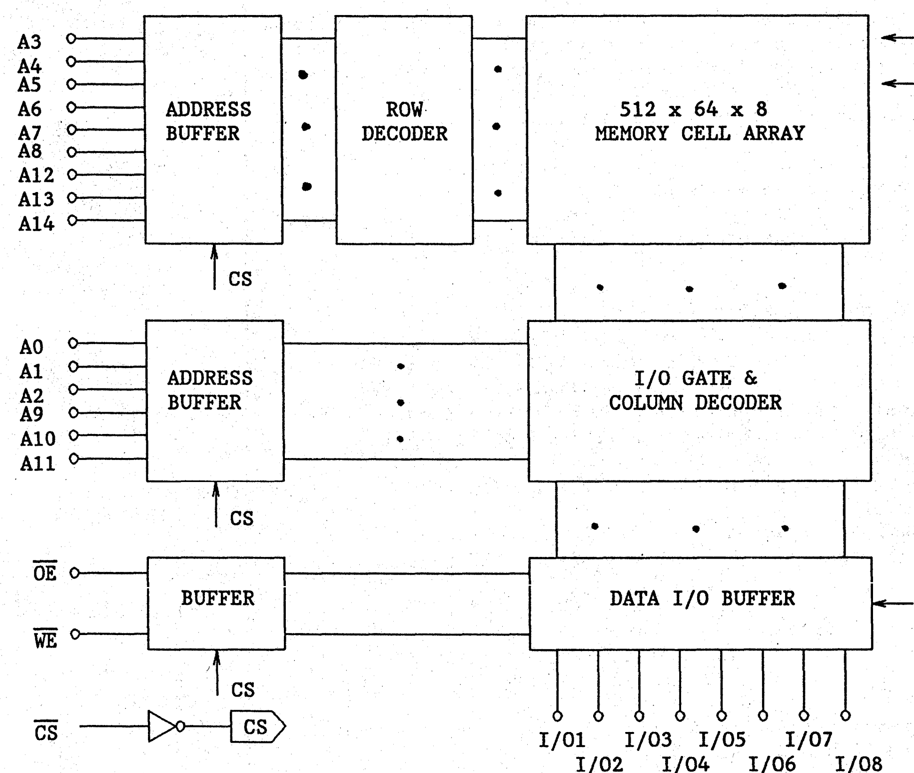
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

6

Fig. 1 – MB84F256 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	ISB	High-Z
L	H	H	DOUT Disable	ICC	High-Z
L	L	H	Read	ICC	DOUT
L	X	L	Write	ICC	DIN

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			8	pF
Input Capacitance (VIN=0V)	CIN			7	pF

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	1.1	1.5	1.8	V
		2.2	3.0	3.6	
		4.0	5.0	5.5	
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.) *1*2

Parameter	Symbol	Supply Voltage VCC (V)	Min	Max	Unit	Condition
Standby Supply Current	ISB1	1.1V to 1.8V		1.0	μA	$\overline{CS}$≥VCCx0.9
		2.2V to 3.6V		5.0		
		4.0V to 5.5V		10.0		
	ISB2	1.1V to 1.8V		0.1	mA	$\overline{CS}$=VIH
		2.2V to 3.6V		0.5		
		4.0V to 5.5V		2.0		
Active Supply Current	ICC1	1.1V to 1.8V		2.0	mA	VIN=VIH or VIL
		2.2V to 3.6V		5.0		$\overline{CS}$=VIL
		4.0V to 5.5V		10.0		IOUT=0mA
Operating Supply Current	ICC2	1.1V to 1.8V		5.0	mA	Cycle=Min
		2.2V to 3.6V		20.0		Duty=100%
		4.0V to 5.5V		40.0		IOUT=0mA
Input Leakage Current	ILI	1.1V to 1.8V		0.1	μA	VIN=0V to VCC
		2.2V to 3.6V		0.5		
		4.0V to 5.5V		1.0		
Output Leakage Current	ILI/O	1.1V to 1.8V		0.1	μA	VI/O=0V to VCC
		2.2V to 3.6V		0.5		$\overline{CS}$=VIH
		4.0V to 5.5V		1.0		$\overline{OE}$=VIH or $\overline{WE}$=VIL
Input High Voltage	VIH	1.1V to 1.8V	VCCx0.8	VCC+0.3	V	
		2.2V to 3.6V	VCCx0.8	VCC+0.3		
		4.0V to 5.5V	2.2	VCC+0.3		
Input Low Voltage	VIL	1.1V to 1.8V	-0.3	0.2	V	
		2.2V to 3.6V	-0.3	0.3		
		4.0V to 5.5V	-0.3	0.6 *3		
Output High Voltage	VOH	1.1V to 1.8V	0.8		V	IOH=-0.1mA
		2.2V to 3.6V	2.0			IOH=-0.5mA
		4.0V to 5.5V	2.4			IOH=-1.0mA
Output Low Voltage	VOL	1.1V to 1.8V		0.2	V	IOL= 0.2mA
		2.2V to 3.6V		0.3		IOL= 1.0mA
		4.0V to 5.5V		0.4		IOL= 2.1mA

Note: *1 All voltages are referenced to GND.
*2 Please refer to "TYPICAL CHARACTERISTICS CURVES" when VCC=1.8V to 2.2V and 3.6V to 4.0V.
*3 VIL max.=0.8V at VCC=4.5V to 5.5V.

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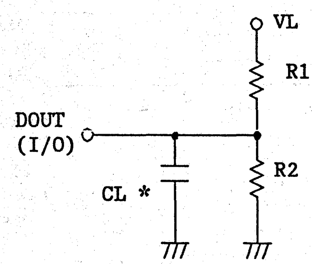
AC CHARACTERISTICS TEST CONDITIONS

Parameter	Supply Voltage VCC (V)	Conditions
Input Pulse Level	1.1V to 1.8V	VIH=VCC, VIL=0V
	2.2V to 3.6V	VIH=VCC, VIL=0V
	4.0V to 5.5V	VIH=2.4V, VIL=0.5V
Input Pulse Rise & Fall Times	1.1V to 1.8V	5 ns (Transient between 0.2V and VCCx0.8)
	2.2V to 3.6V	5 ns (Transient between 0.3V and VCCx0.8)
	4.0V to 5.5V	5 ns (Transient between 0.7V and 2.2V)
Timing Reference Level	1.1V to 1.8V	Input: VIH=VCCx0.8, VIL=0.2V Output: VOH=VCCx0.7, VOL=0.3V
	2.2V to 3.6V	Input: VIH=VCCx0.8, VIL=0.3V Output: VOH=VCCx0.7, VOL=0.4V
	4.0V to 5.5V	Input: VIH=2.2V, VIL=0.7V Output: VOH=2.2V, VOL=0.8V
Output Load	1.1V to 1.8V	VL=1.5V
	2.2V to 3.6V	VL=3.0V
	4.0V to 5.5V	VL=5.0V

Fig. 2 – AC TEST CONDITIONS



* Including Jig and stray capacitance.

	R1	R2	CL	Parameters Measured
Load1	1.8KΩ	990Ω	100pF	except tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ
Load2	1.8KΩ	990Ω	5pF	tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

READ CYCLE *1*6

Parameter	Symbol	VCC= 1.1V to 1.8V		VCC= 2.2V to 3.6V		VCC= 4.0V to 5.5V		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	5000		2000		250		ns
Address Access Time *2	tAA		5000		2000		250	ns
$\overline{CS}$ Access Time *3	tACS		5000		2000		250	ns
Output Enable to Output Valid	tOE		1000		500		100	ns
Output Hold from Addresss Change	tOH	200		100		50		ns
$\overline{CS}$ to Output Low-Z *4*5	tCLZ	150		70		30		ns
Output Enable to Output Low-Z *4*5	tOLZ	120		50		20		ns
$\overline{CS}$ to Output High-Z *4*5	tCHZ	80	200	40	100	5	50	ns
Output Enable to Output High-Z *4*5	tOHZ		200		100		50	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the following points from steady state voltage.
- VCC=1.1V to 1.8V : ±100mV
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

*5 This parameter is specified with Load 2 in Fig. 2.
*6 Please refer to "TYPICAL CHARACTERISTICS CURVES" when VCC=1.8V to 2.2V and 3.6V to 4.0V.

6

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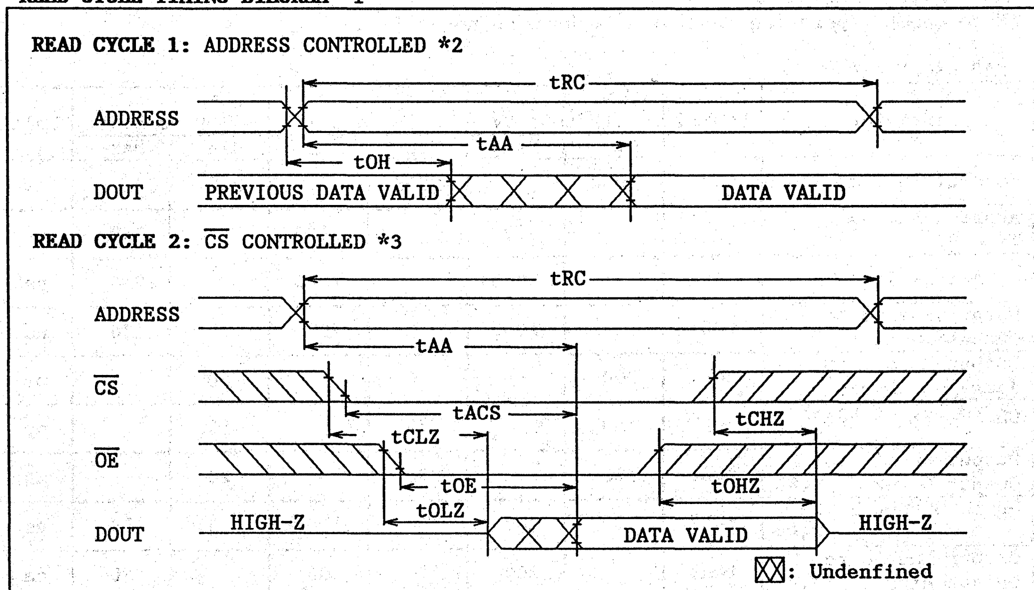
READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the following points from steady state voltage.
- VCC=1.1V to 1.8V : ±100mV
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

*5 This parameter is specified with Load 2 in Fig. 2.
*6 Please refer to "TYPICAL CHARACTERISTICS CURVES" when VCC=1.8V to 2.2V and 3.6V to 4.0V.

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE *1*2*7

Parameter	Symbol	VCC= 1.1V to 1.8V		VCC= 2.2V to 3.6V		VCC= 4.0V to 5.5V		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time *3	tWC	5000		2000		250		ns
Address Valid to End of Write	tAC	4500		1500		200		ns
Chip Select to End of Write	tCW	4500		1500		200		ns
Data Valid to End of Write	tDW	2000		800		100		ns
Data Hold Time	tDH	0		0		0		ns
Write Pulse Width	tWP	3000		1000		150		ns
Address Setup Time	tAS	0		0		0		ns
Write recovery Time *4	tWR	0		0		0		ns
$\overline{WE}$ to Output Low-Z *5*6	tWLZ	50		30		10		ns
$\overline{WE}$ to Output High-Z *5*6	tWHZ		200		100		50	ns

Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the following points from steady state voltage.

- VCC=1.1V to 1.8V : ±100mV
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

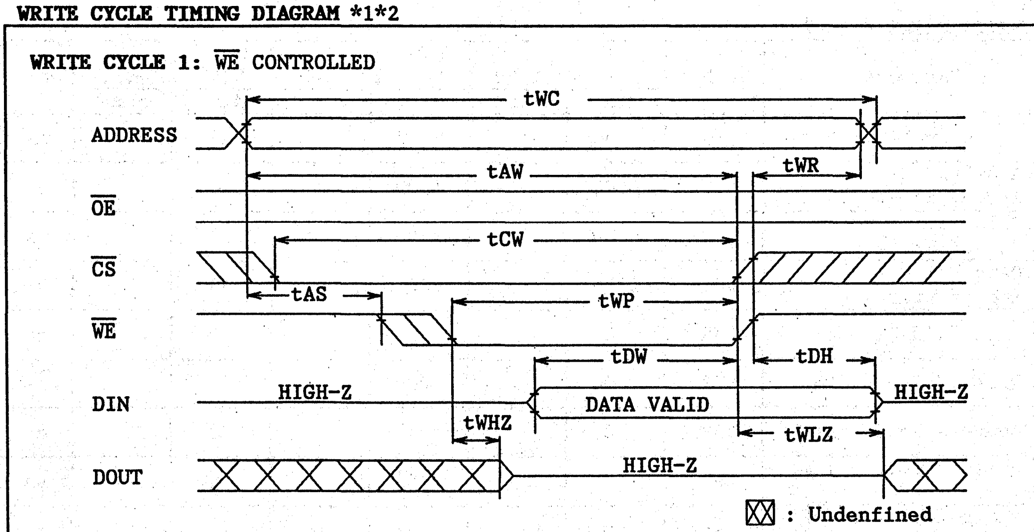
*6 This parameter is specified with Load 2 in Fig. 2.

*7 Please refer to "TYPICAL CHARACTERISTICS CURVES" when VCC=1.8V to 2.2V and 3.6V to 4.0V.

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the following points from steady state voltage.

- VCC=1.1V to 1.8V : ±100mV
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

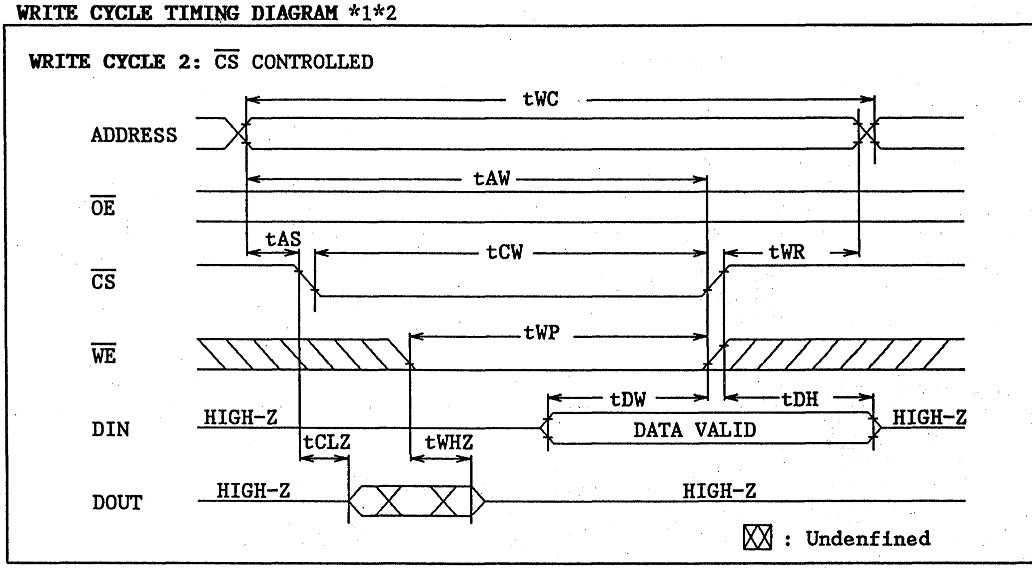
*6 This parameter is specified with Load 2 in Fig. 2.

*7 Please refer to "TYPICAL CHARACTERISTICS CURVES" when VCC=1.8V to 2.2V and 3.6V to 4.0V.

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 If OE, CS are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the following points from steady state voltage.
- VCC=1.1V to 1.8V : ±100mV
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

*6 This parameter is specified with Load 2 in Fig. 2.

*7 Please refer to "TYPICAL CHARACTERISTICS CURVES" when VCC=1.8V to 2.2V and 3.6V to 4.0V.

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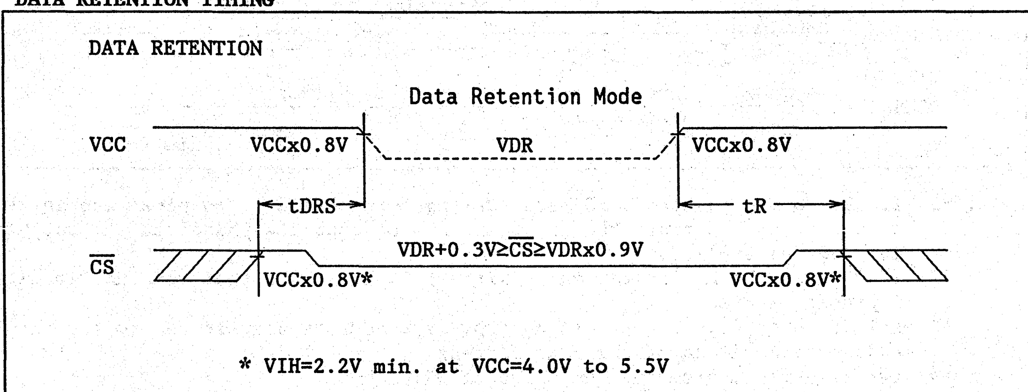
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Data Retention Supply Voltage *1	VDR	1.1	5.5	V
Data Retention Supply Current *2	IDR		1.0	μA
Data Retention Setup Time	tDRS	0		ns
Operation Recovery Time	tR	tRC *3		ns

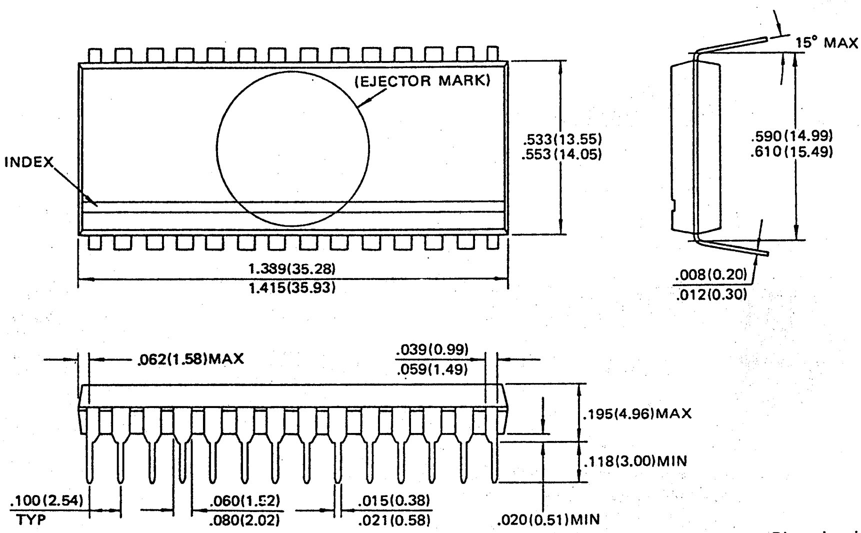
Note: *1 VDR+0.3V≥$\overline{CS}$≥VDRx0.9
*2 VDR=1.8V, VDR≥$\overline{CS}$≥VDRx0.9
*3 tRC: Read Cycle

DATA RETENTION TIMING



PACKAGE DIMENSIONS
(Suffix: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M02)

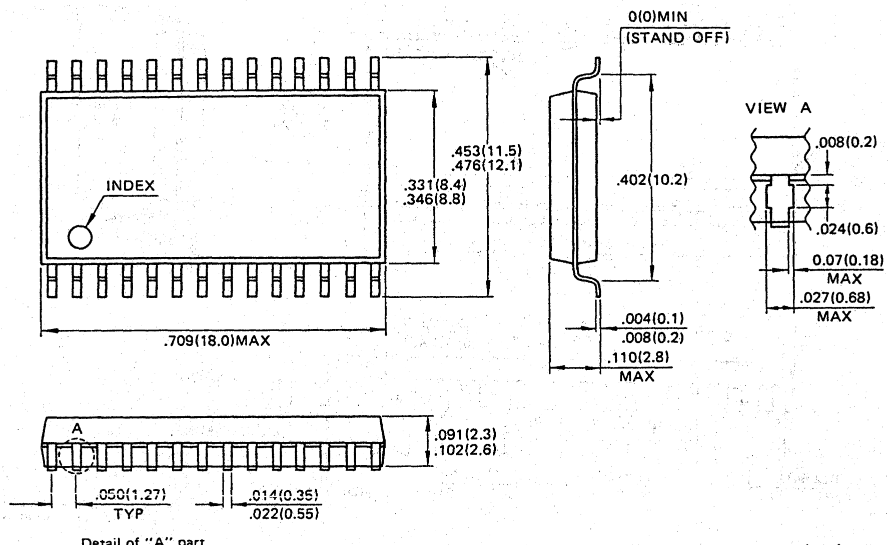


Dimensions in inches (millimeters)

6

PACKAGE DIMENSIONS
(Suffix: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



Dimensions in inches (millimeters)

Section 7

Application-Specific Static Memories

Page	Device	Maximum Access Time(ns)	Capacity	Package Options			Sealing Method
7-3	MB81C79B-35	35	73728 bits	28-pin	Plastic	DIP	Plastic
	MB81C79B-45	45	(8192w x 9b)	28-pin	Plastic	FPT	Plastic
7-15	MB8287-25	25	262144 bits	32-pin	Plastic	DIP	Plastic
	MB8287-35	35	(32768w x 8b)	32-pin	Plastic	FPT	Plastic
7-27	MB82T790-20	20	73728 bits	32-pin	Plastic	DIP	Plastic
	MB82T790-25	25	(8192w x 9b)	32-pin	Plastic	FPT	Plastic
7-39	MB81C51-25	25	2048 bits	68-pad	Plastic	LCC	Plastic
	MB81C51-30	35	512 x 4-way or	64-pin	Ceramic	PGA	Metal
			1024 x 2-way				
7-55	MB8421-90	90	16384-bits	64-pin	Plastic	FPT	Plastic
	MB8421-90 L	90	(2048w x 8b)	52-pin	Plastic	DIP	Plastic
	MB8421-12	120		48-pin	Plastic	DIP	Plastic
	MB8421-12L	120					
	MB8422-90	90					
	MB8422-90 L	90					
	MB8422-12	120					
	MB8422-12L	120					
7-73	MB8431-90	90	16384-bits	52-pin	Plastic	DIP	Plastic
	MB8431-90L	90	(2048w x 8b)	64-pin	Plastic	FPT	Plastic
	MB8431-12	120		48-pin	Plastic	DIP	Plastic
	MB8431-12L	120					
	MB8432-90	90					
	MB8432-90L	90					
	MB8432-12	120					
	MB8432-12L	120					

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FUJITSU

CMOS 73728-BIT STATIC RANDOM ACCESS MEMORY

MB81C79B-35
MB81C79B-45

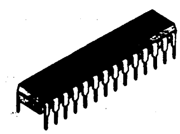
TS244-B888
August 1988

72K-BIT (8192x9) HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

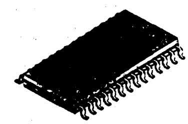
The Fujitsu MB81C79B is 8192 words x 9 bits static random access memory fabricated with a CMOS process. Because of 9 bit organization, this device is convenient to be used for parity check function and also this device has two fast column addresses, therefore MB81C79B is very suitable to used as cache buffers. To make power dissipation lower, peripheral circuits consist of CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors. All pins are TTL compatible and a single 5 volts power supply is required.

All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 8192 words x 9 bits
- Static operation: No clock or timing strobe required
- Fast access time: tAA=tACS1=35ns max, tOE=10ns max.
  A11, A12 access time=12ns max. (MB81C79B-35)
  tAA=tACS1=45ns max, tOE=15ns max.
  A11, A12 access time=15ns max. (MB81C79B-45)
- Low power consumption: 550mW (Operation)
  138mW (TTL Standby)
  83mW (CMOS Standby)
- Single +5V supply, ±10% tolerance
- TTL compatible inputs and outputs
- Three-state inputs and outputs
- Chip selects for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 28-pin Plastic DIP package (Suffix: -P-SK)
- Standard 28-pin Gull wing flat package (Suffix: -PF)



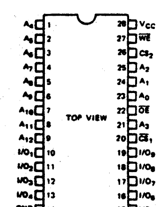
PLASTIC PACKAGE
DIP-28P-M04



PLASTIC PACKAGE
FPT-28P-M02

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	-3.5 to +7	V
Output Voltage on any I/O with respect to GND	V_{OUT}	-0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-40 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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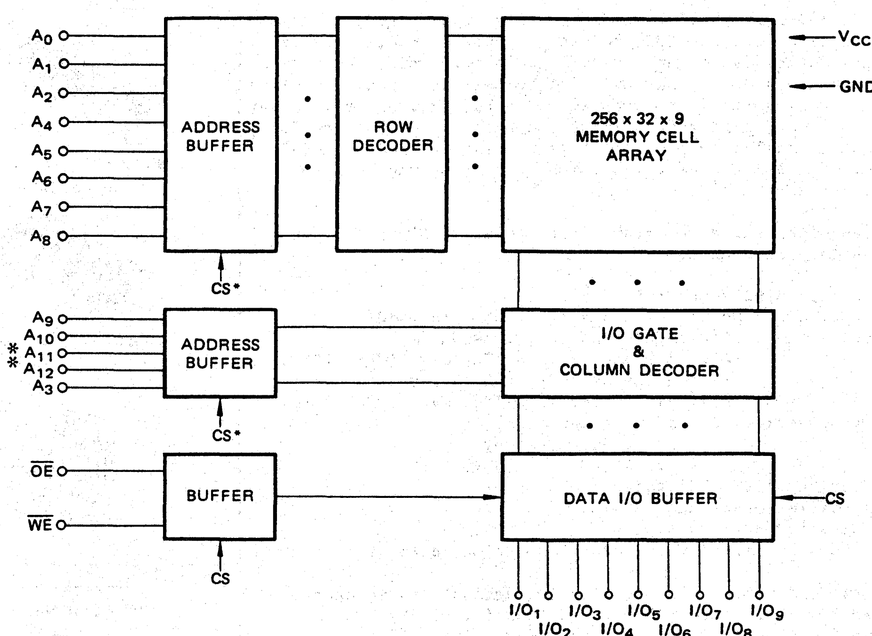
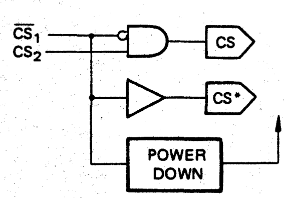
Fig. 1 – MB 81C79A BLOCK DIAGRAM





TRUTH TABLE

$\overline{CS}_1$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

* Fast address

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V) ($\overline{CS}_1$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN} = 0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* –2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = –0.5V at DC level)

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DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{LO}	-10	10	μA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}
Operating Supply Current	I_{CC}		130	mA	$\overline{CS_1}$ = V_{IL} I/O = Open, Cycle = Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC} = Min to Max. $\overline{CS_1}$ = V_{CC}–0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}–0.2V
	I_{SB2}		25	mA	$\overline{CS_1}$ = V_{IH}
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = –4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC} = 0V to V_{CC} Min. $\overline{CS_1}$ = Lower of V_{CC} or V_{IH} Min.

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AC TEST CONDITIONS

Input Pulse Levels: 0.6V to 2.4V

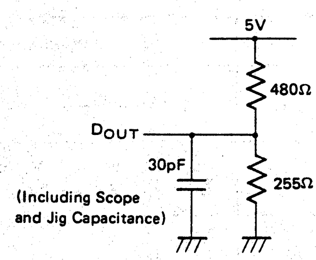
Input Pulse Rise And Fall Times: 5ns (Transient time between 0.8V and 2.2V)

Timing Measurement Reference Levels: Input: 1.5V
Output: 1.5V

Fig. 2

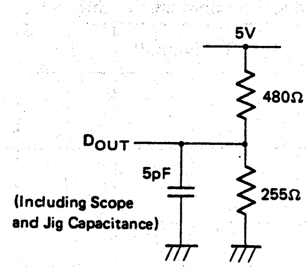
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE[*1]

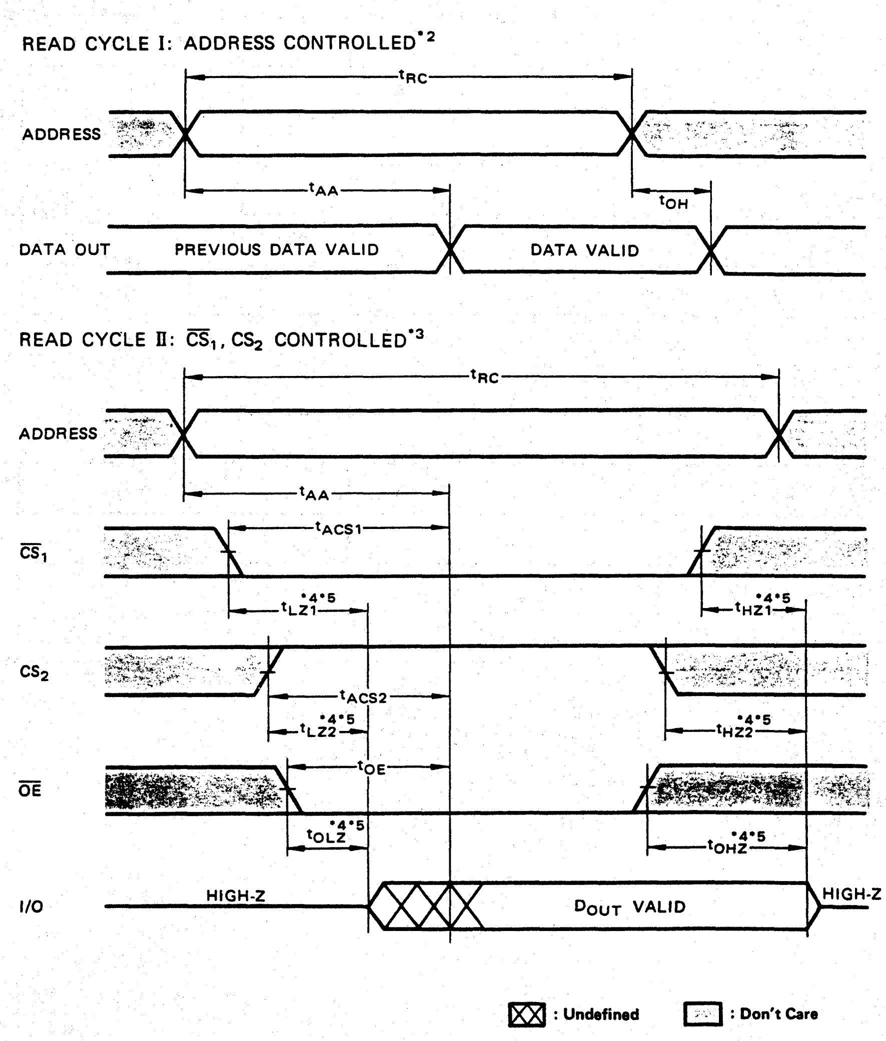
Parameter	Symbol	MB81C79B-35		MB81C79B-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time[*2]	t_{AA}		35 #1		45 #2	ns
$\overline{CS}_1$ Access Time[*3]	t_{ACS1}		35		45	ns
CS_2 Access Time[*3]	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		10		15	ns
Output Active from $\overline{CS}_1$[*4*5]	t_{LZ1}	5		5		ns
Output Active from CS_2[*4*5]	t_{LZ2}	2		2		ns
Output Active from $\overline{OE}$[*4*5]	t_{OLZ}	2		2		ns
Output Disable from $\overline{CS}_1$[*4*5]	t_{HZ1}		20		25	ns
Output Disable from CS_2[*4*5]	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$[*4*5]	t_{OHZ}		20		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

#1 A11, A12 address access time is 12ns max.
#2 A11, A12 address access time is 15ns max.

7

READ CYCLE TIMING DIAGRAM[*1]



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE[*1]

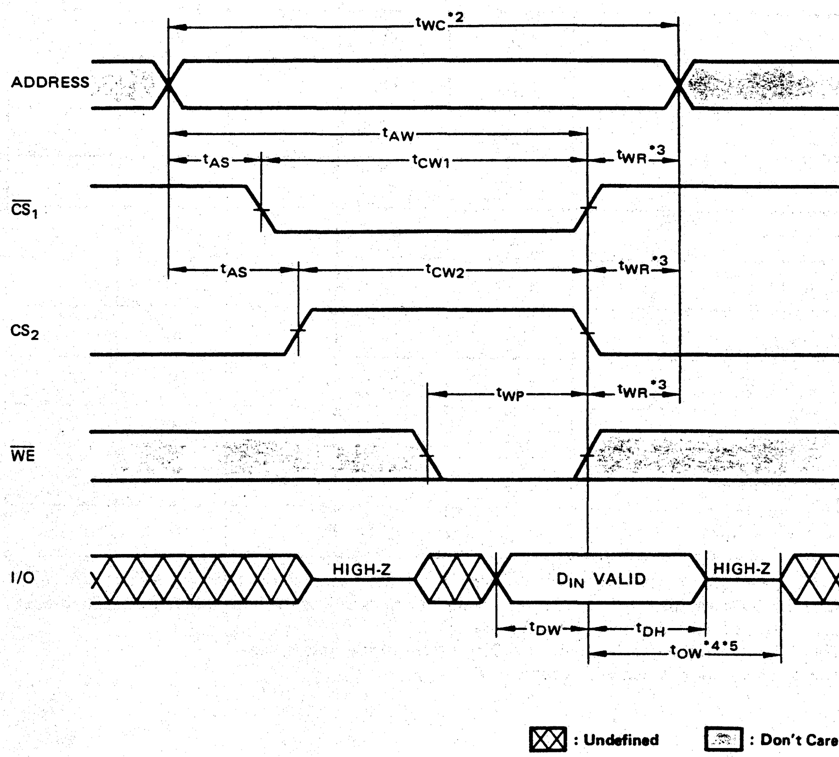
Parameter	Symbol	MB81C79B-35		MB81C79B-45		Unit
		Min	Max	Min	Max	
Write Cycle Time[*2]	t_{WC}	35		45		ns
$\overline{CS}_1$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time[*3]	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$[*4*5]	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$[*4*5]	t_{OW}	0		0		ns

Note: *1 If $\overline{CS}_1$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

7

WRITE CYCLE TIMING DIAGRAM[*1]

WRITE CYCLE I: $\overline{CS}_1$, CS_2 CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS}_1$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycle are determined from the last address transition to the first address transition of next address.

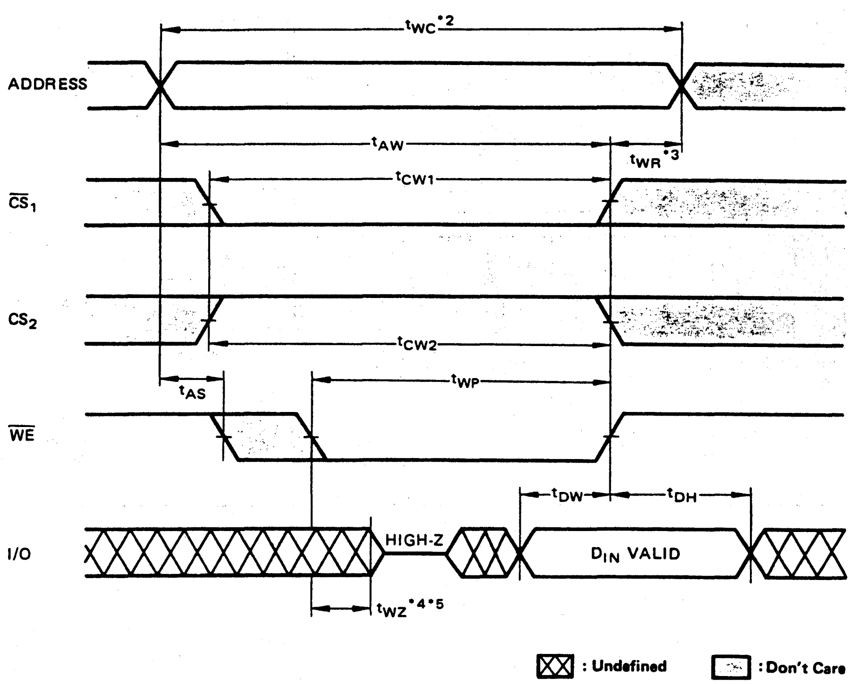
*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage.

*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED

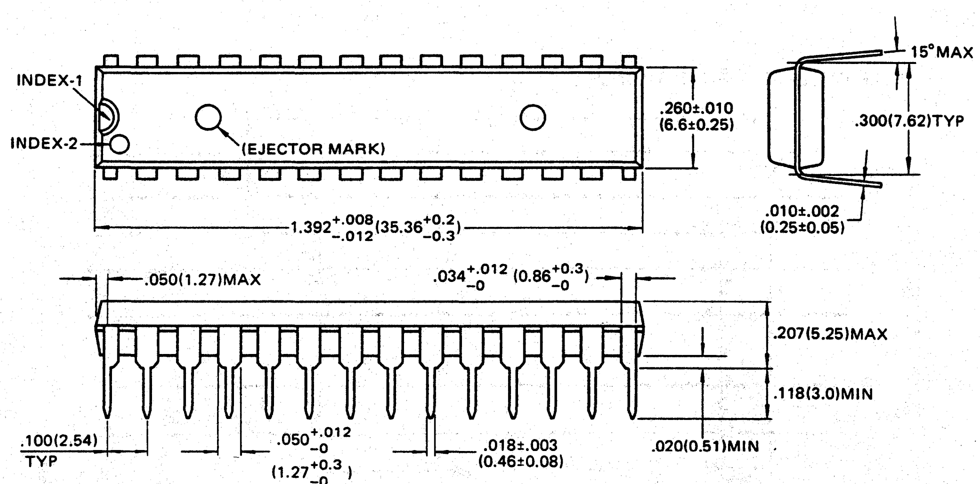


Note: *1 If $\overline{OE}$, $\overline{CS}_1$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)

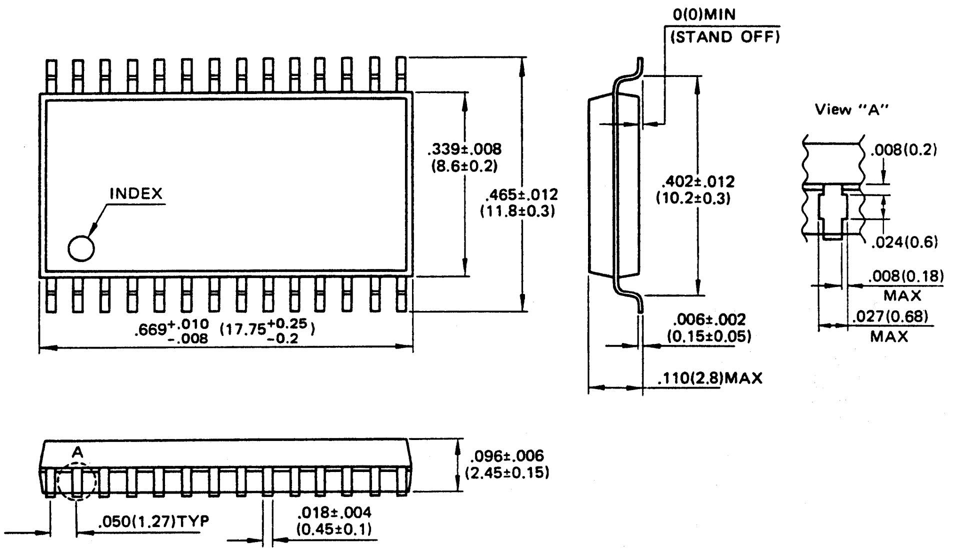


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: -PF)



Dimensions in inches (millimeters)

7

7

FUJITSU

CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

MB8287-25 MB8287-35

September 1988
Edition 1.0

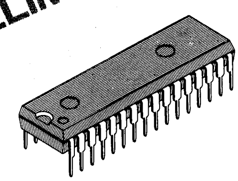
PRELIMINARY

32K x 8-BIT STATIC RANDOM ACCESS MEMORY WITH PARITY GENERATOR AND CHECKER

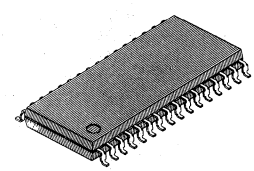
The Fujitsu MB8287 is 32768 words x 8 bits high speed static random access memory with parity generator and checker, fabricated with CMOS technology. To obtain smaller chip, cell consists of NMOS transistors and resistors therefore this device is assembled in 300 mil DIP and has such small power dissipation as 550mW max.
All pins are TTL compatible and single 5 volt power supply is required.

A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS_1}$ the other deselected packages automatically power down.
All devices offer the advantages of low power dissipation, low cost, and high performance.

- Organization: 32768 words x 8 bits
- Static operation: no clocks or timing strobe required
- Fast access time:
  $t_{AA} = t_{ACS1}$ = 25ns max,
  t_{ACS2} = 14ns max (MB8287-25)
  $t_{AA} = t_{ACS1}$ = 35ns max,
  t_{ACS2} = 15ns max (MB8287-35)
- Low power consumption:
  660mW max. (Operating) for 25ns
  550mW max. (Operating) for 35ns
  138mW max. (TTL Standby)
  83mW max. (CMOS Standby)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- Internal parity generator and checker.
- All inputs and outputs have protection against static charge
- Standard 32-pin DIP package (300 mil): (Suffix: P—SK)
- Standard 32-pin FPT package (450 mil): (Suffix: PF)

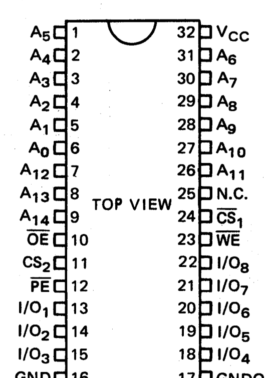


PLASTIC PACKAGE
(DIP-32P-M02)



PLASTIC PACKAGE
(FPT-32P-M02)

PIN ASSIGNMENT



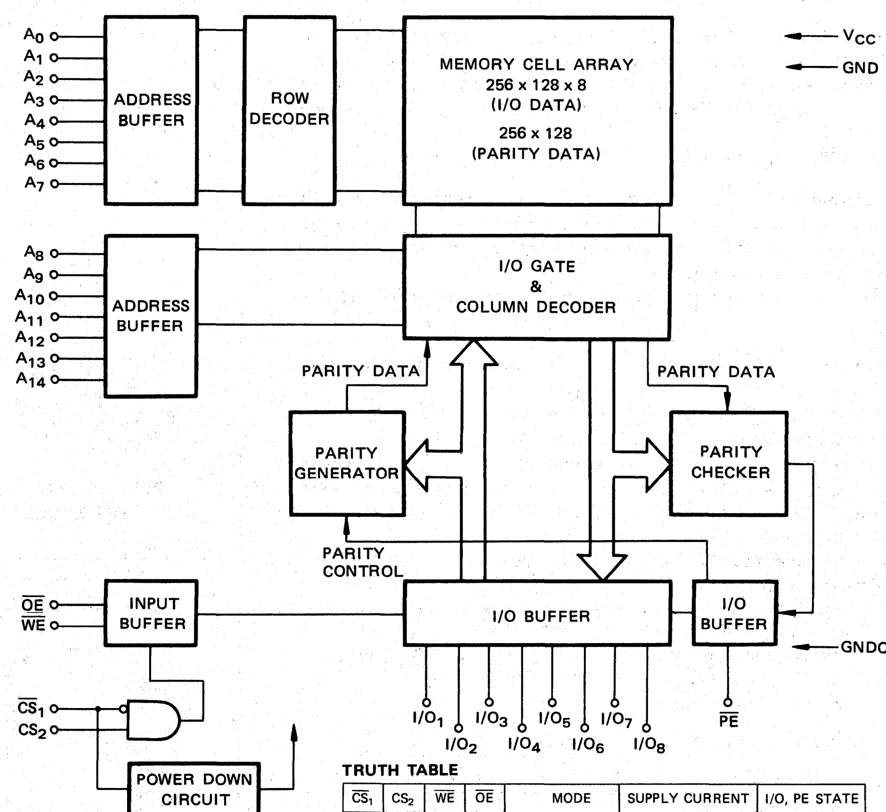
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	–3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	–0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature Range	T_{STG}	–45 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB8287 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}_1$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O, PE STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS}_1$, CS_2, $\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	C_{I1}			8	pF
Input Capacitance (Other Input)	V_{IN} = 0V	C_{I2}			7	pF
I/O Capacitance (with $\overline{PE}$)	$V_{I/O}$ = 0V	$C_{I/O}$			8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

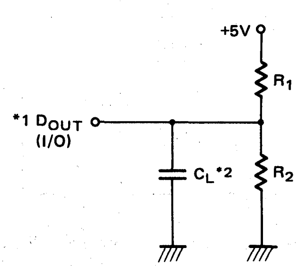
(Recommended operating conditions unless otherside noted.)

Parameter		Symbol	Test Conditions	Min	Max	Unit
Standby Supply Current		I_{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$		15	mA
		I_{SB2}	$V_{IN} \leq 0.2V$ $\overline{CS}_1 = V_{IH}$		25	mA
Operating Supply Current	25ns	I_{CC}	$I_{OUT} = 0mA$, $\overline{CS}_1 = V_{IL}$ Cycle = Min.		120	mA
	35ns				100	
Input Leakage Current		I_{LI}	$V_{IN} = 0V$ to V_{CC}	–5	5	μA
Output Leakage current		$I_{LI/O}$	$\overline{CS}_1 = V_{IH}$ = or $\overline{CS}_2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $OE = V_{IH}$, $V_{I/O} = 0V$ to V_{CC}	–5	5	μA
Input Low Voltage		V_{IL}		–2.0*1	0.8	V
Input High Voltage		V_{IH}		2.2	6.0	V
Output High Voltage		V_{OH}	$I_{OH} = -4mA$	2.4		V
Output Low Voltage		V_{OL}	$I_{OL} = 8mA$		0.4	V

Note: *1 –2.0V Min. for pulse width less than 20ns. (V_{IL} min. = –0.5V at DC level)
All voltages are referenced to GND.

Fig. 2 — AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$
  Output: $V_{OL} = 0.8V$, $V_{OH} = 2.2V$
- Output Load:



*1 $\overline{PE}$ pin is included.
*2 Including Scope and Jig Capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, t_{OHZ}, t_{PHZ} and t_{POHZ}
Load II	480Ω	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, t_{OHZ}, t_{PHZ} and t_{POHZ}

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE*1

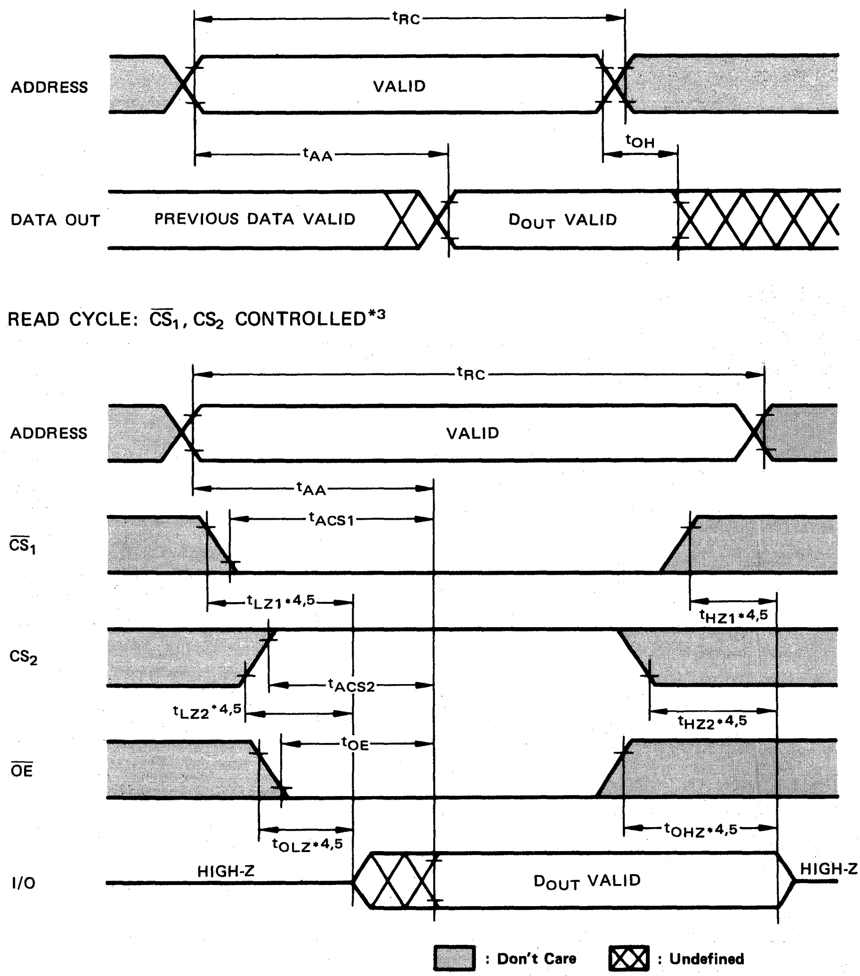
Parameter	Symbol	MB8287-25		MB8287-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time*2	t_{AA}		25		35	ns
$\overline{CS_1}$ Access Time*3	t_{ACS1}		25		35	ns
CS_2 Acces Time*3	t_{ACS2}		14		15	ns
$\overline{OE}$ Access Time	t_{OE}		12		14	ns
Output Hold from Address Change	t_{OH}	3		3		ns
Output Active from $\overline{CS_1}$ *4*5	t_{LZ1}	5		8		ns
Output Active from CS_2 *4*5	t_{LZ2}	2		3		ns
Output Active from $\overline{OE}$*4*5	t_{OLZ}	2		3		ns
Output Disable from $\overline{CS_1}$ *4*5	t_{HZ1}	1	15	1	15	ns
Output Disable from CS_2 *4*5	t_{HZ2}	1	15	1	15	ns
Output Disable from $\overline{OE}$*4*5	t_{OHZ}	1	15	1	15	ns
Parity Error Access from Address*2	t_{APA}		28		40	ns
Parity Error Access from $\overline{CS_1}$ *3	t_{APCS1}		28		40	ns
Parity Error Access from CS_2 *3	t_{APCS2}		14		15	ns
Parity Error Access from $\overline{OE}$	t_{APOE}		12		14	ns
Parity Error Hold from Address Change	t_{POH}	3		3		ns
Parity Error Disable from Address Change*4*5	t_{PHZA}	1	20	1	25	ns
Parity Error Disable from $\overline{CS_1}$ *4*5	t_{PHZ1}	1	15	1	15	ns
Parity Error Disable from CS_2 *4*5	t_{PHZ2}	1	15	1	15	ns
Parity Error Disable from $\overline{OE}$*4*5	t_{POHZ}	1	15	1	15	ns

Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM*1

READ CYCLE: ADDRESS CONTROLLED*2

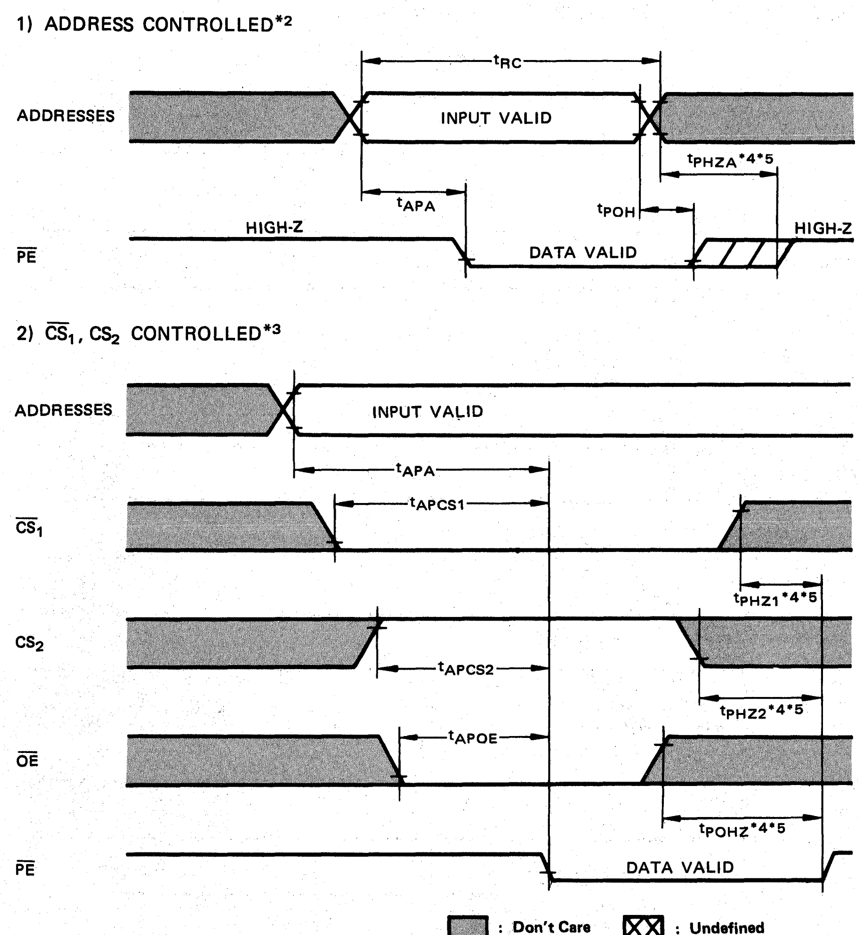
READ CYCLE: $\overline{CS}_1$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

7

PARITY READ FUNCTION TIMING DIAGRAM*1,6



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1}$ = "L", CS_2 = "H" and $\overline{OE}$ = "L".
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.
*6 When error occurred, $\overline{PE}$ pin outputs "L". But when no error, $\overline{PE}$ pin is in High-Z state.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE*1,*6,*7

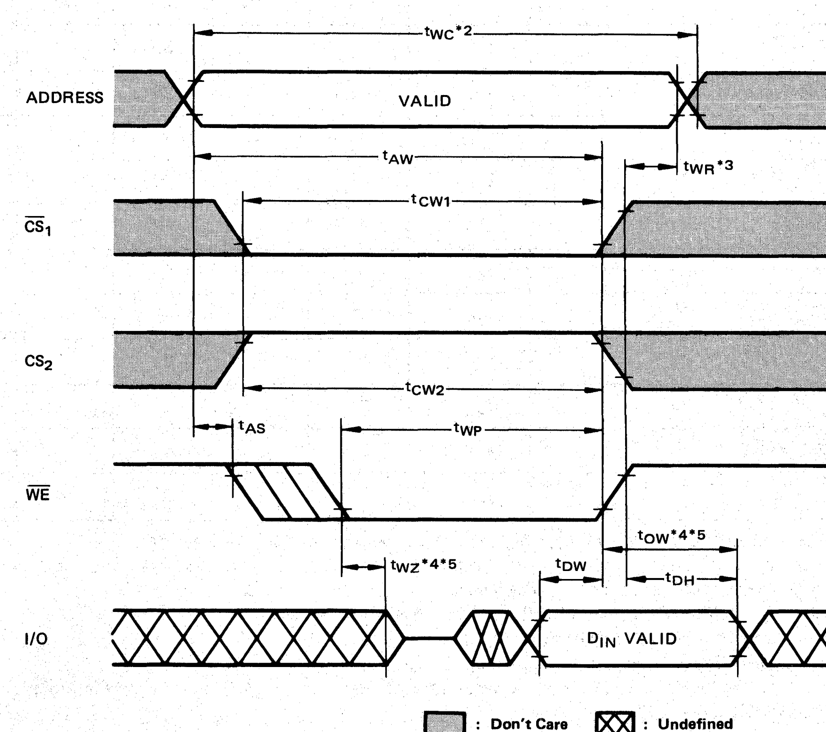
Parameter	Symbol	MB8287-25		MB8287-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	18		28		ns
$\overline{CS}_1$ to End of Write	t_{CW1}	16		26		ns
CS_2 to End of Write	t_{CW2}	13		20		ns
Data Setup Time	t_{DW}	8		12		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Write Recovery Time*3	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$*4*5	t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$*4*5	t_{WZ}	0	8	0	14	ns

Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.
*6 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*7 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

7

WRITE CYCLE TIMING DIAGRAM *1,*6,*7

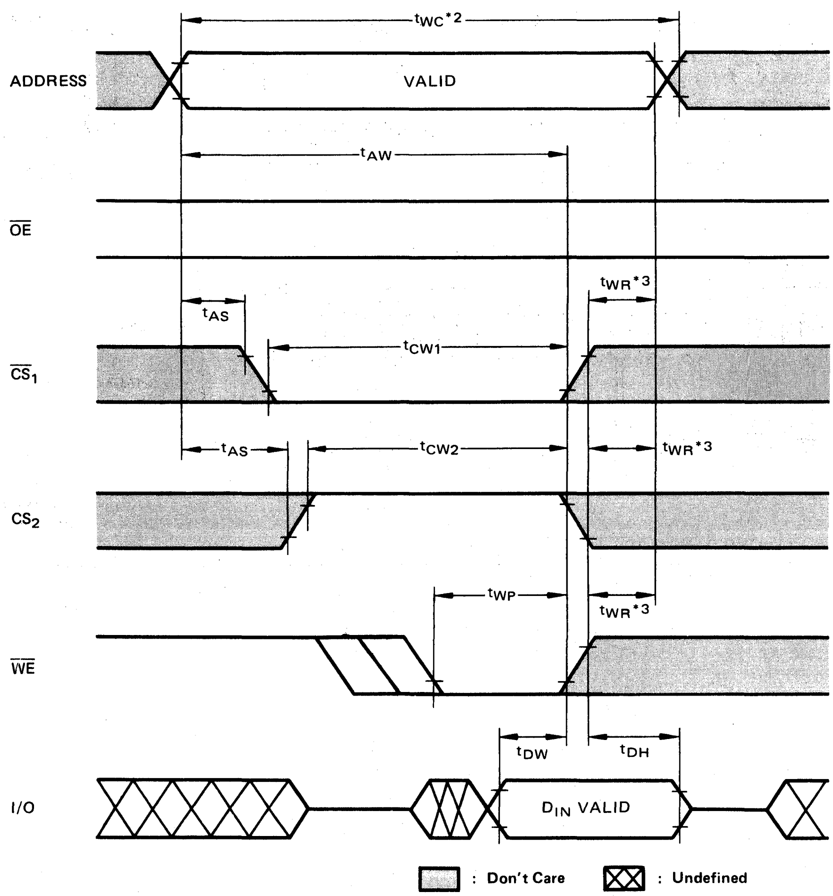
WRITE CYCLE No. 1 ($\overline{WE}$ CONTRORRED)



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.
*6 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*7 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

WRITE CYCLE TIMING DIAGRAM *1,*6,*7

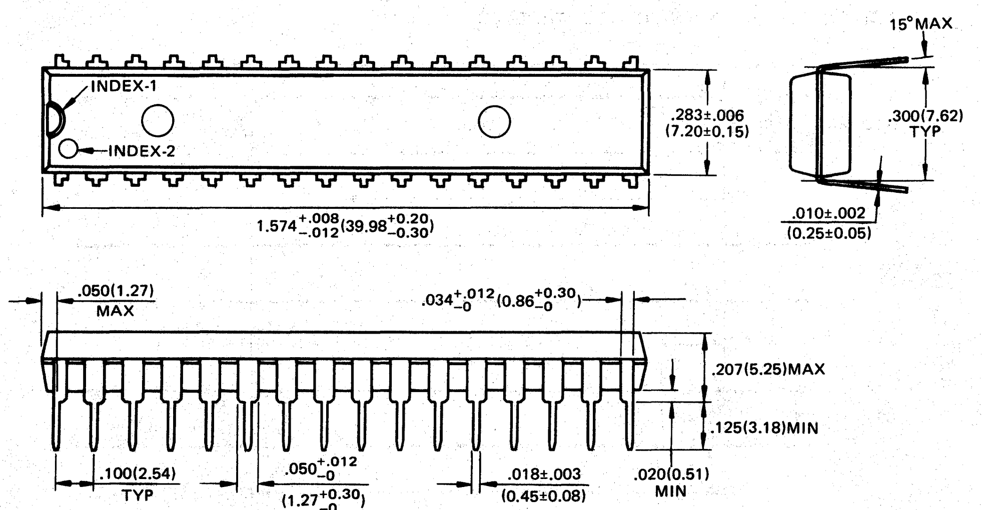
WRITE CYCLE No. 2 ($\overline{CS}_1$, CS2 CONTROLLED)



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.
*6 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*7 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

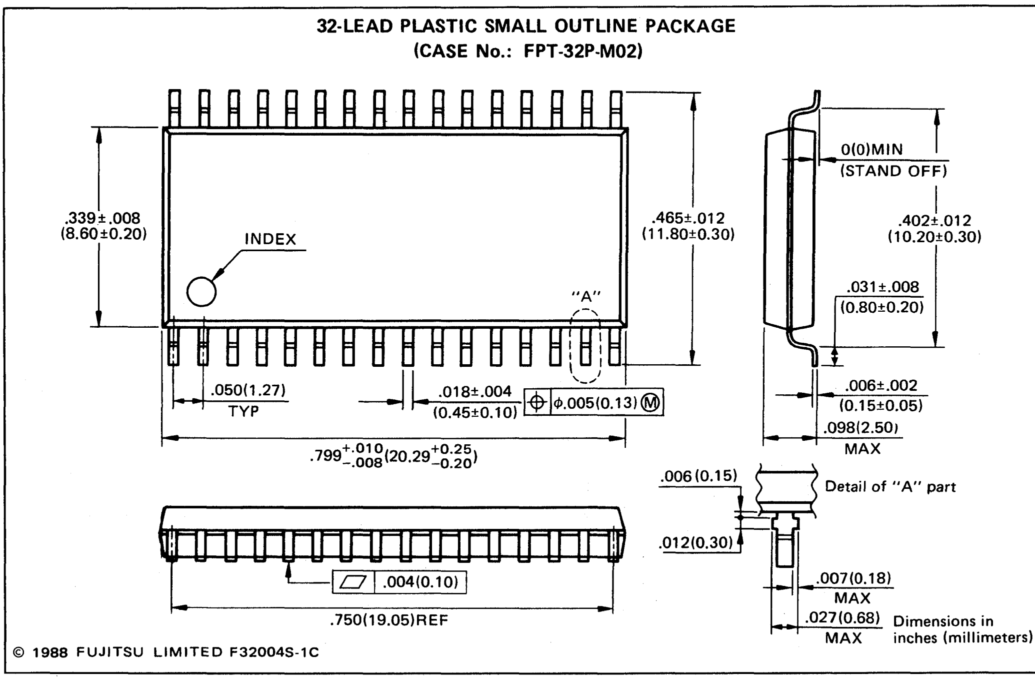
PACKAGE DIMENSIONS

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (continued)



FUJITSU

CMOS 73728-BIT STATIC RANDOM ACCESS MEMORY

MB82T790-20
MB82T790-25

September 1988
Edition 1.0

PRELIMINARY

72K-BIT (8192 x 9) SYNCHRONOUS CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

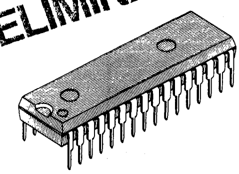
The Fujitsu MB82T790 is a 8,192-words by 9-bits synchronous static random access memory fabricated with a CMOS silicon gate process.

Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK pin therefore external control of write pulse width is not necessary. Compared to the traditional RAM, MB82T790 drastically improves the system level cycle time because signal skews are not necessarily concerned.

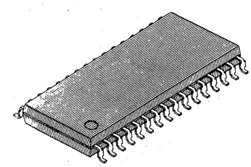
The MB82T790 has a 32-pin plastic skinny DIP package and 32-pin plastic flat package as package options.

All pins are TTL compatible, and a single +5V power supply is required.

- 8,192 words x 9 bits organization
- Fast access time:
  - t_{ACL} = 20ns max. / t_{ACS2} = t_{PE2} = 10ns max. (MB82T790-20)
  - t_{ACL} = 25ns max. / t_{ACS2} = t_{PE2} = 12ns max. (MB82T790-25)
- Registered addresses, $\overline{CS_1}$, $\overline{WE}$ and Data inputs
- Write cancel function by asynchronous CS_2 pin
- On-chip write pulse generator
- On-chip parity checker
- CMOS peripheral
- Single = 5V (±10%) power supply with low current drain
  - Active operation = 90mA max.
  - Standby operation = 15mA max.
- Common data inputs/outputs
- TTL compatible inputs/outputs
- Three-state data output and open drain parity error output
- Standard 32-pin plastic DIP package: (Suffix P, SK)
  Standard 32-pin plastic flat package (Suffix PF)



PLASTIC PACKAGE DIP-32P-M02



PLASTIC PACKAGE FPT-32P-M02

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	$V_{I/O}$	–0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature Range	T_{STG}	–40 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

(TOP VIEW)

A_3	1	32	V_{CC}
A_4	2	31	A_2
A_5	3	30	A_1
A_6	4	29	A_0
A_7	5	28	$\overline{CLR}$
A_8	6	27	CLK
A_9	7	26	INH
A_{10}	8	25	$\overline{CS_1}$
A_{11}	9	24	$\overline{WE}$
A_{12}	10	23	CS_2
I/O_1	11	22	$\overline{PE}$
I/O_2	12	21	I/O_9
I/O_3	13	20	I/O_8
I/O_4	14	19	I/O_7
I/O_5	15	18	I/O_6
GND	16	17	GNDQ

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

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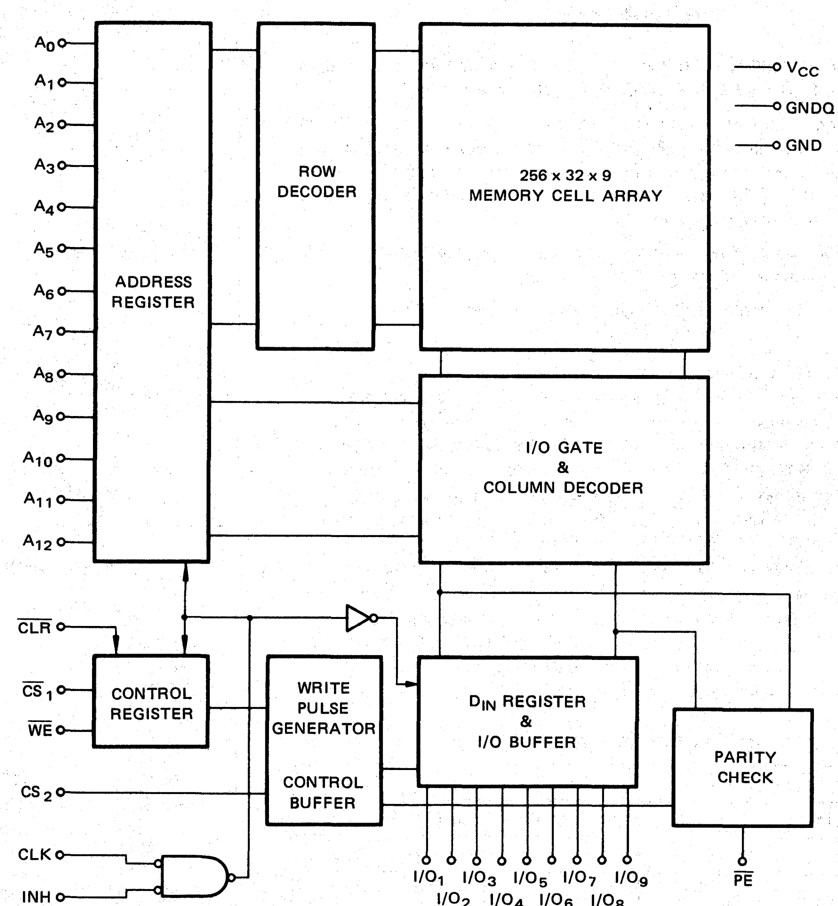
Fig. 1 – MB82T790 BLOCK DIAGRAM



CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

PIN DESCRIPTION

Symbol	Pin name	Input/ Output	Function
CLK	Clock	Input	Address, $\overline{CS}_1$ and $\overline{WE}$ are fetched at the rising edge of the CLK, and D_{IN} is fetched at falling edge of the CLK.
INH	Inhibit	Input	While INH = "H", a low level of CLK is disabled.
$\overline{CLR}$	Clear	Input	When $\overline{CLR}$ = "L", the contents of $\overline{CS}_1$ and $\overline{WE}$ register are cleared to standby.
A_0 to A_{12}	Address Input	Input	Synchronous address inputs.
$\overline{CS}_1$	Chip Select 1	Input	Synchronous Chip Select 1 ($\overline{CS}_1$) input. (This pin can be used as power down.)
CS_2	Chip Select 2	Input	Asynchronous high-speed Chip Select 2 (CS_2) input. (This pin can be used as write cancel.)
$\overline{WE}$	Write Enable	Input	Synchronous Write Enable ($\overline{WE}$) input.
I/O_1 ot I/O_9	Data Input/Output	Input/ Output	Data inputs/outputs. (Synchronous data inputs/Asynchronous data outputs)
$\overline{PE}$	Parity Error	Output	Asynchronous parity error output: $\overline{PE}$ output remains High-Impedance state through undefined area.
V_{CC}	Power Supply	–	+5V ±10% power supply.
GNDQ	Ground for Output	–	Ground for output circuits.
GND	Ground for Others	–	Ground for other circuits.

TRUTH TABLE

$\overline{CLR}$	$\overline{CS}_1$	CS_2	$\overline{WE}$	MODE	I/O PIN	$\overline{PE}$ OUTPUT PIN	SUPPLY CURRENT
L	X	X	X	STANDBY	HIGH-Z	HIGH-Z	STANDBY
H	H	X	X	STANDBY	HIGH-Z	HIGH-Z	STANDBY
H	L	L	X	CHIP DISABLE	HIGH-Z	HIGH-Z	ACTIVE
H	L	H	H	READ	D_{OUT}	$\overline{PE}$ OUTPUT	ACTIVE
H	L	H	L	WRITE	D_{IN}	HIGH-Z	ACTIVE

Legend: H = High level, L = Low level, X = Don't care.
Notes: $\overline{CS}_1$ and $\overline{WE}$ are input at the rising edge of the CLK.
$\overline{PE}$ output remains High-Impedance state through undefined area.

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RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

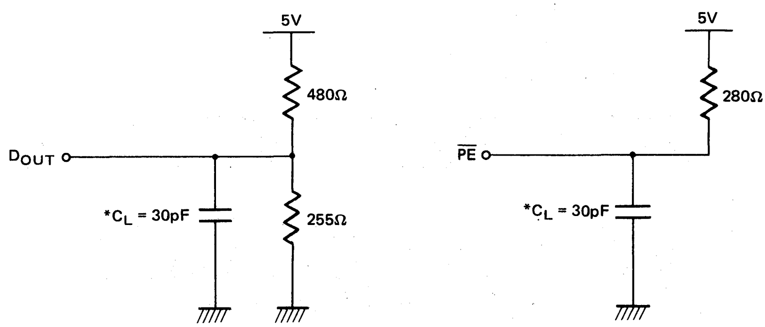
(Recommended operating conditions otherwise noted.)

Parameter		Test Conditions	Symbol	Min	Max	Unit
Standby Supply Current		$\overline{CS}_1 = V_{IH}$	I_{SB}		15	mA
Operating Supply Current		$\overline{CS}_1 = V_{IL}$, I/O = Open Cycle = min.	I_{CC}		90	mA
Input Leakage Current		V_{IN} = GND to V_{CC}	I_{LI}	−10	10	μA
Output Leakage Current		$\overline{CS}_1 = V_{IH}$ or $CS_2 = V_{IL}$ V_{OUT} = GND to V_{CC}	$I_{LI/O}$	−10	10	μA
Input Low Voltage			V_{IL}	−2.0*1	0.8	V
Input High Voltage			V_{IH}	2.2	6.0	V
Output High Voltage		I_{OH} = −4mA	V_{OH}	2.4		V
Output Low Voltage	D_{OUT}	I_{OL} = 8mA	V_{OL}		0.4	V
	$\overline{PE}$	I_{OL} = 16mA				
Peak Power-on Current*2		V_{CC} = GND to 4.5V $\overline{CLR}$ = GND	I_{PO}		90	mA

Note: *1 −2.0V Min. for pulse width less than 20ns. (V_{IL} = −0.3V at DC level)
*2 The $\overline{CLR}$ input should be connected to GND to keep the device deselected.

Fig. 2 — AC TEST CONDITIONS

- INPUT PULSE LEVELS: 0.6V TO 2.4V
- TIMING REFERENCE LEVELS: INPUT: V_{IL} = 0.8V, V_{IH} = 2.2V
  OUTPUT: V_{OL} = 0.8V, V_{OH} = 2.2V
- OUTPUT LOAD



*INCLUDING JIG AND STRAY CAPACITANCE.

(C_L = 5pF for t_{LZ}, t_{HZ}, t_{LZ2}, t_{HZ2} and t_{CRHZ}) (C_L = 5pF for t_{PLZ}, t_{PHZ}, t_{PLZ2}, t_{PHZ2} and t_{CRHZ})

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter		Symbol	MB82T790-20		MB82T790-25		Unit
			Min	Max	Min	Max	
Read Cycle Time	When no uses $\overline{PE}$	t_{RC}	20		25		ns
	When uses $\overline{PE}$	t_{RC}	25		30		ns
Clock "H" Level Pulse Width		t_{CLH}	8		10		ns
Clock "L" Level Pulse Width		t_{CLL}	8		10		ns
Input Setup Time		t_S	4		4		ns
Input Hold Time		t_H	2		2		ns
Clock Access Time	D_{OUT}	t_{ACL}		20		25	ns
	$\overline{PE}$	t_{PE}		25		30	ns
CS_2 Access Time	D_{OUT}	t_{ACS2}		10		12	ns
	$\overline{PE}$	t_{PE2}		10		12	ns
CS_2 to Output Low-Z	D_{OUT}	t_{LZ2}	2		2		ns
	$\overline{PE}$	t_{PLZ2}	2		2		ns
CS_2 to Output High-Z	D_{OUT}	t_{HZ2}	2	8	2	10	ns
	$\overline{PE}$	t_{PHZ2}	2	8	2	10	ns
Output Hold from Clock	D_{OUT}	t_{OH}	2		2		ns
	$\overline{PE}$	t_{PH}	2		2		ns
Output Hold from CS_2	D_{OUT}	t_{OH2}	2		2		ns
	$\overline{PE}$	t_{PH2}	2		2		ns

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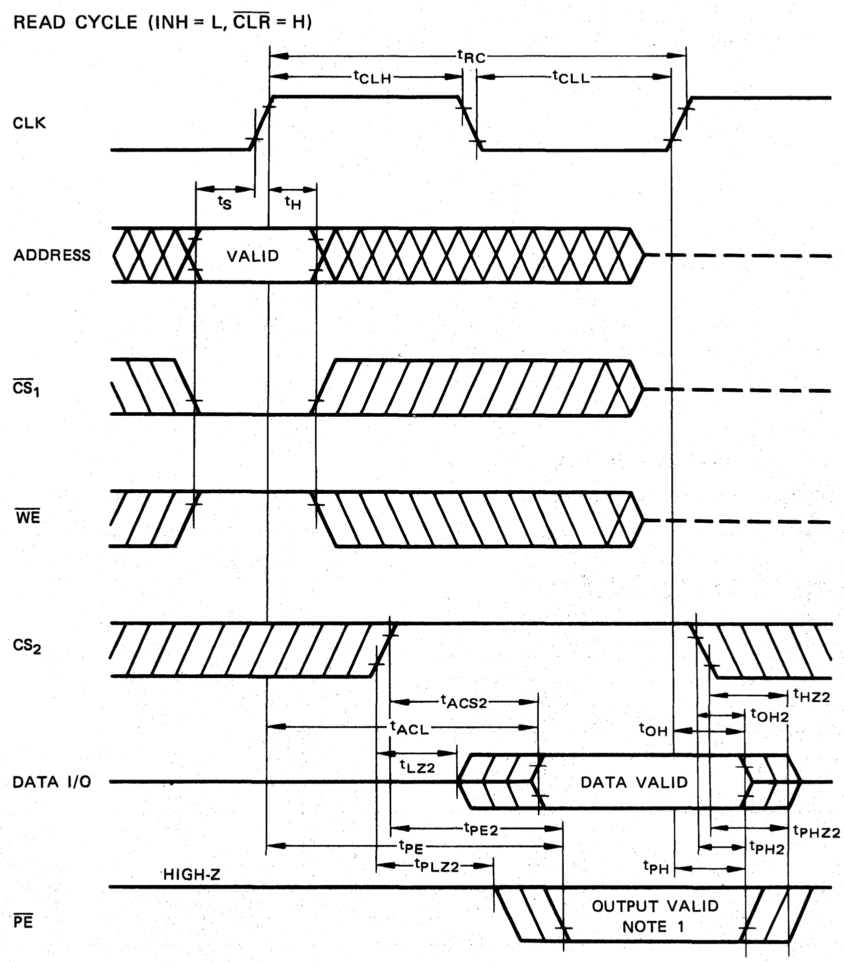
READ CYCLE TIMING DIAGRAM



Note 1: $\overline{PE}$ output remains High-Impedance state through undefined area.

WRITE CYCLE

Parameter		Symbol	MB82T790-20		MB82T790-25		Unit
			Min	Max	Min	Max	
Write Cycle Time		t_{WC}	20		25		ns
Clock "H" Level Pulse Width		t_{CLH}	8		10		ns
Clock "L" Level Pulse Width		t_{CLL}	8		10		ns
Input Setup Time		t_S	4		4		ns
Input Hold Time		t_H	2		2		ns
CS_2 Setup Time		t_{CS}	2		2		ns
CS_2 Hold Time		t_{CH}	8		10		ns
Data Setup Time		t_{DS}	0		0		ns
Data Hold Time		t_{DH}	6		6		ns
CLK to Output High-Z	D_{OUT}	t_{HZ}	2	8	2	10	ns
	$\overline{PE}$	t_{PHZ}	2	8	2	10	ns
CLK to Output Low-Z	D_{OUT}	t_{LZ}	2		2		ns
	$\overline{PE}$	t_{PLZ}	2		2		ns

CLOCK INHIBIT TIMING

Parameter	Symbol	MB82T790-20		MB82T790-25		Unit
		Min	Max	Min	Max	
Clock Inhibit Setup Time	t_{CLIS}	2		2		ns
Clock Inhibit Hold Time	t_{CLIH}	2		2		ns
Clock Enable Setup Time	t_{CLES}	2		2		ns
Clock Enable Hold Time	t_{CLEH}	0		0		ns

REGISTOR CLEAR TIMING

Parameter	Symbol	MB82T790-20		MB82T790-25		Unit
		Min	Max	Min	Max	
Clear Pulse Width	t_{CRW}	7		7		ns
Clear Hold Time	t_{CRH}	10		10		ns
Clear Recovery Time	t_{CRR}	10		10		ns
Clear to Output High-Z	t_{CRHZ}	2	8	2	10	ns

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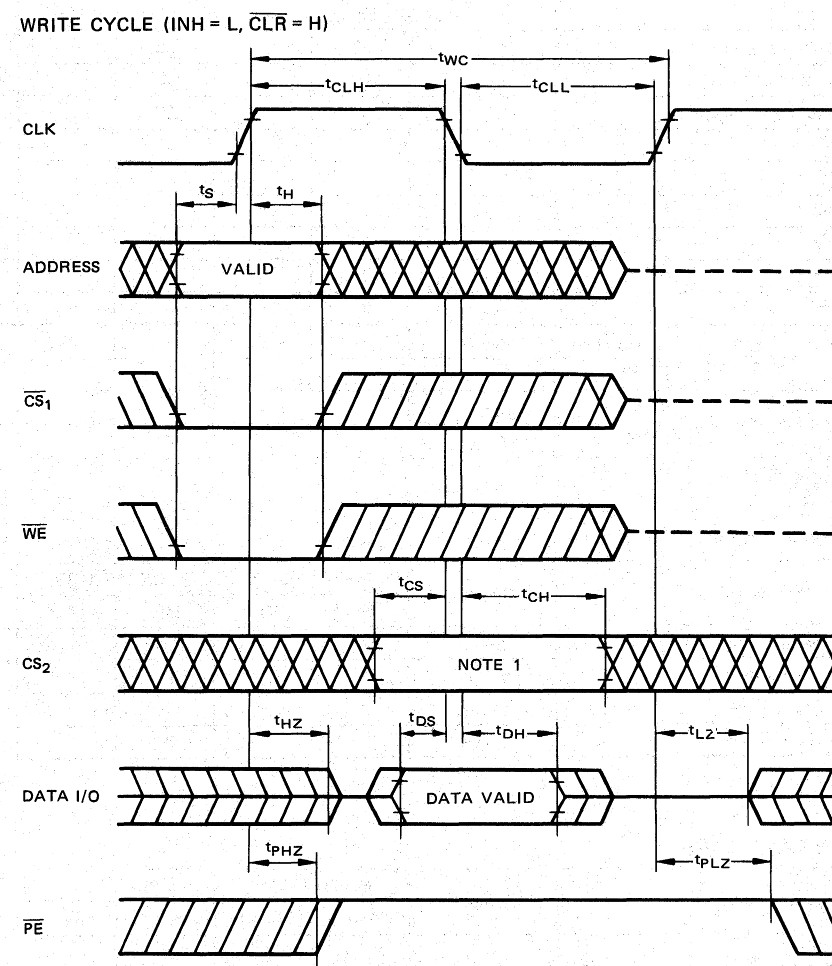
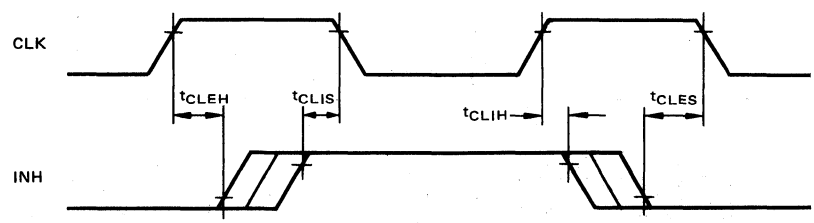
WRITE CYCLE TIMING DIAGRAM



Note 1: When CS_2 = H level, write operation is excuted and when CS_2 = L level, write operation is cancelled.

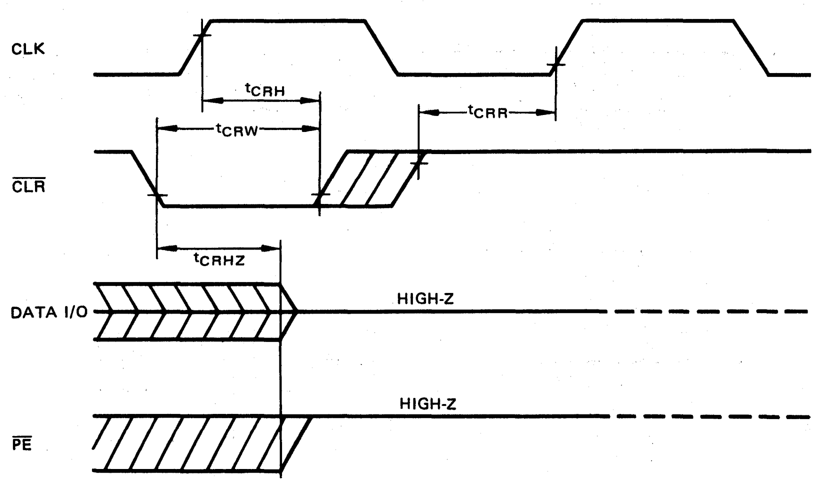
CLOCK INHIBIT TIMING DIAGRAM

CLOCK INHIBIT



REGISTER CLEAR TIMING

REGISTER CLEAR



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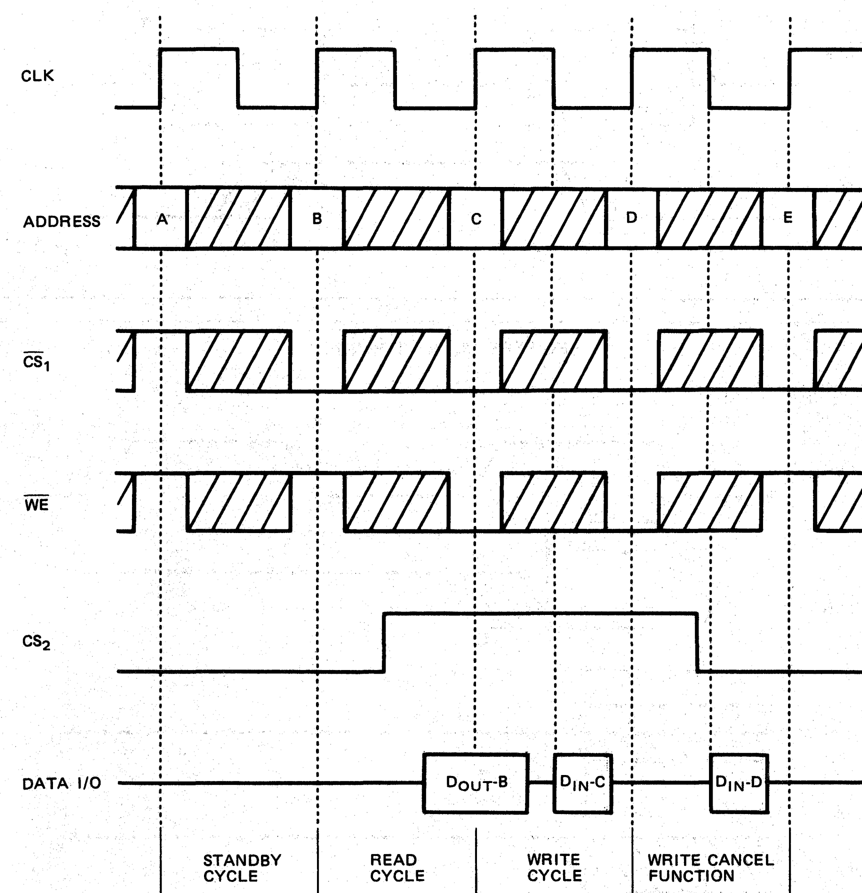
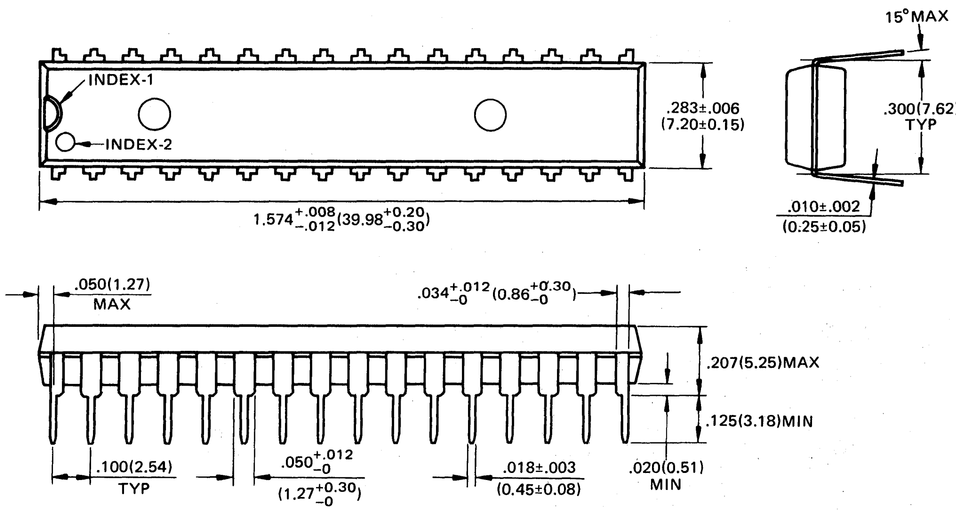
EXAMPLE OF MB82T790 BASIC FUNCTION



PACKAGE DIMENSIONS

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)



Dimensions in inches (millimeters)

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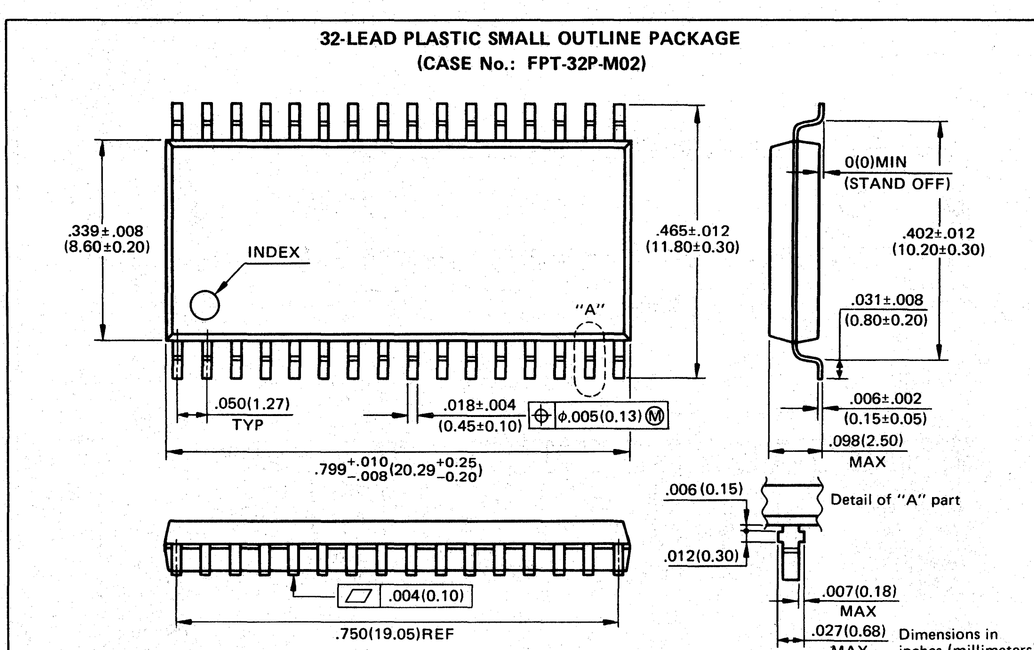
PACKAGE DIMENSIONS (continued)



$.799^{+.010}_{-.008}(20.29^{+0.25}_{-0.20})$

FUJITSU

CMOS TAG RANDOM ACCESS MEMORY

MB81C51-25
MB81C51-30

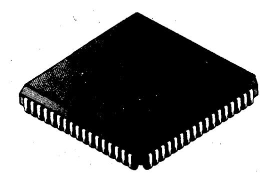
November 1988
Edition 1.0

CMOS TAG RANDOM ACCESS MEMORY

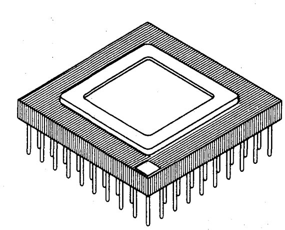
The Fujitsu MB81C51 is 512 entry x 4 way/1024 entry x 2 way TAG Random Access Memory (TAG RAM) fabricated with a CMOS technology.

MB81C51 has been developed aiming to be used in an easily handled cache system with the other DATA RAMs (ex. MB81C79A). Especially this device offers the advantages on designing compact and high performance cache system which will be used in a system adopting 32-bit CPU.

- Organization: 512 Entry x 4 Way or 1024 Entry x 2 Way
- Fast access time: 25/30 ns max from Address Inputs; 18 ns max from Compare Data Inputs
- Power Consumption: 1100mW max.
- Single +5 V supply ±10% tolerance
- TTL compatible inputs and outputs
- LRU (Least Recently Used) Replacement Logic
- Purge Function (All-purge & Partial-purge)
- Internal Parity Generator/Checker
- 64 pin Pin-Grid-Array (Suffix: CR)
- 68 pin Plastic LCC (Suffix: PD)



LCC-68P-M01
(PLASTIC PACKAGE)



PGA-64C-A02
(PIN GRID ARRAY)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	-3.0 to +7.0	V
Output Voltage on any pin with respect to GND		V_{OUT}	-0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.5	W
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	Ceramic	T_{STG}	-65 to +125	°C
	Plastic		-45 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB81C51 BLOCK DIAGRAM 1

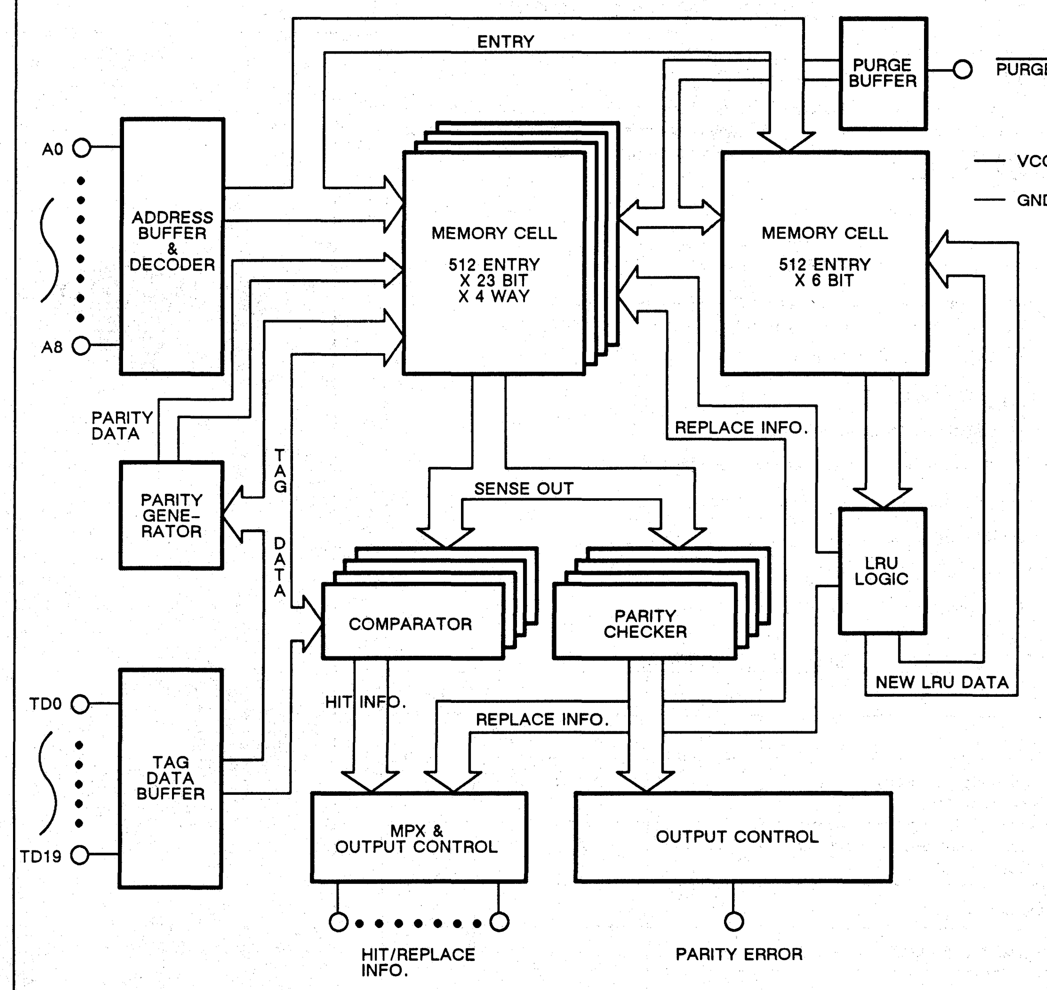
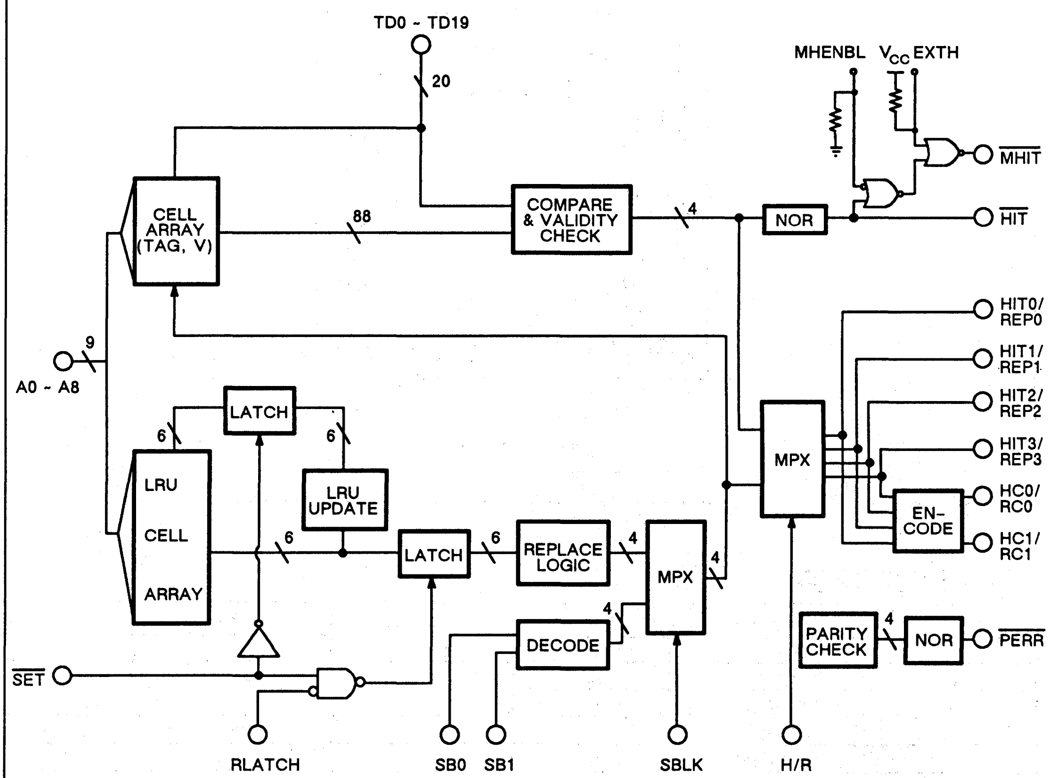


Fig. 2 — MB81C51 BLOCK DIAGRAM 2



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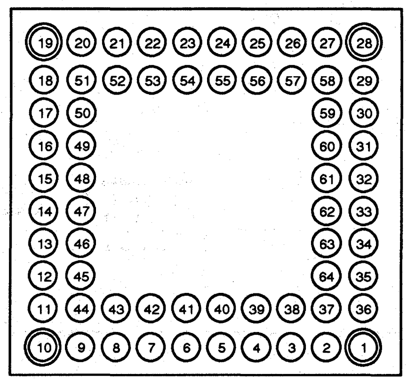
CAPACITANCE (TA = 25°C, f = 1 MHZ)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0V)	CIN		10	pF

PIN ASSIGNMENT

64 PIN PIN GRID ARRAY(PGA-64C-A02)

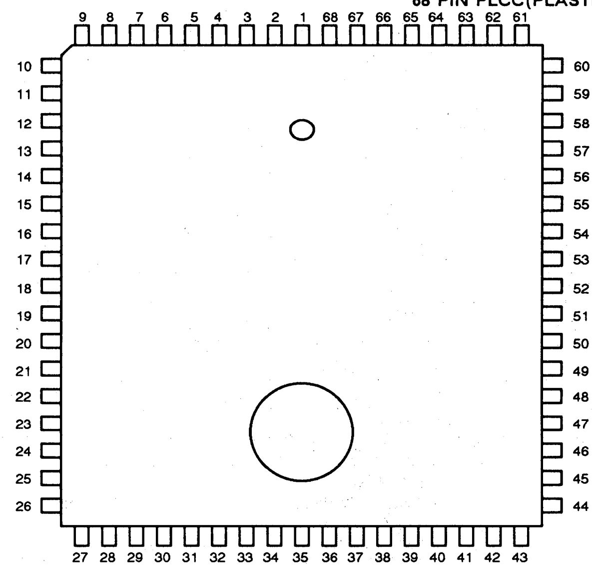


BOTTOM VIEW

PIN FUNCTION

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N.C.	23	A4	45	TD6
2	$\overline{\text{MHIT}}$	24	A5	46	TD9
3	HIT0/REP0	25	A7	47	Vcc
4	HIT2/REP2	26	A9	48	TD13
5	HIT3/REP3	27	N.C.	49	TD15
6	TD0	28	N.C.	50	TD17
7	TD2	29	$\overline{\text{PINV}}$	51	TD19
8	EXTH	30	SBLK	52	A0
9	MHENBL	31	SB1	53	A2
10	N.C.	32	$\overline{\text{INH}}$	54	GND
11	TD7	33	$\overline{\text{INVL}}$	55	A6
12	TD8	34	$\overline{\text{SET}}$	56	A8
13	TD10	35	H/R	57	$\overline{\text{PURGE}}$
14	TD11	36	$\overline{\text{HIT}}$	58	MODE
15	TD12	37	HC0/RC0	59	$\overline{\text{VINV}}$
16	TD14	38	HC1/RC1	60	SB0
17	TD16	39	HIT1/REP1	61	Vcc
18	TD18	40	GND	62	$\overline{\text{WRITE}}$
19	N.C.	41	TD1	63	RLATCH
20	N.C.	42	TD3	64	$\overline{\text{PERR}}$
21	A1	43	TD4		
22	A3	44	TD5		

PIN ASSIGNMENT 68 PIN PLCC(PLASTIC LEAD CHIP CARRIER)



TOP VIEW

PIN FUNCTION (continued)

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	GND	24	TD17	47	$\overline{PINV}$
2	TD0	25	TD18	48	SBLK
3	TD1	26	TD19	49	SB0
4	TD2	27	N.C.	50	SB1
5	TD3	28	N.C.	51	$\overline{INH}$
6	EXTH	29	N.C.	52	Vcc
7	TD4	30	A0	53	$\overline{INV}$
8	N.C.	31	A1	54	$\overline{WRITE}$
9	N.C.	32	A2	55	$\overline{SET}$
10	MHENBL	33	A3	56	RLATCH
11	TD5	34	A4	57	H/R
12	TD6	35	GND	58	$\overline{PERR}$
13	TD7	36	A5	59	$\overline{HIT}$
14	TD8	37	A6	60	HC0/RC0
15	TD9	38	A7	61	N.C.
16	TD10	39	A8	62	N.C.
17	TD11	40	A9	63	HC1/RC1
18	Vcc	41	N.C.	64	$\overline{MHIT}$
19	TD12	42	N.C.	65	HIT0/REP0
20	TD13	43	N.C.	66	HIT1/REP1
21	TD14	44	$\overline{PURGE}$	67	HIT2/REP2
22	TD15	45	$\overline{MODE}$	68	HIT3/REP3
23	TD16	46	$\overline{VINV}$		

PIN DESCRIPTION

OUTPUTS

$\overline{HIT}$	HIT OUTPUT. "NOR" OF HIT0 TO HIT3
HCn/RCn	CODED OUTPUTS OF HIT OR REPLACE INFORMATION (n = 0 ~ 1)
HITn/REPn	UNCODED OUTPUTS OF HIT OR REPLACE INFORMATION (n = 0 ~ 3)
$\overline{PERR}$	PARITY ERROR
$\overline{MHIT}$	HIT OUTPUT MODIFIED BY MHENBL AND EXTH

INPUTS

MODE	MODE SELECTION MODE = 1 : 512 Entry x 4 Way MODE = 0 : 1024 Entry x 2 Way
A0–A9	ADDRESS INPUTS (A9 is not used for 4 way)
TD0–19	TAG INFORMATION INPUTS
$\overline{PURGE}$	ALL-PURGE TIMING PULSE
$\overline{INVL}$	PARTIAL-PURGE. V-BIT FORCED TO "0". LRU IS REVERSIVELY UPDATED
SBLK	ENABLE WAY-SELECTION EXTERNALLY AT REPLACEMENT AND INVALIDATION
SB0, SB1	EXTERNAL WAY-ADDRESS INPUTS
$\overline{WRITE}$	WRITE CYCLE SIGNAL
$\overline{SET}$	TIMING PULSE Write : Registrate TAG, V-bit "H", LRU update Read : LRU updated PARTIAL PURGE : LRU reversively update, V-bit "L"
$\overline{INH}$	ALL FUNCTIONS EXCEPT PURGE ARE INHIBITED
H/R	OUTPUT SELECTION H/R = 1 : Hit Information H/R = 0 : Replace Information
RLATCH	LATCH CONTROL FOR REPLACE INFORMATION
$\overline{PINV}$	USE FOR "TESTING" ONLY (GENERALLY "H")
$\overline{VINV}$	USE FOR "TESTING" ONLY (GENERALLY "H")
MHENBL	ENABLE $\overline{MHIT}$ OUTPUT
EXTH	FORCE $\overline{MHIT}$ OUTPUT TO "L"

FUNCTION TABLE

1) BASIC FUNCTION (Any combination except below are inhibited.)

Input					TAG Info.	Control Info.		LRU	
$\overline{INH}$	$\overline{PURGE}$	$\overline{SET}$	$\overline{WRITE}$	$\overline{INVL}$	TAG	P bit	V bit	LRU	Function Mode
L	H	X	X	X	N-CNG	N-CNG	N-CNG	N-CNG	INHIBIT[3]
H	H	H	X	X	N-CNG	N-CNG	N-CNG	N-CNG	TAG READ
H	H	⊔	H	H	N-CNG	N-CNG	N-CNG	N-CNG[1] or UP-D	TAG READ
H	H	⊔	L	H	TD0 to TD19	SET	H	UP-D	TAG WRITE
X	L	H	X	X	UNDEFINED	UNDEFINED	L (All)	INCLZ	ALL PURGE
H	H	⊔	H	L	N-CNG	N-CNG	N-CNG/L[2]	N-CNG[1] or RUP-D	PARTIAL PURGE

X : "H" or "L"
N-CNG : No Change   INCLZ : INITIALIZE
UP-D : Up Dated   RUP-D : Reversively Updated
1. When SBLK = "L" and no-HIT, then LRU is no change (N-CNG).
2. When SBLK = "L" and no-HIT, then V-Bit is no change (N-CNG).
3. During INHIBIT mode, $\overline{HIT}$ and $\overline{PERR}$ outputs are "H" but the other outputs are "L".

2) OUTPUT PIN FUNCTION

Input		Internal Info.[1, 2]				Output							
Mode	A9	hit0/ rep0	hit1/ rep1	hit2/ rep2	hit3/ rep3	HIT0/ REP0	HIT1/ REP1	HIT2/ REP2	HIT3/ REP3	HC0/ RC0	HC1/ RC1	[3]/ $\overline{\text{HIT}}$	Mode
H	X	L	L	L	L	L	L	L	L	L	L	H	
H	X	H	L	L	L	H	L	L	L	L	L	L	4
H	X	L	H	L	L	L	H	L	L	H	L	L	W
H	X	L	L	H	L	L	L	H	L	L	H	L	A
H	X	L	L	L	H	L	L	L	H	H	H	L	Y
L	L	L	X	L	X	L	L	L	L	L	L	H	
L	L	H	X	L	X	H	L	L	L	L	L	L	2
L	L	L	X	H	X	L	L	H	L	L	H	L	W
L	H	X	L	X	L	L	L	L	L	L	L	H	A
L	H	X	H	X	L	L	H	L	L	H	L	L	Y
L	H	X	L	X	H	L	L	L	H	H	H	L	

X: "H" or "L"

1. Internal information, rep0 to rep3 are determined by on-chip LRU logic when SBLK = "L". When SBLK = "H", the internal information are determined by external signal of SB0 & SB1.
2. Correct operation is not guaranteed if 2 ways or more become HIT at the same time.
3. Output of $\overline{\text{HIT}}$ is valid when H/R = "H".

3) PARTIAL PURGE ($\overline{\text{INVL}}$ = "L")

INPUT					INTERNAL INFO.				PURGE BLOCK				$\overline{\text{SET}}$	
					HIT				BLOCK					
MODE	A9	SBLK	SB0	SB1	0	1	2	3	0	1	2	3	LRU	MODE
H	X	L	X	X	L	L	L	L	—	—	—	—	---	
H	X	L	X	X	H	L	L	L	Q	—	—	—	RUP-D	4
H	X	L	X	X	L	H	L	L	—	Q	—	—	RUP-D	
H	X	L	X	X	L	L	H	L	—	—	Q	—	RUP-D	W
H	X	L	X	X	L	L	L	H	—	—	—	Q	RUP-D	A
H	X	H	L	L	X	X	X	X	Q	—	—	—	RUP-D	Y
H	X	H	H	L	X	X	X	X	—	Q	—	—	RUP-D	
H	X	H	L	H	X	X	X	X	—	—	Q	—	RUP-D	
H	X	H	H	H	X	X	X	X	—	—	—	Q	RUP-D	
L	L	L	X	X	L	X	L	X	—	—	—	—	---	
L	L	L	X	X	H	X	L	X	Q	—	—	—	RUP-D	
L	L	L	X	X	L	X	H	X	—	—	Q	—	RUP-D	2
L	L	H	L	L	X	X	X	X	Q	—	—	—	RUP-D	
L	L	H	L	H	X	X	X	X	—	—	Q	—	RUP-D	W
L	H	L	X	X	X	L	X	L	—	—	—	—	---	A
L	H	L	X	X	X	H	X	L	—	Q	—	—	RUP-D	Y
L	H	L	X	X	X	L	X	H	—	—	—	Q	RUP-D	
L	H	H	H	L	X	X	X	X	—	Q	—	—	RUP-D	
L	H	H	H	H	X	X	X	X	—	—	—	Q	RUP-D	

Note: Correct operation is not guaranteed if 2 ways or more become HIT at the same time.

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4) PARITY ERROR & V-BIT[1] (n : 0 to 3)

pen	vn0	vn1	PEn	HIT Info.[2]
L	L	L	L	---
L	L	H	H	HIT
L	H	L	H	HIT
L	H	H	L	HIT
H	L	L	L	---
H	L	H	H	HIT
H	H	L	H	HIT
H	H	H	H	HIT

1. $\overline{PERR}$ is "NOR" of PE0 to PE3
2. Output information when internal "HIT" is valid.

pen : Internal parity error of way "n"
vn0/vn1 : Duplicate validity bits.
PEn : Determined by the following equation.

$$PEn = (vn0 + vn1) \bullet pen + (vn0 \oplus vn1)$$

BASIC FUNCTIONS

TAG READ

A comparison between the TAG input data (TD0-19) and the contents of the addressed location is performed. If both data are the same, that is "FOUND". Then $\overline{HIT}$ will be "LOW" and outputs of HCn, HITn indicate hitted "Associative way". In the case of "NOT-FOUND", the TAG RAM will specify the "way", which should be replaced, by using the LRU logic automatically.

The replacement information will be presented at the outputs of RCn and REPn by forcing the H/R input into "LOW". These signals will be latched and used for the data Memory move-in operation.

TAG WRITE

When "NOT-FOUND" is occurred, the TAG-RAM also should be updated. The write operation is performed by $\overline{WRITE}$ "LOW" and $\overline{SET}$ pulse input. The TAG data will be written into the proper "way" by the internal LRU logic.

TAG-WRITE mode, V-bit (Validity bit) and the parity are set, and LRU logic is updated.

On the other hand, it will be able to specify the "way" externally by using SBLK, SB0 and SB1 inputs.

ALL PURGE

By asserting $\overline{PURGE}$ input "LOW", the V-bit are reset and LRU logic is initialized.

In this operation, the contents of each TAG and its parity will not be identified.

PARTIAL PURGE

The partial purge operation is performed by $\overline{INVL}$ "LOW" and $\overline{SET}$ pulse input.

The V-bit, which is specified by the address inputs, will be reset, and LRU logic will be reversively updated.

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.5*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

Note:
*-3.0V min. for pulse width less than 20ns.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	-10	10	µA
Operating Supply Current	D_{OUT} = Open, Cycle = min.	I_{CC}		200	mA
Output Low Voltage	I_{OL} = 8mA	V_{OL}		0.4	V
Output High Voltage	I_{OH} = -4mA	V_{OH}	2.4		V

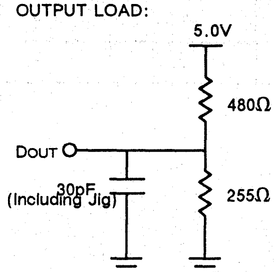
Fig. 3 — AC TEST CONDITION

INPUT PULSE LEVELS : 0.0V to 3.0V

INPUT PULSE RISE AND FALL TIMES: 5ns (Transient time between 0.8V and 2.2V)

TIMING REFERENCE LEVELS : Input : 1.5V
Output : 1.5V

OUTPUT LOAD:



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

TAG READ CYCLE (MODE = "H" or "L", $\overline{PURGE}$ = "H", $\overline{WRITE}$ = "H", $\overline{INVL}$ = "H", $\overline{PINV}$ = "H", or "L", $\overline{VINV}$ = "H" or "L", $\overline{INH}$ = "H")

Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	50		50		ns
Address Valid to $\overline{HIT}$, HCn, HITn	t_{AH}		25		30	ns
Address Valid to $\overline{MHIT}$	t_{AMH}		27		32	ns
TAG Data Valid to $\overline{HIT}$, HCn, HITn	t_{TH}		18		18	ns
TAG Data Valid to $\overline{MHIT}$	t_{TMH}		20		20	ns
$\overline{HIT}$, HCn, HITn Hold Time	t_{HH}	0		0		ns
Address Valid to RCn, REPn	t_{AR}		35		40	ns
Address Valid to $\overline{PERR}$	t_{AP}		35		40	ns
Address Setup Time for $\overline{SET}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{SET}$	t_{TS}	25		25		ns
$\overline{SET}$ Pulse Width	t_{SW}	20		20		ns
$\overline{SET}$ Recovery Time	t_{SR}	5		5		ns
RLATCH Setup Time	t_{RLS}	10		10		ns
RCn, REPn Hold Time for RLATCH	t_{RH}	0		0		ns
SBLK, SB0, SB1 Setup Time for RCn, REPn	t_{SBR}		25		25	ns
SBLK, SB0, SB1 Hold Time	t_{SBH}	5		5		ns
RCn, REPn Hold Time for SBLK, SB0, SB1	t_{SH}	0		0		ns
SBLK, SB0, SB1 Setup Time for $\overline{SET}$	t_{SBS}	25		25		ns
$\overline{PERR}$ Hold Time	t_{PH}	0		0		ns
H/R to Multiplex output change	t_{HR}		10		12	ns
MHENBL, EXTH to $\overline{MHIT}$ output	t_{MMH}		10		12	ns

TAG WRITE CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "L", $\overline{\text{INVL}}$ = "H", H/R = "L", $\overline{\text{INH}}$ = "H")

Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	50		50		ns
Address Valid to RC$_n$, REP$_n$	t_{AR}		35		40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
RLATCH Setup Time	t_{RLS}	10		10		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
SBLK, SB0, SB1 Setup Time for PC$_n$, REP$_n$	t_{SBR}		25		25	ns
PC$_n$, REP$_n$ Hold Time for SBLK, SB0, SB1	t_{SH}	0		0		ns
SBLK Hold Time	t_{SBH}	5		5		ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Setup Time for $\overline{\text{SET}}$	t_{IS}	25		25		ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Recovery Time for $\overline{\text{SET}}$	t_{IR}	5		5		ns

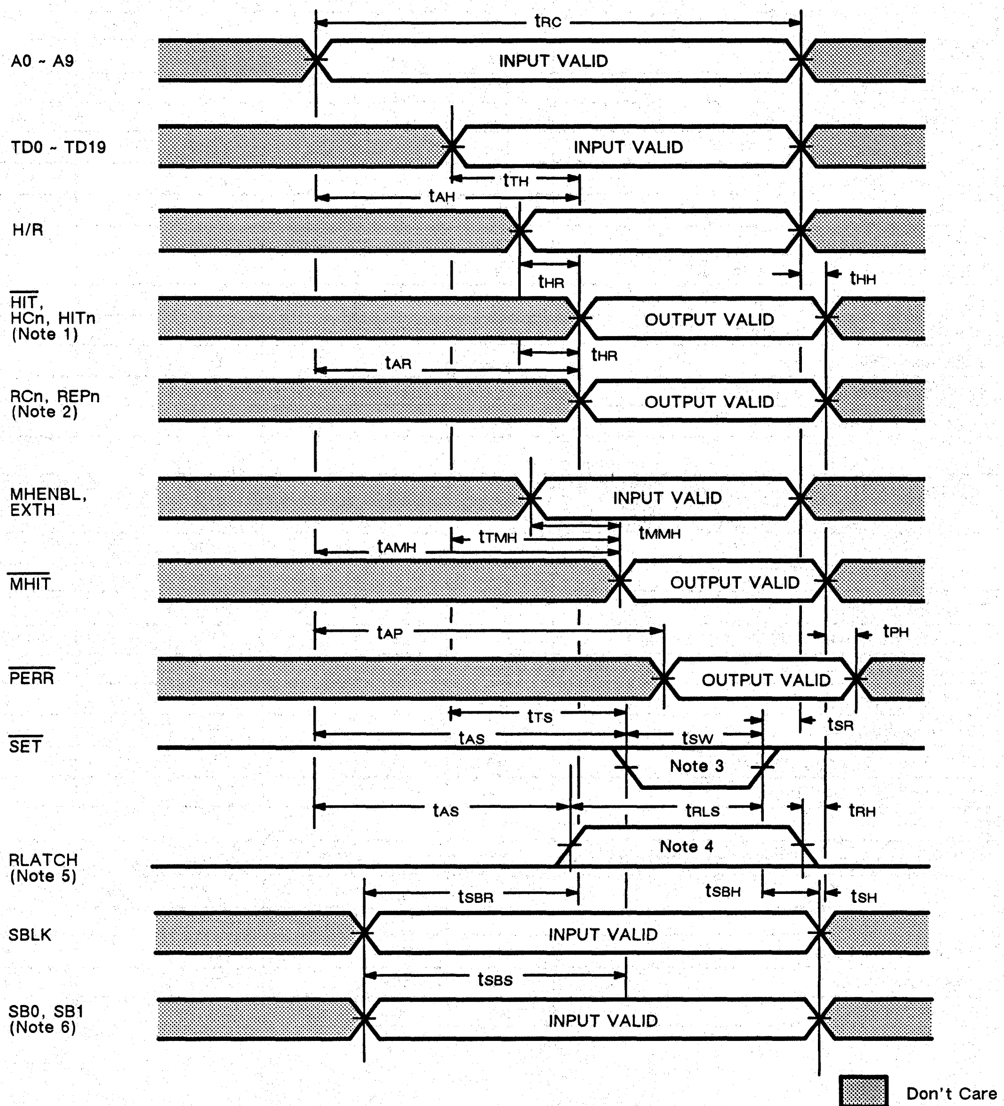
PERTIAL PURGE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "L", H/R = "H" or "L", $\overline{\text{INH}}$ = "H", RLATCH = "L", $\overline{\text{PINV}}$= "H" or "L", $\overline{\text{VINV}}$ = "H" or "L")

Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Pertial Purge Cycle	t_{PPC}	50		50		ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
SBLK, SB0, SB1 Hold Time	t_{SBH}	5		5		ns

ALL PURGE ($\overline{\text{SET}}$ = "H", Other control inputs are "H" or "L")

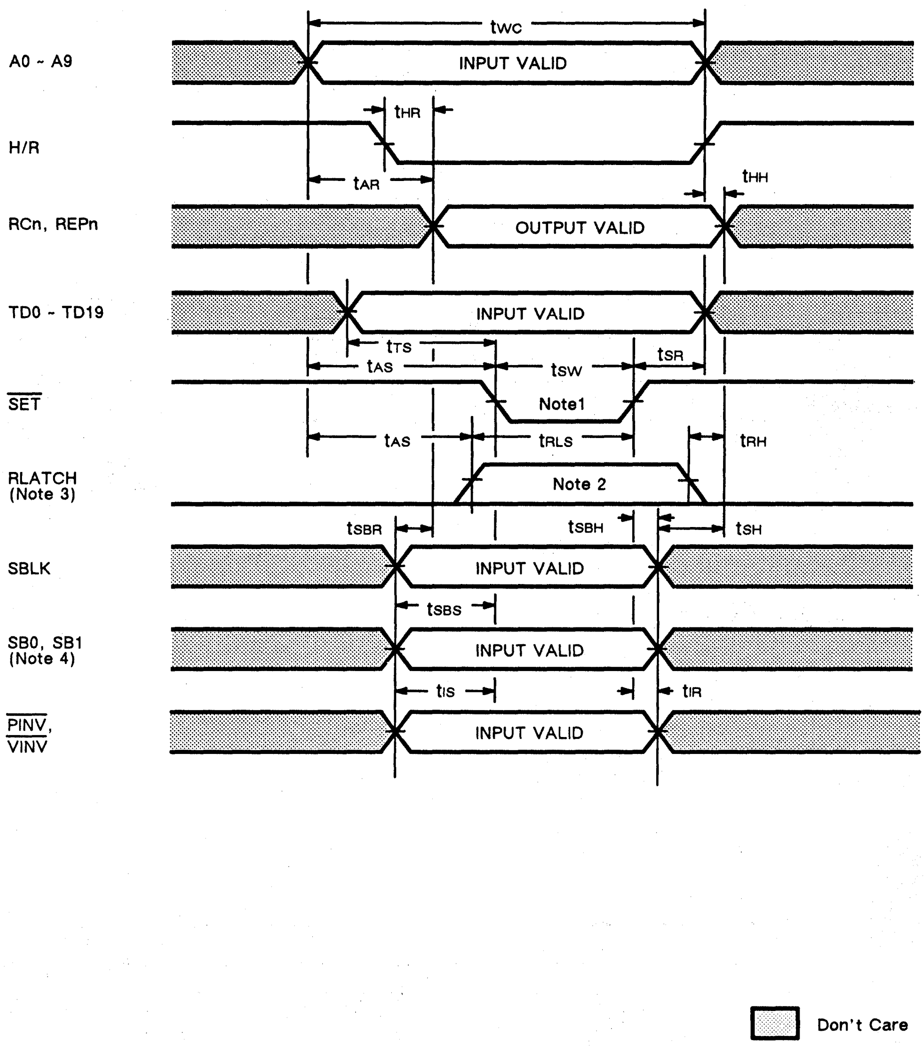
Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
All Purge Cycle Time	t_{APC}	100		100		ns
Purge Pulse Width	t_{PPW}	50		50		ns
Purge Recovery Time	t_{PR}	50		50		ns

TAG READ CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "H", $\overline{\text{PINV}}$ = "H" or "L", $\overline{\text{VINV}}$ = "H" or "L", INH = "H")



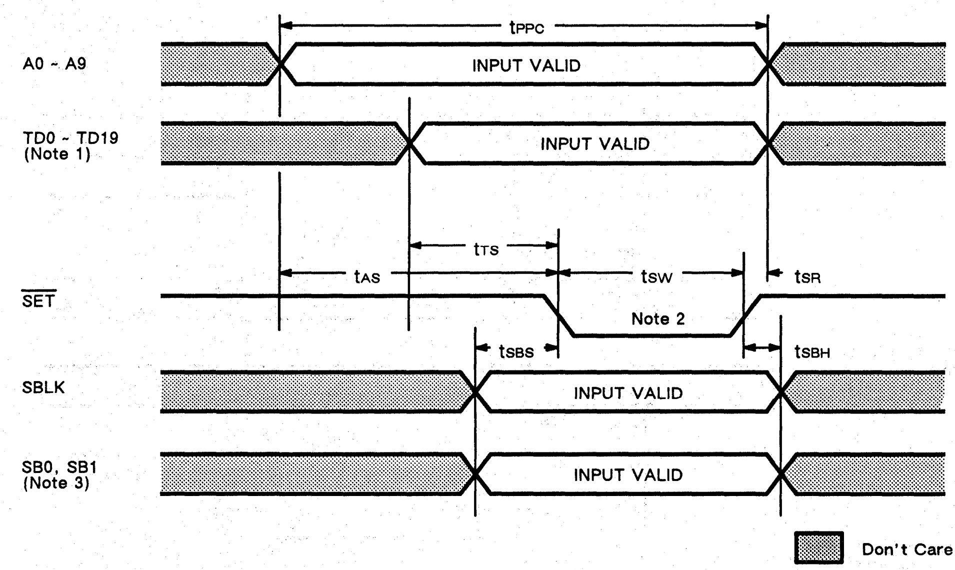
Notes 1: Valid at H/R = "H".
2: Valid at H/R = "L".
3: LRU is updated at $\overline{\text{SET}}$ = "L".
4: Replace latched at RLATCH = "H".
5: Valid at SBLK = "L".
6: Valid at SBLK = "H".

TAG WRITE CYCLE (MODE = "H" or "L", $\overline{PURGE}$ = "H", $\overline{WRITE}$ = "L", $\overline{INVL}$ = "H", $\overline{INH}$ = "H")



Notes 1. Registrate TAG, V-bit "H", LRU update.
2. Replace latched at $\overline{RLATCH}$ = "H".
3. Valid at SBLK = "L".
4. Valid at SBLK = "H".

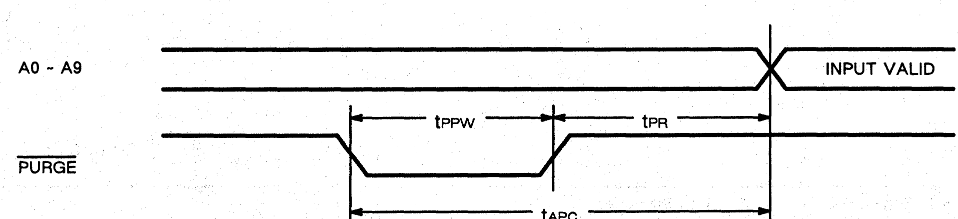
PARTIAL PURGE CYCLE (MODE = "H" or "L", $\overline{PURGE}$ = "H", $\overline{WRITE}$ = "H", $\overline{INVL}$ = "L", H/R = "H" or "L", $\overline{INH}$ = "H", RLATCH = "L", $\overline{PINV}$ = "H" or "L", $\overline{VINV}$ = "H" or "L")



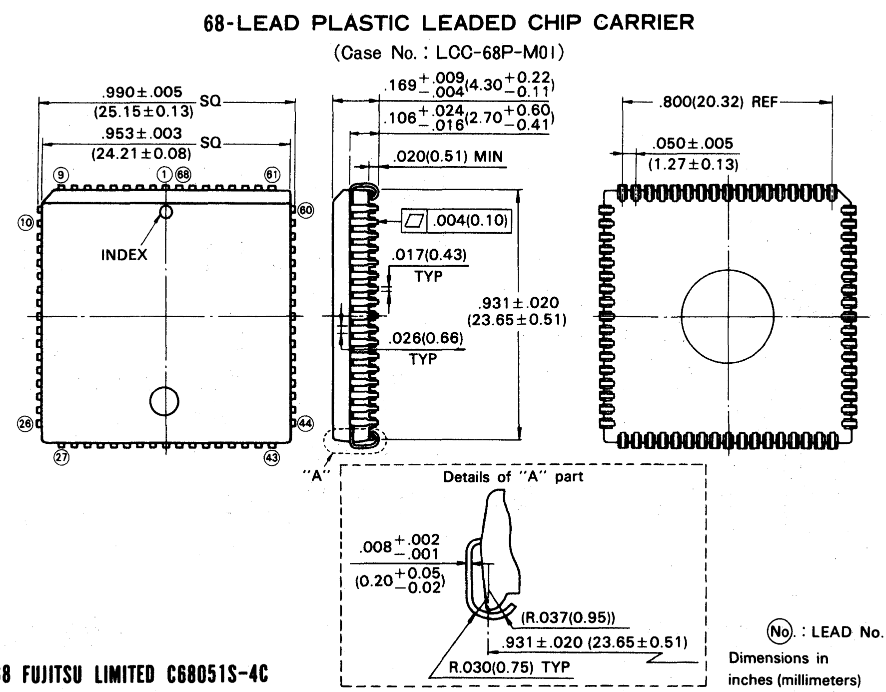
Notes:

1. Valid at SBLK = "L".
2. LRU is reversively updated, V-bit "L".
3. Valid at SBLK = "H".

All purge ($\overline{SET}$ = "H", OTHER CONTROL INPUTS ARE "H" or "L")

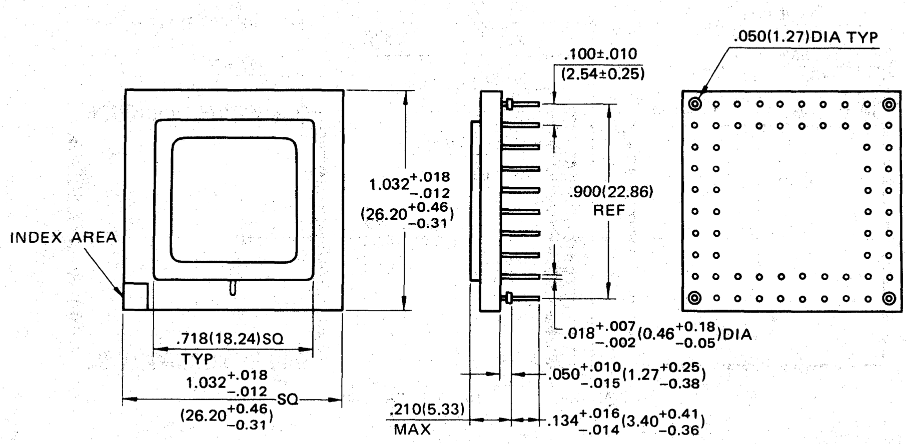


PACKAGE DIMENSIONS



PACKAGE DIMENSIONS (continued)

64-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-64C-A02)



Dimensions in inches (millimeters)

FUJITSU

CMOS 16384-BIT DUAL PORT STATIC RANDOM ACCESS MEMORY

MB8421/22-90/90L
MB8421/22-12/12L

TS213-B867
July 1986

2K X 8-BIT CMOS DUAL PORT STATIC RANDOM ACCESS MEMORY

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

The Fujitsu MB8421/22 are 2K words x 8 bits Dual port high-performance -static Random Access Memories (SRAMs) fabricated in CMOS. The SRAMs use asynchronous circuits; thus no external clockes are required.
The MB8421 and MB8422 provide the user with tow separately contorolled I/O ports with independent address, Chip select($\overline{CS}$), Write Enable($\overline{WE}$), Output Enable ($\overline{OE}$) and I/O functions.
This arrangement permits independent access to any memory location for either a Read orwWrite operation - a useful feature for shared data processing applications. These devices have an automatic power-down feature controlled by ($\overline{CS}$).
To avoide data contention on the same address, a ($\overline{BUSY}$) flag is provided for address arbitration; In addition, MB8421 utilizes ($\overline{INT}$) flag which allows communication between systems on either side of the RAM.
Both devices use a single +5 volte power supply and all pins are TTL-compatible. A simplified block diagram of the SRAM is shown in Figure 1.
Some typical applications for these memory devices are mutiprocessing systems, distributed networks, external register files and peripheral controllers.

Organization : 2048 words x 8 bits
Static operation : No clocks or timing strobe required

- Fast access time : $t_{AA}=t_{ACS}$=90ns max. (MB8421/22-90, MB8421/22-90L)
  $t_{AA}=t_{ACS}$=120ns max.(MB8421/22-12, MB8421/22-12L)
- Low power consumption : 660mW max. (Both ports active)
  385mW max. (One port active)
  38.5mW max.(Both ports standby, TTL)
  11mW max. (Both ports standby, CMOS)
  L-version : 495mW max. (Both ports active)
  275mW max. (One port active)
  27.5mW max.(Both ports standby, TTL)
  1.1mA max. (Both ports standby, CMOS)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- All inputs and outputs have protection against static charge
- Data Retention Voltage : 2V min.
- Address Arbitration Function : $\overline{BUSY}$ flag
- Interrupt Function for Communication between Systems (MB8421 only) : $\overline{INT}$ flag

FPT-64P-M01
(MB8421)

DIP-52P-M01
(MB8421)

DIP-48P-M02
(MB8422)

PIN ASSIGNMENT

Refer to the attachment

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

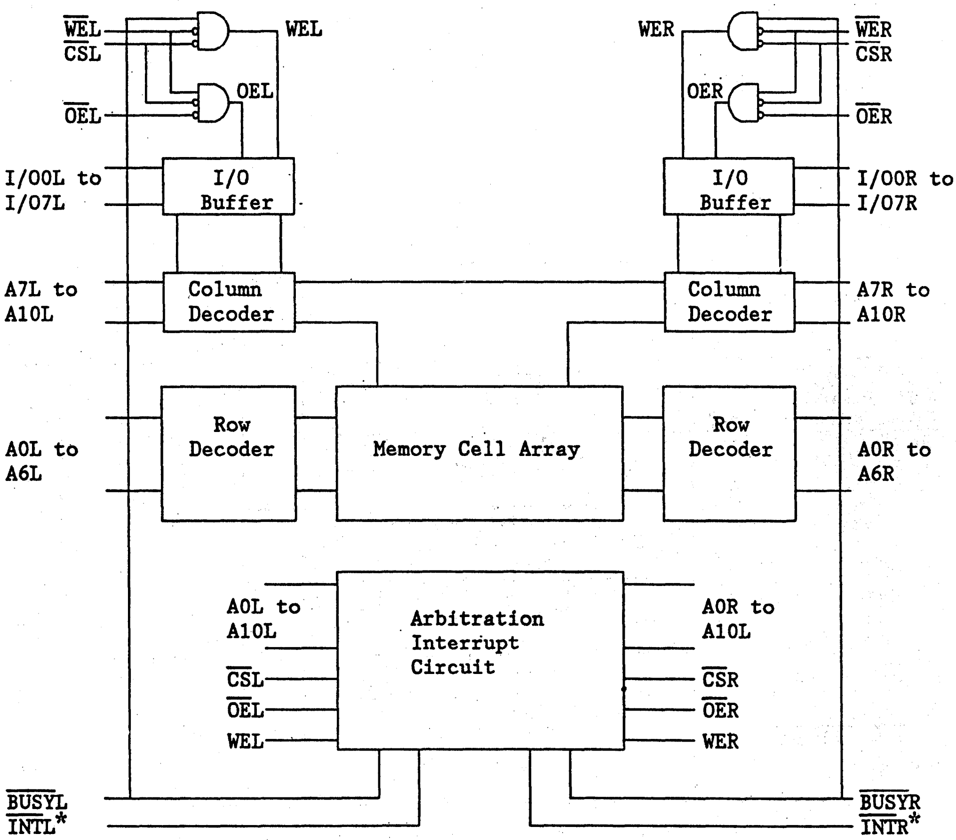
Rating	Symbol		Value	Unit
Supply Voltage	VCC		-0.5 to +7	V
Input Voltage on any pin with respect to VSS	VIN		-0.5 to +7	V
Output Voltage on any I/O pin with respect to VSS	VOUT		-0.5 to +7	V
Output Current	IOUT		±20	mA
Power dissipation	PD		1.0	W
Temperature Under Bias	TBIAS		-10 to +85	°C
Storage Temperature	TSTG	Ceramic	-65 to +150	°C
		Plastic	-40 to +125	

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CSL}$	$\overline{CSR}$	CHIP SELECT
$\overline{WEL}$	$\overline{WER}$	WRITE ENABLE
$\overline{OEL}$	$\overline{OER}$	OUTPUT ENABLE
$\overline{INTL}$	$\overline{INTR}$	INTERRUPT FLAG
$\overline{BUSYL}$	$\overline{BUSYR}$	BUSY FLAG
A0L to A10L	A0R to A10R	ADDRESS
I/O0L to I/O7L	I/O0R to I/O7R	DATA INPUT/OUTPUT
VCC		POWER
GND		GROUND

Fig. 1 – MB8421/22/21L/22L BLOCK DIAGRAM



* Applies to MB8421 only.

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN=0V)	CIN		10	pF
I/O Capacitance (VI/O=0V)	CI/O		10	pF

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RECOMMENDED OPERATING CONDITIONS
(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Input High Voltage	VIH	2.2		VCC+0.3	V
Input Low Voltage	VIL	-0.3		0.8	V
Operating Temperature	TA	0		70	°C

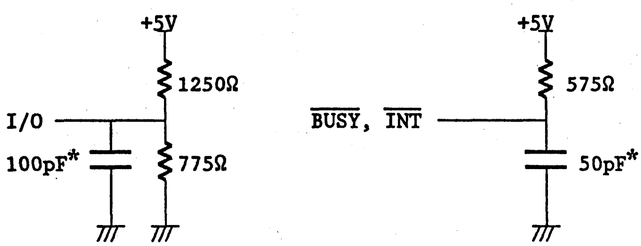
DC CHARACTERISTICS
(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Condition	MB8421/ MB8422- 90/12		MB8421/ MB8422- 90L/12L		Unit
			Min	Max	Min	Max	
Operating Supply Current (Both ports Active)	ICC	Cycle=Min. Duty=100% IOUT=0 mA		120		90	mA
Standby Supply Current	ISB1	Both ports=Standby $\overline{\text{CSL}}$ & $\overline{\text{CSR}}$=VIH		7		5	mA
	ISB2	One port=Standby $\overline{\text{CSL}}$ or $\overline{\text{CSR}}$=VIH, IOUT=0 mA		70		50	mA
	ISB3	Both ports=Full standby $\overline{\text{CSL}}$ & $\overline{\text{CSR}}$≥VCC-0.2V		2		0.2	mA
	ISB4	One port=Full standby $\overline{\text{CSL}}$ or $\overline{\text{CSR}}$≥VCC-0.2V, IOUT=0 mA		70		50	mA
Input Leakage Current	ILI	VIN=0V to VCC	-10	10	-10	10	µA
Output Leakage Current	ILO	$\overline{\text{CS}}$=VIH, VOUT=0V to VCC	-10	10	-10	10	µA
Output High Voltage	VOH*	IOUT=-1.0 mA	2.4		2.4		V
Output Low Voltage	VOL	IOUT=3.2 mA		0.4		0.4	V
Output Low Voltage for Open-Drain	VOL	IOUT=8 mA		0.4		0.4	V

* The $\overline{\text{BUSY}}$ and $\overline{\text{INT}}$ pins require pull-up resistors because they are open-drain outputs.

AC TEST CONDITIONS

- Input Pulse Levels : 0V to 3.0V
- Input Pulse Rise & Fall Times : tR, tF = 5ns
- Timing Reference Levels : 1.5V
- Output Load



*Including Jig and stray capacitance

AC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted)

READ CYCLE

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	90		120		ns
Address Access Time	tAA		90		120	ns
Chip Select Access Time	tACS		90		120	ns
Output Enable Access Time	tAOE		40		50	ns
Output Hold from Address Change	tOH	10		10		ns
Chip Select to Output Low-Z *1	tCLZ	5		5		ns
Output Enable to Output Low-Z *1	tOLZ	5		5		ns
Chip Select to Output High-Z *1	tCHZ		40		50	ns
Output Enable to Output High-Z *1	tOHZ		40		50	ns
Power up from Chip Select	tPU	0		0		ns
Power down from Chip Select	tPD		50		60	ns

WRITE CYCLE

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8421-12/12L		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	90		120		ns
Address Valid to End of Write	tAW	85		100		ns
Chip Select to End of Write	tCW	85		100		ns
Address Setup Time	tAS	0		0		ns
Write Pulse Width	tWP	60		70		ns
Write Recovery Time	tWR	0		0		ns
Data Valid to End of Write	tDW	40		40		ns
Data Hold Time	tDH	0		0		ns
Write Enable to Output Low-Z *1	tOW	0		0		ns
Write Enable to Output High-Z *1	tWZ		40		50	ns

BUSY TIMING

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
BUSY Access Time from Address	tBAA		45		60	ns
BUSY Output High-Z from Address	tBDA		45		60	ns
BUSY Access Time from CS	tBAC		45		60	ns
BUSY Output High-Z from CS	tBDC		45		60	ns
Arbitration priority Set up Time	tAPS	20		25		ns

INTERRUPT TIMING

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
INT Set Time *2	tINS		80		100	ns
INT Reset Time *2	tINR		80		100	ns

Note : *1 Transition is measured at the point of ±500mV from steady state voltage with CL=5pF.
*2 This parameter is specified MB8421 only.

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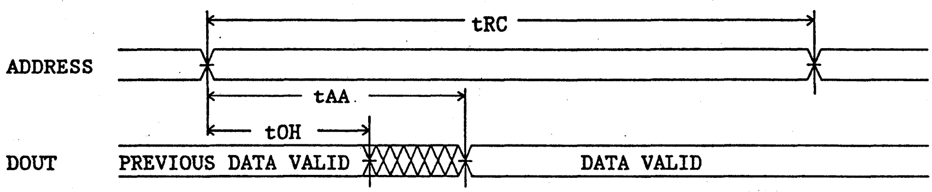
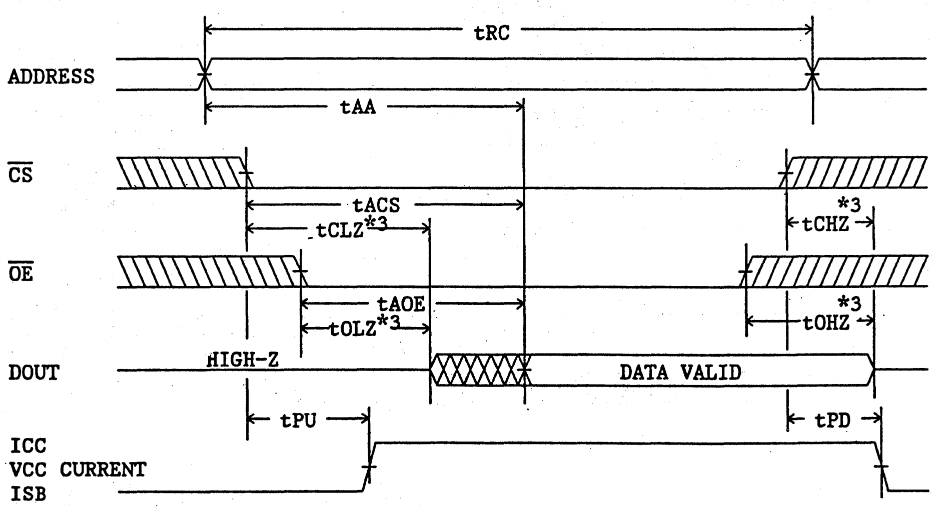
READ CYCLE TIMING DIAGRAMS

READ CYCLE No. I *1*2



READ CYCLE No. II *1

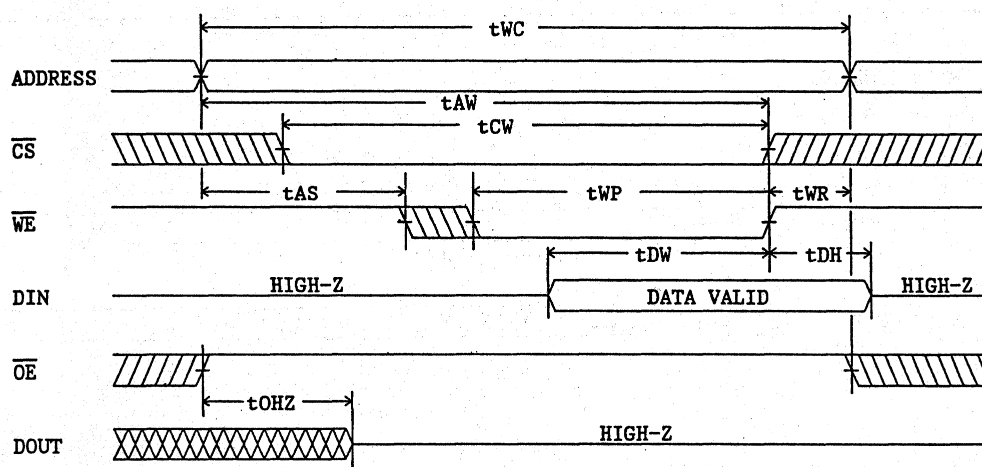


: Don't Care : Undefined

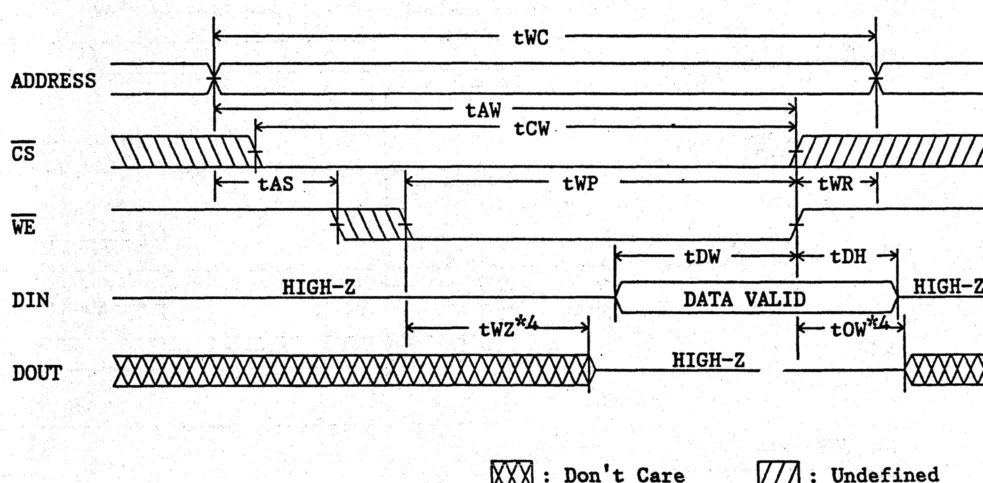
Note : *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=VIL.
*3 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

WRITE CYCLE TIMING DIAGRAMS

WRITE CYCLE No. I *1*2 : $\overline{WE}$ CONTROLLED



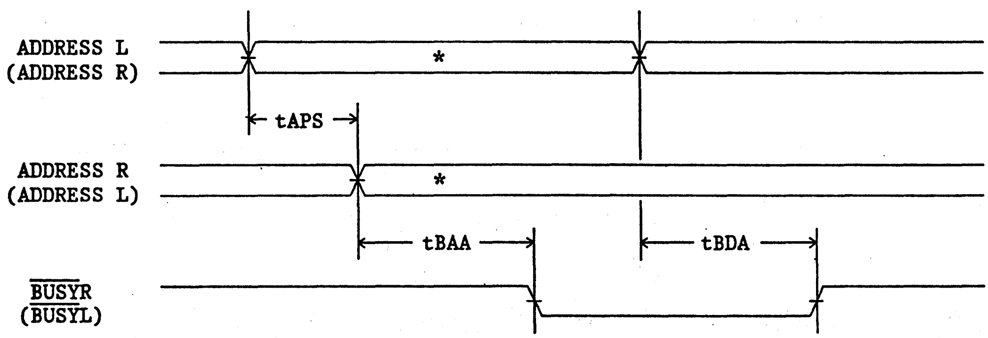
WRITE CYCLE No. II *1*2*3 : $\overline{WE}$ CONTROLLED



Note : *1 $\overline{WE}$ must be high during address transition.
*2 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3 If $\overline{CS}$ goes high prior to or coincident with WE transition high, the output remains in high impedance state.
*4 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5 pF.

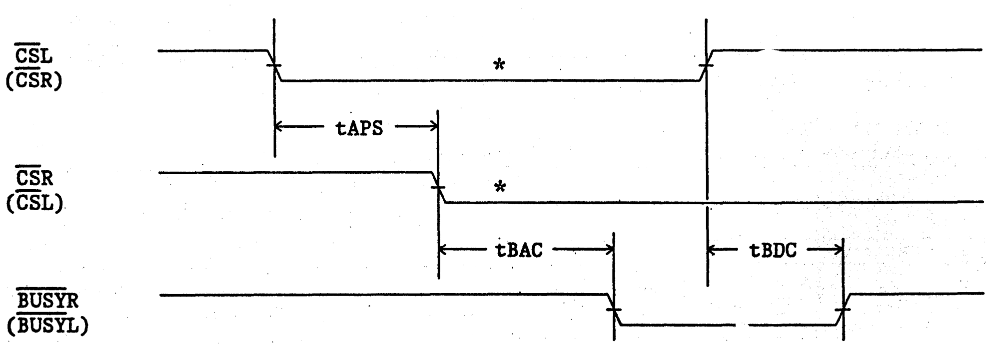
CONTENTION CYCLE TIMING DIAGRAMS *1

CONTENTION CYCLE No. I *2 : ADDRESS CONTROLLED



* ADDRESS L = ADDRESS R

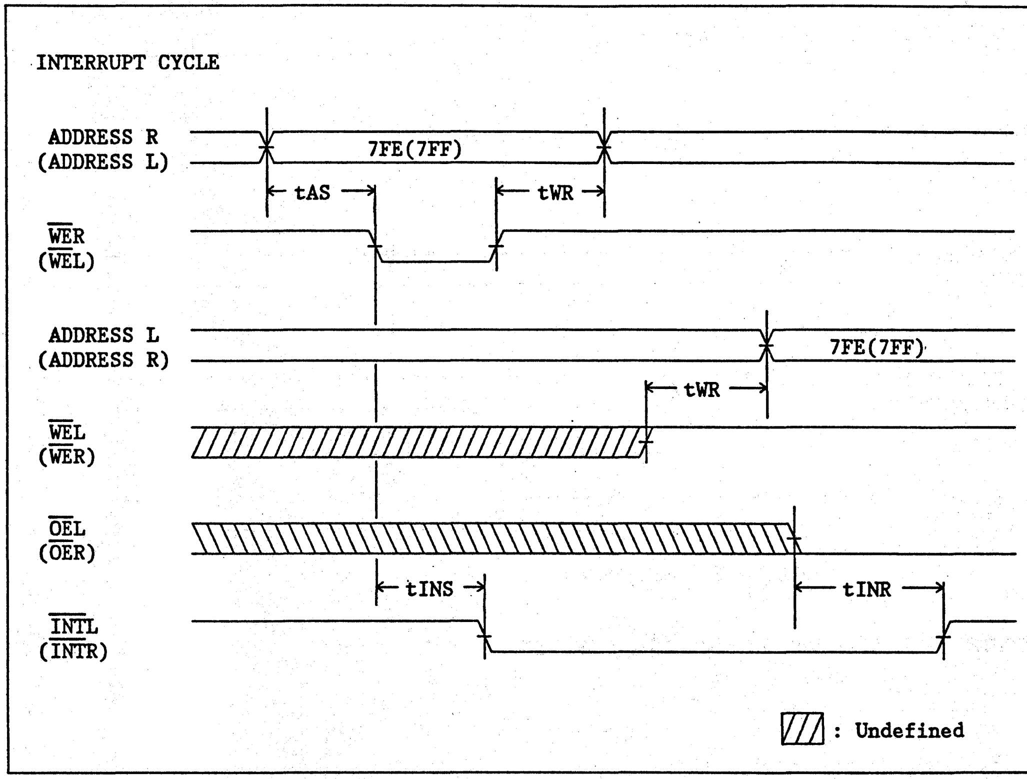
CONTENTION CYCLE No. II *3 : $\overline{\text{CS}}$ CONTROLLED



* ADDRESS L = ADDRESS R

Note : *1 In case of dualaccess at the same memory location, the port that access the RAM first sets the $\overline{\text{BUSY}}$ flag high.
*2 $\overline{\text{CS}}$ must be low before or coincident with transition of address.
*3 Address is valid prior to cincident with high-to-low transition of $\overline{\text{CS}}$.

INTERRUPT CYCLE TIMING DIAGRAMS *1



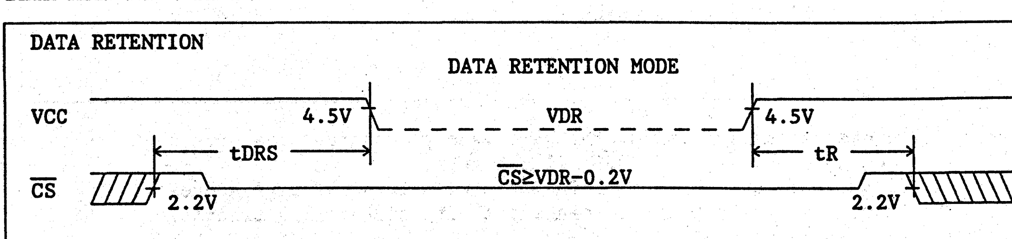
Note : *1 Applies to MB8421 only.

DATA RETENTION CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8421-90/12 MB8422-90/12		MB8421-90L/12L MB8422-90L/12L		Unit
		Min	Max	Min	Max	
Data Retention Supply Voltage	VDR	2.0	5.5	2.0	5.5	V
Data Retention Supply Current *2	IDR		0.2		0.02	mA
Data Retention Setup Time	tDRS	0		0		ns
Operation Recovery Time	tR	tRC		tRC		ns

*2 VCC=VDR=3V
$\overline{CSL}$ & $\overline{CSR}$≥VCC-0.2V

DATA RETENTION TIMING



TRUTH TABLES

TABLE I NON-CONTENTION READ/WRITE CONTROL

LEFT PORT INPUTS *1			RIGHT PORT INPUTS *1			FLAGS		FUNCTION
$\overline{CSL}$	$\overline{WEL}$	$\overline{OEL}$	$\overline{CSR}$	$\overline{WER}$	$\overline{OER}$	$\overline{BUSYL}$	$\overline{BUSYR}$	
H	X	X	X	X	X	H	H	Left Port in Power Down Mode
X	X	X	H	X	X	H	H	Right Port in Power Down Mode
L	L	X	X	X	X	H	H	Data on Left Port Written Into Memory
L	H	L	X	X	X	H	H	Data in Memory Output on Left Port
X	X	X	L	L	X	H	H	Data on Right Port Written Into Memory
X	X	X	L	H	L	H	H	Data in Memory Output on Right Port

H = High L = Low X = Don't Care
Note : *1 A0L to A10L ≠ A0R to A10R

TABLE II $\overline{CS}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CS}$

LEFT PORT INPUTS				RIGHT PORT INPUTS				FLAGS		FUNCTION
$\overline{CSL}$	$\overline{WEL}$	$\overline{OEL}$	A0L to A10L	$\overline{CSR}$	$\overline{WER}$	$\overline{OER}$	A0R to A10R	$\overline{BUSYL}$	$\overline{BUSYR}$	
LBR	X	X	MATCH	L	X	X	MATCH	H	L	Left Operation Permitted Right Operation Not Permitted
L	X	X	MATCH	LBL	X	X	MATCH	L	H	Left Operation Not Permitted Right Operation Permitted
LST	X	X	MATCH	LST	X	X	MATCH	H	L	Arbitration Resolved

H = High L = Low X = Don't Care
LST = Low Same Time LBR = Low Before Right LBL = Low Before Left

TABLE III ADDRESS ARBITRATION WITH $\overline{CS}$ LOW BEFORE ADDRESS MATCH

LEFT PORT INPUTS				RIGHT PORT INPUTS				FLAGS		FUNCTION
$\overline{CSL}$	$\overline{WEL}$	$\overline{OEL}$	A0L to A10L	$\overline{CSR}$	$\overline{WER}$	$\overline{OER}$	A0R to A10R	$\overline{BUSYL}$	$\overline{BUSYR}$	
L	X	X	VBR	L	X	X	VALID	H	L	Left Operation Permitted Right Operation Not Permitted
L	X	X	VALID	L	X	X	VBL	L	H	Left Operation Not Permitted Right Operation Permitted
L	X	X	VST	L	X	X	VST	H	L	Arbitration Resolved

H = High L = Low X = Don't Care
VST = Valid Same Time VBR = Valid Before Right VBL = Valid Before Left

FUNCTIONAL DESCRIPTION

The Fujitsu MB8421/22 provide two ports with separate control signals, address inputs and input/output data pins that allow asynchronous read and write operation to any memory location.
These devices have an automatic power-down feature controlled by $\overline{CS}$.
There is an on-chip power down circuitry that places the respective port into a standby mode when $\overline{CS}$ is high (chip deselected). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the $\overline{OE}$ is active and it turns on the output drivers. Non-contention READ/WRITE conditions are illustrated in table I.

ARBITRATION LOGIC

Functional Description:

The arbitration logic resolves an address match or chip enable match and determines the priority of the access. In both cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

In a dual-port RAM, both ports are asynchronous, thus there exists a possibity of accessing the same memory location from both sides. This possibity does not pose a problem if both the ports are in read mode. Though it creates a problem when both the ports are in write mode with different data words or else one port is in write mode and the other port is in the read mode. For such situations, $\overline{BUSY}$ flags are provided on the dual-port RAM devices. Hence whenever, both the ports access the same memory location, then the on-chip arbitration logic will determine which port has access. Next it will set the $\overline{BUSY}$ flag of the delayed ports to active low. This prohibits any operation on that port. The delayed port gets the access when the $\overline{BUSY}$ flag becomes inactive.

Two modes of arbitration are present:

1) When the addresses match for the left and the right ports are valid before $\overline{CS}$, on-chip control logic arbitrates between $\overline{CSL}$ and $\overline{CSR}$ for access (refer to Fig. on Data Contention Cycle No. II($\overline{CS}$ controlled), and Table II).

2) When the $\overline{CSL}$ and $\overline{CSR}$ are low before an address match, on-chip control logic arbitrates between the left and the right addresses for access (refer to Fig. on Data Contention Cycle No. I(Address controlled), and Table III).

It should be noted that for the case when both $\overline{CSL}$ and $\overline{CSR}$ are low at the same time ($\overline{CS}$ controlled), or when both address left and address right are valid at the same time (address controlled), then arbitration logic sets the $\overline{BUSYR}$ flag low, providing the priority to left port.

For most microprocessors like the Intel 8086, the asyncronous $\overline{BUSY}$ line can be tied to the READ input, as long it meets the set-up and hold requirements.

INTERRUPT FUNCTION

The interrupt function ($\overline{\text{INT}}$) is provided to allow communication between the systems on either sides of the dual-port RAM. $\overline{\text{INTL}}$ is set to low, when the processor on the right port writes to address 7FE(A0=L and A1 to A10 =H). $\overline{\text{INTL}}$ is then reset to High, when the left port acknowledges by reading the same address 7FE. Thus the address 7FE is like a 8 bit word mail-box transferring information from the right-port to the left-port.

$\overline{\text{INTR}}$ on the other hand is set to low, when processor on the left port writes to the address 7FF(A0 to A10 =H). $\overline{\text{INTR}}$ is reset to High, when the right port acknowledges by reading this address. Hence, the address 7FF is a second 8 bit word mail-box transferring information from the left port to the right port.

The $\overline{\text{INTL}}$ and $\overline{\text{INTR}}$ are set to High on power-up. If the port is in the standby mode, it can still get interrupted by the processor on the other side.

In case the $\overline{\text{BUSY}}$ flag is set to low, then the pertinent port can not set or reset the $\overline{\text{INT}}$ flag.

Attachment 1.

48 PIN DIP (MB8422)

TOP VIEW

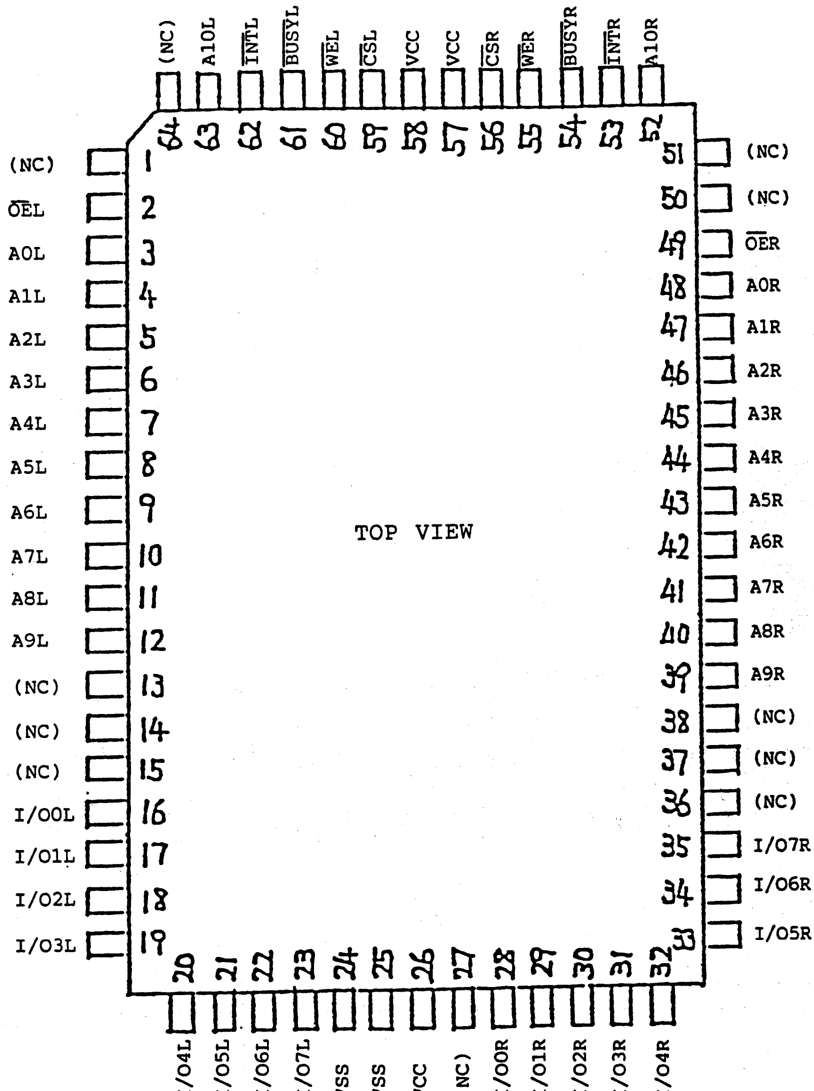
$\overline{\text{CSL}}$	1	48	VCC
$\overline{\text{WEL}}$	2	47	$\overline{\text{CSR}}$
$\overline{\text{BUSYL}}$	3	46	$\overline{\text{WER}}$
A10L	4	45	$\overline{\text{BUSYR}}$
$\overline{\text{OEL}}$	5	44	A10R
A0L	6	43	$\overline{\text{OER}}$
A1L	7	42	A0R
A2L	8	41	A1R
A3L	9	40	A2R
A4L	10	39	A3R
A5L	11	38	A4R
A6L	12	37	A5R
A7L	13	36	A6R
A8L	14	35	A7R
A9L	15	34	A8R
I/O0L	16	33	A9R
I/O1L	17	32	I/O7R
I/O2L	18	31	I/O6R
I/O3L	19	30	I/O5R
I/O4L	20	29	I/O4R
I/O5L	21	28	I/O3R
I/O6L	22	27	I/O2R
I/O7L	23	26	I/O1R
VSS	24	25	I/O0R

52 PIN SHRINK DIP (MB8421)

TOP VIEW

$\overline{\text{CSL}}$	1	52	VCC
$\overline{\text{WEL}}$	2	51	$\overline{\text{CSR}}$
$\overline{\text{BUSYL}}$	3	50	$\overline{\text{WER}}$
$\overline{\text{INTL}}$	4	49	$\overline{\text{BUSYR}}$
NC	5	48	$\overline{\text{INTR}}$
A10L	6	47	NC
$\overline{\text{OEL}}$	7	46	A10R
A0L	8	45	$\overline{\text{OER}}$
A1L	9	44	A0R
A2L	10	43	A1R
A3L	11	42	A2R
A4L	12	41	A3R
A5L	13	40	A4R
A6L	14	39	A5R
A7L	15	38	A6R
A8L	16	37	A7R
A9L	17	36	A8R
I/O0L	18	35	A9R
I/O1L	19	34	I/O7R
I/O2L	20	33	I/O6R
I/O3L	21	32	I/O5R
I/O4L	22	31	I/O4R
I/O5L	23	30	I/O3R
I/O6L	24	29	I/O2R
I/O7L	25	28	I/O1R
VSS	26	27	I/O0R

PIN ASSIGNMENT FOR MB8421 (QFP)



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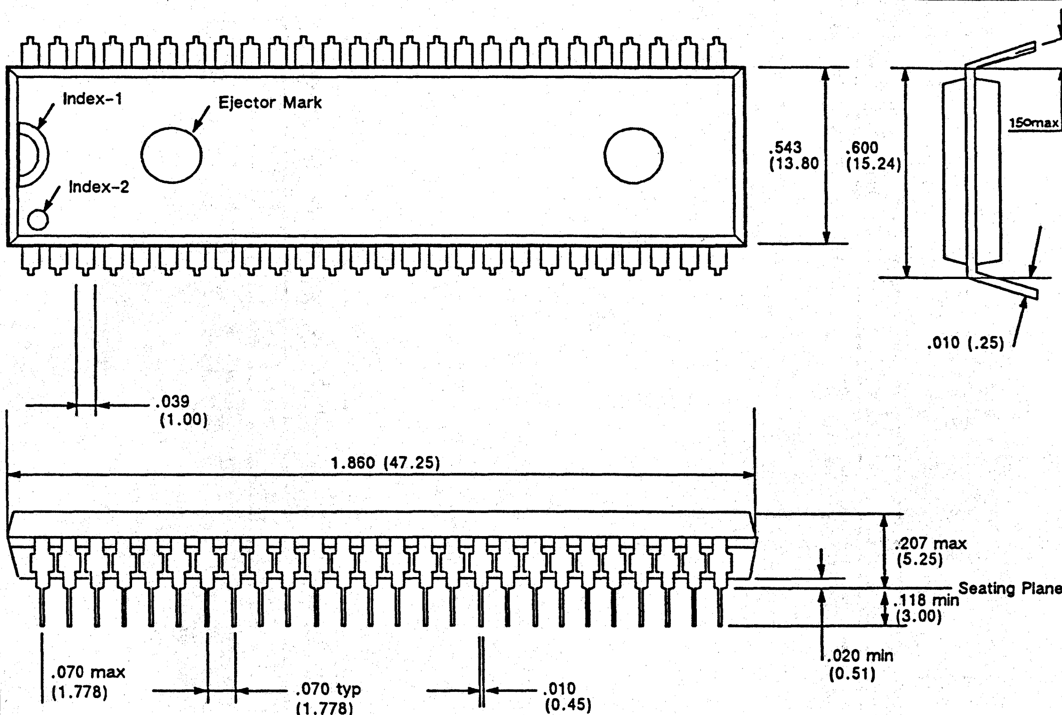
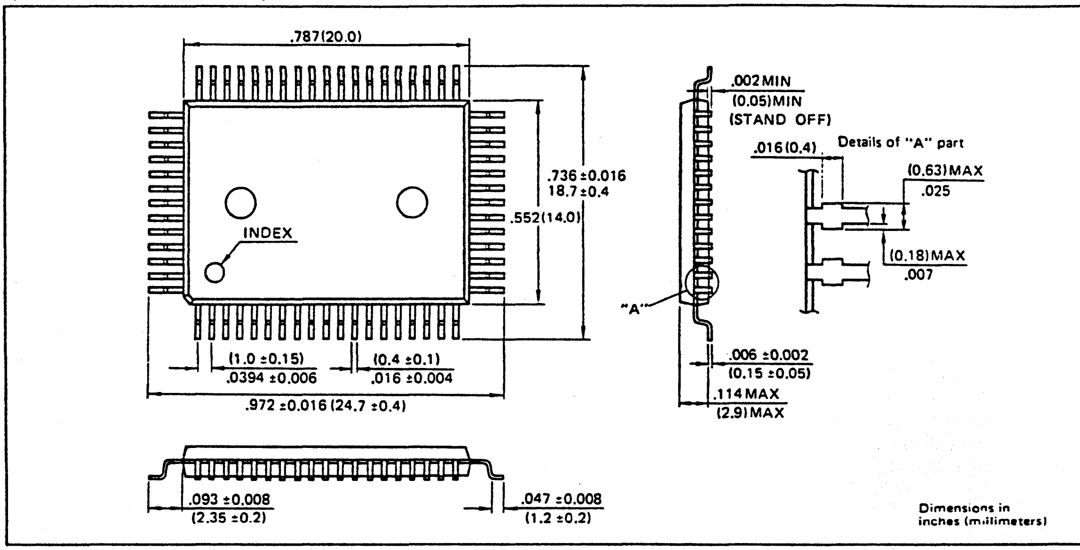
52 LEAD PLASTIC DUAL-IN-LINE PACKAGE
(DIP-52P-M01)

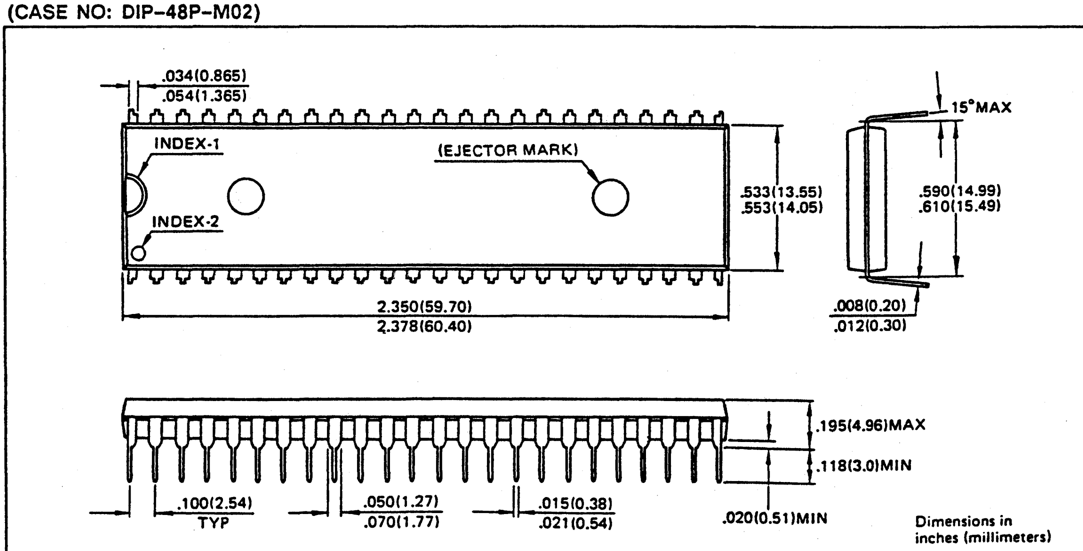


Note:
Dimensions in inches (millimeters).

64-LEAD PLASTIC FLAT PACKAGE
(CASE NO: FPT-64P-M01)



48-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE NO: DIP-48P-M02)



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FUJITSU

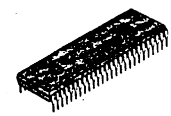
CMOS 16384-BIT STATIC RANDOM ACCESS MEMORY

MB8431/32-90
MB8431/32-90L
MB8431/32-12
MB8431/32-12L

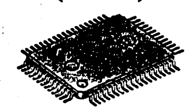
TS254-A889
September 1, 1988

2K X 8-BIT CMOS DUAL PORT STATIC RANDOM ACCESS MEMORY

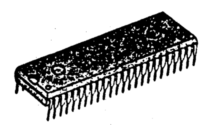
The Fujitsu MB8431/32 are 2K words x 8 bits Dual port high-performance -static Random Access Memories (SRAMs) fabricated in CMOS. The SRAMs use asynchronous circuits; thus no external clockes are required.
The MB8431 and MB8432 provide the user with two separately contorolled I/O ports with independent address, Chip select($\overline{CS}$), Write Enable($\overline{WE}$), Output Enable ($\overline{OE}$) and I/O functions.
This arrangement permits independent access to any memory location for either a Read or Write operation - a useful feature for shared data processing applications. These devices have an automatic power-down feature controlled by ($\overline{CS}$).
To avoide data contention on the same address, a ($\overline{BUSY}$) input is provided for address arbitration; In addition, MB8431 utilizes ($\overline{INT}$) flag which allows communication between systems on either side of the RAM.
Both devices use a single +5 volt power supply and all pins are TTL-compatible. A simplified block diagram of the SRAM is shown in Figure 1.
Some typical applications for these memory devices are multiprocessing systems, distributed networks, external register files and peripheral controllers.



DIP-52P-M01
(MB8431)



FPT-64P-M01
(MB8431)



DIP-48P-M02
(MB8432)

- Organization : 2048 words x 8 bits
- Static operation : No clocks or timing strobe required
- Fast access time : t_{AA}=t_{ACS}=90ns max. (MB8431/32-90
  MB8431/32-90L)
  t_{AA}=t_{ACS}=120ns max.(MB8431/32-12
  MB8431/32-12L)
- Low power consumption : 660mW max. (Both ports active)
  385mW max. (One port active)
  38.5mW max.(Both ports standby, TTL)
  11mW max. (Both ports standby, CMOS)
  L-version : 495mW max. (Both ports active)
  275mW max. (One port active)
  27.5mW max.(Both ports standby, TTL)
  1.1mA max. (Both ports standby, CMOS)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- All inputs and outputs have protection against static charge
- Data Retention Voltage : 2V min.
- Address Arbitration Function : $\overline{BUSY}$ input
- Interrupt Function for Communication between Systems (MB8431 only) : $\overline{INT}$ flag
- Expanding capability using MB8421/22(Master)-MB8431/32(Slave)

PIN ASSIGNMENT

See Page 15

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +7	V
Input Voltage on any pin with respect to VSS	VIN	-0.5 to VCC +0.5	V
Output Voltage on any I/O pin with respect to VSS	VOUT	-0.5 to VCC +0.5	V
Output Current	IOUT	±20	mA
Power dissipation	PD	1.0	W
Temperature Under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-40 to +125	°C

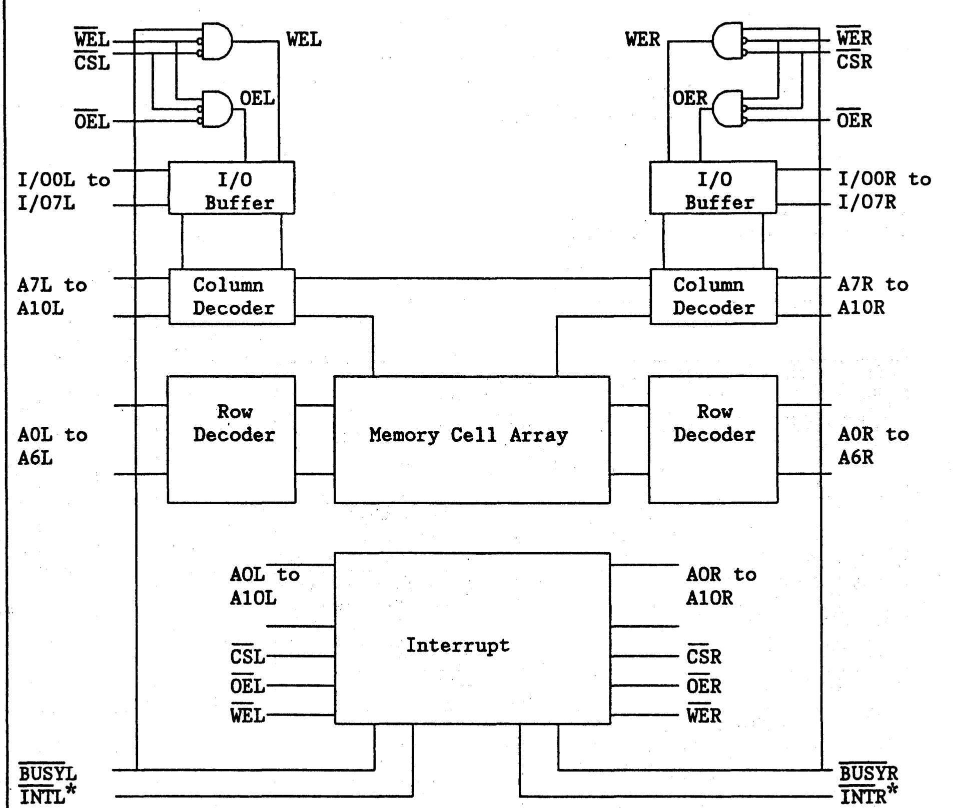
Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{\text{CSL}}$	$\overline{\text{CSR}}$	CHIP SELECT INPUT
$\overline{\text{WEL}}$	$\overline{\text{WER}}$	WRITE ENABLE INPUT
$\overline{\text{OEL}}$	$\overline{\text{OER}}$	OUTPUT ENABLE INPUT
$\overline{\text{INTL}}$	$\overline{\text{INTR}}$	INTERRUPT * FLAG OUTPUT
$\overline{\text{BUSYL}}$	$\overline{\text{BUSYR}}$	BUSY FLAG INPUT
A0L to A10L	A0R to A10R	ADDRESS INPUT
I/O0L to I/O7L	I/O0R to I/O7R	DATA INPUT/OUTPUT
VCC		POWER
GND		GROUND

*: Applies to MB8431 only.

Fig. 1 – MB8431/32/31L/32L BLOCK DIAGRAM



* Applies to MB8431 only.

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN=0V)	CIN		10	pF
I/O Capacitance (VI/O=0V)	CI/O		10	pF

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RECOMMENDED OPERATING CONDITIONS
(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Input High Voltage	VIH	2.2		VCC+0.3	V
Input Low Voltage	VIL	-0.3 *1		0.8	V
Operating Temperature	TA	0		70	°C

*1 Undershoot -3.0V min at less than 20ns pulse width.

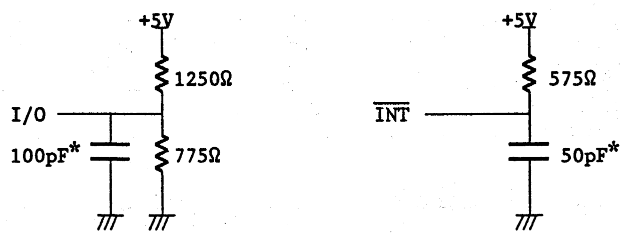
DC CHARACTERISTICS
(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Condition	MB8431/ MB8432-90/12		MB8431/ MB8432-90L/12L		Unit
			Min	Max	Min	Max	
Operating Supply Current (Both ports Active)	ICC	Cycle=Min. Duty=100% IOUT=0 mA		120		90	mA
Standby Supply Current	ISB1	Both ports=Standby $\overline{CSL}$ & $\overline{CSR}$=VIH		7		5	mA
	ISB2	One port=Standby $\overline{CSL}$ or $\overline{CSR}$=VIH, IOUT=0 mA		70		50	mA
	ISB3	Both ports=Full standby $\overline{CSL}$ & $\overline{CSR}$≥VCC-0.2V		2		0.2	mA
	ISB4	One port=Full standby $\overline{CSL}$ or $\overline{CSR}$≥VCC-0.2V, IOUT=0 mA		70		50	mA
Input Leakage Current	ILI	VIN=0V to VCC	-10	10	-10	10	μA
Output Leakage Current	ILO	$\overline{CS}$=VIH, VOUT=0V to VCC	-10	10	-10	10	μA
Output High Voltage	VOH*	IOUT=-1.0 mA	2.4		2.4		V
Output Low Voltage	VOL	IOUT=3.2 mA		0.4		0.4	V
Output Low Voltage for Open-Drain	VOL	IOUT=8 mA		0.4		0.4	V

* The $\overline{INT}$ pins require pull-up resistors because they are open-drain outputs.

AC TEST CONDITIONS

- Input Pulse Levels : 0V to 3.0V
- Input Pulse Rise & Fall Times : tR, tF = 5ns
- Timing Reference Levels : 1.5V
- Output Load



*Including Jig and stray capacitance

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AC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted)

READ CYCLE

Parameter	Symbol	MB8431-90/90L MB8432-90/90L		MB8431-12/12L MB8432-12/12L		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	90		120		ns
Address Access Time	tAA		90		120	ns
Chip Select Access Time	tACS		90		120	ns
Output Enable Access Time	tAOE		40		50	ns
Output Hold from Address Change	tOH	10		10		ns
Chip Select to Output Low-Z *1	tCLZ	5		5		ns
Output Enable to Output Low-Z *1	tOLZ	5		5		ns
Chip Select to Output High-Z *1	tCHZ		40		50	ns
Output Enable to Output High-Z *1	tOHZ		40		50	ns
Power up from Chip Select *2	tPU	0		0		ns
Power down from Chip Select *2	tPD		50		60	ns

WRITE CYCLE

Parameter	Symbol	MB8431-90/90L MB8432-90/90L		MB8431-12/12L MB8431-12/12L		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	90		120		ns
Address Valid to End of Write	tAW	85		100		ns
Chip Select to End of Write	tCW	85		100		ns
Address Setup Time	tAS	0		0		ns
Write Pulse Width	tWP	60		70		ns
Write Recovery Time	tWR	0		0		ns
Data Valid to End of Write	tDW	40		40		ns
Data Hold Time	tDH	0		0		ns
Write Enable to Output Low-Z *1	tOW	0		0		ns
Write Enable to Output High-Z *1	tWZ		40		50	ns

SLAVE BUSY TIMING

Parameter	Symbol	MB8431-90/90L MB8432-90/90L		MB8431-12/12L MB8432-12/12L		Unit
		Min	Max	Min	Max	
Busy Access Time	tBO		0		0	ns
Write Set Up Time To Busy	tWS	-10		-10		ns
Write Hold Time From Busy	tWH	20		25		ns

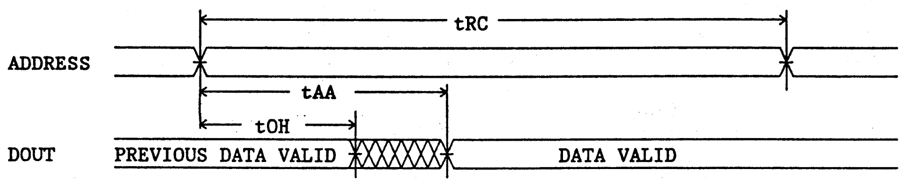
INTERRUPT TIMING

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
INT Set Time *3	tINS		80		100	ns
INT Reset Time *3	tINR		80		100	ns

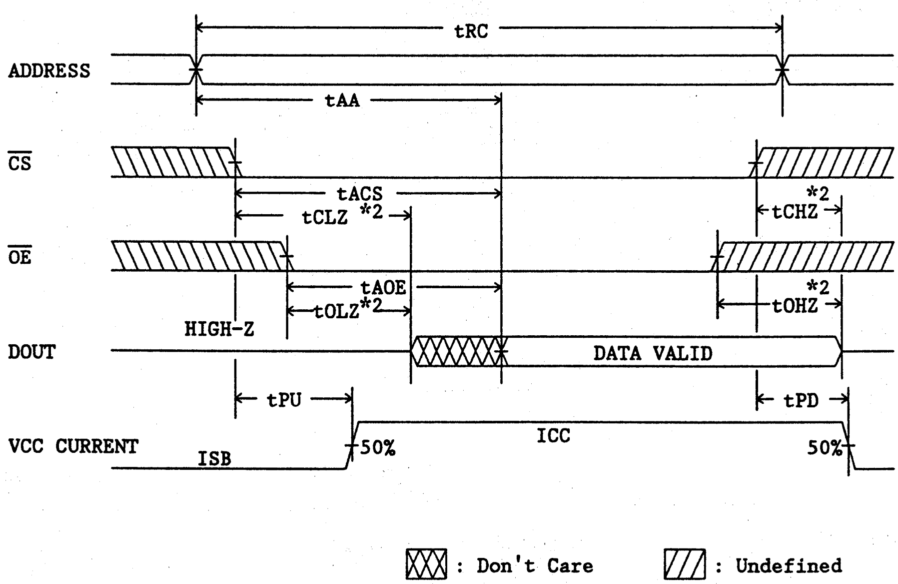
Note : *1 Transition is measured at the point of ±500mV from steady state voltage with CL=5pF.
*2 This parameter is not tested 100%.
*3 This parameter is specified for MB8431 only.

READ CYCLE TIMING DIAGRAMS ($\overline{WE}$=VIH)

READ CYCLE No. I (ADDRESS CONTROLLED) ($\overline{CS}$=$\overline{OE}$=VIL)



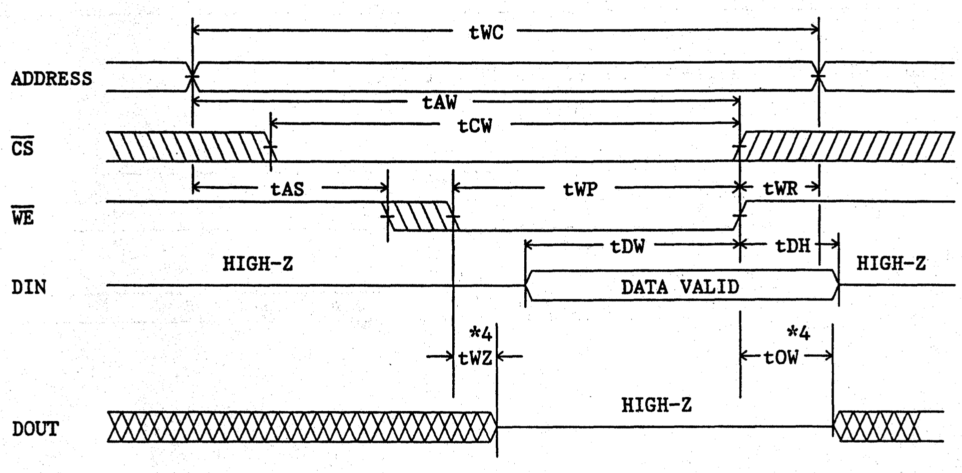
READ CYCLE No. II *1 ($\overline{CS}$ CONTROLLED)



Note : *1 Address should be fixed before high-to-low transition of $\overline{CS}$.
*2 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

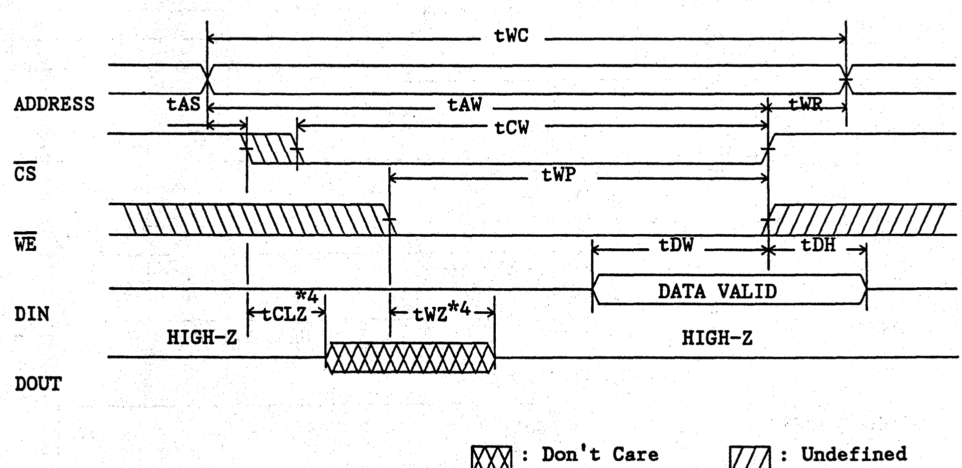
WRITE CYCLE TIMING DIAGRAMS (OE= Don't care)

WRITE CYCLE No. I *1*2*3 : (WE CONTROLLED)



7

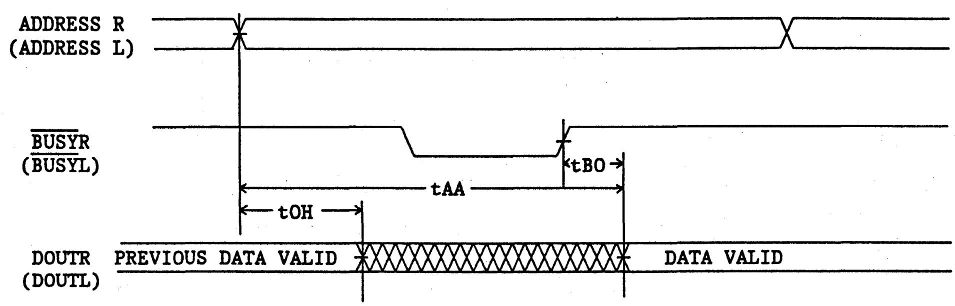
WRITE CYCLE No. II *1*2*3 : (CS CONTROLLED)



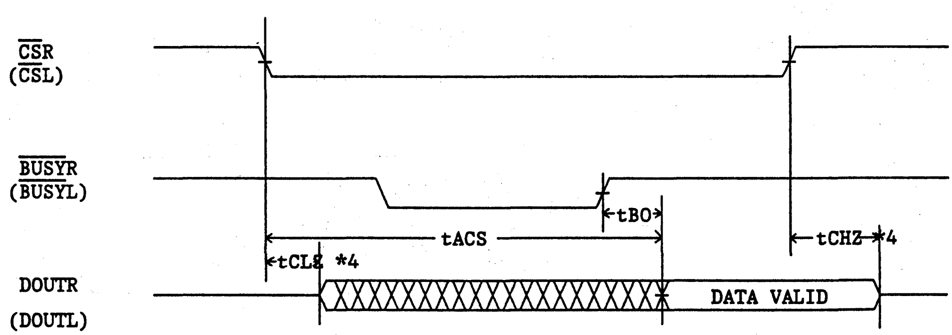
Note : *1 WE must be high during address transition.
*2 If OE, CS are in the READ Mode, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3 If CS goes high prior to or coincident with WE transition to high, the output remains in high impedance state.
*4 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5 pF.

CONTENTION CYCLE TIMING DIAGRAMS ($\overline{\text{WE}}$=VIH)

CONTENTION READ CYCLE No. I *2 : (ADDRESS CONTROLLED) ($\overline{\text{CS}}$=$\overline{\text{OE}}$=VIL)



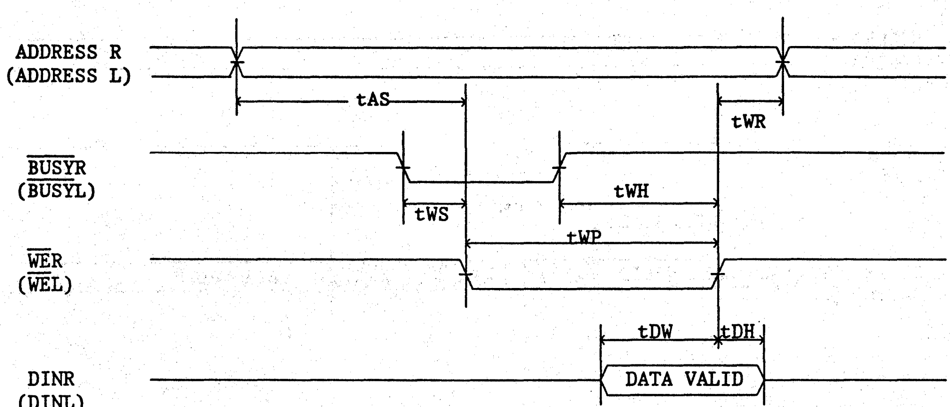
CONTENTION READ CYCLE No. II *3 : ($\overline{\text{CS}}$ CONTROLLED)



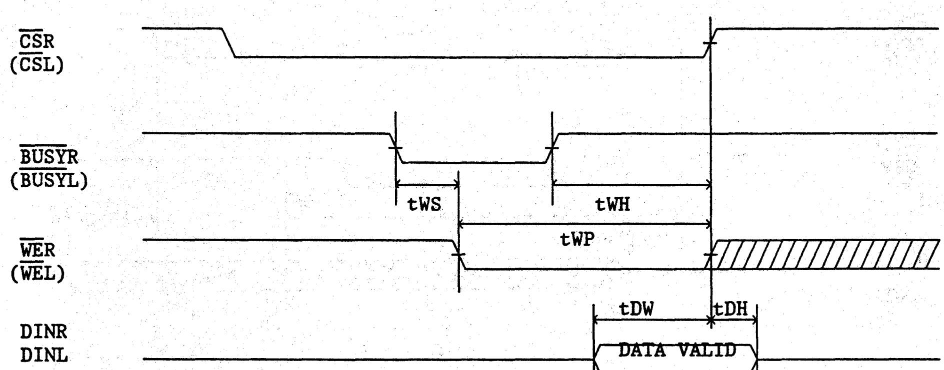
Note : *1 In case of dualaccess at the same memory location, the port that access the RAM first sets the $\overline{\text{BUSY}}$ flag high.
*2 $\overline{\text{CS}}$ must be low before or coincident with transition of address.
*3 Address is valid prior to cincident with high-to-low transition of $\overline{\text{CS}}$.
*4 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

CONTENTION CYCLE TIMING DIAGRAMS

CONTENTION WRITE CYCLE No. I : *1*2*3 ($\overline{\text{WE}}$ CONTROLLED)

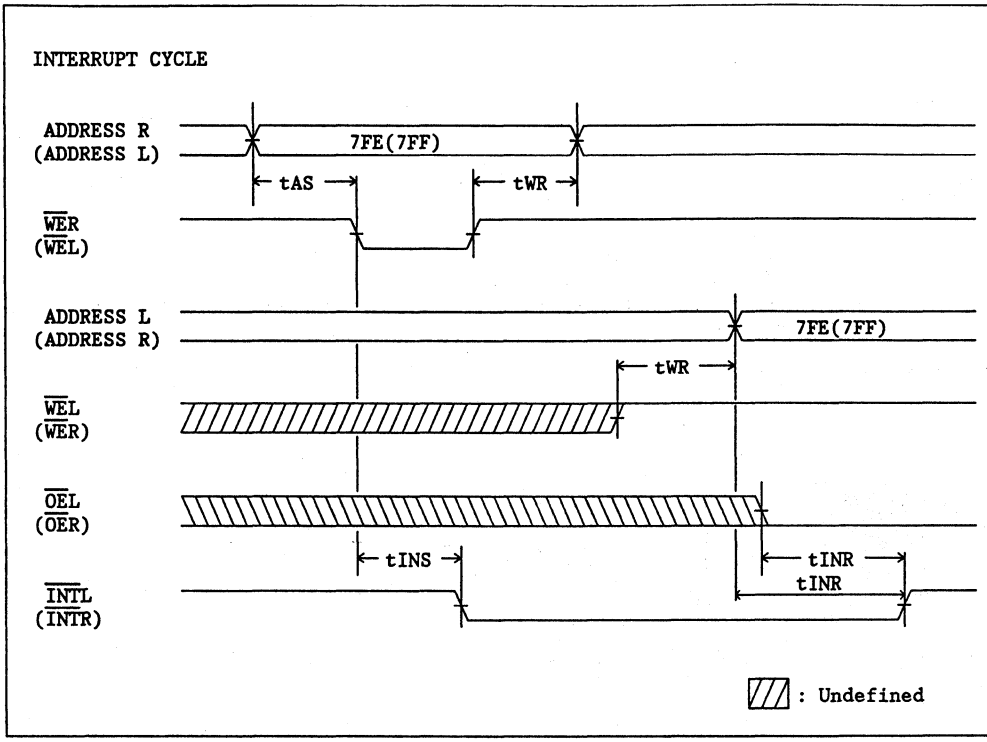


CONTENTION WRITE CYCLE No. II *3 : *1*2*3 ($\overline{\text{CS}}$ CONTROLLED)



Note : *1 $\overline{\text{WE}}$ must be high during address transition.
*2 I/O pins are in the output state, so the input signals of opposite phase must not be applied.
*3 During $\overline{\text{BUSY}}$ input is low, write operation can not be excuted even if $\overline{\text{WE}}$ is low.

INTERRUPT CYCLE TIMING DIAGRAMS *1



Note : *1 Applies to MB8431 only.

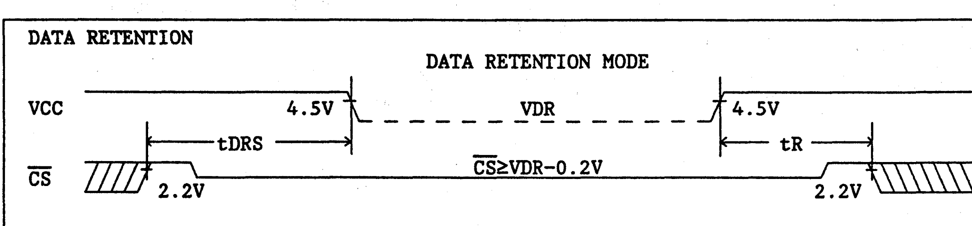
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8431-90/12 MB8432-90/12		MB8431-90L/12L MB8432-90L/12L		Unit
		Min	Max	Min	Max	
Data Retention Supply Voltage	VDR	2.0	5.5	2.0	5.5	V
Data Retention Supply Current *2	IDR		0.2		0.02	mA
Data Retention Setup Time	tDRS	0		0		ns
Operation Recovery Time	tR	tRC		tRC		ns

*2 VCC=VDR=3V
CSL & CSR≥VCC-0.2V

DATA RETENTION TIMING



POWER ON/RESET CHARACTERISTICS

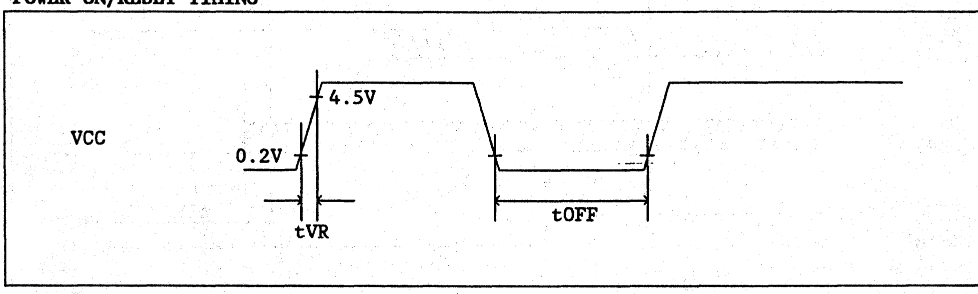
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	MB8431-90/12 MB8432-90/12		MB8431-90L/12L MB8432-90L/12L		Unit
			Min	Max	Min	Max	
Power Up Time	*1	tVR	0.05	50	0.05	50	ms
Power Off Time	*2	tOFF	1		1		s

*1 This is required to keep normal operation for power on/reset circuit which initialize $\overline{\text{INT}}$ output to "H" automatically when VCC is applied.

*2 This is required to keep normal operation for power on/reset circuit which VCC is repeatly turn on/off.

POWER ON/RESET TIMING



FUNCTION DISCRIPTION :

1. ORGANIZATION :

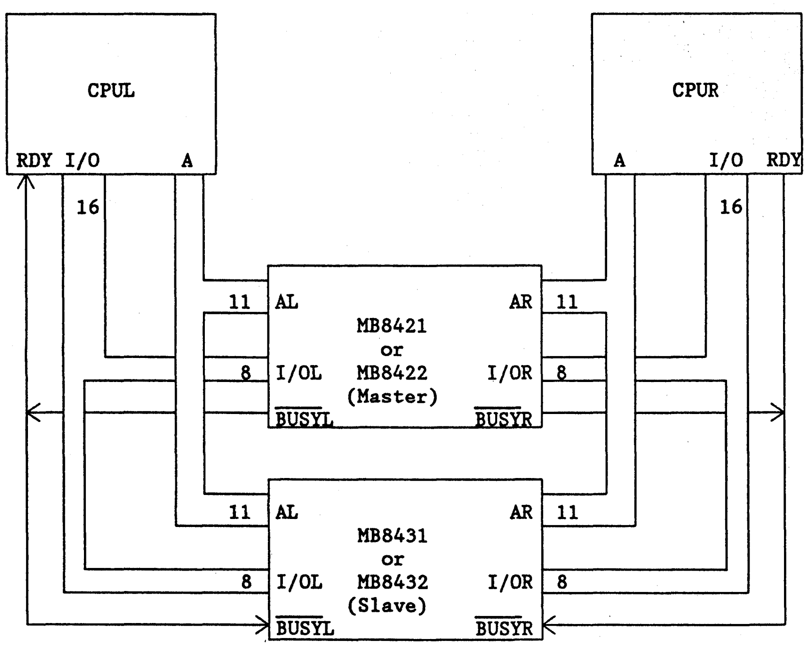
MB8431/32 are 2K words x 8 bits Dual port Static Random Access Memory. Each port has independent addresses, chip select ($\overline{\text{CS}}$), write enable ($\overline{\text{WE}}$), output enable ($\overline{\text{OE}}$) and data input/output (I/O) fucntions.

2. SLAVE BUSY FUNCTION :

In order to do bit expansion using 8 bit width dual port RAM such as MB8421/22, two or more parts should be connected paralel. But such case, there is a possibility, which depends on arbitration timing, of outputting $\overline{\text{BUSY}}$ signal to different ports and put both CPUs in waiting state. This causes a trouble. Using MB8431/32 which have slave busy function (busy input) is one of the solutaion for such trouble.
Bit expansion is easily achievable to pair-use slave type dual port RAM such as MB8431/32 and master type dual port RAM such as MB8421/22.

(Example)

As an example, Fig 1 shows 16 bit dual port memory system.
In this system, master type Dual port RAM (MB8421/22) judge arbitration for address contention and output result of the judgement from BUSY pin. This output returned to CPU and make the CPU in waiting state and also the output is applied to slave type dual port RAM (MB8431/32).
Though slave type dual port RAM (MB8431/32) do not judge for arbitration, they have BUSY input pin and inhibit write operation of the correspondent port during "L" signal form BUSY output of master type dual port RAM (MB8421/22) is applied to the BUSY input.
A system consists of one master dual port RAM (MB8421/22) and three slave dual port RAMs (MB8431/32) is harmonized for 32 bit application.



3. INTERRAPT FUNCTION :

The interrupt function ($\overline{\text{INT}}$) is provided to allow communcation between the systems on either sides of the dual-port RAM. $\overline{\text{INTL}}$ is set to low, when the processor on the right port writes to address 7FE (A0=L and A1 to A10=H). $\overline{\text{INTL}}$ is then reset to High, when the left port acknowledges by reading the same address 7FE. Thus the address 7FE is like a 8 bit word mail-box transferring information from the right-port to the left-port.

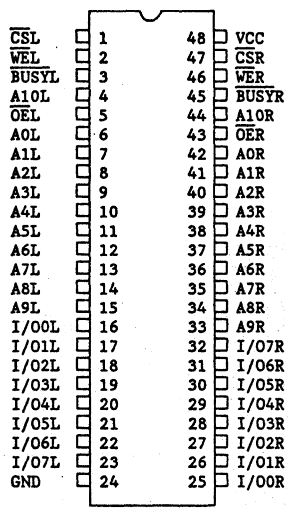
$\overline{\text{INTR}}$ on the other hand is set to low, when processor on the left port writes to the address 7FF (A=0 to A10=H). $\overline{\text{INTR}}$ is reset to High, when the right port acknowledges by reading this address. Hence, the address 7FF is a second 8 bit word mail-box transferring information form the left port to the right port.

7

The $\overline{\text{INTL}}$ and $\overline{\text{INTR}}$ are set to High on power-up. If the port is in the standby mode, it can still get interrupted by the processor on the other side.

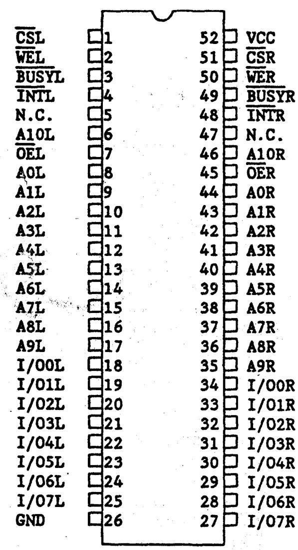
In case the $\overline{\text{BUSY}}$-flag is set to low, then the pertinent port can not set or reset the $\overline{\text{INT}}$ flag.

TOP VIEW

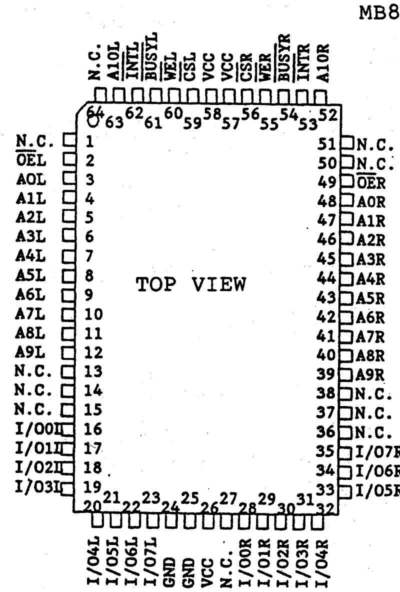


MB8432

TOP VIEW



MB8431



MB8431

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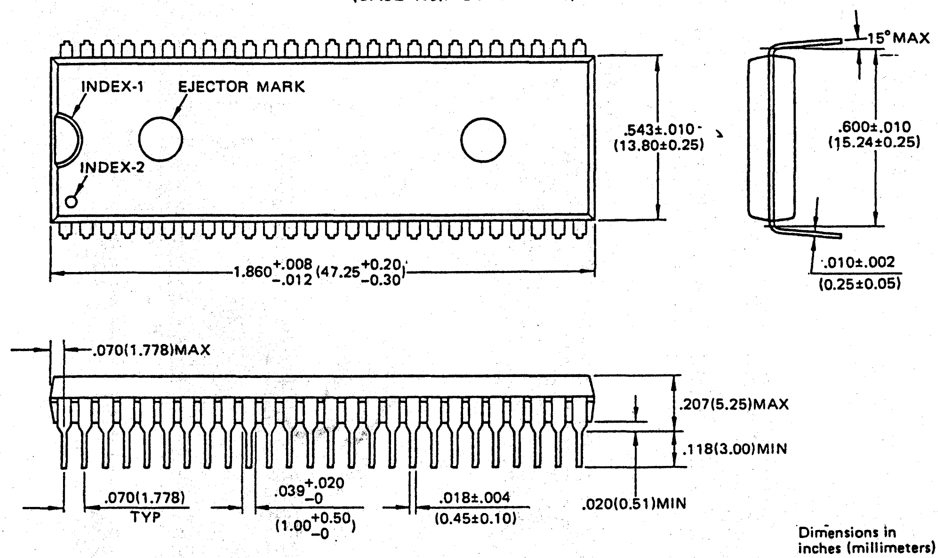
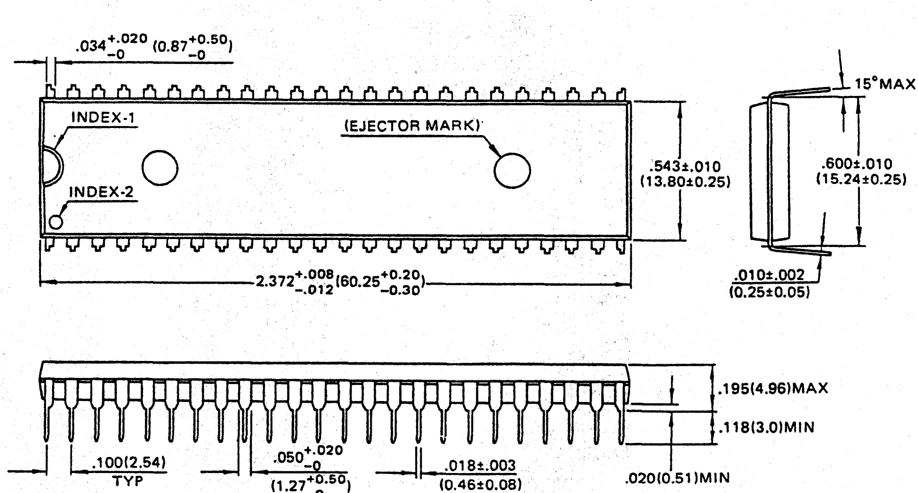
52-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-52P-M01)



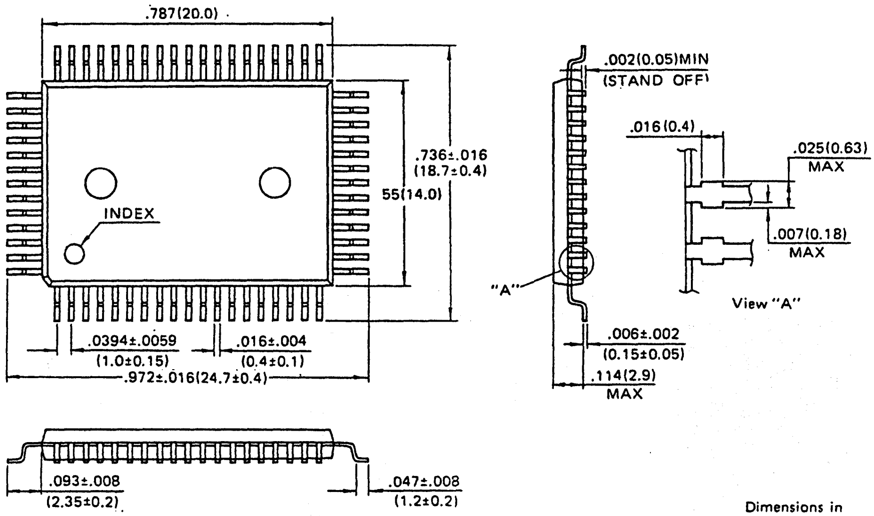
48-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-48P-M02)



Dimensions in inches (millimeters)

7

64-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-64P-M01)



Dimensions in inchs (millimeters)

Section 8

NMOS Erasable PROMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options	Sealing Method
8-3	MB2764-20	200	65536 bits	28-pin Ceramic DIP	CERDIP
	MB2764-25	250	(8192w x 8b)	32-pad Ceramic LCC	Metal
	MB2764-30	300			
8-15	MB27128-20	200	131072 bits	28-pin Ceramic DIP	CERDIP
	MB27128-25	250	(16384w x 8b)	32-pad Ceramic LCC	Metal
	MB27128-30	300			
8-27	MB27256-17	170	262144 bits	28-pin Ceramic DIP	CERDIP
	MB27256-20	200	(32768w x8b)	32-pad Ceramic LCC	Metal
	MB27256-25	250			

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8

FUJITSU

UV ERASABLE 65536-BIT READ ONLY MEMORY

MBM 2764-20 MBM 2764-25 MBM 2764-30

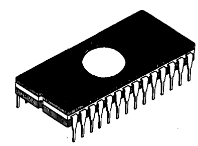
January 1984
Edition 4.0

MOS 8192x8BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

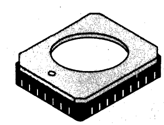
The Fujitsu MBM 2764 is a high speed 65,536-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin Dual-In-Line package and a 32-pad Leadless-Chip-Carrier with a transparent lid are used to package the MBM 2764. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 2764 is fabricated using N-MOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8192 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



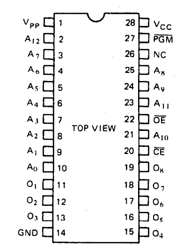
CERAMIC PACKAGE
DIP-28C-C01

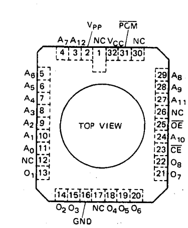


CERAMIC PACKAGE
LCC-32C-A01

- 8192 words x 8 bits organization, fully decoded
- Simple programming requirements
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- Programs with one 50ms or 1ms pulse
- Low power requirement
  - Active : 788mW (550mW)
  - Standby : 184mW (193mW)
  - (Value in parentheses is for "AB" version.)
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Fast access time:
  - 200ns max. (MBM 2764-20)
  - 250ns max. (MBM 2764-25)
  - 300ns max. (MBM 2764-30)
- Single +5V operation
- Standard 28-pin DIP package and 32-pad LCC
- Interchangeable with Intel 2764

PIN ASSIGNMENT





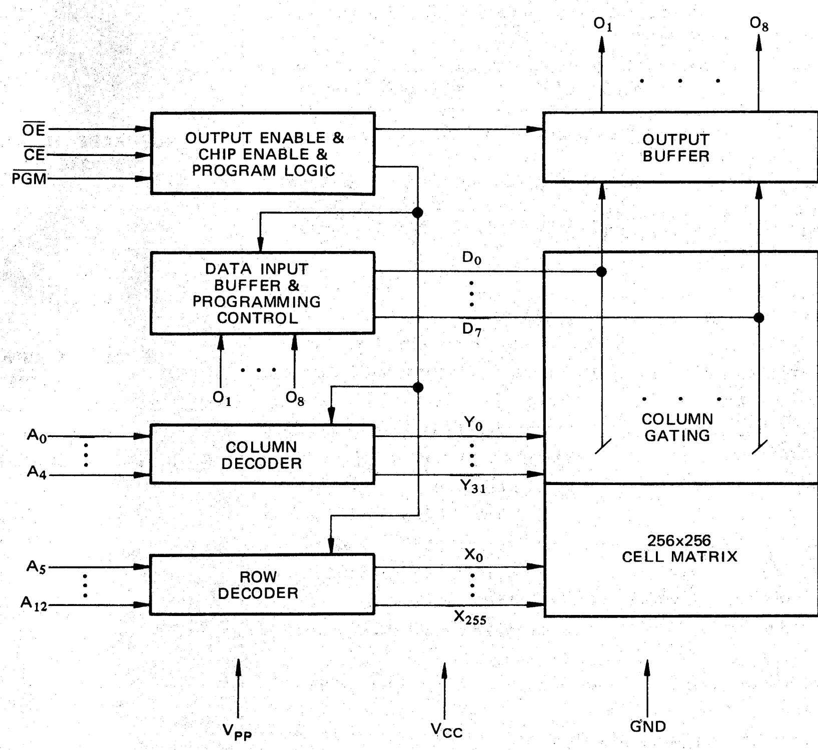
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	-0.6 to +7	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +22	V
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restriced to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MBM 2764 BLOCK DIAGRAM



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CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	–	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	–	8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2~10, 23~25, 21)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Output Disable	Don't Care	High-Z	V_{IL}	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
				Don't Care	V_{IL}			
Standby	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	GND

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*1	V_{CC}	4.75 (4.5)*2	5.0	5.25 (5.5)*2	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} −0.6	–	V_{CC} + 0.6	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−0.1	–	0.8	V
Operating Temperature	T_A	0		70	°C

Note: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.
*2 Value in parentheses is for "AB" version.

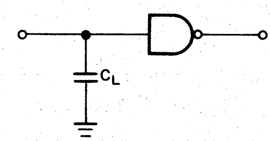
DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)*1	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.25V)*1	I_{LO}			10	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}			35	mA
V_{CC} Supply Current ($\overline{CE}$ = V_{IL})	I_{CC2}			150 (100)*2	mA
V_{PP} Supply Current (V_{PP} = V_{CC} ± 0.6V)	I_{PP}			15	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4			V

Note: *1 V_{IN} and V_{OUT} voltage for "AB" parts is 5.5V.
*2 Value in parentheses is for "AB" version.

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



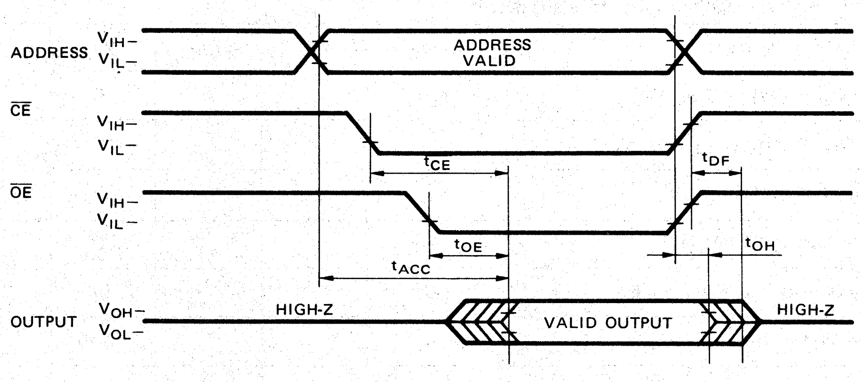
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 2764-20			MBM 2764-25			MBM 2764-30			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time*1	t_{ACC}			200			250			300	ns
$\overline{CE}$ to Output Delay	t_{CE}			200			250			300	ns
$\overline{OE}$ to Output Delay*1	t_{OE}	10		70	10		100	10		120	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		105	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



CHARACTERISTICS CURVES

Fig. 3 – SUPPLY CURRENT (STANDBY) vs SUPPLY VOLTAGE

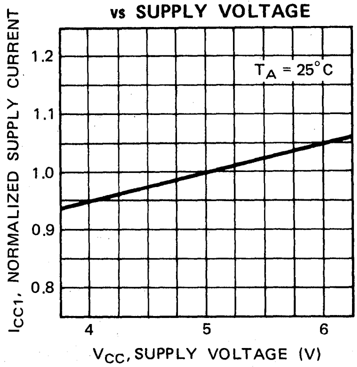


Fig. 4 – SUPPLY CURRENT (STANDBY) vs AMBIENT TEMPERATURE

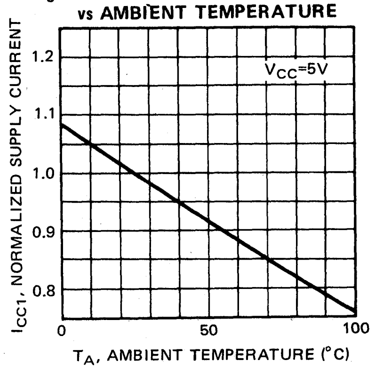


Fig. 5 – SUPPLY CURRENT (ACTIVE) vs SUPPLY VOLTAGE

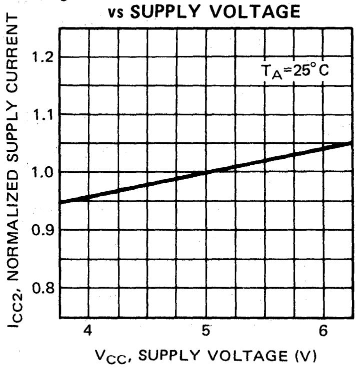


Fig. 6 – SUPPLY CURRENT (ACTIVE) vs AMBIENT TEMPERATURE

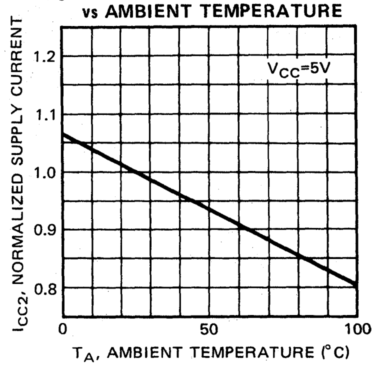


Fig. 7 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

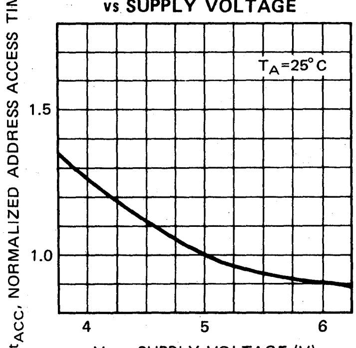
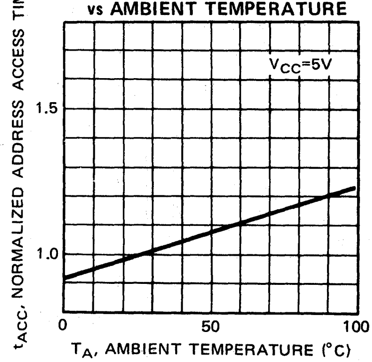


Fig. 8 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE



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CHARACTERISTICS CURVES (continued)

Fig. 9 — $\overline{CE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE

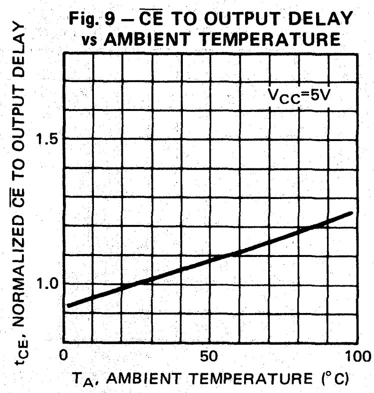


Fig. 10 — $\overline{OE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE

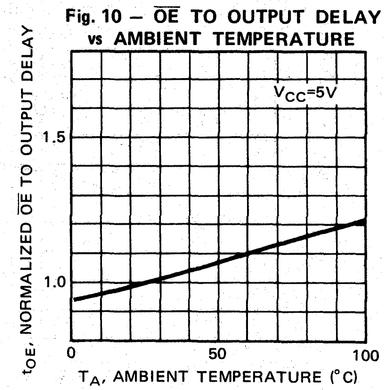


Fig. 11 — $\overline{OE}$ HIGH TO OUTPUT FLOAT vs AMBIENT TEMPERATURE

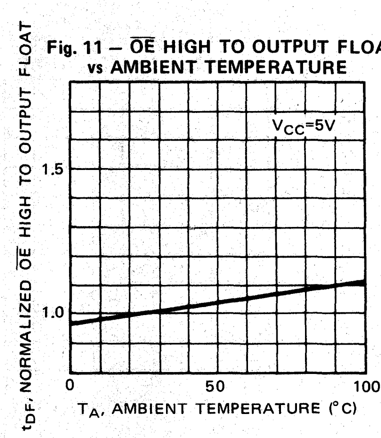


Fig. 12 — OUTPUT SOURCE CURRENT vs OUTPUT HIGH VOLTAGE

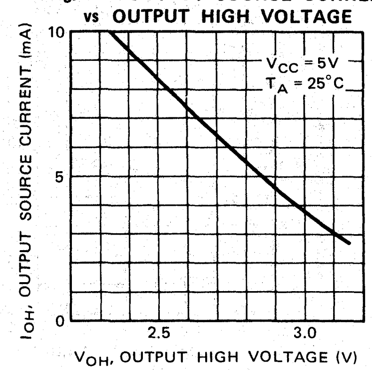


Fig. 13—OUTPUT SINK CURRENT vs OUTPUT LOW VOLTAGE

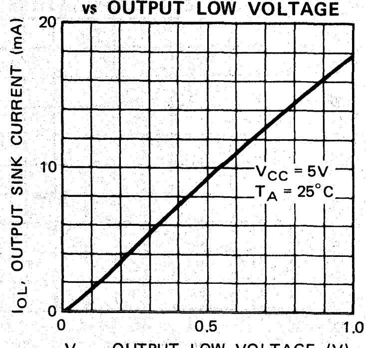
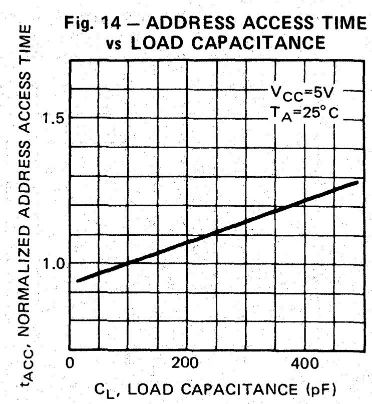


Fig. 14 — ADDRESS ACCESS TIME vs LOAD CAPACITANCE



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PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM 2764 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 15). The top gate is connected to the row decorder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 16). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 16.

Fig. 15 — MEMORY CELL

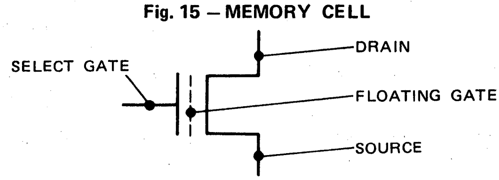
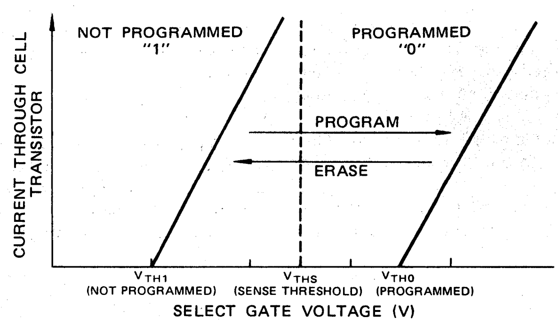


Fig. 16 — MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 2764 has all 65,536 bits in the "1", or high, state. "0's" are loaded into the MBM 2764 through the procedure of programming.

Normal Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are both at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL low-level pulse is applied to the $\overline{PGM}$ input to accomplish the programming. The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

Quick Programming

In addition to the standard 50 msec pulse width programming procedure, the MBM 2764 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown Fig. 17) untilizes a sequence of ONE millisecond pulse to program each location.

The programming mode is entered when +21V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{PGM}$ and $\overline{OE}$ are V_{IH}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit pattern are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 msec, TTL low-level pulse is applied to the $\overline{PGM}$ pin and after that additional pulse is applied to the $\overline{PGM}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to Fig. 17.)

1) Input the start address (Address=G)
2) Set the V_{CC} = 6V and V_{PP} = 21V

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PROGRAMMING/ERASING INFORMATION (continued)

3) Data input.
4) Compare the input data. If data are FF, jump to the 11). If data are not FF, proceed the next step.
5) Set the number of programming pulse to 0. (X=0)
6) Apply ONE programming pulse to $\overline{PGM}$ pin (t_{PW} =1 ms Typ.).
7) Count the programming pulse (X=X+1)
8) Compare the number of programming pulse. If X=20, jump to the 10). If X<20, proceed the next step.
9) Verify the data. If programmed data are the same as input data, proceed the next step. If programming data are not the same as input data, repeat the 6) thru 8).
10) Apply the additional programming pulse to the $\overline{PGM}$ pin (1 ms x X or X ms x 1).
11) Compare the address. If the programmed address is end address, proceed the next step. If the programmed address is not end address, proceed from step 3) for next address (G+1).
12) Verify the data. If programmed data are not the same as input data, the part is no good. If programmed data are the same as input data, programming is end.

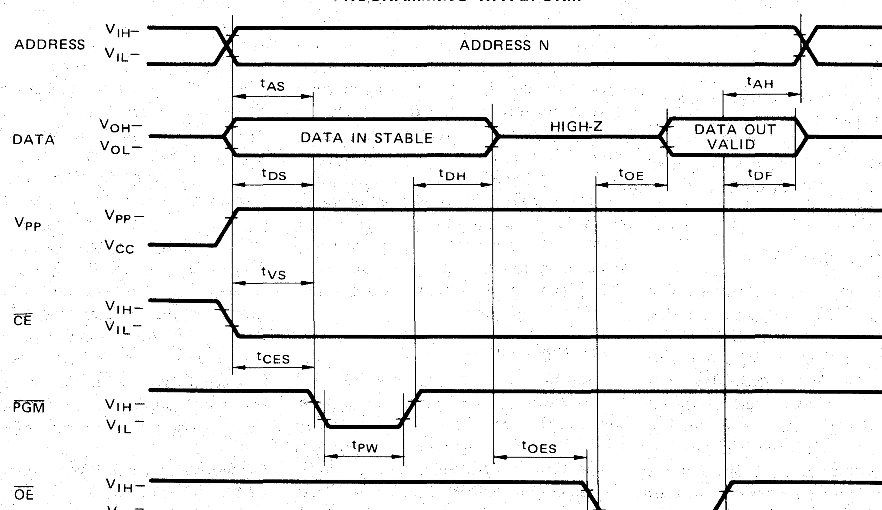
All that is required is that one 1 msec program pulse be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 1.05 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 2764 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM 2764. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM 2764 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 2764 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 2764, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING WAVEFORM



1. Nomal Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}^{*1} = 5V±5%, V_{PP}^{*2} = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			150 (100) *3	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$=$\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from V_{CC} to 21 volts or vise-versa.
*3 Value in parentheses is for "AB" version.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 5V±5%, V_{PP} = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
V_{PP} Setup Time	t_{VS}	2			μs
$\overline{PGM}$ Pulse Width	t_{PW}	45	50	55	ms

PROGRAMMING/ERASING INFORMATION (continued)

2. Quick Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}*1 = 6V±0.25V, V_{PP}*2 = 21V±0.5V

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			150 (100)*3	mA
Input Low Level	V_{IL}	−0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verfify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occuring the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from V_{IL} to V_{PP} volts or vise-versa.
*3 Value in parentheses is for "AB" version.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}*	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}*	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
V_{PP} Setup Time	t_{VS}	2			μs
$\overline{PGM}$ Pulse Width	t_{PW}	0.95	1	1.05	ms

* $t_{DH} + t_{OES} \geq 50\mu s$

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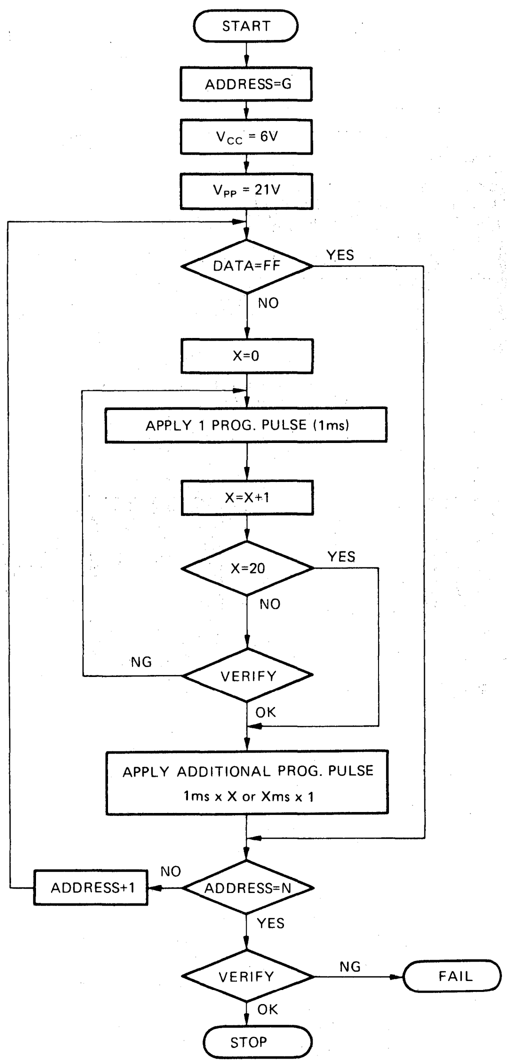
Fig. 17—PROGRAMMING FLOW CHART FOR Quick Pro™

V_{CC} = 6V±0.25V
V_{PP} = 21V±0.5V

Tpw = 1ms±50μs
(*=Xms±5%)

G : START ADDRESS
N : STOP ADDRESS

MAXIMUM 40ms + α/BYTE
MINIMUM 2ms + α/BYTE
(FOR EXAMPLE)
64K BIT EPROM
MAXIMUM 320sec + β
MINIMUM 16sec + β



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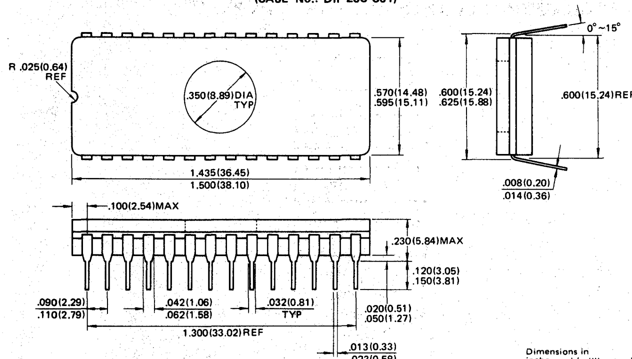
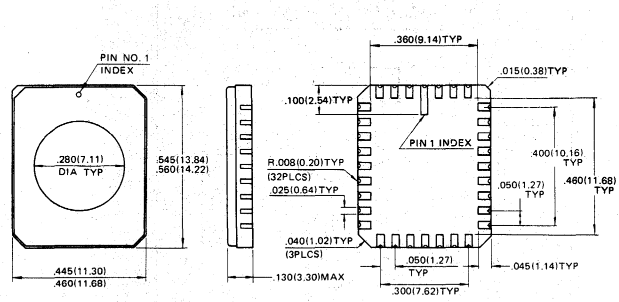
PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)



32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No. : LCC-32C-A01)



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

UV ERASABLE 131072-BIT READ ONLY MEMORY

MBM 27128-20
MBM 27128-25
MBM 27128-30

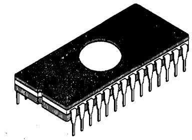
June 1984
Edition 2.0

MOS 131072 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

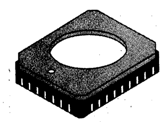
The Fujitsu MBM 27128 is a high speed 131,072-bit static N-channel MOS erasable and electrically reporogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin Dual-In-Line package and a 32-pad Leadless-Chip-Carrier with a transparent lid are used to package the MBM 27128. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27128 is fabricated using N-MOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 16,384 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



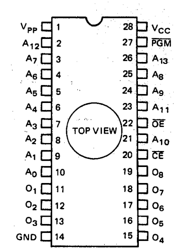
CERAMIC PACKAGE
DIP-28C-C01

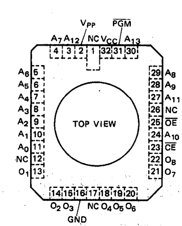


CERAMIC PACKAGE
LCC-32C-A01

- 16,384 words x 8 bits organization, fully decoded
- Simple programming requirements
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- Programs with one 50ms or 1ms pulses
- Low power
  Active: 550mW
  Standby: 193mW
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
- Fast access time:
  200ns max. (MBM 27128-20)
  250ns max. (MBM 27128-25)
  300ns max. (MBM 27128-30)
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Single +5V Supply, ±10% tolerance
- Standard 28-pin DIP package and 32-pad LCC
- Interchangeable with Intel 27128-type device

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Strage Temperature	T_{STG}	-65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	-0.6 to +7	V
Voltage on A_9 with Respect to GND	V_{A9}	-0.6 to +13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +22	V
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restriced to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal précautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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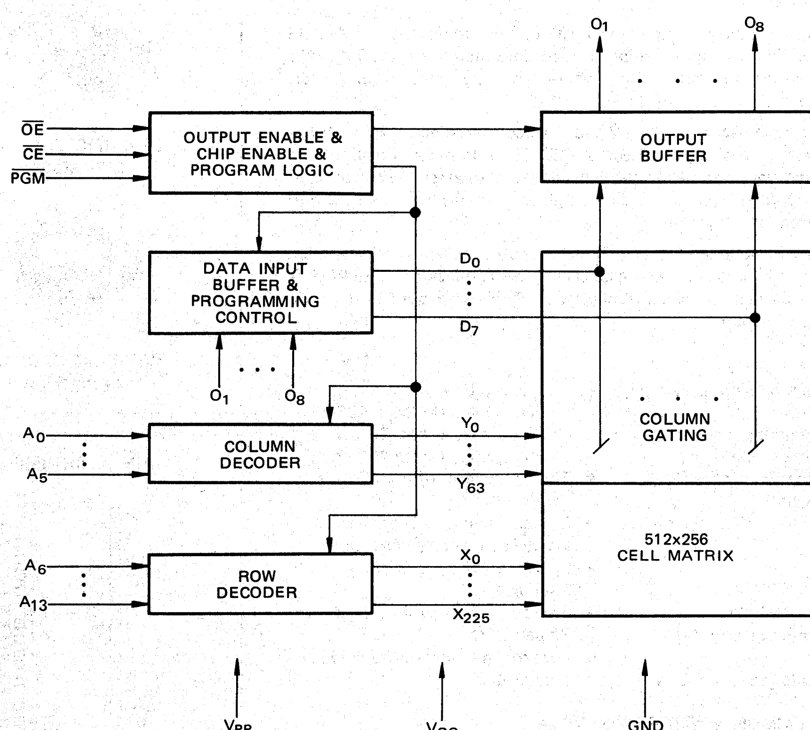
Fig. 1 — MBM 27128 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2~10, 23~26, 21)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
				Don't Care	V_{IL}			
Standby	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	GND

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} −0.6		V_{CC} + 0.6	V
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V
Input Low Voltage	V_{IL}	−0.1		0.8	V
Operating Temperature	T_A	0		70	°C

Note: * V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

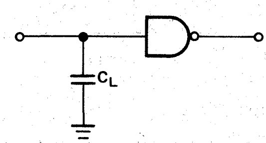
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.5V)	I_{LO}			10	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}			35	mA
V_{CC} Supply Current ($\overline{CE}$ = V_{IL})	I_{CC2}			100	mA
V_{PP} Supply Current (V_{PP} = V_{CC} ± 0.6V)	I_{PP}			15	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



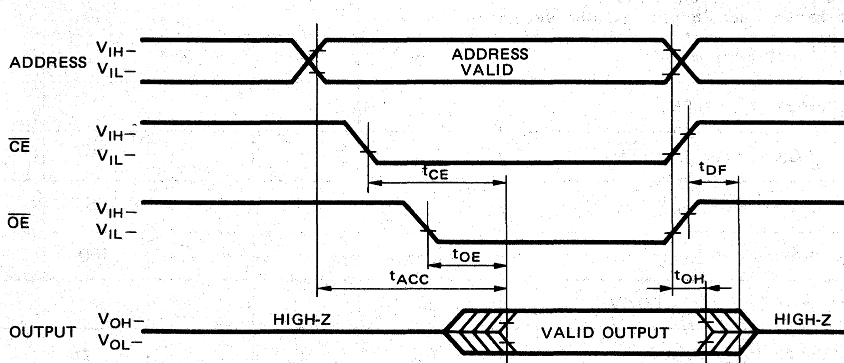
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27128-20			MBM 27128-25			MBM 27128-30			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time*1	t_{ACC}			200			250			300	ns
$\overline{CE}$ to Output Delay	t_{CE}			200			250			300	ns
$\overline{OE}$ to Output Delay*1	t_{OE}			70			100			150	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		105	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



CHARACTERISTICS CURVES

Fig. 3 –SUPPLY CURRENT (STANDBY) vs SUPPLY VOLTAGE

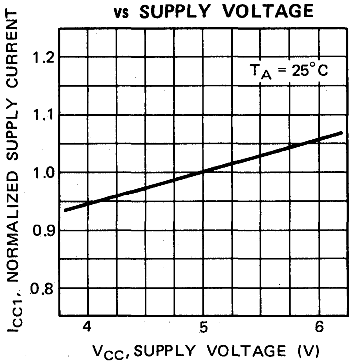


Fig. 4 – SUPPLY CURRENT (STANDBY) vs AMBIENT TEMPERATURE

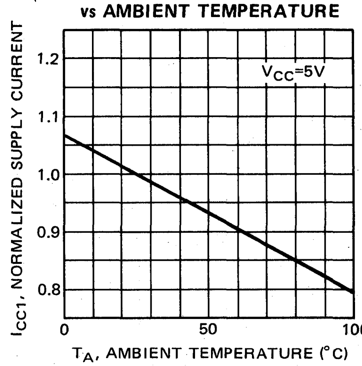


Fig. 5 – SUPPLY CURRENT (ACTIVE) vs SUPPLY VOLTAGE

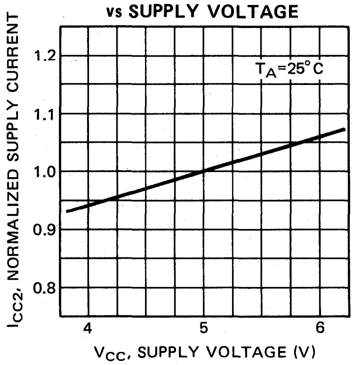


Fig. 6 – SUPPLY CURRENT (ACTIVE) vs AMBIENT TEMPERATURE

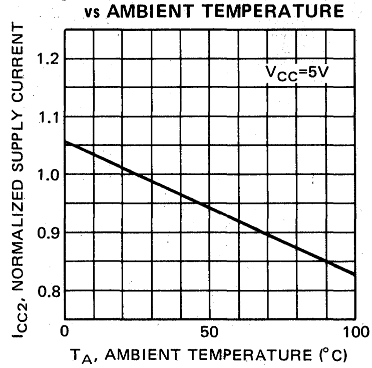


Fig. 7 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

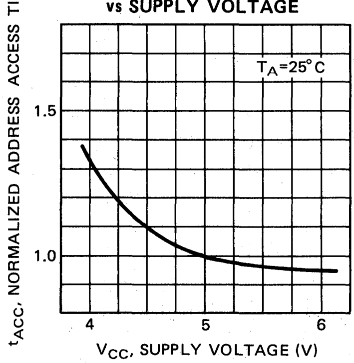
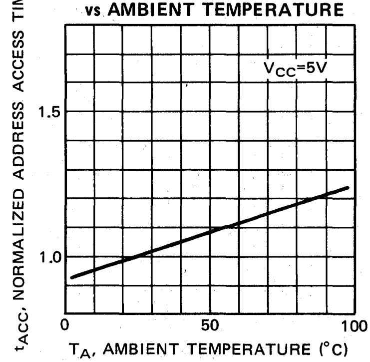


Fig. 8 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE



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CHARACTERISTICS CURVES (continued)

Fig. 9 — $\overline{CE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE

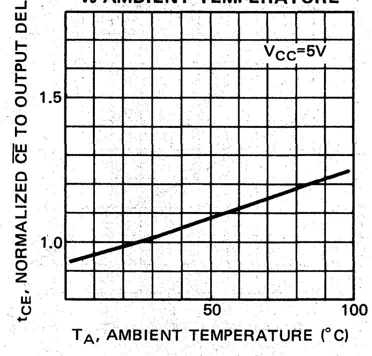


Fig. 10 — $\overline{OE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE

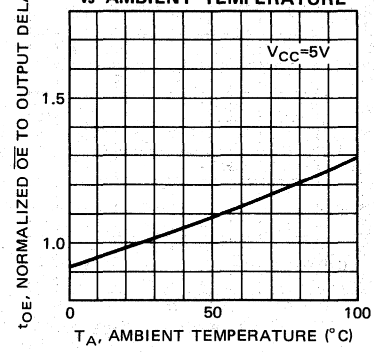


Fig. 11 — $\overline{OE}$ HIGH TO OUTPUT FLOAT vs AMBIENT TEMPERATURE

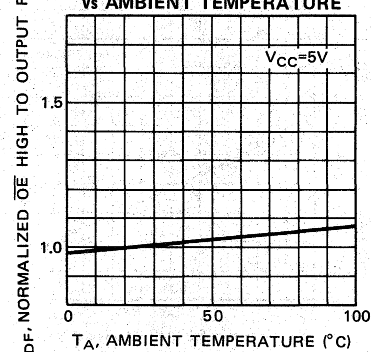


Fig. 12 — OUTPUT SOURCE CURRENT vs OUTPUT HIGH VOLTAGE

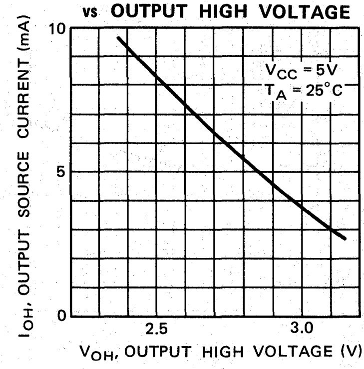


Fig. 13—OUTPUT SINK CURRENT vs OUTPUT LOW VOLTAGE

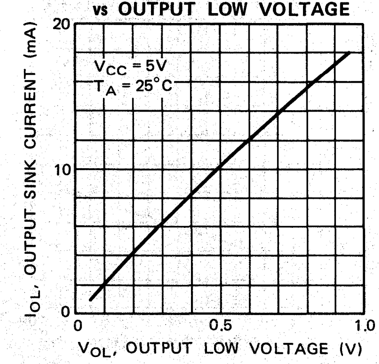
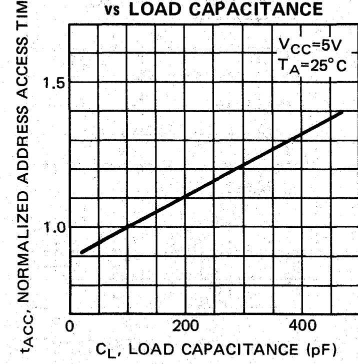


Fig. 14 — ADDRESS ACCESS TIME vs LOAD CAPACITANCE



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PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM 27128 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 15). The top gate is connected to the row decorder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 16). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 16.

Fig. 15 – MEMORY CELL

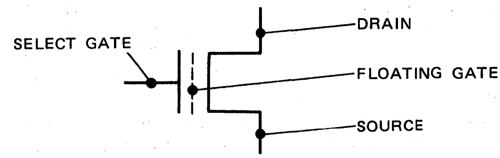
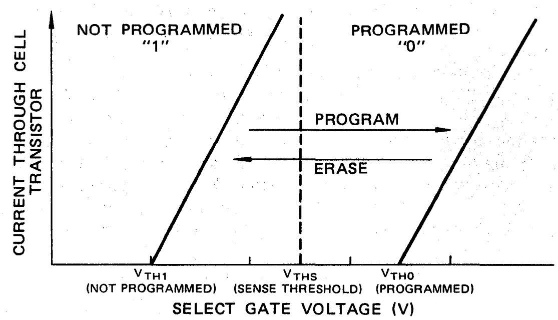


Fig. 16 – MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27128 has all 131,072 bits in the "1", or high, state. "0's" are loaded into the MBM 27128 through the procedure of programming.

Standard Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are both at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL low-level pulse is applied to the $\overline{PGM}$ input to accomplish the programming. The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

Quick Programming

In addition to the standard 50 msec pulse width programming procedure, the MBM 27128 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown Fig. 17) utilizes a sequence of a 1ms pulse to program each location.
The programming mode is entered when +21V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{PGM}$ and $\overline{OE}$ are V_{IH}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit pattern are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of a 1 msec, TTL low-level pulse is applied to the $\overline{PGM}$ pin and after that additional pulse is applied to the $\overline{PGM}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to Fig. 17.)

1) Input the start address (Address=G).

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PROGRAMMING/ERASING INFORMATION (continued)

2) Set the V_{CC} = 6V and V_{PP} =21V.
3) Input data.
4) Compare the input data with FF. If data are FF. go to the step 11). If not, proceed the next step.
5) Clear the counter. (X←0).
6) Apply ONE programming pulse to $\overline{PGM}$ pin (t_{PW} = 1 ms Typ.)
7) Increment the counter (X←X+1).
8) Compare the counter value with 20. If X=20, go to the step 10). If X<20, proceed the next step.
9) Verify the data. If programmed data are the same as input data, proceed the next step. If not, go back to the step 6).
10) Apply the additional programming pulse to the $\overline{PGM}$ pin (1 ms x X or X ms x 1).
11) Compare the address with the end address. If the programmed address is the end address, proceed the next step.
If not, go back to the step 3) for next address (G←G+1).
12) Verify the data. If the programmed data are not the same as the input data, the part is failed. If the programmed data are the same as the input data, programming is at an end.

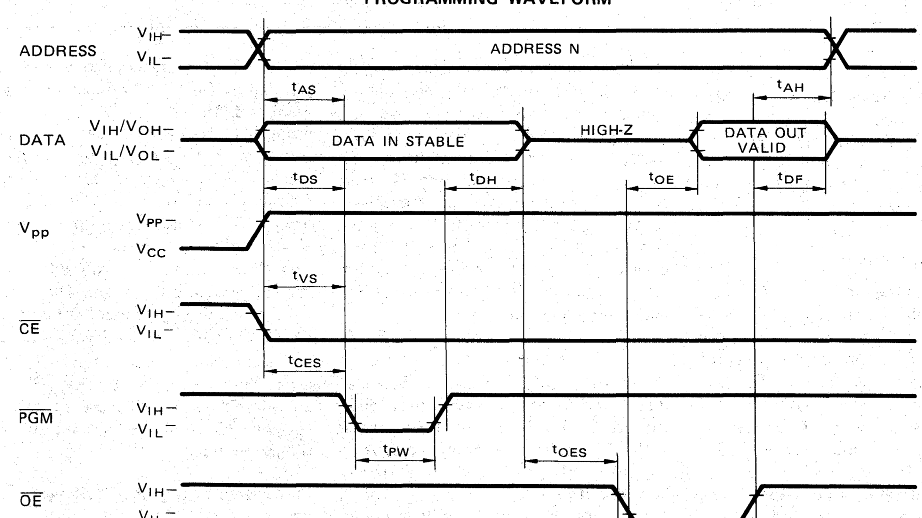
All that is required is that initial 1 msec program pulses and additional program pulse (21 ms Max.) be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 21 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 27128 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM 27128. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM 27128 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27128 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27128, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING WAVEFORM



1. Standard Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}^{*1} = 5V±5%, V_{PP}^{*2} = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			100	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$=$\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 to 21 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 5V±5%, V_{PP} = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	4			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
Programming Pulse Width	t_{PW}	45	50	55	ms

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PROGRAMMING/ERASING INFORMATION (continued)

8

2. Quick Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}*1= 6V±0.25V, V_{PP}*2=21V±0.5V

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			100	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verfify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occuring the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 6 to 21 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}*	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}*	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
Programming Pulse Width	t_{PW}	0.95		1.05	ms

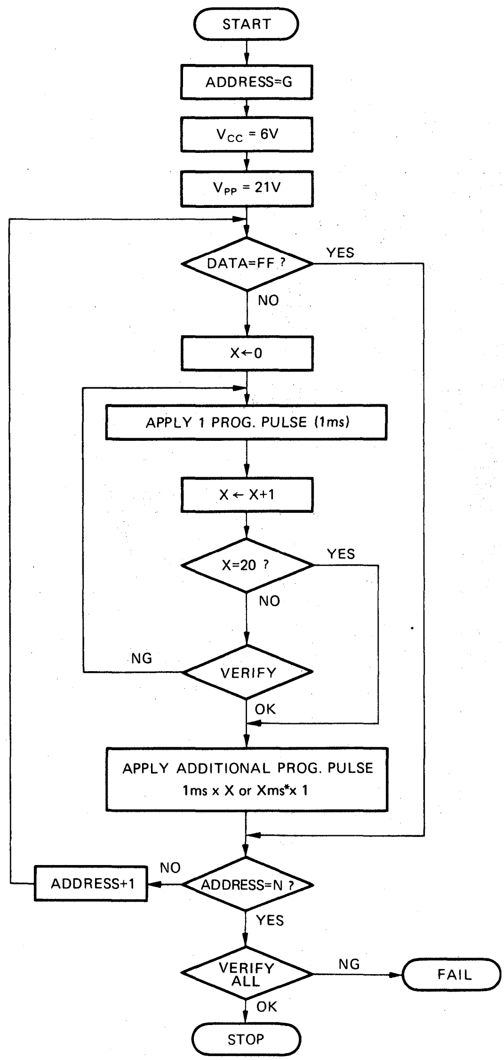
* $t_{DH} + t_{OES} \geqq 50\mu s$

Fig. 17—PROGRAMMING FLOW CHART FOR Quick Pro™

V_{CC} = 6V±0.25V
V_{PP} = 21V±0.5V

T_{PW} = 1ms±50μs
(* = Xms±5%)

G : START ADDRESS
N : STOP ADDRESS
X : COUNTER VALUE
MAXIMUM 42ms/BYTE
MINIMUM 1.9ms/BYTE



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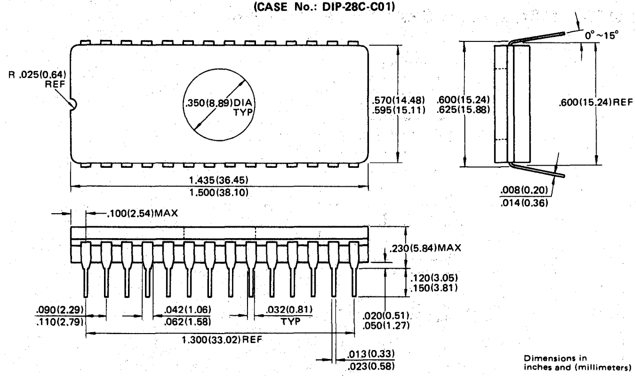
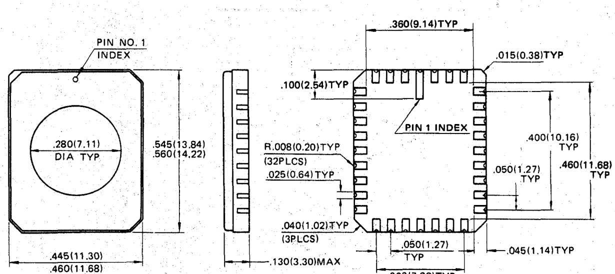
PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)



32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No. : LCC-32C-A01)



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

UV ERASABLE 262144-BIT READ ONLY MEMORY

MBM 27256-17
MBM 27256-20
MBM 27256-25

February 1986
Edition 3.0

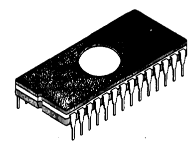
MOS 262144 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM 27256 is a high speed 262,144-bit static NMOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

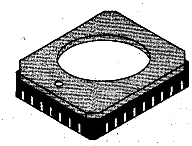
A 28-pin Dual In-Line package and a 32-pad Leadless Chip Carrier with a transparent lid is used to package the MBM 27256. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27256 is fabricated using NMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

- 32,768 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ algorithm
- Program voltage: 12.5V
- Low power requirement
  Active: 525mW
  Standby: 210mW
- No clocks required (fully static operation)
- Output Enable ($\overline{OE}$) pin for simple memory expansion
- Fast access time:
  170ns max. (MBM 27256-17)
  200ns max. (MBM 27256-20)
  250ns max. (MBM 27256-25)
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Single +5V supply, ±5% tolerance
- Standard 28-pin Ceramic (Cerdip) DIP: Suffix-Z
  Standard 32-pad Ceramic LCC: Suffix-CV

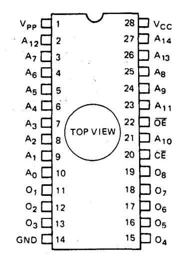


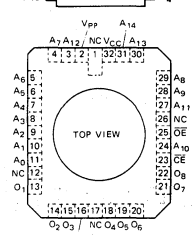
CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-A01

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +14	V
Voltage on A_9 with Respect to GND	V_{A9}	-0.6 to +13.5	V
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	-0.6 to +7	V
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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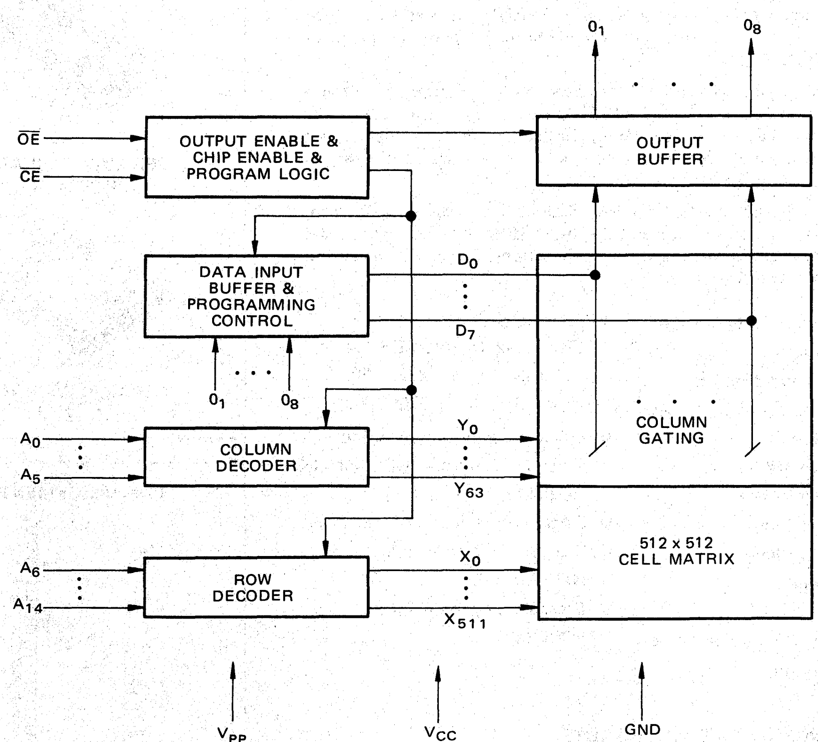
Fig. 1 — MBM 27256 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2 ~ 10, 21, 23, 25 ~ 27)	A_9 (24)	Data I/O (11 ~ 13, 15 ~ 19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5V	+5V	GND
Output Disable	A_{IN}	A_{IN}	High-Z	V_{IL}	V_{IH}	+5V	+5V	GND
Standby	Don't Care	Don't Care	High-Z	V_{IH}	Don't Care	+5V	+5V	GND
Program	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	+6V	+12.5V	GND
Program Verify	A_{IN}	A_{IN}	D_{OUT}	Don't Care	V_{IL}	+6V	+12.5V	GND
Program Inhibit	Dont't Care	Don't Care	High-Z	V_{IH}	V_{IH}	+6V	+12.5V	GND
Electronic Signature	A_{IN}	+12V	Code	V_{IL}	V_{IL}	+5V	+5V	GND

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltate*	V_{CC}	4.75	5.0	5.25	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} -0.6		V_{CC} +0.6	V
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

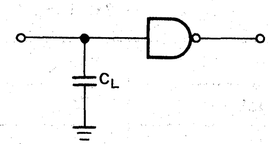
Note:*V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	$\lvert I_{LI} \rvert$			10	μA
Output Leakage Current (V_{OUT} = 5.25V)	$\lvert I_{LO} \rvert$			10	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}			40	mA
V_{CC} Supply Current ($\overline{CE}$ = V_{IL})	I_{CC2}			100	mA
V_{PP} Supply Current (V_{PP} = V_{CC} ± 0.6V)	I_{PP1}			5	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤ 20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



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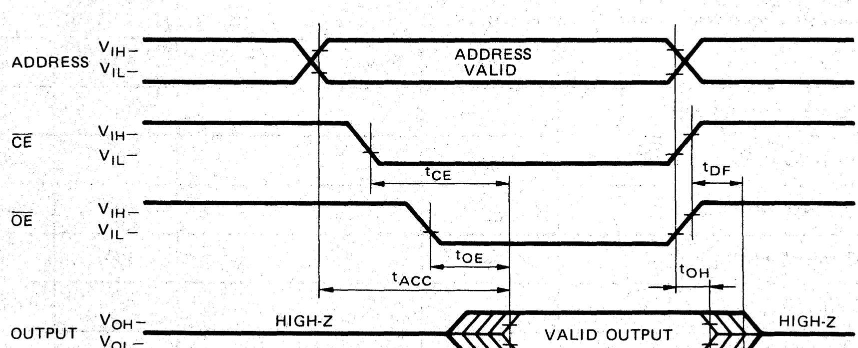
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27256-17			MBM 27256-20			MBM 27256-25			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time*1 ($\overline{CE} = \overline{OE} = V_{IL}$)	t_{ACC}			170			200			250	ns
$\overline{CE}$ to Output Delay ($\overline{OE} = V_{IL}$)	t_{CE}			170			200			250	ns
$\overline{OE}$ to Output Delay*1 ($\overline{CE} = V_{IL}$)	t_{OE}			75			75			100	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		105	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



CHARACTERISTICS CURVES

Fig. 3 – SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE

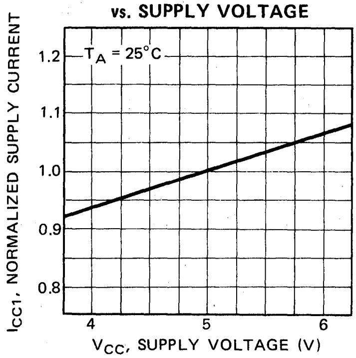


Fig. 4 – SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE

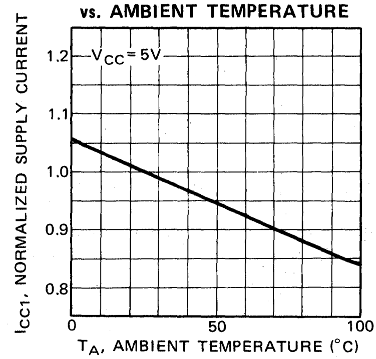


Fig. 5 – SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE

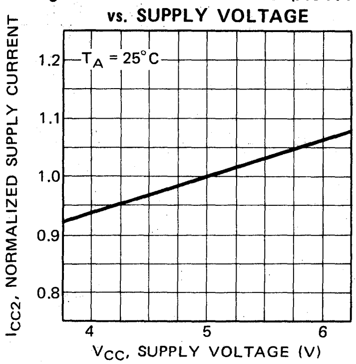


Fig. 6 – SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE

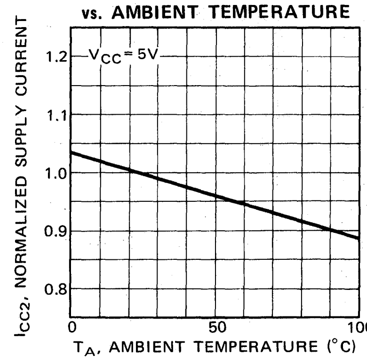


Fig. 7 – ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE

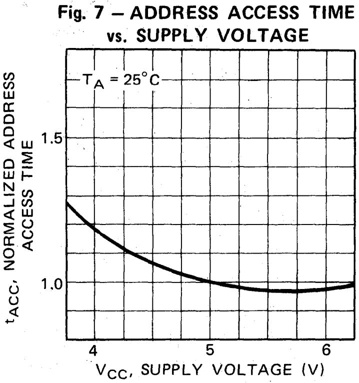


Fig. 8 – ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE

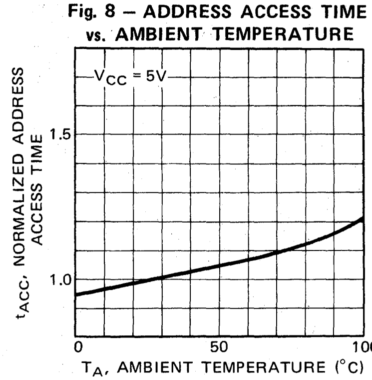


Fig. 9 — $\overline{CE}$ TO OUTPUT DELAY vs. AMBIENT TEMPERATURE

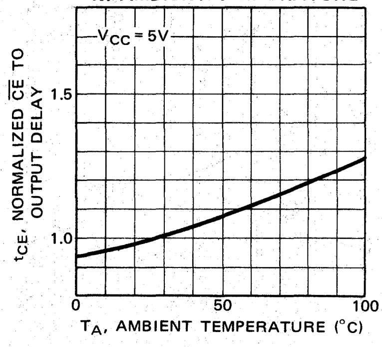


Fig. 10 — $\overline{CE}$ TO OUTPUT DELAY vs. SUPPLY VOLTAGE

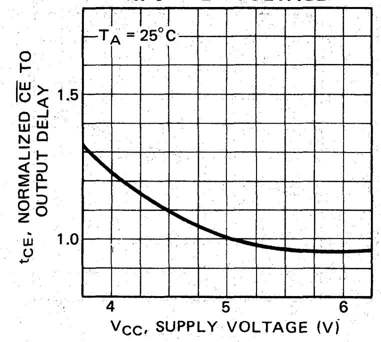


Fig. 11 — $\overline{OE}$ TO OUTPUT DELAY $\overline{OE}$ HIGH TO OUTPUT FLOAT vs. AMBIENT TEMPERATURE

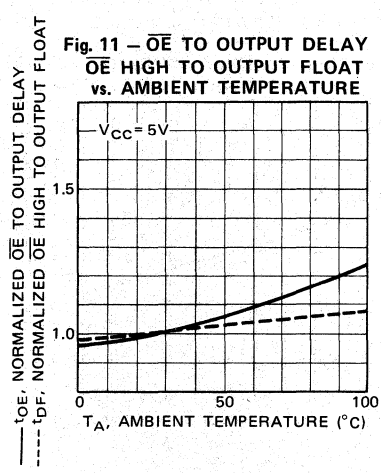


Fig. 12 — OUTPUT SOURCE CURRENT vs. OUTPUT HIGH VOLTAGE

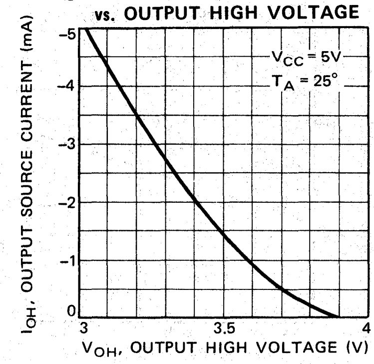


Fig. 13 — OUTPUT SINK CURRENT vs. OUTPUT LOW VOLTAGE

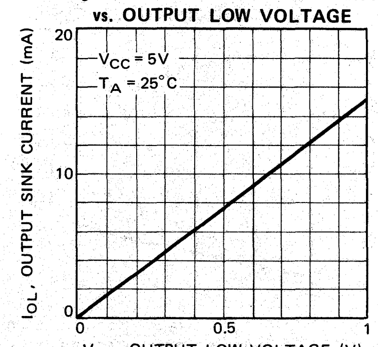
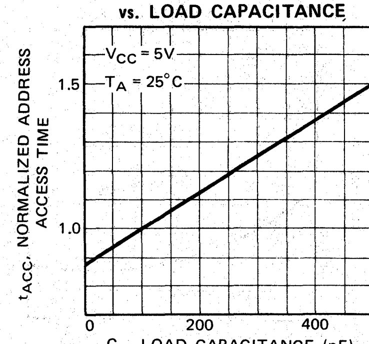


Fig. 14 — ADDRESS ACCESS TIME vs. LOAD CAPACITANCE



PROGRAMMING/ERASING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27256 has all 262,144 bits in the "1", or high state. "0's" are loaded into the MBM 27256 through the procedure of programming.

The MBM 27256 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{CE}$ and $\overline{OE}$ are V_{IH}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1ms programming pulse is applied to $\overline{CE}$ and after that one additional pulse which is 3 times as wide as previous pulse is applied to $\overline{CE}$ to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{CE}$ = V_{IH}.
3) Clear the programming pulse counter (X ← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1ms Typ.) to $\overline{CE}$.
6) Increment the counter (X ← X+1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X = 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G ← G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

ERASURE

In order to clear all locations of their programmed contents it is necessary to expose the MBM 27256 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM 27256. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 21 minutes.

The MBM 27256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27256 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27256, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ELECTRONIC SIGNATURE

The MBM 27256 has electronic signature mode which is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

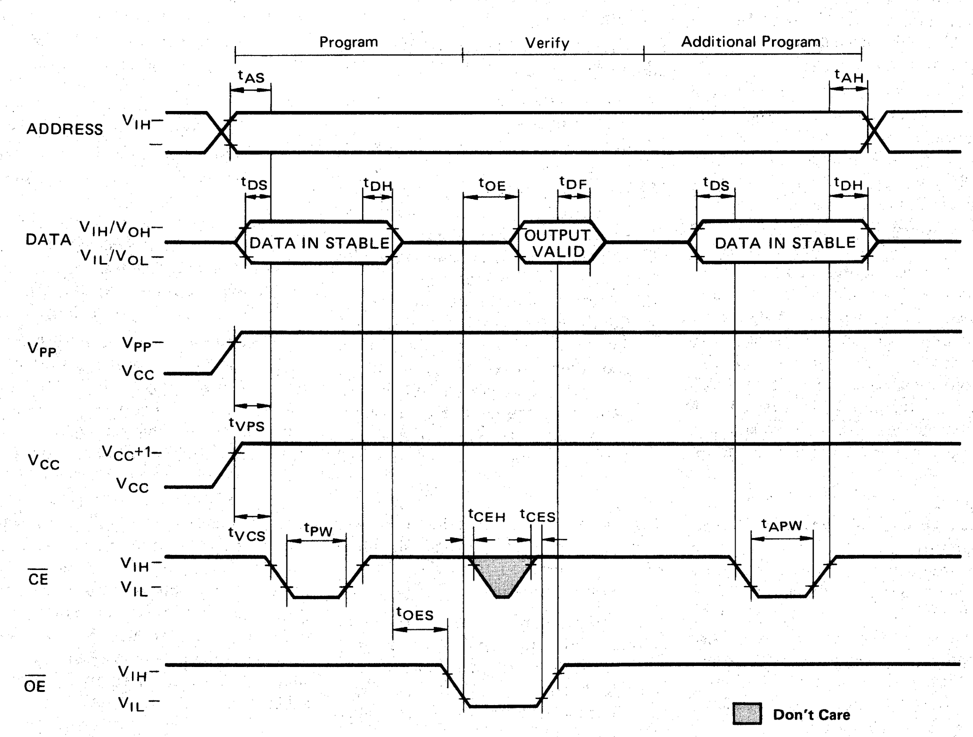
The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM 27256. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be hold at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	0	1	0	0	0	0	0	0	Device

Note: A_9 = 12V ± 0.5V
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}
A_{14} = Either V_{IL} or V_{IH}

PROGRAMMING/ERASING INFORMATION (Cont'd)

PROGRAMMING WAVEFORM



DC CHARACTERISTICS
(T_A = 25±5°C, V_{CC}*1=6V±0.25V, V_{PP}*2=12.5V±0.3V)

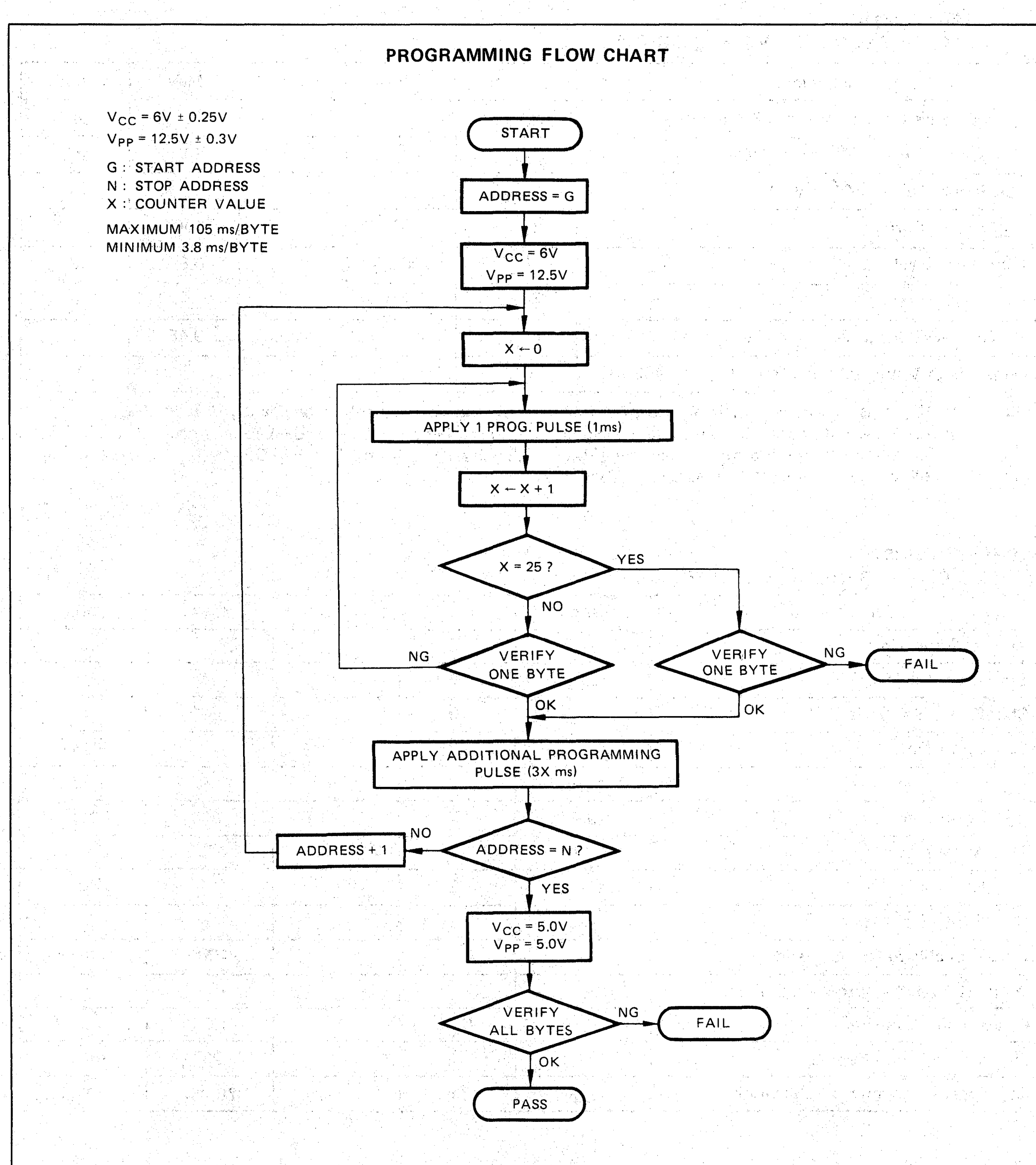
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	$\|I_{LI}\|$			10	μA
V_{PP} Supply Current ($\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{OE}$ = V_{IL})	I_{PP3}			5	mA
V_{CC} Supply Current	I_{CC3}			100	mA
Input Low Level	V_{IL}	–0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = –400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IH}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

AC CHARACTERISTICS
(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V)

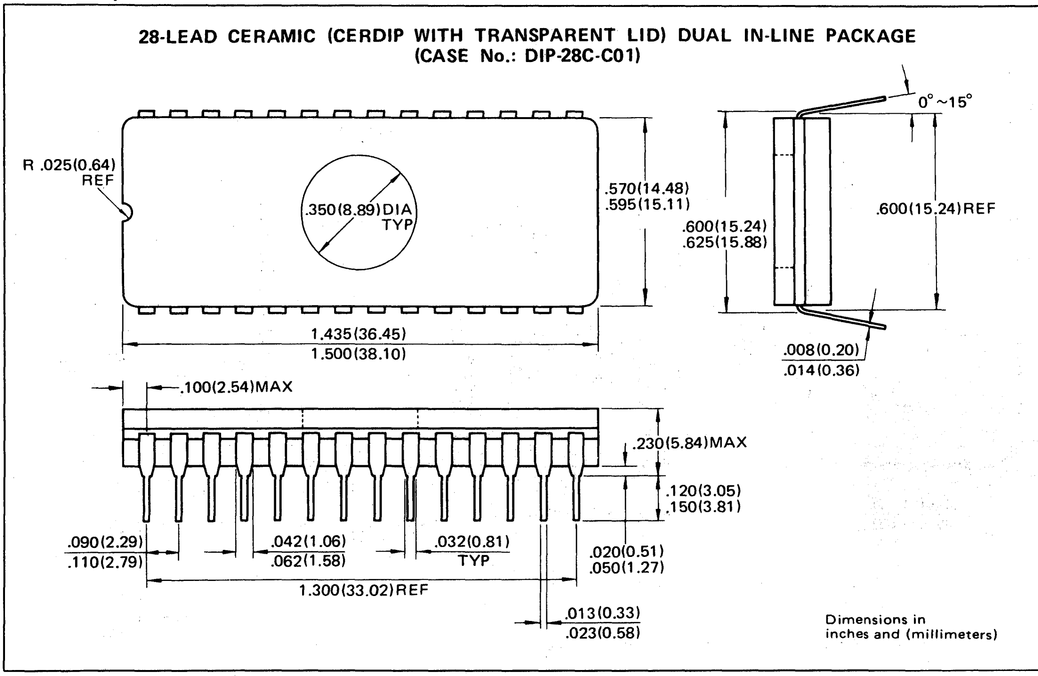
Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VPS}	2			μs
V_{CC} Setup Time	t_{VCS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Chip Enable Hold Time	t_{CEH}	2			μs
Output Enable to Output Valid	t_{OE}			120	ns
Output Disable to Output Float Delay	t_{DF}			105	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Programming Pulse Number		1		25	times
Additional Programming Pulse width	t_{APW}	2.85		78.75	ms

PROGRAMMING/ERASING INFORMATION (Cont'd)



PACKAGE DIMENSIONS

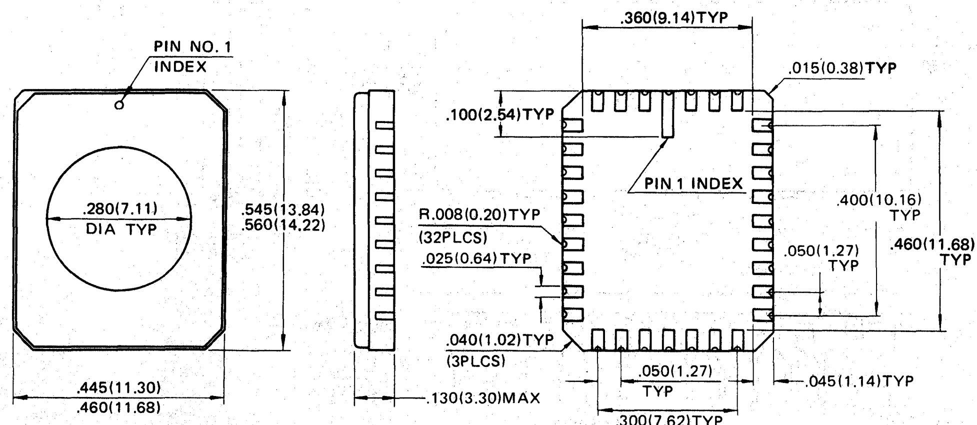
Standerd 28-pin Ceramic DIP (Suffix : -Z)



PACKAGE DIMENSIONS

Standerd 32-pad Ceramic LCC (Suffix : -CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No. : LCC-32C-A01)



*Shape of Pin index: Subject to change without notice

Dimensions in inches (millimeters)

Section 9

CMOS Erasable PROMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options	Sealing Method
9-3	MBM27C64-20 MBM27C64-25 MBM27C64-30	200 250 300	65536 bits (8192w x 8b)	28-pin Ceramic DIP 32-pad Ceramic LCC	CERDIP Metal
9-15	MBM27C128-17 MBM27C128-20 MBM27C128-25	170 200 250	131072 bits (16384w x 8b)	28-pin Ceramic DIP 32-pad Ceramic LCC	CERDIP Frit Glass
9-27	MBM27C256A-15 MBM27C256A-17 MBM27C256A-20 MBM27C256A-25	150 170 200 250	262144 bits (32768w x 8b)	28-pin Ceramic DIP 32-pad Ceramic LCC	CERDIP Frit Glass
9-37	MBM27C256H-10 MBM27C256H-12	100 120	262144 bits (32768w x 8b)	28-pin Ceramic DIP 32-pad Ceramic LCC	CERDIP Frit Glass
9-47	MBM27C512-15 MBM27C512-17	150 170	524288 bits (65536w x 8b)	28-pin Ceramic DIP 32-pad Ceramic LCC	CERDIP Frit Glas
9-59	MBM27C512-20 MBM27C512-25 MBM27C512-30	200 250 300	524288 bits (65536w x 8b)	28-pin Ceramic DIP 32-pad Ceramic LCC	CERDIP Frit Glass
9-71	MBM27C1000-15 MBM27C1000-20 MBM27C1000-25	150 200 250	1048576 bits (131072w x 8b)	32-pin Ceramic DIP 36-pad Ceramic LCC	CERDIP Frit Glass
9-83	MBM27C1001-15 MBM27C1001-20 MBM27C1001-25	150 200 250	1048576 bits (131072w x 8b)	32-pin Ceramic DIP 36-pad Ceramic LCC	CERDIP Frit Glass
9-95	MBM27C1024-15 MBM27C1024-20 MBM27C1024-25	150 200 250	1048576 bits (65536w x 16b)	40-pin Ceramic DIP 44-pad Ceramic LCC	CERDIP Frit Glass
9-107	MBM27C1028-15 MBM27C1028-20 MBM27C1028-25	150 200 250	1048576 bits (65536w x 16b)	28-pin Ceramic DIP 32-pad Ceramic LCC	CERDIP Frit Glass

9

9

FUJITSU

CMOS UV ERASABLE 65536-BIT READ ONLY MEMORY

MBM 27C64-20
MBM 27C64-25
MBM 27C64-30

June 1983
Edition 3.0

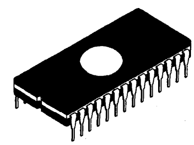
CMOS 8192x8BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM 27C64 is a high speed 65,536 bit static complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

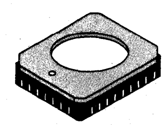
A 28-pin dual-in line package with a transparent lid and 32-Pad Leadless Chip Carrier (LCC) are used to package the MBM 27C64. The Transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C64 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8192 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

- CMOS power consumption 550μW max. ...... Standby
  40mW/MHz ...... Active
- 8,192 words by 8 bits organization, fully decoded
- Simple programming requirements
- Single location programming
- Programs with one 50ms or 1ms pulse
- No clock required (fully static operation)
- TTL compatible inputs and outputs
- Three state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion.
- Fast access time: 200 ns max. (MBM 27C64-20)
  250 ns max. (MBM 27C64-25)
  300 ns max. (MBM 27C64-30)
- Single +5V operation
- Standard 28-pin DIP package/32-pad LCC
- Interchangeable with 2764-type devices

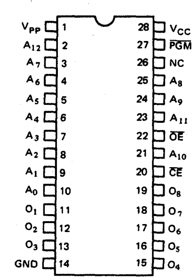


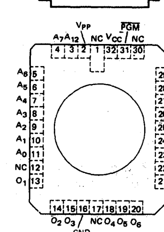
CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-A01

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (see NOTE)

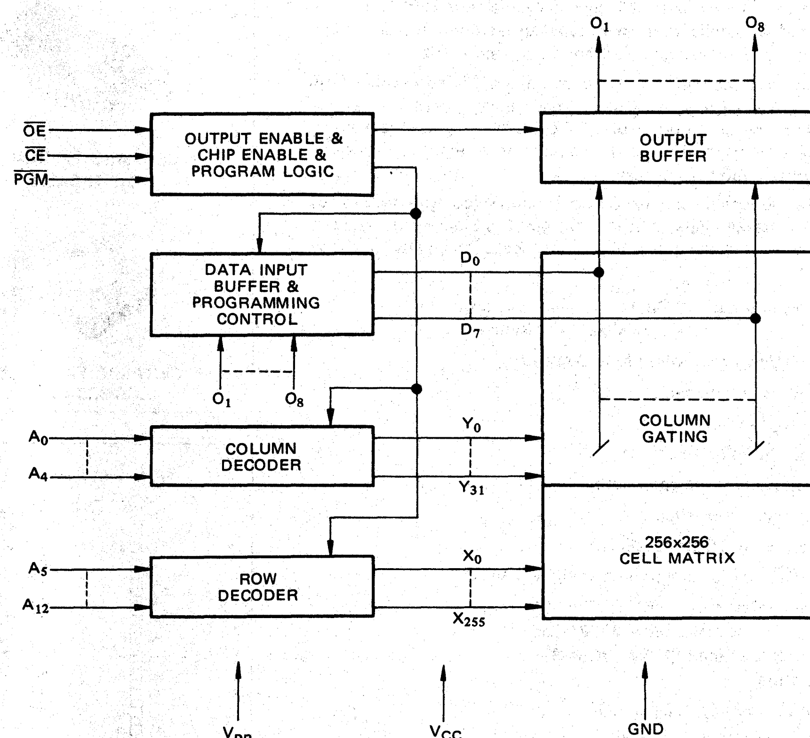
Rating	Symbol	Value	Unit
Temperature Under Bias	T_A	-25 to +85	°C
Storage Temperature	T_{stg}	-65 to +125	°C
Inputs/Outputs with Respect to GND	V_{IN}, V_{OUT}	-0.6 to +7	V
V_{PP} with Respect to GND	V_{PP}	-0.6 to +22	V
V_{CC} with Respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

9

Fig. 1 — MBM 27C64 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	–	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	–	8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2~10, 21, 23~25)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Output Disable	Don't Care	High Z	V_{IL}	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
				Don't Care	V_{IL}			
Stand By	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	GND

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} Supply Voltage(1)	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
V_{PP} Supply Voltage	V_{PP}	V_{CC} -0.6	–	V_{CC} +0.6	V	
Input High Voltage	V_{IH}	2.0	–	V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	-0.1	–	0.8	V	

Note: (1) V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

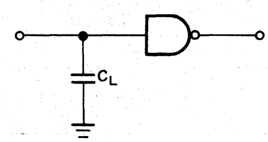
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.5V)	I_{LO}			10	μA
V_{PP} Supply Current	I_{PP}		1	100	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 0.3V, I_{OUT} = 0mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}$ = V_{IL})	I_{CC1}			30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0 mA)	I_{CC2}			30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = -400μA)	V_{OH}	2.4			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels: 0.8V to 2.2V
Input Rise and Fall Time: ≤20ns
Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
Output Load: 1 TTL gate and C_L = 100pF



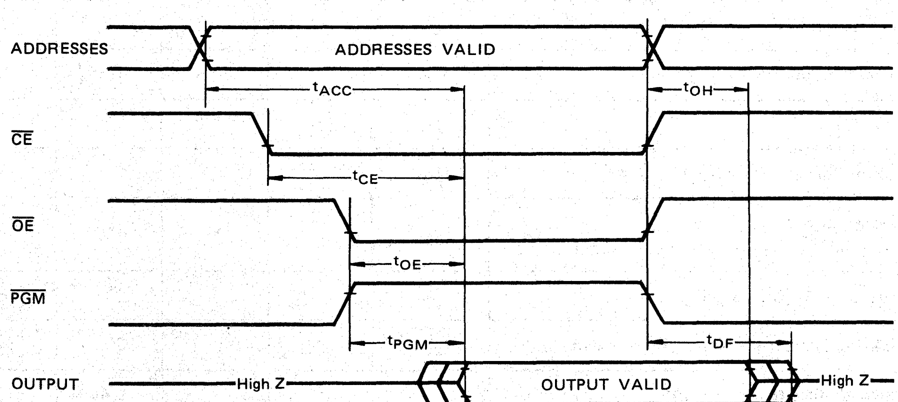
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27C64-20			MBM 27C64-25			MBM 27C64-30			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Accress to Output Delay ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH})	t_{ACC}			200			250			300	ns
$\overline{CE}$ to Output Delay ($\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH})	t_{CE}			200			250			300	ns
$\overline{OE}$ ot Output Delay ($\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH})	t_{OE}	10		70	10		100	10		120	ns
$\overline{PGM}$ to Output Delay ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{PGM}	10		70	10		100	10		120	ns
Output Enable High to Output Float (See Note)	t_{DF}	0		60	0		85	0		105	ns
Address to Output Hold	t_{OH}	0			0			0			ns

Note: t_{DF} is specified from $\overline{CE}$, $\overline{OE}$, or $\overline{PGM}$, whichever occurs first.

OPERATION TIMING DIAGRAM



Notes: (1) $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{CE}$, $\overline{OE}$, or $\overline{PGM}$, whichever occurs first.

9

CHARACTERISTICS CURVES

Fig. 3 — STANDBY CURRENT vs SUPPLY VOLTAGE

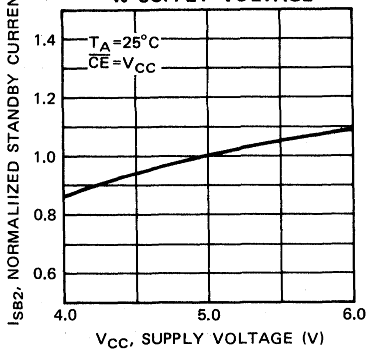


Fig. 4 — STANDBY CURRENT vs AMBIENT TEMPERATURE

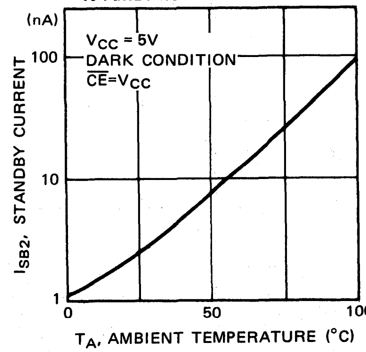


Fig. 5 — OPERATION CURRENT vs SUPPLY VOLTAGE

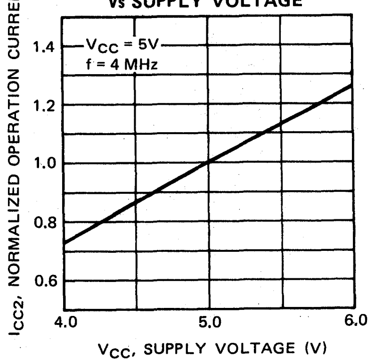


Fig. 6 — OPERATION CURRENT vs FREQUENCY

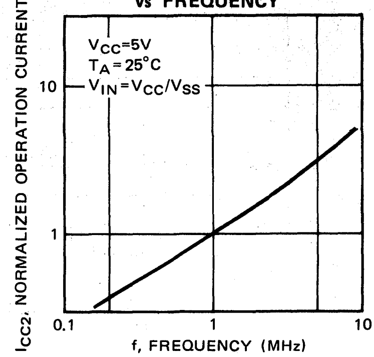


Fig. 7 — ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

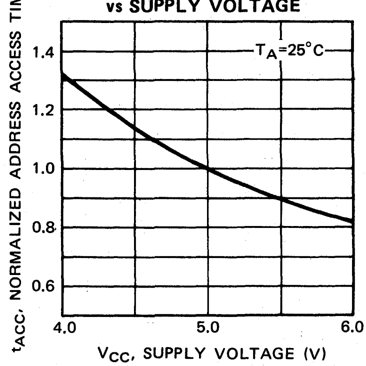
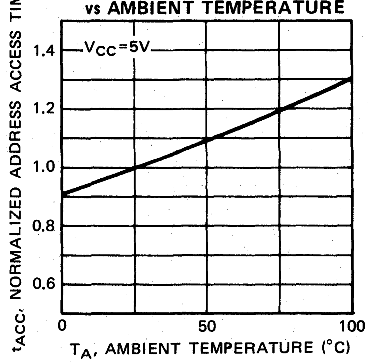


Fig. 8 — ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE



CHARACTERISTICS CURVES (continued)

Fig. 9 — $\overline{CE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE

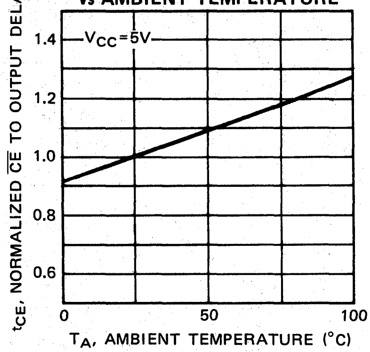


Fig. 10 — $\overline{OE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE

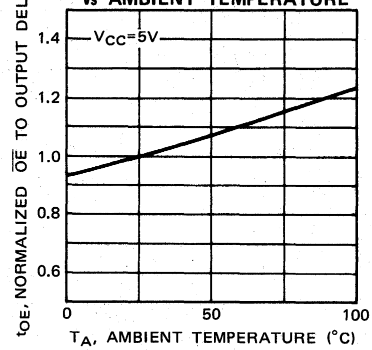


Fig. 11 — $\overline{OE}$ HIGH TO OUTPUT FLOAT vs AMBIENT TEMPERATURE

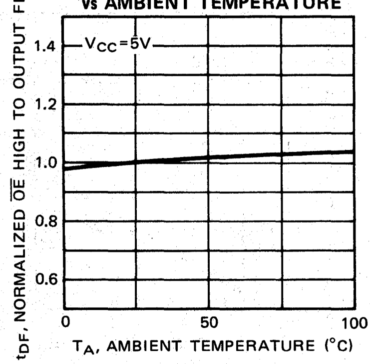


Fig. 12 — OUTPUT SOURCE CURRENT vs OUTPUT HIGH VOLTAGE

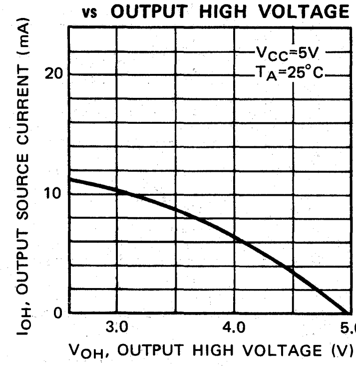


Fig. 13—OUTPUT SINK CURRENT vs OUTPUT LOW VOLTAGE

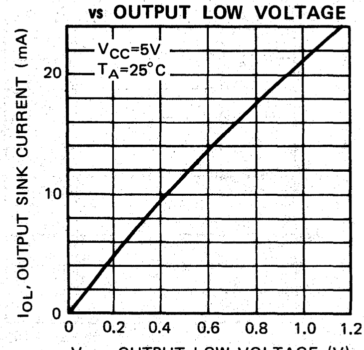
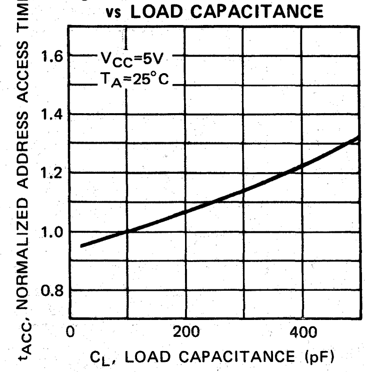


Fig. 14 — ADDRESS ACCESS TIME vs LOAD CAPACITANCE



9

PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM 27C64 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 15). The top gate is connected to the row decorder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 16). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 16.

Fig. 15 – MEMORY CELL

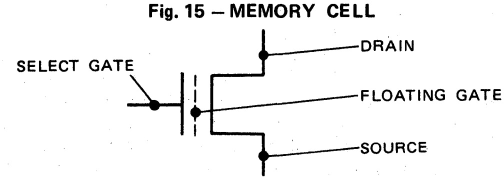
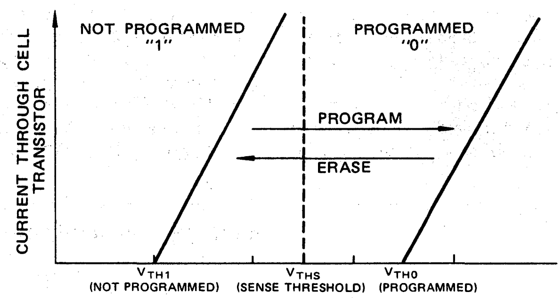


Fig. 16 – MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27C64 has all 65,536 bits in the "1", or high, state. "0's" are loaded into the MBM 27C64 through the procedure of programming.

Normal Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are both at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL Low-level pulse is applied to the $\overline{PGM}$ input to accomplish the programming. The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

Quick Programming

The programming mode is entered when +21V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{CE}$, $\overline{PGM}$ and $\overline{OE}$ are V_{IL} and V_{IH} respectively. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit pattern are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 msec, TTL low-level pulse is applied to the $\overline{PGM}$ pin and after that additional pulse is applied to the $\overline{PGM}$ pin to accomplish the programming.

Procedure of Quick Programming (Refer to the attached flow chart.)

1) Input the start address (Address=G)
2) Set the V_{CC} = 6V and V_{PP} = 21V
3) Data input.
4) Compare the input data. If data are FF, jump to the 11). If data are not FF, proceed the next step.
5) Set the number of programming pulse to 0. (X=0)
6) Apply 1 programming pulse to $\overline{PGM}$ pin (t_{PW} =1 ms Typ.).
7) Count the programming pulse

PROGRAMMING/ERASING INFORMATION (continued)

(X=X+1)

8) Compare the number of programming pulse. If X=20, jump to the 10). If X<20, proceed the next step.
9) Verify the data. If programmed data are same as input data, proceed the next step. If programming data are not same as input data, repeat the 6) thru 8).
10) Apply the additional programming pulse to the $\overline{PGM}$ pin (1 ms x X or X ms x 1).
11) Compare the address. If the programmed address is not end address, proceed the next step.
12) Verify the data. If programmed data are not same as input data, the part is no good. If programmed data are same as input data, programming is end.

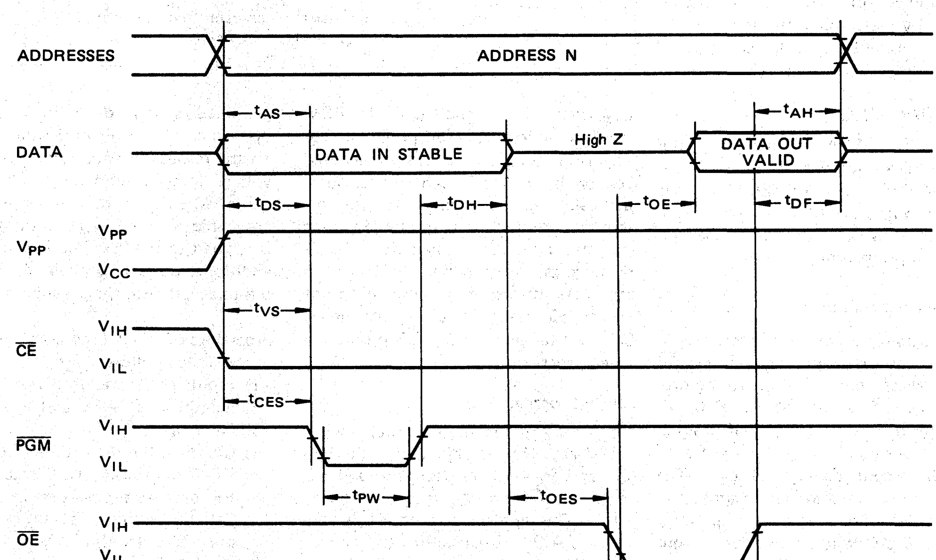
All that is required is that one 1 msec program pulse be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 1.05 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 27C64 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM 27C64. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM 27C64 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27C64 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27C64, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING WAVEFORM



1. NORMAL PROGRAMMING

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 5V±5%, V_{PP} = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			30	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400μA)	V_{OH}	2.4			V

Note: (1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
(2) V_{PP} must not be greater than 21.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 21 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 5V±5%, V_{PP} = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
Chip Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
V_{PP} Setup Time	t_{VS}	2			μs
$\overline{PGM}$ Pulse Width	t_{PW}	25	50	55	ms

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2. QUICK PROGRAMMING

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			30	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4			V

Note: (1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
(2) V_{PP} must not be greater than 21.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice-versa.

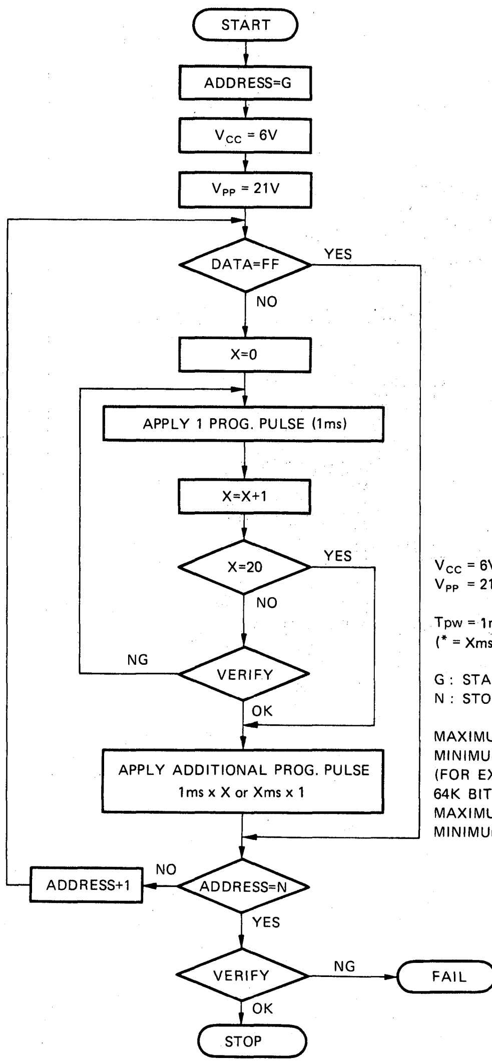
AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP}=21V±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time *	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time *	t_{DH}	2			μs
Chip Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
V_{PP} Setup Time	t_{VS}	2			μs
$\overline{PGM}$ Pulse Width	t_{PW}	0.95	1	1.05	ms

*$t_{DH} + t_{OES} \geqq 50\mu s$

FAST PROGRAMMING FLOW CHART FOR QUICK PROGRAMMING



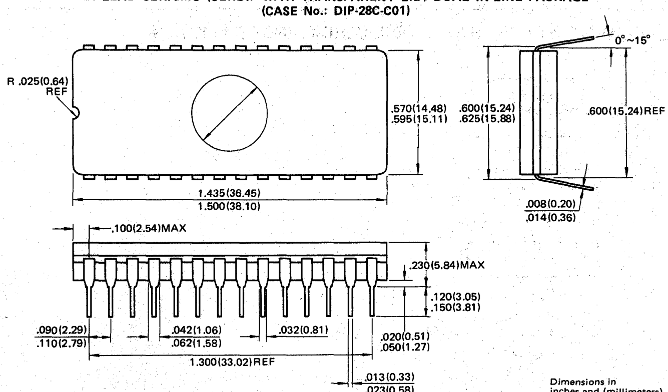
V_{CC} = 6V±0.25V
V_{PP} = 21V±0.5V

Tpw = 1ms ± 50μs
(* = Xms ±5%)

G : START ADDRESS
N : STOP ADDRESS

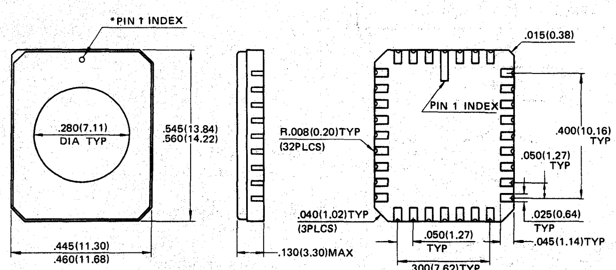
MAXIMUM (40ms + α)/BYTE
MINIMUM (2ms + α)/BYTE
(FOR EXAMPLE)
64K BIT EPROM
MAXIMUM 320sec. + β
MINIMUM 16sec. + β

28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)



Dimensions in inches and (millimeters)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A01)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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FUJITSU

CMOS UV ERASABLE 131072-BIT READ ONLY MEMORY

MBM 27C128-17
MBM 27C128-20
MBM 27C128-25

February 1987
Edition 2.0

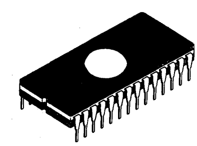
CMOS 131072 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM 27C128 is a high speed 131,072 bit static complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

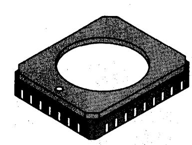
A 28-pin dual-in line package with a transparent lid and 32-Pad Leadless Chip Carrier (LCC) are used to package the MBM 27C128. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C128 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 16,384 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

- CMOS power consumption
  Standby : 100μA max.
  Active : 30mA max.
- 16,384 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- Programs with one 50ms or 1ms pulses
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
- Fast access time :
  170ns max. (MBM 27C128-17)
  200ns max. (MBM 27C128-20)
  250ns max. (MBM 27C128-25)
- Three-state output with OR-tie capability
- Output Enable (OE) pin for simplified memory expansion
- Single +5V supply, ± 10% tolerance
- Standard 28-pin Ceramic DIP : (Suffix: -Z)
- Standard 32-pad Ceramic LCC : (Suffix: -TV)



CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-F01

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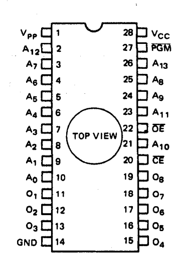
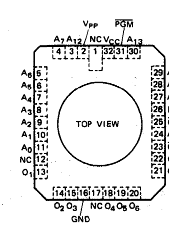
PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

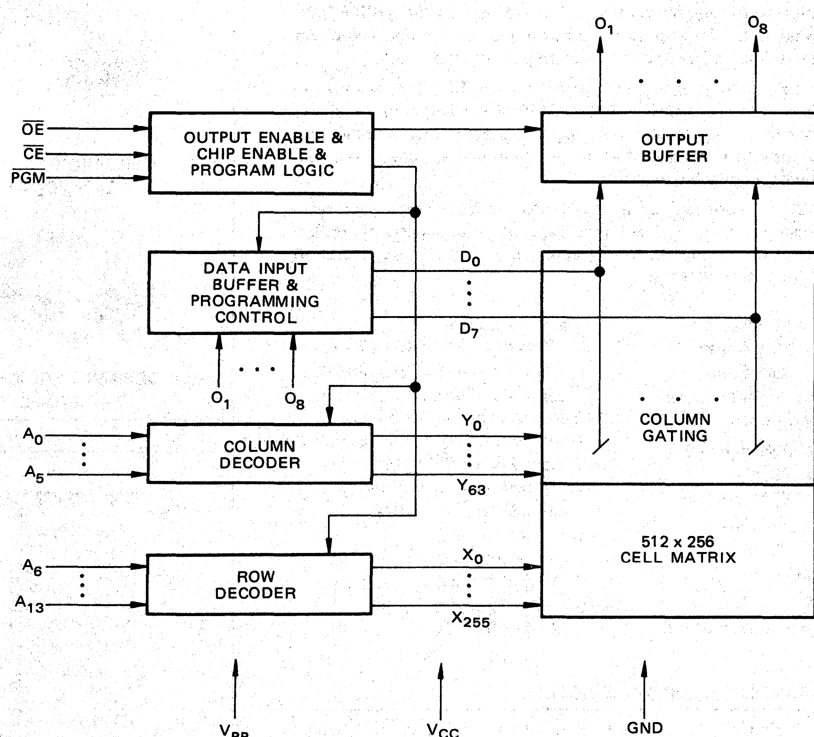
Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	-0.6 to V_{CC}+0.6	V
Voltage on A_9 with Respect to GND	V_{A9}	-0.6 to +13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +22	V
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Quick Pro™ is a trademark of FUJITSU LIMITED.

Fig. 1 – MBM 27C128 BLOCK DIAGRAM



9

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2 to 10, 21, 23 to 26)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
				Don't Care	V_{IL}			
Standby	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	GND

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Supply Voltage*1	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	$V_{CC}-0.6$		$V_{CC}+0.6$	V
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.1		0.8	V
Operating Temperature	T_A	0		70	°C

Note: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

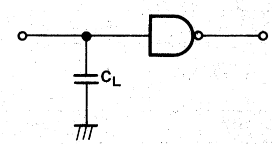
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Load Current (V_{IN} = 5.5V)	$\|I_{LI}\|$			10	μA
Output Leakage Current (V_{OUT} = 5.5V)	$\|I_{LO}\|$			10	μA
V_{PP} Supply Current	I_{PP1}		1	100	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{CE}$ = $V_{CC}\pm0.3V$, I_{OUT} = 0mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC1}		2	30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0mA)	I_{CC2}		4	30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = −100μA)	V_{OH2}	$V_{CC}-0.7$			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels: 0.8V to 2.2V
Input Rise and Fall Times: ≤20ns

Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for output

Output Load: 1 TTL gate and C_L = 100pF



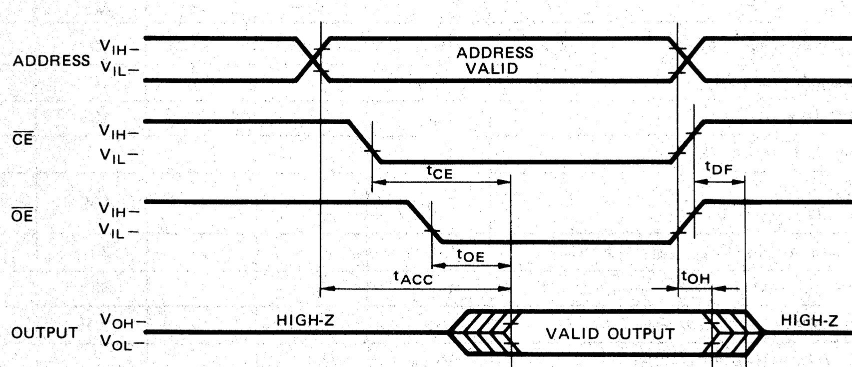
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27C128-17			MBM 27C128-20			MBM 27C128-25			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time*1	t_{ACC}			170			200			250	ns
$\overline{CE}$ to Output Delay	t_{CE}			170			200			250	ns
$\overline{OE}$ to Output Delay*1	t_{OE}			70			70			100	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		60	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



PROGRAMMING/ERASING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27C128 has all 131,072 bits in the "1", or high, state. "0's" are loaded into the MBM 27C128 through the procedure of programming.

Standard Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are both at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL low-level pulse is applied to the $\overline{PGM}$ input to accomplish the programming. the procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

Quick Programming

In addition to the standard 50 msec pulse width programming procedure, the MBM 27C128 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm utilizes a sequence of a 1ms pulse to program each location. The programming mode is entered when +21V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{PGM}$ and $\overline{OE}$ are V_{IH}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit patgterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of a 1 msec, TTL low-level pulse is applied to the $\overline{PGM}$ pin and after that additional pulse is applied to the $\overline{PGM}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flow chart.)

1) Input the start address (Address=G)
2) Set the V_{CC}=6V and V_{PP}=21V
3) Input data.
4) Compare the input data with FF. If data are FF, go to the step 11). If not, proceed the next step.
5) Clear the counter (X←0).
6) Apply ONE programming pulse to $\overline{PGM}$ pin (t_{PW} = 1ms Typ.).
7) Inclement the counter (X←X+1).
8) Compare the counter value with 20. If X=20, go to the step 10). If X<20, proceed the next step.
9) Verify the data. If the programmed data are the same as the input data, proceed the next step. If not, go back to the step 6).
10) Apply the additional programming pulse to the $\overline{PGM}$ pin (1ms x X or Xms x 1).
11) Compare the address with the end address. If the programmed address is the end address, proceed the next step. If not, go back to the step 3) for next address (G←G+1).
12) Verify the data. If the programmed data are not the same as the input data, the part is failed. If the programmed data the same as the input data, programming is at an end.

All that is required is that initial 1 msec program pulse and additional program pulse (21 msec Max.) be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 21 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 27C128 to an ultraviolet light source. A dosage of 15 W-seconds/cm² is required to completely erase an MBM 27C128. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm² for 15 to 21 minutes. The MBM 27C128 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27C128 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although

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PROGRAMMING/ERASING INFORMATION (continued)

erasure time will be much longer than with an UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27C128, and exposure to the device should be prevented to realize maximum system reliability. If used in light environment, the package windows should be covered by an opaque label or substance.

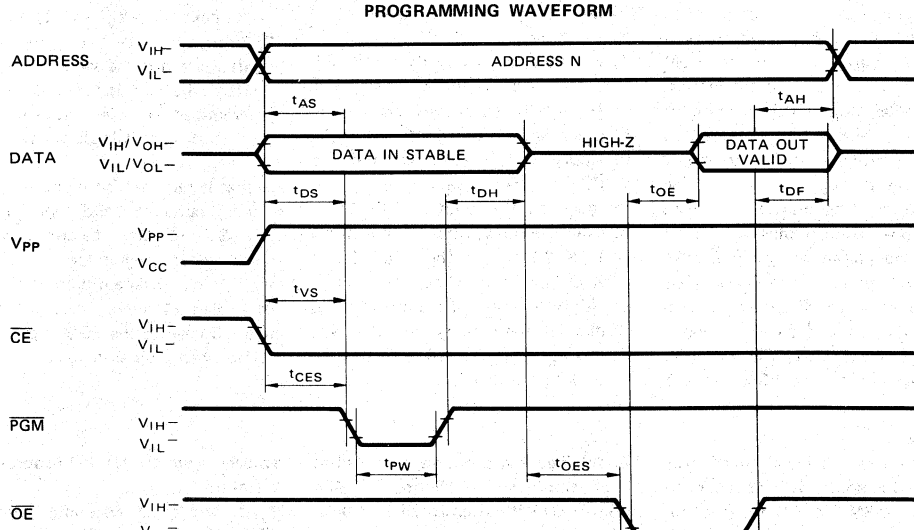
ELECTRONIC SIGNATURE

The MBM 27C128 has an electronic signature mode which can be intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.
The electronic signature is activated when +12V is applied to the address line A_9 (pin 24) of the MBM 27C128. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 through A_{13} must be hold at V_{IL} during the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Mnufacture
V_{IH}	1	0	0	0	0	1	0	1	Device

Note: $A_9 = 12V \pm 0.5V$
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.

PROGRAMMING WAVEFORM



1. Standard Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}^{*1} = 5V±5%, V_{PP}^{*2} = 21±0.5V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP2}			40	mA
V_{CC} Supply Current	I_{CC3}			30	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$=$\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 to 21 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 5V±5%, V_{PP} = 21±0.5V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
$\overline{PGM}$ Pulse Width	t_{PW}	25	50	55	ms

PROGRAMMING/ERASING INFORMATION (continued)

2. Quick Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}^{*1} = 6V±0.25V, V_{PP}^{*2} = 21V±0.5V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP2}			40	mA
V_{CC} Supply Current	I_{CC3}			30	mA
Input Low Level	V_{IL}	–0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = –400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occur the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 6 to 21 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V)

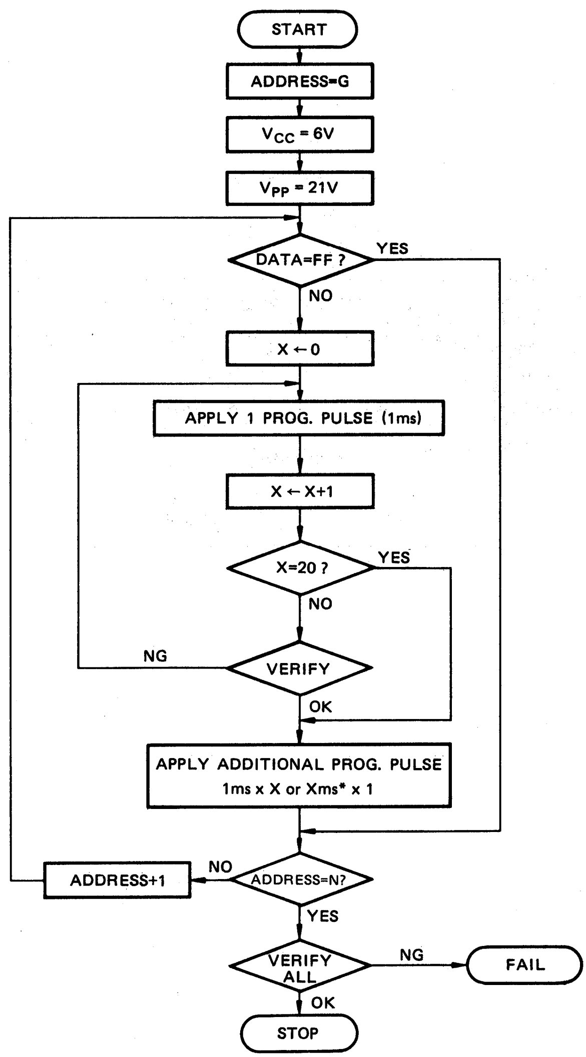
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
$\overline{PGM}$ Pulse Width	t_{PW}	0.95	1	1.05	ms

PROGRAMMING FLOW CHART FOR Quick Pro™

V_{CC} = 6V±0.25V
V_{PP} = 21V±0.5V

T_{PW} = 1ms±50µs
(* = Xms±5%)

G : START ADDRESS
N : STOP ADDRESS
X : COUNTER VALUE
MAXIMUM 42ms/BYTE
MINIMUM 1.9ms/BYTE



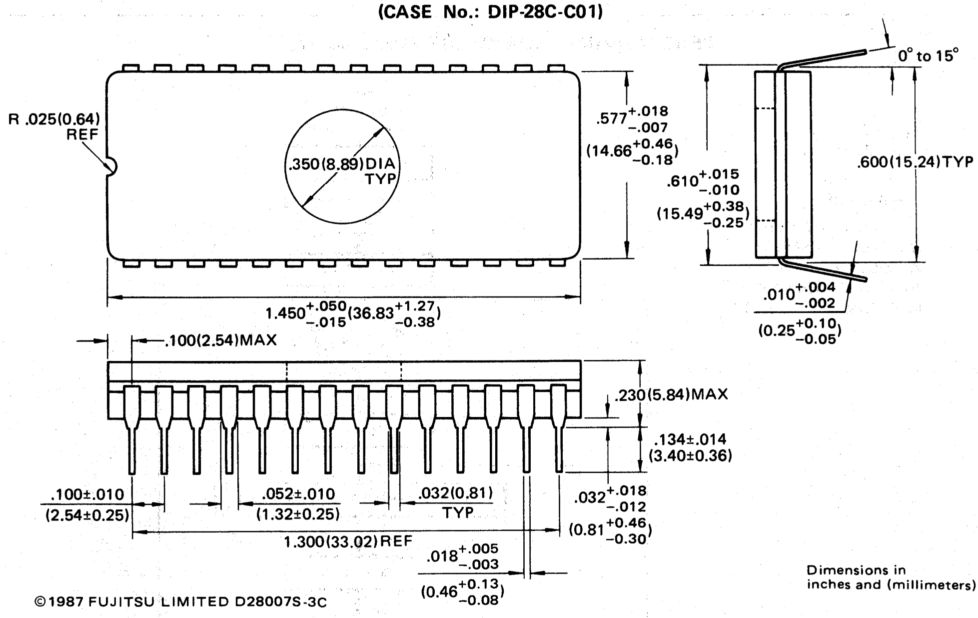
Quick Pro™ is a trademark of FUJITSU LIMITED.

9

PACKAGE DIMENSIONS

Standard 28-pin Ceramic DIP(Suffix: -Z)

28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)



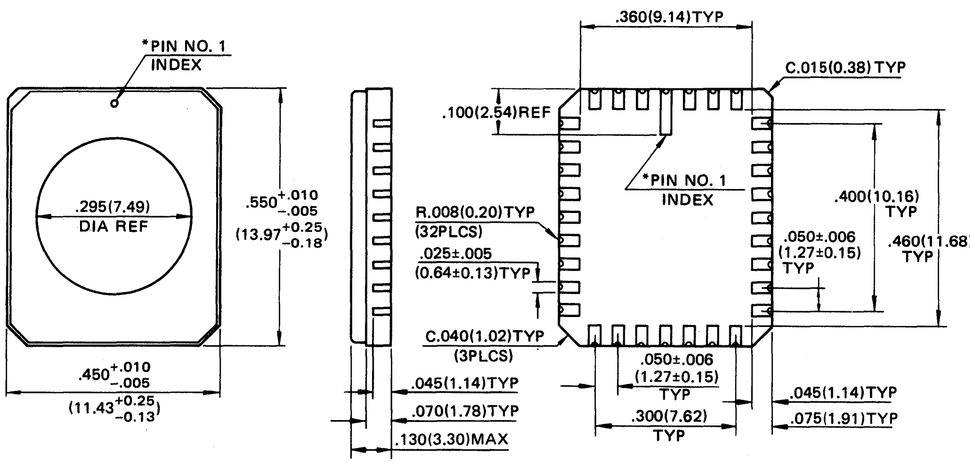
Dimensions in inches and (millimeters)

9

PACKAGE DIMENSIONS

Standard 32-pad Ceramic LCC (Suffix: -TV)

32-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in inches and (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

9

CMOS UV ERASABLE 262144-BIT READ ONLY MEMORY

MBM27C256A-15
MBM27C256A-17
MBM27C256A-20
MBM27C256A-25

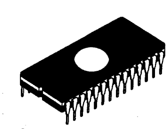
September 1987
Edition 2.0

CMOS 262144 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

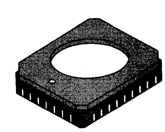
The Fujitsu MBM 27C256A is a high speed 262,144 bits complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad Leadless Chip Carrier (LCC) are used to package the MBM 27C256A. The transparent lid allows the user to expose the device to ultra-violet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C256A is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



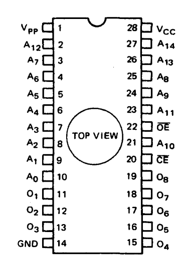
CERAMIC PACKAGE
DIP-28C-C01

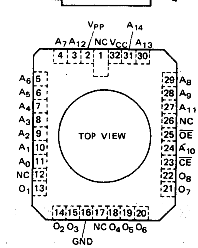


CERAMIC PACKAGE
LCC-32C-F01

- CMOS power consumption
  Standby: 550 μW max.
  Active: 41 mW/MHz
- 32,768 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ algorithm
- Programming voltage: 12.5V
- No clocks required (fully static operation)
- Three-state output with OR-tie capability
- Fast access time:
  150 ns max. (MBM27C256A-15)
  170 ns max. (MBM27C256A-17)
  200 ns max. (MBM27C256A-20)
  250 ns max. (MBM27C256A-25)
- TTL compatible inputs/outputs
- Single +5V supply, ±10% tolerance
- Standard 28-pin ceramic DIP: Suffix-Z
- Standard 32-pad ceramic LCC: Suffix-TV

PIN ASSIGNMENT





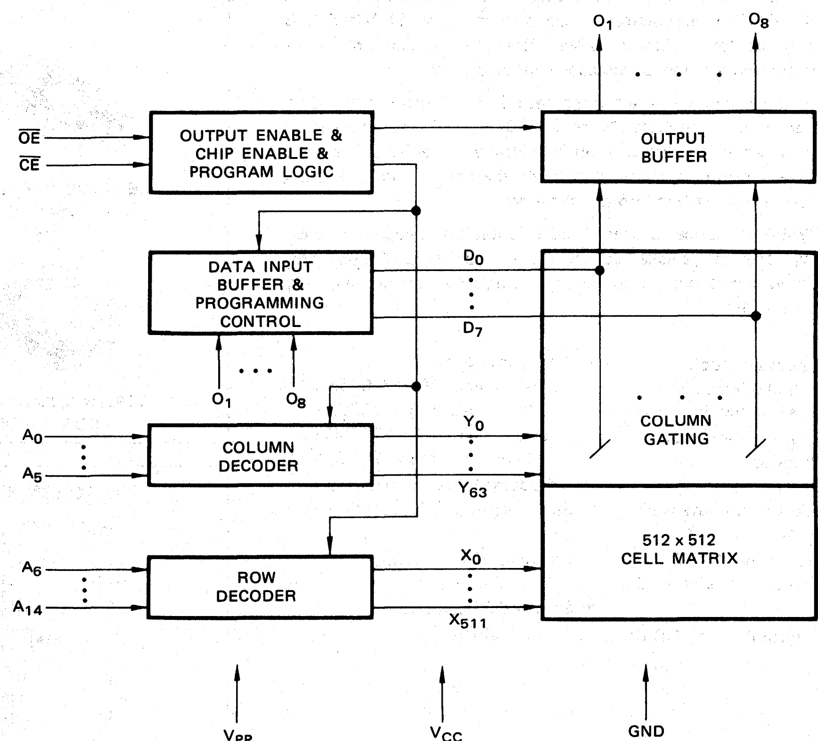
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	–25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C
All Inputs/Outputs Voltage with respect to GND	V_{IN}, V_{OUT}	-0.6to V_{CC}+0.5	V
Voltage on A_9 with respect to GND	V_{A9}	-0.6 to +13.5	V
V_{PP} Voltage with respect to GND	V_{PP}	-0.6 to +14	V
Supply Voltage with respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MBM 27C256A BLOCK DIAGRAM



9

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2 ~ 10, 21, 23, 25 ~ 27)	A_9 (24)	Data I/O (11 ~ 13, 15 ~ 19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5 V	+5 V	GND
Output Disable	A_{IN}	A_{IN}	High-Z	V_{IL}	V_{IH}	+5 V	+5 V	GND
Standby	Don't Care	Don't Care	High-Z	V_{IH}	Don't Care	+5 V	+5 V	GND
Program	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	+6 V	+12.5 V	GND
Program Verify	A_{IN}	A_{IN}	D_{OUT}	Don't Care	V_{IL}	+6 V	+12.5 V	GND
Program Inhibit	Don't Care	Don't Care	High-Z	V_{IH}	V_{IH}	+6 V	+12.5 V	GND
Electronic Signature	A_{IN}	+12 V	Code	V_{IL}	V_{IL}	+5 V	+5 V	GND

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	V
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

Note: *V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

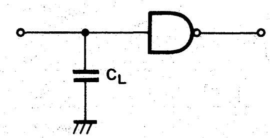
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5 V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.5 V)	I_{LO}			10	μA
V_{PP} Supply Current ($V_{PP} = V_{CC} \pm 0.6$ V)	I_{PP1}		1	100	μA
V_{CC} Standby Current ($\overline{CE} = V_{IH}$)	I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{CE} = V_{CC} \pm 0.3$ V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}=V_{IL}$)	I_{CC1}		2	30	mA
V_{CC} Operation Current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}		5	30	mA
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = –400 μA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = –100 μA)	V_{OH2}	$V_{CC}-0.7$			V

Fig. 2 – AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.45 V to 2.4 V
Input Rise and Fall Times:	$\leq$ 20 ns
Timing Measurement Reference Levels:	1.0 V and 2.0 V for inputs
	0.8 V and 2.0 V for outputs
Output Load:	1 TTL gate and C_L = 100 pF



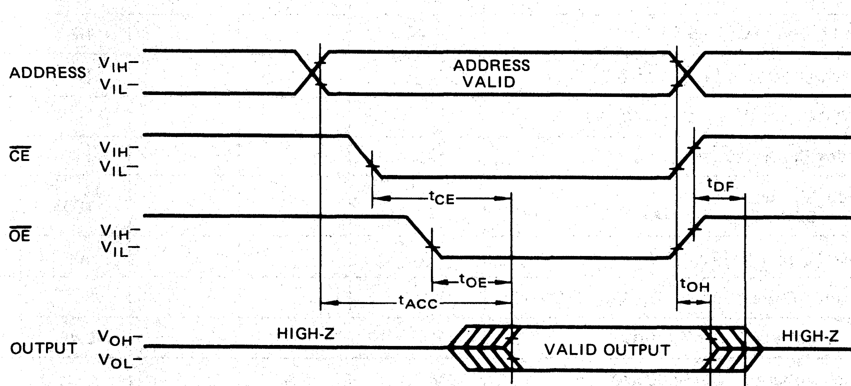
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27C256A-15		MBM 27C256A-17		MBM 27C256A-20		MBM 27C256A-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Access Time*1 ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{ACC}		150		170		200		250	ns
$\overline{CE}$ to Output Delay ($\overline{OE}$ = V_{IL})	t_{CE}		150		170		200		250	ns
$\overline{OE}$ to Output Delay*1 ($\overline{CE}$ = V_{IL})	t_{OE}		60		70		75		100	ns
Address to Output Hold	t_{OH}	0		0		0		0		ns
Output Enable High to Output Float*2	t_{DF}	0	60	0	60	0	60	0	60	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the folling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Floating is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



9

PROGRAMMING/ERASING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27C256A has all 262,144 bits in the "1", or high state. "0's" are loaded into the MBM 27C256A through the procedure of programming.

The MBM 27C256A is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{CE}$ and $\overline{OE}$ are V_{IH}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1ms programming pulse is applied to $\overline{CE}$ and after that one additional pulse which is 3 times as wide as previous pulse is applied to $\overline{CE}$ to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{CE}$ = V_{IH}.
3) Clear the programming pulse counter (X ← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1ms Typ.) to $\overline{CE}$.
6) Increment the counter (X ← X+1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X = 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G ← G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 27C256A to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM 27C256A. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 21 minutes. The MBM 27C256A should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27C256A and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27C256A, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ELECTRONIC SIGNATURE

The MBM 27C256A has electronic signature mode which is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

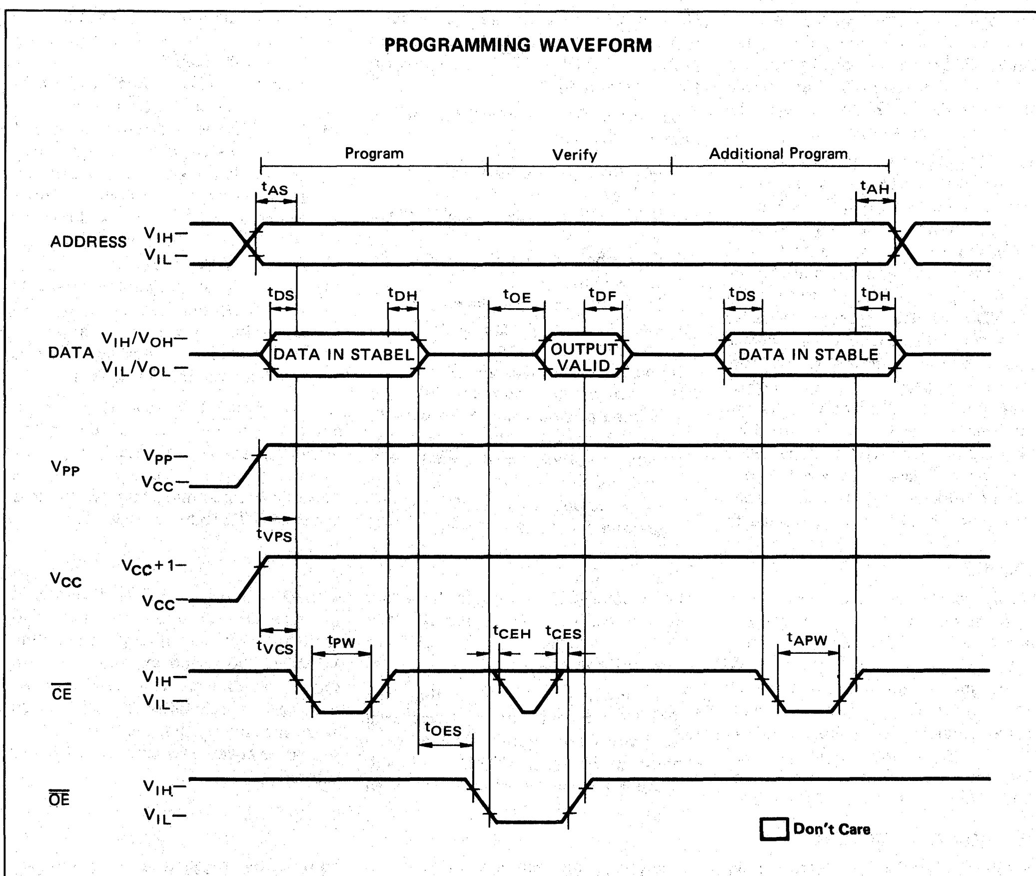
The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM 27C256A. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be hold at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	0	1	0	0	x	1	1	0	Device

Note: A_9 = 12V±0.5V
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
A_{14} = Either V_{IL} or V_{IH}

Quick Pro™ is a trademark of FUJITSU LIMITED

PROGRAMMING/ERASING INFORMATION (Cont'd)



DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}*1 = 6V±0.25V, V_{PP}*2 = 12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{IL}			10	μA
V_{PP} Supply Current ($\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{OE}$ = V_{IL})	I_{PP3}			5	mA
V_{CC} Supply Current	I_{CC}			30	mA
Input Low Level	V_{IL}	−0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VPS}	2			μs
V_{CC} Setup Time	t_{VCS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Chip Enable Hold Time	t_{CEH}	2			μs
Output Enblea to Output Valid	t_{OE}			120	ns
Output Disable to Output Float Delay	t_{DF}			105	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Programming Pulse Number	x	1		25	times
Additional Programming Pulse Width	t_{APW}	2.85		78.75	ms

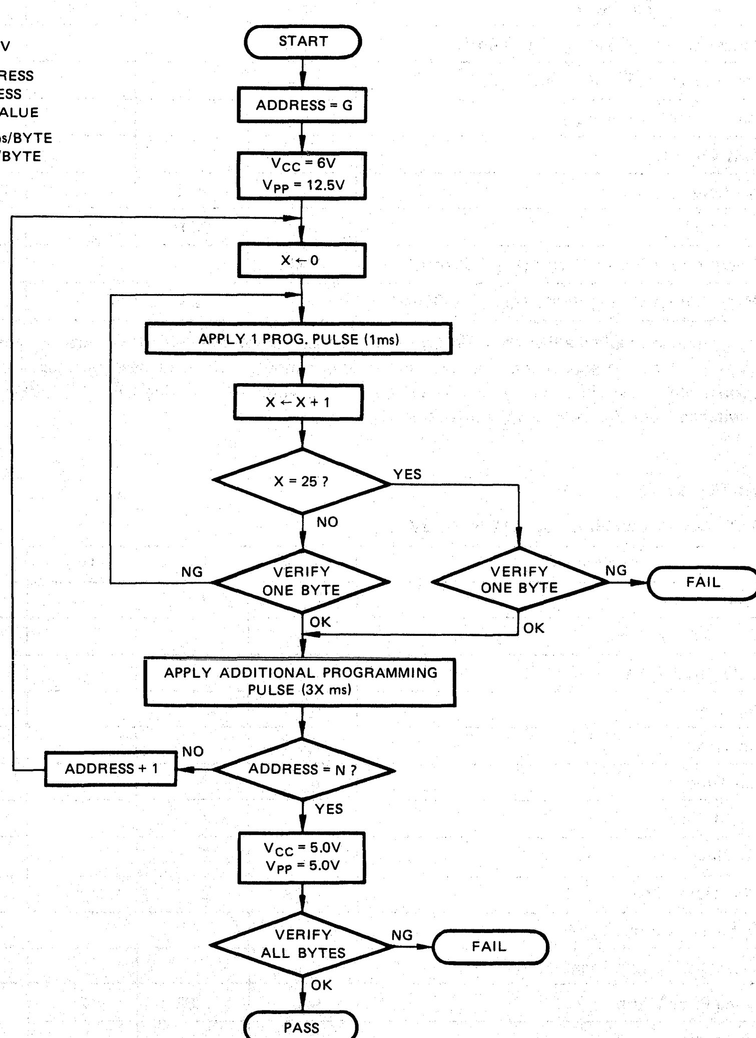
PROGRAMMING／ERASING INFORMATION (Cont'd)

PROGRAMMING FLOW CHART FOR Quick Pro™

V_{CC} = 6V ± 0.25V
V_{PP} = 12.5V ± 0.3V

G : START ADDRESS
N : STOP ADDRESS
X : COUNTER VALUE

MAXIMUM 105 ms/BYTE
MINIMUM 3.8 ms/BYTE

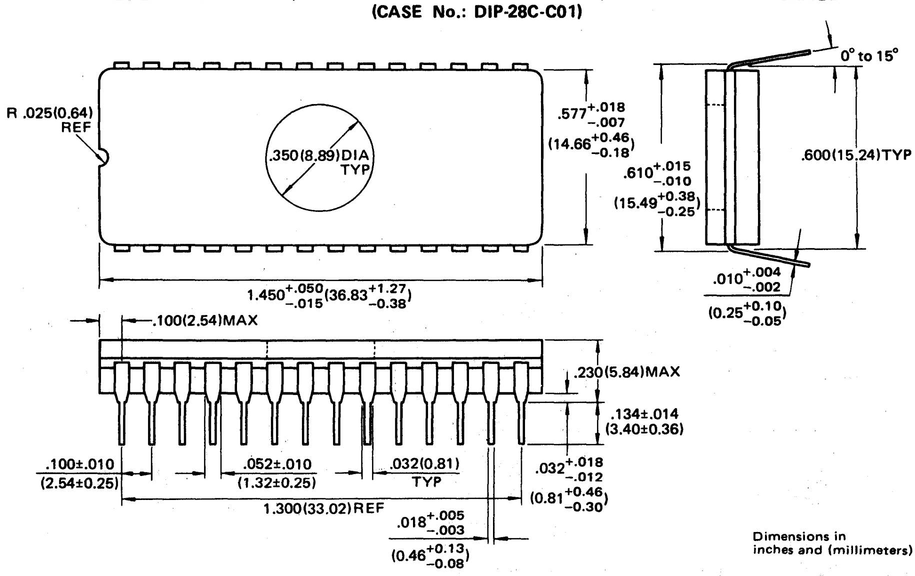


Quick Pro™ is a trademark of FUJITSU LIMITED

PACKAGE DIMENSIONS

Standard 28-pin Ceramic DIP (Suffix: -Z)

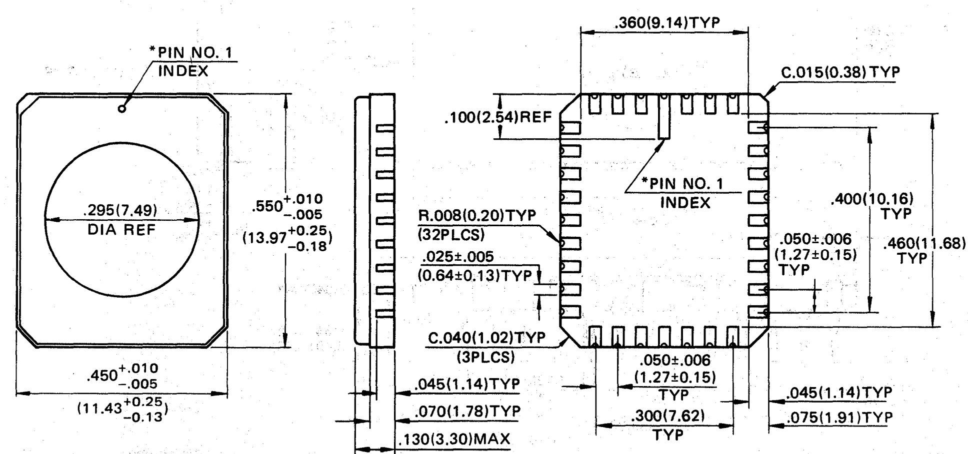
28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)



PACKAGE DIMENSIONS

Standard 32-pad Ceramic LCC (Suffix: -TV)

32-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER (CASE No.: LCC-32C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in inches and (millimeters)

FUJITSU

CMOS UV ERASABLE 262144-BIT READ ONLY MEMORY

MBM 27C256H-10
MBM 27C256H-12

June 1986
Edition 1.0

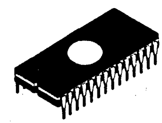
CMOS 262144 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM 27C256H is a 262,144 bits high speed CMOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

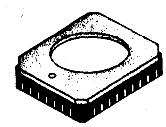
A 28-pin dual-in line package with a transparent lid and 32-pad Leadless Chip Carrier (LCC) are used to package the MBM 27C256H. The transparent lid allows the user to expose the device to ultra violet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C256H is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

PRELIMINARY



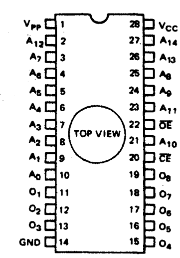
CERAMIC PACKAGE
DIP-28C-C01

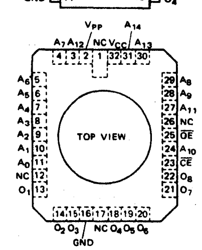


CERAMIC PACKAGE
LCC-32C-F01

- CMOS power consumption
  Standby: 550 μW max.
  Active: 330 mW max.
- 32,768 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ algorithm
- Programming voltage: 12.5V
- No clocks required (fully static operation)
- Fast access time:
  100 ns max. (MBM 27C256H-10)
  120 ns max. (MBM 27C256H-12)
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Single +5V supply, ±10% tolerance
- Standard 28-pin ceramic
  DIP: Suffix-Z
- Standard 32-pad ceramic
  LCC: Suffix-TV

PIN ASSIGNMENT





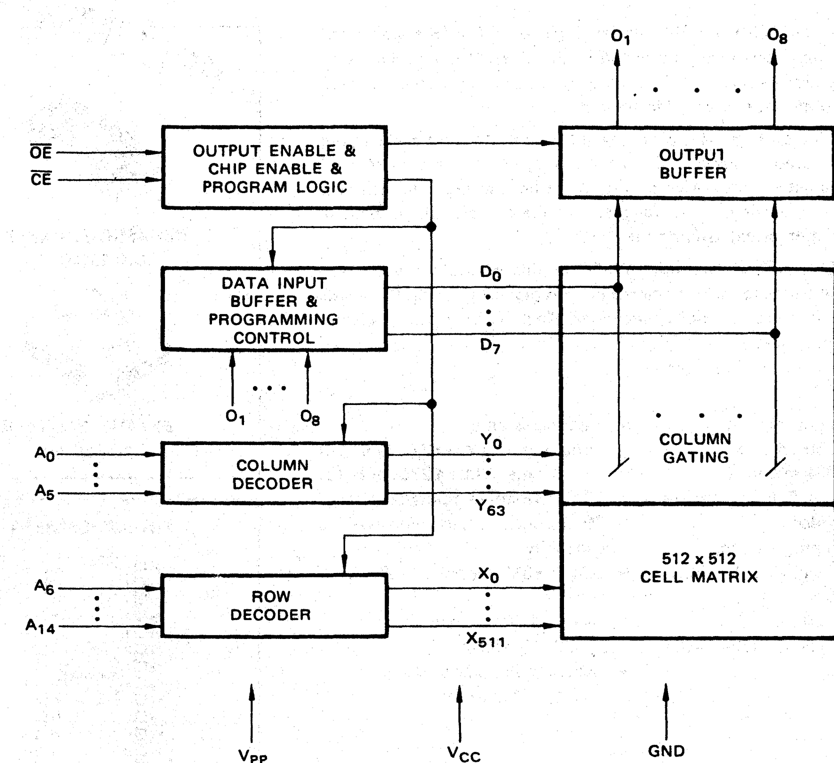
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C
All Inputs/Outputs Voltage with respect to GND	V_{IN}, V_{OUT}	-0.6 to $+V_{CC}$ + 0.6	V
Voltage on A_9 with respect to GND	V_{A9}	-0.6 to +13.5	V
V_{PP} Voltage with respect to GND	V_{PP}	-0.6 to +13.5	V
Supply Voltage with repsect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MBM 27C256H BLOCK DIAGRAM



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CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2 ~ 10, 21, 23, ~ 27)	A_9 (24)	Data I/O (11 ~ 13, 15 ~ 19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5 V	+5 V	GND
Output Disable	A_{IN}	A_{IN}	High-Z	V_{IL}	V_{IH}	+5 V	+5 V	GND
Standby	Don't Care	Don't Care	High-Z	V_{IH}	Don't Care	+5 V	+5 V	GND
Program	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	+6 V	+12.5 V	GND
Program Verify	A_{IN}	A_{IN}	D_{OUT}	Don't Care	V_{IL}	+6 V	+12.5 V	GND
Program Inhibit	Don't Care	Don't Care	High-Z	V_{IH}	V_{IH}	+6 V	+12.5 V	GND
Electronic Signature	A_{IN}	+12 V	Code	V_{IL}	V_{IL}	+5 V	+5 V	GND

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	V
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

Note: *V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

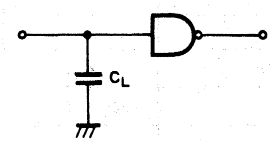
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5 V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.5 V)	I_{LO}			10	μA
V_{PP} Supply Current ($V_{PP} = V_{CC} \pm 0.6$ V)	I_{PP}		1	100	μA
V_{CC} Standby Current ($\overline{CE} = V_{IH}$)	I_{SB1}			3	mA
V_{CC} Standby Current ($\overline{CE} = V_{CC} \pm 0.3$ V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}=V_{IL}$)	I_{CC1}			30	mA
V_{CC} Operation Current (f = min., I_{OUT} = 0 mA)	I_{CC2}			60	mA
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400 μA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = −100 μA)	V_{OH2}	$V_{CC}-0.7$			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.45 V to 2.4 V
Input Rise and Fall Times:	≦5 ns
Timing Measurement Reference Levels:	0.8 V and 2.0 V for inputs 0.8 V and 2.0 V for outputs
Output Load:	1 TTL gate and C_L = 100 pF C_L = 5 pF (t_{DF})



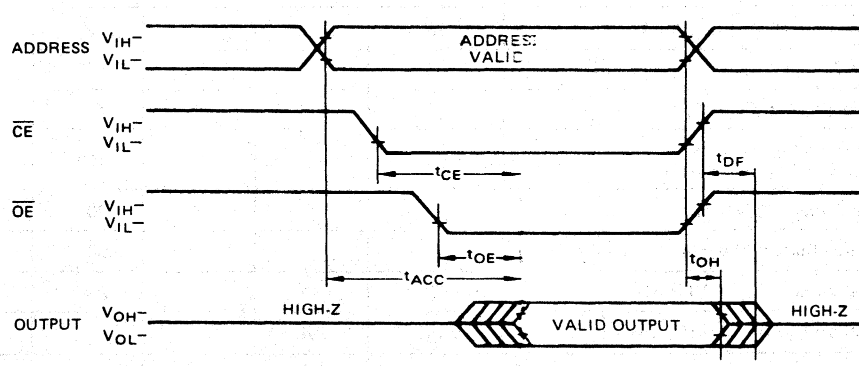
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27C256H-10			MBM 27C256H-12			Units
		Min	Typ	Max	Min	Typ	Max	
Address Access Time*1 ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{ACC}			100			120	ns
$\overline{CE}$ to Output Delay ($\overline{OE}$ = V_{IL})	t_{CE}			100			120	ns
$\overline{OE}$ to Output Delay*1 ($\overline{CE}$ = V_{IL})	t_{OE}			45			50	ns
Address to Output Hold	t_{OH}	0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		35	0		35	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Transition is measured at the point of ±500 mV from steady state voltage.

OPERATION TIMING DIAGRAM



PROGRAMMING / ERASING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27C256H has all 262,144 bits in the "1", or high state. "0's" are loaded into the MBM 27C256H through the procedure of programming.

The MBM 27C256H is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{CE}$ and $\overline{OE}$ are V_{IH}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1ms programming pulse is applied to $\overline{CE}$ and after that one additional pulse which is 3 times are wide as previous pulse is applied to $\overline{CE}$ to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{CE}$ = V_{IH}.
3) Clear the programming pulse counter ($X \leftarrow 0$).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1ms Typ.) to $\overline{CE}$.
6) Increment the counter ($X \leftarrow X+1$).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X < 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address ($G \leftarrow G+1$) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 27C256H to an ultraviolet light source. A dosage of 15 W-seconds/cm² is required to completely erase an MBM 27C256H. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm² for 15 to 21 minutes. The MBM 27C256H should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27C256H and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27C256H, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ELECTRONIC SIGNATURE

The MBM 27C256H has electronic signature mode which is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM 27C256H. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be hold at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	0	1	0	0	0	1	1	0	Device

Note: A_9 = 12V ± 0.5V
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
A_{14} = Either V_{IL} or V_{IH}

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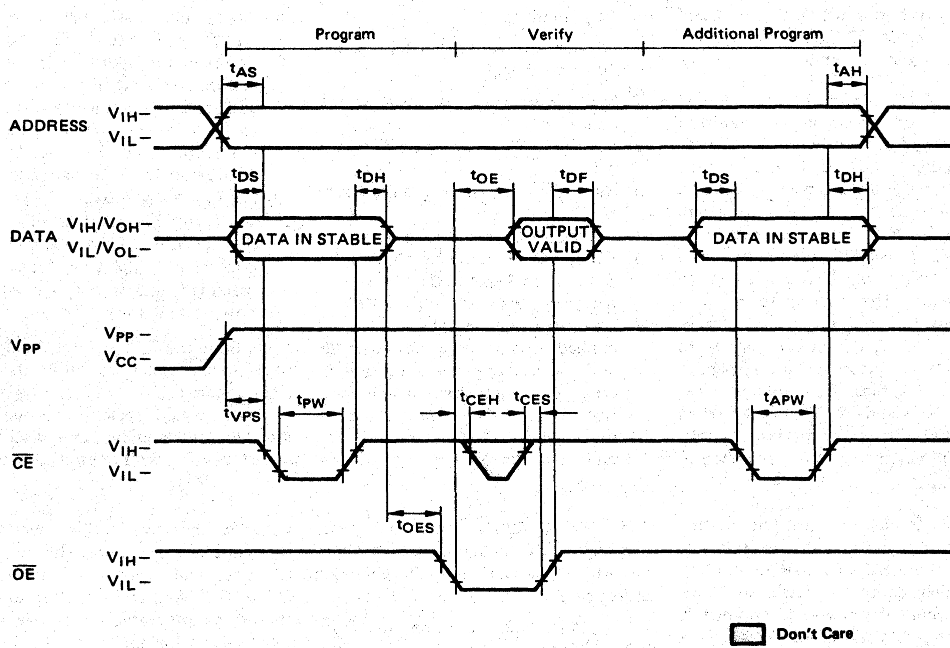
Quick Pro™ is a trademark of FUJITSU LIMITED

PROGRAMMING ⁄ ERASING INFORMATION (Cont'd)

PROGRAMMING WAVEFORM



DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}*1 = 6V±0.25V, V_{PP}*2 = 12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	$\lvert I_{IL} \rvert$			10	µA
V_{PP} Supply Current ($\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{OE}$ = V_{IL})	I_{PP3}			5	mA
V_{CC} Supply Current	I_{CC3}			50	mA
Input Low Level	V_{IL}	–0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = –400µA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 13.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

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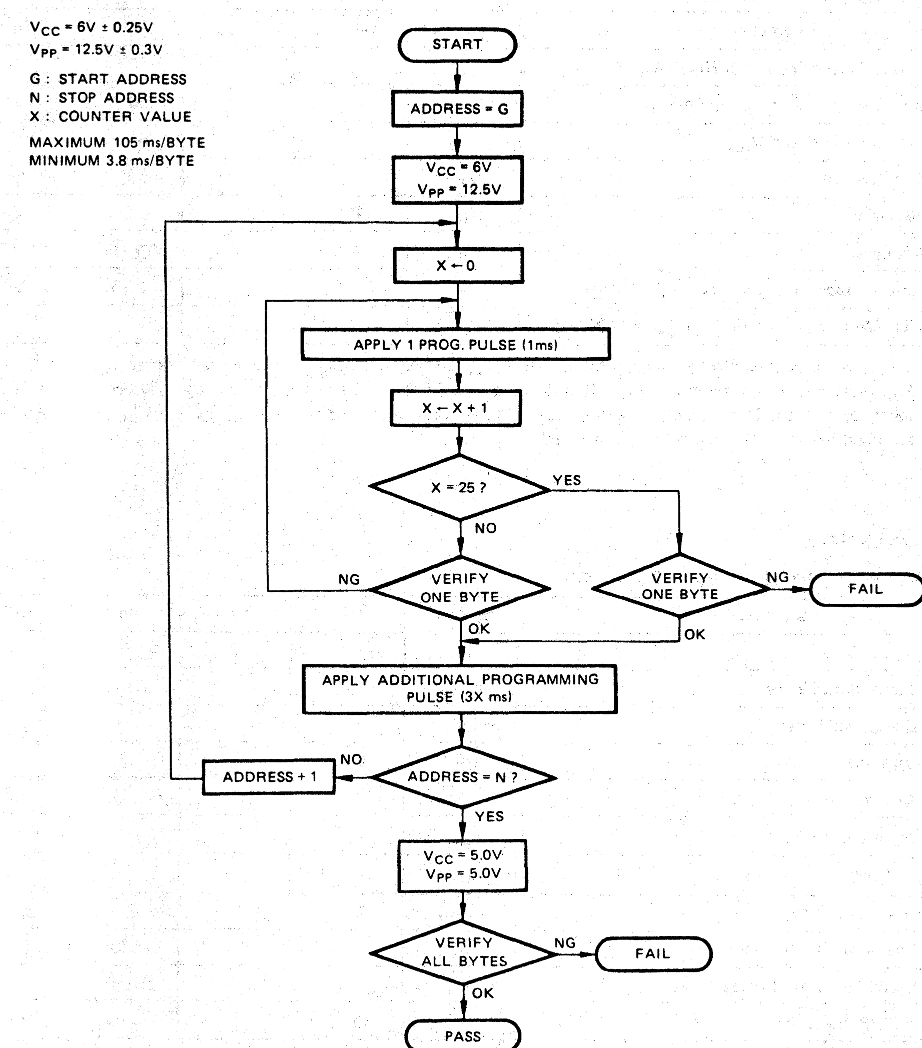
AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Data Setup Time	t_{DS}	2			µs
V_{PP} Setup Time	t_{VPS}	2			µs
Address Hold Time	t_{AH}	2			µs
Data Hold Time	t_{DH}	2			µs
Chip Enable Hold Time	t_{CEH}	2			µs
Output Enable to Output Valid	t_{OE}			120	ns
Output Disable to Output Float Delay	t_{DF}			105	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Programming Pulse Number	x	1		25	times
Additional Programming Pulse Width	t_{APW}	2.85		78.75	ms

PROGRAMMING / ERASING INFORMATION (Cont'd)

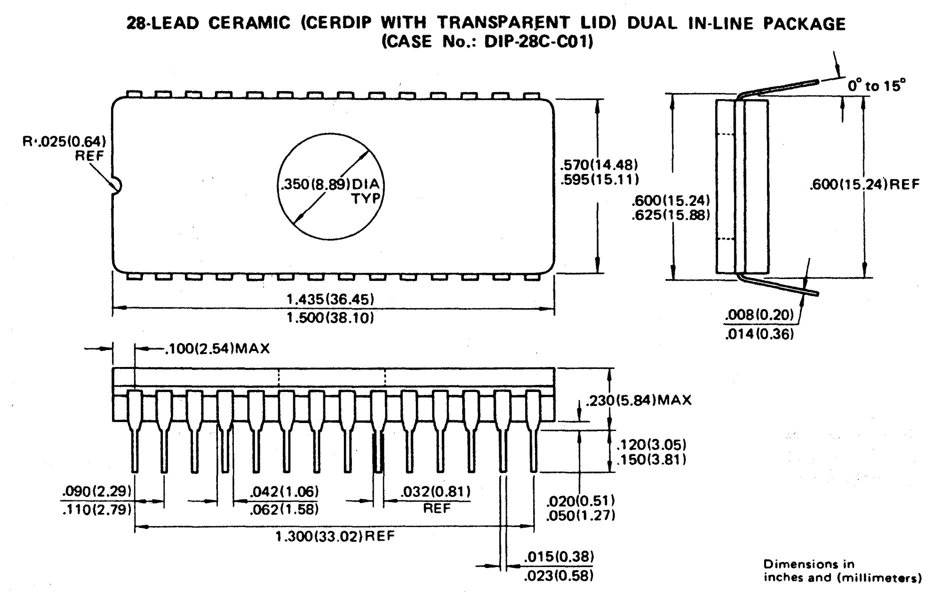
PROGRAMMING FLOW CHART FOR Quick Pro™



Quick Pro™ is a trademark of FUJITSU LIMITED

PACKAGE DIMENSIONS

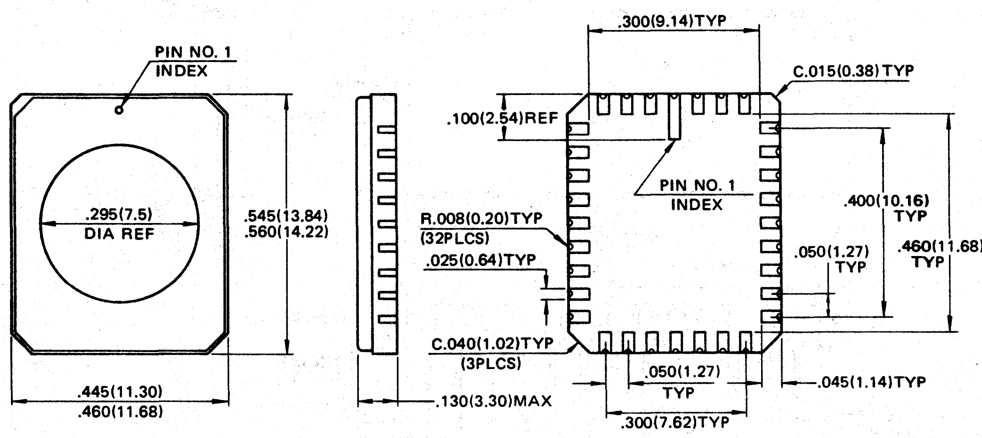
Standard 28-pin Ceramic DIP (Suffix: -Z)



PACKAGE DIMENSIONS

Standard 32-pad Ceramic LCC (Suffix: -TV)

32-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-F01)



Dimension in inches
and (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

CMOS UV ERASABLE 524288-BIT READ ONLY MEMORY

MBM27C512-15
MBM27C512-17

October 1987
Edition 1.0

CMOS 524288 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM 27C512 is a high speed 524,288 bit static CMOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

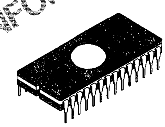
A 28-pin dual-in line package with a transparent lid and 32-Pad Leadless Chip Carrier (LCC) are used to package the MBM 27C512. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C512 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 65,536 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

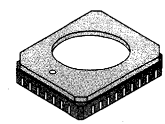
This specification is applied to "HW" version.

- CMOS power consumption
  Standby: 550μW/max.
  Active: 220mW/max.
- 65,536 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
- Fast access time:
  150ns max. (MBM27C512-15)
  170ns max. (MBM27C512-17)
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Single +5V supply, ±10% tolerance
- Standard 28-pin Ceramic DIP: (Suffix: -Z)
- Standard 32-pad Ceramic LCC: (Suffix: -TV)

ADVANCE INFORMATION

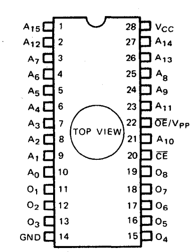


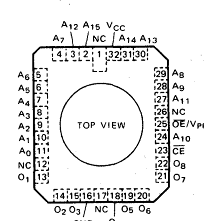
CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-F01

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	−25 to +85	°C
Storage Temperature	T_{STG}	−65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	−0.6 to V_{CC}+0.6	V
Voltage on A_9 with Respect to GND	V_{A9}	−0.6 to 13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	−0.6 to +14	V
Supply Voltage with Respect to GND	V_{CC}	−0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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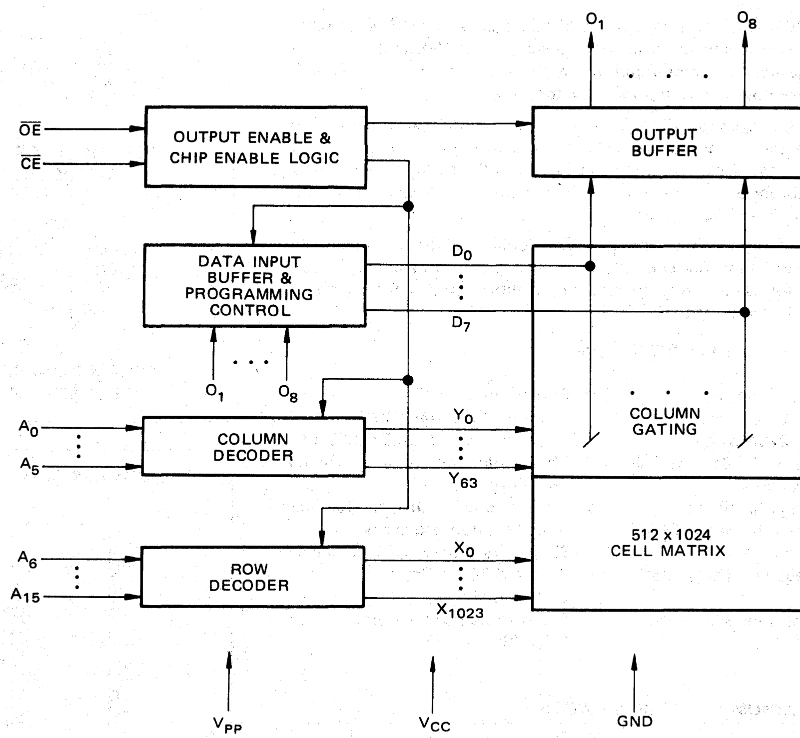
Fig. 1 — MBM 27C512 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0 V, except $\overline{OE}/V_{PP}$)	C_{IN1}	—	4	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance (V_{IN} = 0 V)	C_{IN2}	—	—	20	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}	—	8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (1~10, 21, 23~27)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	5V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	5V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	5V	GND
Program	A_{IN}	D_{IN}	V_{IL}	12.5V	6V	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	6V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	12.5V	6V	GND

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

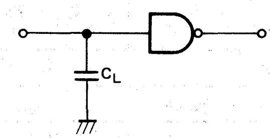
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Input Load Current (V_{IN} = 5.5 V)		$\lvert I_{LI}\rvert$			10	μA
Output Leakage Current (V_{OUT} = 5.5 V)		$\lvert I_{LO}\rvert$			10	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})		I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{CE}$ = V_{CC} ±0.3 V, I_{OUT} = 0 mA)		I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA)	150 ns	I_{CC1}		4	40	mA
	170 ns				30	
V_{CC} Operation Current (f = 4 MHz, I_{OUT} = 0 mA)		I_{CC2}		10	40	mA
Output Low Voltage (I_{OL} = 2.1 mA)		V_{OL}			0.45	V
Output High Voltage (I_{OH} = -400 μA)		V_{OH1}	2.4			V
Output High Voltage (I_{OH} = -100 μA)		V_{OH2}	V_{CC} -0.7			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



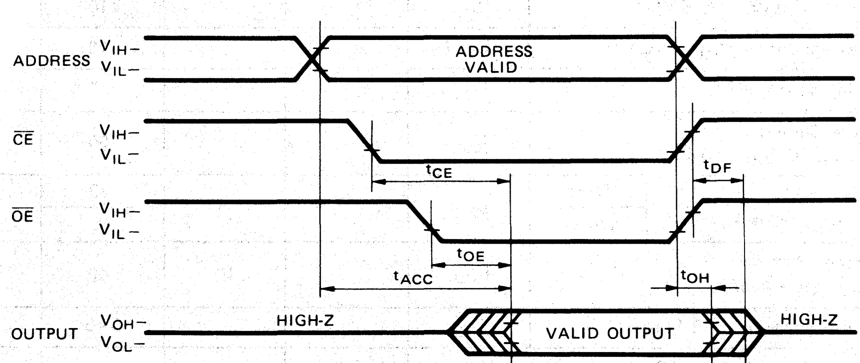
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27C512-15			MBM 27C512-17			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time*1	t_{ACC}			150			170	ns
$\overline{CE}$ to Output Delay	t_{CE}			150			170	ns
$\overline{OE}$ to Output Delay*1	t_{OE}			60			70	ns
Address to Output Hold	t_{OH}	0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



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PROGRAMMING/ERASING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27C512 has all 524,288 bits in the "1", or high state. "0's" are loaded into the MBM 27C512 through the procedure of programming.

The MBM 27C512 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{CE}$ is V_{IH}. A $0.1\mu F$ capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 ms programming pulse is applied to $\overline{CE}$ and after that one additional pulse which is 3 times as wide as previous pulse is applied to $\overline{CE}$ to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{CE}$ = V_{IH}.
3) Clear the programming pulse counter ($X \leftarrow 0$).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1ms Typ.) to $\overline{CE}$.
6) Increment the counter ($X \leftarrow X+1$).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If $X < 25$ and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address ($G \leftarrow G+1$) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V and V_{CC} = 6V) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 27C512 to an ultraviolet light source. A dosage of 15 W-seconds/cm² is required to completely erase an MBM 27C512. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm² for 15 to 21 minutes. The MBM 27C512 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27C512 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27C512, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ELECTRONIC SIGNATURE

The MBM 27C512 has electronic signature mode which is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

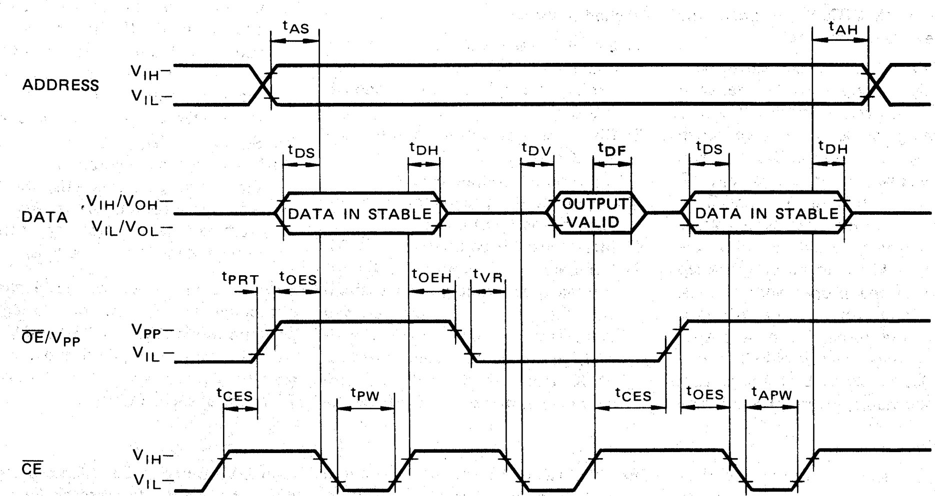
The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM 27C512. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be hold at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	1	1	0	0	0	1	1	1	Device

Note: A_9 = 12V ± 0.5V
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
A_{14} = A_{15} = Either V_{IL} or V_{IH}

PROGRAMMING/ERASING INFORMATION (Cont'd)

PROGRAMMING WAVEFORM



DC CHARACTERISTICS
(T_A = 25±5°C, V_{CC}^{*1} = 6V±0.25V, V_{PP}^{*2} = 12.5V±0.3V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Leakage Current (V_{IN} = 5.25 V/0.45 V)	$\lvert I_{LI} \rvert$			10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = V_{IL})	I_{PP}			50	mA
V_{CC} Supply Current	I_{CC}			30	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400 µA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from 5 to 12.5 volts or vice-versa.

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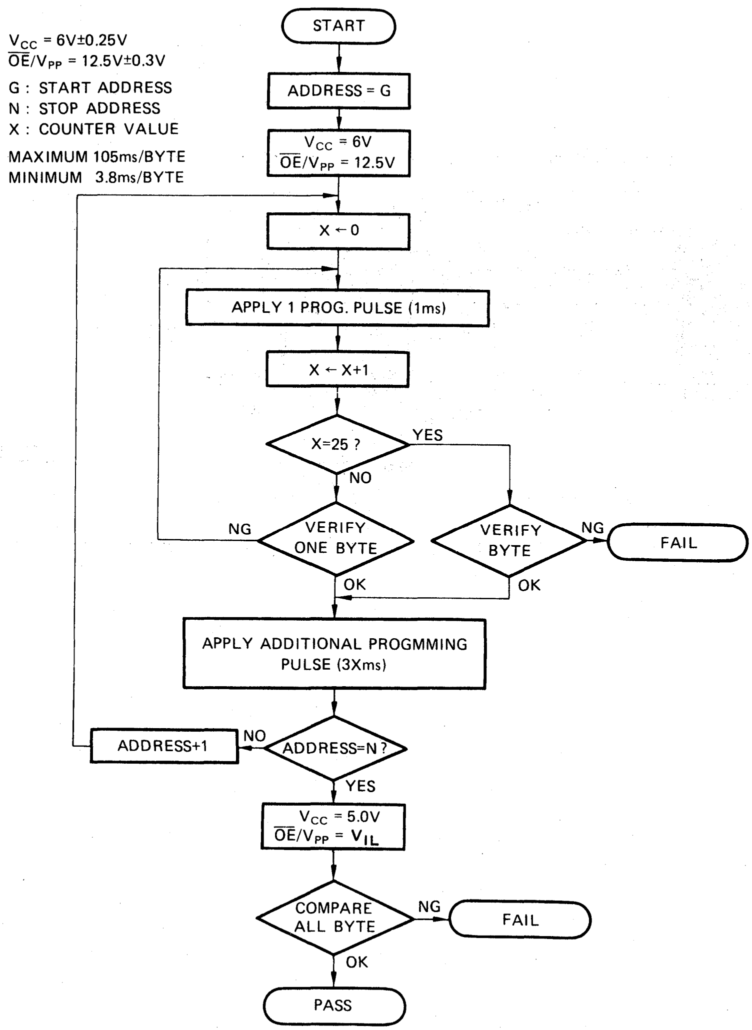
PROGRAMMING/ERASING INFORMATION (Cont'd)

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{CC} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Output Enable Hold Time	t_{OEH}	2			μs
V_{PP} Recovery Time	t_{VR}	2			μs
Chip Enable to Data Valid	t_{DV}			1	μs
Output Disable to Output Float Delay	t_{DF}	0		130	ns
V_{PP} Program Pulse Rise Time	t_{PRT}	50			ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Additional Programming Pulse Width	t_{APW}	2.85		78.75	ms

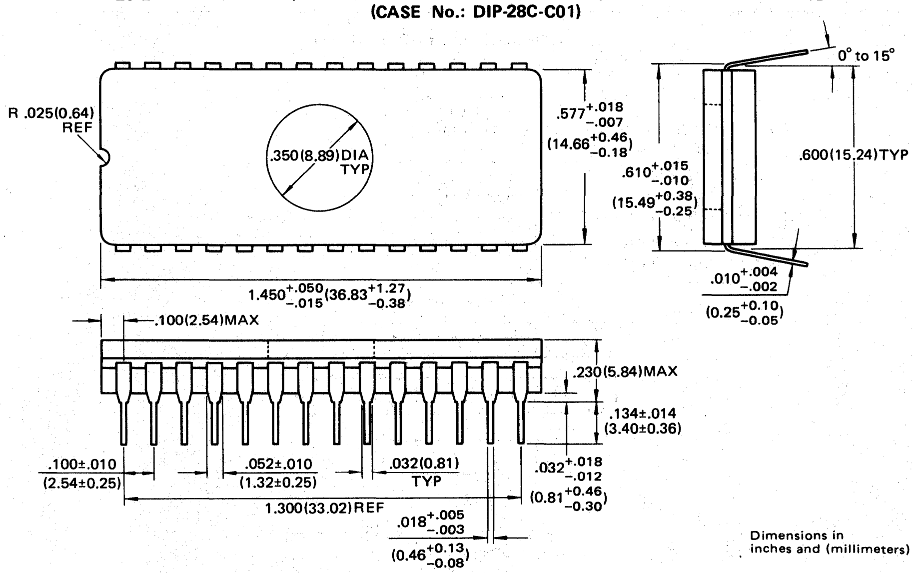
PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

Standard 28-pin Ceramic DIP (Suffix: -Z)

28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)



Dimensions in inches and (millimeters)

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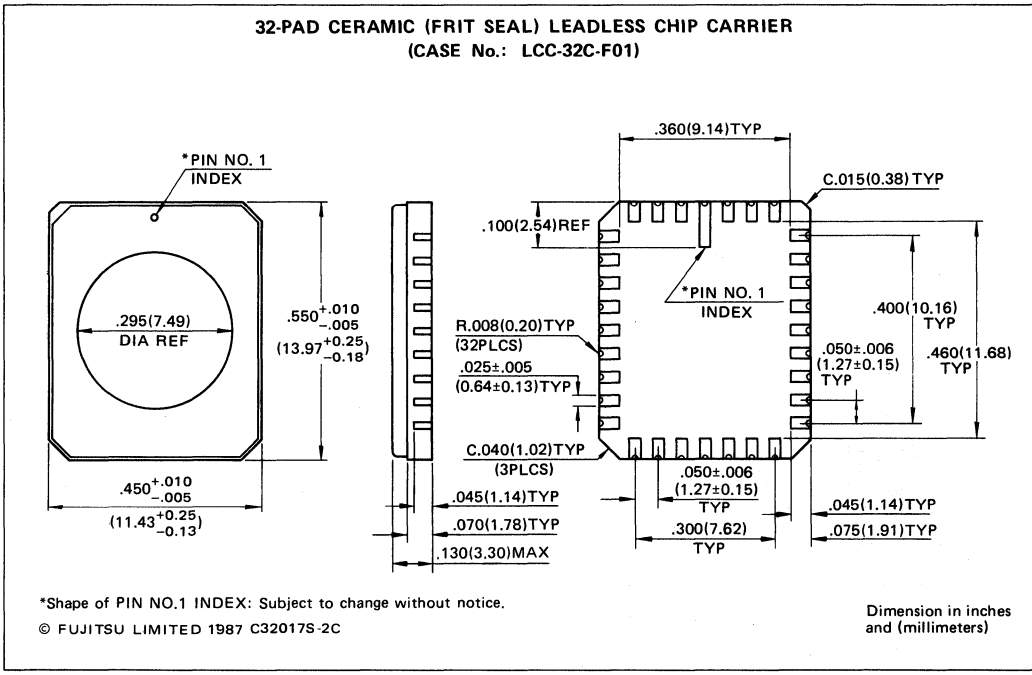
PACKAGE DIMENSIONS

Standard 32-pad Ceramic LCC (Suffix: -TV)



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FUJITSU

CMOS UV ERASABLE 524288-BIT READ ONLY MEMORY

MBM 27C512-20
MBM 27C512-25
MBM 27C512-30

September 1986
Edition 2.0

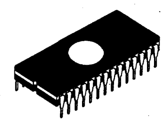
CMOS 524288 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM 27C512 is a high speed 524,288 bit static CMOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

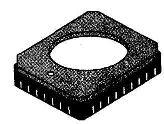
A 28-pin dual-in line package with a transparent lid and 32-Pad Leadless Chip Carrier (LCC) are used to package the MBM 27C512. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C512 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 65,536 words by 8 bits for use in microprocessor applications. Single + 5V operation greatly facilitates its use in systems.

- CMOS power consumption
  Standby: 550μW/ max.
  Active : 40mW/MHz
- 65,536 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
- Fast access time:
  200ns max. (MBM 27C512-20)
  250ns max. (MBM 27C512-25)
  300ns max. (MBM 27C512-30)
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Single +5V supply, ±10% tolerance
- Standard 28-pin Ceramic DIP : (Suffix: -Z)
- Standard 32-pad Ceramic LCC : (Suffix: -TV)

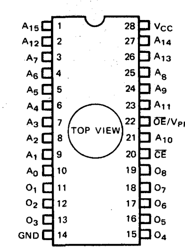


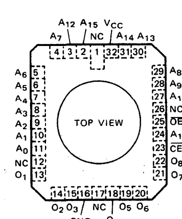
CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-F01

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	-0.6 to V_{CC}+0.6	V
Voltage on A_9 with Respect to GND	V_{A9}	-0.6 to 13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +14	V
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Quick Pro™ is a trademark of FUJITSU LIMITED

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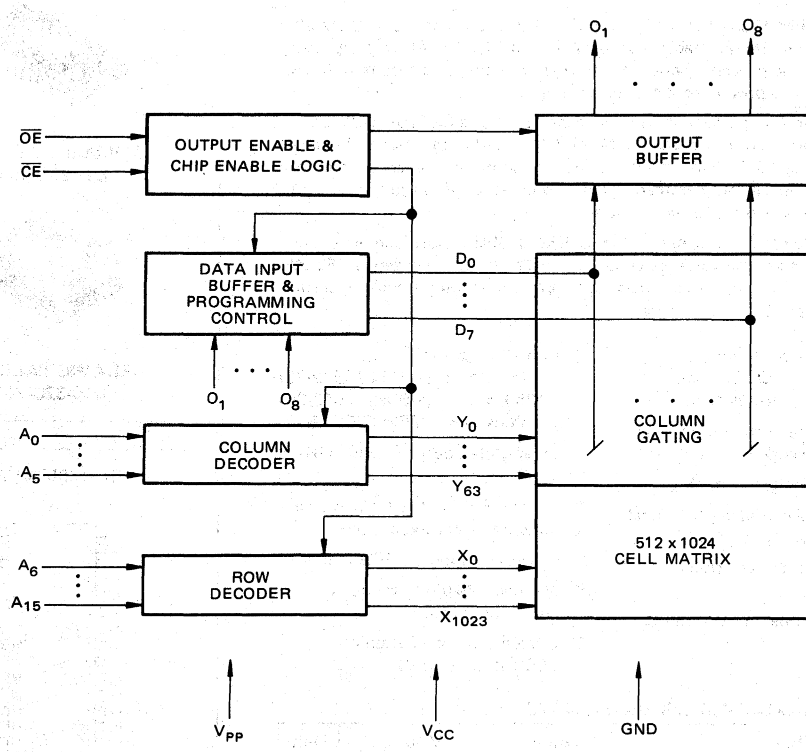
Fig. 1 — MBM 27C512 BLOCK DIAGRAM



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CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0 V, except $\overline{OE}/V_{PP}$)	C_{IN1}	–	4	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance (V_{IN} = 0 V)	C_{IN2}	–	–	20	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}	–	8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (1~10, 21, 23~27)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	5V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	5V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	5V	GND
Program	A_{IN}	D_{IN}	V_{IL}	12.5V	6V	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	6V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	12.5V	6V	GND

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

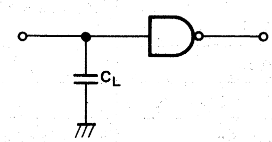
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Load Current (V_{IN} = 5.5 V)	$\|I_{LI}\|$			10	μA
Output Leakage Current (V_{OUT} = 5.5 V)	$\|I_{LO}\|$			10	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{CE}$ = V_{CC} ±0.3 V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA)	I_{CC1}		4	30	mA
V_{CC} Operation Current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}		10	30	mA
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400 μA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = −100 μA)	V_{OH2}	V_{CC} −0.7			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤ 20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



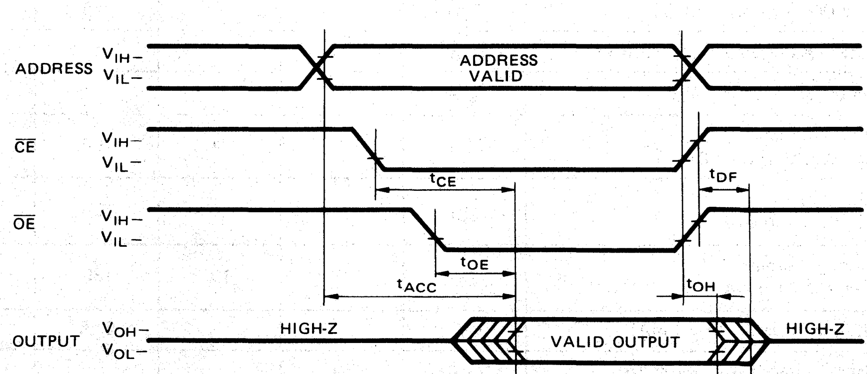
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27C512-20			MBM 27C512-25			MBM 27C512-30			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time*1	t_{ACC}			200			250			300	ns
$\overline{CE}$ to Output Delay	t_{CE}			200			250			300	ns
$\overline{OE}$ to Output Delay*1	t_{OE}			70			100			120	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		105	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



PROGRAMMING/ERASING INFORMATION

PROGRAMMING

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Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{CE}$ = V_{IH}.
3) Clear the programming pulse counter (X ← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1ms Typ.) to $\overline{CE}$.
6) Increment the counter (X ← X+1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X < 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G ← G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V and V_{CC} = 6V) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 27C512 to an ultraviolet light source. A dosage of 15 W-seconds/cm² is required to completely erase an MBM 27C512. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm² for 15 to 21 minutes. The MBM 27C512 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

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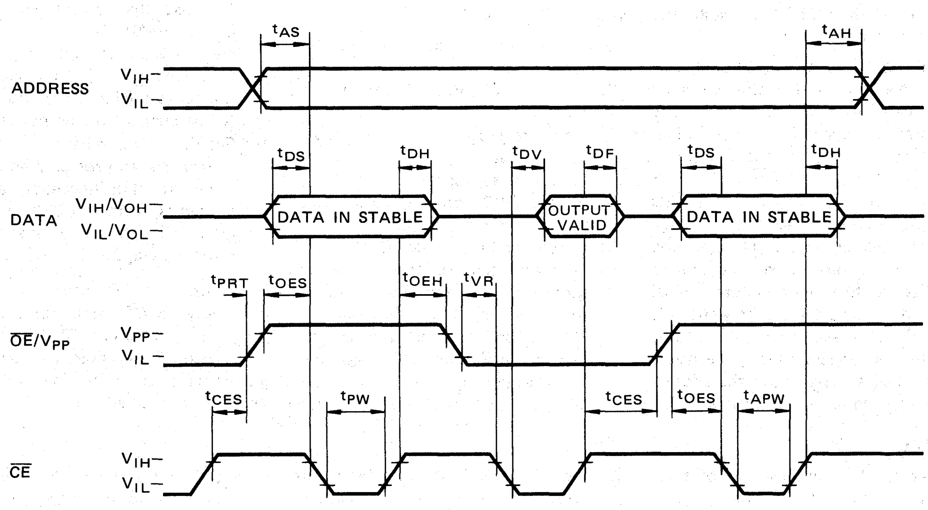
The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM 27C512. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be hold at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	1	1	0	0	0	1	1	1	Device

Note: A_9 = 12V ± 0.5V
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
A_{14} = A_{15} = Either V_{IL} or V_{IH}

PROGRAMMING/ERASING INFORMATION (Cont'd)

PROGRAMMING WAVEFORM



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DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}^{*1} = 5V±5%, V_{PP}^{*2} = 12.5V±0.3V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Leakage Current (V_{IN} = 5.25 V/0.45 V)	$\lvert I_{LI} \rvert$			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = V_{IL})	I_{PP}			50	mA
V_{CC} Supply Current	I_{CC}			30	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400 μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from 5 to 12.5 volts or vice-versa.

9

PROGRAMMING/ERASING INFORMATION (Cont'd)

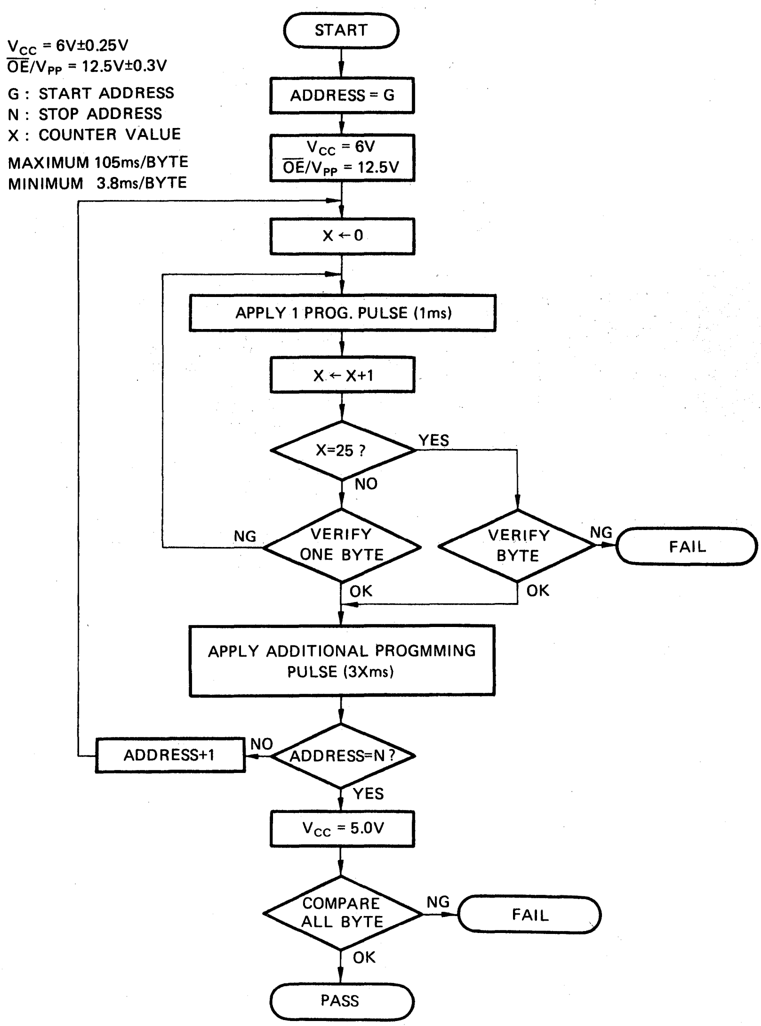
AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{CC} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Output Enable Hold Time	t_{OEH}	2			μs
V_{PP} Recovery Time	t_{VR}	2			μs
Chip Enable to Data Valid	t_{DV}			1	μs
Output Disable to Output Float Delay	t_{DF}	0		130	ns
V_{PP} Program Pulse Rise Time	t_{PRT}	50			ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Additional Programming Pulse Width	t_{APW}	2.85	3	78.75	ms

9

PROGRAMMING FLOW CHART



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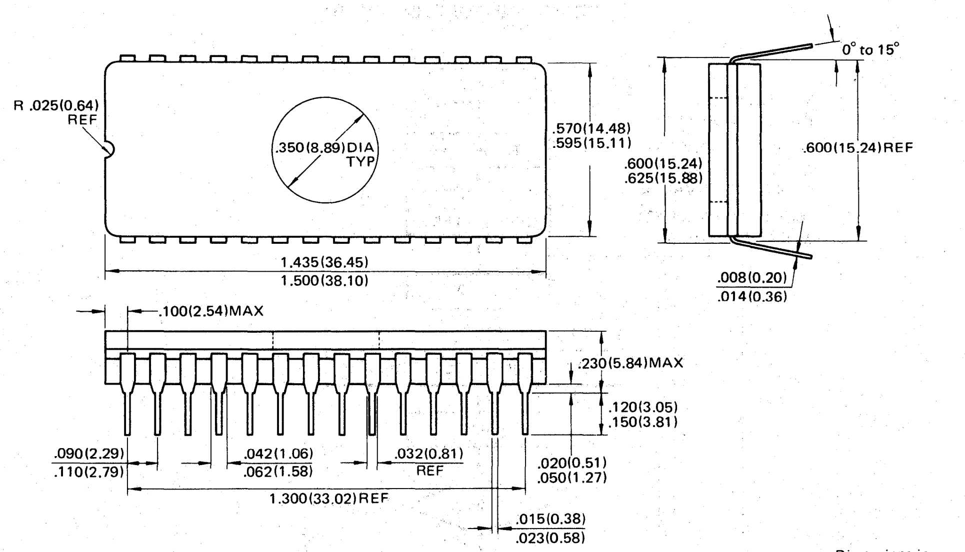
PACKAGE DIMENSIONS

Standard 28-pin Ceramic DIP (Suffix: -Z)

28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE (CASE No.: DIP-28C-C01)

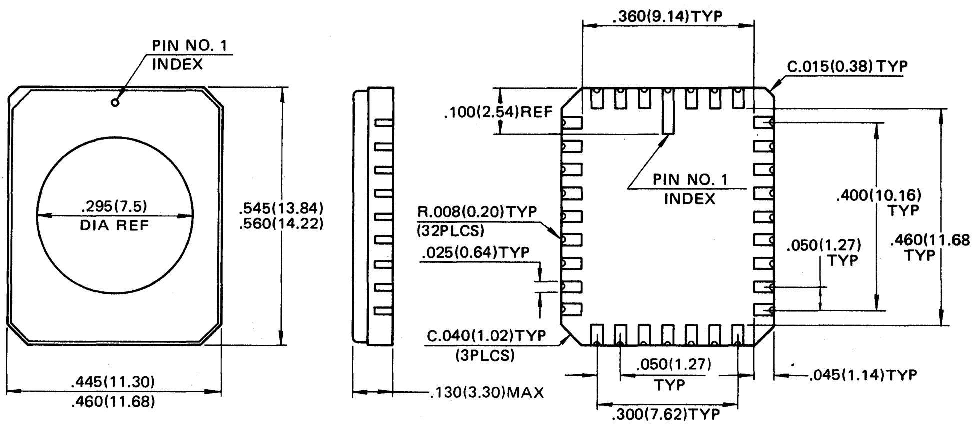


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

Standard 32-pad Ceramic LCC (Suffix: -TV)

32-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-F01)



Dimension in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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FUJITSU

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

MBM27C1000-15
MBM27C1000-20
MBM27C1000-25

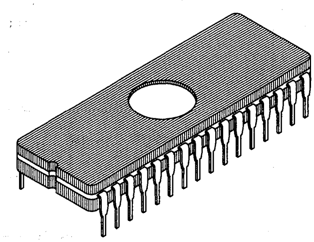
April 1988
Edition 2.0

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

The Fujitsu MBM27C1000 EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable. The device contains 1,048,576 programmable or reprogrammable bits organized in a 131,072-byte/8-bit format. The MBM27C1000 is housed in a 32-pin DIP and 36-pad LCC with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15-to-21 minutes. A new bit pattern can then be written into memory.

The MBM27C1000 EPROM is fabricated using CMOS double poly-silicon gate technology with stacked single-transistor gate cells. The MBM27C1000 is an excellent choice for system development work and in other applications where program changes are frequently necessary. Once programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

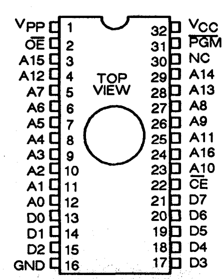
- 131,072-byte/8-bit organization with on-chip decoding
- Single-byte or four-byte programming capability with Quick Pro™ algorithm
- Static operation (no clocks required)
- Interchangeable with 1M mask ROM
- Fast access time:
  MBM27C1000-15 = 150 ns (max)
  MBM27C1000-20 = 200 ns (max)
  MBM27C1000-25 = 250 nx (max)
- Easy and simple memory expansion via @pin
- Three-state output for wired-OR capability
- TTL-compatible inputs/outputs
- Single =5V (±10%) power supply with low current drain:
  Active operation = 30 mA (max) for 200ns/250ns
  40mA (max) for 150ns
  Standby operation = 0.1 mA (max)
- Programming voltage: +12.5V
- 32-pin CERDIP



CERAMIC PACKAGE
DIP-32C-C01

LCC-36C-F01 See Page 11

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with respect to ground	V_{CC}	-0.6 to + 7.0	V
Programming Voltage with respect to ground	V_{PP}	-0.6 to + 14.0	V
Input/Output Voltage (except for A_9 with respect to ground)	$V_{IN\ 1}$	-0.6 to V_{CC} + 0.3	V
Programming Voltage with respect to ground	$V_{IN\ 2}$	-0.6 to + 13.5	V
Temperature under Bias	T_{BIAS}	-25 to + 85	°C
Storage Temperature Range	T_{STG}	-65 to + 125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Quick Pro™ is a trademark of FUJITSU LIMITED

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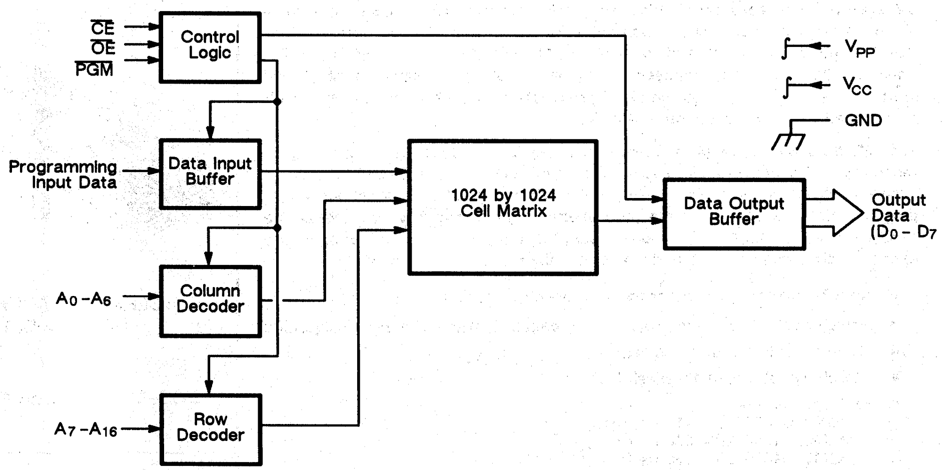
Fig. 1 — BLOCK DIAGRAM



CAPACITANCE (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}			12	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			12	pF

PIN DESCRIPTION

Symbol	Pin No. *	Function
V_{PP}	1	+12.5V programming voltage.
$\overline{OE}$	2	Output enable. When $\overline{OE}$ and $\overline{CE}$ are active low and the $\overline{PGM}$ strobe is active High; all output lines (D_0- D_7)are enabled.
A_0 - A_{16}	3-12, 23-29	Address lines.
O_0 - O_7	13-15, 17-21	Three-state output data lines.
GND	16	Circuit ground.
$\overline{CE}$	22	When active Low, the device is enabled for data read.
NC	30	No connection.
$\overline{PGM}$	31	When active Low, programming data from the input buffer is written into a specified address of memory.
V_{CC}	32	+5V power supply

*This numbers are applied to DIP package.

FUNCTIONS AND PIN CONNECTIONS

OPERATING MODE	A_0- A_8	A_9	A_{10} - A_{16}	Data	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}	GND
Standby	X	X	X	HI-Z	V_{IH}	X	X	5V	5V	0V
Read	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
Output Disable	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IL}	V_{IH} X	X V_{IL}	5V	5V	0V
Electronic Signature	Note 1	12V	X	CODE	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
Single Byte Program	A_{IN}	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	6V	12.5V	0V
Single Byte Verify	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
Single Byte Program Inhibit	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IL}	V_{IH}	V_{IH}	6V	12.5V	0V
Four Byte Data Input	Note 2	A_{IN}	A_{IN}	D_{IN}	V_{IH}	V_{IH}	V_{IH}	6V	12.5V	0V
Four Byte Program	X	A_{IN}	A_{IN}	HI-Z	V_{IH}	V_{IL}	V_{IL}	6V	12.5V	0V
Four Byte Verify	Note 2	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
Four Byte Program Inhibit	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IH}	V_{IL}	V_{IH}	6V	12.5V	0V

Legend:
X = Don't care

Notes:
1. A_0 is toggling address. A_1 is V_{IL} .
2. A_0 and A_1 can be either V_{IL} or V_{IH}

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RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{PP}	V_{CC} -0.6	V_{CC}	V_{CC} +0.6	V
Input High Level	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Level	V_{IL}	-0.1		0.8	V
Supply Voltage	GND		0		V
Operating Temperature	T_A	0		70	°C

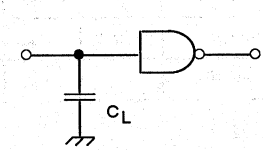
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	I_{LI}	$V_{IN} = V_{CC} = 5.5V$			10	μA
Output Leakage Current	I_{LO}	$V_{IN} = V_{CC} = 5.5V$			10	μA
V_{CC} Standby Current	I_{SB1}	$\overline{CE}=V_{IH}$			1	mA
V_{CC} Standby Current	I_{SB2}	$\overline{CE}=V_{CC} \pm 0.3V$		1	100	μA
V_{CC} Active Current	I_{CC1}	$\overline{CE}=V_{IL}$, I_{OUT} =0mA			30	mA
V_{CC} Operation Current 150ns	I_{CC2}	$\overline{CE}=V_{IL}$: f=min, I_{OUT} =0mA			40	mA
V_{CC} Operation Current 200ns/250ns	I_{CC2}	$\overline{CE}=V_{IL}$: f=min, I_{OUT} =0mA			30	mA
V_{PP} Supply Current	I_{PP}	$V_{PP} = V_{CC} \pm 0.6V$		1	100	μA
Output Low Level	V_{OL}	I_{OL} =2.1mA			0.45	V
Output High Level	V_{OH1}	I_{OH} = -400 μA	2.4			V
Output High Level	V_{OH2}	I_{OH} = -100 μA	V_{CC} -0.7			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input pulse levels:	0.45V to 2.4V (0.3V to 2.8V programming)
Input Rise/Fall Times:	≤20ns
Input Reference Levels:	0.8V to 2.0V (0.6V to 2.4V programming)
Output Reference Levels:	0.8V to 2.0V
Output Load:	1 TTL gate and C_L =100pF



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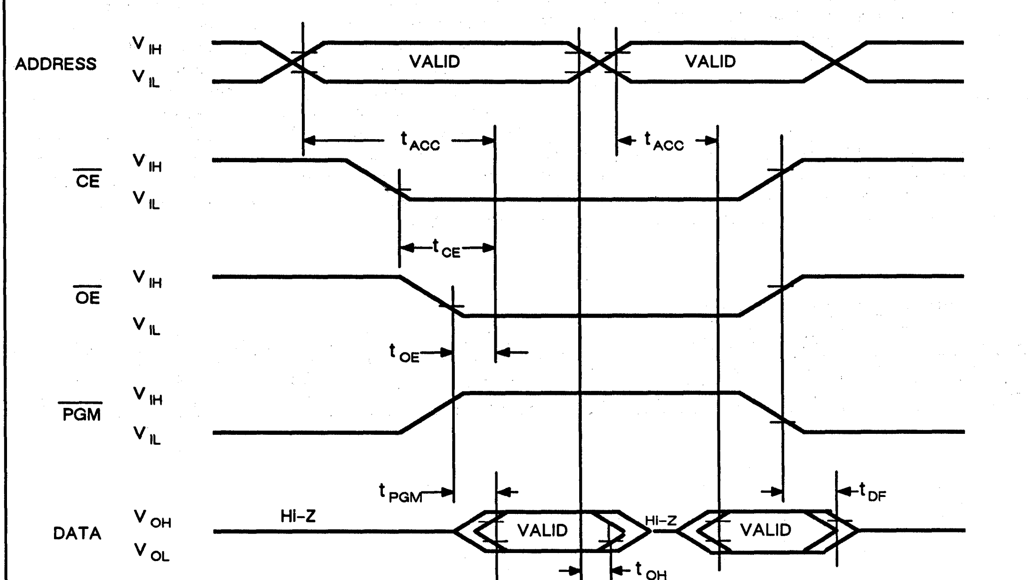
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C1000-15 Values		MBM27C1000-20 Values		MBM27C1000-25 Values		Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_{ACC}		150		200		250	ns
$\overline{CE}$ to Output Delay Time	t_{CE}		150		200		250	ns
$\overline{OE}$ to Output Delay Time	t_{OE}		70		70		100	ns
$\overline{PGM}$ to Output Delay Time	t_{PGM}		70		70		100	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float Delay (Note)	t_{DF}		60		60		60	ns
Address to Output Hold Time	t_{OH}	0		0		0		ns

NOTE: Output Float is defined as the point where data is no longer driven.

READ WAVEFORM



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PROGRAMMING / ERASING INFORMATION

PROGRAMMING

Single-Byte Programming. When +12.5V(±0.3) volts is applied to V_{PP}, +6(±0.25) volts is applied to V_{CC}, $\overline{CE}$ and $\overline{PGM}$ = V_{IH}, and $\overline{OE}$= V_{IH}, the programming mode is initiated. Next, the proper address is input and the data pattern is applied to the input buffer (Figure 1). When both address and data are stable, a 0.5-millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of one byte. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Four-Byte Programming. When compared to single-byte programming, the four-byte programming method reduces the programming time by about 75% one quarter. Voltages applied to VPP and VCC are the same as those for single-byte programming; however, some logic levels differ--refer to "Four Byte Programming" in the Truth Table. In conjunction with the $\overline{OE}$ pin, address pins A0 and A1 are used to latch four bytes of data. When both address and data are stable, a 0.5 millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write,) should be applied to complete the programming of four bytes. Refer to the PROGRAMMING FLOWCHART for step-by-step programming procedures.

Caution

The width of one programming pulse must not exceed 40-millisecond; thus, a continuous TTL low-level voltage should not be applied to the $\overline{PGM}$ pin. Also, a 0.1-microfarad capacitor must be connected between V_{PP} and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

Electronic Signature/Programming Algorithm. When the MBM27C1000 is shipped from the factory, all memory cells (1,048,576 bits) are set to the High state (logic 1). During the programming procedure, affected bit cells are set to the Low (logic 0) state.

The MBM27C1000 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. Manufacturer and device codes are electronically stored in each device; these codes can be read at the output port (D0-D7) for the purpose of matching the device with the Quick Pro™ algorithm. The Electronic Signature Code List is shown preceding the ELECTRICAL CHARACTERISTICS.

ERASING

In order to clear all memory cells of programmed contents, the MBM27C1000 must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 15Wsec/cm^2 is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 2537 Angstroms and with an intensity of 12mW/cm^2. Remove all filters from the lamp and clean the transparent lid of the MBM27C1000 with a non-abrasive cleaner. Hold the MBM27C1000 approximately one inch from the light source for 15-to-21 minutes. (Note. The MBM27C1000 and other similar devices can be erased by light sources with longer wavelengths: however, the erasing time is much greater. Nonetheless, exposure to fluorescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

ELECTRONIC SIGNATURE CODE LIST

Definition	AO	A1 TO A6	A9	A7,A8, A10 to A16	D0	D1	D2	D3	D4	D5	D6	D7	HEX
Manufacture	VIL	VIL	12(±0.5)V	Don't Care	0	0	1	0	0	0	0	0	#04
Device	VIH	VIL	12(±0.5)V	Don't Care	1	0	1	0	0	1	1	1	#E5

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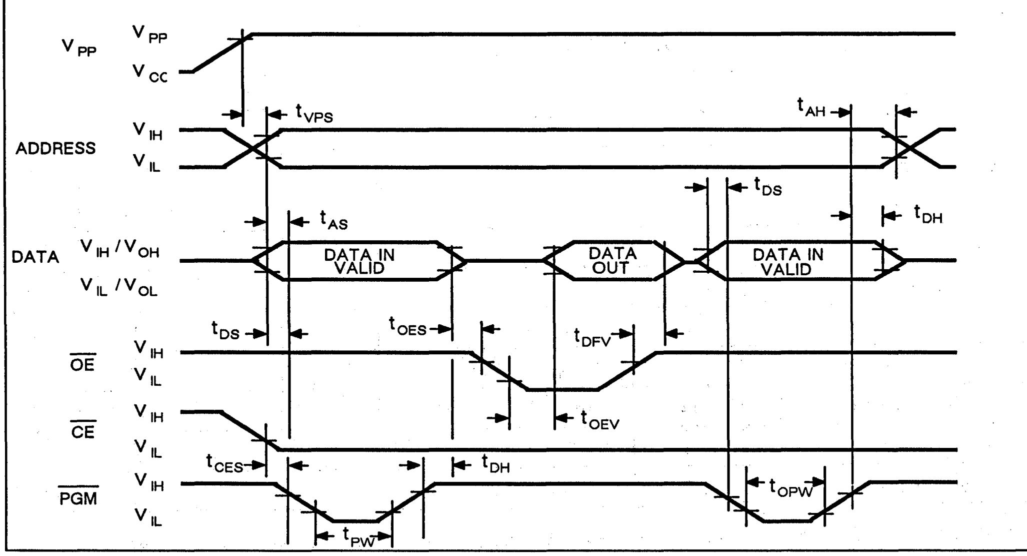
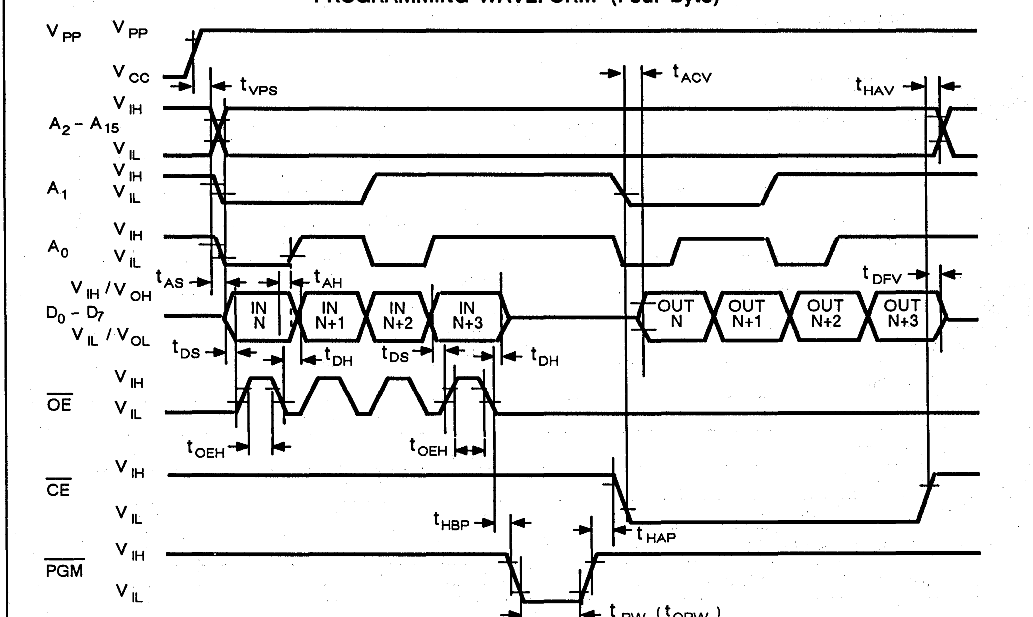
PROGRAMMING WAVEFORM (Single Byte)



PROGRAMMING WAVEFORM (Four Byte)



PROGRAMMING / ERASING INFORMATION (Cont'd)

DC CHARACTERISTICS

(T_A= 25 °C ± 5°C, V_{CC}[1] = 6V ± 0.25V, V_{PP}[2] = 12.5V ± 0.3V)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	I_{LI}	VIN = 6.25V/0V			10	μA
Input High Level	V_{IH}		2.4		V_{CC}+0.3	V
Input Low Level	V_{IL}		-0.1		0.6	V
V_{CC} Supply Current	I_{CC}				30	mA
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$=$\overline{PGM}$=V_{IL} ; $\overline{OE}$=V_{IH}			30	mA
V_{PP} Supply Current	I_{PP3}	$\overline{CE}$=V_{IH} ; $\overline{OE}$=$\overline{PGM}$=V_{IL}			100	mA
V_{PP} Supply Current	I_{PP4}	$\overline{PGM}$=V_{IH}			5	mA
Output Low Level	V_{OL}	IOL=2.1mA			0.45	V
Output High Level	V_{OH}	IOH=-400 μA	2.4			V

NOTE *1 V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}

*2 V_{PP} must not be greater than 13.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL} , $\overline{OE}$ = V_{IH} , V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

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AC CHARACTERISTICS
(Single Byte Programming)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			μS
Address Setup Time	t_{AS}	2			μS
Data Setup Time	t_{DS}	2			μS
$\overline{CE}$ Setup Time	t_{CES}	2			μS
$\overline{OE}$ Setup time	t_{OES}	2			μS
Address Hold Time	t_{AH}	2			μS
Data Hold Time	t_{DH}	2			μS
$\overline{OE}$ to Output Valid	t_{OEV}			500	ns
$\overline{OE}$ to Output Float	t_{DFV}			150	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Over Programming Pulse Number	N	1		25	times
Over Programming Pulse Width (Note)	t_{OPW}	1.4	1.5	39.4	ms

NOTE: t_{OPW} = 1.5 x Nms ± 5%

AC CHARACTERISTICS
(Four Byte Programming)

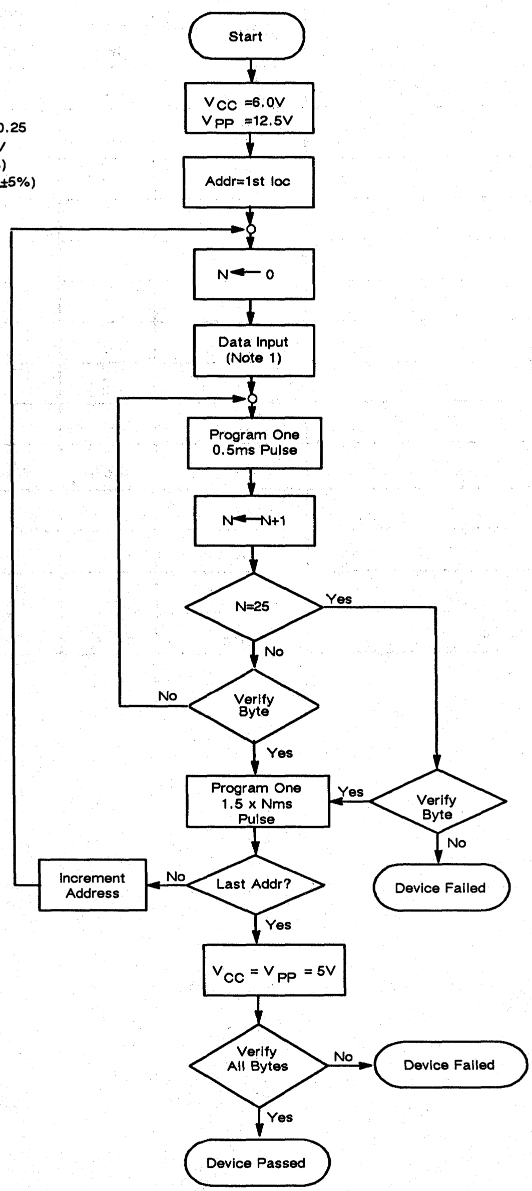
Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			µS
Address Setup Time	t_{AS}	2			µS
Data Setup Time	t_{DS}	2			µS
Address Hold Time	t_{AH}	2			µS
Data Hold Time	t_{DH}	2			µS
$\overline{OE}$ High Hold Time	t_{OEH}	2			µS
Hold Time Before Programming	t_{HBP}	2			µS
Hold Time After Program	t_{HAP}	2			µS
Address Access Time at Verify	t_{ACV}			500	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
$\overline{CE}$ to Output Float at Verify	t_{DFV}			150	ns
Hold Time After Verify	t_{HAV}	0			µs
Over Programming Pulse Number	N	1		25	times
Over Programming Pulse Width (Note)	t_{OPW}	1.4	1.5	39.4	ms

NOTE: $t_{OPW} = 1.5 \times N$ms ± 5%

PROGRAMMING / ERASING INFORMATION (Cont'd)

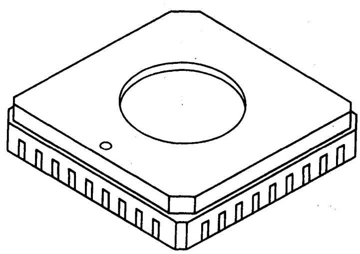
PROGRAMMING FLOWCHART FOR QUICK PRO ™

Notes:
1. 1-byte or 4-bytes
2. Conditions:
   - V_{CC} =6V(+5%) ± 0.25
   - V_{PP} =12.5(± 0.3)V
   - t_{PW} =0.5ms (±5%)
   - t_{OPW} =1.5 x Nms (±5%)

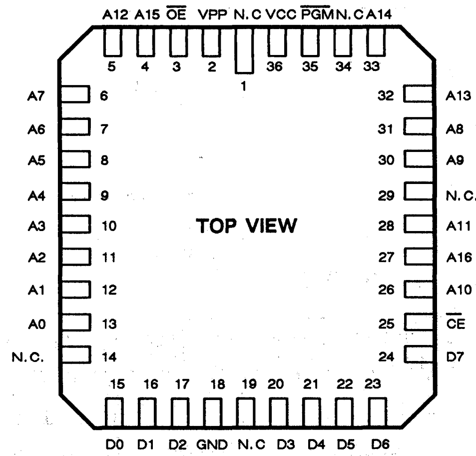


Quick Pro™ is a trademark of FUJITSU LIMITED

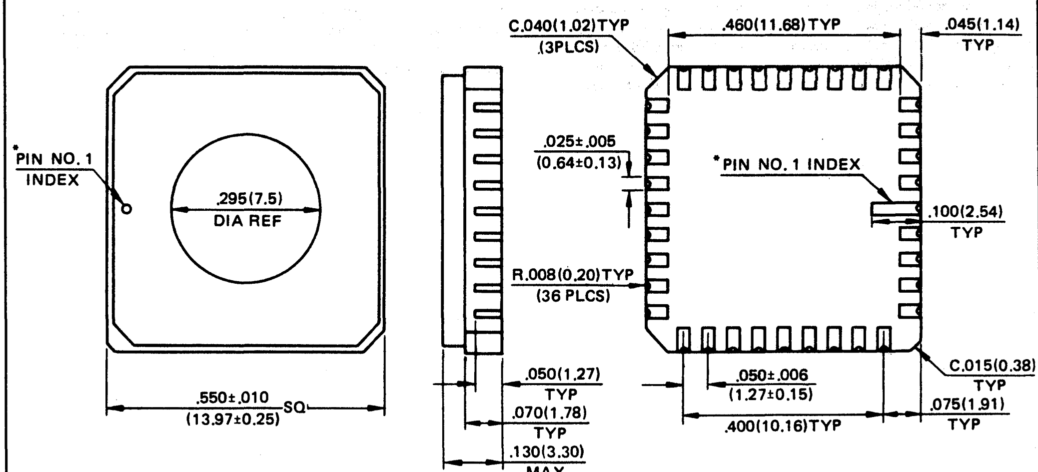
PACKAGE DIMENSIONS



LCC-36C-F01



36-LEAD CERAMIC LEADLESS CHIP CARRIER
(Case No.: LCC-36C-F01)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

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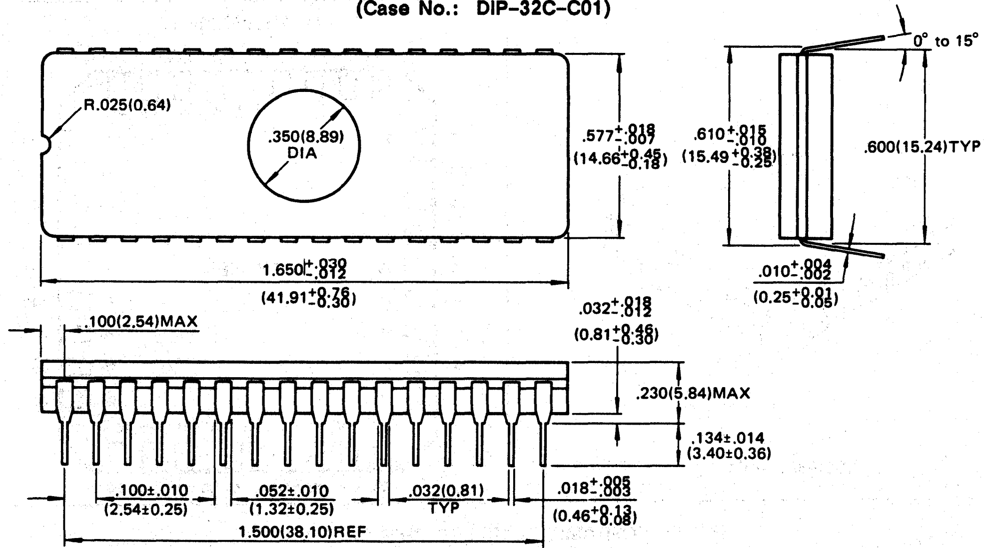
PACKAGE DIMENSIONS

32-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(Case No.: DIP-32C-C01)



Dimensions in inches (millimeters).

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The information contained in this document has been carefully checked and is believed to be reliable. However, Fujitsu assumes no responsibility for inaccuracies. Fujitsu reserves the right to change products or specifications without notice.

FUJITSU

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

MBM27C1001-15
MBM27C1001-20
MBM27C1001-25

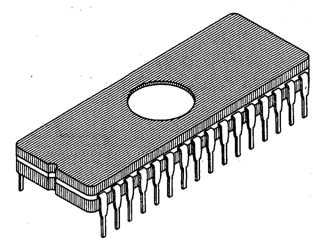
April 1988
Edition 2.0

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

The Fujitsu MBM27C1001 EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable. The device contains 1,048,576 programmable or reprogrammable bits organized in a 131,072-byte/8-bit format. The MBM27C1001 is housed in a 32-pin DIP and 36-pad LCC with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15-to-21 minutes. A new bit pattern can then be written into memory.

The MBM27C1001 EPROM is fabricated using CMOS double poly-silicon gate technology with stacked single-transistor gate cells. The MBM27C1001 is an excellent choice for system development work and in other applications where program changes are frequently necessary. Once programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

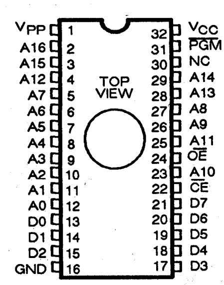
- 131,072-byte/8-bit organization with on-chip decoding
- Single-byte or four-byte programming capability with Quick Pro™ algorithm
- Static operation (no clocks required)
- Upward compatible with 256K/512K EPROMS
- Fast access time:
  MBM27C1001-15 = 150 ns (max)
  MBM27C1001-20 = 200 ns (max)
  MBM27C1001-25 = 250 nx (max)
- Easy and simple memory expansion via @pin
- Three-state output for wired-OR capability
- TTL-compatible inputs/outputs
- Single =5V (+10%) power supply with low current drain:
  Active operation = 30 mA (max) for 200ns/250ns
  40 mA (max) for 150ns
  Standby operation = 0.1 mA (max)
- Programming voltage: +12.5V
- JEDEC-approved pin assignments
- 32-pin CERDIP



CERAMIC PACKAGE
DIP-32C-C01

LCC-36C-F01 See Page 11

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with respect to ground	V_{CC}	-0.6 to + 7.0	V
Programming Voltage with respect to ground	V_{PP}	-0.6 to + 14.0	V
Input/Output Voltage (except for A_9 with respect to ground)	V_{IN_1}	-0.6 to V_{CC} + 0.3	V
Programming Voltage with respect to ground	V_{IN_2}	-0.6 to + 13.5	V
Temperature under Bias	T_{BIAS}	-25 to + 85	°C
Storage Temperature Range	T_{STG}	-65 to + 125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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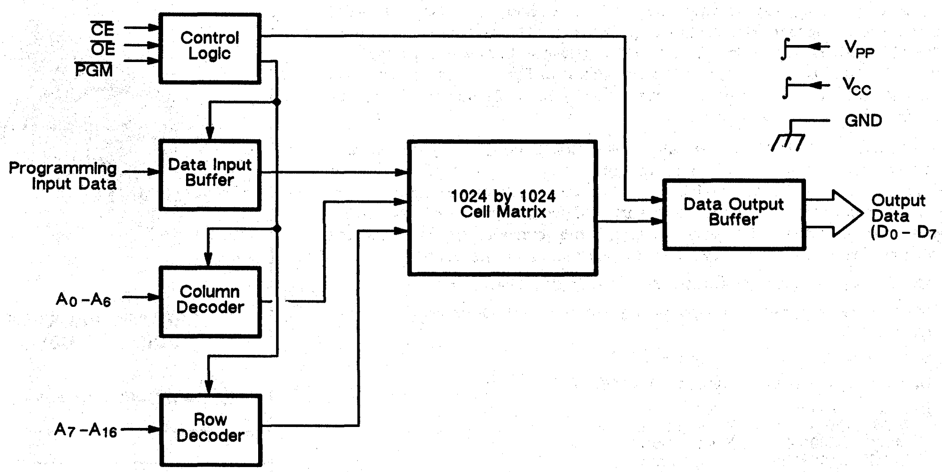
Fig. 1 — BLOCK DIAGRAM



9

CAPACITANCE (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}			12	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			12	pF

PIN DESCRIPTION

Symbol	Pin No. *	Function
V_{PP}	1	+12.5V programming voltage.
$A_0 - A_{16}$	2-12, 23 25-29	Address lines.
$O_0 - O_7$	13-15, 17-21	Three-state output data lines.
GND	16	Circuit ground.
$\overline{CE}$	22	When active Low, the device is enabled for data read.
$\overline{OE}$	24	Output enable. When $\overline{OE}$ and $\overline{CE}$ are active low and the $\overline{PGM}$ strobe is active High; all output lines ($D_0 - D_7$) are enabled.
NC	30	No connection.
$\overline{PGM}$	31	When active Low, programming data from the input buffer is written into a specified address of memory.
V_{CC}	32	+5V power supply

* This numbers are applied to DIP package.

FUNCTIONS AND PIN CONNECTIONS

OPERATING MODE	$A_0 - A_8$	A_9	$A_{10} - A_{16}$	Data	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}	GND
Standby	X	X	X	HI - Z	V_{IH}	X	X	5V	5V	0V
Read	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
Output Disable	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IL}	V_{IH} X	X V_{IL}	5V	5V	0V
Electronic Signature	Note 1	12V	X	CODE	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
Single Byte Program	A_{IN}	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	6V	12.5V	0V
Single Byte Verify	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
Single Byte Program Inhibit	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IL}	V_{IH}	V_{IH}	6V	12.5V	0V
Four Byte Data Input	Note 2	A_{IN}	A_{IN}	D_{IN}	V_{IH}	V_{IH}	V_{IH}	6V	12.5V	0V
Four Byte Program	X	A_{IN}	A_{IN}	HI-Z	V_{IH}	V_{IL}	V_{IL}	6V	12.5V	0V
Four Byte Verify	Note 2	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
Four Byte Program Inhibit	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IL}	V_{IH}	V_{IH}	6V	12.5V	0V

Legend:
X = Don't care

Notes:
1. A_0 is toggling address. A_1 is V_{IL}.
2. A_0 and A_1 can be either V_{IL} or V_{IH}

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{PP}	V_{CC} −0.6	V_{CC}	V_{CC} +0.6	V
Input High Level	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Level	V_{IL}	−0.1		0.8	V
Supply Voltage	GND		0		V
Operating Temperature	T_A	0		70	°C

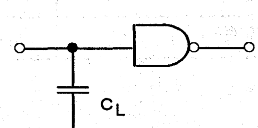
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Conditions	Values			Unit
				Min	Typ	Max	
Input Leakage Current		I_{LI}	$V_{IN} = V_{CC} = 5.5V$			10	µA
Output Leakage Current		I_{LO}	$V_{IN} = V_{CC} = 5.5V$			10	µA
V_{CC} Standby Current		I_{SB1}	$\overline{CE}=V_{IH}$			1	mA
V_{CC} Standby Current		I_{SB2}	$\overline{CE}=V_{CC}\pm0.3V$		1	100	µA
V_{CC} Active Current		I_{CC1}	$\overline{CE}=V_{IL}$, I_{OUT} =0mA			30	mA
V_{CC} Operation Current	150ns	I_{CC2}	$\overline{CE}=V_{IL}$: f =min, I_{OUT} =0mA			40	mA
	200ns/250ns					30	
V_{PP} Supply Current		I_{PP}	$V_{PP} = V_{CC} \pm0.6V$		1	100	µA
Output Low Level		V_{OL}	I_{OL} =2.1mA			0.45	V
Output High Level		V_{OH1}	I_{OH} = −400 µA	2.4			V
Output High Level		V_{OH2}	I_{OH} = −100 µA	V_{CC} −0.7			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input pulse levels:	0.45V to 2.4V (0.3V to 2.8V programming)
Input Rise/Fall Times:	≤20ns
Input Reference Levels:	0.8V to 2.0V (0.6V to 2.4V programming)
Output Reference Levels:	0.8V to 2.0V
Output Load:	1 TTL gate and C_L =100pF



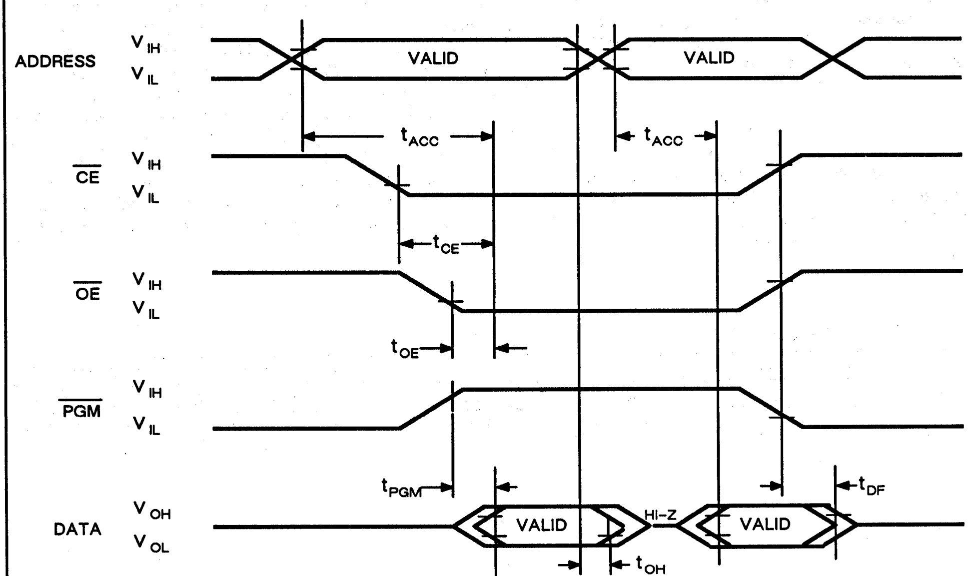
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C1001-15 Values		MBM27C1001-20 Values		MBM27C1001-25 Values		Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_{ACC}		150		200		250	ns
$\overline{CE}$ to Output Delay Time	t_{CE}		150		200		250	ns
$\overline{OE}$ to Output Delay Time	t_{OE}		70	0	70	0	100	ns
$\overline{PGM}$ to Output Delay Time	t_{PGM}		70	0	70	0	100	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float Delay (Note)	t_{DF}		60		60		60	ns
Address to Output Hold Time	t_{OH}	0		0		0		ns

NOTE: Output Float is defined as the point where data is no longer driven.

READ WAVEFORM



9

PROGRAMMING / ERASING INFORMATION

PROGRAMMING

Single-Byte Programming. When +12.5V(±0.3) volts is applied to V_{PP}, +6(±0.25) volts is applied to V_{CC}, $\overline{CE}$ and $\overline{PGM}$ = V_{IH}, and $\overline{OE}$= V_{IH}, the programming mode is initiated. Next, the proper address is input and the data pattern is applied to the input buffer (Figure 1). When both address and data are stable, a 0.5-millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of one byte. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Four-Byte Programming. When compared to single-byte programming, the four-byte programming method reduces the programming time by about 75% one quarter. Voltages applied to VPP and VCC are the same as those for single-byte programming; however, some logic levels differ--refer to "Four Byte Programming" in the Truth Table. In conjunction with the $\overline{OE}$ pin, address pins A0 and A1 are used to latch four bytes of data. When both address and data are stable, a 0.5 millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write,) should be applied to complete the programming of four bytes. Refer to the PROGRAMMING FLOWCHART for step-by-step programming procedures.

Caution

The width of one programming pulse must not exceed 40-millisecond; thus, a continuous TTL low-level voltage should not be applied to the $\overline{PGM}$ pin. Also, a 0.1-microfarad capacitor must be connected between V_{PP} and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

Electronic Signature/Programming Algorithm. When the MBM27C1001 is shipped from the factory, all memory cells (1,048,576 bits) are set to the High state (logic 1). During the programming procedure, affected bit cells are set to the Low (logic 0) state.

The MBM27C1001 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. Manufacturer and device codes are electronically stored in each device; these codes can be read at the output port (D0-D7) for the purpose of matching the device with the Quick Pro™ algorithm. The Electronic Signature Code List is shown preceding the ELECTRICAL CHARACTERISTICS.

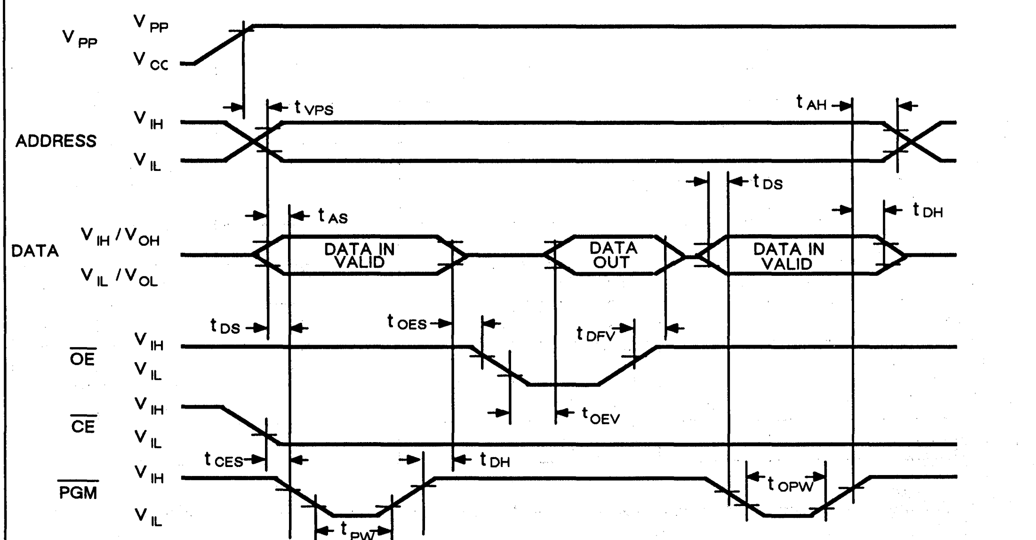
ERASING

In order to clear all memory cells of programmed contents, the MBM27C1001 must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 15Wsec/cm^2 is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 2537 Angstroms and with an intensity of 12mW/cm^2. Remove all filters from the lamp and clean the transparent lid of the MBM 27C1001 with a non-abrasive cleaner. Hold the MBM 27C1001 approximately one inch from the light source for 15-to-21 minutes. (Note. The MBM 27C1001 and other similar devices can be erased by light sources with longer wavelengths: however, the erasing time is much greater. Nonetheless, exposure to fluorescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

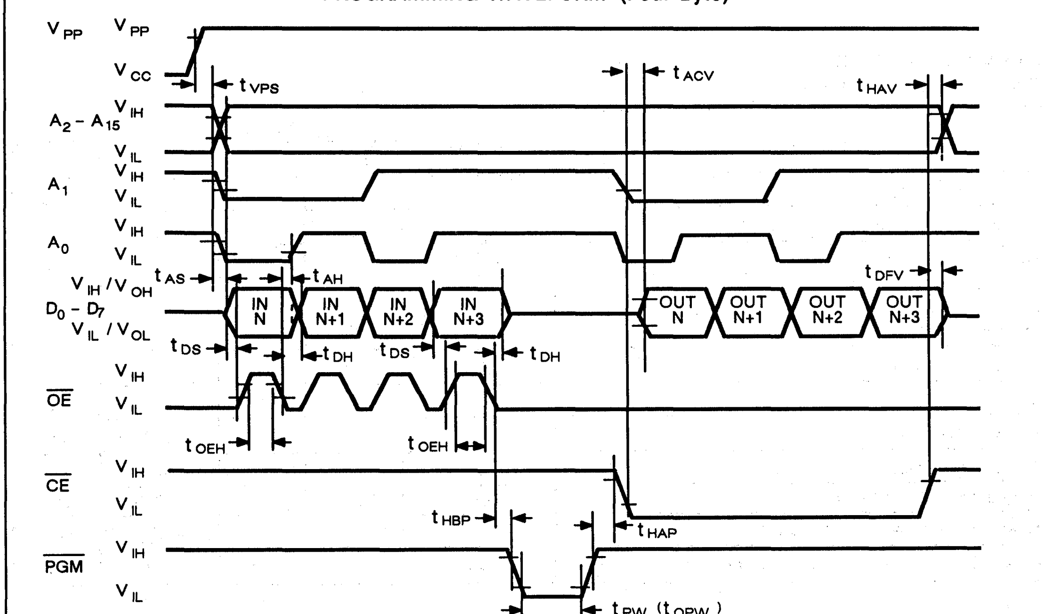
ELECTRONIC SIGNATURE CODE LIST

Definition	AO	A1 TO A6	A9	A7 to A16	D0	D1	D2	D3	D4	D5	D6	D7	HEX
Manufacture	VIL	VIL	12(±0.5)V	Don't Care	0	0	1	0	0	0	0	0	#04
Device	VIH	VIL	12(±0.5)V	Don't Care	0	1	1	0	0	1	1	1	#E6

PROGRAMMING WAVEFORM (Single Byte)



PROGRAMMING WAVEFORM (Four Byte)



9

DC CHARACTERISTICS (Programming Mode)
(T_A= 25 °C ± 5°C, V_{CC}[1] = 6V ± 0.25V, V_{PP}[2] = 12.5V ± 0.3V)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	I_{LI}	VIN = 6.25V/0V			10	μA
Input High Level	V_{IH}		2.4		V_{CC}+0.3	V
Input Low Level	V_{IL}		-0.1		0.6	V
V_{CC} Supply Current	I_{CC}				30	mA
V_{PP} Supply Current	I_{PP1}	$\overline{CE}$=$\overline{PGM}$=V_{IL} ; $\overline{OE}$=V_{IH}			30	mA
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$=V_{IH} ; $\overline{OE}$=$\overline{PGM}$=V_{IL}			100	mA
V_{PP} Supply Current	I_{PP3}	$\overline{PGM}$=V_{IH}			5	mA
Output Low Level	V_{OL}	IOL=2.1mA			0.45	V
Output High Level	V_{OH}	IOH=-400 μA	2.4			V

NOTE *1 V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP} .

*2 V_{PP} must not be greater than 13.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL} , $\overline{OE}$ = V_{IH} , V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

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AC CHARACTERISTICS
(Single Byte Programming)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			μS
Address Setup Time	t_{AS}	2			μS
Data Setup Time	t_{DS}	2			μS
$\overline{CE}$ Setup Time	t_{CES}	2			μS
$\overline{OE}$ Setup time	t_{OES}	2			μS
Address Hold Time	t_{AH}	2			μS
Data Hold Time	t_{DH}	2			μS
$\overline{OE}$ to Output Valid	t_{OEV}			500	ns
$\overline{OE}$ to Output Float	t_{DFV}			150	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Over Programming Pulse Number	N	1		25	times
Over Programming Pulse Width (Note)	t_{OPW}	1.4	1.5	39.4	ms

NOTE: t_{OPW} = 1.5 x Nms ± 5%

AC CHARACTERISTICS
(Four Byte Programming)

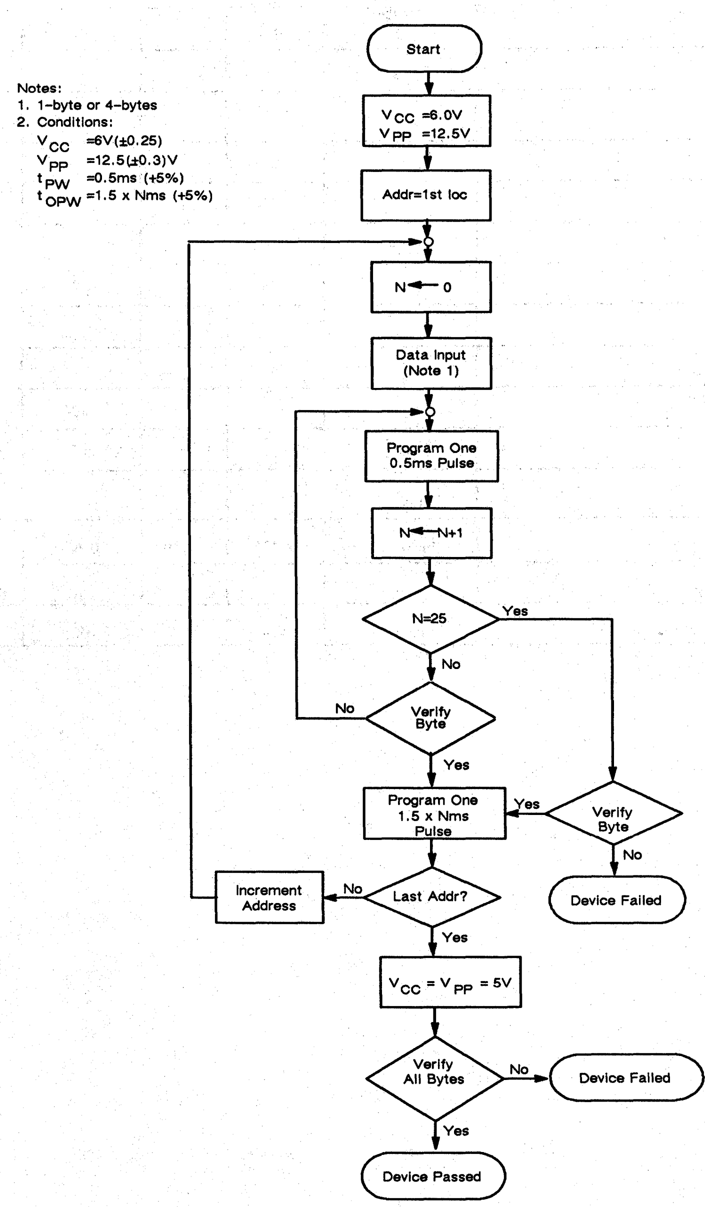
Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			μs
Address Setup Time	t_{AS}	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
$\overline{OE}$ High Hold Time	t_{OEH}	2			μs
Hold Time Before Programming	t_{HBP}	2			μs
Hold Time After Program	t_{HAP}	2			μs
Address Access Time at Verify	t_{ACV}			500	ns
$\overline{CE}$ to Output Float at Verify	t_{DFV}			150	ns
Hold Time After Verify	t_{HAV}	0			μs
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Over Programming Pulse Number	N	1		25	times
Over Programming Pulse Width (Note)	t_{OPW}	1.4	1.5	39.4	ms

NOTE: t_{OPW} = 1.5 x Nms ± 5%

9

PROGRAMMING / ERASING INFORMATION (Cont'd)

PROGRAMMING FLOWCHART FOR QUICK PRO™



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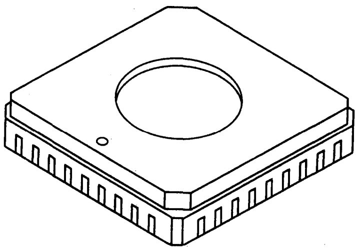
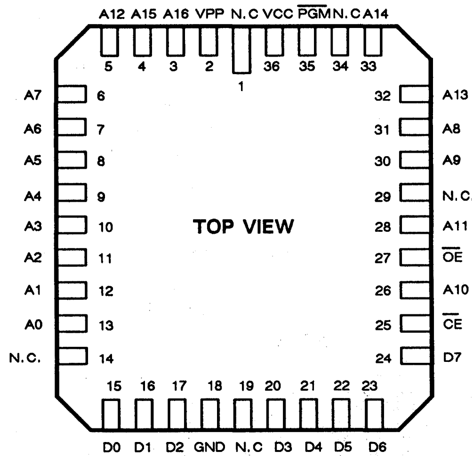
PACKAGE DIMENSIONS

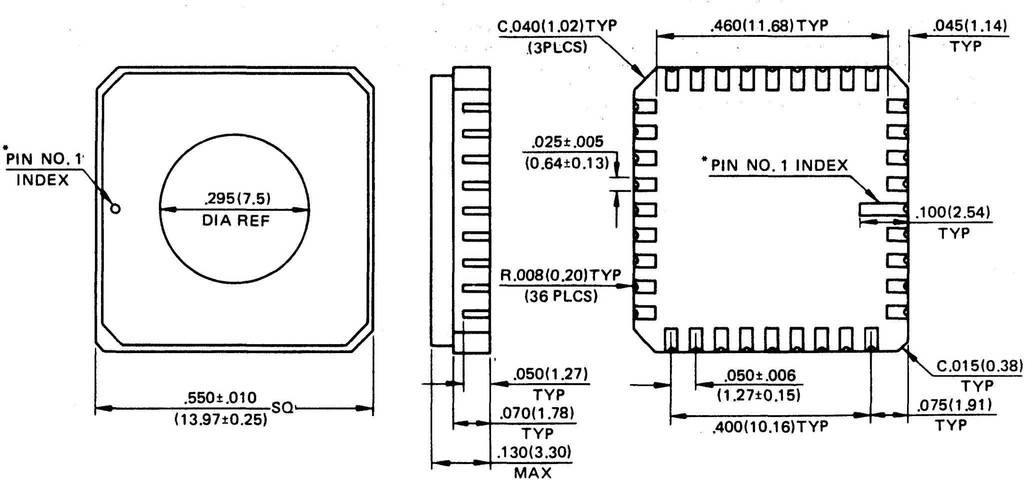


LCC-36C-F01

PIN ASSIGNMENT



32-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(Case No.: LCC-36C-F01)



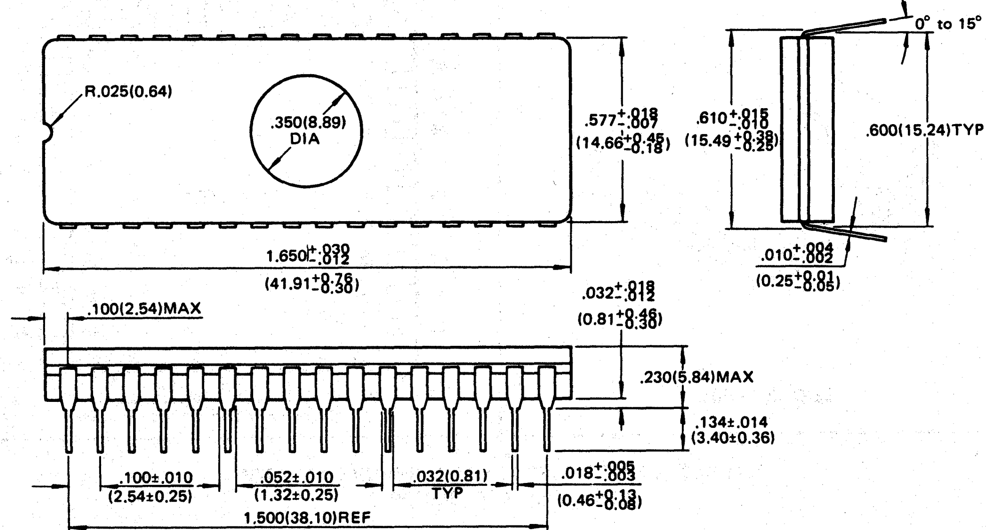
* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in inches (millimeters)

9

PACKAGE DIMENSIONS

32-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(Case No.: DIP-32C-C01)



Dimensions in inches (millimeters).

FUJITSU

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

MBM27C1024-15 MBM27C1024-20 MBM27C1024-25

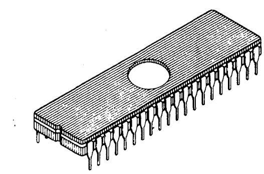
August 1988
Edition 1.0

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

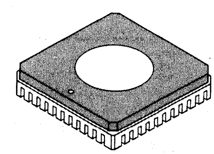
The Fujitsu MBM27C1024 is a high speed read-only static memory that is UV-erasable and reprogrammable. The devices contains 1,048,576 programmable or reprogrammable bits organized in a 65,536-word/16-bits format. The MBM27C1024 is housed in both 40-pin DIP and 44-pad LCC package with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 12 to 21 minutes. A new bit pattern can then be written into memory.

The MBM27C1024 is fabricated using CMOS double poly-silicon gate technology with stacked single-transistor gate cells. The MBM27C1024 is an excellent choice for system development work and in other applications where programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the acitve and standby modes of operation.

- 65,536 words x 16 bit organization, with on chip decoding
- One-word or two-word programming capability with Quick-Pro™ algorithm
- Static operation (no clocks required)
- Easy and simple memory expansion via $\overline{OE}$
- High active bus enables $\overline{PGM}$
- Three-state output for wired-OR capability
- Fast access time:
  150ns max. (MBM27C1024-15)
  200ns max (MBM27C1024-20)
  250ns max. (MBM27C1024-25)
- Single +5V(±10%) power supply with low current drain:
  Active operation = 30mA (max) for 200ns/250ns
  40mA (max) for 150ns
  Standby operation = 0.1mA (max)
- Programming voltage: 12.5V
- JEDEC approved pin assignment
- 40-pin Ceramic(Cerdip) DIP Package: suffix =Z
- 44-pad Frit seal LCC package: Suffix =TV

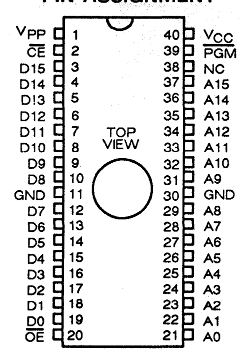


CERAMIC PACKAGE
DIP-40C-C02



CERAMIC PACKAGE
LCC-44C-F01

PIN ASSIGNMENT



LCC : See page 11

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

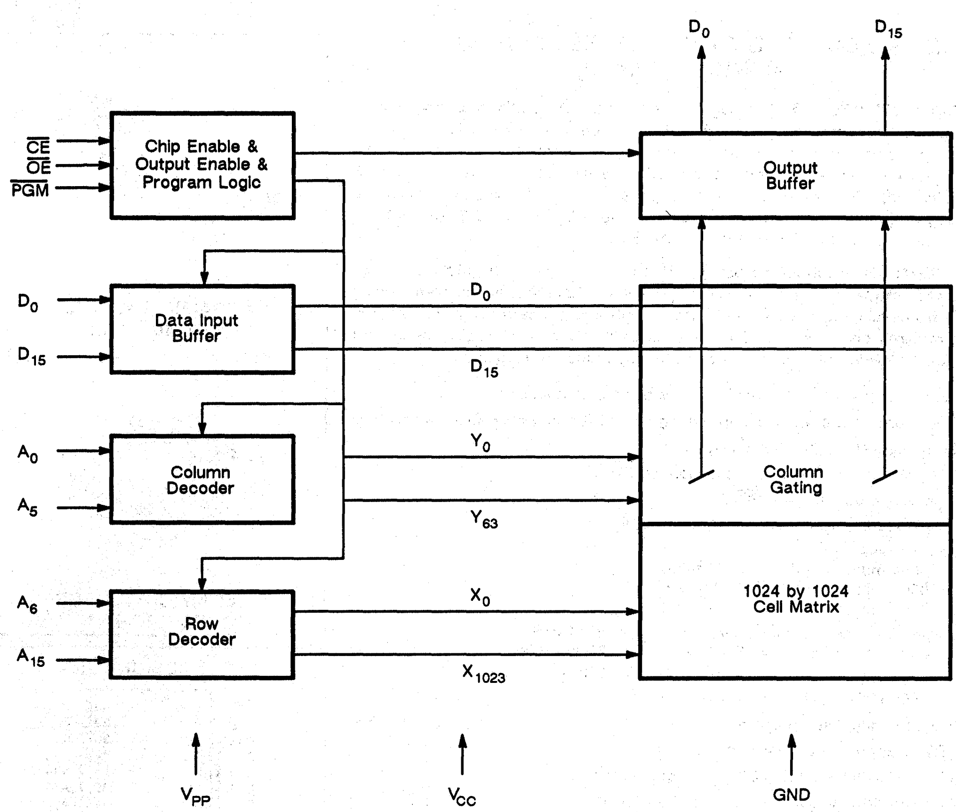
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
V_{CC} Supply Voltage with respect to GND	V_{CC}	-0.6 to 7.0	V
V_{PP} Supply Voltage with respect to GND	V_{PP}	-0.6 to 14.0	V
All Input/Output Voltage except for A_9 with respect to ground	$V_{IN\ 1}$	-0.6 to V_{CC} +0.3	V
A9 Voltage with respect to GND	$V_{IN\ 2}$	-0.6 to + 13.5	V
Temperature under Bias	T_{BIAS}	-25 to + 85	°C
Storage Temperature Range	T_{STG}	-65 to + 125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Quick Pro™ is a trademark of FUJITSU LIMITED

Fig. 1 — BLOCK DIAGRAM



9

CAPACITANCE (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}		10	12	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		10	12	pF

PIN DESCRIPTION

Symbol	Pin No. *	Function
V_{PP}	1	+5V power supply. When +12.5V is applied, the device is enabled for programming operation.
$\overline{CE}$	2	Chip enable. When active Low, the device is enabled for data read and programming operations.
D_0 - D_{15}	19-12, 10-3	Three-state output data line.
GND	11,30	Circuit ground.
$\overline{OE}$	20	Output enable. When active Low, all output lines are enabled.
A_0 - A_{15}	21-29, 31-37	Address lines.
NC	38	No connection.
$\overline{PGM}$	39	Program.
V_{CC}	40	+5V power supply

*This numbers are applied to DIP package.

FUNCTIONAL TRUTH TABLE

MODE	A_0-A_8	A_9	A_{10} - A_{15}	Data	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}	GND
Standby	X	X	X	HI-Z	V_{IH}	X	X	5V	5V	0V
Read	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
Output Disable	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IL}	V_{IH} / X	X / V_{IL}	5V	5V	0V
One-Word Program	A_{IN}	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	6V	12.5V	0V
One-Word Verify	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
One-Word Program Inhibit	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IL}	V_{IH}	V_{IH}	6V	12.5V	0V
Two-Word Data Input	A_{IN} *	A_{IN}	A_{IN}	D_{IN}	V_{IH}	V_{IH}	V_{IH}	6V	12.5V	0V
Two-Word Program	A_{IN} *	A_{IN}	A_{IN}	HI-Z	V_{IH}	V_{IL}	V_{IL}	6V	12.5V	0V
Two-Word Verify	A_{IN} *	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
Two-Word Program Inhibit	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IH}	V_{IL}	V_{IH}	6V	12.5V	0V
Electronic Signature	A_{IN} *	12V	X	CODE	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V

Legend: X = Don't care
A_{IN} = Address input
D_{IN} = Data input
D_{OUT} = Data output

Notes: *. A_0 is toggling address.

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

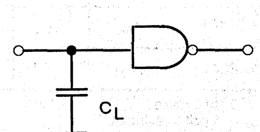
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} -0.6	V_{CC}	V_{CC} +0.6	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted)

Parameter		Conditions	Symbol	Values Min	Values Typ	Values Max	Unit
Input Leakage Current		V_{IN} = V_{CC} = 5.5V	I_{LI}	-10		10	μA
Output Leakage Current		V_{OUT} = V_{CC} = 5.5V	I_{LO}	-10		10	μA
V_{CC} Standby Current		$\overline{CE}$=V_{IH}	I_{SB1}			1	mA
V_{CC} Standby Current		$\overline{CE}$=V_{CC} ±0.3V	I_{SB2}		1	100	μA
V_{CC} Active Current		$\overline{CE}$=V_{IL}, I_{OUT} =0mA	I_{CC1}			30	mA
V_{CC} Operation Current	150 ns 200ns/250ns	$\overline{CE}$=V_{IL}: f =Min, I_{OUT} =0mA	I_{CC2}			40 30	mA
V_{PP} Supply Current		V_{PP} = V_{CC} ±0.6V	I_{PP1}		1	100	μA
Input High Level			V_{IH}	2.0		V_{CC} +0.3	V
Input Low Level			V_{IL}	-0.1		0.8	V
Output Low Level		I_{OL} =2.1mA	V_{OL}			0.45	V
Output High Level		I_{OH} = -400 μ A	V_{OH_1}	2.4			V
Output High Level		I_{OH} = -100 μ A	V_{OH_2}	V_{CC}-0.7			V

AC TEST CONDITIONS

Input pulse levels:	0.45V TO 2.4V
Input Rise/Fall Times:	≤20ns
Input Reference Levels:	0.8V TO 2.0V
Output Reference Levels:	0.8V to 2.0V
Output Load:	1 TTL gate and C_L =100pF



9

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

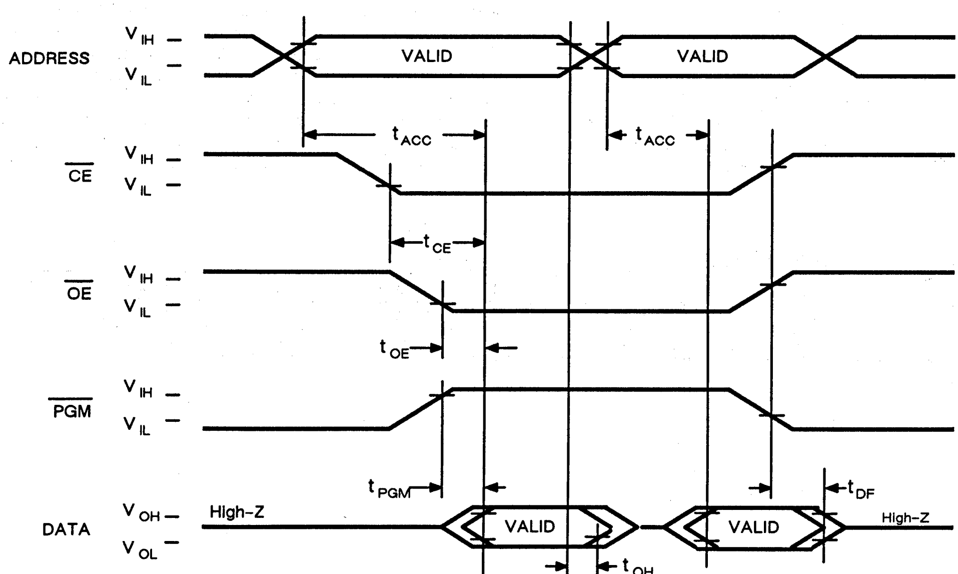
Parameter	Symbol	MBM27C1024-15 Values		MBM7C1024-20 Values		MBM27C1024-25 Values		Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_{ACC}		150		200		250	ns
$\overline{CE}$ to Output Delay Time	t_{CE}		150		200		250	ns
$\overline{OE}$ to Output Delay Time *1	t_{OE}		70		70		100	ns
$\overline{PGM}$ to Output Delay Time *1	t_{PGM}		70		70		100	ns
$\overline{CE}$, $\overline{OE}$ or $\overline{PGM}$ to Output Float Delay*2	t_{DF}	0	60	0	60	0	60	ns
Address to Output Hold Time	t_{OH}	0		0		0		ns

NOTE: *1: $\overline{OE}$ ($\overline{PGM}$) may be delayed up to tACC-tOE(tPGM) after the falling edge of $\overline{CE}$ without impact on tACC.

*2: tDF is specified from $\overline{CE}$, $\overline{OE}$ or $\overline{PGM}$, whichever occurs first. tDF is defined as the point where data is no longer driven.

9

READ WAVEFORM



PROGRAMMING / ERASING INFORMATION

PROGRAMMING

One-Word Programming. When +12.5V(±0.3V) is applied to V_{PP}, +6V (±0.25V) is applied to V_{CC}, $\overline{CE}$ = VIL, $\overline{PGM}$ and $\overline{OE}$ = VIH, the programming mode is initiated. Next, the proper address is input and the data pattern is applied to the input buffer(Figure 1). When both address and data are stable, a 0.5ms negative pulse is applied to the $\overline{PGM}$. Upon verification of written data read out by $\overline{OE}$ an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of one word. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Two-Word Programming. When compared to one-word programming, the two-word programming method reduces the programming time by about 50% one half. Voltages applied to V_{PP} and V_{CC} are the same as those for one-word programming; however, some logic levels differ--refer to "Two Word Programming" in the Truth Table. In conjunction with the $\overline{OE}$ pin, address A0 is used to latch two words of data. When both address and data are stable, a 0.5ms negative pulse is applied to the $\overline{PGM}$. Upon verification of written data read out by $\overline{OE}$ an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of two words. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Caution

The width of one programming pulse must not exceed 40ms; thus, a continuous TTL low-level voltage should not be applied to the $\overline{PGM}$ pin. Also, a 0.1µF capacitor must be connected between V_{PP} and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

Electronic Signature/Programming Algorithm. When the MBM27C1024 is shipped from the factory, all memory cells (1,048,576 bits) are set to the High state (logic 1). During the programming procedure, affected bit cells are set to the Low state (logic 0).

The MBM27C1024 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. Manufacturer and device codes are electronically stored in each device; these codes can be read at the output port (D0 to D15) for the purpose of matching the device with the Quick Pro™ algorithm. The ELECTRONIC SIGNATURE CODE LIST is shown preceding the ELECTRICAL CHARACTERISTICS.

ERASING

In order to clear all memory cells of programmed contents, the MBM27C1024 must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 15Wsec/cm^2 is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 253.7nm with an intensity of 12mW/cm^2. Remove all filters from the lamp and clean the transparent lid of the MBM27C1024 with a non-abrasive cleaner. Hold the MBM27C1024 approximately one inch from the light source for 15-to-21 minutes. (Note. The MBM27C1024 and other similar devices can be erased by light sources with longer wavelengths: however, the erasing time is much greater. Nonetheless, exposure to fluorescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

ELECTRONIC SIGNATURE CODE LIST

Definition	AO	A1 TO A5	A6 to A15	O0	O1	O2	O3	O4	O5	O6	O7	D8 to D15	HEX
Manufacture	VIL	VIL	Don't Care	0	0	1	0	0	0	0	0	0	#04
Device	VIH	VIL	Don't Care	0	0	1	0	0	1	1	0	0	#64

Note: A9=12V±0.5V

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DC CHARACTERISTICS *(DURING PROGRAMMING)*
(T_A= 25 °C ± 5°C, V_{CC}*1 = 6V ± 0.25V, V_{PP}*2 = 12.5V ± 0.3V)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Input Low Level	V_{IL}	-0.1		0.8	V
Input Load Current	I_{LI}	-10		10	μA
V_{CC} Supply Current	I_{CC}			30	mA
V_{PP} Supply Current ($\overline{CE}$=$\overline{PGM}$=V_{IL} ; $\overline{OE}$=V_{IH})	I_{PP21}			50	mA
V_{PP} Supply Current ($\overline{CE}$=V_{IH} ; $\overline{OE}$=$\overline{PGM}$=V_{IL})	I_{PP22}			100	mA
V_{PP} Supply Current ($\overline{PGM}$=V_{IH})	I_{PP3}			5	mA
Output Low Level (IOL=2.1mA)	V_{OL}			0.45	V
Output High Level (IOH=-400 μA)	V_{OH}	2.4			V

NOTE *1 V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP} .

*2 V_{PP} must not be greater than 13V including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{PGM}$ = V_{IL} ,V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

AC CHARACTERISTICS *(AT ONE WORD PROGRAMMING)*

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			μs
Address Setup Time	t_{AS}	2			μs
Data Setup Time	t_{DS}	2			μs
$\overline{CE}$ Setup Time	t_{CES}	2			μs
$\overline{OE}$ Setup time	t_{OES}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
$\overline{OE}$ to Output Valid	t_{OEV}			500	ns
$\overline{OE}$ to Output Float	t_{DFV}			150	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Programming Pulse Number	N	1		25	times
Over Programming Pulse Width	t_{OPW}	1.4	1.5*	39.4	ms

NOTE: t_{OPW} = 1.5 x Nms ± 5%

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AC CHARACTERISTICS *(AT TWO WORD PROGRAMMING)*

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			µS
Address Setup Time	t_{AS}	2			µS
Data Setup Time	t_{DS}	2			µS
Address Hold Time	t_{AH}	2			µS
Data Hold Time	t_{DH}	2			µS
$\overline{OE}$ High Hold Time	t_{OEH}	2			µS
Hold Time Before Programming	t_{HBP}	2			µS
Hold Time After Program	t_{HAP}	2			µS
Hold Time After Verify	t_{HAV}	0			µS
Address Access Time at Verify	t_{ACV}			500	ns
$\overline{CE}$ to Output Float at Verify	t_{DFV}			150	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Programming Pulse Number	N	1		25	times
Over Programming Pulse Width (Note)	t_{OPW}	1.4	1.5*	39.4	ms

NOTE: t_{OPW} = 1.5 x Nms ± 5%

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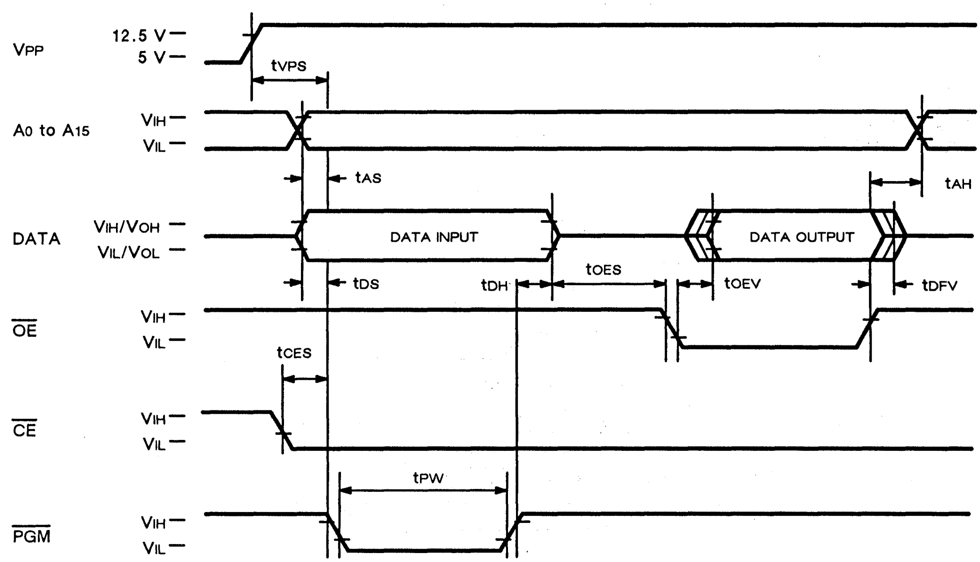
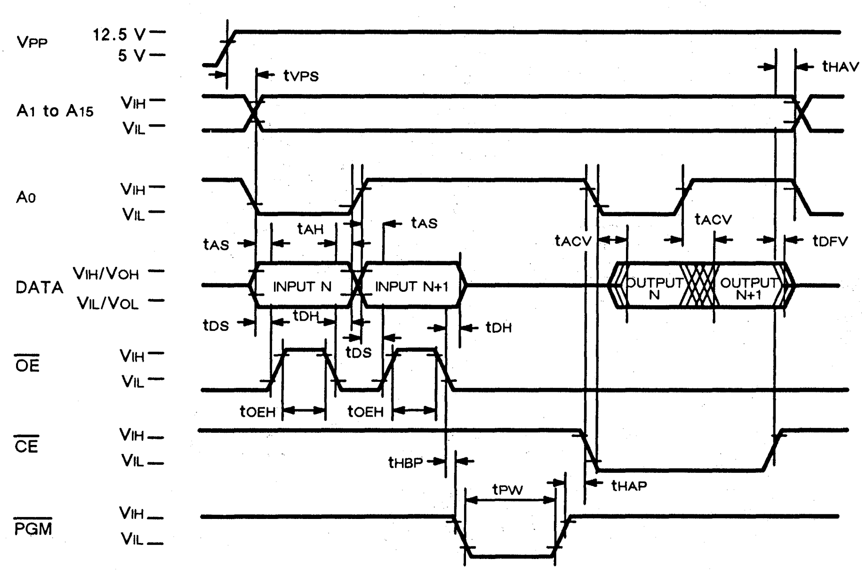
ONE-WORD PROGRAMMING WAVEFORM



TWO-WORD PROGRAMMING WAVEFORM



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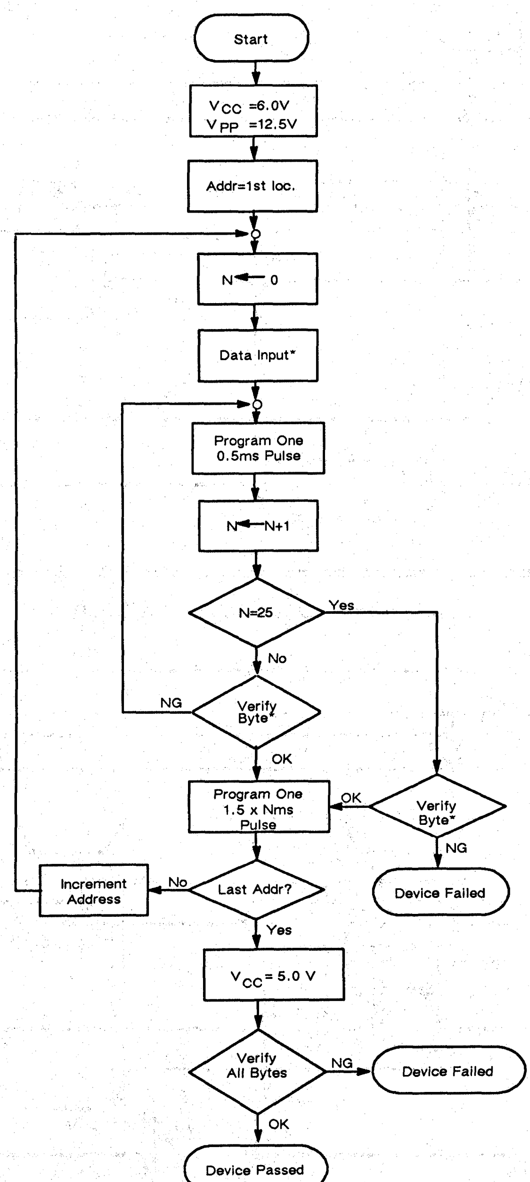
PROGRAMMING FLOWCHART

V_{CC} =6V ±0.25V
V_{PP} =12.5 ± 0.3V
t_{PW} =0.5ms ± 5%
t_{OPW} =1.5 x Nms ±5%



*: 1 word or 2 words

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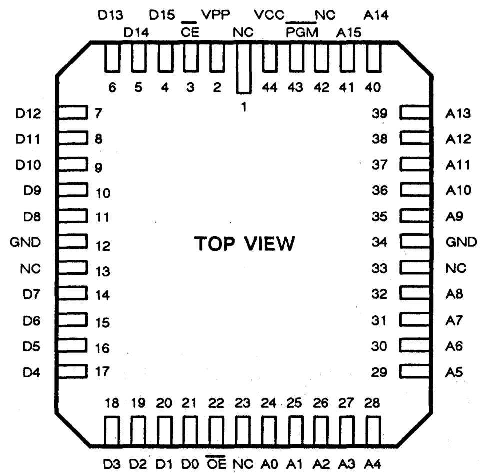
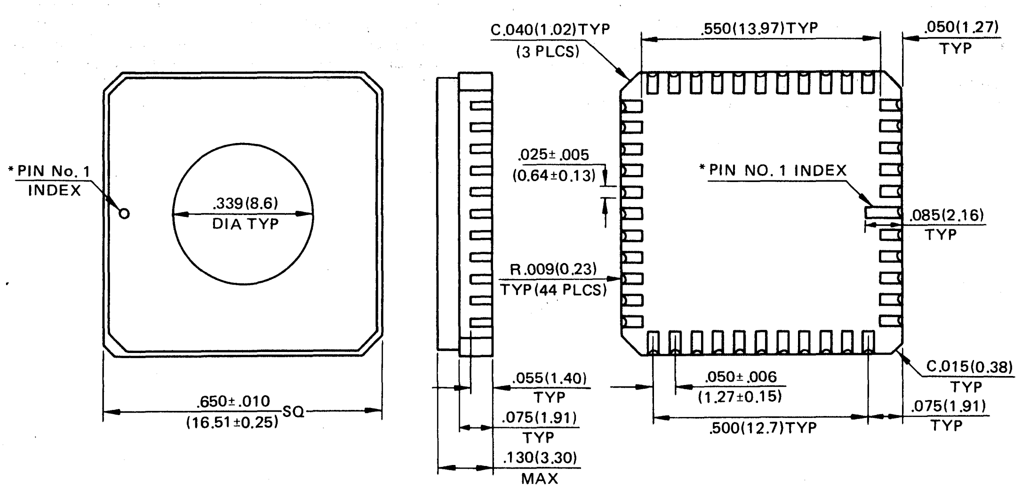
PACKAGE DIMENSIONS



44-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIR
(CASE No.: LCC-44C-F01)

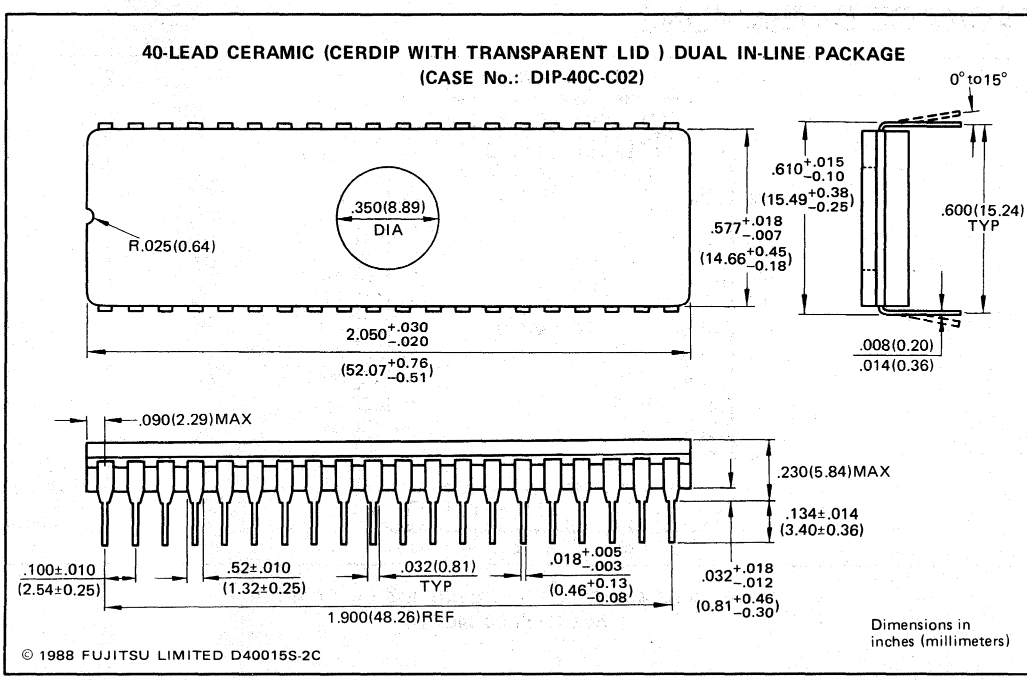


* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS



9

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY

MBM27C1028-15
MBM27C1028-20
MBM27C1028-25

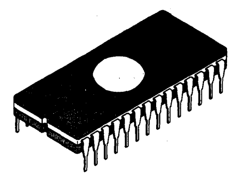
CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

September 1988
Edition 1.0

The Fujitsu MBM27C1028 EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable. The devices contains 1,048,576 programmable or reprogrammable bits organized in a 131,072-byte/8 bit or 65,536-word/16-bit format. The MBM27C1028 has a mulitplexed address and data pin which permits the device to reduce the number of pin-count for portable system where compact circuit layout is required. The MBM27C1028 can then be housed in a 28-pin DIP or a 32-pad LCC with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15-to-21 minutes. A new bit pattern can then be written into memory.

The MBM27C1028 EPROM is fabricated using CMOS double polysilicon gate technology with stacked single transistor gate cells. The MBM27C1028 is an excellent choice for system development work and in other applications where program changes are frequently necessary. Once programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

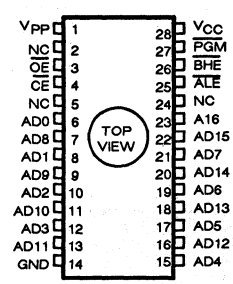
- 65,536 word/16 bit organization with on chip decoding
- 16-bit or 8-bit organization capability using a control signal
- On-chip latches for address
- Easy and simple memory expansion via $\overline{OE}$ pin
- Three-state output for word-OR capability
- TTL-compatible inputs/outputs
- Fast access time:
  MBM27C1028-15 = 150ns (max.)
  MBM27C1028-20 = 200ns (max.)
  MBM27C1028-25 = 250ns (max.)
- Single +5V(±10%) power supply with low current drain:
  Active operation = 30mA (max)
  Standby operation = 0.1mA (max)
- Programming voltage: +12.5V(±0.3V)
- Programming capability with Quick Pro™ algorithm
- No interface to be required to MBL8086 and MBL80168
- JEDEC approved pin assignments
- Standard package:
  28-pin Ceramic (Cerdip) DIP Package : suffix = Z
  32-pad Frit seal LCC Package : suffix = TV



CERAMIC PACKAGE
DIP-28C-C01

LCC-32C-F01 See Page 11

PIN ASSIGNMENT



LCC : See page 11

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7.0	V
VPP Voltage with Respect to GND	V_{PP}	-0.6 to +14.0	V
All Inputs, I/Os Voltage with Respect to GND	V_{IN}, $V_{I/O}$	-0.6 to V_{CC}+0.3	V
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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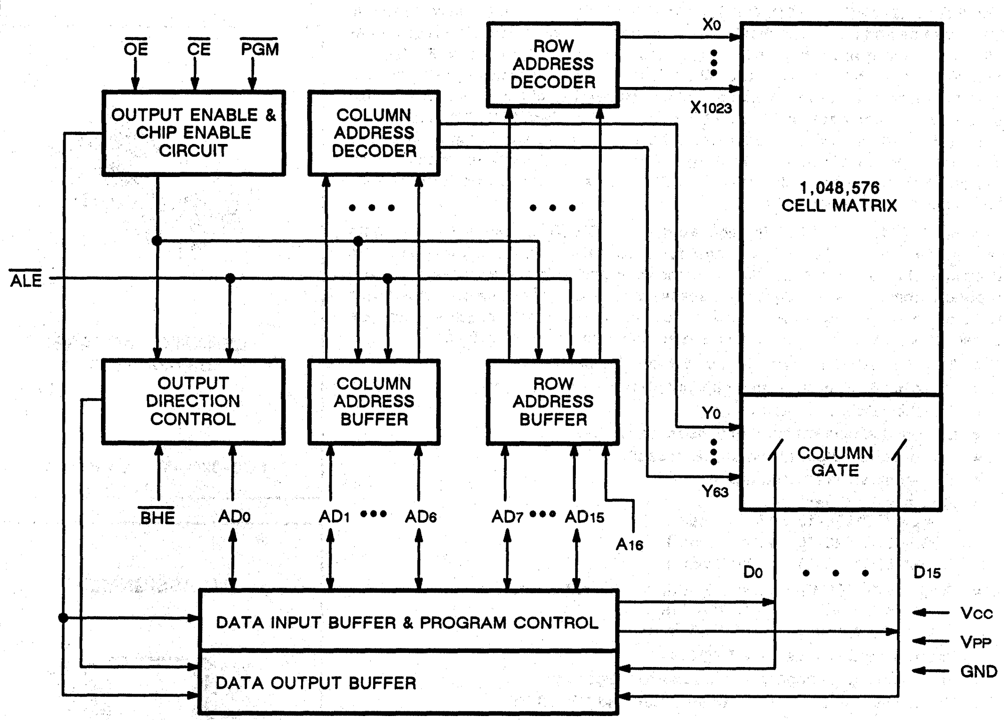
Fig. 1 — MBM27C1028 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}		6	8	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	12	pF

PIN DESCRIPTION

Symbol	Pin No. (Pad No.)	Function
VPP	1 (2)	+12.5V programming voltage
NC	2,5,24 (1,3,6,12,17,26,28)	No connection
$\overline{OE}$	3 (4)	Output enable. When $\overline{OE}$ and $\overline{CE}$ are active low and the $\overline{PGM}$ strove is active High; all proper output lines (Either "AD0 to AD15" or "AD0 to AD7" are enabled.
$\overline{CE}$	4 (5)	Chip enable. When active low, the device is enabled for data read and programming operations.
AD0 to AD15	6-13,15-22 (7-11,13-15,18-25)	Address/Data. When $\overline{OE}$ is High, all ADs work as address input line. When Low, all ADs work as data output line.
GND	14 (16)	Circuit ground
A16	23 (27)	Address line (MSB)
$\overline{ALE}$	25 (29)	Address latch enable. When $\overline{CE}$ is Low and $\overline{ALE}$ is High, the address from input buffer is transffer to address decoder by falling edge of ALE.
$\overline{BHE}$	26 (30)	Bus high enable. When $\overline{BHE}$ is Low in conjection with AD0, a word/16-bit data is available. When $\overline{BHE}$ is High, a byte/8-bit data is avalrable.
$\overline{PGM}$	27 (31)	Program Control/Output Enable. When active Low, programming data from the input buffer is written into a specified of memory provided the following conditions are met: VPP=12.5V; VCC=6V, CE=ALE=Low; OE=High.
VCC	28 (32)	+5V Power supply

FUNCTIONAL TRUTH TABLE

Mode \ Pin Name	AD_0	$AD_1 - AD_{15}$	A16	$\overline{ALE}$	$\overline{BHE}$	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}	GND
STANDBY	High-Z	High-Z	X*1	X	X	VIH	X	X	5V	5V	OV
READ ADDRESS LATCH	X*2	AIN	AIN	↓	X*2	VIL	VIH / X	X / VIL	5V	5V	OV
READ	DOUT*2	DOUT*2	X	VIL	X	VIL	VIL	VIH	5V	5V	OV
OUTPUT DISABLE	High-Z	High-Z	X	VIL	X	VIL	VIH / X	X / VIL	5V	5V	OV
PROGRAM ADDRESS LATCH	VIL	AIN	AIN	↓	VIL	VIL	VIH	VIH	6V	12.5V	OV
PROGRAM	DIN	DIN	X	VIL	X	VIL	VIH	VIL	6V	12.5V	OV
RROGRAM VERIFY	DOUT	DOUT	X	VIL	X	VIL	VIL	VIH	6V	12.5V	OV
PROGRAM INHIBIT	High-Z	High-Z	X	X	X	VIH	X	X	6V	12.5V	OV

Note *1: X can be either VIL or VIH.
*2: See below.

ADo and $\overline{BHE}$ should be basically used to enable for the lower and upper byte of the data, respectively. But when both ADo and $\overline{BHE}$ are high, it enable to transfer the upper byte data to lower byte bus, ADo to AD7; thus, if $\overline{BHE}$ pulled High, the MBM27C1028 can be used for byte wide/8-bit memory, organized 128K words by 8 bit.

ADo	$\overline{BHE}$	ADo to AD7	AD8 to AD15
VIL	VIL	Do to D7	D8 to D15
VIL	VIH	Do to D7	High-Z
VIH	VIL	High-Z	D8 to D15
VIH	VIH	D8 to D15	High-Z

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RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

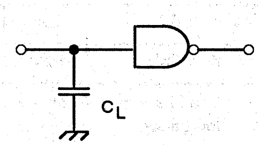
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{CC}-0.6	V_{CC}	V_{CC} +0.6	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Load Current V_{IN} = 5.5V)	$\lvert I_{LI} \rvert$			10	µA
Output Leakage Current (V_{OUT}=5.5V)	$\lvert I_{LO} \rvert$			10	µA
V_{PP} Supply Current	I_{PP_1}		1	100	µA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{SB_1}		0.3	1	mA
V_{CC} Standby Current ($\overline{CE}$ =V_{CC} +0.3V)	I_{SB_2}		1	100	µA
V_{CC} Active Current ($\overline{CE}$ = V_{IL},I_{OUT} = 0mA)	I_{CC_1}		10	30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0mA)	I_{CC_2}		8	30	mA
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = -400 µA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = -100 µA)	V_{OH2}	V_{CC}-0.7			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input pulse levels:	0.45V TO 2.4V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs
	0.8V and 2.0V for outpust
Output Load:	1 TTL gate and C_L =100pF



9

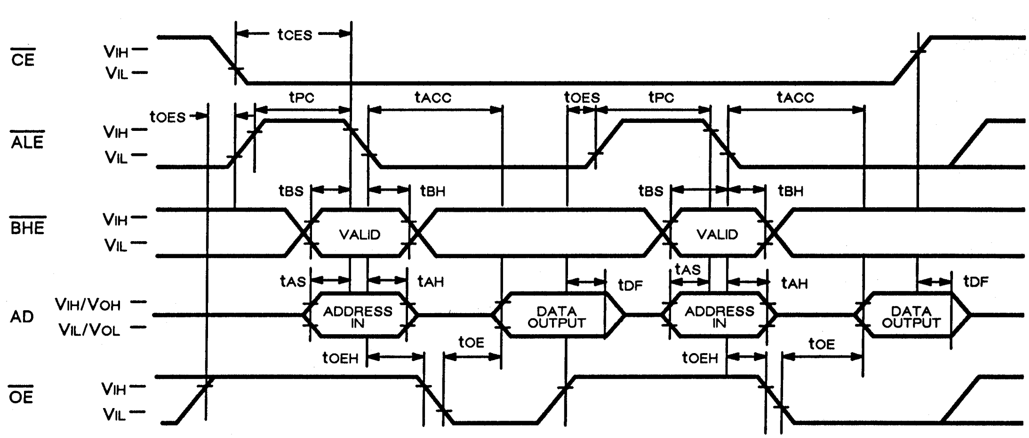
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C1028-15			MBM7C1028-20			MBM27C1028-25			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ALE Active to Output Valid ($\overline{CE}$=$\overline{OE}$=V_{IL}, $\overline{PGM}$=V_{IH})	t_{ACC}			150			200			250	ns
$\overline{ALE}$ Precharge Time ($\overline{CE}$=V_{IL})	t_{PC}	60			75			100			ns
$\overline{CE}$ Setup Time	t_{CES}	60			75			100			ns
Address Setup Time	t_{AS}	20			25			30			ns
Address Hold Time	t_{AH}	20			25			30			ns
$\overline{BHE}$ Setup Time	t_{BS}	20			25			30			ns
$\overline{BHE}$ Hold Time	t_{BH}	20			25			30			ns
$\overline{OE}$ Setup Time	t_{OES}	0			0			0			ns
$\overline{OE}$ Hold Time	t_{OEH}	20			25			30			ns
$\overline{OE}$ to Output Valid*1 ($\overline{PGM}$=V_{IH})	t_{OE}	0		70	0		70	0		100	ns
$\overline{PGM}$ to Output Valid*1 ($\overline{OE}$=V_{IL})	t_{PGM}	0		70	0		70	0		100	ns
Ooutput Disable to Output Float*3	t_{DF}	0		60	0		60	0		60	ns

NOTE: *1 $\overline{OE}$ ($\overline{PGM}$) may be delayed up to t_{ACC}−t_{OE}(t_{PGM}) after the falling edge of $\overline{ALE}$.
*2 t_{DF} is specified from $\overline{CE}$, $\overline{OE}$ or $\overline{PGM}$ or $\overline{ALE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

TYPICAL READ WAVEFORM



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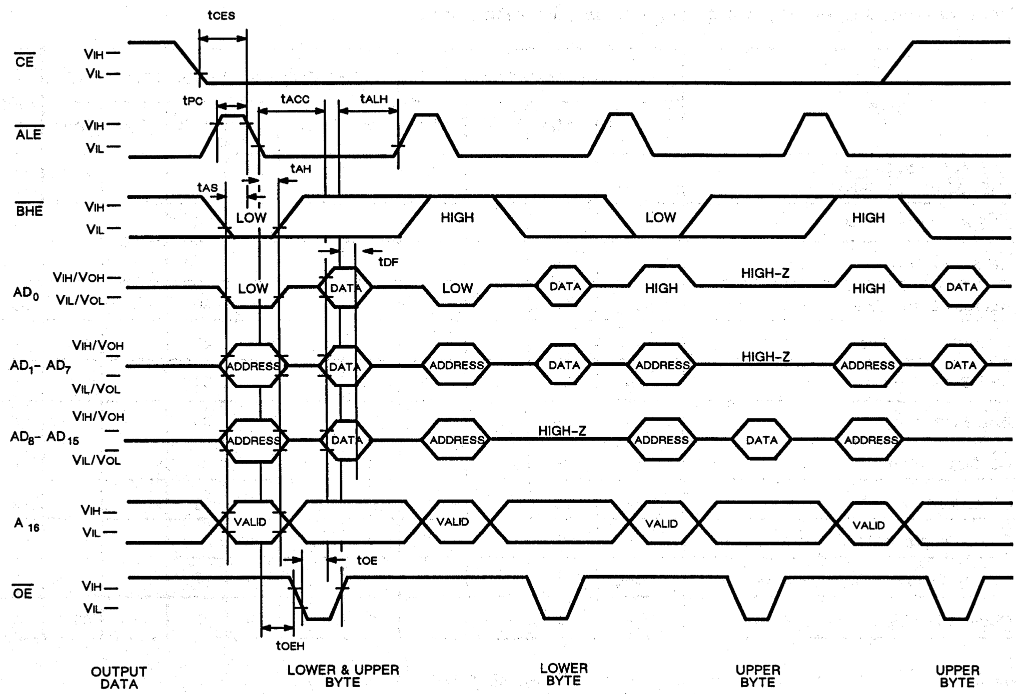
READ WAVEFORM



PROGRAMMING / ERASING INFORMATION

PROGRAMMING

When the MBM27C1028 is shipped the factory, all memory cells (1,048,576 bits) are set to High state (logic 1). During the programming procedure, affected bit cells are set to the Low state (logic 0).

The MBM27C1028 is programmed with a fast programming algorithm design by Fujitsu called Quick Pro™. When +12.5V(±0.3V) is applied to Vpp, +6V(±0.25V) is applied to Vcc, $\overline{CE}$ = VIL, $\overline{PGM}$ and $\overline{OE}$ = VIH, the programming mode is initiated. Next, the proper address in conjection with $\overline{BHE}$ are input by falling edge of $\overline{ALE}$, and the data pattern is applied to the input buffer (Figure1). When both address (and $\overline{BHE}$) and data are stable, a 0.5ms negative pulse is applied to the $\overline{PGM}$. Upon verification of written data read out by $\overline{OE}$ an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complate the programming of one byte. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Caution

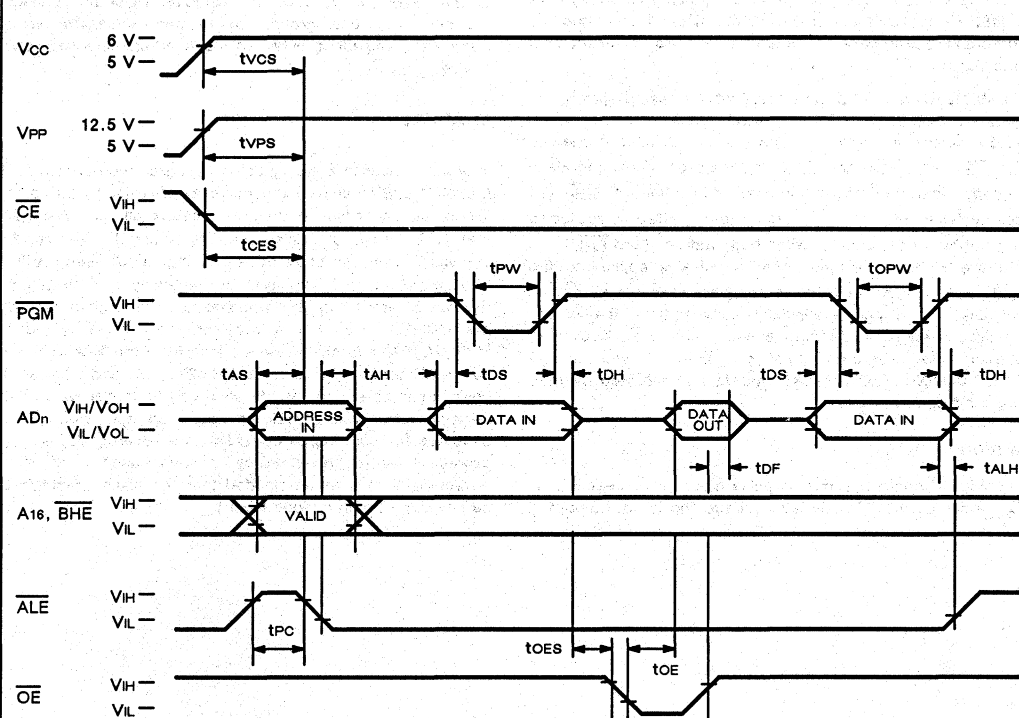
The width of one programming pulse must not exceed 40ms; thus, a continuous TTL low-level voltage should not be applied to the $\overline{PGM}$. Also, a 0.1µF capacitor must be connected between V_{PP} and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

ERASING

In order to clear all memory cells of programmed contents, the MBM27C1028 must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 15Wsec/cm^2 is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 253.7nm with an intensity of 12mW/cm^2. Remove all filters from the lamp and clean the transparent lid of the MBM27C1028 with a non-abrasive cleaner. Hold the MBM27C1028 approximately one inch from the light source for 15-to-21 mimute. (Note. The MBM27C1028 and other similar devices can be erased by light sources with longer wavelength: however, the erasing time is much greater. Nonetheless, exposure to fluorescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

PROGRAMMING / ERASING INFORMATION (Cont'd)

PROGRAMMING WAVEFORM



DC CHARACTERISTICS DURING PROGRAMMING

(T_A= 25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Input Low Level	V_{IL}	-0.1		0.8	V
Input Load Current	I_{LI}	-10		10	µA
V_{CC} Supply Current ($\overline{CE}$=V_{IH})	I_{SB3}			1	mA
V_{CC} Supply Current ($\overline{CE}$=V_{CC}± 0.3V)	I_{SB4}		1	100	µA
V_{PP} Supply Current ($\overline{CE}$=V_{IL})	I_{CC3}			30	mA
V_{PP} Supply Current ($\overline{CE}$=$\overline{PGM}$=V_{IL}, OE=V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{PGM}$=V_{IH})	I_{PP3}			5	mA
Output Low Level (I_{OL}=2.1mA)	V_{OL}			0.45	V
Output High Level (I_{OH}=-400 µA)	V_{OH}	2.4			V

AC CHARACTERISTICS DURING PROGRAMMING

(T_A= 25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{CC} Setup Time	t_{VCS}	4			µS
V_{PP} Setup Time	t_{VPS}	4			µS
$\overline{CE}$ Setup Time	t_{CES}	4			µS
Address Setup Time	t_{AS}	1			µS
Address Hold Time	t_{AH}	1			µS
$\overline{ALE}$ Precharge Time	t_{PC}	2			µS
$\overline{ALE}$ Low Hold Time	t_{ALH}	2			µS
Data Setup Time	t_{DS}	2			µS
Data Hold Time	t_{DH}	2			µS
$\overline{OE}$ Setup Time	t_{OES}	2			µS
$\overline{OE}$ to Output Valid	t_{OE}			100	ns
$\overline{OE}$ to Output Float	t_{DF}			60	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Over Programming Pulse Number	n	1		25	times

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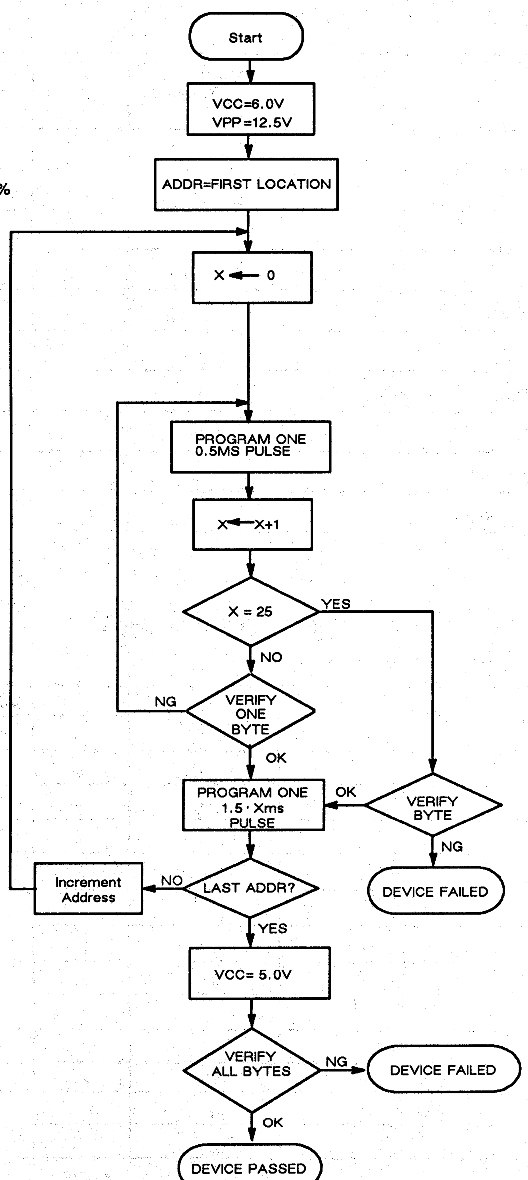
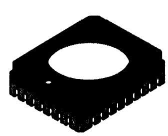
Fig. 3 — PROGRAMMING CHART

V_{CC}=6V ± 0.25V
V_{PP}=12.5V ± 0.3V
t_{PW}=0.5ms ± 5%
t_{OPN}=1.5xNms ± 5%

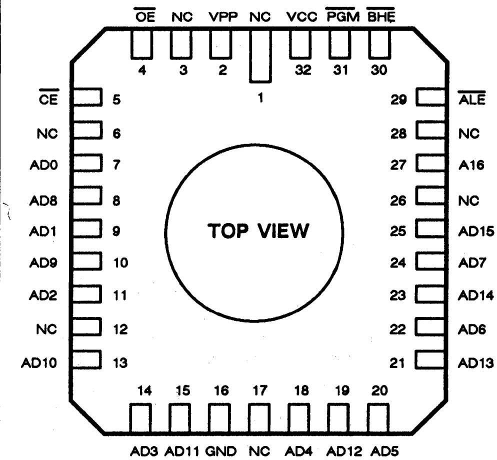


PACKAGE DIMENSIONS



LCC-32C-F01

PIN ASSIGNMENT



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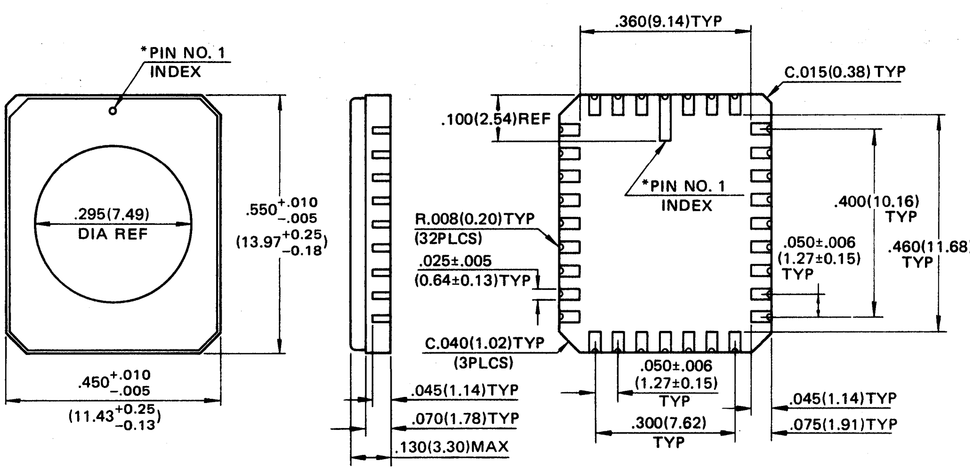
32-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(Case No.: LCC-32C-F01)

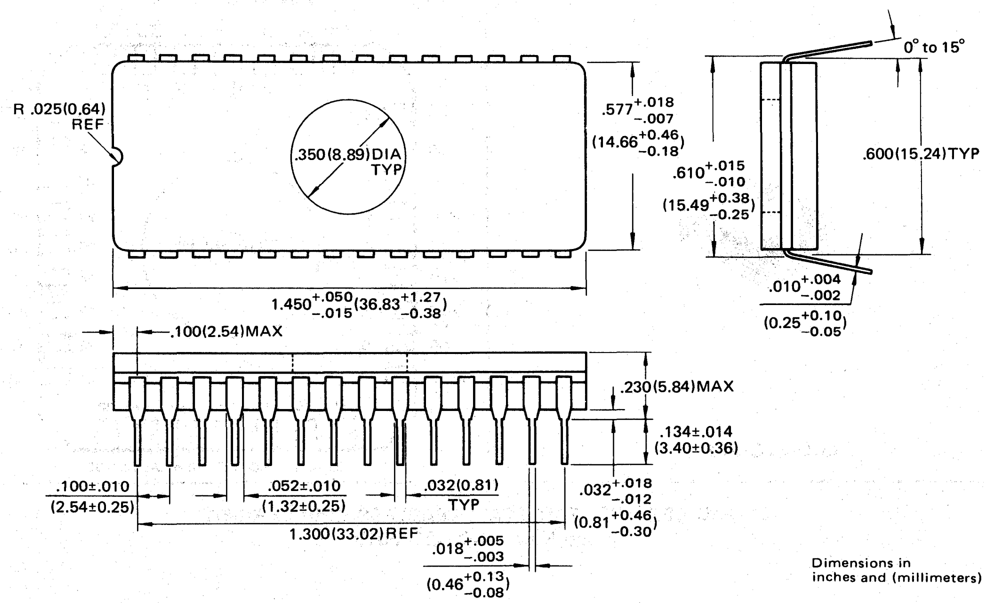


*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in inches and (millimeters)

PACKAGE DIMENSIONS

28-PIN CERAMIC DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-C01)



Section 10

CMOS One-Time PROMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options	Sealing Method
10-5	MBM27C128P-25	250	131072 bits (16384w x 8b)	28-pin Plastic DIP	Plastic
10-15	MBM27C256AP-25	250	262144 bits (32768w x 8b)	28-pin Plastic DIP	Plastic
10-25	MBM27C512P-25	250	524288 bits (65536w x 8b)	28-pin Plastic DIP	Plastic

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One–Time Programmable Handling Recommendation

To ensure the best results from a One–Time Programmable (OTP) ROM, Fujitsu suggests the following procedure:

1. Program device in accordance with data sheet specifications
2. Age device for 48 hours at 150 degrees centigrade
3. Verify programmed data (Vcc = 5.5V and 4.5V).

NOTE: Because One–Time Programmable ROMs are not erasable and therefore cannot be quality tested for programmming reliability, Fujitsu cannot quarantee 100% programming yield on OTP devices.

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FUJITSU

CMOS 131072-BIT ONE TIME PROM

MBM27C128P-25

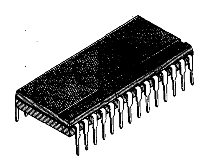
September 1987
Edition 1.0

CMOS 128K (131,072) BIT ONE TIME ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM27C128P is a high speed 131,072 bits CMOS one time electrically programmable read only memory (OTPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

The MBM27C128P is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells and housed in standard 28-pin plastic DIP package. It is organized as 16,384 words by 8 bits for use in microprocessor application. Single +5V operation greatly facilitates its use in systems.

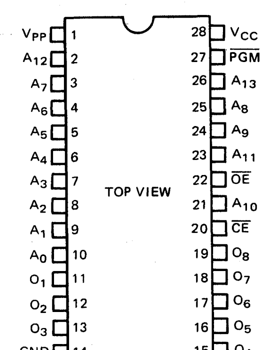
The MBM27C128P has the same functions including write operations as MBM27C128 (EPROM) except for erase.



PLASTIC PACKAGE
DIP-28P-M02

- CMOS power consumption
  Standby: 100μA max.
  Active: 30 mA max.
- 16,384 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- Programs with one 50 ms or 1 ms pulses
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
  Fast access time:
  250ns max. (MBM27C128P-25)
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Single +5V supply, ±10% tolerance
- Standard 28-pin Plastic DIP: (Suffix: -P)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

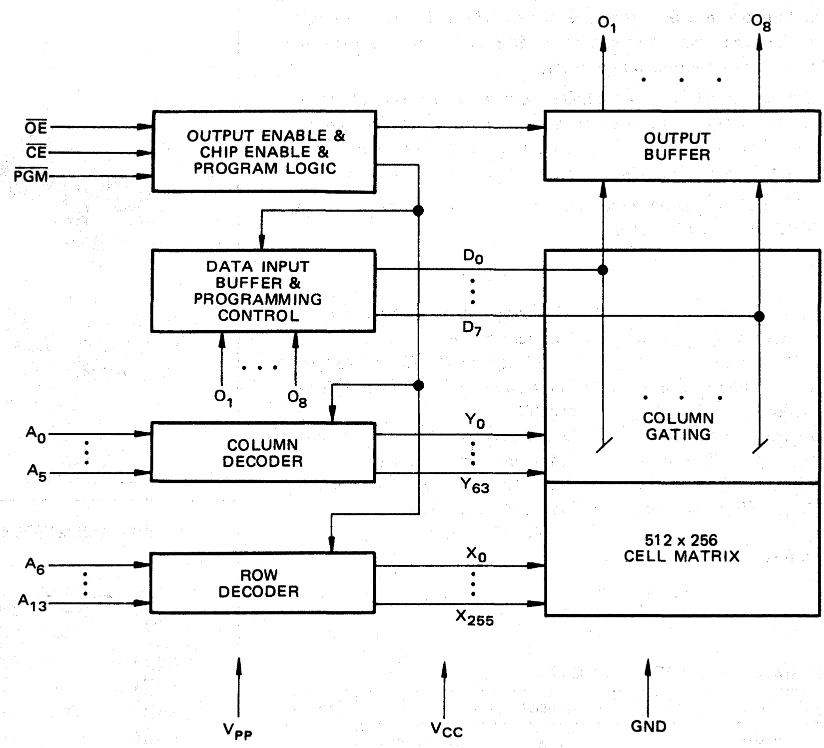
Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-45 to +125	°C
All Inputs/Outputs Voltage with respect to GND	V_{IN}, V_{OUT}	-0.6 to V_{CC}+0.6	V
Voltage on A_9 with Respect to GND	V_{A9}	-0.6 to +13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +22	V
Supply Voltage with respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Quick Pro™ is a trademark of FUJITSU LIMITED

Fig. 1 — MBM27C128P BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2 to 10, 21, 23 to 26)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
				Don't Care	V_{IL}			
Standby	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	GND

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Supply Voltage*1	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	$V_{CC}-0.6$		$V_{CC}+0.6$	V
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

Note: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Load Current (V_{IN} = 5.5V)	$\|I_{LI}\|$			10	μA
Output Leakage Current (V_{OUT} = 5.5V)	$\|I_{LO}\|$			10	μA
V_{PP} Supply Current	I_{PP1}		1	100	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{CE}$ = V_{CC}±0.3V, I_{OUT} = 0mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC1}		2	30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0mA)	I_{CC2}		4	30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = −100μA)	V_{OH2}	$V_{CC}-0.7$			V

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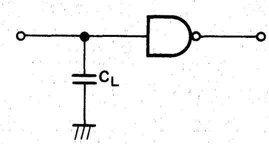
Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outpust
Output Load:	1 TTL gate and C_L = 100pF



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C128P-25			Units
		Min	Typ	Max	
Address Access Time*1	t_{ACC}			250	ns
$\overline{CE}$ to Output Delay	t_{CE}			250	ns
$\overline{OE}$ to Output Delay*1	t_{OE}			100	ns
Address to Output Hold	t_{OH}	0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

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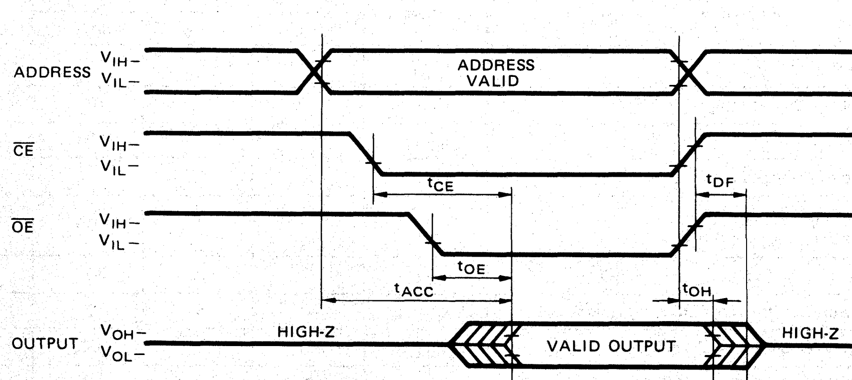
OPERATION TIMING DIAGRAM



PROGRAMMING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C128P has all 131,072 bits in the "1", or high, state. "0's" are loaded into the MBM27C128P through the procedure of programming.

Standard Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are both at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL low-level pulse is applied to the $\overline{PGM}$ input to accomplish the programming. the procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

Quick Programming

In addition to the standard 50 msec pulse width programming procedure, the MBM27C128P can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm utilizes a sequence of a 1ms pulse to program each location. The programming mode is entered when +21V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{PGM}$ and $\overline{OE}$ are V_{IH}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit patgterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of a 1 msec, TTL low-level pulse is applied to the $\overline{PGM}$ pin and after that additional pulse is applied to the $\overline{PGM}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flow chart.)

1) Input the start address (Address=G)
2) Set the V_{CC}=6V and V_{PP}=21V
3) Input data.
4) Compare the input data with FF. If data are FF, go to the step 11). If not, proceed the next step.
5) Clear the counter (X←0).
6) Apply ONE programming pulse to $\overline{PGM}$ pin (t_{PW} = 1ms Typ.).
7) Inclement the counter (X←X+1).
8) Compare the counter value with 20. If X=20, go to the step 10). If X<20, proceed the next step.
9) Verify the data. If the programmed data are the same as the input data, proceed the next step. If not, go back to the step 6).
10) Apply the additional programming pulse to the $\overline{PGM}$ pin (1ms x X or Xms x 1).
11) Compare the address with the end address. If the programmed address is the end address, proceed the next step. If not, go back to the step 3) for next address (G←G+1).
12) Verify the data. If the programmed data are not the same as the input data, the part is failed. If the programmed data the same as the input data, programming is at an end.

All that is required is that initial 1 msec program pulse and additional program pulse (21 msec Max.) be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 21 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

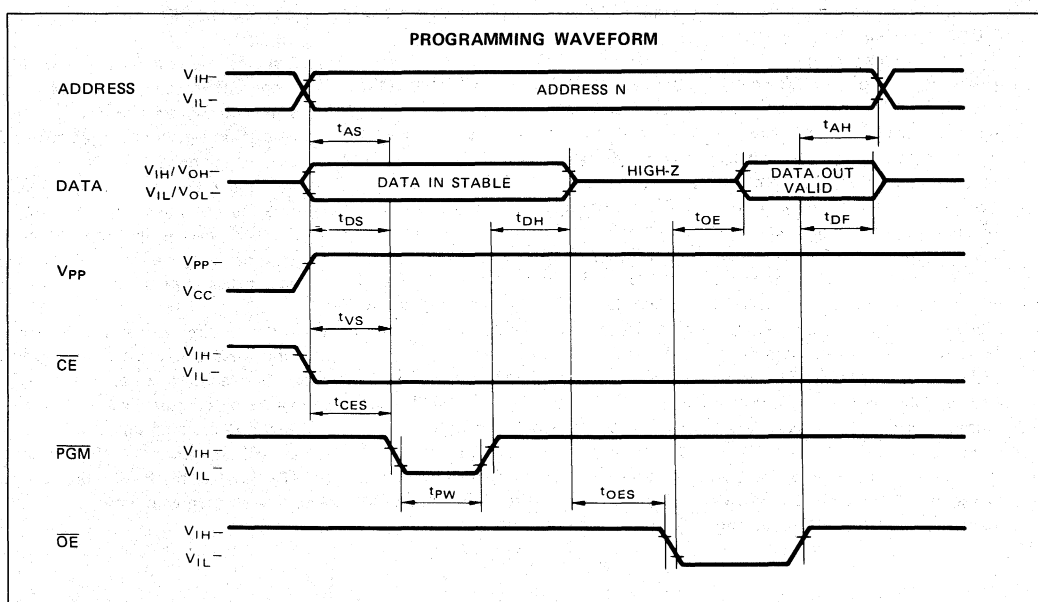
PROGRAMMING INFORMATION (continued)

ELECTRONIC SIGNATURE

The MBM27C128P has an electronic signature mode which can be intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.
The electronic signature is activated when +12V is applied to the address line A_9 (pin 24) of the MBM27C128P. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 through A_{13} must be hold at V_{IL} during the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Mnufacture
V_{IH}	1	0	0	0	0	1	0	1	Device

Note: $A_9 = 12V \pm 0.5V$
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.



1. Standard Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}^{*1} = 5V±5%, V_{PP}^{*2} = 21±0.5V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP2}			40	mA
V_{CC} Supply Current	I_{CC3}			30	mA
Input Low Level	V_{IL}	−0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$=$\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 to 21 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 5V±5%, V_{PP} = 21±0.5V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
$\overline{PGM}$ Pulse Width	t_{PW}	25	50	55	ms

PROGRAMMING INFORMATION (continued)

2. Quick Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}^{*1} = 6V±0.25V, V_{PP}^{*2} = 21V±0.5V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP2}			40	mA
V_{CC} Supply Current	I_{CC3}			30	mA
Input Low Level	V_{IL}	–0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = –400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occur the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 6 to 21 volts or vise-versa.

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AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V)

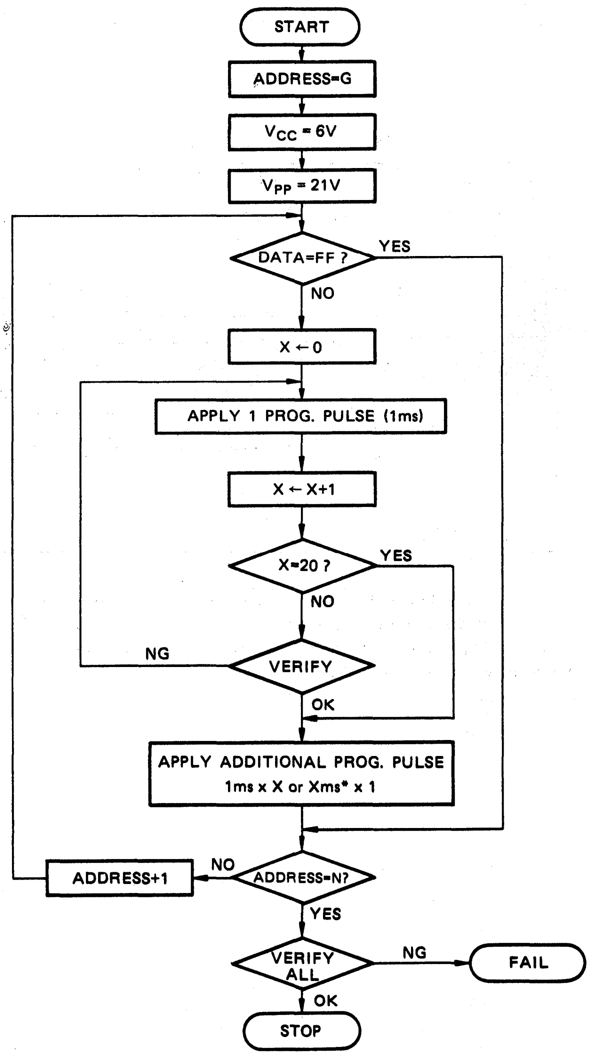
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
$\overline{PGM}$ Pulse Width	t_{PW}	0.95	1	1.05	ms

PROGRAMMING FLOW CHART FOR Quick Pro™

V_{CC} = 6V±0.25V
V_{PP} = 21V±0.5V

T_{PW} = 1ms±50μs
(* = Xms±5%)

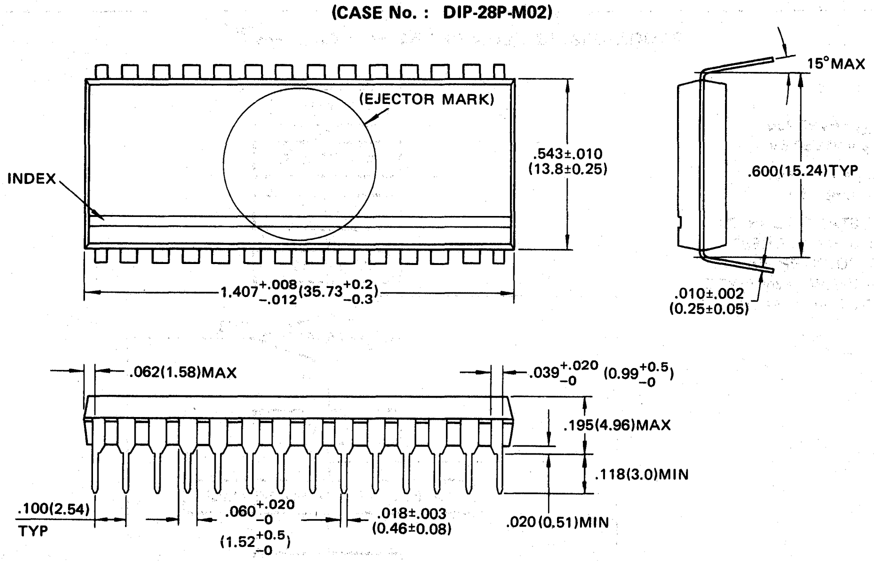
G : START ADDRESS
N : STOP ADDRESS
X : COUNTER VALUE
MAXIMUM 42ms/BYTE
MINIMUM 1.9ms/BYTE



PACKAGE DIMENSIONS

Standard 28-pin Plastic DIP (Suffix: -P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



Dimensions in inches (millimeters)

CMOS 262144-BIT ONE TIME PROM

MBM27C256AP-25

September 1987
Edition 1.0

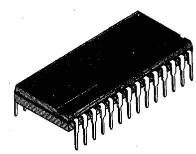
CMOS 256K (262,144) BIT ONE TIME ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

The Fujitsu MBM27C256AP is a high speed 262,144 bits CMOS one time electrically programmable read only memory (OTPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

The MBM27C256AP is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells and housed in standard 28-pin plastic DIP package. It is organized as 32,768 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

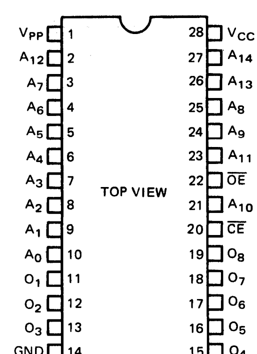
The MBM27C256AP has the same functions including write operations as MBM27C256A (EPROM) except for erase.



PLASTIC PACKAGE
DIP-28P-M02

- CMOS power consumption
  Standby: 100 μA max.
  Active: 30mA max.
- 32,768 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ algorithm
- Programming voltage: 12.5V
- No clocks required (fully static operation)
- Fast access time:
  250 ns max. (MBM27C256AP-25)
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Single +5V supply, ±10% tolerance
- Standard 28-pin plastic
  DIP: (Suffix: -P)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

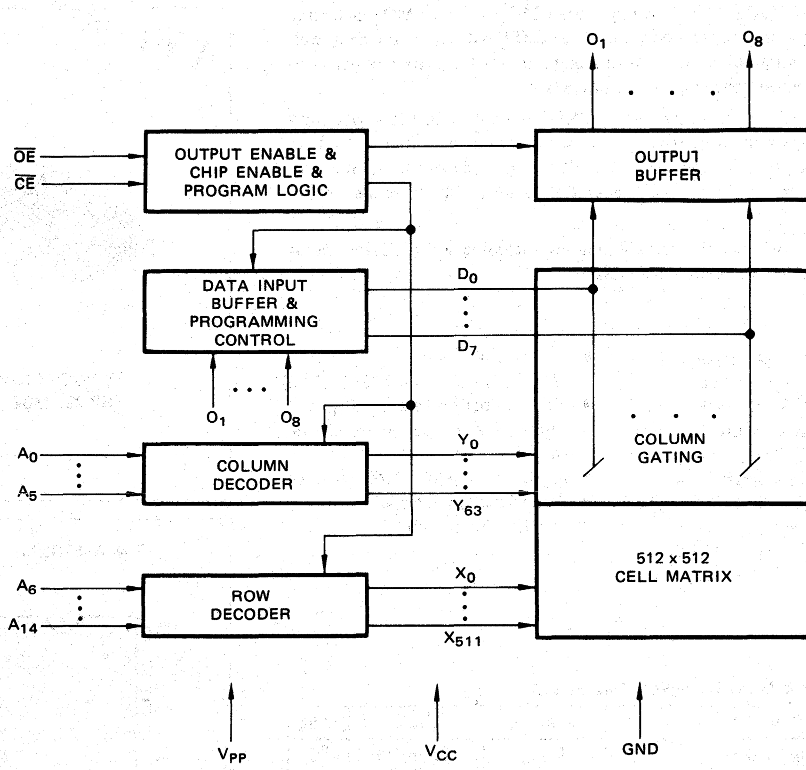
Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-45 to +125	°C
All Inputs/Outputs Voltage with respect to GND	V_{IN}, V_{OUT}	-0.6 to +7	V
Voltage on A_9 with respect to GND	V_{A9}	-0.6 to +13.5	V
V_{PP} Voltage with respect to GND	V_{PP}	-0.6 to +14	V
Supply Voltage with respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Quick Pro™ is a trademark of FUJITSU LIMITED

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MBM27C256AP BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2 ~ 10, 21, 23, 25 ~ 27)	A_9 (24)	Data I/O (11 ~ 13, 15 ~ 19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5 V	+5 V	GND
Output Disable	A_{IN}	A_{IN}	High-Z	V_{IL}	V_{IH}	+5 V	+5 V	GND
Standby	Don't Care	Don't Care	High-Z	V_{IH}	Don't Care	+5 V	+5 V	GND
Program	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	+6 V	+12.5 V	GND
Program Verify	A_{IN}	A_{IN}	D_{OUT}	Don't Care	V_{IL}	+6 V	+12.5 V	GND
Program Inhibit	Don't Care	Don't Care	High-Z	V_{IH}	V_{IH}	+6 V	+12.5 V	GND
Electronic Signature	A_{IN}	+12 V	Code	V_{IL}	V_{IL}	+5 V	+5 V	GND

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	V
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

Note: *V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

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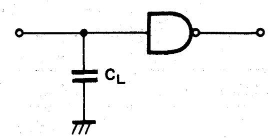
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5 V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.5 V)	I_{LO}			10	μA
V_{PP} Supply Current ($V_{PP} = V_{CC} \pm 0.6$ V)	I_{PP}		1	100	μA
V_{CC} Standby Current ($\overline{CE} = V_{IH}$)	I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{CE} = V_{CC} \pm 0.3$ V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}=V_{IL}$)	I_{CC1}			30	mA
V_{CC} Operation Current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}			30	mA
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = –400 μA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = –100 μA)	V_{OH2}	V_{CC}-0.7			V

Fig. 2 – AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.45 V to 2.4 V
Input Rise and Fall Times:	≦20 ns
Timing Measurement Reference Levels:	1.0 V and 2.0 V for inputs
	0.8 V and 2.0 V for outputs
Output Load:	1 TTL gate and C_L = 100 pF



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C256AP-25			Units
		Min	Typ	Max	
Address Access Time[*1] ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{ACC}			250	ns
$\overline{CE}$ to Output Delay ($\overline{OE}$ = V_{IL})	t_{CE}			250	ns
$\overline{OE}$ to Output Delay[*1] ($\overline{CE}$ = V_{IL})	t_{OE}			100	ns
Address to Output Hold	t_{OH}	0			ns
Output Enable High to Output Float[*2]	t_{DF}	0		60	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the folling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Floating is defined as the point where data is no longer driven.

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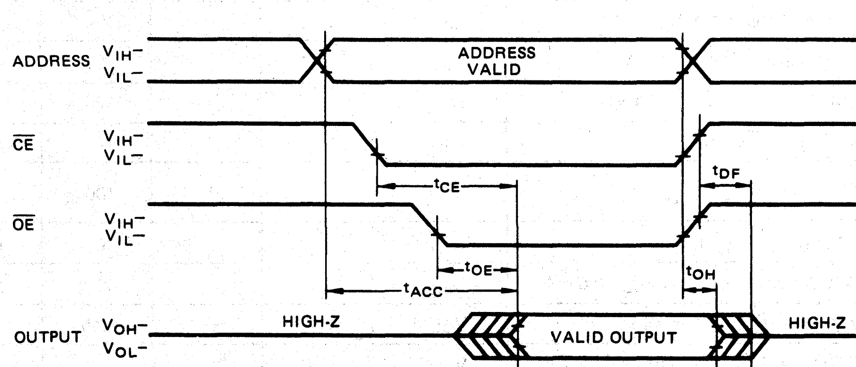
OPERATION TIMING DIAGRAM



PROGRAMMING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C256AP has all 262,144 bits in the "1", or high state. "0's" are loaded into the MBM27C256AP through the procedure of programming.

The MBM27C256AP is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{CE}$ and $\overline{OE}$ are V_{IH}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1ms programming pulse is applied to $\overline{CE}$ and after that one additional pulse which is 3 times as wide as previous pulse is applied to $\overline{CE}$ to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{CE}$ = V_{IH}.
3) Clear the programming pulse counter (X ← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1ms Typ.) to $\overline{CE}$.
6) Increment the counter (X ← X+1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X = 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G ← G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

ELECTRONIC SIGNATURE

The MBM27C256AP has electronic signature mode which is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM27C256AP. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be hold at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	0	1	0	0	x	1	1	0	Device

Note: A_9 = 12V±0.5V
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
A_{14} = Either V_{IL} or V_{IH}

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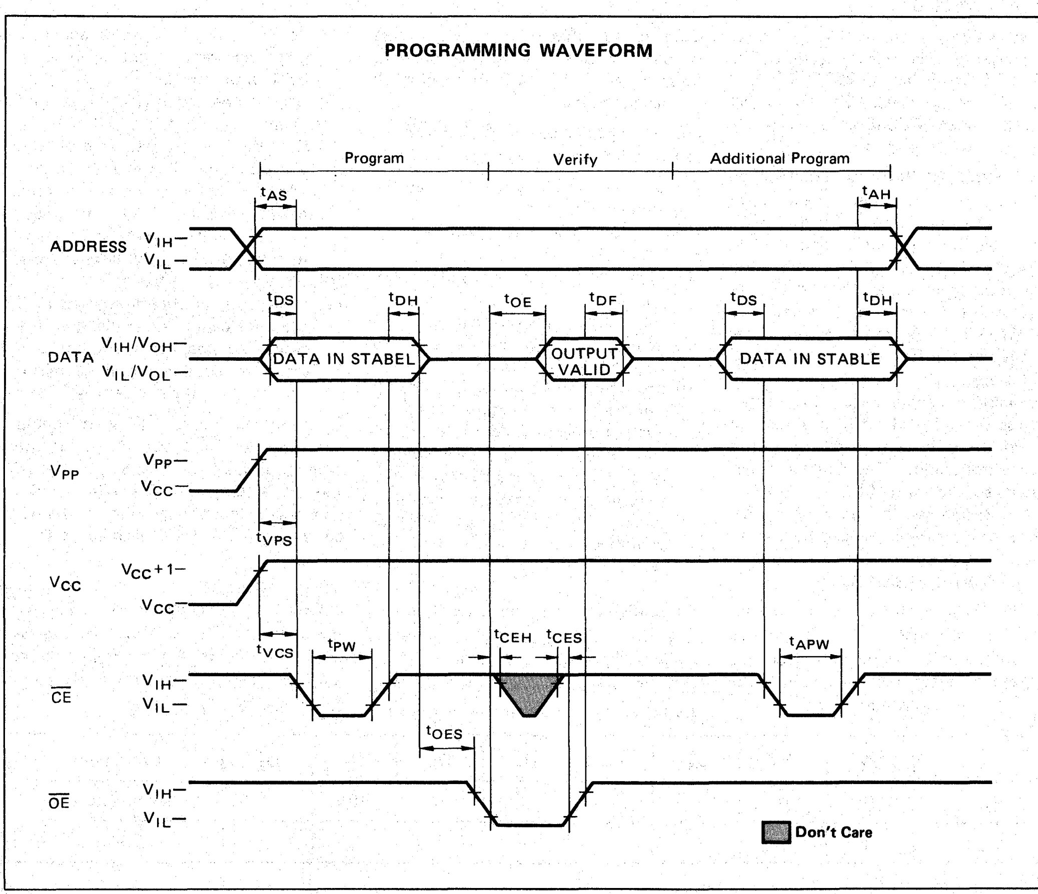
PROGRAMMING INFORMATION (Cont'd)



DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}*1 = 6V±0.25V, V_{PP}*2 = 12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{IL}			10	μA
V_{PP} Supply Current ($\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{OE}$ = V_{IL})	I_{PP3}			5	mA
V_{CC} Supply Current	I_{CC}			100	mA
Input Low Level	V_{IL}	–0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = –400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

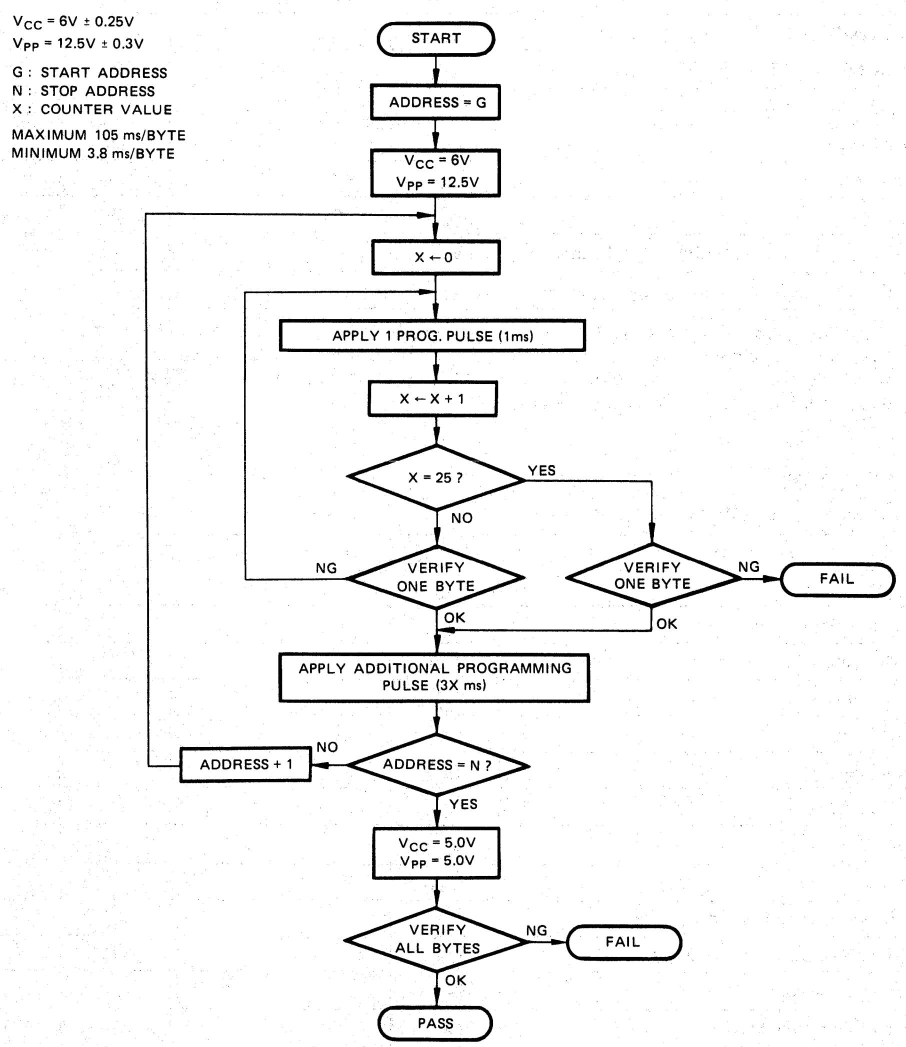
AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VPS}	2			μs
V_{CC} Setup Time	t_{VCS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Chip Enable Hold Time	t_{CEH}	2			μs
Output Enblea to Output Valid	t_{OE}			120	ns
Output Disable to Output Float Delay	t_{DF}			105	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Programming Pulse Number	x	1		25	times
Additional Programming Pulse Width	t_{APW}	2.85		78.75	ms

PROGRAMMING INFORMATION (Cont'd)

PROGRAMMING FLOW CHART FOR Quick Pro™



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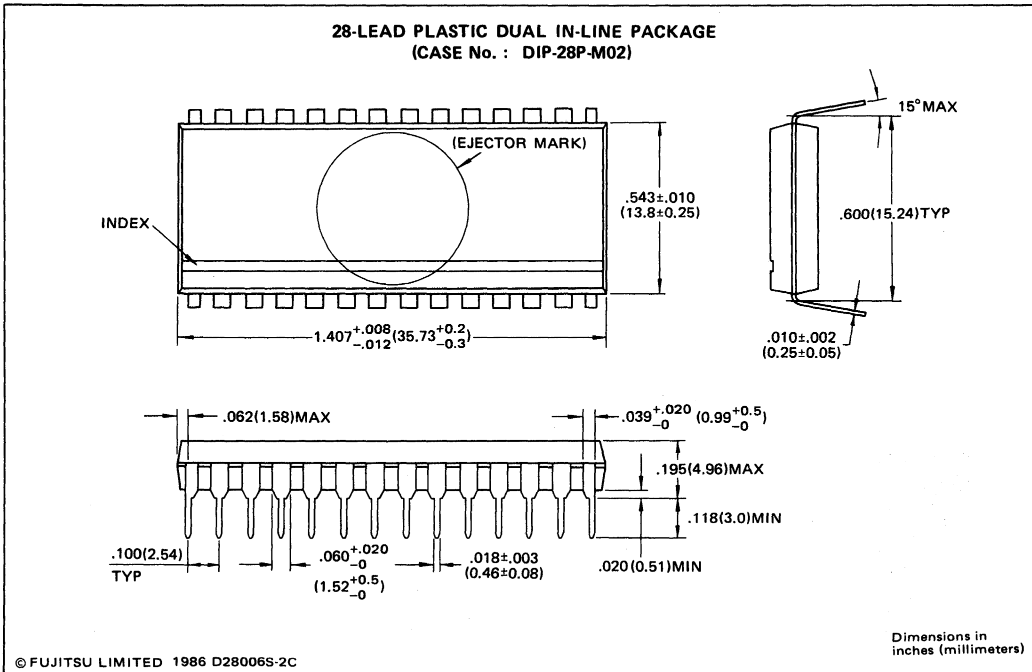
PACKAGE DIMENSIONS

Standard 28-pin Plastic DIP (Suffix: -P)



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FUJITSU

CMOS 524288-BIT ONE TIME PROM

MBM27C512P-25

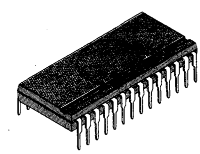
September 1987
Edition 1.0

CMOS 512K (524,288) BIT ONE TIME ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM27C512P is a high speed 524,288 bits CMOS one time electrically programmable read only memory (OTPROM). It is especailly well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

The MBM27C512P is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells and housed in standard 28-pin plastic DIP package. It is organized as 65,536 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

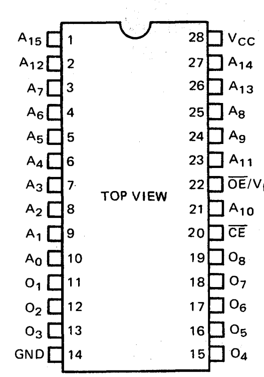
The MBM27C512P has the same functions including write operations as MBM27C512 (EPROM) except for erase.



PLASTIC PACKAGE
DIP-28P-M02

- CMOS power consumption
  Standby: 100 μA max.
  Active: 30mA max.
- 65,536 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
- Fast access time:
  250 ns max. (MBM27C512P-25)
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Single +5V supply, ±10% tolerance
- Standard 28-pin plastic DIP: (Suffix: -P)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	–25 to +85	°C
Storage Temperature	T_{STG}	–45 to +125	°C
All Inputs/Outputs Voltage with respect to GND	V_{IN}, V_{OUT}	–0.6 to V_{CC}+0.6	V
Voltage on A_9 with Respect to GND	V_{A9}	–0.6 to +13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	–0.6 to +22	V
Supply Voltage with respect to GND	V_{CC}	–0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Quick Pro™ is a trademark of FUJITSU LIMITED

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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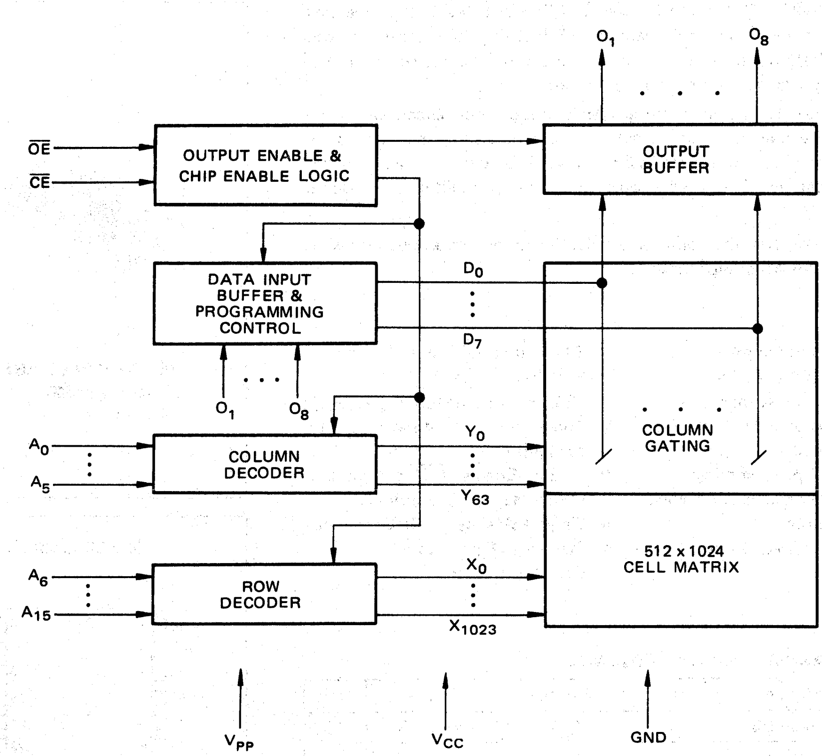
Fig. 1 — MBM27C512P BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0 V, except $\overline{OE}/V_{PP}$)	C_{IN1}	–	4	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance (V_{IN} = 0 V)	C_{IN2}	–	–	20	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}	–	8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (1~10, 21, 23~27)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	5V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	5V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	5V	GND
Program	A_{IN}	D_{IN}	V_{IL}	12.5V	6V	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	6V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	12.5V	6V	GND

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

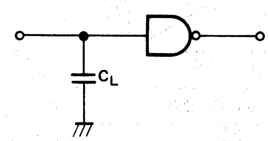
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Load Current (V_{IN} = 5.5 V)	$\|I_{LI}\|$			10	μA
Output Leakage Current (V_{OUT} = 5.5 V)	$\|I_{LO}\|$			10	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{CE}$ = V_{CC} ±0.3 V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA)	I_{CC1}		4	30	mA
V_{CC} Operation Current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}		10	30	mA
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = -400 μA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = -100 μA)	V_{OH2}	V_{CC} -0.7			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤ 20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C512P-25			Units
		Min	Typ	Max	
Address Access Time*1	t_{ACC}			250	ns
$\overline{CE}$ to Output Delay	t_{CE}			250	ns
$\overline{OE}$ to Output Delay*1	t_{OE}			100	ns
Address to Output Hold	t_{OH}	0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

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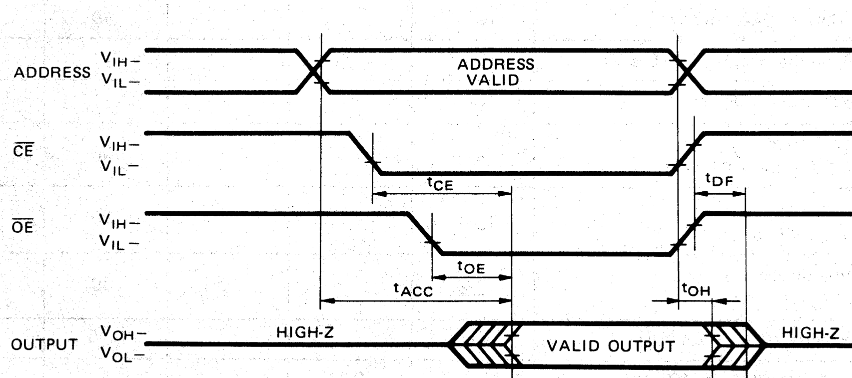
OPERATION TIMING DIAGRAM



PROGRAMMING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C512P has all 524,288 bits in the "1", or high state. "0's" are loaded into the MBM27C512P through the procedure of programming.

The MBM27C512P is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{CE}$ is V_{IH}. A 0.1µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 ms programming pulse is applied to $\overline{CE}$ and after that one additional pulse which is 3 times as wide as previous pulse is applied to $\overline{CE}$ to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{CE}$ = V_{IH}.
3) Clear the programming pulse counter (X ← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1ms Typ.) to $\overline{CE}$.
6) Increment the counter (X ← X+1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X < 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G ← G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V and V_{CC} = 6V) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

ELECTRONIC SIGNATURE

The MBM27C512P has electronic signature mode which is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM27C512P. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be hold at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	1	1	0	0	0	1	1	1	Device

Note: A_9 = 12V ± 0.5V
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
A_{14} = A_{15} = Either V_{IL} or V_{IH}

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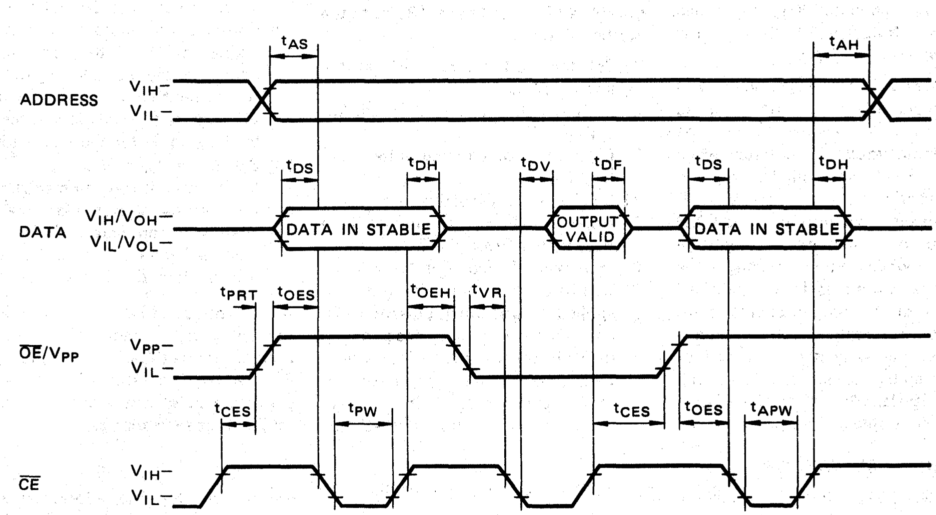
PROGRAMMING INFORMATION (Cont'd)

PROGRAMMING WAVEFORM



DC CHARACTERISTICS
(T_A = 25±5°C, V_{CC}^{*1} = 6V ± 0.25V, V_{PP}^{*2} = 12.5V±0.3V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Leakage Current (V_{IN} = 5.25 V/0.45 V)	$\|I_{LI}\|$			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = V_{IL})	I_{PP}			50	mA
V_{CC} Supply Current	I_{CC}			30	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400 μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from 5 to 12.5 volts or vice-versa.

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PROGRAMMING INFORMATION (Cont'd)

AC CHARACTERISTICS
(T_A = 25±5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{DS}	2			µs
V_{CC} Setup Time	t_{VS}	2			µs
Address Hold Time	t_{AH}	2			µs
Data Hold Time	t_{DH}	2			µs
Output Enable Hold Time	t_{OEH}	2			µs
V_{PP} Recovery Time	t_{VR}	2			µs
Chip Enable to Data Valid	t_{DV}			1	µs
Output Disable to Output Float Delay	t_{DF}	0		130	ns
V_{PP} Program Pulse Rise Time	t_{PRT}	50			ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Additional Programming Pulse Width	t_{APW}	2.85	3	78.75	ms

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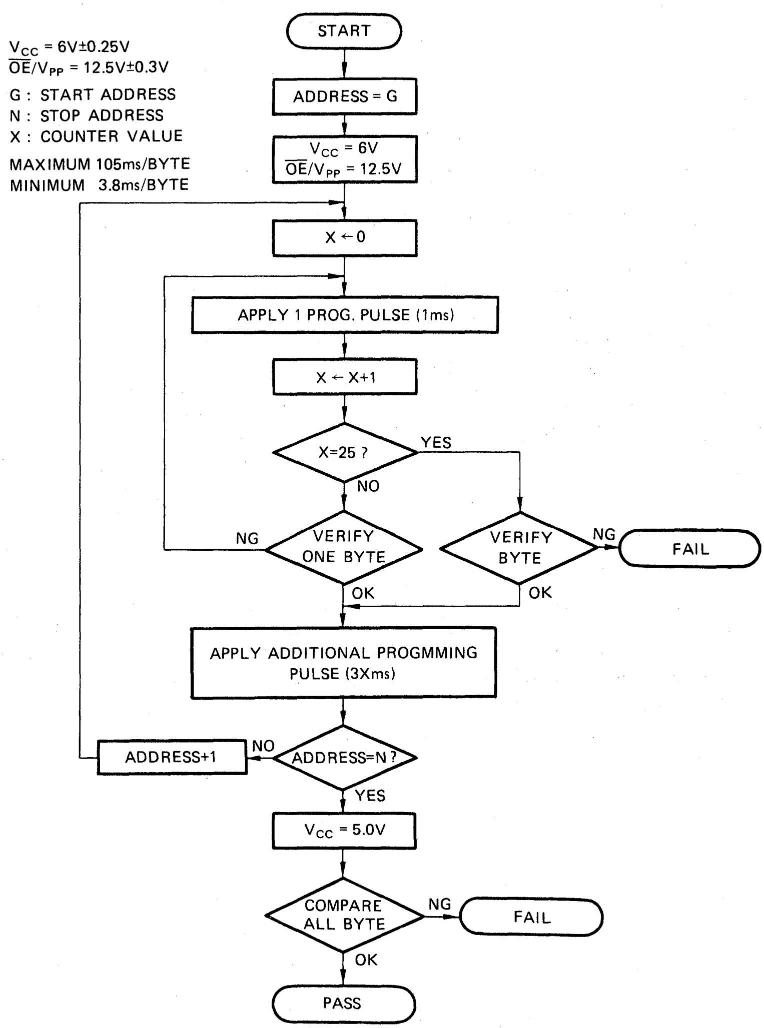
PROGRAMMING FLOW CHART



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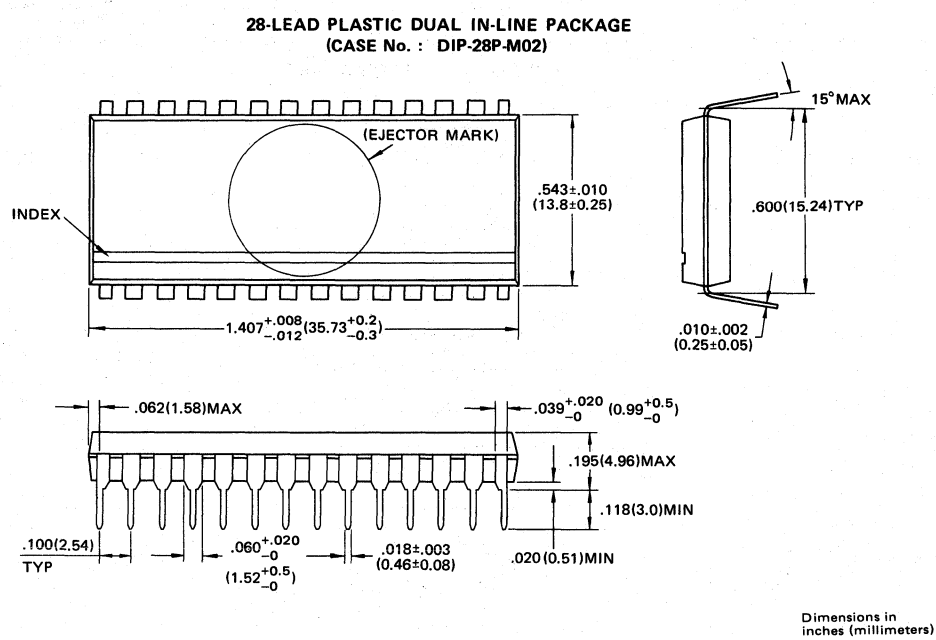
PACKAGE DIMENSIONS

Standard 28-pin Plastic DIP (Suffix: -P)



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Section 11

CMOS EEPROMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options	Sealing Method
11-3	MBM28C64-25	250	65536 bits	28-pin Plastic DIP	Plastic
	MBM28C64-35	350	(8192w x 8b)	28-pin Ceramic DIP	CERDIP
11-11	MBM28C65-25	250	65536 bits	28-pin Plastic DIP	Plastic
	MBM28C65-35	350		28-pin Ceramic DIP	CERDIP
11-19	MBM28C256	150	262144 bits (32768w x 8b)	28-pin Plastic DIP	Plastic

11

11

FUJITSU

CMOS 65536-BIT ELECTRICALLY ERASABLE PROGRAMMABLE ROM

MBM28C64-25
MBM28C64-35

September 1987
Edition 2.0

PRELIMINARY

CMOS 8192 x 8 ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY

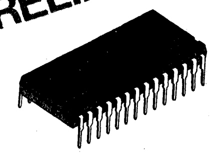
The Fujitsu MBM 28C64 is a high speed 65,536 bits CMOS electrically erasable and electrically programmable read only memory (EEPROM) using a single 5 V supply. It is especailly well suited not only for application where rapid turn-around. and/or bit pattern experimentation and low-power consumption are important but also as replacement of battery-backed-up RAM application.

The MBM 28C64's write operation is similar to that of a Static RAM. Byte write operation is initiated with a TTL low level signal to the $\overline{WE}$ pin, and addresses and data which are internally latched allow the system to do for other tasks during the write operation.

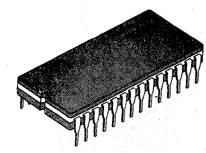
The MBM 28C64 automatically erases the memory bit pattern previously written and then completes writing/verifying a new pattern.
It also has a good $\overline{DATA}$ Polling function to make the processor realized the completion of write operation by data bus line.

The MBM 28C64 is fabricated using CMOS double polysilicon gate technology with stacked gate cells and housed in standard 28-pin DIP package.

- 8,192 words x 8 bit, fully decoded
- Internally latched address/data in writing
- Automatic Erase before Write
- Self timed Byte Write
- Data protection from short write pulse or noise on $\overline{WE}$
- On chip data verification
- Chip Erase capability using external power supply.
- Write status identificator
  $\overline{DATA}$ POLLING
- Lower power
  Active: 110 mW/MHz max.
  Standby: 550μW max.
- Single +5V supply, ±10% tolerance
- Access time
  250 ns max. (MBM 28C64-25)
  350 ns max. (MBM 28C64-35)
- TTL compatible input/output for fully MPU interface
- Tri-state output for wired-OR capability
- Output enable ($\overline{OE}$) for simple memory expansion
- Minimum Endurance of 10000 Erase/Write cycle per Byte
- JEDEC approved pin assignment and package
- Standard 28 pin CERAMIC (CERDIP) package: Suffix: -Z
- Standard 28 pin PLASTIC DIP package: Suffix: -P



PLASTIC PACKAGE
DIP-28P-M02



CERAMIC PACKAGE
DIP-28C-C02

PIN ASSIGNMENT

TOP VIEW

1	NC	28	V_{CC}
2	A_{12}	27	$\overline{WE}$
3	A_7	26	NC
4	A_6	25	A_8
5	A_5	24	A_9
6	A_4	23	A_{11}
7	A_3	22	$\overline{OE}$
8	A_2	21	A_{10}
9	A_1	20	$\overline{CE}$
10	A_0	19	I/O_8
11	I/O_1	18	I/O_7
12	I/O_2	17	I/O_6
13	I/O_3	16	I/O_5
14	GND	15	I/O_4

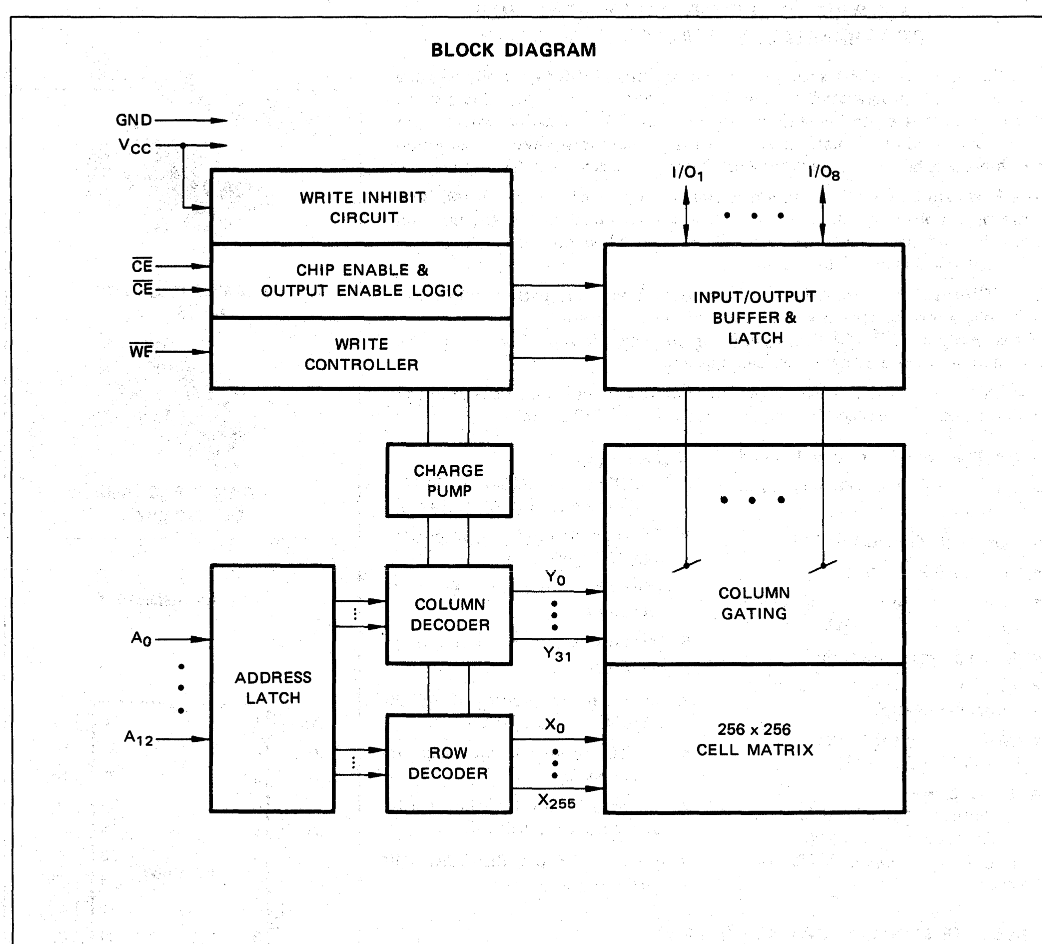
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage with Respect to GND		V_{CC}	−0.3 to +7.0	V
All Input/output Voltage with Respect to GND		V_{IN}, V_{OUT}	−0.3 to V_{CC}+0.3	V
Voltag on A_9 with Respect to GND		V_{A9}	−0.3 to +13.5	V
Voltage on $\overline{OE}$ with Respect to GND		V_{OE}	−0.3 to +15.5	V
Temperature under Bias		T_{BIAS}	−25 to +85	°C
Storage Temperature	Ceramic	T_{STG}	−65 to +125	°C
	Plastic		−45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

11



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CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance (V_{IN} = 0V)	C_{IN}			10	pF
Output Pin Capacitance (V_{OUT} = 0V)	C_{OUT}			10	pF

FUNCTION TRUTH TABLE

Mode \ Pin Name	Address	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Data I/O	Power
Read	A_{IN}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and Write Inhibit	X	V_{IH}	X	X	High-Z	Standby
Write	A_{IN}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Write
DATA POLLING*	A_{IN}	V_{IL}	V_{IL}	V_{IH}	$I/O_8 = \overline{I_8}$ I/O_1 to I/O_7 = High-Z	Write
Write Inhibit	A_{IN}	X	V_{IL}	X	High-Z	Active
			X	V_{IH}		
Chip Erase	X	V_{IL}	V_{OE}	V_{IL}	V_{IH}	Chip Erase

Note: X Can be either V_{IL} or V_{IH}.
V_{OE} 13.5V ± 1.5V
* The address must be applied the written address and the all output data becomes input data from the point where the write mode is completed.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max.	Unit
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

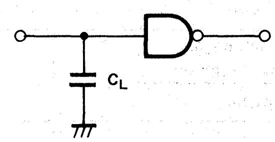
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = 5.5V	I_{LI}	−10	10	μA
Output Leakage Current	V_{OUT} = 5.5V	I_{LO}	−10	10	μA
V_{CC} Standby Current	$\overline{CE} = V_{IH}$	I_{SB1}		1	mA
V_{CC} Standby Current	$\overline{CE} = V_{CC}$±0.3V	I_{SB2}		100	μA
V_{CC} Active Current	$\overline{CE} = V_{IL}$	I_{CC1}		20	mA
V_{CC} Active Current	$\overline{CE} = V_{IL}$, f = 4MHz, I_{OUT} = 0mA	I_{CC2}		20	mA
V_{CC} Write Current	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$	I_{CCW}		40	mA
V_{CC} Chip Erase Current	$\overline{CE} = \overline{WE} = V_{IL}$, $\overline{OE} = V_{OE}$	I_{CCE}		100	mA
Output Low Level	I_{OL} = 2.1mA	V_{OL}		0.45	V
Output High Level	I_{OH} = −400μA	V_{OH}	2.4		V
Write Inhibit V_{CC} Level		V_{INH}		3	V
Chip Erase Voltage		V_{OE}	12	15	V

AC TEST CONDITIONS

Input pulse levels:	0.45V to 2.4V
Input Rise/Fall Times:	$\leqq$ 20ns
Input Reference Levels:	1.0V to 2.0V
Output Reference Levels:	0.8V to 2.0V
Output Load:	1 TTL gate and C_L = 100pF



AC CHARACTERISTICS (READ)

(Recommended operating conditions unless otherwise noted.)

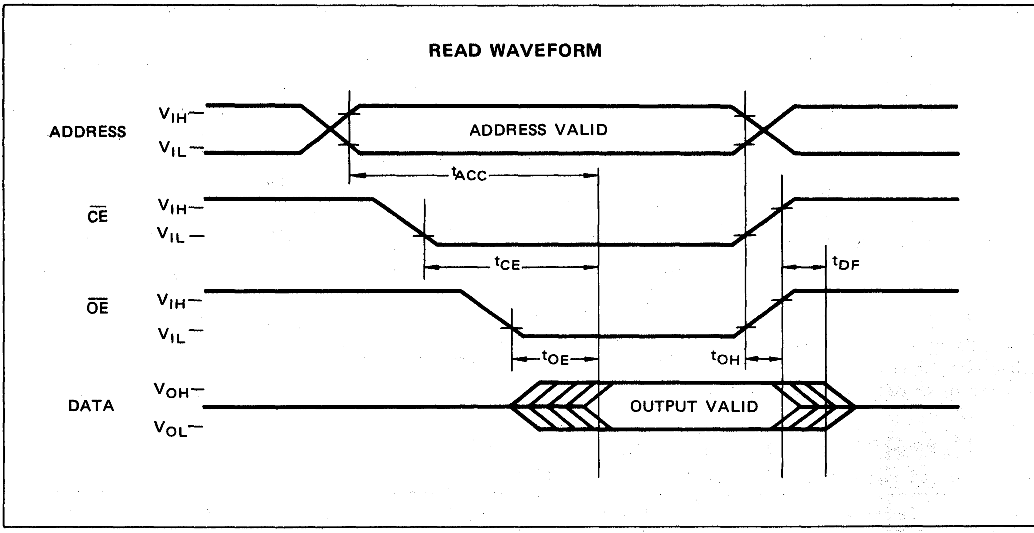
Parameter	Symbol	MBM 28C64-25		MBM 28C64-35		Unit
		Min	Max	Min	Max	
Address Access Time	t_{ACC}		250		350	ns
$\overline{CE}$ to Output Delay	t_{CE}		250		350	ns
$\overline{OE}$ to Output Delay*1	t_{OE}		100		120	ns
$\overline{OE}$ High to Output	t_{OH}	0		0		ns
$\overline{CE}$, $\overline{OE}$ High to Output Float*2	t_{DF}		60		80	ns

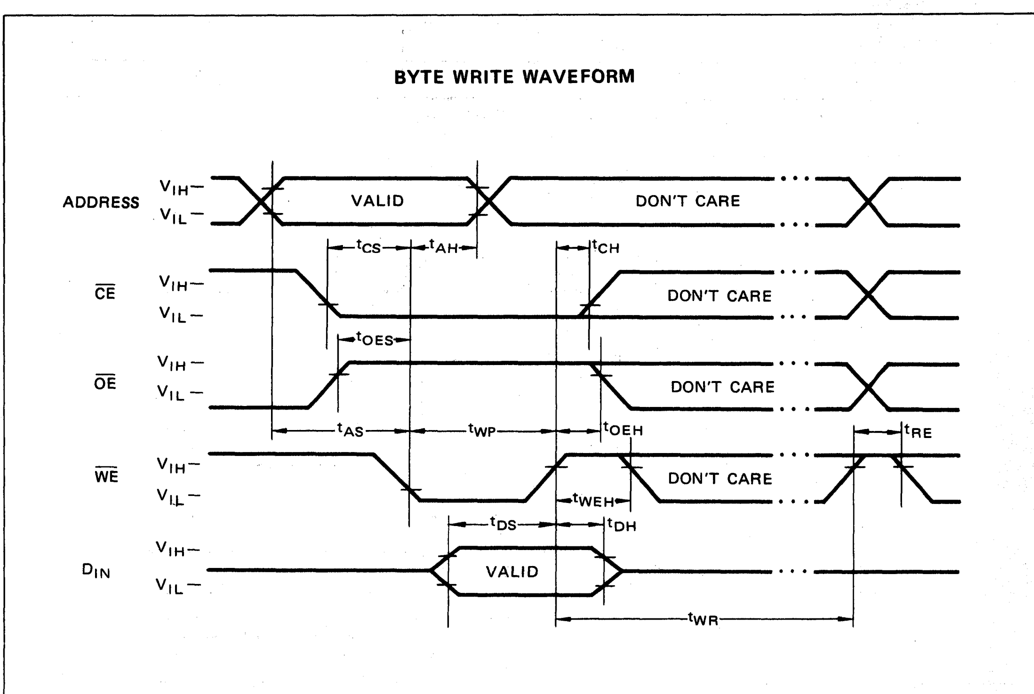
Note: *1 t_{OE} delays up t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

AC CHARACTERISTICS (BYTE WRITE)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	20			ns
Chip Enable Setup Time	t_{CS}	0			ns
Output Enable Setup Time	t_{OES}	20			ns
Write Pulse Width	t_{WP}	100			ns
Address Hold Time	t_{AH}	50			ns
Data Setup Time	t_{DS}	50			ns
Data Hold Time	t_{DH}	20			ns
Chip Enable Hold Time	t_{CH}	0			ns
Output Enable Hold Time	t_{OEH}	20			ns
Write Enable hold Time	t_{WEH}	10			ns
Byte Write Cycle Time	t_{WR}			10	ms
Write Recovery Time	t_{RE}	50			ns
Number of Write per Byte	n	10			x1000


READ WAVEFORM
ADDRESS
VIH
VIL
ADDRESS VALID
tACC
CE
tCE
tDF
OE
tOE
tOH
DATA
VOH
VOL
OUTPUT VALID


BYTE WRITE WAVEFORM
ADDRESS
VIH
VIL
VALID
DON'T CARE
tCS
tAH
tCH
CE
DON'T CARE
tOES
OE
DON'T CARE
tAS
tWP
tOEH
tRE
WE
DON'T CARE
tWEH
tDS
tDH
DIN
VALID
tWR

WRITE INFORMATION

BYTE WRITE

The MBM 28C64's write mode is similar to that of Static RAM. The write cycle is completely self-timed, and initiated by a low going TTL pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address data is latched. On the rising edge, the input data is latched. During the write cycle, the MBM 28C64 automatically erases the memory data previously written and new data written into the memory is verified to ensure successufully the byte write.

CHIP ERASE

The MBM 28C64 has a chip erase mode using external power supply which all data can be written to high state (= the erased state). The chip erase mode is initiated by setting $\overline{OE}$ to 13.5V and applying low TTL level to $\overline{WE}$ while holding all data inputs on high TTL level.

$\overline{DATA}$ POLLING

The MBM 28C64 features $\overline{DATA}$ Polling to signal the completion of a byte write cycle. During a write cycle, an attemped read of the last byte written results in the data complement of that byte at I/O_8. After completion of the write cycle, true data is available.

$\overline{DATA}$ Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

DATA PROTECTION

The MBM 28C64 has three features to prevent a erroneous initiation of write mode.

V_{CC} Detecter: When the V_{CC} is less than +3V during V_{CC} power-on and power-off, the write function is inhibited.

Noise Filter: When initiating write cycle, the write pulse of less than 20ns is locked.

Write Inhibit: When $\overline{OE}$ is low TTL or $\overline{CE}$ is high TTL, the initiation of write cycle is inhibited.

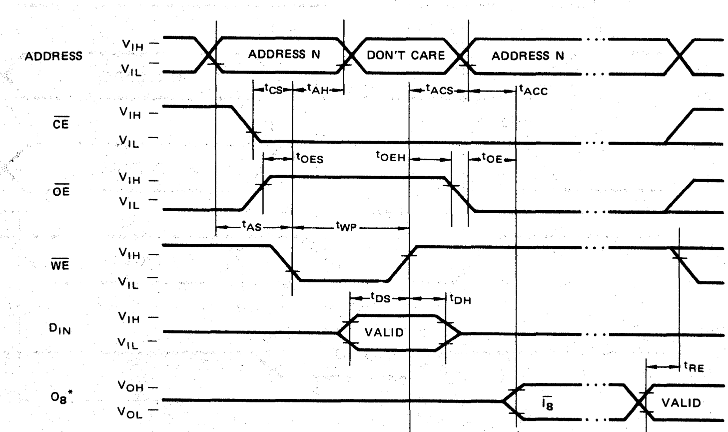
AC CHARACTERISTICS (DATA POLLING)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time to $\overline{WE}$	t_{ACS}	20			ns
Address Access Time	t_{ACC}			350	ns
Output Enable Access Time	t_{OE}			120	ns

Note *1 t_{OE} delays up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

$\overline{DATA}$ PULLING WAVEFORM



Note: * O_1 through O_7 are in High-Z state till end of write.

11

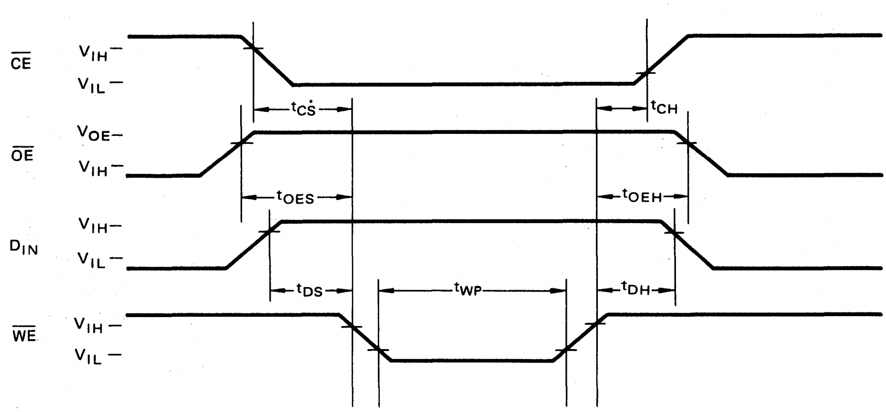
AC CHARACTERISTICS (CHIP ERASE*)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Chip Enable Setup Time	t_{CS}	150			ns
Output Enable Setup Time	t_{OES}	150			ns
Write Pulse Width	t_{WP}	5		20	ms
Data Setup Time	t_{DS}	150			ns
Data Hold Time	t_{DH}	100			ns
Chip Enable Hold Time	t_{CH}	100			ns
Output Enable Hold Time	t_{OEH}	100			ns

Note: * $\overline{OE}$ = 13.5V ± 1.5V

CHIP ERASE WAVEFORM

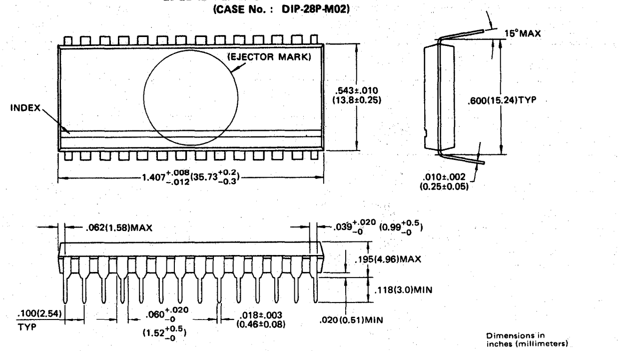


11

PACKAGE DIMENSIONS

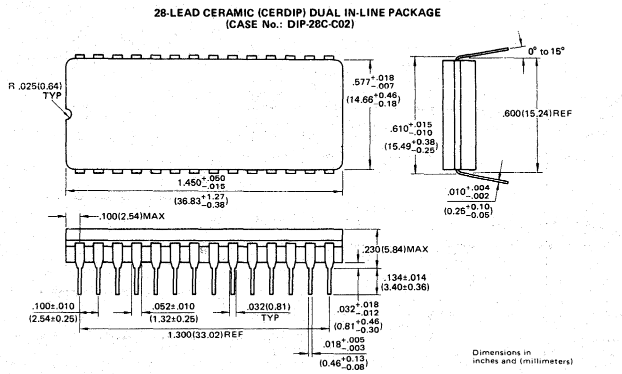
Standard 28-pin Plastic DIP (Suffix: -P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



Standard 28-pin Ceramic DIP (Suffix: -Z)

28-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C02)



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FUJITSU

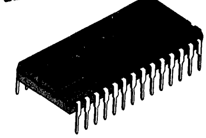
CMOS 65536-BIT ELECTRICALLY ERASABLE PROGRAMMABLE ROM

MBM28C65-25
MBM28C65-35

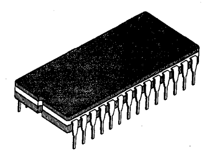
September 1987
Edition 2.0

CMOS 8192 x 8 ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY



PLASTIC PACKAGE
DIP-28P-M02



CERAMIC PACKAGE
DIP-28C-C02

The Fujitsu MBM 28C65 is a high speed 65,536 bits CMOS electrically erasable and electrically programmable read only memory (EEPROM)using a single 5V supply. It is especially well suited not only for application where rapid turn-around and/or bit pattern experimentation and low-power consumption are important but also as replacement of battery-backed-up RAM application.

The MBM 28C65's write operation is similar to that of a Static RAM. Byte write operation is initiated with a TTL low level signal to the $\overline{WE}$ pin, and addresses and data which are internally latched allow the system to do for other tasks during the write operation.

The MBM 28C65 automatically erases the memory bit pattern previously written and then completes writing/verifying a new pattern.
It also has a good DATA Polling function to make the processor realized the completion of write operation by data bus line and RDY/$\overline{BSY}$ control.

The MBM 28C65 is fabricated using CMOS double polysilicon gate technology with stacked gate cells and housed in standard 28-pin DIP package.

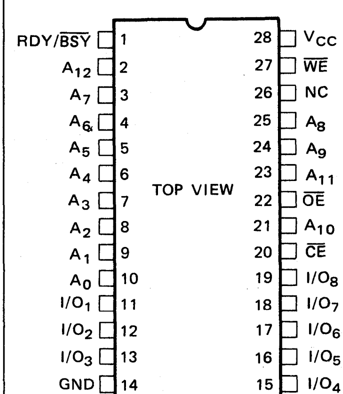
- 8,192 words x 8 bit, fully decoded
- Internally latched address/data in writing
- Automatic Erase before Write
- Self timed Byte Write
- Data protection from short write pulse or noise on $\overline{WE}$
- On chip data verification
- Chip Erase capability using external power supply.
- Write status identificator $\overline{DATA}$ POLLING
- Lower power
  Active: 110 mW/MHz max.
  Standby: 550μW max.
- Single +5V supply, ±10% tolerance
- Access time
  250 ns max. (MBM 28C65-25)
  350 ns max. (MBM 28C65-35)
- TTL compatible input/output for fully MPU interface
- Tri-state output for wired-OR capability
- Output enable ($\overline{OE}$) for simple memory expansion
- Minimum Endurance of 10000 Erase/Write cycle per Byte
- JEDEC approved pin assignment and package
- Standard 28 pin CERAMIC (CERDIP) package: Suffix: -Z
- Standard 28 pin PLASTIC DIP package: Suffix: -P

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage with Respect to GND		V_{CC}	–0.3 to +7.0	V
All Input/output Voltage with Respect to GND		V_{IN}, V_{OUT}	–0.3 to V_{CC}+0.3	V
Voltag on A_9 with Respect to GND		V_{A9}	–0.3 to +13.5	V
Voltage on $\overline{OE}$ with Respect to GND		V_{OE}	–0.3 to +15.5	V
Output Current on RDY/$\overline{BSY}$ with Tespect to GND		I_{OS}	+10.0	mA
Temperature under Bias		T_{BIAS}	–25 to +85	°C
Storage Temperature	Ceramic	T_{STG}	–65 to +125	°C
	Plastic		–45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

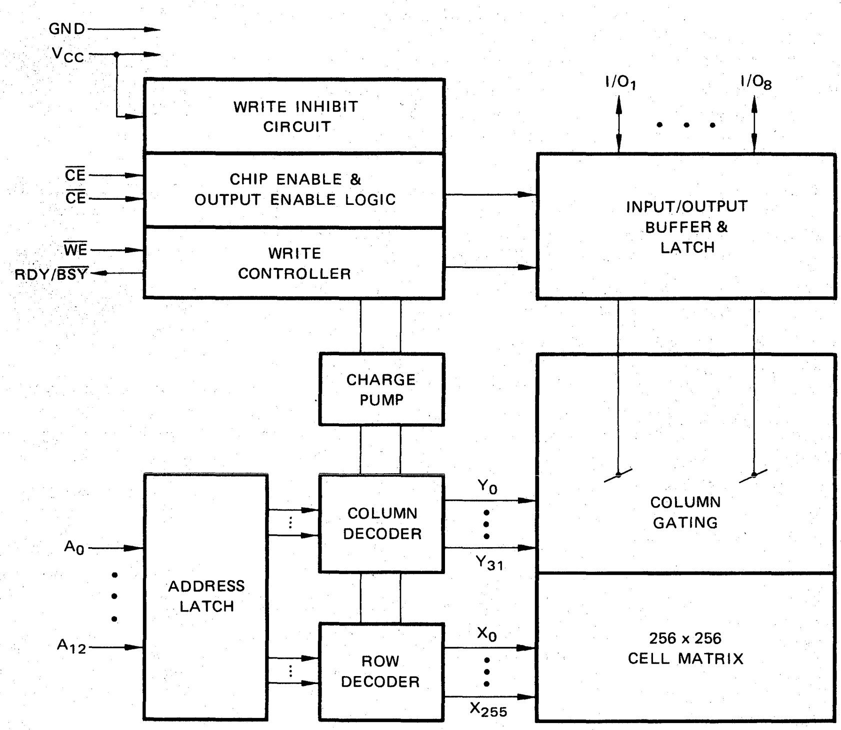


This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

11

11

BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}			10	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			10	pF

FUNCTION TRUTH TABLE

Mode \ Pin Name	Address	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/BSY (Open Drain)	Data I/O	Power
Read	A_{IN}	V_{IL}	V_{IL}	V_{IH}	High-Z	D_{OUT}	Active
Standby and Write Inhibit	X	V_{IH}	X	X	High-Z	High-Z	Standby
Write	A_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{OL}	D_{IN}	Write
DATA POLLING*	A_{IN}	V_{IN}	V_{IL}	V_{IH}	V_{OL}	$I/O_8 = \overline{I_8}$ I/O_1 to I/O_7 = High-Z	Write
Write Inhibit	A_{IN}	X	V_{IL}	X	High-Z	High-Z	Active
			X	V_{IH}			
Chip Erase	X	V_{IL}	V_{OE}	V_{IL}	V_{OL}	V_{IH}	Chip Erase

Note X: Can be either V_{IL} to V_{IH}.
V_{OE}: 13.5V ± 1.5V
*: The address must be applied the written address and the all output data becomes input data from the point where the write mode is completed.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3V	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

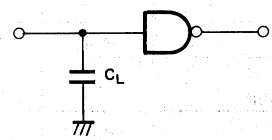
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = 5.5V	I_{LI}	−10	10	μA
Output Leakage Current	V_{OUT} = 5.5V	I_{LO}	−10	10	μA
V_{CC} Standby Current	$\overline{CE} = V_{IH}$	I_{SB1}		1	mA
V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3V$	I_{SB2}		100	μA
V_{CC} Active Current	$\overline{CE} = V_{IL}$	I_{CC1}		20	mA
V_{CC} Active Current	$\overline{CE} = V_{IL}$ f = 4MHz, I_{OUT} = 0mA	I_{CC2}		20	mA
V_{CC} Write Current	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$	I_{CCW}		40	mA
V_{CC} Chip Erase Current	$\overline{CE} = \overline{WE} = V_{IL}$, $\overline{OE} = V_{OE}$	I_{CCE}		100	mA
Output Low Level	I_{OL} = 2.1mA	V_{OL}		0.45	V
Output High Level	I_{OH} = −400μA	V_{OH}	2.4		V
Write Inhibit V_{CC} Level		V_{INH}		3	V
Chip Erase Voltage		V_{OE}	12	15	V

AC TEST CONDITIONS

Input pulse levels: 0.45V to 2.4V
Input Rise/Fall Times: ≦ 20ns
Input Reference Levels: 1.0V to 2.0V
Output Reference Levels: 0.8V to 2.0V
Output Load: 1 TTL gate and C_L = 100pF



AC CHARACTERISTICS (READ)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM 28C64-25		MBM 28C64-35		Unit
		Min	Max	Min	Max	
Address Access Time	t_{ACC}		250		350	ns
$\overline{CE}$ to Output Delay	t_{CE}		250		350	ns
$\overline{OE}$ to Output Delay*1	t_{OE}		100		120	ns
$\overline{OE}$ High to Output	t_{OH}	0		0		ns
$\overline{CE}$, $\overline{OE}$ High to Output Float*2	t_{DF}		60		80	ns

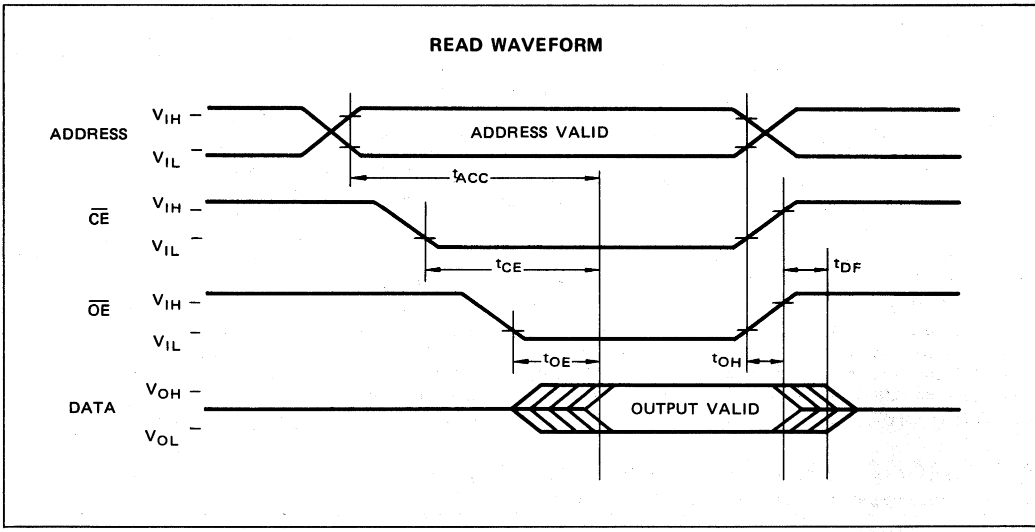
Note: *1 t_{OE} delays up t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

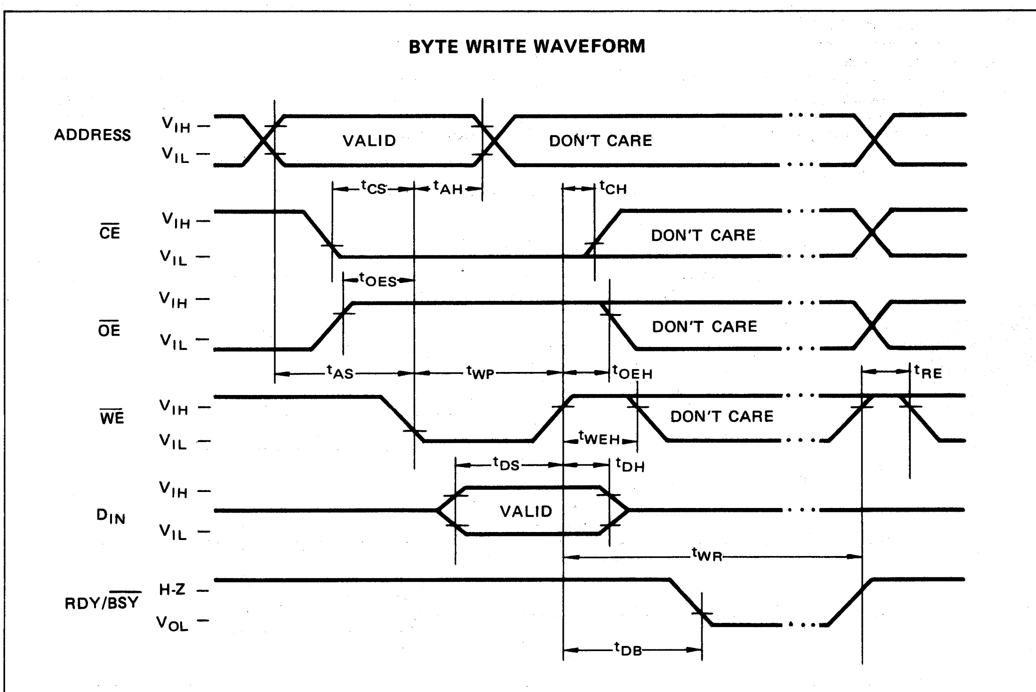
AC CHARACTERISTICS (BYTE WRITE)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	20			ns
Chip Enable Setup Time	t_{CS}	0			ns
Output Enable Setup Time	t_{OES}	20			ns
Write Pulse Width	t_{WP}	100			ns
Address Hold Time	t_{AH}	50			ns
Data Setup Time	t_{DS}	50			ns
Data Hold Time	t_{DH}	20			ns
Chip Enable Hold Time	t_{CH}	0			ns
Output Enable Hold Time	t_{OEH}	20			ns
Write Enable Hold Time	t_{WEH}	10			ns
Time to Device Busy	t_{DB}			120	ns
Byte Write Cycle Time	t_{WR}			10	ms
Write Recovery Time	t_{RE}	50			ns
RDY/$\overline{BSY}$ to Output Time*	t_{RBO}			100	ns
Number of Write per Byte	n	10			x1000

Note: * If $\overline{CE}$ = $\overline{OE}$ = V_{IL} and RDY/$\overline{BSY}$ is going to OFF, The readed data is valid after t_{RBO}.


READ WAVEFORM
ADDRESS
V_{IH}
V_{IL}
ADDRESS VALID
t_{ACC}
$\overline{CE}$
t_{CE}
t_{DF}
$\overline{OE}$
t_{OE}
t_{OH}
DATA
V_{OH}
V_{OL}
OUTPUT VALID


BYTE WRITE WAVEFORM
ADDRESS
V_{IH}
V_{IL}
VALID
DON'T CARE
t_{CS}
t_{AH}
t_{CH}
$\overline{CE}$
DON'T CARE
t_{OES}
$\overline{OE}$
DON'T CARE
t_{AS}
t_{WP}
t_{OEH}
t_{RE}
$\overline{WE}$
DON'T CARE
t_{WEH}
t_{DS}
t_{DH}
D_{IN}
VALID
t_{WR}
RDY/$\overline{BSY}$
H-Z
V_{OL}
t_{DB}

WRITE INFORMATION

BYTE WRITE

The MBM 28C65's write mode is similar to that of Static RAM. The write cycle is completely self-timed, and initiated by a low going TTL pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address data is latched. On the rising edge, the input data is latched. During the write cycle, the MBM 28C65 automatically erases the memory data previously written and new data written into the memory is verified to ensure successufully the byte write.

The RDY/$\overline{BSY}$ pin (Pin 1) goes to a low TTL level indicating that the MBM 28C65 is in a write cycle. When RDY/$\overline{BSY}$ goes back to a high impedance state, the MBM 28C65 has complete writing, and is ready to execute another cycle.

CHIP ERASE

The MBM 28C65 has a chip erase mode using external power supply which all data can be written to high state (= the erased state). The chip erase mode is initiated by setting $\overline{OE}$ to 13.5V and applying low TTL level to $\overline{WE}$ while holding all data inputs on high TTL level.

DATA POLLING

The MBM 28C65 features DATA Polling to signal the completion of a byte write cycle. During a write cycle, an attemped read of the last byte written results in the data complement of that byte at I/O_8. After completion of the write cycle, true data is available.

DATA Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

DATA PROTECTION

The MBM 28C65 has three features to prevent a erroneous initiation of write mode.

V_{CC} Detecter: When the V_{CC} is less than +3V during V_{CC} power-on and power-off, the write function is inhibited.

Noise Filter: When initiating write cycle, the write pulse of less than 20ns is locked.

Write Inhibit: When $\overline{OE}$ is low TTL or $\overline{CE}$ is high TTL, the initiation of write cycle is inhibited.

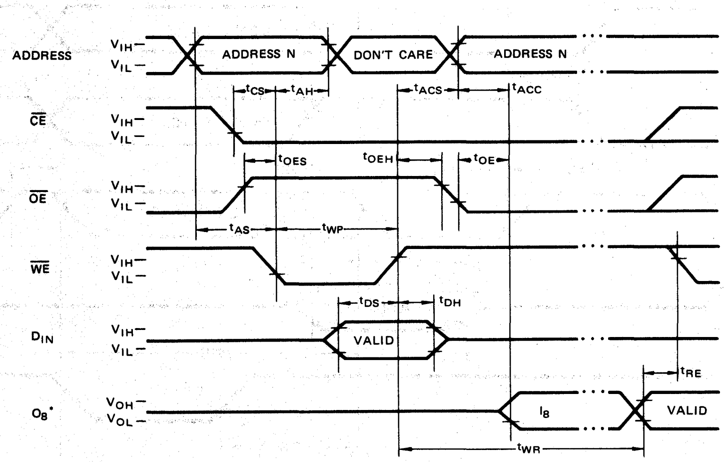
AC CHARACTERISTICS ($\overline{DATA}$ POLLING)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time to $\overline{WE}$	t_{ACS}	20			ns
Address Access Time	t_{ACC}			350	ns
Output Enable Access Time	t_{OE}			120	ns

Note: * t_{OE} delays to up t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

$\overline{DATA}$ PULLING WAVEFORM



Note: *0_1 through 0_7 are in High-Z state till end of write.

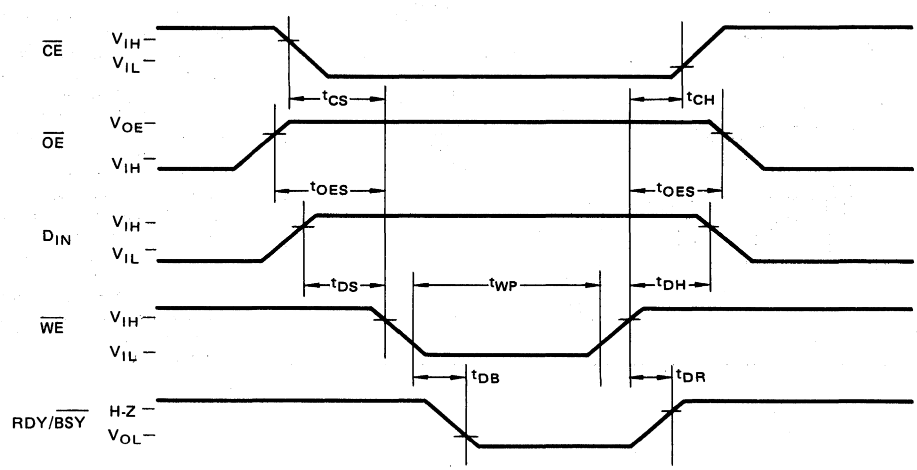
AC CHARACTERISTICS (CHIP ERASE*)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Chip Enable Setup Time	t_{CS}	150			ns
Output Enable Setup Time	t_{OES}	150			ns
Write Pulse Width	t_{WP}	5		20	ms
Data Setup Time	t_{DS}	150			ns
Data Hold Time	t_{DH}	100			ns
Chip Enable Hold Time	t_{CH}	100			ns
Output Enable Hold Time	t_{OEH}	100			ns
Time to Device Busy	t_{DB}			120	ns
Time to Device Ready	t_{DR}			120	ns

Note: * $\overline{OE}$ = 13.5V ± 1.5V

CHIP ERASE WAVEFORM



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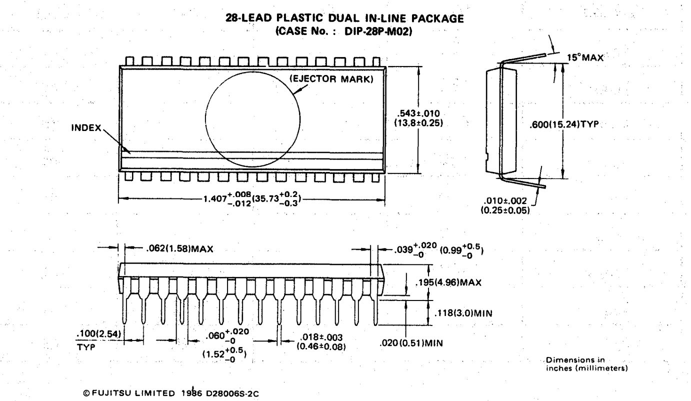
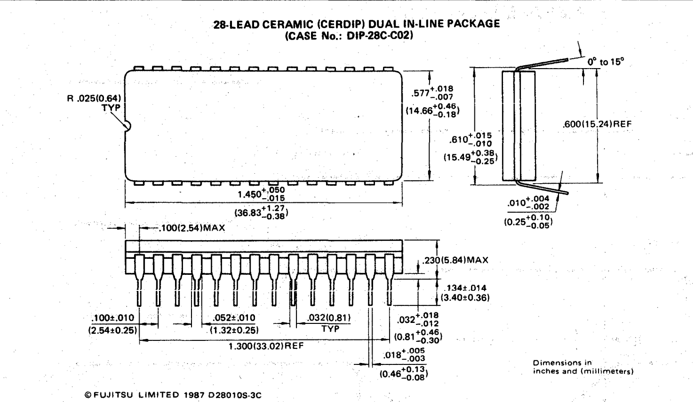
PACKAGE DIMENSIONS

Standard 28-pin Plastic DIP (Suffix: -P)



Standard 28-pin Ceramic DIP (Suffix: -Z)



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FUJITSU

256K CMOS ELECTRICALLY ERASABLE PROM

MBM28C256

April 1988
Edition 1.0

256K BIT(32,768 x 8) CMOS ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY

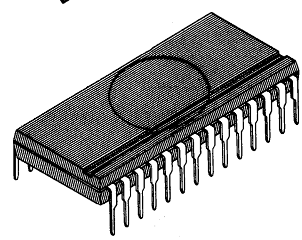
The Fujitsu MBM28C256 is a high speed read-only static memory that is electrically erasable and reprogrammable. The device contains 262,144 reprogrammable bits organized in a 32,768-byte/8-bit format.

The MBM28C256 has a high-voltage generator on chip; which allow to program or erase data using single +5V supply, the write operation can be similar to that of a static RAM.

The MBM28C256 is fabricated using CMOS double polysilicon gate technology with stacked gate cells and housed in a standard 28-pin plastic DIP package.

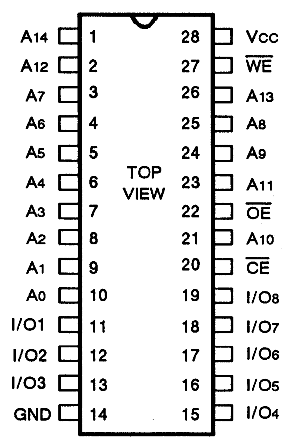
- 32,768-byte/8-bit organization with on-chip decoding
- Internally latched address/data in writing
- Automatic Erase before Write
- Single-byte or 64-byte programming capability
- Data protection from short write pulse or noise on $\overline{WE}$
- Software data protection
- Chip Erase capability using external power supply
- Write status identificator DATA POLLING
- Single +5V(±10%) power supply with low current drain:
  Active operation : 50 mA max.
  Standby operation: 0.1 mA max.
- Fast access time :
  150 ns max. (MBM28C256-15)
- TTL-compatible inputs/outputs
- Three-state output for wired-OR capability
- Output enable($\overline{OE}$) for simple memory expansion
- Minimum Endurance of 10000 Erase/Write cycle per Byte
- JEDEC approval pin assignment and package
- Standard 28-pin PLASTIC DIP package (600mil): Suffix -P

ADVANCE INFORMATION



PLASTIC PACKAGE
(DIP-28P-M02)

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Section 12

NMOS Non-Volatile RAMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options	Sealing Method
12-3	MBM2212-20 MBM2212-25	200 250	1024 bits (256w x 4b)	18-pin Plastic DIP 18-pin Ceramic DIP	Plastic CERDIP

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FUJITSU

MOS 1024-BIT NON-VOLATILE RANDOM ACCESS MEMORY

MBM2212-20
MBM2212-25

December 1987
Edition 3.0

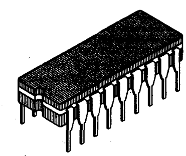
1024-BIT NON-VOLATILE STATIC RANDOM ACCESS MEMORY

The Fujitsu MBM 2212 is a 1024-bit non-volatile static random access memory (NVRAM) combined 1024 bit static random access memory (SRAM) and electrically erasable programmable read only memory (EEPROM) on one-chip. It is designed for applications such as system potentiometer or electrical switch to memorize the system condition etc.

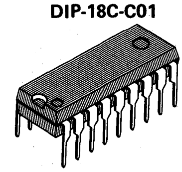
The MBM 2212 is organized as 256 words by 4 bit. Each one word is constituted with a pair of SRAM and EEPROM cell. The read and write operations are performed on the SRAM cell. The data transfer between SRAM and EEPROM is performed using two control pins. The store mode (transfering SRAM data to EEPROM) is executed with one shot pulse applied to $\overline{ST}$ pin in 10ms. The recall mode (transfering EEPROM data to SRAM) is executed with one shot pulse applied to $\overline{RC}$ pin in 1.2μs. Both store and recall operations are completed all bits at one time.

The MBM 2212 is fabricated using N-MOS silicon gate technology with floating gate cells. Single +5V supply and TTL input/output level operations greatly facilitate microprocessor applications.

- 256 words x 4 bit organization, fully decoded
- 10ms self-timed auto store
- 10 years data retention for each store
- Unlimited endurance for recall
- TTL compatible inputs/outputs
- Tri-state output
- Write protection on power-on/off and surge pulse
- Low power consumption;
  Active: 330mW max.
  Standby: 165mW max.
- Fast access time;
  200ns max. (MBM 2212-20)
  250ns max. (MBM 2212-25)
- Standard 18 pin CERAMIC DIP package: Suffix-Z
- Standard 18 pin PLASTIC DIP package: Suffix-P
- Pin compatible with Xicor X2212

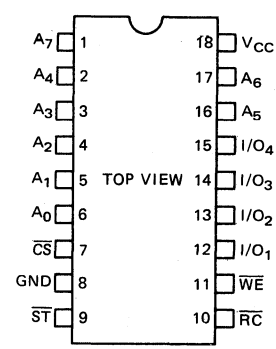


CERAMIC PACKAGE
(CERDIP)
DIP-18C-C01



PLASTIC PACKAGE
(PLASTIC)
DIP-18P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with Respect to GND	V_{CC}	–1.0 to +7.0	V
All Input/Output Voltage with Respect to GND	V_{IN}, V_{OUT}	–1.0 to +7.0	V
Output Current with Respect to GND	I_{OUT}	+5.0	mA
Temperature under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature	T_{STG}	–65 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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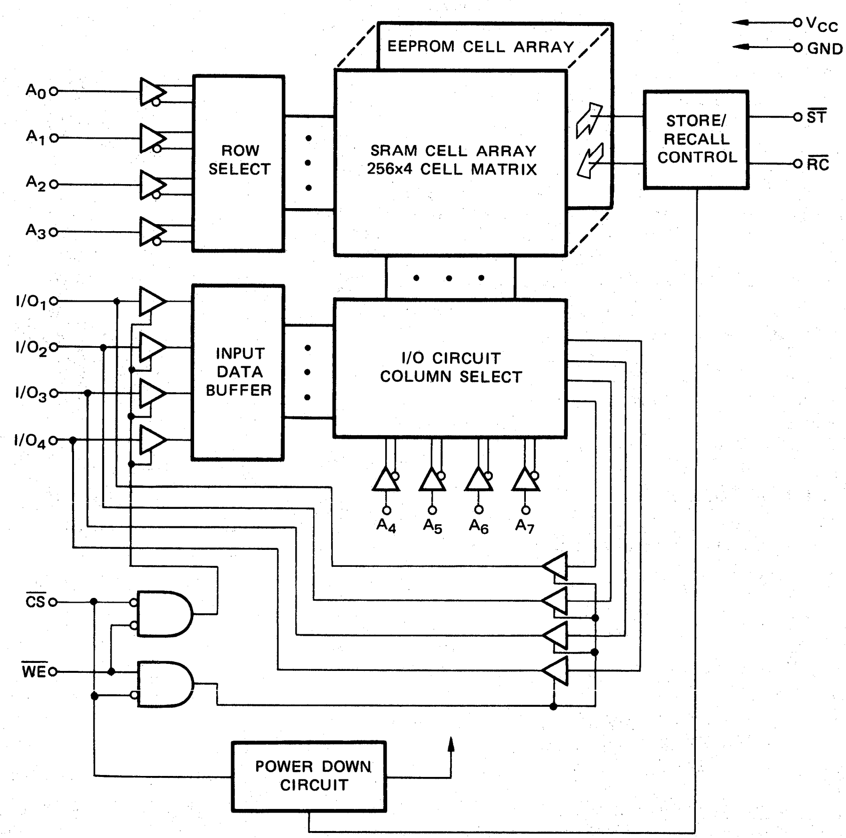
Fig. 1 — MBM 2212 BLOCK DIAGRAM



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CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{RC}$	$\overline{ST}$	I/O	V_{CC}	GND	POWER
Standby	V_{IH}	X	V_{IH}	V_{IH}	High-Z	5V	GND	Standby
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	D_{OUT}	5V	GND	Active
Write	V_{IL}	V_{IL}	V_{IH}	V_{IH}	D_{IN}	5V	GND	Active
Recall	X	V_{IH}	V_{IL}	V_{IH}	High-Z	5V	GND	Standby
	V_{IH}	X						
Store	X	V_{IH}	V_{IH}	V_{IL}	High-Z	5V	GND	Active
	V_{IH}	X						

Note: X Can be either V_{IL} or V_{IH}

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltae	V_{CC}	4.5	5.0	5.5	V
Input High Level	V_{IH}	2.0		$V_{CC}+0.5$	V
Input Low Level	V_{IL}	-1.0*		0.8	V
Operating Temperature	T_A	0		70	°C

Note: * For less than 50ns undershoot, but -0.5V for DC.

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = GND to 5.5V	$\lvert I_{LI} \rvert$		10	μA
I/O Leakage Current	$\overline{CS} = V_{IH}$, $V_{I/O}$ = GND to 5.5V	$\lvert I_{LO} \rvert$		10	μA
V_{CC} Standby Current	$\overline{CS} = V_{IH}$, V_{CC} = 4.5V to 5.5V, $I_{I/O}$ = 0mA*1	I_{SB}		30	mA
V_{CC} Active Current	$\overline{CS} = V_{IL}$, V_{CC} = 5.5V, $I_{I/O}$ = 0mA*2	I_{CC}		60	mA
Output Low Level	I_{OL} = 4.2mA	V_{OL}		0.4	V
Output High Level	I_{OH} = -2.0mA	V_{OH}	2.4		V
Store Inhibit V_{CC} Voltage		V_{IHBT}		2.7	V

Note: *1 Supply current increases to I_{CC} while store mode regardless of $\overline{CS}$ level.
*2 Supply current reduces to I_{SB} while recall mode regardless of $\overline{CS}$ level.

AC CHARACTERISTICS

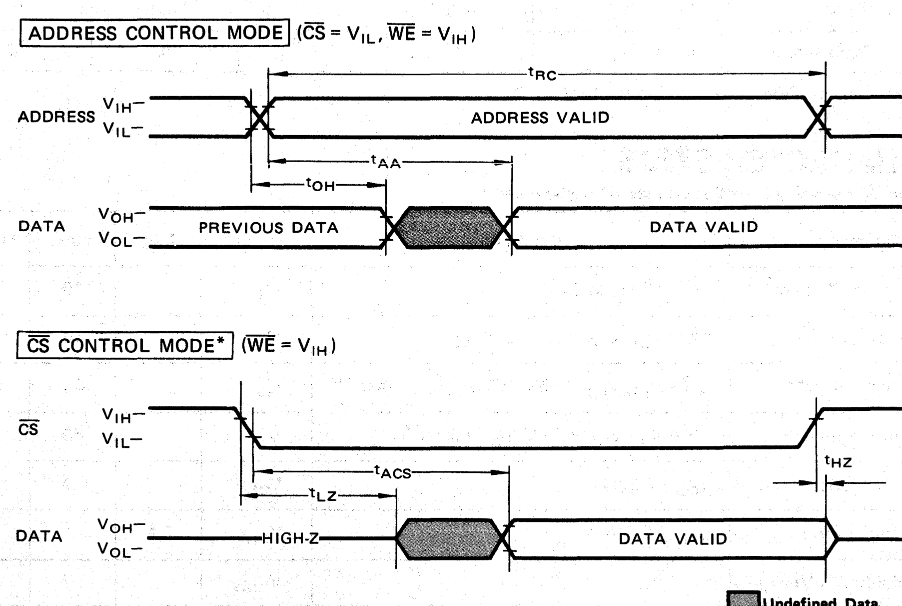
(Recommended operating conditions unless otherwise noted.)

READ MODE ($\overline{WE}$ = $\overline{ST}$ = $\overline{RC}$ = V_{IH})

Parameter	Symbol	MBM 2212-20		MBM 2212-25		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		ns
Address Access Time	t_{AA}		200		250	ns
Chip Select Access Time	t_{ACS}		200		250	ns
Output Hold after Address Change	t_{OH}	50		50		ns
Chip Select to Output Active*	t_{LZ}	10		10		ns
Chip Select to Output Disable*	t_{HZ}		100		100	ns

Note: * Transition is measured at point of ±500mV from steady state voltage.

READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH} for Read Cycle)



Note: *Address valid prior to or coincident with $\overline{CS}$ transition low.

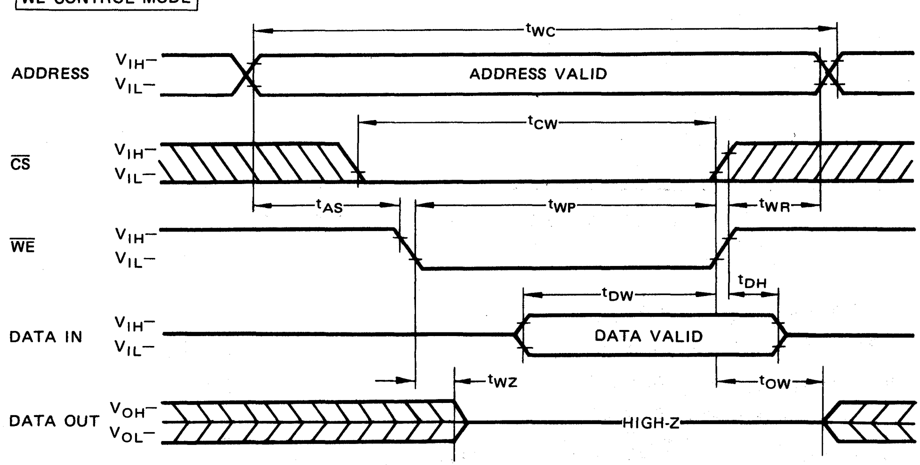
WRITE MODE ($\overline{ST}$ = $\overline{RC}$ = V_{IH})

Parameter	Symbol	MBM 2212-20/25		Unit
		Min	Max	
Write Cycle Time	t_{WC}	300		ns
Chip Select to End of Write ($\overline{WE}$ = V_{IL})	t_{CW}	150		ns
Address Setup Time	t_{AS}	50		ns
Write Pulse Width ($\overline{CS}$ = V_{IL})	t_{WP}	150		ns
Write Recovery Time*1	t_{WR}	25		ns
Data Valid to End of Write	t_{DW}	100		ns
Data Hold Time	t_{DH}	0		ns
Write Enable to Output High-Z*2	t_{WZ}		100	ns
Output Active from End of Write*3	t_{OW}	10		ns

Note: *1 t_{WR} is defined from the end point of write.
*2 Transition is measured at point of ±500mV from steady state voltage.
*3 If $\overline{CS}$ goes high coincident with $\overline{WE}$ high transition, DATA OUT remains in a high impedance state.

WRITE CYCLE TIMING DIAGRAM

$\overline{WE}$ CONTROL MODE



Note: † If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high transition, DATA OUT remains in a high impedance state.

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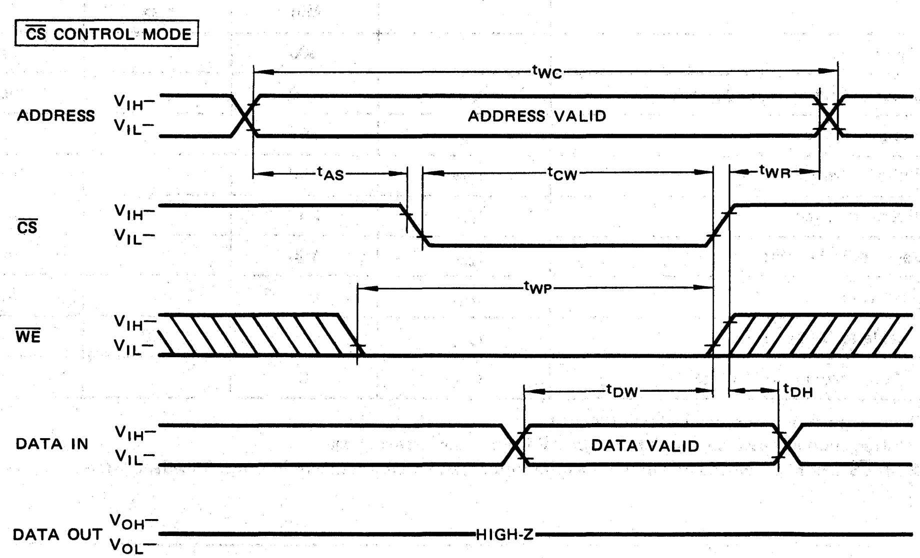
WRITE CYCLE TIMING DIAGRAM



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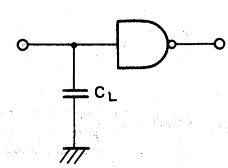
AC TEST CONDITIONS (including EEPROM mode)

Input Pulse Levels:	0.6V to 2.4V
Input Rise/Fall Times:	≦ 10 ns
Input Reference Levels:	0.8V, 2.2V
Output Reference Levels:	0.8V, 2.2V
Output Load:	1 TTL gate and C_L = 100pF



EEPROM READ/WRITE INFORMATION

The MBM 2212 can not read or write EEPROM data externally and it must be transferred from/to SRAM cell array corresponding to each EEPROM bit. $\overline{RC}$ and $\overline{ST}$ pins are assigned to execute these operation easily.

RECALL MODE

The recall mode is initiated when negative pulse (⅂_⌐) is applied to $\overline{RC}$ pin while either $\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IH}$ and is completed within 1.2μs. The supply current is reduced to standby current automatically.
Please notice that the SRAM data is replaced by the EEPROM data after the execution of this operation.

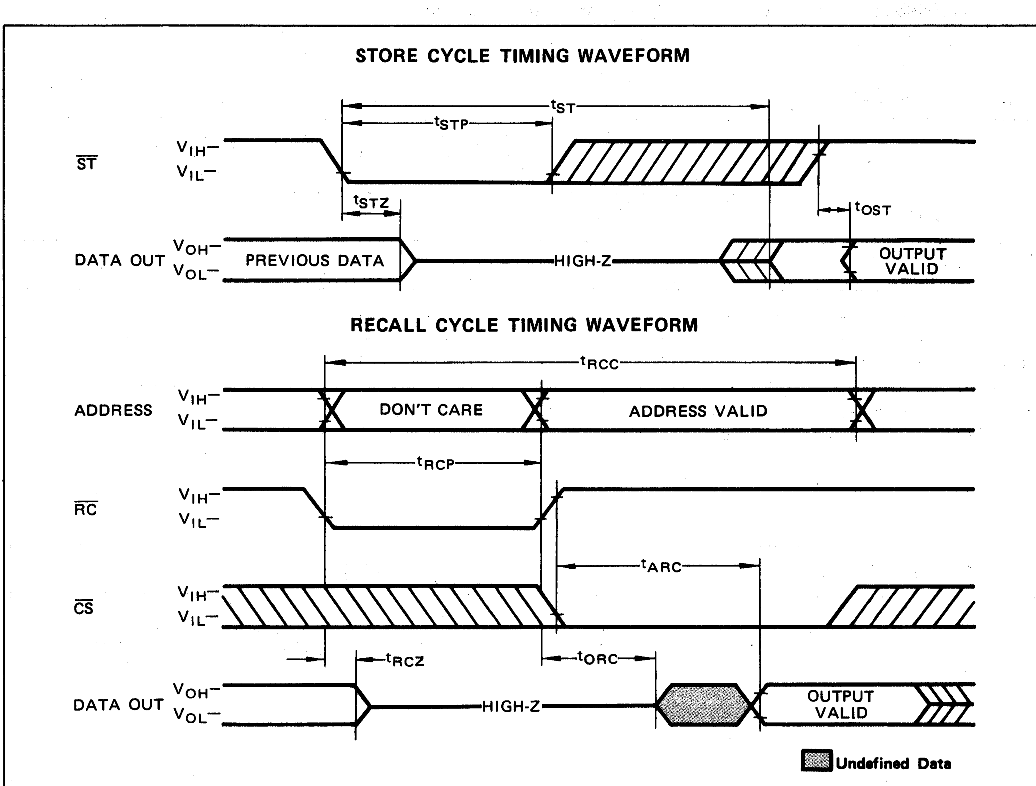
STORE MODE

The store mode is initiated when negative pulse (⅂_⌐) is applied to $\overline{ST}$ pin while either $\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IH}$ and is completed automatically be the on-chip timer. During this operation mode, all input and output pins are inhibited. The original SRAM data remains after the store mode.

The MBM 2212 has two protection circuits to prevent a erroneous store mode. Noise filter circuit for duration of less than 20ns negative pulse on $\overline{ST}$ pin is on the chip.
Auto-standby circuit prevents the store data on the EEPROM cell array from the destruction when V_{CC} is less than +3V.

When V_{CC} power is ON or OFF, the V_{IH} input level must be applied to $\overline{ST}$ pin before or while V_{CC} is greater than +3V.

These operation modes as store mode, recall mode and SRAM write mode have the same logical priority. Normally the first set logical condition determines the following operation mode among $\overline{ST}$, $\overline{RC}$ and $\overline{WE}$ pins.



EEPROM READ/WRITE INFORMATION (cont'd)

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

RECALL MODE ($\overline{WE}$ = $\overline{ST}$ = V_{IH})

Parameter	Symbol	MBM 2212-20/25		Unit
		Min	Max	
Recall Cycle Time	t_{RCC}	1200		ns
Recall Pulse Width	t_{RCP}	450		ns
$\overline{RC}$ to Output Disable*	t_{RCZ}		150	ns
$\overline{RC}$ to Output Active*	t_{ORC}	10		ns
$\overline{RC}$ to Output Valid	t_{ARC}		750	ns

Note: * Transition is measured at point of ±500mV from steady state voltage.

STORE MODE ($\overline{WE}$ = $\overline{RC}$ = V_{IH})

Parameter	Symbol	MBM2212-20		MBM2212-25		Unit
		Min	Max	Min	Max	
Store Cycle Time	t_{ST}		10		20	ms
Store Pulse Width*1	t_{STP}	100		100		ns
Store to Output Disable*2	t_{STZ}		500		500	ns
Output Valid from End of Store	t_{OST}		200		250	ns

Note: *1 It is protected to enter into the store mode by less than 20ns pulse width.
*2 Transition is measured at point of ±500mV from steady state voltage.

ENDURANCE

Number of Store Cycles	Number of Data Changes per Bit	Unit
100,000	10,000	times

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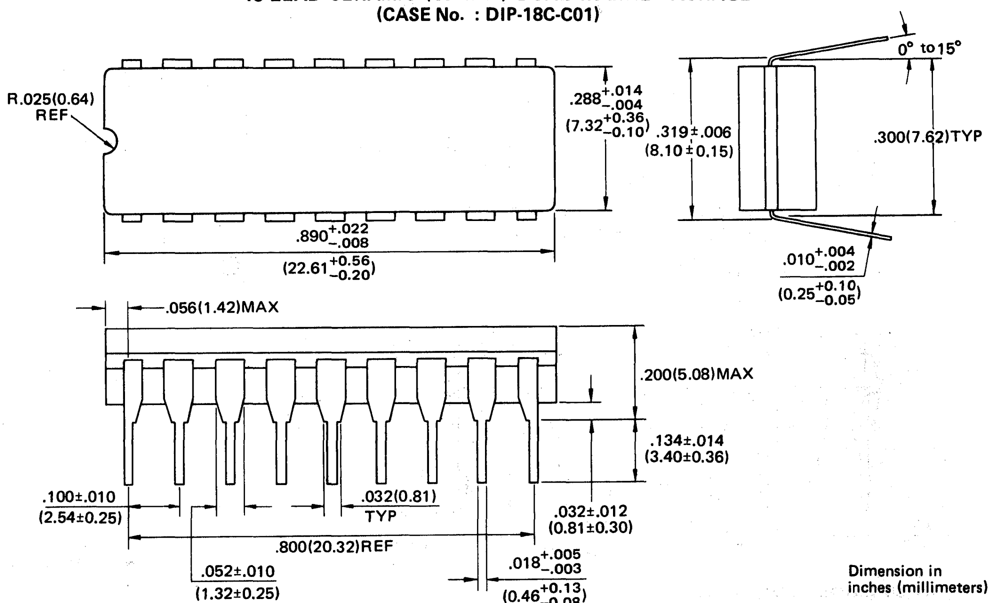
PACKAGE DIMENSIONS

Standard 18-pin Ceramic DIP (Suffix: -Z)

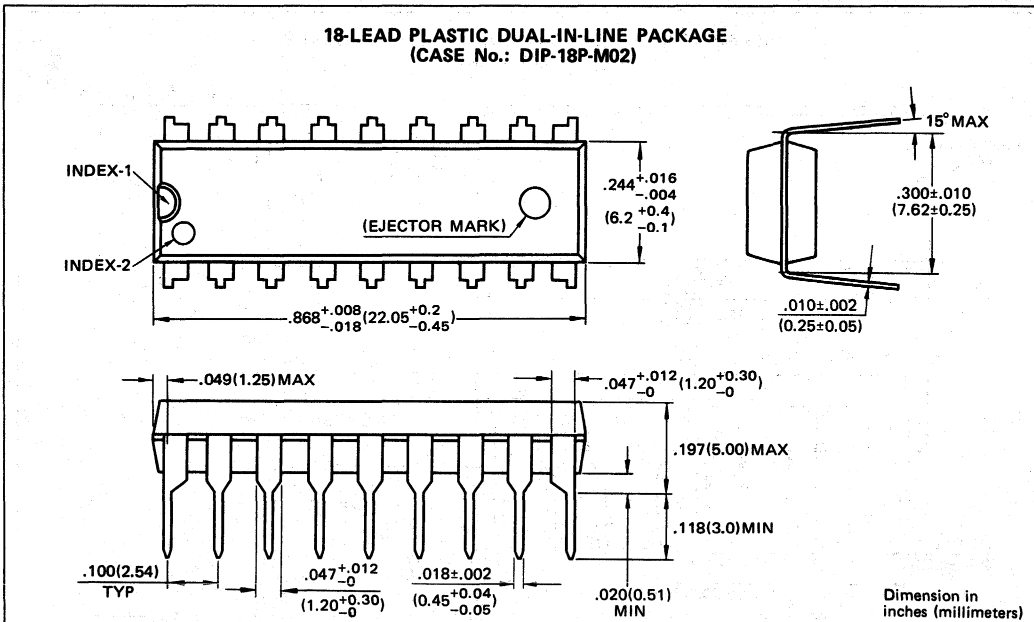
18-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-18C-C01)



Dimension in inches (millimeters)

PACKAGE DIMENSIONS

Standard 18-pin Plastic DIP (Suffix: -P)



Section 13

CMOS Mask ROMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options	Sealing Method
13-3	MB83256	250	262144 bits (32768w x 8b)	28-pin Plastic DIP	Plastic
13-11	MB83512	150	524288 bits (65536w x 8b)	28-pin Plastic DIP	Plastic
13-17	MB831000-15 MB831000-20	150 200	1048576 bits (131072w x 8b)	28-pin Plastic DIP	Plastic
13-25	MB832000	200	2097152 bits (262144w x 8b)	32-pin Plastic DIP	Plastic
13-31	MB834100	250	4194304 bits (262144w x 16b) (524288w x 8b)	40-pin Plastic DIP	Plastic
13-37	MB834000-20 MB834000-25	200 250	4194304 bits (524288w x 8b)	32-pin Plastic DIP	Plastic
13-43	MB8324200	250	4194304 bits (262144w x 16b) (524288w x 8b)	40-pin Plastic DIP 64-pin Plastic FPT	Plastic Plastic

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13

FUJITSU

CMOS 262,144-BIT MASK-PROGRAMMABLE READ ONLY MEMORY

MB 83256

June 1983
Edition 1.0

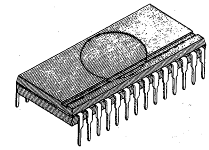
256K-BIT (32,768 x 8) CMOS READ ONLY MEMORY

The Fujitsu MB 83256 is a CMOS Si-gate mask-programmable static read only memory organized as 32,768 words by 8 bits.

The MB 83256 has TTL-compatible I/O and 3-state output level with fully-static operation (i.e. no need of clock signal) and single +5V power supply. Also, the MB 83256 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

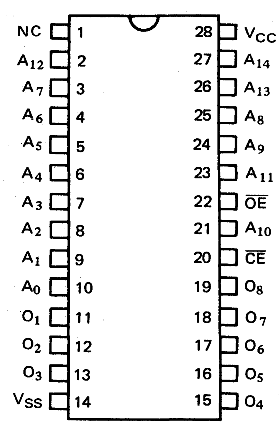
The package for the MB 83256 is a standard 28-pin dual-in-line package and its pin-out is compatible with standard 28-pin EPROM.

- Organization: 32,768 words x 8 bits
- Fast access time: 250 ns max.
- Completely static operation: No clock required
- TTL compatible input/output
- Three-state output
- Single +5V power supply
- Power consumption: 83 mW (Operation)
  8.3 mW (Standby, TTL input level)
  165 μW (Standby, CMOS input level)
- Standard 28-pin DIP



PLASTIC PACKAGE
DIP-28P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Storage Temperature Range	T_{stg}	-40 to +125	°C
Operating Temperature	T_A	-10 to +85	°C
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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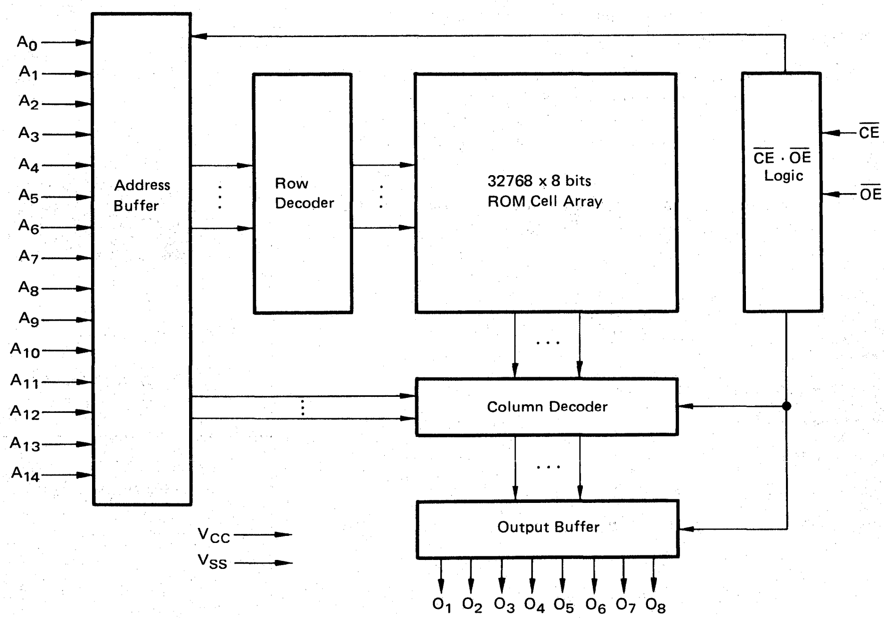
Fig. 1 — MB 83256 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	Output	Power Consumption Mode
H	X	Non-selected	High-Z	Standby
L	H	Non-selected	High-Z	Active
L	L	Selected	Output	Active

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CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitnace (V_{OUT} = 0V)	C_{OUT}	–	–	10	pF
Input Capacitnace (V_{IN} = 0V)	C_{IN}	–	–	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3	–	0.8	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Ambient Temperature	T_A	0	–	70	°C

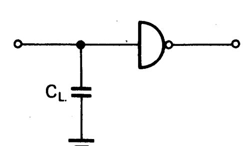
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Stanby Supply Current	I_{SB1}		1.5	mA	$\overline{CE} = V_{IH}$
	I_{SB2}		30	μA	$\overline{CE} = V_{CC}$, V_{IN} = GND or V_{CC}
Active Supply Current	I_{CC}		15	mA	$\overline{CE} = V_{IL}$, Minimum Cycle
Input Leakage Current	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	-10	10	μA	$\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -400 μA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 2.1 mA

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise and Fall Time: t_T = 10 ns
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
  Output: V_{OL} = 0.8V, V_{OH} = 2.2V
- Output Load: 1 TTL Gate and C_L = 100pF



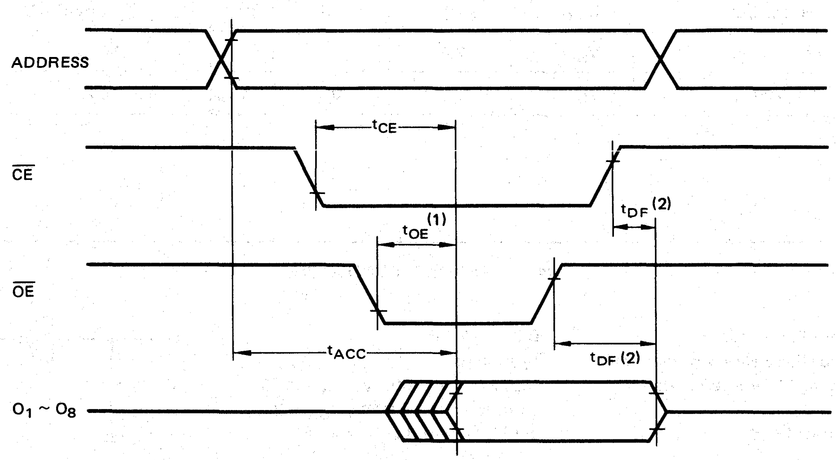
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Valve			Unit
		Min	Typ	Max	
Address Access Time ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{ACC}			250	ns
Chip Enable Access Time ($\overline{OE}$ = V_{IL})	t_{CE}			250	ns
Output Enable Access Time [NOTE 1]	t_{OE}			100	ns
Output Disable Time [NOTE 2]	t_{DF}			80	ns
Output Hold Time	t_{OH}	0			ns

Note: (1) $\overline{OE}$ may be delayed up to ($t_{ACC} - t_{OE}$) after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs earlier.

TIMING DIAGRAM



Note: (1) $\overline{OE}$ may be delayed up to (T_{ACC} − t_{OE}) after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs earlier.

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TYPICAL CHARACTERISTICS CURVES

Fig. 3.– OUTPUT LOW CURRENT vs OUTPUT LOW VOLTAGE

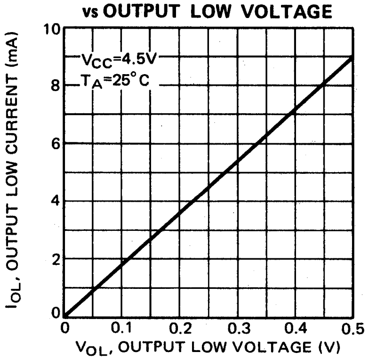


Fig. 4.– OUTPUT HIGH CURRENT vs OUTPUT HIGH VOLTAGE

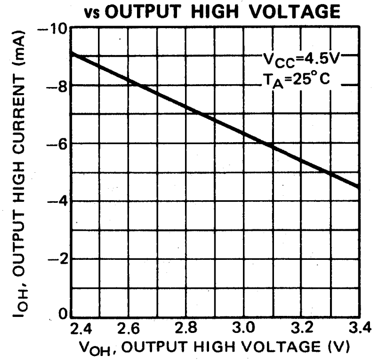


Fig. 5.– POWER SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

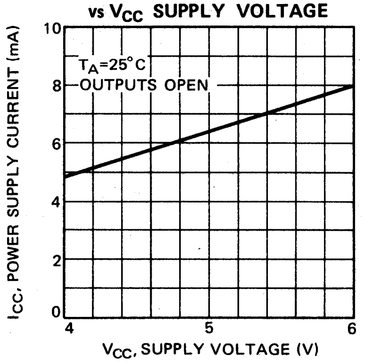


Fig. 6.– POWER SUPPLY CURRENT vs AMBIENT TEMPERATURE

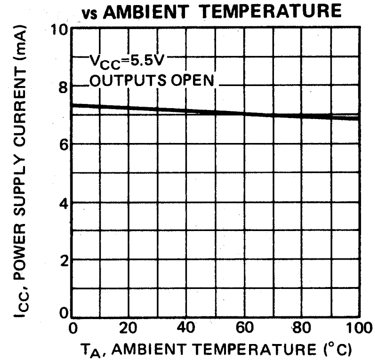


Fig. 7.– ADDRESS ACCESS TIME vs V_{CC} POWER SUPPLY VOLTAGE

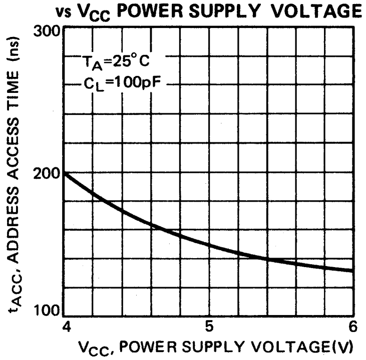


Fig. 8.– POWER SUPPLY CURRENT vs CYCLE TIME

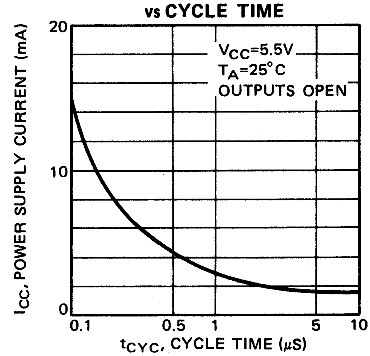


Fig. 9.– OUTPUT ENABLE ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

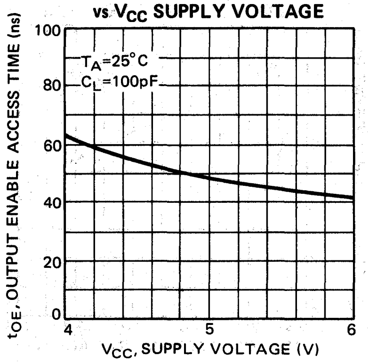


Fig. 10.– OUTPUT DISABLE TIME vs AMBIENT TEMPERATURE

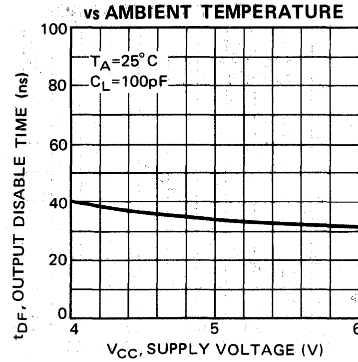


Fig. 11.– ADDRESS ACCESS TIME vs. LOAD CAPACITANCE

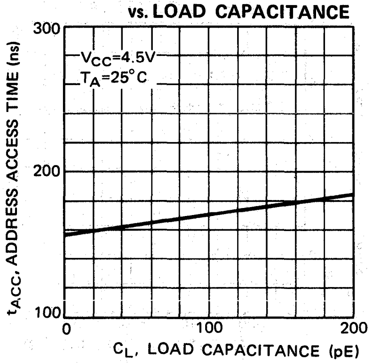
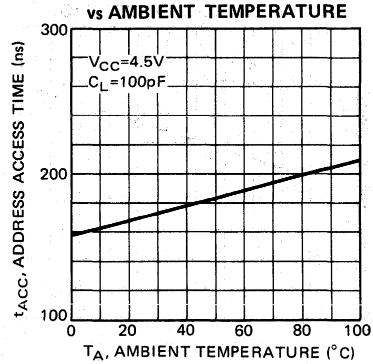
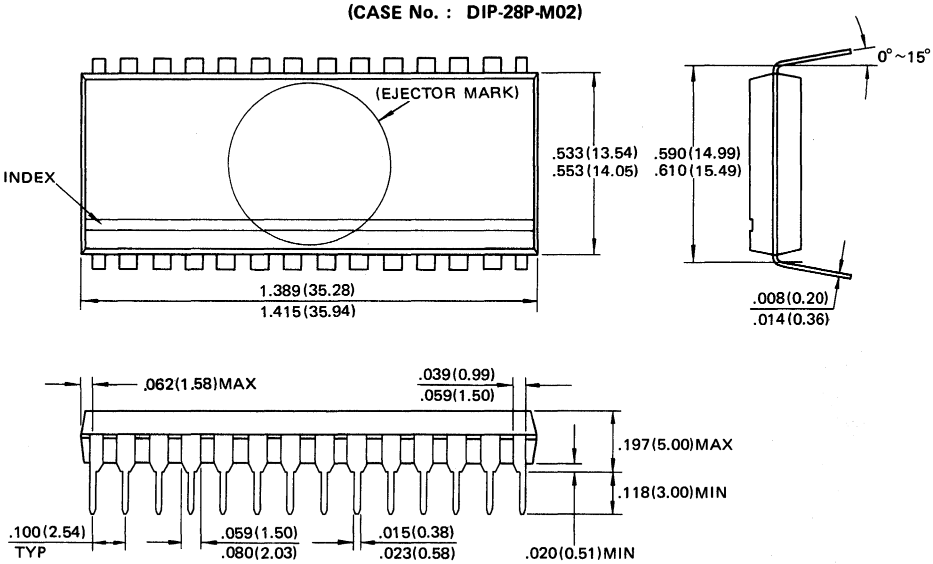


Fig. 12.– ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE



PACKAGE DIMENSIONS

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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FUJITSU

CMOS 524,288-BIT MASK-PROGRAMMABLE READ ONLY MEMORY

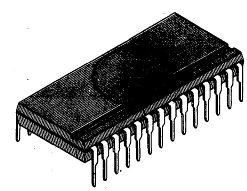
MB 83512

April 1987
Edition 1.0

524, 288-BIT (65,536 x 8) CMOS READ ONLY MEMORY

The Fujitsu MB 83512 is a CMOS Si-gate mask-programmable static read only memory organized as 65,536 words by 8 bits.

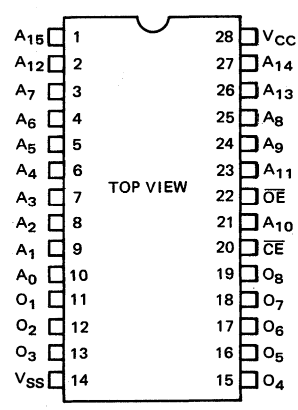
The MB 83512 has TTL-compatible I/O and 3-state output level with fully-static operation (i.e. no need of clock signal) and single +5 V power supply. Also, the MB 83512 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.



PLASTIC PACKAGE
DIP-28P-M02

- Organization: 65,536 words x 8 bits
- Access time : 150 ns
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5 V power supply
- Power dissipation : 220 mW max. (Active)
  16.5 mW max. (Standby, TTL input level)
  275 μW max. (Standby, CMOS input level)
- Standard 28-pin DIP

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE) (Reference to VSS)

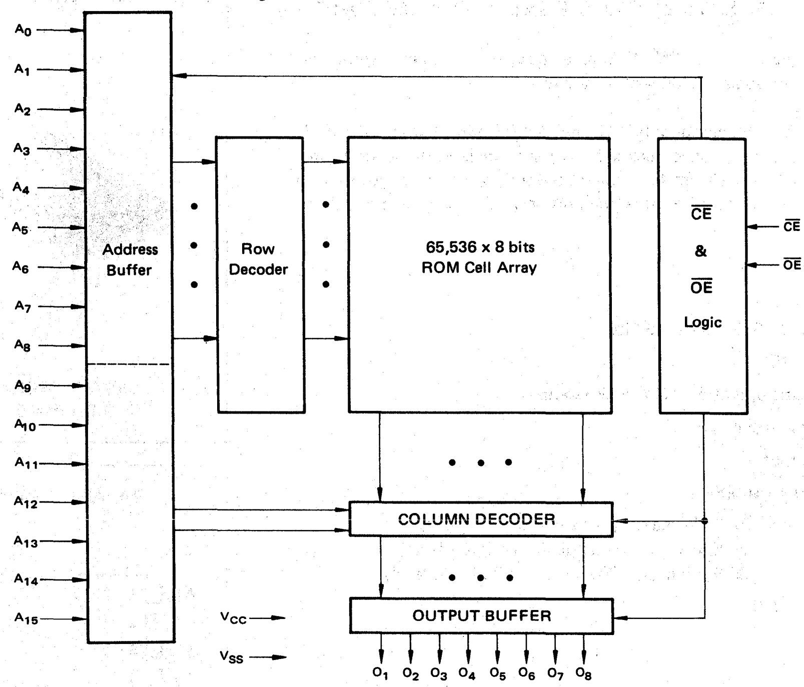
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}+0.5	V
Output Voltage	V_{OUT}	-0.5 to V_{CC}+0.5	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature Range	T_{STG}	-45 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

13

Fig. 1 — MB 83512 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUT	POWER DISSIPATION MODE
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	H	NOT SELECTED	HIGH-Z	ACTIVE
L	L	SELECTED	OUTPUT	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}			10	pF
Input Capacitance (V_{IN} = 0 V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

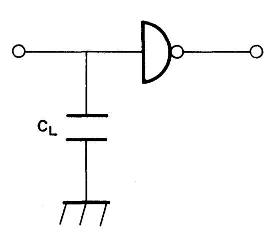
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Active Supply Current	$\overline{CE} = V_{IL}$, Minimum Cycle	I_{CC}		40	mA
Standby Supply Current	$\overline{CE} = V_{IH}$	I_{SB1}		3	mA
	$V_{IN} = V_{SS}$ or V_{CC} $\overline{CE} = V_{CC} = V_{IH}$	I_{SB2}		50	μA
Input Leakage Current	V_{IN} = 0 to V_{CC}	I_{LI}	-10	10	μA
Output Leakage Current	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$	I_{LO}	-10	10	μA
Output High Voltage	I_{OH} = -400 μA	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}		0.4	V

Fig. 2 — AC TEST CONDITION

- Input Pulse Level : 0.6 to 2.4 V
- Input Pulse Rise and Fall Time : t_T = 5 ns
- Timing Reference Levels : Input : V_{IL} = 0.8 V, V_{IH} = 2.2 V
  Output : V_{OL} = 0.8V, V_{OH} = 2.2 V
  : 1 TTL Gate and C_L (100 pF)

- Output Load



AC CHARACTERISTICS

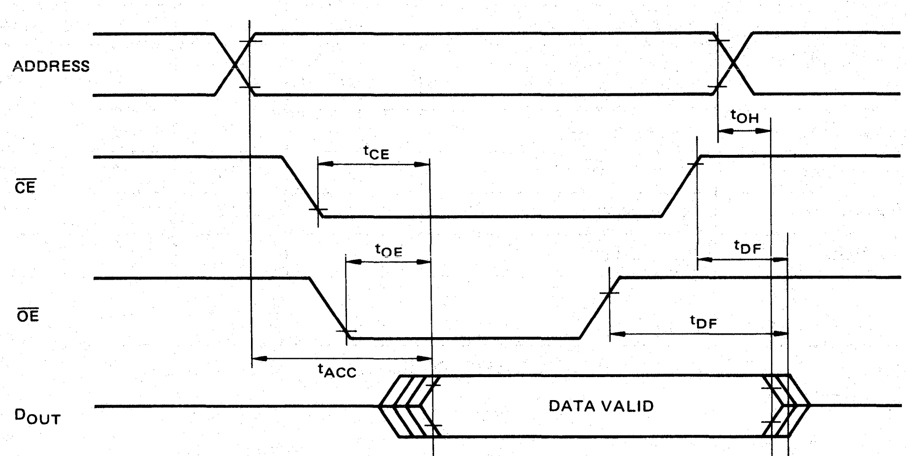
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	t_{ACC}		150	ns
Chip Enable Access Time	$\overline{OE} = V_{IL}$	t_{CE}		150	ns
Output Enable Access Time	Note 1	t_{OE}		80	ns
Output Disable Time	Note 2	t_{DF}		60	ns
Output Hold Time		t_{OH}	0		ns

Note 1 $\overline{OE}$ may be delayed up to (t_{ACC}-t_{OE}) after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occers earlier.

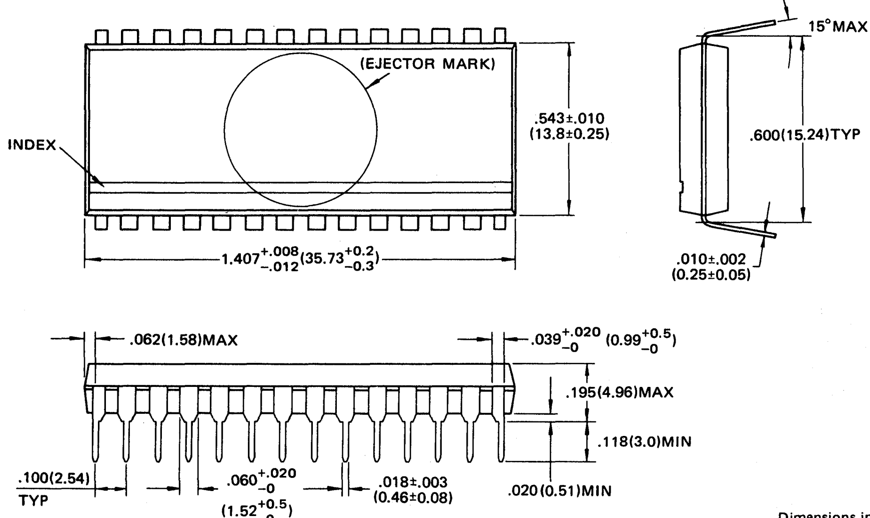
TIMING DIAGRAM



13

PACKAGE DIMENSIONS

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

CMOS 1M-BIT MASK-PROGRAMMABLE READ ONLY MEMORY

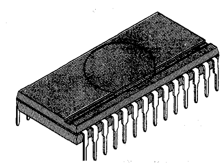
MB831000-15
MB831000-20

November 1987
Edition 2.0

1M-BIT (131,072 x 8) CMOS READ ONLY MEMORY

The Fujitsu MB 831000 is a CMOS Si-gate mask-programmable static read only memory organized as 131,072 words by 8 bits.

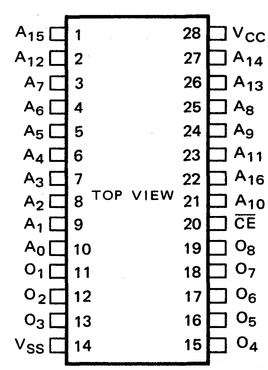
The MB 831000 has TTL-compatible I/O and 3-state output level with fully-static operation (i.e. no need of clock signal) and a single +5V power supply is required. Also, the MB 831000 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.



PLASTIC PACKAGE
DIP-28P-M02

- Organization: 131,072 words x 8 bits
- Access time: 150 ns (MB 831000-15)
  200 ns (MB 831000-20)
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5V power supply
- Power dissipation: 220 mW max. (Active)
  16.5 mW max. (Standby, TTL input level)
  275 μW max. (Standby, CMOS input level)
- Standard 28-pin DIP

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0*	V
Input Voltage	V_{IN}	-0.5 to V_{CC}+0.5*	V
Output Voltage	V_{OUT}	-0.5 to V_{CC}+0.5*	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature Range	T_{STG}	-45 to +125	°C

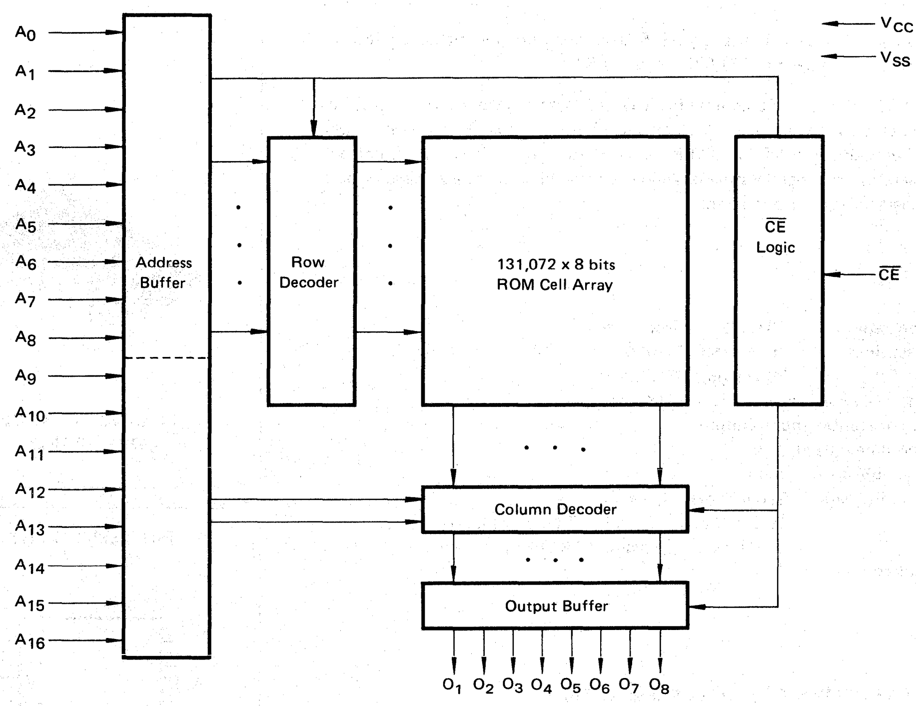
* Referenced to GND

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

13

Fig. 1 — MB 831000 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	MODE	Output	Power Dissipation Mode
H	Not selected	High-Z	Standby
L	Selected	Output	Active

13

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

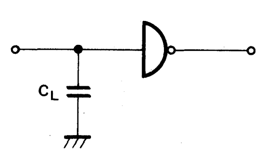
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Active Supply Current	I_{CC}		40	mA	$\overline{CE} = V_{IL}$, Minimum Cycle
Standby Supply Current	I_{SB1}		3	mA	$\overline{CE} = V_{IH}$
	I_{SB2}		50	μA	$\overline{CE} = V_{CC}$, V_{IN} = GND or V_{CC}
Input Leakage Current	I_{LI}	−10	10	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−10	10	μA	$\overline{CE} = V_{IH}$
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −400μA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 2.1mA

Fig. 2 — AC TEST CONDITION

Input Pulse Level : 0.6 to 2.4 V
Input Pulse Rise and Fall Time : t_T = 10 ns
Timing Reference Levels : Input: V_{IL} = 0.8V, V_{IH} = 2.2V
: Output: V_{OL} = 0.8V, V_{OH} = 2.2V
Output Load : 1 TTL Gate and 100pF



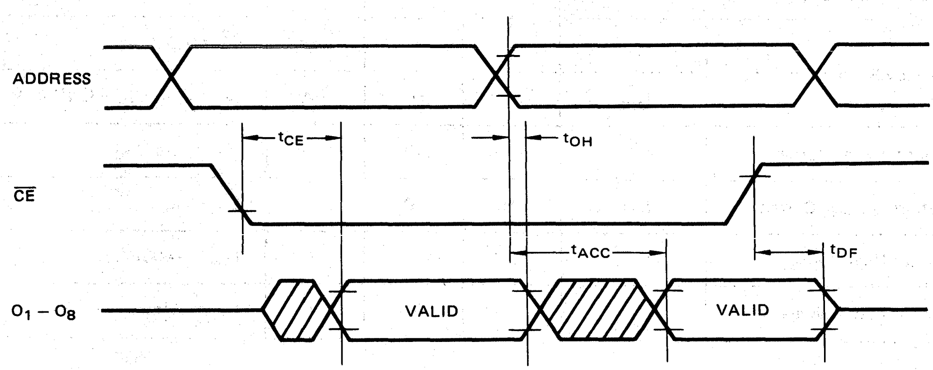
13

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB 831000-15		MB 831000-20		Unit
		Min	Max	Min	Max	
Address Access Time	t_{ACC}		150		200	ns
Chip Enable Access Time	t_{CE}		150		200	ns
Output Disable Time	t_{DF}		60		60	ns
Output Hold Time	t_{OH}	0		0		ns

TIMING DIAGRAM



13

MB 831000 ROM CODE DATA INPUT METHOD

Fujitsu's preferred method of receiving ROM Code Data is in the form of Programmed EPROMs or Magnetic Tapes.
Fujitsu produces the Masks in accordance with the Data in received EPROMs or Magnetic Tapes using Fujitsu computer systems.

MASK ROM CODE DATA RELEASE BY EPROMS:

- 128K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use 8 pcs of MBM 27128 or equivalent and program data of 8 address blocks (Address 0 to 16 K, 16 K to 32 K, 32 K to 48 K, 48 K to 64 K, 64 K to 80 K, 80 K to 96 K, 96 K to 112 K and 112 K to 128 K) of MB 831000 to each MBM 27128 EPROM. Fujitsu requires 3 sets, total 24 pcs, of such programmed EPROMs. (Two sets, total 16 pcs, are acceptable.)
In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (8 pcs) for supplying customer ROM Data Code verification.

MSB — LSB

A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	MBM 27128 (No. 1: 0 to 16 K)													
0	0	1	MBM 27128 (No. 2: 16 K to 32 K)													
0	1	0	MBM 27128 (No. 3: 32 K to 48 K)													
0	1	1	MBM 27128 (No. 4: 48 K to 64 K)													
1	0	0	MBM 27128 (No. 5: 64 K to 80 K)													
1	0	1	MBM 27128 (No. 6: 80 K to 96 K)													
1	1	0	MBM 27128 (No. 7: 96 K to 112 K)													
1	1	1	MBM 27128 (No. 8: 112 K to 128 K)													

- 256K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use 4 pcs of MBM 27C256 or equivalent and program data of 4 address blocks (Address 0 to 32K, 32K to 64K, 64K to 96K and 96K to 128K) of MB 831000 to each MBM 27C256 EPROM.
Fujitsu requires 3 sets, total 12 pcs, of such programmed EPROMs. (Two sets, total 8 pcs, are acceptable.)
In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (4 pcs) for supplying customer ROM Data Code verification.

MSB — LSB

A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	MBM 27C256 (No. 1: 0 to 32 K)														
0	1	MBM 27C256 (No. 2: 32 K to 64 K)														
1	0	MBM 27C256 (No. 3: 64 K to 96 K)														
1	1	MBM 27C256 (No. 4: 96 K to 128 K)														

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MASK ROM CODE DATA RELEASE BY MAGNETIC TAPES:

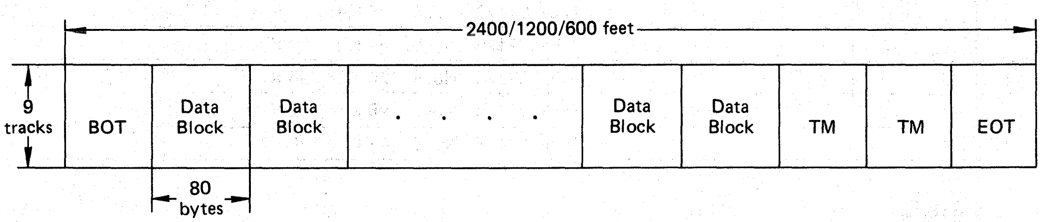
When the customer releases his Mask ROM Code Data in the form of Magnetic Tapes (MT), he should use tapes that can be used on IBM compatible equipment and meet the following requirements.

- Physical Requirements:

  1 Length : 2400 feet, 1200 feet, or 600 feet
  2 Width : 1/2 inch
  3 Track : 9 tracks
  4 Density : 800 BPI or 1600 BPI

- MT Format:

  1 Label : No tape mark on the header of tape
  2 Record Size : 80 bytes/record
  3 Block Size : Single record/block
  4 File : Single file/volume
  5 Code Used : EBCDIC code



Note: BOT : Beginning of Tape
EOT : End of Tape
TM : Tape mark

Data Block Format:

Row Number	1 – 9	10 – 15	16 – 19	20 – 67	68 – 72	73 – 80
	Undefined Field	Address Field (1 Head Address)	Undefined Field	Data Field (16 words)	Undefined Field	Sequence
Number of Byte	9 bytes	6 bytes	4 bytes	48 bytes	5 bytes	8 bytes

Note: 1 byte/row

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Undefined Filed (Row 1~9/Row 16~19/Row 68~72):

In this field, blanks (ƀ) should be recorded.

Address Field (Row 10~15):

In the address field, the header address of the 16-word data that follow the address field should be recorded in the form of a five-digit hexadecimal number following a symbol "#". The correspondence of actual binary address to this hex address is shown in the following example.

	MSB																LSB
Address Bit	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Binary Address	0	0	0	1	1	1	0	1	1	1	0	0	1	0	0	1	0
Hex Address	0	3				B				9				2			
Recorded Form	#03B92																

Data Field (Row 20 ~ 67):

In this field, 16-word data with 16 successive addresses should be recorded in the form of two-digit hexadecimal numbers followed by a blank (ƀ). (The header data is for the address recorded in the address field.) The correspondence of actual binary data to this hex data is shown in the following example.

Data Bit	08	07	06	05	04	03	02	01
Binary Data	1	1	1	1	0	0	1	0
Hex Data	F				2			
Recorded Data	F2ƀ							

Sequence Number field (Row 73 ~ 80)

In this field, the sequence number of each record (data block) should be recorded in the form of an eight-digit decimal number, which must be counted up by tens. All digits to the left of the most significant digit should be zeros, not blanks. Refer to the following example.

Address	Data				Sequence No.
10 15	20 22	23 25		65 67	73 80
#03B92	F2ƀ	A0ƀ	· · · ·	07ƀ	00000010

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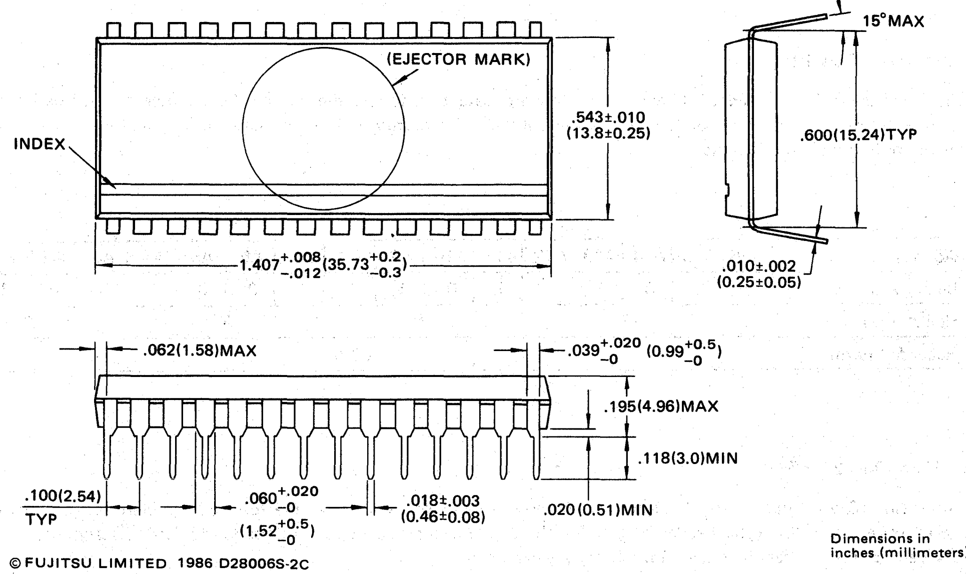
PACKAGE DIMENSIONS



13

FUJITSU

CMOS 2M-BIT MASK-PROGRAMMABLE READ ONLY MEMORY

MB832000

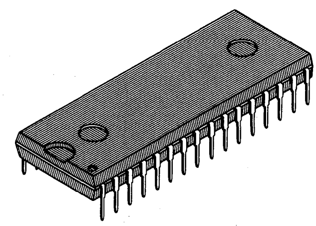
April 1988
Edition 1.0

2M-BIT(262,144 x 8) CMOS READ ONLY MEMORY

The Fujitsu MB832000 is a CMOS Si-gate mask-programmable static read only memory organized as 262,144 words by 8 bits.

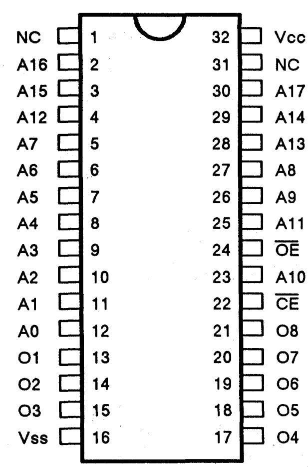
The MB832000 has TTL-compatible I/O and 3-state output level with fully-static operation (i.e. no need of clock signal) and a single +5V power supply is required. Also, the MB832000 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

- Organization: 262,144 words x 8 bits
- Access time: 200 ns
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state ouput
- Single +5V power supply
- Power dissipation:
  220 mW max. (Active)
  16.5mW max. (Standby, TTL input level)
  275 µW max. (Standby, CMOS input level)
- 32-pin DIP(Pin compatible with MBM27C1001)



PLASTIC PACKAGE
DIP-32P-M01

PIN ASSIGNMENT
MB832000



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

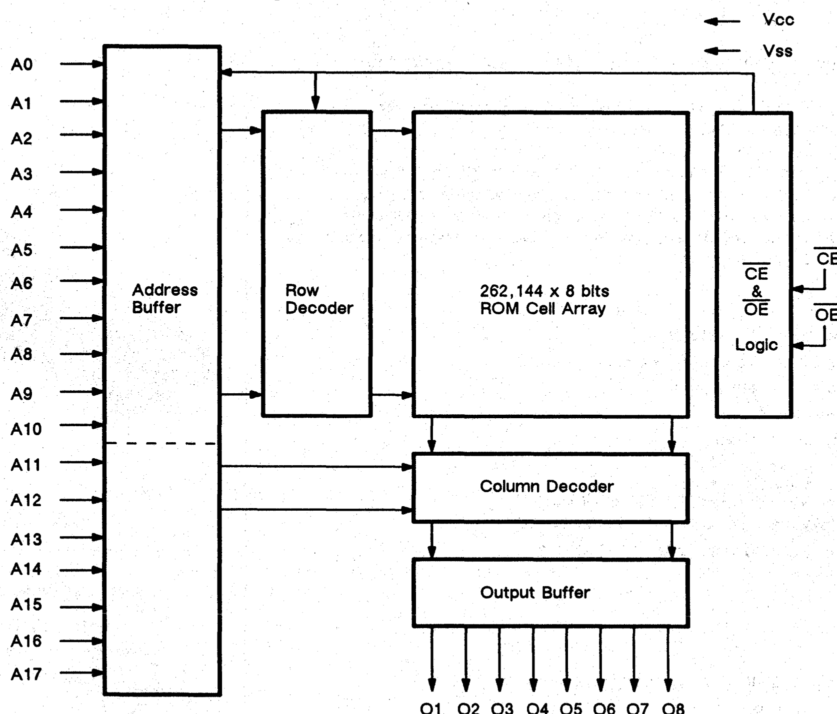
ABSOLUTE MAXIMUM RATINGS (see NOTE)

(Referenced to GND)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.5 to VCC+0.5	V
Output Voltage	V_{OUT}	-0.5 to VCC+0.5	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature Range	T_{STG}	-45 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1–MB832000 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	Mode	Output	Power Mode
H	X	Not Selected	High-Z	Standby
L	H	Not Selected	High-Z	Active
L	L	Selected	Data Out	Active

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CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (VOUT=0V)	COUT			15	pF
Input Capacitance (VIN=0V)	CIN			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Input Low Voltage	VIL	-0.3		0.8	V
Input High Voltage	VIH	2.2		VCC+0.3	V
Ambient Temperature	TA	0		70	°C

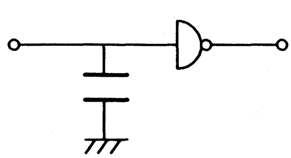
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Active Supply Current	$\overline{CE}$=VIL, Min. Cycle	ICC			40	mA
Standby Supply Current	$\overline{CE}$=VIH	ISB1			3	mA
	$\overline{CE}$=VIH=VCC,VIN=VSS or VCC	ISB2			50	µA
Input Leakage Current	VIN=0 to VCC	ILI	-10		10	µA
Output Leakage Current	$\overline{CE}$=VIH, $\overline{OE}$=VIH	ILO	-10		10	µA
Output High Voltage	IOH=-400µA	VOH	2.4			V
Output Low Voltage	IOL=2.1mA	VOL			0.4	V

Fig. 2 - AC TEST CONDITION

- Input Pulse Level : 0.6 to 2.4V
- Input Pulse Rise and Fall Time : tT=5ns
- Timing Reference Levels : Input VIL=0.8V, VIH=2.2V
  Output VOL=0.8V, VOH=2.2V
- Output Load : 1 TTL Gate and 100pF



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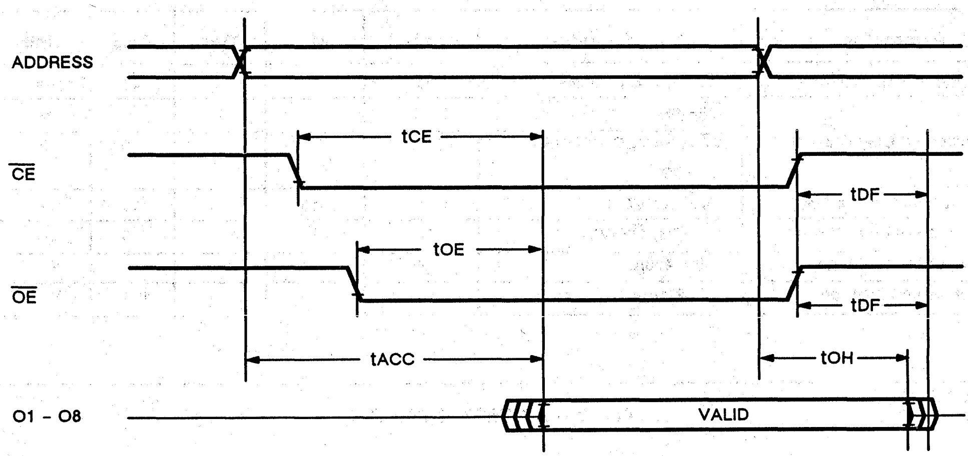
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Address Access Time	tACC	$\overline{CE}$=$\overline{OE}$=VIL			200	ns
$\overline{CE}$ Access Time	tCE	$\overline{OE}$=VIL			200	ns
$\overline{OE}$ Access Time	tOE	Note 1			100	ns
Output Disable Time	tDF	Note 2			60	ns
Output Hold Time	tOH	$\overline{CE}$=$\overline{OE}$=VIL	0			ns

Note 1: $\overline{OE}$ may be delayed up to (tACC-tOE) after the falling edge of $\overline{CE}$ without impact on tACC.
Note 2: tDF is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs earlier.

TIMING DIAGRAM



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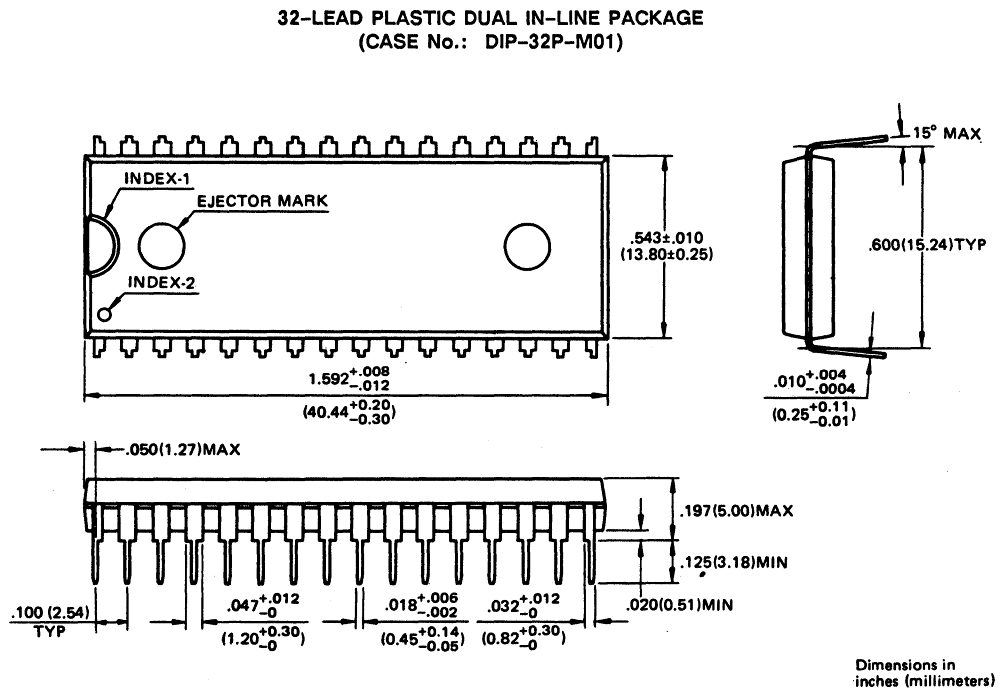
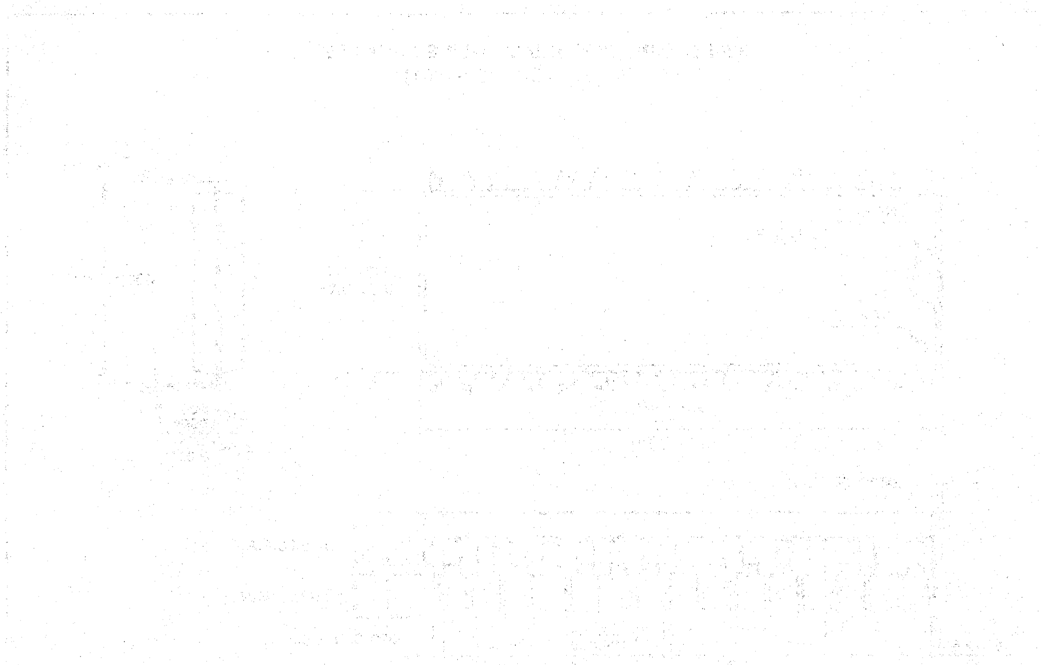
PACKAGE DIMENSIONS





13

FUJITSU

CMOS 4M-BIT MASK-PROGRAMMABLE READ ONLY MEMORY

MB834100

November 1987
Edition 2.0

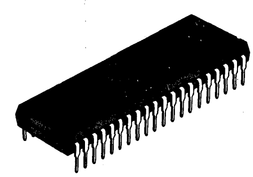
4M-BIT (256K x 16, 512K x 8) CMOS READ ONLY MEMORY

The Fujitsu MB 834100 is a CMOS Si-gate mask-programmable static read only memory organized as 262,144 words by 16 bits. (524,288 words by 8 bits).

The MB 834100 has TTL-compatible I/O and 3-state output level with fully-static operation (i.e. no need of clock signal) and single +5 V power supply. Also, the MB 834100 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

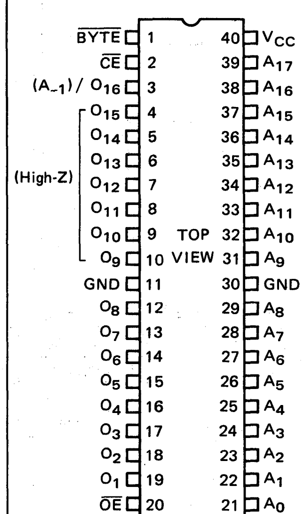
Memory organization of MB 834100 in changeable between 16 bits and 8 bits. (ex. The system using 8 bits CPU and 16 bits CPU can use common data on the same chip.)

- Organization: 262,144 words x 16 bits
  : 524,288 words x 8 bits
- Access time : 250 ns max.
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5 V power supply
- Power dissipation : 275 mW max. (Active)
  5.5 mW max. (Standby, TTL input level)
  275 μW max. (Standby, CMOS input level)
- JEDEC Standard 40-pin Plastic DIP



PLASTIC PACKAGE
DIP-40P-M01

PIN ASSIGNMENT



( ) is applied to 8 bits.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0*	V
Input Voltage	V_{IN}	-0.5 to V_{CC}+0.5*	V
Output Voltage	V_{OUT}	-0.5 to V_{CC}+0.5*	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature Range	T_{STG}	-45 to +125	°C

* Referenced to GND

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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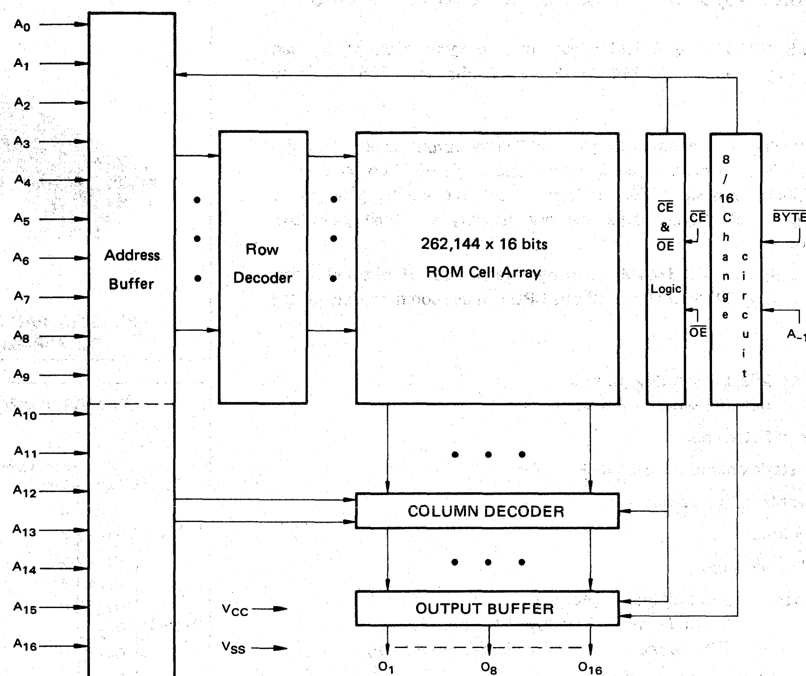
Fig. 1 — MB 834100 BLOCK DIAGRAM



OUTPUT MODE SELECTION

A_{-1}	$\overline{BYTE}$	O_1 to O_8	O_9 to O_{15}	O_{16}
X	H	D_1 to D_8	D_9 to D_{15}	D_{16}
L	L	D_1 to D_8	High-Z	A_{-1}
H	L	D_9 to D_{15}	High-Z	A_{-1}

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUT	POWER DISSIPATION MODE
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	X	NOT SELECTED	HIGH-Z	ACTIVE
L	L	SELECTED	D_{OUT}	ACTIVE

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CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}			15	pF
Input Capacitance (V_{IN} = 0 V)	C_{IN}			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC} +0.3	V
Ambient Temperature	T_A	0		70	°C

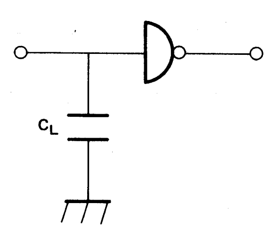
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Active Supply Current	$\overline{CE}$ = V_{IL}, Minimum Cycle	I_{CC}		50	mA
Standby Supply Current	$\overline{CE}$ = V_{IH}	I_{SB1}		1	mA
	$\overline{CE}$ = V_{CC}, V_{IN} = GND or V_{CC}	I_{SB2}		50	μA
Input Leakage Current	V_{IN} = 0 to V_{CC}	I_{LI}	-10	10	μA
Output Leakage Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}	$I_{LI/O}$	-10	10	μA
Output High Voltage	I_{OH} = -400 μA	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}		0.4	V

Fig. 2 — AC TEST CONDITION

- Input Pulse Level : 0.6 to 2.4 V
- Input Pulse Rise and Fall Time : t_T = 5 ns
- Timing Reference Levels : Input : V_{IL} = 0.8 V, V_{IH} = 2.2 V
  Output : V_{OL} = 0.8V, V_{OH} = 2.2 V
  : 1 TTL Gate and 100 pF
- Output Load



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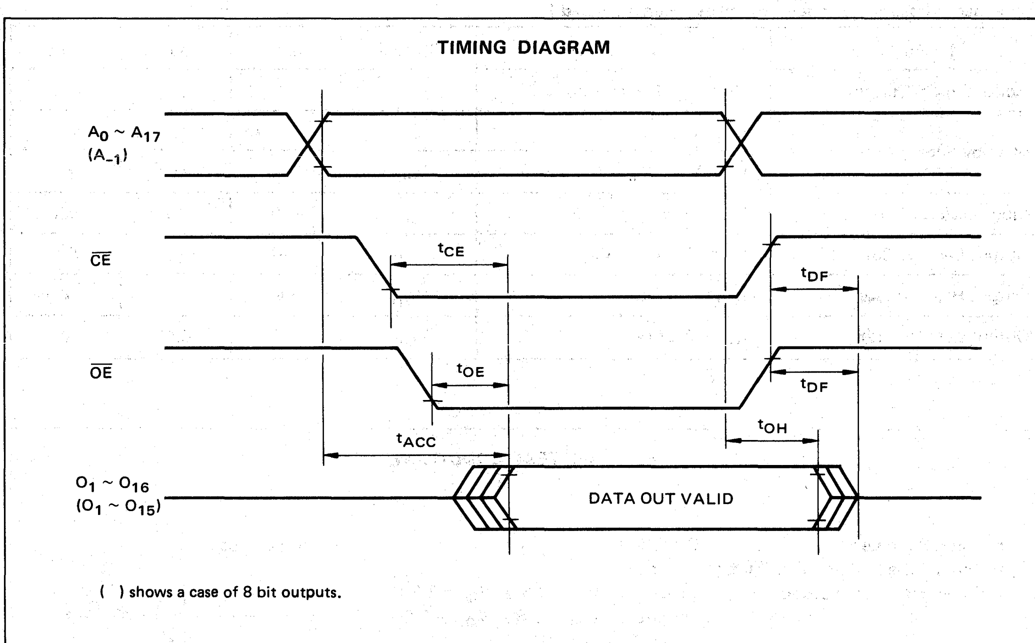
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	t_{ACC}		250	ns
Chip Enable Access Time	$\overline{OE} = V_{IL}$	t_{CE}		250	ns
Output Enable Access Time	*1	t_{OE}		100	ns
Output Disable Time	*2	t_{DF}		60	ns
Output Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	t_{OH}	0		ns

*1: Maximum $\overline{OE}$ delay which does not affect t_{ACC} is $t_{ACC} - t_{OE}$.

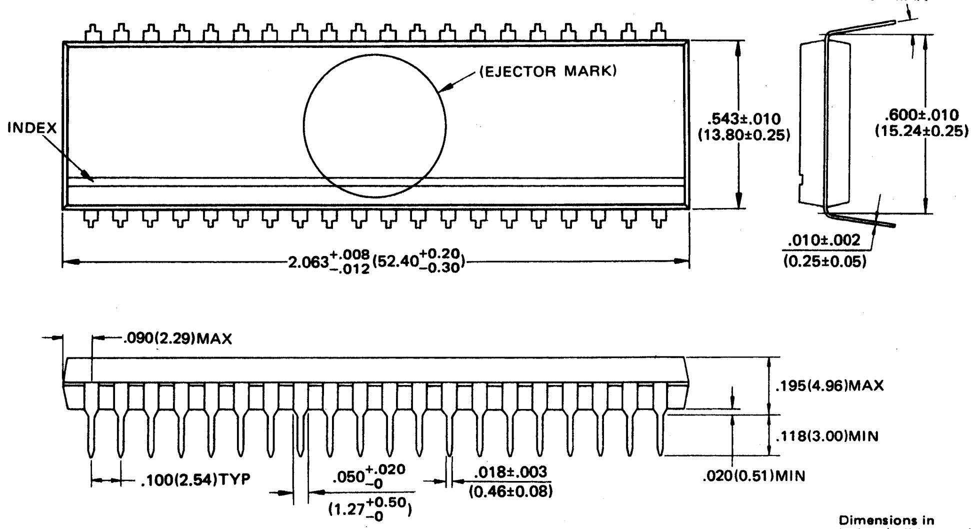
*2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to High earlier.



13

PACKAGE DIMENSIONS

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40P-M01)



Dimensions in inches (millimeters)

FUJITSU

CMOS 4M-BIT MASK PROGRAMMABLE READ ONLY MEMORY

MB834000-20
MB834000-25

April 1988
Edition 1.0

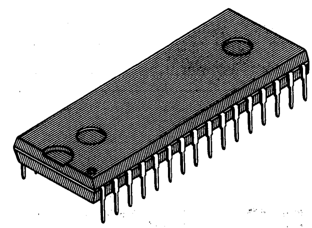
4M-BIT (512K x 8) CMOS READ ONLY MEMORY

The Fujitsu MB834000 is a CMOS Si-gate mask-programmable static read only memory organized as 524,288 words by 8 bits.

The MB834000 has TTL-compatible I/O 3-state ouput level with fully-static operation (i.e. no need of clock signal) and single +5V power supply.

Also, the MB834000 is designed for applications such as character generator or program strage which require large memory capacity and high-speed/low-power operation.

- Organization: 524,288 words x 8 bits
- Access time: 250ns max.
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5 V power supply
- Power dissipation: 275 mW max. (Active)
  5.5 mW max. (Standby, TTL input level)
  275 μW max. (Standby, CMOS input level)
- 32-pin Plastic DIP : Suffix-P



PLASTIC PACKAGE
DIP-32P-M01

PIN ASSIGNMENT

(TOP VIEW)

NC	1	32	Vcc
A16	2	31	A18
A15	3	30	A17
A12	4	29	A14
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CE}$
A0	12	21	O8
O1	13	20	O7
O2	14	19	O6
O3	15	18	O5
Vss	16	17	O4

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0*	V
Input Voltage	V_{IN}	-0.5 to V_{CC} +0.5*	V
Output Voltage	V_{OUT}	-0.5 to V_{CC} +0.5*	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature Range	T_{STG}	-45 to +125	°C

* Referenced to GND

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Active Supply Current	$\overline{CE}$=V_{IL}, Minimum Cycle	I_{CC}			50	mA
Standby Supply Current	$\overline{CE}$=V_{IH}	I_{SB1}			3	mA
	$\overline{CE}$=V_{CC}=V_{IH}, GND or V_{CC}	I_{SB2}			50	µA
Input Leakage Current	V_{IN}=0 to V_{CC}	I_{LI}	−10		10	µA
Output Leakage Current	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IH}	$I_{LI/O}$	−10		10	µA
Output High Voltage	I_{OH}=−400µA	V_{OH}	2.4			V
Output Low Voltage	I_{OL}=2.1mA	V_{OL}			0.4	V

Fig. 2 – AC TEST CONDITION

- Input Pulse Level : 0.6 to 2.4V
- Input Pulse Rise and Fall Time : t_T=5ns
- Timing Reference Levels : Input : V_{IL}=0.8V, V_{IH}=2.2V
  Output : V_{OL}=0.8V, V_{OH}=2.2V
- Output Load : 1 TTL Gate and 100pF

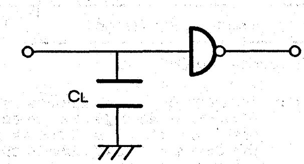


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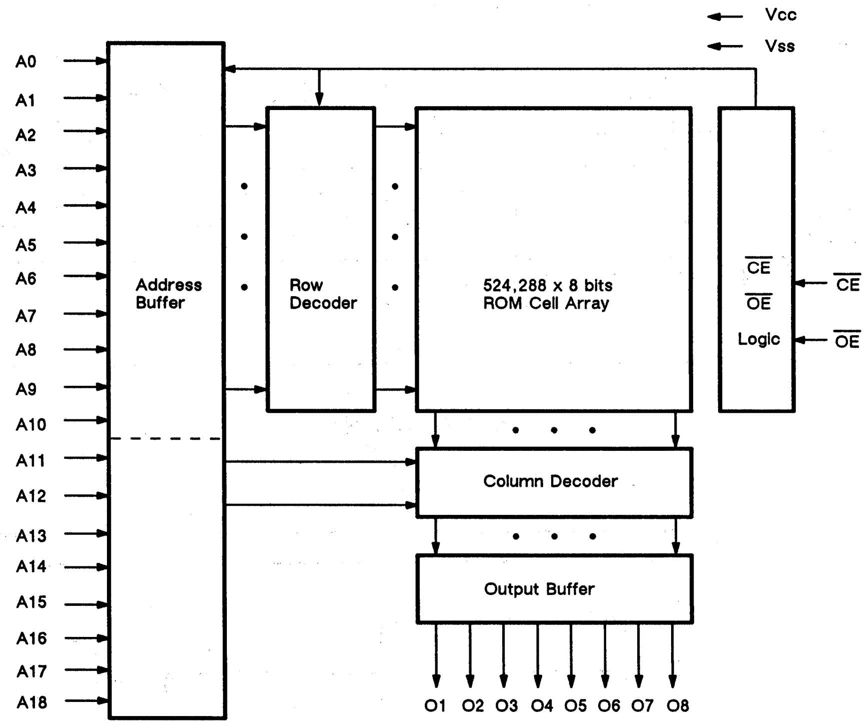
Fig. 1-MB834000 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	Mode	Output	Power Dissipation Mode
H	X	Not Selected	High-Z	Standby
L	H	Not Selected	High-Z	Active
L	L	Selected	D_{OUT}	Active

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT}=0 V)	C_{OUT}			15	pF
Input Capacitance (V_{IN}=0 V)	C_{IN}			10	pF

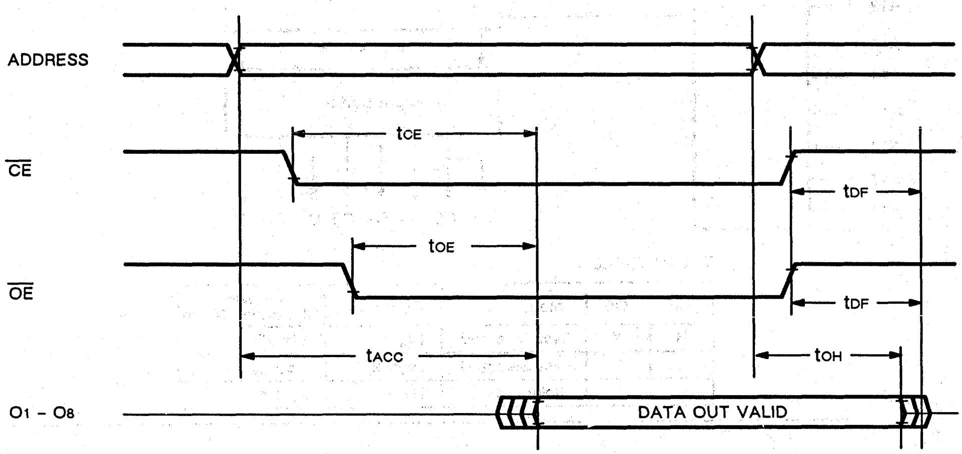
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	t_{ACC}		250	ns
Chip Enable Access Time	$\overline{OE}$=V_{IL}	t_{CE}		250	ns
Output Enable Access Time	Note 1	t_{OE}		100	ns
Output Disable Time	Note 2	t_{DF}		60	ns
Output Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	t_{OH}	0		ns

Note 1: Maximum $\overline{OE}$ delay which does not affect t_{ACC} is $t_{ACC} - t_{OE}$.
Note 2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to High earlier.

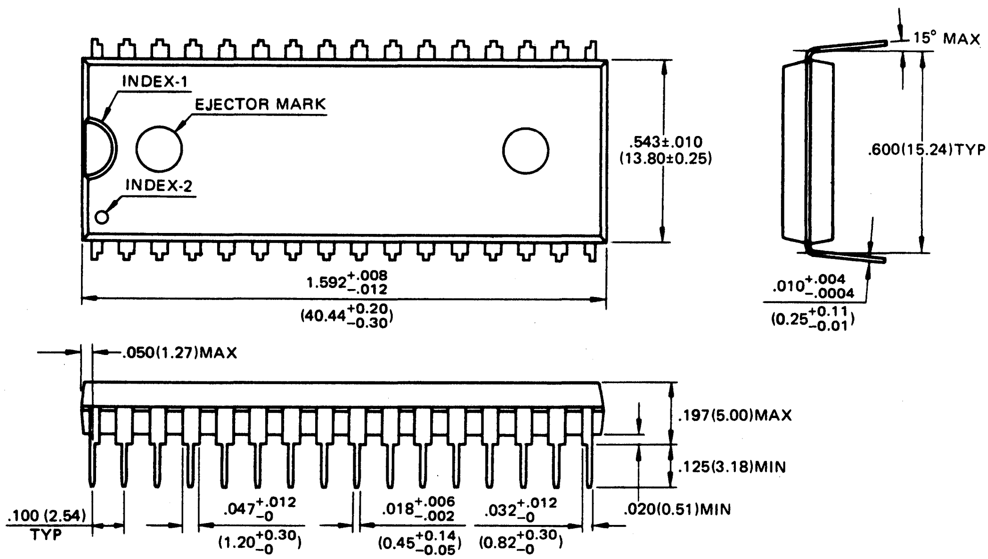
TIMING DIAGRAM



13

PACKAGE DIMENSIONS

32-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. DIP-32P-M01)



Dimensions in inches (millimeters)

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13

FUJITSU

CMOS 4M-BIT MASK PROGRAMMABLE READ ONLY MEMORY

MB834200

April 1988
Edition 1.0

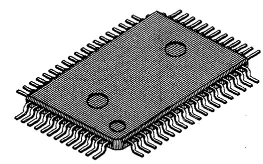
4M-BIT (256K x 16, 512K x 8) CMOS READ ONLY MEMORY

The Fujitsu MB834200 is a CMOS Si-gate mask-programmable static read only memory organized as 262,144 words by 16 bits. (524,288 words by 8 bits).

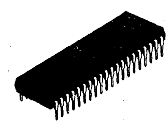
The MB834200 has TTL-compatible I/O 3-state output level with fully-static operation (i.e. no need of clock signal) and single +5V power supply.
Also, the MB834200 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

Memory organization of MB834200 is changeable between 16 bits and 8 bits. (ex. The system using 8 bits CPU and 16 bits CPU can use common data on the same chip.)

- Organization: 262,144 words x 16 bits
  524,288 words x 8 bits
- Access time: 250ns max.
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5 V power supply
- Power dissipation: 275 mW max. (Active)
  5.5 mW max. (Standby, TTL input level)
  275 µW max. (Standby, CMOS input level)
- Standard 40-pin Plastic DIP
- 64-pin Plastic Flat Package

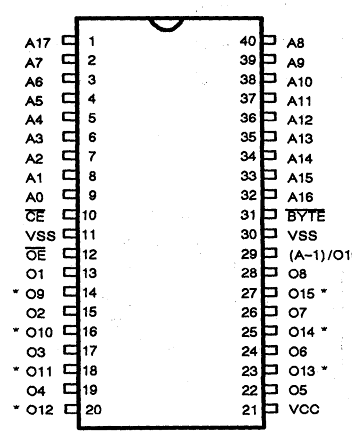


PLASTIC PACKAGE
FPT-64P-M01



PLASTIC PACKAGE
DIP-40P-M01

PIN ASSIGNMENT
(TOP VIEW)



* is applied to 8 bits.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

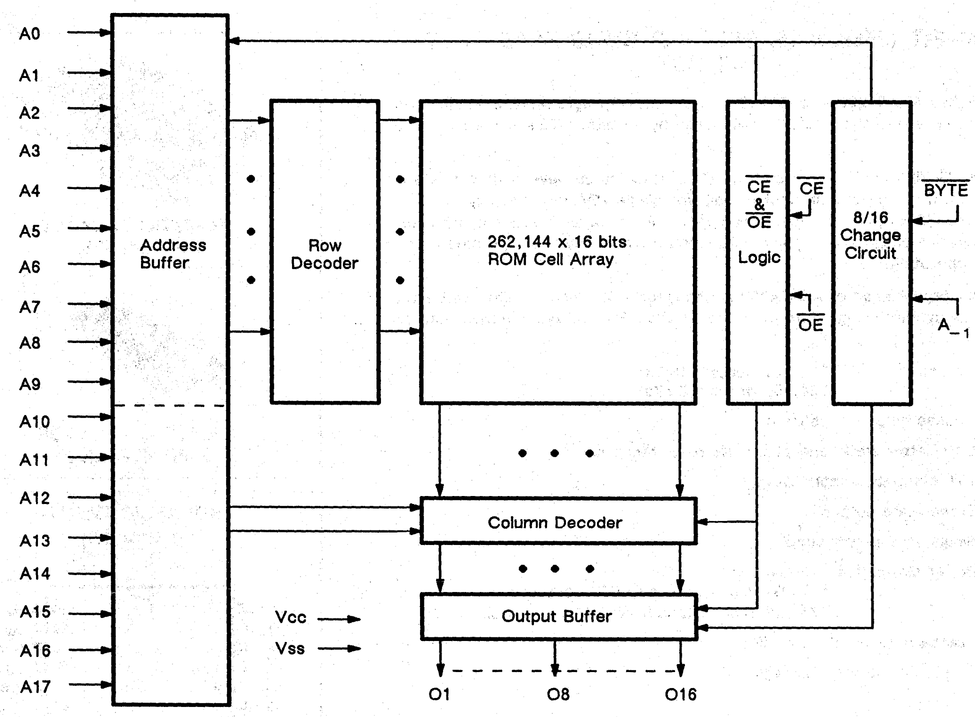
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0*	V
Input Voltage	V_{IN}	-0.5 to V_{CC} +0.5*	V
Output Voltage	V_{OUT}	-0.5 to V_{CC} +0.5*	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature Range	T_{STG}	-45 to +125	°C

* Referenced to GND

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1-MB834200 BLOCK DIAGRAM



OUTPUT SELECTION MODE

A_{-1}	$\overline{BYTE}$	O_1 to O_8	O_9 to O_{15}	O_{16}
X	H	D_1 to D_8	D_9 to D_{15}	D_{16}
L	L	D_1 to D_8	High-Z	A_{-1}
H	L	D_9 to D_{16}	High-Z	A_{-1}

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	Mode	Output	Power Dissipation Mode
H	X	Not Selected	High-Z	Standby
L	X	Not Selected	High-Z	Active
L	L	Selected	D_{OUT}	Active

13

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT}=0 V)	C_{OUT}			15	pF
Input Capacitance (V_{IN}=0 V)	C_{IN}			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient Temperature	T_A	0		70	°C

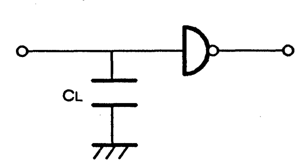
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Active Supply Current	$\overline{CE}=V_{IL}$, Minimum Cycle	I_{CC}			50	mA
Standby Supply Current	$\overline{CE}=V_{IH}$	I_{SB1}			1	mA
	$\overline{CE}=V_{CC}=V_{IH}$, GND or V_{CC}	I_{SB2}			50	μA
Input Leakage Current	V_{IN}=0 to V_{CC}	I_{LI}	-10		10	μA
Output Leakage Current	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IH}$	$I_{LI/O}$	-10		10	μA
Output High Voltage	I_{OH}=-400μA	V_{OH}	2.4			V
Output Low Voltage	I_{OL}=2.1mA	V_{OL}			0.4	V

Fig. 2 - AC TEST CONDITION

- Input Pulse Level : 0.6 to 2.4V
- Input Pulse Rise and Fall Time : t_T=5ns
- Timing Reference Levels : Input : V_{IL}=0.8V, V_{IH}=2.2V
  Output : V_{OL}=0.8V, V_{OH}=2.2V
- Output Load : 1 TTL Gate and 100pF



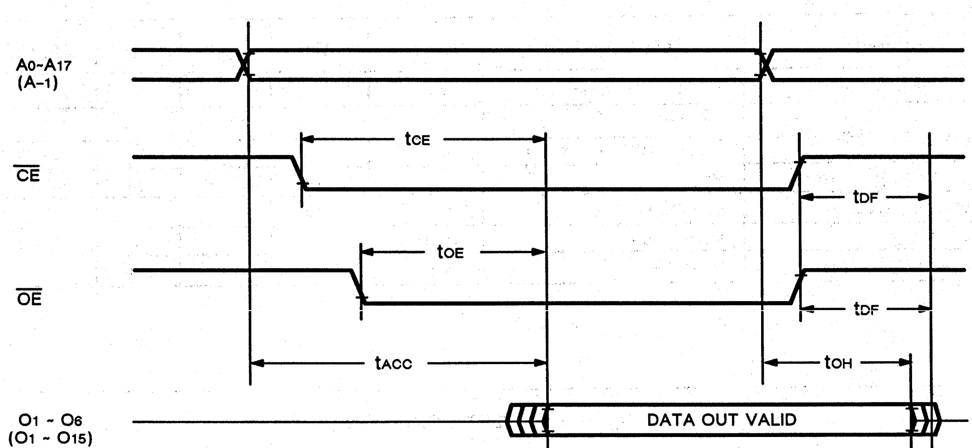
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	t_{ACC}		250	ns
Chip Enable Access Time	$\overline{OE}=V_{IL}$	t_{CE}		250	ns
Output Enable Access Time	* 1	t_{OE}		100	ns
Output Disable Time	* 2	t_{DF}		60	ns
Output Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	t_{OH}	0		ns

* 1: Maximum $\overline{OE}$ delay which does not affect t_{ACC} is $t_{ACC} - t_{OE}$.
* 2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to High earlier.

TIMING DIAGRAM

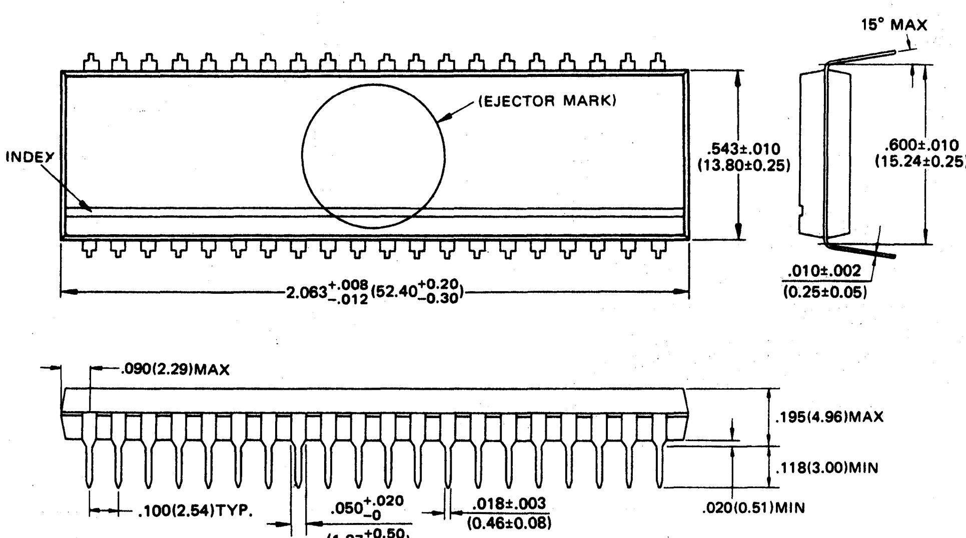


( ) shows a case of 8 bit outputs.

13

PACKAGE DIMENSIONS

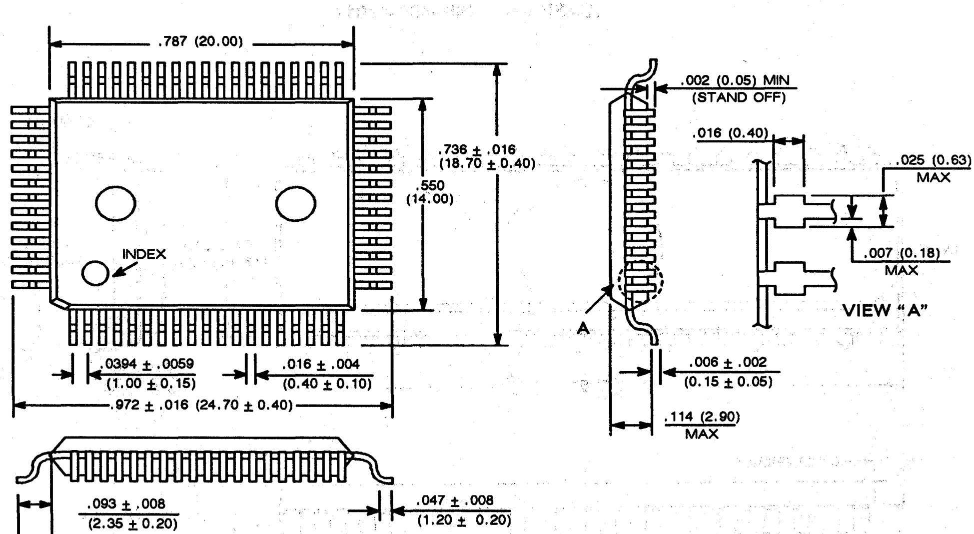
40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40P-M01)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

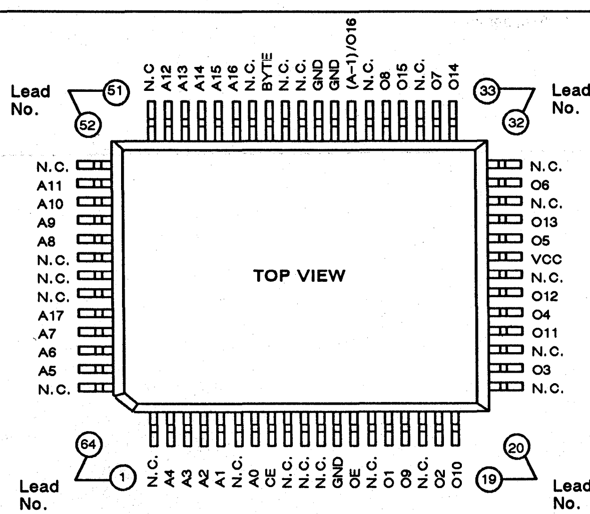
64-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-64P-M01)



Dimensions in inches (millimeters)

F64005S-5C

PIN ASSIGNMENT



Section 14

Quality and Reliability

14

14

Quality Control At Fujitsu

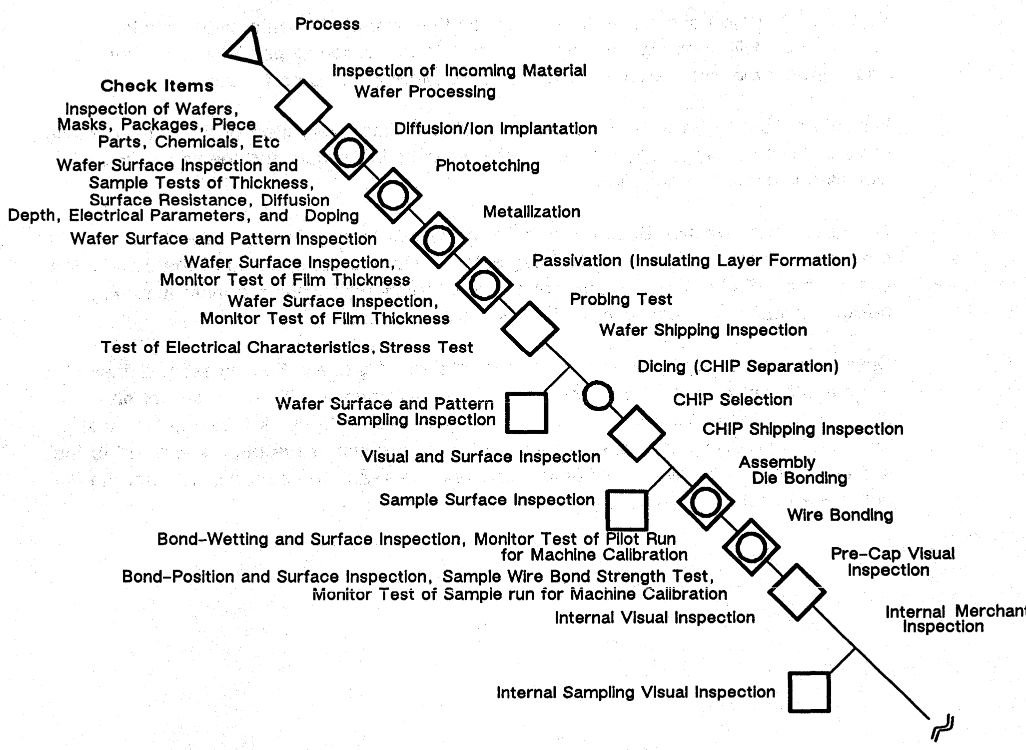
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end on the Fujitsu factory floor. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

Quality Control Flowchart



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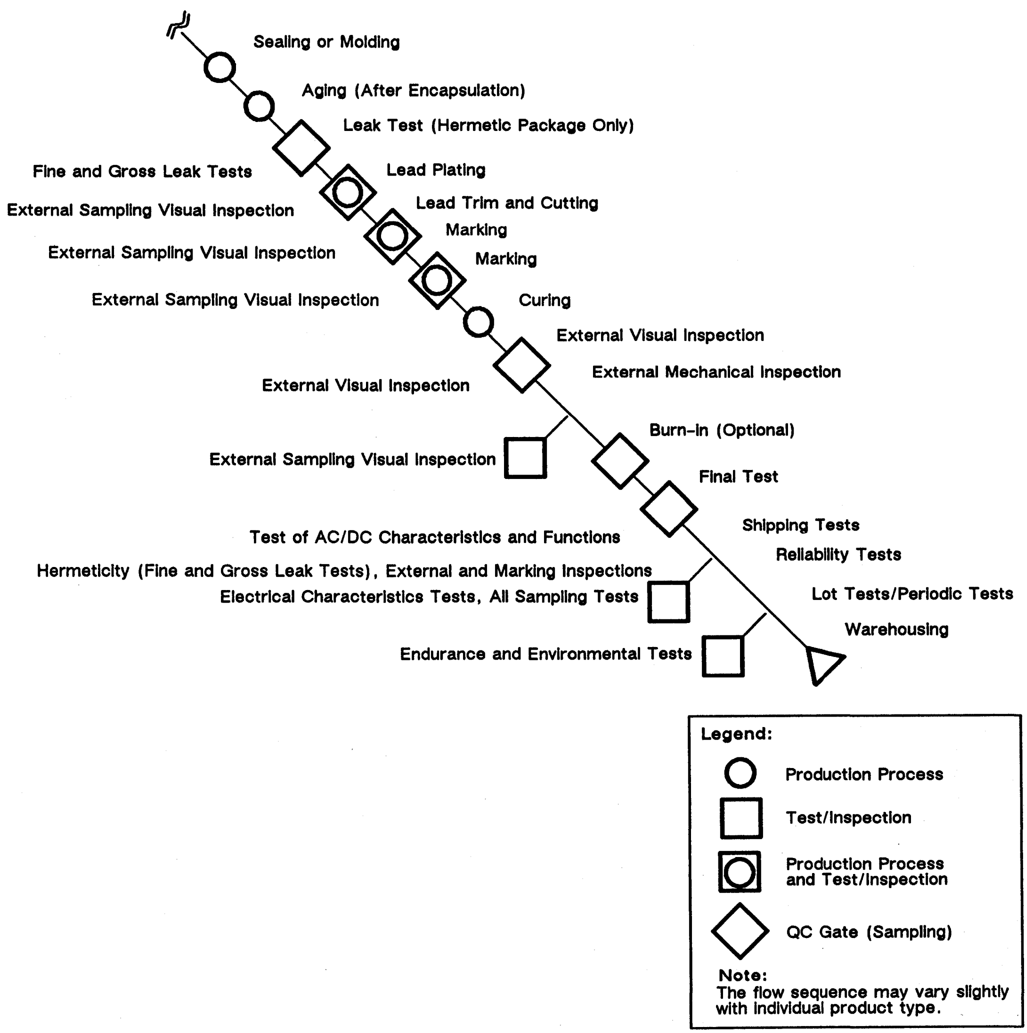
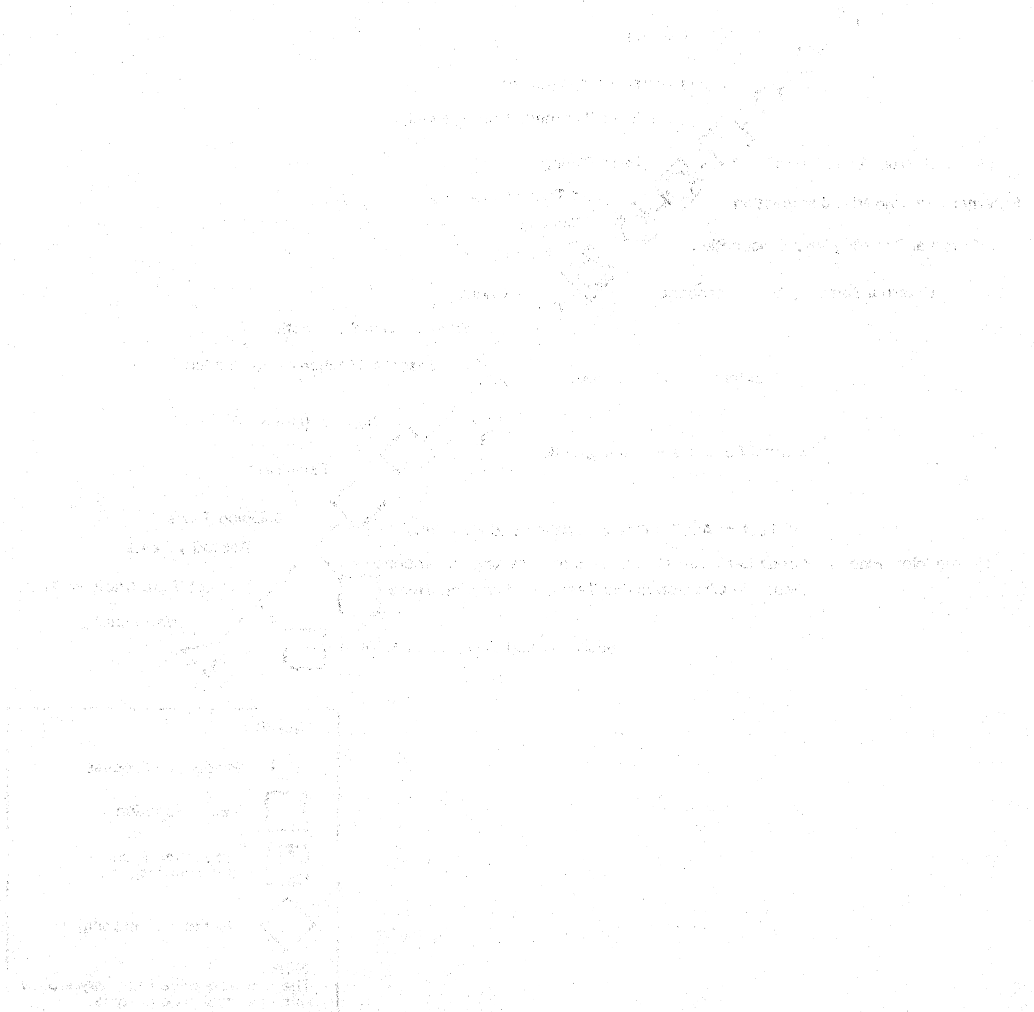
Quality Control Flowchart (Continued)



14

14



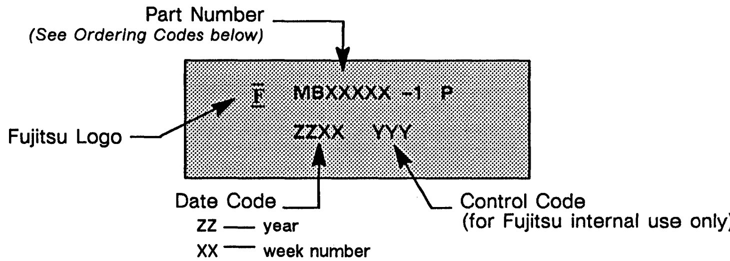
Section 15

Ordering Information

15

Ordering Information

Product Marking



Note: Marking formats may vary, depending on the product. The country of origin appears on all finished parts.

Ordering Codes

MB XXXXX -1 P

- **P** — Package Code *(See Package Codes below)*
- **-1** — Speed Designator *(When applicable)*
- **XXXXX** — Device Type
- **MB** — Manufacturer Designator
  - **MB** Device type is designed by FJ
  - **MBL** Device type is single source contracted by FJ

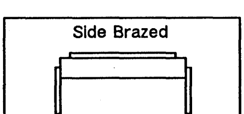
Note: Regarding ordering code, please contact your Fujitsu sales office for more information.

Package Codes

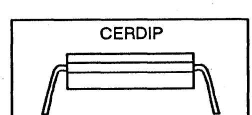
Ceramic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	TV,CV
PGA (Pin Grid Array)	CR
DIP (Side Brazed) [1]	C
DIP (CERDIP) [2]	Z
Shrink DIP	CSH
Flatpack	CF
SOJ (Single Outline Junction)	CJ

Plastic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	PV
PLCC (Leaded Chip Carrier)	PD
PGA (Pin Grid Array)	PR
DIP (Dual In-line Package)	P,M
Shrink DIP	PSH
Flatpack	PF
Single In-line, Straight Leads	PS
Single In-line, Zig-zag Leads	PSZ,PZ
SOJ (Single Outline Junction)	PJ

1



2



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Section 16

Sales Information

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Introduction to Fujitsu

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly-owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to include one research and development division, two marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The research and development division, Advanced Products Division (APD), using US-based engineering, has jointly developed RISC for Sun Microsystems and Ethernet®, a chip set used in local area networks. APD also markets AFP, an adaptive filter processor, and EtherStar™, the first VLSI device to integrate both StarLAN™ and Ethernet protocols into one device.

The Microwave and Optoelectronics Division (MOD) markets GaAs, FETs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD).

Fujitsu Microelectronics, Inc. (Continued)

Memory and programmable devices marketed by ICD include the following:

DRAMs
EPROMs
EEPROMs
NOVRAMs
CMOS masked ROMs
CMOS SRAMs Bipolar PROMs
ECL RAMs
STRAMs (the first self-timed RAM)
High speed ECL
Linear ICs and transistors.

ASIC products offered by ICD include the following:

CMOS gate arrays Bipolar gate arrays
Standard cells.

Customer support and customer CAE training for ASIC designs are available through the following FMI design centers:

San Jose
Dallas
Atlanta
Chicago
Boston.

Microcomputer and communications products offered by ICD include the following:

4-bit MCUs
8- and 16-bit MPUs
SCSI and controllers
DSPs
Prescalers
PLLs.

Fujitsu Microelectronics, Inc. (Continued)

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, FMI opened the Gresham Manufacturing Division to manufacture ASIC products. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Components of America**, markets connectors, keyboards, plasma displays, relays, and hybrid ICs.

Fujitsu Mikroelektronik GmbH (European Sales Center)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a wholly-owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Europe. The wide range of ICs, LSI memories, microprocessors, and ASIC products are noted throughout Europe for design excellence and unmatched reliability. Branch offices are located in Munich, London, Paris, Stockholm, and Milan.

Fujitsu Microelectronics Ireland, Ltd. (European Production Center)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980 in the suburbs of Dublin as Fujitsu's European Production Center for integrated circuits. FME assembles DRAMs, EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd. (European Design Center)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with highly sophisticated CAD systems to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Pacific Asia Ltd. (Asian/Oceanian Sales Center)

Fujitsu Microelectronics Pacific Asia Ltd. (FMP) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

Headquarters Locations

WORLD HEADQUARTERS

Fujitsu Limited
Furukawa Sogo Bldg.
6-1 Marunouchi 2-chome
Chiyoda-ku, Tokyo 100
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Tel: 0118132163211
TWX: 781-228833

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San Jose, CA 95134-1804
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FAX: (408) 432-9044
TWX: 910-338-0190

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D-6000 Frankfurt 71
Federal Republic of Germany
Tel: 496966320
Telex: 441963
FAX: 069-6632122

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West Wing
66 Mody Road, Tsimshatsui East
Kowloon, Hong Kong
Tel: 85237320100
Telex: 31959 FUJIS HX
FAX: 3-7227984

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Sales Office Locations — USA

NORTHERN CALIFORNIA
Fujitsu Microelectronics, Inc.
10600 N. DeAnza Blvd.
Suite 225
Cupertino, CA 95014
Tel: (408) 996-1600
FAX: (408) 725-8746

SOUTHERN CALIFORNIA
Fujitsu Microelectronics, Inc.
Century Centre
2603 Main Street
Suite 510
Irvine, CA 92714
Tel: (714) 724-8777
FAX: (714) 724-8778

Fujitsu Microelectronics, Inc.
5330 Carroll Canyon Road
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San Diego, CA 92121
Tel: (619) 452-3717
FAX: (619) 587-0507

GEORGIA
Fujitsu Microelectronics, Inc.
3500 Parkway Lane
Suite 210
Norcross, GA 30092
Tel: (404) 449-8539
FAX: (404) 441-2016

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FAX: (312) 250-8591

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FAX: (617) 964-3301

MINNESOTA
Fujitsu Microelectronics, Inc.
3460 Washington Drive
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Eagan, MN 55122-1303
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FAX: (612) 454-0601

NEW JERSEY
Fujitsu Microelectronics, Inc.
Horizon Corporate Center
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FAX: (609) 727-9797

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FAX: (516) 361-6480

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Fujitsu Microelectronics, Inc.
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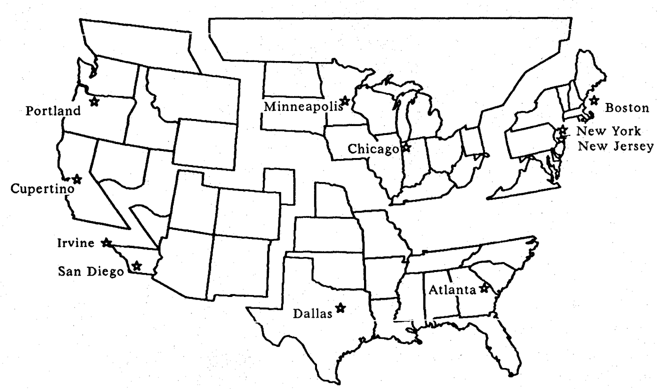
Lake Oswego, OR 97035-9998
Tel: (503) 684-4545
FAX: (503) 684-4547

TEXAS
Fujitsu Microelectronics, Inc.
14785 Preston Road
Suite 670
Dallas, TX 75240
Tel: (214) 233-9394
FAX: (214) 386-7917



Distributors — USA

Alabama
Marshall Industries
3313 S. Memorial Highway
Suite 121
Huntsville, AL 35801
(205) 881-9235

Arizona
Insight Electronics
1515 W. University Drive
Suite 103
Tempe, AZ 85281
(602) 829-1800

Marshall Industries
9830 S. 51st Street
Suite B121.
Phoenix, AZ 85044
(602) 496-0290

California
Image Electronics
9410 Topanga Canyon Road
Suite 103
Chatsworth, CA 91311
(818) 407-8850

Image Electronics
1342 Bell Avenue
Tustin, CA 92680
(714) 259-0900

Insight Electronics
28035 Dorothy Drive
Suite 220
Agoura, CA 91301
(818) 707-2100

Insight Electronics
3505 Cadillac Ave.
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Costa Mesa, CA 92626
(714) 556-6890

Insight Electronics
6885 Flanders Drive
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(619) 587-99757

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9710 Desoto Ave.
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One Morgan
Irvine, CA 92718
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Marshall Industries
336 Los Coches Stret
Milpitas, CA 95035
(408) 942-4600

Marshall Industries
3039 Kilgore Ave.
Rancho Cordova, CA 95670
(916) 635-9700

Marshall Industries
10105 Carroll Canyon Road
San Diego, CA 92131
(619) 578-9600

Merit Electronics
2362A Qume Drive
San Jose, CA 95131
(408) 434-0800

Western Microtechnology
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Orange, CA 92667
(714) 637-0200

Western Microtechnology
6837 Nancy Ridge Drive
San Diego, CA 92121
(619) 453-8430

Western Microtechnology
12900 Saratoga Ave.
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