April 1991
Edition 2.0

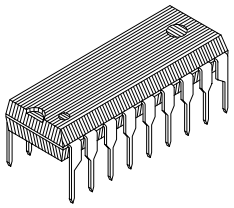
DATA SHEET

MB87017B
DTMF RECEIVER

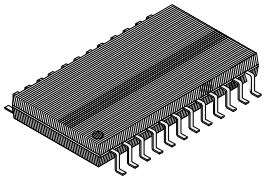
DUAL TONE MULTI FREQUENCY RECEIVER

The Fujitsu MB87017B is a one chip DTMF receiver with an input amplifier gain adjuster and low power consumption, integrating filter and decoder circuits. The MB87017B can select either automatic guard time setting mode or adjustable external guard time setting mode.

This circuit consists of SCFs (Switched Capacitor Filters) and decoders which convert 16 types of DTMF tone pairs into hexadecimal four-bit codes.



PLASTIC PACKAGE
(DIP-18P-M02)



PLASTIC PACKAGE
(FPT-24P-M02)

FEATURES

- All DTMF receiver functions are integrated on one chip
- Low power consumption
- Built-in input amplifier gain adjustment circuit
- Selectable automatic or adjustable external guard time setting modes

ABSOLUTE MAXIMUM RATINGS (see NOTE)

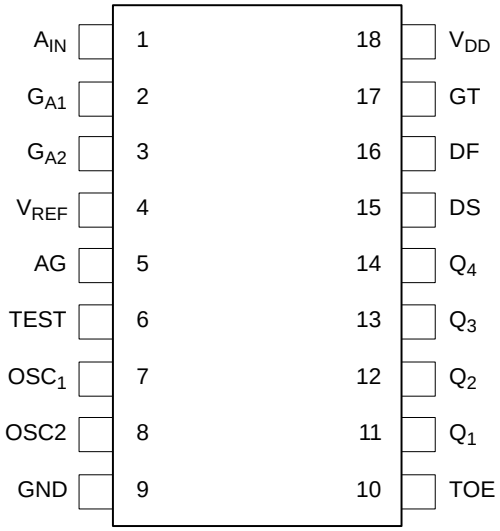
Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	+6.0	V
Analog Input Voltage	V_{AIN}	–0.3 to V_{DD} +0.3	V
Digital Input Voltage	V_{DIN}	–0.3 to V_{DD} +0.3	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

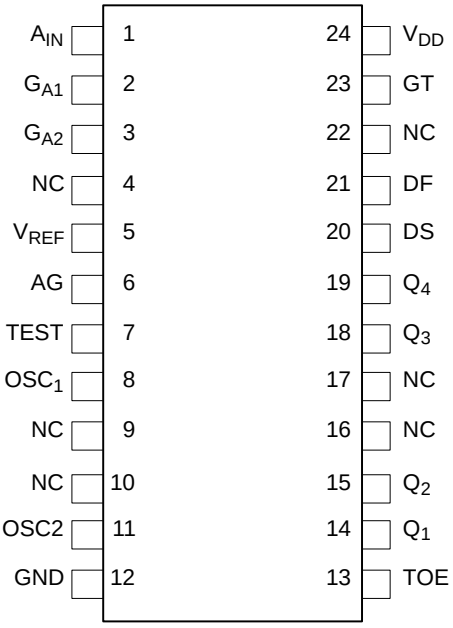
PIN ASSIGNMENT

(TOP VIEW)



(DIP-18P-M02)

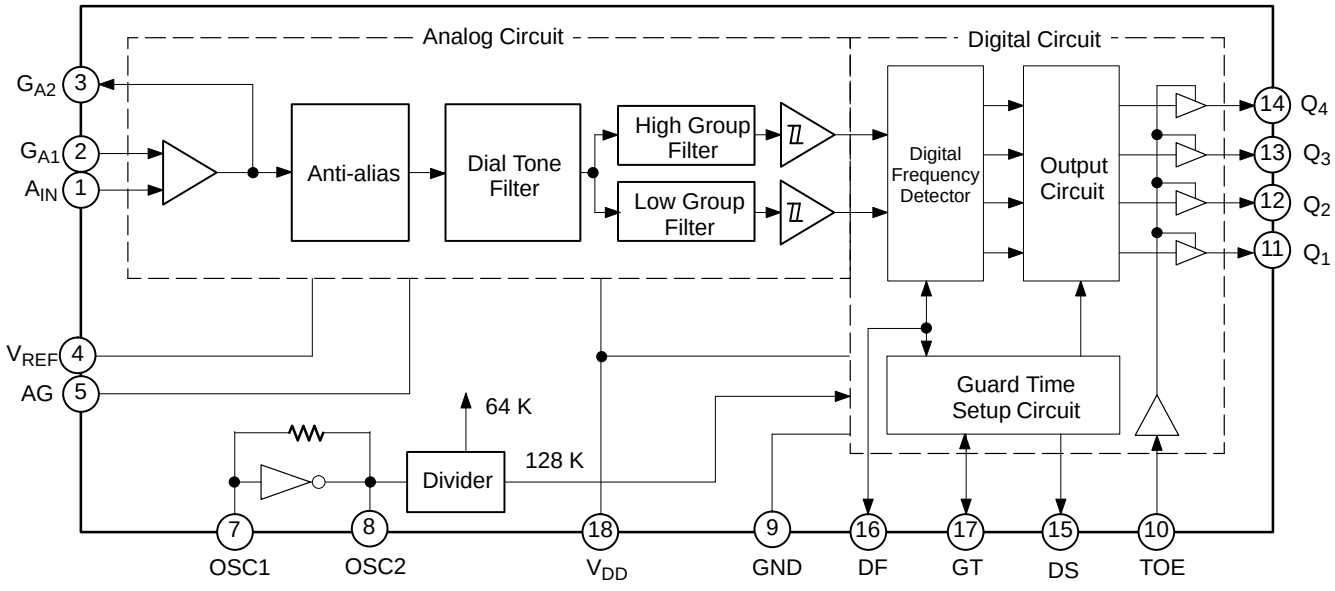
(TOP VIEW)



(FPT-24P-M02)

BLOCK DIAGRAM

(DIP PACKAGE)



PIN DESCRIPTION

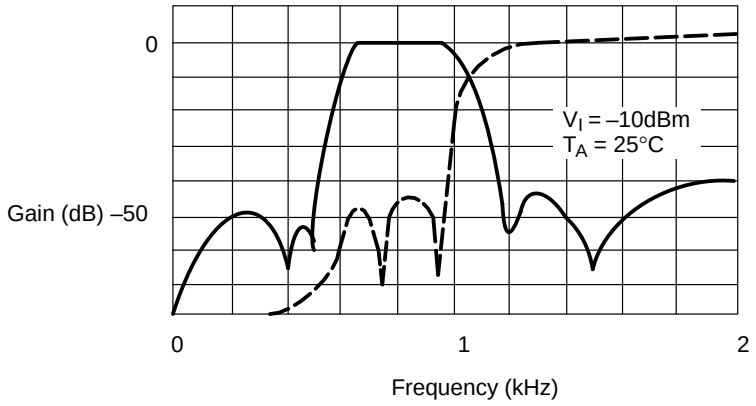
Pin No.		Symbol	I/O	Description
DIP	FPT			
1	1	A_{IN}	I	Analog input pin (non-inverted operational amplifier input)
2	2	G_{A1}	I	Operational amplifier gain adjustment pin 1 (inverted operand amplifier input). Operational amplifier gain adjustment pin 2 (operand amplifier output pin). * These pins are provided for operational amplifier gain adjustment. The polarity of G_{A1} is opposite to that of G_{A2}.
3	3	G_{A2}	O	
4	5	V_{REF}	O	Reference voltage output pin (1/2 V_{DD})
5	6	AG	–	Analog ground pin
6	7	TEST	–	Test pin. Usually set to ground level.
7	8	OSC1	I	Clock input pin.
8	11	OSC2	O	Clock output pin. * Connect a 3.5795MHz crystal between OSC1 and OSC2 pins.
9	12	GND	–	Ground pin
10	13	TOE	I	Three-state output enable pin. * Data from Q_1 to Q_4 may be output when this pin is set to “High”.
11 to 14	14, 15 18, 19	Q_1 to Q_4	O	Three-state data output pin.
15	20	DS	O	Signal detection pin. * This pin goes to “High” when a valid tone pair is received and decoded, and the data in the output data-bus is updated.
16	21	DF	O	Frequency detection pin. * This pin goes to “High” when a received tone pair is acknowledged as the valid DTMF signal frequency.
17	23	GT	O	Guard time mode select pin. * When GT pin is clamped to V_{DD}, automatic guard time setting circuit is selected; Guard Time Present (GTP) and Guard Time Absent (GTA) are set to 20 milliseconds. * See functional descriptions on page 5. * When GT pin exceeds 1/2V_{DD}, DS pin outputs high level. When GT pin is less than 1/2V_{DD}, DS pin outputs low level.
18	24	V_{DD}	–	Positive supply voltage pin. * The voltage must be +5 $\pm$ 5%.
–	4, 9 10, 16 17, 22	NC	–	No connection

FUNCTIONAL DESCRIPTIONS

FILTER

The filters consist of 3 sixth-order SCFs. The dial tone removal filter (including the 60Hz filter) output is connected to the individual hysteresis comparators through the low group and high group filters.

In the figure below, the solid line shows the characteristics of the low group filter while the broken line shows the characteristics of the high group filter. At a frequency of 770Hz it is assumed that 0dB are lost, therefore this point is used for reference.



DECODER

1. Digital Frequency-detecting Circuit

   The DF (Detect Frequency) pin goes to “High” when the detector circuit acknowledges the output signals from the two comparators as valid DTMF signal frequencies in the digital frequency detecting block.

2. Guard Time Setting Circuit

   Automatic or adjustable external guard time setting modes are provided. Guard time has two types: GTP (Guard Time Present) and GTA (Guard Time Absent).

   2.1 Automatic Guard Time Setting Circuit

   When GT pin is clamped to V_{DD}, automatic guard time setting circuit is selected; t_{GTP} and t_{GTA} are set to 20 milliseconds. The output signal from the filters may be acknowledged as a DTMF signal if:

   a) A signal with valid DTMF frequency lasts more than 40 milliseconds. This signal is decoded into a DTMF signal. These pulses correspond to the input signal enable period and disable period for alternative current characteristics.

   b) A period of more than 40 milliseconds exists between DTMF signals n and (n + 1). If this is not the case the DTMF signal (n + 1) is disabled.

      These pulses correspond to the inter-digit pauses for acceptance and rejection for alternative current characteristics.

   In a), it takes the DS (Detect Signal) pin GTP to acknowledge that the input signal is a DTMF signal after DF switches to “High”. The DS pin switches to “High” when the input signal is acknowledged as a DTMF signal.

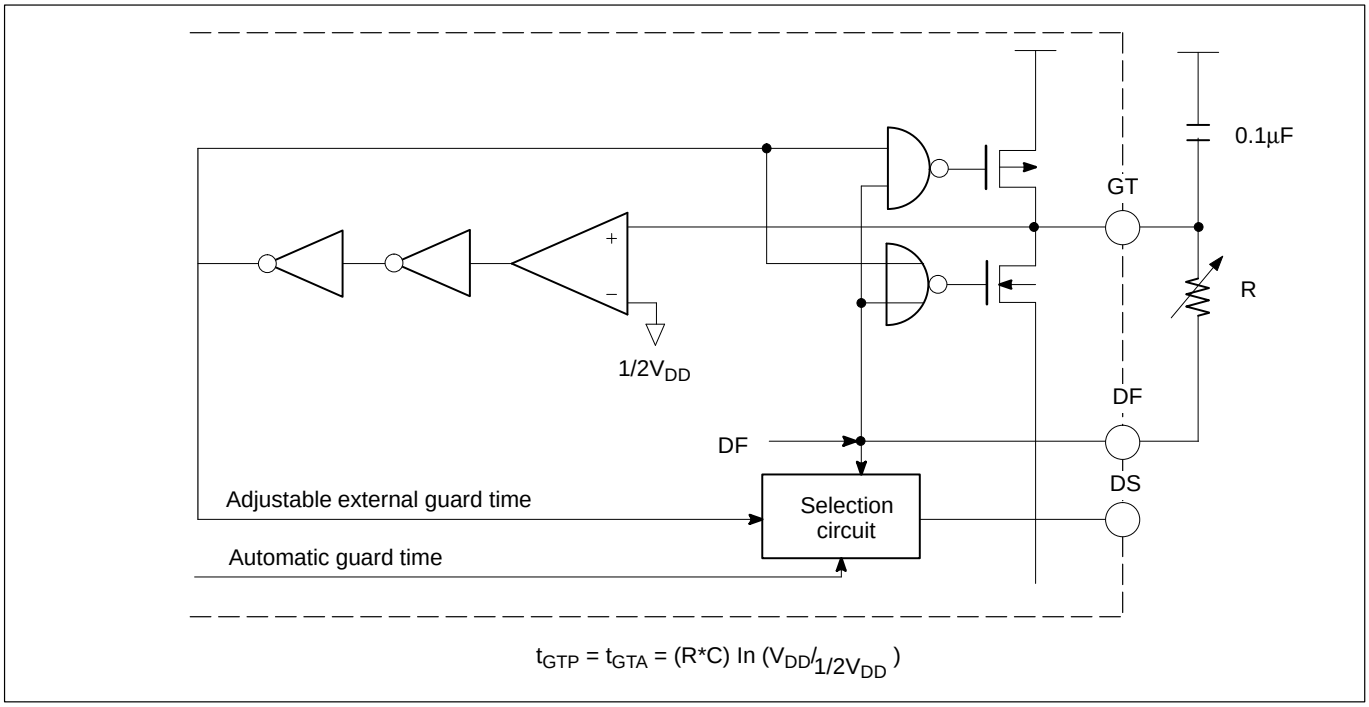
   In b), it takes the DS pin GTA to disable DTMF signal n after DF signal switches to “Low”. The DS pin switches to “Low” when the signal is disabled. (See the Timing Chart.)

   $t_{SDA} > t_{GTP} + t_{PDF}$
   $t_{IDA} > t_{ADF} + t_{GTA}$

2.2 Adjustable External Guard Time Setting Circuit

The simplified adjustable external guard time setting circuit shown below enables any guard time present (GTP) or guard time absent (GTA) setting.

The guard time is adjusted by selecting external register R when the external capacitor is 0.1µF.



2.3 Automatic Guard-time/Adjustable External Guard-time Setting Mode Selection Circuit

- Adjustable external guard time setting mode – The Adjustable external guard time setting mode (GT pin is set low) is selected on the rising edge of the detected frequency (DF).
- Automatic guard time setting mode – The automatic guard time setting mode (GT pin is set high) is selected with the power-on reset signal and on the rising edges of the DF.

2.4 Power-on Reset Circuit

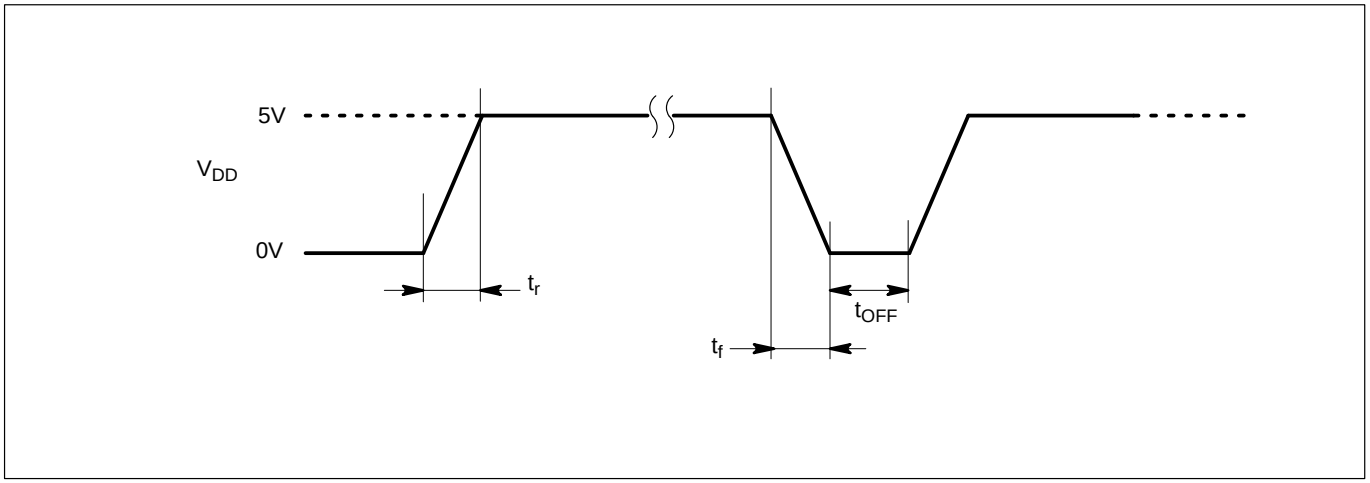
The power-on reset circuit generates a reset signal to initialize the automatic guard time or adjustable guard time setting circuit when power is applied.

The power-on reset circuit specifications ad timing diagram are shown in the following table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply rise time Power supply fall time	t_r t_f	0.1	–	50	ms	Power-on reset operation conditions
Power-off time	t_{off}	100	–	–	ms	

FUNCTIONAL DESCRIPTIONS

- Power-on reset timing diagram



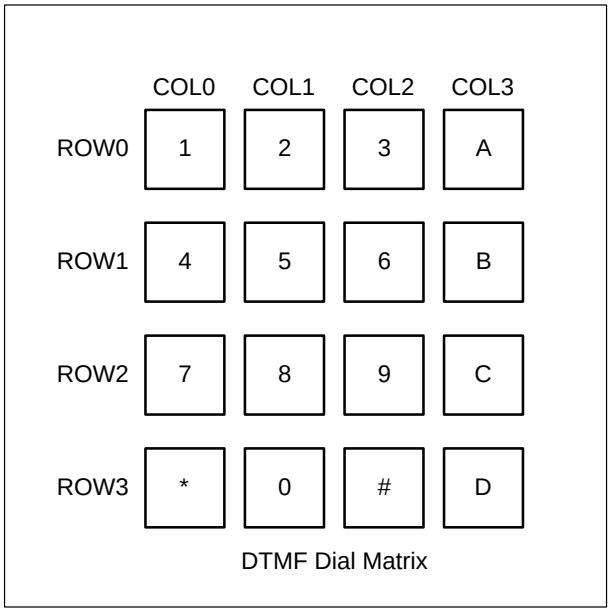
Note: If the values of power supply rise time, fall time, and power off time shown in the table are not satisfied, the power-on reset signal will not be generated and the automatic guard time setting circuit may not recover from malfunction (receive disabled).

The adjustable external guard time setting circuit will not enter malfunction even if the power-on reset signal is not generated.

Therefore, if power supply conditions disable the power-on reset circuit, the adjustable external guard setting circuit can be used.

OUTPUT CIRCUIT

When the signal detector pin (DS) switches to “High”, a received tone pair is stored in the output circuit register. The output latch status ay be output on the output bus by setting the three state control input (TOE) to “High”.

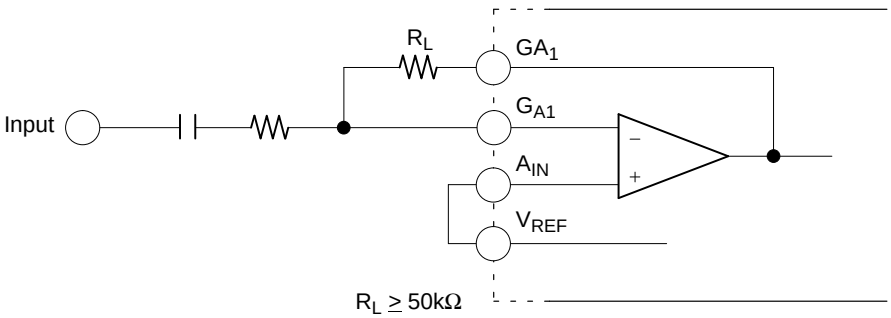


DTMF Dial Matrix

Dial	A_{IN} Input		Input	Output			
	Low group: fo	High group: fo	TOE	Q_4	Q_3	Q_2	Q_1
1	697	1209	1	0	0	0	1
2	697	1336	1	0	0	1	0
3	697	1447	1	0	0	1	1
4	770	1209	1	0	1	0	0
5	770	1336	1	0	1	0	1
6	770	1477	1	0	1	1	0
7	852	1209	1	0	1	1	1
8	852	1336	1	1	0	0	0
9	852	1477	1	1	0	0	1
0	941	1336	1	1	0	1	0
*	941	1209	1	1	0	1	1
#	941	1477	1	1	1	0	0
A	697	1633	1	1	1	0	1
B	770	1633	1	1	1	1	0
C	852	1633	1	1	1	1	1
D	941	1633	1	0	0	0	0

SAMPLE DIFFERENCE INPUT CONFIGURATION

The MB87017B uses a difference input amplifier and provides for a bias power source (V_{REF}) to apply a bias voltage to the input signal. this also allows a pin to connect a gain adjustment resistor tot he amplifier output.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V_I	0	–	V_{DD}	V
Oscillation Frequency	f_{OSC}	3.5759	3.5795	3.5831	MHz
OSC1 Pin Load Capacitance	C_{LDI}	10.0	–	50.0	pF
OSC2 Pin Load Capacitance	C_{LDO}	10.0	–	50.0	pF
GA2 Pin Load Resistance	R_{LA}	50	–	–	kΩ
GA2 Pin Load Capacitance	C_{LA}	–	–	100	pF
Operating Temperature	T_A	0	–	70	°C

DC CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Power Consumption	p_D	f = 3.58MHz, V_{DD} = 5V	–	25	37	mW
Low-level Input Voltage	V_{IL}		0	–	0.8	V
High-level Input Voltage	V_{IH}		2.0	–	V_{DD}	V
Low Level Input Leak Current	I_{iL}	V_I = GND	–10	–	10	µA
High Level Input Leak Current	I_{iH}	V_I = V_{DD}	–10	–	10	µA
Low-level Output Voltage	V_{OL}	I_{OL} = 2mA	0	–	0.4	V
High-level Output Voltage	V_{OH}	I_{OH} = –0.4mA	2.4	–	V_{DD}	V
V_{REF} Output Voltage	v_{REF}		–	2.5	–	V

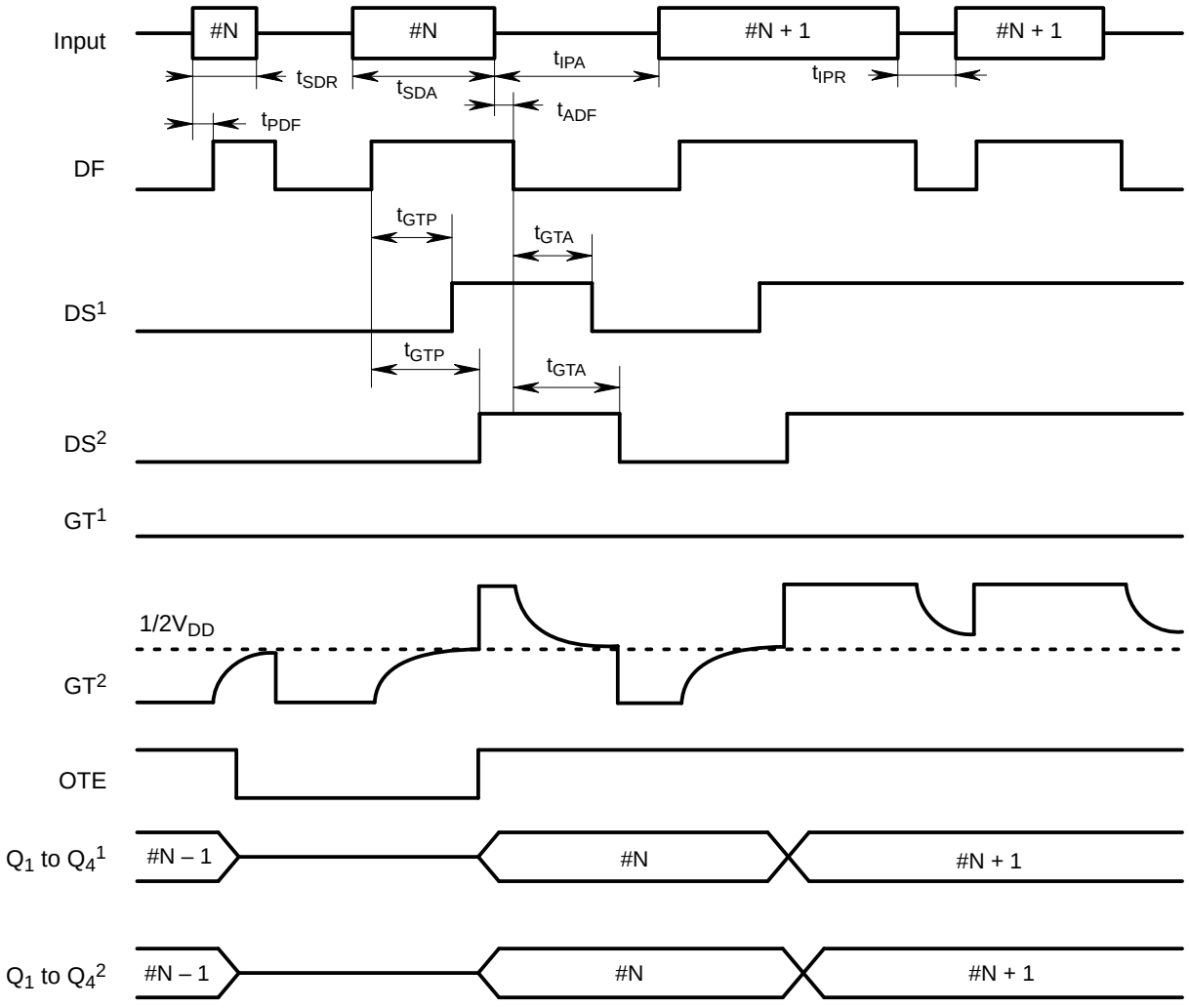
AC CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Signal Input Level [1]		T_A = 25°C, V_{DD} = 5V	–29	–10	–1	dBm
TWIST [2]			–	±10	–	dB
Allowable Frequency Deviation			±1.5±2 Hz	–	–	%
Prohibited Frequency Deviation			±3.5	–	–	%
Allowable Noise Level [3]			–	–12	–	dB
Allowable Dial Tone Level [4]			–	22	–	dB
Input Signal Detection Timing (Present) [5]	t_{PDF}		5	11	14	ms
Input Signal Detection Timing (Absent) [5]	t_{ADF}		0.5	4	8.5	ms
Input Signal Enable Period (Accept) [5, 6]	t_{SDA}		–	–	40	ms
Input Signal Enable Period (Reject) [5, 6]	t_{SDR}		20	–	–	ms
Inter-digit Pause (Accept) [5, 6]	t_{IPA}		–	–	40	ms
Inter-digit Pause (Reject) [5, 6]	t_{IPR}		9	–	–	ms
Input Clock Frequency	f_{IN}		3.5759	3.5795	3.5831	MHz
Clock Rise Time	tr		–	–	110	ns
Clock Fall Time	tf		–	–	110	ns
Clock Duty	DR		–	50	–	%

1. dBm: 600Ω reference.
2. TWIST = High group tone voltage/Low group tone voltage.
3. Allowable noise = Total allowable noise within the range 30Hz to 3.4kHz/Minimum amplitude tone level in valid tone pairs.
4. Allowable dial tone level = Tone allowable normal dial tone volume/Minimum amplitude tone in valid tone pairs.
5. See Timing Chart.
6. Specified values are referenced to the automatic guard time setting mode. See page 5 for t_{GTP}, and t_{GTA} in the adjustable external guard time setting mode.

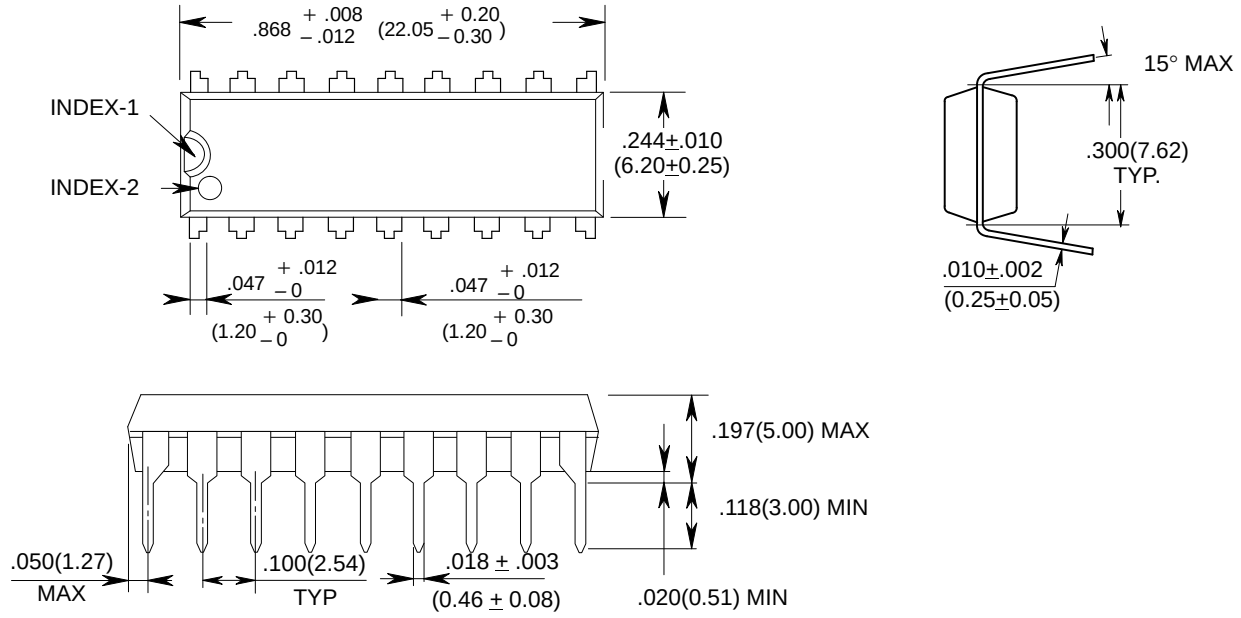
TIMING CHART



NOTE: 1. Automatic guard time setting mode (GT pin is clamped to V_{DD})
2. Adjustable external guard time setting mode (see circuit on page 5)

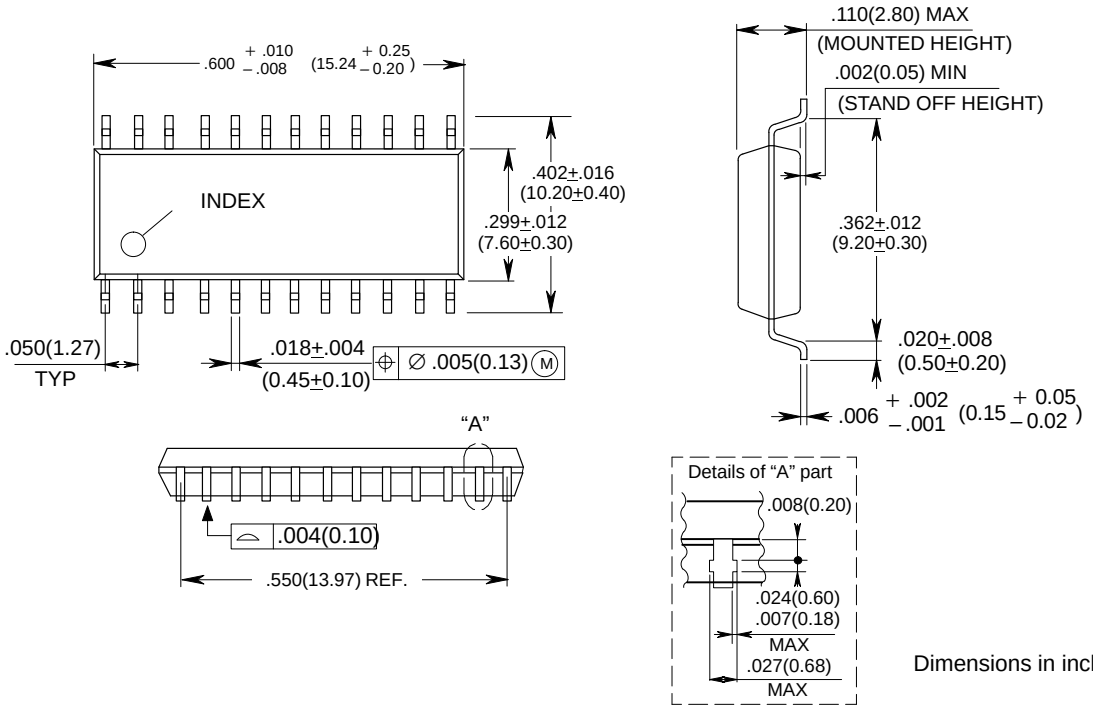
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-18P-M02)



Dimensions in inches (millimeters).

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: FPT-24P-M02)



Dimensions in inches (millimeters).

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