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Edition 0.1

Product Profile Sheet

MB15B11

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

On-chip 1.1GHz & 400MHz PRESCALER'S

The Fujitsu MB15B11 is a serial input Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. Two synthesizers; 400MHz system has a low sensitivity charge pump for transmit modulation, 1.1GHz system has a high sensitivity charge pump for fast lock up of receive frequency. An analog switch is provided for each PLL circuit for faster lock up.
These various features help compact system designing important in mobile radio applications. Typical applications are cellular phones, cordless phones and other radio applications where IF modulation is adopted.

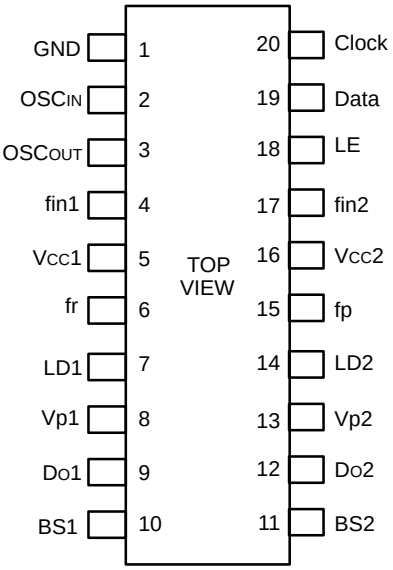
It operates with a supply voltage of 3.0V typ. and dissipates totally 9.5 mA typ. of current realized through the use of Fujitsu's Bi-CMOS technology. The power saving function maintains current reduction.

PRELIMINARY

FEATURES

- Dual PLL frequency synthesizers; 400MHz (PLL1) & 1.1 GHz (PLL2)
- Low power supply current: I_{CC} (total) = 9.5 mA typ. (Vcc = 3V)
- Power saving function : I_{CC1} = I_{CC2} = 100 µA typ (Vcc = 3V)
- Pulse swallow function;
  – 1.1GHz Prescaler: 64/65 or 128/129
  – 400MHz Prescaler: 32/33 or 64/65
- Serial input 14-bit programmable reference counter: R = 8 to 16383
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 16 to 2047
  PLL1 and PLL2 programmable counters can be controlled independently.
- Functionally tuned up charge pumps
  – Transmit (PLL1): Low sensitivity charge pump (for modulation)
  – Receive (PLL2): High sensitivity charge pump (for fast lock up)
- Low power supply voltage: V_{CC} = 2.7 to 3.5V
- On-chip analog switches achieve fast lock up time
- Wide operating temperature: T_A = –30 to 80°C
- Plastic 20-pin SSOP package

PIN ASSIGNMENT

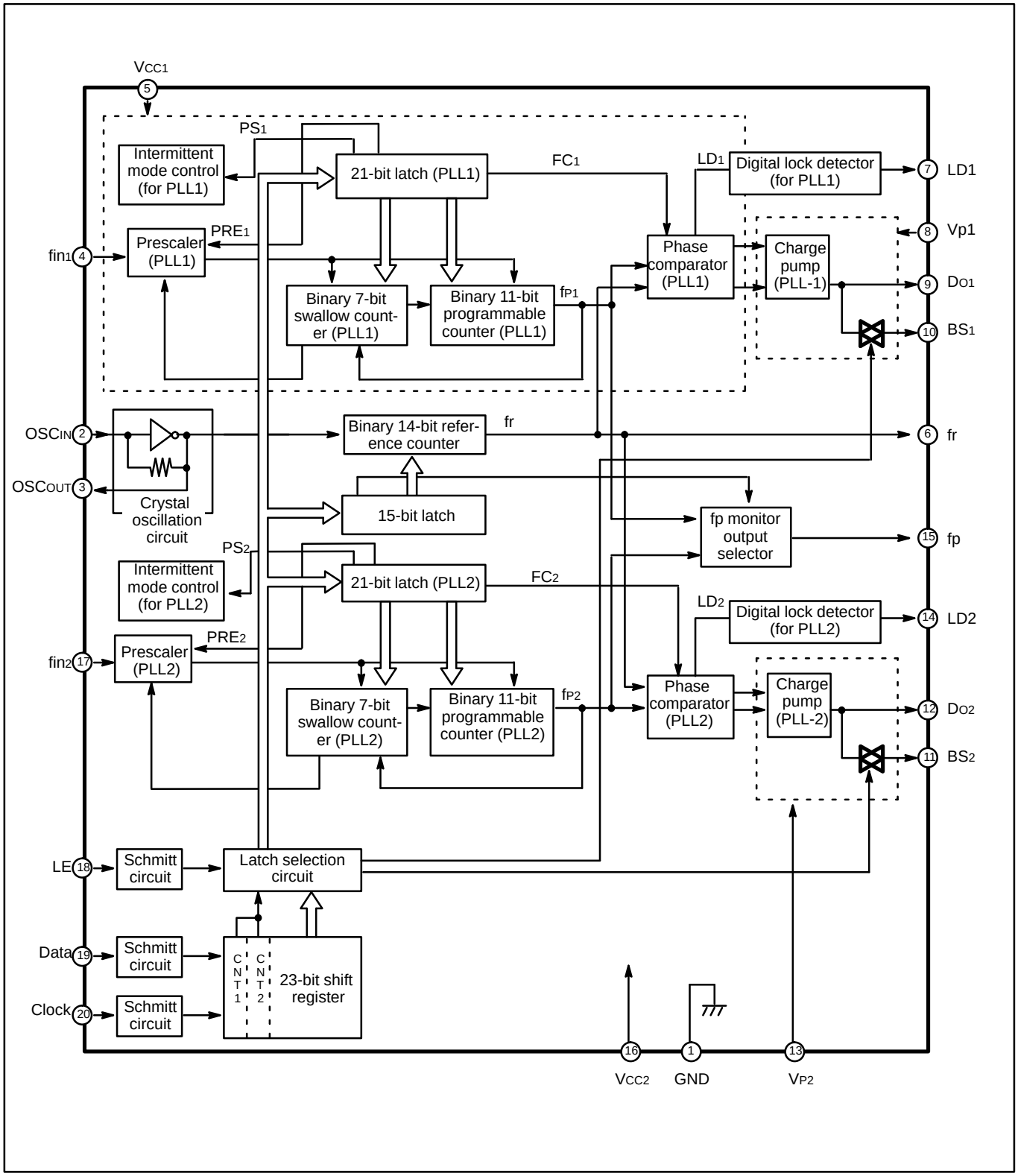


ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Remark	Value	Unit
Power Supply Voltage	V_{CC}		–0.5 to 5.0	V
	V_P		V_{CC} to 7.0	V
Output Voltage	V_{OUT}		–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}		±10	mA
Storage Temperature	T_{STG}		–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground.</td></tr>
<tr><td>2
3</td><td>OSCIN
OSCOUT</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSCIN pin and OSCOUT pin.</td></tr>
<tr><td>4</td><td>fin1</td><td>I</td><td>Prescaler input pin of PLL1 section.
The connection with VCO should be AC.</td></tr>
<tr><td>5</td><td>VCC1</td><td>–</td><td>Power supply voltage input pin of PLL1 section.
When power is OFF, latched data of PLL1 section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output. (Open drain output)</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of PLL1 section.
<table>
<tr><td>Condition</td><td>LD pin output level</td></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>8</td><td>Vp1</td><td>–</td><td>Power supply pin for PLL1’s charge pump and analog switch</td></tr>
<tr><td>9</td><td>DO1</td><td>O</td><td>Charge pump output pin of PLL1 section.
Phase characteristics of the phase detector can be reversed according to FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of PLL1 section.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of PLL2 section.</td></tr>
<tr><td>12</td><td>DO2</td><td>O</td><td>Charge pump output pin of PLL2 section.
Phase characteristics of the phase detector can be reversed according to FC-bit setting.</td></tr>
<tr><td>13</td><td>Vp2</td><td>–</td><td>Power supply pin for PLL2’s charge pump and analog switch</td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detection signal output pin of PLL2 section.
<table>
<tr><td>Condition</td><td>LD pin output level</td></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output. (Open drain output)
This pin outputs divided frequency of PLL1 section or PLL2 section according to FP bit setting.
<table>
<tr><td>FP bit</td><td>Output</td></tr>
<tr><td>H</td><td>PLL1 section (fp1)</td></tr>
<tr><td>L</td><td>PLL2 section (fp2)</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	Vcc2	–	Power supply voltage input pin for PLL2 section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of PLL2 section and reference counter is cancelled.
17	fin2	I	Prescaler input pin of PLL2 section. The connection with VCO should be AC.
18	LE	I	Load enable input pin. This pin is followed by a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch according to a control data.
19	Data	I	Serial data input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit. The stored data in the shift register is transferred to one of PLL1 section, PLL2 section and programmable counter depending upon control data settings. Control bit data: H → The destination of data: Latch of PLL1 section Control bit data: L → The destination of data: Latch of PLL2 section
20	Clock	I	Clock input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit. On rising edge of the clock, one bit of data is transferred into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)

P: Preset divide ratio of dual modulus prescaler (32 or 64 for PLL1, 64 or 128 for PLL2)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

f_{OSC}: Reference oscillation frequency

R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable divider of PLL1 section, programmable divider of PLL2 section and programmable reference divider are controlled individually.
Serial data of binary data is entered into Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Control bits		Destination of serial data
CNT1	CNT2	
L	L	Programmable reference counter
L	H	Programmable counter of PLL1
H	H	Programmable counter of PLL2

SHIFT REGISTER CONFIGURATION

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CN1	CN2	FP	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

R1 to R14 : Divide ratio setting bit for the reference programmable counter (8 to 16383)
FP : Test purpose bit (monitor output fp1/fp2 selection)
CN1, 2 : Control bit

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	PS	PRE	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio setting bit for the programmable counter (16 to 2047)
A1 to A7 : Divide ratio setting bit for the swallow counter (0 to 127)
FC : Phase control bit for the phase detector
PRE : Divide ratio setting bit for the prescaler (64/65, 128/129)
PS : Power saving control bit
CN1, 2 : Control bit

BINARY 14-BIT PROGRAMMABLE REFERENCE COUNTER DATA SETTING

Divide Ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 8 is prohibited.
• Divide ratio (R) range = 8 to 16383

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
V	V	V	V	V	V	V	V	V	V	V	V
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 16 is prohibited.
• Divide ratio (N) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
V	V	V	V	V	V	V	V
127	1	1	1	1	1	1	1

Note:• Divide ratio (A) range = 0 to 127

PRESCALER DATA SETTING

		PRE = "H"	PRE = "L"
Prescaler Divide ratio	**PLL1**	32/33	64/65
	PLL2	64/65	128/129

Note: • Divide ratio for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.

POWER SAVING FUNCTION CONTROL

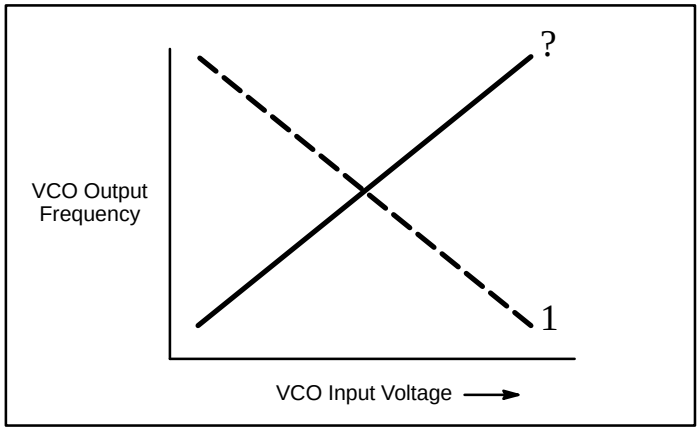
	PS	
	H	L
PLL1's section	ON	OFF
PLL2's section and common section	ON	OFF

Note:
- Power saving mode for each PLL1 and PLL2 is selected by the serial data at that time of divide ratio setting for each programmable divider.
- Common section ; Crystal oscillator circuit, programmable reference counter

PHASE COMPARATOR PHASE CONTROL DATA SETTING

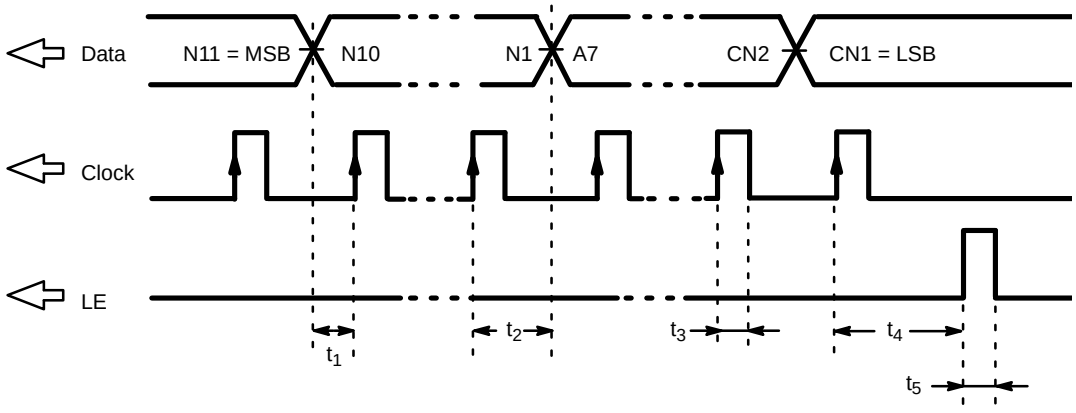
	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	?	1

Note:
- Z = High-impedance
- Depending upon the VCO polarity, FC bit should be set.
- Phase characteristic for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.



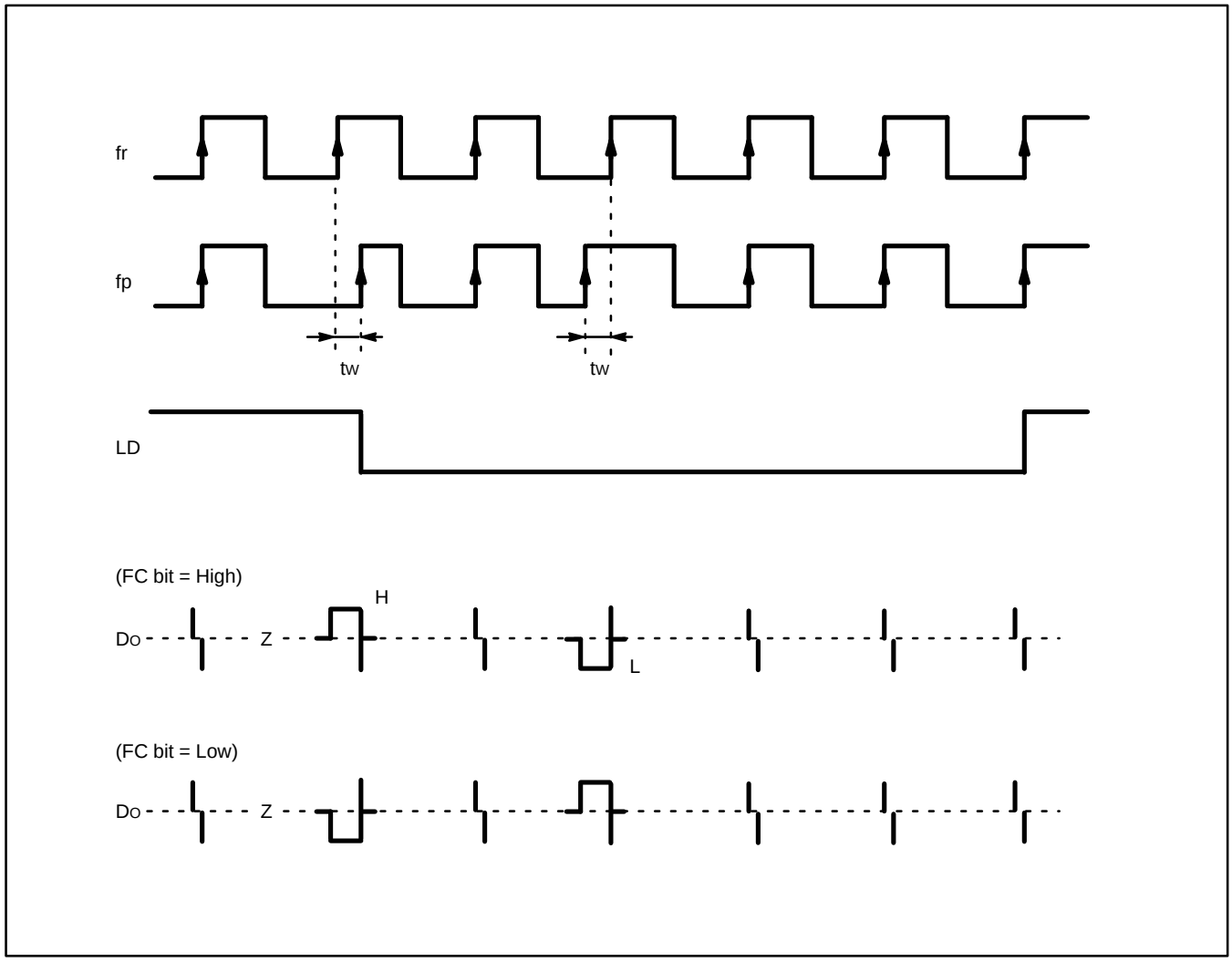
SERIAL DATA INPUT TIMING

t1 (>100ns) : Data set up time t2 (>1000ns) : Data hold time t3 (>300ns) : Clock pulse width
t4 (>100ns) : LE set up time to the rising edge of the last clock t5 (>800ns) : LE pulse width



On rising edge of the clock, one bit of the data is transferred into the shift register.

PHASE DETECTOR OUTPUT WAVEFORM



Note:
- Phase difference detection range = –2π to +2π
- LD output becomes low when phase difference is tw or more.
- LD output becomes high when phase difference is tw or less and continues to be so for three cysles or more.
- tw depends on OSCin input frequency.
  (e.g. tW635ns to 1250ns when foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	$V_{CC}1 = V_{CC}2$
	V_{CC}	Vcc	–	6.0	V	
Input Voltage	V_{IN}	GND	–	V_{CC}	V	
Operating Temperature	T_A	–30	–	+80	°C	

HANDLING PRECAUTIONS

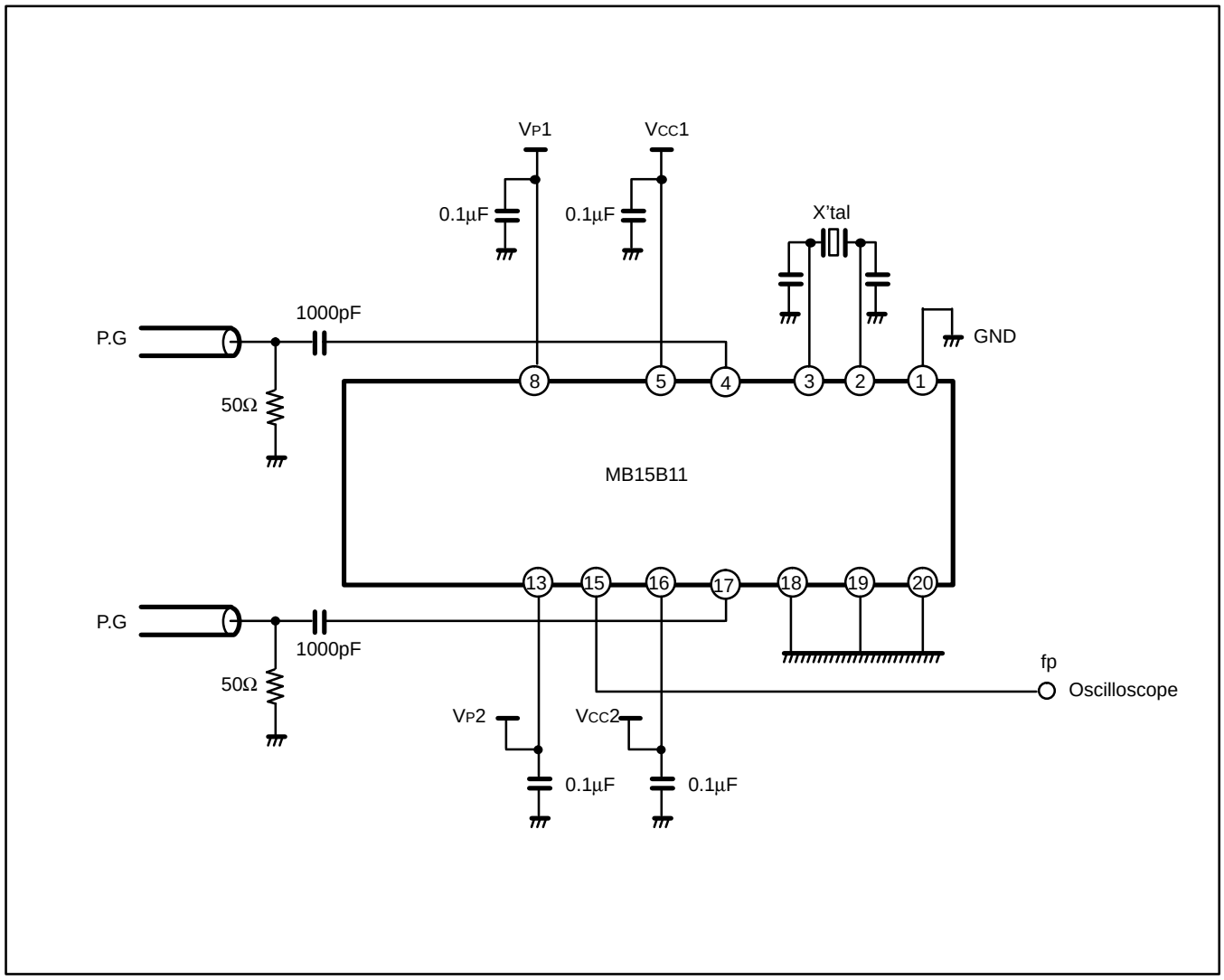
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

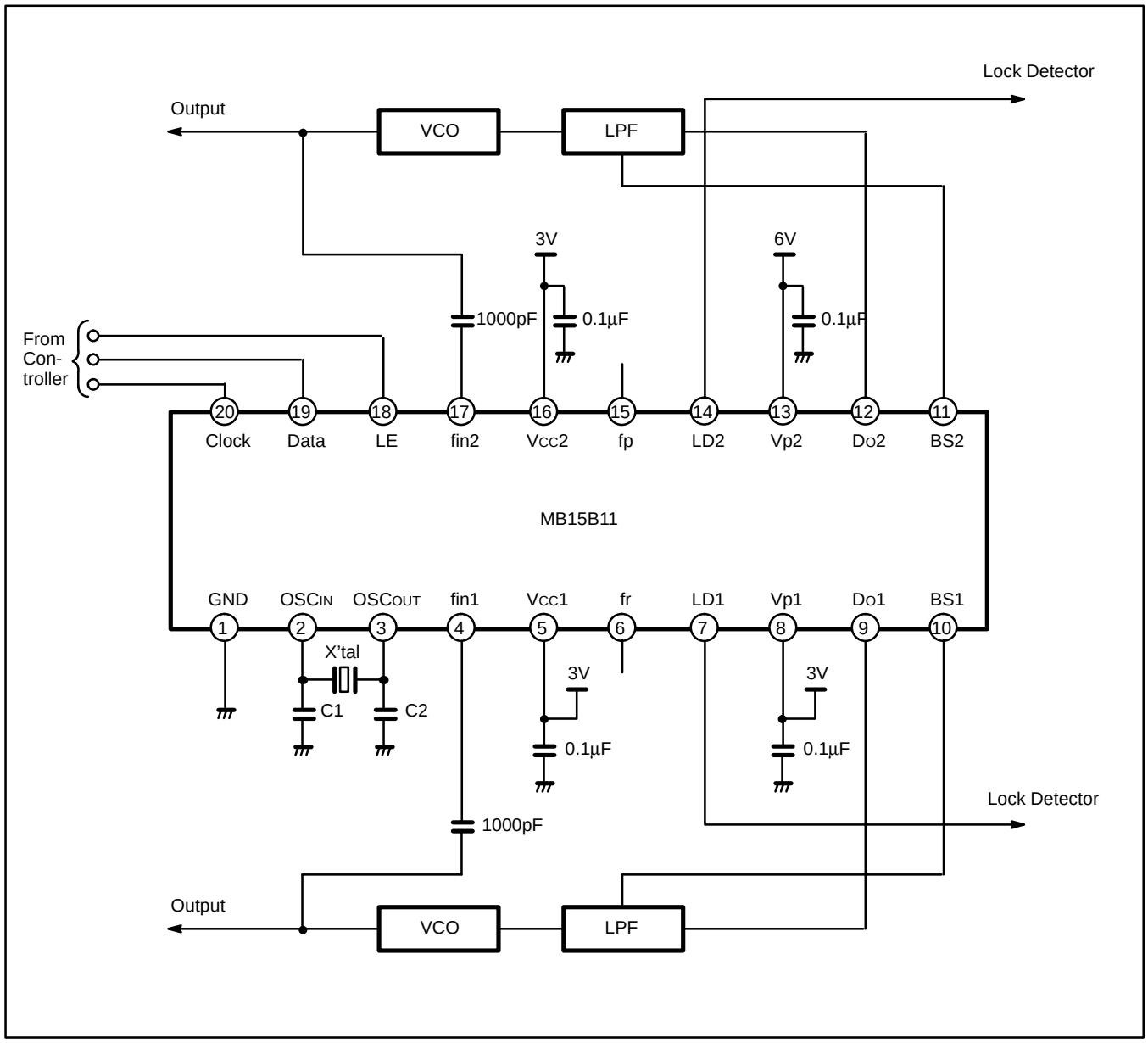
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		$I_{CC}1$	PLL1 section	–	3.5(0.1) *1	–	mA
		$I_{CC}2$	PLL2 section	–	6.0(0.1) *1	–	
Operating Frequency	fin1	fin1		100	–	400	MHz
	fin2	fin2		100	–	1100	
	OSC_{IN}	f_{OSC}		–	12.8	20.0	
Input Sensitivity	fin1	Pfin1	PLL1, 50Ω system	–10	–	4	dBm
	fin2	Pfin2	PLL2, 50Ω system	–10	–	4	dBm
	OSC_{IN}	V_{OSC}		0.5	–	–	Vp-p
High–level Input Voltage	Except fin and OSCin	V_{IH}		V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3–0.4	
High–level Input Current	Data, Clock LE	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	
High–level Output Voltage	Except Do and OSCout	V_{OH}	V_{CC} = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}		–	–	0.4	
High–impedance Cutoff Current	Do, ΦP	I_{OFF}	Vp = Vcc to 8.0V, Voop = GND to 8.0V	–	–	1.1	µA
Output Current	Except Do and OSCout	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	
	Do1	I_{OH}	V_P = 6.0V	–	–1	–	mA
		I_{OL}	V_{CC} = 3.0V	–	12	–	
	Do2	I_{OH}	V_P = 6.0V	–	–3	–	mA
		I_{OL}	V_{CC} = 3.0V	–	6	–	
Analog Switch ON Resistance		R_{ON}		–	50	–	Ω

Notes: *1 : The value in ( ) is power supply current in power saving mode.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



APPLICATION EXAMPLE



Note: X'tal ; 12.8MHz
C1, C2 : depends on a crystal oscillator.
Clock, Data, LE : involves a schmitt circuit.
(When inputs are open, pull up/down resistor is necessary to prevent self-oscillation.)
Vp1, Vp2 : 6V max.

PACKAGE INFORMATION