February 1994
Edition 1.0

FUJITSU

DATA SHEET

MB85342A-60/-70/-80

CMOS 2M x 32 Fast Page Mode DRAM Module

CMOS 2,097,152 x 32 Bit Fast Page Mode DRAM Module

The Fujitsu MB85342A is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of sixteen MB814400A devices. The MB85342A is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85342A are the same as the MB814400A which features fast page mode operation. For ease of memory expansion, the MB85342A is offered in a 72–pad Single In–line Memory Module package (SIMM).

See page 6

MSS–72P–P10

PRODUCT LINE & FEATURES

Parameter	MB85342A-60	MB85342A-70	MB85342A-80
$\overline{RAS}$ Access Time	60ns max.	70ns max.	80ns max.
Random Cycle Time	110ns min.	125ns min.	140ns min.
Address Access Time	30ns max.	35ns max.	40ns max.
$\overline{CAS}$ Access Time	15ns max.	20ns max.	20ns max.
Fast Page Mode Cycle Time	40ns min.	45ns min.	45ns min.
Power Dissipation • Operating mode	4928mW max.	4488mW max.	4048mW max.
• Standby mode	176mW max. (TTL level) / 88mW max. (CMOS level)		

- Organization :
  2,097,152 words x 32 bits
- Memory :
  MB814400A, 16 pcs
- Decoupling Capacitor :
  0.22 µF, 16 pcs
- Package and Ordering Information:
  72–pad SIMM, order as MB85342A–xxPJPBK
  (PJPBK = Gold Pad)

ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–1.0 to +7.0	V
Input Voltage	V_{IN}	–1.0 to +7.0	V
Output Voltage	V_{OUT}	–1.0 to +7.0	V
Short Circuit Output Current	I_{OUT}	50	mA
Power Dissipation	P_D	16	W
Storage Temperature	T_{STG}	–55 to +125	°C

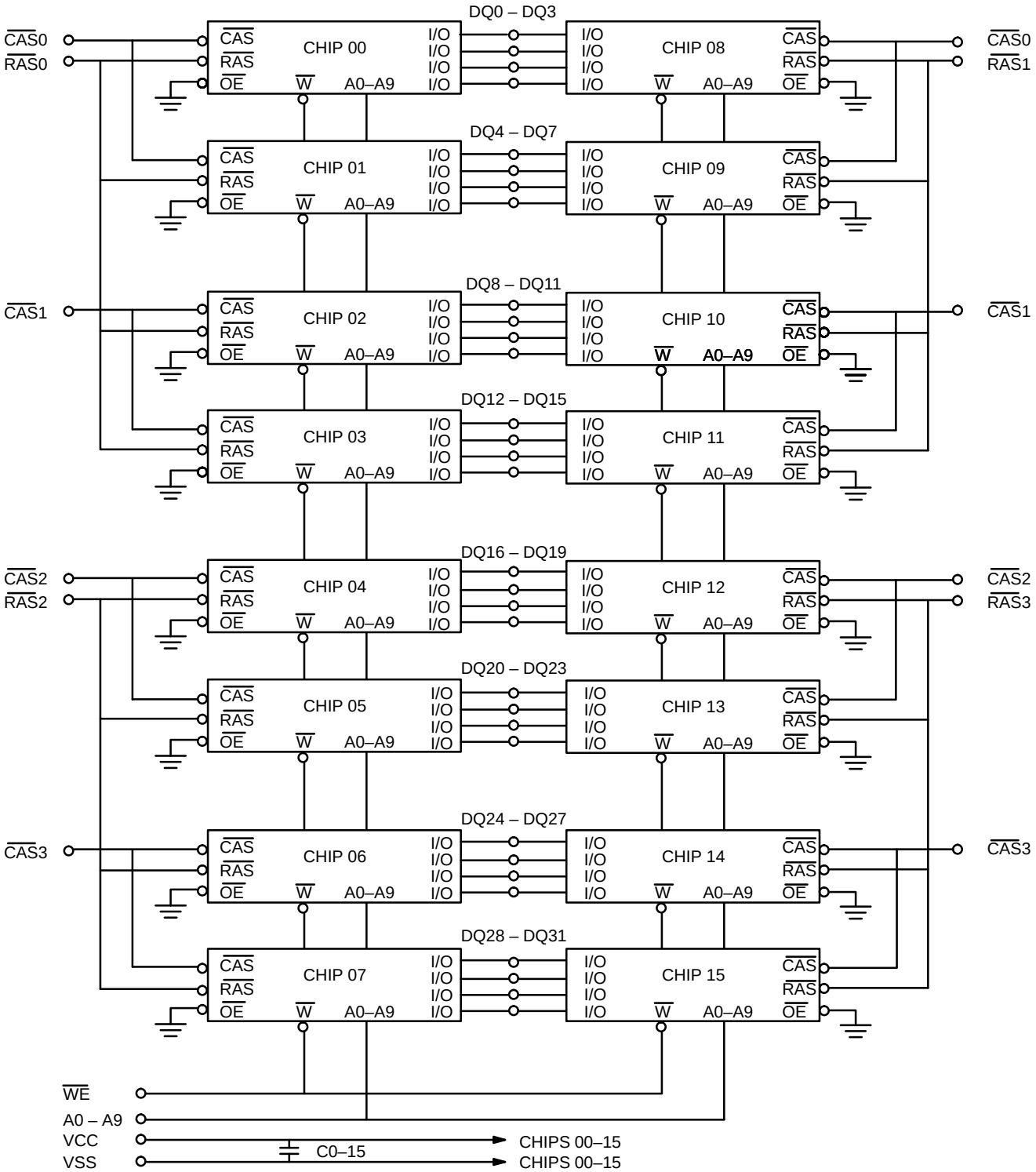
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DQ0	2	1	VSS
DQ1	4	3	DQ16
DQ2	6	5	DQ17
DQ3	8	7	DQ18
VCC	10	9	DQ19
A0	12	11	NC
A2	14	13	A1
A4	16	15	A3
A6	18	17	A5
DQ4	20	19	NC
DQ5	22	21	DQ20
DQ6	24	23	DQ21
DQ7	26	25	DQ22
A7	28	27	DQ23
VCC	30	29	NC
A9	32	31	A8
$\overline{RAS}$2	34	33	$\overline{RAS}$3
NC	36	35	NC
NC	38	37	NC
$\overline{CAS}$0	40	39	VSS
$\overline{CAS}$3	42	41	$\overline{CAS}$2
$\overline{RAS}$0	44	43	$\overline{CAS}$1
NC	46	45	$\overline{RAS}$1
NC	48	47	$\overline{WE}$
DQ24	50	49	DQ8
DQ25	52	51	DQ9
DQ26	54	53	DQ10
DQ27	56	55	DQ11
DQ28	58	57	DQ12
DQ29	60	59	VCC
DQ30	62	61	DQ13
DQ31	64	63	DQ14
NC	66	65	DQ15
PD2	68	67	PD1
PD4	70	69	PD3
VSS	72	71	NC

Pin #	Symbol	-60	-70	-80
67	PD1	NC	NC	NC
68	PD2	NC	NC	NC
69	PD3	NC	V_{SS}	NC
70	PD4	NC	NC	V_{SS}

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Value			Unit	Ambient Operating Temp.
			Min	Typ	Max		
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to 70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V_{IL}	–2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	–1.0	—	0.8	V	

*** :** Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Notes	Symbol	Conditions	Value			Unit
					Min	Typ	Max	
Output High Voltage		1	V_{OH}	I_{OH} = –5mA	2.4	—	—	V
Output Low Voltage		1	V_{OL}	I_{OL} = 4.2mA	—	—	0.4	V
Input Leakage Current	$\overline{RAS}$		$I_{I(L)}$	0V ≤ V_{IN} ≤ 5.5V; 4.5V ≤ V_{CC} ≤ 5.5V; V_{SS}=0V; all other pins not under test = 0V	–30	—	30	µA
	$\overline{CAS}$				–30	—	30	
	ADD, $\overline{WE}$				–90	—	90	
Output Leakage Current			$I_{O(L)}$	0V ≤ V_{OUT} ≤ 5.5V; Data out disabled	–10	—	10	µA
Operating Current (Average power supply current)	MB85342A-60	2	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min.	—	—	896	mA
	MB85342A-70						816	
	MB85342A-80						736	
Standby Current (Power supply current)	TTL Level		I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	32	mA
	CMOS Level			$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC}-0.2V			16	
Refresh Current #1 (Average power supply current)	MB85342A-60	2	I_{CC3}	$\overline{CAS}$ = V_{IH}; $\overline{RAS}$ = cycling; t_{RC} = min.	—	—	896	mA
	MB85342A-70						816	
	MB85342A-80						736	
Fast Page Mode Current	MB85342A-60	2	I_{CC4}	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = cycling; t_{PC} = min.	—	—	456	mA
	MB85342A-70						416	
	MB85342A-80						376	
Refresh Current #2 (Average power supply current)	MB85342A-60	2	I_{CC5}	$\overline{RAS}$ = cycling; $\overline{CAS}$–before–$\overline{RAS}$ t_{RC} = min.	—	—	736	mA
	MB85342A-70						656	
	MB85342A-80						576	

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9	C_{IN1}	—	94	pF
Input Capacitance, $\overline{RAS}$0 to $\overline{RAS}$3	C_{IN2}	—	37	pF
Input Capacitance, $\overline{CAS}$0 to $\overline{CAS}$3	C_{IN3}	—	29	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	81	pF
I/O Capacitance, (DQ0-31)	C_{DQ}	—	15	pF

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB85342A-60		MB85342A-70		MB85342A-80		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	140	—	ns
3	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	60	—	70	—	80	ns
4	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	15	—	20	—	20	ns
5	Column Address Access Time	8,9	t_{AA}	—	30	—	35	—	40	ns
6	Output Hold Time		t_{OH}	0	—	0	—	0	—	ns
7	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	0	—	ns
8	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	—	20	ns
9	Transition Time		t_T	2	50	2	50	2	50	ns
10	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	45	—	50	—	ns
11	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	80	100000	ns
12	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	20	—	20	—	ns
13	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	5	—	5	—	5	—	ns
14	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	20	50	20	60	ns
15	$\overline{CAS}$ Pulse Width		t_{CAS}	15	—	20	—	20	—	ns
16	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	80	—	ns
17	$\overline{CAS}$ Precharge Time (Normal)	17	t_{CPN}	10	—	10	—	10	—	ns
18	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
19	Row Address Hold Time		t_{RAH}	10	—	10	—	10	—	ns
20	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
21	Column Address Hold Time		t_{CAH}	12	—	12	—	15	—	ns
22	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	15	40	ns
23	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	40	—	ns
24	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	30	—	35	—	40	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	10	—	10	—	12	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	12	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	20	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	15	—	18	—	20	—	ns
33	DIN Setup Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	10	—	12	—	ns
35	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB85342A-60		MB85342A-70		MB85342A-80		Unit
				Min	Max	Min	Max	Min	Max	
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before–$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before–$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	12	—	ns
38	$\overline{WE}$ Set Up Time from $\overline{RAS}$	18	t_{WSR}	0	—	0	—	0	—	ns
39	$\overline{WE}$ Hold Time from $\overline{RAS}$	18	t_{WHR}	10	—	10	—	10	—	ns
40	DIN to $\overline{CAS}$ Delay Time		t_{DZC}	0	—	0	—	0	—	ns
41	Fast Page Mode $\overline{RAS}$ Pulse width		t_{RASP}	—	200000	—	200000	—	200000	ns
42	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	45	—	ns
43	Access Time from $\overline{CAS}$ Precharge	9,16	t_{CPA}	—	35	—	40	—	40	ns
44	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	ns
45	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35	—	40	—	40	—	ns

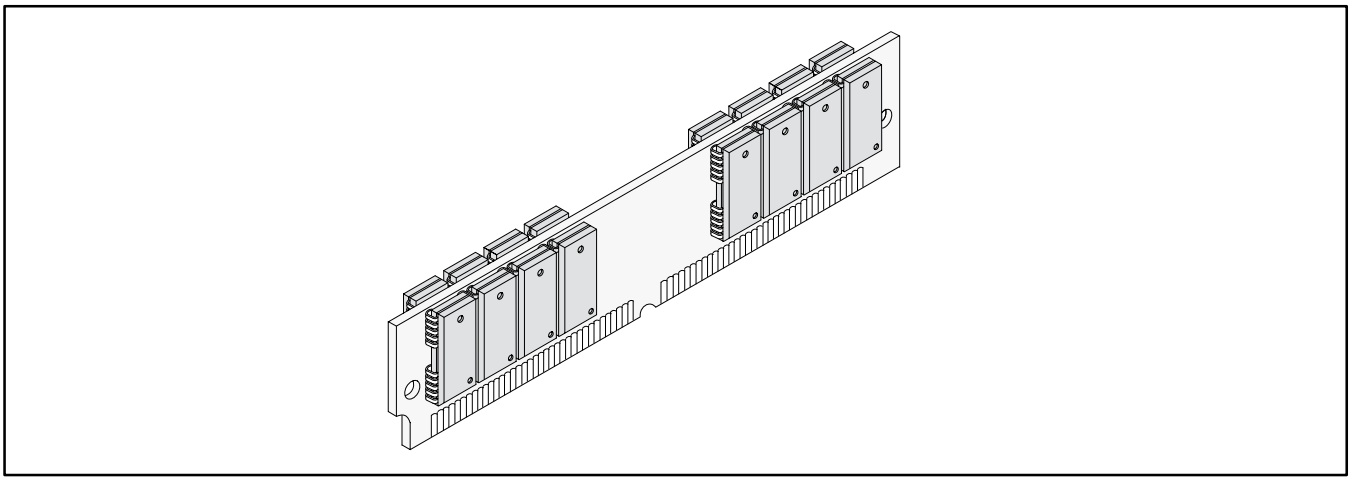
Notes:

1. Referenced to VSS.
2. ICC depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   ICC depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH, VIL > –0.5V.
   ICC1, ICC3 and ICC5 are specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   ICC4 is specified at one time of address change during one Page cycle.
3. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} is long, t_{CPA} is longer than tCPA (max).
17. Assumes that $\overline{CAS}$ –before–$\overline{RAS}$ refresh.
18. Assumes that Test mode function.

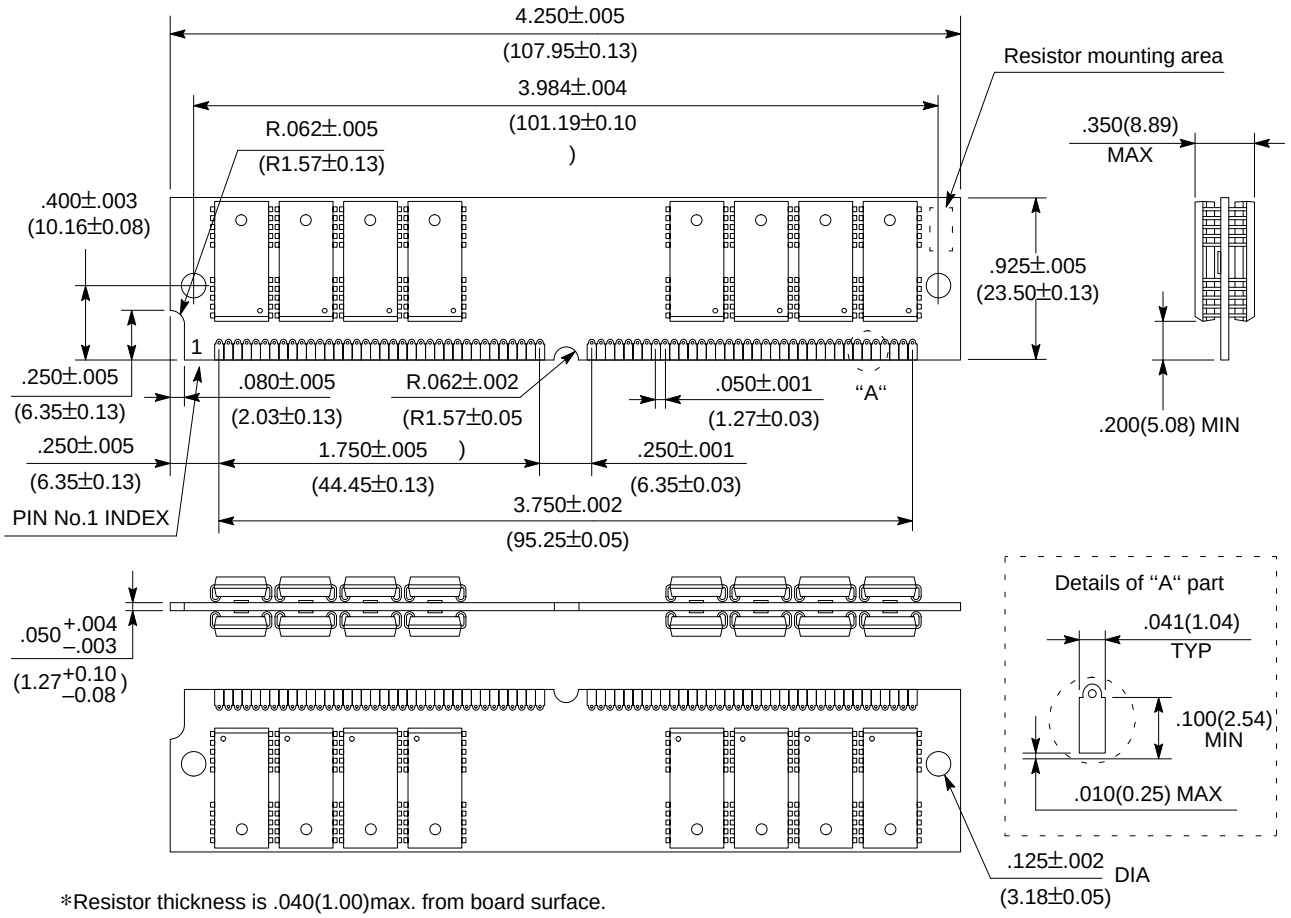
* Source: See MB814400A Data Sheet for details on the electricals.

PACKAGE DIMENSIONS

(Suffix: PJPBK)



72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P10)



*Resistor thickness is .040(1.00)max. from board surface.

Dimensions in
inches (millimeters)