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FUJITSU

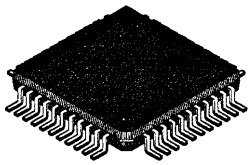
DATA SHEET

MB86465A

1200 BPS MSK MODEM WITH BASEBAND FILTER AND SPEECH SCRAMBLER

BUILT-IN SPEECH SCRAMBLER FOR CORDLESS PHONE

The Fujitsu MB86465A 1200 bps MSK modem contains a baseband filter for cordless telephones with built-in speech scramblers. The baseband filter constitutes an SCF splatter filter with built–in transmitter amplifier, receiver amplifier, frequency–inverting acoustic scrambler, a limiter, and a mute circuit. The MSK modem communicates at a speed of 1200 bps and has built–in frame monitoring function. This LSI operates on voltages as low as 2.7 volts.

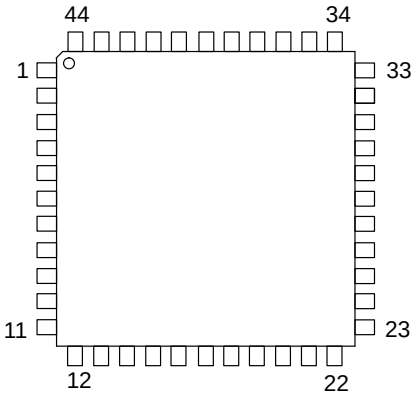


(FPT-44P-M01)

FEATURES

- Transmitter/Receiver filters:
  - Built–in amplifiers with input gain control
  - Built–in frequency inversion type speech scrambler
  - Permits external control of the transmissions speech limiter level
  - Permits transmission and reception mute
- Modem:
  - 1,200 bps MSK modem
  - Selectable frame synchronization patterns (for both parent and child sets)
  - Built–in parent/child set frame signal detecting function
  - Permits full–duplex operation
- Crystal oscillator circuit: Selectable between 3.6864MHz and 3.456MHz
- Built–in standby function
- Logical input/output level: CMOS input/output level serial interface circuit
- Low power supply voltage: 2.7V to 5.5V
- Ambient temperature range: –30°C to +70°C

PIN ASSIGNMENT
(TOP VIEW)



MAXIMUM RATINGS (See NOTE) (A. GND = D. GND = 0V[2], T_A = =25°C)

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ.	Max.	
Power Voltage	V_{DD}	V_{DDD}, V_{DDA}[1]	GND -0.3	–	7	V
Input Voltage	V_I	All input pins	GND -0.3	–	V_{DD} +0.3	V
Output Voltage	V_O	All output pins	GND -0.3	–	V_{DD} +0.3	V
Output Current	I_O	All output pins	–10	–	10	mA
Storage temperature	Tstg	–	–40	–	135	°C

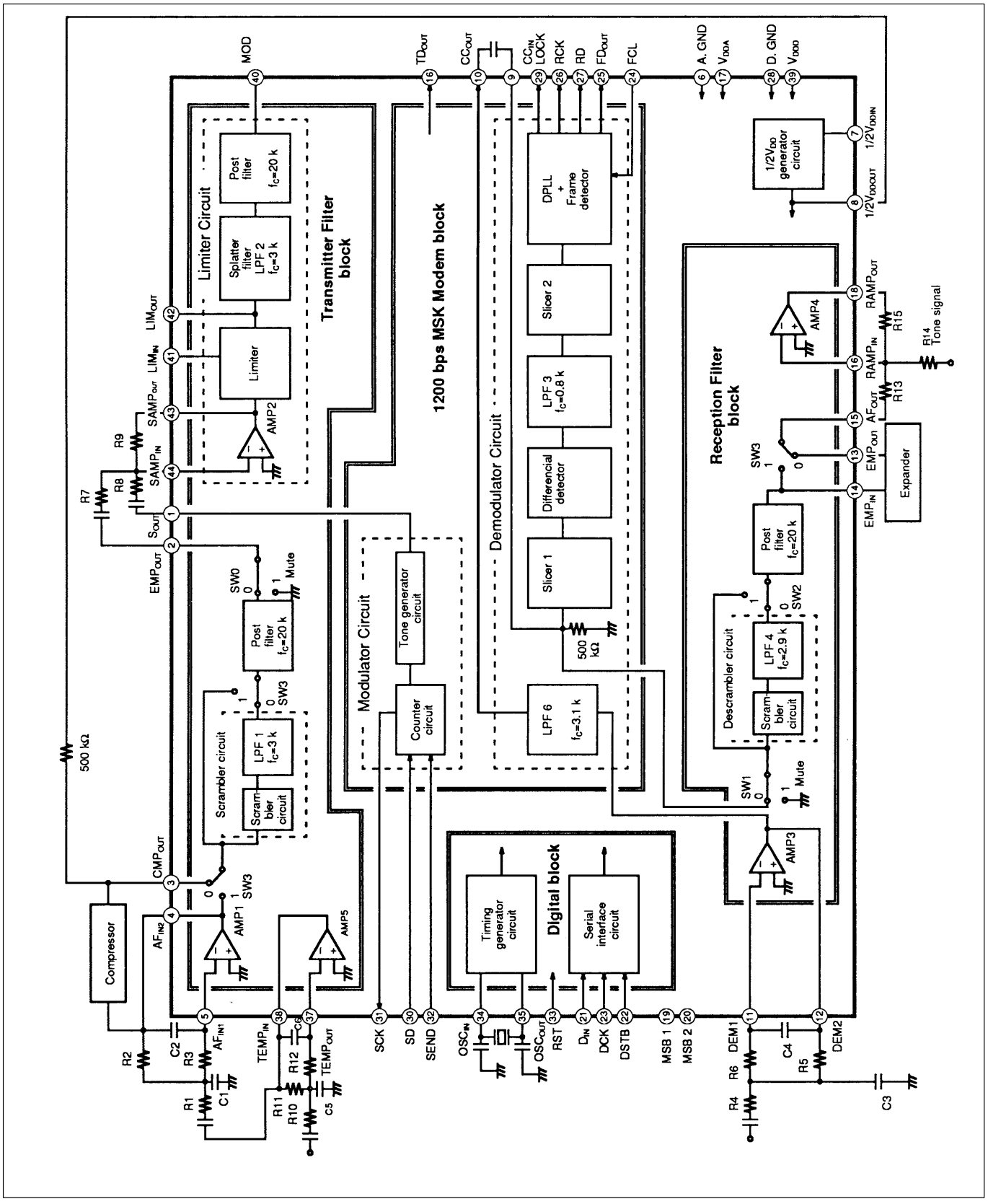
1. $V_{DD} = V_{DDD} = V_{DDA}$
2. GND = A. GND = D. GND

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This device should not be used in restricted applications, such as in wiretapping or evesdropping.

BLOCK DIAGRAM (Thick line shows boundary of external and internal circuits.)



PIN ASSIGNMENTS

Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol
1	O	S_{OUT}	12	O	DEM_2	23	I	DCK	34	I	OSC_{IN}
2	O	EMP_{OUT}	13	I	EXP_{OUT}	24	I	FCL	35	O	OSC_{OUT}
3	I	CMP_{OUT}	14	O	EXP_{IN}	25	O	FD_{OUT}	36	O	TD_{OUT}
4	O	AF_{IN2}	15	O	AF_{OUT}	26	O	RCK	37	O	$TAMP_{OUT}$
5	I	AF_{IN1}	16	I	$RAMP_{IN}$	27	O	RD	38	I	$TAMP_{IN}$
6	–	A. GND	17	–	V_{DDA}	28	–	D. GND	39	–	V_{DDD}
7	I	$^1/_2V_{DDIN}$	18	O	$RAMP_{OUT}$	29	O	LOCK	40	O	MOD
8	O	$^1/_2V_{DDOUT}$	19	–	MSB1	30	I	SD	41	I	LIM_{IN}
9	I	CC_{IN}	20	–	MSB2	31	O	SCK	42	O	LIM_{OUT}
10	O	CC_{OUT}	21	I	D_{IN}	32	I	SEND	43	O	$SAMP_{OUT}$
11	I	DEM_1	22	I	DSTB	33	I	RST	44	I	$SAMP_{IN}$

PIN DESCRIPTION

Pin Type	Pin No.	Symbol	I/O	Name	Description
Power Supply Pins	17	V_{DDA}	–	Analog power supply pin	For power supply, input the same level of voltage within a range of 2.7V to 5.5V
	39	V_{DDD}	–	Digital power supply pin	
	6	A. GND	–	Analog ground pin	–
	28	D. GND	–	Digital ground pin	–
Input pins	3	CMP_{OUT}	I	Input pin from external compressor	–
	5	AF_{IN1}	I	Amplifier inverted input pin (1) for transmitter input filter	A transmitter input filter is formed by connecting external resistors R1, R2 and R3 together with external capacitors C1 and C2 to pins AF_{IN1} and AF_{IN2}
	7	$^1/_2V_{DDIN}$	I	$^1/_2V_{DD}$ generator circuit input pin	A 1 µF bypass capacitor is placed between pins $^1/_2V_{DDIN}$ and A. GND
	11	DEM_1	I	Inverted input to receiver input filter amplifier	A receiver input filter is formed by connecting external resistors R4, R5, and R6 and external capacitors C3 and C4 to pins DEM_1 and DEM_2
	13	EXP_{OUT}	I	Input pin from external expander	–
	16	$RAMP_{IN}$	I	Inverted input pin for receiver adder amplifier	–
	19	MSB1	–	Non connection pin	Leave this pin open
	22	DSTB	I	Serial signal input strobe pin	Input serial signals are read into the mode selector register at the rising edge of DSTB
	23	DCK	I	Serial signal input clock pin	The serial signal is taken from pin D_{IN} simultaneous with the rising edge of DCK
	21	D_{IN}	I	Serial signal input pin	Inputs a serial signal for the interface
	24	FCL*	I	Frame detecting latch clear pin	A low on this pin sets the FD_{OUT} output to the L level. Set this pin on low before engaging the frame detecting function. The pin need not be set on low to reset the frame scanning function.
	30	SD	I	MSK modem transmission data input pin	–
	32	SEND	I	MSK modem transmission mute pin	Setting this pin on the “H” level generates an MSK signal
	33	RST*	I	Reset signal input pin	All circuits are reset when this pin is on the L level

PIN DESCRIPTION (Continued)

Pin Type	Pin No.	Symbol	I/O	Name	Description
Input pins	34	OSC_{IN}	I	Crystal oscillator circuit input pin	A 3.6864MHz or 3.456MHz quartz oscillator is connected between OSC_{IN} and OSC_{OUT}
	41	LIM_{IN}	I	Limiter level input pin	When open, the limiter level is set at $0.05 \bullet V_{DD}$(V)
	44	$SAMP_{IN}$	I	Amplifier inverted input pin to transmitter adder	–
	38	$TEMP_{IN}$	I	Inverted input pin (2) to transmitter input filter amplifier	A transmitter input filter is formed by connecting external resistors to pins $TAMP_{IN}$ and $TAMP_{OUT}$.
	9	CC_{IN}	I	Pin for demodulator external capacitor	A 1µF DC–blocking condenser is placed between pins CC_{IN} and CC_{OUT}
Output pins	10	CC_{OUT}	O		
	2	EMP_{OUT}	O	Transmitter scrambler output pin	–
	37	$TAMP_{OUT}$	O	Amplifier output pin (1) for transmitter input filter	A transmitter input filter is formed by connecting a resistor and a capacitor to pins $TAMP_{iN}$ and $TAMP_{OUT}$
	4	AM_{IN2}	O	Amplifier output pin (2) for transmitter input filter	A transmitter input filter is formed by connecting a resistor and a capacitor to pins AF_{iN2} and AF_{IN1}
	8	$^1/_2V_{DDOUT}$	O	$^1/_2V_{DD}$ generator circuit output pin	Internal circuits operate with the $^1/_2V_{DDOUT}$ voltage as a reference voltage
	12	DEM_2	O	Amplifier output pin for receiver input filter	A receiver input filter is formed by connecting a resistor and a capacitor to pins DEM_1 and DEM_2
	14	EXP_{IN}	O	Output pin to external expander	–
	15	AF_{OUT}	O	Output pin to external expander or de–emphasis circuit	–
	18	$RAMP_{OUT}$	O	Receiver adder amplifier output pin	Becomes the receiver output pin
	20	MSB2	–	Non connection pin	This pin is left open
	25	FD_{OUT}	O	Frame detecting circuit output signal pin	After reset clears, the FD_{OUT} pin changes from “L” level to “H” level high when a code matching the frame synch pattern is output from the RD pin
	26	RCK	O	MSK modem reception clock output pin	The rising edge of RCK causes SD data intake
	27	RD	O	MSK modem reception data output pin	–
	31	SCK	O	MSK modem transmission clock output pin	The rising edge of SCK causes SD data intake
	35	OSC_{OUT}	O	Output pin for crystal oscillator	–
	36	TD_{OUT}	O	Digital output test pin	–
	40	MOD	O	Transmitter output pin	–
	42	LIM_{OUT}	O	Limiter circuit output pin	–
	43	$SAMP_{OUT}$	O	Transmitter adder amplifier output pin	–
	1	S_{OUT}	O	MSK modem MSK modulation signal output pin	–
	29	LOCK	O	Lock signal output pin	The LOCK pin changes from “H” level to “L” level as the DPLL signal reaches $^1/_4$ cycle of RCK

*: This pin is pulled up with a high resistance coupling.

BLOCK FUNCTIONS

1. Transmitter Filter Block

(1) Compressor Coupler – This filter consists of input amplifiers AMP1 and AMP2 and an external RC for band control of transmission speech signals. The gain is controlled by external resistors R1 and R2. After band control, the speech signal is output to the external compressor from pin AF_{IN2}.

(2) Scrambler circuit – The output signal from the compressor is input into the scrambler circuit through pin CMP_{OUT}. It passes through LPF1 and output as a scrambled speech signal. The serial signal input at pin D_{IN} can bypass the scrambler circuit or mute the speech output.

(3) Limiter circuit – Output from the EMP_{OUT} pin is input into the $SAMP_{IN}$ pin. It is added to an MSK modulation signal in the adder amplifier AMP2 and input into the limiter. The limiter level is controlled by the input to LIM_{IN}. The voice signal is limited to the 3KHz band by the splatter filter LPF2 and output from the MOD pin.

2. Reception Filter Block

The band of the reception speech signal is limited by a filter consisting of input amplifier AMP3 and an external RC. The gain is controlled by external resistors R4 and R5.

(1) Descrambler circuit – The input signal input into the scrambler circuit passes through LPF4 and is output as an ordinary speech signal. The speech input is muted or can bypass the descrambler circuit with a serial signal input to pin D_{IN}.

(2) Expander Coupler – The output from the descrambler circuit is sent to the external expander through pin EXP_{IN}. The output from the expander circuit is merged with a TONE signal by adder amplifier AMP4 and placed at pin $RAMP_{OUT}$ as the receiver acoustic signal.

3. MSK Modem Block

(1) Modulator circuit (MSK modulator) – Synchronous with the transmitter SCK, a 1200Hz sine wave is generated for “1” data input to pin SD, and a 1,800Hz sine wave signal for “0” data is output from pin S_{OUT}. The output signal is synthesized with the transmission speech signal by adder amplifier AMP2.

(2) Demodulator circuit (MSK demodulator) – The reception signal is input to LPF6 through input gain amplifier AMP3 in reception filter unit. LPF6 eliminates all noise components except 1200Hz and 1800Hz from the input signal and feeds the output to slicer circuit 1 which converts the analog input to a digital signal. The output from the slicer circuit is used by the differential detector to generate reproduced data. After LPF3 eliminates the noise components of the regenerated data from the differential detector, slicer 2 converts the regenerated data to digital signals. The DPLL circuit generates the reception clock signal RCK which is synchronized with the regenerated data signal, and outputs the regenerated data from pin RD. This circuit has a built–in frame detecting function and sets pin FD_{OUT} at “H” level when the regenerated data output from pin RD matches the frame synchronization pattern. The serial signal can select the frame synchronization pattern for the parent or child units.

2. Digital Block

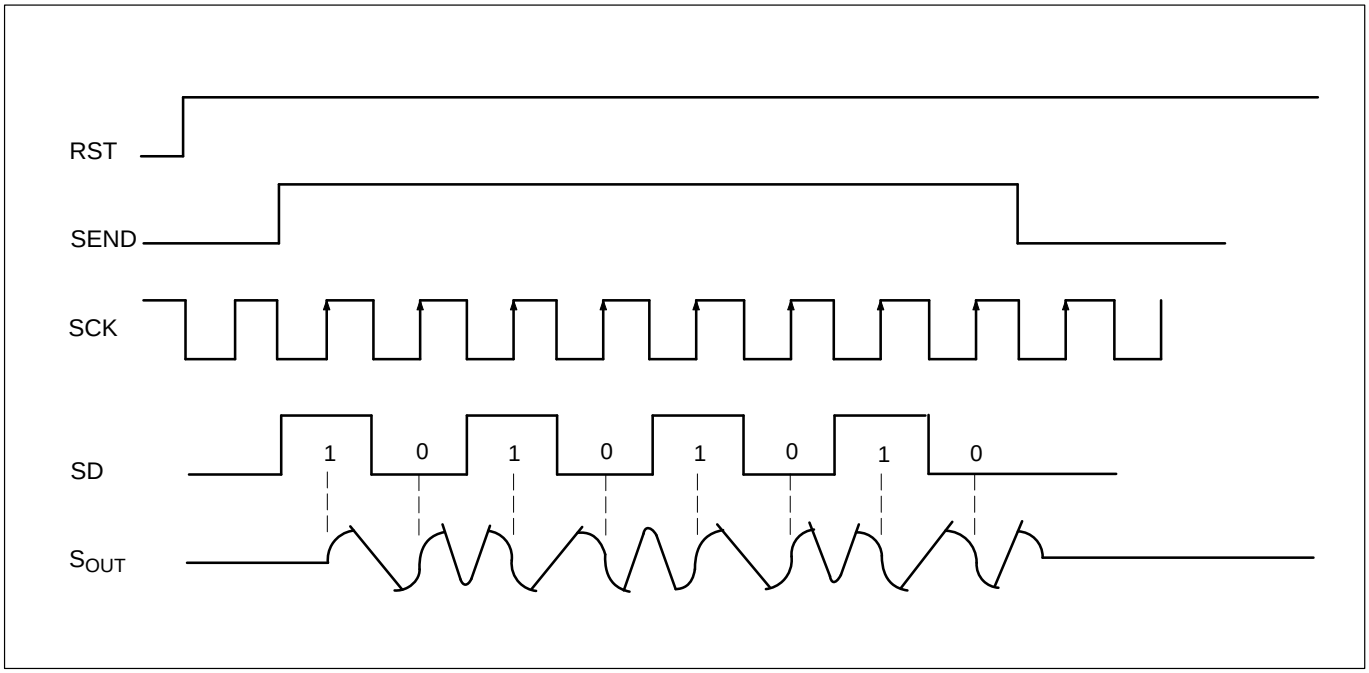
(1) Timing generator circuit – The timing generator circuit uses an external quartz oscillator element (3.6864MHz or 3.456MHz) and its built–in quartz oscillator circuit to generate the basic clock signal. The MSK modulator, MSK demodulator and transmitter and receiver filters share clock signals from the basic clock signal.

(2) Serial interface circuit – When the serial interface circuit receives a serial signal through serial signal pins D_{IN}, DCK and DSTB it can set up the stand–by or bypass mode, turn the transmitter/receiver mute function on and off, and set the frame synchronization pattern. A microcomputer may be used to supply a serial input to the serial interface circuit.

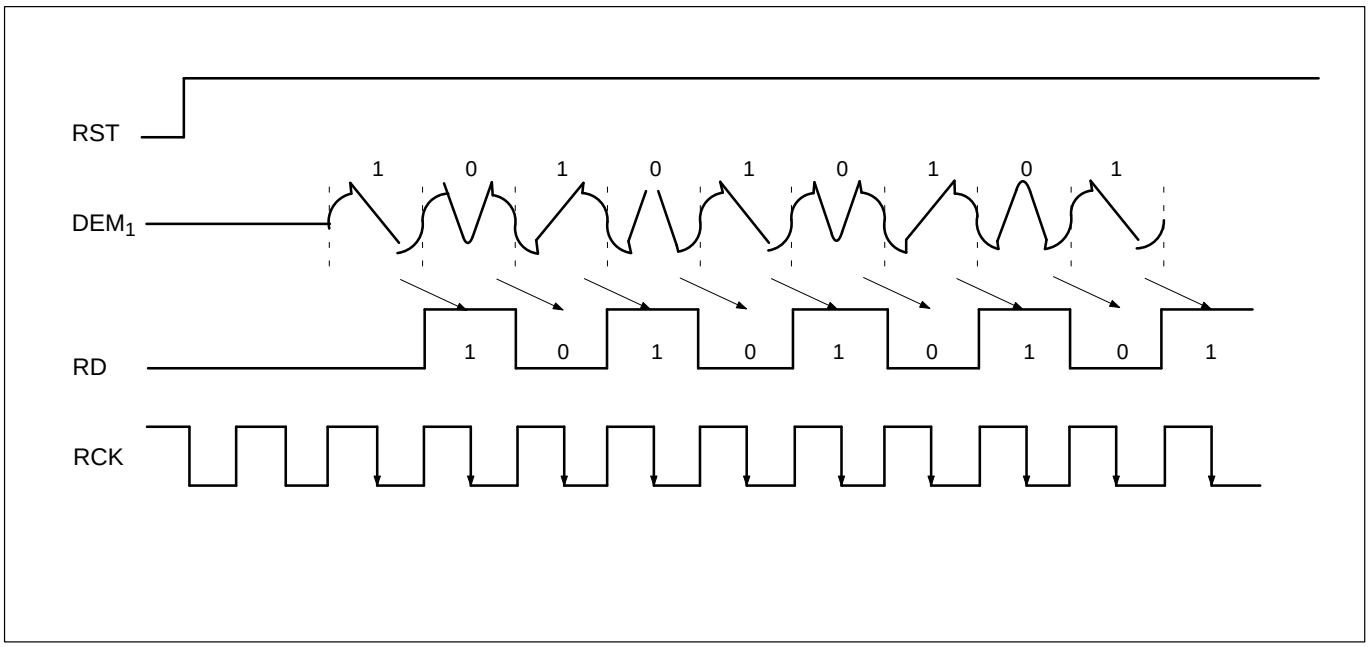
OPERATIONAL DESCRIPTIONS

1. MSK Modem Operation Timing

(1) Modulation mode timing chart – When the SEND pin is on “H” level, at the rising edge of SCK the SD pin outputs a 1200Hz sine signal for “1” and an 1800Hz sine signal or “0” from the S_{OUT} pin.

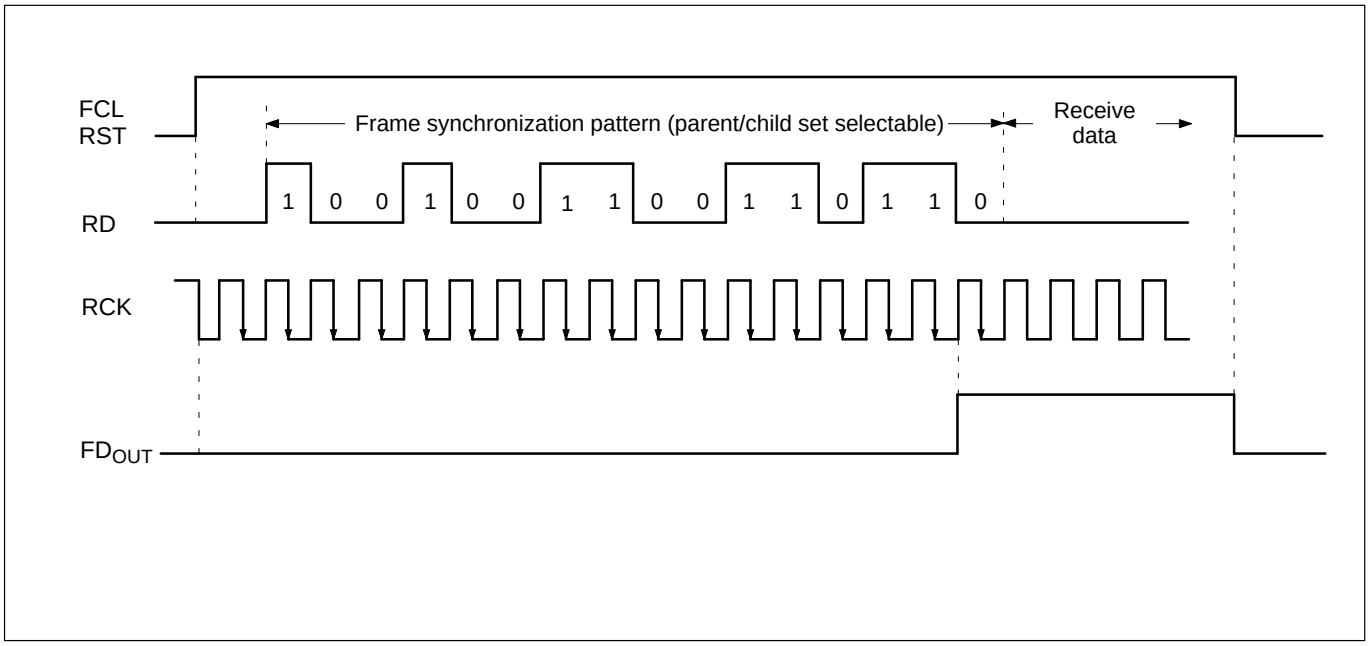


(2) Demodulation mode timing chart – At the falling edge of RCK, the DEM_1 pin outputs a 1200Hz sine signal for “1” and an 1800Hz sine signal for “0”.

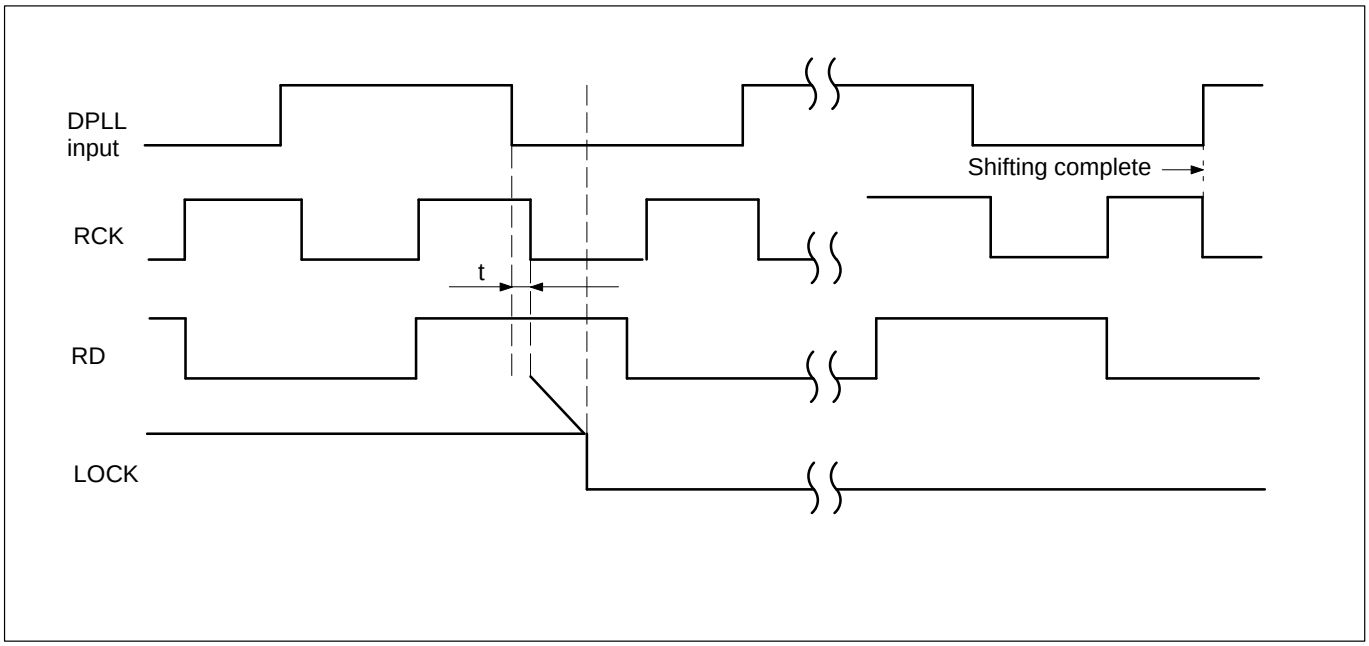


(3) Frame detecting mode timing chart – The bit pattern used for frame detection is identified by the fifth bit of the serial signal which is input to pin D_{IN}. The following bit patterns are generated according to the state of this signal.

Bit 5 = 1: "1001 0011 0011 0110" (from parent telephone set to child telephone set)
Bit 5 = 0: "1100 0100 1101 0110" (from child telephone set to parent telephone set)



(4) Timing for shifting DPLL – As the pulse interval (t) between the falling edge of DPLL and the falling edge of RCK becomes $^1/_4$ period of RCK or less, pin LOCK goes low and the timing of DPLL input is shifted to that of RCK, which maintains the lock state.



2. Limitter Circuit

The limitter in the limitter unit keeps the level of the LIM_{OUT} signal to its upper limit when the input to pin $SAMP_{OUT}$ exceeds the upper limit of the limitter input and to its lower limit when the input is below the lower limit of the limitter input.

(1) When pin LIM_{IN} is open.

LIM_{IN} input level	**$SAMP_{OUT}$ input level**	**LIM_{OUT} output level**	**Remarks**
LIM_{IN} pin open V_{DD} = 5.0V	$V_I > \frac{V_{DD}}{2} + 0.25$	$\frac{V_{DD}}{2} + 0.25$	Upper limit
	$\frac{V_{DD}}{2} + 0.25 \geq V_I \geq \frac{V_{DD}}{2} - 0.25$	V_I	–
	$\frac{V_{DD}}{2} - 0.25 > V_I$	$\frac{V_{DD}}{2} - 0.25$	Lower limit

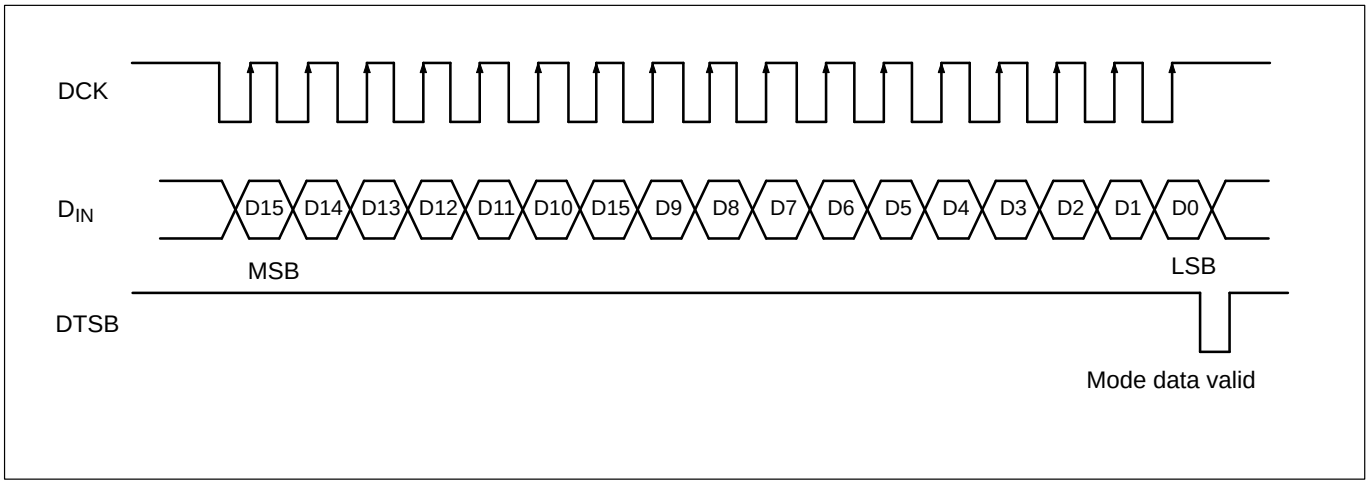
(1) When pin LIM_{IN} is set to V_{LIM}.

LIM_{IN} input level	**$SAMP_{OUT}$ input level**	**LIM_{OUT} output level**	**Remarks**
LIM_{IN} pin = V_{LIM}	$V_I > V_{DD} - V_{LIM}$	$V_{DD} - V_{LIM}$	Upper limit
	$V_{DD} - V_{LIM} \geq V_I \geq V_{LIM}$	V_I	–
	$V_{LIM} > V_I$	V_{LIM}	Lower limit

3. Serial Interface Circuit

The standby and mute modes are controlled by bit codes which are received in the form of serial signals.

(1) Serial signal input timing – Serial signals are read at the rising edge of the DCK clock from pin D_{IN}. The mode data becomes valid at the rising edge of the DSTB signal.



(2) Serial signal bit codes

Serial Signal Bit No.	Select Function
D2, D1, D0	Select the stand–by mode
D4, D3	Select the mute mode
D5	Selects the synchronization frame pattern
D6	Selects the scrambler/descrambler circuits bypass mode
D7	Selects the compander circuit bypass mode
D8	Undefined
D9	Selects the oscillation frequency
D15, D14, D13, D12, D11, D10	Inputs “000000”

Remarks: The bit code is set to “0000000000000010” at reset time (only bit D2 is 1 and the other bits are all zeros).

- Stand–by mode selection code table
  The stand–by mode is defined by bits D2, D1, and D0.

Mode			M0	M1[1]	M2	M3	M4[2]	M5[1]
Input code (D2, D1, D0)			000	001	010	011	100	101
Block name		Circuit name						
Transmitter	Speech filter	AMP1	O	O	X	X	X	X
		LPF1	O	O	X	X	X	X
		Post filter 1	O	O	X	X	X	X
		AMP2	O	O	X	X	X	X
		Limiter	O	O	X	X	X	X
		LPF2	O	O	X	X	X	X
		Post filter 3	O	O	X	X	X	X
		AMP5	O	O	X	X	X	X
	Modem	Modulator circuit	O	X	X	X	X	X
Receiver	Speech filter	AMP3	O	O	O	O	X	X
		LPF4	O	O	O	X	X	X
		Post filter 3	O	O	O	X	X	X
		AMP4	O	O	O	X	X	X
	Modem (modulator circuit)	BPF1	O	O	O	O	X	X
		Slicer 1	O	O	O	O	X	X
		LPF3	O	O	O	O	X	X
		Slicer 2	O	O	O	O	X	X
Others		OSC	O	O	O	O	O	X
		SCK	O	X	O	O	O	X
		$^1/_2$ V_{DD} generation	O	O	O	O	X	X

O: Active mode
X: Inactive mode
1. The SCK output is fixed in stand–by modes M1 and M5.
2. Mode M4 is selected at reset time.

- Mute mode

Bit No.	Parameter	"0"	"1"	Remarks
D3	Transmit mute mode	Operating	Mute	SW0
D4	Receive mute mode	Operating	Mute	SW1

- Synchronization frame pattern

Bit No.	Parameter	"0"	"1"	Remarks
D5	Mode for selecting between the parent and child bit patterns	Parent side	Child side	

- Scrambler/descrambler bypass mode

Bit No.	Parameter	"0"	"1"	Remarks
D6	Scrambler/descrambler bypass mode	Used	Bypass mode	SW2

- Compander circuit bypass mode

Bit No.	Parameter	"0"	"1"	Remarks
D7	Compander bypass mode	Used	Bypass mode	SW3

- Oscillation frequency

Bit No.	Parameter	"0"	"1"	Remarks
D9	Crystal frequency select mode	3.6864MHz	3.456MHz	–

- D10 to D15

Bit No.	Parameter	"0"	"1"	Remarks
D10 to D15	–	Fixed	–	–

Note: Bit D8 is not used.
Bits D10 to D15 is set to 0.

RECOMMENDED OPERATING CONDITIONS

(A. GND = D. GND = 0V[1])

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Power voltage	V_{DD}	V_{DDD}, V_{DDA} [2]	3.0 [3]	5.0	5.5	V
Input voltage	V_I	All input pins	0	–	V_{DD}	V
Analog output load resistance	R_{L1}	AF_{IN2}, EXP_{OUT}, MOD $SAMP_{OUT}$, $TAMP_{OUT}$ $RAMP_{OUT}$, DEM_2, EXP_{IN} $^1/_2$ V_{DDOUT}, AF_{OUT}	10	–	–	kΩ
	R_{L2}	CC_{OUT}, LIM_{OUT}, S_{OUT}	50	–	–	kΩ
Analog output load resistance	C_L	All analog output pins	–	–	30	pF
OSC pin load capacitance	C_{OSC}	OSC_{IN}, OSC_{OUT}	20	30	50	pF
Ambient temperature	T_A	–	–30	25	70	°C

1. GND = A. GND = D. GND
2. $V_{DD} = V_{DDD} = V_{DDA}$
3. MB86465A can operate at up to 2.7V, however the electrical characteristics are not guaranteed at supply voltage of 2.7 to 3.0V.

ELECTRICAL CHARACTERISTICS

1. DC characteristics

(V_{DD} = 3.0V to 5.5V, A. GND = D. GND = 0V, T_A = –30°C to +70°C)

Parameter	Symbol	Pin name	Conditions	Rating			Unit
				Min.	Typ.	Max.	
Supply current	$I_{DD}0$	V_{DDD}, V_{DDA}	Stand–by mode 0	3	7.5	13.5	mA
	$I_{DD}1$		Stand–by mode 1	2.5	7.2	13.0	mA
	$I_{DD}2$		Stand–by mode 2	1.5	4.5	8.0	mA
	$I_{DD}3$		Stand–by mode 3	1.0	3.5	6.5	mA
	$I_{DD}4$		Stand–by mode 4	0.1	1.0	2.0	mA
	$I_{DD}5$		Stand–by mode 5	–	25	100	µA
L level input voltage	V_{iL}	Digital input pin	–	0	–	$0.3 \times V_{DD}$	V
H level input voltage	V_{IH}		–	$0.7 \times V_{DD}$		V_{DD}	V
L level input current	I_{IL}	Analog input pin (SD, SEND, D_{IN}, DCK, DSTB)	V_I = 0V	–10	–	10	µA
H level input current	I_{IH}		$V_I = V_{DD}$	–10	–	10	µA
L level output voltage	V_{OL}	Digital output pin	I_{OL} = 0.5mA	0	–	$0.2 \times V_{DD}$	V
H level output voltage	V_{OH}		I_{OH} = –0.5mA	$0.8 \times V_{DD}$		V_{DD}	V
Pull–up resistance	R_{PLU}	RST	–	50	100	200	kΩ
Oscillation frequency	f_{OSC}	OSC_{IN}, OSC_{OUT}	Mode 0	–	3.6864	–	MHz
			Mode 1	–	3.456	–	
Analog input resistance 1	R_{AIN1}	$^1/_2V_{DDIN}$	–	50	100	200	kΩ
Analog input resistance 2	R_{AIN3A}	LIM_{IN}	Operating–time, across this pin and $^1/_2V_{DD}$	10	20	40	kΩ
	R_{AIN3B}		PD mode, across this pin and GND	90	180	360	
Analog output load resistance	R_{L1}	AF_{IN2}, EMP_{OUT} $TAMP_{OUT}$, MOD $SAMP_{OUT}$, DEM_2 $RAMP_{OUT}$, EXP_{IN}	Across this pin and $^1/_2V_{DD}$	10	–	–	kΩ
	R_{L2}	CC_{OUT}, S_{OUT}, LIM_{OUT}		50	–	–	
Analog output load capacitance 1	C_{L1}	AF_{IN2}, CMP_{IN} EXP_{OUT}, S_{OUT} $SAMP_{OUT}$, DEM_2 MOD, LIM_{OUT} $RAMP_{OUT}$, EXP_{IN}	–	–	–	100	pF
Analog input voltage range	V_{IA}	CMP_{OUT}	–	$^1/_4V_{DD}$	–	$^3/_4V_{DD}$	V
Analog output voltage range	V_{OA}	AF_{IN2}, EMP_{OUT} MOD $SAMP_{OUT}$, DEM_2 $EXPI_{IN}$, $RAMP_{OUT}$ $TAMP_{OUT}$, LIM_{OUT}	–	$^1/_4V_{DD}$	–	$^3/_4V_{DD}$	V
Modulator output voltage	V_{MOT1}	S_{OUT}	Operating time	$0.16 \times V_{DD}$	$0.2 \times V_{DD}$	$0.24 \times V_{DD}$	Vp–p
	V_{MOT2}		Operating–time offset voltage	$^1/_2V_{DD}$ –0.3	$^1/_2V_{DD}$	$^1/_2V_{DD}$ +0.3	V
	V_{MOT3}		SEND = “L”	$^1/_2V_{DD}$ –0.3	$^1/_2V_{DD}$	$^1/_2V_{DD}$ +0.3	
Limiter H level input voltage	V_{DLL}	$SAMP_{OUT}$ – LIM_{OUT}	LIM_{IN} pin = open	$^1/_2V_{DD}$ +0.04V_{DD}	$^1/_2V_{DD}$ +0.05V_{DD}	$^1/_2V_{DD}$ +0.06V_{DD}	V
			LIM_{IN} pin = V_{LIM}	$^1/_2V_{DD}$+0.8 ×($^1/_2V_{DD}$ – V_{LIM})	$^1/_2V_{DD}$+1.0 ×($^1/_2V_{DD}$ – V_{LIM})	$^1/_2V_{DD}$+1.2 ×($^1/_2V_{DD}$ – V_{LIM})	
Limiter L level input voltage	V_{DLL}	$SAMP_{OUT}$ – LIM_{OUT}	LIM_{IN} pin = open	$^1/_2V_{DD}$ –0.06V_{DD}	$^1/_2V_{DD}$ –0.05V_{DD}	$^1/_2V_{DD}$ –0.04V_{DD}	V
			LIM_{IN} pin = V_{LIM}	$^1/_2V_{DD}$–1.2 ×($^1/_2V_{DD}$ – V_{LIM})	$^1/_2V_{DD}$–1.0 ×($^1/_2V_{DD}$ – V_{LIM})	$^1/_2V_{DD}$–0.8 ×($^1/_2V_{DD}$ – V_{LIM})	

2. Transmission characteristics

(V_{DD} = 3.0V to 5.5V, A. GND = D. GND = 0V, T_A = –30°C to +70°C)

Parameter	Symbol	Pin name	Conditions	Rating			Unit
				Min.	Typ.	Max.	
Transmitter gain 1	T_{GAIN1}	AF_{IN1} –MOD	Input: –27dBV, 1kHz $R_1 = R_2$, $R_7 = R_9$, $R_{10} = R_{11}$ Scrambler and compander bypass modes	7.0	9.0	11.0	dB
Transmit mute	T_{MUTE}	AF_{IN1} –MOD	Input: –27dBV, 1kHz $R_1 = R_2$, $R_7 = R_9$, $R_{10} = R_{11}$ Scrambler and compander bypass modes Transmitter mute mode	45	–	–	dB
Transmitter signal-to-noise ratio	$T_{S/N}$	AF_{IN1}–MOD	Input: –27dBV, 1kHz $R_1 = R_2$, $R_7 = R_9$, $R_{10} = R_{11}$ Scrambler and compander bypass modes Band width = 50Hz to 20kHz	40	–	–	dB
Transmitter distortion factor	$T_{S/D}$			–	–	–40	dB
Receiver gain 1	R_{GAIN1}	DEM_1 – $RAMP_{OUT}$	Input: –26dBV, 1kHz $R_4 = R_6$, $R_{12} = R_{14}$ Scrambler and compander bypass modes	–1.0	0.0	1.0	dB
Receiver mute	R_{MUTE}	DEM_1 – $RAMP_{OUT}$	Input: –18dBV, 1kHz $R_4 = R_6$, $R_{12} = R_{14}$ Scrambler and compander bypass modes Receiver mute mode	45	–	–	dB
Receiver signal-to-noise factor	$R_{S/N}$	DEM_1 – $RAMP_{OUT}$	Input; –18dBV, 1kHz $R_4 = R_6$, $R_{12} = R_{14}$ Scrambler and compander bypass modes Band width = 50Hz to 20kHz	40	–	–	db
Receiver distortion factor	$R_{S/D}$			–	–	–40	
Transmitter gain 2	T_{GAIN2}	AF_{IN1} – EMP_{OUT}	Input: –27dBV, 1kHz $R_1 = R_2$, $R_7 = R_9$, $R_{10} = R_{11}$ Scrambler and compander bypass modes	–1.0	0.0	1.0	dB
Transmitter gain 3	T_{GAIN3}	$SAMP_{IN}$ – $TAMP_{OUT}$	Input: –27dBV, 1kHz $R_7 = R_9$, $R_{10} = R_{11}$	8.0	9.0	10.0	dB
Total signal-to-noise ratio	S//N	AF_{IN1} – $RAMP_{OUT}$	Input: –18dBV, 1kHz $R_1 = R_2$, $R_4 = R_6$, $R_7 = R_9$ $R_{10} = R_{11}$, $R_{12} = R_{14}$ When $TAMP_{OUT}$ and DEM_1 are connected Band width = 0.3kHz to 3kHz	35	–	–	dB
Total distortion factor	S/D			–	–	–35	

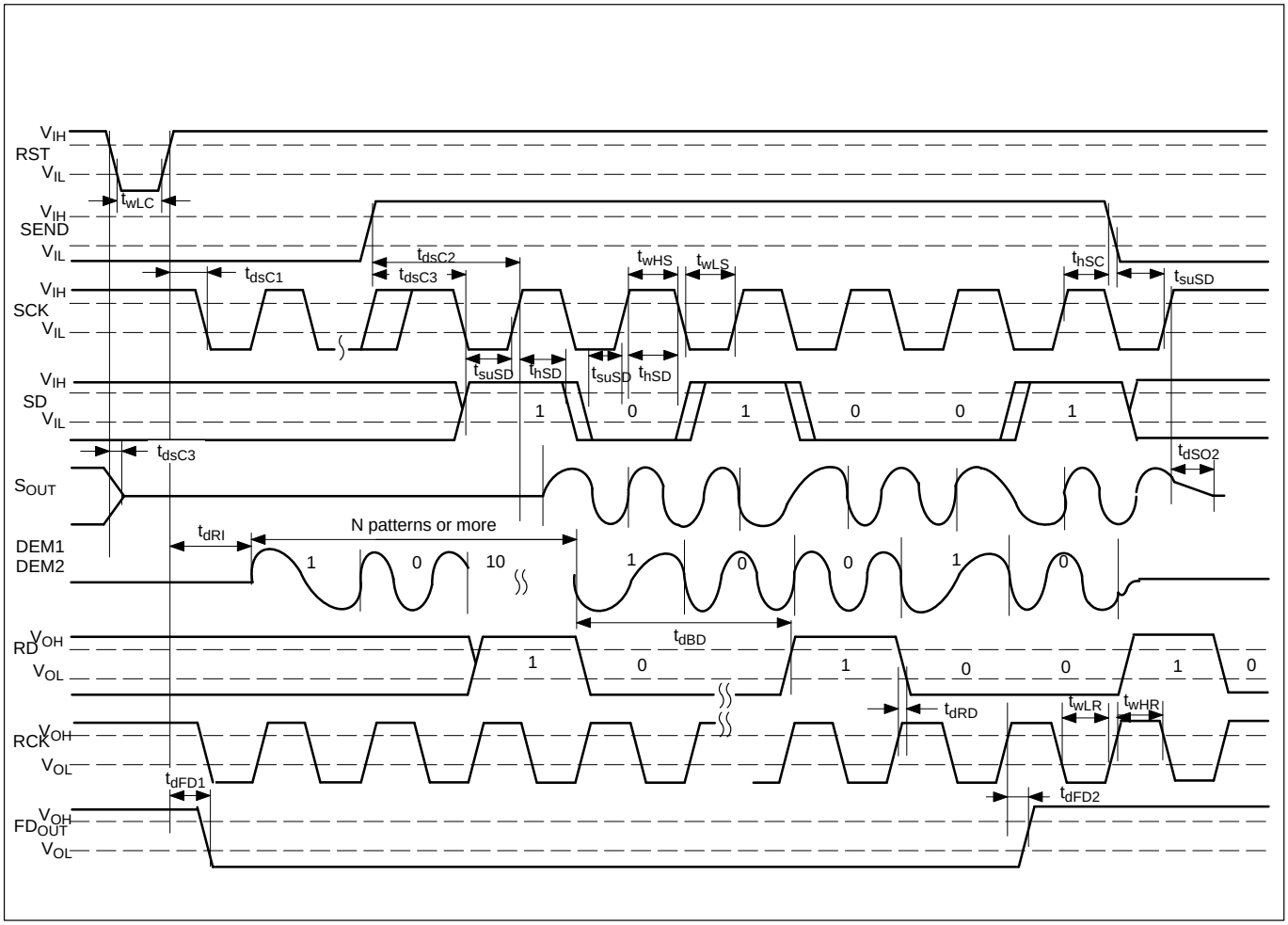
3. AC characteristics

(V_{DD} = 3.0V to 5.5V, A. GND = D. GND = 0V, T_A = –30°C to +70°C)

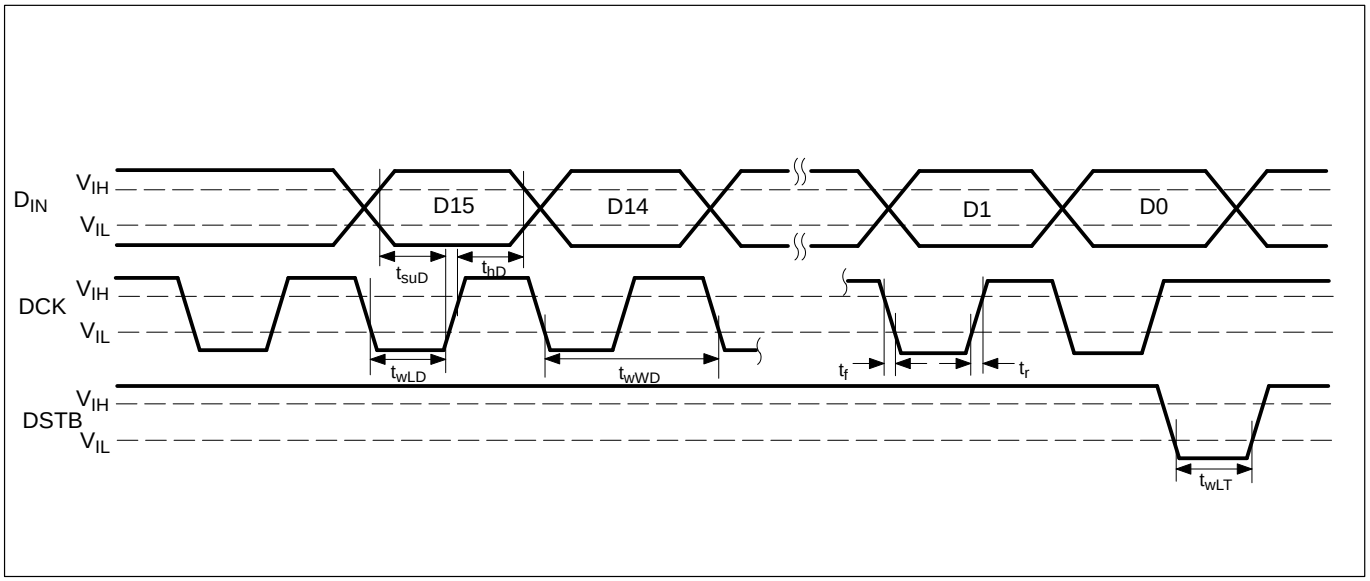
Parameter	Symbol	Pin name	Conditions	Rating			Unit
				Min.	Typ.	Max.	
SCK delay time 1	t_{dSC1}	SCK	–	0	150	417	µs
SCK delay time 2	t_{dSC2}	SCK	–	417	570	834	µs
SCK delay time 3	t_{dSC3}	SCK	–	0	150	417	µs
FD_{OUT} delay time 1	t_{dFD1}	FD_{OUT}	–	0	–	1	µs
FD_{OUT} delay time 2	t_{dFD2}	FD_{OUT}	–	0	–	1	µs
SDK L level width	t_{WLS}	SCK	–	390	417	444	µs
SCK H level width	t_{WHS}	SCK	–	390	417	444	µs
SEND setup time	t_{suSE}	SEND	–	1	–	–	µs
SEND hold time	t_{hSE}	SEND	–	1	–	–	µs
SD setup time	t_{suSD}	SD	–	1	–	–	µs
SD hold time	t_{hSD}	SD	–	1	–	–	µs
S_{OUT} delay time 1	t_{dSO1}	S_{OUT}	–	0	–	20	µs
S_{OUT} delay time 2	t_{dSO2}	S_{OUT}	–	0	–	20	µs
S_{OUT} delay time 3	t_{dSO3}	S_{OUT}	–	0	–	10	µs
MSK input disenabled time	t_{dRI}	DEM_1, DEM_2	–	0	–	10	ms
Number of shift bits	N	–	DEM_1 DEM_2 no-noise	–	–	15	bit
Demodulator delay time	t_{dBD}	RD	$N \geq DEM_1$ DEM_2 no noise	1483	1900	2317	µs
RD timing	t_{dRD}	RD	–	–1	–	–1	µs
RCK L level width	$t_{\omega LR}$	RCK	$N \geq DEM_1$ DEM_2 no noise	338	417	496	µs
RDK H level width	$t_{\omega HR}$	RCK	$N \geq DEM_1$ DEM_2 no noise	338	417	496	µs
RST L level width	$t_{\omega LC}$	RST	–	20	–	–	µs
Digital input rise time	t_r	RST, SEND, SD, DCK, DSTB, D_{IN}	–	–	–	100	ns
Digital input fall time	t_f	RST, SEND, SD, DCK, DSTB, D_{IN}	–	–	–	100	ns
D_{IN} setup time	t_{suD}	D_{IN}	–	100	–	–	ns
D_{iN} hold time	t_{hD}	D_{IN}	–	100	–	–	ns
Strobe setup time	t_{suT}	DSTB	–	100	–	–	ns
DCK L level width	$t_{\omega LD}$	DCK	–	100	–	–	ns
DCK period	$t_{\omega WD}$	DCK	–	2	–	–	µs
Strobe L level width	$t_{\omega LT}$	DSTB	–	100	–	–	ns

TIMING CHART

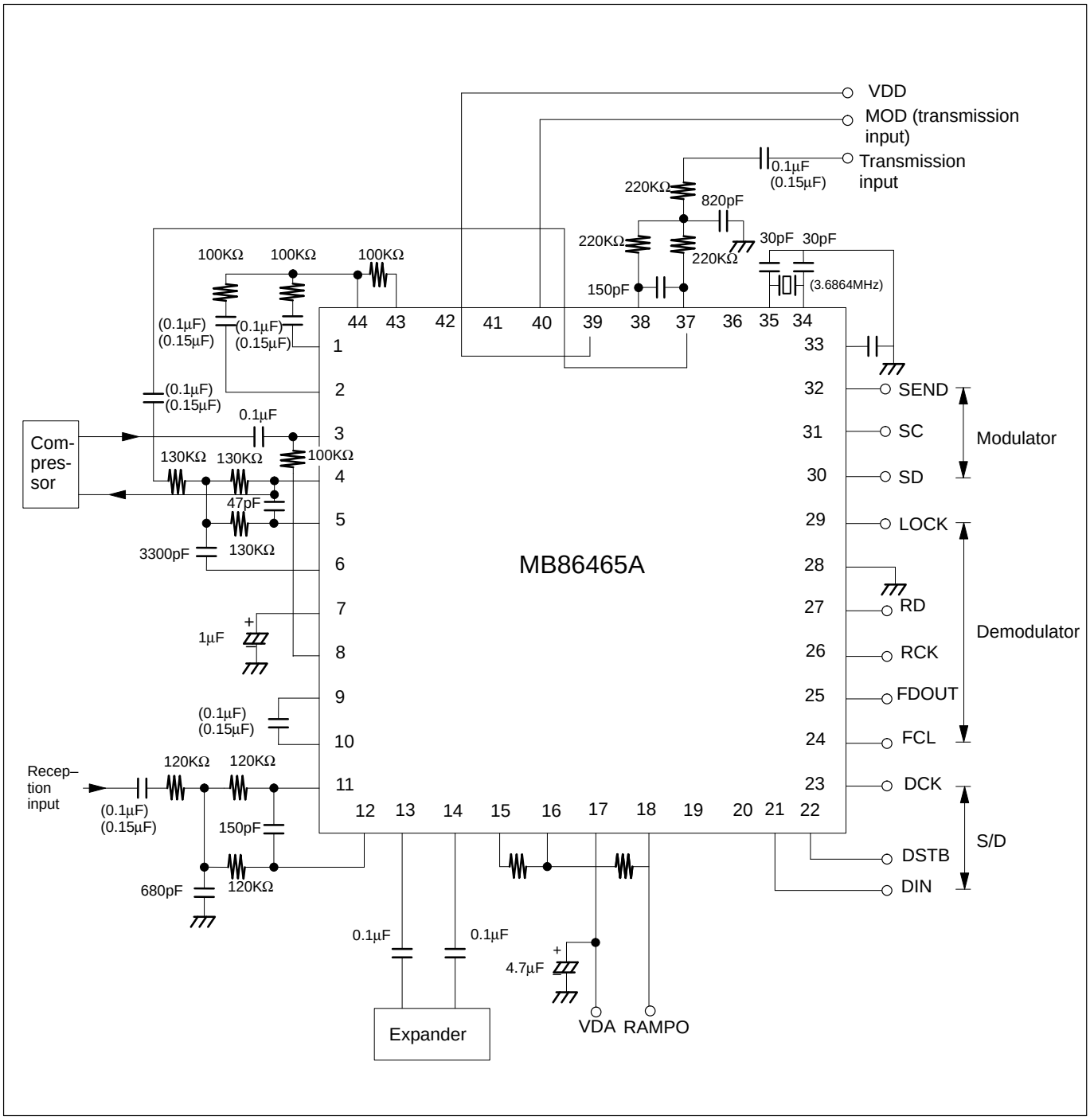
1. MSK modem timing chart



2. Serial interface timing chart

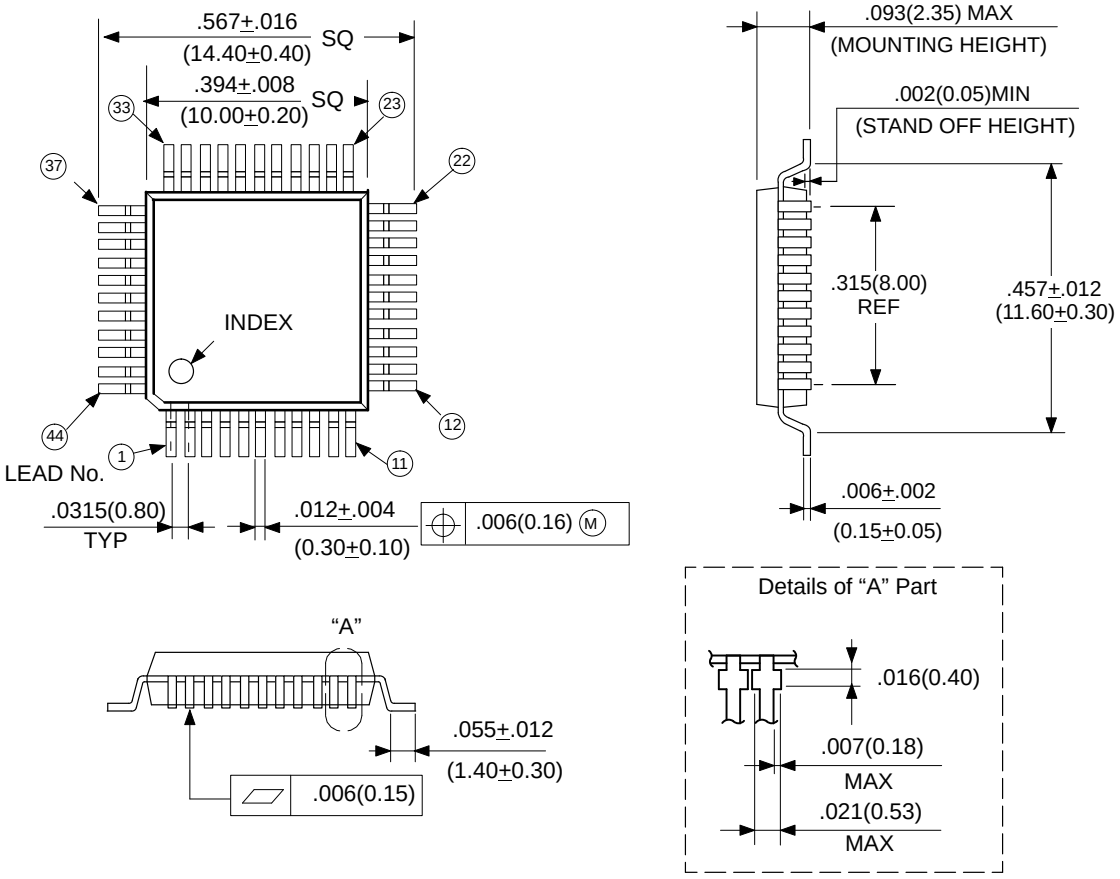


EVALUATION BOARD CIRCUIT



PACKAGE DIMENSIONS

44-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-44P-M01)



Dimensions in inches (millimeters).

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