March 1992
Edition 3.0B

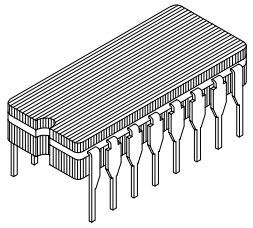
FUJITSU

DATA SHEET

MB6021A and MB6022A
PCM Coders/Decoders

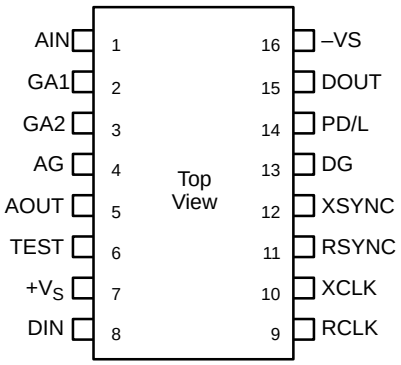
The Fujitsu CMOS MB6020A series consists of both μ-law and A-law single-chip coder/decoder (CODEC) filter ICs for either synchronous-only or synchronous/asynchronous operation. These monolithic, single-channel, voice-frequency CODECs incorporate both transmit and receive circuitries that are used for pulse coded modulation (PCM) systems.

- Transmit high-pass and low-pass filters
- Receive low-pass filter with SinX/X Correction
- Anti-aliasing filter
- Conforms to CCITT and AT&T specifications
- Synchronous and asynchronous operation
- Serial data rates of 64 kHz to 3.152 MHz
- PLL circuits serve as an internal clock generator
- Internal voltage reference
- Internal auto-zero circuit
- TTL-compatible digital interface
- Input gain adjust amplifier
- Pin selectable on-chip analog loopback
- μ-law: MB6021A
  A-law: MB6022A
- Package and Ordering Information:
  16-pin plastic DIP package
  Order as MB6021AP and MB6022AP



Plastic DIP Package
(DIP-16P-M03)

Pin Assignment



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Pin No.	Min.	Max.	Unit
Positive Supply Voltage	$+V_S$	7	–0.3	7	V
Negative Supply Voltage	$–V_S$	16	–7	0.3	V
Test	TEST	6	$–V_S$	$+V_S$	V
Analog Input Voltage	V_{AIN}	1	$–V_S$–0.3	$+V_S$+0.3	V
Digital Input Voltage	V_{DIN1}	8, 9, 10, 11, 12	–0.3	$+V_S$+0.3	V
Digital Input Voltage	V_{DIN2}	14	$–V_S$–0.3	$+V_S$+0.3	V
Storage Temperature	T_{STG}		–55	150	°C

– Note –
Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM

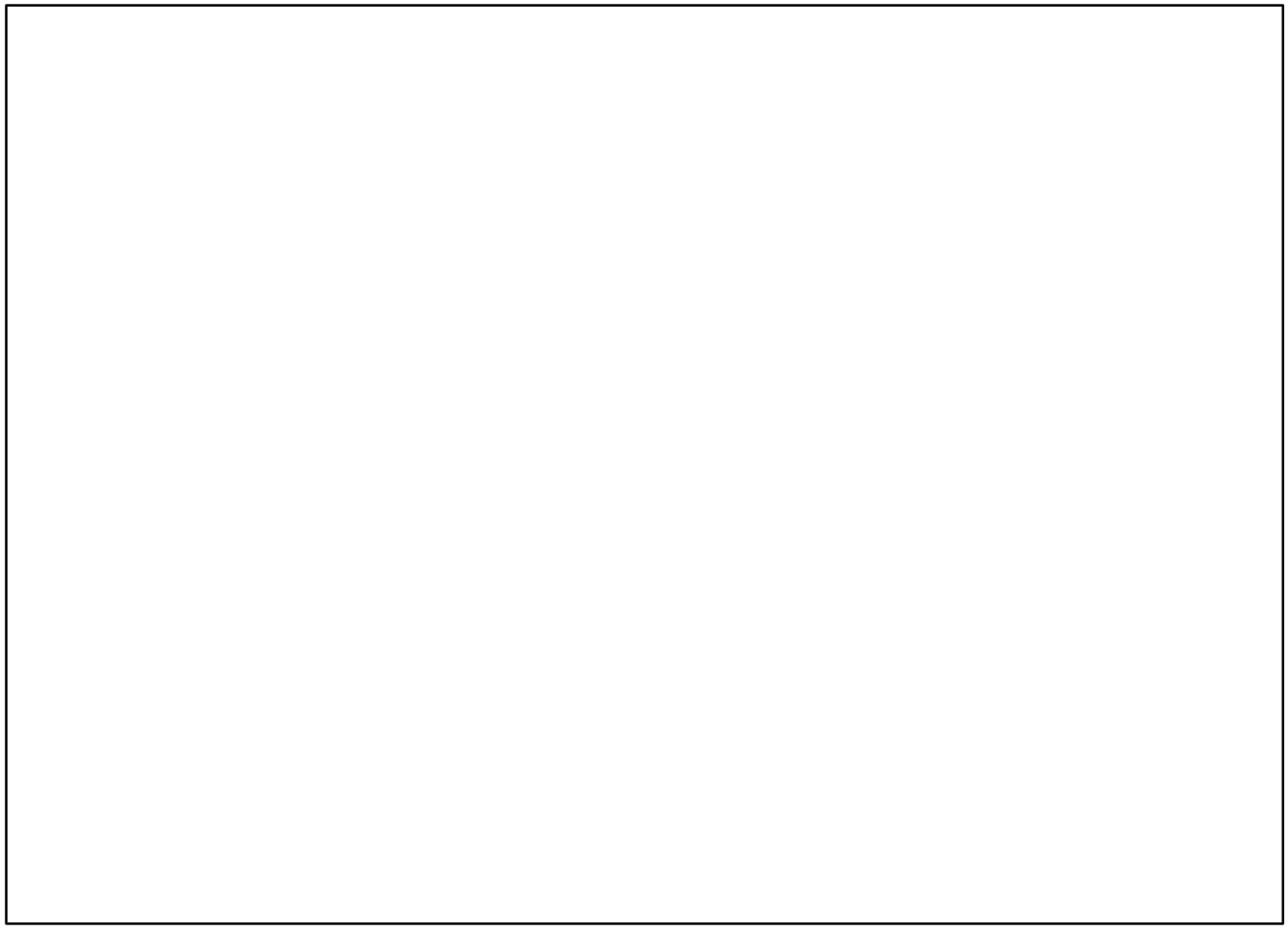


Figure 1. MB6021A and MB6022A Block Diagram

FUNCTIONAL DESCRIPTION

Figure 1 shows a simplifed block diagram of MB6021A and MB6022A.

The Transmit Section in the upper-half of the block diagram is comprised of an input gain amplifier, an anti-aliasing filter (Anti-Alias), a band-pass filter (COS, LPT, and HPF), and a compressing coder (Coder). An auto-zero circuit (AZ) is also included in this section. The Receive Section in the lower half of the block diagram is comprised of an expanding decoder (Decoder) and a low-pass filter (LPF).

Transmit Section

The Transmit Section receives analog signals that are input to an operational amplifier to provide gain adjustment. The signal from the op amp is transmitted to a second-order analog anti-aliasing filter (Anti-Alias). This filter provides attenuation of 40 dB (typical) at the 256 kHz effective clock frequency of the switched capacitor cosine filter (COS). From the cosine filter, the signals enter a fifth-order low-pass filter (LPF) clocked at 128 kHz. From the LPF, the signals pass into a third-order high-pass filter (HPF) clocked at 128 kHz. The resulting band-pass characteristics meet both the D3/D4 specification and the CCIT G.712 recommendation. The output of the high-pass filter is then sampled by the coder (Coder) at 8 kHz. This coder transforms the analog signals into 8-bit words using compression law. The encoded PCM data is then output serially from the Output Register at a frequency determined by the external clock, 64 kHz to 3.152 MHz. An auto-zero circuit (AZ) is utilized for DC offset correction.

Receive Section

The Receive Section's Input Register filter smooths the decoded signals and corrects for SinX/X attenuation caused by the 8 kHz sample and hold operation. The decoder reconstructs the analog signals from the PCM data using expansion law. The output from the decoder is transmitted to a fifth-order low-pass filter (LPF). This LPF smooths the decoded signals and corrects them for the SinX/X attenuation due to the 8 kHz sampling and holding operation.

Internal Clocks

Two independent phase locked loops (PLLs) generate internal clocks for the Transmit and Receive Sections from the respective synchronization clocks (XSYNC and RSYNC).

OPERATING MODES

Analog Loopback Mode

The Analog Loopback Mode allows all decoding and coding functions to be exercised without using the analog input (AIN) and analog output (AOUT). In this mode, a digital input signal is decoded and internally routed to the transmit filters.The output is available from the digital output (DOUT). The analog output (AOUT) is forced to the analog ground (AG) level. The Analog Loopback Mode is selected by connecting the PD/L input to the negative supply voltage (–VS).

Power-down Mode

Two Power-down Modes are provided. The Transmit and Receive Sections independently go into power-down operation in the absence of the respective synchronization clocks (XSYNC and RSYNC). If the external power down input (PD/L) is connected to a TTL low level, both the Transmit and Receive Sections are powered down regardless of the synchronization clocks. During power-down operation, AOUT is forced to the level of AG, and DOUT goes into a high-impedance state.

Test Mode

In the Test Mode the TEST pin is connected to –VS. The Test Mode allows independent evaluation of the coder and decoder. In this mode, AIN is internally connected to the input of the coder and its output is available on the DOUT pin. The output of the decoder is made available on the AOUT pin.

PIN DESCRIPTION

Pin Name	Pin No.	Description
AIN	1	**Analog Input.** This is an input pin for analog signals to be filtered and coded.
GA1 GA2	2 3	**Gain Adjust 1** **Gain Adjust 2** These pins are provided for adjusting the gain of the Transmit Section. GA1 and GA2 are the inverted input and output of the amplifier, respectively. GA2 can drive a load impedance of 10 to 20 kΩ and 50 pF or less.
AG	4	**Analog Ground.** All analog signals are referenced to this pin.
AOUT	5	**Analog Output.** This pin outputs the decoded and filtered analog signals. It can drive a load impedance of 3 kΩ or greater, and 100 pF or less. This output is forced to AG level in the Analog Loopback Mode and Power-down Mode.
TEST	6	**Test.** If this pin is at the TTL low level or left open, normal operating mode is selected.If it is connected to –VS, the TEST mode is selected. In TEST mode, A_{IN} is internally connected to the coder input and its output is available on the D_{OUT} pin. Decoder output is available on the A_{OUT} pin. Applied voltage should not exceed 2.0 V.
+VS	7	**Positive Voltage Supply:** +5 V ± 5%.
DIN	8	**Digital Input.** This is a TTL-compatible input to the decoder and accepts an eight-bit data word into the shift register on the falling edge of RCLK.
RCLK	9	**Receive Clock.** This TTL-compatible input defines the bit rate on the receive PCM highway. The device can operate with clock rates of 64 kHz to 3.152 MHz. The digital PCM codes are accepted on the falling edge of the clock.
XCLK	10	**Transmit Clock.** This TTL-compatible input defines the bit rate on the transmit PCM highway. The device can operate with bit rates of 64 kHz to 3.152 MHz. The digital PCM codes are shifted out of the digital output (DOUT) pin on the rising edge of the XCLK.
RSYNC	11	**Receive Synchronization Clock.** This TTL-compatible input defines the beginning of the receive time slot on the receive PCM highway. It must be synchronized with RCLK. The clock rate is typically 8 kHz and its duration can be equal to or more than one RCLK cycle.
XSYNC	12	**Transmit Synchronization Clock.** This TTL-compatible input defines the beginning of the transmit time slot on the transmit PCM highway. It must be synchronized with XCLK. The clock rate is typically 8 kHz and its duration can be equal to or more than one XCLK cycle.
DG	13	**Digital Ground.** All digital signals are referenced to this pin.
PD/L	14	**Power-down/Analog Loopback.** This three-level input is provided for the selection of the Power-down Mode or Analog Loopback Mode. If this pin is at the TTL high level, the normal operation is selected. If this pin is at the TTL low level, the device is powered down regardless of the synchronization clocks. If this pin is connected to –VS, the Analog Loopback Mode is selected. In this mode, the output of the receive filter is internally connected to the input of the transmit filter and AOUT is forced to AG level.
DOUT	15	**Digital Output.** This is a TTL-compatible open-drain output. A pull-up resistor with greater than 0.5 kΩ must be connected to +VS. PCM digital codes are shifted out of the device on the rising edges of XCLK in a serial format. This output goes into high-impedance state when eight bits are shifted out of the output shift register.
–VS	16	**Positive Voltage Supply:** –5 V ± 5%.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value			Unit
			Min.	Typ.	Max.	
Positive Supply Voltage	7	+VS	+4.75	+5.0	+5.25	V
Negative Supply Voltage	16	–VS	–5.25	–5.0	–4.75	V
Digital Output Load Resistance	15	R_{DL}	0.5	—	—	kΩ
Digital Output Load Capacitance	15	C_{DL}	—	—	144	pF
Analog Output Load Resistance	5	R_L	3	—	—	kΩ
Analog Output Load Capacitance	5	C_L	—	—	100	pF
Operating Temperature	—	T_{OP}	0	25	70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Positive Supply Current	$+I_{VS}$	7	Operating		7.0	10.0	mA
Negative Supply Current	$-I_{VS}$	16	Operating	–10.0	–5.0	—	mA
Positive Supply Current	$+I_{VSST}$	7	XSYNC = RSYNC = VIL SYNC = VIL	—	1.0	2.0	mA
Power Down Mode			PD/L = VIL	—	0.3	1.0	mA
Negative Supply Current	$-I_{VSST}$	16	XSYNC = RSYNC = VIL SYNC = VIL	–0.5	–0.1	—	mA
Power Down Mode			PD/L = VIL	–0.5	–0.1	—	mA
Digital Input High Voltage	V_{IH}	8, 9, 10, 11, 12, 14		2.0	—	+VS	V
Digital Input Low Voltage	V_{IL}	8, 9, 10, 11, 12, 14		0	—	0.8	V
Digital Input High Current	I_{IH}	8, 9, 10, 11, 12, 14		—	—	10	µA
Digital Input Low Current	I_{IL}	8, 9, 10, 11, 12, 14		—	—	10	µA
Digital Input Capacitance	C_{DIN1}	8, 9, 10, 11, 12, 14		—	—	10	pF
Digital Input Capacitance	C_{DIN2}	—		—	—	20	pF
Digital Output Low Voltage	V_{OL1}	15	R_{DL} = 0.5 kΩ $+I_{OL}$ = 0.4 mA	—	—	0.4	V
Digital Output Leakage Current	I_{LO}	15		—	—	10	µA
Digital Output Capacitance	C_{DOUT}	15		—	—	12	pF
Analog Input Offset Voltage	A_{INOFF}	1		–200	0	200	mV
Analog Input Resistance	R_{AIN}	1		300	—	—	kΩ
Analog Input Capacitance	C_{AIN}	1		—	—	10	pF
Analog Output Offset Voltage	A_{OUTOFF}	5		–150	—	150	mV
Analog Output Resistance	R_{AOUT}	5		—	10	30	Ω
Pull Down Current	I_{PLD}	6	V_{IN} =+2.0 V	0	—	80	µA

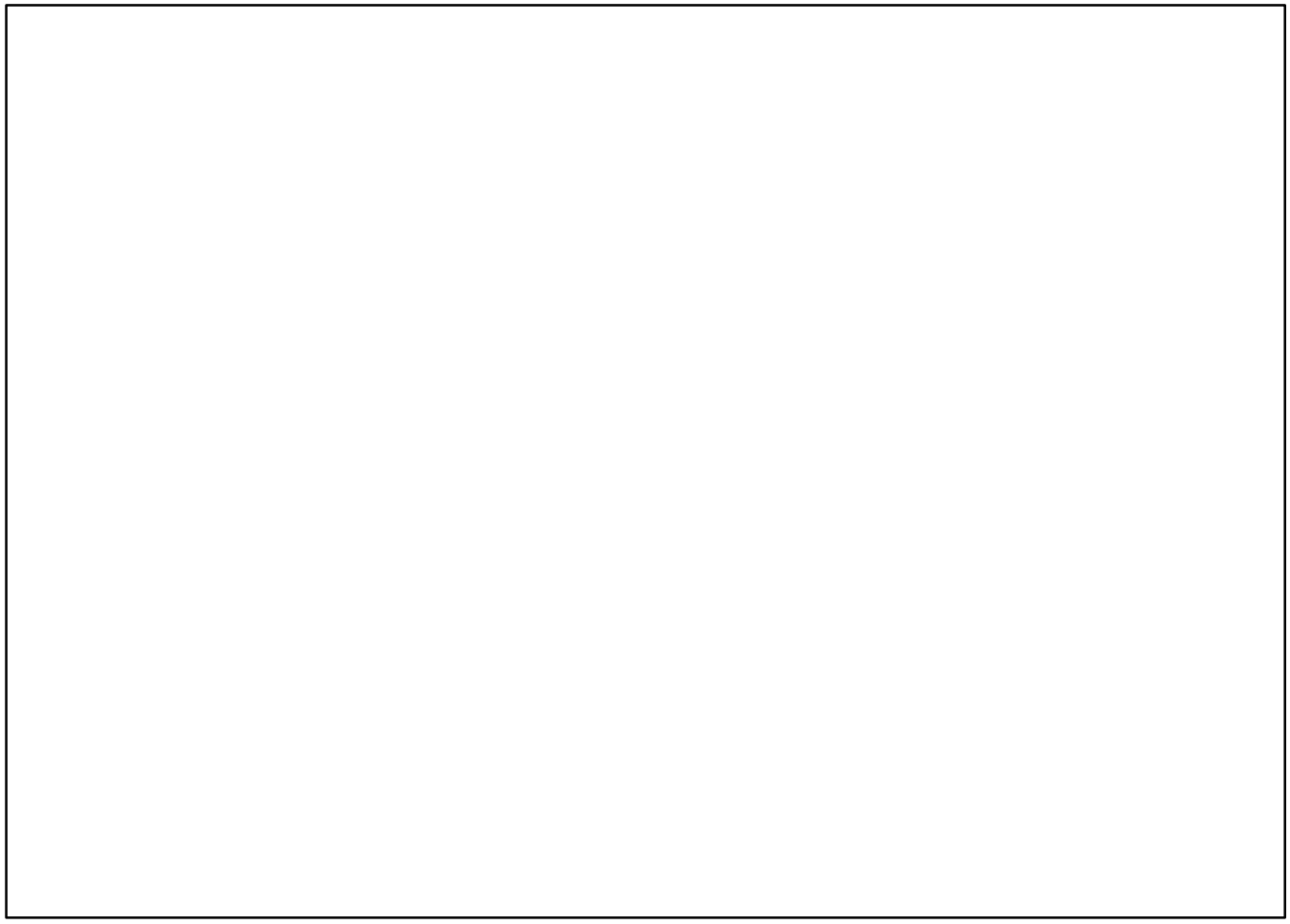
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Digital Input Rise Time	t_r	8, 9, 10, 11, 12	0.8 V → 2.0 V	—	—	50	ns
Digital Input Fall Time	t_f	8, 9, 10, 11, 12	2.0 V → 0.8 V	—	—	50	ns
Shift Clock Frequency	F_C	9, 10	—	64	—	3152	kHz
Shift Clock High Width	t_{WCH}	9, 10	V_{IH} = 2.0 V	140	—	—	ns
Shift Clock Low Width	t_{WCL}	9, 10	V_{IL} = 0.8 V	140	—	—	ns
Synchronization Frequency	F_S	11, 12	—	—	8	—	kHz
Synchronization High Width	t_{WSH}	11, 12	V_{IH} = 2.0 V	1/Fc Fc: MHz)	—	117	µA
XSYNC to XCLK Delay	t_{SX}	10, 12	—	100	—	—	ns
XCLK to XSYNC Delay	t_{XS}	10, 12	—	50	—	—	ns
RSYNC to RCLK Delay	t_{SR}	9, 11	—	100	—	—	ns
RCLK to RSYNC Delay	t_{RS}	9, 11	—	50	—	—	ns
RCLK to DIN Delay	t_{RD}	8, 9	—	50	—	—	ns
DIN to RCLK Delay	t_{DR}	8, 9	—	50	—	—	ns
XCLK or XSYNC to DOUT Delay[1]	t_{ZD}	10, 12, 15	—	30	—	200	ns
XCLK to DOUT Delay[2]	t_{XD}	10, 15	—	30	—	—	ns
XCLK to DOUT Disable Time	t_{DZ}	10, 15	High-Z	30	—	—	ns
DOUT Fall Time	t_{DF}	15	—	10	—	100	ns

Note: [1]Bit 1 DOUT load conditions: R_{DL} = 0.5 kΩ, C_{DL} = 144 pF, $+I_{OL}$ = 0.4 mA
[2]Bits 2 to 8 DOUT load conditions: R_{DL} = 0.5 kΩ, C_{DL} = 144 pF, $+I_{OL}$ = 0.4 mA

TIMING DIAGRAM



TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021A)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Conditions		Value Min.	Value Typ.	Value Max.	Unit
Signal to Distortion (A to A)	SDA	1020 Hz tone (C message)	+3 to –30 dBm0 –40 dBm0 –45 dBm0	35.0 30.0 25.0	—	—	dB dB dB
Signal to Distortion (A to D)	SDX	1020 Hz tone (C message)	+3 to –30 dBm0 –40 dBm0 –45 dBm0	36.0 31.0 26.0	—	—	dB dB dB
Signal to Distortion (D to A)	SDR	1020 Hz tone (C message)	+3 to –30 dBm0 –40 dBm0 –45 dBm0	36.0 31.0 26.0	—	—	dB dB dB
Gain Tracking (A to A)	GTX	1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	–0.4 –0.8 –2.0	—	0.4 0.8 2.0	dB dB dB
Gain Tracking (A to D)	GTX	1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	–0.2 –0.4 –0.8	—	0.2 0.4 0.8	dB dB dB
Gain Tracking (D to A)	GTR	1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	–0.2 –0.4 –0.8	—	0.2 0.4 0.8	dB dB dB
Frequency Response (A to A)	FRA	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0 dBm0, 820 Hz		24.0 –0.2 –0.2 –0.2 Note 1 64.0	—	 0.3 1.6	dB dB dB dB dB dB
Frequency Response (A to D)	FRX	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0 dBm0, 820 Hz		24.0 –0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8	dB dB dB dB dB dB
Frequency Response (D to A)	FRR	0 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0 dBm0, 820 Hz		–0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8	dB dB dB dB dB dB

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Notes: 1. $29\ (1 - \mathrm{Sin}\ \frac{\pi(4000 - f)}{1200})$

2. $29\ (1 - \mathrm{Sin}\ \frac{\pi(4000 - f)}{1200})$

TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021A) (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Idle Channel Noise (A to A)	ICNA	C message	—	–80	–72.0	dBm0c
Idle Channel Noise (A to D)	ICNX	C message	—	–83	–74.0	dBm0c
Idle Channel Noise (D to A)	ICNR	C message	—	–83	–78.0	dBm0c
Crosstalk (A to A)	CTA	1020 Hz, 0dBm0	—	—	–66	dB
Crosstalk (D to D)	CTD	1020 Hz, 0dBm0	—	—	–66	dB
Absolute Level	VABS	Overload Level 3.17 dBm0	—	2.500	—	V_{OP}
Analog Input Level	AIL	1020 Hz, 0dBm0 ±VS = ±5.0 V, T_A = 25 °C	—	1.227	—	V_{rms}
Analog Output Level	AOL	1020 Hz, 0dBm0 ±VS = ±5.0 V, T_A = 25 °C	1.206	1.227	2.248	V_{rms}
Gain Accuracy (A to A)	GAA	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A = 25 °C	–0.5 –0.3	0 0	+0.5 +0.3	dB dB
Gain Accuracy (A to D)	GAX	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A = 25 °C Variation with power supply Variation with temperature	–0.25 –0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/°C
Gain Accuracy (D to A)	GAR	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A = 25 °C Variation with power supply Variation with temperature	–0.25 –0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/°C
Propagation Delay (A to A)	PDA	FC ≥ 1544 kHz	—	—	540	μs

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TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021A) (Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Delay to Distortion (A to A)	DDA	500 to 600 Hz 600 to 1000 Hz 1000 to 2600 Hz 2600 to 2800 Hz 1020 Hz, 0dBm0 Relative to minimum delay	—	—	1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	PSRRA+	0 < f ≤ 50 kHz Idle Channel Noise (C Message) +VS +50 m V_{OP} AIN = AG	25	30	—	dB
PSRR (–VS) (A to A)	PSRRA–	0 < f ≤ 50 kHz Idle Channel Noise (C Message) –VS +50 m V_{OP} AIN = AG	35	40	—	dB
Intermoduration (A to A)	IMA1	AIN a. 0.47 kHz, – 10 dBm0 b. 0.32 kHz, – 10 dBm0 AOUT (a – b)	—	—	–38	dB
Intermoduration (A to A)	IMA2	AIN a. 1.02 kHz, –9 dBm0 b. 0.05 kHz, –23 dBm0 AOUT (2a – b)	—	—	–52	dBm0
Signal Frequency Noise (A to A)	SFNA	0 to 4 kHz 4 to 200 kHz AIN = AG	—	—	–70 –50	dBm0 dBm0
Discrimination (A to A)	DISA	AIN = 0dBm0 4.6 to 200 kHz	30	—	—	dB
In Band Spurious (A to A)	IBSA	2nd, 3rd Harmonic AIN = 0dBm0, 700 – 1100 Hz	43	—	—	dB

TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022A)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Conditions		Value Min.	Value Typ.	Value Max.	Unit
Signal to Distortion (A to A)	SDA	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to –30 dBm0	35.0	—	—	dB
			–40 dBm0	30.0			dB
			–45 dBm0	25.0			dB
		CCITT G.712 Method 1	–3 dBm0	28.0			dB
			–6 to –27 dBm0	35.5			dB
			–34 dBm0	33.5			dB
			–40 dBm0	28.5			dB
			–55 dBm0	13.5			dB
Signal to Distortion (A to D)	SDX	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to –30 dBm0	36.0	—	—	dB
			–40 dBm0	31.0			dB
			–45 dBm0	26.0			dB
		CCITT G.712 Method 1	–3 dBm0	30.0			dB
			–6 to –27 dBm0	36.0			dB
			–34 dBm0	34.0			dB
			–40 dBm0	29.5			dB
			–55 dBm0	14.5			dB
Signal to Distortion (D to A)	SDR	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to –30 dBm0	36.0	—	—	dB
			–40 dBm0	31.0			dB
			–45 dBm0	26.0			dB
		CCITT G.712 Method 1	–3 dBm0	30.0			dB
			–6 to –27 dBm0	36.0			dB
			–34 dBm0	34.0			dB
			–40 dBm0	29.5			dB
			–55 dBm0	14.5			dB

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TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022A) (Continued)

Parameter	Symbol	Conditions		Value Min.	Value Typ.	Value Max.	Unit
Gain Tracking (A to A)	GTA	CCITT G.712 Method 2 1020 Hz tone	+3 to –30 dBm0	–0.4	—	0.4	dB
			–40 to –50 dBm0	–0.8		0.8	dB
			–50 to –55 dBm0	–2.0		2.0	dB
		CCITT G.712 Method 1	–10 to –50 dBm0	–0.5	—	0.5	dB
			–55 to –60 dBm0	–1.0		1.0	dB
Gain Tracking (A to D)	GTX	CCITT G.712 Method 2 1020 Hz tone	+3 to –30 dBm0	–0.2	—	0.2	dB
			–40 to –50 dBm0	–0.4		0.4	dB
			–50 to –55 dBm0	–0.8		0.8	dB
		CCITT G.712 Method 1	–10 to –50 dBm0	–0.25	—	0.25	dB
			–50 to –55 dBm0	–0.4		0.4	dB
			–55 to –60 dBm0	–0.8		0.8	dB
Gain Tracking (D to A)	GTR	CCITT G.712 Method 2 1020 Hz tone	+3 to –40 dBm0	–0.2	—	0.2	dB
			–40 to –50 dBm0	–0.4		0.4	dB
			–50 to –55 dBm0	–0.8		0.8	dB
		CCITT G.712 Method 1	–10 to –50 dBm0	–0.25	—	0.25	dB
			–50 to –55 dBm0	–0.4		0.4	dB
			–55 to –60 dBm0	–0.8		0.8	dB
Frequency Response (A to A)	FRA	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0dBm0, 820 Hz		24.0 –0.2 –0.2 –0.2 Note 1 64.0	—	 0.3 1.6 	dB dB dB dB dB dB
Frequency Response (A to D)	FRX	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0dBm0, 820 Hz		24.0 –0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8 	dB dB dB dB dB dB
Frequency Response (D to A)	FRR	0 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0dBm0, 820 Hz		–0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8 	dB dB dB dB dB dB

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Notes: 1. $29\ (1 - \mathrm{Sin}\ \frac{\pi(4000 - f)}{1200})$

2. $14.5\ (1 - \mathrm{Sin}\ \frac{\pi(4000 - f)}{1200})$

TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022A) (Continued)

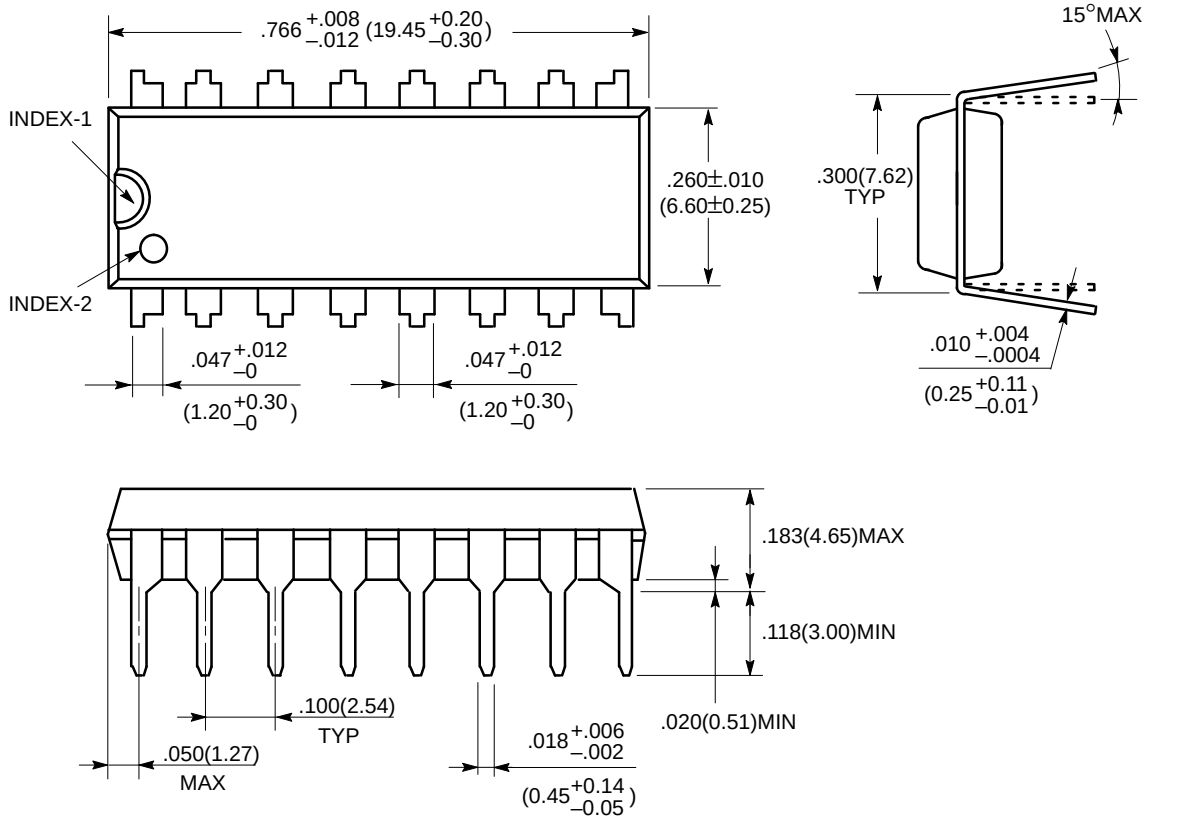
Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Idle Channel Noise (A to A)	ICNA	P Message	—	–80	–72.0	dBm0p
Idle Channel Noise (A to D)	ICNX	P Message	—	–83	–74.0	dBm0p
Idle Channel Noise (D to A)	ICNR	P Message	—	–83	–78.0	dBm0p
Crosstalk (A to A)	CTA	1020 Hz, 0dBm0	—	—	–66	dB
Crosstalk (D to D)	CTD	1020 Hz, 0dBm0	—	—	–66	dB
Absolute Level	VABS	Overload Level 3.14 dBm0	—	2.500	—	V_{OP}
Analog Input Level	AIL	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A 25 °C	—	1.231	—	V_{rms}
Analog Output Level	AOL	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A 25 °C	1.210	1.231	1.252	V_{rms}
Gain Accuracy (A to A)	GAA	1020 Hz, 0dBm0 Internal VREF	–0.5	0	+0.5	dB
		± VS = ± 5.0 V, T_A 25 °C	–0.3	0	+0.3	dB
Gain Accuracy (A to D)	GAX	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		± VS = ± 5.0 V, T_A 25 °C	–0.15	0	+0.15	dB
		Variation with Power Supply	—	±0.02	—	dB
		Variation with Temperature	—	±0.001	—	dB/ °C
Gain Accuracy (D to A)	GAR	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		± VS = ± 5.0 V, T_A 25 °C	–0.15	0	+0.15	dB
		Variation with Power Supply	—	±0.02	—	dB
		Variation with Temperature	—	±0.001	—	dB/ °C
Propagation Delay (A to A)	PDA	FC ≥ 1544 kHz	—	—	540	µs

Continued on next page

TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022A) (Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Delay to Distortion (A to A)	DDA	500 to 600 Hz 600 to 1000 Hz 1000 to 2600 Hz 2600 to 2800 Hz 1020 Hz, 0dBm0 Relative to Minimum Delay	— — — —	— — — —	1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	PSRRA+	0 < f ≤ 50 kHz Idle Channel Noise (P Message) +VS +50 m V_{OP} AIN = AG	25	30	—	dB
PSRR (–VS) (A to A)	PSRRA–	0 < f ≤ 50 kHz Idle Channel Noise (P Message) +VS +50 m V_{OP} AIN = AG	35	40	—	dB
Intermoduration (A to A)	IMA1	AIN a. 0.47 kHz, –10 dBm0 b. 0.32 kHz, –10 dBm0 AOUT (2a–b)	—	—	–38	dB
Intermoduration (A to A)	IMA2	AIN a. 1.02 kHz, –9 dBm0 b. 0.05 kHz, –23 dBm0 AOUT (a–b)	—	—	–52	dBm0
Single Frequency Noise (A to A)	SFNA	0 to 4 kHz 4 kHz to 200 kHz AIN = AG	— —	— —	–70 –50	dBm0 dBm0
Discrimination (A to A)	DISA	AIN = dBm0 4.6 kHz to 200 kHz	30	—	—	dB
In Band Spurious (A to A)	IBSA	2nd, 3rd Harmonic AIN = dBm0, 700 to 1100 kHz	43	—	—	dB

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



Dimensions in
inches (millimeters)

Circuit diagrams using Fujitsu products are included to illustrate typical semiconductor applications. Information sufficient for construction purposes may not be shown.

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