DS04–13202–3aE

FUJITSU

DATA SHEET

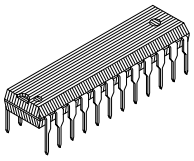
LINEAR IC CMOS

8 BIT 4-CHANNEL D/A CONVERTER MB86021

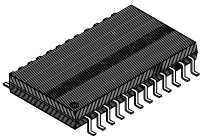
CMOS 8-BIT 4-CHANNEL D/A CONVERTER

The Fujitsu MB86021 is a 8-bit 4-channel Digital to Analog Converter which is fabricated with Fujitsu CMOS Technology. The data latch and output buffer circuitry are provided on each channel which can operate independently selected by 2bit data.

- Resolution : 8-Bits (4-channels)
- Conversion Rate : 200k sps
- Digital Input Voltage : TTL Level
- Power Supply Voltage : ±5V
- Low Power Dissipation : 38mW typ. at ±5V
- Each channel operates independently
- On-chip Data Initialization & Power Down Function
- Reference voltage mode selection: On-chip or External generation
- Easy to take interface with micro processor (Parallel Data Input)



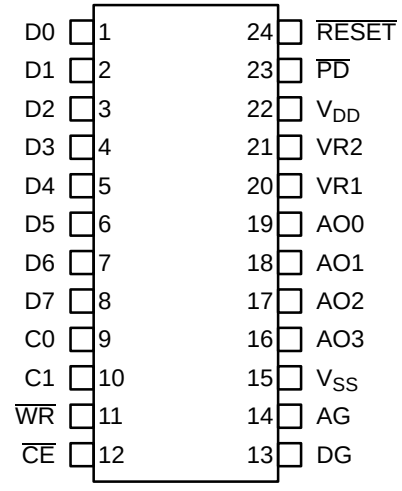
PLASTIC PACKAGE
DIP-24P-M03



PLASTIC PACKAGE
FPT-24P-M02

PIN ASSIGNMENT

(TOP VIEW)



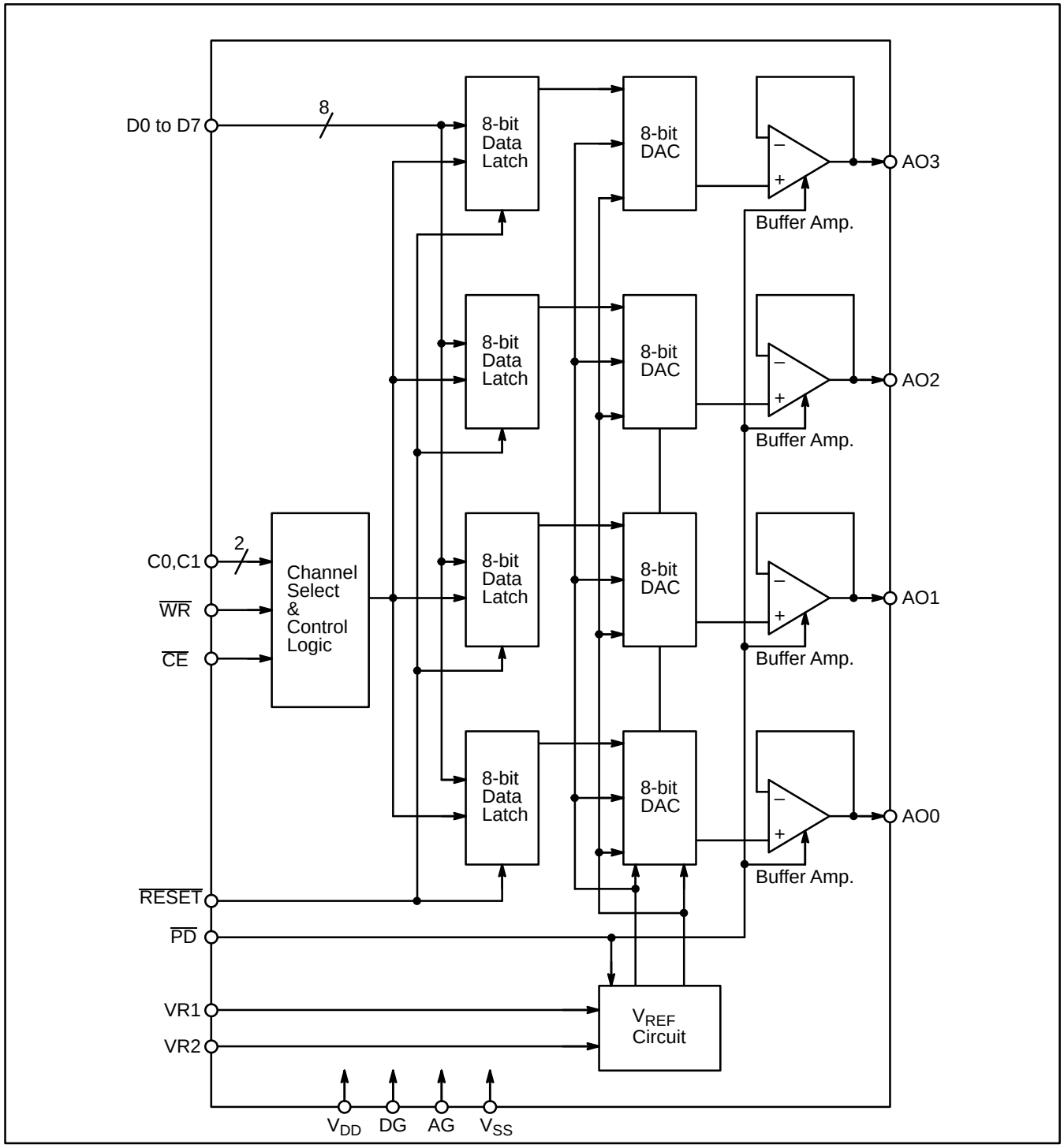
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Pin Name	Rating			Unit
			Min	Typ	Max	
Power supply voltage1	V_{DD}	V_{DD}	GND–0.3	–	7	V
Power supply voltage2	V_{SS}	V_{SS}	–7		GND+0.3	V
Digital input voltage		All digital input pins	GND–0.3		V_{DD}+0.3	
Analog input voltage	V_1, V_2	VR1,VR2	GND–0.3	–	V_{DD}+0.3	V
Analog output voltage	V_{AO}	AO0,AO1,AO2,AO3	V_{SS}–0.3	–	V_{DD}+0.3	V
Analog output voltage	I_{AO}	AO0,AO1,AO2,AO3	–10	–	10	mA
Storage temperature	Tstg		–40	–	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>System</th><th>Pin Number</th><th>Symbol</th><th>Descriptions</th></tr>
<tr><td rowspan="4">Power Supply</td><td>22</td><td>V_{DD}</td><td>Power supply voltage 5V</td></tr>
<tr><td>15</td><td>V_{SS}</td><td>Power supply voltage –5V</td></tr>
<tr><td>13</td><td>DG</td><td>GND for Digital System</td></tr>
<tr><td>14</td><td>AG</td><td>GND for Analog System</td></tr>
<tr><td rowspan="13">Digital Input</td><td>23</td><td>$\overline{PD}$</td><td>Power down control signal pin. The circuit is set power down when this pin goes to “L”. This pin is pulled up by high resistance. TTL interface.</td></tr>
<tr><td>24</td><td>$\overline{RESET}$</td><td>Reset input signal pin. The data at all channels is initialized when this pin goes to “L”. At this time, the D/A output is set at D(A)=128.
This pin is pulled up by high resistance. TTL interface.</td></tr>
<tr><td>12</td><td>$\overline{CE}$</td><td>Chip enable signal pin. The data can be written when this pin goes to “L”. This pin is pulled up by high resistance. TTL interface.</td></tr>
<tr><td>11</td><td>$\overline{WR}$</td><td>Data write pin. The data from D0 to D7 is written when the rising edge (L → H) of this pin. TTL interface.</td></tr>
<tr><td>9</td><td>C0</td><td rowspan="2">Channel selection signal pin. Channels are selected by following table. TTL interface.
<table><tr><th>C1</th><th>C0</th><th>Channel</th></tr><tr><td>L</td><td>L</td><td>0</td></tr><tr><td>L</td><td>H</td><td>1</td></tr><tr><td>H</td><td>L</td><td>2</td></tr><tr><td>H</td><td>H</td><td>3</td></tr></table></td></tr>
<tr><td>10</td><td>C1</td></tr>
<tr><td>1</td><td>D0</td><td rowspan="8">Data input signal pin. The digital data is read by the channel which is selected by C0 and C1 pins when the rising edge of $\overline{WR}$ (L → H), and analog output is shown correspond to that digital code. D0 is LSB and D7 is MSB. Code is set at 10000000 when reset. TTL interface.</td></tr>
<tr><td>2</td><td>D1</td></tr>
<tr><td>3</td><td>D2</td></tr>
<tr><td>4</td><td>D3</td></tr>
<tr><td>5</td><td>D4</td></tr>
<tr><td>6</td><td>D5</td></tr>
<tr><td>7</td><td>D6</td></tr>
<tr><td>8</td><td>D7</td></tr>
<tr><td rowspan="2">Analog Input</td><td>20</td><td>VR_1</td><td>Reference voltage (H level) input pin. $\frac{1}{2}V_{DD}$ is given by internal reference voltage circuitry to this pin when internal reference voltage mode. In this case, the capacitor between this pin and AG pin is required to limit noise generation. In case of external reference voltage mode, the reference voltage should be given from this pin.</td></tr>
<tr><td>21</td><td>VR_2</td><td>Middle point of reference voltage input pin. This pin should be AG level when internal reference voltage mode. In case of external reference voltage mode, the middle point of reference voltage should be given from this pin.</td></tr>
</table>

(Continued)

System	Pin Number	Symbol	Descriptions
Analog Output	16	AO3	Analog output pin of channel 3. This pin is set to high–impedance state at Power Down.
	17	AO2	Analog output pin of channel 2. This pin is set to high–impedance state at Power Down.
	18	AO1	Analog output pin of channel 1. This pin is set to high–impedance state at Power Down.
	19	AO0	Analog output pin of channel 0. This pin is set to high–impedance state at Power Down.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Power supply voltage1	V_{DD}	V_{DD}	4.75	5.0	5.25	V
Power supply voltage2	V_{SS}	V_{SS}	–5.25	–5.0	–4.75	V
Digital input voltage	V_{DI}	All digital input pins	0	–	V_{DD}	V
Analog input voltage	V_1	VR1	–3.0	2.5	3.0	V
	V_2	VR2	$\frac{V_1-3.0}{2}$	0	$\frac{V_1+3.0}{2}$	V
Analog output load resistance	R_{AL}	AO0, AO1, AO2, AO3	20	–	–	kΩ
Analog output load capacitance	C_{AL}		–	–	50	pF
Operating temperature	Ta		–20	–	70	°C

ELECTRICAL CHARACTERISTICS

(V_{DD}=4.75V to 5.25V, V_{SS}=–5.25V to –4.75V, Ta=–20°C to 70°C)

Parameter		Symbol	Pin Name	Conditions		Value			Unit
						Min	Typ	Max	
Power supply current 1		I_{DD1}	V_{DD}	No load	PD="H"	–	3.8	7.5	mA
		I_{DD2}			PD="L"	–	–	0.5	mA
Power supply current 2		I_{SS1}	V_{SS}		PD="H"	–7.5	–3.8	–	mA
		I_{SS2}			PD="L"	–0.5	–	–	mA
Digital Input	"L" Voltage	V_{IL}	All digital input pins			0	–	0.8	V
	"H" Voltage	V_{IH}				2.2	–	V_{DD}	V
	"L" Current	I_{IL}	D0 to D7, $\overline{WR}$	V_{DI}=GND		–10	–	10	µA
	"H" Current	I_{IH}		V_{DI}=V_{DD}		–10	–	10	µA
Pull upcurrent		I_{PLU}	$\overline{PD}$, $\overline{CE}$, $\overline{RESET}$	V_{DI}=GND		–100	–50	–25	µA
$\overline{WR}$ "H" Width		t_{WHWR}	$\overline{WR}$	Ref. to timing chart		200	–	–	ns
$\overline{WR}$ "L" Width		t_{WLWR}	$\overline{WR}$	Ref. to timing chart		200	–	–	ns
Digital input "L" width		t_{WLRP}	$\overline{RESET}$, $\overline{PD}$	Ref. to timing chart		500	–	–	ns
DATA set up time 1		t_{SD1}	D0 to D7, $\overline{WR}$	Ref. to timing chart		100	–	–	ns
DATA set up time 2		t_{SD2}	C0, C1, $\overline{WR}$	Ref. to timing chart		100	–	–	ns
$\overline{CE}$ set up time		t_{SCE}	$\overline{CE}$, $\overline{WR}$	Ref. to timing chart		0	–	–	ns
DATA Hold time 1		t_{HD1}	D0 to D7, $\overline{WR}$	Ref. to timing chart		50	–	–	ns
DATA Hold time 2		t_{HD2}	C0, C1, $\overline{WR}$	Ref. to timing chart		50	–	–	ns
$\overline{CE}$ Hold time		t_{HCE}	$\overline{CE}$, $\overline{WR}$	Ref. to timing chart		0	–	–	ns

(Continued) **(V_{DD}=4.75V to 5.25V, V_{SS}=–5.25V to –4.75V, Ta=–20°C to 70°C)**

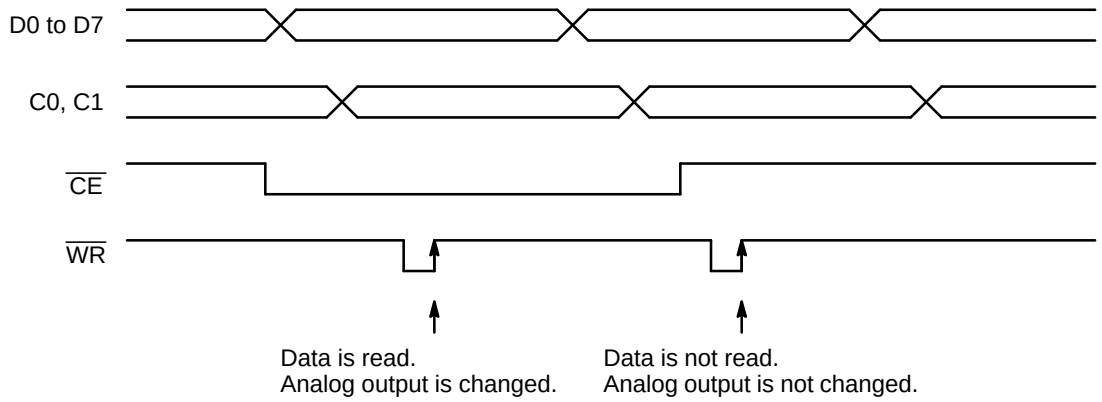
Parameter	Symbol	Pin Name	Conditions		Value			Unit
					Min	Typ	Max	
Rising time 1	t_{r1}	$\overline{WR}$	Ref. to timing chart		0	–	50	ns
Falling time 1	t_{f1}	$\overline{WR}$	Ref. to timing chart		0	–	50	ns
Rising time 2	t_{r2}	D0 to D7, C0, C1, $\overline{CE}$, $\overline{RESET}$, $\overline{PD}$	Ref. to timing chart		0	–	50	ns
Falling time 2	t_{f2}	D0 to D7, C0, C1, $\overline{CE}$, $\overline{RESET}$, $\overline{PD}$	Ref. to timing chart		0	–	50	ns
Resolution	Res	AO0, AO1, AO2, AO3			–	8	–	bits
Analog output Min. voltage	V_{AOL1}		Input Code D(A)=0	No external VR input VR1=open VR2=0V (AG)	(Typ.) –0.1	$-\frac{1}{2} \times V_{DD}$	(Typ.) +0.1	V
	V_{AOL2}			External VR input VR1=V_1 VR2=V_2	(Typ.) –0.1	$2 \times V_2 - V_1$	(Typ.) +0.1	V
Analog output Max. voltage	V_{AOH1}		Input Code D(A)=255	No external VR input VR1=open VR2=0V (AG)	(Typ.) –0.1	$\frac{127}{256} \times V_{DD}$	(Typ.) +0.1	V
	V_{AOH2}			External VR input VR1=V_1 VR2=V_2	(Typ.) –0.1	$V_1 - \frac{V_1 - V_2}{128}$	(Typ.) +0.1	V
Analog input resistance	R_I	VR_1			30	50	200	kΩ
Analog input leak current	I_{AIH}	VR_2	$V_{IH}=V_{DD}$		–10	–	10	µA
	I_{AIL}		$V_{IL}=V_{SS}$		–10	–	10	µA
Linearity error	LE	AO0, AO1, AO2, AO3	No external VR input VR1=open VR2=0V (AG)		–1.5	–	1.5	LSB
Differential linearity error	D_{LE}				–1	–	1	LSB
Setting time	t_S		Full scale change (Ref. to timing chart)		–	–	5	µs

FUNCTION DESCRIPTION

TRUTH TABLE

$\overline{PD}$	$\overline{RESET}$	$\overline{CE}$	$\overline{WR}$	C0, C1	D0 to D7	Function
0	x	x	x	–	–	Power down
1	0	x	x	–	–	Initialization
1	1	1	x	–	No data input	No analog output change
1	1	0	⊓	Channel selection	Data input	Analog output change

Fig. 1 – DATA SET TIMING DIAGRAM



SETTING OF ANALOG OUTPUT VOLTAGE

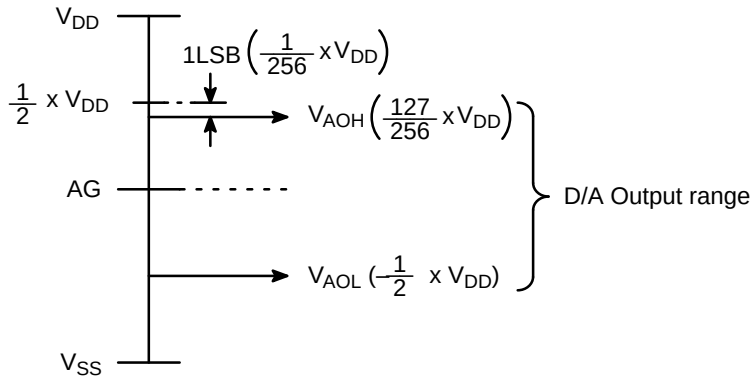
Data									Analog Output Voltage		
D(A)	D7	D6	D5	D4	D3	D2	D1	D0	VR1=Open VR2=0V (AG) (No external VR input)	VR1=V_1 VR2=0V (AG) (External VR1 input)	VR1=V_1 VR2=V_2 (External VR input)
255	1	1	1	1	1	1	1	1	$\frac{127}{256} \times V_{DD}$	$\frac{127}{128} \times V_1$	$\frac{V_1-V_2}{128} \times 127 + V_2$
254	1	1	1	1	1	1	1	0	$\frac{126}{256} \times V_{DD}$	$\frac{126}{128} \times V_1$	$\frac{V_1-V_2}{128} \times 126 + V_2$
253	1	1	1	1	1	1	0	1	$\frac{125}{256} \times V_{DD}$	$\frac{125}{128} \times V_1$	$\frac{V_1-V_2}{128} \times 125 + V_2$
⋮					⋮				$\frac{1}{256} \times V_{DD} \times (D(A)-128)$	$\frac{V_1}{128} \times (D(A)-128)$	$\frac{V_1-V_2}{128} \times (D(A)-128) + V_2$
129	1	0	0	0	0	0	0	1	$\frac{1}{256} \times V_{DD}$	$\frac{1}{128} \times V_1$	$\frac{V_1-V_2}{128} + V_2$
128	1	0	0	0	0	0	0	0	0	0	V_2
127	0	1	1	1	1	1	1	1	$-\frac{1}{256} \times V_{DD}$	$-\frac{1}{128} \times V_1$	$\frac{V_1-V_2}{128} \times (-1) + V_2$
126	0	1	1	1	1	1	1	0	$-\frac{2}{256} \times V_{DD}$	$-\frac{2}{128} \times V_1$	$\frac{V_1-V_2}{128} \times (-2) + V_2$
⋮					⋮				⋮	⋮	⋮
2	0	0	0	0	0	0	1	0	$-\frac{126}{256} \times V_{DD}$	$-\frac{126}{128} \times V_1$	$\frac{V_1-V_2}{128} \times (-126) + V_2$
1	0	0	0	0	0	0	0	1	$-\frac{127}{256} \times V_{DD}$	$-\frac{127}{128} \times V_1$	$\frac{V_1-V_2}{128} \times (-127) + V_2$
0	0	0	0	0	0	0	0	0	$-\frac{1}{2} \times V_{DD}$	$-V_1$	$-(V_1-V_2) + V_2$
1LSB									$\frac{1}{256} \times V_{DD}$	$\frac{1}{128} \times V_1$	$\frac{V_1-V_2}{128}$

* Code is set at ”10000000” when reset mode.

ANALOG OUTPUT VOLTAGE RANGE

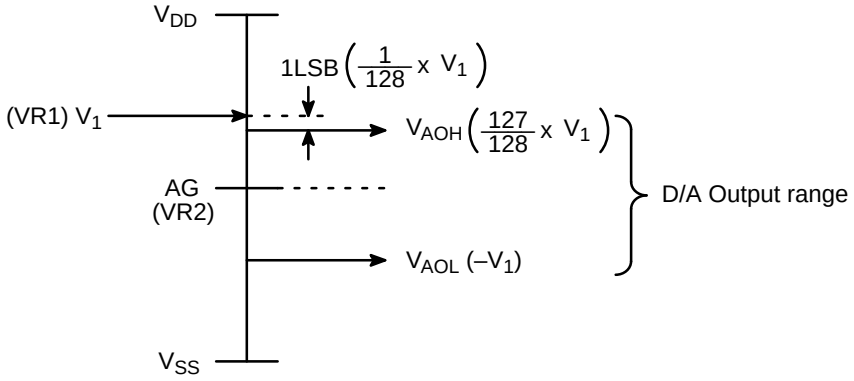
(VR1=OPEN, VR2=0V (AG))

Fig. 2 – ON-CHIP REFERENCE VOLTAGE MODE



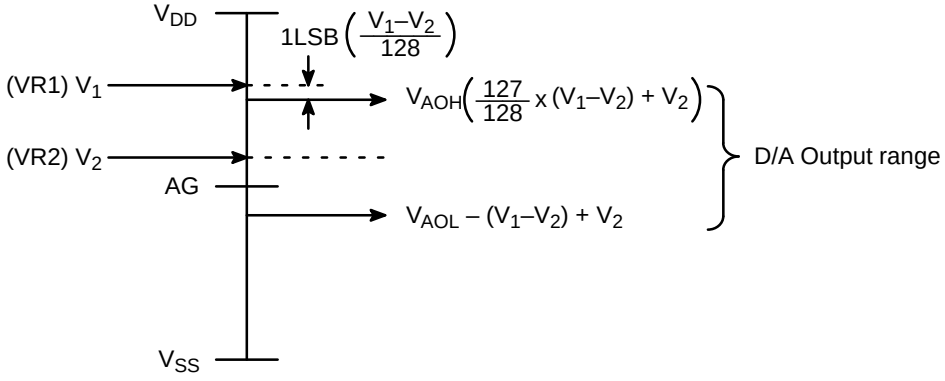
(VR1=V_1, VR2=0V (AG))

Fig. 3 – EXTERNAL REFERENCE VOLTAGE MODE



(VR1=V_1, VR2=V_2)

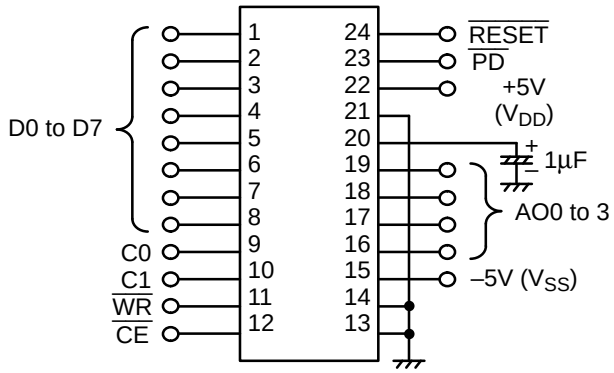
Fig. 4 – EXTERNAL REFERENCE VOLTAGE MODE



TYPICAL APPLICATION CIRCUIT FOR EACH MODE

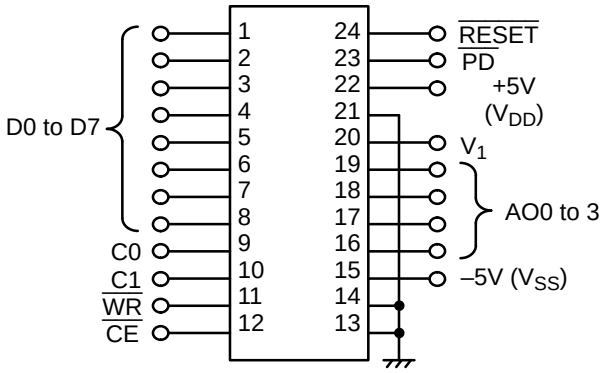
(VR1=OPEN, VR2=0V (AG))

Fig. 5 – ON-CHIP REFERENCE VOLTAGE MODE



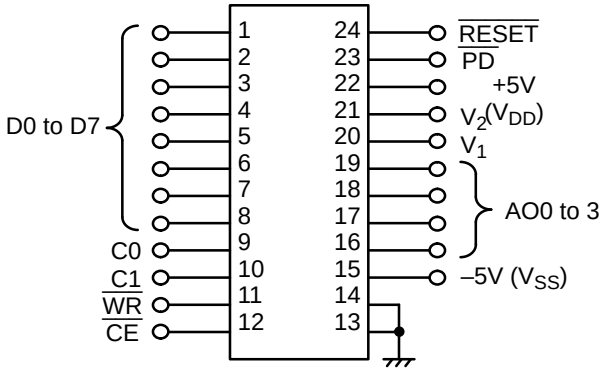
(VR1=V_1, VR2=0V (AG))

Fig. 6 – EXTERNAL REFERENCE VOLTAGE MODE

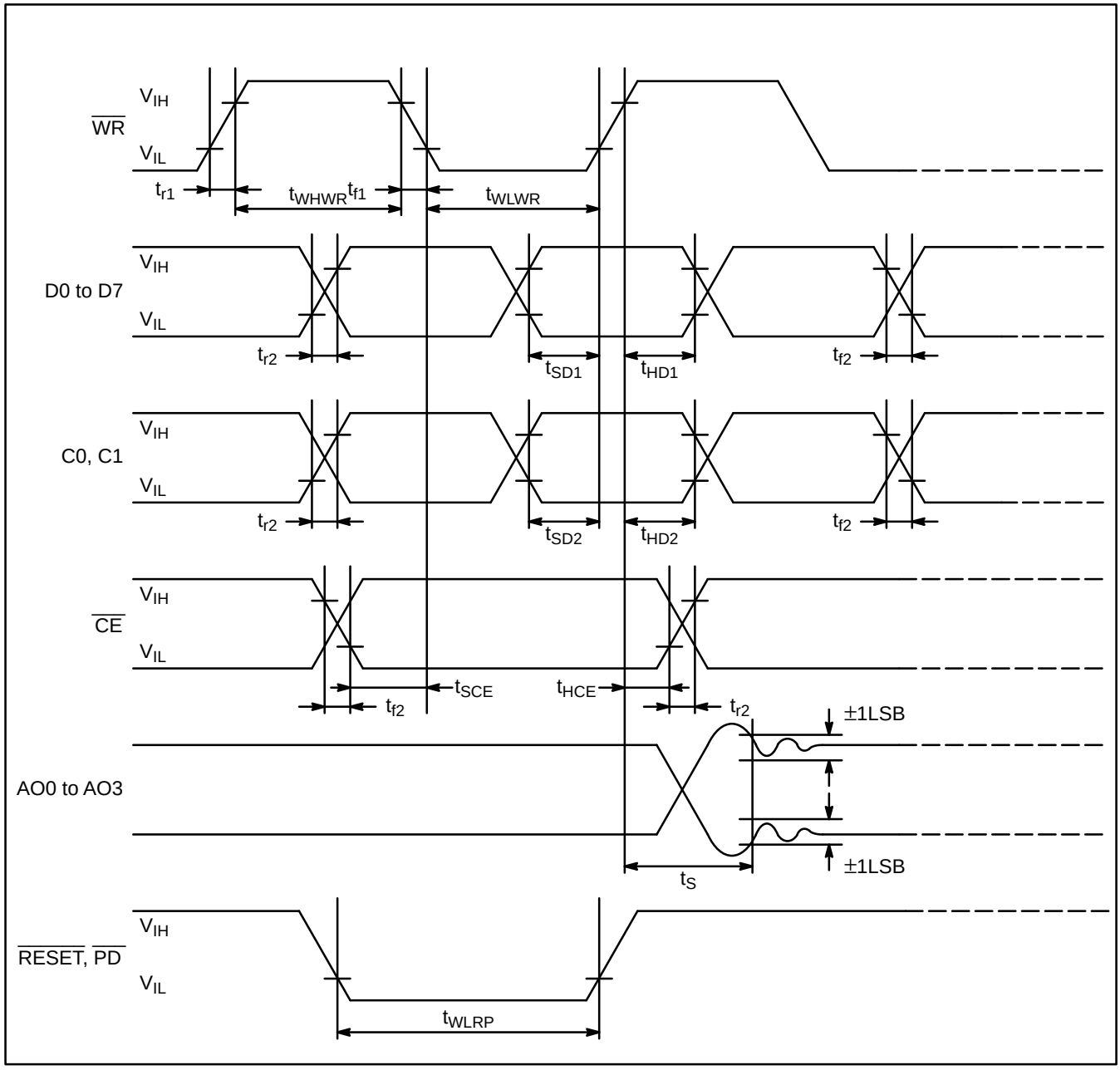


(VR1=V_1, VR2=V_2)

Fig. 7 – ON-CHIP REFERENCE VOLTAGE MODE

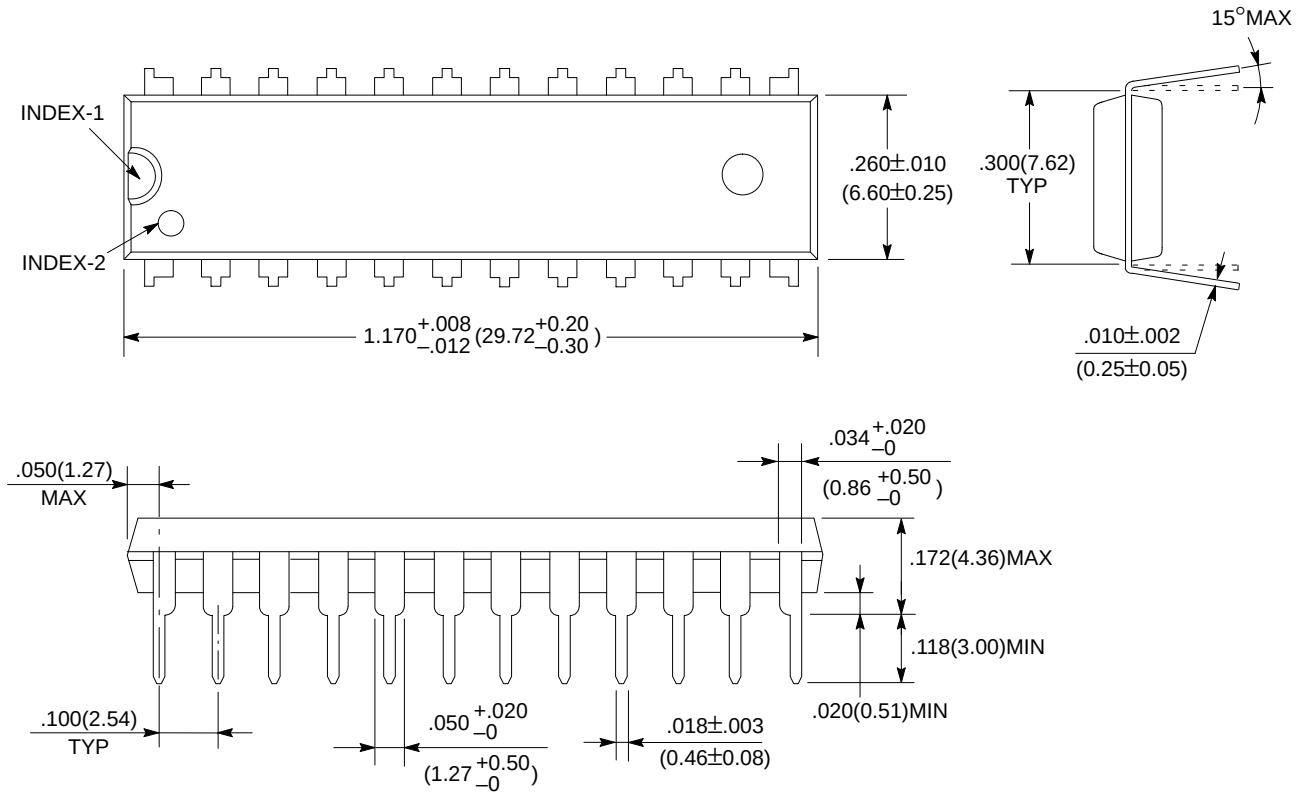


TIMING DIAGRAM



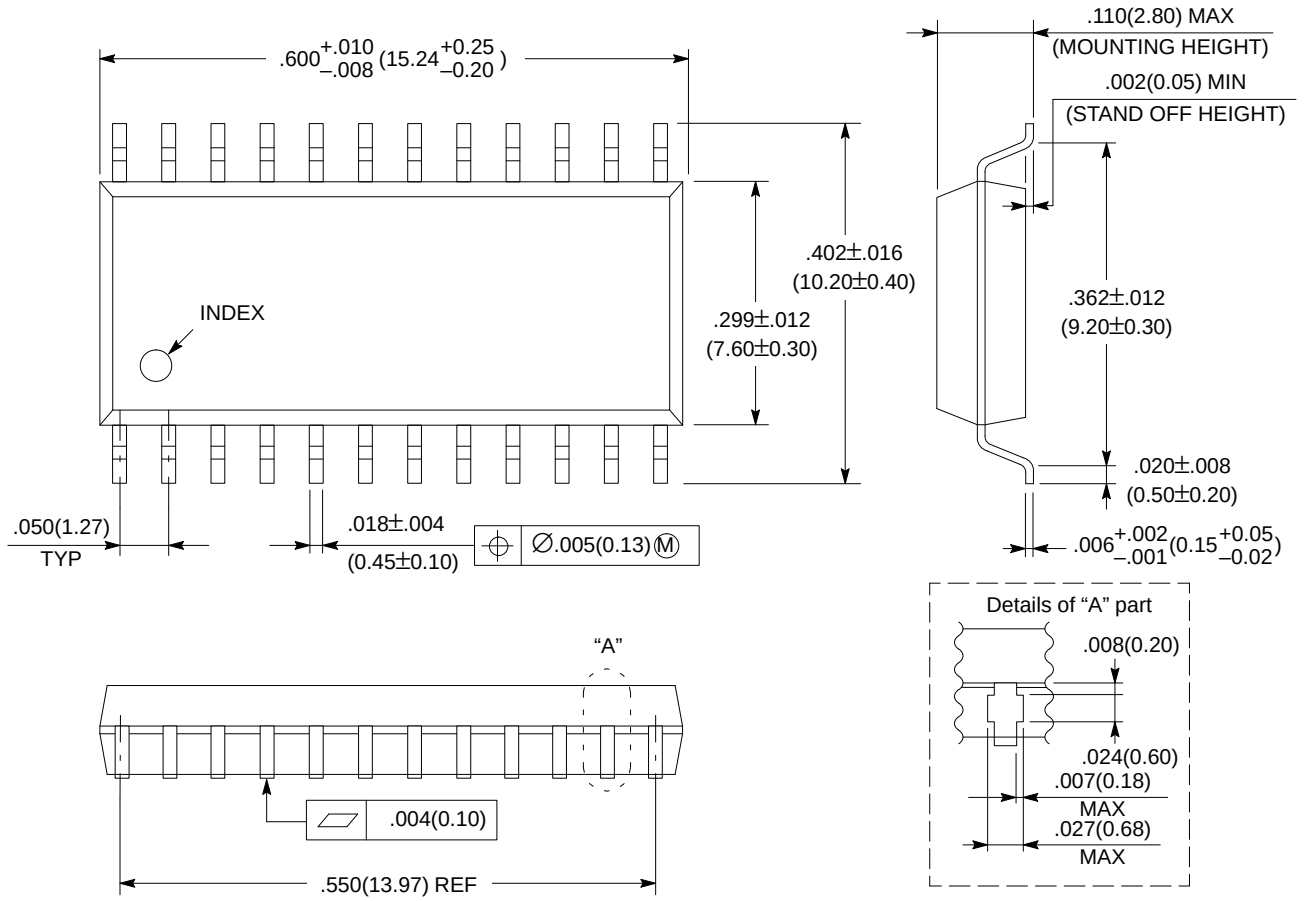
PACKAGE DIMENSIONS

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)



Dimensions in
inches (millimeters)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete Information sufficient for construction purposes is not necessarily given.

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