DS04-21324-3L

FUJITSU

DATA SHEET

ASSP for DTS
Bi-CMOS
1.1 GHz PLL Frequency Synthesizer
MB15A01

■ DESCRIPTION

The MB15A01 is a serial-input PLL (phase locked loop) frequency synthesizer LSI supporting a pulse swallow system.

The LSI consists of: a 1.1 GHz band, dual-modulus prescaler allowing either of 64/65 and 128/129 frequency divisions to be selected, a control signal generator circuit, a 19-bit shift register, a 15-bit latch, a reference divider (binary 14-bit reference counter), a 1-bit switch counter, a phase comparator with phase conversion functions, a charge pump, a crystal oscillator, an 18-bit latch, and programmable dividers (binary 7-bit swallow counter and binary 11-bit programmable counter).

The LSI is housed in a 16-pin or 20-pin SSOP package, contributing to space saving of the system incorporating it.

In addition, the MB15A01 operates at a low supply voltage of 3.0 V (typical), achieving low current consumption (typically I_{CC} = 6.5 mA)

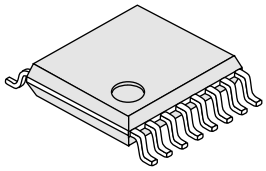
■ FEATURES

- Operation at high speed: fin = 1.1 GHz (Vin = –10 dBm)
- Pulse swallow function: Internal dual-modulus prescaler allowing either of 64/65 and 128/129 frequency divisions to be selected
- Low current consumption: I_{CC} = 6.5 mA (typical)

(Continued)

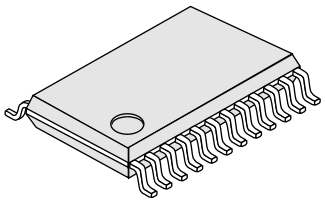
■ PACKAGES

16-pin Plastic SSOP



(FPT-16P-M05)

20-pin Plastic SSOP

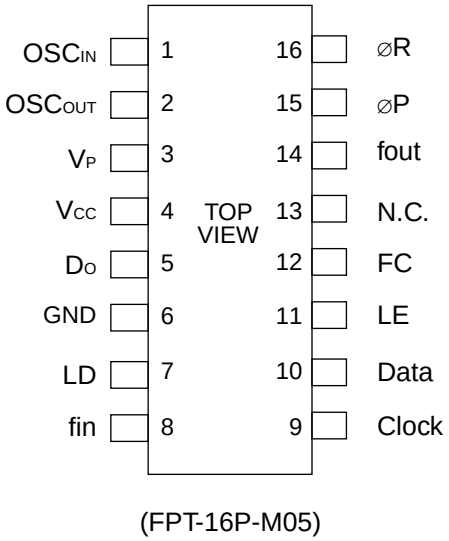


(FPT-20P-M03)

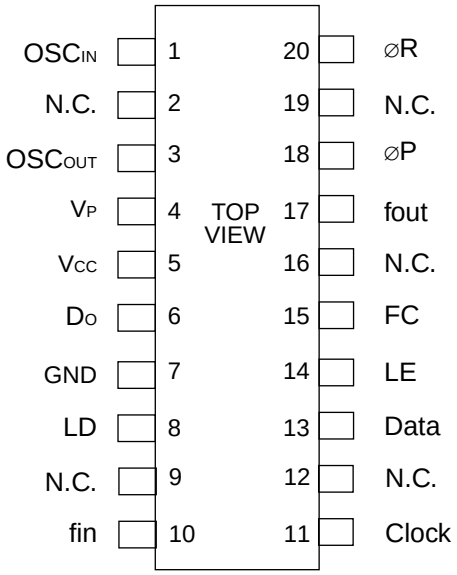
(Continued)

- Serial-input 18-bit programmable divider
  Divide ratio of binary 7-bit swallow counter (0 to 127)
  Binary 11-bit programmable counter (16 to 2,047)
- Serial-input 15-bit reference divider
  Divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
  1-bit switch counter (for setting the prescaler divide ratio)
- Serial data configuration compatible with conventional models such as MB1511
- Two different phase comparator outputs
  Internal charge pump output (bipolar type)
  Output for external charge pump
- Wide range of operating temperature: Ta = –40 to +85°C

■ PIN ASSIGNMENTS



(FPT-16P-M05)

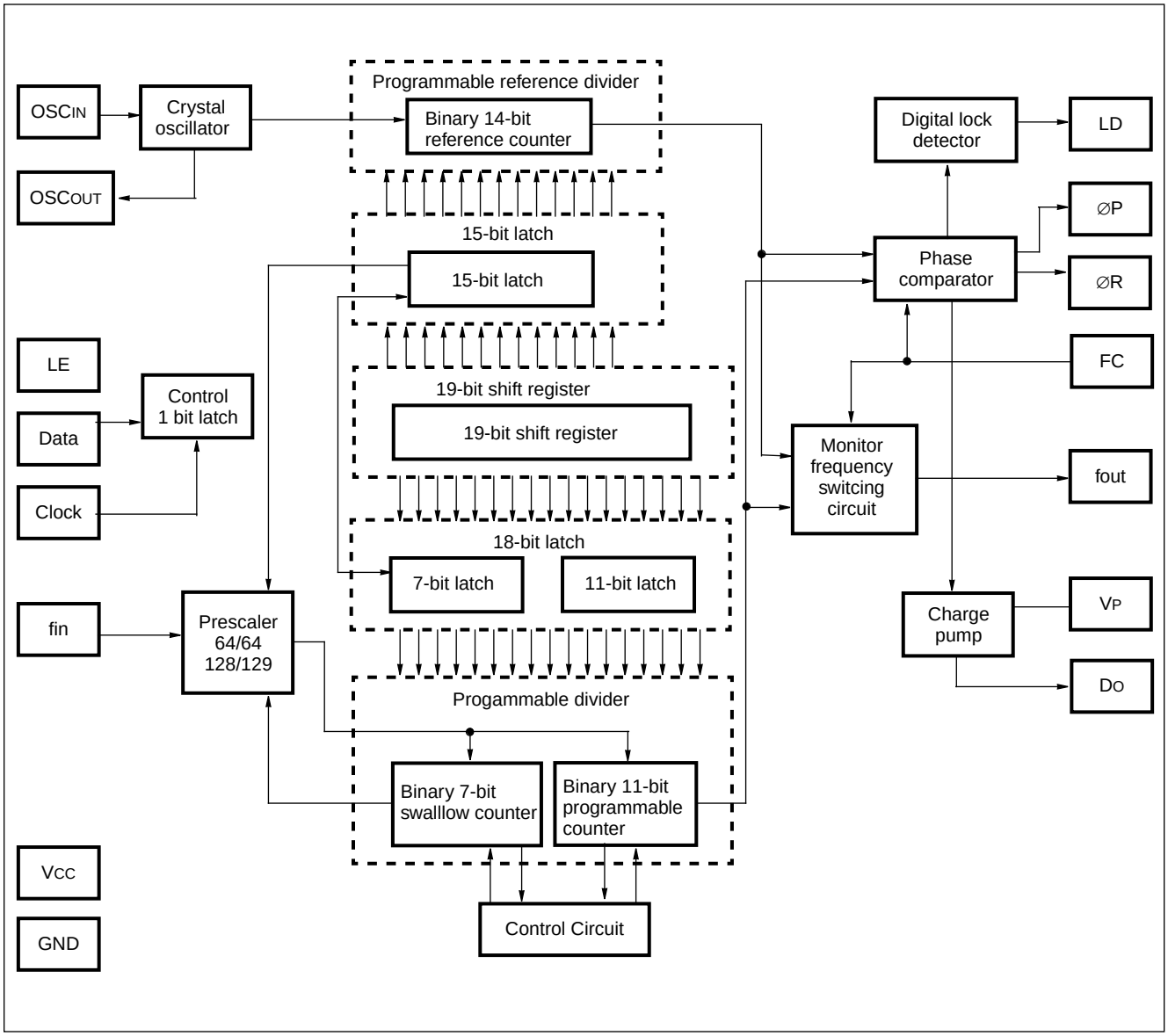


(FPT-20P-M03)

■ PIN DESCRIPTION

Pin No.		Pin name	I/O	Function
SSOP-16	SSOP-20			
1	1	OSC_{IN}	I	Crystal oscillator connection pin serving as a reference divider input pin (Oscillator circuit input pin)
2	3	OSC_{OUT}	O	Crystal oscillator connection pin (Oscillator circuit output pin)
3	4	V_P	—	Power supply pin for charge pump output Connect this pin to V_{CC} when the internal charge pump is not used.
4	5	V_{CC}	—	Power supply pin
5	6	D_O	O	Internal charge pump output pin
6	7	GND	—	GND pin
7	8	LD	O	Lock detector output pin When locked: LD = “H”, When unlocked: LD = “L”
8	10	fin	I	Prescaler input pin The pin must be AC-coupled for input.
9	11	Clock	I	Clock input pin for 19-bit and 16-bit shift registers The shift resistors reads data at the rise of the clock pulse.
10	13	Data	I	Binary-coded serial data input pin The last bit in the data is a control bit. Control bit = “H”: Sends data to the 15-bit latch. “L”: Sends data to the 18-bit latch.
11	14	LE	I	Load enable signal input pin (with pull-up resistor) When LE = “H”, the pin sends the contents of the shift register to the latch according to the control bit.
12	15	FC	I	Phase comparator phase switching pin (with pull-up resistor) When FC = “L”, the pin inverts characteristics of the phase comparator. It also switches the fout pin (test pin) output between fr and fp.
13	2, 9, 12, 16, 19	N.C.	—	No connection.
14	17	fout	O	Phase comparator input monitor pin The pin outputs the reference divider output (fr) or programmable divider output (fp) signal depending on the FC pin input level. It is an N channel open-drain output.
15	18	øP	O	Phase comparator output pin for external charge pump This pin is an N channel open-drain output.
16	20	øR	O	Phase comparator output pin for external charge pump This pin is a CMOS output.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	–0.5	+5.0	V	
	V_P	V_{CC}	+8.0	V	
Output voltage	V_O	–0.5	V_{CC} + 0.5	V	
Open-drain voltage	V_{OOP}	–0.5	+6.0	V	øP pin
Output current	I_O	–10	+10	mA	
Storage temperature	Tstg	–55	+125	°C	

Precaution: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	2.7	3.0	3.5	V
	V_P	V_{CC}	—	6.0	V
Input voltage	V_I	GND	—	V_{CC}	V
Operating temperature	Ta	–40	—	+85	°C

Precautions: Although the MB15A01 contains an antistatic element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device:

- When storing or carrying the device, put it in a conductive case.
- This is static-sensitive device; take proper anti-ESD precautins. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Before fitting the device into or removing it from the socket, turn the power supply off.
- Protect leads with conductive sheet when handling or transporting PC boads with devices.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 3.5 V, Ta = –40°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CC}	V_{CC} = 3 V, assuming fin = 1.1 GHz and OSC_{IN} = 12 MHz, in locking	—	6.5	—	mA
Operating frequency	fin	fin	Must be AC-coupled. The minimum operating frequency assumes coupling at 1000 pF.	10	—	1100	MHz
	OSC_{IN}	f_{OSC}	—	—	12	23	MHz
Input sensitivity	fin	V_{fin}	50 Ω system (Refer to the test circuit example)	–10	—	6	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	—	V_{P-P}
"H" level input voltage	Clock Data LE	V_{IH}	—	$V_{CC} \times 0.7$	—	—	V
"L" level input voltage		V_{IL}	—	—	—	$V_{CC} \times 0.3$	V
"H" level input current	Clock Data	I_{IH}	—	—	—	1.0	µA
"L" level input current		I_{IL}	—	—	—	–1.0	µA
Input current	OSC_{IN}	I_{OSC}	—	—	±50	—	µA
	LE, FC	I_{LE}	—	—	–60	—	µA
"H" level output voltage	øR, LD	V_{OH}	V_{CC} = 3 V, I_{OH} = –1.0 mA	2.1	—	—	V
"L" level output voltage	øP/R, LD	V_{OL}	V_{CC} = 3 V, I_{OL} = 1.0 mA	—	—	0.4	V
High-impedance cutoff current	D_O øP	I_{OFF}	V_P = V_{CC} to 6.0 V V_{OOP} = GND to 6.0 V	—	—	1.1	µA
Output current	øR, LD	I_{OH}	V_{CC} = 3 V	–1.0	—	—	mA
	øP/R, LD	I_{OL}	V_{CC} = 3 V	—	—	1.0	mA

■ FUNCTIONAL DESCRIPTIONS

1. Pulse Swallow Function

For the pulse swallow function, use the following equations to select their respective setting values:

$$f_{VCO} = ((P \times N) + A) \times f_{OSC} \div R$$

f_{VCO}	:	Output frequency of externally connected VCO
P	:	Prescaler divide ratio (64 or 128)
N	:	Divide ratio of 11-bit programmable counter (16 to 2047)
A	:	Divide ratio of 7-bit swallow counter (0 to 127, A < N)
f_{OSC}	:	Reference oscillation frequency
R	:	Divide ratio of 14-bit programmable reference counter (6 to 16383)

2. Serial Data Input Method

Serial data is processed using three input pins (Data, Clock, and LE pins) to control the 15-bit reference divider and the 18-bit programmable divider separately.

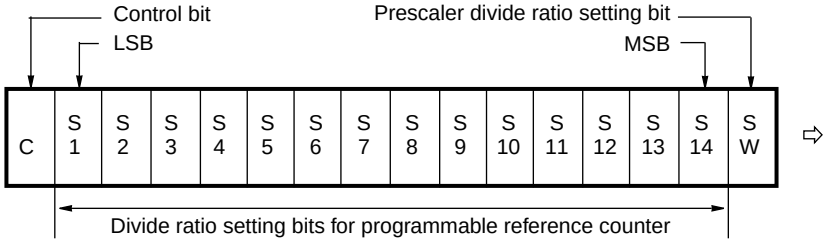
Input binary-coded serial data to the Data pin.

Serial data is input to the internal shift register in sequence at the rise of each clock pulse. When the load enable signal input pin has a high level (or open), the input data is transferred to the latch depending on the control bit.

Control bit = “H”: Transfer to the 15-bit latch
Control bit = “L”: Transfer to the 18-bit latch

(1) Divide Ratio of Reference Divider

The reference divider consisits of a 16-bit shift register, a 15-bit latch, and a 14-bit reference counter. Serial data is made up of the following 16 bits:



- 14-bit programmable reference divide ratio

Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

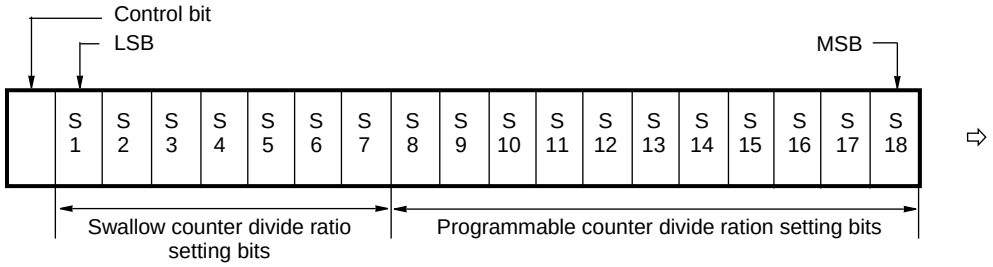
Note: The divide ratio must not be less than 6. (Set value: 6 to 16383)

SW: Prescaler division bit
SW = “H”: 64/65 division
SW = “L”: 128/129 division
S1 to S14: Divide ration setting bits (Divide ratio of 6 to 16383)
C: Control bit (Set it to “H”.)

Note: Start data input with MSB first.

(2) Divide Ratio of Programmable Divider

The programmable divider consists of a 19-bit shift register, an 18-bit latch, 7-bit swallow counter, and an 11-bit programmable counter. Serial data is made up of the following 19 bits:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•

(Set value: 0 to 127)

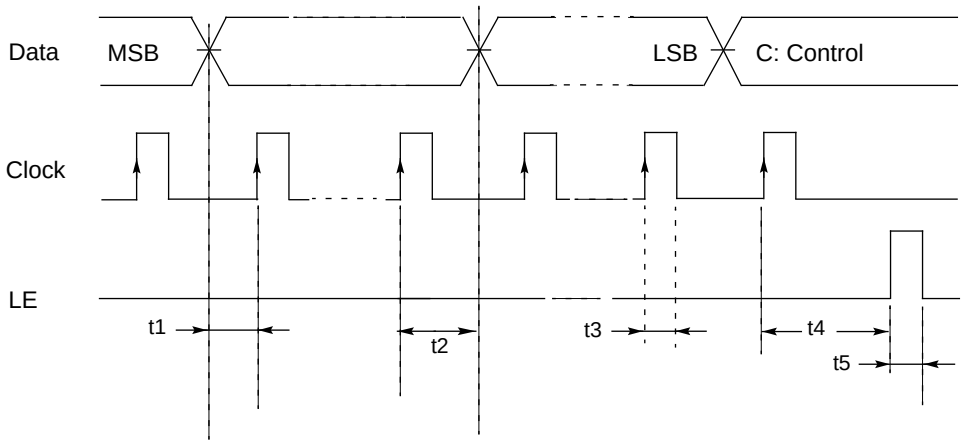
Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	1	0	0	0	0	0
17	0	0	0	0	0	1	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•

Note: The divide ratio must not be less than 16. (Set value: 16 to 2047)

S1 to S7: Swallow counter divide ratio setting bits (Divide ration of 0 to 127)
S8 to S18: Programmable counter divide ration setting bits (Divide ration of 16 to 2047)
C: Control bit (Set it to “L”)

Note: Start data input with MSB first.

(3) Serial Data Input Timing



t1, t4>100 ns, t2>1000 nw, t3>300 ns, t5>800 ns

Note: Serial data is fetched a the rise of each clock pulse.

3. Relation between FC Pin Inputs and Phase Characteristics

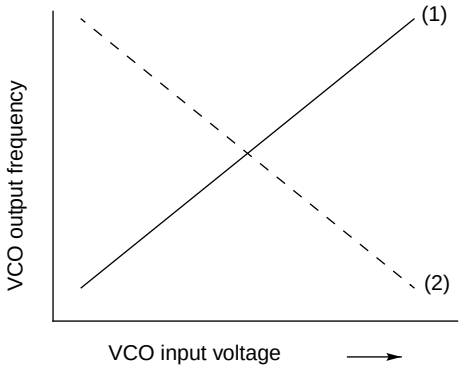
The FC pin is the phase switching pin for the phase comparator. Controlling the FC pin inverts the characteristics of the internal charge pump output (D_O) and phase comparator outputs (øR, øP). In addition, the phase comparator input monitor pin (fout) is also controlled via the FC pin. The following table lists relation between FC pin inputs and D_O, øR, øP, and fout:

	FC: "H" (or open)				FC: "L"			
	D_O	øR	øP	fout	D_O	øR	øP	fout
fr > fp	H	L	L	fr	L	H	Z	fp
fr < fp	L	H	Z		H	L	L	
fr = fp	Z	L	Z		Z	L	Z	

Z: High impedance

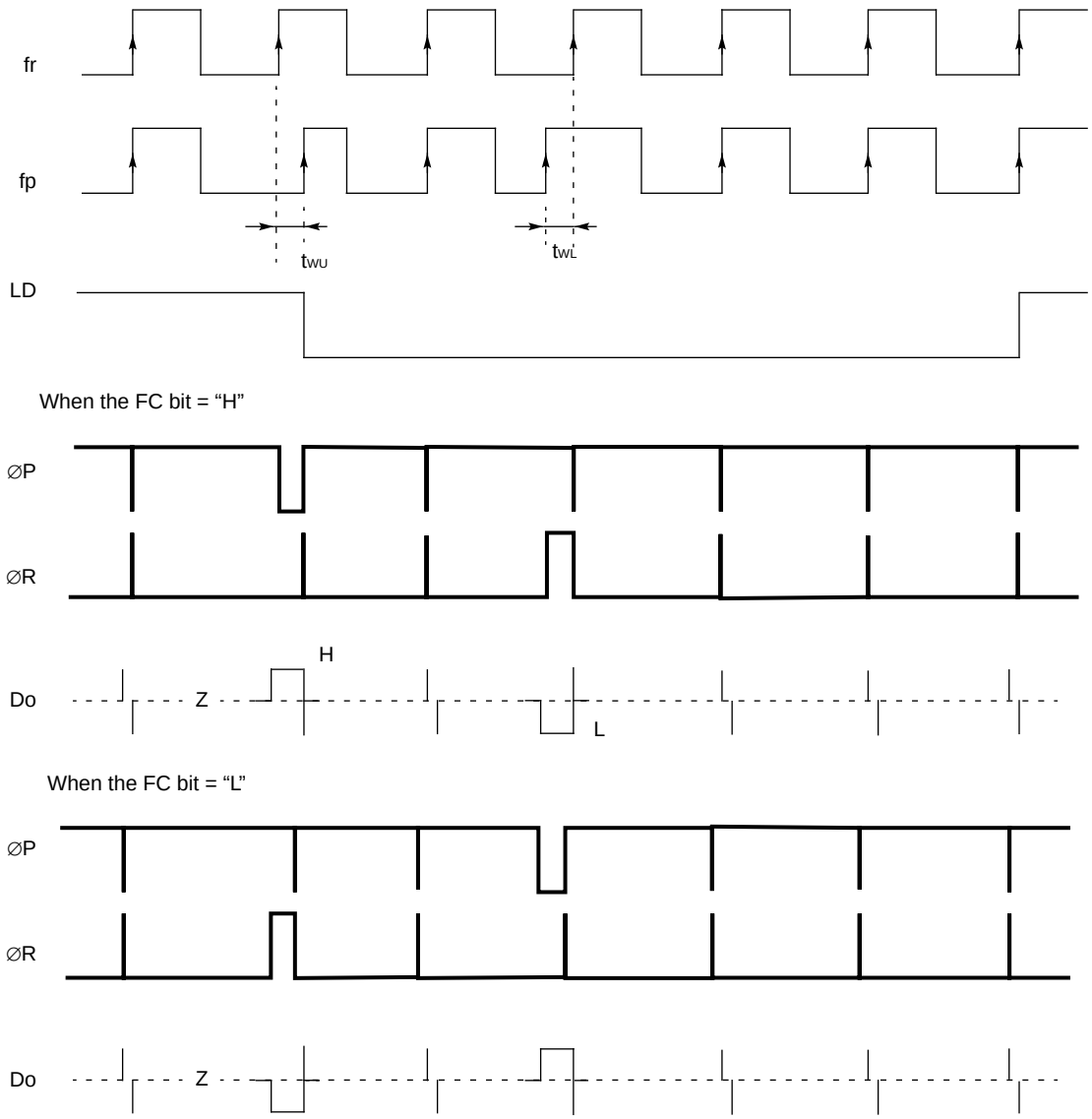
When disigning a synthesizer, control the FC pin depending on the VCO polarity.

- When the VCO polarity is (1)
  FC: "H" or open
- When the VCO polarity is (2)
  FC: "L"



Note: When using an active lowpass filter, pay attention to its polarity

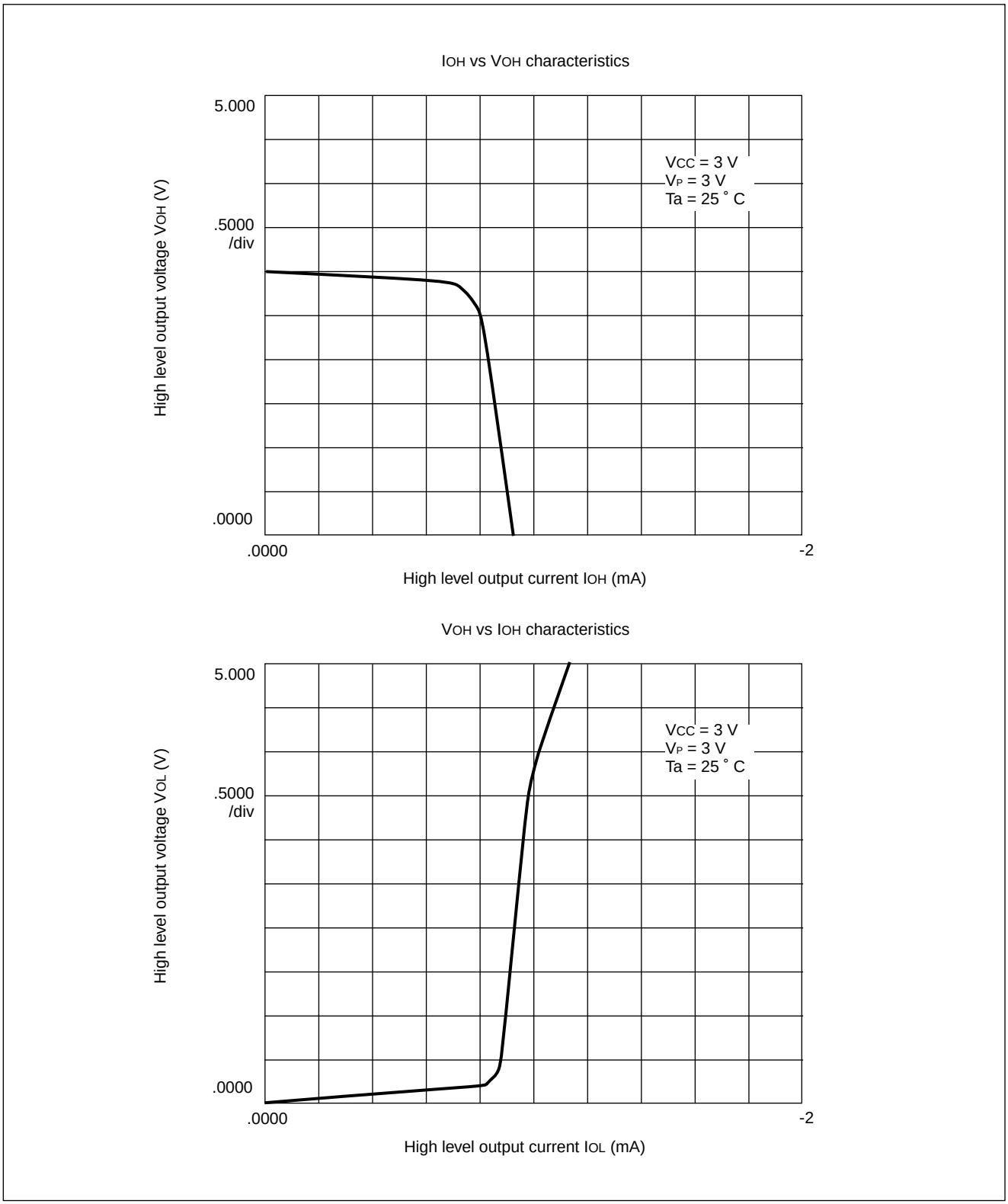
■ PHASE COMPARATOR OUTPUT WAVEFORMS



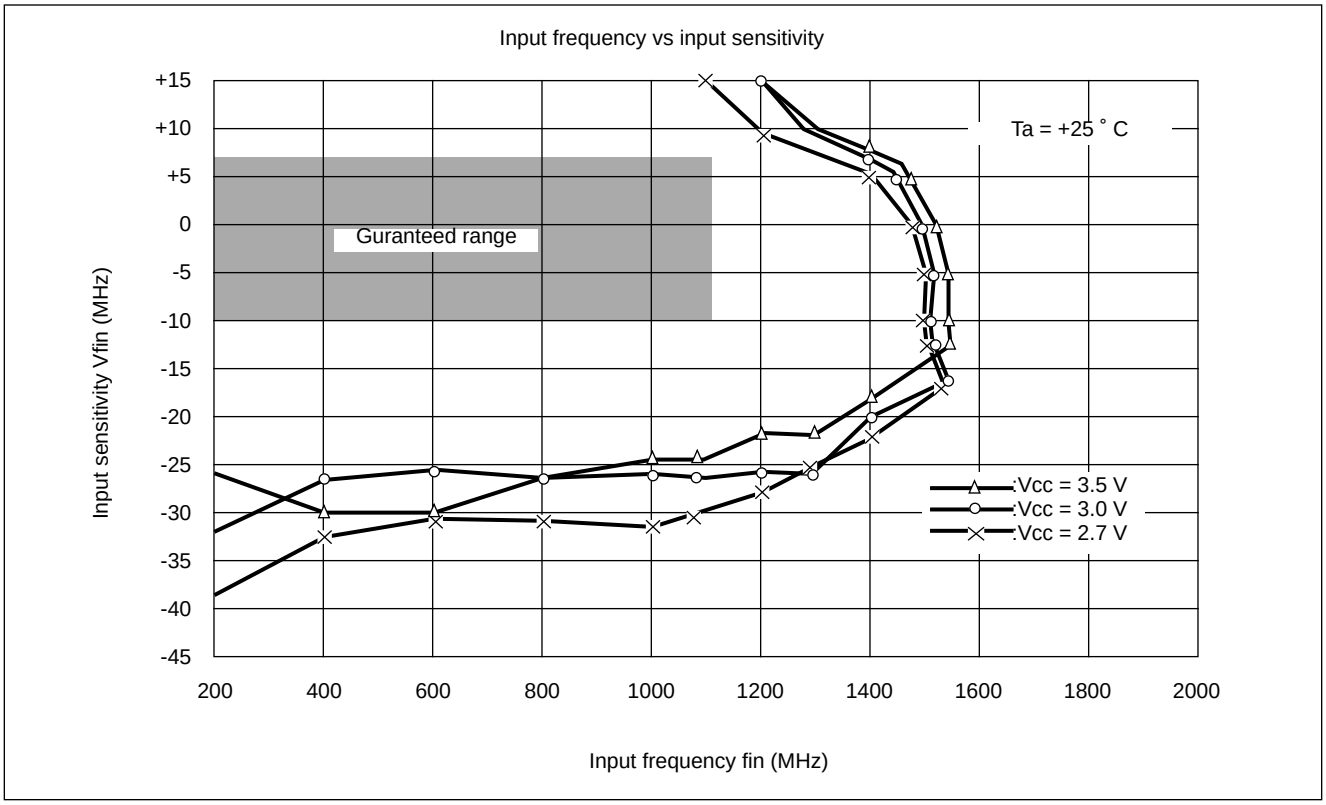
Notes:
- A phase differecnce is detected between -2π and +2π, with gain = Vp/4π
- The LD output goes low when it becomes phase between phase difference two or more. The LD output goes high when it remains equal to or smaller than twl, for three cycles or more.
- twu and twL are determined by the OSCIN input frequency as follows:
  twu ≥ 8/fosc (s)
  When focs = 12.8 MHz: twu ≥ 625 ns
  twl ≤ 16/fosc (s)
  When fosc = 12.8 MHz: twl ≤ 1250 ns

■ TYPICAL CHARACTERISTIC CURVES

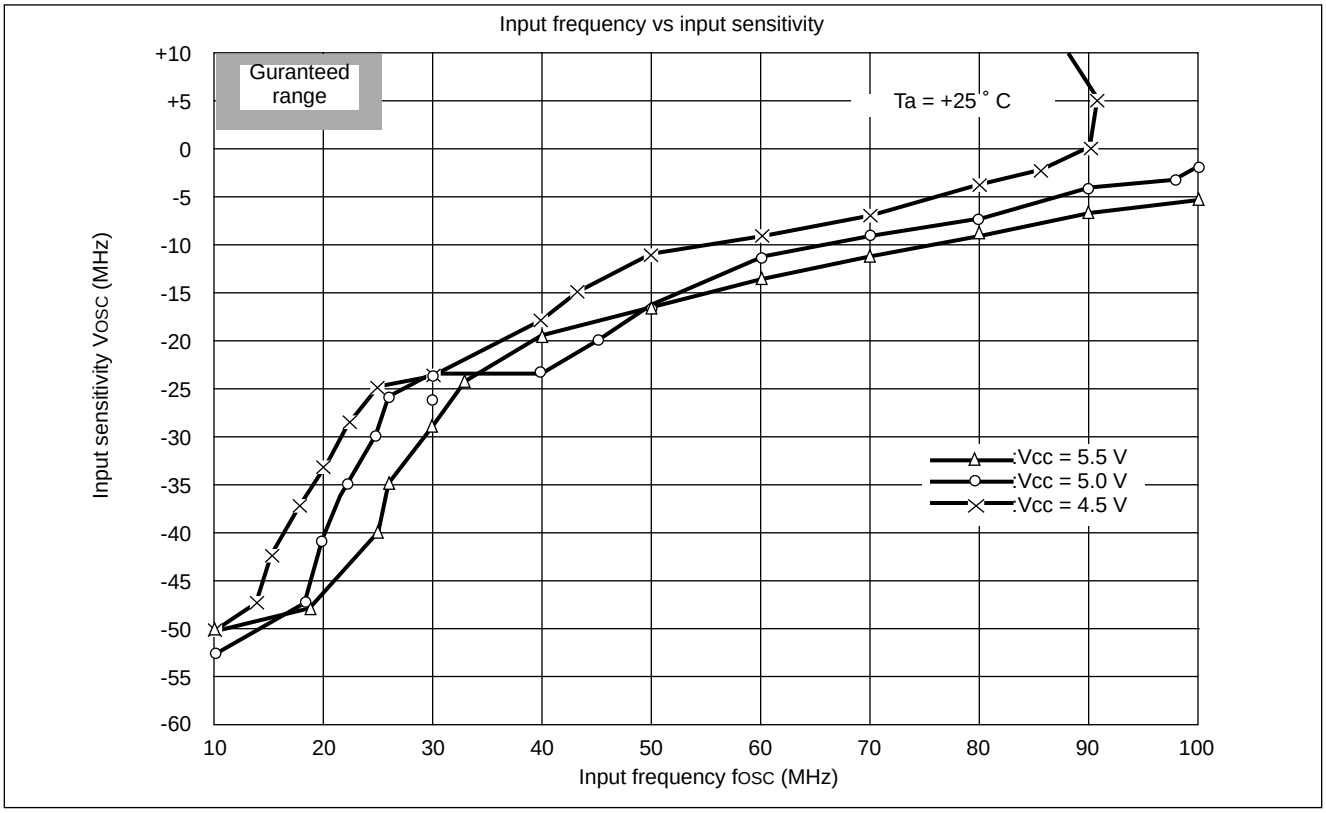
1. D_O Output Current Characteristics



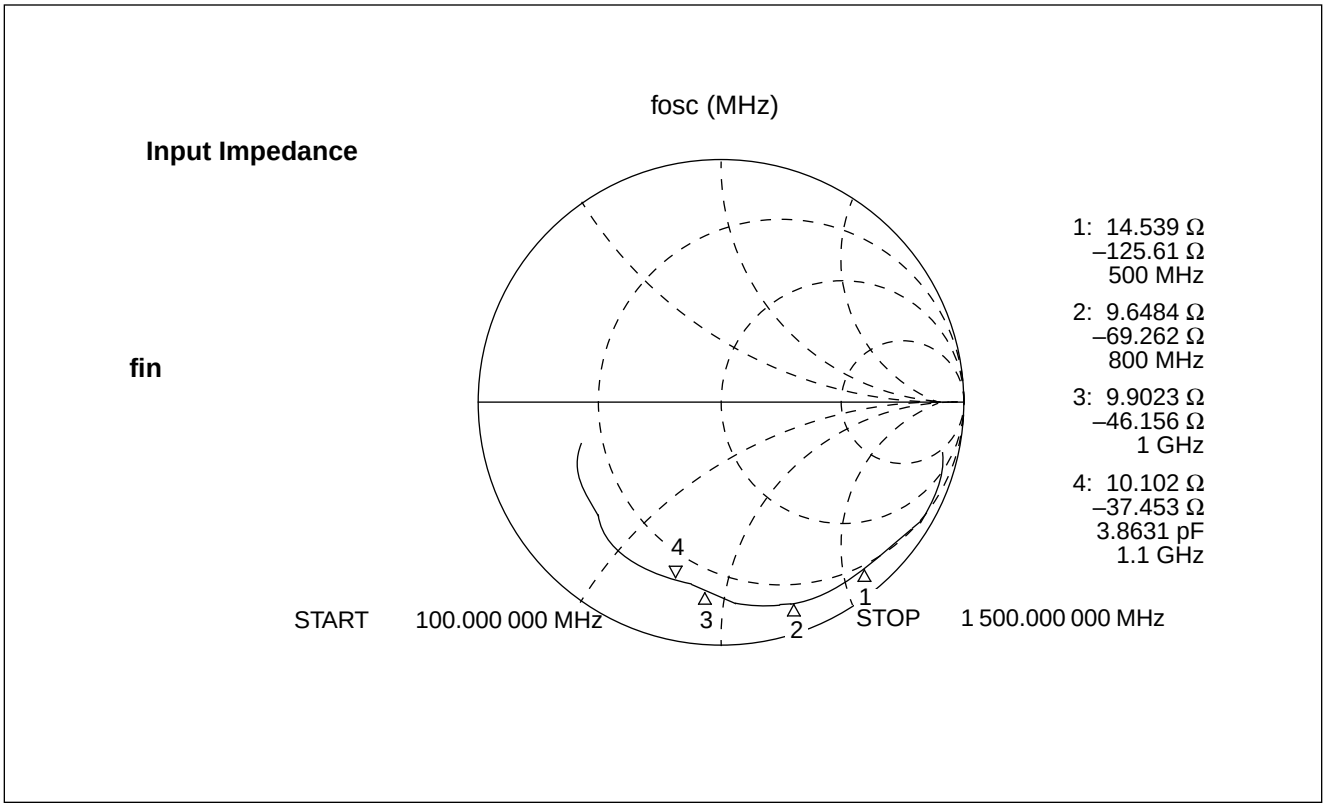
2. fin Input Sensitivity Characteristics



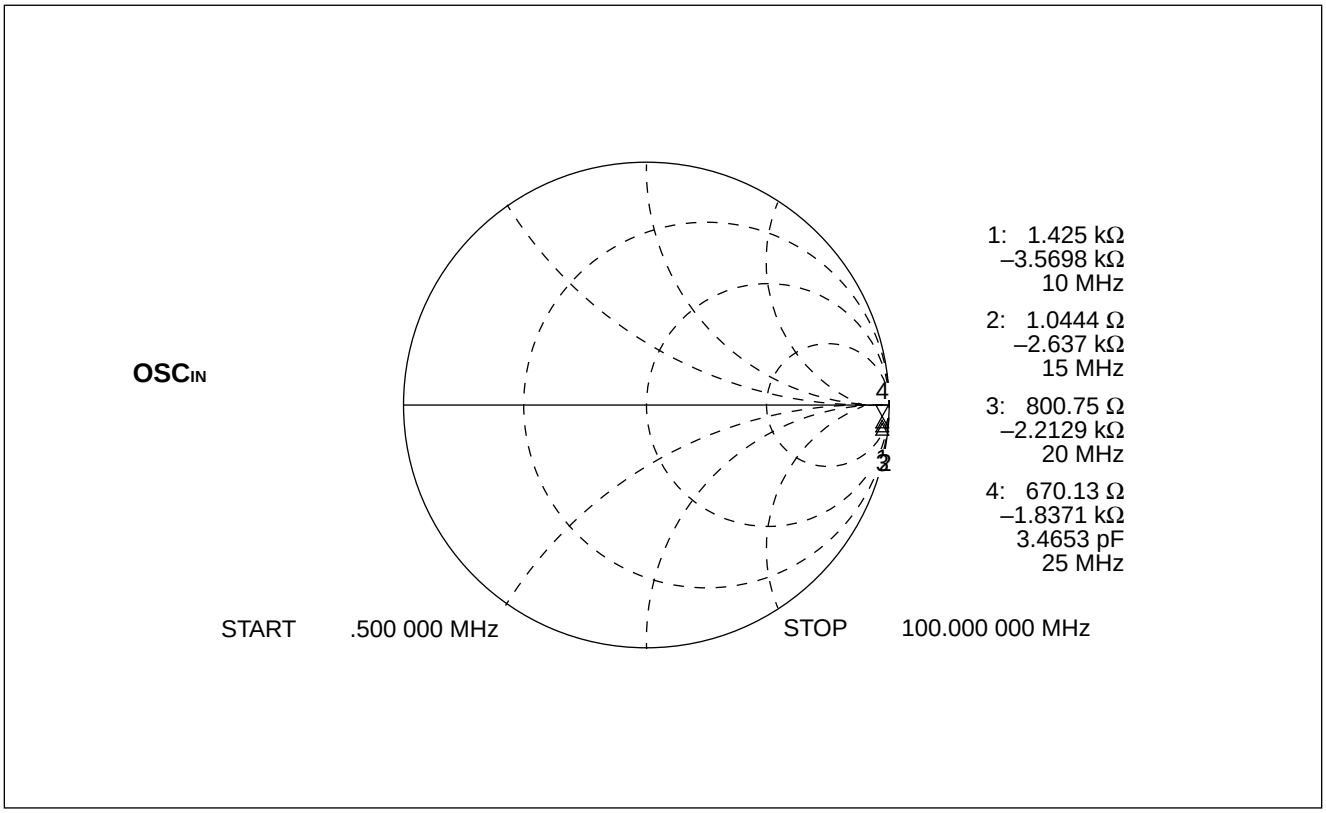
3. OSC_{IN} Input Sensitivity Characteristics



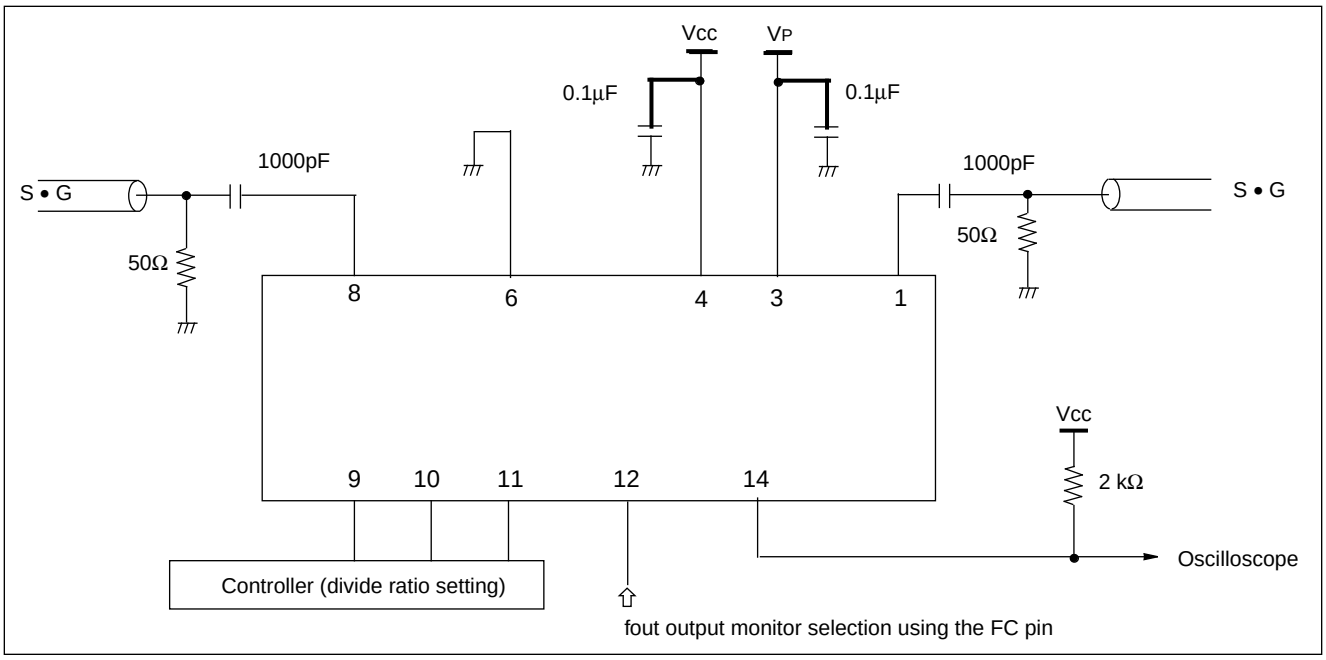
4. fin Input Impedance Characteristics



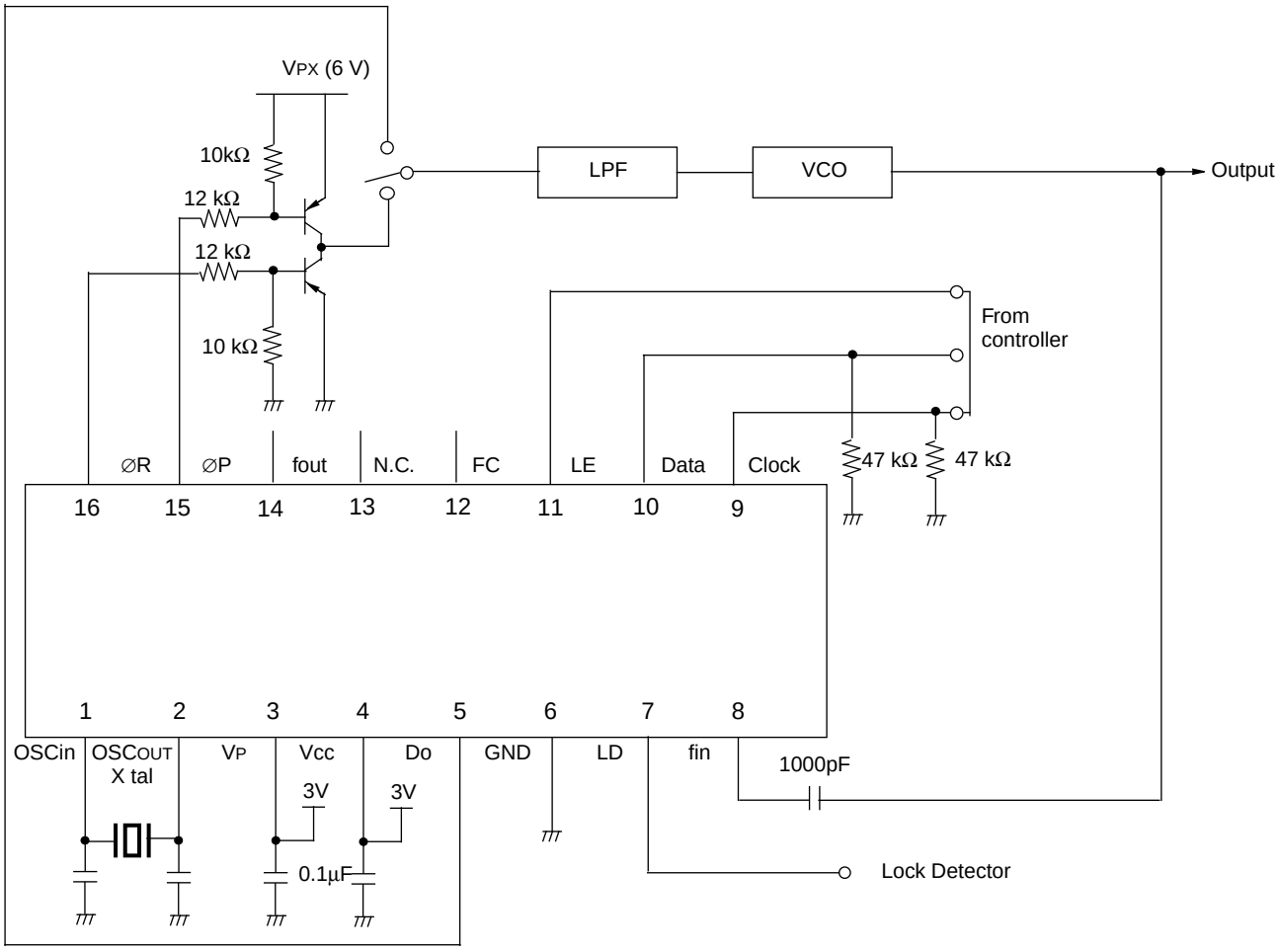
5. OSC_{IN} Input Impedance Characteristics



■ TEST CIRCUIT EXAMPLE (fin/OSC_{IN} Input Sensitivity Measurement)



■ APPLICATION EXAMPLE (16-pin Package)

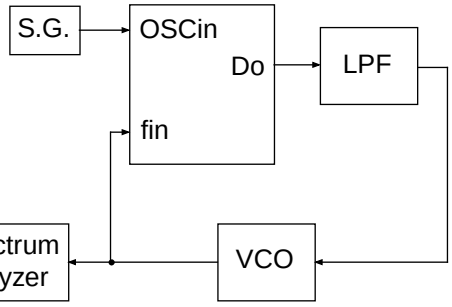


VPX	6V max.
VP	Connect the pin to Vcc when the internal charge pump is not used.
LE, FC	With pull-up resistor
ØP, fout	N channel open-drain output
ØR	CMOS output

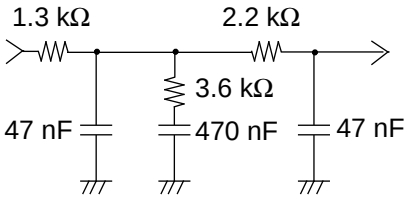
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plots show lock up time, phase noise, and reference leakage.

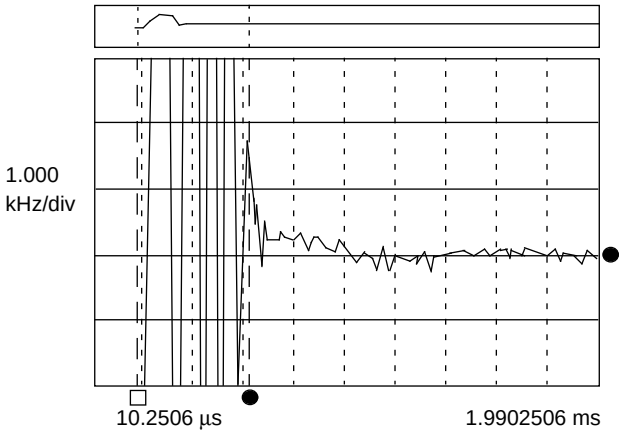
Test Circuit



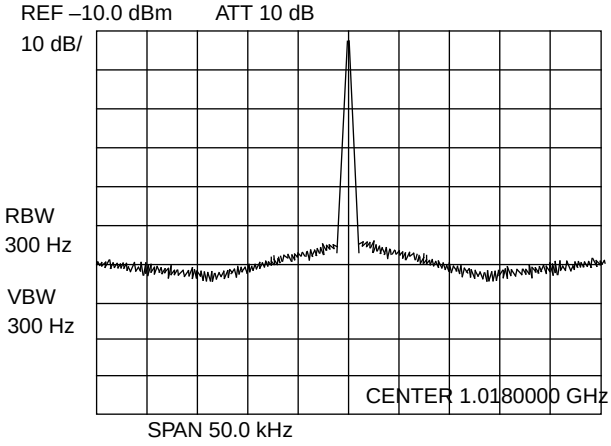
- f_{VCO} = 836.49 MHz
- K_V = 12 MHz/V
- f_r = 30 kHz
- f_{OSC} = 15.36 MHz
- LPF



PLL Lock Up Time = 12 ms
(824.010 MHz → 848.97 MHz, within ±800 Hz)

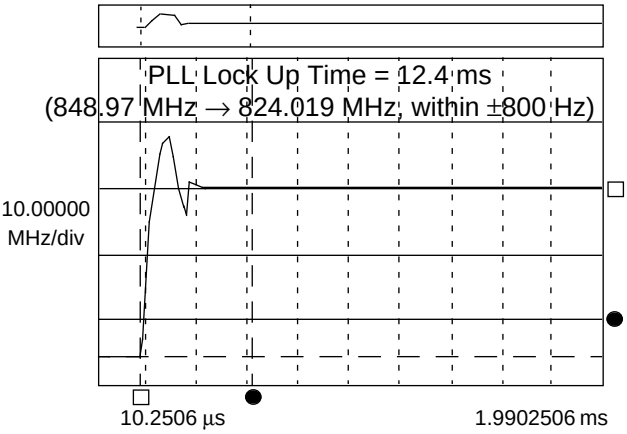


PLL Phase Noise
@ within loop band = 78.9 dBc/Hz

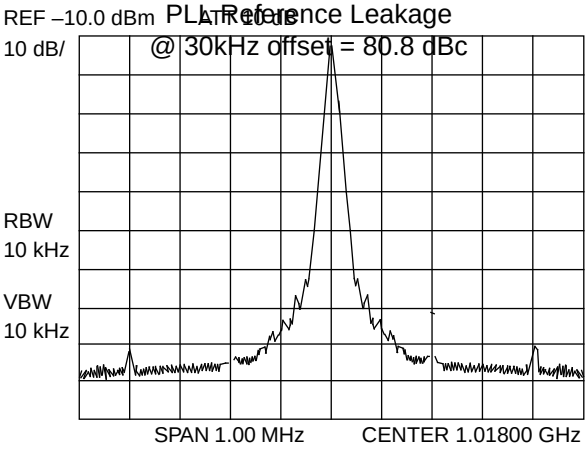


PLL Reference Leakage
@ 200kHz offset = 68dBc

PLL Lock Up Time = 12.4 ms
(848.97 MHz → 824.019 MHz, within ±800 Hz)



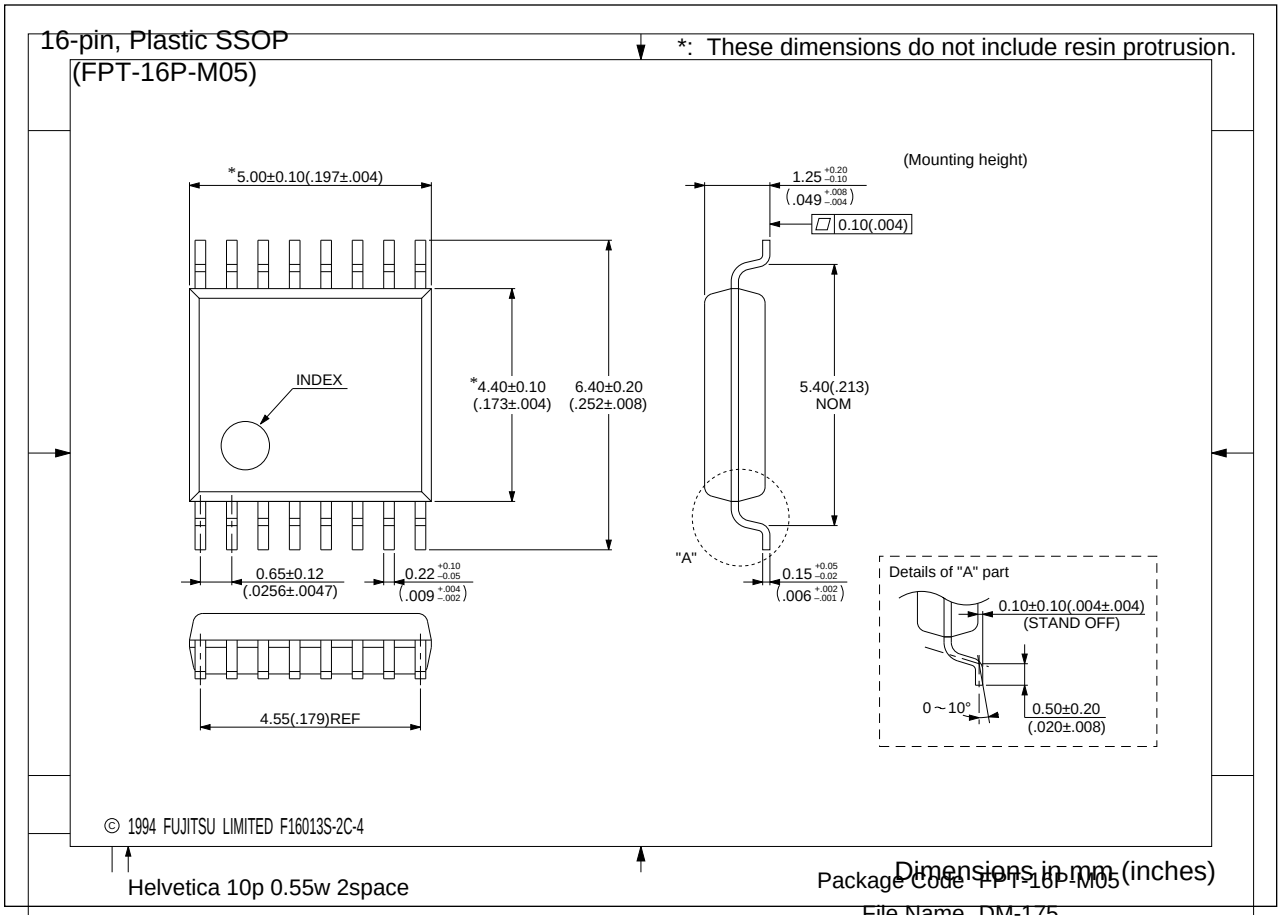
PLL Reference Leakage
@ 30kHz offset = 80.8 dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15A01PFV1	16-pin, Plastic SSOP (FPT-16P-M05)	
MB15A01PFV2	20-pin, Plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSIONS



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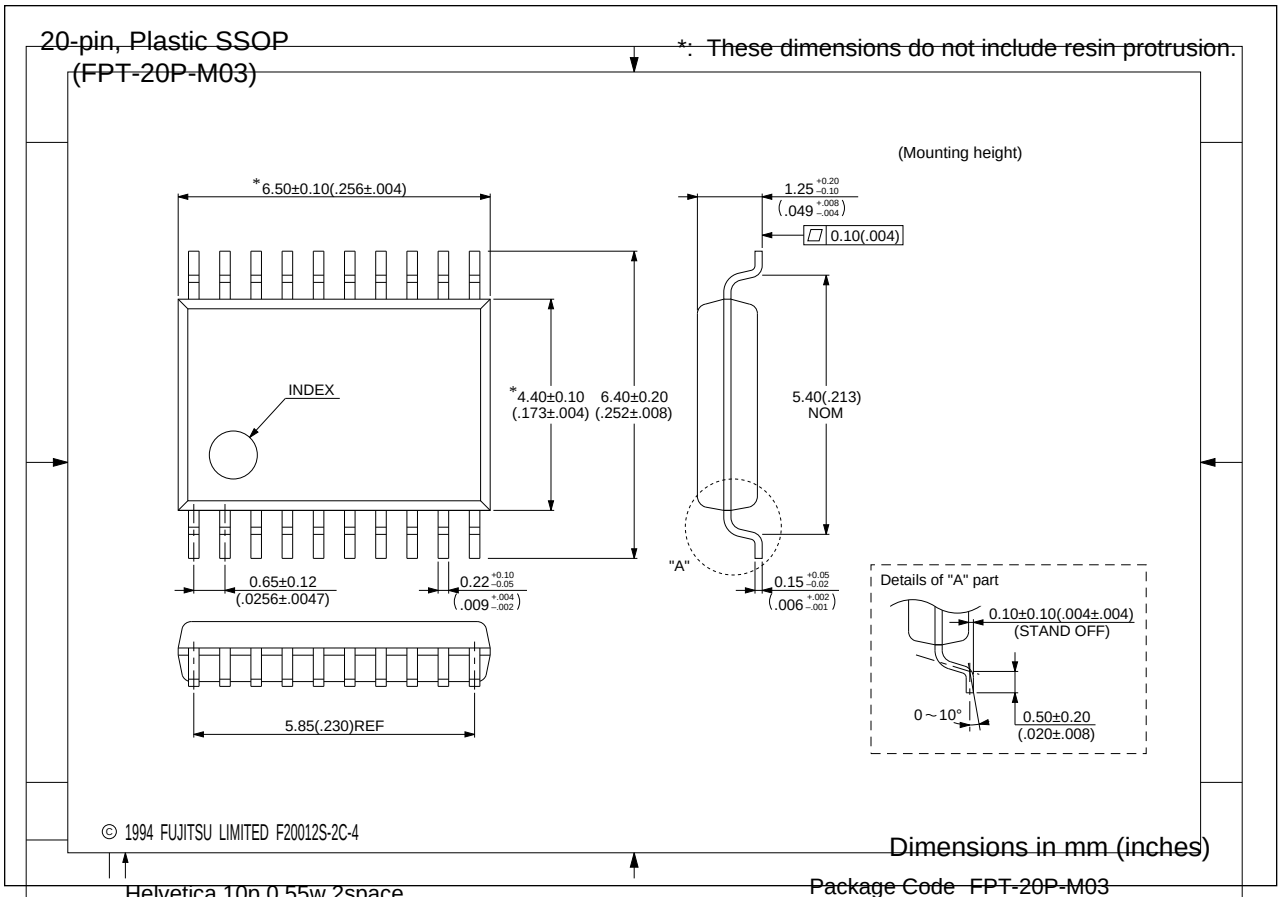
20-pin, Plastic SSOP
(FPT-20P-M03)
*: These dimensions do not include resin protrusion.
(Mounting height)
*6.50±0.10(.256±.004)
1.25 +0.20 −0.10 (.049 +.008 −.004)
0.10(.004)
INDEX
*4.40±0.10 (.173±.004)
6.40±0.20 (.252±.008)
5.40(.213) NOM
"A"
0.65±0.12 (.0256±.0047)
0.22 +0.10 −0.05 (.009 +.004 −.002)
0.15 +0.05 −0.02 (.006 +.002 −.001)
Details of "A" part
0.10±0.10(.004±.004) (STAND OFF)
0~10°
0.50±0.20 (.020±.008)
5.85(.230)REF
© 1994 FUJITSU LIMITED F20012S-2C-4
Dimensions in mm (inches)
Package Code FPT-20P-M03
Helvetica 10p 0.55w 2space

FUJITSU LIMITED

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F9512