October 1990
Edition 1.0

FUJITSU

DATA SHEET

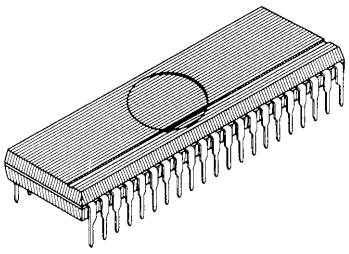
MB86260

D/A CONVERTER (4CH, 4BIT) WITH LOOK UP TABLE

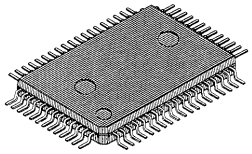
CMOS DIGITAL TO ANALOG CONVERTER (4CH 4-BIT) WITH LOOK UP TABLE

The MB86260 contains four 4-bit D/A converters, which can handle either monochrome or color, and a 256 word Look Up Table (LUT). It can simultaneously display 256 colors out of a total color palette of 4096 colors. It is also equipped with a text data overlay function, and operates with a 50 MHz cycle time.

- 50 MHz, 4-bit precision D/A converters
- Contains RGB color D/A converters and monochrome D/A converter
- Simultaneously display of 256 colors out of a total palette of 4096 colors
- Text overlay display
- Text brightness control
- Asynchronous writing to and reading from LUT
- Flicker prevention function using dual port RAM
- Current driven analog output with 75 Ohm external termination (Each terminal 37.5 Ohms)
- Fine control of analog output level



PLASTIC PACKAGE (DIP–42P–MO1)



PLASTIC PACKAGE (FTP–64P–MO1)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

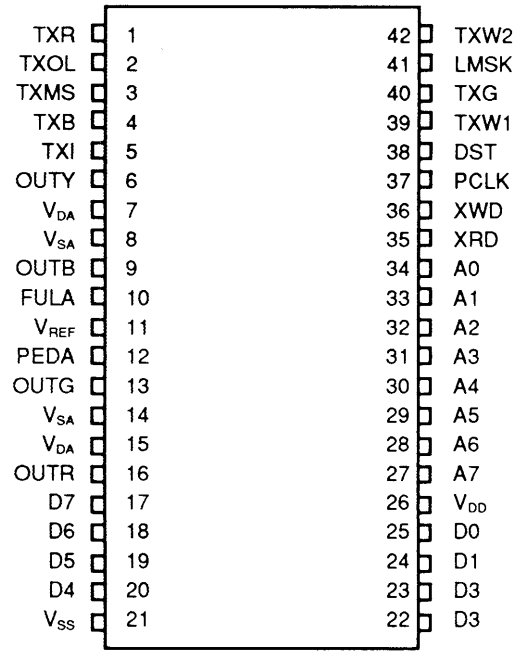
ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Pin Name	Value	Unit
Power supply voltage	V_{DD}	V_{DD}, V_{DA}	–0.3 to 6.0	V
Pin current	I_{TD}	V_{DA}	–10 to 200	mA
	I_{TP}	V_{DD}	–10 to 50	mA
	I_{TS}	V_{SA}	–200 to 10	mA
	I_{TO}	OUTY, OUTR, OUTG, OUTB	–10 to 35	mA
	I_{TA}	PEDA, FULA, V_{REF}	–10 to 10	mA
Pin voltage	V_T	Other than power supply pin.	–0.3 to V_{DD} +0.3	V
Storage temperature	V_{stg}	–	–40 to 125	°C
Operating temperature	T_A	–	0 to 70	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

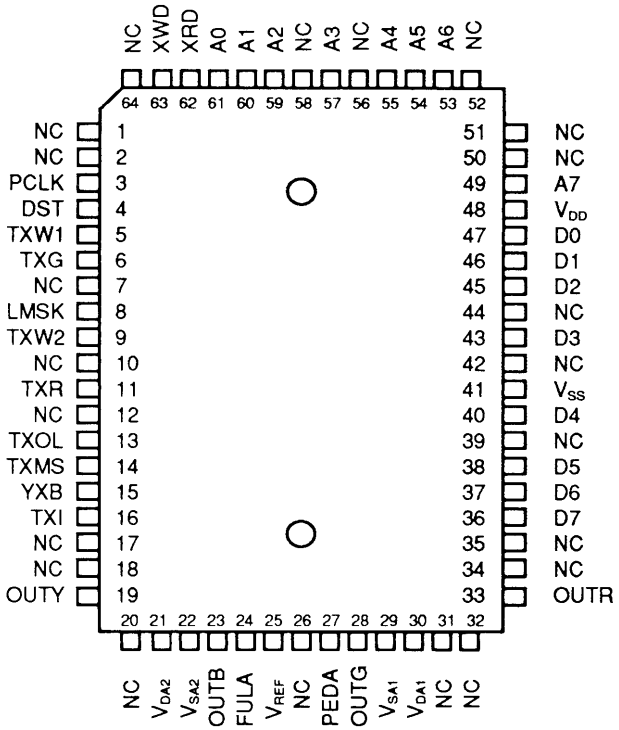
PIN ASSIGNMENT

(TOP VIEW)



(DIP-42P-M01)

(TOP VIEW)



(FPT-64P-M01)

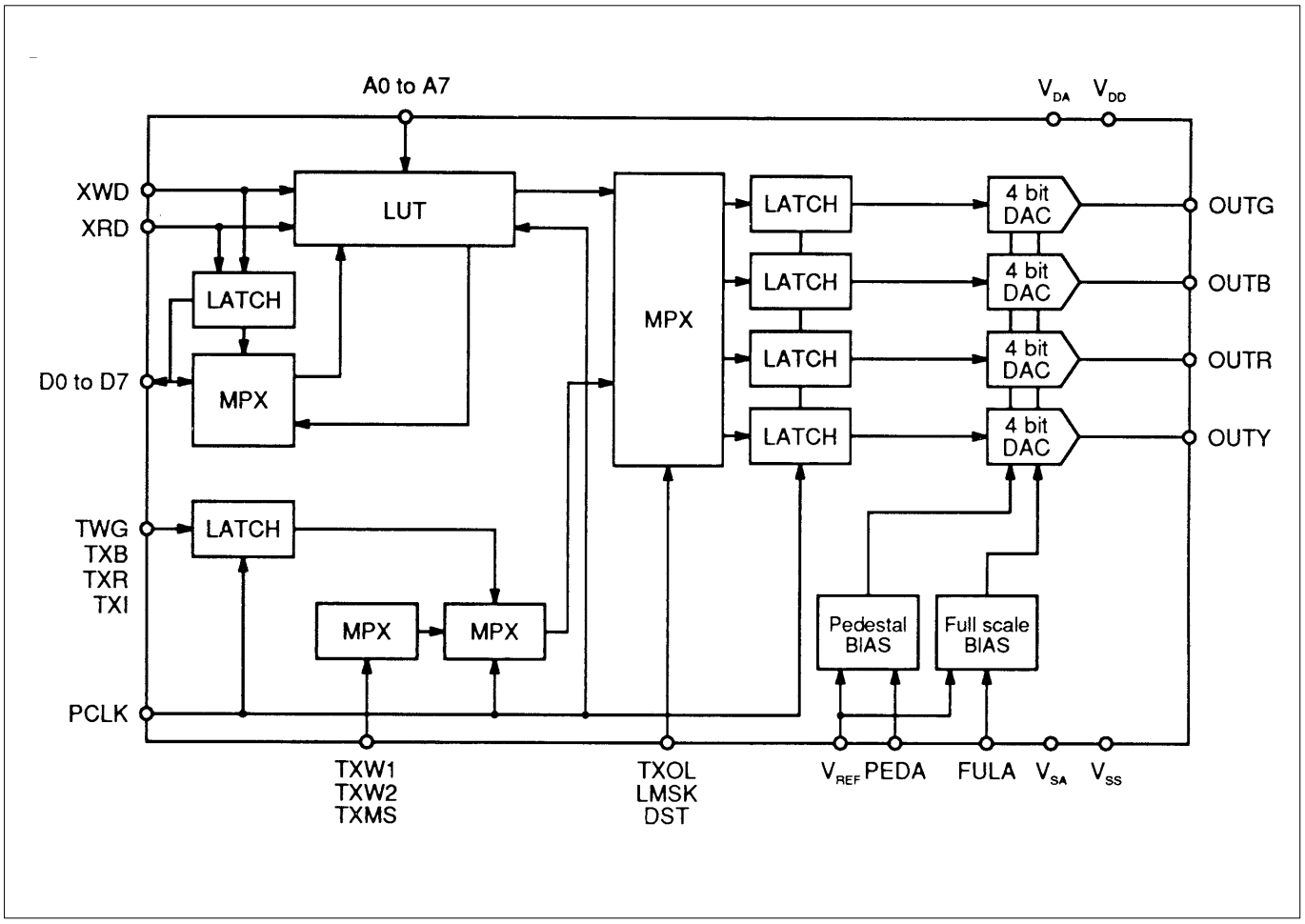
INPUT/OUTPUT SIGNALS AND THEIR FUNCTIONS

<table>
<tr><th rowspan="2">Category</th><th colspan="2">Pin No.</th><th rowspan="2">Pin Name</th><th rowspan="2">I/O</th><th rowspan="2">Explanation of Functions</th></tr>
<tr><th>DIP</th><th>QFP</th></tr>
<tr><td rowspan="3">Clock</td><td>37</td><td>3</td><td>PCLK</td><td>I</td><td>This is the pixel clock. Text data and V-RAM data are loaded in accordance with this clock.</td></tr>
<tr><td>35</td><td>62</td><td>XRD</td><td>I</td><td>This is the LUT read clock. It loads the select data for either R, G, or B at the falling edge. (The read address is set by the XWD signal.)</td></tr>
<tr><td>36</td><td>63</td><td>XWD</td><td>I</td><td>This is the LUT write clock. It loads the address, R, G, and B select data at the falling edge. It also writes the address, R, G, and B data at the rising edge.</td></tr>
<tr><td rowspan="2">Data</td><td>27 to 34</td><td>49, 53, to 55, 57, 59 to 61</td><td>A7 to A0</td><td>I</td><td>V-RAM data (LUT address) signals, load using the PCLK signal.</td></tr>
<tr><td>17 to 20
22 to 25</td><td>36 to 38, 40, 43, 45 to 47</td><td>D7 to D0</td><td>I/O</td><td>Interface bus to the CPU. Loads address and R G B select data with D6 and D7. Performs input and output of R G B data with D0 to D3, and LUT address data input with D0 to D7.</td></tr>
<tr><td rowspan="11">Control</td><td>41</td><td>8</td><td>LMSK</td><td>I</td><td>This signal masks the LUT output. LUT data is output when LMSK = 1. When LMSK = 0, mask mode is turned on, and the LUT output is set to blanking level.</td></tr>
<tr><td>2</td><td>13</td><td>TXOL</td><td>I</td><td>This signal is for overlaying text data. When TXOL = 0 the LUT output signal is output, and when TXOL = 1 the text data output signal is output.</td></tr>
<tr><td>3</td><td>14</td><td>TXMS</td><td>I</td><td>The text data display mode can be selected with the TXMS signal. The white balance mode is selected when TXMS = 1, and the enhancement mode is selected when TXMS = 0.</td></tr>
<tr><td>39</td><td>5</td><td>TXW1</td><td rowspan="2">I</td><td rowspan="2">The intensity of the white in white balance mode, and the enhanced color in enhancement changing mode, are selected using these two bits.
<table><tr><th>TXW2</th><th>TXW1</th><th>Intensity (Weight)</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>3</td></tr></table></td></tr>
<tr><td>42</td><td>9</td><td>TXW2</td></tr>
<tr><td>4</td><td>15</td><td>TXB</td><td>I</td><td>This is the data signal for BLUE text in the color signal.</td></tr>
<tr><td>1</td><td>11</td><td>TXR</td><td>I</td><td>This is the data signal for RED text in the color signal.</td></tr>
<tr><td>40</td><td>6</td><td>TXG</td><td>I</td><td>This is the data signal for GREEN text in the color signal.</td></tr>
<tr><td>5</td><td>16</td><td>TXI</td><td>I</td><td>This is the brightness signal for text data.</td></tr>
<tr><td>38</td><td>4</td><td>DST</td><td>I</td><td>This signal controls the display period. When DST = display is not performed (the output is set to blanking level); display is possible when DST = 1.</td></tr>
<tr><td>10</td><td>24</td><td>FULA</td><td>O</td><td>The pedestal level current is regulated with external resistance connected between this pin and V_{SA}.</td></tr>
<tr><td>12</td><td>27</td><td>PEDA</td><td>O</td><td>The synchronous level current is regulated with external resistance connected between this pin and V_{SA}.</td></tr>
<tr><td>11</td><td>25</td><td>V_{REF}</td><td>I</td><td>This is the reference voltage input pin for bias setting.</td></tr>
</table>

INPUT/OUTPUT SIGNALS AND THEIR FUNCTIONS (continued)

Category	Pin No.		Pin Name	I/O	Explanation of Functions
	DIP	QFP			
Output	6	23	OUTB	O	Analog output signal for BLUE signal.
	16	33	OUTR	O	Analog output signal for RED signal.
	13	28	OUTG	O	Analog output signal for GREEN signal.
	6	19	OUTY	O	Analog output signal for monochrome.
Power Supply	8, 14	22, 29	V_{SA}	–	Ground pin for analog section.
	7, 15	21, 30	V_{DA}	–	Power supply for analog section.
	26	48	V_{DD}	–	Power supply for digital section.
	21	41	V_{SS}	–	Ground pin for digital section.
Others	–	1, 2, 7, 10, 12, 17, 18, 20, 26, 31, 32, 34, 35, 39, 42, 44, 50, 51, 52, 56, 58, 64	NC	–	No connection. Must be kept open.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin name	Minimum	Typical	Maximum	Unit
Power supply voltage	V_{DD}	V_{DD}, V_{DA}	4.75	5.0	5.25	V
Reference voltage	V_{REF}	V_{REF}	2.0	2.5	3.0	V
Load resistance	R_L	OUTY, OUTR OUTG, OUTB	–	37.5	–	Ω
Resistance for setting current	R_R	FULA, PEDA	–	5.22	–	kΩ
Output voltage	V_{OC}	OUTY, OUTR OUTG, OUTB	0	–	0.8	V
Operating temperature	T_A	–	–	25	–	°C

Note: R_L: Composite load resistance at each pin.

ELECTRICAL CHARACTERISTICS

V_{REF} = 2.5 V, R_{PR} = R_{FR} = 5.22 KΩ
R_{BL} = R_{RL} = R_{GL} = R_{YL} = 75Ω

Parameter	Symbol	Pin name	Minimum	Typical	Maximum	Unit
DAC full scale current	I_F	OUTY, OUTR OUTG, OUTB	18	20	22	mA
Offset current for pedestal level	I_P	OUTY, OUTR OUTG, OUTB	1.2	1.33	1.5	mA
DAC non-linearity	LE	OUTY, OUTR OUTG, OUTB	–3	–	3	%FSR
DAC full scale current error between channels	ΔI_F	Definition: Maximum (I_F) – Minimum ($I_{F)}$	–	–	6	%FSR
DAC pedestal current error between channels	ΔI_P	Definition: Maximum (I_P) – Minimum (I_P)	–	–	6	%FSR
Bias setting pin current	V_B	FULA, PEDA	2.4	–	2.6	V
Power supply current	I_{DA}	V_{DD}, V_{DA}	–	120	160	mA

Figure	Parameter	Symbol	Minimum	Typical	Maximum	Unit
Figure 1	PCLK low clock width	t_{LCW}	10.0	–	–	ns
	PLCK high clock width	t_{HCW}	10.0	–	–	ns
	Maximum operating frequency	–	–	–	50	MHz
Figure 2	LUT data set up time for PCLK	t_{STA}	3.1	–	–	ns
	LUT data hold time for PCLK	t_{HTA}	11.2	–	–	ns
Figure 3	Text data set up time for PCLK	t_{STD}	3.1	–	–	ns
	Text data hold time for PCLK	t_{HTD}	11.2	–	–	ns
Figure 4	XWD low clock width	t_{WLCW}	75.7	–	–	ns
	XWD high clock width	t_{WHCW}	32.7	–	–	ns
	Select data set up time	t_{SDST}	13.7	–	–	ns
	Select data hold time	t_{SDHT}	4.5	–	–	ns
	Address set up time	t_{WAST}	14.7	–	–	ns
	Address hold time	t_{WAHT}	3.7	–	–	ns
	Write data set up time	t_{WDST}	60.0	–	–	ns
	Write data hold time	t_{WDHT}	3.7	–	–	ns
	LUT data out delay	t_{OD}	32.7	–	–	ns
	LUT data hold time	t_{OHD}	4.5	–	–	ns
Figure 5	Effective output time for PCLK	t_V	1.9	–	–	ns
	Output settling time for PCLK	t_S	–	–	22.4	ns
Figure 6	Effective output time for PCLK	t_{VP1}	0	–	–	ns
	Output settling time for PCLK	t_{SP1}	–	–	50.0	ns
	Effective output time for PCLK	t_{VP2}	0	–	–	ns
	OUtput settling time for PCLK	t_{SP2}	–	–	22.4	ns

*See timing charts on pages 6 and 7.

TIMING CHARTS

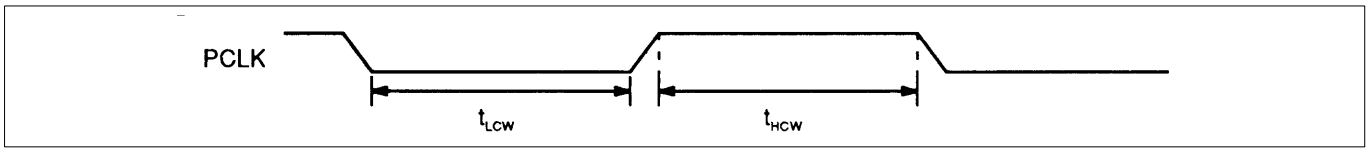


Figure 1. Clock input timing

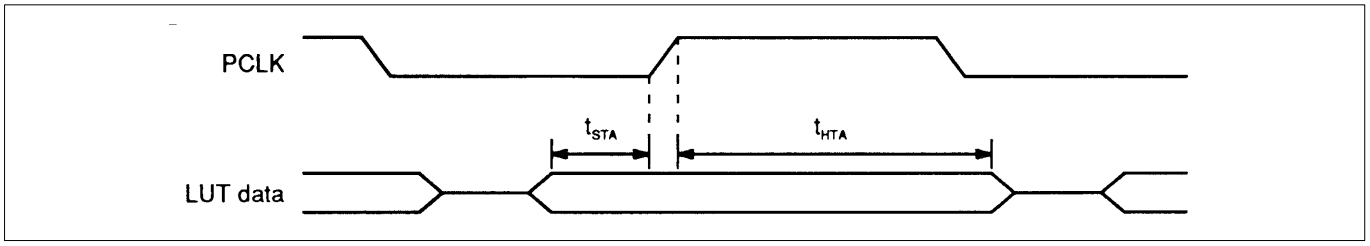


Figure 2. LUT data input timing

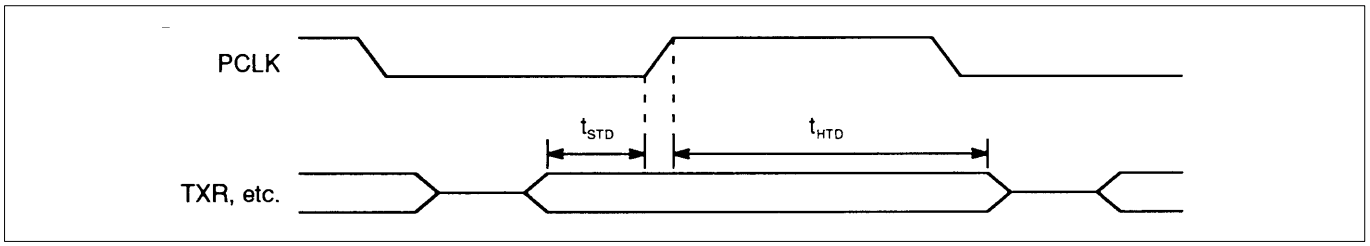


Figure 3. Text data input timing

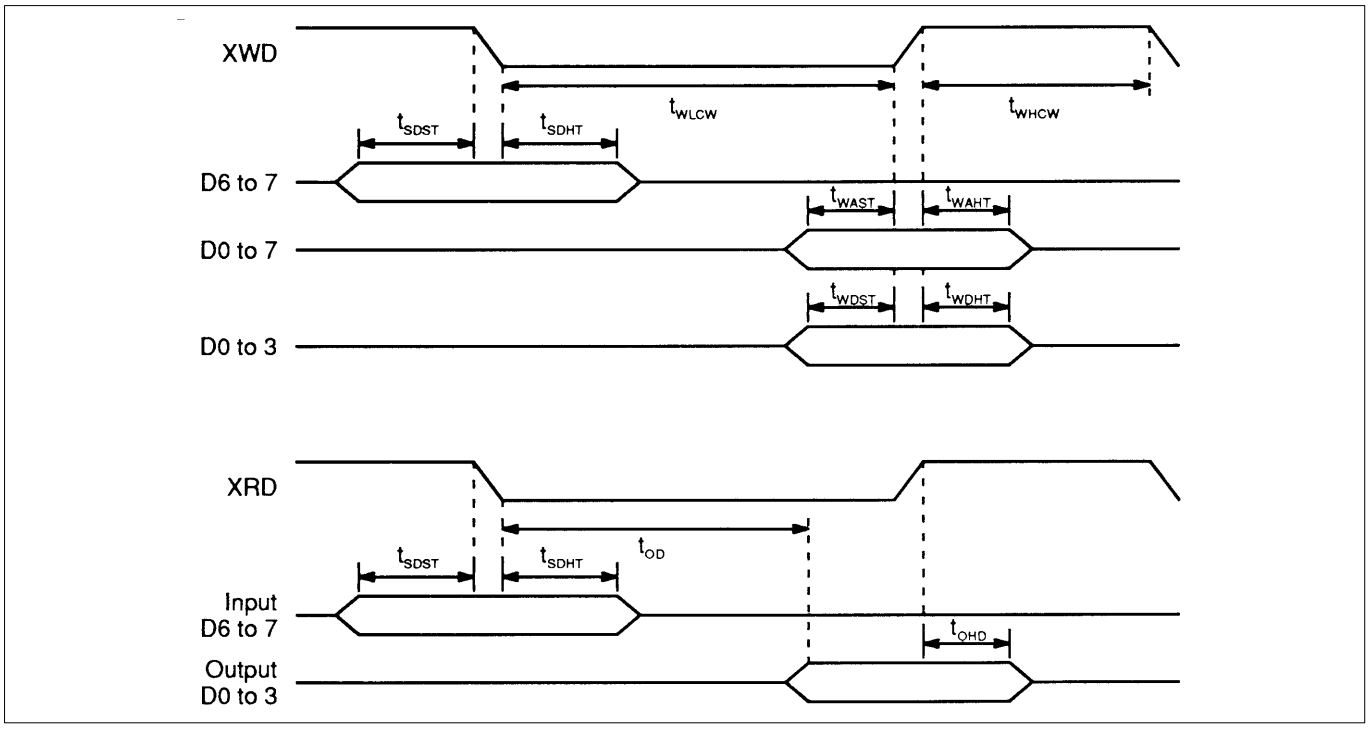


Figure 4. LUT update/read timing

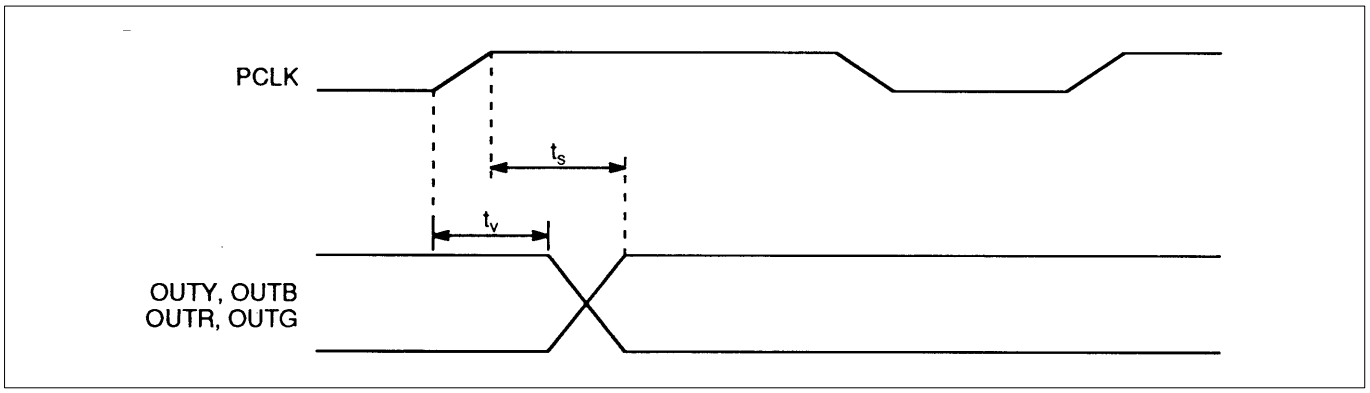


Figure 5. Color signal output timing

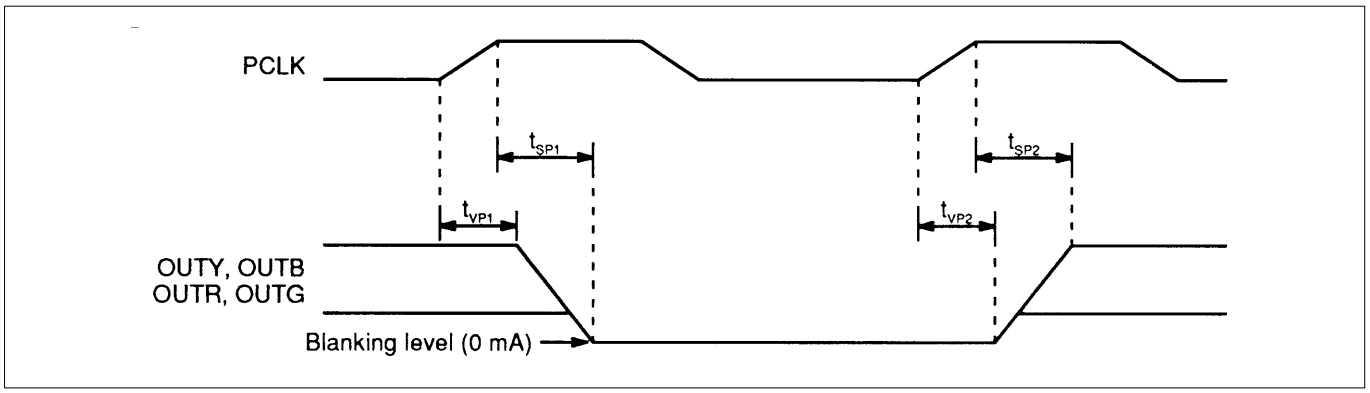


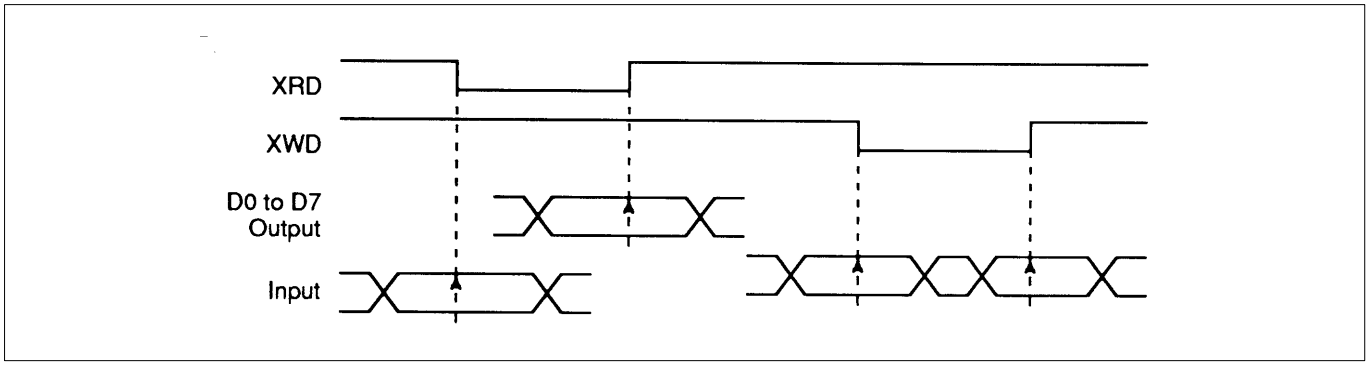
Figure 6. Blanking output timing

EXPLANATION OF FUNCTIONS

1. INTERFACE WITH CPU

An 8-bit data bus (D0 to D7), and two read/write signals (XRD/XWD) are used for the interface with the CPU.

1.1 Timing



- Demarcations between the LUT buffer R, G, B and LUT addresses are input according to D7 to D0 at the falling edge of XRD/XWD.
- Data input or output is performed according to D7 to D0, at the rising edge of XRD/XWD.
- In the LUT read, first the LUT address is read from D7 to D0 by XWD (the LUT address is selected from D7, D6 at the falling edge at this time). At the next XRD falling edge, the demarcations between R, G and B are loaded by D7, D6, and data is output.
- To rewrite LUT, first the LUT address is read by XWD from D7 to D0 (the LUT address is selected from D7, D6 at the falling edge at this time). Then at the next XWD falling edge, the demarcations between R, G and B are loaded by D7, D6, and data is written.

1.2 LUT Buffer and Address

An address is selected according to D7 or D6 values.

D7	D6	Contents
0	0	LUT address
0	1	B LUT
1	0	R LUT
1	1	G LUT

The procedure is as follows:

1.2.1 LUT update

① XWD ↓ Select LUT address. (D7 = 0, D6 = 0)

② XWD ↑ Input LUT address.

③ XWD ↓ Input R, G, B demarcations.

④ XWD ↑ Input data.

1.2.2 LUT read

① XWD ↓ Select LUT address. (D7 = 0, D6 = 0)

② XWD ↑ Input LUT address.

③ XRD ↓ Input R, G, B demarcations.

④ Output data. (D4 to D7 clipped to low.)

⑤ XRD ↑ Data loaded externally.

2. LUT MASK MODE

The LMSK signal masks the LOT output signal.
LMSK = 1 : LUT data is output.
= 0 : Sets to mask mode, LUT output is set to blanking level.
LUT data input is synchronized with PCLK. The data is reflected to the analog output via the same number of pipeline steps as the A0 to A7 signals within the IC.

3. TEXT DATA OVERLAY FUNCTION

The TXOL signal is provided for overlaying the LUT data with the text data.
TXOL = 0 : Select LUT.
= 1 : Select the text data signal of TXB, TXR, TXG, or TXI.
The TXOL signal and the text data signal inputs are synchronized with PCLK. The data is reflected to the analog output via the same number of pipeline steps as the A0 to A7 signals within the IC.

3.1 Text Data Display Mode

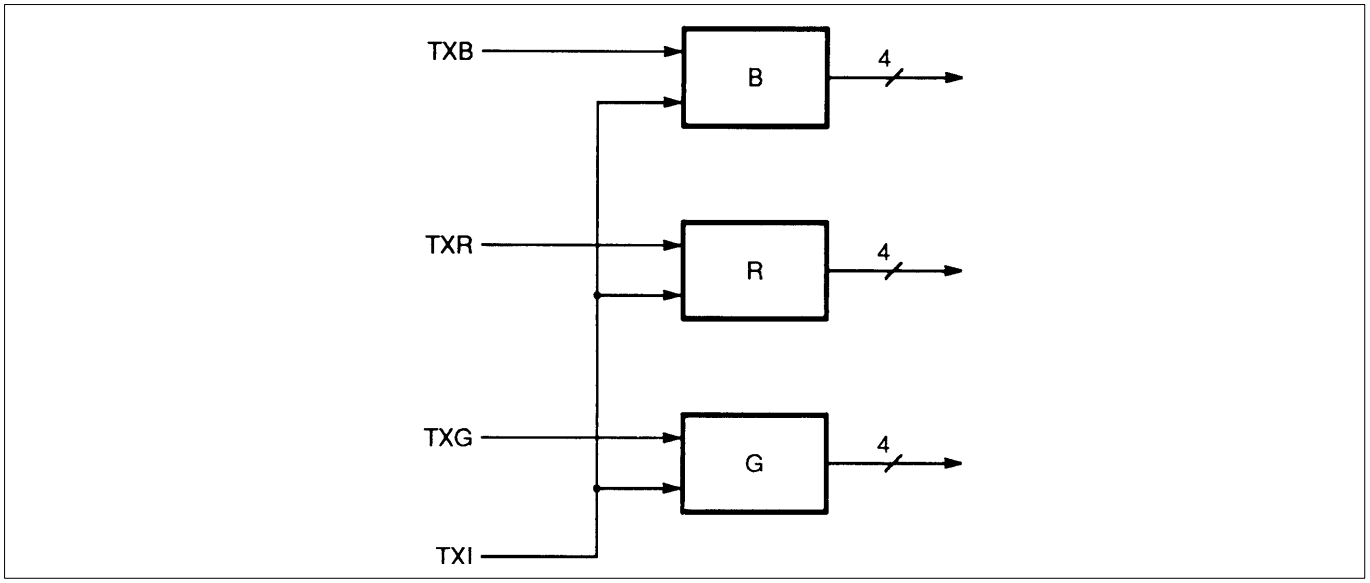
The text data display mode can be selected using the TXMS signal.
TXMS = 1 : White balance mode
= 0 : Enhancement mode
The enhanced color in the enhancement change mode, and the intensity of the white in the white balance mode can be selected by using the TXW1 signal and the TXW2 signal. (The TXMS signal, TXW1 signal and TXW2 signal input cannot be synchronized with the PCLK signal, and so it is necessary to be careful.)

TXW2	TXW1	Intensity (Enhancement)
0	0	0
0	1	1
1	0	2
1	1	3

EXPLANATION OF FUNCTIONS

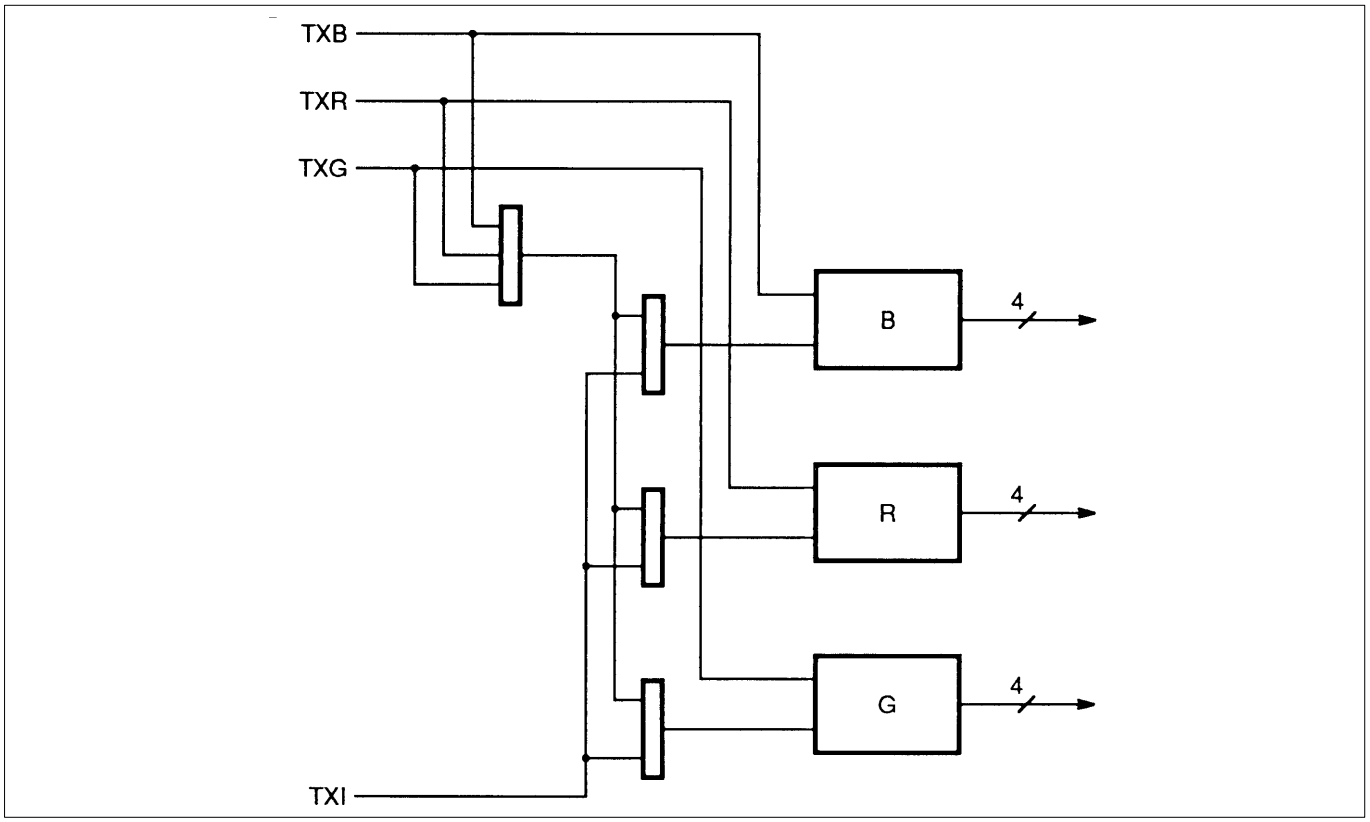
3.2 White Balance Mode

As shown in the clock diagram below, with the white-balance method, the output determinations according to the values of TXB, TXR and TXG, together with the TXI input signal, affect the text output without regard to other inputs.



3.3 Enhancement Change Mode

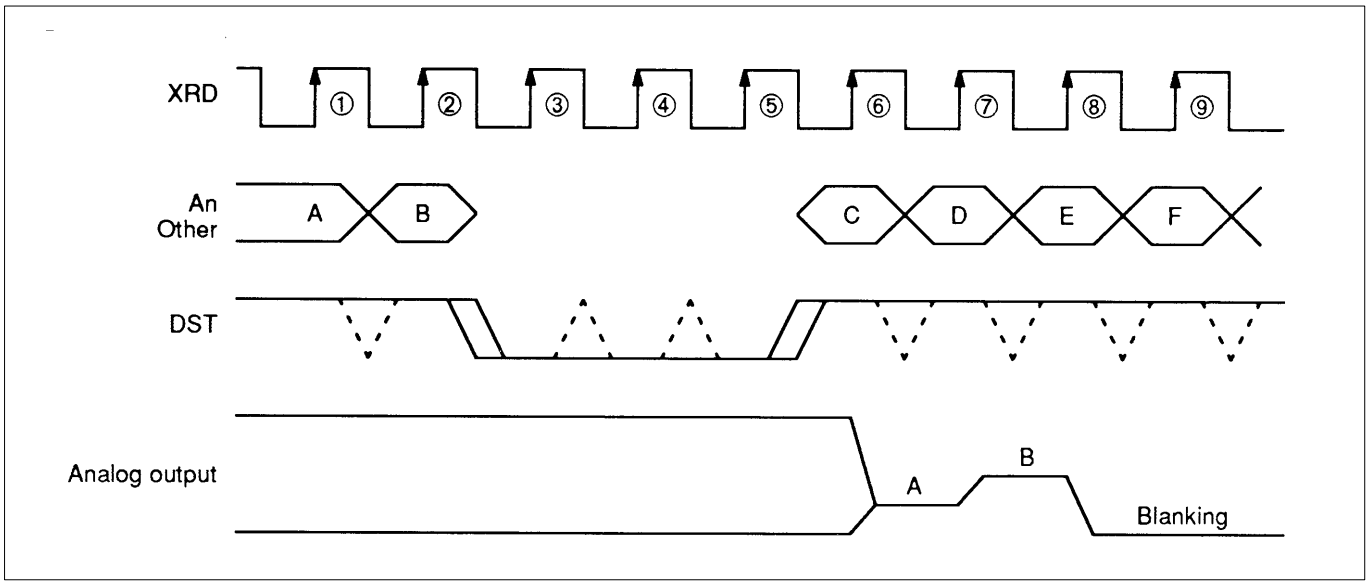
As shown in the clock diagram below, with the enhancement change mode, the output determinations according to the values of TXB, TXR and TXG, together with the TXl input signal, affect the text output according to whether input is TXB, TXR or TXG input values.



4. DISPLAY TIMING

- Analog output and DST timing
  PCLK and the following signals are output in synchronized timing.
  A0 to 7, TXB, TXR, TXG, TXI
  TXOL, LMSK, DST
  OUTR, OUTG, OUTB, OUTY

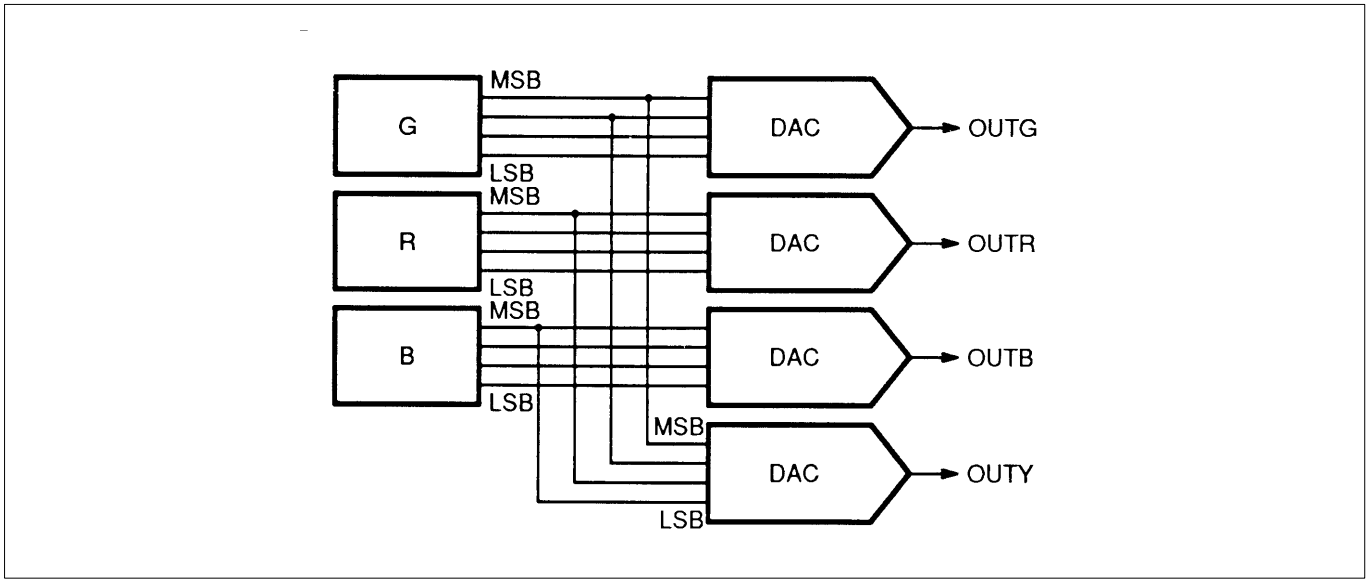
There are six pipeline steps.



5. MONOCHROME COMPILATION

Compilation is performed by fetching 4-bits from one of the 4-bit digital signals making up the OUTG, OUTR, OUTB output.

The monochrome 4 bits are compiled in the following order: MSB of G, 2nd bit of G, MSB of R, MSB of B.

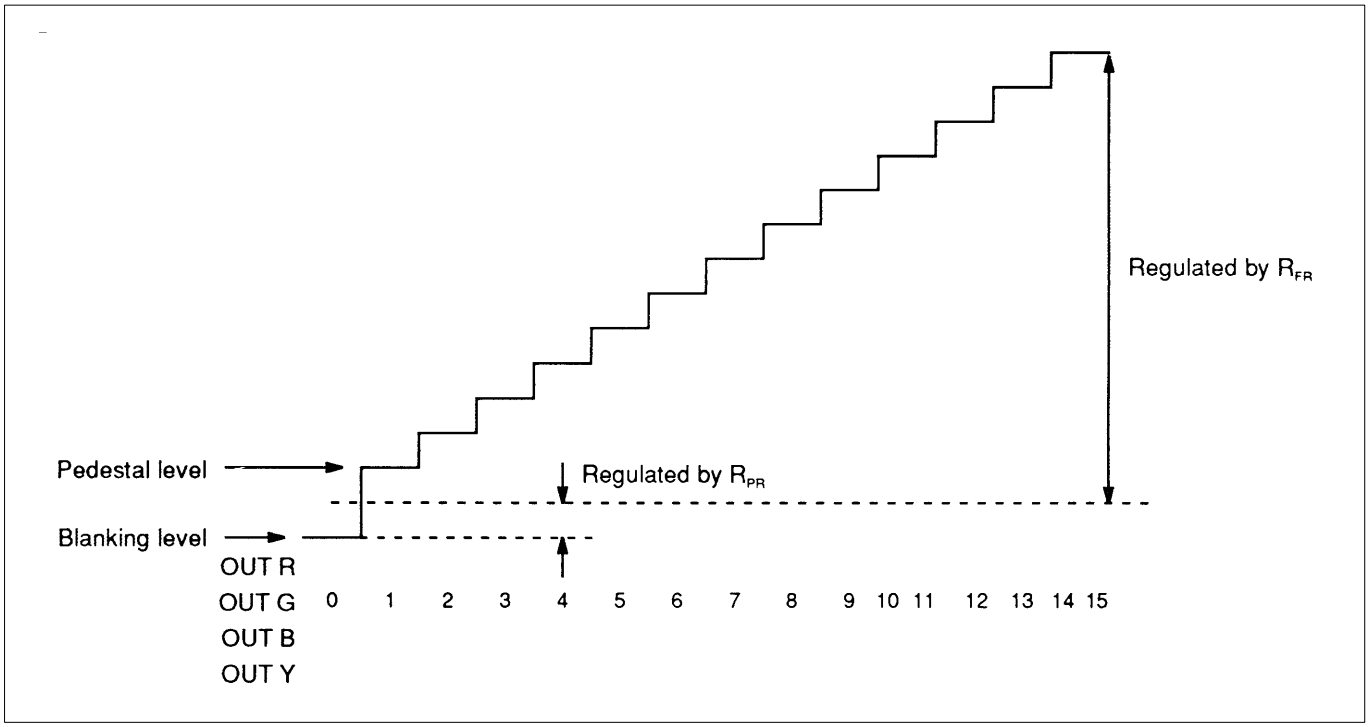


EXPLANATION OF FUNCTIONS

6. ANALOG OUTPUT OPERATION

The analog segment is made up of a 4 channel D/A converter (DAC) and its bias. The input data for each channel is input independently at 4-bit intervals. The input data is read on a rising edge of the PCLK clock. DAC output is also performed on a rising edge of the PCLK.

DAC output is obtained by electric current, and electric voltage can be obtained through the connection of load resistance. The output current is set by external resistance. Adjustment segments at different resistances are shown below.



The relationship between the output voltage and these resistances is as follows:

$$V_O = R_L \times \left(\frac{K_F}{R_{FR}} \times X + \frac{K_P}{R_{PR}} \times P \right) \times V_{REF}$$

X: Input code (0 to 15), P: 0 when X = 0,
1 when X ≠ 0

K_F = 2.784 K_P = 2.784

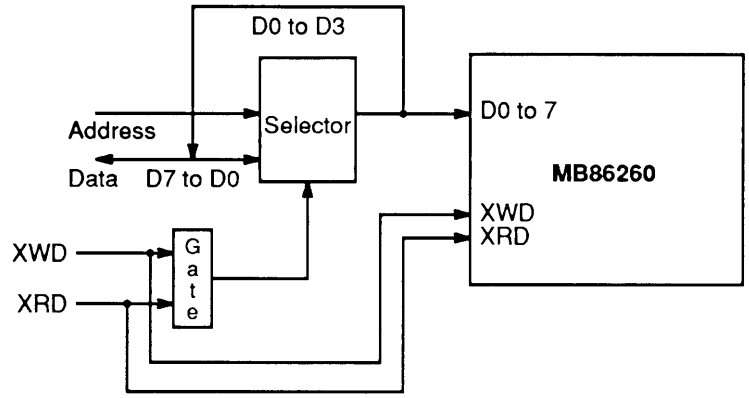
Usually: R = 37.5Ω, $R_{FR} = R_{PR}$ = 5.22Ω, V_{REF} = 2.5 V

Note: R_L: Load resistance at both terminals after composition.

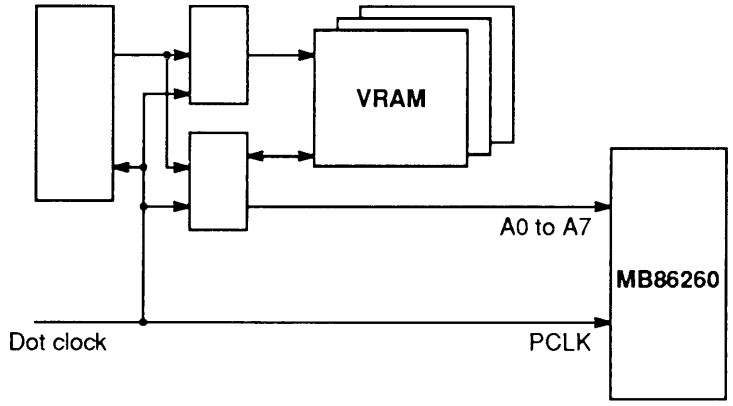
EXAMPLE OF EXTERNAL CONNECTION

INTERFACE CIRCUITS

1. CPU INTERFACE CIRCUIT EXAMPLE

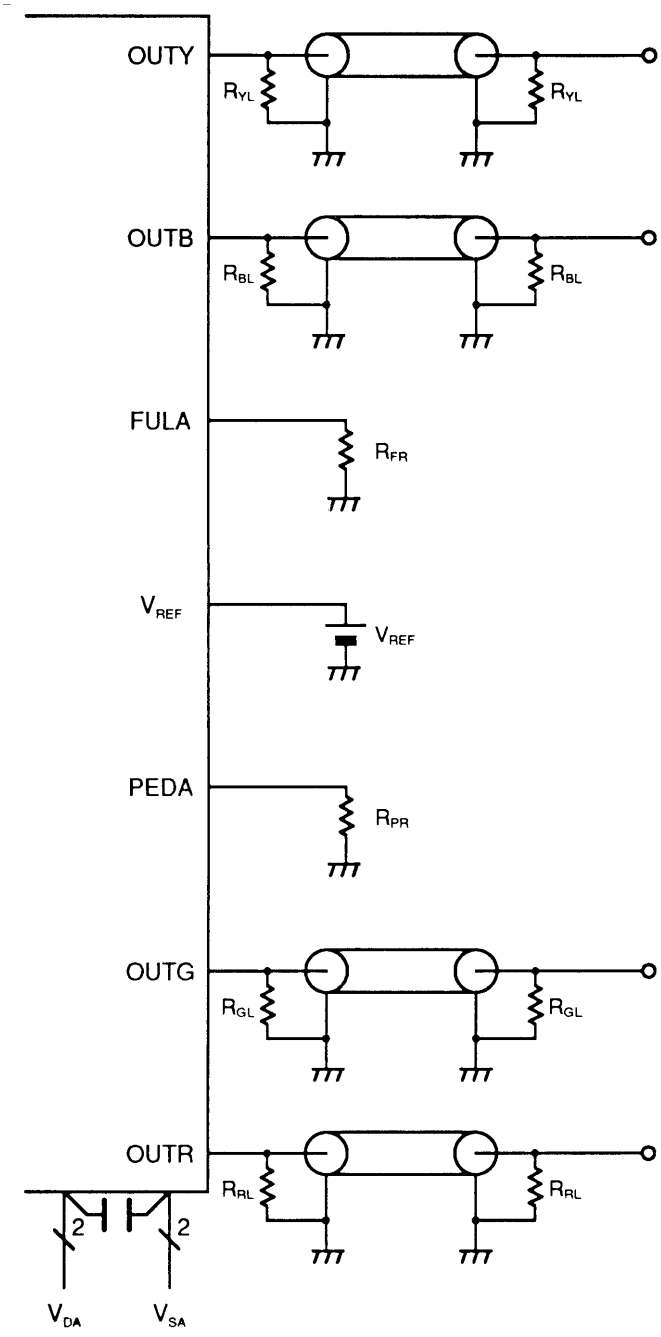


2. VRAM INTERFACE CIRCUIT EXAMPLE



EXAMPLE OF EXTERNAL CONNECTION

3. ANALOG CIRCUIT INTERFACE EXAMPLE



TEXT DISPLAY DATA

As explained in the section entitled “Explanation of Functions,” the text display data is decided after the display is determined using the TXMS, TXW2 and TXW1 signals (not synchronized with the PCLK signal).

There are eight display modes, each one of which is set by TX1, TXB, TXR and TXG signals input in synchronized timing with the PCLK signal, and the output OUTR, OUTG, OUTB and OUTY signals determined. The following table shows which mode is set by each fixed input signal, and also how the output signal changes in accordance with the synchronous input signal, in decimal form. Concerning the output voltage, please refer to the decimal values in the table and the section entitled “6. Analog Output Operation” in “Explanation of Functions.”

1. WHITE BALANCE MODES

1.1 White Balance Mode 1

TXMS = 1
TXW2 = 0 TXW1 = 0

TXI	TXB	TXR	TXG	OUTB	OUTR	OUTG	OUTY
0	0	0	0	0	0	0	0
0	0	0	1	0	0	15	12
0	0	1	0	0	15	0	2
0	0	1	1	0	15	15	14
0	1	0	0	15	0	0	1
0	1	0	1	15	0	15	13
0	1	1	0	15	15	0	3
0	1	1	1	15	15	15	15
1	0	0	0	8	8	8	11
1	0	0	1	8	8	15	15
1	0	1	0	8	15	8	11
1	0	1	1	8	15	15	15
1	1	0	0	15	8	8	11
1	1	0	1	15	8	15	15
1	1	1	0	15	15	8	11
1	1	1	1	15	15	15	15

1.2 White Balance Mode 2

TXMS = 1
TXW2 = 0 TXW1 = 1

TXI	TXB	TXR	TXG	OUTB	OUTR	OUTG	OUTY
0	0	0	0	0	0	0	0
0	0	0	1	8	8	15	15
0	0	1	0	8	15	8	11
0	0	1	1	8	15	15	15
0	1	0	0	15	8	8	11
0	1	0	1	15	8	15	15
0	1	1	0	15	15	8	11
0	1	1	1	15	15	15	15
1	0	0	1	0	0	15	12
1	0	0	1	0	0	15	12
1	0	1	0	0	15	0	2
1	0	1	1	0	15	15	14
1	1	0	0	15	0	0	1
1	1	0	1	15	0	15	13
1	1	1	0	15	15	0	3
1	1	1	1	15	15	15	15

TEXT DISPLAY DATA (continued)

1.3 White Balance Mode 3
TXMS = 1
TXW2 = 1 TXW1 = 0

TXI	TXB	TXR	TXG	OUTB	OUTR	OUTG	OUTY
0	0	0	0	0	0	0	0
0	0	0	1	0	0	15	12
0	0	1	0	0	15	0	2
0	0	1	1	0	15	15	14
0	1	0	0	15	0	0	1
0	1	0	1	15	0	15	13
0	1	1	0	15	15	0	3
0	1	1	1	15	15	15	15
1	0	0	0	4	4	4	4
1	0	0	1	4	4	15	12
1	0	1	0	4	15	4	6
1	0	1	1	4	15	15	14
1	1	0	0	15	4	4	5
1	1	0	1	15	4	15	13
1	1	1	0	15	15	4	7
1	1	1	1	15	15	15	15

1.4 White Balance Mode 4
TXMS = 1
TXW2 = 1 TXW1 = 1

TXI	TXB	TXR	TXG	OUTB	OUTR	OUTG	OUTY
0	0	0	0	0	0	0	0
0	0	0	1	4	4	15	12
0	0	1	0	4	15	4	6
0	0	1	1	4	15	15	14
0	1	0	0	15	4	4	5
0	1	0	1	15	4	15	13
0	1	1	0	15	15	4	7
0	1	1	1	15	15	15	15
1	0	0	0	4	4	4	4
1	0	0	1	0	0	15	12
1	0	1	0	0	15	0	2
1	0	1	1	0	15	15	14
1	1	0	0	15	0	0	1
1	1	0	1	15	0	15	13
1	1	1	0	15	15	0	3
1	1	1	1	15	15	15	15

2. ENHANCEMENT CHANGE MODES

2.1 Enhancement Change Mode 1
TXMS = 0
TXW2 = 0 TXW1 = 0

TXI	TXB	TXR	TXG	OUTB	OUTR	OUTG	OUTY
0	0	0	0	0	0	0	0
0	0	0	1	0	0	13	12
0	0	1	0	0	13	0	2
0	0	1	1	0	13	13	14
0	1	0	0	13	0	0	1
0	1	0	1	13	0	13	13
0	1	1	0	13	13	0	3
0	1	1	1	13	13	13	15
1	0	0	0	8	8	8	11
1	0	0	1	0	0	15	12
1	0	1	0	0	15	0	2
1	0	1	1	0	15	15	14
1	1	0	0	15	0	0	1
1	1	0	1	15	0	15	13
1	1	1	0	15	15	0	3
1	1	1	1	15	15	15	15

2.2 Enhancement Change Mode 2
TXMS = 0
TXW2 = 0 TXW1 = 1

TXI	TXB	TXR	TXG	OUTB	OUTR	OUTG	OUTY
0	0	0	0	0	0	0	0
0	0	0	1	0	0	15	12
0	0	1	0	0	15	0	2
0	0	1	1	0	15	15	14
0	1	0	0	15	0	0	1
0	1	0	1	15	0	15	13
0	1	1	0	15	15	0	3
0	1	1	1	15	15	15	15
1	0	0	0	8	8	8	11
1	0	0	1	0	0	13	12
1	0	1	0	0	13	0	2
1	0	1	1	0	13	13	14
1	1	0	0	13	0	0	1
1	1	0	1	13	0	13	13
1	1	1	0	13	13	0	3
1	1	1	1	13	13	13	15

2. ENHANCEMENT CHANGE MODES (continued)

2.3 Enhancement Change Mode 3

TXMS = 0
TXW2 = 1 TXW1 = 0

TXI	TXB	TXR	TXG	OUTB	OUTR	OUTG	OUTY
0	0	0	0	0	0	0	0
0	0	0	1	0	0	11	8
0	0	1	0	0	11	0	2
0	0	1	1	0	11	11	10
0	1	0	0	11	0	0	1
0	1	0	1	11	0	11	9
0	1	1	0	11	11	0	3
0	1	1	1	11	11	11	11
1	0	0	0	8	8	8	11
1	0	0	1	0	0	15	12
1	0	1	0	0	15	0	2
1	0	1	1	0	15	15	14
1	1	0	0	15	0	0	1
1	1	0	1	15	0	15	13
1	1	1	0	15	15	0	3
1	1	1	1	15	15	15	15

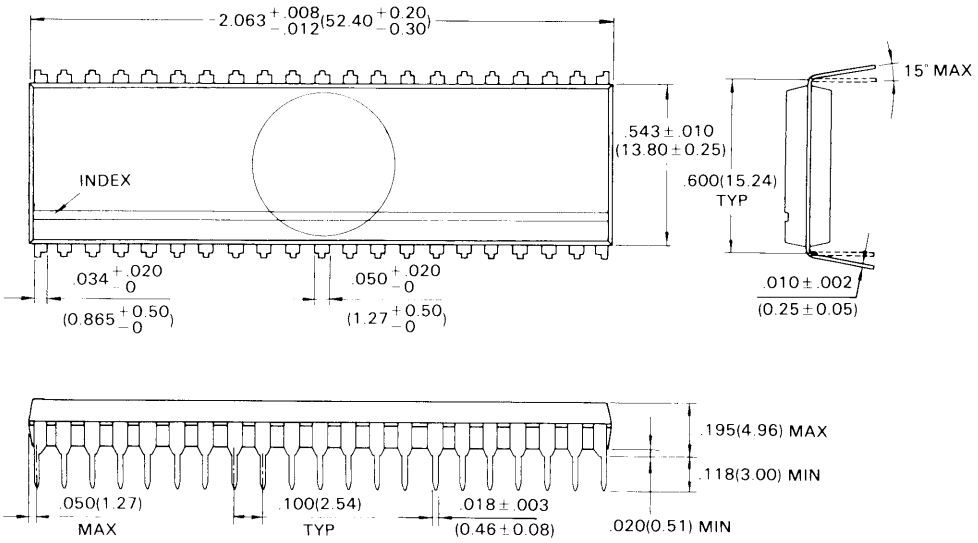
2.4 Enhancement Change Mode 4

TXMS = 0
TXW2 = 1 TXW1 = 1

TXI	TXB	TXR	TXG	OUTB	OUTR	OUTG	OUTY
0	0	0	0	0	0	0	0
0	0	0	1	0	0	15	12
0	0	1	0	0	15	0	2
0	0	1	1	0	15	15	14
0	1	0	0	15	0	0	1
0	1	0	1	15	0	15	13
0	1	1	0	15	15	0	3
0	1	1	1	15	15	15	15
1	0	0	0	8	8	8	11
1	0	0	1	0	0	11	6
1	0	1	0	0	11	0	2
1	0	1	1	0	11	11	10
1	1	0	0	11	0	0	1
1	1	0	1	11	0	11	9
1	1	1	0	11	11	0	3
1	1	1	1	11	11	11	11

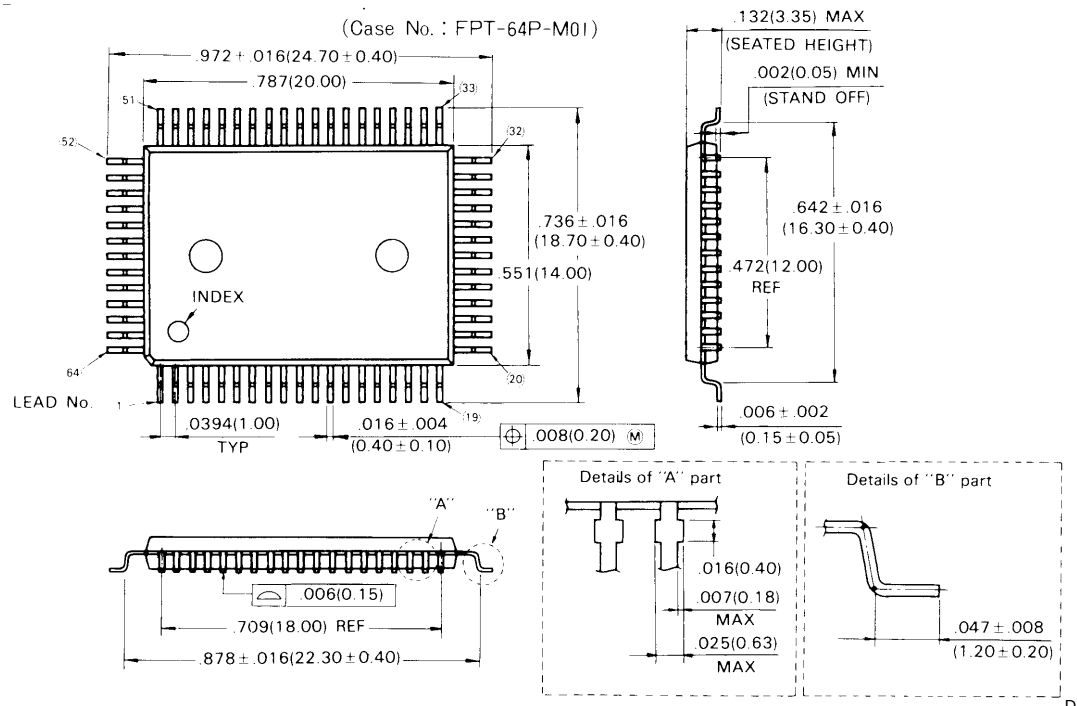
PACKAGE DIMENSIONS

42-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-42P-M01)



Dimensions in
inches (millimeters)

64-LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT-64P-M01)



Dimensions in
inches (millimeters)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg., 6-1, Marunouchi 1-chome
Chiyoda-ku, Tokyo 100 Japan
Tel: (03) 216-3211
Telex: 781-2224361
Fax: (03) 321 6-9771

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804 USA
Tel: 408-922-9000
Fax: 408-432-9044

Europe

FUJITSU MIKROELEKTRONIK GmbH
Arabella Centre 9. OG
Lyoner Strasse 44-48
D-6000 Frankfurt 71
Federal Republic of Germany
Tel: (069) 66320
Telex: 441963
Fax: (069) 6632122

Asia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
#06-04 to #06-07
Plaza By The Park
No. 51 Bras Basah Road
Singapore 0718
Tel: 336-1600
Telex: 55573
Fax: 336-1609

Printed in Japan JV0093-90XA1