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FUJITSU

DATA SHEET

MB1520/MB1530/MB1540/MB1550 SERIES Bi–CMOS LSI RF IC SPECIFICATION

ADVANCED SEMICUSTOM TECHNOLOGY OF SUPER PLL WITH RF SYSTEM ON LSI

The Fujitsu MB1520/1530/1540/1550 series are semicustom LSI IC's based on a master slice method. Super PLL (PLL and Prescaler) macros and high frequency analog macros, such as VCO's. IF amplifiers , RF amplifiers and mixers can be realized on a single chip in accordance with customer requests. This is achieved by means of predefined blocks (Super PLL's and analog macros) laid out on the respective frames in a number of different combinations. The performance of each block is custom specified.

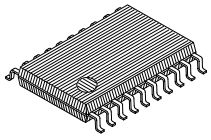
The MB1520/1530/1540/1550 series makes it possible to compose single chip silicon front ends for mobile communication systems. Due to the design process used, development cycles and cost are greatly reduced over standard full custom LSI designs, resulting in lower system cost solutions and reduced time-to-market.

Features

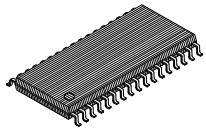
- Super PLL's as well as high frequency analog circuits, such as VCO's, mixers, RF and IF amplifiers.
- Four available frame sizes, offering various combinations of Super PLL's and analog macros.
- Choice of a wide variety of existing Super PLL's and analog functions, as well as custom specifications of the same.
- Choice of power supply voltages between 2.7V and 5.5V. (Minimum 2.0V with some restrictions available.)
- Available high speed lock up circuit for digital mobile communications such as DECT, GSM, PDC, and so on.
- A number of standard features, such as power saving modes, phase shifter circuit, analog switches, charge pumps, depending on the frame size.
- Development cycle is typically 14 weeks.

Application Examples

- MB1520 series: BS tuner, car navigation systems
- MB1530 series: MCA wireless for business use, analog cordless phones
- MB1540 series: Analog cellular phones, trunked radios
- MB1550 series: Digital cellular and digital cordless phones



FPT-20P-M03



FPT-34P-M01

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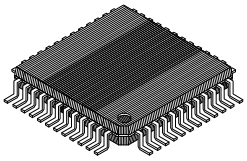
FPT-34P-M03



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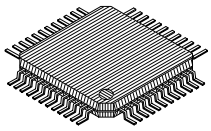

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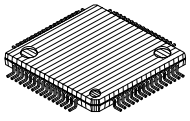


FPT-64P-M03

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Bi–CMOS LSI RF IC SERIES

Master-slice methodology is that wafers of a particular frame are prefabricated as much as having finished diffusion processes, forming the basic elements, such as transistors, resistors and capacitors. The remaining contact and wiring process steps then determine and configure the function and value of each element according to cases.

This series is based on a master-slice method for which predefined blocks are laid out. Four series, MB1520/1530/1540/1550 are available in accordance with combinations of the predefined blocks. (Please refer to “Chip Layout”.) Table 1 shows representative blocks and features of each series.

Table 1. SERIES

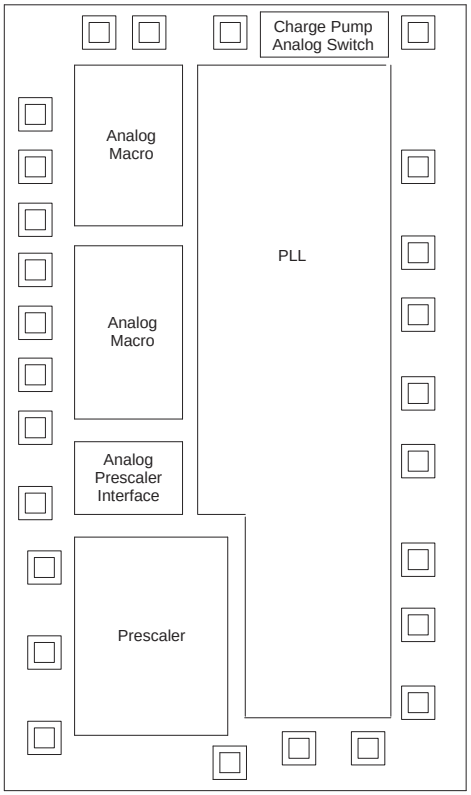
Series Name	Prescaler	PLL	Analog Macro	Operating Frequency (max.)	Package		
					SSOP	QFP	SQFP
MB1520	1 circuit	1 circuit	2 circuits	2.4GHz	20-pin	–	–
MB1530	2 circuits	2 circuits	4 circuits	1.9GHz	34-pin	–	–
MB1540	2 circuits	2 circuits	6 circuits	2.4GHz	–	48-pin	48-pin
MB1550	3 circuits*	3 circuits	8 circuits	2.4GHz	–	48-pin	64-pin

* 1 Prescaler or 90° phase shifter

CHIP LAYOUT

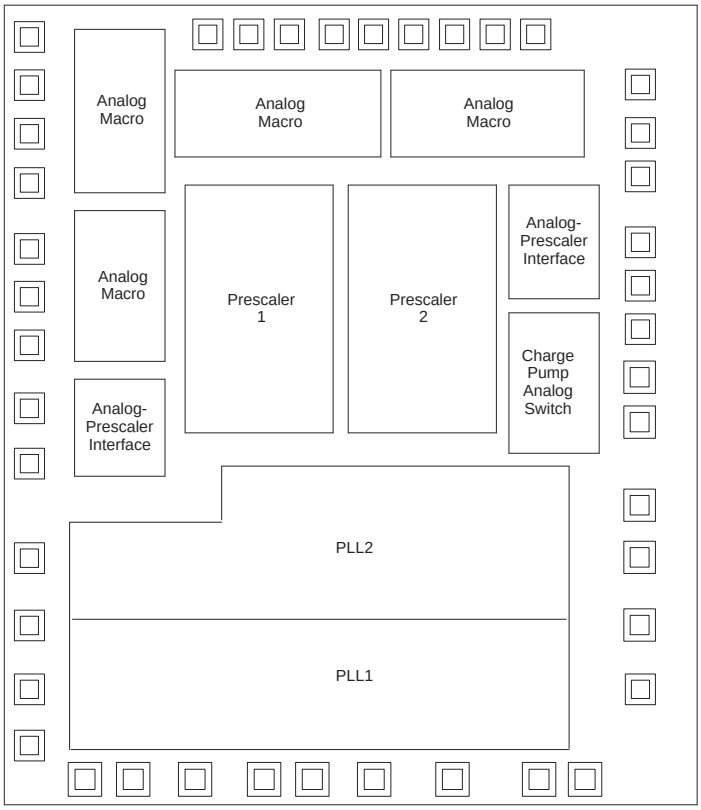
MB1520 Series

1 Prescaler
1 PLL
2 Analog Macros



MB1530 Series

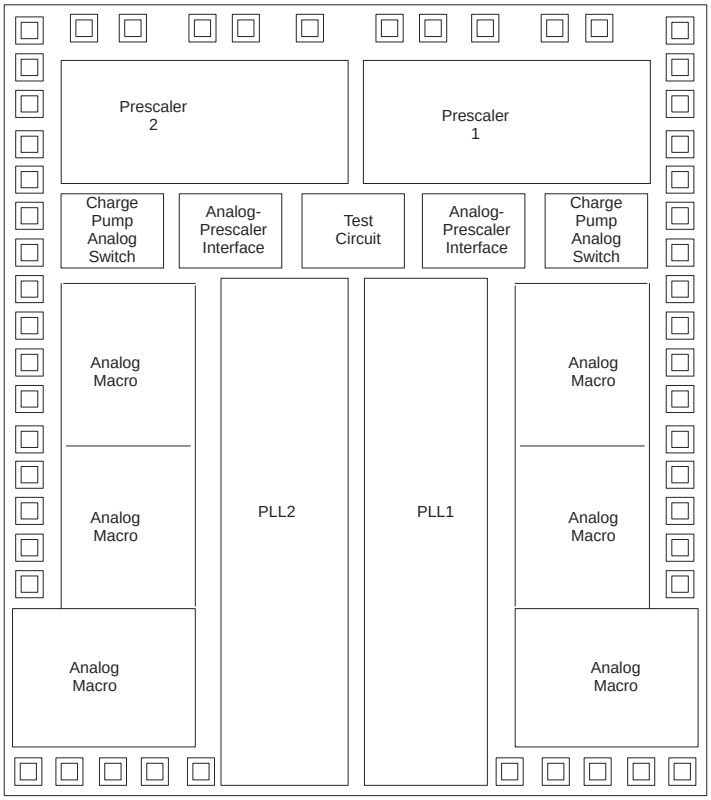
2 Prescaler
2 PLL
4 Analog Macros



CHIP LAYOUT (Continued)

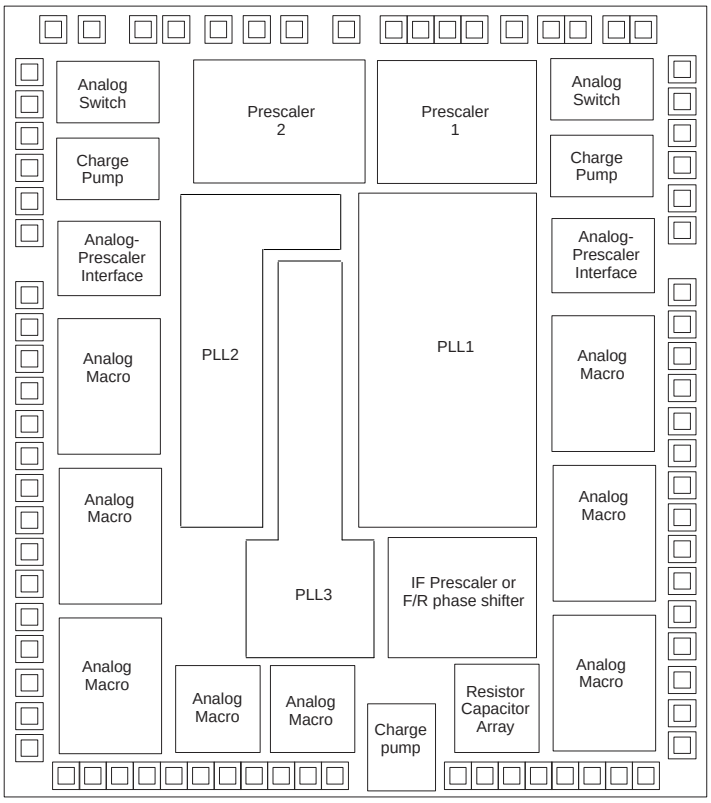
MB1540 Series

2 Prescaler
2 PLL
6 Analog Macros



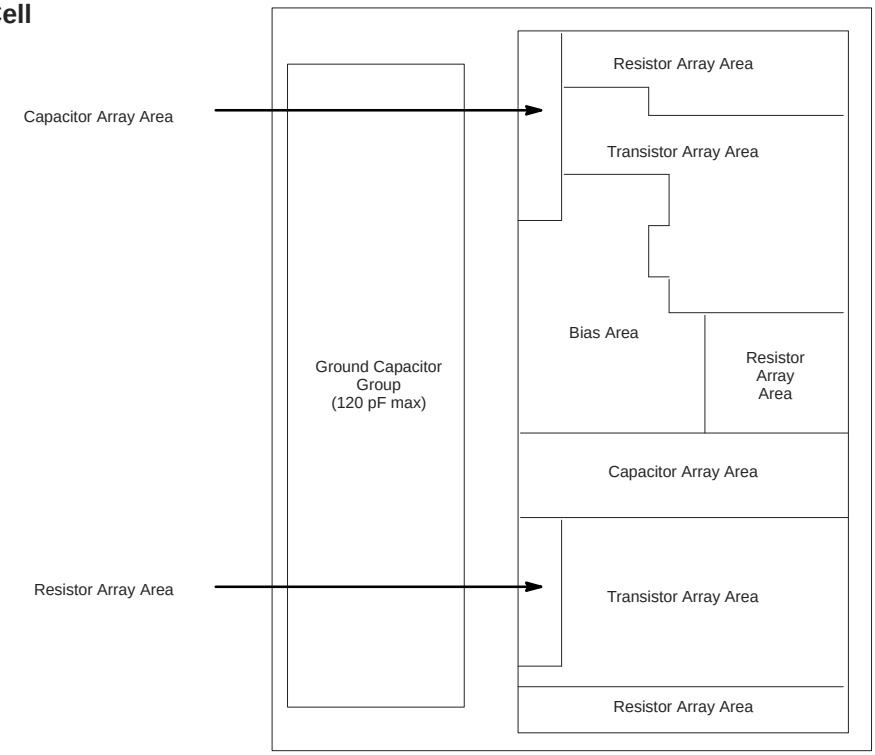
MB1550 Series

2 Prescaler
3 PLL
8 Analog Macros
1 Prescaler or
90° phase shifter



CHIP LAYOUT (Continued)

Analog Cell



ABSOLUTE MAXIMUM RATINGS

(Reference voltage is GND.)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Output Voltage	I_{OUT}	±10	mA
Ambient Temperature	T_{STG}	–50 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

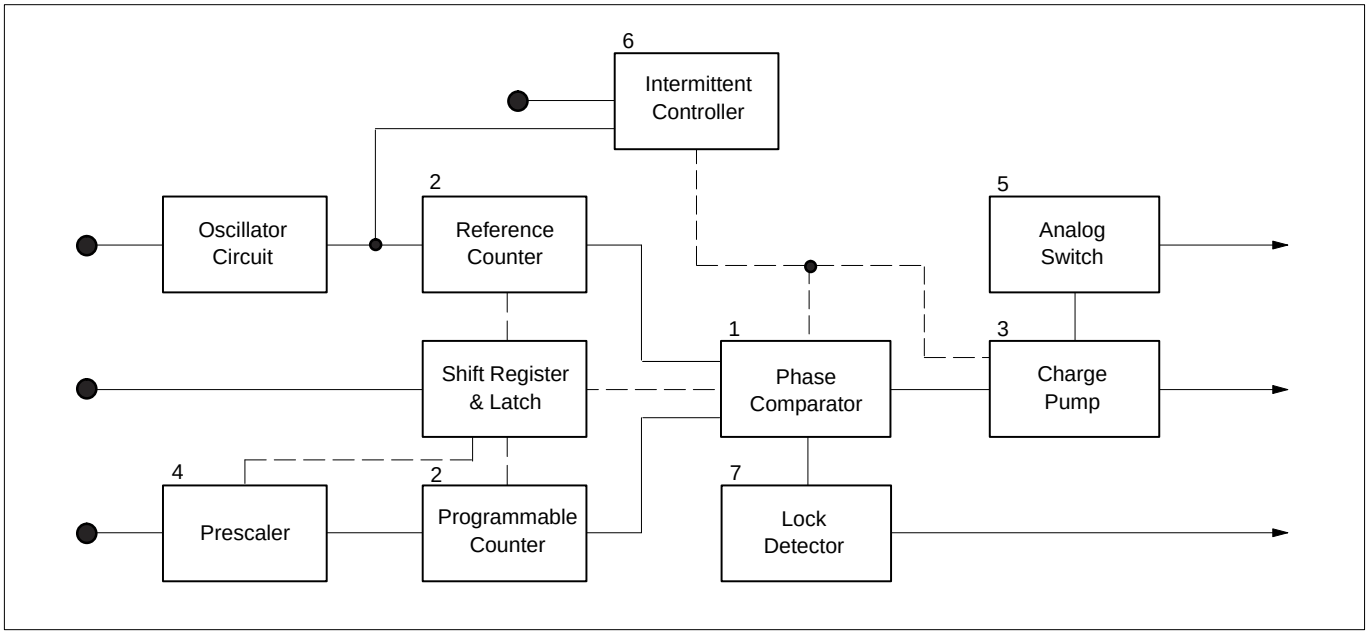
(Reference voltage is GND.)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	2.7*		5.5	V
	GND		0		V
Ambient Temperature	T_A	–40		+85	°C

* The minimum operating voltage is at 2.0V, but some restriction may be required.

MACRO CELLS DESCRIPTIONS

1. Super PLL (PLL and Prescaler)



1.1 Functional Descriptions

In designing “super PLL block”, some functions may be restricted depending on kind of series (MB1520/1530/1540/1550). Availability of main functions is summarized in Table 2.

1. Phase comparator

Phase difference detection range is –2π (pi) to +2π (pi). In order to minimize the dead zone area, the phase comparator is designed to deliver a minimum signal to the charge pump even when the phase difference is zero. Also, it is possible to choose the characteristics of the phase comparator to meet polarity of VCO.

2. Counter (Reference Counter and Programmable Counter)

Two types of counters are available for PLL1 and PLL2 of all series : programmable and fixed
Regarding PLL3, one type of counter is available : Fixed

3. Charge pump

All charge pumps are based on bipolar technology. Their voltage levels at “H” depend on the power supply voltage chosen. It is possible to optimize charge pump characteristics individually according to customer needs.

– High speed lock up circuit
This circuit is an option to further increase the lock up time of the PLL, and is available for PLL1 and PLL2 (except PLL3). It will mainly be required in the new emerging digital communication standards.

4. Prescaler

Divide ratio can be chosen freely, so can two modulus type and fixed type. However, regarding PLL3, only fixed type is available and the divide ratio can be chosen from 1/2, 1/4, and 1/8.

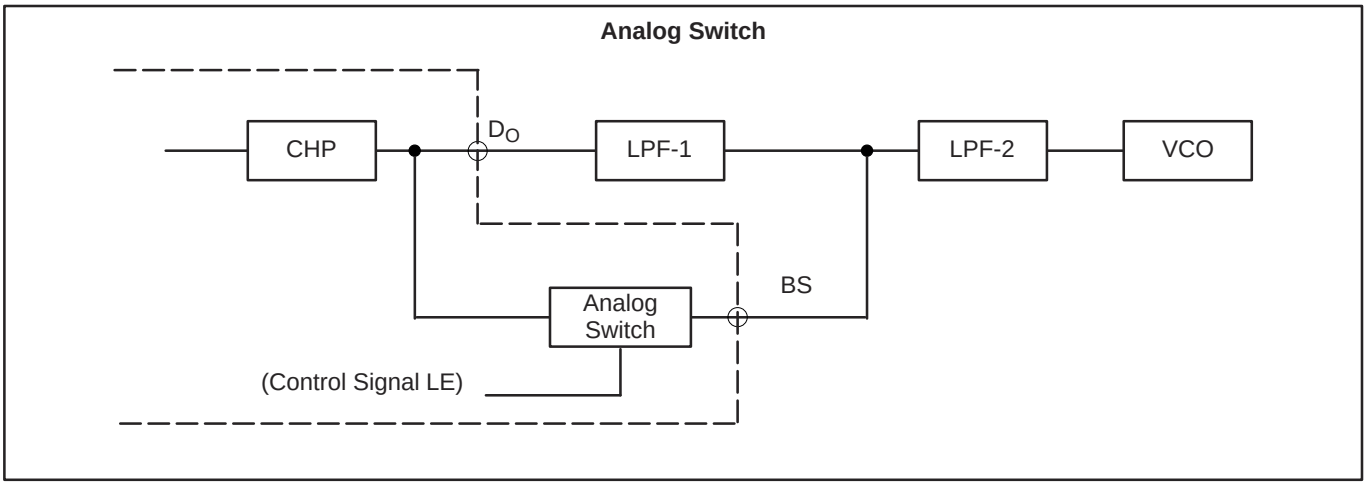
Table 2. SUPER PLL FUNCTION TABLE

		Prescaler	Programmable Counter	Reference Counter	High Speed Lock Up Function	Power Save Mode
MB1520	PLL1	T	P/F	P/F	X	X
MB1530	PLL1	T	P/F	P/F*	X	X
	PLL2	T	P/F		–	–
MB1540	PLL1	T	P/F	P/F	X	X
	PLL2	T	P/F	P/F	–	X
MB1550	PLL1	T	P/F	P/F	X	X
	PLL2	T	P/F	P/F	X	X
	PLL3	S	F	F	–	X

NOTE: T: Two Modulus S: Single Modulus (1/2, 1/4, or 1/8) P/F: Programmable or Fixed F: Fixed X: Available
*: Common for PLL1 and 2

5. Analog switch

This switch is controlled by the LE signal. When LE is at “H”, the analog switch is closed (ON). In this mode, the charge pump output (D_O) is fed in parallel to the pin BS. This decreases the time constant of the loop filter and reduces the charge pump load. The result is an increased lock up speed.



6. Intermittent operation control circuit

The intermittent operation reduces the power consumption by powering down or waking up parts of the PLL circuitry. All the transmission, the reception and IF block PLL may be controlled by this circuit.

If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between the reference frequency (fn) and the comparison frequency (fp) and may in the worst case take longer time for lock up of the loop.

To prevent this, the intermittent operation control circuit forces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

The circuit can be controlled externally or internally, depending on customer requirements. If controlled externally, the circuit is activated by an external signal to the PS pin. If controlled internally, the intermittent control circuit follows the power state set by the analog cells. When the power supply for the analog cells is shut down, the stand by state is automatically selected. When the analog cells are supplied with power, the active state is selected.

The charge pump output is in a high impedance state during stand by, so that the VCO control voltage is being clamped at the active state level.

During the stand by state, the latches store the data which they hold at the time of power down. The shift register data, on the contrary, may be renewed during stand by.

NOTE: Powering up for the digital blocks (V_{CCRD}, V_{CCTD}), (after they are disconnected) has to be done in stand by mode.

Table 3. STANDARD STAND BY STATE OF PLL BLOCK

		Circuit State	
		Active Mode	**Stand By Mode**
Rx	Reception circuits	X	PD
	Oscillator circuit	X	X*
	Reference counter	X	–
Tx	Transmission circuits	X	PD
	Oscillator circuit	X	X
	Reference counter	X	–
IF	IF circuits	X	PD
	Oscillator circuit	X	X
	Reference counter	X	–

NOTE: X: Active state PD: Power down mode –: Stop working
*: Oscillator circuit can be stopped in accordance with PK's PD signal.

7. Lock detector circuit

LD output is selected by setting the “T” bit. (See 1.2 Serial data format.)
When the phase difference is equal or higher than tw (see diagram below), LD goes into “L”. When the phase difference is tw or less and continues to be so for three cycles or more, the LD goes into “H”. For example, in case of a 12.8MHz oscillator frequency tw, is 625ns to 1250ns. The relation between LD and PLL circuit is shown in Table 4.

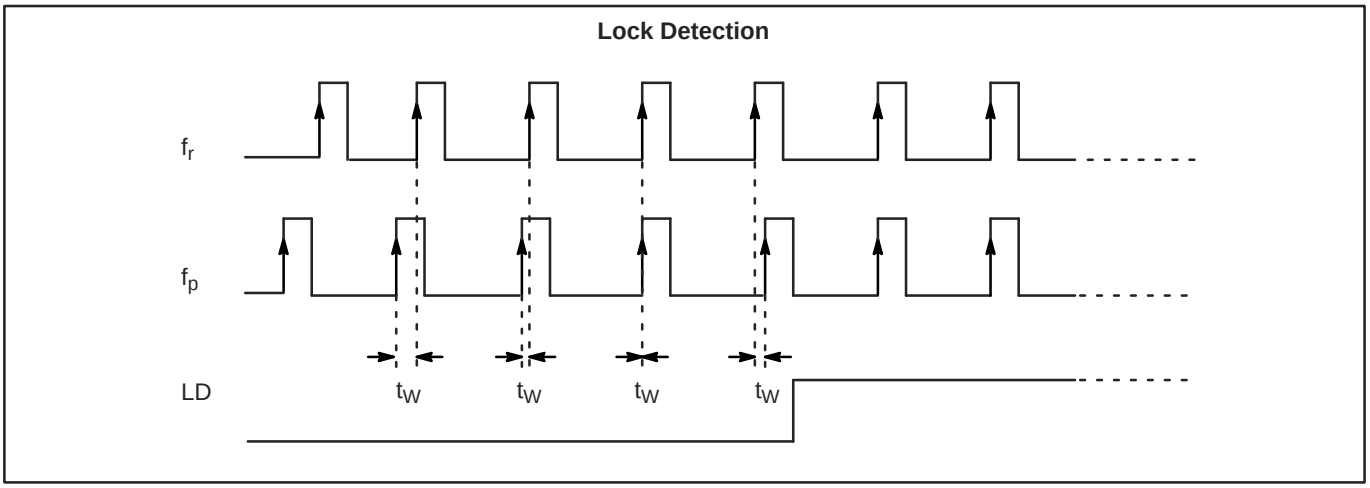


Table 4. RELATIONSHIP BETWEEN LD SIGNAL AND THE CIRCUIT STATE

Operation Mode	PLL circuit	LD Output
Stand-by	Stand-by	L
Active	Unlock	L
	Lock	H

1.2 Serial Data Format

The PLL operation is controlled by serial data inputs. The parameters of the serial data are shown below. The data input starts with the MSB bit. The data length may vary between 22 and 37 bits. The actual data format is being worked out with the customer.

Table 5. SERIAL DATA FORMAT

Name		Function	Typical Bit Number
Control Bit (CNT bit)		Selects direction of data transfer (Rx or Tx)	1 to 2
LD Select Bit (T bit)		Selects the LD output	1 to 2
FC Bit (F bit)		Switches phase of the comparator	1
Programmable Counter Bit (N bit)		Sets programmable counter’s divide ratio	11
Swallow Counter Bit (A bit)		Sets swallow counter’s divide ratio	7
Reference Counter Bit (R bit)	Fixed	Sets reference counter’s divide ratio	1 to 2
	Programmable	Sets reference counter’s divide ratio	14

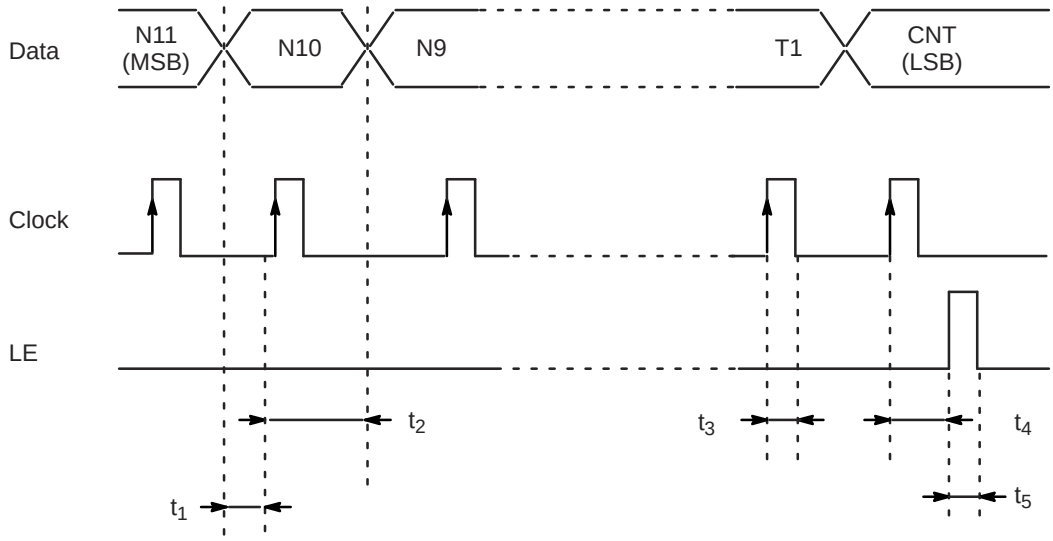
1.3 Serial Data Input Timing

Binary data is entered using the Data, Clock, and LE pins. The serial data separately controls the programmable reference divider as well as the programmable divider.

Each data bit is shifted into the internal shift register at the rising edge of each clock pulse. When the LE pin is “H”, stored data is transferred from the shift register into the latch, chosen by the control bit. A schmitt trigger at each input improves noise immunity.

NOTE: 1. One clock pulse always shifts one data bit into the shift register, even during stand by state.
2. Input voltages (Data, Clock, and LE pins) should always be lower than Vcc.

Serial Data Input Timing



t1: Data set up time (≥ 1 μsec)
t2: Data hold time (≥ 1 μsec)
t3: Clock pulse width (≥ 1 μsec)
t4: LE set up time to the rising edge of the last clock (≥ 1 μsec)
t5: LE pulse width (≥ 1 μsec)

Notes: 1. One bit of data is shifted into the shift register on the rising edge of the clock (edge trigger).
2. Data in the shift register is transferred to the latch when LE becomes H.

2. Mixer, IF Amplifier

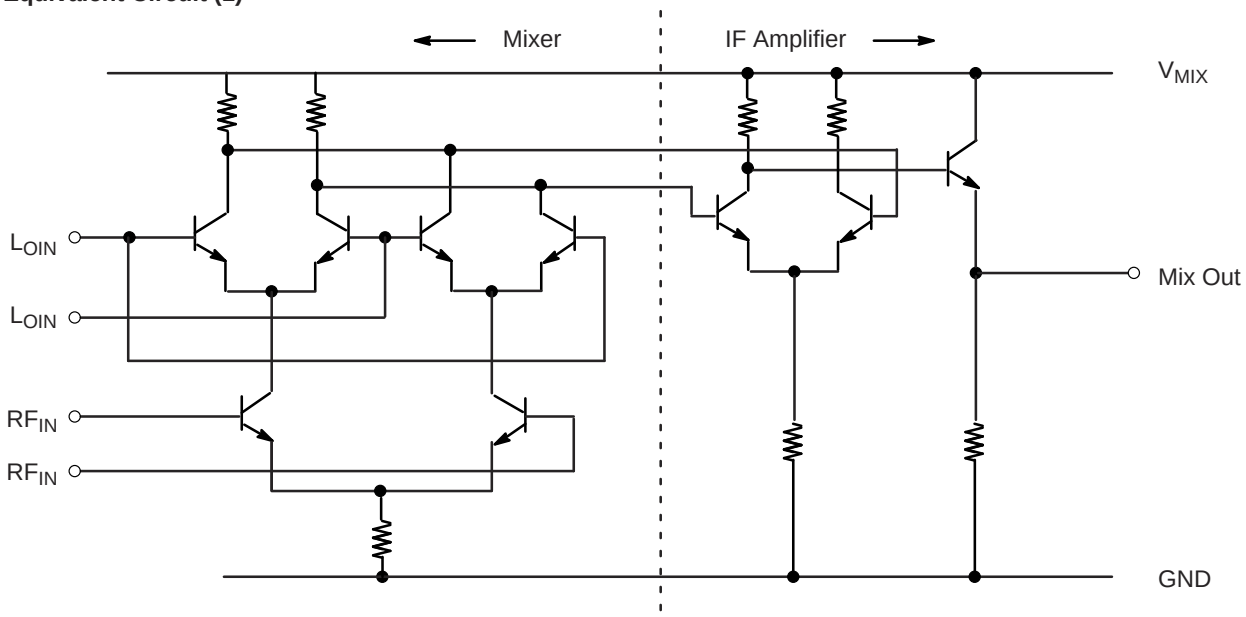
Some basic examples for achievable circuits are shown below. However, concerning circuitry and performance, it is possible to configure each analog macro cell to customer requirements.

2.1 Basic Construction

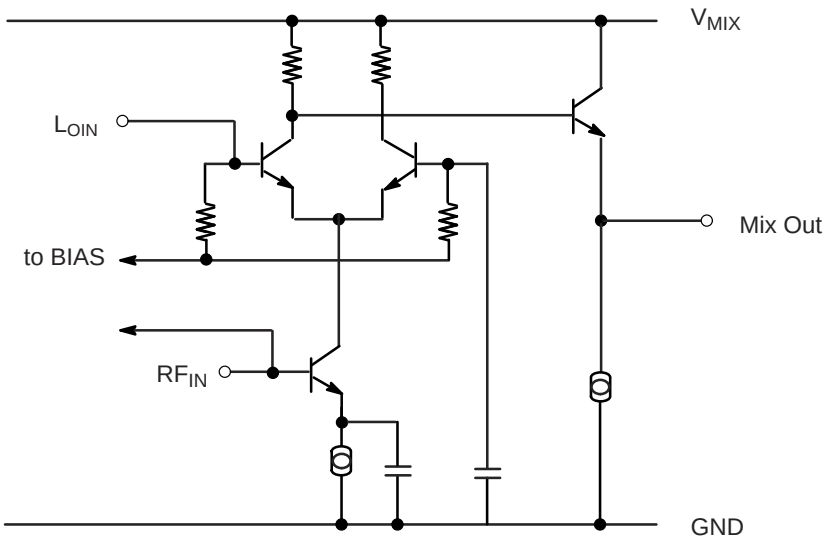
Mixer circuit can either be of DBM (Doubled Balanced Mixer) or SBM (Single Balanced Mixer) type. LO and RF inputs can be connected with the internal bias circuit, if necessary. The mixer output is connected with its own power supply (V_{MIX}) via a load resistor, then connected with the following IF amplifier.

The IF amplifier consists of a differential amplifier and NPN transistor, which forms the emitter follower output.

Basic Equivalent Circuit (1)



Basic Equivalent Circuit (2)

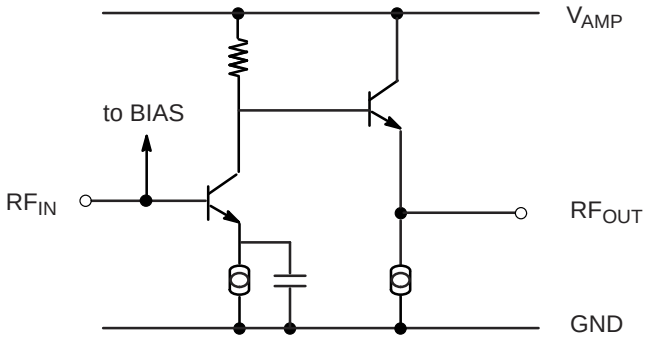


3. RF Amplifier

3.1 Basic Construction

The output signal from the common emitter circuit will be supplied though an emitter follower.

Basic Equivalent Circuit

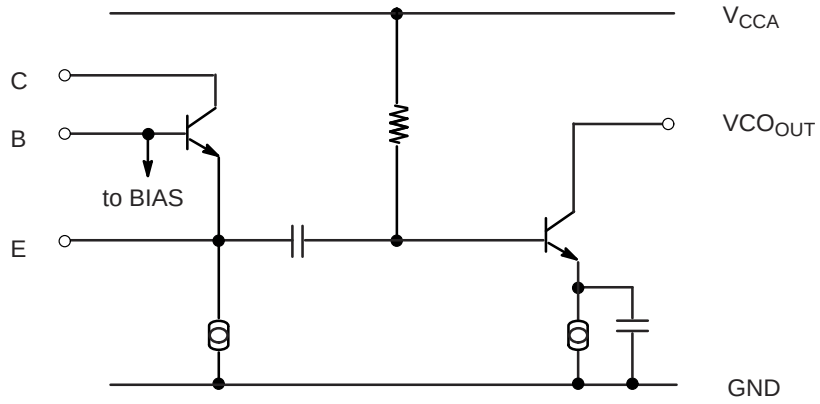


4. VCO

4.1 Basic Construction

The VCO circuit consists of an output buffer transistor and an oscillation transistor, which construct a base grounded colpitts circuit. Resonator and varicap can't be integrated in the chip, so they need to be connected externally.

Basic Equivalent Circuit



EXAMPLES OF AN ANALOG CIRCUIT'S BASIC CHARACTERISTICS

VCO

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	4.5		5.5	V	
Current Consumption		6		mA	
Operating Frequency			400	MHz	
C/N		70		dB	Offset frequency = 25kHz, BW = 15kHz
S/N		50		dB	
Output Power		–5		dBm	
Mod Sense		3		MHz/V	

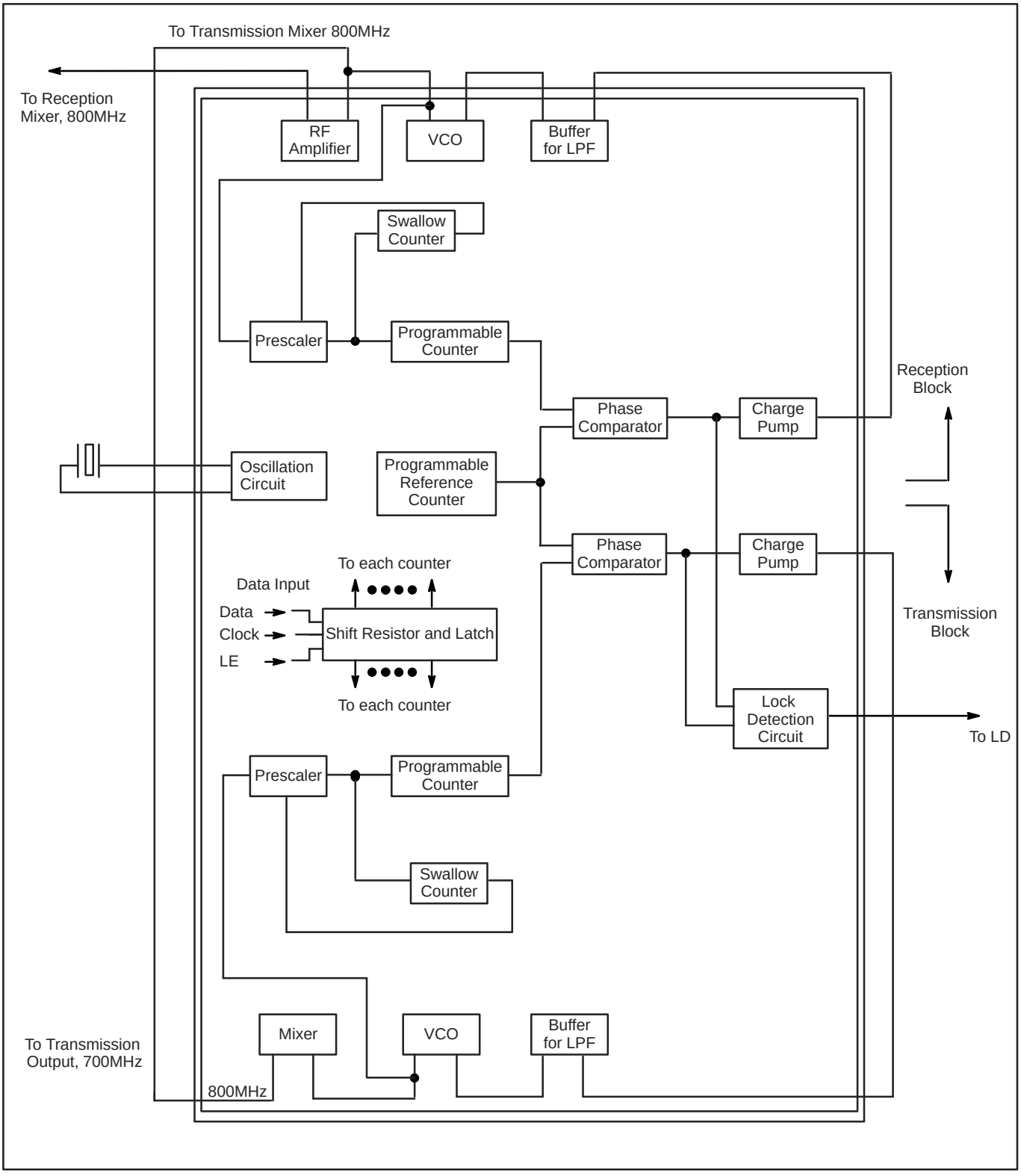
Mixer

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	4.5		5.5	V	
Current Consumption		6		mA	
Gain		13		dB	
Maximum Output Power		–5		dBm	
1 dB Compresssion Point		–10		dBm	Output level
Intercept Point		–16		dBm	Input level
Noise Figure		10		dB	DSB measurement
RF-L_O Isolation		20		dB	

Amplifier

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	4.5		5.5	V	
Current Consumption		6		mA	
Operating Frequency		400		MHz	
Gain		20		dB	f = 400MHz (small signal input)
Maximum Output Power		–3		dBm	f = 400MHz
1 dB Compresssion Point		–10		dBm	f = 400MHz, Output level
Intercept Point		–19		dBm	f = 400MHz, 400.1MHz, Input level
Noise Figure		3		dB	f = 400MHz

MB1540 APPLICATION CIRCUIT EXAMPLE



DEVELOPMENT PROCEDURE

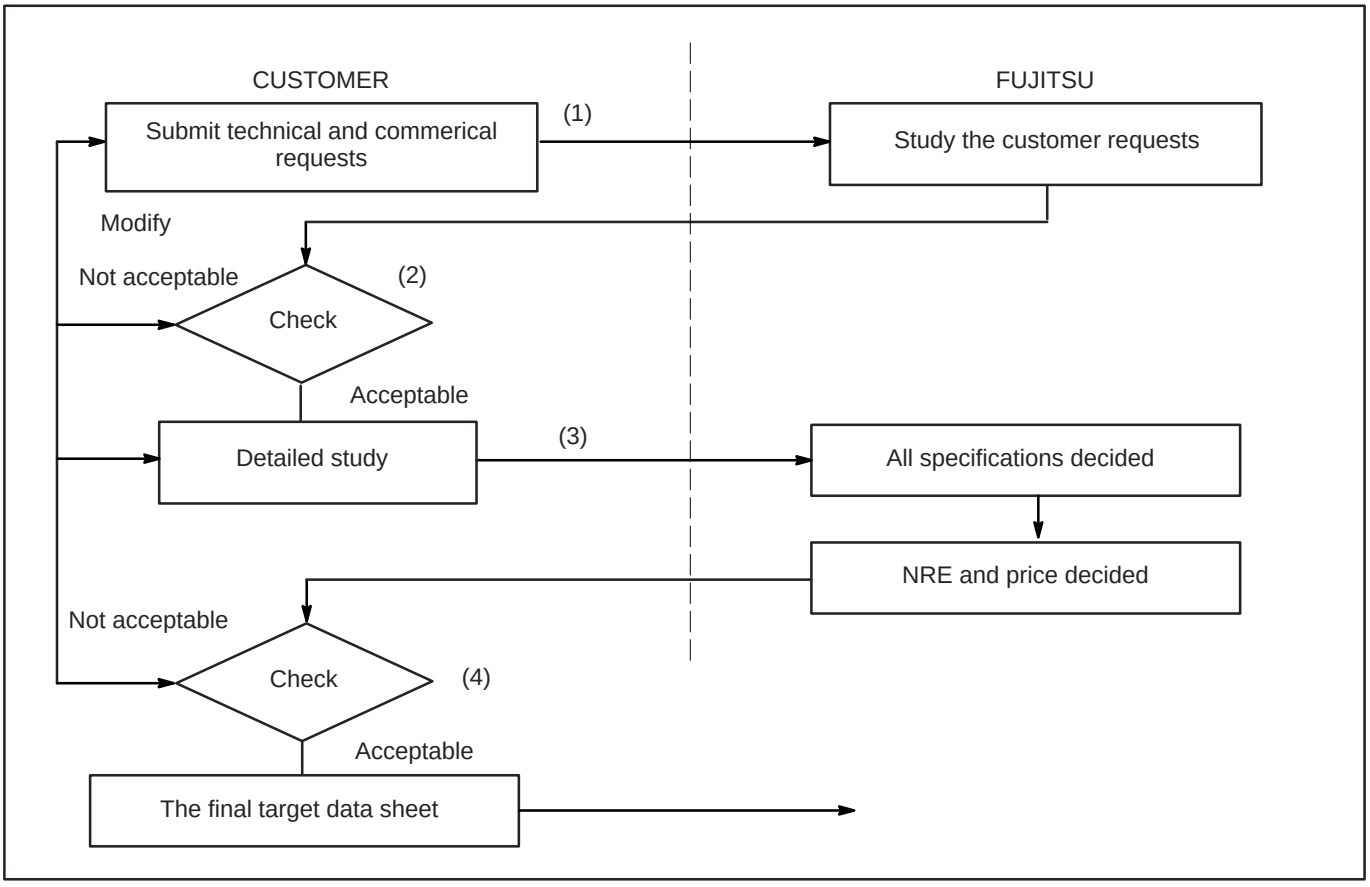
1. Study about product development

(1) The customer submits technical and commercial requests to Fujitsu. Fujitsu reviews the customer requirements, if necessary simulation is done.
[Technical request]
Function: Functional descriptional material, I/O signal descriptional material, Block diagram, etc.
Specifications: Prescaler, PLL, VCO, Mixer, Amplifier, etc.
[Commercial request]
Delivery and price: Development schedule, development assignment plan, demand, NRE, target price, etc.

(2) Fujitsu submits a counter proposal. And the final target specification evolves from the discussions about proposal/counter proposals between the customer and Fujitsu.

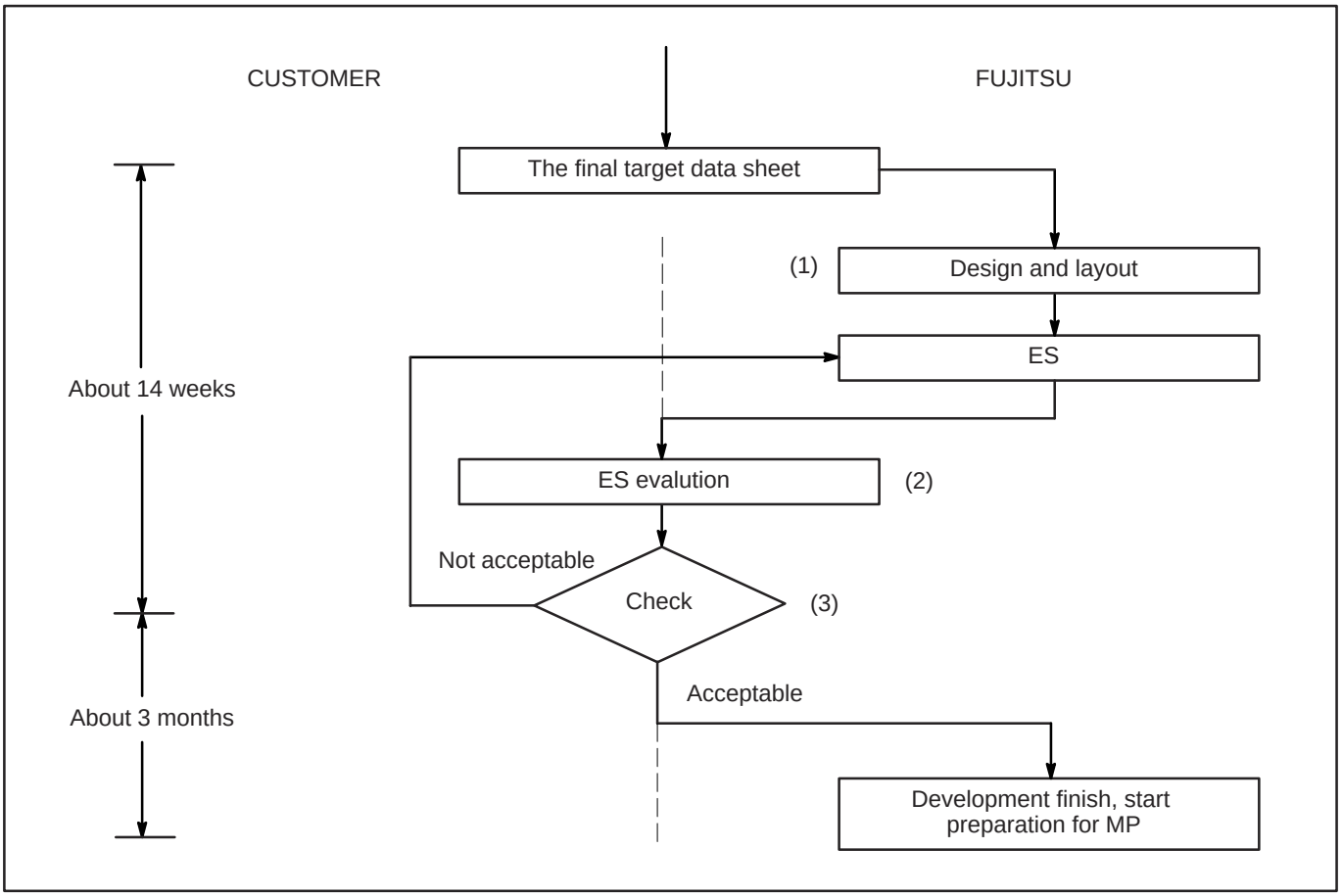
(3) Detailed circuit and test specifications are studied. Then all of the specifications are decided. After that development schedule, NRE, quotation are estimated formally.

(4) After the customer and Fujitsu agree to develop the device, the final specification (data sheet) is submitted to the customer to confirm the specification.



2. Development of IC

(1) Design and layout of the chip starts. First engineering samples become available approximately 14 weeks after the final target data sheet is issued.
(2) ES is evaluated by the customer and Fujitsu.
(3) The final specification sheet of finished product is submitted to the customer from Fujitsu when the customer is satisfied with evaluation result. Then, preparation for mass production is started. Typically 3 months are necessary for the first shipment from when the final specification sheet (for finished products) is issued.



TARGET SPECIFICATION BLANK

MB1520 Series

Parameter		Symbol	Request Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Current		I_{CCD}				mA	Digital section
		I_{CCA}				mA	Analog section
Power Supply Voltage		V_{CCO}				V	Digital section (PLL, Prescaler)
		V_{CCA}				V	Analog section (VCO)
VCO	Operating Frequency Range	f_{VCO}				MHz	
	Output Power	P_{OUT}				dBm	
	C/N Ratio	C/N				dB	Detuning Δ f :_____kHz Bandwidth: _____kHz
	S/N Ratio	S/N				dB	Reference deviation:_____kHz/dev Bandwidth: _____kHz to _____kHz
	Mod Sense	Δf_{VCO}				MHz/V	Control voltage V_T:_____ to_____V
RF-Amp	Operating Frequency Range	f_{AMP}				MHz	
	Gain	Gain				dB	
	Noise Figure	NF				dB	
	Intercept Point	IP_3				dBm	Input level
	1 dB Compression Point	CP				dBm	Output level
	In-out Isolation	I_{SO}				dB	

MB1520 Series (Continued)

Parameter		Symbol	Request Value			Unit	Note
			Min.	Typ.	Max.		
Mixer	Operating Frequency	f_{RF}				MHz	
		f_{LO}				MHz	
		f_{IF}				MHz	Output frequency
	Gain	GAIN				dB	
	Noise Figure	NF				dB	Measurement method; SSB or DSB measurement value
	Intercept Point	IP_3				dBm	Input level
	1 dB Compression Point	CP				dBm	Output level
	LO-RF Isolation	I_{SO}				dB	
PLL	Oscillation Frequency	f_{OSC}				MHz	Comparison frequency: f_r = _____kHz
	Lock-up Time	T_{LR}				ms	Step frequency: Δf = _____kHz
Memo:							

* If you have any questions, please fill in the above “Memo” column.

Customer name:

Application:

ES request day:

CS request day:

Planning quantity:

TARGET SPECIFICATION BLANK

MB1530/MB1540 Series

Parameter		Symbol	Request Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Current		I_{CCR}				mA	Reception section
		I_{CCT}				mA	Transmission section
Power Supply Voltage		V_{CCD}				V	Digital section (PLL, Prescaler)
		V_{CCA}				V	Analog section (VCO)
TX-VCO	Operating Frequency Range	f_{VCO}				MHz	
	Output Power	P_{OUT}				dBm	
	C/N Ratio	C/N				dB	Detuning Δ f :_____kHz Bandwidth: _____kHz
	S/N Ratio	S/N				dB	Reference deviation:_____kHz/dev Bandwidth: _____kHz to _____kHz
	Mod Sense	Δf_{VCO}				MHz/V	Control voltage V_T:_____ to_____V
RX-VCO	Operating Frequency Range	f_{VCO}				MHz	
	Output Power	P_{OUT}				dBm	
	C/N Ratio	C/N				dB	Detuning Δ f :_____kHz Bandwidth: _____kHz
	S/N Ratio	S/N				dB	Reference deviation:_____kHz/dev Bandwidth: _____kHz to _____kHz
	Mod Sense	Δf_{VCO}				MHz/V	Control voltage V_T:_____ to_____V
RF-Amp	Operating Frequency Range	f_{AMP}				MHz	
	Gain	Gain				dB	
	Noise Figure	NF				dB	
	Intercept Point	IP_3				dBm	Input level
	1 dB Compression Point	CP				dBm	Output level
	In-out Isolation	I_{SO}				dB	

MB1530/MB1540 Series (Continued)

Parameter		Symbol	Request Value			Unit	Note	
			Min.	Typ.	Max.			
Mixer	Operating Frequency	f_{RF}				MHz		
		f_{LO}				MHz		
		f_{IF}				MHz	Output frequency	
	Gain	GAIN				dB		
	Noise Figure	NF				dB	Measurement method; SSB or DSB measurement value	
	Intercept Point	IP_3				dBm	Input level	
	1 dB Compression Point	CP				dBm	Output level	
	LO-RF Isolation	I_{SO}				dB		
PLL	Oscillation Frequency	f_{OSC}				MHz	Comparison frequency: f_r = _____kHz	
	Lock-up Time	T_{LR}				ms	Reception	Step frequency; Δf = _____kHz
		T_{LT}				ms	Transmission	
Memo:								

* If you have any questions, please fill in the above “Memo” column.

Customer name:

Application:

ES request day:

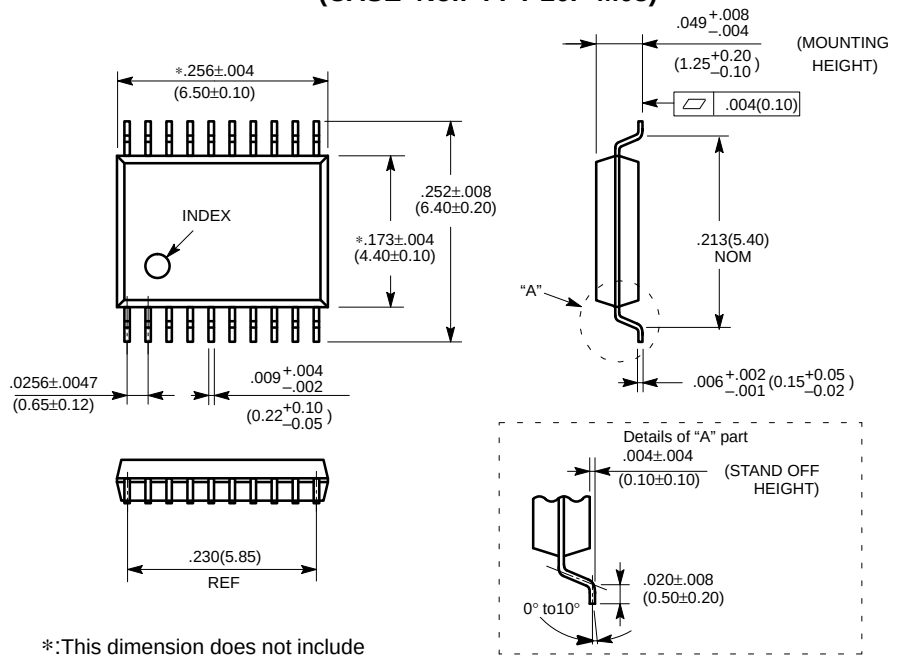
CS request day:

Planning quantity:

PACKAGE DIMENSIONS

MB1520 Series

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



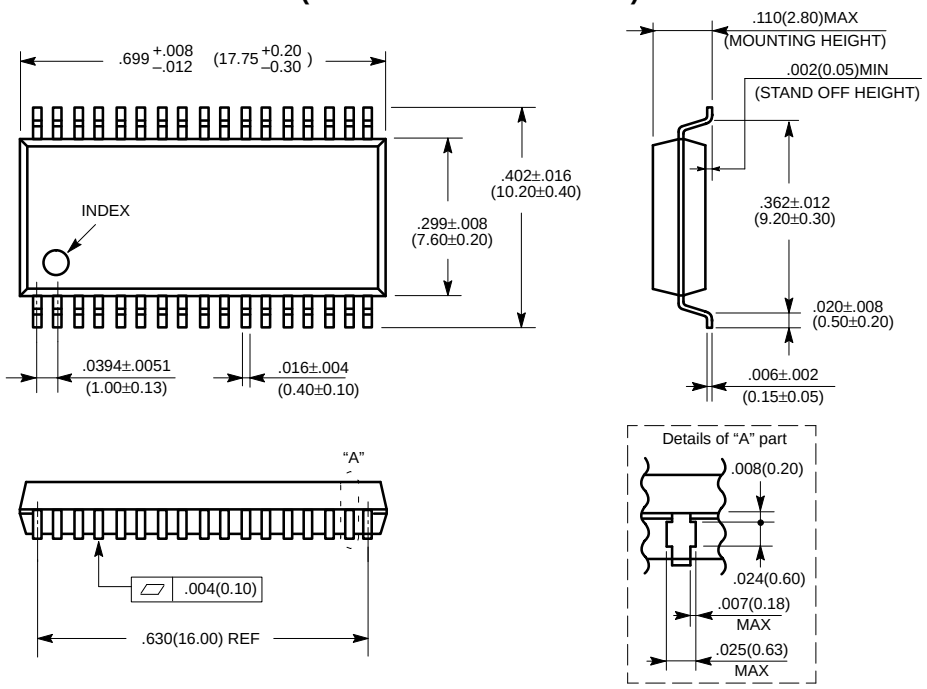
*:This dimension does not include resin protrusion.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

MB1530 Series

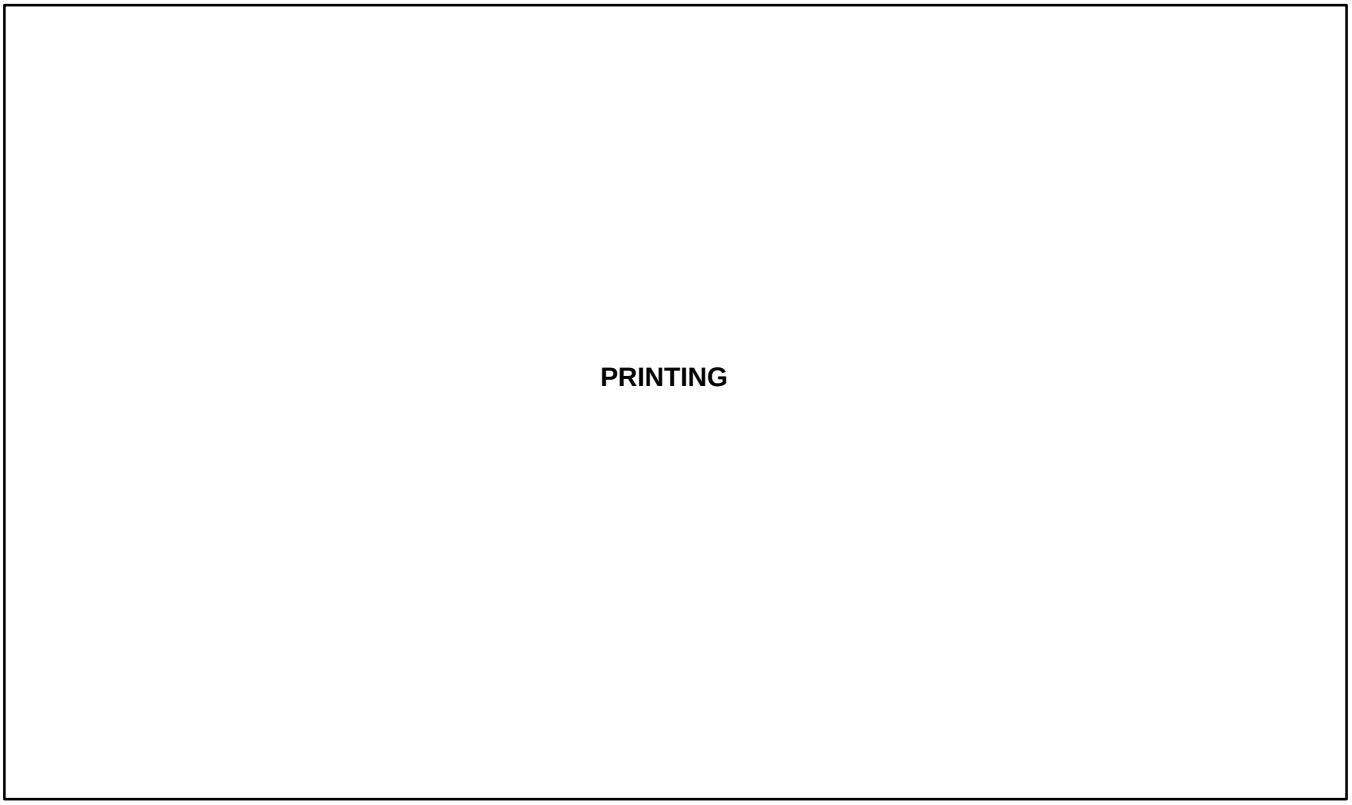
34-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-34P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

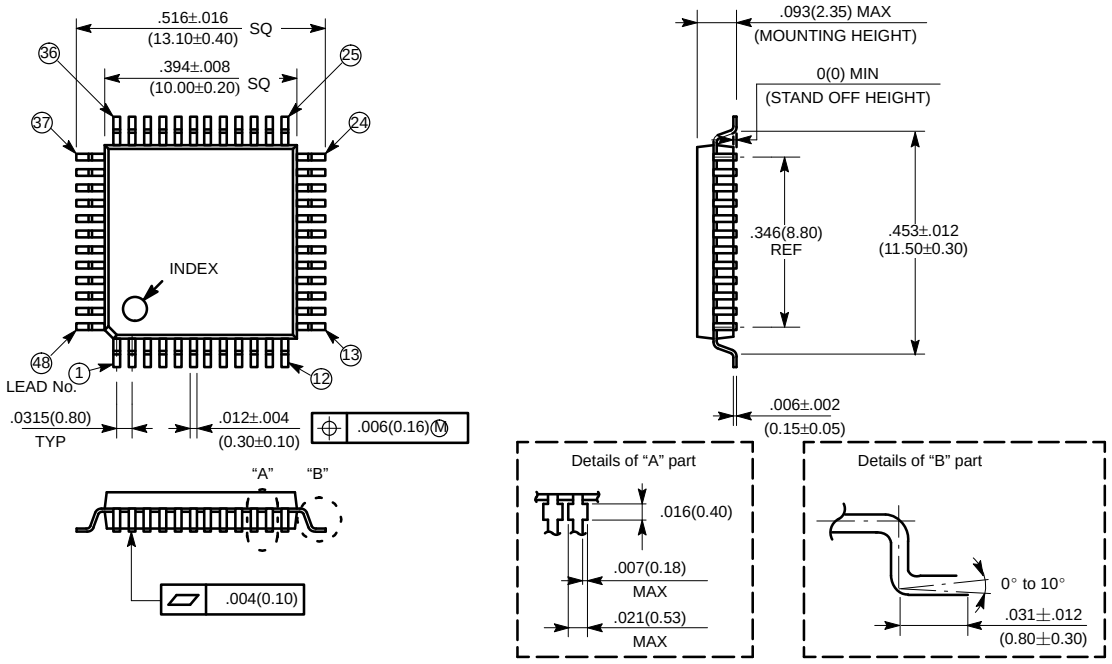
MB1530 Series



PACKAGE DIMENSIONS (Continued)

MB1540 Series
MB1550 Series

48-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-48P-M04)

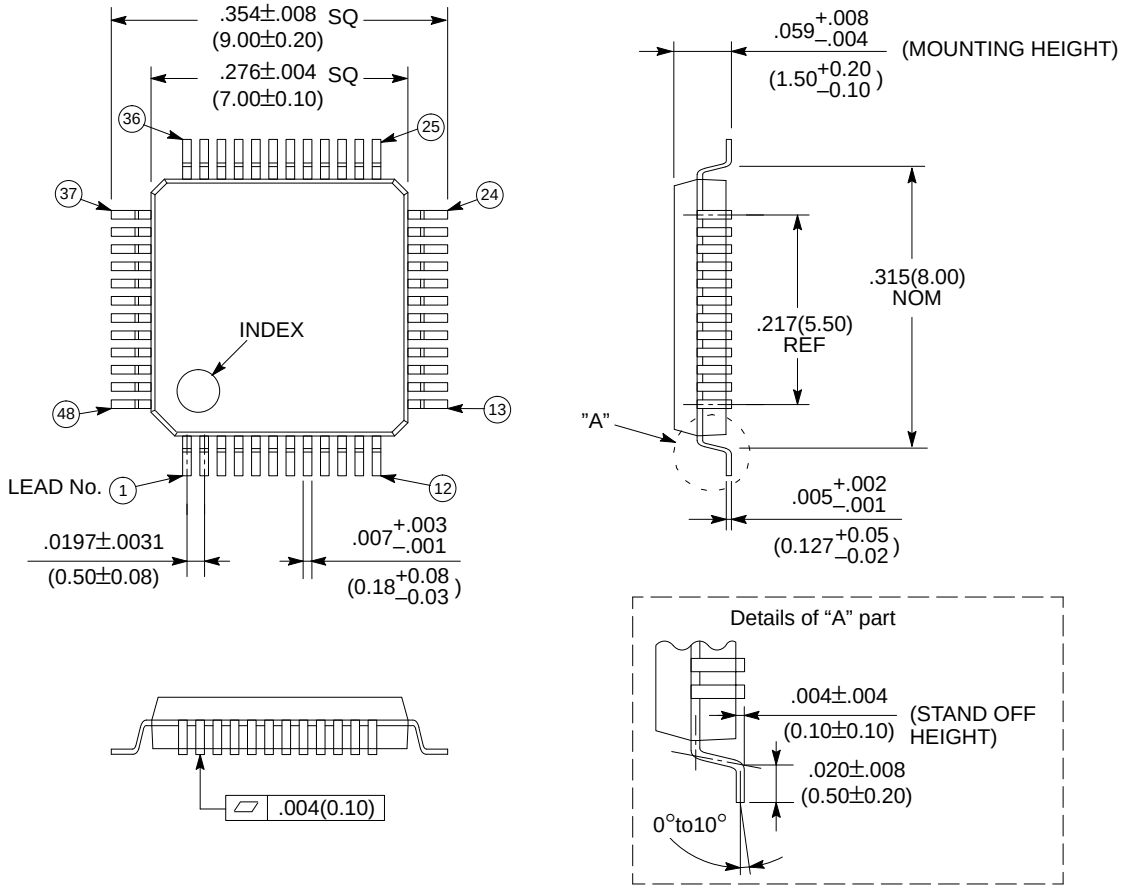


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

MB1540 Series

48-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-48P-M05)

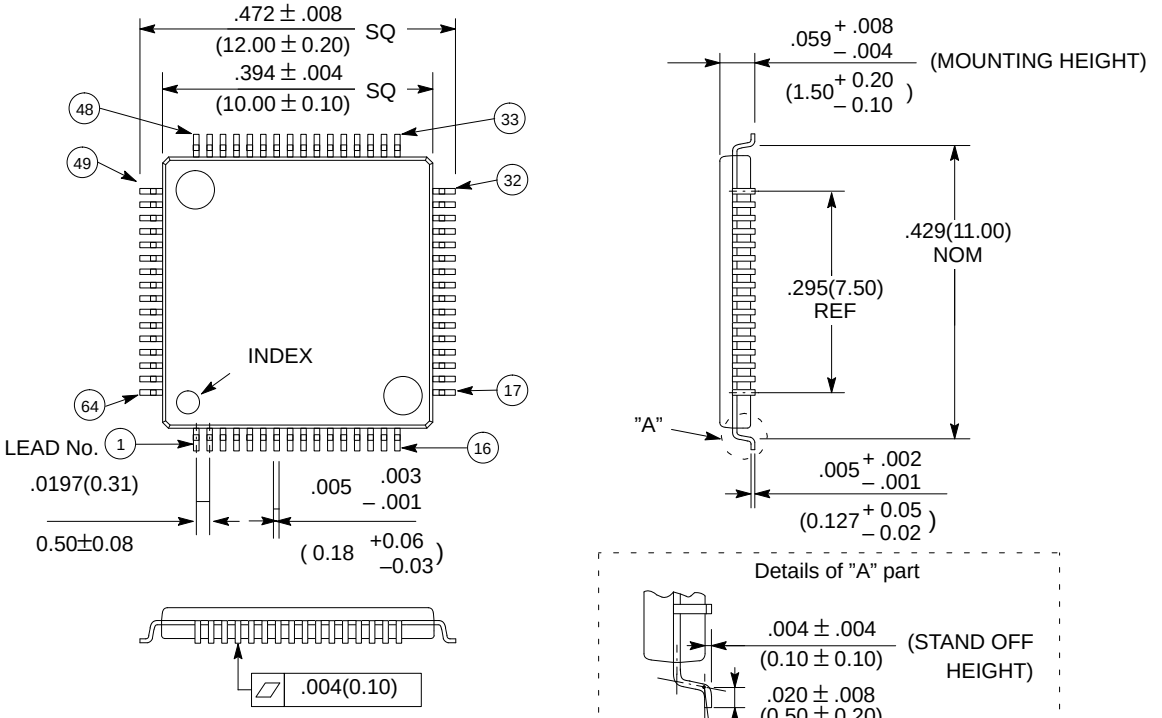


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

MB1550 Series

64-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-64P-M03)



Dimensions in
inches (millimeters)

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