March 1992
Edition 1.0

DATA SHEET

MB814400A-60/-70/-80

CMOS 1M x 4 BIT FAST PAGE MODE DRAM

CMOS 1,048,576 x 4 BIT FAST PAGE MODE DYNAMIC RAM

The Fujitsu MB814400A is a fully decoded CMOS Dynamic RAM (DRAM) that contains a total of 1,048,576 memory cells in 4-bit increments. The MB814400A features a "fast page" mode of operation whereby high-speed random access of up to 1,024-bits of data within the same row can be selected. The MB814400A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB814400A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB814400A is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814400A are not critical and all inputs are TTL compatible.

PRODUCT LINE & FEATURES

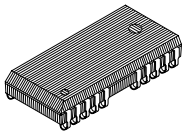
Parameter		MB814400A-60	MB814400A-70	MB814400A-80
$\overline{RAS}$ Access Time		60ns max.	70ns max.	80ns max.
$\overline{CAS}$ Access Time		15ns max.	20ns max.	20ns max.
Address Access Time		30ns max.	35ns max.	40ns max.
Random Cycle Time		110ns min.	125ns min.	140ns min.
Fastpage Mode Cycle Time		40ns min.	45ns min.	45ns min.
Low Power Dissipation	Operating current	605mW max.	550mW max.	495mW max.
	Standby current	11mW max. (TTL level) 5.5mW max. (CMOS level)		

- 1,048,576 word x 4 bit organization
- Early write or $\overline{OE}$ controlled write capability
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- All input and output are TTL compatible
- Fast Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance
- 1024 refresh cycles every 16.4ms

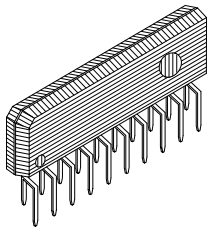
ABSOLUTE MAXIMUM RATINGS (see Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	–1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	–1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current		50	mA
Storage Temperature	TSTG	–55 to +125	°C

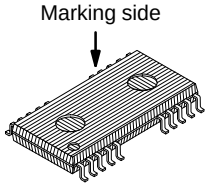
Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



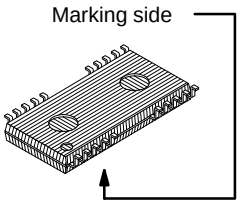
LCC-26P-M04



ZIP-20P-M02



(Normal Bend)
FPT-26P-M01



(Reserve Bend)
FPT-26P-M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB814400A DYNAMIC RAM – BLOCK DIAGRAM

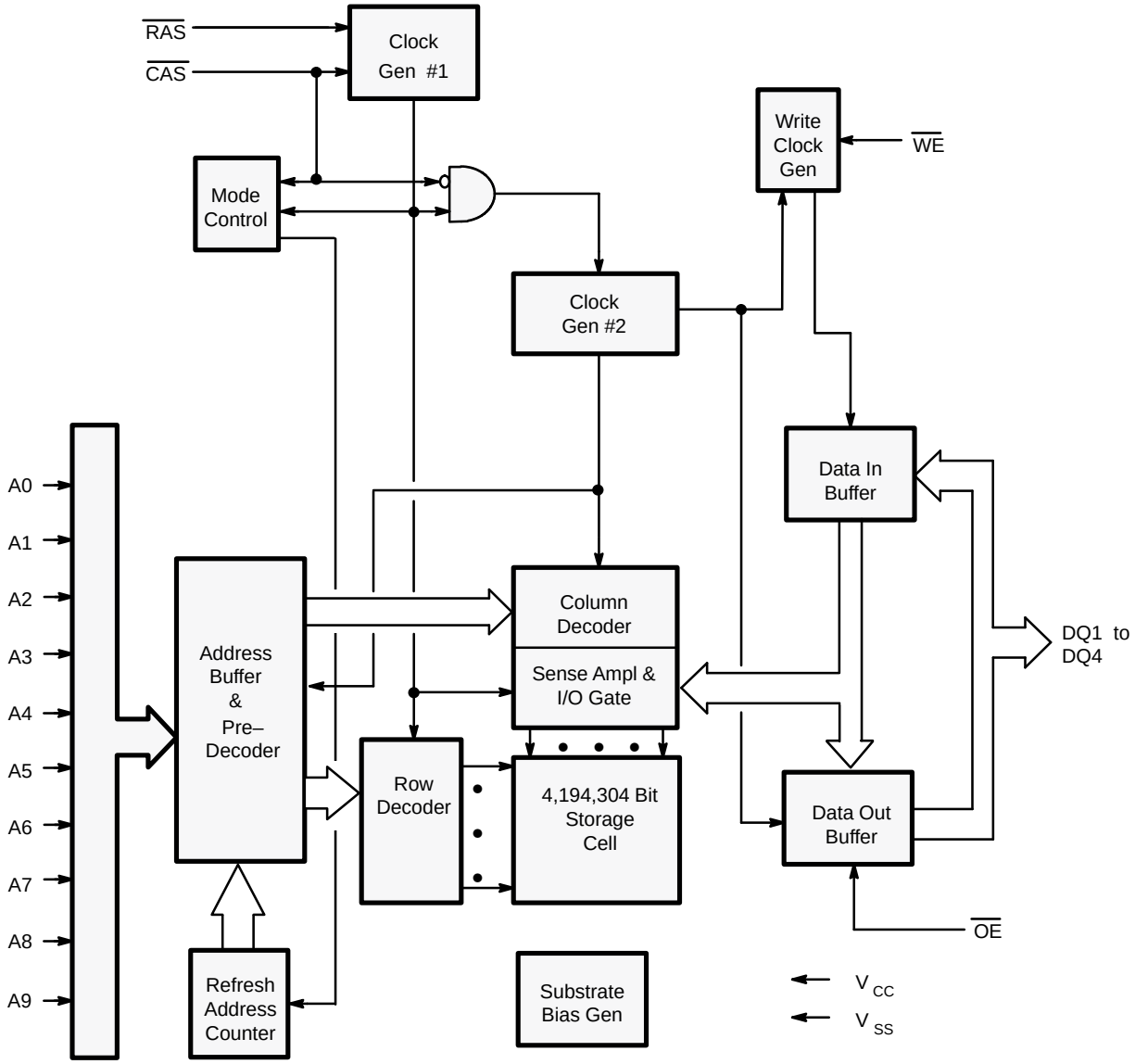


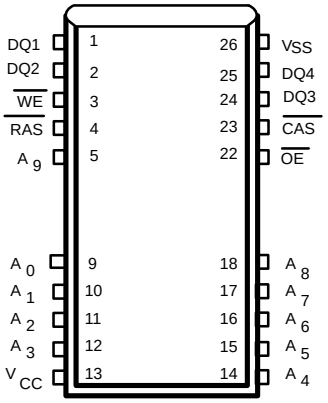
FIgure 1. MB814400A Dynamic Ram – Block Diagram

CAPACITANCE (T_A = 25°C, f = MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10, DIN	C_{IN1}		5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}		7	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}		7	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

26–Pin SOJ:
(TOP VIEW)



26–Pin FPT:
(TOP VIEW)

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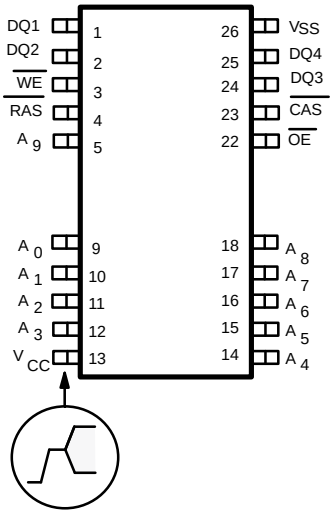
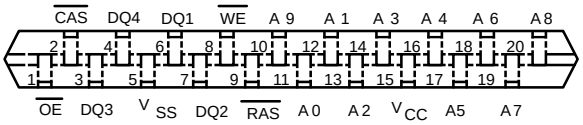


20–Pin ZIP:
(TOP VIEW)



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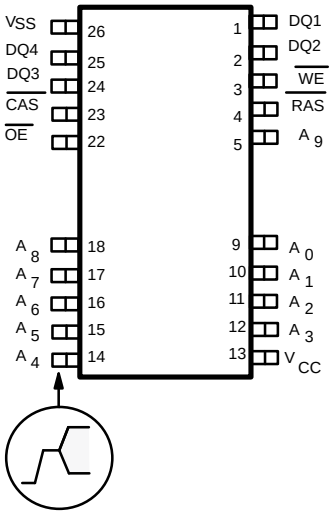


Designator	Function
DQ1 to DQ4	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{RAS}$	Row Address Strobe
A0 to A9	Address Inputs
VCC	+5 volt power supply
$\overline{OE}$	Output enable
$\overline{CAS}$	Column address strobe
VSS	Circuit ground

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage [1]	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
	V_{SS}	0	0	0		
Input High Voltage, all inputs [1]	VIH	2.4		6.5	V	
Input Low Voltage, all inputs [1]	VIL	–2.0		0.8	V	
Input Low Voltage, DQ [1]	VILD	–1.0		0.8	V	

Notes: Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 4,194,304 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{RAS}$ and $\overline{CAS}$ as shown in Figure 5. First, ten row address bits are applied on pins A0 through A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are applied and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$ respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of two basic ways — an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data (DQ1-DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- **t_{RAC} :** from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.
- **t_{CAC} :** from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).
- **t_{AA} :** from column address input when t_{RAD} is greater than t_{RAD} (max).
- **t_{OEA} :** from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after tRAC, tCAC, or tAA

The data remains valid until either $\overline{CAS}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 1,024 bits can be accessed and, when multiple MB814400s are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready-modify-write cycles are permitted.

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted) [3]

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Output high voltage [1]		V_{OH}	I_{OH} = –5 mA	2.4			V
Output low voltage [1]		V_{OL}	I_{OL} = 4.2 mA			0.4	
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤5.5V 4.5≤V_{CC}≤5.5V; V_{SS} = 0V; All other pins not under test = 0V	–10		10	µA
Output leakage current		$I_{O(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	–10		10	
Operating current (Average Power supply current)	MB814400A-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min			110	mA
	MB814400A-70					100	
	MB814400A-80					90	
Standby Current (Power supply current) [2]	TTL level	I_{CC2}	$\overline{RAS}$ =$\overline{CAS}$ =V_{IH}			2.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$≥V_{CC}–0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB814400A-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min			110	mA
	MB814400A-70					100	
	MB814400A-80					90	
Fast Page Mode current [2]	MB814400A-60	I_{CC4}	$\overline{RAS}$ =V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min			55	mA
	MB814400A-70					50	
	MB814400A-80					45	
Refresh current #2 (Average power supply current) [2]	MB814400A-60	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min			90	mA
	MB814400A-70					80	
	MB814400A-80					70	

AC CHARACTERISTICS
(At recommended operating conditions unless otherwise noted)[3, 4, 5]

No.	Parameter	Symbol	MB814400A-60		MB814400A-70		MB814400A-80		Unit
			Min.	Max	Min.	Max	Min.	Max	
1	Time Between Refresh	t_{REF}		16.4		16.4		16.4	ms
2	Random Read/Write Cycle Time	t_{RC}	110		125		140		ns
3	Read-Modify-Write Cycle Time	t_{RW}	130		150		165		ns
4	Access Time from $\overline{RAS}$ [6, 9]	t_{RAC}		60		70		80	ns
5	Access Time from $\overline{CAS}$ [7, 9]	t_{CAC}		15		20		20	ns
6	Column Address Access Time [8, 9]	t_{AA}		30		35		40	ns
7	Output Hold Time	t_{OH}	0		0		0		ns
8	Output Buffer Turn On Delay Time	t_{ON}	0		0		0		ns
9	Output Buffer Turn Off Delay Time [10]	t_{OFF}		15		15		20	ns
10	Transition Time	t_T	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time	t_{RP}	40		45		50		ns
12	$\overline{RAS}$ Pulse Width	t_{RAS}	60	100000	70	100000	80	100000	ns
13	$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time [11, 12]	t_{RCD}	20	45	20	50	20	60	ns
16	$\overline{CAS}$ Pulse Width	t_{CAS}	15		20		20		ns
17	$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns
18	$\overline{CAS}$ Precharge Time (Normal) [17]	t_{CPN}	10		10		10		ns
19	Row Address Set Up Time	t_{ASR}	0		0		0		ns
20	Row Address Hold Time	t_{RAH}	10		10		10		ns
21	Column Address Set Up Time	t_{ASC}	0		0		0		ns
22	Column Address Hold Time	t_{CAH}	12		12		15		ns
23	$\overline{RAS}$ to Column Address Delay Time [13]	t_{RAD}	15	30	15	35	15	40	ns
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30		35		40		ns
25	Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	30		35		40		ns
26	Read Command Set Up Time	t_{RCS}	0		0		0		ns
27	Read Command Hold Time Reference to $\overline{RAS}$ [14]	t_{RRH}	0		0		0		ns
28	Read Command Hold Time Referenced to $\overline{CAS}$ [14]	t_{RCH}	0		0		0		ns
29	Write Command Set Up Time [15]	t_{WCS}	0		0		0		ns
30	Write Command Hold Time	t_{WCH}	10		10		12		ns
31	$\overline{WE}$ Pulse Width	t_{WP}	10		10		12		ns
32	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15		20		20		ns
33	Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15		18		20		ns
34	DIN Set Up Time	t_{DS}	0		0		0		ns
35	DIN Hold Time	t_{DH}	10		10		12		ns
36	$\overline{RAS}$ to $\overline{WE}$ Delay Time [15]	t_{RWD}	85		95		110		ns
37	$\overline{CAS}$ to $\overline{WE}$ Delay Time [15]	t_{CWD}	40		45		50		ns
38	Column Address to WE Delay Time [15]	t_{AWD}	55		60		70		ns
39	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	t_{RPC}	0		0		0		ns

AC CHARACTERISTICS (Continued)
(At recommended operating conditions unless otherwise noted) [3, 4, 5]

No.	Parameter	Symbol	MB814400A-60		MB814400A-70		MB814400A-80		Unit
			Min.	Max	Min.	Max	Min.	Max	
40	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CSR}	0		0		0		ns
41	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	10		10		12		ns
42	$\overline{WE}$ Set Up Time from $\overline{RAS}$ [18]	t_{WSR}	0		0		0		ns
43	$\overline{WE}$ Hold Time from $\overline{RAS}$ [18]	t_{WHR}	10		10		10		ns
44	Access Time from $\overline{OE}$ [9]	t_{OEA}		15		20		20	ns
45	Output Buffer Turn off Delay from $\overline{OE}$ [10]	t_{OEZ}		15		15		20	ns
46	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data	t_{OEL}	10		10		10		ns
47	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$ [16]	t_{OEH}	0		0		0		ns
48	$\overline{OE}$ to Data in Delay Time	t_{OED}	15		15		15		ns
49	DIN to $\overline{CAS}$ Delay Time [17]	t_{DZC}	0		0		0		ns
50	DIN to $\overline{OE}$ Delay Time [17]	t_{DZO}	0		0		0		ns
51	Fast Page Mode Read/Write Cycle Time	t_{PC}	40		45		45		ns
52	Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	60		68		70		ns
53	Access Time from $\overline{CAS}$ Precharge [9, 18]	t_{CPA}		35		40		40	ns
54	Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10		10		10		ns
55	Fast Page Mode $\overline{RAS}$ Pulse width	t_{RASP}		200000		200000		200000	ns
56	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		40		ns
57	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	60		65		70		ns

Notes:
1. Referenced to VSS
2. I_{CC} depends on the output load conditions and cycle rates. The specified values are obtained with the output open. I_{CC} depends on the number of address change as $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$. I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$. I_{CC4} is specified at one time of address change during one Page Cycle.
3. An Initial pause ($\overline{RAS}=\overline{CAS}=$VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Figures 2 and 3.
7. If $t_{RCD} \geq \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min).
17. Either t_{RRH} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.
20. Assumes that Test mode function.

FUNCTIONAL TRUTH TABLE

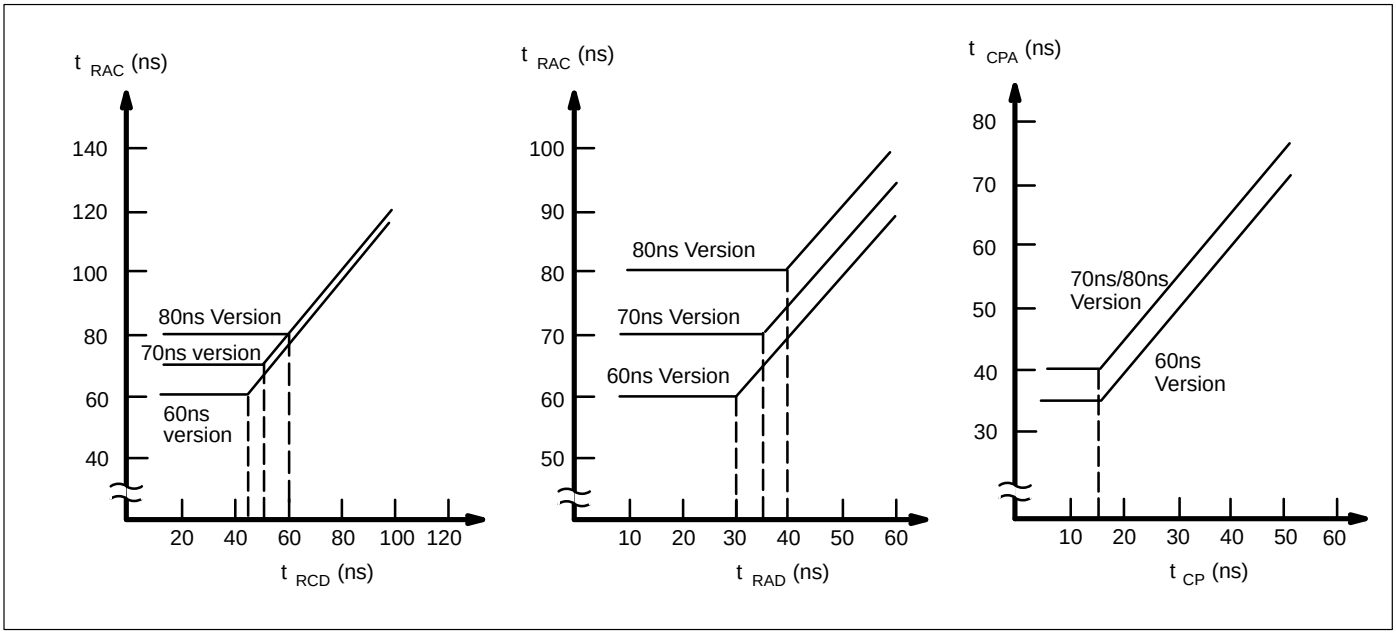


Figure 2. t_{RAC} **vs.** t_{RCD}

Figure 3. t_{RAC} **vs.** t_{RCD}

Figure 4. t_{CPA} **vs.** t_{CP}

Operation Mode	Clock Input				Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X				High-Z		
Read Cycle	L	L	H	L	Valid	Valid		Valid	Yes [1]	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes [1]	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L	H → L	L → H	Valid	Valid	Valid	Valid	Yes [1]	
$\overline{RAS}$-only Refresh Cycle	L	H	X	X	Valid			High-Z	Yes	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	H	X				High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	H	L				Valid	Yes	Previous data is kept
Test mode set cycle (CBR)	L	L	L	X				High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min) $t_{WSR} \geq t_{WSR}$ (min)
Test Mode set cycle (Hidden)	H → L	L	L	L				Valid	Yes	$t_{CSR} \geq t_{CSR}$ (min) $t_{WSR} \geq t_{WSR}$ (min)

Notes: X= “H” or “L”

1. It is impossible in Fast Page Mode.

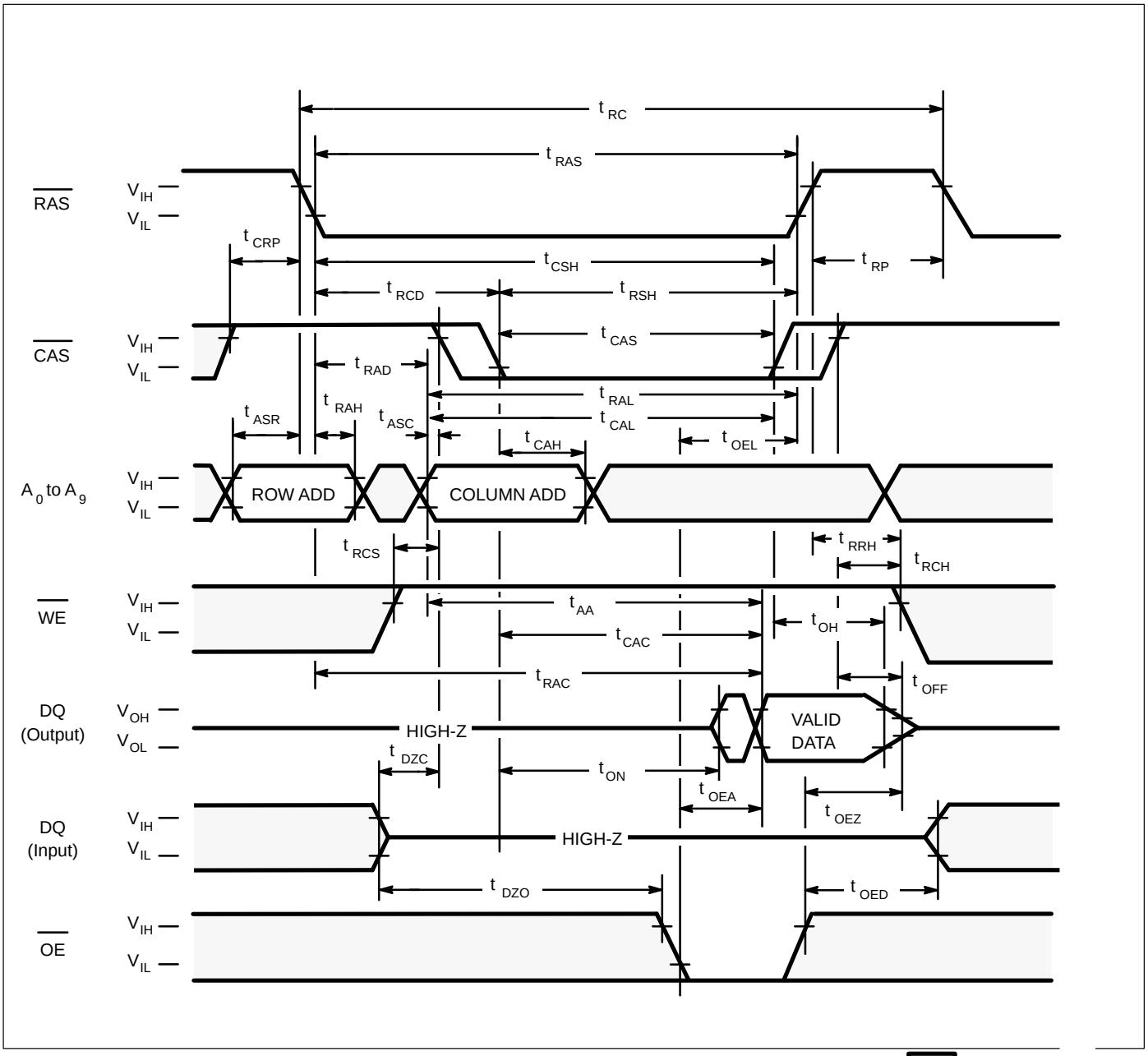


Figure 5. Read Cycle

DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and with $\overline{WE}$ set to a High Level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), $\overline{OE}$ (tOEA) or column addresses (tAA) under the following conditions:

If tRCD > tRCD (max), access time = tCAC
If tRAD > tRAD (max), access time = tAA
If $\overline{OE}$ is brought Low after tRAC, tCAC, or tAA (whichever occurs later), access time = tOEA

However, if either $\overline{CAS}$ of $\overline{OE}$ goes High, the output returns to a high-impedance state after tOH is satisfied

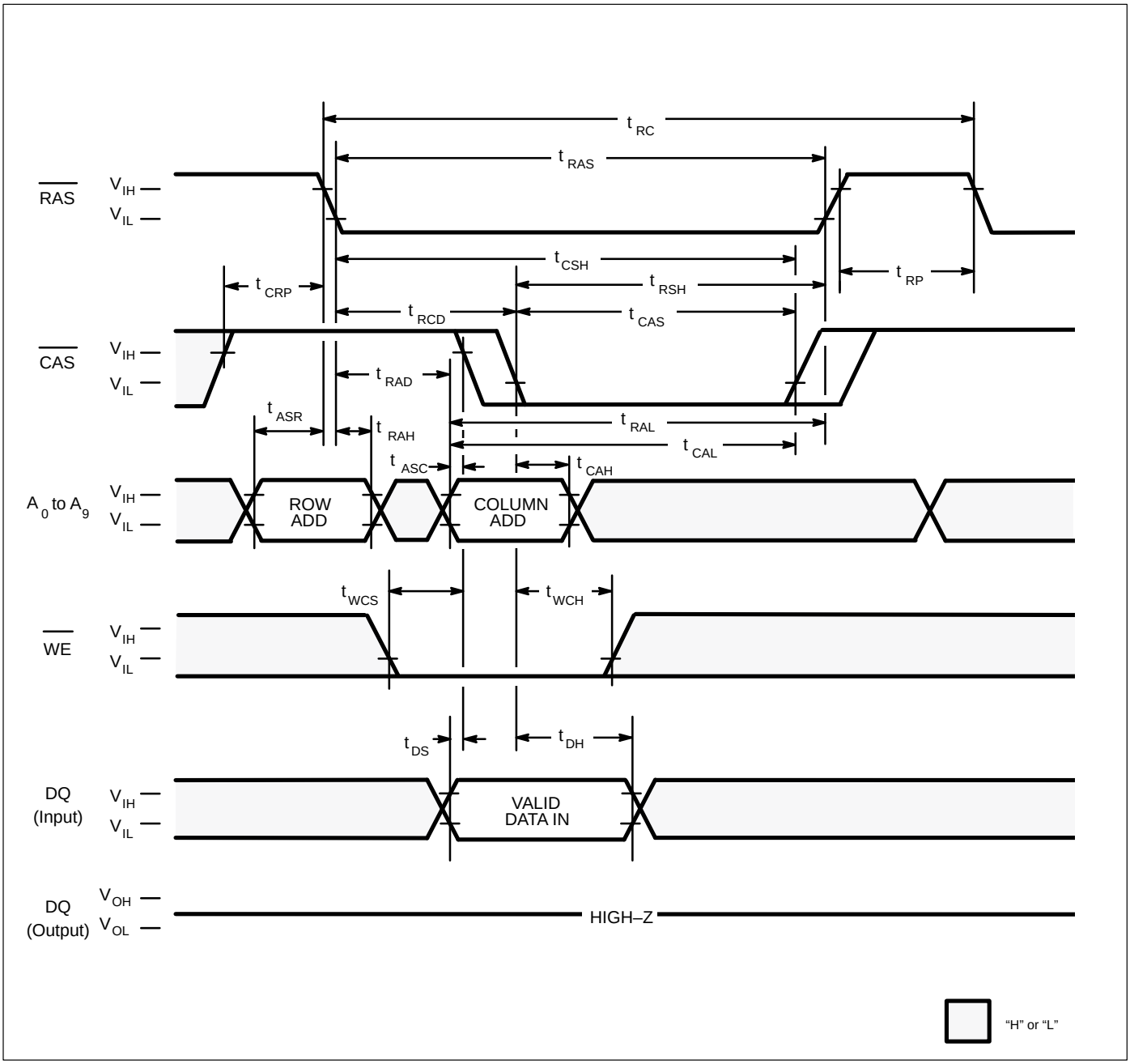


Figure 6. Early Write Cycle ($\overline{OE}$ = "H" or "L")

DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, $\overline{OE}$ write (delayed write), or read-modify-write. During all write cycles, timing parameters tWRL, tCWL and tRAL must be satisfied. In the early shown above tWRS satisfied, data on the DQ pin is latched with the falling edge of $\overline{CAS}$ and written into memory.

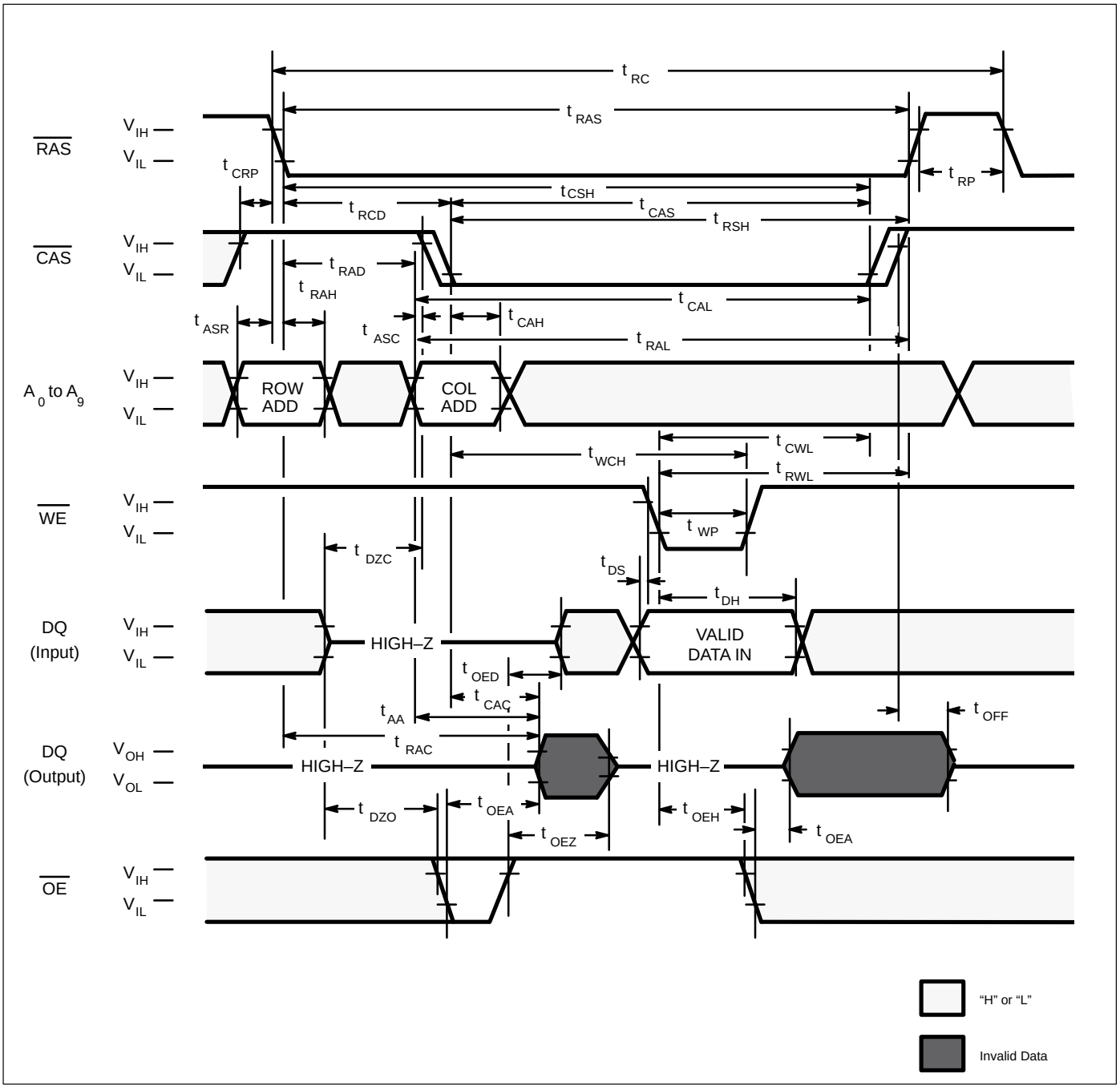


Figure 7. $\overline{OE}$ (Delayed Write Cycle)

DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, tWCS is not satisfied; thus, the data on the DQ pins is latched with falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tT + tDS).

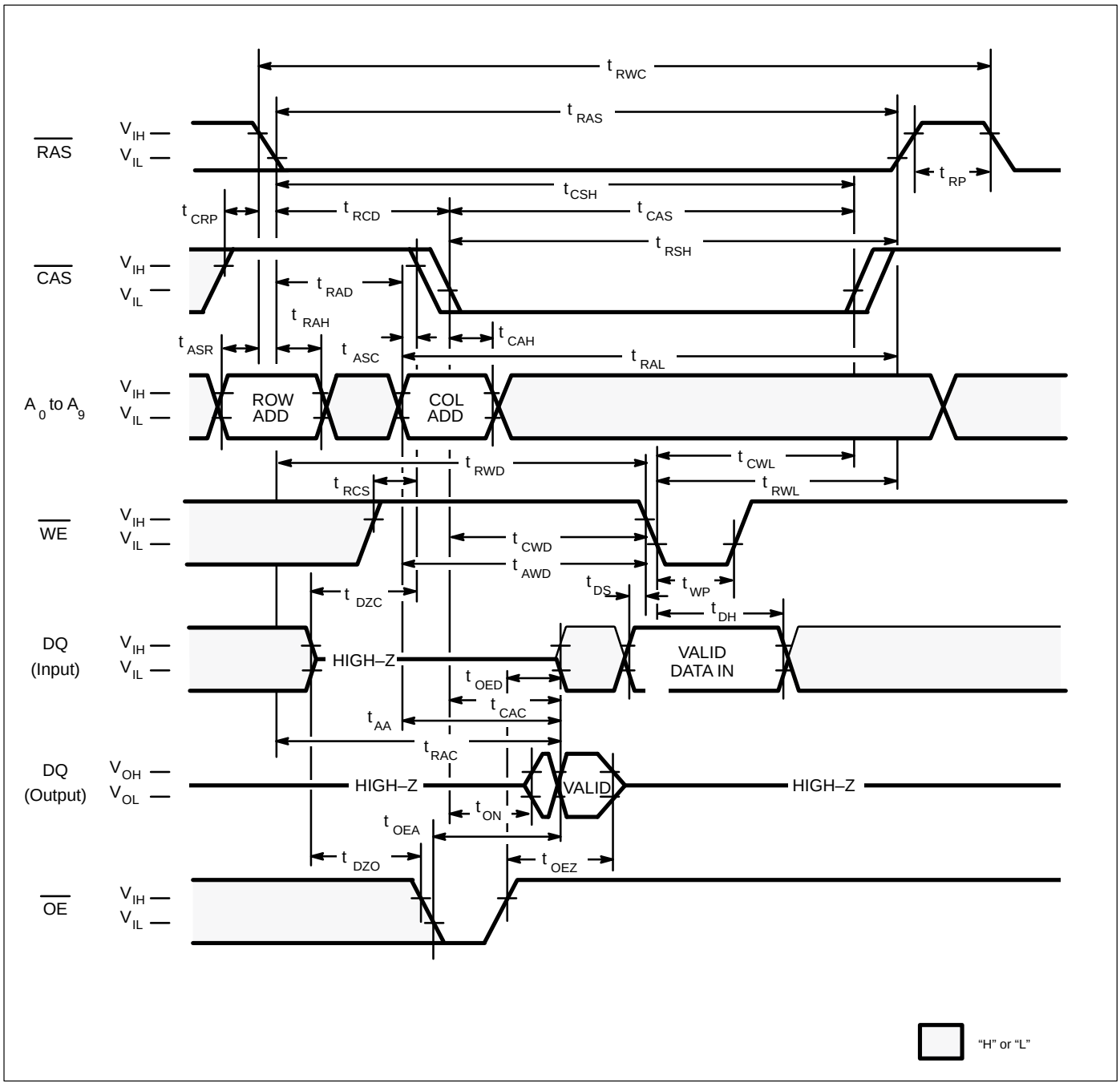


FIgure 8. Read-Modify-Write Cycle

DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

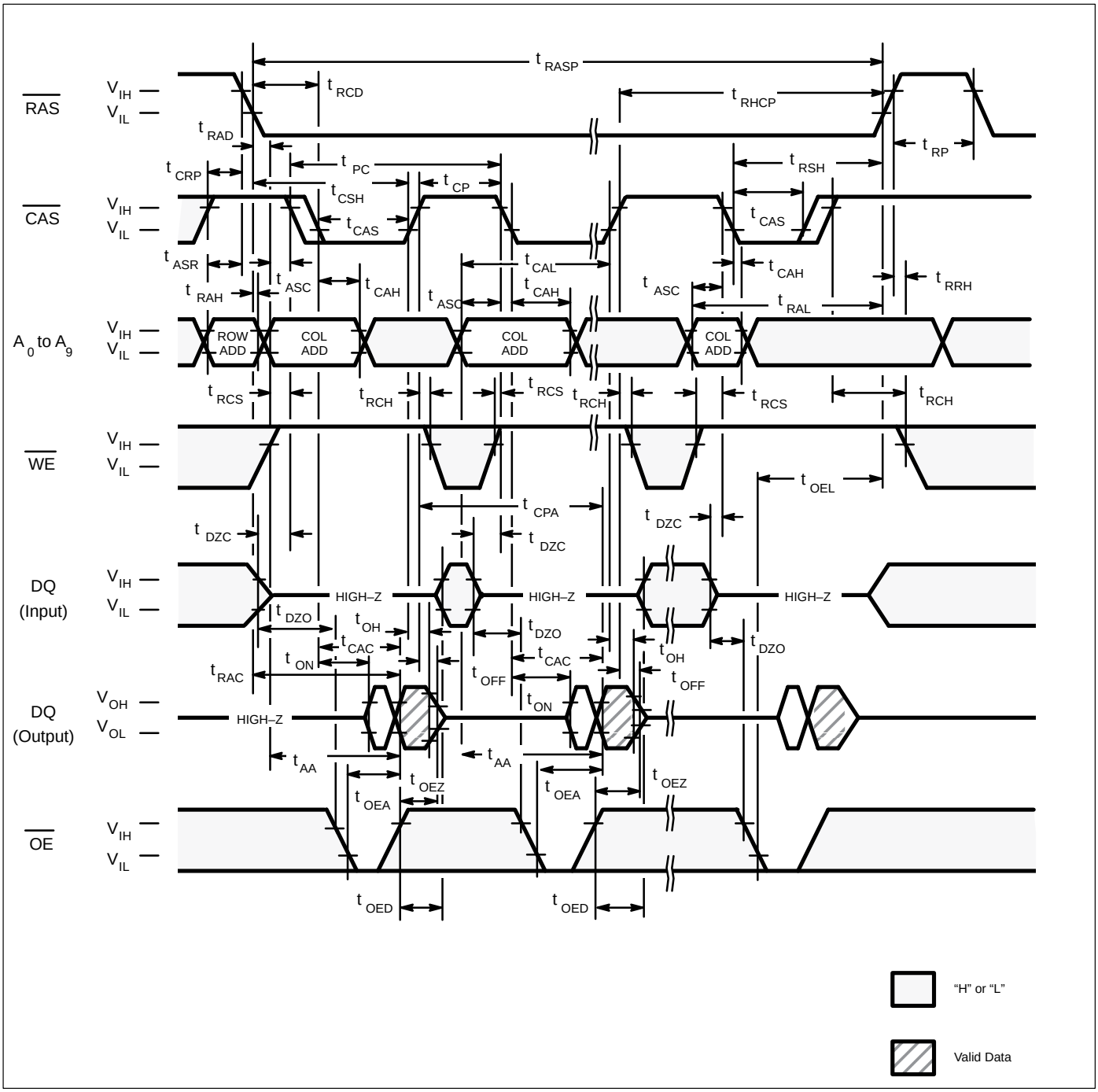


Figure 9. Fast Page Mode Read Cycle

DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, which one is the latest in occurring.

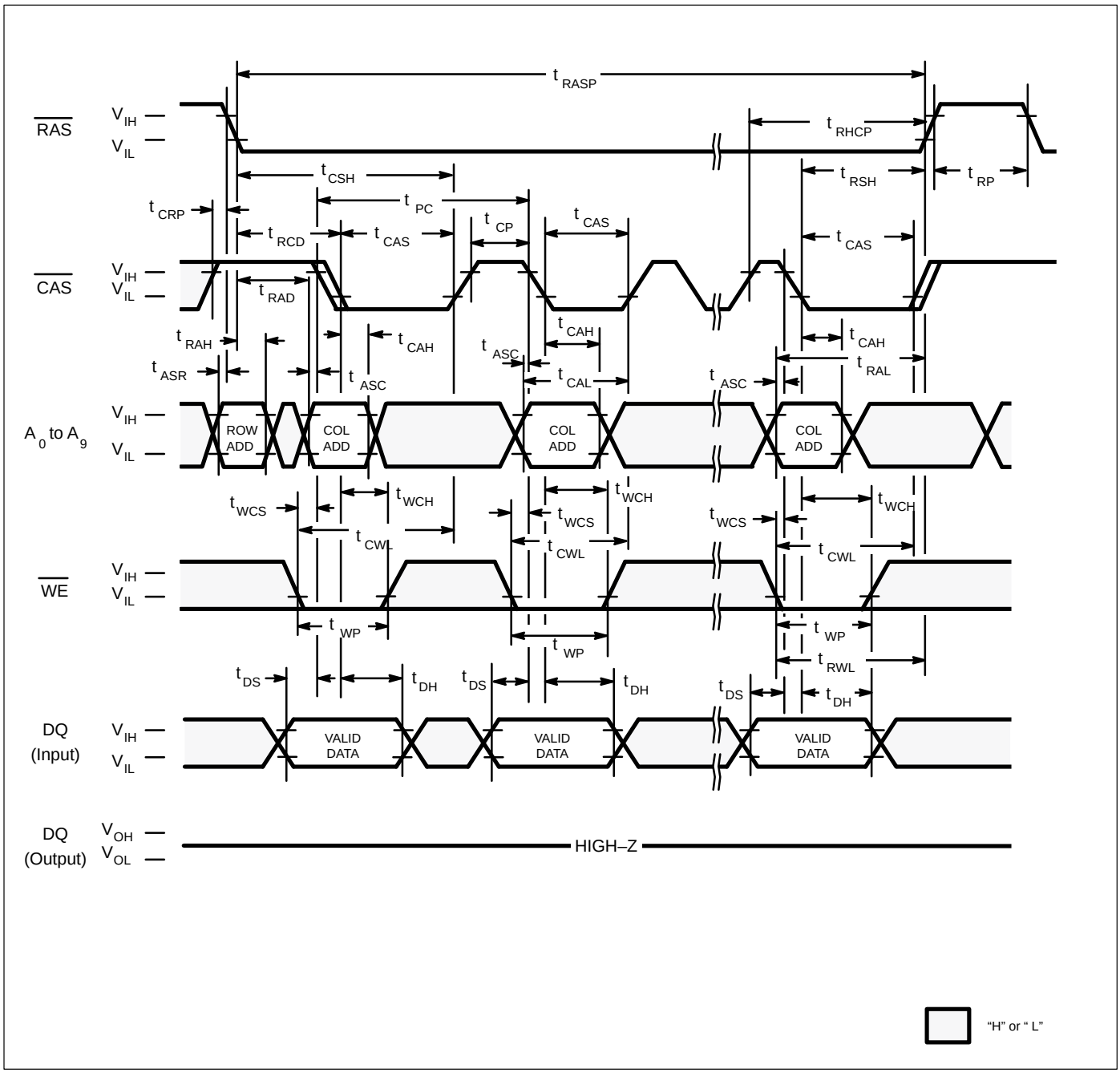


FIgure 10. Fast Page Mode Write Cycle ($\overline{OE}$ = "H" or "L")

DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing in the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read-modify-write cycles, tCWL must be satisfied.

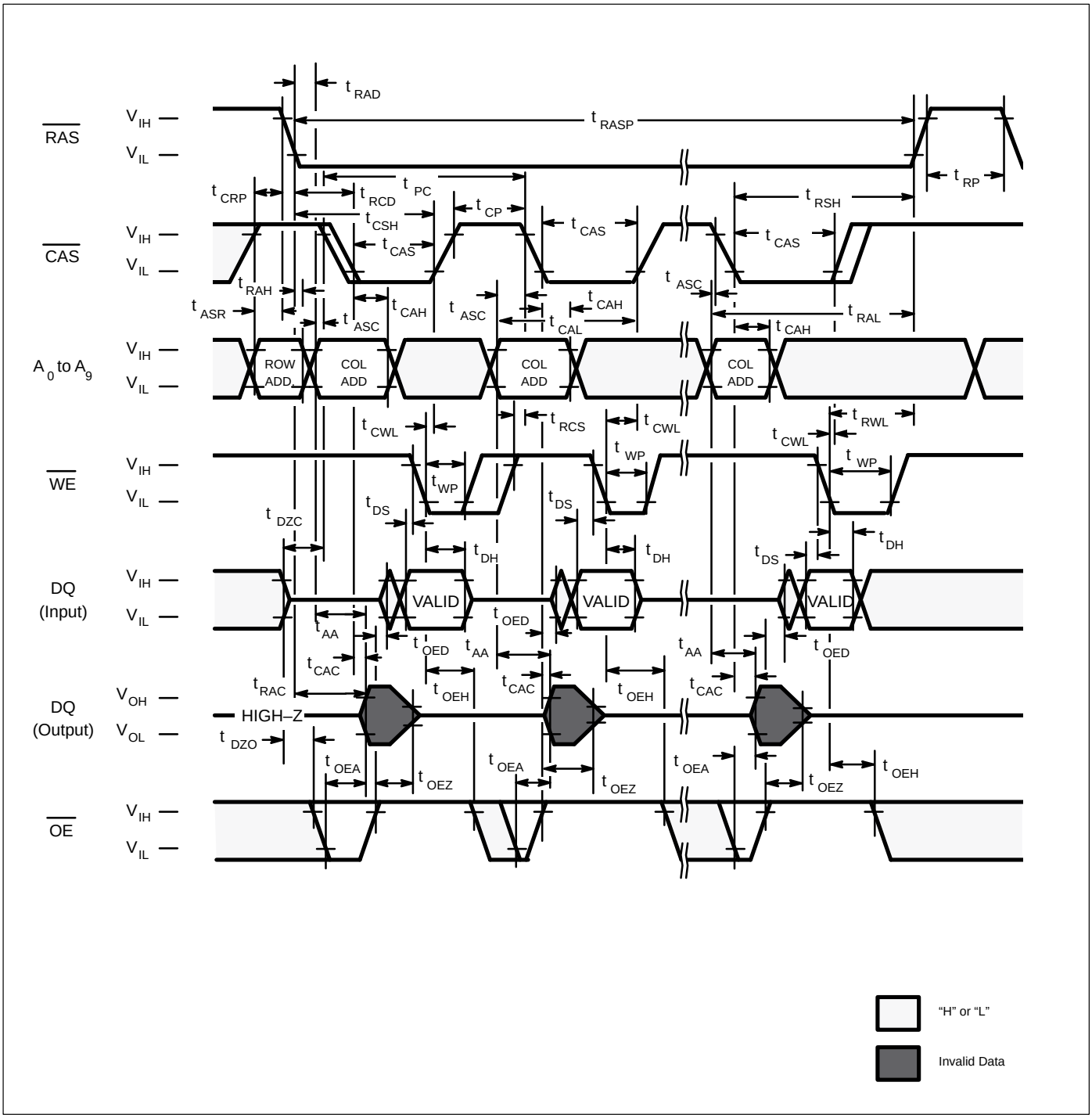


Figure 11. Fast Page Mode $\overline{OE}$ Write Cycle

DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is execute in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tT + tDS).

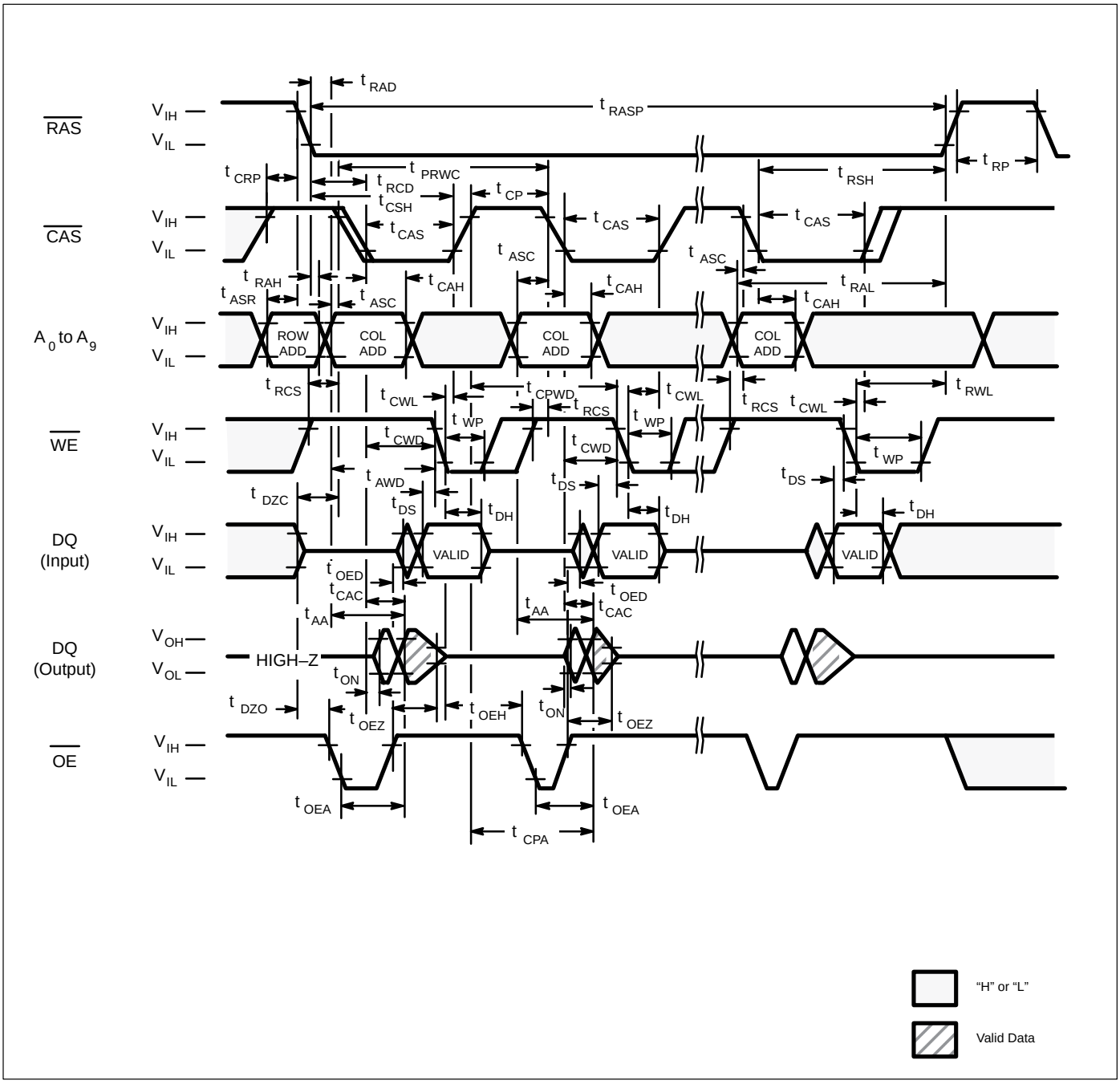


Figure 12. FAST PAGE MODE READ–MODIFY–WRITE CYCLE

DESCRIPTION

During fast page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

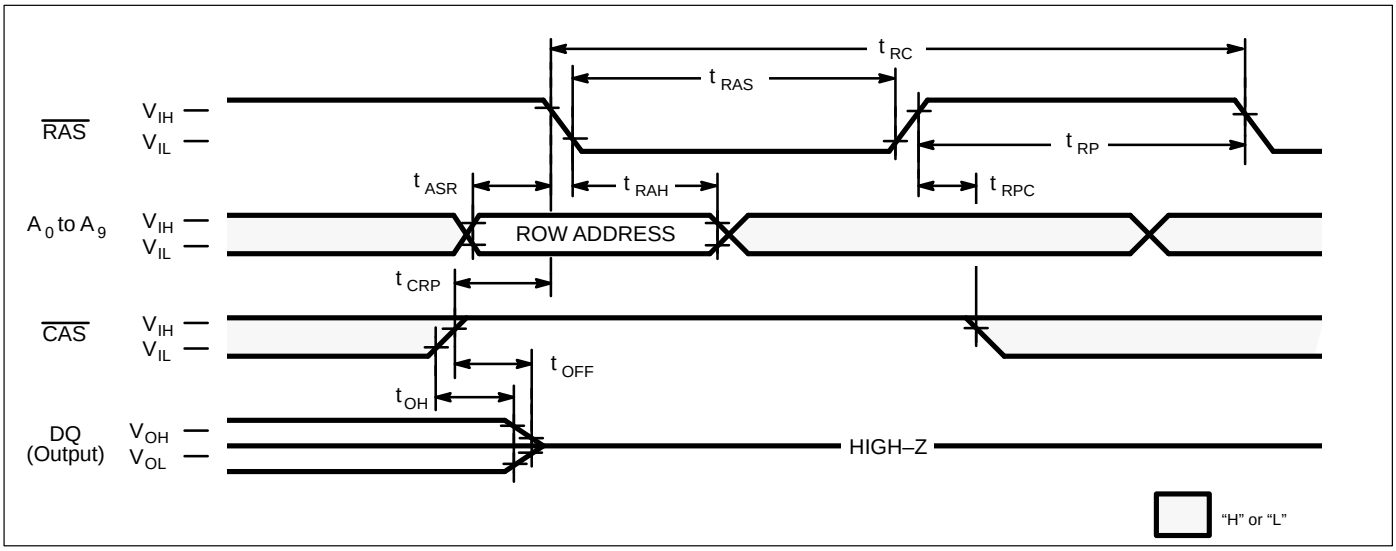


Figure 13. $\overline{RAS}$-Only Refresh ($\overline{WE}$ = $\overline{OE}$ = "H" of "L")

DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1024 row addresses every 16.4 milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed os latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pin is kept in a high-impedance state.

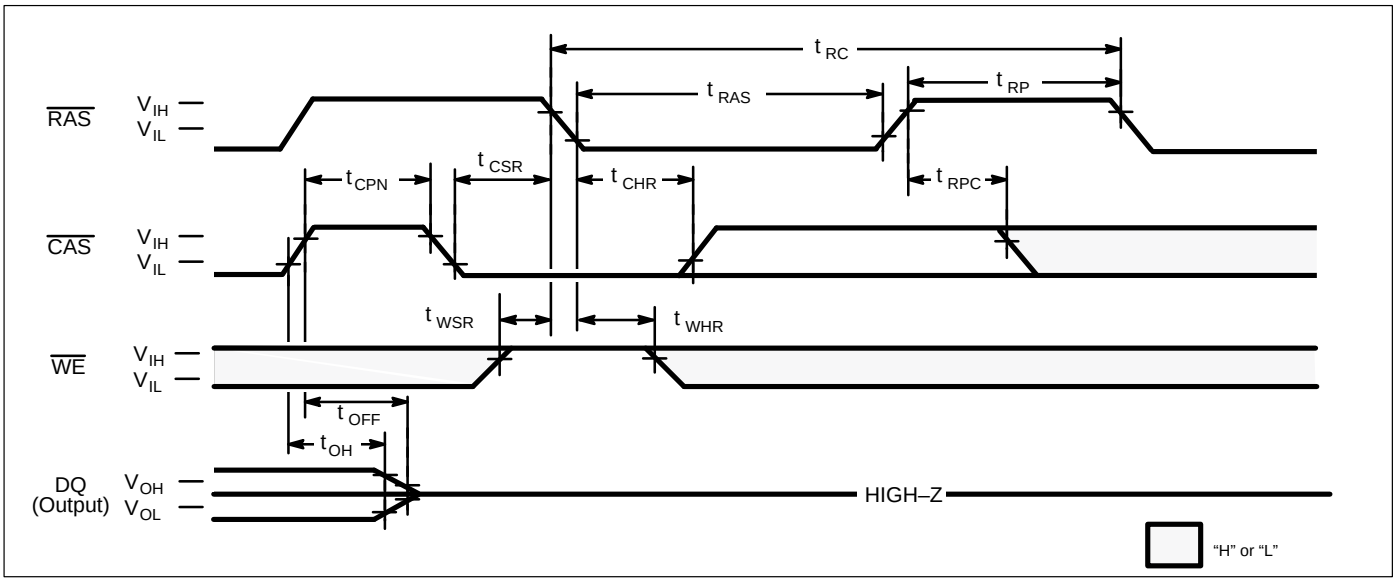


Figure 14. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh (Addresses = $\overline{OE}$ = "H" or "L")

DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented on preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

$\overline{WE}$ must be held High for the specified setup time (tWSR) before $\overline{RAS}$ low in order not enter "test mode".

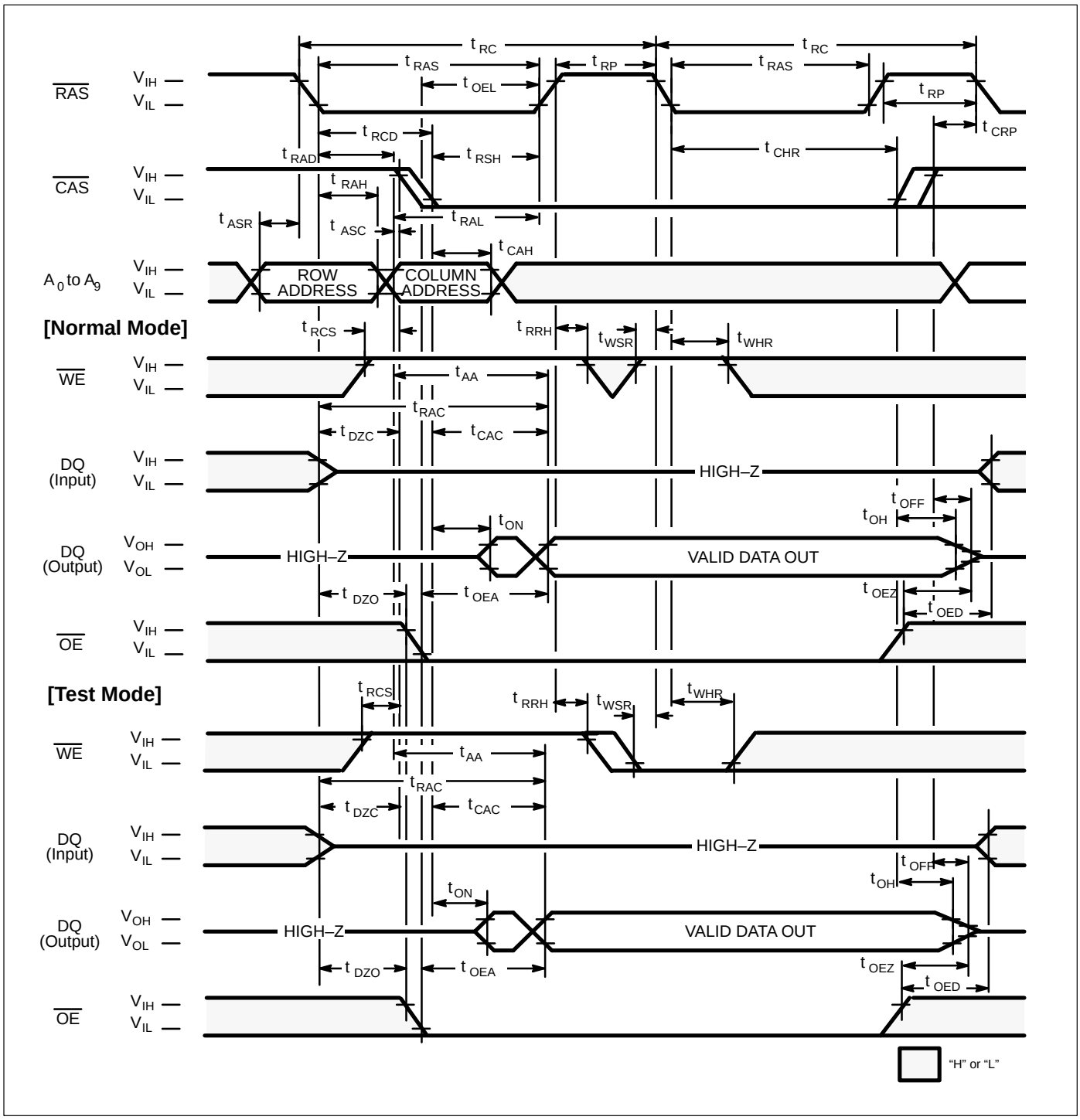


Figure 15. Hidden Refresh Cycle

DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ capability.

$\overline{WE}$ must be held High for the specified set up time (tWSR) before $\overline{RAS}$ goes Low in order not to enter "test mode".

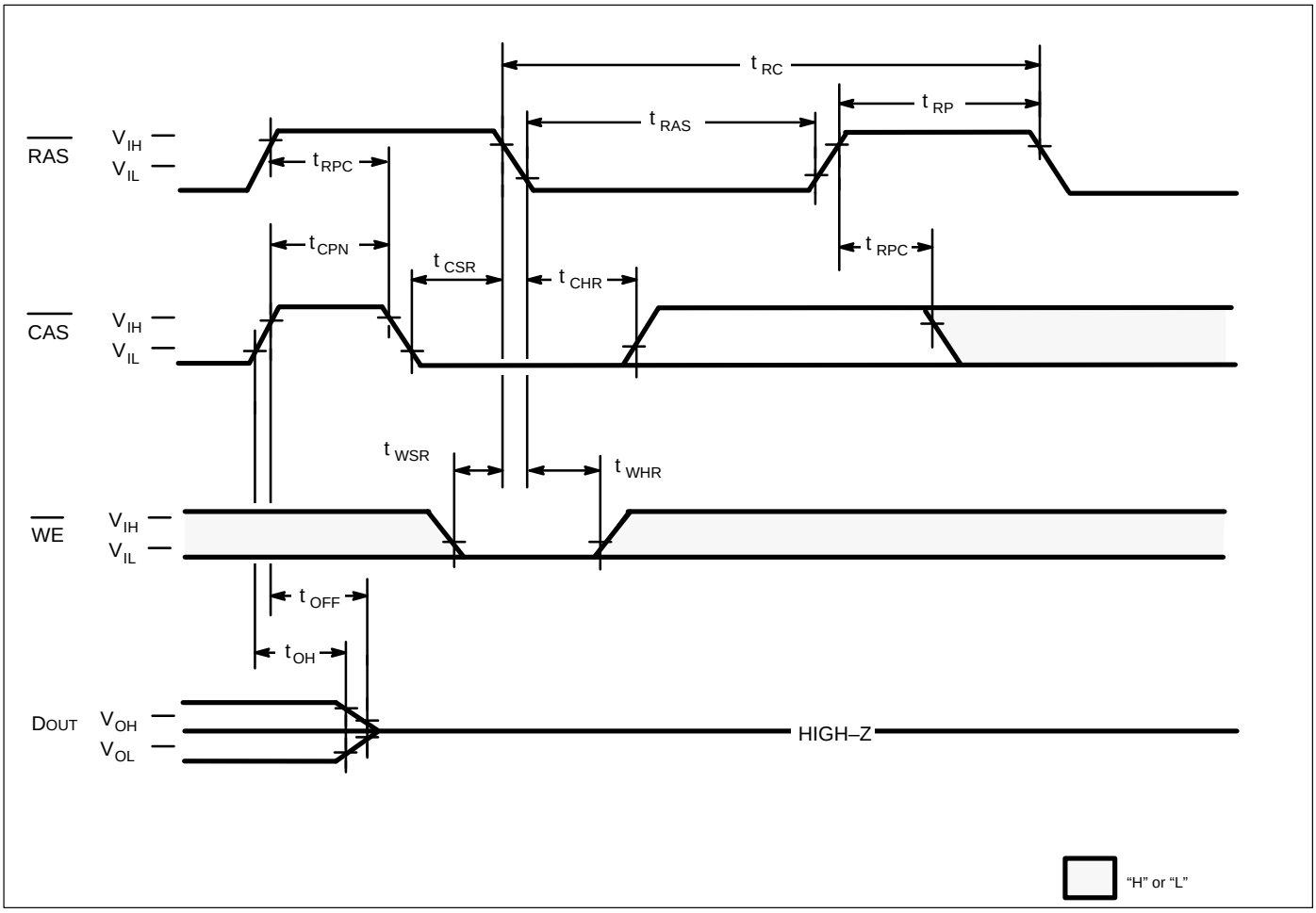


Figure 16. Test Mode Set Cycle (A0 to A9, $\overline{OE}$ = "H" or "L")

DESCRIPTION

Test Mode

The purpose of this test mode is to reduce device test time to one eight of that required to test the device conventionally. The test mode function is entered by performing a $\overline{WE}$ and $\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh for the entry cycle. In the test mode, read and write operations are executed in units of eight bits which are selected by the address combination of CAO. In the write mode, data is written into eight cells simultaneously. But the data must be input from DQ2 only. In the read mode, the data of eight cells at the selected addresses are read out from DQ and checked in the following manner.

When the eight bits are all "L" or all "H" level is output.
When the eight bits show a combination of "L" and "H", a "L" level is output.

The test mode function is exited by performing a RAS-only refresh or a $\overline{CAS}$-before-$\overline{RAS}$ refresh for the exit cycle. In test mode operation, the following parameters are delayed approximately 5ns from the specified value in the data sheet.

tRC, tRWC, tRAC, tAA, tRAS, tCSH, tRAL, tRWD, tAWD, tWP, tPRWC, tCPA, tRHCP, tCPWD

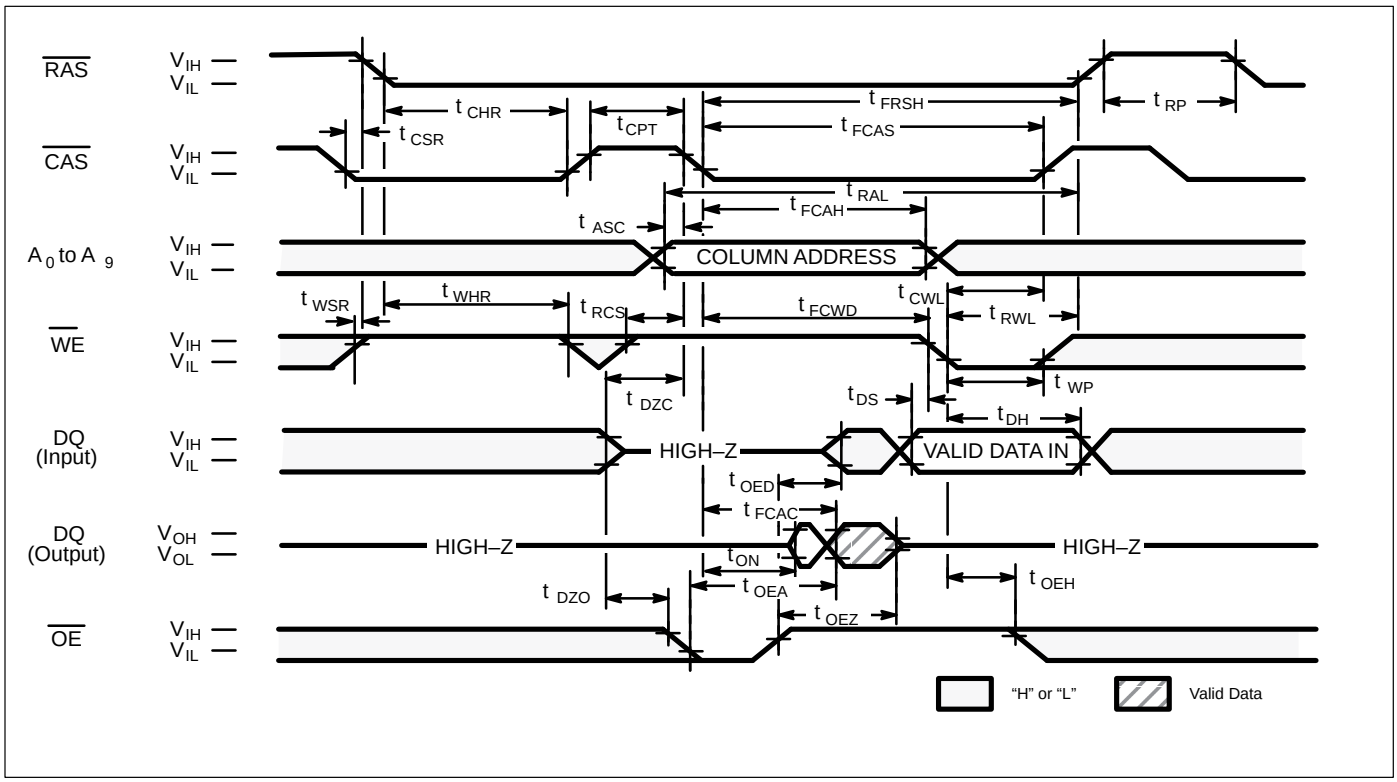


Figure 17. $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A10 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A10 are defined by latching levels on A0-A9 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows:

1. Initialize the internal refresh address counter by using 8 $\overline{RAS}$ only refresh cycles.
2. Use the same column address throughout the test.
3. Write “0” to all 1024 row addresses at the same column address by using normal write cycles.
4. Read “0” written in procedure 3 and check, simultaneously write “1” to the same addresses by using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test (read-modify-write cycles). Repeat this procedure 1024 times with addresses generated by the internal refresh address counter.
5. Read and check data written in procedure 4 by using normal read cycle for all 1024 memory locations.
6. Reverse test data and repeat procedures 3, 4, and 5.

(At recommended operating conditions unless otherwise noted)

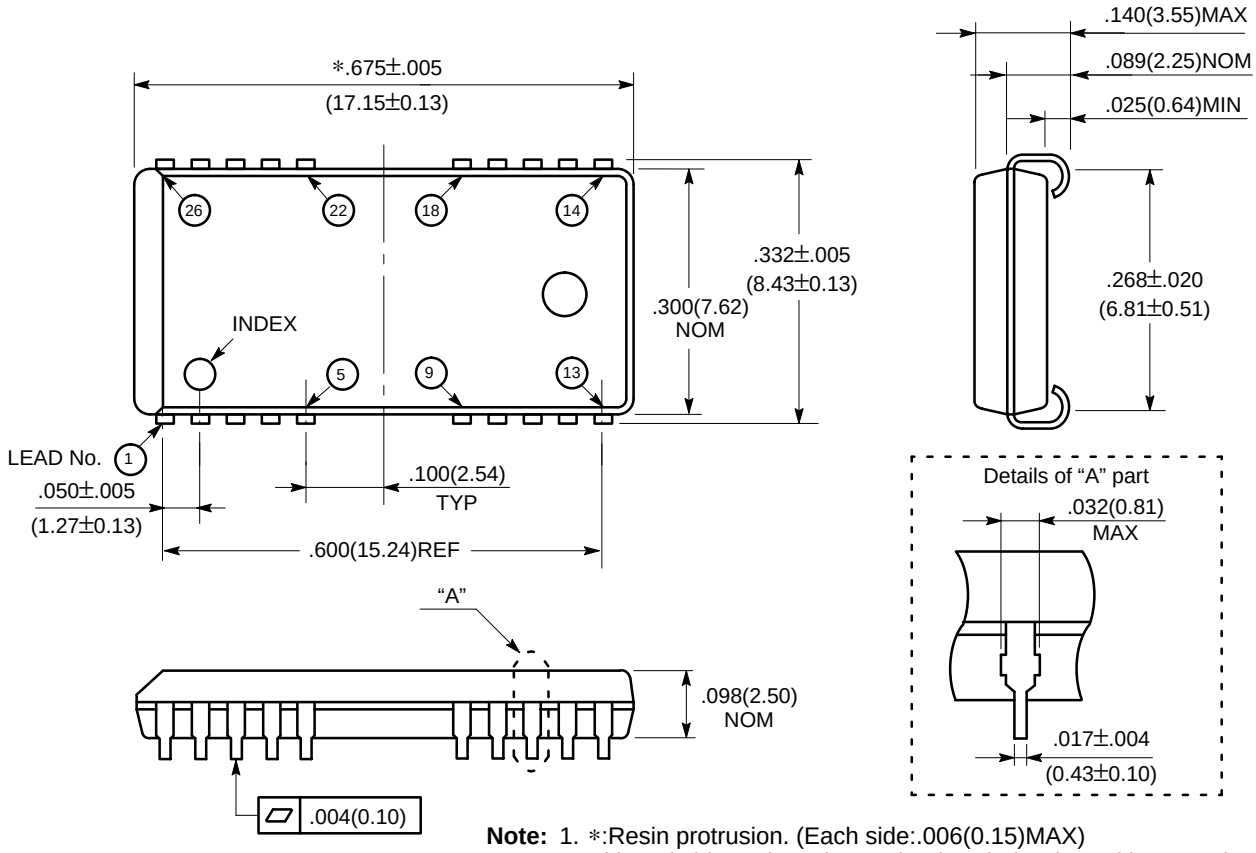
No.	Parameter	Symbol	MB814400A-60		MB814400A-70		MB814400A-80		Unit
			Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	50	—	55	—	60	ns
91	Column Address Hold Time	t_{FCAH}	30	—	30	—	35	—	ns
92	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{FCWD}	50	—	55	—	60	—	ns
93	$\overline{CAS}$ Pulse Width	t_{FCAS}	50	—	55	—	60	—	ns
94	$\overline{RAS}$ Hold Time	t_{FRSH}	50	—	55	—	60	—	ns

Note: Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix: -PJN)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)

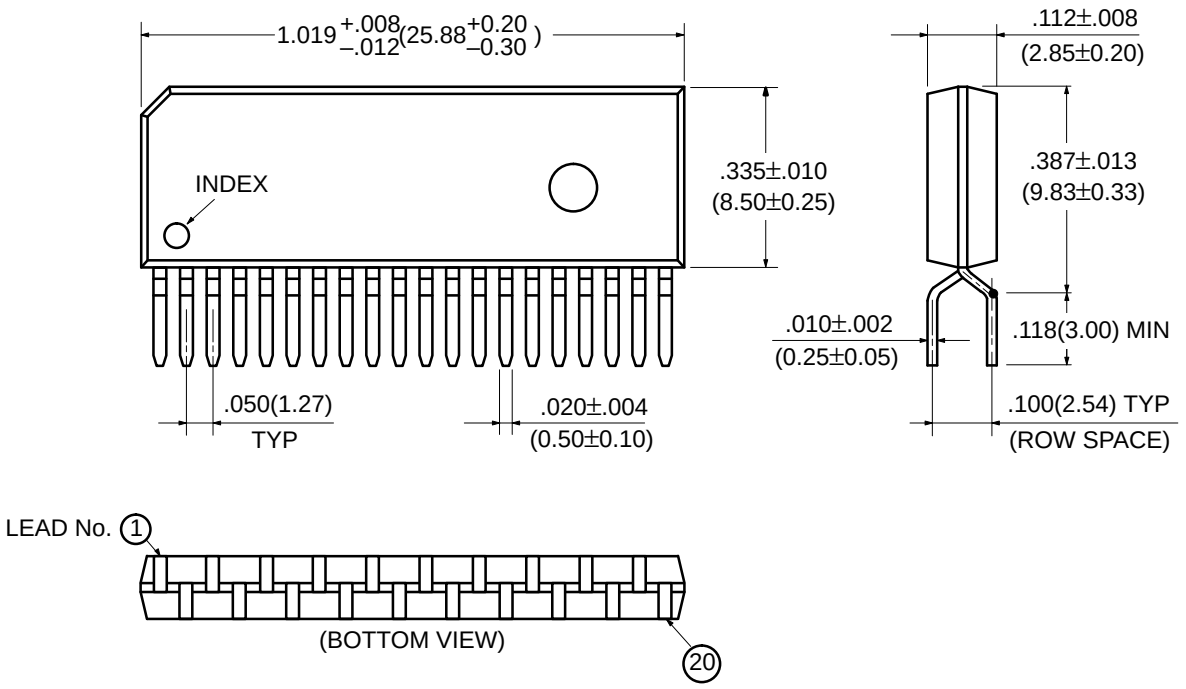


Note: 1. *:Resin protrusion. (Each side:.006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
3. Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)

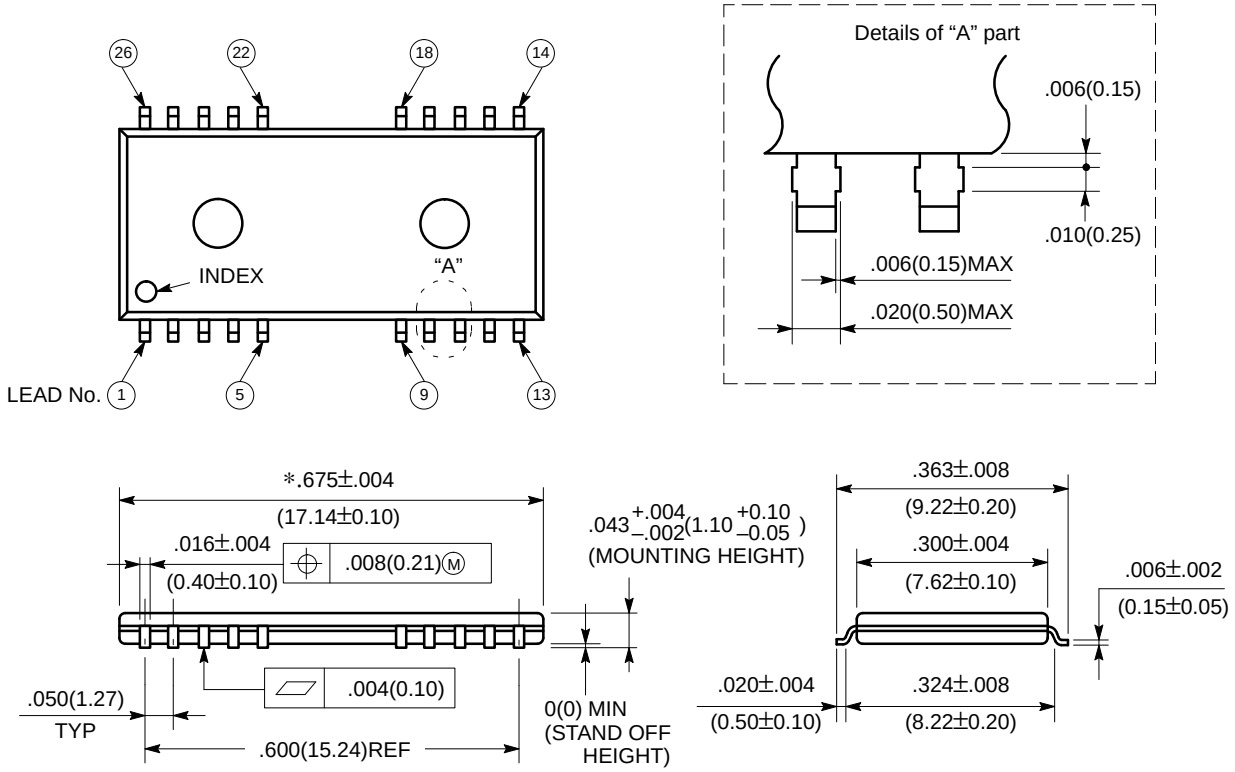


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN)

26-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-26P-M01)



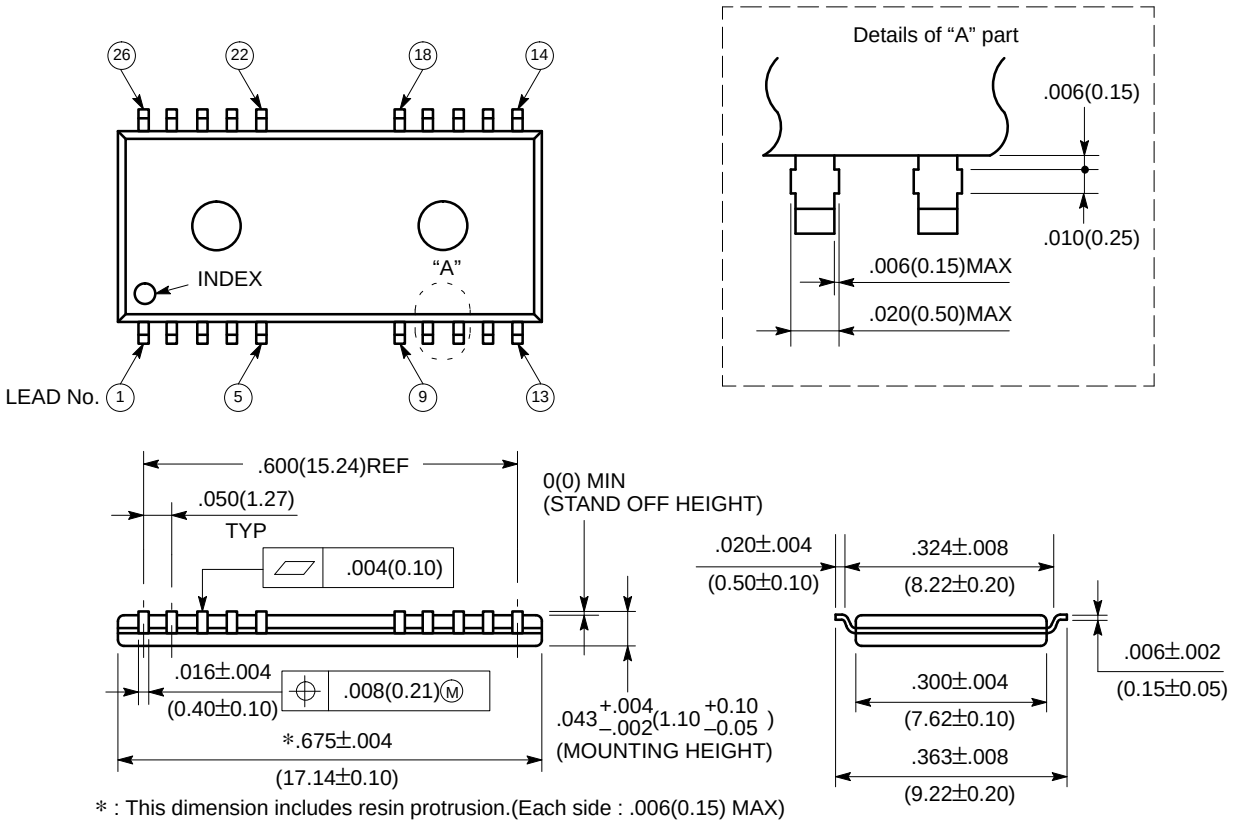
* : This dimension includes resin protrusion.(Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTR)

26-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-26P-M02)



* : This dimension includes resin protrusion.(Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

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