Sept 1995
Edition 2.0

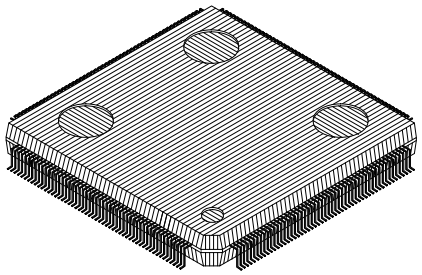
DATA SHEET

MB86687
Adaptation Layer Controller (ALC)

Adaptation Layer Controller

The FUJITSU MB86687 is an ATM protocol controller which autonomously terminates ATM Adaptation Layer standards Type 3/4 and Type 5. The device is ideally suited to applications in a variety of customer premises equipment such as ATM workstation Adaptor Cards and ATM Hubs. The device supports simultaneous segmentation and reassembly on up to 1024 virtual circuits (VCs).

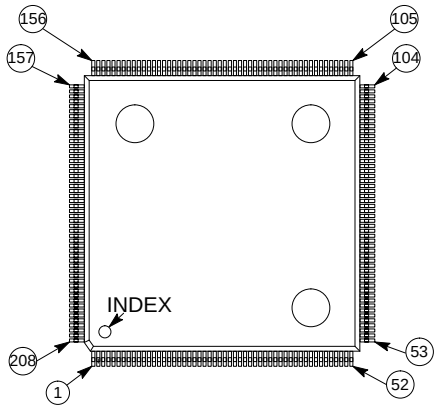
PLASTIC PACKAGE
SQFP208



FEATURES

- Supports Broadband ISDN Adaptation Layer standards Type 3/4 and Type 5.
- Supports simultaneous segmentation and reassembly on up to 1024 VCs.
- Supports up to 12 peak segmentation rates with leaky bucket averaging on a per VC basis with optional bucket fill before segmentation continues.
- Programmable peak and average rates and leaky bucket averaging on total ALC cell stream output.
- Support for scatter / gather mode.
- Transparent ATM cell and cell payload modes including support for OAM and Resource Management cells.
- UTOPIA v2.01 compliant cell stream interface with optional HEC checking on receive.
- Flexible routing tag append / remove mode for direct ATM Switch connection.
- Supports buffer chaining and buffer streaming.
- Supports buffer ageing time-out.
- Separate 32 bit data and 16 bit control ports with optimized DMA interface including 128 circuit cache to reduce DMA bus occupancy.
- Supports JTAG to IEEE1149.1
- Fabricated in sub–micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

APPENDICES

TABLES

FIGURES

FIGURES (CONTINUED)

FIGURES (CONTINUED)

1. OVERVIEW

The ALC simultaneously supports autonomous segmentation and reassembly of user data packets on up to 1024 virtual circuits (VCs).

User data packets are transferred to and from shared data structure memory using a high speed intelligent DMA controller with a 32 bit data bus.

Shared data structures are stored in SAR (Segmentation and Reassembly) memory which can be either dual port memory or a partition of system memory.

Packets for segmentation and packets being reassembled are stored in the SAR memory together with external data structures. These are accessed using the ALC's high speed intelligent DMA controller. In non-demanding applications, system memory can be used as SAR memory. When dual port memory is used the ALC's DMA controller has full access to the SAR memory bus. When system memory is used the DMA controller will negotiate access to a portion of the system bus bandwidth. The ALC provides the user with the facility to partition the shared data structures into dual port memory and user data into shared memory.

The DMA controller supports autonomous traffic shaping functions. Up to twelve different peak rate queues can be configured for packet segmentation. In addition each VC can be assigned to either 100%, 50% or 25% of the nominal peak rate.

In this way the user can select from one of 36 possible peak rates. Average rate management is in accordance with either the single or double leaky bucket averaging algorithms.

Fig. 1 shows three possible system configurations.

Adaptation Layer Support

The ALC autonomously terminates the protocols involved in segmenting and reassembling data streams conforming to Adaptation Layer Types 3/4 and 5. AAL 3/4 and AAL 5 traffic can be handled simultaneously. Streaming and Message Modes as defined for AAL 3/4 and AAL5 are supported.

In Message Mode, the Convergence Sublayer payload (Service Data Unit) is considered to be the user data transmitted from or received into a single entity. A single entity being regarded as one user data buffer or linked chain of user data buffers.

In Streaming Mode, the Convergence Sublayer payload is considered to be the user data transmitted from or received into multiple entities separated in time. This allows a partial segmentation or reassembly. In Streaming Mode the chaining of buffers is not supported.

The ALC Device supports two transparent modes. In transparent payload mode the 48 byte ATM cell payload is received or transmitted transparently into or from SAR Memory. In transparent cell mode the ATM cell is received or transmitted transparently into or from SAR Memory.

System Configurations

In adaptor card applications, the ALC interfaces to the Fujitsu MB86683 Network Termination Controller Device (NTC) (or compatible CCITT I.432 device) via a full duplex 8-bit wide UTOPIA compliant cell stream interface for connection to the transmission medium.

In Hub or Router applications, the ALC connects directly to the Fujitsu MB86680B Self-routing Switch Element (SRE) for autonomous routing. In this case a programmable Tag of 3 bytes must be appended to each cell.

Alternatively, it may be connected to a proprietary backplane architecture. To support this application the ALC can be configured to transmit and receive ATM cells with a four byte header minus the HEC field.

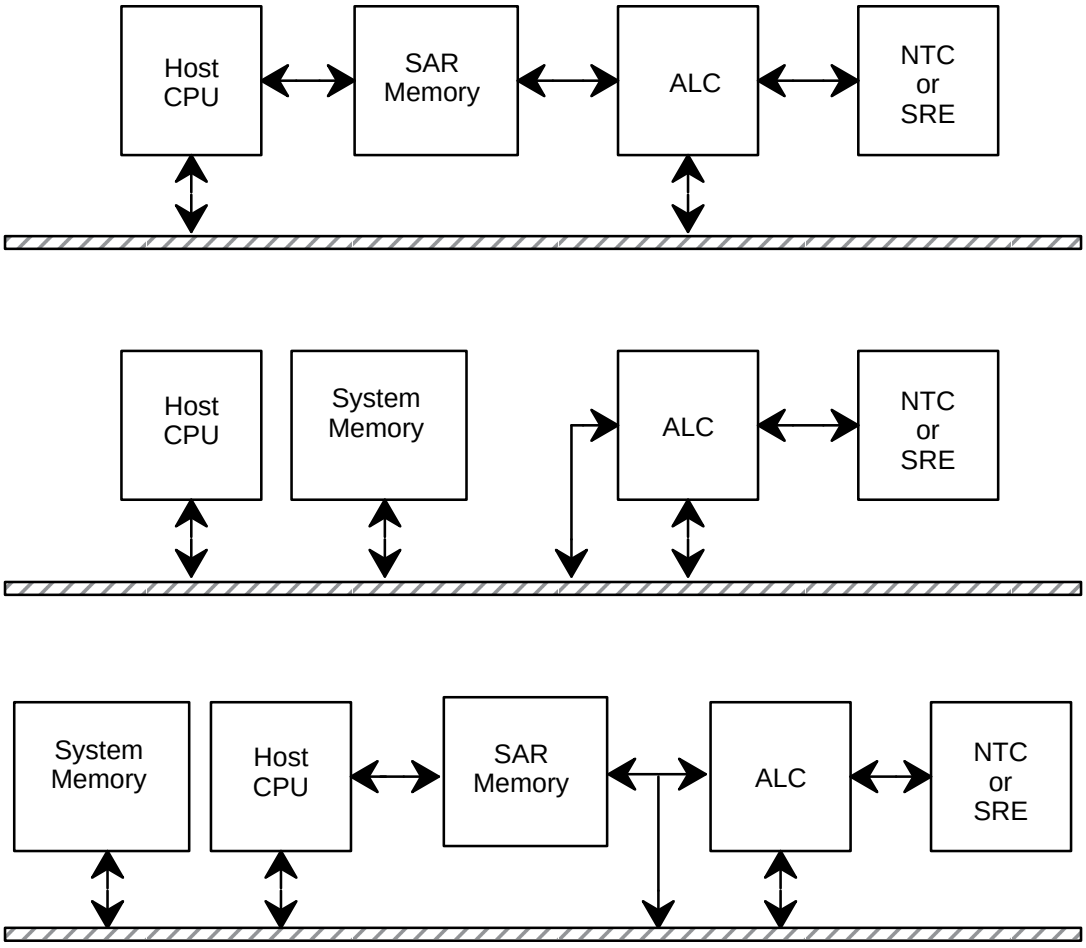


Fig. 1 – Possible System Configurations

2. EXTERNAL INTERFACES

2.1 Logical Outline

A logical view of the ALC's external pins is illustrated in Fig. 2, and a physical pin assignment is shown in Appendix F.

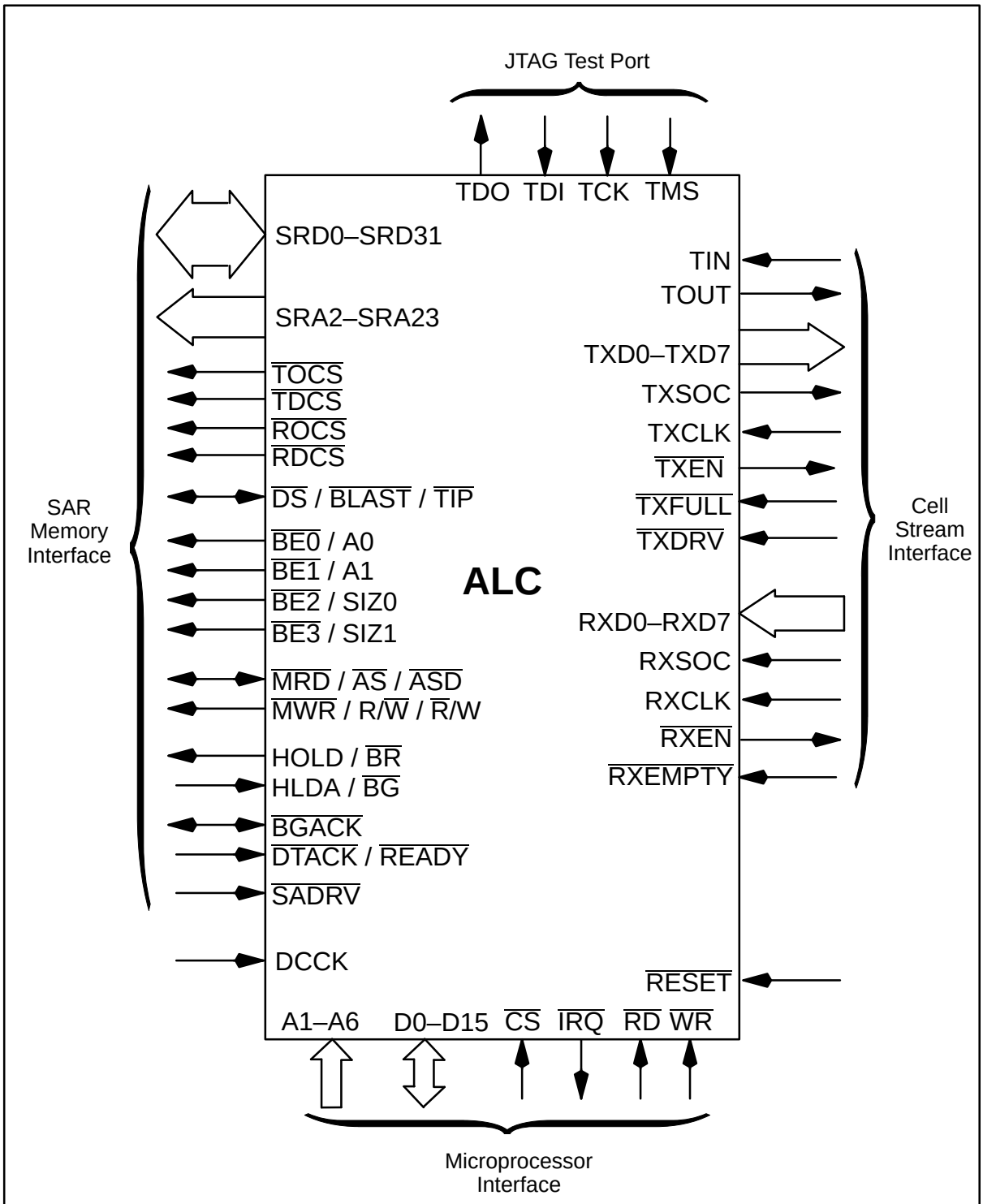


Fig. 2 – ALC External Interfaces

2.2 Detailed Description

2.2.1 SAR Memory Interface

This interface provides the ALC DMA controller with access to external dual port memory or shared access to system memory.

The interface comprises the following signals:

SRD0 – SRD31
Bi–directional SAR memory data bus.

SRA2 – SRA23
Most significant 22 bits of the SAR memory address bus. All bits are tri-state outputs.

$\overline{\text{SADRV}}$
This input allows the SAR memory interface to be permanently driven.

$\overline{\text{BE0}}$ / SRA0
Multifunction tri-state output. Functions are as follows:

- Intel mode:
  $\overline{\text{BE0}}$: Byte Enable 0
  Enables data byte on
  SRD0 – SRD7,
- Motorola mode
  SRA0: SAR Memory Address bus bit 0.

$\overline{\text{BE1}}$ / SRA1
Multifunction tri-state output. Functions are as follows:

- Intel mode:
  $\overline{\text{BE1}}$: Byte Enable 1
  Enables data byte on
  SRD8 – SRD15.
- Motorola mode
  SRA1: SAR Memory Address bus bit 1.

$\overline{\text{BE2}}$ / SIZ0
Multifunction tri-state output. Functions are as follows:

- Intel mode:
  $\overline{\text{BE2}}$: Byte Enable 2
  Enables data byte on SRD16 – SRD23,
- Motorola mode
  SIZ0.

$\overline{\text{BE3}}$ / SIZ1
Multifunction tri-state output. Functions are as follows:

- Intel mode:
  $\overline{\text{BE3}}$: Byte Enable 3
  Enables data byte on
  SRD24 – SRD31,
- Motorola mode
  SIZ1.

The coding of the SIZ signals has the following meaning:

SIZ1	SIZ0	Meaning
0	1	Burst of 8
1	0	Word
1	1	Burst of 4
0	0	Long Word

$\overline{\text{MRD}}$ / $\overline{\text{AS}}$ / $\overline{\text{ASD}}$
Bi-function tri-state bi-directional signal. SAR memory read signal (Intel mode), SAR memory address strobe (Motorola mode). This signal is used as an input during Motorola mode bus arbitration and is the $\overline{\text{ASD}}$ signal in extended modes.

$\overline{\text{MWR}}$ / R/$\overline{\text{W}}$/ $\overline{\text{R}}$/W
Multifunction tri-state output. SAR Memory write signal (Intel mode), SAR Memory read/$\overline{\text{write}}$ signal (Motorola modes) and $\overline{\text{read}}$/write (Intel Extended mode).

DS / $\overline{\text{BLAST}}$ / $\overline{\text{TIP}}$
Multifunction tri-state output. Data Strobe in Motorola mode; $\overline{\text{BLAST}}$ (last in burst) in Intel extended mode; $\overline{\text{TIP}}$ (transmission in progress) in extended Motorola mode.

$\overline{\text{TOCS}}$
Transmit Overhead Cycle Start output. This is asserted before any transmit cycle that is not a data cycle.

$\overline{\text{TDCS}}$
Transmit Data Cycle Start output. This is asserted before a transmit data cycle.

$\overline{\text{ROCS}}$
Receive Overhead Cycle Start output. This is asserted before any receive cycle that is not a data cycle.

$\overline{\text{RDCS}}$
Receive Data Cycle Start output. This is asserted before a receive data cycle.

HOLD / $\overline{\text{BR}}$
Tri-state Hold/Bus request output used to request bus access for ALC DMA controller.

HLDA / $\overline{\text{BG}}$
Hold/Bus Grant input used to pass control of the bus to the ALC DMA controller.

$\overline{\text{BGACK}}$
Bus Grant Acknowledge output indicates ALC DMA controller is assuming control of the bus.

$\overline{\text{READY}}$ / $\overline{\text{DTACK}}$
Ready/Data Transfer Acknowledge input. In standard mode used to terminate DMA / DPR cycles. In FAST mode used to generate an ALC interrupt indicating memory access conflict.

DCCK, DMA CYCLE CLOCK
Clock input used to drive the ALC DMA cycles.

2.2.2 Microprocessor Interface

The microprocessor interface comprises the following signals:

A1–A6
Microprocessor address bus inputs.

DATA0–DATA15
Bi-directional microprocessor data bus signals DATA 0–15.

$\overline{\text{CS}}$
Microprocessor bus chip select input.

$\overline{\text{RD}}$
Microprocessor bus read input.

$\overline{\text{WR}}$
Microprocessor bus write input.

$\overline{\text{IRQ}}$
Interrupt request output.

$\overline{\text{RESET}}$
ALC master reset input.

2.2.3 Cell Stream Interface

This interface comprises the following signals:

TXD0–TXD7
These tri–state output signals provide 8 bit parallel transmit data which is cell aligned and asynchronous. To enable daisy chaining of ALCs these signals are tri-state.

TXSOC
Transmit start of cell sync output. This tri –state output indicates that the first byte of an ATM cell or routing tag is available on the TXD0 – TXD7 data lines. The frequency of this signal depends on the cell transmission rate from the ALC. To enable daisy chaining this pin is tri-state.

TXCLK
This input signal is used to clock transmit data out of the ALC. The signal can be of arbitrary frequency but should be sufficient to support the bandwidth specified by the ALC traffic shaping parameters. No phase relationship is assumed with RXCLK.

$\overline{\text{TXEN}}$
This tri–state output signal is asserted in UTOPIA mode when the cell stream transmit is outputting valid data.

$\overline{\text{TXFULL}}$
This input is used in UTOPIA mode to halt the ALC transmit cell stream data.

RXD0–RXD7
These 8 input pins provide the ALC with 8 bit parallel, cell aligned receive data.

RXSOC
Receive start of cell sync input. This signal indicates when the first byte of an ATM cell or routing tag is available on the RXD0 – RXD 7 pins.

RXCLK
This input signal is used to clock received data into the ALC. No phase relationship is assumed with TXCLK.

$\overline{\text{RXEN}}$
This output signal is used in UTOPIA mode to control the flow of receive cells when using an external FIFO. The signal indicates that the ALC receive buffers are full.

$\overline{\text{RXEMPTY}}$
This input signal is used to control the flow of receive cells when using an external FIFO. The signal indicates that the FIFO is empty.

TOUT
Token out output. This signal is used to enable daisy chaining. The ALC transmits a ‘token’ pulse on the falling edge of TXCLK to indicate that it has completed a cell transfer or has no data to transmit. The output is held low during cell transmission.

TIN
Token In input. This input should be wired to the TOUT output of other ALC devices to form a daisy chain. If unused this pin should be pulled high.

$\overline{\text{TXDRV}}$
This input allows the ALC to permanently drive the transmit cell stream interface

2.2.4 JTAG Test Port

TCK
JTAG test clock input

TDI
JTAG test data input

TMS
JTAG test mode input

TDO
JTAG test data output

SIGNAL	PULL	VALUE	COMMENT
The following are essential for correct operation			
$\overline{\text{BGACK}}$	High	2K7	DMA mode
	High	10K	Dual Port Memory mode
$\overline{\text{IRQ}}$	High	2K7	
TXSOC	Low	10K	Only when $\overline{\text{TXDRV}}$ is not asserted
$\overline{\text{TXEN}}$	High	10K	Only when $\overline{\text{TXDRV}}$ is not asserted
HOLD/$\overline{\text{BR}}$	Low	2K7	Only in Intel DMA mode
	High	2K7	Only in Motorola DMA mode
$\overline{\text{MRD}}$/$\overline{\text{AS}}$	High	10K	DMA mode *
	High	100K	Dual Port Memory mode
HLDA/$\overline{\text{BG}}$	High	10K	
$\overline{\text{DS}}$	High	100K	
The following are not essential, but are advisable			
TXD0–7	High/Low	100K	Only when $\overline{\text{TXDRV}}$ is not asserted
SRD0–31	High	100K	Only when $\overline{\text{SADRV}}$ is not asserted
The following can be omitted if the data bus can be guaranteed not to float between 2.2v and 0.8v.			
$\overline{\text{MWR}}$/R/$\overline{\text{W}}$	High	100K	*
$\overline{\text{BE0}}$/A0	High	100K	*
$\overline{\text{BE1}}$/A1	High	100K	*
$\overline{\text{BE2}}$/SIZ0	High	100K	*
$\overline{\text{BE3}}$/SIZ1	High	100K	*
A2–21	High	100K	*

Note: * – These signals are continuously driven when Dual Port Ram mode is selected or $\overline{\text{SADRV}}$ is asserted.

Table 1 – Pull Values

3. FUNCTIONAL DESCRIPTION

This section describes the behaviour of each major functional block within the ALC, as illustrated in Fig. 3. The descriptions in this section are from a user's perspective and are intended to give a detailed description of device functionality and modes of operation. The ALC comprises the following major components:

- High Speed DMA Controller,
- Traffic Management Controller,
- Transmit and Receive Buffers,
- Segmentation and Convergence Sub-layer Controller,
- Reassembly and Convergence Sub-layer Controller,
- Cell Stream Interface,
- Microprocessor Interface,
- Segmentation and Reassembly Memory Interface.

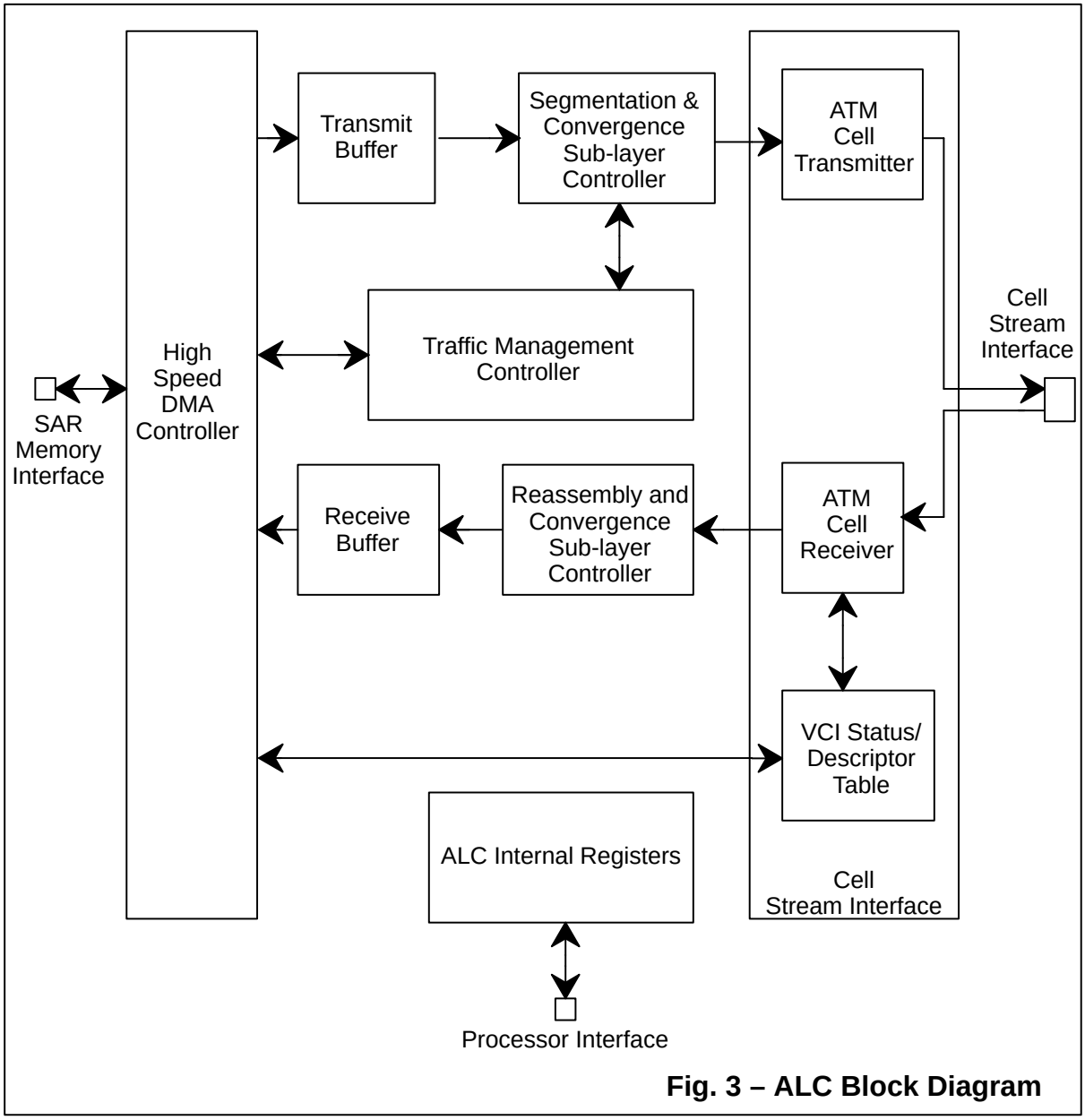


Fig. 3 – ALC Block Diagram

3.1 DMA Controller and SAR Memory Interface

3.1.1 General

The ALC contains an intelligent DMA Controller to manage the segmentation and reassembly of user data packets using the minimum of host processor intervention. Communication with the host processor is mainly through shared data structures in either dual port or system memory.

The system implications of a dual port or system memory approach are largely performance related.

3.1.2 Shared Data Structures

The shared data structures used to control the segmentation and reassembly of user data are shown in Fig. 4 on page 10. The transmit side is controlled via the Transmit Pending Queue, the Transmit Descriptor Table, the Circuit Reference Table and the Transmit Buffer Release Queue. The ALC uses reserved fields in the Transmit Descriptor to compose peak rate queues for segmentation at the specified peak rate and for leaky bucket averaging. The host can programme up to 12 peak rates for the ALC.

The receive side is controlled by the Receive Buffer Free Queue, the Receive Descriptor Table and the Receive Buffer Ready Queue. In addition the DMA Controller uses an internal RAM table, the Receive Status / Descriptor Table to store receive VCI status and descriptor identifiers. The purpose of each of these tables is described below.

3.1.3 Transmit Data Structures

The host writes commands to the Transmit Pending Queue to instruct the ALC to queue a data packet for segmentation. The packet can be queued for transmission on one of 12 peak rate queues. Each Transmit Pending Queue entry contains a pointer to a Transmit Descriptor in the Transmit Descriptor Table.

The Transmit Descriptor Table is composed of up to 4096 descriptors. Each descriptor contains a pointer to data for segmentation. The reserved fields in the Transmit Descriptor are used by the ALC to construct queues of transmit packets for each selected peak rate. The Transmit Descriptor also contains a pointer to an entry in the Circuit Reference Table (CRT).

The CRT is composed of up to 1024 entries, one entry for each active Virtual Circuit. Each entry contains fields for the ATM cell header, an optional routing tag, and the leaky bucket parameters for the virtual circuit. The ALC reads the cell header and the leaky bucket parameters from the CRT each time a cell is segmented from a transmit buffer.

Management of the Peak Rate segmentation queues is handled autonomously by the ALC. The only host intervention required is on a per packet basis. To queue a packet the host constructs the relevant descriptor and writes the pointer to the descriptor into the Transmit Pending Queue. Transmit descriptors are recovered by the host by reading the Transmit Buffer Release Queue.

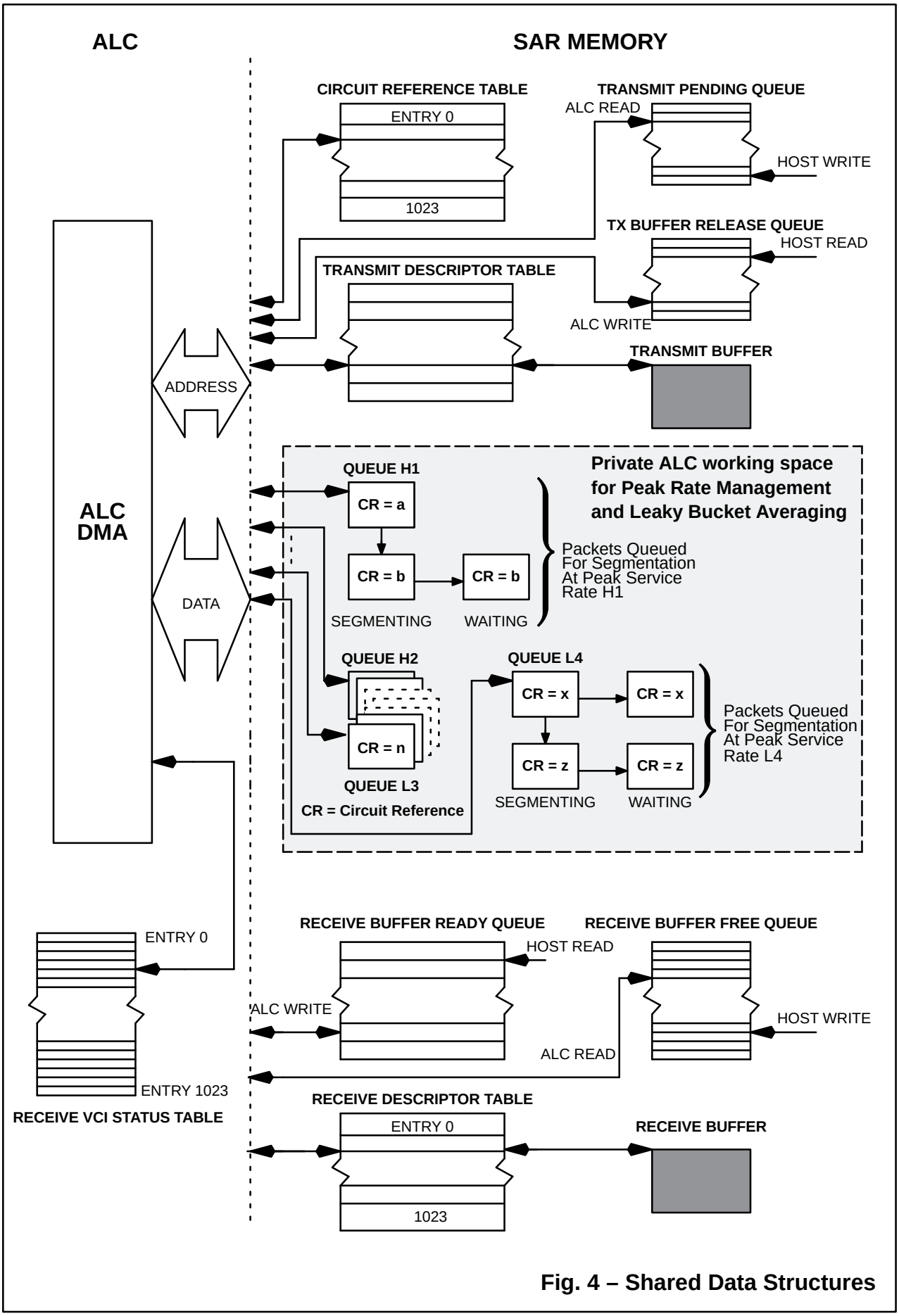


Fig. 4 – Shared Data Structures

After a packet has been transmitted, the ALC will return the Transmit Descriptor used to the host via the Transmit Buffer Release Queue. Each entry in this queue contains a pointer to the relevant descriptor in the Transmit Descriptor Table.

3.1.4 Receive Data Structures

At the start of reassembly for each new packet the ALC finds a new Receive Descriptor (RD) by reading the Receive Buffer Free Queue. Each entry contains a pointer to a RD in the Receive Descriptor Table.

The Receive Descriptor Table is composed of up to 4096 RDs. Each RD contains a pointer to a receive buffer. The RD also contains fields to support receive buffer chaining and the received VCI or MID fields. A reserved field in the RD is used by the ALC to support a receive buffer ageing timeout.

After reception is complete, the ALC passes the receive descriptor to the host using the Receive Buffer Ready Queue. Each entry in the queue contains a pointer to the appropriate RD and the status of the receive buffer.

A more detailed description of the shared data structures is provided in Section 4, Developers Notes, of this datasheet.

3.1.5 Packet Segmentation

The DMA Controller is responsible for linking transmit descriptors into one of the 12 service rate queues. The queues are composed of a linked list of TDs. The structure of each of the service rate queues is shown in Fig. 5.

When the ALC reads a transmit packet command from the Transmit Pending Queue, it links the packet into the service rate queue specified in the appropriate Circuit Reference Table entry (see Fig. 20 on page 36).

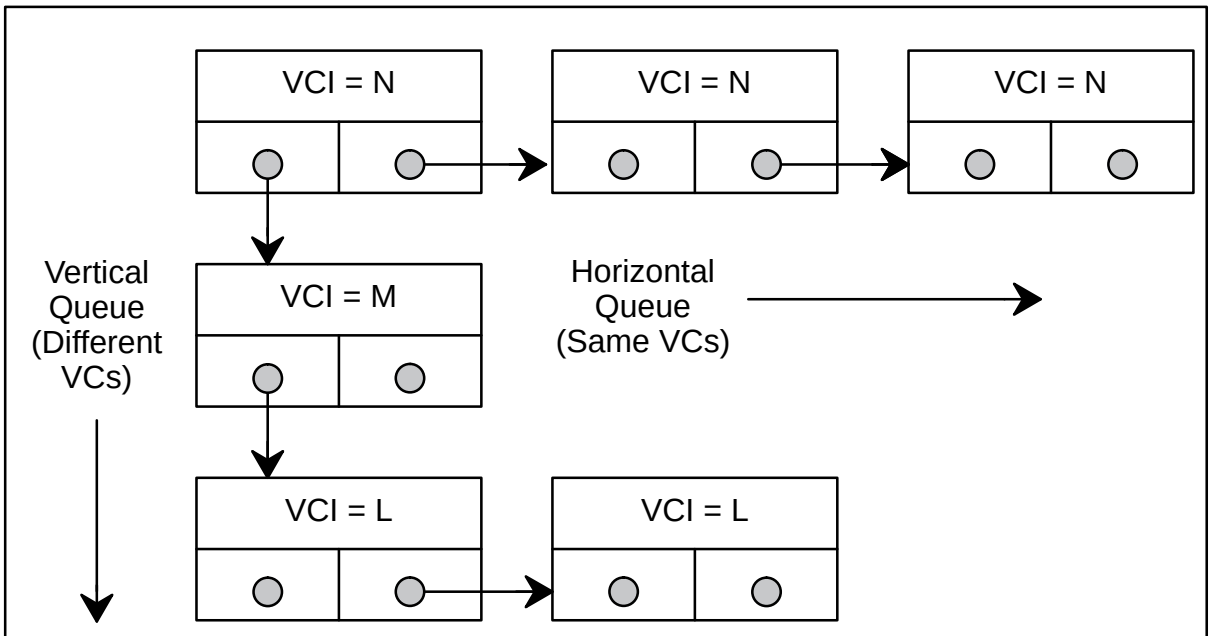


Fig. 5 – Transmit Queue Structure

Packets with the same circuit reference, ie same VPI/VCI or MID are queued horizontally. Packets with different circuit references for transmission on the same service rate queue are queued vertically. Horizontally queued packets will be serviced when the packet at the front of the queue is completed.

Each service rate queue is serviced vertically at the specified peak rate under the control of the Traffic Management Controller. A queue entry has been serviced when a complete SAR–PDU payload of either 44 or 48 bytes has been read from the packet. The queue has been serviced when each queue entry linked vertically has been serviced.

Message Mode Operation

In Message Mode, the user data buffer associated with a Transmit Descriptor will contain the full CS–PDU payload to which the CS–PDU header and trailer will be added to terminate the protocol.

Alternatively, the CS–PDU payload may

Streaming Mode Operation (PR)

The size of the CS–PDU payload may be much greater than the size of one receive data buffer. In addition, the memory resource as a whole may be limited or the user may require that sections of the CS–PDU be forwarded to the host as soon as they fill each buffer.

This partial reassembly is accomplished by programming the ALC for streaming mode operation.

Buffer Chaining is not possible when the streaming mode register bit has been programmed.

		MESSAGE MODE		STREAMING MODE
OPERATION	DIR	SINGLE BUFFER	CHAINING	
Queue Packet	Tx	M=0, $\overline{CS}$=0, $\overline{CE}$=0 Whole packet in single buffer	M=0 $\overline{CS}$ 1st buffer=0 $\overline{CS}$ other buffers=1 $\overline{CE}$ last buffer=0 $\overline{CE}$ other buffers=1	M=1, $\overline{CS}$=0 in first buffer $\overline{CE}$=0
Add buffers via TPQ *	Tx	NA	NA	M=1 in extra buffers M=0 in last buffer $\overline{CE}$=0
Release buffer	Tx	When packet Tx complete	Released on a buffer by buffer basis (–> TRBQ)	Released on a buffer by buffer basis (–> TRBQ)
Start Re-assembly	Rx	BCHAIN=O, SMODE=O Get next BFQ entry	BCHAIN=1, SMODE=0 Get next BFQ entry	BCHAIN=O, SMODE=1 Get next BFQ entry
Buffer full	Rx	Error buffer overflow	Get next BFQ entry Link buffers	Get next BFQ entry Release buffer to host (–> RBRQ)
Packet complete	Rx	Release buffer to host	Release first buffer to host (–> RBRQ) **	Release buffer to host (–> RBRQ)

Notes:

*** In Transmit Streaming mode the host must queue all current packet buffers on any given circuit before starting a new packet.**

**** In Receive Chaining the host will be given the descriptor reference of the first buffer in the chain. The host must follow the chain until the condition V=0 is set in the descriptor.**

Table 2 – Single Buffer, Chaining and Streaming Modes

Buffer Ageing Support

Buffer Ageing support is programmed by setting bit D12 (BAS) in Register 17. If set, upon reassembling the first cell of a packet, the ALC stamps a time base in the RD.

On reassembly of further cells for the same packet, the ALC compares the time elapsed against the value programmed in Register 52 – Receive Buffer Timeout Counter Register.

If the difference is greater than the value in this register, the RD is returned to the Buffer Ready Queue with a code ‘1100’ indicating Buffer Timed Out – Reassembly Aborted. The rest of the packet will be discarded by the ALC

For a greater time range, Register 51 – Receive Buffer Timeout Counter Period Register – can be programmed. This scales the DCCK used to increment the time base counter. For example, a DCCK at 25MHz provides a time range up to 170 seconds.

Buffer Ageing Support is only available in Message Non–Chaining mode.

Maximum Packet Length

At the start of cell reassembly, the ALC compares the value of Bytes Received accumulated in the RD with the value programmed in Register 54 – Maximum Received Packet length Register.

If the register value is exceeded, the ALC writes out the RD to the Buffer Ready Queue with a code ‘1001’ indicating Receive Maximum Length Exceeded.

For Message Chaining mode, the ALC compares the accumulated value of Bytes Received to date across the chain at the moment of adding a further RD to the chain.

Maximum Packet Length checking is not supported in Streaming mode

3.2 Traffic Management Controller

The Traffic Management Controller is responsible for the following functions:

- Initiate periodic packet segmentation from one of the 12 Peak Rate Queues at intervals specified in the Queue Service Rate registers. The queues are grouped into three priority classes: high, medium and low, with 4 queues in each priority class.
- Manage total ALC peak transmission rate. If the total peak transmission rate exceeds a specified threshold, the traffic management controller will service the queues according to their priority until the total peak rate falls below the threshold. This feature can be used to ensure that the ALC will not exceed the negotiated quality of service for the overall link connection.
- Manage average rate shaping of transmit traffic on a per virtual circuit basis using the leaky bucket algorithm. The leaky bucket parameters for this are supplied from the Circuit Reference Table referenced in the Transmit Descriptor.
- Manage average rate shaping on the total ALC transmission according to the leaky bucket algorithm. The leaky bucket parameters for this averaging are determined by the ALC Peak Cell Transmission and ALC Average Cell Transmission registers. This feature is also used to ensure that the ALC will not exceed the quality of service for the overall connection.

3.2.1 Peak Rate Queue Service Requests

The ALC peak rate queue service control logic is responsible for requesting the transmission of cells queued to the peak rate queues on a per virtual circuit basis. Twelve programmable counters are used to specify the peak transmission rate for each queue.

The twelve counter values are programmed using the Queue Service Rate Registers and enabled using the Queue Enable Registers. The counter is clock TXCLK (for TXCLK period, see Appendix D.) which can be pre-scaled to increase it’s dynamic range. The peak service rate value is used to determine the frequency of access to the respective peak rate queue. Each time the queue is accessed one cell may be transmitted for each queued entry (one per VC) if a leaky bucket token is available for that queue entry.

Each Circuit Reference Table contains a sub rate select field which can be used to further reduce the peak cell transmission rate to 50% or 25% of the nominal peak rate specified in the Queue Service Rate Register. This gives a total available range of 32 effective peak transmission rates for entries of each peak rate queue.

3.2.2 Total ALC Peak Rate Control

The ALC contains link capacity control logic which is used to ensure that the overall ALC link transmission rate does not exceed a pre-programmed value as specified in the ALC Peak Cell Transmission Rate register.

If the overall required transmission rate exceeds this programmed value, the link capacity controller will mask the lower priority queues. This will cause cell transmission to cease on the low priority queues until the overall peak rate falls below the programmed total ALC value. Note that the queues are masked in the following priority: All four L queues followed by all four M queues.

3.2.3 Per VC Leaky Bucket Traffic Shaping

The leaky bucket algorithm is used to shape the transmit data characteristics on a per virtual circuit basis by controlling the average rate of cell transmission and the length of each burst of cells generated. The leaky bucket parameters are determined by the values in the Circuit Reference Table for each active VC. (See section NO TAG, Transmit Data Structures).

The parameters relevant to leaky bucket management are the user programmable parameters, Bucket Capacity M and the Bucket Utilization U.

The bucket capacity is used to calculate the maximum sustained burst of cells at the specified peak rate. The average rate of emptying the bucket is derived from the utilisation.

The utilisation is expressed as a fraction of the peak rate. See section 4 on ALC configuration and control for full details.

Two modes of operation are supported: single leaky bucket mode and double leaky bucket mode.

In single leaky bucket mode, cells are transmitted in an initial burst as defined by M at the specified peak rate. The burst length may exceed the bucket capacity since tokens are added to the bucket at the same time as tokens are removed. Subsequent cells are transmitted at the average rate as tokens are added to the bucket.

In double leaky bucket mode, cell transmission will only occur in bursts at the peak rate when the bucket associated with that VC is full of tokens.

3.2.4 Total ALC Leaky Bucket Traffic Shaping

In addition to the traffic shaping applied to the traffic transmitted from each virtual circuit the ALC can manage both the peak and average transmission rate on the total ALC output traffic.

A total ALC Leaky bucket size is defined in the ALC Leaky Bucket Capacity Register. This capacity value is used in conjunction with the leaky bucket utilization to limit the ALC output burst length. The total ALC utilisation value is derived from the ALC Peak Cell Rate and ALC Average Cell Rate Register contents.

3.3 Segmentation and Convergence Sub-layer Controller

This block is responsible for managing the transmission of cells according to the specified Adaptation Layer protocol: AAL3/4 or AAL5.

3.3.1 SAR Sub-layer functions

Fig. 6 shows the format of SAR Protocol Data Units (SAR–PDU) for AAL types 3/4 and 5. The following protocol actions are performed on each SAR–PDU for AAL 3/4:

- Preservation of SAR service data unit integrity through generation of the segment type field,
- Error Protection through Sequence Number and CRC generation,
- Multiplexing/Demultiplexing using the Multiplexing ID,
- Support of the Abort function.

The fields of AAL Type 3/4 are detailed in the following text.

ST, Segment Type
The first SAR–PDU generated from a user data packet carries the Beginning of Message (BOM) code 10. Subsequent SAR–PDUs carries the (Continuation Of Message) COM code 00.

The final SAR–PDU carries the End of Message (EOM) code 01. SAR–PDUs which carry entire SAR–SDUs such as those defined for signalling carry the Single Segment Message (SSM) code 11.

SN, Sequence Number
The four bits of this field are used for modulo 16 numbering of each SAR–PDU. The Sequence Number is set to zero at the start of each SAR–SDU.

MID, Multiplexing Identification
This field is used for multiplexing multiple CS–PDU (Convergence Sub-layer Protocol Data Units) connections on a single ATM layer connection. When MID mode is selected, this field carries the MID specified in the Circuit Reference Table. The MID field is set to zero when multiplexing is not used.

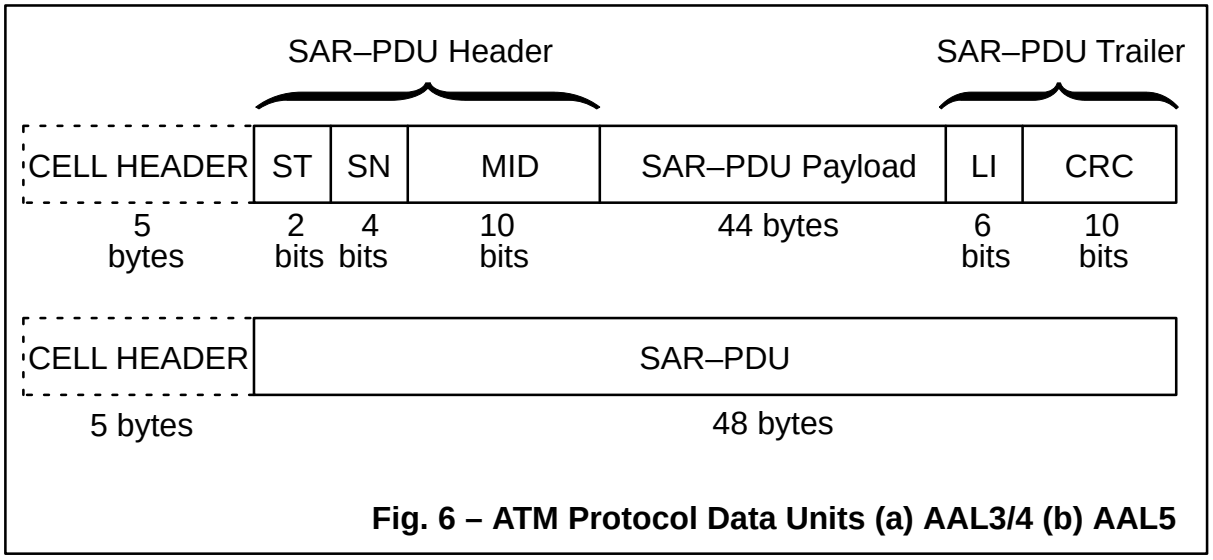


Fig. 6 – ATM Protocol Data Units (a) AAL3/4 (b) AAL5

LI, Length Indicator
This field indicates the number of bytes contained in the SAR–PDU. The SAR–SDU bytes are left justified within the SAR–PDU payload field and remaining bytes will be set to 0.

CRC, Cyclic Redundancy Check
This field contains the 10 bit CRC code. It is calculated (as defined in CCITT I.363 for AAL3/4) over the SAR–PDU including header, trailer, payload and length indication.

3.3.2 Convergence Sub-layer Functions

Fig. 7, below, shows how the user data is formatted in the convergence sub-layer before segmentation. The ALC maintains internal tables to manage AAL3/4 sequence numbers and AAL5 CRC results.

The fields of the CS–PDU header and trailer are listed and described on the following pages.

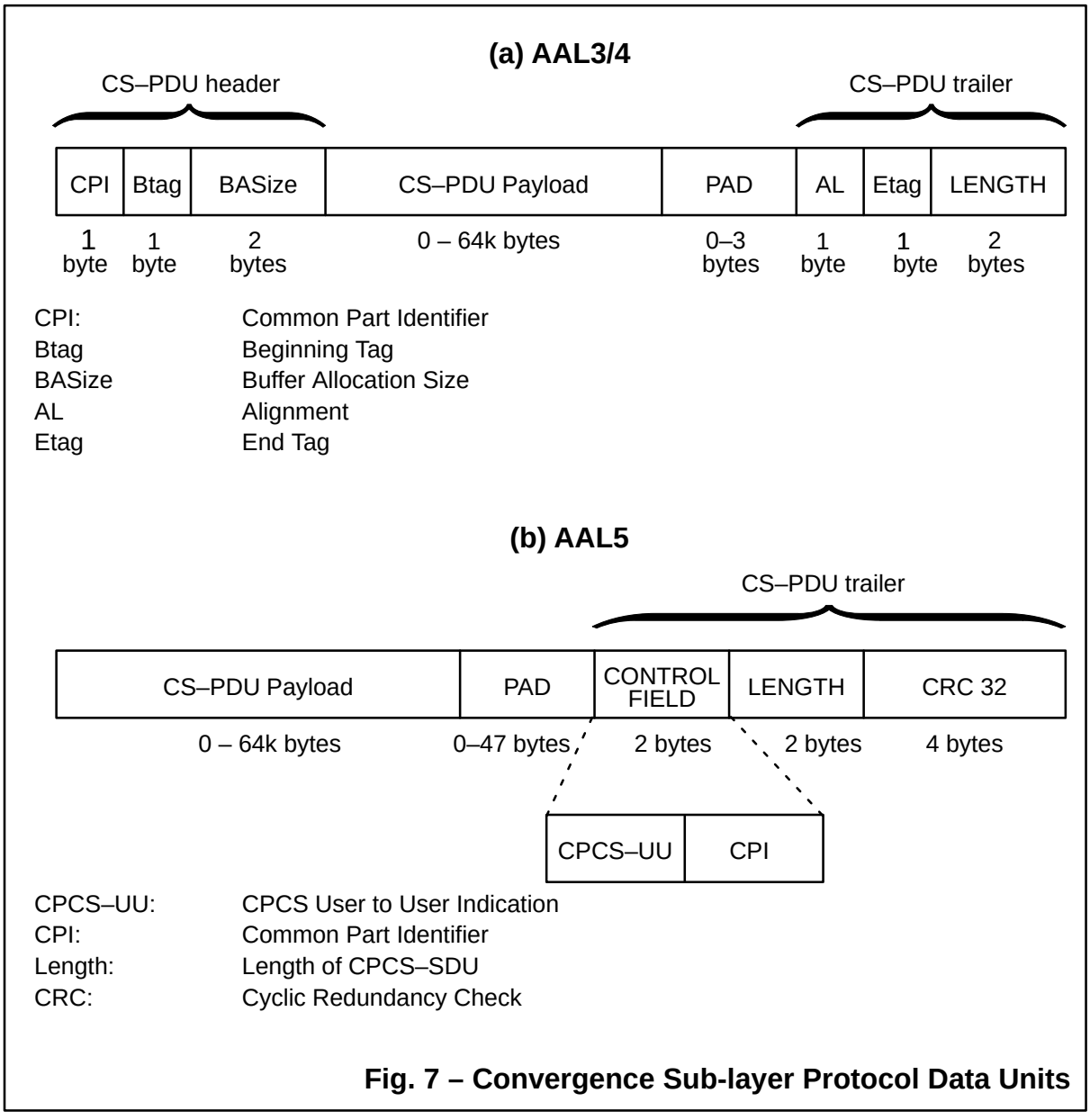


Fig. 7 – Convergence Sub-layer Protocol Data Units

AAL 3/4 HEADER AND TRAILER

CPI, Common Part Identifier
This field is coded to all zeros to indicate that the values in BASize and Length Fields are measured as unit multiples of bytes.

BTAG, ETAG, Beginning & End Tags
These Fields are given the same modulo 256 value for each CS–PDU and incremented on successive CS–PDUs. The receiver will check that they are the same value on a CS–PDU to CS–PDU basis but will not check for incrementation over successive CS–PDUs.

BASize, Buffer Allocation Size
This value will be the size of the CS–PDU payload when Message Mode Service is being run. In Streaming Mode this value may be greater than or equal to the CS–PDU payload size. Its purpose is to inform the receiving entity of the buffering required to accommodate the transmitted data.

AL, Alignment
No information is conveyed by this field. It merely provides 32 bit alignment in the CS–PDU trailer. The Pad field has the effect of making the CS–PDU an integral multiple of 4 bytes.

Length
Length of CS–PDU payload.

PAD, Padding Field
This field complements the CPCS–PDU to an integral multiple of 4 bytes and conveys no information.

AAL 5 TRAILER
For AAL 5 the CS–PDU has no header. The trailer is derived from the data structure and the 32 bit CRC stored in the convergence sub-layer table. The fields of the CS–PDU trailer are listed below.

PAD, Padding Field
The purpose of the PAD bytes is to align the CS–PDU trailer into the last 8 bytes of a SAR–PDU. If this calculation results in the transmission of an extra cell it is not transmitted back to back with the previous SAR–PDU, as this would compromise the transmission rate and the Traffic Management Controller parameters.

Control Field
The Control Field comprises 2 fields shown in Fig. 7. These fields are:

- CPCS–UU
  This field is used to transparently transfer CPCS user to user information.
- CPI
  This field is used to align the CPCS_PDU to 64 bits and should be coded as zero.

Length
Length of CS–PDU payload.

CRC, Cyclic Redundancy Check
The CRC field is filled with the value of a CRC calculation (as defined in CCITT I.363 for AAL 5) which is performed over the entire contents of the CS–PDU. This includes the payload, the PAD field, and the first four bytes of the trailer. The initial CRC remainder is preset to all ones before generation and checking.

3.3.3 Error Recovery & Notification

The ALC provides provisions for sending SAR–U–ABORT ATM Cells in streaming mode in accordance with the selected protocol. In accordance with AAL5 protocol the ABORT SAR–PDU is defined as SDU=1, LENGTH FIELD coded to zero and CRC32 correct. In accordance with AAL3/4 protocol the ABORT SAR–PDU is defined by ST= EOM, payload coded to zero, and LI = 63. The CRC–10 and MID field must be valid.

3.3.4 Transparent Modes

Transparent Cell Mode

In this mode the host provides cells of 52 bytes (4 header and 48 data) in a transmit descriptor to the transmit pending queue. The transmit side generates and includes the HEC byte (if mode register 17 bit D9 = 0) and transmits the resulting 53 byte cell with an optional CRC10 included otherwise no further protocol carried out.

On receiving a transparent cell the receive side checks and removes the HEC byte before loading the remaining 52 bytes into the internal receive buffer. The receive side DMA then obtains a descriptor from the buffer free queue, writes all 52 bytes into the buffer and then writes out the descriptor to the buffer ready queue.

Note that the only updated field within the receive descriptor is the VCI field (the bytes received is not updated as it is always 52).

Transparent Payload Mode

In this mode the host provides a multiple of 48 bytes of cell payload data within a single transmit descriptor to the transmit pending queue. The header information is obtained from the Circuit reference table, a HEC byte is generated (if mode register 17, bit 9 = 0) and the cell is transmitted. As with transparent cell mode, apart from including an optional CRC10, no further protocol is performed.

The receive operation is also similar to transparent cell mode but with only the 48 payload bytes being transfered by DMA to SAR memory. The CRC 10 can be checked if the cell is detected to be an OAM or Resource management cell.

3.4 Reassembly and Convergence Sub-layer Controller

This block is responsible for managing the reception of cells according to the specified Adaptation Layer protocol: AAL3/4 or AAL5.

The following adaptation layer functions are performed on a SAR–PDU basis:

- Preservation of SAR service data unit.
  Checking the Segment Type Field,
- Error Detection and Handling.
  CRC and Sequence Number Integrity Checking,
- Multiplexing / Demultiplexing using the MID field,
- Support of the Abort Function.

The following adaptation layer functions are performed on a CS–PDU basis:

- Detection of BTag, ETag fields,
- Detection of Incorrect Length Field,
- Detection of Alignment errors,
- Detection of errors using CRC 32 calculation.

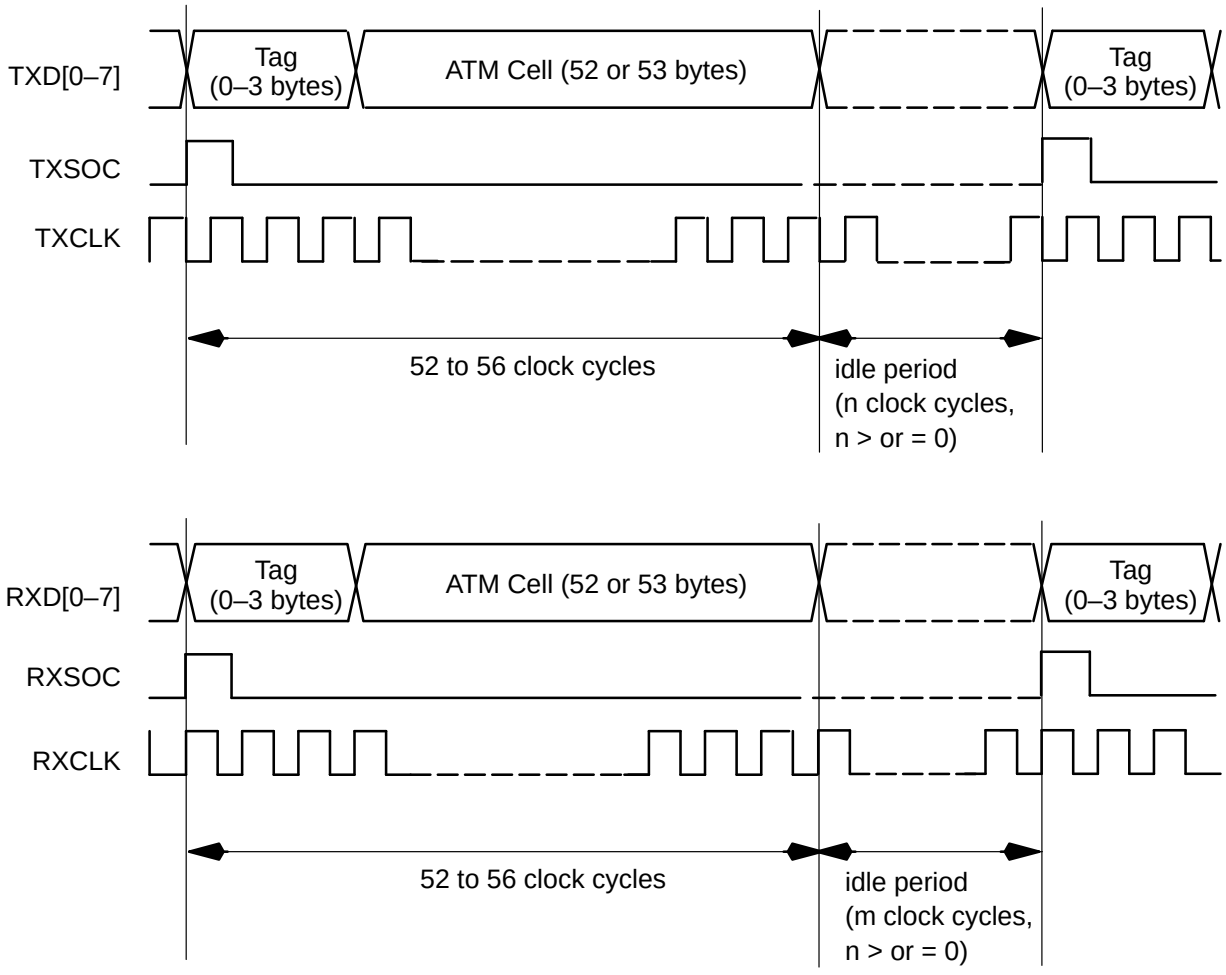


Fig. 8 – Cell Stream Interface

3.5 Cell Stream Interface

The Cell Stream Interface will transmit and receive an asynchronous stream of ATM cells. Cells will be transmitted and received in 8-bit parallel form with separate synchronisation signals used to identify the start of a cell.

The ALC cell stream interface may be required to operate in one of two environments either in a Switch Device or a Termination Device.

3.5.1 Termination Device Operation

In termination device operation the ALC is intended to connect to the Fujitsu MB86683 Network Termination Controller or equivalent device for physical media interfacing. Cells are transmitted and received header to trailer or with an idle period between each cell, see Fig. 8.

The idle period may be of any number of clock cycles including zero. There is no relationship between the transmit and receive sync pulses.

3.5.2 Switch Device Operation

In switch device operation, for example in hub and router applications, the ALC can be connected directly to an ATM switch fabric port such as the Fujitsu MB86680B Self–routing ATM Switch Element, or to a proprietary backplane structure.

In this environment the ALC will append a programmable routing Tag of up to 3 bytes to the start of each cell. In the receive direction the Tag is removed before protocol processing of the cell commences. In addition, the HEC field can optionally be omitted resulting in a 52 byte cell. Switch Device timing is also shown in Fig. 8.

3.5.3 Cell Stream and UTOPIA

The Fujitsu Cell Stream mode has been superceded by the UTOPIA specification from the ATM Forum, but is still supported for backward compatibilty. The mode selection is performed by tying the CS/$\overline{UT}$ pin high or low as required. By default, Fujitsu cell stream is selected by internal pull–up resistor.

3.5.4 Utopia Flow Control

Forward and backward byte-level flow control is supported in both directions. The forward flow control signal indicates the validity of the current data. The backward flow control signal indicates whether data will be accepted in a particular cycle. Neither flow control signal is directly qualified by the other : they can change state independently. Unused flow control inputs should be tied off to their active levels. All signals are transmitted and sampled on the rising edge of the clock.

Timings for UTOPIA are illustrated in Fig. 10 and Fig. 11. Note that all of the flow control signals can change state independently.

3.5.5 Cell Stream Flow Control

In Cell Stream mode the ALC will provide an indication that its receive buffer is full by using the $\overline{RXEN}$ output signal as shown in Fig. 9. The other flow control signals are not supported in Cell Stream mode.

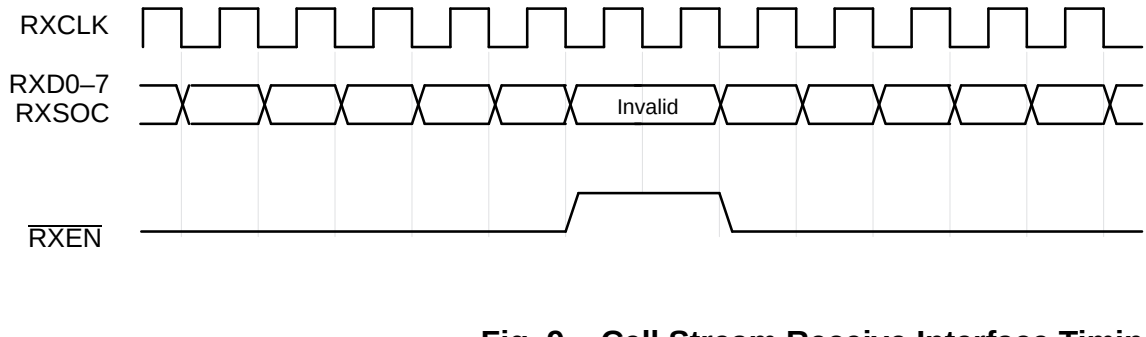


Fig. 9 – Cell Stream Receive Interface Timing

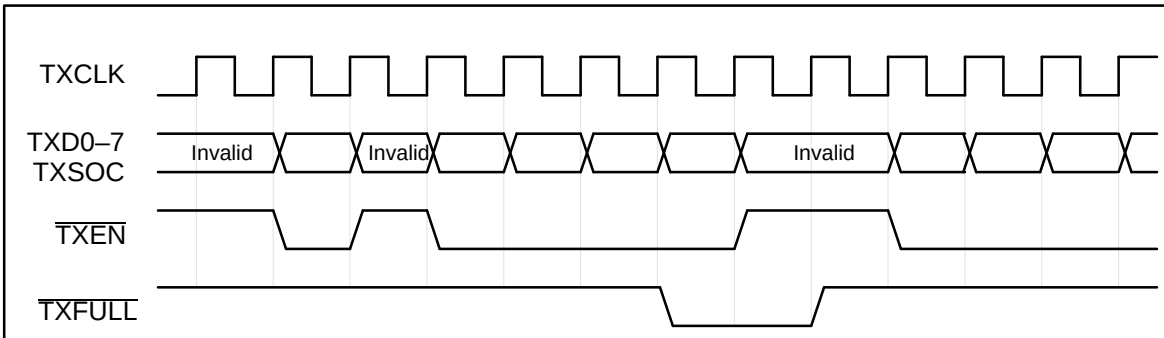


Fig. 10 – UTOPIA Transmit Interface Timing

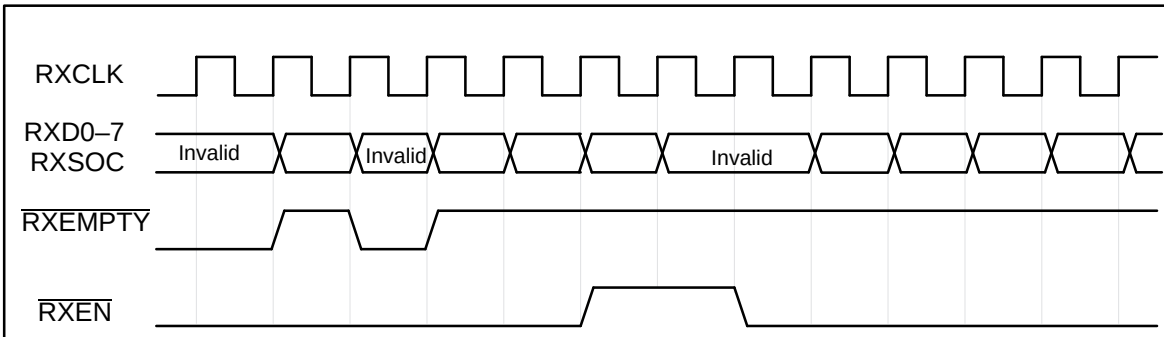


Fig. 11 – UTOPIA Receive Interface Timing

3.5.6 Transmit Multiplex Operations

A token passing mechanism is used when more than one ALC share the same cell stream interface. In this case the ALC should be wired in a daisy chain configuration using the TIN (Token In) and TOUT (Token Out). This mechanism is illustrated in Fig. 12.

TIN should be connected to the TOUT output of an ALC higher up the daisy chain. When the TIN input is inactive (low), the ALC stops transmitting data and places its TXD and TSN pins in high impedance.

The ALC will transmit a Token pulse, on TOUT, on the falling edge of TXCLK to indicate that it has completed a cell transfer or that it has no data to transmit.

Note that if one ALC is able to transmit cells continuously on this interface (ie. no gaps between cells) TOUT will only pulse at the end of a cell if TIN is inactive one clock period before the last byte in the cell.

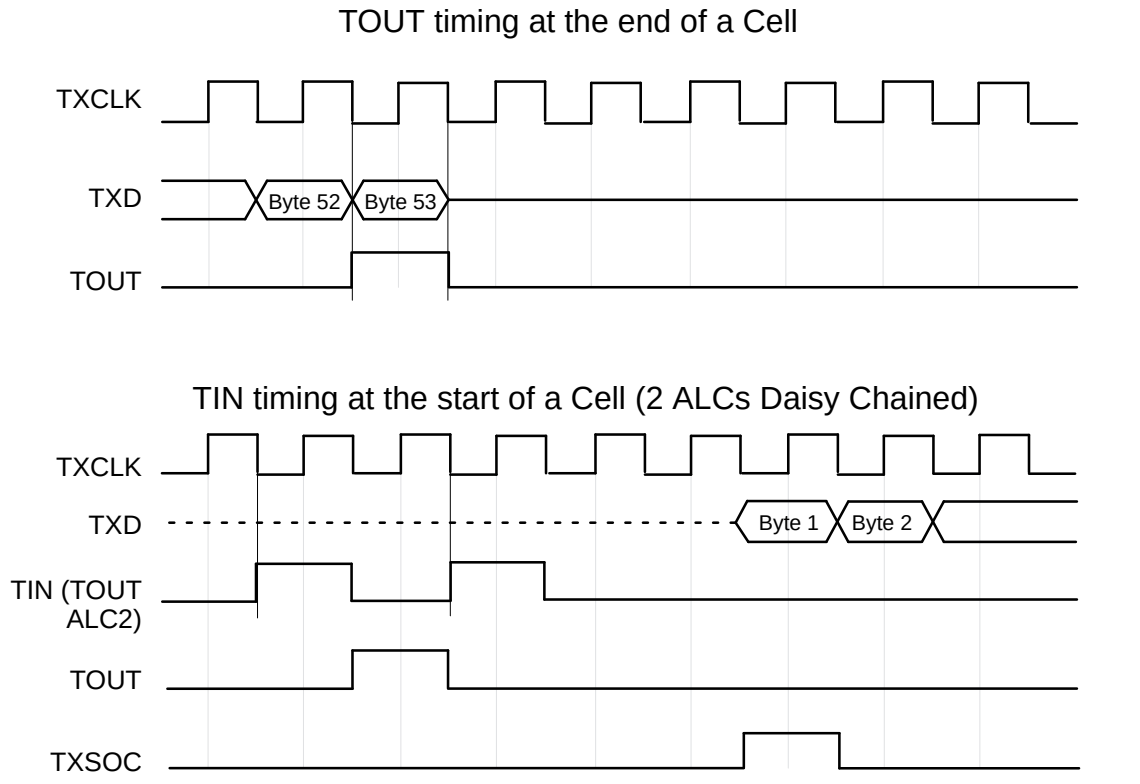


Fig. 12 – CSI Token In/Out Timing

3.5.7 $\overline{\text{TXDRV}}$ (TX cell stream Drive):

Earlier ALC devices needed pull down resistors on the TX cell stream interface because the selection of Cell Stream Daisy Chaining was controlled by a register. Using the $\overline{\text{TXDRV}}$ signal on MB86687 allows these resistors to be omitted.

This mode is selected by tying the $\overline{\text{TXDRV}}$ pin low. By default, it is deselected by an internal pull–up resistor and the register controls the operation

3.5.8 Receive Circuit Reference and VPI/VCI Filter Mechanism

The ALC constructs a 10 bit receive circuit value depending on the setting of the RID bit in register 17.

RID 0
Receive Circuit Reference value is equal to VPB least significant bits of the VPI field concatenated with (10–VPB) least significant bits of the VCI field where VPB is the value of VPI bits to be used in the receive address mapping, specified by bits VPB2, VPB1 and VPB0 in register 16.

AF17–AF14 matched with VPI11–VPI8 for NNI mode

AF17–AF14 are not considered for UNI mode.

AF13–AF0 matched with unused VPI bits concatenated with unused VCI bits.

For VPI filter inactive (VPF=0) the mask bits for the unused VPI bits must be cleared to zero.

RID 1
Receive Circuit Reference is equal to the value in the MID field (AAL3/4 only).

The Receive Circuit Reference value should be used during programming register 59 when enabling receive channels. When re–assembling a packet, this value is loaded into the receive circuit reference field in the receive descriptor.

The ALC performs filtering on the VPI and VCI bits not used for the receive circuit value. Bits AF17 and AF16 in register 16 together with bits AF15 – AF0 in register 56 make up the mask value to be used to filter incoming cells. Programming of the mask bits AF17–AF0 is dependent on the settings of the UNSEL bit in register 16 and the VPF bit in register 17.

3.6 Microprocessor Interface

The Microprocessor Interface is responsible for supporting the following functions:

- Providing Host Processor access to all programmable ALC registers,
- Providing the Host Processor initialisation / test access to the Receive Status / Descriptor Tables,
- Managing the ALCs interrupt mechanism.

3.6.1 Interrupt Controller

The ALC will indicate certain abnormal conditions using the Interrupt signal. The cause of an interrupt is provided in the Interrupt status register.

Each interrupt condition can be individually masked to prevent external interrupt signal generation. A full description of each interrupt source is given in Appendix B., Fig. 42 and Fig. 43 as part of the interrupt status register description.

3.7 Segmentation and Reassembly Memory Interface

3.7.1 Features

The SAR interface is responsible for accessing queues, tables and data stored in either dedicated dual port memory or within the host system memory. The SAR interface can support the following features:

Motorola or Intel compatible bus cycles
Examples of Motorola and Intel Mode Normal Read cycles are shown in Fig. 13 and Fig. 14 respectively.

Extended Intel (486) & Motorola (040) modes.
These modes allow Single Cycle data bursts. Examples of the Intel extended normal and burst read cycles are shown in Fig. 15 and Fig. 16 respectively.

Addressing Schemes
- Little or Big Endian addressing schemes in Intel mode
- Big Endian addressing schemes in Motorola mode.

Other Features
- Direct connection to Dual Port RAM;
- Bus arbitration as required in DMA mode;
- DMA burst length limiting in the range 1 to 255 memory cycles.
- $\overline{\text{READY}}$/$\overline{\text{DTACK}}$ extended cycles in Ready dependent SAR memory mode.
- Memory contention interrupt generation in response to $\overline{\text{READY}}$/$\overline{\text{DTACK}}$ transition when using Fast Cycle Mode.
- $\overline{\text{SADRV}}$ (TX cell stream Drive) – Using the $\overline{\text{SADRV}}$ signal on MB86687 allows pull–up resistors to be omitted. Earlier ALC devices needed pull–up resistors on all the address and control signals because the selection of DPR or DMA modes was controlled by a register.

This mode is selected by tying the $\overline{\text{SADRV}}$ pin low. By default, it is deselected by an internal pull–up resistor and the register controls the operation

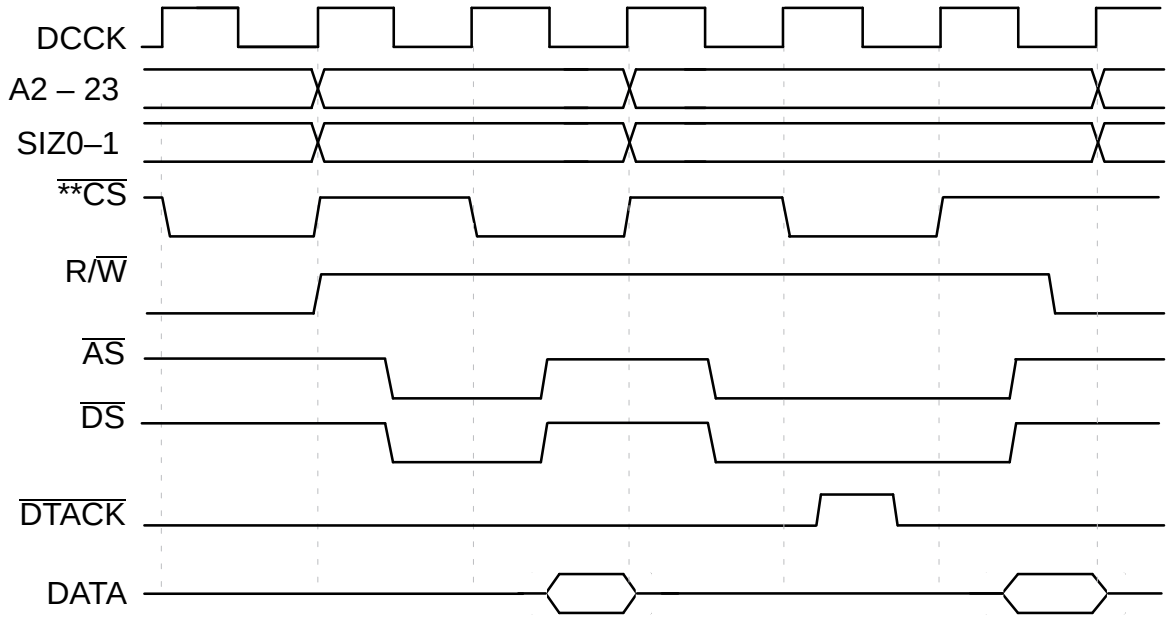


Fig. 13 – Motorola 32 Bit Mode – Normal Mode Read Timing

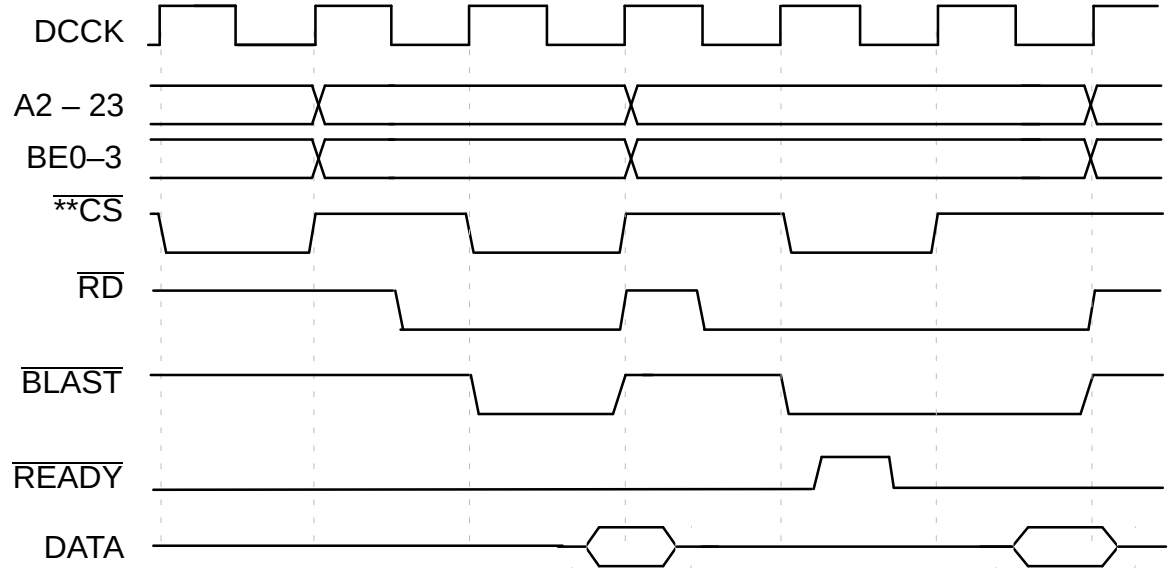


Fig. 14 – Intel 32 Bit Mode – Normal Mode Extended Read Timing

READY is sampled on the falling edge of DCCK at the end of state 3. The example shown uses a synchronous READY signal.

An asynchronous READY signal takes one extra clock cycle to take effect due to internal synchronisation.

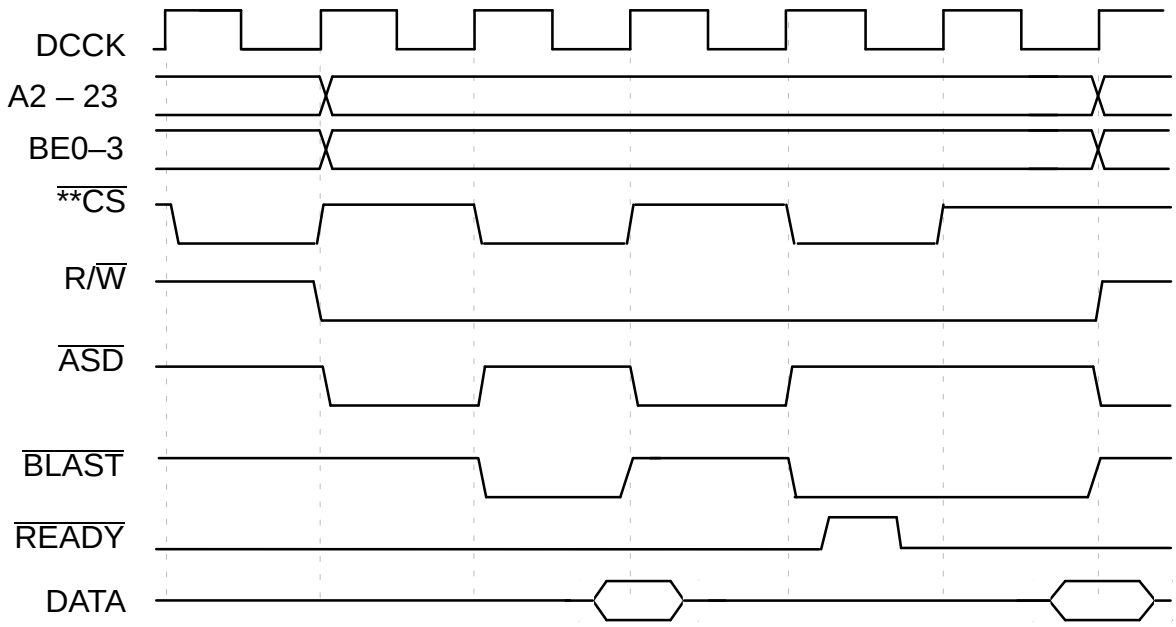


Fig. 15 – Intel 486 Mode – Normal Reads Timing

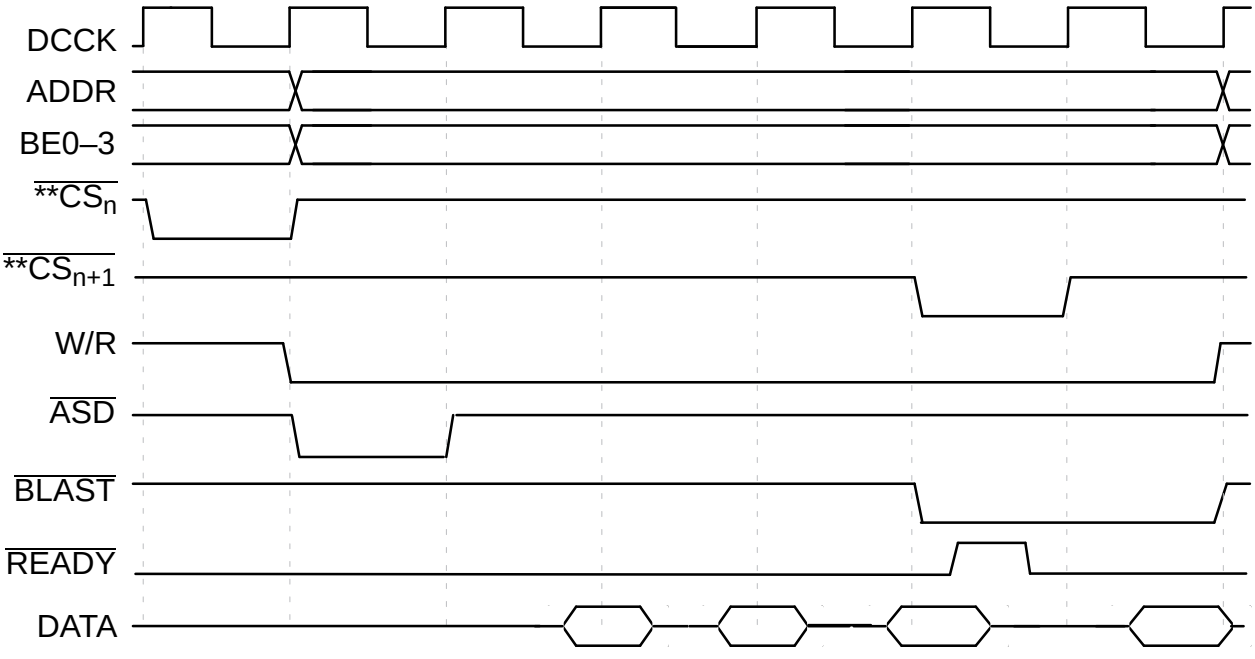


Fig. 16 – Intel 486 Mode Single Cycle Burst Timing

3.7.2 Start of Cycle Signals

There are four start of cycle signals. They are as follows :–

- **$\overline{\text{TOCS}}$**

Transmit Overhead Cycle Start output.

- **$\overline{\text{TDCS}}$**

Transmit Data Cycle Start output.

- **$\overline{\text{ROCS}}$**

Receive Overhead Cycle Start output.

- **$\overline{\text{RDCS}}$**

Receive Data Cycle Start output.

These start of cycle signals are asserted before the associated operation. In normal mode, this will be one clock cycle before the next operation. In $\overline{\text{READY}}$ dependent mode where cycles are back to back, the signal will be asserted during the second clock of the previous cycle. In shared memory systems, this period may be indeterminate because an active start of cycle may be asserted for an operation that will occur after the bus has first been released and then regained. When stealing or forced bursting is enabled a single start of cycle pulse may precede a group of consecutive operations of the same type.

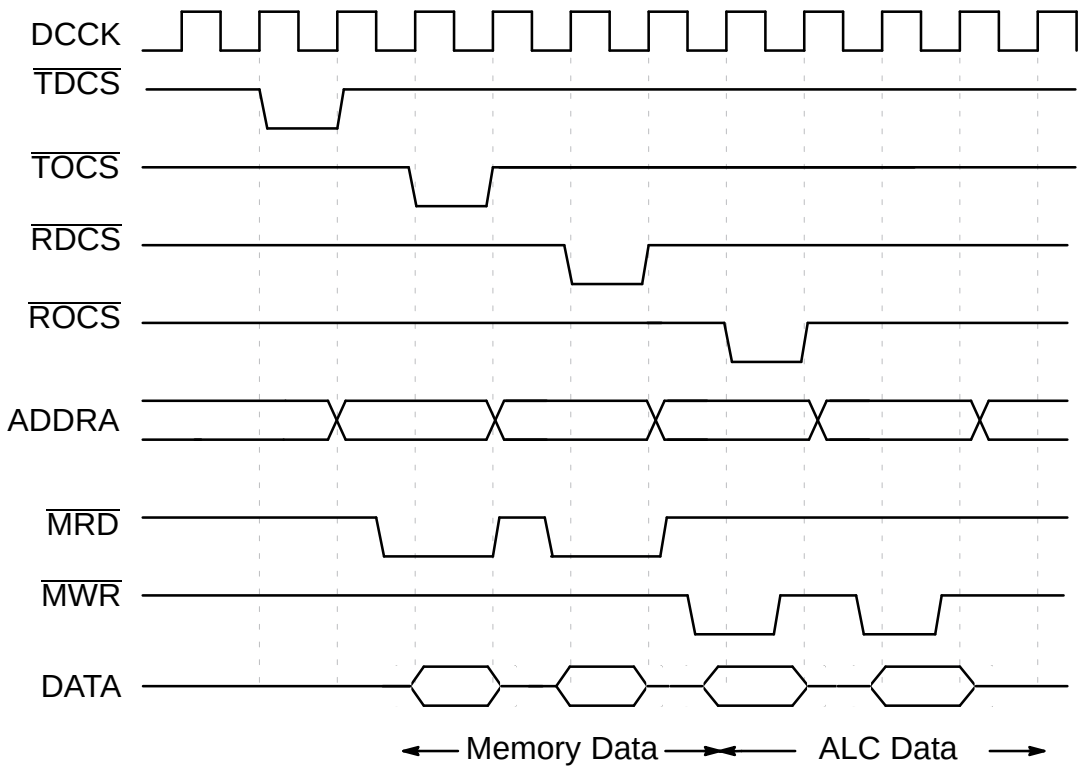


Fig. 17 – Start of Cycle Signal Timing – Fast Mode Extended Read

Parity Bits

Parity generation and detection on a per byte basis is supported on the SAR memory interface using four bi–directional signals.

A register bit determines if the parity generation/ checking is to be odd or even. If a parity error occurs an interrupt is generated.

3.7.3 DMA Cycle Optimisation

The ALC can be programmed to change the cycle ordering on its DMA interface to be optimal for different system configurations This is achieved by progressively setting more bits in the most significant word of the DMA Mode Register. The settings are as follows:–

- 0H – cycles are compatible with 86A ready dependant cycles
- 1H – cycles are compatible with 86A fast cycles with stealing on data cycles only
- 7H – cycles are optimised for dual port RAM systems with stealing of data and overhead cycles
- 1FH – cycles are optimised for shared memory systems where there may be different memory partitions. The cycles will be grouped according to their type.

3.7.4 Transmit DMA CACHE

The ALC uses shared or private memory to create and maintain queues of data packets, packet segmentation information and traffic management data.

To reduce the number of overhead cycles used to access these, a caching mechanism may be used whereby the parameters for up to 128 circuits can be stored on–chip.

The cache is operated in the following way and requires a small processor overhead to maintain a table of cached entries.

- The host software assesses the traffic requirements of each circuit and makes a decision about which circuits would benefit being in the cache.
- The host signals to the ALC that a circuit should be cached via the Circuit Reference Table using the cache start bit and address fields.
- The host then schedules a packet or packets via the TPQ mechanism.
- On its first pass through the data structures, the ALC fetches the appropriate parameters from the Circuit Reference Table and the current Transmit Descriptor and stores them on chip.
- Subsequently the ALC will process the internal copies of its data structures.
- Further queued packets will cause the ALC to fetch the new Transmit Descriptor information only.
- On completion of the packet, if no more packets are queued, the cache entry will remain valid but idle until a new packet is queued or the entry is overwritten with a new entry.
- Additional codes added to the Buffer Release Queue return codes will notify the host when all packets for a particular circuit have been assembled. At this time the host can choose to re-use the cache entry for another circuit.

4. DEVELOPERS NOTES

4.1 Configuration Control Issues

This section is intended to give an overview of the ALC from a system programmers perspective. The following operations need to be performed by the host to configure the ALC.

- Set up the shared data structures,
- Set up queue addresses,
- Set up queue service rate parameters,
- Program ALC mode registers.

During normal operation the host is also required to perform the following operations.

- Pass user data buffers to the ALC for transmission,
- Reclaim used transmit buffers from the ALC for reuse after transmission completes,
- Allocate receive buffer space for use by the ALC,
- Receive packets when completion is indicated by the ALC,
- Activate and de-activate virtual circuits,
- Respond to exception interrupts as required.

These operations are explained in more detail below.

4.2 Transmit Data Structures

A detailed view of the transmit side data structures is shown in Fig. 18. Before data can be transmitted the host has to programme the ALC with the base address of the following transmit data structures: Transmit Descriptor Table, Circuit Reference Table, Transmit Pending Queue and the Transmit Buffer Release Queue.

In addition the host has to initialise the appropriate entries in the Transmit Descriptor and Circuit Reference Tables.

Transmit Descriptor Table
The Transmit Descriptor Table is composed of a contiguous list of Transmit Descriptors (TDs). The host composes a TD for each packet to be transmitted and adds the TD to the TD table. The table can contain up to 4096 TDs. A TD is composed of the following fields, see Fig. 19 on page 33.

M (More)
The host sets this bit to 0 to indicate that the transmit buffer associated with this TD contains the End of Message segment of the CS–PDU. The ALC will append a CS–PDU trailer after the end of this buffer. All other TDs associated with the buffer should have M set to 1.

S (Segmenting)
This bit is set by the ALC to indicate that segmentation is in progress on the transmit buffer. The host sets the S bit to zero before passing the TD to the Transmit Descriptor Table.

$\overline{\text{CE}}$ (Chain End)
The host sets this bit to 0 to indicate that this is the last TD in the chain. If CE is set, the ALC assumes that the Next Chained Descriptor Reference field is valid.

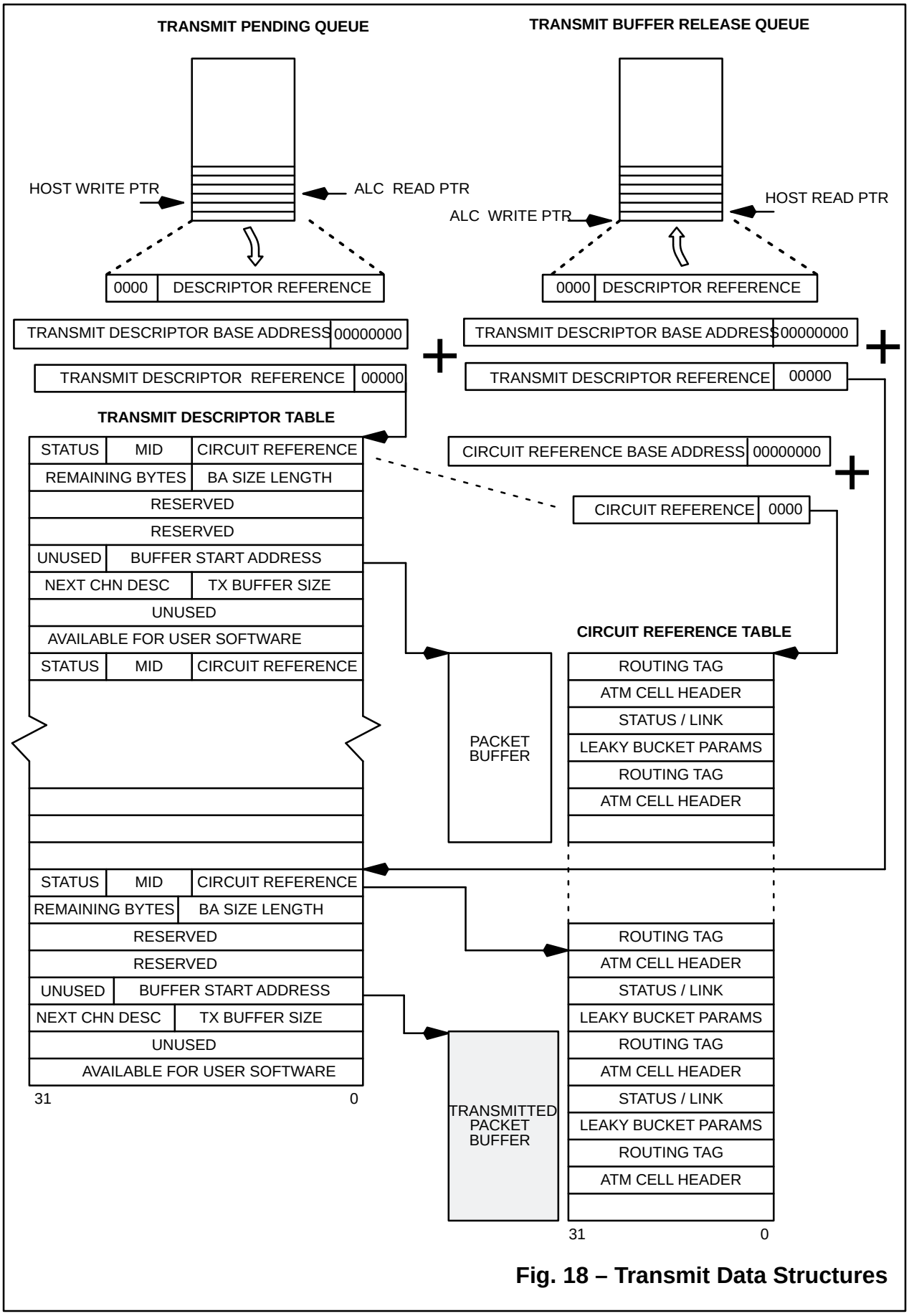


Fig. 18 – Transmit Data Structures

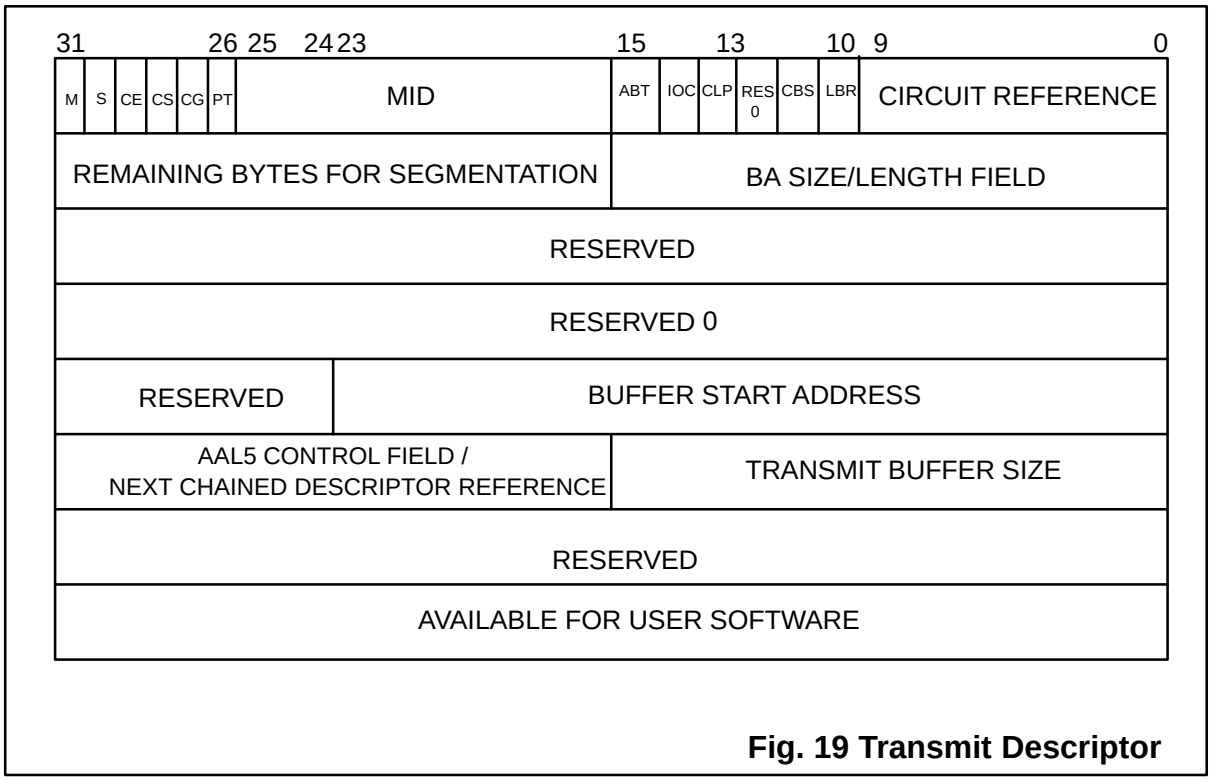


Fig. 19 Transmit Descriptor

$\overline{\text{CS}}$ (Chain Start)
The host sets this bit to indicate that the associated transmit buffer is not the first buffer of a chain or stream of descriptors. This bit is used for AAL3/4 or for AAL5 when using external calculation of Convergence Sublayer parameters.

CG (Congestion indication)
The host sets this bit to indicate that ATM cells generated from the associated buffer should have the congestion notification bit set in the Payload Type Field.

PT (Pass Transparent)
The host sets this bit to indicate that the ALC should set the CG bit in the PTI field and CLP bit of the ATM cell header directly as coded in the Circuit Reference Table for each cell, otherwise the CG and CLP bits are as programmed in the Transmit Descriptor.

MID (Multiplexing Identification)
The ALC writes this ten bit field into the ATM cell's MID field.

ABT (Abort)
The host sets this bit to instruct the ALC to transmit an Abort cell as defined for streaming mode operation. When an abort AAL3/4 or AAL5 cell has been transmitted the following queued descriptor should not have the CS bit set ie. it should be the first descriptor in a new packet.

IOC (Interrupt On Completion)
The host sets this bit to indicate that the ALC should generate an interrupt when segmentation of the packet is complete.

CLP (Cell Loss Priority bit)
The host sets this bit to indicate that ATM cells generated from the associated buffer should have the CLP bit set = 1.

CBS (Copy Buffer Size)
The host should set this bit if the Transmit Buffer Size field is the initial value for bytes for segmentation.

LBR (Leaky Bucket Reset)
The host should set this bit if the leaky bucket variable capacity is to be re–initialised the first time data is re–assembled from this TD.

Circuit Reference
This field is a 10 bit index into the Circuit Reference Table. It is shifted left by 4 bits then added to the Circuit Reference Table base address (shifted left by 8 bits) to generate a pointer to the appropriate entry in the Circuit Reference Table. The circuit reference index could be either the VCI or MID of the connection.

Remaining Bytes for Segmentation
This field is initially loaded with the total number of bytes in the packet for segmentation. This field is modified by the ALC during packet transmission. In streaming and chaining modes, the length of each buffer can be any number of bytes provided that the next streamed or chained buffer can fill any remaining partially assembled cell. In streaming mode a buffer that does not terminate on a cell boundary will be held by the ALC until a subsequent buffer is linked on.

BA Size / Length Field
In AAL 3 /4 mode the ALC transmits this value in the BA Size field of the AAL 3/4 CS–PDU header. In AAL5 mode the AAL transmits this value in the AAL5 CS–PDU trailer LENGTH field.

Reserved 0
These fields are for internal ALC usage. They should be initialised to 0 and reset to 0 when the host retrieves the transmit descriptor through the transmit buffer release queue but otherwise should not be used by the host.

Reserved
These fields are for internal ALC usage and should not be used by the host.

Buffer Start Address
This 24 bit pointer provides the ALC with the start address of the associated transmit buffer. Any number of header bytes can be read from a user data buffer by writing the correct byte (non 32 bit aligned) address to this location.

AAL5 Control Field /
Next Descriptor Reference
In chaining mode the host programmes the next descriptor reference in the chain into this field. In AAL5 mode, this field contains the Control Field of the CS–PDU trailer only if this is the final TD in the chain.

Transmit Buffer Size
This 16 bit value is set by the host. It specifies the number of bytes in the associated transmit buffer. This field is optionally used by the ALC, if the CBS bit is set, as the initial value of bytes for segmentation.

Available for User Software
This field is not used by the ALC and will not be used by future ALC devices. This field may be utilised by user software.

Re–initialisation of Transmit Descriptors

Field	Mode		
	Message	**Chaining**	**Streaming**
Segmenting (S) bit	0	0	0
AAL5 Control/ Next Chain	set	AAL5: control in last TD Next chain descriptor	Set last TD only
Buffer Start Address	Programmed by Host		
AAL3/4 BASIZE AAL5 Length	set *	AAL3/4: BASIZE in first TD AAL5: length in last TD *	
Bytes remaining	Programmed by Host **		
Reserved 0	Program to 0		

Note * In AAL5, if the MAAL5 bit is set, this value is computed automatically by the ALC.
Note ** If copy buffer size is set, this field will be refreshed by the ALC to the value in the Transmit Buffer Size field.

Circuit Reference Table

The Circuit Reference Table is composed of a list of contiguous Circuit Reference entries. There is a Circuit Reference for each active Virtual Circuit. Each Circuit Reference Table entry contains the ATM Cell header and the Leaky Bucket parameters for the relevant VC. The Circuit Reference is composed of the following fields, see Fig. 20.

Routing Tag 0 – 3

Optional routing tag appended in applications where the ALC is interfacing directly with a Fujitsu Self Routing Switch Element MB86680B device or any similar device. Up to three octets of routing is supported.

- **GFC** – Generic Flow Control,
- **VPI** – Virtual Path Identifier,
- **VCI** – Virtual Channel Identifier,
- **PTI** – Payload Type Identifier**,**
- **CLP** – Cell Loss Priority.

These form the ATM Header Field as defined by the UNI Specification. The ALC will code the PT bit of the PTI field according to the state of assembly of the SDU.

U, Leaky Bucket utilisation parameter

This field contains the average rate of cell transmission for leaky bucket management expressed as a ratio of the peak rate. The coding is as follows:

Bit no.	11	10	9	8
Peak Rate Ratio	1	1/2	1/4	1/8

The host can select any combination of bits to generate the required average rate. If the ratio is programmed to 1, the peak and average rates will be identical which could be used for constant bit rate traffic. Average rates greater than 1 are not supported.

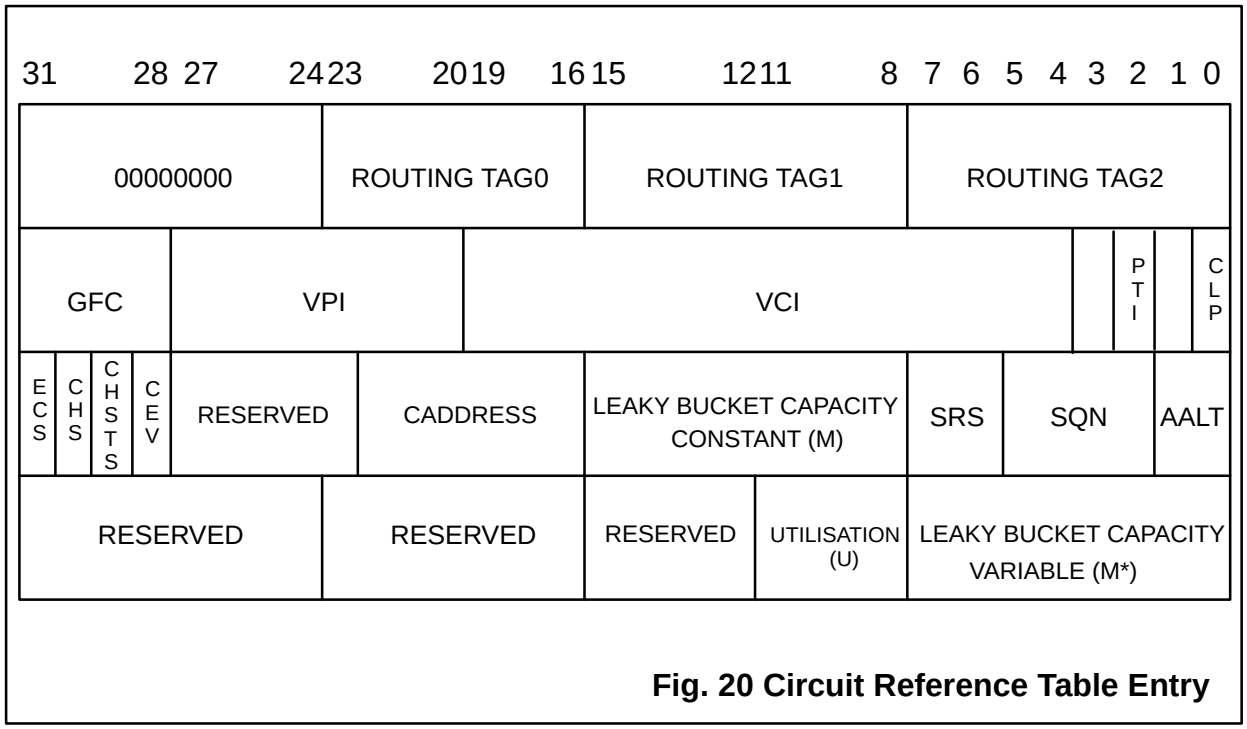


Fig. 20 Circuit Reference Table Entry

ECS (External Calculation of SPCS*)*
Single bit instruction to use external memory for AAL5, CRC32 and AAL3/4 length field and sequence number. This is used for non–cached entries when internal memory is not available: set by HOST. (Each cache entry uses the storage of 8 equivalent VC entries)

Additionally used in transparent cell and transparent payload to indicate to the ALC that the CRC10 should be calculated and placed in the last 10 bits of the payload.

CHS (Cache Start)
Set by HOST.

CHSTS (Cache Status)
Initialised to ’0’ by the HOST, set by ALC.

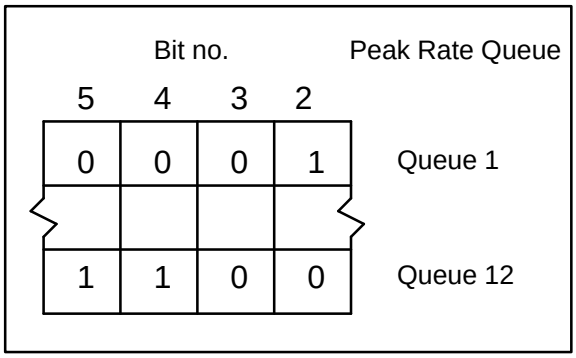
CEV (Chain End Valid)
Initialised to ’0’ by the HOST, set by ALC

CADDRESS (Cache Address)
(7 bit field): set by HOST; valid if the CHS bit is set.

SRS (Sub-Rate Select)
These bits are used to select the required sub-rate of the nominal transmit queue peak rate. The coding is as follows.

Bit no. 7	Bit no. 6	Sub-rate selected
0	1	25%
1	0	50%
1	1	100%

SQN (Service Queue Number)
The host uses this field to assign the associated Virtual Circuit to one of the 12 peak rate queues. The coding is as follows:



Queue 1 corresponds to Low Priority and Queue 12 corresponds to High Priority Queue 4.

AALT (ATM Adaption Layer Type)
This field is used to specify the AAL type for the VC. Two transparent modes can also be selected. The coding is as follows:

1	0	AAL Type selected
0	0	AAL 3/4
0	1	Transparent Payload
1	0	Transparent Cell
1	1	AAL 5

M (Leaky Bucket capacity constant)
M in the Circuit Reference Table entry is the bucket capacity used to implement leaky bucket averaging on a per VC basis. The host programmes this field with a Leaky Bucket capacity in the range of 0 – 255. The relationship between the bucket capacity (M), the utilization (U) and the maximum burst length (B) at the selected peak rate is given by:

$$M = (B – 1) \times (1 – U)$$

for single leaky bucket method and by:

$$M = B \times (1 – U)$$

for double leaky bucket method.

Note:
If the resulting M value is not an integer then in the single leaky bucket case M should be rounded DOWN to the nearest integer and in the double leaky bucket case M should be rounded UP to the next integer.

Also, for the single leaky bucket case a minimum value of B is specified for each utilization value as given below:

U = 0.875 minimum allowed B = 9,

U = 0.75 minimum allowed B = 5,

U = 0.625 minimum allowed B = 4,

For all other values of U the minimum value allowed for B is 3.

M* (Leaky Bucket capacity variable)
The ALC uses this variable to implement leaky bucket averaging on a per virtual circuit basis. The host initially sets M* to the same value as M, M* is then modified by the ALC as the ALC implements the leaky bucket algorithm for that VC. The ALC uses the constant value M for reference when carrying out leaky bucket calculations. M* may also be refreshed to M when the LBR bit is set in a TD.

Reserved
These fields are for internal ALC usage and should not be used by the host.

4.2.1 Transmit Pending Queue

The transmit pending queue is used by the host to instruct the ALC to queue a transmit packet for segmentation. Each command passed to the queue includes a 12 bit index reference into the Transmit Descriptor table. A Transmit Pending Queue entry is shown in Fig. 21.

This queue is defined by registers 2 – 6. The Host Processor must assign values for the Transmit Pending Queue base, start address, end, read and write pointers. The initial values of the read and write pointers should be the start address to reflect an empty queue.

To pass a new entry to the TPQ the Host Processor should read the current value of the on-chip write register. This address should be used to store the new TPQ entry. The host should then update the write pointer register, wrapping around to the start address if necessary.

When the DMA Controller has available transmit bandwidth (or once every five segmentation periods), i.e a cycle where cell segmentation is not required, it reads the value of the Transmit Descriptor Reference addressed by its internal read pointer.

In addition, the Transmit Pending Queue can be used as follows:

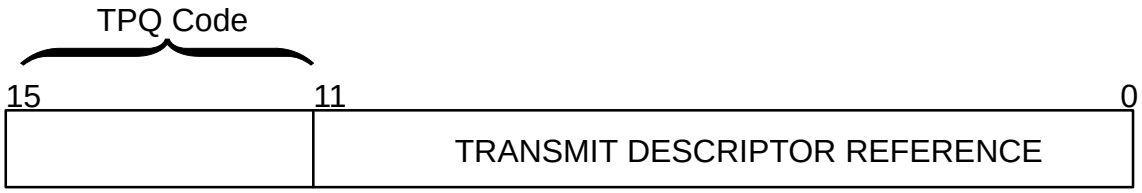
- Utilisation adjustment;

The U value in the CRT pointed to by the associated TD will be set to the given value.

This is not applicable to cached entries.

- Send Express Cell;

If an entry is placed on the queue with the 1100 coding then it will not be assigned to a rate queue but will be sent immediately.



0 0 0 0	Queue Packet
0 0 0 1	Set Utilisation to 0.125
0 0 1 0	Set Utilisation to 0.25
0 0 1 1	Set Utilisation to 0.375
0 1 0 0	Set Utilisation to 0.5
0 1 0 1	Set Utilisation to 0.625
0 1 1 0	Set Utilisation to 0.75
0 1 1 1	Set Utilisation to 0.875
1 0 0 0	Set Utilisation to 1.0
1 1 0 0	Queue Express Cell
1 1 1 1	Set Utilisation to 0

Fig. 21 – Transmit Pending Queue Format

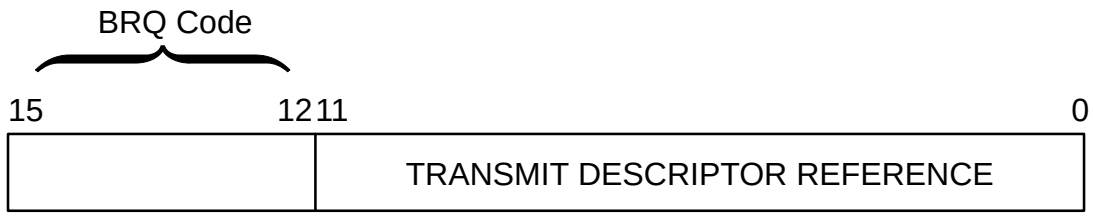
4.2.2 Transmit Buffer Release Queue

The ALC returns segmented transmit buffers to the host using the Buffer Release Queue. Each queue entry will contain a 12 bit reference index into the Transmit Descriptor table. A queue entry is shown in Fig. 22.

This queue is defined by registers 2 and 7 – 10. The Host Processor must assign values for the Buffer Release Queue base, start address, end, read and write pointers.

The initial values of the read and write pointers may be the start address to reflect an empty queue or the write pointer may be set to the read pointer minus 1 to reflect a pool of free buffers.

To release a buffer to the host the ALC increments the TBRQ write pointer and, if the IOC bit in the Transmit descriptor is set, generates an interrupt. The host may then choose to immediately acknowledge this action by updating the TBRQ read pointer or if using the queue as a pool of free buffers, only update the pointer when reusing the TD.



0 0 0 0	Default code
0 0 0 1	Changed Utilisation
0 0 1 0	Packet complete. No further packets for this circuit
0 0 1 1	Packet complete. No further packets for this queue
0 1 0 0	Buffer complete. Moving to next streamed buffer
0 1 0 1	Changed utilisation to 0
0 1 1 0	Buffer complete. Awaiting next streamed buffer
0 1 1 1	Buffer complete. No further packets in this queue. Awaiting next streamed buffer
1 0 0 0	Buffer complete. Not end of chain
1 0 1 0	Express Cell Sent
1 1 0 0	Abort sent
1 1 1 0	Abort sent. No further packets for this circuit
1 1 1 1	Abort sent. No further packets in this queue

Fig. 22 – Transmit Buffer Release Queue Format

4.2.3 INCWRAP – Wrap and Increment Mechanism

When writing to the host–controlled queue registers, if the most significant bit of the control data bus is set, the ALC will automatically increment its internal copy of the pointer being written to regardless of the pointer value specified on the data bus.

Two status conditions are available when reading the host–controlled pointers:

- **EMPTY condition**

If this bit is set, it indicates that the ALC's pointer for the queue is at the same value as the host pointer's value returned by the read and that the queue is empty.

- **FULL condition**

If this bit is set, it indicates that the host pointer and ALC pointer values are the same and that the queue is full.

4.3 Receive Data Structures

A detailed view of the receive data structures is shown in Fig. 23. Before data can be received the host has to programme the ALC with the base address of following receive data structures: Receive Descriptor Table, Receive Buffer Free Queue and the Receive Buffer Ready Queue.

4.3.1 Receive Descriptor Table

The Receive Descriptor Table is composed of a contiguous list of Receive Descriptors (RDs). The host is responsible for composing sufficient RDs to handle the expected number of receive packets.

Each time a start of packet cell is received the ALC will use the next entry in the Receive Buffer Free Queue to locate the relevant RD in the table. A typical RD is composed of the following fields, see Fig. 24 on page 43.

V (Valid)
The ALC sets this bit to 1 to indicate that the Next Chain Descriptor field in this descriptor is valid. This is used in chaining mode when the received packet does not terminate in the current receive buffer. When this bit is cleared to 0 it indicates that the chain of receive buffer descriptors terminates with this descriptor. The host is required to initialise this bit to 0 and also in chaining mode to clear this bit to 0 before returning the receive descriptor to the ALC through the buffer free queue.

Next Chain Descriptor Reference
When receive buffer chaining is used this 12 bit field is programmed by the ALC with the descriptor reference of the next receive descriptor in the chain.

Reserved
These fields are for internal ALC usage and should not be accessed by the host.

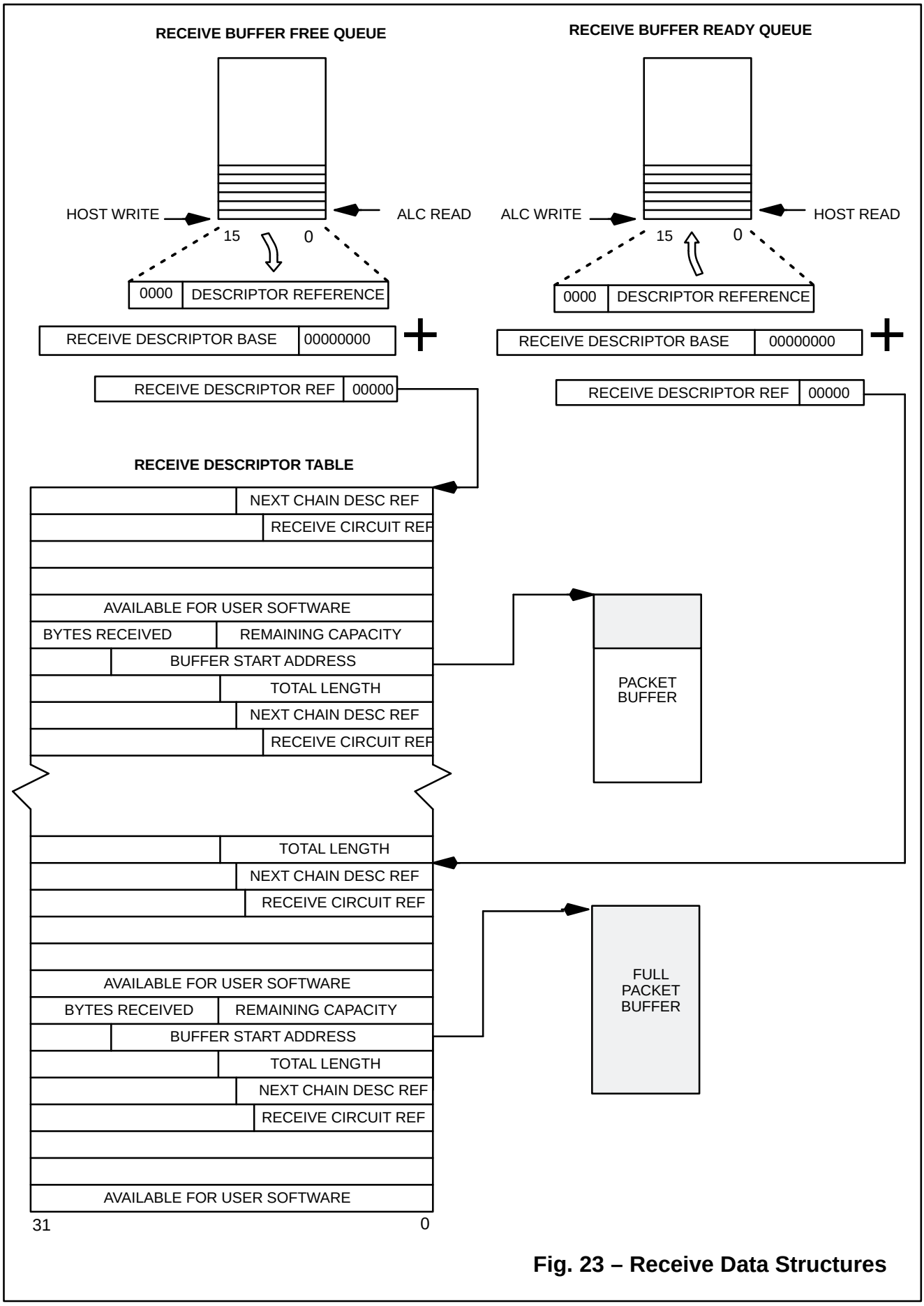


Fig. 23 – Receive Data Structures

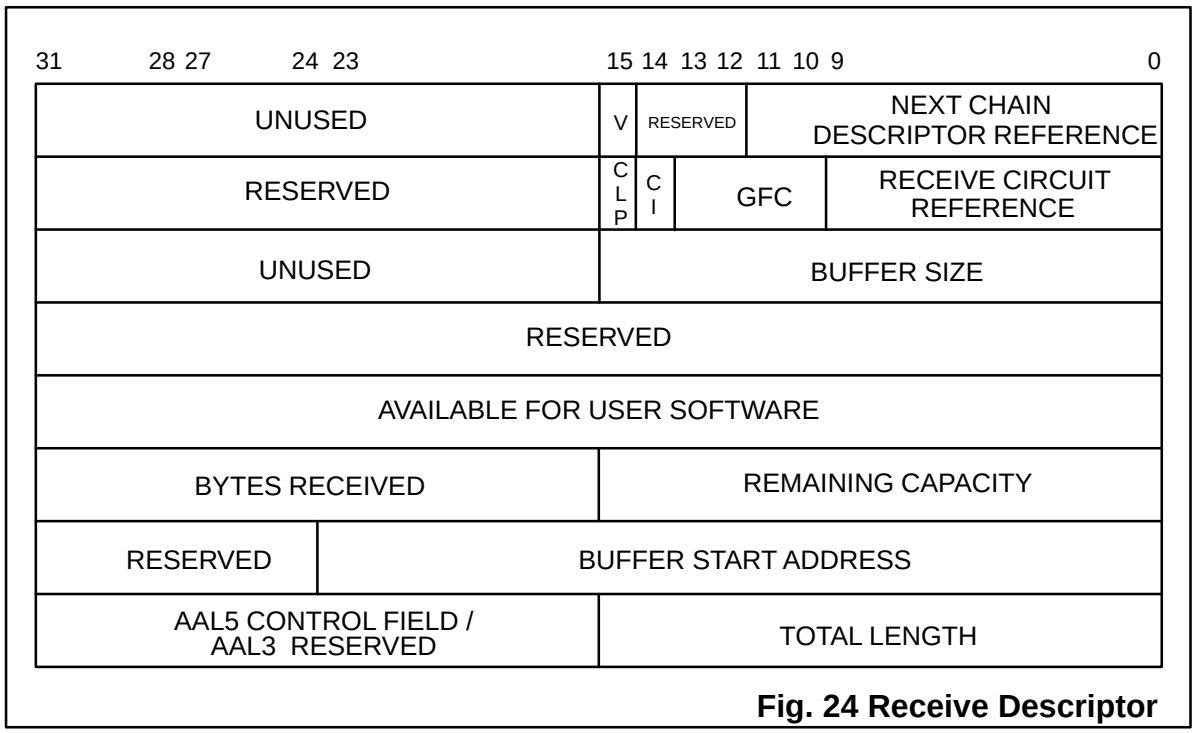


Fig. 24 Receive Descriptor

Receive Circuit Reference
This 10 bit field is programmed by the ALC with the receive channel supplying data to the associated receive buffer. This channel number will imply a particular VP/VC according to the programming of VPB2, VPB1 & VPB0 in Register 16. If chaining is used, this value is only valid in the first descriptor of the chain.

CLP (Cell Loss Priority)
The ALC sets this bit to indicate that the last ATM cell re–assembled into the associated buffer had the CLP bit set = 1.

CI (Congestion Indication)
The ALC sets this bit to indicate that the last ATM cell re–assembled into the associated buffer had the CI bit set = 1.

GFC (Generic Flow Control)
The ALC sets this field to the GFC value in the last ATM cell reassembled into the associated buffer.

Unused
These fields should not be utilized by user software but may be cleared to 0 by the host.

Buffer Size
If the RDAU bit is set in Register 16, this value is automatically copied into the Remaining Capacity field when the RD is first accessed. The value is not modified by the ALC.

Available for User Software
This field is not used by the ALC and will not be used by future ALC devices. This field may be utilized by user software.

Bytes Received
This 16 bit field is programmed by the ALC with the number of bytes written to the associated receive buffer.This field should be initialized to 0 and reset to 0 before returning the descriptor for reuse through the buffer free queue. This count is always a multiple of 4 bytes and hence, will include up to 3 bytes of pad at the end of a packet.

Remaining Capacity
This field indicates the number of unused bytes within the associated buffer. This field should be initialized to the buffer capacity and reset to the buffer capacity before returning the descriptor for reuse through the buffer free queue. This count is always a multiple of 4 bytes and hence, will include up to 3 bytes of pad at the end of a packet.

Buffer Start Address
This 24 bit pointer is programmed by the host with the start address of the receive buffer associated with this descriptor.

AAL5 Control Field / AAL3 Reserved
When AAL5 is selected this field is used to hold the received AAL5 control value obtained from the incoming CS–PDU trailer. If chaining is enabled then this field is only valid in the initial receive descriptor of the chain. In all other descriptors in the AAL5 chain this field is reserved. In AAL 3 for all descriptors this field is reserved. In chaining mode this field should be initialized to 0 and reset to 0 before returning the descriptor for re–use through the buffer free queue.

Total Length
This 16 bit value is programmed by the ALC with the total length field received in the CS–PDU trailer. If chaining is used then this field contains the total length only in the initial receive descriptor of the chain. In chaining mode this field should be initialized to 0 and reset to 0 before returning the descriptor for reuse through the buffer free queue.

Re–initialisation of Receive Descriptors

Field	Mode		
	Message	Chaining	Streaming
V & next chain RD	N/R	0	N/R
Bytes Received	0 *	0 *	0 *
Remaining Capacity	buffer size **	buffer size **	buffer size **
BufferStart Address	Programmed by Host		
AAL5 Control/AAL3 Reserved	0	0	0
Total Length	N/R	0	N/R

N/R Reinitialisation not required
Note * If RDAU is set in Register 16, Bytes Received is automatically cleared when the RD is first accessed; Reinitialisation is then not required.
Note ** If RDAU is set in Register 16, Buffer Size is automatically copied into Remaining Capacity when the RD is first accessed. Reinitialisation is then not required.

4.3.2 Receive Buffer Free Queue

The Receive Buffer Free Queue is used by the ALC to locate the next Receive Descriptor each time a new packet is received.

Each queue entry contains a reference into the Receive Descriptor table. The format of a queue entry is shown in Fig. 25.

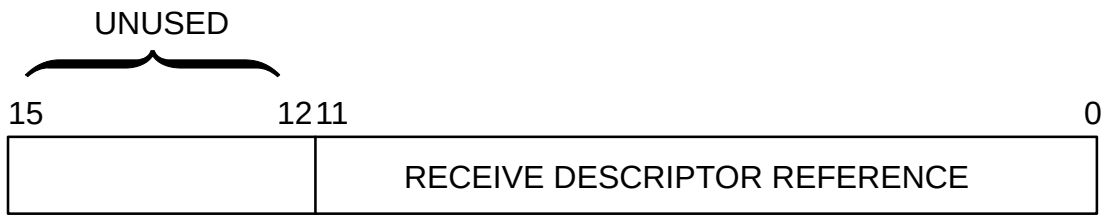


Fig. 25 – Buffer Free Queue Format

4.3.3 Receive Buffer Ready Queue

The ALC passes reassembled packets to the host using the Receive Buffer Ready Queue. Each queue entry contains a reference to the relevant Receive Descriptor. In addition the ALC writes the status of the received packet to the Buffer Ready Queue. The format of each queue entry is shown in Fig. 26.

4.3.4 Increment and Wrap Mechanism

This mechanism is similar to that used by the transmit queues and is described in section 4.2.3.

0 0 0 0	Reassembly Complete With No Errors (M=0)
0 0 0 1	Buffer Complete With No Errors (M = 1)
0 0 1 0	Reassembly Complete With f5 OAM cell – CRC10 passed
0 0 1 1	Reassembly Complete With f4 or f5 OAM cell – CRC10 failed
0 1 0 0	Reassembly Complete With f4 OAM cell – CRC10 passed
0 1 0 1	Sequence Number Error
0 1 1 0	Invalid Length Indication
0 1 1 1	Partial reassembly: Missing EOM
1 0 0 0	Receive Buffer Overflow
1 0 0 1	Receive Maximum Length Exceeded
1 0 1 0	No Chaining buffers Available
1 0 1 1	AAL3 Trailer Error Indication
1 1 0 0	Buffer Timed Out Reassembly Aborted
1 1 0 1	Packet Length Error Indication
1 1 1 0	RAS Abort Indication
1 1 1 1	AAL5 CRC 32 Error Indication || AAL3 BTag / ETag mismatch

Fig. 26 – Receive Buffer Ready Queue Format

4.3.5 Receive Descriptor Table Access Mechanism

Writing to the Table

The write to RSD table process operates in the following way. The host sets the data intended for the RSD by writing it to the Host Receive Descriptor/Status Table Write Register (Register 58) – (This will normally involve setting the ACT bit when a channel is about to be activated). The host then writes to the Host Receive Descriptor/Status Table Access Register (Register 59). The HOSTR and RD/WR must be set to generate the internal write to the RSD table. The values in Register 58 together with the AAL bits from Register 59 are written into the RSD table at the address specified by the VCI values in Register 59.

The TAC interrupt will be generated in response to the write to Register 59 to inform the host that the RSD table has been updated.

Reading from the Table

The read from RSD table process comprises the following sequence of events. The host writes to Register 59 setting HOSTR and clearing RD/WR. This causes the ALC to carry out an internal read to the RSD table using the address specified by the VCI value in Register 59.

The contents of the read are written to the Host Receive Descriptor/Status Table Read Register (Register 57) and the TAC interrupt is generated indicating to the host that Register 57 has been updated.

The host then reads the RSD table contents from Register 57.

Notes

Register 57 is read only.

Accesses to Registers 57 and 58 have no effect on the RSD table until Register 59 is written to.

During normal operation, Register 59 should not be written to with HOSTR and RD/WR (bits D15 and D14) set after the initialisation stage.

4.3.6 OAM Cell Handling

The ALC will flexibly handle incoming OAM cells.

The ALC considers a cell to be an F5 OAM cell if the most significant bit of the PTI field is set. This means that resource management cells (PTI field = 110) are also treated as these cells.

The ALC considers a cell to be an f4 OAM cell if the cell arrives on a channel which has the RIP bit set and the AAL bits set for Transparent Cell mode (10) in the RSD table.

If the DCOAM bit (CR16) is set, only F5 OAM cells are discarded. Discarded OAM cells do not alter the dropped cell counter value.

If cleared, the OAMCRC bit (CR16) only disables CRC10 checking on F5 OAM cells. The ALC always performs CRC10 checking on F4 OAM cells.

A. REGISTER TABLE

The ALC register address table is shown on the following pages. Please note that the Register Tables TYPE field indicates the type of host access cycle used to access each register.

Abbreviations used are as follows:

R/O = Host read access only.

W/O = Host write access only.

(T) = After initialisation, these registers are updated using TCLK and have a recovery time dependent on TCLK.

CW/R = Host write access only after setting the control write enable bit (CWRE) of the ALC Control Register.

The Registers listed in Fig. 27 to Fig. 29 are further described in Appendix B.

An ‘x’ symbol in a register bit location indicates that that bit is not used by the ALC. These unused bits should be written to ‘0’ when writing to the register and will return ’1’ when reading the register.

All the ALC write registers are initialised to 0 after power–up.

ADDRESS	TYPE	FUNCTION	REF
0	W / O	TRANSMIT DESCRIPTOR TABLE BASE ADDRESS REGISTER	Fig. 30
1	W / O	CIRCUIT REFERENCE TABLE BASE ADDRESS REGISTER	Fig. 30
2	W / O	TRANSMIT QUEUE BASE ADDRESS REGISTER	Fig. 30
3	W / O	TRANSMIT PENDING QUEUE START ADDRESS REGISTER	Fig. 31
4	W / O	TRANSMIT PENDING QUEUE END ADDRESS REGISTER	Fig. 31
5	W/R	TRANSMIT PENDING QUEUE WRITE POINTER	Fig. 31
6	CW / R	TRANSMIT PENDING QUEUE READ POINTER	Fig. 32
7	W / O	TRANSMIT BUFFER RELEASE QUEUE START ADDRESS REG.	Fig. 32
8	W / O	TRANSMIT BUFFER RELEASE QUEUE END ADDRESS REG.	Fig. 32
9	CW / R	TRANSMIT BUFFER RELEASE QUEUE WRITE POINTER	Fig. 33
10	W/R	TRANSMIT BUFFER RELEASE QUEUE READ POINTER	Fig. 33
11	——	RESERVED	
12	——	RESERVED	
13	R/O	GFC/CI STATUS CHANGE REGISTER	Fig. 34
14	W / O	DMA BURST REGISTER	Fig. 33
15	W / O	DMA MODE REGISTER	Fig. 36
16	W / O	CONTROL REGISTER	Fig. 38
17	W / O	MODE REGISTER	Fig. 40 Fig. 41
18	R / O	INTERRUPT STATUS REGISTER	Fig. 42 Fig. 43
19	W/R	INTERRUPT MASK REGISTER	Fig. 44

Fig. 27 – ALC REGISTER MAP (1 of 3)

ADDRESS	TYPE	FUNCTION	REF
20	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER LOW 1	Fig. 44
21	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER LOW 2	Fig. 44
22	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER LOW 3	Fig. 44
23	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER LOW 4	Fig. 44
24	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER MEDIUM 1	Fig. 44
25	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER MEDIUM 2	Fig. 44
26	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER MEDIUM 3	Fig. 44
27	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER MEDIUM 4	Fig. 44
28	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER HIGH 1	Fig. 44
29	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER HIGH 2	Fig. 44
30	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER HIGH 3	Fig. 44
31	W / O(T)	TRANSMIT QUEUE SERVICE RATE REGISTER HIGH 4	Fig. 44
32	W / O(T)	TRANSMIT QUEUE SERVICE ENABLE REGISTER	Fig. 45
33	W / O(T)	ALC PEAK CELL TRANSMISSION RATE REGISTER	Fig. 46
34	W / O(T)	ALC AVERAGE CELL TRANSMISSION RATE REGISTER	Fig. 46
35	W / O(T)	ALC LEAKY BUCKET CAPACITY REGISTER	Fig. 47
36	——	RESERVED	
37	——	RESERVED	
38	——	RESERVED	
39	——	RESERVED	

Fig. 28 – ALC REGISTER MAP (2 of 3)

ADDRESS	TYPE	FUNCTION	REF
40	W / O	RECEIVE QUEUE BASE ADDRESS REGISTER	Fig. 48
41	W / O	RECEIVE BUFFER FREE QUEUE START ADDRESS REGISTER	Fig. 48
42	W / O	RECEIVE BUFFER FREE QUEUE END ADDRESS REGISTER	Fig. 49
43	W/R	RECEIVE BUFFER FREE QUEUE WRITE POINTER	Fig. 49
44	CW / R	RECEIVE BUFFER FREE QUEUE READ POINTER	Fig. 49
45	W / O	RECEIVE DESCRIPTOR BASE ADDRESS REGISTER	Fig. 48
46	W / O	RECEIVE BUFFER READY QUEUE START ADDRESS REGISTER	Fig. 50
47	W / O	RECEIVE BUFFER READY QUEUE END ADDRESS REGISTER	Fig. 50
48	CW / R	RECEIVE BUFFER READY QUEUE WRITE POINTER	Fig. 51
49	W/R	RECEIVE BUFFER READY QUEUE READ POINTER	Fig. 51
50	R / O	DROPPED PACKET COUNTER	Fig. 51
51	W / O	RECEIVE BUFFER TIME OUT COUNTER PERIOD REGISTER	Fig. 52
52	W / O	RECEIVE BUFFER TIME OUT INTERVAL REGISTER	Fig. 52
53	R / O	RECEIVED BUFFER READY DATA HOLD REGISTER	Fig. 53
54	W / O	MAXIMUM RECEIVED PACKET LENGTH REGISTER	Fig. 53
55	R / O	DROPPED CELL COUNTER	Fig. 53
56	W / O	RECEIVE ADDRESS FILTER REGISTER	Fig. 54
57	R / O	HOST RECEIVE DESCRIPTOR / STATUS TABLE READ REG.	Fig. 55
58	W / O	HOST RECEIVE DESCRIPTOR / STATUS TABLE WRITE REG.	Fig. 55
59	W / R	HOST RECEIVE DESCRIPTOR / STATUS TABLE ACCESS REG.	Fig. 56

Fig. 29 – ALC REGISTER MAP (3 of 3)

B. REGISTER MAPS

Register 0 – Transmit Descriptor Table Base Address Register

D15

TDA15	TDA14	TDA13	TDA12	TDA11	TDA10	TDA9	TDA8
TDA7	TDA6	TDA5	TDA4	TDA3	TDA2	TDA1	TDA0

D0

This base address (shifted left by 8 bits) is added to the 12 bit Transmit Descriptor address (shifted left by 5 bits) from the Transmit Pending or Release Queue to obtain the full 24 bit address of the Transmit Descriptor required to execute a packet transmission.

Register 1 – Circuit Reference Table Base Address Register

D15

CRA15	CRA14	CRA13	CRA12	CRA11	CRA10	CRA9	CRA8
CRA7	CRA6	CRA5	CRA4	CRA3	CRA2	CRA1	CRA0

D0

This base address (shifted left by 8 bits) is added to the 10 bit circuit reference address (shifted left by 4 bits) from the Transmit Descriptor to obtain the full 24 bit address of the Circuit Reference Table entry describing the circuit to be used when executing the requested transmission.

Register 2 – Transmit Queue Base Address Register

D15

0	0	X	X	X	X	TQA9	TQA8
TQA7	TQA6	TQA5	TQA4	TQA3	TQA2	TQA1	TQA0

D0

This register contains the upper10 bits of both the Transmit Pending and Buffer Release Queue addresses. This base address is concatenated with the start or end address (shifted left by 1 bit) or with the write or read pointers (shifted left by 1 bit) to obtain the upper 23 bits of the system or dual port SAR memory address of the Pending or Release Queue entry. Address bit 0 is always set to 0 by the ALC.

Fig. 30 – REGISTERS 0, 1 AND 2

Register 3 – Transmit Pending Queue Start Address Register

D15

X	X	X	TPS12	TPS11	TPS10	TPS9	TPS8
TPS7	TPS6	TPS5	TPS4	TPS3	TPS2	TPS1	TPS0

D0

This offset address is shifted left by one bit and concatenated to the Transmit Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Transmit Pending Queue start address. This start address indicates the beginning of the Transmit Pending Queue space which is used to pass transmit request buffer descriptor addresses from the Host to the ALC. Address bit 0 is always be set to 0 by the ALC.

Register 4 – Transmit Pending Queue End Address Register

D15

X	X	X	TPE12	TPE11	TPE10	TPE9	TPE8
TPE7	TPE6	TPE5	TPE4	TPE3	TPE2	TPE1	TPE0

D0

This offset address is shifted left by one bit and concatenated to the Transmit Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Transmit Pending Queue end address. This end address indicates the finish of the Transmit Pending Queue space which is used to pass transmit request buffer descriptor addresses from the Host to the ALC. Address bit 0 is always set to 0 by the ALC.

Register 5 – Transmit Pending Queue Write Pointer

D15

INCWRAP	EMPTY	FULL	TPW12	TPW11	TPW10	TPW9	TPW8
TPW7	TPW6	TPW5	TPW4	TPW3	TPW2	TPW1	TPW0

D0

This offset address is shifted left by 1 bit and concatenated to the Transmit Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Transmit Pending Queue write pointer. The Host uses this pointer when entering transmit requests by writing a transmit descriptor reference address to the transmit pending queue. Address bit 0 is always be set to 0 by the ALC.

INCWRAP – When writing to the host–controlled queue registers, if the most significant bit of the control data bus is set, the ALC will automatically increment its internal copy of the pointer being written to regardless of the pointer value specified on the data bus.

EMPTY – If this bit is set, it indicates that the ALC's pointer for the queue is at the same value as the host pointer's value returned by the read and that the queue is empty.

FULL – If this bit is set, it indicates that the host pointer and ALC pointer values are the same and that the queue is full.

Fig. 31 – REGISTER 3, 4 AND 5

Register 6 – Transmit Pending Queue Read Pointer

D15							D0
X	X	X	TPR12	TPR11	TPR10	TPR9	TPR8
TPR7	TPR6	TPR5	TPR4	TPR3	TPR2	TPR1	TPR0

This offset address is shifted left by 1 bit and concatenated to the Transmit Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Transmit Pending Queue read pointer. The ALC uses this pointer when retrieving transmit requests by reading a transmit descriptor reference address from the Transmit Pending Queue. Address bit 0 is always set to 0 by the ALC.

Register 7 – Buffer Release Queue Start Address Register

D15							D0
X	X	X	BRS12	BRS11	BRS10	BRS9	BRS8
BRS7	BRS6	BRS5	BRS4	BRS3	BRS2	BRS1	BRS0

This offset address shifted left by 1 bit is concatenated to the Transmit Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Transmit Release Queue start address. This start address indicates the beginning of the Transmit Release Queue space used by the ALC to indicate the availability of free transmit descriptors to the host. Address 0 is always set to 0.

Register 8 – Buffer Release Queue End Address Register

D15							D0
X	X	X	BRE12	BRE11	BRE10	BRE9	BRE8
BRE7	BRE6	BRE5	BRE4	BRE3	BRE2	BRE1	BRE0

This offset address shifted left by 1 bit is concatenated to the Transmit Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Transmit Release Queue end address. This end address indicates the finish of the Transmit Release Queue space used by the ALC to indicate the availability of free transmit descriptors to the host. Address 0 is always set to 0.

Fig. 32 – REGISTER 6, 7 AND 8

Register 9 – Buffer Release Queue Write Pointer

D15

X	X	X	BRW12	BRW11	BRW10	BRW9	BRW8
BRW7	BRW6	BRW5	BRW4	BRW3	BRW2	BRW1	BRW0

D0

This offset address is shifted left by one bit and concatenated to the Transmit Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Transmit Buffer Release Queue write pointer. The ALC uses this pointer when a packet transmission has been completed to return the transmit descriptor used to the pool of free transmit descriptors for use by the host in future transmit requests.

Register 10 – Buffer Release Queue Read Pointer

D15

INCWRAP	EMPTY	FULL	BRR12	BRR11	BRR10	BRR9	BRR8
BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0

D0

This offset address is shifted left by one bit and concatenated to the Transmit Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Transmit Buffer Release Queue read pointer. The Host uses this read pointer to obtain an available transmit descriptor when a packet is ready for transmission.

INCWRAP – When writing to the host–controlled queue registers, if the most significant bit of the control data bus is set, the ALC will automatically increment its internal copy of the pointer being written to regardless of the pointer value specified on the data bus.

EMPTY – If this bit is set, it indicates that the ALC's pointer for the queue is at the same value as the host pointer's value returned by the read and that the queue is empty.

FULL – If this bit is set, it indicates that the host pointer and ALC pointer values are the same and that the queue is full.

Fig. 33 – REGISTERS 9 and 10

Register 13 – CE/GFC Change Indication

D15

X	CE	GFC3	GFC2	GFC1	GFC0	RCR9	RCR8
RCR7	RCR6	RCR5	RCR4	RCR3	RCR2	RCR1	RCR0

D0

This register shows the status of the latest change in congestion experienced and GFC status with its associated Receive Circuit Reference.

CE: Status of Congestion Experienced Bit.

GFC3–0: Status of GFC Field (UNI mode only).

RCR9–0: Receive Circuit Reference of circuit with changed status.

Fig. 34 – REGISTER 13

Register 14 – DMA Burst Length Register

D15

RIF3	RIF2	RIF1	RIF0	TIF3	TIF2	TIF1	TIF0
DBL7	DBL6	DBL5	DBL4	DBL3	DBL2	DBL1	DBL0

D0

RIF3–RIF0: Receive Buffer Ready Interrupt Frequency.
This count specifies the frequency of receive buffer ready interrupts.

This value specifies the number of received buffers that are completed before the ALC generates a service request to the host using the Receive Buffer Ready Queue Write interrupt.

TIF3–TIF0: Transmit Buffer Release Interrupt Frequency.
This count specifies the frequency of transmit buffer release interrupts.

This value specifies the number of transmitted buffers that are completed with the IOC bit set before the ALC generates a service request to the host using the Receive Buffer Ready Queue Write interrupt.

DBL7–DBL0: This register may be set to limit the maximum number of ALC, system memory DMA access cycles that may occur in a single block. This burst length is applicable only when the ALC is operating in ready dependent, DMA mode.

A burst length limit of 0 indicates unlimited burst length.

A burst length limit in the range 1 – 255 indicates the maximum number of ALC DMA cycles that can occur before the bus is released to allow re-arbitration for control of the system bus.

Fig. 35 – REGISTER 14

Register 15 – DMA Mode Register

D15

SBL	PARSEL	SCE	BRSTO	BURSTD	DMAOPT	STEALO	STEALD
WMOD	RMOD	SYN	CMODE	MMODE	ORDER	BMODE1	BMODE0

D0

SBL: Single Cycle Burst Length. This selects between 8–transfer (set) and 4–transfer (cleared) data bursts.

PARSEL: Parity Select. This bit is set for odd parity and cleared for even parity.

SCE: Single Cycle Enable. This bit is set to enable single clock cycle burst data transfers

BURSTO: Bust Overhead. If this bit is set then the ALC will finish all control transfers for transmit before switching over to receive and vice versa.

BURSTD: Bust Data. If this bit is set then the ALC will finish all data transfers for transmit before switching over to receive and vice versa.

DMAOPT: DMA Optimise. Setting ths bit will cause the ALC to optimise the dead cycles between overhead operations.

STEALO: Steal Overhead. If this bit is set then the ALC will allow transmit to steal overhead cycles from receive and vice versa.

STEALD: Steal Data. If this bit is set then the ALC will allow transmit to steal data cycles from receive and vice versa.

Fig. 36 – REGISTER 15

Register 15 – DMA Mode Register (Continued)

D15

SBL	PARSEL	SCE	BRSTO	BURSTD	DMAOPT	STEALO	STEALD
WMOD	RMOD	SYN	CMODE	MMODE	ORDER	BMODE1	BMODE0

D0

WMOD:
0 WR signal as MB86686
1 WR signal extended.

RMOD:
0 Data sampled on falling edge of DCLK, RD signal as MB86686.
1 Data sampled on rising edge RD signal extended.

SYN:
0 DMA treated as asynchronous.
1 DMA treated as synchronous.

CMODE: SAR Memory Cycle Time.
This bit is cleared to select ready dependent SAR memory cycles (minimum cycle time = 2 x DCCLK) and set to select fast mode SAR memory cycles (cycle time = 2 x DCCLK).

MMODE: SAR Memory Mode.
This memory mode bit is set to select dual port RAM use for segmentation and reassembly and cleared to select DMA use of system memory for segmentation and reassembly.

ORDER: SAR Memory Byte Ordering Convention.
This bit is cleared to select Big Endian (Motorola/SPARC) byte ordering and set to select Little Endian (Intel/DEC Alpha) byte ordering. This byte ordering only applies to the transmit and receive buffer data. Descriptor data uses the Little Endian ordering convention. The queue data format is configurable as Big Endian or Little Endian, using word swapping.

BMODE1–0: SAR Memory Control Signal Mode.
00 Intel / GP Timings
01 Intel 486 Timings
10 Motorola Timings
11 Motorola 68x40 timings

Fig. 37 – REGISTER 15 contd.

Register 16 – Control Register

D15

MBRQE	VPB2	VPB1	VPB0	AF17	AF16	UNSEL	DCOAM
OAMCRC	RDAU	TSTLP	RSTRT	INIT	SRST	CWRE	MAAL5L

D0

MBRQE: Enable Buffer Ready Queue Interrupt when M=0. When in streaming mode setting this bit will cause a buffer ready queue interrupt to occur every time a packet is terminated (M=0) irrespective of the setting of the receive buffer Interupt frequency.

VPB2–0: Virual Path Detect bits (Valid range 000 – 101). These are used to control how many bits of the VP are used in the receive address mapping.

AF17–16: Address Filter Bits 17 –16. These are the 2 msbs of the receive address filter. For a full description of this function see section 3.5.8.

UNSEL: UNI/NNI Select. If set this bit uses an NNI address for filtering (uses all 18 bits of Address Filter). If it is cleared it uses a UNI address for filtering (used only 14 lsbs of the Address Filter)

DCOAM: Discard OAM. If this bit is set the ALC will discard all cells received (excepting F4 cells) which are not user data cells.

Fig. 38 – REGISTER 16

Register 16 – Control Register (Continued)

D15

MBRQE	VPB0	VPB1	VPB2	AF17	AF16	UNSEL	DCOAM
OAMCRC	RDAU	TSTLP	RSTRT	INIT	SRST	CWRE	MAAL5L

D0

OAMCRC: OAM CRC checking. This bit should be set to enable CRC–10 checking on all non–user data cells excepting F4 cells.

RDAU: Receive Descriptor Auto Update of Remaining Capacity. Setting this bit enables automatic initialisation of the bytes remaining field in the Receive Descriptor with the Buffer Size field and automatic clearing of the Bytes Received field.

TSTLP: Test Loop Enable.
When this bit is set the ALC's transmit cell stream interface is internally looped back into the receive cell stream interface using TXCLK.

RSTRT: ALC Cell Stream Interface Daisy Chain Restart.
When this bit is set a daisy chain token pulse is generated on ALC's TOUT line. This is used to restart the token daisy chain if the token has been lost.

INIT: Host Initialisation Complete.
This bit is set by the Host when it (the host) has completed all required initialisation of ALC registers and memory structures.

SRST: ALC Software Reset.
This bit is set to reset all internal ALC circuitry.

CWRE: ALC Host Queue Pointer Initialisation Enable.
This bit is set to allow the Host to initialise the Transmit Pending Queue Read Pointer, the Transmit Buffer Release Queue Write Pointer, the Receive Buffer Free Queue Read Pointer and the Receive Buffer Ready Queue Write Pointer.
This bit should be cleared after initialisation for normal operation.

MAAL5L: Maintain AAL5 Length. Setting this bit will cause the ALC to automatically compute the AAL5 length field across multiple chained or streamed transmit buffers

Fig. 39 – REGISTER 16 contd.

Register 17 – Mode Register

D15

TRTL1	TRTL0	AM	BAS	VPF	HEC2	HEC1	HEC0
BCHAIN	SMODE	DCHAIN	DMASK	0	RID	RTL1	RTL0

D0

TRTL1 – TRTL0: Transmit Routing Tag Length.
This field specifies the length (if any) of routing tag to be appended to all transmitted cells.
00: No Routing Tag
01: One Octet Routing Tag
10: Two Octet Routing Tag
11: Three Octet Routing Tag.

AM: Traffic Rate Averaging Method.
This bit is cleared to select the single leaky bucket (trickle) method of traffic rate averaging and set to select the double leaky bucket (burst) method. The method chosen applies to averaging for each individual virtual circuit and also for the total ALC output traffic.

BAS: Buffer Ageing Support.
This bit is set to support receive buffer ageing. For a full description of this function, please refer to section 3.1.6.

VPF: Virtual Path Filter Enable.
If this bit is set then only incoming cells whose VPI matches the value specified in the Receive Address Filter Register are processed. If this bit is cleared then the incoming VPI value is ignored.

HEC2 – HEC0: Header Error Check Operation.
Cell header error check mask byte value.

HEC2 = 0	Mask = 0x55.
HEC2 = 1	Mask = 0x00.
HEC1 = 0	Transmitted cell header check octet included (53 byte cell).
HEC1 = 1	Transmitted cell header check octet omitted (52 byte cell).
HEC0 = 0	Cell header error checking enabled.
HEC0 = 1	Cell header error checking disabled.

Fig. 40 – REGISTER 17

Register 17 – Mode Register (continued)

D15

TRTL1	TRTL0	AM	BAS	VPF	HEC2	HEC1	HEC0
BCHAIN	SMODE	DCHAIN	DMASK	0	RID	RTL1	RTL0

D0

BCHAIN: Receive Buffer Chaining Mode Enable
Set to enable chaining mode whereby a single packet may be located in different reassembly buffers each described by a different descriptor but linked using pointers into a single chain.
Cleared to disable buffer chaining.

SMODE: Receive Streaming Mode Enable
Set to enable ALC streaming mode whereby processing of large received packets can begin before all the packet data is available.
Cleared to disable streaming mode.

DCHAIN: Transmit Cell Stream Daisy Chain Enable
Set to allow multiple ALC devices to share a single network interface device by using token passing. Cleared if using a single ALC device per network interface device.

DMASK: Disable Transmit Queue Masking
Set to disable automatic service request masking from medium and low priority queues when the total ALC data rate limit is exceeded. Cleared to enable masking.

RID: Reassembly ID Select (applies to entire receive side of the ALC)
RID = 0: VCI is used for addressing.
RID = 1: MID field is used for addressing.

RTL1–RTL0: Receive Routing Tag Length
This field specifies the length (if any) of routing tag expected to be appended to received cells.
00: No Routing Tag
01: One Octet Routing Tag
10: Two Octet Routing Tag
11: Three Octet Routing Tag.

Fig. 41 – REGISTER 17 (continued)

Register 18 – Interrupt Status / Service Register

D15

X	PARERR	CEC	GFCC	DTCOM	RRCOM	SRCOM	BUSERR
TAC	RFE	TRF	TRW	RRFL	RRFU	RRW	INIT

D0

On detection of an interrupt condition the ALC sets an interrupt flag in this register. If the corresponding interrupt mask bit in Register 19 is set then the ALC activates the output interrupt pin. The host processor may determine the interrupt cause by reading this register. An interrupt is cleared and disabled by writing a ”1” to the associated bit and re–enabled by writing a ”0”.

TAC: Receive Status / Descriptor Table Access Complete.
Set when the host read or write access to the receive status/ descriptor table as requested through register 59 has completed.

RFE: Receive Buffer Free Queue Empty.
Set if no receive buffer descriptors are available for ALC use. Host must service previously received packets.

TRF: Transmit Buffer Release Queue Full.
Set if the last available location in the transmit buffer release queue has been used by the ALC. The host must respond to previously completed transmissions by reading the transmit release queue entries.

TRW: Transmit Buffer Release Queue Write.
Set when the ALC has completed the requested packet transmission. Host should acknowledge this by reading the corresponding release queue entry.

RRFL: Receive Buffer Ready Queue Write Fail.
Set if the ALC attempts to write to an already full receive buffer ready queue. The host must service previously received packets.

RRFU: Receive Buffer Ready Queue Full.
Set when the receive buffer ready queue is full. The host must service previously received packets.

RRW: Receive Buffer Ready Queue Write.
Set when the ALC has completed reception of a packet (or number of packets – see register 16). Host must acknowledge reception by reading the associated receive buffer ready queue entry.

INIT: Initialisation Complete.
Set when the ALC internal initialisation is complete.

Fig. 42 – REGISTER 18

Register 18 – Interrupt Status Register (continued)

D15							
X	PARERR	CEC	GFCC	DTCOM	RRCOM	SRCOM	BUSERR
TAC	RFE	TRF	TRW	RRFL	RRFU	RRW	INIT
							D0

PARERR: Parity Error on DMA Interface

CEC: Congestion Experienced Change. Circuit Changed in register 13

GFCC: GFC Field Change (UNI Mode only). Circuit changed in register 13

DTCOM: Descriptor Table Test Complete.
Set by the ALC to indicate that the ALC's internal RSD memory test has completed.

RRCOM: Receive RAM Test Complete.
Set by the ALC to indicate that the ALC's internal receive scratch pad memory test has completed.

SRCOM: Send RAM Test Complete.
Set by the ALC to indicate that the ALC's internal transmit scratch pad memory test has completed.

BUSERR Set by the ALC in Fast Mode when host activates the $\overline{\text{DTACK}}/\overline{\text{READY}}$ input to indicate a bus error

Register 19 – Interrupt Mask Register

This interrupt mask register contains one bit for each possible interrupt source as described for the Interrupt Status Register 18. above. Each interrupt condition can be enabled to activate the ALC's output interrupt signal by setting the corresponding interrupt mask bit in this register. Likewise each interrupt source can be prevented from activating the external interrupt pin by clearing the corresponding bit in this register.

For each mask location:

0 = Interrupt generation masked.
1 = Interrupt generation enabled.

In addition this register, when read indictes the revision of the MB86687. This is set to 0xXX00h.

Fig. 43 – REGISTER 18 (continued) and 19

1 = Interrupt generation enabled

Registers 20 to 31 – Transmit Queue Service Rate Registers

D15							D0
X	X	X	X	X	X	SC1	SC0
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

The Service Rate counters are used to implement leaky bucket traffic management on each of the ALC's 12 peak rate queues. Bits SR7 – SR0 are used to specify the rate at which tokens are removed from the leaky buckets of each circuit associated with that queue. In single leaky bucket mode this value determines the rate of cell transmission during the initial burst. In double leaky bucket mode this value determines the rate of cell transmission in each burst.

The counter value specified is decremented using a scaled version of the input transmission clock (TCLK). TCLK is divided by the scaling factor specified in bits SC0 and SC1 of this register as shown below. Each time the counter reaches zero it is reloaded to its initial value.

SC1	SC0	Scaling Factor
0	0	4
0	1	16
1	0	64
1	1	256

Note: The maximum value which SR0 – SR7 can take is given by:

$$\frac{L}{SCP}$$

Where L is cell width in nano-seconds, SCP the selected counter period integer multiple of the system clock period.

This maximum value corresponds to a single active Virtual Circuit using the total link capacity.

Register 20 = LP1
Register 31 = HP4

Fig. 44 – REGISTERS 20 to 31

Register 32 – Transmit Queue Service Enable Register

D15

X	X	ENL1	ENL2	ENL3	ENL4	ENM1	ENM2
ENM3	ENM4	ENH1	ENH2	ENH3	ENH4	ENAP	ENAA

D0

Servicing of each of the 12 available transmission descriptor queues can be enabled by setting and disabled by clearing their respective peak cell transmission rate counter enables as shown below. Also the total ALC peak and average rate counters can be individually enabled by setting and disabled by clearing the ENAP and ENAA bits respectively.

Low Priority Transmit Queue Service Enables:

ENL1: Enable counter for low priority service queue 1
ENL2: Enable counter for low priority service queue 2
ENL3: Enable counter for low priority service queue 3
ENL4: Enable counter for low priority service queue 4

Medium Priority Transmit Queue Service Enables:

ENM1: Enable counter for medium priority service queue 1
ENM2: Enable counter for medium priority service queue 2
ENM3: Enable counter for medium priority service queue 3
ENM4: Enable counter for medium priority service queue 4

High Priority Transmit Queue Service Enables:

ENH1: Enable counter for high priority service queue 1
ENH2: Enable counter for high priority service queue 2
ENH3: Enable counter for high priority service queue 3
ENH4: Enable counter for high priority service queue 4

Total ALC Traffic Management Counter Enables:

ENAP: Enable counter for ALC peak transmission rate.
ENAA: Enable counter for ALC average transmission rate.

Fig. 45 – REGISTER 32

Register 33 – ALC Peak Cell Transmission Rate Register

D15							D0
X	X	X	X	X	X	PS1	PS0
PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0

This total ALC output peak rate counter is used to implement leaky bucket traffic management on the ALC's transmitted cell stream. Bits PR7 – PR0 are used to specify the rate at which tokens are removed from the leaky bucket. In single leaky bucket mode this value determines the rate of cell transmission during the initial burst. In double leaky bucket mode this value determines the rate of cell transmission in each burst.

The counter value specified is decremented using a scaled version of the input transmission clock (TCLK). TCLK is divided by the scaling factor specified in bits PS0 and PS1 of this register as shown below. Each time the counter reaches zero it is reloaded to its initial value.

PS1	PS0	Scaling Factor
0	0	1
0	1	2
1	0	4
1	1	8

Register 34 – ALC Average Cell Transmission Rate Register

D15							D0
X	X	X	X	X	X	AS1	AS0
AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

This total ALC output average rate counter is used to implement leaky bucket traffic management on the ALC's transmitted cell stream. Bits AR7 – AR0 are used to specify the rate at which tokens are removed from the leaky bucket. In single leaky bucket mode this value determines the rate of cell transmission during the initial burst. In double leaky bucket mode this value determines the length of time that the output cell stream is idle between bursts.

The counter value specified is decremented using a scaled version of the input transmission clock (TCLK). TCLK is divided by the scaling factor specified in bits AS0 and AS1 of this register as shown below. Each time the counter reaches zero it is reloaded to its initial value.

AS1	AS0	Scaling Factor
0	0	1
0	1	2
1	0	4
1	1	8

Fig. 46 – REGISTER 33 AND 34

Register 35 – ALC Leaky Bucket Capacity Register

D15

X	X	X	X	X	X	X	X
LBC7	LBC6	LBC5	LBC4	LBC3	LBC2	LBC1	LBC0

D0

This register specifies the number of tokens held in the ALC total traffic management leaky bucket. This parameter together with the ALC peak transmission rate register setting and the ALC average transmission rate register setting determines the total cell transmission rate at the ALC's output.

This capacity value can be used together with the ALC peak cell rate and average cell rate to calculate the maximum burst length of transmitted cells generated by the ALC.

For Single Leaky Bucket Mode:

$$M = (B–1) \times (1–U)$$

In this case a minimum allowed value of B is specified for each selected U.

U = 0.875 minimum B = 9.
U = 0.75 minimum B = 5
U = 0.625 minimum B = 4

All other values of U minimum B = 3.

For Double Leaky Bucket Mode:

$$M = B \times (1–U)$$

B = maximum number of cells in the output burst.
M = leaky bucket capacity as specified in LBC7 – LBC0
U = utilisation = average cell output rate / peak cell output rate
= (AR7 – AR0) / (PR7 – PR0)

Note:
If the resulting value of M is not a positive integer then in the single leaky bucket method it should be rounded DOWN to the nearest positive integer and in the double leaky bucket method it should be rounded UP to the next positive integer.

Fig. 47 – REGISTER 35

Register 40 – Receive Queue Base Address Register

D15

X	X	X	X	X	X	RQA9	RQA8
RQA7	RQA6	RQA5	RQA4	RQA3	RQA2	RQA1	RQA0

D0

This register contains the upper10 bits of both the Recieve Buffer Free Queue and Buffer Ready Queue addresses. This base address is concatenated with the start or end address (shifted left by 1 bit) or with the write or read pointers (shifted left by 1 bit) to obtain the upper 23 bits of the system or dual port SAR memory address of the Pending or Release Queue entry. Address bit 0 is always set to 0 by the ALC.

Register 45 – Receive Descriptor Table Base Address Register

D15

RDA15	RDA14	RDA13	RDA12	RDA11	RDA10	RDA9	RDA8
RDA7	RDA6	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

D0

This base address (shifted left by 8 bits) is added to the 12 bit receive descriptor address (shifted left by 5 bits) from the Receive Buffer Ready Queue or Receive Buffer Free queue entry to obtain the full 24 bit address of the receive descriptors.

Register 41 – Receive Buffer Free Queue Start Address Register

D15

X	X	X	RBFS12	RBFS11	RBFS10	RBFS9	RBFS8
RBFS7	RBFS6	RBFS5	RBFS4	RBFS3	RBFS2	RBFS1	RBFS0

D0

This offset address is shifted left by one bit and concatenated to the Recieve Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Recieve Pending Queue start address. This start address indicates the beginning of the Recieve Pending Queue space which is used to pass recieve request buffer descriptor addresses from the Host to the ALC. Address bit 0 is always be set to 0 by the ALC.

Fig. 48 – REGISTER 40, 45 AND 41

Register 42 – Receive Buffer Free Queue End Address Register

D15

X	X	X	RBFE12	RBFE11	RBFE10	RBFE9	RBFE8
RBFE7	RBFE6	RBFE5	RBFE4	RBFE3	RBFE2	RBFE1	RBFE0

D0

This offset address is shifted left by one bit and concatenated to the Recieve Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Recieve Pending Queue end address. This end address indicates the finish of the Receive Pending Queue space which is used to pass Receive request buffer descriptor addresses from the Host to the ALC. Address bit 0 is always set to 0 by the ALC.

Register 43 – Receive Buffer Free Queue Write Pointer

D15

INCWRAP	EMPTY	FULL	RBFW12	RBFW11	RBFW10	RBFW9	RBFW8
RBFW7	RBFW6	RBFW5	RBFW4	RBFW3	RBFW2	RBFW1	RBFW0

D0

This offset address is shifted left by 1 bit and concatenated to the Receive Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Receive Pending Queue write pointer. The Host uses this pointer when entering Receive requests by writing a receive descriptor reference address to the Receive pending queue. Address bit 0 is always be set to 0 by the ALC.

INCWRAP – When writing to the host–controlled queue registers, if the most significant bit of the control data bus is set, the ALC will automatically increment its internal copy of the pointer being written to regardless of the pointer value specified on the data bus.

EMPTY – If this bit is set, it indicates that the ALC's pointer for the queue is at the same value as the host pointer's value returned by the read and that the queue is empty.

FULL – If this bit is set, it indicates that the host pointer and ALC pointer values are the same and that the queue is full.

Register 44 – Receive Buffer Free Queue Read Pointer

D15

X	X	X	RBFR12	RBFR11	RBFR10	RBFR9	RBFR8
RBFR7	RBFR6	RBFR5	RBFR4	RBFR3	RBFR2	RBFR1	RBFR0

D0

This offset address is shifted left by 1 bit and concatenated to the Receive Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Receive Pending Queue read pointer. The ALC uses this pointer when retrieving transmit requests by reading a receive descriptor reference address from the Receive Pending Queue. Address bit 0 is always set to 0 by the ALC.

Fig. 49 – REGISTER 42, 43 AND 44

Register 46 – Receive Buffer Ready Queue Start Address Register

D15

X	X	X	RBRS12	RBRS11	RBRS10	RBRS9	RBRS8
RBRS7	RBRS6	RBRS5	RBRS4	RBRS3	RBRS2	RBRS1	RBRS0

D0

This offset address shifted left by 1 bit is concatenated to the Receive Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Receive Release Queue start address. This start address indicates the beginning of the Receive Release Queue space used by the ALC to indicate the availability of free Receive descriptors to the host. Address 0 is always set to 0.

Register 47 – Receive Buffer Ready Queue End Address Register

D15

X	X	X	RBRE12	RBRE11	RBRE10	RBRE9	RBRE8
RBRE7	RBRE6	RBRE5	RBRE4	RBRE3	RBRE2	RBRE1	RBRE0

D0

This offset address shifted left by 1 bit is concatenated to the Receive Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Receive Release Queue end address. This end address indicates the finish of the Receive Release Queue space used by the ALC to indicate the availability of free Receive descriptors to the host. Address 0 is always set to 0.

Fig. 50 – REGISTER 46 AND 47

Register 48 – Receive Buffer Ready Queue Write Pointer

D15

X	X	X	RBRW12	RBRW11	RBRW10	RBRW9	RBRW8
RBRW7	RBRW6	RBRW5	RBRW4	RBRW3	RBRW2	RBRW1	RBRW0

D0

This offset address is shifted left by 1 bit and concatenated to the Receive Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Receive Buffer Ready Queue write pointer. The ALC uses this pointer to write the address of the Receive Descriptor for a received packet which has been reassembled and placed in the receive buffer. Address bit 0 is always set to 0.

Register 49 – Receive Buffer Ready Queue Read Pointer

D15

INCWRAP	EMPTY	FULL	RBRR12	RBRR11	RBRR10	RBRR9	RBRR8
RBRR7	RBRR6	RBRR5	RBRR4	RBRR3	RBRR2	RBRR1	RBRR0

D0

This offset address is shifted left by 1 bit and concatenated to the Receive Queue Base Address Register contents (shifted left by 14 bits) to obtain the upper 23 bits of the Receive Buffer Ready Queue read pointer. The Host uses this pointer to read the address of the Receive Descriptor for a received packet which has been reassembled and placed in the receive buffer. Address bit 0 is always set to 0.

Register 50 – Dropped Packet Counter

D15

DPC15	DPC14	DPC13	DPC12	DPC11	DPC10	DPC9	DPC8
DPC7	DPC6	DPC5	DPC4	DPC3	DPC2	DPC1	DPC0

D0

This counter is incremented each time a received packet is lost because no receive buffer space is available to hold the incoming data. Reading of this register will cause its value to be reset to zero.

Fig. 51 – REGISTER 48, 49 AND 50

Register 51 – Receive Buffer Time Out Counter Period Register

D15

BTC15	BTC14	BTC13	BTC12	BTC11	BTC10	BTC9	BTC8
BTC7	BTC6	BTC5	BTC4	BTC3	BTC2	BTC1	BTC0

D0

The value in this register represents the number of DCCK clock periods required to increment the receive buffer ageing time base counter. this value is used to pre scale the ALC input DCCK clock before clocking the ALC's time base counter. The time base counter is used to check for receive buffer time out conditions

Register 52 – Receive Buffer Time Out Counter Interval Register

D15

BTI15	BTI14	BTI13	BTI12	BTI11	BTI10	BTI9	BTI8
BTI7	BTI6	BTI5	BTI4	BTI3	BTI2	BTI1	BTI0

D0

The value written to this register defines the maximum time period allowed between the arrival of a incoming packet and the host servicing the receive buffer.

If the time required by the host to service received packets exceeds this value then the Received Buffer Ready Queue Status code of 1100b indicating receive buffer timeout condition is written to the Receive Buffer Ready Queue entry corresponding to that channel. The ALC's time base counter is incremented using the DCCK clock pre-scaled by the value in the Receive Buffer Time Out Counter Period register as described above.

Fig. 52 – REGISTERS 51 AND 52

Register 53 – Receive Buffer Ready Data Hold Register

D15

DHR15	DHR14	DHR13	DHR12	DHR11	DHR10	DHR9	DHR8
DHR7	DHR6	DHR5	DHR4	DHR3	DHR2	DHR1	DHR0

D0

When the ALC receives an incoming packet while only a single location is available in the Receive Buffer Ready Queue, writing the Receive Buffer entry corresponding to this packet will cause the generation of the Receive Buffer Ready Queue Full Interrupt . If a further packet is received after this interrupt but before the host has serviced the Receive Buffer Ready Queue then no Receive Buffer Ready queue space is available to hold the packet received indication. In this case the ALC instead writes the Receive Buffer Ready Queue entry to this Receive Buffer Ready Data Hold Register and generates the Receive Buffer Ready Queue Write Fail interrupt. Note that if additional packets are received the value in this register will be overwritten with the most recently received packet's Receive Buffer Ready Queue entry data.

Register 54 – Maximum Received Packet Length Register

D15

MPL15	MPL14	MPL13	MPL12	MPL11	MPL10	MPL9	MPL8
MPL7	MPL6	MPL5	MPL4	MPL3	MPL2	MPL1	MPL0

D0

This register contains the maximum number of bytes of incoming packet data that can be received by the ALC. If the length of the received packet exceeds this number then the ALC will deliver the packet but drop the cells beyond the level programmed.

Register 55 – Dropped Cell Counter

D15

DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0

D0

This counter value is incremented each time a received cell is dropped by the ALC due to protocol errors. Reading of this register will cause its value to be reset to zero.

Fig. 53 – REGISTER 53, 54 AND 55

Register 56 – Receive Address Filter Register

D15

AF15	AF14	AF13	AF12	AF11	AF10	AF9	AF8
AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0

D0

Address Filter These bits, together with AF17 and AF16 in Register 16, are used as a filter for those address bits not covered in the 10 bits of the ALC mapped address.

Fig. 54 – REGISTER 56

Register 57 – Host Receive Descriptor / Status Table Read Register

D15

DP	RIP	DSC11	DSC10	DSC9	DSC8	DSC7	DSC6
DSC5	DSC4	DSC3	DSC2	DSC1	DSC0	ACT	DCRD

D0

This register is used by the host to read the Receive Descriptor / Status Table.
This table specifies the location and status of specific receive channel descriptors.

DSC0 – DSC11: Receive descriptor pointer for this Receive Circuit Reference.

DP: Receive descriptor pointer in DSC0 – DSC11 above is valid.

RIP: Reception in progress on the Receive Circuit Reference corresponding to this entry.

ACT: Active monitoring of the Receive Circuit Reference corresponding to this entry.

DCRD: Discard in progress on the channel referenced by this entry.

Register 58 – Host Receive Descriptor / Status Table Write Register

D15

DP	RIP	DSC11	DSC10	DSC9	DSC8	DSC7	DSC6
DSC5	DSC4	DSC3	DSC2	DSC1	DSC0	ACT	DCRD

D0

This register is used in conjunction with the Host Receive Descriptor / Status Table Access Register by the host to write Receive Descriptor / Status Table entries.
The host normally accesses this table only during initialisation.

DSC0 – DSC11: Receive descriptor pointer for this Receive Circuit Reference.

DP: Receive descriptor pointer in DSC0 – DSC11 above is valid.

RIP: Set Receive in progress on the Receive Circuit Reference corresponding to this entry.

ACT: Activate monitoring of the Receive Circuit Reference corresponding to this entry

DCRD: Discard received packets on the channel referenced by this entry.

Fig. 55 – REGISTER 57 and 58

Register 59 – Host Receive Descriptor / Status Table Access Register

D15

HOSTR	$\overline{RD}$/WR	AAL TYP0	AAL TYP1	RES	RES	RCR9	RCR8
RCR7	RCR6	RCR5	RCR4	RCR3	RCR2	RCR1	RCR0

D0

This register is used, together with registers 57 and 58 to gain read and write access to the ALC's internal Receive Descriptor / Status Table. The tables need to be accessed by the host for initialization, scatter/gather mode and emergency buffer recovery.

When the Host Access Request (HOSTR) bit is set and the read/write control (RD/WR) bit is SET, the contents of register 58 and the AAL Type bits are written to the table entry at the address indicated by RCR 0:9. The ALC will generate a TAC interrupt to indicate that the write operation is complete.

When the Host Access Request (HOSTR) bit is set and the read/write control bit (RD/WR) is CLEARED, the ALC is configured to read the internal Receive Descriptor / Status Table entry at the address indicated by RCR 0:9. The ALC will generate a TAC interrupt to indicate that the read operation is complete. At this time Register 57 will contain the requested table entry contents.

RCR0 –RCR9: This is the Table address Receive Circuit Reference.

AAL TYP:
00 AAL3/4
01 Transparent Mode
10 Transparent Cell Mode
11 AAL5.

HOSTR:
Set to 1: Host Access Requested
Cleared to 0: Host Access Completed.

RD/WR:
Set to 1: Write Request
Cleared to 0: Read Request.

Fig. 56 – REGISTER 59

C. RATINGS

C.1 Absolute Maximum Ratings

Rating	symbol	Values		Units
		Min	Max	
Positive Supply Voltage	$+V_{DD}$	–0.5	6.0	V
Input Voltage	V_{DIN}	–0.5	$+V_{DD}$ + 0.5	V
Output Voltage	V_{O1}	–0.5	$+V_{DD}$ + 0.5	V
Input Current	I_{MAX}	–10.0	125	μA
Storage Temperature	T_{STG}	–40	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Rating**s are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C.2 DC Characteristics

Parameter	Symbol	Pin	Test Condition	Value			Unit
				Min.	Typ.	Max.	
Positive Supply Voltage	V_{DD}		+4.75	+4.75	+5.0	+5.25	V
Positive Supply Current	$+I_{VS}$		Static no load	–	–	100	mA
Input High Voltage (TTL)	V_{IH}			2.2	–	$+V_{DD}$	V
Input Low Voltage (TTL)	V_{IL}			0	–	0.8	V
Input Leakage Current	I_L		$0<=V_I<=+V_{DD}$	–10	–	10	μA
Output Low Voltage	V_{OL}		I_{OL}=3.2mA	V_{SS}	–	0.4	V
Output High Voltage	V_{OH}		I_{OH}=–2mA	4.2	–	V_{DD}	V
Output Off Leakage Current	I_{LO}			–10	–	10	mA
Input Pin Capacitance	C_{in}			–	–	8	pF
Output Pin Capacitance	C_{out}			–	–	16	pF
I/O Pin Capacitance	$C_{i/o}$			–	–	21	pF
Operating Temperature	T_A			0	–	+70	°C
Power Dissipation (operating)	P_O				1000		mW

D. AC TIMINGS

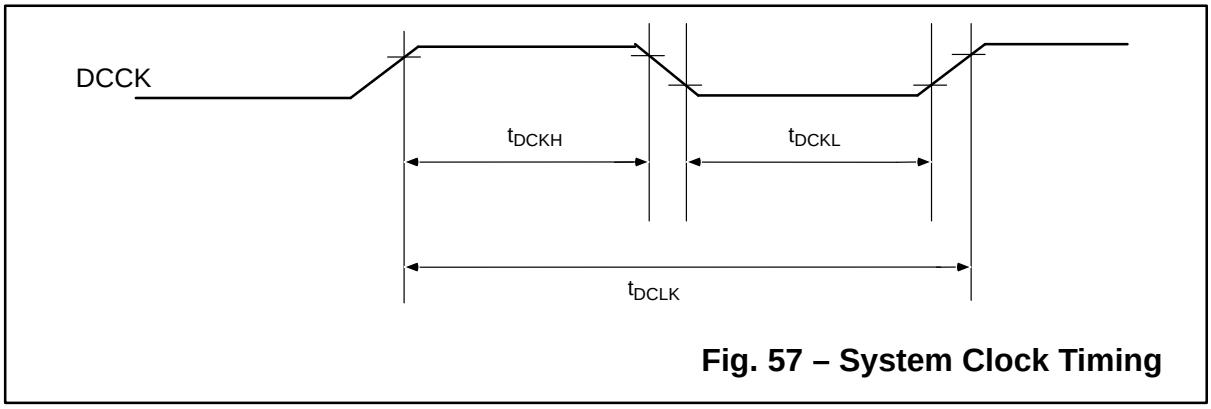


Fig. 57 – System Clock Timing

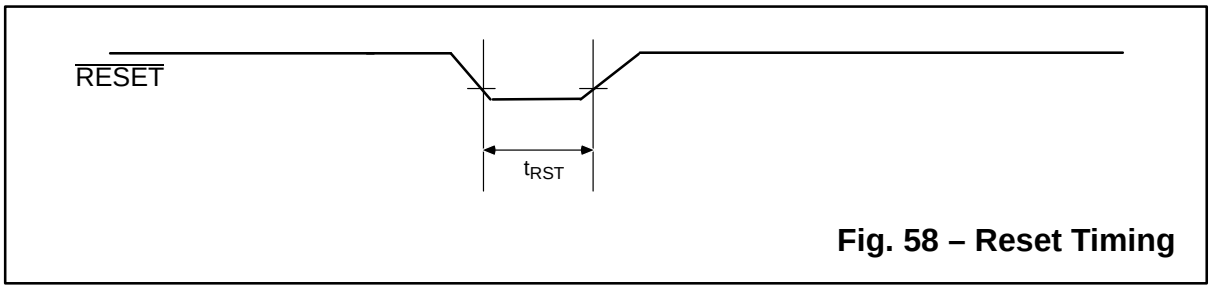


Fig. 58 – Reset Timing

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
Clock High Time	DCCK	t_{DCKH}				ns
Clock Low Time	DCCK	t_{DCKI}				ns
Clock Period	DCCK	t_{DCLK}	30*			ns
Reset Pulse Width	$\overline{RESET}$	t_{RST}	10 t_{DCLK}			ns

Table 3 – Miscellaneous – AC Timing Parameters

*** Note:** In certain operating modes,the clock period is restricted to 40ns. These modes are:

i) Cache operations,

ii) Single cycle operation with 0 wait states.

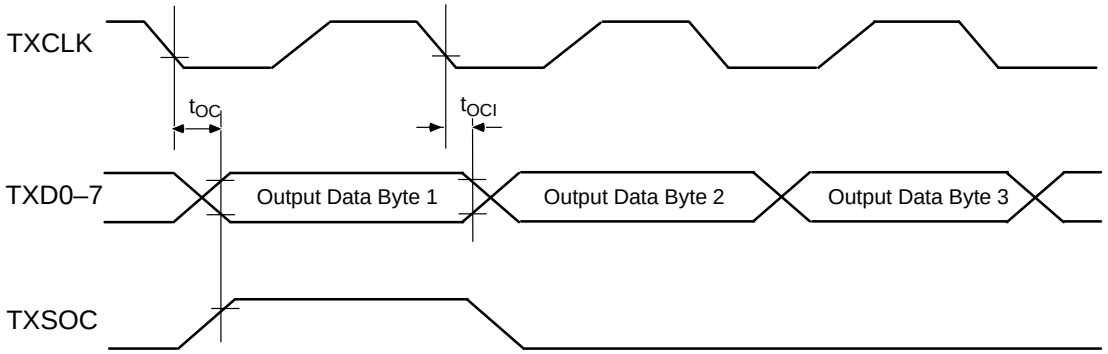


Fig. 59 – Cell Stream Interface Transmit Port (Fujitsu Mode) Timing

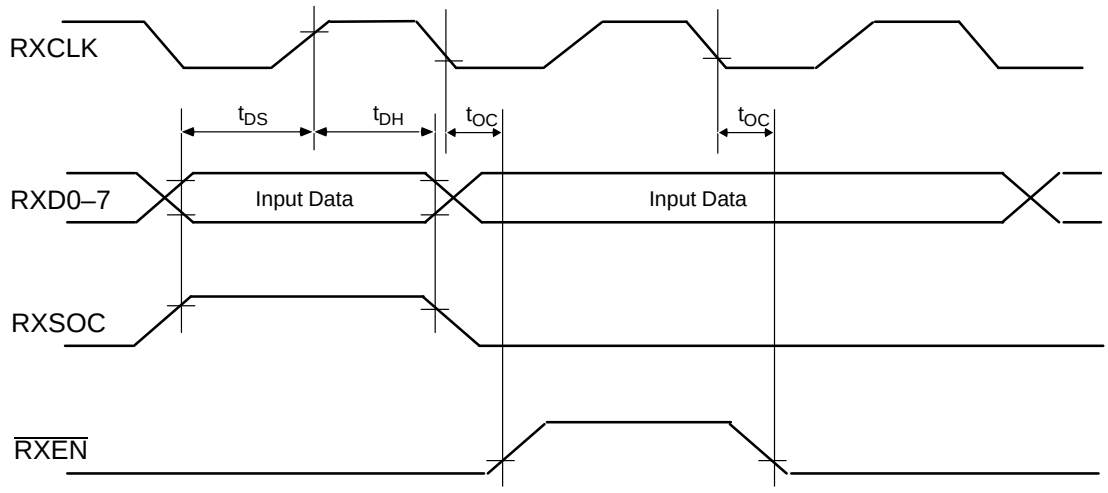


Fig. 60 – Cell Stream Interface Receive Port (Fujitsu Mode) Timing

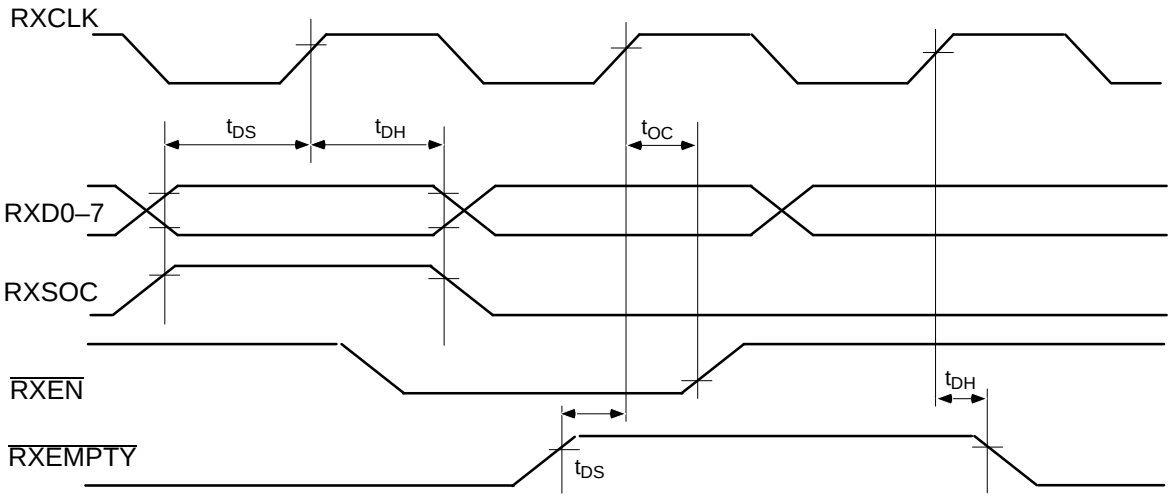


Fig. 61 – Cell Stream Interface Receive Port (Utopia mode) Timing

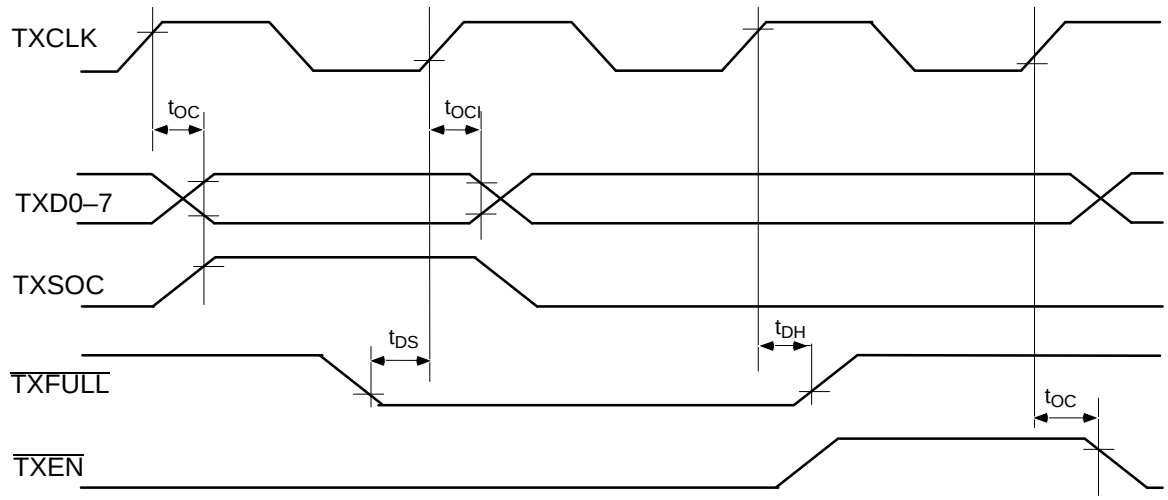


Fig. 62 – Cell Stream Interface Transmit Port (Utopia mode) Timing

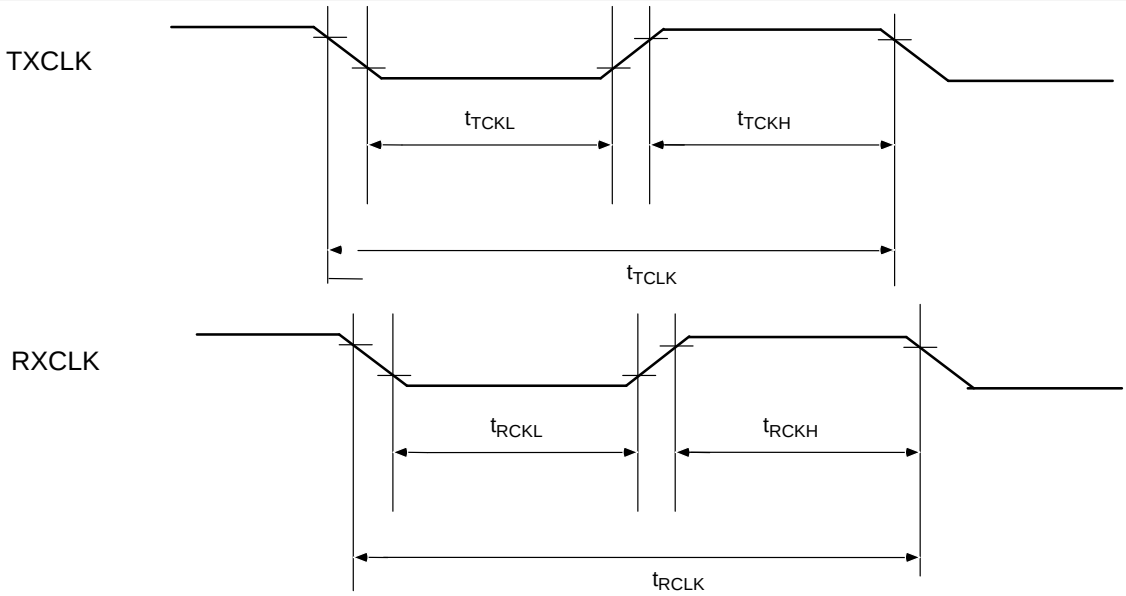


Fig. 63 – Cell Stream Clock Timing

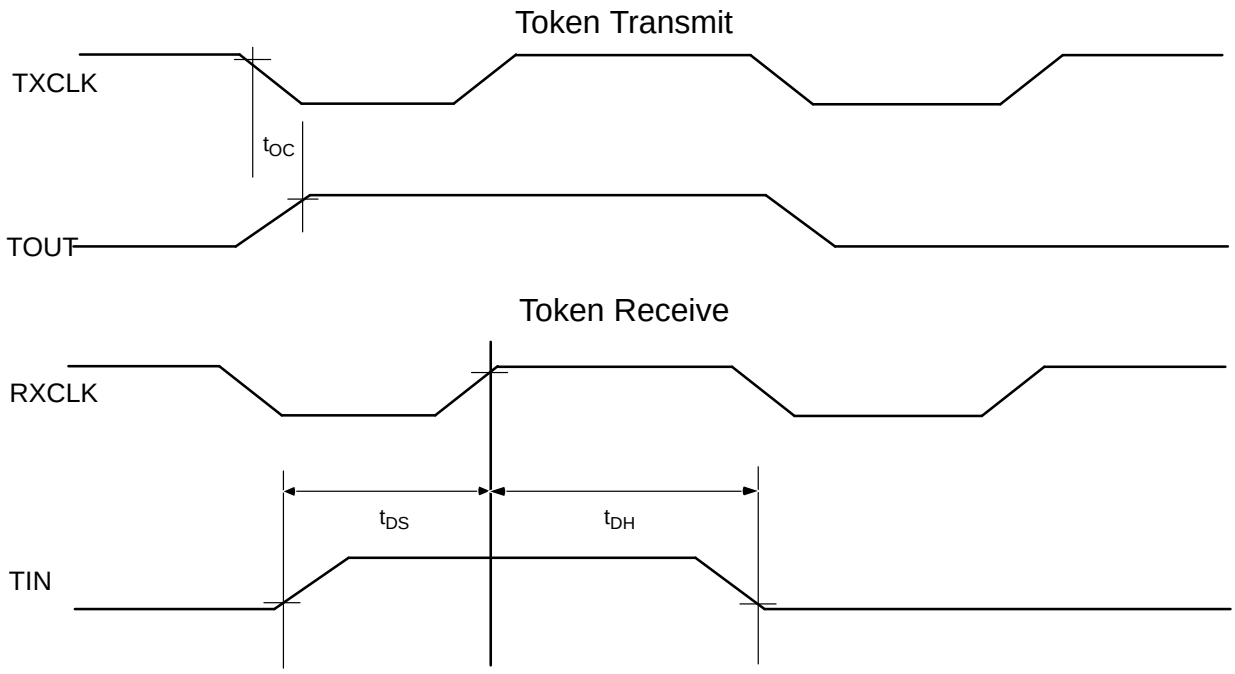


Fig. 64 – CSI Token Transmit and Receive Timing

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
Transmit Clock High Time	TXCLK	t_{TCKH}	15			ns
Transmit Clock Low Time	TXCLK	t_{TCKL}	15			ns
Transmit Clock Period	TXCLK	t_{TCLK}	50*			ns
Receive Clock High Time	RXCLK	t_{RCKH}	13			ns
Receive Clock Low Time	RXCLK	t_{RCKL}	14			ns
Receive Clock Period	RXCLK	t_{RCLK}	50*			ns

Table 4 – Cell Stream Interface clocks – AC Timing Parameters

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
RXSOC, RXD Setup Time	RXCLK	t_{DS}	0			ns
RXSOC, RXD Hold Time	RXCLK	t_{DH}	8			ns
RXEN Delay	RXCLK	t_{OC}	12		17	ns
TXSOC, TXD Active Delay	TXCLK	t_{OC}	11		17	ns
TXD Inctive Delay	TXCLK	t_{OCI}	10			ns

Table 5 – Cell Stream Interface Fujitsu Mode – AC Timing Parameters

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
RXSOC, RXD, RXEMPTY Setup	RXCLK	t_{DS}	0			ns
RXSOC, RXD, RXEMPTY Hold	RXCLK	t_{DH}	8			ns
RXEN Delay	RXCLK	t_{OC}	14		19	ns
TXSOC, TXD, TXEN Delay	TXCLK	t_{OC}	10		18	ns
TXD Inactive Delay	TXCLK	t_{OC}	10			ns
TXFULL Setup Time	TXCLK	t_{DS}	2			ns
TXFULL Hold Time	TXCLK	t_{DH}	3			ns

Table 6 – Cell Stream Interface UTOPIA Mode – AC Timing Parameters

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
TIN Setup Time	TXCLK	t_{DS}	0			ns
TIN Hold Time	TXCLK	t_{DH}	5			ns
TOUT Delay	TXCLK	t_{OC}	14		18	ns

Table 7 – Cell Stream Interface Token Passing – AC Timing Parameters

*** Note:** The period of TXCLK and RXCLK must be greater or equal to the period of DCCK.

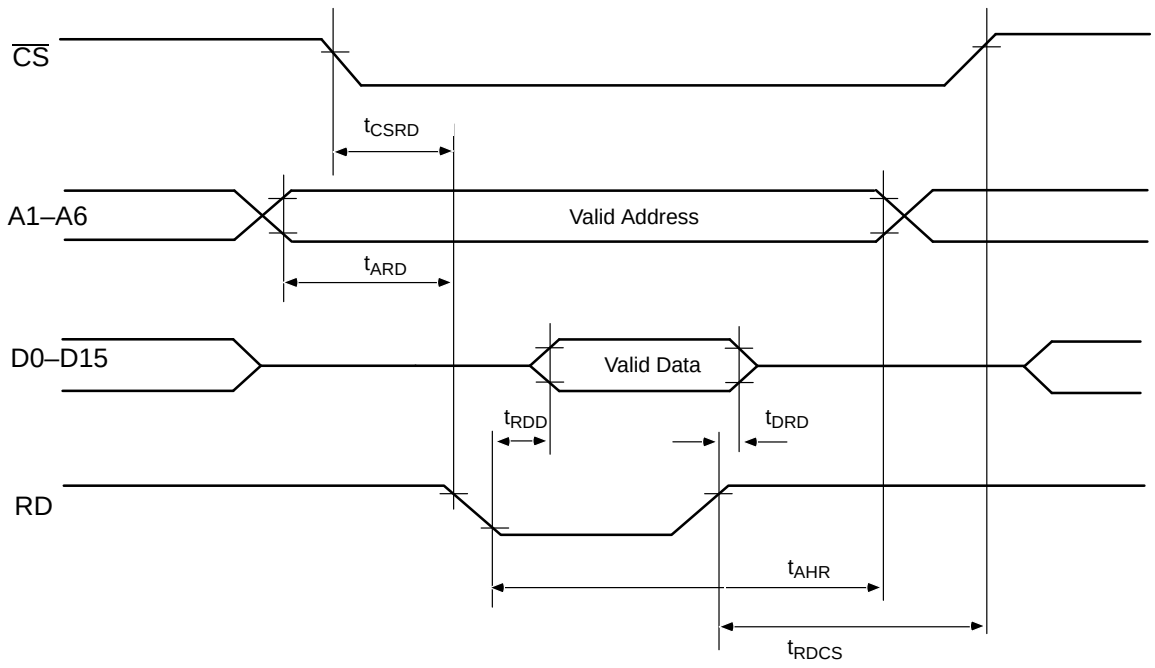


Fig. 65 – Microprocessor Interface – Read Timing

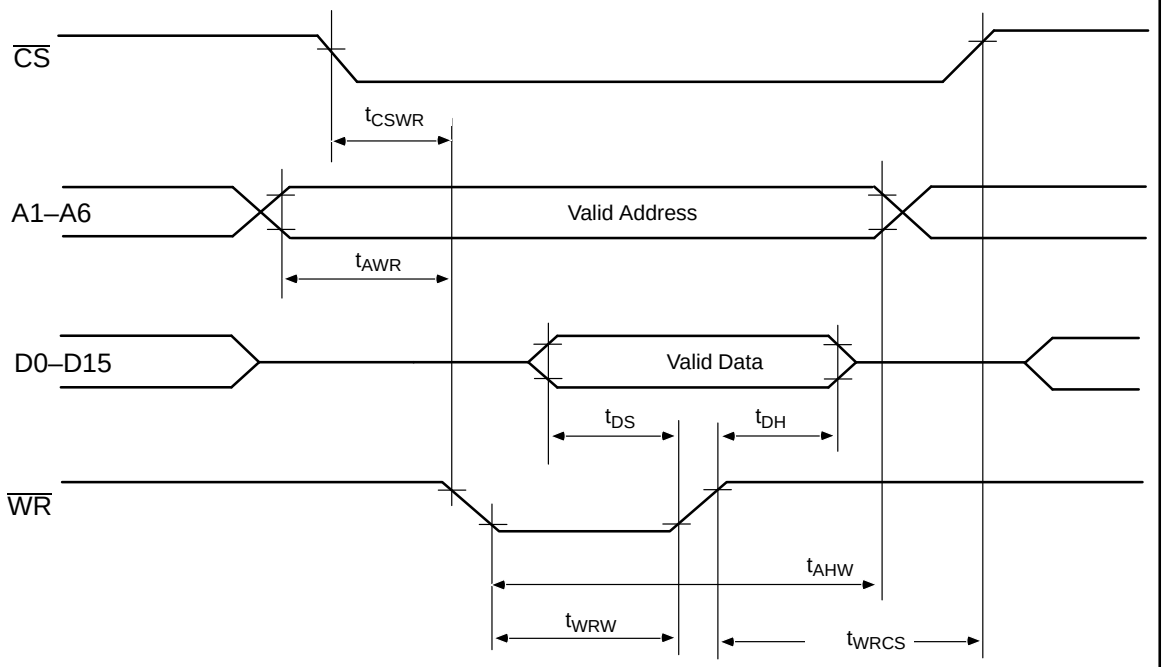


Fig. 66 – Microprocessor Interface – Write Timing

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
Address Valid to Read Active	$\overline{RD}$	t_{ARD}	0			ns
$\overline{CS}$ Valid to Read Active	$\overline{RD}$	t_{CSRD}	0			ns
Read Active to Valid Data	$\overline{RD}$	t_{RDD}	22		33	ns
Read Inactive to Invalid Data	$\overline{RD}$	t_{DRD}	10			ns
Read Active to Invalid Address	$\overline{RD}$	t_{AHR}	5			ns
Read Inactive to $\overline{CS}$ Inactive	$\overline{RD}$	t_{RDCS}	0			ns
Address Active to Write Active	$\overline{WR}$	t_{AWR}	0			ns
$\overline{CS}$ Valid to Write Active	$\overline{WR}$	t_{CSWR}	0			ns
Write Pulse Width	$\overline{WR}$	t_{WRW}	3			ns
Data Setup Time	$\overline{WR}$	t_{DS}	5			ns
Data Hold Time	$\overline{WR}$	t_{DH}	0			ns
Write Inactive to Invalid Address	$\overline{WR}$	t_{AHW}	5			ns
Write Inactive to $\overline{CS}$ Inactive	$\overline{WR}$	t_{WRCS}	0			ns

Table 8 – Microprocessor Interface – AC Timing

Fig. 67 – Microprocessor Interface – Write to Write Timing

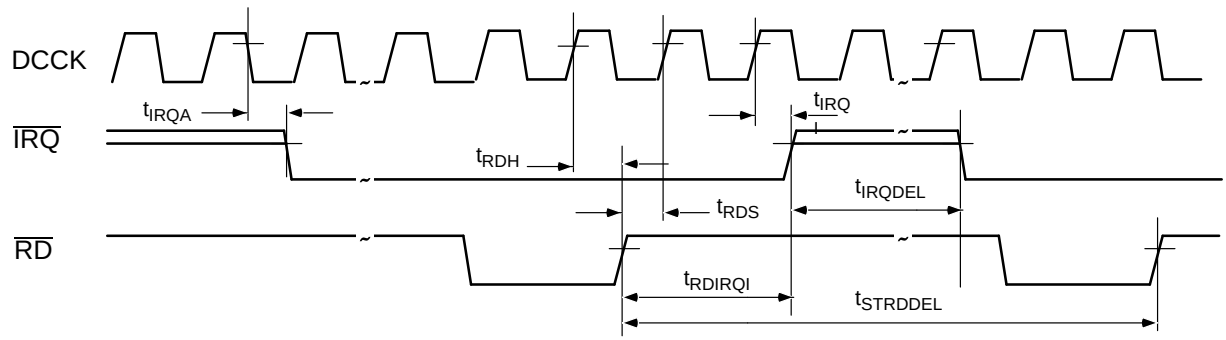


Fig. 68 – Microprocessor Interface – Interrupt Timing

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
Write to Write Delay – DCLK	$\overline{WR}$	t_{WWD}	4DCLK			ns
Write to Write Delay – TCLK	$\overline{WR}$	t_{WWT}	4TCLK			ns
$\overline{IRQ}$ Active Delay	$\overline{IRQ}$	t_{IRQA}	11		15	ns
Setup Time of $\overline{RD}$ Inactive	$\overline{RD}$	t_{RDS}	0			ns
Hold Time of $\overline{RD}$ Inactive	$\overline{RD}$	t_{RDH}	5			ns
RD Inactive to $\overline{IRQ}$ Inactive	$\overline{RD}$ $\overline{IRQ}$	t_{RDIRQI}	DCLK		2DCLK	ns
$\overline{IRQ}$ Inactive Delay	$\overline{IRQ}$	t_{IRQI}	38		42	ns
$\overline{IRQ}$ Inactive to Active	$\overline{IRQ}$	t_{IRQDEL}	2DCLK			ns
Read to Read Delay Interrupt Status Register	$\overline{WR}$	$t_{STRDDEL}$	4DCLK			ns

Table 9 – Microprocessor Interface – AC Timing

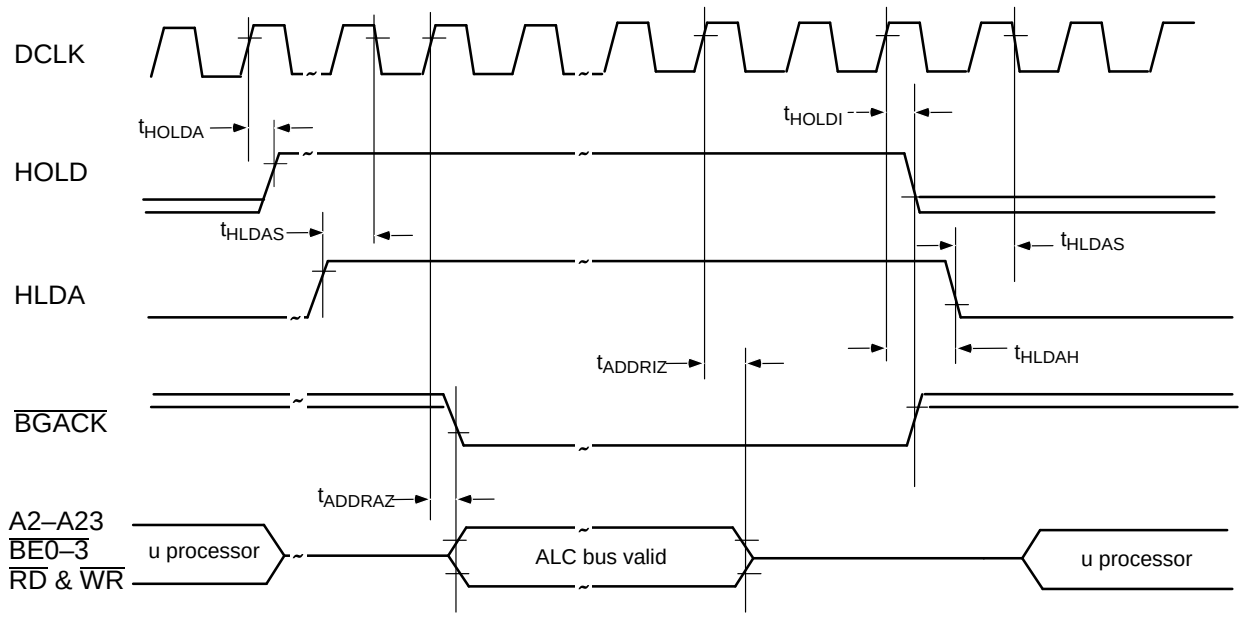


Fig. 69 – Microprocessor Interface – Intel DMA Access Timing

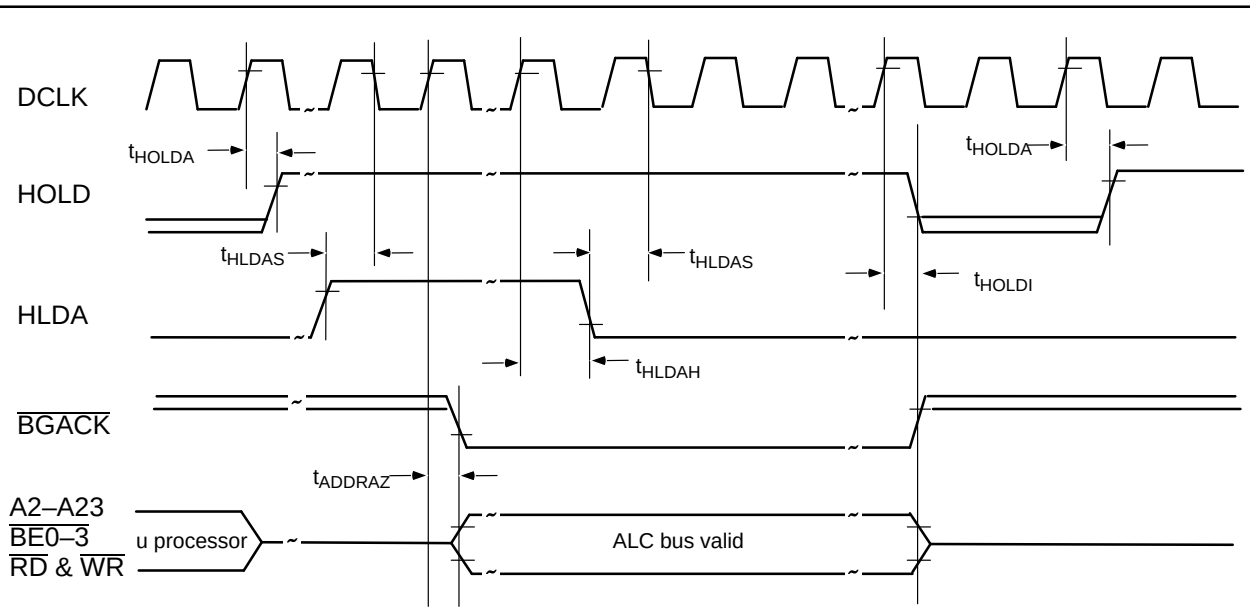


Fig. 70 – Microprocessor Interface – Intel DMA Access Control Override Timing

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
HOLD Active Delay	HOLD	t_{HOLDA}	9		14	ns
HOLD Inactive Delay	HOLD	t_{HOLDI}	50		72	ns
Setup Time of HLDA Active	HLDA	t_{HLDAS}	0			ns
Hold Time of HLDA Invalid	HLDA	t_{HLDAH}	2			ns
ALC Bus Active Delay	A2–A23, BE3–0, $\overline{MRD}$, $\overline{MWR}$,	t_{ADDRAZ}	10		30	ns
ALC Bus Inactive Delay	A2–A23, BE3–0, $\overline{MRD}$, $\overline{MWR}$	t_{ADDRIZ}	25		72	ns

Table 10 – Microprocessor Interface – Intel DMA Access AC Timing

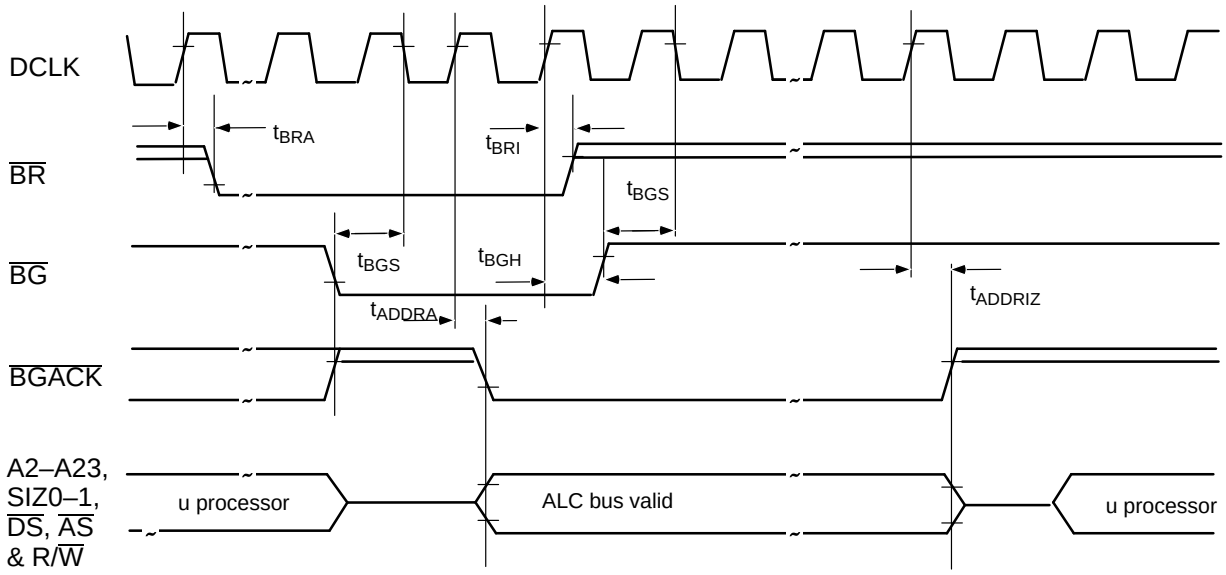


Fig. 71 – Microprocessor Interface – Motorola DMA Access Timing

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
$\overline{BR}$ Active Delay	$\overline{BR}$	t_{BRA}	9		14	ns
$\overline{BR}$ Inactive delay	$\overline{BR}$	t_{BRI}	26		47	ns
Setup Time of $\overline{BG}$, $\overline{AS}$ & $\overline{BGACK}$ Active	$\overline{BG}$	t_{BGS}	0			ns
Hold Time of $\overline{BG}$, $\overline{AS}$ & $\overline{BGACK}$ Invalid	$\overline{BG}$	t_{BGH}	2			ns
ALC Bus Active Delay	A2–A23, SIZ0–1, $\overline{DS}$, $\overline{AS}$, R/$\overline{W}$	t_{ADDRAZ}	10		30	ns
ALC Bus Inactive Delay	A2–A23, SIZ0–1, $\overline{DS}$, $\overline{AS}$, R/$\overline{W}$	t_{ADDRIZ}	25		72	ns

Table 11 – Microprocessor Interface – Motorola DMA Access AC Timing

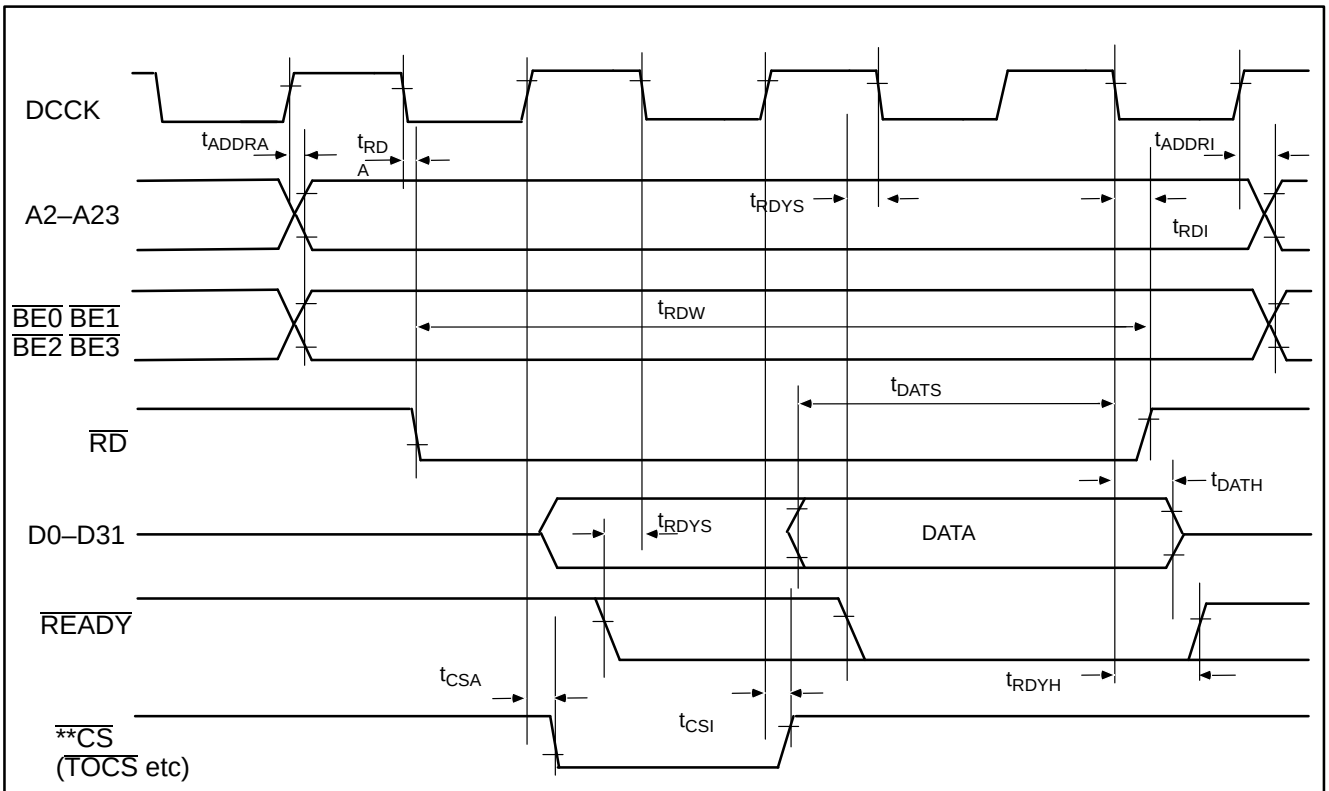


Fig. 72 – DPR / DMA Interface – Intel Read Cycle

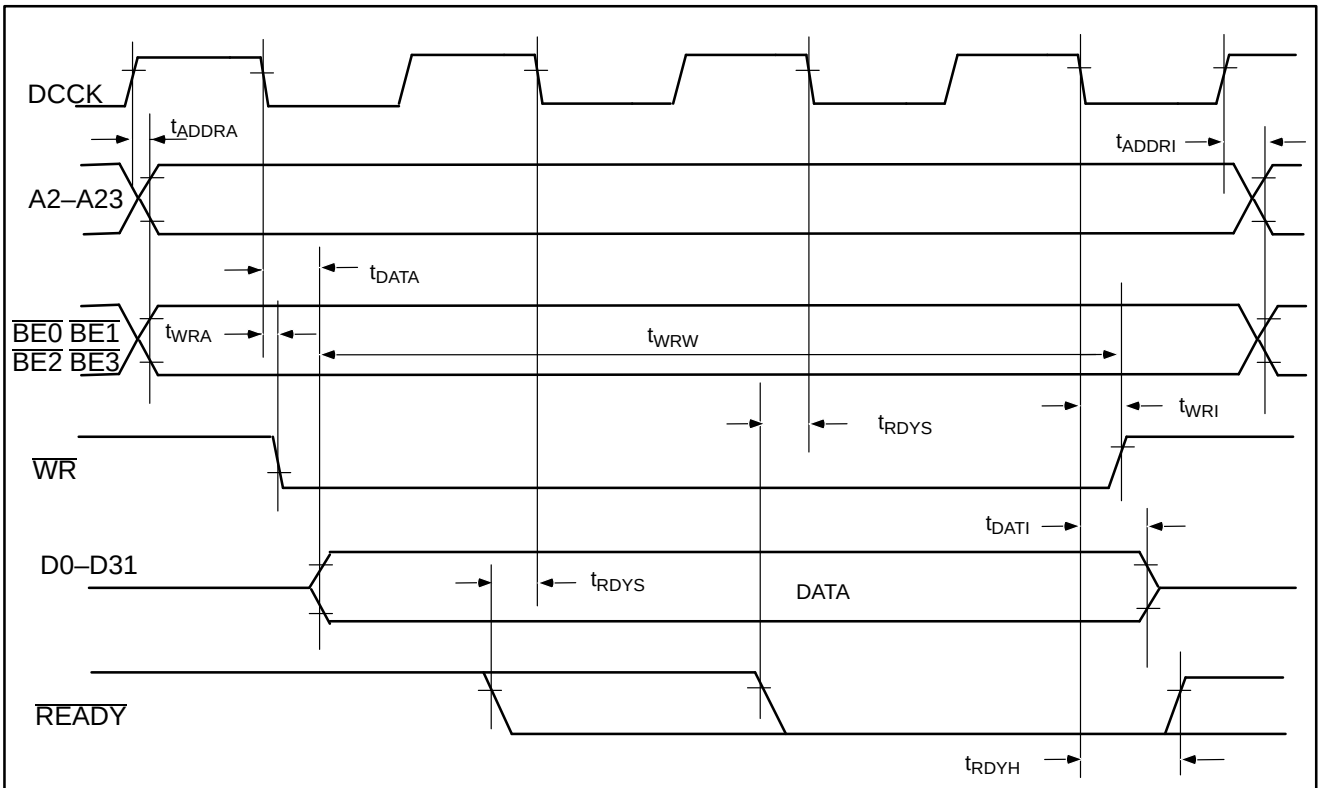


Fig. 73 – DPR / DMA Interface – Intel Write Cycle

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
Address Active Delay	A2–A23	t_{ADDRA}	17		25	ns
BE Active Delay	BE0–BE3	t_{ADDRA}	23		30	ns
Address BE Inactive Delay	A2–A23	t_{ADDRI}	10			ns
Read Active Delay	$\overline{RD}$	t_{RDA}	11		15	ns
Read Inactive Delay	$\overline{RD}$	t_{RDI}	10		15	ns
Setup Time of Ready	$\overline{READY}$	t_{RDYS}	0			ns
Hold Time of Ready	$\overline{READY}$	t_{RDYH}	2			ns
Read Active Width	$\overline{RD}$	t_{RDW}	$t_{DCLK - 1ns}$			ns
Setup Time of Data	D0–D15	t_{DATS}	5			ns
Hold Time of Data	D0–D15	t_{DATH}	8			ns
Write Active Delay	$\overline{WR}$	t_{WRA}	11		15	ns
Write Inactive Delay	$\overline{WR}$	t_{WRI}	10		15	ns
Write Active Width	$\overline{WR}$	t_{WRW}	$t_{DCLK - 1ns}$			ns
Write Data Active Delay	D0–D31	t_{DATA}	18		27	ns
Write Data Inactive delay	D0–D31	t_{DATI}	10			ns
Cycle Start Active delay	**CS	t_{CSA}	12		18	ns
Cycle State Inactive delay	**CS	t_{CSI}	11		16	ns

Table 12 – DPR / DMA Interface – Intel Cycle AC Timing

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
Address Active delay	A2–A23	t_{ADDRA}	17		25	ns
SIZ0/1 Active Delay	SIZ0/1	t_{ADDRA}	23		30	ns
Address SIZ0/1 Inactive Delay	A2–A23	t_{ADDRI}	10			ns
Read $\overline{AS}$ $\overline{DS}$ Active Delay	$\overline{DS}$	t_{ASDSA}	11		16	ns
Read $\overline{AS}$ $\overline{DS}$ Inactive Delay	$\overline{DS}$	t_{ASDSI}	10		15	ns
Setup Time of $\overline{DTACK}$	$\overline{DTACK}$	t_{DTKS}	0			ns
Hold Time of $\overline{DTACK}$	$\overline{DTACK}$	t_{DTKH}	2			ns
Read $\overline{DS}$ Active Width	$\overline{DS}$	t_{DSW}	$t_{DCLK - 1ns}$			ns
Setup Time of Data	D0–D31	t_{DATS}	5			ns
Hold Time of Data	D1–D31	t_{DATH}	8			ns
Write $\overline{AS}$ Active Delay	$\overline{AS}$	t_{ASA}	12		16	ns
Write $\overline{DS}$ Active Delay	$\overline{DS}$	t_{DSA}	11		16	ns
Write $\overline{AS}$ DS Inactive Delay	$\overline{DS}$	t_{ASDSI}	10		15	ns
Write $\overline{AS}$ Active Width	$\overline{AS}$	t_{ASW}	$t_{DCLK - 1ns}$			ns
Write $\overline{DS}$ Active Width	$\overline{DS}$	t_{DSW}	$^1/_2\ t_{DCLK - 1ns}$			ns
Write Data Active Delay	D0–D31	t_{DATA}	14		27	ns
Write Data Inactive Delay	D0–D31	t_{DATI}	10			ns

Table 13 – DPR / DMA Interface – Motorola Cycle AC Timing

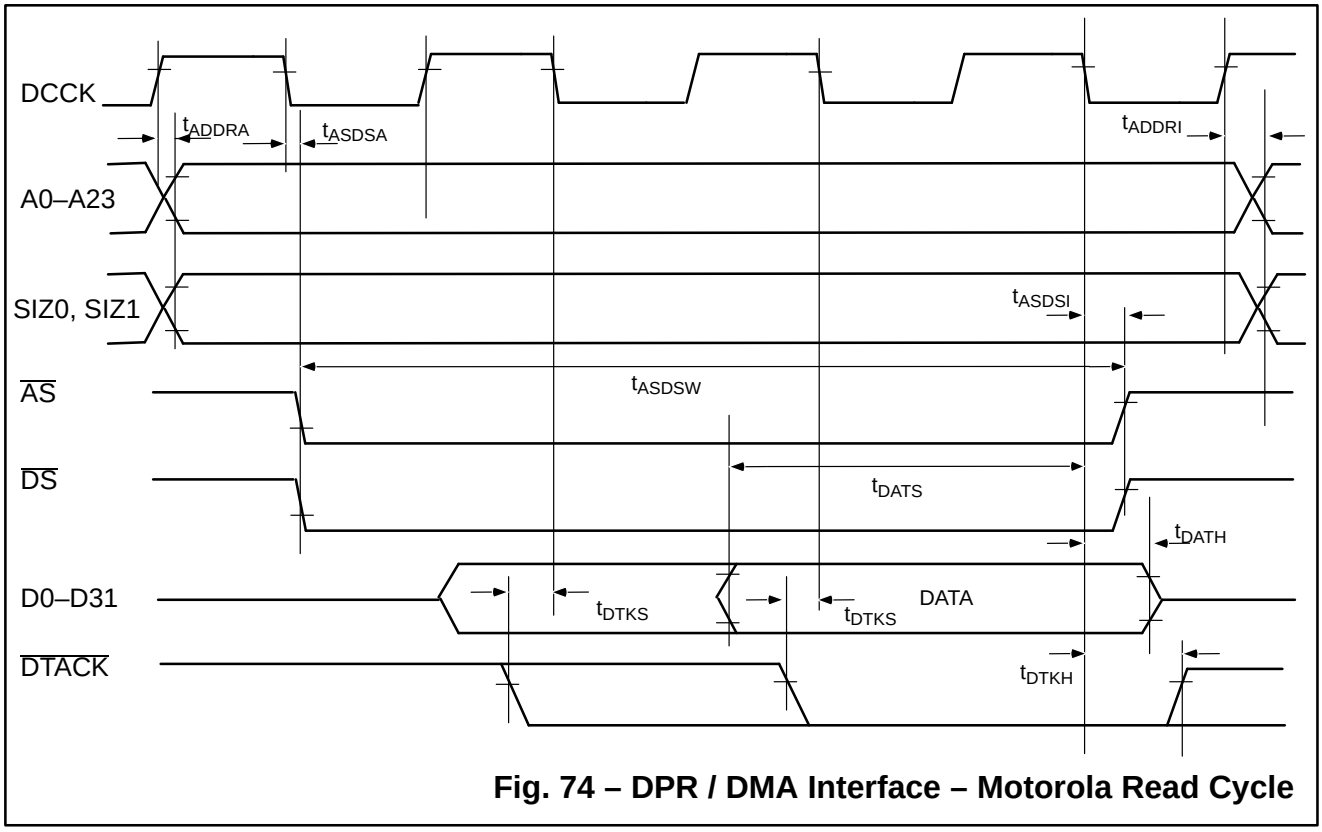


Fig. 74 – DPR / DMA Interface – Motorola Read Cycle

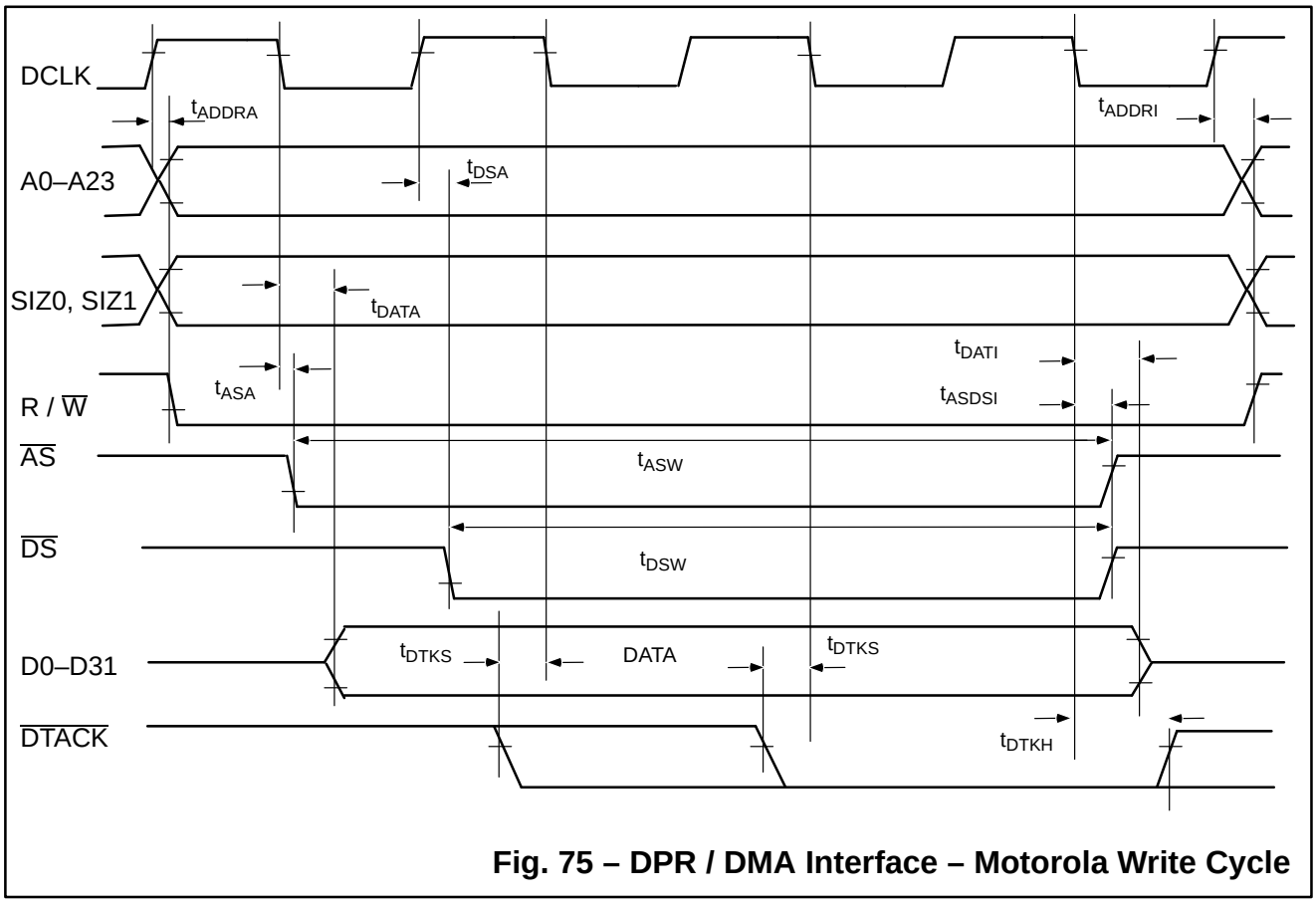


Fig. 75 – DPR / DMA Interface – Motorola Write Cycle

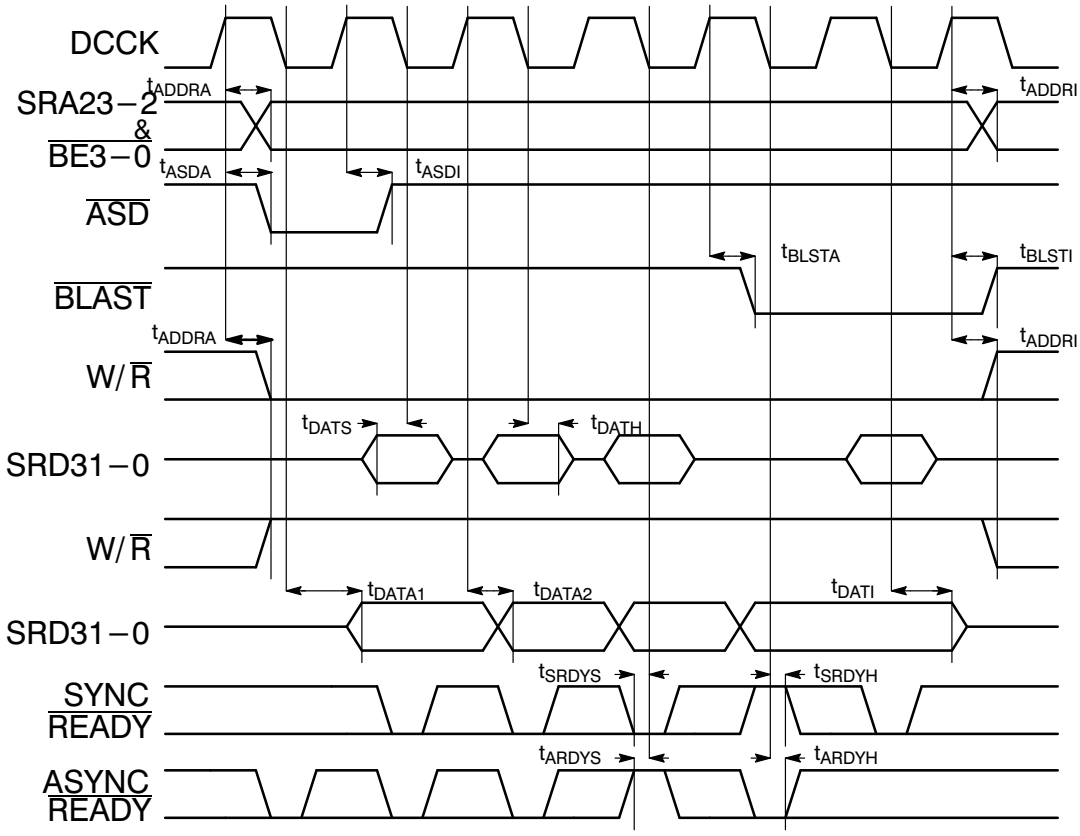


Fig. 76 – Single Cycle Burst – Intel Extended Cycle (SBL="1")

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
Address Active Delay	A23–2	t_{ADDRA}	17		25	ns
Write/Read Active Delay	W/$\overline{R}$	t_{ADDRA}	17		24	ns
BE Active Delay	$\overline{BE3–0}$	t_{ADDRA}	23		30	ns
Address BE Write/Read Inactive Delay	A23–2, $\overline{BE3–0}$, W/$\overline{R}$	t_{ADDRI}	10			ns
ASD Active Delay	$\overline{ASD}$	t_{ASDA}	16		22	ns
ASD Inactive Delay	$\overline{ASD}$	t_{ASDI}	11		15	ns
$\overline{BLAST}$ Active Delay	$\overline{BLAST}$	t_{BLSTA}	11		15	ns
$\overline{BLAST}$ Inactive Delay	$\overline{BLAST}$	t_{BLSTI}	10		14	ns
Setup Time of Data	SRD31–0	t_{DATS}	0			ns
Hold Time of Data	SRD31–0	t_{DATH}	6			ns
Write Active Delay1	SRD31–0	t_{DATA1}	14		27	ns
Write Active Delay2	SRD31–0	t_{DATA2}	20		30	ns
Write Inactive Delay	SRD31–0	t_{DATI}	10			ns
Setup Time of SYNC READY	$\overline{READY}$	t_{SRDYS}	0			ns
Hold Time of SYNC READY	$\overline{READY}$	t_{SRDYH}	2			ns
Setup Time of ASYNC READY	$\overline{READY}$	t_{ARDYS}	0			ns
Hold Time of ASYNC READY	$\overline{READY}$	t_{ARDYH}	2			ns

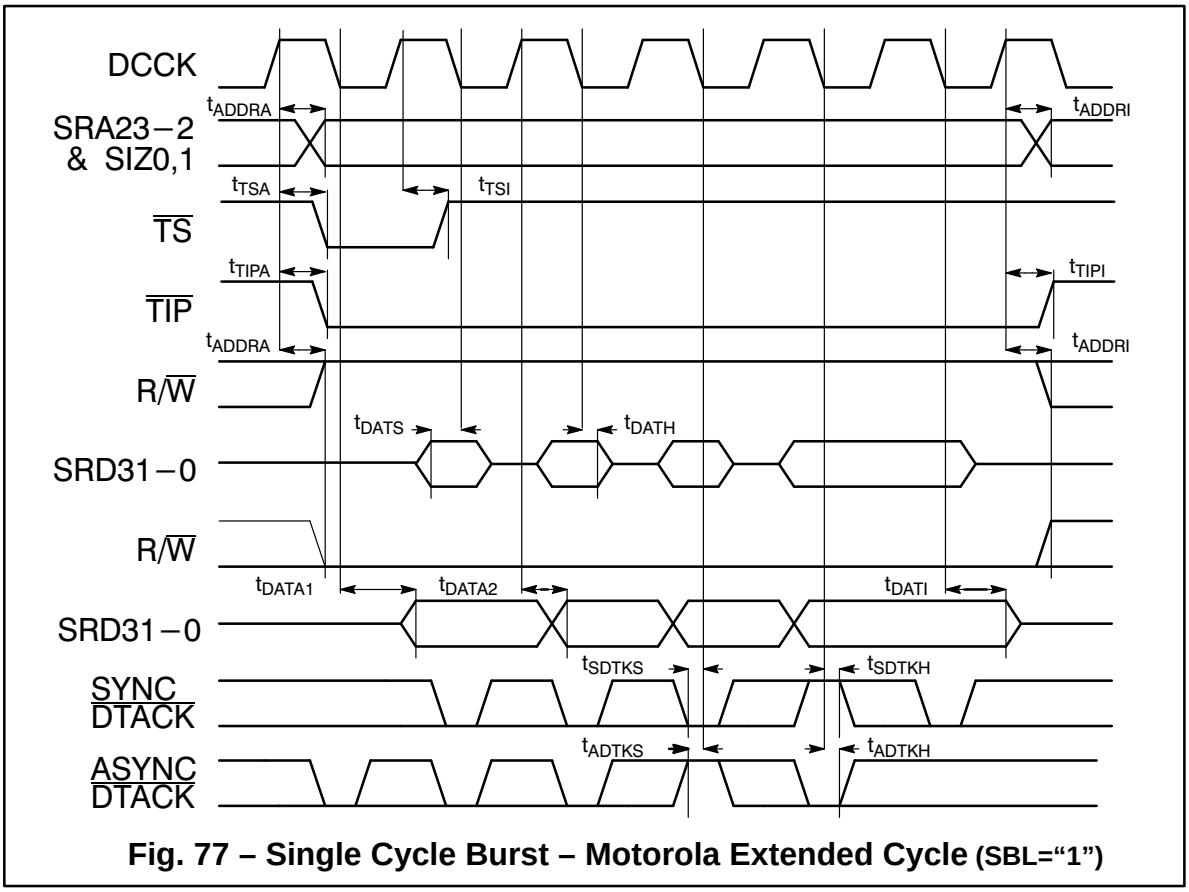


Fig. 77 – Single Cycle Burst – Motorola Extended Cycle (SBL="1")

Parameter	Signal	Abbrev	Values			Units (ns)
			Min	Typical	Max	
Address Active Delay	A23–2	t_{ADDRA}	17		25	ns
R/$\overline{W}$ Active Delay	R/$\overline{W}$	t_{ADDRA}	15		23	ns
SIZ0, SIZ1 Active Delay	SIZ0, SIZ1	t_{ADDRA}	23		30	ns
Address BE Write/Read Inactive Delay	A23–2, SIZ0, SIZ1, W/$\overline{R}$	t_{ADDRI}	10			ns
$\overline{TS}$ Active Delay	$\overline{TS}$	t_{TSA}	17		22	ns
$\overline{TS}$ Inactive Delay	$\overline{TS}$	t_{TSI}	11		15	ns
$\overline{TIP}$ Active Delay	$\overline{TIP}$	t_{TIPA}	17		23	ns
$\overline{TIP}$ Inactive Delay	$\overline{TIP}$	t_{TIPI}	15		21	ns
Setup Time of Data	SRD31–0	t_{DATS}	0			ns
Hold Time of Data	SRD31–0	t_{DATH}	6			ns
Write Active Delay1	SRD31–0	t_{DATA1}	14		27	ns
Write Active Delay2	SRD31–0	t_{DATA2}	20		30	ns
Write Inactive Delay	SRD31–0	t_{DATI}	10			ns
Setup Time of SYNC $\overline{DTACK}$	$\overline{DTACK}$	t_{SDTKS}	0			ns
Hold Time of SYNC $\overline{DTACK}$	$\overline{DTACK}$	t_{SDTKH}	2			ns
Setup Time of ASYNC $\overline{DTACK}$	$\overline{DTACK}$	t_{ADTKS}	0			ns
Hold Time of ASYNC $\overline{DTACK}$	$\overline{DTACK}$	t_{ADTKH}	2			ns

E. JTAG

E.1 JTAG Cells

The Boundary Scan Register (BSR) consists of 123 registers, which form a serial shift register starting from pin 83, moving in a generally anti–clockwise direction around the chip to finish at pin 24.

It should be noted that none of the internal D–types which form the BSR are reset, and hence are initially undefined. A valid pattern needs to be shifted into the register prior to any testing. However, while the JTAG TAP controller is reset, the I/O pins are connected through to the system logic.

I / O Pin Type: I = Input
C = Clock input
O = Output
B = Bidirectional
T = Tristate
Iu = Input with pull-up resistor.

BSR Cell Type: BSI 1 allows capture of device input pin and control of logic input pin.
BSI 3 allows capture of device input pin only.
BSO allows capture of logic output pin and control of device output pin (= BSI1).
BSOE allows control of tristate-able output pin (preset–able).
BSDI allows control of bidirectional pin (= BSOE).
BSBI allows capture and control of bidirectional input and output pin (= BSI 1 + BSO).

Control Group No.: Denotes a JTAG BSR cell which controls a (group of) tristate-able output(s) or bidirectional pin(s).

Controlled Group No.: Denotes a JTAG BSR cell which connects to a tristate-able output or bidirectional pin which is controlled by the JTAG BSR cell numbered in the previous column.

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
1	BSI1			Iu	83	TXDRV
2	BSOE	1				
3	BSO		1	T	88	$\overline{\text{DS/BLAST/TIP}}$
4	BSDI	2				
5 & 6	BSBI		2	B	93	$\overline{\text{MRD}}$ / $\overline{\text{AS/ ASD}}$
7	BSO		1	T	94	$\overline{\text{MWR}}$ / R/$\overline{\text{W}}$ $\overline{\text{R}}$/W
8	BSOE	3				
9	BSO		3	T	95	HOLD / $\overline{\text{BR}}$
10	BSI1			I	98	HLDA / $\overline{\text{BG}}$
11	BSDI	4				
12 & 13	BSBI		4	B	99	BGACK
14	BSI1			I	100	$\overline{\text{DTACK}}$ / $\overline{\text{READY}}$
15	BSI1			I	101	RESET
16	BSI1			I	102	$\overline{\text{CS}}$
17	BSOE	5				
18	BSO		5	T	103	$\overline{\text{IRQ}}$
19	BSI1			I	104	$\overline{\text{RD}}$
20	BSI1			I	105	$\overline{\text{WR}}$
21	BSI1			I	106	A1
22	BSI1			I	108	A2
23	BSI1			I	109	A3
24	BSI1			I	110	A4
25	BSI1			I	111	A5
26	BSI1			I	112	A6
27	BSI1			I	113	TEST
28	BSDI	6				
29 & 30	BSBI		6	B	115	DATA0
31 & 32	BSBI		6	B	116	DATA1
33 & 34	BSBI		6	B	117	DATA2
35 & 36	BSBI		6	B	118	DATA3
37 & 38	BSBI		6	B	121	DATA4
39 & 40	BSBI		6	B	122	DATA5
41 & 42	BSBI		6	B	123	DATA6
43 & 44	BSBI		6	B	125	DATA7
45 & 46	BSBI		6	B	126	DATA8
47 & 48	BSBI		6	B	127	DATA9
49 & 50	BSBI		6	B	128	DATA10
51 & 52	BSBI		6	B	133	DATA11
53 & 54	BSBI		6	B	134	DATA12
55 & 56	BSBI		6	B	135	DATA13
57 & 58	BSBI		6	B	136	DATA14
59 & 60	BSBI		6	B	138	DATA15
61	BSI3			C	139	DCCK
62	BSO			O	140	TOUT
63	BSI1			I	155	TIN
64	BSOE	7				
65	BSDI	8				
66	BSO		7	T	143	TXSOC
67	BSI3			C	144	TXCLK
68	BSO		7	T	145	TXD0
69	BSO		7	T	146	TXD1
70	BSO		7	T	148	TXD2
71	BSO		7	T	149	TXD3

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
72	BSO		7	T	150	TXD4
73	BSO		7	T	151	TXD5
74	BSO		7	T	152	TXD6
75	BSO		7	T	153	TXD7
76	BSO			O	156	$\overline{\text{RXEN}}$
77	BSI1			I	157	RXSOC
78	BSI3			C	158	RXCLK
79	BSI1			I	159	RXD0
80	BSI1			I	160	RXD1
81	BSI1			I	161	RXD2
82	BSI1			I	162	RXD3
83	BSI1			I	163	RXD4
84	BSI1			I	166	RXD5
85	BSI1			I	168	RXD6
86	BSI1			I	169	RXD7
87	BSI1			Iu	167	$\overline{\text{TXFULL}}$
88	BSO		7	T	55	$\overline{\text{TXEN}}$
89	BSI1			Iu	56	$\overline{\text{RXEMPTY}}$
90	BSI1			Iu	57	CS / $\overline{\text{UT}}$
91	BSO		1	T	89	$\overline{\text{BE0}}$ / SRA0
92	BSO		1	T	90	BE1 / SRA1
93	BSO		1	T	91	BE2 / SIZ0
94	BSO		1	T	92	$\overline{\text{BE3}}$ / SIZ1
95	BSO		1	T	87	SRA2
96	BSO		1	T	197	SRA3
97	BSO		1	T	199	SRA4
98	BSO		1	T	202	SRA5
99	BSO		1	T	203	SRA6
100	BSO		1	T	204	SRA7
101	BSO		1	T	8	SRA8
102	BSO		1	T	9	SRA9
103	BSO		1	T	11	SRA10
104	BSO		1	T	12	SRA11
105	BSO		1	T	13	SRA12
106	BSO		1	T	37	SRA13
107	BSO		1	T	39	SRA14
108	BSO		1	T	40	SRA15
109	BSO		1	T	41	SRA16
110	BSO		1	T	59	SRA17
111	BSO		1	T	62	SRA18
112	BSO		1	T	63	SRA19
113	BSO		1	T	64	SRA20
114	BSO		1	T	66	SRA21
115	BSO		1	T	67	SRA22
116	BSO		1	T	68	SRA23
117	BSO			O	44	$\overline{\text{TOCS}}$
118	BSO			O	45	$\overline{\text{TDCS}}$
119	BSO			O	46	$\overline{\text{ROCS}}$
120	BSO			O	47	$\overline{\text{RDCS}}$
121 & 122	BSBI		8	B	29	PRTY0
123 & 124	BSBI		8	B	31	PRTY1
125 & 126	BSBI		8	B	32	PRTY2
127 & 128	BSBI		8	B	33	PRTY3

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
129	BSI1			Iu	35	$\overline{\text{SADRV}}$
130 & 131	BSBI		8	B	170	SRD0
132 & 133	BSBI		8	B	172	SRD1
134 & 135	BSBI		8	B	173	SRD2
136 &137	BSBI		8	B	175	SRD3
138 & 139	BSBI		8	B	178	SRD4
140 & 141	BSBI		8	B	179	SRD5
142 & 143	BSBI		8	B	181	SRD6
144 & 145	BSBI		8	B	185	SRD7
146 & 147	BSBI		8	B	187	SRD8
148 & 149	BSBI		8	B	190	SRD9
150 & 151	BSBI		8	B	192	SRD10
152 & 153	BSBI		8	B	193	SRD11
154 & 155	BSBI		8	B	195	SRD12
156 & 157	BSBI		8	B	196	SRD13
158 & 159	BSBI		8	B	205	SRD14
160 & 161	BSBI		8	B	206	SRD15
162 & 163	BSBI		8	B	207	SRD16
164 & 165	BSBI		8	B	208	SRD17
166 & 167	BSBI		8	B	1	SRD18
168 & 169	BSBI		8	B	2	SRD19
170 & 171	BSBI		8	B	4	SRD20
172 & 173	BSBI		8	B	5	SRD21
174 & 175	BSBI		8	B	6	SRD22
176 & 177	BSBI		8	B	7	SRD23
178 & 179	BSBI		8	B	14	SRD24
180 & 181	BSBI		8	B	16	SRD25
182 & 183	BSBI		8	B	17	SRD26
184 & 185	BSBI		8	B	18	SRD27
186 & 187	BSBI		8	B	20	SRD28
188 & 189	BSBI		8	B	21	SRD29
190 & 191	BSBI		8	B	22	SRD30
192 & 193	BSBI		8	B	24	SRD31
				C	73	TCK
				I	75	TMS
				I	77	TDI
				T	81	TDO

F. PIN DESCRIPTION

F.1 Physical Pin Diagram

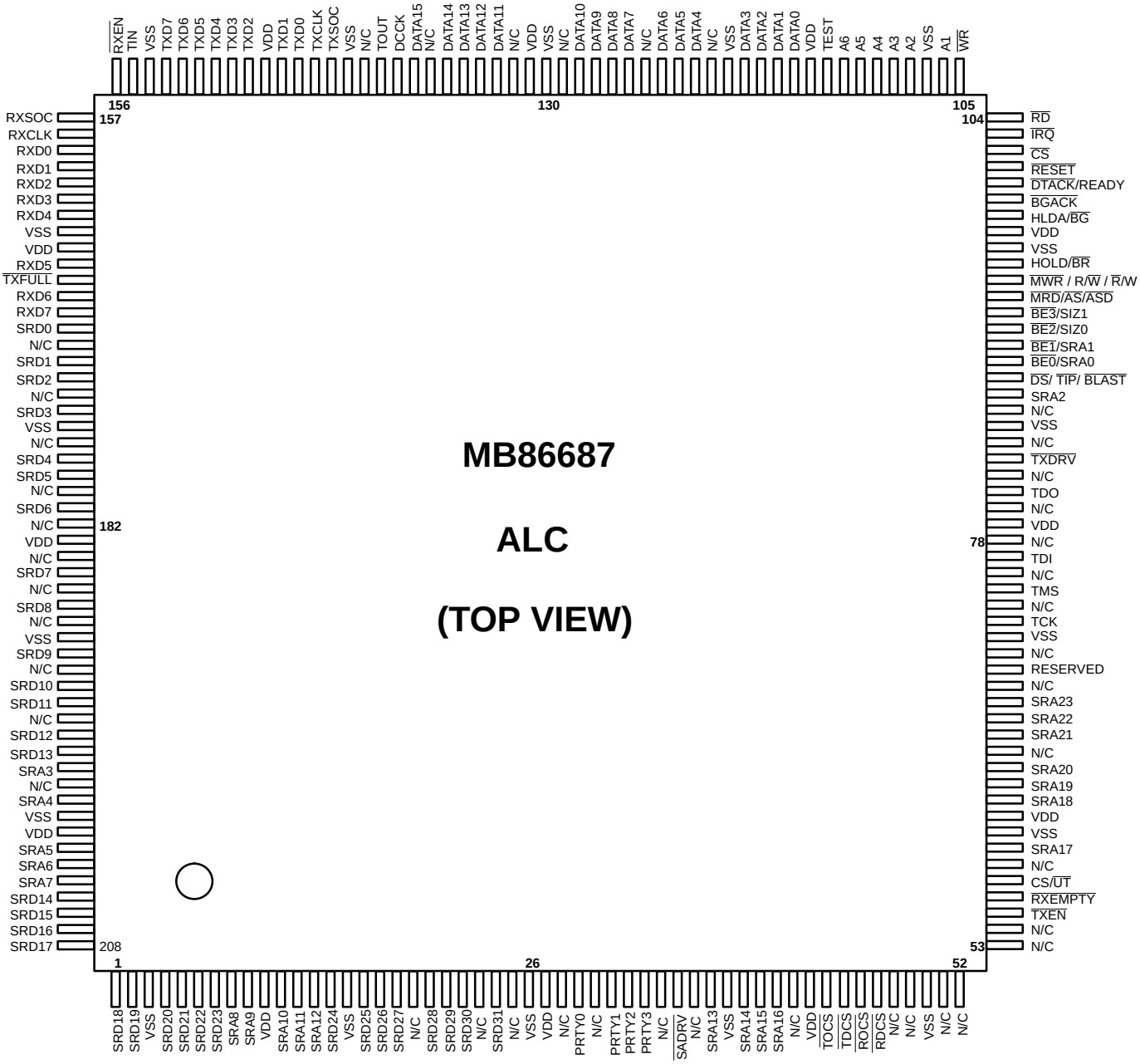


Fig. 78 – ALC Pin Assignment

F.2 Pin Description Table

Pin No.	Pin Name	Type	Function
1	SRD18	I/O	SAR Memory data bus bit 18
2	SRD19	I/O	SAR Memory data bus bit 19
3	VSS	–	
4	SRD20	I/O	SAR Memory data bus bit 20
5	SRD21	I/O	SAR Memory data bus bit 21
6	SRD22	I/O	SAR Memory data bus bit 22
7	SRD23	I/O	SAR Memory data bus bit 23
8	SRA8	O (3-state)	SAR Memory address bit 8
9	SRA9	O (3-state)	SAR Memory address bit 9
10	VDD	–	
11	SRA10	O (3-state)	SAR Memory address bit 10
12	SRA11	O (3-state)	SAR Memory address bit 11
13	SRA12	O (3-state)	SAR Memory address bit 12
14	SRD24	I/O	SAR Memory data bus bit 24
15	VSS	–	
16	SRD25	I/O	SAR Memory data bus bit 25
17	SRD26	I/O	SAR Memory data bus bit 26
18	SRD27	I/O	SAR Memory data bus bit 27
19	N/C	–	Not Connected
20	SRD28	I/O	SAR Memory data bus bit 28
21	SRD29	I/O	SAR Memory data bus bit 29
22	SRD30	I/O	SAR Memory data bus bit 30
23	N/C	–	Not Connected
24	SRD31	I/O	SAR Memory data bus bit 31
25	N/C	–	Not Connected
26	VSS	–	
27	VDD	–	
28	N/C	–	Not Connected
29	PRTY0	I/O	Parity for SRD7 – SRD0
30	N/C	–	Not Connected
31	PRTY1	I/O	Parity for SRD15 – SRD8
32	PRTY2	I/O	Parity for SRD23 – SRD16
33	PRTY3	I/O	Parity for SRD31 – SRD24
34	N/C	–	Not Connected
35	$\overline{\text{SADRV}}$	I	SAR Memory constant drive
36	N/C	–	Not Connected
37	SRA13	O (3-state)	SAR Memory address bit 13
38	VSS	–	
39	SRA14	O (3-state)	SAR Memory address bit 14
40	SRA15	O (3-state)	SAR Memory address bit 15
41	SRA16	O (3-state)	SAR Memory address bit 16
42	N/C	–	Not Connected
43	VDD	–	
44	$\overline{\text{TOCS}}$	O	Transmit Overhead Start of Cycle
45	$\overline{\text{TDCS}}$	O	Transmit Data Start of Cycle
46	$\overline{\text{ROCS}}$	O	Receive Overhead Start of Cycle
47	$\overline{\text{RDCS}}$	O	Receive Data Start of Cycle
48	N/C	–	Not Connected
49	N/C	–	Not Connected
50	VSS	–	
51	N/C	–	Not Connected
52	N/C	–	Not Connected
53	N/C	–	Not Connected

Pin No.	Pin Name	Type	Function
54	N/C	–	Not Connected
55	$\overline{\text{TXEN}}$	O (high–Z)	UTOPIA Transmit Enable
56	$\overline{\text{RXEMPTY}}$	I	UTOPIA Receive Empty
57	CS/$\overline{\text{UT}}$	I	Fujitsu Cell Stream / UTOPIA Select
58	N/C	–	Not Connected
59	SRA17	O (3-state)	SAR Memory address bit 53
60	VSS	–	
61	VDD	–	
62	SRA18	O (3-state)	SAR Memory address bit 18
63	SRA19	O (3-state)	SAR Memory address bit 19
64	SRA20	O (3-state)	SAR Memory address bit 20
65	N/C	–	Not Connected
66	SRA21	O (3-state)	SAR Memory address bit 21
67	SRA22	O (3-state)	SAR Memory address bit 22
68	SRA23	O (3-state)	SAR Memory address bit 23
69	N/C	–	Not Connected
70	N/C	–	Reserved
71	N/C	–	Not Connected
72	VSS	–	
73	TCK	I	JTAG Port Clock
74	N/C	–	Not Connected
75	TMS	I	JTAG Test Mode Select
76	N/C	–	Not Connected
77	TDI	I	JTAG Data Input
78	N/C	–	Not Connected
79	VDD	–	
80	N/C	–	Not Connected
81	TDO	O	JTAG Data Output
82	N/C	–	Not Connected
83	$\overline{\text{TXDRV}}$	I	Cell Stream Constant Drive
84	N/C	–	Not Connected
85	VSS	–	
86	N/C	–	Not Connected
87	SRA2	O (high–Z)	SAR Memory data bus bit 62
88	$\overline{\text{DS}}$ / $\overline{\text{BLAST}}$ / $\overline{\text{TIP}}$	O (3–state)	Data Strobe / Burst Last / Transfer in Progress
89	$\overline{\text{BE0}}$	O (3-state)	SAR Memory $\overline{\text{BE0}}$/SRA0
90	$\overline{\text{BE1}}$	O (3-state)	SAR Memory $\overline{\text{BE1}}$/SRA1
91	$\overline{\text{BE2}}$	O (3-state)	SAR Memory $\overline{\text{BE2}}$/SIZ0
92	$\overline{\text{BE3}}$	O (3-state)	SAR Memory $\overline{\text{BE3}}$/SIZ1
93	$\overline{\text{MRD}}$/$\overline{\text{AS}}$/ $\overline{\text{ASD}}$	I/O	SAR Memory $\overline{\text{MRD}}$/$\overline{\text{AS}}$/$\overline{\text{ASD}}$
94	$\overline{\text{MWR}}$/ R/$\overline{\text{W}}$/ $\overline{\text{R}}$/W	O (3-state)	SAR Memory $\overline{\text{MWR}}$/R/$\overline{\text{W}}$ / $\overline{\text{R}}$/W
95	HOLD/$\overline{\text{BR}}$	O (high-Z)	SAR Memory HOLD/$\overline{\text{BR}}$
96	VSS	–	
97	VDD	–	
98	HLDA/$\overline{\text{BG}}$	I	SAR Memory HLDA/$\overline{\text{BG}}$
99	BGACK	O (high-Z)	SAR Memory $\overline{\text{BGACK}}$
100	READY	I	SAR Memory READY
101	RESET	I	ALC Master Reset input
102	CS	I	μp Chip Select
103	IRQ	O (high-Z)	Interrupt Request
104	RD	I	μp Read
105	WR	I	μp Write
106	A1	I	Microprocessor Address bit 1
107	VSS	–	
108	A2	I	Microprocessor Address bit 2

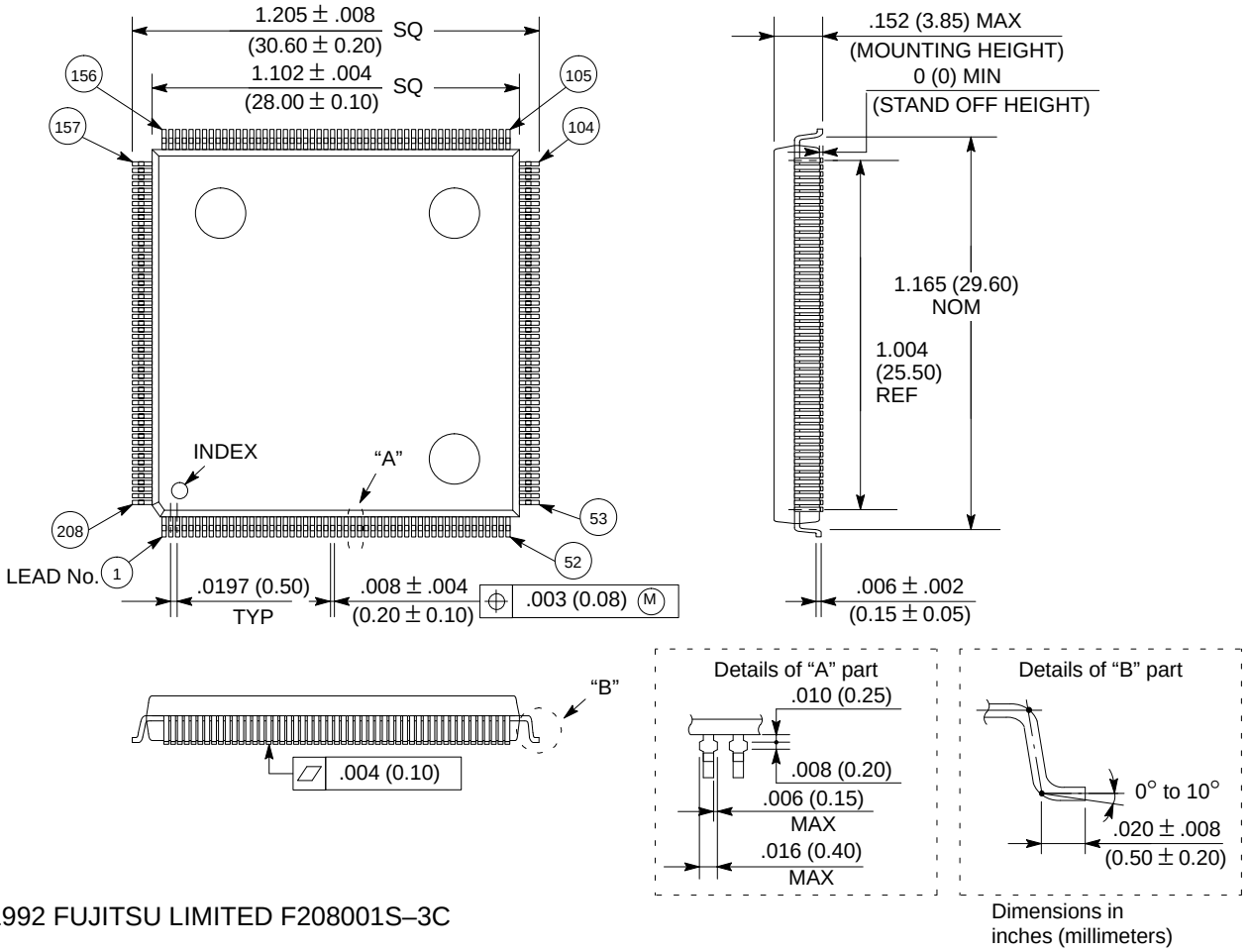
Pin No.	Pin Name	Type	Function
109	A3	I	Microprocessor Address bit 3
110	A4	I	Microprocessor Address bit 4
111	A5	I	Microprocessor Address bit 5
112	A6	I	Microprocessor Address bit 6
113	TEST	I	
114	VDD	–	
115	DATA0	I/O	Microprocessor Data Bus bit 0
116	DATA1	I/O	Microprocessor Data Bus bit 1
117	DATA2	I/O	Microprocessor Data Bus bit 2
118	DATA3	I/O	Microprocessor Data Bus bit 3
119	VSS	–	
120	N/C	–	Not Connected
121	DATA4	I/O	Microprocessor Data Bus bit 4
122	DATA5	I/O	Microprocessor Data Bus bit 5
123	DATA6	I/O	Microprocessor Data Bus bit 6
124	N/C	–	Not Connected
125	DATA7	I/O	Microprocessor Data Bus bit 7
126	DATA8	I/O	Microprocessor Data Bus bit 8
127	DATA9	I/O	Microprocessor Data Bus bit 9
128	DATA10	I/O	Microprocessor Data Bus bit 10
129	N/C	–	Not Connected
130	VSS	–	
131	VDD	–	
132	N/C	–	Not Connected
133	DATA11	I/O	Microprocessor Data Bus bit 11
134	DATA12	I/O	Microprocessor Data Bus bit 12
135	DATA13	I/O	Microprocessor Data Bus bit 13
136	DATA14	I/O	Microprocessor Data Bus bit 14
137	N/C	–	Not Connected
138	DATA15	I/O	Microprocessor Data Bus bit 15
139	DCCK	I	DMA Cycle Clock input
140	TOUT	O	Token Out output
141	N/C	–	Not Connected
142	VSS	–	
143	TXSOC	O (3-state)	Cell Stream Interface Transmit Sync
144	TXCLK	I	Cell Stream Interface Transmit
145	TXD0	O (3-state)	Cell Stream Interface Transmit data bit 0
146	TXD1	O (3-state)	Cell Stream Interface Transmit data bit 1
147	VDD	–	
148	TXD2	O (3-state)	Cell Stream Interface Transmit data bit 2
149	TXD3	O (3-state)	Cell Stream Interface Transmit data bit 3
150	TXD4	O (3-state)	Cell Stream Interface Transmit data bit 4
151	TXD5	O (3-state)	Cell Stream Interface Transmit data bit 5
152	TXD6	O (3-state)	Cell Stream Interface Transmit data bit 6
153	TXD7	O (3-state)	Cell Stream Interface Transmit data bit 7
154	VSS	–	
155	TIN	–	Token In input
156	RXEN	O	Indicates ALC receive buffers full
157	RXSOC	I	Cell Stream Interface Receive Sync
158	RXCLK	I	Cell Stream Interface Receive
159	RXD0	I	Cell Stream Interface Receive data bit 0
160	RXD1	I	Cell Stream Interface Receive data bit 1
161	RXD2	I	Cell Stream Interface Receive data bit 2
162	RXD3	I	Cell Stream Interface Receive data bit 3
163	RXD4	I	Cell Stream Interface Receive data bit 4

Pin No.	Pin Name	Type	Function
164	VSS	–	
165	VDD	–	
166	RXD5	I	Cell Stream Interface Receive data bit 5
167	$\overline{\text{TXFULL}}$	I	UTOPIA Transmit Full
168	RXD6	I	Cell Stream Interface Receive data bit 6
169	RXD7	I	Cell Stream Interface Receive data bit 7
170	SRD0	I/O	SAR Memory data bus bit 0
171	N/C	–	Not Connected
172	SRD1	I/O	SAR Memory data bus bit 1
173	SRD2	I/O	SAR Memory data bus bit 2
174	N/C	–	Not Connected
175	SRD3	I/O	SAR Memory data bus bit 3
176	VSS	–	
177	N/C	–	Not Connected
178	SRD4	I/O	SAR Memory data bus bit 4
179	SRD5	I/O	SAR Memory data bus bit 5
180	N/C	–	Not Connected
181	SRD6	I/O	SAR Memory data bus bit 6
182	N/C	–	Not Connected
183	VDD	–	
184	N/C	–	Not Connected
185	SRD7	I/O	SAR Memory data bus bit 7
186	N/C	–	Not Connected
187	SRD8	I/O	SAR Memory data bus bit 8
188	N/C	–	Not Connected
189	VSS	–	
190	SRD9	I/O	SAR Memory data bus bit 9
191	N/C	–	Not Connected
192	SRD10	I/O	SAR Memory data bus bit 10
193	SRD11	I/O	SAR Memory data bus bit 11
194	N/C	–	Not Connected
195	SRD12	I/O	SAR Memory data bus bit 12
196	SRD13	I/O	SAR Memory data bus bit 13
197	SRA3	O (3-state)	SAR Memory address bit 3
198	N/C	–	Not Connected
199	SRA4	O (3-state)	SAR Memory address bit 4
200	VSS	–	
201	VDD	–	
202	SRA5	O (3-state)	SAR Memory address bit 5
203	SRA6	O (3-state)	SAR Memory address bit 6
204	SRA7	O (3-state)	SAR Memory address bit 7
205	SRD14	I/O	SAR Memory data bus bit 14
206	SRD15	I/O	SAR Memory data bus bit 15
207	SRD16	I/O	SAR Memory data bus bit 16
208	SRD17	I/O	SAR Memory data bus bit 17

G. PACKAGE DIMENSIONS

FPT-208P-M01

208-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-208P-M01)



Dimensions in
inches (millimeters)

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