September 1988
Edition 1.0

FUJITSU

DATA SHEET

MB87020
16-BIT A/D AND D/A CONVERTER

16-BIT A/D AND D/A CONVERTER

The Fujitsu MB87020 is a 50kSPS (Kilo Sample Per Second) 16-bit Analog-to-Digital and Digital-to-Analog converter fabricated by Fujitsu Advanced CMOS technology. A/D or D/A function is selected by MODE input.

The MB87020 is synchronous/asynchronous 8-/16-bit oriented data interface in order to transfer data between any processor directly and easily, and serial data can also be managed.

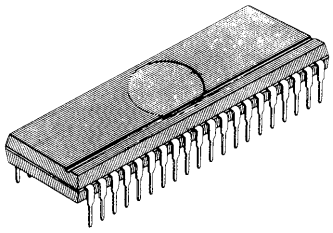
FEATURES

- Conversion Mode Selectable: A to D or D to A
- High Resolution: 16-bit
- High Conversion Speed: 50kSPS max.
- High Linearity: 12-bit
- Low Power Dissipation and Stand-by Mode Available
- Microprocessor oriented 8-/16-bit bus compatibility including interrupt request as conversion completion
- Serial Data Port Available
- On-chip Sample and Hold circuit for Analog Input/Output
- On-chip Reference Voltage Generator: 2.5V typ.
- External Reference Voltage can be used
- Power Supply Voltage: ±5V
- Package: 40-pin Plastic Dual In-Line Package

ABSOLUTE MAXIMUM RATINGS (see NOTE)

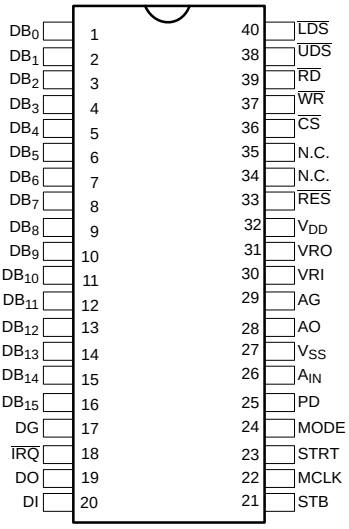
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	–0.3 to +7.0	V
	V_{SS}	–7.0 to +3.0	
Analog Input/Output Voltage	V_{TA}	V_{SS} –0.3 to V_{DD} +0.3	V
Digital Input/Output Voltage	V_{TD}	–0.3 to V_{DD} +0.3	V
Input/Output Current	I_T	–10 to +10	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to +125	°C
Ambient Operating Temperature	T_A	0 to +70	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



PLASTIC PACKAGE
DIP-40P-M01

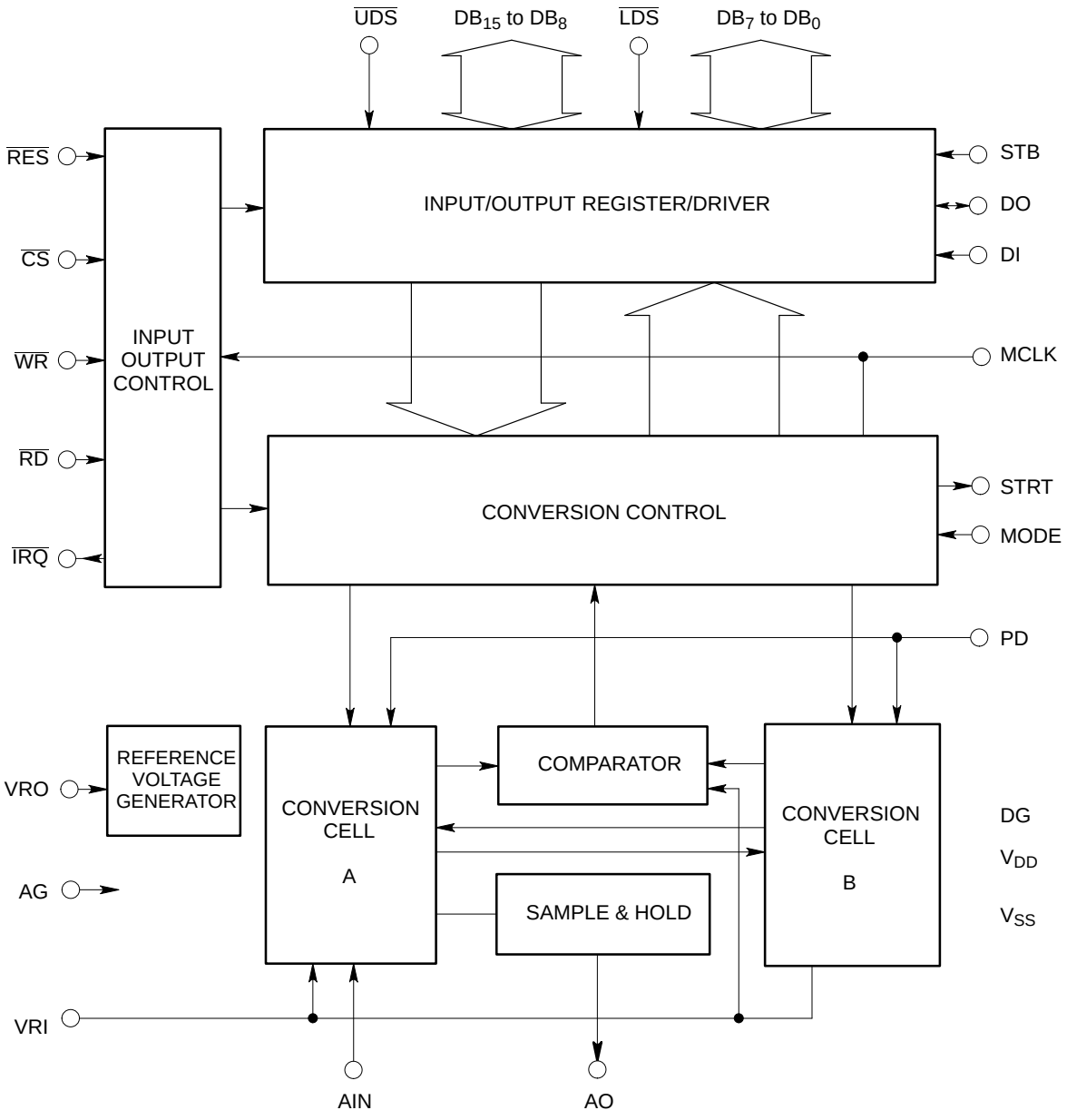
(TOP VIEW)



DIP-40P-M01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin No.	Description
V_{DD}	32	+5V Power Supply Input for Digital/Analog Circuit
V_{SS}	27	–5V Power Supply Input for Digital/Analog Circuit
DG	17	Digital Ground
AG	29	Analog Ground
VRI	30	External Reference Voltage Input. +2.5V typ. When the internal reference voltage is used VRI and VRO should be connected together.
VRO	31	Internal Reference Voltage Output. +2.5V typ.
MODE	24	Conversion Mode Select Input: When MODE is high, A/D mode is selected. When MODE is low, D/A mode is selected.
PD	25	Stand-by Mode Select Input for Analog Circuit: When PD is high, Stand-by mode is selected. When PD is low, the normal operation is selected.
$\overline{RES}$	33	Reset Input: When $\overline{RES}$ is low, all internal registers are reset and cleared. After power on, the reset operation is needed first.
MCLK	22	Conversion Clock Input: Conversion operation is synchronized with this clock.
A_{IN}	26	Analog Input for A/D Conversion: During STRT = H, this input is sampled. During D/A conversion, tit is recommended that this input pin be tied with AG.
AO	28	Analog Output for D/A Conversion: This output is updated after conversion, and keep the level until next completion of conversion.
DB_0 to DB_{15}	1 to 16	Parallel Data Input/Output: Can transmit A/D conversion data output or D/A conversion data input in 8- or 16-bit parallel. Due to three-state input, the pins are connected with microprocessor's bus directly. DB_{15} is MSB, DB_0 is LSB. When connected with 8-bit bus, DB_n and DB_{n+8} are connected together, where n = 0 to 7.
DI	20	Serial Data Input: At the rising edge of STB, the 1-bit data is transferred to the LSB of the input/output register. (See Serial Data Transfer.)
DO	19	Serial Data Output: The MSB of the input/output register is output. At the falling edge of STB, the output is changed. (See Serial Data Transfer.)
STB	21	Strobe Signal Input for Serial Data Transfer: Using $\overline{RD}$, $\overline{CS}$, $\overline{UDS}$, and $\overline{LDS}$, this input is internally gated. The rising edge of STB signal makes the output/input register shift by 1 bit. (See Serial Data Transfer.)
$\overline{CS}$	36	Chip Select Input: When $\overline{CS}$ is low, $\overline{RD}$ and $\overline{WR}$ signals are effective.
$\overline{WR}$	37	Data Write Input: When $\overline{WR}$ is low, stored data in DB_0 to DB_{15} are shifted into the input/output register, and the rising edge of the input makes the data latched and ready for AD or DA conversion operation. After $\overline{WR}$ goes high, conversion starts at the rising edge of MCLK, or at the completion of previous conversion.
$\overline{RD}$	38	Data Read Input: When $\overline{RD}$ is low, the stored data in output/input register are output at DB_0 to DB_{15}.
$\overline{UDS}$	39	High-order byte Select: When $\overline{UDS}$ is low, upper 8-bit data is transferred.
$\overline{LDS}$	40	Low-order byte Select: When $\overline{LDS}$ is low, the lower 8-bit data is transferred.
STRT	23	Conversion Start Output: This output indicates conversion start. During the first clock cycle of conversion, it becomes high. When it is high for AD conversion, A_{IN} input is sampled.
$\overline{IRQ}$	18	Interrupt Request Output as Conversion Completion: When conversion is completed, $\overline{IRQ}$ becomes low. When data transfer is instructed, ($\overline{RD}$ or $\overline{WR}$) and $\overline{CS}$, it becomes high. This output is an open-drain output.

NOTE: All digital input/output is TTL compatible.

OPERATIONAL DESCRIPTION

Input analog signal is converted to 16-bit digital signal or 16-bit digital signal is converted to analog signal. Either function is selected by mode select pin. MB87020 can be used for either parallel I/O connection or serial I/O connection with microprocessor.

Parallel I/O: Connected with μP 80 series 8-bit, 68 series 8-bit, 8086 series 16-bit and 68000 series 16-bit.
Serial I/O: Does not need as many signal lines as parallel I/O.

The following is a description of how to control MB87020 through these signal lines and receiving/delivering digital data.

1) MODE CONTROL

MB87020 has three operational modes: D/A conversion mode, A/D conversion mode and analog circuit stand-by mode. These modes are selected by MODE and PD pin as listed below.

When the mode change is indicated during conversion, the actual change of operational mode is done after the completion of conversion.

Mode	PD	Function
L	L	D/A conversion mode
	H	Analog circuit stand-by mode
H	L	A/D conversion mode
	H	Analog circuit stand-by mode

2) CONVERSION SEQUENCE

MB 87020's conversion sequence is comprised of the following four processes.

Conversion start request process — (Instruction to start conversion)
Conversion start process
Conversion process — Conversion process
Conversion completion process

The above processes are synchronized with MCLK signal, but data management can be independent from MCLK signal. And during conversion, next conversion startrequest can be provided.

Conversion start request process

Conversion start request is generated by the write cycle ($\overline{CS}$=$\overline{WR}$=L). After write cycle is completed (Rising edge of $\overline{CS}$ or $\overline{WR}$), conversion start request is generated. During D/A mode, write is possible in using write cycle. 16-bit data is written from lower 8-bit then the upper 8-bit. After that conversion start request is generated.

$\overline{LDS}$ AND $\overline{UDS}$ IN WRITE CYCLE AND CONVERSION START REQUEST

Mode	$\overline{LDS}$	$\overline{UDS}$	Conversion Start Request	Data Xmit (Write)	Operation
D/A	L or ⎍	L or ⎍	Generated	DB_0 to DB_{15}	16-bit Parallel Write
	L or ⎍	H	Not Generated	DB_0 to DB_7	Low-order Byte Write
	H	L or ⎍	Generated	DB_0 to DB_{15}	High-order Byte Write
	H	H	Generated		Serial Data Conversion
A/D	Don't Care	Don't Care	Generated		A/D Conversion Start

CONVERSION START PROCESS

When conversion is requested to start, operational conversion starts at the next rising edge of MCLK clock. When previous conversion is not completed, following conversion is postponed until previous conversion is completed. At this moment, START becomes High level in one clock cycle in order to indicate conversion start. At this time, it is prohibited that $\overline{WR}$=$\overline{CS}$="L". When A/D is converted, A_{IN} input is sampled at the same time.

CONVERSION PROCESS

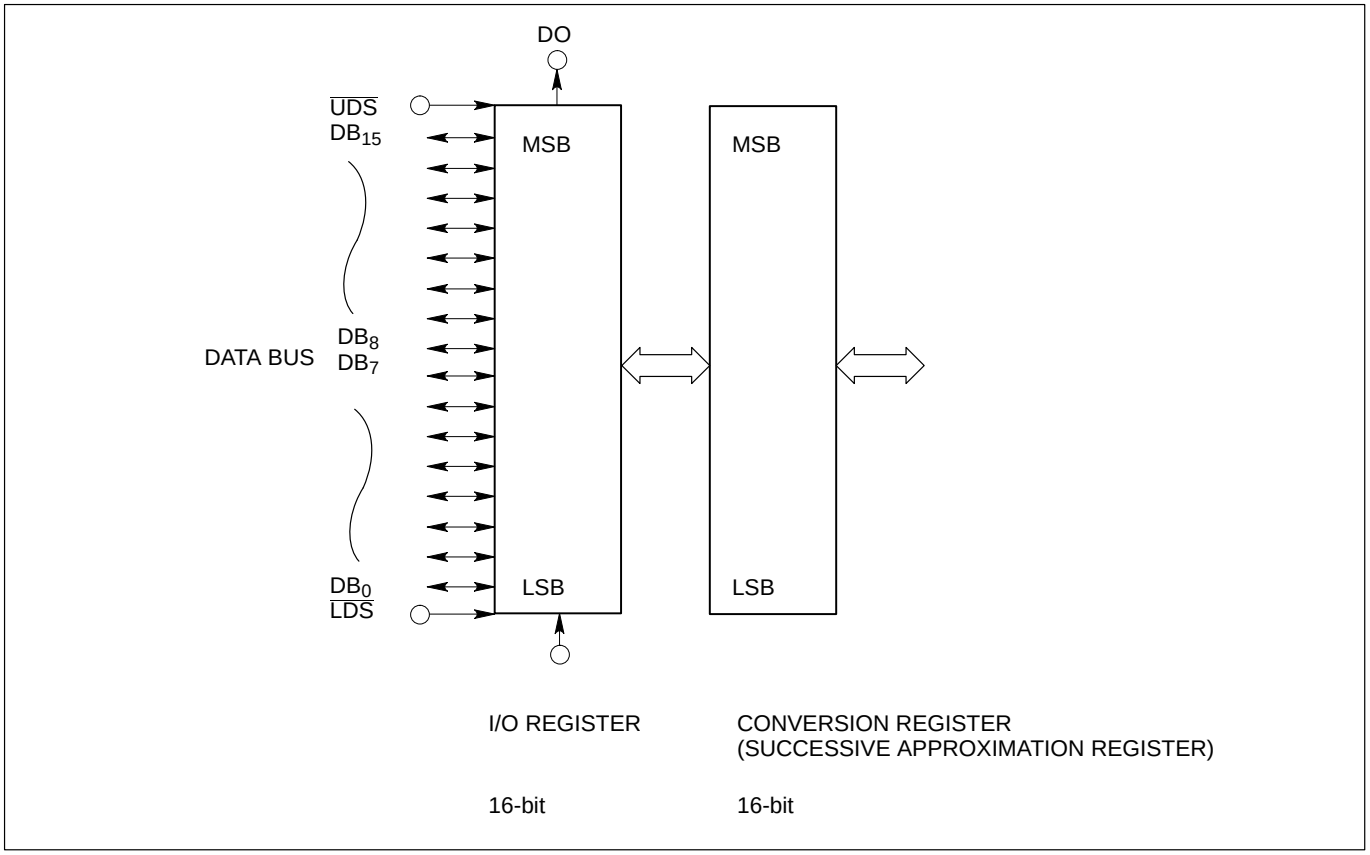
16th MCLK clock cycles are needed for one conversion process. From the second MCLK clock cycle, Write Mode is available and Conversion Start Request can be generated for the following conversion. Write Mode can be repeated in this period, but only the last Conversion Start Request and the last written data are effective.

CONVERSION COMPLETION PROCESS

The Conversion Process is completed after 16th MCLK clock cycles are passed from the conversion start. At the end of the conversion, $\overline{IRQ}$ goes low to tell the completion of the conversion outside of the chip. This output is an open-drain output and connected to microprocessor and provides interrupt request signal to it. When Write or Read Mode is executed, $\overline{IRQ}$ goes high. If Conversion Start Request is generated during conversion, the next conversion will start continuously after the current conversion is completed. The result of D/A conversion is output at A_0 at this time and output will remain at its last level. More than 1 MCLK cycle passed after conversion is completed, the result of A/D conversion can be read out at DB_0 to DB_{15} when $\overline{RD}$=$\overline{CS}$=$\overline{UDS}$=$\overline{LDS}$="L".

3) DATA TRANSMISSION

Data transmission between MB87020 and external is made through I/O register. I/O register does not control conversion directly, but they store A/D conversion results or D/A conversion data. Therefore, write/read are done freely except for the time of data transmission with register which directly control at the beginning and ending of conversion. Using this function, 8-bit parallel transmission, 8-bit serial transmission and data exchange during conversion are possible.



PARALLEL TRANSMISSION

Data is transmitted through DB_0 to DB_{15} and controlled by $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{UDS}$ and $\overline{LDS}$. In the transmission mode, it requires $\overline{CS}$ = Low. And in the write mode to MB87020, it requires $\overline{WR}$ = Low and read mode, $\overline{RD}$ = L. Upper byte (DB_8 to DB_{15}) transmission mode, it requires $\overline{UDS}$ = L, lower byte (DB_7 to DB_0), $\overline{LDS}$ = L. All required conditions are satisfied, data is transmitted. If no, data transmission mode is stopped and data is latched for write mode. During A/D mode, data is not written regardless $\overline{UDS}$ and $\overline{LDS}$.

I/O register stores latest A/D mode result or latest written data of D/A mode. During read cycle, it is possible to read out A/D conversion result and confirm D/A conversion result. Read/write of parallel data is controlled by control signal.

DATA CONTROL SIGNAL AND PARALLEL DATA TRANSMISSION

Mode	Reso-lution (Bit)	Read/Write	Data control signal					Condition		Conversion Start request	$\overline{IRQ}$=L Clear	Operation	
			$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{LDS}$	$\overline{UDS}$	DB_0 to DB_7	DB_8 to DB_{15}				
A/D			L	L	X	X	X	HZ	HZ	Generated	Clear	A/D conversion start request	
			L	X	L	H	H	HZ	HZ	Not Generated	Clear	Serial output	
	8	Read mode		H		L	H	Output	HZ	Not Generated	Clear	Read out conversion result	Lower byte
						H	L	HZ	Output	Not Generated	Clear		Upper byte
	16					L	L	Output	Output	Not Generated	Clear		All byte
D/A			L	L	X	H	H	HZ	HZ	Generated	Clear	Conversion start request of serial input data	
	8	Write mode				L	H	Input	HZ	Not Generated	Clear	Read out conversion result	Lower byte
						H	L	HZ	Input	Generated	Clear		Upper byte
	16					L	L	Input	Input	Generated	Clear		All byte
			L	X	L	H	H	HZ	Hz	Not Generated	Clear	Serial input	
	8	Read mode		H		L	H	Output	Hz	Not Generated	Clear	Confirm conversion result	Lower byte
						H	L	HZ	Output	Not Generated	Clear		Upper byte
	16					L	L	Output	Output	Not Generated	Clear		All byte
X			L	H	H	X	X	HZ	HZ	Not Generated	Not Clear		
			H	X	X	X	X	HZ	HZ	Not Generated	Not Clear		

Note: X = Don't care

SERIAL TRANSMISSION

DI, DO, STB, $\overline{RD}$ and $\overline{CS}$ are used for serial transmission. $\overline{UDS}$, $\overline{LDS}$ are settled as High, $\overline{RD}$, $\overline{CS}$ indicate transmission timing.

A/D MODE (DO OUTPUT)

After conversion is completed, MSB is output at the first falling edge of MCLK clock. When STB = H and $\overline{CS}$ = $\overline{RD}$ = L, from 2nd rising edge of MCLK clock, A/D conversion result is output serially from upper side synchronized with falling edge of STB clock. The output after 16-bit output is not related to any of converter result. Serial transmissions stop when STB = L and $\overline{CS}$ or $\overline{RD}$ = H.

D/A MODE (DI INPUT)

After conversion is completed, when $\overline{CS}$ = $\overline{RD}$ = L at STB = H after one clock cycle, DI is sampled as MSB and after that DI is sampled from the MSB every rising edge of STB clock. Transmission is completed when 16th DI is sampled as $\overline{CS}$ or $\overline{RD}$ = H at STB = L.

When 2 pcs. of MB87020 are used A/D, D/A mode separately with connecting DO of A/D and DI of D/A, STB, $\overline{RD}$, $\overline{CS}$ direct transmission becomes possible. If STB clock frequency is higher than MCLK clock, other signal or other conversion data can be transmitted by time sharing serially. If not, STB requires H, DI requires H or L.

CONVERSION RANGE AND CODE

A/D MODE

Input Voltage	Output code (DB_{15} to DB_0)
≥ $+V_{REF}$	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
$+V_{REF}$ –1LSB	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
$+V_{REF}/2$	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
–1LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
$-V_{REF}/2$	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
$-V_{REF}$ +1LSB	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
≤ $-V_{REF}$	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Note: V_{REF} = VRI input voltage
1LSB = $V_{REF}/2^{15}$
Output code will not become 1000 0000 0000 0000 under $-V_{REF}$ input voltage.

D/A MODE

Input code (DB_{15} to DB_0)	Output Voltage
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	≥ $+V_{REF}$
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}$ –1LSB
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$+V_{REF}/2$
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	–1LSB
1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}$ +1LSB
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	≤ $-V_{REF}$

Note: V_{REF} = VRI input voltage
1LSB = $V_{REF}/2^{15}$
Code input of 1000 0000 0000 0000 will not make the output of $-V_{REF}$.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin Name	Rating			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}	4.75	5.00	5.25	V
	V_{SS}	V_{SS}	–5.25	–5.00	–4.75	
Reference Voltage	V_{RI}	V_{RI}		2.5		V
Load Impedance	R_L	AO	20			kΩ
	C_L				20	pF
Ambient Operating Temperature	T_A		0		70	°C

DC CHARACTERISTICS

(DG = AG = 0V, V_{DD} = 5V ± 5%, V_{SS} = –5V ± 5%, f_{MCLK} = 800kHz, V_{RI} = 2.5V, T_A = 0 to 70°C)

Parameter		Symbol	Pin Name	Condition	Rating			Unit
					Min	Typ	Max	
Power Supply Current		I_{DD}	V_{DD}				15	mA
		I_{SS}	V_{SS}		–15			mA
Power Supply Current at Power Down		I_{DDST}	V_{DD}				1	mA
		I_{SSST}	V_{SS}		–0.5			mA
Reference Voltage		V_{RO}	V_{RI}			2.5		V
Digital High-level Input Voltage		V_{IH}	*1		2		V_{DD}	V
Digital Low-level Input Voltage		V_{IL}			0		0.8	V
Digital High-level Output Voltage		V_{OH}	*2	I_{OH} = 0.1mA	4.0		V_{DD}	V
				I_{OH} = 1mA	2.4		V_{DD}	V
Digital Low-level Output Voltage		V_{OL}	*3	I_{OL} = 2.4mA	0		0.4	µA
Digital Input Leak Current	“L” Level	I_{IL}	*3		–10		10	µA
	“H” Level	I_{IH}			–10		10	µA
$\overline{IRQ}$ Leakage Current at OFF		I_{LIRQ}	$\overline{IRQ}$	V_{OH} = V_{DD}	–10		10	µA
DB High-level Leakage Current at OFF		I_{LDBH}	DB_0 to DB_{15}		–10		10	µA
DB Low-level Leakage Current at OFF		I_{LDBL}		V_{OL}= 0V	–10		10	µA
Off-set Voltage		V_{OFF}	A_{IN}, A_O		–50		+50	mV
Linearity Error		LE				±0.02		%FSR
Differential Linearity Error		DLE				±0.02		%FSR

Note: *1. DB_0 to DB_{15}, DI, STB, MCLK, $\overline{UDS}$, $\overline{LDS}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, PD, MODE, $\overline{RES}$
*2. DB_0 to DB_{15}, DO
*3. DB_0 to DB_{15}, DO, $\overline{IRQ}$

AC CHARACTERISTICS

(DG = AG = 0V, V_{DD} = 5V ± 5%, V_{SS} = –5V ± 5%, f_{MCLK} = 800kHz, V_{RI} = 2.5V, T_A = 0 to 70°C)

Parameter	Symbol	Pin Name	Condition		Rating			Unit
					Min	Typ	Max	
Clock Frequency	f_{MCLK}	MCLK			10		800	kHz
	f_{STB}	STB					2.5	MHz
Clock Duty Ratio	D_{MCLK}	MCLK			45	50	55	%
Sampling Rate	f_{SAMPLE}						50	kSPS
Absolute Gain	G_A		1kHz, FS –20dB sine wave 50kSPS T_A = 25°C BW = 20kHz	V_{RI} = 2.5V	–0.1	0	+0.1	dB
				Connect to V_{RI} and V_{RO}	–0.5	0	+0.5	
Total Harmonic Distortion	T.H.D.		1kHz, sine wave 50kSPS T_A = 25°C PW = 20kHz	FS –20dB			–60	dB
				FS		–76		
Input Impedance (R_1/C_1)	R_1	A_{IN}	A/D mode during STRT = H		100			kΩ
	C_1					50	100	pF

SWITCHING CHARACTERISTICS

(DG = AG = 0V, V_{DD} = 5V, V_{SS} = –5V, f_{MCLK} = 720kHz, V_{RI} = 2.5V, T_A = 25°C)

Parameter	Figure	Symbol	Rating		Unit
			Min	Max	
Data Write Pulse Width	1	t_{WT}	200		ns
Data Setup Time for Data Write	1	t_{SBW}	200		ns
Data Hold Time for Data Write	1	t_{HBW}	50		ns
Data Write Interval	1	t_{IW}	200		ns
Data Non-Write $\overline{LDS}$/$\overline{UDS}$ Setup Time	1	t_{SDW}	50		ns
Data Non-Write $\overline{LDS}$/$\overline{UDS}$ Hold Time	1	t_{HDW}	50		ns
Write Command Pulse Width	1	t_{WW}	200		ns
Write Command Hold Time for First Conversion Cycle	2	t_{HWN}	0		ns
Write Command Setup Time Preventing from Conversion Start	2	t_{SWI}	100		ns
Write Command Hold Time Not to Start Conversion	2	t_{HWP}	100		ns
Write Command Hold Time for Conversion Start	2	t_{SWP}	100		ns
$\overline{WR}$ Setup Time for Data Read (D/A mode only)	3	t_{SWC}	50		ns
$\overline{WR}$ Hold Time for Data Read (D/A mode only)	3	t_{HWC}	50		ns
Data Read Pulse Width	3	t_{WR}	200		ns

SWITCHING CHARACTERISTICS (Continued)

(DG = AG = 0V, V_{DD} = 5V, V_{SS} = –5V, f_{MCLK} = 720kHz, V_{RI} = 2.5V, T_A = 25°C)

Parameter	Figure	Symbol	Rating		Unit
			Min	Max	
Delay Time to Valid Data Output	3	t_{EB}	0	200	ns
Disappearance Time for Valid Data	3	t_{DB}	0		ns
$\overline{RD}$ Hold Time for Last Conversion Cycle	4/5	t_{HRK}	0		ns
$\overline{RD}$ Setup Time for Last Conversion Cycle	4/5	t_{SRK}	0		ns
$\overline{LDS}$/$\overline{UDS}$ Setup Time for Serial Data Transfer Start	5	t_{SDR}	50		ns
$\overline{LDS}$/$\overline{UDS}$ Hold Time for Serial Data Transfer Completion	5	t_{HDR}	50		ns
STB Setup Time for Read Command	5	t_{STR}	100		ns
STB Hold Time for Read Command	5	t_{HTR}	100		ns
High-level STB Pulse Width	5	t_{WSH}	200		ns
Low-Level STB Pulse Width	5	t_{WSL}	200		ns
MSB Output Delay Time	5	t_{DOK}	0	500	ns
Serial Output Delay Time	5	t_{DOT}	0	150	ns
MSB Input Setup Time	5	t_{SIR}	50		ns
MSB Input Hold Time	5	t_{HIR}	50		ns
Serial Input Setup Time	5	t_{SIT}	50		ns
Serial Input Hold Time	5	t_{HIT}	50		ns
STRT Output Delay Time	6	t_{DSK}	0	300	ns
Analog Input Setup Time	6	t_{SA}	1.2		µs
Analog Input Hold Time	6	t_{HA}	0		ns
Command Setup Time for $\overline{IRW}$ = Low	6	t_{SCK}	200		ns
$\overline{IRQ}$ Falling Delay Time	6	t_{DIK}	0	200	ns
$\overline{IRQ}$ Rising Delay Time (Pull-up Resistance = 5kΩ, C_L = 10pF)	6	t_{DIC}	0	200	ns
Analog Output Settling Time	6	t_{DA}	0	8	µs
Valid Output Hold Time	6	t_{AE}		500	µs
$\overline{CS}$ Setup Time for Reset Completion	7	t_{SRES}	500		ns
$\overline{CS}$ Hold Time for Reset Completion	7	t_{HRES}	20		clock cycle
Reset Pulse Width	7	t_{WRES}	500		ns
PD Setup Time	8	t_{SPK}	100		ns
PD Hold Time	8	t_{HPK}	500		ns
MODE Setup Time	8	t_{SMK}	100		ns
MODE Hold Time	8	t_{HMK}	500		ns
Power Down Time from Conversion Completion	9	t_{PDK}		1	ms
Power Down Time from PD	9	t_{PDP}		1	ms
Power Up Time	9	t_{PUP}		10	ms

TIMING DIAGRAMS

PARALLEL TRANSMISSION

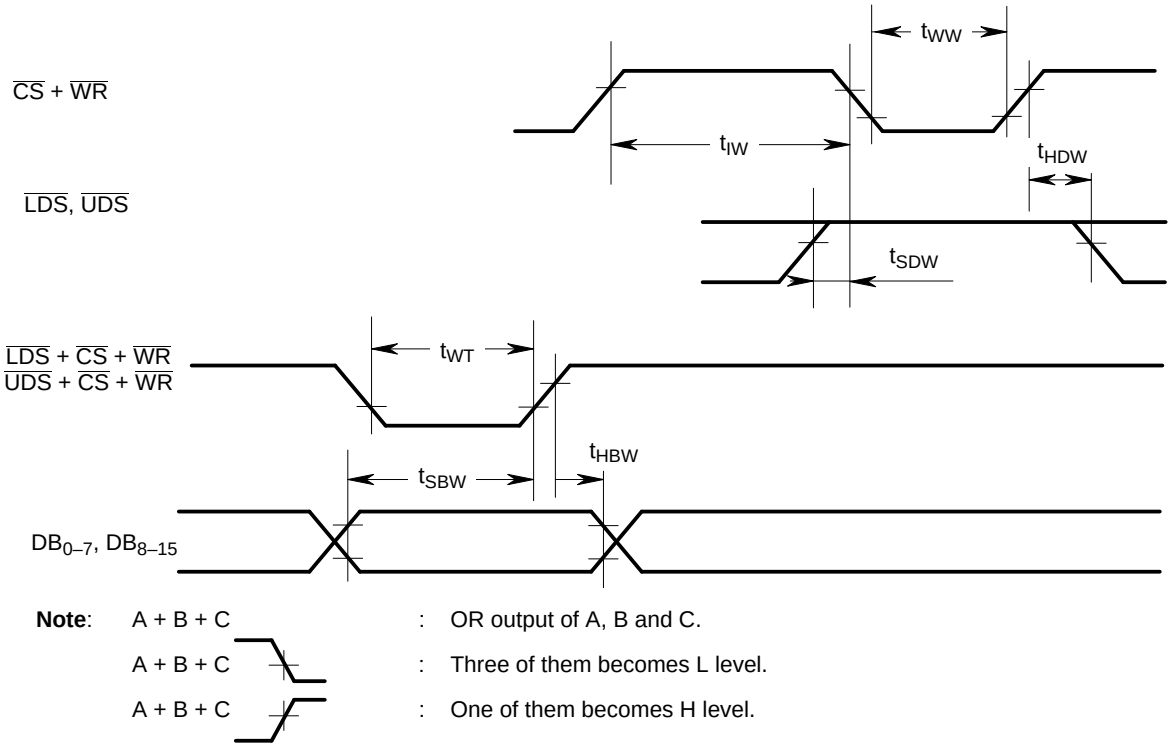


Figure 1. Write Cycle Timing 1 (Data Transmission)

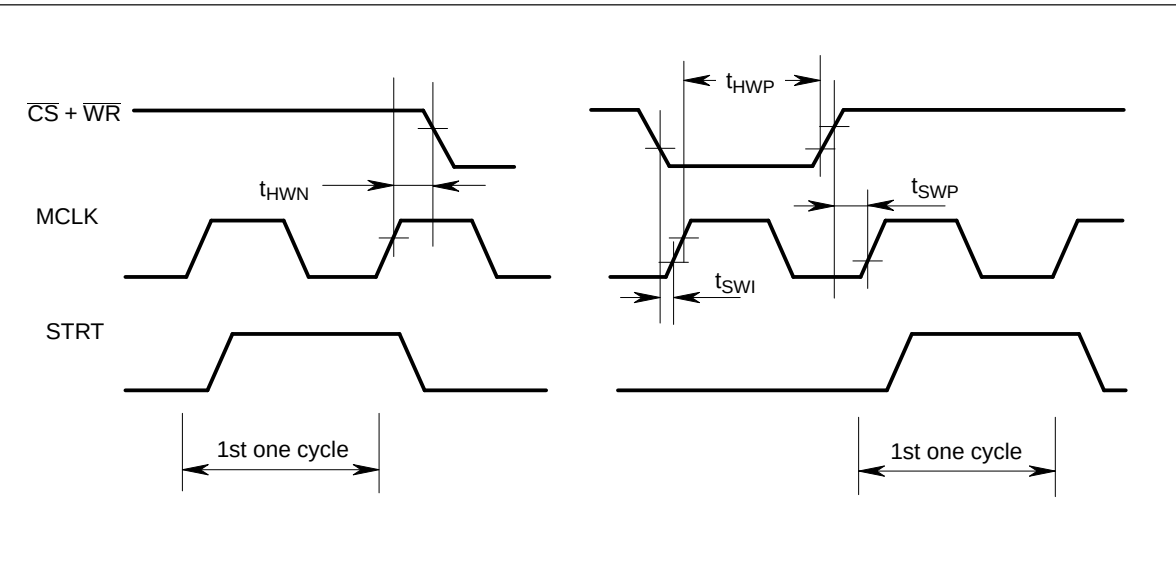


Figure 2. Write Cycle Timing 2 (Conversion Start)

TIMING DIAGRAMS (Continued)

PARALLEL TRANSMISSION

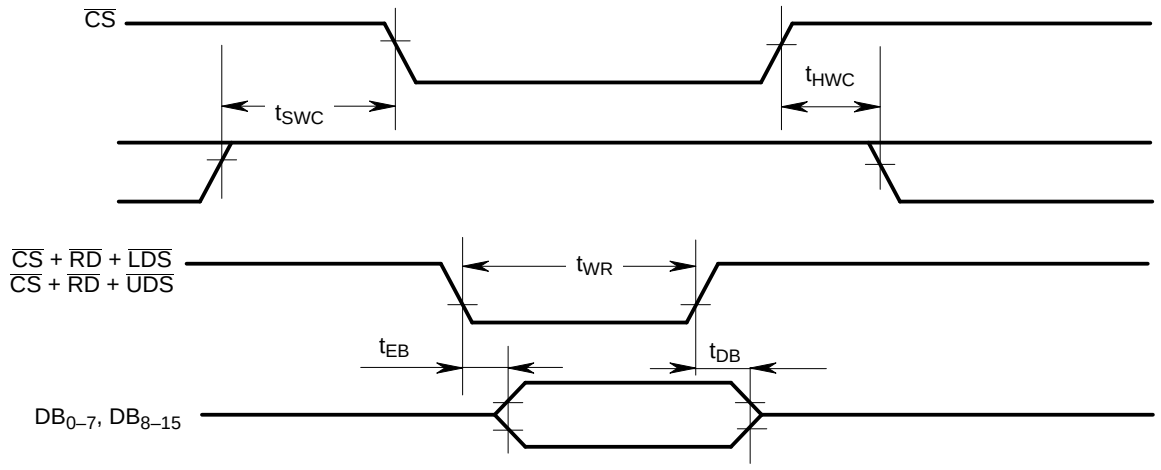
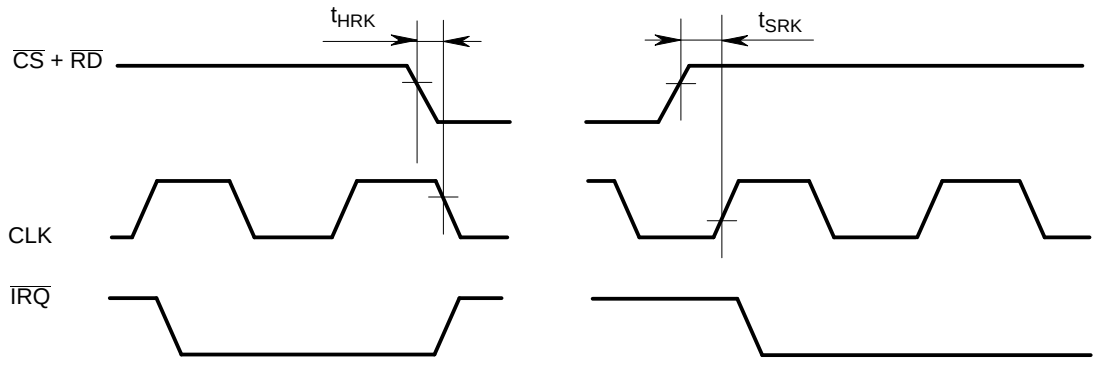


Figure 3. Read Cycle Timing 1 (Data Transmission)



Note: Except for serial transmission mode, t_{HRK}, t_{SRK} specification is necessary to read out normally. Unless these spec are specified, the data will not destroy.

Figure 4. Read Cycle Timing 2 (Conversion Start)

TIMING DIAGRAMS (Continued)

SERIAL TRANSMISSION

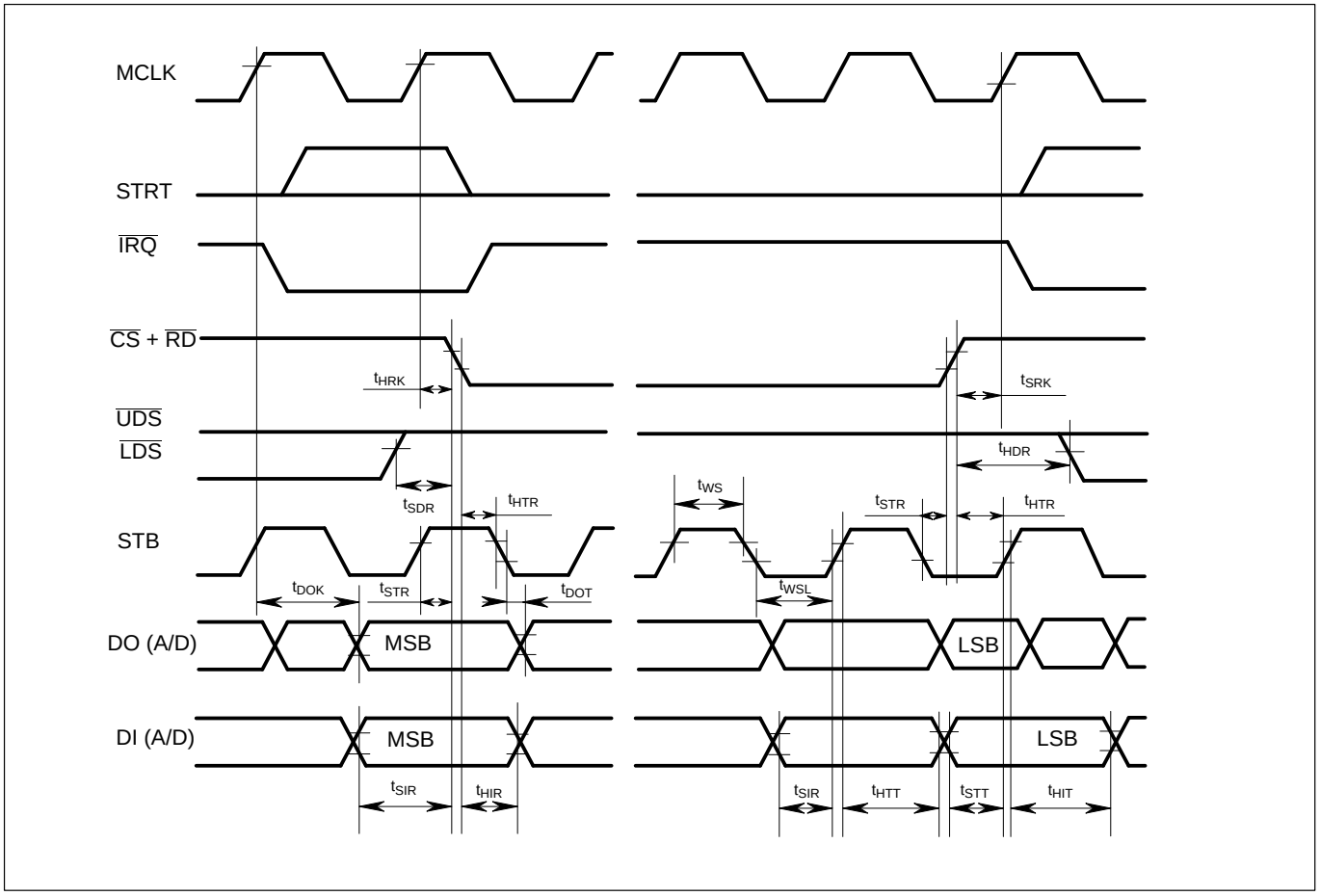
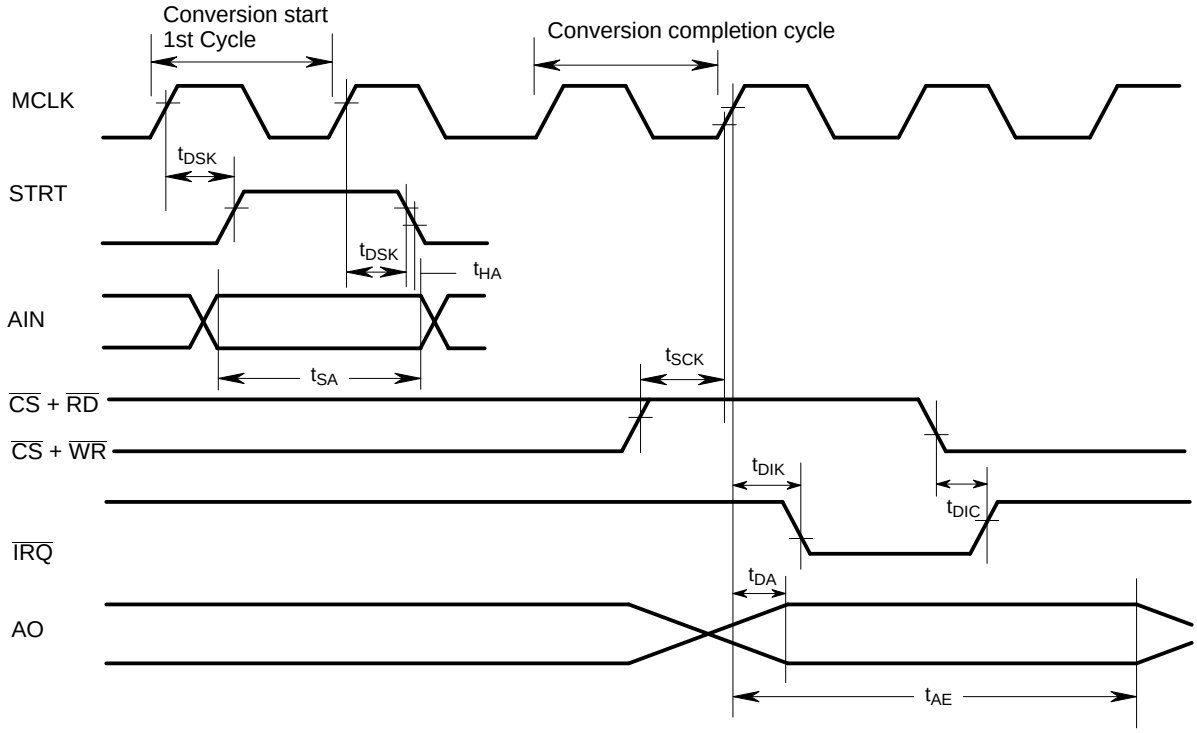


Figure 5. Serial Input/Output

TIMING DIAGRAMS (Continued)

OTHER TIMING



Note: t_{SCX} is a necessary condition that $\overline{IRQ}$ becomes L. However, if this condition is not satisfied, the operation has no effect.

Figure 6. STRT, IRQ, AIN, PO Timing

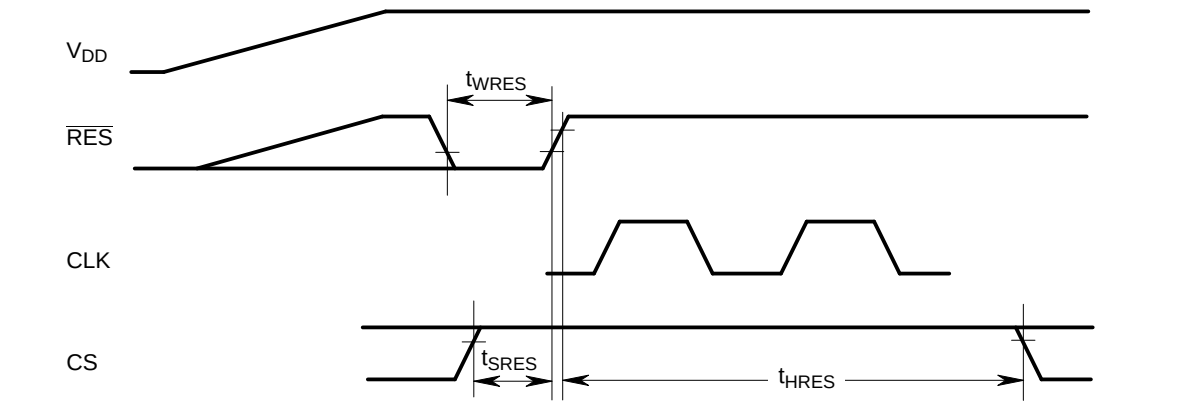


Figure 7. Power On/Rest Timing

TIMING DIAGRAMS (Continued)

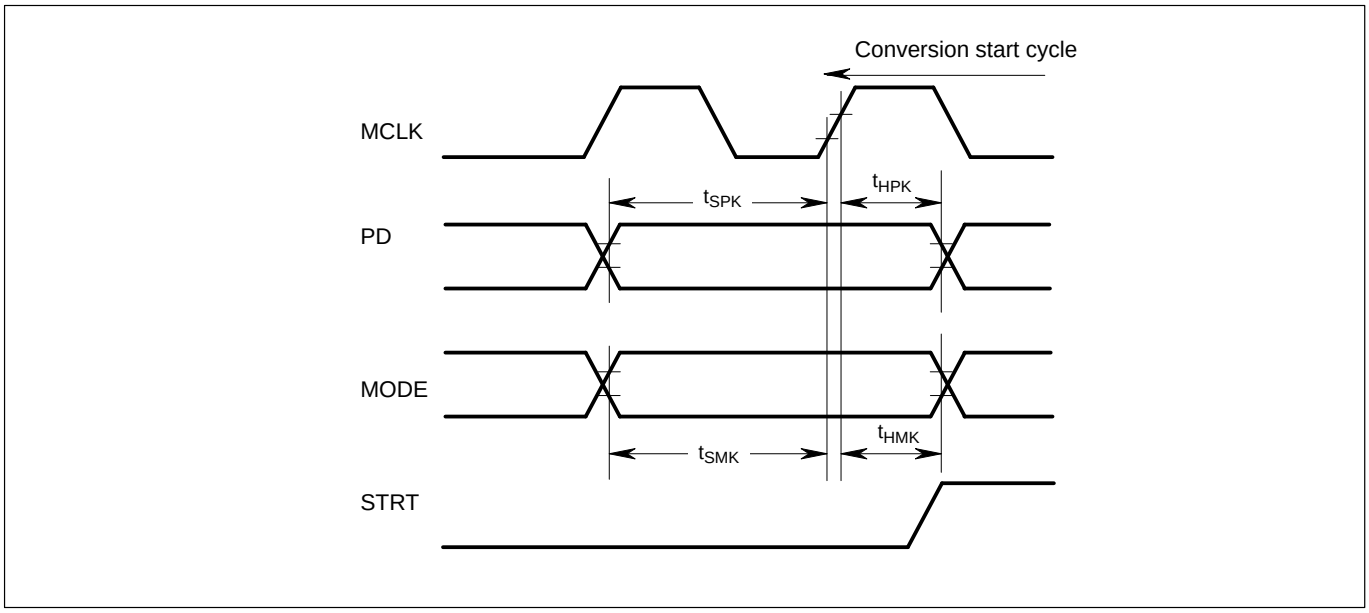


Figure 8. Mode Changing Timing

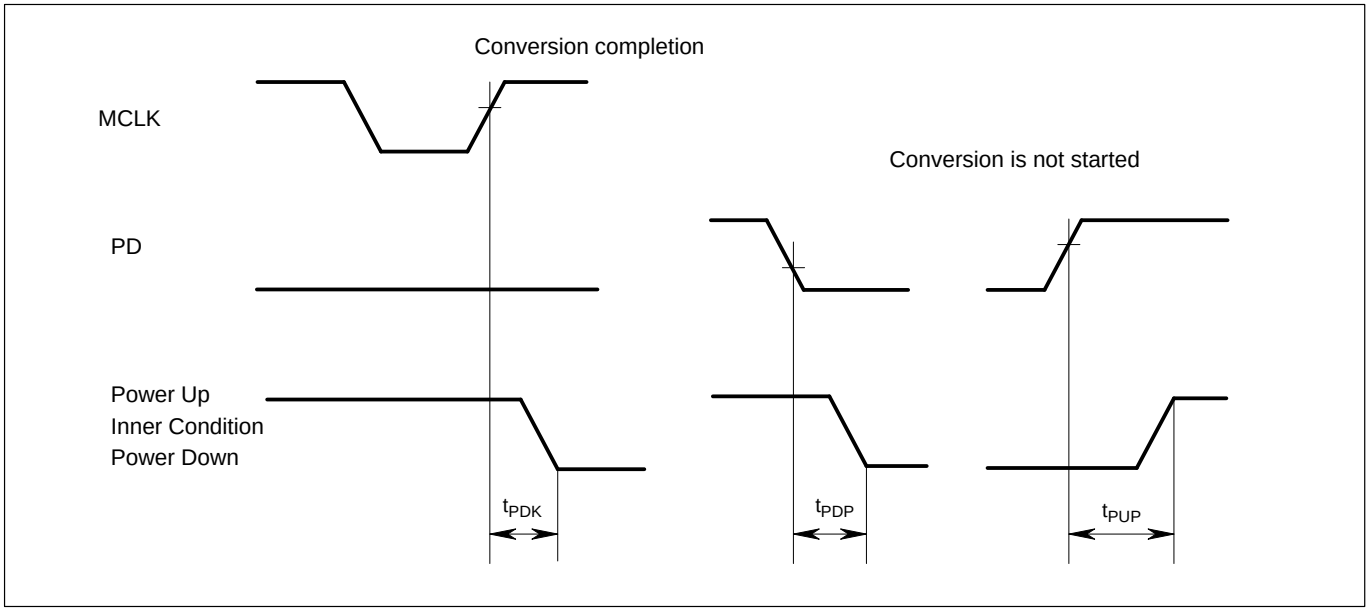


Figure 9. Power Down Timing

OPERATING TIMING

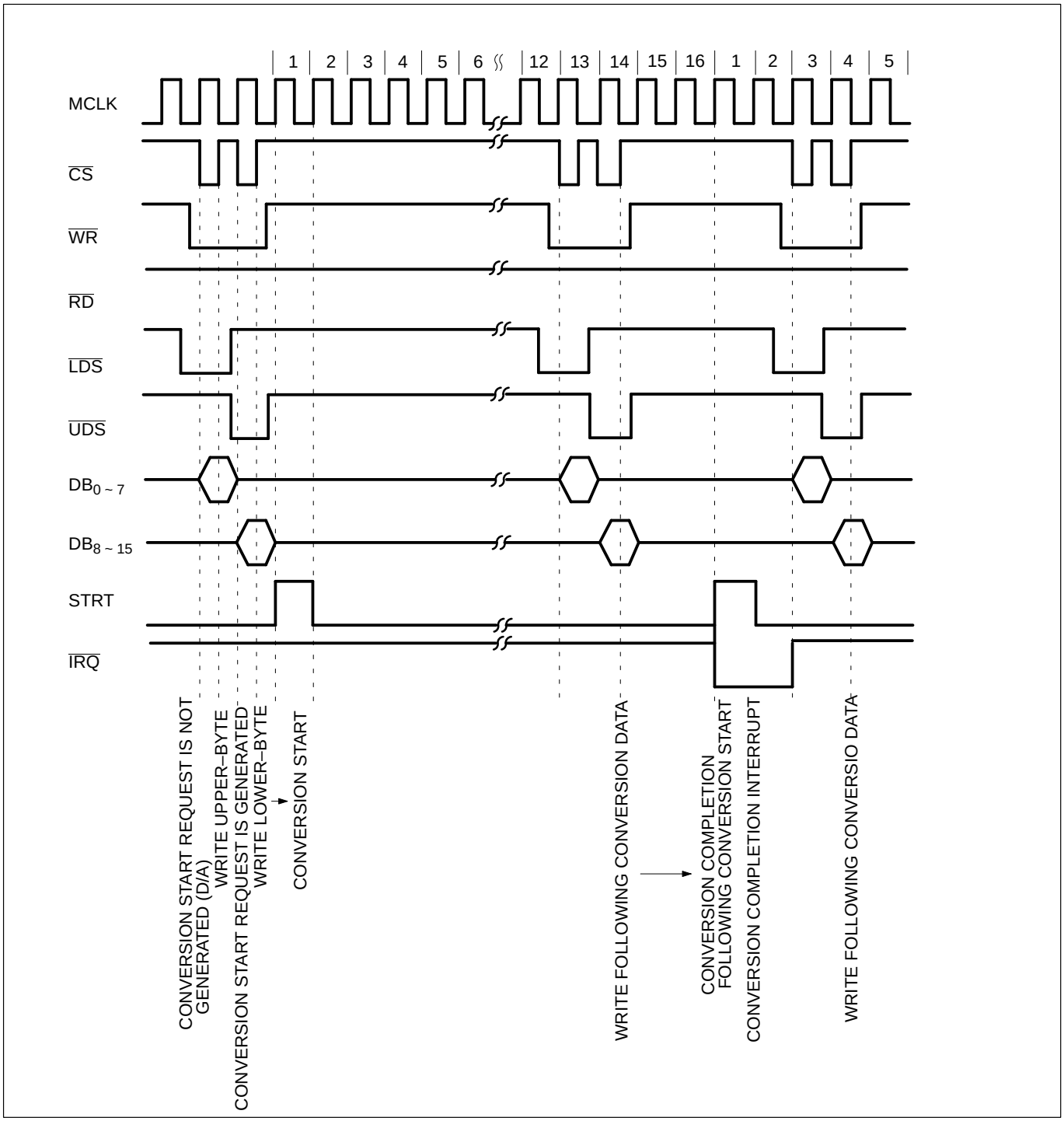


Figure 10. D/A, 8–bit Microprocessor

OPERATING TIMING (Continued)

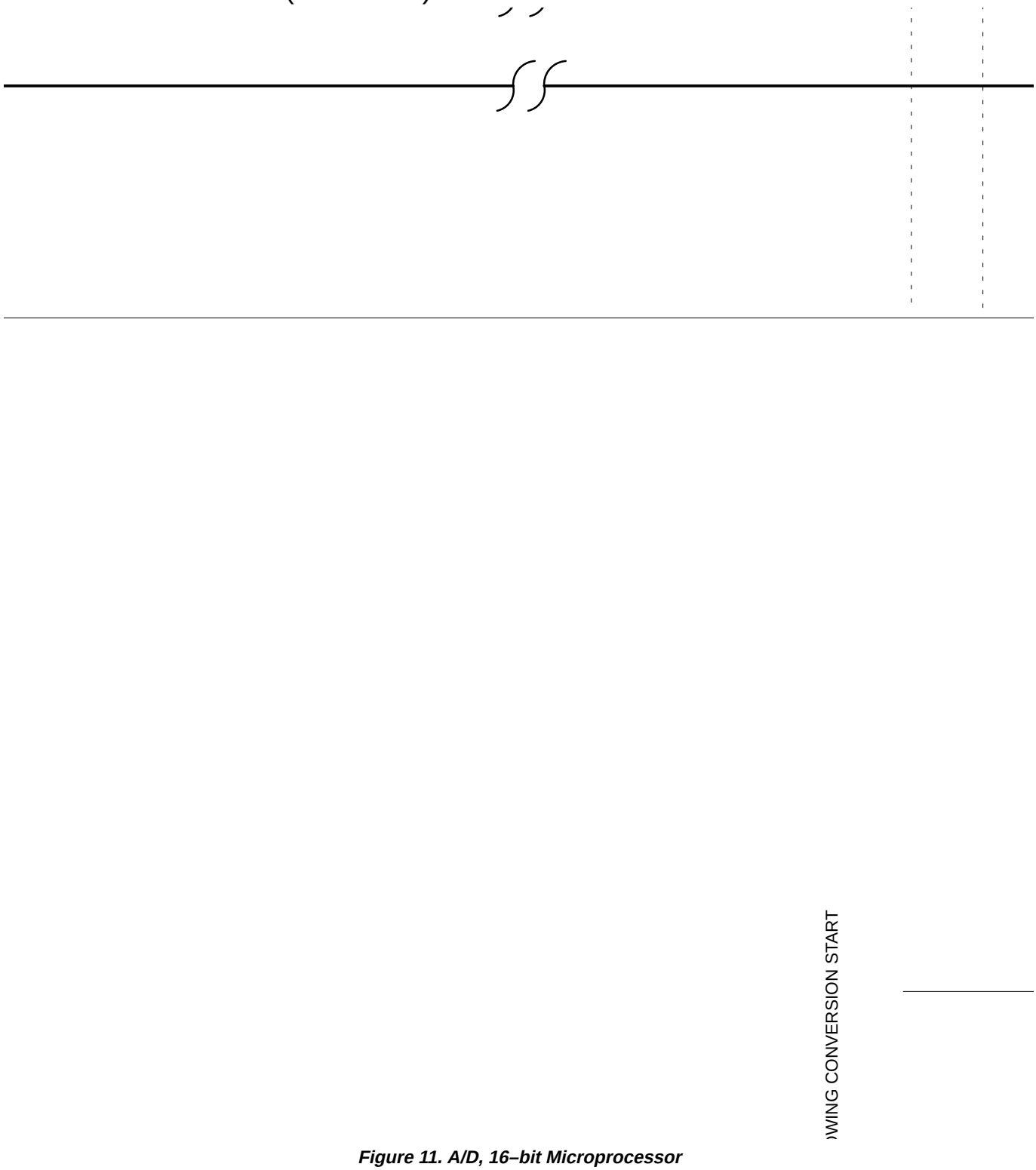


Figure 11. A/D, 16–bit Microprocessor

OPERATING TIMING (Continued)

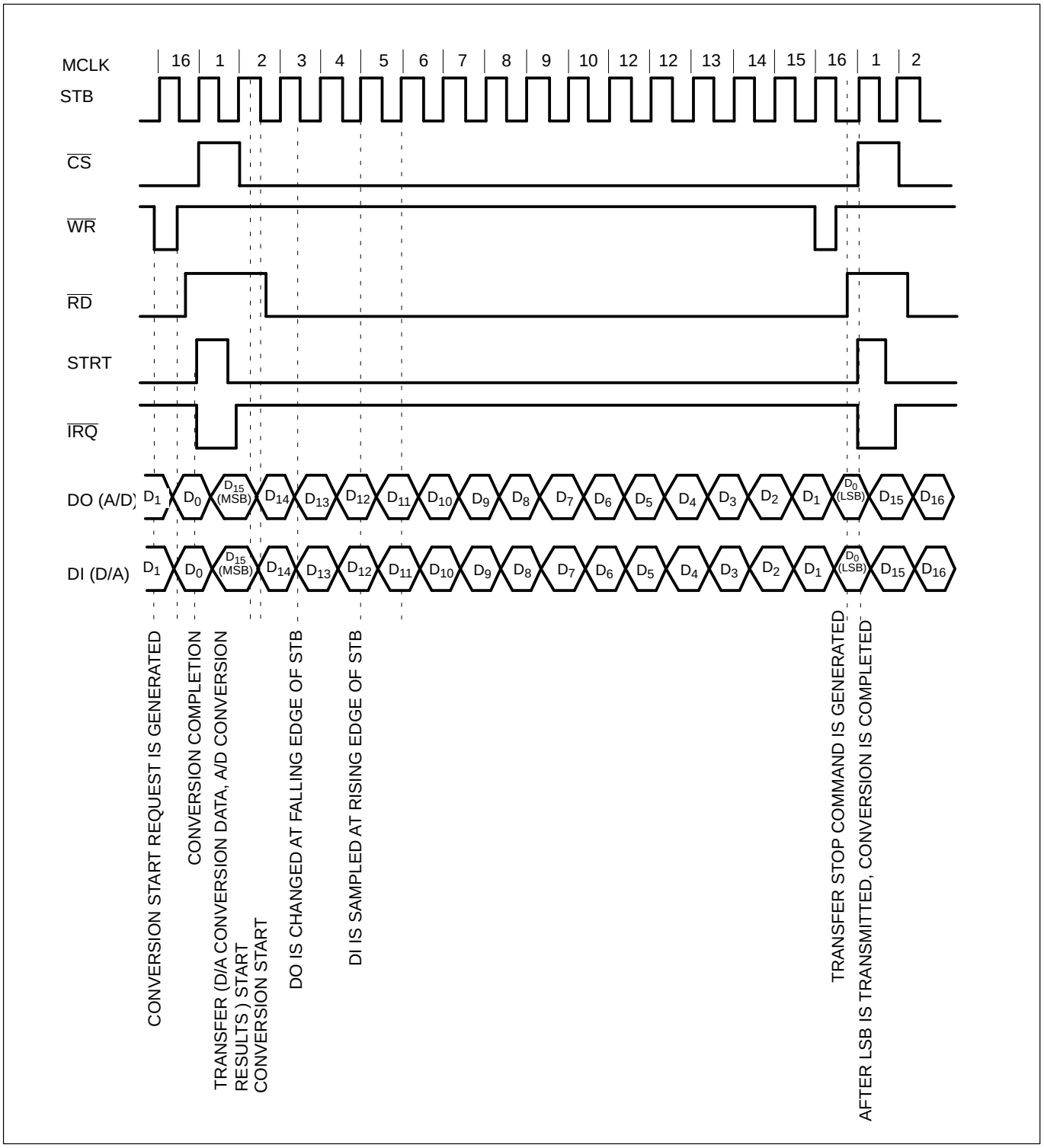
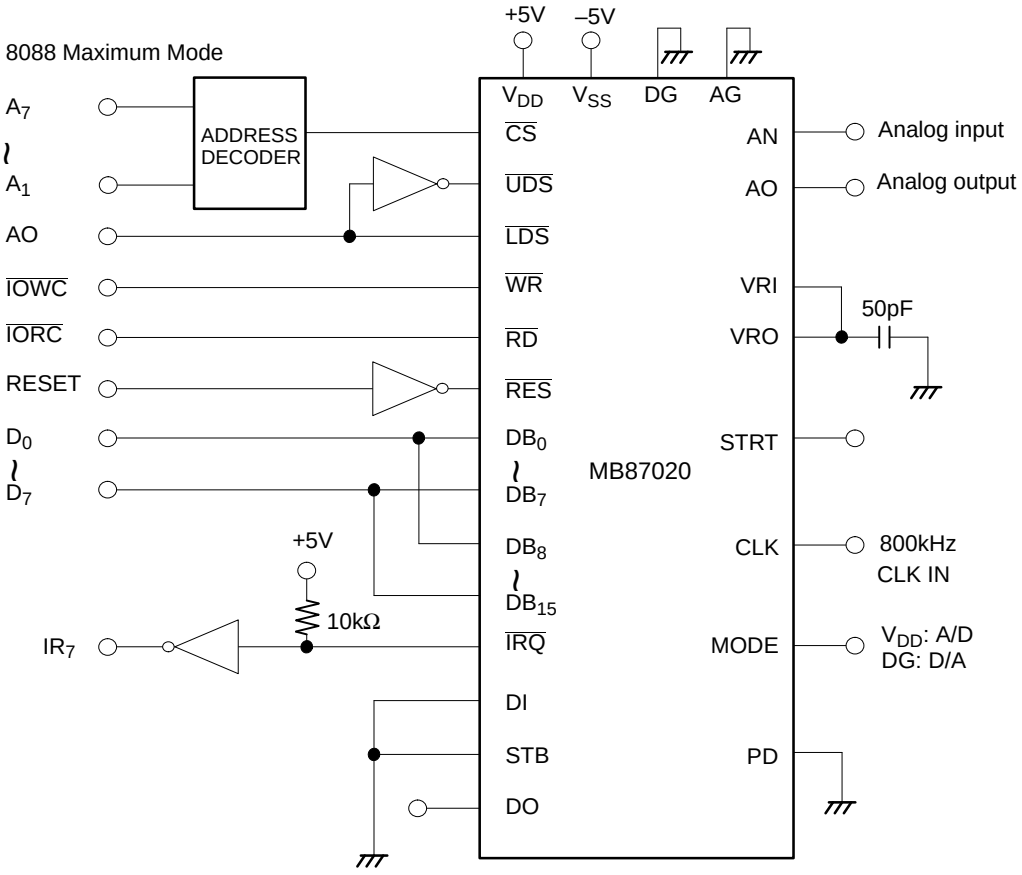


Figure 12. A/D, Serial Output or D/A, Serial Input

INTERFACE CIRCUIT EXAMPLE



Note: When $\overline{LDS}$ is low, even bytes are stored in the lower I/O register.
When $\overline{UDS}$ is low, odd bytes are stored in the high I/O register.
Interruption is used as the highest priority.
Conversion range is between –2.5V and +2.5V.
The data stored in AX register are D/A converted by OUT command.

Figure 13. Interface with 8088 Maximum Mode

INTERFACE EXAMPLE WITH VARIOUS INTERFACE

Object		Control Signal	Example of main input control pin of MB87020						
			DB_0 to DB_7	DB_8 to DB_{15}	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{UDS}$	$\overline{LDS}$
MP	Z80 (80 series 8-bit CPU)	$\overline{WR}$, $\overline{RD}$, D_0 to D_7, A_0 to A_{15}	D_0 to D_7	D_0 to D_7	Address decoder output	$\overline{WR}$	$\overline{RD}$	Inverted output of A	AO
	6800 (68 series 16-bit CPU)	R/$\overline{W}$, VMA, ∅2, D_0 to D_7, A_0 to A_{15}	D_0 to D_7	D_0 to D_7	***	R/$\overline{W}$	Inverted output of R/$\overline{W}$	Inverted output of A	AO
	8068 (86 series 16-bit CPU)	$\overline{MWTC}$, $\overline{MRDC}$, D_0 to D_{15}, A_0 to A_{19}	D_0 to D_7	D_8 to D_{15}	Address decoder output	$\overline{MWTC}$	$\overline{MRDC}$	$\overline{BHE}$	AO
	6800 (6800 series 16-bit CPU)	R/$\overline{W}$, AS, $\overline{LDS}$, $\overline{UDS}$, A_0 to A_{23}	D_0 to D_7	D_8 to D_{15}	****	R/$\overline{W}$	Inverted output of R/$\overline{W}$	$\overline{UDS}$	$\overline{LDS}$
D/A conversion only, D_0 to D_{15} (Parallel data), Conversion start request signal ST (Low active)			D_0 to D_7	D_8 to D_{15}	L	$\overline{ST}$	H	L	L
A/D conversion only, Conversion start request signal ST (Low active) D_0 to D_{15} (Parallel data request)			D_0 to D_7	D_8 to D_{15}	L	$\overline{ST}$	L	L	L
A/D or D/A serial conversion transmission BUSY (Low active) Conversion start request signal ST (Low active)			L or H	L or H	L	$\overline{ST}$	$\overline{BUSY}$	H	H
MB87064 (Fujitsu 16-bit DSP)		$\overline{BCT}$, $\overline{ACT}$, D_0 to D_{15}	D_0 to D_7	D_8 to D_{15}	L	$\overline{BCT}$	$\overline{ACT}$	L	L

*** Address decoder output after VMA, ∅2 gate

**** Address decoder output after AS gate

TEST CIRCUITS

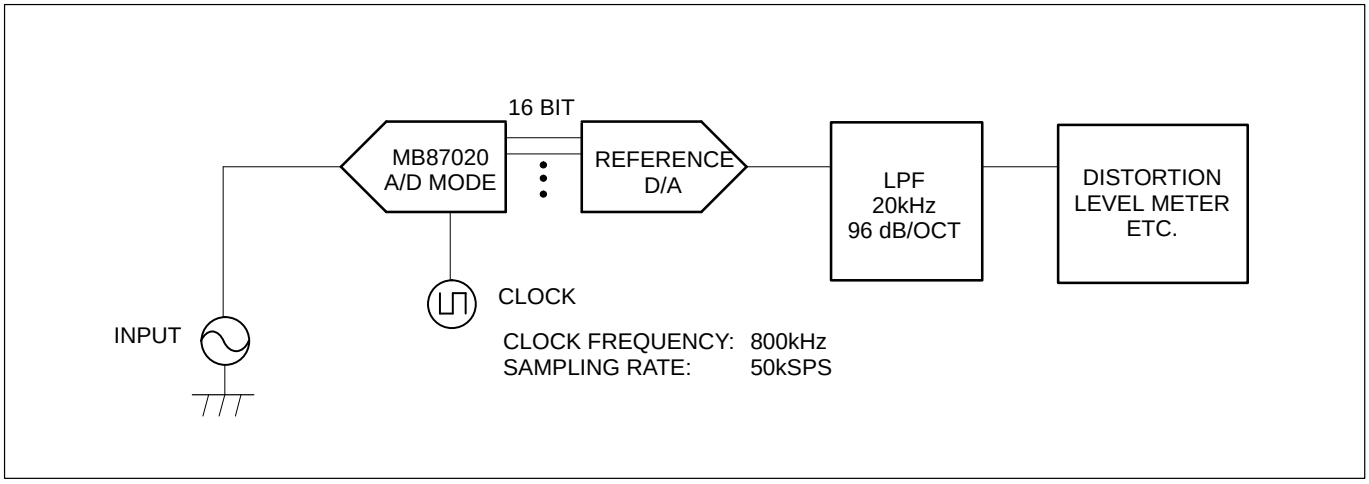


Figure 14. Test Circuit for Distortion Ratio (1)

TEST CIRCUITS (Continued)

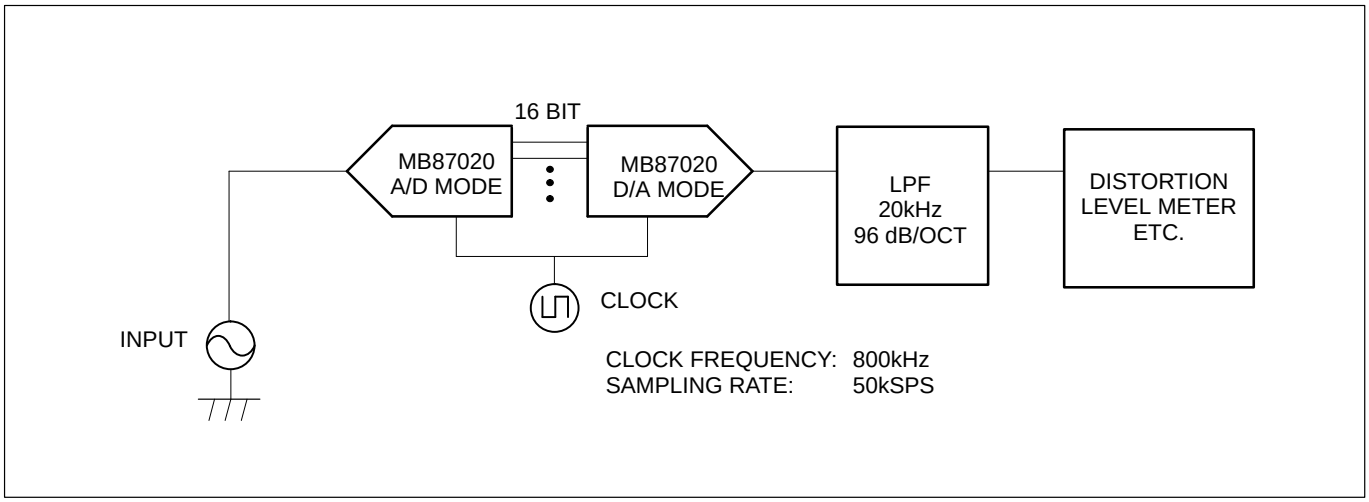


Figure 15. Test Circuit for Distortion Ratio (2)

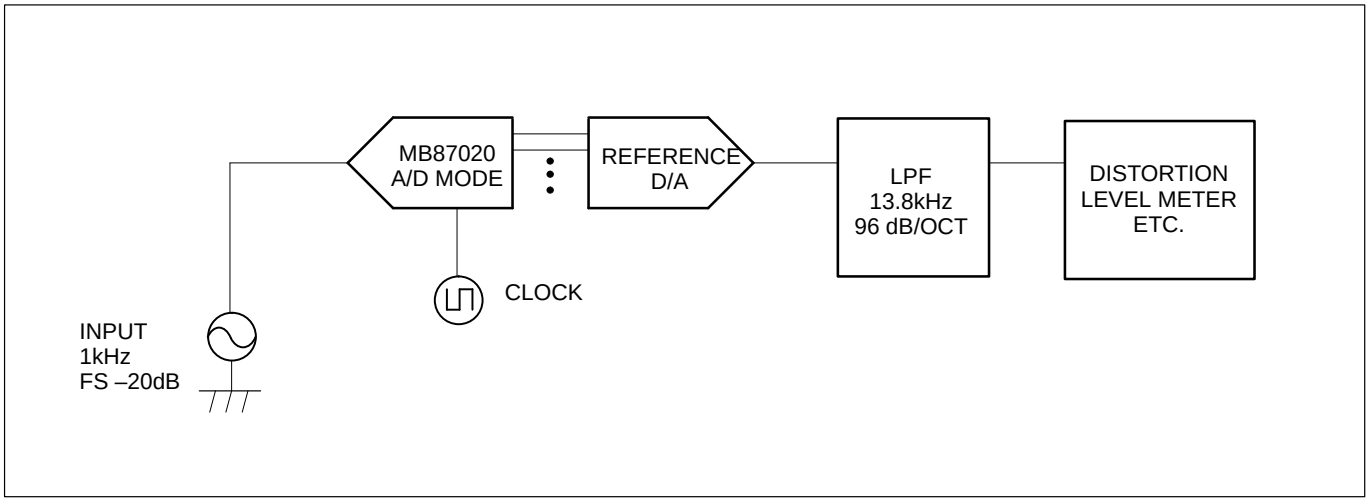


Figure 16. Test Circuit for Distortion Ratio (3)

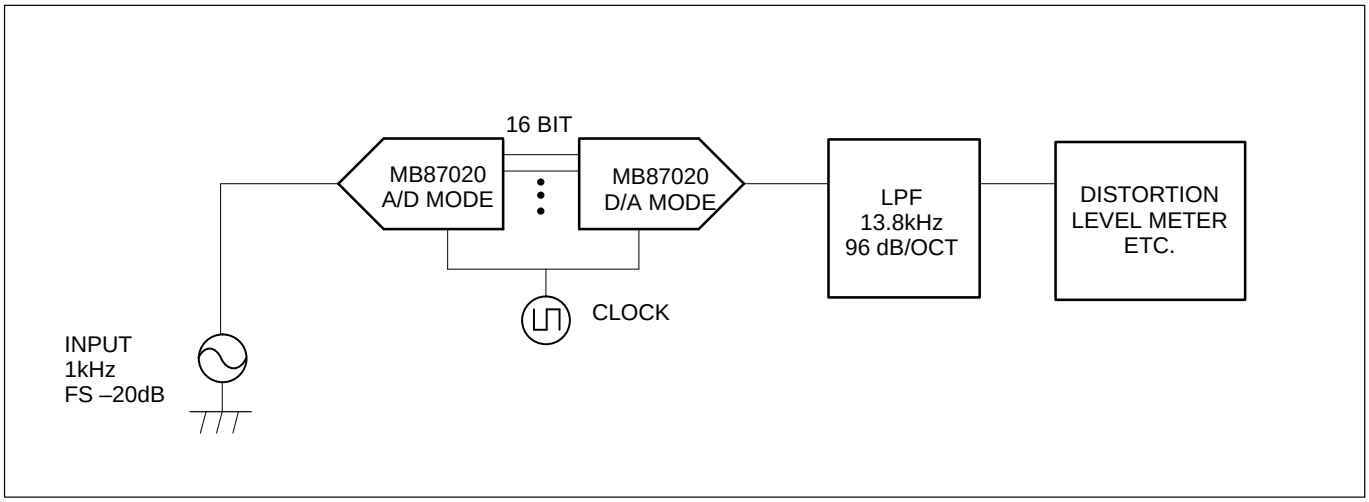


Figure 17. Test Circuit for Distortion Ratio (4)

TEST CIRCUITS (Continued)

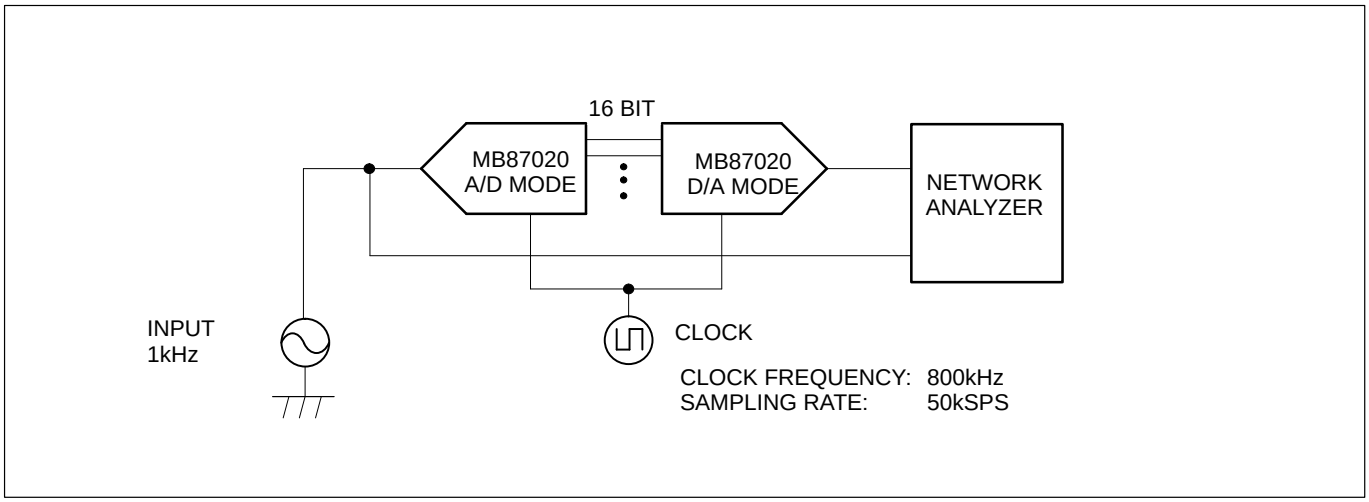


Figure 18. Test Circuit for Absolute Gain

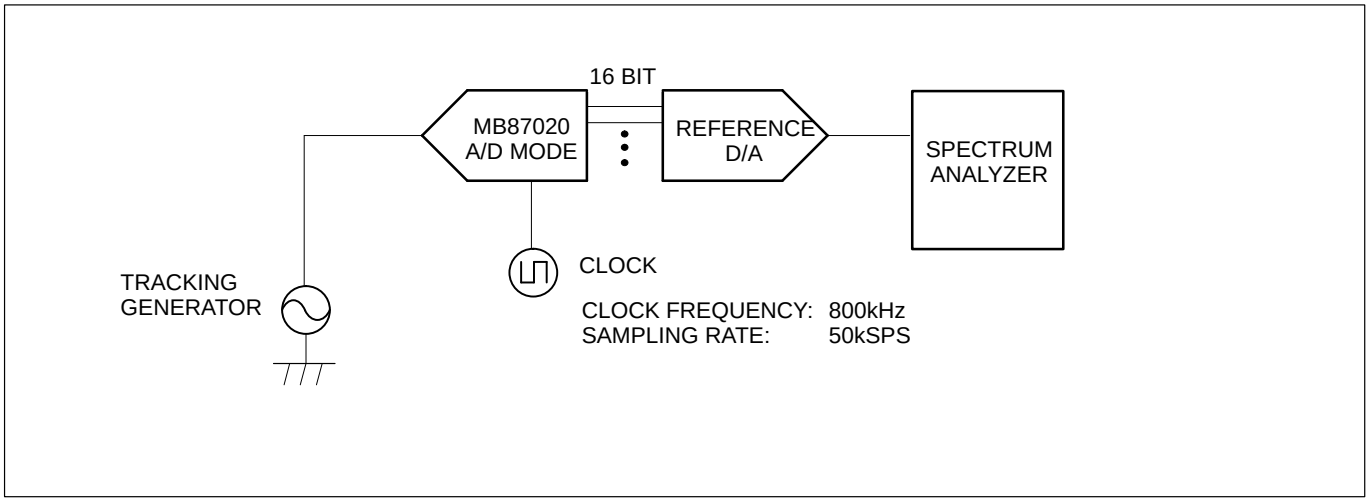


Figure 19. Test Circuit for Frequency Characteristics (1)

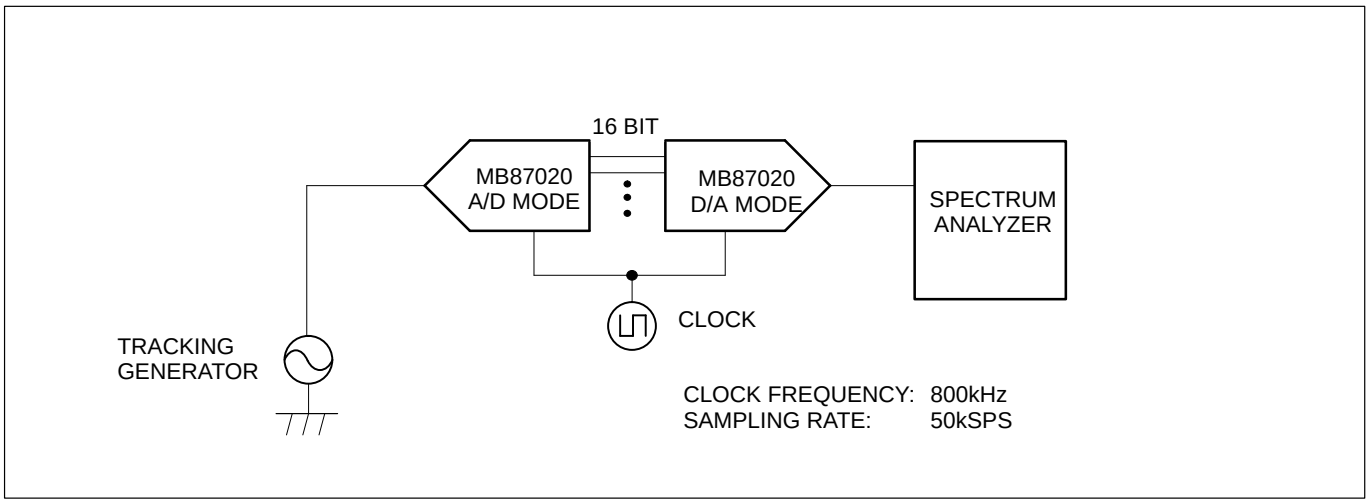


Figure 20. Test Circuit for Frequency Characteristics (2)

TYPICAL PERFORMANCE CHARACTERISTICS

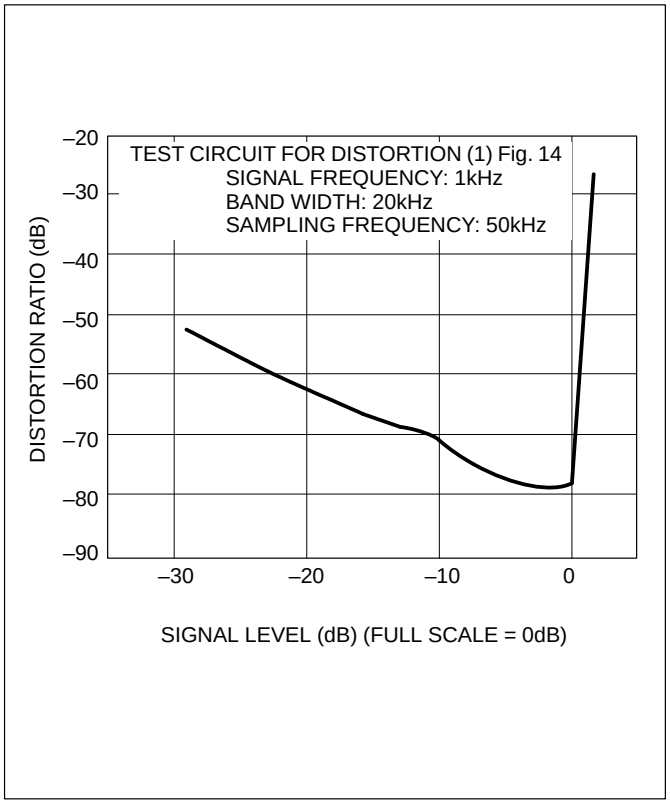


Figure 21. Signal Level of ADC Mode vs. Distortion Ratio

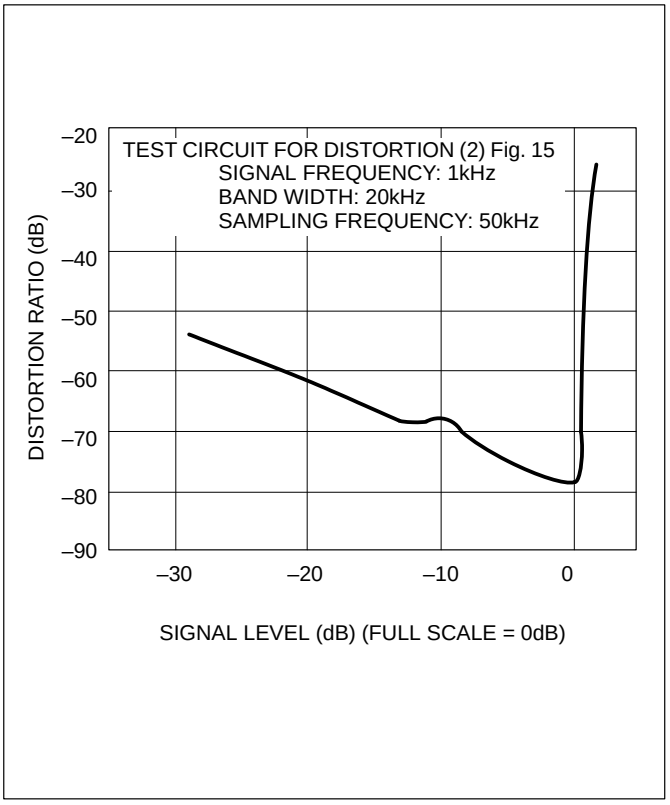


Figure 22. Signal Level of DAC Mode vs. Distortion Ratio

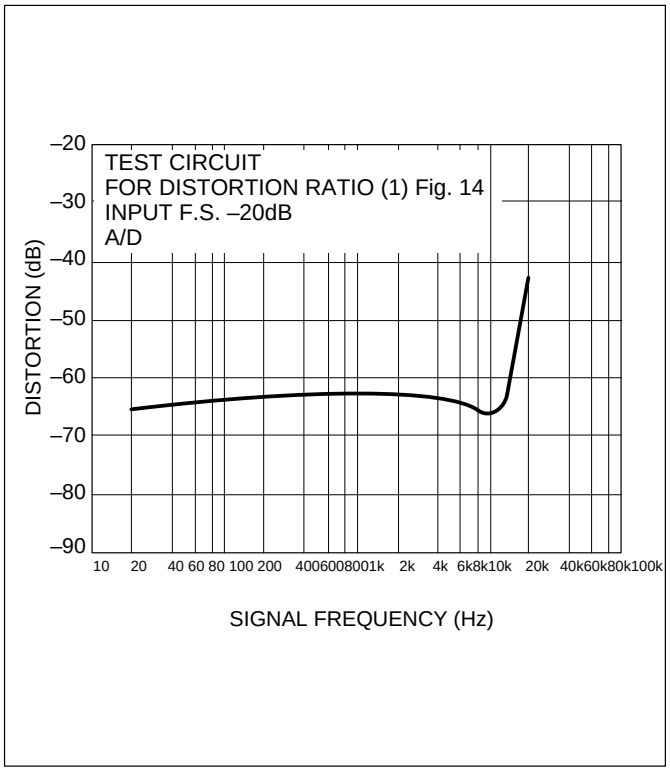


Figure 23. Signal Frequency vs. Distortion Ratio

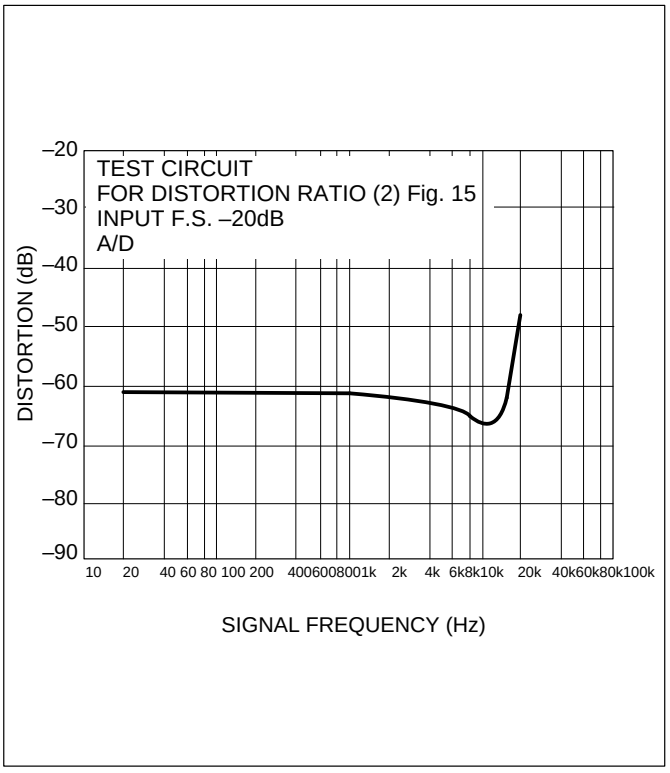


Figure 24. Signal Frequency vs. Distortion

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

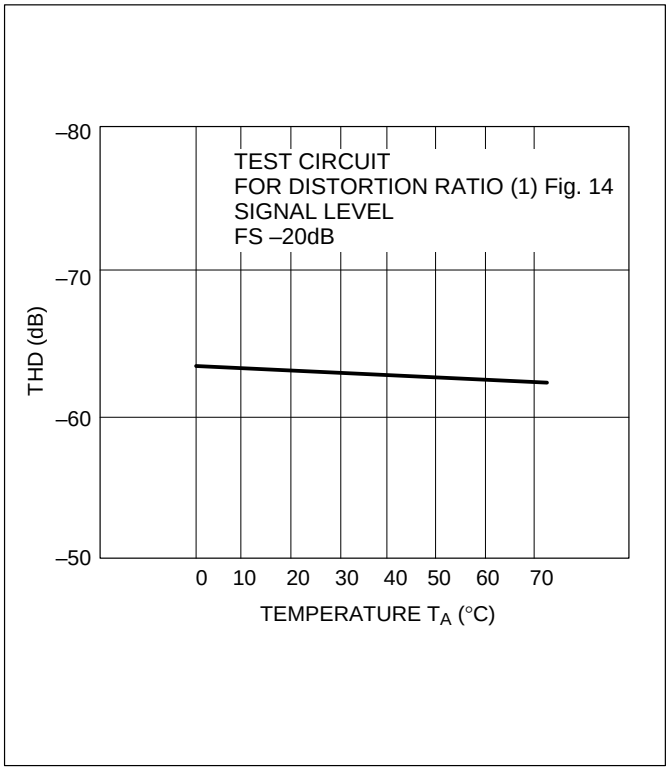


Figure 25. Temperature vs. Distortion Ratio (A/D Mode)

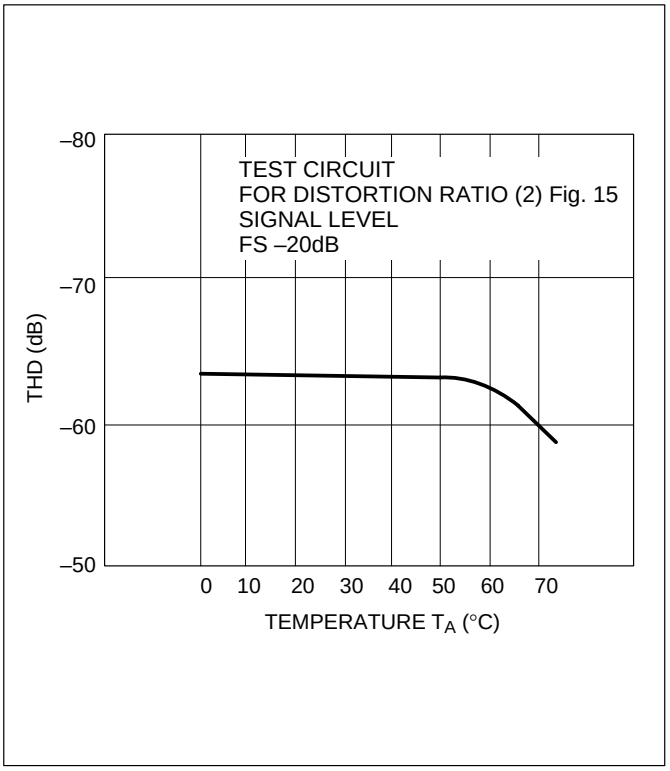


Figure 26. Temperature vs. Distortion Ratio (D/A Mode)

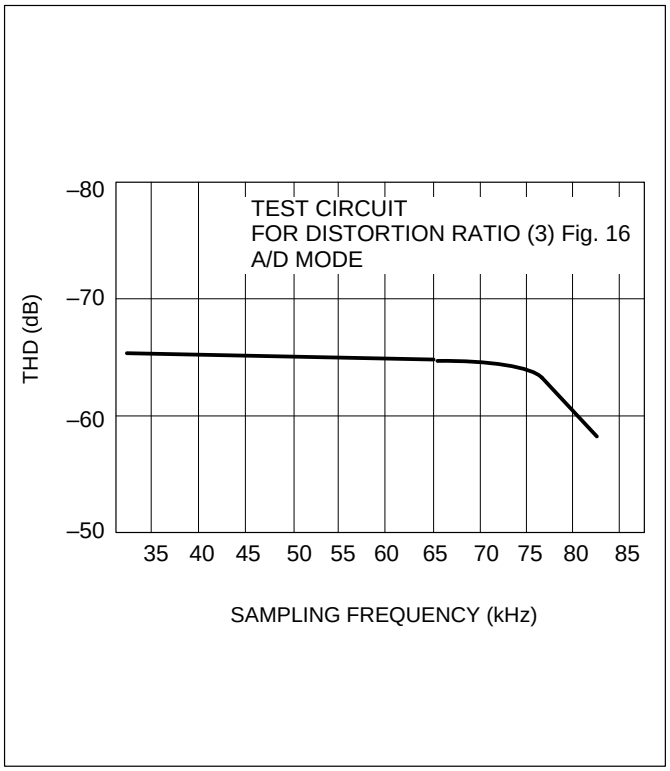


Figure 27. Sampling Frequency vs. Distortion Ratio

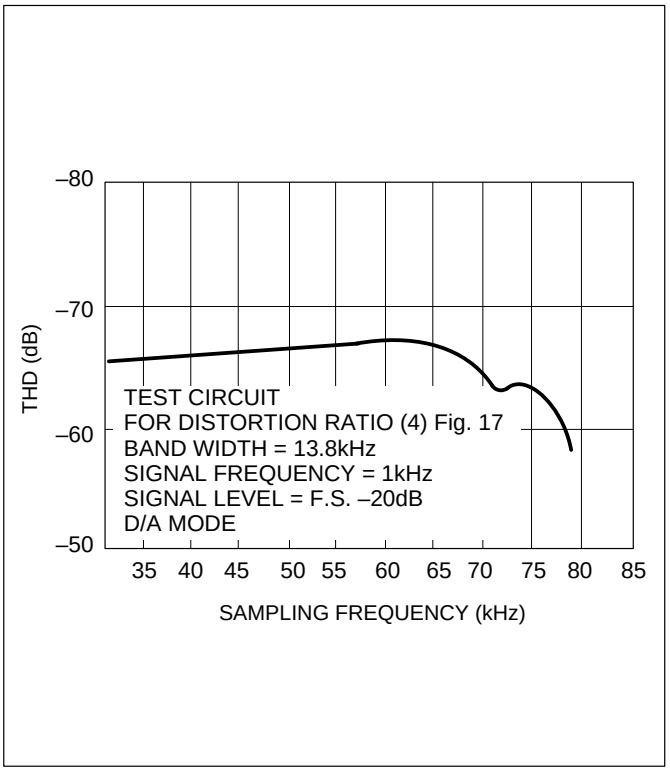


Figure 28. Sampling Frequency vs. Distortion Ratio

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

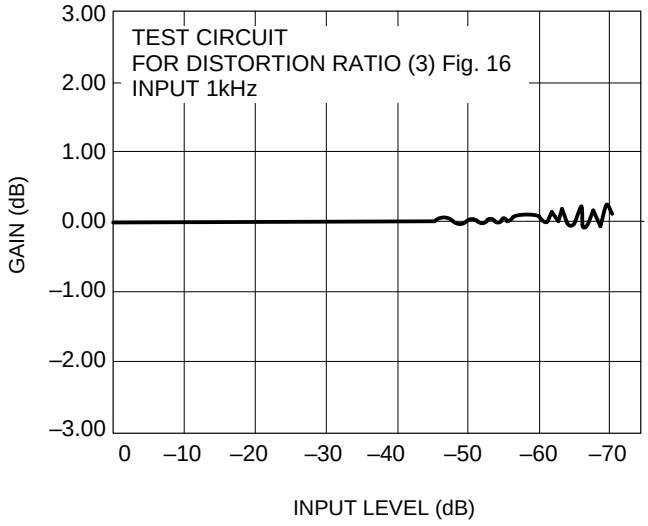


Figure 29. Input Level vs. Gain

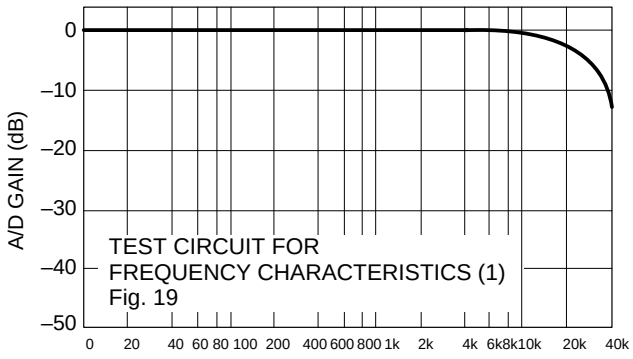


Figure 30. Signal Frequency vs. Gain

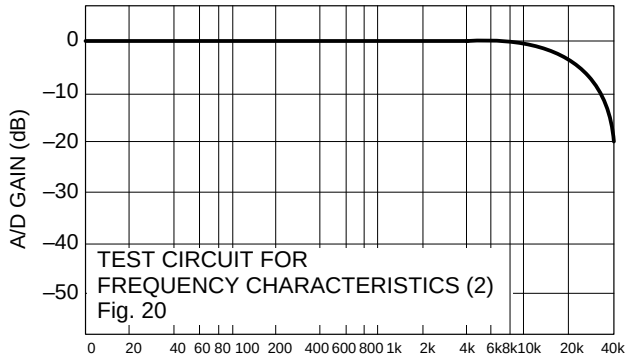
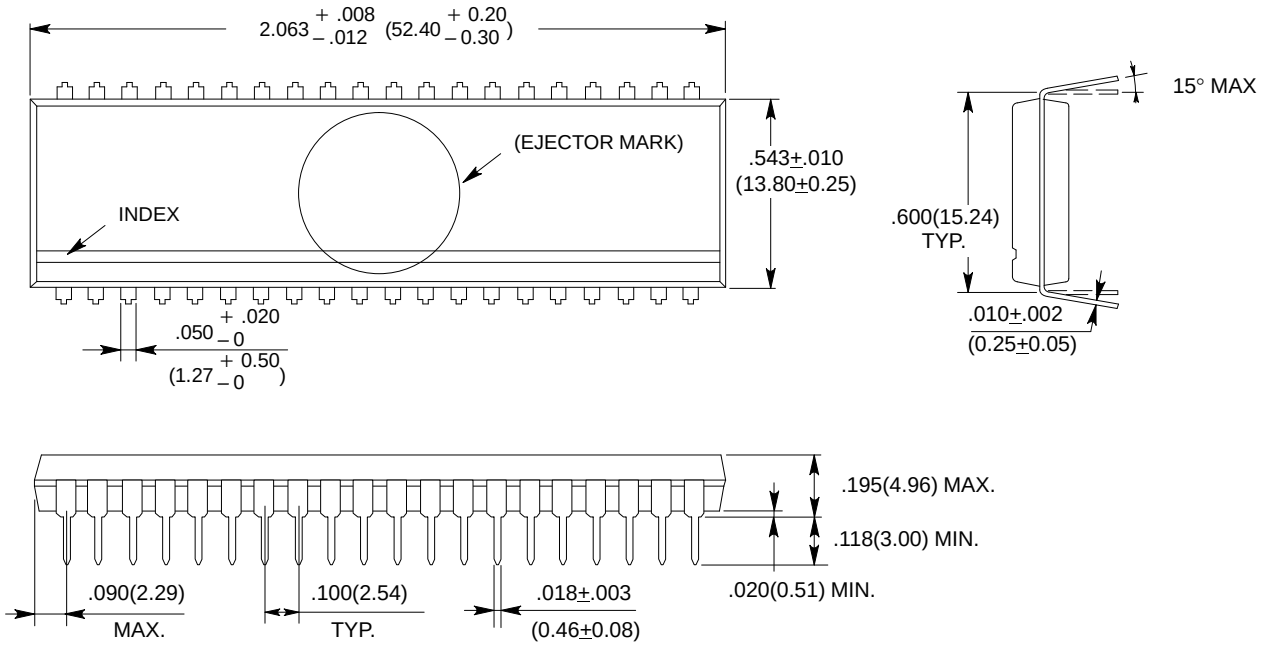


Figure 31. Signal Frequency vs. Gain

PACKAGE DIMENSIONS

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40P-M01)



Dimensions in
inches (millimeters).

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