DS04-21334-1E

FUJITSU

DATA SHEET

ASSP
Dual Serial Input
PLL Frequency Synthesizer
MB15F03

■ DESCRIPTION

The Fujitsu MB15F03 is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2.0GHz and a 500MHz prescalers. A 64/65 or a 128/129 for the 2.0GHz prescaler, and a 16/17 or a 32/33 for 500MHz prescaler can be selected that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 9.0mA typ. at a supply voltage of 3.0V.

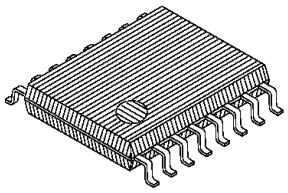
Furthermore, a super charger circuit is included to provide a fast tuning as well as low noise performance. As a result of this, MB15F03 is ideally suitable for digital mobile communications, such as PHS(Personal Handy Phone System), PCN (Personal Communication Network) and PCS(Personal Communication Service).

■ FEATURES

- High frequency operation RF synthesizer : 2.0GHz max.
  IF synthesizer : 500MHz max.
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current : I_{CC} = 9.0 mA typ. (Vcc = 3V)
- Power saving function : I_{PS1} = I_{PS2} = 10 µA max.
- Serial input 14–bit programmable reference divider: R = 5 to 16,383
- Serial input 18–bit programmable divider consisting of:
  - Binary 7–bit swallow counter: 0 to 127
  - Binary 11–bit programmable counter: 5 to 2,047
- On–chip high performance charge pump circuit and phase comparator, achieving high–speed lock–up and low phase noise
- Wide operating temperature: Ta = –40 to 85°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

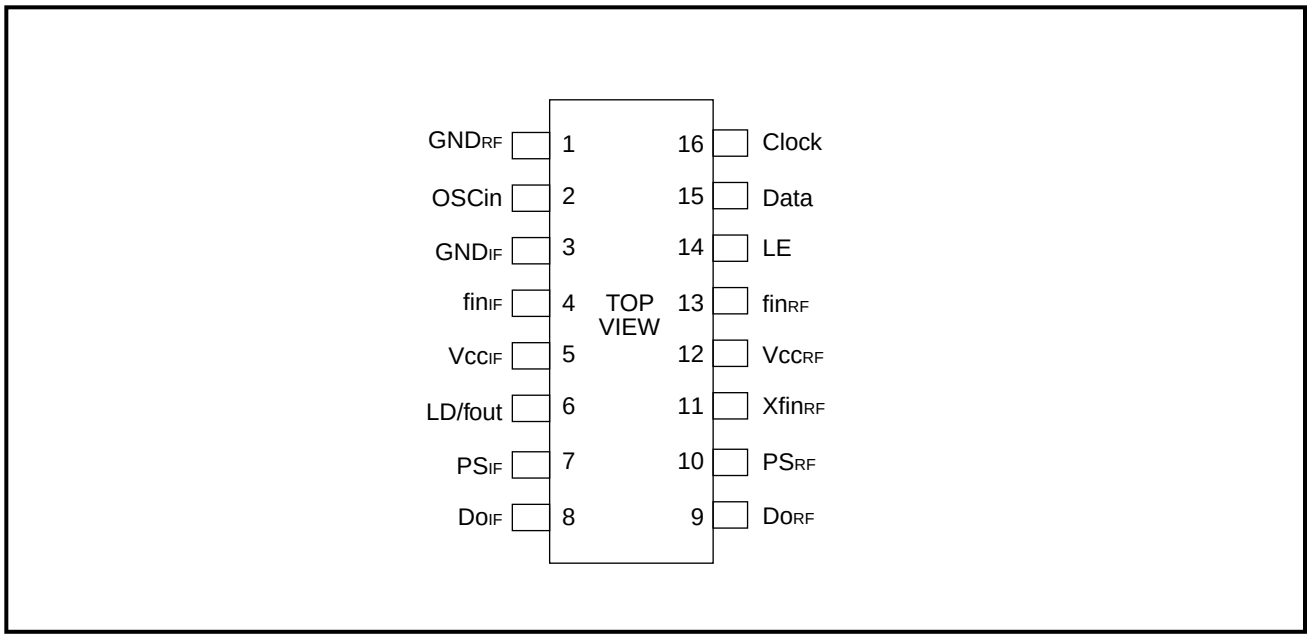
■ PACKAGE

16-pin, Plastic SSOP



(FPT-16P-M05)

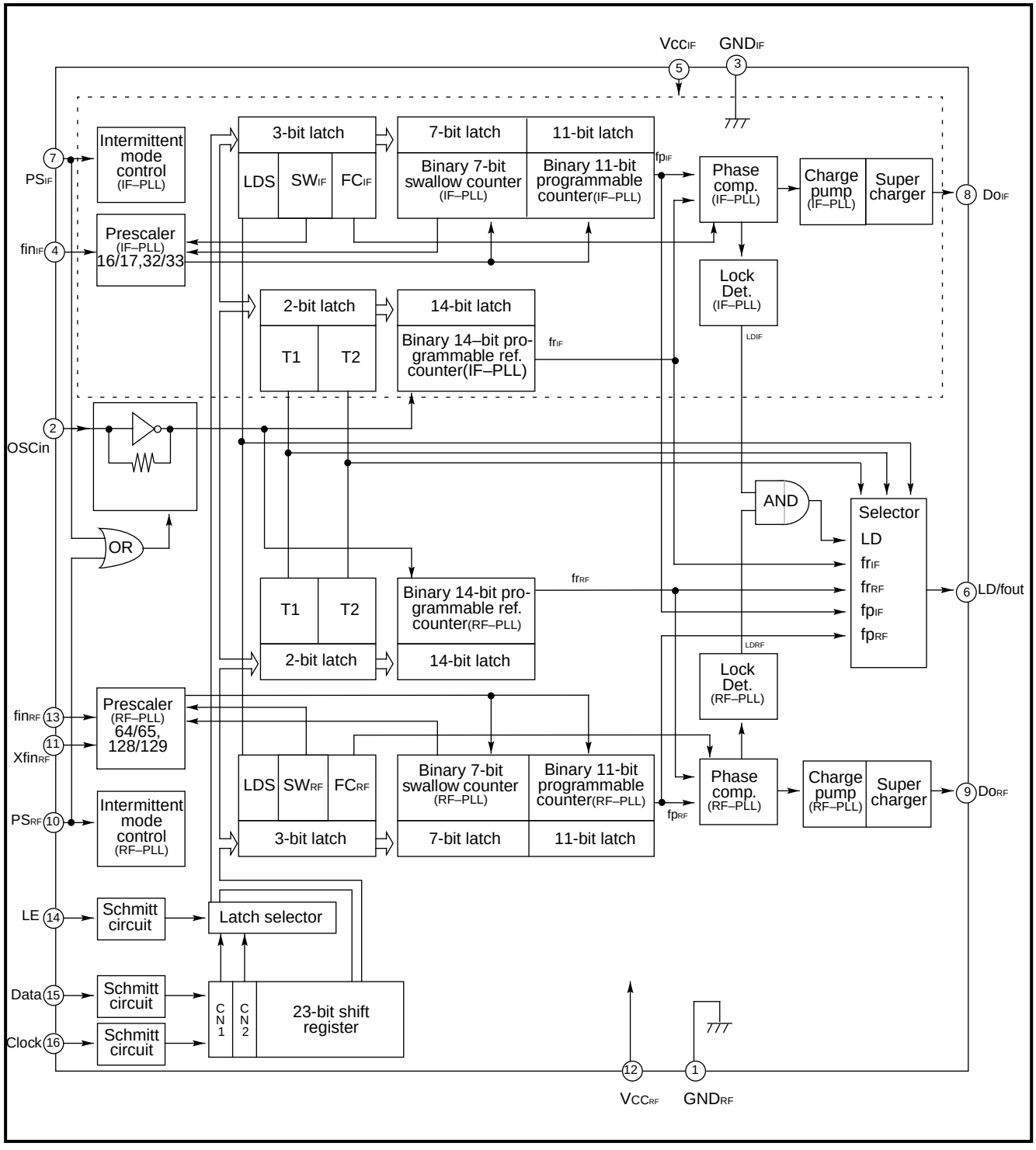
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	I/O	Descriptions
1	GND_{RF}	–	Ground for RF–PLL section.
2	OSCin	I	The programmable reference divider input. TCXO should be connected with a coupling capacitor.
3	GND_{IF}	–	Ground for the IF-PLL section.
4	fin_{IF}	I	Prescaler input pin for the IF-PLL. The connection with VCO should be AC coupling.
5	Vcc_{IF}	–	Power supply voltage input pin for the IF-PLL section. When power is OFF, latched data of IF-PLL is cancelled.
6	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout) The output signal is selected by a LDS bit in a serial data. LDS bit = ”H” ; outputs fout signal LDS bit = ”L” ; outputs LD signal
7	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at ”L” Power-ON. (Open is prohibited.) PS_{IF} = ”H” ; Normal mode PS_{IF} = ”L” ; Power saving mode
8	Do_{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
9	Do_{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
10	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at ”L” Power-ON. (Open is prohibited.) PS_{RF} = ”H” ; Normal mode PS_{RF} = ”L” ; Power saving mode
11	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
12	Vcc_{RF}	–	Power supply voltage input pin for the RF-PLL section, the shift register and the oscillator input buffer. When power is OFF, latched data of RF-PLL is cancelled.
13	fin_{RF}	I	Prescaler input pin for the RF-PLL. The connection with VCO should be AC coupling.
14	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is ”H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
15	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-Prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
16	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a riging edge of the clock.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	–0.5 to +4.0	V	
Input voltage	V_I	–0.5 to V_{CC} +0.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Storage temperature	T_{STG}	–55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	$V_{CCIF} = V_{CCRF}$
Input voltage	V_i	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current*1		I_{CCIF}	fin_{IF} = 500MHz, fosc = 12MHz	–	3.0	–	mA
		I_{CCRF}	fin_{RF} = 2000MHz, fosc = 12MHz	–	6.0	–	
Power saving current		I_{PSIF}	Vcc_{IF} current at PS_{IF} ="L"	–	–	10	µA
		I_{PSRF}	Vcc_{RF} current at $PS_{IF/RF}$ ="L"	–	–	10	
Operating frequency	fin_{IF}	fin_{IF}	IF–PLL	50	–	500	MHz
	fin_{RF}	fin_{RF}	RF–PLL	100	–	2000	
	OSCin	f_{OSC}	min. 500mVp-p	3	–	40	
Input sensitivity	fin_{IF}	$Vfin_{IF}$	IF–PLL, 50Ω termination	–10	–	+2	dBm
	fin_{RF}	$Vfin_{RF}$	RF–PLL, 50Ω termination	–10	–	+2	dBm
	OSCin	V_{OSC}		500	–	V_{CC}	mVp-p
Input voltage	Data, Clock, LE	V_{IH}	Schmitt trigger input	V_{CC}x0.7+ 0.4	–		V
		V_{IL}	Schmitt trigger input	–	–	V_{CC}x0.3– 0.4	
	PS_{IF}, PS_{RF}	V_{IH}		V_{CC}x0.7	–		V
		V_{IL}		–	–	V_{CC}x0.3	
Input current	Data, Clock, LE, PS_{IF}, PS_{RF}	I_{IH}		–1.0		+1.0	µA
		I_{IL}		–1.0	–	+1.0	
	OSCin	I_{IH}		0	–	+100	µA
		I_{IL}		–100	–	0	
Output voltage	LD/fout	V_{OH}		V_{CC}–0.4	–		V
		V_{OL}		–	–	0.4	
	Do_{IF}, Do_{RF}	V_{DOH}		V_{CC}–0.4	–		V
		V_{DOL}		–	–	0.4	
High impedance cutoff current	Do_{IF}, Do_{RF}	I_{OFF}		–	–	1.1	µA
Output current	LD/fout	I_{OH}	Vcc = 3.0V	–	–	–1.0	mA
		I_{OL}	Vcc = 3.0V	1.0	–	–	
	Do_{IF}, Do_{RF}	I_{DOH}	Vcc = 3.0V, V_{DOH} = 2.0V	–	–6.0*2	–	mA
		I_{DOL}	Vcc = 3.0V, V_{DOL} = 1.0V	–	–10.0*2	–	

*1: Conditions ; $Vcc_{IF/RF}$ = 3V, Ta = 25°C, in locking state.

*2: Conditions ; Ta = 25°C

■ FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)
P: Preset divide ratio of dual modulus prescaler (16 or 32 for IF-PLL, 64 or 128 for RF-PLL)
N: Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC}: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF–PLL sections, programmable reference dividers of IF/RF PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table1. Control Bit

Control bit		Destination of serial data
CN1	CN2	
L	L	The programmable reference counter for the IF-PLL.
H	L	The programmable reference counter for the RF-PLL.
L	H	The programmable counter and the swallow counter for the IF-PLL
H	H	The programmable counter and the swallow counter for the RF-PLL

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

CNT1, 2 : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bits for the programmable reference counter (5 to 16,383) [Table. 2]
T1, 2 : Test purpose bit [Table. 3]
NOTE: Data input with MSB first.

Programmable Counter

LSB ← Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT1, 2 : Control bit [Table. 1]

N1 to N14 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 4]

A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 5]

SW : Divide ratio setting bit for the prescaler (16/17 or 32/33 for the IF-PLL, 64/65 OR 128/129 for the RF-PLL) [Table. 6]

FC : Phase control bit for the phase detector [Table. 7]

LDS : LD/fout signal select bit [Table. 8]

NOTE: Data input with MSB first.

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 Test Purpose Bit Setting

T 1	T 2	LD/fout pin state
L	L	Outputs $fr_{IF.}$
H	L	Outputs $fr_{RF.}$
L	H	Outputs $fp_{IF.}$
H	H	Outputs $fp_{RF.}$

Table.4 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.5 Binary 7-bit Swallow Counter Data Setting

Divide ratio (N)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table. 6 Prescaler Data Setting

		SW = ”H”	SW = ”L”
Prescaler divide ratio	**IF-PLL**	16/17	32/33
	RF-PLL	64/65	128/129

Table. 7 Phase Comparator Phase Switching Data Setting

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	¨	

Note: • Z = High–impedance
• Depending upon the VCO and LPF polarity, FC bit should be set.

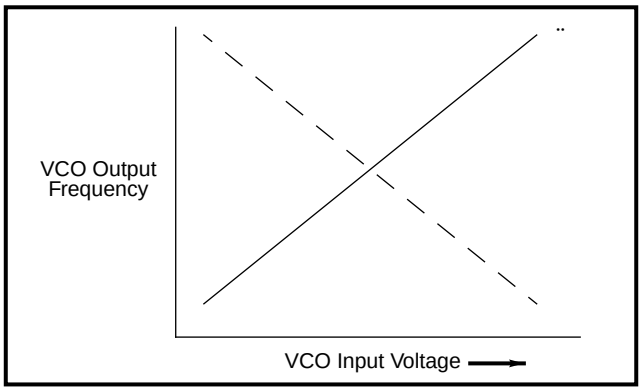
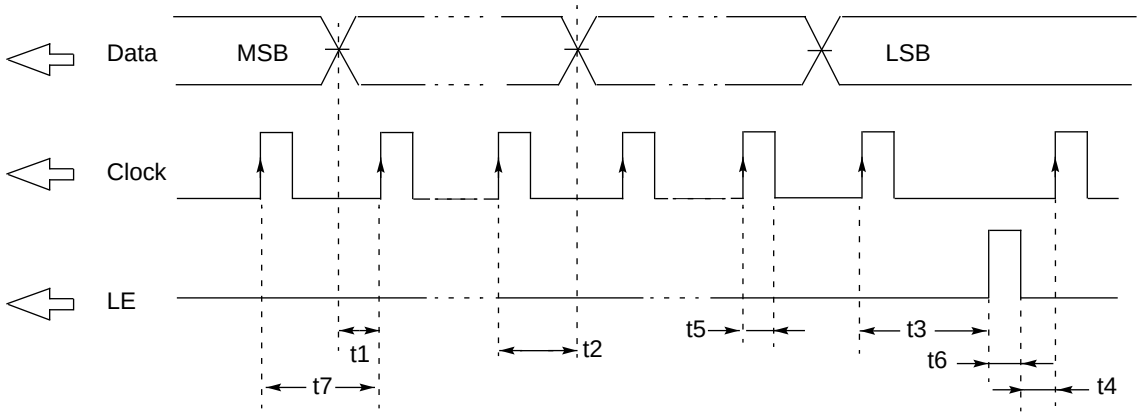


Table. 8 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout ($fr_{IF/RF}$, $fp_{IF/RF}$) signals
L	LD signal

Serial Data Input Timing

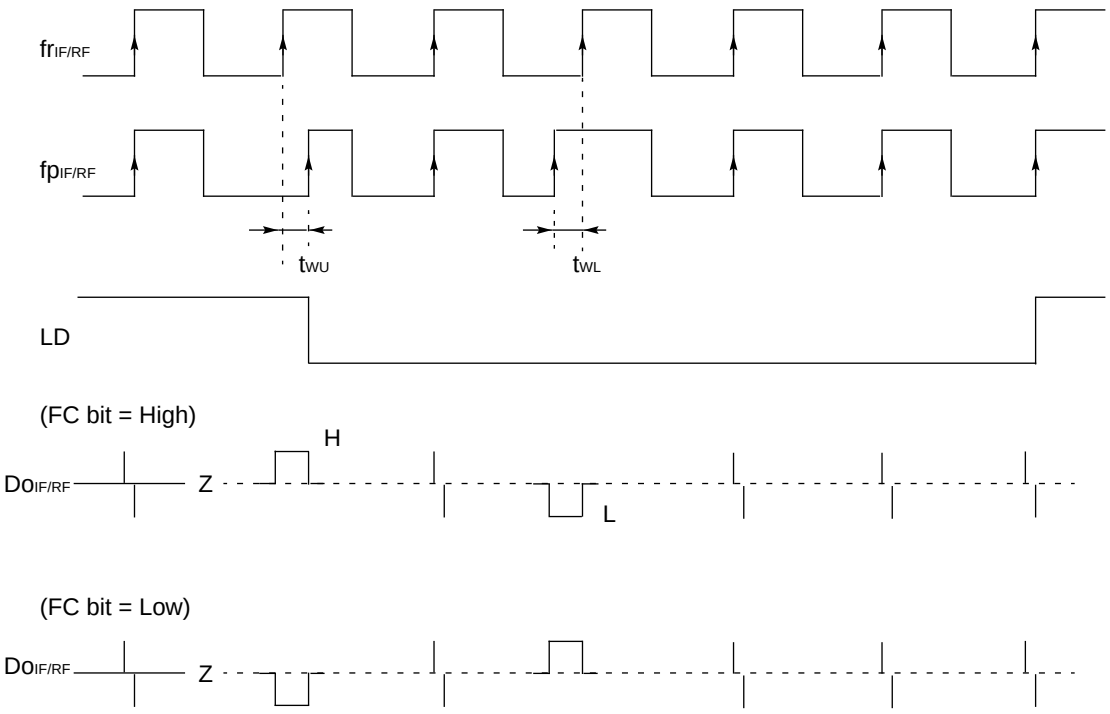


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min	Typ	Max	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	20	–	–	ns

Parameter	Min	Typ	Max	Unit
t5	30	–	–	ns
t6	100	–	–	ns
t7	100	–	–	ns

■ PHASE DETECTOR OUTPUT WAVEFORM



LD Output Logic Table

IF–PLL section	RF–PLL section	LD output
Locking state / Power saving state	Locking state / Power saving state	H
Locking state / Power saving state	Unlocking state	L
Unlocking state	Locking state / Power saving state	L
Unlocking state	Unlocking state	L

Note:
- Phase error detection range = -2π to $+2\pi$
- Pulses on $Do_{IF/RF}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSCin input frequency as follows.
  $t_{WU} \geq 8/fosc$: i.e. $t_{WU} \geq 625ns$ when foscin = 12.8 MHz
  $t_{WL} \leq 16/fosc$: i.e. $t_{WL} \leq 1250ns$ when foscin = 12.8 MHz

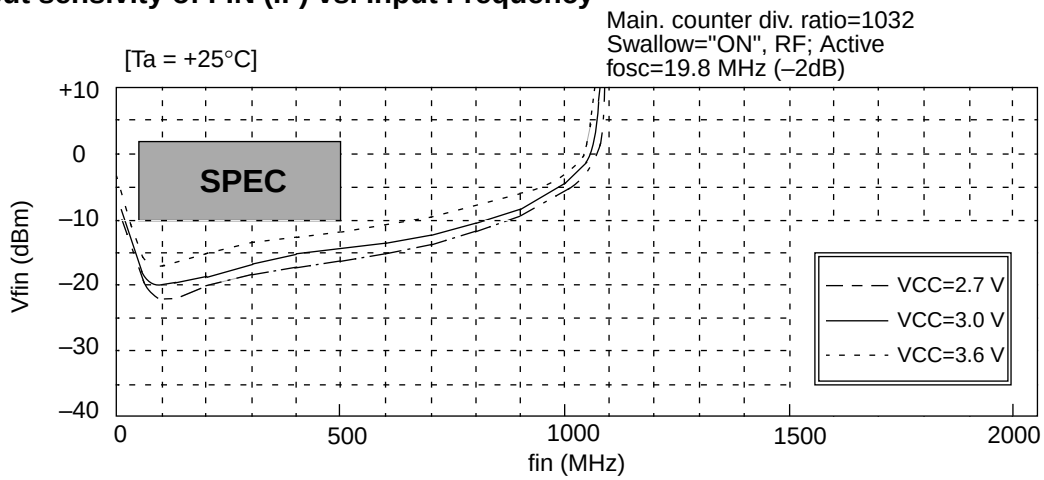
■ POWER SAVING MODE (Intermittent Mode Control Circuit)

Setting a $PS_{IF(RF)}$ pin to Low, IF-PLL (RF-PLL) enters into power saving mode resultant current consumption can be limited to 10μA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally. In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (fr) and comparison frequency (fp) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up. Thus keeping the loop locked.
PS pin must be set "L" at Power-ON.
Allow 1 μs after frequency stabilization on power-up for exiting the power saving mode (PS: L to H)
Serial data can be entered during the power saving mode.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF's time constant. As a result of this, VCO's frequency is kept at the locking frequency.

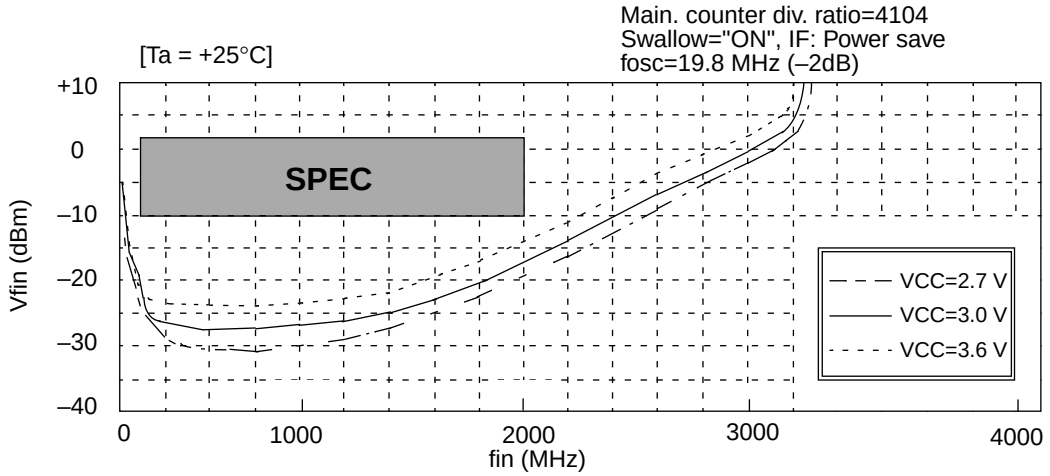
PS_{IF}	PS_{RF}	IF-PLL counters	RF-PLL counters	OSC input buffer
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON

■ TYPICAL CHARACTERISTICS

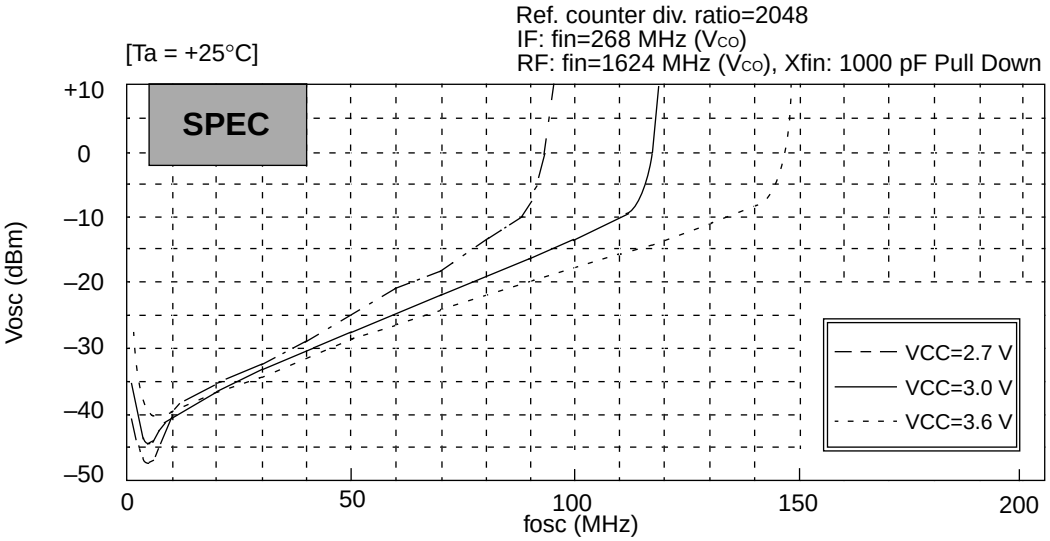
Input sensivity of FIN (IF) vs. Input Frequency



Input sensivity of FIN (RF) vs. Input Frequency



Input sensivity of OSC vs. Input Frequency



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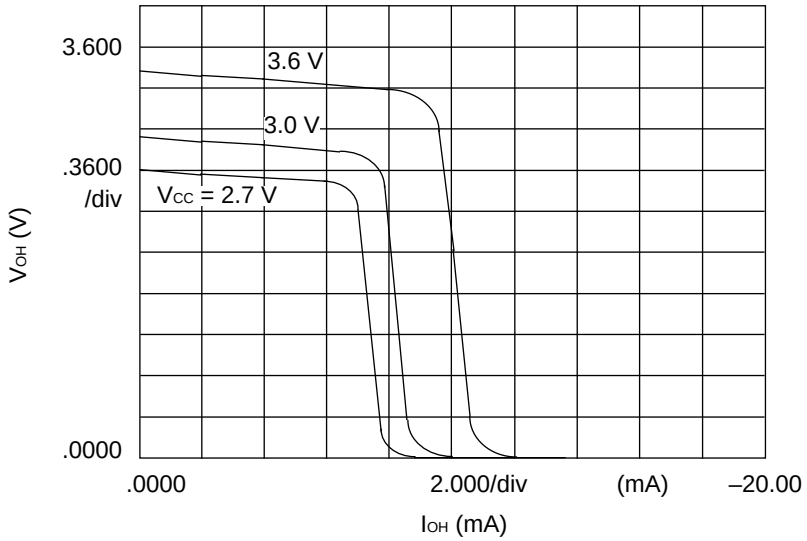
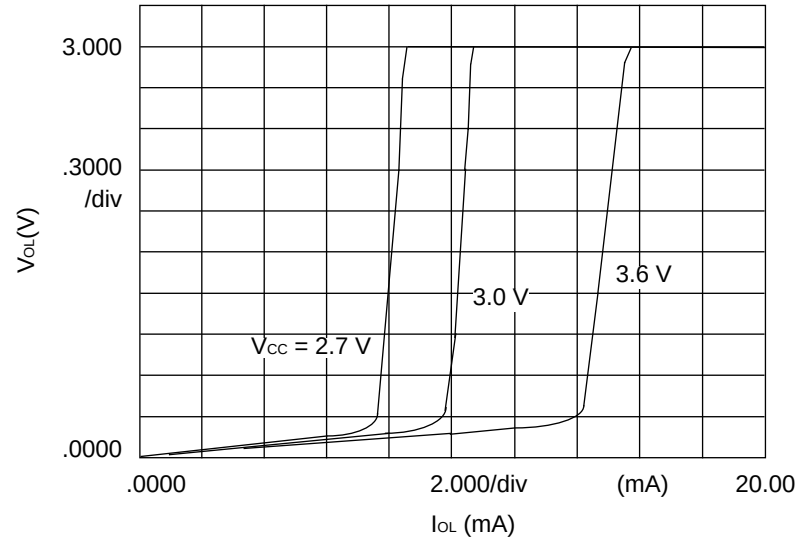
Do output Current

Conditions: Ta = +25°C
V_{CC}= 2.7, 3.0, 3.6 V





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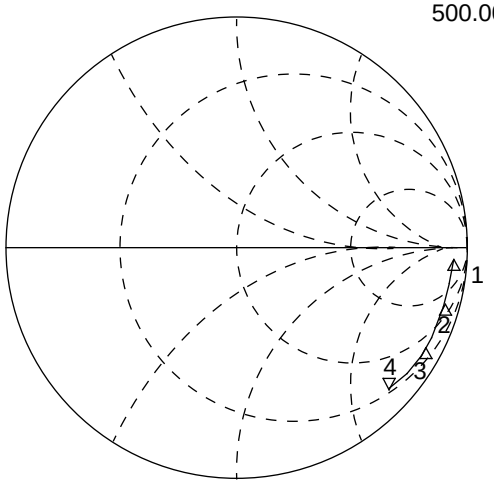
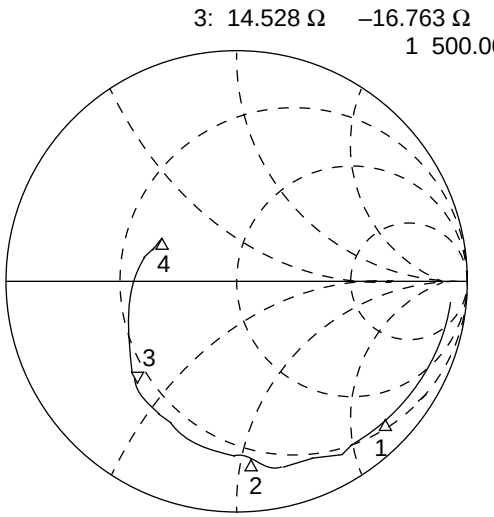
Input Impedance

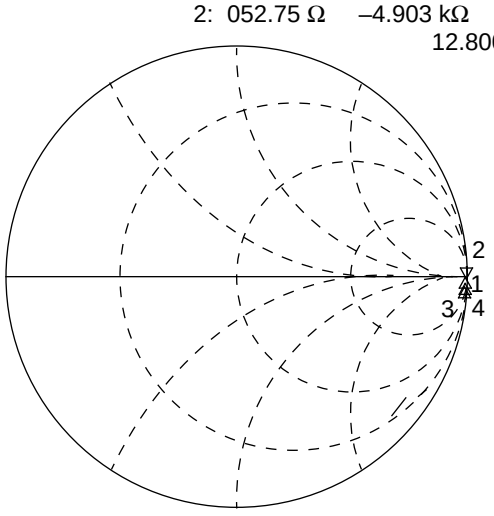
fin_{IF} Pin



fin_{RF} Pin



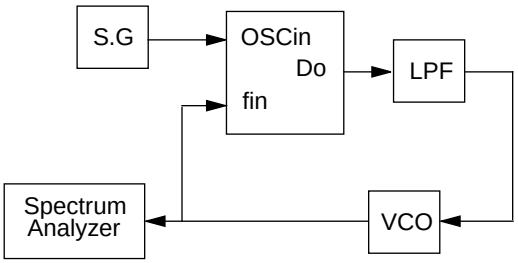
OSCin Pin



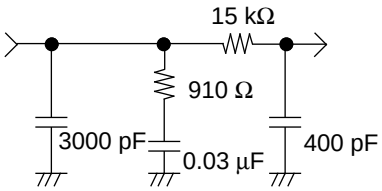
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise and reference leakage.

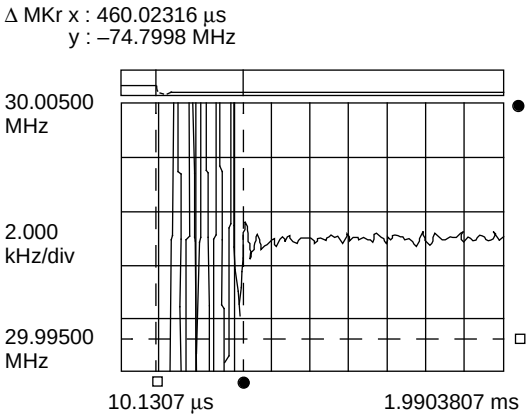
Test Circuit

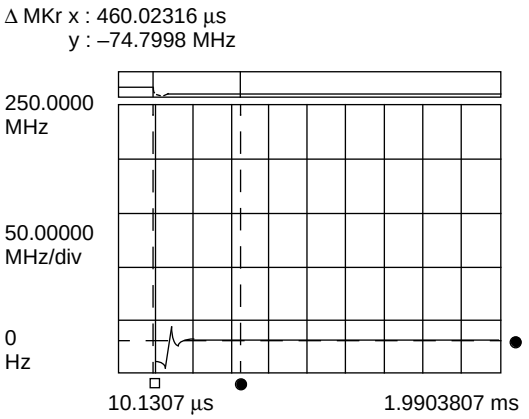


- fvco = 1835 MHz
- Kv = 87 MHz/v
- fr = 200 kHz
- fosc = 13 MHz
- LPF:

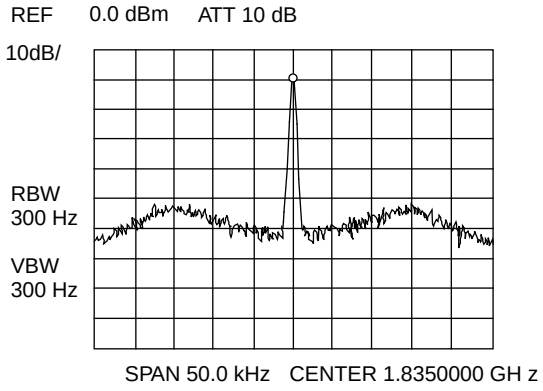


PLL Lock Up Time = 460 µs
(1797.6 MHz → 1872.4 MHz, within ± 1kHz)

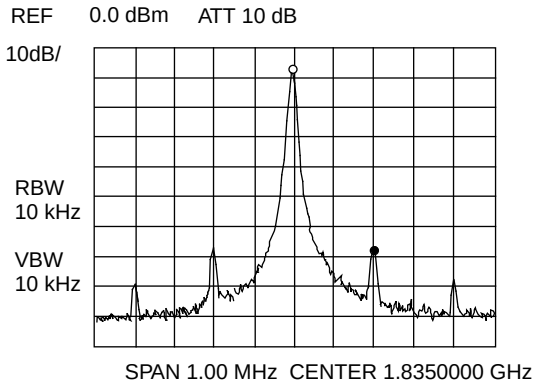




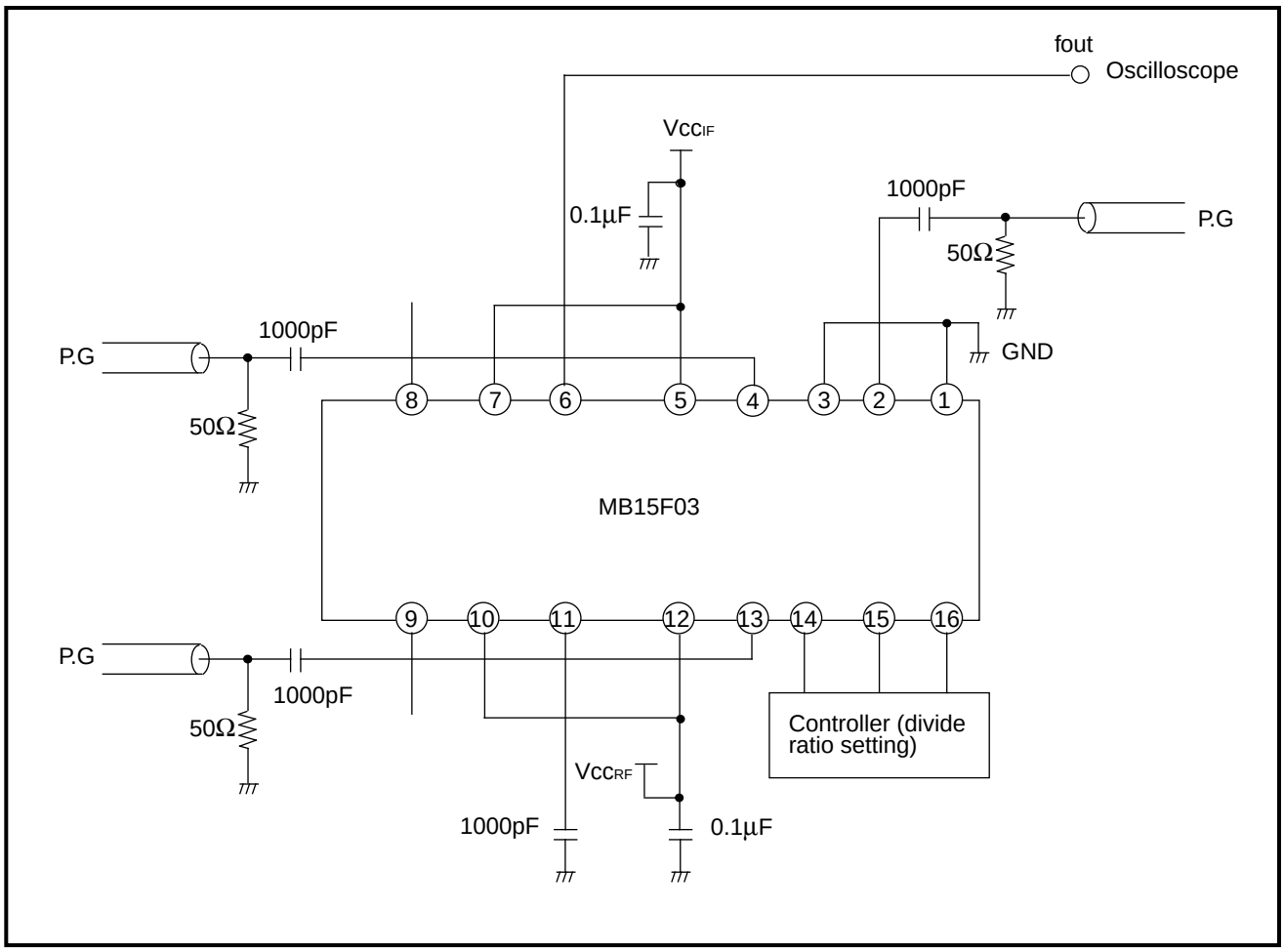
PLL Phase Noise
@ within loop band = 70.1 dBc/Hz



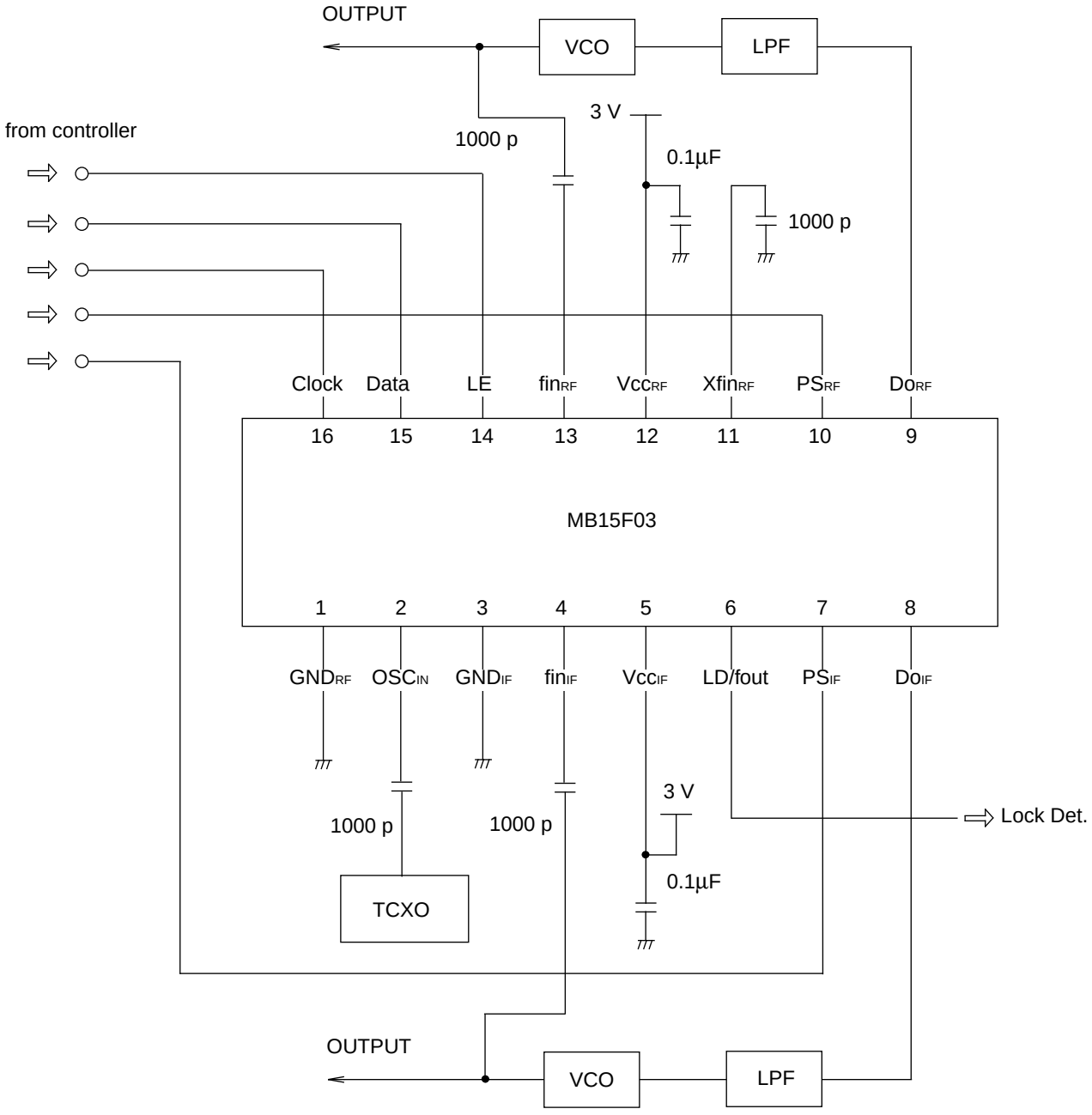
PLL Reference Leakage
@ 200 kHz offset = 59 dBc



■ TEST CIRCUIT (Prescaler Input/Programmable Reference Divider Input Sensitivity Test)



■ APPLICATION EXAMPLE

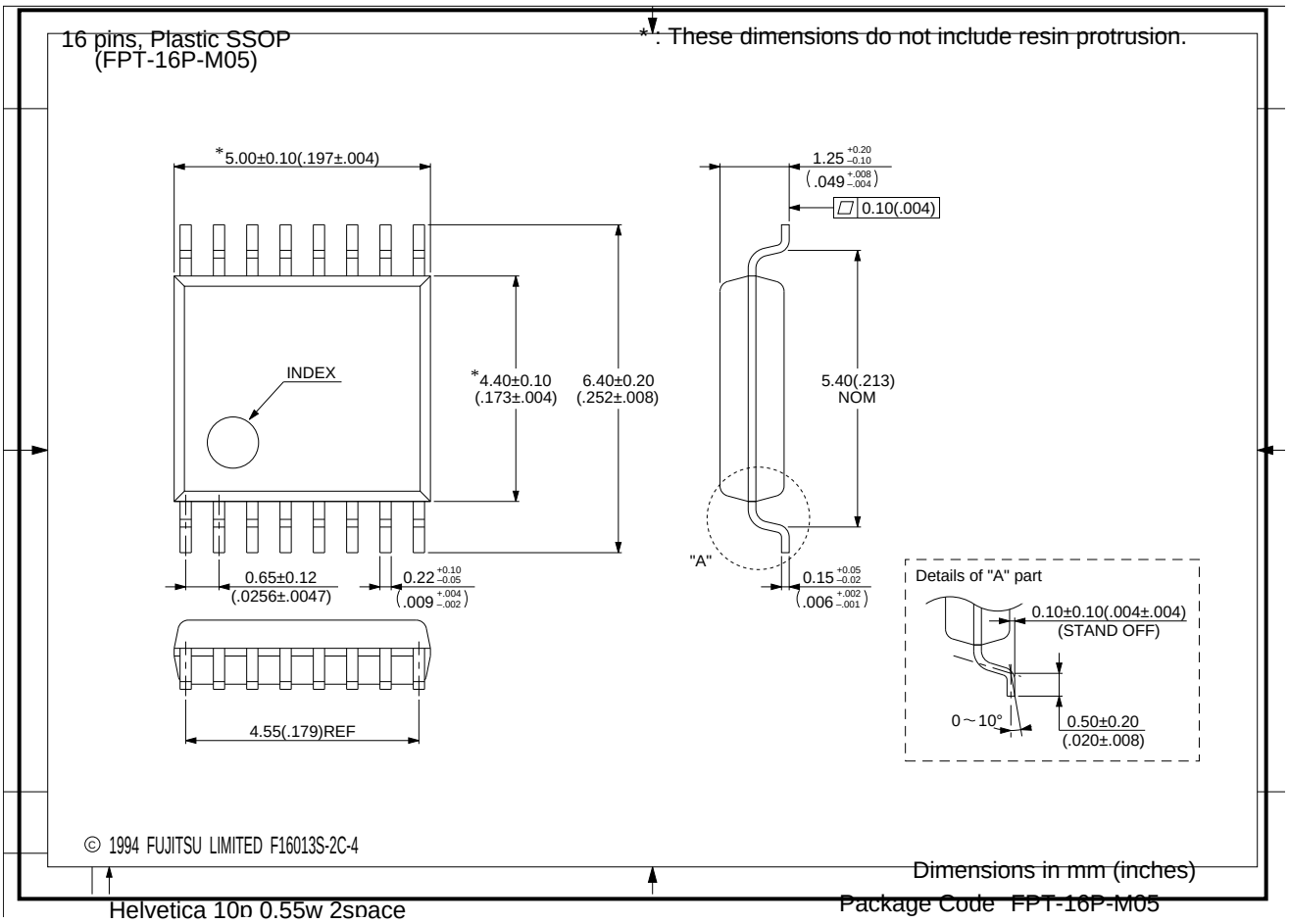


Clock, Data, LE: Schmitt trigger circuit is provided (insert a pull-down or pull-up resistor to prevent oscillation when open-circuited in the input).

■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F03 PFV	16pin, Plastic SSOP (FPT-16P-M05)	

■ PACKAGE DIMENSION



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