FUJITSU

Plasma Display Data Book

1993 – 1994
Data
Book

Fujitsu Microelectronics, Inc.
San Jose, California, U.S.A.

This document is published by the Technical Communications Department, Fujitsu Microelectronics, Inc. 3545 North First Street, San Jose, California, U.S.A. 95134–1804; U.S.A.

Printed in the U.S.A.

Edition 1.0

Section 1

Plasma Display Introduction — *At a Glance*

Fujitsu Plasma Display Product

Introduction

Fujitsu Limited, Japan, began research and development for flat panel displays in 1965 and has been mass producing them since 1972. Today, with over 100,000 high–information content displays shipped annually, the Company is the largest worldwide commercial supplier of AC–memory plasma displays. Fujitsu Microelectronics, Incorporated, Electronic Components Division, located in San Jose, California, functions as the marketing arm for the Company's Plasma Display Panels (PDPs) in the United States, Canada, and South America.

Fujitsu chose to focus its efforts on AC–Memory plasma display technology because the resulting panels thin profile, light weight, graphics generation capability and crisp readability best address the future of display technology – high–definition television. Today, Fujitsu Plasma Displays are found in a variety of applications from financial transactions displays (ATMs, POS terminals) and medical instrumentation to factory automation equipment and computer workstations. This wide–range usage is due largely to the panels high reliability and large capacity, coupled with brightness and high contrast. Furthermore, AC–Memory plasma displays employ a non–scanning technology and are inherently immune to electromagnetic interference. These features make them well suited for use in equipment that operates where electromagnetic fields (EMI) are present. Examples of such EMI–Resistant applications include aluminum and steel mills, electrical control rooms, and magnetic resonance medical equipment.

AC–Memory Technology

Plasma display panels are unique from other display technologies because they are powered by emissions generated by a gas discharge. The PDP consists of two glass substrates, each containing an array of electrodes. These substrates are arranged so that the two electrode arrays (X and Y) face each other, separated by a 0.1 mm gap. After the periphery of the substrate assembly is hermetically sealed, neon gas is pumped in. Discharge between the electrodes occurs when 100 to 200 volts as applied to specific X and Y electrodes, causing the neon gas to emit the panel's characteristic orange light.

Types of Panels

Plasma display panels are available as numeric displays, where the electrodes are fixed in an 8–segment configuration, or as graphics displays, where stripe matrix–addressed electrodes cross each other at right angles to form a pixel.

There are two types of plasma displays, classified by panel structure: The DC type, where the electrodes are exposed, and the AC type, where the electrodes are covered by protective insulating layers.

The DC PDP requires lower driving voltage, but its brightness eventually decreases over time due to the lack of an insulating layer to prevent electrode deterioration at the time of discharge. Sometimes the compound Mercury is used as a gas stabilizer inside the panel which presents a health concern. The DC panel also requires a preliminary discharge which brightens surrounding dots and results in the deterioration of display contrast. Furthermore,, its intensity decreases markedly as the number of horizontal scan lines increases (Figure 1).

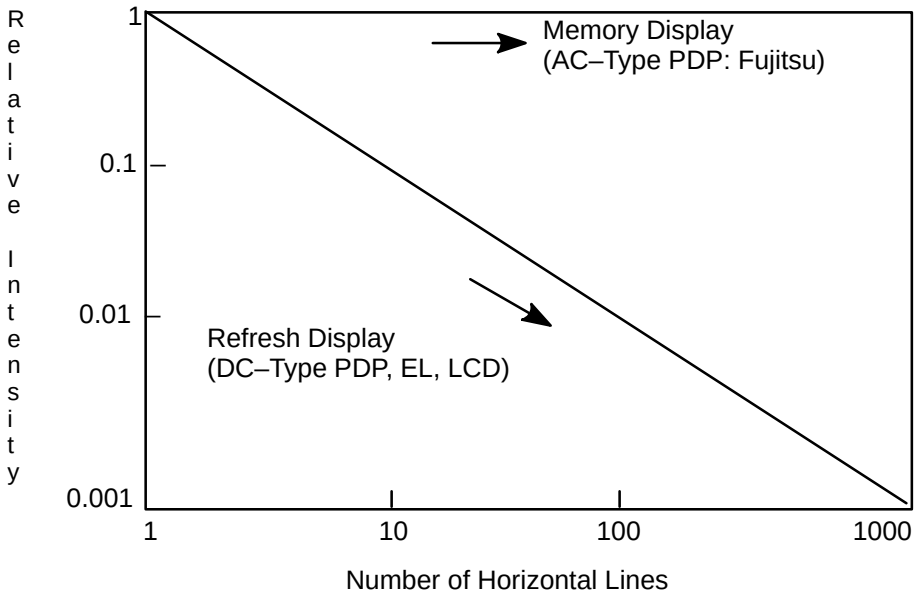


Figure 1 Brightness Comparison Between Memory and Refresh Display

With AC PDs, the protective Magnesium Oxide Layer insulates the electrodes and prevents deterioration of the of the display brightness level. In addition, the panel memory function stores the electric charge generated at the time of discharge in the protective layer surface. This allows the panel to continue displaying one line even while another is being modified. In effect, once a pixel is lit, it stays lit until another signal turns it off. Therefore, an increased number of scanning lines enables the panel to display a great volumn of data over a large surface area with uniform intensity without sacrificing panel brightness.

High Information Content Displays

Fujitsu began manufacturing ultra–high information PDPs in 1989. To respond to the demand for smaller and lighter displays with improved performance for the personal computer and workstation markets. Ultra–high information content displays are characterized as those with 1024 X 768, 1024 X 816, and 1280 X 1024 resolutions.

To keep panel thickness to a minimum, Fujitsu uses a 40V voltage resistant 64–bit LSI to drive the 1024 electrodes. As a result, its standalone 1024 X 768 PDP has a depth of 9cm (3.5”) weights 5kg (11 lbs), and requires only an AC100V to 120V input. While the panel’s physical size is impressive, the technology needed to produce it presents some manufacturing challenges.

For example, compared to an LCD display, the PDP requires a higher driving voltage, which increases the driver circuitry cost. In order to reduce the number of drive circuits and bring PDP cost in line with other flat panel technologies used in PC and workstation applications, Fujitsu developed the float–electrode system and low–voltage drive technology.

Reduction of Drive Circuits

Using the float–electrode (capacitance matrix) method, electrodes are scanned in an interlaced pattern to reduce the total number of high–voltage driver ICs. Two capacitors are situated at each end of each row of display electrodes inside the glass substrate (Figure 2). Though these capacitors, two sets of drive electrodes are wired into the matrix.

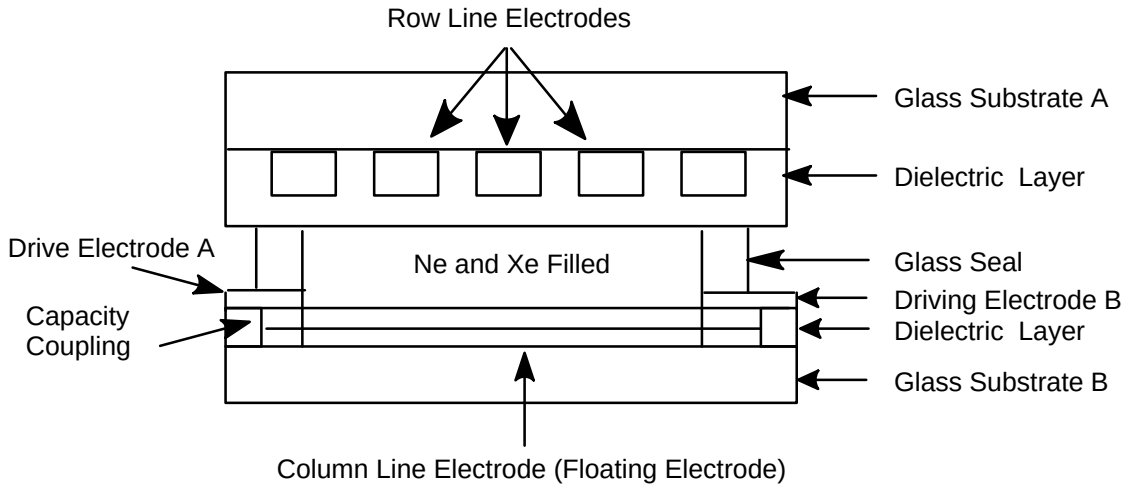


Figure 2 Cross Section of Plasma Display Panel Using Float Electrode Method

When two sets of drive electrodes are combined (voltage is applied), the row display electrode (with both sides of the drive electrodes) reaches selective potential (high voltage) and other display electrodes become half–selective (1/2 of applied voltage) or non–selective (zero voltage).

If a voltage waveform sequence selects the application of voltage to display cells only at the intersection of the column electrodes and the high voltage row display electrodes, multiple driving of the row electrode occurs. For example, when a row electrode with 400 lines is driven in a matrix of 20 X 20, row lines of row electrodes are selected and riven in 40 drive circuits. In this manner, the number of row electrode drive circuits is reduced to that of conventional circuits. The advantages are: 1) less power is needed to drive fewer circuits; and, 2) a thinner panel profile.

Pursuit of Low Voltage

The specific features of AC memory drive circuitry also contribute to obtaining low drive voltage. After lighting all the dots on one row electrode, simultaneous application of an erase voltage pulse to the row electrode and erase cancel electrode enables selective cancellation with low voltage. This erase cancel address method reduce drive voltage from 100V to 30V and creates highly integrated, miniaturized drive LSIs at a lower cost..

Grey–Scale Display

Fujitsu also developed gray–scale display technologies that utilize multiple gradation application software. DC PDPs achieve gradation display by using pulse duration modulation, which varies the discharging time. With AC PDPs, graduation is obtained by frequency modulation, which varies the number of discharges.

For example, with four–level grey scale, a small number of discharges (which produce low brightness) and a large number of discharges (which produce high brightness) are displayed alternatively on two display screens at a high speed. This combination produce for levels of brightness. Displaying one frame on three screens with different brightness produces eight gradations, and on four screens; 16 gradations.

In PDP graduation, the gray scale level is stable and the display brightness is proportional to the number of discharges. In either the pulse duration modulation or frequency modulation method, more than 64 gradations are theoretically possible. However, a newly developed drive method technology for Ac multigradation eliminates the need for frame memory.

VGA Compatibility: Ease of Design

While modifications in panel design have enhanced the use of plasma displays in PC and workstation environments, VGA compatibility and design–in time are other important factors. Since CRTs and the flat panels don't communicate with the host system in exactly the same way, each requires its own semi–custom, flat panel display controller card. Fujitsu eliminates the problem and reduces the video subsystem cost by making its displays compatible with readily available standard VGA graphics cards. It is only necessary to slightly modify the video BIOS and obtain a simple capable assembly to make the Fujitsu plasma display plug compatible with a CRT used for VGA applications.

Future Developments

Fujitsu is continuing its plasma display R&D with efforts to attain finer dot pitch and produce new driver ICs. A new gradation technology is also under development. Color PDPs are currently being engineered, with production for the US market expected to begin by 1Q'93.

Section 2

Plasma Display Unit–Character Type — *At a Glance*

February 1991
Edition 1.0

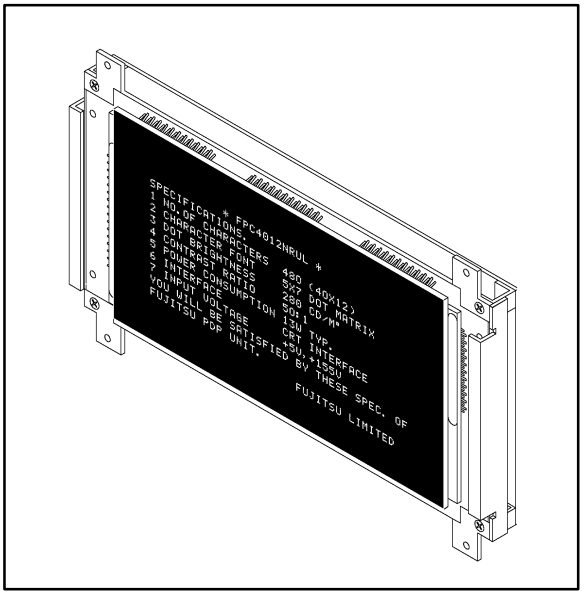
FUJITSU

DATA SHEET

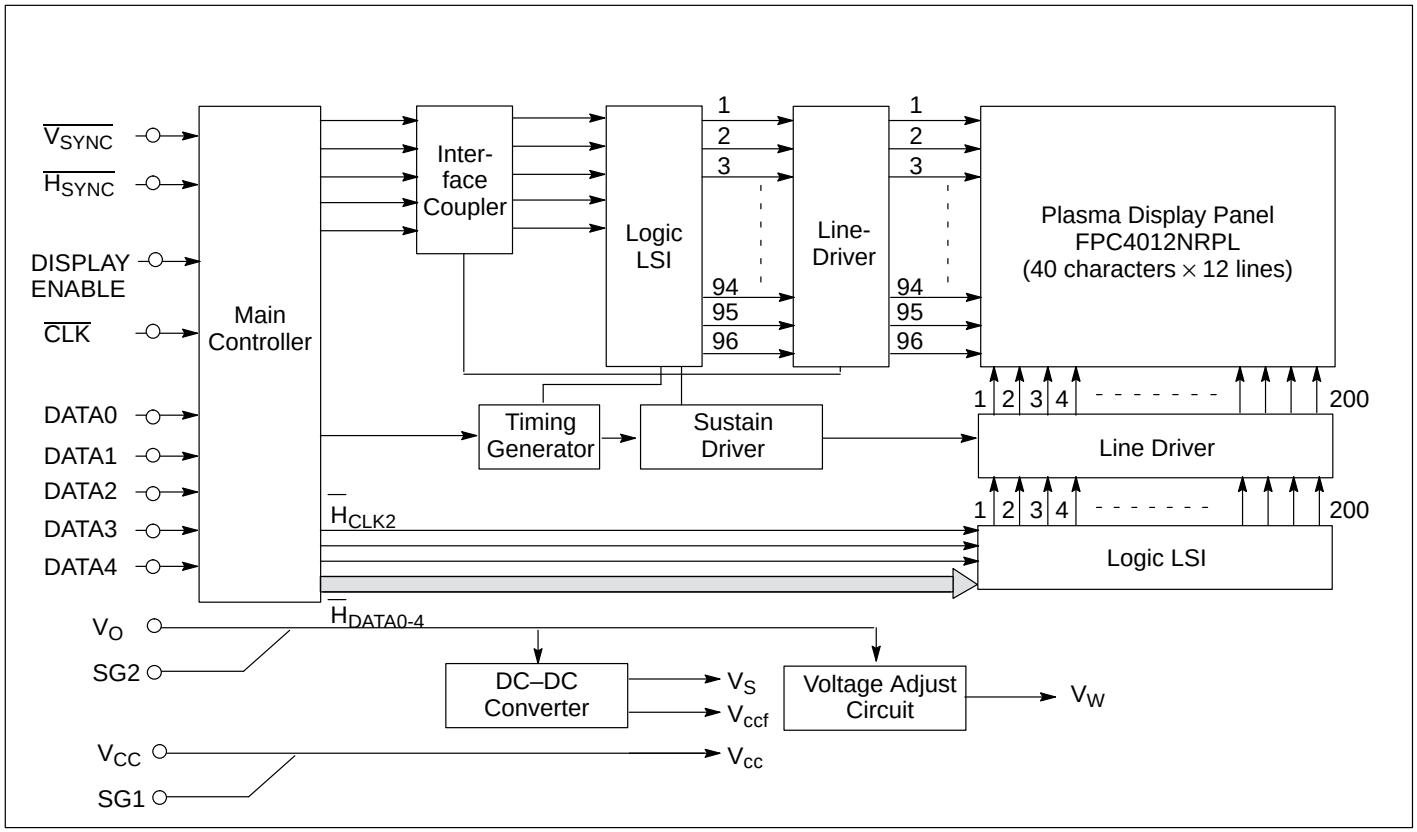
FPC4012NRUL-01
Plasma Display Unit

The FPC4012NRUL plasma display unit is an easy-to-view, high-brightness, 480-character AC-memory type plasma display panel. Dielectric strength monolithic ICs are used for the drive circuits, and CMOS LSIs are used for the control logic, making the unit more compact and reliable. Because the interface is set up to match standard CRTs, the unit can be easily connected to all types of equipment.

- Bright, even, orange-on-black display
- Easy-to-use CRT interface
- Monolithic IC driver
- Power-saving features
- Space-saving size and shape
- High reliablity



BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Display Power Voltage	V_O	170 V
Logic Power Voltage	V_{CC}	7.0 V
Logic 1 Voltage	V_{IH}	5.5 V
Logic 0 Voltage	V_{IL}	–0.5 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Display Power Voltage	V_O	147	155	165	V
Display Power Current (V_O = 155 V)	I_S	—	60	75	mA
Logic Power Voltage	V_{CC}	4.75	5.0	5.25	V
Logic Power Current (V_{CC} = 5.5 V)	I_{CC}	—	0.6	0.65	A
Logic 1 Voltage	V_{IH}	2.4	—	5.25	V
Logic 1 Current (V_{IH} = 3.0 V)	I_{IH}	—	—	80	µA
Logic 0 Voltage	V_{IL}	0	—	0.4	V
Logic 0 Current (V_{IL} = 0.4 V)	I_{IL}	—	—	–3.2	mA

Note: The maximum display power current is measured by displaying Bs at all positions.

MECHANICAL SPECIFICATIONS

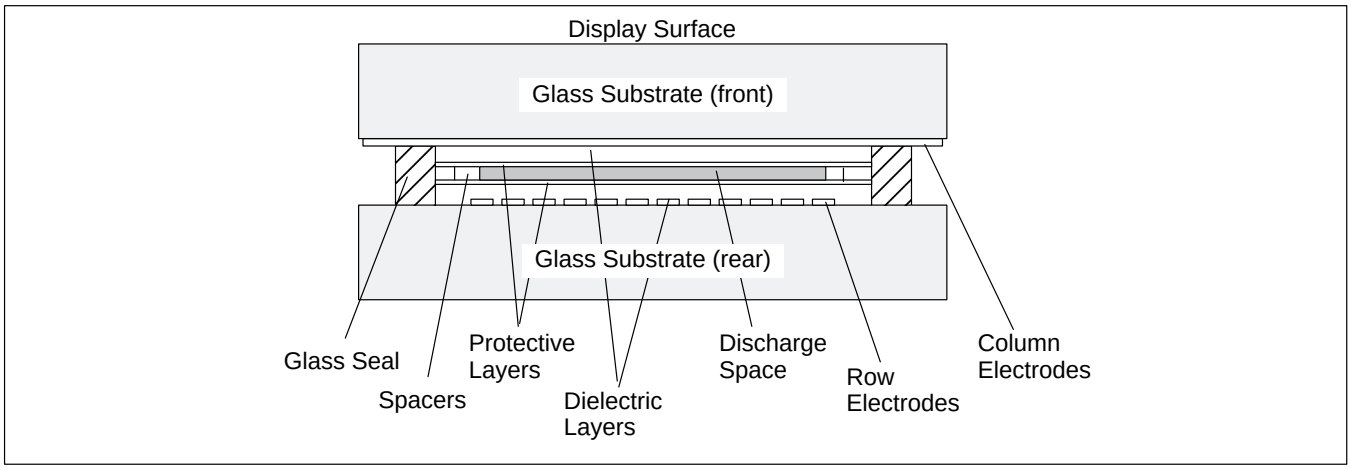
Physical Specifications

Item	Value
Display Panel	FPC4012NRPL
Number of Characters	480 (40 characters/line × 12 lines)
Character Size	2.7 mm × 3.9 mm
Character Font	5 × 7 dot matrix + cursor
Character Spacing	Row Spacing: 2 dots Line Spacing: 4 dots
Effective Display Screen Size	166.2 (width) × 77.4 (height)
Dot Pitch	0.635 (H) × 0.6 (V) mm
Display Color	Neon Orange
Dot Brightness	280 cd/m^2 typ.
Average Character Brightness	75 cd/m^2 typ.
Contrast Ratio	50:1
Viewing Angle	120 deg. min.
Weight	1.2 kg (approx.)
External Dimensions	See External Dimensions figure

Performance Specifications

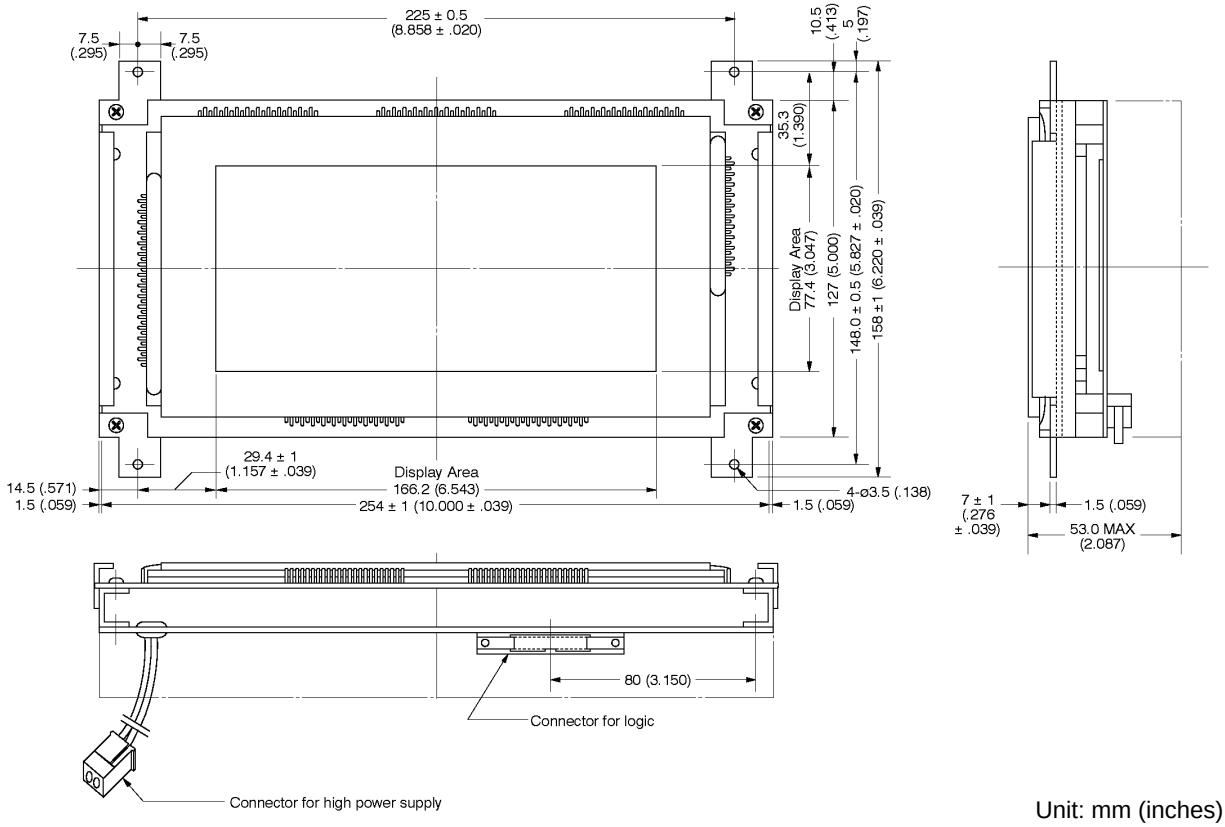
Item	Value
Ambient Temperature	–5 to +50 °C
Storage Temperature	–20 to +70 °C
Humidity	20 to 85% RH
Ambient Pressure Operation: Non-operation:	 550 to 800 torr 250 to 800 torr
Vibration Frequency: Acceleration: Time:	 10 to 55 Hz 2 G max. Operation: 5 min. in X, Y, and Z direction Non-operation: 2 hours in X, Y, and Z direction
Shock (non-operation) Acceleration: Time:	 40 G max. 11 msec max.

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

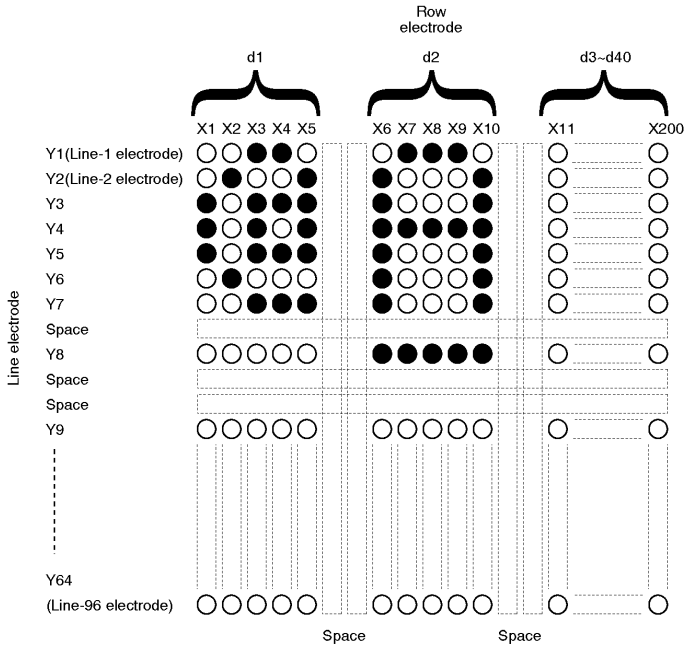


INTERFACE SIGNALS

Type of Signals (TTL Compatible)

Signal	Symbol	Definition and Function
Character Data	(DATA 0 to 4)	Character dot pattern (5 dots) input signal. Character dot data is read into the unit's register in order from character 1 to character 40 at the rising edge of each clock signal. Data is displayed when these signals are at logic 1 level; nothing is displayed when signals are at logic 0 level.
Clock	CLK	Input signal for controlling input timing of character data. Character dot data is read into the unit when the clock signal rises.
Line Synchronous Signal	$\overline{H_{SYNC}}$	Input signal for controlling scan timing of line electrodes. When each pulse falls, the address is changed to the next line electrode.
Screen Synchronous Signal	$\overline{V_{SYNC}}$	Input signal for controlling refresh speed of the screen. The scan position returns to line 1 when the $\overline{V_{SYNC}}$ signal falls.
Display Enable	(DE)	Regardless of the status of other signals, data is erased when this signal is at logic 0 level.

Relationship Between Display Data and Display Dots

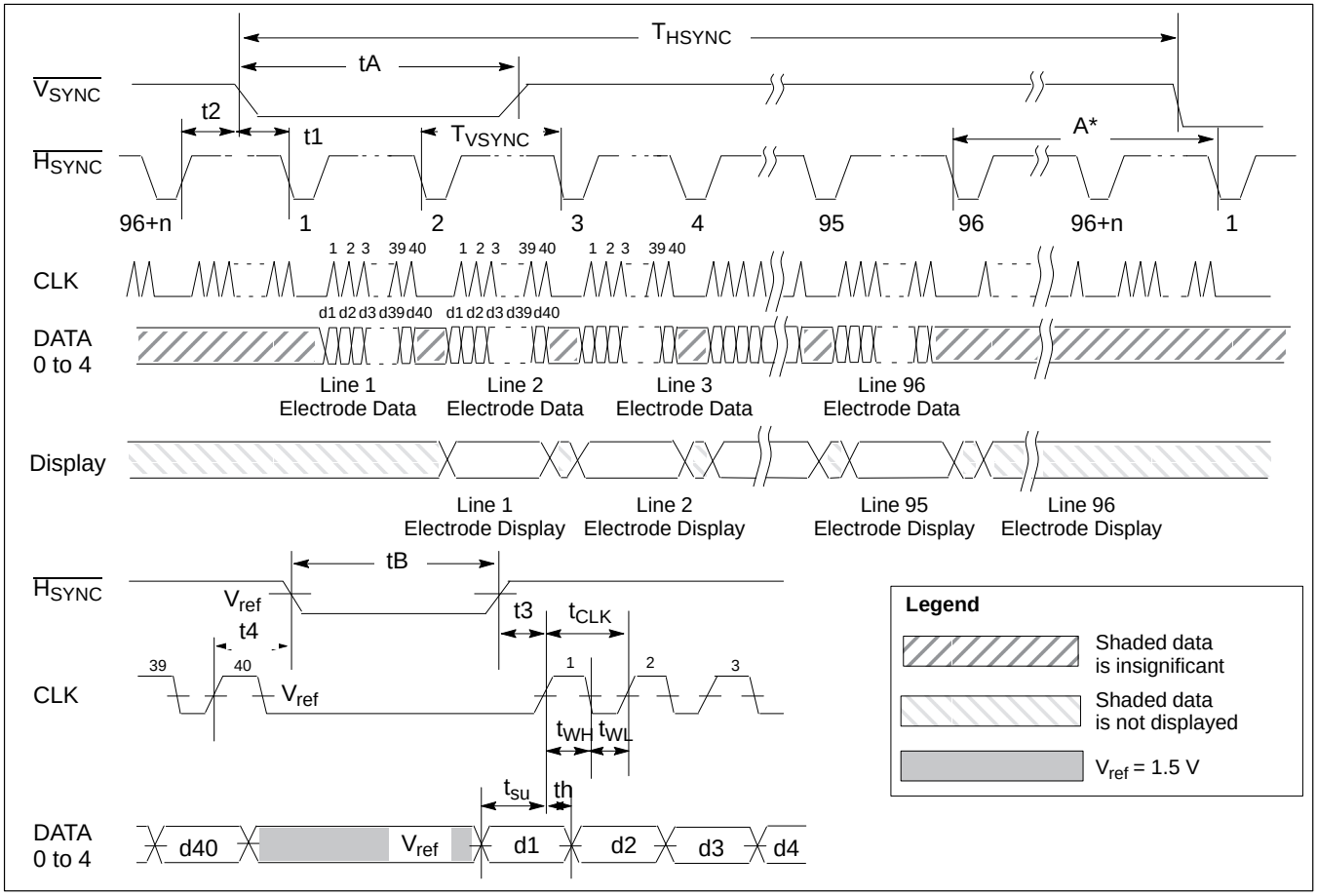


Interface Signal Timing

Symbol	Min.	Max.	Unit
T_{VSYNC}	—	16.7	ms
tA	1	—	µs
T_{HSYNC}	150	190	µs
tB/T_{HSYNC}*	10	30	%
t1	1	—	µs
t2	1	—	µs
T_{clk}	1000	—	ns
t_{WL}, t_{WH}	200	—	ns
t3	100	—	ns
t4	800	—	ns
t_{su}	150	—	ns
th	80	—	ns

Note: *The typical value for tB/T_{HSYNC} is approximately 20%.

Interface Signal Timing Chart



Note: *Equivalent to retrace time in a CRT, but not necessary in this unit. Brightness is increased by reducing this period.

CONNECTOR PIN ASSIGNMENT

Logic Connector

FCN-705P026-AU/M (Fujitsu)

Pin No.	Signal	Pin No.	Signal
1	V_{CC} (+5 V)	2	V_{CC} (+5 V)
3	V_{CC} (+5 V)	4	V_{CC} (+5 V)
5	V_{CC} (+5 V)	6	V_{CC} (+5 V)
7	SG1	8	SG1
9	DATA0	10	SG1
11	DATA1	12	SG1
13	DATA2	14	SG1
15	DATA3	16	SG1
17	DATA4	18	SG1
19	CLK	20	SG1
21	$\overline{H_{SYNC}}$	22	SG1
23	$\overline{V_{SYNC}}$	24	SG1
25	DISPLAY ENABLE	26	SG1

High Power Supply Connector

Pin No.	Signal
1	V_O (+155 V)
2	NC
3	SG2

Applicable Connectors:
Housing: FCN-813J003-A (Fujitsu)
Contact: FCN-813J-T/Q (Fujitsu)

Section 3

Graphic Unit–Small Size — *At a Glance*

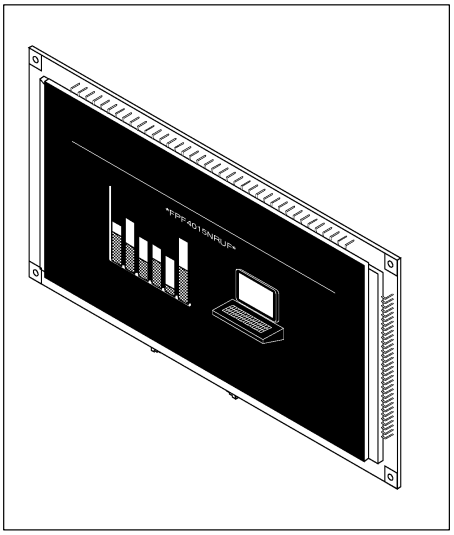
February 1991
Edition 1.0

FUJITSU

DATA SHEET

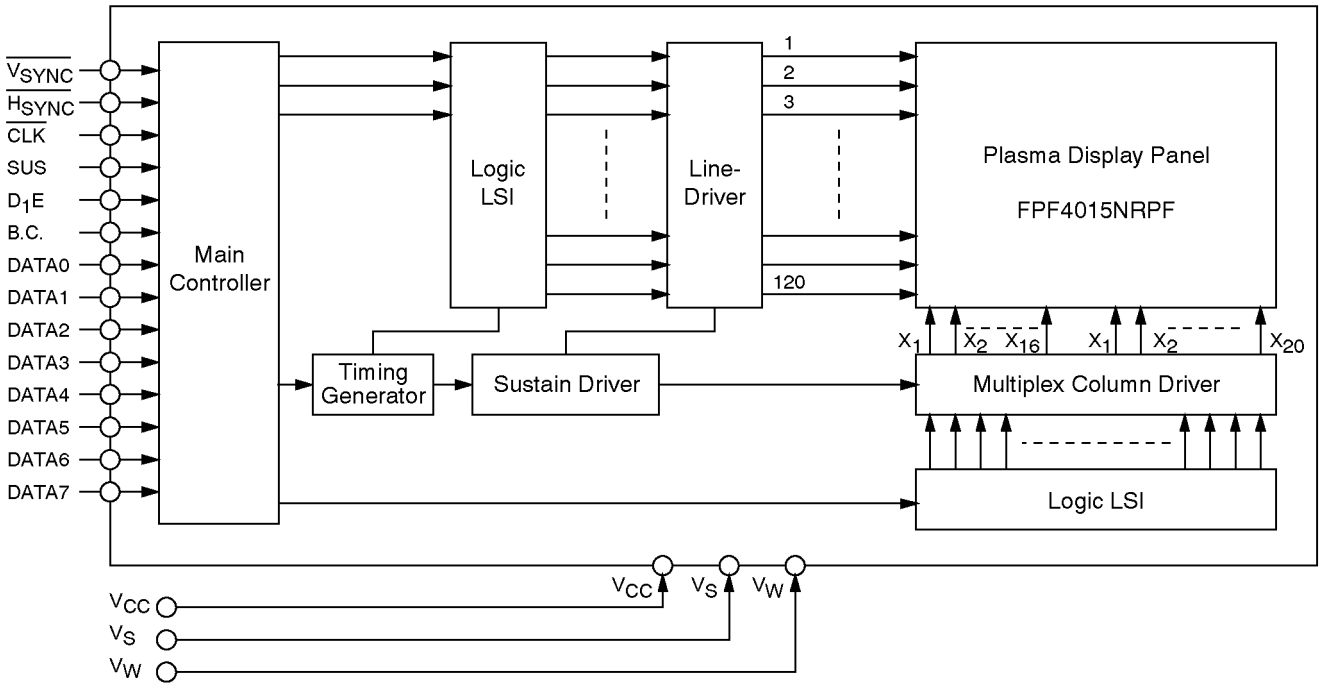
FPF4015NRUF
Plasma Display Unit

The FPF8050HFUGA plasma graphics display unit consists of an AC memory–type display panel with associated driver circuitry. This unit uses a multiplex drive to provide a generous 320 X 120 full–dot matrix. Dielectric strength monolithic ICs are used for the drive circuits, and CMOS LSIs are used for the control logic, making the unit more compact and reliable. The orange–on–black, high–contrast panel provides an easy–to–read display with no flicker or warp. Because the interface is set up to match standard CRTs, the unit can be easily connected to all types of equipment.



- Bright, even, orange-on-black display
- Easy-to-use CRT interface
- Monolithic IC driver
- Power saving features
- Space–saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Display Supply Voltage 1	V_S	110 V
Display Supply Voltage 2	V_W	155 V
Logic Supply Voltage		7.0 V
Logic 1 Input Voltage	V	5.5 V
Logic 0 Input Voltage	V	–0.5 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Display Supply Voltage 1	V_S	—	90[1]	—	V
Display Supply Current 1 (V_S = 90 V)	I_S	—	—	140	mA
Display Supply Voltage 2	V_W	—	140[2]	—	V
Display Supply Current 2 (V_W = 135 V)	I_W	—	—	30	mA
Logic Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Logic Supply Current (V_{CC} = 5.5 V)	I_{CC}	—	—	0.8	A
Logic 1 Input Voltage	V_{IH}	2.4	—	5.25	V
Logic 1 Input Current (V_{IH} = 3.0V)	I_H	—	—	80	µA
Logic 0 Input Voltage	V_{IL}	0	—	0.4	V
Logic 0 Input Current (V_{IL} = 0.4 V)	I_{IL}	—	—	–5.5	mA

Notes: [1]The power source is required to be variable from 80 to 100 VDC.
[2]The power source is required to be variable from 130 to 150 VDC.

MECHANICAL SPECIFICATIONS

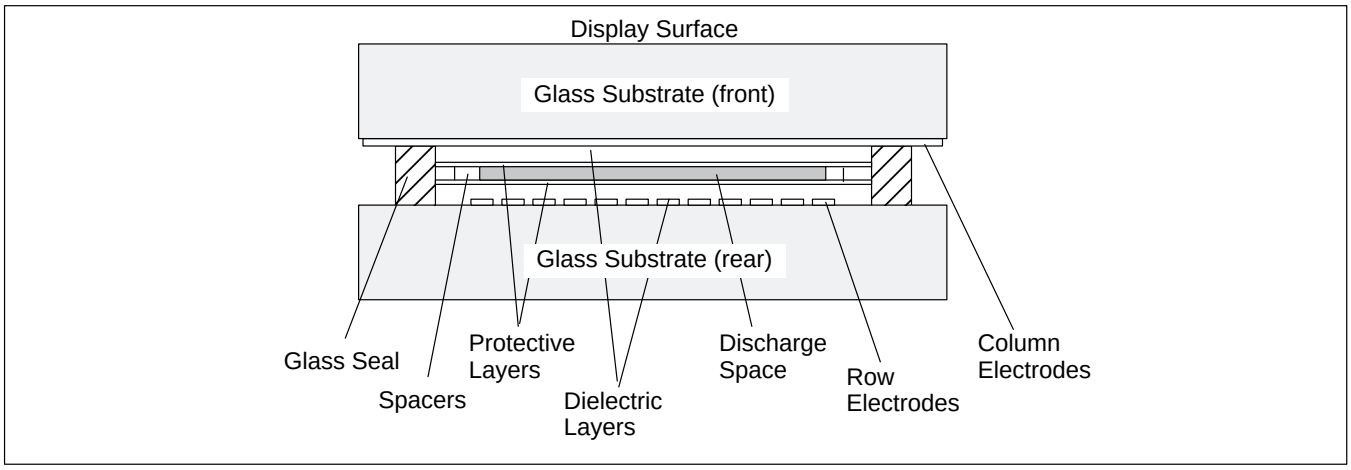
Physical Specifications

Item	Value
Number of Display Dots	320 (H) X 120 (V) dots (38,000 dots)
Dot Pitch	0.6 mm
Dot Size	Approx 0.3 mm dia
Effective Screen Size	191.4 X 71.4 mm
Display Color	Neon Orange
Dot Brightness (peak)	280 cd/m^2 typ
Contrast Ratio	20:1 min.
Viewing Angle	120° min.
Display Capacity	33% (12,800 dots) max
External Dimensions	See External Dimensions Figure
Weight	0.8 kg

Performance Specifications

Item	Value
Operating Temperature	–5 to +50°C
Storage Temperature	–20 to 70°C
Humidity	20 to 80% RH (no condensation)
Atmospheric Pressure Operation: Non–Operation:	 700 to 1114 mb 340 to 1114
Vibration Frequency: Acceleration: Time:	 10 to 55 Hz 2 G max Operation: 5 min in X, Y and Z direction Non–Operation: 2 hours in X, Y and Z direction
Shock (non–operation) Acceleration: Time:	 40 G max 11 msec max

Physical Construction and Operation



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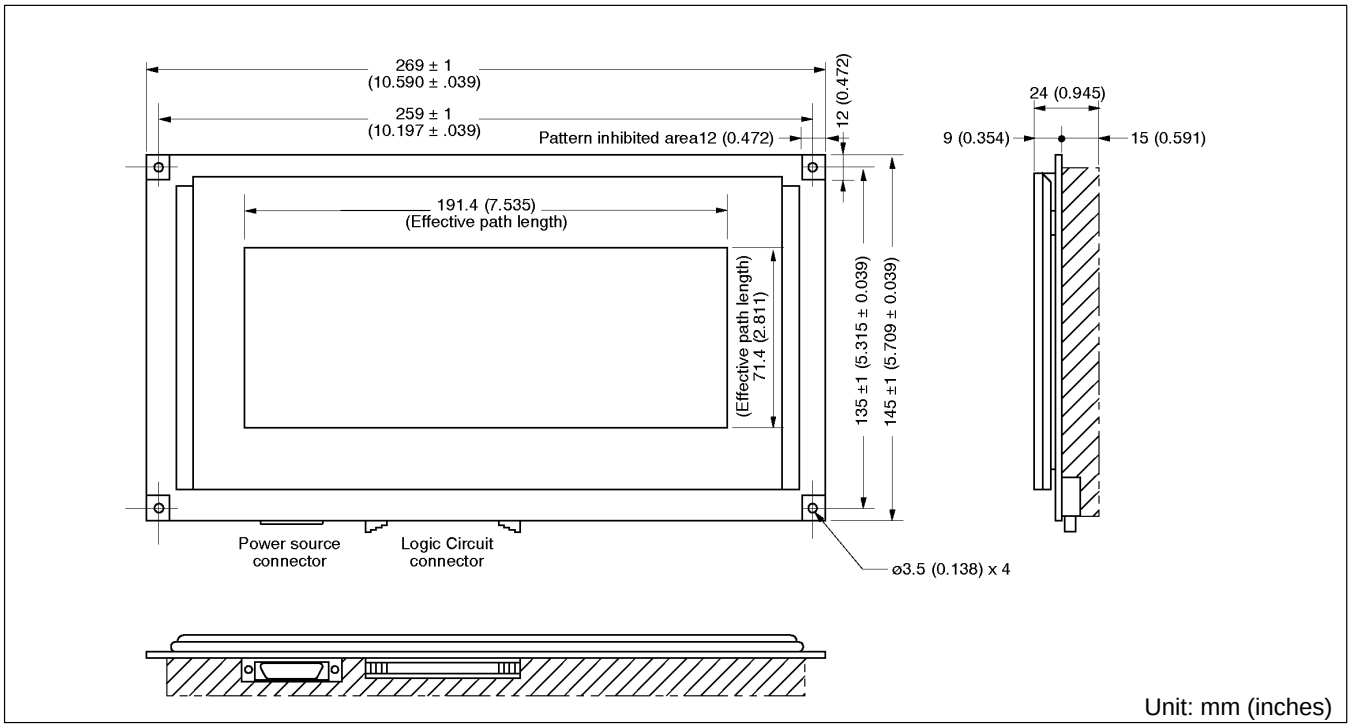
External Dimensions



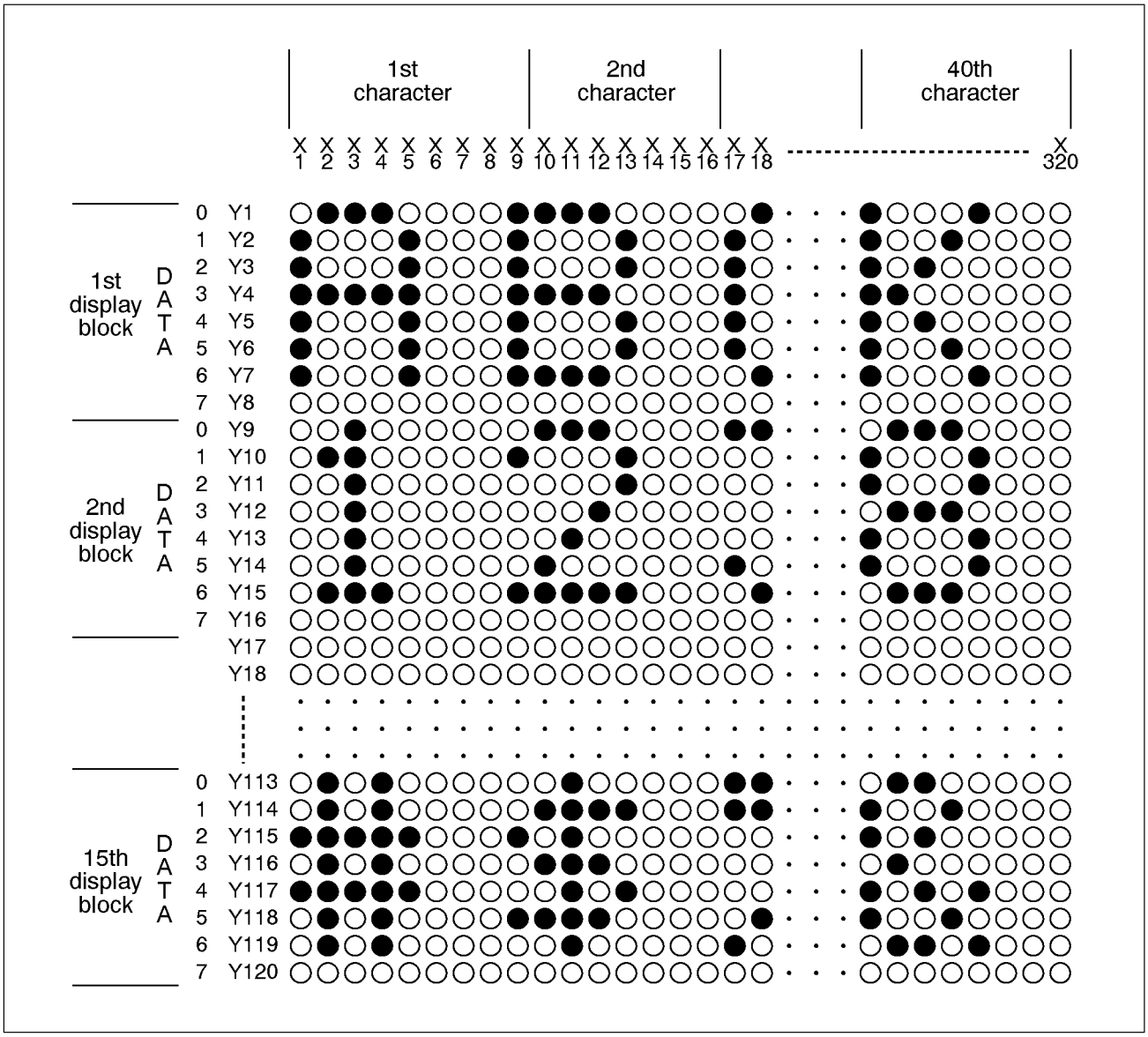
INTERFACE SIGNALS

Type of Signals (TTL Compatible)

Signal	Symbol	Definition and Function
Display Data Signal	DATA	Dot matrix display data, which comprises of 8–bit parallel signals, is read at the rise of each CLK signal into the shift register in order from display blocks 1 to 15. Dots light up at logic 1 and turn off at logic 0.
Clock Signal	CLK	The CLK signal is the input signal used to control display data input timing. Dot data is read into the unit at the rise of each CLK signal.
Line Synchronous Signal	$\overline{H_{SYNC}}$	The $\overline{H_{SYNC}}$ signal is the input signal used to control column electrode scan timing. Addressing is shifted to the next column electrode at the fall of each $\overline{H_{SYNC}}$ signal.
Frame Synchronous Signal	$\overline{V_{SYNC}}$	The $\overline{V_{SYNC}}$ signal is the input signal used to control the screen refresh speed. Scanning returns to the first column electorde at teh fall of each $\overline{V_{SYNC}}$ signal.
Brightness Control Signal	B.C.	The BRIGHTNESS CONTROL signal controls the display screen brightness. The screen goes to 100% brightness at logic 1 and to 50% at logic 0.
Display Enable	D. ENABLE	The DISPLAY ENABLE signal controls whether or not data is displayed, and overrides other signals. Display is enabled at logic 1 and disabled at logic 0.

Relationship Between Display Data and Display Dots

Relationship Between Display Data and Display Dots



Interface Signal Timing Table

Symbol	Min	Max	Unit
T_{VSYNC}	___	___	ms
t_A	1	___	µs
T_{HSYNC}	180	200	µs
tB	5	___	µs
t1	1	___	µs
t2	4	___	µs
T_{CLK}	1000	___	ns
twh,twl	250	___	ns
t3	100	___	ns
t4	4	___	µs
tsu	150	___	ns
th	100	T_{CLK}	ns

CONNECTOR PIN ASSIGNMENT

Logic Connector

FCN-705Q034-AU/M

Pin No.	Symbol	Pin No.	Symbol
1	V_{CC}	2	V_{CC}
3	V_{CC}	4	V_{CC}
5	DATA0	6	SG1
7	DATA1	8	SG1
9	DATA2	10	SG1
11	DATA3	12	SG1
13	DATA4	14	SG1
15	DATA5	16	SG1
17	DATA6	18	SG1
19	DATA7	20	SG1
21	CLK	22	SG1
23	$\overline{H_{SYNC}}$	24	SG1
25	$\overline{V_{SYNC}}$	26	SG1
27	B.C.	28	SG1
29	SUS	30	SG1
31	$\overline{\text{D. ENABLE}}$	32	SG1
33	N.C.	34	N.C.

Power Source Connector

FCN–365P016–AU

Pin No.	A	B
1	V_S	V_S
3	GND	GND
4	GND	GND
5	GND	GND
6	GND	GND
7	V_W	V_W
8	V_W	V_W

Section 4

Graphic Units (640 by 400 dots) — *At a Glance*

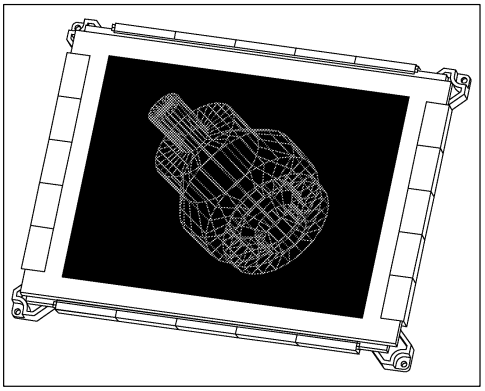
February 1991
Edition 1.0

FUJITSU

DATA SHEET

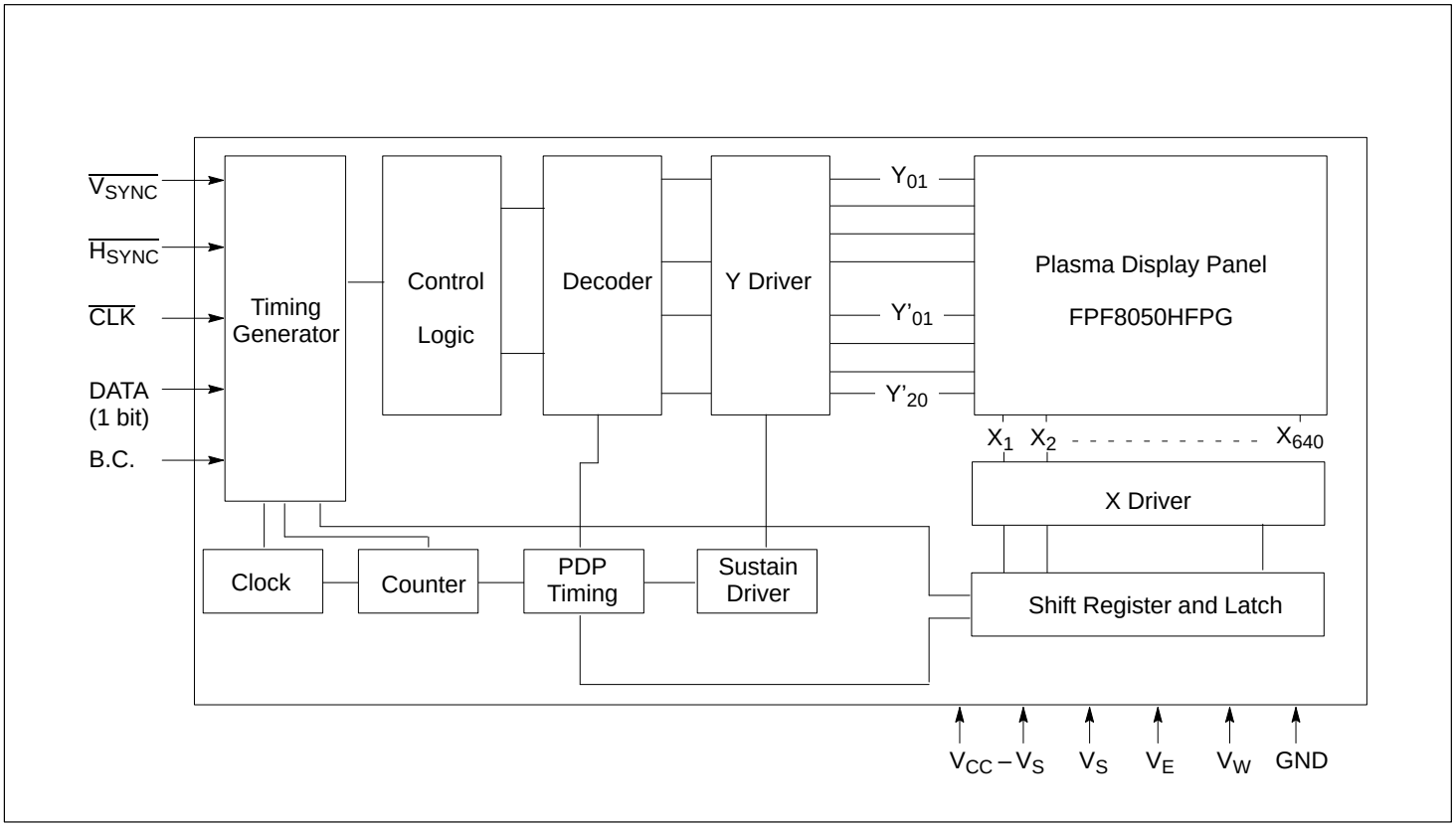
FPF8050HFUGA
Plasma Display Unit

The FPF8050HFUGA plasma graphics display unit consists of an AC gas discharge plasma display panel with bistable memory and associated driver circuitry. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. This compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8050HFUGA a highly reliable display device.



- Bright, even, orange-on-black display
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Sustain Voltage 1	V_S	125 V
Sustain Voltage 2	$-V_S$	–125 V
Write Voltage	V_W	180 V
Erase Voltage	V_E	45 V
Logic Voltage	V_{CC}	7 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage 1 for Sustain	V_S	85	95[1]	105	V
Supply Current 1 for Sustain (V_S = 95 V)	I_S	—	75	160	mA
Supply Voltage 2 for Sustain	$-V_S$	–85	–95[2]	–105	V
Supply Current 2 for Sustain ($-V_S$ = –95 V)	$-I_S$	—	–75	–160	mA
Supply Voltage for Writing	V_W	150	165[3]	175	V
Supply Current for Writing (V_W = 165 V)	I_W	—	10	20	mA
Supply Voltage for Erase	V_E	38	40	42	V
Supply Current for Erase (V_E = 40 V)	I_E	—	100	150	mA
Supply Voltage for Logic	V_{CC}	—	5.0	5.25	V
Supply Current for Logic (V_{CC} = 5 V)	I_{CC}	—	0.35	0.5	A
Signal Input Voltage (H-Level)	V_{IH}	2.4	—	5.25	V
Signal Input Current (H-Level) (V_{IH} = 2.75 V)	I_{IH}	—	—	20	µA
Signal Input Voltage (L-Level)	V_{IL}	—	—	0.4	V
Signal Input Current (L-Level) (V_{IL} = 0.4 V)	I_{IL}	—	—	–16	mA

Notes: [1]The power source is required to be variable from 85 to 105 VDC.
[2]The power source is required to be variable from –85 to –105 VDC.
[3]The power source is required to be variable from 150 to 175 VDC.

MECHANICAL SPECIFICATIONS

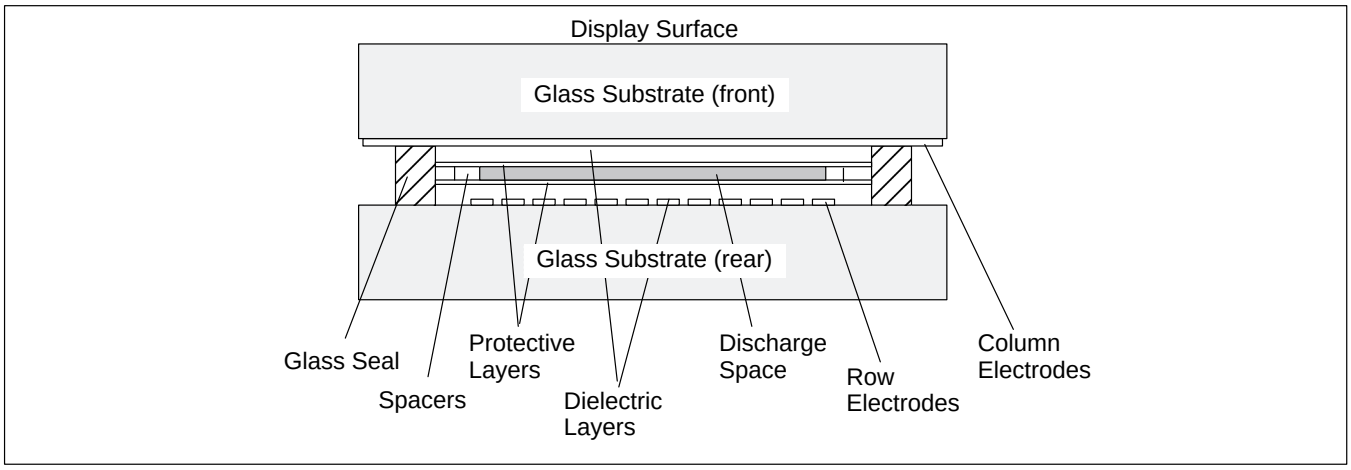
Physical Specifications

Item	Value
Display Panel	FPF8050HFPG
Number of Display Dots	640 (H) × 400 (V) dots (256,000 dots)
Dot Pitch	0.33 (H) × 0.33 (V) mm (0.013 × 0.013 in.)
Dot Size	0.2 mm (0.008 in.) dia.
Effective Screen Area	132 (V) × 211 (H) mm (5.197 × 8.307 in.)
Dot Brightness (peak)	150 cd/m^2
Contrast Ratio	20:1 min.
Viewing Angle	160° min.
Weight	1.7 kg
External Dimensions	See External Dimensions Figure

Performance Specifications

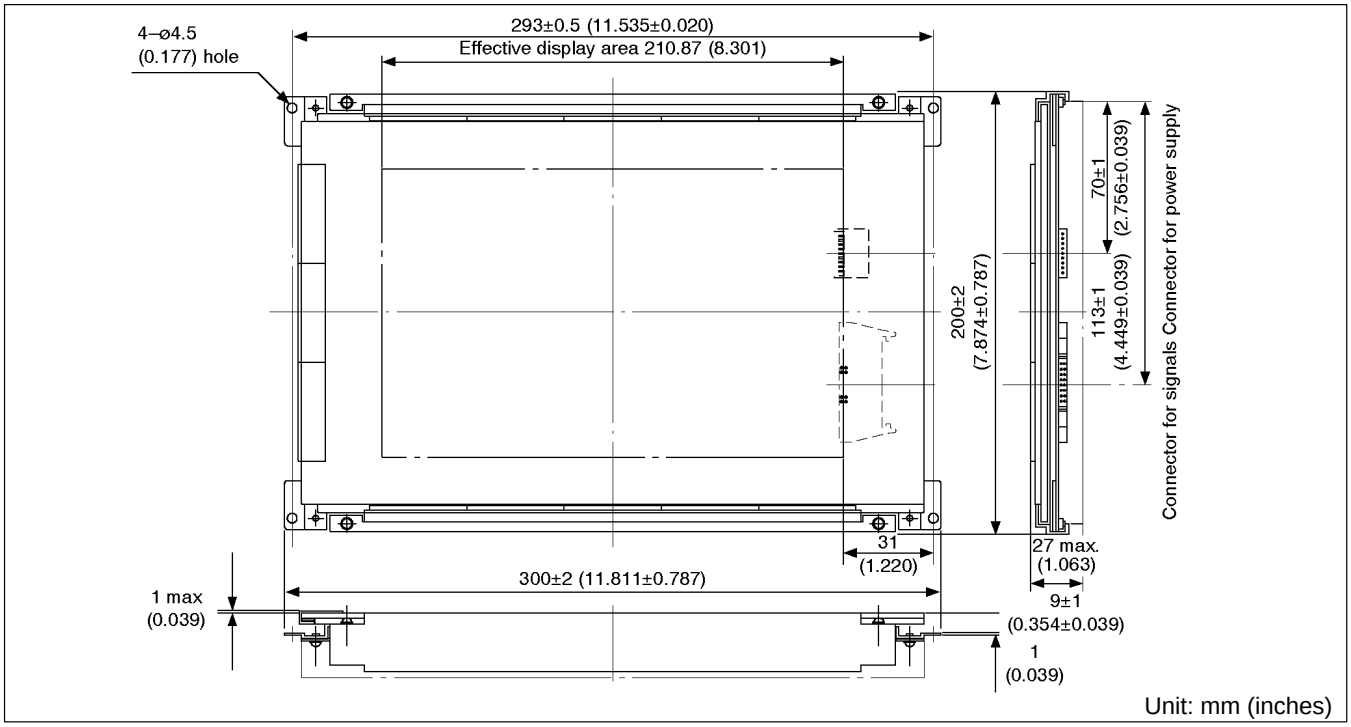
Item	Value
Operating Temperature	0 to +50°C
Operating Humidity	20 to 85% RH
Storage Temperature	–20 to +70°C
Storage Humidity	20 to 85% RH
Atmospheric Pressure	Non-Operation: 340 to 1114 hPa
Vibration	2 G
Shock	40 G

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

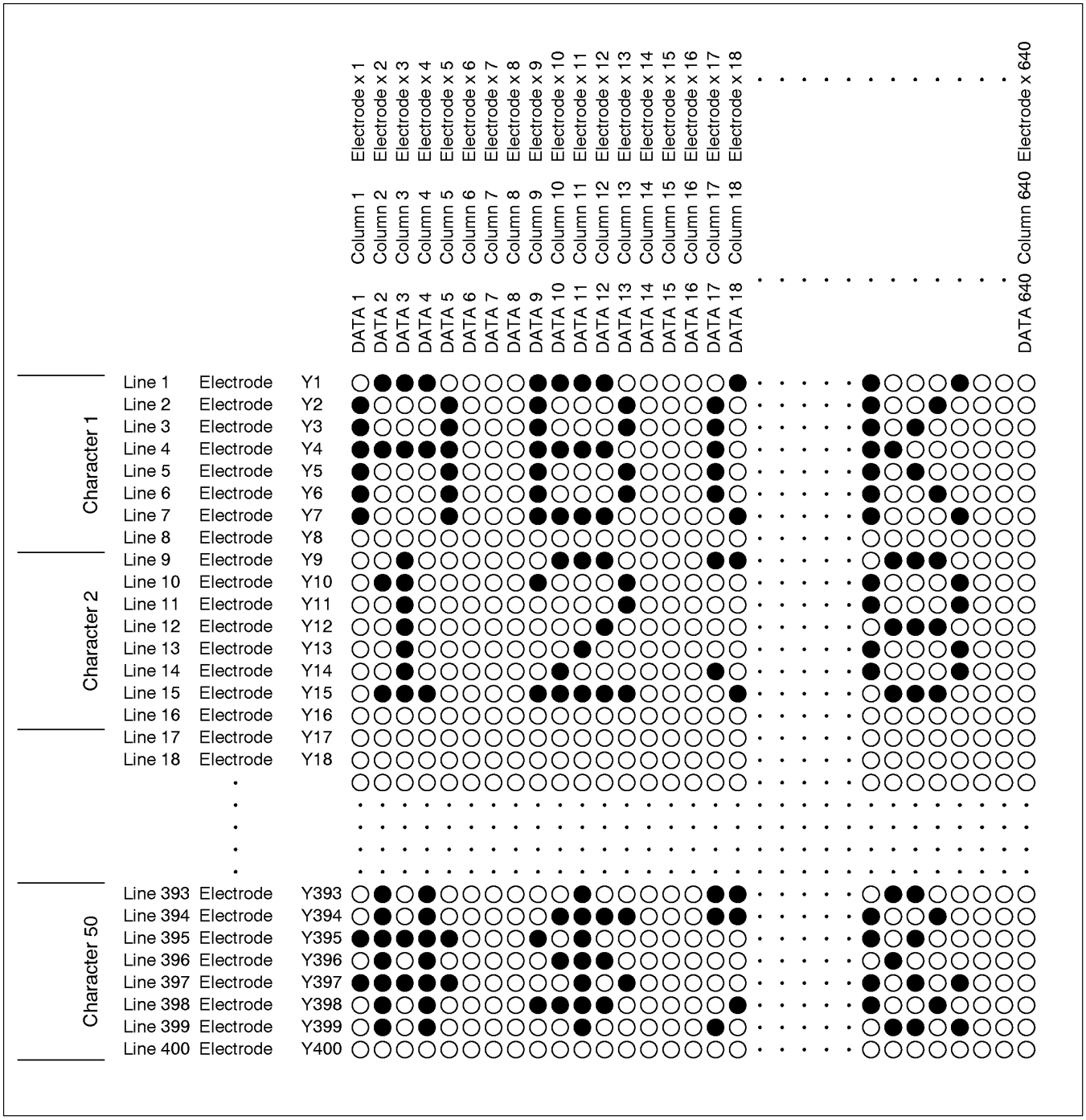


INTERFACE SIGNALS

Type of Signals (TTL Compatible)

Signal	Symbol	Definition and Function
Display Data Signal	DATA	The serial dot data which is input synchronized with the leading edge of the clock signal. Dots are lit at logical High and are not lit at logical Low. The relationship between display data and display dots is shown in the following figure.
Clock Signal	CLK	The input signal which controls the input timing of the display data. Dot data is read into the shift register at the leading edge of the signal. The number of clock signals during the period $\overline{H_{SYNC}}$ is 640.
Line Synchronous Signal	$\overline{H_{SYNC}}$	The input signal which controls the scanning timing of the line electrode. Address increment to select the next line electrode is done at the trailing edge of each signal.
Frame Synchronous Signal	$\overline{V_{SYNC}}$	The input signal which controls the refresh speed of the screen. The scanning position returns to the first line electrode (home position) at the trailing edge of the $\overline{V_{SYNc}}$.
Brightness Control Signal	B.C.	The input signal which controls the screen brightness. Brightness is at its maximum at logic High, and is 50% of the maximum at logic Low.

Relationship Between Display Data and Display Dots

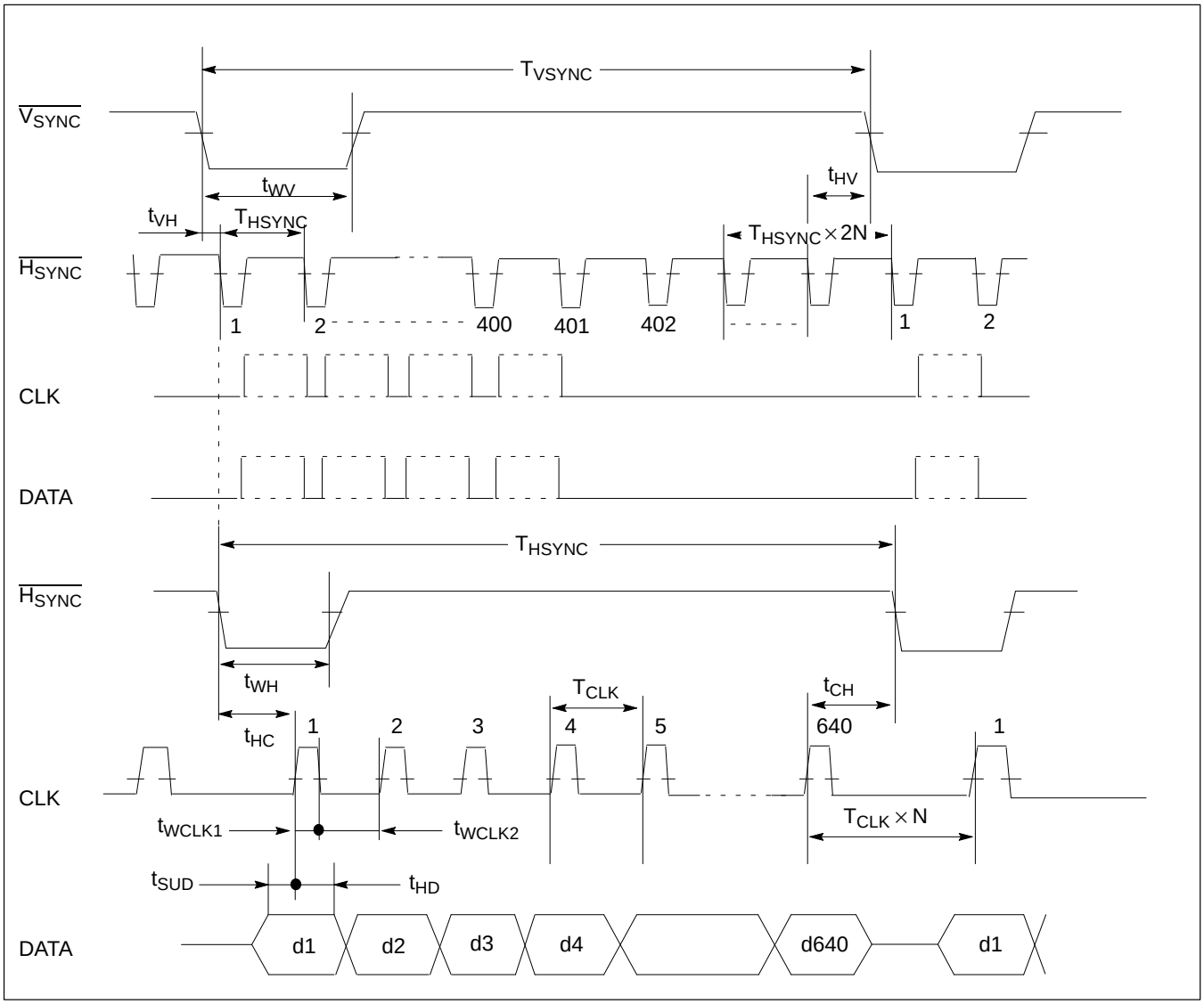


Interface Signal Timing Table

Symbol	Description	Min.	Typ.	Max.	Unit
T_{VSYNC}	A Cycle of Frame Synchronous Signal	16.8	25	—	ms
t_{WV}	Pulse Width of Frame Synchronous Signal	2	—	—	µs
t_{VH}	Delay Time $\overline{V_{SYNC}}$ – $\overline{H_{SYNC}}$	1	—	—	µs
t_{HV}	Delay Time $\overline{H_{SYNC}}$ – $\overline{V_{SYNC}}$	2	—	—	µs
T_{HSYNC}	A Cycle of Line Synchronous Signal	40	60	80	µs
t_{WH}	Pulse Width of Line Synchronous Signal	2	—	—	µs
t_{HC}	Delay Time $\overline{H_{SYNC}}$ – CLK	1	—	—	µs
t_{CH}	Delay Time CLK – $\overline{H_{SYNC}}$	0.5	—	—	µs
T_{CLK}	A Cycle of Clock Signal	45	80	110	ns
$t_{WCLK1,2}$	Pulse Width of Clock Signal*	22	40	—	ns
t_{SUD}	Set Up Time for Data	20	40	—	ns
t_{HD}	Hold Time for Data	22	40	—	ns

Notes: *Recommended ratio between t_{WCLK1} and T_{WCLK2} is 1:1

Interface Signal Timing Chart (400-line display mode)



Note: 200-line display mode with double scanning function is available by setting short socket on the back of unit.

CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-605Q016-G/S

Pin No.	Symbol	Pin No.	Symbol
1	N.C.	2	N.C.
3	N.C.	4	S. GND
5	DATA	6	S. GND
7	N.C.	8	S. GND
9	$\overline{H_{SYNC}}$	10	S. GND
11	$\overline{V_{SYNC}}$	12	S. GND
13	B.C.	14	S. GND
15	CLK	16	S. GND

Notes: Applicable Connector:
FCN-607B016-G/D without strain relief (attached)

N.C. means “No Connection.”

Power Supply Connector

FCN-815P-009TA

Pin No.	Symbol
1	V_{CC}
2	GND (L)
3	$-V_S$
4	GND (H)
5	$+V_S$
6	V_W
7	N.C.
8	V_E
9	N.C.

Notes: Applicable Connectors:
FCN-813J009-A, Housing
FCN-813J-T/Q, Contact for Manual Use
FCN-813J-T/R, Contact for Automatic Use

January 1992
Edition 1.0

DATA SHEET

FPF8050HRUC-001

640 x 400 Dots, High Brightness, Plasma Display Unit

9.8-IN DIAGONAL SCREEN GRAPHIC UNIT WITH HIGH BRIGHTNESS, FLICKER-FREE DISPLAY

DESCRIPTION

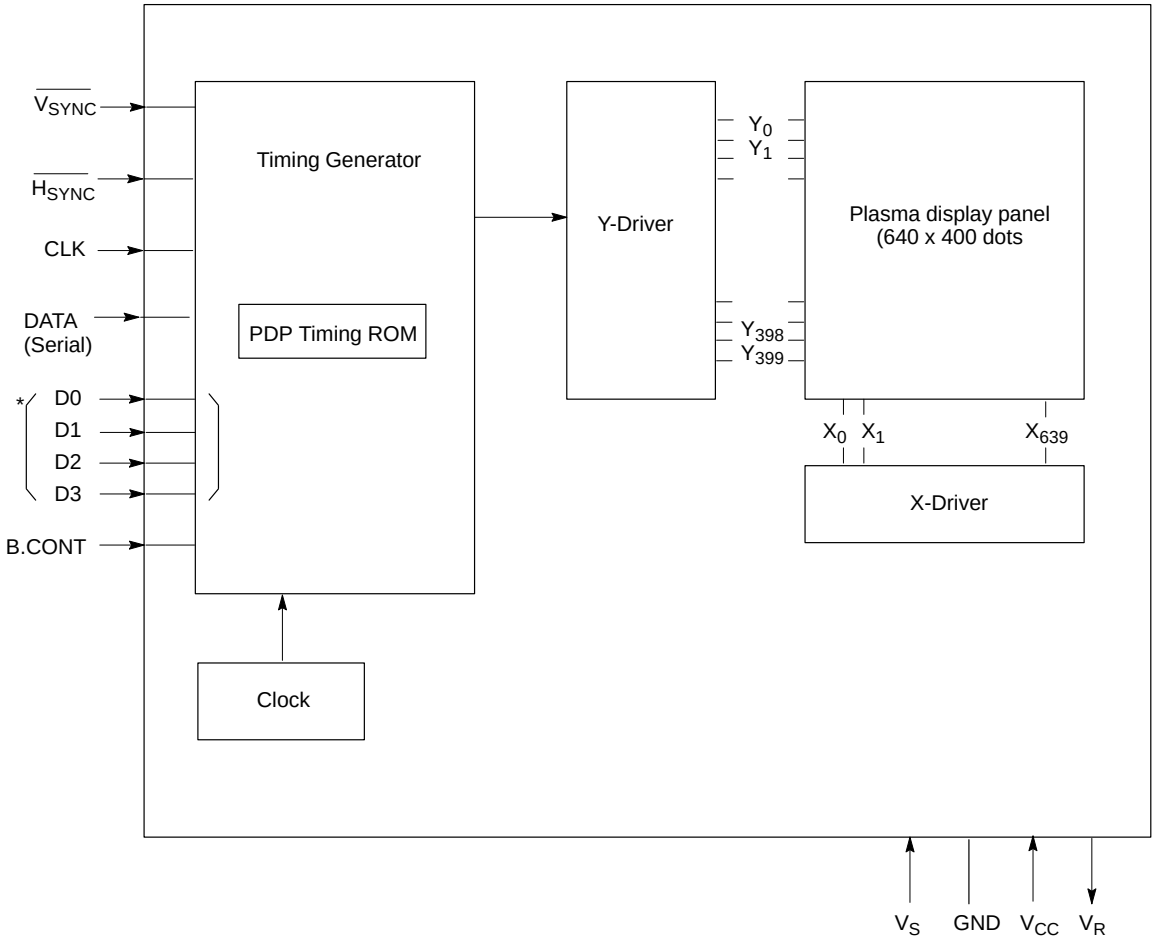
Fujitsu plasma display unit consists of an AC-type gas discharge plasma panel with memory function based on Fujitsu's unique panel technologies and its driving circuit.

The black-faced panel provides a clear display even in bright conditions, and memory function provides easy-to-view flicker-free display; the newly developed panel gives high brightness display.

FEATURES

- High brightness of 150 cd/m^2
- High contrast: 20 :1
- Easy-to-view flicker-free display
- 50,000 hours of panel life without brightness reduction
- Easy-to-use interface conforming to CRT interface

BLOCK DIAGRAM



*Use DATA signal line for serial data; use D0 to D3 signal lines for 4-bit parallel data
Refer to the signal pin arrangement for the signal line connections.

SPECIFICATIONS

Item	Specifications
Number of display dots	640(H) x 400(V) (256,000)
Dot pitch	0.33 mm (H) x 0.33 mm (V) (0.013 in x 0.013 in)
Dot size	Approximately 0.2 mm (0.008 in x 5.184 in)
Display resolution	77 dots per linear inch
Effective display screen area	210.87 mm (H) x 131.67 mm (V) 8.302 in x 5.184 in)
Display color	Neon orange
Brightness	Dot: 150 cd/m^2 typical at 90 µs of $\overline{H_{SYNC}}$ signal Plane avg: 25 cd/m^2 typical at 90 µs of $\overline{H_{SYNC}}$ signal
Contrast ratio	20 : 1 minimum
Viewing angle	160 degrees
Weight	Approximately 1 kg
Dimensions	See DIMENSIONS, page 11

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Sustain voltage	V_S	120	V
Logic voltage	V_{CC}	7	V

OPERATING RATINGS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply voltage for sustain*	V_S	88	95	100.5	V
Supply current for sustain (V_S = 95V)	I_S	50	200	340	mA
Supply voltage for logic	V_{CC}	4.75	5.0	5.25	V
Supply voltage for logic (V_{CC} = 5V)	I_{CC}	60	120	450	mA
Signal input voltage for logic 1 (H-level)	V_{IH}	2.0		5.25	V
Signal input current for logic 1 (V_{IH} = 2.75V)	I_{IH}			20	µA
Signal input voltage for logic 2 (L-level)	V_{IL}	–0.5		0.8	V
Signal input current for logic 1 (V_{IL} = 0.4V)	I_{IL}			–16	mA

ENVIRONMENTAL CONDITIONS

Rating	Symbol	Value	Unit
Operating temperature	T_{OP}	0 to 50	°C
Storage temperature	T_{STG}	–20 to 70	°C
Humidity	RH_{STG}	20 to 85 (no condensation)	%RH
Vibration	V	2	G
Shock	S	40	G
Pressure (non-operating)		340 to 1114	mb

TYPE OF SIGNALS

Signal Name		Symbol	Signal Lines	Function
Data	Serial input	D	1	Display data signals. Dots are lit at logical high and are not lit at logical low. Relation between display data and display dots in parallel input is shown in Figure 3.
	Parallel input	D0 ~ D3	4	
Clock		CLK	1	This input signal controls the input timing of the display data. Dot data is read into the shift register at the rising edge of each signal. The number of clock signals in one cycle of $\overline{H_{SYNC}}$ is 640 in serial input, 160 in parallel input.
Line synchronous		$\overline{H_{SYNC}}$	1	The input signal that controls the scanning timing of the line electrode. Y address increment to select the next line electrode is done at the falling edge of each signal. The number of $\overline{H_{SYNC}}$ signals during the period $\overline{V_{SYNC}}$ must be 402 +2N.
Frame synchronous		$\overline{V_{SYNC}}$	1	This input signal controls the refresh speed of the screen. The scanning position returns to the first electrode (home position) at the failing edge of the $\overline{V_{SYNC}}$ signal
Brightness control		B.CONT	1	The input signal that controls the screen brightness. Brightness is at its maximum at logical high, and 33% of the maximum at logical low. Brightness varies from 33 to 100%.

Note: This plasma display has a function to detect and set the serial/parallel data input signal by counting the number of clock signal inputs during the first and second $\overline{H_{SINC}}$ signal periods.

No. of Clock Signals	Serial/Parallel
640 clocks	Serial
160 clocks	Parallel

TIMING OF INTERFACE SIGNALS

	Symbol	Min	Typ	Max	Unit	Reparks
1	T_{VSYNC}		39.6		ms	Frame frequency: 22 Hz, typical
2	t_{WV}	1			H	H: Horizontal sync period
3	t_{VH}	1		Remark	μs	$t_{VH} < T_{HSYNC}$
4	t_{HV}	2		Remark	μs	$t_{HV} < T_{HSYNC}$
5	T_{HSYNC}	88	90	92	μs	See Note 1
6	t_{WH}	2	6		μs	
7	t_{HC}	2			μs	
8	t_{CH}	2	3		μs	
9	T_{CLK}	44			ns	
10	t_{WCLK1}	$\frac{0.9}{2} T_{CLK}$	$\frac{1}{2} T_{CLK}$	$\frac{1.1}{2} T_{CLK}$	ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$ See Note 2
11	t_{WCLK2}					
12	t_{SUD}	22			ns	
13	t_{HD}	22			ns	

Note 1: T_{HSYNC} ranges from 40 to 45 μs and from 60 to 65 μs are also available. In these cases, brightness control range changes. Refer to the Horizontal Synchronous Signal

Note 2: Recommended t_{WCLK1}/t_{WCLK2} ratio is 1 : 1.

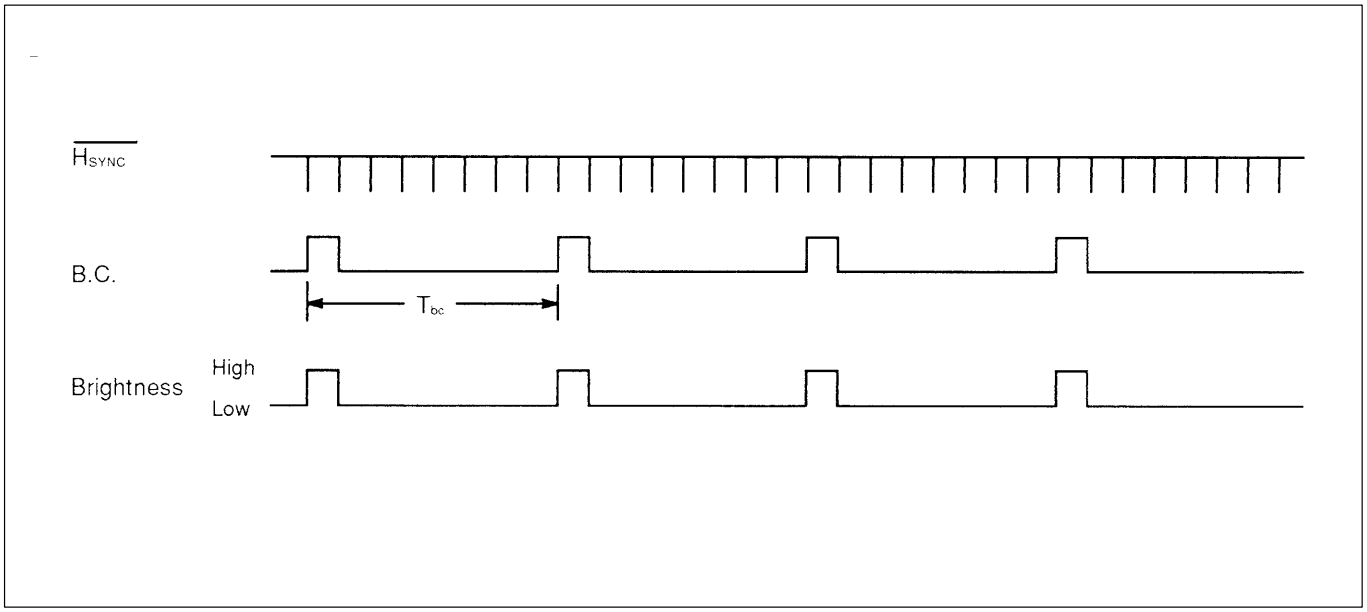
HORIZONTAL SYNCHRONOUS SIGNAL

Recommended T_{HSYNC} condition is from 88 to 92 μs. In addition to this condition, T_{HSYNC} conditions shown in table below are also available. In some cases, note that the brightness, brightness control range, and input current also varies.

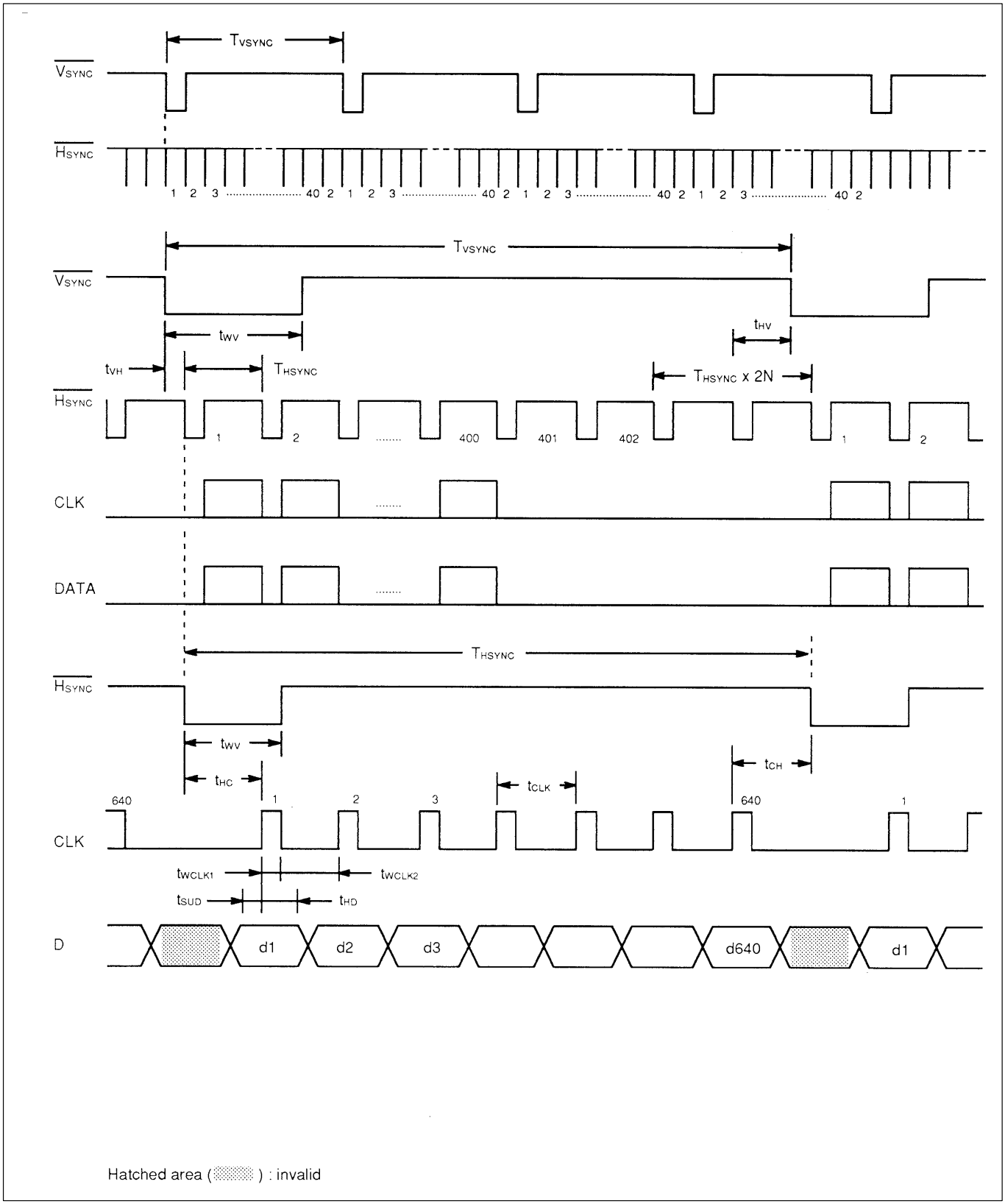
Typical T_{HSYNC} value		42μs	62 μs	90 μs
T_{HSYNC} range		40 ~ 45 μs	60 ~ 65 μs	88 ~ 92 μs
Brightness	Minimum	14 cd/m^2	19 cd/m^2	20 cd/m^2
	Typical	17 cd/m^2	23 cd/m^2	25 cd/m^2
Brightness control range		0 ~ 100%	50 ~ 100%	33 ~ 100%
Input current I_S		280 mA	330 mA	340 mA

TYPE OF SIGNALS

Symbol	Min	Typ	Max	Unit
Tbc	—	14.0	16.6	ms

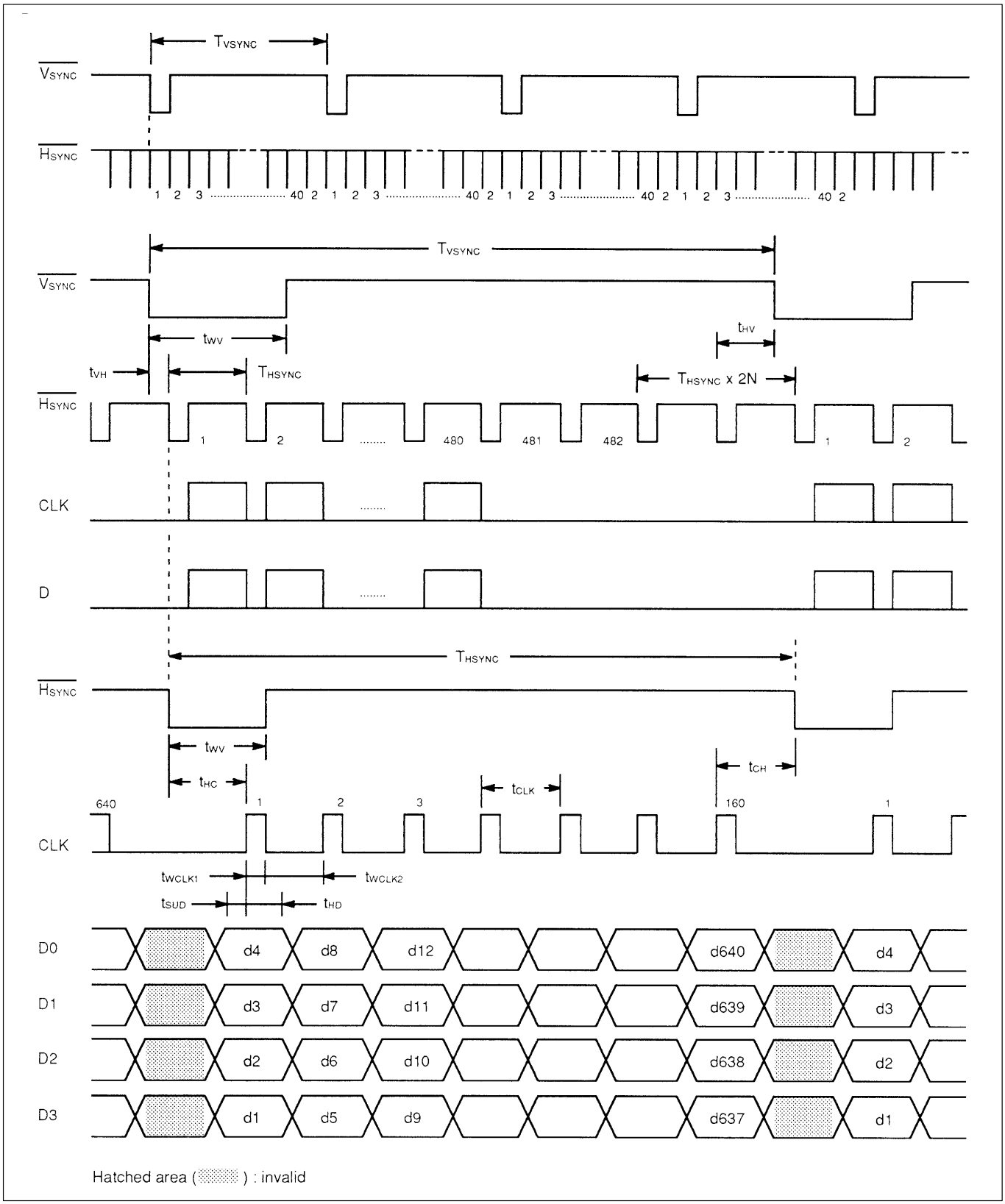


INTERFACE SIGNAL TIMING CHART OF SERIAL DATA INPUT



Hatched area (▒▒▒) : invalid

INTERFACE SIGNAL TIMING CHART OF PARALLEL DATA INPUT



CONNECTORS

Connector for signals: FCN-605Q026-G/S

Mating connector: FCN-607B026-G/D

Pin No.	Symbol	Pin No.	Symbol
1	$\overline{\text{VSYNC}}$	2	S. GND
3	$\overline{\text{HSYNC}}$	4	S. GND
5	N.C. (D0)	6	N.C.
7	N.C. (D1)	8	N.C.
9	N.C. (D2)	10	N.C.
11	N.C. (D3)	12	N.C.
13	N.C.	14	S. GND
15	DATA	16	S. GND
17	N.C.	18	S. GND
19	CLK	20	S. GND
21	B.C.	22	N.C.
23	N.C.	24	N.C.
25	N.C. ($V_{CC)}$	26	N.C. (V_{CC})

Notes: N.C. = No connection
Terminals 25 and 26 output V_{CC} for optionals. No connection with these terminals

Use terminal 15 (DATA) for serial data input
Use terminals 5 (D0), 7 (D1), 9 (D2), and 11 (D3) for parallel data input.

CONNECTORS, continued

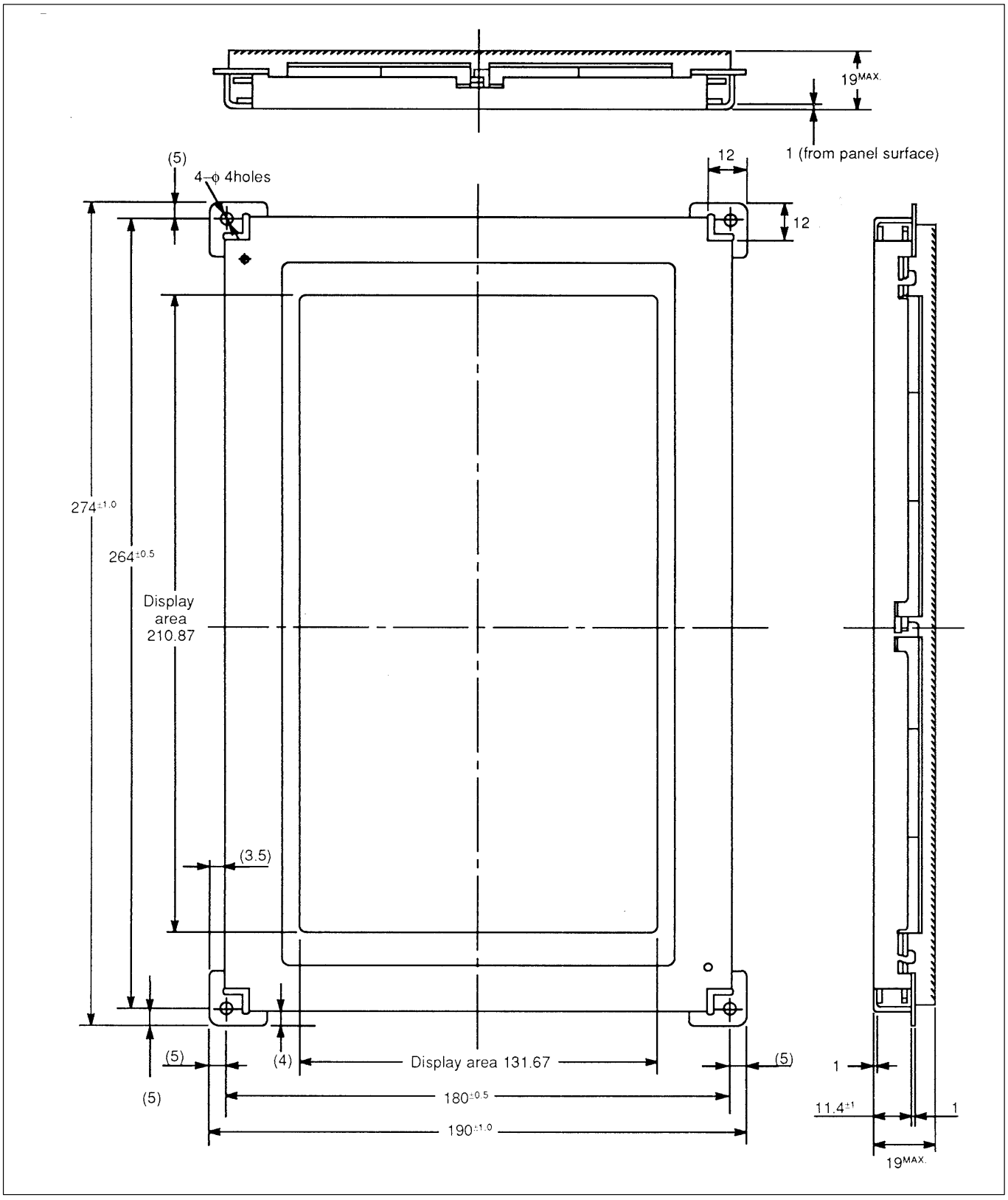
Connector for power supply: FCN-815O009-TA

Mating connectors: FCN-813J009-A, Housing;
FCN-813J-T/Q, contact for manual use
FCN-813J-T/R, contact for automatic use

Pin No.	Symbol
1	V_{CC}
2	GND
3	N.C.
4	GND
5	V_S
6	N.C.
7	N.C.
8	GND
9	V_{R*}

* This PDP unit outputs the voltage V_R from 0 to 2.5 VDC through the ninth terminal of power supply connector. This voltage is used for the supply voltage adjustment of FPF07P series power supply unit.

PACKAGE DIMENSIONS



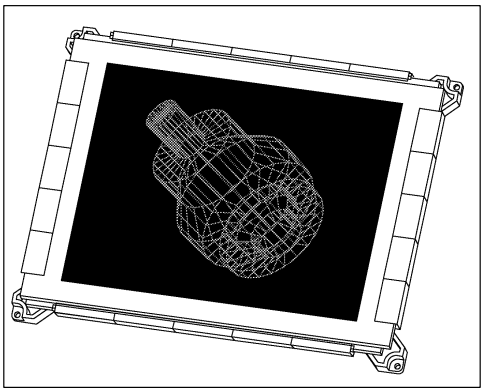
June 1992
Edition 1.0

FUJITSU

DATA SHEET

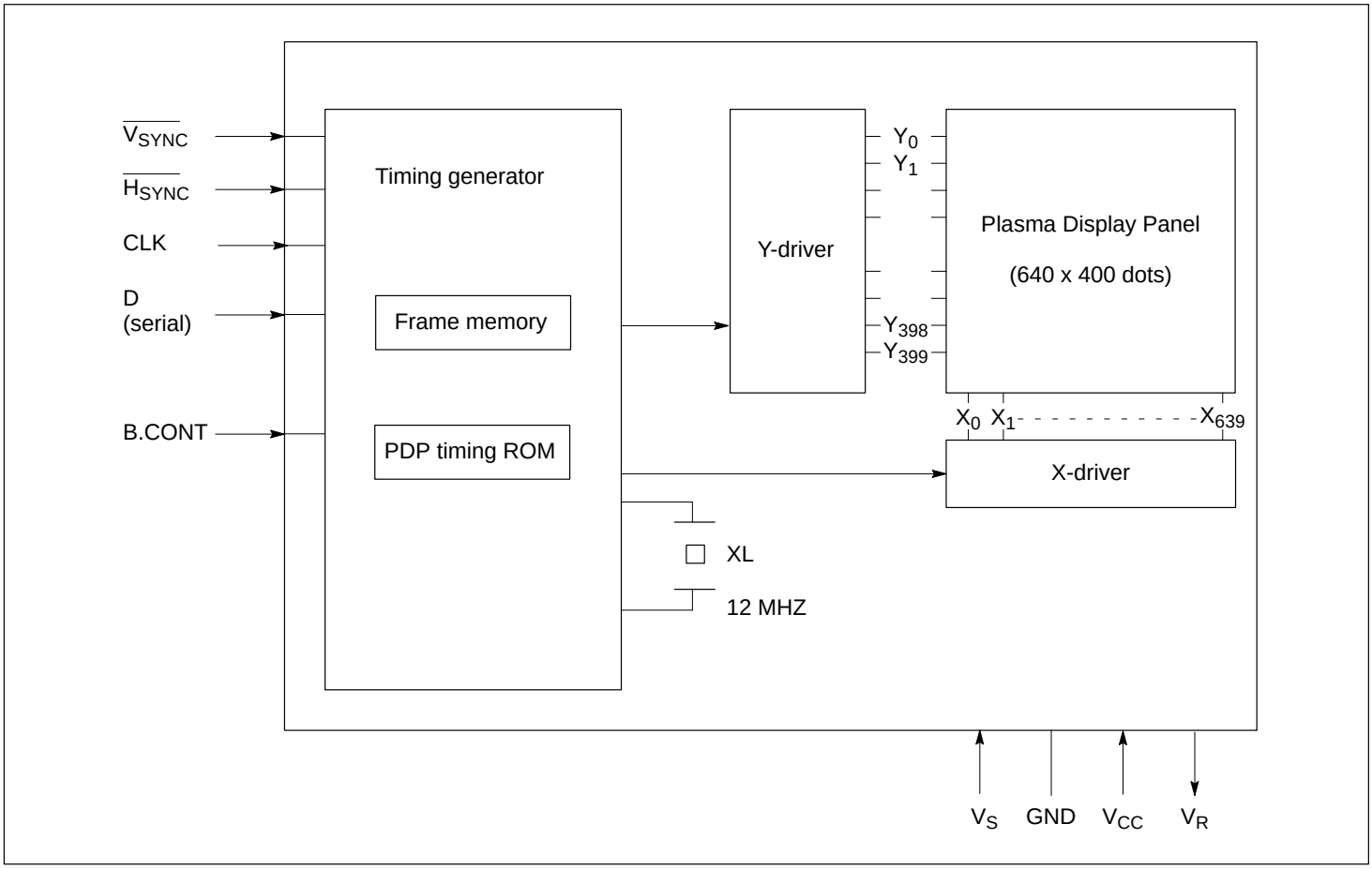
FPF8050HRUD–001
Plasma Display Graphics Unit

The FPF8050HRUD-001 plasma display unit consists of an AC gas discharge plasma display unit with bistable memory and associated driver circuitry. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8050HRUD-001 a highly reliable display device.



- High resolution
- Bright, even, orange-on-black display
- No flicker or warp
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Sustain voltage	V_S	120 V
Logic voltage	V_{CC}	7 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for sustain*	V_S	88	95	100.5	V
Supply current for sustain (V_S = 95 V)	I_S			310	mA
Supply voltage for logic	V_{CC}		5		V
Supply current for logic (V_{CC} = 5 V)	I_{CC}	0.15		0.45	A
Signal input voltage for logic 1	V_{IH}	2.0		5.25	V
Signal input current for logic 1 (V_{IH} = 2.75)	I_{IH}			20	μA
Signal input voltage for logic 0	V_{IL}	-0.5		0.8	V
Signal input current for logic 0 (V_{IL} = 2.75 V)	I_{IL}			-16	mA

Note: * The power source is required to be variable from 88 to 100.5V DC.

MECHANICAL SPECIFICATIONS

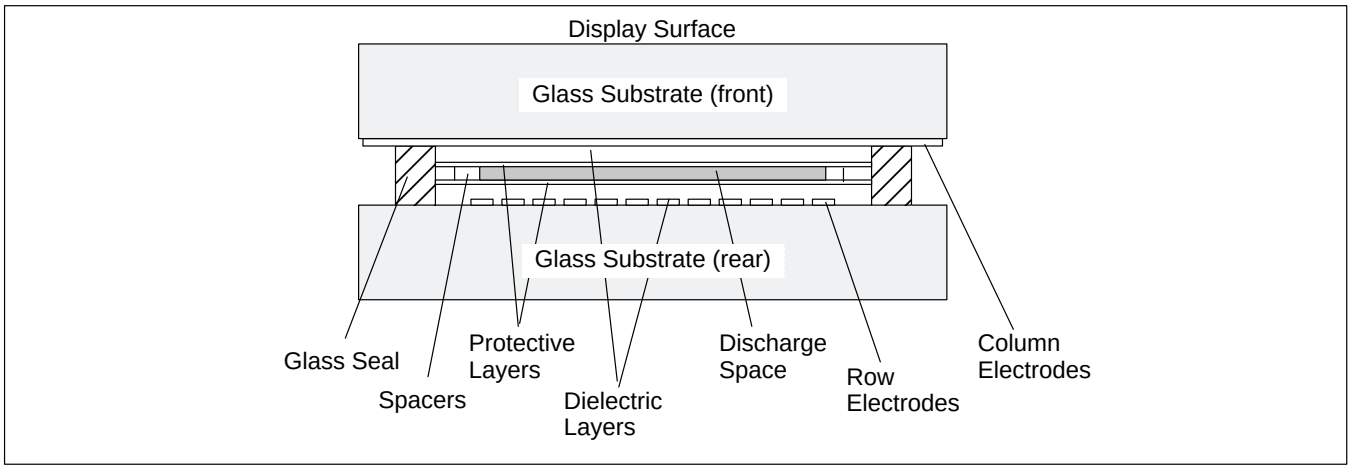
Physical Specifications

Item	Value
Number of display dots	640 × 400 dots (256,000 dots)
Dot pitch	0.3 (H) × 0.3 (V) mm (0.012 × 0.012 in.)
Dot size	0.2 mm (0.008 in.) dia
Effective display area	191.7 (H) × 119.7 (V) mm (7.547 × 4.713 in.)
Display color	Neon orange
Brightness	110 cd/m^2 (Peak) 15 cd/m^2 (Average)
Contrast ratio	20 : 1 min
Viewing angle	160° min
Weight	Approx. 1 kg
External dimensions	See External Dimensions

Performance Specifications

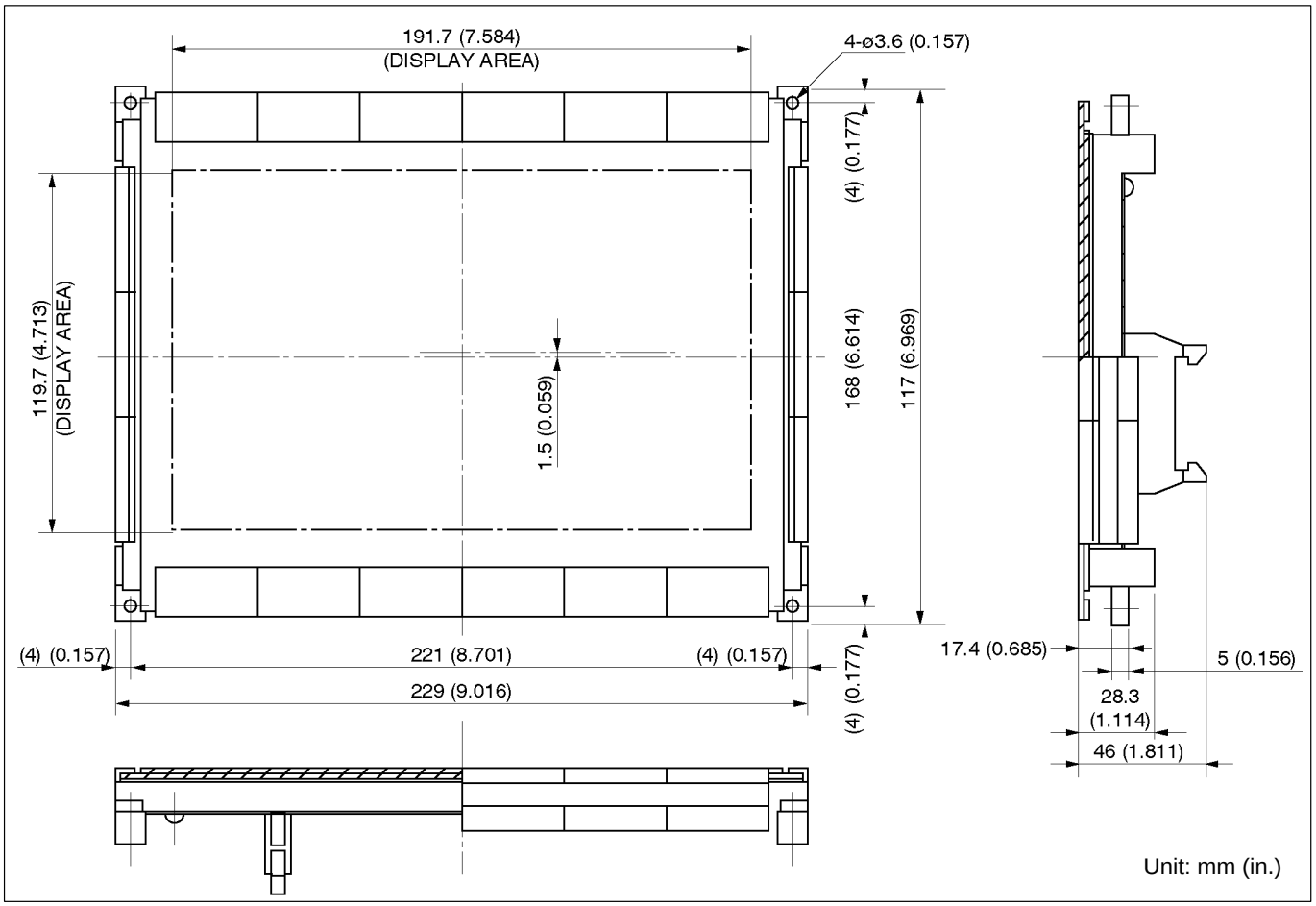
Item	Symbol	Value
Operating temperature	T_{OP}	0 to +50°C
Operation humidity	RH_{OP}	20 to 85%
Storage temperature	T_{STG}	–20 to +70°C
Storage humidity	RH_{STG}	20 to 85%
Vibration	V	2 G
Shock	S	40 G
Pressure (non-operating)		340 to 1114 hPa

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

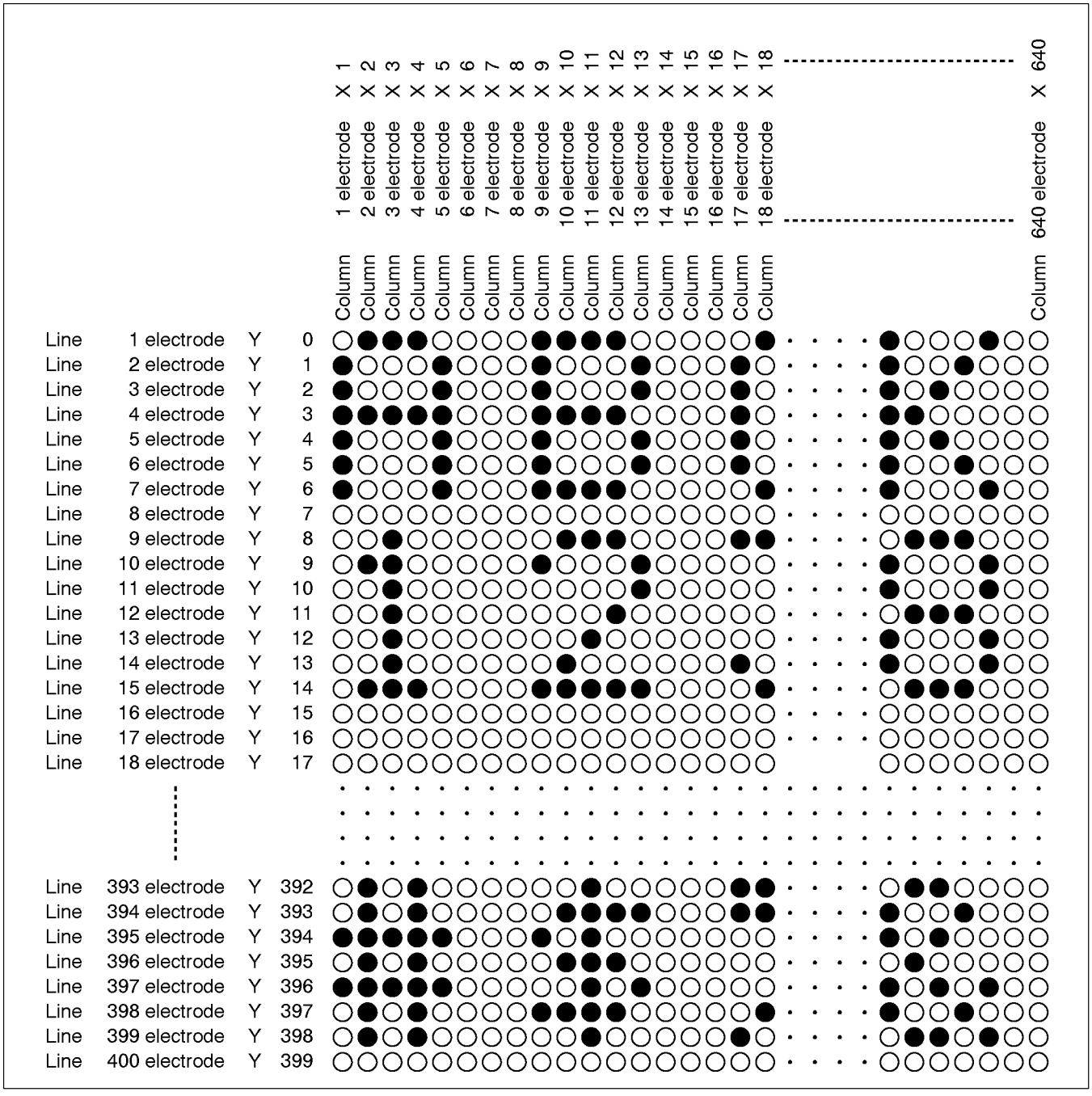


INTERFACE SIGNALS

Type of Signals (TTL Compatible)

Signal	Symbol	Logic	Definition and Function
Display data	D	Posi	Serial display data. Relation between display data and display dots is shown below.
Clock signal	CLK	Posi	The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 640.
Line synchronous	$\overline{H_{SYNC}}$	Nega	The number of $\overline{H_{SYNC}}$ signals in one cycle of $\overline{V_{SYNC}}$ must be 400 or more even numbers.
Frame synchronous	$\overline{V_{SYNC}}$	Nega	The input signal which controls the refresh speed of the screen.
Brightness control	B.CONT	The input signal which controls the screen brightness. Brightness is its maximum at logical “High” and 33% of maximum at logical “Low.”	

Relationship Between Display Data and Display Dots



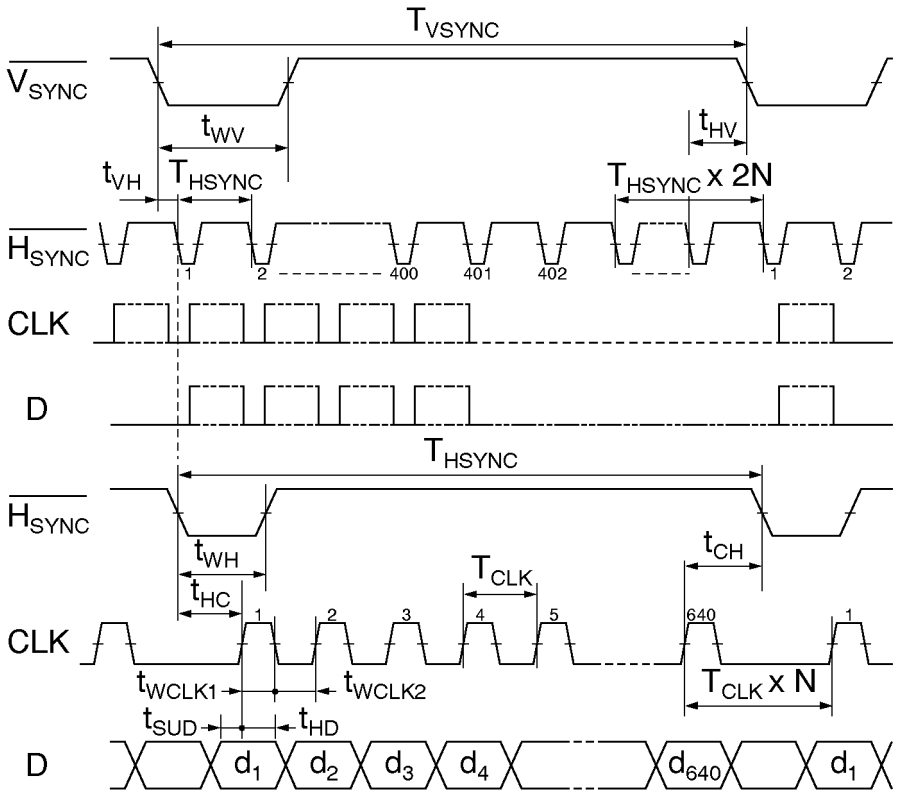
Interface Signal Timing Table

Symbol	Min.	Typ.	Max.	Unit
T_{VSYNC}	—	39.6	—	ms
t_{WV}	T_{HSYNC}	—	—	µs
t_{VH}	1	—	—	µs
t_{HV}	2	—	—	µs
T_{HSYNC}[1]	88	90	92	µs
t_{WH}	2	6	—	µs
t_{HC}	2	—	—	µs
t_{CH}	2	3	—	µs
T_{CLK}	44	—	—	ns
$t_{WCLK1,2}$[2]	22	—	—	ns
t_{SUD}	22	—	—	ns
t_{HD}	22	—	—	ns

Notes: [1] T_{HSYNC} ranges from 40 to 45 µs and from 60 to 65 µs are also available. In these cases, brightness control range changes.

[2] Recommended ratio between t_{WCLK1} and t_{WCLK2} is 1 : 1.

Interface Signal Timing Chart



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-604Q26-G/S (Fujitsu)

Pin No.	Signal	Pin No.	Signal
1	$\overline{V_{SYNC}}$	2	S.GND
3	$\overline{H_{SYNC}}$	4	S.GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S.GND
15	D	16	S.GND
17	N.C.	18	S.GND
19	CLK	20	S.GND
21	B.CONT	22	N.C.
23	N.C.	24	N.C.
25	V_{CC}	26	V_{CC}

Applicable connector:
FCN-607B026-G/D

Power Supply Connector

FCN-814P009-TA (Fujitsu)

Pin No.	Signal
1	V_{CC}
2	GND (L)
3	N.C.
4	GND (H)
5	V_S
6	N.C.
7	N.C.
8	N.C.
9	V_R*

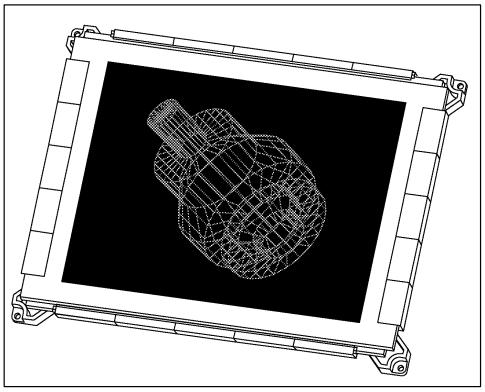
Applicable connectors:
FCN-813J009-A housing (Fujitsu)
FCN-813J-T/A contact (Fujitsu)

* This terminal is connected only when FPF07P-AC100 power supply unit is used.

June 1992
Edition 1.0

DATA SHEET

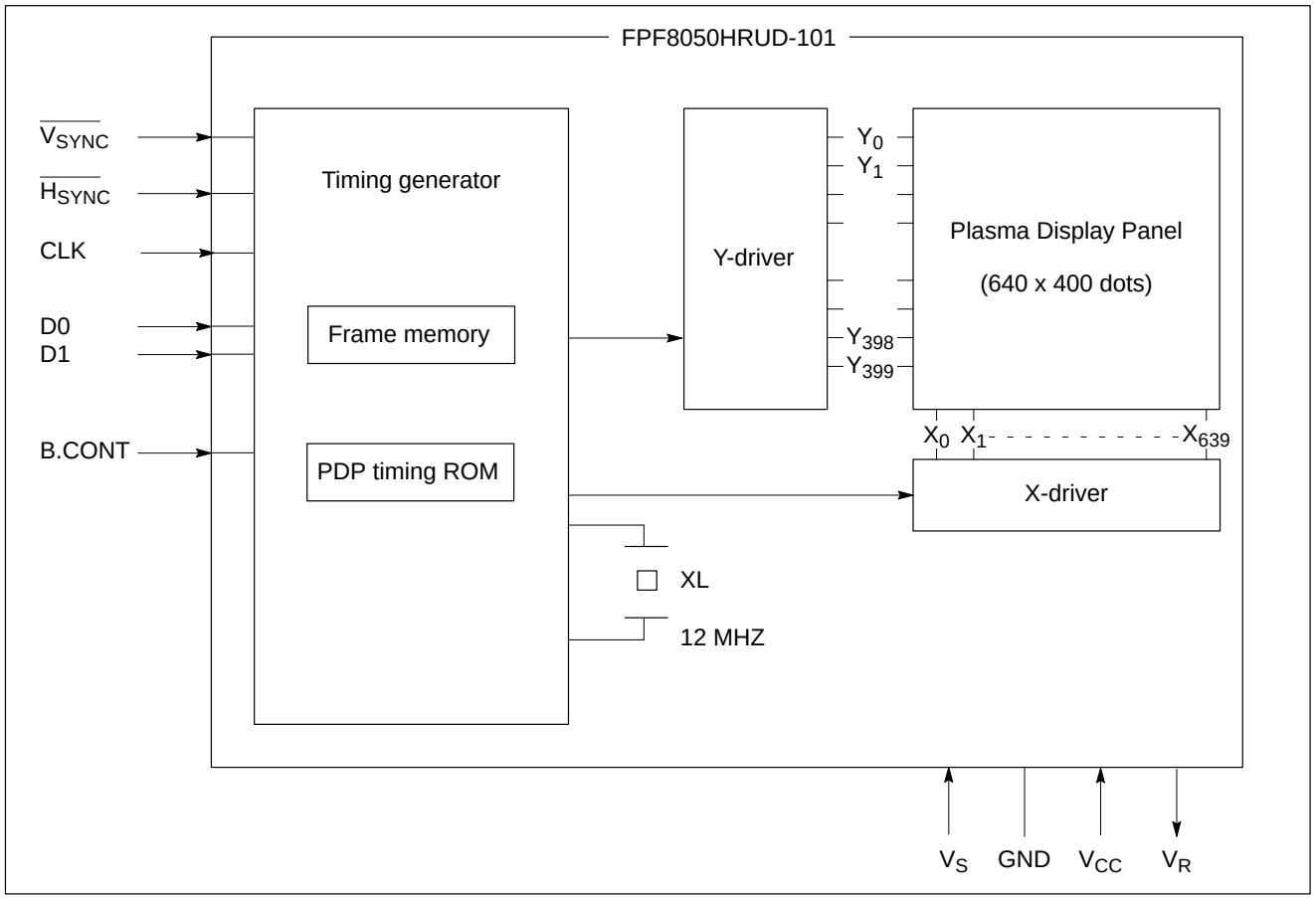
FPF8050HRUD–101
Plasma Display Graphics Unit



The FPF8050HRUD-101 plasma display graphics unit consists of an AC gas discharge plasma display panel with bistable memory and associated driver circuitry. Fujitsu's proprietary control method provides a clear display with a four-level gray scale. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8050HRUD-101 a highly reliable display device.

- Bright, even, orange-on-black display
- Four-level gray scale
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Sustain voltage	V_S	120 V
Logic voltage	V_{CC}	7 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for sustain*	V_S	88	95	100.5	V
Supply current for sustain (V_S = 95 V)	I_S			310	mA
Supply voltage for logic	V_{CC}		5		V
Supply current for logic (V_{CC} = 5 V)	I_{CC}	0.15		0.50	A
Signal input voltage for logic 1	V_{IH}	2.0		5.25	V
Signal input current for logic 1 (V_{IH} = 2.75)	I_{IH}			20	µA
Signal input voltage for logic 0	V_{IL}	–0.5		0.8	V
Signal input current for logic 0 (V_{IL} = 2.75)	I_{IL}			–16	mA

Note: *The power source is required to be variable from 88 to 100.5V DC.

MECHANICAL SPECIFICATIONS

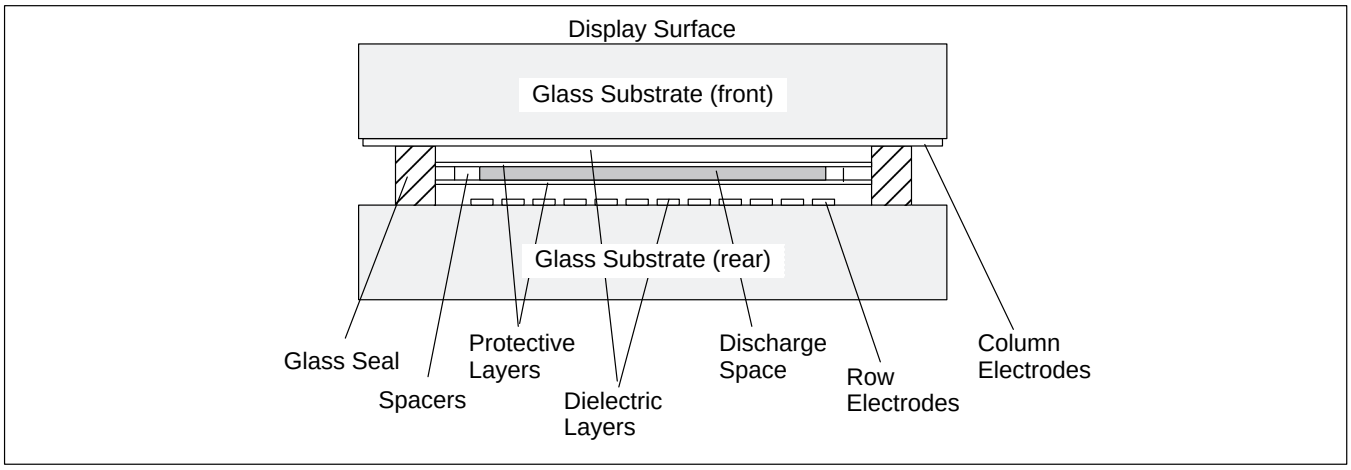
Physical Specifications

Item	Value
Number of display dots	640 × 400 dots (256,000 dots)
Dot pitch	0.3 (H) × 0.3 (V) mm (0.012 × 0.012 in.)
Dot size	0.2 mm (0.008 in.) dia
Effective display area	191.7 (H) × 119.7 (V) mm (7.547 × 4.713 in.)
Display color	Neon orange
Gray scale	4-level (Approx. 100%, 67%, 33%, 0%)
Brightness	110 cd/m^2 (Peak)
Contrast ratio	20 :1 min
Viewing angle	160° min
Weight	Approx. 1 kg
External dimensions	See External Dimensions

Performance Specifications

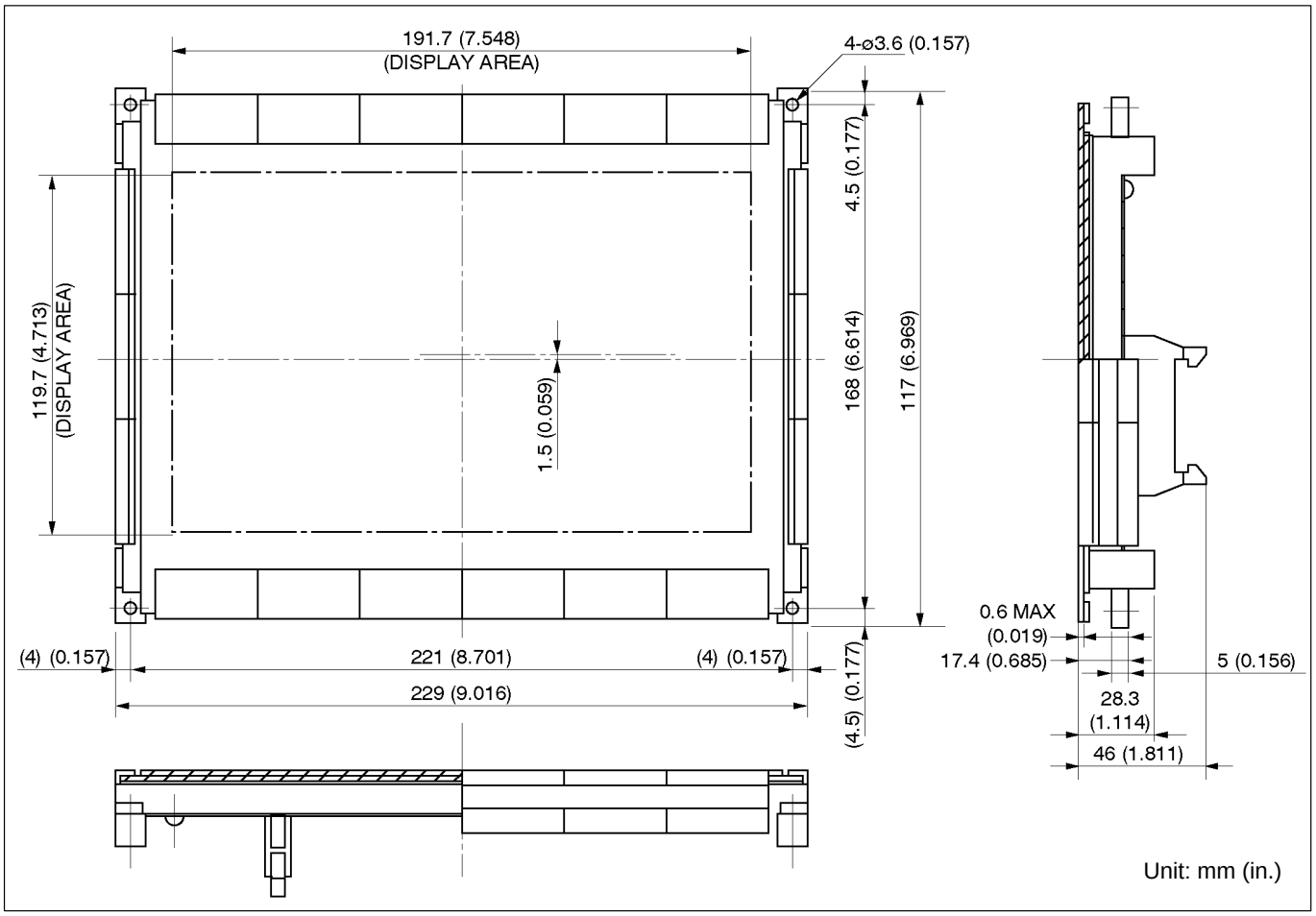
Item	Symbol	Value
Operating temperature	T_{OP}	0 to +50°C
Operation humidity	RH_{OP}	20 to 85%
Storage temperature	T_{STG}	–20 to +70°C
Storage humidity	RH_{STG}	20 to 85%
Vibration	V	2 G
Shock	S	40 G
Pressure (non-operating)		340 to 1114 hPa

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

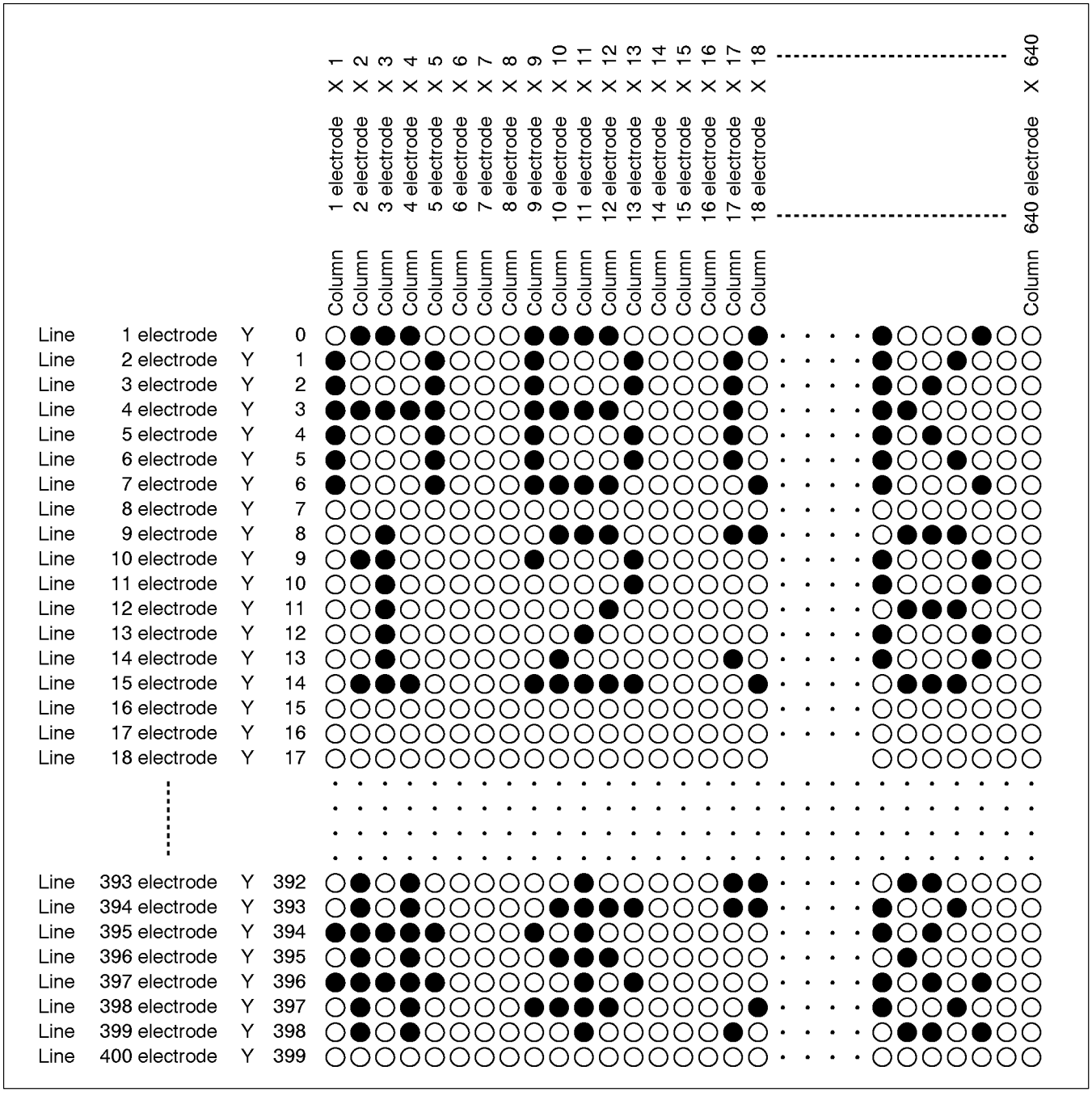


INTERFACE SIGNALS

Type of Signals (TTL Compatible)

<table>
<tr><th>Signal</th><th>Symbol</th><th>Logic</th><th>Definition and Function</th></tr>
<tr><td>Display data</td><td>D0
D1</td><td>Posi</td><td>2-bit display data.
Relationship between data and gray scale level is shown below.
<table>
<tr><th>D1</th><th>D0</th><th>Gray scale level</th><th>(Relative brightness)</th></tr>
<tr><td>0</td><td>0</td><td></td><td>(0)</td></tr>
<tr><td>0</td><td>1</td><td>Low</td><td>(33%)</td></tr>
<tr><td>1</td><td>0</td><td>Medium</td><td>(67%)</td></tr>
<tr><td>1</td><td>1</td><td>High</td><td>(100%)</td></tr>
</table></td></tr>
<tr><td>Clock signal</td><td>CLK</td><td>Posi</td><td>The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 640.</td></tr>
<tr><td>Line synchronous</td><td>$\overline{H_{SYNC}}$</td><td>Nega</td><td>The number of $\overline{H_{SYNC}}$ signals in one cycle of $\overline{V_{SYNC}}$ must be 402 or more even numbers.</td></tr>
<tr><td>Frame synchronous</td><td>$\overline{V_{SYNC}}$</td><td>Nega</td><td>The input signal which controls the refresh speed of the screen.</td></tr>
<tr><td>Brightness control</td><td>B.CONT</td><td colspan="2">The input signal which controls the screen brightness. Brightness is its maximum at logical “High” and 33% of maximum at logical “Low.”</td></tr>
</table>

Relationship Between Display Data and Display Dots



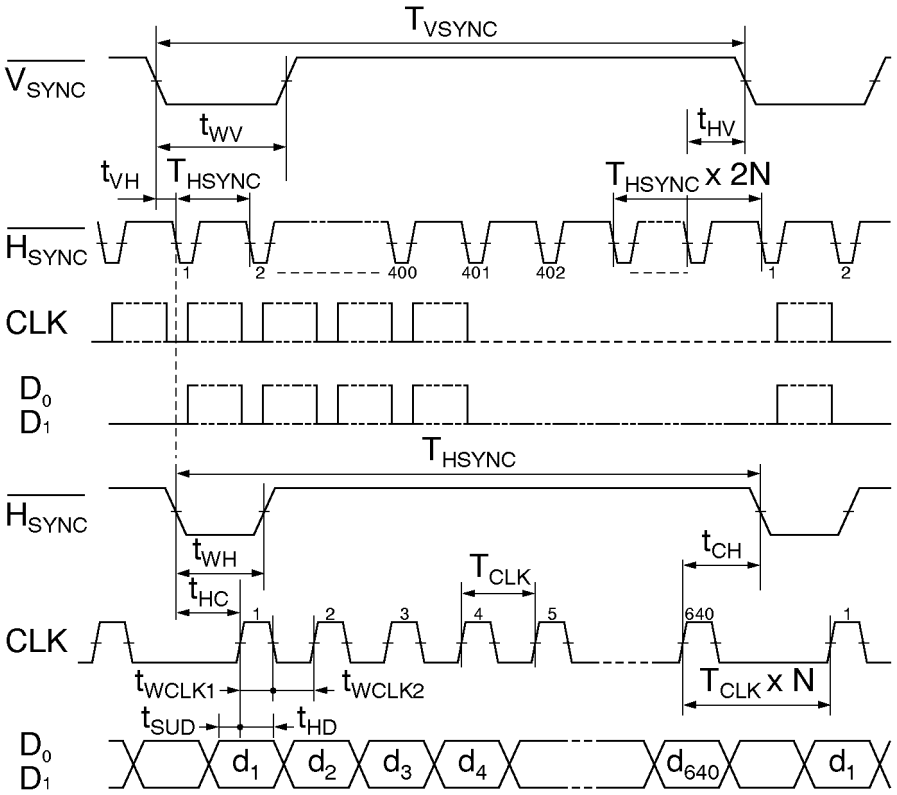
Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit
T_{VSYNC}	—	16.7	20	ms
t_{WV}[1]	—	—	—	µs
t_{VH}	1	—	—	µs
t_{HV}	2	—	—	µs
T_{HSYNC}	40	42	45	µs
t_{WH}	2	5	—	µs
t_{HC}	2	—	—	µs
t_{CH}	2	3	—	µs
T_{CLK}	44	—	—	ns
$t_{WCLK1,2}$[2]	22	—	—	ns
t_{SUD}	22	—	—	ns
t_{HD}	22	—	—	ns

Notes: [1] $T_{WV} > T_{HSYNC}$

[2] Recommended ratio between t_{WCLK1} and t_{WCLK2} is 1 : 1.

Interface Signal Timing Chart



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-604Q26-G/S (Fujitsu)

Pin No.	Signal	Pin No.	Signal
1	$\overline{V_{SYNC}}$	2	S.GND
3	$\overline{H_{SYNC}}$	4	S.GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S.GND
15	D0	16	S.GND
17	D1	18	S.GND
19	CLK	20	S.GND
21	B.CONT	22	N.C.
23	N.C.	24	N.C.
25	V_{CC}	26	V_{CC}

Applicable connector:
FCN-607B026-G/D

Power Supply Connector

FCN-814P009-TA (Fujitsu)

Pin No.	Signal
1	V_{CC}
2	GND (L)
3	N.C.
4	GND (H)
5	V_S
6	N.C.
7	N.C.
8	N.C.
9	V_R*

Applicable connectors:
FCN-813J009-A housing (Fujitsu)
FCN-813J-T/A contact (Fujitsu)

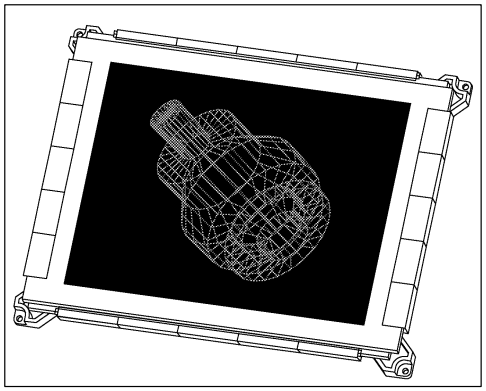
* This terminal is connected only when FPF07P-AC100 power supply unit is used.

August 1990
Edition 1.0

FUJITSU

DATA SHEET

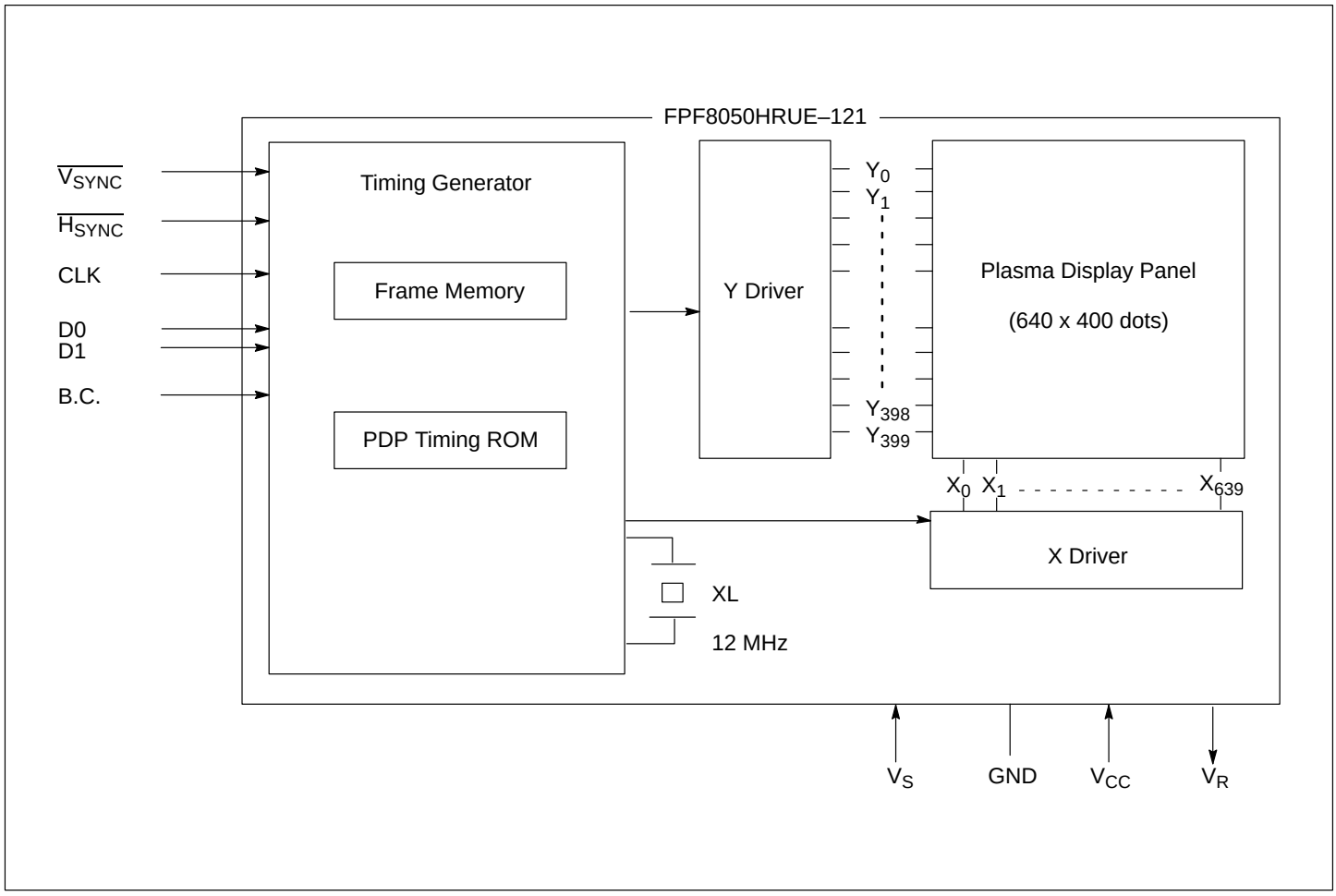
FPF8050HRUE–121
Plasma Display Unit



The FPF8050HRUE-121 plasma graphics display unit consists of an AC gas discharge plasma display panel with bistable memory and associated driver circuitry. Fujitsu's proprietary control method provides a clear display with a 4-level gray scale. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8050HRUE-121 a highly reliable display device.

- Bright, even, orange-on-black display
- Four-level gray scale
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Supply Voltage for Sustain	V_S	+120 V
Supply Voltage for Logic	V_{CC}	+7 V

DC Characteristics

	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
For Display	Voltage	V_S	Variable[1,2]	88	95	100.5	V
	Ripple/Noise	V_{NRS}	At Resistive Load	—	—	500	mV
	Stability (Average)	—	At Resistive Load	—	—	±1.5	%
	Set-up Stability	—	Tolerance of equation in Note 2	—	—	±0.5	%
	Stability (Peak)	—	(I_S = 2 A)	—	—	-5	%
	Current (Average)[3,4,5]	I_S	T_{HSYNC} = 42 µs/H T_{HSYNC} = 34 µs/H	50 50	150 150	270 325	mA
	Current (Peak)	I_{SP}	1 µs width at I_{SP} = 1 A and 5 to 8 µs cycle	0.5	—	2	A
For Logic	Voltage	V_{CC}		4.75	5	5.25	V
	Ripple/Noise	V_{NRC}	At Resistive Load	—	—	200	mV
	Stability	—	At Resistive Load	—	—	±5	%
	Current (Average)	I_{CC}		150	250	500	mA

Notes: [1] A variable power supply is required for voltage V_S (for display) because each display unit requires a specific voltage within range specified in the above table.

[2] The specific voltage for V_S is indicated on each display unit. However, when V_R (reference voltage) is used, it adjusts the specified voltage automatically. Each display unit outputs a specific V_R voltage corresponding to the V_S voltage required by that display unit. The relationship between V_S and V_R is as follows:

$V_S = 88 + V_R \times 5$ (V)

Example: V_S = 93 V → V_R = 2.0 V

[3] Current I_S is specified at condition below:

(1) Minimum displayed ratio = 0%

(2) Typical displayed ratio = 33% (Character “B” is displayed on white screen)

(3) Maximum displayed ratio = 100%

[4] The I_S value in the table above is the value at the 42 µs and 34 µs cycle period of $\overline{H_{SYNC}}$. The I_S value changes corresponding to the cycle period of $\overline{H_{SYNC}}$.

[5] Current I_S is 0 mA under following conditions:

(1) When V_{CC} is not supplied.

(2) During the period of three frames after V_{CC} begins to be supplied. (Operation starts after three pulses of $\overline{V_{SYNC}}$ are input).

(3) When $\overline{H_{SYNC}}$ is not input.

(4) When CLK is not input.

MECHANICAL SPECIFICATIONS

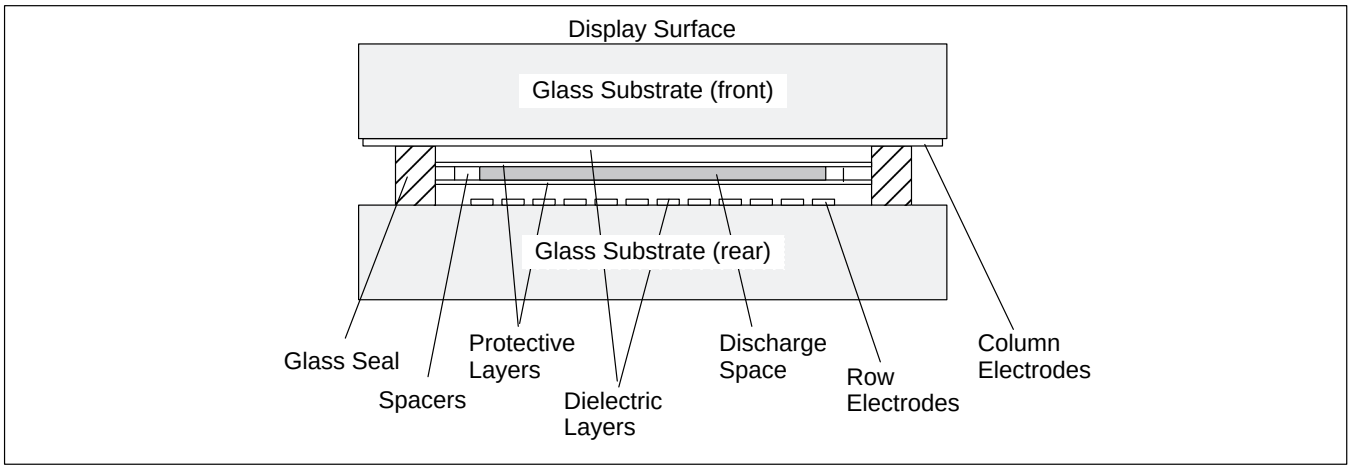
Physical Specifications

Item	Value
Number of Display Dots	640 (H) × 400 (V) dots (256,000 dots)
Dot Pitch	0.3 (H) mm × 0.3 (V) mm (0.012 in. × 0.012 in.)
Dot Size	Approximately 0.2 mm (0.008 in.) dia.
Display Resolution	85 dpi
Effective Screen Area	191.7 (H) mm × 119.7 (V) mm (7.547 in. × 4.713 in.)
Gray Scale	4 levels Approximately 100%, 67%, 33%, and 0%
Display Color	Neon orange
Dot Brightness (peak) (plane average)	110 cd/m^2 (43.5 fL) at maximum brightness level 15 cd/m^2 (5.9 fL)
Brightness Control	Variable from 0 to 100% by brightness control signal
Contrast Ratio	1:20 (min.)
Viewing Angle	160° (min.)
Brightness Unevenness	30% (max.)
Weight	Approximately 900 g

Performance Specifications

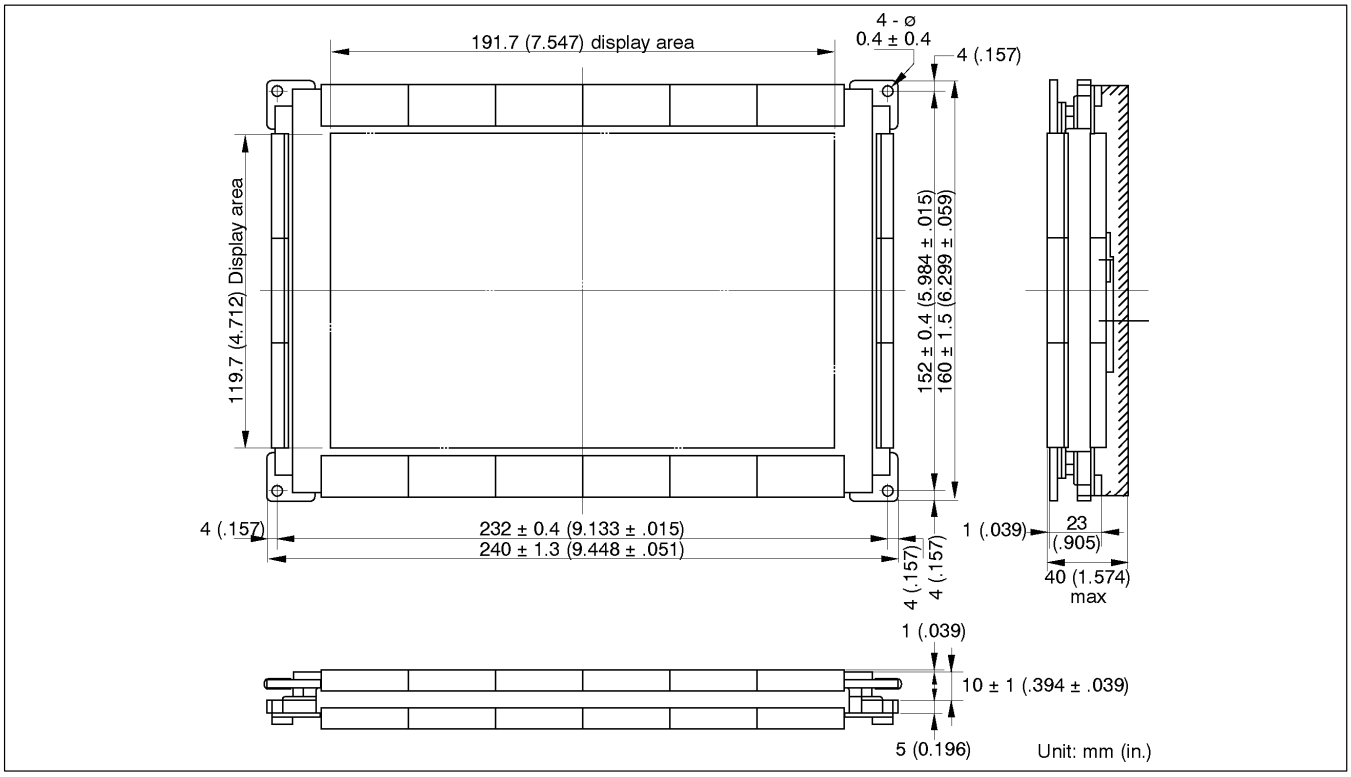
Item	Value
Vibration Frequency: Acceleration: Time:	 10 to 55 Hz 2 G (max.) Operation: 5 min in X, Y, and Z direction Non-Operation: 2 hr. in X, Y, and Z direction
Shock Acceleration: Time:	 40 G (max.) in X and Y direction 20 G (max.) in Z direction 11 ms (max.)
Operating Temperature	0°C to +50°C
Storage Temperature	-20°C to +70°C
Humidity	20 to 80% RH (no condensation)
Atmospheric Pressure Durability	Operation: 70,000 to 111,400 Pa (1 Pa = 1.403 e–3 psi) Non-Operation: 34,000 to 111,400 Pa

Physical Construction and Operation

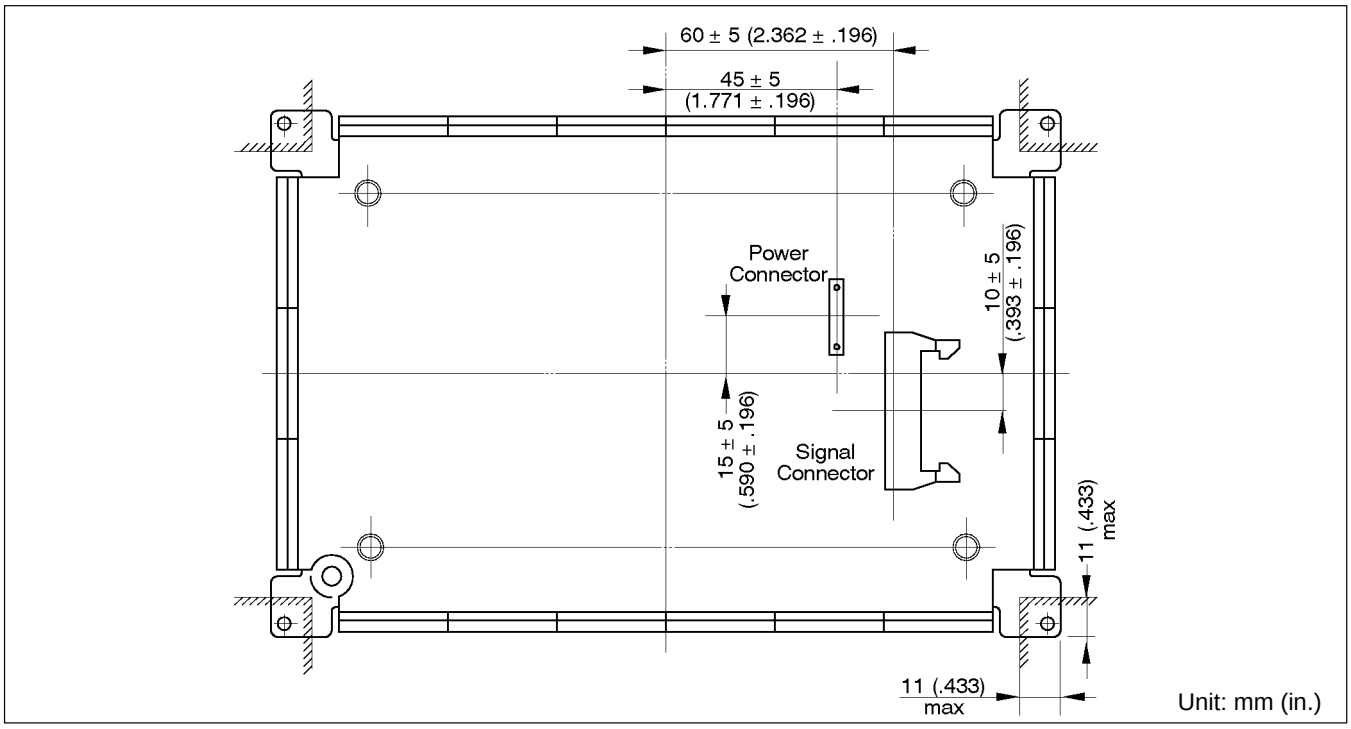


The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

Plasma Display External Dimensions



Connector External Dimensions

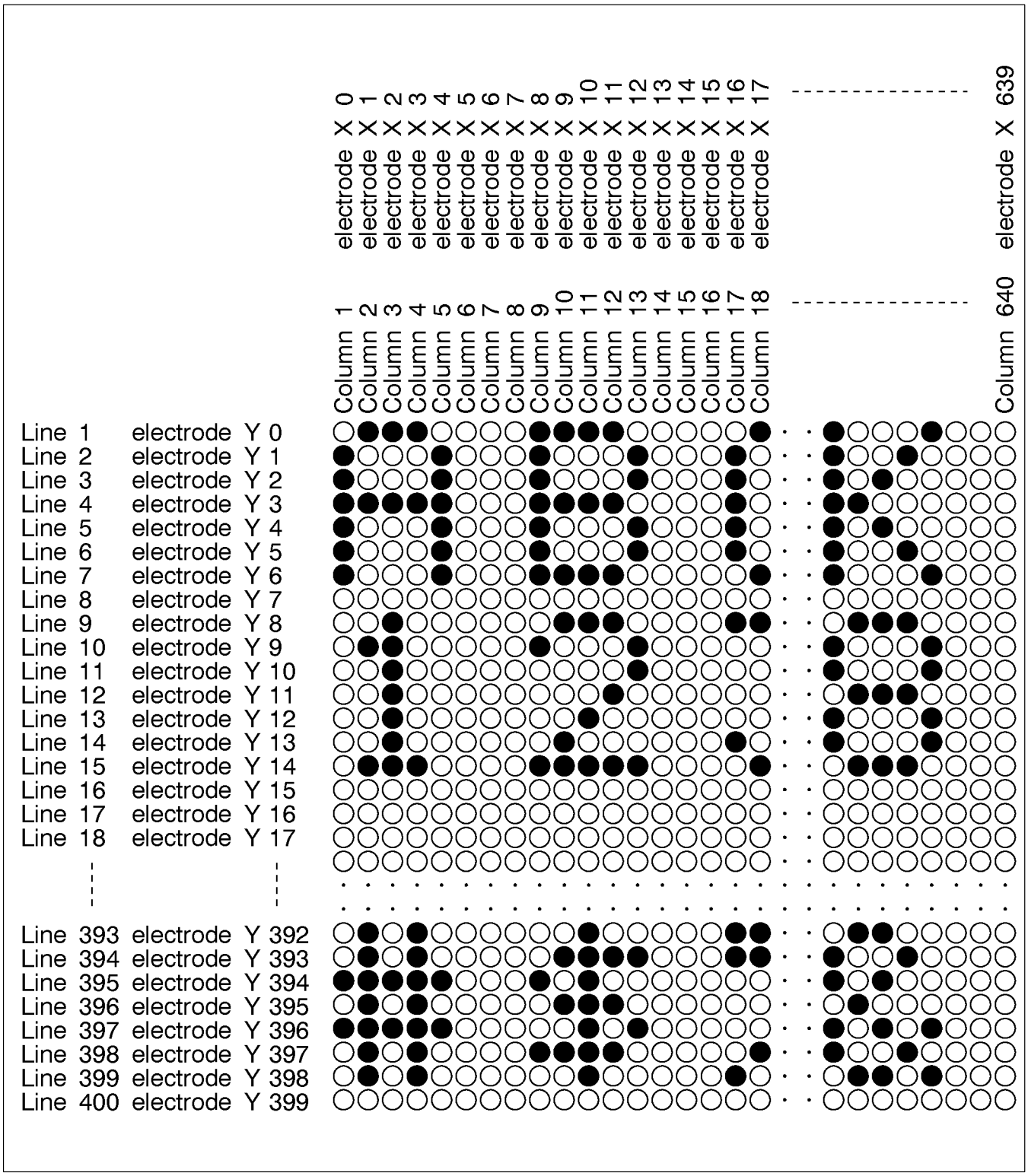


INTERFACE SIGNALS

Type of Signals (TTL Compatible)

<table>
<tr><th>Signal</th><th>Symbol</th><th>Signal Line</th><th>Definition and Function</th></tr>
<tr><td>Data Signal</td><td>D0
D1</td><td>2 Lines</td><td>Signal for 2 bits display data. Logic: H = Light On, L = Light Off. The figure on the following page shows the relationship between display data and display dots.
Relationship Between Display Data and Gray Scale Level
<table>
<tr><th>D1</th><th>D0</th><th>Gray Scale Level</th><th>(Relative Brightness)</th></tr>
<tr><td>0</td><td>0</td><td></td><td>0%</td></tr>
<tr><td>0</td><td>1</td><td>low</td><td>(33%)</td></tr>
<tr><td>1</td><td>0</td><td>medium</td><td>(67%)</td></tr>
<tr><td>1</td><td>1</td><td>high</td><td>(100%)</td></tr>
</table></td></tr>
<tr><td>Clock Signal</td><td>CLK</td><td>1 Line</td><td>The input signal which controls the input timing of the display data. The dot data is read into the shift register at the rising edge of each signal.
The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 640.</td></tr>
<tr><td>Horizontal Synchronous Signal</td><td>$\overline{H_{SYNC}}$</td><td>1 Line</td><td>The input signal which controls the scanning timing of the line electrode. Y address increment to select the next line electrode is done at the falling edge of each signal. The number of $\overline{H_{SYNC}}$ signals during the period $\overline{V_{SYNC}}$ must be 402 or more even numbers. This signal is input continuously at a constant interval.</td></tr>
<tr><td>Vertical Synchronous Signal</td><td>$\overline{V_{SYNC}}$</td><td>1 Line</td><td>The input signal which controls the refresh speed of the screen. The scanning position returns to the first electrode (home position) at the falling edge of the $\overline{V_{SYNC}}$ signal.</td></tr>
<tr><td>Brightness Control Signal</td><td>B.C.</td><td>1 Line</td><td>The input signal which controls the screen brightness. Brightness is at its maximum at logic high, and 0% of the maximum at logic low.</td></tr>
</table>

Relationship Between Display Data and Display Dots



INTERFACE SIGNALS

Type of Signals (TTL Compatible)

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The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 640.</td></tr>
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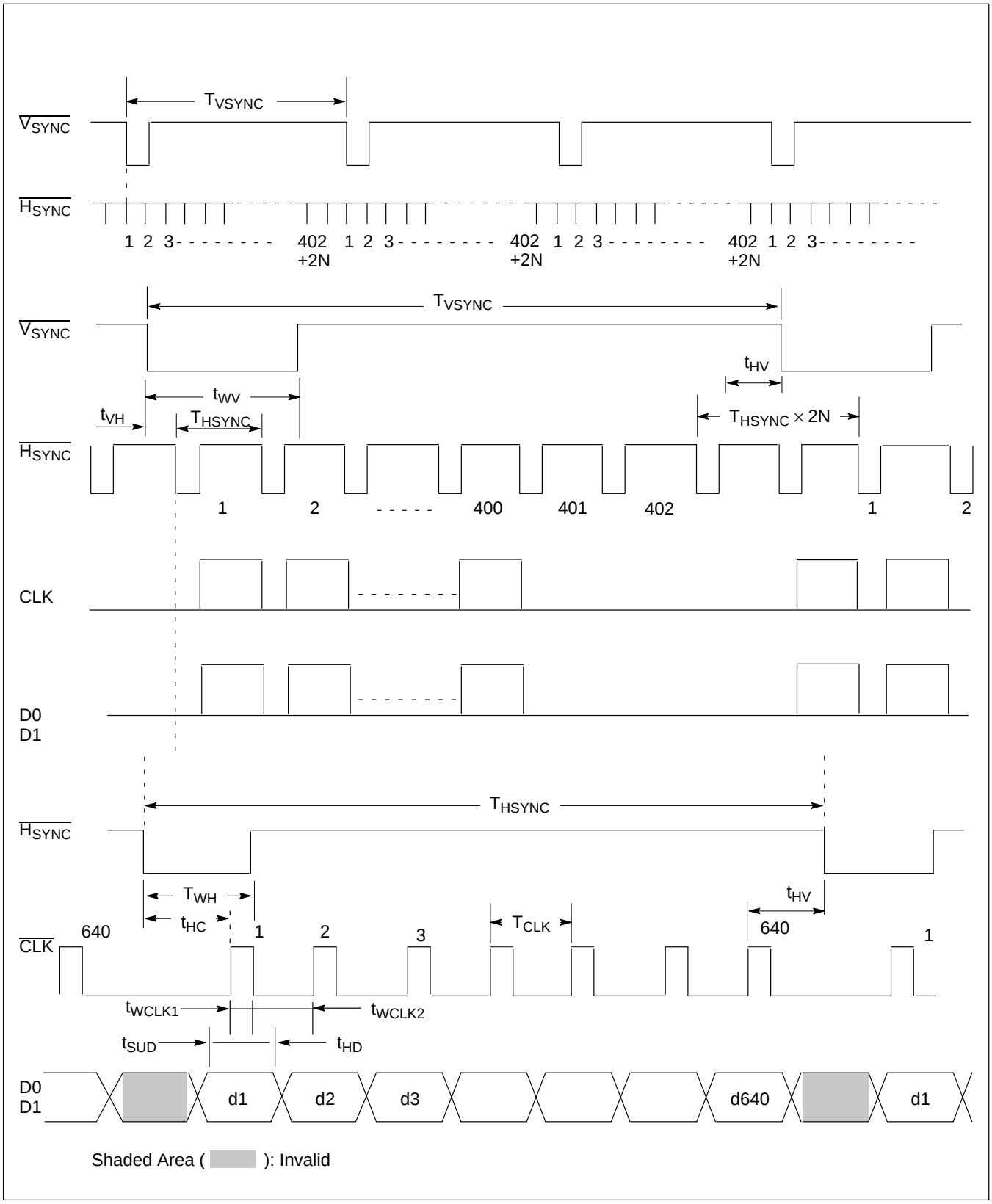
<tr><td>Vertical Synchronous Signal</td><td>$\overline{V_{SYNC}}$</td><td>1 Line</td><td>The input signal which controls the refresh speed of the screen. The scanning position returns to the first electrode (home position) at the falling edge of the $\overline{V_{SYNC}}$ signal.</td></tr>
</table>

Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}		16.7	20	ms	Frame Frequency: 60 Hz
t_{WV}	1			H	H: Cycle of Horizontal Sync. Signal
t_{VH}	1			µs	
t_{HV}	2			µs	
T_{HSYNC}	35	42	45	µs	
t_{WH}	2	5		µs	
t_{HC}	2			µs	
t_{CH}	2	3		µs	
T_{CLK}	34			ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{WCLK1}	22			ns	
t_{WCLK2}	22			ns	
t_{SUD}	22			ns	
t_{HD}	22			ns	

Interface Signal Timing Chart



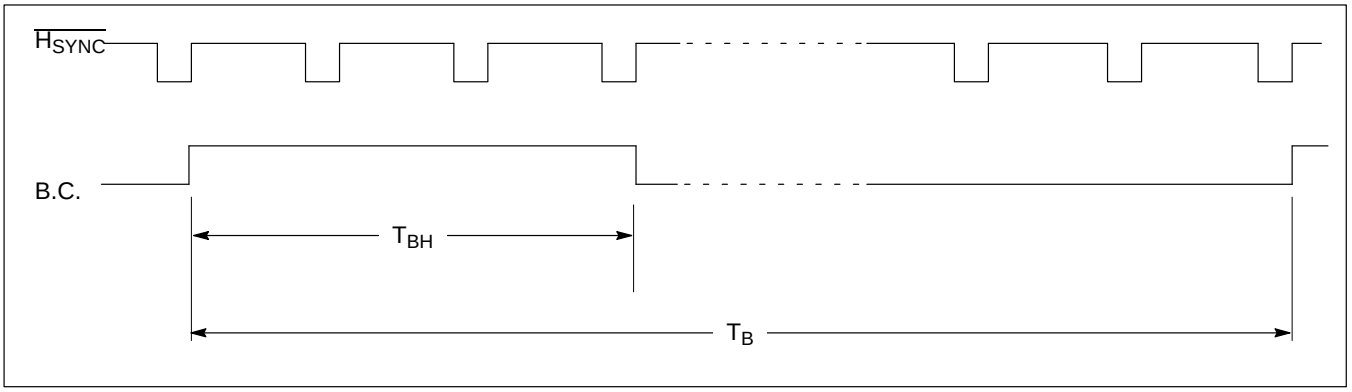
Brightness Control Signal Timing

The brightness of the screen is controlled by the pulse form of the brightness control (B.C.) signal. Brightness varies with the duty cycle of the B.C. signal. Pulse condition and timing are shown below.

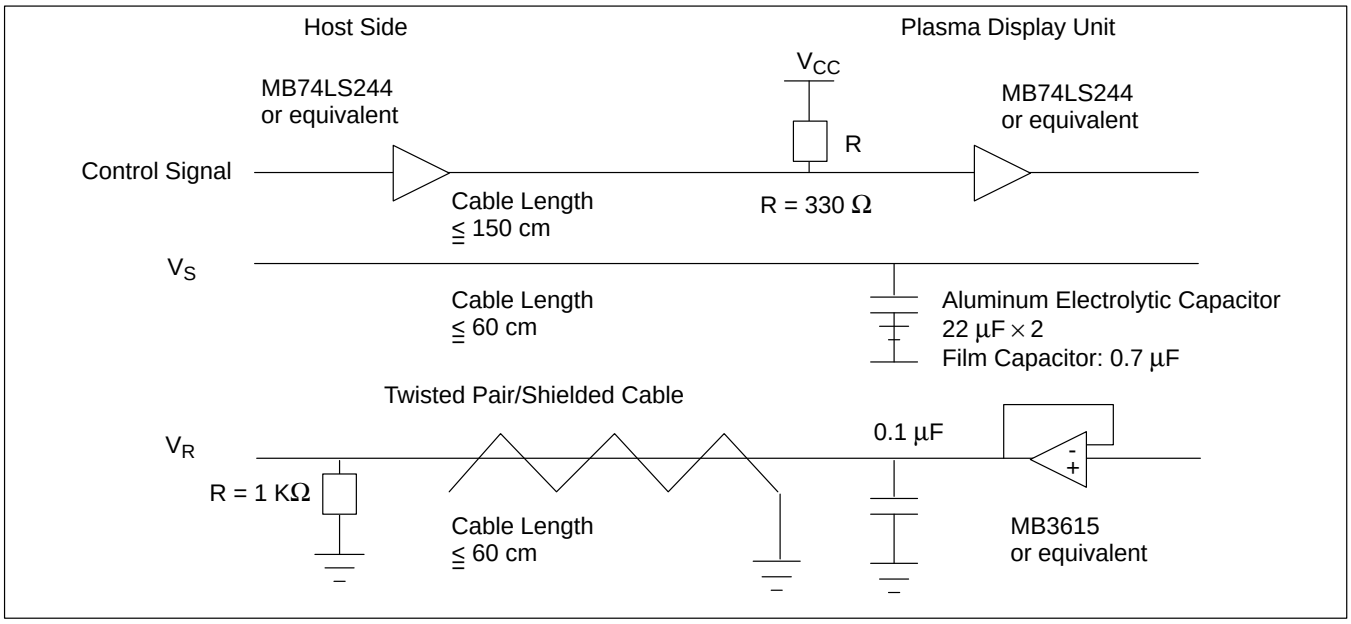
Symbol	Min.	Typ.	Max.	Unit	
T_B	—	$2 \times V/N$	—	H	H: A Cycle of H_{SYNC} Signal
T_{BH}	—	—	$2 \times V/N$	H	

Notes: V: A cycle of $\overline{V_{SYNC}}$/A Cycle of $\overline{H_{SYNC}}$
N: Integer

Brightness Control Signal Timing Chart



Interface Circuit



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-605Q026-G/S (Fujitsu)

Pin No.	Signal	Pin No.	Signal
1	$\overline{V_{SYNC}}$	2	S.GND
3	$\overline{H_{SYNC}}$	4	S.GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S.GND
15	D0	16	S.GND
17	D1	18	S.GND
19	CLK	20	S.GND
21	B.C.	22	N.C.
23	N.C.	24	N.C.
25	V_{CC}	26	V_{CC}

Note: Applicable connector:
FCN-607B026-G/C

Power Supply Connector

FCN-815P009-TA (Fujitsu)

Pin No.	Signal
1	V_{CC}
2	GND
3	N.C.
4	GND
5	V_S
6	N.C.
7	N.C.
8	GND
9	V_R

Notes: This PDP unit outputs the voltage V_R from 0 to 2.5 VDC through the ninth terminal of the power supply connector. This supply voltage is used for the supply voltage adjustment of FPF07P-AC100.

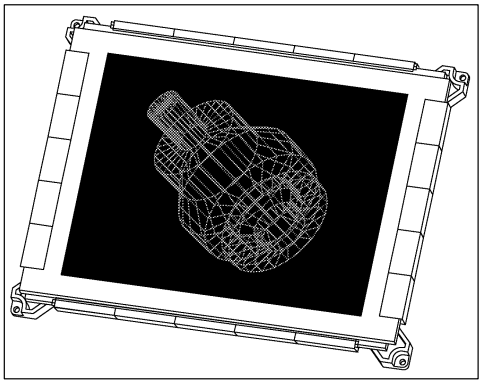
Applicable connectors:
FCN-813J009-A housing
FCN-813J-T/Q contact for hand tool
FCN-813J-T/R contact for auto

August 1990
Edition 1.0

FUJITSU

DATA SHEET

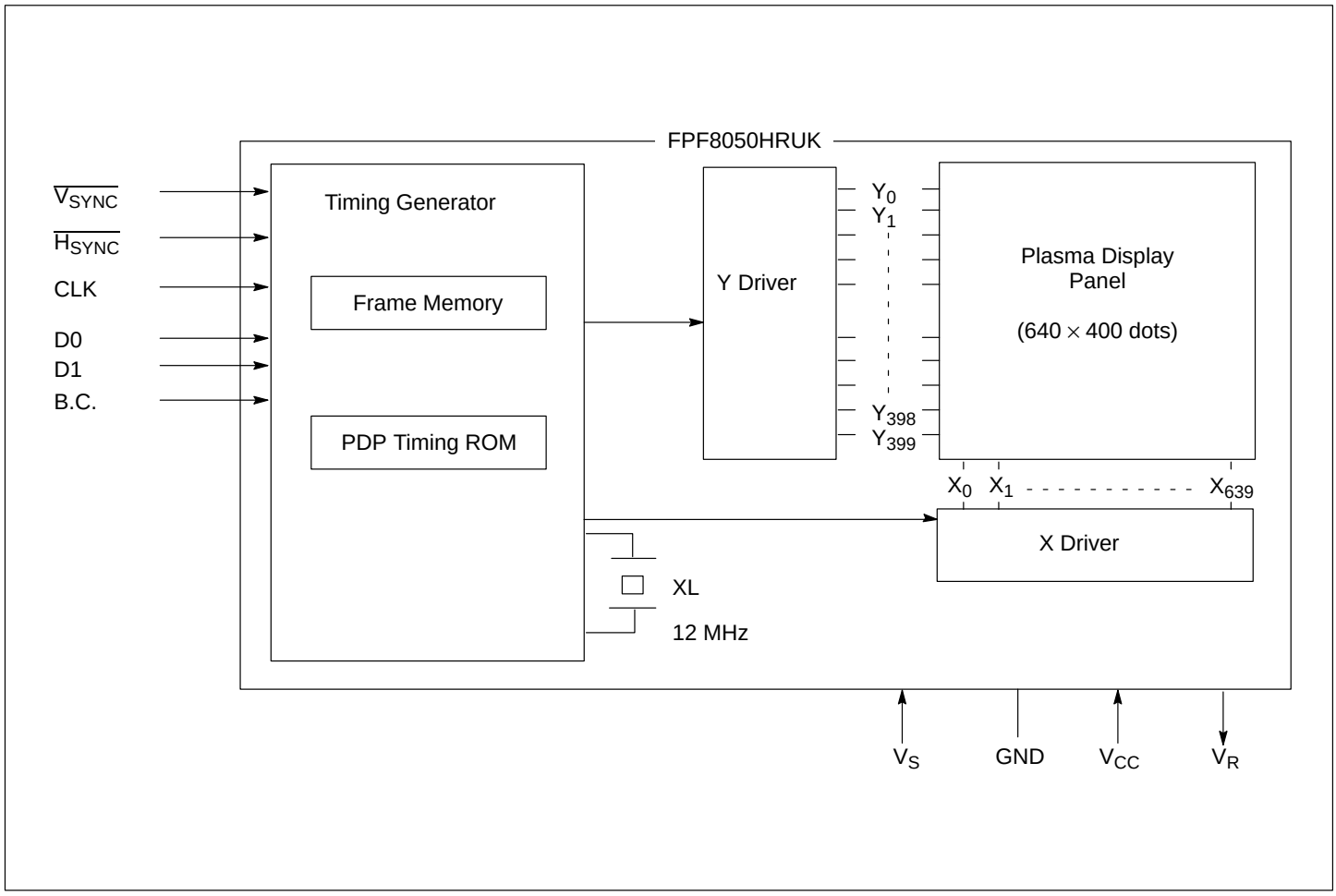
FPF8050HRUK
Plasma Display Graphics Unit



The FPF8050HRUK plasma graphics display unit consists of an AC gas discharge plasma display panel with bistable memory and associated driver circuitry. Fujitsu's proprietary control method provides a clear display with a four-level gray scale. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8050HRUK a highly reliable display device.

- Bright, even, orange-on-black display
- Four-level gray scale
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Supply Voltage for Sustain	V_S	+120 V
Supply Voltage for Logic	V_{CC}	+7 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Ripple (mV_{PP})	Stability
Supply Voltage for Sustain[1,2]	V_S	88	95	100.5	V	500 max.	± 2 % max.
Supply Voltage for Logic	V_{CC}	4.75	5.0	5.25	V	50 max.	± 5 % max.
Supply Current for Sustain (V_S = 95 V)	I_S			310	mA		
Supply Current for Logic (V_{CC} = 5 V)	I_{CC}	150		450	mA		
Signal Input Voltage (H-Level)	V_{IH}	2.0		5.25	V		
Signal Input Voltage (L-Level)	V_{IL}	-0.5		0.4	V		
Signal Input Current (V_{IH} = 2.75 V) (V_{CC} = 5.25 V)	I_{IH}			20	μA		
Signal Input Current (V_{IL} = 0.4 V) (V_{CC} = 5.25 V)	I_{IL}			-16	mA		

Notes: [1]Power source is required to be variable from 88 to 100.5 VDC.
[2]Specified value of V_S is indicated on the back (components mounted side) of each unit. Supply voltage should be trimmed to this specified value

MECHANICAL SPECIFICATIONS

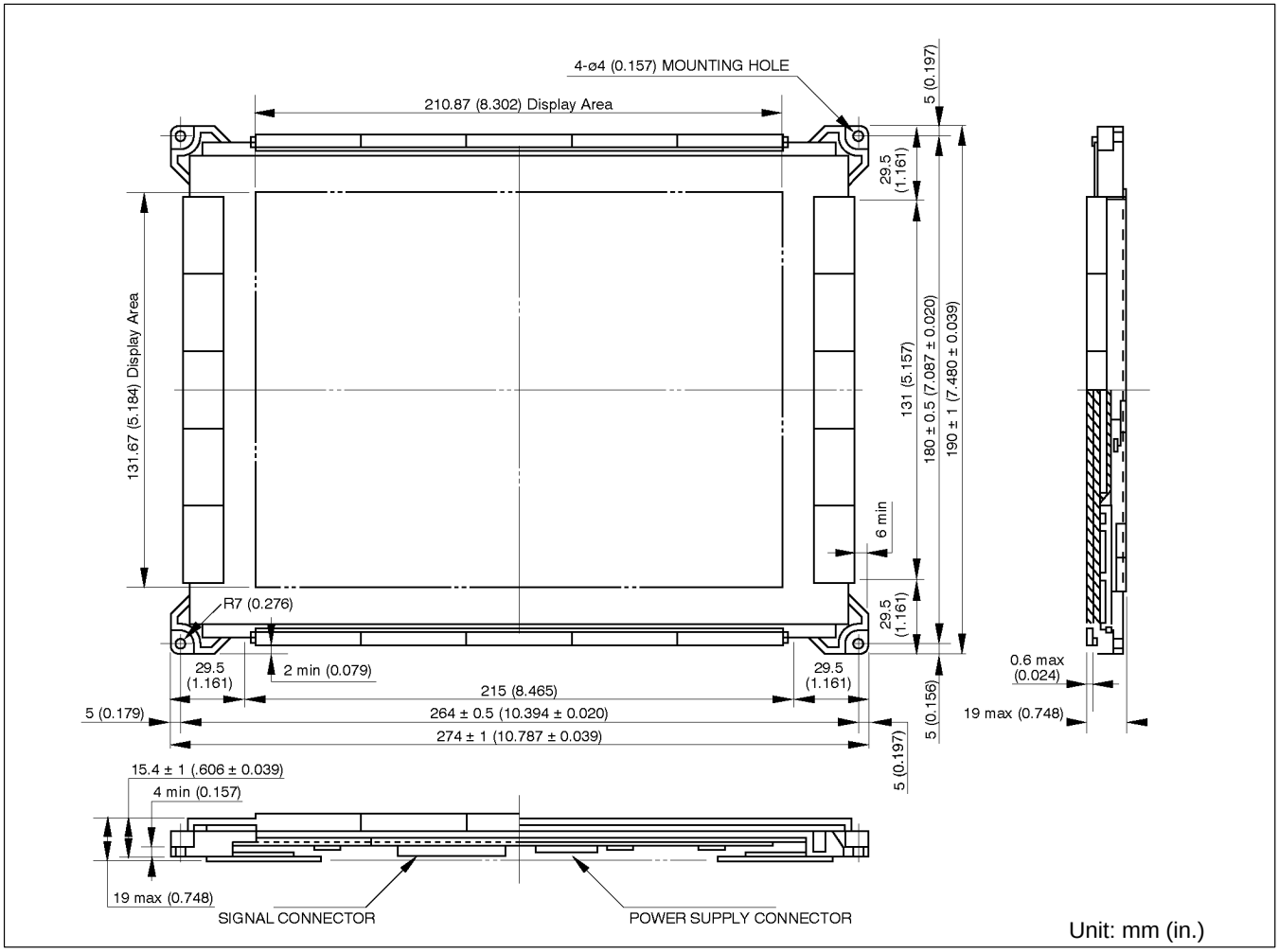
Physical Specifications

Item	Value
Number of Display Dots	640 (H) × 400 (V) dots (256,000 dots)
Dot Pitch	0.33 (H) × 0.33 (V) mm (0.013 × 0.013 in.)
Dot Size	0.2 mm (0.008 in.) dia.
Display Resolution	77 dots per linear inch
Screen Size	210.87 (H) × 131.67 (V) mm (8.302 × 5.184 in.)
Display Color	Neon orange
Gray Scale	4-level (approx. 100%, 67%, 33%, and 0%)
Dot Brightness (peak)	110 cd/m^2 (43.5 fL) max.
Brightness Control	Variable from 0 to 100% (Using B.C. signal)
Contrast Ratio	20:1 min.
Viewing Angle	160° min.
Weight	Approx. 900 g
External Dimensions	See External Dimension Figure

Performance Specifications

Item	Value
Operating Temperature	0 to +50 °C
Storage Temperature	-20 to +70 °C
Humidity	20 to 85% RH (no condensation)
Atmospheric Pressure Durability	Operation: 70,000 to 111,400 Pa Non-Operation: 34,000 to 111,400 Pa
Vibration Frequency: Acceleration: Time:	 10 to 55 Hz 2 G (max.) Operation: 5 min in X, Y, and Z direction Non-Operation: 2 hr. in X, Y, and Z direction
Shock (non-operation) Acceleration: Time:	 40 G (max.) in X and Y direction 20 G (max.) in Z direction 11 ms or less

External Dimensions

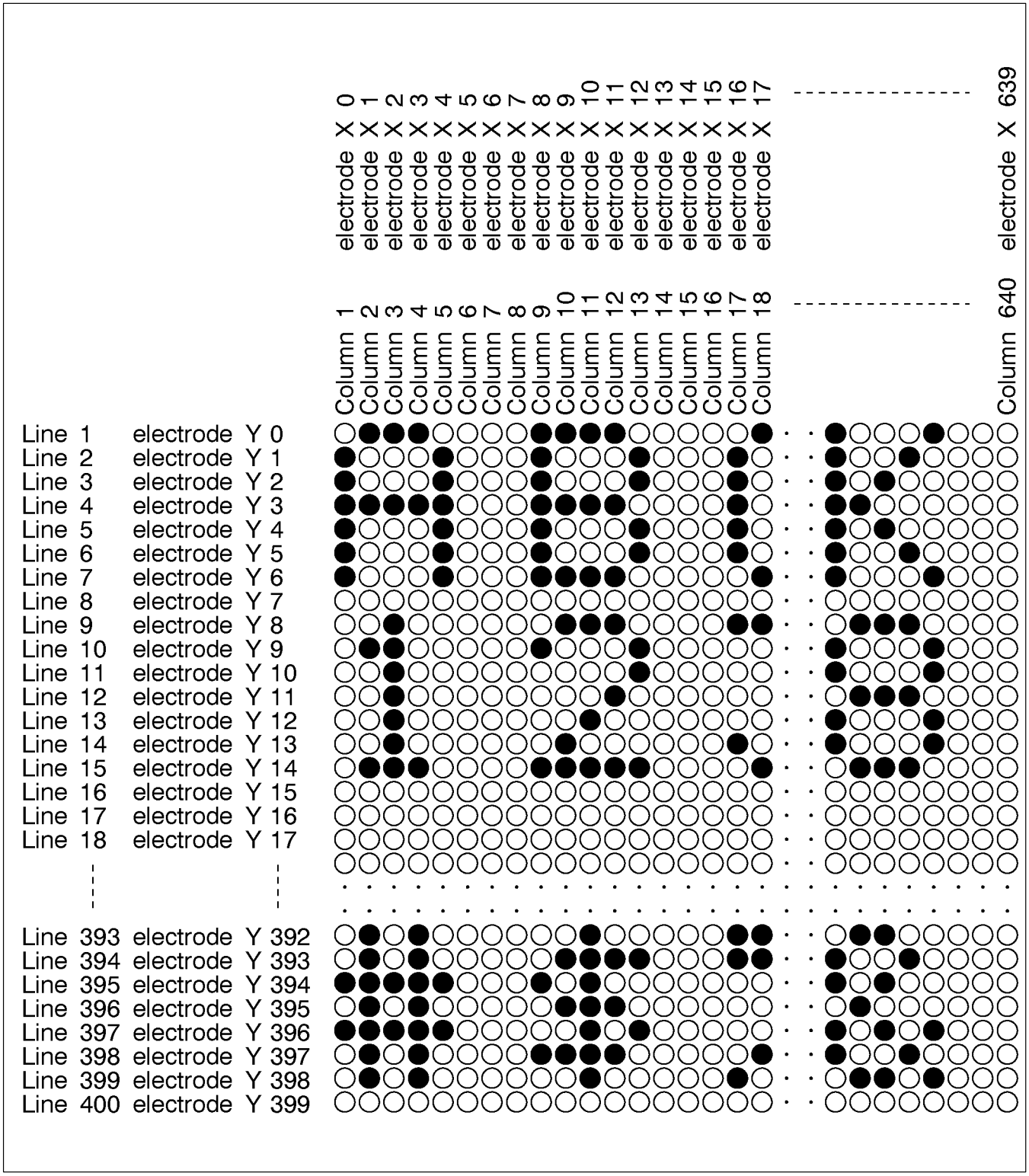


INTERFACE SIGNALS

Type of Signals

<table>
<tr><th>Signal</th><th>Symbol</th><th>Definition and Function</th></tr>
<tr><td>Data</td><td>D0
D1</td><td>2-bit data
Dots are lit at logic high and are not lit at logic low. The figure on the next page shows the relationship between display data and display dots.
Relationship Between Display Data and Gray Scale Level
<table>
<tr><th>D1</th><th>D0</th><th>Gray Scale Level
(Relative Brightness)</th></tr>
<tr><td>0</td><td>0</td><td>0%</td></tr>
<tr><td>0</td><td>1</td><td>low – 33%</td></tr>
<tr><td>1</td><td>0</td><td>medium – 67%</td></tr>
<tr><td>1</td><td>1</td><td>high – 100%</td></tr>
</table></td></tr>
<tr><td>Clock</td><td>CLK</td><td>The input signal which controls the input timing of the display data. Dot data is read into the shift register at the rising edge of each signal.
The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 640.</td></tr>
<tr><td>Line
Synchronous</td><td>$\overline{H_{SYNC}}$</td><td>The input signal which controls the scanning timing of the line electrode. Y address increment to select the next line electrode is done at the falling edge of each signal.
The number of $\overline{H_{SYNC}}$ signals during the period $\overline{V_{SYNC}}$ must be 402 or more even numbers.</td></tr>
<tr><td>Frame
Synchronous</td><td>$\overline{V_{SYNC}}$</td><td>The input signal which controls the refresh speed of the screen. The scanning position returns to the first electrode (home position) at the falling edge of the $\overline{V_{SYNC}}$ signal.</td></tr>
<tr><td>Brightness
Control</td><td>B.C.</td><td>The input signal which controls the screen brightness. Brightness is at its maximum at logic high, and 0% of the maximum at logic low.</td></tr>
</table>

Relationship Between Display Data and Display Dots

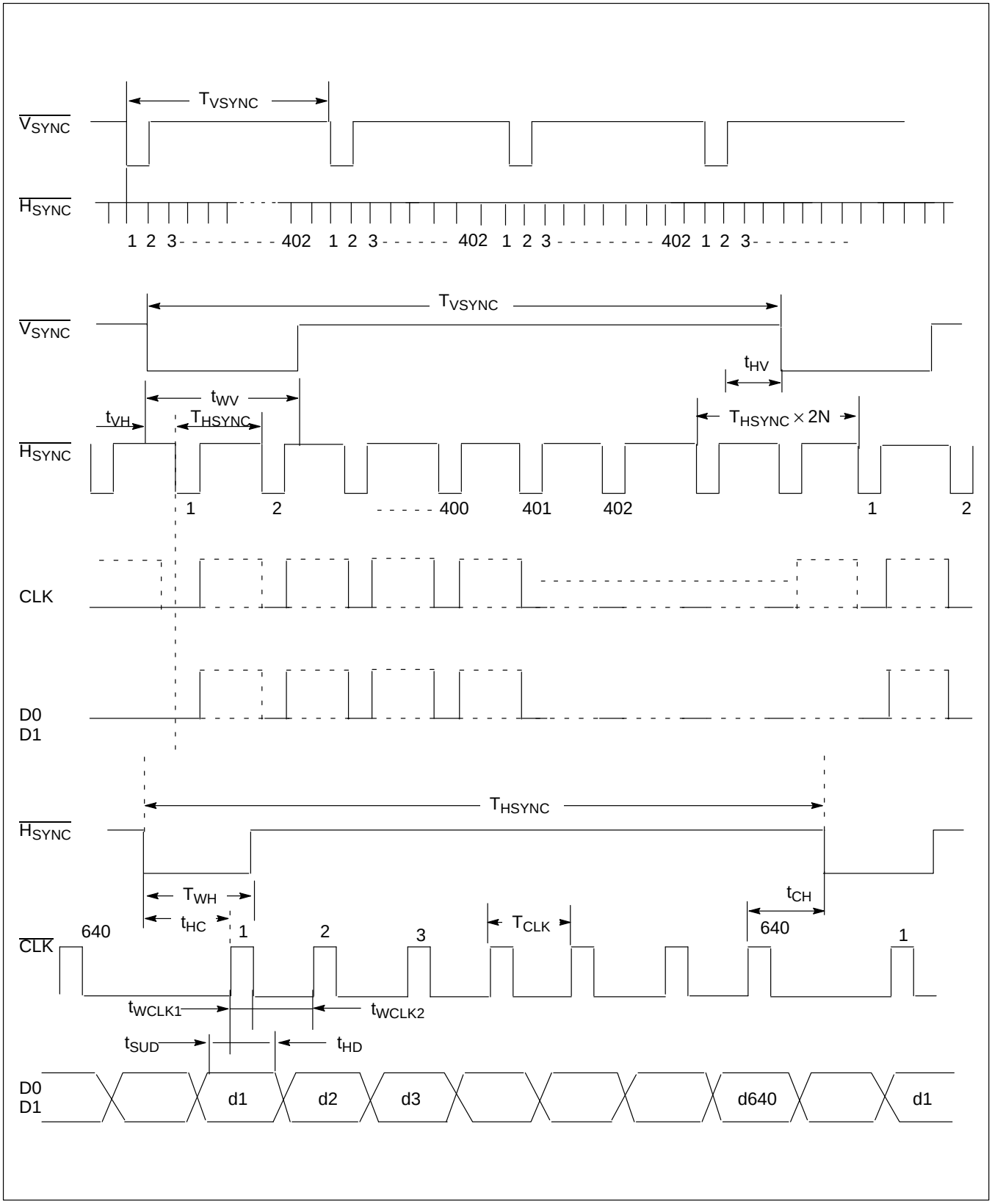


Interface Signal Timing

Symbol	Description	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}	A Cycle of Vertical Synchronous Signal		16.7	20	ms	Frame Frequency: 60 Hz
t_{WV}[1]	Pulse Width of Vertical Synchronous Signal	—	—	—	µs	
t_{VH}	Delay Time $\overline{V_{SYNC}}$ – $\overline{H_{SYNC}}$	1			µs	
t_{HV}	Delay Time $\overline{H_{SYNC}}$ – $\overline{V_{SYNC}}$	2			µs	
T_{HSYNC}	A Cycle of Horizontal Synchronous Signal	40	42	45	µs	
t_{WH}	Pulse Width of Horizontal Synchronous Signal	2	5		µs	
t_{HC}	Delay Time $\overline{H_{SYNC}}$ – CLK	2			µs	
t_{CH}	Delay Time CLK – $\overline{H_{SYNC}}$	2	3		µs	
T_{CLK}	A Cycle of Clock Signal	44			ns	
t_{WCLK1}[2]	Pulse Width of Clock Signal (H)	22			ns	
t_{WCLK2}[2]	Pulse Width of Clock Signal (L)	22			ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{SUD}	Set Up Time for Data	22			ns	
t_{HD}	Hold Time for Data	22			ns	

Notes: [1]$t_{WV} > T_{HSYNC}$
[2]Recommended ratio between t_{WCL1} and T_{WCL2} is 1:1

Interface Signal Timing Chart

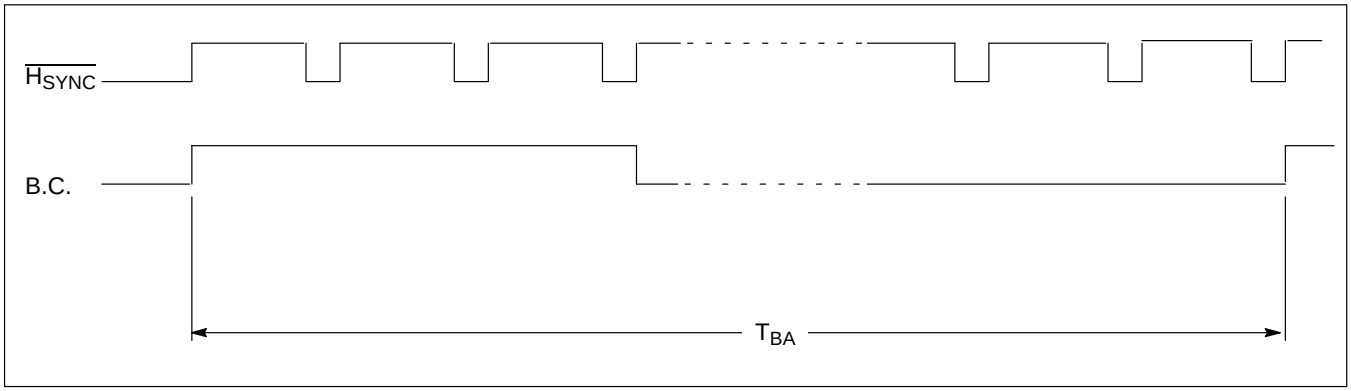


Brightness Control Signal Timing

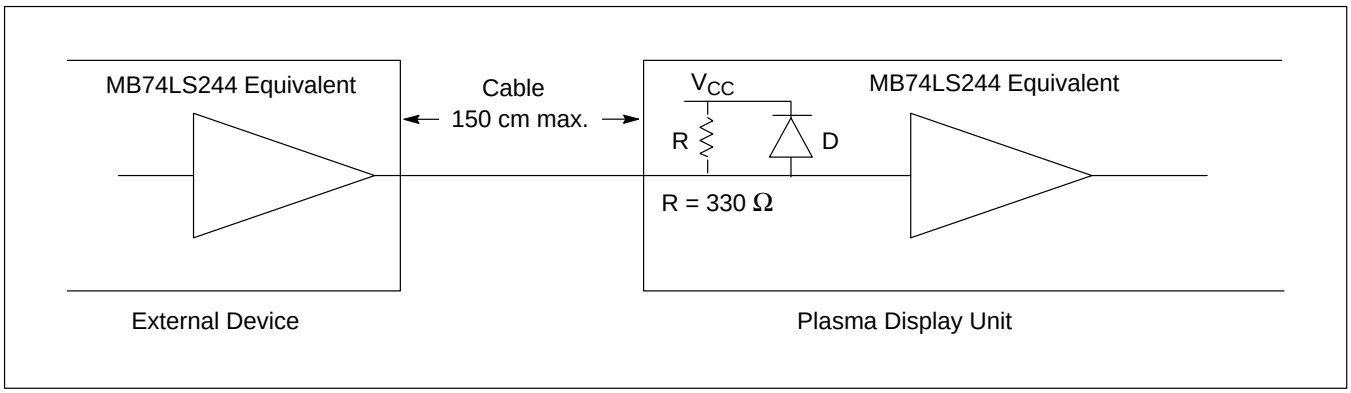
The brightness control signal can be input with a pulse form signal. The brightness is variable from 0 to 100% depending on its duty cycle. Signal conditions are shown in the table below and in the interface circuit diagram.

Symbol	Min.	Typ.	Max.	Unit	Remark
T_{BA}	—	16	16	H	H: A cycle of line synchronous signal

Brightness Control Signal Timing Chart



Interface Circuit



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN–605Q026–G/S

Pin No.	Symbol	Pin No.	Symbol
1	$\overline{V_{SYNC}}$	2	S. GND
3	$\overline{H_{SYNC}}$	4	S. GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S. GND
15	D0	16	S. GND
17	D1	18	S. GND
19	CLK	20	S. GND
21	B.C.	22	N.C.
23	N.C.	24	N.C.
25	V_{CC}	26	V_{CC}

Note: Applicable Connector:
FCN–607B026–G/D

N.C. means “No Connection.”

Power Supply Connector

FCN–815P–009TA

Pin No.	Symbol
1	V_{CC}
2	GND (L)
3	N.C.
4	GND (H)
5	V_S
6	N.C.
7	N.C.
8	N.C.
9	V_R*

Notes: Applicable Connectors:
FCN–813J009–A, Housing
FCN–813J–T/Q, Contact for Manual Use
FCN–813J–T/R, Contact for Automatic Use

* This plasma display unit outputs the voltage V_R from 0 to 2.5 VDC through the ninth terminal of the power supply connector. This supply voltage is used for the supply voltage adjustment of FPF07P-AC100 (power supply unit).

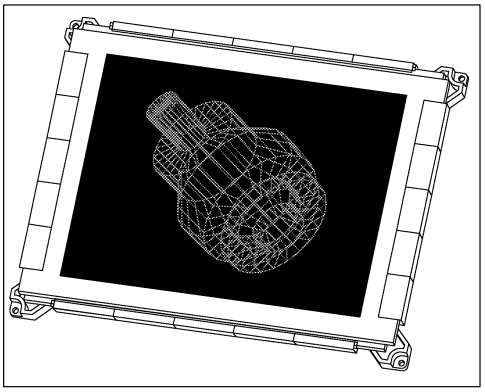
June 1992
Edition 1.0

FUJITSU

DATA SHEET

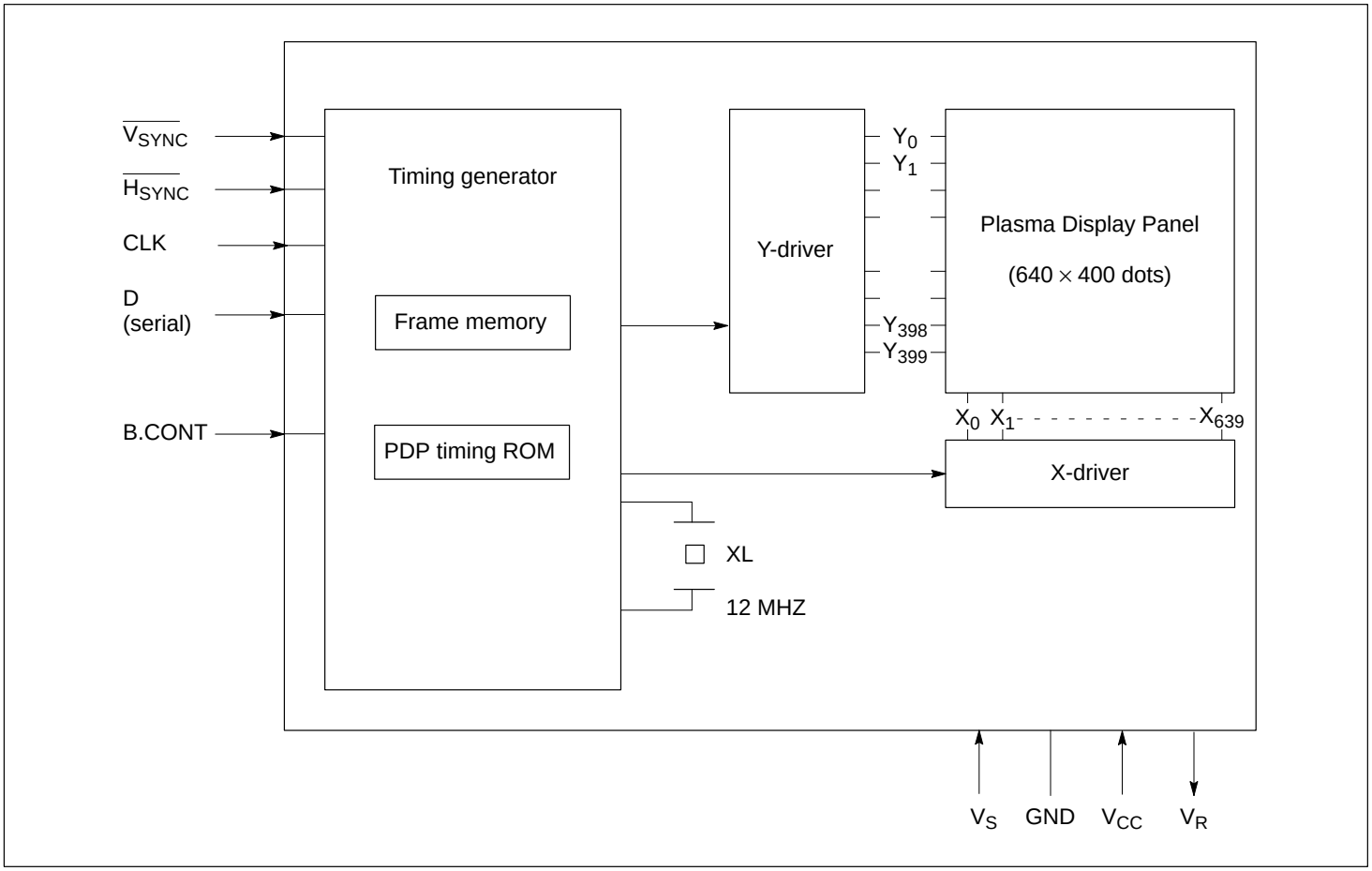
FPF8050HRUM
Plasma Display Graphics Unit

The FPF8050HRUM plasma display unit consists of an AC gas discharge plasma display unit with bistable memory and associated driver circuitry. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8050HRUM a highly reliable display device.



- Bright, even, orange-on-black display
- No flicker or warp
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Sustain voltage	V_S	120 V
Logic voltage	V_{CC}	7 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for sustain*	V_S	88	95	100.5	V
Supply current for sustain (V_S = 95 V)	I_S			310	mA
Supply voltage for logic	V_{CC}		5		V
Supply current for logic (V_{CC} = 5 V)	I_{CC}	0.15		0.45	A
Signal input voltage for logic 1	V_{IH}	2.0		5.25	V
Signal input current for logic 1 (V_{IH} = 2.75)	I_{IH}			20	μA
Signal input voltage for logic 0	V_{IL}	-0.5		0.4	V
Signal input current for logic 0 (V_{IL} = 2.75 V)	I_{IL}			-16	mA

Note: * The power source is required to be variable from 88 to 100.5 VDC.

MECHANICAL SPECIFICATIONS

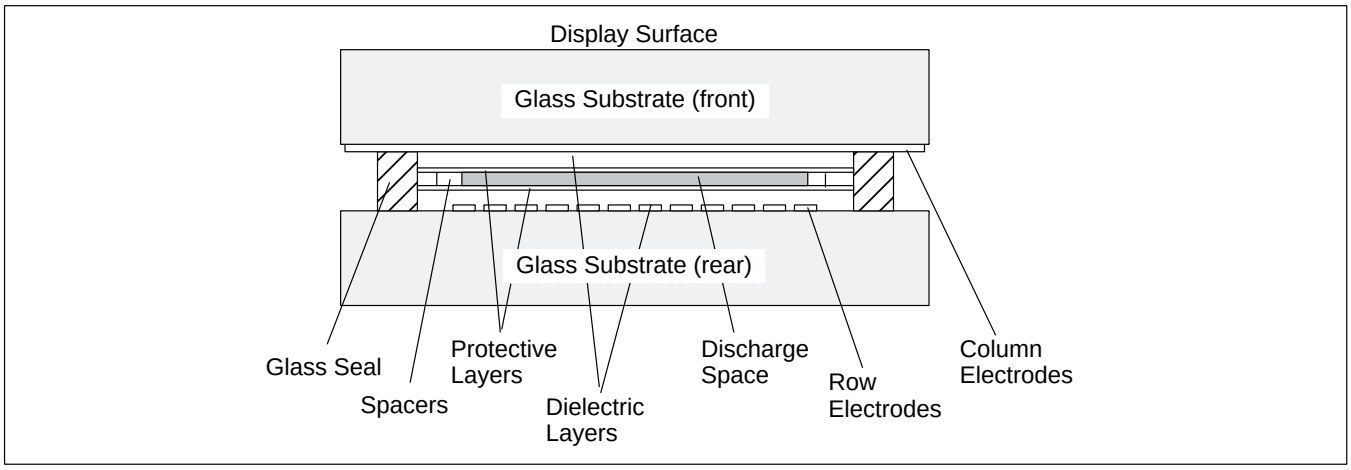
Physical Specifications

Item	Value
Number of display dots	640 × 400 dots (256,000 dots)
Dot pitch	0.33 (H) × 0.33 (V) mm (0.013 × 0.013 in.)
Dot size	0.2 mm (0.008 in.) dia
Effective display area	211 (H) × 132 (V) mm (8.307 × 5.197 in.)
Display color	Neon orange
Brightness	110 cd/m^2 (Peak) 15 cd/m^2 (Average)
Contrast ratio	20 : 1 min
Viewing angle	160° min
Weight	Approx. 900 g
External dimensions	See External Dimensions

Performance Specifications

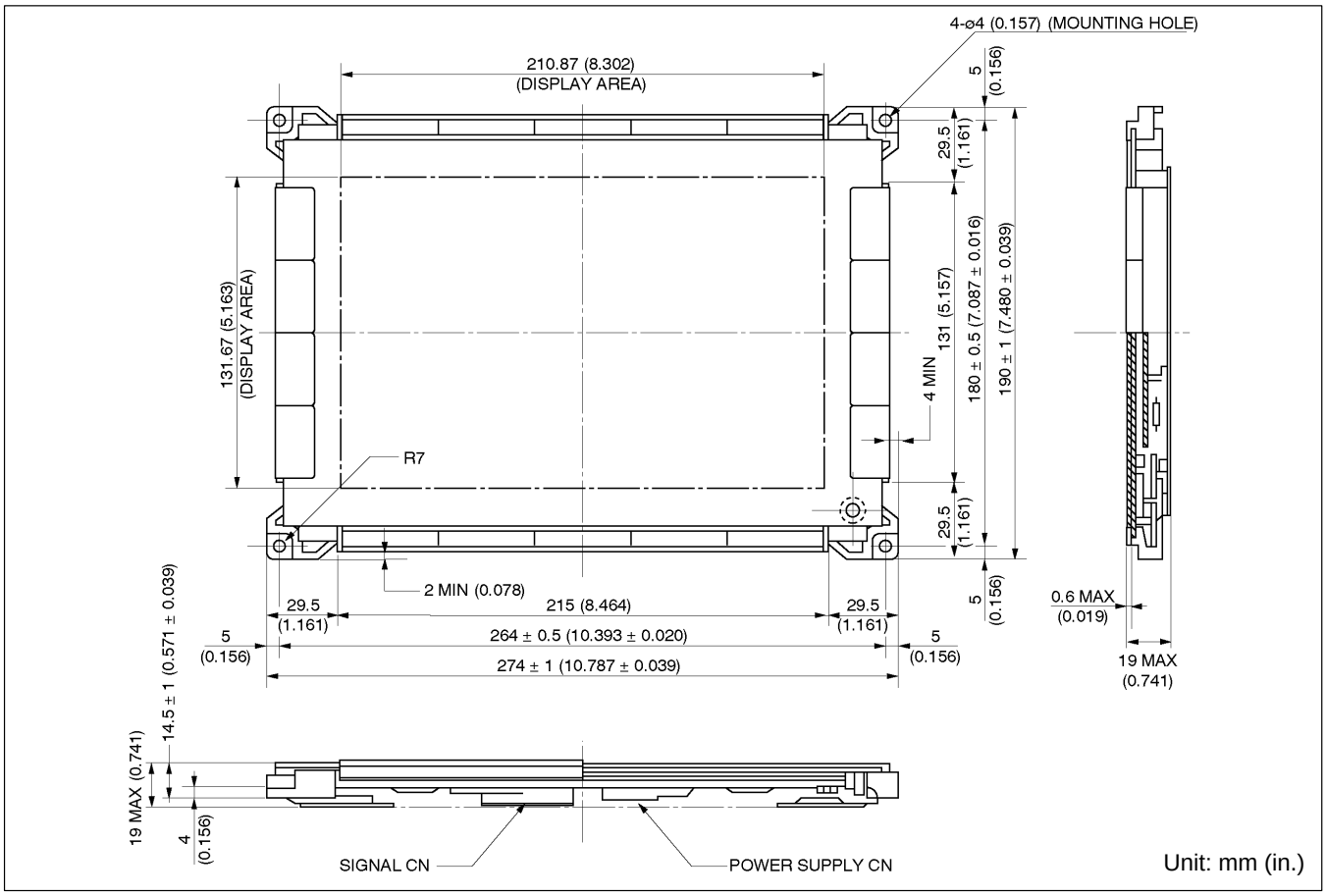
Item	Symbol	Value
Operating temperature	T_{OP}	0 to +50 °C
Operating humidity	RH_{OP}	20 to 85%
Storage temperature	T_{STG}	–20 to +70 °C
Storage humidity	RH_{STG}	20 to 85%
Vibration	V	2 G
Shock	S	40 G
Pressure (non-operating)		340 to 1114 hPa

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

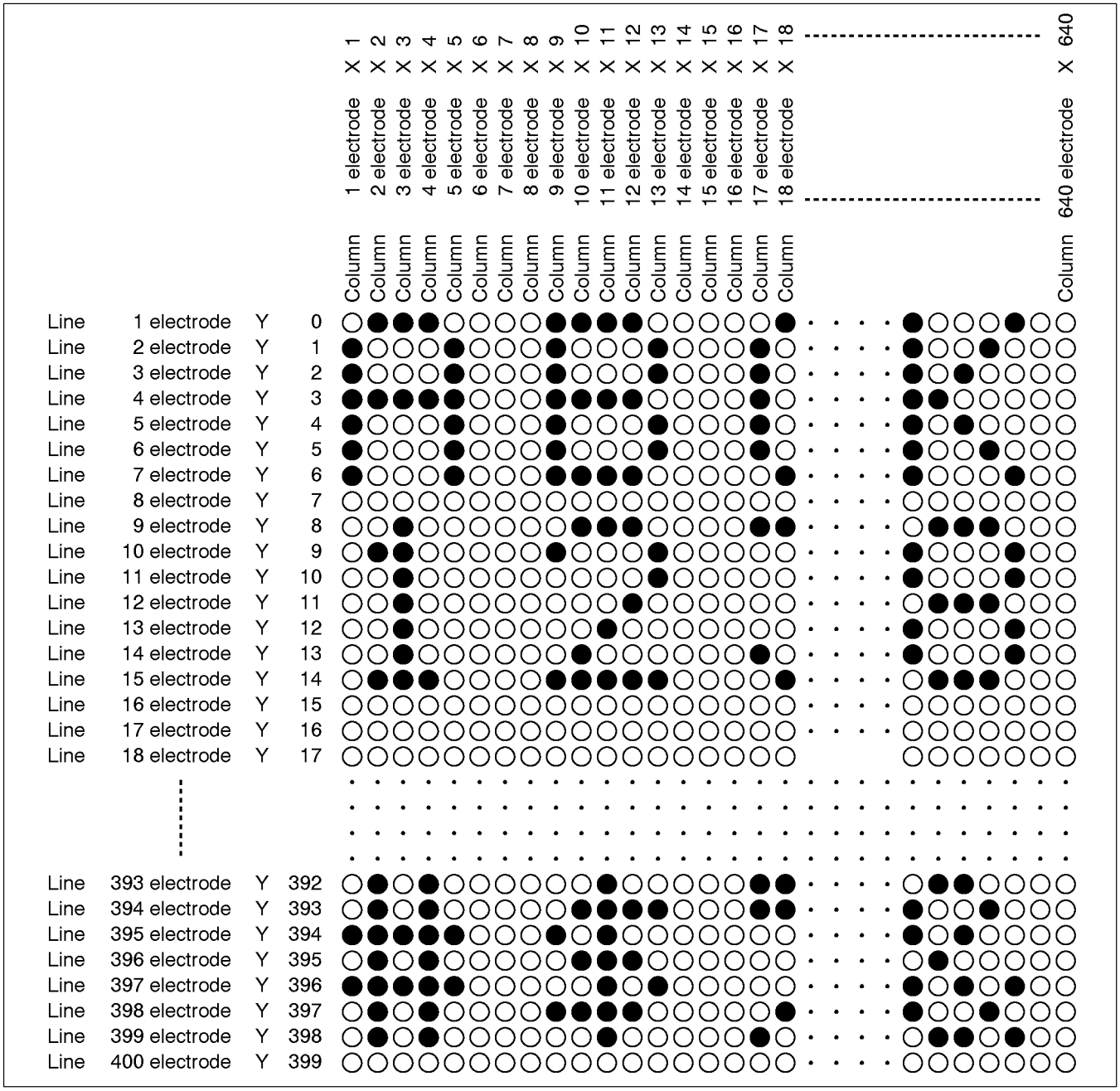


INTERFACE SIGNALS

Type of Signals (TTL Compatible)

Signal	Symbol	Logic	Definition and Function
Display data	D	Posi	Serial display data. Relationship between display data and display dots is shown in the following figure.
Clock signal	CLK	Posi	The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 640.
Line synchronous	$\overline{H_{SYNC}}$	Nega	The number of $\overline{H_{SYNC}}$ signals in one cycle of $\overline{V_{SYNC}}$ must be 402 or more even numbers.
Frame synchronous	$\overline{V_{SYNC}}$	Nega	The input signal controls the refresh speed of the screen.
Brightness control	B.CONT	The input signal which controls the screen brightness. Brightness is its maximum at logical “High” and 33% of maximum at logical “Low.”	

Relationship Between Display Data and Display Dots



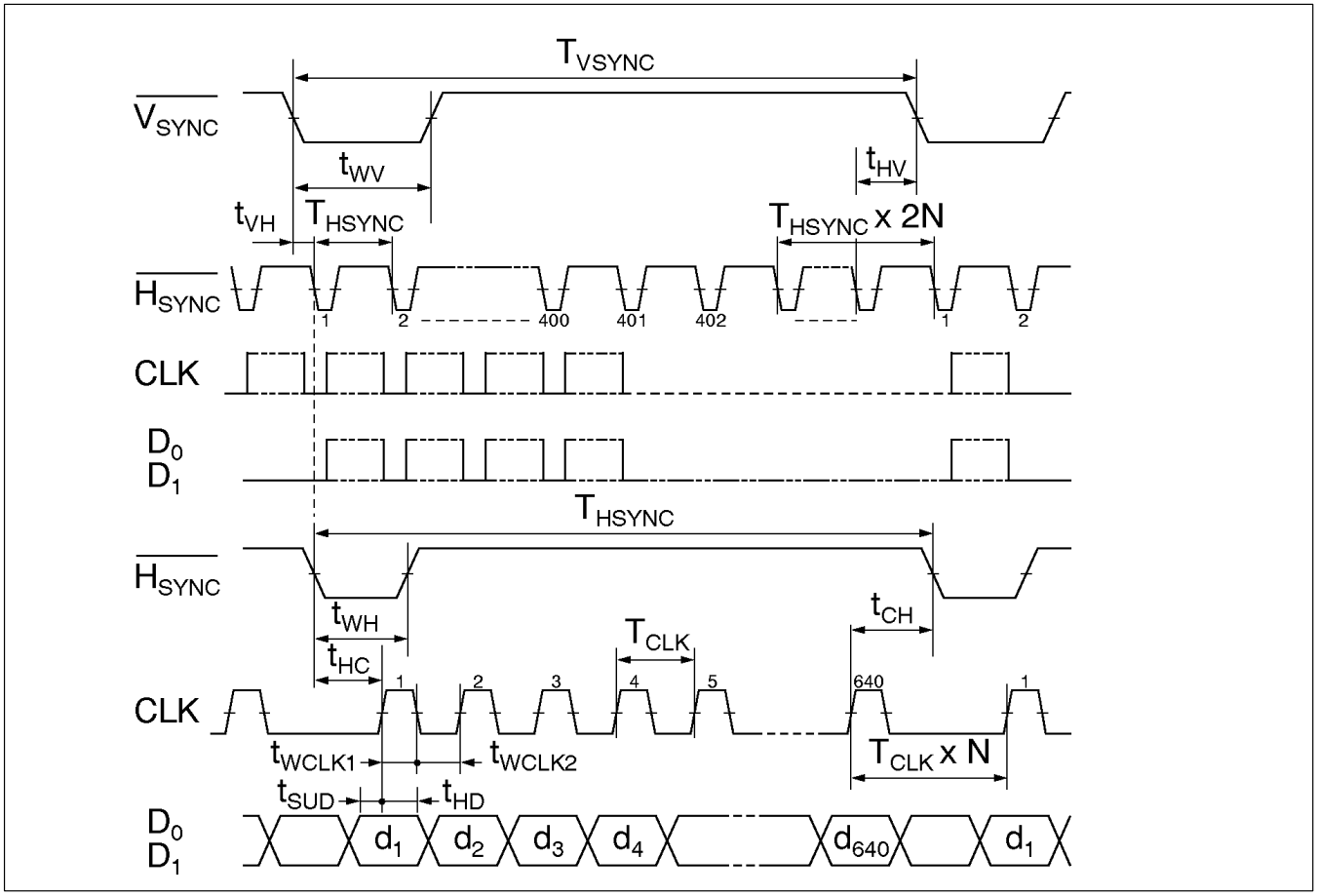
Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit
T_{VSYNC}	—	39.6	—	ms
t_{WV}	T_{HSYNC}	—	—	µs
t_{VH}	1	—	—	µs
t_{HV}	2	—	—	µs
T_{HSYNC}[1]	88	90	92	µs
t_{WH}	2	6	—	µs
t_{HC}	2	—	—	µs
t_{CH}	2	3	—	µs
T_{CLK}	44	—	—	ns
$t_{WCLK1,2}$[2]	22	—	—	ns
t_{SUD}	22	—	—	ns
t_{HD}	22	—	—	ns

Notes: [1] T_{HSYNC} ranges from 40 to 45 µs and from 60 to 65 µs are also available. In these cases, brightness control range changes.

[2] Recommended ratio between t_{WCLK1} and t_{WCLK2} is 1 : 1.

Interface Signal Timing Chart



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-605Q26-G/S (Fujitsu)

Pin No.	Signal	Pin No.	Signal
1	$\overline{V_{SYNC}}$	2	S.GND
3	$\overline{H_{SYNC}}$	4	S.GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S.GND
15	D	16	S.GND
17	N.C.	18	S.GND
19	CLK	20	S.GND
21	B.CONT	22	N.C.
23	N.C.	24	N.C.
25	V_{CC}	26	V_{CC}

Applicable connector:
FCN-607B026-G/D

Power Supply Connector

FCN-815P009-TA (Fujitsu)

Pin No.	Signal
1	V_{CC}
2	GND (L)
3	N.C.
4	GND (H)
5	V_S
6	N.C.
7	N.C.
8	N.C.
9	V_R*

Applicable connectors:
FCN-813J009-A housing (Fujitsu)
FCN-813J-T/A contact (Fujitsu)

* This terminal is connected only when FPF07P-AC100 power supply unit is used.

Section 5

Graphic Units (640 by 480 dots) — *At a Glance*

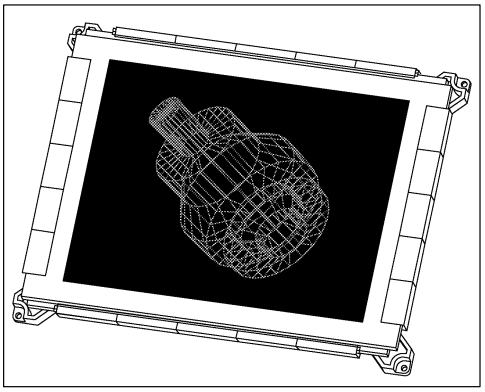
July 1992
Edition 1.0

FUJITSU

DATA SHEET

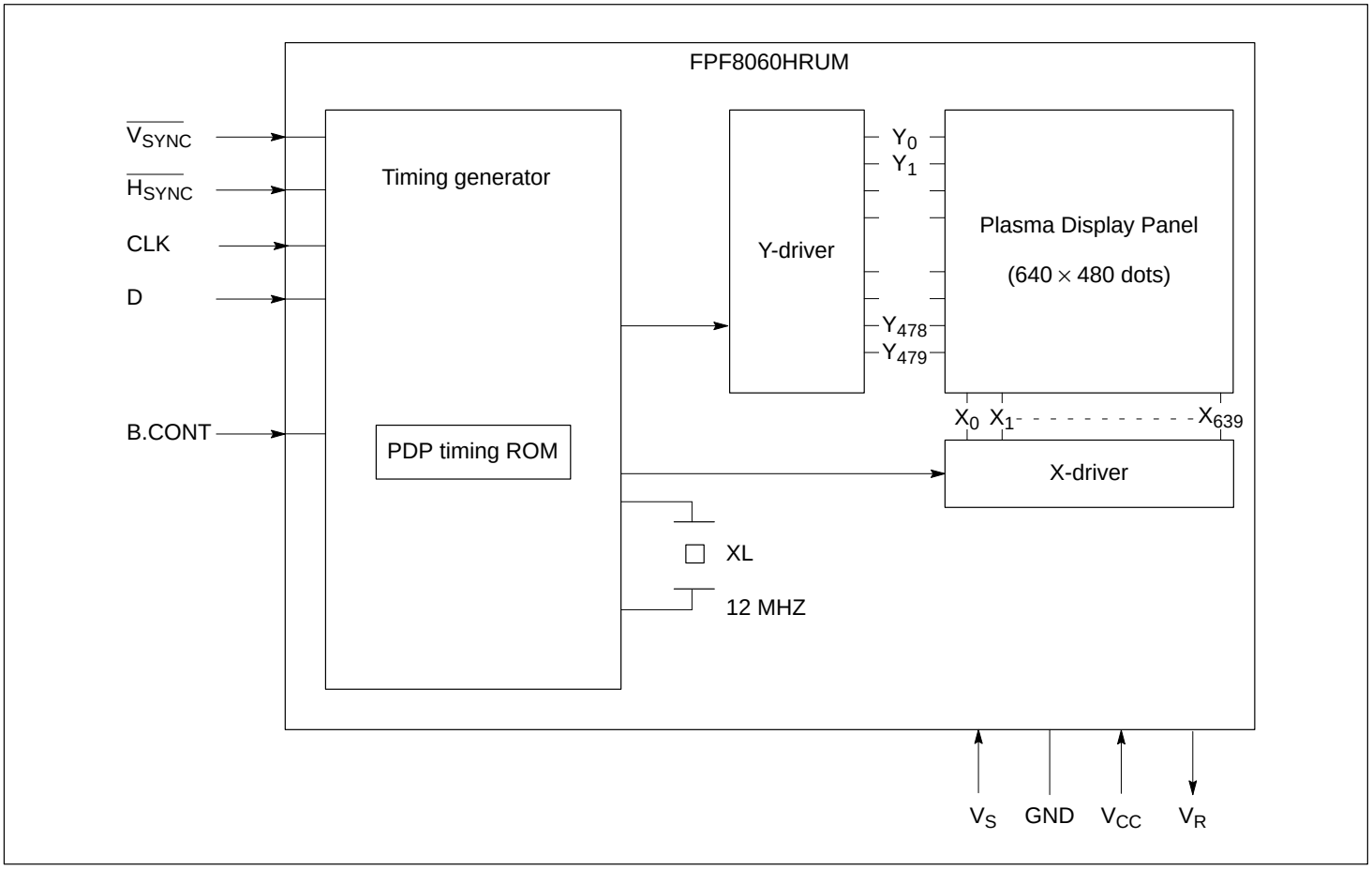
FPF8060HRUB–002
Plasma Display Graphics Unit

The FPF8060HRUB-022 plasma display unit consists of an AC gas discharge plasma display unit with bistable memory and associated driver circuitry. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8060HRUB-022 a highly reliable display device.



- High resolution
- Bright, even, orange-on-black display
- No flicker or warp
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Sustain voltage	V_S	120 V
Logic voltage	V_{CC}	7 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for sustain*	V_S	88	95	100.5	V
Supply current for sustain (V_S = 95 V)	I_S			340	mA
Supply voltage for logic	V_{CC}		5		V
Supply current for logic (V_{CC} = 5 V)	I_{CC}	0.15		0.45	A
Signal input voltage for logic 1	V_{IH}	2.0		5.25	V
Signal input current for logic 1 (V_{IH} = 2.75)	I_{IH}			20	µA
Signal input voltage for logic 0	V_{IL}	–0.5		0.4	V
Signal input current for logic 0 (V_{IL} = 2.75 V)	I_{IL}			–16	mA

Note: The power source is required to be variable from 88 to 100.5V DC.

MECHANICAL SPECIFICATIONS

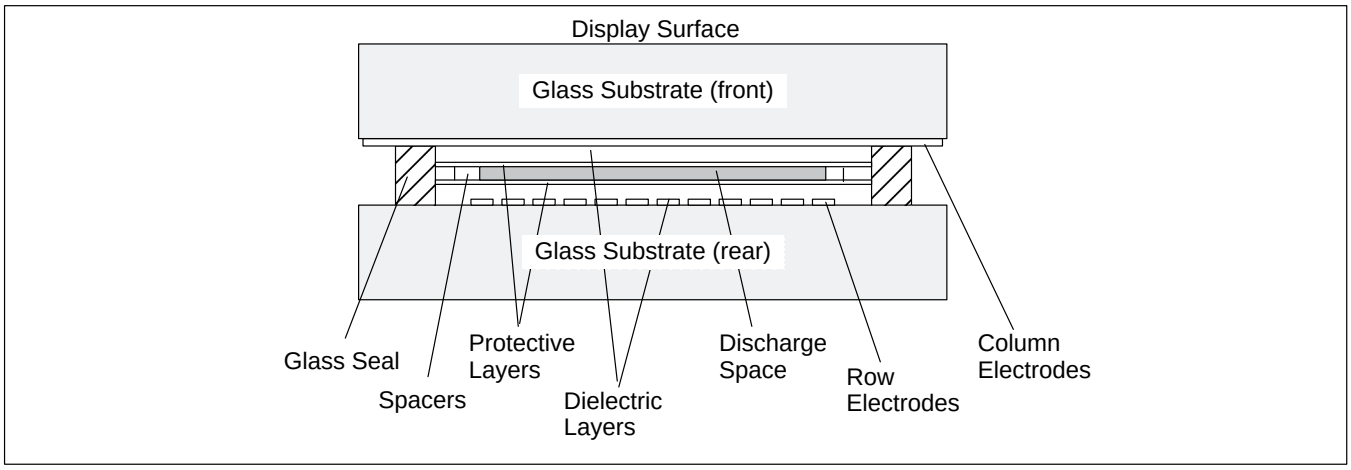
Physical Specifications

Item	Value
Number of display dots	640 × 480 dots (307,200 dots)
Dot pitch	0.33 (H) × 0.33 (V) mm (0.013 × 0.013 in.)
Dot size	0.2 mm (0.008 in.) dia
Effective display area	211 (H) × 158 (V) mm (8.307 × 6.220 in.)
Display color	Neon orange
Brightness	110 cd/m^2
Contrast ratio	20 : 1 min
Viewing angle	160° min
Weight	Approx. 1 kg
External dimensions	See External Dimensions

Performance Specifications

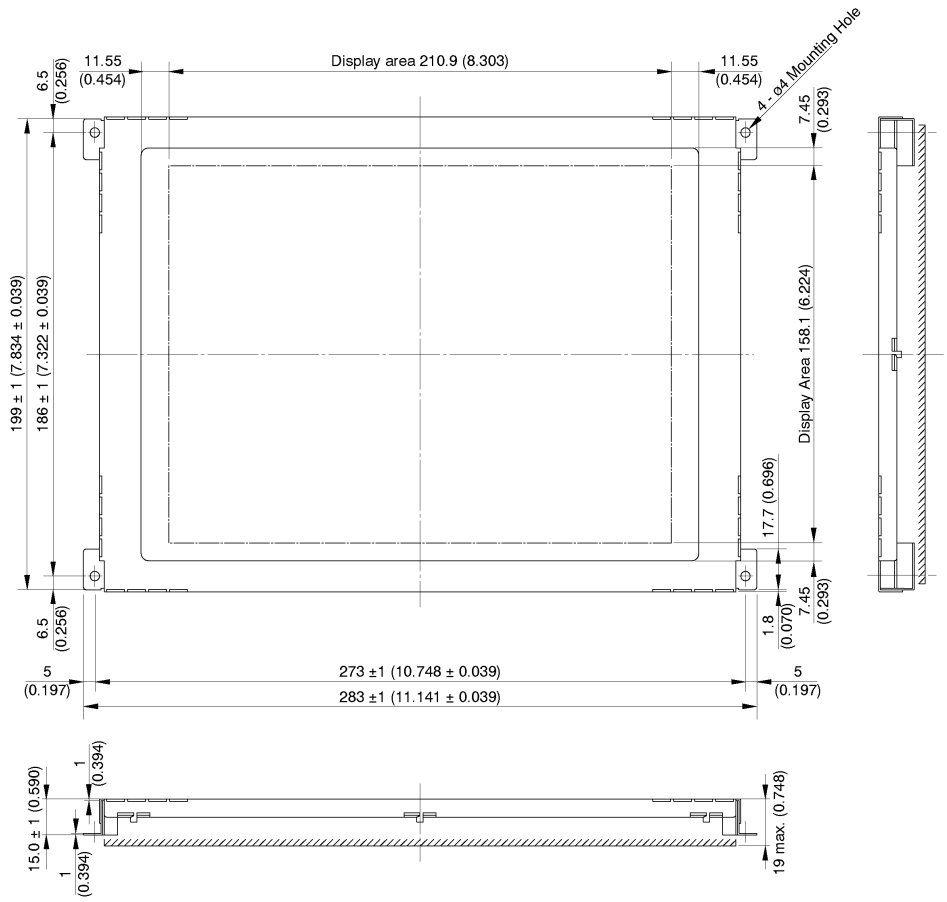
Item	Symbol	Value
Operating temperature	T_{OP}	0 to +50°C
Operation humidity	RH_{OP}	20 to 85%
Storage temperature	T_{STG}	–20 to +70°C
Storage humidity	RH_{STG}	20 to 85%
Vibration	V	2 G
Shock	S	40 G
Pressure (non-operating)		340 to 1114 hPa

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

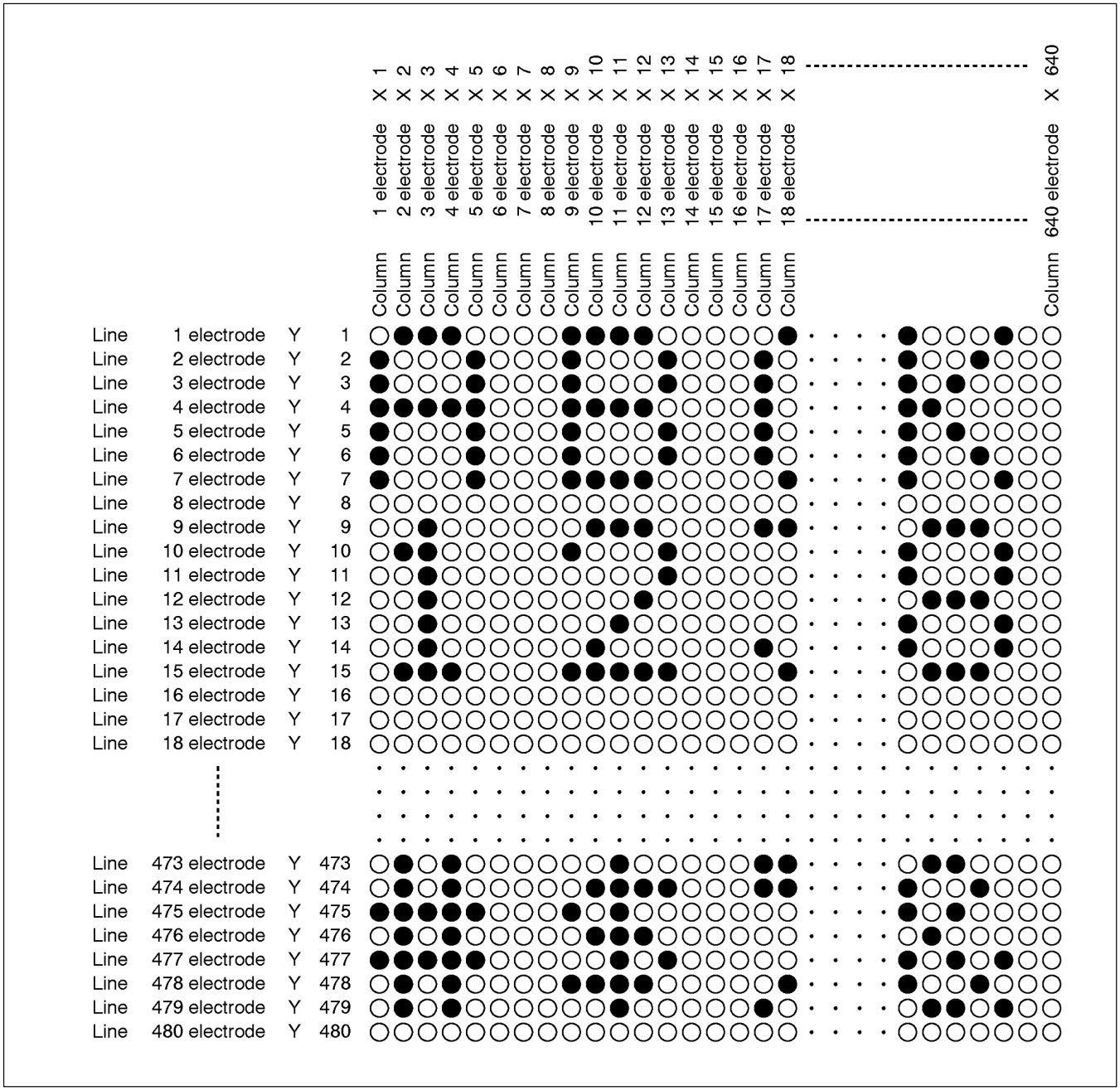


INTERFACE SIGNALS

Type of Signals (TTL Compatible)

Signal	Symbol	Logic	Definition and Function
Display data	D	Posi	Serial display data. Relation between display data and display dots is shown in the following figure.
Clock signal	CLK	Nega	The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 160.
Line synchronous	$\overline{H_{SYNC}}$	Nega	The number of $\overline{H_{SYNC}}$ signals in one cycle of $\overline{V_{SYNC}}$ must be 482 or more even numbers.
Frame synchronous	$\overline{V_{SYNC}}$	Nega	The input signal which controls the refresh speed of the screen.
Brightness control	B.CONT	The input signal which controls the screen brightness. Brightness is its maximum at logical “High” and 0% of maximum at logical “Low.”	

Relationship Between Display Data and Display Dots

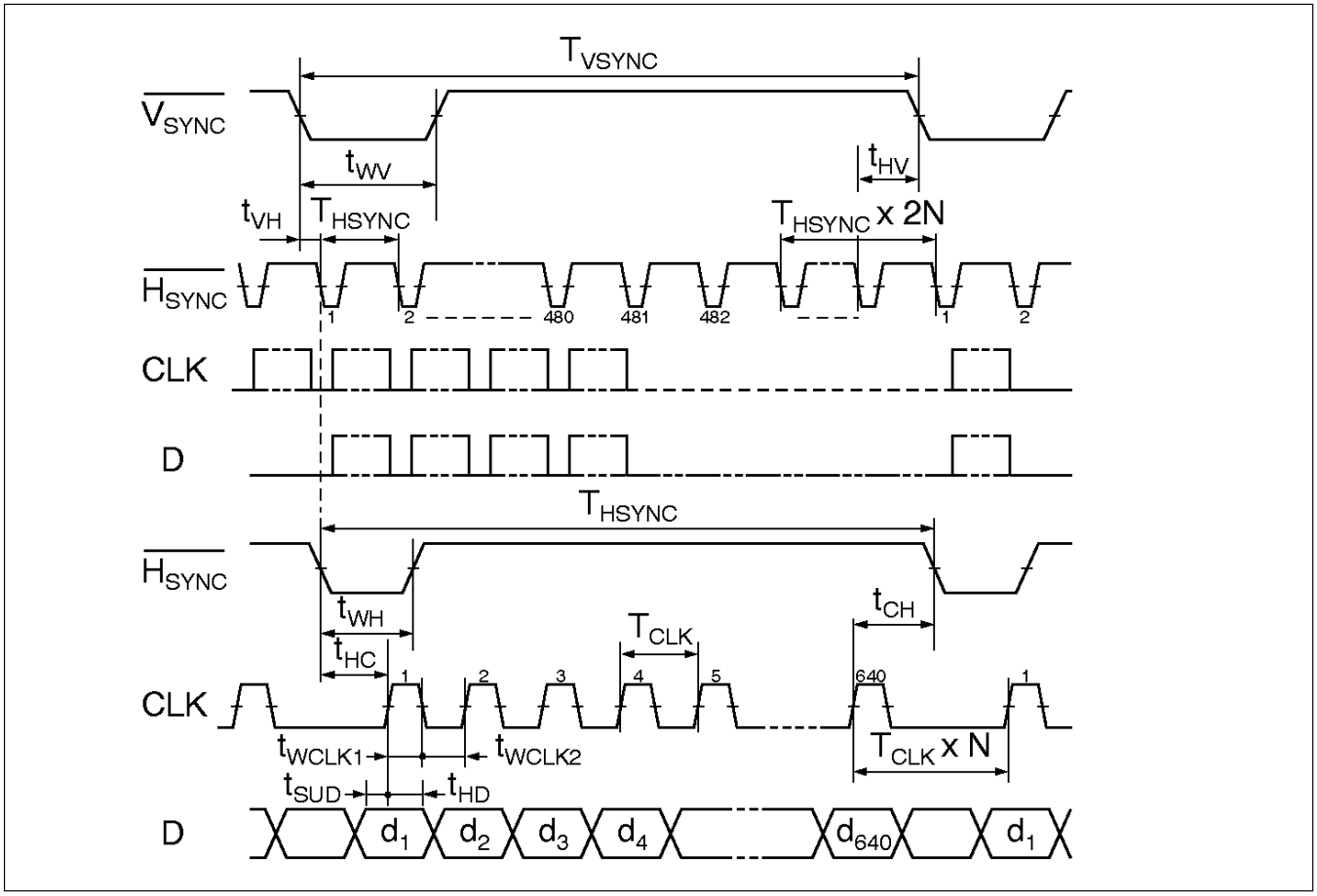


Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit
T_{VSYNC}	—	44.46	—	ms
t_{WV}[1]	—	—	—	µs
t_{VH}	1	—	—	µs
t_{HV}	2	—	—	µs
T_{HSYNC}	88	90	92	µs
t_{WH}	2	6	—	µs
t_{HC}	2	—	—	µs
t_{CH}	2	3	—	µs
T_{CLK}	44	—	—	ns
$t_{WCLK1,2}$[2]	22	—	—	ns
t_{SUD}	22	—	—	ns
t_{HD}	22	—	—	ns

Notes: [1]$T_{WV} > T_{HSYNC}$.
[2]Recommended ratio between t_{WCLK1} and t_{WCLK2} is 1 : 1.

Interface Signal Timing Chart



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-605Q26-G/S (Fujitsu)

Pin No.	Signal	Pin No.	Signal
1	$\overline{V_{SYNC}}$	2	S.GND
3	$\overline{H_{SYNC}}$	4	S.GND
5	$\overline{D0}$	6	N.C.
7	$\overline{D1}$	8	N.C.
9	$\overline{D2}$	10	N.C.
11	$\overline{D3}$	12	N.C.
13	S.GND	14	S.GND
15	$\overline{CKE}$	16	S.GND
17	BCE	18	S.GND
19	S.GND	20	ENA

Applicable connector:
FCN-607B026-G/D

Power Supply Connector

FCN-815P009-TA (Fujitsu)

Pin No.	Signal
1	V_{CC}
2	GND (L)
3	N.C.
4	GND (H)
5	V_S
6	N.C.
7	N.C.
8	N.C.
9	V_R*

Applicable connectors:
FCN-813J009-A housing (Fujitsu)
FCN-813J-T/A contact (Fujitsu)

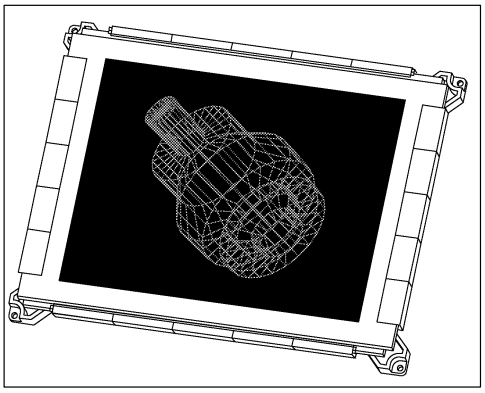
* This terminal is connected only when FPF07P-AC100 power supply unit is used.

June 1992
Edition 2.0

FUJITSU

DATA SHEET

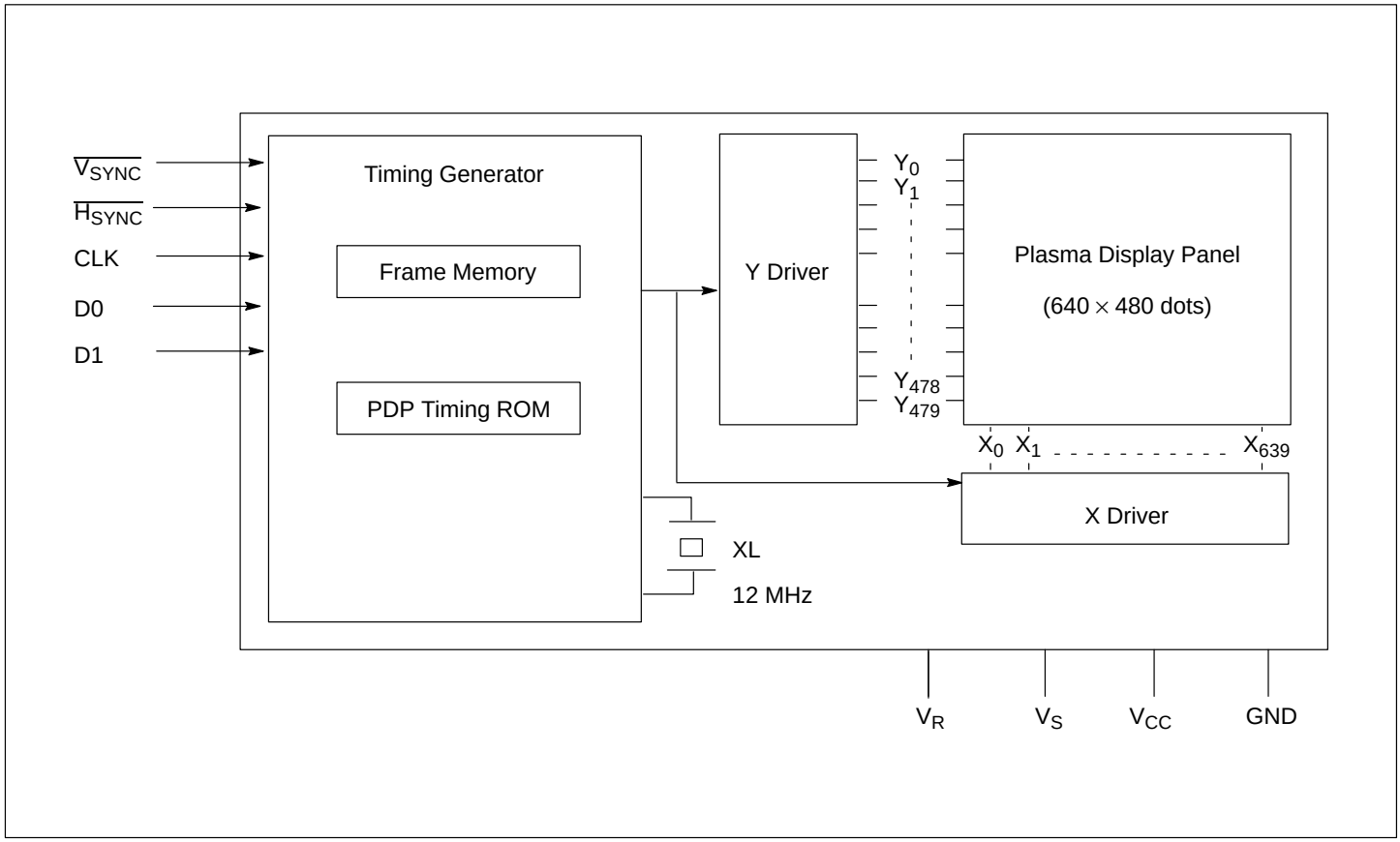
FPF8060HRUC–120
Plasma Display Graphics Unit



The FPF8060HRUC-120 plasma graphics display unit consists of an AC gas discharge plasma display panel with bistable memory and associated driver circuitry. Fujitsu's proprietary control method provides a clear display with a 4-level gray scale. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8060HRUC-120 a highly reliable display device. This display model is well–suited for touchscreen input applications with its ergonomie design.

- Bright, even, orange-on-black display
- Four-level gray scale
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Supply Voltage for Sustain	V_S	+130 V
Supply Voltage for Logic	V_{CC}	+7 V

DC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit
For Display	Supply Voltage for Sustain[1,2]	V_S	88	95	100.5	V
	Ripple/Noise (mV_{PP})	V_{NRS}	—	—	500	mV
	Stability (Average)	—	—	—	—	±1.5	%
	Accuracy (Against V_S specified on label of unit)	—	—	—	±0.5	%
	Stability (moment)	—	—	—	-5	%
	Supply Current for Sustain (V_S = 95 V)[3,4]	I_S	50	200	340	mA
	Supply Current (moment)	I_{SP}	0.5	—	2	A
For Logic	Supply Voltage for Logic	V_{CC}	4.75	5.0	5.25	V
	Ripple/Noise (mV_{PP})	V_{NRC}	—	—	200	mV
	Stability	—	—	—	±5	%
	Supply Current for Logic (V_{CC} = 5 V)	I_{CC}	150	250	500	mA
	Signal Input Voltage (H-Level)	V_{IH}	2.0	—	5.25	V
	Signal Input Voltage (L-Level)	V_{IL}	–0.5	—	0.8	V
	Signal Input Current (V_{IH} = 2.75 V) (V_{CC} = 5.25 V)	I_{IH}	—	—	20	µA
	Signal Input Current (V_{IL} = 0.4 V) (V_{CC} = 5.25 V)	I_{IL}	—	—	–16	mA

Notes: [1]Power source is required to be variable from 88 to 100.5 VDC.

[2]Specified value of V_S is indicated on the back (component mounted side) of each unit. Supply voltage should be trimmed to this specified value.

[3]Current I_S (and brightness) depends on horizontal frequency (1/H). Above values of I_S are specified on condition of standard horizontal frequency (37 µs/H).

[4]For power supply design purposes, I_S (for display) becomes 0 mA, (no load) under the following conditions.

i) V_{CC} is not applied

ii) 2 frame periods after V_{CC} is applied (I_S is in operation after 3 frame synchronous pulses are applied)

iii) $\overline{H_{SYNC}}$ is not applied

iv) CLK is not applied

MECHANICAL SPECIFICATIONS

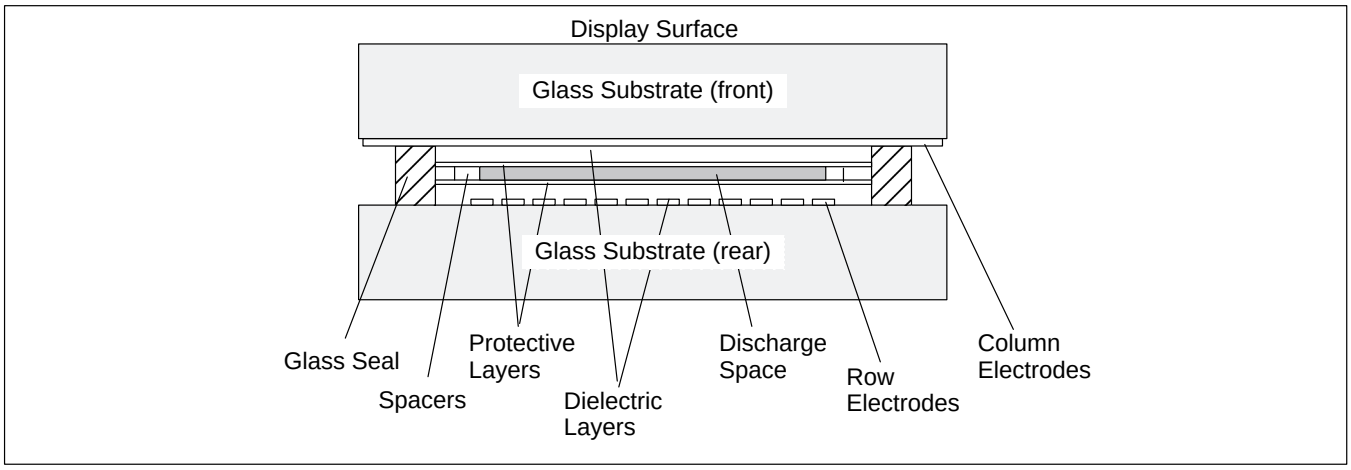
Physical Specifications

Item	Value
Number of Display Dots	640 (H) × 480 (V) dots (307,200 dots)
Dot Pitch	0.36 (H) mm × 0.36 (V) mm
Dot Size	Approximately 0.2 mm (0.008 in.) dia.
Effective Screen Area	230.04 (H) mm × 172.44 (V) mm
Gray Scale	4 levels Approximately 100%, 67%, 33%, and 0%
Display Color	Neon orange
Dot Brightness (peak) (plane average)	110 cd/m^2 (43.5 fL) at maximum brightness level (typ.) 15 cd/m^2 (5.9 fL) (typ.)
Viewing Angle	160 degrees min.
Brightness Unevenness	30% max.
Weight	Approximately 1.0 kg
Contrast	20:1 min

Performance Specifications

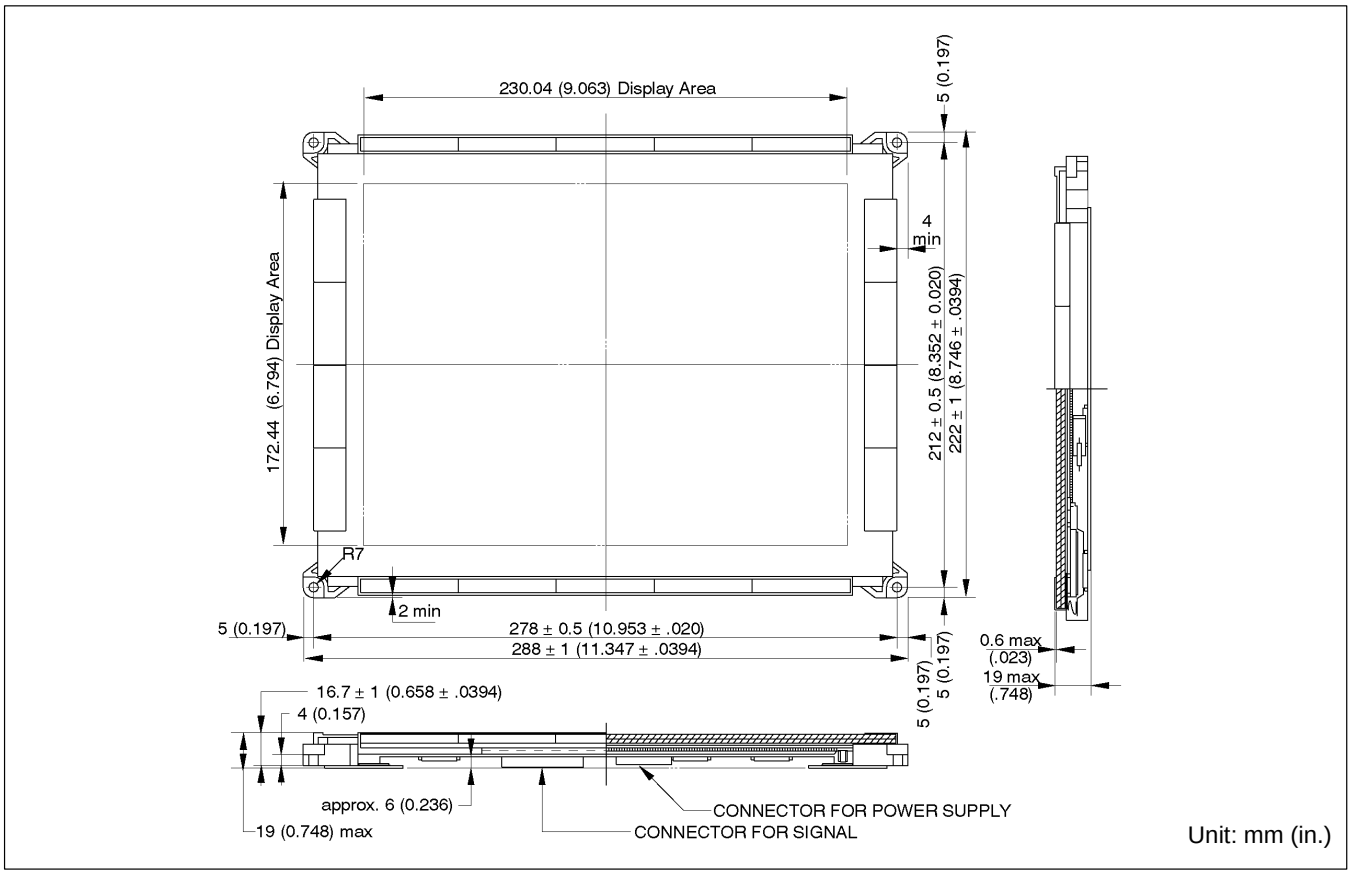
Item	Value
Operating Temperature	0 to 50°C
Storage Temperature	-20 to 70°C
Humidity	20 to 85% RH (no condensation)
Atmospheric Pressure Durability	Operation: 700 to 1114 mb Non-operation: 340 to 1114 mb
Vibration Frequency: Acceleration: Time:	 10 to 55 Hz 2 G (max.) Operation: 5 min. in X, Y, and Z direction Non-operation: 2 hours in X, Y, and Z direction
Shock Acceleration: Time:	 40 G max. in X and Y direction 20 G max. in Z direction 11 ms max.

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

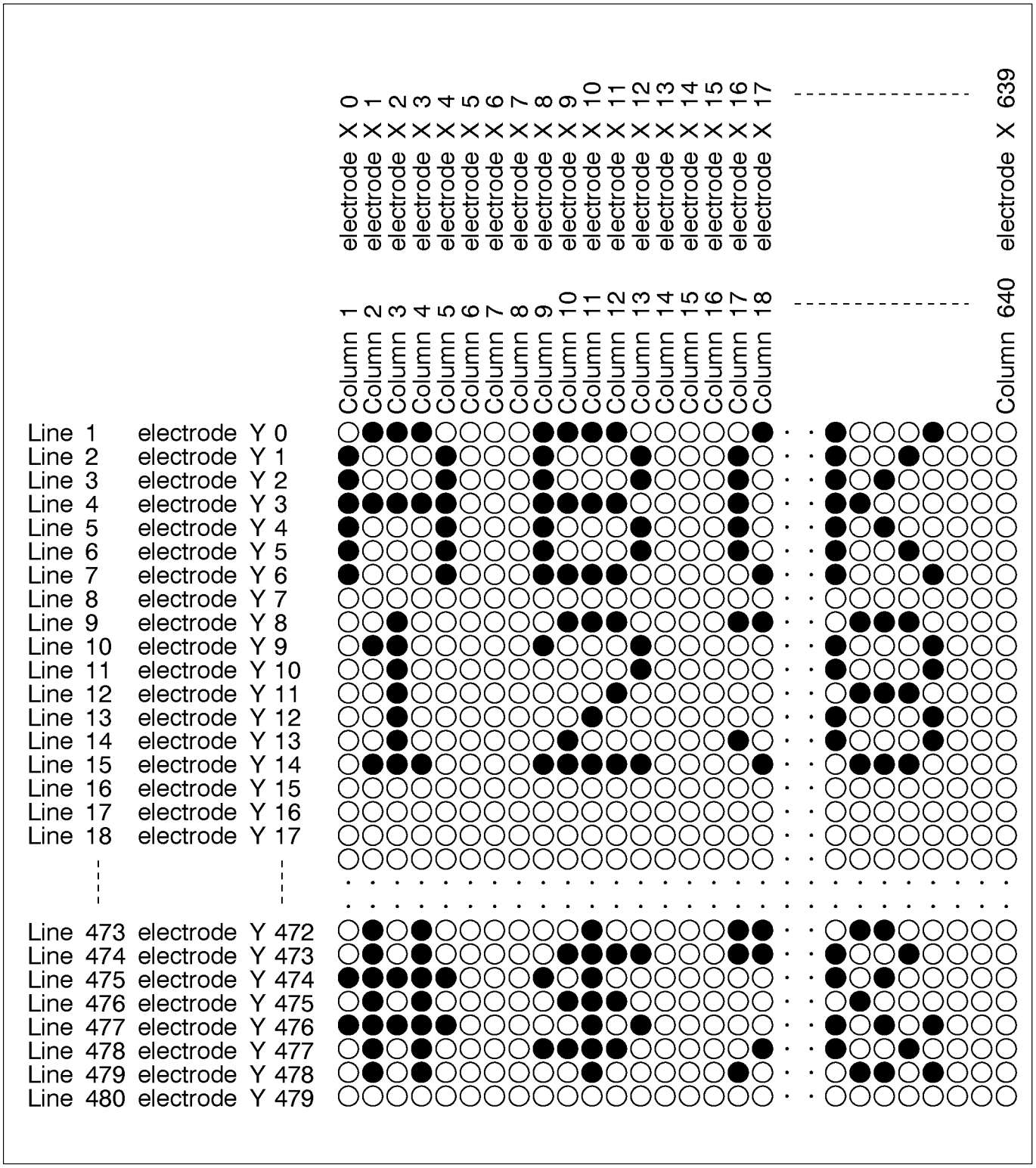


INTERFACE SIGNALS

Types of Signals (TTL Compatible)

<table>
<tr><th>Name of Signal</th><th>Symbol</th><th>Function</th></tr>
<tr><td>Data Signal</td><td>D0
D1</td><td>2 Bit Parallel Dot Data. The figure on the following page shows the relationship between display data and display dots.
Relationship Between Data and Gray Scale Level
<table>
<tr><th>D1</th><th>D0</th><th>Gray Scale Level
(Relative Brightness)</th></tr>
<tr><td>0</td><td>0</td><td>0%</td></tr>
<tr><td>0</td><td>1</td><td>low – 33%</td></tr>
<tr><td>1</td><td>0</td><td>medium – 67%</td></tr>
<tr><td>1</td><td>1</td><td>high – 100%</td></tr>
</table></td></tr>
<tr><td>Clock Signal</td><td>CLK</td><td>The input signal which controls the input timing of the display data. Dot data is read into the shift register at the rising edge of each signal.
The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 640.</td></tr>
<tr><td>Line Synchronous Signal</td><td>$\overline{H_{SYNC}}$</td><td>The input signal which controls the scanning timing of the line electrode. Y address increment to select the next line electrode is done at the falling edge of each signal.
The number of $\overline{H_{SYNC}}$ signals during the period $\overline{V_{SYNC}}$ must be 482 or more even numbers.</td></tr>
<tr><td>Frame Synchronous Signal</td><td>$\overline{V_{SYNC}}$</td><td>The input signal which controls the refresh speed of the screen. The scanning position returns to the first electrode (home position) at the falling edge of the $\overline{V_{SYNC}}$ signal.</td></tr>
</table>

Relationship Between Display Data and Display Dots

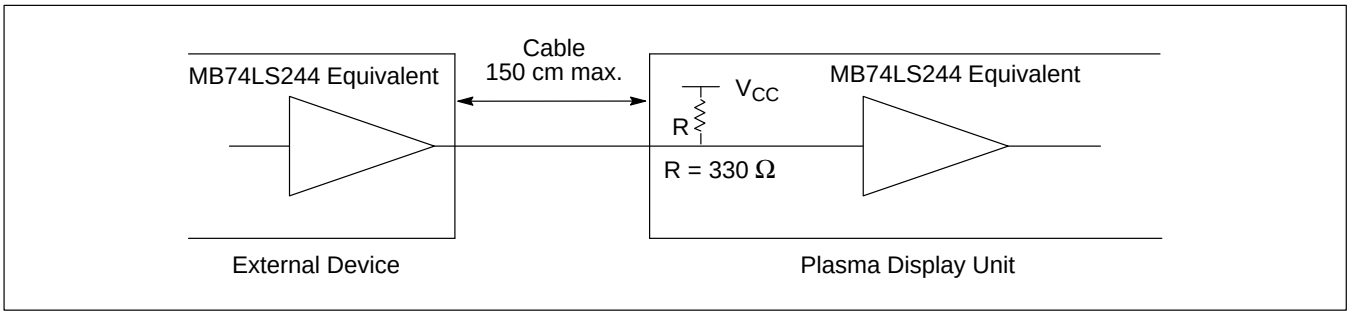


Interface Signal Timing Table

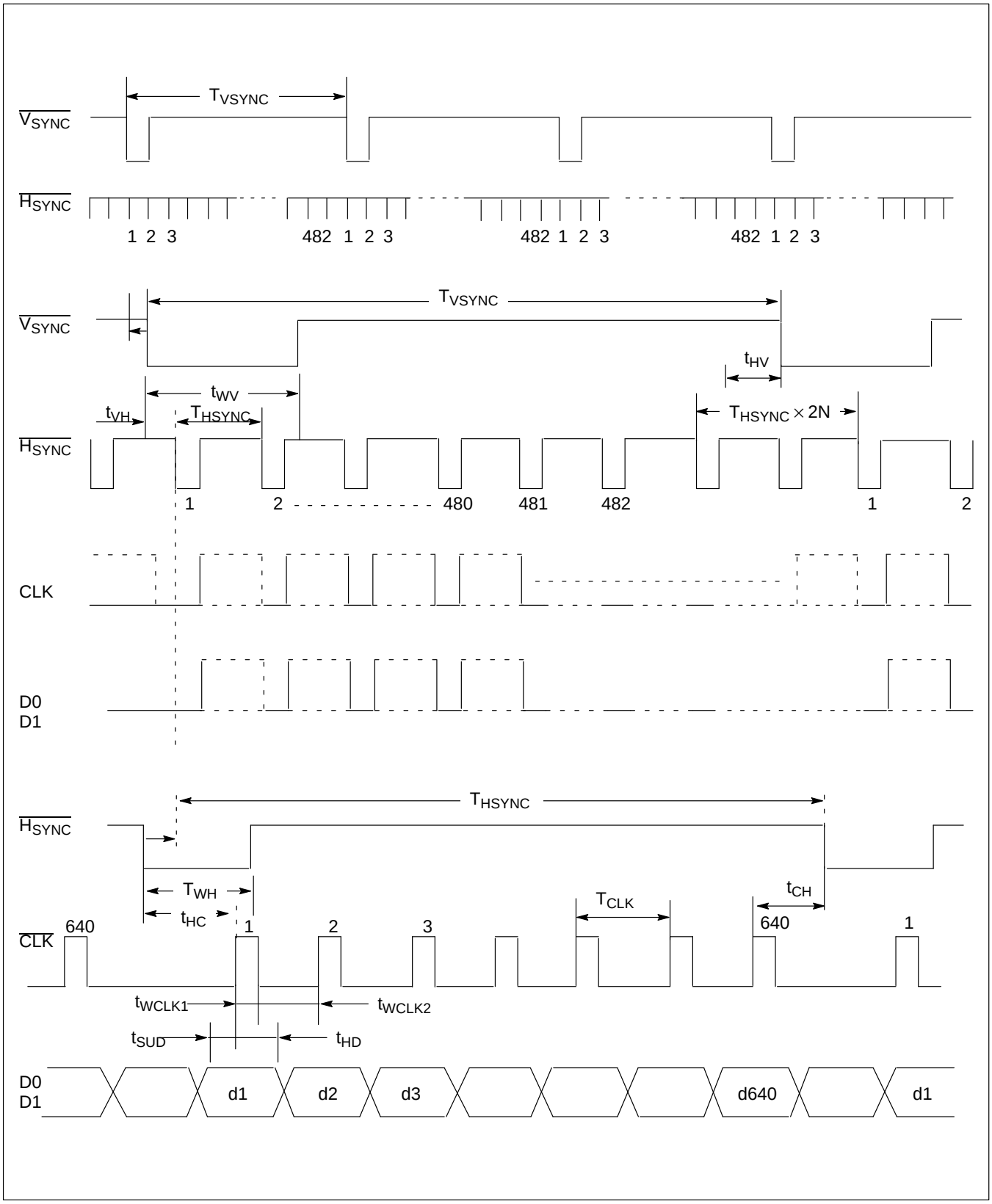
Symbol	Description	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}	A Cycle of Vertical Synchronous Signal		16.7	20	ms	Frame Freq.: 60 Hz
t_{WV}[1]	Pulse Width of Vertical Synchronous Signal	1	—	—	H	H: Horizontal Freq.
t_{VH}	Delay Time $\overline{V_{SYNC}}$ – $\overline{H_{SYNC}}$	1			µs	
t_{HV}	Delay Time $\overline{H_{SYNC}}$ – $\overline{V_{SYNC}}$	2			µs	
T_{HSYNC}	A Cycle of Horizontal Synchronous Signal	31		36	µs	
t_{WH}	Pulse Width of Horizontal Synchronous Signal	2	5		µs	
t_{HC}	Delay Time $\overline{H_{SYNC}}$ – CLK	1			µs	
t_{CH}	Delay Time CLK – $\overline{H_{SYNC}}$	1	3		µs	
T_{CLK}	A Cycle of Clock Signal	35			ns	
t_{WCLK1}[2]	Pulse Width of Clock Signal (H)	17			ns	
t_{WCLK2}[2]	Pulse Width of Clock Signal (L)	17			ns	t_{WCLK1} + t_{WCLK2} = T_{CLK}
t_{SUD}	Set Up Time for Data	15			ns	
t_{HD}	Hold Time for Data	15			ns	

Notes: [1]$t_{WC} > T_{HSYNC}$
[2]Recommended ratio between t_{WCLK1} and t_{WCLK2}; 1:1

Interface Circuit



Interface Signal Timing Chart



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-605Q026-G/S

Pin No.	Symbol	Pin No.	Symbol
1	$\overline{V_{SYNC}}$	2	S. GND
3	$\overline{H_{SYNC}}$	4	S. GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S. GND
15	D0	16	S. GND
17	D1	18	S. GND
19	CLK	20	S. GND
21	N.C.	22	N.C.
23	N.C.	24	N.C.
25	V_{CC}	26	V_{CC}

Notes: Applicable Connector: FCN-607B 026-G/D

N.C. means “No Connection.”

Power Supply Connector

FCN-815P-009TA

Pin No.	Symbol
1	V_{CC}
2	GND (L)
3	N.C.
4	GND (H)
5	V_S
6	N.C.
7	N.C.
8	GND (H)
9	V_R*

Notes: Applicable Connectors:
FCN-813J009-A, Housing
FCN-813J-T/Q, Contact for Manual Use
FCN-813J-T/R, Contact for Automatic Use

* This PDP unit outputs the voltage V_R from 0 to 2.5 VDC through the ninth terminal of power supply connector.

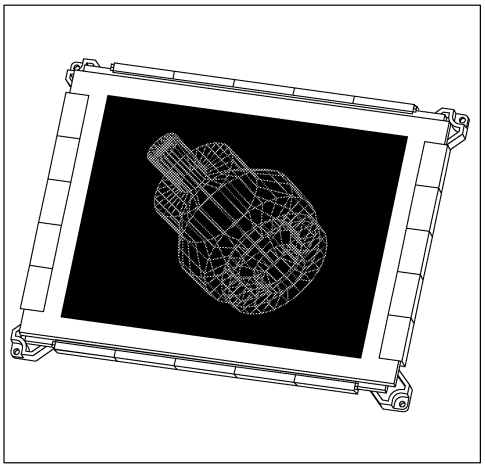
June 1992
Edition 2.0

FUJITSU

DATA SHEET

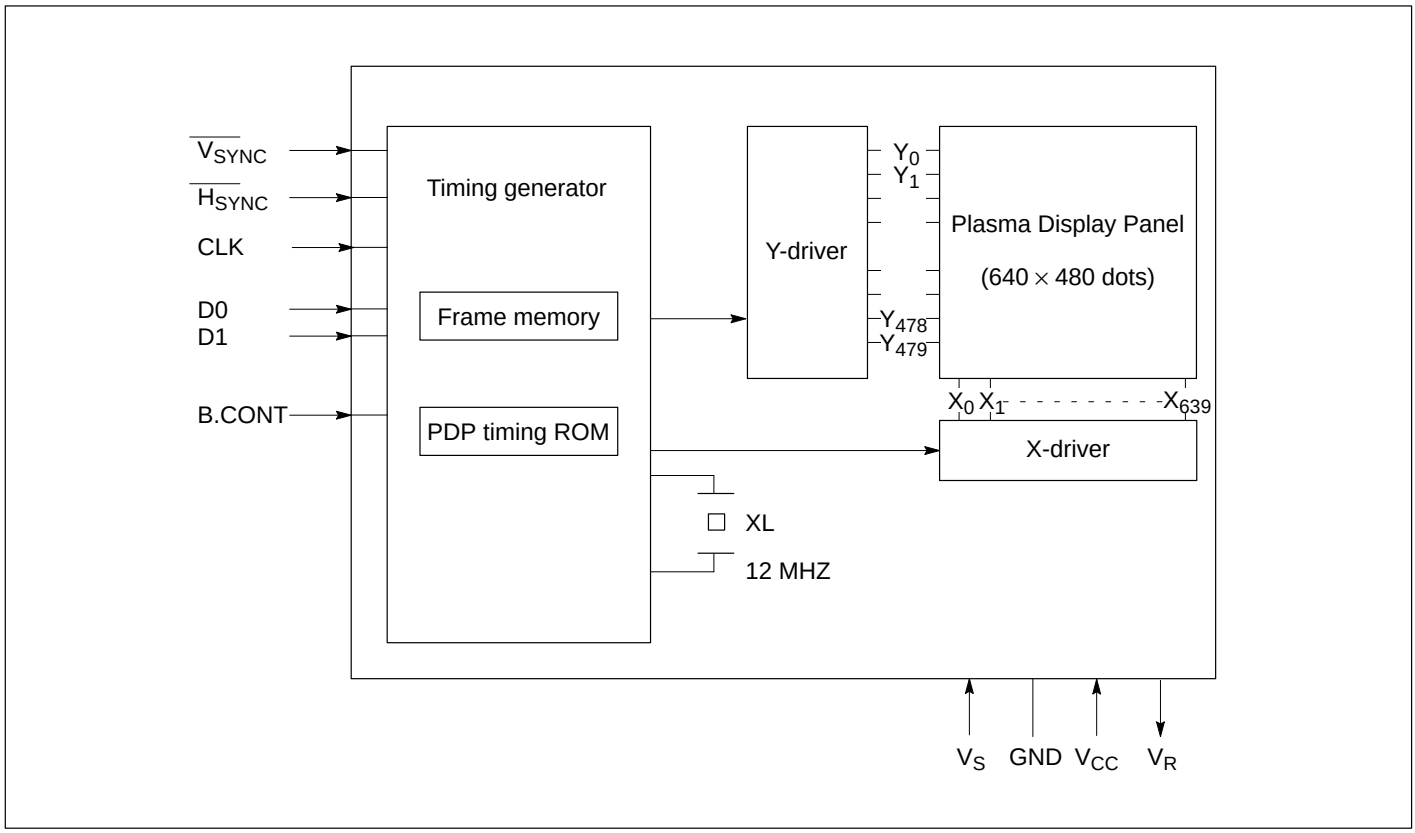
FPF8060HRUK
Plasma Display Graphics Unit

The FPF8060HRUK plasma display unit consists of an AC gas discharge plasma display unit with bistable memory and associated driver circuitry. Fujitsu's proprietary control method provides a clear display with a four-level gray scale. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8060HRUK a highly reliable display device.



- Four-level gray scale
- High resolution
- Bright, even, orange-on-black display
- No flicker or warp
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Sustain voltage	V_S	120 V
Logic voltage	V_{CC}	7 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for sustain*	V_S	88	95	100.5	V
Supply current for sustain (V_S = 95 V)	I_S			340	mA
Supply voltage for logic	V_{CC}		5		V
Supply current for logic (V_{CC} = 5 V)	I_{CC}	0.15		0.45	A
Signal input voltage for logic 1	V_{IH}	2.0		5.25	V
Signal input current for logic 1 (V_{IH} = 2.75)	I_{IH}			20	µA
Signal input voltage for logic 0	V_{IL}	-0.5		0.4	V
Signal input current for logic 0 (V_{IL} = 2.75 V)	I_{IL}			-16	mA

Note: * The power source is required to be variable from 88 to 100.5V DC.

MECHANICAL SPECIFICATIONS

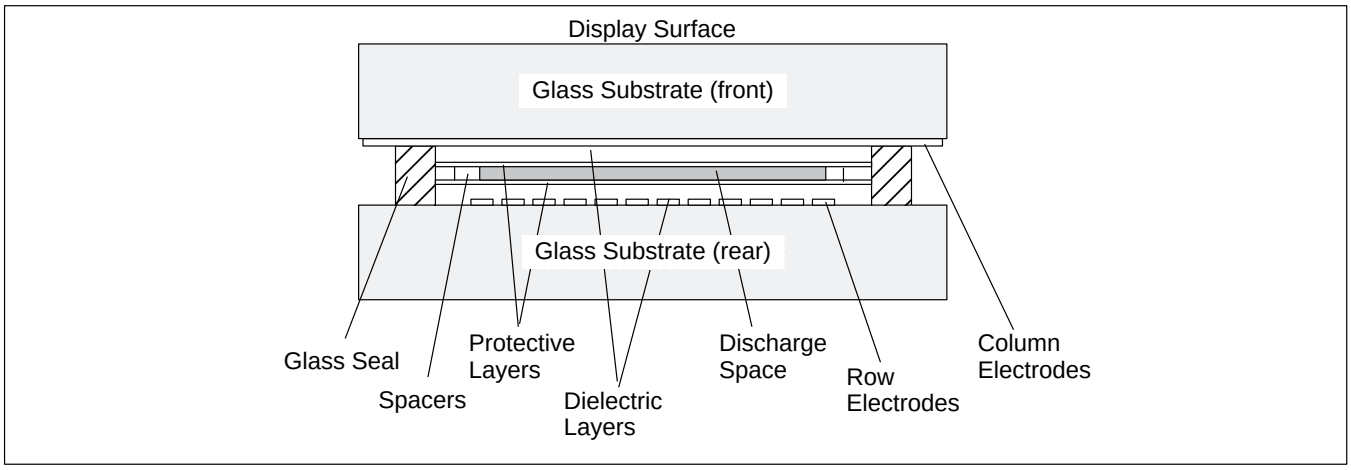
Physical Specifications

Item	Value
Number of display dots	640 × 480 dots (307,200 dots)
Dot pitch	0.33 (H) × 0.33 (V) mm (0.013 × 0.013 in.)
Dot size	0.2 mm (0.008 in.) dia
Effective display area	211 (H) × 158 (V) mm (8.307 × 6.220 in.)
Display color	Neon orange
Gray scale	4-level (Approx. 100%, 67%, 33%, 0%)
Brightness	110 cd/m^2
Contrast ratio	20 : 1 min
Viewing angle	160° min
Weight	Approx. 1 kg
External dimensions	See External Dimensions

Performance Specifications

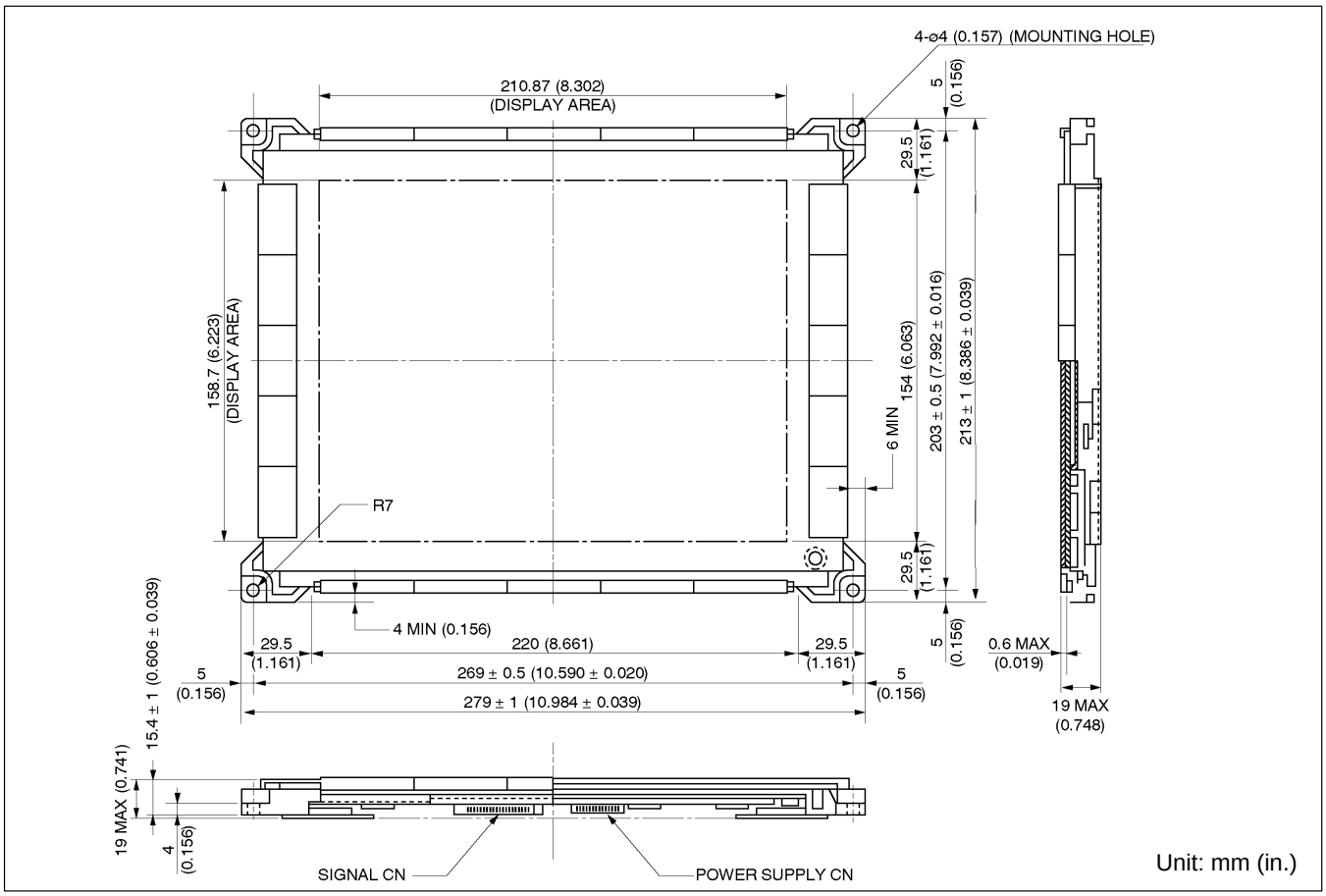
Item	Symbol	Value
Operating temperature	T_{OP}	0 to +50°C
Operation humidity	RH_{OP}	20 to 85%
Storage temperature	T_{STG}	–20 to +70°C
Storage humidity	RH_{STG}	20 to 85%
Vibration	V	2 G
Shock	S	40 G
Pressure (non-operating)		340 to 1114 hPa

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

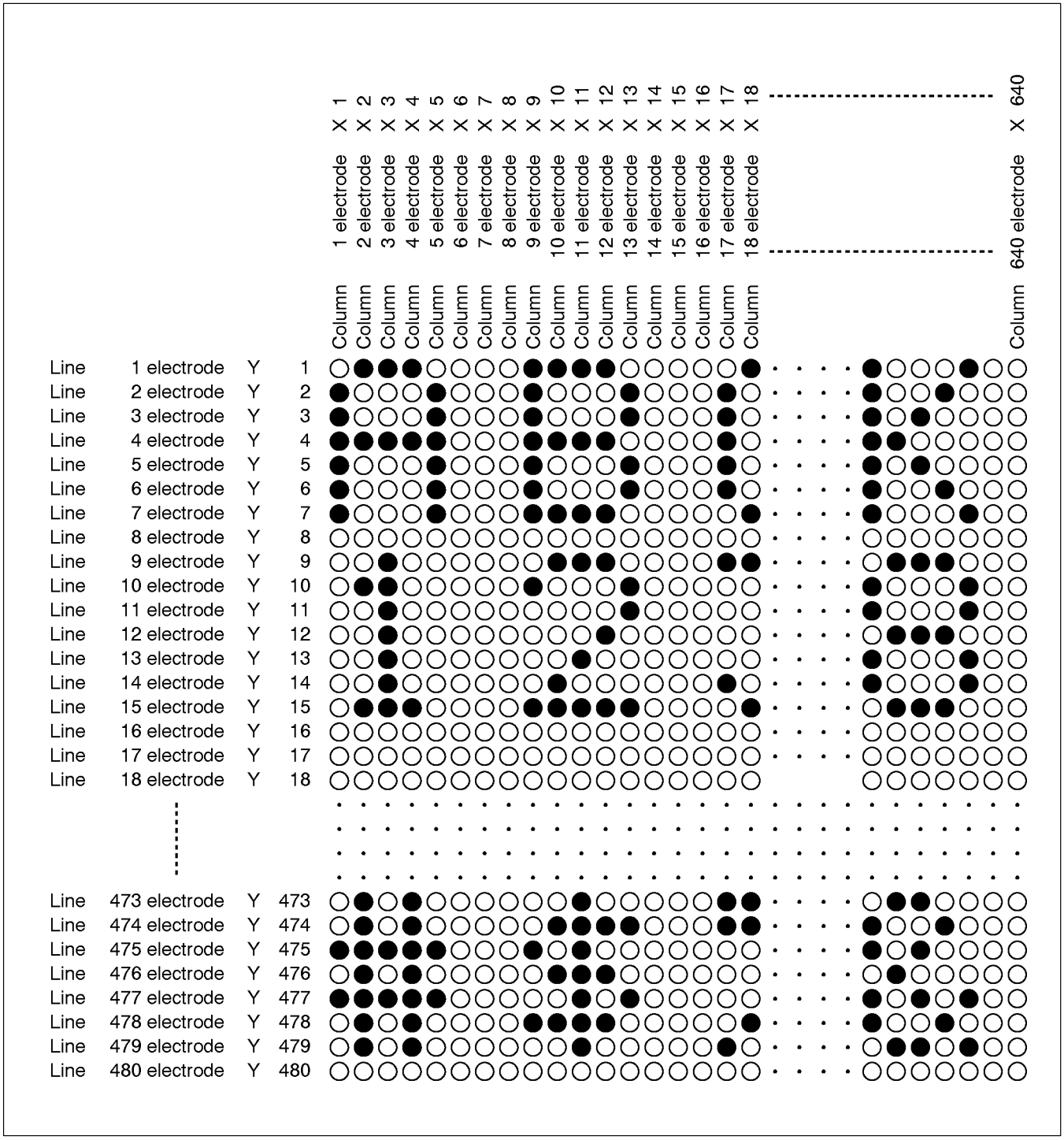


INTERFACE SIGNALS

Type of Signals (TTL Compatible)

<table>
<tr><th>Signal</th><th>Symbol</th><th>Logic</th><th>Definition and Function</th></tr>
<tr><td>Display data</td><td>D0
D1</td><td>Posi</td><td>2-bit display data.
Relation between Data and Gray scale level is shown below.
Relationship Between Data and Gray Scale Level
<table>
<tr><th>D1</th><th>D0</th><th>Gray scale level</th><th>(Relative brightness)</th></tr>
<tr><td>0</td><td>0</td><td></td><td>(0)</td></tr>
<tr><td>0</td><td>1</td><td>Low</td><td>(33%)</td></tr>
<tr><td>1</td><td>0</td><td>Medium</td><td>(67%)</td></tr>
<tr><td>1</td><td>1</td><td>High</td><td>(100%)</td></tr>
</table></td></tr>
<tr><td>Clock signal</td><td>CLK</td><td>Posi</td><td>The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 640.</td></tr>
<tr><td>Line synchronous</td><td>$\overline{H_{SYNC}}$</td><td>Nega</td><td>The number of $\overline{H_{SYNC}}$ signals in one cycle of $\overline{V_{SYNC}}$ must be 482 or more even numbers.</td></tr>
<tr><td>Frame synchronous</td><td>$\overline{V_{SYNC}}$</td><td>Nega</td><td>The input signal controls the refresh speed of the screen.</td></tr>
<tr><td>Brightness control</td><td>B.CONT</td><td colspan="2">The input signal which controls the screen brightness. Brightness is its maximum at logical “High” and 0% of maximum at logical “Low.”</td></tr>
</table>

Relationship Between Display Data and Display Dots

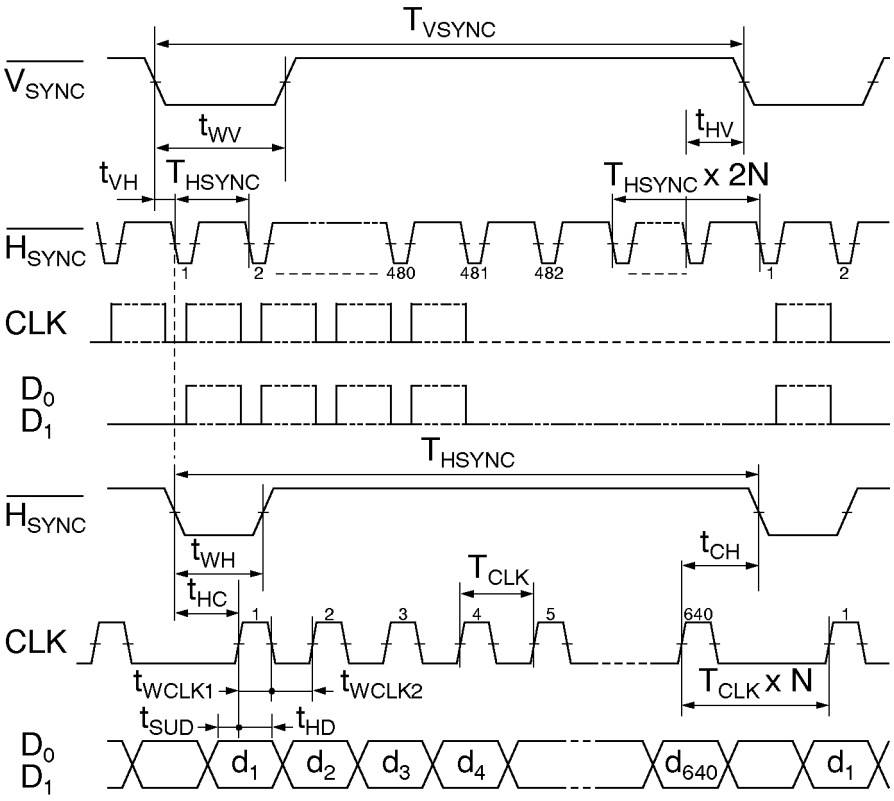


Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit
T_{VSYNC}	—	16.7	20	ms
t_{WV}[1]	—	—	—	µs
t_{VH}	1	—	—	µs
t_{HV}	2	—	—	µs
T_{HSYNC}	35	37	45	µs
t_{WH}	2	5	—	µs
t_{HC}	2	—	—	µs
t_{CH}	2	3	—	µs
T_{CLK}	44	—	—	ns
$t_{WCLK1,2}$[2]	22	—	—	ns
t_{SUD}	22	—	—	ns
t_{HD}	22	—	—	ns

Notes: [1] $T_{WV} > T_{HSYNC}$
[2] Recommended ratio between t_{WCLK1} and t_{WCLK2} is 1 : 1.

Interface Signal Timing Chart



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-605Q26-G/S (Fujitsu)

Pin No.	Signal	Pin No.	Signal
1	$\overline{V_{SYNC}}$	2	S.GND
3	$\overline{H_{SYNC}}$	4	S.GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S.GND
15	D0	16	S.GND
17	D1	18	S.GND
19	CLK	20	S.GND
21	B.CONT	22	N.C.
23	N.C.	24	N.C.
25	V_{CC}	26	V_{CC}

Applicable connector:
FCN-607B026-G/D

Power Supply Connector

FCN-815P009-TA (Fujitsu)

Pin No.	Signal
1	V_{CC}
2	GND (L)
3	N.C.
4	GND (H)
5	V_S
6	N.C.
7	N.C.
8	N.C.
9	V_R*

Applicable connectors:
FCN-813J009-A housing
FCN-813J-T/A contact

* This terminal is connected only when FPF07P-AC100 power supply unit is used.

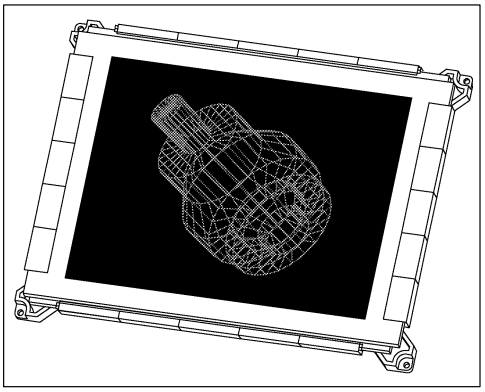
June 1992
Edition 1.0

FUJITSU

DATA SHEET

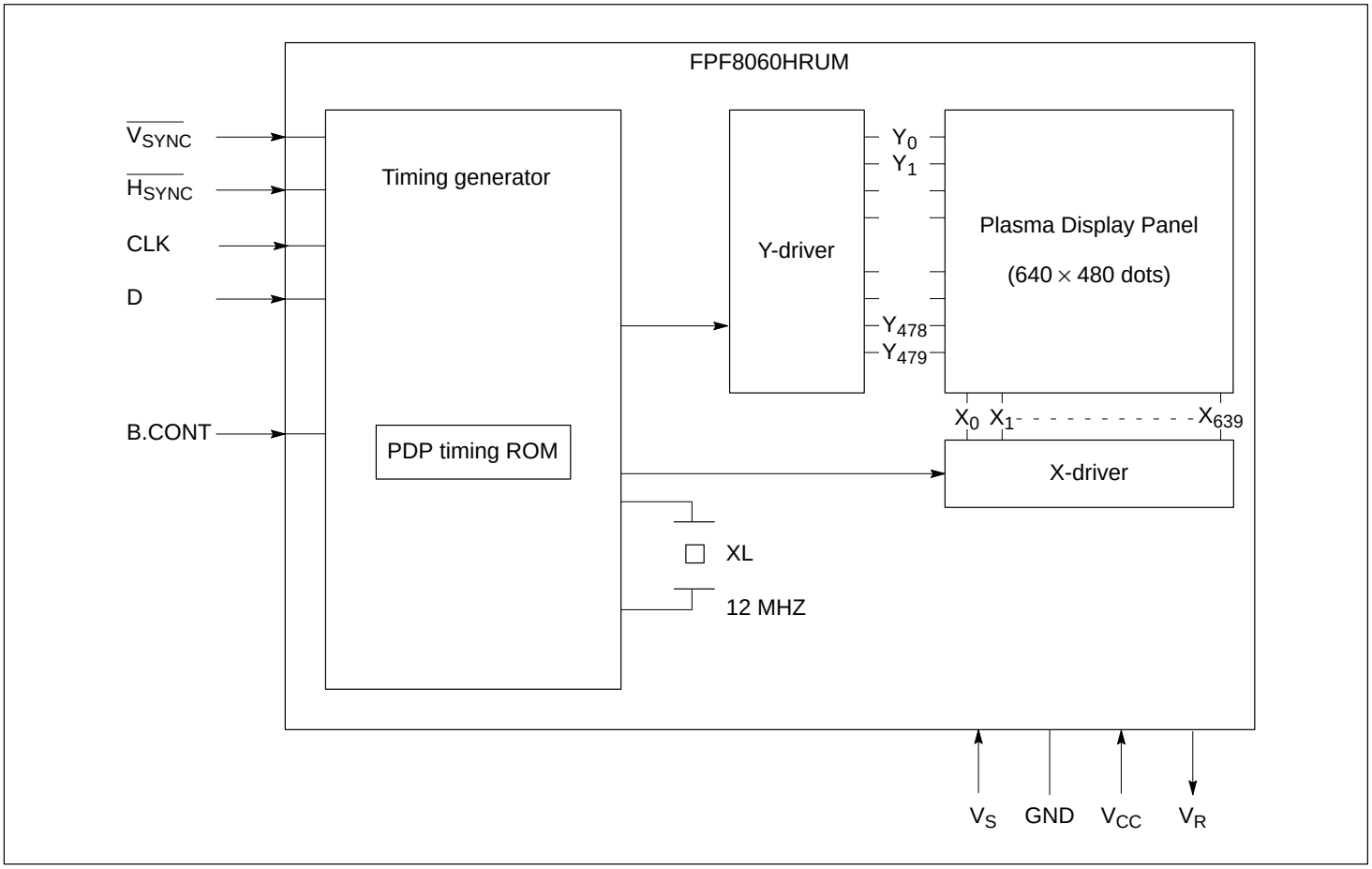
FPF8060HRUM
Plasma Display Graphics Unit

The FPF8060HRUM plasma display unit consists of an AC gas discharge plasma display unit with bistable memory and associated driver circuitry. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF8060HRUM a highly reliable display device.



- High resolution
- Bright, even, orange-on-black display
- No flicker or warp
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Sustain voltage	V_S	120 V
Logic voltage	V_{CC}	7 V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for sustain*	V_S	88	95	100.5	V
Supply current for sustain (V_S = 95 V)	I_S			340	mA
Supply voltage for logic	V_{CC}		5		V
Supply current for logic (V_{CC} = 5 V)	I_{CC}	0.15		0.45	A
Signal input voltage for logic 1	V_{IH}	2.0		5.25	V
Signal input current for logic 1 (V_{IH} = 2.75)	I_{IH}			20	µA
Signal input voltage for logic 0	V_{IL}	–0.5		0.4	V
Signal input current for logic 0 (V_{IL} = 2.75 V)	I_{IL}			–16	mA

Note: The power source is required to be variable from 88 to 100.5V DC.

MECHANICAL SPECIFICATIONS

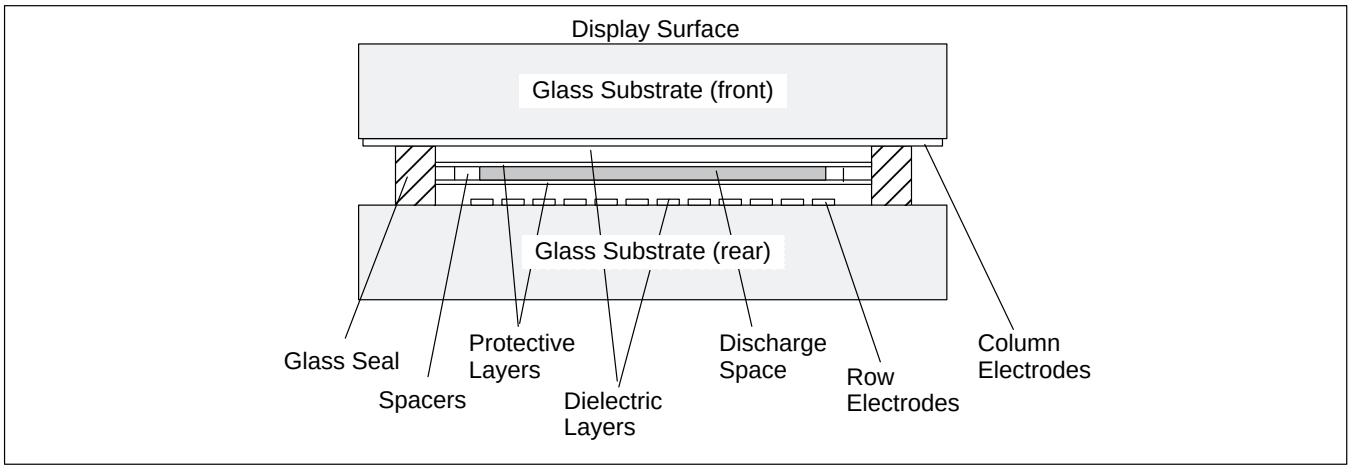
Physical Specifications

Item	Value
Number of display dots	640 × 480 dots (307,200 dots)
Dot pitch	0.33 (H) × 0.33 (V) mm (0.013 × 0.013 in.)
Dot size	0.2 mm (0.008 in.) dia
Effective display area	211 (H) × 158 (V) mm (8.307 × 6.220 in.)
Display color	Neon orange
Brightness	110 cd/m^2
Contrast ratio	20 : 1 min
Viewing angle	160° min
Weight	Approx. 1 kg
External dimensions	See External Dimensions

Performance Specifications

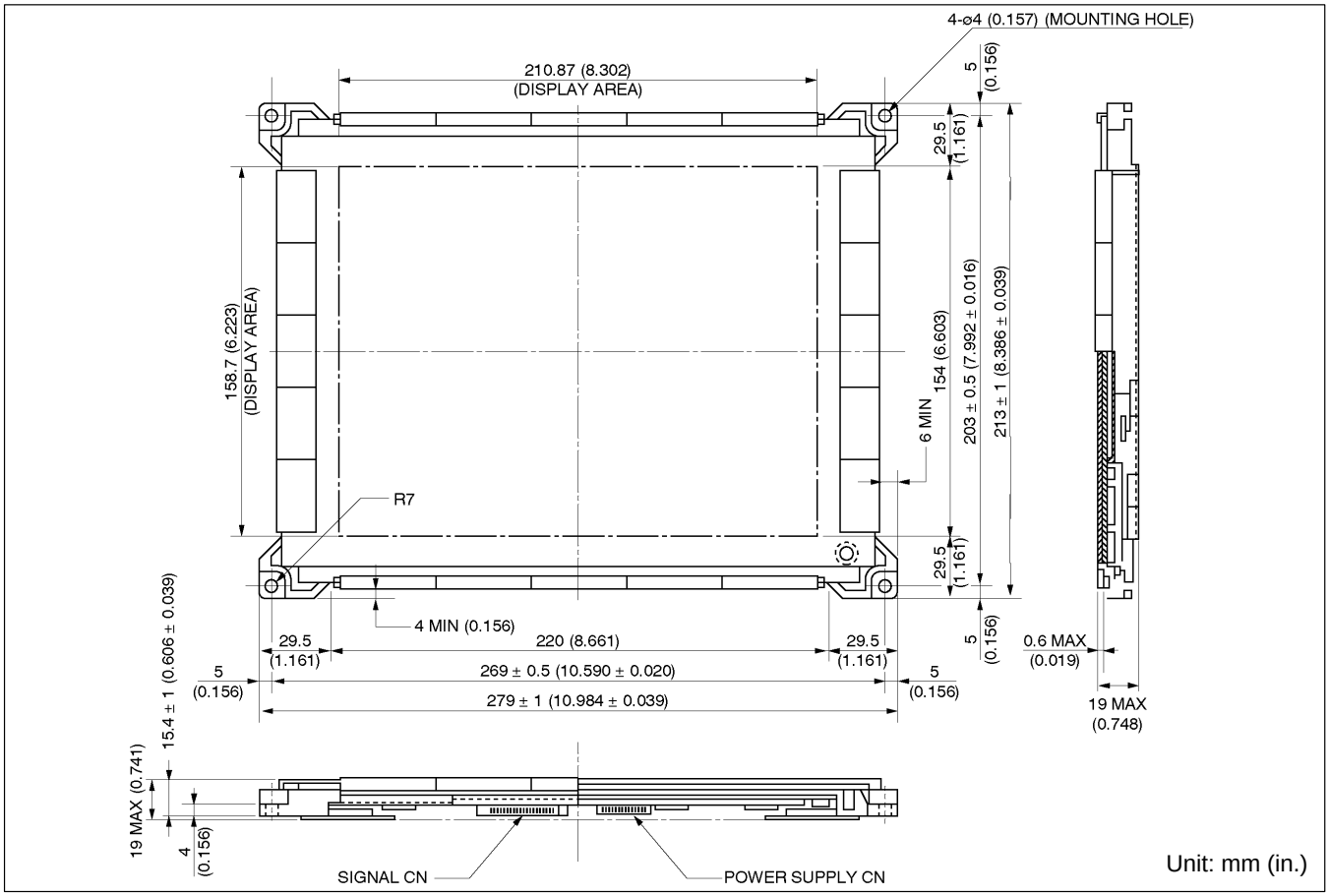
Item	Symbol	Value
Operating temperature	T_{OP}	0 to +50°C
Operation humidity	RH_{OP}	20 to 85%
Storage temperature	T_{STG}	–20 to +70°C
Storage humidity	RH_{STG}	20 to 85%
Vibration	V	2 G
Shock	S	40 G
Pressure (non-operating)		340 to 1114 hPa

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

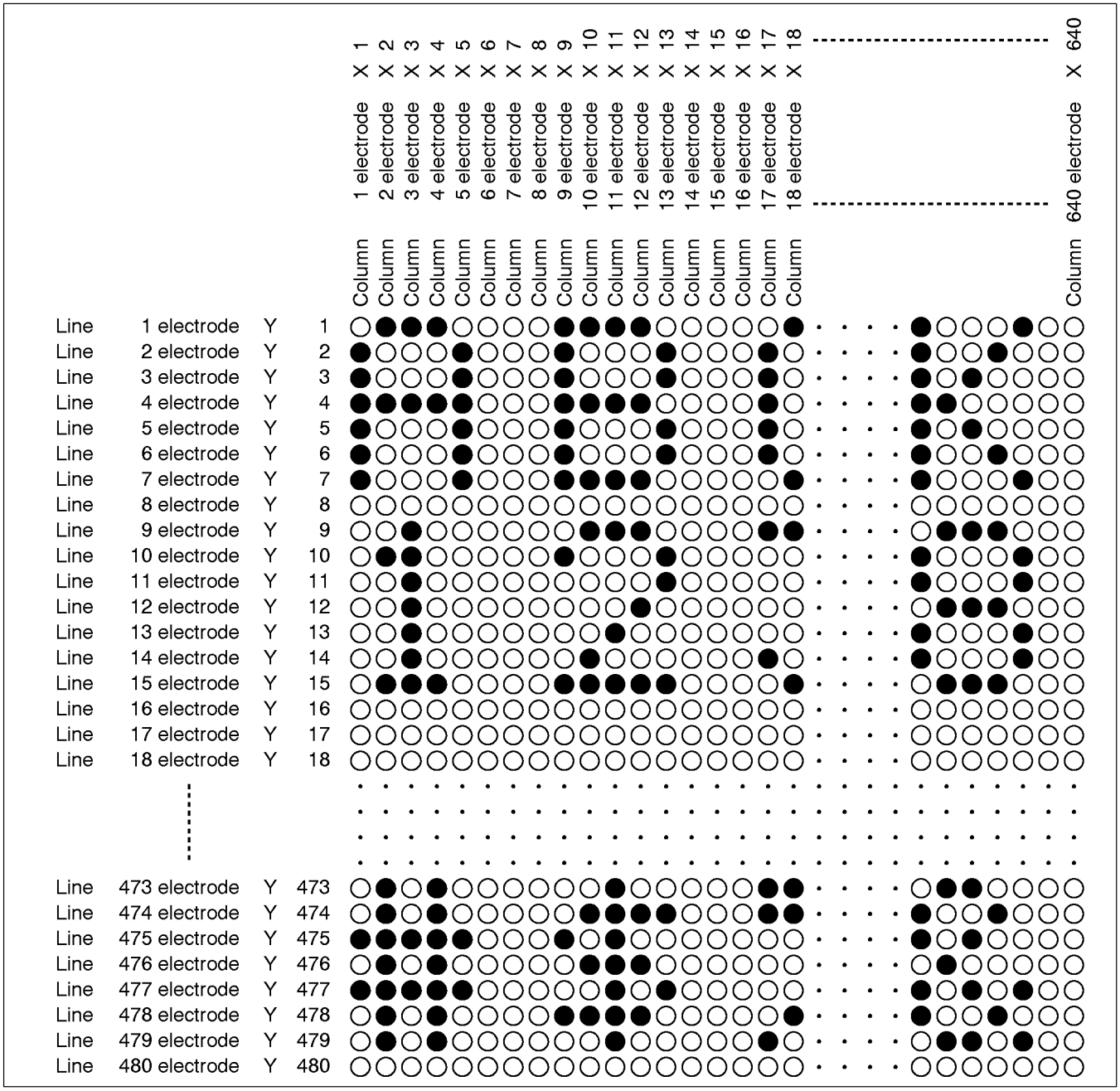


INTERFACE SIGNALS

Type of Signals (TTL Compatible)

Signal	Symbol	Logic	Definition and Function
Display data	D	Posi	Serial display data. Relation between display data and display dots is shown in the following figure.
Clock signal	CLK	Posi	The number of clock signals in one cycle of $\overline{H_{SYNC}}$ must be 640.
Line synchronous	$\overline{H_{SYNC}}$	Nega	The number of $\overline{H_{SYNC}}$ signals in one cycle of $\overline{V_{SYNC}}$ must be 482 or more even numbers.
Frame synchronous	$\overline{V_{SYNC}}$	Nega	The input signal which controls the refresh speed of the screen.
Brightness control	B.CONT	The input signal which controls the screen brightness. Brightness is its maximum at logical “High” and 0% of maximum at logical “Low.”	

Relationship Between Display Data and Display Dots

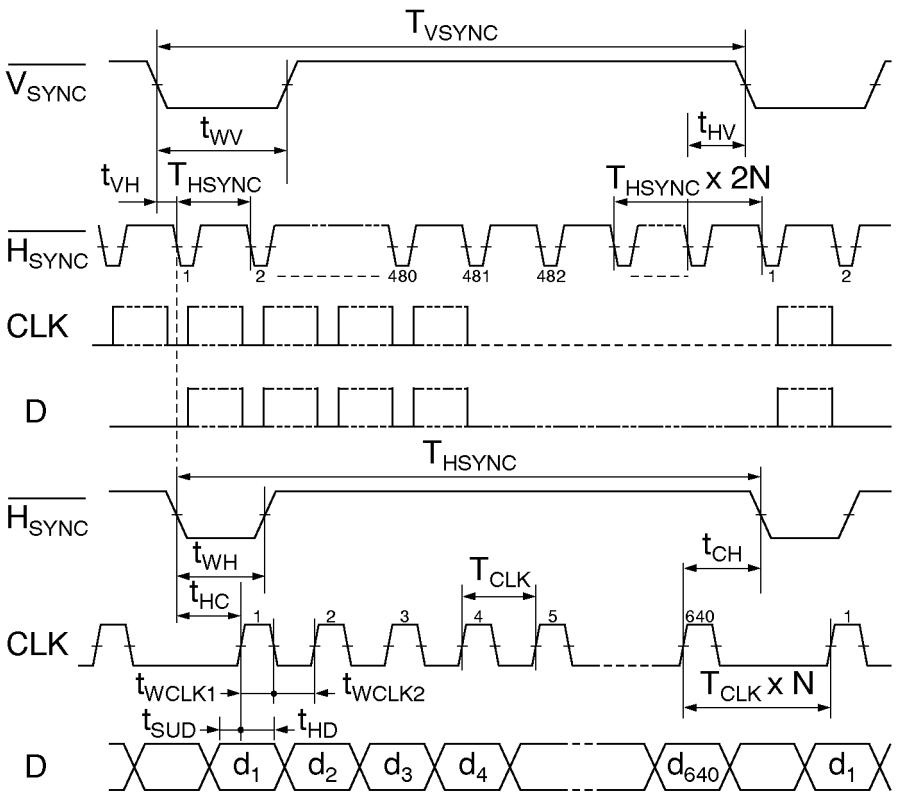


Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit
T_{VSYNC}	—	44.46	—	ms
t_{WV}[1]	—	—	—	µs
t_{VH}	1	—	—	µs
t_{HV}	2	—	—	µs
T_{HSYNC}	88	90	92	µs
t_{WH}	2	6	—	µs
t_{HC}	2	—	—	µs
t_{CH}	2	3	—	µs
T_{CLK}	44	—	—	ns
$t_{WCLK1,2}$[2]	22	—	—	ns
t_{SUD}	22	—	—	ns
t_{HD}	22	—	—	ns

Notes: [1]$T_{WV} > T_{HSYNC}$.
[2]Recommended ratio between t_{WCLK1} and t_{WCLK2} is 1 : 1.

Interface Signal Timing Chart



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-605Q26-G/S (Fujitsu)

Pin No.	Signal	Pin No.	Signal
1	$\overline{V_{SYNC}}$	2	S.GND
3	$\overline{H_{SYNC}}$	4	S.GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S.GND
15	D	16	S.GND
17	N.C.	18	S.GND
19	CLK	20	S.GND
21	B.CONT	22	N.C.
23	N.C.	24	N.C.
25	V_{CC}	26	V_{CC}

Applicable connector:
FCN-607B026-G/D

Power Supply Connector

FCN-815P009-TA (Fujitsu)

Pin No.	Signal
1	V_{CC}
2	GND (L)
3	N.C.
4	GND (H)
5	V_S
6	N.C.
7	N.C.
8	N.C.
9	V_R*

Applicable connectors:
FCN-813J009-A housing (Fujitsu)
FCN-813J-T/A contact (Fujitsu)

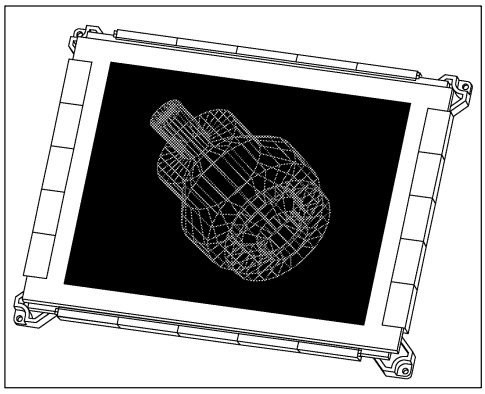
* This terminal is connected only when FPF07P-AC100 power supply unit is used.

August 1989
Edition 1.0

FUJITSU

DATA SHEET

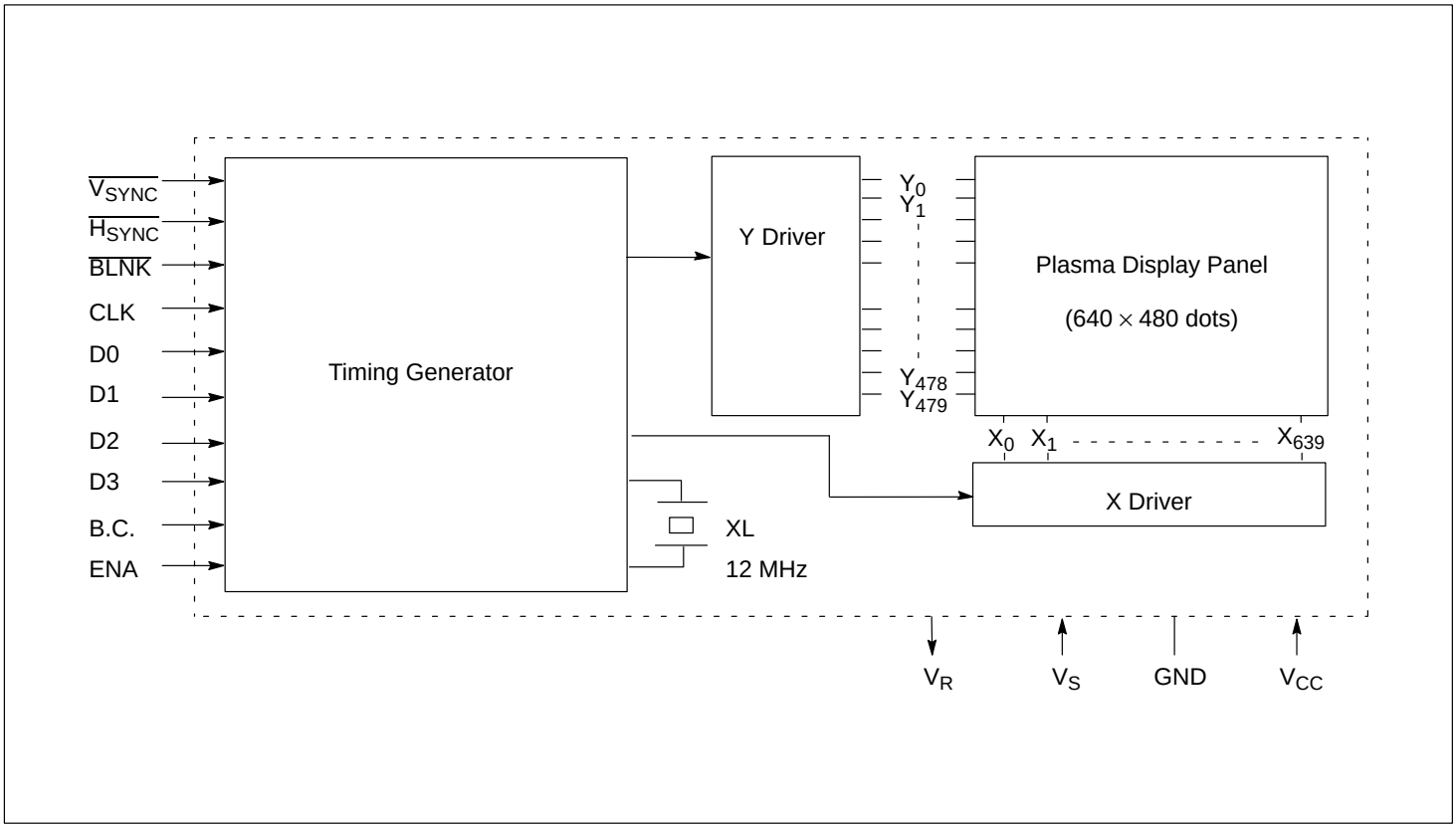
FPF8060HRUS–120
AC Memory Plasma Display Unit



The FPF8060HRUS-120 plasma display unit is a thin, flat display device that uses gas discharge luminescence. The display is clear and easy to read, has a long life, and is highly reliable. The FPF8060HRUS-120 consists of an AC gas discharge plasma display panel with bistable memory function and driver circuitry. The low-profile FPF8060HRUS-120 display is ideal for fast, cost-efficient, easy design where space is at a premium, in applications such as portable computers, medical instrumentation, or factory automation.

- Bright, even, orange-on-black display
- Sixteen-level gray scale
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability
- Capable of interfacing with standard VGA card feature connectors
- 50,000-hour reliability with no brightness degradation over the life of the product

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Voltage for Sustain Driver	V_S	120 V
Voltage for Logic	V_{CC}	7 V

DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage (H – Level)	V_{IH}		2.0	—	5.25	V
Input Voltage (L – Level)	V_{IL}		–0.5	—	0.8	V
Input Current (H – Level)	I_{IH}	V_{IH} = 2.75 V, V_{CC} = 5.25 V	—	—	20	µA
Input Current (L – Level)	I_{IL}	V_{IH} = 0.4 V, V_{CC} = 5.25 V	—	—	–16	mA

Input Power

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
For Display	Voltage [1,2]	V_S	Variable	88	95	100.5	V
	Ripple/Noise	V_{NRS}	At Resistive Load	—	—	500	mV
	Stability (avg.)	—	At Resistive Load	—	—	±1.5	%
	(peak)	—	(I_S = 2 A)	—	—	-5	%
	Current (avg.) [3, 4, 5,]	I_S	T_{HSYNC} = 31.78 µs/H	50	—	340	mA
	(peak)[6]	I_{SP}	5 to 8 µs cycle	0.5	—	2	A
For Logic	Voltage	V_{CC}		4.75	5	5.25	V
	Ripple/Noise	V_{NRC}	At Resistive Load	—	—	50	mV
	Stability	—	At Resistive Load	—	—	±5	%
	Current (avg.)	I_{CC}		150	—	500	mA

Notes: [1] Variable power supply is required for voltage V_S (for display) because each display unit requires voltage within the range specified in the above table.

[2] Specific voltage for V_S is indicated on each display unit. However, when using V_R (reference voltage), it is possible to adjust the specified voltage automatically. Each display unit outputs a specific V_R voltage corresponding to the V_S voltage required by each display unit. The relationship between V_S and V_R is as follows:

$V_S = 88 + V_R \times 5$ (V)

Example: V_S = 93 V $\rightarrow$ V_R = 1.0 V

[3] Current I_S is specified under the conditions listed below.

Minimum: displayed ratio = 0%

Maximum: displayed ratio = 100%

[4] The I_S value changes corresponding to the cycle period of $\overline{H_{SYNC}}$.

[5] The value of I_S is 10 mA under the following conditions:

When V_{CC} is not supplied.

For three frame periods after V_{CC} is supplied. (Operation starts after the input of four pulses of $\overline{V_{SYNC}}$.)

When $\overline{H_{SYNC}}$ is not input.

When the enable signal level is “L” (low).

[6] 1 µs pulse width at 1_{SP} = 1 A

Output Power

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
For V_S Adjust	Voltage	V_R	At 1 kΩ Load	0	—	2.5	V
	Ripple/Noise	V_{NRR}	At 1 kΩ Load	—	—	±500	mV
	Stability (avg.)	—	At 1 kΩ Load	—	—	±0.1	%
	Current (avg.)	I_{CC}	At 1 kΩ Load	—	—	10	mA

Note: V_R is preset to relate to V_S as follows:
$V_S = 88 + V_R \times 5$ (V)
Example: $V_S = 93$ V $\rightarrow V_R = 1.0$ V

MECHANICAL SPECIFICATIONS

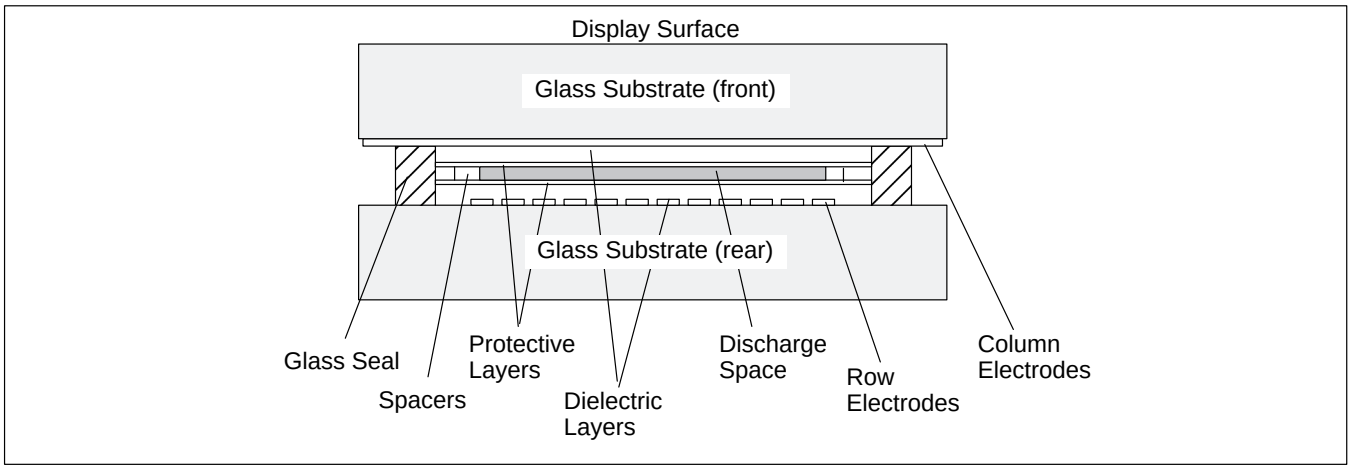
Physical Specifications

Item	Value
Number of Display Dots	640 (H) × 480 (V) dots (307,200 dots)
Dot Pitch	0.33 (H) mm × 0.33 (V) mm (0.013 in. × 0.013 in.)
Dot Size	Approx. 0.2 mm (0.008 in.) dia.
Effective Screen Area	210.87 (H) mm × 158.07 (V) mm (8.302 in. × 6.223 in.)
Gray Scale	16 levels
Display Color	Neon orange
Dot Brightness (peak) (average)	110 cd/m^2 typ. 15 cd/m^2 typ. (12 cd/m^2 min.) at 31.5 kHz frequency of $\overline{H_{SYNC}}$
Brightness Control	Variable from 10 to 100%
Contrast Ratio	20:1 min.
Viewing Angle	160° min.
Brightness Unevenness	30% max.
Weight	1 kg

Performance Specifications

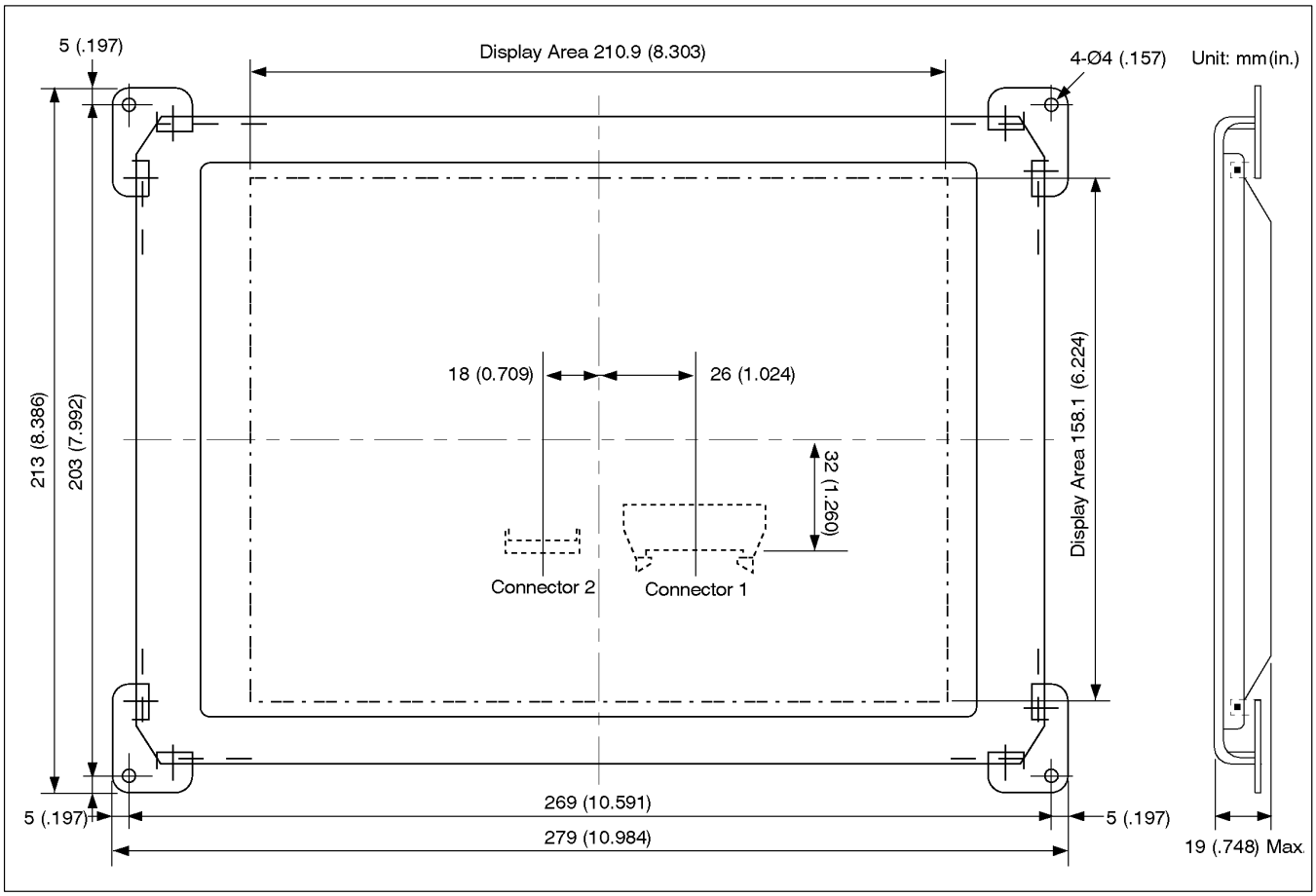
Item	Value
Vibration Acceleration: Frequency: Time:	2 G max. 10 to 55 Hz Operation: 5 minutes in X and Y direction Non-operation: 2 hours in Z direction
Shock (at non-operation) Acceleration: Time:	40 G max. in X and Y direction 20 G max. in Z direction 11 ms
Operating Temperature	0 to 50°C
Storage Temperature	–20 to 70°C
Humidity	20 to 85% RH (No Condensation)
Pressure	Operation: 70,000 to 111,400 Pa Non Operation: 34,000 to 111,400 Pa

Physical Construction and Operation



The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions



INTERFACE SIGNALS

Type of Signals (TTL Compatible)

Signal	Symbol	Signal Line	Definition and Function
Data Signal	D3 D2 D1 D0	4 Lines	Signal for display data: H = Light On, L = Light Off The relationship between display data and brightness level (gray scale level) is shown in the table below.
Clock Signal	CLK	1 Line	Timing signal to read display data (dot clock). Display data are read at the rising edge of CLK. If clock is continuous, display data are input when signal is at H level.
Blanking Signal	$\overline{BLNK}$	1 Line	Timing signal for no data input period. L = No data input period, H = Data input period This is equivalent to display timing (Active:H).
Vertical Synchronous Signal	$\overline{V_{SYNC}}$	1 Line	Signal controlling the refresh speed of the screen. Address returns to first electrode at the falling edge of this signal.
Horizontal Synchronous Signal	$\overline{H_{SYNC}}$	1 Line	Signal controlling the scanning timing of the line electrode at the falling edge of this signal. Input continuously at constant intervals.
Display Control Signal	ENA	1 Line	H = Light On, L = Light Off
Brightness Control Signal	B.C.	1 Line	Signal controlling display brightness by the pulse duty cycle synchronous with $\overline{H_{SYNC}}$ signal. (8 levels of brightness can be selected. 1 cycle is the period of 8 $\overline{H_{SYNC}}$ pulses.)

Relationship Between Display Data and Brightness Level (Gray Scale)

Interface Signal					Relative Brightness Level (Relative Level)
ENA	D3	D2	D1	D0	
L	X	X	X	X	Black (0)
H	L	L	L	L	Brightness Level 0
H	L	L	L	H	Brightness Level 1
H	L	L	H	L	Brightness Level 2
H	L	L	H	H	Brightness Level 3
H	L	H	L	L	Brightness Level 4
H	L	H	L	H	Brightness Level 5
H	L	H	H	L	Brightness Level 6
H	L	H	H	H	Brightness Level 7
H	H	L	L	L	Brightness Level 8
H	H	L	L	H	Brightness Level 9
H	H	L	H	L	Brightness Level 10
H	H	L	H	H	Brightness Level 11
H	H	H	L	L	Brightness Level 12
H	H	H	L	H	Brightness Level 13
H	H	H	H	L	Brightness Level 14
H	H	H	H	H	Brightness Level 15

x: invalid

Interface Signal Timing Table

Symbol	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}	14.144	14.268	14.368	ms	350/400 lines display (70 Hz)
T_{VSYNC}	16.538	16.683	16.8	ms	480 lines display (60 Hz)
t_{WV}	1	—	—	H	H: cycle of horizontal sync. signal
t_{VH}	0	—	—	µs	
t_{HV}	1	—	—	µs	
T_{HSYNC}	31.5	31.778	32.0	µs	(31.5 kHz)
t_{WH}	1	—	—	µs	
t_{HC}	1	—	—	µs	
t_{CH}	0	—	—	µs	
T_{CLK}	34	—	—	ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{WCLK1}	15	—	—	ns	
t_{WCLK2}	15	—	—	ns	
t_{SUD}	15	—	—	ns	
t_{HD}	10	—	—	ns	
t_{SUB}	5	—	—	ns	
t_{HB}	15	—	—	ns	
t_{CD}	20	—	—	µs	

Relationship Between Waveform Conditions and Vertical Effective Display

Symbol	Condition	Effective Display	Number of Display Lines	Remarks[3,4,5]
T_{VDA}	N = 525[1]	$H_{35} – H_{514}$	480	T_{VDA}: Vertical data period Hn: Horizontal period N: Number of horizontal periods in a single vertical period
T_{VDA}	N = 449[2]	$H_{35} – H_{434}$	400 or 350	

Notes: [1] The display enters 480-line mode when N = 525 and displays horizontal period (H_{35}) data on the first line and H_{514} data on line 480.

[2] The display determines 400-line mode or 350-line mode when N = 449. The two modes are not distinguished.When the top display is set, H_{35} data is displayed on line 2 and H_{434} data on line 401. When the center display is set, H_{35} data is displayed on line 33 and H_{434} data on line 432.

[3] An effective clock signal is required for the vertical data period (T_{VDA}) and also for the single horizontal period immediately before. Other periods do not need effective clock signals.

[4] Do not enter data except during the above vertical data period (T_{VDA}). Data entry will be ignored if no effective clock signals are input.

[5] In V-mode, the unit can be used only under the conditions in Note 1 and Note 2.

Relationship Between Waveform Conditions and Vertical Effective Display Period

Symbol	Standard Value	Unit	Condition	Remarks[1, 2, 3, 4]
T_{ACK}	656	CK	K = 656 (number of effective clock signals)	The effective period of horizontal data is from 9 (I = 9) for 9 clock signals to 648 (J = 648) for 640 clock signals. CK: clock.
T_{BFD}	8	CK	Horizontal data is assumed to be 640 dots at J = 656	
T_{ACD}	640	CK		
T_{AFD}	8	CK		
T_{ACK}	328	CK	K = 328 (number of effective clock signals)	The effective period of horizontal data is from 5 (I = 5) for 5 clock signals to 324 (J = 324) for 320 clock signals. CK: clock.
T_{BFD}	4	CK	Horizontal data is assumed to be 320 dots at K = 328	
T_{ACD}	320	CK		
T_{AFD}	4	CK		

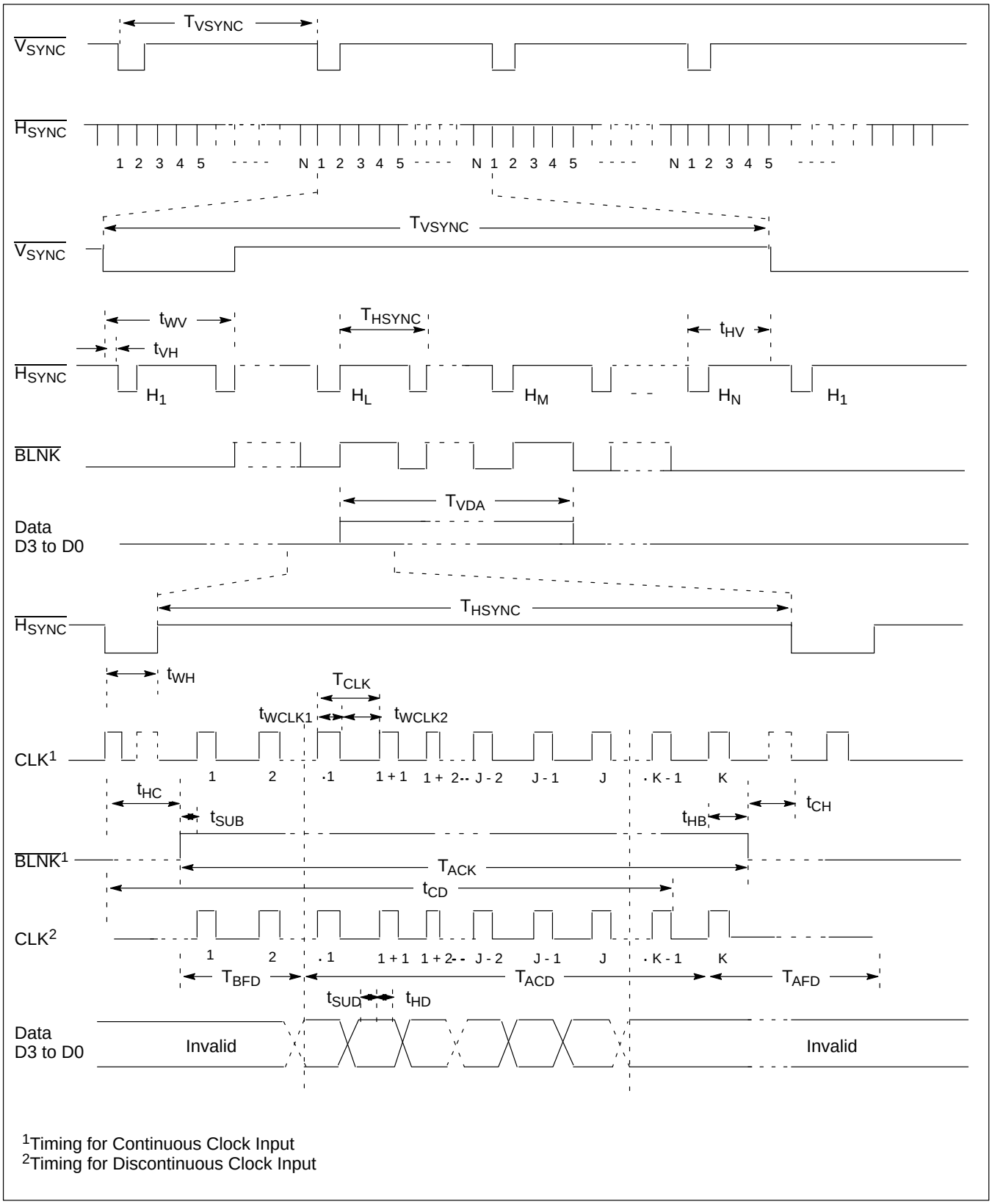
Notes: [1] A clock signal is effective when the blanking signal level is high.

[2] The plasma display determines the number of horizontal display dots by counting the number of effective clock signals during the horizontal cycle.

[3] For the 320-pixel display, each display data dot is doubled. The number of horizontal dots on the plasma screen thus becomes 640.

[4] The number of effective clock signals during the horizontal period should be 656 or 328.

Interface Signal Timing Chart



[1]Timing for Continuous Clock Input
[2]Timing for Discontinuous Clock Input

Brightness Control Timing

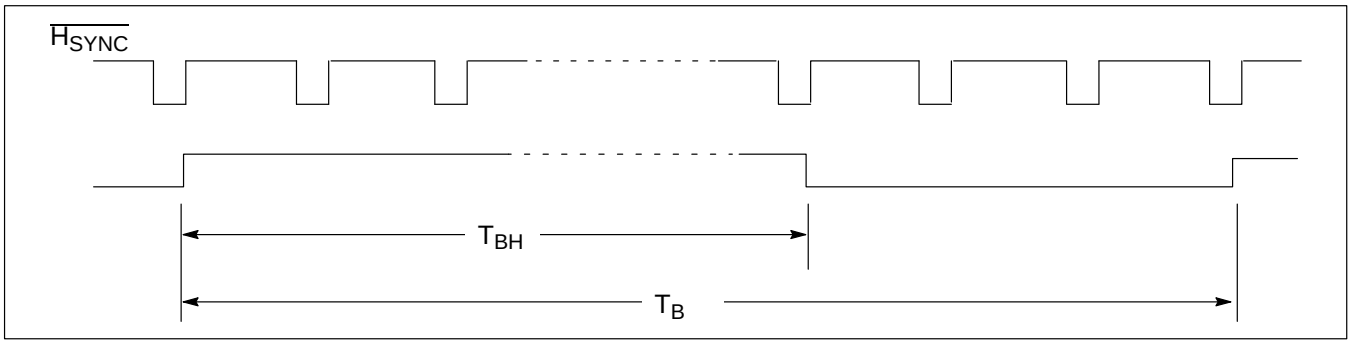
The brightness is controlled by the pulse form of the brightness control signal. Brightness varies depending on its duty cycle.

Symbol	Min.	Typ.	Max.	Unit	
T_B	8	8	8	H	H: A Cycle of $\overline{H_{SYNC}}$ Signal
T_{BH}	0	—	8	H	

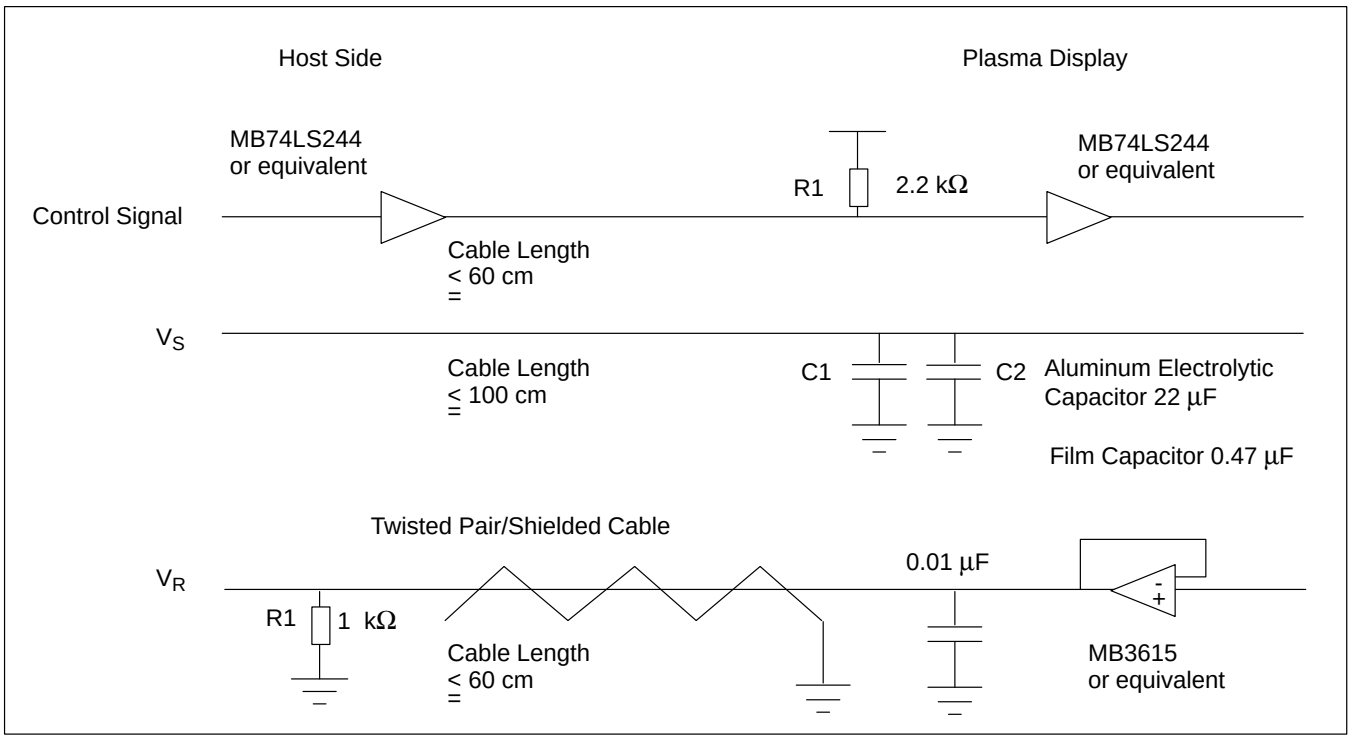
* Brightness is at its maximum at 8xH and 7xH.

Brightness Control Signal Timing Diagram

The brightness control signal is synchronized with the rising edge of the $\overline{H_{sync}}$ signal.



Interface Circuit



CONNECTOR PIN ASSIGNMENT

Signal Connector (FCN-605Q020-AU/N)

No.	Signal	No.	Signal
1	$\overline{V_{SYNC}}$	2	S. GND
3	$\overline{H_{SYNC}}$	4	S. GND
5	DATA D0	6	S. GND
7	DATA D1	8	S. GND
9	DATA D2	10	S. GND
11	DATA D3	12	S. GND
13	$\overline{BLNK}$	14	S. GND
15	CLK	16	S. GND
17	+5VDC	18	+5 VDC
19	B.C.	20	ENA

Note: Mating Connector (optional): FCN-607B020-G/D.

Power Supply Connector (FCN-815-009TA)

No.	Power Input
1	V_{CC}
2	GND
3	N.C.
4	GND
5	V_S
6	N.C.
7	N.C.
8	GND
9	V_R*

Notes: Mating Connector (optional):
FCN-813J009-A, Housing
FCN-813J-T/Q, Contact (for hand tool)
FCN-813J-T/R, Contact (for auto)

*This PDP unit outputs the voltage V_R from 0 to 2.5 VDC through the ninth terminal of the power supply connector. This supply voltage is used for the supply voltage adjustment FPF07P series power supply units.

Section 6

Graphic Units (large size) — *At a Glance*

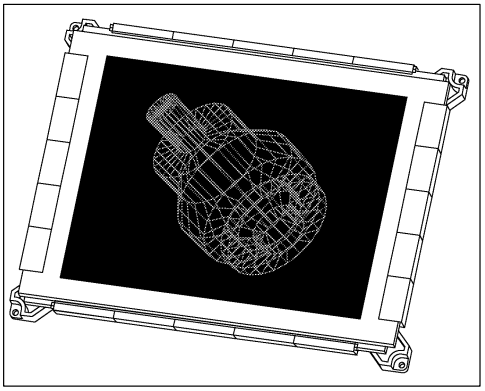
August 1990
Edition 1.0

FUJITSU

DATA SHEET

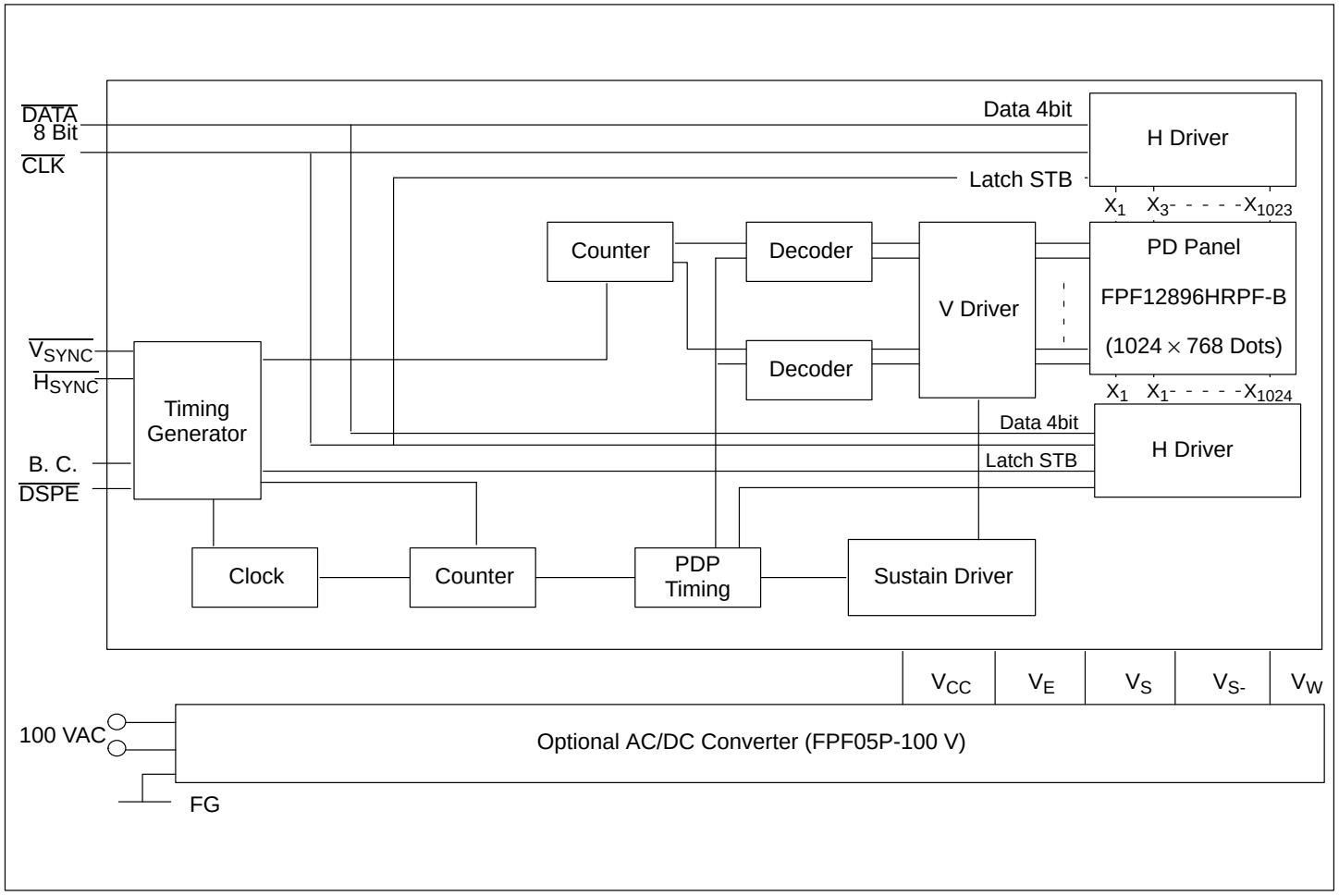
FPF12896HRUF–B
Plasma Display Graphics Unit

The FPF12896HRUF-B plasma display graphics unit consists of an AC gas discharge plasma display panel with bistable memory and associated driver circuitry. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF12896HRUF-B a highly reliable display device.



- Bright, even, orange-on-black display
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Maximum Ratings
Voltage for Sustain Driver	V_S	+120 V
Voltage for Sustain Driver	V_{S-}	–120 V
Voltage for Writing Driver	V_W	+195 V
Voltage for Addressing	V_E	+45 V
Voltage for Logic	V_{CC}	+7 V

Operation Ratings

Item	Symbol	Voltage	Variable Range	Stability	Ripple	Current (Max.)
Voltage for Sustain Driver	V_S	+96 V	± 9 V	± 2% max.	600 mV_{PP} max.	400 mA
Voltage for Sustain Driver	V_{S-}	–96 V	± 9 V	± 2% max.	600 mV_{PP} max.	400 mA
Voltage for Writing Driver	V_W	+160 V	± 5 V	± 3% max.	100 mV_{PP} max.	50 mA
Voltage for Addressing	V_E	+37 V	—	± 10% max.	100 mV_{PP} max.	250 mA
Voltage for Logic	V_{CC}	+5 V	—	± 5% max.	100 mV_{PP} max.	1.0 A

Note: Variable power sources are required for V_S, V_{S-}, and V_W because they have specified voltages. Each specified voltage is indicated on each plasma display unit.

MECHANICAL SPECIFICATIONS

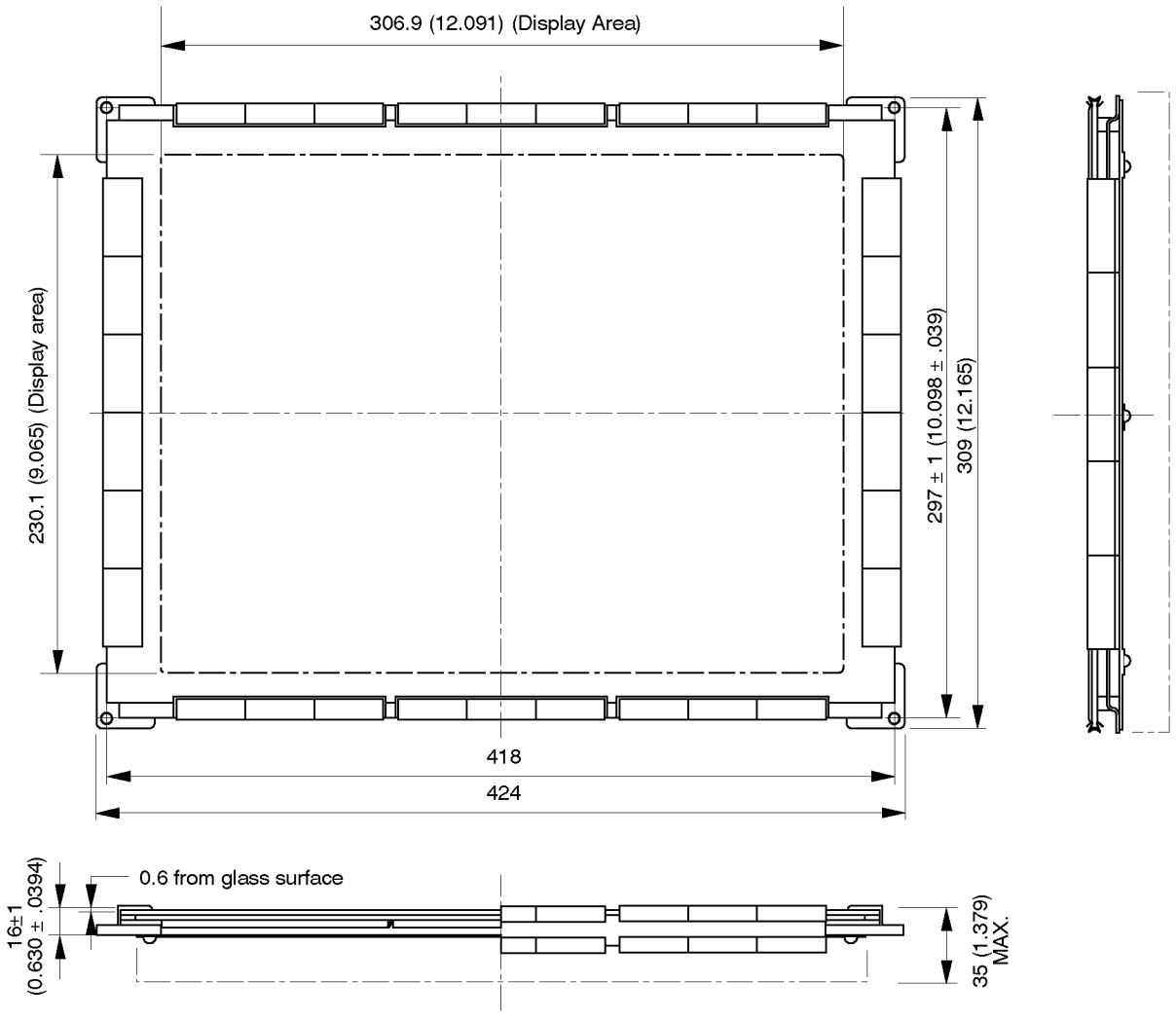
Physical Specifications

Item	Value
Number of Display Dots	1024 (H) × 768 (V) (786,432 dots)
Dot Pitch	0.3 mm (H) × 0.3 mm (V) (0.012 in. × 0.012 in.)
Dot Size	0.2 mm (0.08 in.) dia.
Effective Screen Area	307 mm (H) × 230 mm (V) (12.087 × 9.055 in.)
Display Color	Neon Orange
Dot Brightness	15 cd/m^2 (5.9 fL) min. (plane average)
Brightness Uneveness	50% max. (at max. brightness)
Contrast Ratio	1:10 min. (at max. brightness)
Viewing Angle	160° min.
External Dimensions	309 (W) × 402 (H) × 35 (D) mm (12.165 × 15.827 × 1.378 in.)
Weight	3.5 kg (7.7 lb)

Performance Specifications

Item	Value
Operating Temperature	5 to 40°C
Operating Humidity	20 to 80% RH (no condensation)
Storage Temperature	–10 to 55°C
Storage Humidity	20 to 80% RH (no condensation)
Atmospheric Pressure	70,000 to 111,400 Pa
Vibration Acceleration: Frequency: Time:	 2 G (max.) 10 to 55 Hz Operation: 5 min. in X, Y, and Z direction. Non-Operation: 2 hr. in X, Y, and Z direction.
Shock (Non-Operation) Acceleration: Time:	 40 G (max.) in X and Y direction. 10 G (max.) in Z direction 11 ms

External Dimensions



Unit: mm (in.)

INTERFACE SIGNALS

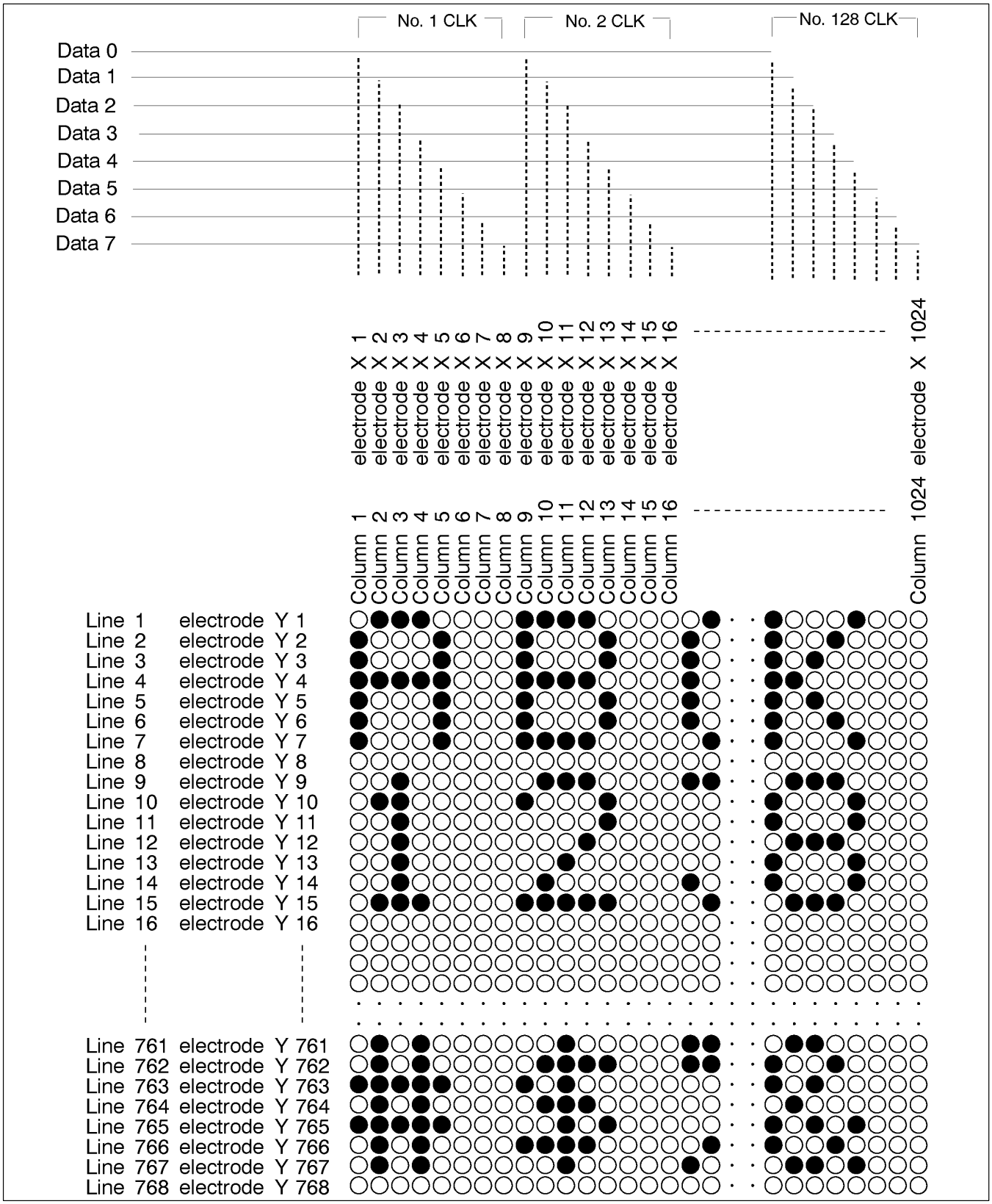
Type of Signals (TTL)

Signal	Symbol	Data Line	Description
Data Signal	$\overline{DATA0\ to\ 7}$	8	8-bit parallel display data. Logic: L: light on, H: light off Relationship between display data and display dots is shown in the figure on the following page.
Clock Signal	$\overline{CLK}$	1	Signal controlling the input of timing of display data. Display data are input at falling edge of this signal. Number of signals during one $\overline{H_{SYNC.}}$ cycle is 128.
Line Synchronous Signal	$\overline{H_{SYNC}}$	1	Signal controlling the scanning timing of the line-electrode. Y address increment to select the next line electrode is done at the falling edge of each signal. The number of signals during the period of one $\overline{V_{SYNC}}$ must be 769 or more.
Frame Synchronous Signal	$\overline{V_{SYNC}}$	1	Signal controlling the refresh speed of the screen. The scanning position returns to the first electrode (home position) at the falling edge of the signal.
Brightness Control Signal	B. C.	1	Signal controlling the screen brightness. Logic: L: 67% maximum brightness H: maximum brightness.
Display Enable Signal	$\overline{DSPE}$	1	Signal controlling the display enable. Logic: L: Light on. H: Light off whole screen display.

Recommended Driving Condition

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Input Voltage (H-Level)	—	V_{IH}	2.4	—	—	V
Input Voltage (L-Level)	—	V_{IL}	—	—	0.4	V
Input Current (H-Level)	V_{IH} = 2.75 V, V_{CC} = 5.25 V	I_{IH}	—	—	10	mA
Input Current (L-Level)	V_{IL} = 0.4 V, V_{CC} = 5.25 V	I_{IL}	—	—	-16	mA

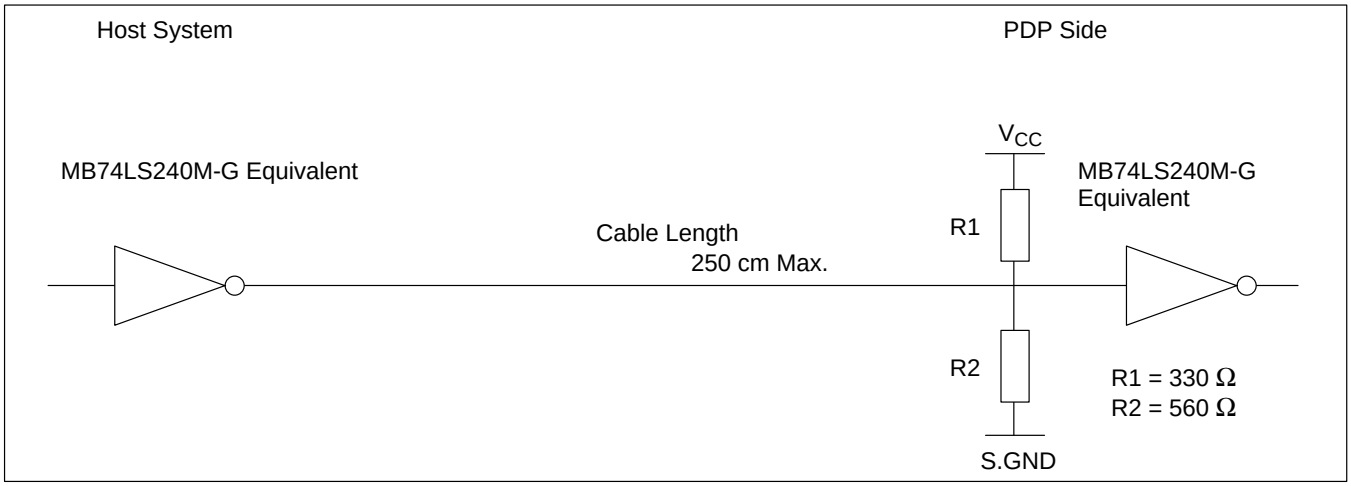
Relationship Between Display Data and Display Dot



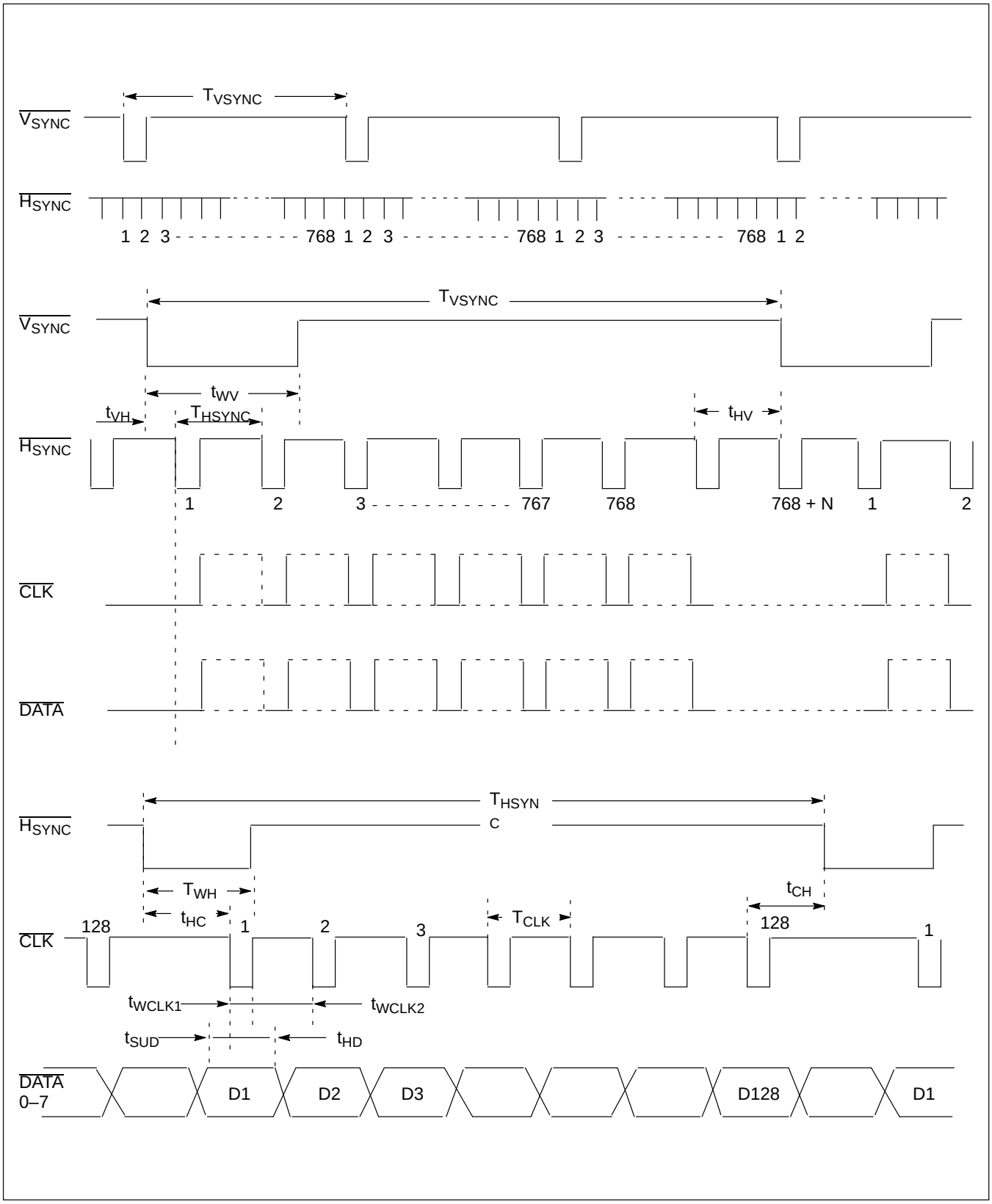
Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}	61.44	65		ms	F_{VSYNC} = 15 Hz (Typ.)
t_{WV}	2	160		µs	
t_{VH}	1	77		µs	
t_{HV}	2	5		µs	
T_{HSYNC}	80	82	90	µs	
t_{WH}	2	5		µs	
t_{HC}	5	10		µs	
t_{CH}	1	8		µs	
t_{CLK}	300	500		ns	F_{CLK} = 2 MHz (Typ.)
t_{WCLK1}	150	250		ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{WCLK2}	150	250		ns	Duty Cycle = 50% (Typ.)
t_{SUD}	100	180		ns	
t_{HD}	80	135		ns	

Interface Circuit



Interface Signal Timing Chart

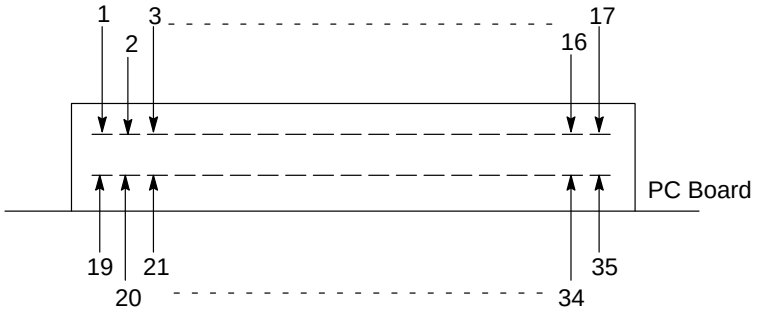


CONNECTOR PIN ASSIGNMENT

Signal Connector

P/N:HIF6-34PA-1.27DS (by Hirose) Applicable Connector: HIF6-34B-1.27R (by Hirose)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	$\overline{\text{DATA 0}}$	2	S. GND	19	H_{SYNC}	20	S. GND
3	$\overline{\text{DATA 0}}$	4	S. GND	21	V_{SYNC}	22	S. GND
5	$\overline{\text{DATA 0}}$	6	S. GND	23	DSPE	24	S. GND
7	$\overline{\text{DATA 0}}$	8	S. GND	25	B. C.	26	S. GND
9	$\overline{\text{DATA 0}}$	10	S. GND	27	N.C.	28	S. GND
11	$\overline{\text{DATA 0}}$	12	S. GND	29	N.C.	30	S. GND
13	$\overline{\text{DATA 0}}$	14	S. GND	31	V_{CC} (OUT)	32	S. GND
15	$\overline{\text{DATA 0}}$	16	S. GND	33	V_{CC} (OUT)	34	S. GND
17	$\overline{\text{CLK}}$			35	V_{CC} (OUT)		



Notes:
1. This figure shows the connector viewed from the mating surface.
2. Though the mounted connector has 34 terminals, the pins are numbered as a 36-terminal connector. (No. 18 and 36 are not specified.) Numbering on the PC board is the same as in this figure.
3. V_{CC} terminals output +5 VDC.

Power Supply Connector

P/N: 65595-113#10 (by Berg)

Pin No.	Symbol	Voltage
1	V_W	165 V
2	N.C.	—
3	V_S	95 V
4	—*	—
5	GND (H)	0 V
6	GND (H)	0 V
7	N.C.	—
8	V_{S-}	-95 V
9	N.C.	—
10	S. GND	0 V
11	S. GND	0 V
12	V_E	37 V
13	V_{CC}	5 V

Notes: Applicable Connector:
Housing: 65486-13 (by Berg)
Contact: 76804-36 (by Berg)

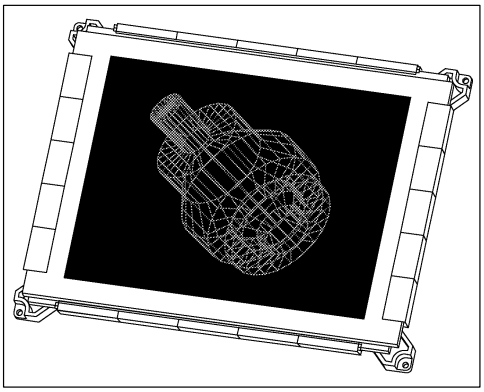
*Polarization key inserted

May 1993
Edition 1.0

DATA SHEET

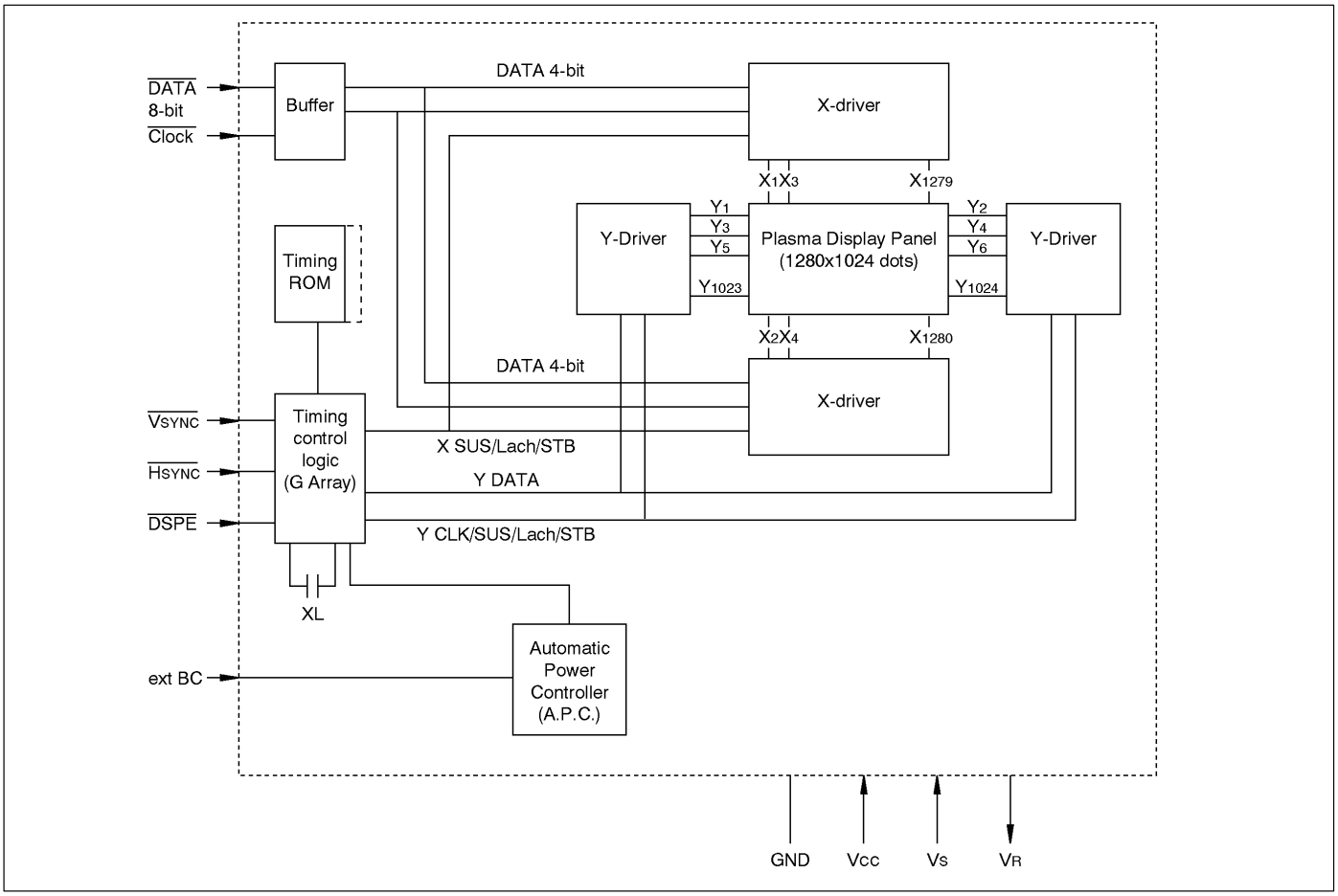
FPF160128SRUA-001
Plasma Display Graphics Unit

The FPF160128SRUA–001 plasma display graphics unit consists of an AC gas discharge plasma display panel with bi-stable memory and associated driver circuitry.The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF160128SRUA–001 a highly reliable display device.



- Bright, even, orange-on-black display
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



SPECIFICATIONS

Display Performance

Item	Performance
Number of display dots	1,310,720 dots (1280 X 1024 dots)
Dot pitch	0.25 mm (0.01 in) aspect ratio: 1:1
Dot size	0.15 mm diameter (0.006 in)
Display area	319.75 (H) X 255.75 (V) mm diagonal: 16 in (12.589 X 10.069 in)
Display color	Neon orange
Brightness	18 cd/m_2 typical, 12 cd/m_2 minimum Plane average of solid pattern in 8x8 dots area Dispay ratio: up to 25% H_{SYNC} = 31.25 μs Is = 300 mA
Brightness unevenness	40% maximum (20% maximum in each 10 mm distant area)
Contrast ratio	1 : 20 minimum
Maximum viewing angle	140° typical
Defective dots	Total 30 dots maximum 2 adjacent dots: 6 portion maximum 3 adjacent dots: 0 portion 3 dots maximum in any 32 x 32 dots area (including flickering dots)

Environmental Conditions

Item	Rating
Operating temperature	0 to +50° C
Operating humidity	20 to 80% RH (no condensation)
Storage temperature	–20 to +70°C
Storage humidity	20 to 80% RH (no condensation)
Atmospheric pressure	700 to 1114 hPa

MECHANICAL SPECIFICATIONS

Physical Specifications

Item	Specification
Dimension (H) X (W) X (D)	See External Dimensions figure 309 X 402 X 30 mm (12.165 x 15.827 x 1.81 in)
Weight	3.0 kg (max)
Vibration	Acceleration: 2G maximum Frequency: 10 to 55 Hz Time: Operation: 5 minutes in each direction of X, Y, Z No operation: 2 hours in each direction of X,Y,Z
Shock (no operation)	Acceleration: 40G maximum in each direction X, Y 20G maximum in the direction of Z Time: 11 ms

Electrical Characteristics

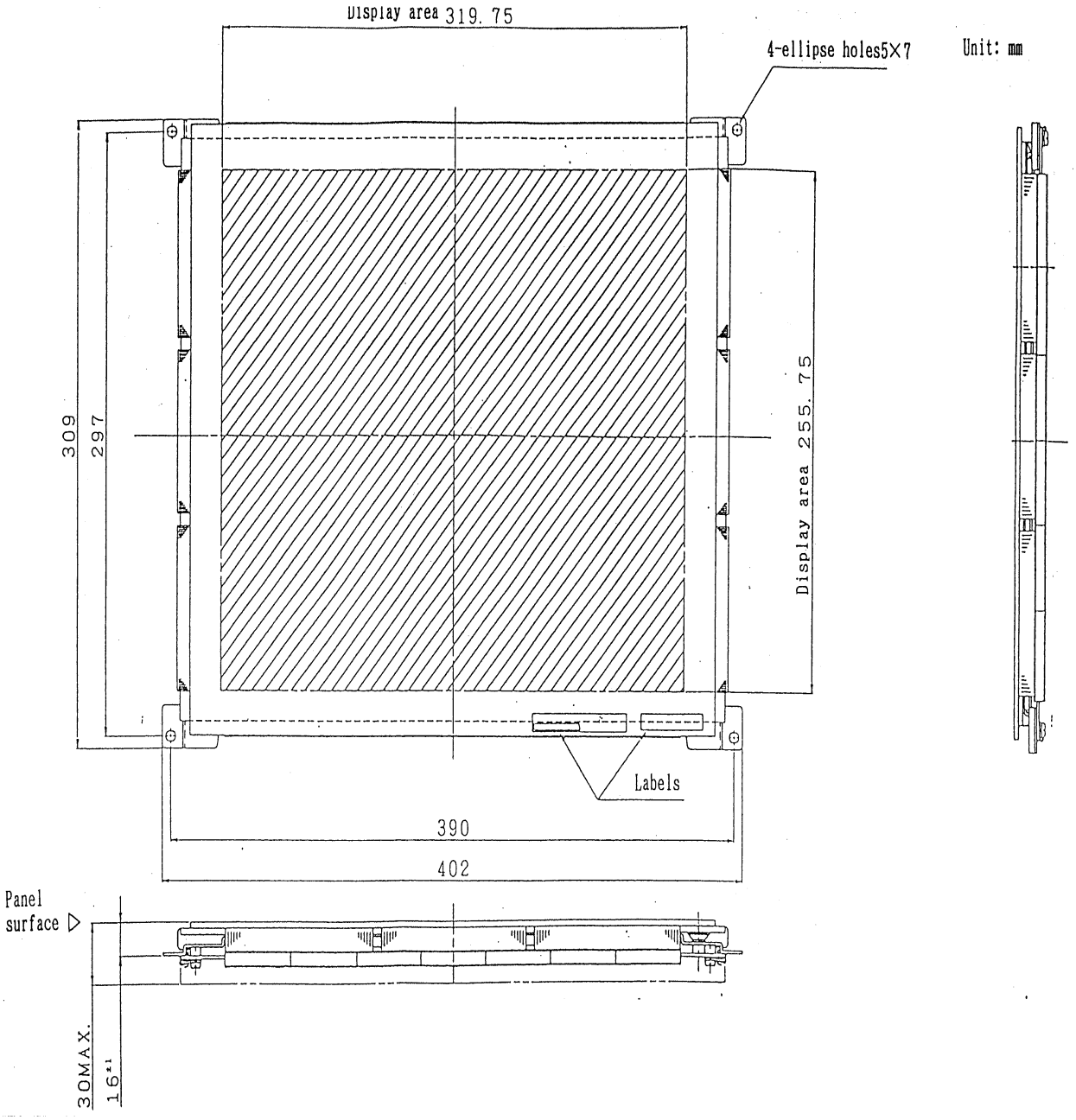
Item	Symbol	Voltage	Stability (Max)	Ripple (Max)	Current (Max)
Logic	V_{CC}	+5V	± 5%	100 mV_{PP}	0.3A
Sustain driver	V_S	+88 to 100.5V	± 0.5%	500 mV_{PP}	Set value ± 30mA
V_S reference	V_R	Set value	± 0.05V	500 mV_{PP}	10mA

Notes: Current for sustain driver ($V_{S)}$ is specified by set value of Automatic Power Controller (APC). Typical set value is 300 mA.
For the V_S voltage setting, the plasma display unsit outputs the reference voltage $V_{S.}$

Absolute Maximum Ratings

Item	Symbol	Rating
Supply voltage for logic	V_{CC}	+ 7V
Supply voltage for sustain	V_S	+120 V

External Dimensions



INTERFACE SIGNALS

Type of Signals

Signal	Symbol	Data Line	Description
Display data	$\overline{D0}$ ~ $\overline{D7}$	8	8-bit parallel display data. Logic: L: On, H: Off The figure on page 6 shows the relation between data $\overline{D0}$ ~ $\overline{D7}$ and display position.
Clock	$\overline{CLK}$	1	Signal controlling the input of timing of display data. Display data is input at falling edge of $\overline{CLK}$ and transferred in sequence. Number of signals in one $\overline{H_{SYNC}}$ period is 160.
Horizontal synchronous	$\overline{H_{SYNC}}$	1	Signal controlling the scanning timing and display time of each line electrode. Address incremeent to the next line is done at the falling edge of $\overline{H_{SYNC}}$. The number of signals in one $\overline{V_{SYNC}}$ period is required to be 1024 or more, and a continuous signal is required.
Vertical synchronous	$\overline{V_{SYNC}}$	1	Signal controlling the refresh speed of the screen.The scanning position returns to the first electrode at the falling edge of the $\overline{V_{SYNC}}$ signal.
Brightness control	B. C.	1	Signal controlling the brightness of the entire screen. Logic: L: Low brightness H: High brightness.
Display enable	$\overline{DSPE}$	1	Signal controlling the display enable. Logic: L: On. H: Off

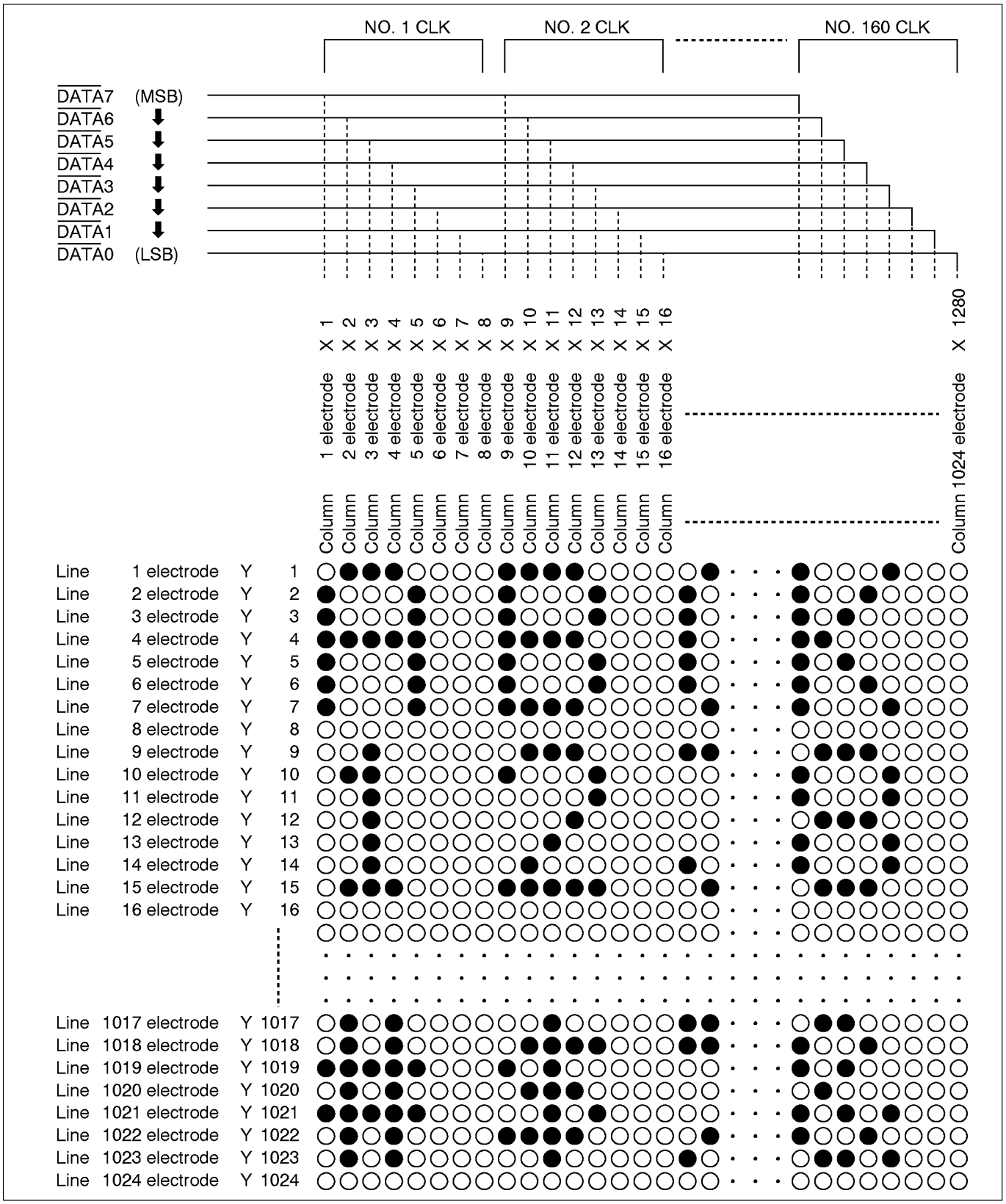
Note: Brightness control signal can be input with pulse form signal. Brightness is variable depending on the duty of pulse signal. The following table shows input conditions:

Item	Symbol	Min	Typ	Max	Unit
Period	T_B	140	167	195	μs
High brightness setting time	T_{BH}	0		T_B	μs

Recommended Electrical Conditions

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Input voltage (H-Level)	—	V_{IH}	2.4	—	—	V
Input voltage (L-Level)	—	V_{IL}	—	—	0.4	V
Input current (H-Level)	V_{IH} = 2.75 V, V_{CC} = 5.25 V	I_{IH}	—	—	20	μA
Input current (L-Level)	V_{IH}= 0.4 V, V_{CC} = 5.25 V	V_{IL}	—	—	-3.0	mA

Relationship Between Display Data and Display Dot

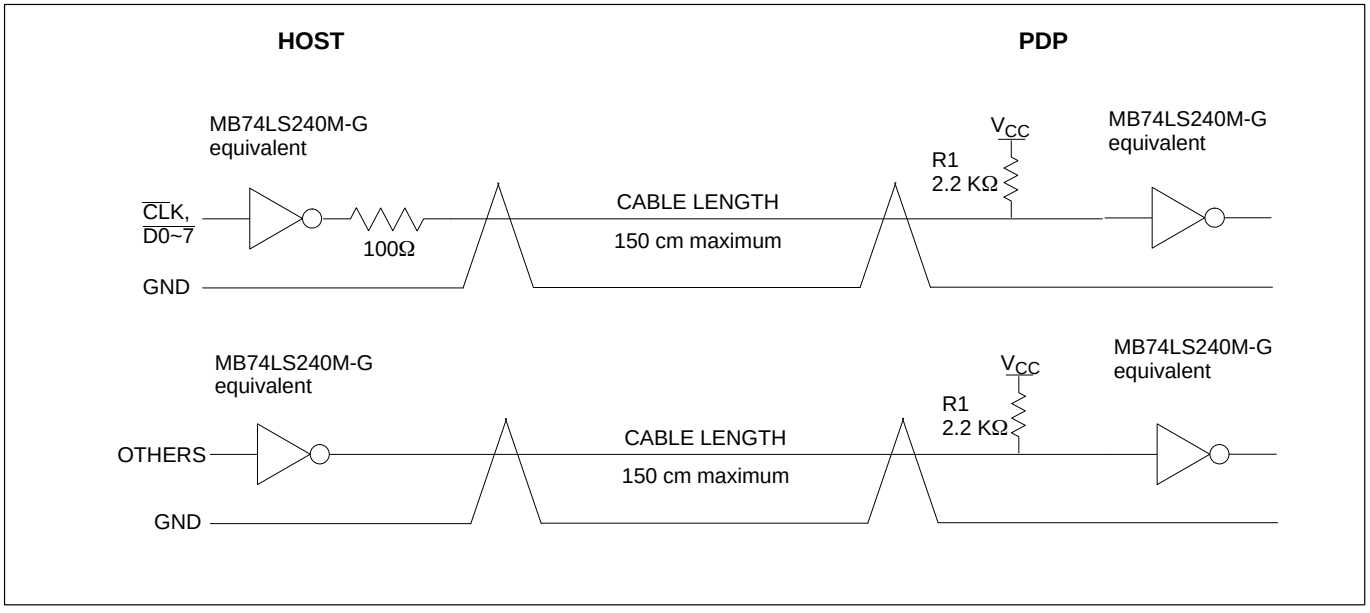


Interface Signal Timing

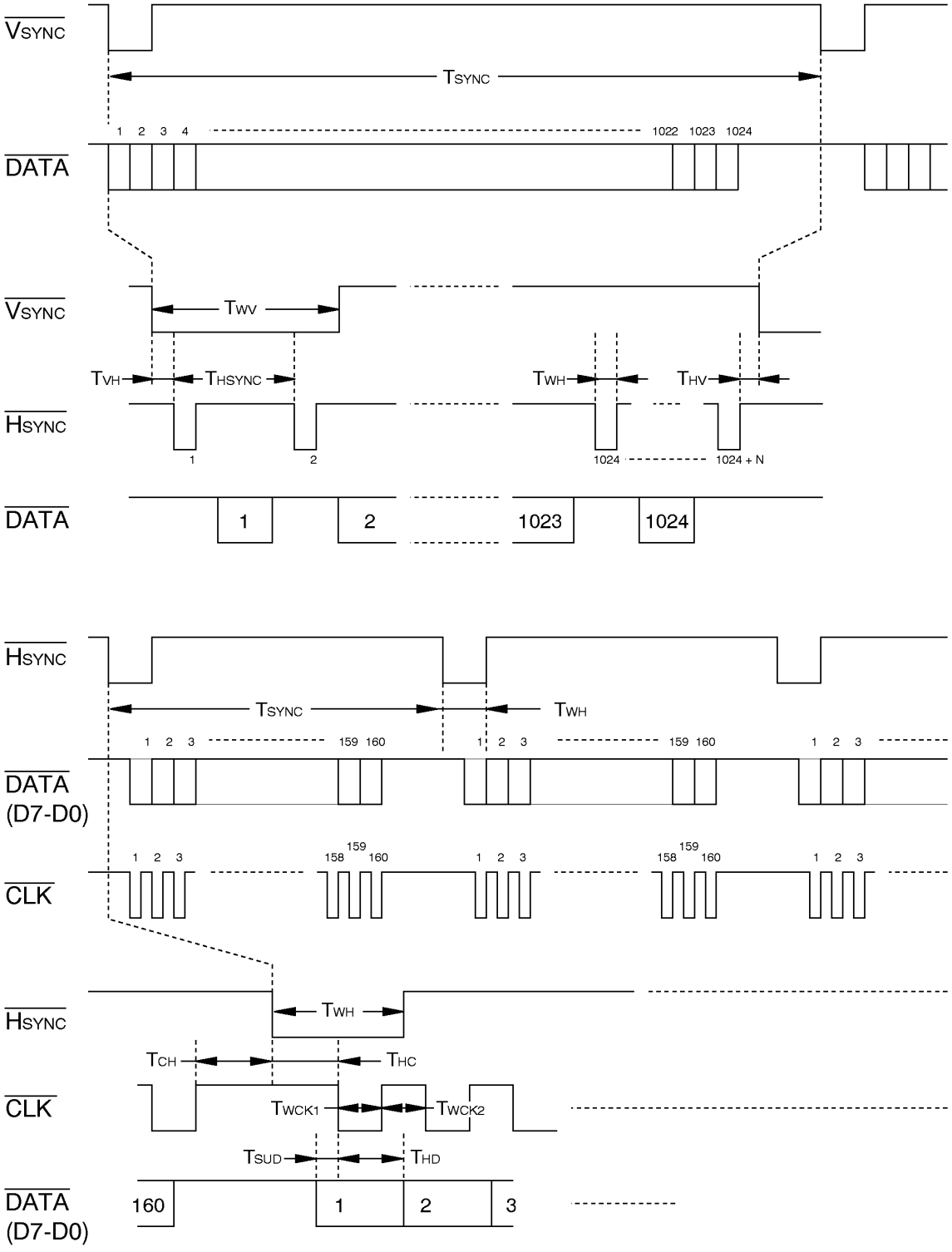
Symbol	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}	1024	1067		H	F_{VSYNC} = 30 Hz typical
t_{WV}	1	3		H	
t_{VH}	1	14		µs	
t_{HV}	2	15.25		µs	
T_{HSYNC}	30.0	31.25	45.0	µs	F_{VSYNC} = 32 Hz typical
t_{WH}	1	2		µs	
t_{HC}	0.5	2		µs	
t_{CH}	0.1	2.7		µs	
t_{CLK}	166.7			ns	F_{CLK} = 6 MHz maximum
t_{WCLK1}	Typ – 10%	1/2 t_{CLK}	Typ +10%	ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{WCLK2}	Typ – 10%	1/2 t_{CLK}	Typ +10%	ns	Duty = 50% typical
t_{SUD}	40			ns	
t_{HD}	70			ns	

Note: Values in parenthesis () are one example of timing condition.

Interface Circuit



Interface Signal Timing Chart

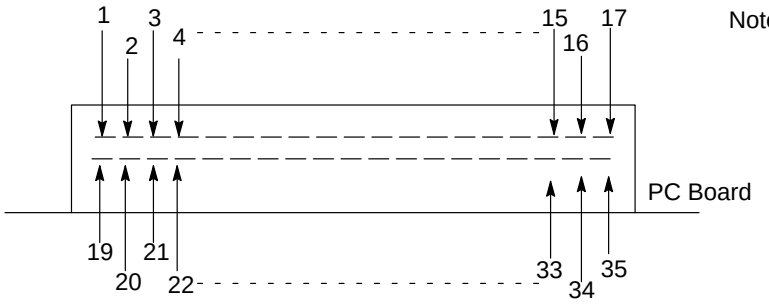


CONNECTOR PIN ASSIGNMENT

Signal Connector

P/N:HIF6-34PA-1.27DS (by Hirose) Mating Connector: HIF6-34B-1.27R (by Hirose)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	$\overline{\text{DATA 7}}$	2	S. GND	19	H_{SYNC}	20	S. GND
3	$\overline{\text{DATA 6}}$	4	S. GND	21	V_{SYNC}	22	S. GND
5	$\overline{\text{DATA 5}}$	6	S. GND	23	DSPE	24	S. GND
7	$\overline{\text{DATA 4}}$	8	S. GND	25	Ext B. C	26	S. GND
9	$\overline{\text{DATA 3}}$	10	S. GND	27	Reserve	28	S. GND
11	$\overline{\text{DATA 2}}$	12	S. GND	29	No Connection	30	S. GND
13	$\overline{\text{DATA 1}}$	14	S. GND	31	V_{CC} (OUT)	32	S. GND
15	$\overline{\text{DATA 0}}$	16	S. GND	33	V_{CC} (OUT)	34	S. GND
17	$\overline{\text{CLK}}$			35	V_{CC} (OUT)		



Notes:
- This drawing shows the signal connector as viewed from the mating side.
- The actual connector has 34 pins, numbered to the 36th pin in this specification.The 18th and 36th pins are the missing numbers. Numbers corresponding to the 36 pins are silk-screened onto the PC board.
- The trianagle mark on the connector does not correspond to the 1st pin. The 31st, 33rd, and 35th pins' output is +5V of DC voltage. The 27th pin is to be connected with GND.

Power Supply Connector

Pin No.	Power Source Name
1	V_{CC}
2	S.GND
3	N.C
4	GND (H)
5	V_S
6	N.C.
7	N.C.
8	S.GND
9	V_R (output)

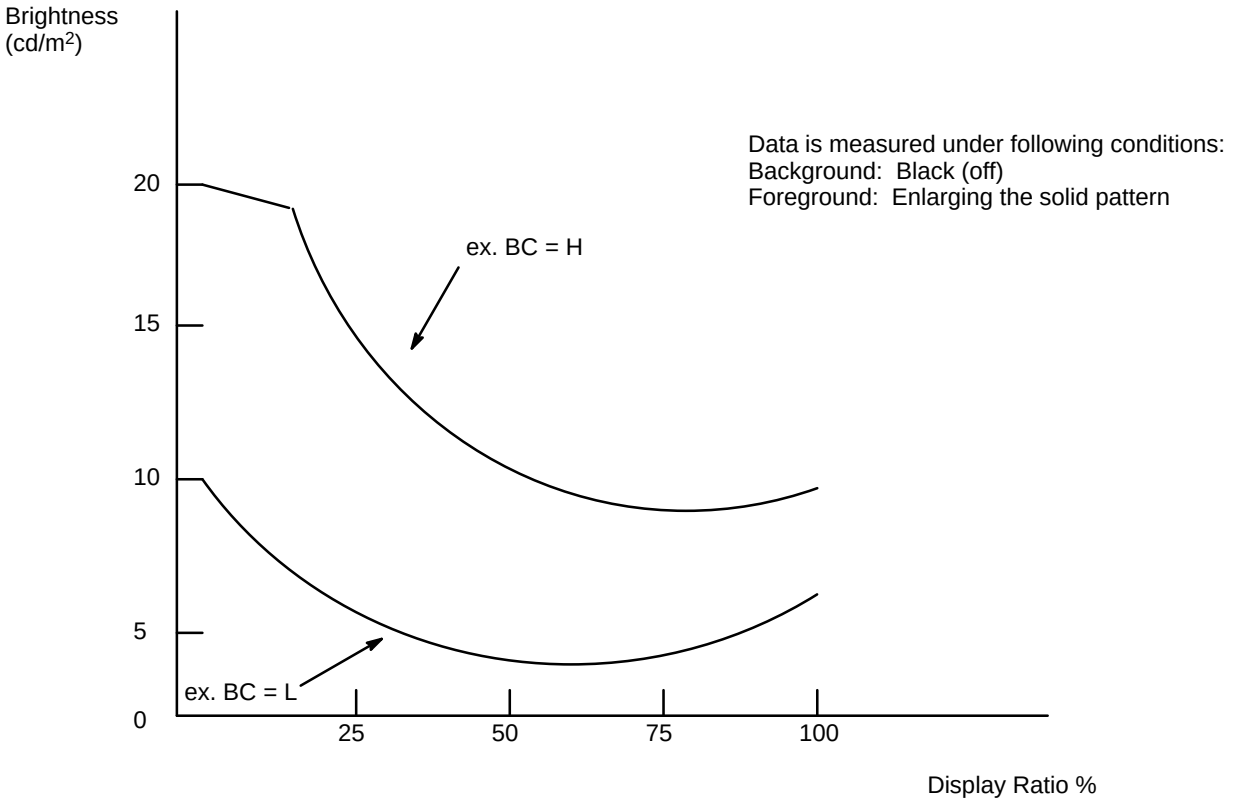
PDP side connector: FCN-815P-009TA (Fujitsu)

Mating Connector (by Fujitsu)
Housing: FCN-813J009-A
Contact: FCN-813J-T/Q (hand crimping
FCN-813J-T/R (automatic crimping machine)
FCN-813J-T/S (hand crimping
FCN-813J-T/T (automatic crimping machine)

Note: V_R is the reference voltage for automatic V_S setting

Relation Between Display Ratio and Brightness

In general, the increased display ratio will increase the current of the VS. This plasma display employs the automatic power controller circuit. Therefore, when the current value of V_S is set at 300 mA, the brightness decreases gradually after exceeding the display ratio of 25%. When the current is limited by the automatic power controller circuit, the brightness decreases.

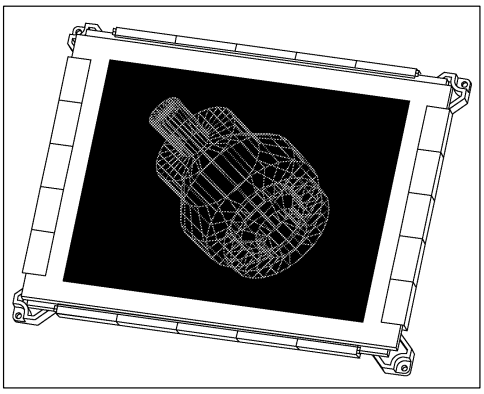


August 1990
Edition 1.0

FUJITSU

DATA SHEET

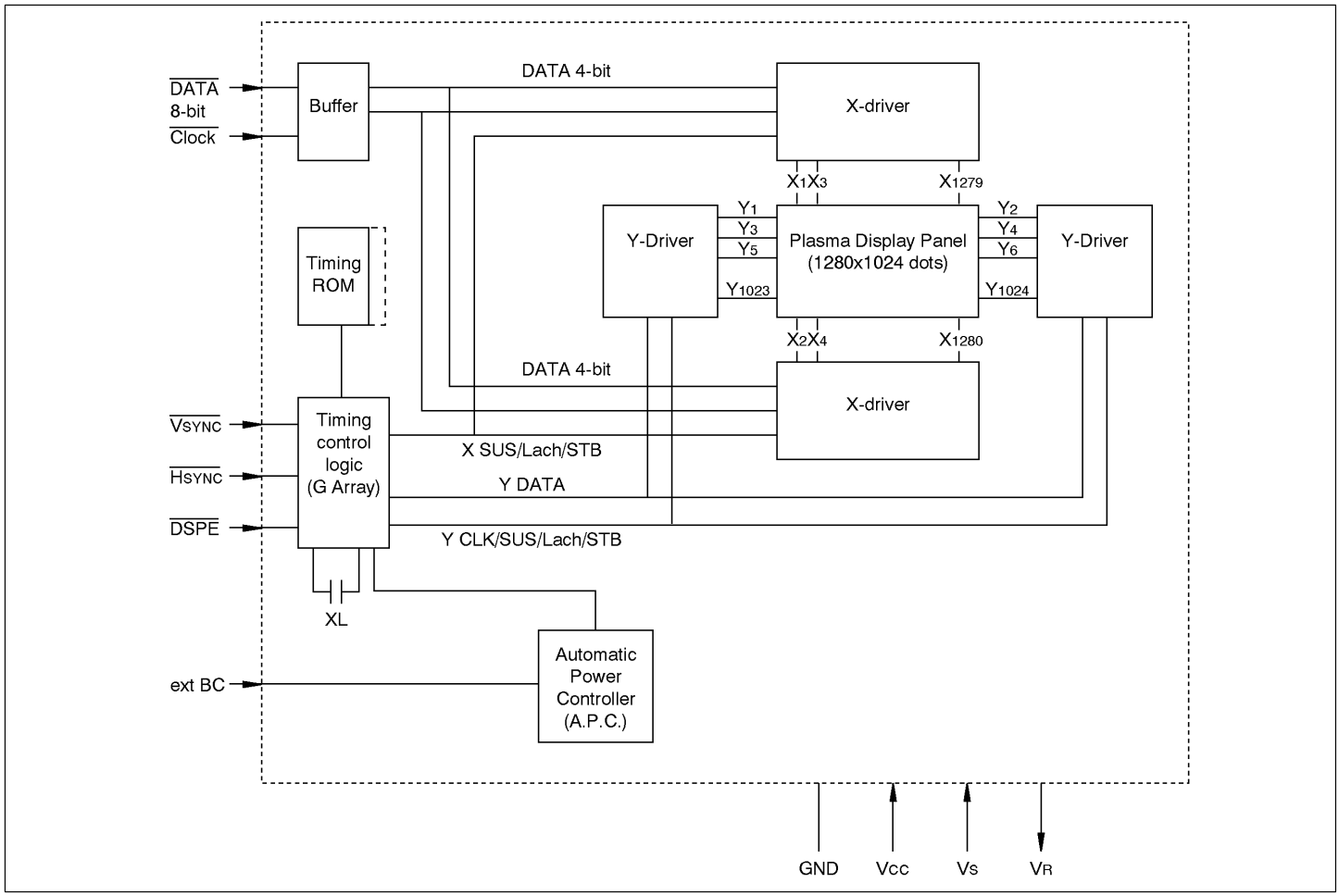
FPF160128SRUA–020
Plasma Display Graphics Unit



The FPF160128SRUA–020 plasma display graphics unit consists of an AC gas discharge plasma display panel with bistable memory and associated driver circuitry. The orange-on-black, high-contrast panel provides an easy-to-read display with no flicker or warp. The compact unit can be connected to all types of equipment with common CRT interfaces. The highly integrated drive and logic circuitry and Fujitsu's unique protective film make the FPF160128SRUA–020 a highly reliable display device.

- Bright, even, orange-on-black display
- Easy-to-use CRT interface
- Space-saving size and shape
- High reliability

BLOCK DIAGRAM



SPECIFICATIONS

Display Performance

Item	Performance
Number of Display Dots	1,310,720 dots (1280X1024 dots)
Dot Pitch	0.25 mm (0.01 in) * aspect ratio: 1:1
Dot Size	0.15 mm diameter (0.006 in)
Display Area	319.75 (H) X 255.75 (V) mm * diagonal: 16 in (12.589 X 10.069 in)
Display Color	Neon Orange
Brightness	35 cd/m_2 (Typ) 27 cd/m_2 (Min) Plane average of solid pattern in 8X8 dots area Dispay ratio: up to 25% HSYNC = 60.00 µs Is = 500 mA
Brightness Unevenness	40% max (20% max in each 10 mm distant area)
Contrast Ratio	1:20 min
Maximum Viewing Angle	140° (Typ)
Defective Dots	Total 30 dots max 2 adjacent dots: 6 portion max 3 adjacent dots: 0 portion 3 dots max in any 32 X 32 dots area (including flickering dots)

Environmental Conditions

Item	Rating
Operating temperature	0 to +40° C
Operating humidity	20 to 80% RH (no condensation)
Storage temperature	–20 to +70°C
Storage humidity	20 to 80% RH (no condensation)
Atmospheric pressure	700 to 1114 hPa

MECHANICAL SPECIFICATIONS

Physical Specifications

Item	Specification
Dimension (H) X (W) X (D)	See Fig 2 307 X 387 X 34 mm
Weight	3.3 kg (max)

Electrical Characteristics

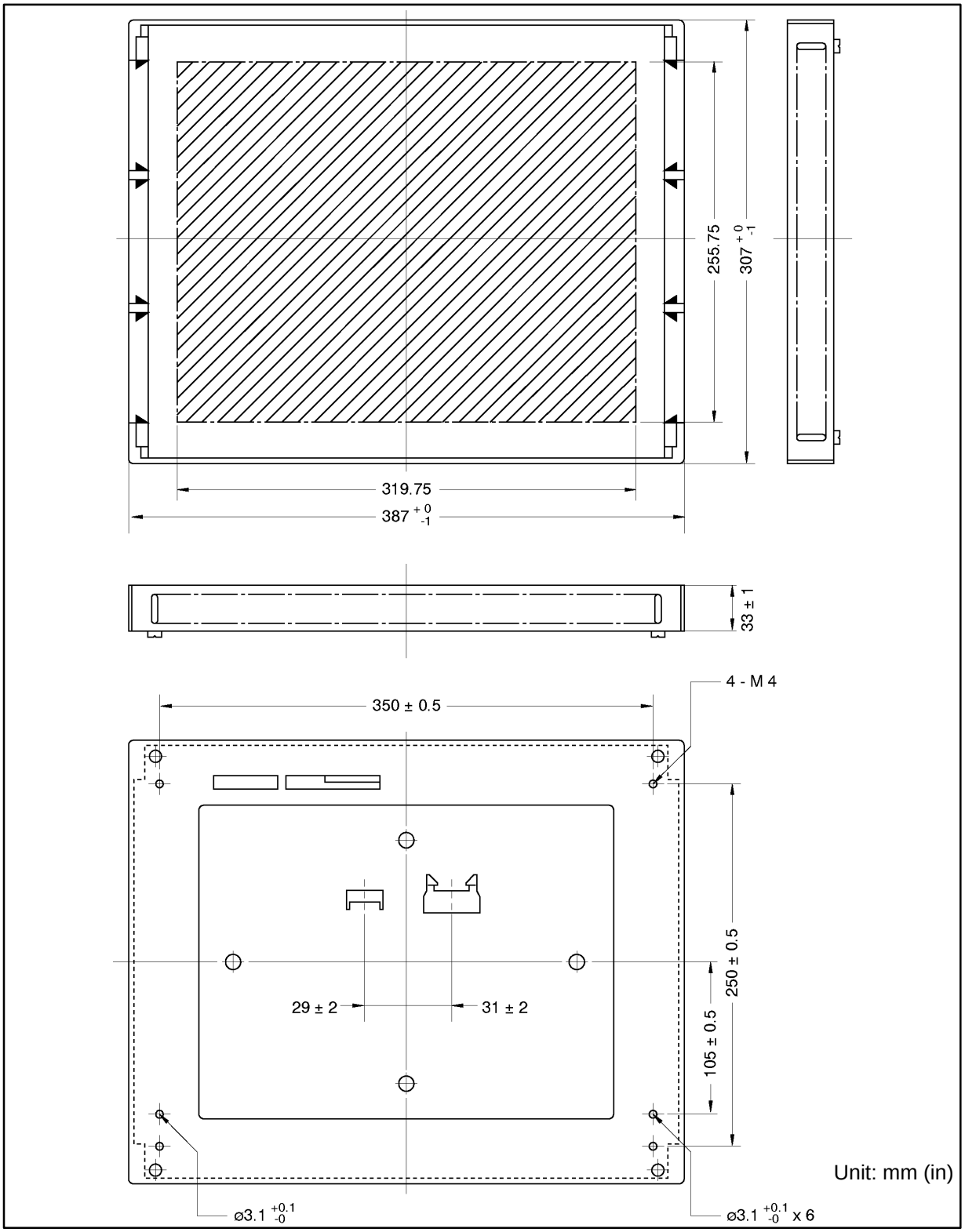
Item	Symbol	Voltage	Stability (Max)	Ripple (Max)	Current (Max)
Logic	V_{CC}	+5%	± 5%	$100mV_{PP}$	0.3A
Sustain driver	V_S	+88 to 100.5 V	± 0.5%	$500mV_{PP}$	Set value ± 30mA
V_S Reference	V_S	Set Value	± 0.05V	$500mV_{PP}$	10mA

Notes: 1) Current for sustain driver ($V_{S)}$ is specified by set value of Automatic Poer Controler (A.P.C.). Typical set value is 300 mA.
2) For the V_S voltage setting, the plasma display unsit outputs the reference voltage $V_{S.}$

Absolute Maximum Ratings

Item	Symbol	Rating
Supply voltage for logic	V_{CC}	+ 7 V
Supply voltage for sustain	V_S	+120 V

External Dimensions



INTERFACE SIGNALS

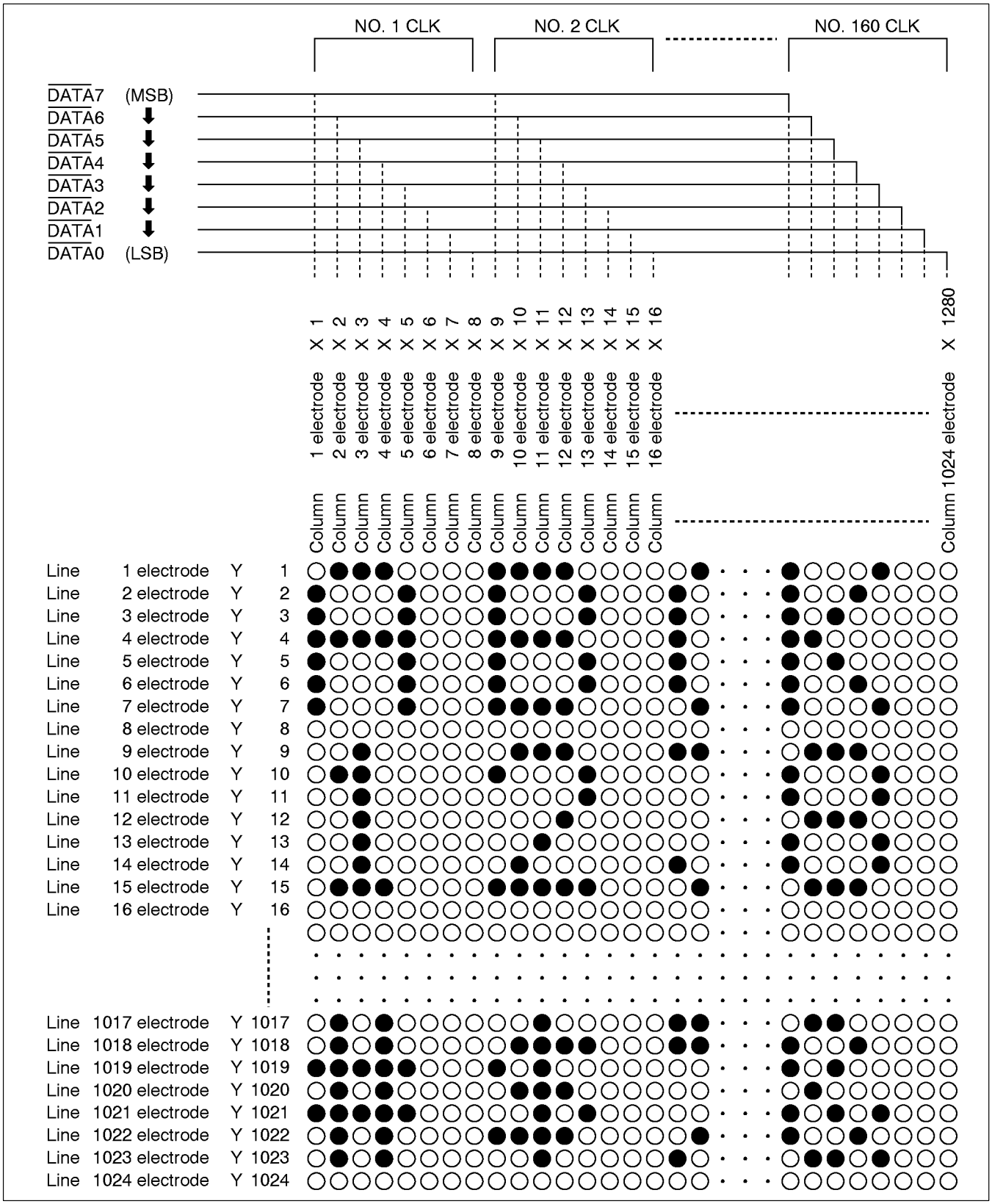
Type of Signals

Signal	Symbol	Data Line	Description
Display Data	$\overline{D0 \sim D7}$	8	8-bit parallel display data. Logic: L: On, H: Off Figure 3 shows the relation between data $\overline{D0 \sim D7}$ and display postion.
Clock	$\overline{CLK}$	1	Signal controlling the input of timing of display data. Display data are input at falling edge of $\overline{CLK}$ and transferred in sequence. Number of signals in one $\overline{H_{SYNC}}$ period is 160.
Horizontal Synchronous	$\overline{H_{SYNC}}$	1	Signal controlling the scanning timing and display time of each line electrode. Address incremeent to the next line is done at the falling edge of $\overline{H_{SYNC}}$. The number of signals in one $\overline{V_{SYNC}}$ period is required to beat 1024 or more. And a continuous signal is required.
Vertical Synchronous	$\overline{V_{SYNC}}$	1	Signal controlling the refresh speed of the screen. The scanning position returns to the first electrode at the falling edge of the $\overline{V_{SYNC}}$ signal.
Brightness Control	B. C.	1	Signal controlling the brightness of the entire screen. Logic: L: Low brightness H: High brightness.
Display Enable	$\overline{DSPE}$	1	Signal controlling the display enable. Logic: L: On. H: Off

Recommended Electrical Conditions

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Input Voltage (H-Level)	—	V_{IH}	2.4	—	—	V
Input Voltage (L-Level)	—	V_{IL}	—	—	0.4	V
Input Current (H-Level)	V_{IH} = 2.75 V, V_{CC} = 5.25 V	I_{IH}	—	—	20	µA
Input Current (L-Level)	V_{IL} = 0.4 V, V_{CC} = 5.25 V	$_{VIL}$	—	—	-3.0	mA

Relationship Between Display Data and Display Dot

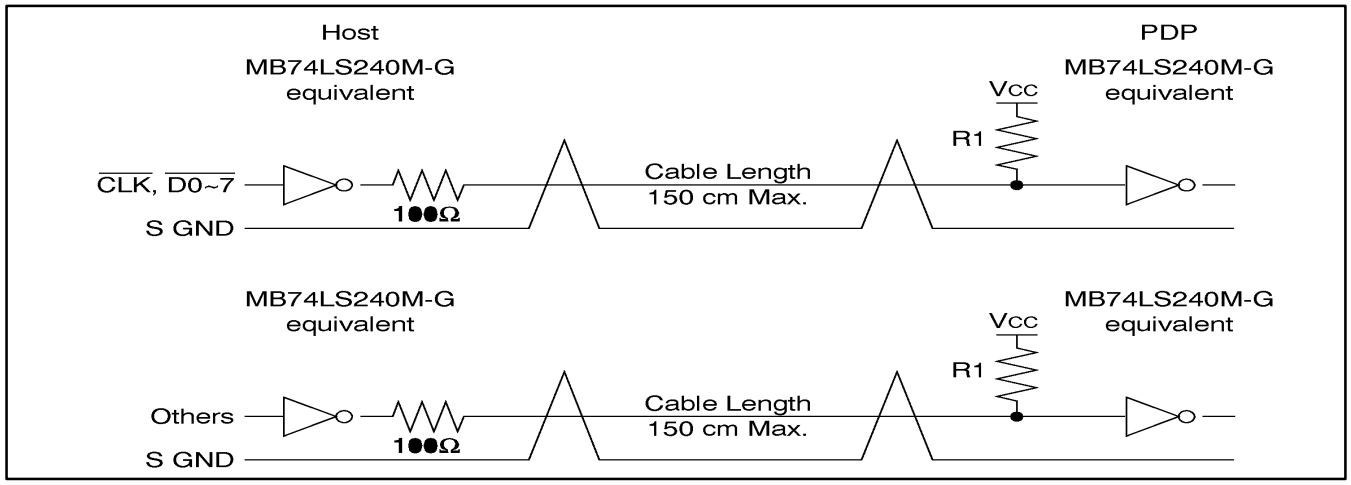


Interface Signal Timing

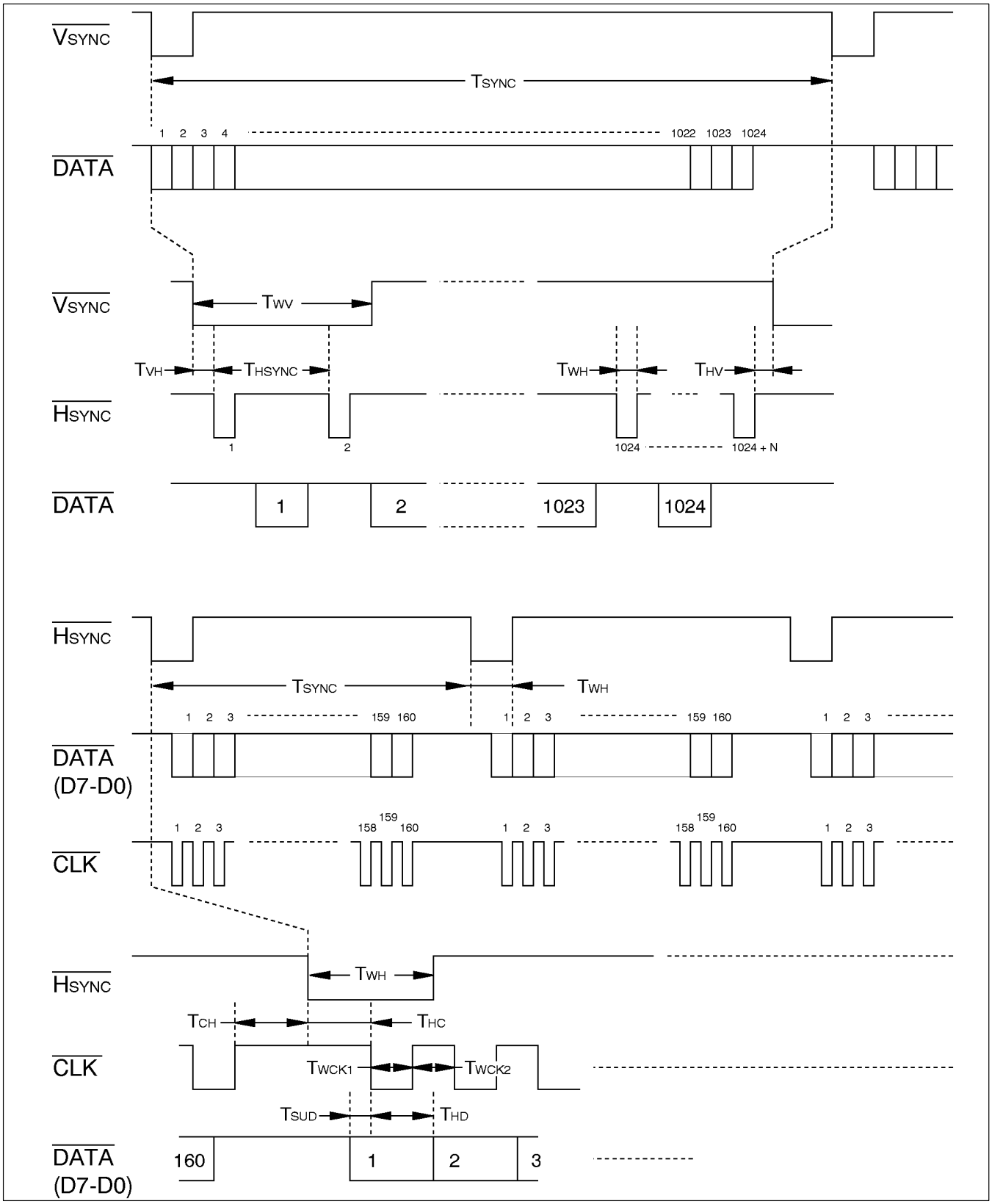
Symbol	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}	1024	1067		H	F_{VSYNC} = 16 Hz (Typ.)
t_{WV}	1	3		H	
t_{VH}	1	14		µs	
t_{HV}	2	15.25		µs	
T_{HSYNC}	58.8	60.0	61.2	µs	
t_{WH}	1	2.7		µs	
t_{HC}	0.5	3.5		µs	
t_{CH}	0.1	3.5		µs	
t_{CLK}	166.7	333.3		ns	F_{CLK} = 3 MHz (Max.)
t_{WCLK1}	Typ – 10%	1/2 t_{CLK}	Typ +10%	ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{WCLK2}	Typ – 10%	1/2 t_{CLK}	Typ +10%	ns	Duty = 50% (Typ.)
t_{SUD}	40			ns	
t_{HD}	70			ns	

Note: Values in parenthesis () are the one example of timing condition.

Interface Circuit



Interface Signal Timing Chart

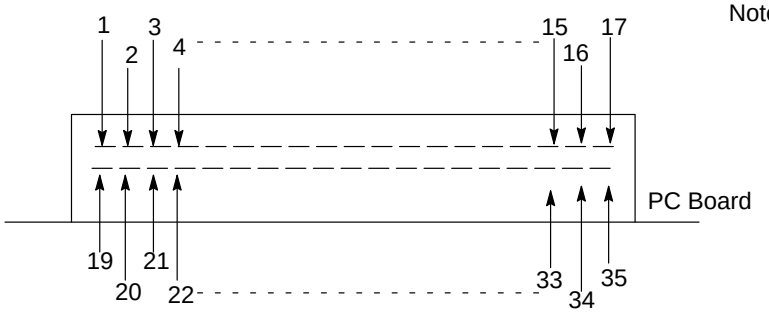


CONNECTOR PIN ASSIGNMENT

Signal Connector

P/N:HIF6-34PA-1.27DS (by Hirose) Mating Connector: HIF6-34B-1.27R (by Hirose)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	$\overline{\text{DATA 7}}$	2	S. GND	19	H_{SYNC}	20	S. GND
3	$\overline{\text{DATA 6}}$	4	S. GND	21	V_{SYNC}	22	S. GND
5	$\overline{\text{DATA 5}}$	6	S. GND	23	DSPE	24	S. GND
7	$\overline{\text{DATA 4}}$	8	S. GND	25	Ext B. C	26	S. GND
9	$\overline{\text{DATA 3}}$	10	S. GND	27	Reserve	28	S. GND
11	$\overline{\text{DATA 2}}$	12	S. GND	29	No Connection	30	S. GND
13	$\overline{\text{DATA 1}}$	14	S. GND	31	V_{CC} (OUT)	32	S. GND
15	$\overline{\text{DATA 0}}$	16	S. GND	33	V_{CC} (OUT)	34	S. GND
17	$\overline{\text{CLK}}$			35	V_{CC} (OUT)		



Notes: 1) This drawing shows the signal connector which is viewed from the mating side.
2) The actual connector has 34 pins, the numbering is to the 36th pin in this specification. The 18th and 36th pins are the missing numbers. On the PC board the numbers which is equivalent to 36 pins are printed with silk printing
3) The trianagle mark on the connector is not corresponding to the 1st pin. The 31st, 33rd, and 35th pins output is +5 V of DC voltage. The 27th pin is to be connected with GND.

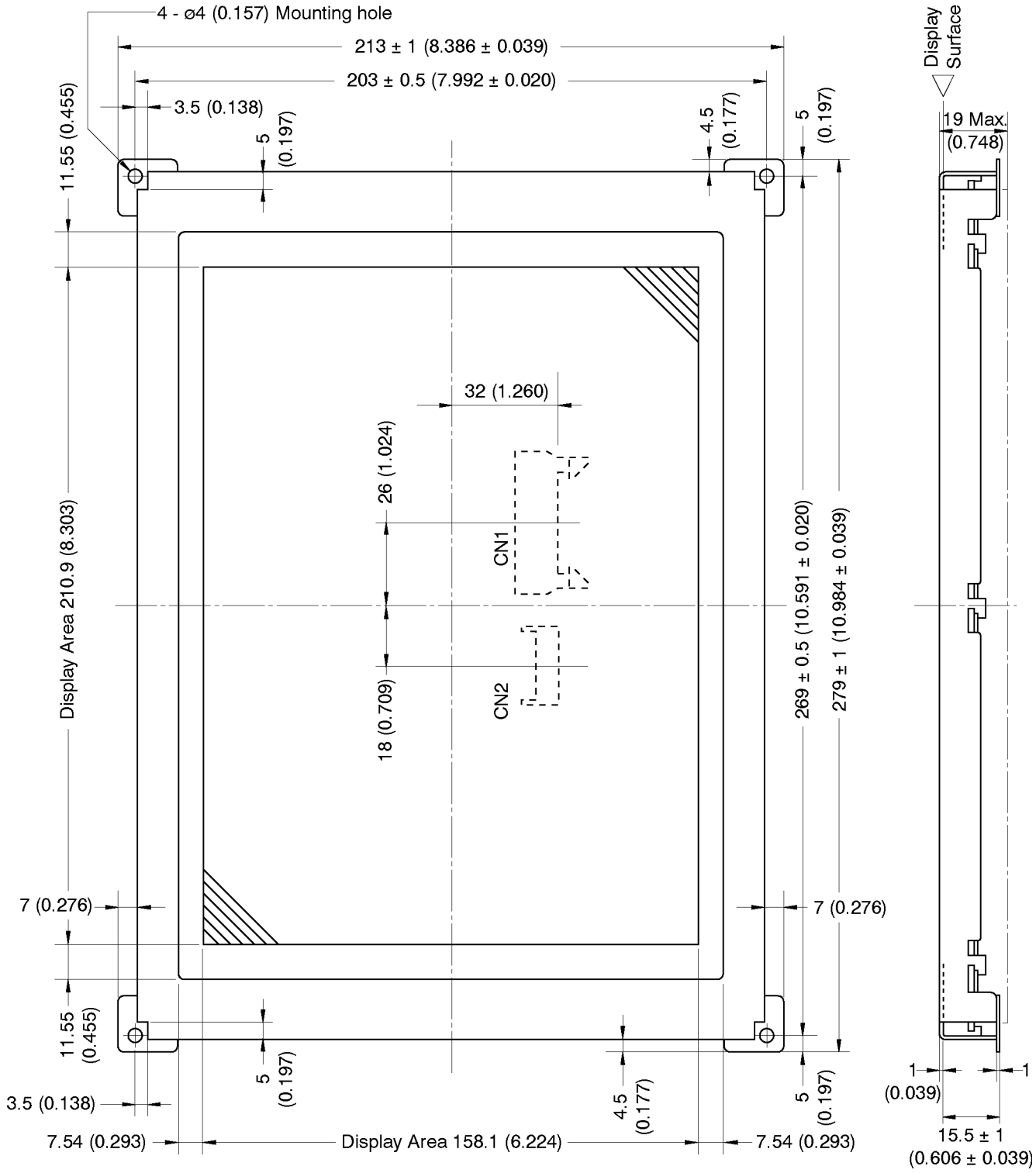
Power Supply Connector

PDP Side Connector: FCN–815P–009TA (by Fujitsu)

Pin No.	Power Source Name
1	Vcc
2	S. GND
3	N. C.
4	GND (H)
5	Vs
6	N. C.
7	N. C.
8	S. GND
9	VR (output)

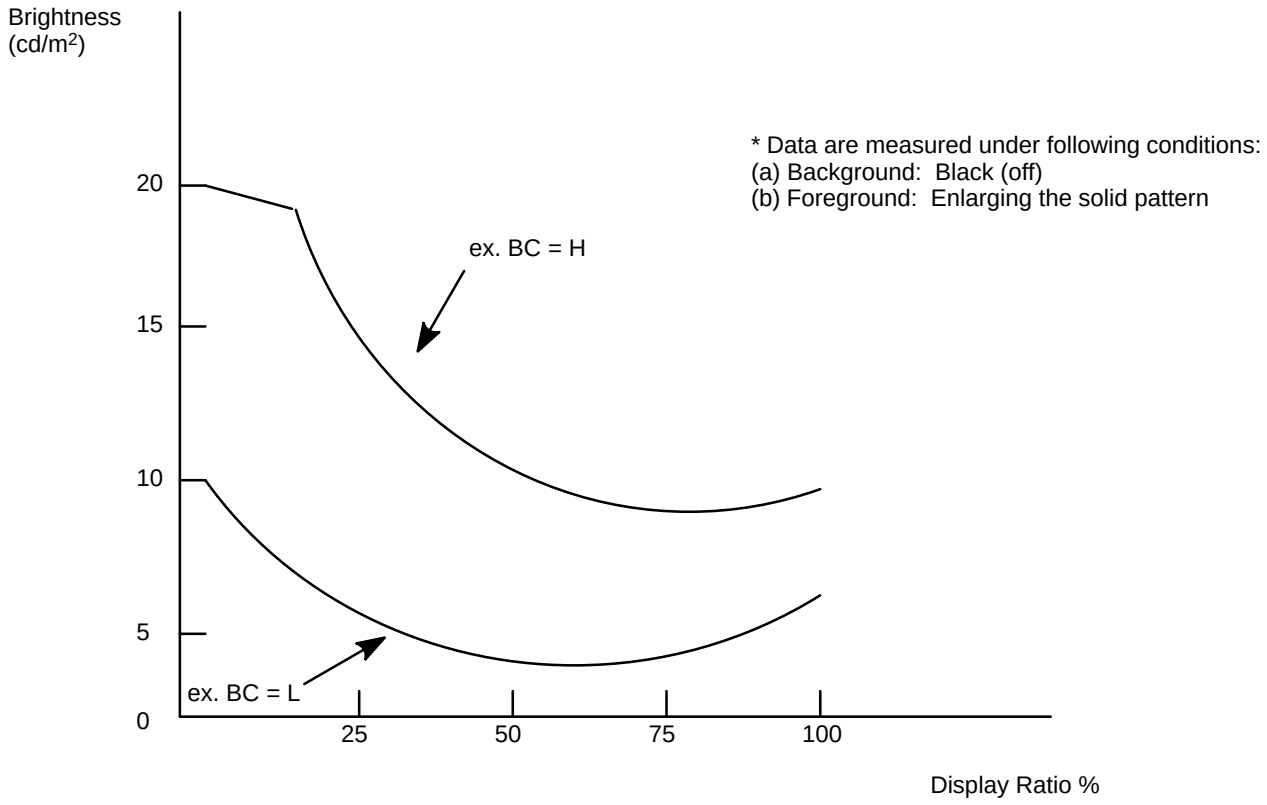
Mating Connector (by Fujitsu)
Housing: FCN–813J009–A
Contact: FCN–813J–T/Q (hand crrimping) FCN–813J–T/S (hand crimping)
FCN–813J–T/R (automatic crimping machine) FCN–813J–T/T (automatic crimping machine)

External Dimensions



Relation Between Display Ratio and Brightness

In general, the increased display ratio will increase the current of the VS. This plasma display is employing the Automatic Power Controller Circuit. Therefore, when the current value of Vs is set at 300 mA, the brightness will decrease gradually after exceeding the display ratio of 25%. When the current is limited by Automatic Power Controller Circuit, the brightness decreases.



Section 7

Graphic Type Stand-alone Units (units plus power supplies plus enclosure) — *At a Glance*

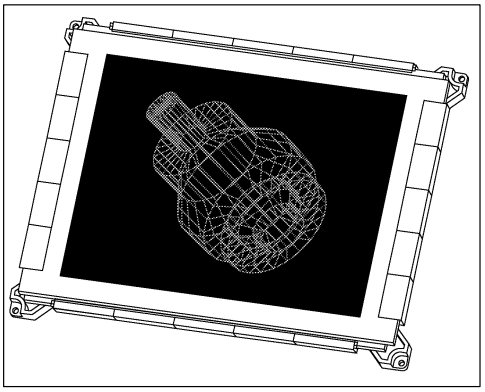
July 1990
Edition 1.0

FUJITSU

DATA SHEET

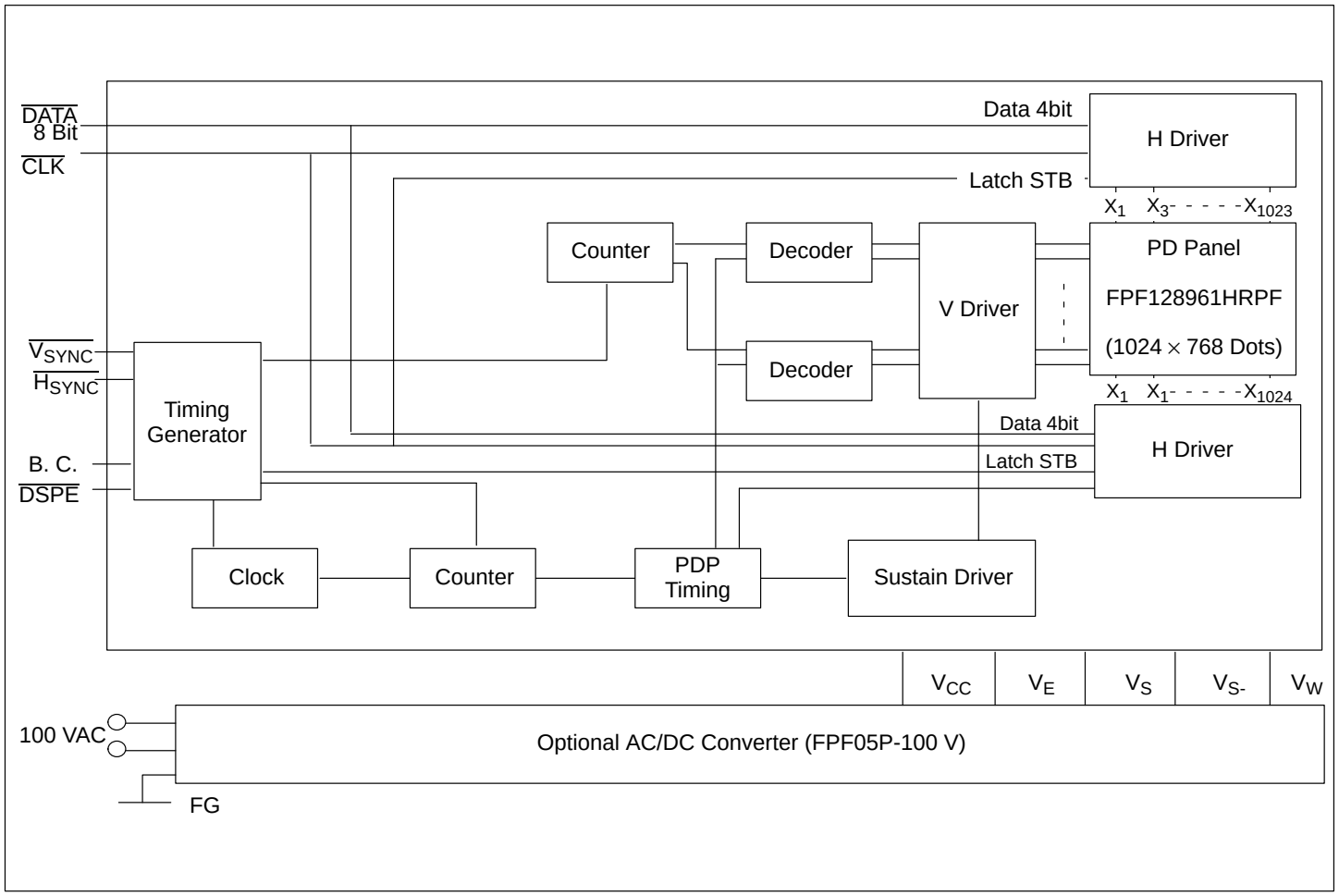
FPF12000SA
Plasma Display Graphics Unit

The Fujitsu FPF12000SA plasma display has a low–profile standalone structure. It can be sued in a wide variety of office automation systems as a space–saving display or a wall–type display.



- Bright, flickering–free display
- 1024 x 768 dot high–resolution graphic display
- Small. thin low power
- Combinations to CRT interface
- Keyboard connection terminal
- 100 VAC single power supply
- Wal–type display (metal hook optional)

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Maximum Ratings
Input Power Voltage	AC IN	135 VAC
Input Signal Voltage	V_1	–0.5 V to +5.5 V

DC Characteristics

Input voltage (Level H)	V_{IH}	2.4	–	–	V
Input voltage (Level L)	V_{IL}	–	–	0.4	V
Input current (Level H) (V_{IH} = 2.75 V V_{CC} = 5.25 V)	I_{IH}	–	–	20	µA
Input current (Level L) (V_{IH} = 0.4 V V_{CC} = 5.25 V)	I_{IL}	–	–	–16	mA
Input voltage (Speaker input (p–p)				0.7	V
Speaker input frequency		0.4		5	kHz

MECHANICAL SPECIFICATIONS

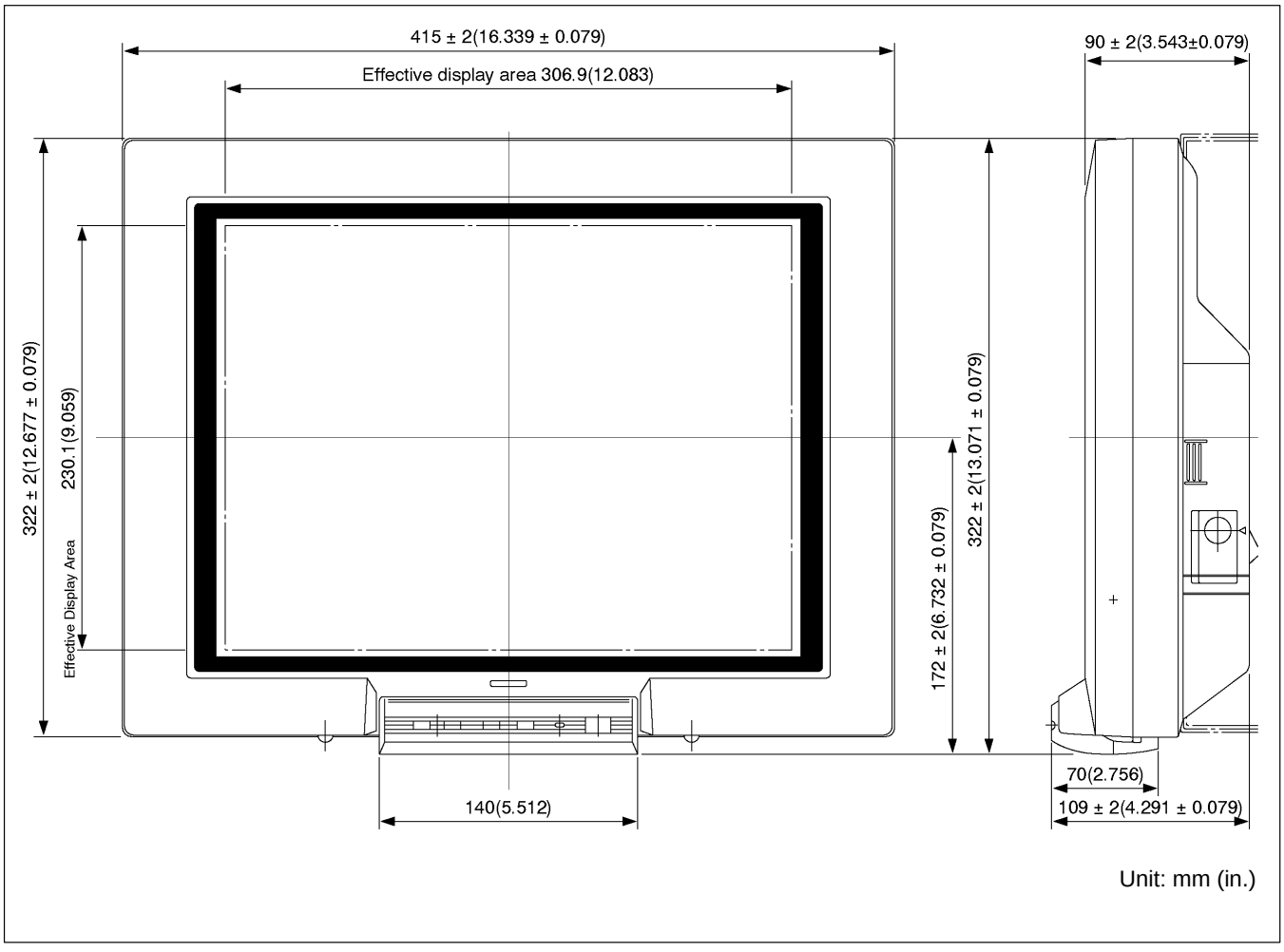
Physical Specifications

Item	Specification
Display Panel	FPF12896HRPF
Number of Display Dots	1024 (H) x 768 (V) dots (786,432 dots)
Dot Pitch	0.3 (H) X 0.3 (V) (0.012 X 0.012 in)
Dot Size	Approximately 0.2 mm (0.008 in)
Screen Size	307 x 230 mm (12.087 x 9.055 in)
Display Color	Neon Orange
Dot Brightness	5 cd/m^2 min (with filter, average)
Brightness Unevenness	Up to 50%
Contrast ratio	20:1 min
Viewing angle	120° min
Weight	Approximately 5Kg
External Dimensions	See External Dimensions Figure

Performance Specifications

Item	Rating
Operating Temperature	5 to +35°C
Storage Temperature	–10 to +50°C
Humidity	20 to 80% RH (no condensation)
Atmospheric Pressure Durability	700 to 1114 hPa
Vibration	Operation: 0.2 G (3–60 Hz sine wave, double sweep time: 2 minutes Non–Operation: 0.4G

External Dimensions

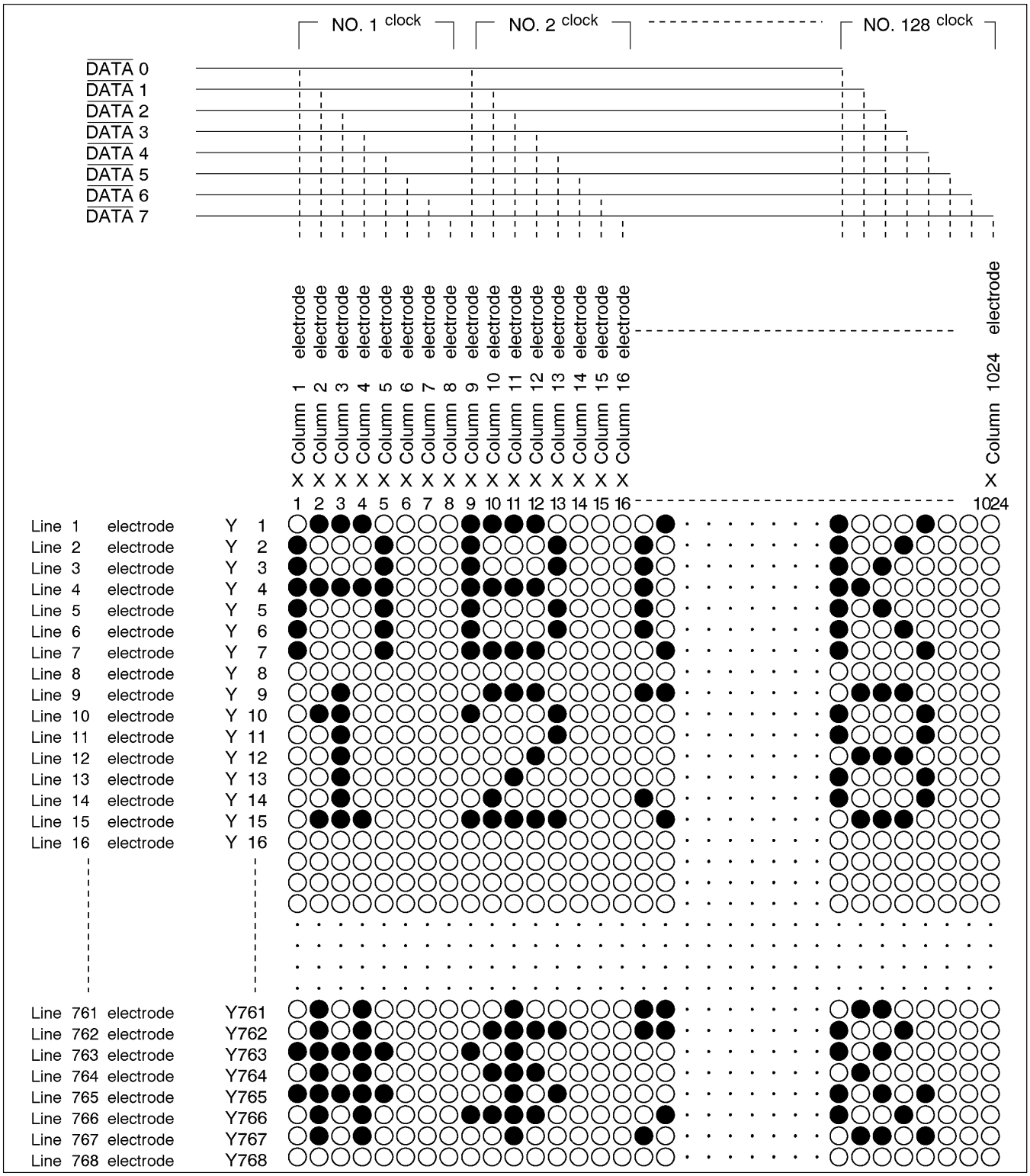


INTERFACE SIGNALS

Type of Signals (TTL)

Signal	Symbol	Number of Lines	Definition and Function
Data	$\overline{DATA0\ to\ 7}$	0	Display data signal Logic L: On, H: Off The relationship between $\overline{DATA0\ to\ 7}$ and display location is shown in the following figure.
Clock	$\overline{CLK}$	1	The display data transfer signal fetches and transfers data sequentially at the falling edge. The number of clock signals during one $\overline{H_{SYNC.}}$ cycle is 128.
Line Synchronous	$\overline{H_{SYNC}}$	1	The signal which controls the period of the display. When this signal is at the falling edge, the address increments to the next line–electrode. The number of $\overline{H_{SYNC}}$ signals per $\overline{V_{SYNC}}$ cycle is 769 and must be generated at regual intervals.
Frame Synchronous	$\overline{V_{SYNC}}$	1	This signal controls the start of screen. When this signal is at the falling edge, the address increments to the first column electrode.
Display Enable	$\overline{DSPE}$	1	This signal enables or disables display. Logic L: On, H: Off
Speaker	$\overline{AUDIO}$	1	Speaker sound control signal
Keyboard	$\overline{RDKB}$ $\overline{TDKB}$	2	The signal which controls the keyboard connected to the main unit.
Power Control	$\overline{ON1B}$ $\overline{ON1M}$ $\overline{ON2M}$ $\overline{ON2}$	4	The signal which controls the CPU power switch. (Usually) Jumpered between $\overline{ON1B}$ and GND and between $\overline{ON2M}$ and $\overline{ON2}$ and open for others
LED Lamp	$\overline{RDY}$	1	The signal which is turned on by switching on the CPU power.

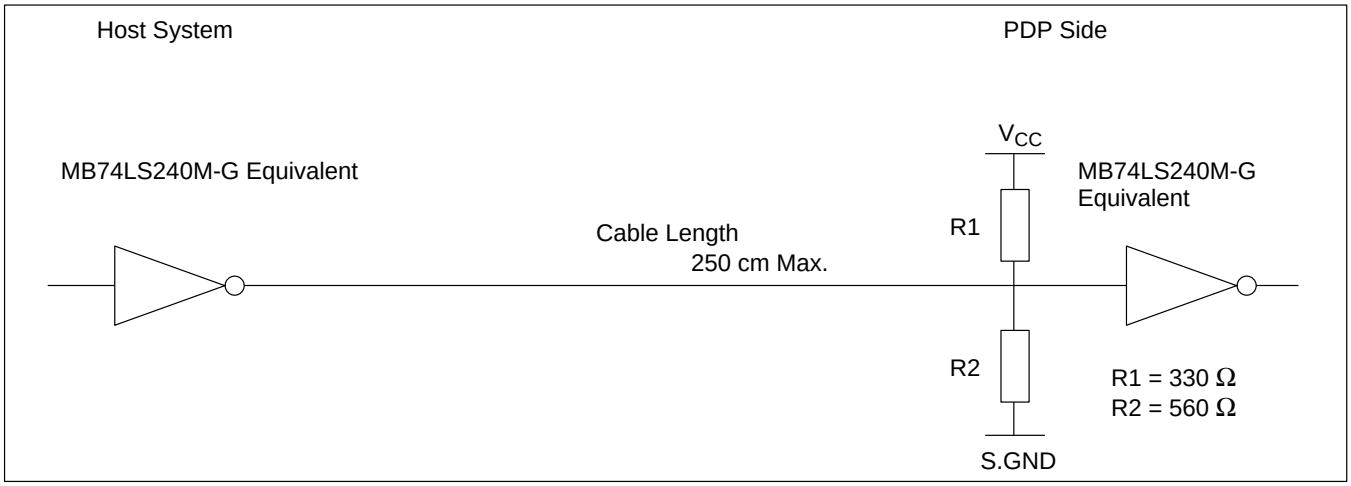
Relationship Between Display Data and Display Dot



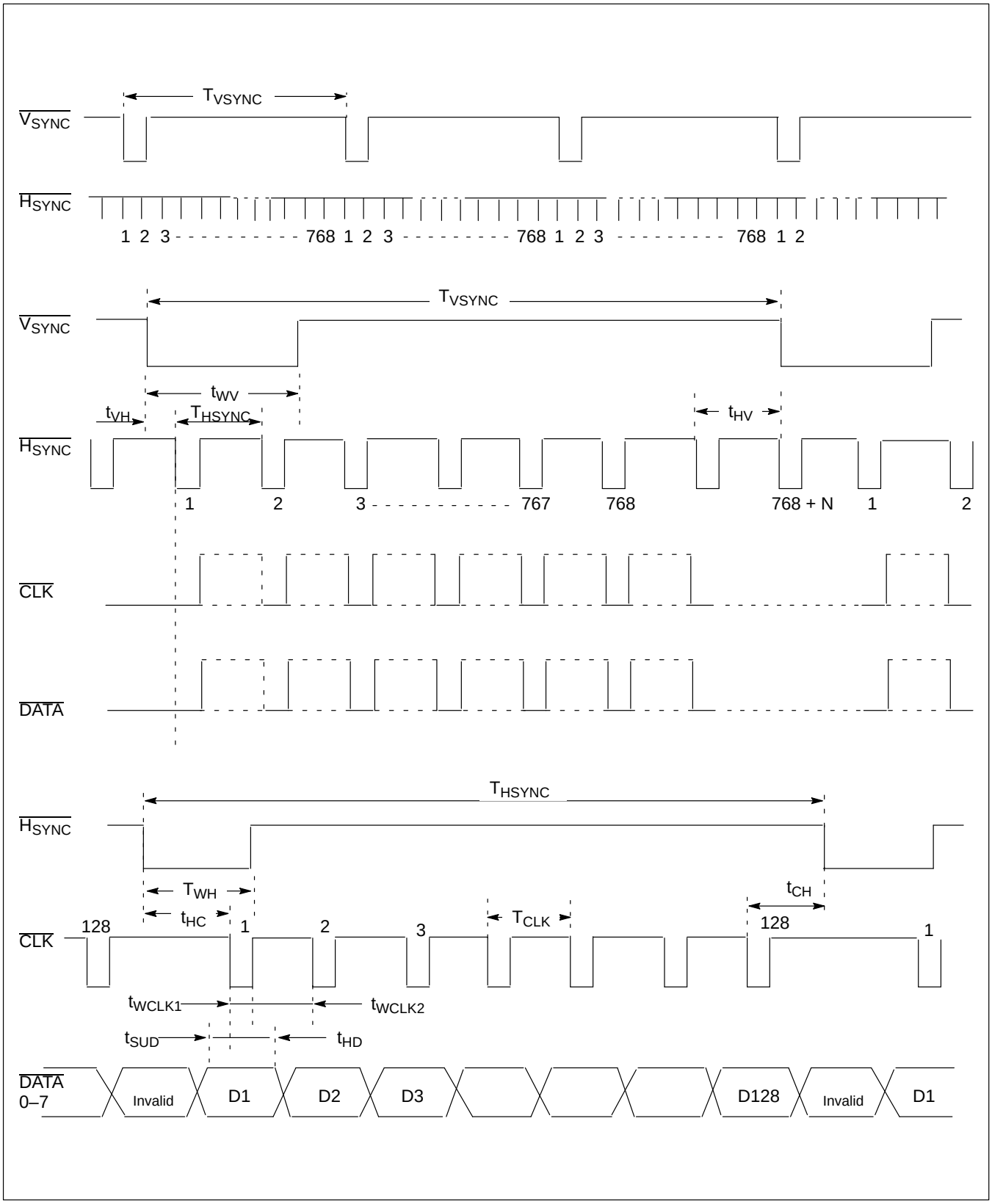
Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}	61.44	61.74	–	ms	F_{VSYNC} = 16 Hz (Typ.)
t_{WV}	2	160		µs	
t_{VH}	1	75		µs	
t_{HV}	5	5.4		µs	
T_{HSYNC}		79.56		µs	±1%
t_{WH}	2	5.4		µs	
tK_C	5	16.74		µs	
t_{CH}	11.7	8		µs	
t_{CLK}	300	360		ns	F_{CLK} = 2.8 MHz (Standard)
t_{WCLK1}	150	180		ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{WCLK2}	150	250		ns	Duty Cycle = 50% (Standard)
t_{SUD}	100	180		ns	
t_{HD}	80	135		ns	

Interface Circuit



Interface Signal Timing Chart



CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN235PO50–G/E (Fujitsu)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	$\overline{\text{DATA 0}}$	2	GND	26	$\overline{\text{ONIB}}$	27	GND
3	$\overline{\text{DATA 1}}$	4	GND	28	$\overline{\text{ON1M}}$	29	N.C.
5	$\overline{\text{DATA 2}}$	6	GND	30	$\overline{\text{ON2M}}$	31	$\overline{\text{ON2}}$
7	$\overline{\text{DATA 3}}$	8	GND	32	$\overline{\text{RDY}}$	33	GND
9	$\overline{\text{DATA 4}}$	10	GND	34	$\overline{\text{AUDIO}}$	35	GND
11	$\overline{\text{DATA 5}}$	12	GND	36	N.C.	37	N.C.
13	$\overline{\text{DATA 6}}$	14	GND	38	TDKB	39	GND
15	$\overline{\text{DATA 7}}$	16	GND	40	RDKB	41	GND
17	$\overline{\text{CLK}}$	18	GND	42	GND	43	GND
19	$\overline{\text{H}_{\text{SYNC}}}$	20	GND	44	GND	45	GND
21	$\overline{\text{V}_{\text{SYNC}}}$	22	GND	46	+12V	47	+12V
23	$\overline{\text{DSPE}}$	24	GND	48	+5V	49	+5V
25	$\overline{\text{NC}}$			50	+5V		

Power Connector

GL–2030F (Tokin Corp)

Pin No.	Signal
1	AC
2	AC (COM)
3	FG

Keyboard Connector

Pin No.	Signal	Pin No.	Signal
1	RDKB	5	GND
2	TDKB	6	GND
3	GND	7	V_{CC}
4	GND	8	V_{CC}

June 1992
Edition 2.0

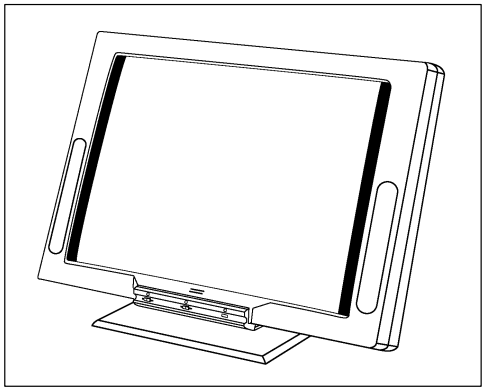
FUJITSU

DATA SHEET

FPF20000S–501
Plasma Display Monitor

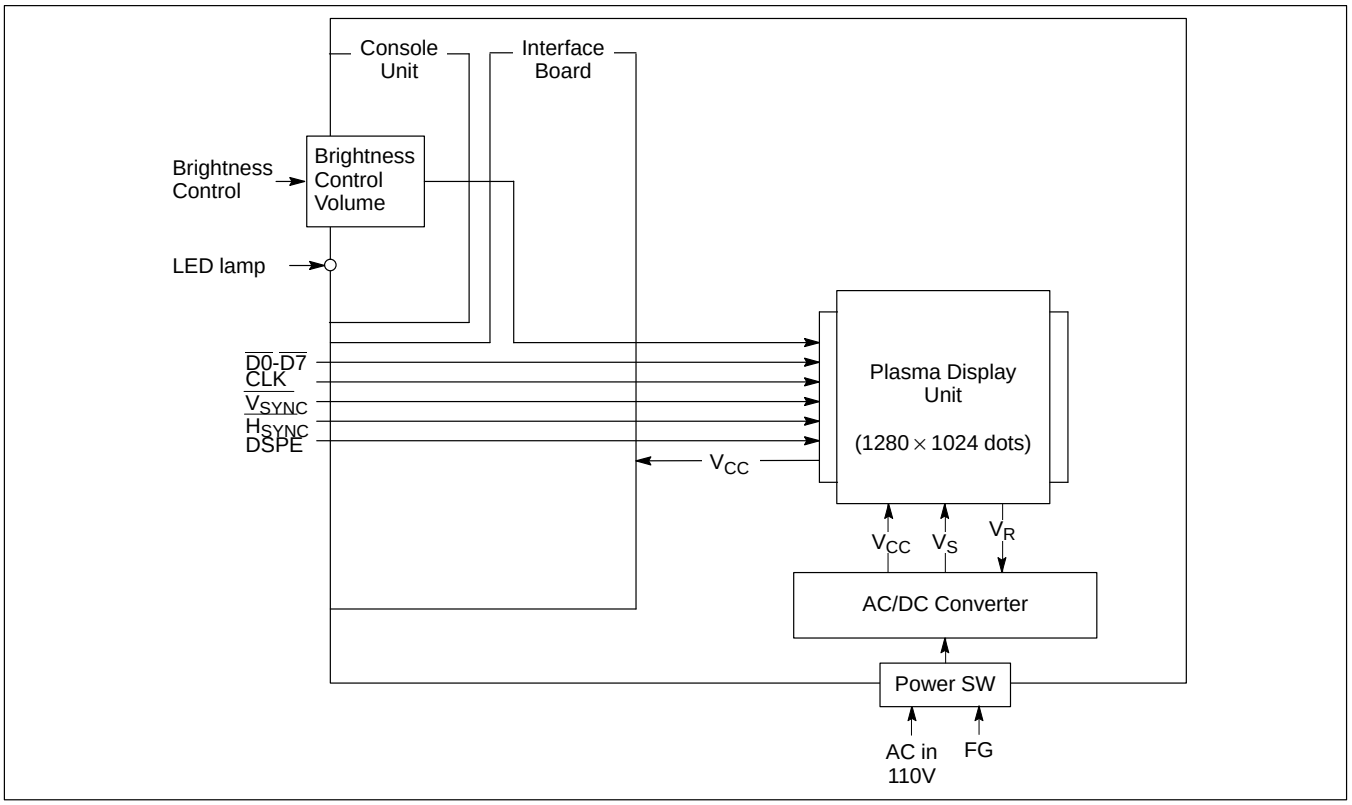
Fujitsu's FPF20000S-501 plasma display is a stand-alone, high resolution, plasma display that offers a large screen (16-inch diagonal effective display area) with a 1280 × 1024-dot capacity (100 dots per inch). The display's thin-profile design has a depth of about one-fifth that of a standard CRT (only 3.5 in. package depth).

Because of Fujitsu's AC memory technology, the display has a reliability of 50,000 hours with no brightness degradation, image burn-in, or flicker over time. This high reliability, coupled with space-saving construction, makes the FPF20000S-501 ideal for QA equipment, engineering workstations, x-terminals, medical monitors, and CAD systems.



- Interface to Sun SPARC stations (IPC, IPX, SPARC Station 2)
- Large 16-inch diagonal screen with 1280 (H) × 1024 (W) pixel format (1.3 megapixel)
- Thin-profile design (14.33 lb)
- Reliability of 50,000 hours with no brightness degradation over time
- Display is free from flicker, warp, and image burn-in
- Easy-to-use interface complies with CRT standards
- Unit includes stand with tilt capability (+5 to –15°)
- FCC class A, UL, and CSA approved

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Input Power Voltage	AC IN	135 VAC
Input Signal Voltage	V1	-0.5 V to +5.5 V

DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage (H)	V_{IH}	–	2.0	–	–	V
Input voltage (L)	V_{IL}	–	–	–	0.8	V
Input current (H)	I_{IH}	V_{CC} = 5.25V, V_I = 2.7V	–	–	20	µA
Input current (L)	I_{IL}	V_{CC} = 5.25V, V_I = 0.4V	–	–	-4	mA

Note: Values are measured at the input connector.

MECHANICAL SPECIFICATIONS

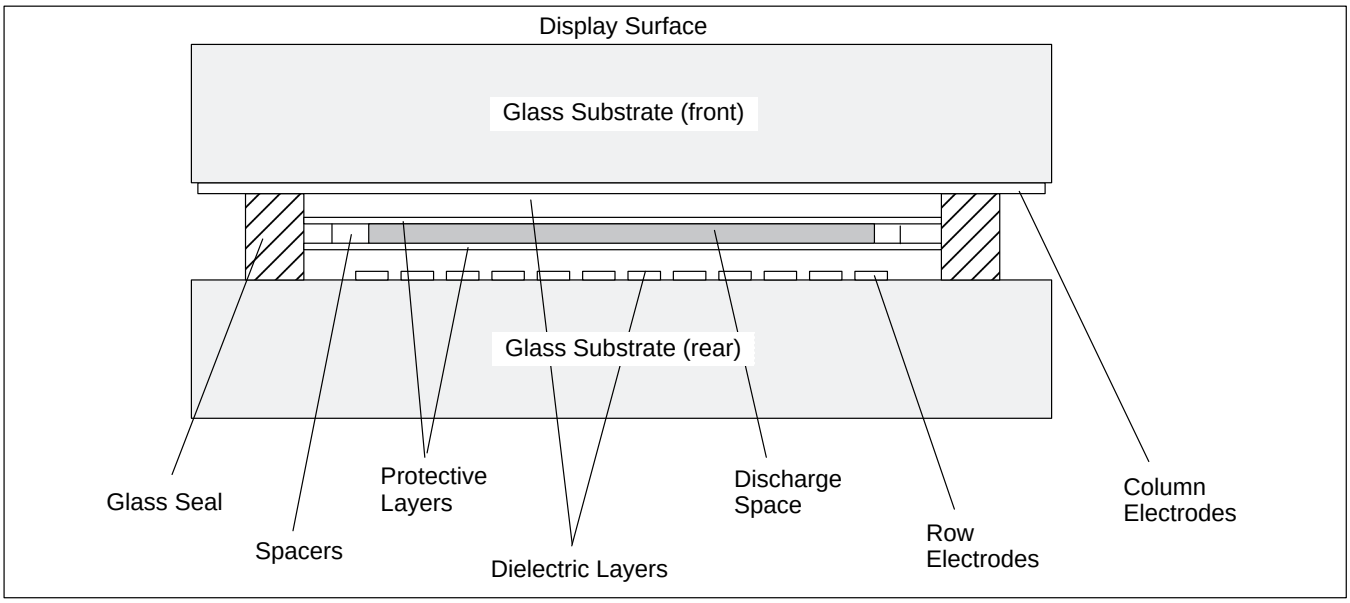
Physical Specifications

Item		Specification
Display Performance	Display Capacity	1280 (H) × 1024 (V) dots (1,310,720 dots)
	Dot Pitch	0.25 (H) × 0.25 (V) mm (0.010 × 0.010 in.)
	Dot Size	Approximately 0.15 mm (0.006 in.) diameter
	Display Area	320 (H) mm × 256 (V) mm (12.60 in. × 10.08 in.)
	Display Color	Neon Orange
	Brightness	7 cd/m^2 or more (at the display ratio of 30% max.)
	Contrast	20:1 or more under office lighting conditions (500 lux)
	Viewing Angle	120°
	Brightness Unevenness	Approximately 50%
Interface	Method	CRT Interface Compliance
	Vertical Sync.	$\overline{V_{SYNC}}$ 33.33 ms Typ. (approx. 30 Hz)
	Horizontal Sync.	$\overline{H_{SYNC}}$ 31.25 µs Typ. (approx. 32 kHz)
	Dot Clock	$\overline{CLK}$ 166.7 ns min. (approx. 6 MHz)
	Display Dot Data	$\overline{D0}$ to $\overline{D7}$ 8 bit parallel display data
	Display Enable	$\overline{DSPE}$ (logic L: On, H: Off)
Power Supply	Input Voltage	100 VAC ± 10%
	Frequency	50/60 Hz ± 5%
	Power Consumption	Approximately 60 W max. (30 W max. for PDP)
Style	Construction	Standalone (with tilt stand)
	Dimensions	415 (W) × 346 (H) × 90 (D) mm (without tilt stand) (approx. 16.34 (W) × 13.62 (H) × 3.54 (D) in.) 415 (W) × 346 (H) × 200 (D) mm (with tilt stand) (approx. 16.34 (W) × 13.62 (H) × 7.8 (D) in.)
Weight	Approximately 14.33 lb (excluding cable)	

Performance Specifications

Item	Rating
Operating Temperature	0 to +35°C
Storage Temperature	–20 to +60°C
Humidity	20 to 80%RH (no condensation)
Atmospheric Pressure	700 to 1114 hPa
Electro Static Damage (ESD) resistance	9KV or greater (No wrong operation after applying for 3 minutes.)

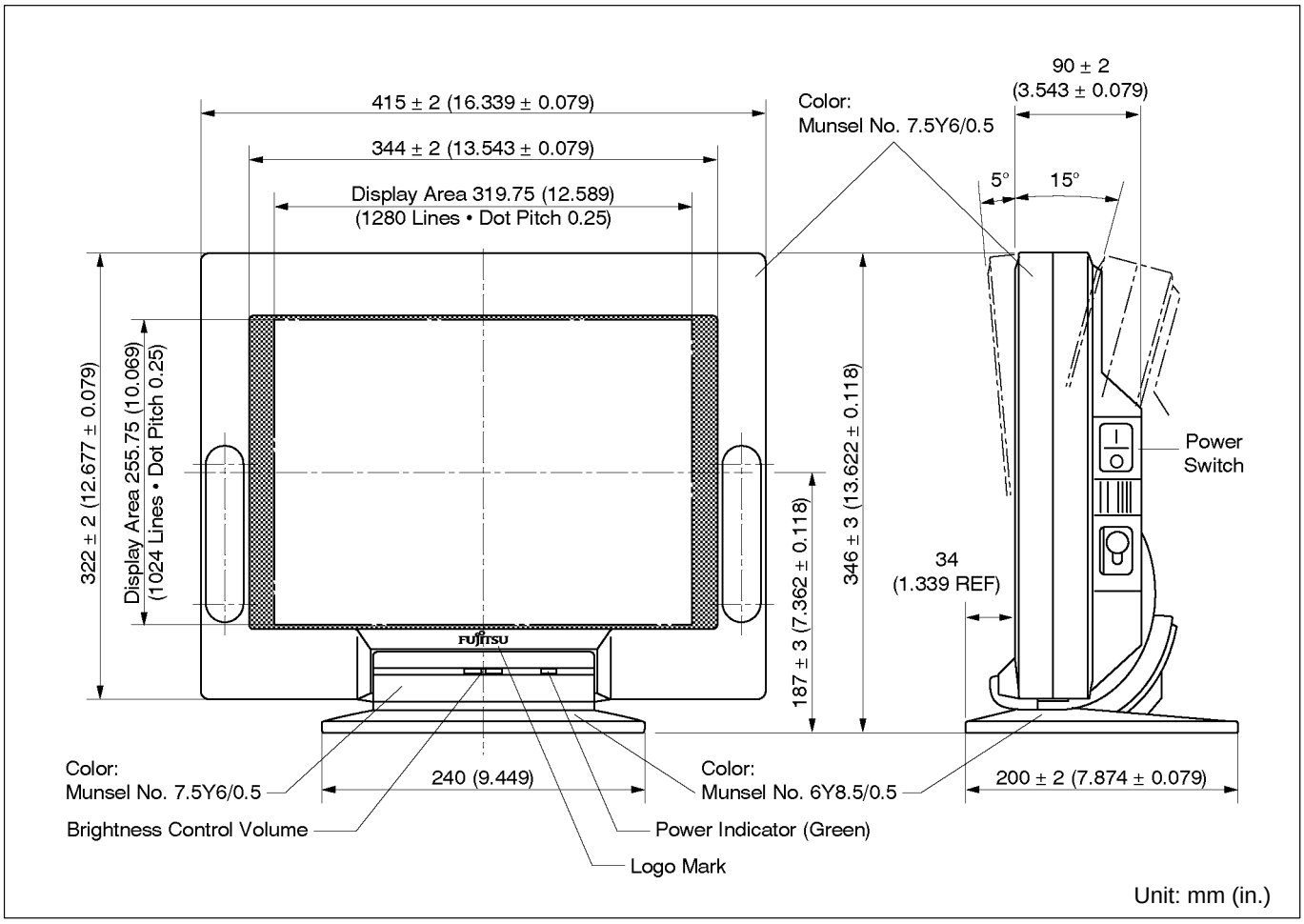
Physical Construction and Operation



PDP Construction and Operation

The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

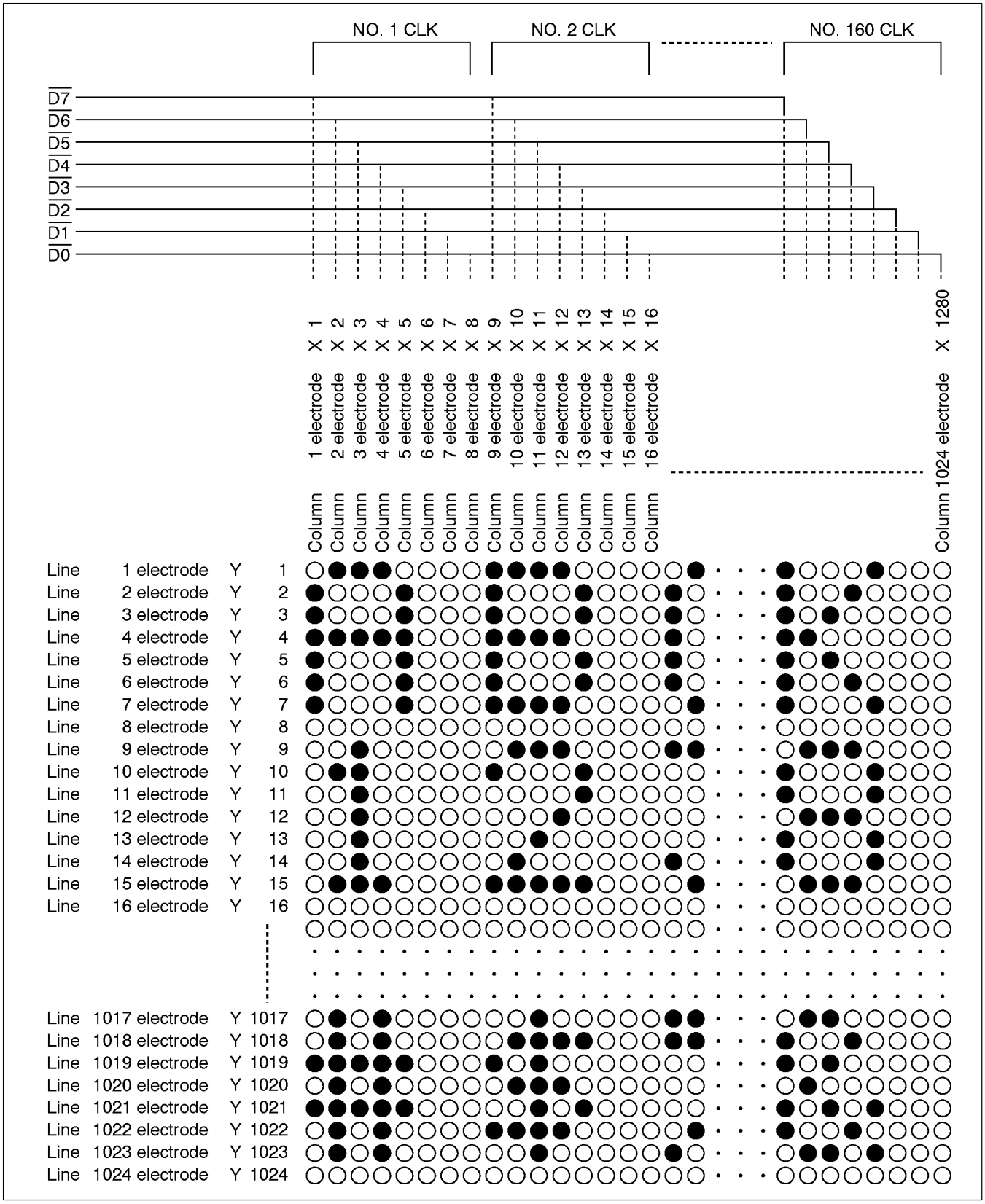


INTERFACE SIGNALS

Types of Signals

Signal Name	Symbol	I/O	Signal Line	Definition and Function
Display data	$\overline{D0}$ to $\overline{D7}$	I	8 lines	8-bit parallel display data. Logic L: On, H: Off The display position and relation between $\overline{D0}$ to $\overline{D7}$ is shown in the figure “Relationship Between Display Data and Display Dots” on the following page.
Clock	$\overline{CLK}$	I	1 line	Timing signal for display data. Display data are loaded at falling edge of this signal and transferred in sequence. 160 clock signals in one $\overline{H_{SYNC}}$ period.
Horizontal synchronous	$\overline{H_{SYNC}}$	I	1 line	Signal controlling the scanning timing and display time of each line electrode. Address increment to next line is done at the falling edge of $\overline{H_{SYNC}}$. 1024 or more $\overline{H_{SYNC}}$ signals in one $\overline{V_{SYNC}}$ period are required.
Vertical synchronous	$\overline{V_{SYNC}}$	I	1 line	Signal controlling the refresh speed of the screen. The scanning position returns to the first line electrode at the falling edge of $\overline{V_{SYNC}}$ signal.
Display enable	$\overline{DSPE}$	I	1 line	Signal controlling the display enable. Logic L: On, H: Off
Reserved	(res)	–	14 lines	Signal line is not permitted to be connected.

Relationship Between Display Data and Display Dots

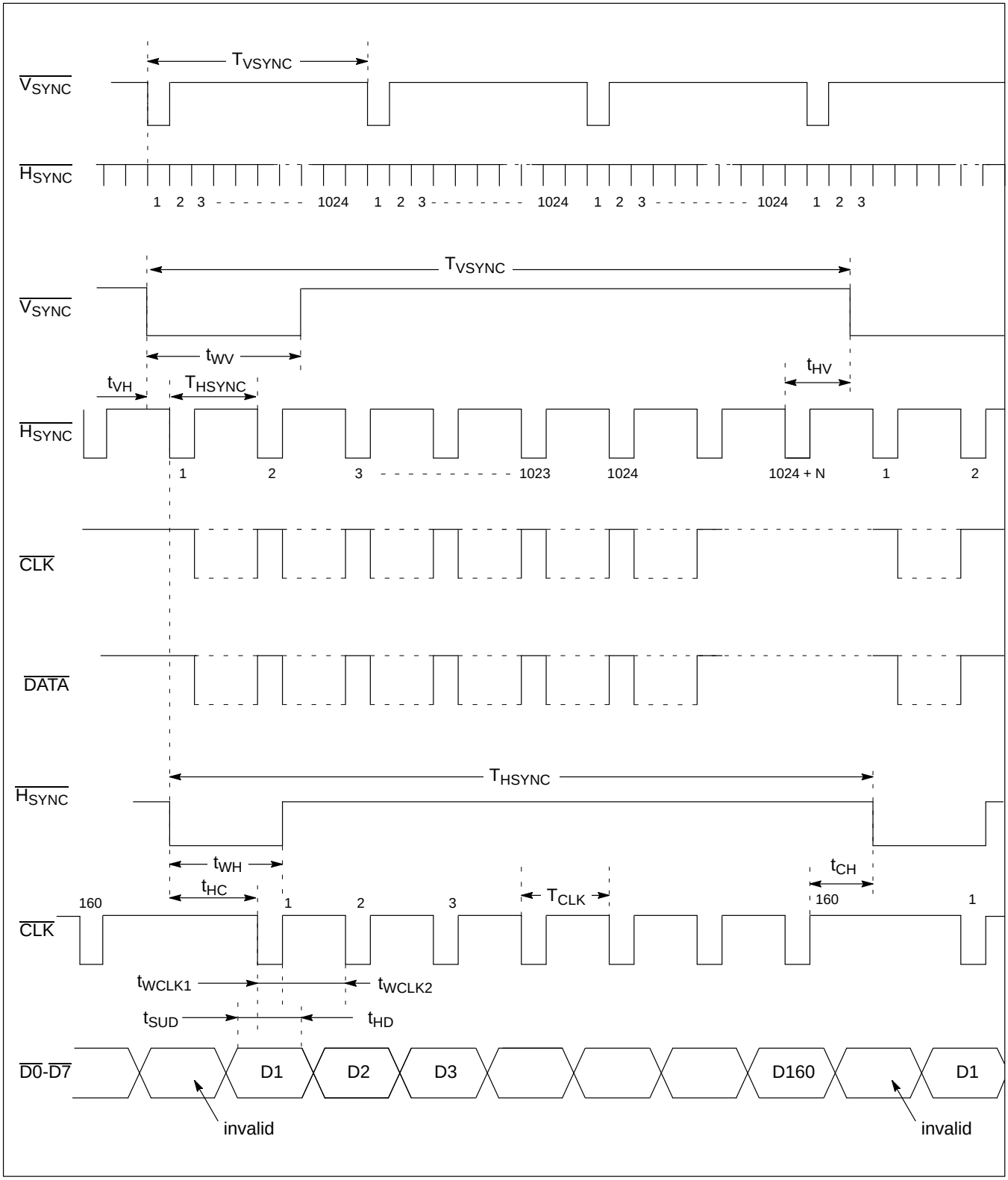


Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}	1024	(1067)	—	H	F_{VSYNC} = (30) Hz (Typ.)
t_{WV}	1	(3)	—	H	H = T_{HSYNC}
t_{VH}	1	(14)	—	µs	
t_{HV}	2	(17.25)	—	µs	
T_{HSYNC}	30.0	(31.25)	45	µs	T_{HSYNC} = (32) kHz (Typ.)
t_{WH}	1	(2)	—	µs	
t_{HC}	0.5	(2)	—	µs	
t_{CH}	0.1	(2.7)	—	µs	
T_{CLK}	166.7	—	—	ns	F_{CLK} = 6 MHz
t_{WCLK1}	83.3	—	—	ns	t_{WCLK1} + t_{WCLK2} = T_{CLK} DUTY = 50% (typ.)
t_{WCLK2}	83.3	—	—	ns	
t_{SUD}	40	—	—	ns	
t_{HD}	70	—	—	ns	

Note: Values in parentheses ( ) are the one example of timing condition.

Interface Signal Timing Chart



Notes: [1]N = 0, 1, 2 . . . .
[2]Number of CLKs in one $\overline{H_{SYNC}}$ period is 160. The continuous CLS is not permitted.

CONNECTOR PIN ASSIGNMENT

Pin Arrangement of Interface Signals (Display Side)

No.	Symbol	No.	Symbol	No.	Symbol	No.	Symbol
1	$\overline{D7}$	2	GND	26	(res)	27	GND
3	$\overline{D6}$	4	GND	28	(res)	29	GND
5	$\overline{D5}$	6	GND	30	(res)	31	(res)
7	$\overline{D4}$	8	GND	32	(res)	33	GND
9	$\overline{D3}$	10	GND	34	(res)	35	GND
11	$\overline{D2}$	12	GND	36	GND	37	GND
13	$\overline{D1}$	14	GND	38	(res)	39	GND
15	$\overline{D0}$	16	GND	40	(res)	41	GND
17	$\overline{CLK}$	18	GND	42	GND	43	GND
19	$\overline{H_{SYNC}}$	20	GND	44	GND	45	(res)
21	$\overline{V_{SYNC}}$	22	GND	46	(res)	47	(res)
23	$\overline{DSPE}$	24	GND	48	(res)	49	(res)
25	GND			50	(res)		

Notes: Applicable connector: FCN-235D050-G/C
(res): reserved

June 1992
Edition 2.0

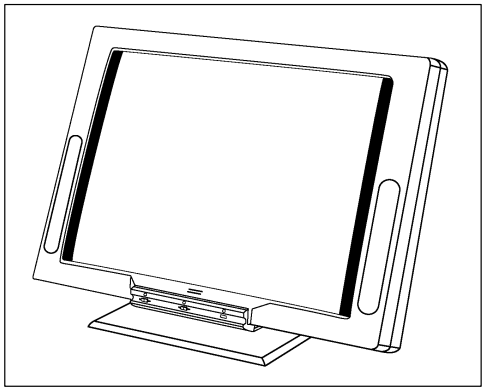
FUJITSU

DATA SHEET

FPF20000S–601
Plasma Display Monitor

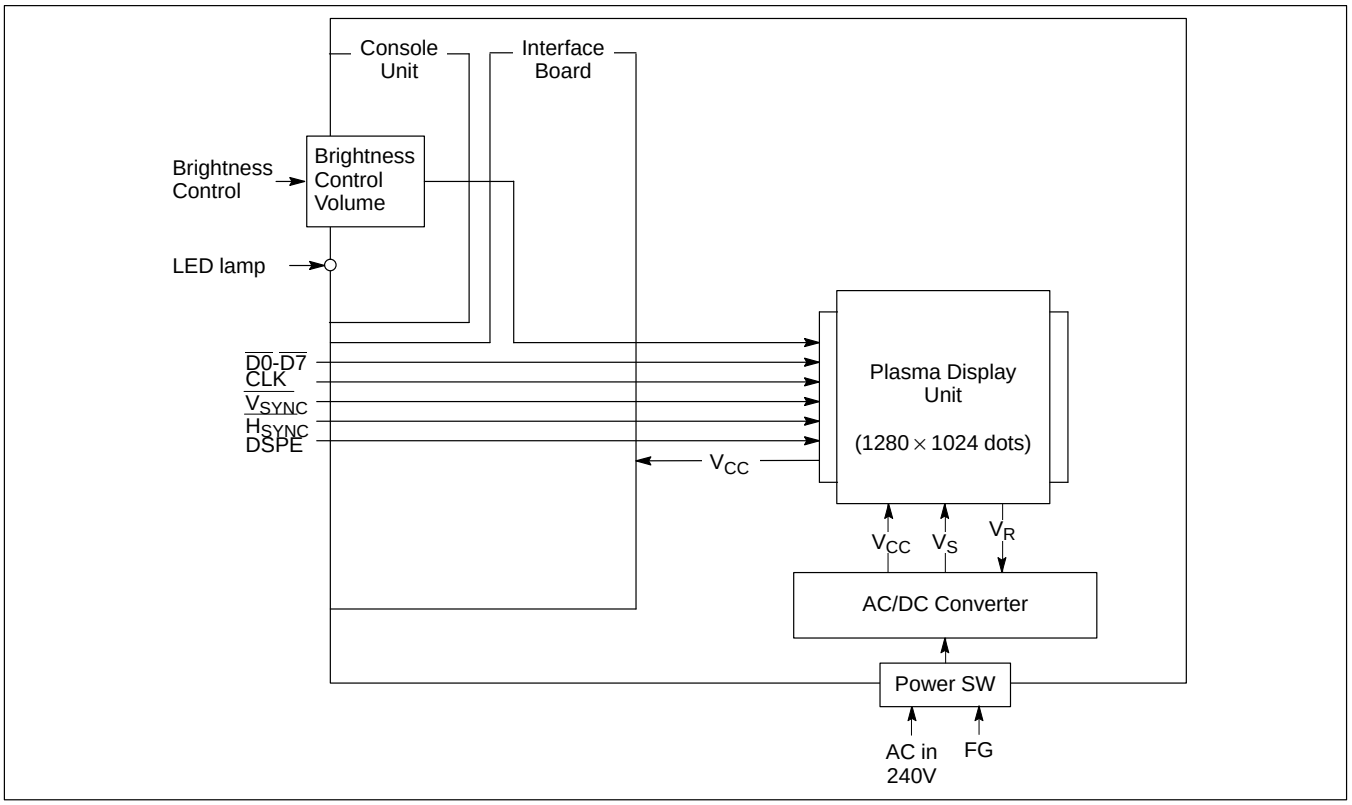
Fujitsu's FPF20000S-601 plasma display is a stand-alone, high resolution, plasma display that offers a large screen (16-inch diagonal effective display area) with a 1280 × 1024-dot capacity (100 dots per inch). The display's thin-profile design has a depth of about one-fifth that of a standard CRT (only 3.5 in. package depth).

Because of Fujitsu's AC memory technology, the display has a reliability of 50,000 hours with no brightness degradation, image burn-in, or flicker over time. This high reliability, coupled with space-saving construction, makes the FPF20000S-601 ideal for QA equipment, engineering workstations, x-terminals, medical monitors, and CAD systems.



- Interface to Sun SPARC stations (IPC, IPX, SPARC Station 2)
- Large 16-inch diagonal screen with 1280 (H) × 1024 (W) pixel format (1.3 megapixel)
- Thin-profile design (16.66 lb)
- Reliability of 50,000 hours with no brightness degradation over time
- Display is free from flicker, warp, and image burn-in
- Easy-to-use interface complies with CRT standards
- Unit includes stand with tilt capability (+5 to –15°)
- FCC class A, UL, and CSA approved

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Rating
Input Power Voltage	AC IN	280 VAC
Input Signal Voltage	V1	-0.5 V to +5.5 V

DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage (H)	V_{IH}	–	2.0	–	–	V
Input voltage (L)	V_{IL}	–	–	–	0.8	V
Input current (H)	I_{IH}	V_{CC} = 5.25V, V_I = 2.7V	–	–	20	µA
Input current (L)	I_{IL}	V_{CC} = 5.25V, V_I = 0.4V	–	–	-4	mA

Note: Values are measured at the input connector.

MECHANICAL SPECIFICATIONS

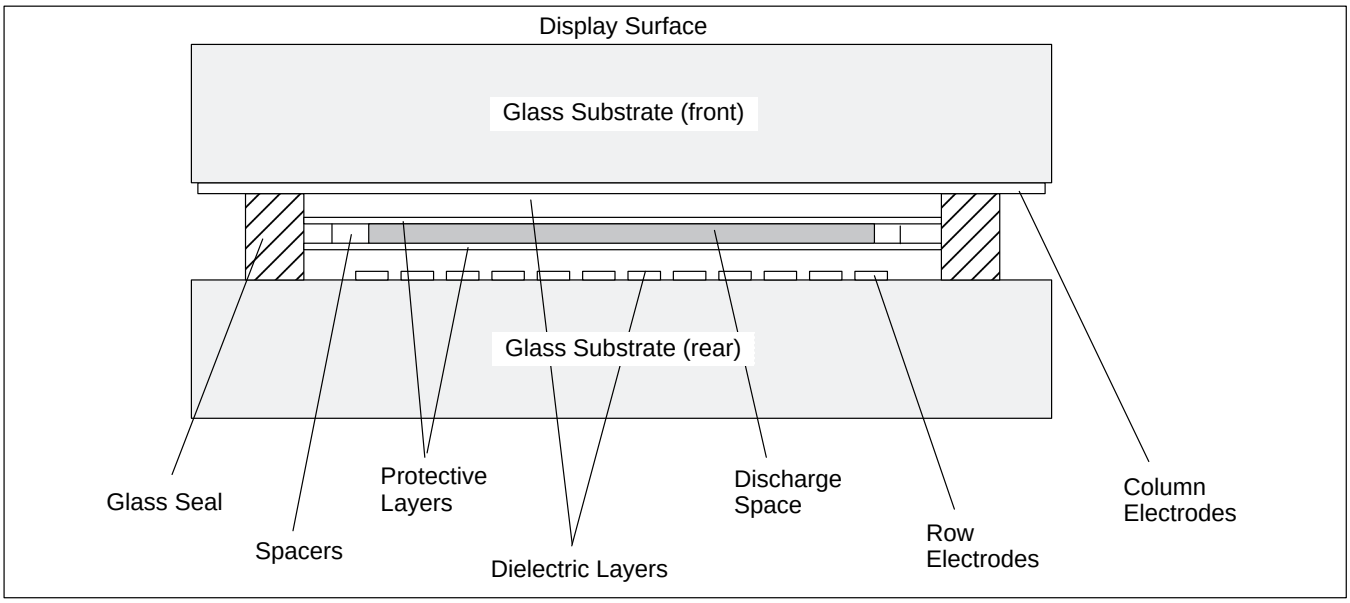
Physical Specifications

Item		Specification
Display Performance	Display Capacity	1280 (H) × 1024 (V) dots (1,310,720 dots)
	Dot Pitch	0.25 (H) × 0.25 (V) mm (0.010 × 0.010 in.)
	Dot Size	Approximately 0.15 mm (0.006 in.) diameter
	Display Area	320 (H) mm × 256 (V) mm (12.60 in. × 10.08 in.)
	Display Color	Neon Orange
	Brightness	7 cd/m^2 or more (at the display ratio of 30% max.)
	Contrast	20:1 or more under office lighting conditions (500 lux)
	Viewing Angle	120°
	Brightness Unevenness	Approximately 50%
Interface	Method	CRT Interface Compliance
	Vertical Sync.	$\overline{V_{SYNC}}$ 33.33 ms Typ. (approx. 30 Hz)
	Horizontal Sync.	$\overline{H_{SYNC}}$ 31.25 µs Typ. (approx. 32 kHz)
	Dot Clock	$\overline{CLK}$ 166.7 ns min. (approx. 6 MHz)
	Display Dot Data	$\overline{D0}$ to $\overline{D7}$ 8 bit parallel display data
	Display Enable	$\overline{DSPE}$ (logic L: On, H: Off)
Power Supply	Input Voltage	220 to 240 VAC
	Frequency	50/60 Hz ± 5%
	Power Consumption	Approximately 60 W max. (30 W max. for PDP)
Style	Construction	Stand-alone (with tilt stand)
	Dimensions	415 (W) × 346 (H) × 90 (D) mm (without tilt stand) (approx. 16.34 (W) × 13.62 (H) × 3.54 (D) in.) 415 (W) × 346 (H) × 200 (D) mm (with tilt stand) (approx. 16.34 (W) × 13.62 (H) × 7.8 (D) in.)
Weight	Approximately 16.66 lb (excluding cable)	

Performance Specifications

Item	Rating
Operating Temperature	0 to +35°C
Storage Temperature	–20 to +60°C
Humidity	20 to 80 %RH (no condensation)
Atmospheric Pressure	700 to 1114 hPa
Electro Static Damage (ESD) resistance	9KV or greater (No wrong operation after applying for 3 minutes.)

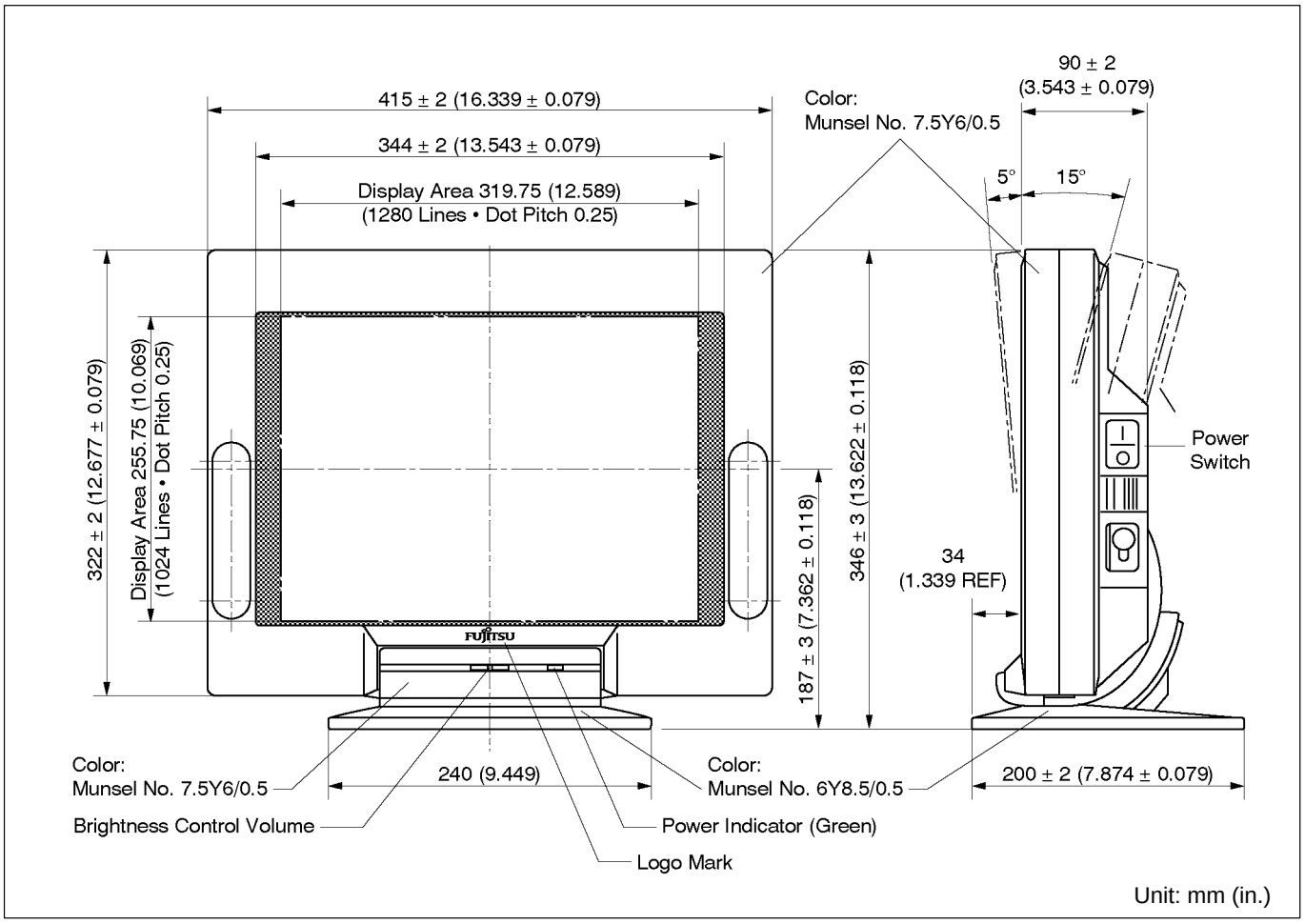
Physical Construction and Operation



PDP Construction and Operation

The figure above illustrates the structure of Fujitsu's AC-type plasma displays. X-electrodes (columns) and Y-electrodes (lines) are formed on two mating glass substrates and are subsequently covered with dielectric material. Each dielectric layer is then covered with a protective layer of magnesium-oxide (MgO) to prevent ion shock damage during discharge and to prolong its service life. This protective layer also emits secondary electrons during cell operation; this greatly improves the light-emission characteristics of the panel since MgO emits large quantities of electrons in the presence of an ionizing gas. Numerous spacers are placed between the glass substrates to maintain gap uniformity at about 0.1 mm over the entire panel. The spacers are so arranged that electrodes are positioned perpendicularly, while their peripheral parts are sealed in glass. The primary discharge gas used in the panel is neon, with a small quantity of xenon to stabilize discharge characteristics within the panel and improve emission.

External Dimensions

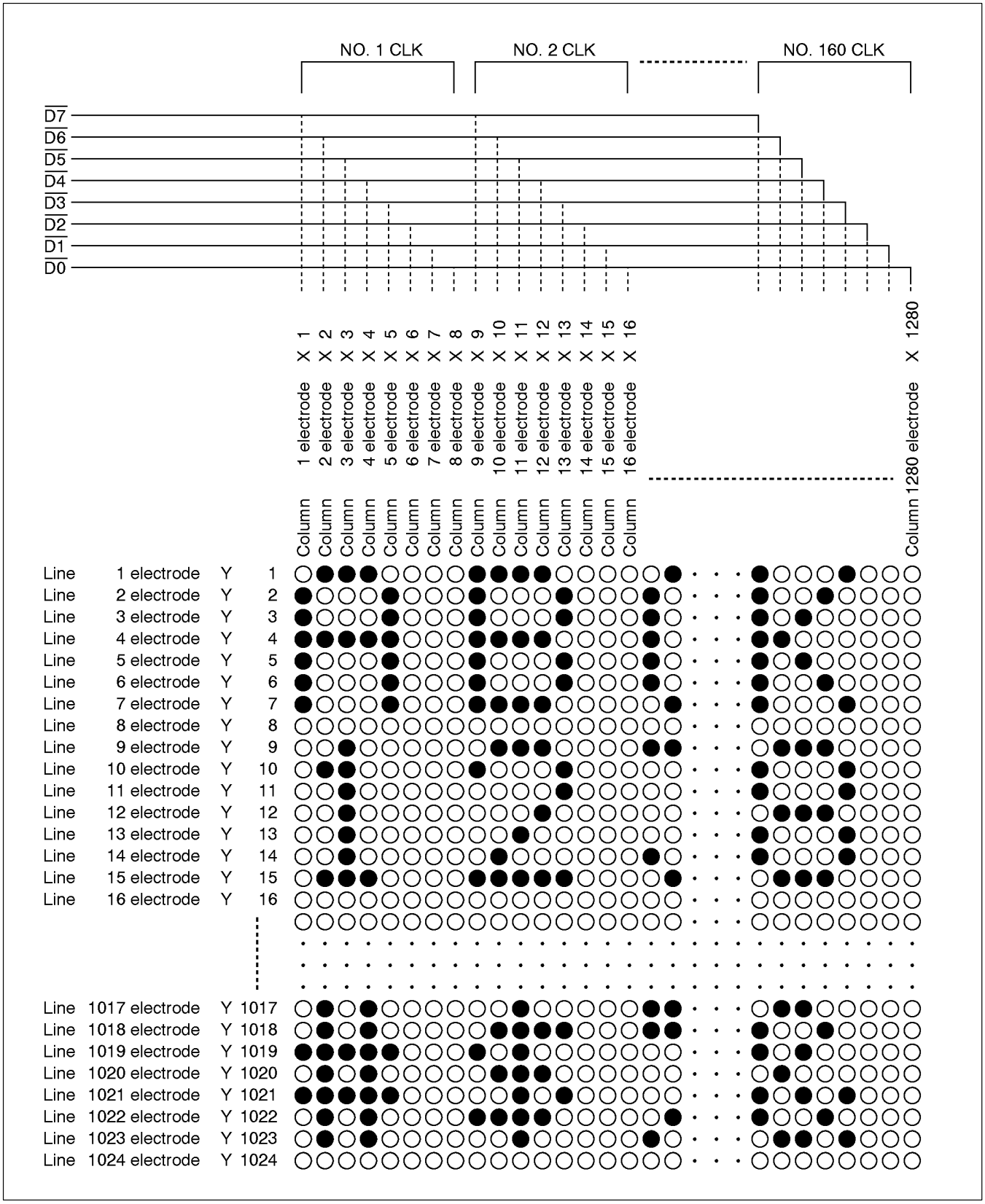


INTERFACE SIGNALS

Types of Signals

Signal Name	Symbol	I/O	Signal Line	Definition and Function
Display data	$\overline{D0}$ to $\overline{D7}$	I	8 lines	8-bit parallel display data. Logic L: On, H: Off The display position and relation between $\overline{D0}$ to $\overline{D7}$ is shown in the figure “Relationship Between Display Data and Display Dots” on the following page.
Clock	$\overline{CLK}$	I	1 line	Timing signal for display data. Display data are loaded at falling edge of this signal and transferred in sequence. 160 clock signals in one $\overline{H_{SYNC}}$ period.
Horizontal synchronous	$\overline{H_{SYNC}}$	I	1 line	Signal controlling the scanning timing and display time of each line electrode. Address increment to next line is done at the falling edge of $\overline{H_{SYNC}}$. 1024 or more $\overline{H_{SYNC}}$ signals in one $\overline{V_{SYNC}}$ period are required.
Vertical synchronous	$\overline{V_{SYNC}}$	I	1 line	Signal controlling the refresh speed of the screen. The scanning position returns to the first line electrode at the falling edge of $\overline{V_{SYNC}}$ signal.
Display enable	$\overline{DSPE}$	I	1 line	Signal controlling the display enable. Logic L: On, H: Off
Reserved	(res)	–	14 lines	Signal line is not permitted to be connected.

Relationship Between Display Data and Display Dots

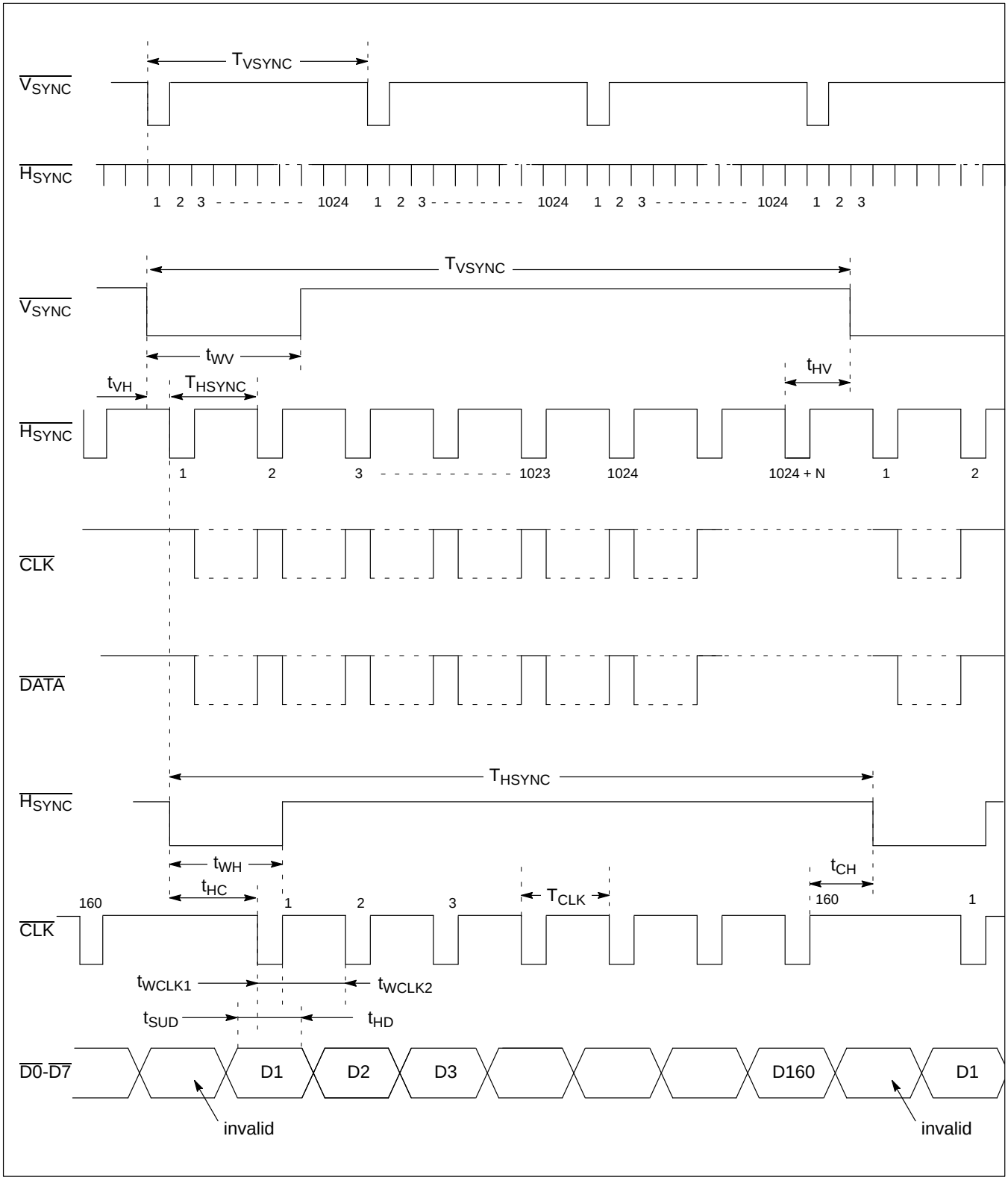


Interface Signal Timing

Symbol	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}	1024	(1067)	—	H	F_{VSYNC} = (30) Hz (Typ.)
t_{WV}	1	(3)	—	H	H = T_{HSYNC}
t_{VH}	1	(14)	—	µs	
t_{HV}	2	(17.25)	—	µs	
T_{HSYNC}	30.0	(31.25)	45	µs	T_{HSYNC} = (32) kHz (Typ.)
t_{WH}	1	(2)	—	µs	
t_{HC}	0.5	(2)	—	µs	
t_{CH}	0.1	(2.7)	—	µs	
T_{CLK}	166.7	—	—	ns	F_{CLK} = 6 MHz
t_{WCLK1}	83.3	—	—	ns	t_{WCLK1} + t_{WCLK2} = T_{CLK} DUTY = 50% (typ.)
t_{WCLK2}	83.3	—	—	ns	
t_{SUD}	40	—	—	ns	
t_{HD}	70	—	—	ns	

Note: Values in parentheses ( ) are the one example of timing condition.

Interface Signal Timing Chart



Notes: [1]N = 0, 1, 2 . . . .
[2]Number of CLKs in one $\overline{H_{SYNC}}$ period is 160. The continuous CLS is not permitted.

CONNECTOR PIN ASSIGNMENT

Pin Arrangement of Interface Signals (Display Side)

No.	Symbol	No.	Symbol	No.	Symbol	No.	Symbol
1	$\overline{D7}$	2	GND	26	(res)	27	GND
3	$\overline{D6}$	4	GND	28	(res)	29	GND
5	$\overline{D5}$	6	GND	30	(res)	31	(res)
7	$\overline{D4}$	8	GND	32	(res)	33	GND
9	$\overline{D3}$	10	GND	34	(res)	35	GND
11	$\overline{D2}$	12	GND	36	GND	37	GND
13	$\overline{D1}$	14	GND	38	(res)	39	GND
15	$\overline{D0}$	16	GND	40	(res)	41	GND
17	$\overline{CLK}$	18	GND	42	GND	43	GND
19	$\overline{H_{SYNC}}$	20	GND	44	GND	45	(res)
21	$\overline{V_{SYNC}}$	22	GND	46	(res)	47	(res)
23	$\overline{DSPE}$	24	GND	48	(res)	49	(res)
25	GND			50	(res)		

Notes: Applicable connector: FCN-235D050-G/C
(res): reserved

Section 8

Graphic Units with Touch Panels (optical touch panels plus units) — *At a Glance*

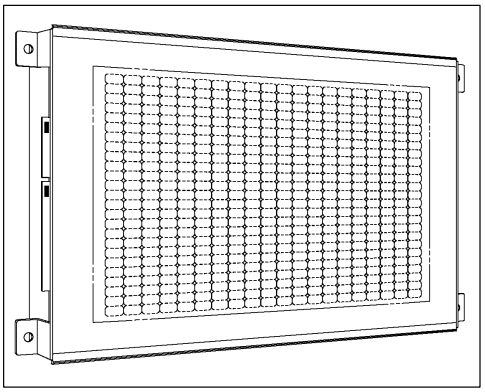
July 1992
Edition 1.0

FUJITSU

DATA SHEET

FTE8050BP
Plasma Display Unit with Touch Panel

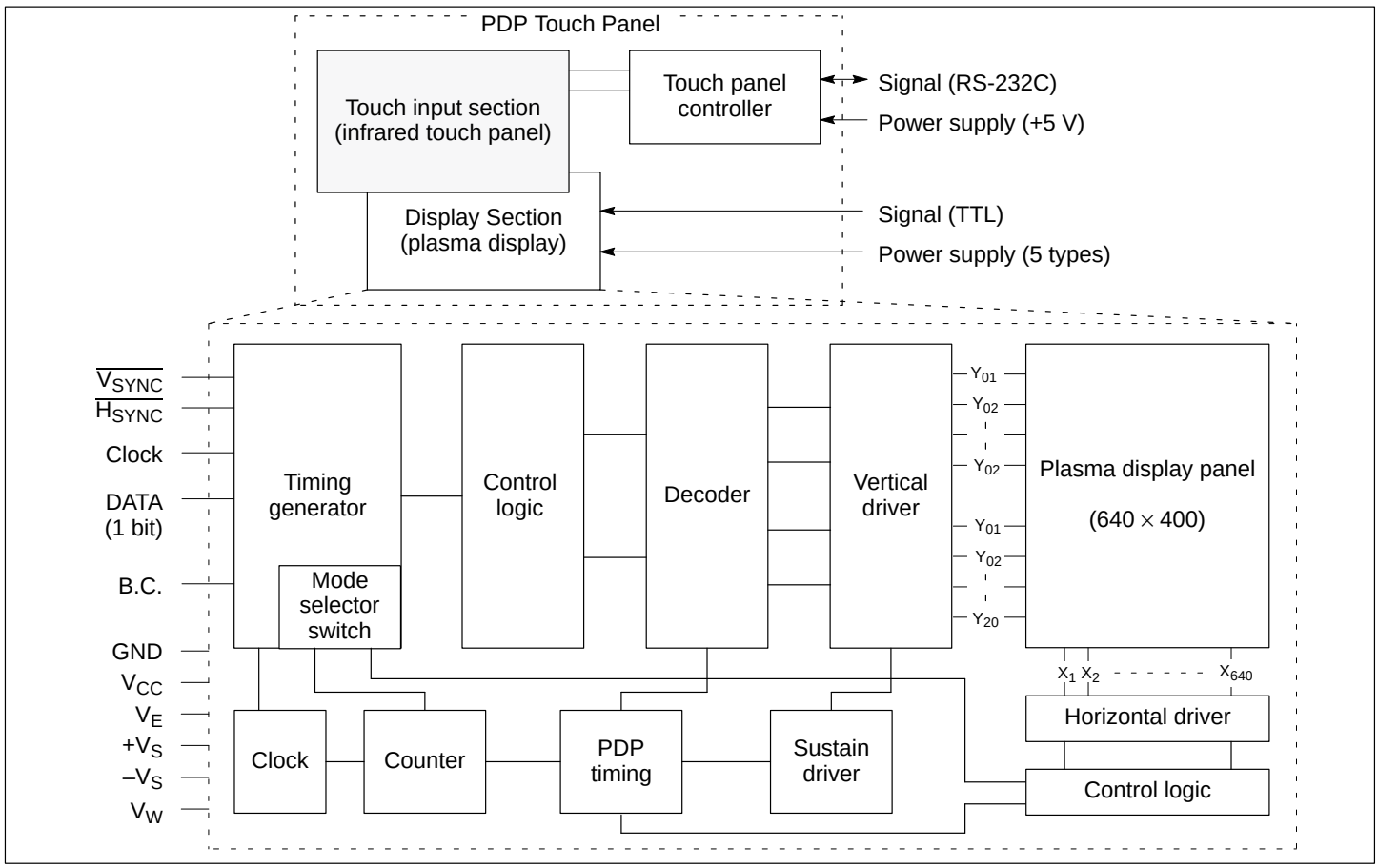
The FTE8050BP is a human-machine interface that provides both screen display and input functions in a single unit. The display unit employs a 640 × 400 dot AC memory plasma displey.



The touch panel controls a display screen which has a resolution of 3.18 mm × 3.18 mm and outputs via an RS-232C interface.

- Compact, thin construction and design
- Anti–glare filter with bezel
- Standard interface
- Integrated display & touch panel with no visible degradation in quality
- Applications:
  – Transaction terminals, ATMs and other banking applications
  –Medical equipment, ie CT scanners
  –Factory automation devices, ie NC controllers, robots, semiconductor fabrication equipment

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item		Symbol	Maximum rating
Display	Sustain driver	$+V_S$	+125 V
	Sustain driver	$-V_S$	–125 V
	Write driver	V_W	+180 V
	Line control driver	V_E	+45 V
	Logic	V_{CC}	+7 V
Touch panel	Touch panel driver	V_{DD}	+7 V

DC Characteristics

Item		Symbol	Minimum	Nominal	Maximum	Unit
Voltage	Input voltage (high level)	V_{IH}	2.4	–	5.25	V
	Input voltage (low level)	V_{IL}	–0.5	–	0.4	V
Current	Input current (high level) (V_I = 2.75 V, V_{CC} = 5.25 V)	I_{IL}	–	–	20	µA
	Input current (low level) V_I = 0.4 V, V_{CC} = 5.25 V	I_{IL}	–	–	–16	mA

Display and Touch Panel Power Supplies

Item		Symbol	Reference voltage (V)	Range (V)[1]	Allowable power fluctuation (maximum)	Noise and ripple (maximum)	Current (mA)	
							Standard[2]	Maximum[2]
Display	Sustain driver	$+V_S$	+95	±15	±2%	500 mV_{PP}	75	160
	Sustain driver	$-V_S$	–95	±15	±2%	500 mV_{PP}	75	160
	Write driver	V_W	+165	+10/–15	±2%	500 mV_{PP}	10	20
	Line control driver	V_E	+40	–	±5%	100 mVpp	100	150
	Logic	V_{CC}	+5	–	±5%	50 mVpp	350	450
Touch Panel	Touch Panel Driver	V_{DD}	+5	–	±5%	50 mVpp	350	400

Display Unit Output Power Supply

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
For V_S specification	Voltage	V_R[1]	With 1 kΩ load	0	–	2.5	
	Ripple and noise	V_{NRR}	With 1 kΩ load	–	–	±500	mV
	Stability (average)	–	With 1 kΩ load	–	–	±0.1	%
	Current (average)	I_{CC}	With 1 kΩ load	–	–	10	mA

MECHANICAL SPECIFICATIONS

Physical Specifications (Display)

Item	Value
Number of Display Dots	640 (H) × 400 (V) dots (256,000 dots)
Dot Pitch	0.33 (H) × 0.33 (V) mm (0.013 × 0.013 in.)
Dot Size	0.2 mm (0.008 in.)
Effective Screen Size	132 (V) × 211 (H) mm (5.197 × 8.307 in.)
Display Color	Neon orange
Dot Brightness	90 cd/m^2 (typical)
Contrast Ratio	20 : 1 minimum
Viewing Angle	120 degrees minimum
Brightness Unevenness	50% maximum
Weight	2.5 kg
External Dimensions	See External Dimensions figure

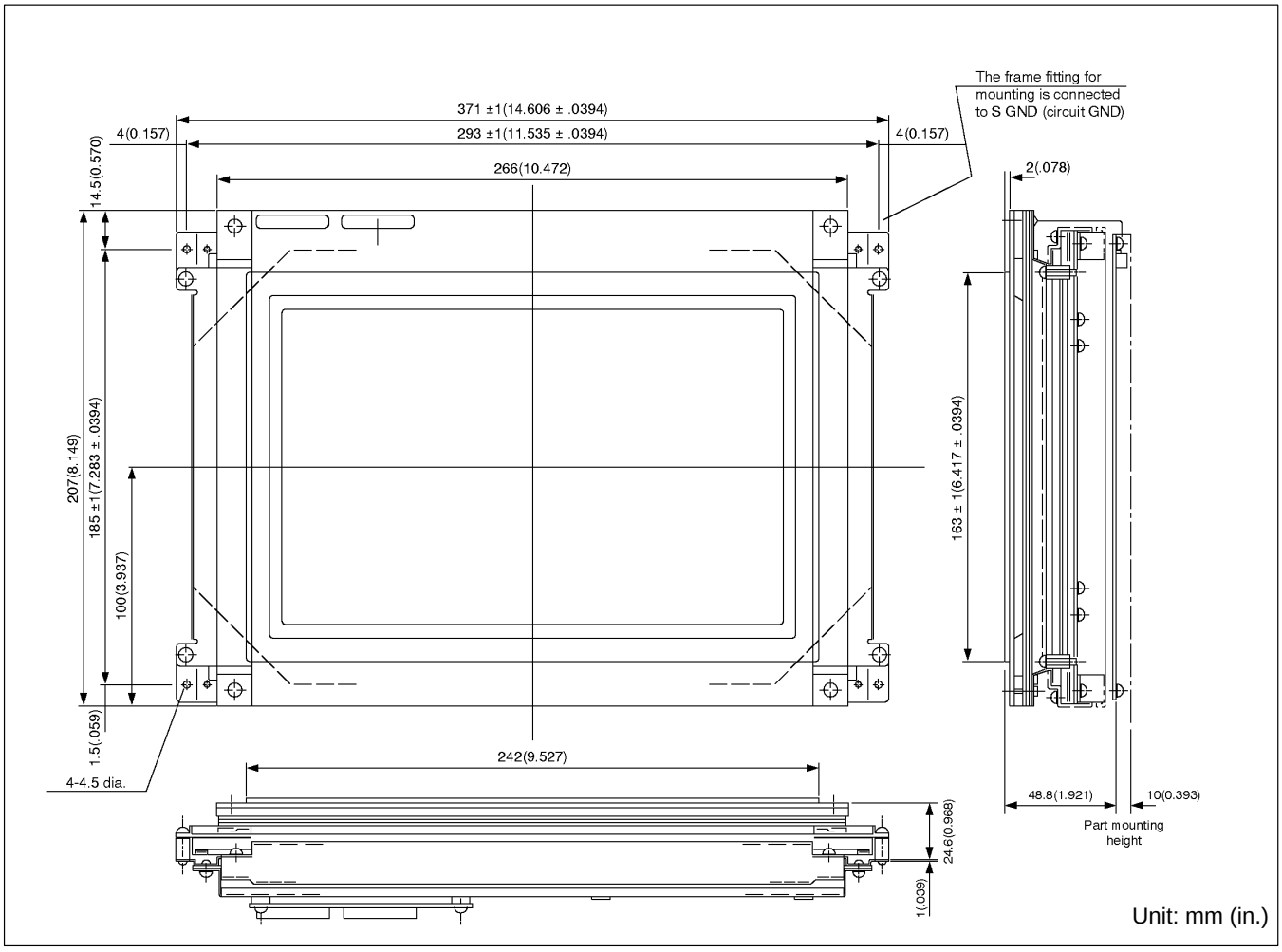
Physical Specifications (Touch Input)

Item	Value
Coordinate Detection Area	210 (H) × 133 (V) mm
Detection Resolution	3.18 (H) × 3.18 (V) mm
Coordinate Detection Time	50 ms (typical)
Surface Filter Treatment	Non-glare treatment
Coordinate Origin	Coordinates at the leftmost end of the detection area is (0,0)

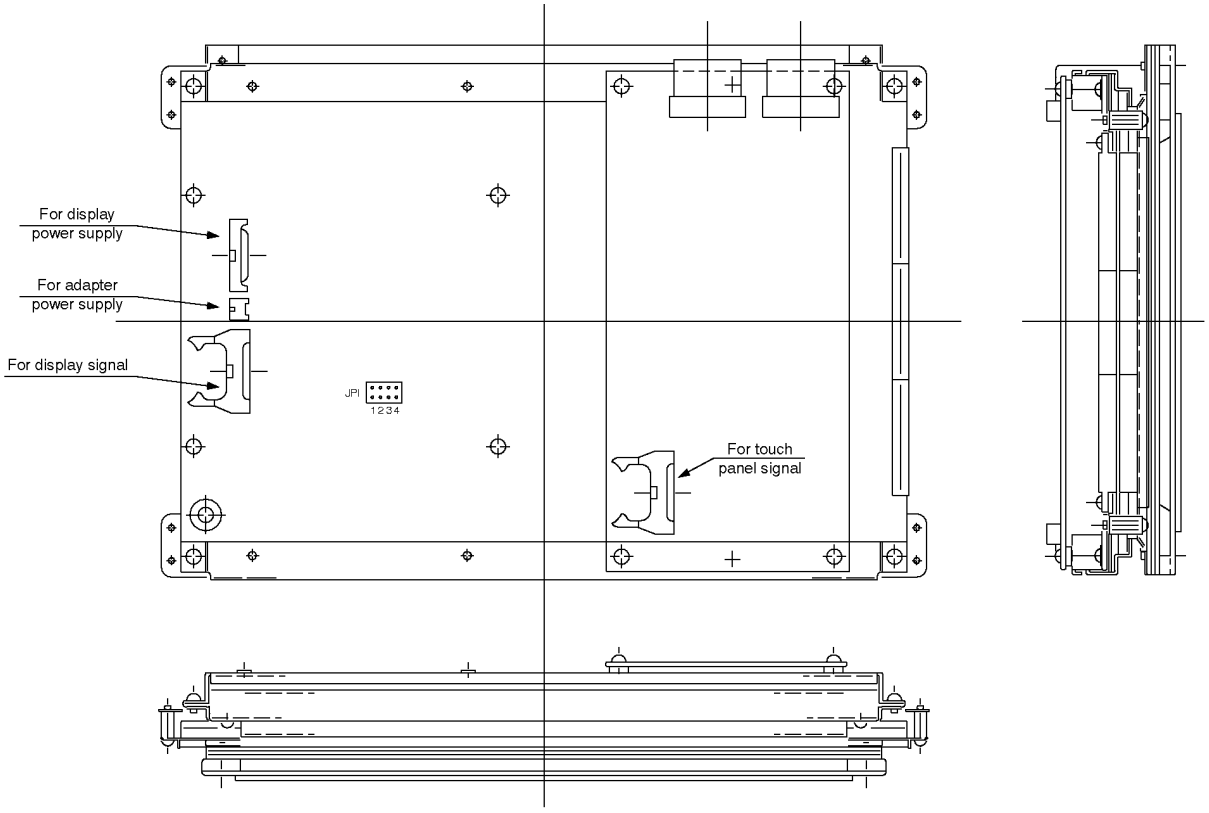
Performance Specifications

Item	Value
Operating Temperature	0 to 50 °C
Storage Temperature	–20 to +70 °C
Humidity	30 to 85% RH (no condensation)
Atmospheric Pressure Durability	Operation: 700 to 1114 hPa Non-operation: 340 to 1114 hPa
Vibration Acceleration: Frequency: Time:	 Operation: 0.5 G maximum Non-operation: 2 G maximum 10 to 55 Hz to 10 Hz/minute Operation: 20 minutes in X, Y, and Z direction Non-operation: 20 minutes in X, Y, and Z direction
Shock (at non-operation) Acceleration: Time:	 20 G max. in X, Y, and Z direction 11 ms maximum
Interference Fringes	When the center of the touch surface is pressed with a maximum force of 500 grams, no interference fringe shall be produced. If generated, the interference fringe shall disappear when pressure is removed.

External Dimensions (front)



External Dimensions (back)



Unit: mm (in.)

INTERFACE SIGNALS

Types of Signals

Signal name	Symbol	Number of lines	Signal definition and function
Data	DATA	1	Display data signal. H: Turns on, L: Turns off
Clock	CLK	1	Display data timing signal. Reads data on the rising edge of CLK. The number of clock pulses during the $\overline{H_{SYNC}}$ period is 640.
Horizontal synchronizing signal	$\overline{H_{SYNC}}$	1	Horizontal data strobe. Moves address to the next line electrode on the falling edge of $\overline{H_{SYNC}}$. The number of $\overline{H_{SYNC}}$ pulses required during the $\overline{V_{SYNC}}$ period depends on the display mode. 400 line mode: 402 + 2N 200 line mode: 202 + N The horizontal synchronous signal must be applied at all times.
Vertical synchronizing signal	$\overline{V_{SYNC}}$	1	Screen start timing signal. Moves address to the first-row electrode on the falling edge of $\overline{V_{SYNC}}$.
Brightness control	B.CONT	1	Brightness control signal. H: 100% L: 50%

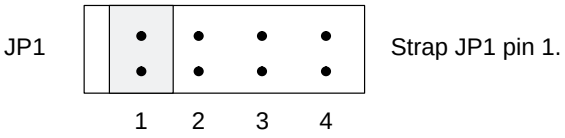
Display Mode Setting

640 × 400 dots	Non-interlaced mode (400-line mode). The standard mode enables a 400-line non-interlaced signal to be received and displayed.
640 × 200 dots	This mode enables operation with a 200-line non-interlaced signal and displays the 400-line unit in interlaced mode.

Interface Signal Timing Table (400 Line Mode)

Symbol	Min.	Nom.	Max.	Unit	Remarks
T_{VSYNC}	16.8	25		ms	Frame frequency: 40 Hz nominal
t_{WV}	2			µs	
t_{VH}	1			µs	
t_{HV}	2			µs	
T_{HSYNC}	40		47	µs	
t_{WM}	2			µs	
t_{MC}	1			µs	
t_{CM}	0.5			µs	
T_{CLK}	45	80	110	ns	
t_{WCLK1}	22	40		ns	
t_{WCLK2}	22	40		ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{SUD}	20	40		ns	
t_{MD}	22	40		ns	

Mode setting (JP1)

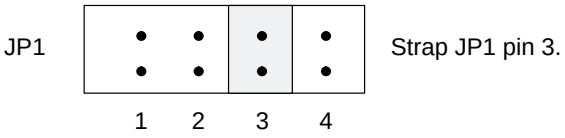


Strap JP1 pin 1.

Interface Signal Timing Table (200 Line Mode)

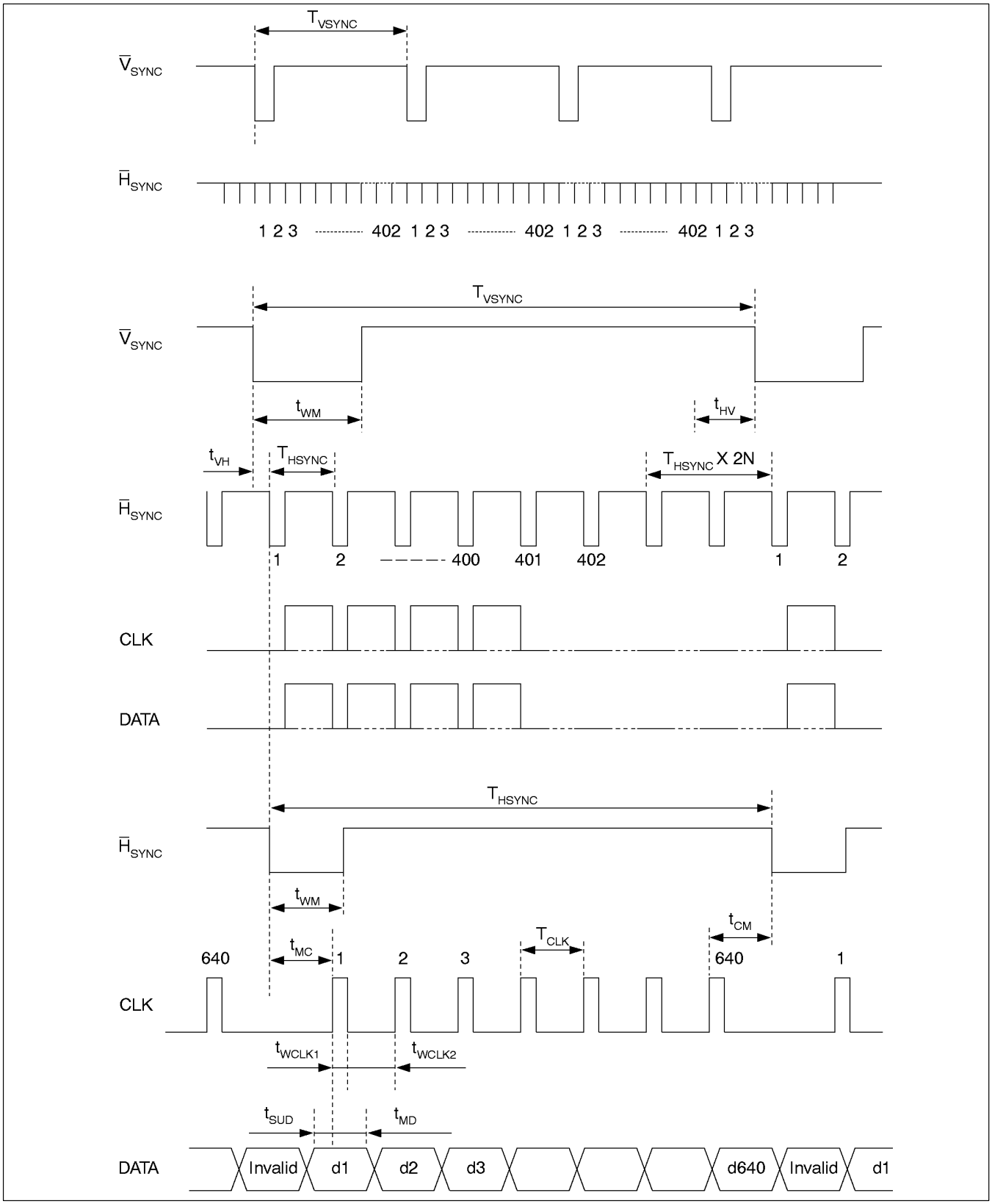
Symbol	Min.	Nom.	Max.	Unit	Remarks
T_{VSYNC}	16.8	25		ms	Frame frequency: 40 Hz nominal
t_{WV}	2			µs	
t_{VH}	1			µs	
t_{HV}	2			µs	
T_{HSYNC}	80		94	µs	
t_{WM}	2			µs	
t_{MC}	1			µs	
t_{CM}	0.5	3		µs	
T_{CLK}	45	80	110	ns	
t_{WCLK1}	22	40		ns	
t_{WCLK2}	22	40		ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{SUD}	20	40		ns	
t_{MD}	22	40		ns	

Mode setting (JP1)

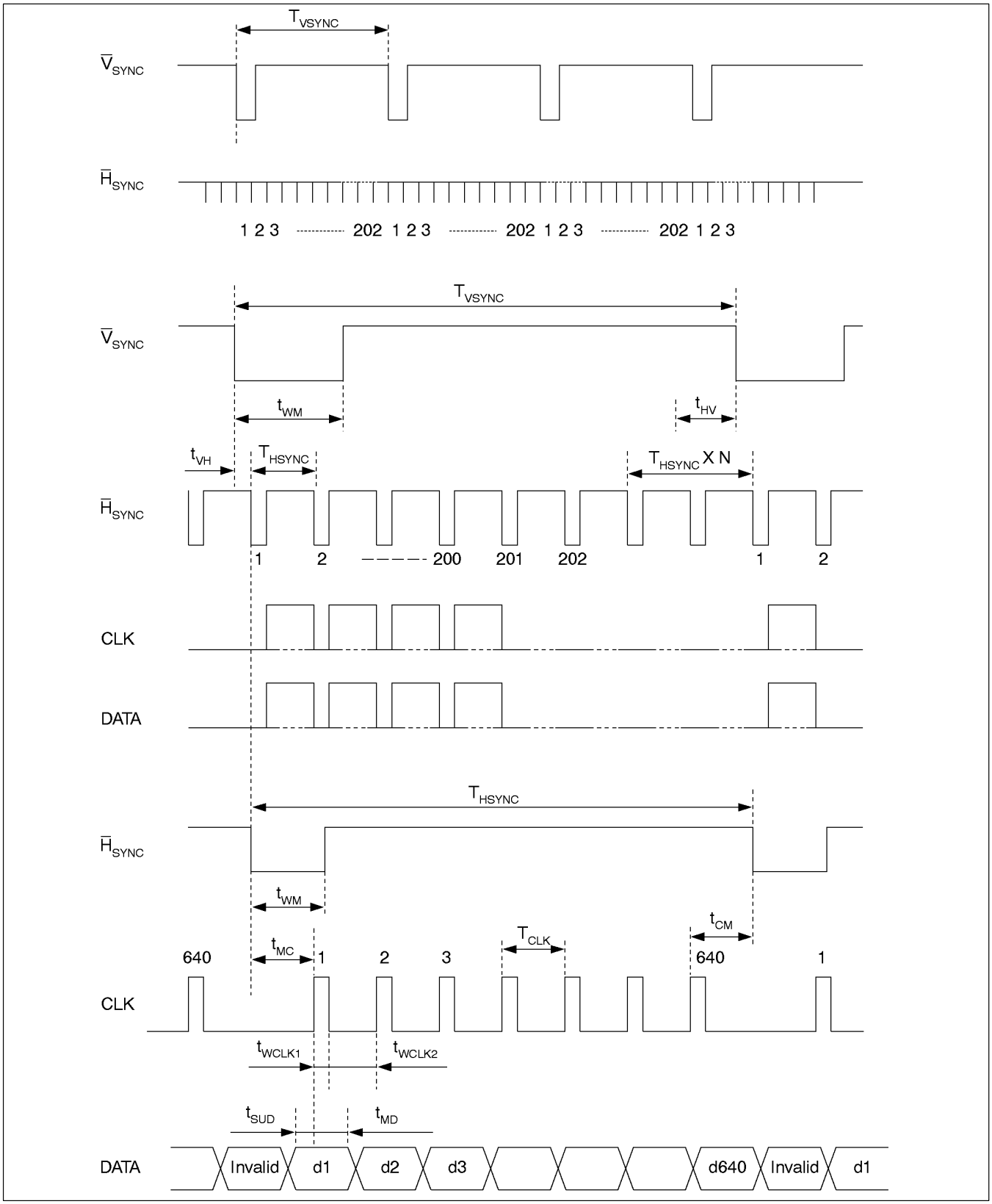


Strap JP1 pin 3.

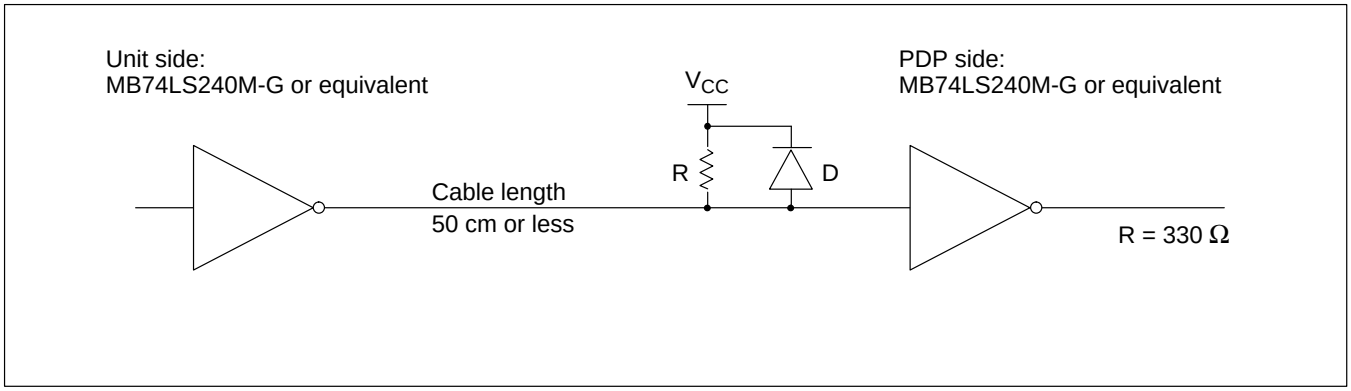
Interface Signal Timing Chart (400 Line Mode)



Interface Signal Timing Chart (200 Line Mode)



Interface Circuit (display)



TOUCH PANEL SPECIFICATIONS

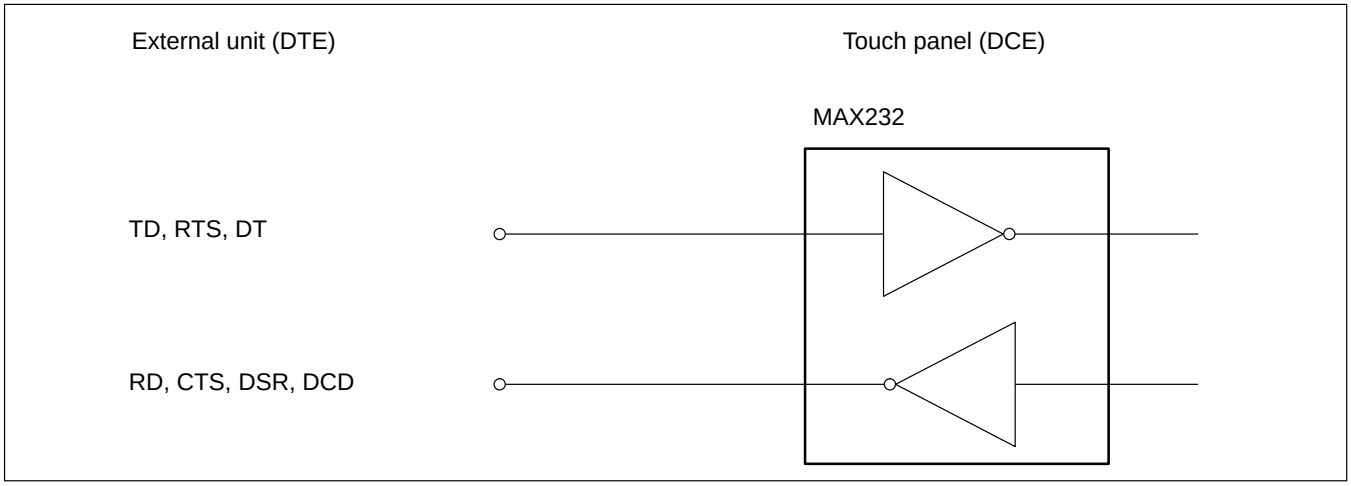
Touch Panel Interface Specification

Interface method	Conforms to EIA RS-232C
Baud rate	Rate can be automatically set to 300, 1200, 2400, 4800, 9600, or 19200 baud (start-stop).
Data configuration	Start bits (St): 1 bit Data (D0 to D7): 8 bits Parity (P): 1 bit, odd or even. Cannot be automatically set. Stop bits (SP): 2 bits

→

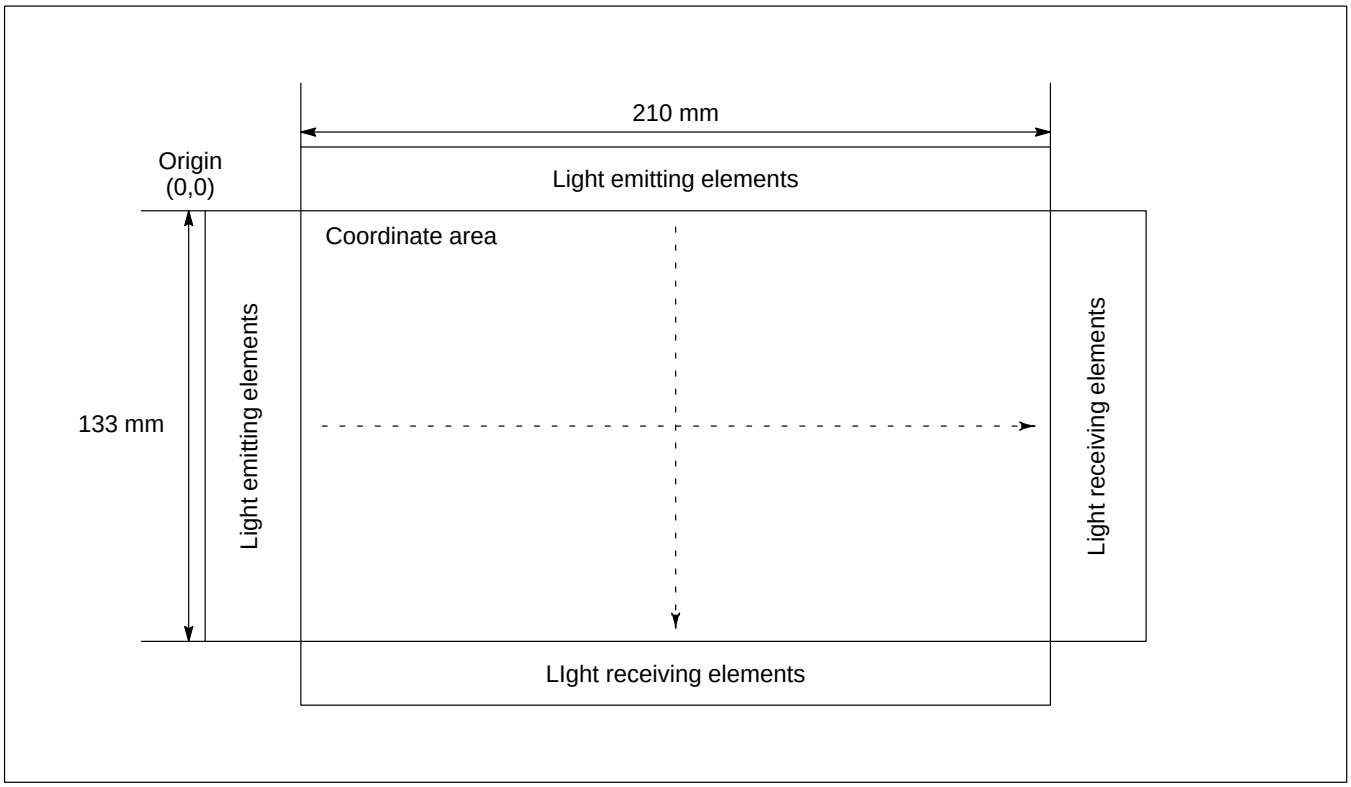
ST	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	P	SP	SP

Interface Circuit (touch panel)

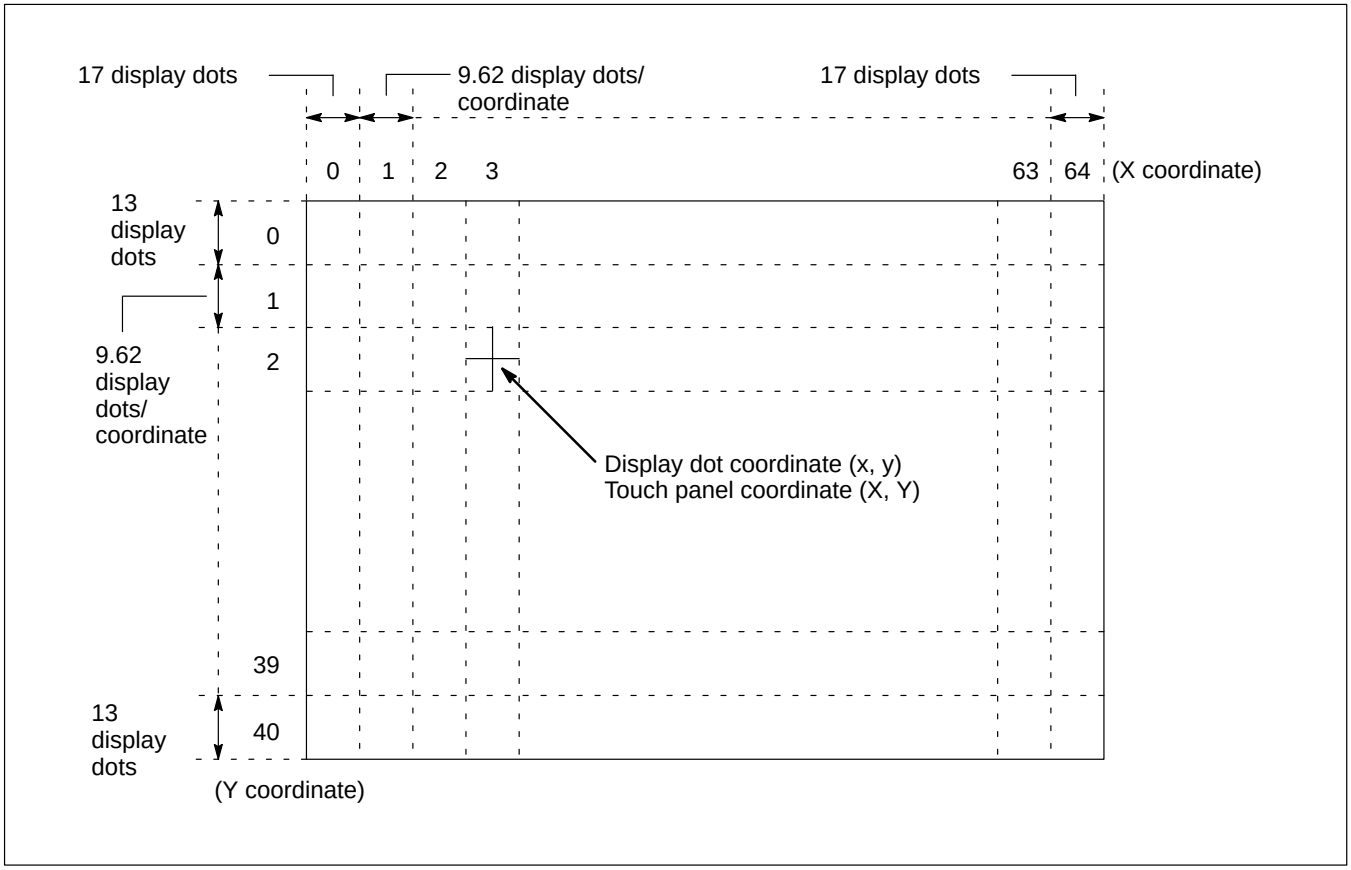


Coordinate Detection at Touch Panel

The coordinate input device of this touch panel has an effective touch area 210 mm wide and 133 mm high. It detects and converts to coordinates. The number of infrared ray emitting and receiving elements is 33 pairs wide and 21 pairs high. The origin is the upper left position.



Display Position and Coordinate Position



As shown in the above figure, when the display dot coordinate is (x, y), and the touch panel coordinate is (X, Y), their relationship can be represented by the following formulas:

$$x = 9.62 \times (X - 0.5) + 17 \quad \pm 6$$
$$y = 9.62 \times (Y - 0.5) + 13 \quad \pm 6$$

Touch panel fitting error

$$X = (x - 17)/9.62 + 0.5 \quad \pm 1$$
$$Y = (y - 13)/9.62 + 0.5 \quad \pm 1$$

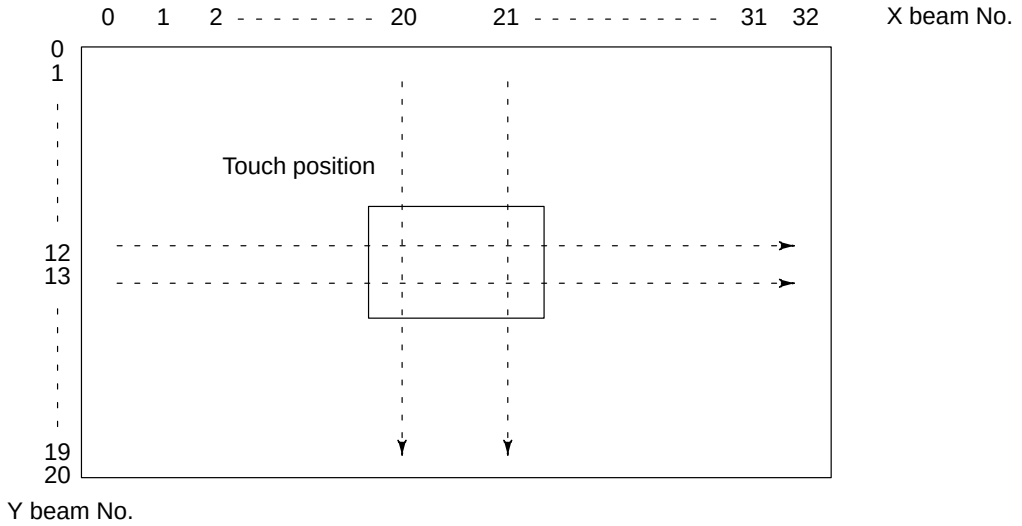
Touch panel fitting error

Round to the nearest unit

Detection Coordinate Transfer Mode

(1) Scan mode

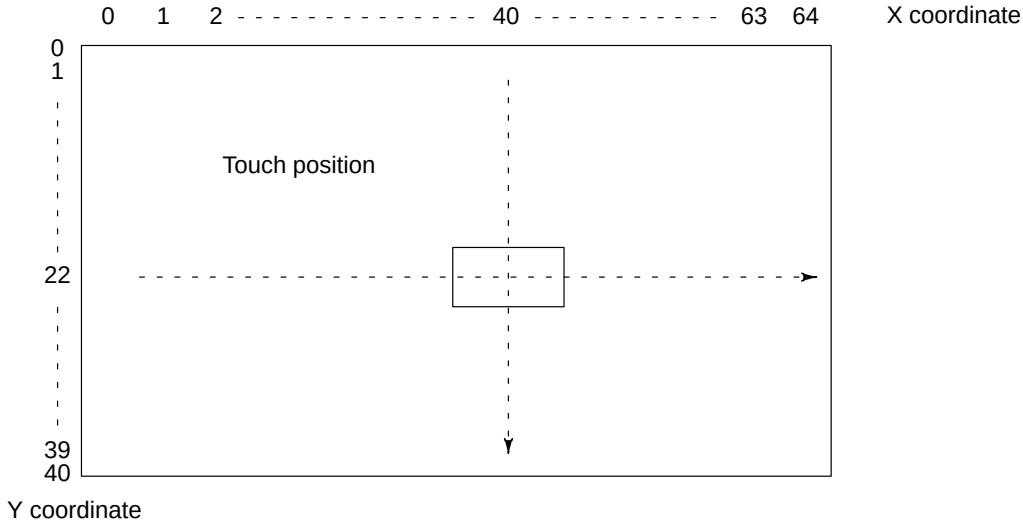
Assigns a beam number to each light-emitting element, and transfers the intercepted beam number.



X beam Nos. 20 and 21, and Y beam Nos. 12 and 13 are transferred.

(2) Coordinate mode

Divides the touch coordinate area into coordinates from X = 0 to 64 and Y = 0 to 40, and transfers the touch position coordinate.



X-coordinate 40 and Y-coordinate 22 are transferred.

Notes: 1. If a touch is broad and two or more beams are intercepted, the coordinate at the center of the touch is transferred.
2. If two or more beams are intercepted and they are not adjacent to each other (if touches occur at separate locations simultaneously), coordinates are not transferred, and a non-adjacent hit code is transferred.

Detection Operation Mode

Input point operation	Transfers the coordinates of the position touched first, and does not transfer the next coordinates until pressure is released.
Track operation	Transfers touch coordinates as long as the pressure is moving within the coordinate area. Does not transfer coordinates when pressure is released.
Continuous operation	Transfers touch coordinates as long as the pressure is within the coordinate area. Transfers touch coordinates even when pressure is released.
End point operation	Transfers coordinates of the point at which pressure is released.
Additional end point operation	In addition to input point operation, follow-up operation, and continuous operation, transfers the coordinates of the point at which pressure is released.

(1) Control commands

Item	Command	Code	Function
1	Reset	3C	Clears all buffers and resets the touch system.
2	Echo mode ON	20	Sends all the received data back to the host computer.
3	Echo mode OFF	21	Turns the echo mode OFF.
4	Touch system ON	2A	Starts touch system scanning.
5	Touch system OFF	2B	Stops touch system scanning.
6	Scan mode setting	22	Sets the detection coordinate mode to the scan mode.
7	Coordinate mode setting	23	Sets the detection coordinate mode to coordinate mode.
8	Input point operation	25	Sets the detection operation mode to input point operation.
9	Follow-up operation	26	Sets the detection operation mode to follow-up operation.
10	Continuous operation	27	Sets the detection operation mode to continuous operation.
11	End-point operation	28	Sets the detection operation mode to the end-point operation.
12	Additional end-point operation	29	Adds the end-point operation, as well as the operations in each detection operation mode. (This command is not used when the end-point operation is set.)
13	Status report	32	Reports the touch system status.
14	Configuration report	33	Reports the number of processors in the touch system.
15	Firmware version report	34	Reports the firmware ROM version.
16	Improper-beam analysis	36	Reports the opto-device status.
17	Frame size report	37	Reports the frame size.
18	Self-diagnostic report	3A	Executes self-diagnostics, and reports the status.
19	Clear	3D	Clears the touch report buffer.
20	Hardware flow control ON	41	Turns hardware handshaking on the serial interface on.
21	Hardware flow control OFF	42	Turns hardware handshaking on the serial interface off.
22	Data transfer ON	44	Enables data transfer.
23	Data transfer OFF	43	Inhibits data transfer.
24	Baud rate/parity reset	45	Return to the data transfer rate and parity setting mode.
25	Touch state report	47	Reports the operation setting status of the touch system.
26	Single report	46	Transfers reports to the host computer report-by-report.

Note: The code is hexadecimal.

(2) Baud rate/parity automatic setting

Shall be set by transferring code (0D) and the Reset command.

(2) Default set values

i. Touch system: OFF

ii. Detection coordinate transfer mode: Coordinate mode

iii. Detection operation mode: Follow-up operation

iv. Additional end-point operation: OFF

v. Data transfer: OFF

vi. Hardware flow control: OFF

CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-705Q016-AU/M

Pin No.	Signal Name	Symbol	Signal Direction		
			Touch Panel (DCE)		External Unit (DTE)
1	Transmit data	TD	←		
2	Receive data	RD	→		
3	Request to send	RTS	←		
4	Clear to send	CTS	→		
5	Data terminal ready	DTR	←		
6	Data set ready	DSR	→		
7	Data carrier detected	DCD	→		
8	Signal ground	SG			
9	Signal ground	SG			
10	Power ground	GND			
11	Power ground	GND			
12	Frame ground	FG			
13	+5 V	V_{DD}			
14	+5 V	V_{DD}			
15	+5 V	V_{DD}			
16	+5 V	V_{DD}			

Note: Mating connector: FCN-707B016-AU/B

Display Signal Connector

FCN-605Q016-G/S

Pin No.	Signal Name	Pin No.	Signal Name
1	N.C.	2	N.C.
3	N.C.	4	S.GND
5	DATA	6	S.GND
7	N.C.	8	S.GND
9	$\overline{H_{SYNC}}$	10	S.GND
11	$\overline{V_{SYNC}}$	12	S.GND
13	B.CONT	14	S.GND
15	CLK	16	S.GND

Notes: Mating connector: FCN-607B016-G/D, no strain relief
Leave N.C. unconnected.

Power Supply Connector

Pin No.	Symbol
1	V_{CC} (Logic)
2	GND(L) (for V_{CC})
3	$-V_S$ (Sustain driver)
4	GND(H) (for $+V_S$, V_W, V_E)
5	$+V_S$ (Sustain driver)
6	V_W (Write driver)
7	N.C.
8	V_E (Line control driver)
9	N.C.

Adaptable connectors: FCN-813J009-A, housing
FCN-813J-T/Q, contact (for manual operation)
FCN-813J-T/R, contact (for automatic device)

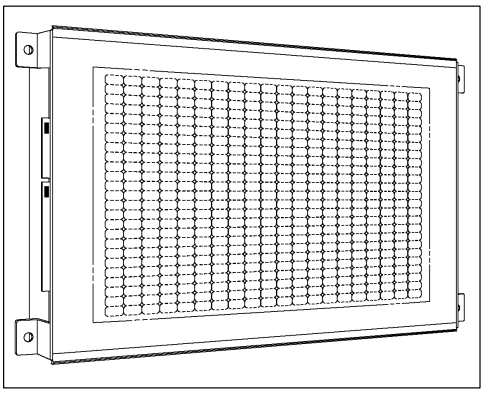
July 1992
Edition 1.0

FUJITSU

DATA SHEET

FTE8050BPE
Plasma Display Unit with Touch Panel

The FTE8050BPE plasma display unit is a human-machine interface that provides both screen display and input functions in a single unit. This unit consists of a 9-inch plasma display with an integrated optical touch panel.

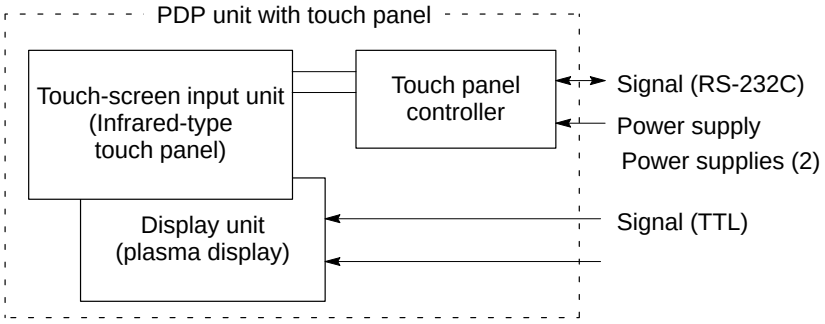


The display unit employs a 640 × 400 dot AC memory plasma display with high brightness, high contrast, and a wide viewing angle. The optical touch panel has its own internal controller, with coordinate sensing resolution of 3.025 × 3.550 mm (0.12 × 0.14 in.) for high-resolution, touch-input applications.

A built-in anti-glare filter eliminates reflection from external light sources. The exclusive bezel design protects the light-sensing and emission elements from dust and other contaminants.

- Integrated display and touch panel with no visible degradation in display quality
- Compact, thin design
- Anti-glare filter with bezel
- Compact, thin construction
- Standard interface
- Applications:
  – Transaction terminals, ATM terminals, and other banking and securities applications
  – Factory automation devices such as Numeric Control (NC) controllers, robots, programmable controllers, injection molding machines, or semiconductor fabrication equipment
  – Many types of automated ticket vending machines
  – Medical equipment, such as CT scanners

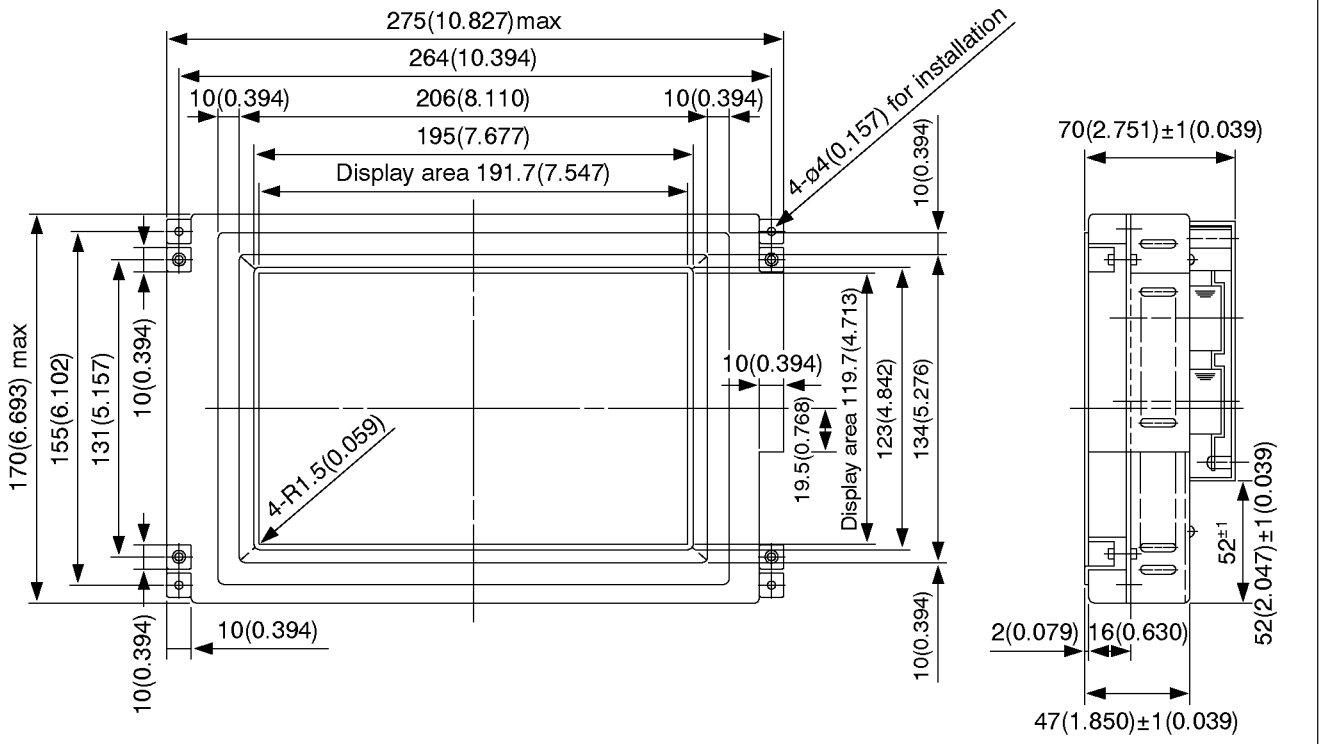
BLOCK DIAGRAM



SPECIFICATIONS

Item		Specification
Display Unit	Display Capacity	640 (horizontal) x 400 (vertical) dots
	Dot Pitch	0.3 (horizontal) x 0.3 (vertical) mm (0.012 × 0.012 in.)
	Dot Size	0.2 mm (approx.) (0.008 in.)
	Effective Display Size	191.7 (horizontal) × 119.7 (vertical) mm (7.55 × 4.71 in.)
	Display Color	Neon orange
	Gray Scale	4–level (approx. 100, 67, 33, and 0%)
	Brightness	Spot: 90 cd/m^2 (typical) Plane: 11 cd/m^2 (typical)
	Contrast	1 : 20 minimum
	Viewing Angle	120° or more (80 degrees at periphery)
	Interface	CRT conformity TTL
	Brightness Adjustment	0 to 100% by BC signal
	Power Supply	2 supplies (5V, 95V)
	Power Consumption	16W (typical)
Touch Input Unit	Coordinate Sensing Range	Infrared sensing and emission element
	Coordinate Sensing Range	192 (horizontal) × 120 (vertical) mm (7.56 × 4.72 in.)
	Sensing Resolution	3.025 (horizontal) × 3.550 (vertical) mm (0.12 × 0.14 in.)
	Coordinate Sensing Interval	50 ms (typical)
	Screen Filter	Non-glare filter
	Interface	RS-232C conformity Data format: 1 start bit, 8 data bits, 1 parity bit, 2 stop bits Baud rates: 300, 1200, 2400, 4800, 9600, 19200 bps (automatic setting)
	Power Supply	+5V (±5%)
	Power Consumption	400 mA (maximum)
Environment temperature		0 to 50°C (changes within 11.5°C/min.)
External Dimensions		257 (W) × 170 (H) × 77 (D) mm (10.1 in. × 6.7 in. × 3.0 in.)
Weight		Approximately 1.9 kg (4.2 lbs.)

External Dimensions



CONNECTOR PIN ASSIGNMENT

Signal Connector

(Connector used: FCN-605Q026-G/S)

Pin No.	Signal Name	Pin No.	Signal Name
1	$\overline{V_{SYNC}}$	2	S. GND
3	$\overline{H_{SYNC}}$	4	S. GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S. GND
15	D0	16	S. GND
17	D1	18	S. GND
19	CLK	20	S. GND
21	B.C.	22	N.C.
23	N.C.	24	N.C.
25	N.C. (V_{CC})	26	N.C. (V_{CC})

Combination connector: FCN-607B026-G/D

Power Supply Connector

(Connector used: FCN-814P-009TA)

Pin No.	Signal Name
1	V_{CC}
2	GND
3	N.C.
4	GND
5	V_E
6	N.C.
7	N.C.
8	GND
9	V_R

Combination connector housing: FCN-813J009-A
Contact: FCN-813J-T/Q

Touch Panel Unit Signal

(Connector: FCN-705Q016 AU/M)

Pin No.	Signal Name	Symbol	Pin No.	Signal Name	Symbol
1	Transmit data	TD	2	Receive data	RD
3	Request to send	RTS	4	Clear to send	CTS
5	Data terminal ready	DTR	6	Data set ready	DSR
7	Data carrier detect	DCD	8	Signal ground	SG
9	Signal ground	SG	10	Power ground	GND
11	Power ground	GND	12	Frame ground	FG
13	+5 V	V_{DD}	14	+5 V	V_{DD}
15	+5 V	V_{DD}	16	+5 V	V_{DD}

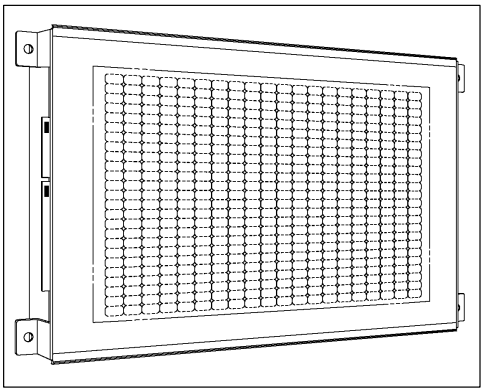
June 1992
Edition 1.0

FUJITSU

DATA SHEET

FTE8060BPC
Plasma Display Unit with Touch Panel

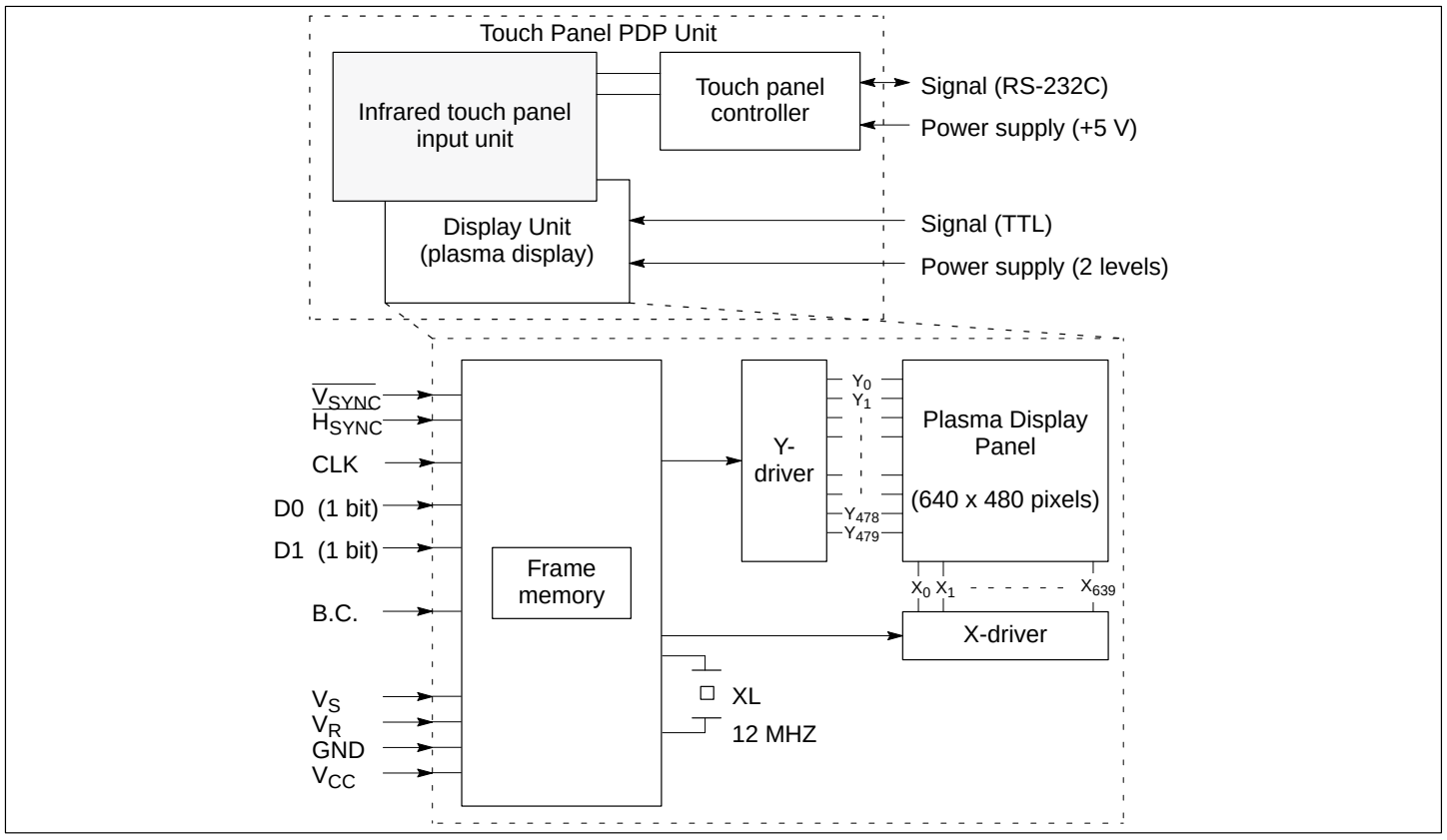
The FTE8060BPC is a human-machine interface that provides both screen display and input functions. The display provides clear images by employing an 11.4-inch display area with 640 x 480-dot resolution.



The display unit can be connected using a standard cathode ray tube controller (CRTC) and the touch panel employs an RS-232C interface.

- Integrated display and touch panel
- Clear, bright display
- Long display life without brightness deterioration
- Compact, thin construction
- Standard interface
- Applications:
  - – Medical equipment, measuring instruments, and analyzers
  - – Factory automation devices, such as Numeric Control (NC) controllers, robots, programmable controllers, equipment for automatic installation of electronic components, semiconductor/LCD manufacturing equipment, and projection formation equipment
  - – Various types of ticket issuing terminals
  - – Transaction terminals, such as ATM machines, and other banking and securities applications
  - – Distribution terminals, such as point-of-sale (POS) terminals

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter		Symbol	Absolute ratings
Display unit	For sustain driver	V_S	+125 V
	For logic	V_{CC}	+7 V
Touch panel unit	For touch panel driver	V_{CC}	+5.5 V

Display Unit DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	–	2.0	–	5.25	V
Low-level input voltage	V_{IL}	–	–0.5	–	0.8	V
High-level input current	I_{IH}	V_I = 2.75 V, V_{CC} = 5.25 V	–	–	20	µA
Low-level input current	I_{IH}	V_I = 0.4 V, V_{CC} = 5.25 V	–	–	–16	mA

Touch Panel DC Characteristics

Parameter	Symbol	Reference voltage (V)	Tolerance to power supply fluctuation	Ripple and noise (maximum limit)	Current	
					Typical	Maximum
For touch panel driver	V_{DD}	+5	±5%	100 mV_{PP}	–	650 mA

Display Unit Input Power Supply

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Display	Supply Voltage[1,2]	V_S	Variable	88	95	100.5	V
	Ripple and noise	V_{NRS}	Determined by load resistance	—	—	500	mV
	Stability (average)	—	Determined by load resistance	—	—	±1.5	%
	Setting precision	—	Deviation from Expression 1	—	—	±0.5	%
	Stability (peak)	—	(I_S = 2A)	—	—	–5	%
	Current (average)[3,4]	I_S	Horizontal cycle = 42 µs/line	50	200	400	mA
	Current (peak)	I_{SP}	Width shall be 1 µs with I_{SP} = 1A at a cycle of 5 to 8 µs	0.5	—	2	A
Logic	Supply Voltage	V_{CC}	May be fixed	4.75	5.0	5.25	V
	Ripple and noise	V_{NRS}	Determined by load resistance	—	—	200	mV
	Stability (average)	—	Determined by load resistance	—	—	±5	%
	Current (average)	I_{CC}		150	250	500	mA

Notes: [1] A power supply variable from 88 V to 100.5 V is required, because the display voltage V_S differs with each unit.
[2] The setting of V_S is described on a label attached to each unit. V_S can be automatically set by using the reference voltage V_R. The relationship between V_S and V_R is explained in the note for the Display Unit Output Power Supply table.
[3] The following conditions are assumed for the value of current I_S.
Minimum: Display ratio (lighting ratio) = 0%
Typical: Display ratio (lighting ratio) = 33% (“B” displayed on the entire screen)
Maximum: Display ratio (lighting ratio) = 100%
[4] Current I_S (and brightness) is inversely proportional to the horizontal frequency. A horizontal frequency of 31 µs/line is assumed for the above values.
[5] I_S (for display) is 0 mA (no load) under the following conditions:
V_{CC} is not supplied,
Two frames after V_{CC} are supplied. (After three vertical pulses are input, operation starts.)
There is no horizontal synchronization signal input.
There is no clock input.

Display Unit Output Power Supply

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
For V_S specification	Voltage	V_R[1]	With 1 kΩ load	0	–	2.5	V
	Ripple and noise	V_{NRR}	With 1 kΩ load	–	–	±500	mV
	Stability (average)	–	With 1 kΩ load	–	–	±0.1	%
	Current (average)	I_{CC}	With 1 kΩ load	–	–	10	mA

Note: [1] V_R is related to V_S as follows:
$V_S = 88 + 5 \times V_R$
Example: When V_S = 93 V, V_R = 1.0 V

MECHANICAL SPECIFICATIONS

Physical Specifications (Display)

Item		Value
Number of Display Dots		640 (H) × 480 (V) dots (307,200 dots)
Dot Pitch		0.36 (H) × 0.36 (V) mm (0.014 × 0.014 in.)
Dot Size		0.2 mm (0.008 in.)
Effective Screen Size		230.04 (H) × 172.44 (V) mm (9.057 × 6.789 in.)
Gray Scale		4 levels (approximately 100%, 67%, 33%, and 0%)
Display Color		Neon orange
Brightness	peak	88 cd/m^2 typical
	average	12 cd/m^2 typical
Brightness Control		Variable from 0 to 100% (using BC signal)
Contrast Ratio		20 : 1 minimum
Viewing Angle		120 degrees minimum
Brightness Unevenness		50% maximum (the average brightness variation between any two points 10 mm apart shall not exceed 30%)
Weight		Approximately 2 kg
External Dimensions		See External Dimensions Figure

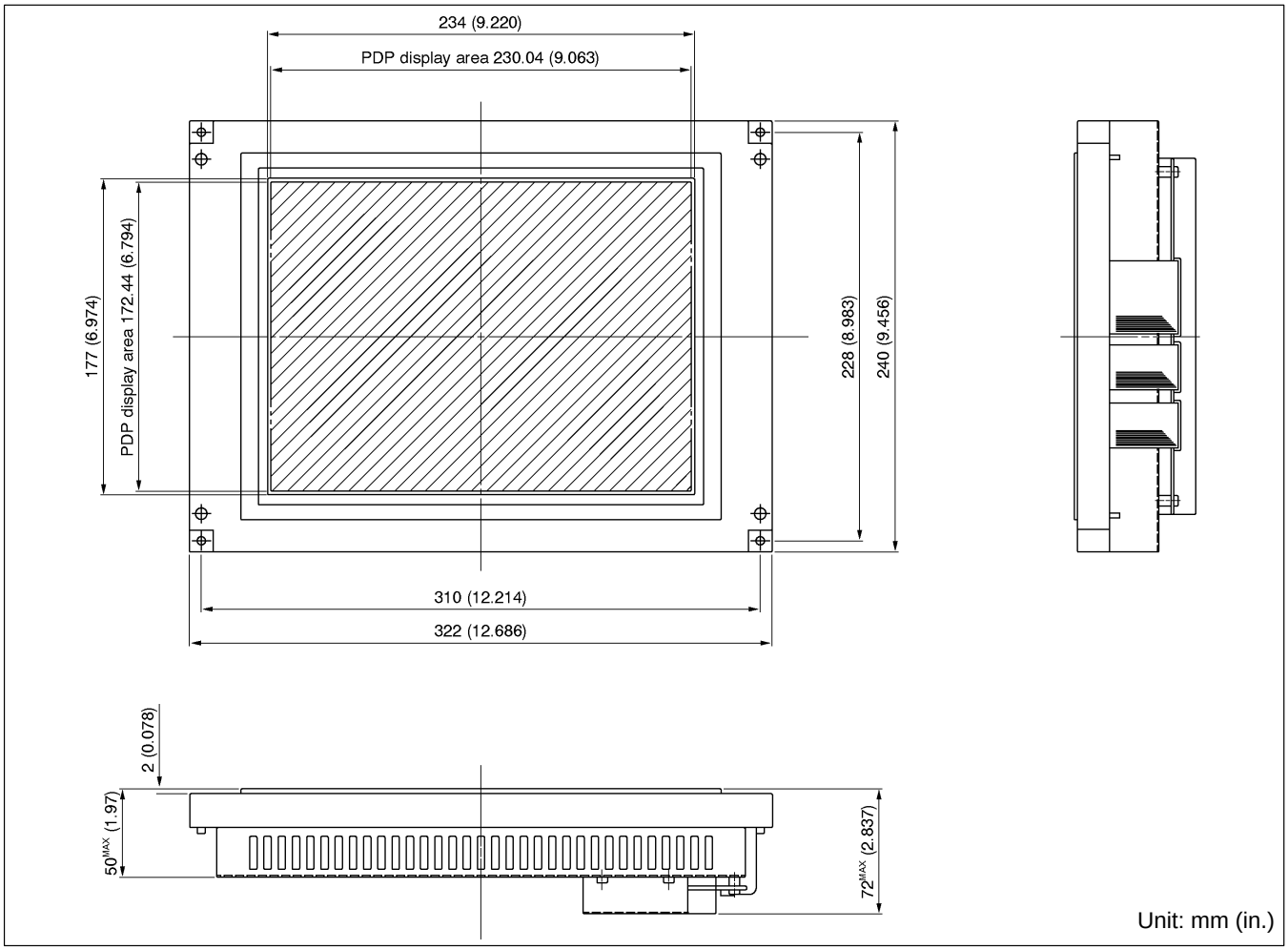
Physical Specifications (Touch Input)

Item	Value
Number of Elements	42 (H) × 26 (V)
Detection Area	231 (H) × 171.6 (V) mm (9.095 × 6.756 in.)
Resolution	2.75 (H) × 3.3 (V) mm (0.108 × 0.130 in.)
Minimum Stylus Size	9.2 mm (0.362 in.)
Surface Filter Treatment	Non-glare treatment
Origin of Coordinates	The coordinates at the left end of the detection shall be (0,0)

Performance Specifications

Item	Value
Operating Temperature	0 to 50°C
Storage Temperature	–20 to +70°C
Humidity	30 to 85% RH (no condensation)
Atmospheric Pressure Durability	Operation: 700 to 1114 hPa Non-operation: 340 to 1114 hPa
Vibration Acceleration: Frequency: Time:	 Operation: 0.5 G maximum Non-operation: 2 G maximum 10 to 55 Hz to 10 Hz/minute Operation: 20 minutes in X, Y, and Z direction Non-operation: 20 minutes in X, Y, and Z direction
Shock (at non-operation) Acceleration: Time:	 20 G max. in X, Y, and Z direction 11 ms maximum
Press force	1 kg maximum at touch panel surface

External Dimensions



INTERFACE SIGNALS (DISPLAY)

Types of Signals

<table>
<tr><th>Name of Signal</th><th>Symbol</th><th>Data Line</th><th>Definition and Function</th></tr>
<tr><td>Data</td><td>D0
D1</td><td>2</td><td>Display data signal.
Logic: High: Lit, Low: Not lit
Relationship Between Data and Gray Scale Level[1]
<table>
<tr><th>D1</th><th>D0</th><th>Gray scale (relative value)</th></tr>
<tr><td>0</td><td>0</td><td>Dark (0)</td></tr>
<tr><td>0</td><td>1</td><td>Low (33%)</td></tr>
<tr><td>1</td><td>0</td><td>Medium (67%)</td></tr>
<tr><td>1</td><td>1</td><td>High (100%)</td></tr>
</table></td></tr>
<tr><td>Clock</td><td>CLK</td><td>1</td><td>Display data timing signal. Data is read at the rising edge of the clock.
Note: There are 640 clocks during the $\overline{H_{SYNC}}$ period.</td></tr>
<tr><td>Horizontal Synchronization</td><td>$\overline{H_{SYNC}}$</td><td>1</td><td>Signal which determines the data period for one horizontal line. The address shifts to the electrode of the next line at the falling edge of $\overline{H_{SYNC}}$. The number of $\overline{H_{SYNC}}$ signals required for the $\overline{V_{SYNC}}$ period is 402 + 2N.
Note: Always enter horizontal synchronization signals at the same intervals.</td></tr>
<tr><td>Vertical Synchronization</td><td>$\overline{V_{SYNC}}$</td><td>1</td><td>Timing signal to control screen start. The address shifts to the electrode of the first column on the falling edge of $\overline{V_{SYNC}}$.</td></tr>
<tr><td>Brightness Control</td><td>B.C.</td><td>1</td><td>Brightness control signal.
High: Lit, Low: Not lit</td></tr>
</table>

Note: [1]The gray scale levels (relative values) are defined by the following expressions:

Low $B_L = a/V \times 100\%$
Medium $B_M = (V–a)/V \times 100\%$
High $B_H = 1 \times 100\%$

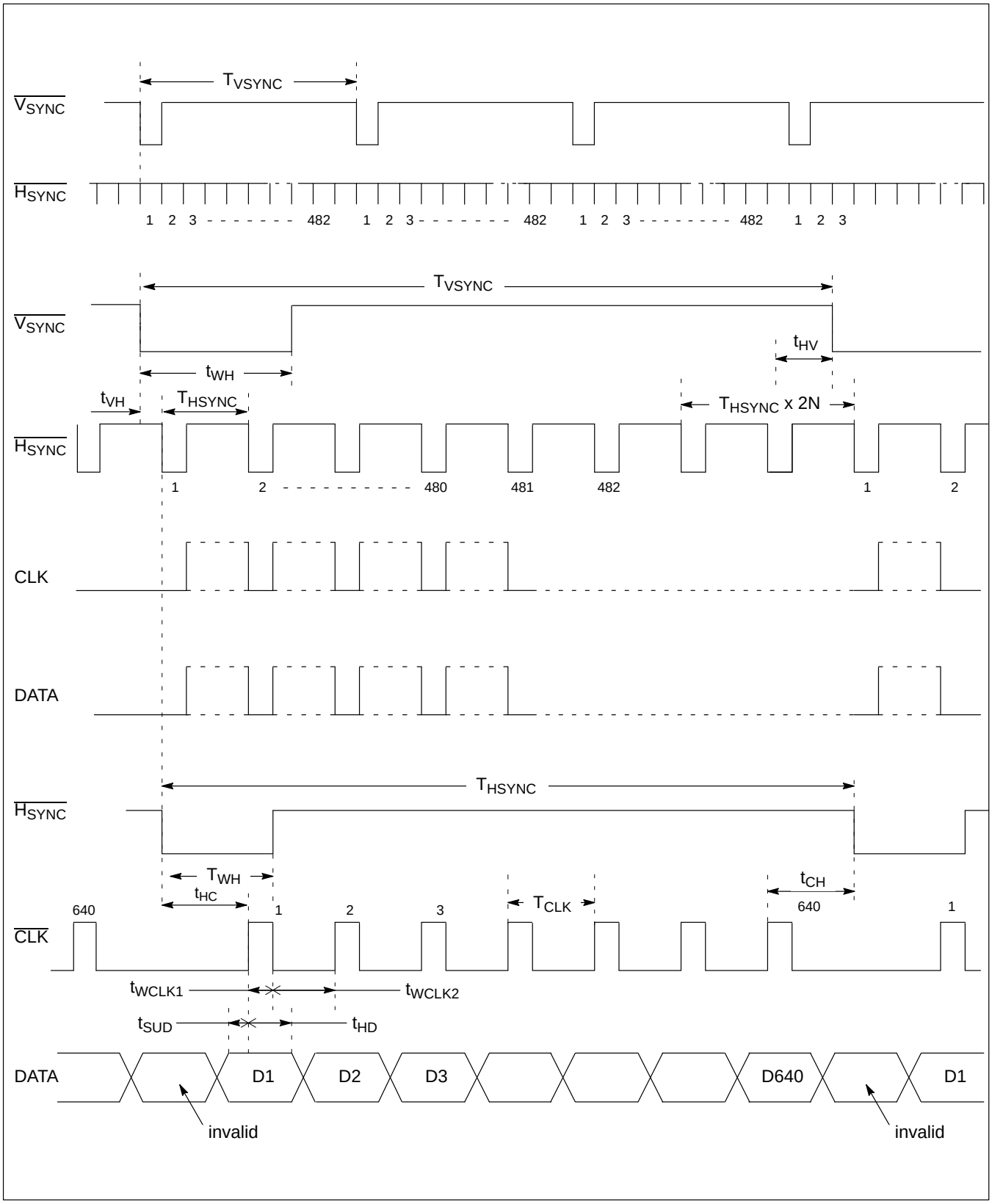
a: Internal unit constant, set to 169
V: Number of horizontal cycles in a vertical period

Interface Signal Timing Table

Symbol	Min.	Typ.	Max.	Unit	Remarks
T_{VSYNC}		16.7	20	ms	Frame Frequency: Standard 60 Hz
t_{WV}	—	—	—		This time period shall exceed one $\overline{H_{SYNC}}$ cycle.
t_{VH}	1	—	—	µs	
t_{HV}	2	—	—	µs	
T_{HSYNC}	31	—	—	µs	
t_{WH}	2	5	—	µs	
t_{HC}	2	—	—	µs	
t_{CH}	2	3	—	µs	
T_{CLK}	44	—	—	ns	
t_{WCLK1}	22	—	—	ns	
t_{WCLK2}	22	—	—	ns	$t_{WCLK1} + t_{WCLK2} = T_{CLK}$
t_{SUD}	22	—	—	ns	
t_{HD}	22	—	—	ns	

Note: Current and intensity are inversely proportional to the horizontal frequency (1/H).

Interface Signal Timing Chart

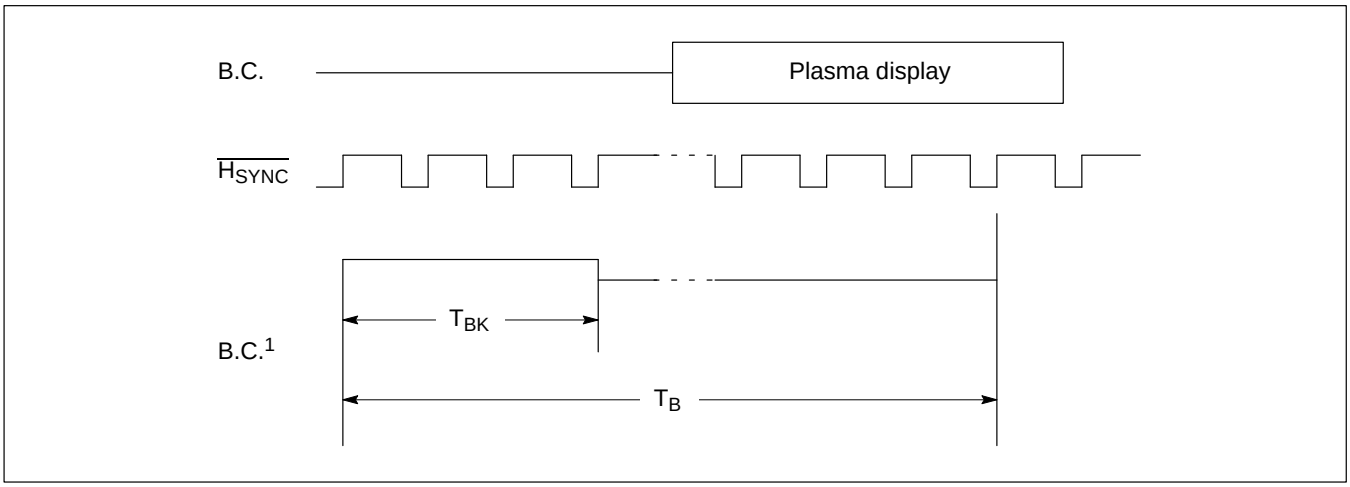


Brightness Control Signal Timing

Symbol	Minimum	Nominal	Maximum	Unit	Remarks
T_B	—	2 x V/N	—	H	H: Horizontal cycle
T_{BK}	—	—	2 x V/N	H	

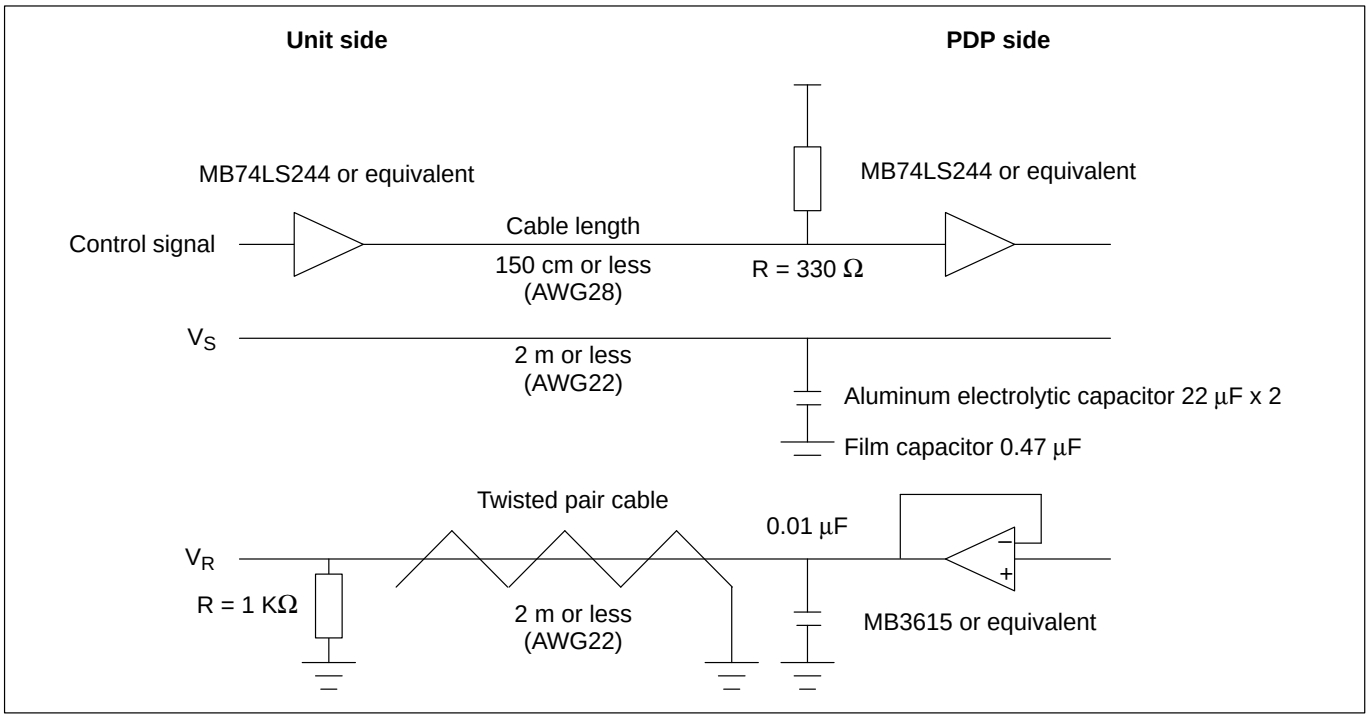
Notes: [1]V: Vertical/horizontal synchronization (number of lines per 1 V period)
[2]N: Integer
[3]The display brightness can be varied between 0 and 100% by controlling the B.C. pulse duty cycle.

Brightness Control Signal Timing Chart



Note: [1]The B.C. signal shall be synchronized with the $\overline{H_{SYNC}}$ signal.

Interface Circuit



TOUCH PANEL SPECIFICATION

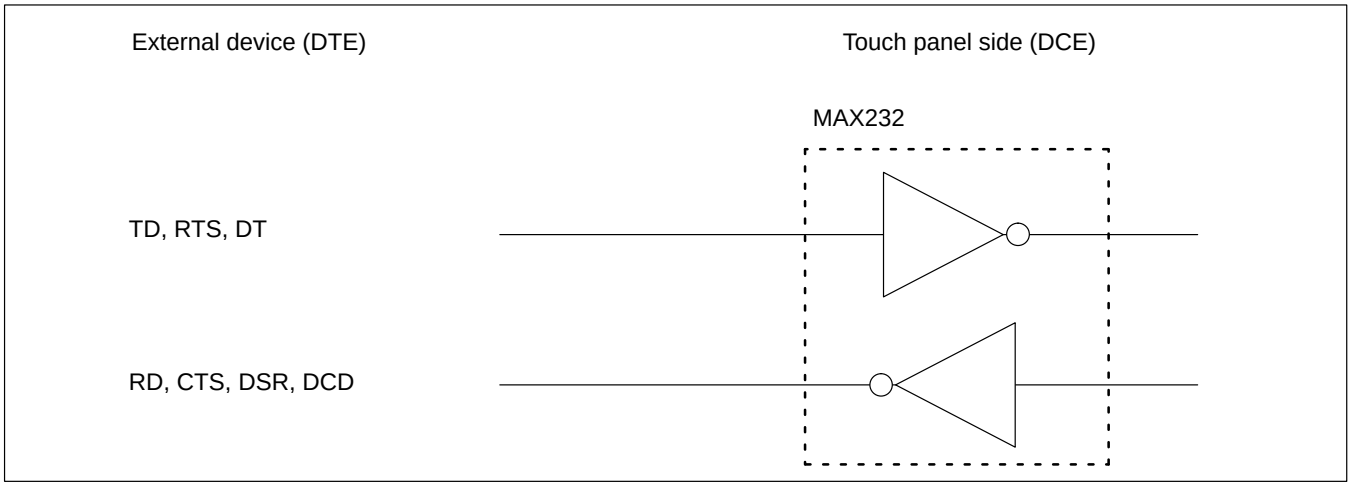
Touch Panel Interface Specifications

Interface method	Conforms to EIA RS-232C
Baud rate	Rate can be automatically set to 300, 1200, 2400, 4800, 9600, and 19200 bps (asynchronous). The specification can be changed by command.
Data configuration	Start bits (St): 1 bit Data (D0 to D7): 8 bits Parity (P): 1 bit, odd, even, or no parity can be selected. The specification can be changed easily.

→

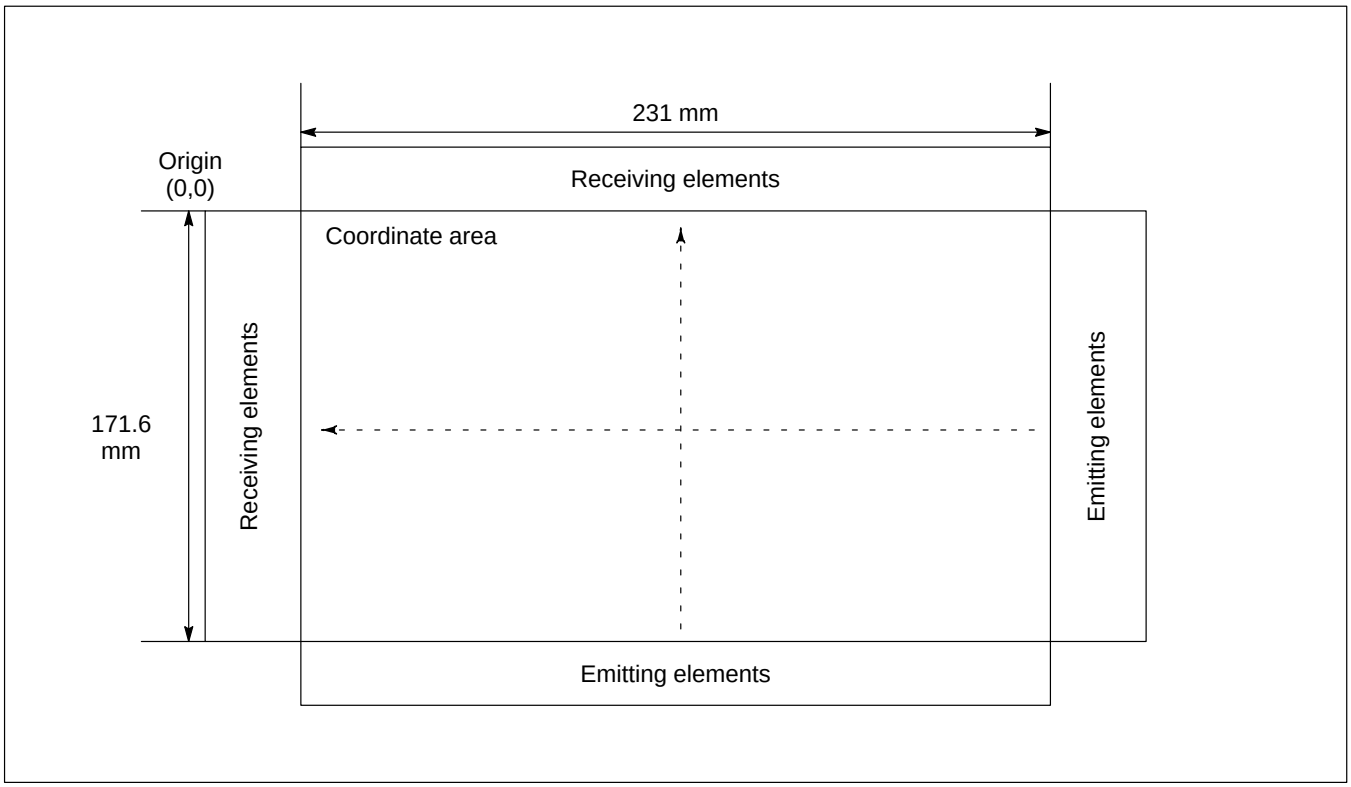
ST	D^0	D^1	D^2	D^3	D^4	D^5	D^6	D^7	P	SP	SP

Interface Circuit (touch panel)

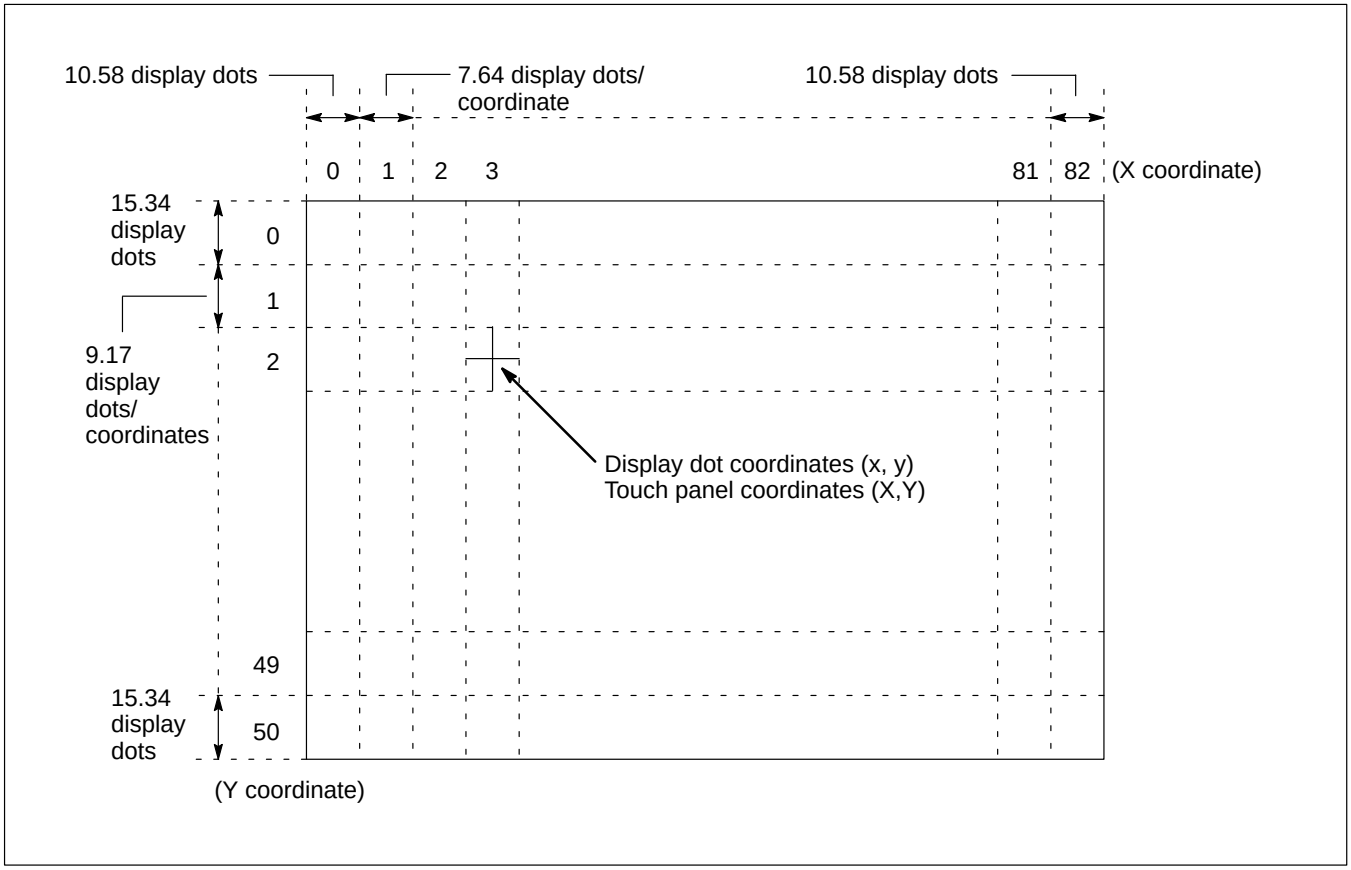


Coordinate Detection at Touch Panel

This unit has an effective area of 231 mm × 171.6 mm and transfers any touch detected within that area as X-Y coordinates. There are 42 pairs of infrared detector and emitting elements along the horizontal line and 26 pairs along the vertical line. The origin of the coordinates shall be the top left corner.



Position of Display and Coordinates



The relationship between display dot coordinates (x, y) and touch panel coordinate is (X, Y) is expressed as shown below:

$$x = 7.64 \times (X - 0.5) + 10.58 \pm 7$$
$$y = 9.17 \times (Y - 0.5) + 15.34 \pm 7$$

Touch panel installation error

$$X = (x - 10.58)/7.64 + 0.5 \pm 1$$
$$Y = (y - 15.34)/9.17 + 0.5 \pm 1$$

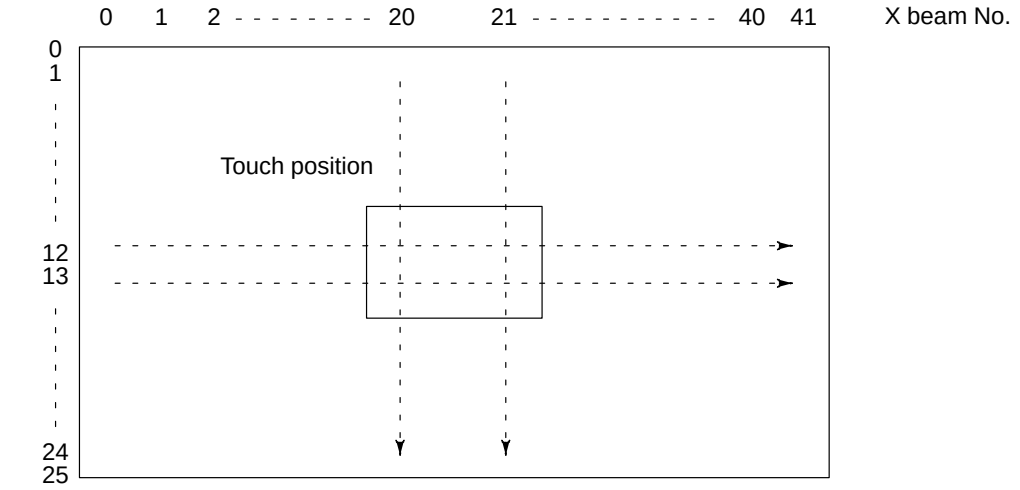
Touch panel installation error

Digits following the decimal point are rounded down.

Detection Coordinate Transfer Mode

(1) Scan mode

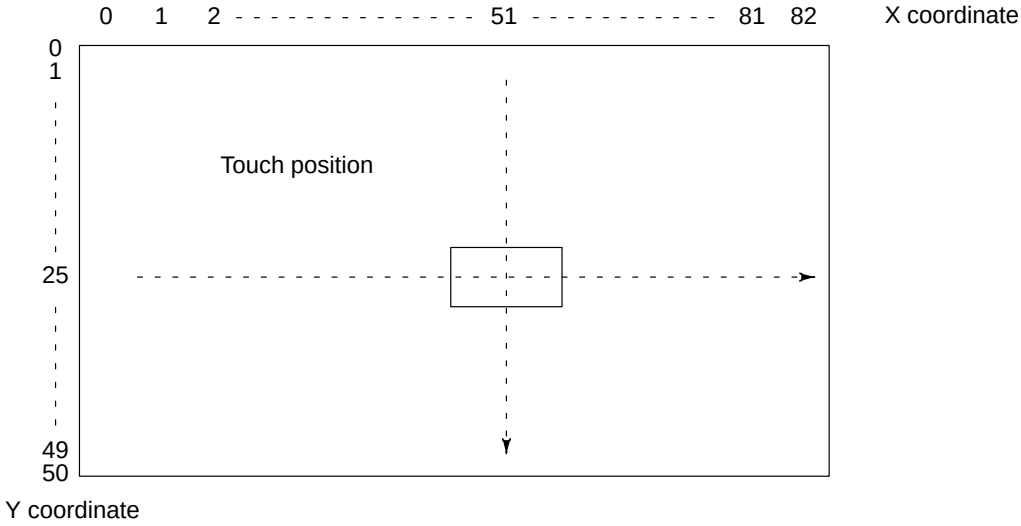
A beam number is assigned to each emitting element. The number of the blocked beam is transferred.



X beams 20 and 21 and Y beams 12 and 13 are transferred.

(2) Coordinate mode

The touch coordinate area is divided into coordinates of X = 0 to 82 and Y = 0 to 50. The coordinates of the touch position are transferred.



X coordinate 51 and Y coordinate 25 are transferred.

Notes: 1. If a wide area is touched and two or more beams are blocked, the central coordinates are transferred.
2. When two or more beams are blocked and they are not adjacent to each other (multiple touches at separate positions), coordinates are not transferred and a code is transferred to indicate non-adjacent hits.

Detection Operation Mode

Input point operation	Transfers the coordinates of the position touched first, and does not transfer the next coordinates until pressure is released.
Track operation	Transfers touch coordinates as long as the pressure is moving within the coordinate area. Does not transfer coordinates when pressure is released.
Continuous operation	Transfers touch coordinates as long as the pressure is within the coordinate area. Transfers touch coordinates even when pressure is released.
End point operation	Transfers coordinates of the point at which pressure is released.
Additional end point operation	In addition to input point operation, follow-up operation, and continuous operation, transfers the coordinates of the point at which pressure is released.

(1) Control commands

Item	Command	Code[1]	Function
1	Reset	3C	Clears all buffers and resets the touch system.
2	Echo mode ON	20	Sends back all received data to the host.
3	Echo mode OFF	21	Turns off the echo mode.
4	Touch system ON	2A	Starts scanning of the touch system.
5	Touch system OFF	2B	Stops scanning of the touch system.
6	Scanning mode set	22	Sets the detection coordinate mode for scanning mode.
7	Coordinate mode set	23	Sets the detection coordinate mode for coordinate mode.
8	Input point operation	25	Sets the detection coordinate mode for input-point operation.
9	Track operation	26	Sets the detection coordinate mode for track operation.
10	Continuous operation	27	Sets the detection coordinate mode for continuous operation.
11	End point operation	28	Sets the detection coordinate mode for end point operation.
12	Additional end-point operation	29	Adds the end-point operation to each detection operation mode (do not use this command when end-point operation is specified.)
13	Status report	32	Reports the status of the touch system.
14	Configuration report	33	Reports the number of processors in the touch system.
15	Firmware version report	34	Reports the firmware ROM version.
16	Defective beam analysis	36	Reports the status of the optical device.
17	Frame size report	37	Reports the frame size.
18	Self-diagnosis report	3A	Executes the self diagnostic test and reports the status.
19	Clear	3D	Clears the touch report buffer.
20	Hardware flow control ON	41	Enables handshaking with serial interface hardware.
21	Hardware flow control OFF	42	Disables handshaking with serial interface hardware.
22	Data transfer ON	44	Allows data transfer.
23	Data transfer OFF	43	Inhibits data transfer.
24	Baud rate/parity respecification	45	Returns to the setup mode for the data transfer rate and parity.
25	Touch state report	47	Reports the operation setting status of the touch system.
26	Single report	46	Transfers reports to the host system one by one.

Note: [1]The codes are hexadecimal.

(2) Automatic baud rate and parity setup

Baud rates and parity are specified by the transfer of the code (0D) and by the reset command.

(2) Default set values

i. Touch system: OFF

ii. Detection coordinate transfer mode: Coordinate mode

iii. Detection operation mode: Track operation

iv. Additional end-point operation: OFF

v. Data transfer: OFF

vi. Hardware flow control: OFF

CONNECTOR PIN ASSIGNMENT

Signal Connector

FCN-605Q026-G/S

Pin No.	Signal Name	Pin No.	Signal Name
1	$\overline{V_{SYNC}}$	2	S. GND
3	$\overline{H_{SYNC}}$	4	S. GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	S. GND
15	D0	16	S. GND
17	D1	18	S. GND
19	CLK	20	S. GND
21	N.C.	22	N.C.
23	N.C.	24	N.C.
25	N.C. (V_{CC})	26	N.C. (V_{CC})

Matching connector: FCN-607B026-G/D

Notes: [1]Do not connect anything to the N.C. pins.
[2]Pins 25 and 26 are V_{CC} output pins for options.

Signal Connector (Touch Panel)

HIF3BD-10PA-2.54DS (Hirose)

Pin No.	Signal Name	Symbol	Signal Direction		
			Touch Panel (DCE)		External Device (DTE)
1	Transmit data	TD	←		
2	Receive data	RD	→		
3	Request to send	RTS	←		
4	Clear to send	CTS	→		
5	Data terminal ready	DTR	←		
6	Data set ready	DSR	→		
7	Data carrier detected	DCD	→		
8	—	—			
9	Signal ground	SG			
10	Frame ground	FG			

Power Supply Connector

FCN-814P-009-TA

Pin No.	Signal Name
1	V_{CC}
2	GND
3	N.C.
4	GND
5	V_S
6	N.C.
7	N.C.
8	GND
9	V_R*

Notes: Matching connectors:
FCN-813J009-A housing
FCN-813J-T/Q contact for manual use
FCN-813J-T/R contact for automatic use

* This pin is the remote pin for automatically setting V_S when using the power supply (FPF07P-AC100). 0 to 2.5 VDC is output.

Power Supply Connector (Touch Panel) 641126–7 by AMP

Pin No.	Signal name
1	V_{CC}
2	GND
3	—
4	GND
5	N.C.
6	N.C.
7	GND

July 1992
Edition 1.0

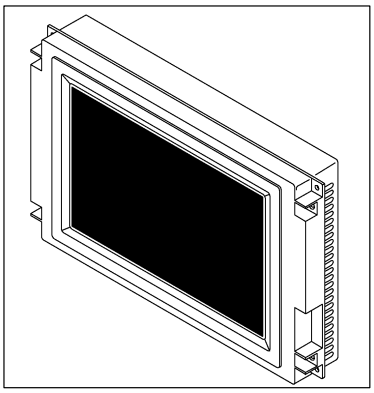
FUJITSU

DATA SHEET

FTE8050RP–003

Plasma Display Unit with Touch Panel (640 x 400 Dot 10″ Screen)

The FTE8050RP–003 is a human–machine interface that provides both screen display and input functions. A new high–brightness plasma display is integrated with a sheet–style resistance–film touch panel.

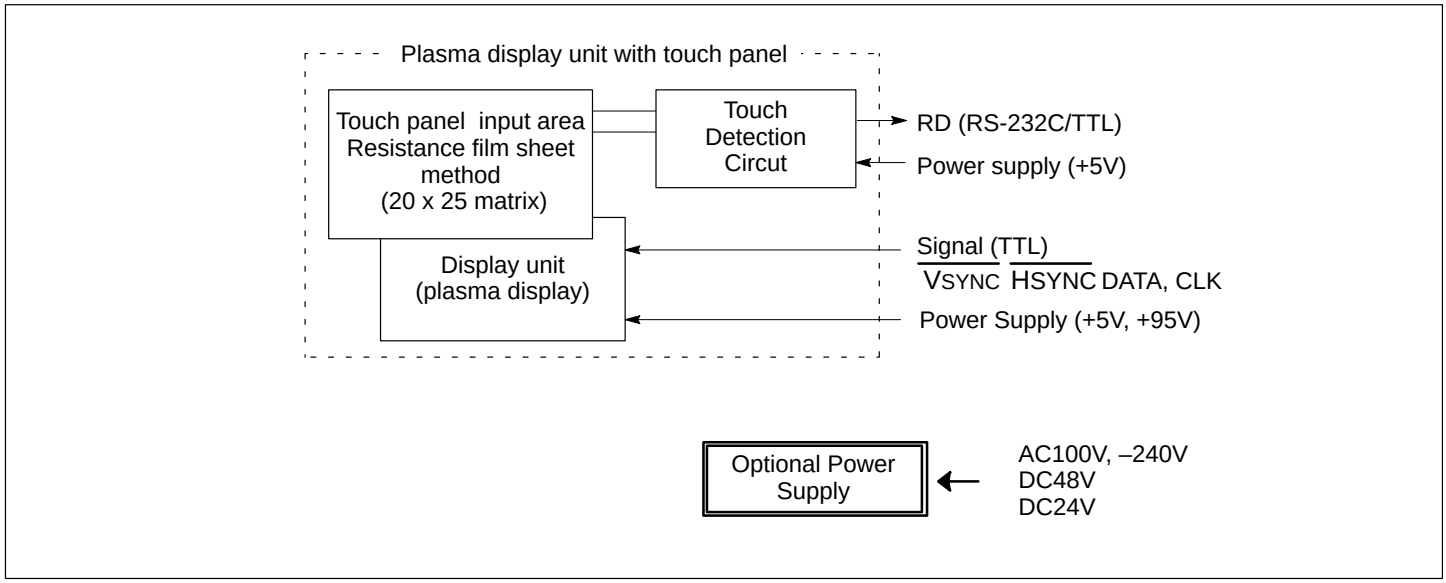


Even with the integration of the touch panel, the new plasma display is 70% brighter. It provides clear images by employing a 10″ display area with 640 x 400 dot resolution. The touch panel has a 20 x 25 key touch switch layout with a built–in touch detection circuit.

Because of its compact size, the FTE8050RP–003 requires less installation space. The enables its use with a greater variety of industrial equipment. Such equipment can be operated more easily by using the FTE8050RP–003 as a guidance display.

- 70% brighter display
- Display electrode insulation for long display life
- 10″ display area
- Integrated display and touch input
- Compact construction
- Standard interface conforming to CRT interface

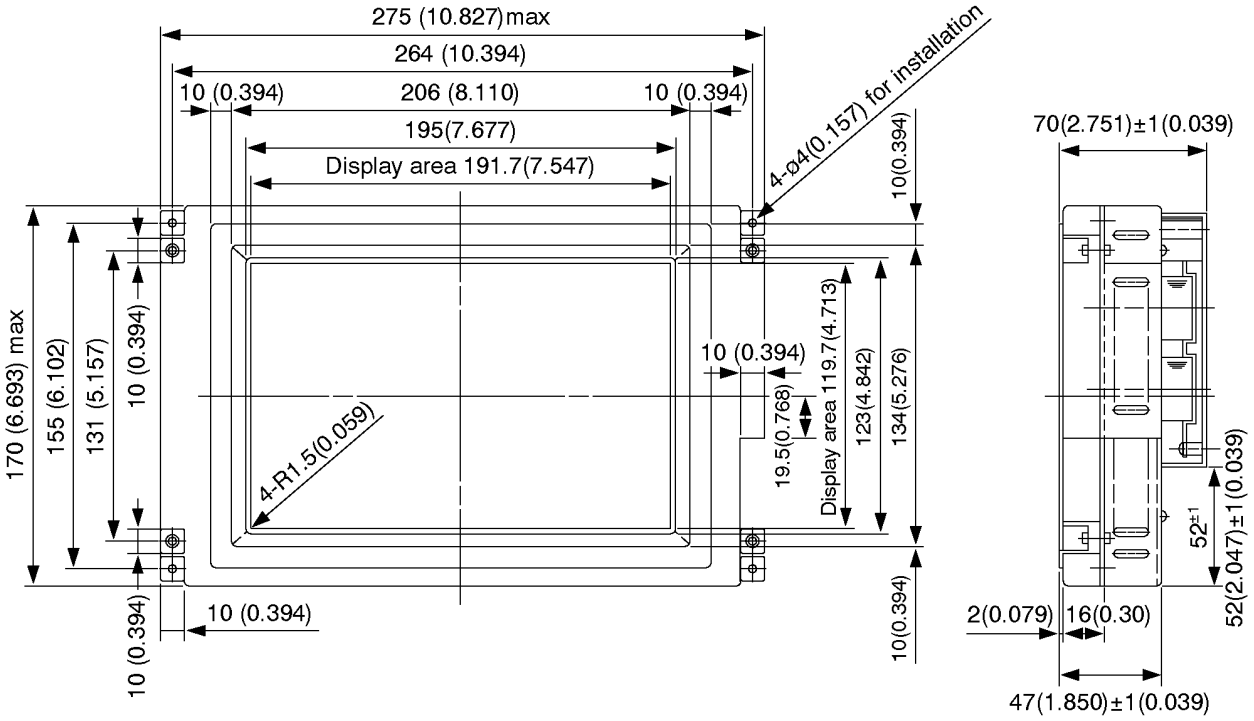
BLOCK DIAGRAM



SPECIFICATIONS

Item		Specification
Display Unit	Display Capacity	640 (horizontal) x 400 (vertical) dots
	Dot Pitch	0.33 mm (0.013”) Horizontal x 0.33 mm (0.013”) Vertical
	Dot Size	0.2 mm (approx.) (0.008 in.)
	Effective Display Dimensions	210.87 mm (8.3”) Horizontal × 131.67 mm (5.2”) Vertical
	Display Color	Neon orange
	Brightness	Spot: 100 cd/m^2 Typical (horizontal synchronous signal cycle 50μs Area Average: 16 cd/m^2 Typical
	Contrast	1:20 min
	Viewing Angle	120°min
	Interface	TTL complying with CRT ($\overline{V_{SYNC}}$ $\overline{H_{SYNC}}$ DATA CLK)
	Power Supply	+5V +95V (typ)
	Power Consumption	20W (typ)
	Method	Resistance Film Sheet Method (lower layer: glass; upper layer: polyester)
	Resolution	20 (horizontal) x 25 (vertical) Matrix Type
Touch Input Unit	Visual Area	221 mm (8.7”) Horizontal x 142 mm (5.6”) Vertical
	Switch Area	210.54 mm (8.29”) Horizontal x 131.34 mm (5.17”) Vertical
	Touch Force	350 g or less
	Input Method	With finger only (input with a pointed object will cause damage)
	Hardness of the Surface	2H or Less (according to JIS K 5400)
	Surface Filter Treatment	Non–Glare Treated
	Interface	Complying with RS–232C and TTL Level <u>Data Structure</u> Start Bit: 1 Bit Data: 8 Bits Stop Bit: 1 or 2 (can be changed) Parity: None, Odd Number, Even Number (can be changed) Baud Rate: 2400, 4800, 9600, 19200 bps (can be changed)
	Power Supply	+5V
	Current Consumption	500mA max
Temperature Range		0 to 40°C (putting unti upright, display rate of 50% or less)
Maximum External Dimensions		290 (W) × 192 (H) × 43 (D) mm (excluding the cable section)
Weight		Approximately 2.5 kg

External Dimensions



Unit: mm (in.)

CONNECTOR PIN ASSIGNMENT

Signal Connector

(Connector used: FCN-605Q026-G/S)

Pin No.	Signal Name	Pin No.	Signal Name
1	$\overline{V_{SYNC}}$	2	S. GND
3	$\overline{H_{SYNC}}$	4	S. GND
5	N.C. (D0)	6	N.C.
7	N.C. (D1)	8	N.C.
9	N.C. (D2)	10	N.C.
11	N.C. (D3)	12	N.C.
13	N.C.	14	S. GND
15	DATA	16	S. GND
17	N.C.	18	S. GND
19	CLK	20	S. GND
21	B.C.	22	N.C.
23	N.C.	24	N.C.
25	N.C. (V_{CC})	26	N.C. (V_{CC})

Mating connector: FCN-607B026-G/D

Power Supply Connector

(Connector used: FCN-815P009–TA)

Pin No.	Signal Name
1	V_{CC}
2	GND
3	N.C.
4	GND
5	V_S
6	N.C.
7	N.C.
8	GND
9	V_{R*}

Mating connector housing: FCN-813J009-A
Connector (manual): FCN-813J-T/Q
Connector (automaatic): FCN813J–T/R

Touch Panel Unit Signal

(Connector: FCN-705Q010–G/S)

Pin No	Signal	Signal Direction	
		Touch Area	Host Side
1	F. GND		
2	N.C.		
3	R.D		
4	N.C.		
5	R.D	→	
6	S.GRND		
7	S.GRND		
8	S.GRND		
9	S.GRND		
10	S.GRND		

Mating Connector: FCN–607B010–G/D

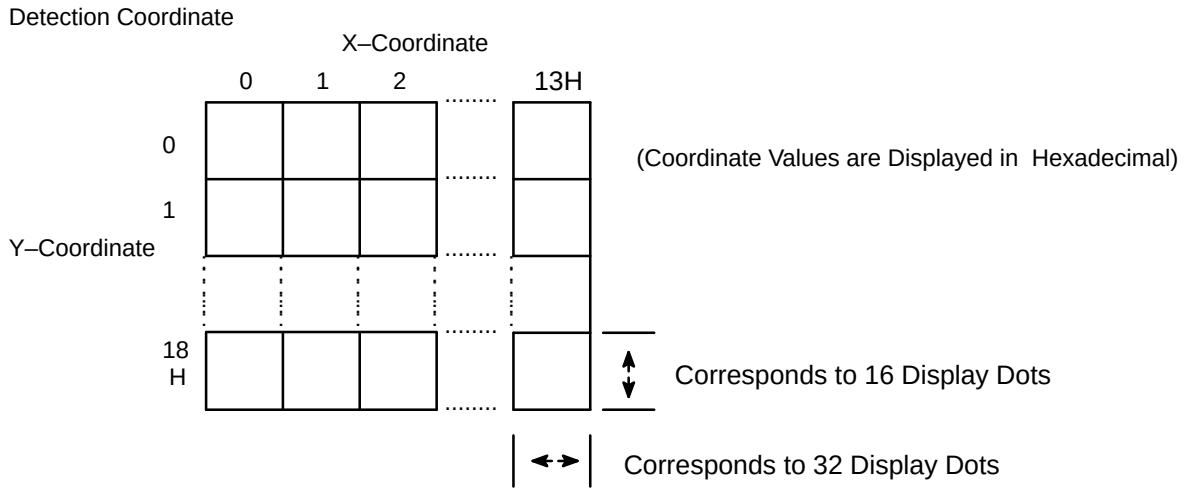
Power Supply Connector

(Connector: FCN–815P009–TA

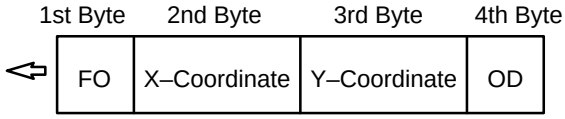
Pin No	Signal
1	VCC
2	GND
3	N.C.
4	GND
5	VS
6	N.C.
7	N.C.
8	N.C.
9	VR

Mating connector housing:FCN–813J009–A
Connector (manual): FCN813J–T/Q
Connector (automatic: FCN–813J–T/R

Data Format and Detection Coordinate



Data Format (4–Byte Structure)



Section 9

Power Supplies — *At a Glance*

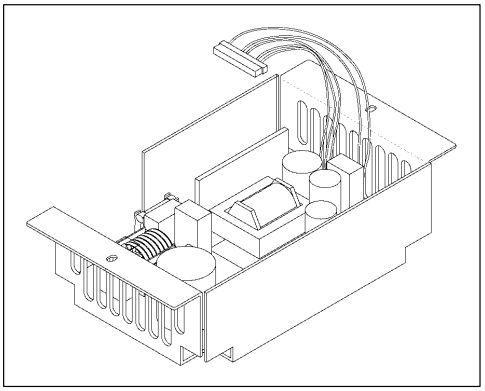
August 1990
Edition 1.0

FUJITSU

DATA SHEET

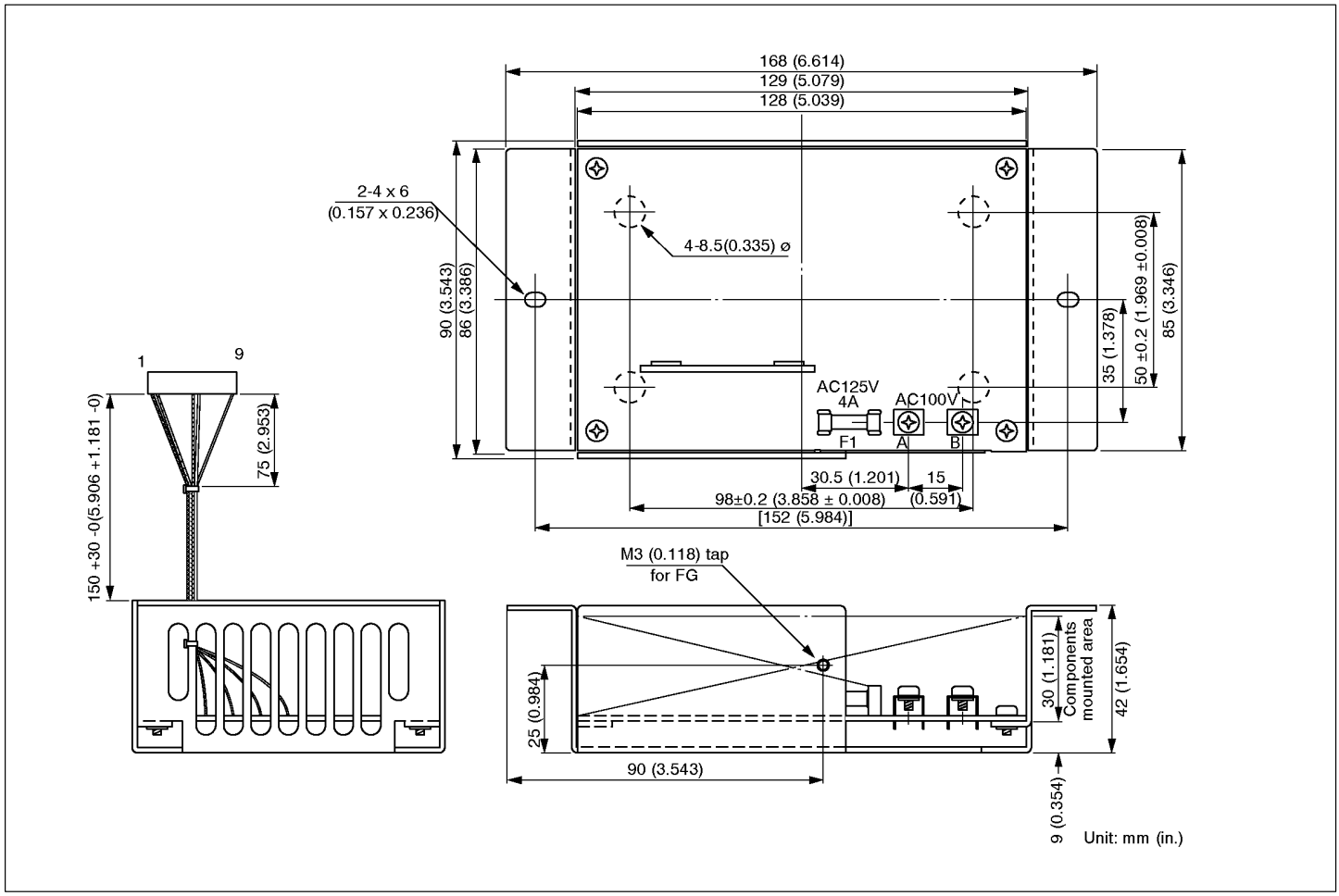
FPF07P-AC100
Power Supply for Plasma Display Unit

The power supply FPF07P-AC100 supplies required specified voltages to plasma display units FPF8050HRUK, FPF8060HRUM, and FPF8060HRUK.



- Strong, durable construction
- Designed to interface with several Fujitsu plasma display units
- Using reference voltage feature, automatically calibrates plasma display units
- Provides five voltage levels
- Meets UL standards

EXTERNAL DIMENSIONS



APPLICATIONS

This power supply unit is applied to the Plasma Display Units as listed below:
FPF8050HRUC, FPF8050HRUK, FPF8050HRUD series, FPF8060HRUM, FPF8060HRUK, FPF8060HRUC series, FPF8060HRUS series, FPF160128SRUA–020, FPF160128SRUA, FTE8050BPE, FTE8050RP series (PDP with touch panel).

Standard	Agency	File Number
NON	NON	
NON	NON	

SPECIFICATIONS

Item	Symbol	Rating	Remark
Input Voltage	V_{IN}	280VAC	(50/60Hz)
Operation Temperature	T_{OP}	0–55°C	
Storage Temperature	T_{STG}	–20–70°C	
Operation Humidity	H_{OP}	20–80%	no condensation
Storage Humidity	H_{STG}	20–85%	no condensation

PRODUCT SPECIFICATION EDITION RECORD

Edit	Date	Design	Check		Appr	Description	Prod Rev

POWER INPUT

Item	Symbol	Condition	Value
Input Voltage	V_{IN}		90–264VAC
Input Apparent Power	P		190 VA max
Input Frequency	f		50–60Hz 〈±5%)
Efficiency			65% min
Leak Current		264VAC	1.0 m4 max
Inrush Current			30A $_{(O–P)}$ max

POWER OUTPUT

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage 1 (Fixed)	V_{CC}	V_{IN} = 85 to 264 VAC 15 to 100% load	—	5.1	—	V
V_{CC} output ripple/noise		at resistive load	—	—	100	mV
Output voltage 2 (Variable)	V_S	V_{IN} = 85 to 264 VAC 15 to 100% load	88	94	100.5	V
V_S output ripple/noise		at resistive load	—	—	500	mV
Output current 1	I_{CC}	V_{IN} = 90 to 264 VAC 15 to 100% load (average)	0.05	—	1.2	A
Output current 2	I_S	V_{IN} = 90 to 264 VAC 15 to 100% load (peak)	—	—	3	A
	I_S	V_{IN} = 90 to 264 VAC 15 to 100% load (average)	0	—	550	mA

Note: Output voltage V_S is adjusted automatically by using reference voltage V_R from PDP unit. Relationship between V_S and V_R is: V_S = 88 + 5 X VR (±0.5V)

OVER SUPPLY PROTECTION

Item	Rated Voltage	Variable Rating	Protection Point Against Over Supply
Output Voltage 1 (Vcc)	5.1	Fixed	6.0 to 7.0 V
Output Voltage 2 (Vs)	88.0 + 5XVR (VR=) to 2.5V)	88.0 to 100.5V	108 to 128 V

MECHANICAL SPECIFICATIONS

Performance Specifications

Item	Value
Vibration Frequency: Acceleration: Time: Operating: Non-Operating	 10 to 55 to 10 Hz/5 min. 2 G max. 5 min. in X, Y, and Z direction 2 hr. in X, Y, and Z direction
Shock (non-operating) Acceleration: Time:	 40 G max. 11 ms, 5 times in X, Y, and Z direction
Pressure Operating: Non-Operating:	 700 to 1114 mb 340 to 1114 mb

MECHANICAL SPECIFICATIONS

General Characteristics

Item	Specification
Short Protection	No breakdown by short between GND and output terminals for 2 hr.
Dielectric Strength	2000V (primary/secondary FG 1000V (secondary FG) 1 min
Insulation Resistance	500 VDC/50MΩ min
Rising Time of Vcc	60 ms max

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Ratings	Remarks
Input Voltage	V_{IN}	135 VAC	50/60 Hz
Input Current	I_{IN}		
Power Consumption	P_O		Output

DC Input Characteristics

Item	Symbol	Condition	Value
Input Voltage	V_{IN}		90 to 132 VAC
Input Current	I_{IN}	90 VAC	1.3 A max.
Frequency	f		50 to 60 Hz (±5%)
Effective Ratio	—		70% min.
Leak Current	—	132 VAC	0.7 mA max.
	—	+15% -20%	within 0.5 sec
Inrush Current	—		30 A max.

DC Output Characteristics

This power supply unit outputs V_{CC} and V_S. V_{CC} is the fixed voltage. V_S varies with the reference voltage V_R (0 to 2.5 VDC) and is input through the 9th contact of the connector.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Voltage 1 (Fixed)	V_{CC}	V_{IN} 90 to 132 VAC 15 to 100% load		5.0		V
V_{CC} Input/Output Ripple/Noise					50	mV
Output Voltage 2 (Variable)	V_S	V_{IN} 90 to 132 VAC 15 to 100% load	88	94	100.5	V
V_S Input/Output Ripple/Noise					500	mV
Output Current 1 (average)	I_{CC}	V_{IN} 90 to 132 VAC 15 to 100% load	0.8	1.35	1.5	A
Output Current 2 (inrush)	I_S	V_{IN} 90 to 132 VAC 15 to 100% load			2	A
(average)	I_S	V_{IN} 90 to 132 VAC 15 to 100% load	50		310	mA

Note: Output voltage V_S is adjusted automatically by using reference voltage V_R. The relationship between V_S and V_R is given by the following equation.

$$V_S = 88 + V_R \times 5 \text{ (V)}$$

MECHANICAL SPECIFICATIONS

Performance Specifications

Item	Value
Vibration	
Frequency:	10 to 55 to 10 Hz/5 min.
Acceleration:	2 G max.
Time:	
Operating:	5 min. in X, Y, and Z direction
Non-Operating	2 hr. in X, Y, and Z direction
Shock (non-operating)	
Acceleration:	40 G max.
Time:	11 ms, 5 times in X, Y, and Z direction
Pressure	
Operating:	700 to 1114 mb
Non-Operating:	340 to 1114 mb

CONNECTOR PIN ASSIGNMENT

Power Input (Terminal)

(Three terminals with M3 Screw)

Terminal No.	Name
1	AC Power
2	AC Power
3	Frame Ground

Power Output (Connector with Cable)

Pin. No.	Name
1	+5 V
2	GND (L)
3	N.C.
4	GND (H)
5	+88 V
6	N.C.
7	N.C.
8	N.C.
9	V_R

Notes: Housing: FCN813J009-A
Contact: FCN813J-T/S
Cable: length – 150 mm (+30,–0)
wire – AWG22

July 1992
Edition 1.0

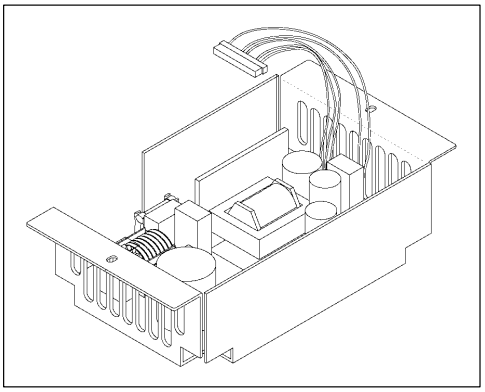
FUJITSU

DATA SHEET

FPF07P-AC110/220D
Power Supply for Plasma Display Unit

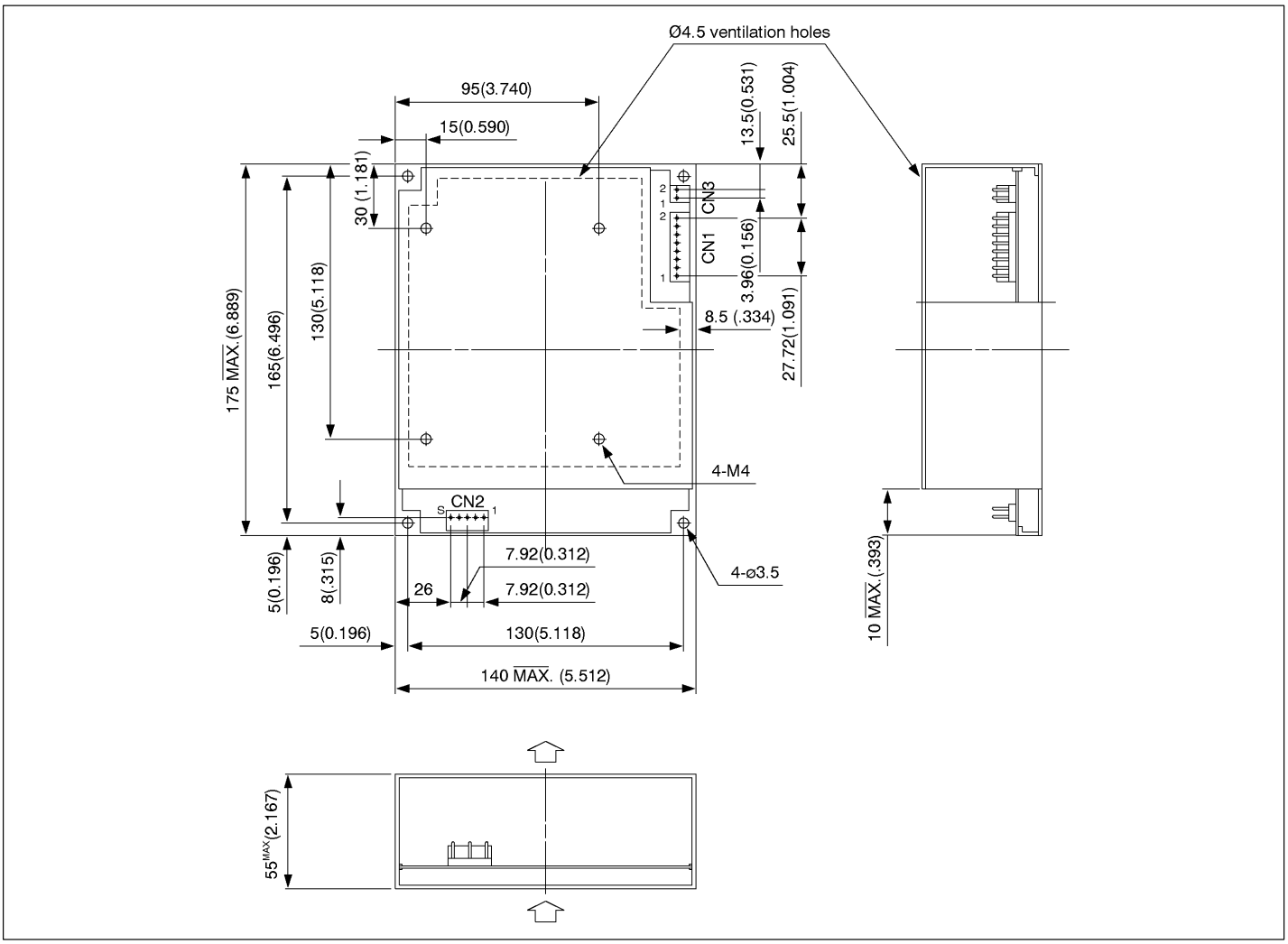
The power supply FPF07P-AC110/220D supplies required specified voltages to the following plasma display series:

FPF8050HRUC, FPF8050HRUK, FPF8050HRUD, FPF8060HRUM, FPF8060HRUK, FPF8060HRUC, FPF8060HRUS, FTE8050BPE, FTE8050RP.



- Strong, durable construction
- Provides ? voltage levels
-
-

EXTERNAL DIMENSIONS



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Ratings	Remarks
Input Voltage			
Input Current			
Power Consumption			

DC Input Characteristics

Item	Symbol	Condition	Value
Input voltage	V_{IN}		85 to 264 VAC
Input apparent power	P		180 VA max.
Input frequency	f		50 to 60 Hz (±5%)
Effeciency	—		65% min.
Leak Current	—	264 VAC	1.0 mA max.
Inrush Current	—		30 $A_{(O-P)}$ max.

DC Output Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage 1 (Fixed)	V_{CC}	V_{IN} = 85 to 264 VAC 15 to 100% load	—	5.1	—	V
V_{CC} output ripple/noise		at resistive load	—	—	100	mV
Output voltage 2 (Variable)	V_S	V_{IN} = 85 to 264 VAC 15 to 100% load	88	94	100.5	V
V_S output ripple/noise		at resistive load	—	—	500	mV
Output current 1	I_{CC}	V_{IN} = 85 to 264 VAC 15 to 100% load (average)	0.15	—	3.2	A
Output current 2 (inrush)	I_S	V_{IN} = 85 to 264 VAC 15 to 100% load (peak)	—	—	2	A
	I_S	V_{IN} = 85 to 264 VAC 15 to 100% load (average)	0	—	400	mA

Note: Output voltage V_S is adjusted automatically by using reference voltage V_R from PDP unit. Relationship between V_S and V_R is,

$$V_S = 88 + 5 \times V_R \ (\pm 0.5V)$$

MECHANICAL SPECIFICATIONS

Physical Specifications

Item	Value
External Dimensions	See external dimensions figure
Weight	Approx. 840g

Performance Specifications

Item	Value
Vibration Frequency: Acceleration: Time: Operation: Non-Operation:	 10 to 55 to 10 Hz/5 min. 2 G max. 5 minutes in X, Y, and Z direction 2 hours in X, Y, and Z direction
Shock (non-operation) Acceleration: Time:	 40 G max. 11 ms max. (5 times in each direction of X, Y, and Z)
Pressure Operation: Non-Operation:	 700 to 1114 mb 340 to 1114 mb
Operating Temperature	0 to 55°C
Storage Temperature	–20 to 70°C
Operating Humidity	20 to 80% RH (no condensation)
Storage Humidity	20 to 85% RH (no condensation)

CONNECTOR PIN ASSIGNMENT

CN-1 (Output)

B8P-VH

Pin No.	Power
1	V_{CC}
2	GND
3	GND
4	N.C.
5	$+V_S$
6	N.C.
7	GND
8	VR

Note: All connectors are made by Japan Solderless Terminals, Co. (J.S.T.)

CN-2 (Input)

B3P5-VH

Pin. No.	Power
1	V_O
2	N.C.
3	V_O
4	N.C.
5	.G.

CN-3 (Output)

B2P-VH

Pin. No.	Power
1	V_{CC}
2	GND

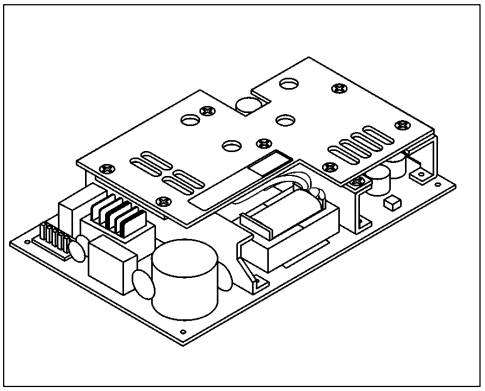
August 1990
Edition 1.0

FUJITSU

DATA SHEET

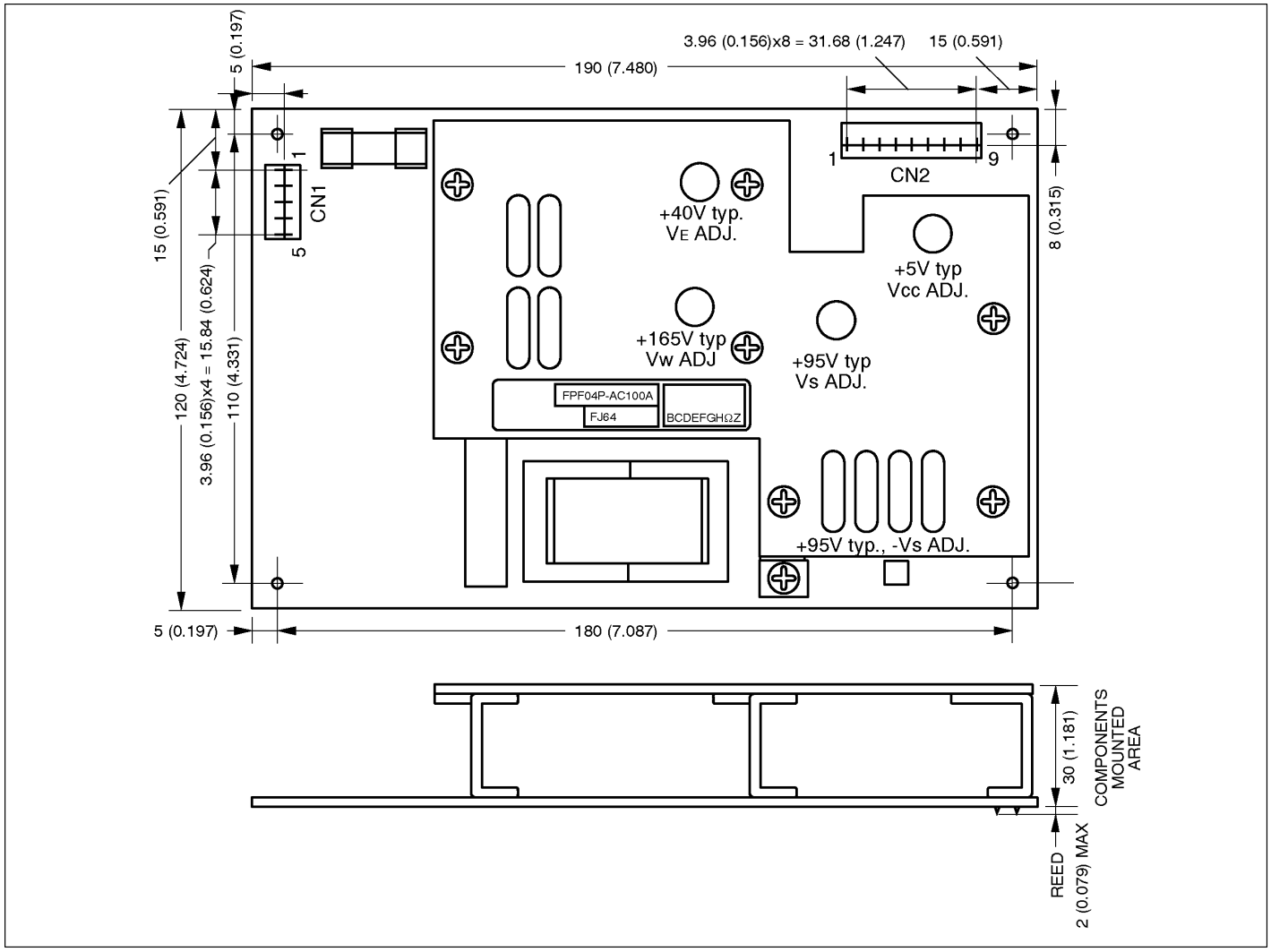
FPF04P-AC100A
Power Supply for Plasma Display Unit

The power supply FPF04P-AC100A supplies required specified voltages to plasma display unit FPF8050HFUGA by providing 100/115 VAC.



- Strong, durable construction
- Designed specifically to interface with plasma display unit FPF8050HFUGA
- Provides two voltage levels
- Meets UL standards

EXTERNAL DIMENSIONS



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Max. Ratings	Remarks
Input Voltage	V_I	135 VAC	
Input Current	I_I	1.5 A	
Power Consumption	P_O	45 W	(Output)
Inrush Current		45 A	

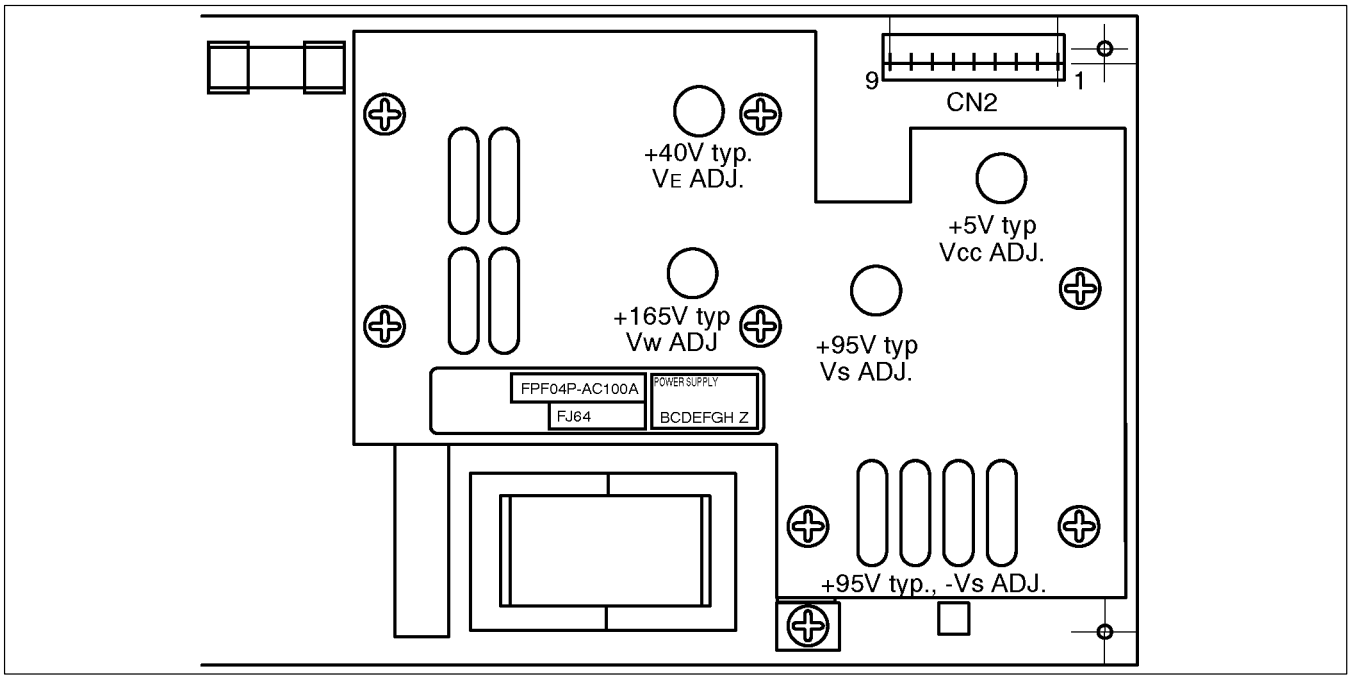
DC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_I	50/60 Hz, 15 to100% Load	90	100	130	VAC
Output Voltage 1	V_{CC}	V_O = 90 to 130	4.5	5.0	5.5	VDC
Output Voltage 2	$+V_S$	V_O = 90 to 130	80	95	110	VDC
Output Voltage 3	$–V_S$	V_O = 90 to 130	–110	–95	–80	VDC
Output Voltage 4	V_W	V_O = 90 to 130	160	165	175	VDC
Output Voltage 5	V_E	V_O = 90 to 130	38	40	42	VDC
Output Current 1	I_{CC}	V_O = 90 to 130 (Average)	0.8		1.4	A
Output Current 2	$+I_S$	V_O = 90 to 130 (Average)	20		160	mA
Output Current 3	$–I_S$	V_O = 90 to 130 (Average)	20		160	mA
Output Current 4	I_W	V_O = 90 to 130 (Average)			20 (300)	mA
Output Current 5	I_E	V_O = 90 to 130			150	mA
Ripple (including noise)		V_O = 90 to 130			1	%
Stability of Output Voltage	(V_{CC})				±5.0	%
Stability of Output Voltage	(V_S)				±2.0	%
Stability of Output Voltage	($–V_S$)				±2.0	%
Stability of Output Voltage	(V_W)				±5.0	%
Stability of Output Voltage	(V_E)				±5.0	%

Note: Output voltages (from 1 to 4) can be varied by variable resistors.

Output Voltage Adjustment

The voltage levels of V_s, $-V_s$, and V_W in the FPF04P-AC100A power supply must be adjusted to match the corresponding voltage levels of the FPF8050HFUGA plasma display unit. The V_S, $-V_S$, and V_W levels specific to each plasma display unit are shown on a label attached to the upper right corner of the plasma display frame. Change the V_S, $-V_S$, and V_W levels of the power supply by turning the volume control on the variable resistors. The location of the variable resistors on the power supply is shown below.



MECHANICAL SPECIFICATIONS

Physical Specifications

Item	Value
External Dimensions	190 x 120 x 30 mm (7.480 x 4.724 x 1.181 in.) See External Dimensions figure
Weight	Approximately 460 g

Performance Specifications

Item	Value
Vibration Frequency: Acceleration: Time: Operation: Non-operation	 10 to 55 to 10 Hz/5 min. 2 G max. 5 min. in X, Y, and Z direction 2 hrs in X, Y, and Z direction
Shock Acceleration: Time:	 40 G max. 11 ms max. in X, Y, and Z direction
Operating Temperature	–5 to 60°C
Storage Temperature	–20 to 70°C
Operating Relative Humidity	20 to 80% RH (no condensation)
Storage Relative Humidity	20 to 85% (no condensation)

CONNECTOR PIN ASSIGNMENT

CN-1

B9P-VH (made by J.S.T.)

Pin. No.	Signal Name
1	V_{CC}
2	GND (L)
3	$-V_S$
4	GND (H)
5	$+V_S$
6	V_W
7	N.C.
8	V_E
9	N.C.

Notes: Attached Connectors:
VHR-9N, Housing (made by J.S.T.)
SVH-21T-1.1, Contact (made by J.S.T.)

J.S.T. is Japan Solderless Terminal

CN-2

B3P-VH (made by J.S.T.)

Pin. No.	Signal Name
1	V_O
2	N.C.
3	V_O
4	N.C.
5	F.G.

Notes: Attached Connectors:
VHR-5N, Housing (made by J.S.T.)
SVH-21T-1.1, Contact (made by J.S.T.)

Crimping Tool:
YC-16 (made by J.S.T.)

Section 10

Sales Information — *At a Glance*

Introduction to Fujitsu

Fujitsu Limited (Japan)

Fujitsu Limited was founded as a telecommunications equipment manufacturer in 1935, and today is not only one of Japan's leading telecommunications companies, but also one of the world's largest computer manufacturers.

The leadership has resulted, at least in part, from the superb quality of the company's semiconductors and electronics components. Manufactured by the company's Electronics Devices Operations Group, these vital electronic devices also contribute to the high reliability and performance of products made by many other manufacturers around the world.

Today, Fujitsu is one the world's top manufacturers of semiconductors and electronic components. In Japan, Fujitsu's R&D laboratories for semiconductor and electronic components are situated in Kawasaki and Mie; the manufacturing works are located in Iwate, Aizu, Wakamatsu and Suzaka. Fujitsu also has six affiliated manufacturing works in the country. Overseas facilities in the US, Europe, and Asia also help to meet the growing global demand for Fujitsu semiconductors and electronic components.

Fujitsu enforces strict quality control at all stages of production, from materials selection, through manufacturing to final testing. As a result, Fujitsu's electronic devices are known for their extremely high reliability and excellent cost-to-performance ratio.

Fujitsu manufactures a full line of semiconductors and electronic components to meet the diverse applications of a wide variety of customers. Backed by Fujitsu's extensive R&D commitment equal to over 10% of annual sales, Fujitsu's electronic devices stay on the cutting edge of electronics technology.

Fujitsu Microelectronics, Inc. (USA)

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California was established in 1979, as a wholly-owned Fujitsu Limited; subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to four marketing division and two manufacturing divisions. FMI offers a complete array of components including semiconductor products for its customers throughout North and South America.

The Semiconductor Division provides a complete range of products and services for the worldwide market, including ASICs, ASSPs, memory devices, SPARC processors, graphics ICs and highly-integrated LAN devices. Fujitsu is a world leader in the designing and manufacturing of ASIC products, many of which are designed at the San Jose headquarters.

The Advanced Products Division (APD) is responsible for designing and selling a full line of SPARC® processors, peripheral chips, and the EtherStar™ LAN controller that it designed. The EtherStar™ LAN controller is the first VLSI device to integrate both StarLAN and Ethernet protocols into one device. The core of APD's Etherstar chip was the result of a cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets Ga As FETs and FET power amplifiers, lightwave microwave devices, optical devices, emitters, and SI transistors.

The largest marketing division is the Integrated Circuits Division (ICD) which offers a diverse range of advanced semiconductor products designed and manufactured by Fujitsu. Standard products include memories, analog/linear products, hybrid circuits, and microcomputer and communications products. ICD's custom and semi-custom products include application specific integrated circuits (ASICs).

The Electronic Components Division (ECD) evolved from a distribution organization for relays and connectors into the present board-based group that includes computer subsystems and standalone or plug-in components. ECD markets connectors, keyboards, thermal printers, plasma displays, and relays.

Fujitsu Electronics Devices Europe:

Fujitsu Mikroelektronik GmbH (FMG), West Germany
Fujitsu Microelectronics Limited (FML), UK
Fujitsu Microelectronics Italia SRL (FMIL), Italy
Fujitsu Microelectronics Ireland, Ltd (FME), Ireland

Fujitsu Mikroelecktronik GmbH (FMG) was established in June 1980 in Frankfurt, Germany, as Fujitsu's European headquarters and is a totally owned subsidiary of Fujitsu Limited, Tokyo. Fujitsu Microelectronics Limited (FML) is a sister company based in Maidenhead, England and dedicated to serving the UK, Ireland, and Scandinavia. Fujitsu Microelectronics Italia (FML) is based in Milan, Italy and serves Italy, Spain, Portugal, and the rest of Southern Europe. Together, GMG, FML, and FMIL supply the European market with a full range of integrated circuits and electronic components. Sales offices are located in Munich, Frankfurt, Stuttgart, Paris, Eindhoven, Milan, Maidenhead, and Stockholm.

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in Dublin, Ireland as Fujitsu's European assembly center for integrated circuits. FME produces DRAMs, EPROMs, and other LSI memory products.
The range of electronic components offered by FMG and FML includes connectors, keyboards, hybrid ICs piezoelectric devices, plasma devices, plasma displays, relays, and thermal printers.

Fujitsu Microelectronics Asia, PTE Ltd. (FMAP) , Singapore

Fujitsu Microelectronics Asia PTE Ltd, (FMAP) opened in August 1986, in Hong Kong, as a wholly-owned Fujitsu subsidiary for sales of electronic devices to the Asian, Australian, and Southwest Pacific markets. In 1990, FMAP moved to a new location in Singapore.

FMAP offers Fujitsu's wide range of electronic components such as connectors, keyboards, plasma displays, relays thermal printers, and integrated circuits.

Plasma Display Video Controller Compatibility Table

PDP Part No.	Flat Panel Based					VME Bus		CRT Based			
	Yamaha Display Master	Yamaha EGA Display Master	Yamaha SVGA Display Master	Allus Tech ATC-1141-XX	Atlantic Digital FPD Controller	Ziatech SVGA Card	Radisys FPD Controller	WD Paradise VGA Plus/EM-16	WD Paradise VGA 1024	Ahead Systems VGA Card	OEM Only CRT Controller
Character & Low Info Content											
FPC4012NRUL-01											X
FPF4015NRUF											X
EGA Compatible (640x400)											
FPF8050HFUGA	X (PROM)	X (PROM)		X (–05A)							
FPF8050HRUC-001	X (PROM)	X (PROM)		X (–05A)							
FPF8050HRUD-001	X (PROM)	X (PROM)		X (–05A)							
FPF8050HRUD-101	X (PROM)	X (PROM)		X (–05A)							
FPF8050HRUE-121	X (PROM)	X (PROM)		X (–05A)							
FPF8050HRUM	X (PROM)	X (PROM)		X (–05A)							
FPF8050HRUK	X (PROM)	X (PROM)		X (–05A)							
VGA Compatible (640x480)											
FPF8060HRUC-120	X (PROM)		X (PROM)	X (–05B)	X	X	X	X (MODIFY)			
FPF8060HRUM	X (PROM)		X (PROM)	X (–05B)	X	X	X				
FPF8060HRUK	X (PROM)		X (PROM)	X (–05B)	X	X	X	X (MODIFY)	X (PROM)	X (PROM)	
FPF8060HRUS-120	X (PROM)		X (PROM)	X (–053)	X	X	X		X (PROM)	X (PROM)	
Touch Screen Modules											
FTE8050RP-003	X (PROM)	X (PROM)		X (–05A)							
FTE8050BP/BPE	X (PROM)	X (PROM)		X (–05A)							
FTE8060BPC	X (PROM)	X (PROM)		X (–03)							
Large Size Units with Monitors											
FPF12896HRUF-B				X (–7B)							(SBUS)
FPF160128SRUA-001				X (–7B)							
FPF160128SRUA-020				X (–7B)							(SBUS)
FPF20000S-501				X (–7B)							(SBUS)
FPF20000S-601				X (–7B)							(SBUS)

Definition of Terms (all supplied by Fujitsu):
(MODIFY): A custom signal cable and ROM BIOS
(PROM): A set of PROMs
(SBUS): A SBUS controller – P/N FPF07A–SBUS

Video Controller Manufacturer List

Yamaha Corporation of America
Systems Technology Division
981 Ridder Park Drive
San Jose, CA 95131
1 (800) 543-7457
(408) 437-3133
(408) 437-8791 (FAX)
Contacts: Kevin Michelizzi, Sr. Engineer
Gene Jiane, Engineer

Allus Technology Corporation
12611 Jones Road
Houston, TX 77070
(713) 984-4455
(713) 894-6709 (FAX)
Contacts: Ray Hill, VP Engineering
Kenny Garrison, Eng. Manager

Atlantic Digital Corporation
851 West State Road 436
Suite 1051
Altamonte Springs, FL 32714
(407) 788-4200
(407) 788-8692 (FAX)
Contacts: Charlie Jordan, Eng. Manager

Ziatech Corporation
3433 Roberto Court
San Luis Obispo, CA 93401
(805) 541-0488
(805) 541-5088 (FAX)
Contact: Mark Evans, Sys. Prod. Manager

Radisys Corporation
19545 NW Von Muemann
Beaverton, OR 97006
1 (800) 950-0044
(503) 690-1229
(503) 690-1228
Contact: Merat Bagha, Engineer
Patty Baid, Account Manager

Western Digital (Paradise) Imaging*
800 West Middlefield Road
Mountain View, CA 94043
(415) 960-3360
(714) 932-5000
Contact: Retail Sales Department

*For Paradise Card Applications, contact FMI/ECD Marketing directly

Adhead Systems, Incorporated
44244 Fremond Blvd.
Fremont, CA 94538
(510) 623-0900
(510) 623-0960 (FAX)
Contact: Robert Wang, HW Engineer
Steve Lee, President

Paradise Card Distributors:

Tobar (Los Angeles)
(714) 951-0133
Contact: Jim Banks

Ingram/MicroD (Orange County)
1 (800) 456-8000 x41
Contact: Retail Sales Department

Fujitsu Plasma Display Data Book 1993–1994

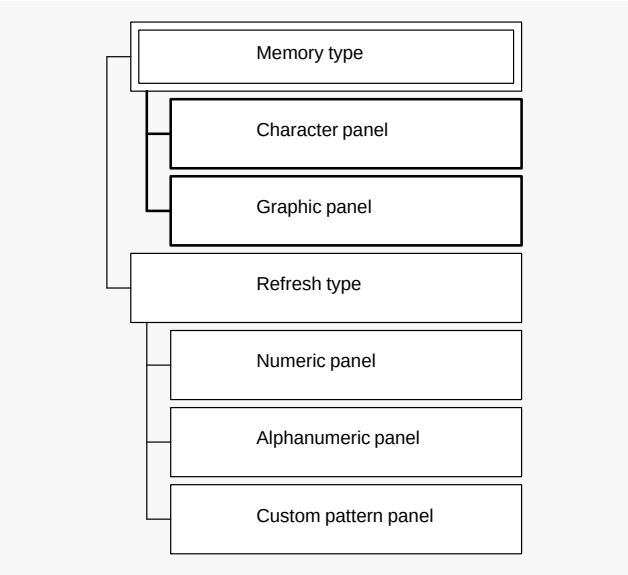
Section 12

Appendices — *At a Glance*

Plasma Displays—Technical Description

Introduction

Plasma display panels are electronic display devices that use the luminescence produced by AC gas discharge. They can be classified as follows.



The memory type plasma display panel has a function to sustain its display, which ensures a bright display that is free from flicker, warp, and image burn-in.

Memory Type

Plasma display panel structure

Figure 1 shows the structure of the plasma display panel. A major feature is that line and column electrodes formed from two glass boards are covered by dielectrics and are completely protected. The glass boards are set very close to each other, the peripheral area is completely sealed with glass, and neon gas and a small concentration of one of the rare gases are mixed and sealed inside.

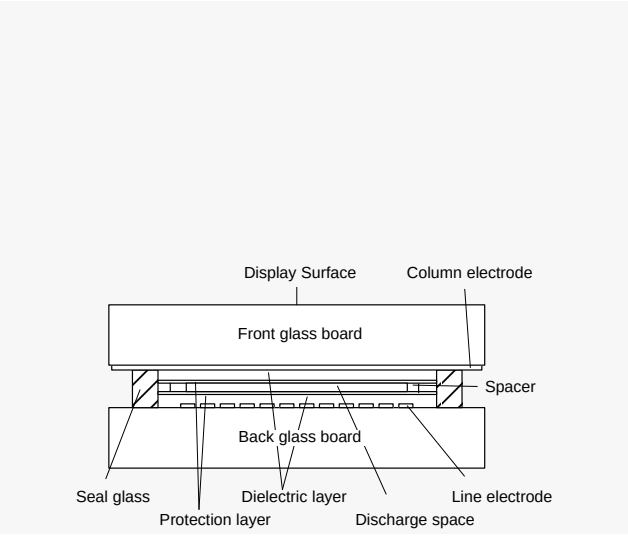


Figure 1. Structure of memory type plasma display panel

Principles of plasma display panel operation

When a gradually increasing voltage is applied between the line and column electrodes, the gas between them is ionized by the few charged particles there, a discharge current flows, and the dielectric plane covering the electrodes is charged (Figures 2a, 2b).

Since the charged voltage has the opposite polarity to the external voltage, voltage between the electrodes drops rapidly, gas ionization between the electrodes stops, and discharging stops. The voltage caused by charge left on the dielectric surface is called the wall voltage, and is retained for a long time.

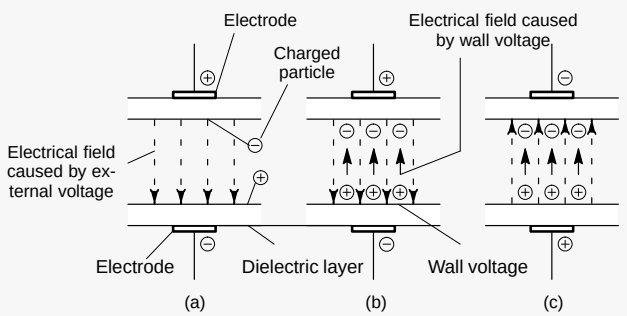


Figure 2. Basic operation principle of memory-type plasma display panel

When the polarity of the applied voltage is reversed, the wall voltage is added to the applied voltage, and the electrical field in the discharge space becomes stronger than during the first cycle. Thus, later discharge begins at a much lower applied voltage than at the first discharge (Figure 2c).

Figure 3 shows the basic voltage waveforms for driving the memory-type plasma display. Three pulsed power supplies (sustain pulse, write-in pulse, erasing pulse) are necessary to control or maintain the display.

The sustain voltage is maintained in an unchanging discharge state by setting it at a voltage which is higher than Vsm (the minimum sustain voltage) but lower than Vf (the voltage when firing begins).

The write-in and erasing pulses are applied to selected electrodes. In the write-in operation, when voltage is applied between the specified selected line and column electrodes and the voltage at the intersection exceeds Vf (firing voltage), discharge begins and continues after the write-in pulse has disappeared (because of the sustain pulse and wall voltage). The voltage does not exceed Vf at unselected electrodes and there is no discharge.

Erasing uses an extremely small pulse. As in the write-in pulse, it is applied between the selected row and column electrodes. The voltage is the same as Vs, but discharge during the erasing pulse is weak because the pulse is so narrow. The wall voltage is also low, so discharge cannot be continued on the following sustain pulse, and the display disappears.

Refresh Type

Plasma display panel structure

Figure 4 shows the basic structure of the refresh–type plasma display panel. The front glass board formed from the digit electrode (a transparent conducting film) protected by the dielectric layer and the back glass board formed from the segment electrode protected by the dielectric layer face each other. After the peripheral area has been sealed, neon gas is sealed inside the display. The refresh-type differs from the memory-type in that there is a layer of cells.

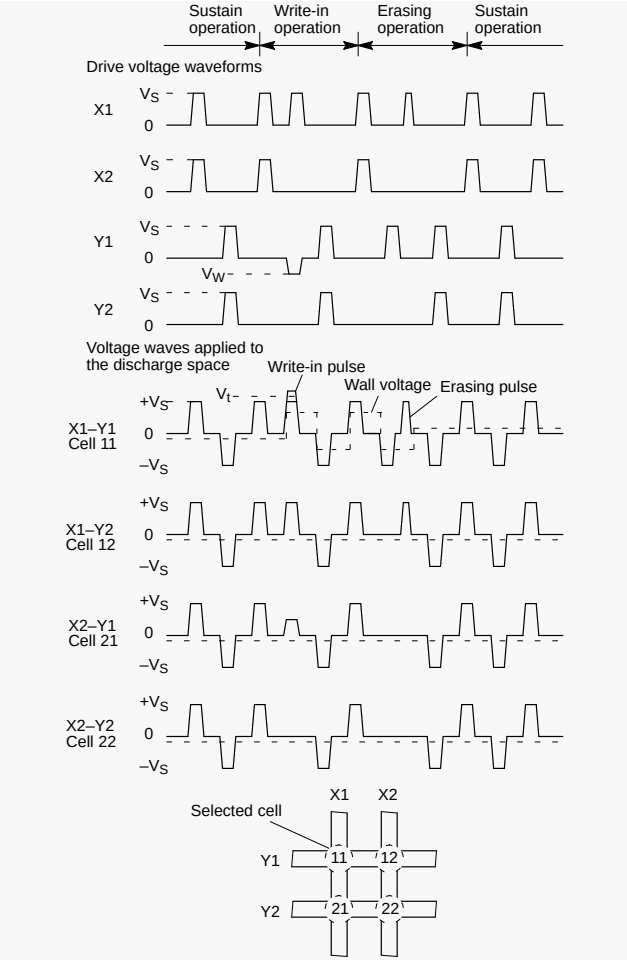


Figure 3. Drive voltage waveforms in memory-type plasma display panel

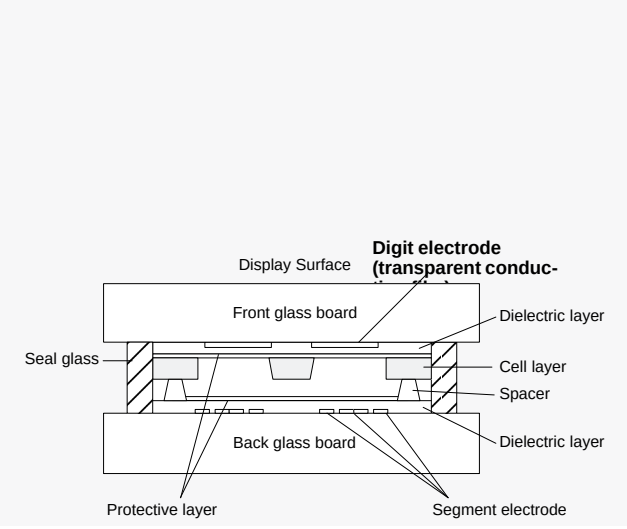


Figure 4. Structure of refresh type plasma display panel

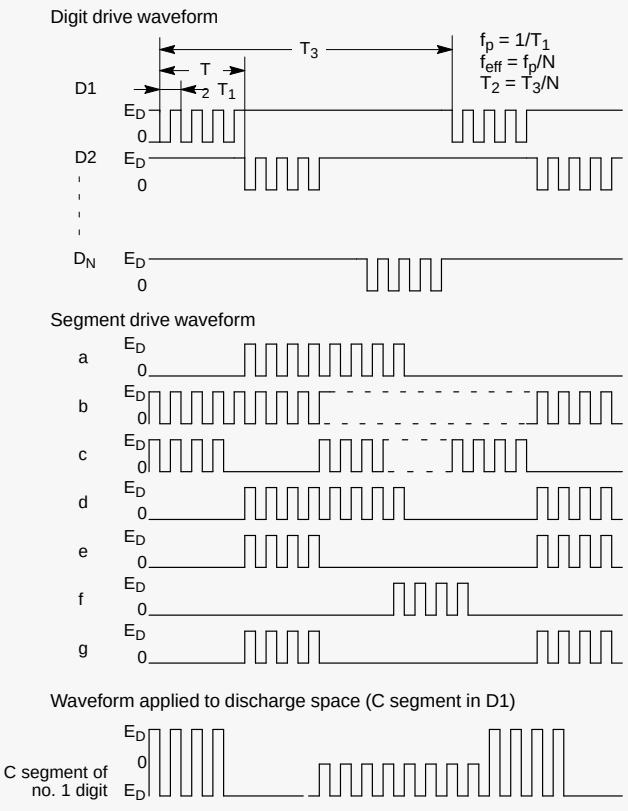


Figure 5. Drive voltage waveforms in refresh-type plasma display panel

Operating principles of plasma display panel

The operating principles of the refresh-type plasma display panel are slightly different to those of the memory-type plasma display.

Figure 5 shows the basic applied voltage waveforms.

A high-frequency drive voltage is applied between the digit electrode and the segment electrode, and discharge begins. The display lights when this exceeds the panel firing voltage. The intensity varies according to the drive pulse frequency.

The divided dynamic drive method is normally used in a display with many digits. The effective frequency for the digit electrode in this case is f_{eff} = fp/N, where fp is the power supply drive pulse frequency, and N is the number of digits. This is an important parameter in determining the intensity of the display.

The minimum drive voltage ($E_D$min.) is the lowest voltage at which the selected segments fire correctly, and the maximum drive voltage ($E_D$max.) is the highest voltage at which unselected elements glow. Consequently, the drive voltage (E_D) must be set between $E_D$max. and $E_D$min. to display data correctly.