

# **Fujitsu**

## **64M Bit**

# **Synchronous**

# **DRAM**

Target Spec

**MB81164441A/MB81164442A**  
**MB81164421A/MB81164422A**  
**64M BIT SYNCHRONOUS DRAM**

VCC	1	54	VSS
NC	2	53	NC
VCCQ	3	52	VSSQ
NC	4	51	NC
DQ0	5	50	DQ3
VSSQ	6	49	VCCQ
NC	7	48	NC
NC	8	47	NC
VCCQ	9	46	VSSQ
NC	10	45	NC
DQ1	11	44	DQ2
VSSQ	12	43	VCCQ
NC	13	42	NC
VCC	14	41	VSS
NC	15	40	NC/VREF
/WE	16	39	DQM
/CAS	17	38	CLK
/RAS	18	37	CKE
/CS	19	36	NC
A13	20	35	A11
A12	21	34	A9
A10	22	33	A8
A0	23	32	A7
A1	24	31	A6
A2	25	30	A5
A3	26	29	A4
VCC	27	28	VSS

## MB81164841A/MB81164842A MB81164821A/MB81164822A 64M BIT SYNCHRONOUS DRAM

Organization 4 banks x 2,097,152 words x 8 bits  
2 bsns x 4,194,304 words x 8 bits

Clock Frequency 125/100/83/67 MHz max.

Refrech Cycle 128ms/8,192cycles

Power Dissipation (4banks) T.B.D  
(2banks) T.B.D

Power Supply 3.3 ± 0.3 V

Fully Synchronous Operation  
Referred To The Positive Clock Edge

LVTTL & SSTL\* I/O Interface

\* : Stub Series-Terminated Transceiver Logic  
MB81164841A/MB81164821A Only

4 or 2 Banks Interleave Operation  
With Bank Select (A12&A13 or A13)

Programmable Wrap Type And  
Burst Length (1,2,4,8,&Full Column)

Auto-refresh & Self-refrsh

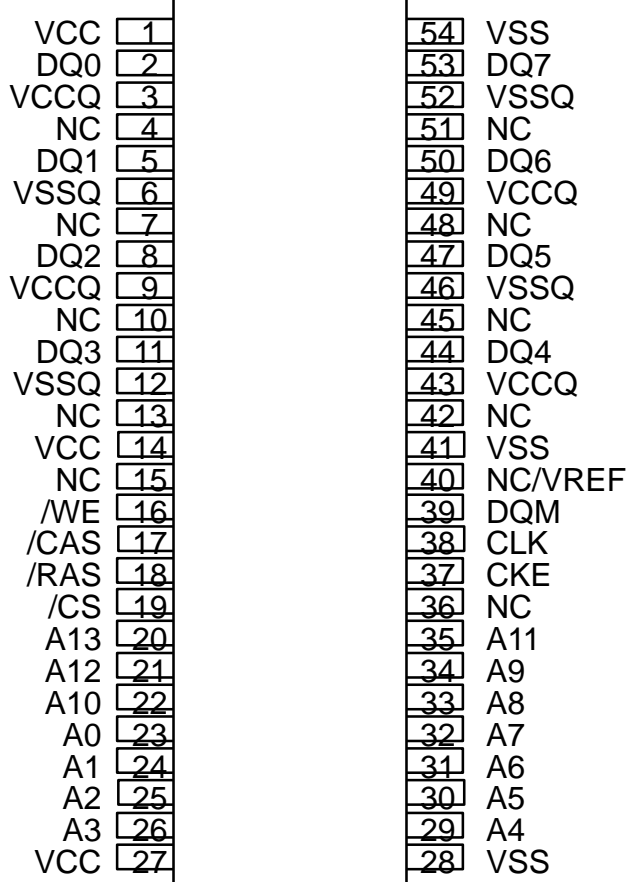
Clock Enable For Timing  
Synchronization And Power Down

Input Data And Output Mask Option

Address

Row Address A0-A10 (4 banks)  
A0-A11 (2 banks)

Column Address A0-A9  
Bank Select A12,A13 (4 banks)  
A13 (2 banks)



## MB811641641A/MB811641642A MB811641621A/MB811641622A 64M BIT SYNCHRONOUS DRAM

Organization 4 banks x 1,048,576 words x 16 bits  
2 banks x 2,097,152 words x 16 bits

Clock Frequency 125/100/83/67 MHz max.

Refrech Cycle 128ms/8,192cycles

Power Dissipation (4banks) T.B.D  
(2banks) T.B.D

Power Supply 3.3 ± 0.3 V

Fully Synchronous Operation  
Referred To The Positive Clock Edge

LVTTL & SSTL\* I/O Interface

\* : Stub Series-Terminated Transceiver Logic  
MB811641641A/MB811641621A Only

4 or 2 Banks Interleave Operation  
With Bank Select (A12&A13 or A13)

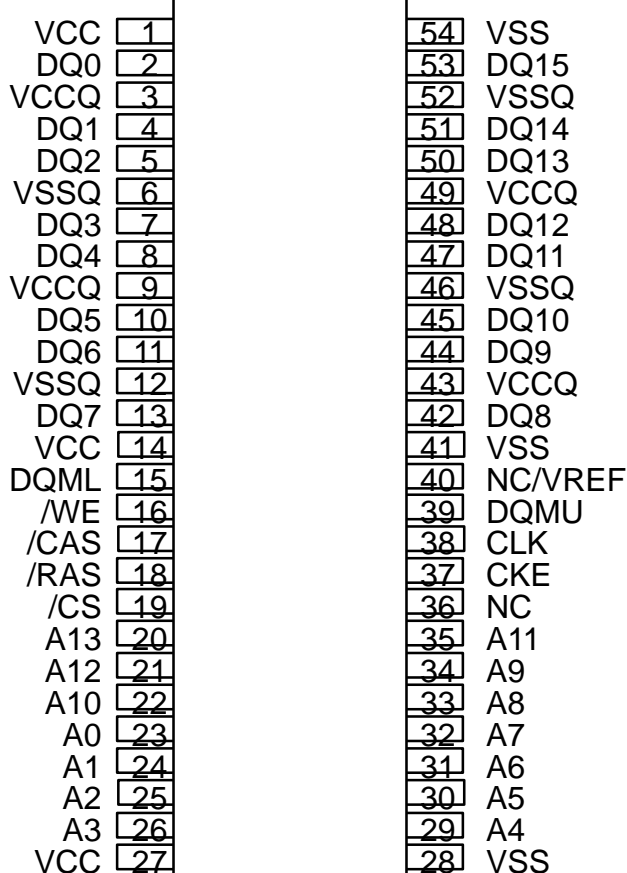
Programmable Wrap Type And  
Burst Length (1,2,4,8,&Full Column)

Auto-refresh & Self-refrsh

Clock Enable For Timing  
Synchronization And Power Down

Input Data And Output Mask Option

Address  
Row Address A0-A10 (4 banks)  
A0-A11 (2 banks)  
Column Address A0-A8  
Bank Select A12,A13 (4 banks)  
A13 (2 banks)



Pin Assignment  
(Top View)

Package : 54pin TSOP Type-II Package  
(400mil, 0.8mm Lead Pitch)

## MB811643241A/MB811643242A MB811643221A/MB811643222A 64M BIT SYNCHRONOUS DRAM

Organization	4 banks x 524,288 words x 32 bits 2 banks x 1,048,576 words x 32 bits				
Clock Frequency	125/100/83/67 MHz max.	VCC	1	84	VSS
Refrech Cycle	128ms/8,192cycles	DQ0	2	83	DQ31
Power Dissipation	(4banks) T.B.D (2banks) T.B.D	VCCQ	3	82	VSSQ
Power Supply	3.3 ± 0.3 V	DQ1	4	81	DQ30
Fully Synchronous Operation Referred To The Positive Clock Edge		DQ2	5	80	DQ29
LVTTL & SSTL* I/O Interface		VSSQ	6	79	VCCQ
* : Stub Series-Terminated Transceiver Logic MB811643241A/MB811643221A Only		DQ3	7	78	DQ28
4 or 2 Banks Interleave Operation With Bank Select (A12&A13 or A13)		DQ4	8	77	DQ27
Programmable Wrap Type And Burst Length (1,2,4,8,&Full Column)		VCCQ	9	76	VSSQ
Auto-refresh & Self-refrsh		DQ5	10	75	DQ26
Clock Enable For Timing Synchronization And Power Down		DQ6	11	74	DQ25
Input Data And Output Mask Option		VSSQ	12	73	VCCQ
Address		DQ7	13	72	DQ24
Row Address	A0-A10 (4 banks)	DQ8	14	71	DQ23
Column Address	A0-A7 (4 banks)	VCCQ	15	70	VSS
Bank Select	A0-A7 or A0-A6 (2 banks)	DQ9	16	69	DQ22
	A12,A13 (4 banks)	DQ10	17	68	DQ21
	A13 (2 banks)	VSSQ	18	67	VCCQ
Package : 84pin TSOP Type-II Package (400mil, 0.5mm Lead Pitch)		DQ11	19	66	DQ20
		VCC	20	65	VSS
		NC	21	64	VC
		NC	22	63	NC
		DQ12	23	62	DQ19
		VCCQ	24	61	VSSQ
		DQ13	25	60	DQ18
		DQ14	26	59	DQ17
		VSSQ	27	58	VCCQ
		DQ15	28	57	DQ16
		DQM0	29	56	VREF/NC
		DQM1	30	55	DQM3
		/WE	31	54	DQM2
		/CAS	32	53	CLK
		/RAS	33	52	CKE
		/CS	34	51	DU
		A13	35	50	A11
		A12	36	49	A9
		A10	37	48	A8
		A0	38	47	A7
		A1	39	46	A6
		A2	40	45	A5
		A3	41	44	A4
		VCC	42	43	VSS

Pin  
Assignment  
(Top View)

## DYNAMIC RAM