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FUJITSU

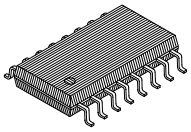
DATA SHEET

MB87091

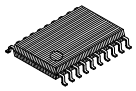
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

CMOS SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH POWER SAVING FUNCTION

The Fujitsu MB87091 is a CMOS serial input Phase Locked Loop (PLL) frequency synthesizer ideal for use in cordless telephone sets and other radio equipment. It incorporates an inverter for an oscillation circuit, a programmable reference divider (14–bit binary programmable reference counter), a shift register control register, latches, a programmable divider (6–bit binary swallow counter with 12–bit binary programmable counter and dual modulus prescaler: 64/65), a phase comparator, an intermittent mode control circuit, and a constant–current charge pump. The power save control input pin (PS) for the intermittent mode control circuit is used to switch between the stand by and active modes. This is used for phase synchronization at the beginning of operation. The MB87091 permits construction of PLL frequency synthesizers with operating frequencies of up to 300 MHz.



(FPT-16P-M06)



(FPT-20P-M03)

FEATURES

- Single power supply voltage: V_{DD} = 2.7 to 3.3V
- Built–in inverter for an oscillator
- Adjustable output current of the charge pump with an external resistor
- Intermittent mode control circuit
- Two phase comparator outputs (for external and internal charge pumps)
- Wide operating temperature range (T_A) –40°C to 60°C
- Plastic DIP ackage(Suffix: –P), Plastic SOP package(Suffix: –PF), Plastic SSOP package (Suffix: –PFV)
- Setting the divide ratio
  Use the below formula to define the parameters for setting the divide ratio
  $\underline{f_{VCO}} = (\underline{N} \times \underline{M} \div \underline{A}) \times (\underline{f_{OSC}} \div \underline{R})$ (N>A)
  (f_{VCO}) Output frequency of the external VCO
  (N) Preset divide ratio of 12–bit binary programmable counter (5 to 4,095)
  (M) Preset modulus of the dual modulus prescaler (64)
  (A) Preset divide ratio of 6–bit binary swallow counter (0 to 63)
  (f_{OSC}) Output frequency of the external reference frequency oscillator
  (R) Preset divide ratio of 14–bit binary programmable reference counte (5 to 16,383)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

(V_{SS}=0V)

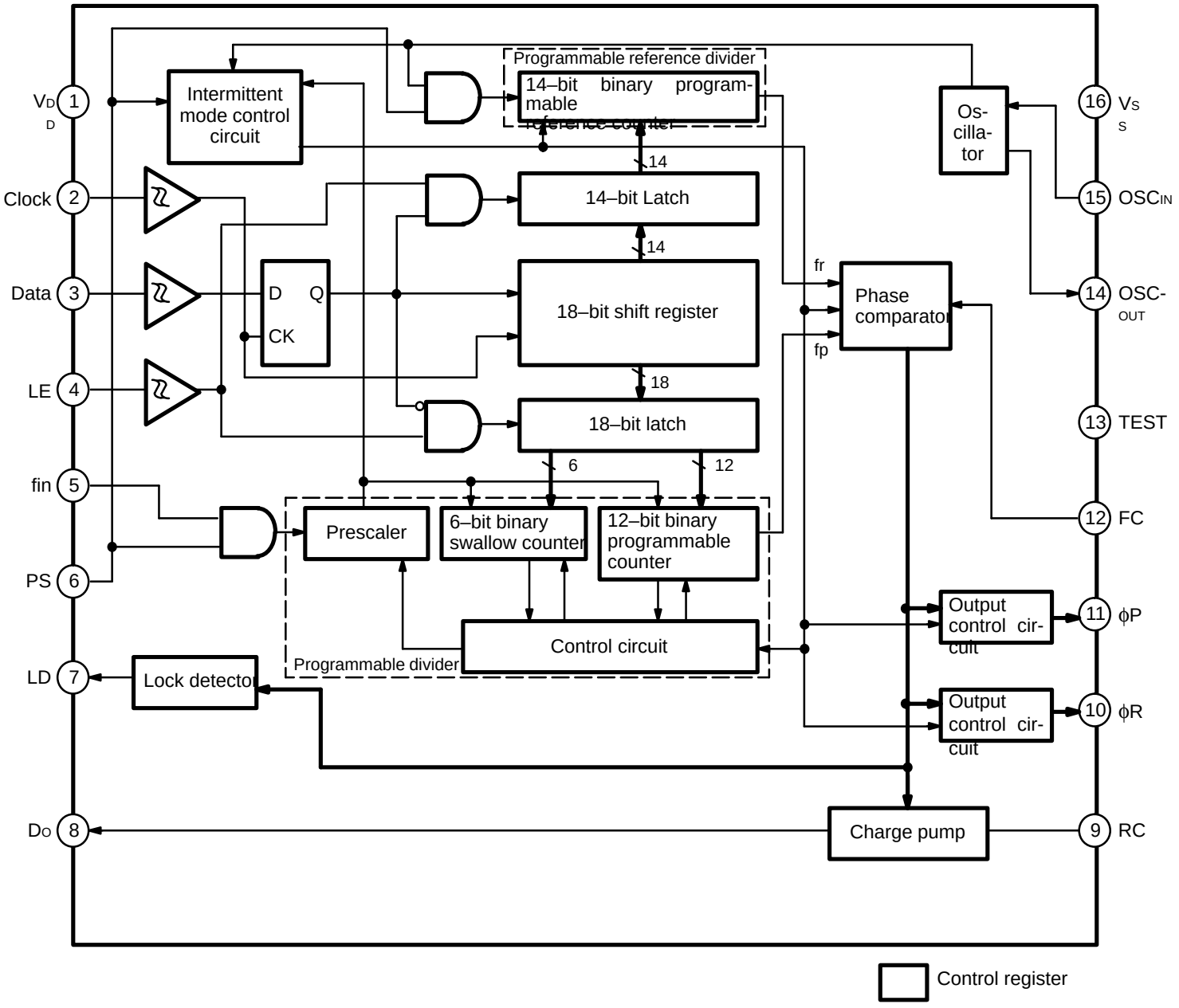
Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	V_{SS}–0.5 to V_{SS}+6.0	V
Input voltage	V_{IN}	V_{SS}–0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	V_{SS}–0.5 to V_{DD}+0.5	V
Output current	I_{OUT}	±10	mA
Ambient temperature	T_A	–40 to +60	°C
Storage temperature	Tstg	–40 to +125	°C
Power dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

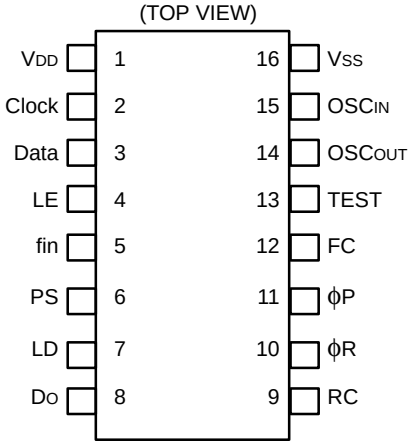
BLOCK DIAGRAM OF MB87091

(This block diagram is for DIP/SOP packages.)



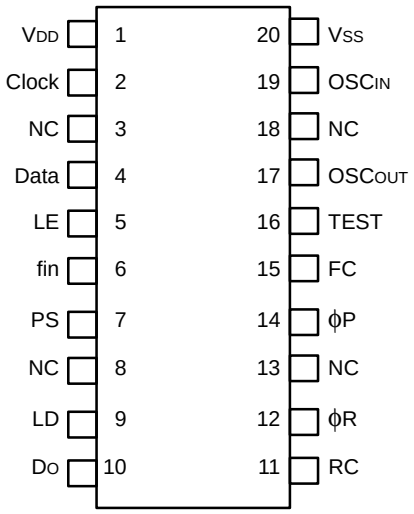
PIN ASSIGNMENT

(TOP VIEW)



(DIP-16P-M04)
(FPT-16P-M06)

(TOP VIEW)



(FPT-20P-M03)

PIN DESCRIPTIONS

Pin No.		Symbol	I / O	Description
DIP /SOP	SSOP			
1	1	V_{DD}	–	Power supply pin.
2	2	Clock	I	Clock input to the shift register. Each rise of the clock shifts one bit of the data into the shift register. The input portion contains a Schmitt trigger circuit.
–	3	NC	–	No Connection.
3	4	Data	I	Serial data input for programmable divider and programmable reference divider. The input portion contains a Schmitt trigger circuit.
4	5	LE	I	Load Enable signal input pin. A high on this pin transfers the contents of the shift register into the latch. The latched data provides the divide ratios of the dividers. The input portion contains a Schmitt trigger circuit.
5	6	fin	I	Input to the programmable divider. The input portion contains a bias circuit and an amplifier. This pin is connected to an external voltage controlled oscillator (VCO) with an AC coupling.
6	7	PS	I	Power save control input pin. A high on this pin places the MB87091 into the active mode and a low into the stand by mode. Pin PS has to be set low at power–on time (see Section 1.1, “Intermittent Operation,” in “Functional Descriptions”).
–	8	NC	–	No Connection.
7	9	LD	O	Phase comparator output pin. LD outputs high when the PLL is locked and low when the PLL is unlocked.
8	10	Do	O	Phase comparator output pin. The output current of this charge pump is adjustable with external resistor R_{RC}. The D_O output may be inverted by FC input. The relationships between the programmable reference divider output fr and the programmable divider output fp are shown below; fr > fp: “H” level (FC = “L”), “L” level (FC = “H”) fr = fp: High impedance fr < fp: “L” level (FC = “L”), “H” level (FC = “H”)
9	11	RC	–	Connect pin with an external resistor R_{RC} (see Section 1.4, ”Phase Comparator” in “Functional Descriptions”).
10	12	ϕR	O	Phase comparator output pin (for external charge pump). The relationships between the programmable reference divider output fr and the programmable divider output fp are shown below; When FC = “L” fr > fp: ϕR = “L” level fr = fp: ϕR = “L” level fr < fp: ϕR = “H” level When FC = “H” fr > fp: ϕR = “H” leve fr = fp: ϕR = “L” level fr < fp: ϕR = “L” level
–	13	NC	–	No Connection.

PIN DESCRIPTIONS

Pin No.		Symbol	I / O	Description
DIP /SOP	SSOP			
11	14	ϕP	O	Phase comparator output pin (for external charge pump). ϕP is an Nch, open–drain output. The relationships between the programmable reference divider output fr and the programmable divider output fp are shown below; When FC = "L" fr > fp: ϕP = "L" level fr = fp: ϕP = High impedance fr < fp: ϕP = High impedance When FC = "H" fr > fp: ϕP = High impedance fr = fp: ϕP = High impedance fr < fp: ϕP = "L" level
12	15	FC	I	Phase comparator input selector pin (see Section 1.4, "Phase Comparator" in "Functional Descriptions").
13	16	TEST	I	This is used to enable test mode. A high on this pin places the MB87091 into the test mode. As this pin is provided with a pull–down resistor, it should be left open as a rule. The pin is used for shipping tests and not used for normal operation.
14	17	OSC_{OUT}	O	Crystal oscillator connect pin.
–	18	NC	–	No connection.
15	19	OSC_{IN}	I	Crystal oscillator connect pin. A crystal oscillator is connected between OSC_{IN} and OSC_{OUT} pins. Can clock input to OSC_{IN} from the external. In this case pin OSC_{IN} must be AC coupled and pin OSC_{OUT} must be left open.
16	20	V_{SS}	–	Ground pin.

FUNCTIONAL DESCRIPTIONS

1. Circuit Description

1.1 Intermittent Operation

The intermittent operation of the MB87091 refers to the process of activating and deactivating its internal circuit as necessary thus saving power dissipation otherwise consumed by the circuit. If the circuit is simply restarted from the stand by state, however, the phase relationship between the reference frequency (fr) and the programmable frequency (fp), which are the input to the phase comparator, is not stable even when they are of the same value. This may cause the phase comparator to generate an excessively large error signal, resulting in an out–of–synch lock frequency.

To preclude the occurrence of this problem, the MB87091 has an intermittent mode control circuit which forces the frequencies into phase synchronization with each other when the MB87091 is reactivated, thus minimizing the error signal and resultant lock frequency fluctuations. The intermittent mode control circuit is controlled by the PS pin. Setting pin PS high provides the normal operation mode and setting the pin low provides the standby mode and places the MB87091 into the stand by state. The MB87091 behavior in the active and stand by modes is summarized below.

- Active mode (PS = “H”)
  All MB87091 circuits are active and provide the normal PLL operation.

- Stand by mode (PS = “L”)
  The circuits that consume power heavily and cause little inconvenience when deactivated run down, and MB87091 enters the low power dissipation state. D_O, ϕR, ϕP, and LD pins take the same state as when the PLL is locked. D_O pin becomes high–impedance state and the input voltage to the voltage controlled oscillator (VCO) is maintained at the same level as is in active mode (lock state) according to a time constant of a low pass filter (LPF). Consequently, the output frequency from the VCO (f_{VCO}) is maintained at approximately the lock frequency.

  The MB87091 continues the intermittent mode operation by alternating the active and stand by modes. When it switches from stand by to active modes, it forces the phase of fr and fp to correspond for minimizing the error signal. In this way, the MB87091 can keep the power dissipation of its entire circuitry to the minimum.

  The MB87091 must be placed into the stand by mode (PS = “L”) when it is powered on.

1.2 Programmable Divider

The f_{VCO} input through fin pin is divided by the programmable divider and then output to the phase comparator as fp. It consists of a dual modulus prescaler, a 6–bit binary swallow counter, a 12–bit binary programmable counter, and a controller which controls the divide ratio of the prescaler.

Divide ratio range:

- Prescaler: M = 64, M+1 = 65
- Swallow counter: A = 0 to 63
- Programmable counter: N = 5 to 4095

The MB87091 uses the pulse swallow method; consequently, the divide ratios of the swallow and programmable counters must satisfy the relationship N > A.

The total divide ratio of the programmable divider is calculated as follows:

Total divide ratio = (M+1)xA+Mx(N–A) = MxN+A = 64xN+A

When N is set within $5 \leq N \leq 63$, the possible divide ratio A of the swallow counter can take values $0 \leq A \leq N–1$ because N must be greater than A. For example, $0 \leq A \leq 19$ is allowed when N = 20 but $20 \leq A \leq 63$ is not allowed in that case. Consequently, $N \geq 64$ must be satisfied for the total divisor to be set within $0 \leq A \leq 63$.

The fp and fin have the following relationship:

$fp = fin \div (64 \times N + A)$

1.3 Programmable Reference divider

The programmable reference divider divides the reference oscillation frequency (f_{OSC}) from the crystal oscillator connected between OSC_{IN} and OSC_{OUT} pins or from the external oscillator input taken in directly through OSC_{IN} pin, then, sends the resultant fr to the phase comparator. It consists of a 14–bit binary programmable reference counter. When the output from the external oscillator is to be input directly to OSC_{IN}, pin the connection must be AC coupled and OSC_{OUT} pin is left open. Also, to prevent OSC_{OUT} from malfunctioning, its traces on the printed circuit board must be kept minimal or eliminated entirely; whenever possible, it must be free of any form of load.

The following divisor is used:

- Programmable reference counter: N = 5 to 16383

The fr and f_{OSC} have the following relationship:

- $fr = f_{OSC} \div R$

1.4 Phase Comparator

The phase comparator detects the phase difference between the outputs fr and fp from the dividers and generates an error signal that is proportional to the phase difference. The outputs from the phase comparator include 1) D_O which takes on one of the three states, namely, “L” (low), “H” (high), and “Z” (high impedance), and is sent to the LPF, 2) ϕR, 3) ϕP, and 4) LD which indicates the PLL lock or unlock state.

1.4.1 Phase Comparator

The phase comparator detects the phase difference between fr and fp and generates an error signal that is proportional to the phase difference. The roles of the fr and fp supplied to the phase comparator may be reversed by switching the logical input level on FC pin. This inverts the logical level on the D_O output. The logical level on D_O output may be selected according to the characteristics of the external LPF and the VCO. (Refer to Table 1.)

Table 1 Phase Comparator Inputs/Output Relationships

Phase Relationship \ Output	FC=“L”			FC=“H”		
	D_O	ϕR	ϕP	D_O	ϕR	ϕP
fr > fp	H	L	L	L	H	Z
fr = fp	Z	L	Z	Z	L	Z
fr < fp	L	H	Z	H	L	L

1.4.2 Charge Pump

The charge pump is available in two forms: internal and external.

- Internal constant–current charge pump output (D_O)
- External charge pump outputs (ϕR, ϕP)

The output current at D_O pin from the internal constant–current charge pump is controlled by varying the external resistance (R_{RC}) connected between RC and GND as shown in Figure 1.

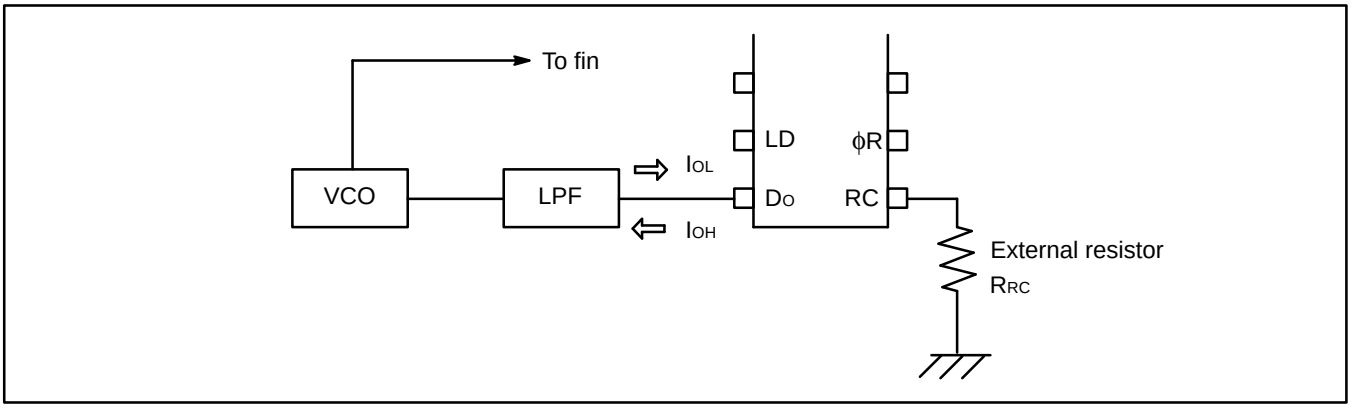
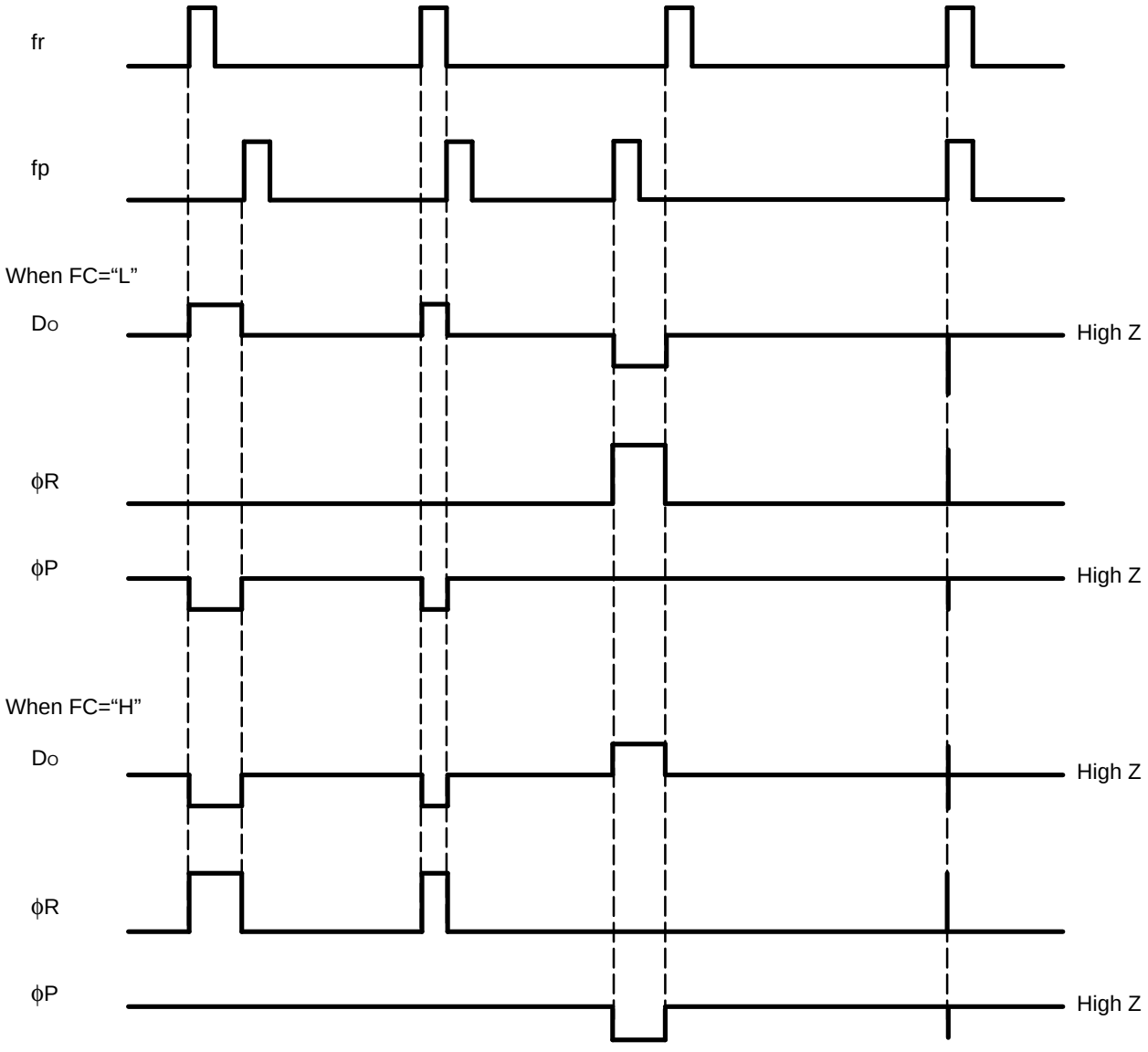


Figure 1 Constant–current Charge Pump

1.4.3 Phase Comparator Input/Output Waveforms

The phase comparator outputs logic levels summarized in Table 1, according to the phase difference between fr and fp phase differences. Note that ϕP is an Nch open drain output. The pulse width of the phase comparator outputs are identical and equal to the phase difference between fr and fp as shown in Figure 2.

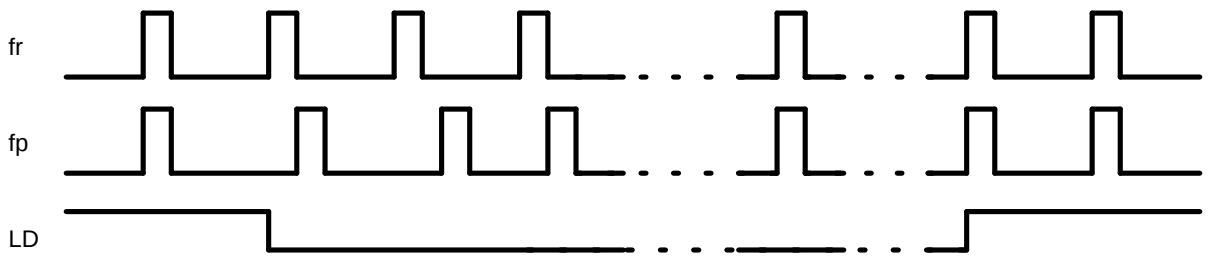
Figure 2 Phase Comparator Input/Output Waveforms (Charge Pump)



1.4.4 Lock Detector

The lock detector detects the lock and unlock states of the PLL. The lock detector outputs “H” when the PLL enters the lock state and outputs “L” when the PLL enters the unlock state as shown in Figure 3. When PS = “L”, the lock detector outputs “H” compulsorily.

Figure 3 Phase Comparator Input/Output Waveform (Lock Detector)



2. Setting the Divide Ratio

2.1 Serial Data Format

The format of the serial data is shown in Figure 4. The serial data is composed of a control bit and divide ratio setting data. The control bit selects the programmable divider or programmable reference divider.
In case of the programmable divider, serial data consists of 18 bits (6 bits for the swallow counter and 12 bits for the programmable counter) and 1 control bit as shown in Figure 4.1. In case of the programmable reference divider, the serial data consists of 14 divisor bits and 1 control bit as shown in Figure 4.2.
The control bit is set to 0 to identify the serial data for the programmable divider and to 1 to select the serial data for the programmable reference divider.

Figure 4 Serial Data Format

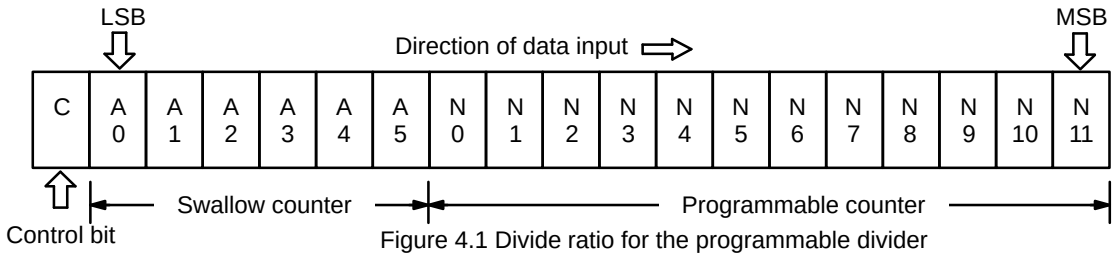


Figure 4.1 Divide ratio for the programmable divider

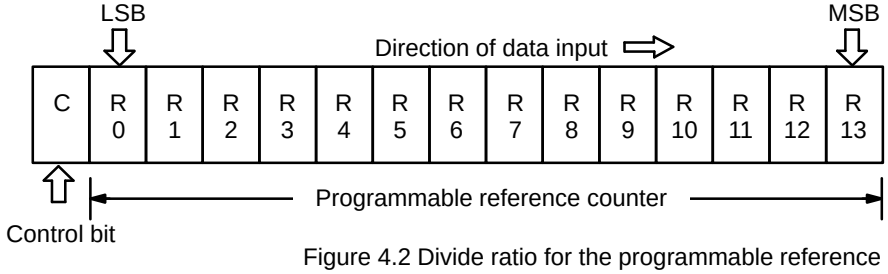
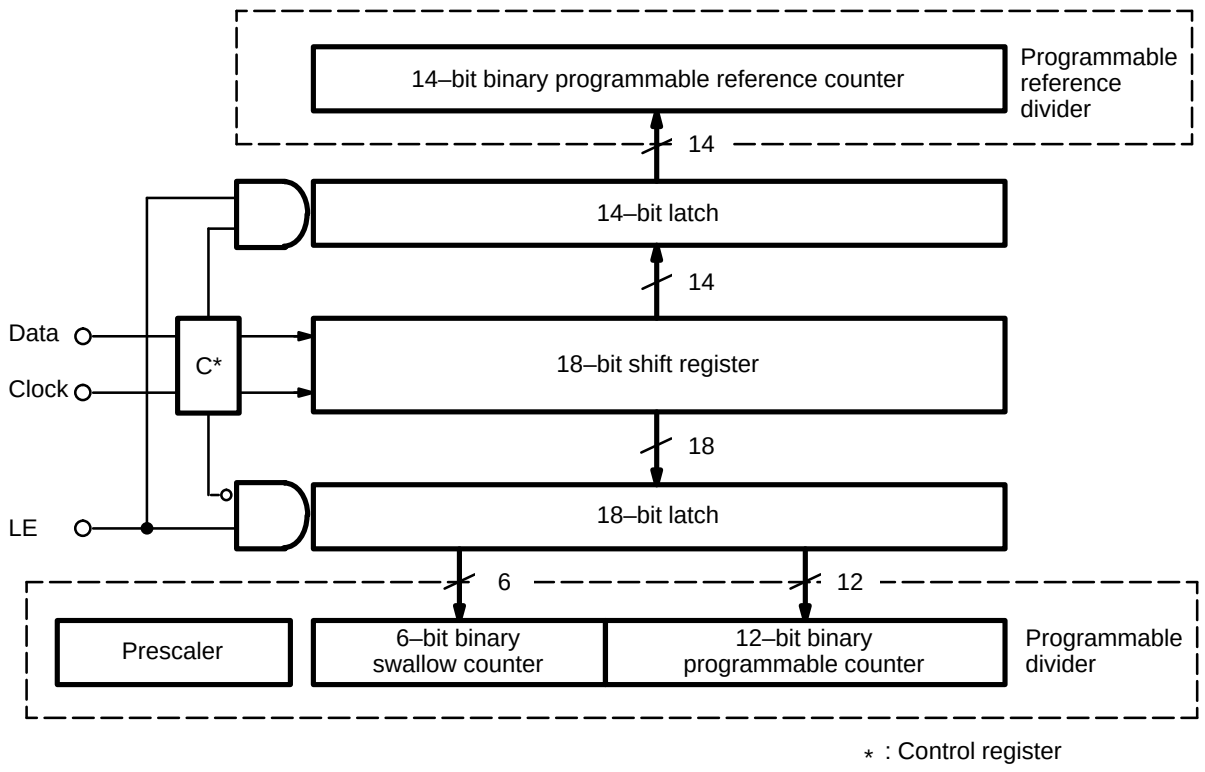


Figure 4.2 Divide ratio for the programmable reference divider

2.2 The Flow of Serial Data

Serial data is received via data pin in synchronization with the Clock input and loaded into shift register which contains the divide ratio setting data and into the control register which contains the control bit. The logical product (through the AND gate in Figure 5) of LE and the control register output (i.e., control bit) is fed to the Enable input of the latches. Accordingly, when LE is set high, the latch for the divider identified by the control bit is enabled and the divide ratio data from the shift register is loaded into the selected counter(s).

Figure 5 The Flow of Serial Data



2.3 Setting the Divide Ratio for the Programmable Divider

Columns A0 to A5 of Table 2.1 represent the divide ratio of the swallow counter and columns N0 to N11 of Table 2.2 represent the divide ratio of the programmable counter. The control bit is set to 0.

Table 2 Divide Ratio for the Divider

Table 2.1 Swallow Counter Divisor A

Divide ratio A	A 0	A 1	A 2	A 3	A 4	A 5
0	0	0	0	0	0	0
1	1	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •
63	1	1	1	1	1	1

Table 2.2 Programmable Counter Divisor N

Divide ratio N	N 0	N 1	N 2	N 3	N 4	N 5	N 6	N 7	N 8	N 9	N 10	N 11
5	1	0	1	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
4095	1	1	1	1	1	1	1	1	1	1	1	1

2.4 Setting the Divide Ratio for the Programmable Reference Divider

Columns R0–R13 of Table 3 represent the divide ratio of the programmable reference counter. The control bit is set to 1.

Table 3 Divide Ratio for the Reference Divider

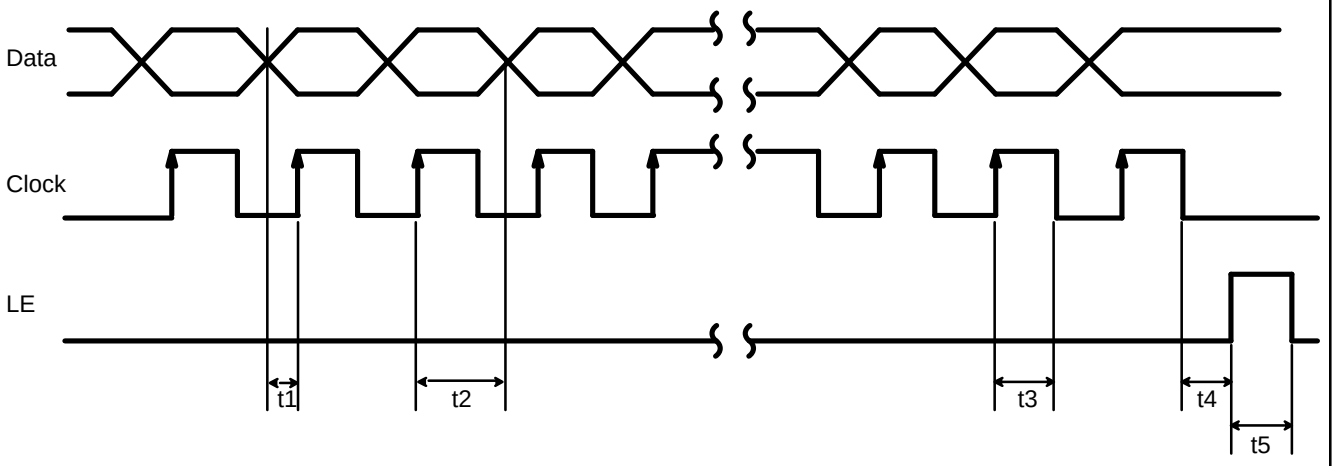
Divide ratio R	R 0	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11	R 12	R 13
5	1	0	1	0	0	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.5 Serial Data Input Timing

The MB87091 uses 19 bits of serial data for the programmable divider and 15 bits for the programmable reference divider. When more bits of serial data than defined for the target divider are received, only the last valid serial data bits are effective.
To set the divide ratio for the MB87091 dividers, it is necessary to supply the Data, Clock, and LE signals at the timing shown in Figure 6.

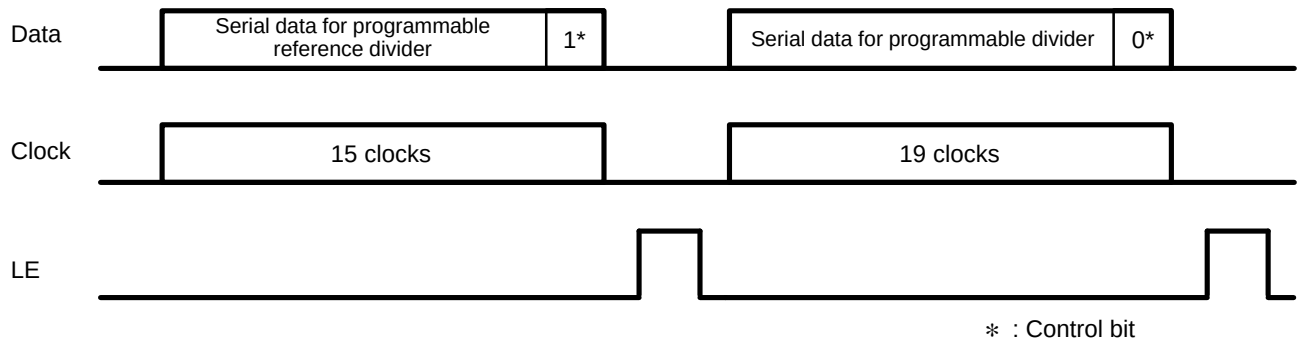
t1 (≥1 µs) : Data setup time t2 (≥1 µs): Data hold time t3 (≥1 µs): Clock pulse width
t4 (≥1 µs) : LE setup time to the fall edge of last clock t5 (≥1 µs): LE pulse width

Figure 6. Serial Data Input Timing



Since the divide ratios are unpredictable when the MB87091 is turned on, it is necessary to initialize the divide ratio for both dividers at power–on time. As shown in Figure 7, after setting the divide ratio for one divider (e.g., programmable reference divider), set LE to the "H" level before setting the divide ratio for the other divider (e.g., programmable divider). To change the divide ratio of one divider after initialization, input the serial data only for that divider (the divide ratio for the other divider is preserved).

Figure 7 Inputting Serial Data (Setting Divisors)



RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	2.7 to 3.3	V
Input voltage	V_{IN}	V_{SS} to V_{DD}	V
Ambient temperature	T_A	–40 to +60	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = –40 to +60°C)

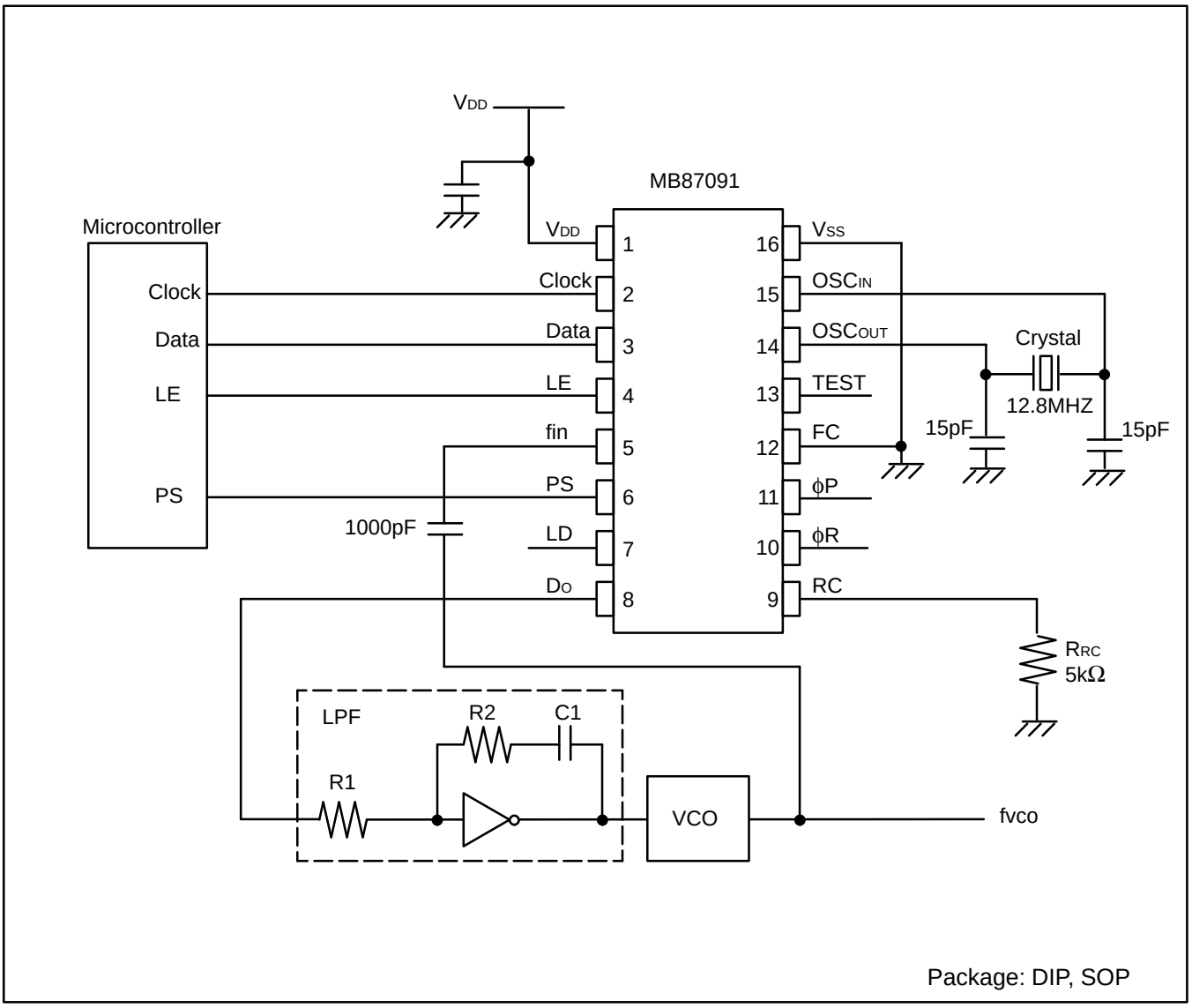
Parameter			Symbol	Conditions	Value			Unit
					Min	Typ	Max	
Input voltage	Except fin & OSC_{IN}	H level	V_{IH}		2.1	–	–	V
		L level	V_{IL}		–	–	0.9	
Input sensitivity	fin		Vf_{PP}	AC coupling amplitude	1.0	–	–	V_{P-P} Sine
	OSC_{IN}		Vsin	AC coupling amplitude	1.0	–	–	
Input current	Except fin, OSC_{IN} & TEST	H level	I_{IH}	$V_{IN} = V_{DD}$	–	–	1.0	µA
		L level	I_{IL}	$V_{IN} = V_{SS}$	–	–	–1.0	
	fin		Ifin	$V_{IN} = V_{SS}$ to V_{DD}	–	±30	–	µA
	OSC_{IN}		I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}	–	±30	–	µA
	TEST		I_{TEST}	$V_{IN} = V_{DD}$	–	50	–	µA
Output voltage	Except OSC_{OUT}	H level	V_{OH}	I_{OH} = 0µA	2.95	–	–	V
		L level	V_{OL}	I_{OL} = 0µA	–	–	0.05	
	OSC_{OUT}	H level	V_{OH}	I_{OH} = 0µA	2.50	–	–	V
		L level	V_{OL}	I_{OL} = 0µA	–	–	0.50	
Output current	Except OSC_{OUT}, D_O & ϕP	H level	I_{OH}	V_{OH} = 2.5V	–0.5	–	–	mA
		L level	I_{OL}	V_{OL} = 0.5V	0.5	–	–	
	D_O only	H level	I_{OH}	V_{OH} = 2.5V ∗1	–	–2.0	–	mA
		L level	I_{OL}	V_{OL} = 0.5V ∗1	–	2.0	–	
	ϕP only	L level	I_{OL}	V_{OL} = 0.5V	0.5	–	–	mA
Cutoff current		D0 only	Ioff1	$V_{OUT} = V_{SS}$ to V_{DD}	–1.0	–	1.0	µA
		ϕP only	Ioff2	$V_{OUT} = V_{DD}$	–	–	1.0	
Supply current		Active mode	I_{DDOP}	∗2	–	8	16	mA
		Stand–by mode	I_{DDS}	∗3	–	10	–	µA
Maximum operating frequency		REF section	fmaxd	Programmable reference divider	40	–	–	MHz
		PD section	fmaxp	Programmable divider	300	–	–	

∗1: R_{RC} = 5 kΩ

∗2: f_{IN} = 300 MHz. 12.8 MHz crystal is connected between OSC_{IN} and OSC_{OUT} pins. R_{RC} = 5 kΩ. Inputs are connected to GND, except f_{IN}, OSC_{IN}, and TEST. Outputs are open.

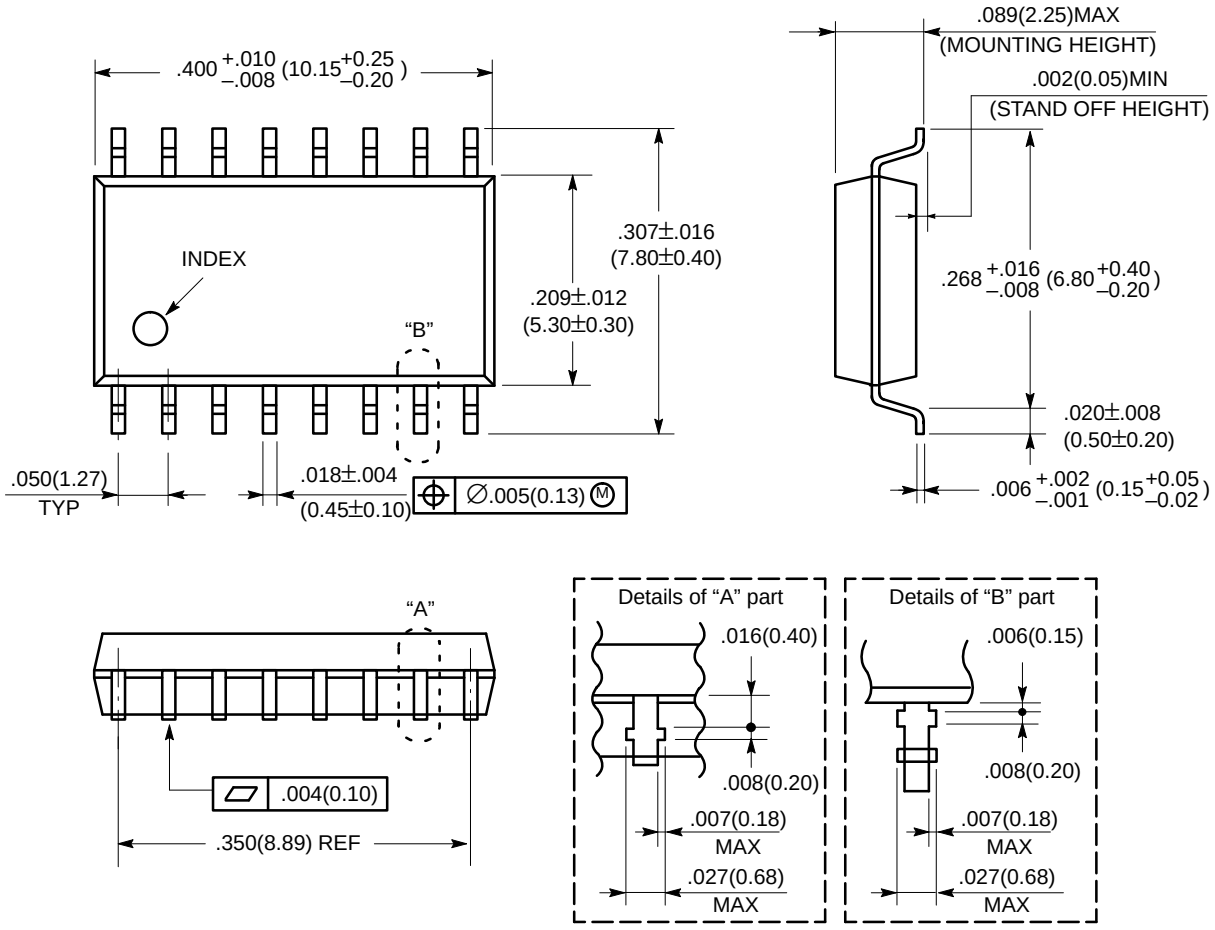
∗3: Current consumption at PS = "L". Inputs are connected to GND, except f_{IN}, OSC_{IN}, and TEST pins. Outputs and RC pin are open.

TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

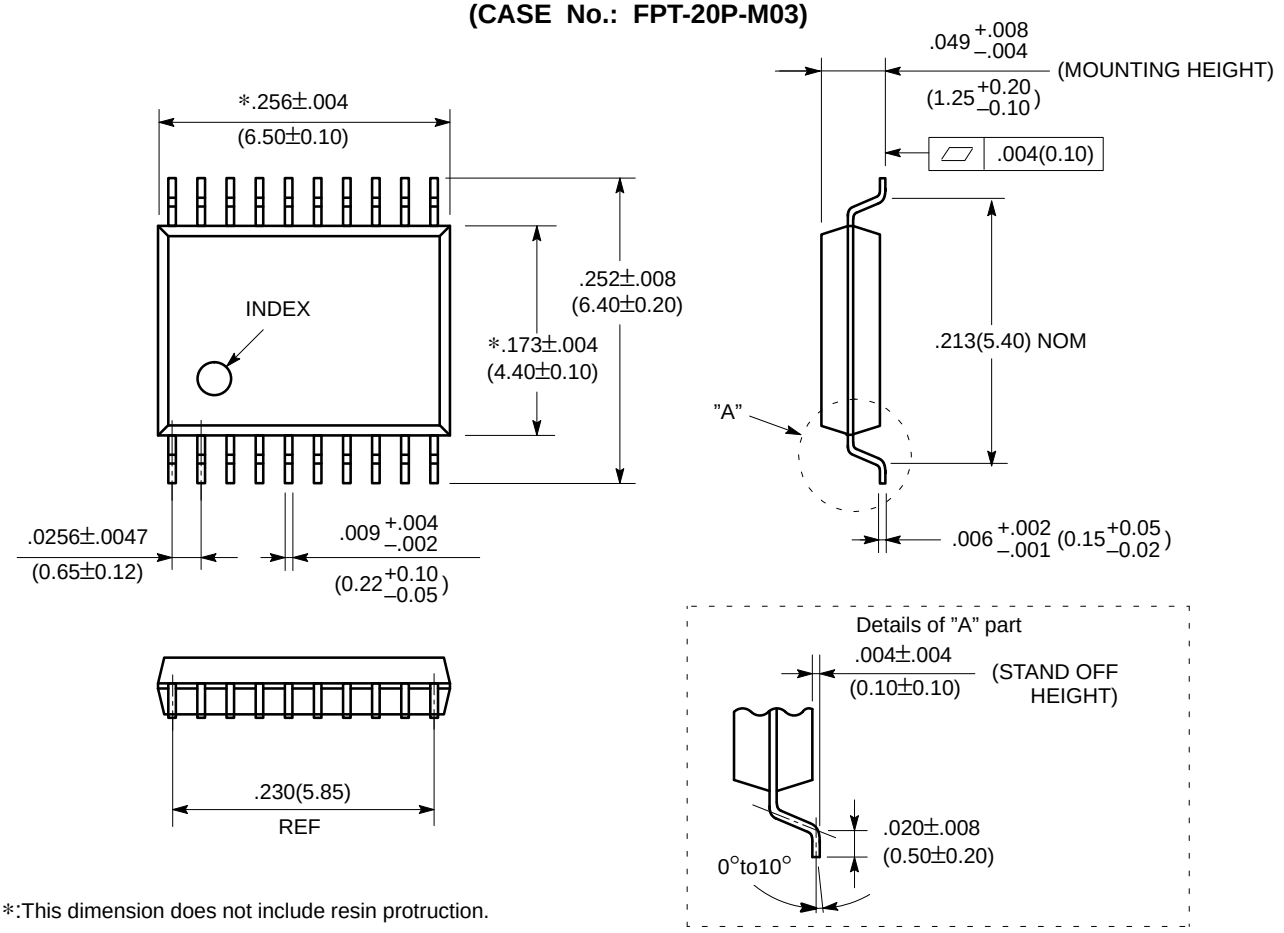
16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (CONTINUED)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in
inches (millimeters)

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Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete Information sufficient for construction purposes is not necessarily given.

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