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FUJITSU

APPLICATION NOTES

PCML I/Os

0.50 MICRON ASIC FAMILY

1.0 INTRODUCTION

As CMOS technology advances to deep sub-micron channel lengths, the internal core is now able to operate at system clock speeds greater than 100 MHz. With the proliferation of high speed, wide bus designs, system designers are now seeking to transfer large amounts of data at 100 Mb/s or above. This application note describes the PCML (Pseudo Current Mode Logic) I/O buffers, available for Fujitsu's 0.5 micron CE/CG51 High Performance ASIC family. These high speed buffers are capable of operating at frequencies in excess of 250 MHz.

These buffers can easily be customized for specific applications, both the center (or reference) voltage, and voltage swing are fully adjustable. This wide range of adjustment is a unique feature and allows Fujitsu's PCML I/O buffers to be used to interface with other types of I/Os, e.g. PECL, LVTTL, etc.

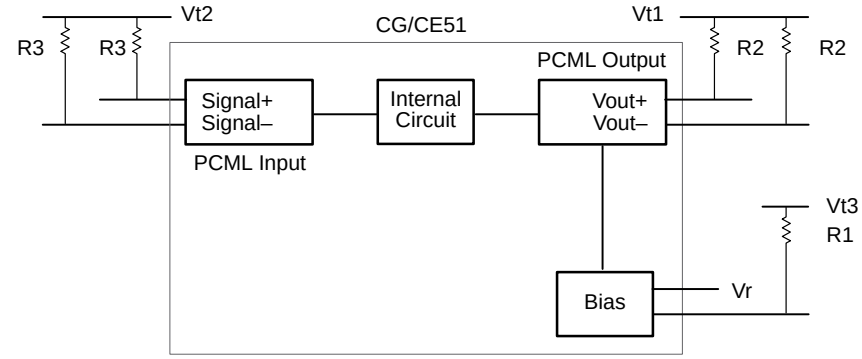
2.0 PCML I/O CIRCUIT OVERVIEW

A typical PCML I/O interface circuit is shown in Fig. 1, with external components R1, R2, and R3, and supplied voltages Vt1,Vt2, Vt3 and Vr., Single ended PCML input buffer can be implemented by connecting Signal– to an external reference voltage, Vref, through a Vref pin. Only Vref pin can supply the reference voltage to the PCML input buffers. At present, there is no plan for offering a single ended PCML output buffer.

The on-chip bias circuits are used to generate the necessary reference voltages for the PCML output buffers. The bias circuits consist of a main bias circuits and local bias circuits. One main bias circuit can support up to 14 local bias circuits. Each PCML output has one local bias circuit.

Each individual PCML input buffer has a terminal (C) to turn off the short circuit current for I_{DDS} testing. This terminal (C) will be set at low level for the normal operation, and will be set at high during the I_{DDS} test. For this reason, a dedicated external input pin and a dedicated input buffer, GIVTESTI, is required when PCML input buffers are used. Connections to terminal (C)'s of PCML input buffers are automatic, and these connections will not be shown in the schematic or netlist.

External components and external supplied voltages are required for the PCML output buffers. R1 and R2 are termination resistors connected to Vt. For 50 Ω transmission line, 50 Ω resistors are used at the receiving end, or 100 Ω resistors are used at both ends of a bus line.



VOH = Vt1
VOL = Vr, if R1 = R2
VOL = if 2Vr – Vt1, R1 = R2/2

Fig. 1. A typical PCML I/O Interface Circuit Connection

3.0 PCML I/O OPTIONS

There are 3 types of PCML I/O buffers available:

a. Single-ended Input Buffer with separate Vref input.

b. Differential Input Buffer.

c. Differential Output Buffer, 50 Ω termination termination.

3.1 Interface Levels for PCML Input Buffers

Each type of input buffer has 3 options for Vcenter values: 1.3V, 1.6V and 2.0V. They are intended for the following interfaces:

Vcenter = 1.3V: optimized for interfacing with other Fujitsu ASICs with PCML I/O buffers.

Vcenter = 1.6V: CTT (Center Tap Termination) levels, e.g. T-LVTTL levels.

Vcenter = 2.0V: PECL levels.

3.2 Interfacing Levels for PCML Output Buffers

V_{OL} and V_{OH} levels can be set as follows:

V_{OH} = Vt1

V_{OL} = Vr, for Vt1 = Vt3 and R1 = R2

V_{OL} = 2Vr – Vt1 for Vt1 = Vt3 and R1 = R2/2

Fig. 2 shows an example of a PCML output interfacing with T-LVTTL input of another chip.

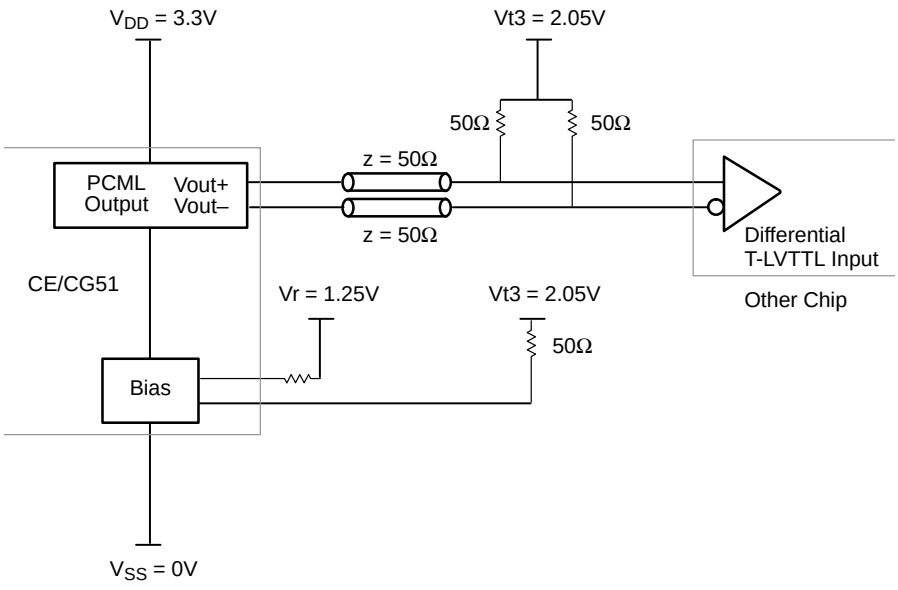


Fig. 2. Example of PCML output interfacing with a T-LVTTL input

4.0 ELECTRICAL CHARACTERISTICS

The following conditions are used unless noted otherwise:

V_{DD} = 3.3 V, Tj = 25 °C.

The DC levels are expected not to vary with supply voltage, temperature and process variations. They follow Vt1, Vt2, Vt3, Vr and the external components R1 and R2. The variations of these external parameters are expected to be about ±100 mV.

4.1 Differential/Single–Ended Input (Vcenter = 1.3V)

DC Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Input Voltage Swing	Vswing	300	400 or 800	V_{DD}	mV	
Input High Voltage	V_{IH}	1.35	1.4 or 1.6	V_{DD}	V	
Input Low Voltage	V_{IL}	V_{SS}	1.0 or 0.8	1.05	V	
Reference Voltage	Vref	1.25	1.3	1.35	V	Single-Ended
Input Leak Current	I_{LI}	–10		10	µA	
Input Capacitance	C_{IN}	2		4	pF	excluding package

4.2 Differential/Single–Ended Input (Vcenter = 1.6V)

DC Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Input Voltage Swing	Vswing	300	400 or 800	V_{DD}	mV	
Input High Voltage	V_{IH}	1.75	1.8 or 2.0	V_{DD}	V	
Input Low Voltage	V_{IL}	V_{SS}	1.4 or 1.2	1.45	V	
Reference Voltage	Vref	1.55	1.6	1.65	V	Single-Ended
Input Leak Current	I_{LI}	–10		10	µA	
Input Capacitance	C_{IN}	2		4	pF	excluding package

4.3 Differential/Single–Ended Input (Vcenter = 2.0V)

DC Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Input Voltage Swing	Vswing	300	400 or 800	V_{DD}	mV	
Input High Voltage	V_{IH}	2.15	2.2 or 2.4	V_{DD}	V	
Input Low Voltage	V_{IL}	V_{SS}	1.8 or 1.6	1.85	V	
Reference Voltage	Vref	1.95	2.0	2.05	V	Single-Ended
Input Leak Current	I_{LI}	–10		10	µA	
Input Capacitance	C_{IN}	2		4	pF	excluding package

4.4 Differential Output

DC Parameter	Symbol	Min.	Typ.	Max.	Unit
Output Voltage Swing	Vswing	300	400 or 800	850	mV
Terminal Voltage	V_T	1.40		2.40	V
Terminal Resistor	R_T		50		Ω
Output High Voltage	V_{OH}	V_T–0.05 (I_{OH}=1mA)		V_T+0.05 (I_{OH}=–1mA)	V
Output Low Voltage	V_{OL}	V_T–0.8 (I_{OL}=16mA)		V_T–0.4 (I_{OL}=8mA)	V

4.5 Bias Input

DC Parameter	Symbol	Min.	Typ.	Max.	Unit
Bias (Low)	Vilow	0.8		1.8	V
Bias (Dummy)	Dummy	Vilow (Min)		Vilow (Max)	V

5.0 ADDITIONAL COMMENTS

This application note presents a brief overview of Fujitsu's PCML I/Os. For further details, consult with your local Fujitsu field application engineer or contact FMI's (Fujitsu Microelectronics, Inc.) ASIC Design Center at (408)456–1000.

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