DS04–28309–2E

FUJITSU

DATA SHEET

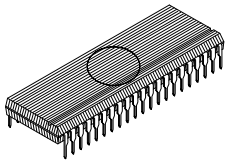
ASSP
TV/VCR D/A CONVERTER
MB86029

The MB86029 is a 3–channel high-speed CMOS 8–bit D/A converter for TV and VCR application. The MB86029 features on–chip voltage reference, pedestal insertion, and power-down circuits, and a maximum conversion speed of 60 MSPS for digital TV and graphic display application.

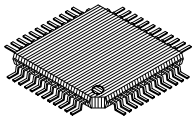
- Functions
  Maximum conversion speed: 60 MSPS max.
  Current output mode
  Output current adjusted by external resistor
  Pedestal insertion
  Power-down function
  On-chip reference power supply (External reference power supply can be used.)
- Conversion

Characteristic	Load resistance		
	37.5 Ω	**75 Ω**	**150 Ω**
Output voltage amplitude	0.80 V	1.60 V	1.60 V
Conversion speed	60 MSPS	30 MSPS	20 MSPS

- Supply voltage
  Single +5 V supply
- Current consumption
  Typical stage: 500 mW
  Power-down mode: 20 mW max.



PLASTIC PACKAGE
(DIP-42P-M01)



PLASTIC PACKAGE
(FPT-48P-M02)

ABSOLUTE MAXIMUM RATINGS (See NOTE) (V_{SSD} = V_{SSA} = 0 V, T_a= +25°C)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD} *	–0.3 to +7.0	V
Analog supply current	I_{DDA}	–10 to +200	mA
Analog ground current	I_{SSA}	–10 to +50	mA
Digital supply current	I_{DDD}	–200 to +10	mA
Digital ground current	I_{SSD}	–10 to +50	mA
Analog output current	I_O	–10 to +30	mA
Digital input/output current	$I_{I/O}$	–10 to +10	mA
Input/output voltage	$V_{I/O}$	–0.3 to V_{DD} +0.3	V
Storage temperature	T_{stg}	–40 to +125	°C

∗ : V_{DD} = V_{DDD} = V_{DDA}

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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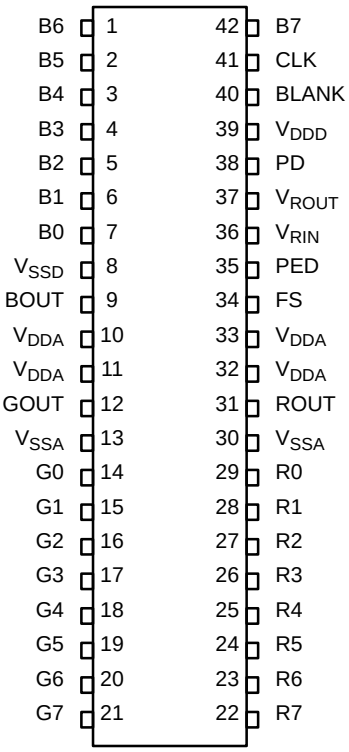
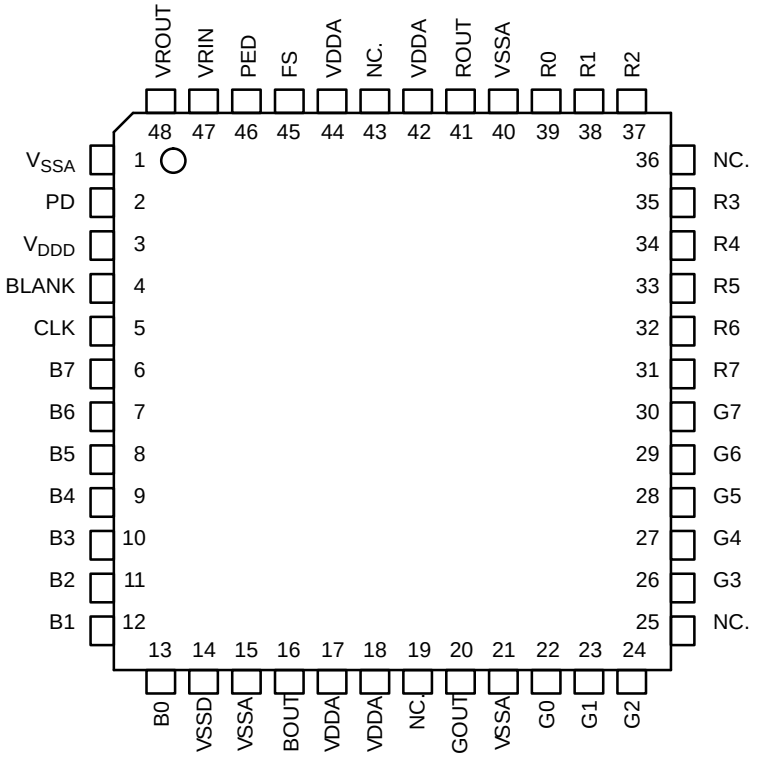
PIN ASSIGNMENT

(TOP VIEW)



(DIP-42P-M01)

(TOP VIEW)

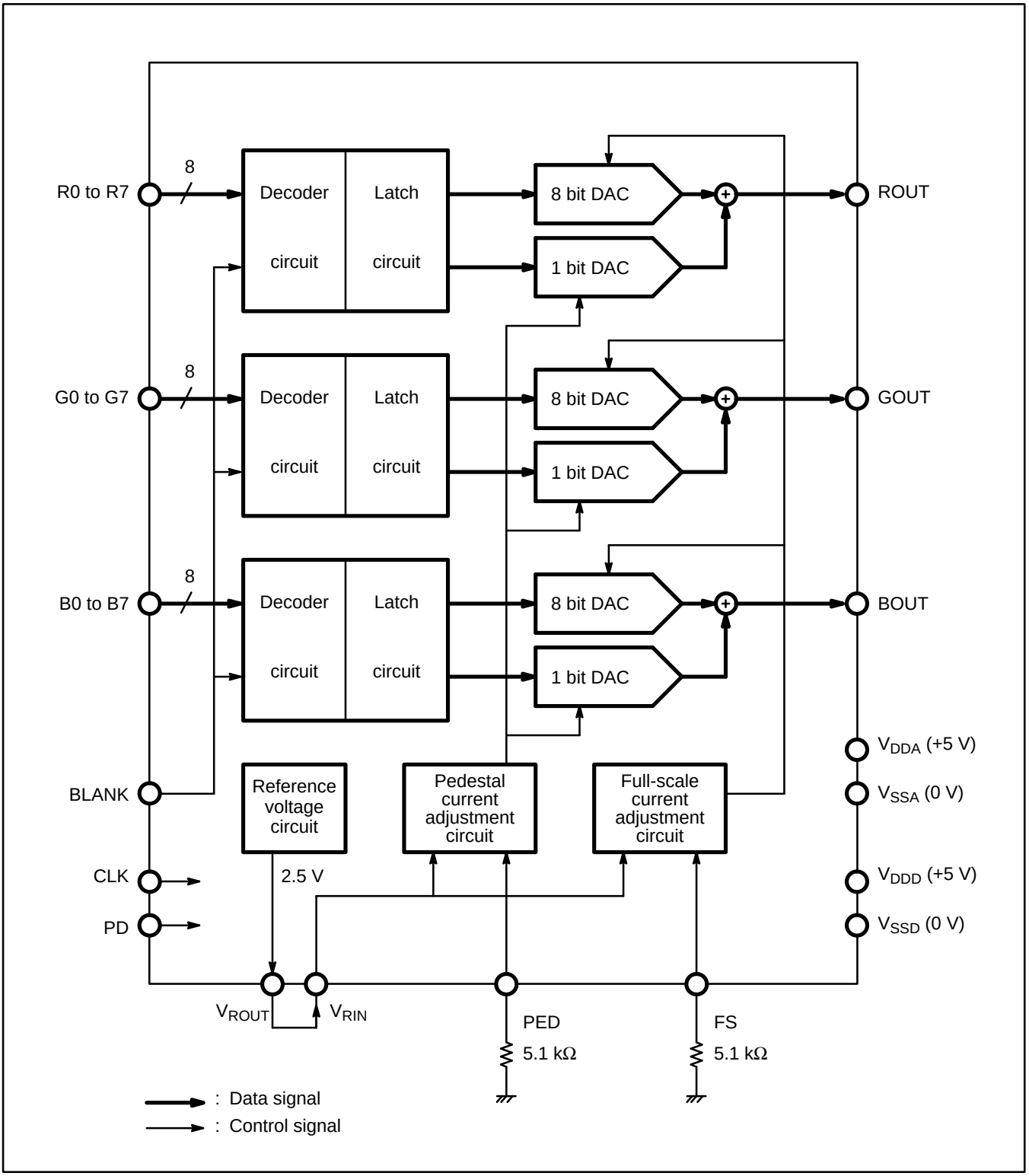


(FPT-48P-M02)

PIN DESCRIPTIONS

Circuit	Pin NO.		Symbol	I/O	Pin Name	Function
	DIP	FPT				
Power supply circuit	10, 11, 32, 33	17, 18, 42, 44	V_{DDA}	–	Analog power supply	Analog power supply +5V
	13, 30	1, 15, 21, 40	V_{SSA}	–	Analog ground	Analog power supply ground
	39	3	V_{DDD}	–	Digital power supply	Digital power supply +5 V
	8	14	V_{SSD}	–	Digital ground	Digital power supply ground
Input circuit	22 to 29	39 to 37, 35 to 31	R0 to R7	I	Digital signal input	Digital signal input.
	14 to 21	22 to 24, 26 to 30	G0 to G7	I		
	1 to 7, 42	13 to 6	B0 to B7	I		MSB : R7, G7, B7 LSB : R0, G0, B0
	38	2	PD	I	Power-down control	High : Power-down mode Low : Operating
	41	5	CLK	I	Clock input	Data is read in, and analog signal is output on the falling edge of the CLK.
	40	4	BLANK	I	Pedestal control	High : Pedestal output Low : No pedestal
	36	47	V_{RIN}	I	External voltage reference	For connection of an external reference voltage (2.5 V typ.)
Output circuit	31	41	ROUT	O	Analog output	Analog RGB output
	12	20	GOUT	O		
	9	16	BOUT	O		
	34	45	FS	O	Full-scale current adjustment	The full-scale current is adjusted by an external resistor connected between this pin and the GND pin.
	35	46	PED	O	Pedestal current adjustment	The pedestal current is adjusted by an external resistor connected between this pin and the GND pin.
	37	48	V_{ROUT}	O	Reference voltage output	On-chip 2.5 V reference output

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

(V_{SSD} = V_{SSA} = 0 V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply voltage	V_{DD} *	4.75	5.00	5.25	V
Reference supply input voltage	V_{RIN}	2.2	2.5	2.8	V
Low-level digital input voltage	V_{IL}	0	–	0.8	V
High-level digital input voltage	V_{IH}	2.2	–	V_{DD}	V
Ambient operating temperature	T_{op}	0	25	70	°C

∗ : V_{DD} = V_{DDD} = V_{DDA}

DC CHARACTERISTICS

(V_{DD} * = 4.75 to 5.25 V, V_{RIN} = 2.5 V, V_{SSD} = V_{SSA} = 0 V, T_a= 0°C to +70°C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Nonlinearity	LE	See the table below for conditions 1	–	–	±1	LSB
Differential linearity	DE	See the table below for conditions 1	–	–	±1	LSB
Full-scale current	I_{FS}	See the table below for conditions 1	18.0	20.0	22.0	mA
		See the table below for conditions 2	18.0	20.0	22.0	
		See the table below for conditions 3	9.2	10.2	11.2	
Pedestal current	I_{PED}	See the table below for conditions 1	1.12	1.25	1.38	mA
		See the table below for conditions 2	1.12	1.25	1.38	
		See the table below for conditions 3	0.57	0.64	0.71	
Channel to channel matching error	DM	I_{FS} average variation between channels under Condition 1	–	–	5.0	%FSR
Output voltage range	V_{OC}	–	0	–	1.6	V
Supply current	I_D	See the table below for conditions 1	–	100	120	mA
		See the table below for conditions 2	–	100	120	
		See the table below for conditions 3	–	60	70	
Reference output voltage	V_{ROUT}	–	2.4	2.5	2.6	V

∗ : V_{DD} = V_{DDD} = V_{DDA}

- **Output voltage setting conditions**

Conditions	Output voltage amplitude	R_{FS} *	R_{PED} *	Load resistance	Maximum conversion speed
Condition 1 (Typical condition)	0.8 V	5.1 kΩ	5.1 kΩ	37.5 Ω	60 MSPS
Condition 2	1.6 V	5.1 kΩ	5.1 kΩ	75 Ω	30 MSPS
Condition 3	1.6 V	10 kΩ	10 kΩ	150 Ω	20 MSPS

∗ : The output voltage amplitude can be adjusted with slight changes in external resistances.

AC CHARACTERISTICS

(V_{DD} * = 4.75 to 5.25 V, V_{RIN} = 2.5 V, V_{SSD} = V_{SSA} = 0 V, T_a = 0°C to +70°C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Output rise time	t_r	–	–	–	2	ns
Output fall time	t_f	–	–	–	2	ns
High-level pulse width	t_{WH}	–	6	–	–	ns
Low-level pulse width	t_{WL}	–	6	–	–	ns
Clock signal period	t_{ck}	–	16.6	–	–	ns
Setup time	t_{su}	–	8	–	–	ns
Hold time	t_h	–	2	–	–	ns
Output propagation deley time	t_d	–	–	20	–	ns
Settling time	t_s	See the table below for conditions 1	–	15	–	ns
		See the table below for conditions 2	–	30	–	
		See the table below for conditions 3	–	50	–	
Output transition time	t_{TLH}	See the table below for conditions 1	–	–	6	ns
		See the table below for conditions 2	–	–	12	
		See the table below for conditions 3	–	–	20	
Output trasition time	t_{THL}	See the table below for conditions 1	–	–	6	ns
		See the table below for conditions 2	–	–	12	
		See the table below for conditions 3	–	–	20	

∗ : V_{DD} = V_{DDD} = V_{DDA}

- **Output voltage setting conditions**

Conditions	Output voltage amplitude	R_{FS} *	R_{PED} *	Load resistance	Maximum conversion speed
Condition 1 (Typical condition)	0.8 V	5.1 kΩ	5.1 kΩ	37.5 Ω	60 MSPS
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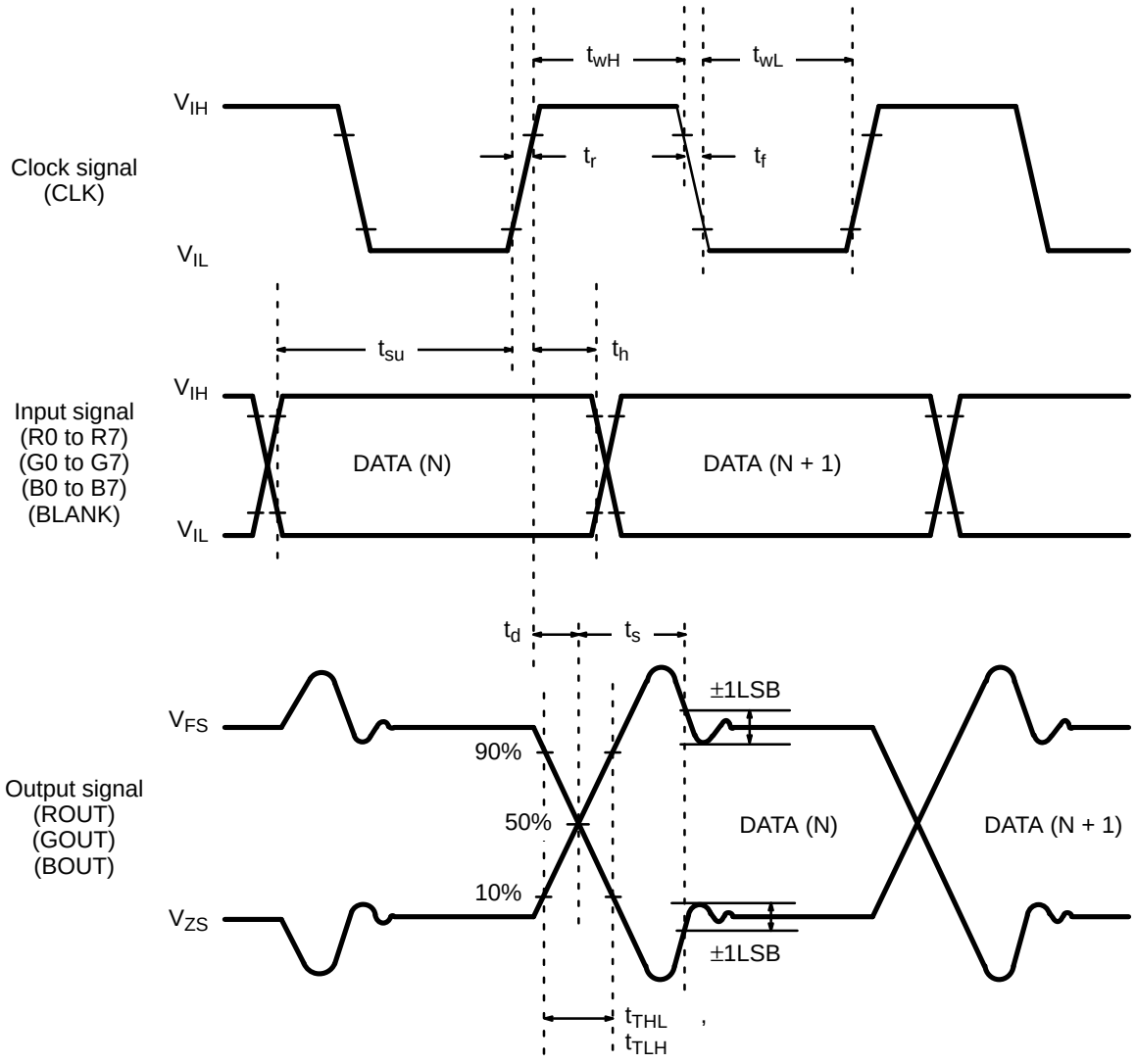
∗ : The output voltage amplitude can be adjusted with slight changes in external resistances.

TIMING CHART



Note: R0 to R7, G0 to G7, B0 to B7 are read on the rising edge of the clock.

OUTPUT VOLTAGE CALCULATION

The DAC output voltage can be calculated from the load resistance, external resistors, and reference voltage values.

$$V_O\ [mV] = R_L\ [\Omega] \times \left(\frac{K_{FS}}{R_{FS}\ [k\Omega]} \times X + \frac{K_{PED}}{R_{PED}\ [k\Omega]} \times B\right) \times V_{RIN}\ [V]$$

X = $00 to $FF digital signal input code
B = 0 (Without Pedestal voltage)
= 1 (With pedestal voltage)
K_{FS} = 0.16 (Constant)
K_{PED} = 2.56 (Constant)
R_L = Load resistance
R_{FS} , R_{PED} = External resistors
V_{RIN} = Reference voltage

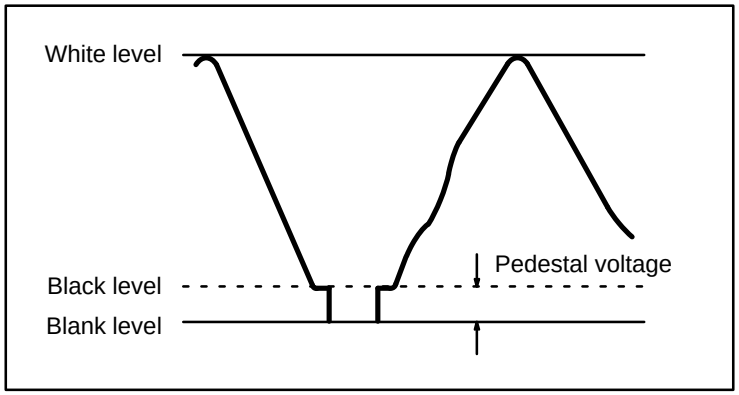
OUTPUT VOLTAGE CHARACTERISTICS

1. With pedestal

- Table of equation for output voltage code

Output voltage	Code	BLANK
800.0 mV	$FF	"H"
:	:	:
425.1 mV	$80	"H"
:	:	:
47.2 mV	$00	"H"
0.0 mV	$00	"L"

- Output waveform chart



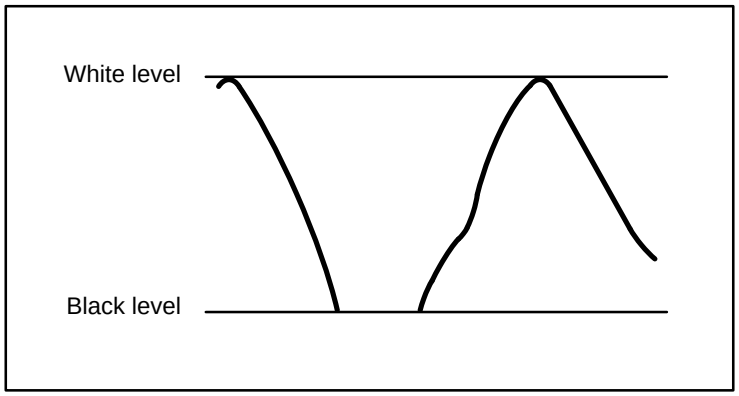
[Condition] $R_{FS} = R_{PED} = 5.1\ k\Omega$, $V_{RIN} = 2.5$ V, $R_L = 75\ \Omega$
(According to the above conditions, 1 LSB = approx. 3.0 mV)

2. Without pedestal

- Table of equation for output voltage code

Output voltage	Code	BLANK
752.8 mV	$FF	"L"
:	:	:
377.9 mV	$80	"L"
:	:	:
0.0 mV	$00	"L"

- Output waveform chart



[Condition] $R_{FS} = R_{PED} = 5.1\ k\Omega$, $V_{RIN} = 2.5$ V, $R_L = 75\ \Omega$
(According to the above conditions, 1 LSB = approx. 3.0 mV)

SPECIFICAITON OF ANALOG OUTPUT CURRENT

1. Pedestal current not output

Analog output current	Digital input code								
	D7	D6	D5	D4	D3	D2	D1	D0	BLANK
0	0	0	0	0	0	0	0	0	0
$I_{FS} \times \frac{1}{255}$	0	0	0	0	0	0	0	1	0
$I_{FS} \times \frac{2}{255}$	0	0	0	0	0	0	1	0	0
$I_{FS} \times \frac{3}{255}$	0	0	0	0	0	0	1	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$I_{FS} \times \frac{253}{255}$	1	1	1	1	1	1	0	1	0
$I_{FS} \times \frac{254}{255}$	1	1	1	1	1	1	1	0	0
$I_{FS} \times \frac{255}{255}$	1	1	1	1	1	1	1	1	0

I_{FS} : Full-scale current

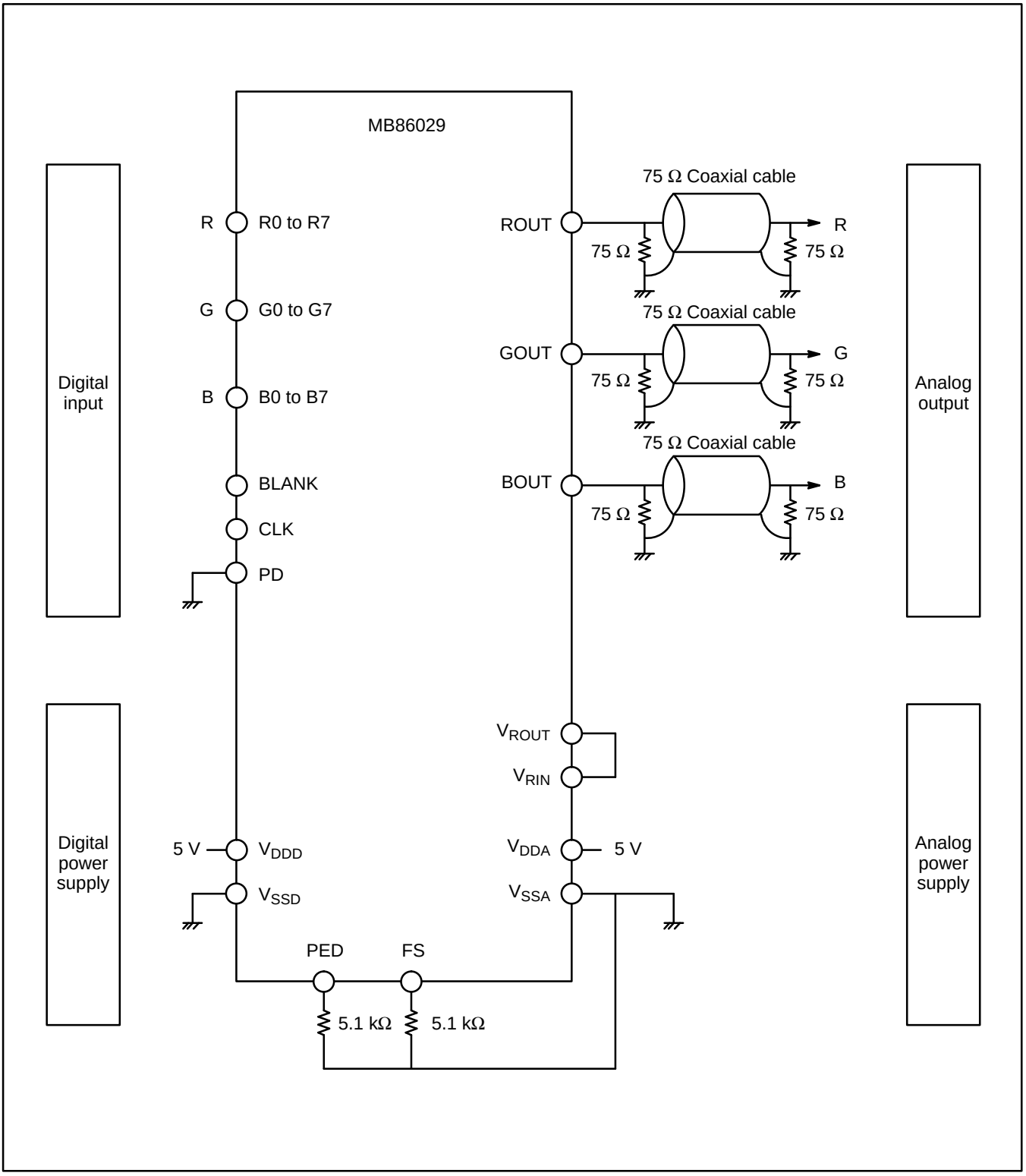
2. Pedestal current output

Analog output current	Digital input code								
	D7	D6	D5	D4	D3	D2	D1	D0	BLANK
I_{PED}	0	0	0	0	0	0	0	0	1
$I_{PED} + I_{FS} \times \frac{1}{255}$	0	0	0	0	0	0	0	1	1
$I_{PED} + I_{FS} \times \frac{2}{255}$	0	0	0	0	0	0	1	0	1
$I_{PED} + I_{FS} \times \frac{3}{255}$	0	0	0	0	0	0	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$I_{PED} + I_{FS} \times \frac{253}{255}$	1	1	1	1	1	1	0	1	1
$I_{PED} + I_{FS} \times \frac{254}{255}$	1	1	1	1	1	1	1	0	1
$I_{PED} + I_{FS} \times \frac{255}{255}$	1	1	1	1	1	1	1	1	1

I_{FS} : Full-scale current

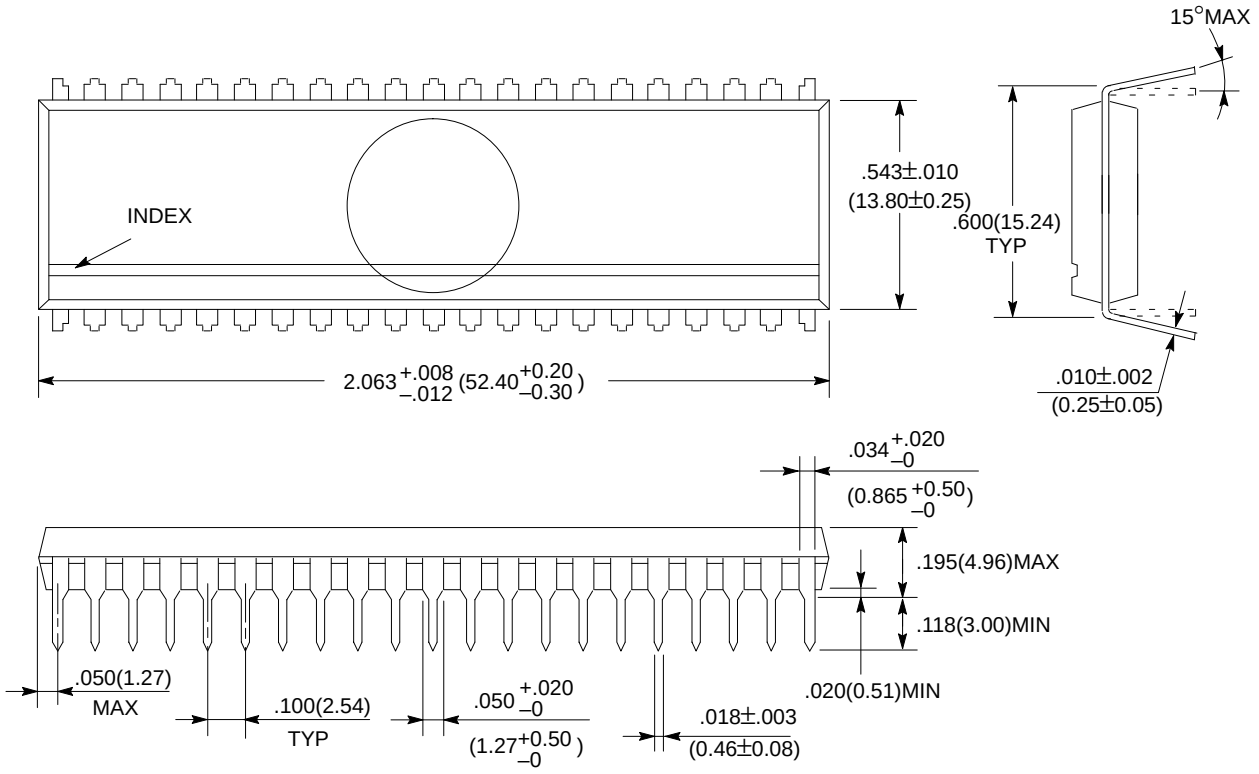
I_{PED} : Pedestal current

APPLICATION CIRCUIT



PACKAGE DIMENSIONS

42-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-42P-M01)



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Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS