FUJITSU

Fujitsu

64M Bit Synchronous DRAM

Target Spec

Target Specification

1095

MB81164441A/MB81164442A
MB81164421A/MB81164422A
64M BIT SYNCHRONOUS DRAM

Organization		4 banks x 4,194,304 words x 4 bits 2 bsnks x 8,386,608 words x 4 bits
Clock Frequency		125/100/83/67 MHz max.
Refrech Cycle		128ms/8,192cycles
Power Dissipation	(4banks) (2banks)	T.B.D T.B.D
Power Supply		3.3 ± 0.3 V

Fully Synchronous Operation
Referred To The Positive Clock Edge

LVTTL & SSTL* I/O Interface

* : Stub Series–Terminated Transceiver Logic
MB81164441A/MB81164421A Only

4 or 2 Banks Interleave Operation
With Bank Select (A12&A13 or A13)

Programmable Wrap Type And
Burst Length (1,2,4,8,&Full Column)

Auto–refresh & Self–refrsh

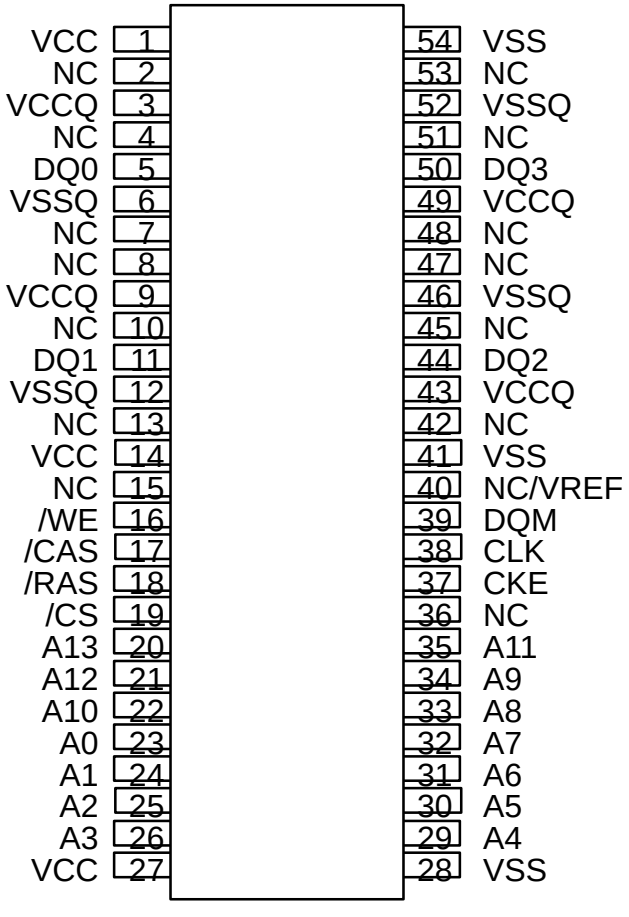
Clock Enable For Timing
Synchronization And Power Down

Input Data And Output Mask Option

Address

Row Address	A0–A10	(4 banks)
	A0–A11	(2 banks)
Column Address	A0–A10	
Bank Select	A12,A13	(4 banks)
	A13	(2 banks)

Package : 54pin TSOP Type–II Package
(400mil, 0.8mm Lead Pitch)



Pin Assignment
(Top View)

DYNAMIC RAM

Target Specification

1095

MB81164841A/MB81164842A
MB81164821A/MB81164822A
64M BIT SYNCHRONOUS DRAM

Organization		4 banks x 2,097,152 words x 8 bits 2 bsnks x 4,194,304 words x 8 bits
Clock Frequency		125/100/83/67 MHz max.
Refrech Cycle		128ms/8,192cycles
Power Dissipation	(4banks) (2banks)	T.B.D T.B.D
Power Supply		3.3 ± 0.3 V

Fully Synchronous Operation
Referred To The Positive Clock Edge

LVTTL & SSTL* I/O Interface

* : Stub Series–Terminated Transceiver Logic
MB81164841A/MB81164821A Only

4 or 2 Banks Interleave Operation
With Bank Select (A12&A13 or A13)

Programmable Wrap Type And
Burst Length (1,2,4,8,&Full Column)

Auto–refresh & Self–refrsh

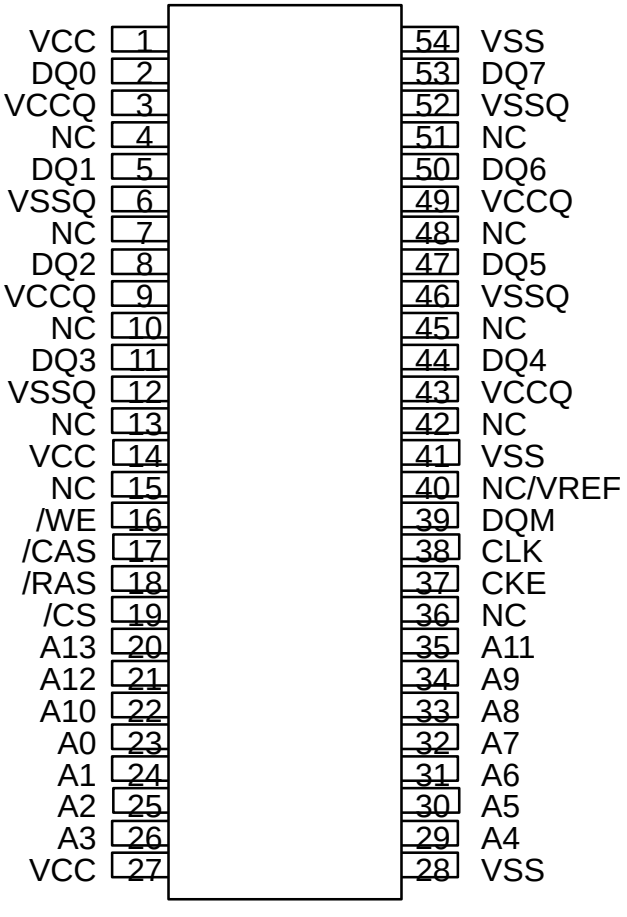
Clock Enable For Timing
Synchronization And Power Down

Input Data And Output Mask Option

Address

Row Address	A0–A10	(4 banks)
	A0–A11	(2 banks)
Column Address	A0–A9	
Bank Select	A12,A13	(4 banks)
	A13	(2 banks)

Package : 54pin TSOP Type–II Package
(400mil, 0.8mm Lead Pitch)



Pin Assignment
(Top View)

DYNAMIC RAM

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1095

MB811641641A/MB811641642A
MB811641621A/MB811641622A
64M BIT SYNCHRONOUS DRAM

Organization		4 banks x 1,048,576 words x 16 bits 2 banks x 2,097,152 words x 16 bits
Clock Frequency		125/100/83/67 MHz max.
Refrech Cycle		128ms/8,192cycles
Power Dissipation	(4banks)	T.B.D
	(2banks)	T.B.D
Power Supply		3.3 ± 0.3 V

Fully Synchronous Operation
Referred To The Positive Clock Edge

LVTTL & SSTL* I/O Interface

* : Stub Series–Terminated Transceiver Logic
MB811641641A/MB811641621A Only

4 or 2 Banks Interleave Operation
With Bank Select (A12&A13 or A13)

Programmable Wrap Type And
Burst Length (1,2,4,8,&Full Column)

Auto–refresh & Self–refrsh

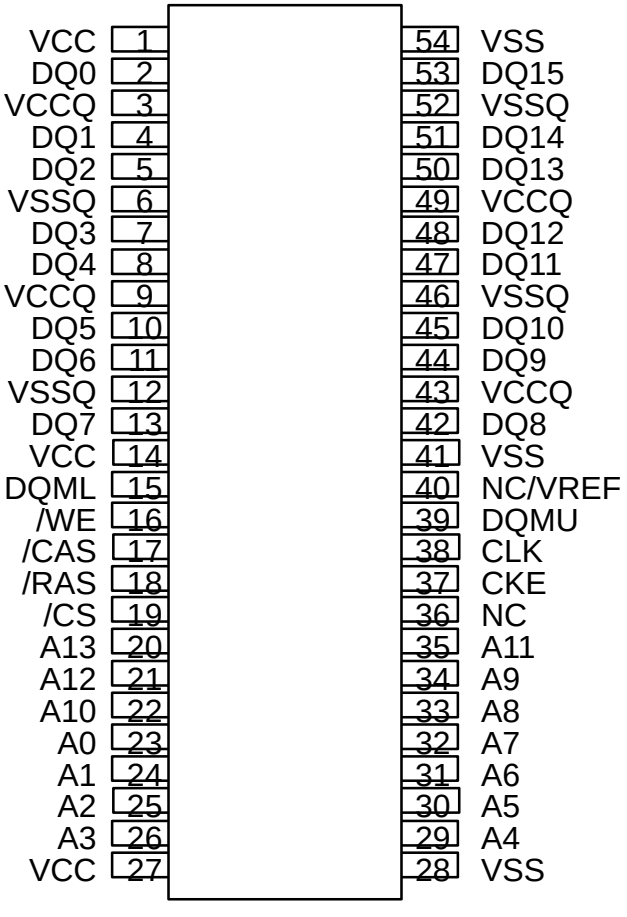
Clock Enable For Timing
Synchronization And Power Down

Input Data And Output Mask Option

Address

Row Address	A0–A10	(4 banks)
	A0–A11	(2 banks)
Column Address	A0–A8	
Bank Select	A12,A13	(4 banks)
	A13	(2 banks)

Package : 54pin TSOP Type–II Package
(400mil, 0.8mm Lead Pitch)



Pin Assignment
(Top View)

Target Specification

1095

MB811643241A/MB811643242A
MB811643221A/MB811643222A
64M BIT SYNCHRONOUS DRAM

Organization	4 banks x 524,288 words x 32 bits 2 banks x 1,048,576 words x 32 bits
Clock Frequency	125/100/83/67 MHz max.
Refrech Cycle	128ms/8,192cycles
Power Dissipation	(4banks) T.B.D (2banks) T.B.D
Power Supply	3.3 ± 0.3 V

Fully Synchronous Operation
Referred To The Positive Clock Edge

LVTTL & SSTL* I/O Interface

* : Stub Series–Terminated Transceiver Logic
MB811643241A/MB811643221A Only

4 or 2 Banks Interleave Operation
With Bank Select (A12&A13 or A13)

Programmable Wrap Type And
Burst Length (1,2,4,8,&Full Column)

Auto–refresh & Self–refrsh

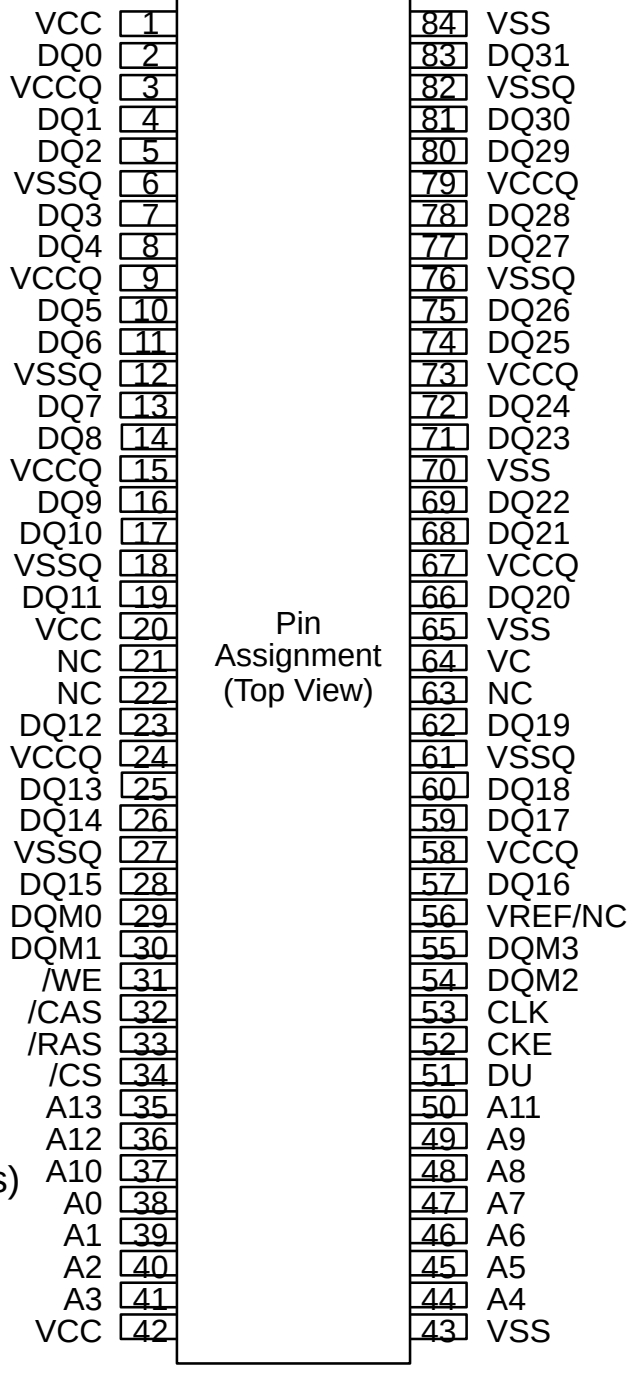
Clock Enable For Timing
Synchronization And Power Down

Input Data And Output Mask Option

Address

Row Address	A0–A10	(4 banks)
	A0–A11	(2 banks)
Column Address	A0–A7	(4 banks)
	A0–A7 or A0–A6	(2 banks)
Bank Select	A12,A13	(4 banks)
	A13	(2 banks)

Package : 84pin TSOP Type–II Package
(400mil, 0.5mm Lead Pitch)



DYNAMIC RAM

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