– PRELIMINARY –

November 1995
Edition 2.0

FUJITSU

PRODUCT PROFILE SHEET

MB81V4100C-60/-70

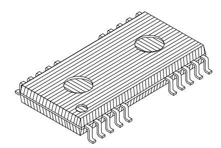
CMOS 4M X 1 BIT FAST PAGE MODE DRAM

CMOS 4,194,304 x 1 bit Fast Page Mode Dynamic RAM

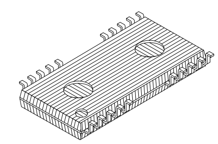
The Fujitsu MB81V4100C is a fully decoded CMOS Dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x1 configuration. The MB81V4100C features a ”fast page” mode of operation whereby high–speed random access of up to 4,096–bits of data within the same row can be selected. The MB81V4100C DRAM is ideally suited for mainframe, buffers, hand–held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81V4100C is very small, the device can be used as a non–volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81V4100C is fabricated using silicon gate CMOS and Fujitsu’s advanced four–layer polysilicon process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81V4100C are not critical and all inputs are LVTTL compatible.

Marking side



(Normal Bend)
FPT–26P–M01



Marking side

(Reverse Bend)
FPT–26P–M02

PRODUCT LINE & FEATURES

Parameter		MB81V4100C–60	MB81V4100C–70
$\overline{RAS}$ Access Time		60ns max.	70ns max.
$\overline{CAS}$ Access Time		15ns max.	20ns max.
Address Access Time		30ns max.	35ns max.
Randam Cycle Time		110ns min.	125ns min.
Fast Page Mode Cycle Time		40ns min.	45ns min.
Low Power Dissipation	Operating current	220 mW max.	195 mW max.
	Standby current	7.2mW max.(LVTTL level) / 3.6mW max.(CMOS level)	

- 4,194,304 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are LVTTL compatible
- 1024 refresh cycles every 16.4ms
- Self refresh function
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read–Modify–Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	–0.5 to +4.6	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	–0.5 to +4.6	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	Iout	–50 to +50	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

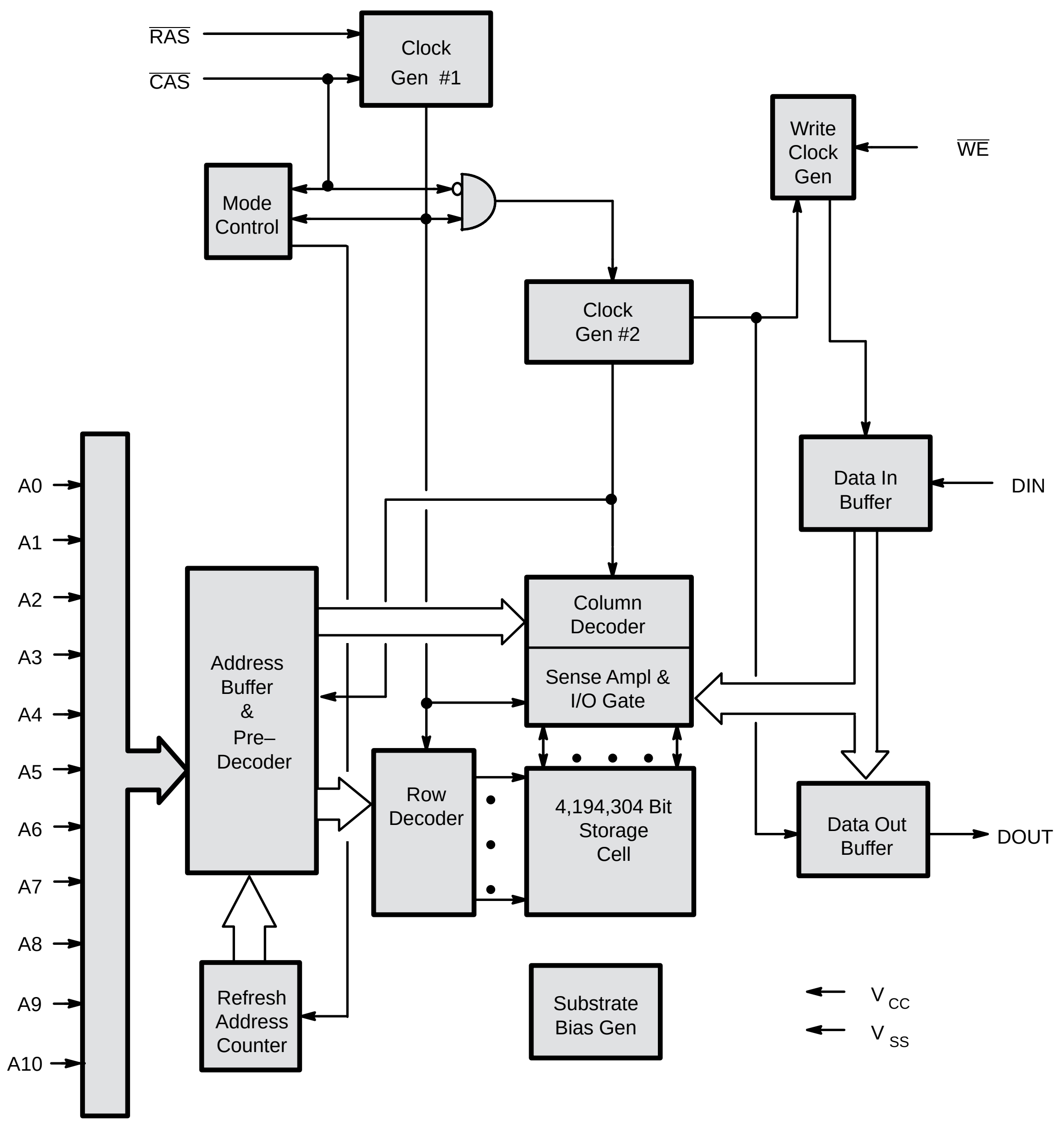
Package and Ordering Information

– 26–pin plastic (300mil) TSOP–II with normal bend leads, order as MB81V4100C–xxPFTN

– 26–pin plastic (300mil) TSOP–II with reverse bend leads, order as MB81V4100C–xxPFTR

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB81V4100C DYNAMIC RAM – BLOCK DIAGRAM

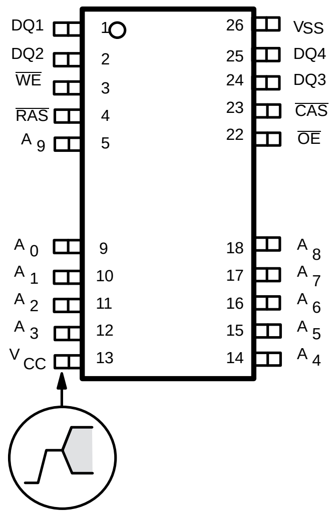


CAPACITANCE (T_A = 25°C, f = 1MHz)

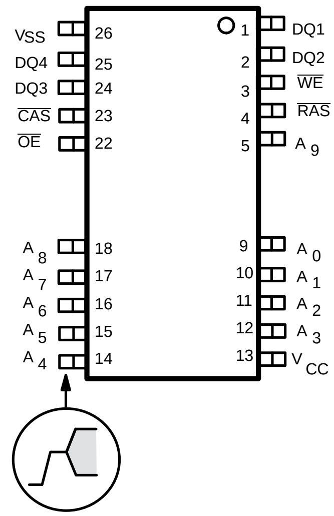
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10, DIN	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	7	pF
Output Capacitance, DOUT	C_{OUT}	—	7	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

26–Pin TSOP:
(TOP VIEW)
<Normal Bend : FPT–26P–M01>



26–Pin TSOP:
(TOP VIEW)
<Reverse Bend : FPT–26P–M02>



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{\text{WE}}$	Write Enable.
$\overline{\text{RAS}}$	Row address strobe.
A0 to A9	Address inputs.
VCC	+3.3 volt power supply.
$\overline{\text{OE}}$	Output enable.
$\overline{\text{CAS}}$	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	3.0	3.3	3.6	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.0	—	V_{CC}+0.3	V	
Input Low Voltage, all inputs*	1	VIL	–0.3	—	0.8	V	

*** :** Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty–two input bits are required to decode any one of 4,194,304 cell addresses in the memory matrix. Since only eleven address bits (A0–A10) are available, the column and row inputs are separately strobed by $\overline{RAS}$ and $\overline{CAS}$ as shown in Figure 5. First, eleven row address bits are applied on pins A0–through–A10 and latched with the row address strobe ($\overline{RAS}$) then, eleven column address bits are applied and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. the flow–through type latch is used for the address latches ; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of two basic ways—an early write cycle and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data is strobed by $\overline{CAS}$ and the setup/hold times are referenced to the falling edge of $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the falling edge of $\overline{WE}$.

DATA OUTPUT

The three–state buffers are LVTTL compatible with a fanout of one TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

t_{RAC} : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

t_{CAC} : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max).

The data remains valid until either $\overline{CAS}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 4,096–bits can be accessed and, when multiple MB 81V4100Cs are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready–modify–write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Paramter	Notes		Symbol	Conditions	Values			Unit
					Min	Typ	Max	
Output high voltage	1		V_{OH}	I_{OH} = –2mA	2.4	—	—	V
Output low voltage	1		V_{OL}	I_{OL} = 2mA	—	—	0.4	V
Input leakage current (any input)			$I_{I(L)}$	$0V \leq V_{IN} \leq 3.6V$ $3.0V \leq V_{CC} \leq 3.6V$ V_{SS} = 0V; All other pins not under test = 0V	–10	—	10	µA
Output leakage current			$I_{O(L)}$	$0V \leq V_{OUT} \leq 3.6V$ Data out disabled	–10	—	10	µA
Operating current (Average Power supply current)	2	MB81V4100C-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	61	mA
		MB81V4100C-70					54	
Standby current (Power supply current)		LVTTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
		CMOS level		$\overline{RAS}$ = $\overline{CAS}$ $\geq$ V_{CC} –0.2V			1.0	
Refresh current #1 (Average power supply current)	2	MB81V4100C-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	61	mA
		MB81V4100C-70					54	
Fast Page Mode current	2	MB81V4100C-60	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	41	mA
		MB81V4100C-70					37	
Refresh current #2 (Average power supply current)	2	MB81V4100C-60	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	49	mA
		MB81V4100C-70					44	
Refresh current #3 (Average power supply current)		MB81V4100C-60	I_{CC9}	$\overline{RAS}$ = VIL, $\overline{CAS}$ = VIL Self refresh ; t_{RASS} = min.	—	—	1000	µA
		MB81V4100C-70					1000	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V4100C-60 Min	MB81V4100C-60 Max	MB81V4100C-70 Min	MB81V4100C-70 Max	Unit
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	130	—	148	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	15	—	20	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	ns
7	Output Hold Time		t_{OH}	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	ns
10	Transition Time		t_{T}	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	45	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	20	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	20	50	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	15	10000	20	10000	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	17	t_{CPN}	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	ns
25	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	30	—	35	—	ns
26	Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	ns
29	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	ns
30	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
31	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	ns
32	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	18	—	ns
33	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	15	—	18	—	ns
34	DIN set Up Time		t_{DS}	0	—	0	—	ns
35	DIN Hold Time		t_{DH}	10	—	10	—	ns
36	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	60	—	70	—	ns
37	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	15	—	20	—	ns

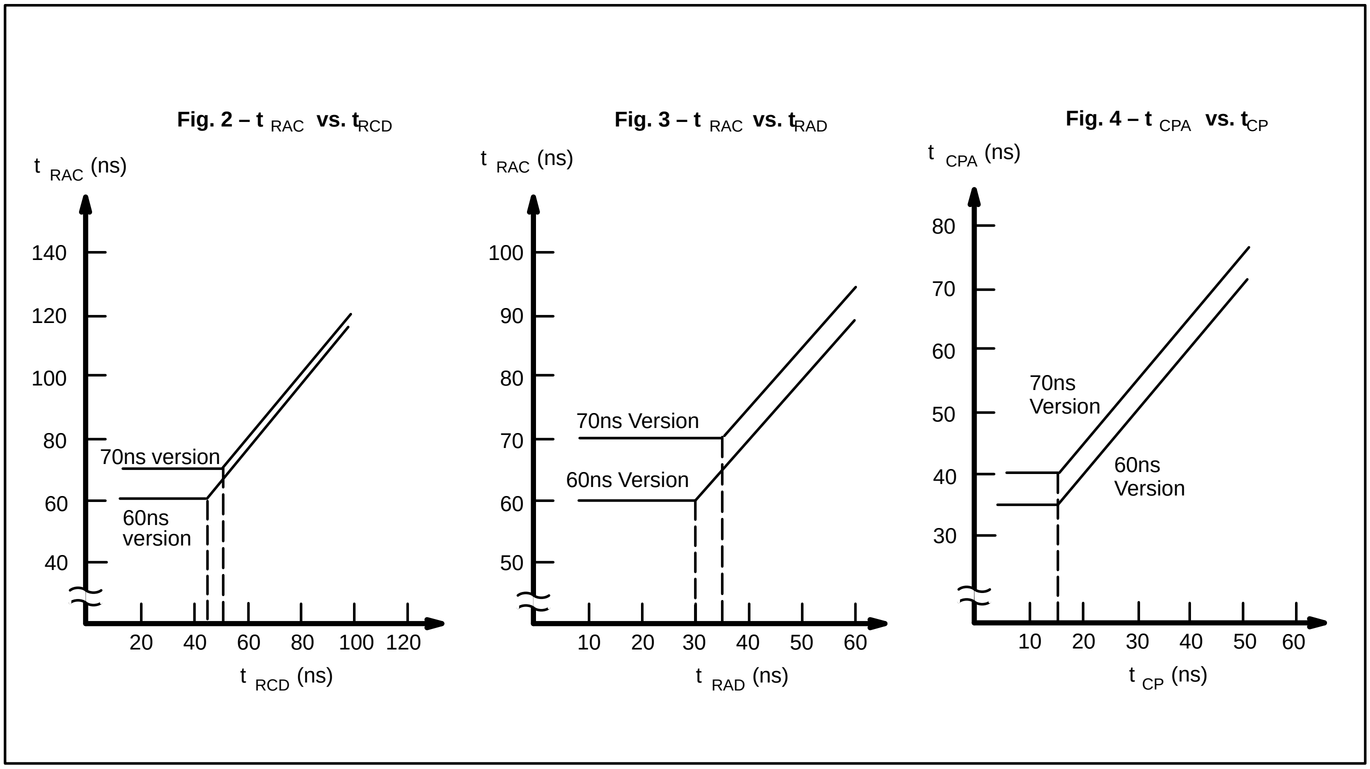
AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V4100C-60		MB81V4100C-70		Unit
				Min	Max	Min	Max	
38	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	30	—	35	—	ns
39	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	5	—	5	—	ns
40	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	ns
41	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	ns
42	$\overline{WE}$ SetUp Time from $\overline{RAS}$	18	t_{WSR}	0	—	0	—	ns
43	$\overline{WE}$ Hold Time from $\overline{RAS}$	18	t_{WHR}	10	—	10	—	ns
51	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	ns
52	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	60	—	68	—	ns
53	Access Time from $\overline{CAS}$ Precharge	9,16	t_{CPA}	—	35	—	40	ns
54	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	ns
55	Fast Page Mode $\overline{RAS}$ Pulse width		t_{RASP}	—	200000	—	200000	ns
56	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35	—	40	—	ns
57	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time		t_{CPWD}	35	—	40	—	ns

Notes:

1. Referenced to VSS
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   I_{CC} depends on the number of address change as $\overline{RAS}$= V_{IL} and $\overline{CAS}$= V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}$= V_{IL} and $\overline{CAS}$= V_{IH}.
   I_{CC4} is specified at one time of address change during one Page Cycle.
3. An Initial pause ($\overline{RAS}$=$\overline{CAS}$=VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$–only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$–before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. Input voltage levels are 0V and 3.0V, and input reference levels are V_{IH} (min) and V_{IL} (max) for measuring timing of input signals. Also, the transmission time (t_T) is measured between V_{IH} (min) and V_{IL} (max). The output reference levels are V_{OH}=2.0V and V_{OL}=0.8V.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to one TTL loads and 100 pF.
10. t_{OFF} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will appear at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, t_{CAL} and t_{RAL} specifications.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$–before–$\overline{RAS}$ refresh.
18. Assumes that Test mode function.



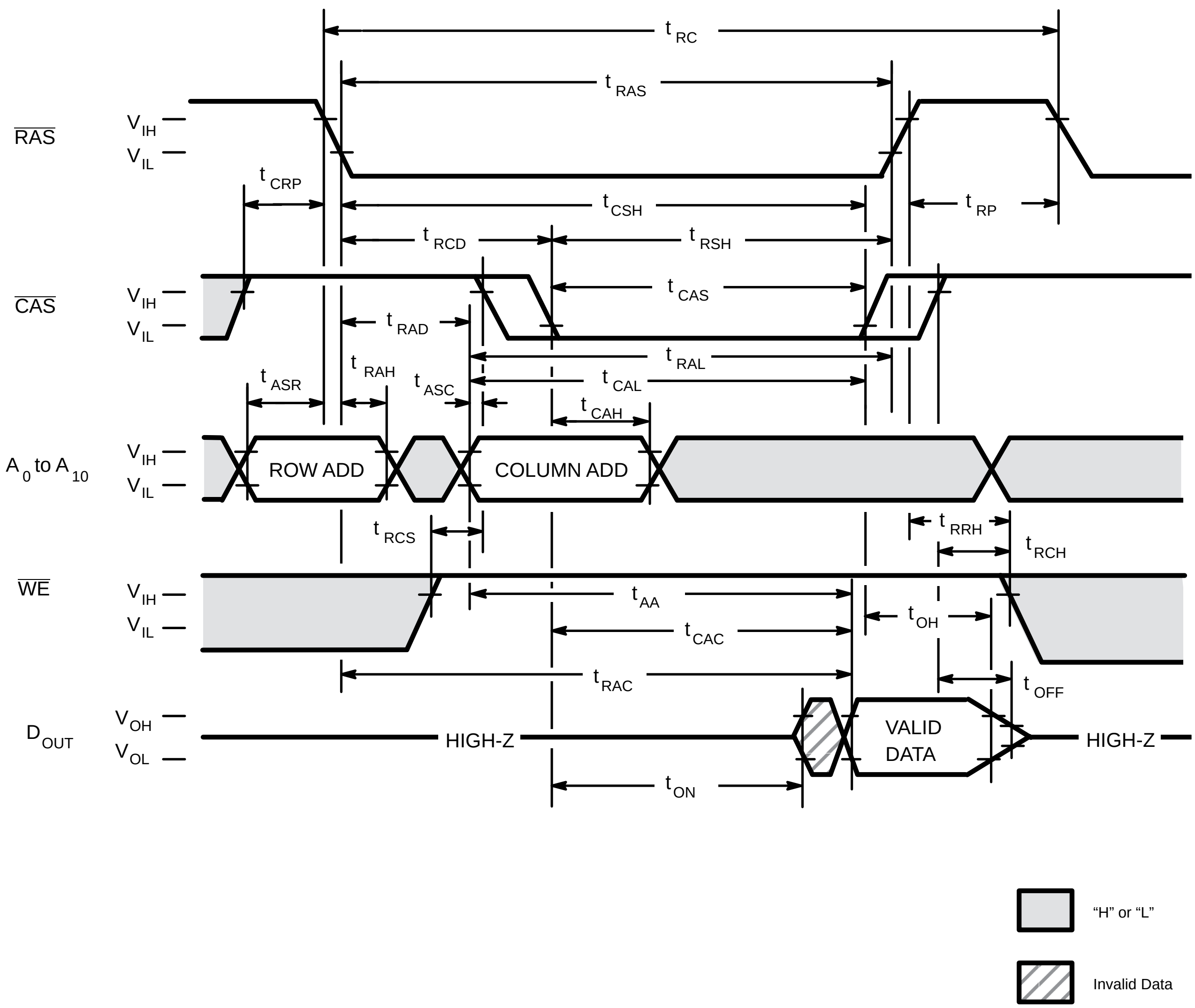
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	H	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	H	—	—	—	Valid	Yes	Previous data is kept
Test mode set cycle (CBR)	L	L	L	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min) $t_{WSR} \geq t_{WSR}$ (min)
Test mode set cycle (Hidden)	H → L	L	L	—	—	—	Valid	Yes	$t_{CSR} \geq t_{CSR}$ (min) $t_{WSR} \geq t_{WSR}$ (min)

Notes:

X : "H" or "L"
*1: It is impossible in Fast Page Mode.

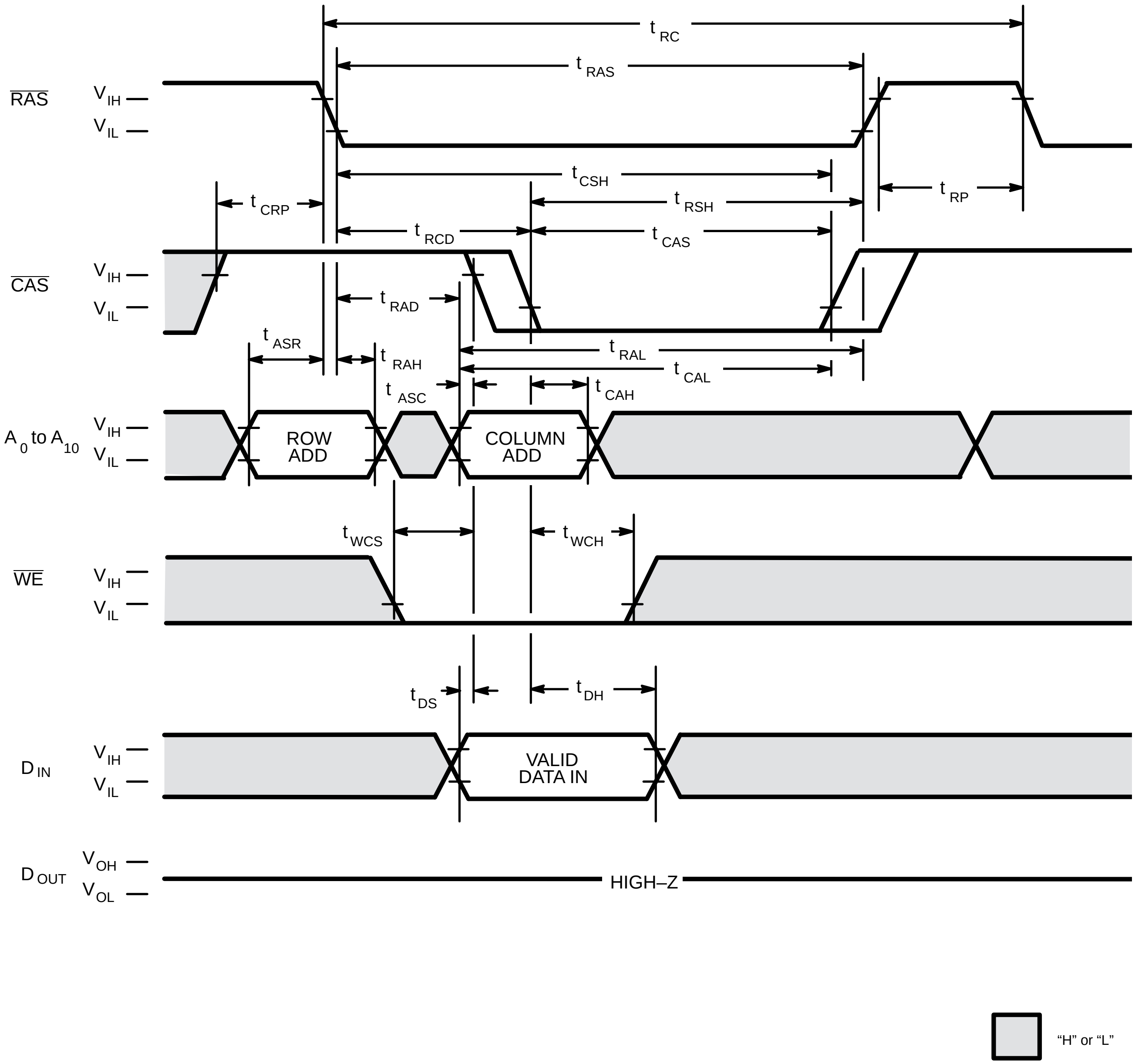
Fig. 5 – READ CYCLE



DESCRIPTION

The read cycle is executed by keeping both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ "L" and keeping $\overline{\text{WE}}$ "H" throughout the cycle. The row and column addresses are latched with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, respectively. The data output remains valid with $\overline{\text{CAS}}$ "L", ie., if $\overline{\text{CAS}}$ goes "H" , the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{\text{RAS}}$ (tRAC), $\overline{\text{CAS}}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time) is greater than the specification, the access time is tAA.

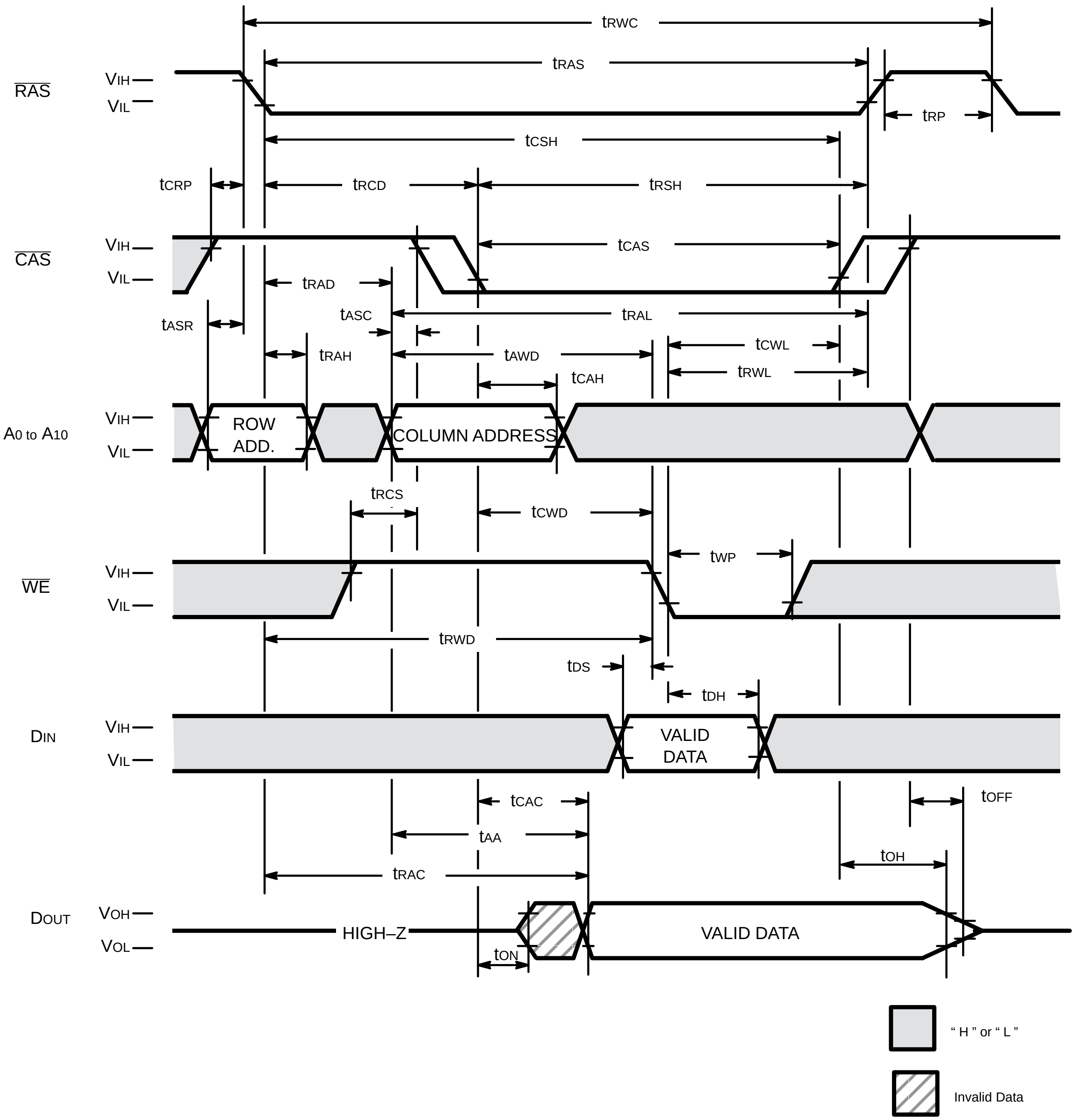
Fig. 6 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

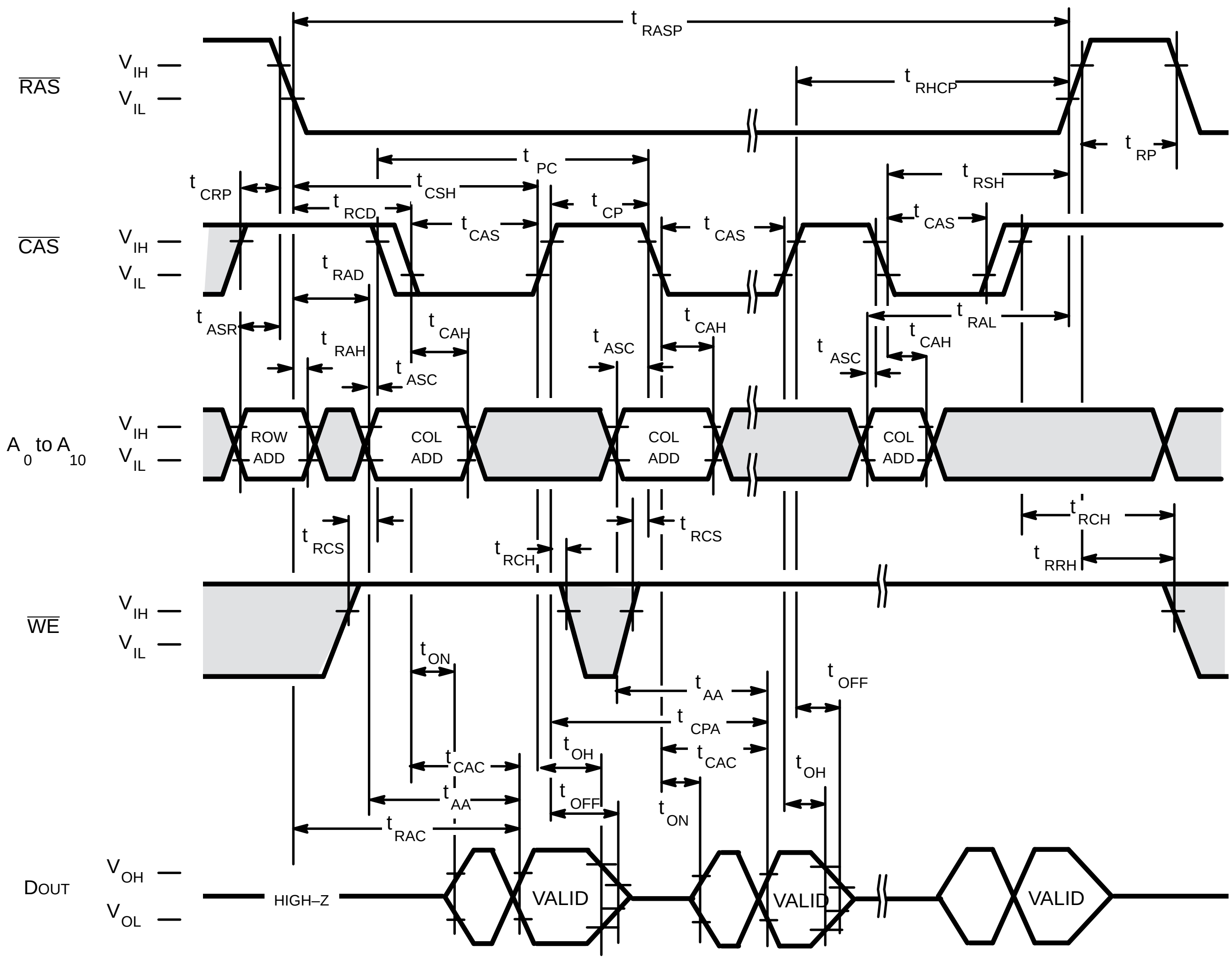
Fig. 7 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin.
After the current data is read out, modified data can be rewritten into the same address quickly.

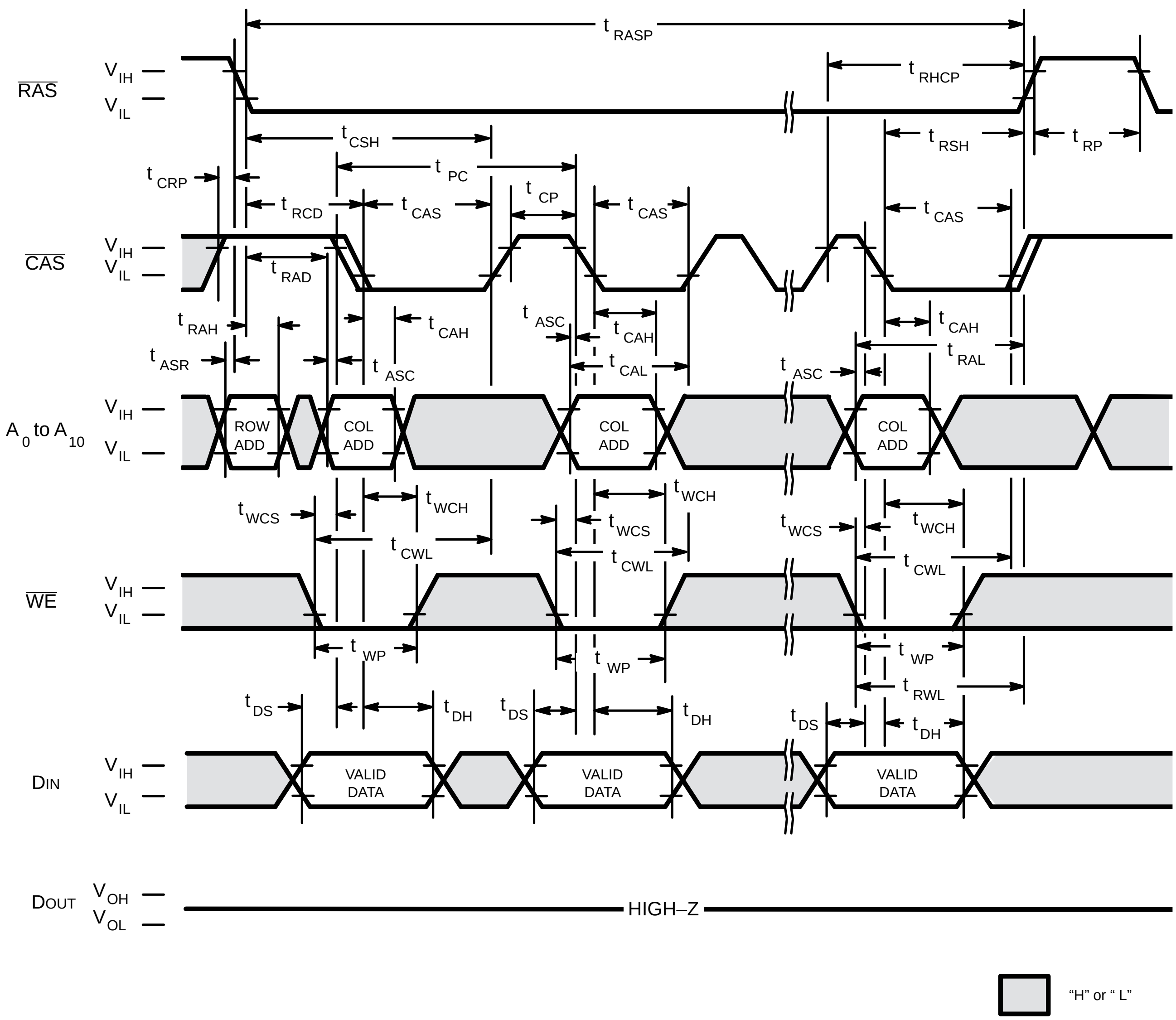
Fig. 8 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H". Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. During fast page mode, the access time is tCAC, tAA, or tCPA, whichever occurs later.
Any of the 2048 bits belonging to each row can be accessed.

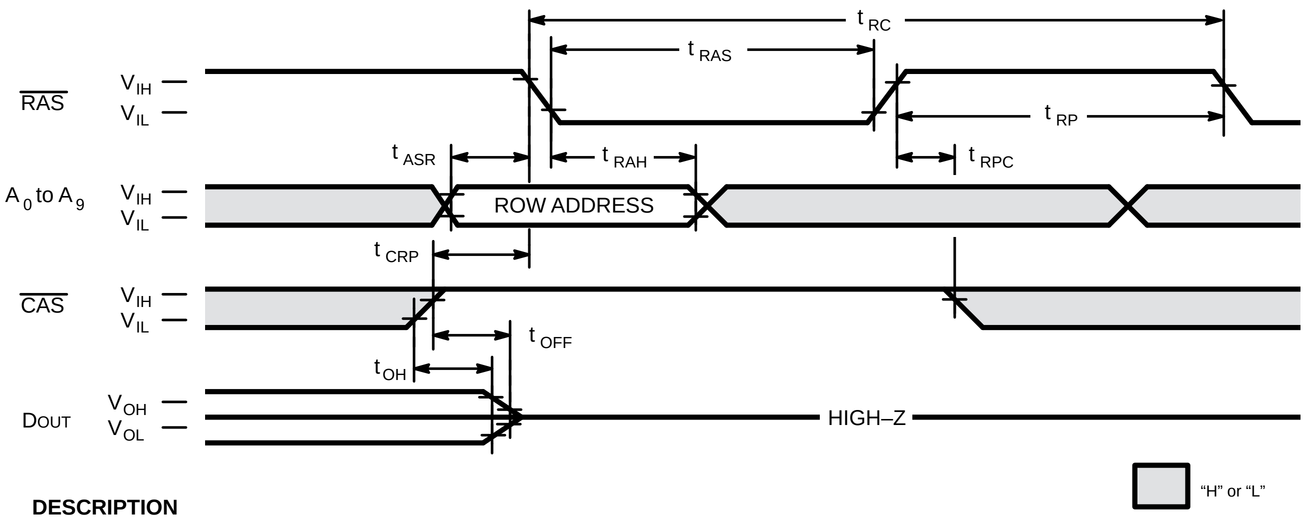
Fig. 9 – FAST PAGE MODE WRITE CYCLE (Early Write)



DESCRIPTION

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$.
The data on DIN pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, tCWL must be satisfied. Any of the 2048 bits belonging to each row can be accessed.

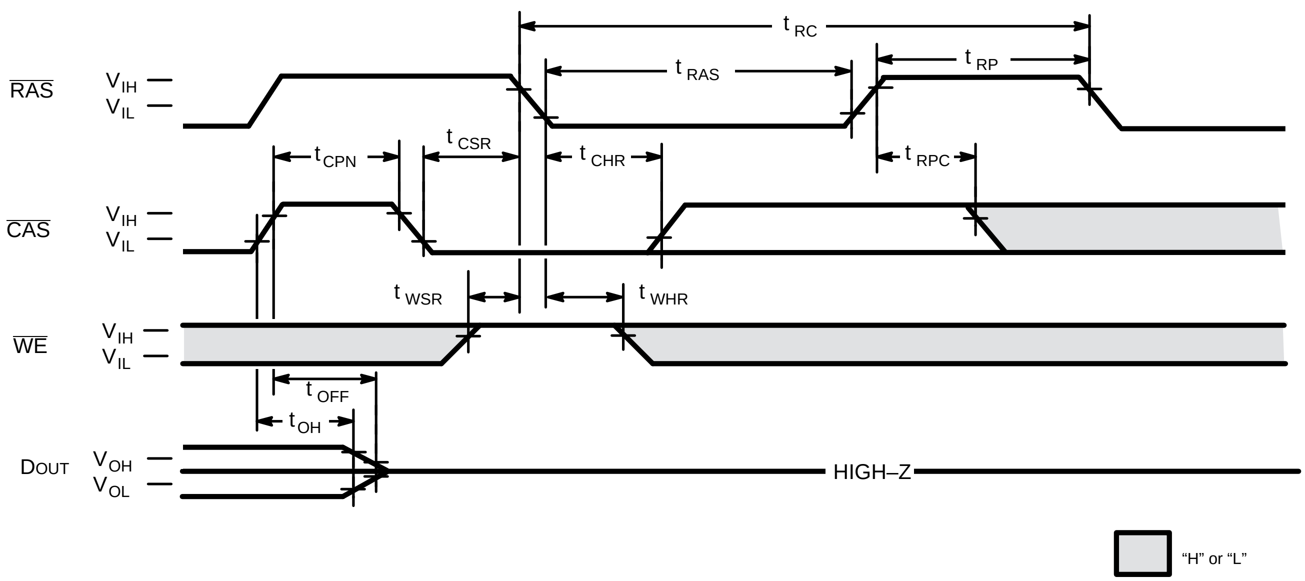
Fig. 11 – $\overline{\text{RAS}}$–ONLY REFRESH ($\overline{\text{WE}}$, DIN, A10 = “H” or “L”)



DESCRIPTION

The refresh of DRAM is executed by normal read, write or read–modify–write cycle, i.e., the cells on the one row line are also refreshed by executing one of three cycles. 1024 row address must be refreshed every 16.4ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re–written to the cell. The MB81V4100C has three types of refresh modes, $\overline{\text{RAS}}$–only refresh, $\overline{\text{CAS}}$–before–$\overline{\text{RAS}}$ refresh, and Hidden refresh.
The $\overline{\text{RAS}}$ only refresh is executed by keeping $\overline{\text{RAS}}$ “L” and $\overline{\text{CAS}}$ “H” throughout the cycle. The row address to be refreshed is latched on the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$–only refresh, the DOUT pin is kept in a high impedance state.

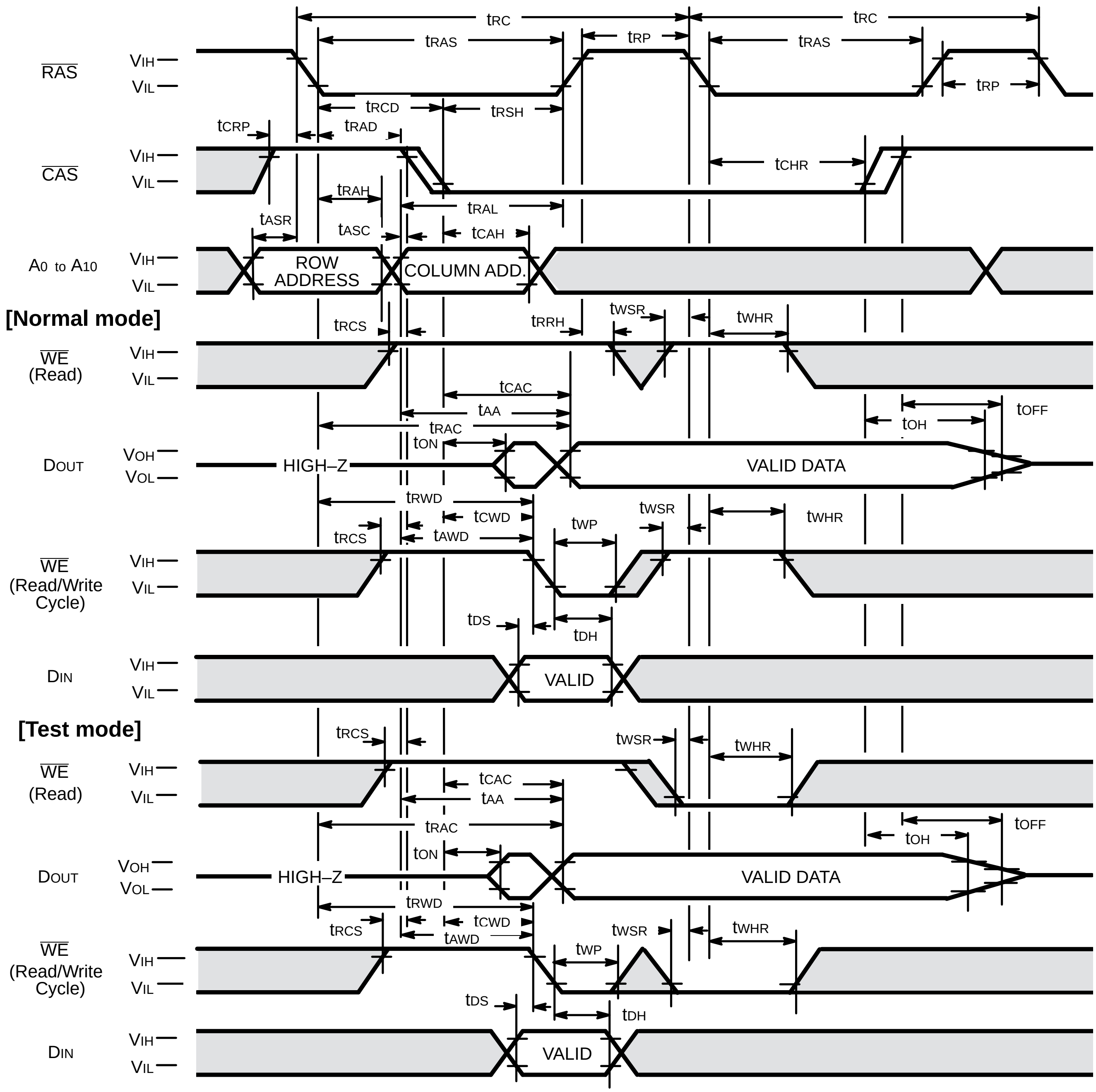
Fig. 12 – $\overline{\text{CAS}}$–BEFORE–$\overline{\text{RAS}}$ REFRESH (A0 to A10, DIN = ”H” or ”L”)



DESCRIPTION

The $\overline{\text{CAS}}$–before–$\overline{\text{RAS}}$ refresh is executed by bringing $\overline{\text{CAS}}$ “L” before $\overline{\text{RAS}}$. By this timing combination, the MB81V4100C executes $\overline{\text{CAS}}$–before–$\overline{\text{RAS}}$ refresh. The row address input is not necessary because it is generated internally.
$\overline{\text{WE}}$ must be held “H” for the specified set up time (tWSR) before $\overline{\text{RAS}}$ goes “L” in order not to enter “test mode”.

Fig. 13 – HIDDEN REFRESH CYCLE

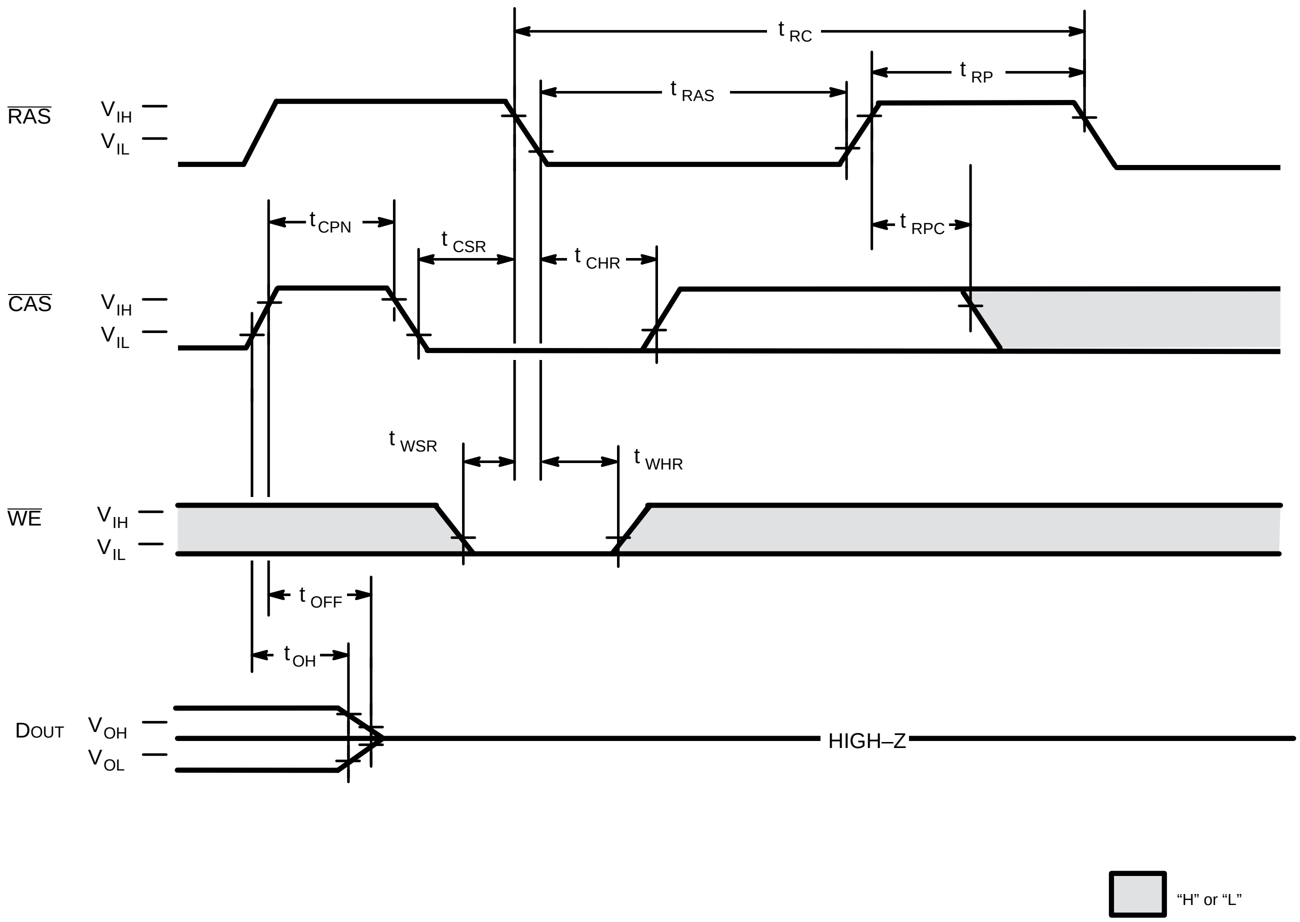


“ H ” or “ L ”

DESCRIPTION

The hidden refresh is executed by keeping $\overline{\text{CAS}}$ “L” to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{\text{CAS}}$ is kept low continuously from previous cycle, followed refresh cycle should be $\overline{\text{CAS}}$–before–$\overline{\text{RAS}}$ refresh.
$\overline{\text{WE}}$ must be held “H” for the specified set up time (tWSR) before $\overline{\text{RAS}}$ goes “L” for the secound time in order not to enter “test mode” to be specified later.

Fig.14 – TEST MODE SET CYCLE (A0 to A10, DIN = ”H” or ”L”)



DESCRIPTION

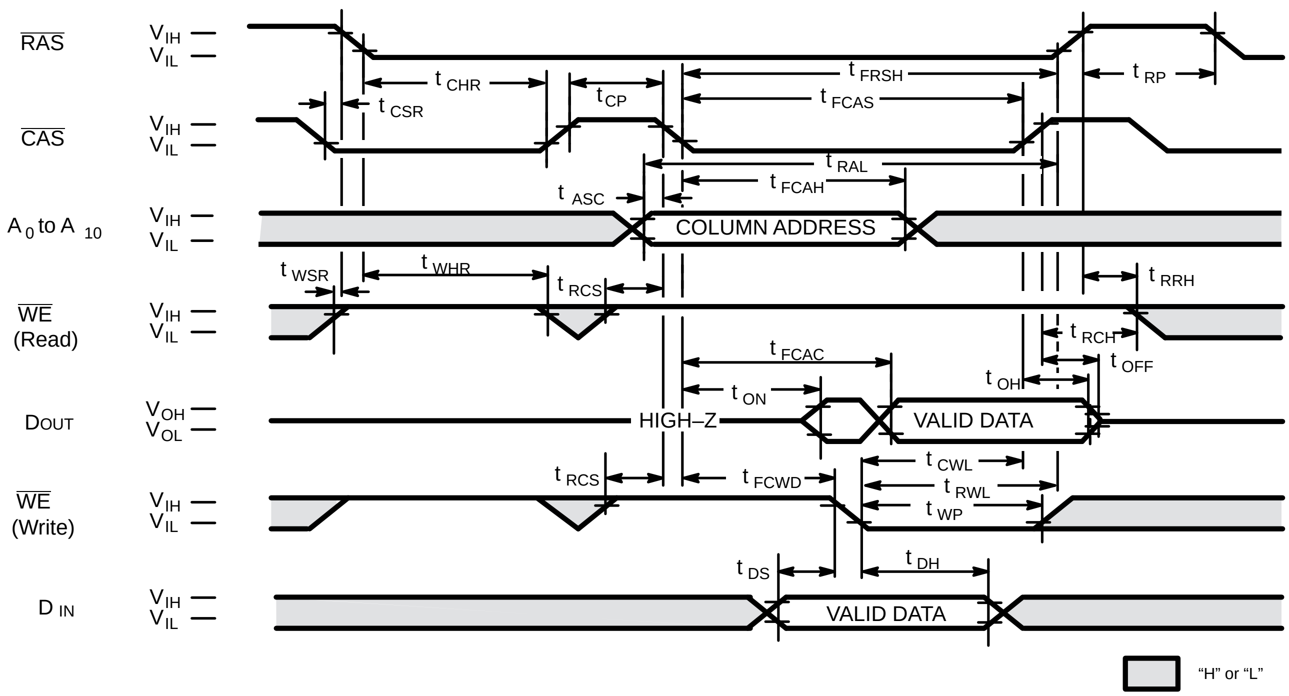
Test Mode ;

The purpose of this test mode is to reduce device test time to one eighth of that required to test the device conventionally.
The test mode function is entered by performing a $\overline{WE}$ and $\overline{CAS}$–before–$\overline{RAS}$ (WCBR) refresh for the entry cycle.
In the test mode, read and write operations are executed in units of eights bits which are selected by the address combination of RA10, CA0 and CA10. In the write mode, data at DIN is written into eight cells simultaneously. In the read mode, eight cells at the selected addresses are read back and checked in the following manner.

When the eight bits are all ”L” or all ”H”, a ”H” level is output..
When the eight bits show a combination of ”L” and ”H”, a ”L” level is output..

The test mode function is exited by performing a $\overline{RAS}$–only refresh or a $\overline{CAS}$–before–$\overline{RAS}$ refresh for the exit cycle.
In test mode operation, the following parameters are delayed approximately 5ns from the specified value in the data sheet..
tRC, tRWC, tRAC, tAA, tRAS, tCSH, tRAL, tRWD, tAWD, tPC, tPRWC, tCPA, tRHCP, tCPWD

Fig. 15 – $\overline{\text{CAS}}$–BEFORE–$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh circuitry. If, after a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle. $\overline{\text{CAS}}$ makes a transition from High to Low while $\overline{\text{RAS}}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A10 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A10 are defined by latching levels on A0–A10 at the second falling edge of $\overline{\text{CAS}}$.

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test procedure is as follows ;

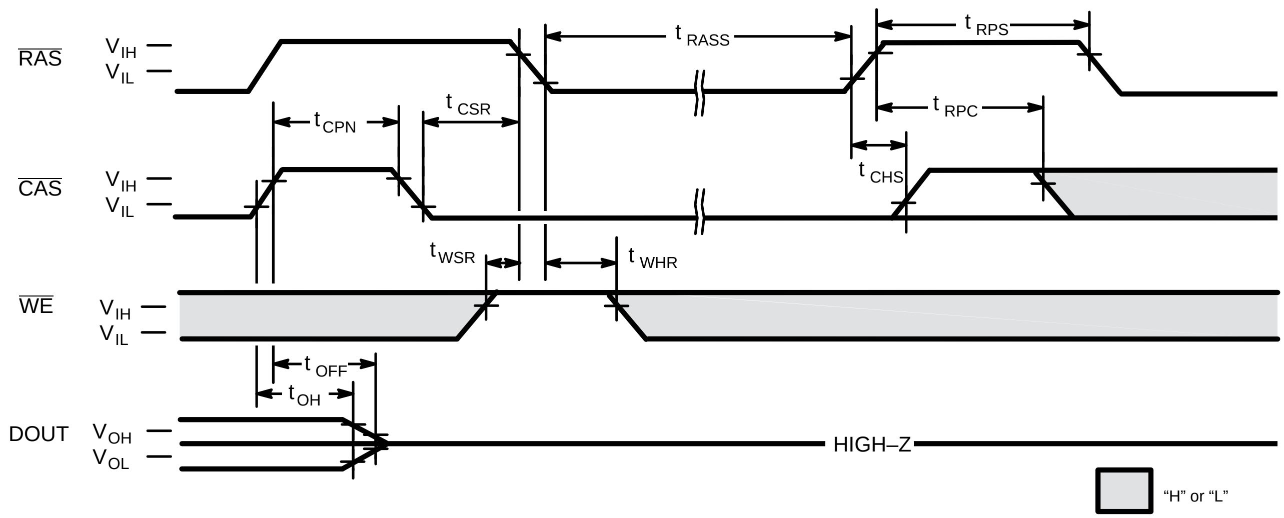
1) Initialize the internal refresh address counter by using 8 $\overline{\text{RAS}}$ only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 1024 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{\text{CAS}}$–before–$\overline{\text{RAS}}$ refresh counter test (read–modify–write cycles). Repeat this procedure 1024 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 1024 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4100C-60		MB81V4100C-70		Unit
			Min	Max	Min	Max	
90	Access Time from $\overline{\text{CAS}}$	t_{FCAC}	—	35	—	40	ns
91	Column Address Hold Time	t_{FCAH}	30	—	30	—	ns
92	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{FCWD}	35	—	40	—	ns
93	$\overline{\text{CAS}}$ Pulse width	t_{FCAS}	35	—	40	—	ns
94	$\overline{\text{RAS}}$ Hold Time	t_{FRSH}	35	—	40	—	ns

Note. Assumes that $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle only.

Fig. 16 – SELF REFRESH CYCLE (A0–A10 = $\overline{\text{OE}}$ = ”H” or ”L”)



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4100C-60		MB81V4100C-70		Unit
			Min	Max	Min	Max	
100	$\overline{\text{RAS}}$ pulse Width	t_{RASS}	100	—	100	—	µs
101	$\overline{\text{RAS}}$ precharge Time	t_{RPS}	110	—	125	—	ns
102	$\overline{\text{CAS}}$ Hold Time	t_{CHS}	–50	—	–50	—	ns

Note . Assumes self refresh cycle only

DESCRIPTION

The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter.

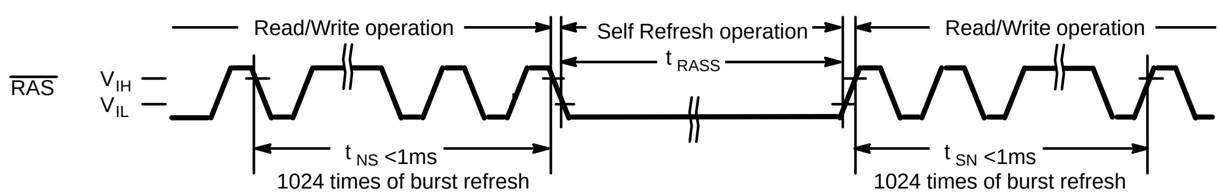
If $\overline{\text{CAS}}$ goes to ”L” before $\overline{\text{RAS}}$ goes to ”L” (CBR) and the condition of $\overline{\text{CAS}}$ ”L” and $\overline{\text{RAS}}$ ”L” is kept for term of tRASS (more than 100µs), the device can be entered the self refresh cycle. And after that, refresh operation is automatically executed per fixed interval using internal refresh address counter during ”$\overline{\text{RAS}}$=L” and ”$\overline{\text{CAS}}$=L”.

And exit from self refresh cycle is performed by toggling of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to ”H” with specifying tCHS min.

Restruction for Self refresh operation ;

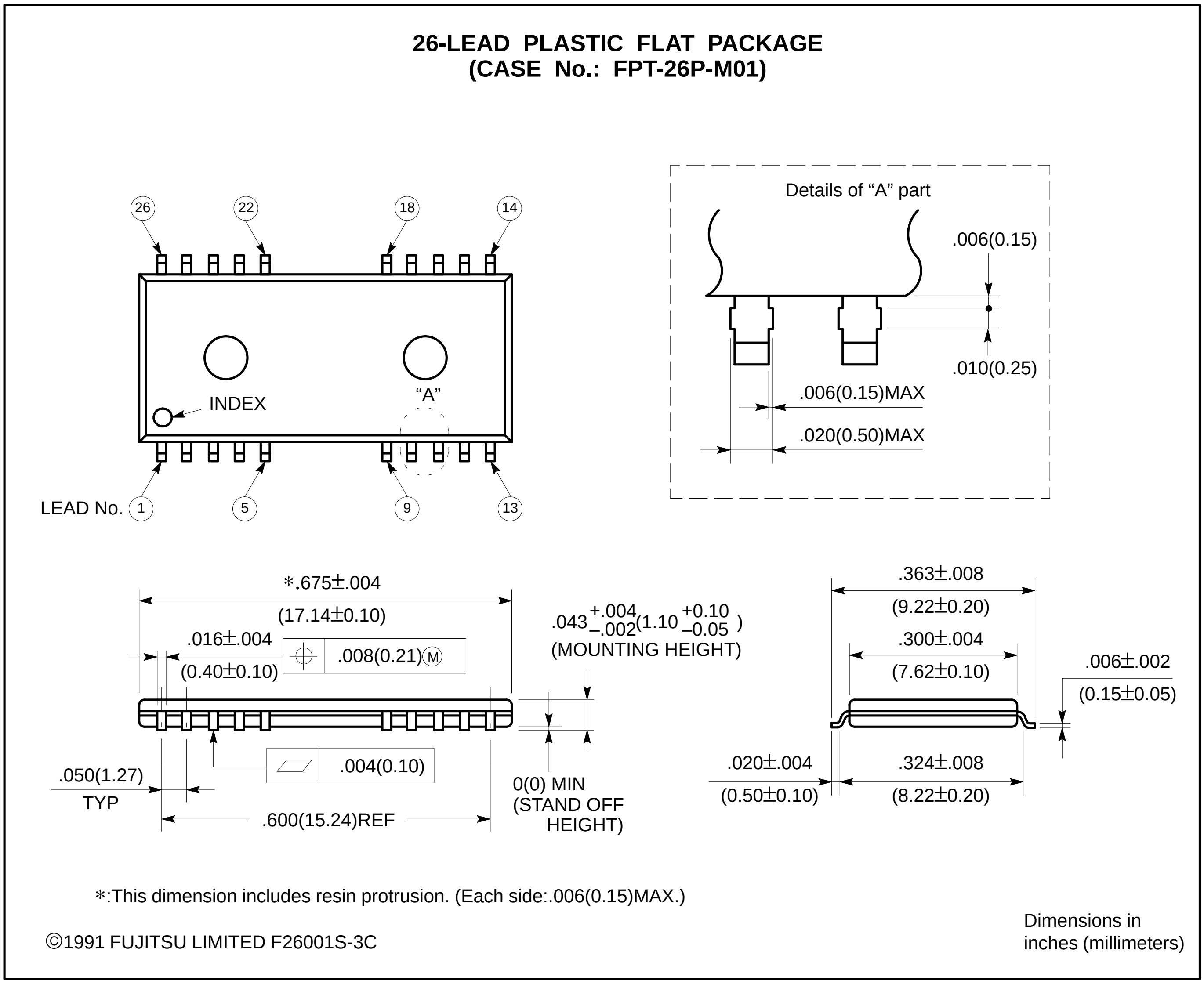
For self refresh operation, the notice below must be considered.

1) In the case that distribut CBR refresh are operated in read/write cycles
   Self refresh cycles can be executed without special rule if 1024 cycles of distribut CBR refresh are executed within tREF max..
2) In the case that burst CBR refresh or $\overline{\text{RAS}}$ only refresh are operated in read/write cycles
   1024 times of burst CBR refresh or 1024 times of burst $\overline{\text{RAS}}$ only refresh must be executed before and after Self refresh cycles.



PACKAGE DIMENSIONS

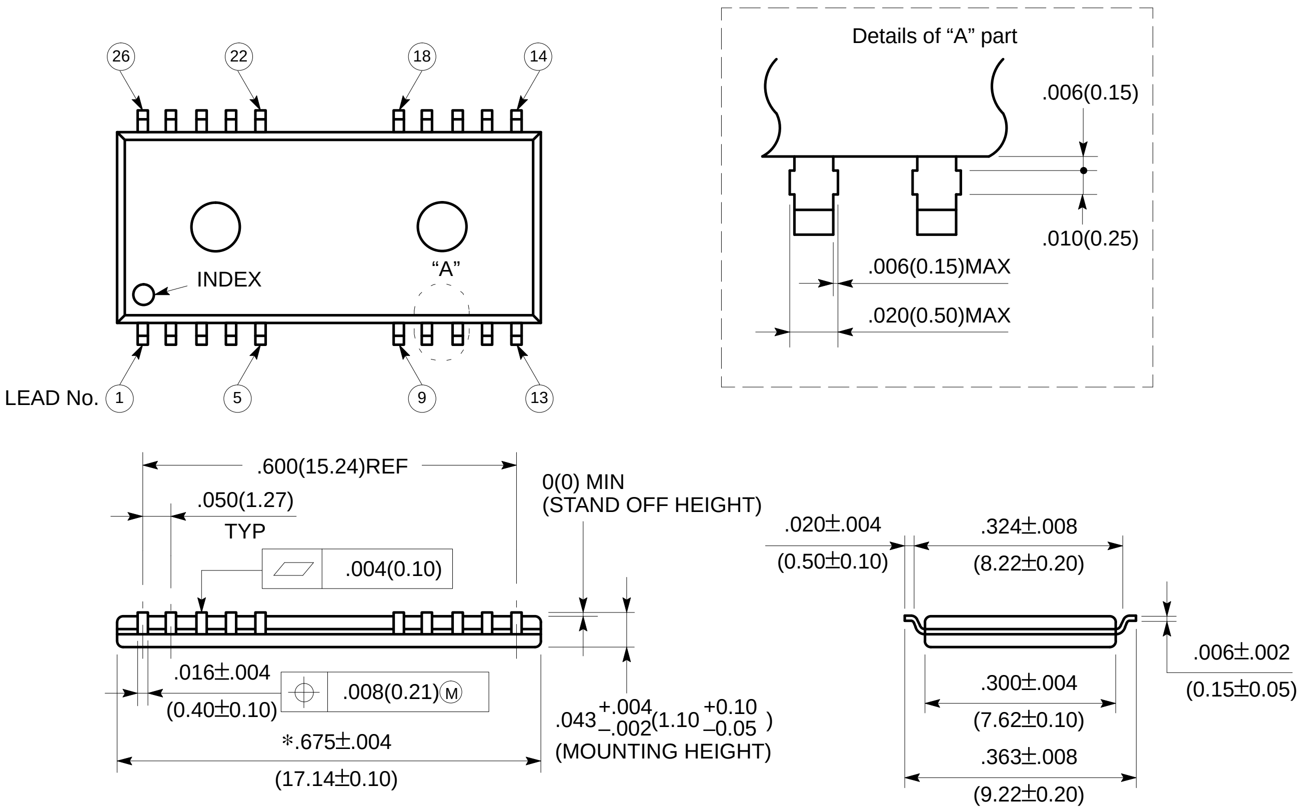
(Suffix : –PFTN)



PACKAGE DIMENSIONS (Continued)

(Suffix : –PFTR)

26-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-26P-M02)



*:This dimension includes resin protrusion. (Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)