DS05–11209–1E

FUJITSU

DATA SHEET

MEMORY

CMOS 4M x 32 FAST PAGE MODE DRAM MODULE MB85391A -60/-70

CMOS 4M x 32 Bit Fast Page Mode DRAM Module

■ DESCRIPTION

The Fujitsu MB85391A is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eight MB8117400A devices. The MB85391A is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85391A are the same as the MB8117400A which features fast page mode operation. For ease of memory expansion, the MB85391A is offered in a 72–pad Single In–line Memory Module package (SIMM).

■ ABSOLUTE MAXIMUM RATINGS (see NOTE.)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	50	mA
Power Dissipation	P_D	8	W
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

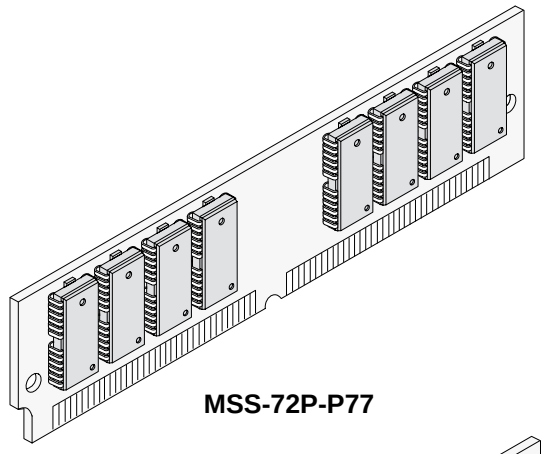
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PRODUCT LINE & FEATURES

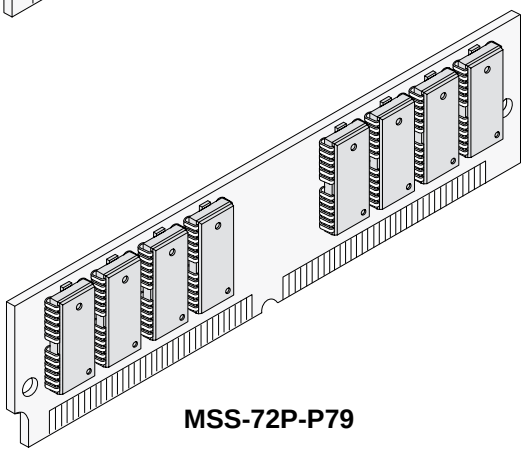
Parameter		MB85391A-60	MB85391A-70
$\overline{RAS}$ Access Time		60ns max.	70ns max.
Random Cycle Time		110ns min.	130ns min.
Address Access Time		30ns max.	35ns max.
$\overline{CAS}$ Access Time		15ns max.	17ns max.
Fast Page Mode Cycle Time		40ns min.	45ns min.
Power Dissipation	Operating Mode	4620mW max.	3960mW max.
	Standby Mode	44mW(CMOS) / 88mW(TTL)	

- Organization :
  4,194,304 words x 32 bits
- Memory : MB8117400A, 8 pcs
- Decoupling Capacitor, 8 pcs
- 5.0V ± 10% Supply Voltage
- Fast Page operation
- 2,048 Refresh Cycles / 32.8ms
- Package and Ordering Information:
  72-pad SIMM, order as
  MB85391A–xxPJPB
  (PJPB = Solder Pad
  MB85391A–xxPJPBK
  (PJPBK = Gold Pad

PACKAGE



MSS-72P-P77



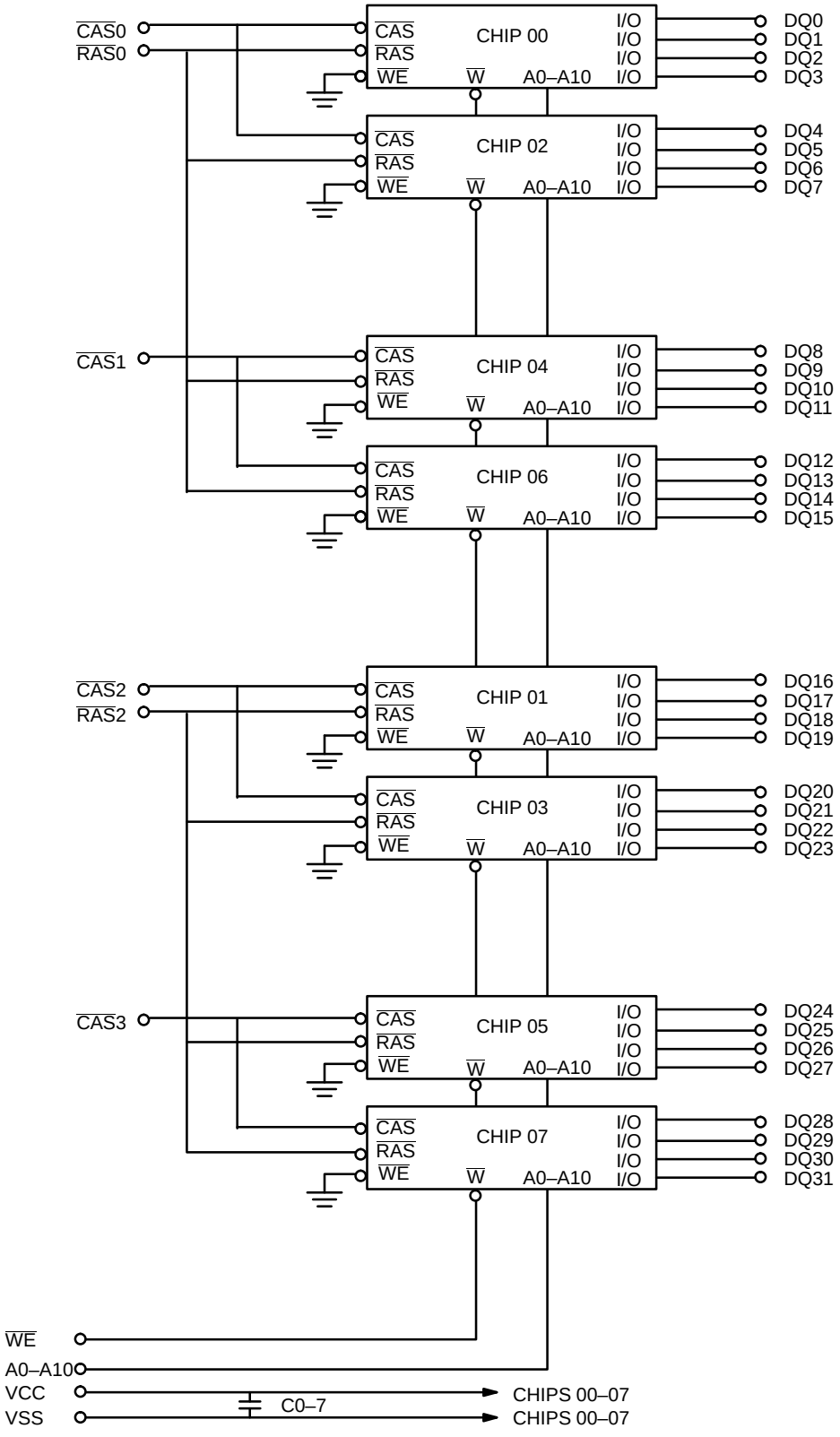
MSS-72P-P79

PIN ASSIGNMENT

DQ0	2	1	VSS
DQ1	4	3	DQ16
DQ2	6	5	DQ17
DQ3	8	7	DQ18
VCC	10	9	DQ19
A0	12	11	NC
A2	14	13	A1
A4	16	15	A3
A6	18	17	A5
DQ4	20	19	A10
DQ5	22	21	DQ20
DQ6	24	23	DQ21
DQ7	26	25	DQ22
A7	28	27	DQ23
VCC	30	29	NC
A9	32	31	A8
$\overline{RAS}$2	34	33	NC
NC	36	35	NC
NC	38	37	NC
$\overline{CAS}$0	40	39	VSS
$\overline{CAS}$3	42	41	$\overline{CAS}$2
$\overline{RAS}$0	44	43	$\overline{CAS}$1
NC	46	45	NC
NC	48	47	$\overline{WE}$
DQ24	50	49	DQ8
DQ25	52	51	DQ9
DQ26	54	53	DQ10
DQ27	56	55	DQ11
DQ28	58	57	DQ12
DQ29	60	59	VCC
DQ30	62	61	DQ13
DQ31	64	63	DQ14
NC	66	65	DQ15
PD2	68	67	PD1
PD4	70	69	PD3
VSS	72	71	NC

Pin #	Symbol	-60	-70
67	PD1	Vss	Vss
68	PD2	NC	NC
69	PD3	NC	Vss
70	PD4	NC	NC

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, all inputs *	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	25	70	°C

Note: * Undershoots of up to –2.0 volts with a pulse width not exceeding 10ns are acceptable.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Test Condition	Min	Max	Unit
Output High Voltage *1		V_{OH}	I_{OH} = –5mA	2.4		V
Output Low Voltage *1		V_{OL}	I_{OL} = 4.2mA		0.4	V
Input Leakage Current	$\overline{RAS}$0, $\overline{RAS}$2	$I_{I(L)}$	0V ≤ V_{IN} ≤ 5.5V, 4.5V ≤ V_{CC} ≤ 5.5V, V_{SS} = 0V, all other pins not under test = 0V	–30	30	µA
	$\overline{CAS}$0 – $\overline{CAS}$3			–20	20	
	Address, $\overline{WE}$			–60	60	
Output Leakage Current		$I_{O(L)}$	0V ≤ V_{OUT} ≤ 5.5V, 4.5V ≤ V_{CC} ≤ 5.5V, Data out disabled	–10	10	µA
Operating Current *2 (Average power supply current)	MB85391A-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling, tRC = min.		840	mA
	MB85391A-70				720	
Standby Current *2 (Power supply current)	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}		16	mA
	CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC}–0.2V		8	
Refresh Current #1 *2 (Average power supply current)	MB85391A-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, tRC = min.		840	mA
	MB85391A-70				720	
Fast Page Mode Current *2	MB85391A-60	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, tPC = min.		560	mA
	MB85391A-70				520	
Refresh Current #2 *2 (Average power supply current)	MB85391A-60	I_{CC5}	$\overline{RAS}$ = cycling, $\overline{CAS}$-before-$\overline{RAS}$, tRC = min.		840	mA
	MB85391A-70				720	

Notes: *1 Referenced to V_{SS}.

*2 I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > –0.3V.
I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC4} is specified at one time of address change during one Page cycle.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85391A-60		MB85391A-70		Unit	Notes
			Min	Max	Min	Max		
1	Time Between Refresh	tREF	—	32.8	—	32.8	ms	
2	Random Read/Write Cycle Time	tRC	110	—	130	—	ns	
3	Access Time from $\overline{RAS}$	tRAC	—	60	—	70	ns	**4, 7**
4	Access Time from $\overline{CAS}$	tCAC	—	15	—	17	ns	**5, 7**
5	Column Address Access Time	tAA	—	30	—	35	ns	**6, 7**
6	Output Hold Time	tOH	3	—	3	—	ns	
7	Output Buffer Turn On Delay Time	tON	0	—	0	—	ns	
8	Output Buffer Turn Off Delay Time	tOFF	—	15	—	17	ns	**8**
9	Transition Time	tT	3	50	3	50	ns	
10	$\overline{RAS}$ Precharge Time	tRP	40	—	50	—	ns	
11	$\overline{RAS}$ Pulse Width	tRAS	60	100000	70	100000	ns	
12	$\overline{RAS}$ Hold Time	tRSH	15	—	17	—	ns	
13	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	0	—	0	—	ns	
14	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	20	45	20	53	ns	**9, 10**
15	$\overline{CAS}$ Pulse Width	tCAS	15	10000	17	10000	ns	
16	$\overline{CAS}$ Hold Time	tCSH	60	—	70	—	ns	
17	$\overline{CAS}$ Precharge Time (C–B–R Refresh)	tCPN	10	—	10	—	ns	**17**
18	Row Address Setup Time	tASR	0	—	0	—	ns	
19	Row Address Hold Time	tRAH	10	—	10	—	ns	
20	Column Address Setup Time	tASC	0	—	0	—	ns	
21	Column Address Hold Time	tCAH	15	—	15	—	ns	
22	Column Address Hold Time from $\overline{RAS}$	tAR	35	—	35	—	ns	
23	$\overline{RAS}$ to Column Address Delay Time	tRAD	15	30	15	35	ns	**11**
24	Column Address to $\overline{RAS}$ Lead Time	tRAL	30	—	35	—	ns	
25	Column Address to $\overline{CAS}$ Lead Time	tCAL	30	—	35	—	ns	
26	Read Command Setup Time	tRCS	0	—	0	—	ns	
27	Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	—	0	—	ns	**12**
28	Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	—	0	—	ns	**12**
29	Write Command Setup Time	tWCS	0	—	0	—	ns	**13**
30	Write Command Hold Time	tWCH	15	—	15	—	ns	
31	Write Command Hold Time from $\overline{RAS}$	tWCR	35	—	35	—	ns	
32	$\overline{WE}$ Pulse Width	tWP	15	—	15	—	ns	
33	Write Command to $\overline{RAS}$ Lead Time	tRWL	15	—	17	—	ns	
34	Write Command to $\overline{CAS}$ Lead Time	tCWL	15	—	17	—	ns	
35	DIN Setup Time	tDS	0	—	0	—	ns	
36	DIN Hold Time	tDH	15	—	15	—	ns	

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless othewise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85391A-60		MB85391A-70		Unit	Notes
			Min	Max	Min	Max		
37	Data Hold Time from $\overline{RAS}$	tDHR	35	—	35	—	ns	
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	tRPC	5	—	5	—	ns	
39	$\overline{CAS}$ Setup Time (C–B–R Refresh)	tCSR	0	—	0	—	ns	
40	$\overline{CAS}$ Hold Time (C–B–R Refresh)	tCHR	10	—	12	—	ns	
41	$\overline{WE}$ Setup Time from $\overline{RAS}$	tWSR	0	—	0	—	ns	**18**
42	$\overline{WE}$ Hold Time from $\overline{RAS}$	tWHR	10	—	10	—	ns	**18**
43	DIN to $\overline{CAS}$ Delay Time	tDZC	0	—	0	—	ns	**15**
44	Fast Page Mode $\overline{CAS}$ Pulth Width	tRASP	—	100000	—	100000	ns	
45	Fast Page Mode Read/Write Cycle Time	tPC	40	—	45	—	ns	
46	Access Time from $\overline{CAS}$ Precharge	tCPA	—	35	—	40	ns	**7, 16**
47	Fast Page Mode $\overline{CAS}$ Precharge Time	tCP	10	—	10	—	ns	
48	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	35	—	40	—	ns	

Notes:

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200µs is required after power–up followed by any eight $\overline{RAS}$–only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$–before–$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.
2. AC characteristics assume tT = 5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measureing the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that tRCD ≤ tRCD (max), tRAD≤ tRAD (max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will be increased by the amount that tRCD exceeds the value shown.
5. If tRCD≥ tRCD (max), tRAD≥ tRAD (max), and tASC≥ tAA– tCAC – tT, access time is tCAC.
6. If tRAD≥ tRAD (max) and tASC≤ tAA– tCAC – tT, access time is tAA.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. tOFF is specified that output buffer change to high impedance state.
9. Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, access time is controlled exclusively by tCAC or tAA.
10. tRCD (min) = tRAH (min)+ 2tT + tASC (min).
11. Operation within the tRAD (max) limit ensures that tRAC (max) can be met. tRAD (max) is specified as a reference point only; if tRAD is greater than the specified tRAD (max) limit, access time is controlled exclusively by tCAC or tAA.
12. Either tRRH or tRCH must be satisfied for a read cycle.
13. tWCS is specified as a reference point only. If tWCS ≥ tWCS (min) the data output pin will remain High-Z state through entire cycle.
14. Assumes that tWCS < tWCS (min).
15. Either tDZC or tDZO must be satisfied.
16. tCPA is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if tCP become long, tCPA also become longer than tCPA (max).
17. Assumes that $\overline{CAS}$-before- $\overline{RAS}$ refresh.
18. Assumes that test mode function.

*Source: See MB8117400A Data Sheet for details on the electricals.

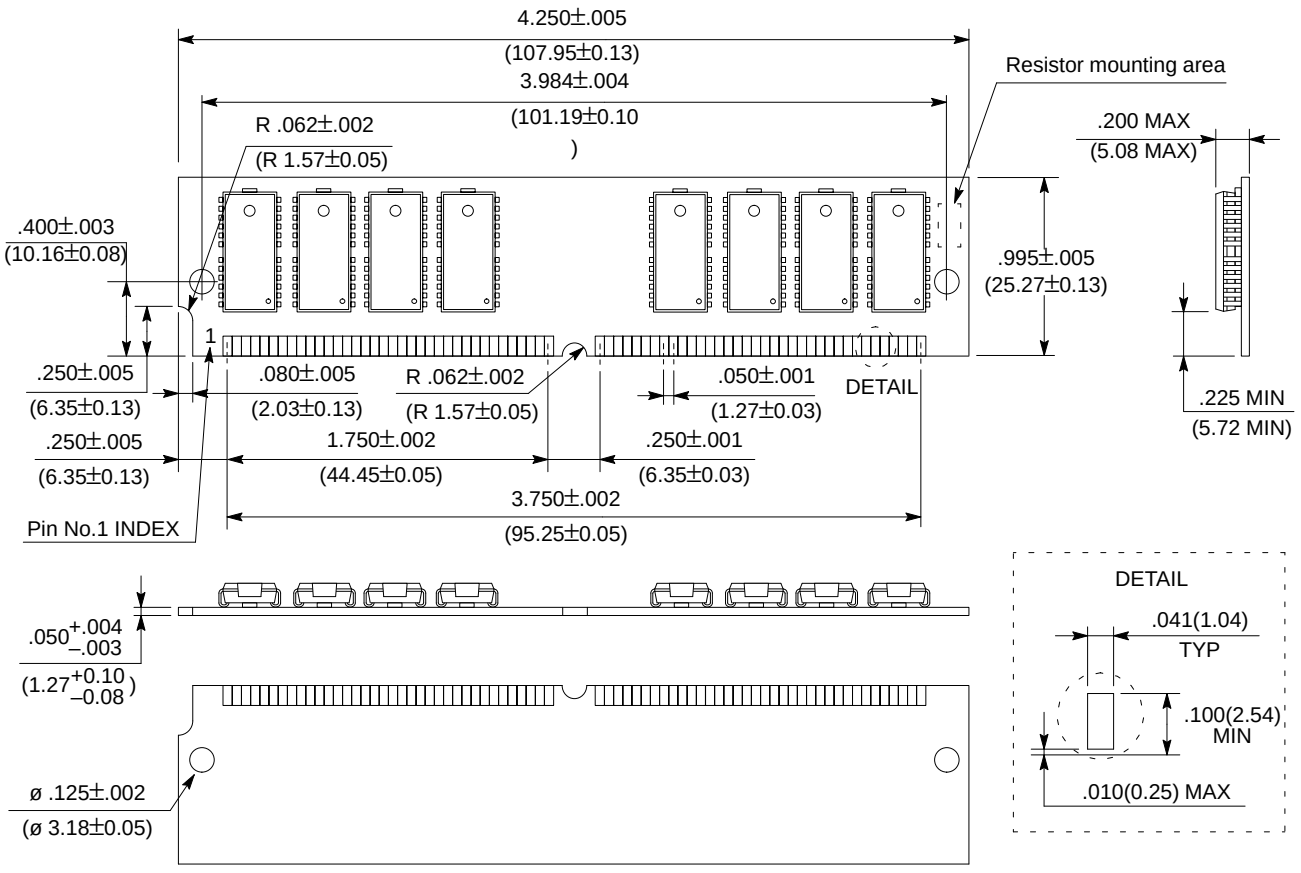
CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance, A0 to A10	C_{IN1}		71	pF
Input Capacitance, $\overline{RAS}$0 and $\overline{RAS}$2	C_{IN2}		39	pF
Input Capacitance, $\overline{CAS}$0 to $\overline{CAS}$3	C_{IN3}		23	pF
Input Capacitance, $\overline{WE}$	C_{IN4}		66	pF
I/O Capacitance, (DQ0-31)	C_{DQ}		12	pF

PACKAGE DIMENSIONS

(Suffix: PJPBK)

72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P77)

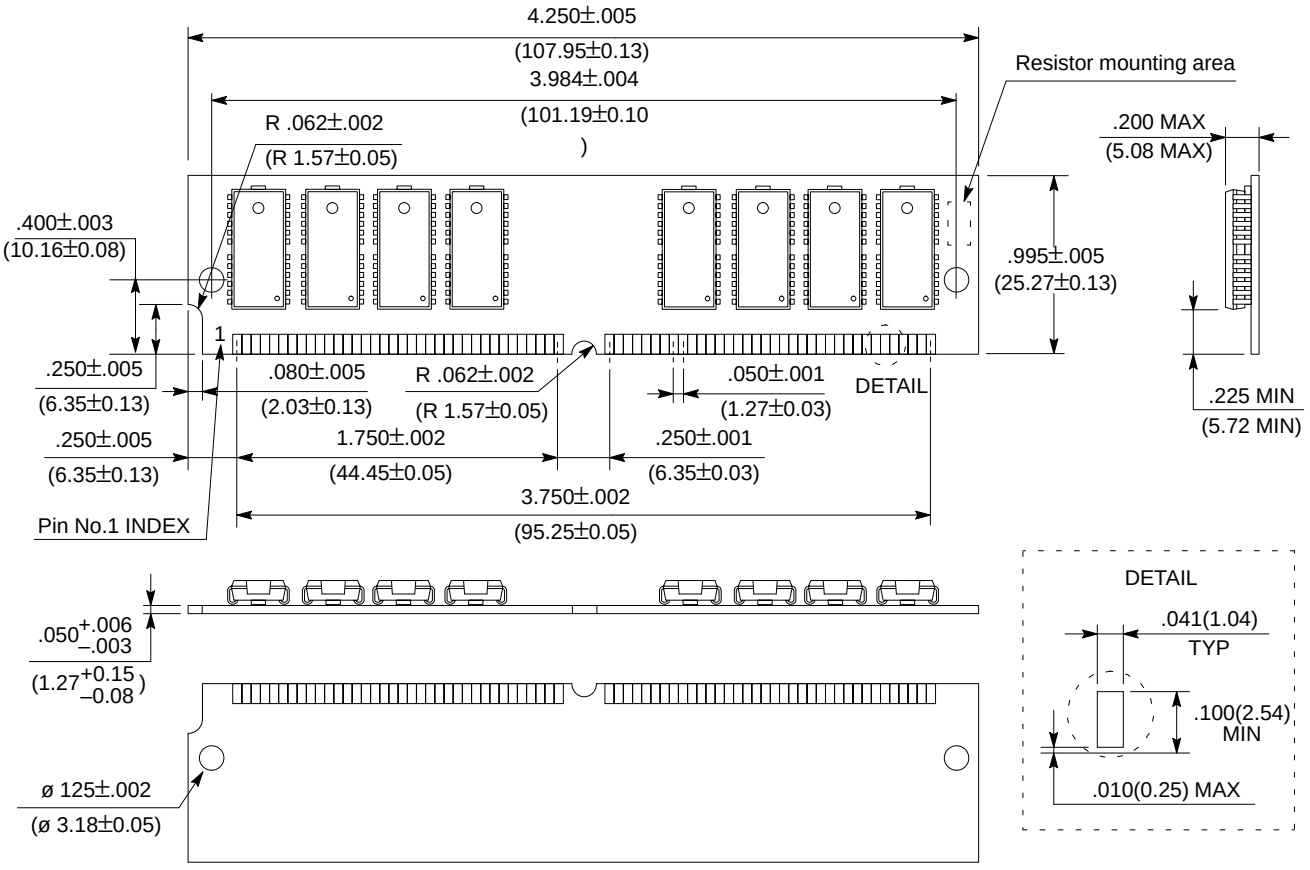


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PJPB)

72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P79)



Dimensions in
inches (millimeters)