August 1990
Edition 1.0

FUJITSU

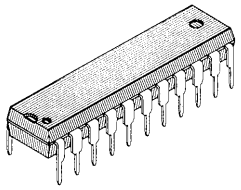
DATA SHEET

MB40568
1-CHANNEL 8-BIT A/D CONVERTER

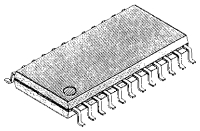
1-CHANNEL 8-BIT LOW POWER VIDEO A/D CONVERTER ON-CHIP CLAMP CIRCUIT

The Fujitsu MB40568 is a low power ultra-high speed video A/D converter fabricated with Fujitsu Advanced Bipolar Technology. The MB40568 also adopts the fully parallel comparison technique (flash method) for high speed conversion and can convert wide-band analog signals, such as a video signal, to digital at a sampling rate of DC through 20 mega-samples/sec. Because of such high-speed operation and on-chip clamp/reference voltage generator circuitry, the MB40568 is suitable for digital video applications such as digital TV, video processing with a computer, or radar signal processing.

- Resolution: 8 bits
- Linearity error: ±0.15 (typical)
- Maximum conversion rate: 20 MSPS minimum
- Analog input voltage: 0V to 3.0V, $2V_{P-P}$ (with clamp circuit)
  3.0V to 5.0V (without clamp circuit)
- Digital I/O level: TTL compatible
- Single power supply: +5V
- Power dissipation: 200 mW typical
- Package: Standard 22–pin DIP package: Suffix: —P
  Standard 24–pin SOP package: Suffix: —PF



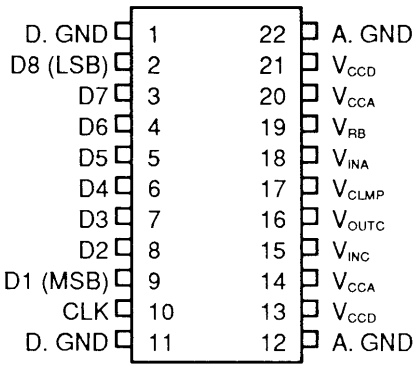
PLASTIC PACKAGE
DIP-22P-M04



PLASTIC PACKAGE
FPT-24P-M02

PIN ASSIGNMENT

(TOP-VIEW)



SOP: Please refer to page 16.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	–0.5 to +7.0	V
Digital Input Voltage	V_{IND}	_0.5 to +7.0	V
Analog Input Voltage	V_{INA}	–0.5 to V_{CC} +0.5	V
Analog Reference Voltage	V_{RB}	–0.5 to V_{CC} +0.5	V
Clamp Circuit Input Voltage	V_{INC}	–0.5 to V_{CC} +0.5	V
Storage Temperature	T_{STG}	–55 to +125	°C

Note : Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

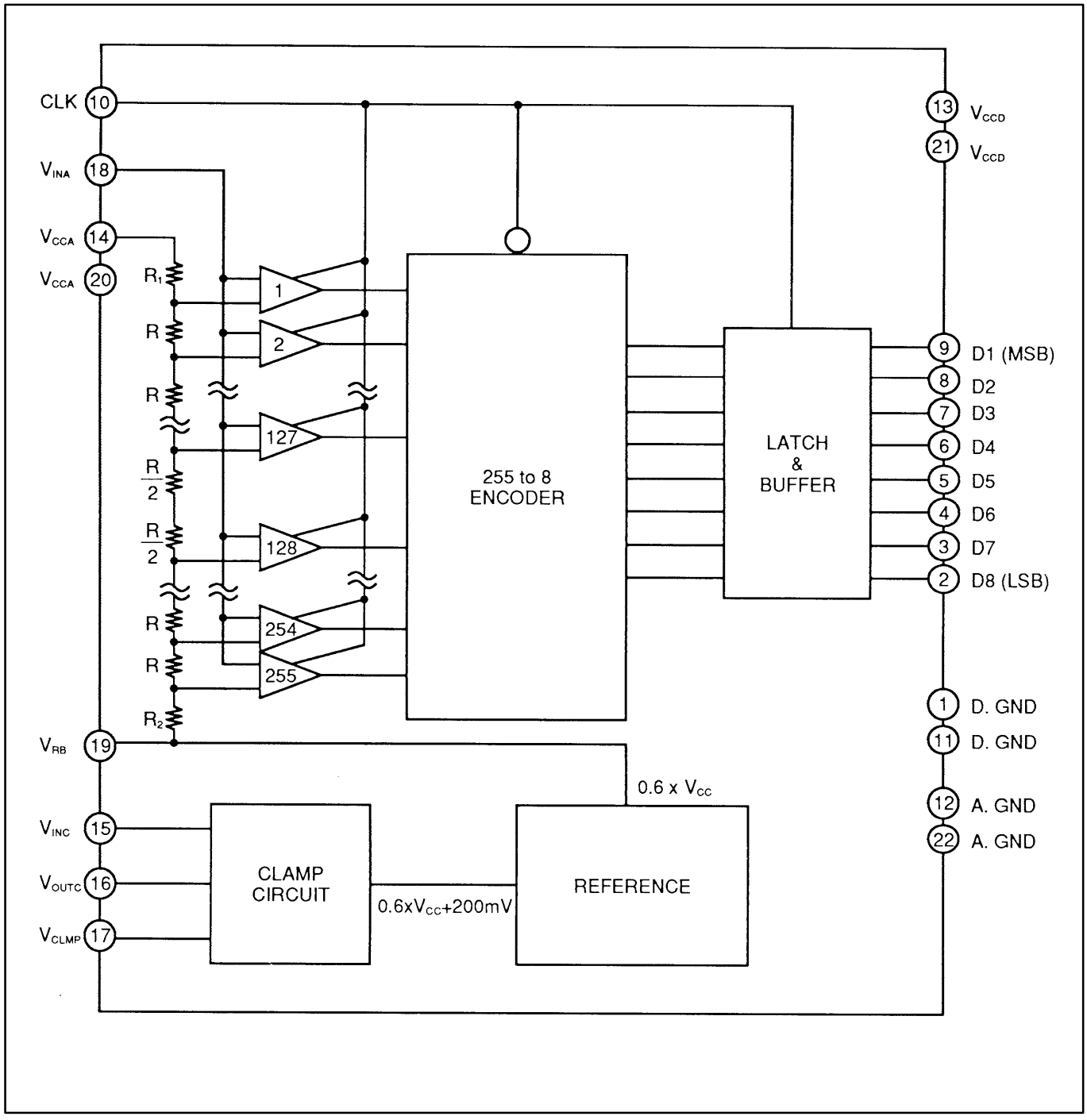


Figure 1a. MB40568 Block Diagram – DIP

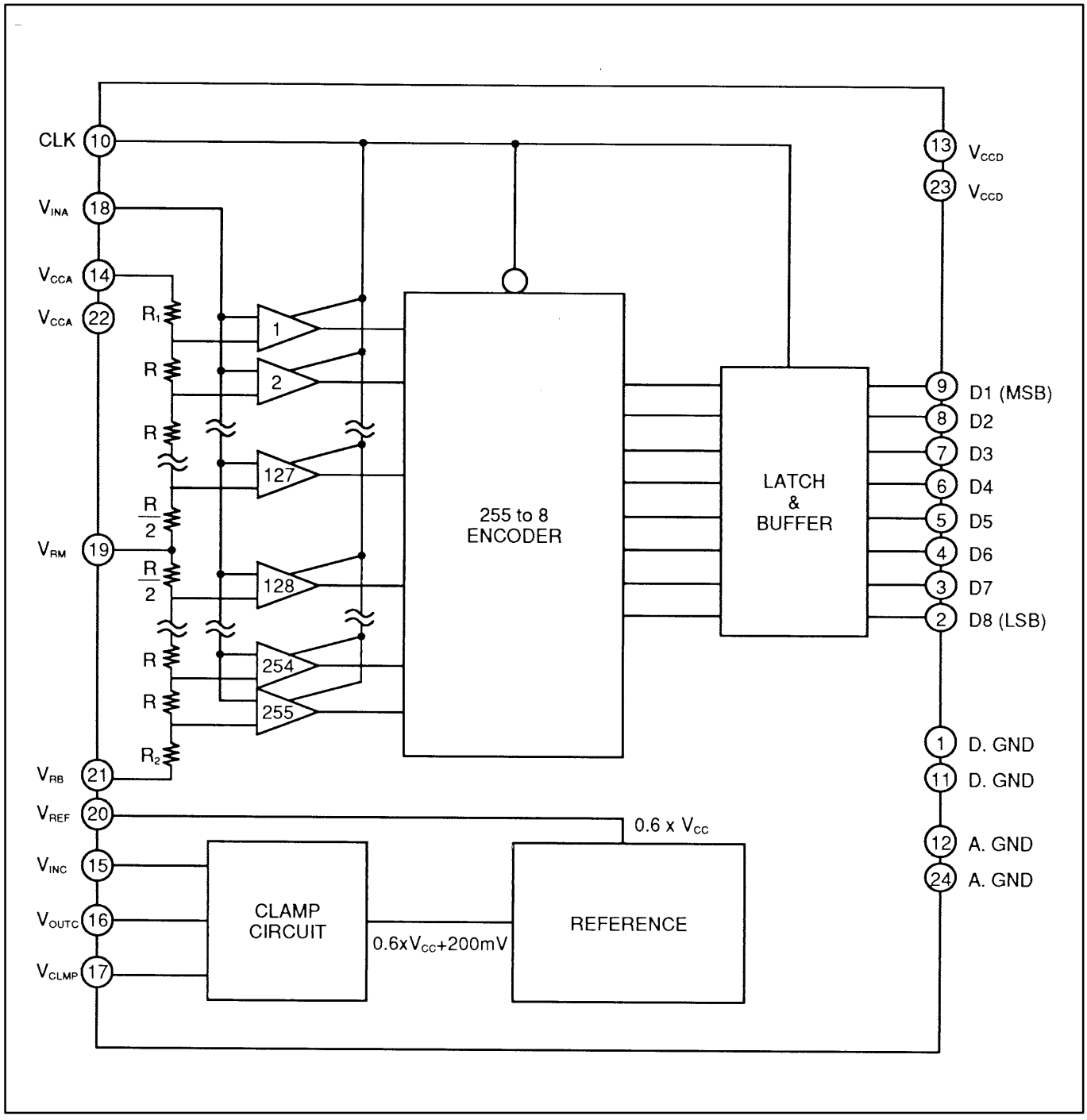


Figure 1b. MB40568 Block Diagram – SOP

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage[1]	V_{CC} V_{CCD}	4.75	5.00	5.25	V
Analog input voltage	V_{INA}	V_{RB}		V_{CCA}	V
Analog reference voltage[2]	V_{RB}	2.75	3	3.25	V
Clamp circuit input voltage	V_{INC}	0		3	V
Clamp capacitance	C_{CLMP}	1			MF
Digital high–level output current[3]	I_{OH}	–400			μA
Digital low–level output current	I_{OL}			1.6	mA
Clock pulse width at high level	t_{W+}	22.5			ns
Clock pulse width at low level	t_{W-}	22.5			ns
Operating temperature	T_A	0		70	°C

Notes: [1] Keep V_{CCA} and V_{CCD} at the same potential.
[2] For SOP, set V_{CCA} and V_{RB} at 2.0V ±0.1V.
[3] Clamp circuit input voltage is set at (V_{CCA}-V_{CLMP}).

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CCA}=V_{CCD}=4.75 to 5.25V, T_A=0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					8	Bit
Linearity Error*	LE	DC		±0.15	±0.3	%
Equivalent Analog Input Resistance	R_{INA}	$R_{INA} = \frac{V_{CCA} - V_{RB}}{I_{IHA} - I_{ILA}}$	300			kΩ
Analog Input Capacitance	C_{INA}	f_{INA}=1 MHz		40	50	pF
Analog High–Level Input Current	I_{IHA}	V_{INA}=V_{CCA}			45	μA
Analog Low–Level Input Current	I_{ILA}	V_{INA}=V_{RB}			40	μA
Clamp Circuit Input Current	I_{INC}	V_{INC}=0V	–600	–200		μA
Clamp Voltage	V_{CLMP}			V_{RB}+0.2		V
Reference Current	I_{RB}	SOP	8.5	–5.5	–3.0	mA
Reference Voltage	V_{RB}	DIP	0.6xV_{CC} –0.1	0.6 x V_{CC}	0.6 x V_{CC} +0.1	V
	V_{REF}	SOP V_{REF}–V_{RB} short circuit				

*V_{CCA}=V_{CCD}=5.00V, T_A=25♂°C

DIGITAL DC CHARACTERISTICS

(V_{CCA}=V_{CCD}=4.75 to 5.25V, T_A=0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-Level Output Voltage	V_{OH}	I_{OH} = –400 μA	2.7			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1 .6 mA			0.4	V
High-Level Input Voltage	V_{IHD}		2.0			V
Low-Level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{ID}= 7V			100	μA
High-Level Input Current	I_{IHD}	V_{IHD}= 2.7V		0	20	μA
Low-Level Input Current	I_{ILD}	V_{ILD}= 0.4V	–100	–10		μA
Power Supply Current	I_{CC}			40*	85	mA

*V_{CCA}=V_{CCD}=5.00V, T_A=25°C

SWITCHING CHARACTERISTICS

(V_{CCA}=V_{CCD}=4.75 to 5.25V, T_A=0 to 70°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Maximum Conversion Rate	FS	20			MSPS
Digital Output Delay Time	t_{pd}	8	15	30	ns

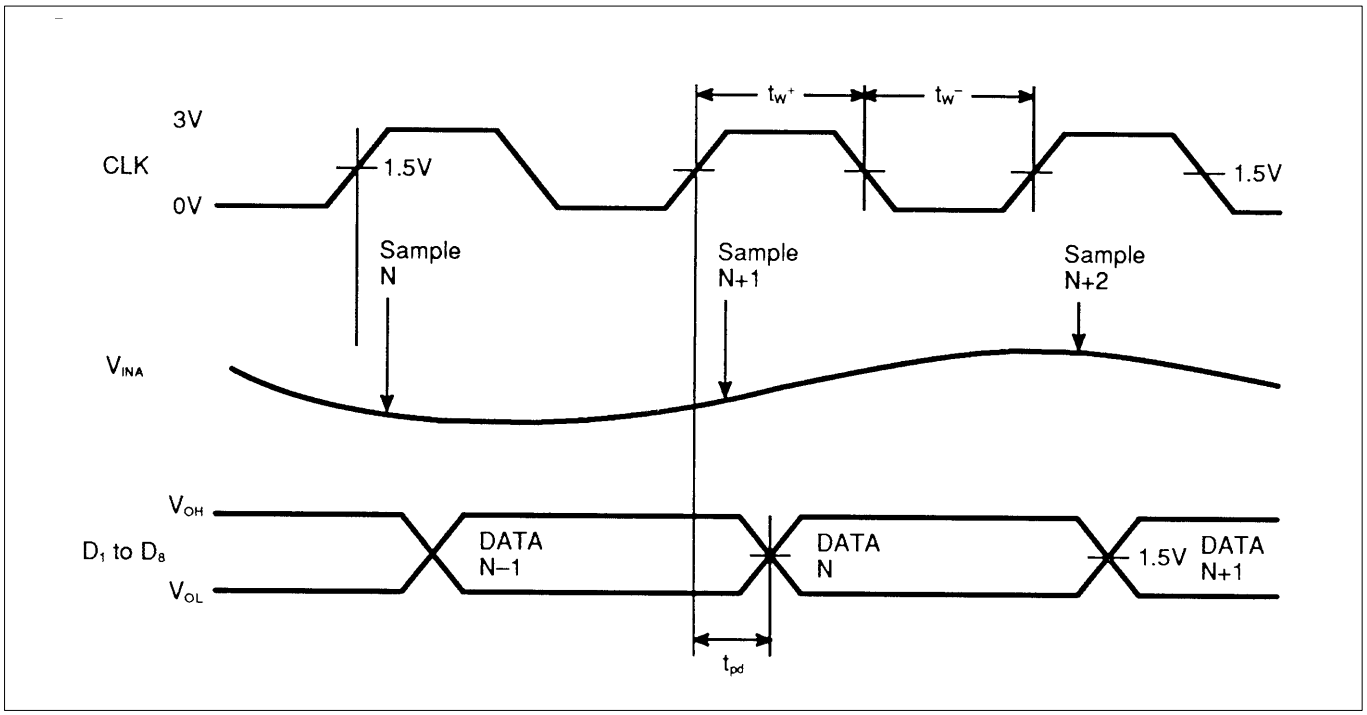


Figure 2. Timing Diagram

TYPICAL ELECTRICAL CURVES

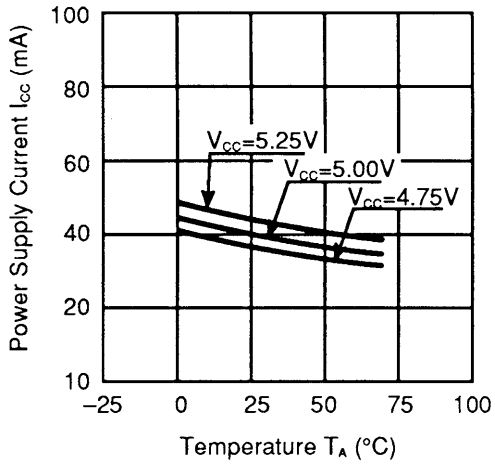


Figure 3. Power Supply Current vs. Temperature

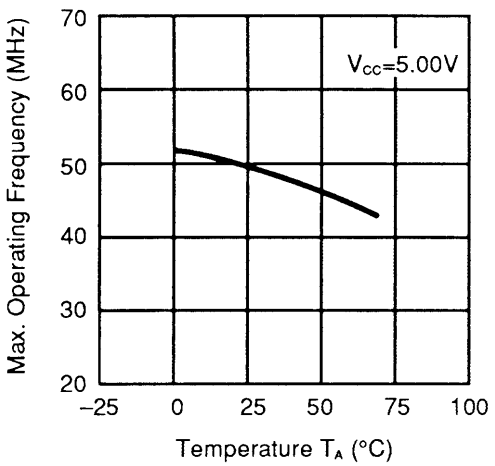


Figure 4. Maximum Operating Frequency vs. Temperature

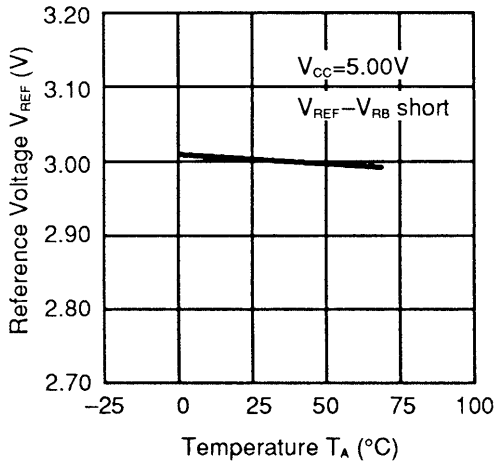


Figure 5. Reference Voltage vs. Temperature

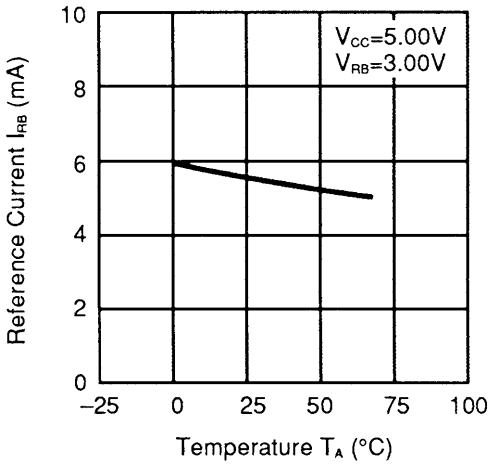


Figure 6. Reference Current vs. Temperature

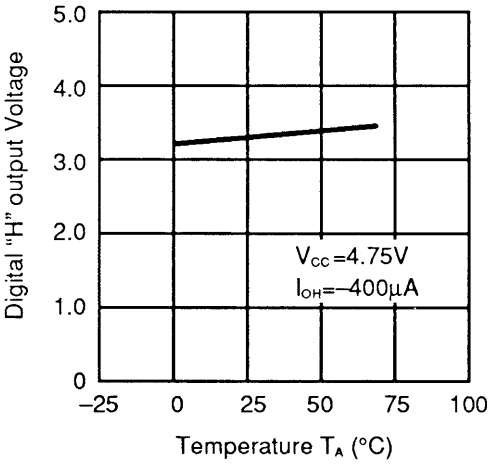


Figure 7. Digital H Output Voltage vs. Temperature

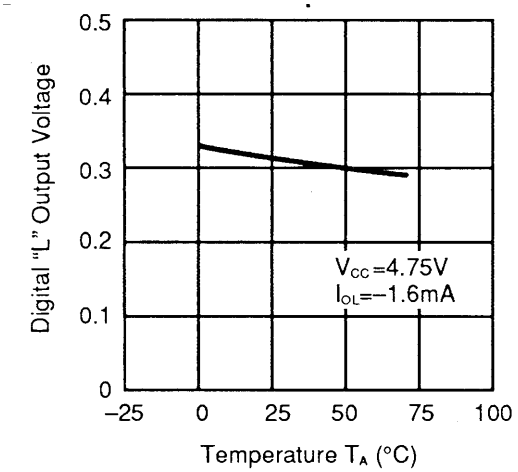


Figure 8. Digital L Output Voltage vs. Temperature

TYPICAL ELECTRICAL CURVES, continued

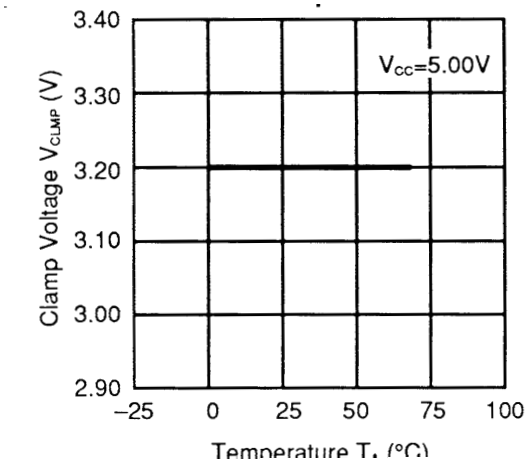


Figure 9. Clamp Voltage vs. Temperature

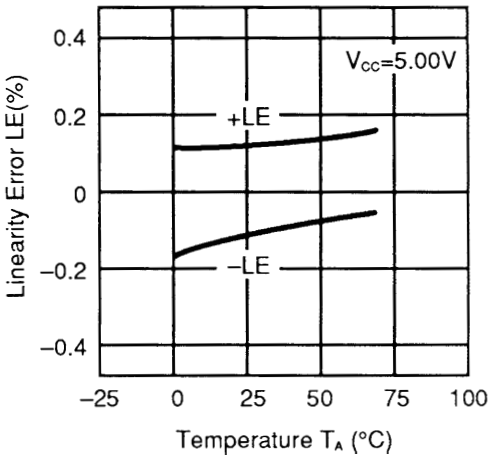


Figure 10. Linearity Error vs. Temperature

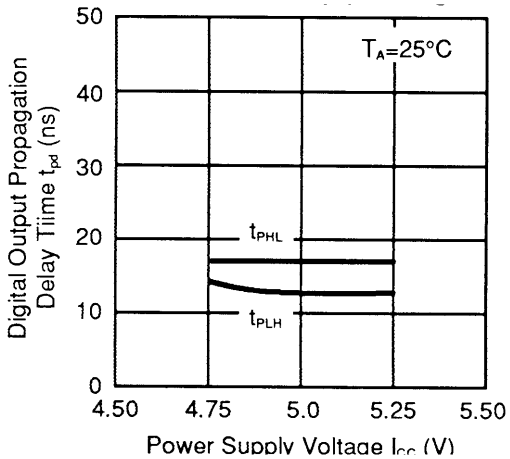


Figure 11. Digital Output Propagation Delay Time vs. Power Supply Voltage

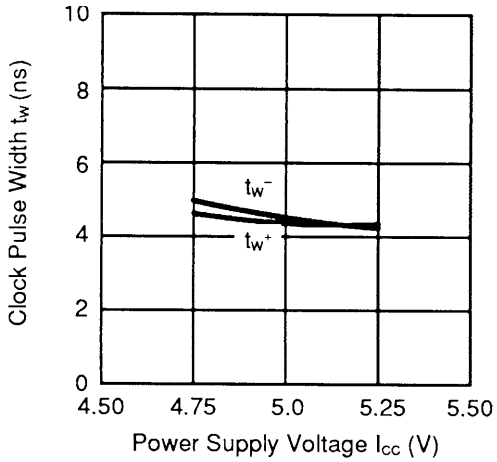


Figure 12. Clock Pulse Width vs. Power Supply Voltage

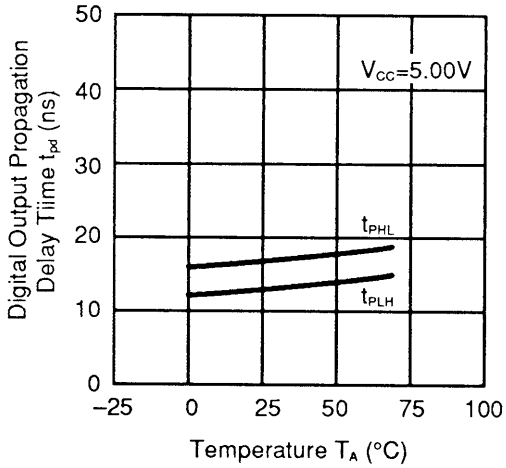


Figure 13. Digital Output Propagation Delay Time vs. Temperature

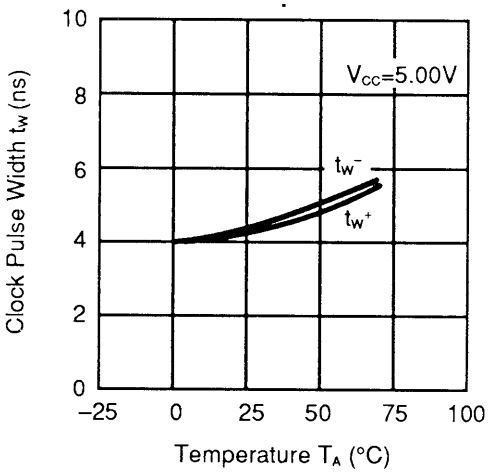


Figure 14. Clock Pulse Width vs. Temperature

TYPICAL ELECTRICAL CURVES, continued

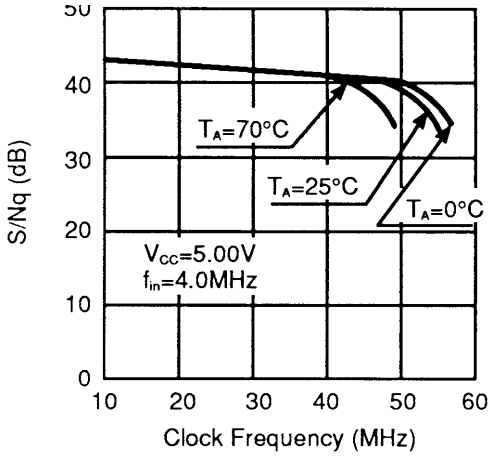


Figure 15. S/Nq (dB) vs Clock Frequency (RMS Signal/RMS Noise)

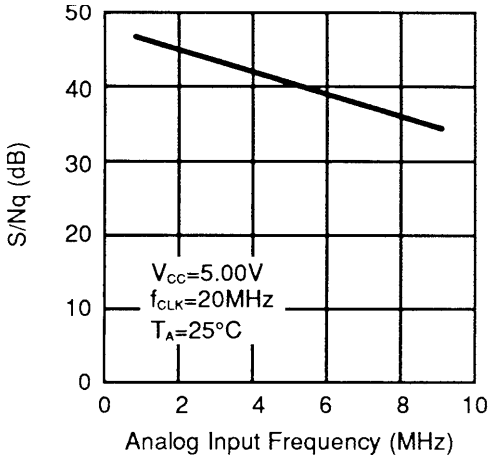


Figure 16. S/Nq (dB) vs. Analog Input Frequency

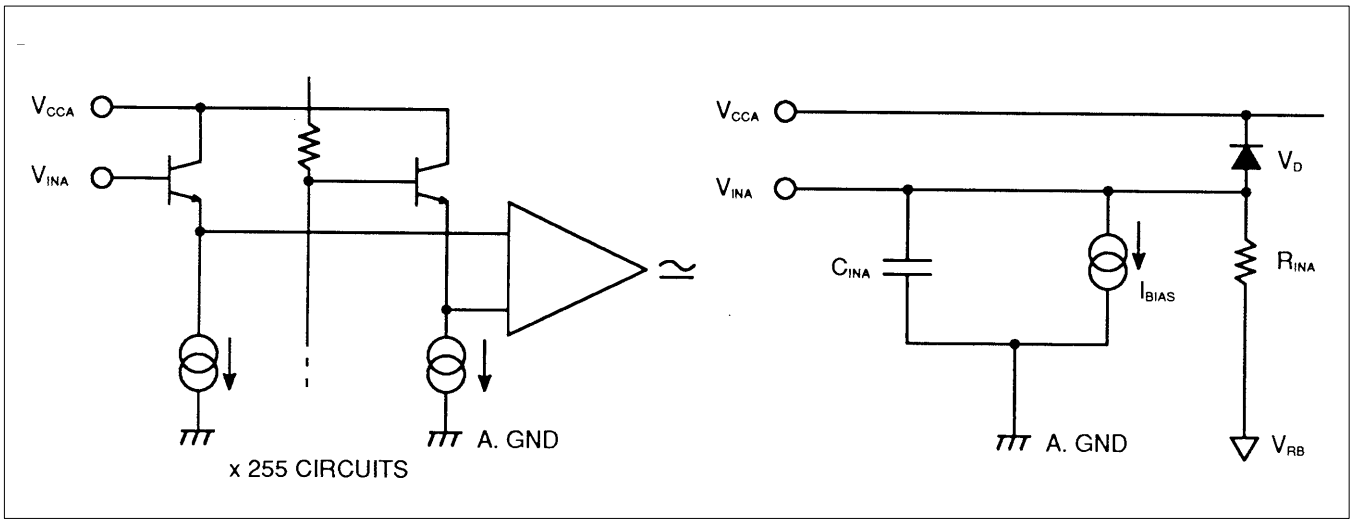


Figure 17. Analog Input Equivalent Circuit

C_{INA} – Nonlinear emitter-follower junction capacitance
R_{INA} – Linear resistance model for input current transition by comparator switching: Infinite value for $V_{INA} < V_{RB}$ or when CLK=High
V_{RB} – Voltage at VRB terminal
IBIAs – Constant input bias current
V_D – Base-collector junction diode of emitter-follower transistor

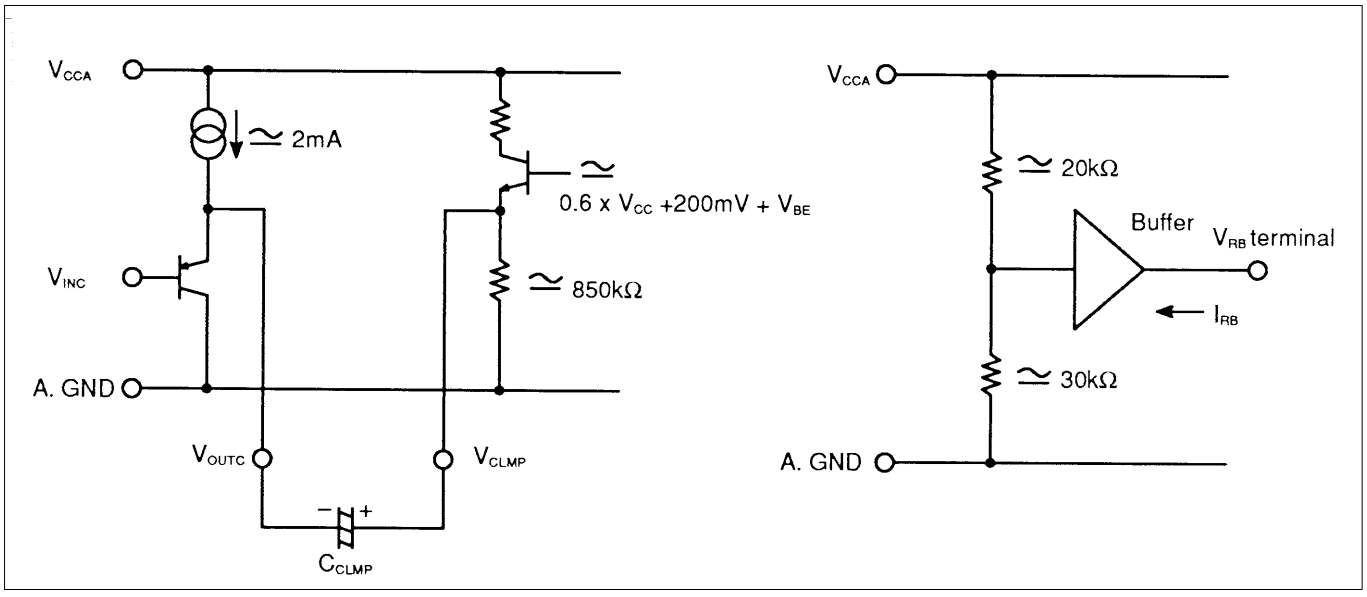


Figure 18. Clamp Equivalent Circuit

Figure 19. Reference Equivalent Circuit

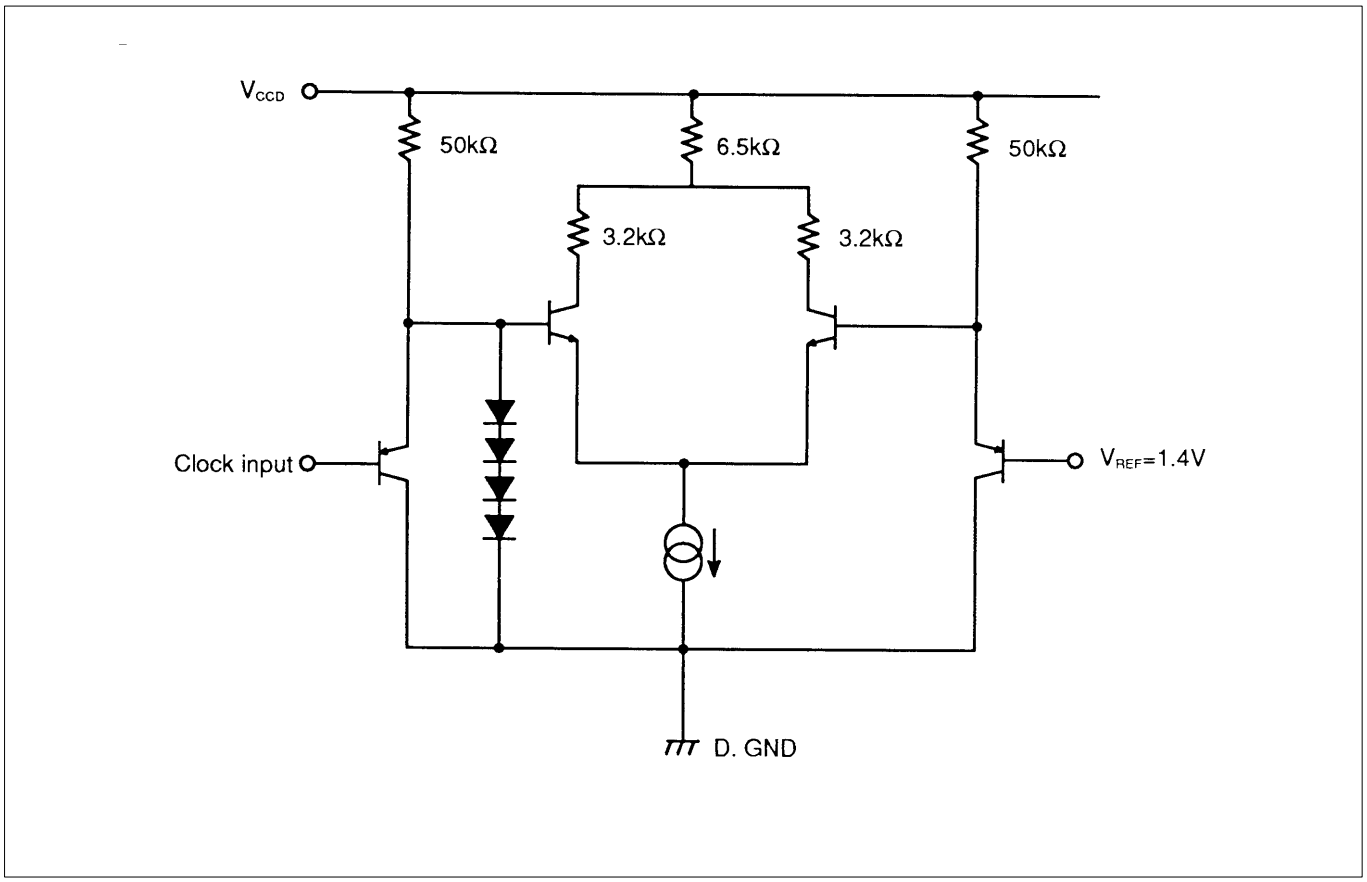


Figure 20. Digital Input Equivalent Circuit

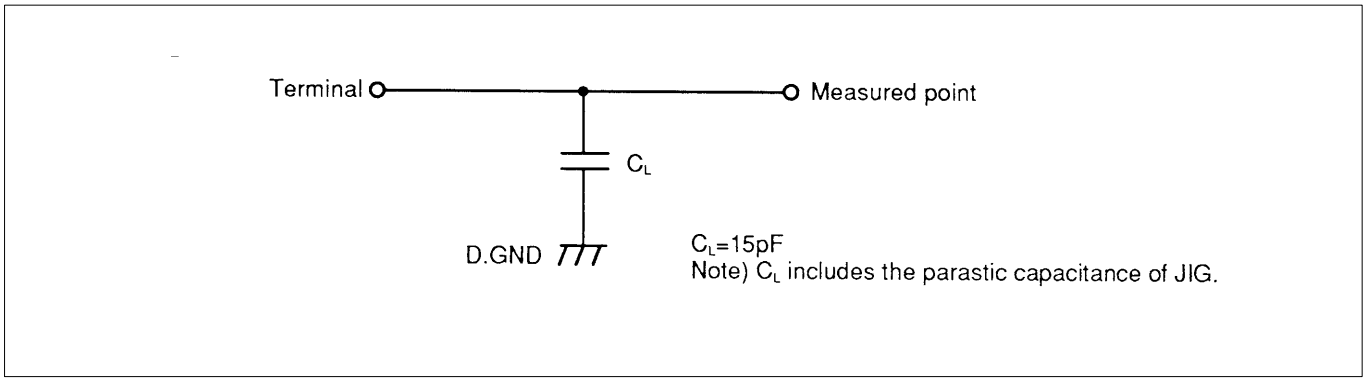


Figure 21. Load Circuit For Output Buffer

LINEARITY ERROR

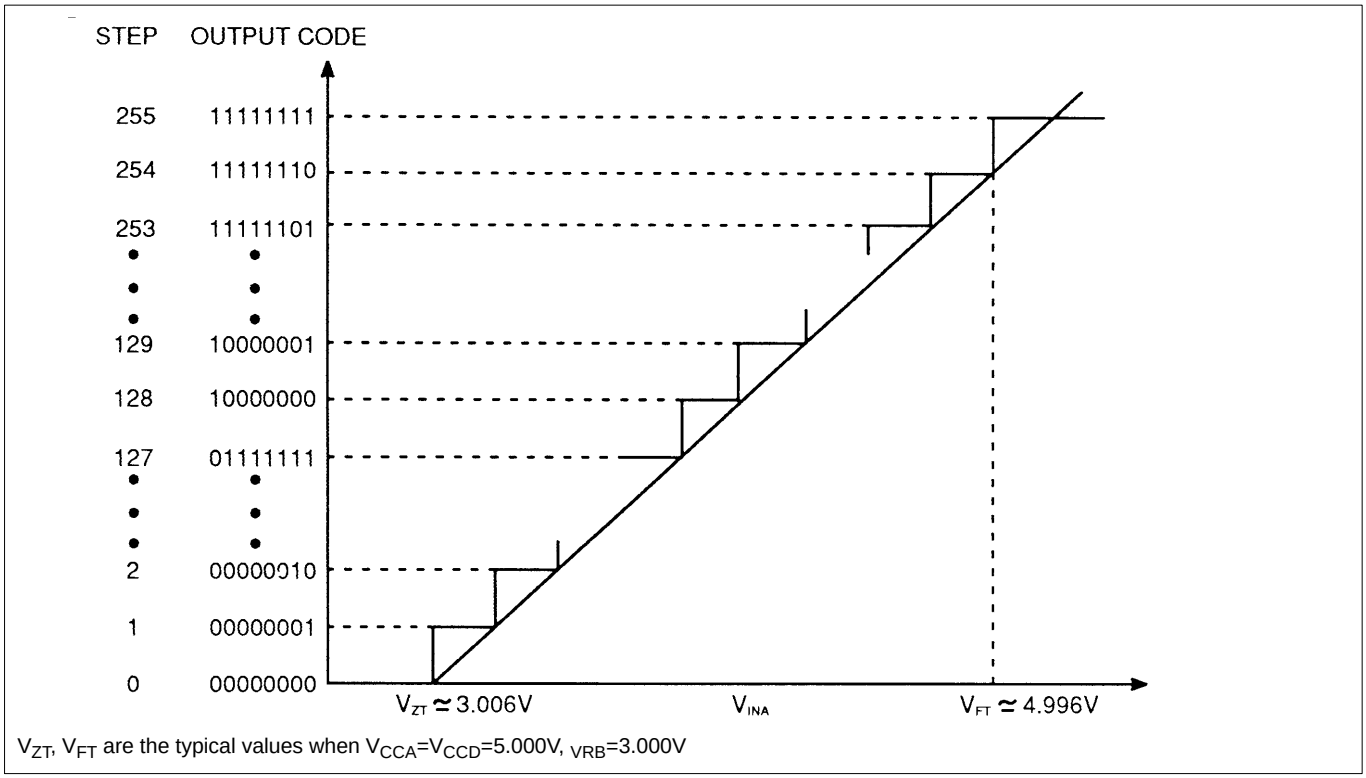


Figure 22. Ideal Conversion Characteristic

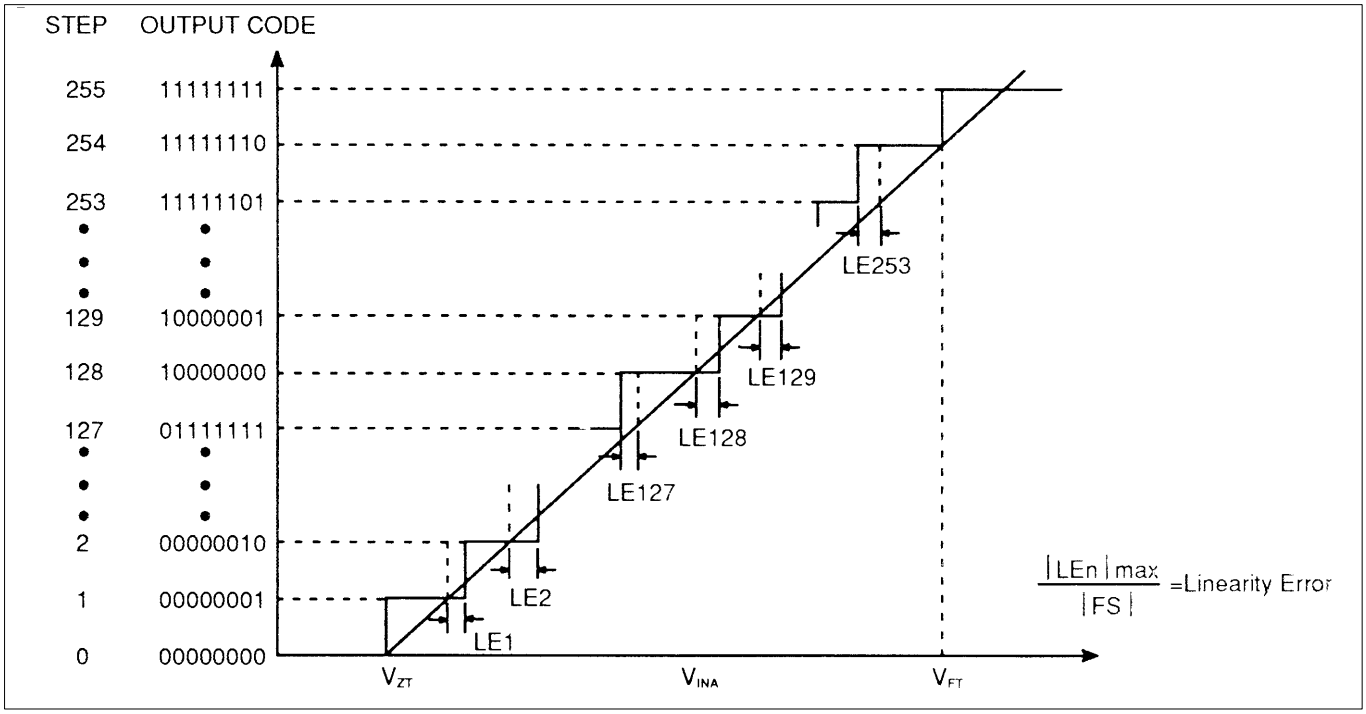


Figure 23. Actual Conversion Characteristic

CLAMP CIRCUIT OPERATION

Please note the following when clamp circuit is not applied.

Terminal	Contents
V_{INC}	Short with GND pin
V_{OUTC}	Open
V_{CLMP}	Open

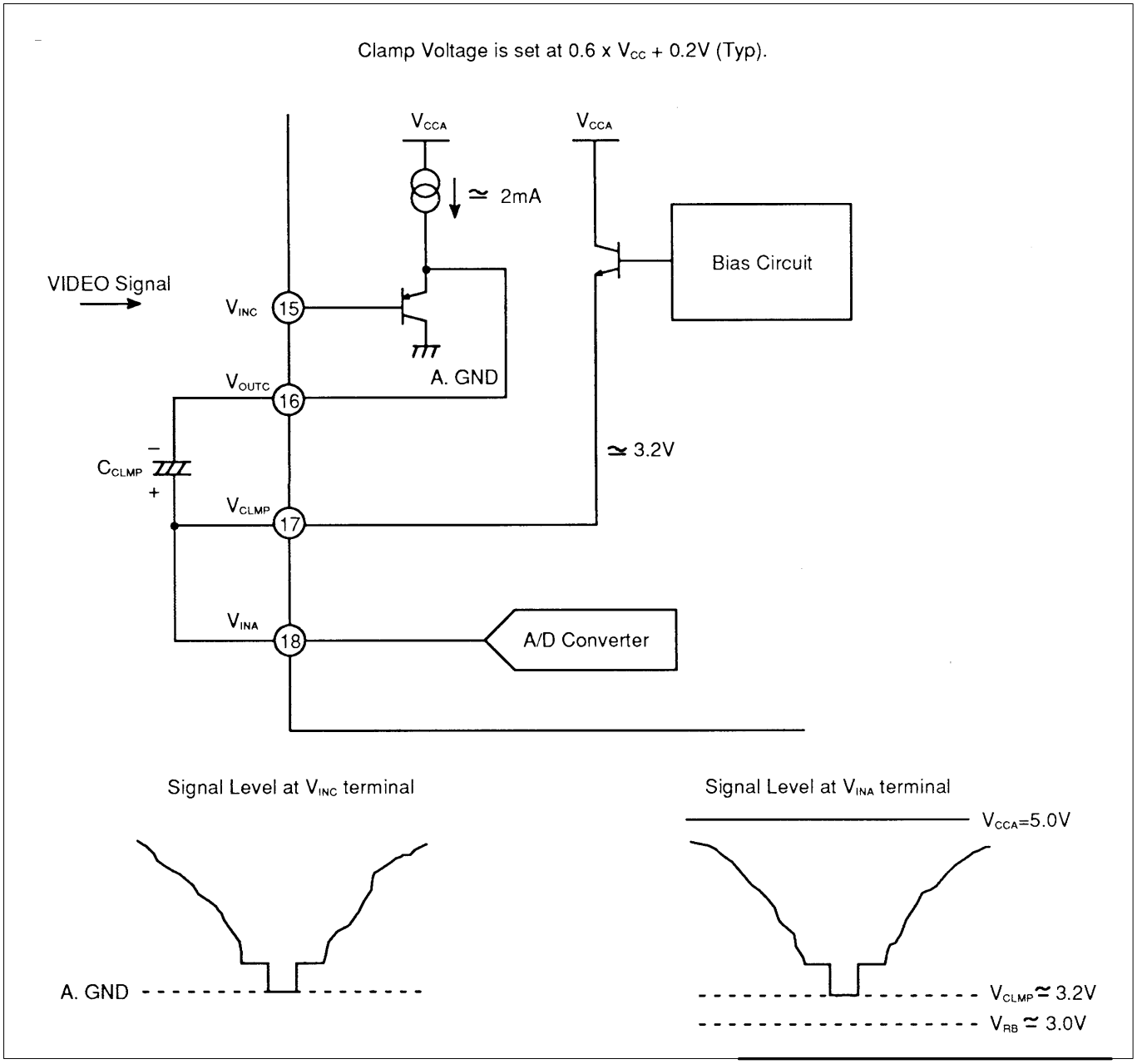


Figure 24. Clamp Circuit

TYPICAL CONNECTION CIRCUIT

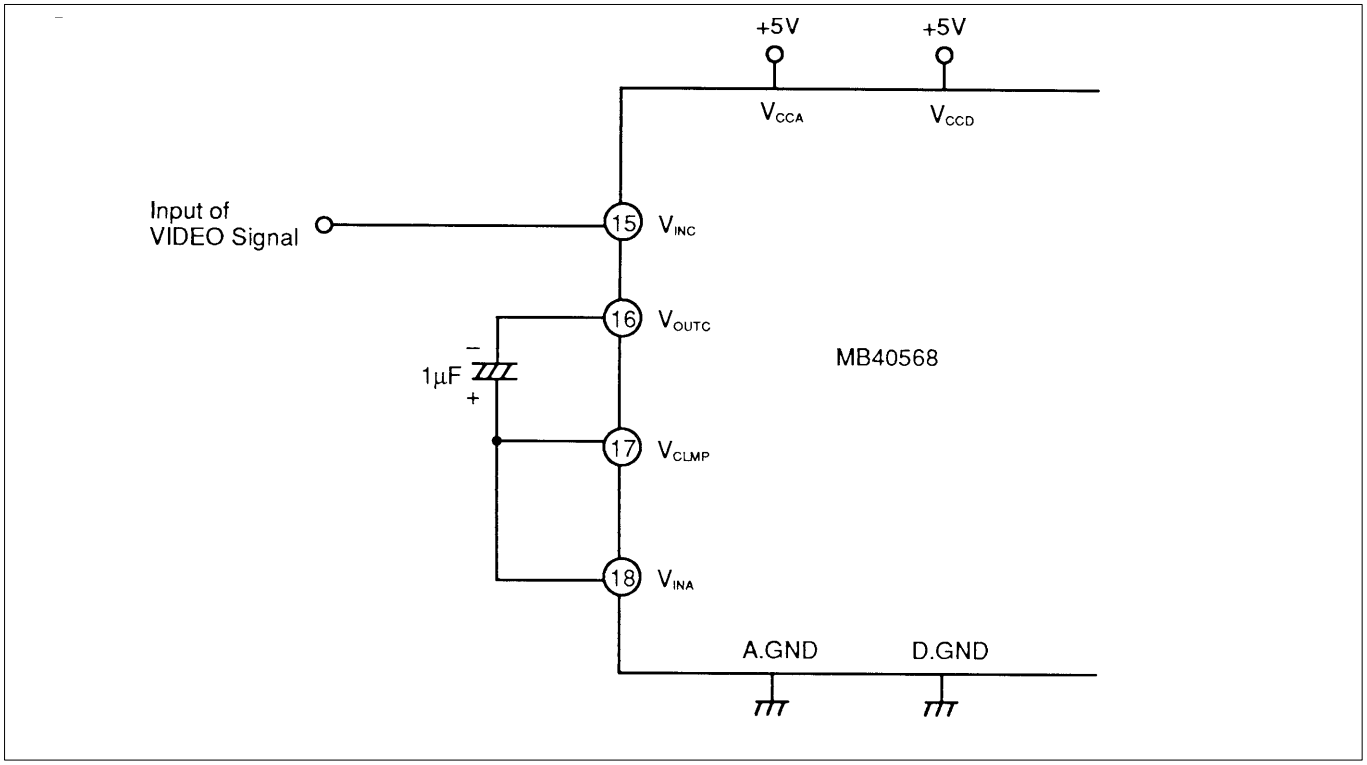


Figure 26. Example for Applying On-Chip Input PNP Tr. of MB40568

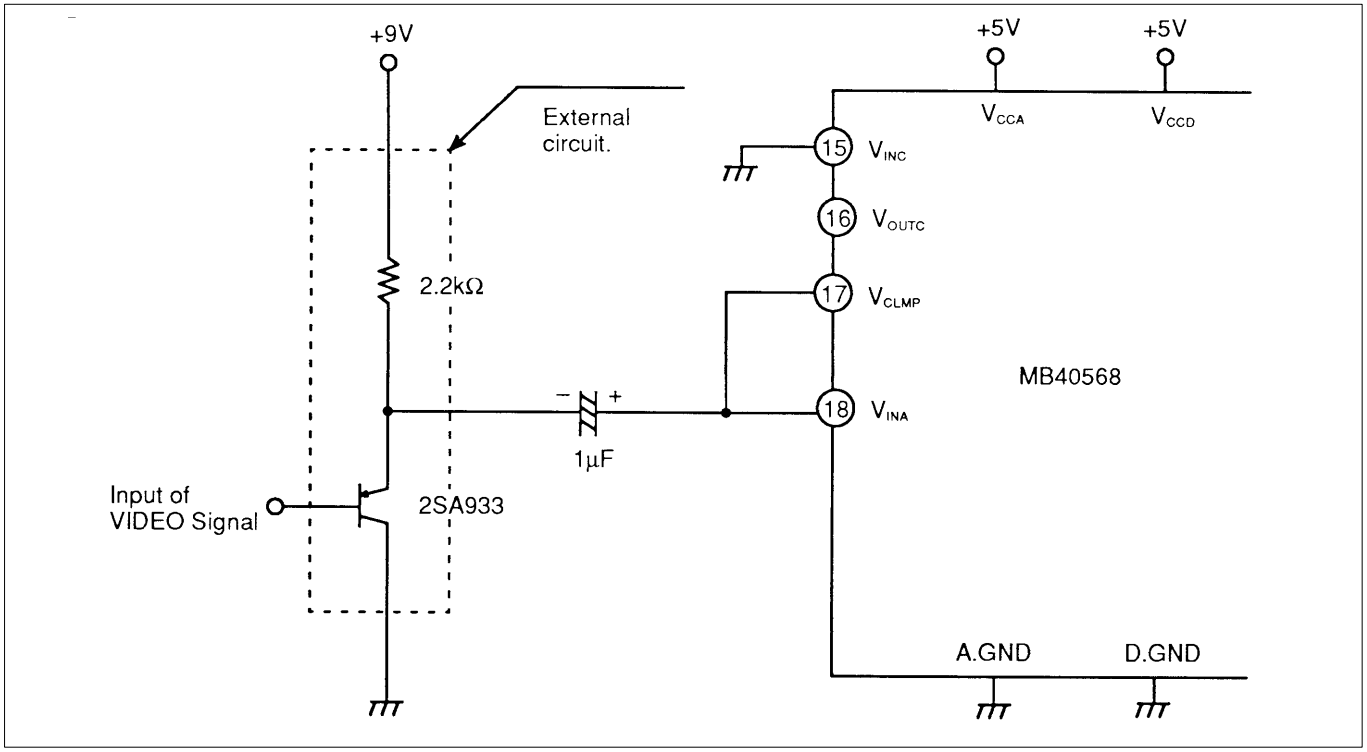
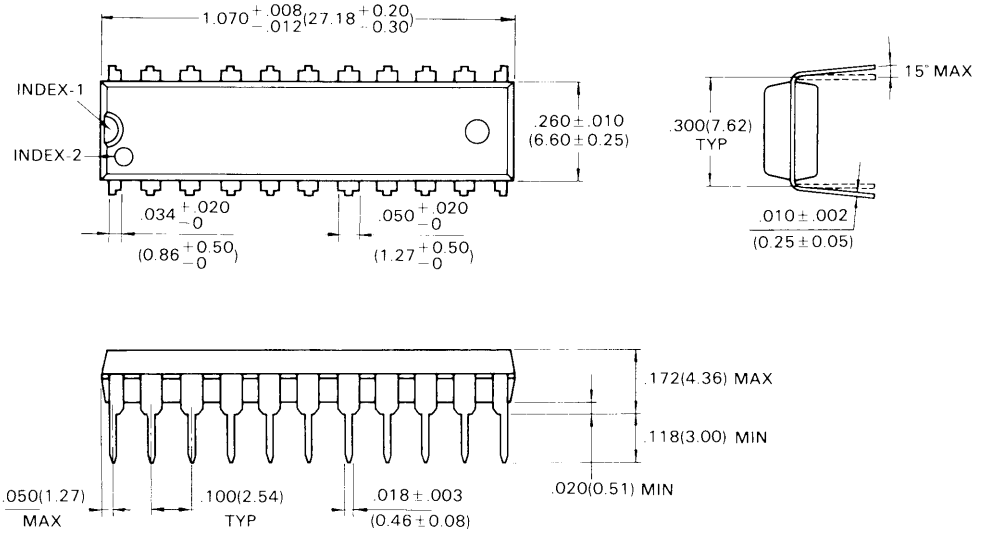


Figure 27. Example for Applying External Clamp Circuit Input PNP Tr.

PACKAGE DIMENSIONS

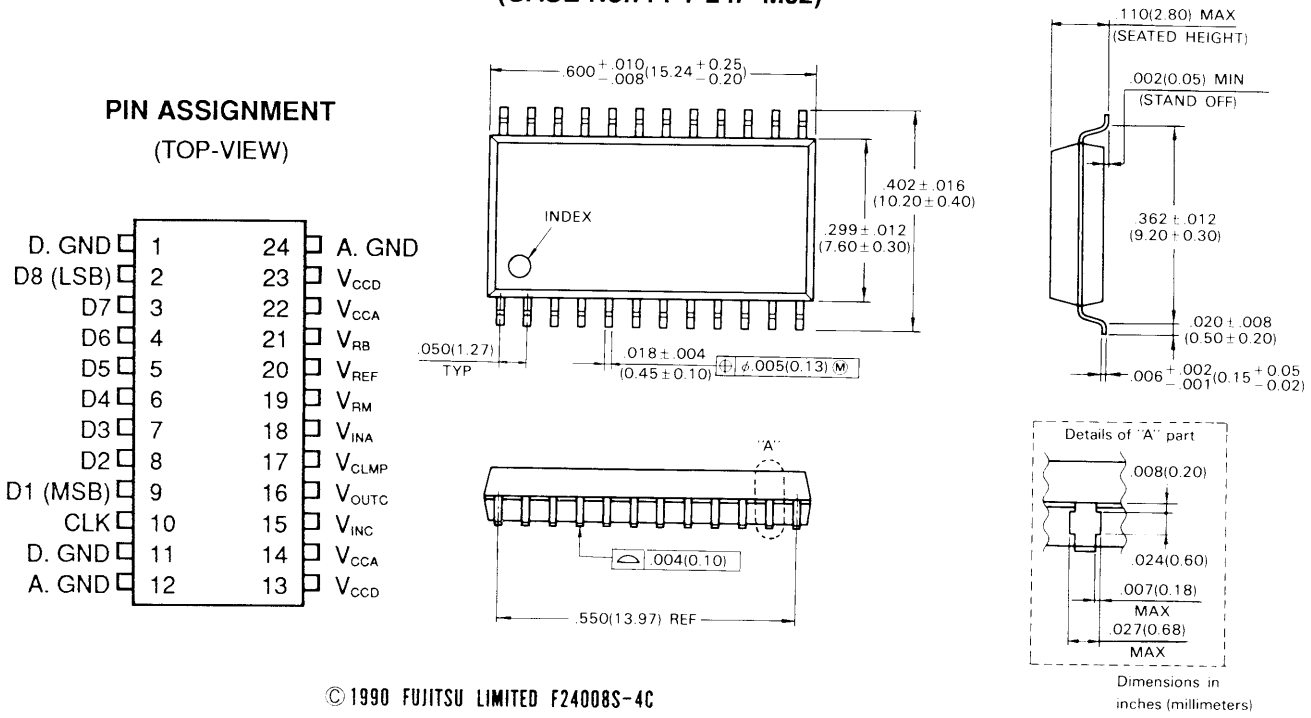
22-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-22P-M04)



Dimensions in inches (millimeters)

24-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: FPT-24P-M02)



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