DS04–21213–1aE

FUJITSU

DATA SHEET

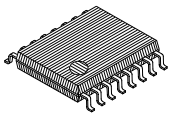
MB87094 *ASSP*

Serial Input PLL Frequency Synthesizer

CMOS SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH POWER SAVING FUNCTION

The Fujitsu MB87094 is a CMOS serial input Phase Locked Loop (PLL) frequency synthesizer. It incorporates an input amplifier, a programmable divider (binary 11-bit programmable counter and binary 7-bit swallow counter), a phase comparator, a charge pump, an oscillator circuit, a programmable reference divider (binary 12-bit programmable reference counter), a shift register/control register, a data latch, an intermittent mode control circuit. A power save control input pin (PS) for the intermittent mode control circuit is used to switch between the stand-by and active modes. This is used for phase synchronization at the beginning of operation from a stand-by mode. The MB87094 permits construction of PLL frequency synthesizers with operating frequencies of up to 15 MHz.

PRELIMINARY



(FPT-16P-M05)

FEATURES

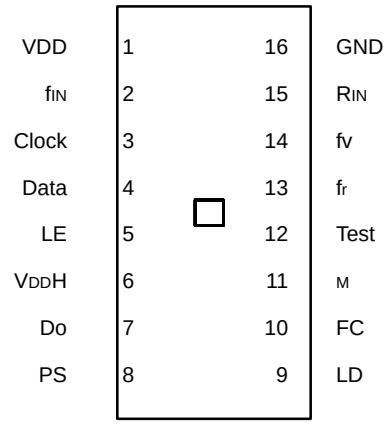
- Low power supply voltage: VDD = 1.1 to 1.7V
  $V_{DD}H$ = 2.6 to 3.3V
- Intermittent mode control circuit
- Ambient temperature range : TA = –10°C to 50°C
- Plastic 16-pin SSOP package (Suffix: –PFV)
- Setting the divide ratio
  Use the below formula to define the parameters for setting the divide ratio

  $\underline{fVCO} = (\underline{N} \times \underline{M} \div \underline{A}) \times (\underline{fOSC} \div \underline{R})$ (N>A)

  (fVCO) Output frequency of the external VCO
  (N) Preset divide ratio of binary11-bit programmable counter (5 to 2047)
  (M) Preset modulus of external dual modulus prescaler (M/M+1)
  (A) Preset divide ratio of binary 7-bit swallow counter value (0 to 127)
  (fOSC) Reference oscillator frequency
  (R) Preset divide ratio of binary 12-bit programmable reference counter (5 to 4095)

This device contains circuitry to protect the inputs against dam age due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high im-pedance circuit.

PIN ASSIGNMENT
(TOP VIEW)



(GND=0V)

Rating	Symbol	Value	Unit
ABSOLUTE MAXIMUM RATINGS (See NOTE)			
Supply voltage	V_{DD}	–0.5 to +5.0	V
	$V_{DD}H$	–0.5 to +5.0	V
Input voltage	V_{IN}	–0.5 to V_{DD}+0.5	V
	$V_{IN}H$	–0.5 to $V_{DD}H$+0.5	V
Output voltage	V_{OUT}	–0.5 to V_{DD}+0.5	V
	$V_{OUT}H$	–0.5 to $V_{DD}H$+0.5	V
Output current	I_{OUT}	±10	mA
Ambient temperature	T_A	–10 to +50	°C
Storage temperature	Tstg	–40 to +125	°C
Power dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

Pin No	Symbol	I / O	Interface *1	Pin Description
1	V_{DD}	–	1V	Power supply pin
2	f_{IN}	I	1V	Programmable divider input pin, and has a bias circuit and an amplifier. Connect an external voltage controlled oscillator (VCO) with AC coupling.
3	Clock	I	3V	Clock input pin for the shift register. Data are loaded at the rising edge of clock. A schmitt trigger circuit is used.
4	Data	I	3V	Serial data input pin for setting divide ratio of dividers. A schmitt trigger is used.
5	LE	I	3V	Load enable signal input pin. When LE is set to high, the data in the shift register is sent to the latch. A schmitt trigger is used.
6	$V_{DD}H$	–	3V	Power supply pin
7	Do	O	3V	Tri-state charge pump output pin. A constant-current feed charge pump is used, and its output current can be controlled by the external resistor R_{RC}. Do output level is inverted by FC. The charge pump output level is changed according to combination of the programmable reference divider output frequency fr and the programmable divider output frequency fv.
8	PS	I	3V	Power save control pin. When PS is set to ”H”, an active mode is selected. When PS is set to ”L”, a stand by mode is selected. *2
9	LD	O	3V	Phase comparator output pin. When a PLL is locked, this pin outputs ”H”. When the PLL is unlocked, outputs ”L”.
10	FC	I	3V	Phase comparator input switch pin. *3
11	M	O	3V	Control output for external dual modulus prescaler.This output level is synchronized with falling edge of fin input signal. Pulse swallow function: M = ”H” : Preset modulus factor M of an external prescaler. M = ”L” : Preset modulus factor M+1 of an external prescaler.
12	Test	I	1V	Test mode pin. Test mode is selected by setting this pin to ”H”. Leave this pin open for ordinal operation, because pull-down resistor is used.
13	fr	O	1V	Monitoring pin for the programmable reference divider output.
14	fv	O	1V	Monitoring pin for the programmable divider output.
15	R_{IN}	I	1V	Connect pin with external reference oscillator (TCXO, etc.). A bias circuit and an amplifier are used. Connect TCXO with AC coupling.
16	GND	−	−	Ground pin.

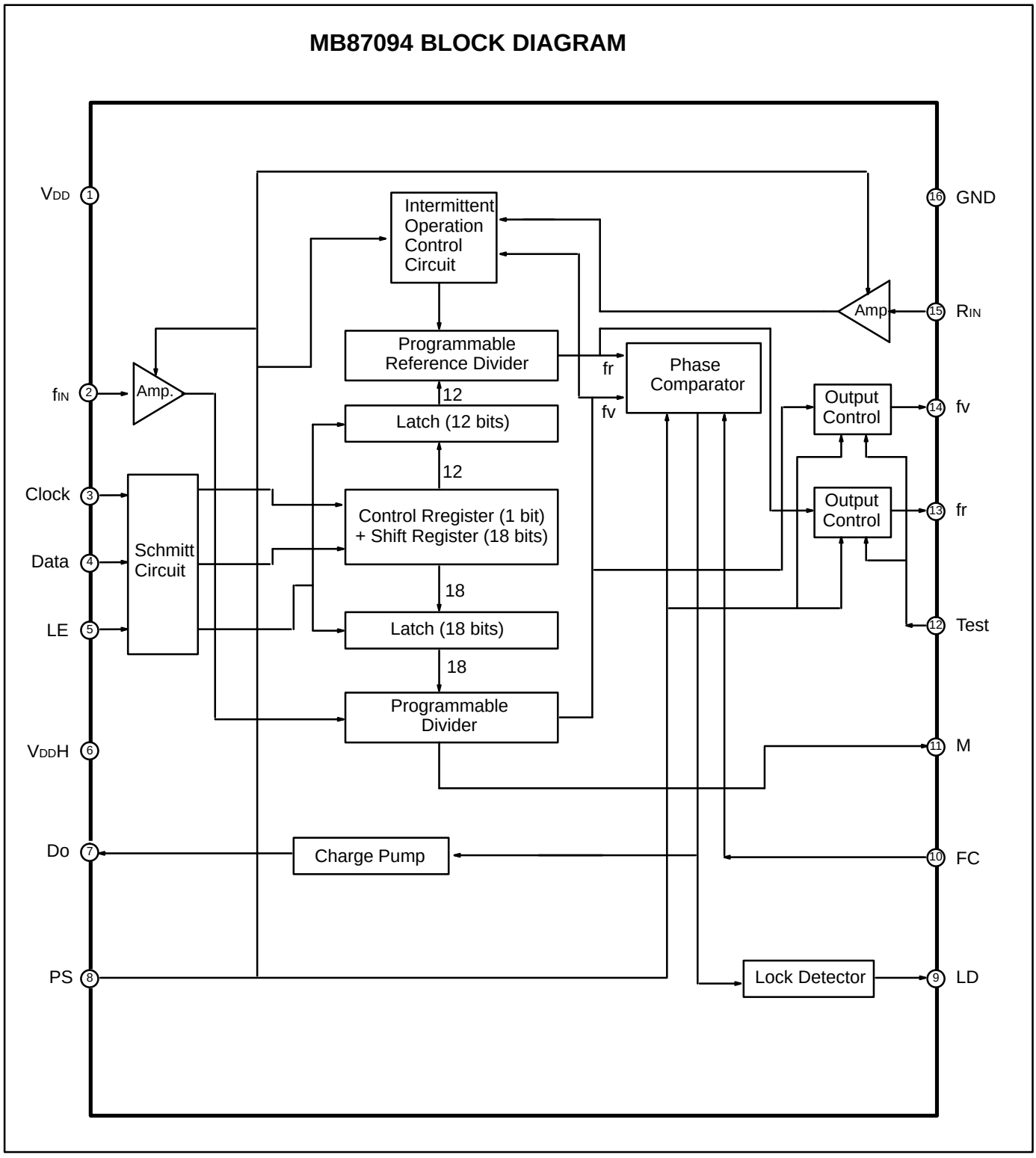
Note:

*1 : In consideration of interface with external circuits like a micro controller, each pin is set to either 3V interface or 1V interface.

*2 : When power is impressed, PS pin have to be set to ”L”. Refer to an intermittent operation in functional description.

*3 : Refer to phase comparator in functional description.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTIONS

1. Circuit Description

1.1 Intermittent Operation

The intermittent operation of the MB87094 refers to the process of activating and deactivating its internal circuit as necessary thus saving electric energy otherwise consumed by the circuit. If the circuit is simply restarted from the standby state, however, the phase relationship between the reference frequency (fr) and the programmable frequency (fv), which are the input to the phase comparator, is not stable even when they are of the same value. This may cause the phase comparator to generate an excessively large error signal, resulting in an out-of-synch lock frequency.

To preclude the occurrence of this problem, the MB87094 has an intermittent mode control circuit which forces the frequencies into phase with each other when the MB87094 is reactivated, thus minimizing the error signal and resultant lock frequency fluctuations. The intermittent mode control circuit is controlled by the PS pin. Setting pin PS high provides the normal operation mode and setting the pin low provides the standby mode and places the MB87094 into the stand–by state. The MB87094 behavior in the active and stand–by modes is summarized below.

- Active mode (PS = “H”)
  All MB87094 circuits are active and provide the normal PLL operation.

- Stand-by mode (PS = “L”)
  The MB87094 stops every circuit that consumes power heavily and that cause little inconvenience when deactivated and enters the low-power dissipation state. D_O and LD pins take the same state as when the PLL is locked. D_O pin becomes a high-impedance state and the input voltage to the voltage control oscillator (VCO) is maintained at the same level as in active mode (that is, lock state) according to a time constant of a low pass filter (LPF). Consequently, the output frequency from the VCO (f_{VCO}) is maintained at approximately the lock frequency.

  The MB87094 continues the intermittent mode operation by alternating the active and stand-by modes. When it switches from stand-by to active modes, it forces the phase of fr and fp to correspond for minimizing the error signal. In this way, the MB87094 can keep the power consumption of its entire circuitry to the minimum.

  The MB87094 must be placed in the stand-by mode (PS = “L”) when power is impressed.

1.2 Programmable Divider

The f_{VCO} of an external VCO output signal or the f_{PSC} of an prescaler output signal, input through fin, are divided by the programmable divider and then output to the phase comparator as fv. It consists of a binary 7-bit swallow counter, a binary 11-bit programmable counter, and a controller which controls the divide ratio of the prescaler.

The following are their divide ratios:

- Swallow counter: A = 0 to 127
- Programmable counter: N = 5 to 2047

The MB87094 uses the pulse swallow method; consequently, the divide ratios of the swallow and programmable counters must satisfy the relationship N > A.

On the supposition that divide ratio of a prescaler is M/M+1 (M=128), the total divide ratio of the programmable divider is calculated as follows:

Total divide ratio = (M+1)xA+Mx(N–A) = MxN+A = 128xN+A

When N is set within $5 \leq N \leq 127$, the divide ratio A of the swallow counter can take values $0 \leq A \leq N-1$ because N must be greater than A. For example, $0 \leq A \leq 19$ is allowed when N = 20 but $20 \leq A \leq 127$ is not allowed in that case. Consequently, $N \geq 128$ must be satisfied for the total divide ratio to be set within $0 \leq A \leq 127$.

1.3 Programmable Reference divider

The programmable reference divider divides the reference oscillation frequency (f_{OSC}) from an external reference oscillator (TCXO) connected with AC coupling, and output fr to the phase comparator. It consists of a 12–bit binary programmable reference counter.

The following divide ratio is used:

- Programmable reference counter: R = 5 to 4095

The fr and fOSC have the following relationship:

- fr = fOSC ÷ R

1.4 Phase Comparator

The phase comparator detects the phase difference between the outputs fr and fv and generates an error signal that is proportional to the phase difference. The outputs from the phase comparator include 1) DO which takes on one of the three states, namely, “L” (low), “H” (high), and “Z” (high impedance), 2) LD which indicates the PLL lock or unlock state.

1.4.1 Phase Comparator

The phase comparator detects the phase difference between fr and fv and generates an error signal that is proportional to the phase difference. The roles of the fr and fp supplied to the phase comparator may be reversed by switching the logical input level of pin FC. This inverts the logical level of the DO output. The logical level of DO may be selected according to the characteristics of the external LPF and the VCO. (Refer to Table 1.)

Table 1. Phase Comparator Inputs/Output Relationships

Phase Relationship \ Output	FC=“L”	FC=“H”
	DO	DO
fr > fv	L	H
fr = fv	High-Impedance	
fr < fv	H	L

1.4.2 Phase Comparator Input/Output Waveforms

The phase comparator outputs logic levels summarized in Table 1, according to the phase difference between fr and fv phase differences. The pulse width of the phase comparator outputs are identical and equal to the phase difference between fr and fv as shown in Figure 1.

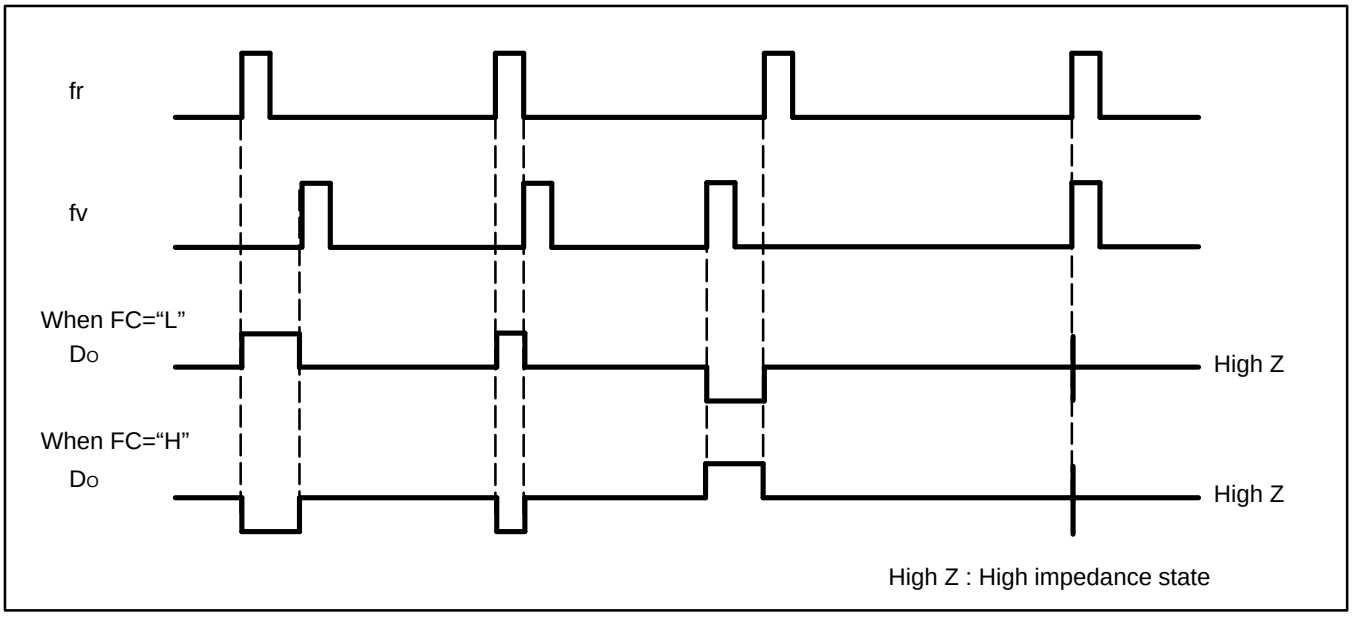


Figure 1. Phase Comparator Input/Output Waveforms (Charge Pump)

1.4.3 Lock Detector

The lock detector detects the lock and unlock states of the PLL. The lock detector outputs “H” when the PLL enters the lock state and outputs “L” when the PLL enters the unlock state as shown in Figure 2. When pulse width of the error signal is kept zero for four (4) clocks, the lock detector outputs ”H” as a lock signal. When it idetects phase diference after the PLL is locked, ”L” is output at once.

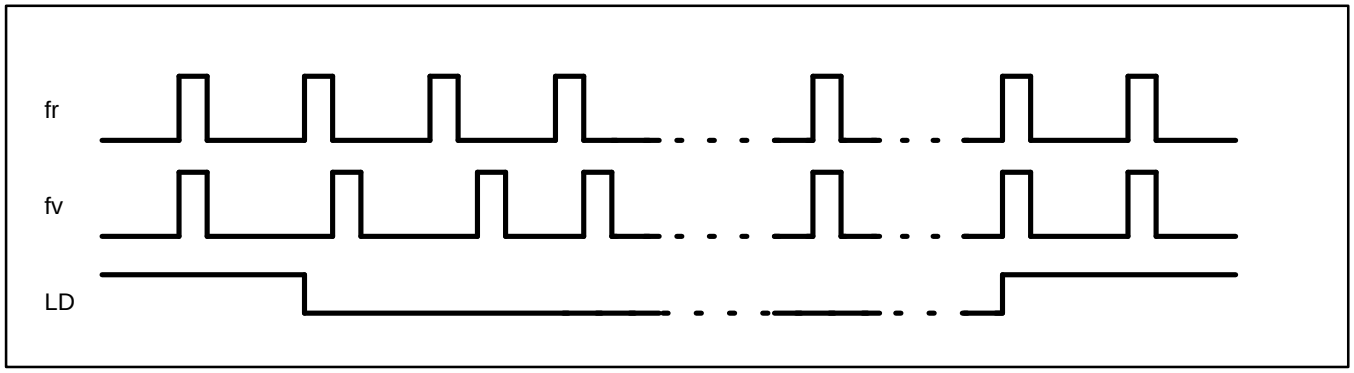


Figure 2. Phase Comparator Input/Output Waveform (Lock Detector)

2. Setting the Divide Ratio

2.1 Serial Data Format

The format of the serial data is shown in Figure 3. The serial data is composed of a control bit and divide ratio setting data. The control bit selects the programmable divider or the programmable reference divider.
In case of the programmable reference divider, serial data consists of 12 bits for the programmable reference counter and 1 control bit as shown in Figure 3.1. In case of the programmable divider, the serial data consists of 18 bits (7 bits for the swallow counter and 11 bits for the programmable counter) and 1 control bit as shown in Figure 3.2.
The control bit is set to 0 to select the serial data for the programmable divider and to 1 to select the serial data for the programmable reference divider.

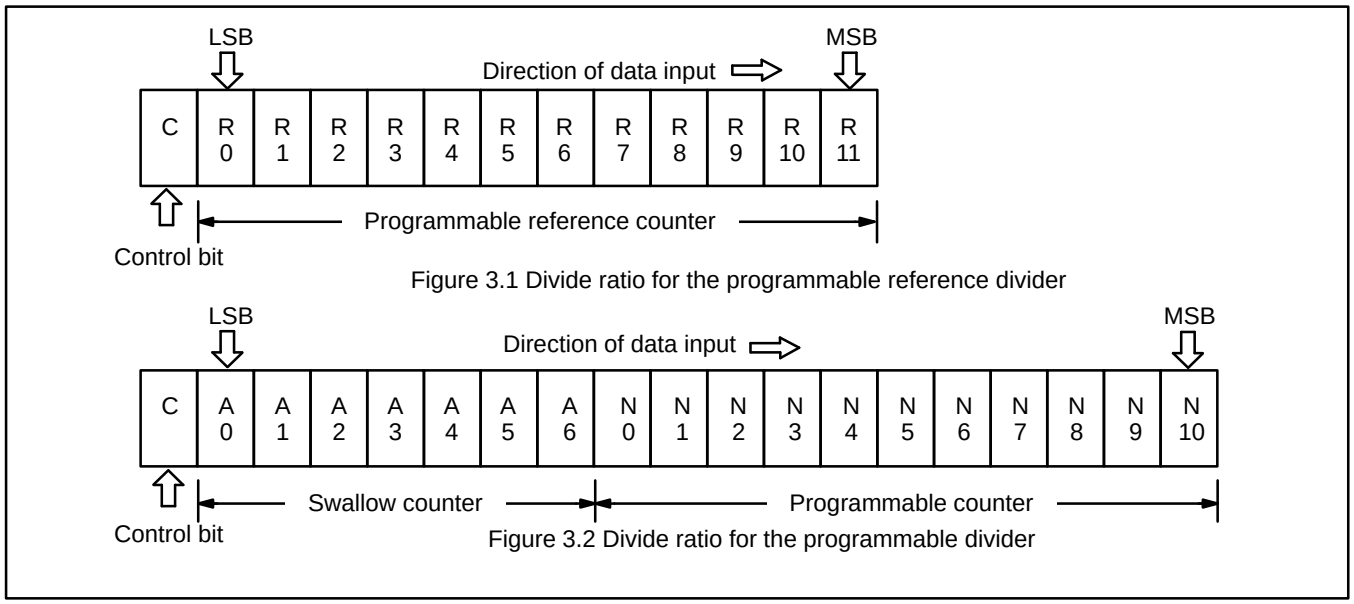


Figure 3. Serial Data Format

2.2 The Flow of Serial Data

Serial data is received via data pin in synchronization with the Clock input and loaded into shift register which contains the divide ratio setting data and into the control register which contains the control bit. The logical product (through the AND gate in Figure 4) of LE and the control register output (i.e., control bit) is fed to the Enable input of the latches. Accordingly, when LE is set high, the latch for the divider identified by the control bit is enabled and the divide ratio data from the shift register is loaded into the selected counter.

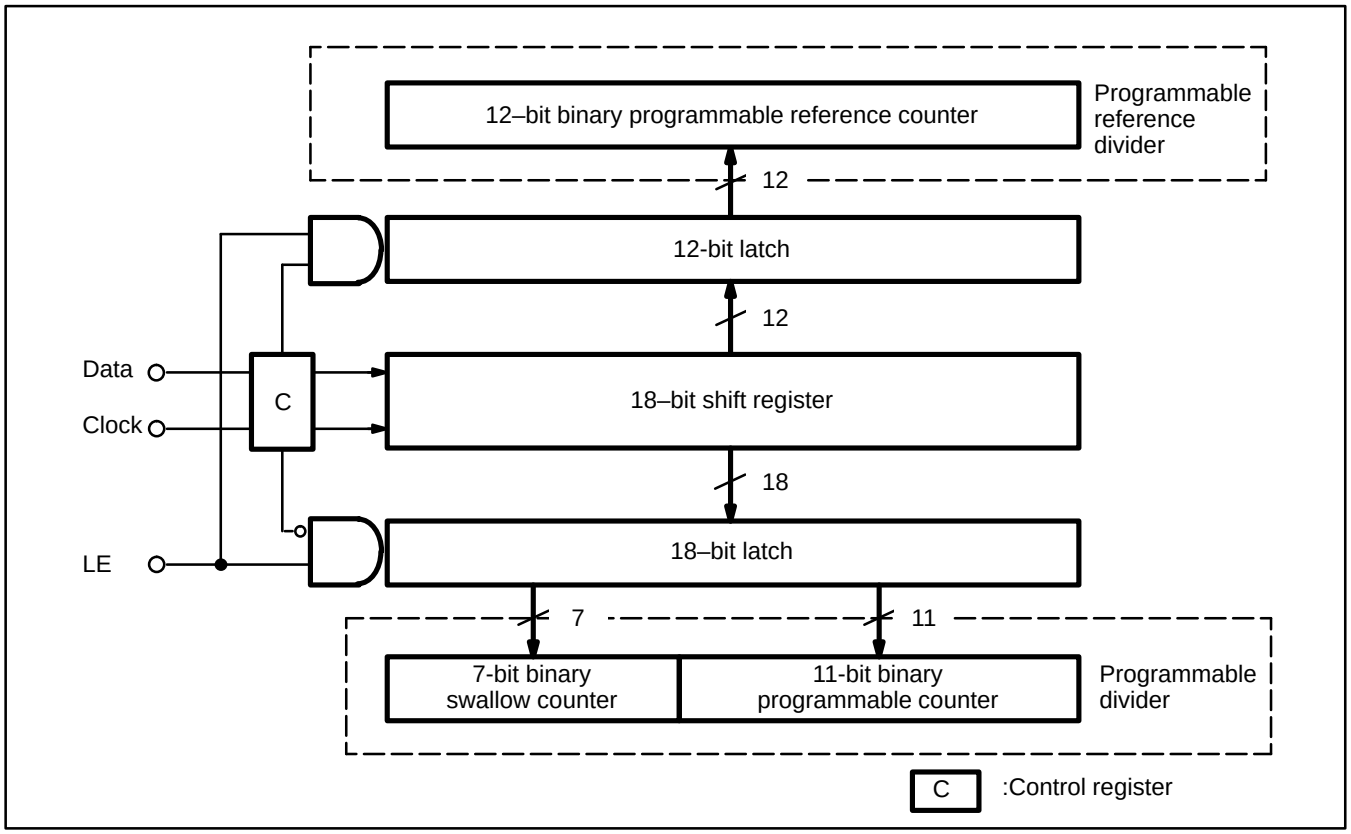


Figure 4. The Flow of Serial Data

2.3 Setting the Divide Ratio for the Programmable Divider

Columns A0 to A6 of Table 2.1 represent the divide ratio of the swallow counter and columns N0 to N10 of Table 2.2 represent the divide ratio of the programmable counter. The control bit is set to 0.

Table 2. Divide Ratio for the Programmable Divider

Table 2.1 Swallow Counter Divide ratio A

Divide ratio A	A 0	A 1	A 2	A 3	A 4	A 5	A 6
0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •
127	1	1	1	1	1	1	1

Table 2.2 Programmable Counter Divide ratio N

Divide ratio N	N 0	N 1	N 2	N 3	N 4	N 5	N 6	N 7	N 8	N 9	N 10
5	1	0	1	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
2047	1	1	1	1	1	1	1	1	1	1	1

2.4 Setting the Divide Ratio for the Programmable Reference Divider

Columns R0–R11 of Table 3 represent the divide ratio of the programmable reference counter. The control bit is set to 1.

Table 3. Divide Ratio for the Programmable Reference Divider

Divide ratio R	R 0	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11
5	1	0	1	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
4095	1	1	1	1	1	1	1	1	1	1	1	1

2.5 Monitor Mode

Setting both the PS pin and TEST pin high, the monitor mode is available. The fr and fv pins output low usually. In the monitor mode, the fr pin outputs signals from the programmable reference divider, and the fv pin outputs signals from the programmable divider.

2.6 Serial Data Input Timing

The MB87094 uses 19 bits of serial data for the programmable divider and 13 bits for the programmable reference divider. When more bits of serial data than defined for the target divider are received, only the last valid serial data bits are effective.
To set the divide ratio for the MB87094 dividers, it is necessary to supply the Data, Clock, and LE signals at the timing shown in Figure 5.

t1 (≥1 µs) :Data setup time t2 (≥1 µs): Data hold time t3 (≥1 µs): Clock pulse width
t4 (≥1 µs) :LE setup time to the falling edge of the last clock t5 (≥1 µs): LE pulse width

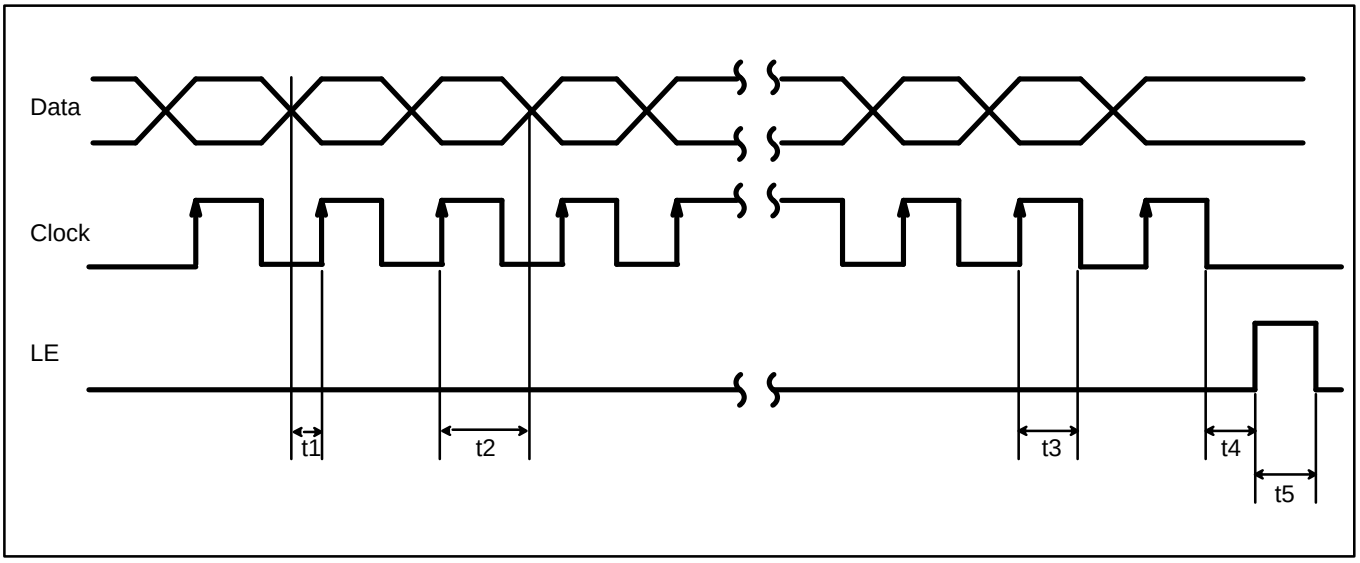


Figure 5. Serial Data Input Timing

Since the divide ratios are unpredictable when the MB87094 is turned on, it is necessary to initialize the divide ratio for both dividers. As shown in Figure 6, after setting the divide ratio for one divider (e.g., programmable reference divider), set LE to the "H" level before setting the divide ratio for the other divider (e.g., programmable divider). To change the divide ratio of one divider after initialization, input the serial data only for that divider (the divide ratio for the other divider is preserved).

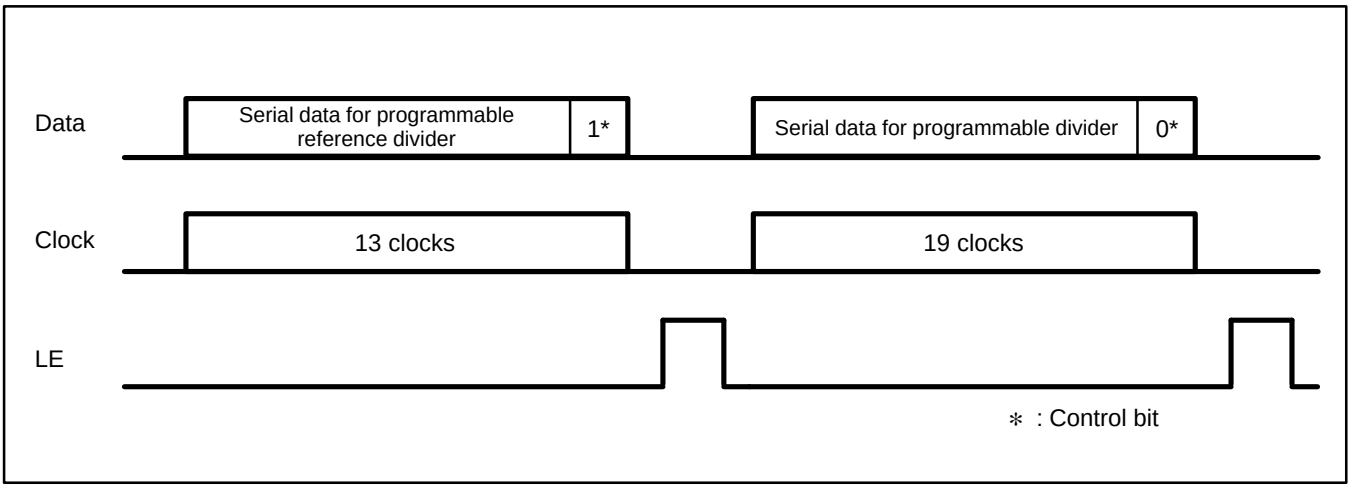


Figure 6 Serial Data Setting Procedure

RECOMMENDED OPERATING CONDITIONS

GND = 0V

Parameter	Symbol	Value	UNIT
Power Supply Voltage	V_{DD}	1.1 to 1.7	V
	$V_{DD}H$	2.6 to 3.3	V
Input Voltage	V_{IN}	GND to V_{DD}	V
	$V_{IN}H$	GND to $V_{DD}H$	V
Ambient Temperature	T_A	–10 to +50	°C

ELECTRICAL CHARACTERISTICS

($V_{DD}H$ = 3.0V, V_{DD} = 1.1V, GND = 0V, T_A = –10 to +50°C)

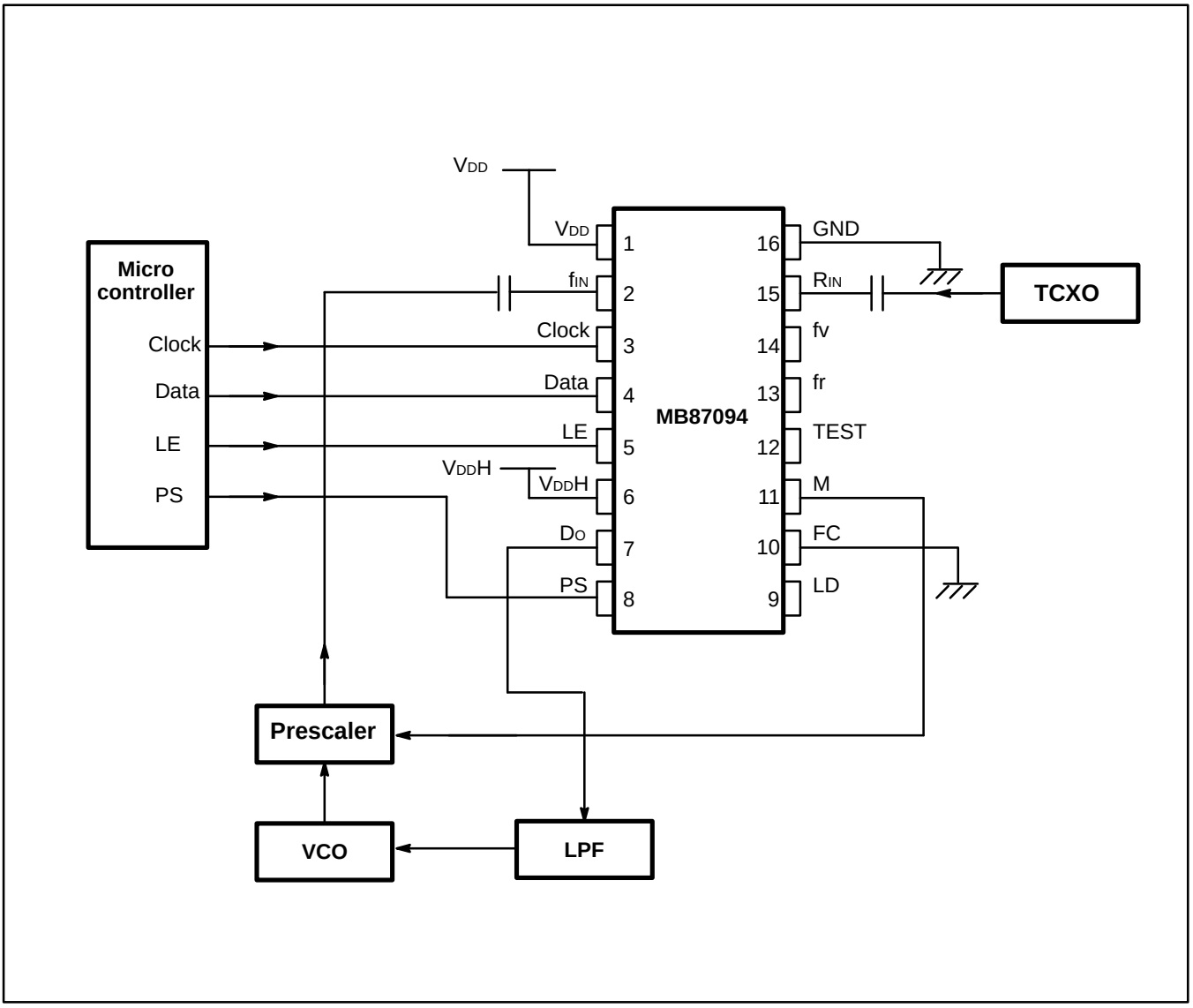
Parameter			Symbol	Conditions	Value			Unit
					Min	Typ.	Max	
Input Voltage	TEST	H Level	V_{IH}		0.77	–	–	V
		L Level	V_{IL}		–	–	0.33	
	CLK, Data, LE, PS, FC	H Level	V_{IH}		2.10	–	–	V
		L Level	V_{IL}		–	–	0.90	
Input Sensitivity	f_{IN}		Vf_{PP}	AC Coupling Amplitude	0.5	–	–	Vp–p Sine
	R_{IN}		Vsin	AC Coupling Amplitude	0.5	–	–	
Input Current	CLK, Data, LE, PS, FC	H Level	I_{IH}	$V_{IH} = V_{DDH}$	–	1.0	–	µA
		L Level	I_{IL}	V_{IL} = GND	–	–1.0	–	
	f_{IN}		If_{IN}	V_I = GND to V_{DD}	–	±30.0	–	µA
	R_{IN}		I_{OSC}	V_I = GND to V_{DD}	–	±30.0	–	µA
	TEST (pull down pin)		I_{TEST}	$V_{IH} = V_{DD}$	–	50.0	–	µA
Output Voltage	fr, fv	H Level	V_{OH}	I_{OH} = 0µA	1.05	–	–	V
		L Level	V_{OL}	I_{OL} = 0µA	–	–	0.05	
	Do, LD, M	H Level	V_{OH}	I_{OH} = 0µA	2.95	–	–	V
		L Level	V_{OL}	I_{OL} = 0µA	–	–	0.05	
Output Current	fr, fv	H Level	I_{OH}	V_{OH} = 0.6V	–0.2	–	–	mA
		L Level	I_{OL}	V_{OL} = 0.5V	0.2	–	–	
	Do, LD, M	H Level	I_{OH}	V_{OH} = 2.5V	–0.4	–	–	mA
		L Level	I_{OL}	V_{OL} = 0.5V	0.4	–	–	
Cutoff Current		Do	IoffH	$V_{OH} = V_{DDH}$	–	–	100	nA
			IoffL	V_{OL} = GND	–	–	100	nA
Supply Current		Active Mode	I_{OP}	∗1	–	–	1.0	mA
		Stand–by Mode	I_{SB}	∗2	–	–	20.0	µA
Maximum Operating Frequency		REF Section	fmaxd	Programmable Reference Divider	15	–	–	MHz
		PD Section	fmaxp	Programmable Divider	15	–	–	

Note;

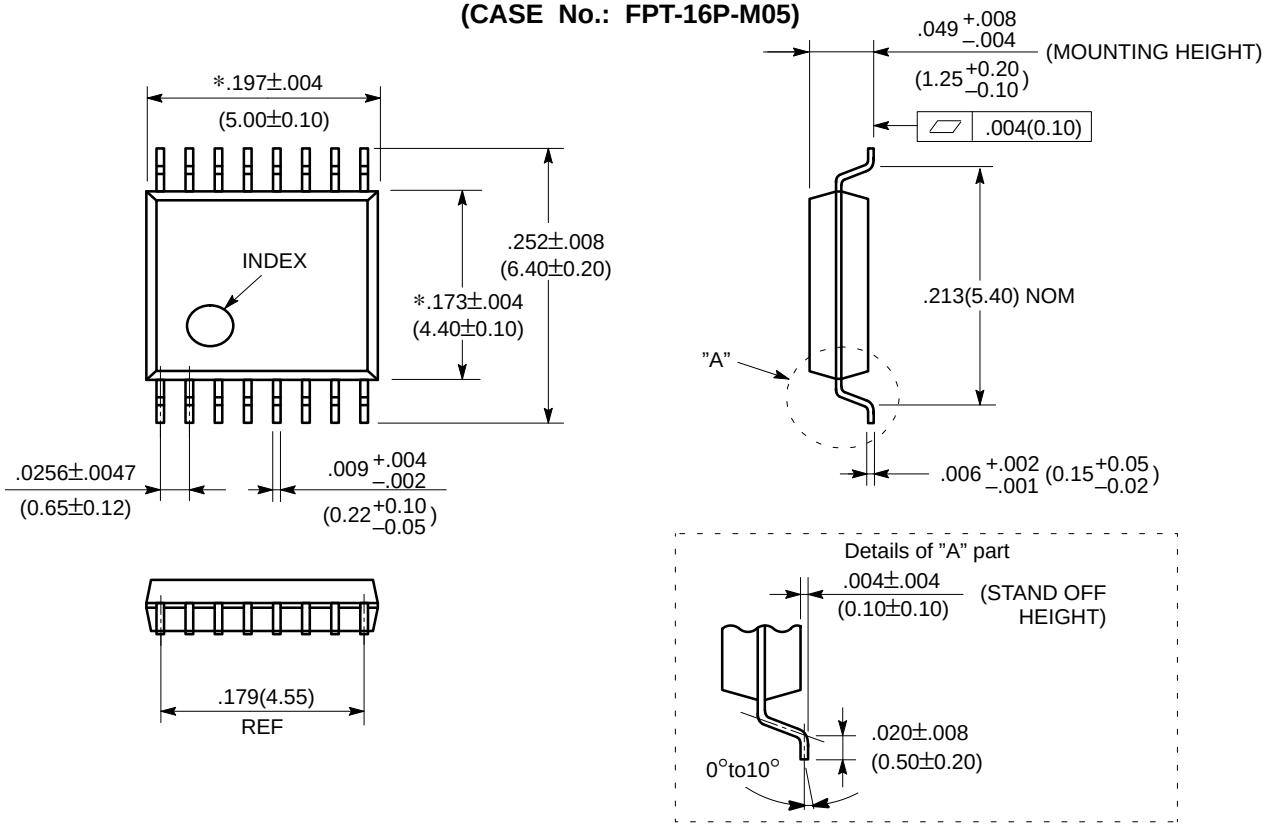
∗1: $f_{IN} = R_{IN}$ = 15 MHz(0.5Vpp), $I_{OP} = I_{DD}$ (1.4V) + $I_{DD}H$ (3V) x 3.3

∗2: Conditions for measuring the stand-by current (I_{SB}) are the same as the case of the active mode (I_{OP}).

TYPICAL APPLICATION EXAMPLE



16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

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