– PRELIMINARY –

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Edition 2.0

FUJITSU

PRODUCT PROFILE SHEET

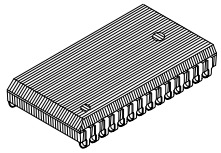
MB81V4800S-60/-70

CMOS 512K X 8 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 524,288 x 8 bit Fast Page Mode Dynamic RAM

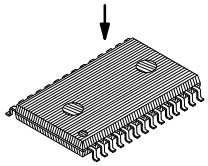
The Fujitsu MB81V4800S is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 8–bit increments. The MB81V4800S features a ”fast page” mode of operation whereby high–speed access of up to 512x8–bits of data can be selected in the same row. The MB81V4800S-60/-70 DRAMs are ideally suited for memory applications such as embedded control, buffer, portable computers, and video imaging equipment where very low power dissipation and high bandwidth are basic requirements of the design.

The MB81V4800S is fabricated using silicon gate CMOS and Fujitsu's advanced four–layer polysilicon process. This process, coupled with three–dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.



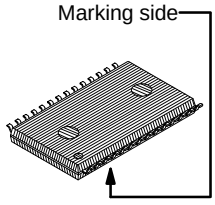
Plastic SOJ Package
(LCC–28P–M05)

Marking side



(FPT–28P–M07)
(Normal Bend)

Marking side



(FPT–28P–M08)
(Reverse Bend)

Plastic TSOP Packages

PRODUCT LINE & FEATURES

Parameter		MB81V4800S-60	MB81V4800S-70
$\overline{RAS}$ Access Time		60ns max.	70ns max.
$\overline{CAS}$ Access Time		20ns max.	20ns max.
Address Access Time		30ns max.	35ns max.
Randam Cycle Time		110ns min.	125ns min.
Fast Page Mode Cycle Time		40ns min.	45ns min.
Low Power Dissipation	Operating current	234mW max.	209mW max.
	Standby current	7.2mW max. (LVTTL level), 3.6mW max. (CMOS level)	

- Low VCC operating
- 524,288 words x 8 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are LVTTL compatible
- 1024 refresh cycles every 16.4ms
- 10 rows x 9 columns, addressing scheme
- Early Write or $\overline{OE}$ controlled Write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Self refresh function
- Fast page Mode, Read–Modify–Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN} , V_{OUT}	–0.5 to +4.6	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	–0.5 to +4.6	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA
Storage Temperature	T_{STG}	–55 to +125	° C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package and Ordering Information

– 28–pin plastic (400mil) SOJ,
order as MB81V4800S–xxPJ

– 28–pin plastic (400mil) TSOP–II
with normal bend leads,
order as MB81V4800S–xxPFTN

– 28–pin plastic (400mil) TSOP–II
with reverse bend leads,
order as MB81V4800S–xxPFTR

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.