– PRELIMINARY –

March 1995
Edition 3.0

FUJITSU

PRODUCT PROFILE SHEET

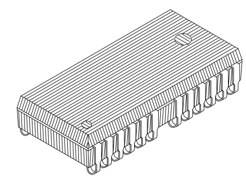
MB8117400A-50/-60/-70

CMOS 4M x 4 BIT FAST PAGE MODE DYNAMIC RAM

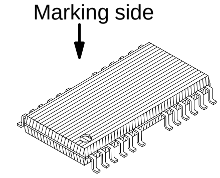
CMOS 4,194,304 x 4 BIT Fast Page Mode Dynamic RAM

The Fujitsu MB8117400A is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 4–bit increments. The MB8117400A features a ”fast page” mode of operation whereby high–speed random access of up to 1,024–bits of data within the same row can be selected. The MB8117400A DRAM is ideally suited for mainframe, buffers, hand–held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB8117400A is very small, the device can be used as a non–volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB8117400A is fabricated using silicon gate CMOS and Fujitsu’s advanced four–layer polysilicon and two–layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB8117400A are not critical and all inputs are TTL compatible.



Plastic SOJ Package
(LCC–26P–M09)



Plastic TSOP Packages
(FPT–26P–M05)
(Normal Bend)

PRODUCT LINE & FEATURES

Parameter	MB8117400A -50	MB8117400A -60	MB8117400A -70
$\overline{RAS}$ Access Time	50ns max.	60ns max.	70ns max.
Randam Cycle Time	90ns min.	110ns min.	130ns min.
Address Access Time	25ns min.	30ns max.	35ns max.
$\overline{CAS}$ Access Time	13ns max.	15ns max.	17ns max.
Fast Page Mode Cycle Time	35ns min.	40ns min.	45ns min.
Low Power Dissipation • Operating current	660mW max.	577.5mW max.	495mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)		

- 4,194,304 words x 4 bit organization
- Silicon gate, CMOS, Advanced Capacitor Cell
- All input and output are TTL compatible
- 2048 refresh cycles every 32ms
- Early Write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read–Modify–Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	–0.5 to + 7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	–0.5 to + 7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Operating Temperature	T_{OPE}	0 to 70	°C
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

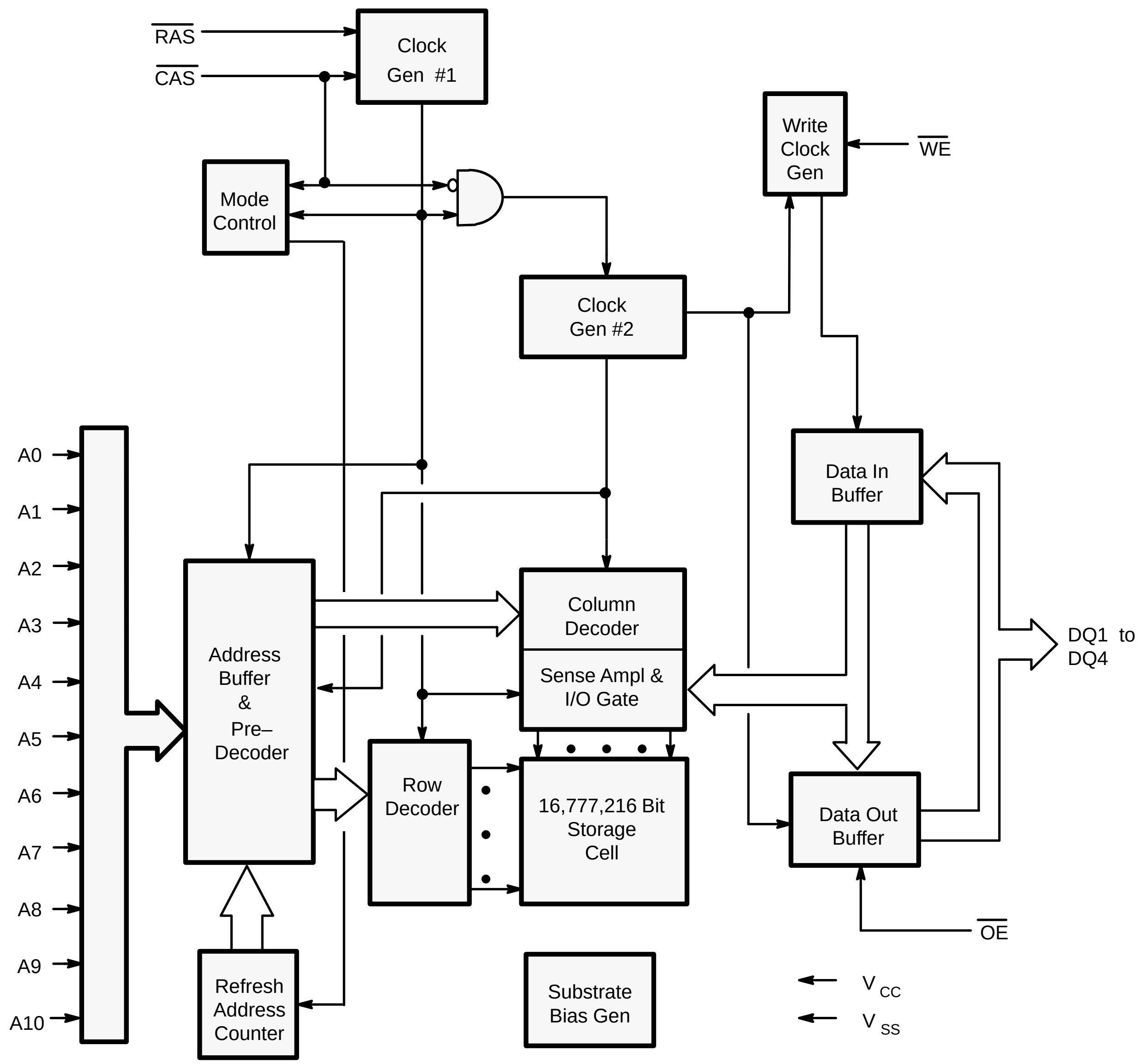
Package and Ordering Information

– 26–pin plastic (300mil) SOJ, order as MB8117400A–xxPJ

– 26–pin plastic (300mil) TSOP–II with normal bend leads, order as MB8117400A–xxPFTN

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB8117400A DYNAMIC RAM – BLOCK DIAGRAM

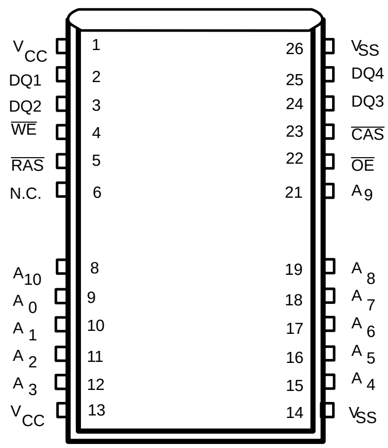


CAPACITANCE (T_A = 25°C, f = 1MHz)

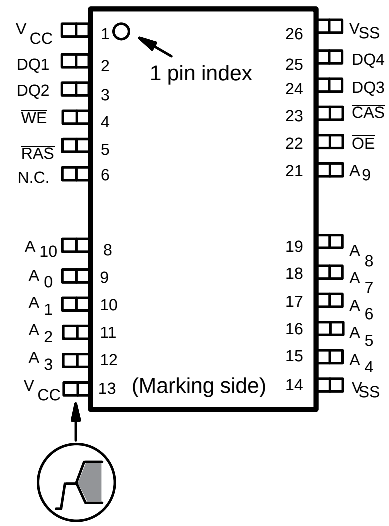
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	7	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

26-Pin SOJ:
(TOP VIEW)



26-Pin FPT:
(TOP VIEW)



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
A0 to A10	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.
N.C.	No Connection

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs/outputs *	1	VIL	–0.3	—	0.8	V	

*** :** Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty–two input bits are required to decode any four of 16,777,216 cell addresses in the memory matrix. Since only eleven address bits (A0 to A10) are available, the row and column inputs are separately strobed by $\overline{RAS}$ and $\overline{CAS}$ as shown in Figure 1. First, eleven row address bits are input on pins A0–through–A10 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

- **tRAC :** from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.
- **tCAC :** from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).
- **tAA :** from column address input when t_{RAD} is greater than t_{RAD} (max).
- **tOEA :** from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} .

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 1,024–bits can be accessed and, when multiple MB 8117400As are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read–modify–write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Value Min	Value Typ	Value Max	Unit
Output high voltage		V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V ≤ V_{IN} ≤ 5.5V; 4.5V ≤ V_{CC} ≤ 5.5V; V_{SS} = 0V; All other pins under test = 0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ V_{OUT} ≤ 5.5V; Data out disabled	–10	—	10	µA
Operating current (Average power supply Current) 2	MB8117400A-50	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	120	mA
	MB8117400A-60					105	
	MB8117400A-70					90	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2			1.0	
Refresh current #1 (Average power supply current) 2	MB8117400A-50	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	120	mA
	MB8117400A-60					105	
	MB8117400A-70					90	
Fast Page Mode current 2	MB8117400A-50	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	80	mA
	MB8117400A-60					70	
	MB8117400A-70					65	
Refresh current #2 (Average power supply current) 2	MB8117400A-50	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	120	mA
	MB8117400A-60					105	
	MB8117400A-70					90	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB8117400A-50		MB8117400A-60		MB8117400A-70		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	32	—	32	—	32	ms
2	Random Read/Write Cycle Time		t_{RC}	90	—	110	—	130	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	126	—	150	—	174	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	50	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	13	—	15	—	17	ns
6	Column Address Access Time	8,9	t_{AA}	—	25	—	30	—	35	ns
7	Output Hold Time		t_{OH}	3	—	3	—	3	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	13	—	15	—	17	ns
10	Transition Time		t_{T}	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	30	—	40	—	50	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	50	100000	60	100000	70	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	13	—	15	—	17	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	37	20	45	20	53	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	13	—	15	—	17	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	50	—	60	—	70	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	19	t_{CPN}	10	—	10	—	10	—	ns
19	Row Address Setup Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	10	—	ns
21	Column Address Setup Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	13	—	15	—	15	—	ns
23	Column Address Hold Time from $\overline{RAS}$		t_{AR}	35	—	35	—	35	—	ns
24	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	25	15	30	15	35	ns
25	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	25	—	30	—	35	—	ns
26	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	25	—	30	—	35	—	ns
27	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
30	Write Command Setup Time	15	t_{WCS}	0	—	0	—	0	—	ns
31	Write Command Hold Time		t_{WCH}	15	—	15	—	15	—	ns
32	Write Hold Time from $\overline{RAS}$		t_{WCR}	35	—	35	—	35	—	ns
33	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	ns
34	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	13	—	15	—	17	—	ns
35	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	13	—	15	—	17	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB8117400A-50		MB8117400A-60		MB8117400A-70		Unit
				Min	Max	Min	Max	Min	Max	
36	DIN Setup Time		t_{DS}	0	—	0	—	0	—	ns
37	DIN Hold Time		t_{DH}	15	—	15	—	15	—	ns
38	Data Hold Time from $\overline{RAS}$		t_{DHR}	35	—	35	—	35	—	ns
39	$\overline{RAS}$ to $\overline{WE}$ Delay Time	20	t_{RWD}	68	—	80	—	92	—	ns
40	$\overline{CAS}$ to $\overline{WE}$ Delay Time	20	t_{CWD}	31	—	35	—	39	—	ns
41	Column Address to $\overline{WE}$ Delay Time	20	t_{AWD}	43	—	50	—	57	—	ns
42	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	5	—	5	—	5	—	ns
43	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
44	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	12	—	ns
45	$\overline{WE}$ SetUp Time from $\overline{RAS}$		t_{WSR}	0	—	0	—	0	—	ns
46	$\overline{WE}$ Hold Time from $\overline{RAS}$		t_{WHR}	10	—	10	—	10	—	ns
47	Access Time from $\overline{OE}$	9	t_{OEA}	—	13	—	15	—	17	ns
48	Output Buffer Turn Off Delay form $\overline{OE}$	10	t_{OEZ}	—	13	—	15	—	17	ns
49	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	5	—	5	—	7	—	ns
50	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	5	—	5	—	5	—	ns
51	$\overline{OE}$ to Data in Delay Time		t_{OED}	13	—	15	—	17	—	ns
52	CAS to Data in Delay Time		t_{CDD}	—	13	—	15	—	17	ns
53	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	ns
54	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	ns
55	Fast Page Mode $\overline{RAS}$ Pulse width		t_{RASP}	—	100000	—	100000	—	100000	ns
60	Fast Page Mode Read/Write Cycle Time		t_{PC}	35	—	40	—	45	—	ns
61	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	71	—	80	—	89	—	ns
62	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	30	—	35	—	40	ns
63	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	ns
64	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	30	—	35	—	40	—	ns
65	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time		t_{CPWD}	48	—	55	—	62	—	ns

Notes:

1. Referenced to VSS.
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open. I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} , $\overline{CAS}$ = V_{IH} and V_{IL} > –0.3V.
   I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}. I_{CC2} is specified during $\overline{RAS}$=V_{IH} and V_{IL}>–0.3V.
3. An initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC} .
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that t_{WCS} < t_{WCS} (min).
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
19. Assumes that $\overline{CAS}$ –before–$\overline{RAS}$ refresh.
20. t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If t_{WCS} > t_{WCS} (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If t_{CWD} > t_{CWD} (min), t_{RWD} > t_{RWD} (min) , and t_{AWD} > t_{AWD} (min), the cycle is a read modify–write cycle and data from the selected cell will appear at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin , and write operation can be executed by satisfying t_{RWL} , t_{CWL} , and t_{RAL} specifications.

Fig. 2 – t_{RAC} vs. t_{RCD}

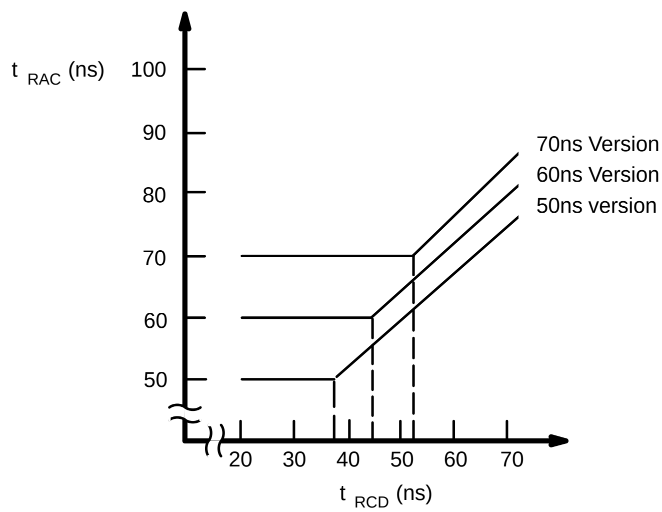
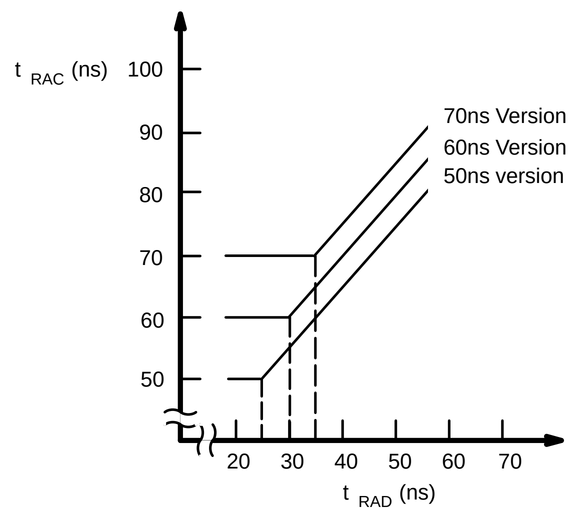


Fig. 3 – t_{RAC} vs. t_{RAD}

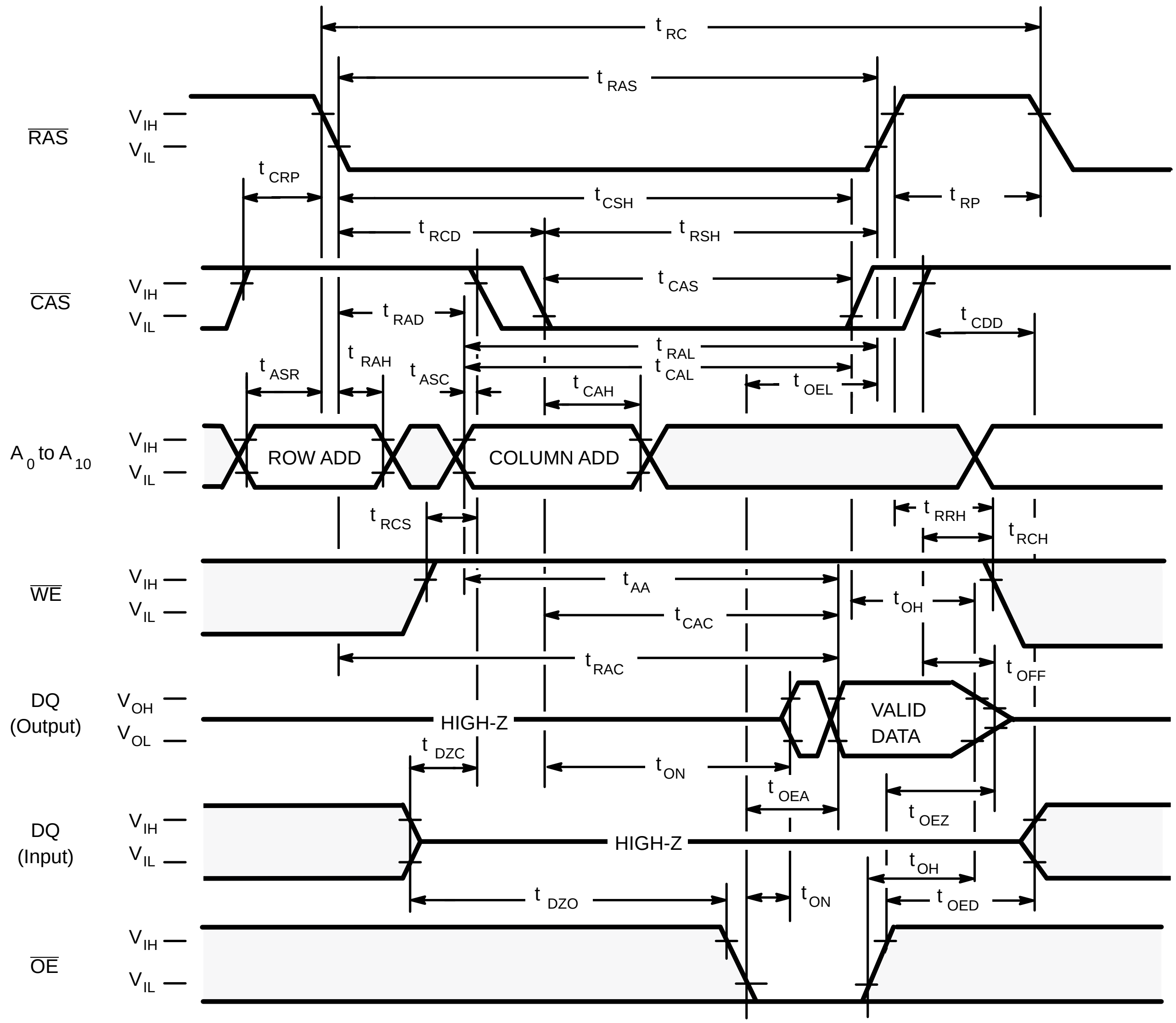


FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High–Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High–Z	Yes *	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
$\overline{\text{RAS}}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High–Z	Yes	
$\overline{\text{CAS}}$–before–$\overline{\text{RAS}}$ Refresh Cycle	L	L	H	X	—	—	—	High–Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H→L	L	H→X	L	—	—	—	Valid	Yes	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

Fig. 4 – READ CYCLE



"H" or "L"

DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ address strobes and with $\overline{\text{WE}}$ set to a High level and $\overline{\text{OE}}$ set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{\text{RAS}}$(tRAC), $\overline{\text{CAS}}$(tCAC), $\overline{\text{OE}}$ (tOEA) or column addresses (tAA) under the following conditions:

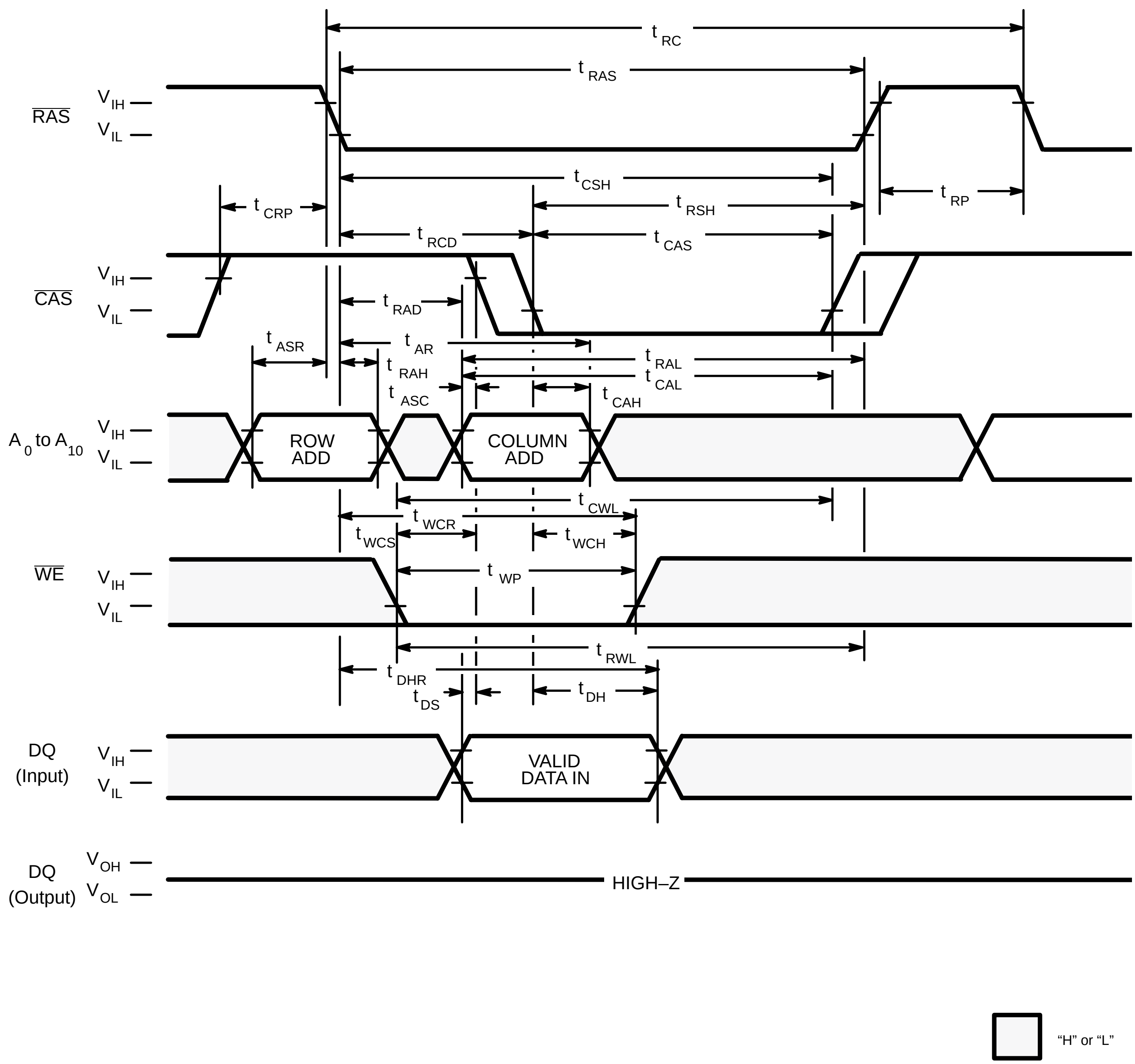
If tRCD > tRCD (max), access time = tCAC.

If tRAD > tRAD (max), access time = tAA.

If $\overline{\text{OE}}$ is brought Low after tRAC, tCAC, or tAA (whichever occurs later), access time = tOEA.

However, if either $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ goes High, the output returns to a high–impedance state after tOH is satisfied.

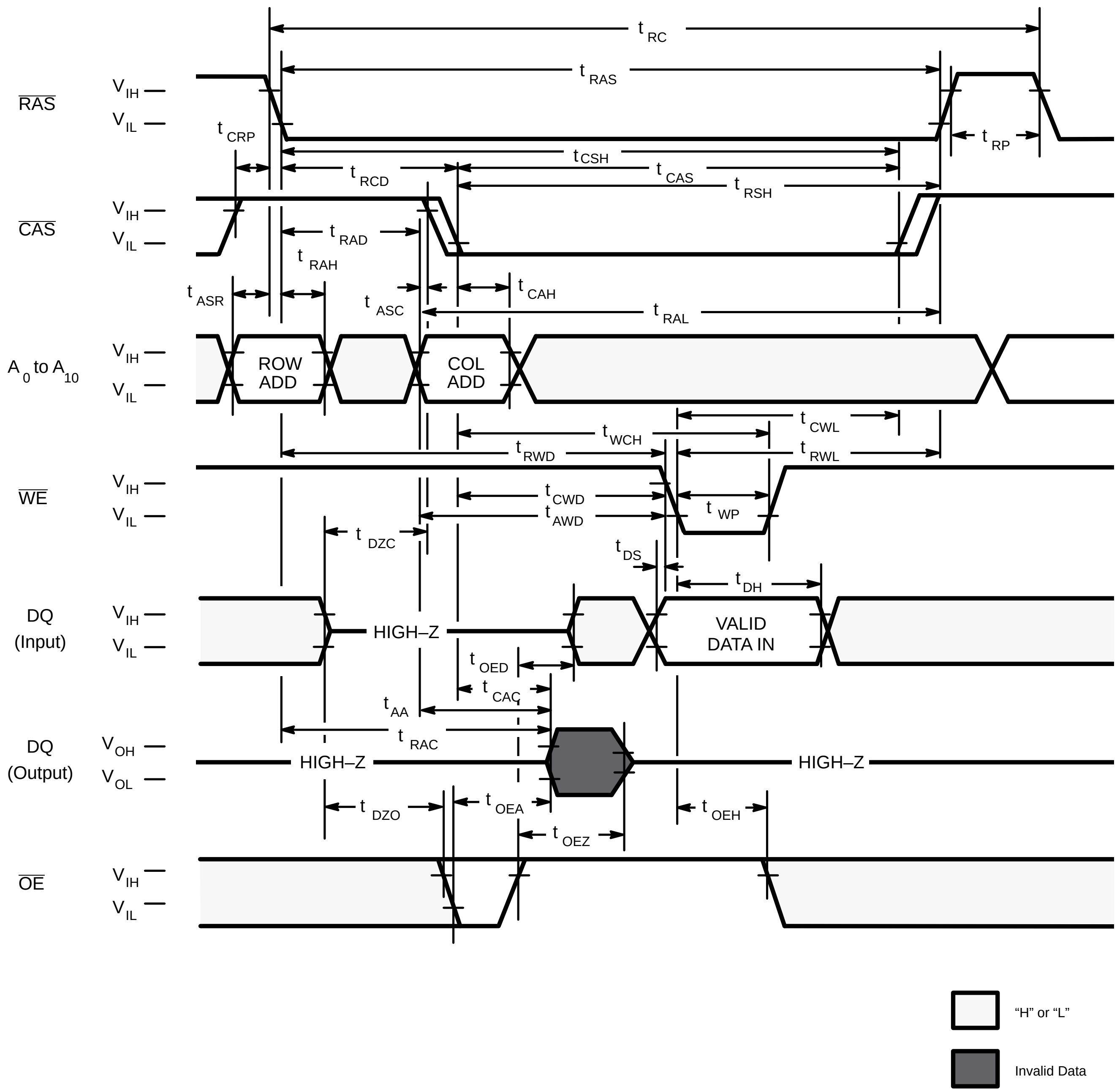
Fig.5 – EARLY WRITE CYCLE ($\overline{OE}$=”H”or”L”)



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a “H” or “L” signal. A write cycle can be implemented in either of three ways – early write, $\overline{OE}$ write (delayed write), or read–modify–write. During all write cycles, timing parameters tRWL, tCWL and tRAL must be satisfied. In the early write cycle shown above tWCS satisfied, data on the DQ pin is latched with the falling edge of $\overline{CAS}$ and written into memory.

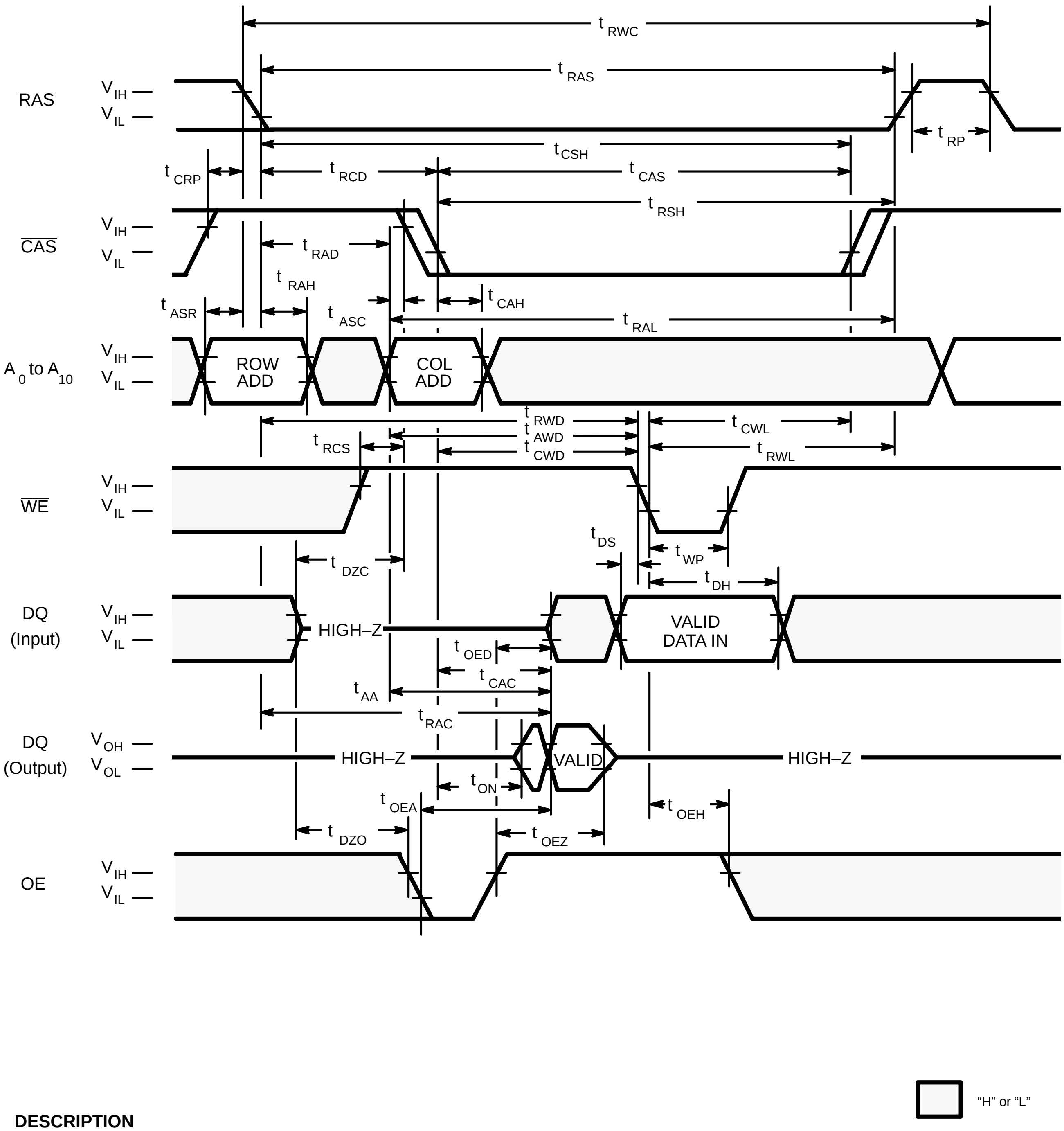
Fig. 6 – $\overline{OE}$ (DELAYED WRITE CYCLE)



DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, tWCS is not satisfied ; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

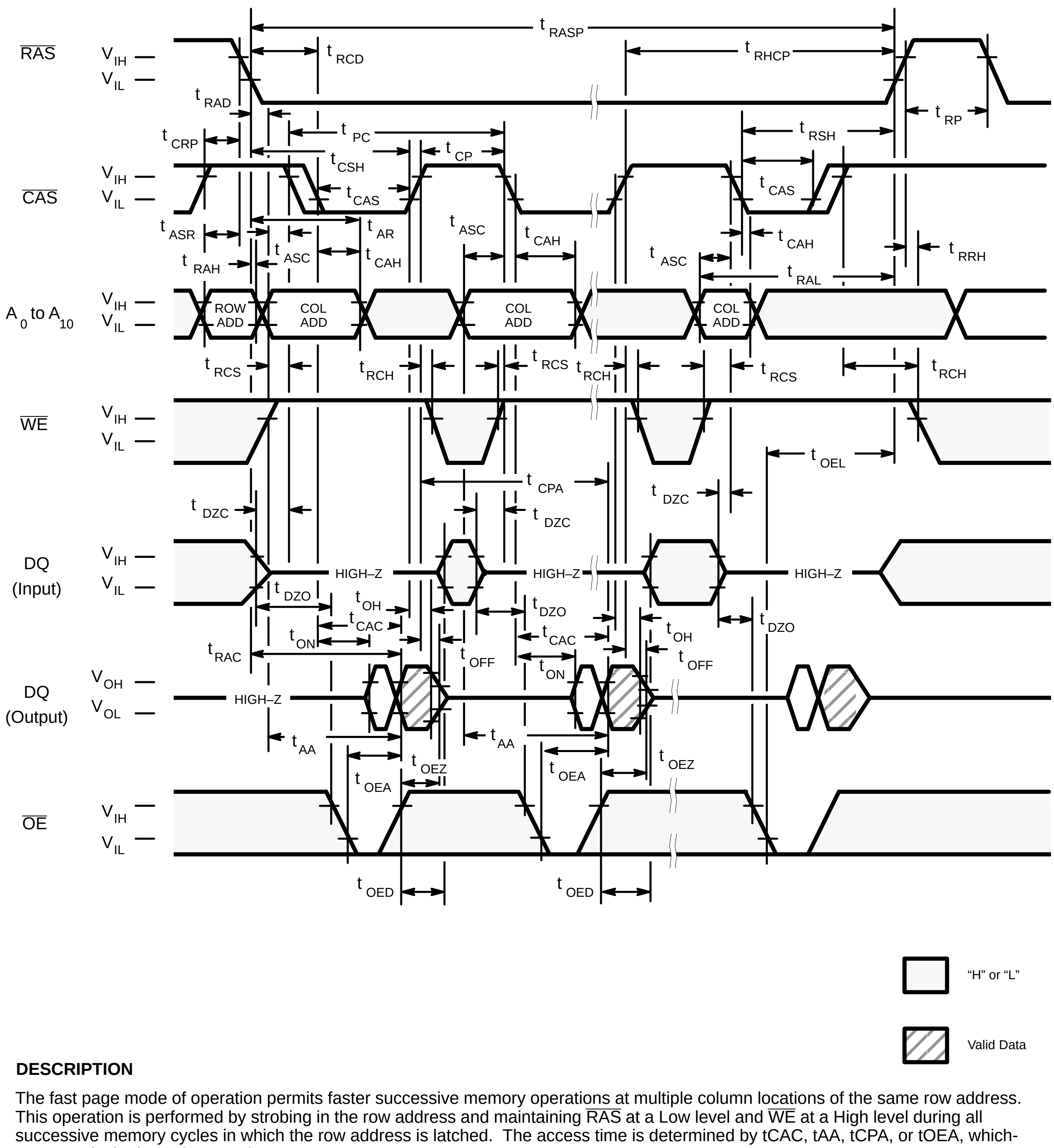
Fig. 7 — READ–MODIFY–WRITE–CYCLE



DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

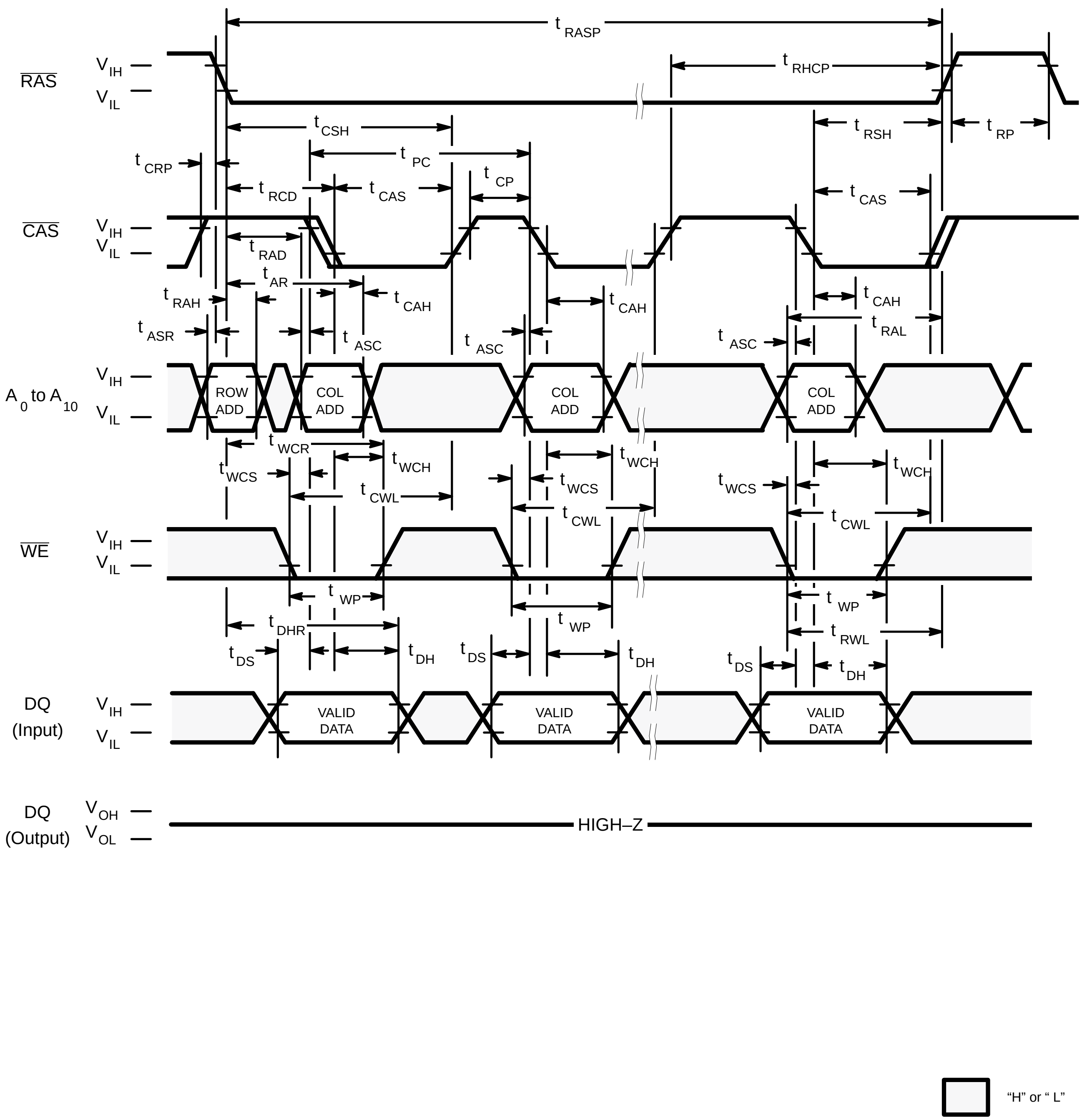
Fig. 8 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occurring.

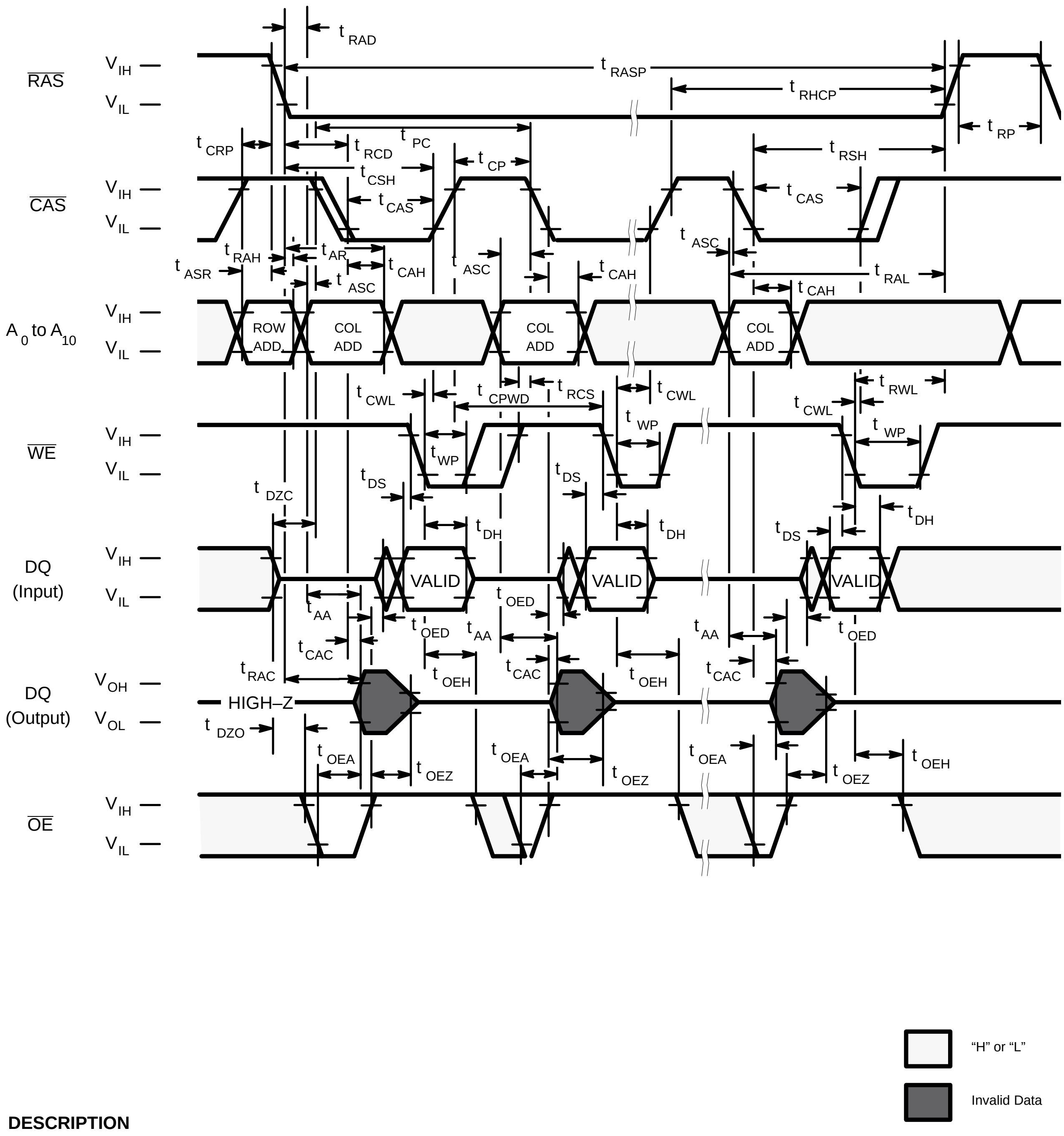
Fig. 9 – FAST PAGE MODE WRITE CYCLE ($\overline{OE}$=”H”or”L”)



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, tCWL must be satisfied.

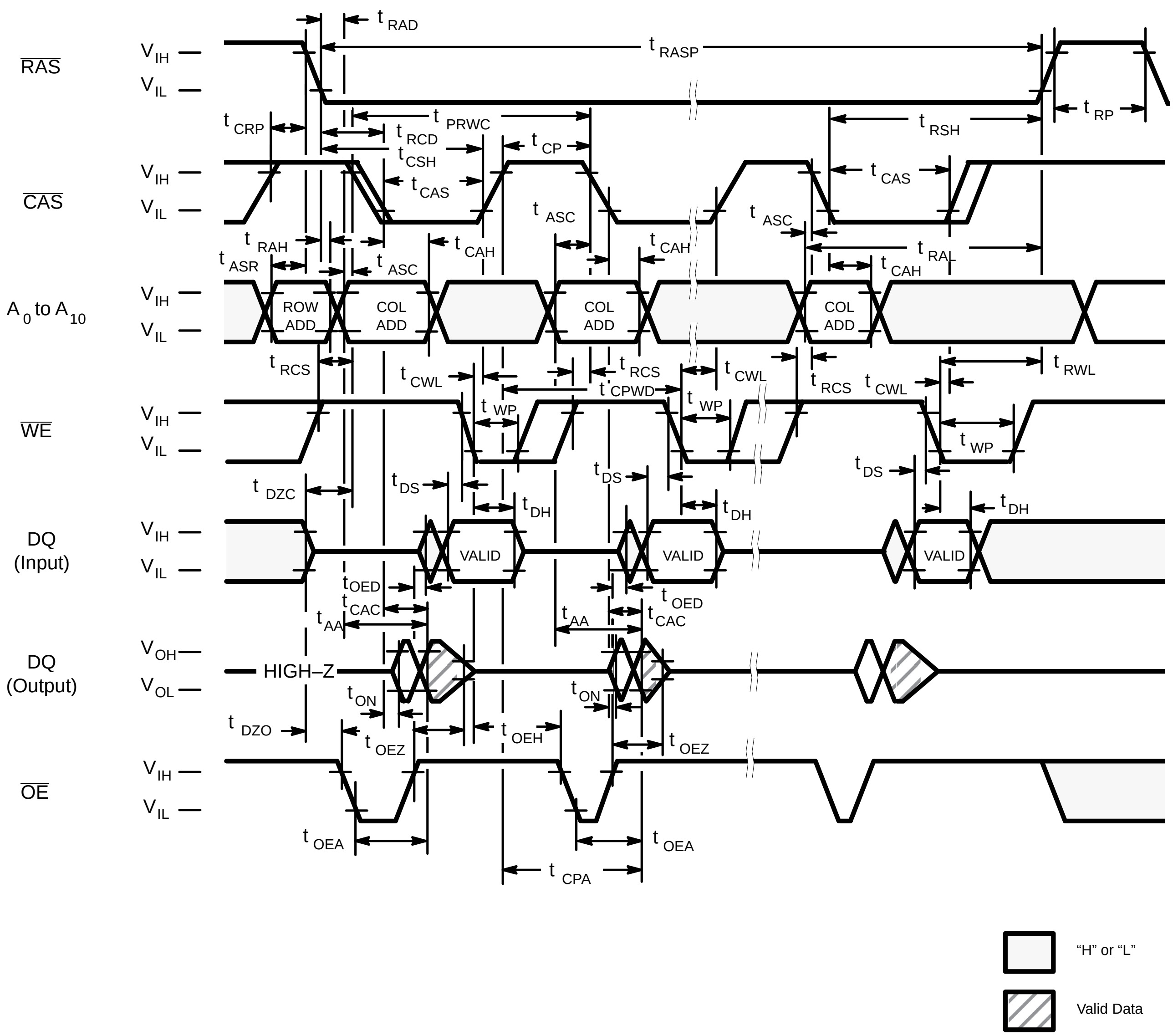
Fig. 10 – FAST PAGE MODE $\overline{OE}$ WRITE CYCLE



DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

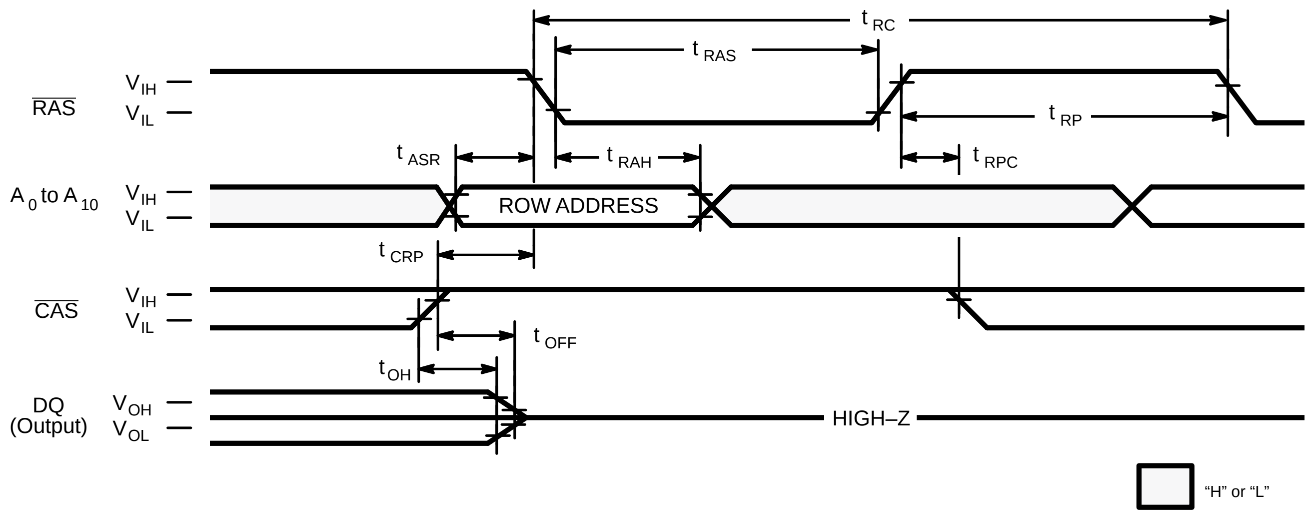
Fig. 11 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During the fast page mode of operation, the read–modify–write cycle can be executed by switching WE from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 12 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$=$\overline{OE}$=”H”or”L”)

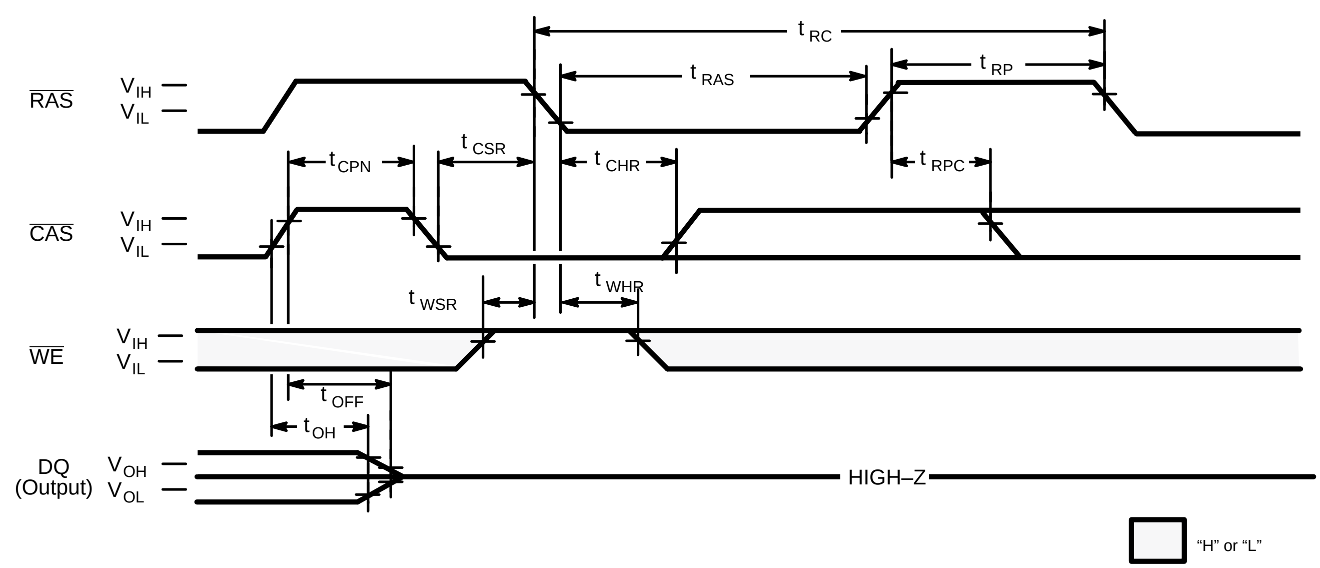


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 2048 row addresses every 32–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DQ pins are kept in a high-impedance state.

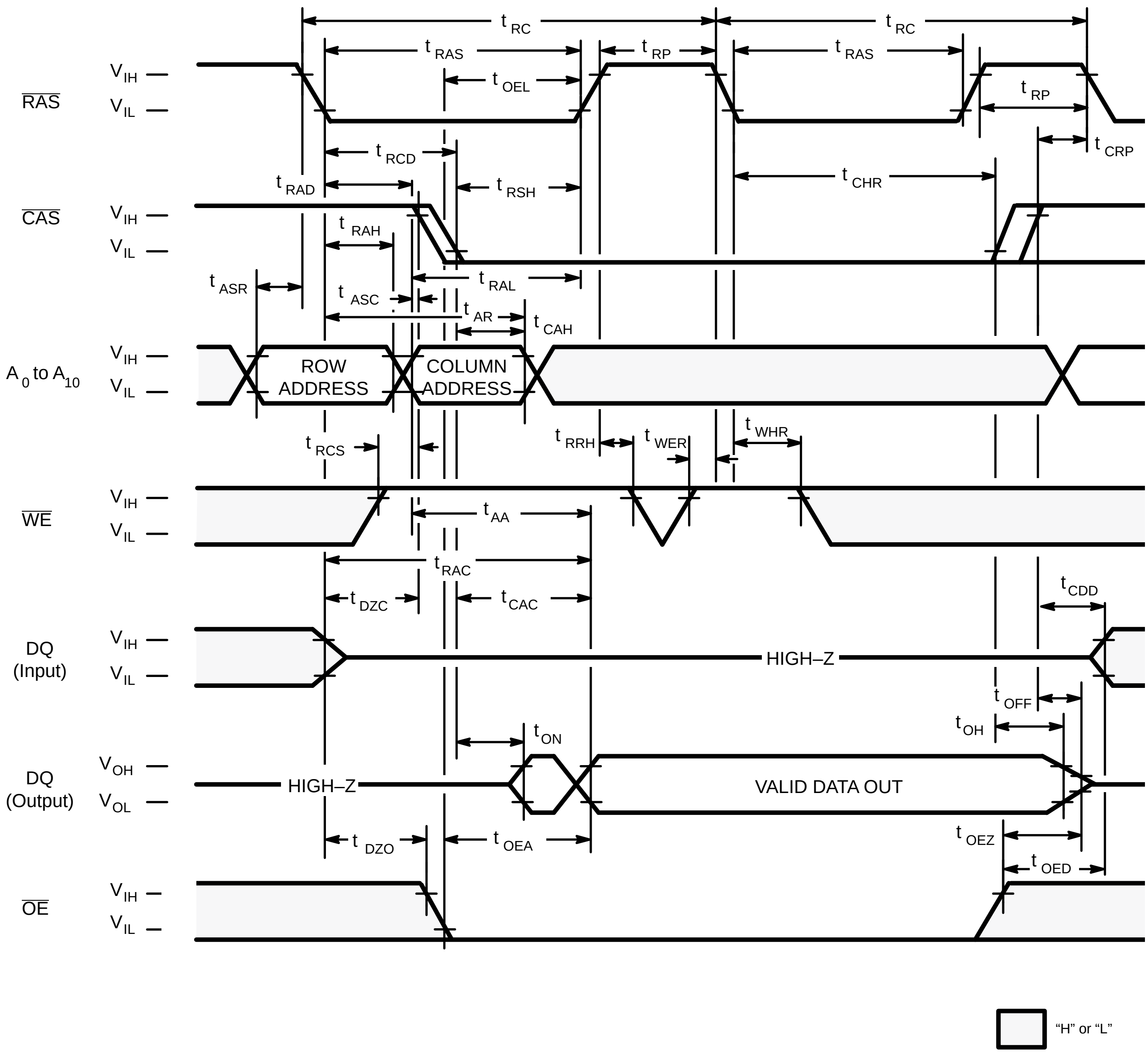
Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (ADRESS=$\overline{OE}$=”H”or”L”)



DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

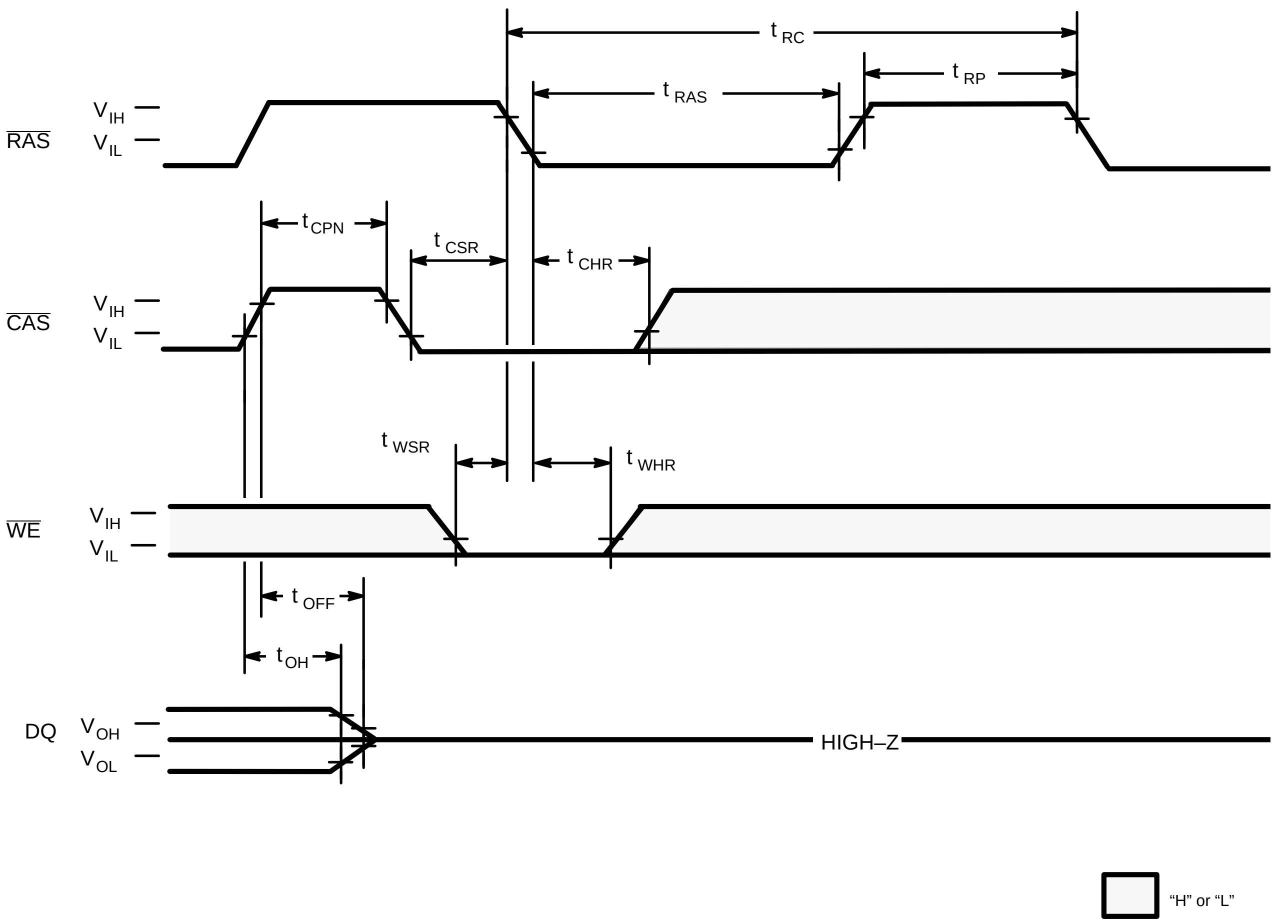
Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig.15 – TEST MODE SET CYCLE (A0 to A10, $\overline{OE}$ = ”H” or ”L”)



DESCRIPTION

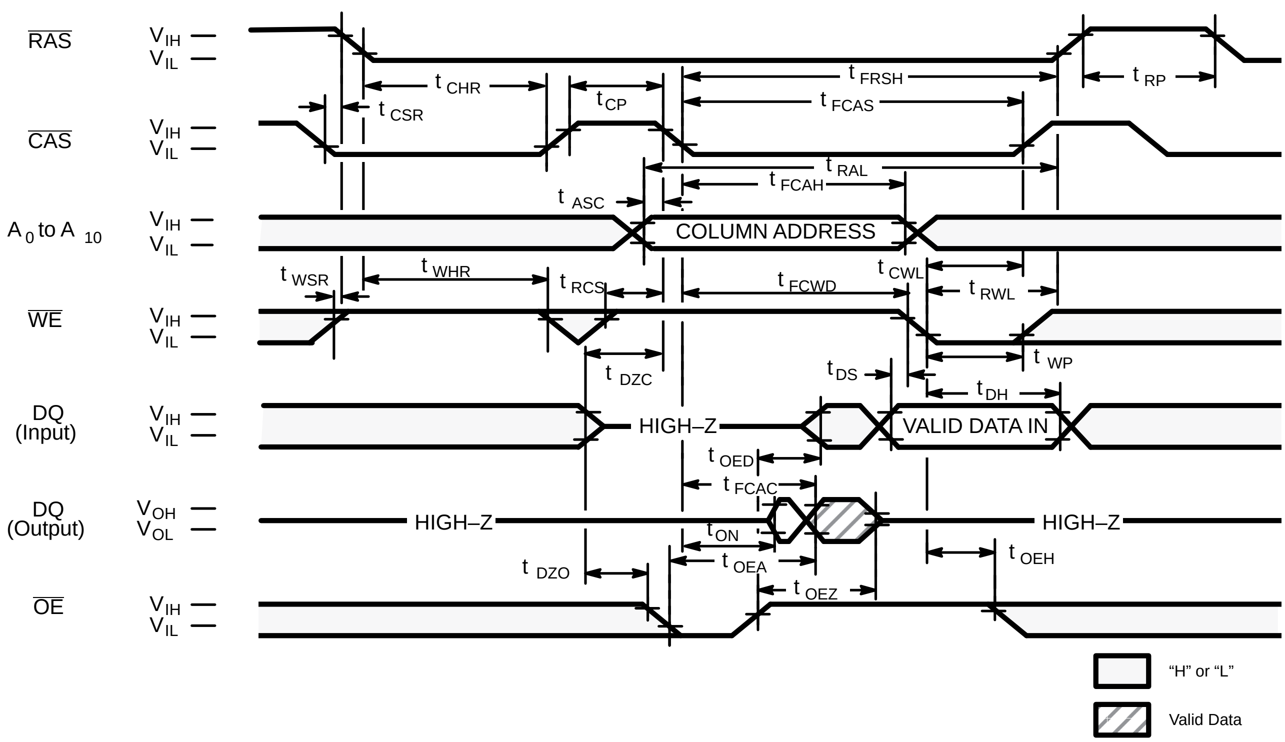
Test Mode ;

The purpose of this test mode is to reduce device test time to one sixteenth of that required to test the device conventionally.
The test mode function is entered by performing a $\overline{WE}$ and $\overline{CAS}$–before–$\overline{RAS}$ (WCBR) refresh for the entry cycle.
In the test mode, read and write operations are executed in units of sixteenth bits which are selected by the address combination of CA0 and CA1. In the write mode, data is written into sixteenth cells simultaneously. But the data must be input from DQ1 only. In the read mode, the data of sixteenth cells at the selected addresses are read out from DQ and checked in the following manner.

When the sixteenth bits are all ”L” or all ”H”, an ”H” level is output.
When the sixteenth bits show a combination of ”L” and ”H”, an ”L” level is output.

The test mode function is exited by performing a $\overline{RAS}$–only refresh or a $\overline{CAS}$–before–$\overline{RAS}$ refresh for the exit cycle.
In test mode operation, the following parameters are delayed approximately 10ns from the specified value in the data sheet.
tRC, tRWC, tRAC, tCAC, tAA, tRAS, tRSH, tCAS, tCSH, tRAL, tCAL, tRWD, tCWD, tAWD

Fig. 16 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle $\overline{CAS}$ makes a transition from High to Low while RAS is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A10 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A10 are defined by latching levels on A0–A10 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{RAS}$ only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 2048 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test (read–modify–write cycles). Repeat this procedure 2048 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 2048 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

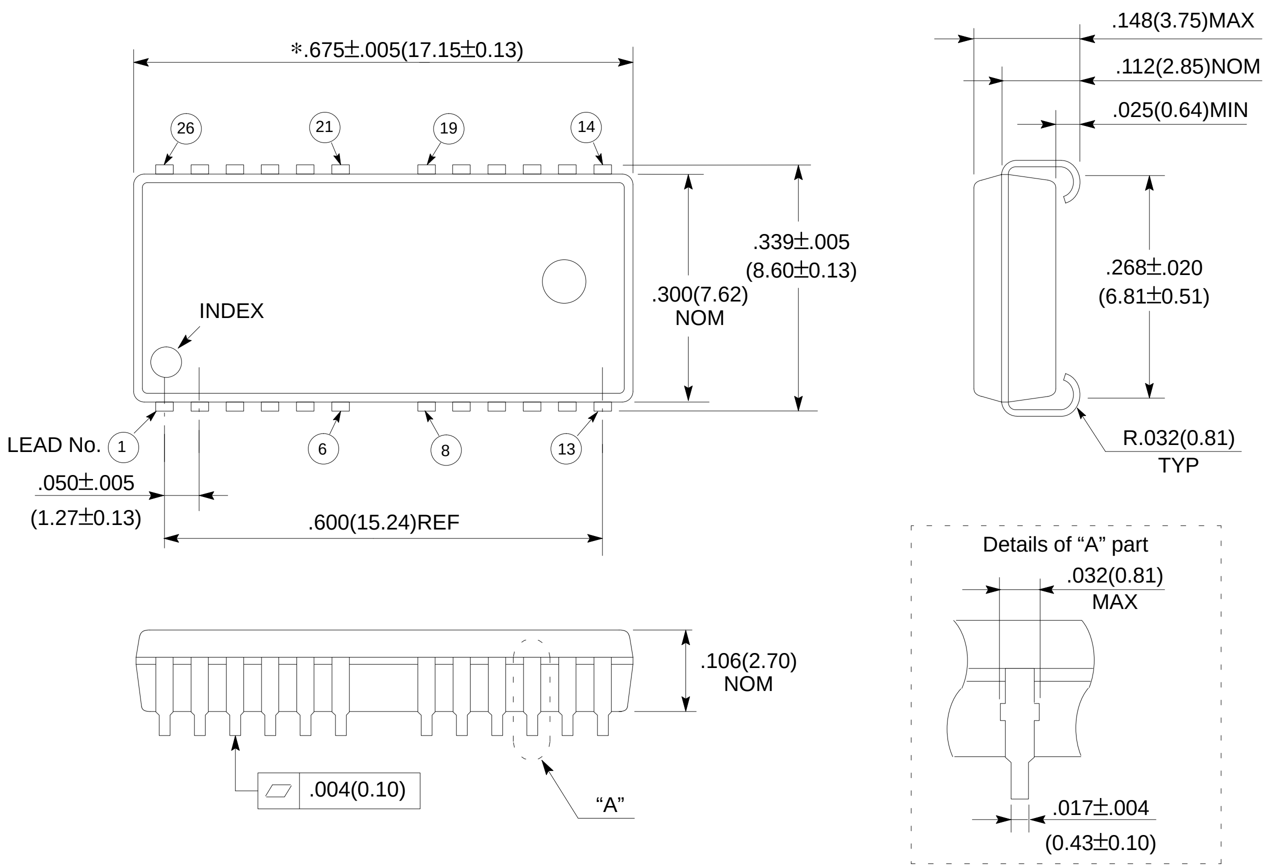
No.	Parameter	Symbol	MB8117400A-50		MB8117400A-60		MB8117400A-70		Unit
			Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	45	—	50	—	55	ns
91	Column Address Hold Time	t_{FCAH}	35	—	35	—	35	—	ns
92	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{FCWD}	63	—	70	—	77	—	ns
93	$\overline{CAS}$ Pulse width	t_{FCAS}	45	—	50	—	55	—	ns
94	$\overline{RAS}$ Hold Time	t_{FRSH}	45	—	50	—	55	—	ns

Note. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix : –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M09)



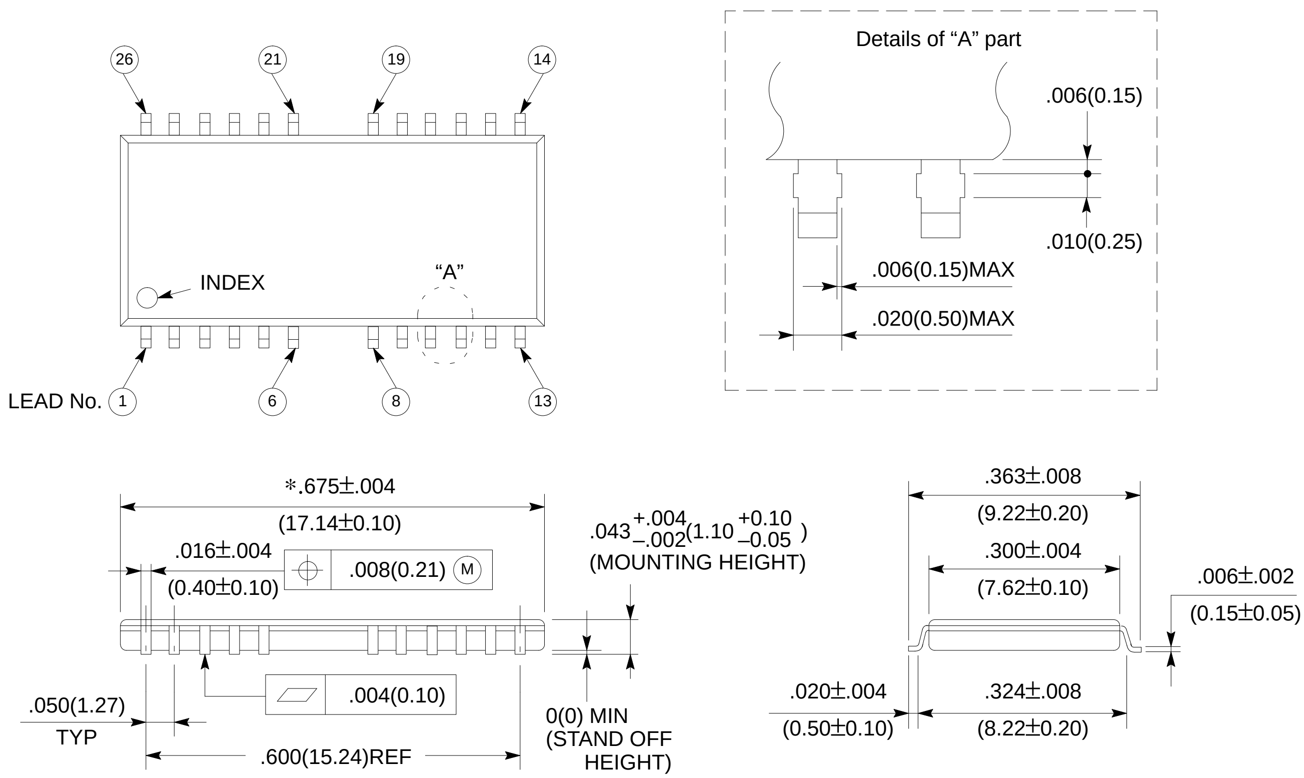
∗: This dimension excludes resin protrusion. (Each side: .006(0.15)MAX)

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: – PFTN)

26-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-26P-M05)



*: This dimension excludes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in inches (millimeters)