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FUJITSU

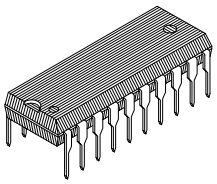
DATA SHEET

MB40730

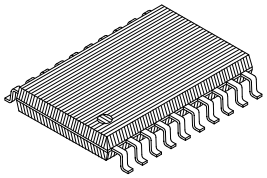
1-Channel, 10-Bit ASSP Image Processing D/A Converter (60 MSPS)

The MB40730 is a low-power consumption, high-speed 10-bit D/A converter. It is characterized by ECL (10KH) compatible digital inputs, an analog output voltage ranging from –2 V to 0 V, and a maximum conversion rate of 60 MHz. It provides reference voltage from a potential divider and band-gap reference, or it can use external reference voltage. The MB40730 D/A converter is suitable for use in high-resolution TVs or VTRs.

- Resolution: 10 bits
- Conversion characteristics:
  - Maximum conversion rate: 60 MHz minimum
  - Linearity error: ±0.1% maximum
  - Differential linearity error: ±0.1% maximum
- Input and output:
  - Digital input voltage: 10KH ECL levels
  - Analog output voltage: 2 Vp-p (–2 V to 0 V)
- Reference voltage:
  - V_{ROUT1}: Potential divider circuit (V_{EEA} x 2/5.2)
  - V_{ROUT2}: Band-gap reference circuit (–2 V)
- Other characteristics:
  - Supply voltage: –5.2 V single power supply
  - Power dissipation: 180 mW (typical value at analog output voltage 2 Vp-p)
    140 mW (typical value at analog output voltage 1 Vp-p)
- Package and ordering information:
  – 20-pin plastic DIP, order as MB40730P
  – 20-pin plastic SOP, order as MB40730PF



Plastic DIP
(DIP-20P-M01)



Plastic SOP
(FPT-20P-M01)

ABSOLUTE MAXIMUM RATINGS ($V_{CCA} – V_{CCD}$ = 0 V, T_A = +25°C

Parameter	Symbol	Rating	Unit
Analog Power Supply Voltage	V_{CCA}	–7.0 to 0	V
Digital Power Supply Voltage	V_{CCD}	–7.0 to 0	V
Power Supply Voltage Difference	$V_{EED}–V_{EEA}$	1.0	V
Digital Signal Input Voltage	V_{ID}	0 to V_{EE}	V
Storage Temperature	T_{STG}	–55 to +125	°C

— Note —

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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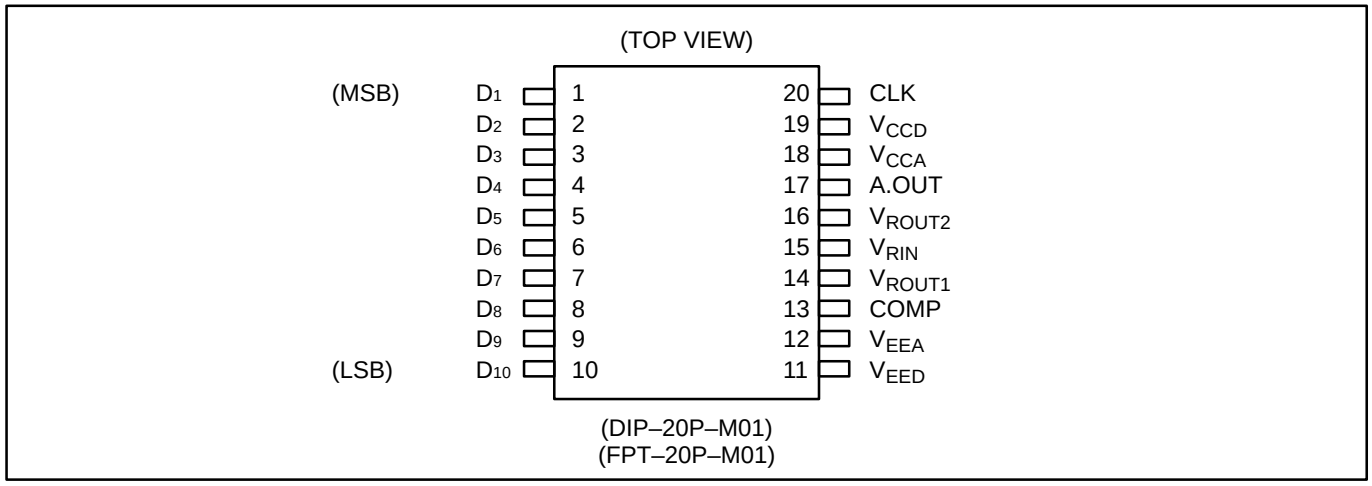
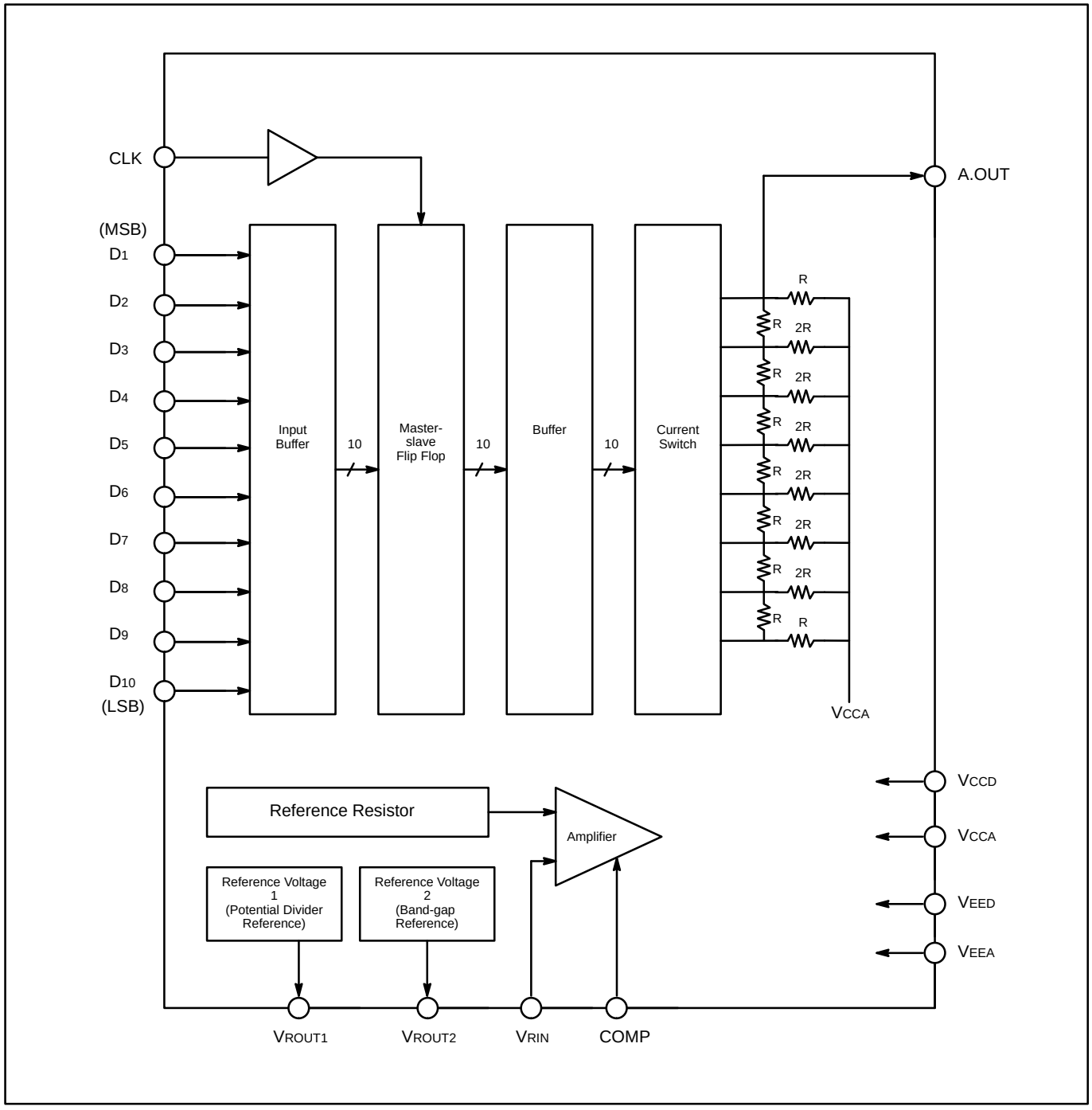
PIN ASSIGNMENT



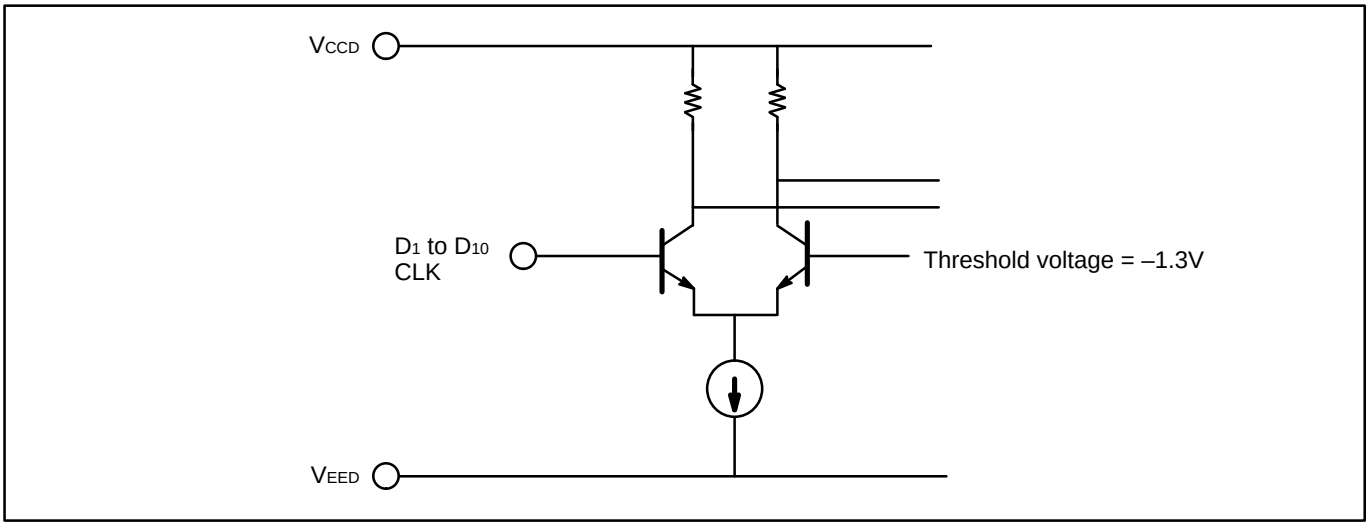
PIN FUNCTIONS

Pin No.	Symbol	I/O	Description
1 to 10	D_1 to D_{10}	I	Data signal input pin (D_1: MSB, D_{10}: LSB)
20	CLK	I	Clock signal input pin
19	V_{CCD}	–	Digital ground pin (0V)
18	V_{CCA}	–	Analog ground pin (0V)
11	V_{EED}	–	Digital power pin (–5.2V)
12	V_{EEA}	–	Analog ground pin (–5.2V)
15	V_{RIN}	I	Reference voltage input pin Analog output dynamic range setup pin (Connect to pin 14 or 16 to use the built-in reference voltage. When using an external reference voltage, the voltage on this pin must be from –2.20V to –0.70V.)
14	V_{ROUT1}	O	Reference voltage output pin 1 (The output voltage of the potential divider reference is fixed at $V_{EEA} \times 2/5.2$. When this pin is connected to pin 15, the analog output voltage ranges from $V_{EEA} \times 2/5.2$ to 0V.)
16	V_{ROUT2}	O	Reference voltage output pin 2 (The output voltage of the band-gap reference is fixed at –2.0V. When the pin is connected to pin 15, the analog output voltage ranges from –2V to 0V.)
13	COMP	–	Phase compensation capacitor pin (Insert a capacitor of 0.1 µF or greater between V_{EEA} and COMP for phase compensation.)
17	A.OUT	O	Analog signal output pin

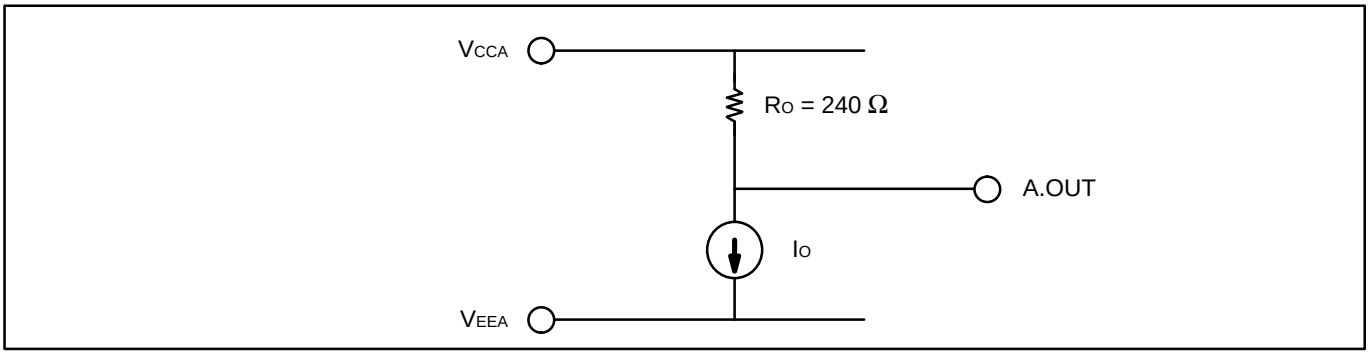
BLOCK DIAGRAM



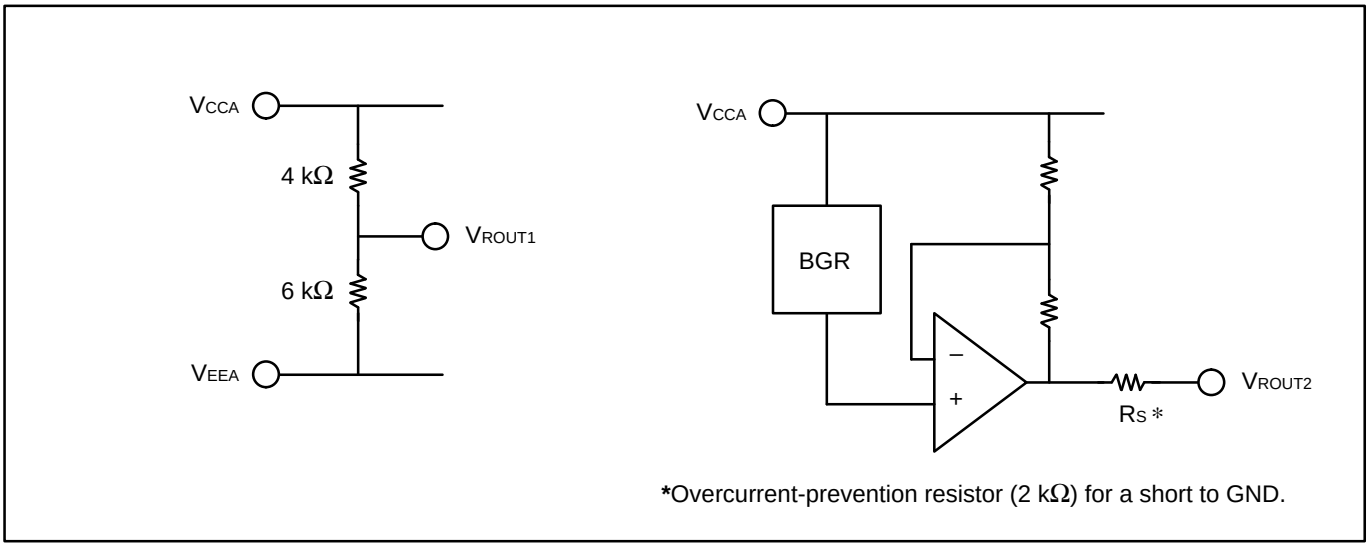
DIGITAL INPUT EQUIVALENT CIRCUIT



ANALOG OUTPUT EQUIVALENT CIRCUIT

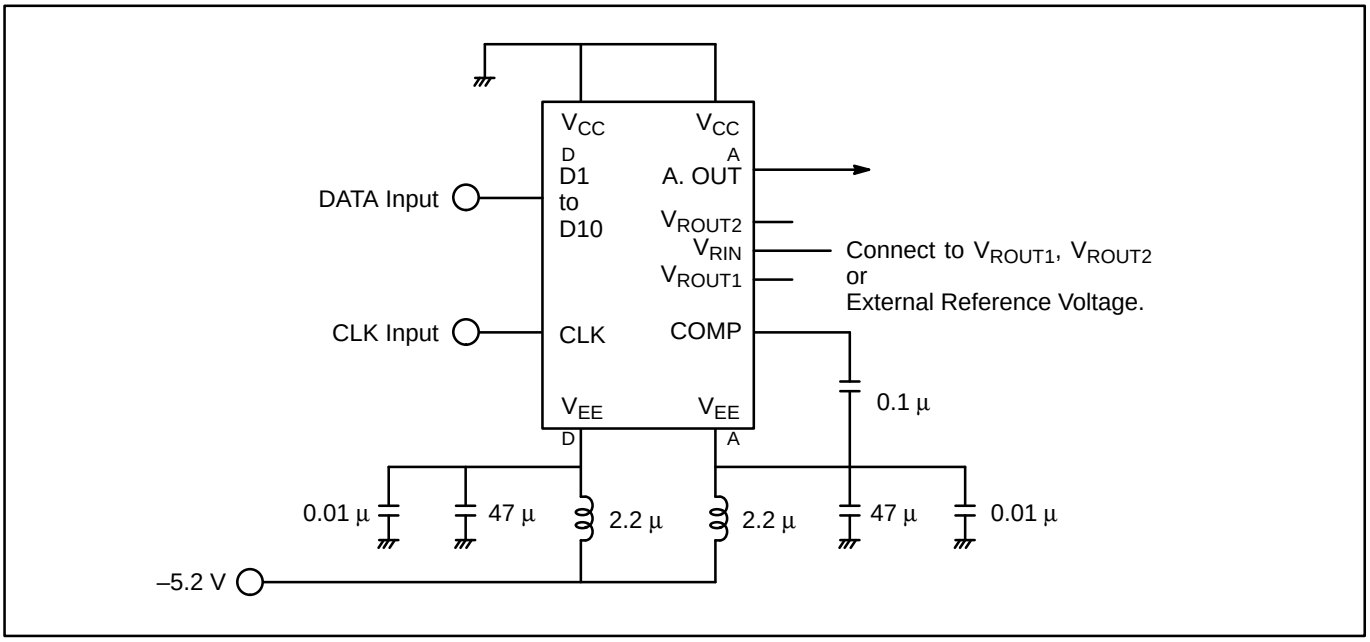


REFERENCE VOLTAGE OUTPUT EQUIVALENT CIRCUIT



*Overcurrent-prevention resistor (2 kΩ) for a short to GND.

TYPICAL CONNECTION EXAMPLE



RECOMMENDED OPERATING CONDITIONS

°C to +75 °C

Parameter		Symbol		Standard Values Min.	Typ.	Max.	Unit
Power supply voltage	Analog power supply voltage	V_{EEA}		–5.46	–5.20	–4.94	V
	Digital power supply voltage	V_{EED}		–5.46	–5.20	–4.94	V
	Power supply voltage difference	V_{EEA}–V_{EED}		–0.2	–	0.2	V
Analog reference voltage		V_{RIN}		–0.220	–2.00	–0.70	V
Digital input high voltage		V_{IHD}	–20°C	–	–	–0.88	V
			–25°C	–1.13	–	–0.81	V
			–75°C	–	–	–0.735	V
Digital input low voltage		V_{ILD}	–20°C	–1.95	–	–	V
			–25°C	–1.95	–	–1.48	V
			–75°C	–1.95	–	–	V
Clock frequency		t_{CLK}		–	–	60	MHz
Setup time		t_{su}		8	–	60	ns
Hold time		t_h		2	–	–	ns
Clock minimum pulse width high		t_{WH}		6.5	–	–	ns
Clock minimum pulse width low		t_{WL}		6.5	–	–	ns
Phase compensation capacitor		C_{COMP}		0.1	–	–	µF
Operating temperature		T_{op}		20	–	75	°C

DC CHARACTERISTICS

(V_{EEA}=V_{EED}=–5.46 to –4.94V, T_A=–20°C to +75°C)

Parameter		Symbol	Conditions	Standard Values			Unit
				Min.	Typ.	Max.	
Resolution		–	–	–	–	10	bit
Linearity error		LE	DC accuracy	–	–	±0.1	%
Differential linearity error		DLE		–	–	±0.1	%
Digital input current high		I_{IHD}	–	–	–	5	µA
Digital input current low		I_{ILD}	–	–0.1	–	–	µA
Reference input current		I_{RIN}	V_{RIN} = –2.000V	–	–	10	µA
Potential divider reference	Reference voltage	V_{ROUT1}	V_{EEA} = –5.20V V_{EED} = –5.20V	–2.100	–2.100	–1.900	V
Band-gap reference	Reference voltage	V_{ROUT2}	–	–2.100	–2.100	–1.900	V
	Temperature coefficient	–	–	–	100	–	ppm/°C
Full-scale output voltage		V_{OFS}	–	–20	0	–	mV
Zero-scale output voltage		V_{OZS}	V_{EEA} = –5.20V V_{EED} = –5.20V V_{RIN} = –2.000V	–2.068	–1.998	–1.928	V
Output resistance		R_O	T_A = +25°C	192	240	288	Ω
Power dissipation		I_{EE}	V_{EEA} = –5.46V V_{EED} = –5.46V V_{RIN} = V_{ROUT1}	–59	–34*	–	mA

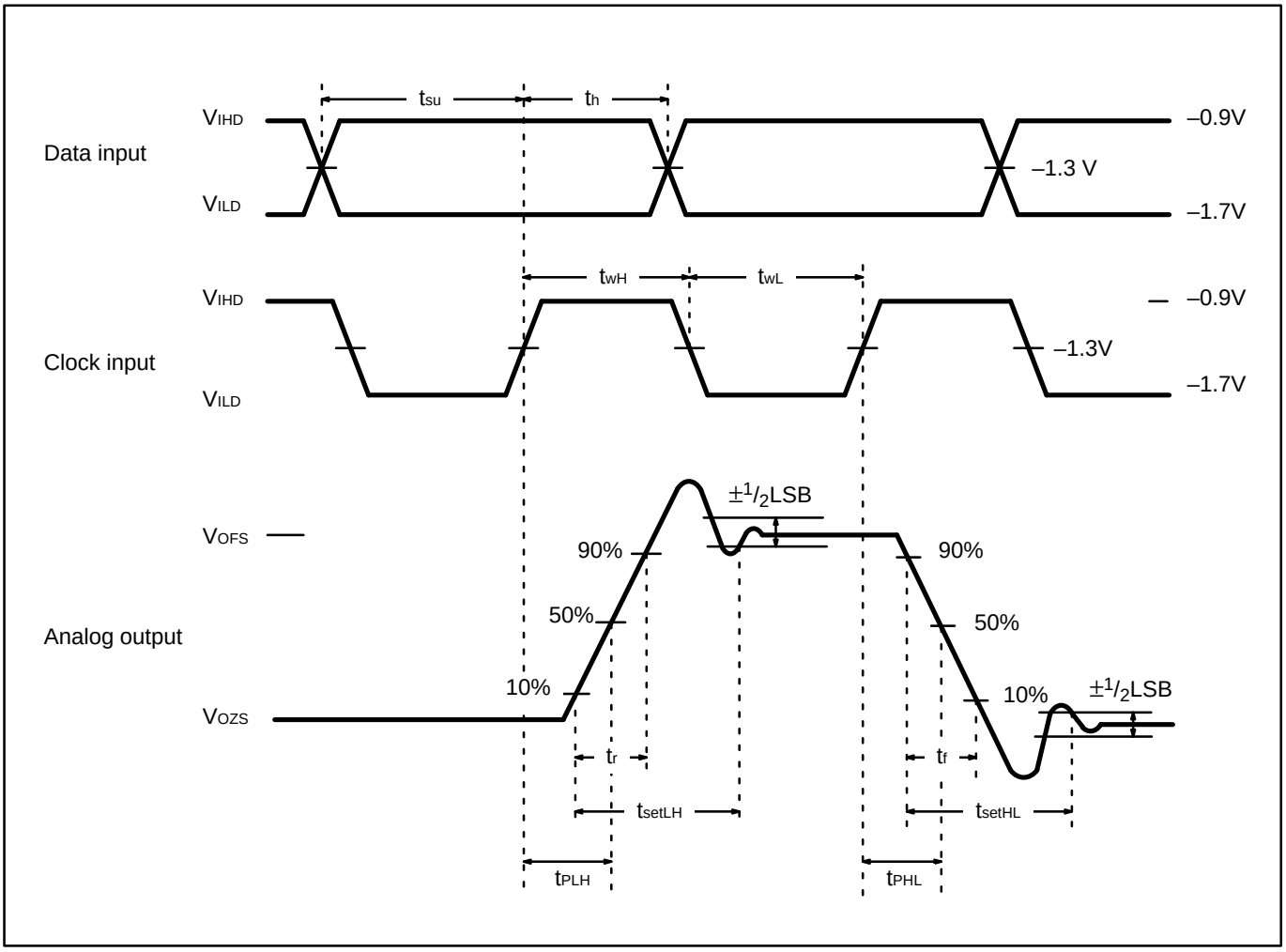
*V_{EEA} = V_{EED} = –5.20V

AC CHARACTERISTICS

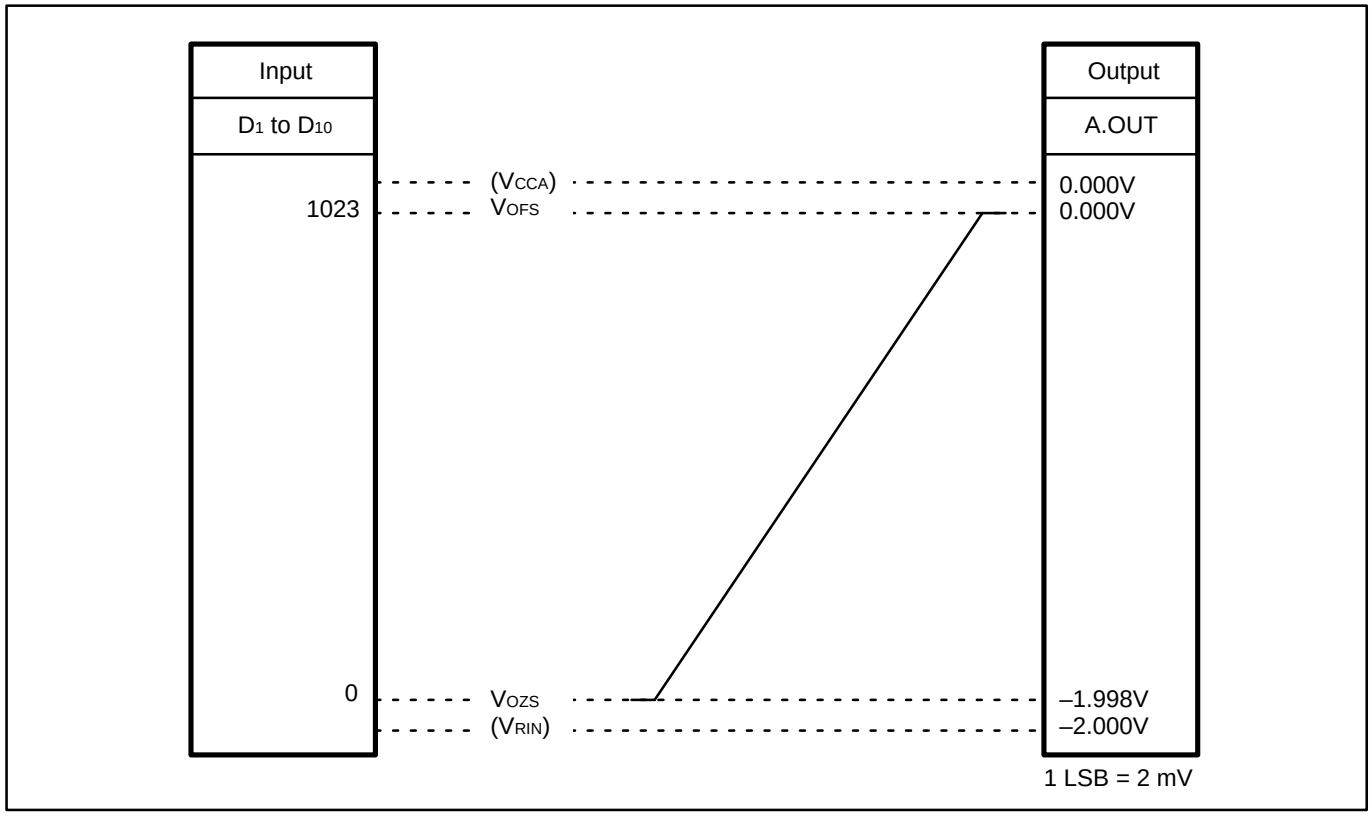
V_{EEA}= V_{EED}=–5.46 to –4.94V, T_A=–20°C to +75°C)

Parameter	Symbol	Conditions	Standard Values			Unit
Maximum conversion rate	F_s	CL = 15 pF	60	–	–	MSPS
Output propagation delay time	t_{pd}	A.OUT pin terminating resistance = 240 Ω	–	7	–	ns
Output rise time	t_r		–	5	–	ns
Output fall time	t_f		–	5	–	ns
Settling time	t_{set}		–	17.5	–	ns

TIMING CHART



DAC OUTPUT VOLTAGE CHARACTERISTICS



DAC OUTPUT VOLTAGE FORMULA UNDER IDEAL CONDITIONS

$$A.OUT = V_{CCA} - \frac{1023 - N}{1024} \times (V_{CCA} - V_{RIN})$$

(N : Digital input code from 0 to 1023)

$$V_{OFS} = V_{CCA}$$

$$V_{OZS} = V_{CCA} - \frac{1023}{1024} \times (V_{CCA} - V_{RIN})$$

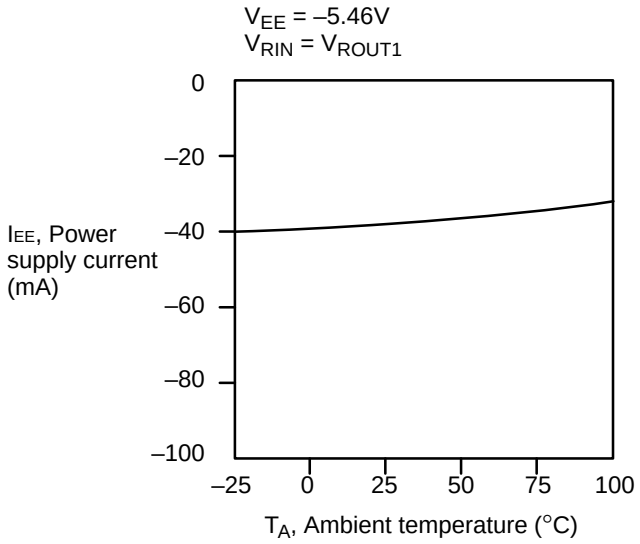
NOTES

1. **Preventing Switching Noise**
   To prevent switching noise in the analog output signal, connect noise limiting capacitors to the V_{EEA} and V_{EED} pins as close to the V_{CCA} and V_{CCD} pins as possible.

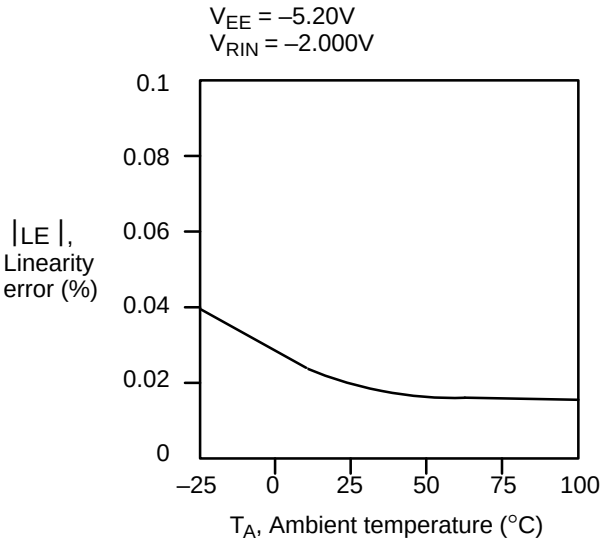
2. **Power Pattern**
   To reduce parasitic impedance, the PC board pattern to the V_{CCA}, V_{CCD}, V_{EEA} and V_{EED} pins should be as wide as possible.

MB40730 STANDARD CURVES

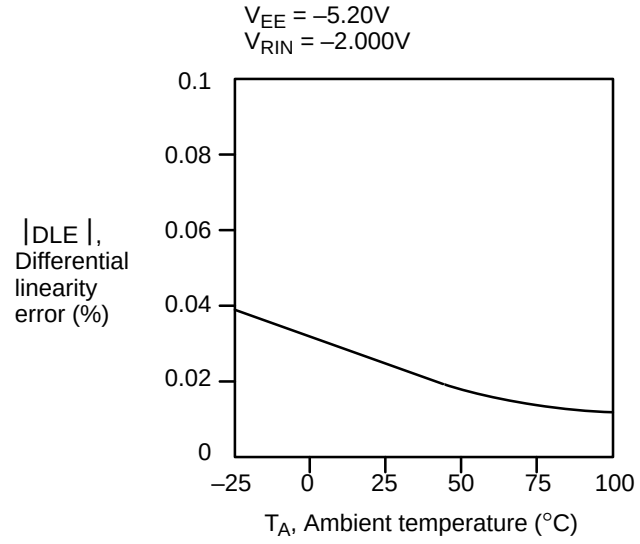
1. Power Supply Current vs. Ambient Temperature



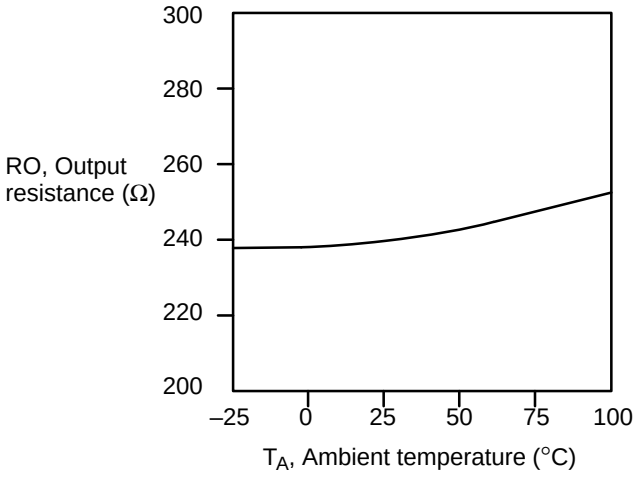
2. Linearity Error vs. Ambient Temperature



3. Differential Linearity Error vs. Ambient Temperature



4. Output Resistance vs. Ambient Temperature



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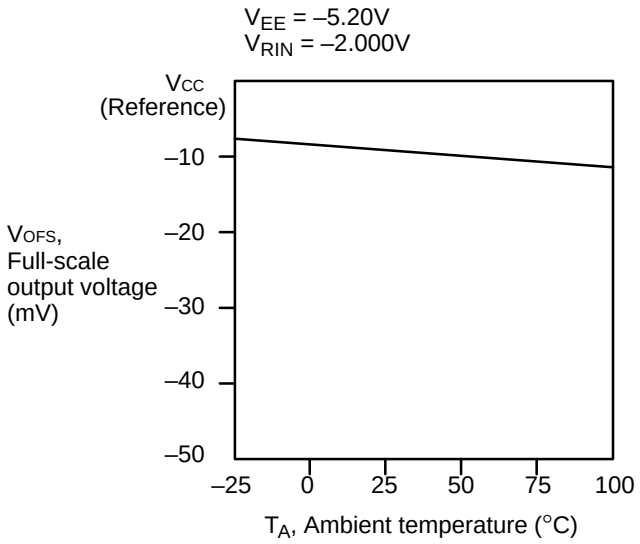
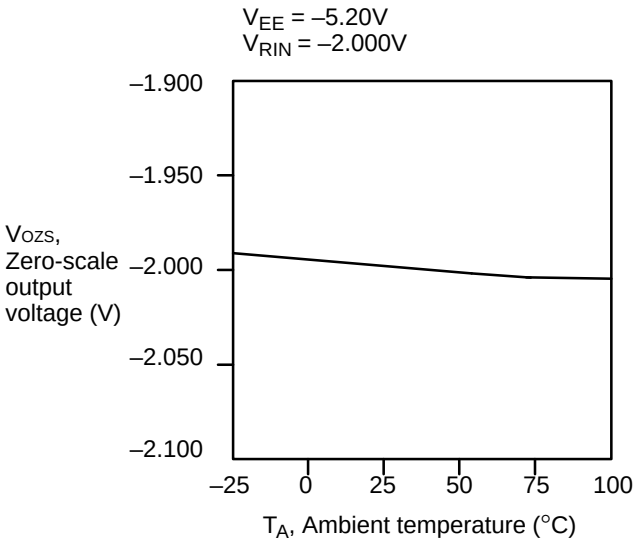
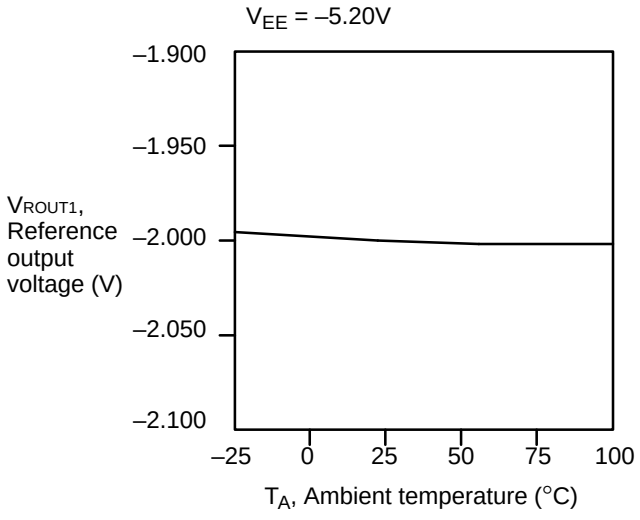
5. Full-Scale Output Voltage vs. Ambient Temperature



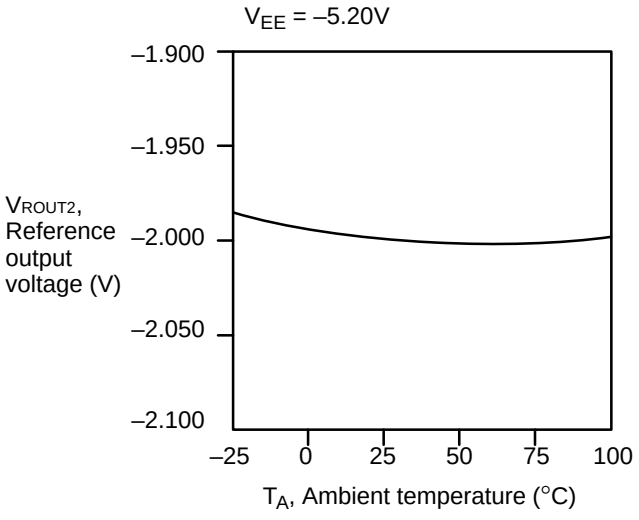
6. Zero-Scale Output Voltage vs. Ambient Temperature



7. V_{ROUT1} Reference Output Voltage vs. Ambient Temperature



8. V_{ROUT2} Reference Output Voltage vs. Ambient Temperature



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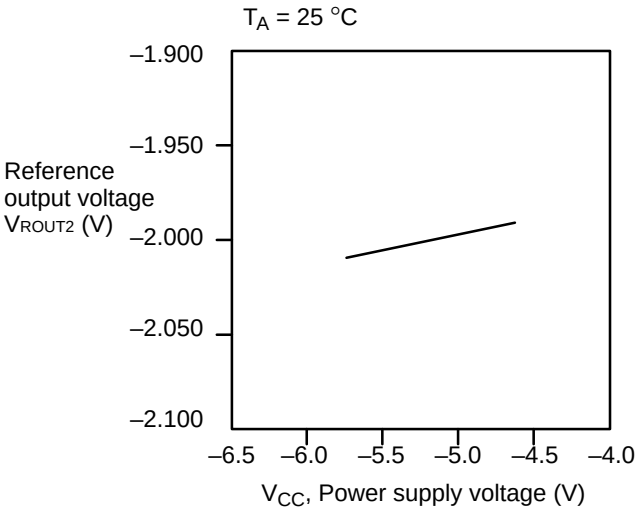
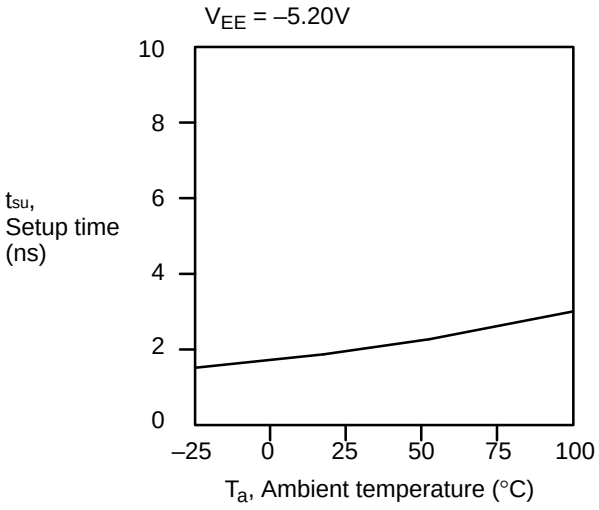
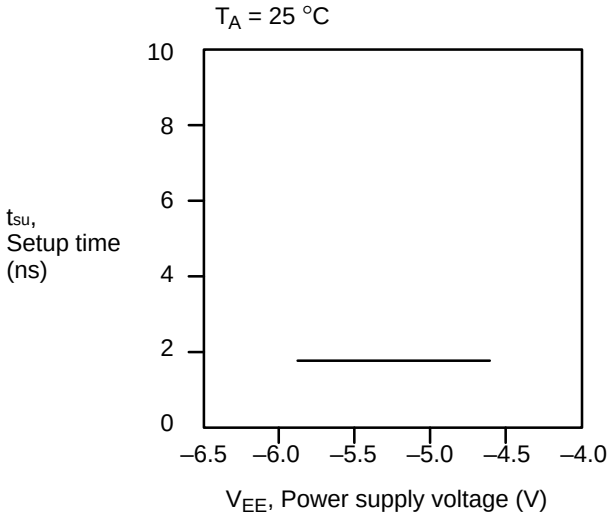
9. V_{ROUT2} Reference Output Voltage vs. Power Supply Voltage



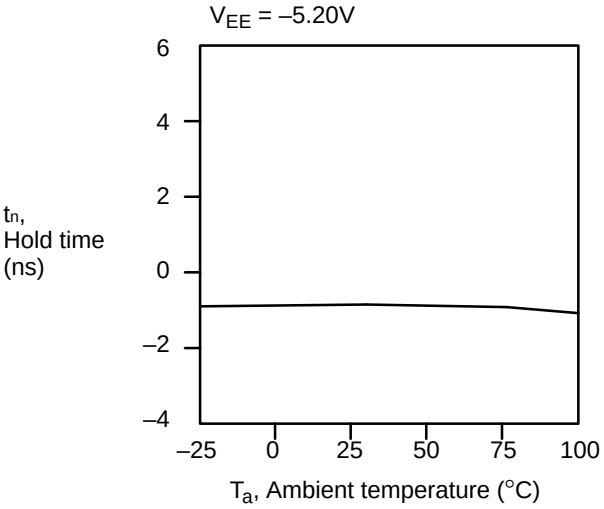
10. Setup Time vs. Ambient Temperature



11. Setup Time vs. Power Supply Voltage



12. Hold Time vs. Ambient Temperature



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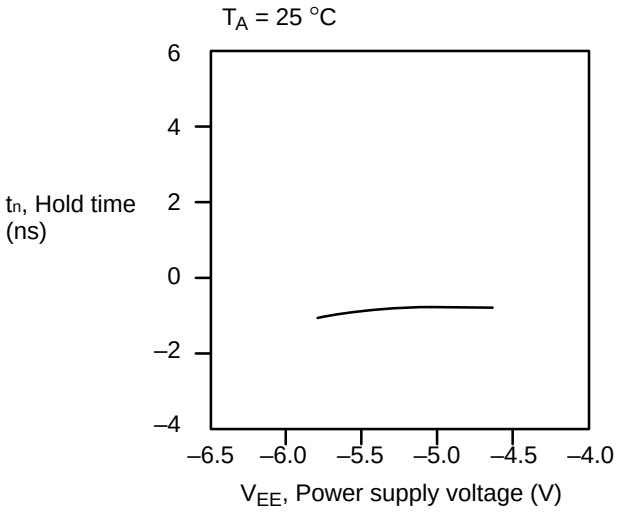
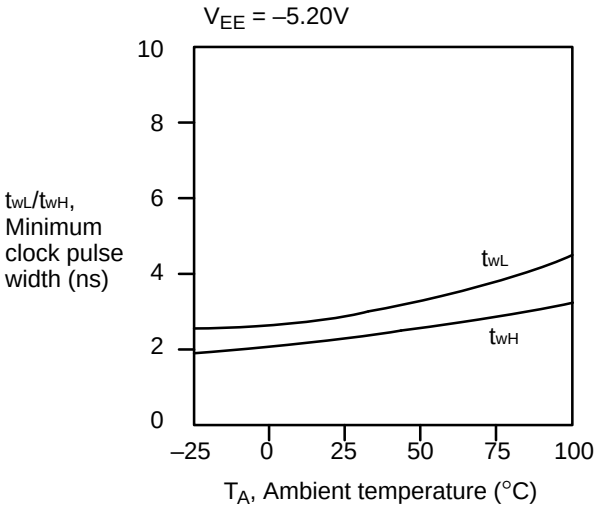
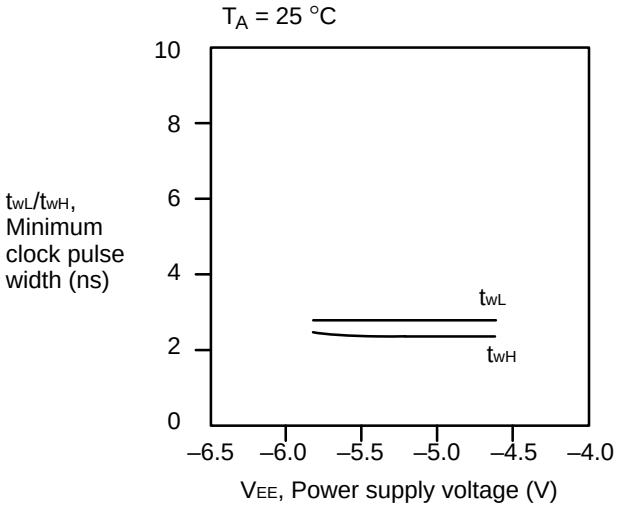
13. Hold Time vs. Power Supply Voltage



14. Minimum Clock Pulse Width vs. Ambient Temperature

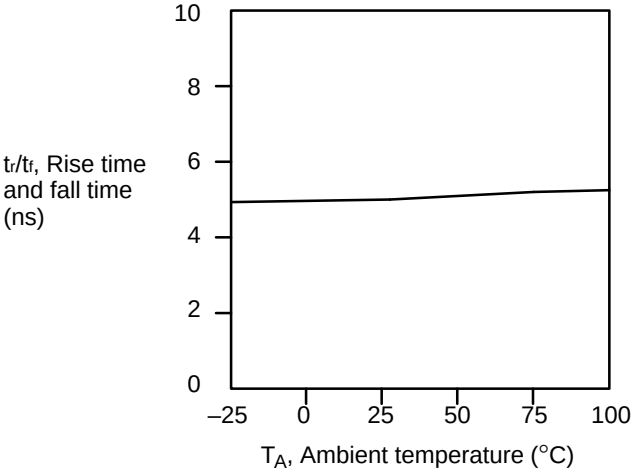


15. Minimum Clock Pulse Width vs. Power Supply Voltage



16. Rise Time / Fall Time vs. Ambient Temperature

V_{EE} = –5.20V
V_{RIN} = –2.000V
CL = 15 pF
Analog output 240 Ω termination
(1V amplitude)



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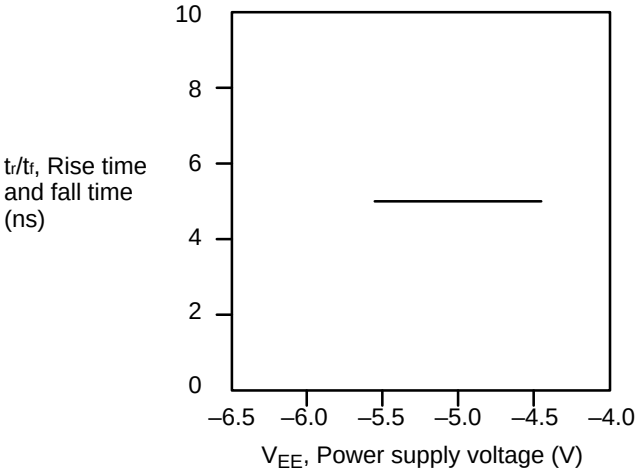
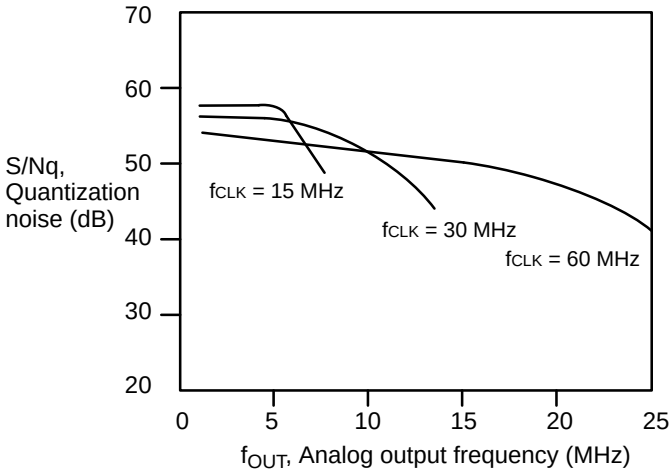
17. Rise Time / Fall Time vs. Power Supply Voltage

T_a= 25 °C
V_{RIN} = –2.000V
C_L = 15 pF
Analog output 240 Ω termination
(1V amplitude)

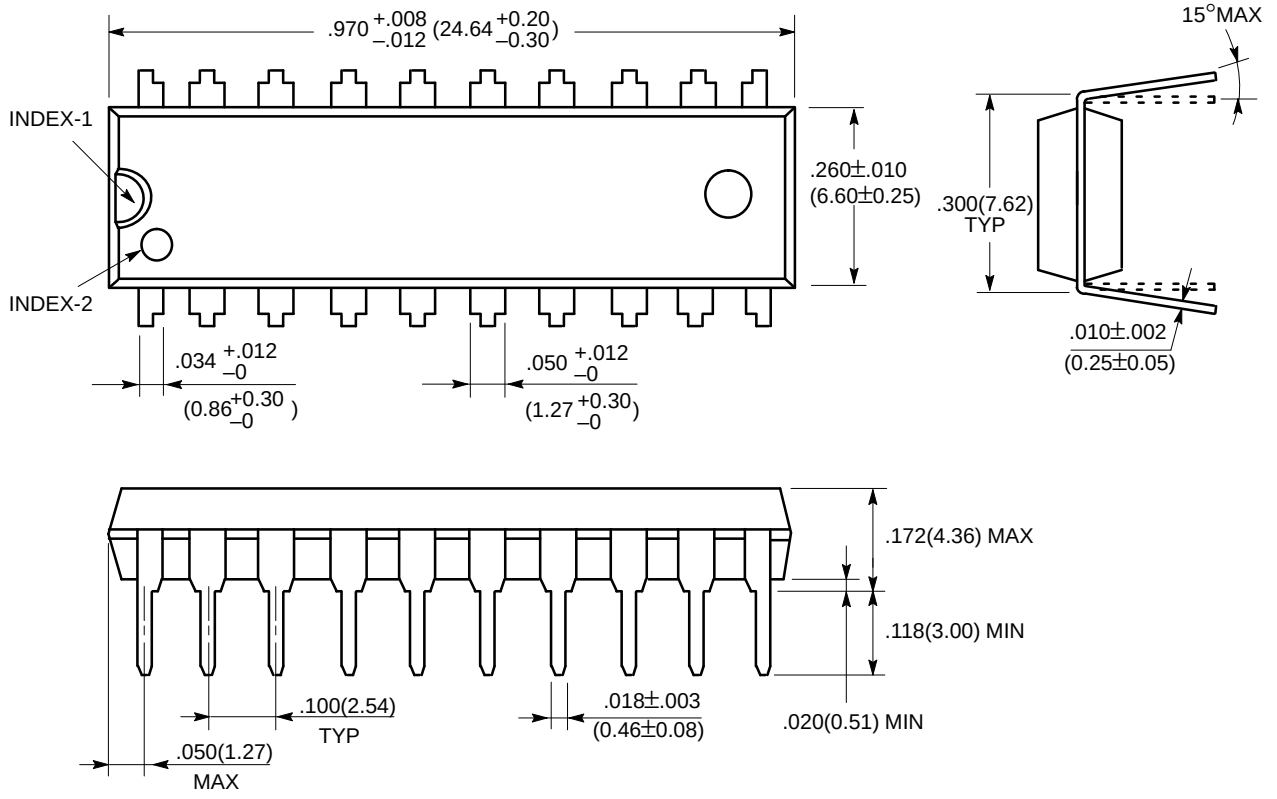


18. Quantization Noise vs. Analog Output Frequency



PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



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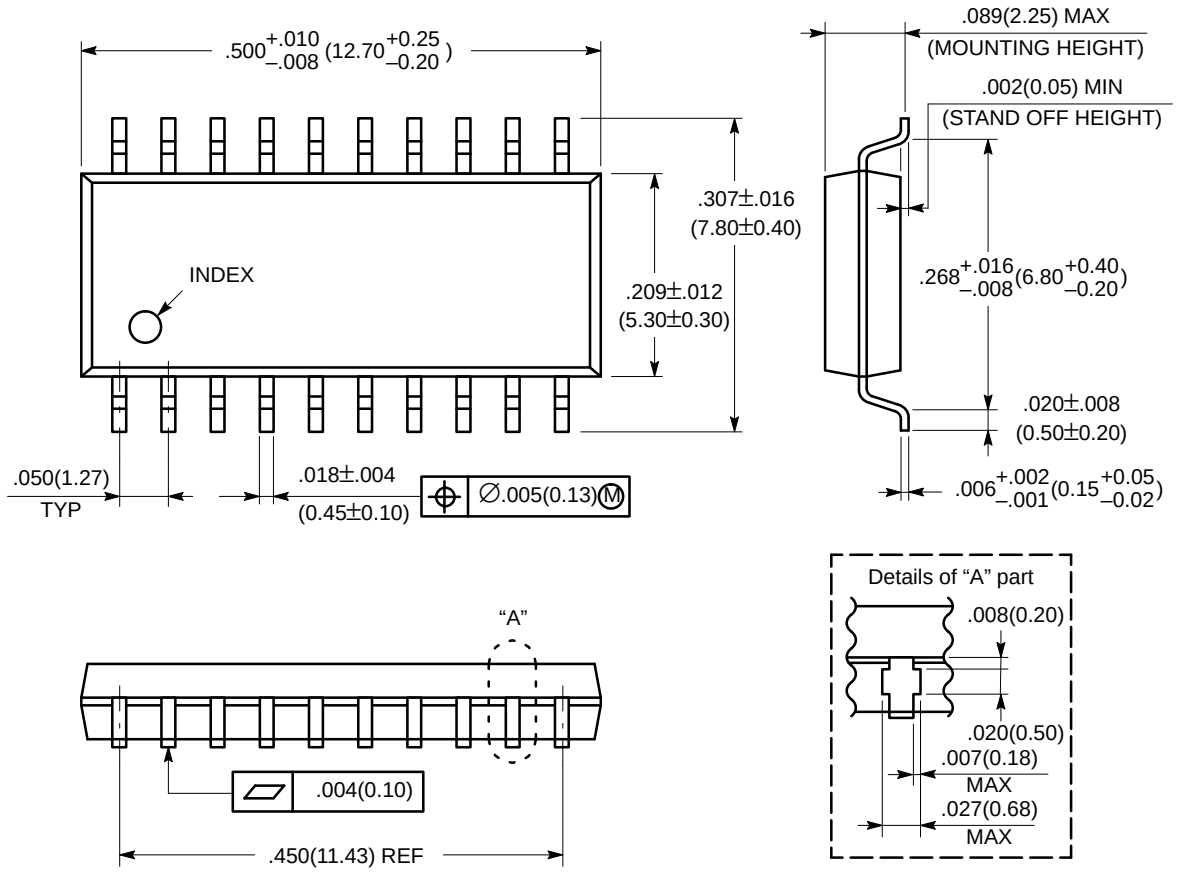
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



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Dimensions in
inches (millimeters)

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