April 1991
Edition 1.0

FUJITSU

DATA SHEET

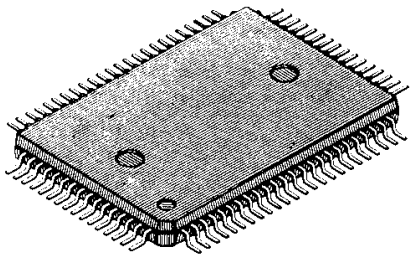
MB86490

CMOS AUTOMOBILE TELEPHONE AUDIO PROCESSOR

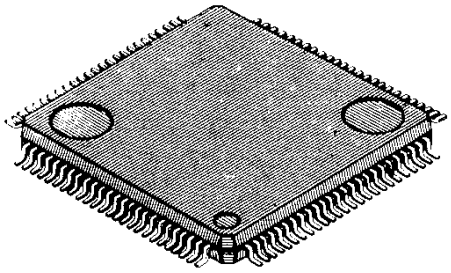
The Fujitsu MB86490 processes the baseband signal for automobile telephones for both AMPS (United States) and TACS (United Kingdom) systems.

The MB86490 combines the control signal processing functions of the MB87084 and the audio signal processing functions of the MB87085 on one chip. The MB86490's digital electronic volume enables highly precise gain control and consists of a 34-step switched capacitor filter (SCF).

PRELIMINARY



PLASTIC PACKAGE
(FPT-80P-M01)



PLASTIC PACKAGE
(FPT-100P-M05)

FEATURES

- Receiver
  - Phase shifter circuit: signal phase adjustable from 0 to 180 degrees
  - Pins for external expander
  - Muting control
- Transmitter
  - Limiter circuit suppresses instantaneous frequency deviation at frequency modulation
  - Muting control
  - DTMF circuit (dual- and single-tone)
    High group: 1633, 1477, 1336, 1209 and 1150Hz
    Low group: 941, 852, 770 and 697Hz
    Output level of low group can be set 2dB lower than high group
- Power Controller
  - 7-bit DAC LSB selectable: 4mV or 20mV
  - Level shifter circuit (5 to 1 Vp–p)
- Electronic volume, DAC, DTMF and stand-by mode controlled by serial data
- Power-saving stand-by function
- Inputs and outputs CMOS compatible
- Supply voltage: +5V

ABSOLUTE MAXIMUM RATINGS (See NOTE)

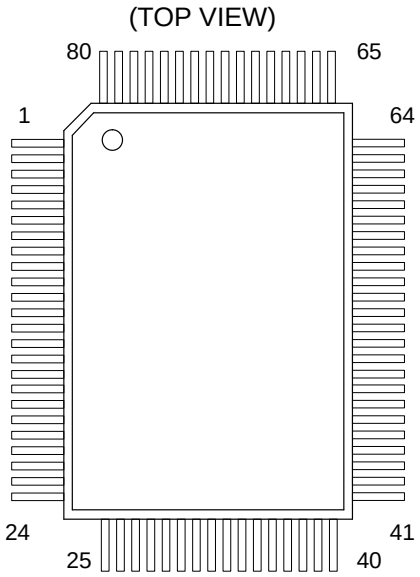
(GND = 0V)

Parameter	Symbol	Pin Name	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{DD}	V_{DD}	GND -0.3	–	7.0	V
Input Voltage	V_I	All input pins	GND -0.3	–	V_{DD} +0.3	V
Output Voltage	V_O	All output pins	GND -0.3	–	V_{DD} +0.3	V
Output Current	I_O	All output pins	–10	–	10	mA
Storage temperature	Tstg	–	–40	–	125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

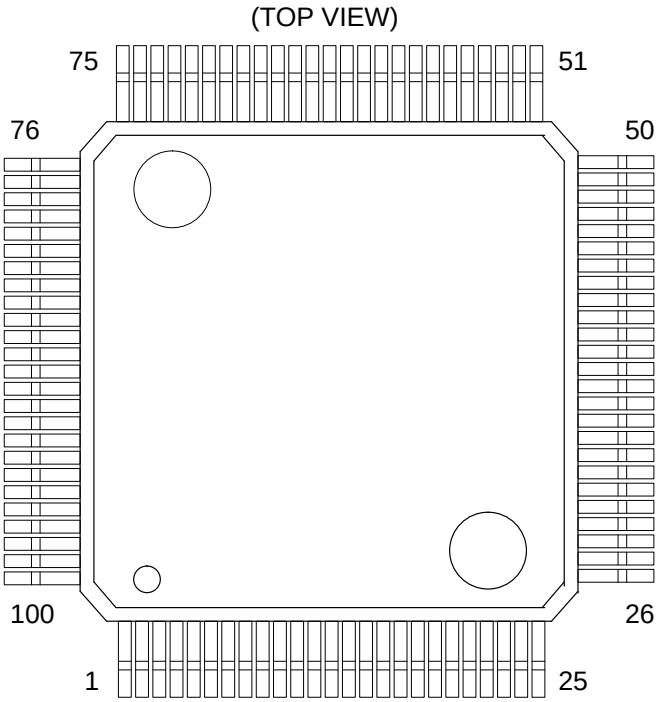
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT



(FPT-80P-M01)

Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol
1	–	(N.C.)	21	I	STB3	41	–	(N.C.)	61	O	AFOUT
2	O	LIMH	22	I	STB2	42	I	CMP2I	62	I	AMP8I
3	O	LIML	23	I	STB1	43	–	(N.C.)	63	O	AMP8O
4	O	LIMO	24	I	MODE	44	I	DISC	64	I	RR2
5	O	VR1O	25	I	DATA	45	–	(N.C.)	65	O	RR3
6	I	AFIN1	26	I	CLK	46	–	(N.C.)	66	O	RVDD2
7	I	AFIN2	27	I	$\overline{\text{RESET}}$	47	I	R2	67	O	RREF
8	O	AFINO	28	I	DTMFSS	48	O	PHSO	68	–	(N.C.)
9	I	AMP2I	29	I	RAM	49	O	C2	69	O	TVDD2
10	O	AMP2O	30	I	BYPS	50	I	R1	70	O	TREF
11	O	VR2O	31	O	RSAT	51	O	C1	71	O	DTMF2
12	–	AGT	32	O	RWBD	52	–	(N.C.)	72	I	AMP3I
13	–	(N.C.)	33	–	VDD1	53	O	AMP6O	73	–	VDD2
14	–	DG	34	–	AGR	54	I	DEM	74	O	AMP3O
15	I	SATS	35	O	PCONT	55	O	RE1	75	I	AFINN
16	I	WBDS	36	O	LS	56	I	EXP2	76	O	AMP1O
17	I	DTMFTS	37	I	PDET	57	O	RR1	77	I	WBDI
18	I	TAM	38	O	VREF	58	O	EXP1	78	I	TSAT
19	I	FRQC	39	I	ATT	59	I	RE2	79	O	TX
20	I	FCLK	40	I	DAREF	60	O	RE3	80	I	LIMI



(FPT-100P-M05)

Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol
1	O	LIMH	26	–	(N.C.)	51	I	DISC	76	–	(N.C.)
2	O	LIML	27	I	MODE	52	–	(N.C.)	77	–	(N.C.)
3	O	LIMO	28	–	(N.C.)	53	I	R2	78	I	RR2
4	O	VR1O	29	I	DATA	54	O	PHSO	79	O	RR3
5	I	AFIN1	30	–	(N.C.)	55	O	C2	80	–	(N.C.)
6	I	AFIN2	31	I	CLK	56	I	R1	81	O	RVDD2
7	O	AFIN0	32	–	(N.C.)	57	–	(N.C.)	82	O	RREF
8	I	AMP2I	33	–	(N.C.)	58	O	C1	83	–	(N.C.)
9	O	AMP2O	34	I	/RESET	59	–	(N.C.)	84	O	TVDD2
10	O	VR2O	35	I	STMFSS	60	–	(N.C.)	85	O	TREF
11	–	(N.C.)	36	I	RAM	61	–	(N.C.)	86	O	DTMF2
12	–	AGT	37	I	BYPS	62	O	AMP6O	87	I	AMP3I
13	–	(N.C.)	38	O	RSAT	63	–	(N.C.)	88	–	(N.C.)
14	–	DG	39	O	RWBD	64	I	DEM	89	–	VDD2
15	I	SATS	40	–	VDD1	65	–	(N.C.)	80	O	AMP3O
16	I	WBDS	41	–	(N.C.)	66	O	RE1	91	I	AFINN
17	I	DTMFTS	42	–	AGR	67	I	EXP2	92	–	(N.C.)
18	I	TAM	43	O	PCONT	68	–	(N.C.)	93	O	AMP1O
19	I	FRQC	44	O	LS	69	O	RR1	94	I	WBDI
20	–	(N.C.)	45	I	PDET	70	O	EXP1	95	I	TSAT
21	I	FCLK	46	O	VREF	71	I	RE2	96	–	(N.C.)
22	–	(N.C.)	47	I	ATT	72	O	RE3	97	O	TX
23	I	STB3	48	I	DATEF	73	O	AFOUT	98	I	LIMI
24	I	STB2	49	I	CMP21	74	I	AMP8I	99	–	(N.C.)
25	I	STB1	50	–	(N.C.)	75	O	AMP8O	100	–	(N.C.)

PIN DESCRIPTIONS

Circuit	Pin No.		I/O	Symbol	Descriptions
	QFP	SQFP			
Power supply	33	40	–	VDD1	Power supply (+5V)
	73	89	–	VDD2	
	12	12	–	AGT	Transmitter ground (0V)
	34	42	–	AGR	Receiver ground (0V)
	14	14	–	DG	Digital ground (0V)
Reference voltage section	70	85	O	TREF	Transmitter $V_{DD}/2$ circuit reference voltage
	69	84	O	TVDD2	Transmitter $V_{DD}/2$ circuit output voltage
	67	82	O	RREF	Receiver $V_{DD}/2$ circuit reference voltage
	66	81	O	RVDD2	Receiver $V_{DD}/2$ circuit output voltage
Power controller	40	48	I	DAREF	DAC reference voltage input (5V)
	39	47	I	ATT	DAC reference voltage input (0V)
	37	45	I	PDET	Level shifter input
	36	44	O	LS	Level shifter output
	38	46	O	VREF	DAC output
	35	43	O	PCONT	AMP11 output
Data input section	25	29	I	DATA	35-bit serial data controls the electronic volume, DAC, DTMF and stand-by function (for details, refer to the USE section). Data is loaded on the rising edge of the clock (CLK). Input data is loaded into the internal buffer register on the rising edge of STB1 to STB3. Pull the $\overline{\text{RESET}}$ pin low to initialize the buffer register. The MODE pin is used to configure the buffer register.
	26	31	I	CLK	
	27	34	I	$\overline{\text{RESET}}$	
	23	25	I	STB1	
	22	24	I	STB2	
	21	23	I	STB3	
	24	27	I	MODE	Buffer register mode switching pin (for details, see the USE section).
	20	21	I	FCLK	768kHz clock input. This pin is used for the reference clock for the SCF and DTMF generator circuits.

PIN DESCRIPTIONS (Continued)

<table>
<tr><th rowspan="2">Circuit</th><th colspan="2">Pin No.</th><th rowspan="2">I/O</th><th rowspan="2">Symbol</th><th rowspan="2">Descriptions</th></tr>
<tr><th>QFP</th><th>SQFP</th></tr>
<tr><td rowspan="9">Data receiver section</td><td>44</td><td>51</td><td>I</td><td>DISC</td><td>Receive signal input</td></tr>
<tr><td>32</td><td>39</td><td>O</td><td>RWBD</td><td>Receiver wideband data output
COMP1 output</td></tr>
<tr><td>51</td><td>58</td><td>O</td><td>C1</td><td rowspan="4">Phase shifter circuit control pins.
Signal phase is selectable with an external capacitor and resistor connected between these pins (for details, see the USE section).</td></tr>
<tr><td>50</td><td>56</td><td>I</td><td>R1</td></tr>
<tr><td>49</td><td>55</td><td>O</td><td>C2</td></tr>
<tr><td>47</td><td>53</td><td>I</td><td>R2</td></tr>
<tr><td>48</td><td>54</td><td>O</td><td>PHSO</td><td>Phase shifter circuit output</td></tr>
<tr><td>31</td><td>38</td><td>O</td><td>RSAT</td><td>SAT signal output</td></tr>
<tr><td>42</td><td>49</td><td>I</td><td>CMP2I</td><td>COMP2 positive input</td></tr>
<tr><td rowspan="9">Data transmitter section</td><td>19</td><td>19</td><td>I</td><td>FRQC</td><td>DTMF generator circuit and LPF3 mode switching pin:
<table>
<tr><th>FRQC</th><th>DTMF generator circuit</th><th>LPF3</th></tr>
<tr><td>H</td><td>No level difference</td><td>fc=20kHz</td></tr>
<tr><td>L</td><td>Output level of the low group signal set 2dB lower than high group signal</td><td>fc=16kHz</td></tr>
</table></td></tr>
<tr><td>74</td><td>90</td><td>O</td><td>AMP3O</td><td rowspan="2">AMP3 gain setting pins
AMP3O : AMP3 output
AMP3I : AMP3 inverting input</td></tr>
<tr><td>72</td><td>87</td><td>I</td><td>AMP3I</td></tr>
<tr><td>71</td><td>86</td><td>O</td><td>DTMF2</td><td>DTMF signal output</td></tr>
<tr><td>17</td><td>17</td><td>I</td><td>DTMFTS</td><td>DTMF output signal muting control “H” level : No mute
“L” level : Mute</td></tr>
<tr><td>16</td><td>16</td><td>I</td><td>WBDS</td><td>Wideband data signal muting control “H” level : No mute
“L” level : Mute</td></tr>
<tr><td>77</td><td>94</td><td>I</td><td>WBDI</td><td>Wideband data signal input</td></tr>
<tr><td>15</td><td>15</td><td>I</td><td>SATS</td><td>SAT signal muting control “H” level : No mute
“L” level : Mute</td></tr>
<tr><td>78</td><td>95</td><td>I</td><td>TSAT</td><td>SAT signal input</td></tr>
</table>

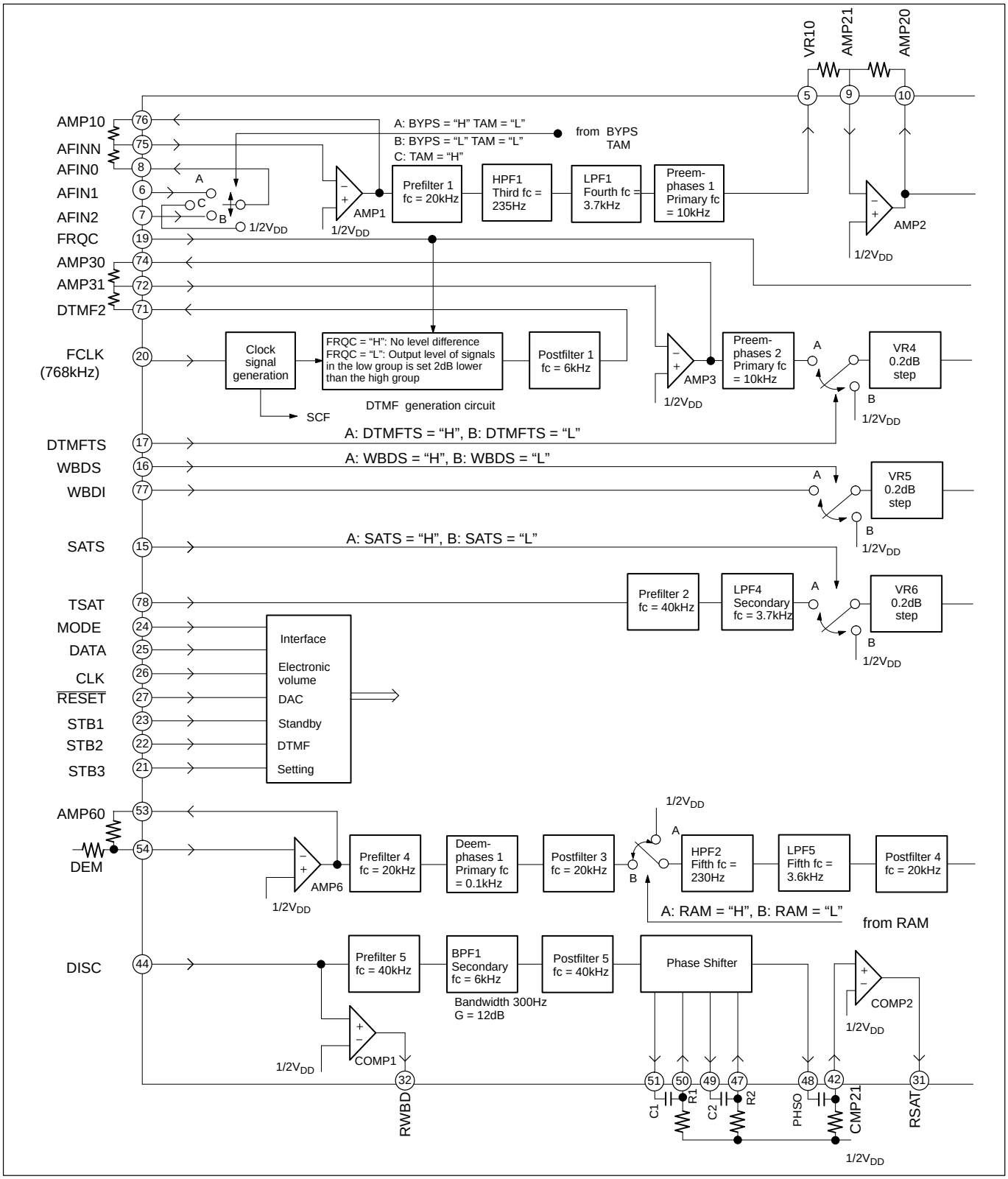
PIN DESCRIPTIONS (Continued)

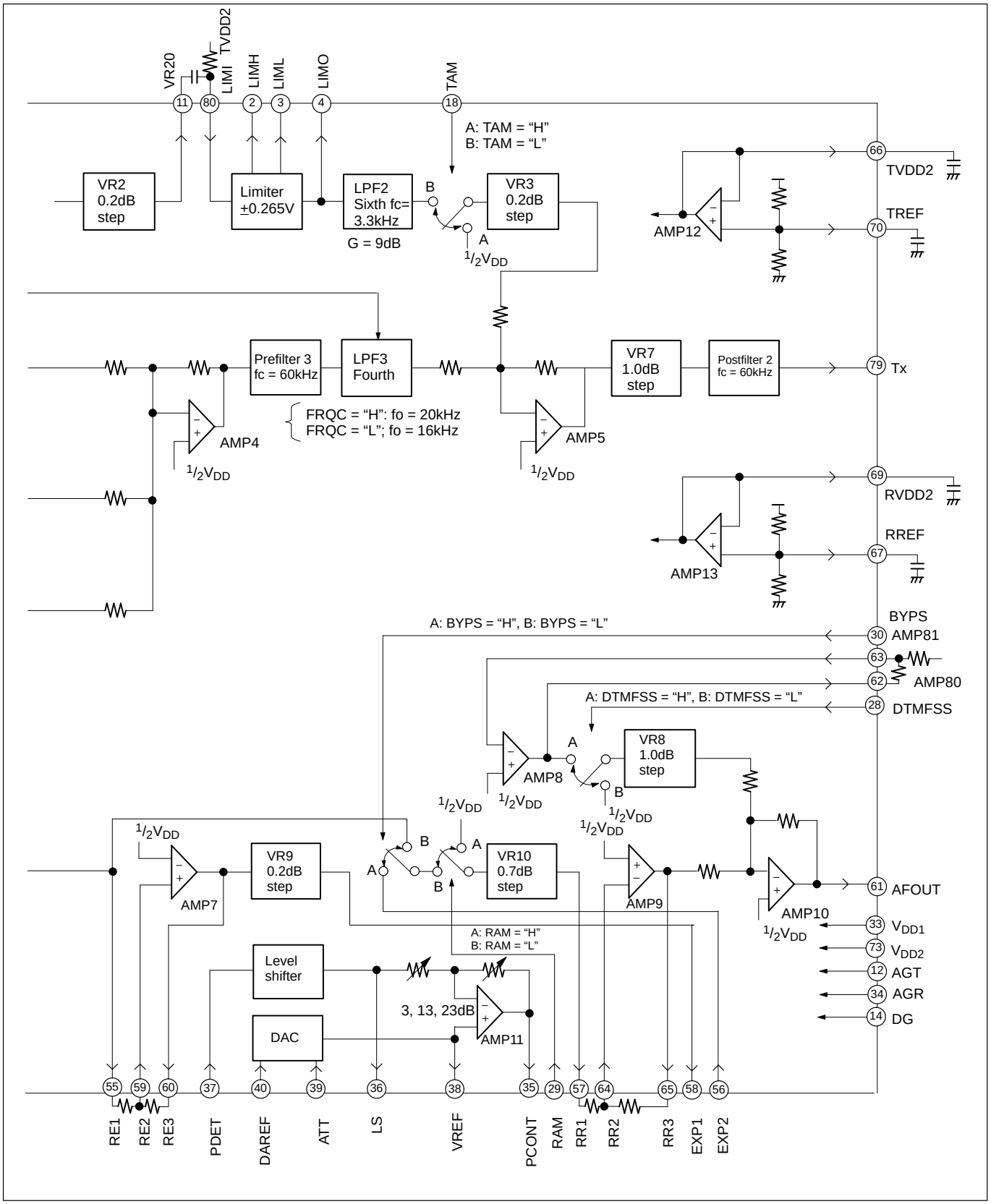
Circuit	Pin No.		I/O	Symbol	Descriptions
	QFP	SQFP			
Audio signal receiver section	54	64	I	DEM	Received audio signal input pin (AMP6 gain control pins) DEM : AMP6 inverting input AMP6O : AMP6 output
	53	62	O	AMP6O	
	29	36	I	RAM	Received audio signal muting control "H" level : No mute "L" level : Mute
	55	66	O	RE1	AMP7 gain setting pins RE1 : Postfilter 4 output RE2 : AMP7 inverting output RE3 : AMP7 output
	59	71	I	RE2	
	60	72	O	RE3	
	57	69	O	RR1	AMP9 gain setting pins RR1 : VR10 output RR2 : AMP9 inverting input RR3 : AMP9 output
	64	78	I	RR2	
	65	79	O	RR3	
	58	70	O	EXP1	Output to external expander. VR9 output
	56	67	I	EXP2	Input from external expander
	61	73	O	AFOUT	Received audio signal output
	63	75	O	AMP8O	AMP8 gain setting pins AMP8O : AMP8 output AMP8I : AMP8 inverting input
	62	74	I	AMP8I	
	28	35	I	DTMFSS	DTMF signal muting control "H" level : No mute "L" level : Mute
	30	37	I	BYPS	Switch control signal "H" level : An external compander is connected. AFIN1 is strapped to AFINO "L" level : An external compander is not connected. AFIN2 is strapped to AFINO

PIN DESCRIPTIONS (Continued)

<table>
<tr><th rowspan="2">Circuit</th><th colspan="2">Pin No.</th><th rowspan="2">I/O</th><th rowspan="2">Symbol</th><th rowspan="2">Descriptions</th></tr>
<tr><th>QFP</th><th>SQFP</th></tr>
<tr><td rowspan="15">Audio signal transmitter section</td><td>6</td><td>5</td><td>I</td><td>AFIN1</td><td rowspan="3">Transmitted audio signal input switching pin:
<table><tr><th>TAM</th><th>BYPS</th><th>SW</th></tr><tr><td>“L”</td><td>“H”</td><td>AFIN1 is strapped to AFINO.</td></tr><tr><td>“L”</td><td>“L”</td><td>AFIN2 is strapped to AFINO.</td></tr><tr><td>“H”</td><td>–</td><td>AFINO is strapped to VDD/2.</td></tr></table></td></tr>
<tr><td>7</td><td>6</td><td>I</td><td>AFIN2</td></tr>
<tr><td>8</td><td>7</td><td>O</td><td>AFINO</td></tr>
<tr><td>5</td><td>4</td><td>O</td><td>VR1O</td><td>Preemphasis 1 output pin</td></tr>
<tr><td>75</td><td>91</td><td>I</td><td>AFINN</td><td rowspan="2">Transmitted audio signal input pin. AMP1 gain setting pins.
AFINN : AMP1 inverting input
AMP1O : AMP1 output</td></tr>
<tr><td>76</td><td>93</td><td>O</td><td>AMP1O</td></tr>
<tr><td>11</td><td>10</td><td>O</td><td>VR2O</td><td>VR2 output</td></tr>
<tr><td>10</td><td>9</td><td>O</td><td>AMP2O</td><td rowspan="2">AMP2 gain setting pins
AMP2O : AMP2 output
AMP2I : AMP2 inverting input</td></tr>
<tr><td>9</td><td>8</td><td>I</td><td>AMP2I</td></tr>
<tr><td>80</td><td>98</td><td>I</td><td>LIMI</td><td>Limiter circuit input</td></tr>
<tr><td>4</td><td>3</td><td>O</td><td>LIMO</td><td>Limiter circuit output</td></tr>
<tr><td>2</td><td>1</td><td>O</td><td>LIMH</td><td>Limiter circuit H-level signal output</td></tr>
<tr><td>3</td><td>2</td><td>O</td><td>LIML</td><td>Limiter circuit L-level signal output</td></tr>
<tr><td>18</td><td>18</td><td>I</td><td>TAM</td><td>Transmitter muting control pin
“H” level : Mute
“L” level : No mute</td></tr>
<tr><td>79</td><td>79</td><td>O</td><td>TX</td><td>Transmitted signal output</td></tr>
</table>

BLOCK DIAGRAM




VR20
TVDD2
LIMI
LIMH
LIML
LIMO
TAM
11
80
2
3
4
18
A: TAM = "H"
B: TAM = "L"
VR2
0.2dB
step
Limiter
±0.265V
LPF2
Sixth fc=
3.3kHz
G = 9dB
B
A
1/2VDD
VR3
0.2dB
step
66
TVDD2
TREF
70
AMP12
Prefilter 3
fc = 60kHz
LPF3
Fourth
FRQC = "H": fo = 20kHz
FRQC = "L"; fo = 16kHz
VR7
1.0dB
step
Postfilter 2
fc = 60kHz
79
Tx
AMP4
AMP5
1/2VDD
69
RVDD2
RREF
67
AMP13
BYPS
A: BYPS = "H", B: BYPS = "L"
30
AMP81
63
62
AMP80
A: DTMFSS = "H", B: DTMFSS = "L"
28
DTMFSS
AMP8
VR8
1.0dB
step
VR9
0.2dB
step
VR10
0.7dB
step
AMP7
AMP9
AMP10
61
AFOUT
33
VDD1
73
VDD2
12
AGT
34
AGR
14
DG
A: RAM = "H"
B: RAM = "L"
Level
shifter
DAC
3, 13, 23dB
AMP11
55
59
60
37
40
39
36
38
35
29
57
64
65
58
56
RE1
RE2
RE3
PDET
DAREF
ATT
LS
VREF
PCONT
RAM
RR1
RR2
RR3
EXP1
EXP2

CIRCUIT CONFIGURATION

1. Receiver

(1) Audio Signal receiver section

The audio signal receiver section processes the demodulated signal input to the demodulator pin (DEM, pin 54). The signal is then output at AFOUT (pin 61). The receiver synthesizes DTMF signals input to AMP8I (pin 62).

- Audio signal receiver section
  Audio receiver section
  - ① Gain control amplifier (AMP6)
  - ② Deemphasis circuit (prefilter4, deemphasis 1 and postfilter 3)
  - ③ Muting switch (control pin: RAM)
  - ④ Filter circuit (HPF2, LPF5 and postfilter 4)
  - ⑤ Gain control amplifier (AMP7)
  - ⑥ Electronic volume (VR9)
  - ⑦ Expander connection pin
  - ⑧ Bypass switch (control pin: BYPS)
  - ⑨ Muting switch (control pin: RAM)
  - ⑩ Electronic volume (VR10)
  - ⑪ Gain control amplifier (AMP9)
  - ⑫ Summing amplifier (AMP10)

  DTMF signal input section
  - ① Gain control amplifier (AMP8)
  - ② Muting switch (control pin: DTMFSS)
  - ③ Electronic volume (VR8)
  - ④ To ⑫ summing amplifier (AMP10) in the audio signal receiver section

(2) Data receiver section

The data receiver section processes demodulated signals input to DISC (pin 44) and outputs them at RSAT (pin 31). It also outputs a wideband data signal at RWBD (pin 32).

- Data receiver section
  - ① Wideband data signal output section (comparator 1)
  - ② Filter circuit (prefilter 5, BPF1 and postfilter 5)
  - ③ Phase shifter circuit
  - ④ Comparator 2

2. Transmitter

(1) Audio signal transmitter section

The audio transmitter section processes the audio signals input to AFIN1 (pin 6) or AFIN2 (pin 7) and output them at tX (pin 79).

- Audio transmitter section circuit
  - ① Audio signal input pin selector switch (control pin: BYPS and TAM)
  - ② Gain control amplifier (AMP1)
  - ③ Filter circuit (prefilter 1, HPF1 and LPF1)
  - ④ Preemphasis circuit (preemphasis 1)
  - ⑤ Gain control amplifier (AMP2)
  - ⑥ Electronic volume (VR2)
  - ⑦ Limiter circuit
  - ⑧ Filter circuit (LPF2)
  - ⑨ Muting switch (control pin: TAM)
  - ⑩ Electronic volume (VR3)
  - ⑪ Summing amplifier (AMP5)
  - ⑫ Electronic volume (VR7)
  - ⑬ Filter circuit (postfilter 2)

(2) Data Transmitter section

The data transmitter section synthesizes and amplifies the clock input to FCLK (pin 20), the wideband data signal from WBDI (pin 16), and SAT signal from TSAT (pin 78). The audio signal is output at the TX pin (pin 79).

- Data transmitter circuit
  DTMF signal section
  - ① Clock generator circuit
  - ② DTMF generator circuit (DTMF generator circuit and postfilter 1)
  - ③ Gain control amplifier (AMP3)
  - ④ Preemphasis circuit (preemphasis 2)
  - ⑤ Muting switch (control pin: DTMFTS)
  - ⑥ Electronic volume (VR4)
  - ⑦ To transmitted data synthesizing section

  Wideband data signal section
  - ① Muting switch (control pin: WBDS)
  - ② Electronic volume (VR5)
  - ③ To transmitted data synthesizing section

CIRCUIT CONFIGURATION

SAT signal section

① Filter circuit (prefilter 2 and LPF4)
② Muting switch (control pin: SATS)
③ Electronic volume (VR6)
④ To transmitted data synthesizing section

Transmitted data synthesizing section

① Input signals from DTMF, wideband data and SAT signal sections
② Summing amplifier (AMP4)
③ Filter circuit (prefilter 3 and LPF3)
④ To ⑪ summing amplifier (AMP5) in the audio transmitter section

(3) Power controller

The power controller detects the transmission power of the modulated signal input to the PDET (pin 37) and controls the transmitter amplifier output using the signal output from PCONT (pin 35).

- Power controller circuit

① Level shifter circuit
② 7-bit DAC
③ Gain amplifier (AMP11)

(3) Reference voltage generator

The transmitter and receiver operate with the reference voltage output fro TVDD2 (pin 69) and RVDD2 (pin 66) respectively.

① VDD/2 generator circuit (AMP12) in transmitter system
② VDD/2 generator circuit (AMP13) in receiver system

USE

The electronic volume, DAC, AMP11, DTMF and the stand–by mode are controlled by data written into the buffer register.

1. Buffer Register

(1) Buffer register configuration

- Mode = “H” level

STB1		–	–
STB2	–		–
STB3	–	–	
D1	–	VR84	–
D2	–	VR83	–
D3	–	VR82	–
D4	–	VR81	–
D5	–	VR74	–
D6	–	VR73	–
D7	–	VR72	–
D8	–	VR71	–
D9	–	AMS2	–
D10	–	AMS1	–
D11	–	VR55	VR105
D12	–	VR54	VR104
D13	–	VR53	VR103
D14	–	VR52	VR102
D15	–	VR51	VR101
D16	—	VR65	VR94
D17	–	VR64	VR93
D18	–	VR63	VR92
D19	–	VR62	VR91
D20	–	VR61	VR35
D21	–	VR45	VR34
D22	–	VR44	VR33
D23	–	VR43	VR32
D24	–	VR42	VR31
D25	–	VR41	VR25
D26	–	DAS1	VR24
D27	–	DAB7	VR23
D28	–	DAB6	VR22
D29	E/DH	DAB5	VR21
D30	DTS1	DAB4	–
D31	DTS2	DAB3	–
D32	DTS3	DAB2	–
D33	E/DL	DAB1	–
D34	DTS4	SB1	SB2
D35	DTS5	SB2	SB1

- Mode = “L” level

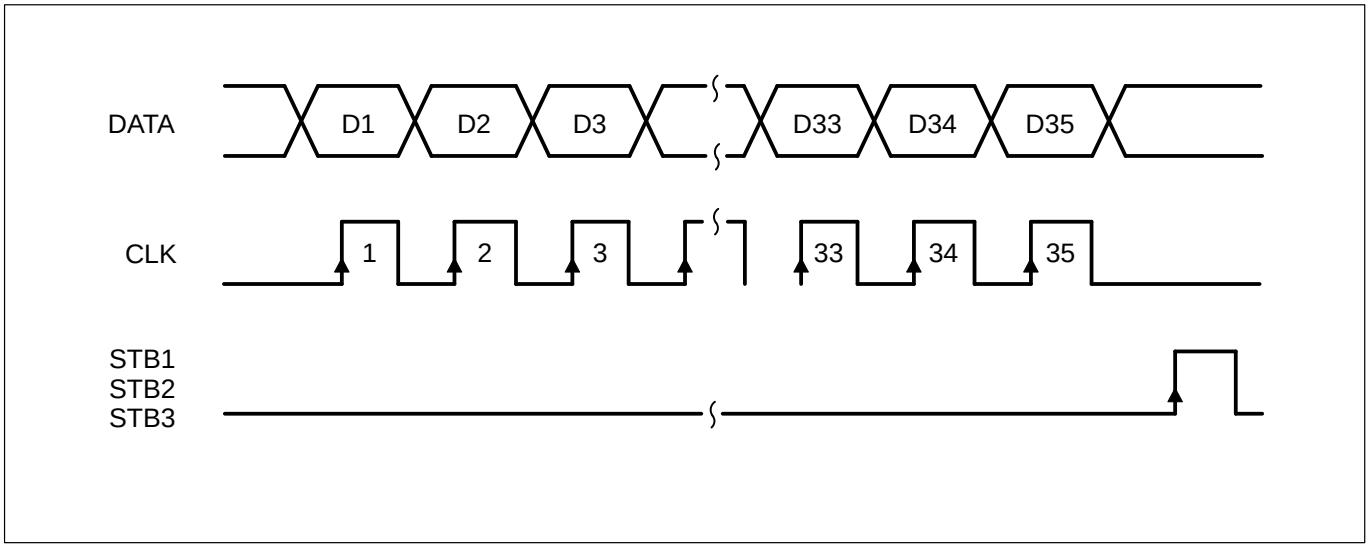
STB1		–	–
STB2	–		–
STB3	–	–	
D1	–	–	VR105
D2	–	–	VR104
D3	–	–	VR103
D4	–	–	VR102
D5	–	–	VR101
D6	–	–	VR94
D7	–	–	VR93
D8	–	–	VR92
D9	–	–	VR91
D10	–	–	VR74
D11	–	–	VR73
D12	–	–	VR72
D13	–	–	VR71
D14	–	–	VR65
D15	–	–	VR64
D16	—	–	VR63
D17	–	–	VR62
D18	–	–	VR61
D19	–	–	VR55
D20	ED/H	–	VR54
D21	DTS1	–	VR53
D22	DTS2	–	VR52
D23	DTS3	–	VR51
D24	E/DL	–	VR35
D25	DTS4	–	VR34
D26	DTS5	AMS2	VR33
D27	VR45	AMS1	VR32
D28	VR44	DAS1	VR31
D29	VR43	DAB7	VR25
D30	VR42	DAB6	VR24
D31	VR41	DAB5	VR23
D32	VR84	DAB4	VR22
D33	VR83	DAB3	VR21
D34	VR82	DAB2	SB2
D35	VR81	DAB1	SB1

NOTE: Each control signal in the buffer register is set to the following logic level if the RESET pin is pulled low.
AAA: Control signals are set to “L” level AAA: Control signals are set to “H” level.

USE

(2) Timing chart

- Data signal read timing



The above timing diagram shows how data is clocked into the DATA buffer register.
The DATA signal is read on the rising edge of CLK and latched in the buffer register on the rising edge of STB1, STB2 or STB3.

2. Electronic volume setting

	Buffer register name					Electronic volume No.			
Electronic volume selection conditions	VR25	VR24	VR23	VR22	VR21	VR2	–	–	–
	VR35	VR34	VR33	VR32	VR31	VR3	–	–	–
	VR45	VR44	VR43	VR42	VR41	VR4	–	–	–
	VR55	VR54	VR53	VR52	VR51	VR5	–	–	–
	VR65	VR64	VR63	VR62	VR61	VR6	–	–	–
	–	VR74	VR73	VR72	VR71	–	–	VR7	–
	–	VR84	V483	VR82	VR81	–	–	VR8	–
	–	VR94	VR93	VR92	VR91	–	VR9	–	–
	VR105	VR104	VR103	VR102	VR101	–	–	–	VR10
Setting condition	**Buffer register input data**					**Electronic volume setting value (dB)**			
	H	H	H	H	H	3.0	1.4	7.0	10.5
	H	H	H	H	L	2.8	1.2	6.0	9.8
	H	H	H	L	H	2.6	1.0	5.0	9.1
	H	H	H	L	L	2.4	0.8	4.0	8.4
	H	H	L	H	H	2.2	0.6	3.0	7.7
	H	H	L	H	L	2.0	0.4	2.0	7.0
	H	H	L	L	H	1.8	0.2	1.0	6.3
	H	H	L	L	L	1.6	0.0	–0.0	5.6
	H	L	H	H	H	1.4	–0.2	–1.0	4.9
	H	L	H	H	L	1.2	–0.4	–2.0	4.2
	H	L	H	L	H	1.0	–0.6	–3.0	3.5
	H	L	H	L	L	0.8	–0.8	–4.0	2.8
	H	L	L	H	H	0.6	–1.0	–5.0	2.1
	H	L	L	H	L	0.4	–1.2	–6.0	1.4
	H	L	L	L	H	0.2	–1.4	–7.0	0.7
	H	L	L	L	L	0.0	–1.6	–8.0	0.0
	L	H	H	H	H	–0.2	–	–	–0.7
	L	H	H	H	L	–0.4	–	–	–1.4
	L	H	H	L	H	–0.6	–	–	–2.1
	L	H	H	L	L	–0.8	–	–	–2.8
	L	H	L	H	H	–1.0	–	–	–3.5
	L	H	L	H	L	–1.2	–	–	–4.2
	L	H	L	L	H	–1.4	–	–	–4.9
	L	H	L	L	L	–1.6	–	–	–5.6
	L	L	H	H	H	–1.8	–	–	–6.3
	L	L	H	H	L	–2.0	–	–	–7.0
	L	L	H	L	H	–2.2	–	–	–7.7
	L	L	H	L	L	–2.4	–	–	–8.4
	L	L	L	H	H	–2.6	–	–	–9.1
	L	L	L	H	L	–2.8	–	–	–9.8
	L	L	L	L	H	–3.0	–	–	–10.5
	L	L	L	L	L	–3.2	–	–	–11.2

To use this table

To set the gain of electronic volume VR2, find VR2 in the “Electronic volume No.” column. Then, select a value in the “Electronic volume setting value” column below the “Electronic volume” column. Find the input data in the columns of VR25, VR23, VR22, VR21 at the left on the same row wo the gain setting value.

USE

3. DAC setting

Buffer register input data							DAC output level	
DAB7	DAB6	DAB5	DAB4	DAB3	DAB2	DAB1	Condition: DAS1 = “H” level	Condition: DAS1 = “L” level
H	H	H	H	H	H	H	3.760V	1.877V
H	H	H	H	H	H	L	3.740V	1.873V
H	H	H	H	H	L	H	3.720V	1.869V
∼	∼	∼	∼	∼	∼	∼	∼	∼
H	H	L	L	L	L	L	3.120V	1.749V
∼	∼	∼	∼	∼	∼	∼	∼	∼
H	L	L	L	L	H	L	2.540V	1.633V
H	L	L	L	L	L	H	2.520V	1.629V
H	L	L	L	L	L	L	2.500V	1.625V
L	H	H	H	H	H	H	2.480V	1.621V
L	H	H	H	H	H	L	2.460V	1.617V
L	H	H	H	H	L	H	2.440V	1.613V
∼	∼	∼	∼	∼	∼	∼	∼	∼
L	H	L	L	L	L	L	1.880V	1.501V
∼	∼	∼	∼	∼	∼	∼	∼	∼
L	L	L	L	L	H	L	1.260V	1.377V
L	L	L	L	L	L	H	1.240V	1.373V
L	L	L	L	L	L	L	1.220V	1.369V

DAREF = 5.0V, ATT = 0.0V

4. AMP11 gain setting

Buffer register input data		AMP11 setting value	
AMS1	AMS2	Gain	PCONT output voltage
H	H	23 (dB)	V_{REF} –14.13 × (LS – V_{REF}) (V)
L	H		
H	L	13 (dB)	V_{REF} – 4.46 × (LS – V_{REF}) (V)
L	L	3 (dB)	V_{REF} – 1.41 × (LS – V_{REF}) (V)

5. DTMF output level setting

(1) High group frequency setting method

Buffer register input data				Output frequency
E/DH	DTS1	DTS2	DTS3	
H	H	H	L	1633Hz
H	H	L	L	1477Hz
H	L	H	L	1336Hz
H	L	L	L	1209Hz
H	L	L	H	1150Hz
H	H	–	H	Counter is not operating.
H	–	H	H	
L	–	–	–	

(2) Low group frequency setting method

Buffer register input data			Output frequency
E/DL	DTS4	DTS5	
H	H	H	941Hz
H	H	L	852Hz
H	L	H	770Hz
H	L	L	697Hz
L	–	–	Counter is not operating.

USE

6. Stand–by mode

(1) Buffer register setting data

SB1 input data		L	H	L	H
SB2 input data		H	L	L	H
Circuit name	COMP1	O	O	O	O
	AMP8, VR8	O	O	O	O
	DTMF generator circuit, postfilter 1	O	X	O	O
	AMP3, preemphasis 2, VR4, VR6, prefilter 2, LPF4, prefilter 5, BPF1, postfilter 5, Phase shifter, COMP2	X	X	X	O
	Level shifter, DAC, AMP11	O	O	X	O
	VR5, AMP4, prefilter 3, LPF3, AMP5, VR7, postfilter 2	O	O	X	O
	AMP1, prefilter 1, HPF1, LPF1, preemphasis 1, AMP2, VR2, limiter, PF2, VR3	X	X	X	O
	AMP6, prefilter 4, deemphasis 1, postfilter 3	X	X	X	O
	AMP10	O	O	O	O
	HPF2, LPH5, postfilter 4, AMP7, VR9, VR10, AMP9	X	X	X	O
	AMP12, AMP13	O	O	O	O
	SW, control circuit, buffer register	O	O	O	O

O : Operating
X : Stand–by

(2) Output pin status in stand–by mode

Pin No.		Symbol	Output pin status			
QFP	SQFP					
32	39	RWBD	–	–	–	–
31	38	RSAT	L	L	L	–
79	97	TX	–	–	D	–
49	55	C2	D	D	D	–
51	58	C1	D	D	D	–
71	86	DTMF2	–	D	–	–
74	90	AMP3O	D	D	D	–
63	75	AMP8O	–	–	–	–
35	43	PCONT (*)	–	–	Z	–
36	44	LS (*)	–	–	Z	–
38	46	VREF	–	–	Z	–
76	93	AMP1O	D	D	D	–
5	4	VR1O	D	D	D	–
10	9	AMP2O	D	D	D	–
11	10	VR2O	D	D	D	–
2	1	LIMH	–	–	–	–
3	2	LIML	–	–	–	–
4	3	LIMO	D	D	D	–
53	62	AMP6O	D	D	D	–
61	73	AFOUT	–	–	–	–
SB1 input data			L	H	L	H
SB2 input data			H	L	L	H

Pin No.		Symbol	Output pin status			
QFP	SQFP					
55	66	RE1	D	D	D	–
60	72	RE3	D	D	D	–
57	69	RR1	D	D	D	–
65	79	RR3	D	D	D	–
58	70	EXP1	D	D	D	–
48	54	PHSO	D	D	D	–
69	84	TVDD2	–	–	–	–
70	85	TREF	–	–	–	–
66	81	RVDD2	–	–	–	–
67	82	RREF	–	–	–	–
SB1 input data			L	H	L	H
SB2 input data			H	L	L	H

Note: * : LS is strapped to PCONT with a high-resistance.
Z : High impedance
D : $V_{DD}/2$ level
H : V_{DD} level
L : Ground level
– : Normal signal output

RECOMMENDED OPERATING CONDITIONS

(GND = 0V)

Parameter		Symbol	Pin name	Value			Unit
				Min.	Typ.	Max.	
Supply voltage		V_{DD}	V_{DD}	4.5	5.0	5.5	V
Input voltage		V_I	All input pins	0.0	–	V_{DD}	V
Analog section	Output load resistance 1	R_{LA1}	TVDD2, RVDD2,VREF, LS, PCONT, EXP1, AFOUT, TX	10	–	–	kΩ
	Output load resistance 2	R_{LA2}	AMP1O, AMP3O, AMP6O, C1, C2, RE1, RE3, RR1, RR3, AMP8O, LOMO, VR2O, VR1O	30	–	–	kΩ
	Output load capacitance 1	C_{L1}	TVDD2, RVDD2	–	–	100.0	pF
	Output load capacitance 2	C_{L2}	TREF, RREF	–	1.0	–	μF
	Output load capacitance 3	C_{L3}	TX, LS, VREF, PCONT, DTMF2, AMP3O, AMP6O	–	–	30.0	pF
Operating temperature		T_A	–	–30	–	70	°C

DC CHARACTERISTICS

(V_{DD} = 4.5 to 5.5V, T_A = –30 to +70°C, 0dBV = 1.0Vrms)

Parameter		Symbol	Pin name	Condition	Value			Unit
					Min.	Typ.	Max.	
Supply current 1		I_{DD1}	V_{DD}	SB1="L", SB2="H"	–	6.1	10.5	mA
Supply current 2		I_{DD2}	V_{DD}	SB1="H", SB2="L"	–	4.9	8.4	mA
Supply current 3		I_{DD3}	V_{DD}	SB1="L", SB2="L"	–	2.9	5.0	mA
Supply current 4		I_{DD4}	V_{DD}	SB1="H", SB2="H"	–	16.0	28.0	mA
Digital section	Low level input voltage	V_{IL}	FRQC, FCLK, DTMFTS, WBDS, SATS, DATA, CLK, $\overline{\text{RESET}}$, STB1, STB2, STB3, RAM, DTMFSS, BYPS, TAM, MODE	–	0.0	–	$V_{DD} \times 0.3$	V
	High level input voltage	V_{IH}	FRQC, FCLK, DTMFTS, WBDS, SATS, DATA, CLK, $\overline{\text{RESET}}$, STB1, STB2, STB3, RAM, DTMFSS, BYPS, TAM, MODE	–	$V_{DD} \times 0.7$	–	V_{DD}	V
	Low level input current	I_{IL}	FRQC, FCLK, DTMFTS, WBDS, SATS, DATA, CLK, $\overline{\text{RESET}}$, STB1, STB2, STB3, RAM, DTMFSS, BYPS, TAM, MODE	V_I = GND	–10	–	10	µA
	High level input current	I_{IH}	FRQC, FCLK, DTMFTS, WBDS, SATS, DATA, CLK, $\overline{\text{RESET}}$, STB1, STB2, STB3, RAM, DTMFSS, BYPS, TAM, MODE	$V_I = V_{DD}$	–10	–	10	µA
	Low level output voltage	V_{OL}	RWBD, RSAT	I_{OL} = 2.0mA	0.0	–	0.4	V
	High level output voltage	V_{OH}	RWBD, RSAT	I_{OL} = –0.1mA	4.0	–	V_{DD}	V
				I_{oI} = –1.0mA	2.4	–	V_{DD}	

DC CHARACTERISTICS

(V_{DD} = 4.5 to 5.5V, T_A = –30 to +70°C, 0dBV = 1.0Vrms)

Parameter		Symbol	Pin name	Condition	Value			Unit
					Min.	Typ.	Max.	
Analog section	Input voltage range	V_{IA}	AFINN, AFIN1, AFIN2, AMP3I, WBDI, TSAT, DEM, DISC, R1, R2, RE2, PDET, RR2, EXP2, AMP8I, LIMI, AMP2I	–	$^{1}/_{5}V_{DD}$	–	$^{4}/_{5}V_{DD}$	V
	Input resistance 1	R_{AIN1}	AFINN, AFIN1, AFIN2, AMP3I, TSAT, DEM, DISC, R1, R2, RE2, RR2, AMP8I, LIMI, AMP2I	Between input pin and $V_{DD}/2$	200	–	–	kΩ
	Input resistance 2	R_{AIN2}	WBDI, DAREF, ATT, PDET, EXP2	Between input pin and $V_{DD}/2$	30	–	–	kΩ
	Output voltage range	V_{OA}	AMP1O, AFINO, AMP3O, DTMF2, AMP6O, C1, C2, RE1, RE3, VREF, LS, PCONT, RR1, RR3, EXP1, AFOUT, AMP8O, TX, LIMO, VR2O, VR1O	–	1.5	–	3.5	V
	DAC output voltage range	V_{ODA}	VREF	DAC minimum output voltage	–	–	1.5	V
				DAC maximum output voltage DAS1, “H” level	3.5	–	–	
				DAC maximum output voltage DAS1, “L” level	1.75	–	–	
	Level shifter output voltage range	V_{OLS}	PCONT	–	1.5	–	3.5	V
	Limiter high level voltage	V_{DLH}	LIMO	Input level $V_{LIMI} = {}^{3}/_{4}V_{DD}$	$V_{DD}/2$ +0.050 × V_{DD}	$V_{DD}/2$ +0.053 × V_{DD}	$V_{DD}/2$ +0.056 × V_{DD}	V
	Limiter low level voltage	V_{DLL}	LIMO	Input level $V_{LIMI} = {}^{1}/_{4}V_{DD}$	$V_{DD}/2$ –0.056 × V_{DD}	$V_{DD}/2$ –0.053 × V_{DD}	$V_{DD}/2$ –0.050 × V_{DD}	V

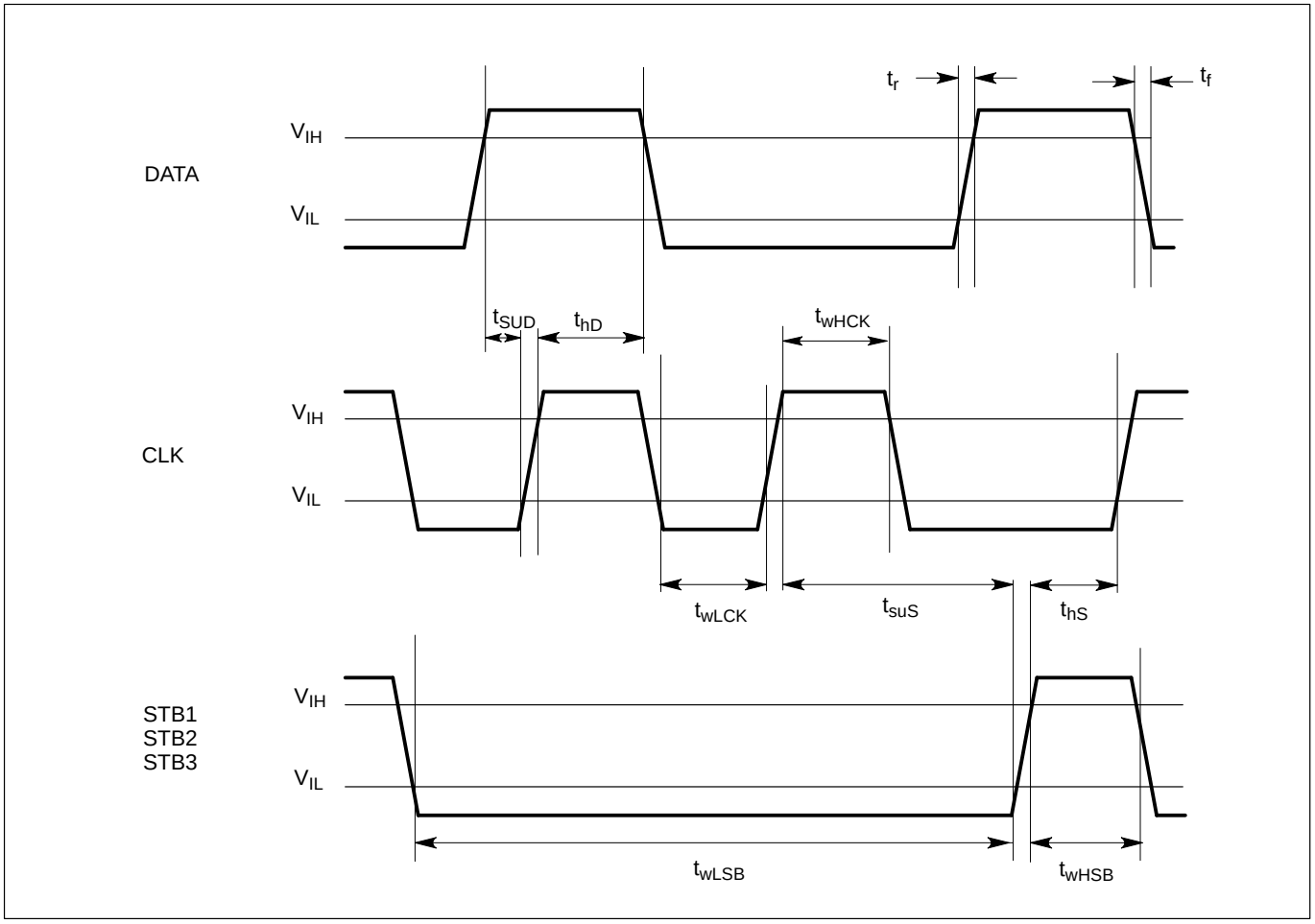
AC CHARACTERISTICS

(V_{DD} = 4.5 to 5.5V, T_A = –30 to +70°C, 0dBV = 1.0Vrms)

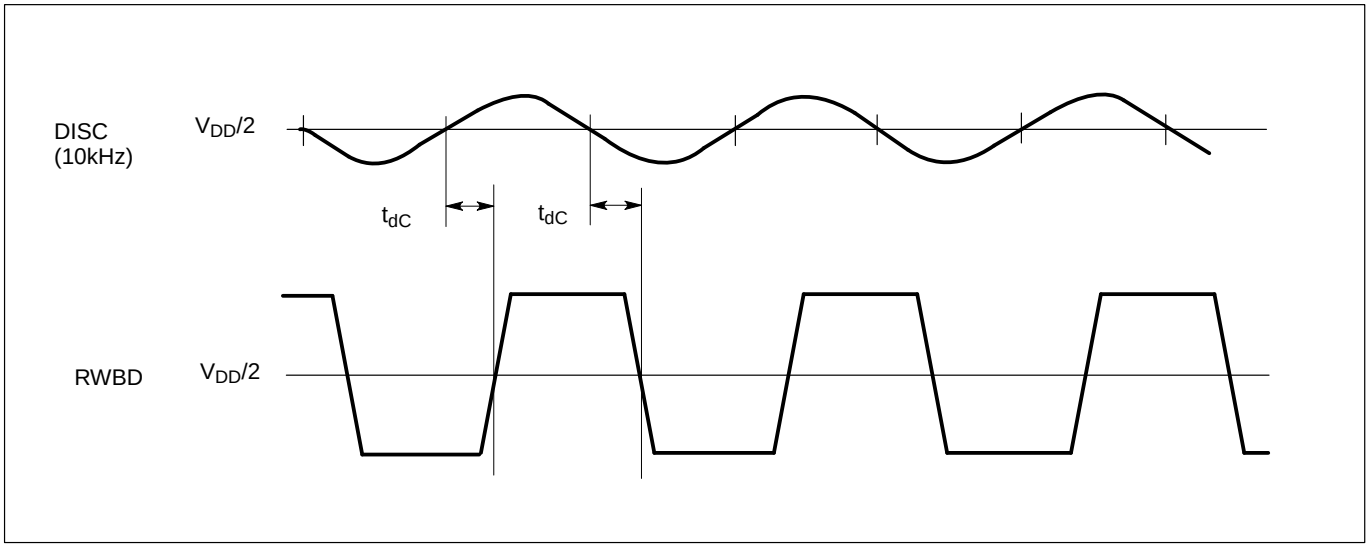
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min.	Typ.	Max.	
Clock duty cycle	D_{CLK}	FCLK	Rate of clock = “H” in a clock cycle	38	50	62	%
Clock High level time	t_{wHCK}	CLK	–	1.0	–	–	µs
Clock Low level time	t_{wLCK}	CLK	–	1.0	–	–	µs
Data setup time	t_{suD}	DATA, CLK	–	1.0	–	–	µs
Data hold time	t_{hD}	DATA, CLK	–	1.0	–	–	µs
High level strobe time	t_{wHSB}	STB1, STB2, STB3	–	1.0	–	–	µs
Low level strobe time	t_{wLSB}	STB1, STB2, STB3	–	1.0	–	–	µs
Strobe setup time	t_{suS}	STB1, STB2, STB3, CLK	–	1.0	–	–	µs
Strobe hold time	t_{hS}	STB1, STB2, STB3, CLK	–	1.0	–	–	µs
Rise time	t_r	STB1, STB2, STB3, FCLK, CLK, DATA	–	0	–	100	ns
Fall time	t_f	STB1, STB2, STB3, FCLK, CLK, DATA	–	0	–	100	ns
Comparator delay time	t_{dc}	DISC, RWBD	DISC input level = –17.2dBV at 10kHz	0	–	1.0	µs
RSAT duty cycle	D_{RSAT}	DISC, RSAT	DISC input level = –29.0dBV at 6kHz Time of RSAT=“H” level	75	83	91	µs

TIMING CHART

1. Interface



2. Comparator



TRANSMISSION CHARACTERISTICS

(V_{DD} = 5.0V ± 10%, T_A = –30 to +70°C, 0dBV = 1.0Vrms)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min.	Typ.	Max.	
Transmit gain 1	T_{G1}	WBDI-TX	Input level=–9.0dBV at 10kHz Electronic volume setting=0.0dB WBDS="H"	–1.0	0.0	1.0	dB
Transit gain 2	T_{G2}	TSAT-TX	Input level=–21.0dBV at 6kHz Electronic volume setting=0.0dB SATS="H"	–1.0	0.0	1.0	dB
Transmit gain 3	T_{G3}	AFINN-TX	Input level=–27.0dBV at 1kHz Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB TAM="L"	7.0	9.0	11.0	dB
Transmit muting level	T_{MUTE}	AFINN-TX	Input level=–27.0dBV at 1kHz Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB TAM="H" 0.05 to 3.0kHz direct detection	45.0	–	–	dB
Transmission S/N	$T_{S/N}$	AFINN-TX	Input level=–27.0dBV at 1kHz Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB TAM="L" Band: 0.05 to 20.0kHz	40.0	–	–	dB
Transmission signal-to-distortion	$T_{S/D}$	AFINN-TX	Input level=–27.0dBV at 1kHz Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB TAM="L" Band: 0.05 to 20.0kHz	–	–	–40.0	dB
Receive gain 1	R_{G1}	DEM-AFOUT	Input level=–26.0dBV at 1kHz Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB EXP1 strapped to EXP2 DTMFSS="L", RAM="L"	–1.0	0.0	1.0	dB
Receive muting level	R_{MUTE}	DEM-AFOUT	Input level=–18.0dBV at 1kHz Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB EXP1 strapped to EXP2 DTMFSS="L", RAM="H" 0.05 to 3.0kHz direct detection	45.0	–	–	dB
Receive S/N	$R_{S/N}$	DEM-AFOUT	Input level=–18.0dBV at 1kHz Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB EXP1 strapped to EXP2 DTMFSS="L", RAM="L" Band: 0.05 to 20.0kHz	45.0	–	–	dB
Receive signal-to-distortion	$R_{S/D}$	DEM-AFOUT	Input level=–18.0dBV at 1kHz Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB EXP1 strapped to EXP2 DTMFSS="L", RAM="L" Band: 0.05 to 20.0kHz	–	–	–40.0	dB

TRANSMISSION CHARACTERISTICS

(V_{DD} = 5.0V ± 10%, T_A = –30 to +70°C, 0dBV = 1.0Vrms)

Parameter		Symbol	Pin name	Condition		Value			Unit
						Min	Typ	Max	
Transmitter	Transmission frequency characteristic 1 (Attenuation characteristic)	T_{F1}	AFINN-TX	Input level=–27.0dBV at 1.0kHz reference Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB TAM="L"		See Figure 1			
	Transmission frequency characteristic 2 (Attenuation characteristic)	T_{F2}	TSAT-TX	Input level=–21.0dBV at 1.0kHz reference Electronic volume setting=0.0dB SATS="H" FRQC="H'	Less than 6.00kHz	–1.0	0.0	3.0	dB
					6.00 to 7.20kHz	–1.0	0.0	5.0	dB
					8.80 to 17.6kHz	3.0	–	–	dB
					17.6 to 60.0kHz	9.0	–	–	dB
					60.0kHz or more	35.0	–	–	dB
Receiver	Receive frequency characteristic 1 (Attenuation characteristic)	R_{F1}	DEM-AFOUT	Input level=–26.0dBV at 1.0kHz reference Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB Strapped between EXP1 and EXP2 DTMFSS="L", RAM="L"		See Figure 2			
	Receive frequency characteristic 1 (Attenuation characteristic)	R_{F2}	DISC-CI	Input level=–29.0dBV at 6kHz reference Electronic volume setting=0.0dB	Less than 5.4kHz	10.0	–	–	dB
					5.4 to 5.8kHz	3.0	–	–	dB
					5.87 to 5.97kHz	–1.0	–	4.5	dB
					5.97 to 6.03kHz	–1.0	–	2.0	dB
					6.03 to 6.13kHz	–1.0	–	4.5	dB
					6.20 to 6.60kHz	3.0	–	–	dB
					6.60kHz or more	9.0	–	–	dB

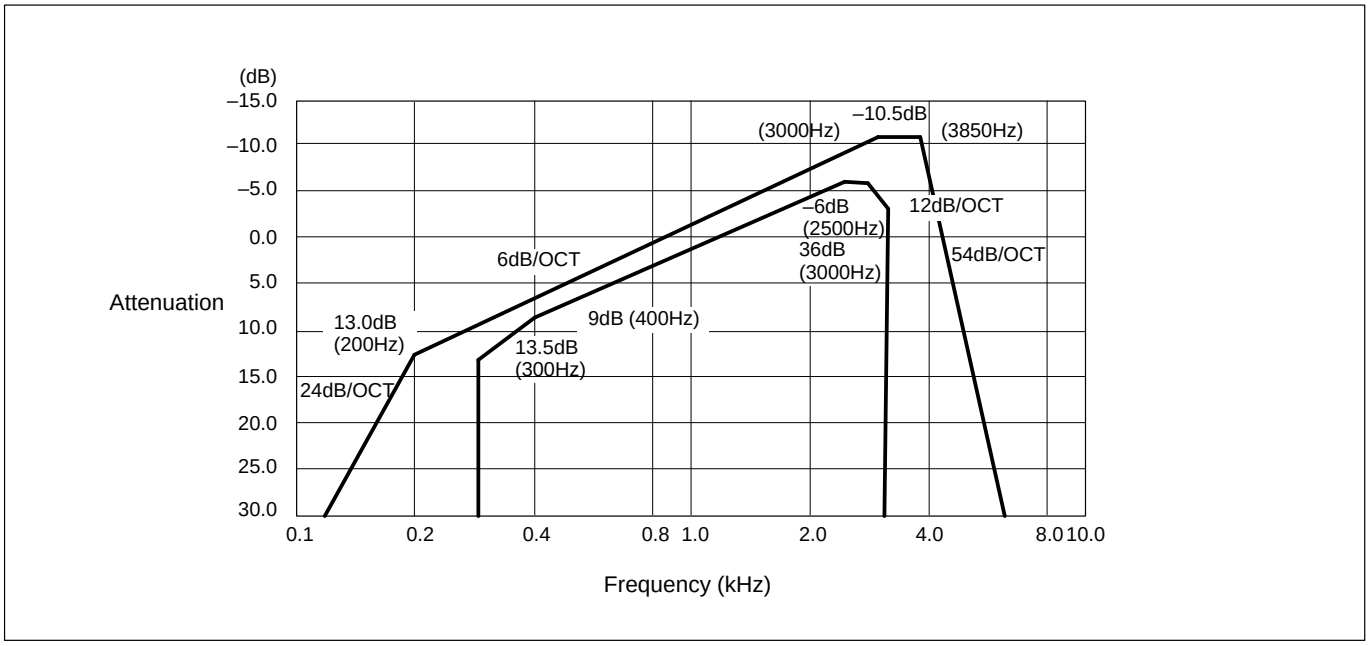


Figure 1. Transmitter Frequency Characteristic (AMPS/TACS)

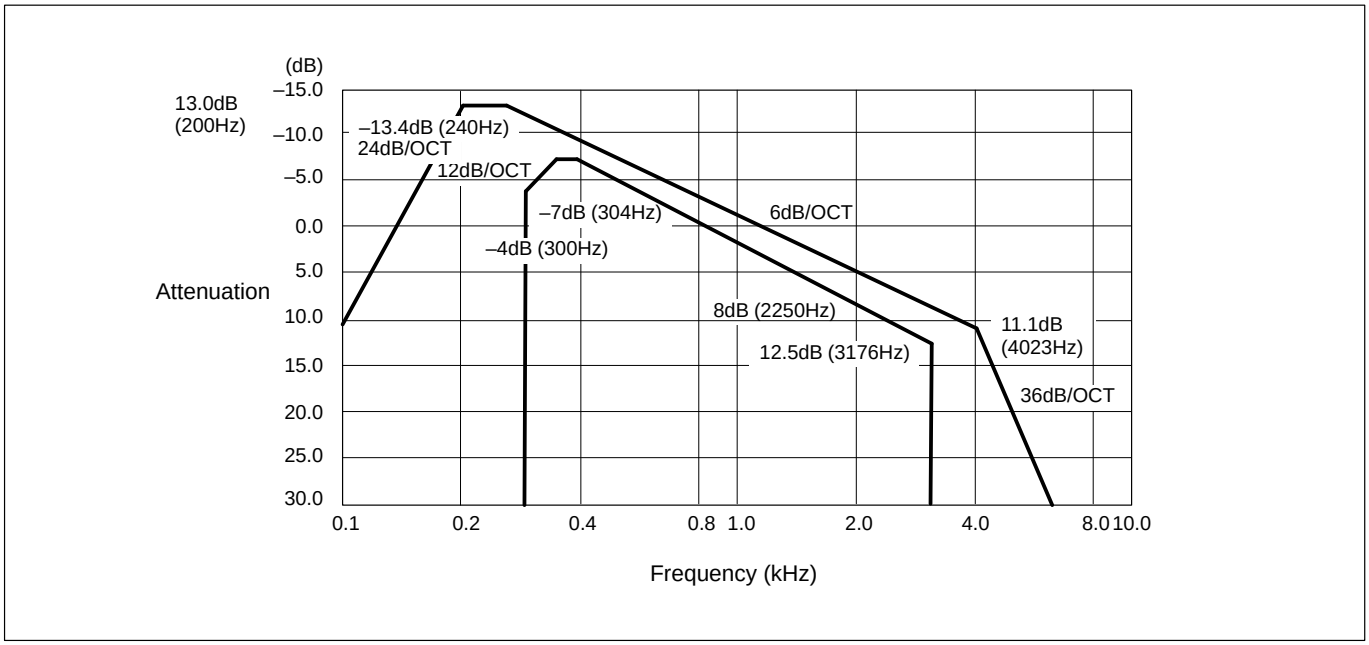


Figure 2. Receiver Frequency Characteristic (AMPS/TACS)

ELECTRONIC VOLUME AND DAC CHARACTERISTICS

(V_{DD} = 5.0V ± 10%, T_A = –30 to +70°C, 0dBV = 1.0Vrms)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Electronic volume minimum step width 1	V_{STP1}	VR9	0.1	0.2	0.3	dB
Electronic volume minimum step width 2	V_{STP2}	VR2, VR3, VR4, VR5, VR6	0.1	0.2	0.3	dB
Electronic volume minimum step width 3	V_{STP3}	VR7, VR8	0.5	1.0	1.5	dB
Electronic volume minimum step width 4	V_{STP4}	VR10	0.4	0.7	1.0	dB
Electronic volume maximum variable width 1	V_{RV1}	VR9	2.6	3.0	3.4	dB
Electronic volume maximum variable width 2	V_{RV2}	VR2, VR3, VR4, VR5, VR6	5.4	6.2	7.0	dB
Electronic volume maximum variable width 3	V_{RV3}	VR7, VR8	14.2	15.0	15.8	dB
Electronic volume maximum variable width 4	V_{RV4}	VR10	20.9	21.7	22.5	dB
DAC minimum step width 1	V_{DA1}	DAS1 = “H”	10.0	20.0	30.0	mV
DAC minimum step width 2	V_{DA2}	DAS1 = “L”	2.0	4.0	6.0	mV

DTMF OUTPUT FREQUENCY

(V_{DD} = 5.0V ± 10%, T_A = –30 to +70°C, 0dBV = 1.0Vrms)

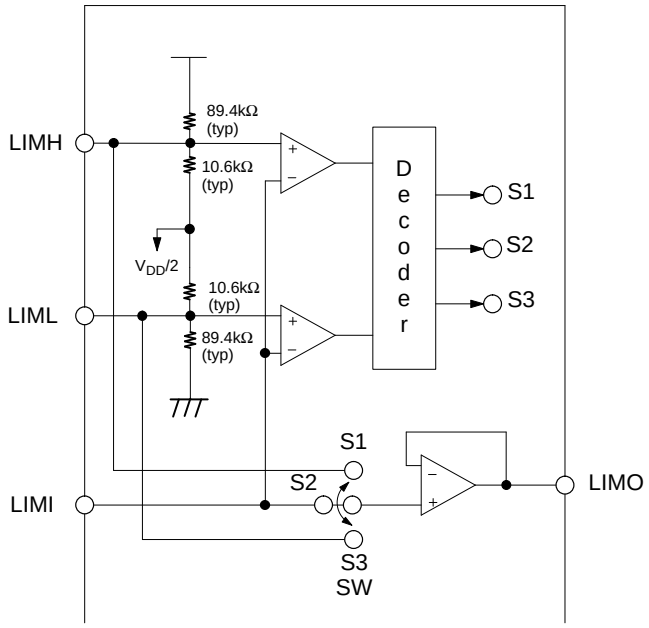
	Specified output frequency	Symbol	Actual output frequency	Error	Error standard	Note
High–group	1633Hz	FH1	1634.0Hz	+0.06%	±0.3%	FCLK=768kHz
	1477Hz	FH2	1476.9Hz	–0.1%		
	1336Hz	FH3	1338.0Hz	+0.15%		
	1209Hz	FH4	1207.5Hz	–0.13%		
	1150Hz	FH5	1149.7Hz	–0.03%		
Low–group	941Hz	FL1	941.2Hz	+0.02%		
	852Hz	FL2	853.3Hz	+0.16%		
	770Hz	FL3	769.5Hz	–0.06%		
	697Hz	FL4	698.2Hz	+0.17%		

DTMF CHARACTERISTICS

(V_{DD} = 5.0V ± 10%, T_A = –30 to +70°C, 0dBV = 1.0Vrms)

Parameter	Symbol	Pin name	Condition		Value			Unit
					Min	Typ	Max	
DTMF output level 1	A_{OT1}	DTMF2	1209Hz output	V_{DD} = 5.0V	–13.3	–12.3	–11.3	dBV
				V_{DD}=5.0V±10%	–14.3	–12.4	–10.3	
DTMF output level 2	A_{OT2}	TX	1209Hz output Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB DTMFTS="H"	V_{DD}=5.0V	–13.8	–12.3	–10.8	dBV
				V_{DD}=5.0V±10%	–14.8	–12.3	–9.8	
DTMF output level 3	A_{OT3}	AFOUT	1209Hz output Electronic volume setting=0.0dB AMP8 gain setting=–15.7dB DTMFSS="H"	V_{DD} = 5.0V	–29.0	–28.0	–27.0	dBV
				V_{DD}=5.0V±10%	–30.0	–28.0	–26.0	
Difference of level between high and low groups of DTMF1	D_{LH1}	DTMF2	High group level – low group level	FRQC="H"	–0.2	0.0	0.2	dB
				FRQC="L"	1.8	2.0	2.2	dB
Difference of level between high and low groups of DTMF2	D_{LH2}	TX	1633Hz level – 697Hz level Electronic volume setting=0.0dB Gain control amplifier setting=0.0dB DTMFTS="H", FRQC="H"		7.2	7.4	7.6	dB
DTMF distortion	T_{HN}	TX	Signal to noise ratio harmonic 697Hz output		23.0	–	–	dB

LIMITER CIRCUIT

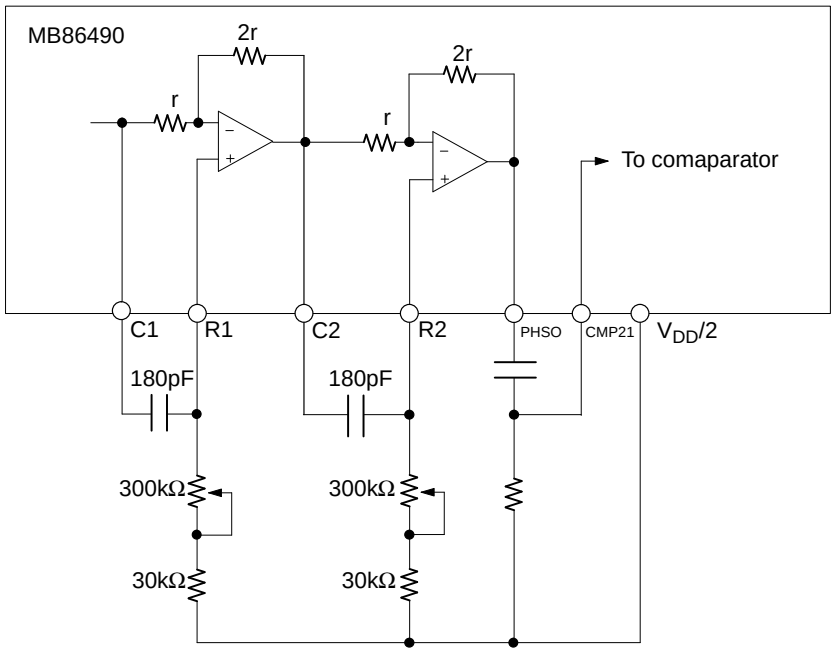


Input level	SW	LIMO output level
$V_{LIML} > V_{LIMI}$	S3	V_{DD}/2 –0.265V
$V_{LIML} \leq V_{LIMI} \leq V_{LIMH}$	S2	V_{LIMI} V
$V_{LIMH} < V_{LIMI}$	S1	V_{DD}/2 + 0.265V

V_{DD} = 5.0V (typical)

PHASE SHIFTER CIRCUIT

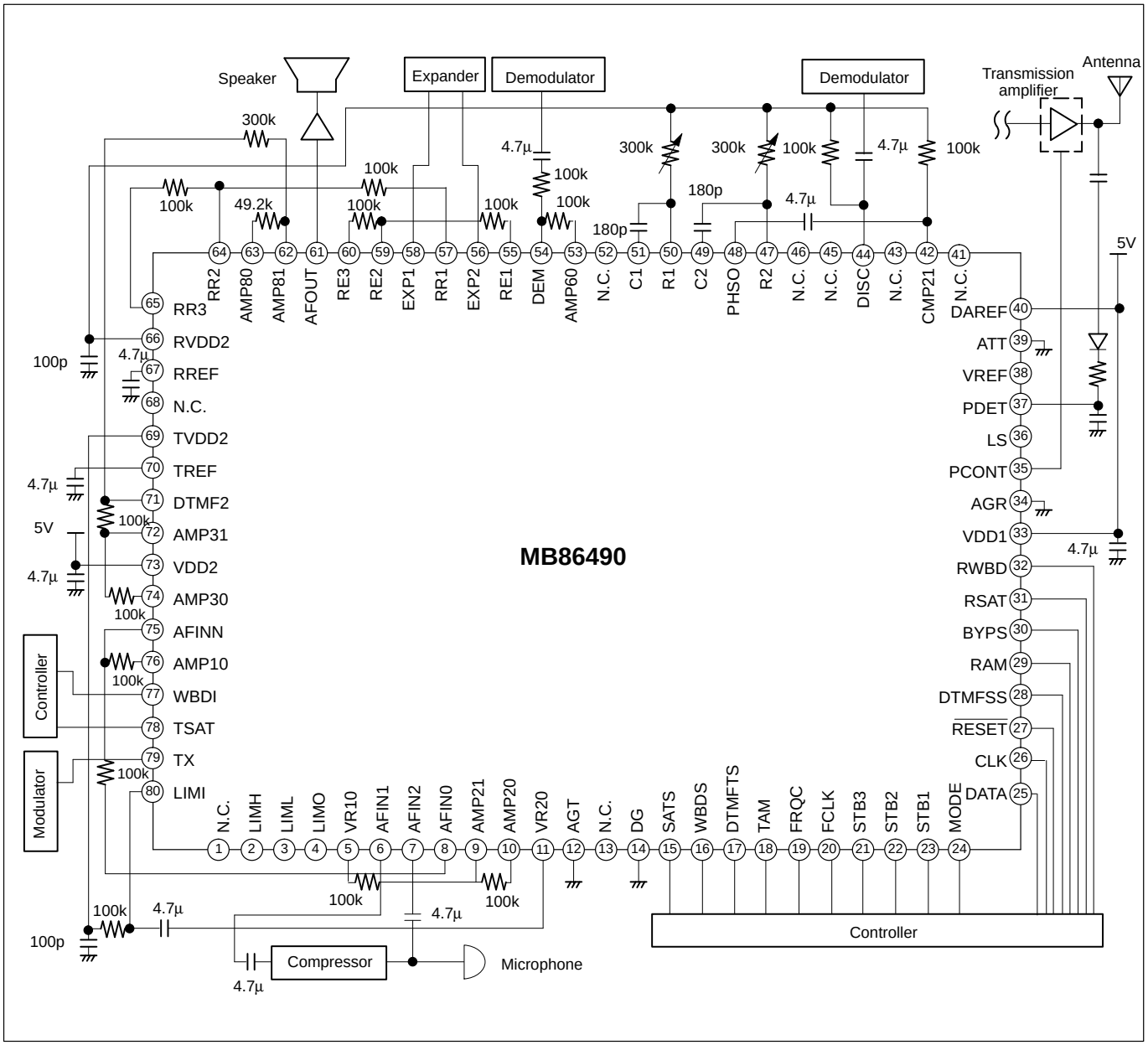
The phase shifter circuit uses an external controller to change the phase of a 6kHz ± 30Hz signal from 180 degrees.



The operational amplifier changes the signal phase from 0 to 90 degrees per step.
The combined resistance from R1 to $V_{DD}/2$ should be at least 30kΩ.

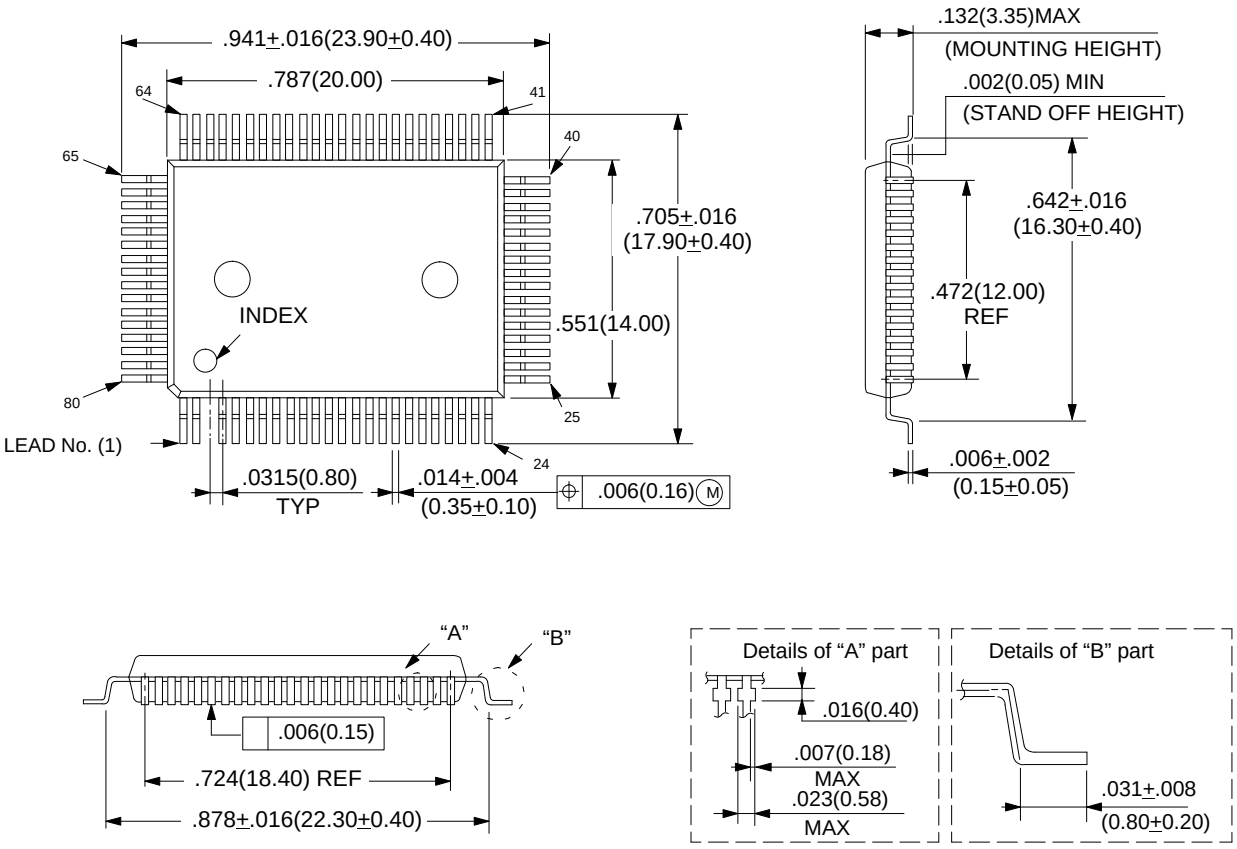
APPLICATION CIRCUIT

(For QFP80)



PACKAGE DIMENSIONS

80-LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT-80P-M01)



Dimensions in inches (millimeters).

PACKAGE DIMENSIONS (Continued)

100-LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT-100P-M05)