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FUJITSU

DATA SHEET

MB86604A

SCSI–II PROTOCOL CONTROLLER WITH SINGLE–ENDED DRIVER/RECEIVER

DESCRIPTION

The Fujitsu MB86604A is a single–ended transmission type SCSI–II Protocol Controller (SPC) with a single–ended driver/receiver. The MB86604A facilitates interface control between small/medium host computer and peripheral devices (such as a hard disk and printer). The specifications conform to the SCSI–II Standard.

The MB86604A supports high–speed synchronous transfer, the MPU/DMA independent system data bus, and user programmable command set to enable configuration of high–performance systems.

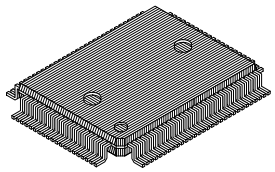
It also supports phase–to–phase sequence control function to reduce the program overhead of the host MPU.

The MB86604A incorporates single–ended type SCSI driver/receiver enableing the (48mA) device to be directly connected with the SCSI bus.

The device can operate with +5V single–power supply and in up to 40MHz clock frequency, is produced in a 100–pin plastic Quad Flat Package.

PRELIMINARY

MB86604A–PF



100–PIN PLASTIC QFP
(FPT–100P–M06)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- **SCSI Bus Interface:**
  - ° Conforming to the SCSI–II standard
  - ° Operatable as Initiator and target
  - ° Two types of high–speed data transfer:
    – Synchronous data transfer (Max. 10Mbytes/s, max. 32 offsets, 32–step transfer rate)
    – Asynchronous data transfer (Max. 5Mbytes/s)
  - ° Transfer parameters (transfer mode, transfer rate, transfer offset) can be set for up to 7 connected devices.
  - ° Single–ended transmission type (Maximum cable length : 6m) :
    – On–chip single–ended driver/receiver which can drive 48mA of ”L” level output current
    – Directly connectable with the SCSI bus
  - ° On–chip three–state bidirectional I/O buffers for SCSI pins except $\overline{RST}$, $\overline{BSY}$, and $\overline{SEL}$ pins ($\overline{DB7}$–$\overline{DB0}$, $\overline{DBP}$, $\overline{ATN}$, $\overline{MSG}$, $\overline{C/D}$, $\overline{I/O}$ pins can be selected from either three–state or open–drain buffer by controlling the TEST pins input.)
- **Transfer Operation:**
  - ° Automatic response to selection/reselection (Preset receiving operation can perform at the selection/reselection.) :
    – Initiator : Automatically operates until message received without command issue.
    – Target : Automatically operates until command received without command issue.
  - ° Automatic receiving :
    – Initiator : Automatically receives information for new phase to which target transited without command issue.
    – Target : Automatically receives message from initiator when initiator generates attention condition.
  - ° On–chip 32–byte data register (FIFO) for data phase

FEATURES (Continued)

- **Transfer Operation: (continued)**
  - On–chip two (send–only and receive–only) 32–byte data buffers for message, command, and status phases
  - On–chip 16–bit transfer block register and 24–bit transfer byte register enabling 1Tbytes transfer (1Tbytes : 16Mbytes x 64k blocks)
  - On–chip independent data transfer bus enabling the MPU operation during the data transfer
  - Parity through/generate can be specified.

- **System Bus Interface:**
  - 8–bit or 16–bit separate MPU and DMA bus
  - Directly connectable with a 80 series or 68 series MPU
  - Two types of transfer operation:
    – Program transfer
    – DMA transfer (Burst / Handshake)

- **Command Set:**
  - Supports sequential commands and programmable commands in addition to singular commands
  - Command queuing (Command can be continuously issued by putting tags to commands in command phase.)
  - On–chip 256–byte memory for command programming memory and command queuing buffer

- **Others**
  - Various effective operation modes to reduce the system overhead :
    – Auto ACK Reset Mode : automatically negates the last ACK signal during Initiator operation.
    – Level–2 Interrupt Disable Mode : does not generate the level–2 interrupts during User program operation.
    – Interrupt Disable Mode for Set/Reset : does not generate the interrupt for Set/Reset Commands
    – REQ Asserted Interrupt Disable Mode : does not generate the REQ Asserted Interrupt during Initiator operation.
    – Command Reject Interrupt Disable Mode : does not generate the Command Rejected Interrupt.
    – INT Signal Hold Mode : keeps to hold the INT signal while SPC holds the interrupt.
    – Command Rejection Mode : Does not accept the command while SPC holds the interrupt.
    – SPC Timeout Set Mode : specifies the SPC timeout after the SPC busy state until INT signal goes active state.

Figure 1. Pin Assignment

MB86604A
(Top View)

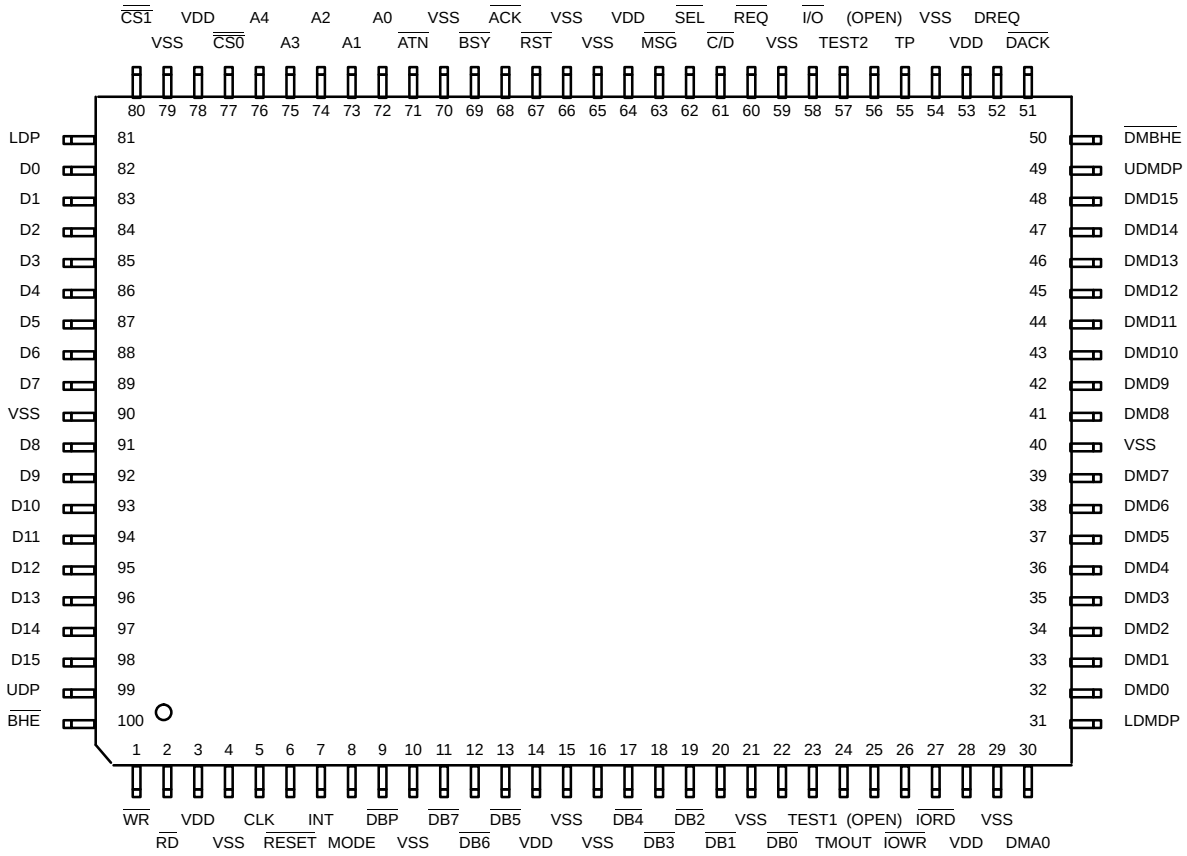
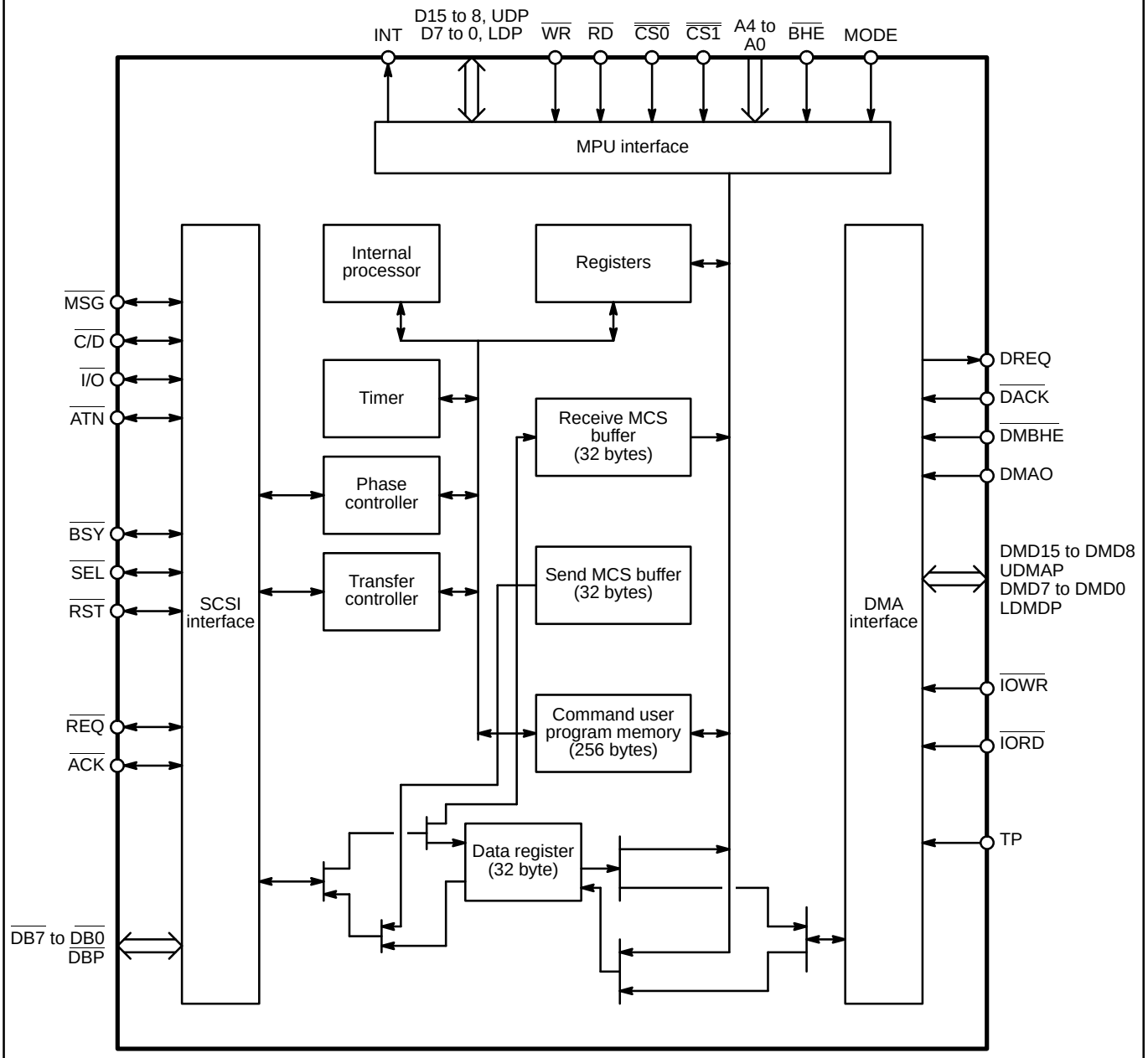


Figure 2. Block Diagram



PIN DESCRIPTION

Figure 1 and Table 1 show the pin assignment and pin description of the MB86604A.

Table 1. Pin Description

Symbol	Pin No.	Type	Name & Function
Power Supply			
V_{DD}	3,14,28,53,64, 78	–	+5V power supply pins.
V_{SS}	4,10,15,16,21, 29,40,54,59,65 ,66,70,79,90		Ground pins.
Clock			
CLK	5	I	Clock signal input pin. 20MHz, 30MHz, or 40MHz can be applied as the input clock frequency.
Reset & Test			
$\overline{RESET}$	6	I	System reset input pin. The input reset active pulse width must have 4 times of the clock cycle at least. This is an active–low pin.
TEST1	23	I	This pin is used to select the type of I/O buffer on SCSI pins. In case that $\overline{DBP}$, $\overline{DB7}$–$\overline{DB0}$ pins are used as an open–drain I/O, this pin is connected to Vss. In case of three–state I/O, connect to V_{DD}.
TEST2	57	I	This pin is used to select the type of I/O buffer on SCSI pins. In case that $\overline{MSG}$, $\overline{C/D}$, $\overline{I/O}$, and $\overline{ATN}$ pins are used as an open–drain I/O, this pin is connected to Vss. In case of three–state I/O, connect to V_{DD}.
SCSI Interface			
$\overline{REQ}$	60	I/O	Transfer request signal in the information transfer phases from target to initiator. The input signal to this pin is used for the timing control of data transfer sequence. This is a three–state I/O pin and an active low pin.
$\overline{ACK}$	68	I/O	This pin is for the acknowledge signal from initiator to target for the $\overline{REQ}$ signal in the information transfer phases. The input signal to this pin is used for the timing control of data transfer sequence. This is a three–state I/O pin and an active low pin.
$\overline{ATN}$	71	I/O	This pin is for the attention signal that initiator requests target for the message transfer phase. This is an active–low pin.
$\overline{MSG}$ *	63	I/O	This pin is for the message signal that specifies type of information transferred on the data bus. This is an active–low pin and becomes ”L” when message phase is specified.
$\overline{C/D}$ *	61	I/O	This pin is for the control/data signal that specifies type of information transferred on the data bus. This is an active–low pin and becomes ”L” level when command, status, or message phase is specified.
$\overline{I/O}$ *	58	I/O	This pin is for the input/output signal that specifies direction of information transferred on the data bus. This is an active–low pin. When this pin is ”L” level, the the information is transferred from target to initiator. When this pin is ”H” level, the information is transferred from initiator to target.
$\overline{BSY}$	69	I/O	This pin is for the SCSI bus busy signal. In the arbitration phase, this is for the request signal for the use of bus acquisition. This is an active–low pin.
$\overline{SEL}$	62	I/O	This pin is for the select signal used by initiator to select target during the selection phase and by target to reselect initiator during the reselection phase. This is an active–low pin.

* : Regarding the status of information transfer which is indicated by $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$ pins, See Table 2.

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name & Function
SCSI Interface			
$\overline{RST}$	67	I/O	This pin is for the reset signal used by any device on the bus. When the device is an input operation, the reset signal is input to this pin. When output operation, the reset signal is output from this pin. This is an active–low pin.
$\overline{DB7}$–$\overline{DB0}$	11,12,13,17,18,19,20,22	I/O	These pins are for the bidirectional 8–bit SCSI data bus and 1–bit odd parity line.
$\overline{DBP}$	9		
MPU Interface			
$\overline{CS0}$	77	I	This is a chip select 0 pin used by MPU to select the SPC as an I/O device. This is an active–low pin.
$\overline{CS1}$	80	I	This is a chip select 1 pin to select when MPU inputs/outputs the data on DMA bus through SPC. the . This is an active–low pin.
D15–D8	98,97,96,95,94,93,92,91	I/O	These pins are for the upper byte and parity bit of MPU data bus. When the $\overline{CS0}$ input is valid, these pins serve as I/O ports for the SPC internal registers. When the $\overline{CS1}$ input is valid, these pins serve as I/O ports for the DMA bus data.
UDP	99		
D7–D0	89,88,87,86,85,84,83,82	I/O	These pins are for the lower byte and parity bit of the MPU data bus. When the $\overline{CS0}$ input is valid, these pins serve as I/O ports for the SPC internal registers. When the $\overline{CS1}$ input is valid, these pins serve as I/O ports for the DMA bus data.
LDP	81		
A4–A0	76,75,74,73,72	I	These are address input pins to select the SPC internal registers.
$\overline{RD}$ (R/$\overline{W}$)	2	I	In the 80–series mode, this is a read signal input pin ($\overline{IORD}$ or $\overline{RD}$) that MPU reads the SPC. This read signal pin is an active–low. In the 68–series mode, this pin functions as the control signal input (R/$\overline{W}$) to control the read/write operation to the SPC. In the read operation, this pin is an active–high. In the write operation, this pin is an active–low.
$\overline{WR}$ (LDS)	1	I	In the 80–series mode, this pin is a write signal input pin ($\overline{IOWR}$ or $\overline{WR}$) that MPU writes to the SPC. This write signal input pin is active–low. In the 68–series mode, this pin functions as the lower data strobe signal input ($\overline{LDS}$) that MPU outputs when the lower byte of data bus is valid. The $\overline{LDS}$ pin is an active–low.
$\overline{BHE}$ (UDS)	100	I	In the 80–series mode, this pin is used for input of the bus high enable signal ($\overline{BHE}$) output from the MPU when the upper byte of the data bus is vaild. The BHE pin is an active–low. In the 68–series mode, this pin functions as the upper data strobe signal input pin (UDS) output from the MPU when the upper byte of the data bus is valid. The $\overline{UDS}$ pin is also an active–low.
$\overline{INT}$ (INT)	7	O	The INT and $\overline{INT}$ pins are the interrupt request signal output. The INT pins is used for the 80–series mode (an active–high pin), and the $\overline{INT}$ signal is used for the 68–series mode (an active–low pin).
MODE	8	I	This input pin is used to select the type of the MPU and DMA buses. In the 80–series mode, a high level is input. In the 68–series mode, a low level is input.

Note : The R/$\overline{W}$, $\overline{LDS}$, $\overline{UDS}$, and $\overline{INT}$ pins represented in a parenthesis are valid when the MODE pin =”L”.

Table 1. Pin Description (Continued)

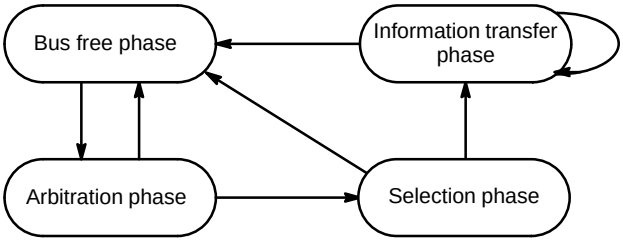
Symbol	Pin No.	Type	Name & Function
DMA Interface			
DREQ	52	O	This is an output pin of DMA transfer request signal to the DMA controller. The data transfer between the SPC and memeory via the DMA bus is requested. This pin is an active–high.
$\overline{\text{DACK}}$	51	I	This is a DMA acknowledge signal input pin output from the DMA controller that enables the DMA transfer. This pin is an active–low. When this pin is an active state, the DMA cycle (read/write) is valid.
DMD15–DMD8	48,47,46,45,44,43,42,41	I/O	These pins are the input/output pins of the upper byte and parity bit of the DMA data bus. When the signal input to the $\overline{\text{CS1}}$ pin (pin 80) is valid, these pins are connected directly to the MPU data bus.
UDMDP	49		
DMD7–DMD0	39,38,37,36,35,34,33,32	I/O	These pins are the input/output pins of the lower byte and parity bit of the DMA data bus. When the $\overline{\text{CS1}}$ (pin 80) input is valid, these pins are connected directly to the MPU data bus.
LDMDP	31		
$\overline{\text{IORD}}$ (DMR/$\overline{\text{W}}$)	27	I	In the 80–series mode, this pin ($\overline{\text{IORD}}$ or $\overline{\text{RD}}$) is used for the input pin to output the data from the SPC to the DMA bus. This is an active–low pin. in the 68–series mode, this pin functions as a control signal input pin (DMR/$\overline{\text{W}}$) to input/output the data to the SPC by the DMA controller. In the output operation, this pin is on the high–state (active–high state). In the input operation, this pin is on the low–state (active–low state).
$\overline{\text{IOWR}}$ ($\overline{\text{DMLDS}}$)	26	I	In the 80–series mode, this ($\overline{\text{IOWR}}$ or $\overline{\text{WR}}$) is used for the input pin to input the the DMA bus data to the SPC. In the 68–series mode, this pin functions as a DMA lower data strobe input ($\overline{\text{DMLDS}}$) that DMA controller outputs when the lower byte of the DMA bus data is valid. Both $\overline{\text{IOWR}}$ and $\overline{\text{DMLDS}}$ pins are an active–low.
$\overline{\text{DMBHE}}$ ($\overline{\text{DMUDS}}$)	50	I	In the 80–series mode, this pin is for the DMA bus high enable signal input pin ($\overline{\text{DMBHE}}$) output from the DMA controller when the upper byte of the DMA data bus is valid. This is an active–low pin. In the 68–series mode, this pin functions as the DMA upper data strobe signal input pin ($\overline{\text{DMUDS}}$) output from the DMA controller when the upper byte of data bus is valid. The $\overline{\text{DMUDS}}$ pin is also an active–low.
DMA0	30	I	In the 80–series mode, this pin is used for the DMA address 0 input pin output from the DMA controller. In the 68–series mode, a high level should be input to this pin.
TP	55	I	This is a DMA transfer permission signal input pin. When this pin is in active–state, the SPC does the DMA transfer. In case that this pin becomes inactive during the DMA transfer, the DMA transfer is paused on the block boundry. This pin is an active high.
Others			
TMOUT	24	O	This is a SCSI Timeout pin that indicates the SPC has been busy longer than the specified time. A high level is output on this pin if the SPC busy time exceeds the specified time.
(OPEN)	25, 26	—	These are open pins. Those pins are not connected with the device internally. Those pins must be left open.

Note : The DMR/$\overline{\text{W}}$, $\overline{\text{DMLDS}}$, and $\overline{\text{DMUDS}}$ pins represented in a parenthesis are valid when the MODE pin ="L".

BLOCK DESCRIPTION

1. INTERNAL PROCESSOR (Sequencer)

Performs sequence control between the various bus phases.



Information transfer phase :

- Command phase
- Data phase
- Status phase
- Message phase

2. TIMER

Manages the SCSI time standards.

Also, conducts the following time management.

- Time until the $\overline{REQ}$ or $\overline{ACK}$ signal is asserted for asynchronous transfer data
- Time until selection or reselection is retried
- $\overline{REQ}$ and $\overline{ACK}$ timeout time during transfers:

  Asynchronous transfer case

  Target: After the $\overline{REQ}$ is asserted, the time until the initiator asserts the $\overline{ACK}$
  Initiator: After the $\overline{ACK}$ is asserted, the time until the target negates the $\overline{REQ}$

  Synchronous transfer case

  Target: After the $\overline{REQ}$ is sent, the time until an $\overline{ACK}$ signal which makes the offset 0 is received from the initiator

- SPC Timeout

  Manages the SPC timeout indicating the SPC busy time longer than the specified time.

3. PHASE CONTROLLER

Controls the various phases executed by SCSI such as arbitration, selection/reselection, data in/out, command, status, and message in/out.

4. TRANSFER CONTROLLER

Controls the information (data, command, status, message) transfer phases executed by SCSI.

The following two types of transfer phases are used.

Asynchronous transfer: Controls interlock (response confirmation format) between the $\overline{REQ}$ and $\overline{ACK}$ signals.
Synchronous transfer: Controls a maximum 32-byte offset value for the data in or data out phases.

The following two modes exist for the data phase.

Program transfer: Uses data register (address 00/01) via the MPU interface.
DMA transfer: Uses DREQ and $\overline{DACK}$ signals via the DMA interface.

The transfer parameter setting values for synchronous transfers (Transfer Mode, transfer speed, transfer offset) can be stored by individual ID number and are automatically established when the data phase is initiated.

The number of transfer bytes is defined as block length × number of blocks.

5. REGISTER

The main registers are listed.

- Command register
  Command is specified by an 8-bit code.
  Specifies the program head address assigned to the user program memory for user program applications.
- Chip status register
  Shows the chip's operating state, nexus counterpart ID, and data register state.
- SCSI bus status register
  Shows the SCSI controller signal state.
- Interrupt status register
  Shows 8-bit code.
- Command step register
  Shows an 8-bit step code indicating the command execution state.
  Error analysis can be performed by referring to the information in this register and the interrupt status register.
- Group 6/7 command length setting register
  Sets the group 6/7 command length which is undefined by the SCSI standard.
  By setting the command length in this register, the SPC can determine the command length.

6. RECEIVE–MCS BUFFER

A receive only, 32-byte data buffer which stores data received via SCSI (message, command, status)

M: Message C: Command S: Status

7. SEND–MCS BUFFER

A send only, 32-byte data buffer which stores data sent via SCSI (message, command, status).

8. COMMAND USER PROGRAM MEMORY

Program memory used for establishing programmable commands (256 bytes).

9. DATA REGISTER

FIFO-type data register which stores data from SCSI executed data phases (32 bytes).

Table 2. Phase Status

Phase Name	Status of Signal			Direction of Transfer	
	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	Initiator	Target
DATA–OUT Phase	H	H	H	→	
DATA–IN Phase	H	H	L	←	
COMMAND Phase	H	L	H	→	
STATUS Phase	H	L	L	←	
MESSAGE–OUT Phase	L	L	H	→	
MESSAGE–IN Phase	L	L	L	←	

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note.)

Parameter	Symbol	Rating			Unit	Remarks
		Min	Typ	Max		
Supply Voltage	V_{DD}	Vss–0.5		Vss+6.0	V	Vss = 0 V
Input Voltage	V_I	Vss–0.5		V_{DD}+0.5	V	Vss = 0 V
Output Voltage	V_O	Vss–0.5		V_{DD}+0.5	V	Vss = 0 V
Operating Ambient Temperature	T_A	–25		+85	°C	
Storage Temperature	T_{STG}	–40		+125	°C	

Note : Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Supply Voltage	V_{DD}	V_{DD}	V_{SS}=0V	4.75	5.00	5.25	V
"H" Level Input Voltage	V_{IH}	CLK	V_{SS}=0V	3.5		–	V
		All pins except SCSI and CLK pins		2.2		–	
		SCSI pins		2.0		–	
"L" Level Input Voltage	V_{IL}	CLK	V_{SS}=0V	–		1.5	V
		All pins except SCSI and CLK pins		–		0.8	
		SCSI pins		–		0.8	
Operating Ambient Temperature	T_A			0	+25	+70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
"H" Level Input Voltage	V_{IH}	CLK	3.5		–	V	See Note 1 below.
		All pins except SCSI and CLK pins	2.2		–		
		SCSI pins	2.0		–		
"L" Level Input Voltage	V_{IL}	CLK	–		1.5	V	See Note 1 below.
		All pins except SCSI and CLK pins	–		0.8		
		SCSI pins	–		0.8		
Input Hysteresis of SCSI pins	V_{HW}	SCSI pins	0.2		–	V	See Note 1 below.
"H" Level Output Voltage	V_{OH}	All pins except SCSI pins	4.2		V_{DD}	V	I_{OH}=–2.0mA
		$\overline{REQ}$, $\overline{ACK}$ pins	2.5		–		I_{OH}=–8.0mA
"L" Level Output Voltage	V_{OL}	All pins except SCSI pins	V_{SS}		0.4	V	I_{OL}=+3.2mA, See Note 1 below.
		$\overline{REQ}$, $\overline{ACK}$ pins	–		0.5		I_{OL}=+48mA
		SCSI pins except $\overline{REQ}$ and $\overline{ACK}$ pins	–		0.5		I_{OL}=+48mA, See Note 1 below.
Leakage Current	I_{LI}	All pins except SCSI pins	–10		+10	µA	VI=0 to V_{DD} [V], See Note 2 below.
	I_{LZ}		–10		+10		
	I_{LI}	SCSI pins	–10		+10	µA	VI=0 to V_{DD} [V], See note 2 below.
	I_{LZ}		–10		+10		

Note 1 : SCSI pins are $\overline{DB7}$–$\overline{DB0}$, $\overline{DBP}$, $\overline{BSY}$, $\overline{SEL}$, $\overline{RST}$, $\overline{ATN}$, $\overline{REQ}$, $\overline{ACK}$, $\overline{MSG}$, $\overline{C/D}$, $\overline{I/O}$ pins.

Note 2 : Leakage current in the above spec indicates the following currents:
(1) Input current on the input pins.
(2) Leakage current at the high–Z state on the three–state output pins.
(3) Leakage current at the output high–Z state (input state) on the bidirectional bus pins.

AC CHARACTERISTICS

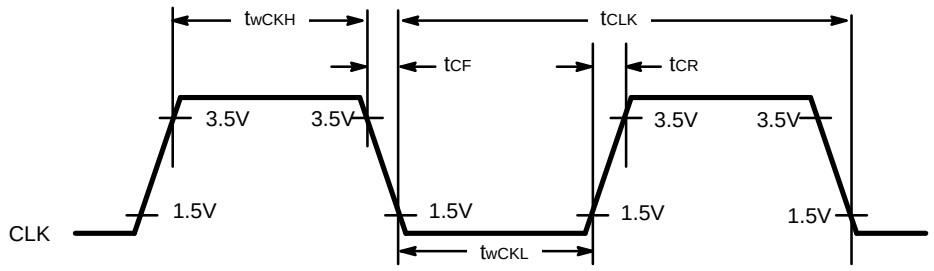
(Recommended operating conditions unless otherwise noted.)

System Clock

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock Cycle Time	t_{CLK}	25.0	–	50.0	ns	
Clock ”H” Pulse Width	t_{WCKH}	10.0	–	–	ns	See Note below.
Clock ”L” Pulse Width	t_{WCKL}	10.0	–	–	ns	See Note below.
Clock Rise Time	t_{CR}	–	–	10.0	ns	
Clock Fall Time	t_{CF}	–	–	10.0	ns	

Note In case that the internal clock frequency and the input clock frequency are the same (i.e. when using the divided–by–one mode), the clock pulse width (for ”H” and ”L”) must have at least 20 [ns] or longer. For example, when input clock frequency=20MHz and clock conversion register value is ”0Bh”.

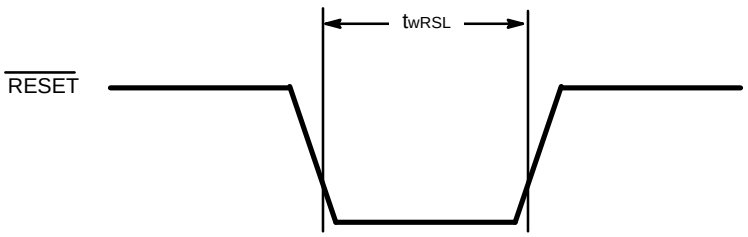
Figure 3. Clock Timing



System Reset

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
$\overline{\text{Reset}}$ ”L” Level Pulse Width	t_{WRSL}	$4t_{CLK}$	–	–	ns	

Figure 4. System Reset Timing

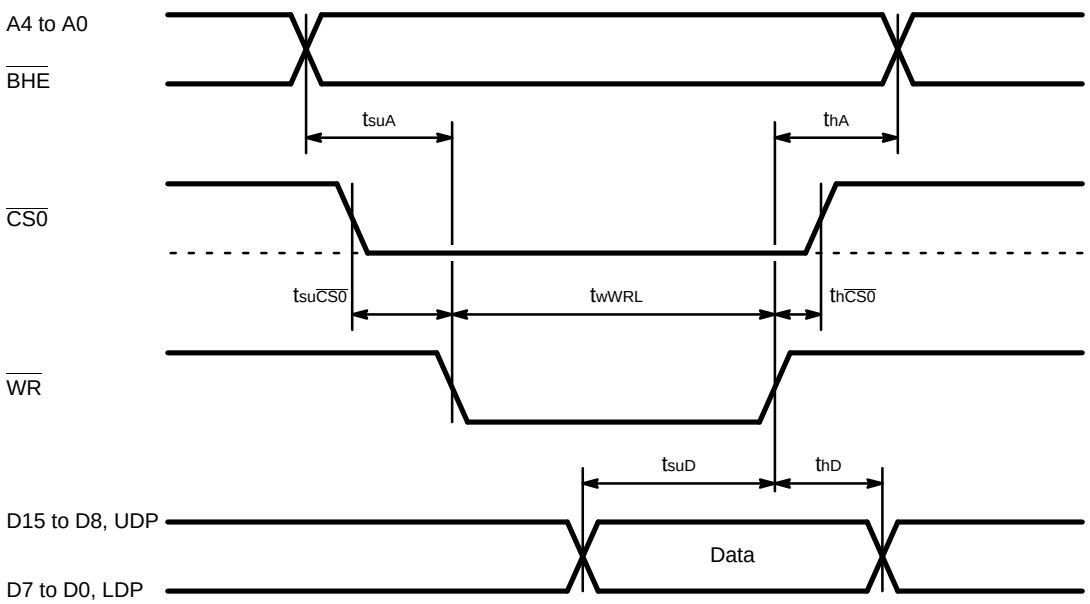


MPU Interface (80 series)

• Register write timing

Parameter	Base signal	Symbol	Value		Unit	
			Min.	Max.		
Address (A4 - A0) $\overline{BHE}$ set up time	$\overline{WR}$ L	t_{suA}	40	—	ns	
Address (A4 - A0) Hold time	$\overline{WR}$ H	t_{hA}	20	—	ns	
$\overline{CS0}$ set up time	$\overline{WR}$ L	$t_{su\overline{CS0}}$	20	—	ns	
$\overline{CS0}$ hold time	$\overline{WR}$ H	$t_{h\overline{CS0}}$	10	—	ns	
$\overline{WR}$ L level pulse width	—	t_{wWRL}	70	—	ns	
Data set up time	$\overline{WR}$ H	t_{suD}	40	—	ns	
Data hold time	$\overline{WR}$ H	t_{hD}	10	—	ns	

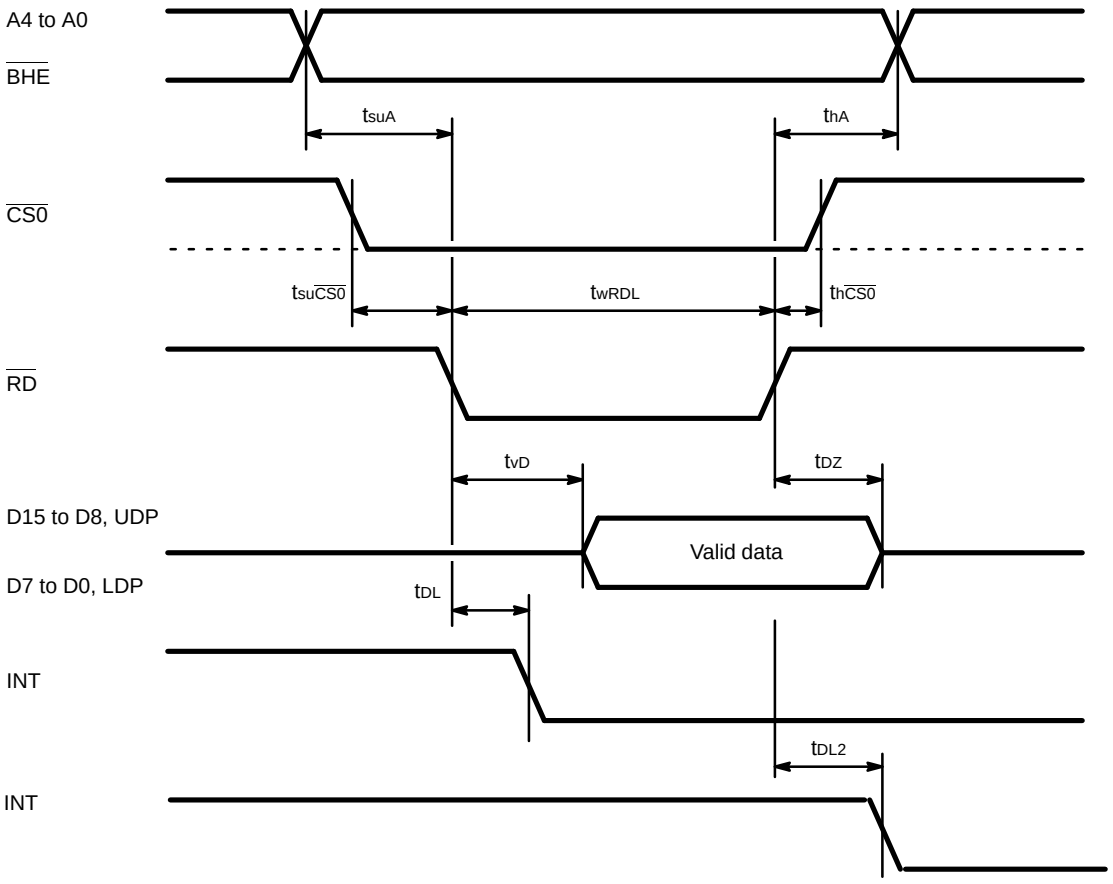
Figure 6. Register Write Timing



• Register read timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Address (A4 - A0) BHE set up time	$\overline{RD}$ L	t_{suA}	40	—	ns	
Address (A4 - A0) Hold time	$\overline{RD}$ H	t_{hA}	20	—	ns	
$\overline{CS0}$ set up time	$\overline{RD}$ L	$t_{su\overline{CS0}}$	20	—	ns	
$\overline{CS0}$ hold time	$\overline{RD}$ H	$t_{h\overline{CS0}}$	10	—	ns	
$\overline{RD}$ L level pulse width	—	t_{wRDL}	70	—	ns	
Data output confirmation time	$\overline{RD}$ L	t_{vD}	—	70	ns	
Data output disable time	$\overline{RD}$ H	t_{DZ}	10	—	ns	
INT signal clear time (1)	$\overline{RD}$ L	t_{DL}	—	50	ns	For INT Non–hold Mode
INT signal clear time (2)	$\overline{RD}$ H	t_{DL2}	—	n•tCLK+50	ns	For INT Hold Mode

Figure 7. Register Read Timing

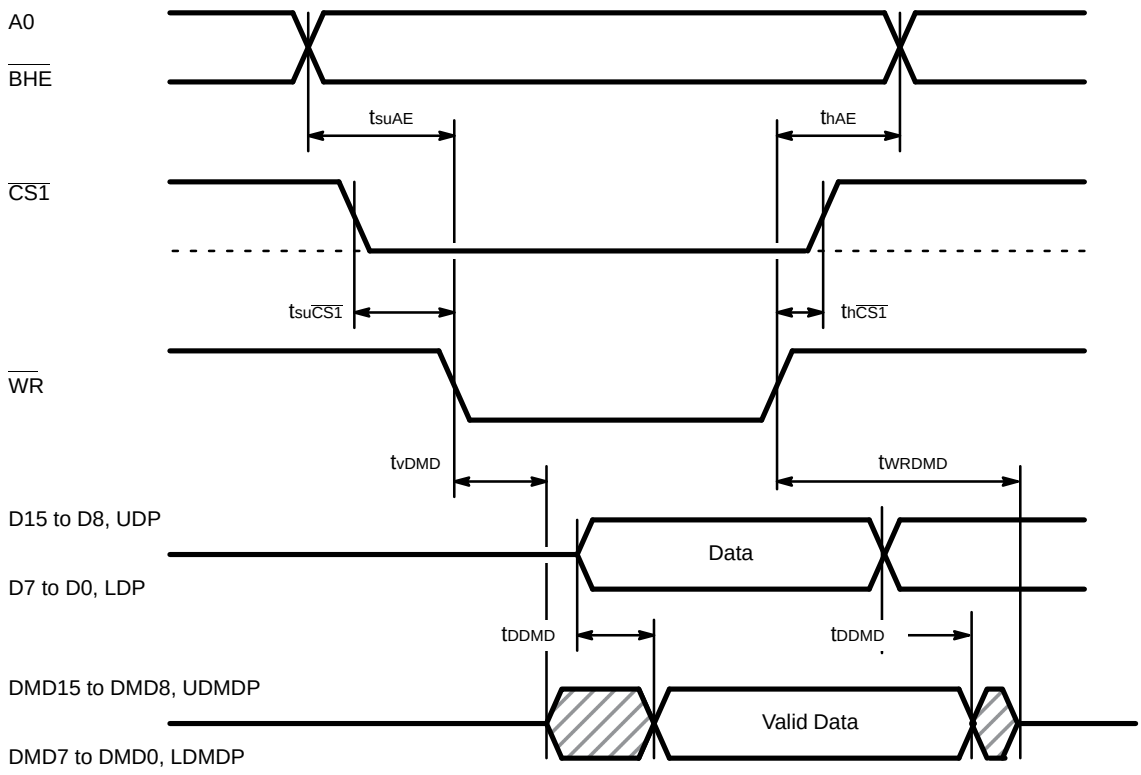


Notes : t_{DL2} is determined by a rising edge of the strobe signal which reads the stepcode for the last interrupt factor. Also, ”n” indicates the division ratio.

• Register write timing (for external access)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Address (A4 - A0) BHE set up time	WR L	t_{suAE}	40	—	ns	
Address (A4 - A0) BHE hold time4	WR H	t_{hAE}	20	—	ns	
CS1 set up time	WR L	$t_{su\overline{CS1}}$	20	—	ns	
CS1 hold time	WR H	$t_{h\overline{CS1}}$	10	—	ns	
DMA data bus output delay time	WR L	t_{vDMD}	—	70	ns	
DMA data bus output undefined time	WR H	t_{WRDMD}	10	—	ns	
MPU data → DMA data bus output delay time	—	t_{DDMD}	—	40	ns	

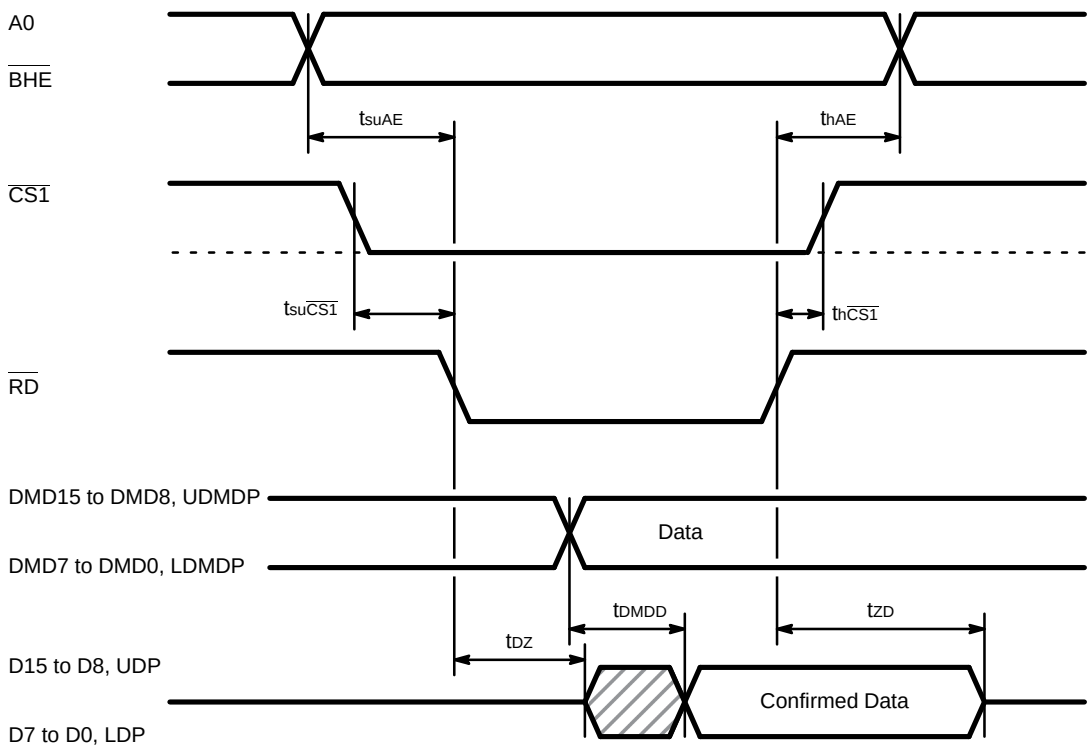
Figure 8. Register Write Timing (for External Access)



• Register read timing (for external access)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Address (A4 - A0) BHE set up time	$\overline{RD}$ L	t_{suAE}	40	—	ns	
Address (A4 - A0) BHE hold time	$\overline{RD}$ H	t_{hAE}	20	—	ns	
$\overline{CS1}$ set up time	$\overline{RD}$ L	$t_{su\overline{CS1}}$	20	—	ns	
$\overline{CS1}$ hold time	$\overline{RD}$ H	$t_{h\overline{CS1}}$	10	—	ns	
MPU data bus output enable time	$\overline{RD}$ L	t_{ZD}	—	70	ns	
MPU data bus output disable time	$\overline{RD}$ H	t_{DZ}	10	—	ns	
DMA data → MPU data bus output delay time	—	t_{DMDD}	—	40	ns	

Figure 9. Register Read Timing (for External Access)

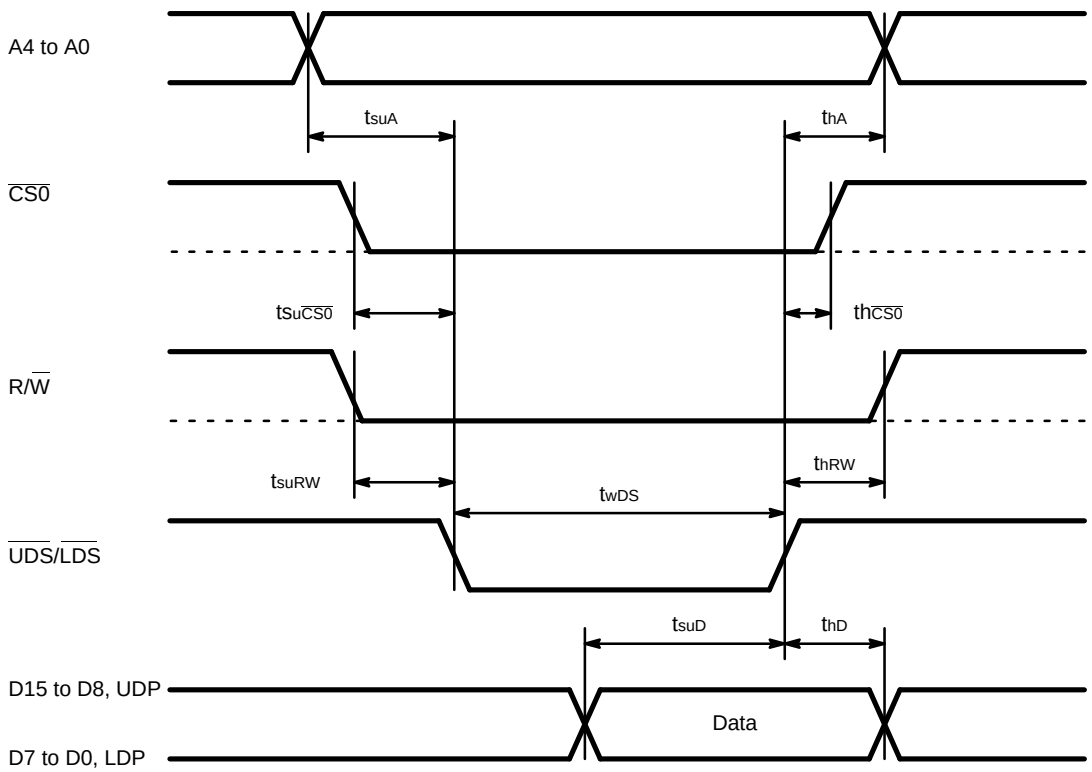


MPU Interface (68 series)

- Register write timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Address (A4 to A0) Set up time	$\overline{UDS}/\overline{LDS}$ L	t_{suA}	40	—	ns	
Address (A4 to A0) Hold time	$\overline{UDS}/\overline{LDS}$ H	t_{hA}	20	—	ns	
$\overline{CS0}$ set up time	$\overline{UDS}/\overline{LDS}$ L	$t_{su\overline{CS0}}$	20	—	ns	
$\overline{CS0}$ hold time	$\overline{UDS}/\overline{LDS}$ H	$t_{h\overline{CS0}}$	10	—	ns	
R/$\overline{W}$ set up time	$\overline{UDS}/\overline{LDS}$ L	t_{suRW}	20	—	ns	
R/$\overline{W}$ hold time	$\overline{UDS}/\overline{LDS}$ H	t_{hRW}	20	—	ns	
$\overline{UDS}/\overline{LDS}$ L level pulse width	—	t_{wDS}	70	—	ns	
Data set up time	$\overline{UDS}/\overline{LDS}$ H	t_{suD}	40	—	ns	
Data hold time	$\overline{UDS}/\overline{LDS}$ H	t_{hD}	10	—	ns	

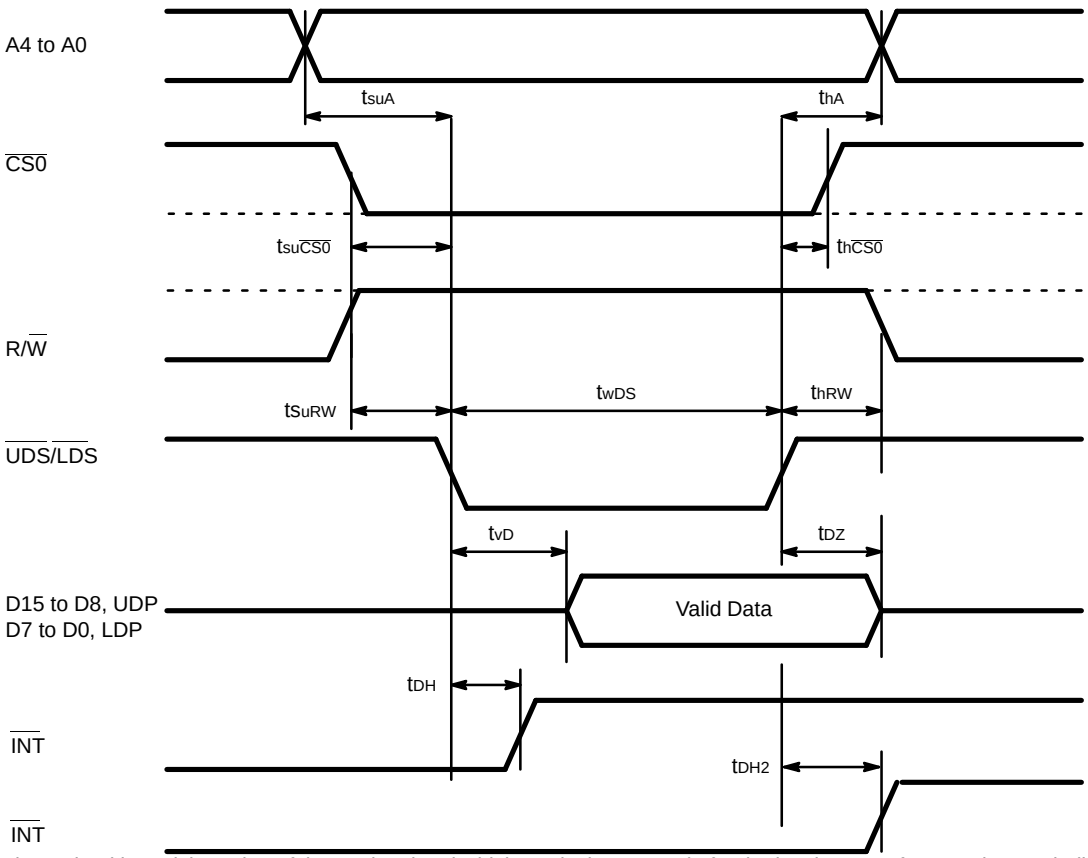
Figure 10. Register Write Timing



• Register read timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Address (A4 - A0) Set up time	$\overline{UDS}/\overline{LDS}$ L	t_{SuA}	40	—	ns	
Address (A4 - A0) Hold time	$\overline{UDS}/\overline{LDS}$ H	t_{hA}	20	—	ns	
$\overline{CS0}$ set up time	$\overline{UDS}/\overline{LDS}$ L	$t_{su\overline{CS0}}$	20	—	ns	
$\overline{CS0}$ hold time	$\overline{UDS}/\overline{LDS}$ H	$t_{h\overline{CS0}}$	10	—	ns	
R/$\overline{W}$ set up time	$\overline{UDS}/\overline{LDS}$ L	t_{suRW}	20	—	ns	
R/$\overline{W}$ hold time	$\overline{UDS}/\overline{LDS}$ H	t_{hRW}	20	—	ns	
$\overline{UDS}/\overline{LDS}$ L level pulse width	—	t_{wDS}	70	—	ns	
Data output confirmation time	$\overline{UDS}/\overline{LDS}$ L	t_{vD}	—	70	ns	
Data output disable time	$\overline{UDS}/\overline{LDS}$ H	t_{DZ}	10	—	ns	
$\overline{INT}$ signal clear time (1)	$\overline{UDS}/\overline{LDS}$ L	t_{DH}	—	50	ns	For INT Non–hold mode
$\overline{INT}$ signal clear time (2)	$\overline{UDS}/\overline{LDS}$ H	t_{DH2}	–	$n \bullet t_{CLK}+50$	ns	For INT Hold mode

Figure 11. Register Read Timing

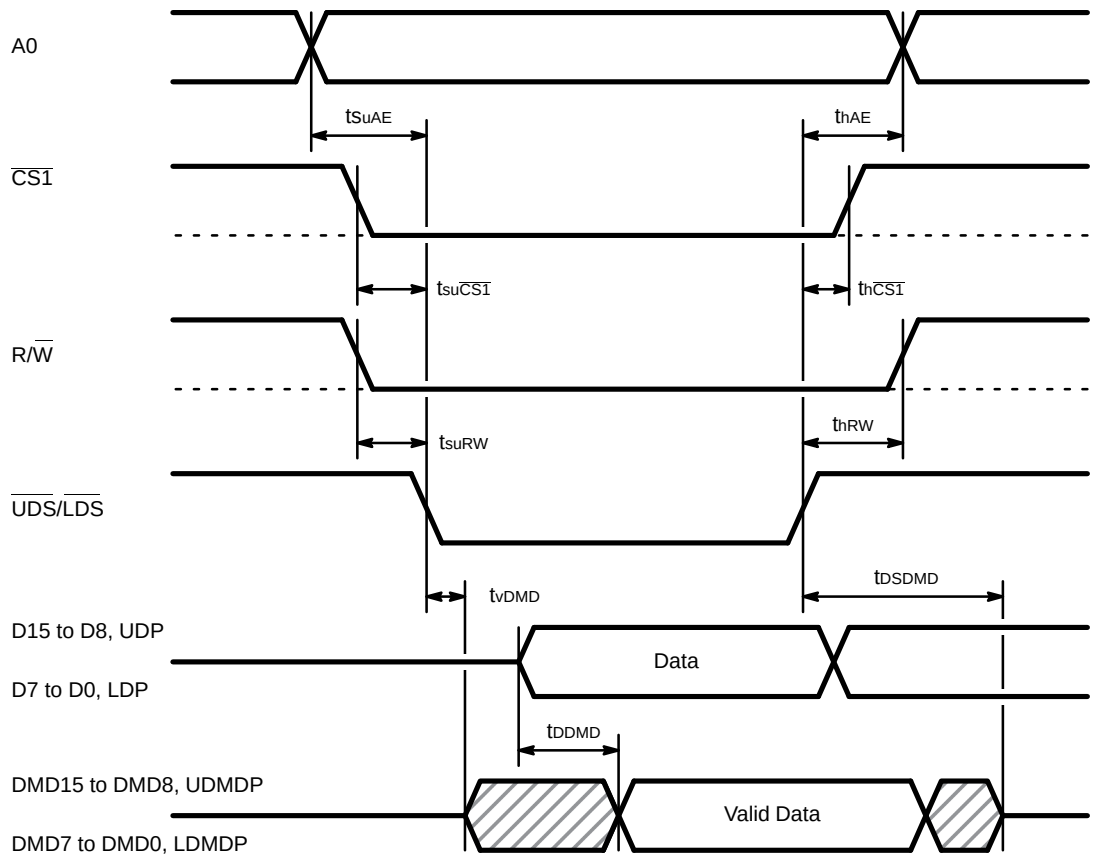


Notes : t_{DL2} is determined by a rising edge of the strobe signal which reads the stepcode for the last interrupt factor. Also, ”n” indicates the division ratio.

• Register write timing (for external access)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Address (A0) Set up time	$\overline{UDS}/\overline{LDS}$ L	t_{suAE}	40	—	ns	
Address (A0) Hold time	$\overline{UDS}/\overline{LDS}$ H	t_{hAE}	20	—	ns	
$\overline{CS1}$ set up time	$\overline{UDS}/\overline{LDS}$ L	$t_{su\overline{CS1}}$	20	—	ns	
$\overline{CS1}$ hold time	$\overline{UDS}/\overline{LDS}$ H	$t_{h\overline{CS1}}$	10	—	ns	
R/$\overline{W}$ set up time	$\overline{UDS}/\overline{LDS}$ L	t_{suRW}	20	—	ns	
R/$\overline{W}$ hold time	$\overline{UDS}/\overline{LDS}$ H	t_{hRW}	20	—	ns	
DMA data bus output delay time	$\overline{UDS}/\overline{LDS}$ L	t_{vDMD}	—	70	ns	
DMA data bus output undefined time	$\overline{UDS}/\overline{LDS}$ H	t_{DSDMD}	10	—	ns	
MPU data ⟶ DMA data bus output delay time	—	t_{DDMD}	—	40	ns	

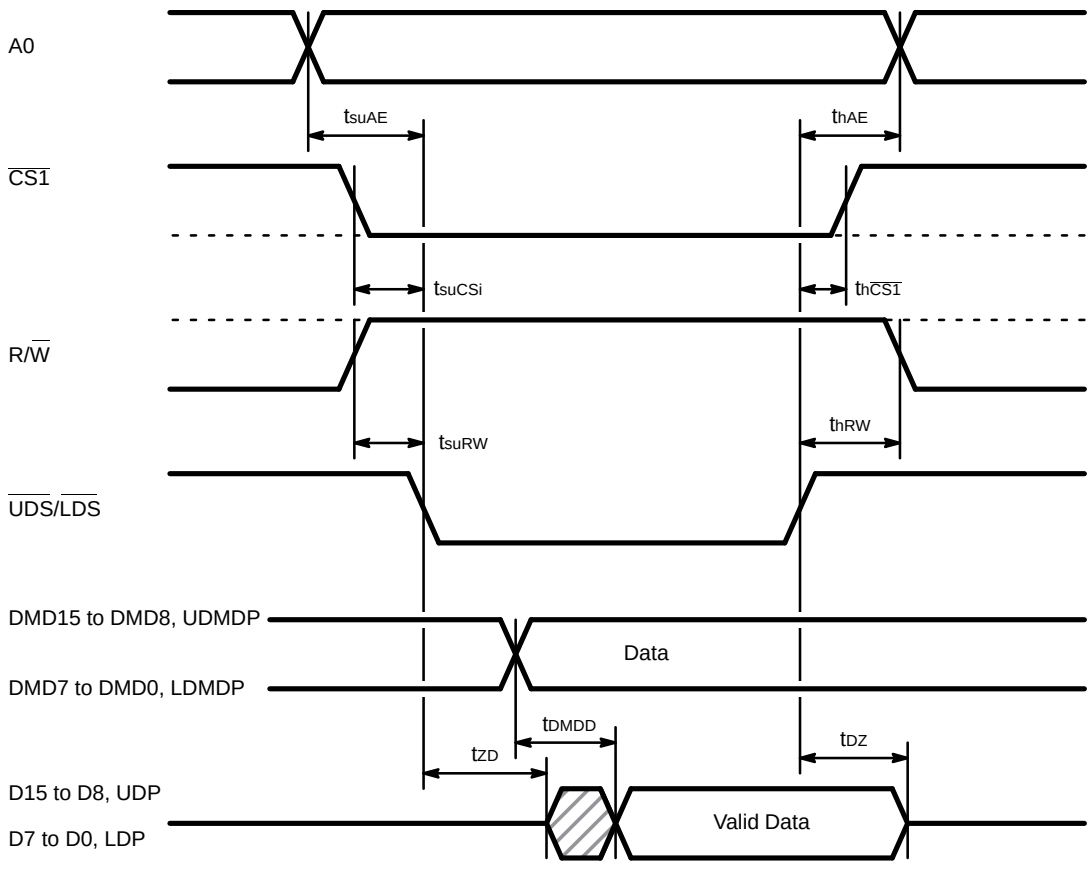
Figure 12. Register Write Timing (for External Access)



• Register read timing (for external access)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Address (A0) Set up time	$\overline{UDS}/\overline{LDS}$ L	t_{suAE}	40	—	ns	
Address (A0) Hold time	$\overline{UDS}/\overline{LDS}$ H	t_{hAE}	20	—	ns	
$\overline{CS1}$ set up time	$\overline{UDS}/\overline{LDS}$ L	$t_{su\overline{CS1}}$	20	—	ns	
$\overline{CS1}$ hold time	$\overline{UDS}/\overline{LDS}$ H	$t_{h\overline{CS1}}$	10	—	ns	
R/$\overline{W}$ set up time	$\overline{UDS}/\overline{LDS}$ L	t_{suRW}	20	—	ns	
R/$\overline{W}$ hold time	$\overline{UDS}/\overline{LDS}$ H	t_{hRW}	20	—	ns	
Data output enable time	$\overline{UDS}/\overline{LDS}$ L	t_{ZD}	—	70	ns	
Data output disable time	$\overline{UDS}/\overline{LDS}$ H	t_{DZ}	10	—	ns	
DMA data ⟶ MPU data bus output delay time	—	t_{DMDD}	—	40	ns	

Figure 13. Register Read Timing (for External Access)



DMA Interface

The DMA access timing described in this section is not applicable in the following cases.

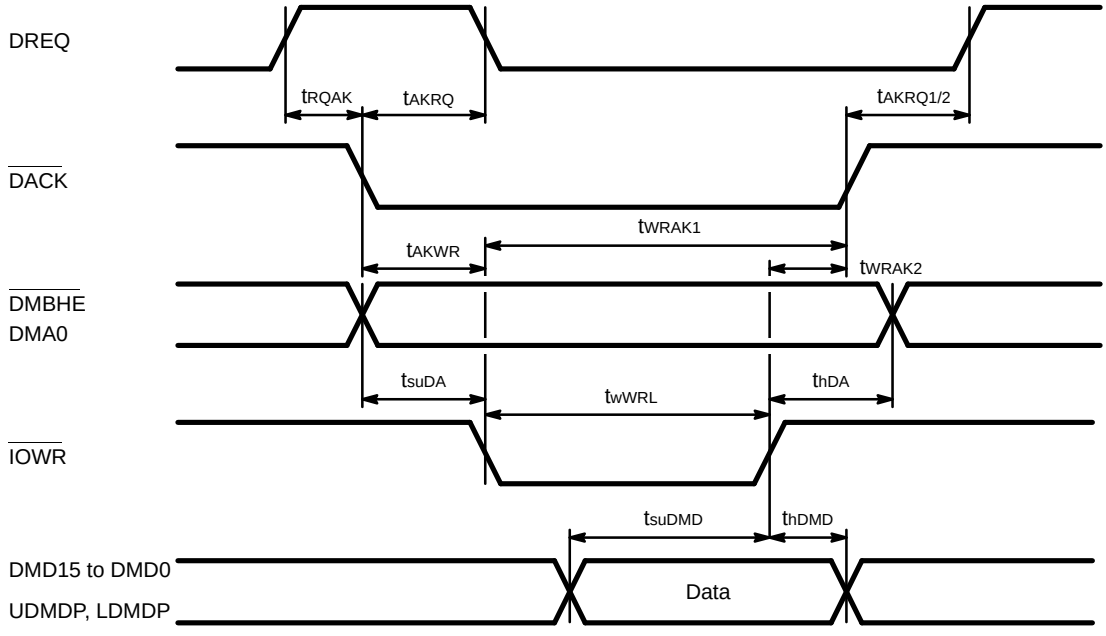
- During SCSI input, when the data buffer is EMPTY or when one byte is stored
- During SCSI output, when the data buffer is FULL or when 31 bytes are stored
- When a parity error is detected (target)
- When an error which interrupts the transfer occurs at the SCSI interface

[80 Series Handshake Mode]

- Write timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{DACK}$ L assert time	DREQ H	t_{RQAK}	0	—	ns	
DREQ L negate time	$\overline{DACK}$ L	t_{AKRQ}	—	40	ns	
DREQ H assert time (8 bit)	$\overline{DACK}$ H	t_{AKRQ1}	—	50	ns	
DREQ H assert time (16 bit)	$\overline{DACK}$ H	t_{AKRQ2}	—	2 tCLK +40	ns	
$\overline{IOWR}$ L assert time	$\overline{DACK}$ L	t_{AKWR}	0	—	ns	
$\overline{DMBHE}$, DMA0 set up time	$\overline{IOWR}$ L	t_{suDA}	20	—	ns	
$\overline{DMBHE}$, DMA0 hold time	$\overline{IOWR}$ H	t_{hDA}	20	—	ns	
$\overline{IOWR}$ L level pulse width	—	t_{wWRL}	40	—	ns	
$\overline{DACK}$ H negate time	$\overline{IOWR}$ L	t_{WRAK1}	1 tCLK	—	ns	
	$\overline{IOWR}$ H	t_{WRAK2}	0	—	ns	
Input data set up time	$\overline{IOWR}$ L	t_{suDMD}	30		ns	
Input data hold time	$\overline{IOWR}$ H	t_{hDMD}	5		ns	

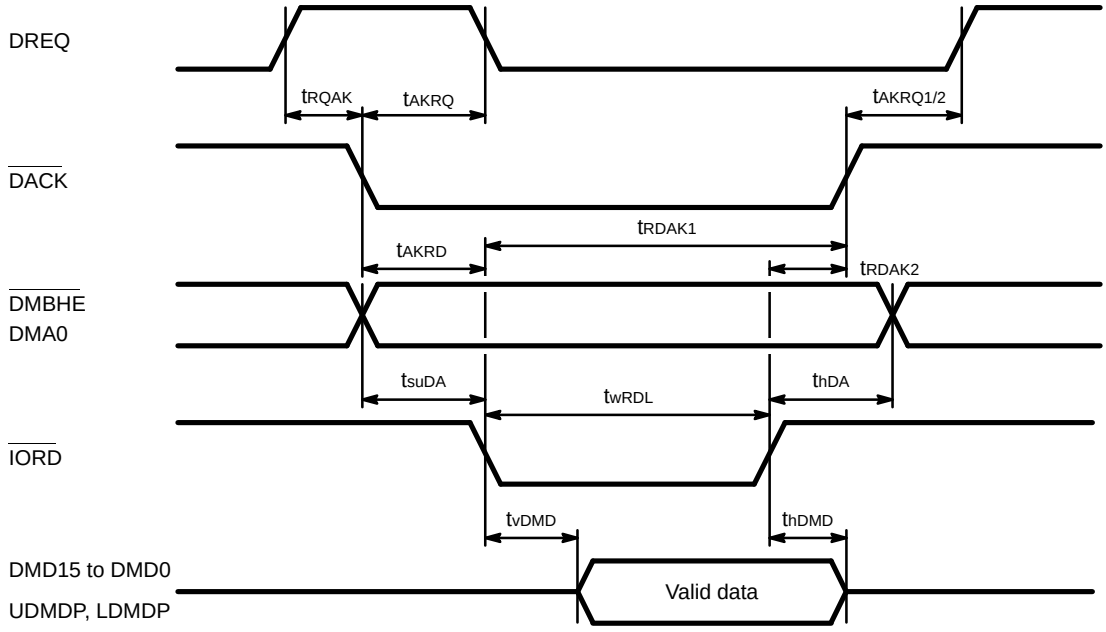
Figure 14. Register write timing



• Read timing

Parameter	Base signal	Symbol	Value Min.	Value Max.	Unit	Remarks
$\overline{\text{DACK}}$ L assert time	DREQ H	t_{RQAK}	0	—	ns	
DREQ L negate time	$\overline{\text{DACK}}$ L	t_{AKRQ}	—	40	ns	
DREQ H assert time (8 bit)	$\overline{\text{DACK}}$ H	t_{AKRQ1}	—	50	ns	
DREQ H assert time (16 bit)	$\overline{\text{DACK}}$ H	t_{AKRQ2}	—	2 tCLK +40	ns	
$\overline{\text{IORD}}$ L assert time	$\overline{\text{DACK}}$ L	t_{AKRD}	0	—	ns	
$\overline{\text{DMBHE}}$, DMA0 set up time	$\overline{\text{IORD}}$ L	t_{suDA}	20	—	ns	
$\overline{\text{DMBHE}}$, DMA0 hold time	$\overline{\text{IORD}}$ H	t_{hDA}	20	—	ns	
$\overline{\text{IORD}}$ L level pulse width	—	t_{wRDL}	40	—	ns	
$\overline{\text{DACK}}$ H negate time	$\overline{\text{IORD}}$ L	t_{RDAK1}	1 tCLK	—	ns	
	$\overline{\text{IORD}}$ H	t_{RDAK2}	0	—	ns	
Data output confirmation time	$\overline{\text{IORD}}$ L	t_{vDMD}	—	40	ns	
Data output hold time	$\overline{\text{IORD}}$ H	t_{hDMD}	10	—	ns	

Figure 15. Register Read Timing

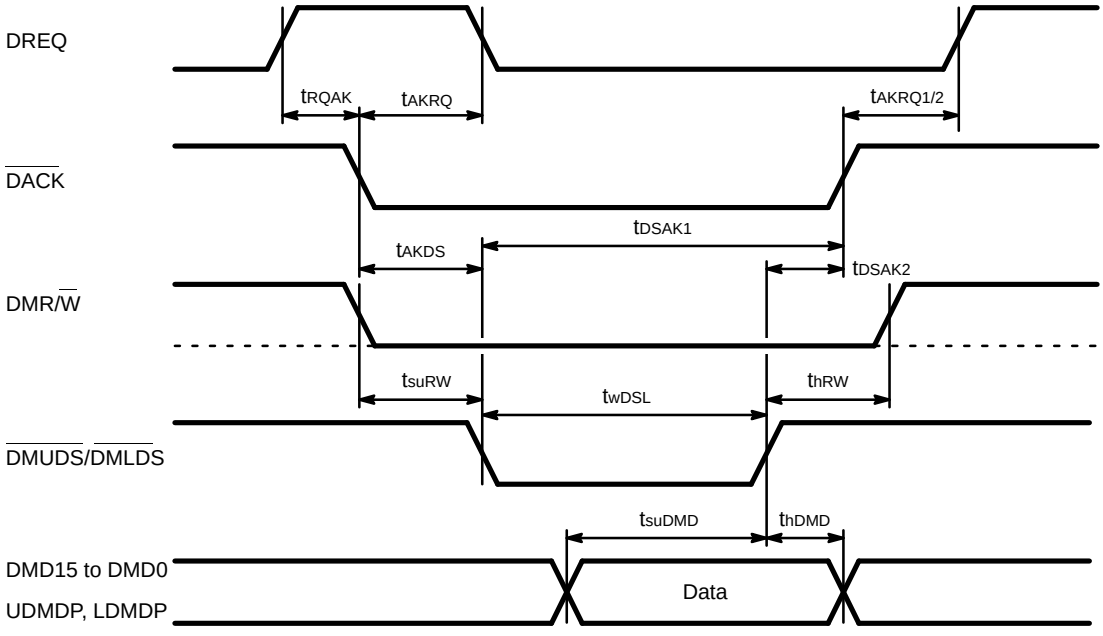


[68 Series Handshake Mode]

• Write timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{DACK}$ L assert time	DREQ H	t_{RQAK}	0	—	ns	
DREQ L negate time	$\overline{DACK}$ L	t_{AKRQ}	—	40	ns	
DREQ H assert time (8 bit)	$\overline{DACK}$ H	t_{RQAK1}	—	50	ns	
DREQ H assert time (16 bit)	$\overline{DACK}$ H	t_{RQAK2}	—	2 tCLK +40	ns	
$\overline{DMUDS}$/$\overline{DMLDS}$ L assert time	$\overline{DACK}$ L	t_{AKDS}	0	—	ns	
DM R/$\overline{W}$ set up time	$\overline{DMUDS}$/$\overline{DMLDS}$ L	t_{suRW}	20	—	ns	
DM R/$\overline{W}$ hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{hRW}	20	—	ns	
$\overline{DMUDS}$/$\overline{DMLDS}$ L level pulse width	—	t_{wDSL}	40	—	ns	
$\overline{DACK}$ H negate time	$\overline{DMUDS}$/$\overline{DMLDS}$ L	t_{DSAK1}	1 tCLK	—	ns	
	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{DSAK2}	0	—	ns	
Input data set up time	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{suDMD}	30	—	ns	
Input data hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{hDMD}	5	—	ns	

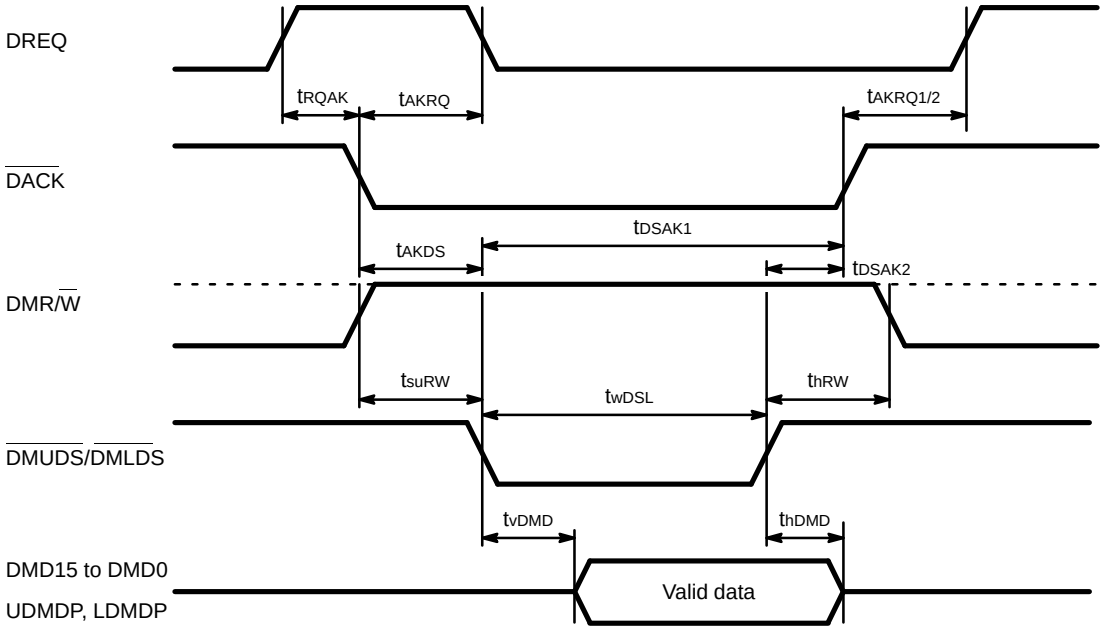
Figure 16. Register Write Timing



• Read timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{DACK}$ L assert time	DREQ H	t_{RQAK}	0	—	ns	
DREQ L negate time	$\overline{DACK}$ L	t_{AKRQ}	—	40	ns	
DREQ H assert time (8 bit)	$\overline{DACK}$ H	t_{AKRQ1}	—	50	ns	
DREQ H assert time (16 bit)	$\overline{DACK}$ H	t_{AKRQ2}	—	2 tCLK +40	ns	
$\overline{DMUDS}$/$\overline{DMLDS}$ L assert time	$\overline{DACK}$ L	t_{AKDS}	0	—	ns	
DM R/$\overline{W}$ set up time	$\overline{DMUDS}$/$\overline{DMLDS}$ L	t_{suRW}	20	—	ns	
DM R/$\overline{W}$ hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{hRW}	20	—	ns	
$\overline{DMUDS}$/$\overline{DMLDS}$ L level pulse width	—	t_{wDSL}	40	—	ns	
$\overline{DACK}$ H negate time	$\overline{DMUDS}$/$\overline{DMLDS}$ L	t_{DSAK1}	1 tCLK	—	ns	
	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{DSAK2}	0	—	ns	
Data output confirmation time	$\overline{DMUDS}$/$\overline{DMLDS}$ L	t_{vDMD}	—	40	ns	
Data output hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{hDMD}	10	—	ns	

Figure 17. Register Read Timing

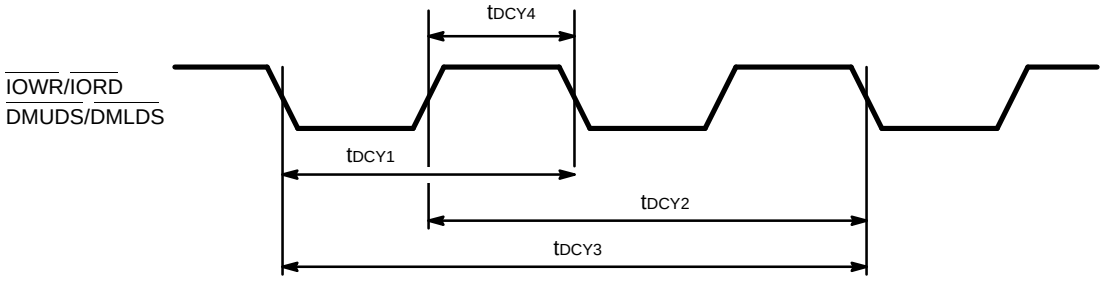


[Burst Mode (80 series/68 series common)]

• Data register access cycle time (8 bit)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Data register access cycle time 1	t_{DCY1}	tCLK	—	ns	
Data register access cycle time 2	t_{DCY2}	3 tCLK	—	ns	
Data register access cycle time 3	t_{DCY3}	4 tCLK	—	ns	
Data register access cycle time 4	t_{DCY4}	10	—	ns	

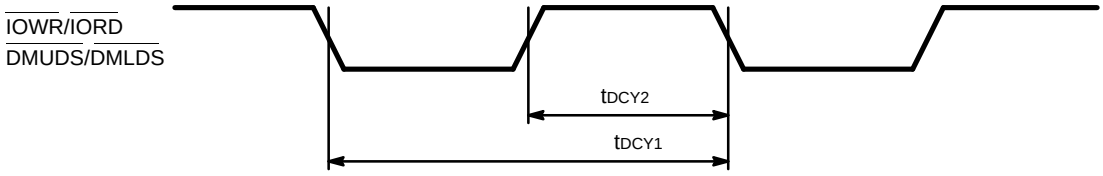
Figure 18. Data Register Access Cycle Time (8 bit)



• Data register access cycle time (16 bit)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Data register access cycle time 1	t_{DCY1}	4 tCLK	—	ns	
Data register access cycle time 2	t_{DCY2}	3 tCLK	—	ns	

Figure 19. Data Register Access Cycle Time (16 bit)

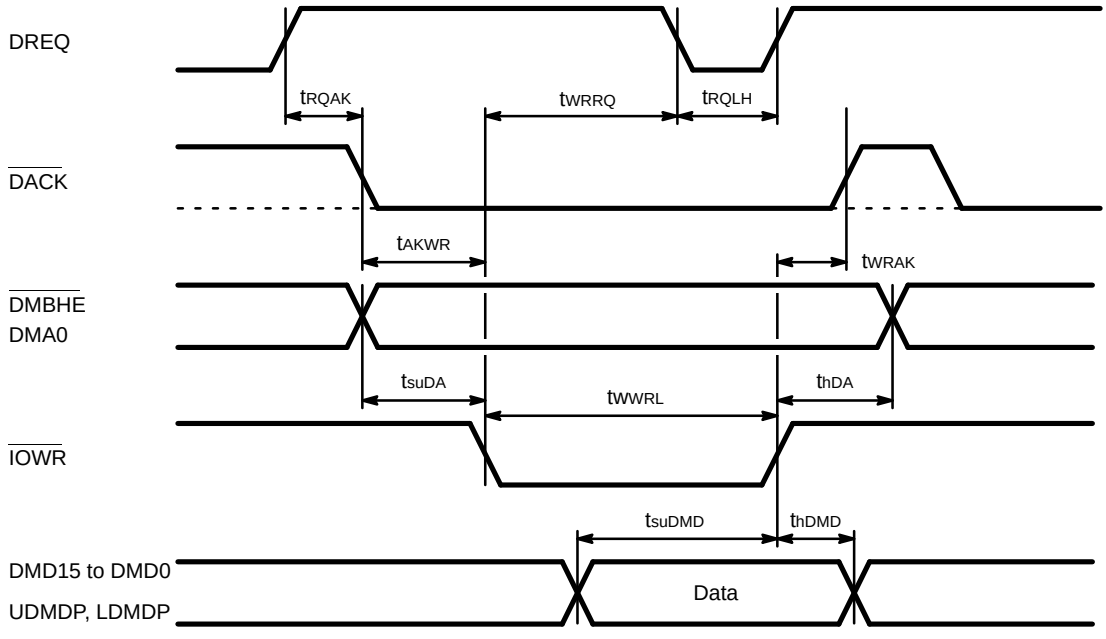


[80 Series Burst Mode]

• Write timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{DACK}$ L assert time	DREQ H	t_{RQAK}	0	—	ns	
DREQ L negate time	$\overline{IOWR}$ L	t_{WRRQ}	—	55	ns	
DREQ l ⟶ DREQ H return time	—	t_{RQLH}	0	—	ns	
$\overline{IOWR}$ L assert time	$\overline{DACK}$ L	t_{AKWR}	0	—	ns	
$\overline{DMBHE}$, DMA0 set up time	$\overline{IOWR}$ L	t_{suDA}	20	—	ns	
$\overline{DMBHE}$, DMA0 hold time	$\overline{IOWR}$ H	t_{hDA}	20	—	ns	
$\overline{IOWR}$ L level pulse width	—	t_{wWRL}	40	—	ns	
$\overline{DACK}$ H negate time	$\overline{IOWR}$ H	t_{WRAK}	0	—	ns	
Input data set up time	$\overline{IOWR}$ H	t_{suDMD}	30	—	ns	
Input data hold time	$\overline{IOWR}$ H	t_{hDMD}	5	—	ns	

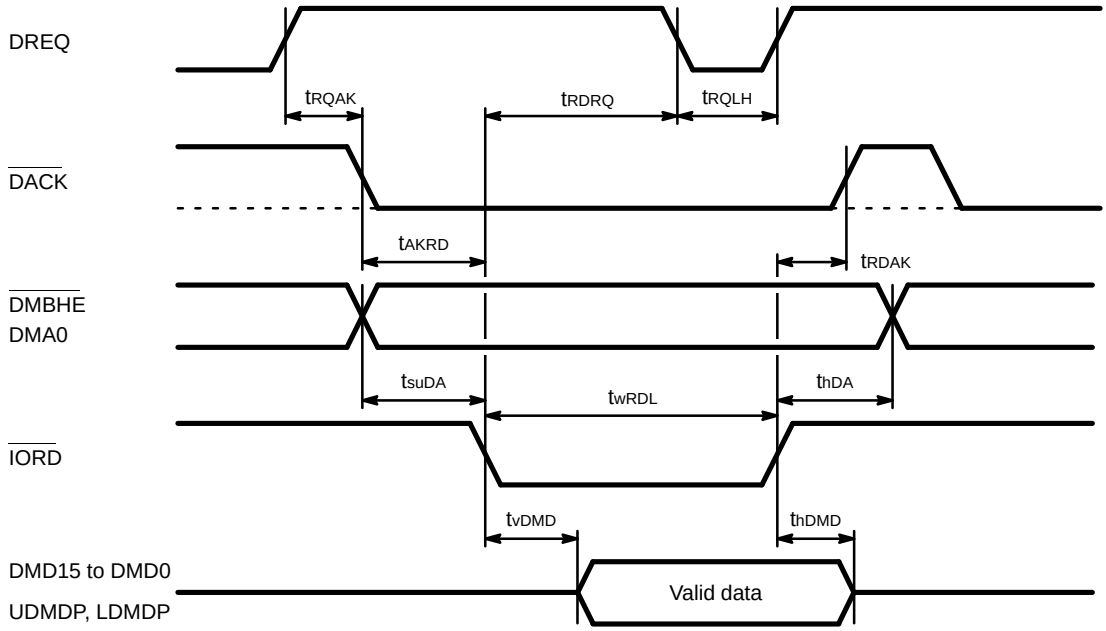
Figure 20. Register Write Timing



• Read timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{\text{DACK}}$ L assert time	DREQ H	t_{RQAK}	0	—	ns	
DREQ L negate time	$\overline{\text{IORD}}$ L	t_{RDRQ}	—	55	ns	
DREQ L → DREQ H return time	—	t_{RQLH}	0	—	ns	
$\overline{\text{IORD}}$ L assert time	$\overline{\text{DACK}}$ L	t_{AKRD}	0	—	ns	
$\overline{\text{DMBHE}}$, DMA0 set up time	$\overline{\text{IORD}}$ L	t_{suDA}	20	—	ns	
$\overline{\text{DMBHE}}$, DMA0 hold time	$\overline{\text{IORD}}$ H	t_{hDA}	20	—	ns	
$\overline{\text{IORD}}$ L level pulse width	—	t_{wRDL}	40	—	ns	
$\overline{\text{DACK}}$ H negate time	$\overline{\text{IORD}}$ H	t_{RDAK}	0	—	ns	
Data output confirmation time	$\overline{\text{IORD}}$ L	t_{vDMD}	—	40	ns	
Data output hold time	$\overline{\text{IORD}}$ H	t_{hDMD}	10	—	ns	

Figure 21. Register Read Timing

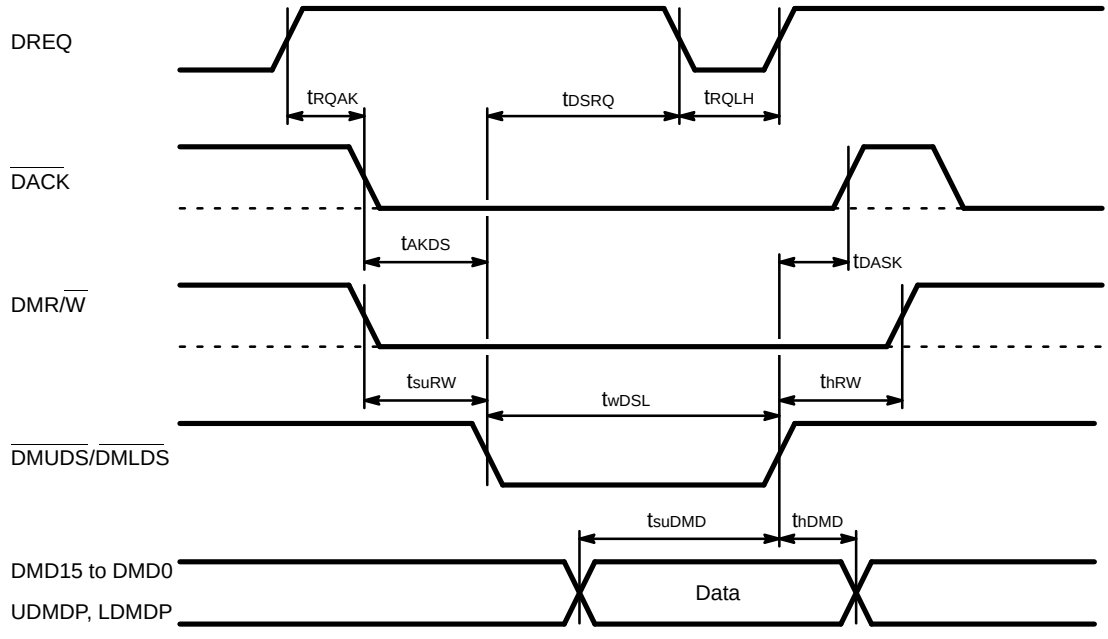


[68 Series Burst Mode]

• Write timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{DACK}$ L assert time	DREQ H	t_{RQAK}	0	—	ns	
DREQ L negate time	$\overline{DMUDS}/\overline{DMLDS}$ L	t_{DSRQ}	—	55	ns	
DREQ L → DREQ H return time	—	t_{RQLH}	0	—	ns	
$\overline{DMUDS}/\overline{DMLDS}$ L assert time	$\overline{DACK}$ L	t_{AKDS}	0	—	ns	
DM R/$\overline{W}$ set up time	$\overline{DMUDS}/\overline{DMLDS}$ L	t_{suRW}	20	—	ns	
DM R/$\overline{W}$ hold time	$\overline{DMUDS}/\overline{DMLDS}$ H	t_{hRW}	20	—	ns	
$\overline{DMUDS}/\overline{DMLDS}$ L level pulse width	—	t_{wDSL}	40	—	ns	
$\overline{DACK}$ H negate time	$\overline{DMUDS}/\overline{DMLDS}$ H	t_{DASK}	0	—	ns	
Input data set up time	$\overline{DMUDS}/\overline{DMLDS}$ H	t_{suDMD}	30	—	ns	
Input data hold time	$\overline{DMUDS}/\overline{DMLDS}$ H	t_{hDMD}	5	—	ns	

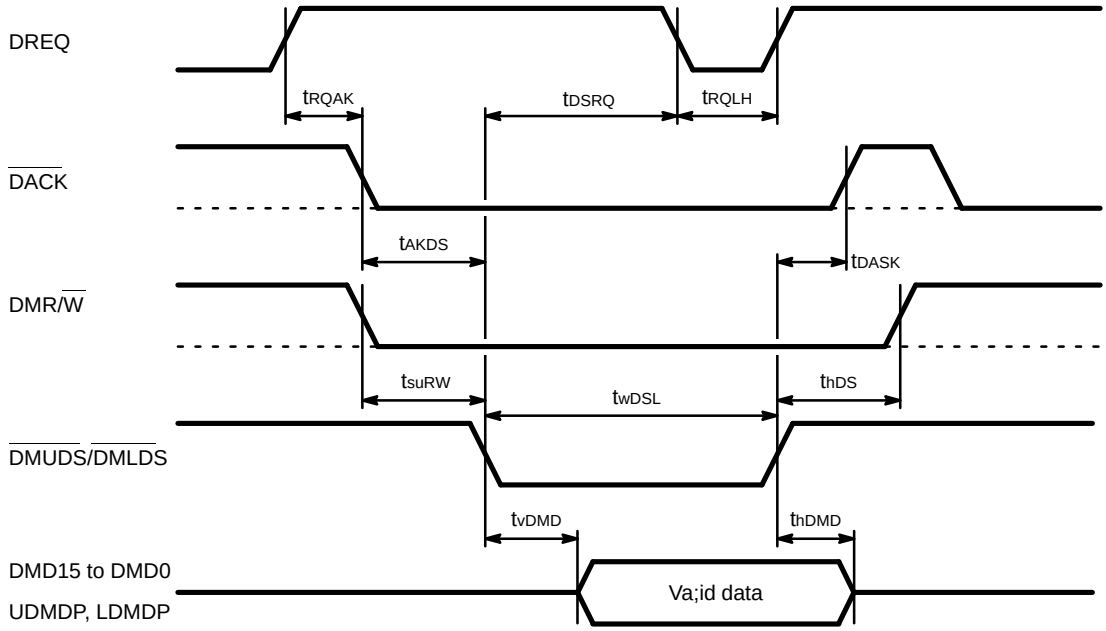
Figure 22. Register Write Timing



• Read timing

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{DACK}$ L assert time	DREQ H	t_{RQAK}	0	—	ns	
DREQ L negate time	$\overline{DMUDS}$/$\overline{DMLDS}$ L	t_{DSRQ}	—	55	ns	
DREQ L → DREQ H return time	—	t_{RQLH}	0	—	ns	
$\overline{DMUDS}$/$\overline{DMLDS}$ L assert time	$\overline{DACK}$ L	t_{AKDS}	0	—	ns	
DM R/$\overline{W}$ set up time	$\overline{DMUDS}$/$\overline{DMLDS}$ L	t_{suRW}	20	—	ns	
DM R/$\overline{W}$ hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{hRW}	20	—	ns	
$\overline{DMUDS}$/$\overline{DMLDS}$ L level pulse width	—	t_{wDSL}	40	—	ns	
$\overline{DACK}$ H negate time	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{DSAK}	0	—	ns	
Data output confirmation time	$\overline{DMUDS}$/$\overline{DMLDS}$ L	t_{vDMD}	—	40	ns	
Data output hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ H	t_{hDMD}	10	—	ns	

Figure 23. Register Read Timing



SCSI Interface (as Initiator)

[Asynchronous transfer Mode]

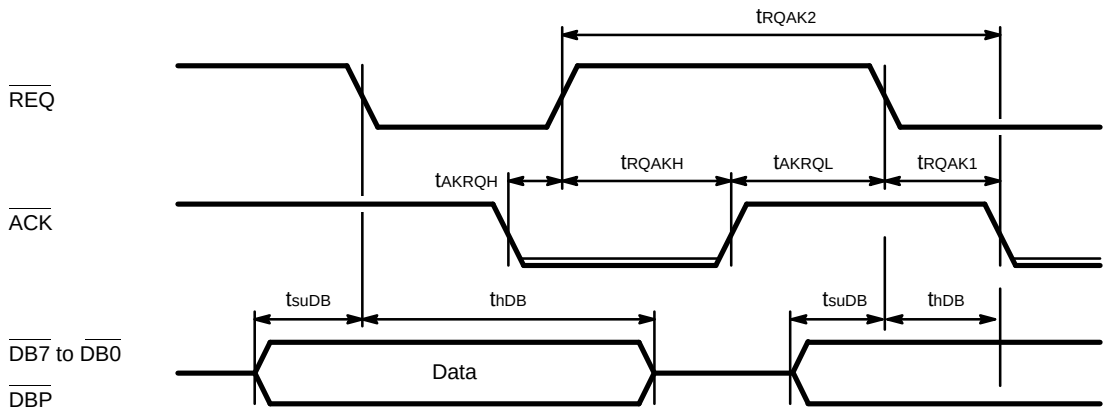
• Input timing (target → initiator)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{REQ}$ H negate time	$\overline{ACK}$ L	t_{AKRQH}	0	—	ns	
$\overline{ACK}$ H negate time	$\overline{REQ}$ H	t_{RQAKH}	—	60	ns	
$\overline{REQ}$ L assert time	$\overline{ACK}$ H	t_{AKRQL}	10	—	ns	
Input data set up time	$\overline{REQ}$ L	t_{suDB}	10	—	ns	
Input data hold time	$\overline{REQ}$ L	t_{hDB}	20	—	ns	
$\overline{ACK}$ L assert time 1	$\overline{REQ}$ L	t_{RQAK1}	—	40	ns	
$\overline{ACK}$ L assert time 2*1	$\overline{REQ}$ H	t_{RQAK2}	—	3 tCLK +40	ns	

*1 The REQ H ⟶ ACK L time (tRQAK2) is compared with (tRQAKH + tAKRQL + tRQAK1) and the longer value is chosen.

Note: The input timing definition is not applied in the following cases.
* When the data register is FULL in the data phase
* When the final byte is being transferred

Figure 24. Input Timing



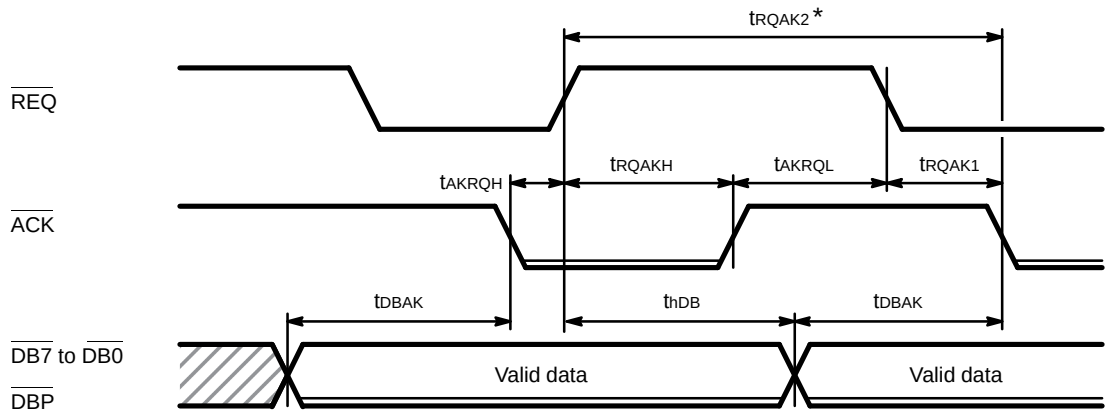
• Output timing (initiator → target)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{REQ}$ H negate time	$\overline{ACK}$ L	t_{AKRQH}	0	—	ns	
$\overline{ACK}$ H negate time	$\overline{REQ}$ H	t_{RQAKH}	—	60	ns	
$\overline{REQ}$ L assert time	$\overline{ACK}$ H	t_{AKRQL}	10	—	ns	
Time from output data confirmation to $\overline{ACK}$ L assert*	—	tDBAK	S·tCLK–10	—	ns	
Output data hold time	$\overline{REQ}$ H	t_{hDB}	2 tCLK	—	ns	
$\overline{ACK}$ L assert time	$\overline{REQ}$ L	t_{RQAK1}	—	40	ns	

* S value is based on the asynchronous set up time setting register (address 17h).

Note: The output timing definitions are not applied when the data register is EMPTY in the data phase.

Figure 25. Output Timing



* The $\overline{REQ}$ H → $\overline{ACK}$ L time (tRQAK2) is defined by either longer of (tRQAKH + tAKRQL + tRQAK1) or (thDB + tDBAK) (see the output timing waveform).

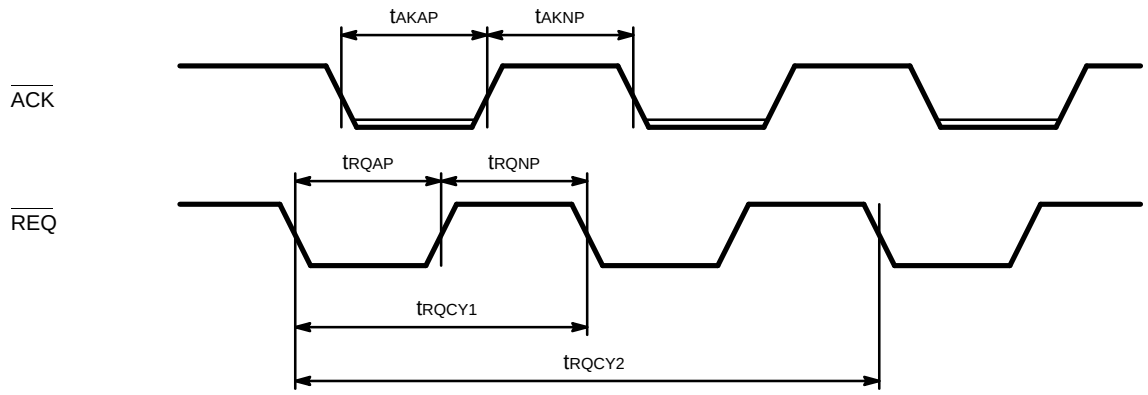
[Synchronous transfer Mode]

- $\overline{REQ}/\overline{ACK}$ signal period

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
$\overline{ACK}$ assert time*1	t_{AKAP}	A·tCLK–12	—	ns	
$\overline{ACK}$ negate time*1	t_{AKNP}	N·tCLK+2	—	ns	
$\overline{REQ}$ assert time	t_{RQAP}	20	—	ns	
$\overline{REQ}$ negate time	t_{RQNP}	20	—	ns	
$\overline{REQ}$ input cycle time 1	t_{RQCY1}	1 tCLK	—	ns	
$\overline{REQ}$ input cycle time 2	t_{RQCY2}	3 tCLK	—	ns	

*1 A and N values are based on the transfer period register (address 0Dh) setting.

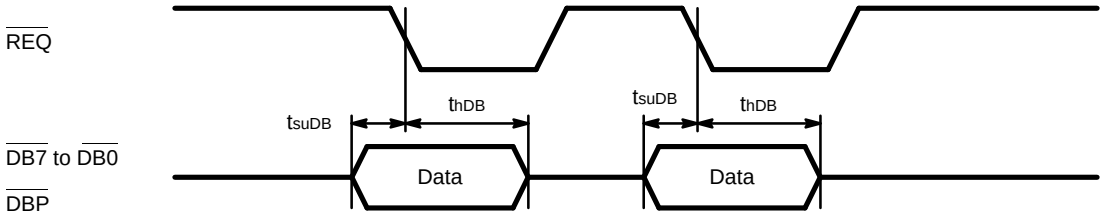
Figure 26. $\overline{REQ}/\overline{ACK}$ Signal Period



• Input timing (target → initiator)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Input data set up time	$\overline{REQ}$ L	t_{suDB}	10	—	ns	
Input data hold time	$\overline{REQ}$ L	t_{hDB}	20	—	ns	

Figure 27. Input Timing

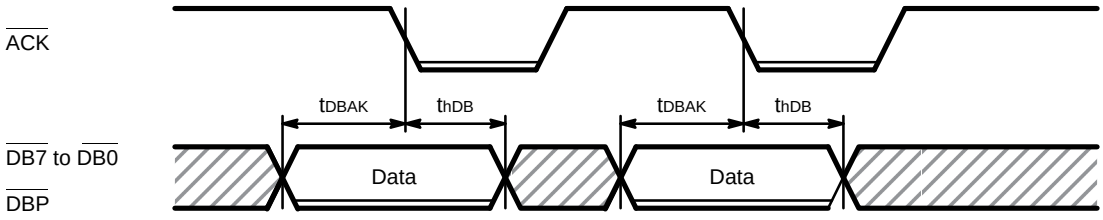


• Output timing (initiator → target)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Time from output data confirmation to $\overline{ACK}$ L assert*2	—	tDBAK	N · tCLK+2	—	ns	
Output data hold time*2	$\overline{ACK}$ L	thDB	A·tCLK–12	—	ns	

*2 A and N values are based on the transfer period register (address 0Dh) setting.

Figure 28. Output Timing



SCSI Interface (as target)

[Asynchronous transfer Mode]

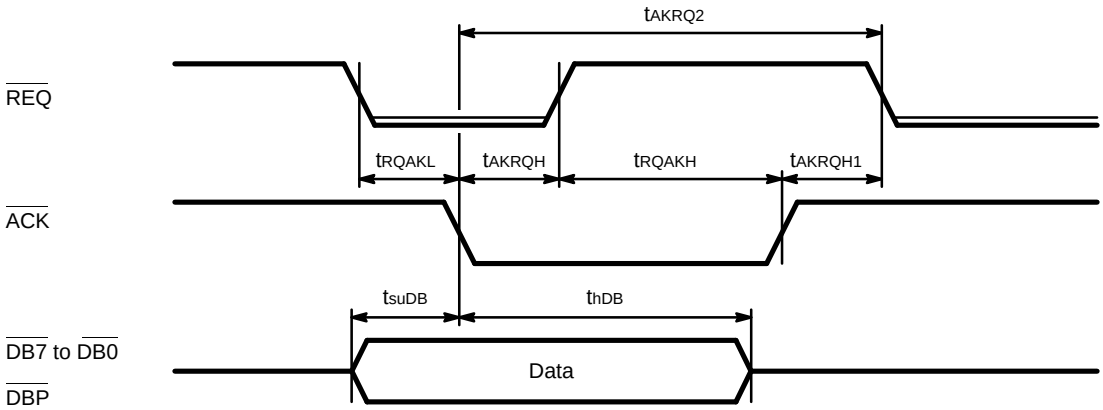
• Input timing (initiator → target)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{ACK}$ L assert time	$\overline{REQ}$ L	t_{RQAKL}	0	—	ns	
$\overline{REQ}$ H negate time	$\overline{ACK}$ L	t_{AKRQH}	—	60	ns	
$\overline{ACK}$ H negate time	$\overline{REQ}$ H	t_{RQAKH}	0	—	ns	
Input data set up time	$\overline{ACK}$ L	t_{suDB}	10	—	ns	
Input data hold time	$\overline{ACK}$ L	t_{hDB}	20	—	ns	
$\overline{REQ}$ L assert time 1	$\overline{ACK}$ H	t_{AKRQ1}	—	40	ns	
$\overline{REQ}$ L assert time 2 *1	$\overline{ACK}$ L	t_{AKRQ2}	—	3 tCLK +40	ns	

*1 The $\overline{ACK}$ L → $\overline{REQ}$ L time (tAKRQ2) is compared with (tAKRQH + tRQAKH + tAKRQ1) and the longer value is chosen.

Note: The input timing definition is not applied in the following cases.
* When the data register is FULL in the data phase

Figure 29. Input timing



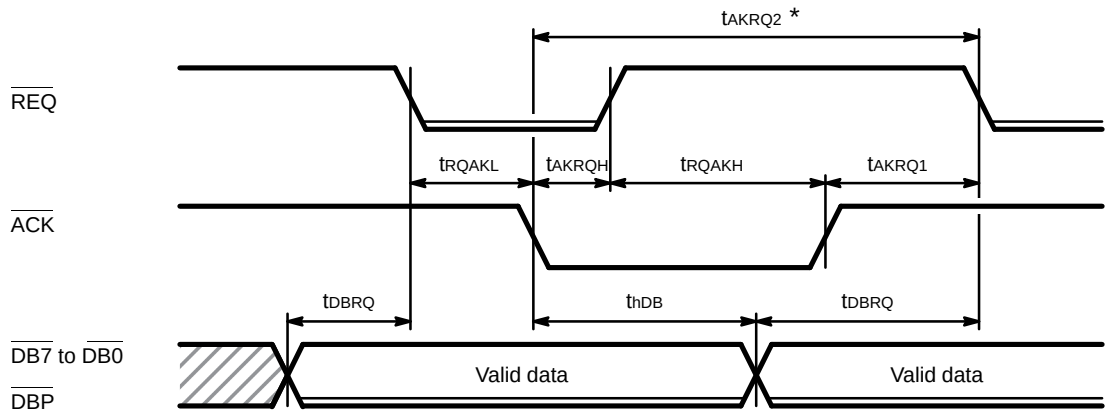
• Output timing (target → initiator)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
$\overline{ACK}$ L assert time	$\overline{REQ}$ L	t_{RQAKL}	0	—	ns	
$\overline{REQ}$ H negate time	$\overline{ACK}$ L	t_{AKRQH}	—	60	ns	
$\overline{ACK}$ H negate time	$\overline{REQ}$ H	t_{RQAKH}	0	—	ns	
Time from output data confirmation to $\overline{REQ}$ L assert6	—	tDBRQ	S·tCLK–10	—	ns	
Output data hold time	$\overline{ACK}$ L	t_{hDB}	2 tCLK	—	ns	
$\overline{REQ}$ L assert time	$\overline{ACK}$ H	t_{AKRQ1}	—	40	ns	

*2 S value is based on the asynchronous set up time setting register (address 17h).

Note: The output timing definitions are not applied when the data register is EMPTY in the data phase.

Figure 30. Output Timing



* The $\overline{ACK}$ L → $\overline{REQ}$ L time (tAKRQ2) is defined by either longer of (tAKRQH + tRQAKH + tAKRQ1) or (thDBC + tDBRQ).

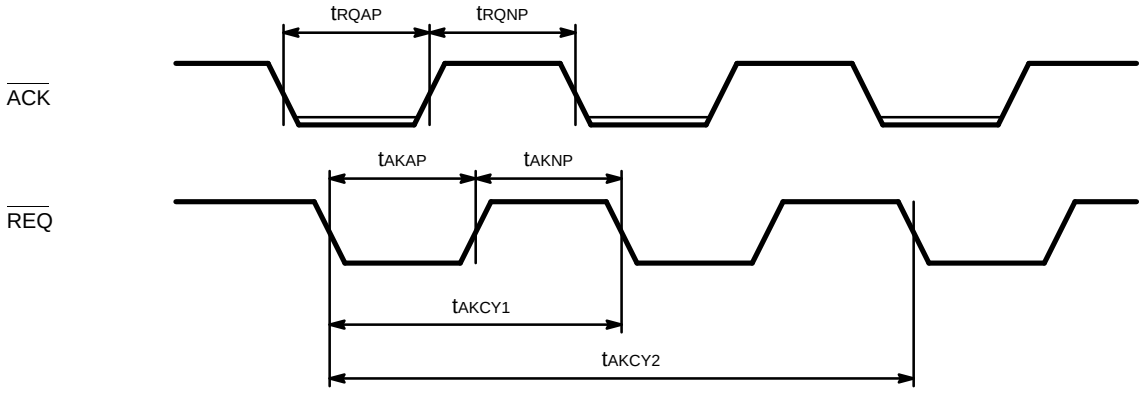
[Synchronous transfer Mode]

- $\overline{REQ}/\overline{ACK}$ signal period

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
$\overline{REQ}$ assert time	t_{RQAP}	A·tCLK–12	—	ns	
$\overline{REQ}$ negate time	t_{RQNP}	N·tCLK+2	—	ns	
$\overline{ACK}$ assert time	t_{AKAP}	20	—	ns	
$\overline{ACK}$ negate time	t_{AKNP}	20	—	ns	
$\overline{ACK}$ input cycle time 1	t_{AKCY1}	1 tCLK	—	ns	
$\overline{ACK}$ input cycle time 2	t_{AKCY2}	3 tCLK	—	ns	

*2 A and N values are based on the transfer period register (address 0Dh) setting. See (8) for more on setting values.

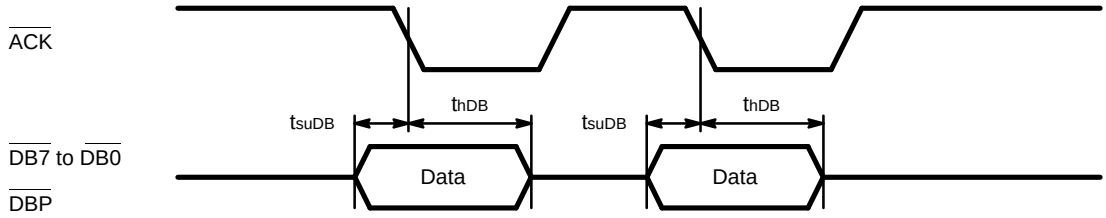
Figure 31. $\overline{REQ}/\overline{ACK}$ Signal Period



• Input timing (target → initiator)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Input data set up time	$\overline{ACK}$ L	t_{suDB}	10	—	ns	
Input data hold time	$\overline{ACK}$ L	t_{hDB}	20	—	ns	

Figure 32. Input timing

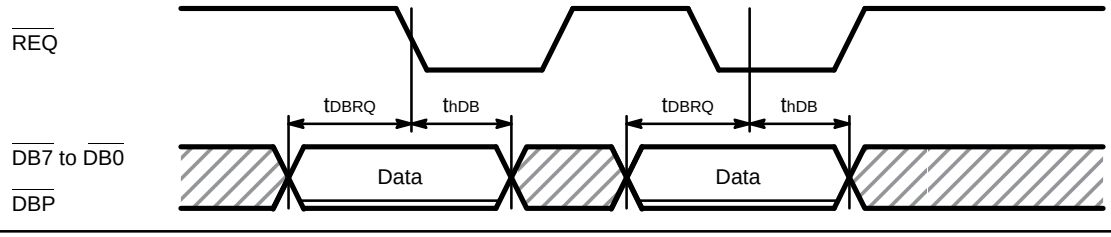


• Output timing (initiator → target)

Parameter	Base signal	Symbol	Value		Unit	Remarks
			Min.	Max.		
Time from output data confirmation to $\overline{REQ}$ L assert*2	—	t_{DBRQ}	N · tCLK +2	—	ns	
Output data hold time*2	$\overline{REQ}$ L	t_{hDB}	A · tCLK –12	—	ns	

*2 A and N values are based on the transfer period register (address 0Dh) setting.

Figure 33. Output Timing



(8) A/N/S Values in SCSI Interface Timing

- Transfer period register (address 07h) and A/N values

Transfer period register					A	N	Transfer period register					A	N
Bit4	Bit3	Bit2	Bit1	Bit0			Bit4	Bit3	Bit2	Bit1	Bit0		
0	0	0	0	1	(prohibit)	(prohibit)	1	0	0	0	1	9	8
0	0	0	1	0	1	1	1	0	0	1	0	9	9
0	0	0	1	1	2	1	1	0	0	1	1	10	9
0	0	1	0	0	2	2	1	0	1	0	0	10	10
0	0	1	0	1	3	2	1	0	1	0	1	11	10
0	0	1	1	0	3	3	1	0	1	1	0	11	11
0	0	1	1	1	4	3	1	0	1	1	1	12	11
0	1	0	0	0	4	4	1	1	0	0	0	12	12
0	1	0	0	1	5	4	1	1	0	0	1	13	12
0	1	0	1	0	5	5	1	1	0	1	0	13	13
0	1	0	1	1	6	5	1	1	0	1	1	14	13
0	1	1	0	0	6	6	1	1	1	0	0	14	14
0	1	1	0	1	7	6	1	1	1	0	1	15	14
0	1	1	1	0	7	7	1	1	1	1	0	15	15
0	1	1	1	1	8	7	1	1	1	1	1	16	15
1	0	0	0	0	8	8	0	0	0	0	0	16	16

The A and N values set in the register represent the assert period and the negate period respectively (unit is clock cycles).

For AC characteristics, A/N use numerals.

- Asynchronous set up time setting register (address 17h) setting values and S value

Asynchronous set up time setting register				S	Asynchronous set up time setting register				S
Bit3	Bit3	Bit3	Bit3		Bit3	Bit3	Bit3	Bit3	
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15
1	0	0	0	8	0	0	0	0	16

The S (set up time) value established in the set up time setting register during asynchronous data transfers indicates the time from setting data in the data bus until the $\overline{REQ}$/$\overline{ACK}$ signals are asserted.
For AC characteristics, S uses numerals.

LIST OF REGISTERS

1. Basic Control Registers (for write)

Address						Register name	Bit assignment							
Hex	A4	A3	A2	A1	A0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	Output data register (First)	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
1	0	0	0	0	1	Output data register (Second)	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8
2	0	0	0	1	0	Direct control register	DC7	0	0	DC4	0	0	0	0
3	0	0	0	1	1	(Reserve)	0	0	0	0	0	0	0	0
4	0	0	1	0	0	SEL/RESEL ID register	SI7	0	0	0	0	SI2	SI1	SI0
5	0	0	1	0	1	Command register	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
6	0	0	1	1	0	Data block register (MSB)	BL15	BL14	BL13	BL12	BL11	BL10	BL9	BL8
7	0	0	1	1	1	Data block register (LSB)	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
8	0	1	0	0	0	Data byte register (LSB)	BY23	BY22	BY21	BY20	BY19	BY18	BY17	BY23
9	0	1	0	0	1	Data byte register	BY15	BY14	BY13	BY12	BY11	BY10	BY9	BY8
0A	0	1	0	1	0	Data byte register (LSB) MC byte register	BY7	BY6	BY5	BY4	BY3	BY2	BY1	BY0
0B	0	1	0	1	1	Diagnostic control register	DG7	DG6	DG5	0	DG3	DG2	DG1	DG0
0C	0	1	1	0	0	Transfer mode register	TM7	0	0	0	0	0	0	0
0D	0	1	1	0	1	Transfer period register	0	0	0	TP4	TP3	TP2	TP1	TP0
0E	0	1	1	1	0	Transfer offset register	0	0	0	TO4	TO3	TO2	TO1	TO0
0F	0	1	1	1	1	Window address register	WA7	WA6	0	0	WA3	WA2	WA1	WA0

2. Basic Control Registers (for read)

Address						Register name	Bit assignment							
Hex	A4	A3	A2	A1	A0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	Input data register (First)	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	0	0	0	1	Input data register (Second)	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
2	0	0	0	1	0	SPC status register	SS7	SS6	SS5	SS4	×	SS2	SS1	SS0
3	0	0	0	1	1	Nexus status register	NS7	NS6	NS5	×	×	NS2	NS1	NS0
4	0	0	1	0	0	Interrupt status register	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
5	0	0	1	0	1	Command step register	CS7	CS6	CS5	$\overline{CS12}$	CS3	CS2	$\overline{CS1}$	$\overline{CS0}$
6	0	0	1	1	0	Data block register (MSB)	BL15	BL14	BL13	BL12	BL11	BL10	BL9	BL8
7	0	0	1	1	1	Data block register (LSB)	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
8	0	1	0	0	0	Data byte register (LSB)	BY23	BY22	BY21	BY20	BY19	BY18	BY17	BY16
9	0	1	0	0	1	Data byte register	BY15	BY14	BY13	BY12	BY11	BY10	BY9	BY8
0A	0	1	0	1	0	Data byte register (LSB) MC byte register	BY7	BY6	BY5	BY4	BY3	BY2	BY1	BY0
0B	0	1	0	1	1	SCSI control signal status register	SC7	SC6	CS5	SC4	SC3	SC2	SC1	SC0
0C	0	1	1	0	0	Transfer mode register	TM7	×	×	×	×	×	×	×
0D	0	1	1	0	1	Transfer period register	×	×	×	TP4	TP3	TP2	TP1	TP0
0E	0	1	1	1	0	Transfer offset register	×	×	×	TO4	TO3	TO2	TO1	TO0
0F	0	1	1	1	1	Modified byte register	×	×	MB5	MB4	MB3	MB2	MB1	MB0

Note: × indicates data undefined (0 or 1).

3. Initial Setting Window (for write/read)

Address						Register name	Bit assignment							
Hex	A4	A3	A2	A1	A1		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10	1	0	0	0	0	Clock conversion setting	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
11	1	0	0	0	1	Self ID setting	0	0	0	0	0	OI2	OI1	OI0
12	1	0	0	1	0	Response Mode setting	AM7	AM6	AM5	AM4	0	0	AM1	AM0
13	1	0	0	1	1	Selection/Reselection Mode setting	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0
14	1	0	1	0	0	Selection/Reselection retry setting	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
15	1	0	1	0	1	Selection/Reselection timeout setting	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
16	1	0	1	1	0	REQ/ACK timeout setting	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0
17	1	0	1	1	1	Asynchronous set up time setting	0	0	0	0	AT3	AT2	AT1	AT0
18	1	1	0	0	0	Parity error detection setting	PE7	PE6	PE5	PE4	PE3	0	PE1	PE0
19	1	1	0	0	1	Interrupt enable setting	IE7	0	IE5	IE4	IE3	IE2	IE1	IE0
1A	1	1	0	1	0	Group 6/7 command length setting	GL7	GL6	GL5	GL4	GL3	GL2	GL1	GL0
1B	1	1	0	1	1	DMA system setting	0	0	DM5	DM4	0	0	0	0
1C	1	1	1	0	0	Automatic operation mode setting	OM7	OM6	OM5	OM4	OM3	OM2	OM1	OM0
1D	1	1	1	0	1	SPC Timeout setting	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
1F	1	1	1	1	1	Device revision indication	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0

4. Mcs Buffer Window

Address						For write	For read
Hex	A4	A3	A2	A1	A0		
10	1	0	0	0	0	SEND MCS buffer	RECEIVE MCS buffer
11	1	0	0	0	1	SEND MCS buffer	RECEIVE MCS buffer
12	1	0	0	1	0	SEND MCS buffer	RECEIVE MCS buffer
13	1	0	0	1	1	SEND MCS buffer	RECEIVE MCS buffer
14	1	0	1	0	0	SEND MCS buffer	RECEIVE MCS buffer
15	1	0	1	0	1	SEND MCS buffer	RECEIVE MCS buffer
16	1	0	1	1	0	SEND MCS buffer	RECEIVE MCS buffer
17	1	0	1	1	1	SEND MCS buffer	RECEIVE MCS buffer
18	1	1	0	0	0	SEND MCS buffer	RECEIVE MCS buffer
19	1	1	0	0	1	SEND MCS buffer	RECEIVE MCS buffer
1A	1	1	0	1	0	SEND MCS buffer	RECEIVE MCS buffer
1B	1	1	0	1	1	SEND MCS buffer	RECEIVE MCS buffer
1C	1	1	1	0	0	SEND MCS buffer	RECEIVE MCS buffer
1D	1	1	1	0	1	SEND MCS buffer	RECEIVE MCS buffer
1E	1	1	1	1	0	SEND MCS buffer	RECEIVE MCS buffer
1F	1	1	1	1	1	SEND MCS buffer	RECEIVE MCS buffer

5. User Program Memory Window

Address						For write	For read
Hex	A4	A3	A2	A1	A0		
10	1	0	0	0	0	User program memory	User program memory
11	1	0	0	0	1	User program memory	User program memory
12	1	0	0	1	0	User program memory	User program memory
13	1	0	0	1	1	User program memory	User program memory
14	1	0	1	0	0	User program memory	User program memory
15	1	0	1	0	1	User program memory	User program memory
16	1	0	1	1	0	User program memory	User program memory
17	1	0	1	1	1	User program memory	User program memory
18	1	1	0	0	0	User program memory	User program memory
19	1	1	0	0	1	User program memory	User program memory
1A	1	1	0	1	0	User program memory	User program memory
1B	1	1	0	1	1	User program memory	User program memory
1C	1	1	1	0	0	User program memory	User program memory
1D	1	1	1	0	1	User program memory	User program memory
1E	1	1	1	1	0	User program memory	User program memory
1F	1	1	1	1	1	User program memory	User program memory

LIST OF COMMANDS

SPC commands can be specified by the command register or the user program memory and are divided into the following main groups.

- Sequential commands

Commands which perform a consecutive (including phase transition) sequence operation. Can only be specified by the command register (1 byte).

- Discrete commands

Commands which perform operations from disassembled sequential commands. Can be specified by the command register (1 byte command) or the user program memory (1/2 byte command).

- Special commands

Can only be specified by the user program memory (1/2 byte command).

1. Initiator Commands

(1) Sequential commands

No	Command code									Operand (for program)	Command name
1	00H	0	0	0	0	0	0	0	0	(not possible)	Select & CMD
2	01H	0	0	0	0	0	0	0	1	(not possible)	Select & 1-MSG & CMD
3	02H	0	0	0	0	0	0	1	0	(not possible)	Select & N-Byte-MSG & CMD
4	03H	0	0	0	0	0	0	1	1	(not possible)	Select & 1-MSG
5	04H	0	0	0	0	0	1	0	0	(not possible)	Select & N-Byte-MSG
6	05H	0	0	0	0	0	1	0	1	(not possible)	Send B-Byte-MSG
7	06H	0	0	0	0	0	1	1	0	(not possible)	Send N-Byte-CMD
8	07H	0	0	0	0	0	1	1	1	(not possible)	Receive N-Byte-MSG

(2) Discrete commands

No	Command code									Operand (for program)	Command name
9	08H	0	0	0	0	1	0	0	0	—	Select
10	09H	0	0	0	0	1	0	0	1	—	Select with “ATN”
11	0AH	0	0	0	0	1	0	1	0	—	Set ATN
12	0BH	0	0	0	0	1	0	1	1	—	Reset ATN
13	0CH	0	0	0	0	1	1	0	0	—	Set ACK
14	0DH	0	0	0	0	1	1	0	1	—	Reset ACK
15	10H	0	0	0	1	0	0	0	0	—	Send Data from MPU
16	11H	0	0	0	1	0	0	0	1	—	Send Data from DMA
17	12H	0	0	0	1	0	0	1	0	—	Receive Data from MPU
18	13H	0	0	0	1	0	0	1	1	—	Receive Data from DMA
19	14H	0	0	0	1	0	1	0	0	—	Send DATA from MPU Padding
20	15H	0	0	0	1	0	1	0	1	—	Send DATA from DMA Padding
21	16H	0	0	0	1	0	1	1	0	—	Receive Data to MPU Padding
22	17H	0	0	0	1	0	1	1	1	—	Receive Data to DMA Padding
23	18H	0	0	0	1	1	0	0	0	Address of MSG sent	Send 1-MSG
24	19H	0	0	0	1	1	0	0	1	Address of MSG sent	Send 1-MSG with ATN
25	1AH	0	0	0	1	1	0	1	0	SAVE address of MSG	Receive MSG
26	1BH	0	0	0	1	1	0	1	1	Address of CMD sent	Send CMD
27	1CH	0	0	0	1	1	1	0	0	SAVE address of STATUS	Receive STATUS

2. Target Commands

(1) Sequential commands

No	Command code									Operand (for program)	Command name
1	20H	0	0	1	0	0	0	0	0	(not possible)	Reselect & 1-MSG
2	21H	0	0	1	0	0	0	0	1	(not possible)	Reselect & N-Byte-MSG
3	22H	0	0	1	0	0	0	1	0	(not possible)	Reselect & 1-MSG & Terminate
4	23H	0	0	1	0	0	0	1	1	(not possible)	Reselect & 1-MSG & Link-Terminate
5	24H	0	0	1	0	0	1	0	0	(not possible)	Terminate
6	25H	0	0	1	0	0	1	0	1	(not possible)	Link-Terminate
7	26H	0	0	1	0	0	1	1	0	(not possible)	Desconnect-Sequence
8	27H	0	0	1	0	0	1	1	1	(not possible)	Send N-Byte-CMD
9	28H	0	0	1	0	1	0	0	0	(not possible)	Receive N-Byte CMD
10	29H	0	0	1	0	1	0	0	1	(not possible)	Receive N-Byte-MSG
11	2AH	0	0	1	0	1	0	1	0	(not possible)	Reselect & N-Byte-MSG & Terminate
12	2BH	0	0	1	0	1	0	1	1	(not possible)	Reselect & N-Byte-MSG & Link Terminate
13	2CH	0	0	1	0	1	1	0	0	(not possible)	Disconnect-Squence2

(2) Discrete commands

No	Command code									Operand (for program)	Command name
14	30H	0	0	1	1	0	0	0	0	—	Reselect
15	31H	0	0	1	1	0	0	0	1	—	Set “REQ”
16	32H	0	0	1	1	0	0	1	0	—	Reset “REQ”
17	33H	0	0	1	1	0	0	1	1	—	Disconnect
18	34H	0	0	1	1	0	1	0	0	—	Send Data from MPU
19	35H	0	0	1	1	0	1	0	1	—	Send Data from DMA
20	36H	0	0	1	1	0	1	1	0	—	Receive Data to MPU
21	37H	0	0	1	1	0	1	1	1	—	Receive Data to DMA
22	38H	0	0	1	1	1	0	0	0	Address of MSG sent	Send 1 MSG
23	39H	0	0	1	1	1	0	0	1	SAVE address of MSG	Receive MSG
24	3AH	0	0	1	1	1	0	1	0	Address of STATUS sent	Send status
25	3BH	0	0	1	1	1	0	1	1	SAVE address of CDB	Receive CMD

3. Common Commands

No	Command code									Operand (for program)	Command name
1	40H	0	1	0	0	0	0	0	0	(not possible)	SOFTWARE RESET
2	41H	0	1	0	0	0	0	0	1	(not possible)	TRANSFER RESET
3	42H	0	1	0	0	0	0	1	0	(not possible)	SCSI RESET
4	43H	0	1	0	0	0	0	1	1	(not possible)	SET UP REG
5	44H	0	1	0	0	0	1	0	0	(not possible)	INIT DIAG START
6	45H	0	1	0	0	0	1	0	1	(not possible)	TARG DIAG START
7	46H	0	1	0	0	0	1	1	0	(not possible)	DIAG END
8	47H	0	1	0	0	0	1	1	1	(not possible)	COMMAND PAUSE
9	48H	0	1	0	0	1	0	0	0	(not possible)	SET RST
10	49H	0	1	0	0	1	0	0	1	(not possible)	RESET RST

4. Programmable Commands

The user program is stored in the user program memory and begins operation when the user program head address is written in the command register.

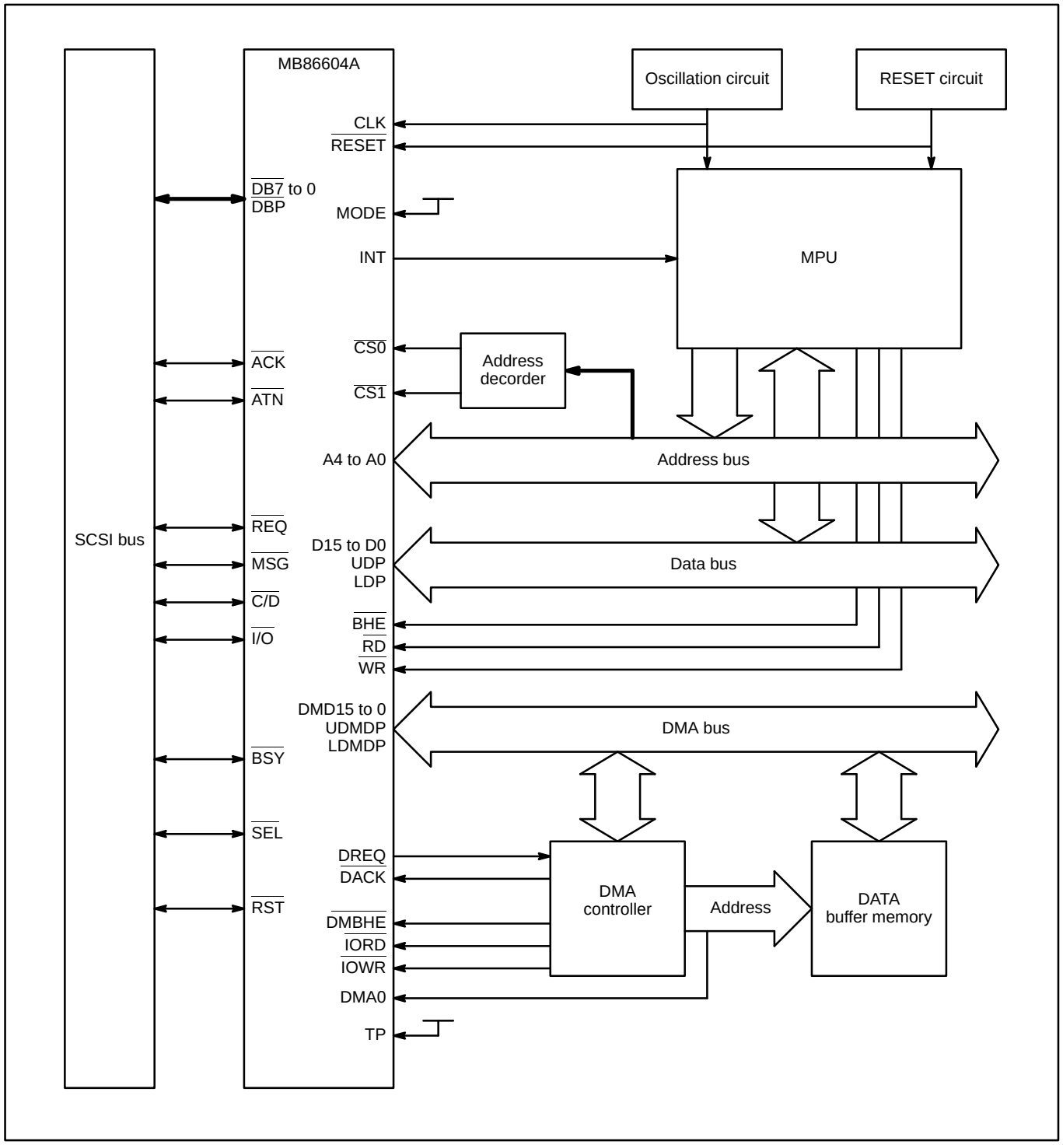
Programmable commands are either discrete or special commands and have a command length of one (1) or two (2) bytes.

- Command Field Assign

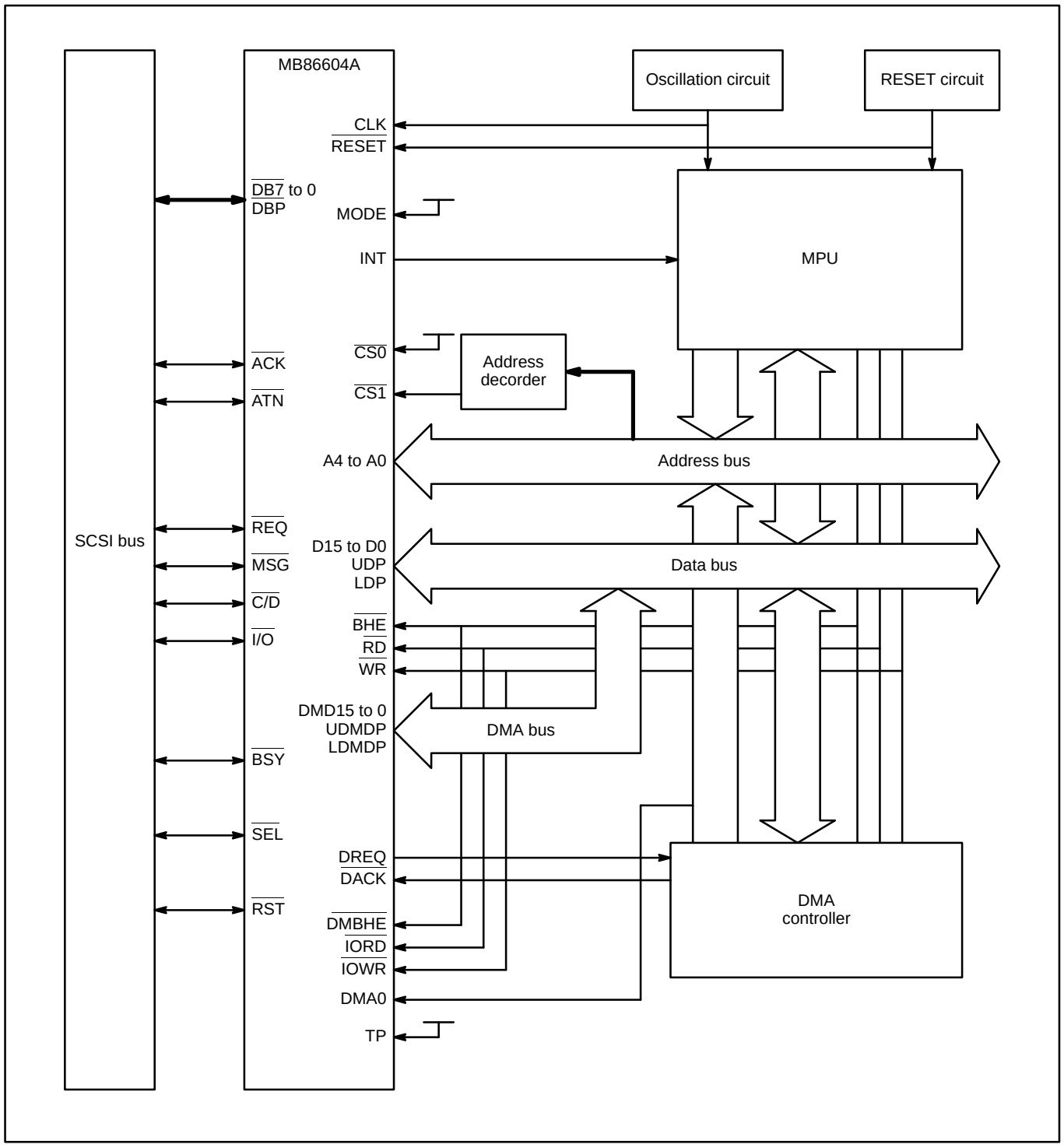
	Command code (1st byte)	Operand (2nd byte)
Discrete commands	Message, command, or status phase send command	Memory address of data to be sent
	Message, command, or status phase receive command	Memory address of received data being stored
	Data phase receive/send command or do not perform transfer command	—
Special commands	AND command	Data for AND operation or memory address of data for AND operation
	TEST AND command	Data for AND operation or memory address of data for AND operation
	COMPARE command	Data for COMPARE operation or memory address of data for COMPARE operation
	Conditional branch command	Jump head address
	MOVE command	Memory address to be moved
	STOP command	User status code
	NOP command	—

SYSTEM CONFIGURATION EXAMPLE

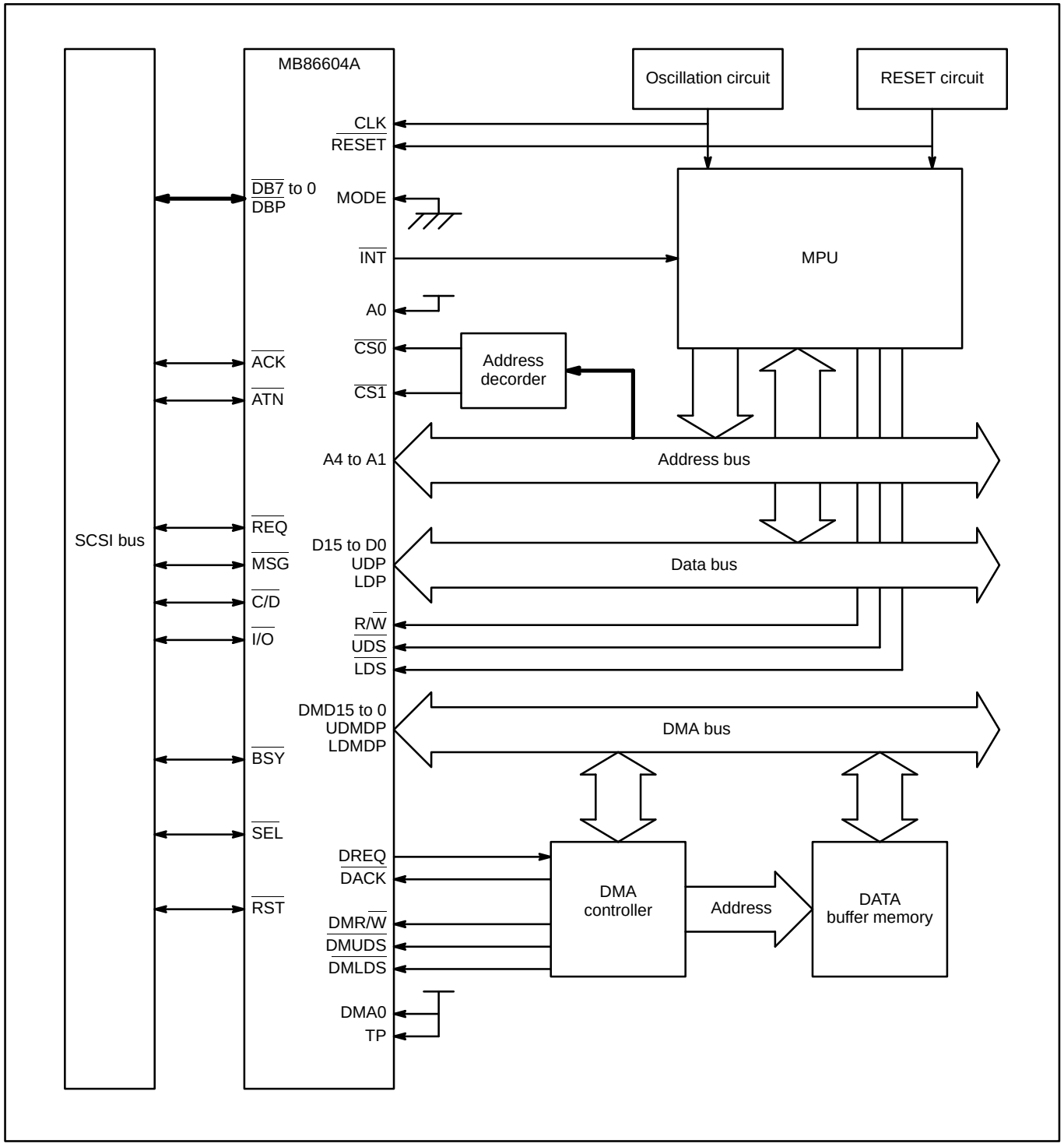
1. 80 Series, Separate Bus Type



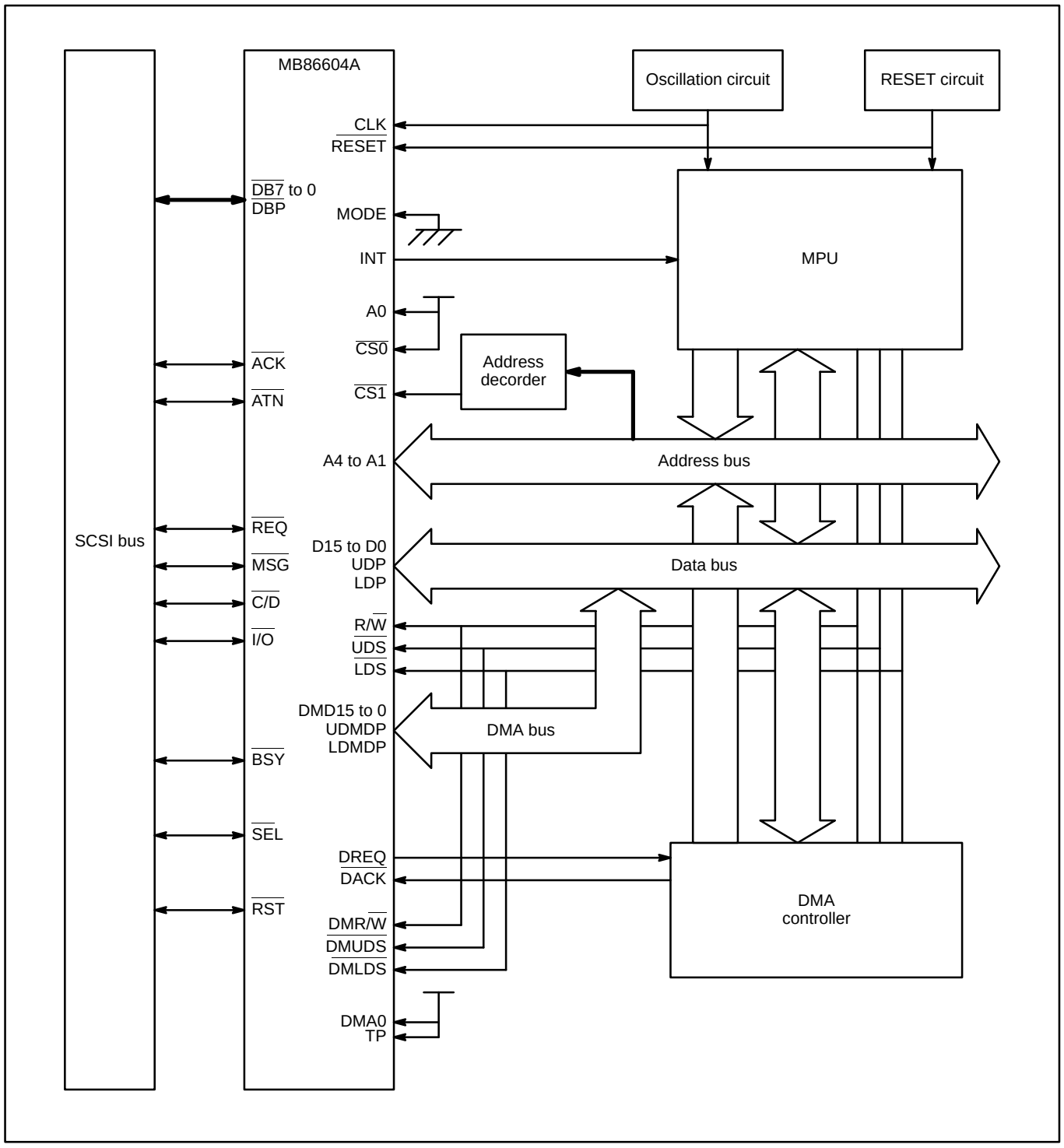
2. 80 Series, Shared Bus Type



3. 68 Series, Separate Bus Type



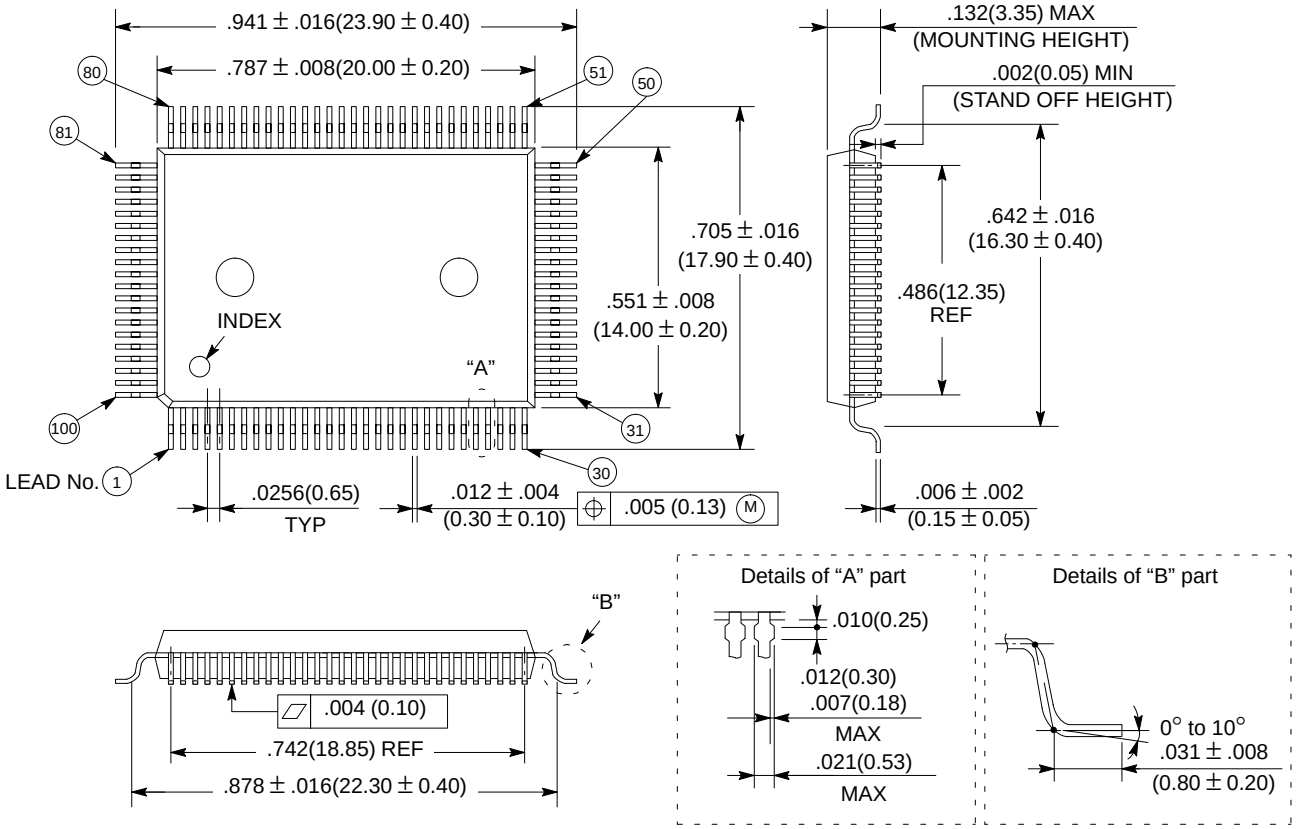
4. 68 Series, Shared Bus Type



PACKAGE DIMENSIONS

MB88604A–PF

100-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-100P-M06)



Dimensions in
inches (millimeters)

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