Doc. Descript. Changes from 1993 MB86930 SPARClite User's Manual 1994

Err. No. Exxxx

Subject Warning Note Cache/Memory Interface

Entered By Bruce McKeever

Created 4/27/94

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Page 2–48

Table

Figure

Section 2.6 Data and Instruction Caches

Subsection 2.6.2 Operation

Location paragraph 5

Was
"Otherwise, a new line needs to be allocated on a read miss ... The fetched word overwrites the appropriate word in this line; its Valid bit is then set, and the Valid bits for the other words in the line are cleared."

Should Be (add)

"Warning note: the entire 32 bits on the data bus are stored in cache. Even when reading bytes or half words from external memory, the external memory should supply the complete word. A subsequent load byte or load half word with the same word address may be processed as a cache hit."

Explanation
A SPARClite customer got in trouble because they implemented their external

memory subsystem to use the byte enable signals literally and only supplied the requested byte or half word.

Doc. Descript. Changes from 1993 MB86930 SPARClite User's Manual 1994

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Page 3–16

Table

Figure

Section 3.2 Data and Instruction Caches

Location paragraph 3

Was
"in the MB86930 processor, each cache is 2 Kbytes in size, organized into two banks of sixty–four 16–byte lines. Cache lines are refilled in 4–byte increments to avoid the interrupt latency incurred by long, uninterruptible cache line replacements."

Should Be
add

"Warning note: all 4–bytes must be supplied by external memory even when responding to load byte or load half word."

Explanation
A SPARClite customer got in trouble because they implemented their external

memory subsystem to use the byte enable signals literally and only supplied the requested byte or half word.

Doc. Descript. Changes from 1993 MB86930 SPARClite User's Manual 1994

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Page 4–5

Table

Figure

Section 4.1 Signals

Subsection 4.1.2 Memory Interface

Location Signal –BE3–0

Was
parenthetical note at end of descriptive paragraph. "(the byte enable signals can be ignored during load operations)."

Should Be

"(the byte enable signals should be ignored during load operations for any section of memory that may be cacheable)."

Explanation
A SPARClite customer got in trouble because they implemented their external

memory subsystem to use the byte enable signals literally and only supplied the requested byte or half word.

Doc. Descript. **MB86930 SPARClite Application Note 1**

Dram Control Interface

Err. No. Exxxx

Subject Warning Note Cache/Memory Interface

Entered By Bruce McKeever

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Page 3

Table

Figure

Section Introduction

Subsection Byte Enable

Location last paragraph

Was
”The Byte Enable signals, –BE<3:0>, from SPARClite are used during write cycles to indicate the data size being transferred and not used during read cycles.

Should Be: add

”Warning note: Since, during memory read operations when data cache is on, all 32 bits on the data bus are stored in cache, external memory should supply the complete word, ignoring byte enables.”

Explanation
A SPARClite customer got in trouble because they implemented their external memory subsystem to use the byte enable signals literally and only supplied the requested byte or half word.

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

Err. No. Exxxx

Subject replace "word" with "window"

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Created 4/11/95

Last Modified

Page 2–36

Table

Figure

Section 2.5 Instructions

Subsection 2.5.4 Control Transfer Inctructions

Location following figure 2–37, 1st paragraph with head "Return from Trap"

Was

> Unless it causes a trap, the RETT instruction does four things: it increments the Current **Word** Pointer (modulo 8), causes a delayed control transfer to the register-indirect target address, restores the processor to the operating mode (user or supervisor) it was in before the trap was taken, and enables traps.

Should be

> Unless it causes a trap, the RETT instruction does four things: it increments the Current **Window** Pointer (modulo 8), causes a delayed control transfer to the register-indirect target address, restores the processor to the operating mode (user or supervisor) it was in before the trap was taken, and enables traps.

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

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Subject switch names of registers 1 and 0

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Page 2–59

Table

Figure 2–37. Debug Status Register

Section 2.8 Debur Support Unit

Subsection 2.8.2 Breakpoint Registers

Location following figure 2–37, 1st paragraph with head "Return from Trap"

Was

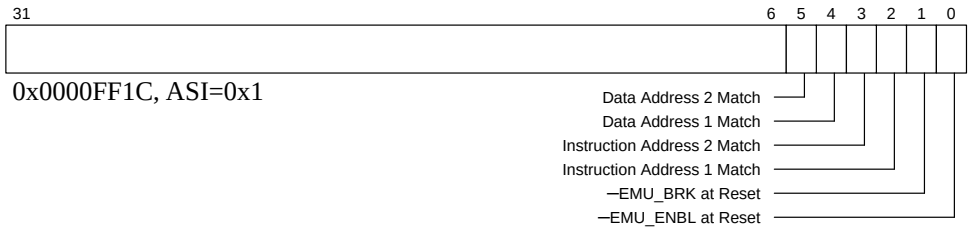

Figure 2-37. Debug Status Register

Should be

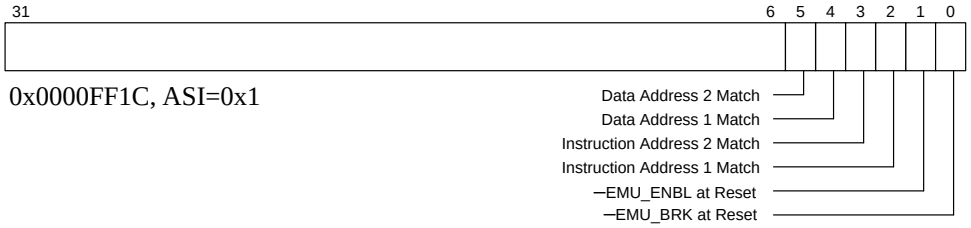

Figure 2-37. Debug Status Register

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

Err. No. Exxxx

Subject Correction of LDD hold cycle equation

Entered By Bruce McKeever

Created 4/11/95

Last Modified

Page 3–6

Table

Figure

Section 3.1 Integer Unit

Subsection 3.1.1 I Block

Location lower part of page, following Note

Was

```
LDD [%r1+%r2],%0r4
ADD %r5,%r5,%r6
```

Should be

```
LDD [%r1+%r2],%r4
ADD %r5,%r5,%r6
```

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

Err. No. Exxxx

Subject Additions to table 3–2 Detection of Trap Conditions

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Page 3–7

Table 3–2 Detection of Trap Conditions

Figure

Section 3.1 Integer Unit

Subsection 3.1.1 I Block

Location: Row 14 and 15 moved to 3rd and 4th row of table

Was

Figure 3-2: Detection of Trap Conditions

Priority	Trap Type	Stage Detected	Trap
1			reset (hardware reset)
1 2 3 4	— 1 3 2	D F D D	reset instruction_access_exception priv_instruction illegal_instruction
5 5 6 7	4 36 5 6	D D D D	fp_disabled cp_disabled window_overflow window_underflow
8 10 11 12 13 13	7 9 10 128-255 255 255	E M E D F M	mem_address_not_aligned data_access_exception tag_overflow trap_instruction (Ticc) instruction_breakpoint data_breakpoint
14 15 — — — 28	31 30 — — — 17		interrupt_level_15 interrupt_level_14 — — — interrupt_level_1

Should be

Figure 3-2: Detection of Trap Conditions

Priority	Trap Type	Stage Detected	Trap
1			reset (hardware reset)
1 1.5 1.5 2 3 4	— 255 255 1 3 2	D F M F D D	reset instruction_breakpoint data_breakpoint instruction_access_exception priv_instruction illegal_instruction
5 5 6 7	4 36 5 6	D D D D	fp_disabled cp_disabled window_overflow window_underflow
8 10 11 12	7 9 10 128-255	E M E D	mem_address_not_aligned data_access_exception tag_overflow trap_instruction (Ticc)
14 15 — — — 28	31 30 — — — 17		interrupt_level_15 interrupt_level_14 — — — interrupt_level_1

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

Err. No. Exxxx

Subject Added minus symbol to EMU_BRK in Table 4–1, Input and Output Signals

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Last Modified

Page 4–2

Table 4–1, Input and Output Signals

Figure

Section 4.1 Signals

Subsection

Location 3rd column of table, 5th entry

Was

Table 4-1: Input and Output Signals

Symbol	Type	Symbol	Type	Symbol	Type	Symbol	Type
ADR <31:2>	O S(L) G(Z) I (1)	–CS0, –CS1 –CS2, –CS3 –CS4, –CS5	O S(L) G(1) I (1)	–LOCK	O S(L) G(Z) I (1)	TDO	O
–AS	O S(L) G(Z) I (1)	D <31:0>	I/O S(L) G(Z) I (Z)	–MEXC	I S(L)	–TIMER_OVF	O S(L) G(Q) I (Q)
ASI <7:0>	O S(L) G(Z) I (1)	**EMU_BRK**	I	–SAME_PAGE	O S(L) G(1) I (1)	TMS	I
–BE 3-0	O S(L) G(Z) I (0)	EMU_D<3:0>	I/O	RD/–WR	O S(L) G(Z) I (1)	–TRST	I
–BGRNT	O S(L) G(0) I (Q)	–EMU_ENB	I	–READY	I S(L)	XTAL1 (CLKIN) XTAL2	I O G(Q) I (Q)
–BREQ	I S(L)	EMU_SD <3:0>	I/O	–RESET	I A(L)		
CLKOUT1 CLKOUT2	O G(Q) I (Q)	–ERROR	O S(L) G(Q) I (Q)	TCK	I		
CLK_ECB	I	IRL <3:0>	I A(L)	TDI	I		

Should be

Table 4-1: Input and Output Signals

Symbol	Type	Symbol	Type	Symbol	Type	Symbol	Type
ADR <31:2>	O S(L) G(Z) I (1)	—CS0, –CS1 —CS2, –CS3 —CS4, –CS5	O S(L) G(1) I (1)	—LOCK	O S(L) G(Z) I (1)	TDO	O
—AS	O S(L) G(Z) I (1)	D <31:0>	I/O S(L) G(Z) I (Z)	—MEXC	I S(L)	—TIMER_OVF	O S(L) G(Q) I (Q)
ASI <7:0>	O S(L) G(Z) I (1)	**—EMU_BRK**	I	—SAME_PAGE	O S(L) G(1) I (1)	TMS	I
—BE 3-0	O S(L) G(Z) I (0)	EMU_D<3:0>	I/O	RD/–WR	O S(L) G(Z) I (1)	—TRST	I
—BGRNT	O S(L) G(0) I (Q)	—EMU_ENB	I	—READY	I S(L)	XTAL1 (CLKIN) XTAL2	I O G(Q) I (Q)
—BREQ	I S(L)	EMU_SD <3:0>	I/O	—RESET	I A(L)		
CLKOUT1 CLKOUT2	O G(Q) I (Q)	—ERROR	O S(L) G(Q) I (Q)	TCK	I		
CLK_ECB	I	IRL <3:0>	I A(L)	TDI	I		

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

Err. No. Exxxx

Subject Correction of code fragment

Entered By Bruce McKeever

Created 4/11/95

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Page 5–2

Table

Figure

Section 5.1 Initialization

Subsection 5.1.1 Establishing the Processor State

Location Center of page 5–2

Was

```
! Reset Initialization
    wr  %g0,    0x0fa7,%psr    ! Set psr: mask interrupts, mode=S, Pmode=U,
                               ! traps enabled, CWP=7
    wr  %g0,    0x0, %wim      ! Initialize wim to window 0
    wr  %g0,    0x0, %tbr      ! Initialize tbr to 0
```

Should be

```
! Reset Initialization
    wr  %g0,    0x0fa7,%psr    ! Set psr: mask interrupts, mode=S, Pmode=S,
                               ! traps enabled, CWP=7
    wr  %g0,    0x0, %wim      ! Initialize wim to window 0
    wr  %g0,    0x0, %tbr      ! Initialize tbr to 0
```

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

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Subject Correction of calling convention

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Last Modified

Page 5–34

Table

Figure

Section 5.5 Division Routines Using the DIVScc Instruction

Subsection 5.5.5 Unsigned Division with Word Dividend (divu1)

Location 9 lines above "5.5.6 Divide Step In Support of A to D Converter Compensation"

Was

```
          .
          divscc %o1, %o2, %o1
          divscc %o1, %o2, %o1 !divide step 31
          retl                 !exit for quotient–only divide
          divscc %o1, %o2, %o1 !divide step 32

   !ALL the following steps may be omitted for quotient–only divide
```

Should be

```
          .
          divscc %o1, %o2, %o1
          divscc %o1, %o2, %o1 !divide step 31
   !      retl                 !exit for quotient–only divide
          divscc %o1, %o2, %o1 !divide step 32

   !ALL the following steps may be omitted for quotient–only divide
```

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

Err. No. Exxxx

Subject Correction of code fragment

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Page 5–37

Table

Figure

Section 5.6 Using the SCAN Instruction

Subsection 5.6.1 Scan in Support of Software Floating Point

Location Bottom of page 5–37

Was

```
        .
          .
            .
    sethi 0x3fe, %g5              !mask for sign and exponent with and
                                  !or for fraction with andn
         sll   %g5,1,%g4
```

Should be

```
        .
          .
            .
    sethi %hi(0xff800000), %g5     !mask for sign and exponent with and
                                   !or for fraction with andn
         sll   %g5,1,%g4
```

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

Err. No. Exxxx

Subject Correction of code fragment

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Last Modified

Page 5–38

Table

Figure

Section 5.6 Using the SCAN Instruction

Subsection 5.6.1 Scan in Support of Software Floating Point

Location 3/4ths of the way down on page 5–38

Was

```
subcc %g2,32,%g0       !test if all significant bits lost
blu   1f               !use unsigned compare for future compatibility
sub   %g2,8,%g2        !remove effect of format's 8 leading 0's
```

Should be

```
subcc %g2,32,%g0       !test if all significant bits lost
blu   1f               !use unsigned compare for future compatibility
                       !blu same as bcs
sub   %g2,8,%g2        !remove effect of format's 8 leading 0's
```

Doc. Descript. Changes from 1994 MB86930 SPARClite User's Manual 1995

Err. No. Exxxx

Subject Correction of code fragment

Entered By Bruce McKeever

Created 4/11/95

Last Modified

Page 7–44

Table

Figure

Section 7.5 Instruction Set

Subsection

Location following formats section

Was

Syntax:

```
jmpl      reg_rs1, reg_rs2, reg_rd
jmpl      reg_rs1, immediate, reg_rd
```

Should be

Syntax:

```
jmpl      reg_rs1+, reg_rs2, reg_rd
jmpl      reg_rs1±, immediate, reg_rd
```

Doc. Descript. Changes from 1994 MB86932 SPARClite User's Manual 1995

Err. No. Exxxx

Subject Correction of typo

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Last Modified

Page B2–8

Table

Figure

Section 2.2 Programmer's Model

Subsection 2.2.5 Instruction Fault Status Register

Location bottom of page

Was

The instruction Fault Status Register is a read-only register. The bits in this regis–ter are set by hardware when an instruction_access_exception occurs and indicate the cause of the instruction_access_exception. This register is **clered** when either

Should be

The instruction Fault Status Register is a read-only register. The bits in this regis–ter are set by hardware when an instruction_access_exception occurs and indicate the cause of the instruction_access_exception. This register is **cleared** when either