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FUJITSU

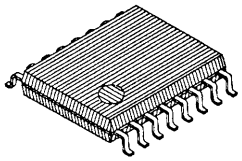
DATA SHEET

MB87093A/MB87095A/MB87096A
CMOS PLL FREQUENCY SYNTHESIZER

CMOS PLL FREQUENCY SYNTHESIZER WITH POWER SAVING FUNCTION

The Fujitsu MB87093A/MB87095A/MB87096A are CMOS Phase Locked Loop (PLL) frequency synthesizers, and are suitable for mobile telephone sets or portable telephone sets. They incorporate an N-divider (10-bit counter), a reference divider (R-divider)(6-bit reference counter), a phase comparator, a charge pump, analog switches, and an intermittent mode control circuit.

A power save control input pin (PS) for the intermittent mode control circuit is used to switch between the standby and active modes. This function reduces a system's total power dissipation. On-chip analog switches enable the switching of the time constants of low-pass filters (LPF). The MB87093A/MB87095A/MB87096A have different divide ratios of R-dividers and N-dividers from each other. Other functions and characteristics are common.



(FPT-16P-M05)

FEATURES

- Single power supply voltage: V_{DD} = 4.5 to 5.5V
- Intermittent mode control circuit
- Wide ambient temperature range: T_A = –40°C to 85°C
- On-chip two analog switches
- Plastic 16-pin SSOP package (Suffix: –PFV)
- $\underline{fin} = (\underline{Rin} / \underline{R}) \times \underline{N}$
  ($\underline{fin}$) Output frequency of an external voltage controlled oscillator (VCO)
  ($\underline{Rin}$) Reference frequency
  ($\underline{R}$) Divide ratio of R-divider
  ($\underline{N}$) Divide ration of N-divider

Part No.	Divide ratio R	Divide ratio N
MB87093A	64	725
MB87095A	64	550
MB87096A	128	750

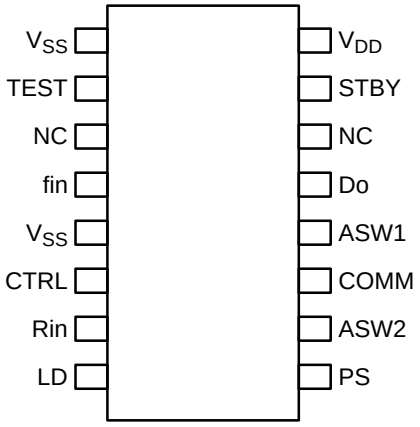
ABSOLUTE MAXIMUM RATINGS (see Note)

(V_{SS} = 0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +6.0	V
Input voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output current	I_{OUT}	±10	mA
Ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{STG}	–40 to +125	°C
Power dissipation	P_D	300	mW

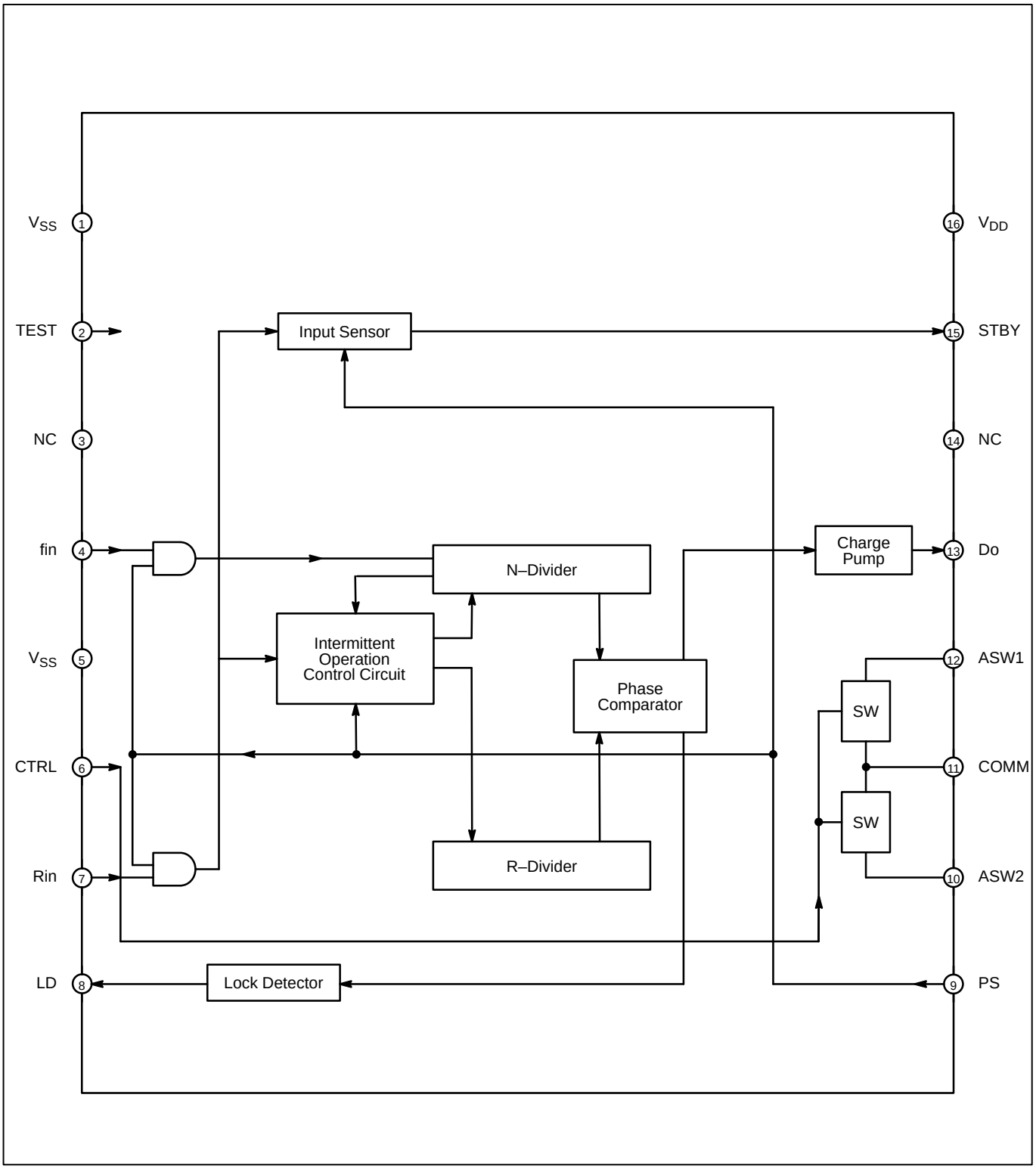
Note : Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Pin Description
1	V_{SS}	–	Ground pin
2	TEST	I	Test mode pin. Leave this pin open for ordinary operation, because pull-down resistor is included.
3	NC	–	No connection
4	fin	I	N-divider input pin, and has a bias circuit and an amplifier. Connection with an external oscillator should be AC coupling.
5	V_{SS}	–	Ground pin
6	CTRL	I	Control signal input pin for the analog switches.
7	Rin	I	Reference divider input pin, and has a bias circuit and an amplifier. Connection with an external oscillator should be AC coupling.
8	LD	O	Lock signal output pin. This pin is high when a loop is locked. This pin is low when the loop is out of lock.
9	PS	I	Power save control pin. When PS is high, an active mode is selected. When PS is low, a standby mode is selected.[1]
10	ASW2	–	Analog switch 2.
11	COMM	–	Common pin of the analog switches.
12	ASW1	–	Analog switch 1.
13	Do	O	Tri-state output pin of the charge pump. The charge pump output level is changed according to combination of the R-divider output frequency fr and the N-divider output frequency fv.
14	NC	–	No connection
15	STBY	O	This pin outputs low when the standby mode is selected. When a signal is input to Rin pin after the active mode is selected, this pin outputs high.
16	V_{DD}	–	Power supply pin.

Note: [1]Refer to an intermittent operation in functional description in page 4.

FUNCTIONAL DESCRIPTIONS

1 Intermittent Operation

The intermittent operation of every MB87093A/MB87095A/MB87096A refers to the process of activating and deactivating its internal circuit for saving power dissipation. If the circuit is simply restarted from the standby state, however, an excessively large error signal might be generated, resulting in an out-of-synch lock frequency. Because the phase relationship between the reference frequency (fr) and the frequency (fv) is not stable even when they are of the same value.

To preclude this problem, every MB87093A/MB87095A/MB87096A has an intermittent mode control circuit which forces the frequencies fr and fv into the same phase other than when the MB87093A/MB87095A/MB87096A are reactivated, this minimizing the error signal and resultant lock frequency fluctuations. The intermittent mode control circuit is controlled by the PS pin. Setting the PS pin high provides the active mode, and setting the PS pin low provides the standby mode and places the MB87093A/MB87095A/MB87096A into the standby state.

The MB87093A/MB87095A/MB87096A must be placed in the standby mode (PS = “L”) when power is impressed.

2 Input sensor

The STBY pin outputs in the standby mode, and outputs high after receiving a signal via Rin pin when the mode switches from the standby mode into the active mode.

For example, it is possible to control a VCO by this function.

3 N-divider

The fvco of an external VCO output signal input through fin is divided by the N-divider and then output to the phase comparator as fv. It consists of a binary 10-bit N-counter. The divide ratio N of the N-divider for each MB87093A/MB87095A/MB87096A is shown in Table 1.

Table 1. N-divider’s Divide Ratio N

Part Number	Divide Ratio N
MB87093A	725
MB87095A	550
MB87096A	750

4 R-divider

The R-divider divides the reference oscillation frequency (fosc) from an external reference oscillator (TCXO), and output fr to the phase comparator. It consists of a binary 6-bit R-counter. Table 2 shows the R-divider’s divide ratio.

Table 2. R-divider’s Divide Ratio R

Part Number	Divide Ratio R
MB87093A	64
MB87095A	64
MB87096A	128

5 Phase Comparator

The phase comparator detects the phase difference between the outputs fr and fv and generates an error signal that is proportional to the phase difference. The outputs from the phase comparator include 1) Do which takes one of the three states; namely, “L” (Low), “H” (high), and “Z” (high-impedance), 2) LD which indicates the PLL lock or unlock state.

5.1 Phase Comparator

The phase comparator detects the phase difference between fr and fv and generates an error signal that is proportional to the phase difference. Table 3 shows logical levels of Do and LD according to the phase relationship between fr and fv.

Table 3. Phase Comparator Inputs/Output Relationships

Phase Relationship	Output	
	Do	LD
fr > fv	H	L
fr = fv	High-Impedance	H
fr < fv	L	L

5.2 Phase Comparator Input/Output Waveforms

The phase comparator outputs logical levels summarized in Table 3. The pulse width of the phase comparator outputs are identical and equal to the phase difference between fr and fv as shown in Figure 1.

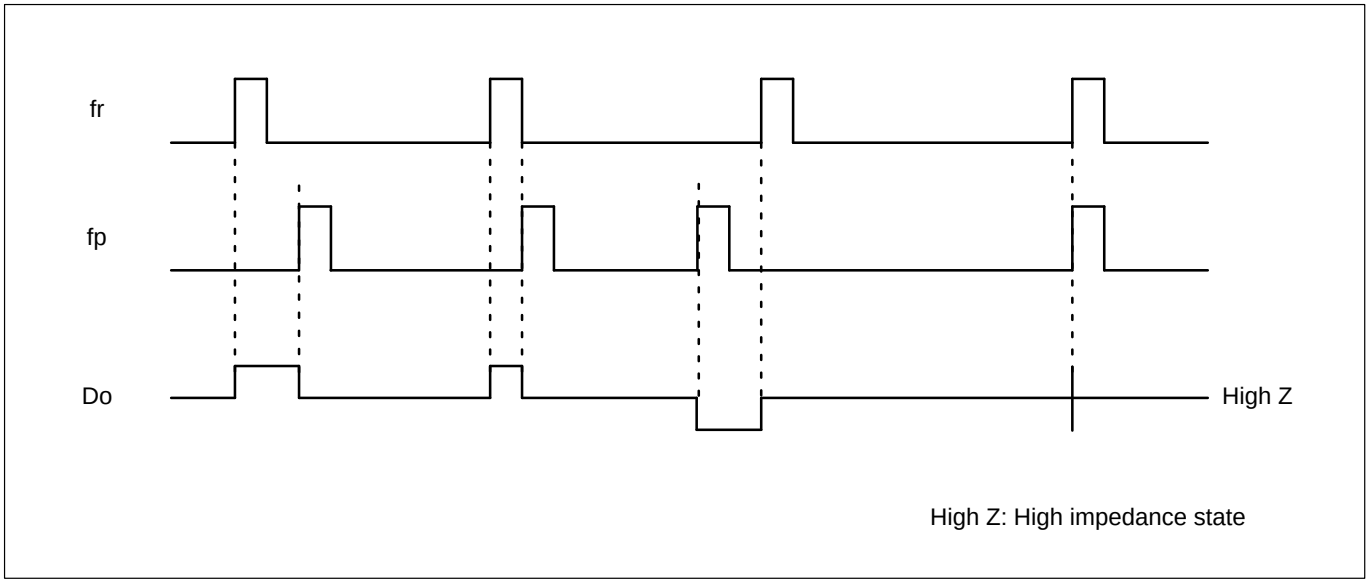


Figure 1. Phase Comparator Input/Output Waveforms (Charge Pump)

5.3 Lock Detector

The lock detector detects the lock and unlock states of the PLL. The lock detector outputs high when the PLL enters the lock state and outputs low when the PLL enters the unlock state as shown in Figure 2. When pulse width of the error signal is kept zero for four (4) clocks, the lock detector outputs high as a lock signal. When it detects phase difference after the PLL is locked, low is output at once. When PS is low, the lock detector outputs high compulsorily.

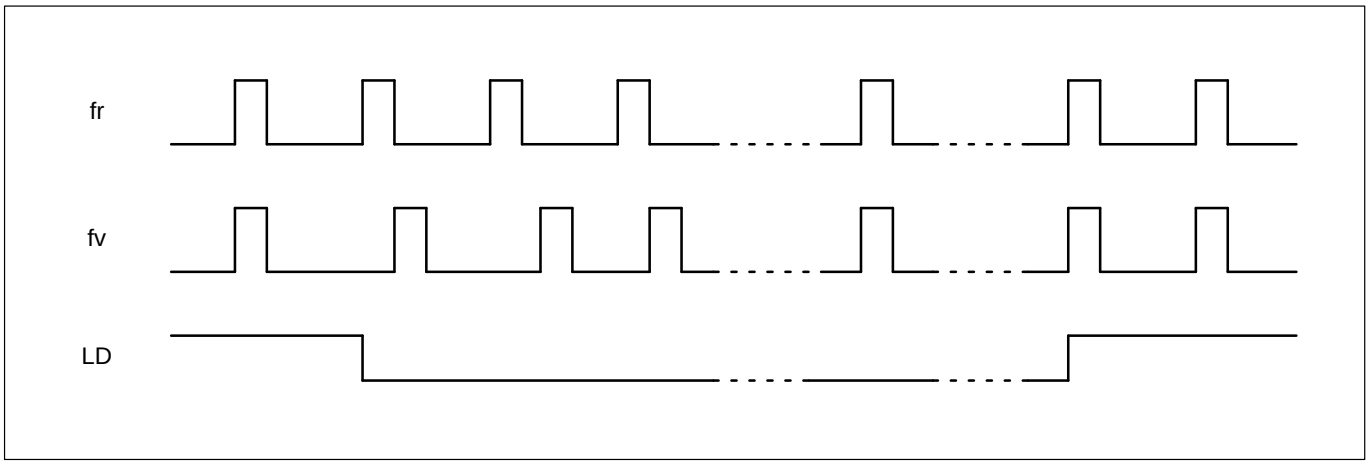


Figure 2. Phase Comparator Input/Output Waveforms (Lock Detector)

6 Analog Switch

The analog switch can be controlled by the CTRL pin. When the CTRL pin is high, each analog switch closes. When low, each analog switch opens. For example, a LPF's time constant can be changed by using a connect, as in Figure 3.

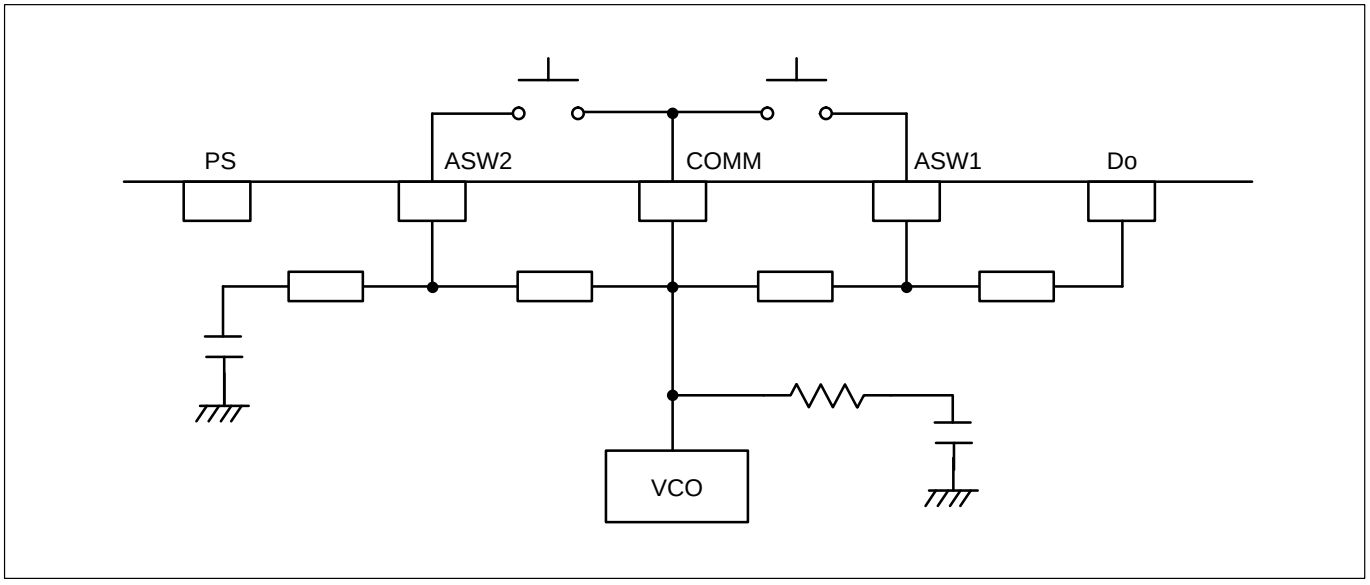


Figure 3. Application Example for Analog Switch

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	4.5 to 5.5	V
Input Voltage	V_{IN}	V_{SS} to V_{DD}	V
Ambient Temperature	T_A	–40 to +85	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_A = –40 to +85°C)

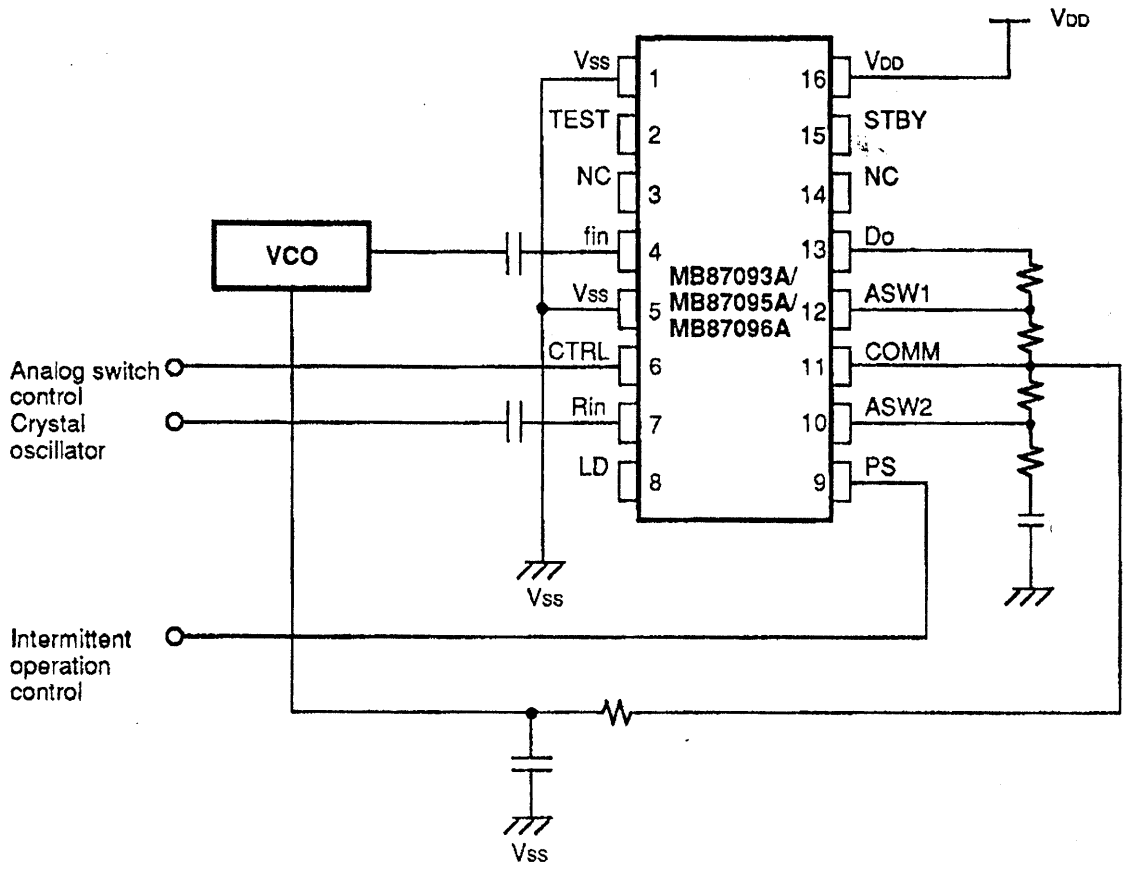
Parameter			Symbol	Conditions	Value			Unit
					Min	Typ	Max	
Input Voltage	Except fin & Rin	H Level	V_{IH}		0.7 x V_{DD}	–	–	V
		L Level	V_{IL}		–	–	0.3 x V_{DD}	
Input Sensitivity	f_{IN}		VVin	AC Coupling Amplitude	0.5	–	–	Vp–p Sine
	R_{IN}		VRin	AC Coupling Amplitude	0.5	–	–	
Input Current	Except Fin, Rin & Test	H Level	I_{IH}	V_{IN} = V_{DD}	–	–	1.0	µA
		L Level	I_{IL}	V_{IN} = V_{SS}	–	–	–1.0	
	fin Rin	H Level	I_{IH}	V_{IN} = V_{DD}	–	30	–	µA
		L Level	I_{IN}	V_{IN} = V_{DD}	–	–30	–	
Output Voltage	All outputs	H Level	V_{OH}	I_{OH} = 0µA	V_{DD} – 0.05	–	–	V
		L Level	V_{OL}	I_{OL} = 0µA	–	–	0.05	
Output Current	All outputs	H Level	I_{OH}	V_{OH} = V_{DD} –0.5V	–1.0	–	–	mA
		L Level	I_{OL}	V_{OL} = 0.5V	1.0	–	–	
Cutoff Current		Do	IZH	V_{OUT} = V_{DD}	–	1.0	–	µA
			IZL	V_{OUT} = V_{SS}	–	–1.0	–	
Supply Current		Active Mode	I_{DDOP}	*1	–	10	–	mA
		Standby Mode	I_{DDS}	*2	–	10	–	µA
Maximum Operating Frequency		REF Section	fmaxd	R-Divider	16	–	–	MHz
	MB87093A	PD Section	fmaxp	N-Divider	145	–	–	
	MB87095A	PD Section	fmaxp	N-Divider	110	–	–	
	MB87096A	PD Section	fmaxp	N-Divider	90	–	–	

Notes:

*1: MB87093A: fin = 145 MHz, Rin = 12.8 MHz, Outputs are opened.
MB87095A: fin = 110 MHz, Rin = 12.8 MHz, Outputs are opened.
MB87096A: fin = 90 MHz, Rin = 15.36 MHz, Outputs are opened.

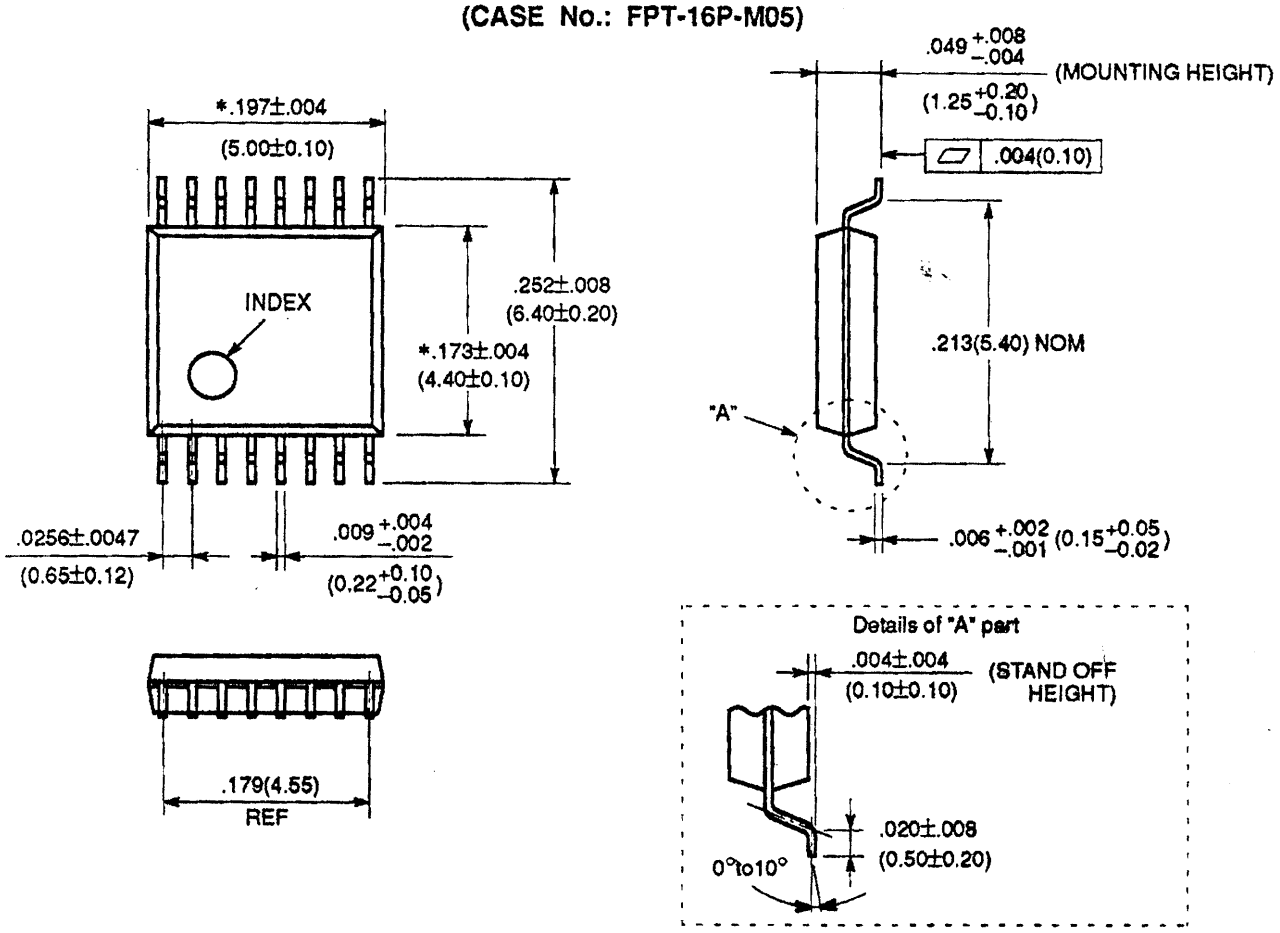
*2: Inputs set low. Outputs are opened.

TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*: This dimension does not include resin protruction.

Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete Information sufficient for construction purposes is not necessarily given.

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