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DATA SHEET

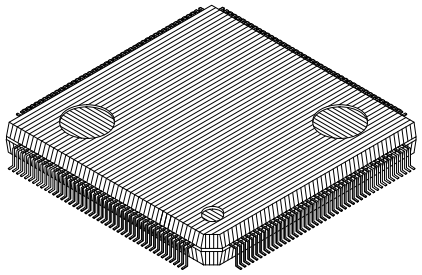
FUJITSU

MB86683B
Network Termination Controller (NTC)

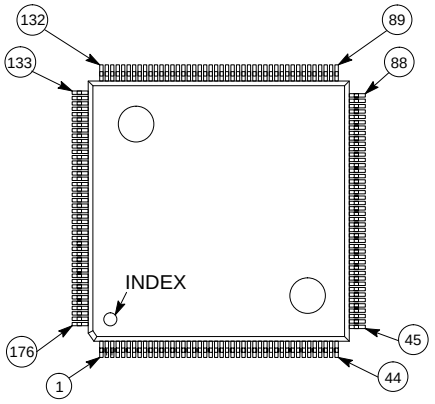
The FUJITSU MB86683B is a highly integrated termination controller for broadband ATM networks. It is designed to implement transmission convergence functions associated with physical media based on SONET (155/51 Mbps), SDH (155 Mbps), DS3 (44 Mbps), E3 (34 Mbps) and unframed protocols. The device includes a generic 8-bit parallel interface to an external transceiver, which is required only to provide serial / parallel conversion, and clock recovery.

The NTC is ideally suited to applications in ATM adapter cards and hubs. It can be used for UNI or NNI applications and conforms to the relevant ATM Forum, ANSI and ITU specifications.

PLASTIC PACKAGE
SQFP–176



PIN ASSIGNMENT



FEATURES

- Implements TC sublayer functions associated with physical media based on SONET (SDH), DS3, E3 and cell based.
- Directly connects to external transceivers via a 20MHz 8-bit parallel interface.
- Implements framed OAM functions for F1/F2/F3 flows.
- Supports F4/F5 OAM cell insertion / extraction.
- Maintains statistics for all active virtual circuits, including cell and error counts, and OAM statistics.
- Terminates serial switch statistics information provided by the MB86680 Self Routing switch Element (SRE).
- On-chip DMA controller for high speed transfer of statistics and inserted/extracted cells to/from system memory.
- Connects directly to the MB86689 Address Translation Controller (ATC) in order to provide real-time address translation in both directions.
- Microprocessor interface compatible with Motorola and Intel families of 16 and 32 bit processors.
- JTAG pins compatible with IEEE1149.1 are provided.
- Fabricated in sub-micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FIGURES (CONTINUED)

1. OVERVIEW

The NTC is a full duplex device which can be used to provide broadband termination functions in a variety of applications. Its primary use is for terminating the user or network ends of a user–network interface based on ITU–T, ANSI, or ATM Forum UNI standards.

Address translation functions, in conjunction with the MB86689A ATC, allow full flexibility for changing VPI and VCI values at either end of the link, and also allow a 24 bit routing tag to be prepended and removed.

At the user end of a UNI connection, the address translation functions allow any incoming VPI / VCI combination to be mapped onto one of 1024 virtual connections supported by the Adaptation Layer Controller (MB86686A/7).

At the network end, address translation allows incoming cell headers to be replaced with VPI and VCI values associated with the outgoing link, and routed to the appropriate output port by means of a routing tag.

Address translation can also be performed on the outgoing link of a network connection. This function may be required, for example, to replace outgoing multicast VPI/VCI values.

Two example system configurations are illustrated in Fig. 1.

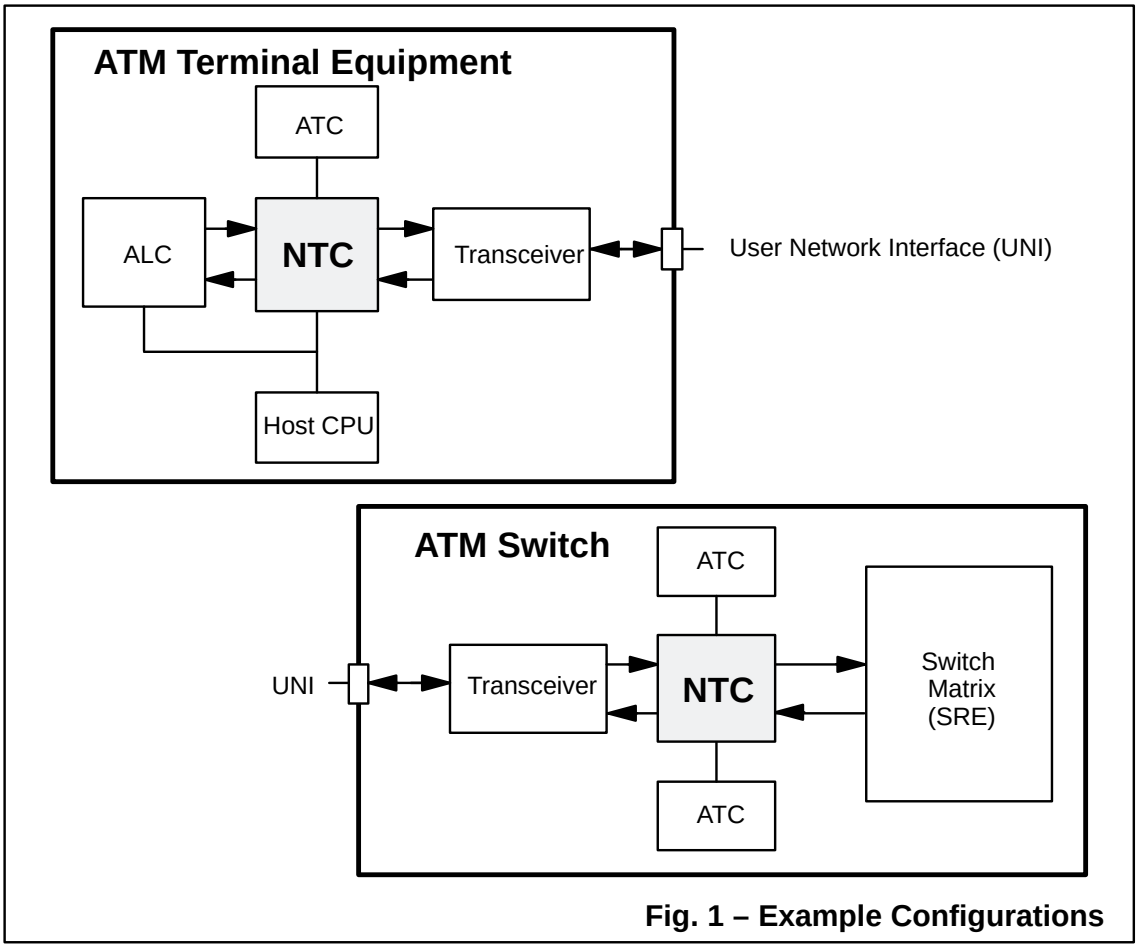


Fig. 1 – Example Configurations

2. EXTERNAL INTERFACES

2.1 Logical Outline

A logical view of the NTC's external pins is illustrated in Fig. 2 below, and a physical pin assignment diagram and table is shown in Appendix F.

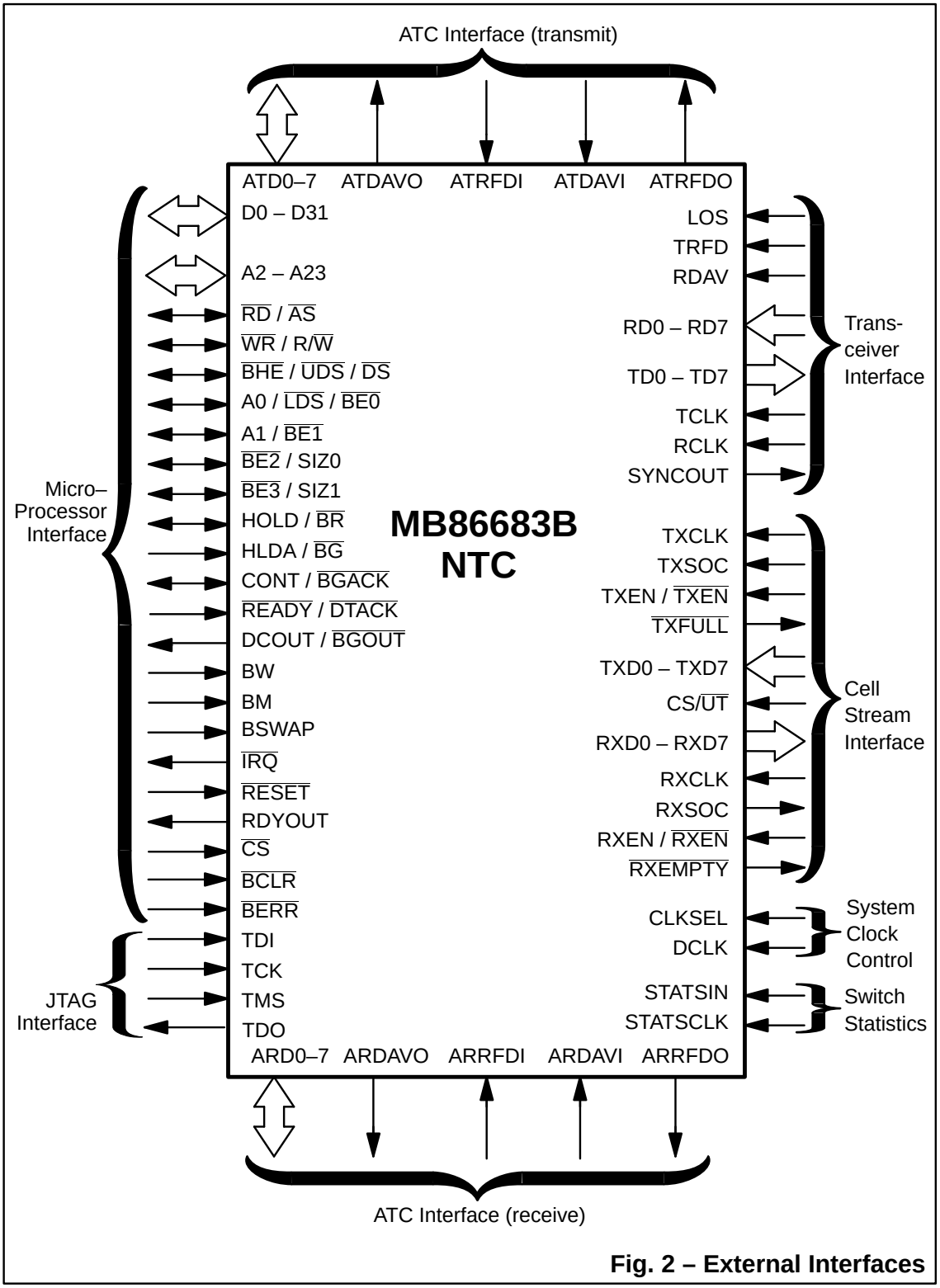


Fig. 2 – External Interfaces

2.2 Detailed Description

2.2.1 Microprocessor Interface

The microprocessor interface includes the control pins for the DMA controller. Most of these pins have multiple functions depending on the mode of operation. In all multibit cases, bit 0 is the LSB.

D0 – D31
Bi–directional 32 bit data bus.
In 16–bit mode, the upper databus is driven high.

A2 – A23
Most significant 22 bits of the 24 bit address bus. Bits A2–A6 are bi–directional; all other lines are tri–state outputs.

$\overline{\text{RD}}$ / $\overline{\text{AS}}$
Multifunction bi–directional signal. Read signal (Intel), Address Strobe signal (Motorola).

$\overline{\text{WR}}$ / R/$\overline{\text{W}}$
Multifunction bi–directional signal. Write signal (Intel), Read/Write signal (Motorola).

$\overline{\text{BHE}}$ / $\overline{\text{UDS}}$ / $\overline{\text{DS}}$
Multifunction bi–directional signal :

- Intel 16 :
  $\overline{\text{BHE}}$: High byte enable
- Motorola 16 :
  $\overline{\text{UDS}}$: Upper data strobe
- Motorola 32 :
  $\overline{\text{DS}}$: Data strobe

A0 / $\overline{\text{LDS}}$ / $\overline{\text{BE0}}$
Multifunction bi–directional signal.

- Motorola 32, Intel 16 :
  A0: Least significant address line
- Motorola 16 :
  $\overline{\text{LDS}}$: Lower data strobe
- Intel 32 :
  $\overline{\text{BE0}}$: Byte 0 enable

A1 / $\overline{\text{BE1}}$
Multifunction bi–directional signal :

- Intel 16, Motorola 16/32 :
  A1 : address bit A1
- Intel 32 :
  $\overline{\text{BE1}}$: byte 1 enable

$\overline{\text{BE2}}$ / SIZ0
Mutlifunction bi–directional signal – used in 32 bit modes to enable long word transfers.

- Intel 32 :
  $\overline{\text{BE2}}$: byte 2 enable
- Motorola 32 :
  SIZ0 : Size 0

$\overline{\text{BE3}}$ / SIZ1
Mutlifunction bi–directional signal – used in 32 bit modes to enable long word transfers.

- Intel 32 :
  $\overline{\text{BE3}}$: byte 3 enable
- Motorola 32 :
  SIZ1 : Size 1

HOLD / $\overline{\text{BR}}$
Mutlifunction bi–directional signal – Hold (Intel), /Bus Request (Motorola) are used for DMA operations.

HLDA / $\overline{\text{BG}}$
Mutlifunction input signal – Hold Acknowledge (Intel), /Bus Grant (Motorola) are used for DMA operations.

CONT / $\overline{\text{BGACK}}$
Mutlifunction bi–directional signal Control override signal in Intel mode, bus grant acknowledge signal in Motorola mode.

$\overline{\text{READY}}$ / $\overline{\text{DTACK}}$
Input signal used to control data transfer operations in Intel/Motorola modes respectively.

DCOUT / $\overline{\text{BGOUT}}$
DMA daisy chain output. This output signal is activated by the NTC when it is releasing control of the system bus. It is used when chaining NTCs, to inform other devices to stop requesting the bus. Daisy chain out in Intel mode, and bus grant out in Motorola mode.

BW
Bus width input signal. Indicates whether bus is 16 bits (0) or 32 bits (1).

BM
Bus mode input signal. Indicates whether bus is Intel (0) or Motorola (1).

BSWAP
Bus swap input signal. Used in Intel mode to allow the system bus to be configured to “Little Endian” or “Big Endian” modes. A “O” selects Little Endian mode and a “I” selects Big Endian mode.

$\overline{\text{IRQ}}$
Interrupt request, open–drain output signal active when the NTC wishes to interrupt the processor.

$\overline{\text{RESET}}$
Reset input signal, places the NTC in a reset state. This signal must be active for at least 2 system clocks, and the system clock must be active during this time. After reset, all internal control registers and most status registers will be cleared.

$\overline{\text{CS}}$
Chip select input. This pin must be set low during read/write accesses to internal NTC registers.

RDYOUT
Ready output signal. Indicates that the current register access cycle may be terminated.

$\overline{\text{BERR}}$
Bus error. This signal may be asserted by the control processor to abort any DMA transfer.

$\overline{\text{BCLR}}$
Bus clear. This signal may be asserted by the control processor to gain control of the system bus by suspending any NTC DMA transfer.

2.2.2 System Clock Interface

The internal operation of the NTC is controlled by the system clock. This clock may either be DCLK or RXCLK. The ATC external interfaces and the microprocessor/DMA external interfaces use the system clock as a reference. The other interfaces synchronise data using their respective clocks.

The system clock must be the highest frequency clock entering the NTC. All other clocks must either be from the same source or at a lower frequency.

DCLK
Optional system clock input. If DCLK is selected, then all internal operations are synchronised to this clock.

This clock allows system bus operations such as DMA transfer to be done more quickly, if using a slow cell stream clock (RXCLK). If this pin is not used, then it should be tied high or low.

CLKSEL
Clock select input pin used to select either RXCLK or DCLK as the system clock.

If this pin is unconnected, an internal pull–up resistor selects RXCLK as default. Tying this pin low selects DCLK.

2.2.3 Cell Stream Interface

The cell stream interface is used to carry cells between the NTC and devices such as an adaptation layer device (ALC) or a switch matrix (SRE).

This interface may be configured either as level 1 UTOPIA, or as Fujitsu cell stream. In all multibit cases, bit 0 is the LSB.

CS / $\overline{\text{UT}}$
Cell Stream or UTOPIA mode select. If this is unconnected, an internal pull–up resistor selects Fujitsu Cell Stream as default. Tying this pin low selects UTOPIA.

RXD0 – RXD7.
These 8 output signals provide 8 bit parallel receive path data.

RXSOC
Receive start of cell output. This output indicates that the first byte of an ATM cell (or routing tag) is available on the RXD0 – RXD7 data lines. This signal is not periodic, since its frequency is dependent on the assigned cell rate.

RXCLK
Receive path data is clocked out on the falling edge of this clock in cell stream mode, and on the rising edge in UTOPIA mode. It can be of an arbitrary frequency which is less than or equal to the system clock frequency, but should be as close as possible to the value as determined by the physical data rate / protocol. It may also be the system clock, depending upon the setting of CLKSEL. A nominal frequency of 20MHz would be used.

RXEN / $\overline{\text{RXEN}}$
Receiver enable. This input signal is used to control data flow in the receive path of the cell stream interface. It is active low for UTOPIA mode.

$\overline{\text{RXEMPTY}}$
Receiver empty. This output signal is used to qualify data flow in the receive path of the cell stream interface.

TXD0 – TXD7
These 8 input signals provide 8 bit parallel transmit path data.

TXSOC
Transmit start of cell input. This input is used to identify when the first byte of an ATM cell (or routing tag) is available on the TXD0 – TXD7 data lines. This signal is not periodic, since its frequency is dependent on the assigned cell rate.

TXCLK
Transmit path data is sampled on the rising edge of this clock. It can be of arbitrary frequency which is less than or equal to the system clock frequency, but should be as close as possible to the value as determined by the physical data rate/protocol. It should be the same nominal frequency as RXCLK, but no particular phase relationship is required.

TXEN / $\overline{\text{TXEN}}$
Transmitter enable. This input signal is used to qualify data flow in the transmit path of the cell stream interface. It is active low for UTOPIA mode.

$\overline{\text{TXFULL}}$
Transmit full. This output signal may be used to control data flow in the transmit path of the cell stream interface.

2.2.4 Transceiver Interface

This interface is used to transfer transmit and receive data between the NTC and an external transceiver.

All data transfers across this interface are referenced to either RCLK or TCLK, except LOS. In all multibit cases, bit 0 is the LSB.

RD0 – RD7
These 8 input signals are used to transfer data from a transceiver to the NTC.

RDAV
This signal is used to qualify data which is received on RD0 – RD7. Incoming data is ignored while RDAV is inactive.
If data qualification is not required, then this signal may be tied permanently high.

RCLK
This input signal is used to synchronise all data received on the RD0–7 and RDAV pins. The frequency must be less than or equal to the system clock frequency.

RD0–7 and RDAV data are sampled on the rising edge of this clock.

LOS
Loss of signal. This input signal is used to indicate to the NTC that the input signal has been completely lost. An internal alarm is set and an interrupt condition is generated.

This signal is not synchronised to RCLK, but is latched using the system clock.

TD0 – TD7
These 8 output signals are used to transfer data from the NTC to a transceiver.

TRFD
This input signal indicates that the transceiver is ready to receive data from the NTC. The NTC will not send any data until the transceiver indicates that it is ready by activating TRFD. When TRFD is inactive the TD0 – TD7 signals will retain their previous values. If data qualification is not required, then this signal may be tied permanently high.

TCLK
This input signal is used to synchronise all data on the TD0–7, SYNCOUT, and TRFD pins. The frequency must be less than or equal to the system clock frequency.

TD0–7 and SYNCOUT data changes on the falling edge of this clock. TRFD data is sampled on the rising edge of this clock.

SYNCOUT
Sync out signal. The function of this output depends on the framing mode selected. It may be used by external circuitry for frame / cell synchronisation.

In framed modes, it is active during the first byte of the frame.

In unframed mode, it is active during the first byte of a cell to indicate the start of the cell on the transceiver transmit interface.

2.2.5 Address Translation Controller Interface

The NTC comprises two separate interfaces for connecting to two ATCs, one each in the receive and transmit paths. These pins are denoted as :

- ARxxx : ATC receive path,
- ATxxx : ATC transmit path.

In all multibit cases, bit 0 is the LSB.

ATD0 – 7, ARD0 – 7
Eight bi–directional data lines which provide the VPI/VCI values to the ATC, and also provide the NTC with the routing tag and translated VPI/VCI values from the ATC.

The data from these pins is clocked out of the NTC on the falling edge of the system clock pin, this being either RXCLK or DCLK. Data is sampled on these pins on the rising edge of the system clock.

ATDAVO, ARDAVO
Data available output signal. Indicates that the NTC has VPI/VCI data available for translation.

These signals are generated on the falling edge of the system clock.

ATRFDI, ARRFDI
Ready for data input signal. Indicates that the ATC is ready to accept new VPI/VCI data for translation.
These signals are sampled on the rising edge of the system clock.

ATDAVI, ARDAVI
Data available input signal. Indicates that the ATC has VPI/VCI and tag data available for transmission to the NTC.

ATDAVI and ARDAVI are sampled on the rising edge of the system clock.

ATRFDO, ARRFDO
Ready for data output signal. Indicates that the NTC is ready to accept new VPI/VCI and tag data from the ATC.

These signals are generated on the falling edge of the system clock.

2.2.6 Switch Statistics Interface

This interface receives statistics information from the switch and comprises the following signals. If this interface is not used, then the STATSIN and STATSCLK inputs should be tied either high or low.

STATSIN
Switch statistics in, this input pin accepts a serial data stream of switch statistic packets which have a format similar to HDLC. This pin would be connected directly to the SRE switch matrix. Data is sampled on the rising edge of STATSCLK.

STATSCLK
Statistics clock, this clock input is used to control the data on the STATSIN input. This input may be asynchronous to any other NTC clock input, but its frequency must be less than or equal to the system clock frequency.

2.2.7 JTAG Interface

The JTAG Interface provides the control signals to carry out boundary-scan tests on the device.

If the JTAG interface is not used, then the TDI, TCK and TMS inputs should be tied high.

TCK
The TCK input pin provides the clock signal for the JTAG test logic.

TMS
The TMS input pin is sampled on the rising edge of TCK and used by the internal test logic to control test operations.

An external pull–up should be connected to this input to ensure that when this input is not driven a response identical to the application of a logical 1 results.

TDI
The TDI input pin is sampled on the rising edge of TCK and provides a data input to the internal test logic.

An external pull–up resistor should be connected to this input to ensure that when this input is not driven a response identical to the application of a logical 1 results.

TDO
The TDO output pin provides a tri–stateable serial output port through which test instructions and data from the internal test logic may be conveyed.

TDO data changes will occur on the falling edge of TCK.

When no signal is being driven through the TDO port the output pin will revert to its tri–state condition.

Immediately following power–up the TDO output pin will be in its undriven tri–state condition.

3. FUNCTIONAL DESCRIPTION

This section describes the behaviour of each major functional block within the NTC, as illustrated in Fig. 3. The descriptions contained in this section are from a user's perspective and are intended to give a detailed description of device functionality and mode of operation. The NTC consists of the following major blocks :

- Receive Framer
- Transmit Framer
- Cell Receiver
- Cell Transmitter
- Cell Stream Interface
- Operations Administration and Maintenance (OAM) Controller
- Statistics Controller
- Switch Statistics Handler
- DMA Controller
- Microprocessor Bus Interface

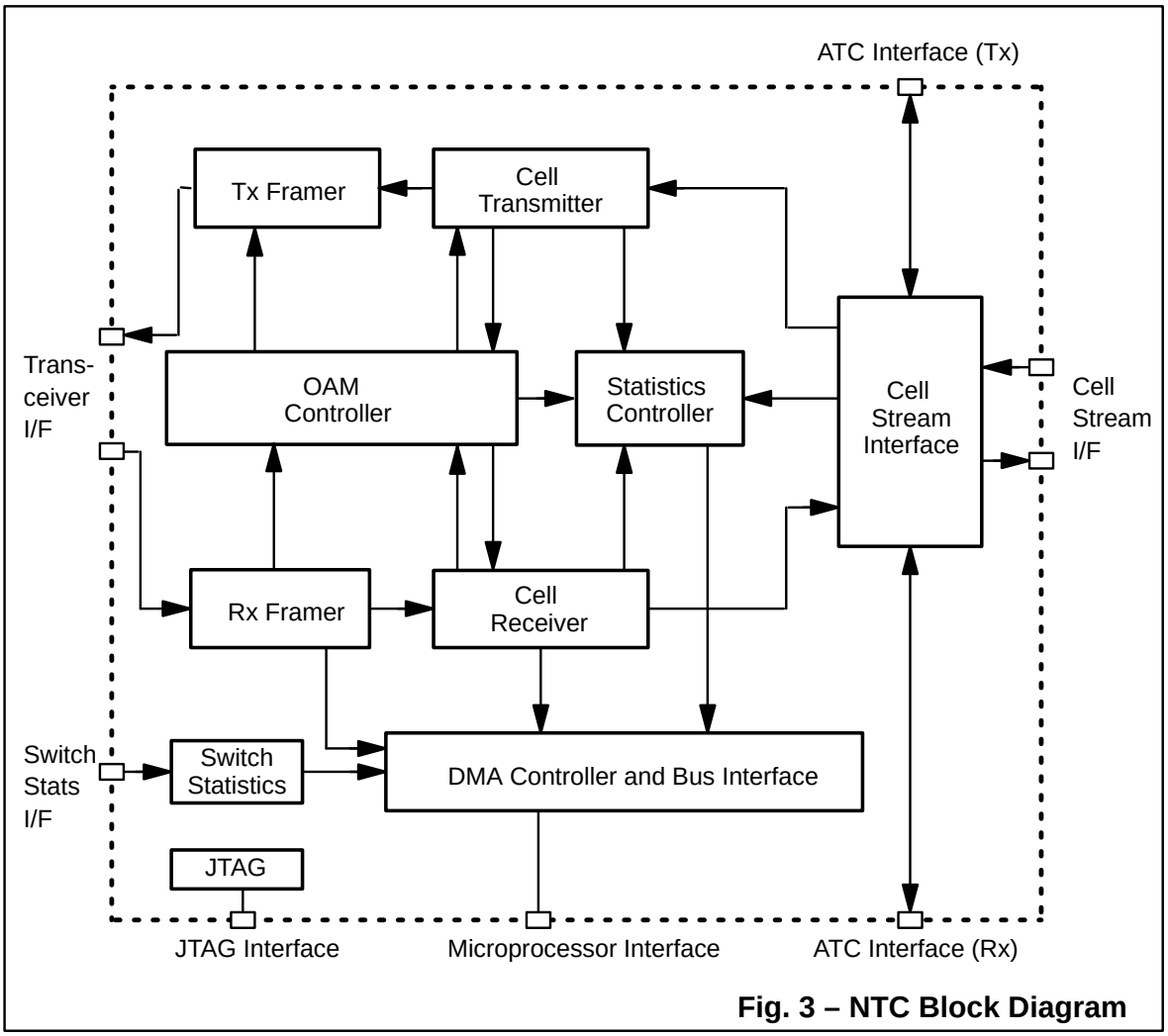


Fig. 3 – NTC Block Diagram

3.1 Basic Operation

This section describes the basic data flow through the device, both in the receive and transmit paths.

3.1.1 Receive Path

Parallel data arriving at the transceiver receive interface is first sampled by RCLK. This data is also qualified by the RDAV pin. This data need not be byte aligned. Valid and synchronised data is then passed onto the receive framer, if the device is configured in a framed mode. If in an unframed mode, this data is passed directly to the cell receiver.

Within the framer, the relevant frame synchronisation is achieved. Having achieved frame synchronisation, the frame is processed accordingly. For example in SONET, the section and path overhead information is extracted and either made available to the host via readable registers, or is processed autonomously for alarms and error monitoring bytes.

The receive framer will eventually extract the user data from the frame (eg the SPE in SONET), and pass this byte aligned data on to the cell receiver.

Any resulting OAM information is passed onto the OAM controller, and either made available to the user via Interrupts and/or status registers, or may be directly processed by the OAM controller and passed on to the transmit framer for inclusion in outgoing frames.

Data arriving at the cell receiver will normally be byte aligned. The cell receiver will first find the start of cell from the data stream, using the HEC byte in the cell header. Single bit correction of the header may also be performed.

Various different cell types will then be recognised and may be discarded and/or copied into an 4 cell extract buffer for DMA processing. Idle and other physical layer cells are discarded.

Also, cells may be inserted into the flow at a programmable peak rate via the DMA controller. This contiguous cell flow is passed onto the cell stream block, where they are initially stored in a 10 cell FIFO.

Within the cell stream block, cell payload information is extracted from the FIFO and optionally transferred to the ATC device for address translation. The returned data will contain a routing tag, along with the new header. The ATC interface also supports multicasting, by allowing multiple returned new header values from the ATC.

The cell stream block optionally calculates the new HEC value, which is required either due to address translation or due to cell insertion.

Finally, the cells are passed out of the cell stream receive interface, in accordance with either Fujitsu Cell Stream or Utopia formats. All data on this interface is synchronised to RXCLK.

The network statistics controller accepts a variety of data from all of these blocks, and records them in an internal table. This is made available to the host via DMA.

3.1.2 Transmit Path

Parallel data arriving at the cell stream transmit interface is first sampled by TXCLK. The cells are stored in a 10 cell FIFO. Address translation functions identical to those in the receive path are optionally available in the transmit path.

Cells from the cell stream are transferred to the cell transmitter block. Any routing tag that the transmit ATC may have generated is first removed as it is not required.

The function of the cell transmitter is to provide a constant stream of cells to the transmit framer, when required. This data will either be from the cell stream, or may be from a cell insert buffer filled via DMA. This is identical in operation to the insert buffer in the receive path. If no data is available from either of these sources, then idle or unassigned cells will be generated. The HEC is then calculated, which is required either due to address translation or due to cell insertion, prior to the cells being passed to the transmit framer.

The transmit framer will pack the received cells into the respective framing envelope (eg the SPE for SONET). It will also generate the relevant overhead information (eg SOH/POH for SONET), which includes all the OAM information. This will either be generated locally, or will be provided by the OAM controller, based on information from the receive framer.
Some of the transmitted overhead bytes may be provided directly by host access.

The frame is then transmitted out of the transceiver transmit interface, having been synchronised to TCLK. All transmitted data is qualified by the TRFD pin. A frame synchronisation output pin is also provided which may used by an external framing device if the framer block is transparent.

The network statistics controller accepts a variety of data from all of these blocks, and records them in an internal table. This is made available to the host via DMA.

3.2 Receive Framer

The receive framer has 7 modes of operation, namely:

- Unframed,
- SDH STM–1,
- SONET STS–3c,
- SONET STS–1,
- DS3 with PLCP,
- DS3 without PLCP,
- E3.

The required operating mode is selected via the NTC mode register CR1. The functions associated with each operating mode are described in the following paragraphs.

3.2.1 Unframed

In this mode of operation the receive framer acts as a transparent link between the transceiver interface and cell receiver section. This mode of operation allows an unframed ATM cell interface to be supported, and facilitates the use of an external framing device for physical interfaces not supported by the NTC.

3.2.2 SDH STM–1

This framing mode operates at 155.52Mbps. Frame alignment functions for STM–1 include detecting the start of an STM–1 frame, detecting the start of the VC–4 payload using the AU–4 pointer, and extracting a byte stream containing ATM cells. The cells are then passed to the cell receiver function.

An STM–1 frame is delimited by frame alignment bytes in the section overhead (A1, A2). The frame alignment bytes are repeated 3 times in the sequence A1, A1, A1, A2, A2, A2, as shown in Fig. 4. Frame alignment is assumed if the frame alignment sequence is detected in N consecutive frames, and frame alignment is assumed to be lost if the pattern is incorrect in P consecutive frames. The parameters N and P can be programmed by the user within the range 1 to 15 in CR1.

After frame alignment has been detected, the data is de-scrambled using the polynomial : $1 + x^6 + x^7$ (except for the first 9 bytes of the SOH), and the AU–4 pointer value is used to identify the start of the VC–4 container. C–4 container bytes are extracted and passed to the cell receiver.

The SOH/POH bytes shown shaded in Fig. 4 are latched into registers within the receive framer and hence are available for reading directly by the processor (SR2–17). The SOH/POH bytes from one frame are latched at the start of the following frame.

The STM–1 receive framer performs performance monitoring and fault detection for STM–1 frames using the Bit Interleaved Parity (BIP) bytes.

These include the following:

- Regenerator Section error monitoring using a BIP–8 code in the B1 byte position,
- Multiplex Section error monitoring using using a BIP–24 code in B2 byte positions,

- Path error monitoring using a BIP–8 code in B3 byte position.

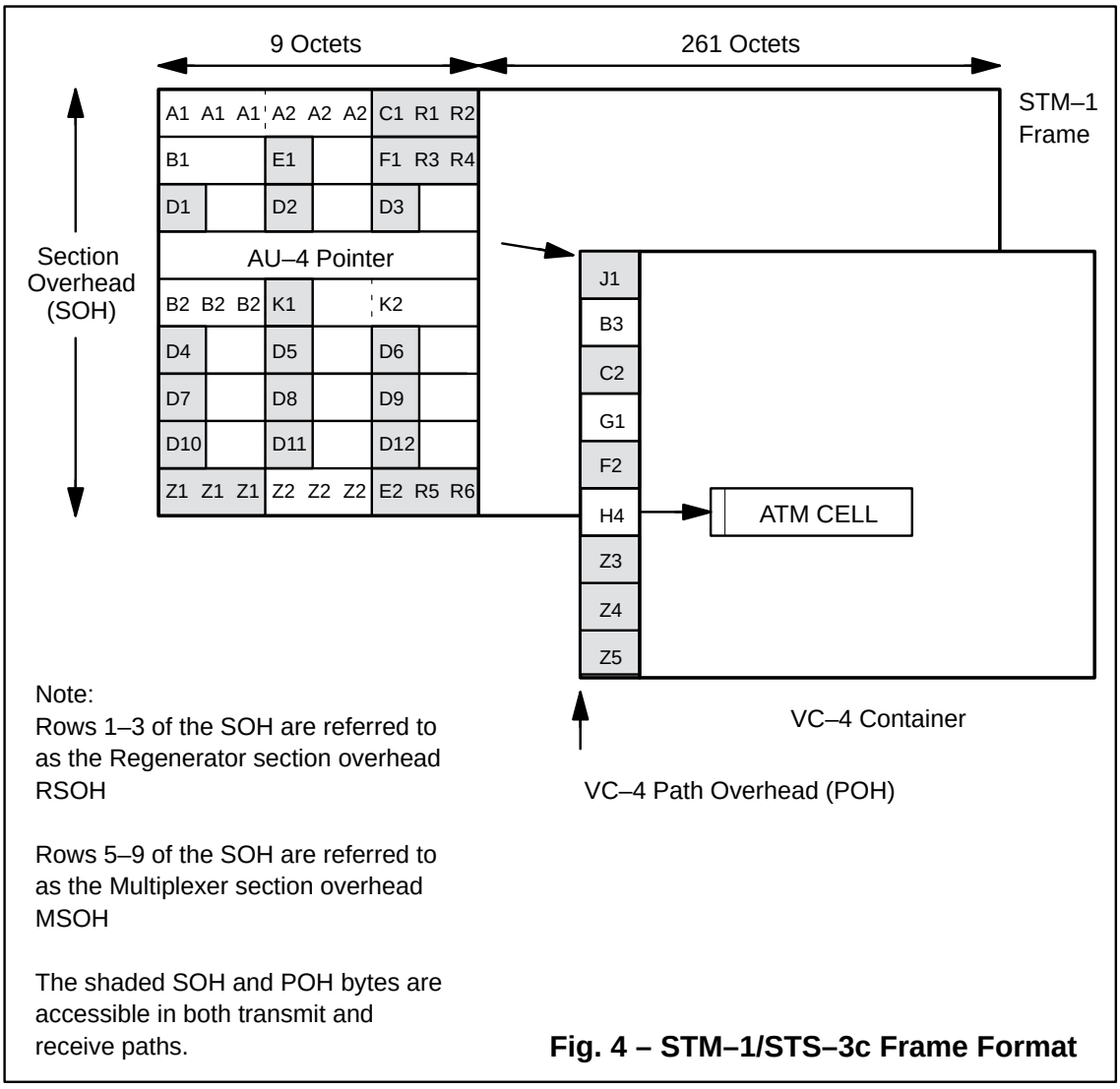


Fig. 4 – STM–1/STS–3c Frame Format

Any detected errors from the BIP checks are passed to the OAM controller. In addition, the receive framer detects and reports the following conditions, which are also passed to the OAM controller. These received conditions are made available in SR59 :

- Received B1 BIP error
- Received B2 BIP error
- Received B3 BIP error
- MS–AIS (received K2 field)
- MS–FERF (received K2 field)
- Path AIS (all 1's in AU–4 pointer)
- Path FERF (received G1 field)
- Positive pointer justification event
- Negative pointer justification event
- New data flag event

The receive framer extracts the received Far End Block Error (FEBE) bytes from the frame and provides these to the statistics controller for recording. The B2 FEBE is contained in bits 20–24 of the Z2 field, and the B3 FEBE is contained in bits 1–4 of the G1 field. There is no B1 FEBE value.

The receive framer generates the following maskable interrupts to the microprocessor:

- Loss Of Signal (LOS),
- Loss Of STM–1 Frame (LOF),
- Loss Of AU–4 Pointer (LOP),
- Start Of Frame (SOFRX),
- Start Of VC–4 Container (SOVRX).

The SOFRX and SOVRX interrupts may be used to control the timing for reading the extracted SOH/POH bytes. For example, a SOFRX interrupt indicates that the previous frame SOH bytes have all been latched, and will be stable for 125μs, until the next frame. Similarly for the SOVRX and POH bytes.

3.2.3 SONET STS–3c Mode

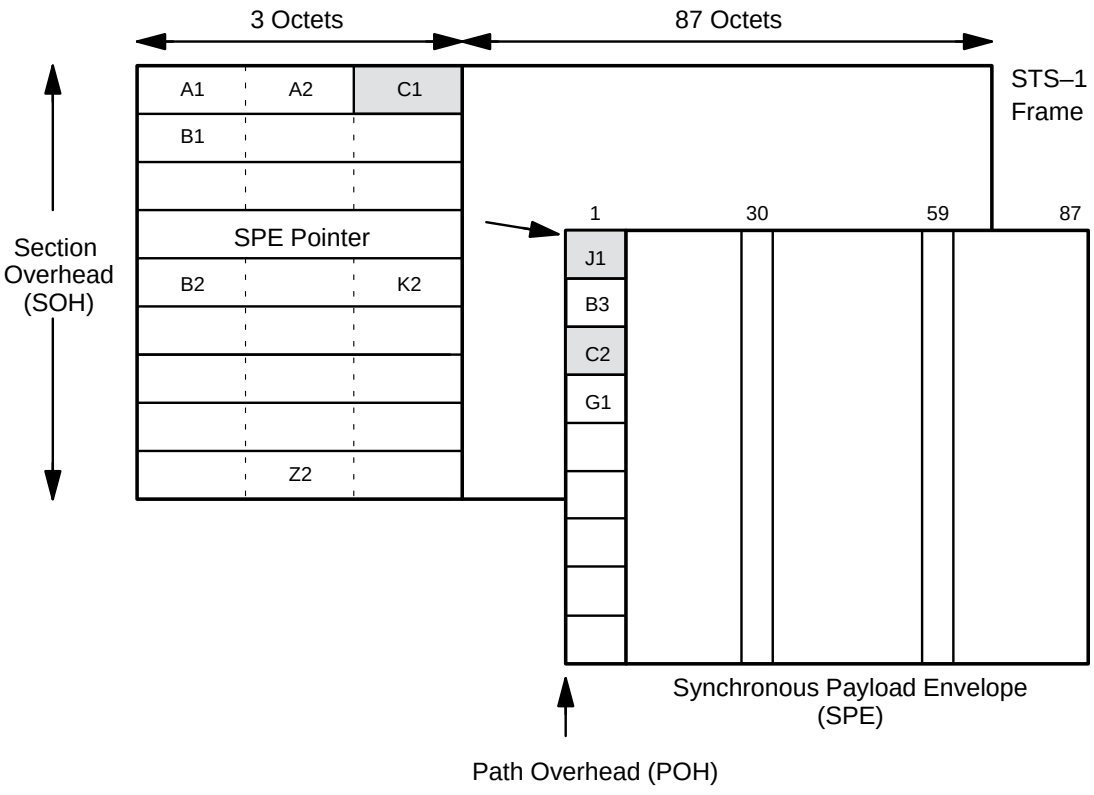
This mode is almost identical to the SDH STM–1 mode. The few differences are in the SOH and POH bytes, which are described in the transmit framer section.

3.2.4 SONET STS–1 Mode

This framing mode operates at 51.84Mbps. The frame structure is almost identical to one third of the SONET STS–3c frame structure.

The STS–1 Frame format is shown below in Fig. 5.

Frame section and path detection and generation are equivalent to STS–3c. Error detection and monitoring are also similar.



Note:

Columns 30 and 59 of the SPE contain stuff bits. They are coded as 00.

Fig. 5 – STS–1 Frame Format

3.2.5 DS3 Mode with PLCP

In this mode the receive framer first synchronises to the 44.736Mbps DS3 frame, as defined in CCITT G.752 and illustrated in Fig. 6, and then synchronises to the physical layer convergence protocol (PLCP) frame as defined in the ATM Forum UNI specification, illustrated in Fig. 7. ATM cells are then extracted and passed to the cell receiver.

The Z1–Z6 PLCP frame overhead bytes are stored in registers and made available for reading by the processor.

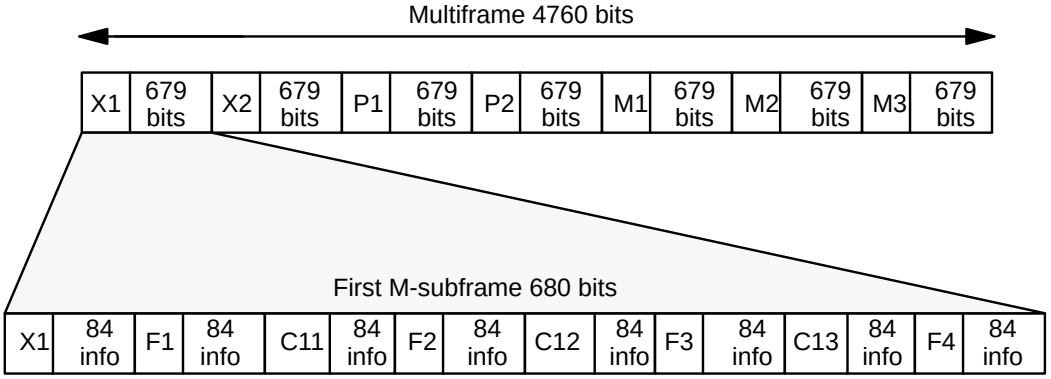
Each DS3 multi-frame contains 4760 bits, and is divided into seven M-subframes of 680 bits. Each M-subframe is further divided into 8 blocks of 85 bits, 1 bit for overhead and 84 bits for payload.

The PLCP bytes are contained within the 84 information bits of each block in each subframe.

The 125µs PLCP frame occupies more than one 107µs DS3 frame, but the PLCP bytes are nibble aligned to the DS3 frame. Nibbles begin after the control bits X, F, P, C and M.

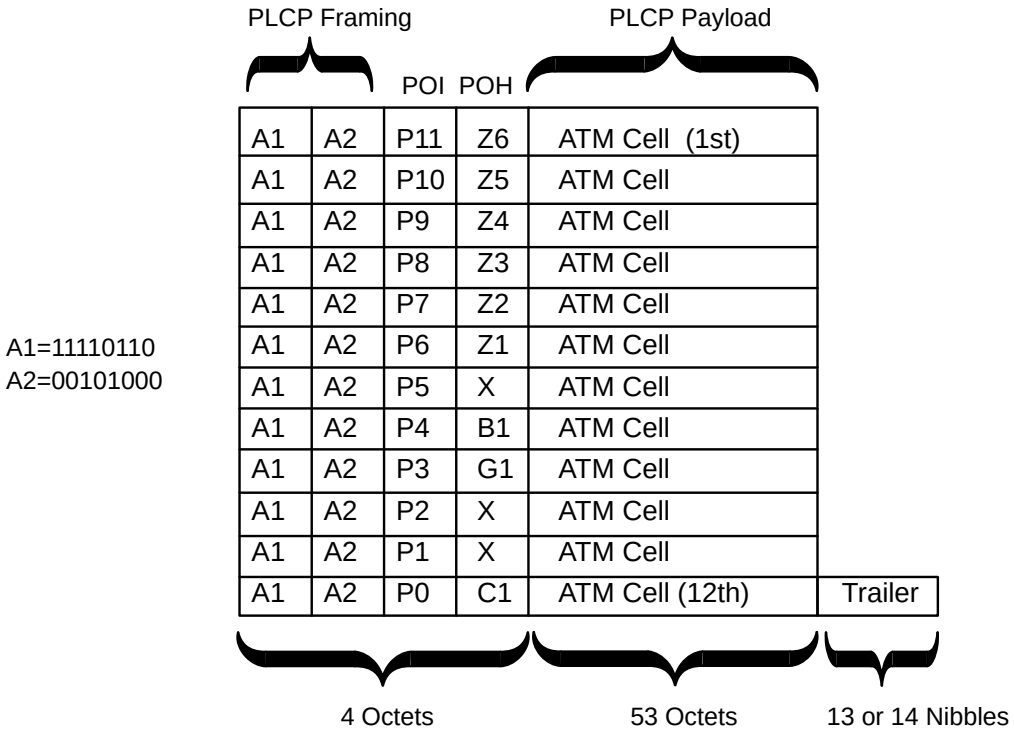
The receive framer checks the B1 field using a BIP–8 code and will report a BIP–8 error count to the OAM controller.

The receive framer also detects PLCP path status using the G1 subfield, and will pass the associated data to the OAM controller.



56 Overhead bits sequential positions							
X1	F1	C11	F2	C12	F3	C13	F4
X2	F1	C21	F2	C22	F3	C23	F4
P1	F1	C31	F2	C32	F3	C33	F4
P2	F1	C41	F2	C42	F3	C43	F4
M1	F1	C51	F2	C52	F3	C53	F4
M2	F1	C61	F2	C62	F3	C63	F4
M3	F1	C71	F2	C72	F3	C73	F4

Fig. 6 – DS3 Frame Format



Path Overhead Identifier Table:

POI	POI Code	POH
P11	00101100	Z6
P10	00101001	Z5
P9	00100101	Z4
P8	00100000	Z3
P7	00011100	Z2
P6	00011001	Z1
P5	00010101	X
P4	00010000	B1
P3	00001101	G1
P2	00001000	X
P1	00000100	X
P0	00000001	C1

Note:
The shaded POH bytes are processor accessible in both transmit and receive paths.

Fig. 7 – PLCP Frame Format

The DS–3 receive framer performs the following functions:

- DS3 frame alignment through detection of the M-subframe alignment signal F1/F2/F3/F4 consisting of 1001, and detection of the multiframe alignment pattern M1/M2/M3 consisting of 010, and then extraction of each 84-bit information payload of every M-subframe,
- Extraction of the PLCP payload and POH bytes by aligning to the PLCP framing and POI bytes,
- Extraction of the ATM cells, which will be forwarded to the cell receiver for cell delineation.
- B1 error and path status monitoring, together with FEBE and RAI reporting to OAM controller,

Any detected error from the BIP check is passed to the OAM controller and may be read by the processor using the physical layer alarms received status register (SR59).

In addition, the receive framer detects and reports the following fault conditions, which are also passed to the OAM controller and then made available in SR59:

- RDI (received G1 field).

The receive framer extracts the received Far End Block Error (FEBE) byte from the frame and provides this to the statistics controller for recording. The FEBE is contained in the G1 field.

The receive framer generates the following maskable interrupts to the microprocessor:

- Loss Of Signal (LOS),
- Loss Of DS–3 Frame (LOF),
- Loss Of PLCP Frame (LOP),
- Start Of DS–3 Frame (SOFRX),
- Start Of PLCP Frame (SOVRX).

The SOVRX interrupt may be used to control the timing for reading the extracted POH bytes. For example, a SOVRX interrupt indicates that the previous PLCP POH bytes have all been latched, and will be stable for 125μs, until the next frame.

3.2.6 DS3 without PLCP

DS3 framing is equivalent to DS3 with PLCP. The data extracted from the DS3 frame is passed directly to the cell receiver without further processing. Error detection and monitoring for the DS3 frame is the same as DS3 with PLCP.

3.2.7 E3 Mode

In this mode, the data rate is defined as 34.368Mbps, and each 125μs frame contains 537 bytes consisting of 7 octets for generic path overhead and 530 octets of payload, as shown in Fig. 8.

The bytes within the ATM cells are octet aligned with the payload, but each received frame does not necessarily contain 10 complete cells, ie ATM cells may cross a 125μs boundary.

The shaded bytes shown are available for reading by the processor.

In this mode the framer performs the following functions:

- Frame alignment through detection of a frame delimiter pattern contained in FA1 / FA2,
- Extraction of the path overhead bytes for OAM error monitoring, performance monitoring, and network communication,
- Extraction of the payload bytes, which will be forwarded to the cell receiver for cell delineation and descrambling.

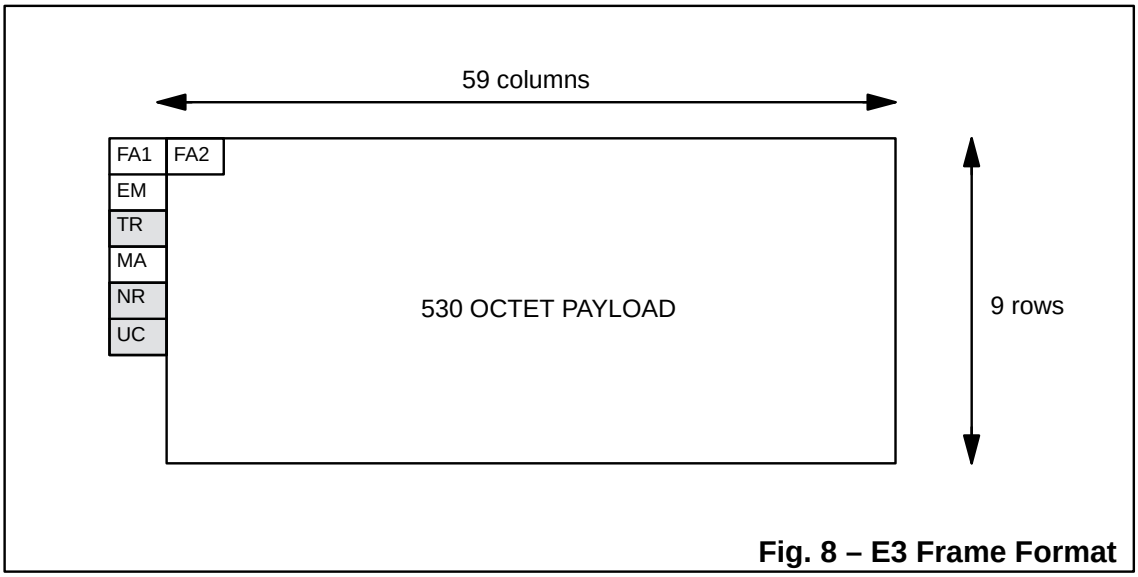


Fig. 8 – E3 Frame Format

3.2.8 Transceiver Receive Interface

The transceiver receive interface allows the transfer of 8-bit parallel data from a transceiver to the receive framer of the NTC. The data is validated using the RDAV active high signal. If this signal is inactive, then no data will be clocked into the NTC. Input data is be sampled on the rising edge of RCLK.

The frequency and phase of RCLK may be arbitrary, relative to the system clock , but its frequency must be less than or equal to the system clock. The RD[0:7] and RDAV signals are internally synchronised to the system clock.

The basic timing of these signals is illustrated in Fig. 9.

In addition to the data control signals, there is also a Loss of Signal (LOS) input. This signal would normally be generated by the opto-electrical device, to indicate that the received signal has been lost due to the power level of the signal being below a threshold. This active high signal may be used to generate an interrupt to the processor. Additionally, it will generate an alarm condition, which may be sent back to the transmitting device via the Transmit Framer. LOS input is not internally latched using RCLK, but is synchronised to the system clock. Hence an interrupt will be generated even in the absence of RCLK.

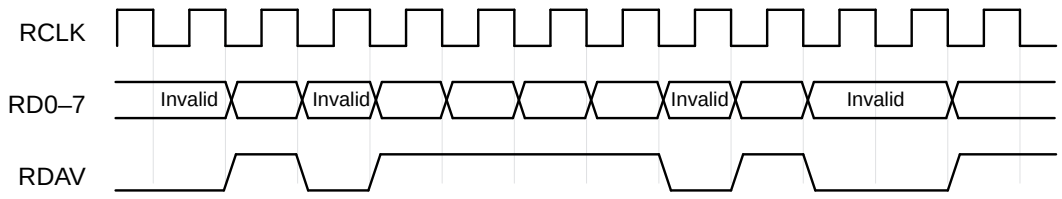


Fig. 9 – Transceiver Receive Interface Timing

3.3 Transmit Framer

The transmit framer operates in the same modes as the receive framer and generates outgoing frame patterns in accordance with the relevant framing mode. Various minor aspects appropriate to the various media are described below.

Some of the overhead bytes are controlled according to data obtained from the OAM controller. The other normally redundant bytes will take the values stored in processor accessible registers. All of these bytes are set to 0 by the NTC as default, and hence some will be required to be set to their appropriate values at configuration. The transmit framer will generate an interrupt to the processor to indicate start of frame. This signal may be used to synchronise the writing of the overhead bytes.

When used in framed modes, the transmit framer inserts outgoing alarms according to data received from the OAM controller. These alarms may optionally be ignored or accepted. Alarm conditions may also be forced, irrespective of the indication from the receive path.

3.3.1 SDH / SONET Modes

The transmit framer transmits data in STM–1/STS–3c or STS–1 frames as illustrated in Fig. 4 or Fig. 5. However, transmitted data is synchronised to the SDH clock, and hence the AU–4 pointer will be set to 522, indicating that the VC–4 container is always aligned to the STM–1/STS–3c payload. The H4 pointer within the VC–4 container is updated for each frame to indicate the position the next ATM cell header.

Section and path overhead bytes are controlled as detailed below:

C1 byte
Normally set to 00000001
(processor accessible).

R1–R2 bytes (Reserved)
Normally set to 10101010 (for SDH).
Normally set to 00000010 and 00000011 (for SONET)
(processor accessible).

B1 byte
This byte will be set according to a BIP–8 code calculated over all bits of the previous frame after scrambling. The value will be inserted in the current frame before scrambling.

E1 byte
Normally set to 00000000
(processor accessible).

F1 byte
Normally set to 00000000
(processor accessible).

R3–R6 bytes (Reserved)
Normally set to 00000000
(processor accessible).

D1–D3 bytes
Normally set to 00000000
(processor accessible).

24 bit AU–4 pointer value
H1 (bits 1 to 4) set to 0110 (NDF = invalid).
H1 (5–6) set to 10 (ie SS = 10) (for SDH).
H1 (5–6) set to 00 (ie SS = 00) (for SONET).
H1,H2 (7–16) set to 522 (VC4 starts after R2 byte).
H3 (17–24) set to 0.

B2 bytes
These 3 bytes will be set according to a BIP–24 code calculated over all bits of the previous frame, except for the first 3 rows of section overhead. The code will be calculated before scrambling, and will be inserted in the current frame before scrambling.

K1 byte
Normally set to 00000000 (processor accessible).

K2 byte
This byte will be set to indicate line AIS and FERF conditions as indicated by the OAM controller. The byte will be encoded as follows. Bits 1 to 5 will be set to zero. Bits 6 to 8 will be set to 111 for line AIS, 110 for FERF, and 000 in all other cases.

D4–D12 bytes
Normally set to 00000000 (processor accessible).

Z1 bytes
Normally set to 00000000 (processor accessible).

Z2 bytes
These bytes will be set to indicate the B2 FEBE error count as indicated by the OAM controller. (Bits 20–24). Other bits set to 0.

E2 byte
Normally set to 00000000 (processor accessible).

J1 byte
Normally set to 00000000 (processor accessible).

B3 byte
This byte will be set according to a BIP–8 code calculated over all bits of the previous VC–4 container before scrambling, and will be inserted in the current VC–4 container before scrambling.

C2 byte
Normally set to 00000001 (for SDH)
Normally set to 00010011 (for SONET) (processor accessible).

G1 byte
This byte will be set according to information received from the OAM controller as follows:
G1 (1–4) FEBE error count (0 to 8).
G1 (1–4) set to 1001 to indicate FERF (for SONET).
G1 (5) set to 1 to indicate P–FERF/RDI (for SDH/SONET).

F2 byte
Normally set to 00000000 (processor accessible).

H4 byte
Set to indicate the offset from itself to the start of the next ATM cell. The value will be between 0 and 52. Bits 3–8 are used for this purpose.

Z3 byte
Normally set to 00000000 (processor accessible).

Z4 byte
Normally set to 00000000 (processor accessible).

Z5 byte
Normally set to 00000000 (processor accessible).

3.3.2 DS3 Mode

In this mode ATM cells are transmitted in PLCP frames having the following attributes. Data transmission rate is synchronised to the DS3 transmission rate and hence no justification is used (ie. no nibble stuffing).

B1 byte
This byte will be set according to a BIP–8 code calculated over the PLCP payload and POH fields of the previous PLCP frame.

G1 byte
G1 (1–4) Set to indicate the FEBE count provided by the OAM controller.

G1 (5) set to 1 when RAI is indicated by the OAM controller, otherwise set to 0.

C1 byte
Set sequentially to 11111111, 00000000 and 01100110 to indicate the frame phase.

Z1–Z6 bytes
Normally set to 00000000
(processor accessible).

X bytes
Set to 00000000.

The PLCP frames will then be segmented and sent as DS3 frames.

3.3.3 E3 Mode

In this mode ATM cells are transmitted in E3 frames having the following attributes. Transmitted ATM cells will be byte aligned with the E3 frame.

The first ATM cell will appear immediately after the FA2 byte. Hence, the 530 byte payload will contain 10 complete cells.

EM byte
This byte will be set according to a BIP–8 code calculated over all the bits of the previous 125µs frame.

MA byte
This byte will contain FERF (bit 1) and FEBE (bit 2) information from the OAM controller. The payload type (bits 3 to 5) are set to 010 (ATM). The payload dependent bits (6–7) are set to 00. The Timing marker (bit 8) is set to 0.

TR byte
Normally set to 00000000
(processor accessible).

NR byte
Normally set to 00000000
(processor accessible).

UC byte
Normally set to 00000000
(processor accessible).

3.3.4 Transceiver Transmit Interface

The transceiver transmit interface allows the transfer of 8-bit parallel data from the NTC to a transceiver. The output data is controlled using the TRFD signal. If this signal is inactive, then the output data will freeze during the next clock cycle. The TRFD signal will be sampled on the rising edge of TCLK.

Output data will be clocked out of the NTC on the falling edge of TCLK. The frequency and phase of TCLK may be arbitrary relative to the system clock, but its frequency must be less than the system clock. The signals are internally synchronised to the system clock.

In addition to the data control signals, there is also a Synchronisation Output (SYNCOUT) signal. This signal may be used to control external logic for additional framing functions, either in cell–based or framed modes.

- Unframed mode :
  SYNCOUT active during first byte of the cell.
- SONET / SDH modes :
  SYNCOUT active during first frame alignment byte A1.
- E3 mode :
  SYNCOUT active during frame alignment byte FA1.
- DS–3 mode :
  SYNCOUT active at the start of the multi–frame, ie when X1 bit plus 7 info bits are being transmitted.

The basic timing of these signals is illustrated in Fig. 10. Both SYNCOUT and TD0–7 signals will be extended if TRFD is inactive.

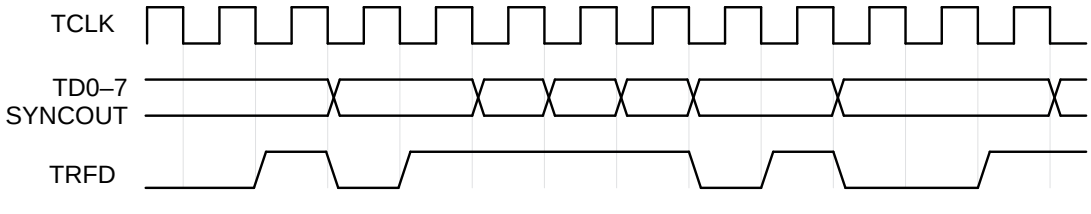


Fig. 10 – Transceiver Transmit Interface Timing

3.4 Cell Receiver

The cell receiver takes data from the receive framer and performs the following functions, generally passing data on to the cell stream interface.

- Cell delineation.
- Cell header error detection and correction.
- Cell payload descrambling.
- Cell type recognition.
- Cell rate decoupling.
- CRC-10 checking for received OAM cells.
- Cell extraction (from the transceiver interface) via DMA.
- Cell discard.
- Cell insertion (towards the cell stream interface) via DMA.

Data flow through the cell receiver is governed by the availability of data, clock-by-clock, from the transceiver interface via the receive framer.

3.4.1 Cell Reception

The cell delineation process will attempt to gain cell alignment continuously on the byte stream coming from the transceiver interface after being enabled. Cell alignment is gained by detecting DELTA correct results to the calculation of the HEC field residue at cell-spaced intervals. An interrupt (ICD) may also be generated. Between 1 and 6 cells will be lost before the first correct HEC is detected

Cell alignment is assumed lost when ALPHA incorrect results to the HEC calculation are detected. An interrupt (OCD) may also be generated.

The parameters DELTA and ALPHA are programmed in CR19 to be between 0 and 15 inclusive. Suggested values in ITU–T I.432 are DELTA = 6, ALPHA = 7 for all of the framed physical interfaces.

The HEC calculation (using the polynomial $1 + x + x^2 + x^8$) is carried out over all 8 possible bit alignments of the data coming from the transceiver interface. It is possible to specify that the data provided at the transceiver interface is byte-aligned by setting the BALIGN bit in CR19.

The modulo-2 subtraction of the pattern “01010101” from the received HEC field, before the calculation is applied, is also under user control by programming the HECMASK bit in CR19.

Once cell alignment has been gained, the header error detection and correction process is capable of detecting most headers with multiple bit errors and correcting single bit errors in alternate frames. The single bit error correction may be disabled by the user if it is not required by clearing the COREN bit in CR19. Error detection is always performed. Error detection and correction events are recorded by the statistics controller.

The cell payloads may be descrambled (using the self-synchronous descrambler with polynomial $1 + x^{43}$) by setting the DESCR bit in CR19.

3.4.2 Cell Type Recognition

The cell header VPI, VCI, PLT and CLP fields are examined to see if the cell is one of the following 12 types :

- Idle
  (VPI=0, VCI=0, PLT=000, CLP=1).
- PL–OAM F1
  (VPI=0, VCI=0, PLT=001, CLP=1).
- PL–OAM F3
  (VPI=0, VCI=0, PLT=100, CLP=1).
- Other physical layer
  (VPI=0, VCI=0, PLT=XXX, CLP=1).
- Unassigned
  (VPI=0, VCI=0, PLT=XXX, CLP=0).
- Meta signalling
  (VPI=X, VCI=1, PLT=0X0, CLP=X).
- Broadcast signalling
  (VPI=X, VCI=2, PLT=0XX, CLP=X).
- Point-to-point signalling
  (VPI=X, VCI=5, PLT=0XX, CLP=X).
- ATM–OAM F4 segment
  (VPI=X, VCI=3, PLT=0X0, CLP=X).
- ATM–OAM F4 end-to-end
  (VPI=X, VCI=4, PLT=0X0, CLP=X).
- ATM–OAM F5 segment
  (VPI=X, VCI≠0, PLT=100, CLP=X).
- ATM–OAM F5 end-to-end
  (VPI=X, VCI≠0, PLT=101, CLP=X).

For ATM–OAM cells, the first byte of the payload is further examined to classify the cell as fault management (FM), activation/de–activation (AD) or performance management (PM).

In addition to these types, ILMI cells can also be identified :
(VPI = 0, VCI = 16, PLT = XXX, CLP = 0).

The GFC field may be ignored for predefined cell type recognition by setting the GFCIGN bit in CR18.

The cell header is also compared to a user-programmed mask which may have any of the 32 header bits set to “0”, “1” or “X”. This allows cell headers to be matched which have either specific values or values in a range. The mask pattern bits are specified in CR22 & CR23 and the “don’t care” bits are specified in CR20 & CR21.

3.4.3 Cell Rate Decoupling

Idle cells (and any other physical layer cells) will not be passed on to the Cell Stream Interface.

If unassigned cells are used for cell rate decoupling, they should be discarded explicitly (see section 3.4.5).

3.4.4 Cell Extraction

Based on the recognised cell type, cells may be extracted (but not removed from the data stream) to system memory using DMA. Cells may be extracted either by specific predefined cell type or by explicitly matching (or not matching) the user mask. Cell extraction is controlled by CR24.

The extract buffer has space for four cells. Transfer of a cell by DMA will not start until the whole cell is in the buffer and the space will not be released until the whole cell has been transferred.

Extraction of OAM cells is subject to checking of the CRC-10 field. If this checking is enabled by setting the CRC10CHK bit in CR18, a cell with a CRC-10 error in the payload will not be extracted.

3.4.5 Cell Discard

Also based on the recognised cell type, cells may be discarded from the data passed to the cell stream interface, again either by specific cell type or by explicitly matching (or not matching) the user mask. Cell discarding is controlled by CR25.

3.4.6 Cell Insertion

Insertion of cells into the data stream towards the cell stream interface via DMA is carried out through a single-cell insert buffer. The peak insertion rate is controlled by the PKIR bits in CR18. These give the number of cells which must be received from the transceiver interface for each cell which may be inserted (e.g PKIR3–0 = “1000” gives an insertion rate of 1 cell inserted per 32 cells (2^{13-8}) received or approximately 3.1% of the bandwidth).

It is important to note that, in order to insert a cell in the data going to the cell stream interface, the cell being received from the transceiver interface must be deleted. This can occur if the cell being received is a physical layer cell or if the user has programmed the discard function to discard the cell, either as one of the pre-defined types or because it matches (or does not match) the user mask.

The peak insertion rate will therefore only be achieved if there are sufficient gaps (i.e. cells being discarded) in the data going to the cell stream interface, unless the INSPRI bit in CR18 is set. In this case, cells will be inserted at the maximum rate governed by the PKIR bits. When a cell is inserted, the cell being received will be lost, irrespective of whether or not it was supposed to be discarded.

The peak insertion rate will only be attained if the NTC’s DMA latency can be satisfied by the host system bus.

Since the data flow through the cell receiver is governed by the availability of data from the transceiver interface, via the receive framer, it follows that cell insertion can only occur if the receive framer is passing data.

3.4.7 OAM Cell CRC-10 Generation

If the cell inserted is recognised as an OAM cell, the CRC-10 field may be generated and placed at the end of the payload. If the CRC generation is not enabled, the data supplied from system memory will be transmitted transparently. This is controlled by the CRC10GEN bit in CR18.

3.5 Cell Transmitter

The cell transmitter takes data from the cell stream interface and performs the following functions. Data is always supplied to the transceiver interface via the transmit framer.

- Cell type recognition.
- Cell extraction (from the cell stream interface) via DMA.
- Cell discard.
- Cell insertion (towards the transceiver interface) via DMA.
- CRC-10 generation for transmitted OAM cells.
- Cell rate decoupling.
- HEC field calculation.
- Cell payload scrambling.

Data flow through the cell transmitter is governed by the ability of the transceiver interface (via the transmit framer) to accept data clock-by-clock.

3.5.1 Cell Type Recognition

The cell header VPI, VCI, PLT and CLP fields are examined to see if the cell is one of the following 8 types :

- Unassigned
  (VPI=0, VCI=0, PLT=XXX, CLP=0).
- Meta signalling
  (VPI=X, VCI=1, PLT=0X0, CLP=X).
- Broadcast signalling
  (VPI=X, VCI=2, PLT=0XX, CLP=X).
- Point-to-point signalling
  (VPI=X, VCI=5, PLT=0XX, CLP=X).
- ATM–OAM F4 segment
  (VPI=X, VCI=3, PLT=0X0, CLP=X).
- ATM–OAM F4 end-to-end
  (VPI=X, VCI=4, PLT=0X0, CLP=X).
- ATM–OAM F5 segment
  (VPI=X, VCI≠0, PLT=100, CLP=X).
- ATM–OAM F5 end-to-end
  (VPI=X, VCI≠0, PLT=101, CLP=X).

For ATM–OAM cells, the first byte of the payload is further examined to classify the cell as fault management (FM), activation/de–activation (AD) or performance management (PM).

In addition to these types, ILMI cells can also be identified :
(VPI = 0, VCI = 16, PLT = XXX, CLP = X).

The GFC field may be ignored for predefined cell type recognition by setting the GFCIGN bit in CR26.

The cell header is also compared to a user-programmed mask which may have any of the 32 header bits set to “0”, “1” or “X”. This allows cell headers to be matched which have either specific values or values in a range. The mask pattern bits are specified in CR30 & CR31 and the “don’t care” bits are specified in CR28 & CR29.

3.5.2 Cell Extraction

Based on the recognised cell type, cells may be extracted (but not removed from the data stream) to system memory using DMA. Cells may be extracted either by specific cell type or by explicitly matching (or not matching) the user mask. Cell extraction is controlled by CR32.

The extract buffer has space for four cells. Transfer of a cell by DMA will not start until the whole cell is in the buffer and the space will not be released until the whole cell has been transferred.

Extraction of OAM cells can be subject to checking of the CRC10 field. If this checking is enabled by setting the CRC10CHK bit in CR26, a cell with a CRC-10 error in the payload will not be extracted.

3.5.3 Cell Discard

Also based on the recognised cell type, cells may be discarded from the data passed to the transceiver interface, again either by specific cell type or by explicitly matching (or not matching) the user mask. Cell discarding is controlled by CR33.

3.5.4 Cell Insertion

Insertion of cells into the data stream towards the transceiver interface via DMA is carried out through a single-cell insert buffer. The peak insertion rate is controlled by the PKIR bits in CR26. This gives the number of cells which must be transmitted towards the transceiver interface for each cell which may be inserted (e.g PKIR3–0 = “0100” gives an insertion rate of 1 cell inserted per 512 cells (2^{13-4}) transmitted or approximately 0.2 % of the bandwidth).

In order to insert a cell in the data going to the transceiver interface, there must be a gap in the cells coming from the cell stream interface. This will occur if the current cell is to be discarded or if there is no cell available.

The peak insertion rate will therefore only be attained if there are sufficient gaps in the data going to the transceiver interface, unless the INSPRI bit in CR26 is set. In this case, cells will be inserted at the maximum rate governed by the PKIR bits and, each time a cell is inserted, the cell coming from the cell stream interface will be delayed by one cell time.

The higher peak insertion rates will only be attained if the NTC’s DMA latency can be satisfied by the host system bus.

3.5.5 OAM cell CRC10 generation

If the cell inserted is an OAM cell, the CRC10 field may be generated and placed at the end of the payload. If the CRC generation is not enabled, the data supplied from system memory will be transmitted transparently. This is controlled by the CRC10GEN bit in CR26.

3.5.6 Cell Rate Decoupling

An idle cell will be generated and sent to the transceiver interface for cell rate decoupling if there is no other cell to be sent.

Unassigned cells may be generated in place of idle cells by setting the UNASGEN bit in CR26.

3.5.7 Cell Transmission

When a cell is transmitted, the HEC residue is calculated (using the polynomial $1 + x + x^2 + x^8$) over the four header bytes. This will overwrite the value in the fifth byte position. The modulo-2 addition of the pattern “01010101” to the result of the HEC calculation is under user control by programming the HECMASK bit in CR27.

The cell payloads may be scrambled (using the self-synchronous scrambler with polynomial $1 + x^{43}$) by setting the SCRAM bit in CR27.

3.6 Cell Stream Interface

The Cell Stream Interface (CSI) passes ATM cells in the receive direction between the Cell Receiver and an external ATM layer device and in the transmit direction between an ATM layer device and the Cell Transmitter. The following functions are provided in both directions :

- FIFO buffering of 512 bytes (9.85 cells)
- Selectable Fujitsu cell stream or level 1 UTOPIA modes
- Cell transfer to & from ATM layer device with byte level flow control
- Address translation
- Congestion & cell loss priority indication control

3.6.1 FIFO buffers

The FIFO buffers allow rate matching between the physical layer and ATM layer cell rates. They also absorb the delay required for address translation and support multicasting by allowing cell payloads to be read more than once. The fill levels of the buffers are reported in SR57. If the buffers overflow (i.e. a cell is being written in when there is not space for one full cell left in the buffer), an interrupt (RXFIFO or TXFIFO) will be generated and the cell being written in will be lost. All other cells will be unaffected.

3.6.2 Cell Stream and UTOPIA

The Fujitsu Cell Stream mode has been superseded by the UTOPIA specification from the ATM Forum, but is still supported for backward compatibility. The mode selection is performed by tying the CS/$\overline{UT}$ pin high or low as required. By default, Fujitsu cell stream is selected by internal pull–up resistor.

3.6.3 Cell Transfer

Cells are transferred in both directions using 9-bit parallel busses. Eight of the bits are used for byte-wide data, the ninth being a synchronisation signal indicating the start of a cell transfer. Cells may be transferred contiguously or with gaps.

The first few bytes of a cell transfer may contain a routing tag intended for use with a Fujitsu Self-Routing switch Element (SRE) or other device supporting the format of the routing tag. The routing tag may vary in length between 0 and 3 bytes. This is controlled by the TAG bits in CR56. In addition, the HEC byte of the cell header (byte 5 in the cell) may be omitted from cells being transferred to and from the ATM layer by setting the OMITHEC bit in CR57. These factors give a total length for a cell transfer of between 52 and 56 bytes.

The format of the cell stream interface is shown in Fig. 11.

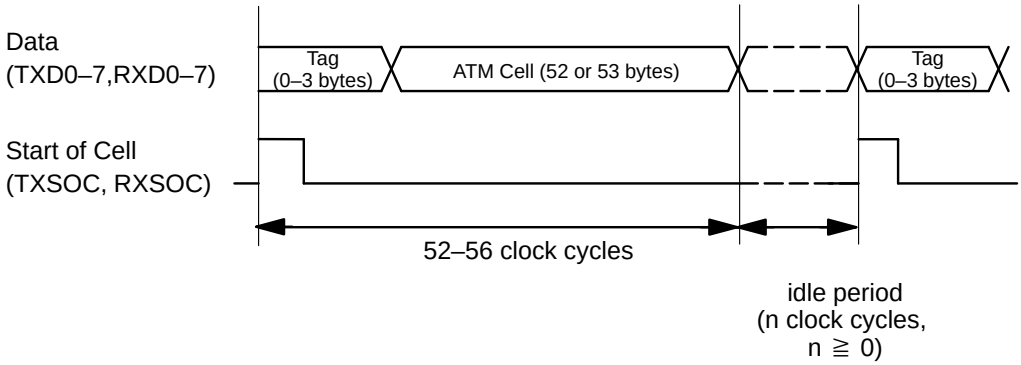


Fig. 11 – Cell Stream Format

3.6.4 Flow Control

Forward and backward byte-level flow control is supported in both directions. The forward flow control signal indicates the validity of the current data. The backward flow control signal indicates whether data will be accepted in a particular cycle. Neither flow control signal is directly qualified by the other; they can change state independently. Unused flow control inputs should tied off to the appropriate levels.

The functional timing of the transmit and receive interfaces for the cell stream timings are illustrated in Fig. 12 and Fig. 13. Similarly, timings for UTOPIA are illustrated in Fig. 14 and Fig. 15. In these diagrams, 0 clocks implies in the same clock cycle.

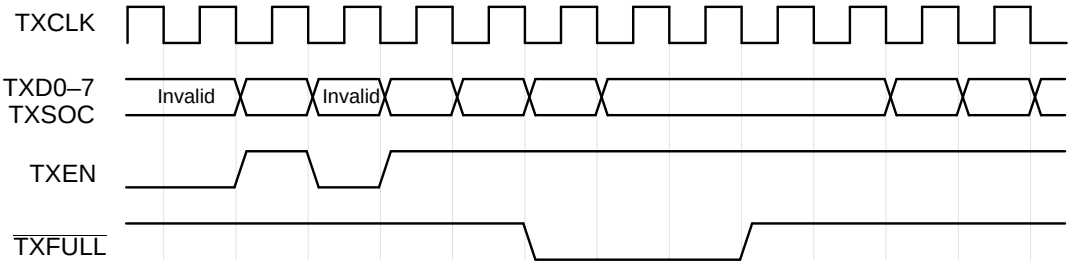


Fig. 12 – Cell Stream Transmit Interface Timing

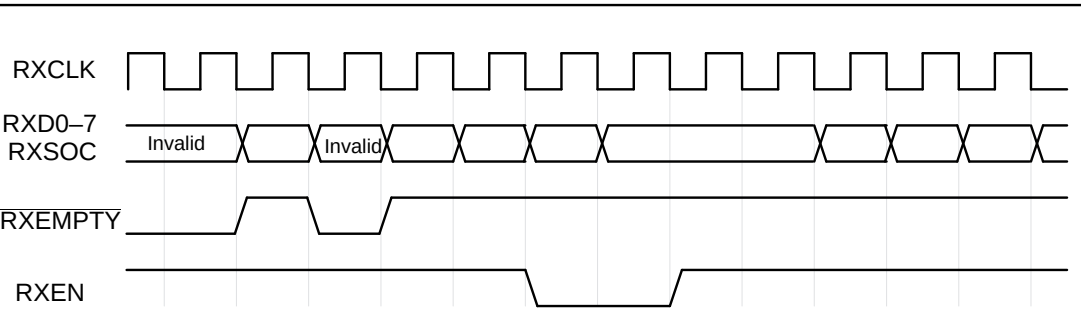


Fig. 13 – Cell Stream Receive Interface Timing

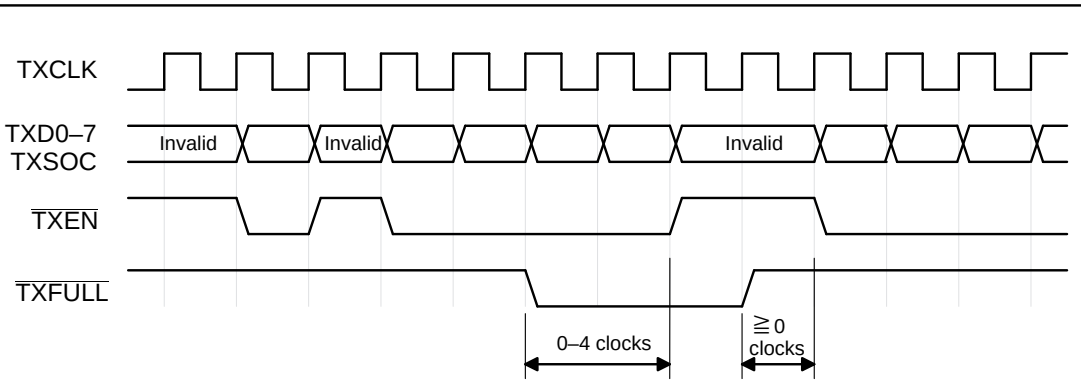


Fig. 14 – UTOPIA Transmit Interface Timing

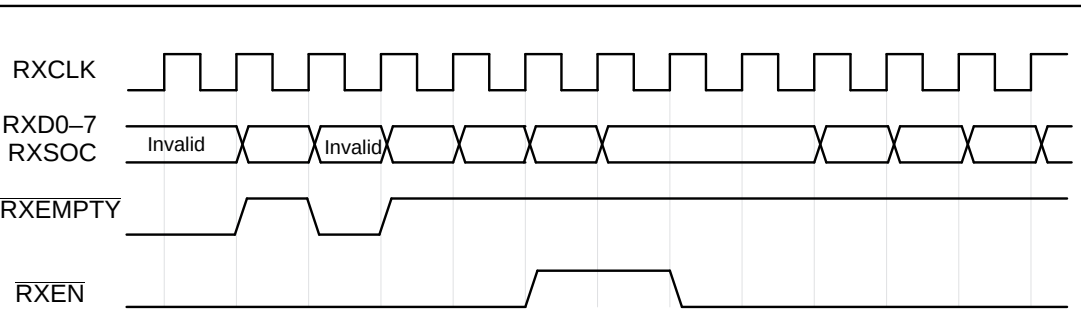


Fig. 15 – UTOPIA Receive Interface Timing

3.6.5 Address Translation

The address translation interfaces on the NTC are designed to connect directly to a Fujitsu Address Translation Controller (ATC) device. Either interface may independently enabled by setting the RXATC and TXATC bits in CR56 as required. Data across these interfaces is synchronised to the system clock .

Basic Operation

The four byte header of a cell is transferred to the ATC at the start of an address translation cycle. The ATC then searches through its table and, if no match is found for the transferred header, indicates that it can accept another cell header. The NTC records this indication as an address translation error (ATE) and then transfers another cell header to start a new cycle. Cells that cause an ATE may either be discarded or forwarded by setting the RXATE and TXATE bits in CR56 as required.

If the ATC finds a match, the new header is extracted from a table and transferred back to the NTC, along with a routing tag to be placed at the front of the cell transfer.

The ATC will continue the search until all entries in the table have been checked : if further matches are found, the corresponding new headers (plus routing tags) are transferred back to the NTC consecutively. For each new header, the NTC will repeat the payload of the cell which contained the original header.

The basic timing of these transfers is shown in Fig. 16 and Fig. 17. The data format for transfers in either direction is shown in Fig. 18 and Fig. 19.

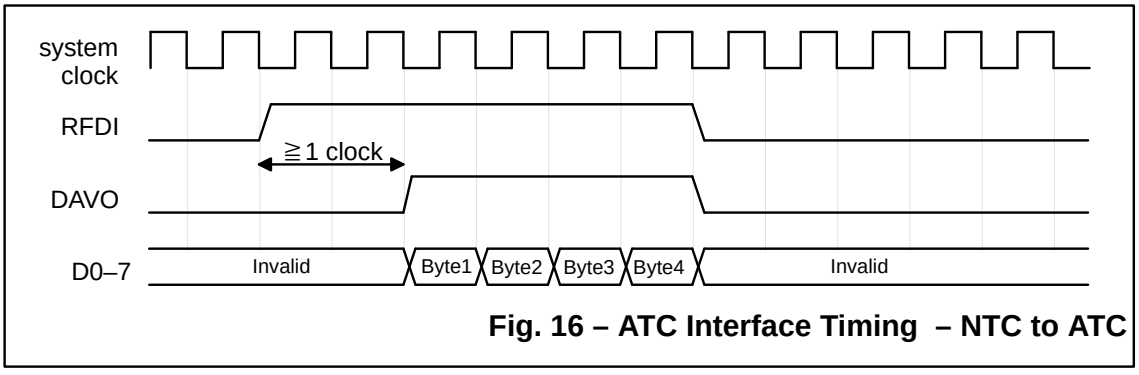


Fig. 16 – ATC Interface Timing – NTC to ATC

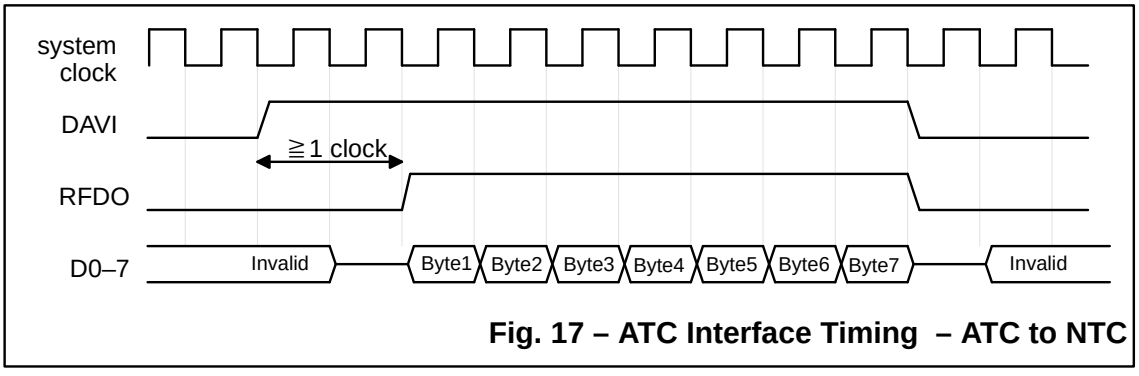


Fig. 17 – ATC Interface Timing – ATC to NTC

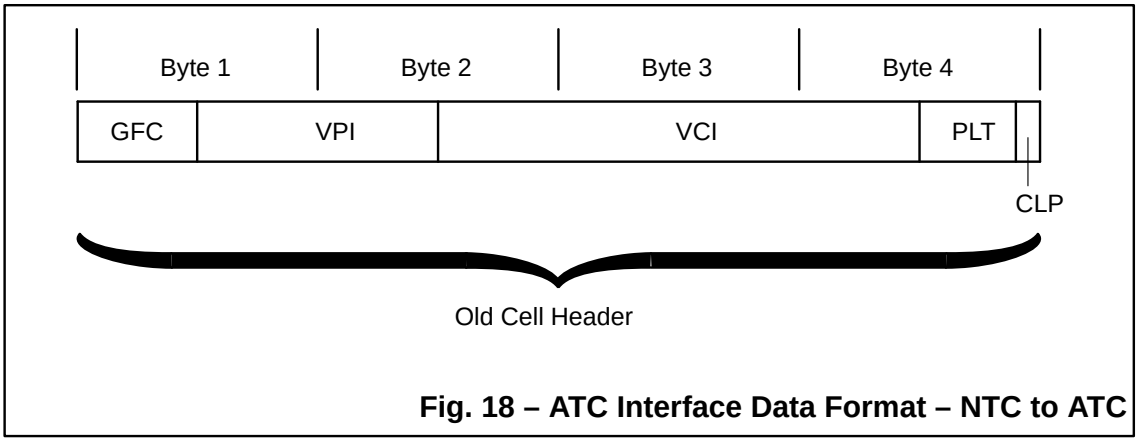


Fig. 18 – ATC Interface Data Format – NTC to ATC

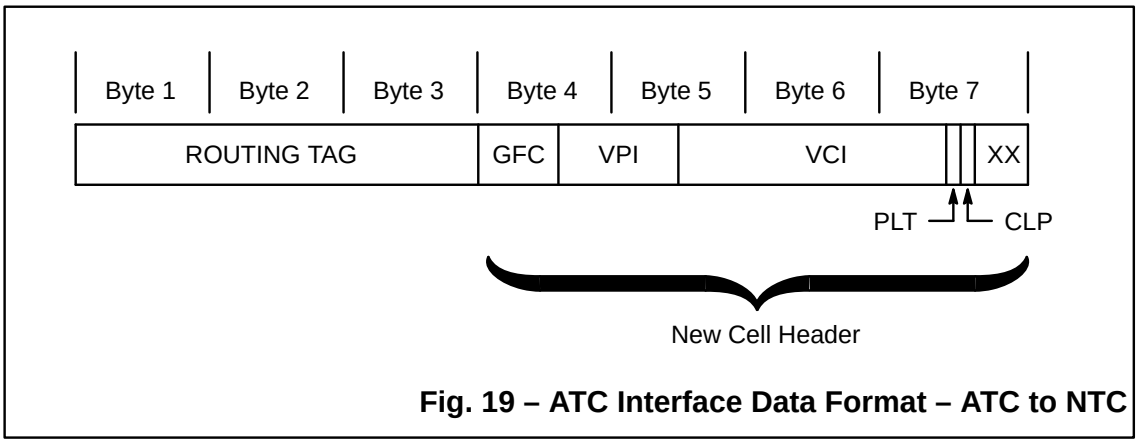


Fig. 19 – ATC Interface Data Format – ATC to NTC

3.6.6 Congestion & Cell Loss Priority

The congestion bit (bit 2 in the PLT field) and the cell loss priority (CLP) bit, both in header byte 4 in the cell, are independently controllable via the PLT and CLP bits in CR56. The bits may be set, cleared or mapped from the original or translated headers. The setting or clearing options are available even if address translation is not carried out or if an address translation error occurs.

Alteration of the CON bit in the PLT field only occurs if the first bit in the PLT field in the original header is set to 0, indicating that the header defines a user cell.

3.6.7 HEC Byte Regeneration

In the receive path, the HEC byte may be regenerated after either an address translation or alteration of the CLP or PLT fields. This is enabled by setting the RXHEC bit in CR57 and the addition modulo–2 of the ”01010101” mask pattern is controlled by the HECMASK bit also in CR57. If the HEC byte is not regenerated, and is transferred (ie the OMITHEC bit in CR57 is cleared), the value of the transmitted HEC byte will be 255.

3.7 OAM Controller

The Operation, Administration and Maintenance (OAM) controller is used to provide support for error and performance monitoring for each of the framed modes of operation.

The OAM controller interfaces between the receive and transmit framers. Various received performance/error conditions within the receive framer may be passed to the transmit framer for inclusion in outgoing frames. Additionally, some conditions are either reported to the host via status registers, or passed to the network statistics section for recording into the NSR.

The OAM controller also supports the forcing of the various alarm conditions by writing various bits in CR34. This will be independent of the receive alarm conditions.

As an example, consider STM–1 frames. Alarm signals such as AIS (Alarm Indication Signal) and FERF (Far End Receive Failure) are carried using specific SOH and POH bytes.

The BIPs are calculated in the receive framer on receive data. These BIPs are then verified with the BIPs which are extracted from the received overhead bytes. Any resulting difference is indicated using a FEBE which is passed over to the transmit framer for inclusion in outgoing frames. If this difference is non–zero, then a B1/B2/B3 status indication is given in SR59. Status register SR59 also indicates a received alarm condition, and a receive framer pointer manipulation for (SONET / SDH) framing modes.

The error monitoring is performed by using overhead bytes which carry the B1/B2/B3 BIP calculations. Error reporting is conveyed using B2 and B3 FEBE (Far End Block Error) bytes.

The FEBE values extracted from received frames are passed to the statistics controller for recording in the NSR.

Similarly for DS3 and E3 frames, the error monitoring and reporting information is carried in overhead bytes.

The OAM controller also supports the inversion of any of the transmitted BIP values (B1/B2/B3), by setting the INV bits in CR34. This may be used for external framer testing.

3.8 Network Statistics Controller

The network statistics controller maintains a record of various events in a network statistics record (NSR), which is maintained in internal RAM. The NSR will be transferred to system memory by DMA under various control conditions.

The main features of the network statistics controller are :

- Maintains statistics on up to 32 VP/VC connections simultaneously.
- Operates on receive and/or transmit paths simultaneously.
- Records total number of cell received/transmitted over the UNI.
- Optional filtering of user statistics using programmable mask.
- Selectable NSR table size.
- Controllable transfer of NSR from internal RAM to external memory.

The NSR consists of two main sections, a header section and a per VC statistics section. The NSR general format is illustrated in Fig. 20 along with the format of each per VC statistics entry and the header.

It is possible to program the size of the NSR table to either header only, header + 16 per VC entries, or header + 32 per VC entries. This will control the overall size of the DMA transfer to either 32, 160, or 288 bytes.

Statistics data is held internally in two separate NSR tables. As data is being transferred via DMA from NSR table 1, new statistics data is recorded in table 2. When this table is transferred, table 1 is then used to record any further information.

The transfer of data from one table by DMA must be completed before the second table requires to transfer data otherwise statistics data may be lost.

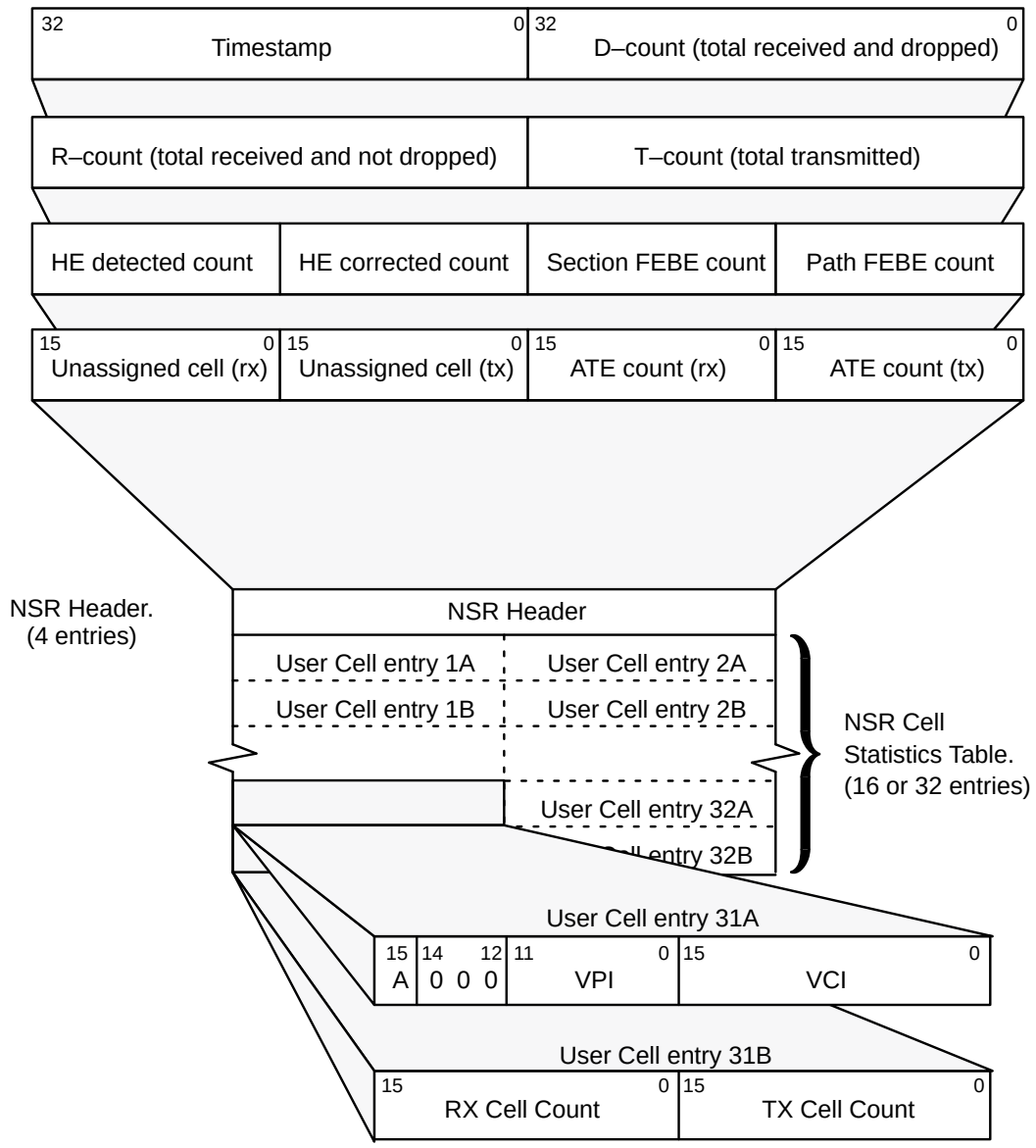


Fig. 20 – Network Statistics Record (NSR) Format

3.8.1 NSR Header

The NSR header consists of 32 bytes, grouped into the following fields :

Timestamp :
The timestamp is based on a 32 bit free running counter which is clocked directly from the system clock. When the NSR is transferred to memory, a snapshot of the counter is recorded.

D–count :
This 32 bit count records the number of cells received at the transceiver receive interface that have been discarded. The cells may have been discarded due to any of the following reasons :

- Cell with uncorrectable HEC error
- Physical layer cells
- ATM layer cell which has been discarded via the discard mask

R–count :
This 32 bit count records the total number of assigned ATM layer cells received at the transceiver receive interface that have not been discarded.

These cells will emerge from the CSI Rx port unless they are discarded due to one of the following reasons:

Being overwritten by an inserted cell;

The CSI buffer overflowing;

Being discarded due to an address translation error.

T–count :
This 32 bit count records the total number of assigned ATM layer cells transmitted at the transceiver transmit interface. This will include assigned ATM layer cells that have been inserted via the cell transmitter insert buffer.

HE Detected / Corrected :
These 16 bit counts are incremented when a header error was detected and a single bit header error was corrected.

Section/Path FEBE :
These 16 bit counts accumulate the number of non–zero Section and Path FEBE values that are extracted from the received data frames.

Unassigned Cells :
These 16 bit counts are incremented when an unassigned cell is detected within the cell stream interface. This check is done after address translation in both receive and transmit paths.

Address Translation Counts :
These 16 bit counts are incremented when an address translation error (ATE) is detected within the cell stream interface in either of the receive or transmit paths.

3.8.2 NSR Cell Statistics Table

The NSR cell statistics table holds transmitted and received cell counts for up to 32 separate VP/VC combinations. The size of the table is programmed as either 0, 16, or 32 entries, by setting the MODE bits in CR51. This will also vary the size of the DMA transfer.

It is possible to select either/both receive and transmit paths to be recorded by setting the RXSTAT and TXSTAT bits in CR51. This will not reduce the size of the table and hence overall DMA transfer, but it may reduce the frequency of the transfer.

3.8.3 Statistics Filtering

Cells being transmitted and received may be filtered before being recorded in the NSR cell statistics table. The filtering operation is enabled by setting the MASK bits in CR51.

The cell header is compared to a user-programmed mask which may have any of the 28 VPI/VCI header bits set to “0”, “1” or “X”. This allows cell headers to be matched which have either specific values or values in a range. The mask pattern bits are specified in CR54 & CR55 and the “don’t care” bits are specified in CR52 & CR53. The filtering can be either positive or negative, ie cells which match or do not match the mask.

By setting the bottom 5 VCI bits to X, and setting the remaining VCI/VPI bits to any 0 or 1 pattern, then a continuous range of 32 VCI values may be monitored.

The filter operation does not affect the recording of the R–count, D–count and the T–count in the NSR header.

3.8.4 Basic Operation

All statistics entries will initially be set to their null state. A statistics entry will be set to its active state when a cell reception event is indicated by either the cell receiver or transmitter. On receiving such an event, the statistics controller will first check all active statistics entries to find whether an entry is active for the indicated VPI/VCI. If an entry is active then it will be updated accordingly, by incrementing the receive or transmit cell count. If no statistics entry is active, then a null entry will be activated and the appropriate information recorded. If no null entries are available, then the entire NSR will be transferred to the DMA controller for subsequent transfer to system memory, all active statistics entries will be set to null and a new entry will be recorded.

3.8.5 NSR DMA Transfer

Several events will cause the NSR to be transferred and re-initialised as listed below :

- Programmable timeout based on a count from the last DMA transfer. The timeout is enabled by setting the TIMERENB bit. The TIME bits in CR51 are used to set the value of the timeout. This is explained fully in CR51 register description.
- Table overflow (TBLOVF bit in CR51). If TBLOVF is set, a DMA transfer will occur on receiving a new VPI/VCI event when no null entries are available.
  If TBLOVF is cleared, a new VPI/VCI event (when there are no null entries available) will not cause a DMA transfer. This new VPI/VCI event will not be recorded as a user entry, but the respective R or T counts will be incremented.
- Any count reaching its maximum value and attempting to overflow. Clearing the CNTOVF bit in CR51 causes the counters to wrap round on reaching their maximum value.
- Force a DMA transfer at any time by setting the FDMA bit in CR51. This bit will be self cleared as soon as the DMA operation has started.

This option when used in conjunction with the cell filter may be used to perform statistics on a selected range of VPI/VCI values over a predefined time.

After the NSR has been transferred, all counters will be set to zero.

Note that the 32-bit timestamp counter will reach its maximum value in 214 seconds when clocked at 20 MHz. The maximum time of the programmable timeout $\simeq (2^{26} - 2^{22)}$ x clock period, which equals 3.14 seconds at 20 MHz. Hence, it will be possible to derive the time relation between successive NSR records, using the timestamp values.

3.8.6 NSR DMA Format

The DMA transfer consists of either 32, 160 or 288 bytes, depending on the NSR table size. Hence, the complete transfer of the NSR will require either 16, 80 or 144 DMA cycles in 16 bit mode and 8, 40 or 72 DMA cycles in 32 bit mode.

The DMA transfer needs to be completed before the secondary NSR buffer overflows. If this is not the case, then a buffer overflow interrupt will be generated.

Data is transferred by reading the NSR from top to bottom, left to right.

To maintain data integrity, NSR data is always transferred as Big Endian.

3.9 Switch Statistics Handler

The Switch Statistics Handler (SSH) interfaces to the switch matrix, formed from SRE devices, via the serial statistics daisy chain mechanism. Its purpose is to collect any valid payload statistics from the serial data stream, remove any of the synchronisation flags and format the data into a 54 bit word ready for transfer to system memory via the NTC DMA controller. The host processor can then use this statistics data to control any congestion within the switch matrix.

3.9.1 Switch Statistics Frame Format

The received serial data stream is formatted into packets, similar to HDLC frames. Each packet is delimited by an 8–bit flag pattern (01111110) and zero stuffing is applied to all data bits between the flags to ensure that the flag pattern is not replicated. Zero stuffing involves the detection of 5 consecutive 1's and the insertion of a 0 bit after these five 1's.

Each frame may be either carrying statistics data (BUSY), or may contain empty payload data (IDLE). Idle packets are used to ensure a constant stream of data.

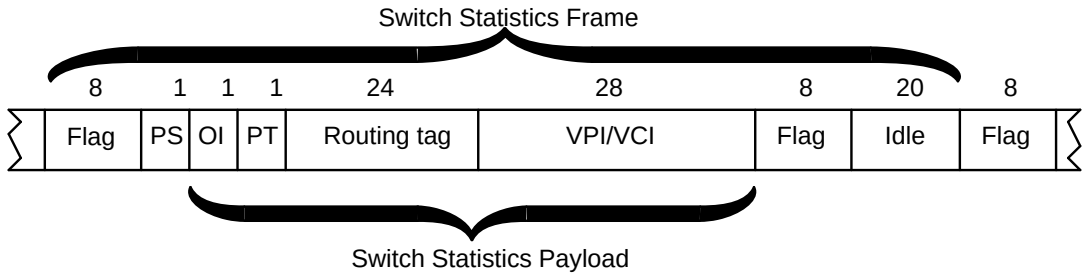
Each frame is fixed at 91 bits and consists of the following: an 8-bit synchronisation flag, a 1-bit flag to indicate an idle or busy frame, a statistics payload which can vary between 55 – 66 bits due to bit stuffing, an 8-bit closing flag and an idle period which varies between 20 – 9 bits to accommodate the bit stuffing. A diagram of the switch statistics frame without bit stuffing is shown in Fig. 21.

3.9.2 Switch Statistics Operation

The statistics handler will clock data in on the rising edge of the STATSCLK clock input. This clock may be asynchronous to the other NTC clock inputs, but its frequency must be less than the system clock.

Initially, the switch statistics handler state machine will search for the 8-bit flag pattern. On detecting this, it will then expect a 1 to indicate a BUSY payload. If it detects a 0, then the frame is IDLE and contains no switch statistics information. Once it has found a BUSY payload, the payload will be loaded into a 54-bit register. Any inserted zero bits will first be removed by counting for 5 consecutive 1's and removing the following 0.

Once a complete 54-bit switch statistics payload has been received, the controller will latch this data into a buffer capable of storing up to 2 54-bit words. The controller will then indicate to the DMA controller that a transfer is requested.



Flag	=	01111110	
PS	=	statistics payload status :	0 = IDLE 1 = BUSY
OI	=	statistics buffer overflow : indication	0 = Normal 1 = Multiple stats buffer overflow
PT	=	statistics payload type :	0 = Normal CLP discard 1 = SRE buffer overflow discard

Fig. 21 – Switch Statistics Frame Format

3.9.3 Switch Statistics DMA Format

The DMA transfer will take either 2 or 4 transfers, depending on the bus width being 32 or 16-bits. The DMA transfer should be completed before the buffer overflows. If this is not the case, then a count of lost switch statistics payloads will be recorded and sent out in the next switch statistics transfer.

All DMA transfers will be done as 64-bit blocks, and as only 54 bits are used for the switch statistics payload, the lost payload count will be recorded in the remaining 10 bits of the switch statistics data.

It is expected that switch statistics data should not be lost because the STATSCLK rate will generally be much slower than the system clock.

The data is always passed to the DMA controller in this format, ie Big Endian, so as to maintain the integrity of the data as it crosses byte boundaries.

3.10 DMA Controller

3.10.1 Basic Operation

The DMA controller allows data to be transferred between the NTC and system memory at high speed without processor intervention. The DMA controller comprises 6 separate channels (0–5) which perform the following functions:

0. Network Statistics Channel. This channel facilitates the autonomous transfer of network statistics records (NSRs) to system memory.
1. Switch Statistics Channel. This channel facilitates the autonomous transfer of switch statistics payloads to system memory.
2. Cell Receiver General Purpose Cell Extract Channel (CRX Extract). This channel facilitates the transfer of 52 byte cells received from the NTC transceiver interface to system memory.
3. Cell Receiver General Purpose Cell Insert Channel (CRX Insert). This channel facilitates the transfer of 52 byte cells from system memory to the NTC for transmission via the cell stream interface.
4. Cell Transmitter General Purpose Cell Extract Channel (CTX Extract). This channel facilitates the transfer of 52 byte cells received from the NTC cell stream interface to system memory.
5. Cell Transmitter General Purpose Cell Insert Channel (CTX Insert). This channel facilitates the transfer of 52 byte cells from system memory to the NTC for transmission via the transceiver interface.

In all cases automatic chaining is supported, which allows multiple system memory buffers to be allocated to each channel.

The nominal burst sizes for these channels are shown in Table 1.

Note that these burst word sizes correspond to the value that should be programmed into the CC field of the descriptor if using a single descriptor for the data transfer.

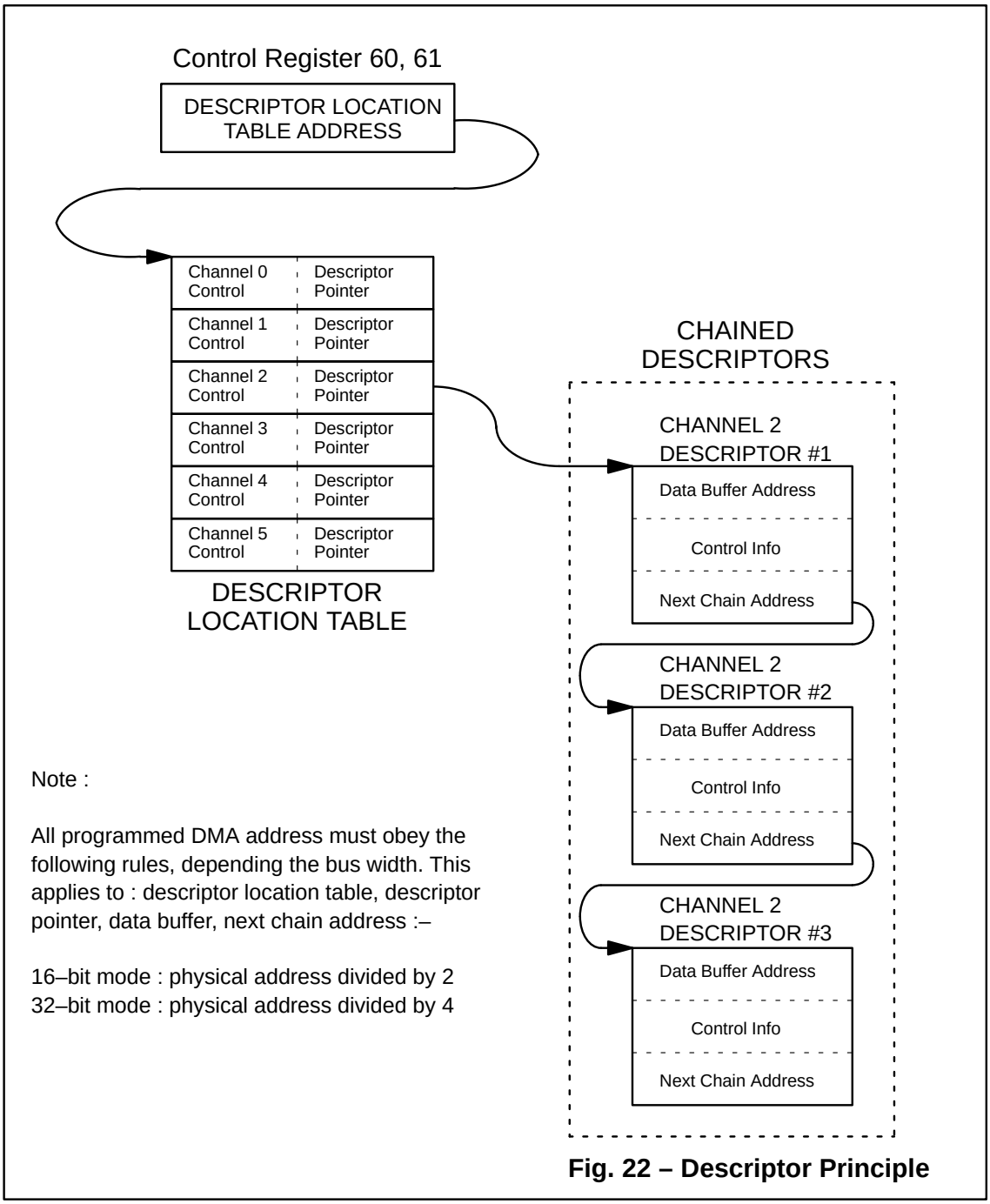
DMA Channel No.	Function	Direction	Burst Word Size (16–bits)
0	Network Statistics	From NTC to memory	16, 80, 144
1	Switch Statistics	From NTC to memory	4
2	CRX Extract	From NTC to memory	26
3	CRX Insert	From memory to NTC	26
4	CTX Extract	From NTC to memory	26
5	CTX Insert	From memory to NTC	26

Table 1 – DMA Channel Map

3.10.2 DMA Descriptors

Each DMA channel requires a descriptor which is held in system memory. The NTC maintains an address which identifies the position of a descriptor table which is also held in system memory. The descriptor location table comprises pointers to descriptors for each DMA channel.

The descriptors themselves may contain a pointer to the address of a further descriptor which may be used to form a chain of descriptors. The principle of the descriptor table, together with chained descriptors is illustrated in Fig. 22.



Note :

All programmed DMA address must obey the following rules, depending the bus width. This applies to : descriptor location table, descriptor pointer, data buffer, next chain address :–

16–bit mode : physical address divided by 2
32–bit mode : physical address divided by 4

Fig. 22 – Descriptor Principle

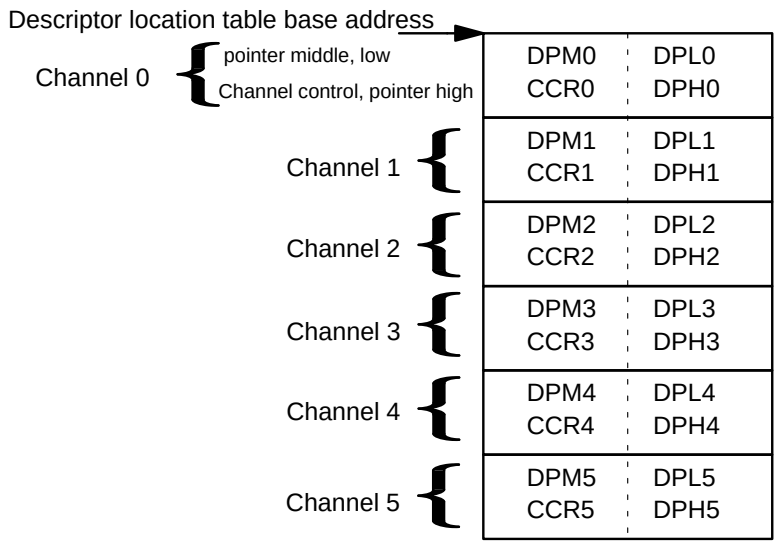
3.10.3 Descriptor Location Table

The format of the descriptor location table varies depending on whether the bus size is configured for 32 or 16 bits.

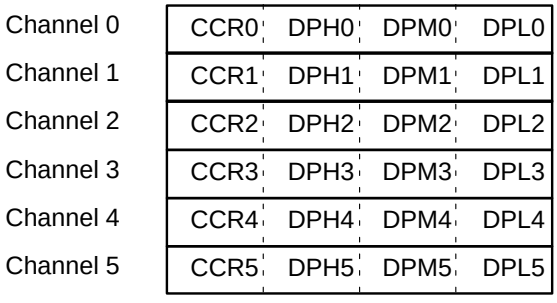
In both cases, the table contains two main information fields for each of the 6 channels.

These fields are an 8-bit Channel Control Register (CCR) and a 24-bit Descriptor Pointer (DP) address. This is illustrated in Fig. 23.

The value of the DP field must contain the physical address divided by two for 16 bit mode, or the physical address divided by four for 32 bit mode.



16-bit mode

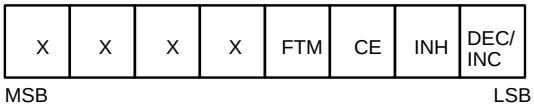


32-bit mode

Fig. 23 – Descriptor Location Table Format

3.10.4 Channel Control Register

Each channel has an associated channel control register (CCR) which is contained in the descriptor location table as illustrated in Fig. 23. This register will be loaded into the NTC when the channel is first enabled. The CCR has the following format :-



Decrement / Increment (DEC/INC)
The DEC/INC bit determines whether the address register is incremented or decremented during data transfer. When this bit is 1 the address register will be incremented, and when this bit is 0 the address register will be decremented.

Inhibit (INH)
The INH bit inhibits the address register from being incremented or decremented. When this bit is 1 data transfer will be performed repetitively at the initial block address only. When this bit is 0 the block address will be incremented or decremented as specified by the DEC/INC bit.

Chaining Enable (CE)
The CE bit controls chaining operation. When this bit is 1 chaining is dependent on the CHE bit in the descriptor BCF field. When this bit is 0 chaining is disabled.

Fast Transfer Mode (FTM)
The FTM bit is used to determine whether the $\overline{\text{READY}}/\overline{\text{DTACK}}$ input affects the DMA transfer cycle.

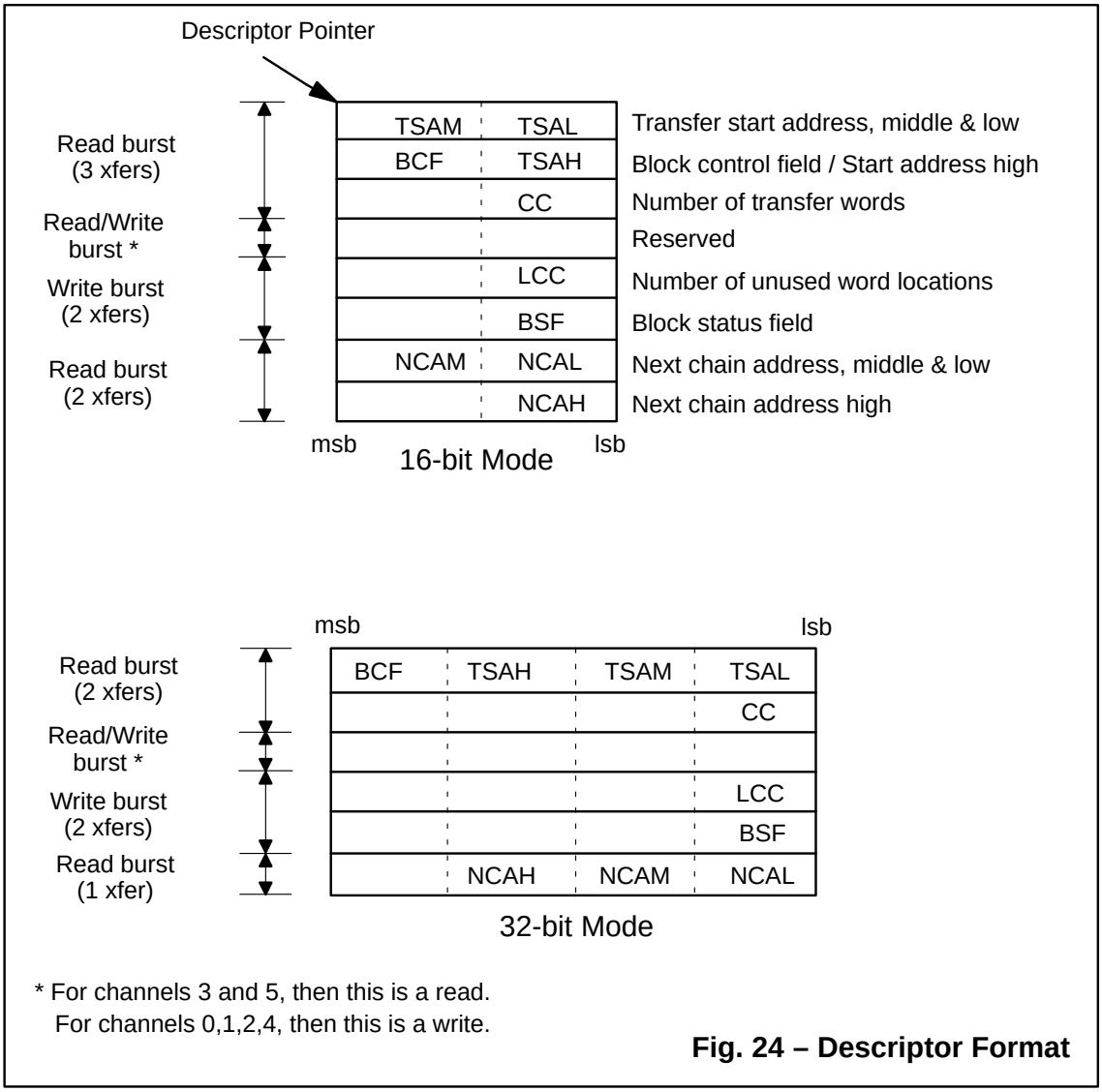
If this bit is set to 1, the $\overline{\text{READY}}/\overline{\text{DTACK}}$ input has no effect and the DMA transfer cycle is fixed at 4 system clock periods.

If this bit is set to 0, the $\overline{\text{READY}}/\overline{\text{DTACK}}$ input will be sampled in every DMA transfer cycle and the cycle may be extended by any number of system clocks ($\geqq 0$) to allow for slower memory systems.

3.10.5 Descriptor Format

For each DMA channel, the descriptor indicates the number of 16-bit words to be transferred, start address, and control information as shown in Fig. 24. When a channel is first enabled, the DMA controller will locate and load the associated descriptor address and control field using a burst mode transfer.

When the DMA controller completes a data block transfer, it will write status information into the current descriptor and will then read the start address of the next descriptor in the chain, if chaining is enabled. An interrupt will be generated on completion of a block transfer, if the DMA interrupt is set in CR58 and if the DIE bit is set in the BCF.



* For channels 3 and 5, then this is a read.
For channels 0,1,2,4, then this is a write.

Fig. 24 – Descriptor Format

3.10.6 Descriptor Control Fields

The meaning of each descriptor control field is given below. Any unused fields in the descriptor are ignored:

Transfer Start Address Field (TSAL, TSAM, TSAH)
This field specifies the start address of a block. Data will be transferred with the address incrementing or decrementing or static, depending on the DEC/INC and INH bits of the CCR.

The value of the Start Address Field should contain the physical address divided by two for 16 bit mode, or the physical address divided by four for 32 bit mode.

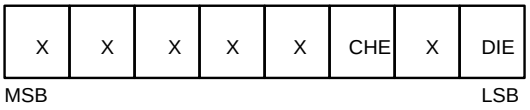
Character Count Field (CC)
This field specifies the block size in 16-bit words. When the number of words specified by the character count field have been transferred, the current block transfer will be terminated.

Last Character Count Field (LCC)
This field will be used to indicate the number of remaining words in a block when a block transfer is terminated.

Next Chain Address Field (NCAL, NCAM, NCAH)
This field indicates the start address of the next DMA descriptor in a chain. This field will be read into the DMA controller at the end of a block transfer when chaining is enabled.

The value of the Next Chain Address Field should contain the physical address divided by two for 16 bit mode, or the physical address divided by four for 32 bit mode.

Block Control Field (BCF)
The block control field has the following format:-



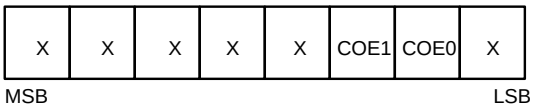
- DMA Interrupt Enable (DIE)

This bit should be set to 1 to cause an interrupt to be generated after the associated block transfer has been completed.

- Chaining Enable (CHE)

This bit should be set to 1 to enable chaining at the end of a block transfer.

Block Status Field (BSF)
This field will be written by the DMA controller at the end of a block transfer operation. It has the following format :-



- COE0

This bit will be set when a block transfer operation has been terminated by the character count register reaching zero. Hence, a successful transfer has occurred.

- COE1

This bit will be set when a block transfer operation has been terminated by the DMA channel enable bit being reset during operation.

3.10.7 Data Transfer Operations

A data transfer operation will be initiated when an internal function requires to transfer some data. The DMA controller will then request use of the system bus by activating the bus request output signal. The DMA controller will then wait for the external processor to grant it use of the bus, and it will then initiate a transfer cycle.

After it has been granted use of the system bus, the DMA controller will transfer the required data in a single burst. Hence ATM cells will be transferred in 52 byte bursts (ie 13 r/w cycles of 32 bits, or 26 r/w cycles of 16 bits) for the cell insert/extract DMA channels. Similarly, the network statistics records will be transferred in either 32, 160, or 288 byte bursts (ie. 8/40/72 write cycles of 32 bits, or 16/80/144 write cycles of 16 bits). The switch statistics data will be transferred in 8 byte bursts (ie 2 write cycles of 32 bits or 4 write cycles of 16 bits).

It is possible to reduce the time that the DMA holds the bus by chaining descriptors.

For example, if the Network Statistics Record (NSR – channel 0) requires 288 bytes to be transferred. This could be done either as one block transfer of 144 16-bit words, or by breaking the transfer into 4 separate blocks by chaining 4 descriptors. The DMA will request the bus at the end of each block transfer, and hence the processor will have access at these points to accept or deny the request.

It is also possible to suspend/abort the DMA transfer. This is described in the next section.

3.10.8 DMA Suspend / Abort

There are various mechanisms to control the operation of the DMA controller. These include control over–ride, DMA stop, bus clear ($\overline{BCLR}$), and bus error ($\overline{BERR}$).

Control Over–ride
This mechanism is supported in INTEL type systems by de–asserting the HLDA pin. This is described in detail later.

DMA Stop :
This is performed by firstly gaining control of the bus, and then by setting the DMA stop bit in CR63. This will suspend the DMA controller and prevent it from requesting the bus until this bit has been cleared. When the DMA stop bit has been cleared, the DMA operation will resume, after having regained the bus.

Bus Clear ($\overline{BCLR}$) :
This signal may be asserted by the control processor to gain control of the system bus by suspending any NTC DMA transfer. It is treated as an asynchronous input and is level detected. It should remain asserted until the NTC releases the bus.

The NTC will release the bus and any DMA transfer will be internally suspended. The NTC will then re–request the bus, and once the bus has been granted, the DMA transfer will resume.

Bus Error ($\overline{BERR}$) :
This signal may be asserted by the control processor to abort any DMA transfer. It is treated as an asynchronous input and is level detected. This signal would normally be asserted if the NTC holds the bus for greater than a set time. This may occur if the DMA descriptors have been incorrectly programmed and the NTC is trying to access invalid memory during a read operation, and hence a $\overline{READY}$/$\overline{DTACK}$ signal will never be generated.

On detecting this active signal, the NTC will release the bus and any DMA transfer will be internally aborted.

An interrupt may also be generated by enabling the $\overline{BERR}$ interrupt in CR58.
On receiving this interrupt, the processor may then read SR63 which will indicate which DMA channel was active when the DMA transfer was aborted.

3.11 Microprocessor Interface

The microprocessor interface has two basic functions. One is to act as an asynchronous slave for microprocessor access to NTC internal registers, and the other is as an asynchronous master for the DMA transfer of data between the NTC and system memory. The microprocessor interface may be configured to be compatible with 16–bit or 32–bit Motorola or Intel systems.

3.11.1 Processor Register Access

The device is in slave mode when the NTC does not have control of the system bus. All internal registers are 16-bits wide. A table showing the control and status registers is shown in Appendix A. Complete descriptions of all the register bits are given in Appendix B.

16-Bit Mode
In 16-bit mode, only word transfers are allowed. Byte access is not provided. Read and write operations are made via the $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, A0 and $\overline{CS}$ signals when in INTEL mode and $\overline{AS}$, R/$\overline{W}$, $\overline{LDS}$, $\overline{UDS}$ and $\overline{CS}$ in MOTOROLA mode. In both modes the cycles are terminated by the NTC via the RDYOUT output pin.

In 16-bit mode register access, there is no difference in byte ordering between Little Endian and Big Endian systems, since the transfers are seen as single 16-bit words and not two 8-bit bytes.

32-Bit Mode
In 32-bit mode transfers can be either words (but only on word boundaries) or long words (but only on long word boundaries), but not bytes. In INTEL mode, read and write transfers are controlled via the $\overline{RD}$, $\overline{WR}$, $\overline{BE0–3}$ and $\overline{CS}$ signals, and in MOTOROLA mode by the $\overline{AS}$, R/$\overline{W}$, $\overline{DS}$ A0–1, SIZ0–1 and $\overline{CS}$ signals. In common with 16-bit mode, the NTC terminates these cycles via the RDYOUT signal.

Since the bus size is 32-bits wide and the registers are only 16-bits wide, the difference between Big Endian and Little Endian needs to be considered. When in INTEL mode and the BSWAP pin (bus swap) is inactive, the configuration will be Little Endian and registers will be numbered right to left.

When in INTEL mode with BSWAP active, or in Motorola mode, the configuration is Big Endian with registers numbered left to right. This is illustrated in Fig. 25 and Fig. 26.

Cycle Termination – RDYOUT
Due to internal synchronisation, there is a minimum time in NTC system clock cycles between consecutive read or write operations. This time is 5 and 7 clock cycles for 16 and 32 bit modes respectively. For single write accesses, however, RDYOUT will respond immediately.

In order to allow software to be written independently of this, the RDYOUT signal is provided which is used by the host to insert wait cycles.

The RDYOUT signal is asynchronous and when high indicates to the host that the present cycle can be terminated, as long as the minimum cycle time has been satisfied.

When the NTC is not being accessed the RDYOUT signal is always inactive.

This is further explained in section 4.

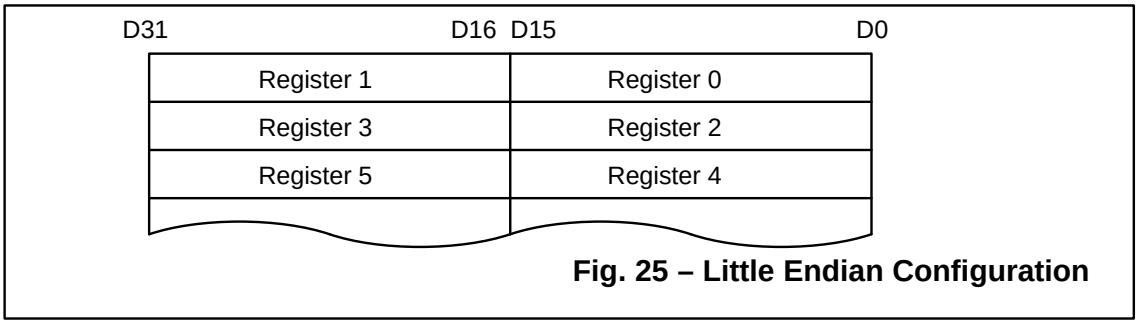


Fig. 25 – Little Endian Configuration

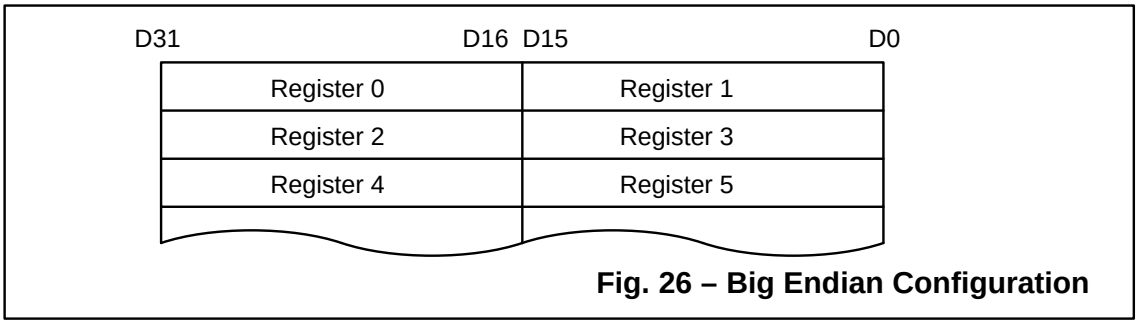


Fig. 26 – Big Endian Configuration

3.11.2 Databus Pin Status

Data is driven onto the databus either as 16 or 32 bit words depending on the configuration. The configuration is controlled by 8 of the microprocessor pins. This is illustrated in Table 2.

A “0” or “1” on the control pins indicate a low or high level respectively, whereas an X indicates that this bit is not used. A ’D’ on the databus indicates valid data, whereas a ’–’ indicates invalid data.

Bus Mode	Control Pins								Databus Pins
	BM	BW	BSWAP	SIZ1 $\overline{BE3}$	SIZ0 $\overline{BE2}$	A1 $\overline{BE1}$	A0 $\overline{LDS}$ $\overline{BE0}$	$\overline{BHE}$ $\overline{UDS}$ $\overline{DS}$	D31–D0
INTEL 32 bit	0	1	0 = LE 1 = BE	1 0 0	1 0 0	0 1 0	0 1 0	X	—DD DD— DDDD
MOTOROLA 32 bit	1	1	X	1 1 0	0 0 0	1 0 0	0 0 0	$\overline{DS}$	—DD DD— DDDD
INTEL 16 bit	0	0	0 = LE 1 = BE**	H	H	A1	0	0	HHDD
MOTOROLA 16 bit	1	0	X	H	H	A1	0	0	HHDD

**Note: BSWAP (Intel 16 bit) only applies to DMA data transfers. Otherwise X.

Table 2 – Databus Pin Status

3.11.3 DMA Arbitration and Chaining

DMA arbitration for control of the system bus is asynchronous, and is fully compliant with both INTEL and MOTOROLA bus cycles. Multiple NTCs can be chained together without the need of an external bus arbiter using proprietary signals. This is described below for both INTEL and MOTOROLA modes.

INTEL Mode Arbitration

When in INTEL mode, DMA arbitration is accomplished using the HOLD and HLDA signals. The HOLD signal is tri–state when inactive to allow it to be connected in a wired OR configuration with other signals and therefore needs a pull down resistor of 2K7Ω.

A DMA transfer can be suspended by negating the HLDA signal and forcing a control override. The NTC will request the bus after two clock cycles and once it has regained control, it will continue from where it was suspended.

INTEL Mode Chaining

A number of NTCs can be chained together without the need of an external arbiter by using the DCOUT signal. This is illustrated in Fig. 27. To the host it appears as if there is only one device. During a DMA cycle with chained NTCs, the control of the bus is simply passed down the chain with NTCs individually controlling the bus if required.

At the end of the chain, the bus will be released if a device has passed the token on. Further DMA transfers must wait until the present chaining cycle has finished and the bus released before requesting the bus. This is to prevent chained NTCs from dominating the bus.

If control override cycles are required when using chains of NTCs the CONT signals must be connected together in a wired OR configuration and pulled low with a 2K7Ω resistor. This signal is used by the present bus master to inform other devices further down the chain that a control override has occurred and they must cease requesting the bus.

For timing diagrams associated with this topic, please refer to section 4.5 on page 74.

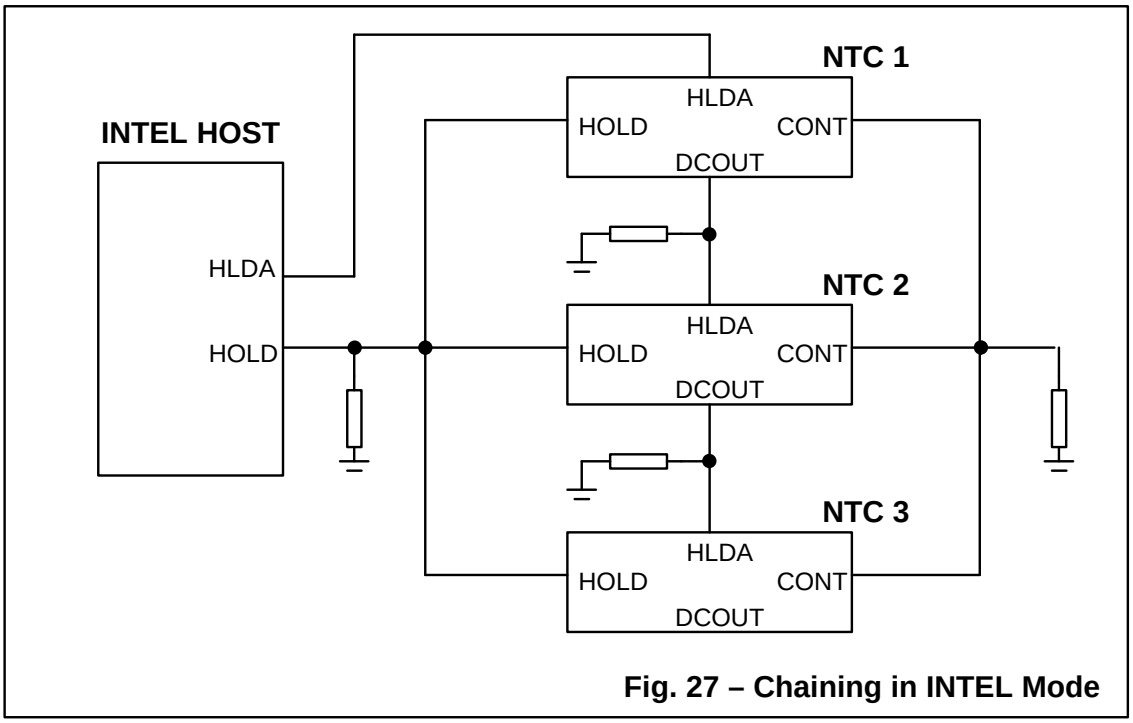


Fig. 27 – Chaining in INTEL Mode

MOTOROLA Mode Arbitration

When in MOTOROLA mode, DMA arbitration is accomplished using the $\overline{BR}$, $\overline{BG}$ and $\overline{BGACK}$ signals. $\overline{AS}$ and $\overline{DTACK}$ are also monitored to indicate the end of a cycle. Both $\overline{BR}$ and $\overline{BGACK}$ are tri–state when inactive and thus need to be pulled high via a 2K7Ω resistor. The NTC will not assume control of the bus after receiving a $\overline{BG}$ active signal unless $\overline{BGACK}$, $\overline{AS}$ and $\overline{DTACK}$ are all inactive.

For timing diagrams associated with this topic, please refer to section 4.5 on page 74.

MOTOROLA Mode Chaining

When NTCs are chained in MOTOROLA mode the $\overline{BR}$ signal is held active throughout the cycle until the last NTC in the chain is being serviced and then the $\overline{BR}$ signal will become inactive after detecting $\overline{BG}$ active.

This indicates to the host that multiple bus requests are occurring and although the $\overline{BGACK}$ signal will be released between each NTC controlling the bus the host will not interrupt the DMA cycle. In this case, the $\overline{BGOUT}$ signal should be pulled up with a 2K7Ω resistor. This is illustrated in Fig. 28.

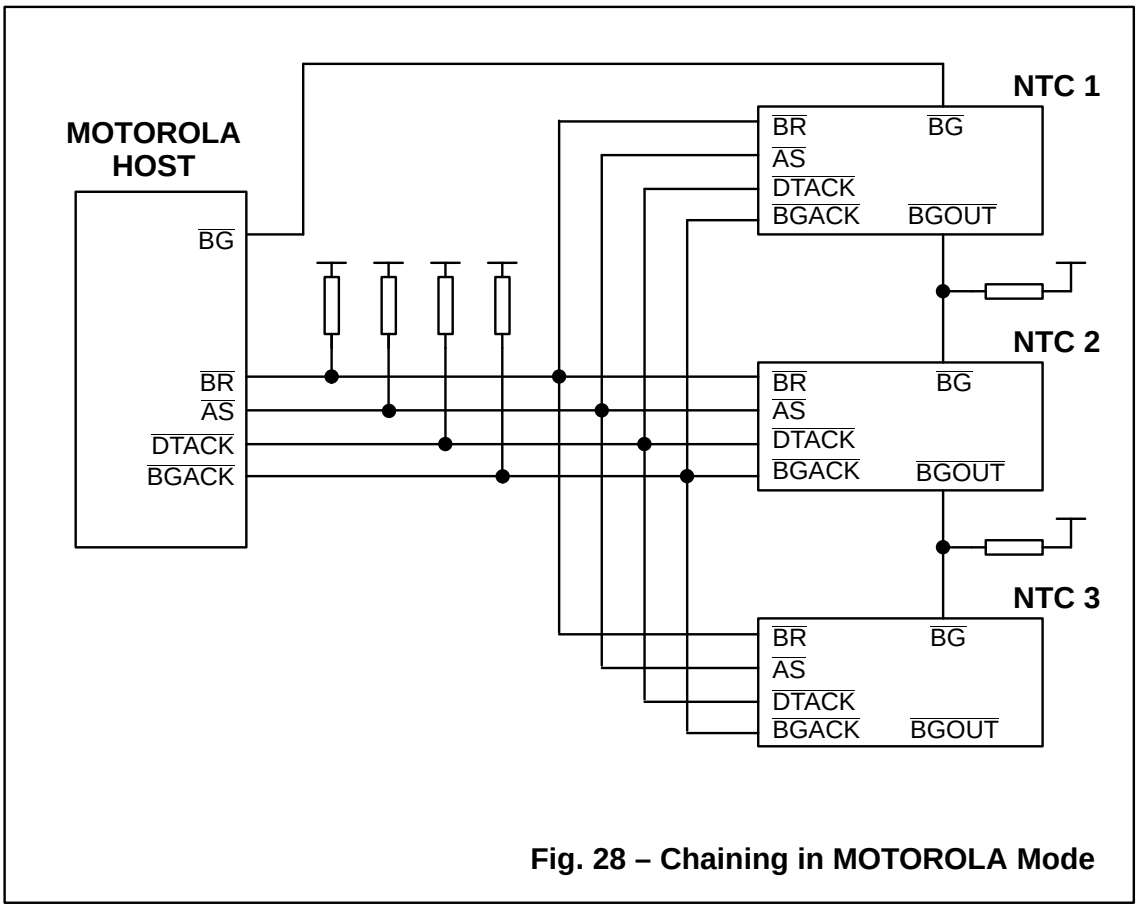


Fig. 28 – Chaining in MOTOROLA Mode

3.11.4 DMA Transfer Cycles

When transferring data between the NTC and system memory, the full data bus width is always used, so in 16-bit mode only words are transferred and in 32-bit mode only long words are transferred. Single byte transfers are not possible.

Wait states can be inserted by the use of the asynchronous $\overline{\text{READY}}$/$\overline{\text{DTACK}}$ signal, if enabled. This is done in two stages. Fast transfer of DMA descriptor read/writes is done by setting the FTM bit in the DMA mode register. Fast transfer of the DMA data is done on a per channel basis by setting the FTM bit in the respective Channel Control Register (CCR) within the descriptor location table.

INTEL 16-bit mode transfers are controlled by the $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and A0 signals. 32-bit mode transfers are controlled by the $\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{BE0–3}}$ signals. Wait states can be inserted by using the $\overline{\text{READY}}$ input.

MOTOROLA 16-bit mode transfers are controlled by the $\overline{\text{AS}}$, R/$\overline{\text{W}}$, $\overline{\text{LDS}}$ and $\overline{\text{UDS}}$ signals. In 32-bit mode transfers are controlled by the $\overline{\text{AS}}$, R/$\overline{\text{W}}$, $\overline{\text{DS}}$, A0–1 and SIZ0–1 signals. Wait states can be inserted by using the $\overline{\text{DTACK}}$ input.

Little Endian / Big Endian

Since the data transferred is individual bytes in both 16-bit and 32-bit modes, the byte configuration is dependant on the system bus being configured as Big Endian or Little Endian.

The NTC DMA data conforms to Little Endian when in INTEL mode and BSWAP pin is low level.

Normally, the NTC DMA data conforms to Big Endian when in INTEL mode and BSWAP pin is high, or when in MOTOROLA mode. This is illustrated in Fig. 29 and Fig. 30.

However, an exception to this is when transferring the network and switch statistics data (channels 0 and 1). This data is always configured as Big Endian, irrespective of the system configuration, so as to maintain data integrity across byte boundaries.

Also, DMA descriptor data is independent of the system configuration, and is always transferred as Little Endian.

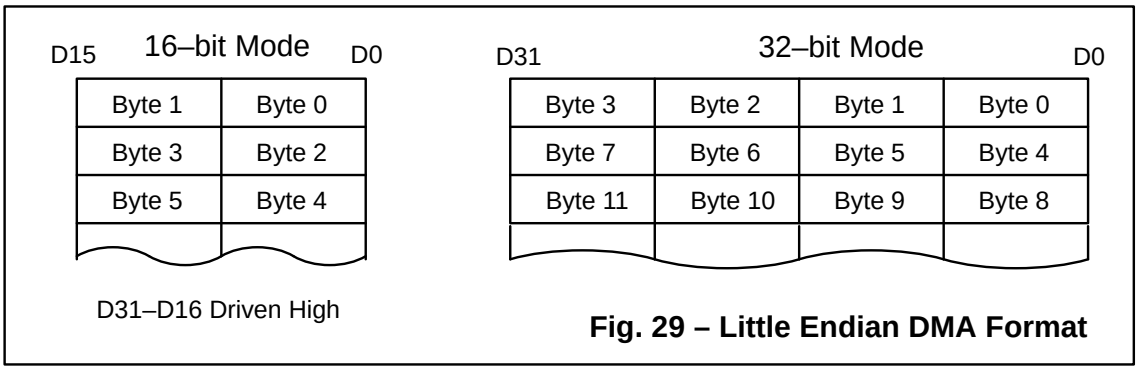


Fig. 29 – Little Endian DMA Format

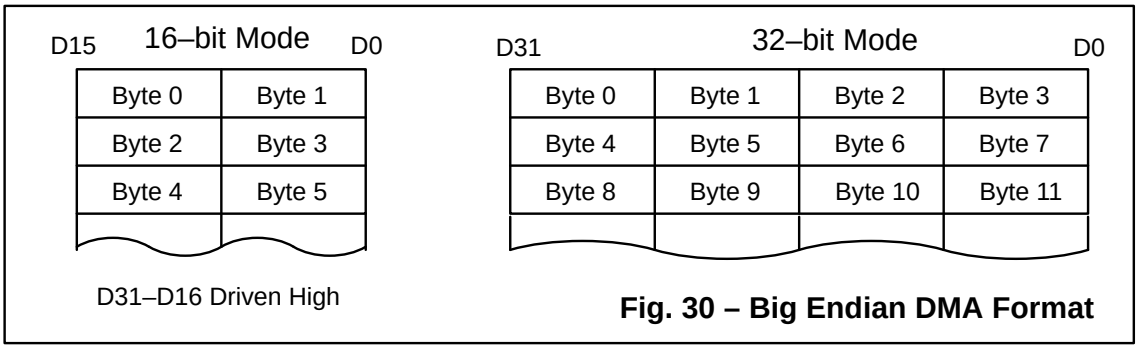


Fig. 30 – Big Endian DMA Format

3.11.5 Interrupt Handling

The NTC can generate an interrupt to the processor using the $\overline{IRQ}$ output pin. There are 10 sources of interrupts from within the NTC, all of which are maskable if not required.

Interrupts will be set in the Interrupt Status Register (SR58) irrespective of being enabled in the Interrupt Enable Register (CR58). The purpose of setting bits in the Interrupt Enable Register (CR58) is to allow an interrupt source to activate the $\overline{IRQ}$ output pin.

The procedure for handling the interrupts is as follows :-

Enable Interrupts by setting bits in CR58.

Wait for $\overline{IRQ}$ output going active.

Read the Interrupt Status Register (SR58).

Write the value from SR58 back into the Interrupt Under Service Register (CR59).
This will clear the interrupt request, and will prevent further interrupts of the same type from being generated.

Process the interrupt.

Enable further interrupts by clearing the bits previously set in the Under Service Register (CR59).

Three of the interrupts provide further information as to the source of the interrupt. These are the BUFFOVF, $\overline{BERR}$ and DMA interrupts. This information may be obtained by reading the interrupt indication registers (SR61, and SR63 respectively). Reading these registers will clear the indication only, not the associated interrupt bit in SR58.

3.11.6 RESET Sequence

If an external reset is applied to the NTC, all of the internal control registers are initialised to zero (ie. 0000h).

Each of the NTC blocks (Framer, Cell Receiver, Cell Transmitter, Cell Stream Interface, OAM Controller, Network Statistics Controller, Switch Statistics Handler and DMA controller) are held in reset until their corresponding Enable (ENB) bits are written to.

Block	Control Register	Enable bit(s)
Framer	CR1	FRMENB
Cell Receiver	CR18	CRXENB
Cell Transmitter	CR26	CTXENB
OAM Controller	CR34	OAMENB
Switch Statistics Controller	CR50	SSHENB
Network Statistics Controller	CR51	MODE 0, MODE 1
Cell Stream Interface	CR56	CSENB
DMA Controller	CR63	DMAENB

Table 3 – Control Register Reset

It is recommended that the various blocks are configured using their control registers before setting the ENB bit in the general control register. Please refer to the register set–up note.

If these enable bits are cleared, the corresponding register will be reset.

In the case of the DMA Controller, if the DMAENB bit is cleared (DMA is reset), all the other DMA control registers (CR60, CR61 & CR62) must re–written to before the block is re–enabled.

This is because CR60, CR61 and CR62 are used for internal purposes as well as being microprocessor control registers.

3.12 JTAG

3.12.1 Introduction

The MB86683A contains Boundary Scan Test Circuitry compliant with IEEE 1149.1 (JTAG). This is accessed using the 4 pins identified below. The JTAG circuitry is internally reset at power on, and hence the optional JTAG reset pin (TRST) is not required.

The JTAG circuitry allows easier board level testing by allowing the signal pins on the device to form a serial scan chain around the device. Test modes are controlled by accessing an internal Test Access Port Controller (TAPC), which is in turn controlled from the TAP.

3.12.2 Test Access Port (TAP)

Four pins are dedicated to JTAG. These are: TDO, TDI, TMS and TCK.

The functions of these signals are described in Section 2.2.7 of this datasheet.

3.12.3 JTAG Boundary Scan

Details of the boundary scan and the cells allocated to JTAG may be found in Appendix E.

3.12.4 Test Instructions

The following JTAG instructions are implemented:

- BYPASS
- SAMPLE/PRELOAD
- EXTEST

BYPASS

The BYPASS instruction is used to bypass a component that is connected in series with other components. This allows more rapid movement of test data through the components of the board, bypassing the ones that do not need to be tested.

The BYPASS operation enables the bypass register, which is a single stage shift register, between TDI and TDO.

The binary code for the BYPASS instruction is 11.

The BYPASS instruction is forced into the instruction register output latches during the Test_Logic_Reset state. Note the distinction between the 01 content of the instruction shift register and the 11 of the instruction register output latch. Therefore, at the start of the instruction-shift cycle, a 01 pattern will be seen instead of 11.

The BYPASS operation does not interfere with the component operation at all.

SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction is used to sample the state of the component pins. The sampled values can be examined by shifting out the data through TDO. The preloaded values are then enabled to the output pins by the EXTEST.

The binary code for the instruction is 01.

The SAMPLE/PRELOAD instruction selects the boundary scan cells to be connected between TDI and TDO in the Shift_DR TAP controller state.

The values of the component pins are sampled on the rising edge of TCK in the Capture_DR TAP controller state.

The preload values shifted in the boundary scan cells are latched into the boundary scan output latch at the falling edge of TCK in the Update_DR TAP controller state.

EXTEST

EXTEST instruction allows testing of off-chip circuitry and board level interconnections.

The PRELOAD/SAMPLE instruction is used to preload the data into the latched parallel outputs of the boundary scan shift register stages. Then, the EXTEST instruction enables the preloaded values to the components output pins.

The binary code for the instruction is 00.

The device outputs the preloaded data to the pins at the falling edge of TCK in the Update_IR TAP controller state at which point the JTAG instruction register is updated with the EXTEST.

The EXTEST instruction selects the boundary scan cells to be connected between TDI and TDO in the Shift_DR test logic controller state.

Once the EXTEST instruction is effective, the output pins can change at the falling edge of TCK in the Update_DR TAP controller state.

4. DEVELOPERS NOTES

4.1 Loopback Modes

The NTC includes two loopback modes for in-line testing purposes. These modes are referred to as transceiver loopback and CSI loopback. The modes are set by setting the appropriate LOOPBACK bits in CR1 and CR56 respectively.

The dataflow is controlled as shown in Fig. 31 for transceiver loopback and in Fig. 32 for CSI loopback.

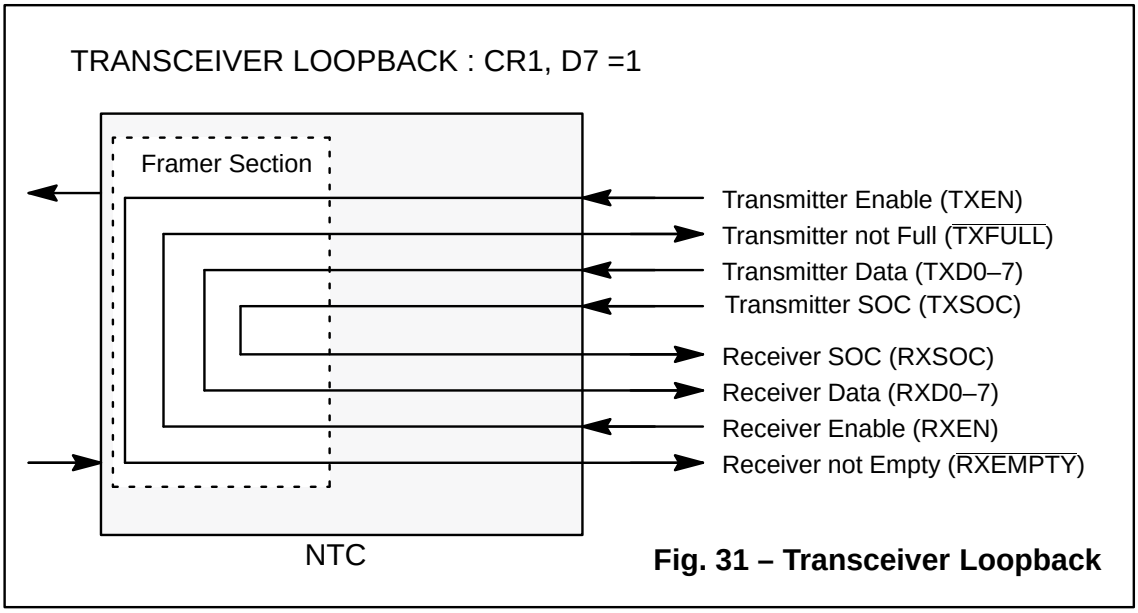


Fig. 31 – Transceiver Loopback

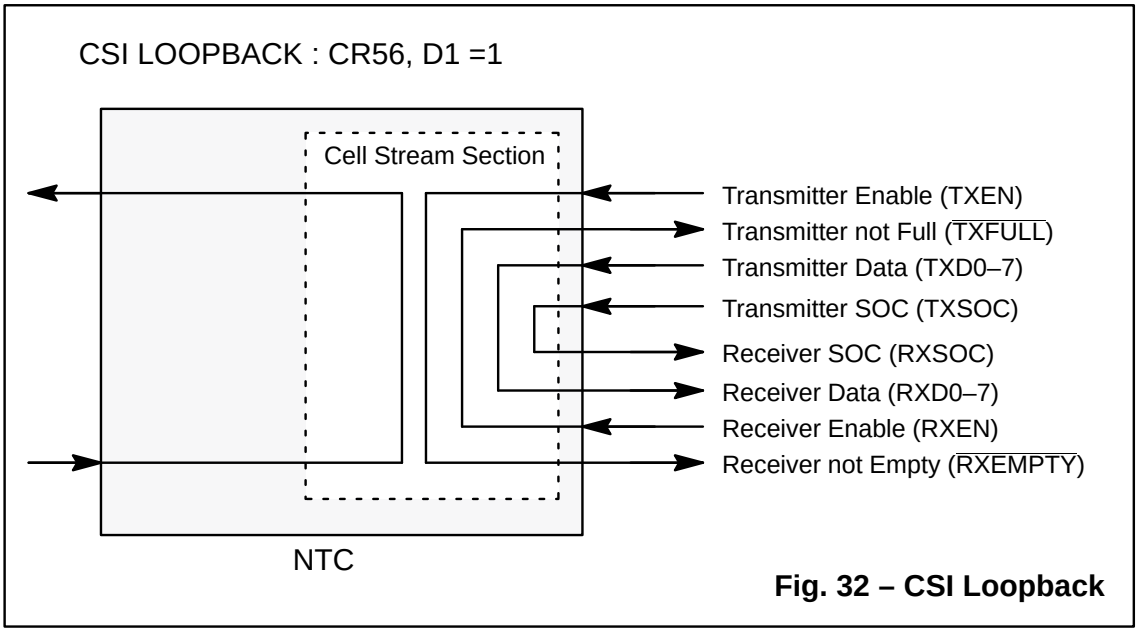


Fig. 32 – CSI Loopback

4.2 Microprocessor Connections

The NTC is capable of interfacing to a variety of processors, including 16/32 bit INTEL or 16/32 bit MOTOROLA devices. Four typical configurations are illustrated in Fig. 33 – Fig. 36.

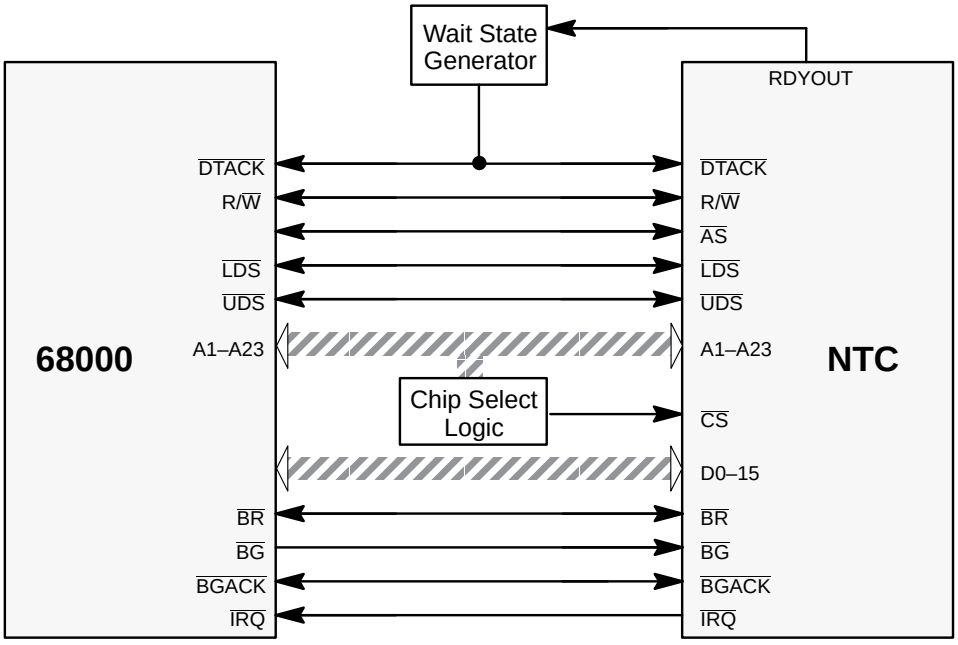


Fig. 33 – 16-bit MOTOROLA Connection

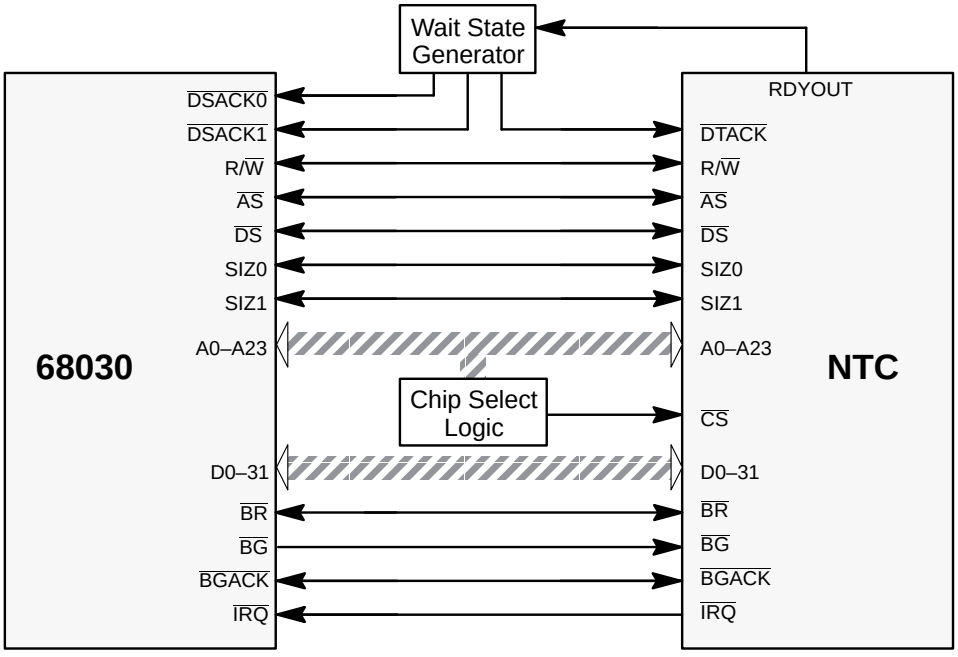


Fig. 34 – 32-bit MOTOROLA Connection

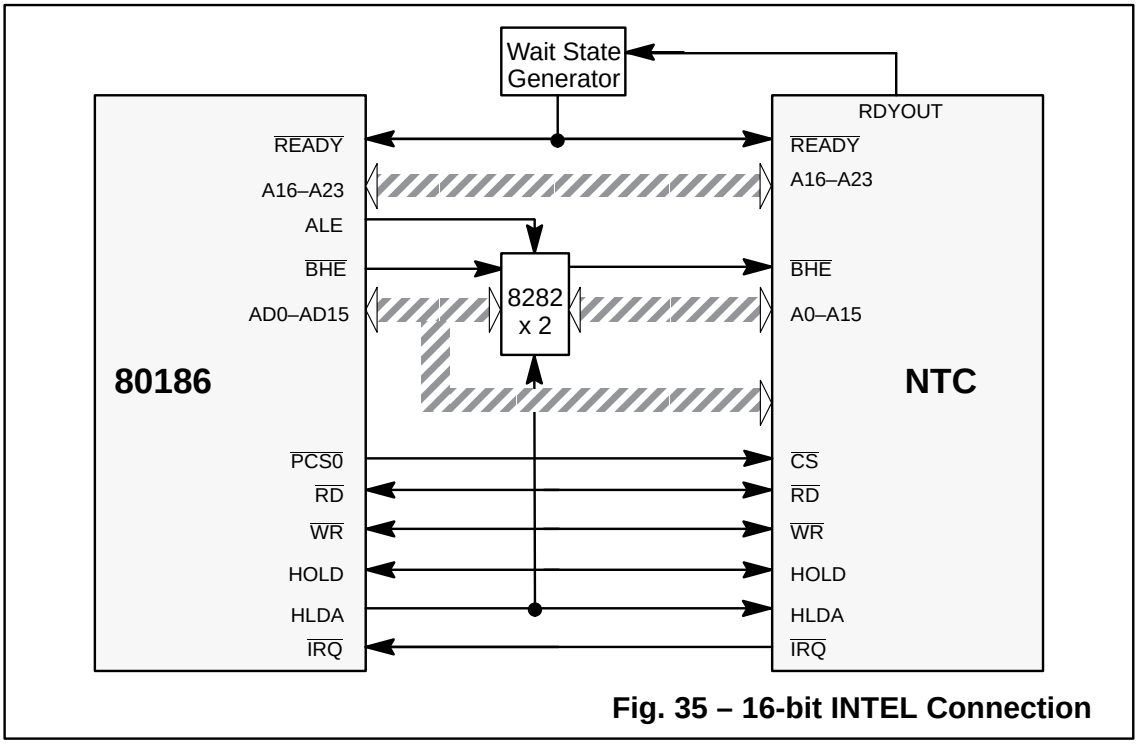


Fig. 35 – 16-bit INTEL Connection

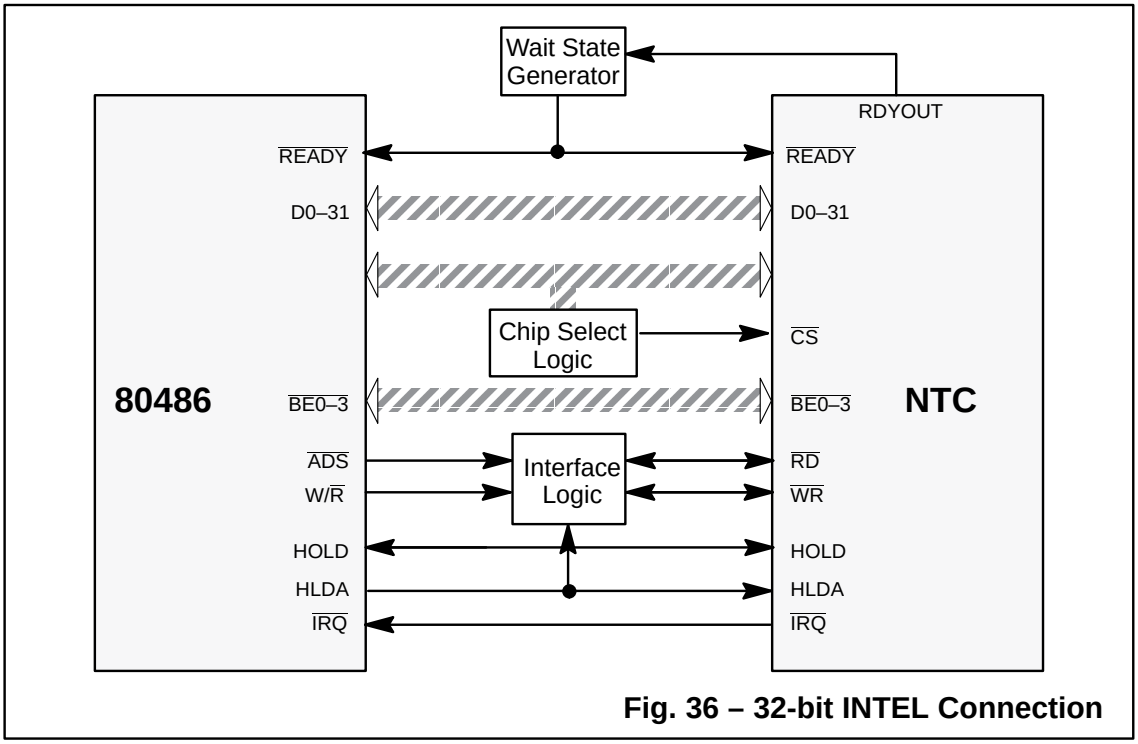


Fig. 36 – 32-bit INTEL Connection

4.3 Big / Little Endian DMA Formats

4.3.1 Network Statistics Record DMA Format

Network Statistics data is always transferred as Big Endian data.

Fig. 37 below, shows the NSR DMA data format in 16 bit mode and Fig. 38 on page 66 shows the data in 32 bit mode.

	D_{15}	D_0
1	TIMESTAMP Byte 3 (MSB)	TIMESTAMP Byte 2
2	TIMESTAMP Byte 1	TIMESTAMP Byte 0 (LSB)
3	D COUNT Byte 3 (MSB)	D COUNT Byte 2
4	D COUNT Byte 1	D COUNT Byte 0 (LSB)
5	R COUNT Byte 3 (MSB)	R COUNT Byte 2
6	R COUNT Byte 1	R COUNT Byte 0 (LSB)
7	T COUNT Byte 3 (MSB)	T COUNT Byte 2
8	T COUNT Byte 1	T COUNT Byte 0 (LSB)
9	HED Byte 1 (MSB)	HED Byte 0 (LSB)
10	HEC Byte 1 (MSB)	HEC Byte 0 (LSB)
11	Section FEBE Byte 1 (MSB)	Section FEBE Byte 0 (LSB)
12	Path FEBE Byte 1 (MSB)	Path FEBE Byte 0 (LSB)
13	Unassigned RX Byte 1 (MSB)	Unassigned RX Byte 0 (LSB)
14	Unassigned TX Byte 1 (MSB)	Unassigned TX Byte 0 (LSB)
15	ATE RX Byte 1 (MSB)	ATE RX Byte 0 (LSB)
16	ATE TX Byte 1 (MSB)	ATE TX Byte 0 (LSB)
17	USER Cell Entry 1A Byte 3 (MSB)	USER Cell Entry 1A Byte 2
18	USER Cell Entry 1A Byte 1	USER Cell Entry 1A Byte 0 (LSB)
19	USER Cell Entry 2A Byte 3 (MSB)	USER Cell Entry 2A Byte 2
20	USER Cell Entry 2A Byte 1	USER Cell Entry 2A Byte 0 (LSB)
287	USER Cell Entry 32B Byte 3 (MSB)	USER Cell Entry 32B Byte 2
288	USER Cell Entry 32B Byte 1	USER Cell Entry 32B Byte 0 (LSB)

Fig. 37 – Network Statistics Record 16 Bit DMA Format

	D_{31}			D_0
1	TIMESTAMP Byte 3 (MSB)	TIMESTAMP Byte 2	TIMESTAMP Byte 1	TIMESTAMP Byte 0 (LSB)
2	D COUNT Byte 3 (MSB)	D COUNT Byte 2	D COUNT Byte 1	D COUNT Byte 0 (LSB)
3	R COUNT Byte 3 (MSB)	R COUNT Byte 2	R COUNT Byte 1	R COUNT Byte 0 (LSB)
4	T COUNT Byte 3 (MSB)	T COUNT Byte 2	T COUNT Byte 1	T COUNT Byte 0 (LSB)
5	HED Byte 1 (MSB)	HED Byte 0 (LSB)	HEC Byte 1 (MSB)	HEC Byte 0 (LSB)
6	Section FEBE Byte 1 (MSB)	Section FEBE Byte 0 (LSB)	Path FEBE Byte 1 (MSB)	Path FEBE Byte 0 (LSB)
7	Unassigned RX Byte 1 (MSB)	Unassigned RX Byte 0 (LSB)	Unassigned TX Byte 1 (MSB)	Unassigned TX Byte 0 (LSB)
8	ATE Count RX Byte 1 (MSB)	ATE Count RX Byte 0 (LSB)	ATE Count TX Byte 1 (MSB)	ATE Count TX Byte 0 (LSB)
9	USER Cell Entry 1A Byte 3 (MSB)	USER Cell Entry 1A Byte 2	USER Cell Entry 1A Byte 1	USER Cell Entry 1A Byte 0 (LSB)
10	USER Cell Entry 2A Byte 3 (MSB)	USER Cell Entry 2A Byte 2	USER Cell Entry 2A Byte 1	USER Cell Entry 2A Byte 0 (LSB)
144	USER Cell Entry 32B Byte 3 (MSB)	USER Cell Entry 32B Byte 2	USER Cell Entry 32B Byte 1	USER Cell Entry 32B Byte 0 (LSB)

Fig. 38 – Network Statistics Record 32 Bit Mode DMA Format

4.3.2 Switch Statistics DMA Format

The DMA byte format in both 16 and 32 bit modes is shown below in Fig. 39.

This data is always transferred in Big Endian mode to preserve its integrity as it crosses byte boundaries.

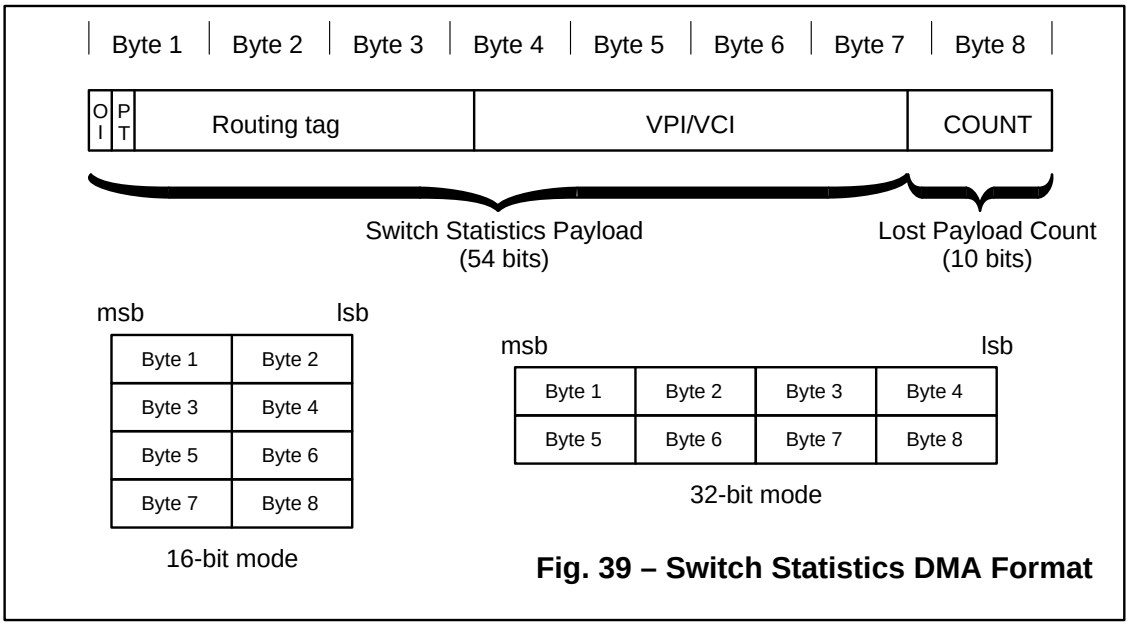


Fig. 39 – Switch Statistics DMA Format

4.3.3 Cell Insertion/Extraction – DMA Channels

Fig. 40 shows Big and Little Endian formats for the insertion or extraction of cells in 16 bit mode.

Fig. 41 shows similar information for 32 bit mode.

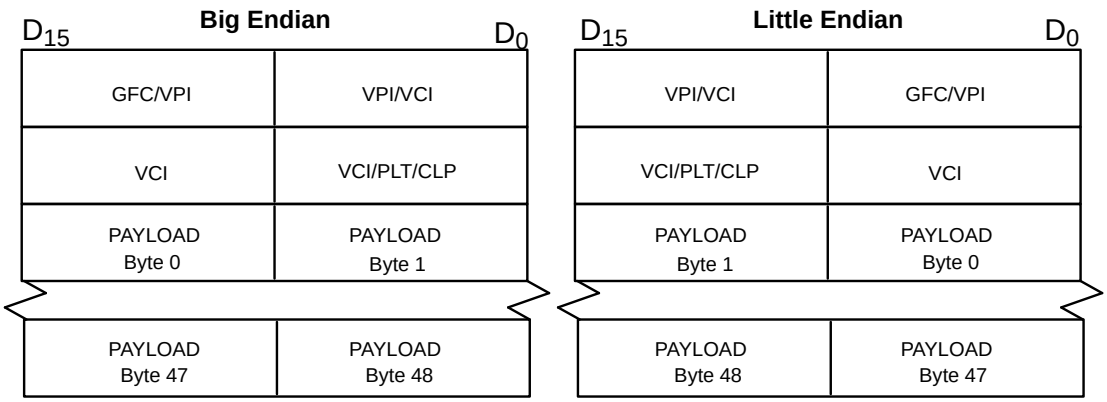


Fig. 40 – Cell Insertion/Extraction 16 Bit Mode DMA Format

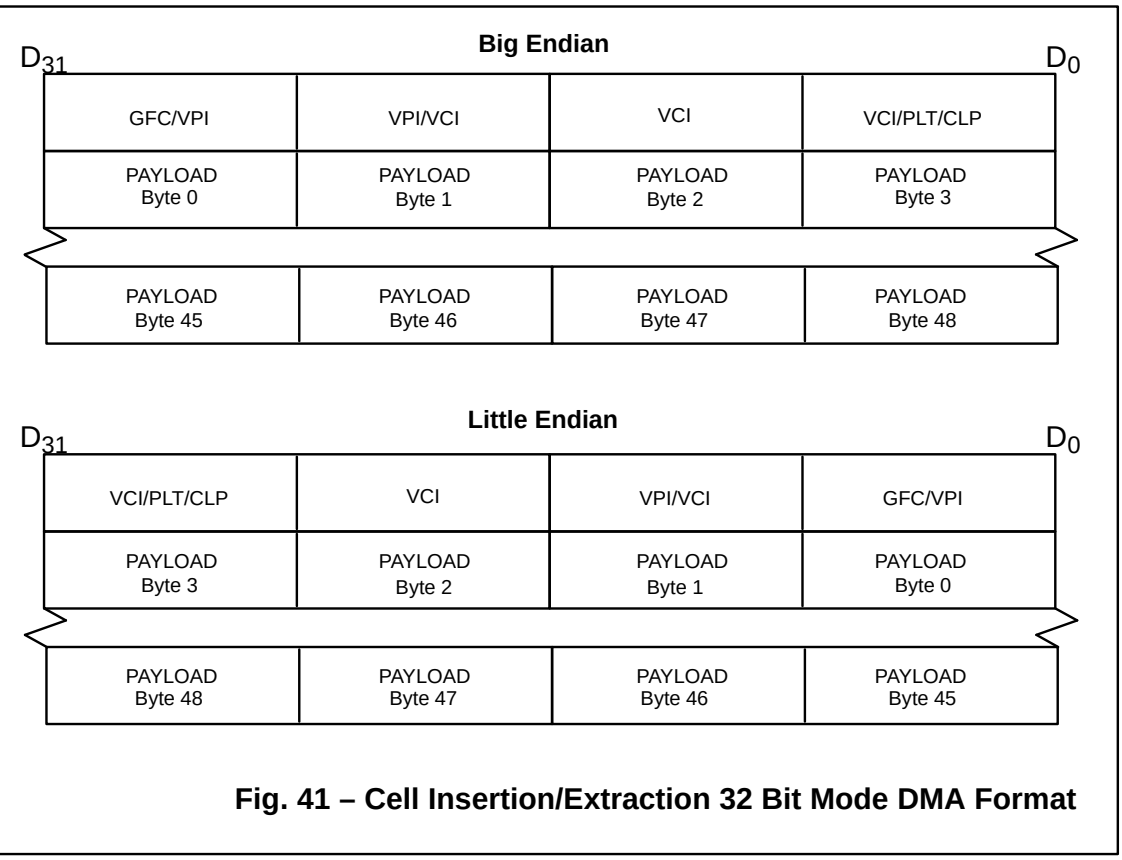


Fig. 41 – Cell Insertion/Extraction 32 Bit Mode DMA Format

4.4 Microprocessor Slave Access Functional Timing

The following diagrams represent the functional timing associated with the RDYOUT signal.

Fig. 42 and Fig. 43 show INTEL 16 bit Slave read and write timings while Fig. 44, Fig. 45 and Fig. 46 show INTEL 32 bit long word, even and odd word read accesses; Fig. 47 to Fig. 49 show INTEL 32 bit long word, even and odd word write accesses; Fig. 50 to Fig. 57 show similar information in the same order for Motorola mode.

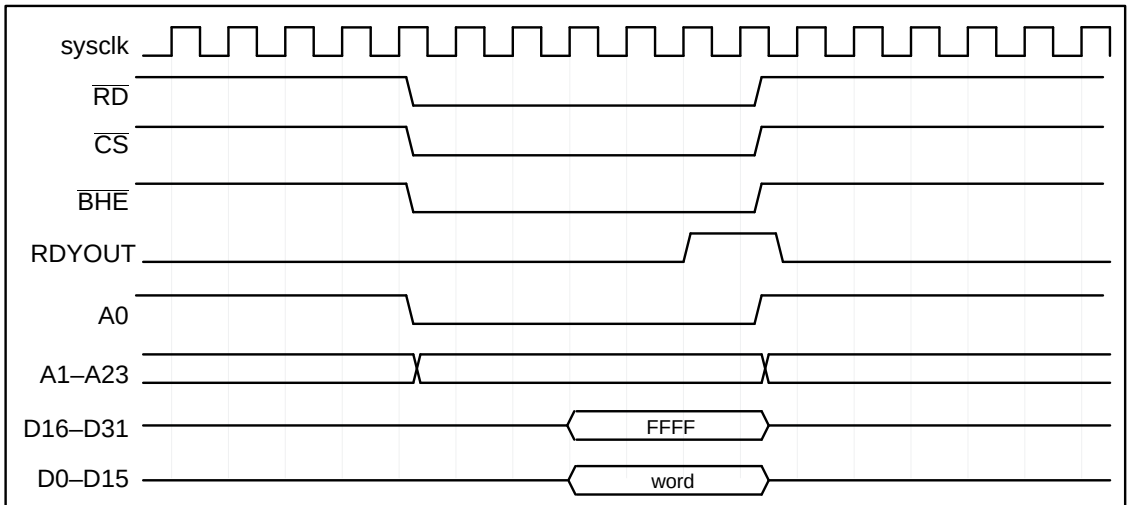


Fig. 42 – INTEL 16–bit Slave Read Timing

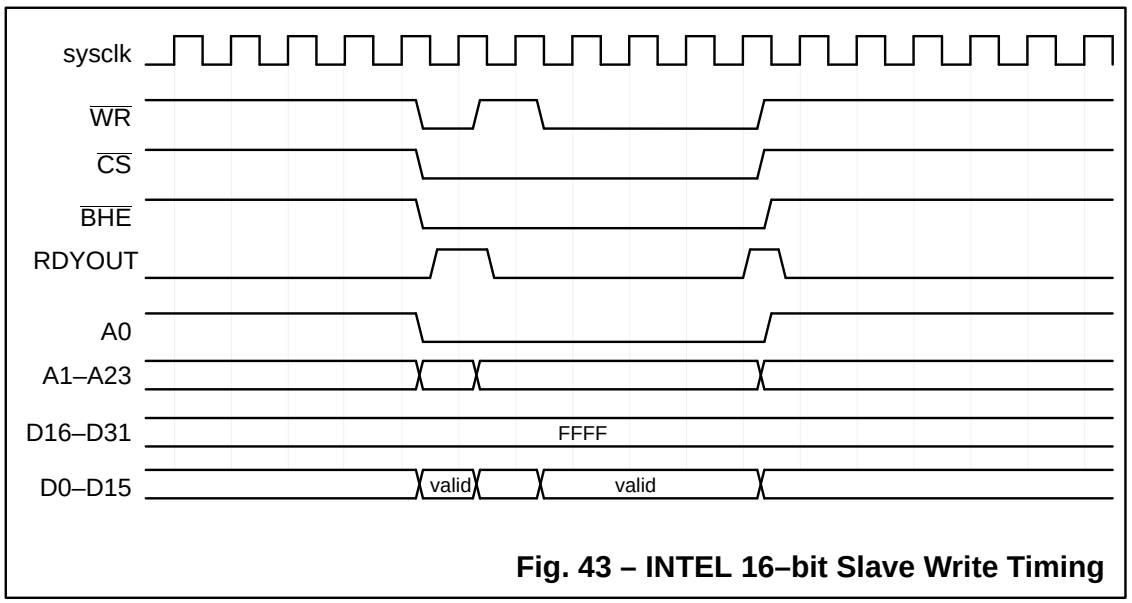


Fig. 43 – INTEL 16–bit Slave Write Timing

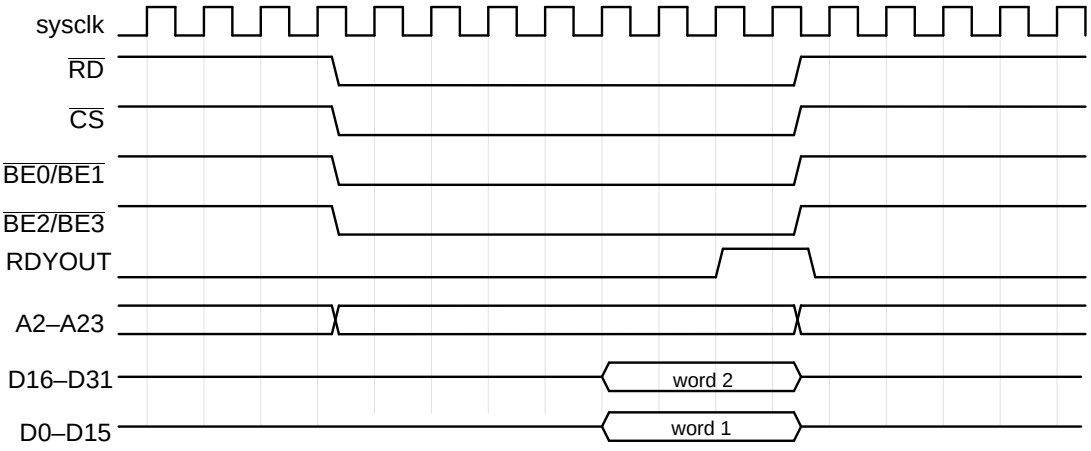


Fig. 44 – INTEL 32–bit Slave Read Timing (Long word access)

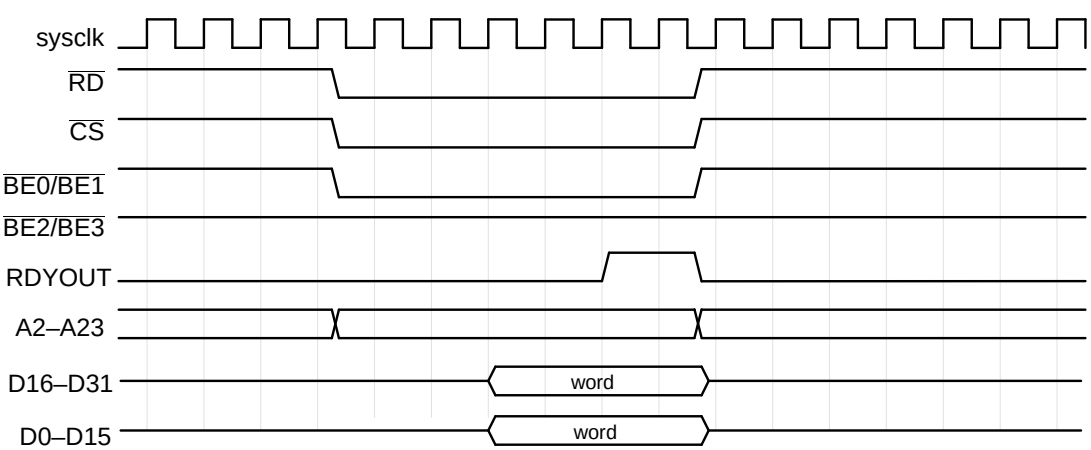


Fig. 45 – INTEL 32–bit Slave Read Timing (Word access – even)

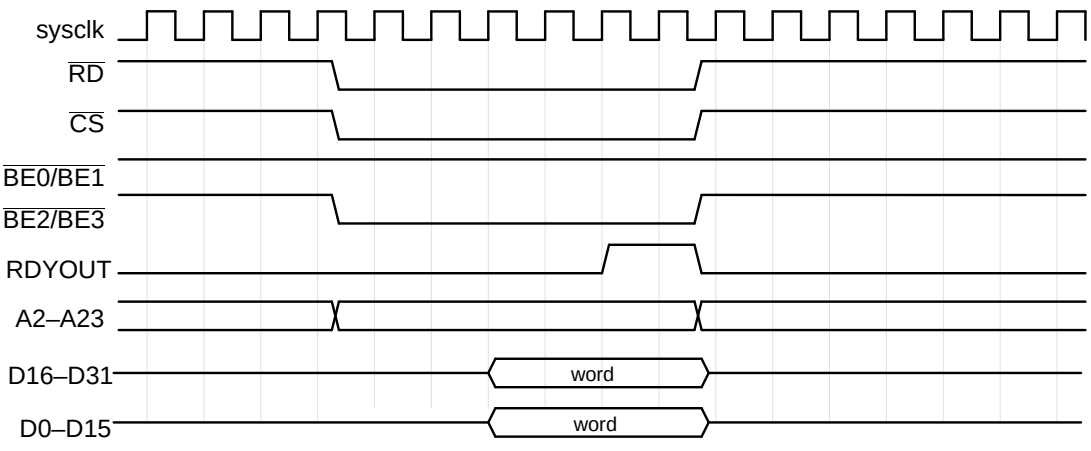


Fig. 46 – INTEL 32–bit Slave Read Timing (Word access – odd)

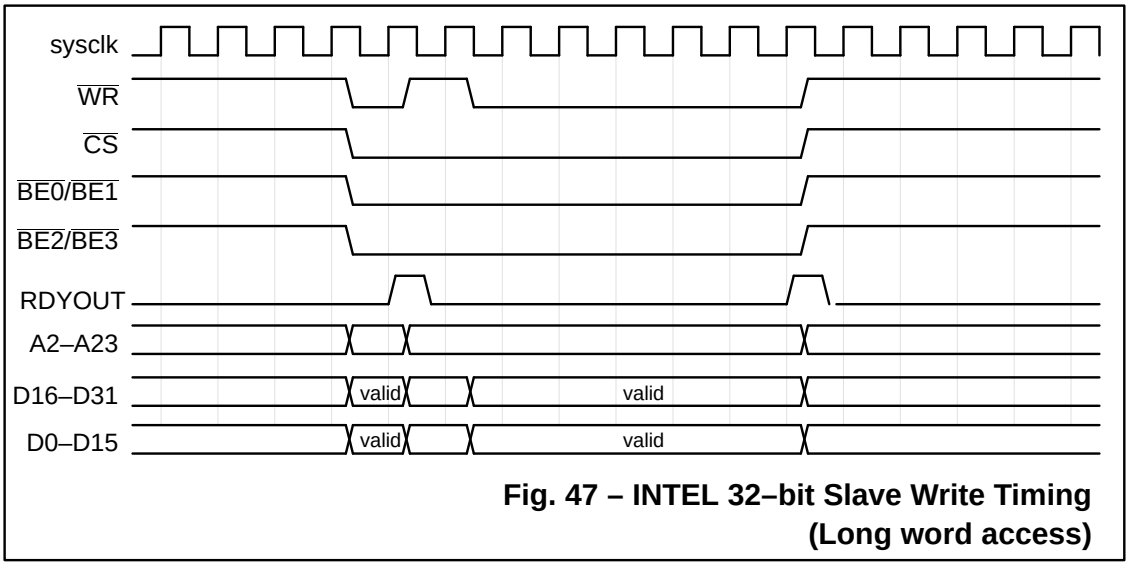


Fig. 47 – INTEL 32–bit Slave Write Timing (Long word access)

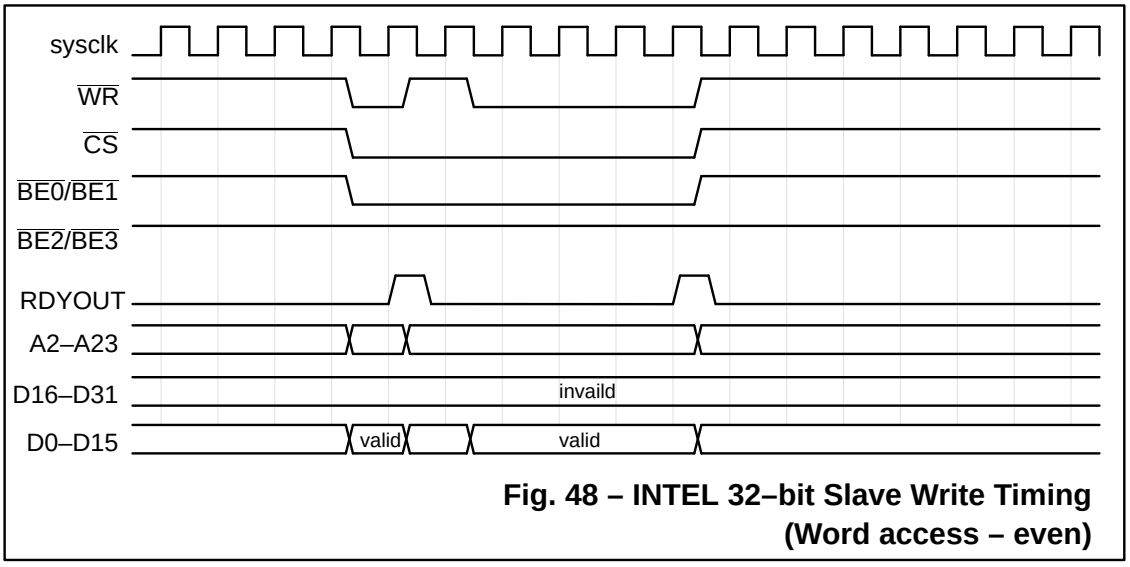


Fig. 48 – INTEL 32–bit Slave Write Timing (Word access – even)

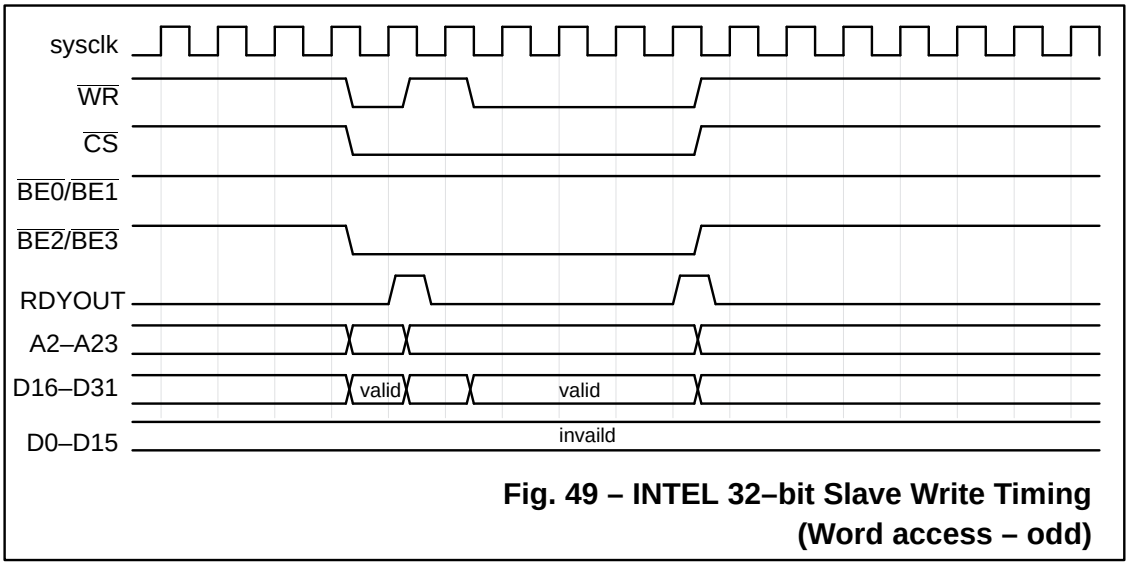


Fig. 49 – INTEL 32–bit Slave Write Timing (Word access – odd)

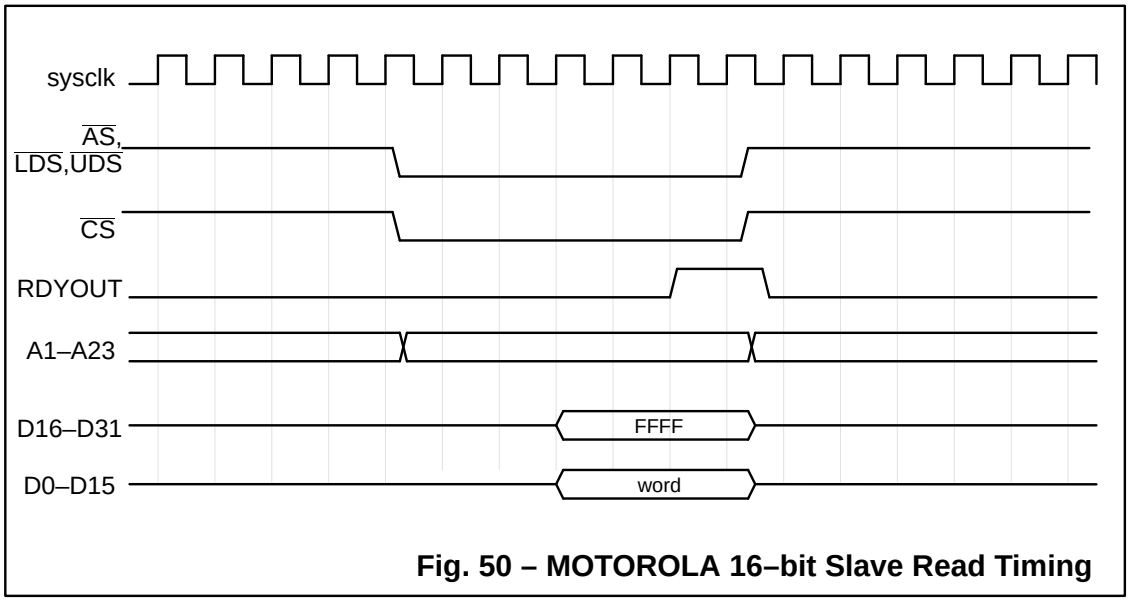


Fig. 50 – MOTOROLA 16–bit Slave Read Timing

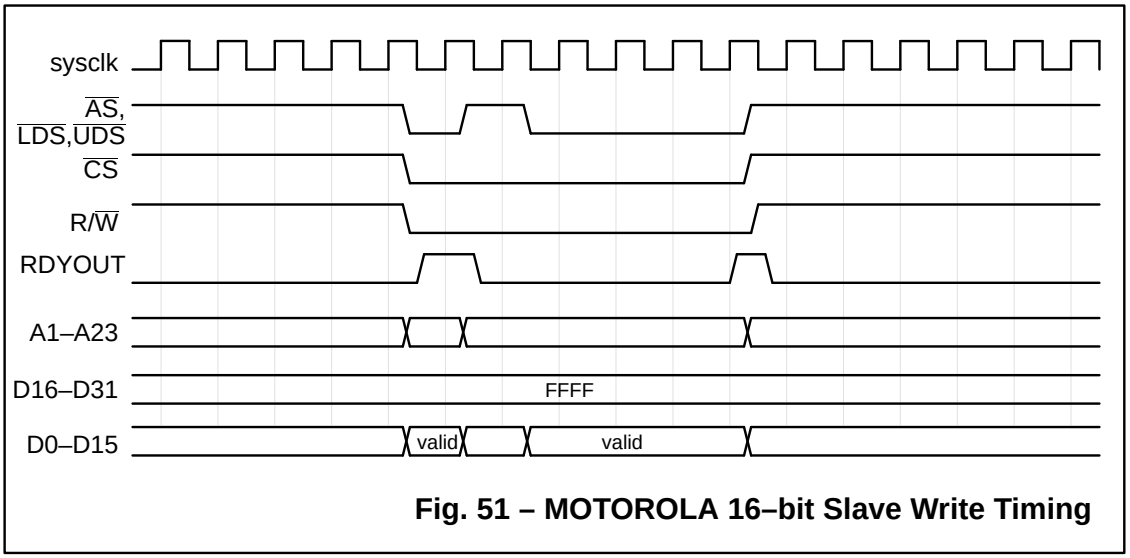


Fig. 51 – MOTOROLA 16–bit Slave Write Timing

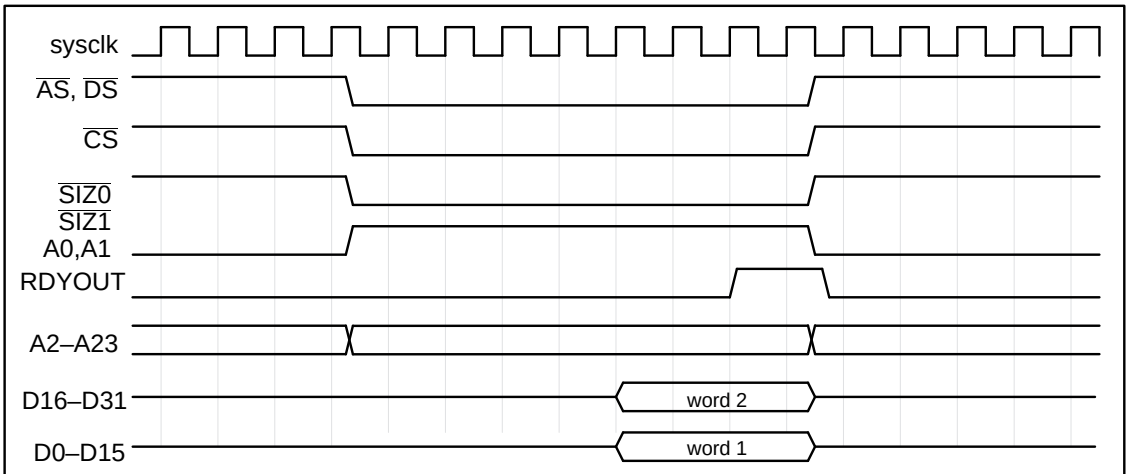


Fig. 52 – Motorola 32–bit Slave Read Timing (Long word access)

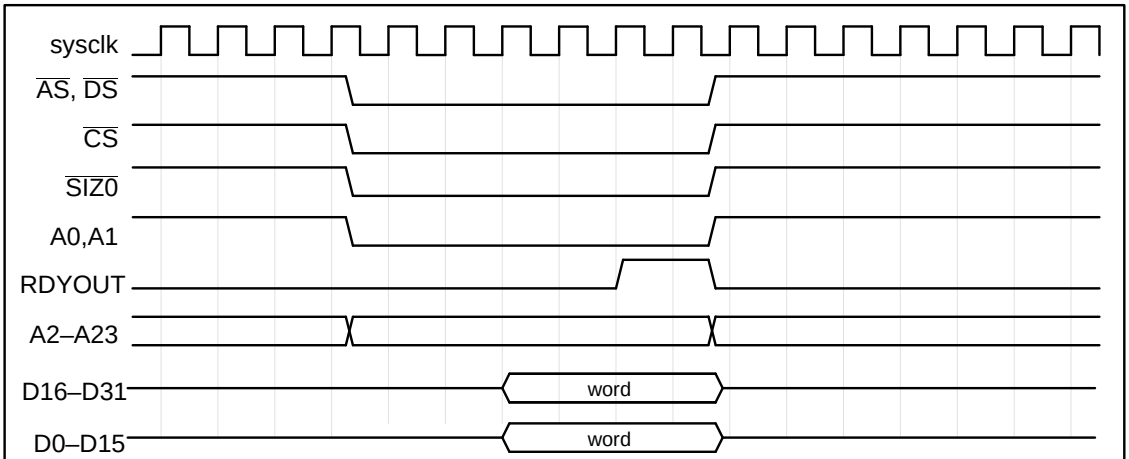


Fig. 53 – Motorola 32–bit Slave Read Timing (Word access – even)

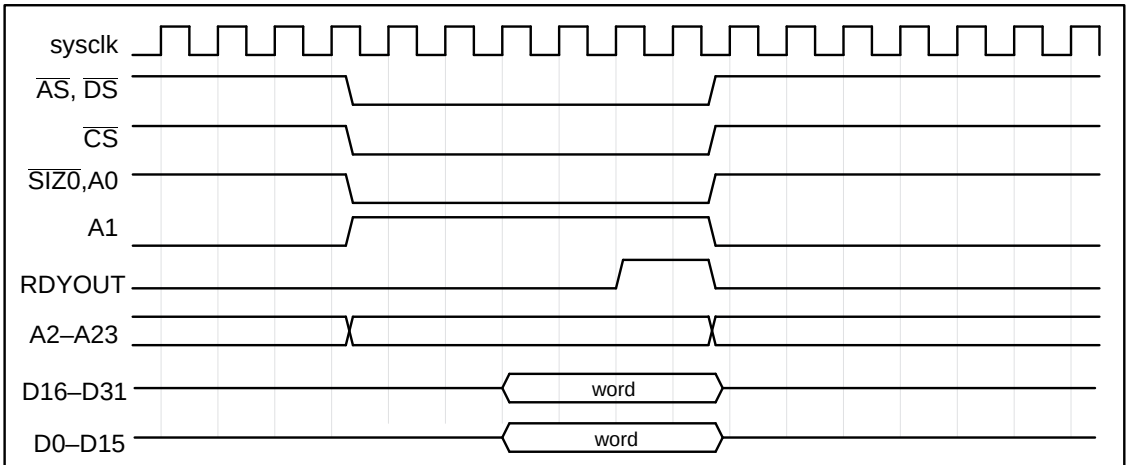


Fig. 54 – Motorola 32–bit Slave Read Timing (Word access – odd)

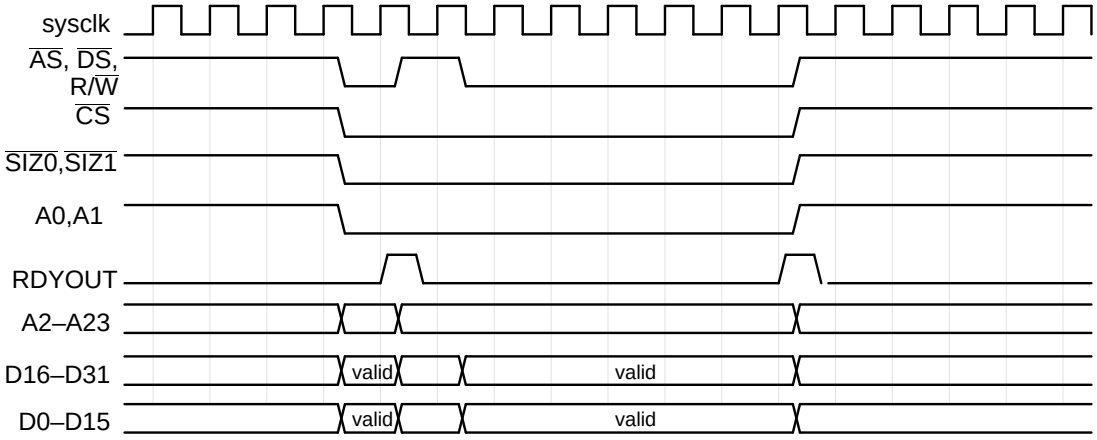


Fig. 55 – Motorola 32–bit Slave Write Timing (Long word access)

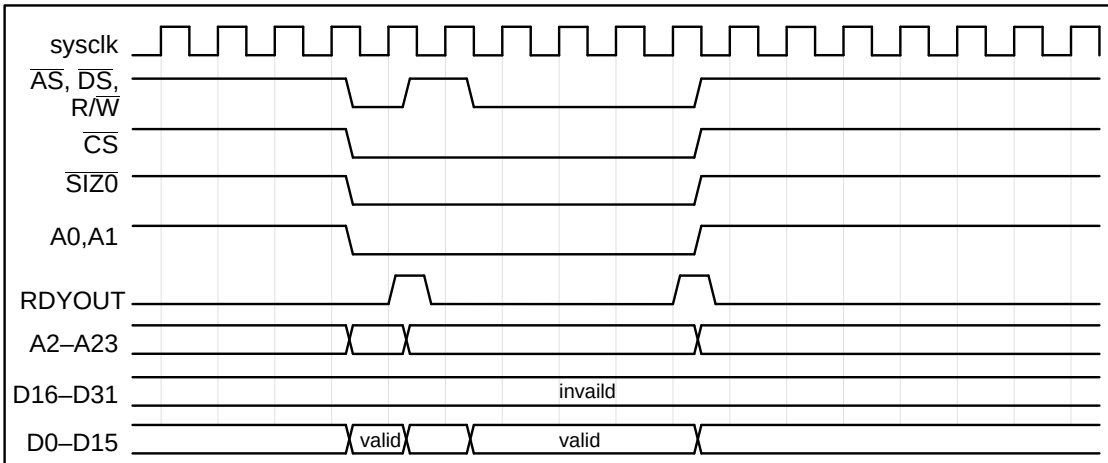


Fig. 56 – Motorola 32–bit Slave Write Timing (Word access – even)

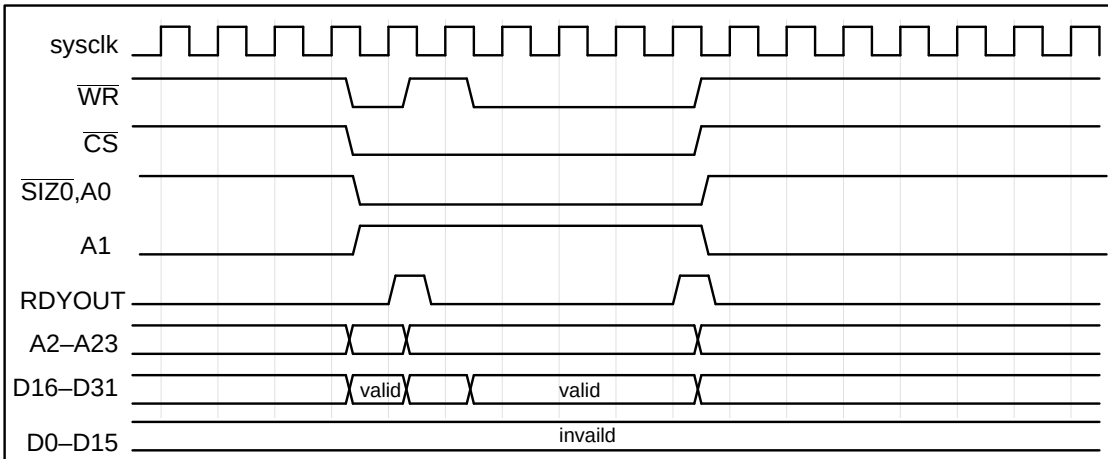


Fig. 57 – Motorola 32–bit Slave Write Timing (Word access – odd)

4.5 Functional Timing of DMA Arbitration and Chaining

The following diagrams illustrate the timings for DMA arbitration during single and multiple bus requests.

Fig. 58 shows timings in Motorola Mode with a single bus request while Fig. 59 shows timings for a multiple bus request.

Fig. 60 shows an example of chaining arbitration timing with 3 NTCs in Intel Mode.

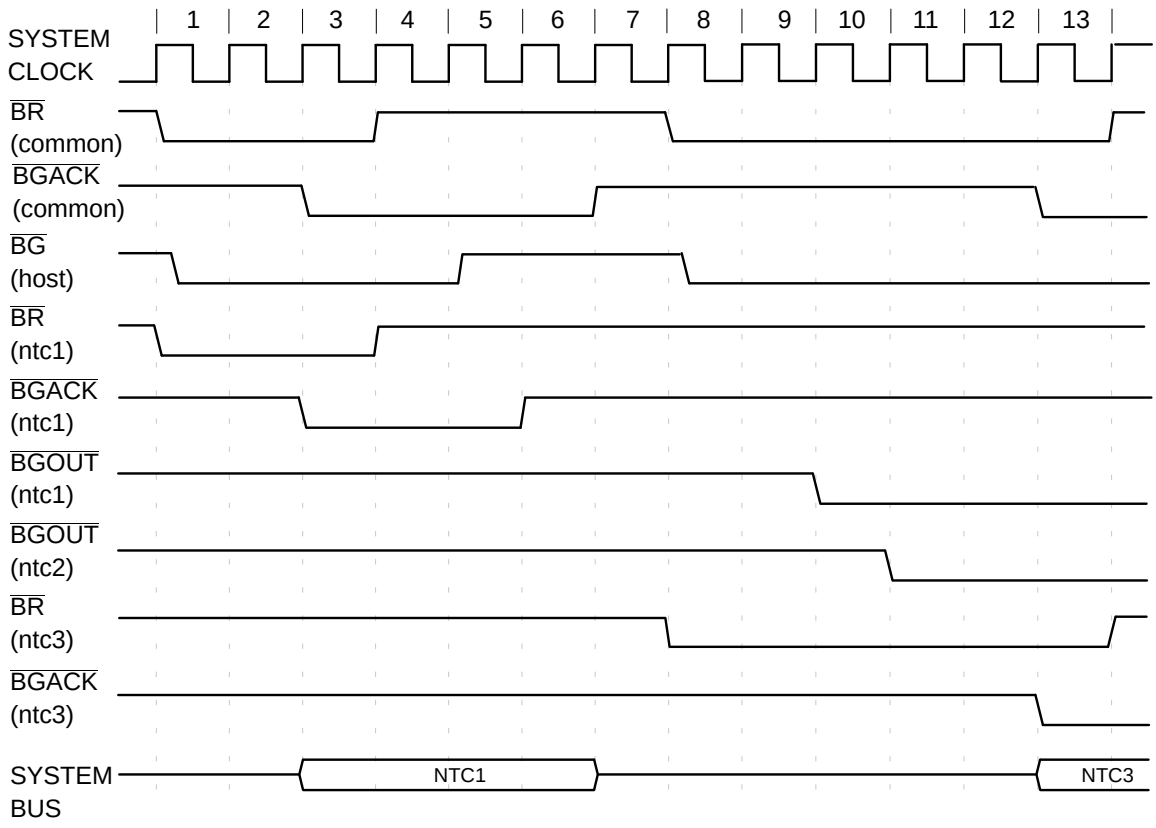


Fig. 58 – Chaining Timings Motorola Mode – Single Bus Request

Once NTC1 completes its bus access, it does not chain on since no other devices requesting at that time. When NTC3 does request the bus, $\overline{BG}$ is passed down the chain.

Please note that the timing is meant only as a representation of what should happen and that actual delays will vary.

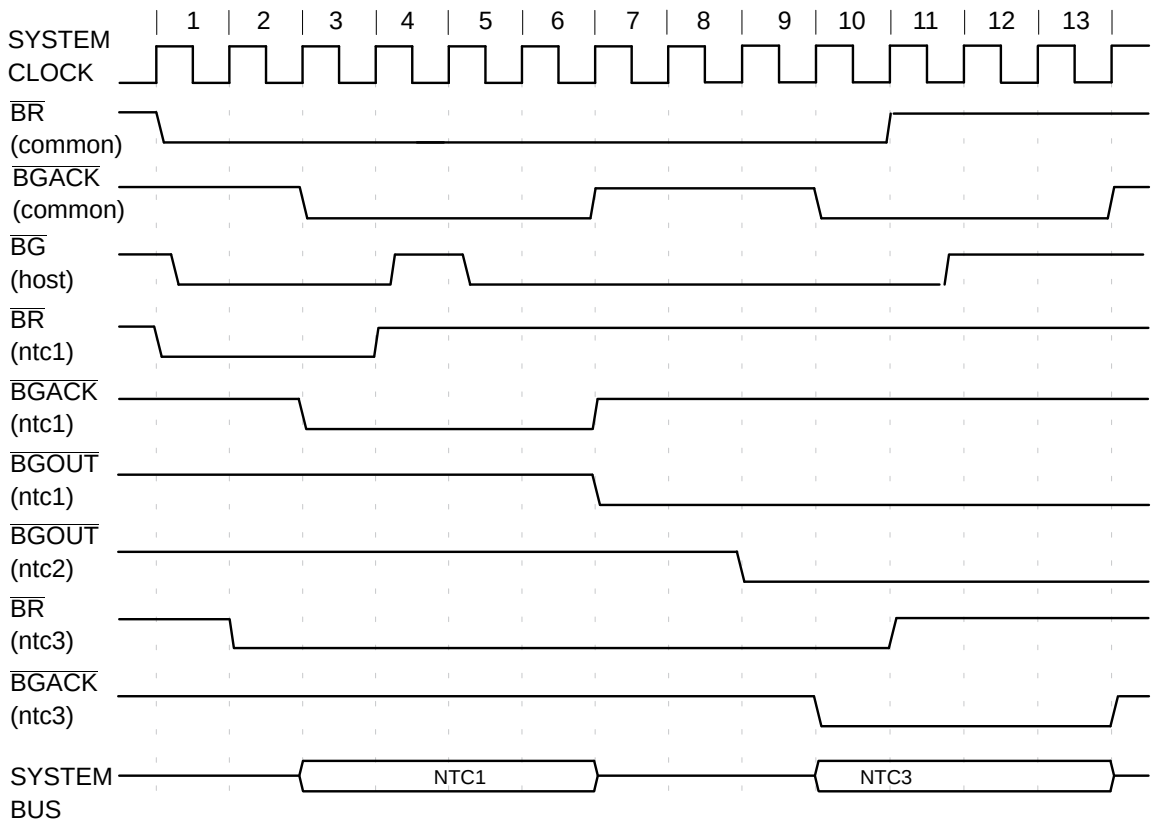


Fig. 59 – Chaining Timings Motorola Mode – Multiple Bus Request

Once NTC1 completes its bus access, it chains on since NTC3 is requesting the bus and $\overline{BG}$ is reasserted prior to the processor performing any external bus cycles.

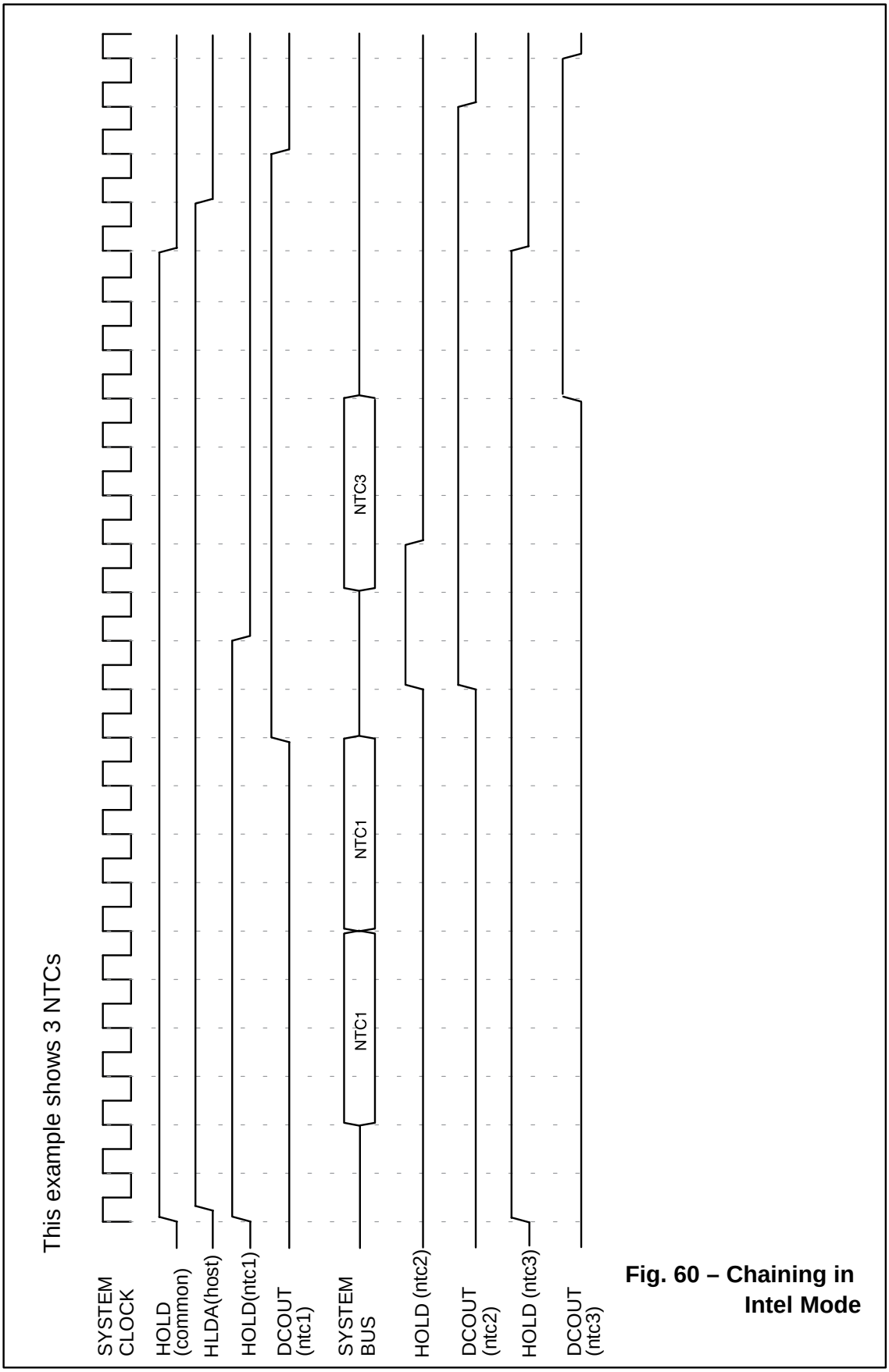


Fig. 60 – Chaining in Intel Mode

A. REGISTER TABLE

A.1 Control Registers

REG	ADDRESS AD0–6	FUNCTION	ACCESS
0	00h	Tx/Rx Framer Control	R / W
1	02h	General Framer Control	R / W
2	04h	Transmit Framer Overhead Access Bytes Block 1	W
3	06h	Transmit Framer Overhead Access Bytes Block 2	W
4	08h	Transmit Framer Overhead Access Bytes Block 3	W
5	0Ah	Transmit Framer Overhead Access Bytes Block 4	W
6	0Ch	Transmit Framer Overhead Access Bytes Block 5	W
7	0Eh	Transmit Framer Overhead Access Bytes Block 6	W
8	10h	Transmit Framer Overhead Access Bytes Block 7	W
9	12h	Transmit Framer Overhead Access Bytes Block 8	W
10	14h	Transmit Framer Overhead Access Bytes Block 9	W
11	16h	Transmit Framer Overhead Access Bytes Block 10	W
12	18h	Transmit Framer Overhead Access Bytes Block 11	W
13	1Ah	Transmit Framer Overhead Access Bytes Block 12	W
14	1Ch	Transmit Framer Overhead Access Bytes Block 13	W
15	1Eh	Transmit Framer Overhead Access Bytes Block 14	W
16	20h	Transmit Framer Overhead Access Bytes Block 15	W
17	22h	Transmit Framer Overhead Access Bytes Block 16	W
18	24h	Cell Receiver General Control	R / W
19	26h	Cell Receiver HEC / Descrambler Control	R / W
20	28h	Cell Receiver User Defined Extract/Discard XMASK #1	R / W
21	2Ah	Cell Receiver User Defined Extract/Discard XMASK #2	R / W
22	2Ch	Cell Receiver User Defined Extract/Discard SMASK #1	R / W
23	2Eh	Cell Receiver User Defined Extract/Discard SMASK #2	R / W
24	30h	Cell Receiver Extract Buffer Control	R / W
25	32h	Cell Receiver Discard Control	R / W
26	34h	Cell Transmitter General Control	R / W
27	36h	Cell Transmitter HEC / Scrambler Control	R / W
28	38h	Cell Transmitter User Defined Extract/Discard XMASK #1	R / W
29	3Ah	Cell Transmitter User Defined Extract/Discard XMASK #2	R / W
30	3Ch	Cell Transmitter User Defined Extract/Discard SMASK #1	R / W
31	3Eh	Cell Transmitter User Defined Extract/Discard SMASK #2	R / W

Control Registers (continued)

REG	ADDRESS AD0–6	FUNCTION	ACCESS
32	40h	Cell Transmitter Extract Buffer Control	R / W
33	42h	Cell Transmitter Discard Control	R / W
34	44h	OAM Framed Alarm Control	R / W
35	46h		
36	48h		
37	4Ah		
38	4Ch		
39	4Eh		
40	50h		
41	52h		
42	54h		
43	56h		
44	58h		
45	5Ah		
46	5Ch		
47	5Eh		
48	60h	Reserved *	R / W
49	62h	Reserved *	R / W
50	64h	Switch Statistics Handler Control	R / W
51	66h	Network Statistics General Control	R / W
52	68h	Network Statistics User Cell Mask XMASK#1	R / W
53	6Ah	Network Statistics User Cell Mask XMASK#2	R / W
54	6Ch	Network Statistics User Cell Mask SMASK#1	R / W
55	6Eh	Network Statistics User Cell Mask SMASK#2	R / W
56	70h	Cell Stream Interface Control #1	R / W
57	72h	Cell Stream Interface Control #2	R / W
58	74h	Interrupt Enable	W
59	76h	Interrupt Under Service	W
60	78h	DMA Descriptor Pointer Table Low	W
61	7Ah	DMA Descriptor Pointer Table High	W
62	7Ch	DMA Channel Activity	W
63	7Eh	DMA Mode	W

* Note : These registers can only be configured with a value of 0000h

A.2 Status Registers

REG	ADDRESS AD0–6	FUNCTION	ACCESS
0	00h		
1	02h		
2	04h	Receive Framer Overhead Access Bytes Block 1	R
3	06h	Receive Framer Overhead Access Bytes Block 2	R
4	08h	Receive Framer Overhead Access Bytes Block 3	R
5	0Ah	Receive Framer Overhead Access Bytes Block 4	R
6	0Ch	Receive Framer Overhead Access Bytes Block 5	R
7	0Eh	Receive Framer Overhead Access Bytes Block 6	R
8	10h	Receive Framer Overhead Access Bytes Block 7	R
9	12h	Receive Framer Overhead Access Bytes Block 8	R
10	14h	Receive Framer Overhead Access Bytes Block 9	R
11	16h	Receive Framer Overhead Access Bytes Block 10	R
12	18h	Receive Framer Overhead Access Bytes Block 11	R
13	1Ah	Receive Framer Overhead Access Bytes Block 12	R
14	1Ch	Receive Framer Overhead Access Bytes Block 13	R
15	1Eh	Receive Framer Overhead Access Bytes Block 14	R
16	20h	Receive Framer Overhead Access Bytes Block 15	R
17	22h	Receive Framer Overhead Access Bytes Block 16	R
18	24h	Not Used	
19	26h	Not Used	
20	28h	Not Used	
21	2Ah	Not Used	
22	2Ch	Not Used	
23	2Eh	Not Used	
24	30h	Not Used	
25	32h	Not Used	
26	34h	Not Used	
27	36h	Not Used	
28	38h	Not Used	
29	3Ah	Not Used	
30	3Ch	Not Used	
31	3Eh	Not Used	

Status Registers (continued)

REG	ADDRESS AD0–6	FUNCTION	ACCESS
32	40h	Not Used	
33	42h	Not Used	
34	44h	Not Used	
35	46h	Not Used	
36	48h	Not Used	
37	4Ah	Not Used	
38	4Ch	Not Used	
39	4Eh	Not Used	
40	50h	Not Used	
41	52h	Not Used	
42	54h	Not Used	
43	56h	Not Used	
44	58h	Not Used	
45	5Ah	Not Used	
46	5Ch	Not Used	
47	5Eh	Not Used	
48	60h	Not Used	
49	62h	Not Used	
50	64h	Not Used	
51	66h	Not Used	
52	68h	Not Used	
53	6Ah	Not Used	
54	6Ch	Not Used	
55	6Eh	Not Used	
56	70h	Not Used	
57	72h	CSI Receive/Transmit Buffer Fill Levels	R
58	74h	Inetrrupt Status Register	R
59	76h	Physical Layer Alarms Received	R
60	78h	Not Used	
61	7Ah	Internal Buffer Overflow Interrupt Indication	R
62	7Ch	DMA Channel Activity	R
63	7Eh	BERR/DMA Interrupt Indication	R

B. REGISTER MAPS

B.1 Control Registers

Control Register 0 – Rx/Tx Framer Control

D15

						FTXENB	FRXENB

D0

FRXENB: Rx Framer Enable
0 : Disabled (Reset)
1 : Enabled (Not Reset)

FTXENB: Tx Framer Enable
0 : Disabled (Reset)
1 : Enabled (Not Reset)

Control Register 1 – General Framer Control

D15

P3	P2	P1	P0	N3	N2	N1	N0
LOOPBACK	STMDESC	STMSCR	TESTMODE	XMODE2	XMODE1	XMODE0	

D0

XMODE2–0: Transceiver mode
000 : Unframed
001 : SDH (STM–1)
010 : SONET (STS–3c)
011 : DS3 (with PLCP)
100 : E3
101 : SONET (STS–1)
110 : DS3 (non PLCP)

TESTMODE: Internal Testmode (User should set to zero)
0 : Disabled
1 : Enabled

STMSCR: $1+x^6+x^7$frame scrambler
0 : Disabled
1 : Enabled

STMDESC: $1+x^6+x^7$ frame descrambler
0 : Disabled
1 : Enabled

LOOPBACK: TX to RX framer loopback
0 : Disabled
1 : Enabled

N3–N0 : Frame sync found count (1 – 15)

P3–P0 : Frame sync lost count (1 – 15)

Note: N3–0 and P3–0 are used on the following framing bytes:

SDH & SONET	: A1, A2
DS3	: F1, F2, F3, F4
E3	: FA1, FA2

Control Registers 2 – 17 (see below)

Control registers 2 to 17 provide access to 32 frame overhead bytes. These are illustrated in the table below for the various modes of operation.

CONTROL REG		TRANSMIT FRAMER OVERHEAD ACCESS BYTES					
REG NO.	REG ADDR	SDH / SONET		E3		DS3 (PCLP)	
		D15 – D8	D7 – D0	D15 – D8	D7 – D0	D15 – D8	D7 – D0
2	04h	C1	R1	TR	NR		see note
3	06h	R2	E1	UC			
4	08h	F1	R3				
5	0Ah	R4	D1				
6	0Ch	D2	D3				
7	0Eh	K1	D4				
8	10h	D5	D6				
9	12h	D7	D8				
10	14h	D9	D10				
11	16h	D11	D12				
12	18h	Z1A	Z1B				
13	1Ah	Z1C	E2				
14	1Ch	R5	R6				
15	1Eh	J1	C2			Z6	Z5
16	20h	F2	Z3			Z4	Z3
17	22h	Z4	Z5			Z2	Z1

Note: D7 – D5 = 0
D4 – D0 = Five of the C–bits

D4 = C1 (AIC)
D3 = C3 (FEAC)
D2 = C13 (DL)
D1 = C14 (DL)
D0 = C15 (DL)

Control Register 18 – Cell Receiver General Control

D15							
TESTMODE							GFCIGN
PKIR3	PKIR2	PKIR1	PKIR0	INSPRI	CRC10GEN	CRC10CHK	CRXENB
							D0

CRXENB:	Cell Receiver Enable	0 : Disabled (Reset) 1 : Enabled (Not Reset)
CRC10CHK :	OAM Cell CRC Check	0 : Disabled 1 : Enabled
CRC10GEN :	OAM Cell CRC Generate	0 : Disabled 1 : Enabled
INSPRI :	Cell Insert Priority	0 : User cells have priority 1 : Insert Buffer cells have priority
PKIR3–0:	Peak cell insertion rate (from insert buffer)	0–11 : See Note below.
GFCIGN :	GFC field Ignore (predefined cells)	0 : 12–bit VPI 1 : 8–bit VPI
TESTMODE :	Internal Testmode (User should set to zero)	0 : Disabled 1 : Enabled

Note:

PKIR3–0 specifies the maximum cell insertion rate via the insert buffer.
The rate is defined by the following relationship:

1 inserted cell in $2^{(13–PKIR)}$ transmitted cells.

eg. For SDH / SONET (155.52 Mbps):

PKIR = 0 :– Max insert rate = 1 in 2^{13} cells (ie equivalent to 19 Kbps)

PKIR = 11 :– Max insert rate = 1 in 2^{2} cells (ie equivalent to 38.9 Mbps)

Control Register 19 – Cell Receiver HEC/Descrambler Control

D15

ALPHA3	ALPHA2	ALPHA1	ALPHA0	DELTA3	DELTA2	DELTA1	DELTA0
			BALIGN	COREN	HECMASK		DESCR

D0

DESCR : Payload Descrambler ($1 + x^{43}$)
0 : Disabled
1 : Enabled

HECMASK : HEC Receive Mask (55h = 01010101b)
0 : Disabled
1 : Enabled

COREN : Header Error Correction (single bit)
0 : Disabled
1 : Enabled

BALIGN: Byte Alignment
0 : Non–byte aligned data
1 : Byte aligned data

DELTA3–0 : Cell sync found count (1 – 15)

ALPHA3–0 : Cell sync lost count (1 – 15)

Control Register 20 – Cell Receiver User Defined Extract/Discard XMASK #1

D15

VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0	VPI7	VPI6	VPI5	VPI4
VPI3	VPI2	VPI1	VPI0	VCI15	VCI14	VCI13	VCI12

D0

Control Register 21 – Cell Receiver User Defined Extract/Discard XMASK #2

D15

VCI11	VCI10	VCI9	VCI8	VCI7	VCI6	VCI5	VCI4
VCI3	VCI2	VCI1	VCI0	PLT2	PLT1	PLT0	CLP

D0

Control Register 22 – Cell Receiver User Defined Extract/Discard SMASK #1

D15

VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0	VPI7	VPI6	VPI5	VPI4
VPI3	VPI2	VPI1	VPI0	VCI15	VCI14	VCI13	VCI12

D0

Control Register 23 – Cell Receiver User Defined Extract/Discard SMASK #2

D15

VCI11	VCI10	VCI9	VCI8	VCI7	VCI6	VCI5	VCI4
VCI3	VCI2	VCI1	VCI0	PLT2	PLT1	PLT0	CLP

D0

These registers are used for user defined cell extraction/discard within the cell receiver.

Each bit of the first 4 bytes of the cell header may be defined as X, 0, or 1.

The XMASK is used to define X states for each bit.
When set to 1, they represent an X for that bit.
When set to 0, the user defined cell extraction/discard will take the state defined in the SMASK.

Control Register 24 – Cell Receiver Extract Buffer Control

D15

				F5EEFMAD	F5SGFMAD	F4EEFMAD	F4SGFMAD
F1F3	F4F5PM	ILMISIG	PPSIG	BROADSIG	METASIG	USERDEF1	USERDEF0

D0

USERDEF1,0 :	User Defined Cell	00 : Extract disabled 01 : Extract all cells defined by mask 11 : Extract all cells not defined by mask 10 : Invalid
METASIG:	Meta Signalling	0 : Extract disabled 1 : Extract enabled
BROADSIG:	Broadcast Signalling	0 : Extract disabled 1 : Extract enabled
PPSIG :	Point–Point Signalling	0 : Extract disabled 1 : Extract enabled
ILMISIG:	ILMI Signalling	0 : Extract disabled 1 : Extract enabled
F4F5PM:	F4/F5 Performance Man	0 : Extract disabled 1 : Extract enabled
F1F3 :	F1/F3 PLOAM	0 : Extract disabled 1 : Extract enabled
F4SGFMAD:	F4 Segment (FM and AD)	0 : Extract disabled 1 : Extract enabled
F4EEFMAD:	F4 End–End (FM and AD)	0 : Extract disabled 1 : Extract enabled
F5SGFMAD:	F5 Segment (FM and AD)	0 : Extract disabled 1 : Extract enabled
F5EEFMAD:	F5 End–End (FM and AD)	0 : Extract disabled 1 : Extract enabled

Control Register 25 – Cell Receiver Discard Control

D15							
				F5EEFMAD	F5SGFMAD	F4EEFMAD	F4SGFMAD
	UNASS	ILMISIG	PPSIG	BROADSIG	METASIG	USERDEF1	USERDEF0
							D0

USERDEF1,0: User Defined Cell
00 : Discard disabled
01 : Discard all cells defined by mask
11 : Discard all cells not defined by mask
10 : Invalid

METASIG: Meta Signalling
0 : Discard disabled
1 : Discard enabled

BROADSIG: Broadcast Signalling
0 : Discard disabled
1 : Discard enabled

PPSIG: Point–Point Signalling
0 : Discard disabled
1 : Discard enabled

ILMISIG: ILMI Signalling
0 : Discard disabled
1 : Discard enabled

UNASS: Unassigned Cell
0 : Discard disabled
1 : Discard enabled

F4SGFMAD: F4 Segment (FM and AD)
0 : Discard disabled
1 : Discard enabled

F4EEFMAD: F4 End–End (FM and AD)
0 : Discard disabled
1 : Discard enabled

F5SGFMAD: F5 Segment (FM and AD)
0 : Discard disabled
1 : Discard enabled

F5EEFMAD: F5 End–End (FM and AD)
0 : Discard disabled
1 : Discard enabled

Control Register 26 – Cell Transmitter General Control

D15

TESTMODE						UNASGEN	GFCIGN
PKIR3	PKIR2	PKIR1	PKIR0	INSPRI	CRC10GEN	CRC10CHK	CTXENB

D0

CTXENB:	Cell Transmitter Enable	0 : Disabled (Reset) 1 : Enabled (Not Reset)
CRC10CHK:	OAM Cell CRC Check	0 : Disabled 1 : Enabled
CRC10GEN:	OAM Cell CRC Generate	0 : Disabled 1 : Enabled
INSPRI :	Cell insert Priority	0 : User cells have priority 1 : Insert Buffer cells have priority
PKIR3–0:	Peak cell insertion rate (from insert buffer)	0–11 : See Note below.
GFCIGN :	GFC field Ignore (predefined cells)	0 : 12–bit VPI 1 : 8–bit VPI
UNASGEN:	Cell Rate Decoupling	0 : Idle cells generated 1 : Unassigned cells generated
TESTMODE :	Internal Testmode (User should set to zero)	0 : Disabled 1 : Enabled

Note:

PKIR3–0 specifies the maximum cell insertion rate via the insert buffer.
The rate is defined by the following relationship:

1 inserted cell in $2^{(13–PKIR)}$ transmitted cells.

eg. For SDH / SONET (155.52 Mbps) :

PKIR = 0 :– Max insert rate = 1 in 2^{13} cells (ie equivalent to 19 Kbps)

PKIR = 11 :– Max insert rate = 1 in 2^{2} cells (ie equivalent to 38.9 Mbps)

Control Register 27 – Cell Transmitter HEC/Scrambler Control

D15

					HECMASK		SCRAM

D0

SCRAM: Payload Scrambler ($1 + x^{43}$)
0 : Disabled
1 : Enabled

HECMASK: HEC Transmit Mask (55h = 01010101b)
0 : Disabled
1 : Enabled

Control Register 28 – Cell Transmitter User Defined Extract/Discard XMASK #1

D15

VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0	VPI7	VPI6	VPI5	VPI4
VPI3	VPI2	VPI1	VPI0	VCI15	VCI14	VCI13	VCI12

D0

Control Register 29 – Cell Transmitter User Defined Extract/Discard XMASK #2

D15

VCI11	VCI10	VCI9	VCI8	VCI7	VCI6	VCI5	VCI4
VCI3	VCI2	VCI1	VCI0	PLT2	PLT1	PLT0	CLP

D0

Control Register 30 – Cell Transmitter User Defined Extract/Discard SMASK #1

D15

VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0	VPI7	VPI6	VPI5	VPI4
VPI3	VPI2	VPI1	VPI0	VCI15	VCI14	VCI13	VCI12

D0

Control Register 31 – Cell Transmitter User Defined Extract/Discard SMASK #2

D15

VCI11	VCI10	VCI9	VCI8	VCI7	VCI6	VCI5	VCI4
VCI3	VCI2	VCI1	VCI0	PLT2	PLT1	PLT0	CLP

D0

These registers are used for user defined cell extraction/discard within the cell transmitter.

Each bit of the first 4 bytes of the cell header may be defined as X, 0, or 1.

The XMASK is used to define X states for each bit.
When set to 1, they represent an X for that bit.
When set to 0, the user defined cell extraction/discard will take the state defined in the SMASK.

Control Register 32 – Cell Transmitter Extract Buffer Control

D15							D0
				F5EEFMAD	F5SGFMAD	F4EEFMAD	F4SGFMAD
	F4F5PM	ILMISIG	PPSIG	BROADSIG	METASIG	USERDEF1	USERDEF0

USERDEF1,0: User Defined Cell
00 : Extract disabled
01 : Extract all cells defined by mask
11 : Extract all cells not defined by mask
10 : Invalid

METASIG: Meta Signalling
0 : Extract disabled
1 : Extract enabled

BROADSIG: Broadcast Signalling
0 : Extract disabled
1 : Extract enabled

PPSIG: Point–Point Signalling
0 : Extract disabled
1 : Extract enabled

ILMISIG: ILMI Signalling
0 : Extract disabled
1 : Extract enabled

F4F5PM: F4/F5 Performance Man
0 : Extract disabled
1 : Extract enabled

F4SGFMAD: F4 Segment (FM and AD)
0 : Extract disabled
1 : Extract enabled

F4EEFMAD: F4 End–End (FM and AD)
0 : Extract disabled
1 : Extract enabled

F5SGFMAD: F5 Segment (FM and AD)
0 : Extract disabled
1 : Extract enabled

F5EEFMAD: F5 End–End (FM and AD)
0 : Extract disabled
1 : Extract enabled

Control Register 33 – Cell Transmitter Discard Control

D15

				F5EEFMAD	F5SGFMAD	F4EEFMAD	F4SGFMAD
	UNASS	ILMISIG	PPSIG	BROADSIG	METASIG	USERDEF1	USERDEF0

D0

USERDEF1,0:	User Defined Cell	00 : Discard disabled 01 : Discard all cells defined by mask 11 : Discard all cells not defined by mask 10 : Invalid
METASIG:	Meta Signalling	0 : Discard disabled 1 : Discard enabled
BROADSIG:	Broadcast Signalling	0 : Discard disabled 1 : Discard enabled
PPSIG:	Point–Point Signalling	0 : Discard disabled 1 : Discard enabled
ILMISIG:	ILMI Signalling	0 : Discard disabled 1 : Discard enabled
UNASS:	Unassigned Cell	0 : Discard disabled 1 : Discard enabled
F4SGFMAD:	F4 Segment (FM and AD)	0 : Discard disabled 1 : Discard enabled
F4EEFMAD:	F4 End–End (FM and AD)	0 : Discard disabled 1 : Discard enabled
F5SGFMAD:	F5 Segment (FM and AD)	0 : Discard disabled 1 : Discard enabled
F5EEFMAD:	F5 End–End (FM and AD)	0 : Discard disabled 1 : Discard enabled

Control Register 34 – OAM Alarm Control

D15

MSFEBE	PFEBE	MSAIS	PAIS	MSFERF1	MSFERF0	PFERF1	PFERF0
INVB1	INVB2	INVB3					OAMENB

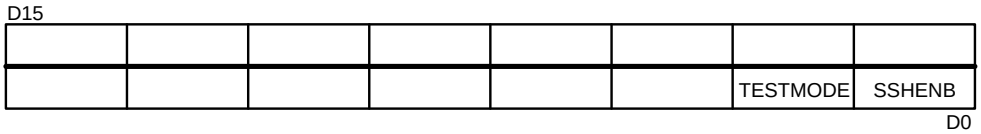
D0

OAMENB:	OAM Controller Enable	0 : Disabled (Reset) 1 : Enabled (Not Reset)
INVB1,2,3:	Invert BIP (B1, B2, B3) (see below)	0 : Normal BIP 1 : Inverted BIP
PAIS:	Tx Path AIS	0 : Clear 1 : Set
MSAIS:	Tx Section AIS	0 : Clear 1 : Set
PFERF1,0 :	Tx Path FERF	00 : Clear 10 : Set
MSFERF1,0 :	Tx Section FERF	00 : Clear 10 : Set
PFEBE:	Tx Path FEBE (B3)	0 : Disabled 1 : Enabled
MSFEBE:	Tx Section FEBE (B2)	0 : Disabled 1 : Enabled

Note 1:
INVB1,2,3 bits may be used for testing. Setting these bits will cause all the bits in the associated transmitted BIP field to be inverted.

Control Registers 35 – 49 Are Not Used

Control Register 50 – Switch Statistics Handler Control



SSHENB:	Switch Statistics Handler Enable	0 : Disabled (Reset) 1 : Enabled (Not Reset)
TESTMODE :	Internal Testmode (User should set to zero)	0 : Disabled 1 : Enabled

Control Register 51 – Network Statistics Record General Control

D15

FDMA	TBLOVF	CNTOVF	TIMERENB	TIME3	TIME2	TIME1	TIME0
TESTMODE		MASK1	MASK0	TXSTAT	RXSTAT	MODE1	MODE0

D0

MODE1, 0:	Statistics Controller Mode (Table size)	00 : Disabled (Reset) 01 : Header Only 10 : Header + 16 User entries 11 : Header + 32 User entries
RXSTAT:	Receive User Statistics	0 : Disabled 1 : Enabled
TXSTAT:	Transmit User Statistics	0 : Disabled 1 : Enabled
MASK1,0:	VP/VC Filter Mask	00 : Mask Disabled 01 : Filter MASK enabled 10 : Invalid 11 : Filter $\overline{\text{MASK}}$ enabled
TESTMODE:	Internal Testmode – User should set to zero	0 : Disabled 1 : Enabled
TIME3–0:	Statistics DMA transfer timeout (see note1 below)	
TIMERENB :	Timer Enable (DMA)	0 : Disabled 1 : Enabled
CNTOVF:	Count Overflow Enable (DMA)	0 : Disabled 1 : Enabled
TBLOVF	Table Overflow Enable (DMA)	0: Disabled 1: Enable
FDMA:	Force DMA transfer (see note2 below)	0 : DMA based on other events above 1 : Force DMA

Note1:

The TIME3–0 bits are used to provide a programmable timeout for the statistics data (NSR) to be sent to memory via DMA, for the situation where no other event has caused this to happen, ie no counter has reached its maximum value, or the table is not yet full.

The relationship is : Timeout Event = $2^{(26-\text{TIMEOUT})}$ x clock period

Note2:

The FDMA bit will be automatically cleared whilst the DMA operation is being performed. This bit is not readable. A 0 bit will be returned in this bit position when this register is read.

Control Register 52 – Statistics VP Filter XMASK

D15							
				VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0
VPI7	VPI6	VPI5	VPI4	VPI3	VPI2	VPI1	VPI0
							D0

Control Register 53 – Statistics VC Filter XMASK

D15							
VCI15	VCI14	VCI13	VCI12	VCI11	VCI10	VCI9	VCI8
VCI7	VCI6	VCI5	VCI4	VCI3	VCI2	VCI1	VCI0
							D0

Control Register 54 – Statistics VP Filter SMASK

D15							
				VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0
VPI7	VPI6	VPI5	VPI4	VPI3	VPI2	VPI1	VPI0
							D0

Control Register 55 – Statistics VC Filter SMASK

D15							
VCI15	VCI14	VCI13	VCI12	VCI11	VCI10	VCI9	VCI8
VCI7	VCI6	VCI5	VCI4	VCI3	VCI2	VCI1	VCI0
							D0

These registers are used for filtering the user statistics prior to being recorded into the NSR. The filter operation may work on cells which pass or fail the filter, or may be disabled. The relevant mode is controlled from CR51.
The filter works on both TX and RX paths. This filtering operation does not effect the total cells received/transmitted counts.

Any of the 28 VPI/VCI bits of the cell header may be defined as X, 0, or 1.

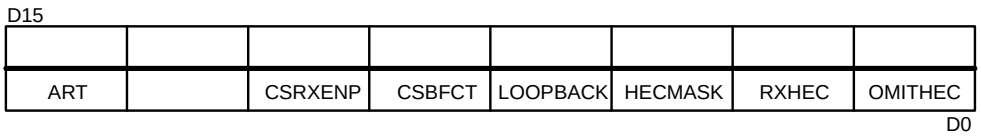
The XMASK is used to define X states for each bit.
When set to 1, they represent an X for that bit.
When set to 0, the filter will take the state defined in the SMASK.

Control Register 56 – Cell Stream Interface Control #1

D15							D0
TXPLT1	TXPLT0	TXCLP1	TXCLP0	TXATE	TXATC	TAG1	TAG0
RXPLT1	RXPLT0	RXCLP1	RXCLP0	RXATE	RXATC	CSTENB	CSRENB

CSRENB:	Rx Cell Stream Interface	0 : Disabled (Reset) 1 : Enabled (Not Reset)
CSTENB:	Tx Cell Stream Interface	0 : Disabled (Reset) 1 : Enabled (Not Reset)
RXATC: **TXATC**:	ATC Interface	0 : ATC not present 1 : ATC present
RXATE: **TXATE**:	Address translation error action	0 : discard cells with ATE 1 : forward cells with ATE
RXCLP1,0: **TXCLP1,0**:	CLP bit option	00 : old header value 01 : from address translation 10 : force to 0 11 : force to 1
RXPLT1,0: **TXPLT1,0**:	PLT congestion bit option	00 : old header value 01 : from address translation 10 : force to 0 11 : force to 1
TAG1,0:	Routing Tag Size	00 : 0 bytes 01 : 1 bytes 10 : 2 bytes 11 : 3 bytes

Control Register 57 – Cell Stream Interface Control #2



OMITHEC:	Omit HEC byte on transmit (Receive path)	0 : 53 byte cell transmission 1 : 52 byte cell transmission
RXHEC:	HEC Generation (Receive path)	0 : Disabled 1 : Enabled
HECMASK :	HEC Mask (55h = 01010101b) (Receive path)	0 : Disabled 1 : Enabled
LOOPBACK:	CSI Rx/Tx Loopback	0 : Disabled 1 : Enabled
CSBFCT:	Timing of Backward Flow Control in CS Mode	0 : Next cycle 1 : Current cycle
CSRXENP:	Polarity of RXEN in CS Mode	0 : RXEN Active high 1 : RXEN Active low
ART:	Timing of ATRFDO, ARRFDO	0 : Normal 1 : Advanced by ½ clock

The RXHEC and HECMASK bits would normally be enabled. These are required to regenerate the HEC byte and corresponding mask after either an address translation in the receive path, or after a cell has been inserted into the receive path via the cell insert function.

If the HEC is not recalculated, then byte 5 of the header will contain FFh.

Clearly, if the cell stream is configured as 52 bytes (ie OMITHEC is set), then the RXHEC and HECMASK bits are redundant.

The CSBFCT and CSRXENP bits allow direct connection to the ALC (MB86686A/7) device(s).

Control Register 58 – Interrupt Enable

D15							D0
				BERR	SOFTX	SOVRX	SOFRX
GOS	BUFFOVF	ICD	OCD	LOP	LOF	LOS	DMA

DMA :	DMA Channel 0–5 Interrupt	0 : Interrupt masked 1 : Interrupt enabled
LOS:	Loss Of Signal	0 : Interrupt masked 1 : Interrupt enabled
LOF:	Loss Of Frame	0 : Interrupt masked 1 : Interrupt enabled
LOP:	Loss Of Pointer (STM–1)	0 : Interrupt masked 1 : Interrupt enabled
OCD:	Out of Cell Delineation	0 : Interrupt masked 1 : Interrupt enabled
ICD:	Into Cell Delineation	0 : Interrupt masked 1 : Interrupt enabled
GOS:	Gain of Signal	0 : Interrupt masked 1 : Interrupt enabled
BUFFOVF:	Internal Buffer Overflow	0 : Interrupt masked 1 : Interrupt enabled
SOFRX:	Start Of Frame (Receive)	0 : Interrupt masked 1 : Interrupt enabled
SOVRX:	Start Of VC–4 (Receive)	0 : Interrupt masked 1 : Interrupt enabled
SOFTX:	Start Of Frame (Transmit)	0 : Interrupt masked 1 : Interrupt enabled
BERR:	Bus Error	0 : Interrupt masked 1 : Interrupt enabled

Control Register 59 – Interrupt Under Service

D15

				BERR	SOFTX	SOVRX	SOFRX
GOS	BUFFOVF	ICD	OCD	LOP	LOF	LOS	DMA

D0

These bits are set by the processor to indicate that the associated exception condition is being dealt with. This has two effects :

1. It will clear the associated interrupt request, and
2. Will inhibit any further interrupt requests of the associated type from being generated.

The associated bits should be set back to zero in order to enable further interrupts to be generated. The interrupt sources are identical to those shown in the Interrupt Enable Register.

Control Register 60 – DMA Descriptor Pointer Table Low

D15

AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9
AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1

D0

Data written into this register form the least significant 16 bits of the DMA descriptor location table.

Control Register 61 – DMA Descriptor Pointer Table High

D15

	AD23	AD22	AD21	AD20	AD19	AD18	AD17

D0

Data written into this register form the most significant 7 bits of the DMA descriptor location table.

Note:

The 23 bit value written into these registers represents the byte address of the Descriptor Pointer Location Table.
(Divided by 2 for 16–bit mode).
(Divided by 4 for 32–bit mode).

Eg. If the table resides at 1EF042 (hex), then these registers should be loaded with the following values:

16–bit mode :	CR60 = 7821 (hex) CR61 = 000F (hex)
32–bit mode :	CR60 = BC10 (hex) CR61 = 0007 (hex)

Control Register 62 – DMA Channel Activity

D15							D0
		CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0

CHAN5–0: DMA Channel Enable
0 : Disabled
1 : Enabled

Channels are:
CHAN5 : CTX insert
CHAN4 : CTX extract
CHAN3 : CRX insert
CHAN2 : CRX extract
CHAN1 : SSR
CHAN0 : NSR

Control Register 63 – DMA Mode

D15							D0
TESTMODE				FTM	PRS	DMAS	DMAENB

DMAENB: DMA Controller Enable
0 : Disabled (Reset)
1 : Enabled (Not Reset)

DMAS: DMA Stop
0 : DMA not stopped
1 : DMA stopped

PRS: Priority Select
0 : Channel 0 has priority
1 : Channel 5 has priority

FTM: Fast Transfer Mode
0 : Descriptor DMA cycle dependent on $\overline{\text{READY}}$/$\overline{\text{DTACK}}$ input
1 : Fast DMA cycle for descriptor transfer

TESTMODE: Internal Testmode (User should set to zero)
0 : Disabled
1 : Enabled

B.2 Status Registers

Status Registers 0 – 1 Are Not Used

Status Registers 2 – 17 (see below)

Status registers 2 to 17 provide access to 32 frame overhead bytes. These are illustrated in the table below for the various modes of operation.

STATUS REG		TRANSMIT FRAMER OVERHEAD ACCESS BYTES					
REG NO.	REG ADDR	SDH/SONET		E3		DS3 (PCLP)	
		D15 – D8	D7 – D0	D15 – D8	D7 – D0	D15 – D8	D7 – D0
2	04h	C1	R1	TR	NR	0	see note
3	06h	R2	R1	UC			
4	08h	F1	R3				
5	0Ah	R4	D1				
6	0Ch	D2	D3				
7	0Eh	K1	D4				
8	10h	D5	D6				
9	12h	D7	D8				
10	14h	D9	D10				
11	16h	D11	D12				
12	18h	Z1A	Z1B				
13	1Ah	Z1C	E2				
14	1Ch	R5	R6				
15	1Eh	J1	C2			Z6	Z5
16	20h	F2	Z3			Z4	Z3
17	22h	Z4	Z5			Z2	Z1

Table 4 – Status Registers Overhead Byte Access

Note: D7 – D5 = 0
D4 – D0 = Five of the C–bits

D4 = C1 (AIC)
D3 = C3 (FEAC)
D2 = C13 (DL)
D1 = C14 (DL)
D0 = C15 (DL)

Status Registers 18 – 56 Are Not Used

Status Register 57 – CSI Receive / Transmit Buffer Fill Levels

D15

RXBUFF3	RXBUFF2	RXBUFF1	RXBUFF0	TXBUFF3	TXBUFF2	TXBUFF1	TXBUFF0
0	0	0	0	0	X	X	X

D0

This register shows the fill levels of both CSI cell buffers.
The count will be in cells (0–9).

The X bits will contain the settings of the control bits as set in CR57.

Status Register 58 – Interrupt Status Register

D15

0	0	0	0	BERR	SOFTX	SOVRX	SOFRX
GOS	BUFFOVF	ICD	OCD	LOP	LOF	LOS	DMA

D0

This register shows the source of the interrupt. The bits are identical to CR58.

Status Register 59 – Physical Layer Alarms Received

D15

PJUST	NJUST	NDF	0	0	B3ERR	P–FERF	P–AIS
LOS	LOF	LOP	OCD	B2ERR	B1ERR	MS–FERF	MS–AIS

D0

	DS–3	**SONET / SDH**	**E3**
MS–FERF	X–bits = 0	K2 (6–8) = 110	MA (bit 1) = 1
MS–AIS	Info = 1010... C–bits = 0 X–bits = 1	K2 (6–8) = 111	Unframed 1’s
P–FERF	G1 (bit 5) = 1	G1 (bit 5) = 1	
P–AIS		pointer = all 1’s	
B1ERR		received B1 byte ≠ calculated BIP	
B2ERR	received CP bits ≠ calculated BIP	received B2 byte ≠ calculated BIP	received EM byte ≠ calculated BIP
B3ERR	received B1 byte ≠ calculated BIP	received B3 byte ≠ calculated BIP	

Note1:
For DS–3 mode, the PLCP (if enabled) carries the path alarms, whereas the DS–3 frame carries the section alarms.

Note 2:
B1ERR, B2ERR, and B3ERR are set on receiving a B1/B2/B3 BIP count that disagrees with the calculated BIP. A corresponding FEBE will be transmitted back via the transmit framer, if the FEBE function is enabled in CR34.

Note 3:
PJUST = positive justification event for SDH/SONET pointer
NJUST= negative justification event for SDH/SONET pointer
NDF = New Data Flag event for SDH/SONET pointer

Status Register 60 – Not Used

Status Register 61 – Internal Buffer Overflow Interrupt Indication

D15

0	0	0	0	0	0	1	1
0	0	STATS	RXEXT	TXEXT	SSHBUFF	RXFIFO	TXFIFO

D0

This register shows which buffer generated the BUFFOVF interrupt.

TXFIFO: CSI transmit buffer overflowed, cell discarded

RXFIFO: CSI receive buffer overflowed, cell discarded

SSHBUFF: switch statistics buffer overflowed, switch statistics record discarded

TXEXT: cell transmitter extract buffer overflowed, cell discarded

RXEXT: cell receiver extract buffer overflowed, cell discarded

STATS: NSR RAM not available, network statistics information lost

Status Register 62 – DMA Channel Activity

D15

0	0	0	0	0	0	0	0
0	0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0

D0

This register shows which DMA channels are currently active

Channels are :
CHAN5 : CTX insert
CHAN4 : CTX extract
CHAN3 : CRX insert
CHAN2 : CRX extract
CHAN1 : SSR
CHAN0 : NSR

Status Register 63 – BERR / DMA Interrupt Indication

D15

0	0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0
0	0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0

D0

This register shows which DMA channel generated either the DMA interrupt or which channel was currently active when the BERR interrupt was generated.

D13 – D8 : DMA Channel due to BERR interrupt

D5 – D0 : DMA Channel due to DIE descriptor bit being set

C. RATINGS

C.1 Absolute Maximum Ratings

Rating	Symbol	Values		Unit
		Min	Max	
Positive Supply Voltage	$+V_{DD}$	4.5	5.5	V
Input Voltage	V_{DIN}	–0.5	$+V_{DD}$+0.5	V
Output Voltage	V_{O1}	–0.5	$+V_{DD}$+0.5	V
Input Current	I_{MAX}	–10.0	10.0	μA
Storage Temperature	T_{STG}	–40	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Rating**s are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

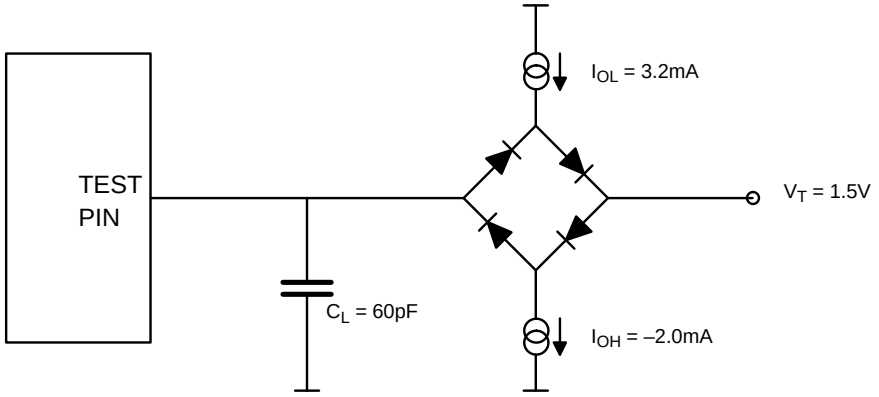
C.2 DC Characteristics

Parameter	Symbol	Pin	Test Condition	Value			Unit
				Min.	Typ.	Max.	
Positive Supply Voltage	V_{DD}		+4.75 V	+4.75	+5.0	+5.25	V
Positive Supply Current	$+I_{VS}$		Static no load	–	–	100	μA
Input High Voltage (TTL)	V_{IH}			2.2	–	$+V_{DD}$	V
Input Low Voltage (TTL)	V_{IL}			0	–	0.8	V
Input Leakage Current	I_L		$0 \leqq V_I \leqq +V_{DD}$	–10	–	10	μA
Output Low Voltage	V_{OL}		I_{OL}=3.2mA	V_{SS}	–	0.4	V
Output High Voltage	V_{OH}		I_{OH}=–2mA	4.2	–	V_{DD}	V
Output Off Leakage Current	I_{LO}			–10	–	10	μA
Input Pin Capacitance	C_{in}			–	–	8	pF
Output Pin Capacitance	C_{out}			–	–	16	pF
I/O Pin Capacitance	$C_{i/o}$			–	–	21	pF
Power Dissipation (operating)	P_O				700		mW
Operating Temperature	T_A			0		+70	°C

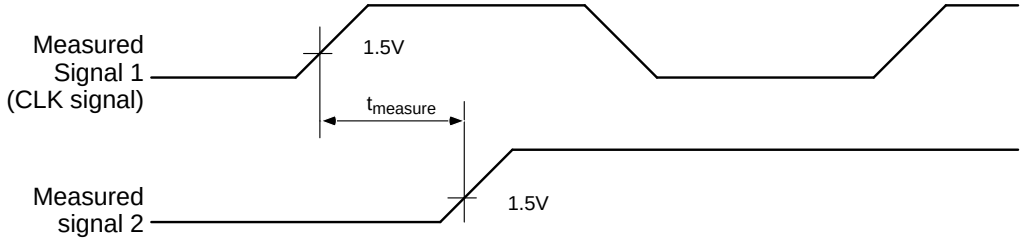
D. AC CHARACTERISTICS

The timing parameters listed in this appendix were measured under the following conditions.
Unless otherwise stated, V_{IL} = 0.0V, V_{IH} = 4.0V.

General Load Circuit :



Timing Measurements (input setup/hold, output delay) :



Timing Measurements (high–Z) :

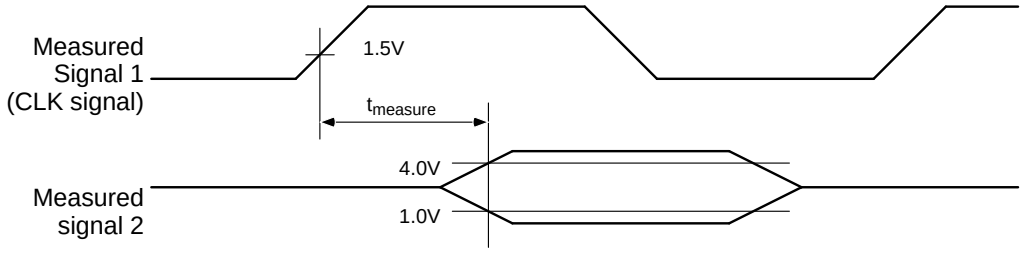


Fig. 61 – AC Timing Test Conditions

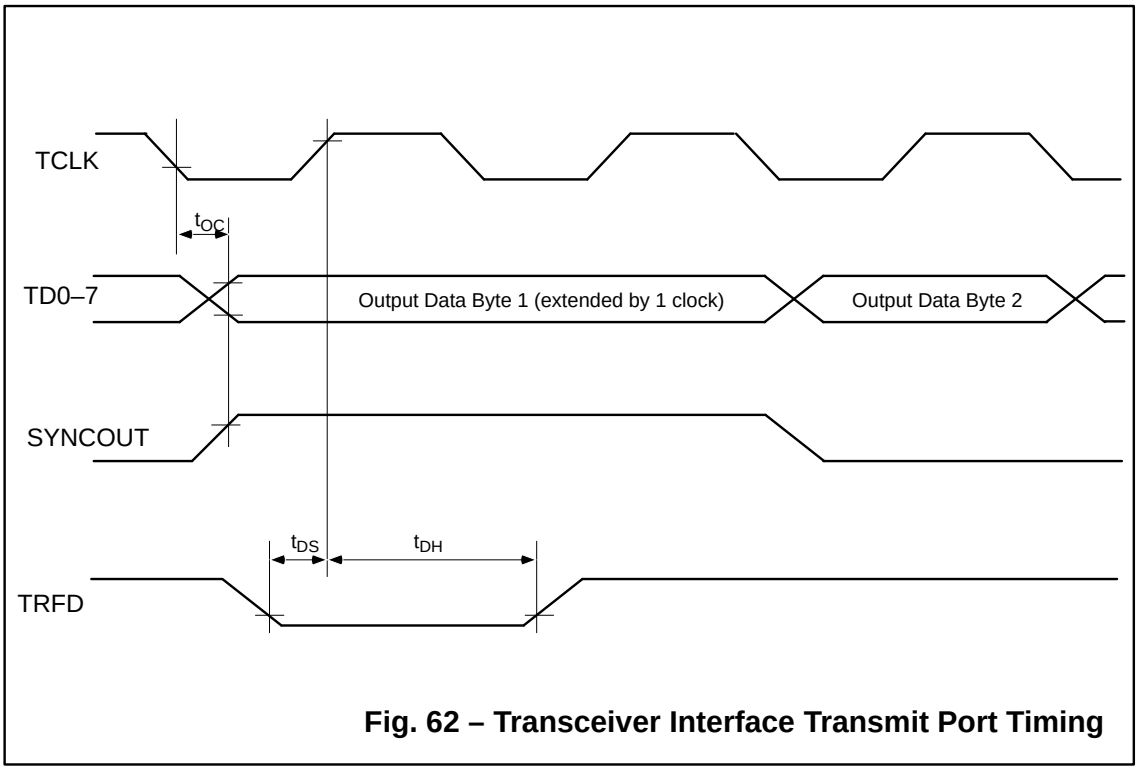


Fig. 62 – Transceiver Interface Transmit Port Timing

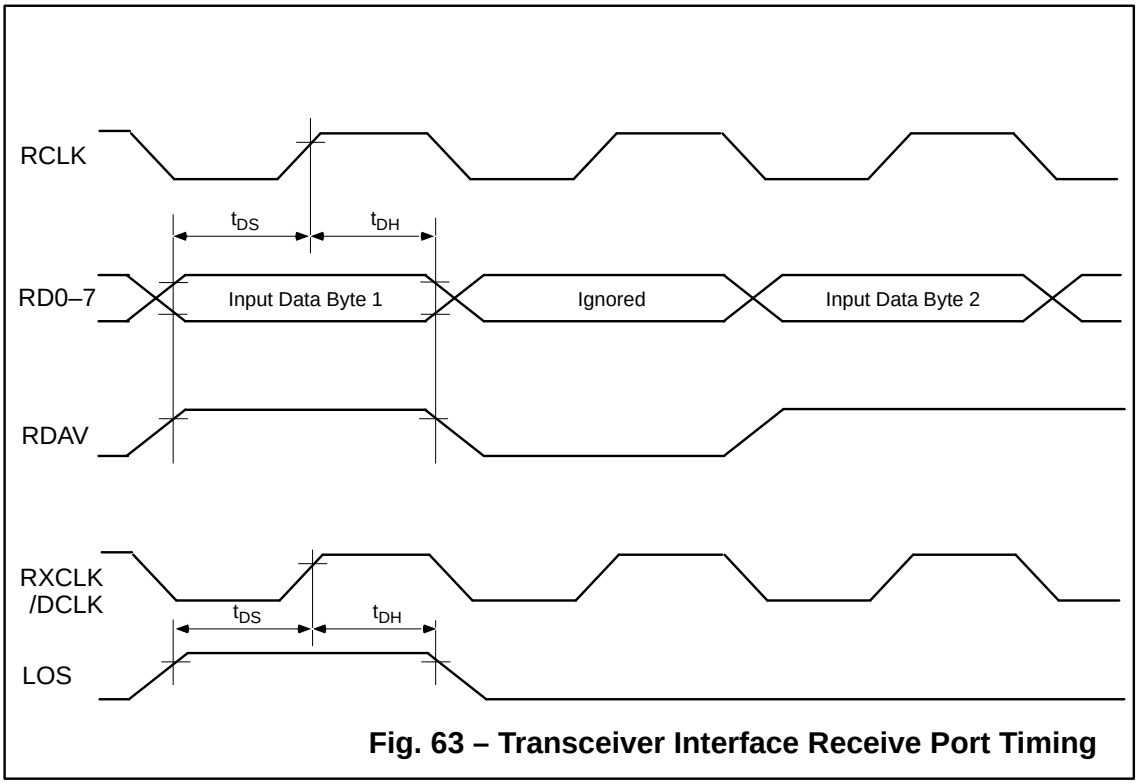


Fig. 63 – Transceiver Interface Receive Port Timing

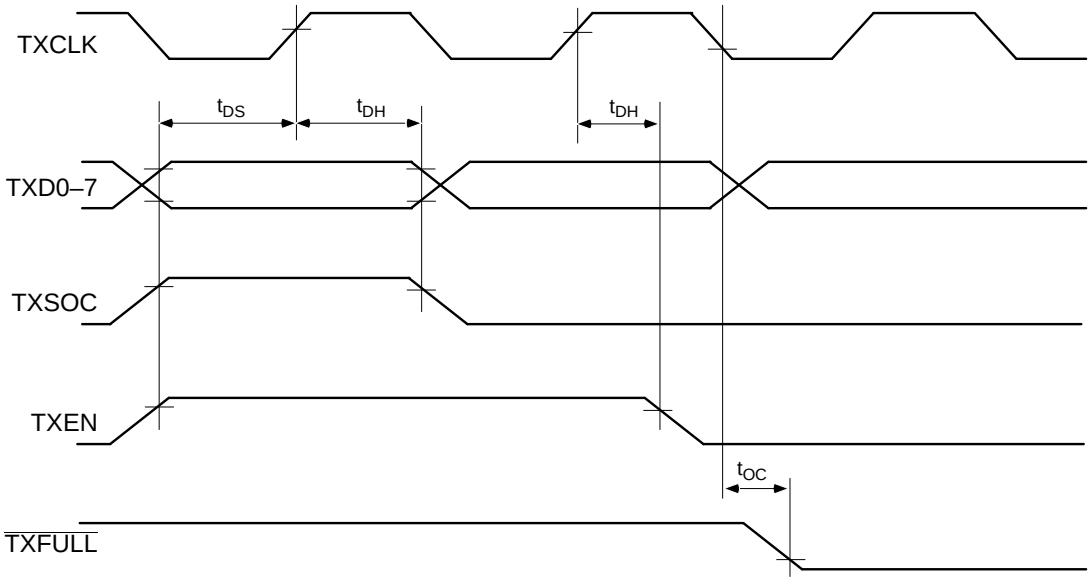


Fig. 64 – Cell Stream Interface Transmit Port (Fujitsu mode) Timing

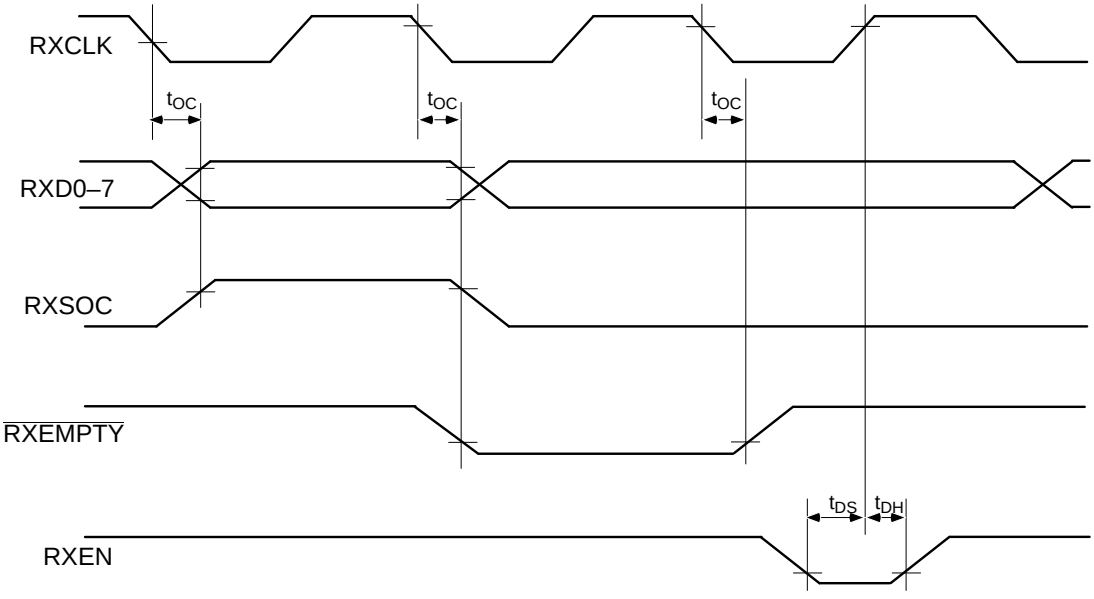


Fig. 65 – Cell Stream Interface Receive Port (Fujitsu mode) Timing

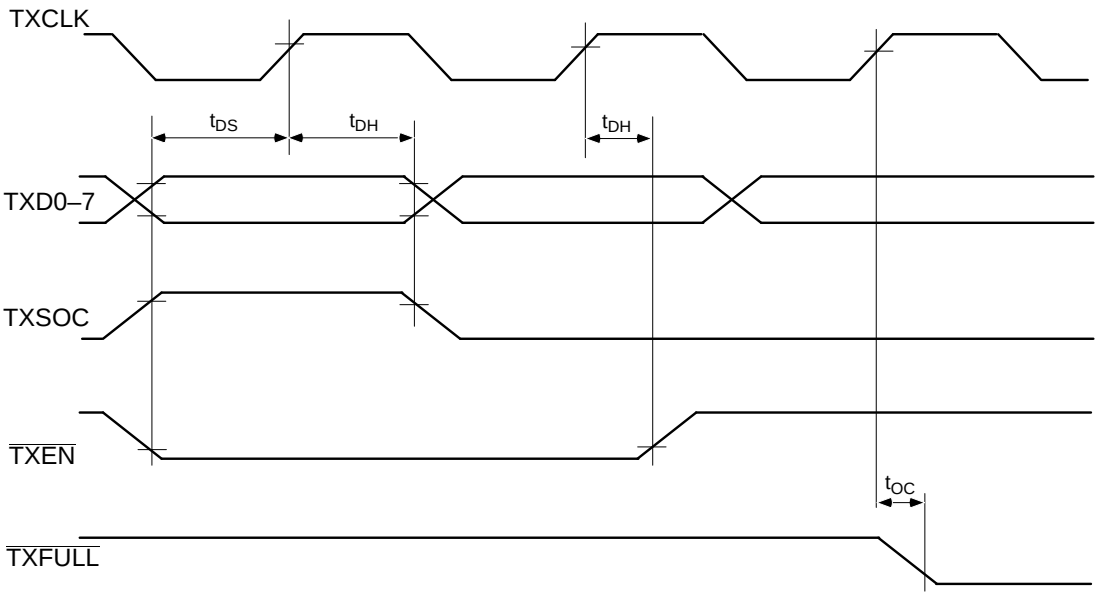


Fig. 66 – Cell Stream Interface Transmit Port (Utopia mode) Timing

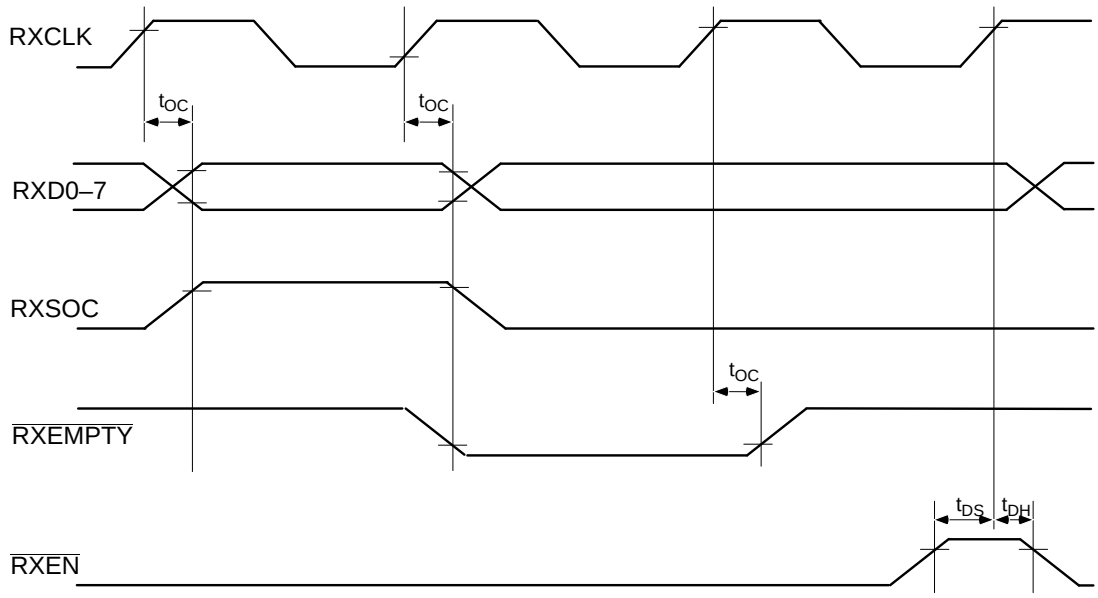


Fig. 67 – Cell Stream Interface Receive Port (Utopia mode) Timing

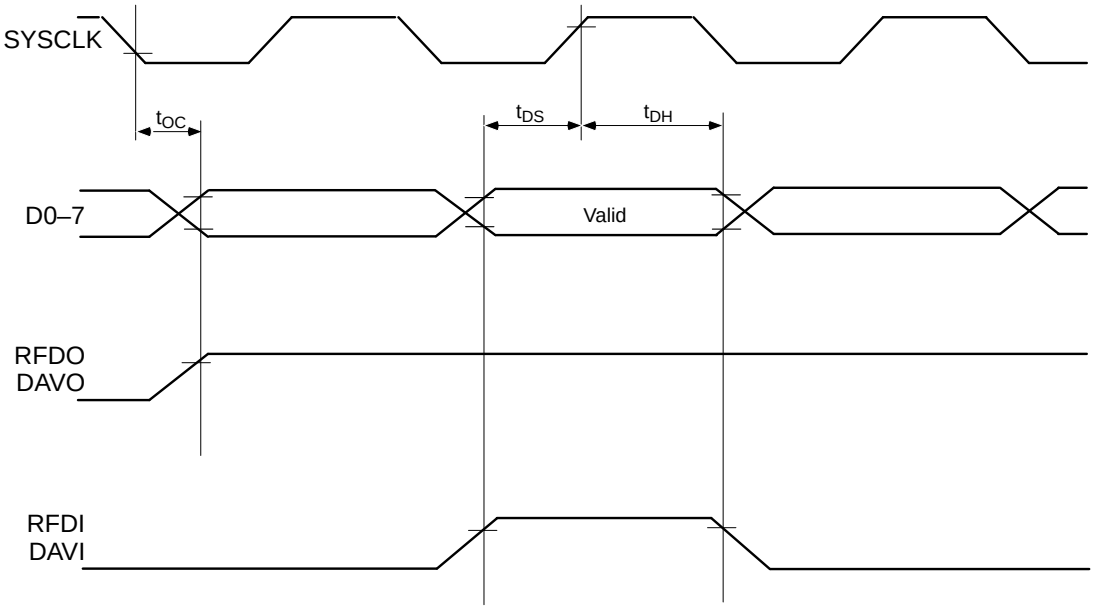


Fig. 68 – ATC Interface Port Timing

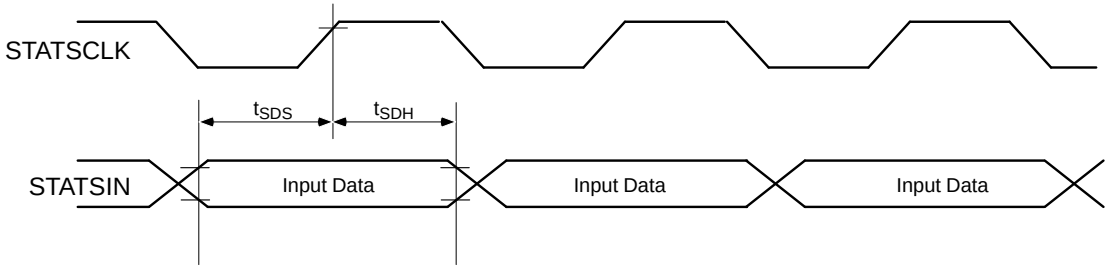


Fig. 69 – Switch Statistics Interface Port Timing

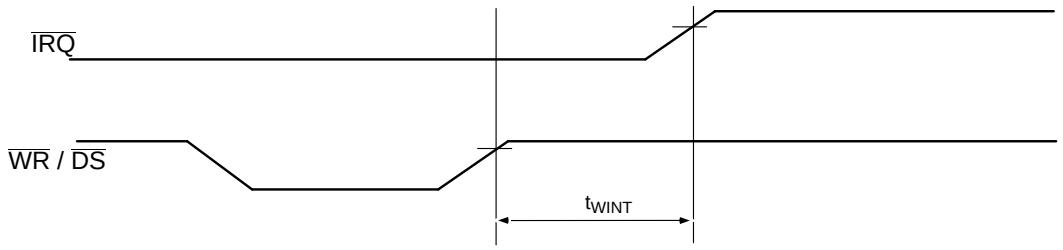


Fig. 70 – Interrupt Timing

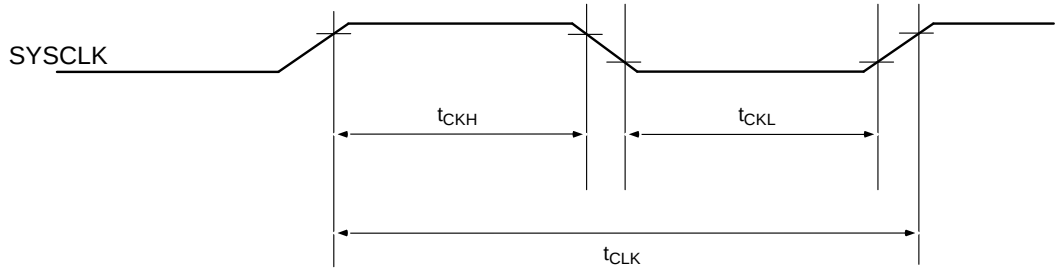


Fig. 71 – System Clock Timing

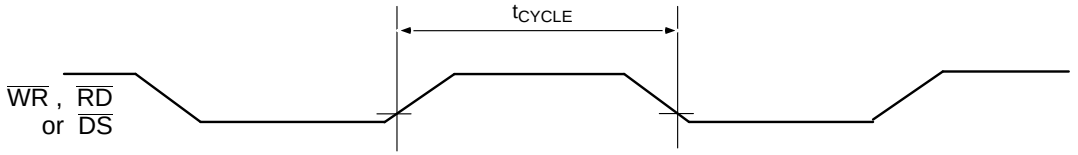


Fig. 72 – Register Access Cycle to Cycle Timing

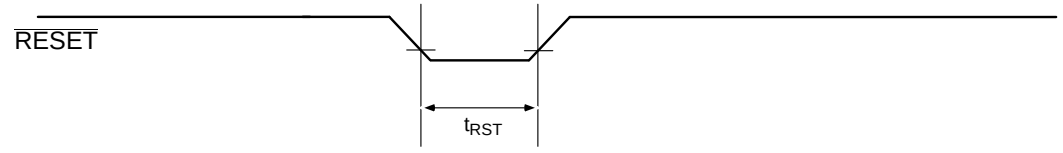


Fig. 73 – Reset Timing

Parameter	Ref Signal	Abrev	Values			Units (ns)
			Min	Typical	Max	
Input Data Setup Time	RCLK,RXCLK, TCLK,TXCLK	t_{DS}				ns
Input Data Hold Time	RCLK,RXCLK, TCLK,TXCLK	t_{DH}				ns
Data Out Delay	RCLK,RXCLK, TCLK,TXCLK	t_{OC}				ns
Statistics Data setup Time	STATSCLK	t_{SDS}				ns
Statistics Data Hold Time	STATSCLK	t_{SDH}				ns
Reset Pulse width	$\overline{RESET}$	t_{RST}				ns

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 5 – External Interfaces 1 – AC Timing

Parameter	Ref Signal	Abrev	Values			Units (ns)
			Min	Typical	Max	
Clock High Time	RXCLK	t_{CKH}				ns
Clock Low Time	RXCLK	t_{CKL}				ns
Clock Period	RXCLK	t_{CLK}				ns
Cycle Recovery Time using Ready_Out	$\overline{WR}$, $\overline{RD}$ & $\overline{DS}$	t_{CYCLE}				ns
Cycle Recovery Time ignoring Ready_Out	$\overline{WR}$, $\overline{RD}$ & $\overline{DS}$	t_{CYCLE}				ns
$\overline{WR}$ to $\overline{IRQ}$ Inactive	$\overline{WR}$, $\overline{DS}$	t_{WINT}				ns

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 6 – External Interfaces 2 – AC Timing

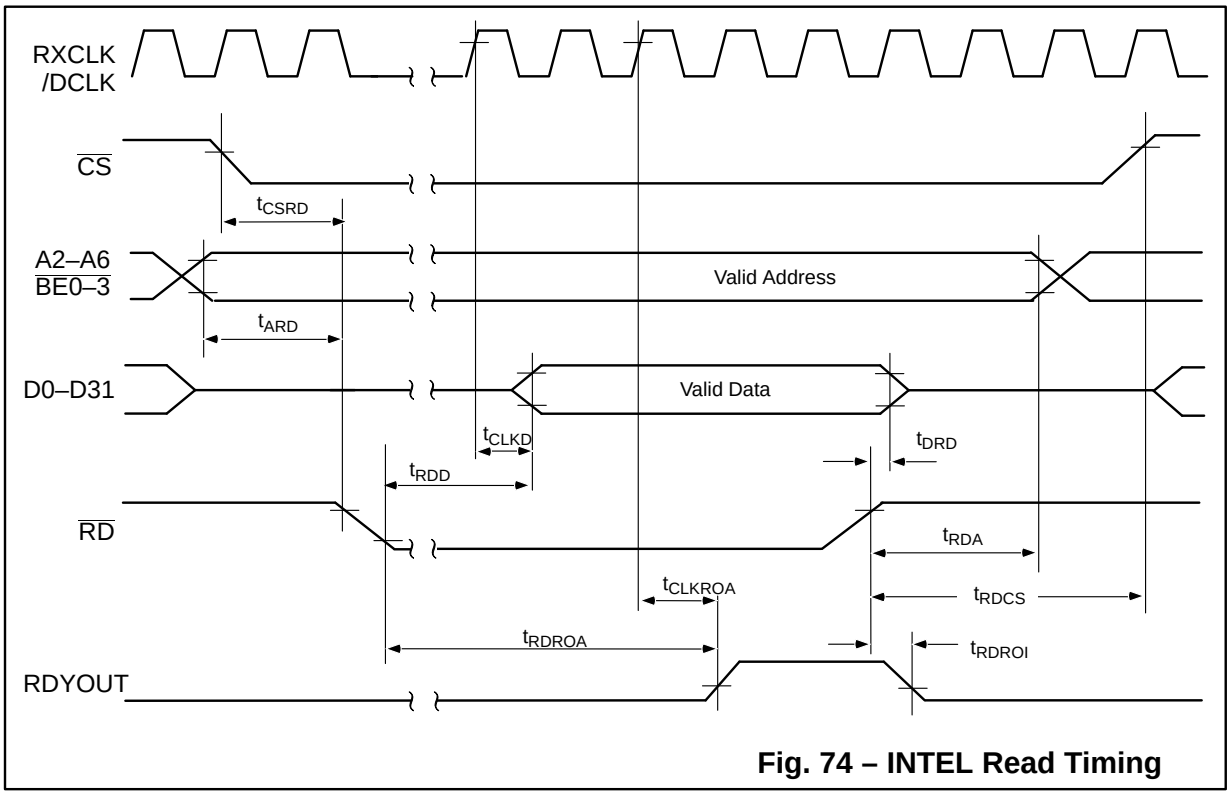


Fig. 74 – INTEL Read Timing

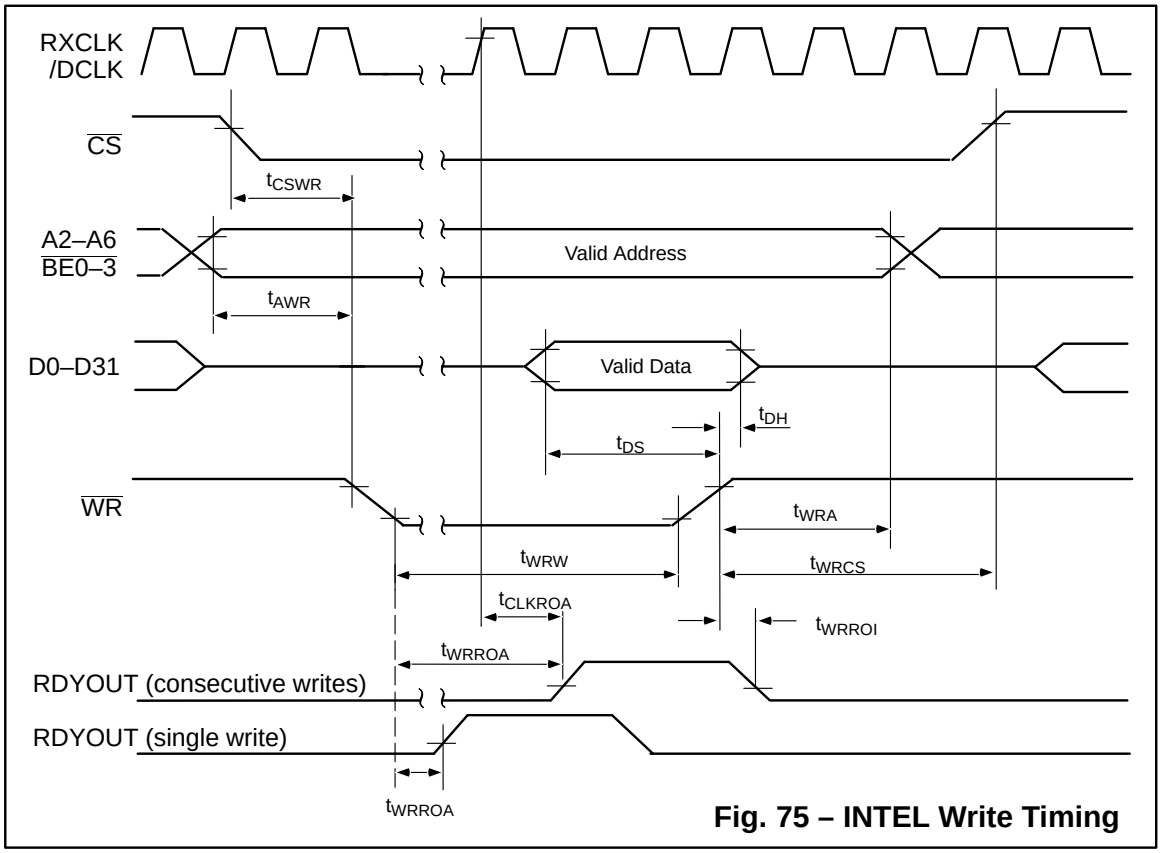


Fig. 75 – INTEL Write Timing

Parameter	Ref Signal	Abrev	Values			Units (ns)
			Min	Typical	Max	
$\overline{CS}$ Active to $\overline{RD}$ Active	$\overline{RD}$	t_{CSRD}	0	0	0	ns
Address Valid to $\overline{RD}$ Active	$\overline{RD}$	t_{ARD}				ns
Data Valid Delay Time	DCLK/ RXCLK	t_{CLKD}				ns
$\overline{RD}$ Active to Valid data	$\overline{RD}$	t_{RDD}			$3(t_{CLK})+t_{CLKD}$ or $5(t_{CLK})+t_{CLKD}$	ns see note 1
RDYOUT Active Delay Time	DCLK/ RXCLK	t_{CLKROA}			$5(t_{CLK})+t_{CLKROA}$ or $7(t_{CLK})+t_{CLKROA}$	ns see note 2
$\overline{RD}$ Active to RDYOUT Active	$\overline{RD}$	t_{RDROA}				ns
$\overline{RD}$ Inactive to Invalid Data	$\overline{RD}$	t_{DRD}				ns
$\overline{RD}$ Inactive to RDYOUT Inactive	$\overline{RD}$	t_{RDROI}				ns
$\overline{RD}$ Inactive to Invalid Address	$\overline{RD}$	t_{RDA}	0	0	0	ns
$\overline{RD}$ Inactive to $\overline{CS}$ Inactive	$\overline{RD}$	t_{RDCS}	0	0	0	ns
$\overline{CS}$ Active to $\overline{WR}$ Active	$\overline{WR}$	t_{CSWR}	0	0	0	ns
Address Valid to $\overline{WR}$ Active	$\overline{WR}$	t_{AWR}				ns
$\overline{WR}$ Pulse Width	$\overline{WR}$	t_{WRW}				ns
$\overline{WR}$ Active to RDYOUT Active (single writes)	$\overline{WR}$	t_{WRROA}				ns
$\overline{WR}$ Active to RDYOUT Active (consecutive writes)	$\overline{WR}$	t_{WRROA}			$5(t_{CLK})+t_{CLKROA}$ or $7(t_{CLK})+t_{CLKROA}$	ns see note 2
Data Setup Time	$\overline{WR}$	t_{DS}				ns
Data Hold Time	$\overline{WR}$	t_{DH}				ns
$\overline{WR}$ Inactive to RDYOUT Inactive	$\overline{WR}$	t_{WRROI}				ns
$\overline{WR}$ Inactive to Invalid Address	$\overline{WR}$	t_{WRA}	0	0	0	ns
$\overline{WR}$ Inactive to $\overline{CS}$ Inactive	$\overline{WR}$	t_{WRCS}	0	0	0	ns

Notes: 1 $3t_{CLK}$ if in 16 bit mode; $5t_{CLK}$ if in 32 bit mode
2 $5t_{CLK}$ if in 16 bit mode; $7t_{CLK}$ if in 32 bit mode

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 7 – Microprocessor Interface –INTEL AC Timing

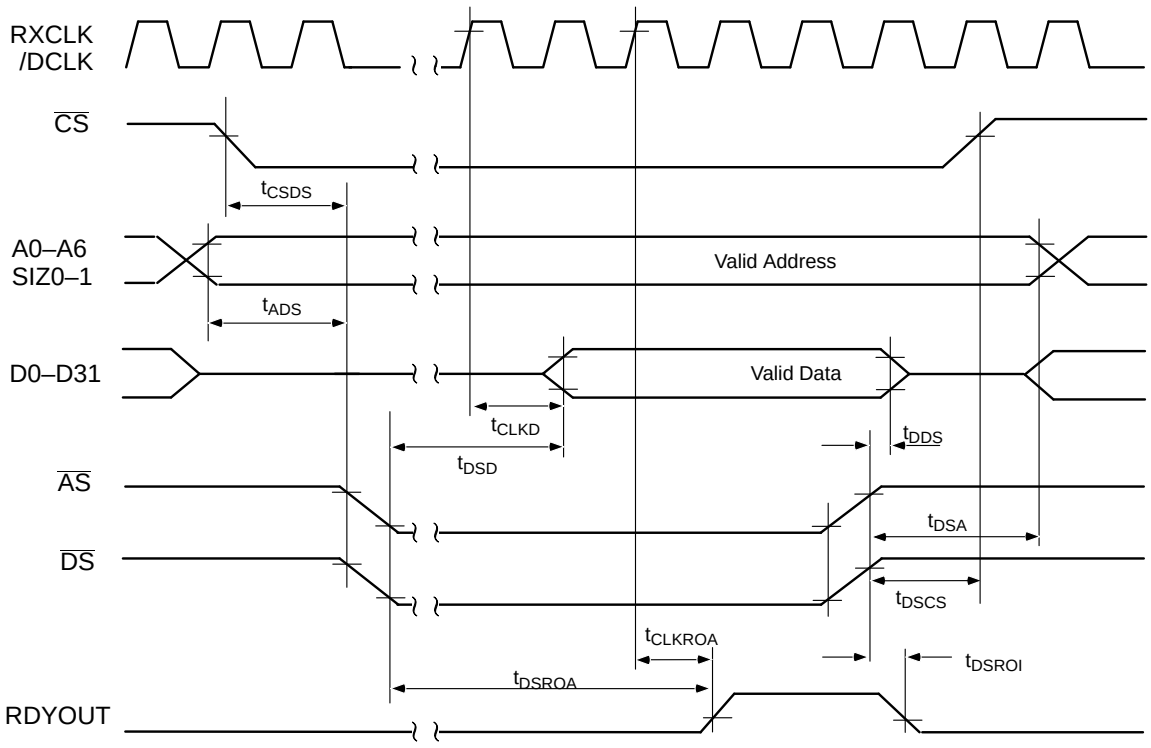


Fig. 76 – MOTOROLA Read Timing

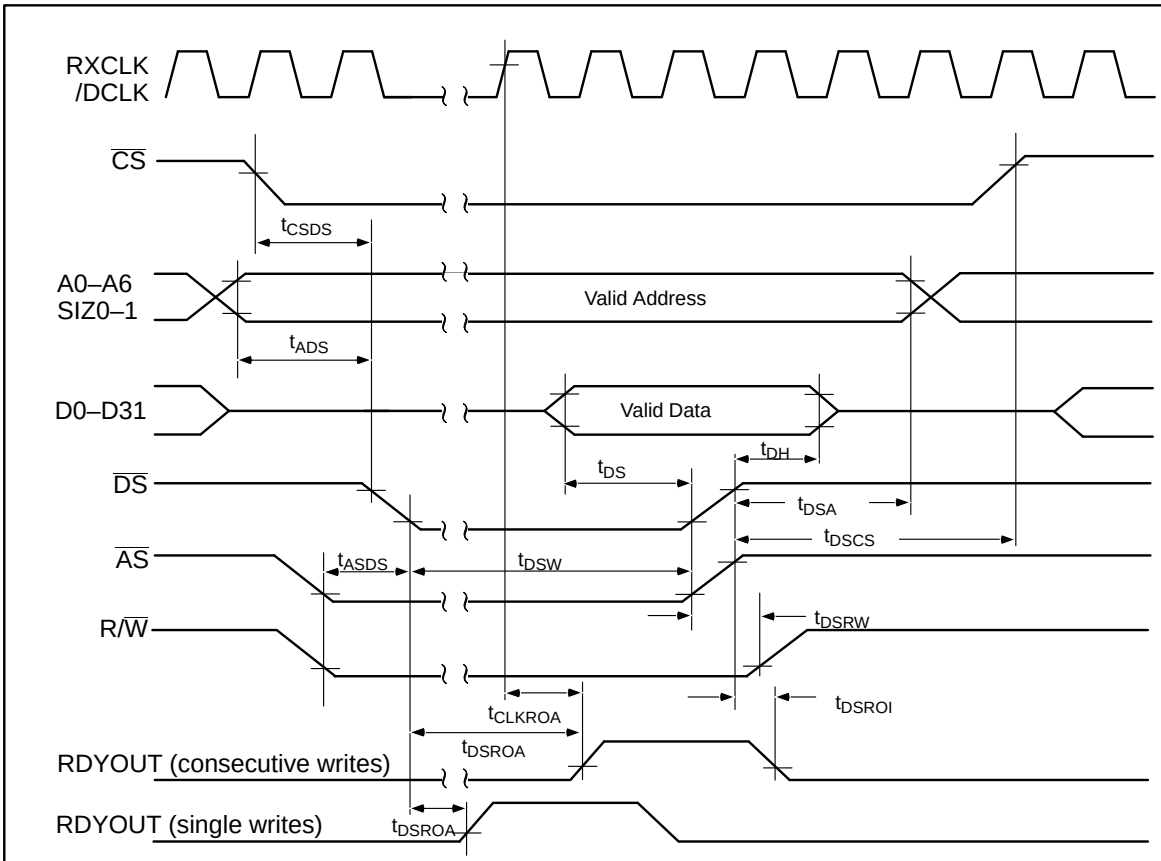


Fig. 77 – MOTOROLA Write Timing

Parameter	Ref Signal	Abrev	Values			Units (ns)
			Min	Typi-cal	Max	
$\overline{CS}$ Active to $\overline{DS}$ Active (Read)	$\overline{DS}$	t_{CSDS}	0	0	0	ns
Address Valid to $\overline{DS}$ Active (Read)	$\overline{DS}$	t_{ADS}				ns
Data Valid Delay Time	DCLK/ RXCLK	t_{CLKD}				ns
$\overline{DS}$ Active to Valid Data (Read)	$\overline{DS}$	t_{DSD}			$3t_{CLK}+t_{CLKD}$ or $5t_{CLK}+t_{CLKD}$	ns see note 1
RDYOUT Active Delay Time	DCLK/ RXCLK	t_{CLKROA}				ns
$\overline{DS}$ Active to RDYOUT Active (Read)	$\overline{DS}$	t_{DSROA}			$5t_{CLK}+t_{CLKROA}$ or $7t_{CLK}+t_{CLKROA}$	ns see note 2
$\overline{DS}$ Inactive to Invalid Data	$\overline{DS}$	t_{DDS}				ns
$\overline{DS}$ Inactive to Invalid Address (Read)	$\overline{DS}$	t_{DSA}	0	0	0	ns
$\overline{DS}$ Inactive to RDYOUT Inactive (Read)	$\overline{DS}$	t_{DSROI}				ns
$\overline{DS}$ Inactive to $\overline{CS}$ Active (Read)	$\overline{DS}$	t_{DSCS}	0	0	0	ns
$\overline{CS}$ Active to $\overline{DS}$ Active (Write)	$\overline{DS}$	t_{CSDS}	0	0	0	ns
Address Valid to $\overline{DS}$ Active (Write)	$\overline{DS}$	t_{ADS}				ns
$\overline{AS}$ and R/$\overline{W}$ Active to $\overline{DS}$ Active	$\overline{AS}$/ R/$\overline{W}$	t_{ASDS}	0	0	0	ns
$\overline{DS}$ Pulse Width (write)	$\overline{DS}$	t_{DSW}				ns
$\overline{DS}$ Active to RDYOUT Active (single write)	$\overline{DS}$	t_{DSROA}				ns
$\overline{DS}$ Active to RDYOUT Active (Consecutive writes)	$\overline{DS}$	t_{DSROA}			$5t_{CLK}+t_{CLKROA}$ or $7t_{CLK}+t_{CLKROA}$	ns see note 2
Data Setup Time (Write)	$\overline{DS}$	t_{DS}				ns
Data Hold Time (Write)	$\overline{DS}$	t_{DH}				ns
$\overline{DS}$ Inactive to Invalid Address (Write)	$\overline{DS}$	t_{DSA}	0	0	0	ns
$\overline{DS}$ Inactive to $\overline{CS}$ Inactive (Write)	$\overline{DS}$	t_{DSCS}	0	0	0	ns
$\overline{DS}$ Inactive to R/$\overline{W}$ Inactive (Write)	$\overline{DS}$	t_{DSRW}	0	0	0	ns
$\overline{DS}$ Inactive to RDYOUT Inactive (write)	$\overline{DS}$	t_{DSROI}				ns

Notes: 1 $3t_{CLK}$ if in 16 bit mode; $5t_{CLK}$ if in 32 bit mode
2 $5t_{CLK}$ if in 16 bit mode; $7t_{CLK}$ if in 32 bit mode

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 8 – Microprocessor Interface – MOTOROLA AC Timing

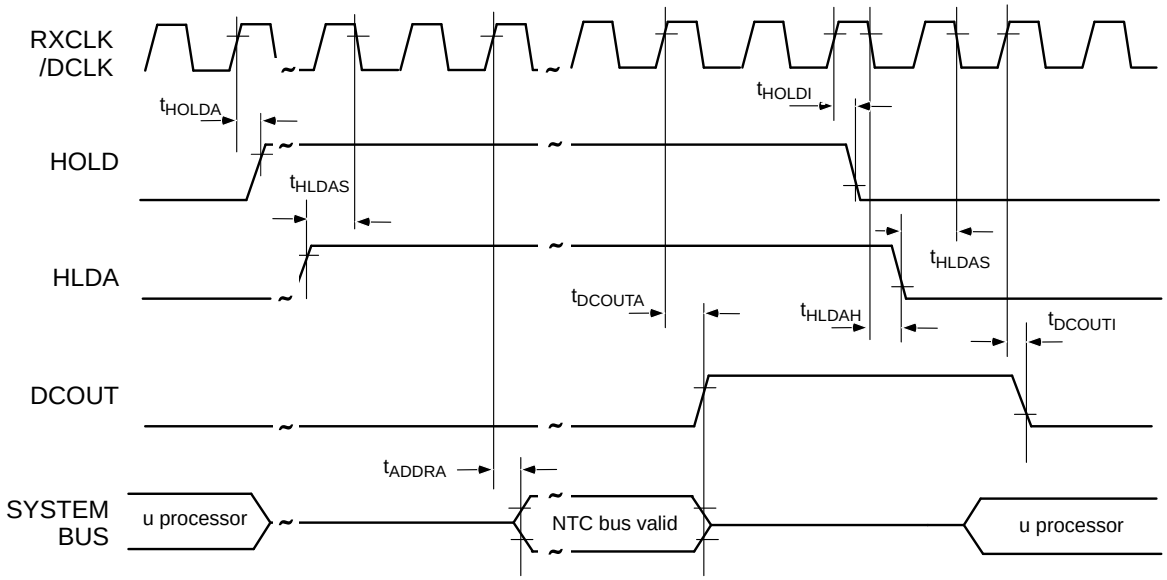


Fig. 78 – INTEL DMA Access Timing

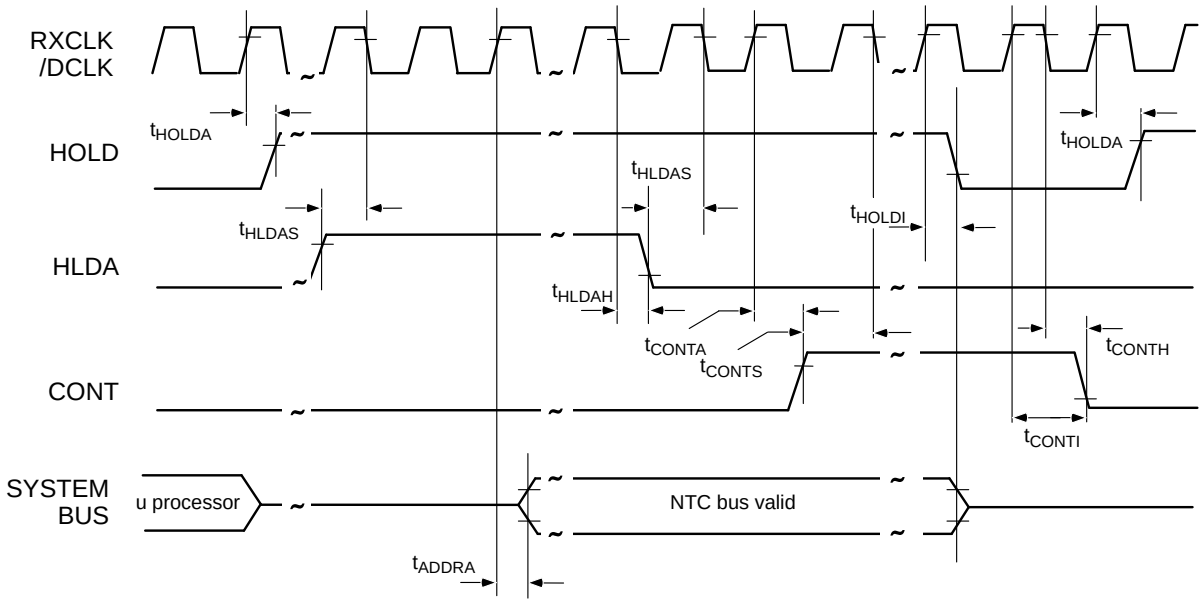


Fig. 79 – INTEL DMA Access Control Override Timing

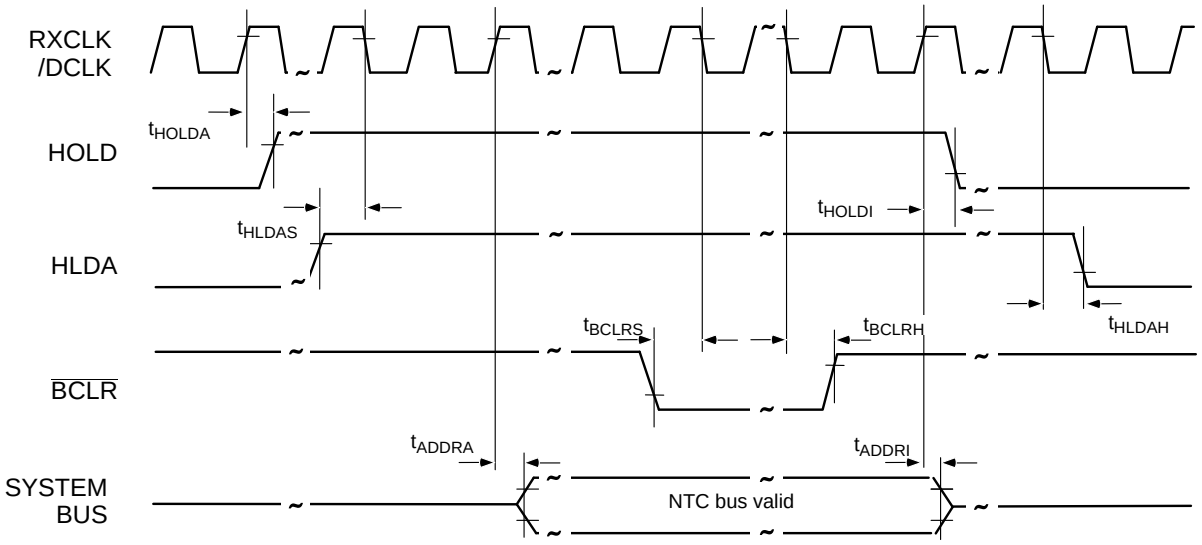


Fig. 81 – INTEL DMA Access Bus Clear Timing

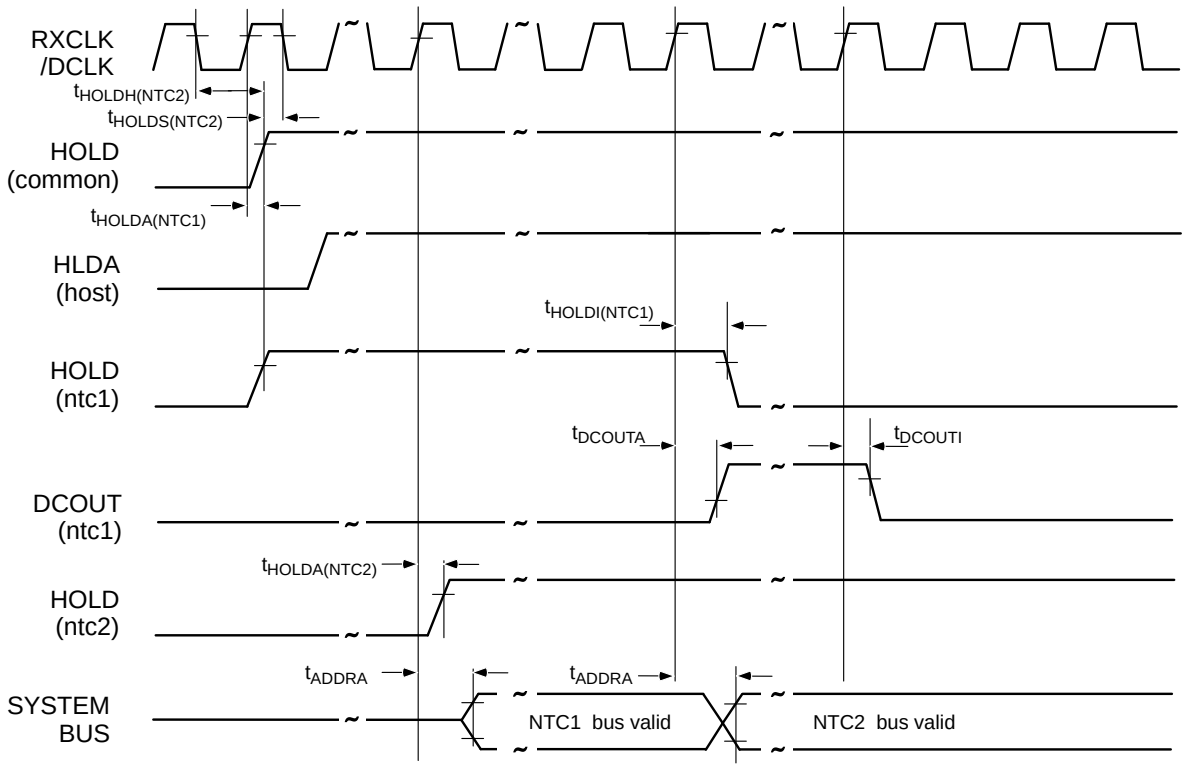


Fig. 80 – INTEL DMA Chaining Timing (2 NTCs)

Parameter	Ref Signal	Abrev	Values			Units (ns)
			Min	Typical	Max	
HOLD Active Delay	HOLD	t_{HOLDA}				ns
HOLD Inactive Delay	HOLD	t_{HOLDI}				ns
HOLD Setup Time	HOLD	t_{HOLDS}				ns
HOLD Hold Time	HOLD	t_{HOLDH}				ns
HLDA Setup Time	HLDA	t_{HLDAS}				ns
HLDA Hold Time	HLDA	t_{HLDAH}				ns
DCOUT Active Delay	DCOUT	t_{DCOUTA}				ns
DCOUT Inactive Delay	DCOUT	t_{DCOUTI}				ns
CONT Active Delay	CONT	t_{CONTA}				ns
CONT Inactive Delay	CONT	t_{CONTI}				ns
CONT Setup Time	CONT	t_{CONTS}				ns
CONT Hold Time	CONT	t_{CONTH}				ns
$\overline{\text{BCLR}}$ Setup Time	$\overline{\text{BCLR}}$	t_{BCLRS}				ns
$\overline{\text{BCLR}}$ Hold Time	$\overline{\text{BCLR}}$	t_{BCLRH}				ns

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 9 – Microprocessor Interface – INTEL DMA Access AC Timing

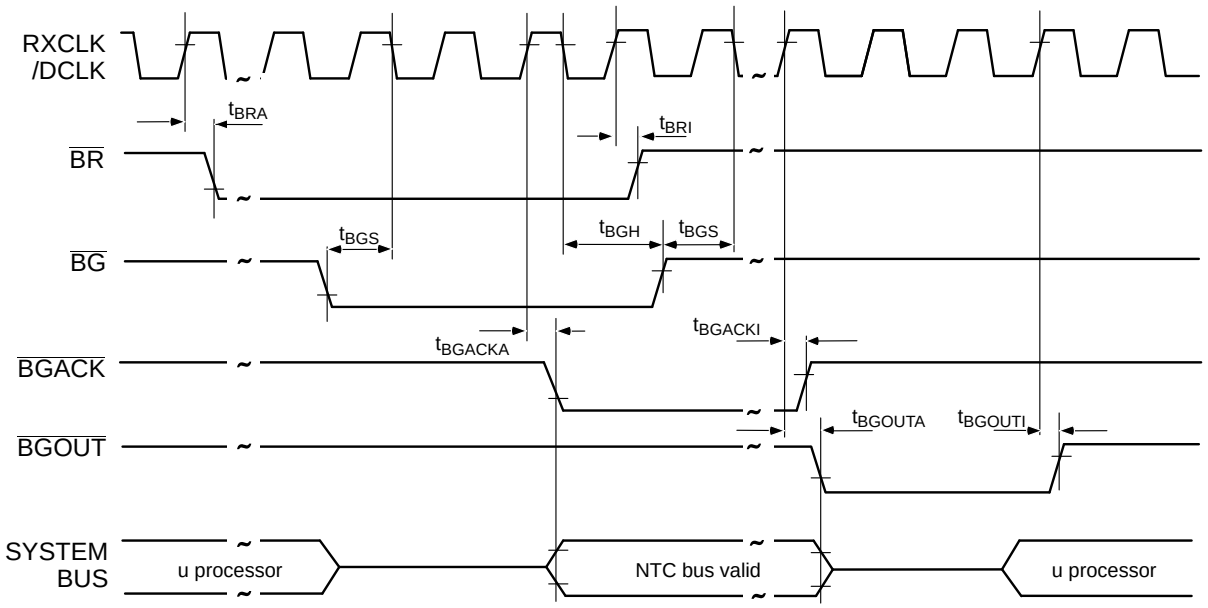


Fig. 82 – MOTOROLA DMA Access Timing

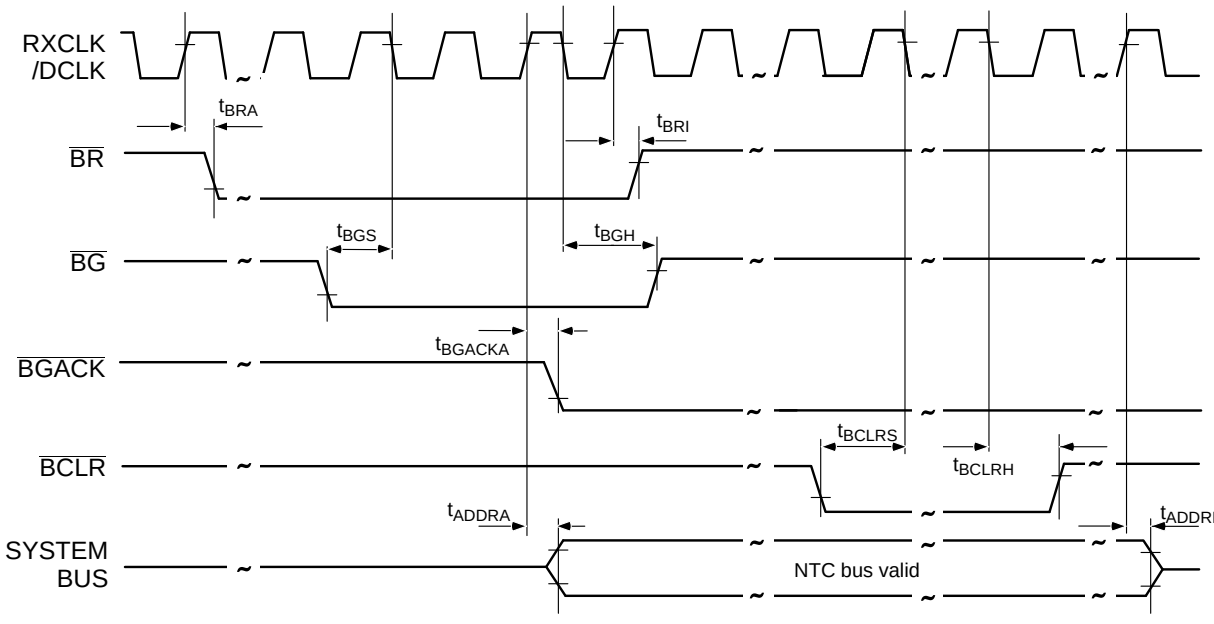


Fig. 83 – MOTOROLA DMA Access Bus Clear Timing

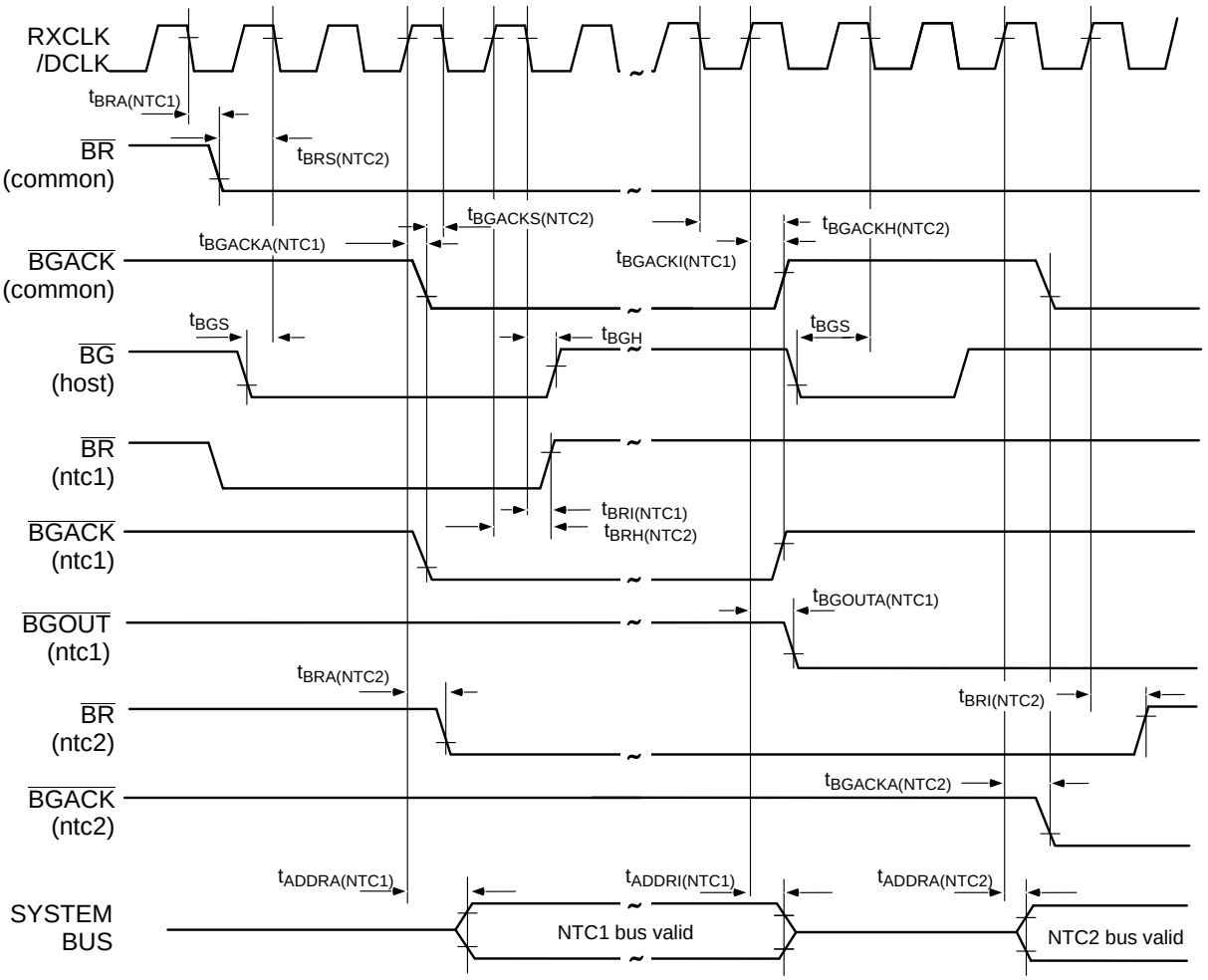


Fig. 84 – MOTOROLA DMA Access Daisy Chaining Timing (2 NTCs)

Parameter	Ref Signal	Abrev	Values			Units (ns)
			Min	Typical	Max	
$\overline{BR}$ Active Delay	$\overline{BR}$	t_{BRA}				ns
$\overline{BR}$ Inactive Delay	$\overline{BR}$	t_{BRI}				ns
$\overline{BR}$ Setup Time	$\overline{BR}$	t_{BRS}				ns
$\overline{BR}$ Hold Time	$\overline{BR}$	t_{BRH}				ns
$\overline{BGACK}$ Active Delay	$\overline{BGACK}$	t_{BGACKA}				ns
$\overline{BGACK}$ Inactive Delay	$\overline{BGACK}$	t_{BGACKI}				ns
$\overline{BGACK}$ Setup Time	$\overline{BGACK}$	t_{BGACKS}				ns
$\overline{BGACK}$ Hold Time	$\overline{BGACK}$	t_{BGACKH}				ns
$\overline{BG}$ Setup Time	$\overline{BG}$	t_{BGS}				ns
$\overline{BG}$ Hold Time	$\overline{BG}$	t_{BGH}				ns
$\overline{BGOUT}$ Active Delay	$\overline{BGOUT}$	t_{BGOUTA}				ns
$\overline{BGOUT}$ Inactive Delay	$\overline{BGOUT}$	t_{BGOUTI}				ns
$\overline{BCLR}$ Setup Time	$\overline{BCLR}$	t_{BCLRS}				ns
$\overline{BCLR}$ Hold Time	$\overline{BCLR}$	t_{BCLRH}				ns

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 10 – Microprocessor Interface – MOTOROLA DMA Access AC Timing

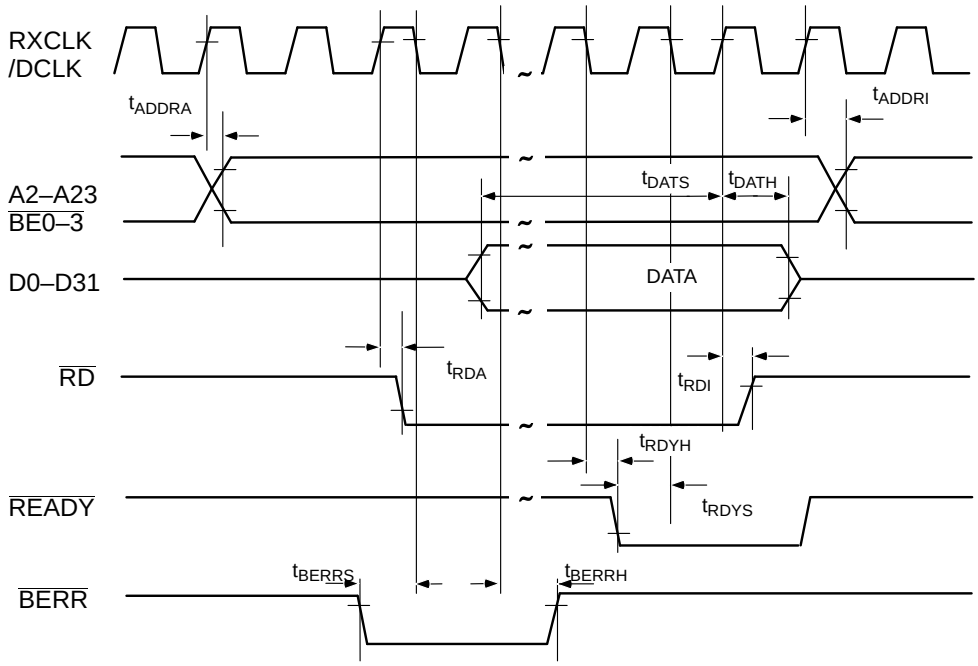


Fig. 85 – INTEL DMA Read Cycle Timing

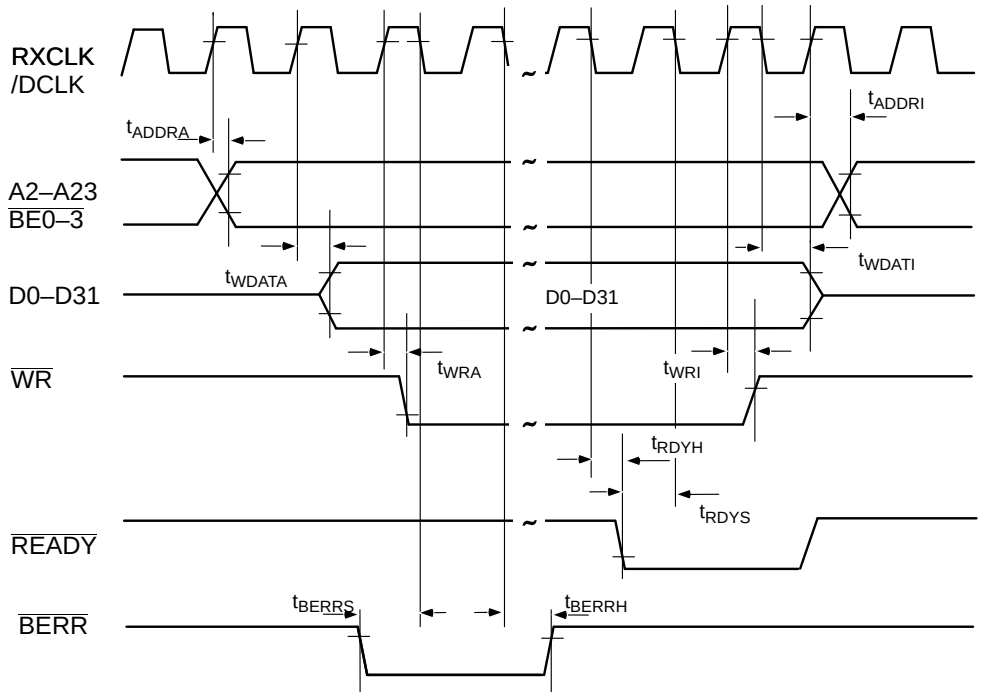


Fig. 86 – INTEL DMA Write Cycle Timing

Parameter	Ref Signal	Abrev	Values			Units (ns)
			Min	Typical	Max	
Address Active Delay	A2–A23	t_{ADDRA}				
Address Inactive Delay	A2–A23	t_{ADDRA}				
Read Active Delay	$\overline{RD}$	t_{RDA}				
Read Inactive Delay	$\overline{RD}$	t_{RDI}				
Setup Time of Ready	$\overline{READY}$	t_{RDYS}				
Hold Time of Ready	$\overline{READY}$	t_{RDYH}				
Setup Time of Data	D0–D31	t_{DATS}				
Hold Time of Data	D0–D31	t_{DATH}				
Write Active Delay	$\overline{WR}$	t_{WRA}				
Write Inactive Delay	$\overline{WR}$	t_{WRI}				
Write Data Active Delay	D0–D31	t_{WDATA}				
Write Data Inactive Delay	D0–D31	t_{WDATI}				
$\overline{BERR}$ Setup Time	$\overline{BERR}$	t_{BERRS}				
$\overline{BERR}$ Hold Time	$\overline{BERR}$	t_{BERRH}				

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 11 – Microprocessor Interface – INTEL DMA Bus Cycle AC Timing

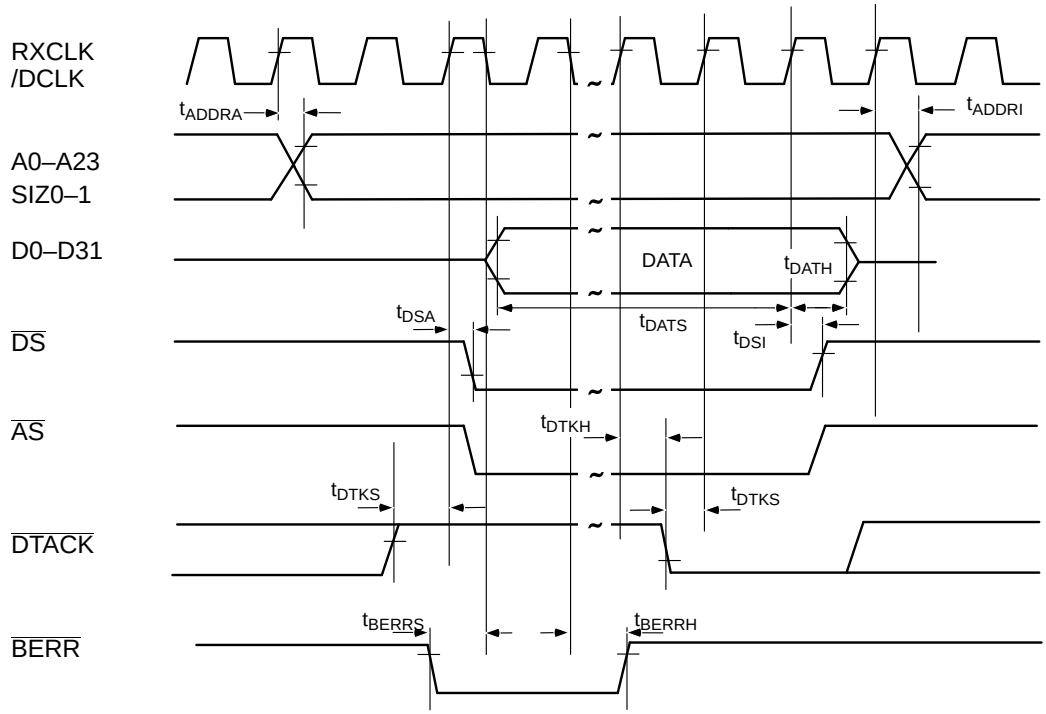


Fig. 87 – MOTOROLA DMA Read Cycle Timing

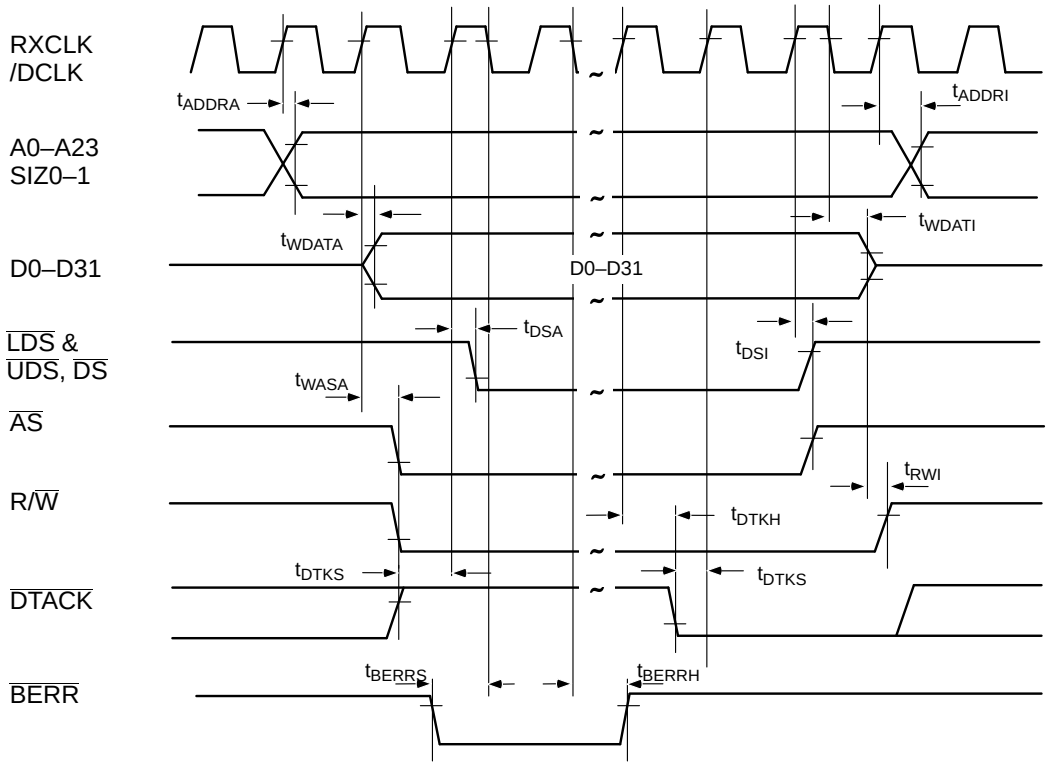


Fig. 88 – MOTOROLA DMA Write Cycle Timing

Parameter	Ref Signal	Abrev	Values			Units (ns)
			Min	Typical	Max	
Address Active Delay	A0–A23	t_{ADSTBA}				ns
Address Inactive Delay	A0–A23	t_{ADSTBI}				ns
$\overline{DS}$ Active Delay	$\overline{DS}$	t_{DSA}				ns
$\overline{DS}$ Inactive Delay	$\overline{DS}$	t_{DSI}				ns
Setup time of $\overline{DTACK}$	$\overline{DTACK}$	t_{DTKS}				ns
Hold Time of $\overline{DTACK}$	$\overline{DTACK}$	t_{DTKI}				ns
Data Setup Time	D0–D31	t_{DATS}				ns
Data Hold Time	D0–D31	t_{DATH}				ns
Write Data Active Delay	D0–D31	t_{DATA}				ns
Write Data Inactive Delay	D0–D31	t_{DATI}				ns
$\overline{AS}$ Active Delay	$\overline{AS}$	t_{WASA}				ns
R/$\overline{W}$ Inactive Delay	R/$\overline{W}$	t_{RWI}				ns
$\overline{BERR}$ Setup Time	$\overline{BERR}$	t_{BERRS}				ns
$\overline{BERR}$ Hold Time	$\overline{BERR}$	t_{BERRH}				ns

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 12 – Microprocessor Interface – MOTOROLA DMA Bus Cycles AC Timing

E. JTAG

E.1 JTAG Cells

The Boundary Scan Register (BSR) consists of 223 registers, which form a serial shift register starting from pin 133 (LOS), moving in an anticlockwise direction around the chip to finish at pin 128 (BW).

It should be noted that none of the internal D–types which form the BSR are reset and hence, are initially undefined. A valid pattern needs to be shifted into the register prior to any testing. However, while the JTAG TAP controller is reset, the I/O pins are connected through to the system logic.

I / O Pin Type:
I = Input,
C = Clock input,
O = Output,
B = Bidirectional,
T = Tristate,
Iu = Input with pull-up resistor.

BSR Cell Type:
BSI1 allows capture of device input pin and control of logic input pin.
BSI3 allows capture of device input pin only.
BSO allows capture of logic output pin and control of device output pin.
BSOE allows control of tristate-able output pin.
BSDI allows control of bidirectional pin.
BSBI allows capture and control of bidirectional input and output pin (= BSI1 + BSO).

Control Group No.:
Denotes a JTAG BSR cell which controls a (group of) tristate-able output(s) or bidirectional pin(s).

Controlled Group No.:
Denotes a JTAG BSR cell which connects to a tristate-able output or bidirectional pin which is controlled by the JTAG BSR cell numbered in the previous column.

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
1	BSI1			I	133	LOS
2	BSI1			I	134	TRFD
3	BSI1			I	136	RDAV
4	BSI1			I	137	RD0
5	BSI1			I	138	RD1
6	BSI1			I	139	RD2
7	BSI1			I	140	RD3
8	BSI1			I	141	RD4
9	BSI1			I	142	RD5
10	BSI1			I	143	RD6
11	BSI1			I	145	RD7
12	BSI3			C	146	RCLK
13	BSO			O	147	TD0
14	BSO			O	148	TD1
15	BSO			O	149	TD2
16	BSO			O	150	TD3
17	BSO			O	151	TD4
18	BSO			O	152	TD5
19	BSO			O	153	TD6
20	BSO			O	155	TD7
21	BSI3			C	156	TCLK
22	BSDI	1				
23 & 24	BSBI		1	B	157	$\overline{RD}$ / $\overline{AS}$
25 & 26	BSBI		1	B	158	$\overline{WR}$ / R/$\overline{W}$
27	BSDI	2				
28 & 29	BSBI		2	B	159	$\overline{BHE}$ / $\overline{UDS}$ / $\overline{DS}$
30 & 31	BSBI		1	B	160	A0 / $\overline{LDS}$ / $\overline{BE0}$
32 & 33	BSBI		1	B	161	A1 / $\overline{BE1}$
34	BSDI	3				
35 & 36	BSBI		3	B	162	SIZ0 / $\overline{BE2}$
37 & 38	BSBI		3	B	163	SIZ1 / $\overline{BE3}$
39	BSDI	4				
40 & 41	BSBI		4	B	165	HOLD / $\overline{BR}$
42	BSI1			I	166	HLDA / $\overline{BG}$
43	BSDI	5				
44 & 45	BSBI		5	B	167	CONT / $\overline{BGACK}$
46	BSI1			I	168	$\overline{DTACK}$ / $\overline{READY}$
47	BSOE	6				
48	BSO		6	T	169	DCOUT / $\overline{BGOUT}$
49	BSOE	7				
50	BSO		7	T	170	$\overline{IRQ}$
51	BSI1			I	171	$\overline{CS}$

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
52	BSO			O	172	RDYOUT
53	BSI1			I	173	$\overline{\text{BCLR}}$
54	BSDI	8				
55 & 56	BSBI		8	B	175	D0
57 & 58	BSBI		8	B	176	D1
59 & 60	BSBI		8	B	1	D2
61 & 62	BSBI		8	B	2	D3
63 & 64	BSBI		8	B	4	D4
65 & 66	BSBI		8	B	5	D5
67 & 68	BSBI		8	B	6	D6
69 & 70	BSBI		8	B	7	D7
71 & 72	BSBI		8	B	8	D8
73 & 74	BSBI		8	B	9	D9
75 & 76	BSBI		8	B	10	D10
77 & 78	BSBI		8	B	11	D11
79 & 80	BSBI		8	B	13	D12
81 & 82	BSBI		8	B	14	D13
83 & 84	BSBI		8	B	15	D14
85 & 86	BSBI		8	B	16	D15
87	BSDI	9				
88 & 89	BSBI		9	B	17	D16
90 & 91	BSBI		9	B	18	D17
92 & 93	BSBI		9	B	19	D18
94 & 95	BSBI		9	B	20	D19
96 & 97	BSBI		9	B	21	D20
98 & 99	BSBI		9	B	23	D21
100 & 101	BSBI		1	B	24	A2
102 & 103	BSBI		1	B	25	A3
104 & 105	BSBI		1	B	26	A4
106 & 107	BSBI		1	B	27	A5
108 & 109	BSBI		1	B	28	A6
110	BSO		1	T	29	A7
111	BSO		1	T	30	A8
112	BSO		1	T	31	A9
113	BSO		1	T	33	A10
114	BSO		1	T	34	A11
115 & 116	BSBI		9	B	35	D22
117 & 118	BSBI		9	B	36	D23
119 & 120	BSBI		9	B	37	D24
121 & 122	BSBI		9	B	38	D25
123 & 124	BSBI		9	B	39	D26
125 & 126	BSBI		9	B	40	D27

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
127 & 128	BSBI		9	B	41	D28
129 & 130	BSBI		9	B	42	D29
131 & 132	BSBI		9	B	43	D30
133 & 134	BSBI		9	B	44	D31
135	BSO		1	T	45	A12
136	BSO		1	T	46	A13
137	BSO		1	T	48	A14
138	BSO		1	T	49	A15
139	BSO		1	T	50	A16
140	BSO		1	T	51	A17
141	BSO		1	T	52	A18
142	BSO		1	T	53	A19
143	BSO		1	T	54	A20
144	BSO		1	T	55	A21
145	BSO		1	T	57	A22
146	BSO		1	T	58	A23
147	BSI3			C	61	DCLK
148	BSI1			Iu	62	CLKSEL
149	BSI1			Iu	64	CS / $\overline{UT}$
150	BSI3			C	65	RXCLK
151	BSO			O	67	RXD7
152	BSO			O	68	RXD6
153	BSO			O	69	RXD5
154	BSO			O	70	RXSOC
155	BSO			O	71	RXD4
156	BSO			O	72	RXD3
157	BSO			O	73	RXD2
158	BSO			O	74	RXD1
159	BSO			O	75	RXD0
160	BSI3			C	77	TXCLK
161	BSI1			I	78	TXD7
162	BSI1			I	79	TXD6
163	BSI1			I	80	TXD5
164	BSI1			I	81	TXSOC
165	BSI1			I	82	TXD4
166	BSI1			I	83	TXD3
167	BSI1			I	84	TXD2
168	BSI1			I	85	TXD1
169	BSI1			I	87	TXD0
170	BSI1			I	88	TXEN
171	BSO			O	89	$\overline{TXFULL}$
172	BSI1			I	90	RXEN

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
173	BSO			O	92	$\overline{\text{RXEMPTY}}$
174	BSDI	10				
175 & 176	BSBI		10	B	93	ATD7
177 & 178	BSBI		10	B	94	ATD6
179 & 180	BSBI		10	B	95	ATD5
181 & 182	BSBI		10	B	96	ATD4
183 & 184	BSBI		10	B	97	ATD3
185 & 186	BSBI		10	B	98	ATD2
187 & 188	BSBI		10	B	99	ATD1
189 & 190	BSBI		10	B	101	ATD0
191	BSO			O	102	ATRFDO
192	BSI1			I	103	ATDAVI
193	BSI1			I	104	ATRFDI
194	BSO			O	105	ATDAVO
195	BSDI	11				
196 & 197	BSBI		11	B	106	ARD7
198 & 199	BSBI		11	B	107	ARD6
200 & 201	BSBI		11	B	108	ARD5
202 & 203	BSBI		11	B	109	ARD4
204	BSI1			I	111	$\overline{\text{RESET}}$
205 & 206	BSBI		11	B	112	ARD3
207 & 208	BSBI		11	B	113	ARD2
209 & 210	BSBI		11	B	114	ARD1
211 & 212	BSBI		11	B	115	ARD0
213	BSO			O	116	ARRFDO
214	BSI1			I	117	ARDAVI
215	BSI1			I	118	ARRFDI
216	BSO			O	119	ARDAVO
217	BSI3			C	121	STATSCLK
218	BSI1			I	122	STATSIN
219	BSI1			I	124	$\overline{\text{BERR}}$
220	BSO			O	125	SYNCOUT
221	BSI1			I	126	BSWAP
222	BSI1			I	127	BM
223	BSI1			I	128	BW
				C	129	TCK
				I	130	TMS
				I	131	TDI
				T	132	TDO

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
					3	V_{SS}
					12	V_{SS}
					32	V_{SS}
					47	V_{SS}
					56	V_{SS}
					76	V_{SS}
					91	V_{SS}
					100	V_{SS}
					120	V_{SS}
					135	V_{SS}
					144	V_{SS}
					164	V_{SS}
					22	V_{DD}
					66	V_{DD}
					86	V_{DD}
					110	V_{DD}
					154	V_{DD}
					174	V_{DD}
					59	N / C
					60	N / C
					63	N / C
					123	RESERVED

F. PHYSICAL PIN DIAGRAM

F.1 Pin Diagram

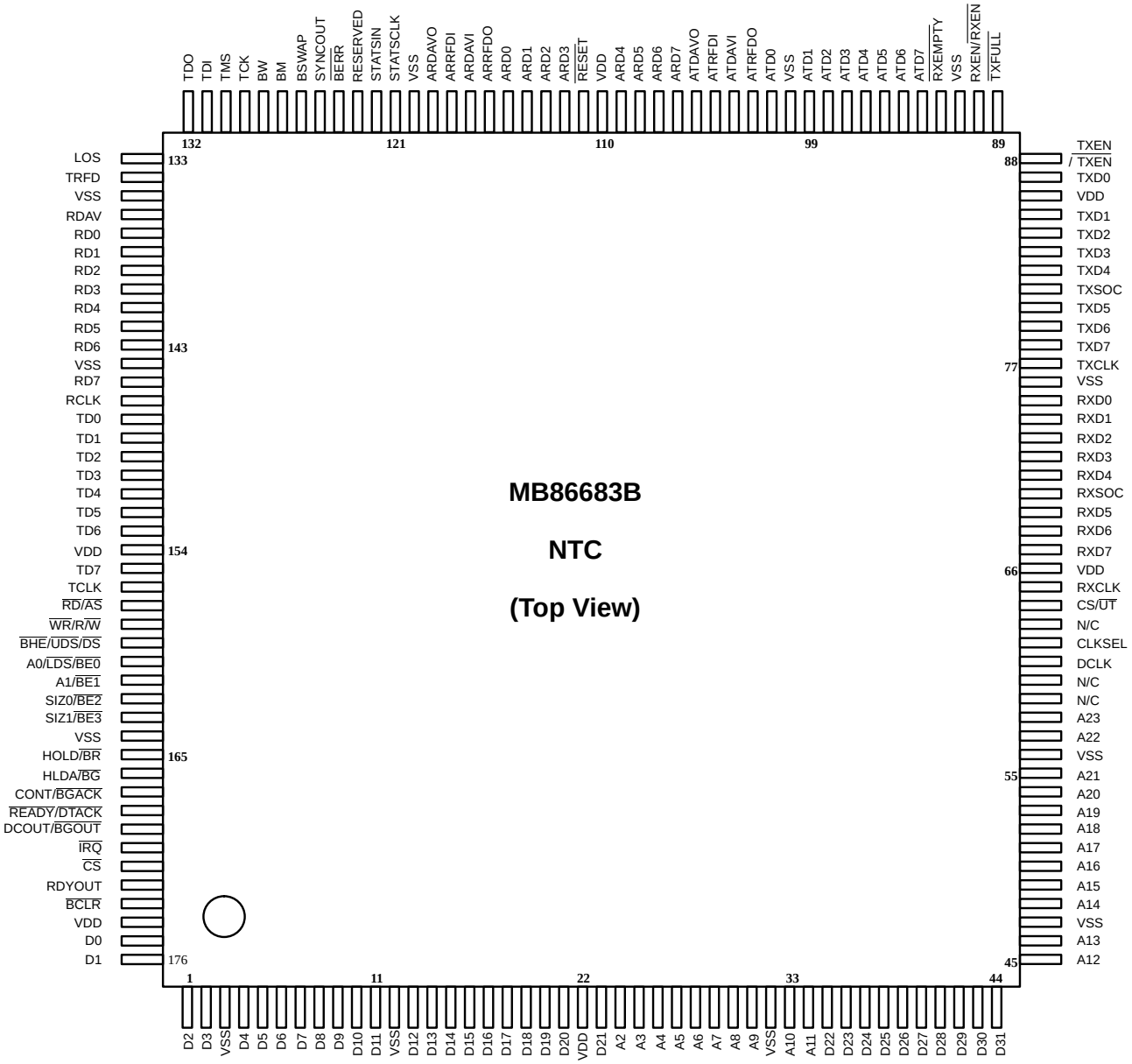


Fig. 89 – NTC Pin Assignment

F.2 Pin Assignments

Pin No.	Pin Name	Type	Function
1	D2	I/O	Microprocessor data bus bit D2
2	D3	I/O	Microprocessor data bus bit D3
3	VSS	–	
4	D4	I/O	Microprocessor data bus bit D4
5	D5	I/O	Microprocessor data bus bit D5
6	D6	I/O	Microprocessor data bus bit D6
7	D7	I/O	Microprocessor data bus bit D7
8	D8	I/O	Microprocessor data bus bit D8
9	D9	I/O	Microprocessor data bus bit D9
10	D10	I/O	Microprocessor data bus bit D10
11	D11	I/O	Microprocessor data bus bit D11
12	VSS	–	
13	D12	I/O	Microprocessor data bus bit D12
14	D13	I/O	Microprocessor data bus bit D13
15	D14	I/O	Microprocessor data bus bit D14
16	D15	I/O	Microprocessor data bus bit D15
17	D16	I/O	Microprocessor data bus bit D16
18	D17	I/O	Microprocessor data bus bit D17
19	D18	I/O	Microprocessor data bus bit D18
20	D19	I/O	Microprocessor data bus bit D19
21	D20	I/O	Microprocessor data bus bit D20
22	VDD	–	
23	D21	I/O	Microprocessor data bus bit D21
24	A2	I/O	Microprocessor address bus bit A2
25	A3	I/O	Microprocessor address bus bit A3
26	A4	I/O	Microprocessor address bus bit A4
27	A5	I/O	Microprocessor address bus bit A5
28	A6	I/O	Microprocessor address bus bit A6
29	A7	O	Microprocessor address bus bit A7
30	A8	O	Microprocessor address bus bit A8
31	A9	O	Microprocessor address bus bit A9
32	VSS	–	
33	A10	O	Microprocessor address bus bit A10
34	A11	O	Microprocessor address bus bit A11
35	D22	I/O	Microprocessor data bus bit D22
36	D23	I/O	Microprocessor data bus bit D23
37	D24	I/O	Microprocessor data bus bit D24
38	D25	I/O	Microprocessor data bus bit D25
39	D26	I/O	Microprocessor data bus bit D26
40	D27	I/O	Microprocessor data bus bit D27
41	D28	I/O	Microprocessor data bus bit D28
42	D29	I/O	Microprocessor data bus bit D29
43	D30	I/O	Microprocessor data bus bit D30
44	D31	I/O	Microprocessor data bus bit D31

Pin No.	Pin Name	Type	Function
45	A12	O	Microprocessor address bus bit A12
46	A13	O	Microprocessor address bus bit A13
47	VSS	–	
48	A14	O	Microprocessor address bus bit A14
49	A15	O	Microprocessor address bus bit A15
50	A16	O	Microprocessor address bus bit A16
51	A17	O	Microprocessor address bus bit A17
52	A18	O	Microprocessor address bus bit A18
53	A19	O	Microprocessor address bus bit A19
54	A20	O	Microprocessor address bus bit A20
55	A21	O	Microprocessor address bus bit A21
56	VSS	–	
57	A22	O	Microprocessor address bus bit A22
58	A23	O	Microprocessor address bus bit A23
59	N/C	–	Not connected
60	N/C	–	Not connected
61	DCLK	I	DMA / System clock
62	CLKSEL	I	System clock select
63	N/C	–	Not connected
64	CS/$\overline{UT}$	I	Fujitsu / Utopia cell stream mode
65	RXCLK	I	Cell stream receive clock (system clock)
66	VDD	–	
67	RXD7	O	Cell stream received data, bit 7
68	RXD6	O	Cell stream received data, bit 6
69	RXD5	O	Cell stream received data, bit 5
70	RXSOC	O	Cell stream receive start of cell
71	RXD4	O	Cell stream received data, bit 4
72	RXD3	O	Cell stream received data, bit 3
73	RXD2	O	Cell stream received data, bit 2
74	RXD1	O	Cell stream received data, bit 1
75	RXD0	O	Cell stream received data, bit 0
76	VSS	–	
77	TXCLK	I	Cell stream transmit clock
78	TXD7	I	Cell stream transmit data, bit 7
79	TXD6	I	Cell stream transmit data, bit 6
80	TXD5	I	Cell stream transmit data, bit 5
81	TXSOC	I	Cell stream transmit clock
82	TXD4	I	Cell stream transmit data, bit 4
83	TXD3	I	Cell stream transmit data, bit 3
84	TXD2	I	Cell stream transmit data, bit 2
85	TXD1	I	Cell stream transmit data, bit 1
86	VDD	–	
87	TXD0	I	Cell stream transmit data, bit 0
88	TXEN/$\overline{TXEN}$	I	Cell stream transmit enable
89	$\overline{TXFULL}$	0	Cell stream transmitter full
90	RXEN/$\overline{RXEN}$	I	Cell stream receive enable

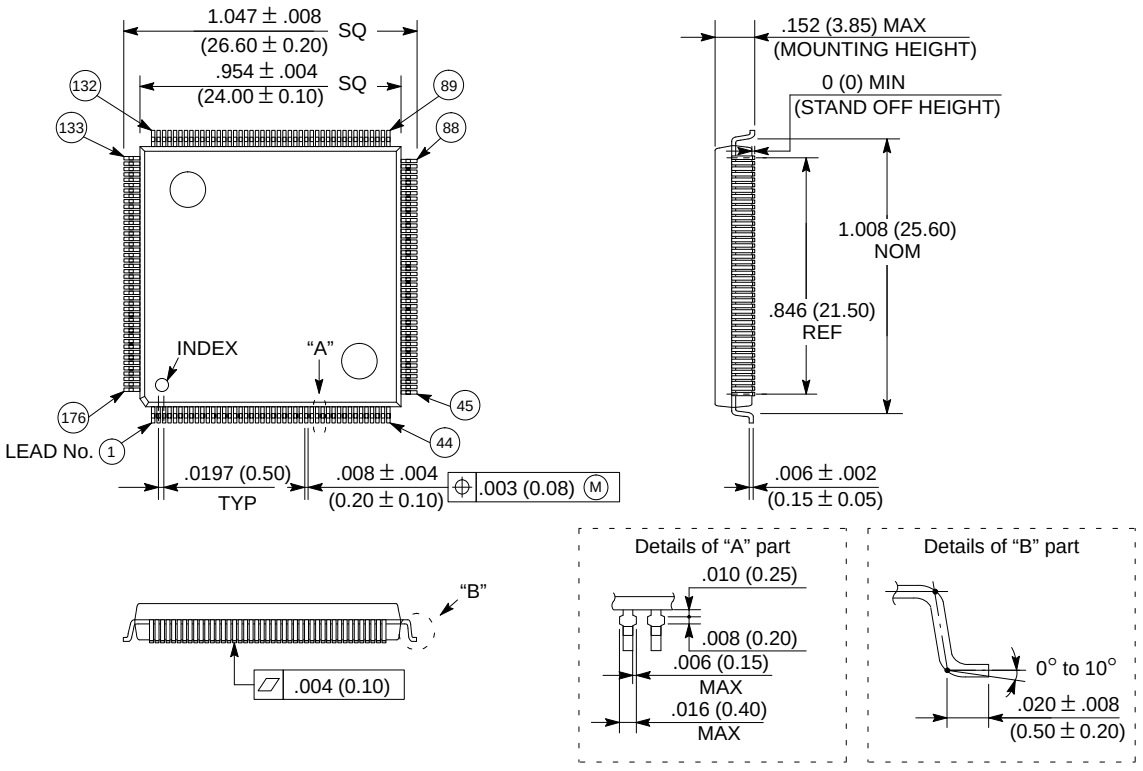
Pin No.	Pin Name	Type	Function
91	VSS	–	
92	$\overline{\text{RXEMPTY}}$	O	Cell stream receiver empty
93	ATD7	I/O	Transmit ATC data bus, bit 7
94	ATD6	I/O	Transmit ATC data bus, bit 7
95	ATD5	I/O	Transmit ATC data bus, bit 7
96	ATD4	I/O	Transmit ATC data bus, bit 7
97	ATD3	I/O	Transmit ATC data bus, bit 7
98	ATD2	I/O	Transmit ATC data bus, bit 7
99	ATD1	I/O	Transmit ATC data bus, bit 7
100	VSS	–	
101	ATD0	I/O	Transmit ATC data bus, bit 7
102	ATRFDO	O	Transmit ATC ready for data output
103	ATDAVI	I	Transmit ATC data available input
104	ATRFDI	I	Transmit ATC ready for data input
105	ATDAVO	O	Transmit ATC data available output
106	ARD7	I/O	Receive ATC data bus, bit 7
107	ARD6	I/O	Receive ATC data bus, bit 6
108	ARD5	I/O	Receive ATC data bus, bit 5
109	ARD4	I/O	Receive ATC data bus, bit 4
110	VDD	–	
111	$\overline{\text{RESET}}$	I	NTC master reset input
112	ARD3	I/O	Receive ATC data bus, bit 3
113	ARD2	I/O	Receive ATC data bus, bit 2
114	ARD1	I/O	Receive ATC data bus, bit 1
115	ARD0	I/O	Receive ATC data bus, bit 0
116	ARRFDO	O	Receive ATC ready for data output
117	ARDAVI	I	Receive ATC data available input
118	ARRFDI	I	Receive ATC ready for data input
119	ARDAVO	O	Receive ATC data available output
120	VSS	–	
121	STATSCLK	I	Switch statistics clock input
122	STATSIN	I	Switch statistics serial data input
123	RESERVED	–	Leave unconnected
124	$\overline{\text{BERR}}$	I	Bus Error Input
125	SYNCOUT	O	Transceiver transmitter Cell/Frame Sync output
126	BSWAP	I	Bus swap; Little Endian [0], Big Endian [1]
127	BM	I	Bus mode; Intel [0], Motorola [1]
128	BW	I	Bus width select input; 16 [0], 32 [1]
129	TCK	I	JTAG test clock
130	TMS	I	JTAG test mode select
131	TDI	I	JTAG test data input
132	TDO	O	JTAG test data output
133	LOS	I	Loss of signal input
134	TRFD	I	Transmit ready for data
135	VSS	–	
136	RDAV	I	Receive data available input

Pin No.	Pin Name	Type	Function
137	RD0	I	Receive data, bus, bit 0
138	RD1	I	Receive data, bus, bit 1
139	RD2	I	Receive data, bus, bit 2
140	RD3	I	Receive data, bus, bit 3
141	RD4	I	Receive data, bus, bit 4
142	RD5	I	Receive data, bus, bit 5
143	RD6	I	Receive data, bus, bit 6
144	VSS	–	
145	RD7	I	Receive data, bus, bit 7
146	RCLK	I	Receive clock input
147	TD0	O	Transmit data, bus, bit 0
148	TD1	O	Transmit data, bus, bit 1
149	TD2	O	Transmit data, bus, bit 2
150	TD3	O	Transmit data, bus, bit 3
151	TD4	O	Transmit data, bus, bit 4
152	TD5	O	Transmit data, bus, bit 5
153	TD6	O	Transmit data, bus, bit 6
154	VDD	–	
155	TD7	O	Transmit data, bus, bit 7
156	TCLK	I	Transmit clock input
157	$\overline{RD}/\overline{AS}$	I/O	µprocessor Read / Address Strobe
158	$\overline{WR}/R\overline{W}$	I/O	µprocessor Write/Read/Write
159	$\overline{BHE}/\overline{UDS}/\overline{DS}$	I/O	µprocessor Byte High Enable / Upper Data Strobe/Data Strobe
160	$A0/\overline{LDS}/\overline{BE0}$	I/O	µprocessor Address bit 0 / Lower data Strobe / Byte Enable 0
161	$A1/\overline{BE1}$	I/O	µprocessor Address bit 0/Byte Enable 1
162	$SIZ0/\overline{BE2}$	I/O	µprocessor Size 0/Byte Enable 2
163	$SIZ1/\overline{BE3}$	I/O	µprocessor Size 1/Byte Enable 3
164	VSS	–	
165	$HOLD/\overline{BR}$	I/O	µprocessor Hold / Bus Request
166	$HLDA/\overline{BG}$	I	µprocessor Hold Ackknowledge / Bus Grant
167	$CONT/\overline{BGACK}$	I/O	µprocessor Control override / Bus Grant Acknowledge
168	$\overline{READY}/\overline{DTACK}$	I	µprocessor Ready / Data Transfer Acknowledge
169	$DCOUT/\overline{BGOUT}$	O	DMA daisy-chain out/Bus Grant out
170	$\overline{IRQ}$	O	Interrupt Request
171	$\overline{CS}$	I	Chip Select
172	RDYOUT	O	Ready Out, indicates R/W cycle can be terminated
173	$\overline{BCLR}$	I	Bus clear input
174	VDD	I	
175	D0	I/O	Microprocessor data bus, bit D0
176	D1	I/O	Microprocessor data bus, bit D1

G. PACKAGE DIMENSIONS

FPT-176P-M01

176-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-176P-M01)



F176001S–3C

Dimensions in
inches (millimeters)

Fig. 90 – Package Dimensions

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