MBL8392A

COAXIAL TRANSCEIVER INTERFACE FOR ETHERNET/THIN ETHERNET

DATA SHEET

APRIL1993

FEATURES

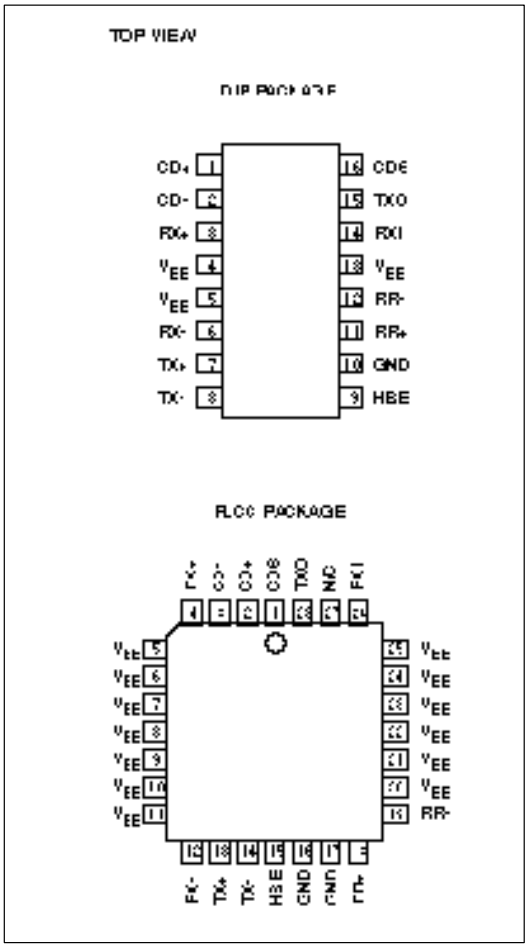
- Compatible with Ethernet II, IEEE 802.3 10BASE5 and 10BASE2, and ISO 8802/-3 interface specifications
- Integrates all active transceiver electronics
- Only one external resistor required for setting coaxial signaling current
- Jabber timer function integrated on chip
- Heartbeat generator can be externally disabled for operation as IEEE 802.3 compatible repeaters
- On-chip precision voltage reference for receive mode collision detection
- Squelch circuitry on all signal inputs rejects noise
- Full ESD protection
- Standard 16-pin DIP and 28-pin PLCC with special lead frames to minimize the operating die temperature
- Power-on reset prevents glitches on coaxial cable during power up

GENERAL DESCRIPTION

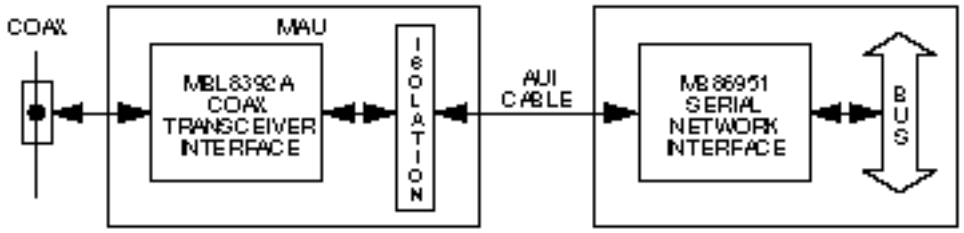
The MBL8392A Coaxial Transceiver Interface (CTI) is a coaxial line driver/receiver for Ethernet (10BASE5) and Thin Ethernet (10BASE2) local area networks. The CTI is part of a three chip set available from Fujitsu that fully implements IEEE 802.3 Ethernet specifications, as shown in the system diagram. The other chip is either the MB8696 NICE™ Ethernet controller or the MB8696S Ether Complexer. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a double terminated 50 Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTl is achieved using DC-to-DC conversion through a power transformer as shown in Figure l.

During transmission the jabber timer is initiated to disable the CTI transmitter in the event of a longer than legal length data packet. Collision detection circuitry monitors the signals on the coaxial cable to determine the presence of colliding packets and signals the DTE in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is functioning correctly. The heart-beat function can be disabled for repeater applications.

PIN CONFIGURATION

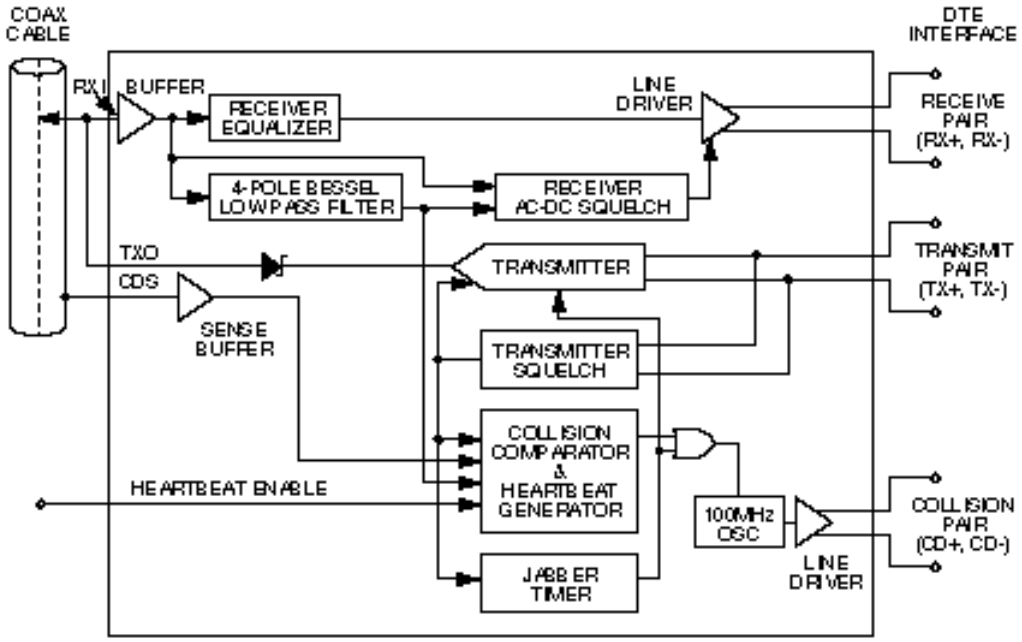


SYSTEM DIAGRAM



MAU = MEDIUM ATTACHMENT UNIT
AUI CABLE = ATTACHMENT UNIT INTERFACE CABLE (NOT USED IN THIN ETHERNET APPLICATIONS)

BLOCK DIAGRAM



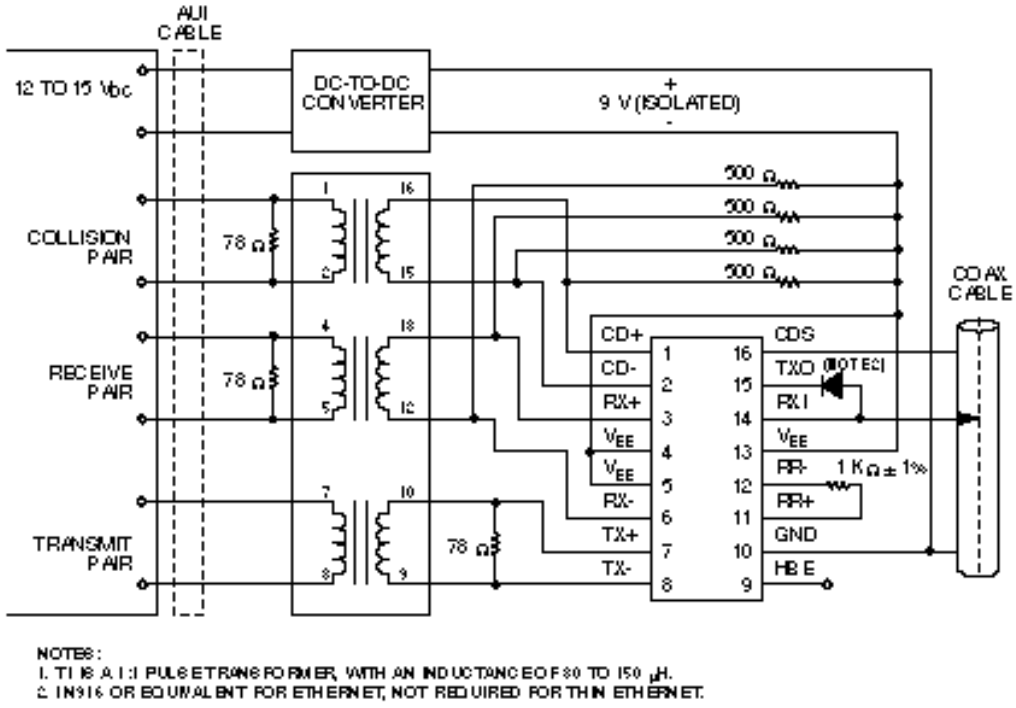


Figure 1. Connection Diagram

PIN DESCRIPTIONS

PIN NO		SYMBOL	TYPE	DESCRIPTION
DIP	PLCC			
1 2	2 3	CD+ CD–	O	**COLLISION OUTPUTS:** Balanced differential line driveroutputs which send a 10 MHz oscillation signal to the DTE inthe event of a collision, jabber interrupt or heartbeat test.
3 6	4 12	RX+ RX–	O	**RECEIVER OUTPUTS:** Balanced differential line driver outputs which send the received signal to the DTE.
7 8	13 14	TX+ TX–	I	**TRANSMITTER INPUTS:** Balanced differential line receiverinputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	15	HBE	I	**HEARTBEAT ENABLE:** The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR–		**EXTERNAL RESISTOR:** A 1 KΩ (1%) resistor connected between these pins establishes the signaling current at TXO.RR– is internally connected to V_{EE}.
14	26	RXI	I	**RECEIVER INPUT:** This pin is connected directly to thecoaxial cable. Received signals are equalized, amplified, andsent to the DTE through the RX± pins.

PIN DESCRIPTIONS

PIN NO		SYMBOL	TYPE	DESCRIPTION
DIP	PLCC			
15	28	TXO	O	**TRANSMITTER OUTPUT:** This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	I	**COLLISION DETECT SENSE:** Ground sense connection for the collision detection circuitry. This pin should be directly connected to the coaxial cable shield to prevent ground drops affecting the collision threshold voltage.
10	16,17	GND	—	**POSITIVE SUPPLY PIN**
4, 5, 13	5 to 11 20 to 25	V_{EE}	—	**NEGATIVE SUPPLY PINS:** These pins also serve as a low thermal resistance path for extracting heat from the die. They should, therefore, be connected to a large metal area on the PC board.

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to 70° C	MBL8393AP-G
28-Pin PLCC	0 to 70° C	MBL8393APD-G

FUNCTIONAL DESCRIPTION

The MBL8392A, as illustrated in the block diagram, contains four main functional blocks. These are:

a. The receiver which takes data from the coaxial cable and sends it to the DTE.

b. The transmitter which receives data from the DTE and sends it onto the coaxial cable.

c. The collision detection and heartbeat generation circuitry which indicates to the DTF any collision on the coaxial cable and tests for collision circuitry functionality at the end of every transmission.

d. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.

RECEIVER FUNCTIONS

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter is lower than the DC squelch threshold. For normal signal levels this will take less than 500 ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250 ns and only enables the receiver again after approximately 1 μs. Receiver timing is shown in Figures 2 and 4.

The differential line driver provides typically ±900 mV signals to the DTE with less than 7 ns rise and fall times. When in idle state (no received signal) its outputs provide less than 20 mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs are emitter followers and, for

Ethernet applications where they drive a 78 Ω transmission line, require 500 Ω pull-down resistors to V_{EE}. For Thin Ethernet applications where the AUl cable is not used, the pull-down resistors can be increased to l.5 KΩ to reduce power consumption.

TRANSMITTER FUNCTIONS

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTl and should not be altered by external circuitry. Controlled rise and fall times of 25 ns (±5 ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2 ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the MBL8392A meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled by negative-going differential signals of typically greater than 225 mV in magnitude and 15 ns in duration. The transmitter will

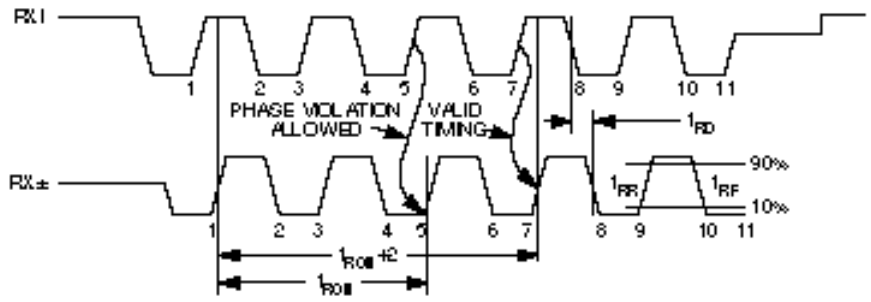


Figure 2. Receiver Timing

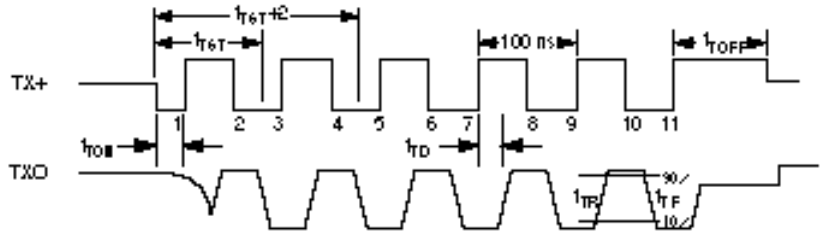


Figure 3. Transmitter Timing

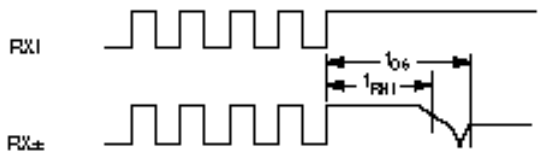


Figure 4. Receiver End–of–Packet Timing

be disabled at the end of a packet if there are no negative-going signals of greater than 225 mV for more than typically 250 ns, as shown in Figure 3.

COLLISION FUNCTIONS

The collision detection scheme implemented in the MBL8392A is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and nonrepeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10 MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10 MHz oscillation signal at the CD outputs and typically occurs within 700 ns of the onset of the collision. The collision signal begins with a negative going pulse and ends with a continuous high-to-idle state longer than 170 ns. Figure 5 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. The pseudo collision consists of a 1 μs burst of 10 MHz oscillation at the line driver outputs approximately 1 μs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) input to V_{EE}. This allows the CTI to be used in repeater applications. Figure 6 illustrates heartbeat timing.

As with the receiver outputs, the collision outputs also require pull down resistors to V_{EE} and maintain less than 20 mV differential voltage offset in the idle state to minimize DC standing current in the isolation transformers.

JABBER FUNCTIONS

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30 ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450 ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 7 illustrates jabber timing.

DETECTION OF COAXIAL CABLE FAULTS

In the MBL8392A there is no internal loopback path from the TX inputs to the RX outputs. This means that when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs. An intelligent DTE can, therefore, detect this fault. If the fault is an open circuit, then a continuous collision signal will be sent to the DTE, provided the average DC voltage at the RXI pin is greater than the typical collision threshold of –l.53V.

If a short or open circuit occurs elsewhere on the coaxial cable, the resulting reflections can result in an impedance at the CTI of any value between a short circuit and 50 Ω, depending on the distance of the CTI from the fault. The upper limit of 50 Ω results from the fact that the coaxial cable is terminated in 50 Ω at both ends. Faults on the cable itself are, therefore, not guaranteed to be detected by simply monitoring the RX and CD pins when in the transmit mode, and more sophisticated schemes may be necessary.

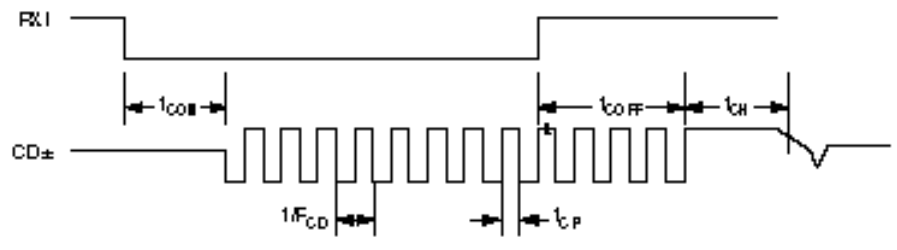


Figure 5. Collision Timing

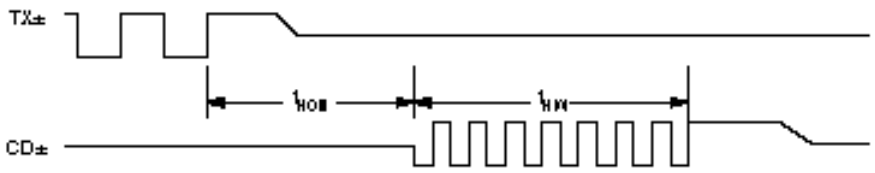


Figure 6. Heartbeat Timing

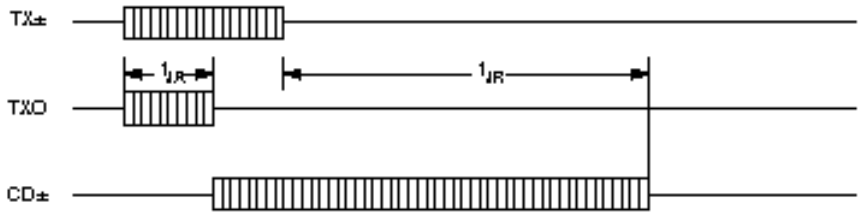


Figure 7. Jabber Timing

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Units
V_{EE}	Supply Voltage[2]	–12	V
V_{IN}	DC Input Voltage[2]	0 to –12	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_{SOLD}	Lead Soldering Temperature (10 sec.)	+300	°C
T_J	Recommended Max Junction Temperature[3]	+130	°C
θ_{JA}	Thermal Impedance (PDIP and PLCC Packages)	60	°C/W

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. 100% measured in production.
3. The junction temperature is calculated from the following expression:

   $T_J = T_A + \theta_{JA} [V_{EE} (0.075 + n \times 0.05/100) + 8 (V_{EE} – 2) / R]$

   where

   T_A = Ambient temperature in °C

   θ_{JA} = Thermal resistance of package.

   V_{EE} = Normal operating supply voltage in volts.

   n = Percentage transmitter duty cycle.

   R = Pull down resistors on the RX and CD pins in ohms

The PDIP package is specially designed to have a low θ_{JA} by directly connecting the four center pins 4, 5,12, and 13 to the die attachment area These tour pins then provide a conductive heat flow path from the die to the PCB where they should be soldered to a large area V_{EE} track. For the PLCC package, pins 5 to 11 and 19 to 25 should similarly be soldered to a large area V_{EE} track.

DC SPECIFICATIONS

V_{EE} = –9V ±5% T_A = 0 to +70°C unless otherwise specified [1, 2]. No external isolation diode on TXO.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power-on reset voltage. Transmitter disabled for $\|V_{EE}\| < \|V_{POR}\|$			–6.5		V
I_{EE}	Supply current non-transmitting			–80	–130	mA
	Supply current transmitting			–125	–180	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+2	+6	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +1.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +0.4	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V		250	500	µA
I_{IL}	HBE input LOW current	V_{HBE} = VEE		–500	–1000	µA
I_{TDC}	Transmit output DC current level [3]		–37		–45	mA
I_{TAC}	Transmit output AC current level [3]		±28		$\pm I_{TDC}$	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance [4]				–3.7	V
V_{CD}	Collision threshold [5]	Measured by applying DC voltage at RXI	–1450	–1530	–1580	mV
V_{OD}	Differential output voltage - non idle at RX± and CD± [6]		±600		±1200	mV
V_{OB}	Differential output voltage imbalance - idle at RX± and CD± [7]				±40	mV
V_{OC}	Output common mode voltage at RX± and CD±		–1.5	–2	–2.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC	–130	–250	–370	mV
V_{TS}	Transmitter squelch threshold	$(V_{TX+} – V_{TX–})$ peak	–175	–225	–300	mV
R_{RXI}	Shunt resistance at RXI non-transmitting		100			kΩ
C_{RXI}	Input Capacitance at RXI			2		pF
R_{TXO}	Shunt resistance at TXO transmitting			10		kΩ

Notes:

1. Currents flowing into device pins are positive All voltages are referenced to ground unless otherwise specified For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as $(V_{MAX} + V_{MIN}) / (2 \times 25)$ where V_{MAX} and V_{MIN} are the max and min voltages at TX0 with a 25 Ω load between TXO and GND. I_{TAC} is measured as $(V_{MAX} – V_{MIN}) / (2 \times 25)$.
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7 V.
5. Collision threshold for an AC signal is within 10% of V_{CD}.
6. Measured on secondary side of isolation transformer as shown in the connection diagram, Figure 1 The transformer has a 1:1 turn ratio with an inductance between 30 and 100 µH at 5 MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = –9V ±5% T_A = 0 to +70°C unless otherwise specified [1]. No external isolation diode on TXO.

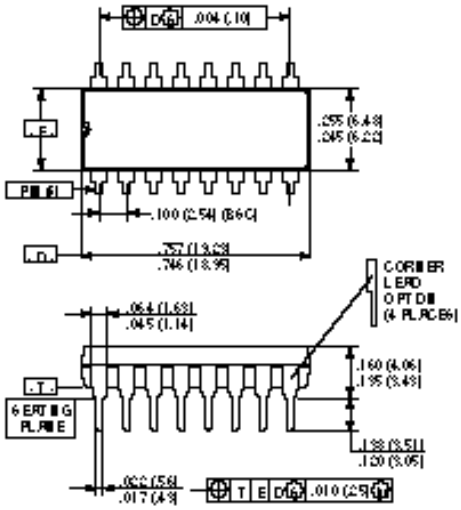
Symbol*	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{RON}(2)	Receiver start up delay RXI to RX± First received bit on RX±	V_{RXI} = –2V peak			5	bits
	First validly timed bit on RX±				t_{RON}+2	bits
t_{RD}(2)	Receiver prop. delay RXI to RXI±	V_{RXI} = –2V peak		35	50	ns
t_{RR}(2)	Differential output rise time on RX± and CD± [2,3]			5		ns
t_{RF}(2)	Differential output fall time on RX± and CD± [2,3]			5		ns
t_{OS}(4)	Differential output settling time on RX± and CD± to V_{OB} = 40 mV[2]			1		µs
t_{RJ}	Receiver and cable total jitter			±3		ns
t_{RHI}(4)	Receiver high to idle time	Measured to +210 mV	150		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	$t_{RF} – t_{RR}$		0.4		ns
t_{TST}(3)	Transmitter start-up delay TX± to TXO First transmitted bit on TXO	$V_{TX±}$ = –1V peak		1	2	bits
	First validly timed bit				t_{TST} + 2	bits
t_{TD}(3)	Transmitter prop delay TX± to TXO	$V_{TX±}$ = 1V peak		35	50	ns
t_{TR}(3)	Transmitter rise time 10% to 90%			25		ns
t_{TF}(3)	Transmitter fall time 10% to 90%			25		ns
t_{TM}	$t_{TF} – t_{TR}$ mismatch			±2		ns
t_{TS}	Transmitter added skew [4]			±2		ns
t_{TON}(3)	Transmitter turn on pulse width	$V_{TX±}$ = 1V peak	10		40	ns
t_{TOFF}(3)	Transmitter turn off pulse width	$V_{TX±}$ = 1V peak	150	250	340	ns
t_{CON}(5)	Collision turn on delay	0V to –2V step at RXI			13	bits
t_{COFF}(5)	Collision turn off delay	–2V to 0V step at RXI			16	bits
t_{CHI}(5)	Collision high to idle time	Measured to +210 mV	150		850	ns
f_{CD}(5)	Collision frequency		8.0	10	12.5	MHz
t_{CP}(5)	Collision signal pulse width		35		70	ns
t_{HON}(6)	Heartbeat turn on delay		0.6		1.6	µs
t_{HW}(6)	Heartbeat test duration		0.5		1.5	µs
t_{JA}(7)	Jabber activation delay measured from TX± to CD±		20		60	ms
t_{JR}(7)	Jabber reset delay measured from TX± to CD±		250		750	ms

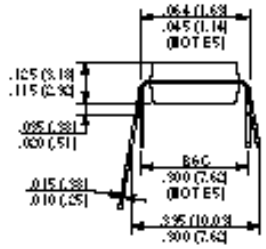
*** Numbers in parentheses indicate figure reference.**

Notes:

1. All typicals are for V_{EE} = –9V and T_A=27°C
2. Measured on secondary side of isolation transformer as shown in the connection diagram, Figure 1. The transformer has a 1:1 turn ratio with an inductance between 30 and 100 µH at 5 MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225 mV to +225 mV, or +225 mV to –225 mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

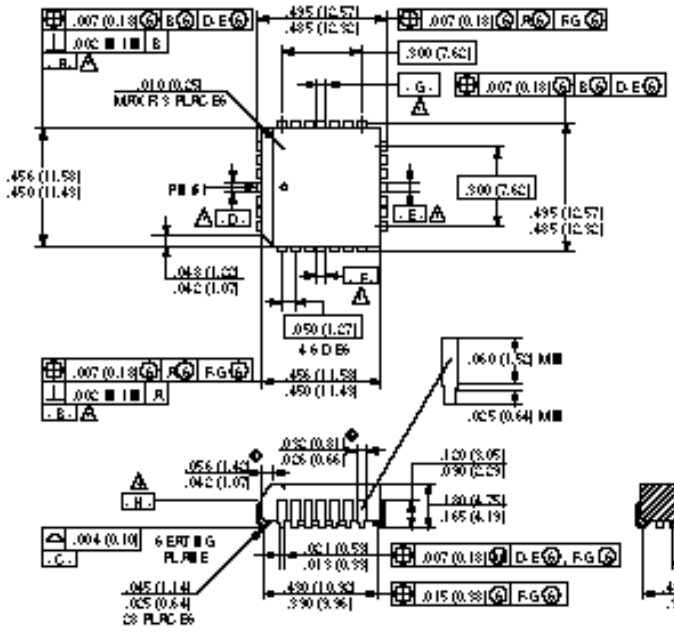
16- PIN PLASTIC DUAL IN- LINE

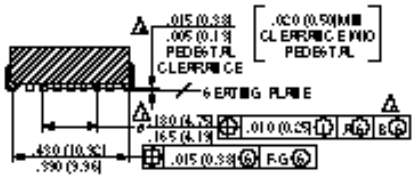




NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AR for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (Issue B, 7/85).
3. Dimensions and tolerancing per ANSI Y14.5M 1982.
4. "T", "D", and "E" are reference datums on the molded body, and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm).
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

28- PIN PLCC





NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AB.
2. Controlling dimension: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M 1982.
4. Datum plane -H- located at the top of mold parting line and coincident with top of lead where lead exits plastic body.
5. Location to datum -A- and -B- to be determined at plane -H-. These datum do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum D-E and F-G are determined where these center leads exit from the body, at plane -H-.
7. Pin numbers continue counterclockwise to pin #28 (top view).
8. Fujitsu order code for product packaged PLCC is the suffix "PD".
9. Applicable to packages with pedestal only.