DS06-8010-1E

FUJITSU

DATA SHEET

ASSP
IF Band
PLL Frequency Synthesizer
MB15S00 Series

■ DESCRIPTION

The Fujitsu MB15S series is an exclusive Intermediate Frequency (IF) band Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. It can operate maximum at 300MHz.

The reference divider and comparison divider have fixed divide ratios, so that it is not required to set the divide ratios by a µcontroller externally. Because the dividers are designed by means of **MASK ROM** method, a customer can chose them optionally. SOP and **SSOP 8-pin** plastic packages are available.

All of the above features help a system designer for **easier** as well as **compact** layout work.

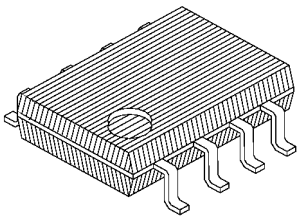
It operates with a supply voltage of 3.0V typ. and dissipates 3.5 mA typ. of current realized through the use of Fujitsu's Bi-CMOS technology.

■ FEATURES

- Operating frequency : 300MHz max.
- Low power supply current: I_{CC} (total) = 3.5 mA typ. (V_{CC} = 3V)
- Pulse swallow function;
  300MHz Prescaler: 16/17 or 32/33
- MASK ROM optional the comparison and reference dividers:
  - Main counter ; 5 to 4,095
  - Swallow counter ; 0 to 31
  - Reference counter ; 5 to 4,095
- Charge pump options:
  - Analog cellular phones ; Low sensitivity charge pump for direct modulation.
  - Digital cellular phones ; Super charger circuit for High speed tuning.
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Wide operating temperature: Ta = –40 to 85°C
- Plastic 8-pin SOP and 8-pin SSOP packages

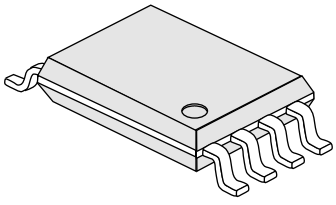
■ PACKAGES

8-pin, Plastic SOP



(FPT-8P-M01)

8-pin, Plastic SSOP



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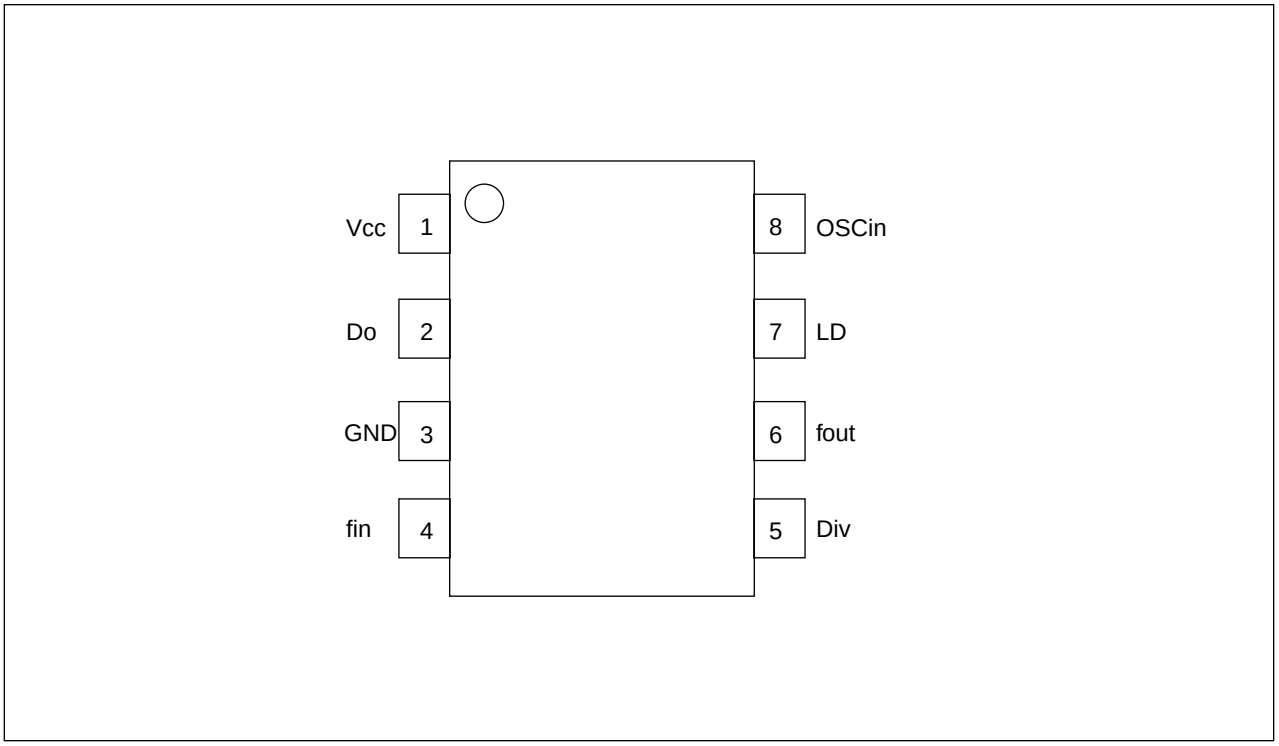
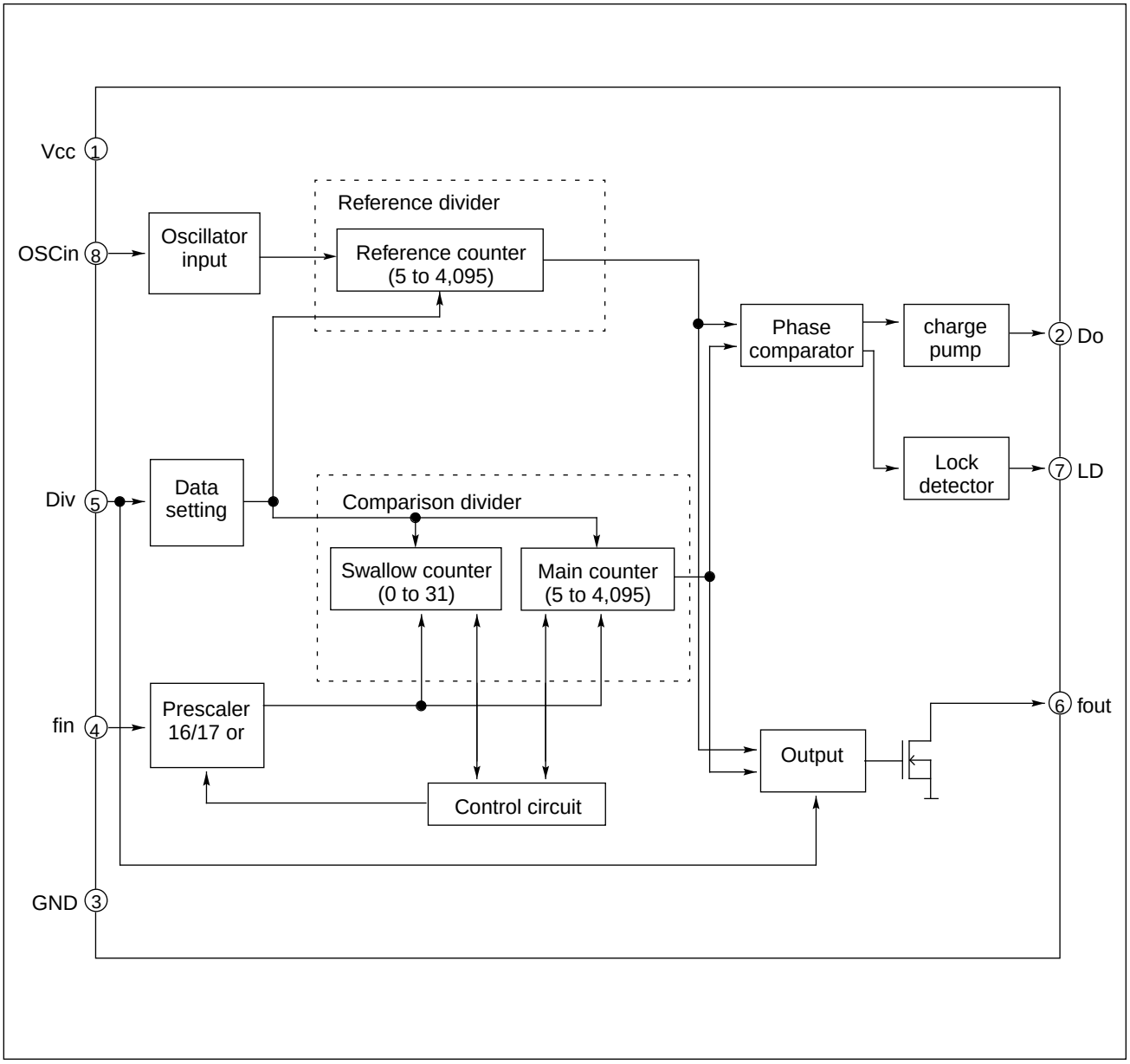
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	Description
1	V_{CC}	Power supply voltage input.
2	Do	Charge pump output.
3	GND	Ground.
4	fin	Prescaler input. Connection should be with AC coupling.
5	Div	Divide ratio switching input. Two kinds of divide ratios are selectable by Div input ”H” or ”L”.
6	fout	Test purpose output. This pin is an open drain output so that should be left open usually.
7	LD	Lock detector output.
8	OSCin	Reference counter input. Connection should be with AC coupling.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.5 to +5.0	V
Inputt voltage	V_I	–0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output current	I_{OUT}	0 to 5	mA
Storage tempareture	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_{IN}	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply current	I_{CC}	PLL is locked. Vcc = 3.0V, Ta = 25°C	–	3.5	5.0	mA
Operating frequency	fin	AC coupling by 1000pF capacitor	50	–	300	MHz
Oscillator input frequency	fosc	AC coupling by 1000pF capacitor	–	12	23	MHz
Input sensitivity	Vin	AC coupling by 1000pF capacitor	–10	–	+2	dBm
Oscillator input sensivity	OSCin	AC coupling by 1000pF capacitor	0.5	–	–	Vpp
Input voltage (Div)	V_{IH}		$V_{CC} \times 0.7$	–	–	V
	V_{IL}		–	–	$V_{CC} \times 0.3$	V
Input current (Div)	I_{IH}		–	–	1.0	µA
	I_{IL}		–1.0	–	–	µA
Input current (OSCin)	I_{OSC}		–100		100	µA
Output voltage	V_{OH}	V_{CC} = 3.0V	2.6	–	–	V
	V_{OL}	V_{CC} = 3.0V	–	–	0.4	V
High impedance cut off current (Do)	I_{OFF}	$VD_O \leq 3.3V$	–	–	1.1	µA

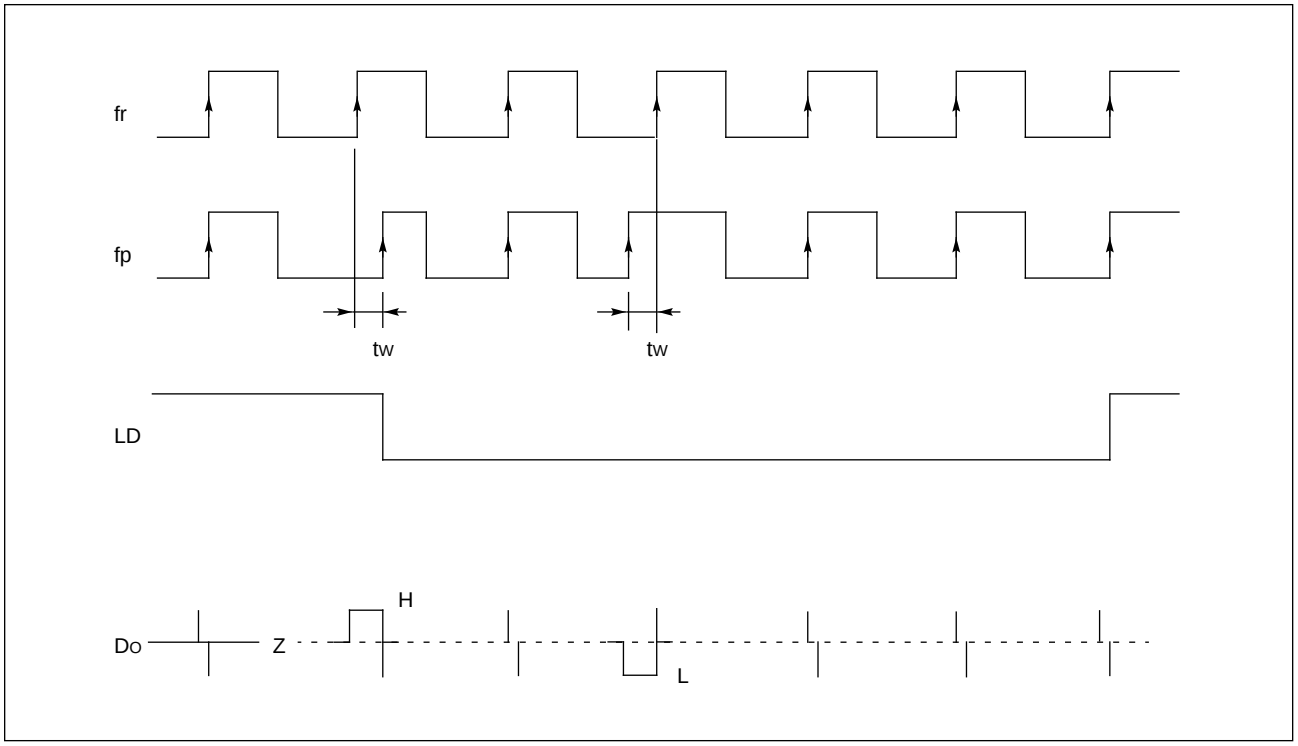
■ FUNCTIONAL DESCRIPTIONS

Divide ratios of the internal counters can be set optionally according to customer requirements. Two different frequencies can be selected by Div input "H" or "L".
The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO: up to 300MHz)
P: Preset divide ratio of dual modulus prescaler (16/17 or 32/33)
N: Divide ratio of the main counter (5 to 4,095)
A: Divide ratio of the swallow counter (0 to 31)
f_{OSC}: Reference oscillation frequency (up to 23MHz)
R: Divide ratio of the reference counter (5 to 4,095)

■ PHASE DETECTOR TIME CHART

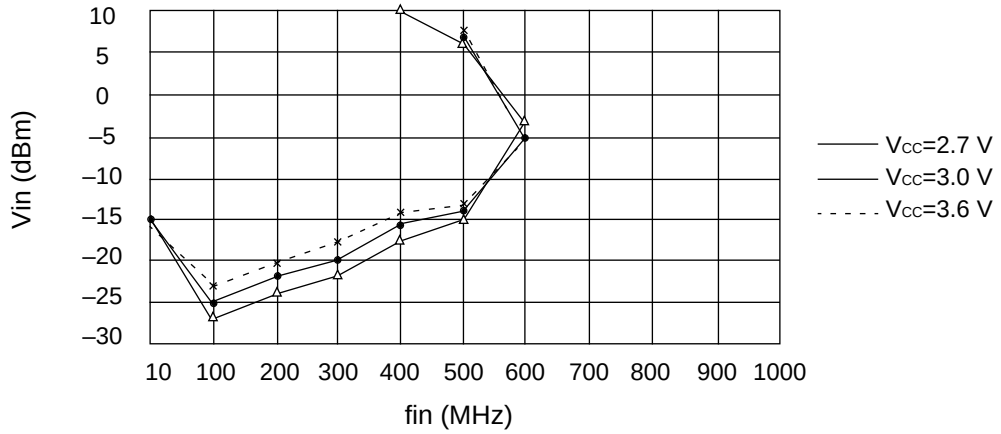


Note: • Phase defference detection range = –2π to + 2π
• Spikes on Do pulse during locking state are output to prevent dead zone.
• LD output becomes low when phase difference is tw or more.
• LD output becomes high when phase difference is tw or less and continues to be so for three cycles or more.
• tw depends on OSCin input frequency.
(e.g. tW635ns to 1250ns when foscin = 12.8 MHz)

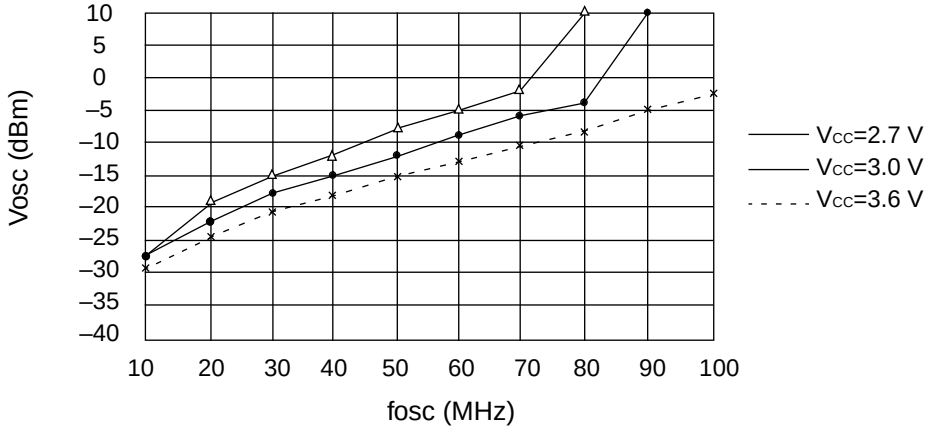
■ TYPICAL CHARACTERISTICS

Prescaler Input Sensitivity Characteristics

• fin Pin



• OSCin Pin



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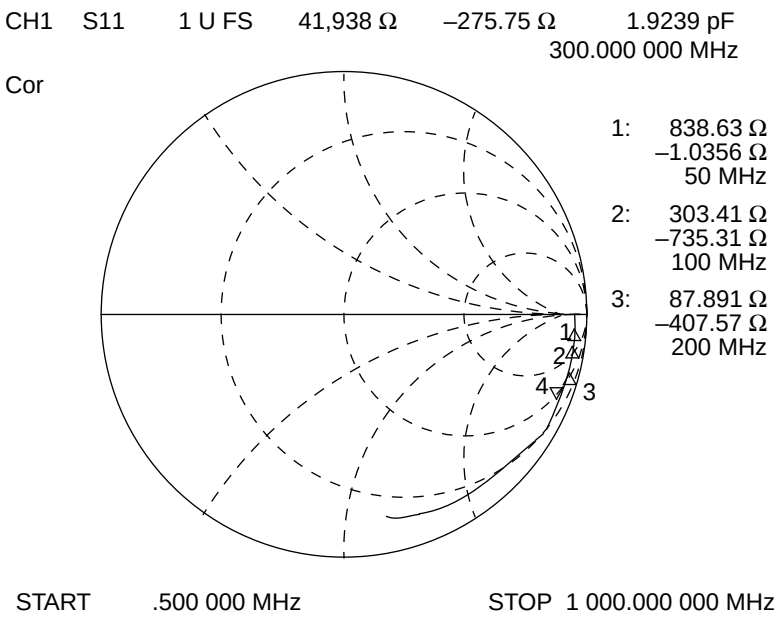
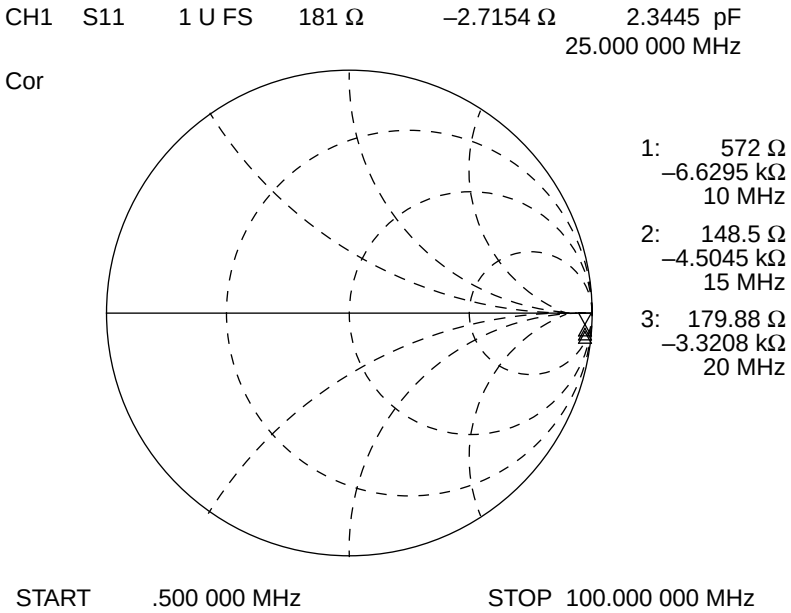
Input/Output Impedance Characteristics

• fin Pin



• OSCin Pin



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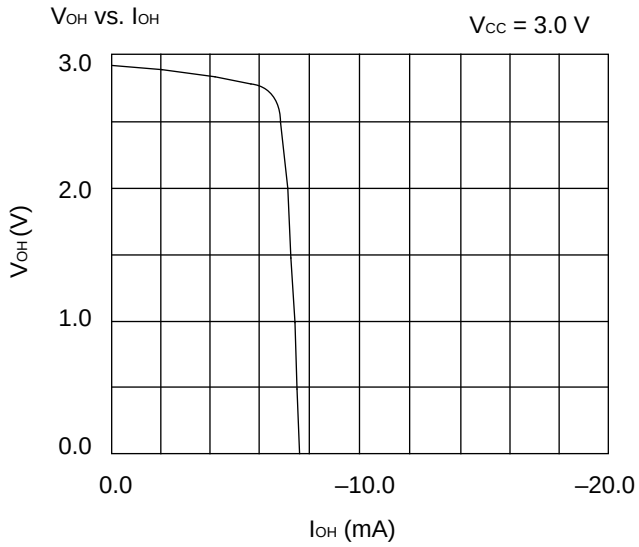
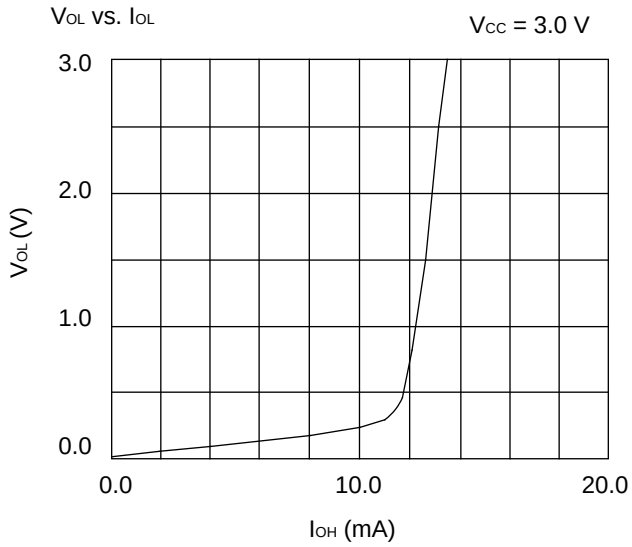
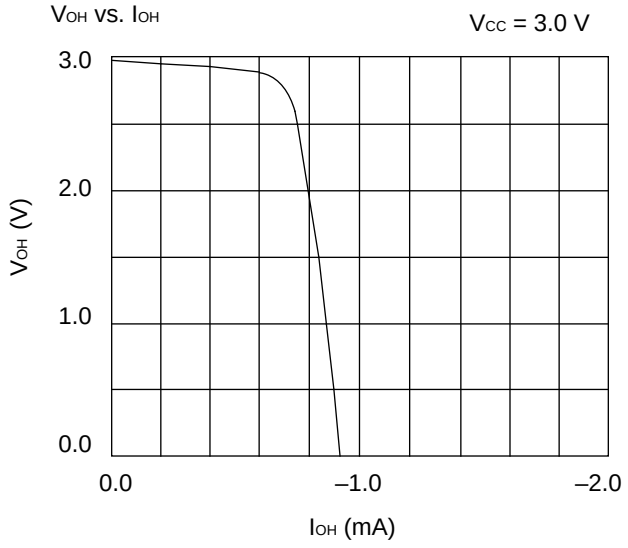
Charge Pump Characteristics

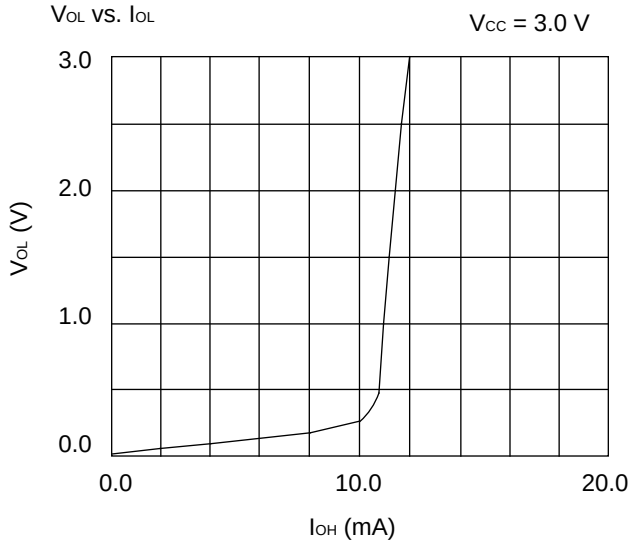
- **Super charger**





- **Low sensitivity type**





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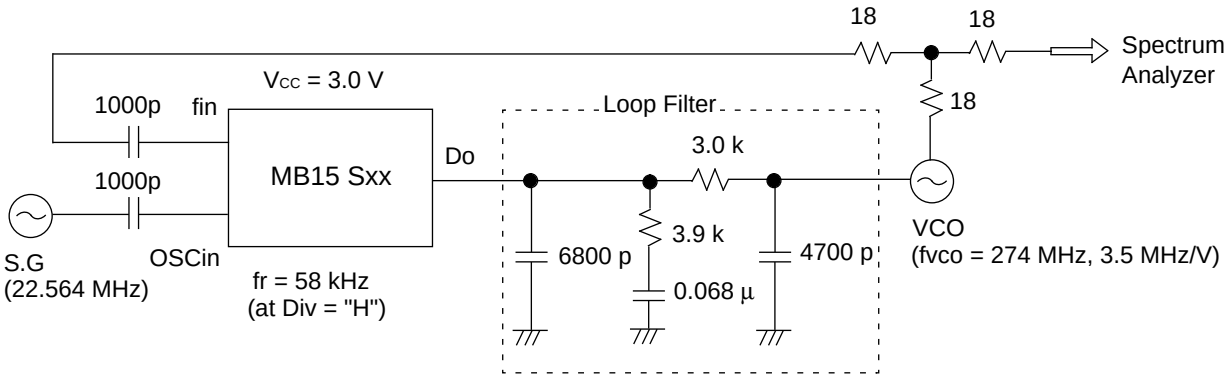
PLL Loop Characteristics (Super Charger)

Parameter	Results
Hoppint time +/– 1 kHz Unlock → Lock Power on → Lock	1.80 ms < 4.50 ms
Suprious Δ f = 58 kHz	–87.0 dBc
Phase noise C/N peak in BW	–82.0 dBc/Hz
V_{CC} (V)	3.0V
VCO	Discrete VCO (Kv = 3.5 MHz/V) Lock frequency = 274.0 MHz (fr = 58 kHz)

Measurement Circuit



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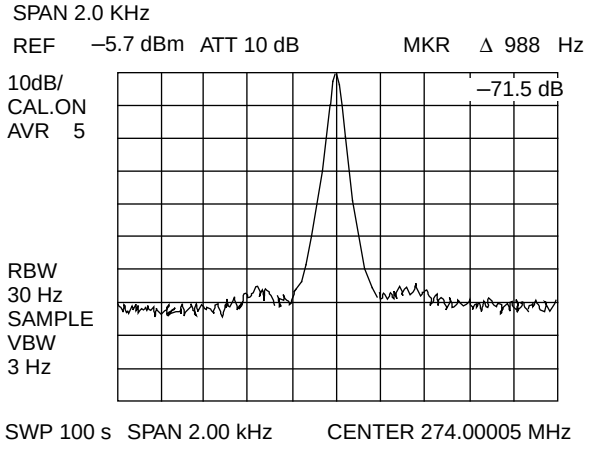
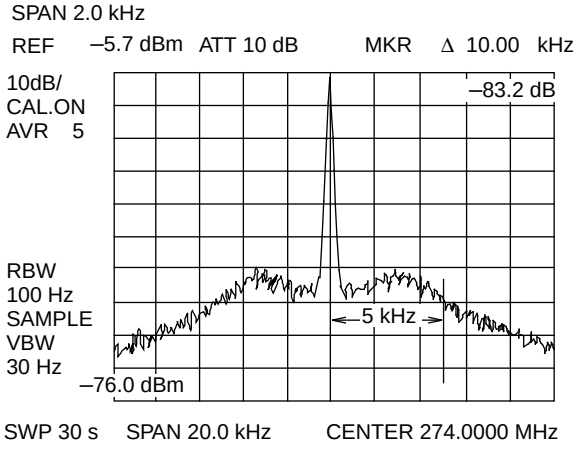
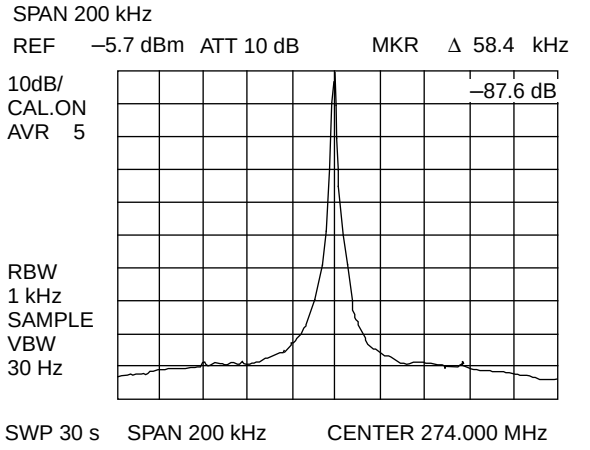
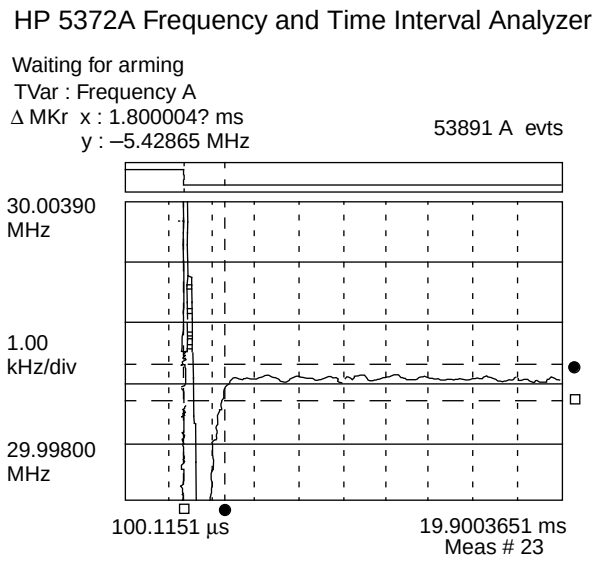
PLL Phase Noise/Suprious







PLL Lock-up Time (unlock→ lock)



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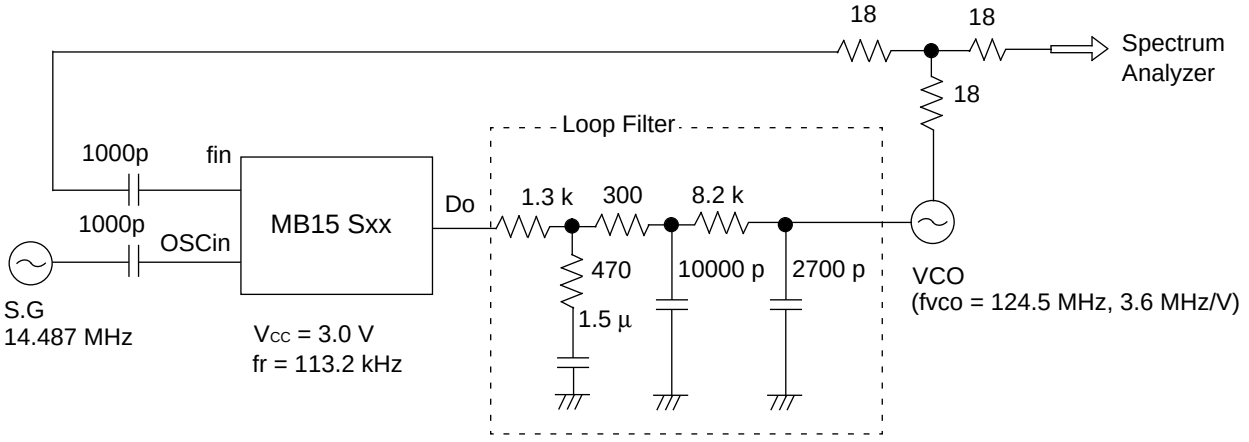
PLL Loop Characteristics (Low Sensitivity Type)

Parameter	Results
Hoppint time +/– 1 kHz Power on → Lock	8.6 ms
Suprious (Δ f = 113.2 kHz)	–86.7 dBc
Phase noise (Δ f = 1 kHz)	–79.0 dBc/Hz
V_{CC} (V)	3.0 v
VCO	Discrete VCO (Kv = 3.6 MHz/V) Lock frequency = 124.5 MHz (fr = 113.2 kHz)

Measurement Circuit



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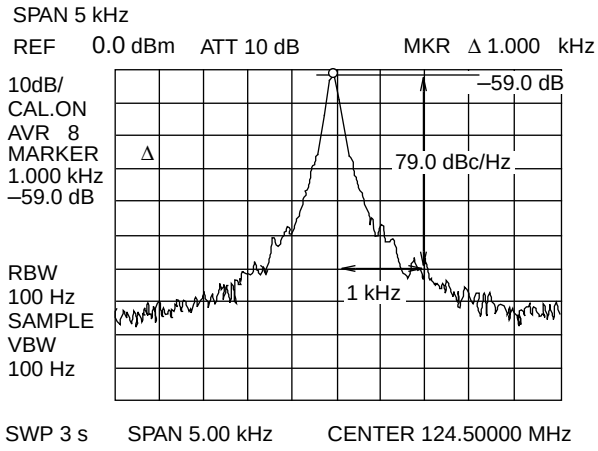
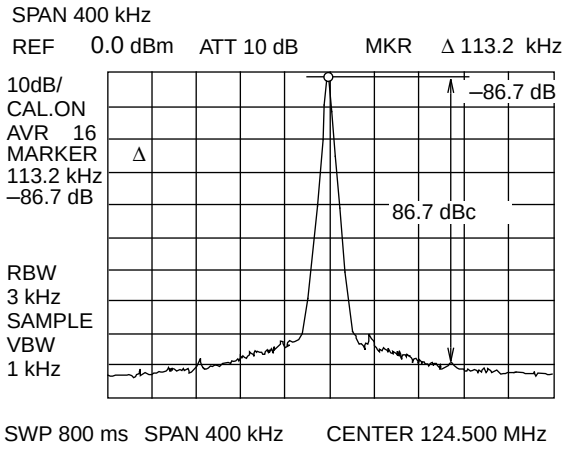
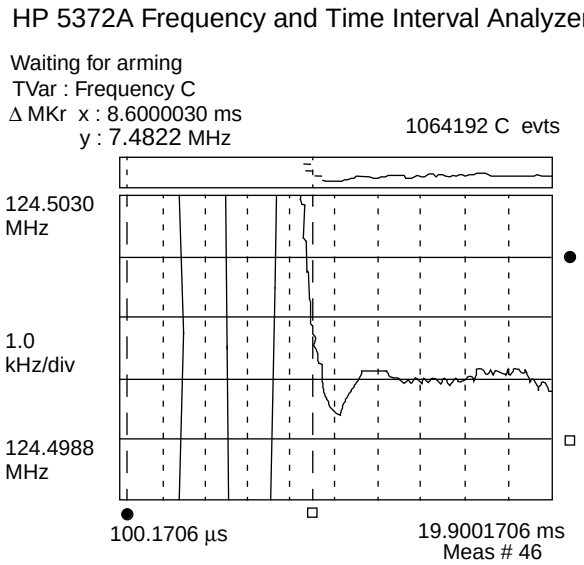
PLL Phase Noise/Suprious

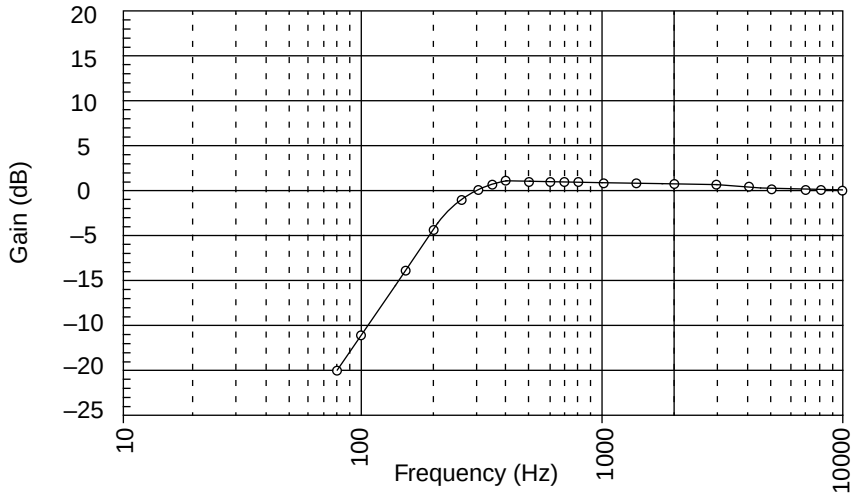




PLL Lock-up Time

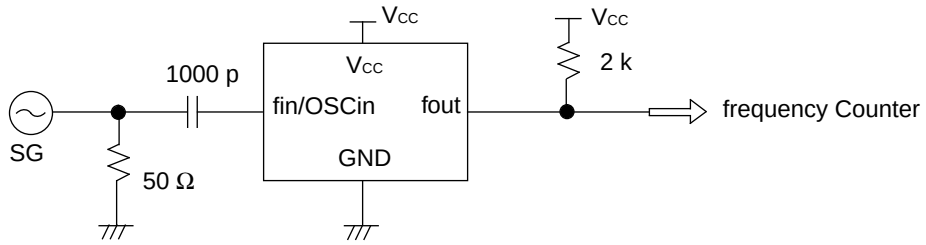


Modulation Characteristics



■ TEST CIRCUIT EXAMPLE (fin/OSCin Input Sensitivity Measurement)

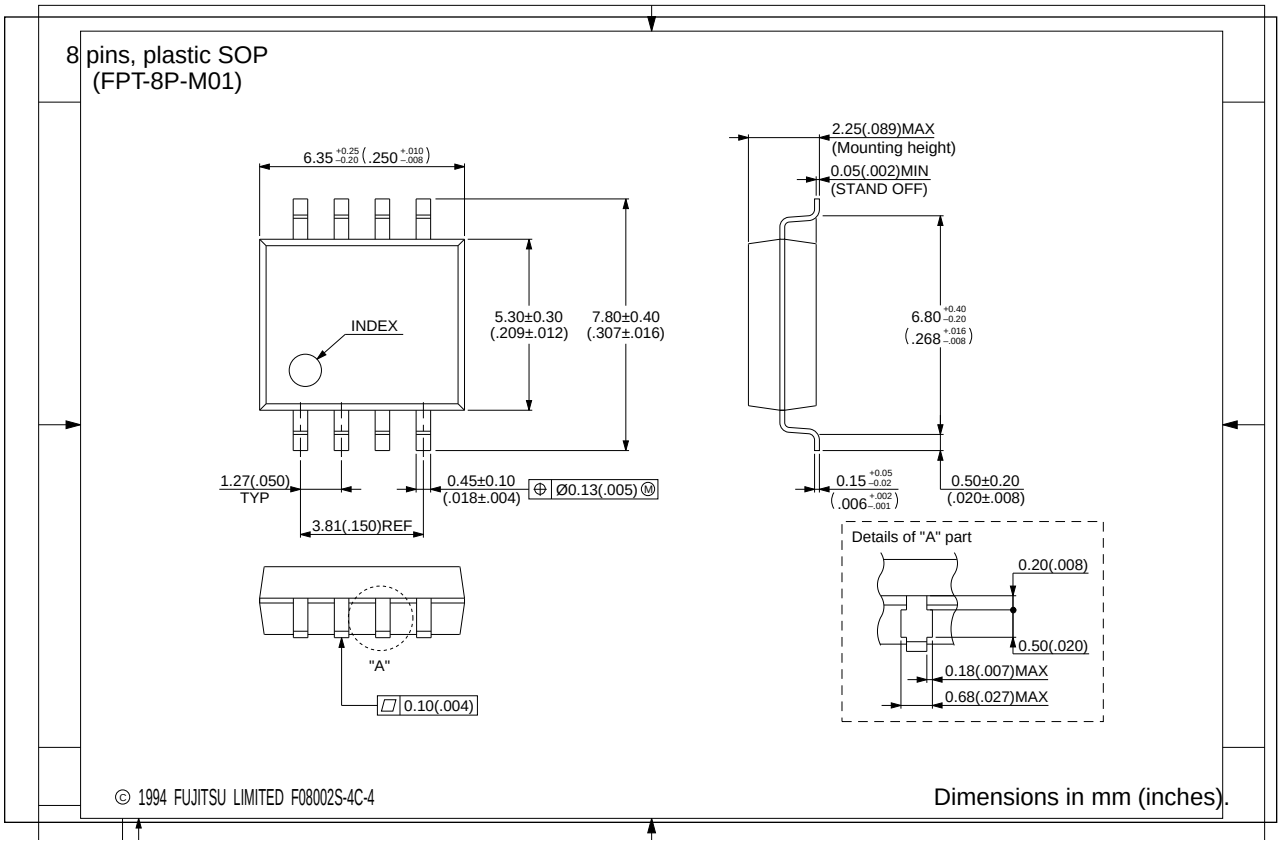
Measurement Circuit



■ CUSTOMER REQUESTING SPECIFICATIONS

Prameter			Option	Requirements
fvco		VCO output frequency	~ 300MHz fvco = {(P x N) + A} x fr	
fosc		Reference oscillation frequency	~ 23MHz fosc = R x fr	
Com-parison divider	N	Main counter divide ratio	5 to 4,095	
	A	Swallow counter divide ratio	0 to 31	
Refer-ence divider	R	Reference counter divide ratio	5 to 4,095	
	fr	Reference frequency	Option	
P		Prescaler divide ratio	16/17 or 32/33	
Charge pump type			Low sensitivity type or super charger	
Package			SSOP 8-pin or SOP 8-pin	
ES request date/qty.			Typically 6 weeks from spec. fix to the first ES.	
CS request date/qty.			–	
MP request date/qty.			–	
Target price			–	
Customer comments				

■ PACKAGE DIMENSIONS



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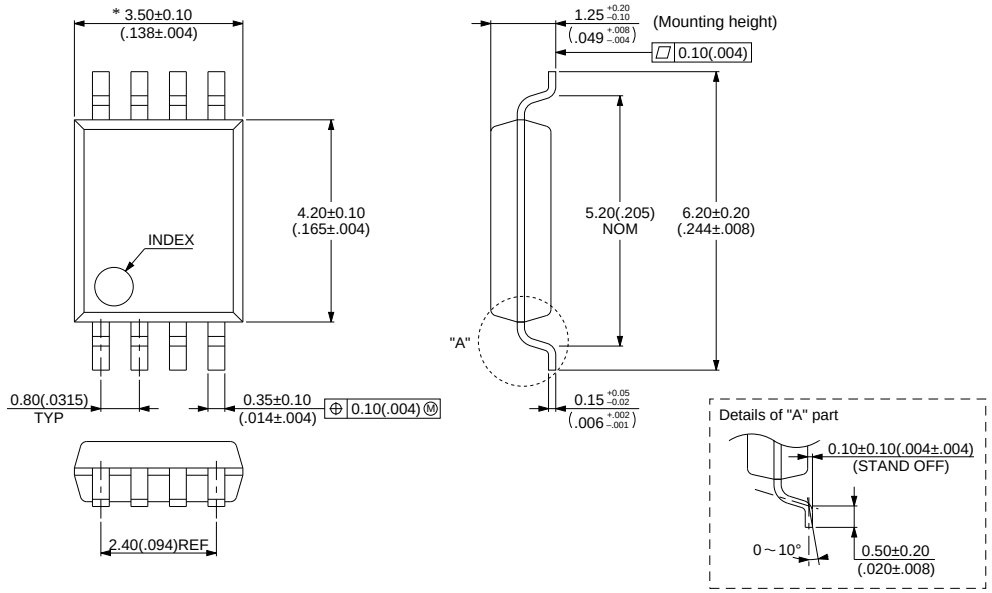
8 pin, plastic SSOP
(FPT-8P-M03)

* : This dimension does not include resin protrusion.



Dimensions in mm (inches).