DS05–11204–1E

FUJITSU

DATA SHEET

MEMORY

CMOS 4M × 72 Fast Page Mode DRAM Module

MB85317A-60/-70

CMOS 4M x 72 Bit Fast Page Mode DRAM Module

■DESCRIPTION

The Fujitsu MB85317A is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eighteen MB8116400A devices. The MB85317A is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85317A are the same as the MB8116400A which features fast page mode operation. For ease of memory expansion, the MB85317A is offered in an 168-pad Dual In-line Memory Module package (DIMM).

■ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	50	mA
Power Dissipation	P_D	20	W
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

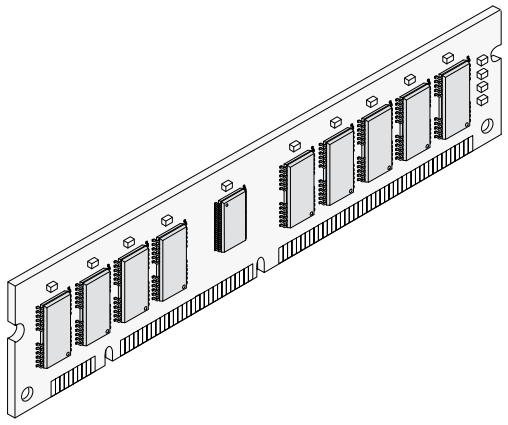
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PRODUCT LINE & FEATURES

Parameter		MB85317A-60	MB85317A-70
$\overline{RAS}$ Access Time		60ns max.	70ns max.
Random Cycle Time		110ns min.	130ns min.
Address Access Time		35ns max.	40ns max.
$\overline{CAS}$ Access Time		20ns max.	22ns max.
Fast Page Mode Cycle Time		40ns min.	45ns min.
Power Dissipation	Operating Mode	9020mW max.	7920mW max.
	Standby Mode	550mW max.	550mW max.

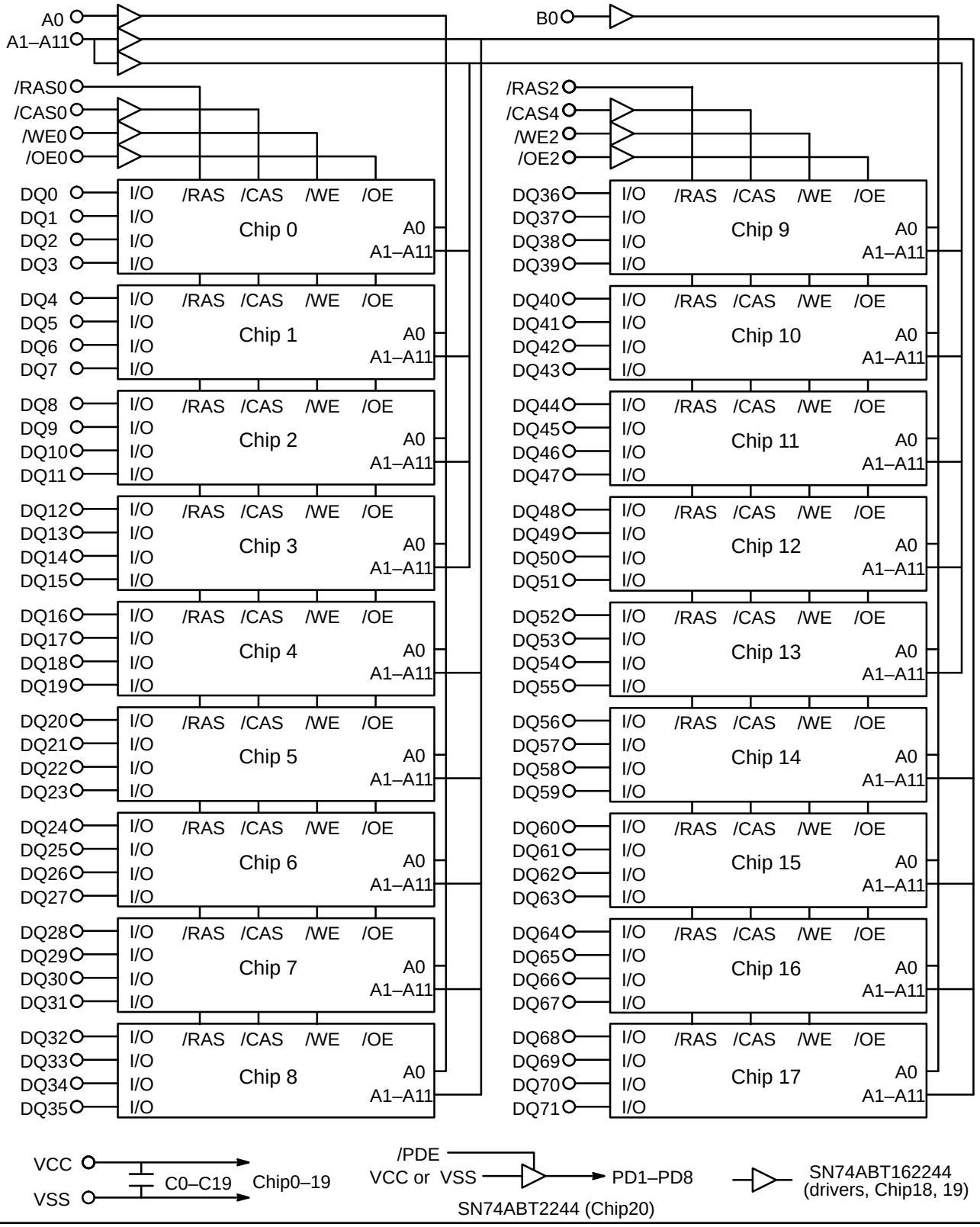
- Conformed to 8-Byte DIMM JEDEC standard
- Organization : 4,194,304 words x 72 bits (ECC)
- Module Size : 1.00” (height) x 5.25” (length) x 0.157” (thick)
- Memory : MB8116400A (4Mx4, 4K ref.), 18 pcs
- TI’s Input Buffers, 2pcs
- TI’s Input Driver for Buffered PD, 1pc
- Decoupling Capacitors, 20pcs
- 5.0V ± 10% Supply Voltage
- 4,096 Refresh Cycles / 65.6ms
- Fast Page operation
- $\overline{RAS}$ Only Refresh / $\overline{CAS}$-before-$\overline{RAS}$ Refresh
- Package and Ordering Information:
  168-pad DIMM, order as
  MB85317A-xxPTPBK (PTPBK = Gold Pad)

PACKAGE



MDS-168P-P04

Fig.1 – BLOCK DIAGRAM



PIN ASSIGNMENTS

Pin No.	MB85317A	Pin No.	MB85317A	Pin No.	MB85317A	Pin No.	MB85317A
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	/OE2	86	DQ36	128	NC
3	DQ1	45	/RAS2	87	DQ37	129	NC
4	DQ2	46	/CAS4	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	VCC	48	/WE2	90	VCC	132	/PDE
7	DQ4	49	VCC	91	DQ40	133	VCC
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	VCC	101	DQ49	143	VCC
18	VCC	60	DQ24	102	VCC	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	VSS	65	DQ25	107	VSS	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	VCC	68	VSS	110	VCC	152	VSS
27	/WE0	69	DQ28	111	NC	153	DQ64
28	/CAS0	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	/RAS0	72	DQ31	114	NC	156	DQ67
31	/OE0	73	VCC	115	NC	157	VCC
32	VSS	74	DQ32	116	VSS	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	VCC	82	PD7	124	VCC	166	PD8
41	NC	83	ID0	125	NC	167	ID1
42	NC	84	VCC	126	B0	168	VCC

PIN DESCRIPTIONS

Symbol	Function	Input / Output	Pin Count
A0 to A11, B0	Address Input	Input	13
/RAS0 and /RAS2	Row Address Strobe	Input	2
/CAS0 and /CAS4	Column Address Strobe	Input	2
/WE0 and /WE2	Write Enable	Input	2
/OE0 and /OE2	Output Enable	Input	2
DQ0 to DQ71	Data-input / Data-output	Input / Output	72
PD1 to PD8	Presence Detect	Output	8
ID0 and ID1	ID bit	Output	2
/PDE	Presence Detect Enable	Input	1
V_{CC}	Power Supply	–	16
V_{SS}	Ground	–	16
NC	No Connection	–	32

PRESENCE DETECT(PD) / ID DEFINITION

Symbol	MB85317A-60	MB85317A-70	Description of PD / ID
PD1	H	H	MODULE DENSITY, DRAM ORGANIZATION AND ADDRESSING; Module Density: 32MB, Number of Bank: 1 Bank Module Configuration: 4M x72 Mounted DRAM Configuration: 4M x4 DRAM Address (Row / Column): 12 / 11
PD2	H	H	
PD3	L	L	
PD4	H	H	
PD5	L	L	EDO DETECTION; Fast Page Mode : PD5 = L
PD6	H	L	MODULE SPEED; 60ns : PD6 = H, PD7 = H 70ns : PD6 = L, PD7 = H
PD7	H	H	
PD8	L	L	ECC / PARITY DETECTION; ECC : PD8 = L
ID0	L	L	MODULE TYPE; x72 ECC : ID0 = L
ID1	L	L	REFRESH MODE; Normal Refresh : ID1 = L

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance, (Address)	C_{IN1}		20	pF
Input Capacitance, (/RAS)	C_{IN2}		80	pF
Input Capacitance, (/CAS, /WE, /OE)	C_{IN3}		20	pF
I/O Capacitance, (DQ)	C_{DQ}		20	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}		0		V
Input High Voltage, all inputs	V_{IH}	2.4		6.0	V
Input Low Voltage, all inputs *	V_{IL}	–0.3		0.8	V
Ambient Temperature	T_A	0		70	°C

Note: * Undershoots of up to –1.5volts with a pulse width not exceeding 10ns are acceptable.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Test Condition	Symbol	Min	Max	Unit
Output High Voltage *1		I_{OH} = –5mA	V_{OH}	2.4		V
Output Low Voltage *1		I_{OL} = 4.2mA	V_{OL}		0.4	V
Input Leakage Current	$\overline{RAS}$	0V ≤ V_{IN} ≤ 5.5V, 4.5V ≤ V_{CC} ≤ 5.5V, V_{SS} = 0V, all other pins not under test = 0V	$I_{I(L)}$	–50	50	µA
	Others			–10	10	
Output Leakage Current		0V ≤ V_{OUT} ≤ 5.5V, 4.5V ≤ V_{CC} ≤ 5.5V, Data out disabled	$I_{O(L)}$	–10	10	µA
Operating Current *2 (Average power supply current)	MB85317A-60	$\overline{RAS}$ & $\overline{CAS}$ cycling, t_{RC} = min.	I_{CC1}		1640	mA
	MB85317A-70				1440	
Standby Current *2 (Power supply current)	TTL Level	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{PDE}$ = V_{IH}	I_{CC2}		100	mA
	CMOS Level	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{PDE}$ ≥ V_{CC} –0.2V			80	
Refresh Current #1 *2 (Average power supply current)	MB85317A-60	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, t_{RC} = min.	I_{CC3}		1640	mA
	MB85317A-70				1440	
Fast Page Mode Current *2	MB85317A-60	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{PC} = min.	I_{CC4}		1640	mA
	MB85317A-70				1440	
Refresh Current #2 *2 (Average power supply current)	MB85317A-60	$\overline{RAS}$ = cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min.	I_{CC5}		1640	mA
	MB85317A-70				1440	

Notes: *1 Referenced to V_{SS}.
*2 I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > –0.3V.
I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC4} is specified at one time of address change during one Page cycle.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85317A-60		MB85317A-70		Unit	Notes
			Min	Max	Min	Max		
1	Time Between Refresh	tREF	—	65.6	—	65.6	ms	
2	Random Read/Write Cycle Time	tRC	110	—	130	—	ns	
3	Read-Modify-Write Cycle Time	tRWC	150	—	174	—	ns	
4	Access Time from $\overline{RAS}$	tRAC	—	60	—	70	ns	**4, 7**
5	Access Time from $\overline{CAS}$	tCAC	—	20	—	22	ns	**5, 7**
6	Column Address Access Time	tAA	—	35	—	40	ns	**6, 7**
7	Output Hold Time	tOH	5	—	5	—	ns	
8	Output Buffer Turn On Delay Time	tON	2	—	2	—	ns	
9	Output Buffer Turn Off Delay Time	tOFF	—	20	—	22	ns	**8**
10	Transition Time	tT	2	16	2	16	ns	
11	$\overline{RAS}$ Precharge Time	tRP	40	—	50	—	ns	
12	$\overline{RAS}$ Pulse Width	tRAS	60	100000	70	100000	ns	
13	$\overline{RAS}$ Hold Time	tRSH	20	—	22	—	ns	
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	ns	
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	18	40	18	48	ns	**9, 10**
16	$\overline{CAS}$ Pulse Width	tCAS	15	—	17	—	ns	
17	$\overline{CAS}$ Hold Time	tCSH	58	—	68	—	ns	
18	$\overline{CAS}$ Precharge Time (C–B–R Refresh)	tCPN	10	—	10	—	ns	**17**
19	Row Address Setup Time	tASR	5	—	5	—	ns	
20	Row Address Hold Time	tRAH	8	—	8	—	ns	
21	Column Address Setup Time	tASC	0	—	0	—	ns	
22	Column Address Hold Time	tCAH	15	—	15	—	ns	
23	Column Address Hold Time from $\overline{RAS}$	tAR	33	—	33	—	ns	
24	$\overline{RAS}$ to Column Address Delay Time	tRAD	13	25	13	30	ns	**11**
25	Column Address to $\overline{RAS}$ Lead Time	tRAL	35	—	40	—	ns	
26	Column Address to $\overline{CAS}$ Lead Time	tCAL	30	—	35	—	ns	
27	Read Command Setup Time	tRCS	0	—	0	—	ns	
28	Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	–2	—	–2	—	ns	**12**
29	Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	—	0	—	ns	**12**
30	Write Command Setup Time	tWCS	0	—	0	—	ns	**13, 18**
31	Write Command Hold Time	tWCH	15	—	15	—	ns	
32	Write Command Hold Time from $\overline{RAS}$	tWCR	33	—	33	—	ns	
33	$\overline{WE}$ Pulse Width	tWP	15	—	15	—	ns	
34	Write Command to $\overline{RAS}$ Lead Time	tRWL	20	—	22	—	ns	
35	Write Command to $\overline{CAS}$ Lead Time	tCWL	15	—	17	—	ns	
36	DIN Setup Time	tDS	–2	—	–2	—	ns	
37	DIN Hold Time	tDH	20	—	20	—	ns	

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85317A-60		MB85317A-70		Unit	Notes
			Min	Max	Min	Max		
38	Data Hold Time from $\overline{RAS}$	tDHR	35	—	35	—	ns	
39	$\overline{RAS}$ to $\overline{WE}$ Delay Time	tRWD	78	—	90	—	ns	**18**
40	$\overline{CAS}$ to $\overline{WE}$ Delay Time	tCWD	35	—	39	—	ns	**18**
41	Column Address to $\overline{WE}$ Delay Time	tAWD	50	—	57	—	ns	**18**
42	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	tRPC	3	—	3	—	ns	
43	$\overline{CAS}$ Setup Time (C–B–R Refresh)	tCSR	5	—	5	—	ns	
44	$\overline{CAS}$ Hold Time (C–B–R Refresh)	tCHR	8	—	10	—	ns	
45	$\overline{WE}$ Setup Time from $\overline{RAS}$	tWSR	5	—	5	—	ns	
46	$\overline{WE}$ Hold Time from $\overline{RAS}$	tWHR	8	—	8	—	ns	
47	Access Time from $\overline{OE}$	tOEA	—	20	—	22	ns	**7**
48	Output Buffer Turn Off Delay from $\overline{OE}$	tOEZ	—	20	—	22	ns	**8**
49	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data	tOEL	10	—	12	—	ns	
50	$\overline{WE}$ Hold Time Referenced to $\overline{WE}$	tOEH	5	—	5	—	ns	**14**
51	$\overline{OE}$ to Data in Delay Time	tOED	20	—	22	—	ns	
52	$\overline{CAS}$ to Data in Delay Time	tCDD	20	—	22	—	ns	
53	DIN to $\overline{CAS}$ Delay Time	tDZC	–2	—	–2	—	ns	**15**
54	DIN to $\overline{OE}$ Delay Time	tDZO	–2	—	–2	—	ns	**15**
55	Fast Page Mode $\overline{RAS}$ Pulse Width	tRASP	—	100000	—	100000	ns	
56	Fast Page Mode Read/Write Cycle Time	tPC	40	—	45	—	ns	
57	Fast Page Mode Read-Modify-Write Cycle Time	tPRWC	80	—	89	—	ns	
58	Access Time from $\overline{CAS}$ Precharge	tCPA	—	40	—	45	ns	**7, 16**
59	Fast Page Mode $\overline{CAS}$ Precharge Time	tCP	10	—	10	—	ns	
60	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	40	—	45	—	ns	
61	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	tCPWD	55	—	62	—	ns	**18**

Notes:

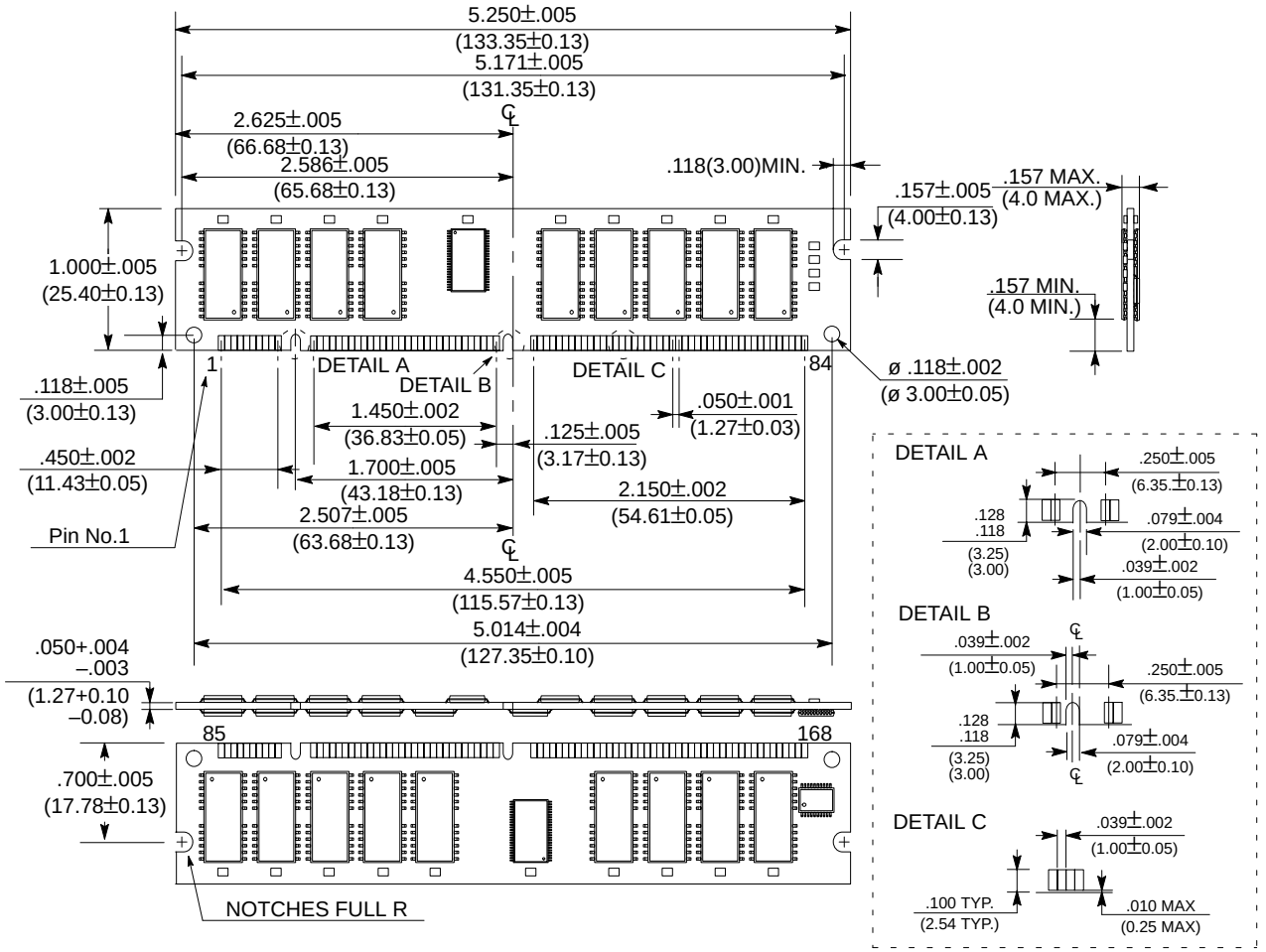
1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200µs is required after power–up followed by any eight $\overline{RAS}$–only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$–before–$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.
2. AC characteristics assume t_T = 5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measureing the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} – t_{CAC} – t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} – t_{CAC} – t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min).
11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
14. Assumes that $t_{WCS} < t_{WCS}$ (min).
15. Either t_{DZC} or t_{DZO} must be satisfied.
16. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} become long, t_{CPA} also become longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$-before- $\overline{RAS}$ refresh.
18. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min) , $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read- modify-write cycle and data from the selected cell will appear at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} specifications.

*Source: See MB8116400A Data Sheet for details on the electricals.

PACKAGE DIMENSIONS

(Suffix: PTPBK)

168-PAD PLASTIC DUAL IN-LINE TYPE MODULE
(CASE No.: MDS-168P-P04)



Dimensions in inches (millimeters)