January 1993
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FUJITSU

DATA SHEET

MB40168/MB40178

SINGLE CHIP 8–BIT A/D AND 9–BIT D/A CONVERTER

PRELIMINARY

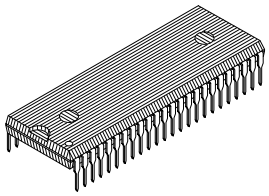
DESCRIPTION

The Fujitsu MB40168 and MB40178 are high speed, low power single chip A/D and D/A converters designed for video processing applications. The A/D converter has a resolution of 8 bits while the D/A converter has 9–bit resolution. They are fabricated in Fujitsu's advanced bipolar technology, and housed in a 48–pin plastic shrink DIP or 44–pin plastic QFP package.

FEATURES

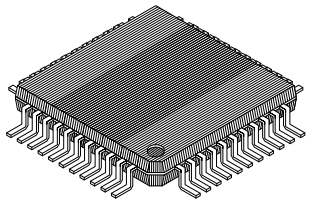
- Resolution — A/D: 8 bits; D/A: 9 bits
- Conversion Rate — A/D: Max. 20 MSPS; D/A: Max. 40 MSPS
- Linearity Error — A/D: Max. ± 0.3%; D/A: Max. ± 0.2%
- On–chip reference voltage generator (resistor divided method) and clamp circuit
- Analog Input Voltage — 3 to 5 V without clamp circuit; 0 to 3 V in 2 V_{P-P} clamp circuit
- Analog Output Voltage — 3 to 5 V
- Digital Input/Output Interface — TTL Levels
- Power Supply Voltage — + 5.0 V single power supply
- Power Dissipation — Typ. 350 mW
- Package Options — 48–pin Plastic Shrink DIP/ 44–pin Plastic QFP Package

MB40168–P–SH/
MB40178–P–SH



PLASTIC SHRINK DIP
(DIP–48P–M01)

MB40168–PF/
MB40178–PF



PLASTIC QFP
(FPT–44P–M01)

ABSOLUTE MAXIMUM RATINGS (see NOTE.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA}, V_{CCD}	–0.5 to 7.0	V
Analog Input Voltage	V_{INA}	–0.5 to V_{CC} + 0.5	V
Digital Input Voltage	V_{IND}	–0.5 to 7.0	V
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Figure 1. Pin Assignment
MB40168–PSH

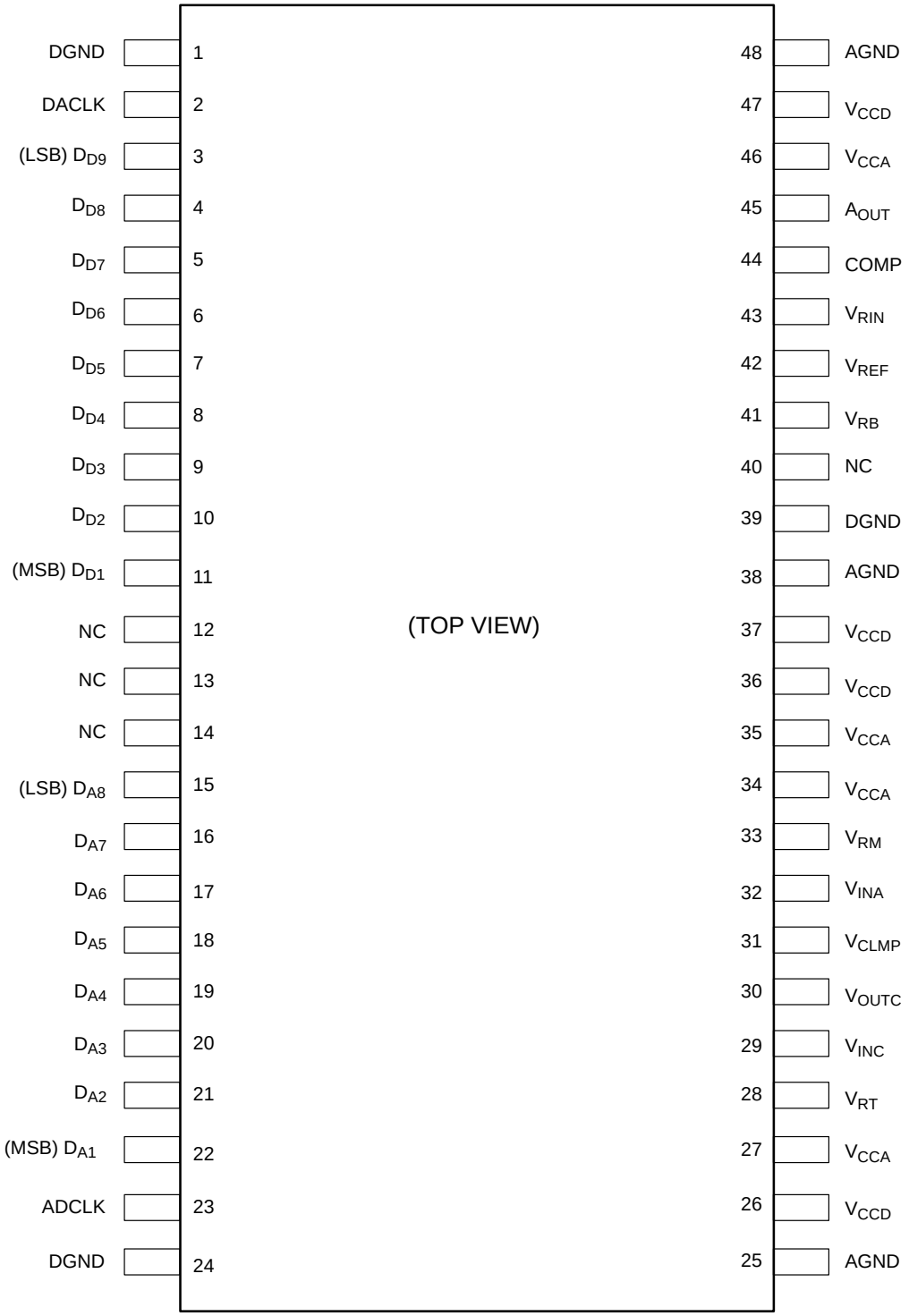


Figure 1. Pin Assignment (Continued)
MB40168–PF

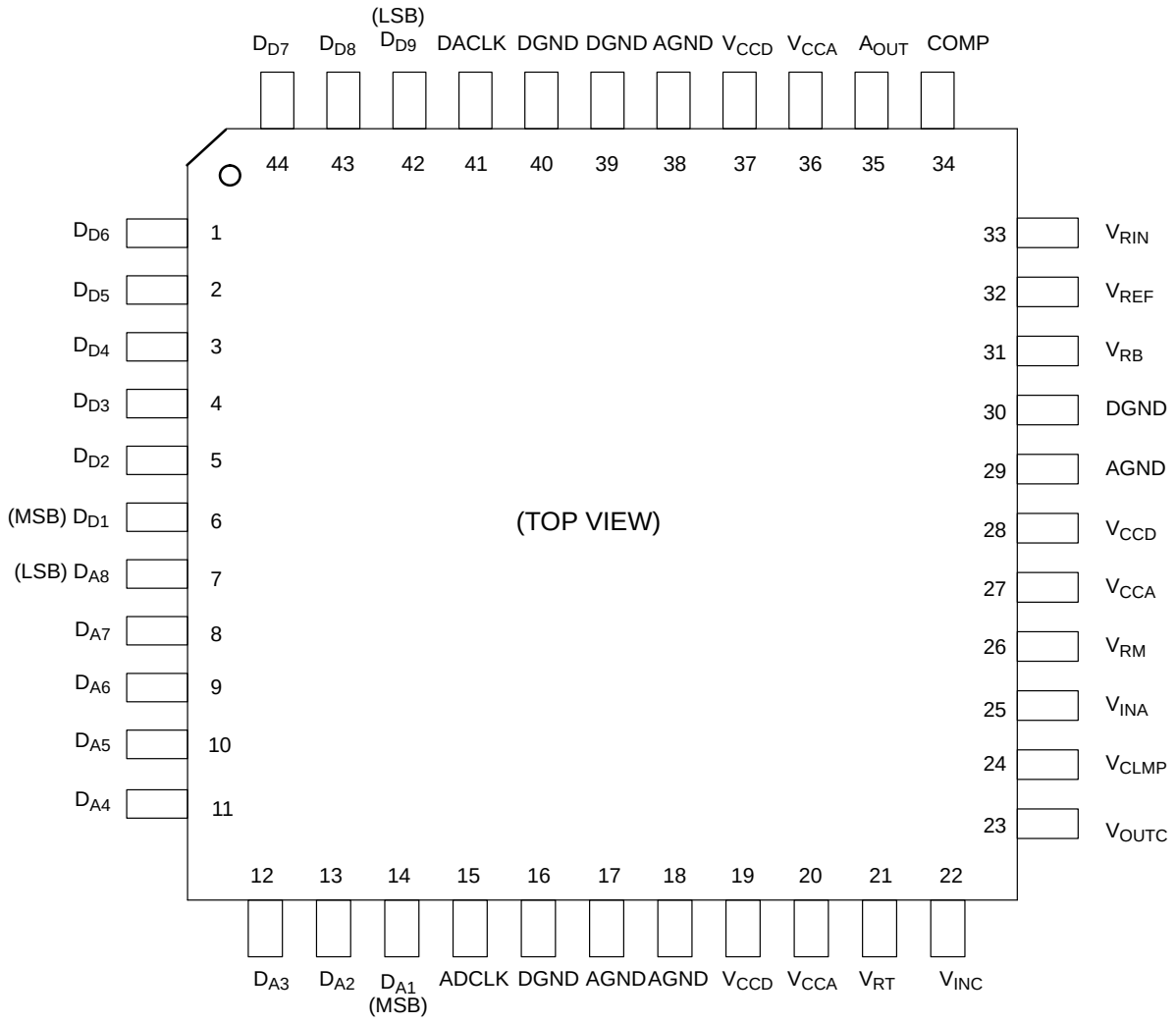


Figure 1. Pin Assignment (Continued)
MB40178–PSH

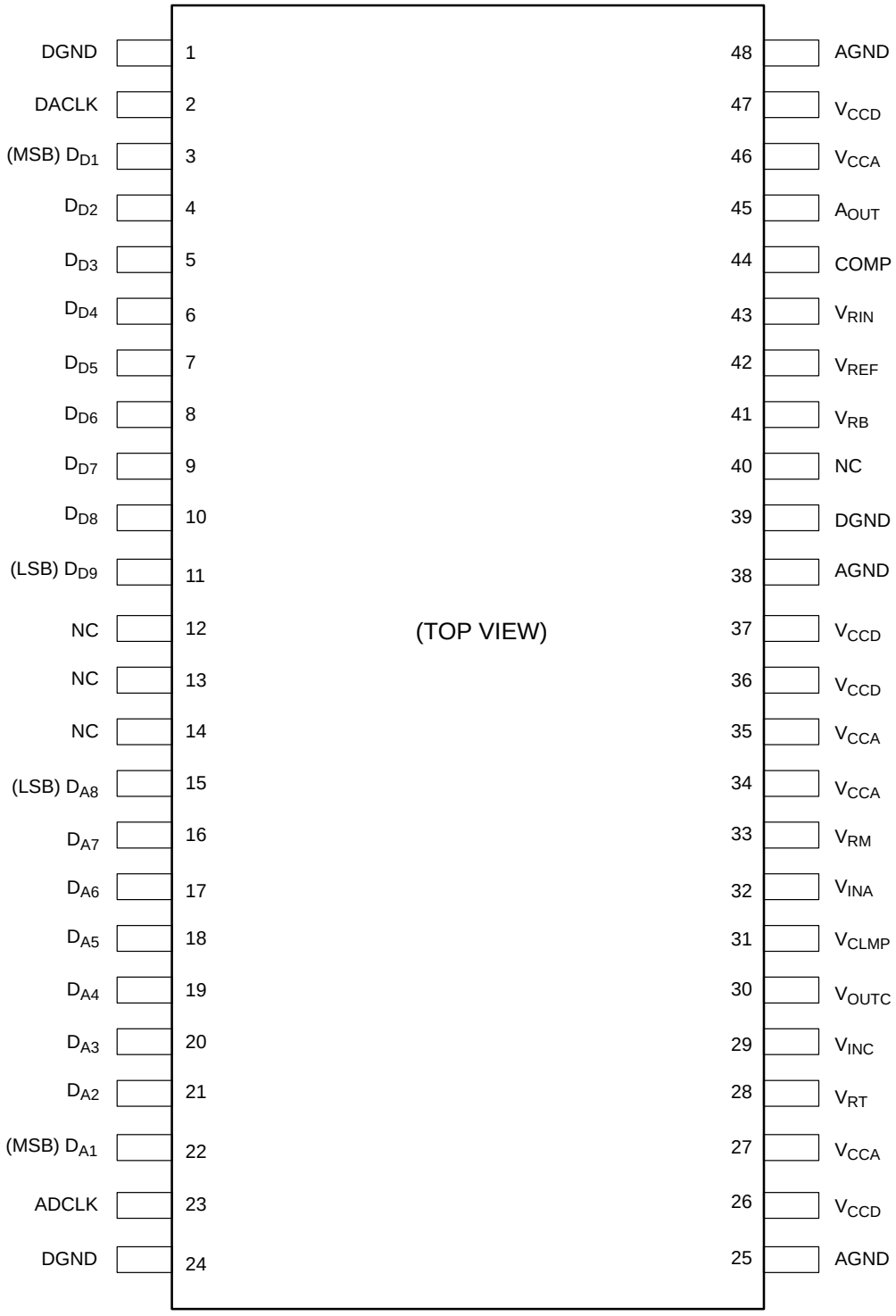


Figure 1. Pin Assignment (Continued)
MB40178–PF

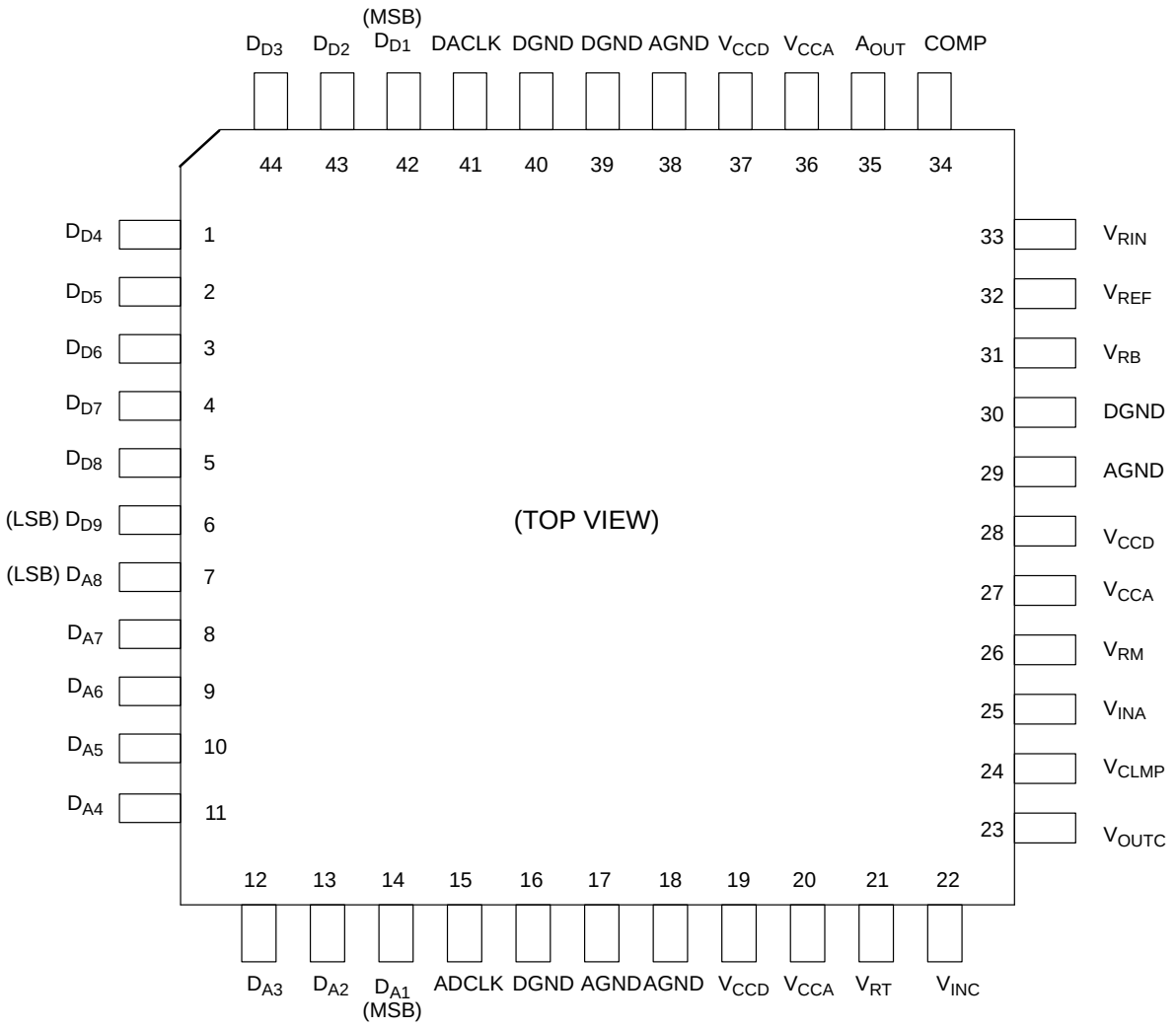
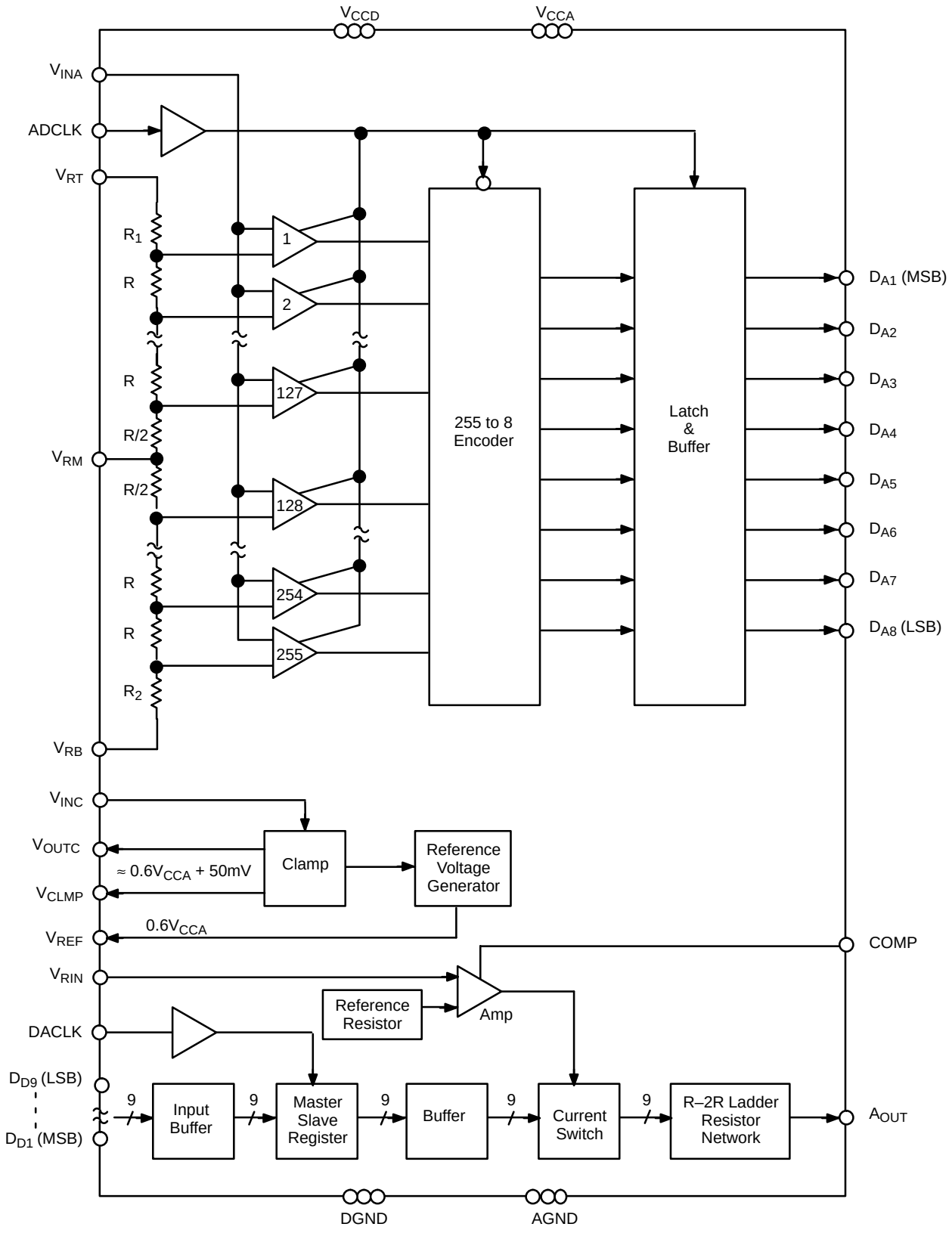


Figure 2. Block Diagram



PIN DESCRIPTION

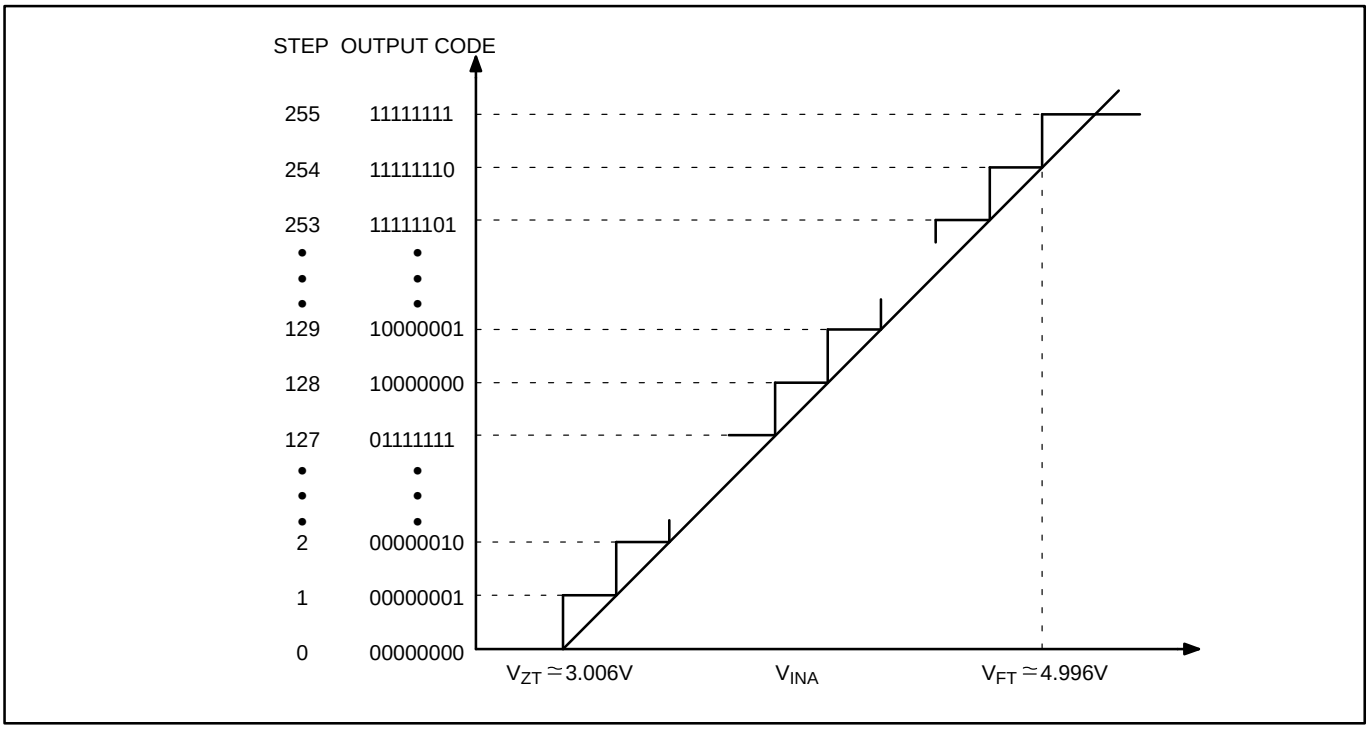
Table 1. Pin Description

Symbol	Pin No.		I/O	Name & Function
	QFP–44	SH–DIP–48		
V_{CCD}	19, 28, 37	26, 36, 37, 47	–	Digital Power Supply pins (+ 5 V).
V_{CCA}	20, 27, 36	27, 34, 35, 46	–	Analog Power Supply pins (+ 5 V).
DGND	16, 30, 39, 40	1, 24, 39	–	Digital Ground (0 V). These pins should be connected to the analog ground on the application system.
AGND	17, 18, 29, 38	25, 38, 48	–	Analog Ground (0 V). These pins should be connected to the analog ground on the application system.
$D_{A8} – D_{A1}$	7 – 14	15 – 22	O	ADC Digital Output pins. TTL level.
ADCLK	15	23	I	ADC Clock Input pin. TTL level.
V_{RT}	21	28	I	ADC Reference Voltage Input pin. (5 V Input)
V_{INC}	22	29	I	Sync Tip Clamp Circuit Analog Input pin. (0 – 3 V, 2 $V_{P–P}$). When a clamp circuit is not used, this pin is connected to ground.
V_{OUTC}	23	30	O	Clamp Circuit Analog Output pin. It is used by adding a capacitor (1 μF or more) between V_{CLMP} and V_{OVTC} pins. When a clamp circuit is not used, this pin is left open.
V_{CLMP}	24	31	O	Clamp Voltage Output pin (3.05V Output). When a clamp circuit is not used, this pin is left open.
V_{INA}	25	32	I	ADC Analog Signal Input pin. (3 – 5 V)
V_{RM}	26	33	–	ADC Middle Reference Voltage Monitor pin. (Mid of $V_{RT} – V_{RB}$ is set to this pin). Normally this pin is left open.
V_{RB}	31	41	I	ADC Reference Voltage Input pin. (3 V)
V_{REF}	32	42	O	Reference Voltage Output pin. (Resistor Divider, 3 V) By connecting this pin to V_{RB} pin, 3V Voltages are generated. When a reference voltage is not used, this pin is left open.
V_{RIN}	33	43	I	DAC Reference Voltage Input pin (3 V)
COMP	34	44	–	Phase Compensation Capacitor pin. (Capacitor greater than 0.1 μF should be connected between this pin and Analog Ground.)
A_{OUT}	35	45	O	Analog Signal Output pin
DACLK	41	2	I	DAC Clock Input pin. TTL level.
$D_{D9} – D_{D1}$*	42 – 6	3 – 11	I	DAC Digital Data Input pins. TTL level.

* For MB40168 only. For the MB40178, this bus is reversed. See pin assignment for full details.

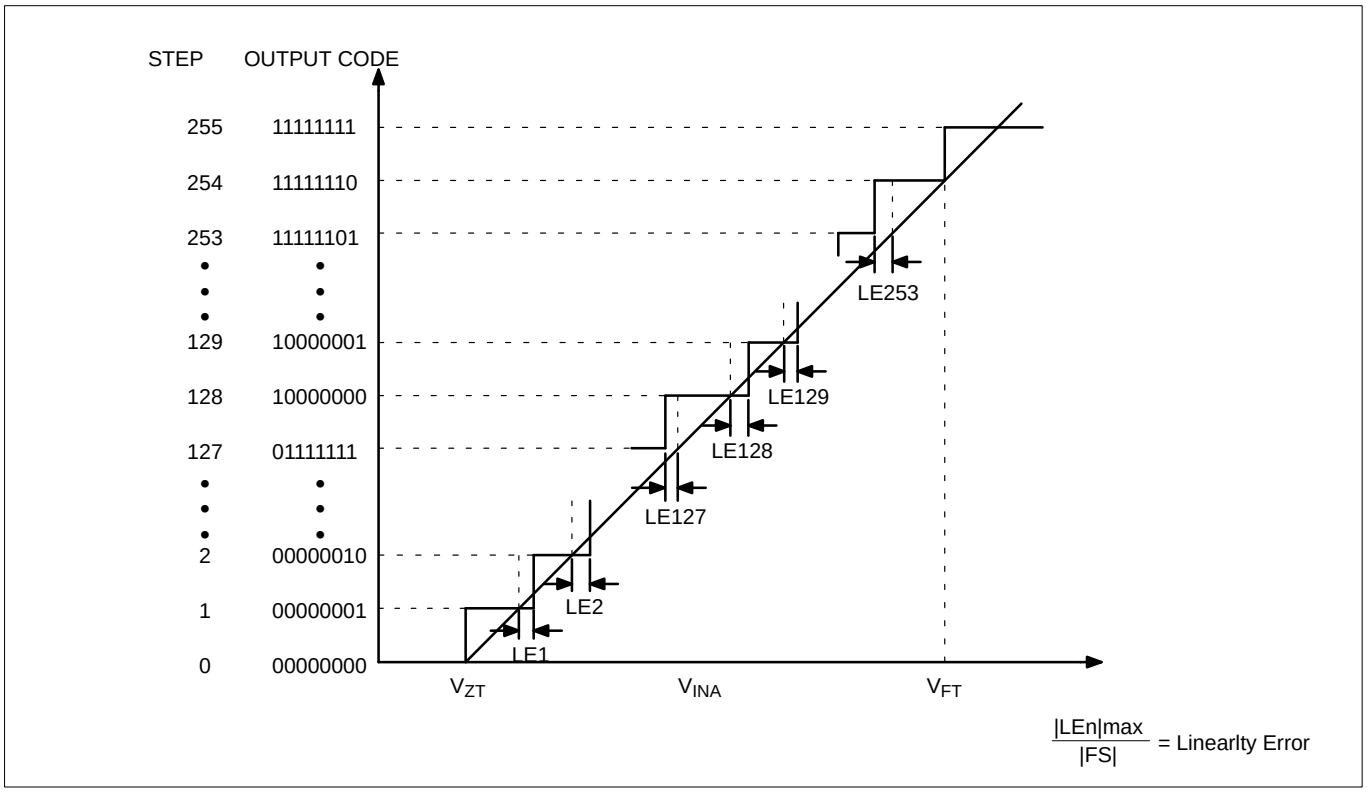
LINEARITY ERROR OF A/D CONVERSION

Ideal Characteristic

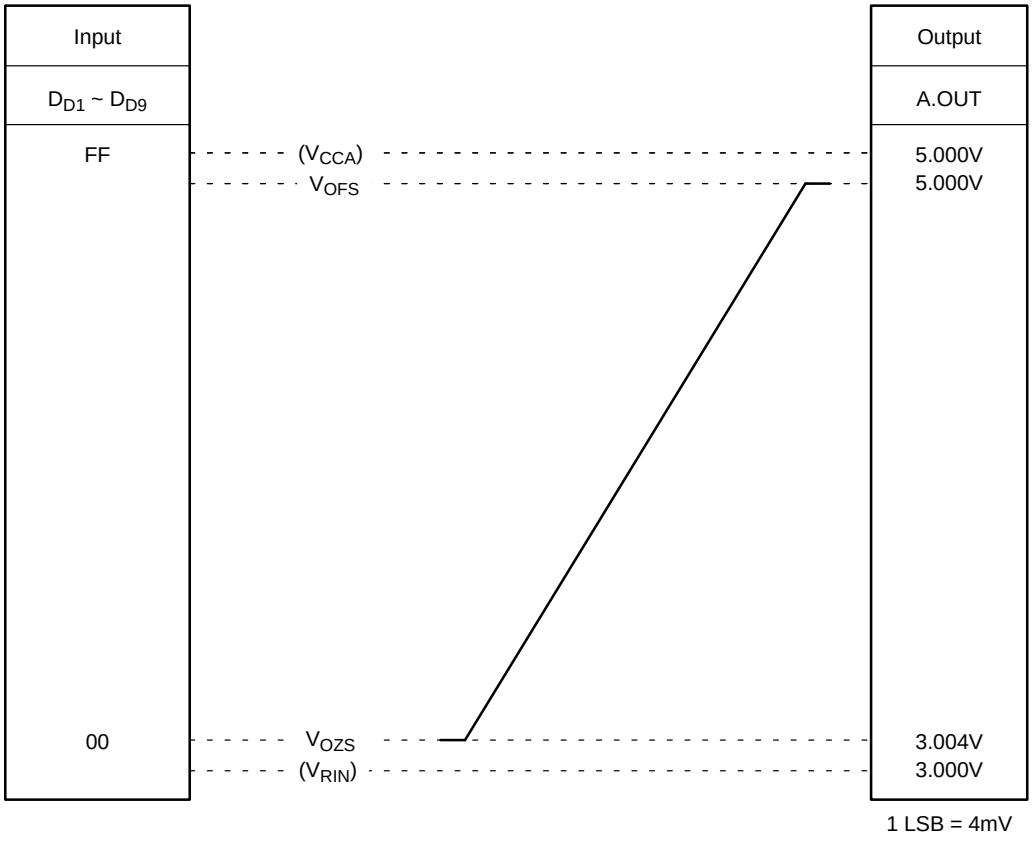


The values for V_{ZT} and V_{FT} are typical values under conditions that $V_{CCA} = V_{CCD} = 5V$ and $V_{RB} = 3V$.

Actual Characteristic



OUTPUT VOLTAGE CHARACTERISTIC OF D/A CONVERTER BLOCK



CALCULATION OF DAC OUTPUT VOLTAGE WHEN THE IDEAL CONVERSION IS PERFORMED

$$AOUT_N = V_{CCA} - \frac{511-N}{512} \times (V_{CCA} - V_{RIN})$$

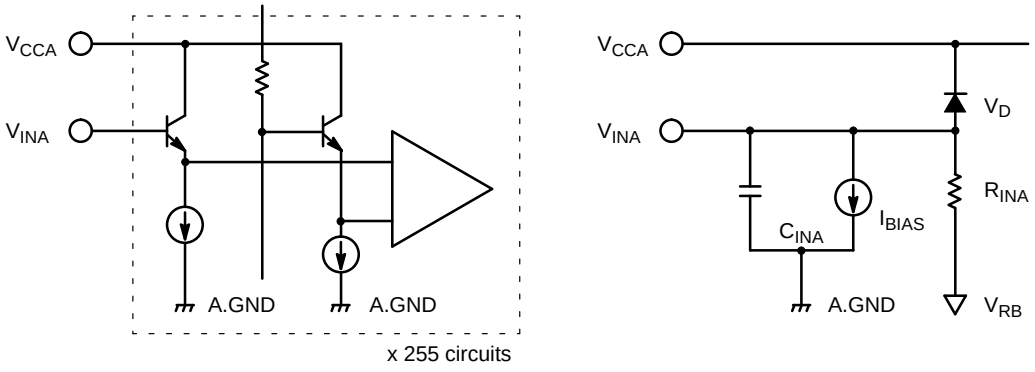
(N: Digital code (0 ~ 511)

$$V_{OFS} = V_{CCA}$$

$$V_{OZS} = V_{CCA} - \frac{511}{512} \times (V_{CCA} - V_{RIN})$$

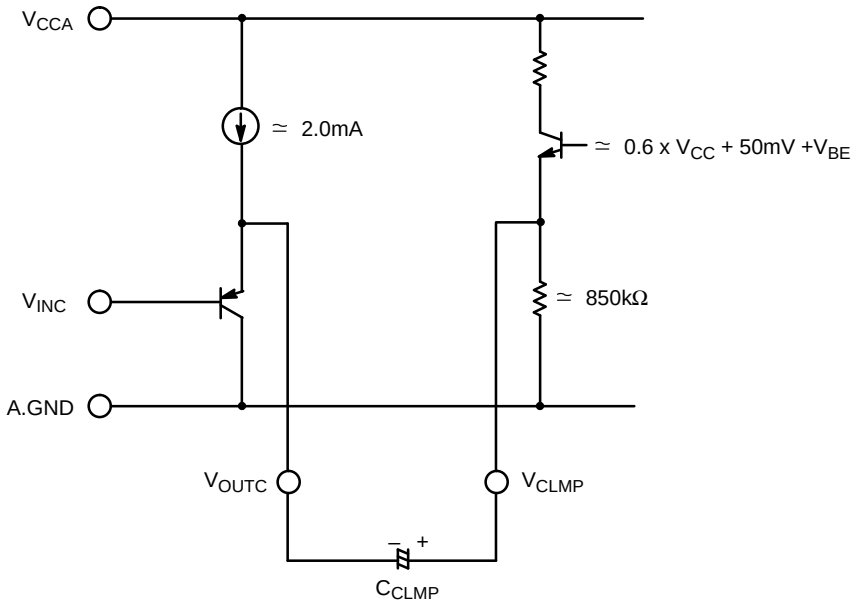
EQUIVALENT CIRCUITS OF ADC BLOCK

Analog Input Equivalent Circuit

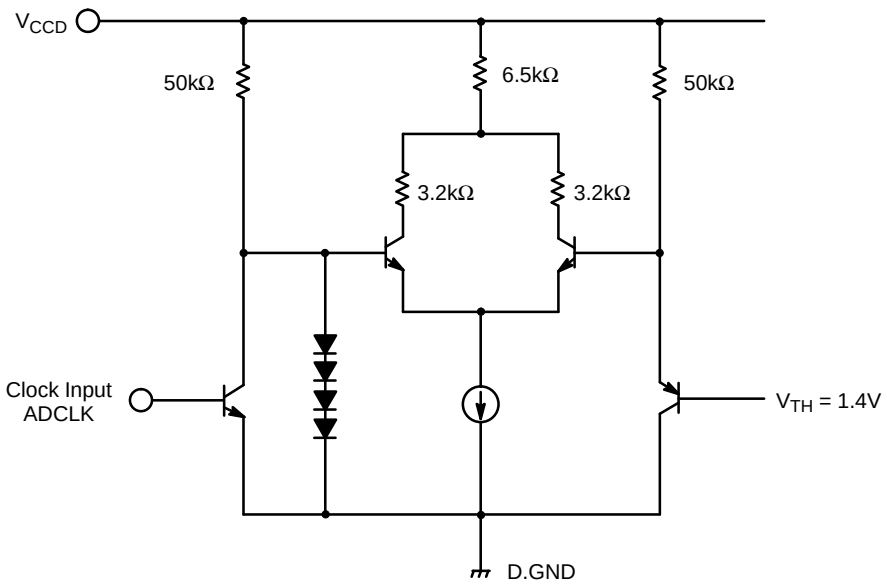


C_{INA}: Junction Capacitance of non–linear emitter follower
R_{INA}: Linear resistance model of input current by the comparator switching
$V_{INA} < V_{RB}$: ∞
CLK = "H": ∞
V_{INA}: This is the voltage on V_{RB} Pin, not V_{RB} Pin itself.
I_{BIAS}: Constant input bias current
V_D: Base–Collector junction diode of emitter follower transistor

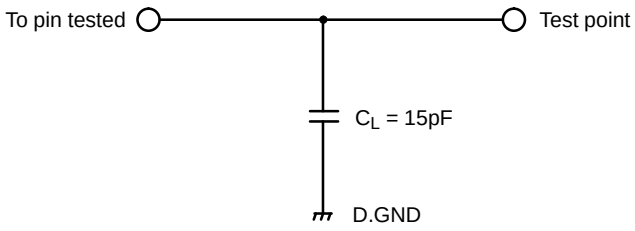
Clamp Input Equivalent Circuit



Digital Input Equivalent Circuit



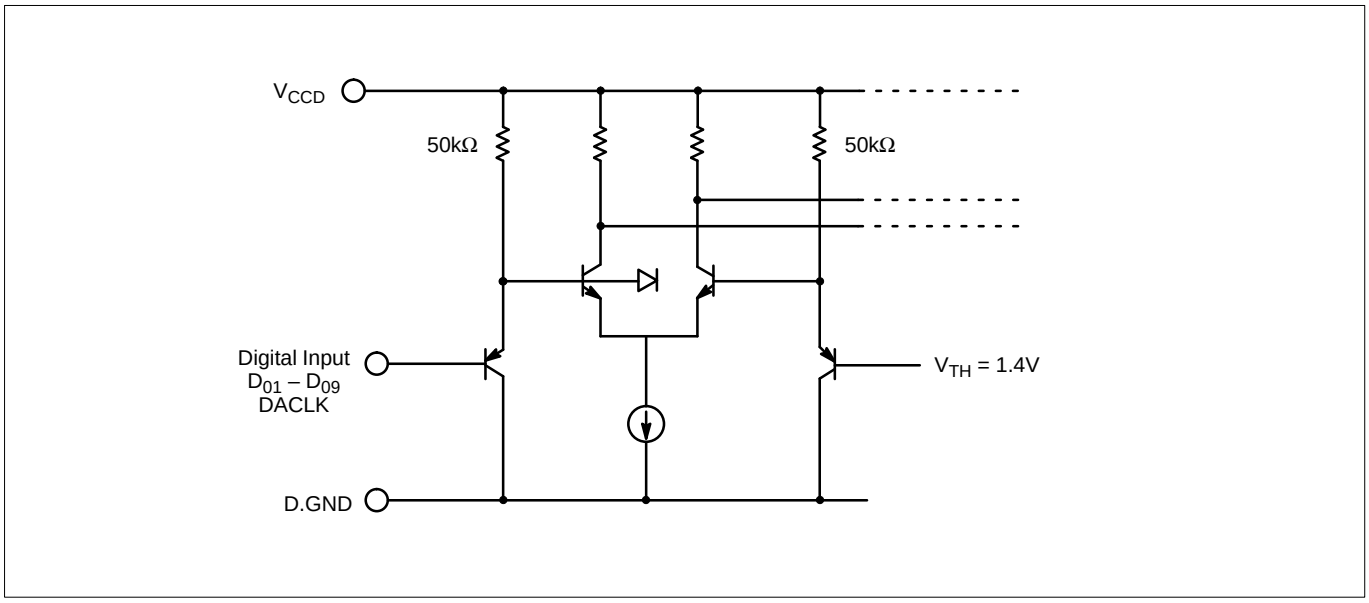
Digital Output Load Circuit



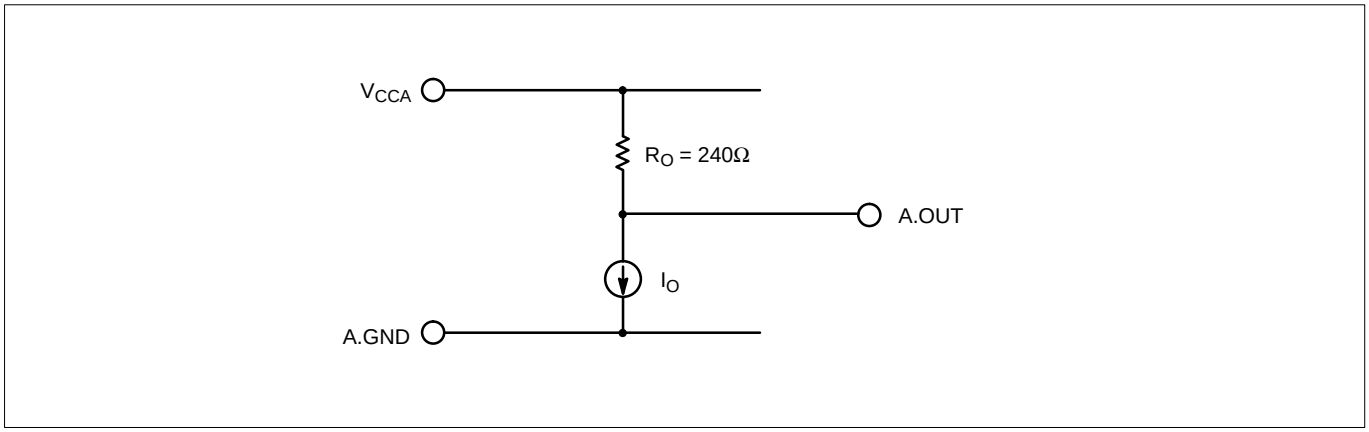
NOTE: C_L includes the floating capacitance of probe and jig.

EQUIVALENT CIRCUITS OF DAC BLOCK

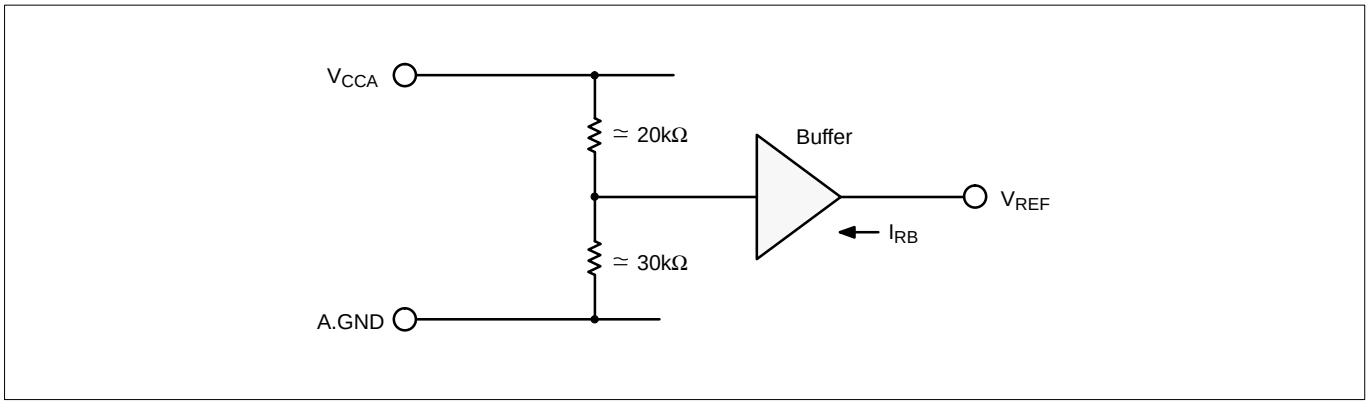
Digital Input Equivalent Circuit



Analog Output Equivalent Circuit



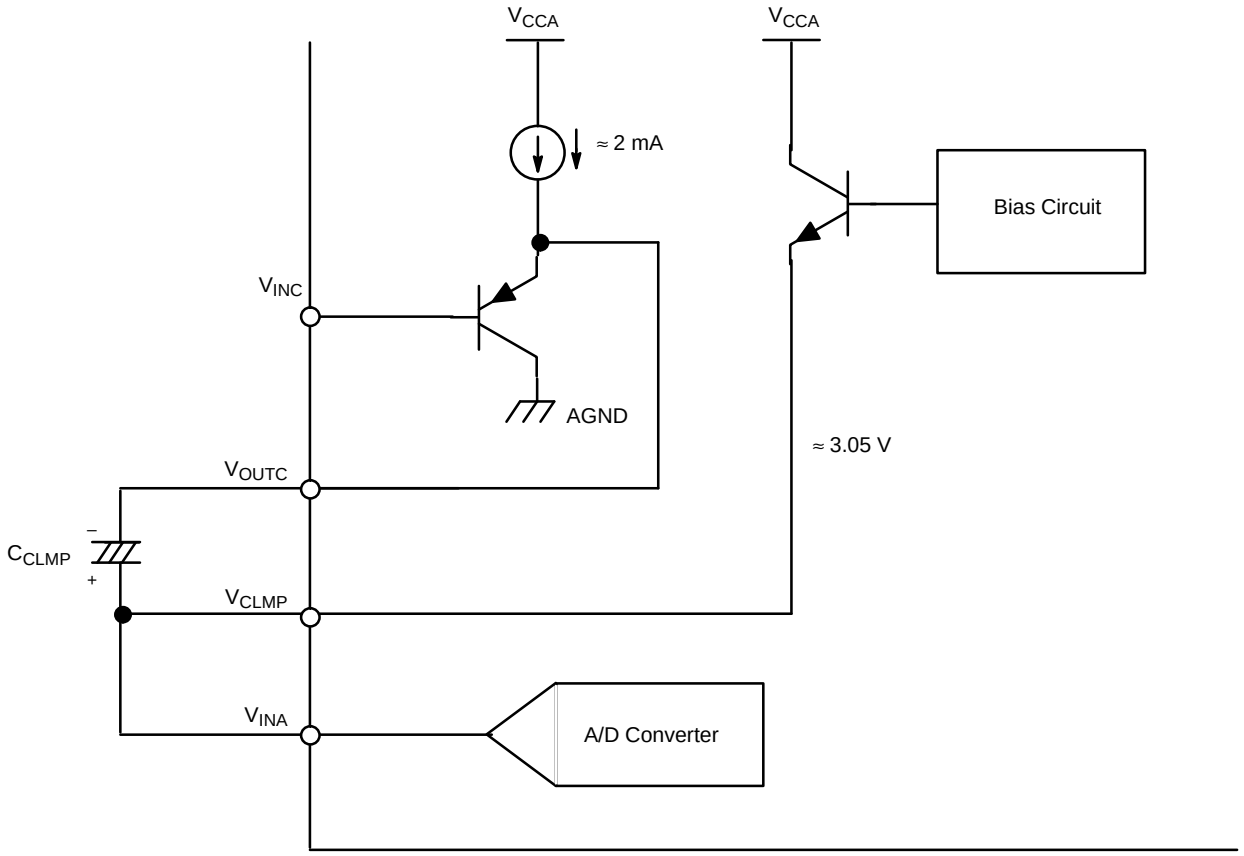
Reference Voltage Generator Equivalent Circuit



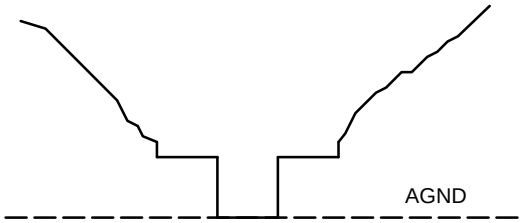
CLAMP CIRCUIT OPERATION

Clamp Circuit

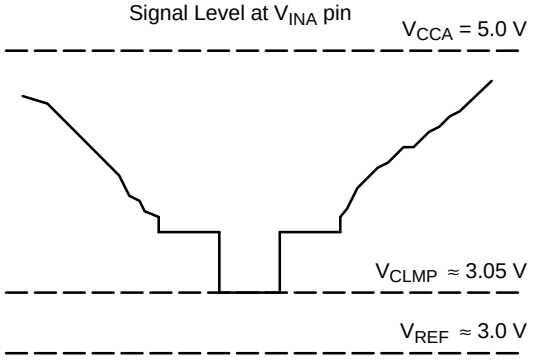
Clamp Voltage is set at 0.6 x V_{CC} + 50 mV (typ.)



Signal Level at V_{INC} pin



Signal Level at V_{INA} pin



Note: When Clamp Circuit is not applied the signals should be connected as follows:

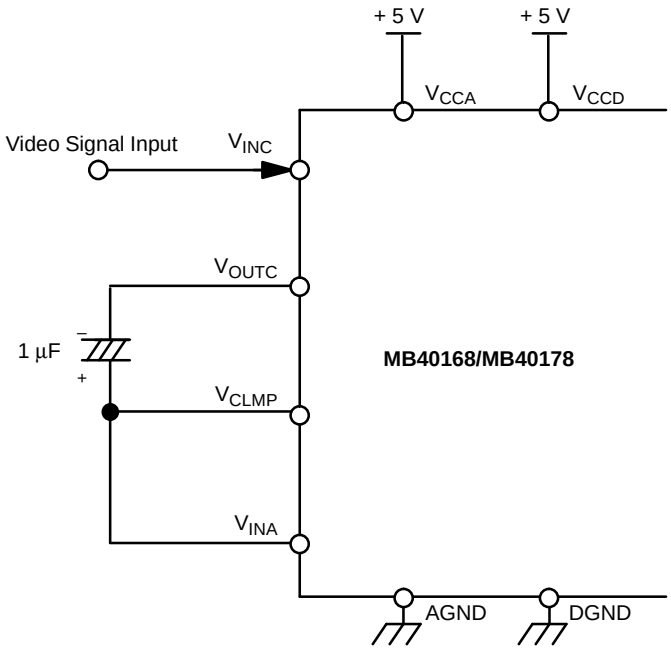
V_{INC}: Connect to GND.

V_{OUTC}: Leave open.

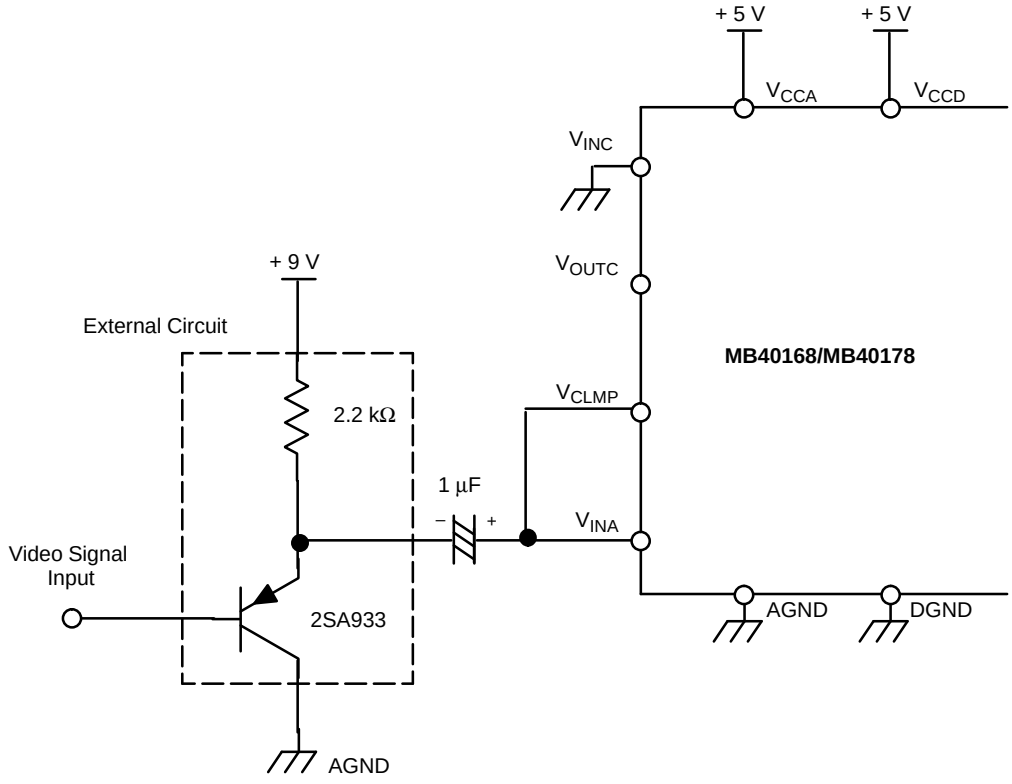
V_{CLMP}: Leave open.

TYPICAL CONNECTION CIRCUITS

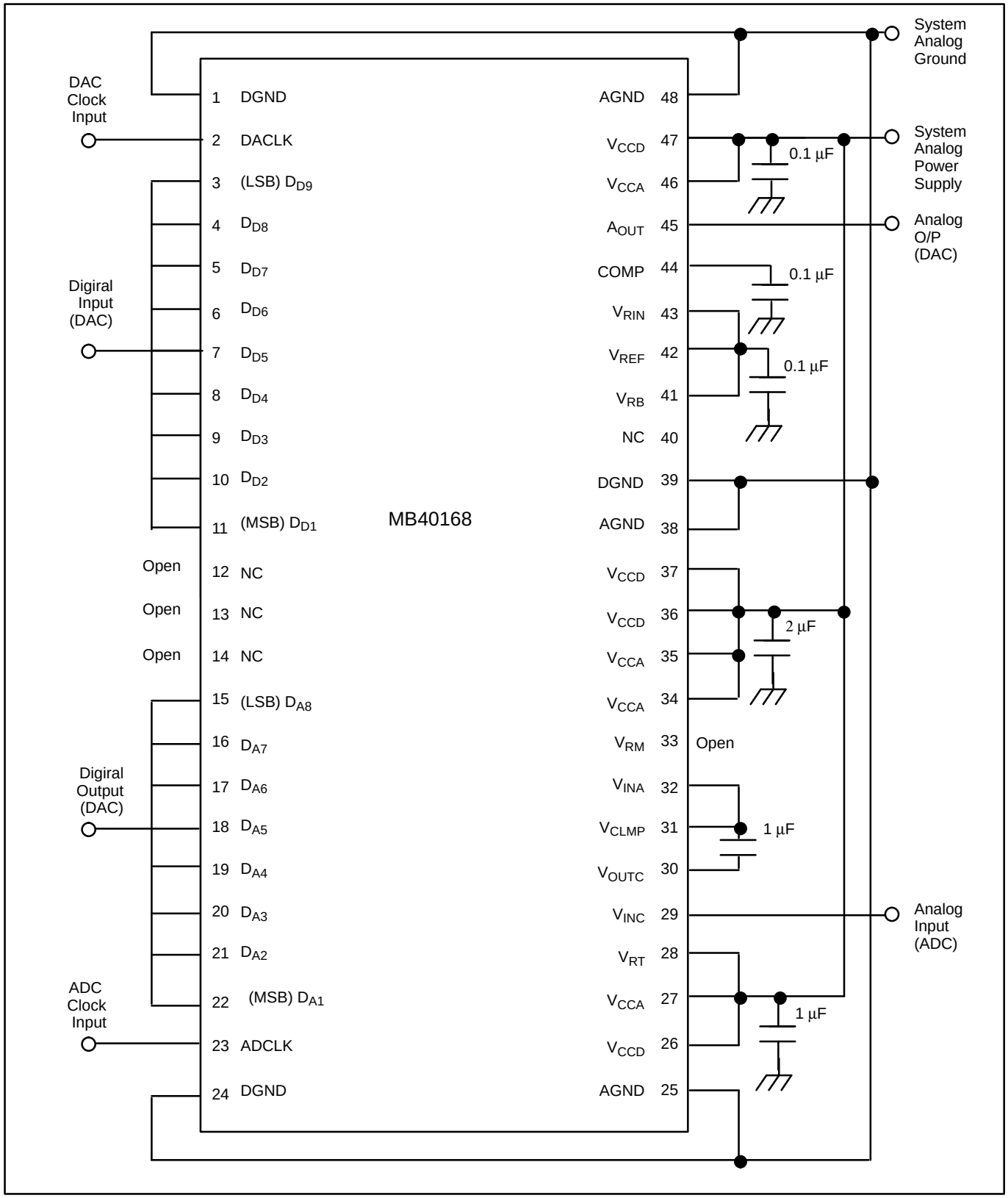
Example 1: Video Signal Input to V_{INC} Pin



Example 2: Video Signal Input to V_{CLMP} and V_{INA} Pins



TYPICAL CONNECTION CIRCUIT(Example)



NOTES ON PCB LAYOUT

Power Supply Lines

The device's power supply lines (V_{CCA}, V_{CCD}, AGND and DGND) should be laid out as analog lines and should be separated in so far as possible from other digital lines in order to reduce noise. Also the track widths of these lines should be as wide as possible to reduce parasitic impedance.

Coupling Capacitors

The device's power supply lines V_{CCA} and V_{CCD} and the reference voltage pins V_{RIN}, V_{REF}, V_{RB}, and V_{RT} should be decoupled to analog ground by means of approx. 1 μF capacitors which should be placed as close as possible to these pins.

Digital Output Load

The load at the digital outputs should be kept as low as possible to prevent noise in the power supply lines caused by digital output switching. If, due to long wiring, the load becomes large then a buffer with small input capacitance should be inserted to reduce load capacitance.

OTHER NOTES ON OPERATION

When using the D/A converter with its V_{RIN} pin connected to the V_{REF} pin, the A/D converter's V_{RB} pin must also be connected to the V_{REF} because otherwise the internal reference voltage generation circuitry cannot output 3 V.

When using the D/A converter with 8 bit resolution the DD9 (LSB) pin should be grounded.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage *1		V_{CCA}, V_{CCD}	4.75	5.00	5.25	V
Clamp Circuit Input Voltage *2		V_{INC}	0	–	3	V
Analog Input Voltage		V_{INA}	V_{RB}	–	V_{RT}	V
ADC Reference Voltage *3	Top	V_{RT}	V_{CCA} – 0.1	V_{CCA}	V_{CCA} + 0.1	V
	Bottom	V_{RB}	2.75	3.0	3.25	V
DAC Reference Voltage		$V_{CCA} – V_{RIN}$	0.7	2.0	2.2	V
		V_{RIN}	2.65	3.0	4.3	V
Digital Input High Voltage		V_{IHD}	2.0	–	–	V
Digital Input Low Voltage		V_{ILD}	–	–	0.8	V
Digital Output High Current		I_{OH}	–400	–	–	µA
Digital Output Low Current		I_{OL}	–	–	1.6	mA
Clock Frequency	A/D	f_{CLKAD}	–	–	20	MHz
	D/A	f_{CLKDA}	–	–	40	MHz
Minimum High Clock Pulse Width	A/D	t_{WHAD}	22.5	–	–	ns
	D/A	t_{WHDA}	10.5	–	–	ns
Minimum Low Clock Pulse Width	A/D	t_{WLAD}	22.5	–	–	ns
	D/A	t_{WLAD}	10.5	–	–	ns
Set up Time		t_{SU}	10	–	–	ns
Hold Time		t_H	4	–	–	ns
Clamp Capacitance		C_{CLMP}	1	–	–	µF
Phase Compensation Capacitance		C_{COMP}	0.1	–	–	µF
Ambient Operating Temperature		T_A	–20	–	+70	°C

Notes:

*1 : V_{CCA} and V_{CCD} must be used in the same voltage level.
*2 : V_{INC} must have an amplitude of $V_{CCA} – V_{CLMP}$.
*3 : $V_{RT} – V_{RB}$ must have 2.0V±0.1V.

DC CHARACTERISTICS

ANALOG BLOCK

(V_{CCA} = V_{CCD} = 4.75 V ~ 5.25 V, T_A = –20 °C ~ +70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
ADC Resolution			–	8	–	bits
DAC Resolution			–	9	–	bits
ADC Linearity Error	LE_{AD}	DC accuracy V_{CCA} = V_{CCD} = 5.0 V	–	± 0.15	± 0.3	%
DAC Linearity Error	LE_{DA}		–	± 0.1	± 0.2	%
Analog Input Equivalent Impedance	R_{INA}	$R_{INA} = \frac{V_{RT} - V_{RB}}{I_{IHA} - I_{ILA}}$	0.3	1.3	–	MΩ
Analog Input Capacitance	C_{INA}	f_{INA} = 1 MHz	–	40	–	pF
Analog Input High Current	I_{IHA}	V_{INA} = V_{RT}	–	–	45	µA
Analog Input Low Current	I_{ILA}	V_{INA} = V_{RB}	–	–	40	µA
Reference Output Voltage	V_{REF}	V_{REF}, V_{RB}, V_{RIN} shorted together	0.6V_{CCA} – 0.1	0.6V_{CCA}	0.6V_{CCA}+ 0.1	V
Clamp Voltage	V_{CLMP}		–	V_{REF} + 50 mV	–	V
ADC Reference Current	I_{RB}		–8.5	– 5.5	– 3.0	mA
DAC Reference Current	I_{RIN}	V_{RIN} = 3.000 V	–	–	10	µA
Clamp Circuit Input Current	I_{INC}	V_{INC} = 0 V	–600	–200	–	µA
Full Scale Output Voltage	V_{OFS}		V_{CCA}=20mV	V_{CCA}	–	V
Zero Scale Output Voltage	V_{OZS}	V_{CCA} = 5.00 V V_{CCD} = 5.00 V V_{RIN} = 3.000 V	2.934	3.004	3.072	V
Output Impedance	R_O	T_A = +25 °C	192	240	288	Ω
Supply Current	I_{CC}		–	70	125	mA

DC CHARACTERISTICS

DIGITAL BLOCK

(V_{CCA} = V_{CCD} = 4.75 V ~ 5.25 V, T_A = –20 °C ~ +70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Digital Output High Voltage	V_{OHD}	I_{OH} = –400 µA	2.7	–	–	V
Digital Output Low Voltage	V_{OLD}	I_{OL} = 1.6 mA	–	–	0.4	V
Digital Input High Voltage	V_{IHD}		2.0	–	–	V
Digital Input Low Voltage	V_{ILD}		–	–	0.8	V
Digital Input High Current	I_{IHD}	V_{IHD} = 2.7 V	–	–	20	µA
Digital Input Low Curent	I_{ILD}	V_{ILD} = 0.4 V	–100	–	–	µA

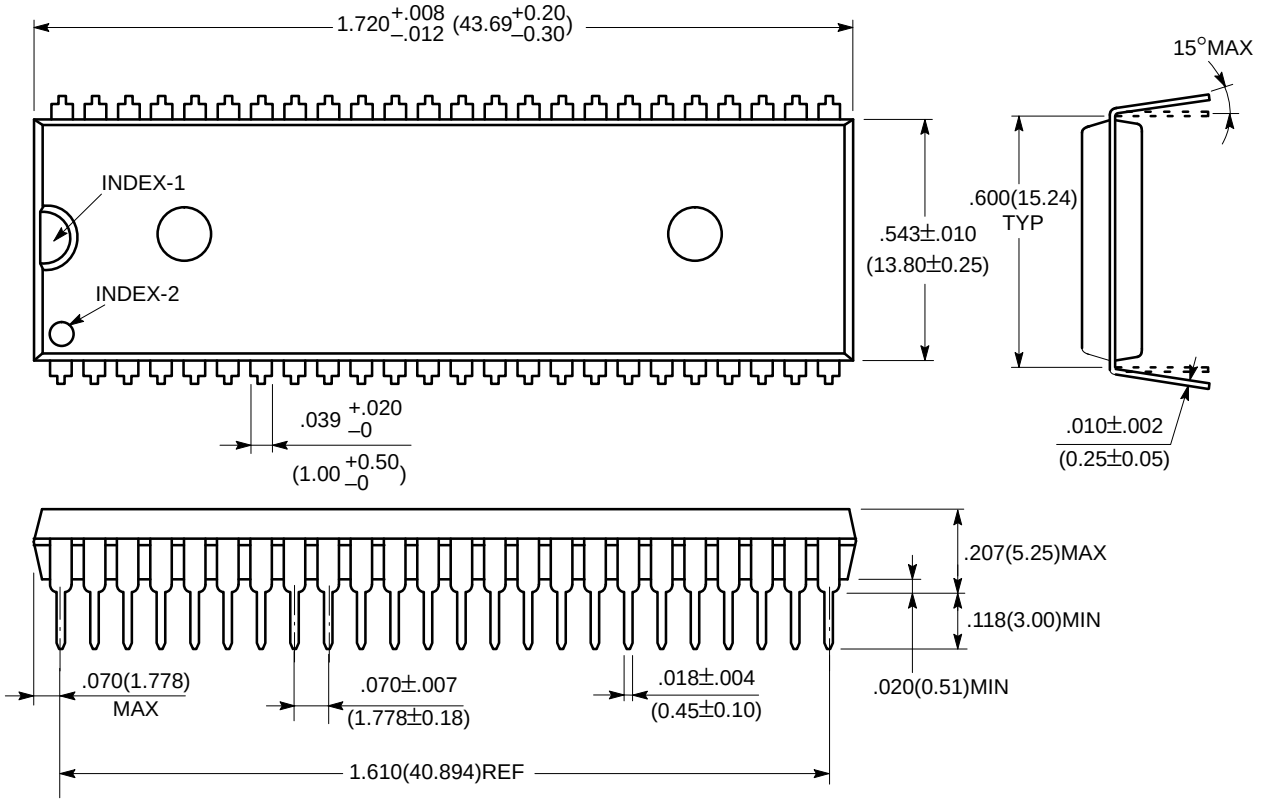
AC CHARACTERISTICS

(V_{CCA} = V_{CCD} = 4.75 V ~ 5.25 V, T_A = –20 °C ~ +70 °C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Maximum Conversion Rate	A/D	f_{SAD}		20	–	–	MSPS
	D/A	f_{SDA}		40	–	–	MSPS
Digital Output Delay Time		$t_{pd\ AD}$		8	15	30	ns
Analog Output Delay Time		$t_{pd\ DA}$	C_L = 15 pF Terminating Resistor A_{OUT} = 240 Ω	–	10	–	ns
Analog Output Rise Time		t_r		–	5	–	ns
Analog Output Fall Time		t_f		–	5	–	ns
Settling Time		$t_{set\ LH}$, $t_{set\ HL}$		–	16	–	ns

PACKAGE DIMENSIONS

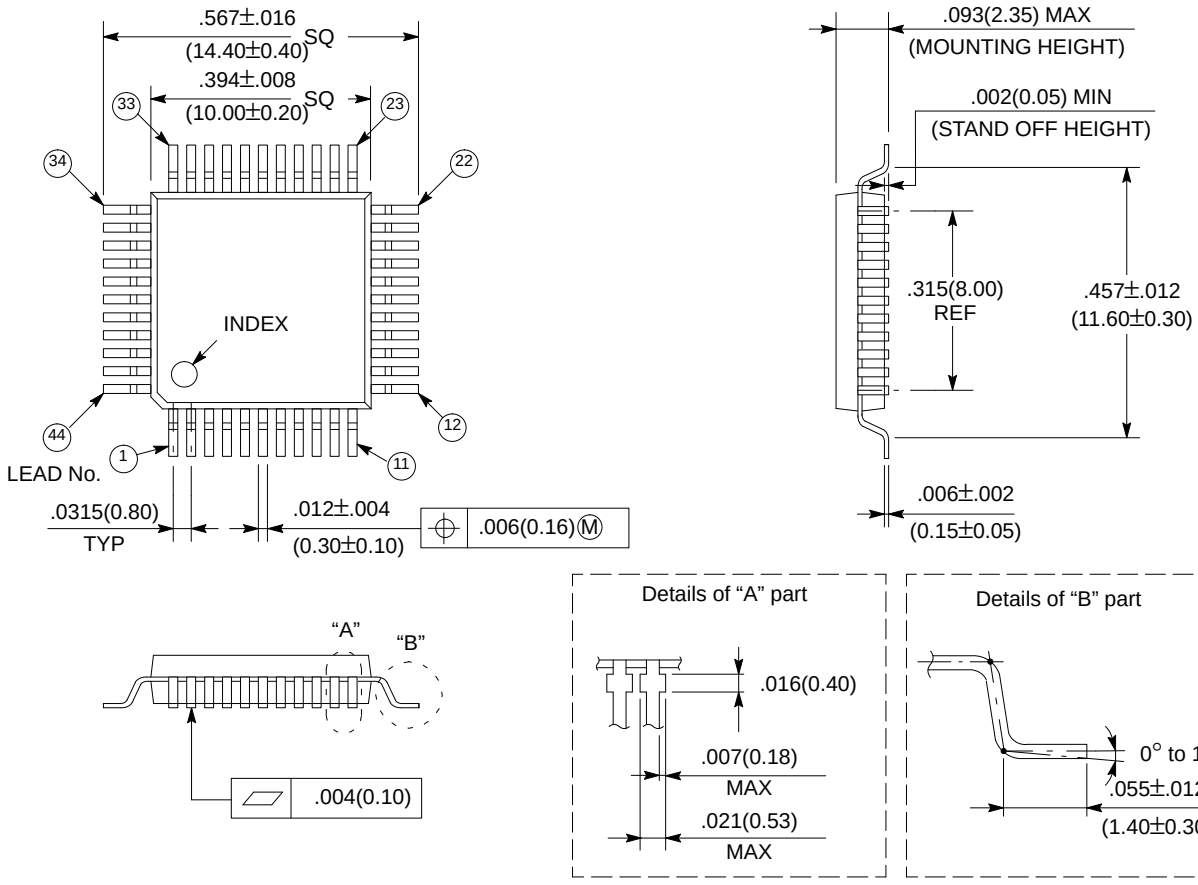
48-PIN PLASTIC SHRINK DIP PACKAGE
(CASE No.: DIP-48P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

44-PIN PLASTIC FLAT PACKAGE
(CASE No.: FPT-44P-M01)



Dimensions in
inches (millimeters)