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FUJITSU

DATA SHEET

CG/CE46
0.65 Micron High Performance, Low Power CMOS Gate Arrays

Description

The Fujitsu CG46 is a high performance, 0.65 µm drawn channel length, digital CMOS gate array family. The CE46 is a 0.65 µm drawn channel length, digital CMOS embedded gate array product family. The CE46 offers full support of diffused high speed RAMs, ROMs and embedded megacells. The CE46 series offers density and performance approaching that achievable with standard cell solutions but with the time to market advantage of traditional gate arrays. Both product families feature channelless (Sea–of–Gates) architecture with two layer metal.

A 5.0 volt product, the CG/CE46 features low power and high pin to gate count ratio. These product families are optimized for cost sensitive, high volume applications such as personal computers, workstations and communication systems. A wide variety of high performance and cost effective packages are available including PQFP, CQFP, TQFP, BGA and MCM's. Pin counts of up to 352 are available.

Features

- 0.65 mm drawn channel length
- 5V ± 5% or 3.3V ± 0.3V supply voltage
- Channelless, Sea–of–gates Architecture
- Internal gate delay of 300ps, F/O = 2, L= 1mm @ 5.0V
- CE46 RAM compiler supports Single/Dual Port RAM
- Supports JTAG boundary scan, full and partial scan
- PCI buffer available
- Clock net for optimized on–chip clock skew control
- High drive capability: 3.2, 8, or 12 mA in a single I/O slot (24 mA available with double I/O)
- Optimized for 5V ±5%, capable of 3.3V ±0.3V
- Maximum toggle frequency is 175 MHz, Supports system clock frequencies in excess to 70 MHz
- CE46 Supports mixed 5V and 3.3V I/Os
- Supports all major third party design tools including Cadence, Mentor, Synopsys and Sunrise.
- Higher performance and 30% lower power than 0.8 µm technology
- High pad to gate ratio

CE46 Embedded Gate Array Product Summary

Device Name	Gross Gates	Usable Gates	Max. Pads	Metal Wiring
CE46F10	53,636	28,427	208	2
CE46F20	71,004	36,922	240	2
CE46F30	83,028	42,344	256	2
CE46F40	90,804	45,402	272	2
CE46F50	101,616	49,791	288	2
CE46F60	113,036	54,257	304	2
CE46F70	137,700	64,719	336	2
CE46F80	154,260	70,959	352	2
CE46F90	198,084	89,137	400	2

CG46 Gate Array Product Summary

Device Name	Gross Gates	Usable Gates	Max. Pads	Metal Wiring
CG46533	53,636	28,427	208	2
CG46713	71,004	36,922	240	2
CG46833	83,028	42,344	256	2
CG46104	101,616	49,791	288	2
CG46134	137,700	64,719	336	2
CG46194	198,084	89,137	400	2

DC CHARACTERISTICS

Measuring conditions: V_{DD} = 5V ± 5%, Vss = 0 V, Ta = 70 °C

Parameter	Symbol	Test Conditions		Requirements			Unit
				Min.	Typ.	Max.	
Supply Voltage	I_{DDS}	Standby mode[1]				0.2[2]	mA
High-level input voltage	V_{IH}	CMOS level	Normal cell	V_{DD}x0.7		V_{DD}	V
			Schmitt trigger	V_{DD}x0.8		V_{DD}	
		TTL level	Normal cell	2.2		V_{DD}	
			Schmitt trigger	2.4		V_{DD}	
Low-level input voltage	V_{IL}	CMOS level	Normal cell	V_{SS}		V_{DD}x0.3	V
			Schmitt trigger	V_{SS}		0.6	
		TTL level	Normal cell	V_{SS}		0.8	
			Schmitt trigger	V_{SS}		0.6	
High-level output voltage	V_{OH}	I_{OH}=–2 mA [3]		4.0		V_{DD}	V
		I_{OH}=–4 mA					
		I_{OH}=–8 mA					
Low-level output voltage	V_{OL}	I_{OL}=3.2 mA		V_{SS}		0.4	V
		I_{OL}=8 mA					V
		I_{OL}=12 mA					V
		I_{OL}=24 mA				0.5	V
Input leakage current (Three-state pin input)[4]	I_{LI}	V_I=0 to V_{DD}		–5		5	μA
	I_{LZ}			–5		5	
Input pull-up/pull-down resistors[5]	R_P	Pull-up V_I = V_{SS}		25	50	100	kΩ
	R_N	Pull-down = V_I = V_{DD}					

NOTES:

1. V_{IH} = V_{dd} and V_{IL} = V_{SS}, the memory is in the standby mode
2. If an input buffer with pull–up/pull–down resistor is used, the supply current may not be assured depending on the circuit configuration.
3. The high level output voltage of the IOL=8mA type output buffer is identical to that (IOH = 2mA) of the IOL = 3.2mA type output buffer.
4. If an input buffer with pull–up/pull–down resistor is used, the input leakage current may exceed the above value.
5. Either a buffer without a resistor or with a pull–up/pull–down resistor can be selected from the input and biodirectional buffers.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Requirements				Unit
Supply Voltage	V_{DD}	V_{SS}[1] –0.5 to +6.0				V
Input voltage	V_I	V_{SS}[1] –0.5 to V_{DD} +0.5				V
Output voltage	V_O	V_{SS}[1] –0.5 to V_{DD} +0.5				°C
Operating temperature	T_a	Plastic –40 to +85				°C
		Ceramic –55 to +125				
Storage temperature	T_{ST}	Plastic –40 to +85				°C
		Ceramic –65 to +150				
		Type/Condition		**$V_O = V_{DD}$**	**V_O = OV**	
Output current	I_O[3]	Normal Type	O_{IL}=3.2 mA	+40	–40	mA
		Power-type	O_{IL}=8 mA	+80	–40	
		High-power type	O_{IL}=12 mA	+120	–60	
		Double high-power type	O_{IL}=24 mA	+180	–90	
Overshoot	—	V_{SS}[1] +1.0 V to max.[2]				
Undershoot	—	V_{SS}[1]+1.0 V to max.[2]				

NOTES:
1. V_{SS} = 0V
2. For 50 ns max.
3. For one second per pin

RECOMMENDED OPERATING CONDITIONS (5.0V)

Parameter		Symbol	Requirements			Unit
			Min.	Typ.	Max.	
Supply Voltage		V_{DD}	4.75	5.0	5.25	V
High-level input voltage	CMOS level	V_{IH}	V_{DD}x0.7	—	V_{DD}	V
	TTL level		2.2	—	V_{DD}	
Low-level input voltage	CMOS level	V_{IL}	V_{SS}[1]	—	V_{DD} x 0.3	V
	TTL level		V_{SS}[1]		0.8	
Operating temperature		T_a	0	25	70	°C

NOTES:
1. V_{SS} = 0V

RECOMMENDED OPERATING CONDITIONS (3.3 V)

Parameter	Symbol	Requirements			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Operating temperature	T_a	0	—	70	°C

INPUT/OUTPUT PIN CAPACITANCE

Parameter		Symbol	Requirements	Unit
Input pin		C_{IN}	Max. 16	pF
Output pin	I_{OL} = 3.2 mA, 8 mA, 12mA type	C_{OUT}	Max. 16	pF
	I_{OL} = 24 mA type		Max. 18	
I/O pin	I_{OL} = 3.2 mA, 8 mA, 12mA type	C_{VO}	Max. 16	pF
	I_{OL} = 24 mA type		Max. 18	

Measuring conditions: T_a=25 °C
V_{DD}=V_I=OV, f=1 MHz

PACKAGE AVAILABILITY

Package	**Array**								
CE46 –	F10	F20	F30	F40	F50	F60	F70	F80	F90
CG46 –	533	713	833	—	104	—	134	—	194
QFP100	P	P	P	P	P				
QFP160	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C
SQFP80	P	P	P						
SQFP100	P	P	P	P					
SQFP144	P	P	P	P	P	P	P	P	
SQFP176	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C	
SQFP208	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C
SQFP240		P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C
SQFP256							P,C	P,C	P,C
TQFP100	P	P	P	P	P	P	P	P	
BGA256(B)			P	P	P	P	P	P	
BGA352(B)								P	P
BGA352(C)						P	P	P	P

NOTES: P: Plastic
C: Cerquad

DC CHARACTERISTICS at 3.3V Operating Conditions

Measuring conditions: V_{DD} = 3.3V ± 0.3V, Vss = 0 V, Ta = 0° to70 °C

Parameter	Symbol	Test Conditions		Requirements			Unit
				Min.	Typ.	Max.	
Supply Current	I_{DDS}	Standby mode *1		—	—	20[2]	μA
High-level input voltage	V_{IH}	CMOS level	Normal cell * 3	V_{DD}x0.7	—	V_{DD}	V
			Schmitt trigger * 4	V_{DD}x0.8	—	V_{DD}	
Low-level input voltage	V_{IL}	CMOS level	Normal cell * 3	V_{SS}	—	V_{DD}	
			Schmitt trigger * 4	V_{SS}		V_{DD}	
High-level output voltage	V_{OH}	I_{OH} = –1 mA * 5		V_{DD}–0.3	—	V_{DD}	V
		I_{OH} = –1 mA * 6					
		I_{OH} = –2 mA * 7					
		I_{OH} = –4 mA * 8					
Low-level output voltage	V_{OL}	I_{OL} = 2 mA * 5		V_{SS}	—	0.4	V
		I_{OL} = 4 mA * 6					V
		I_{OL} = 6 mA * 7					V
		I_{OL} = 12 mA * 8					V
Input pull-up/pull-down resistors *4	R_P	Pull-up V_I = V_{SS}		40	150	350	kΩ
	R_N	Pull-down = V_I = V_{DD}		40	100	200	

NOTES:
*1. V_{IH} = V_{DD} and V_{IL} = V_{SS}, the memory is in the standby mode.
*2. If an input buffer with pull–up/pull–down resistor is used, the supply current may not be assured depending on the circuit configuration.
*3. Equivalent to CMOS Input terminal.
*4. Equivalent to CMOS Schmitt Input terminal.
*5. Equivalent to IOL= 3.2mA ouput (at VDD = 5V).
*6. Equivalent to IOL= 8mA ouput (at VDD = 5V).
*7. Equivalent to IOL= 12mA ouput (at VDD = 5V).
*8. Equivalent to IOL= 24mA ouput (at VDD = 5V).

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