DS04-21332-1E

FUJITSU

DATA SHEET

ASSP
1.2 GHz High-Speed Tuning PLL Frequency Synthesizer
MB15A16

PRELIMINARY

■ DESCRIPTION

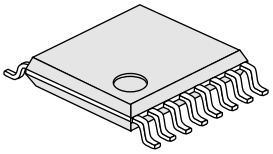
The Fujitsu MB15A16 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function, and is suitable for the digital radio applications such as GSM. MB15A16 achieves the low noise performance as well as the high-speed lock-up which required for digital cellularphones.
The MB15A16 can operate from a single +3 V supply and has an Icc of 7.0 mA (typical).

■ FEATURES

- High operating frequency : f_{IN} = 1.2 GHz (V_{IN} = –10 dBm)
- Pulse-swallow function : High-speed dual-modules prescaler with selectable 64/65 and 128/129 divide ratios
- Low supply current : I_{CC} = 7.0 mA typ. at 3 V
- Power saving funtion : I_{PS} = 100 µA typ. (Controlled with PS pin)
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter : 0 to 127
  Binary 11-bit programmable counter : 5 to 2,047
- Serial input 17-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 6 to 16,383
  1-bit for setting a prescaler divide ratio (SW bit)
  1-bit for switching a phase polarity (FC bit)
  1-bit for selecting LD/fout (LDS bit)
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Two types of phase comparator outputs selectable
  On-chip charge pump output
  Output for an external charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16-pin SSOP (Shrink Small Outline Package)

■ PACKAGE

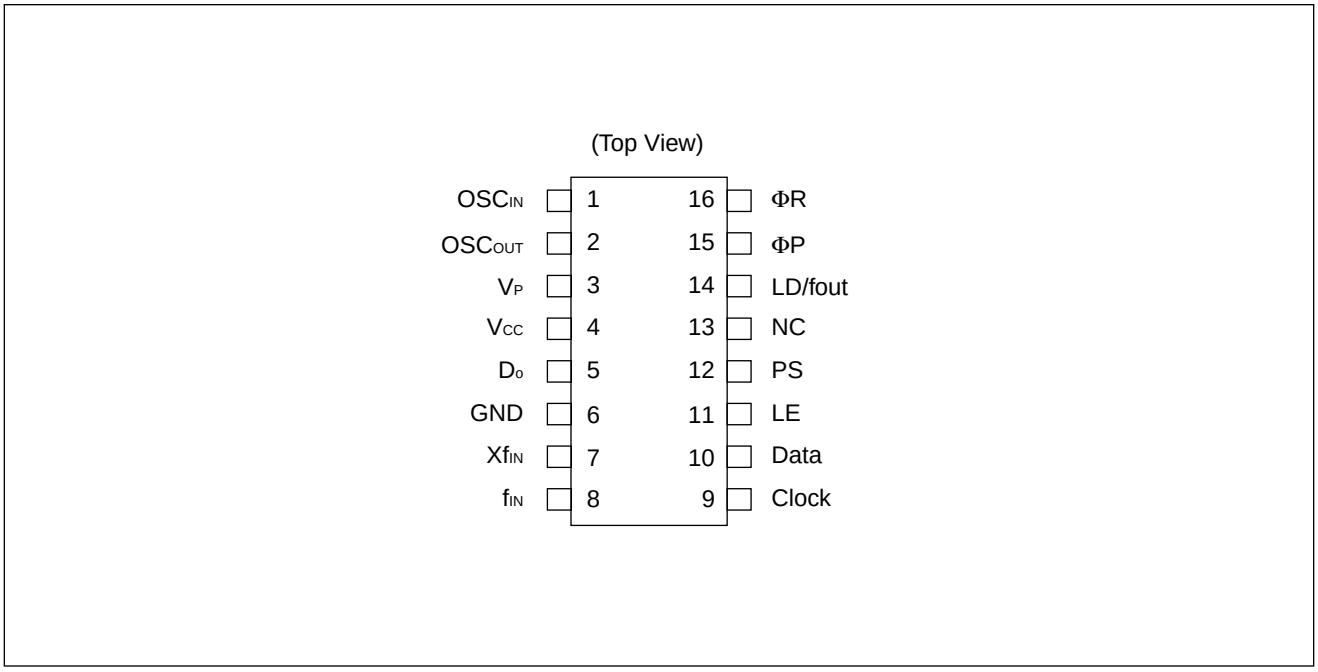
16-pin, Plastic SSOP



(FPT-16P-M05)

This device contains circuitry to protect the inputs against damage due to high static voltages or electroc fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

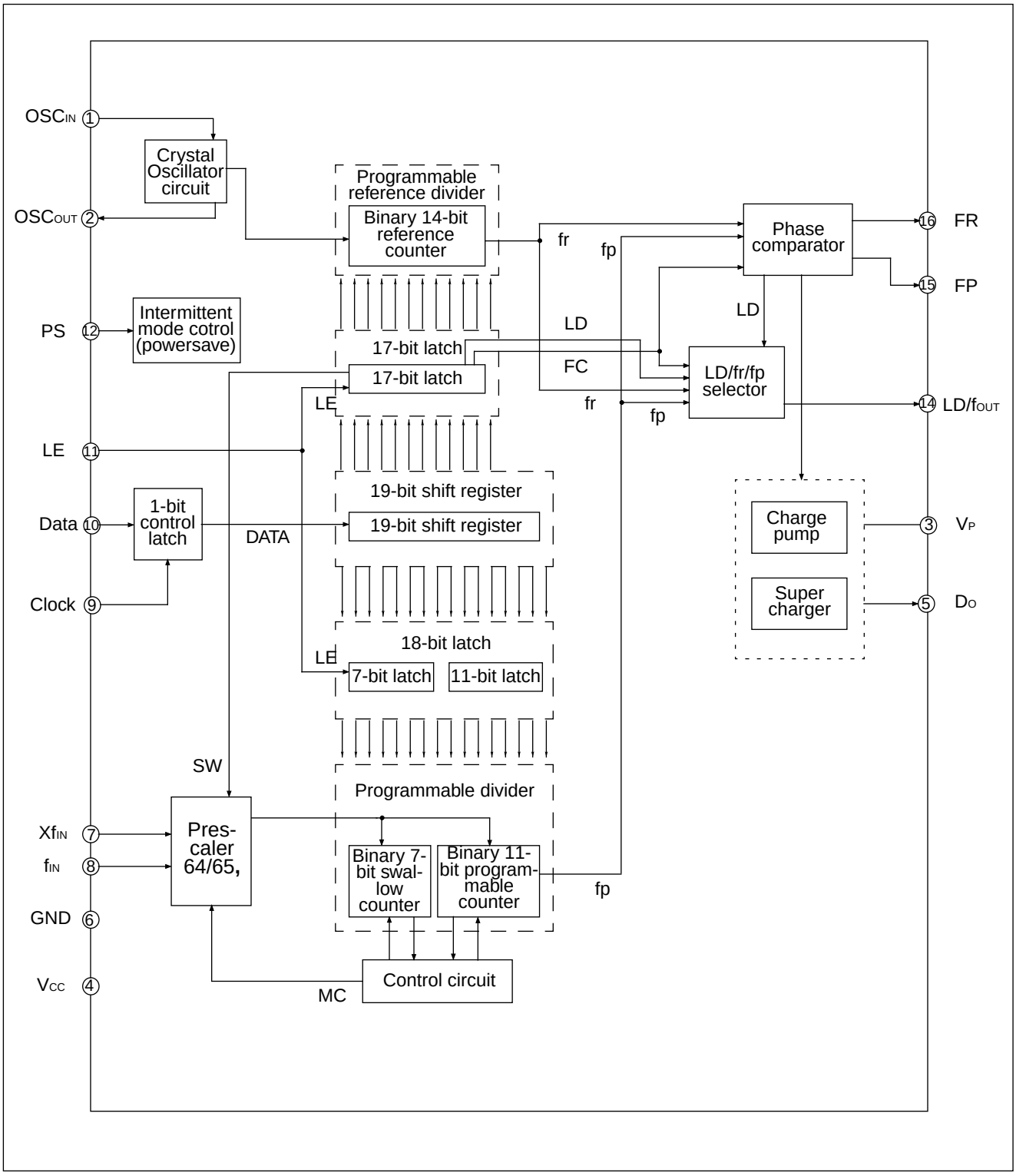
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Connection for external crystal or TCXO.
2	OSC_{OUT}	O	Oscillator output. Connection for the external crystal.
3	V_P	–	Power supply input for the charge pump.
4	V_{CC}	–	Power supply input.
5	D_O	O	Charge pump output. Phase of the charge pump can be reversed according FC input.
6	GND	–	Ground.
7	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8	fin	I	Prescaler input. Connection with an external VCO should be done AC coupled.
9	Clock	I	Clock input for 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. (Open is prohibited.)
10	Data	I	Serial data input using binary code. The last bit of the data is a control bit. (Open is prohibited.) Control bit = ”H” ; Data is transmitted to the 17-bit latch. Control bit = ”L” ; Data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input (Open is prohibited.) When LE is high, the data of the shift register are transferred to a latch, according to the control bit in the serial data.
12	PS	I	Power saving control input. This pin must be set at ”L” at Power-ON. (Open is prohibited.) PS = ”H” ; Normal mode PS = ”L” ; Power saving mode
13	NC	–	No connection.
14	LD/f_{OUT}	O	Lock detector output(LD)/Monitor pin of the phase comparator(fout). A LDS bit in a serial data switchs LD/fout pin’s output. LDS = ”H” ; outputs fout LDS = ”L” ; outputs LD
15	ΦP	O	Phase comparator output for an external charge pump. Phase of the output is reversed according to FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump. Phase of the output is reversed according to FC input. ΦR pin is a C-MOS output.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	–0.5 to +5.0	V	
	V_P	V_{CC} to 5.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	–0.5 to 6.0	V	ΦP
Output current	I_O	±10	mA	
Storage temperature	Tstg	–55 to +125	°C	

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_P	V_{CC}	–	5.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Power supply current (Power saving current)		I_{CC} (I_{PS})	–	7 (0.1)	–	mA	With f_{IN} = 1.2 GHz, OSC_{IN} = 12 MHz, V_{CC} = 3.0 V. In locked state.
Operating frequency	f_{IN}	f_{IN}	300	–	1200	MHz	AC coupling with a 1000pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	23	MHz	
Input sensitivity	f_{IN}	V_{IN}	–10	–	6	dBm	50Ω (refer to the test circuit.)
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp-p	
High-level input voltage	Data, Clock, LE, PS	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock, LE, PS	I_{IH}	–	–	1.0	mA	
Low-level input current		I_{IL}	–1.0	–	–	µA	
Input current	OSC_{IN}	I_{OSC}	–100	–	100	µA	
High-level output voltage	ΦR, LD	V_{OH}	2.1	–	–	V	Vcc = 3 V, I_{OH} = –1.0 mA
Low-level output voltage	ΦR, ΦP, LD	V_{OL}	–	–	0.4	V	Vcc = 3 V, I_{OL} = 1.0 mA
High-impedance cut off current	D_O, ΦP	I_{OFF}	–	–	0.3	µA	V_P = Vcc to 3.6 V V_{OOP} = GND to 6 V
Output current	ΦR, LD	I_{OH}	–1.0	–	–	mA	Vcc = 3 V
	ΦR, ΦP, LD	I_{OL}	–	–	1.0	mA	Vcc = 3 V
	D_O	I_{DOH}	–15	–	–5	mA	Vcc = 3 V, Vp = 5.0 V, V_{DOH} = 4.0 V
		I_{DOL}	6	–	18	mA	Vcc = 3 V, Vp = 5.0 V, V_{DOL} = 1.0 V

■ FUNCTION DESCRIPTIONS

Pulse Swallow Function

The devide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

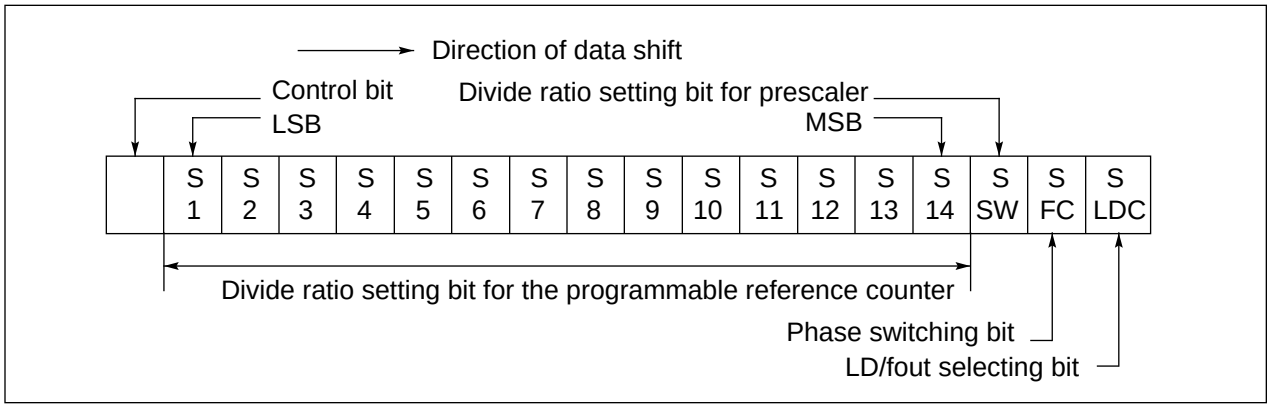
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 16-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high or open, stored data is latched depending on the control data as follows:

Control data	Destination of serial data
H	17 bit latch
L	18 bit latch

(a) Programmable reference divider
The programmable reference divider consists of a 17-bit latch and a 14-bit reference counter. The serial 18-bit data format is shown below:



- 14-bit programmable reference counter divide ratio

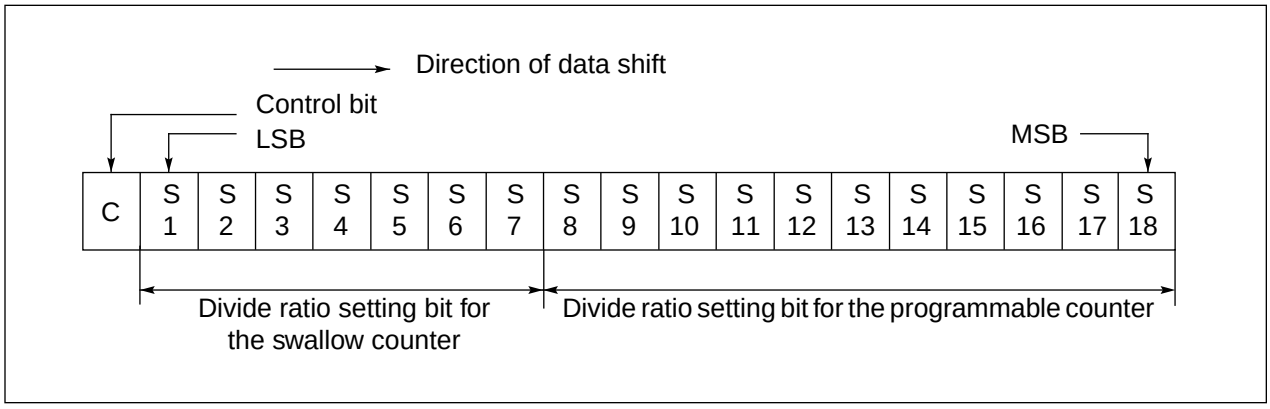
Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

Notes: 1. Divide ratios less than 6 are prohibited.
2. SW : This bit selects the divide ratio of the prescaler.
Low : 128 or 129
High: 64 or 65
3. LDS : This bit selects LD/fout pin output
High: outputs phase comparator monitoring signal(fout).
Low : outputs lock detecting signal(LD)
4. FC : This bit selects phase characteristics.
5. S1 to S14 : These bits select the divide ratio of the programmable reference counter (6 to 16,383).
6. C : Control bit: Set high.
7. Start data input with MSB first.

(b) Programmable divider

The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

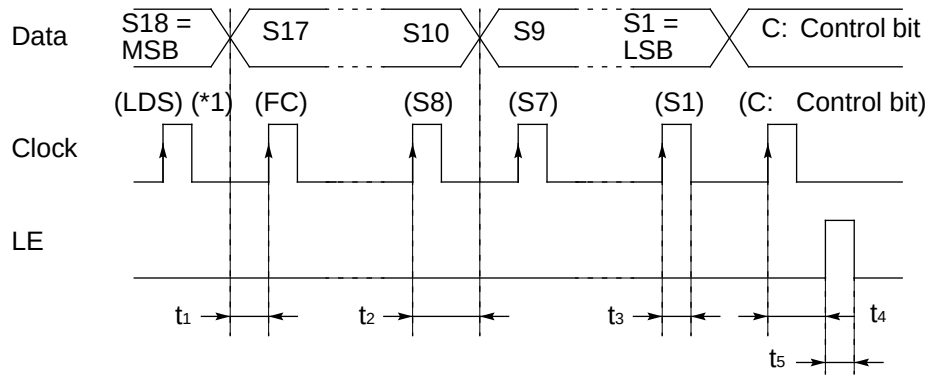
Divide ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

Notes: 1. Divide ratios less than 5 are prohibited for 11-bit programmable counter.
2. S1 to S7 : These bits select the divide ratio of swallow counter (0 to 127).
3. S8 to S18 : These bits select the divide ratio of programmable counter (5 to 2,047).
4. C : Control bit: (Set low)
5. Start data input with MSB first.

Serial Data Input Timing

- t_1 (≥ 100ns) : Data setup time t_2 (≥ 1000ns) : Data hold time t_3 (≥ 300ns) : Clock pulse width
  t_4 (≥ 100ns) : LE setup time to the rising edge of last clock t_5 (≥ 790ns) : LE pulse width



*1: Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Power Saving Mode (Intermittent operation control circuit)

Setting PS pin to Low, MB15A16 enters into power saving mode resultantly current consumption can be limited to 100µA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. The power consumption can be reduced by the intermittent operation that powering down or waking up parts of the PLL circuitry. If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

Note: PS pin must be set ”L” at Power-ON

Relation Between the FC Input and Phase Characteristics

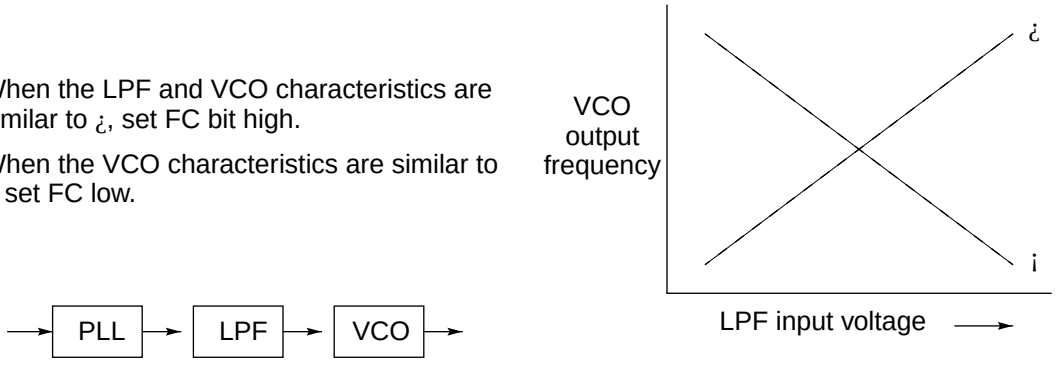
The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (Do) and the phase comparator output (ΦR, ΦP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of D_O, ΦR, and ΦP is shown below.

	FC = High				**FC = Low**			
	Do	ΦR	ΦP	fout	Do	ΦR	ΦP	fout
$f_r > f_p$	H	L	L	(fr)	L	H	Z(*1)	(fp)
$f_r < f_p$	L	H	Z(*1)	(fr)	H	L	L	(fp)
$f_r = f_p$	Z(*1)	L	Z(*1)	(fr)	Z(*1)	L	Z(*1)	(fp)

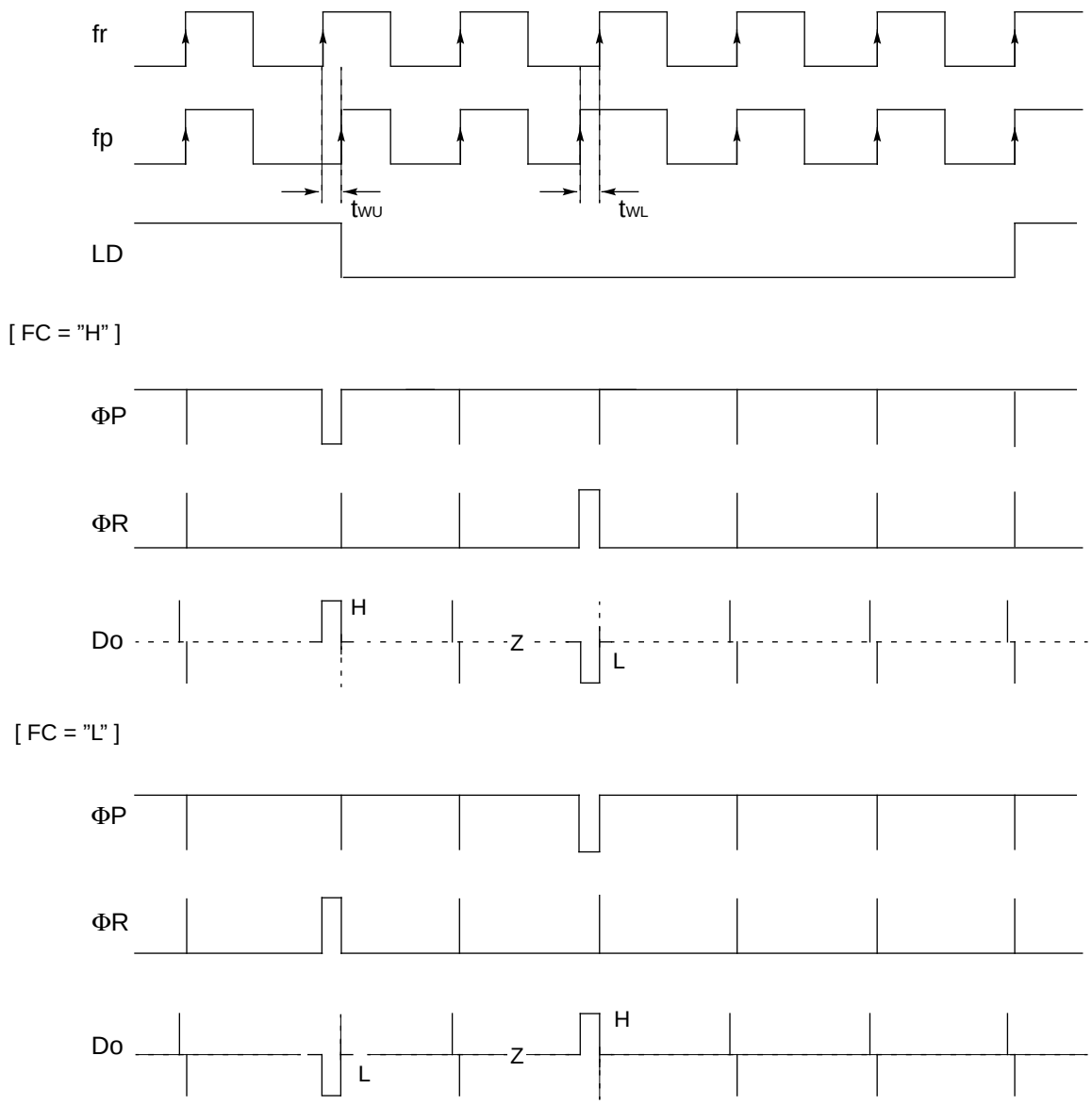
*1: High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

* : When the LPF and VCO characteristics are similar to ¿, set FC bit high.
* : When the VCO characteristics are similar to ¡, set FC low.

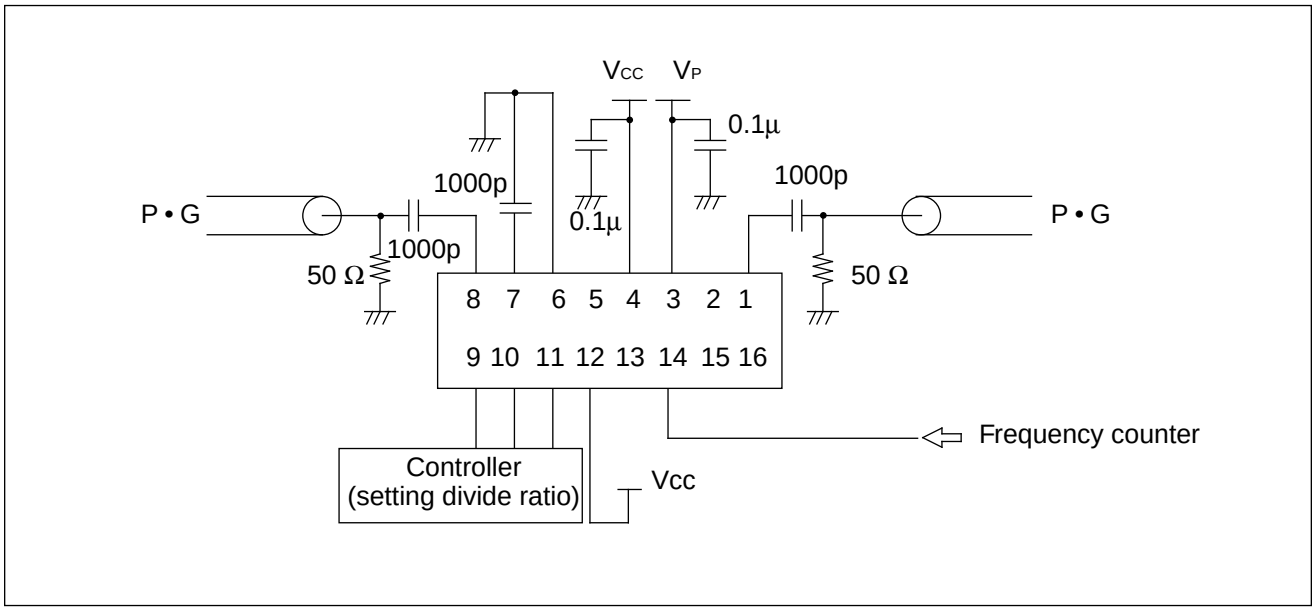


Phase Comparator Output Waveforms



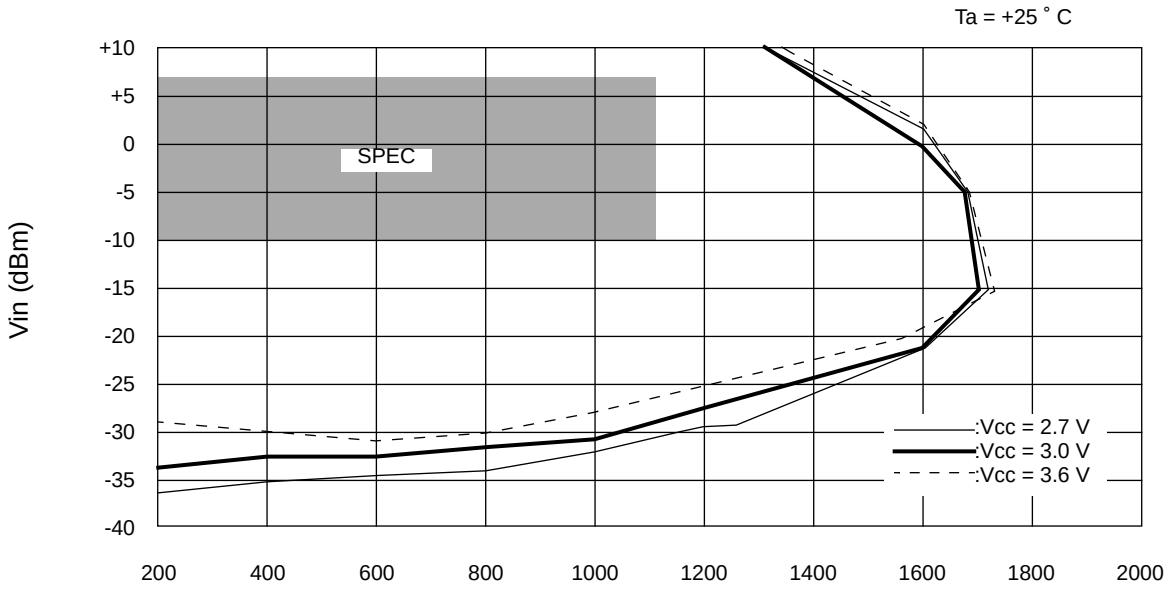
Notes: 1. Phase difference detection range: -2π to $+2\pi$
2. LD output becomes low when phase is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
3. t_{WU} and t_{WL} depend on OSCin input frequency.
   $t_{WU} \leq 8/fosc$ (e. g. $t_{WU} \leq 625ns$, foscin = 12.8 MHz)
   $t_{WL} \geq 16/fosc$ (e. g. $t_{WL} \geq 1250ns$, foscin = 12.8 MHz)

■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)

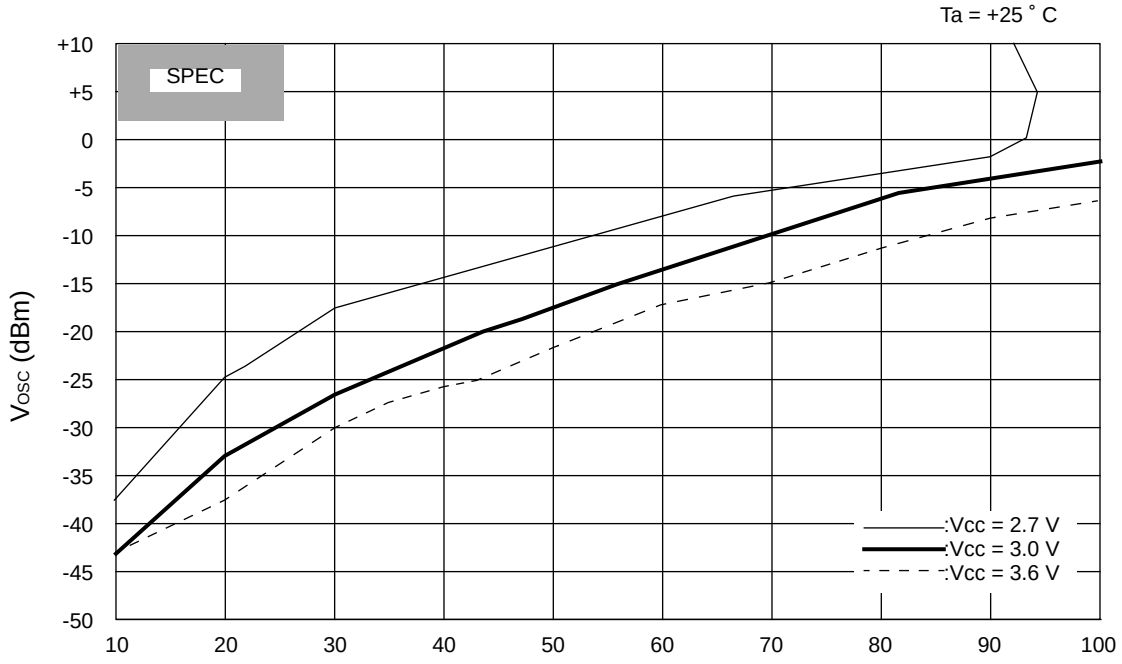


■ TYPICAL CHARACTERISTICS

Input Sensitivity (fin Pin)



Input Sensitivity (OSCin Pin)



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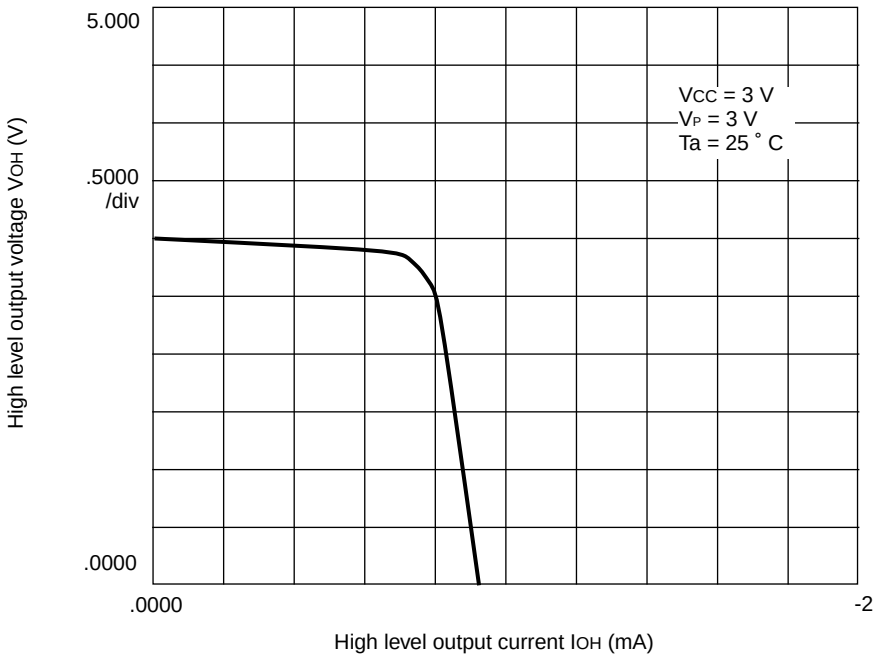
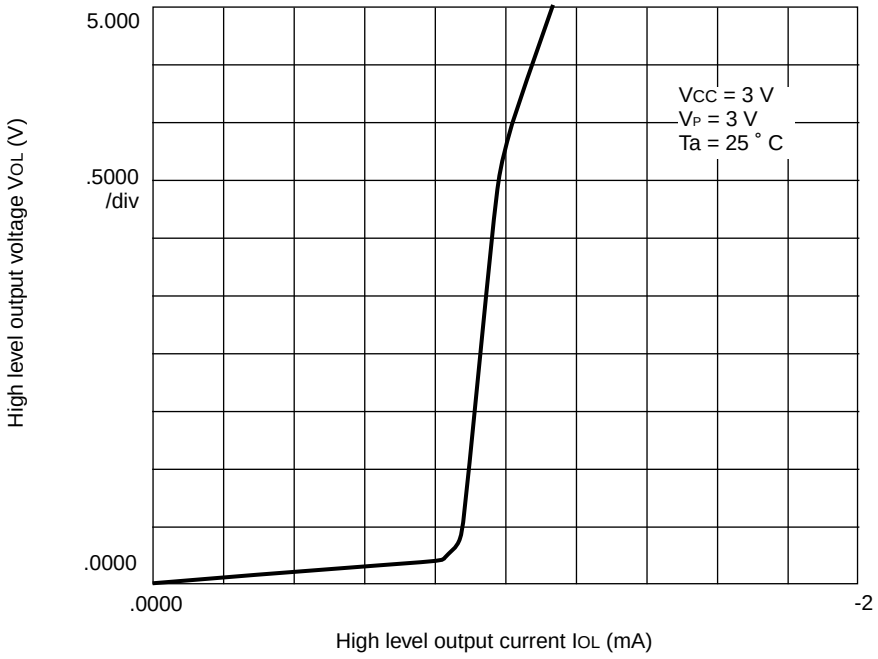
Charge Pump Current vs. Voltage (Do Pin)

I_{OH} vs V_{OH} characteristics



V_{OH} vs I_{OH} characteristics



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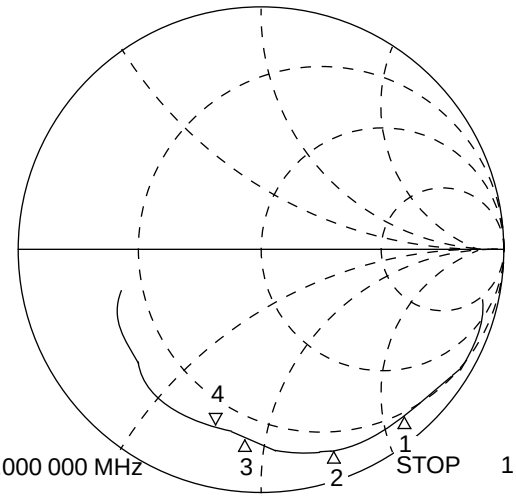
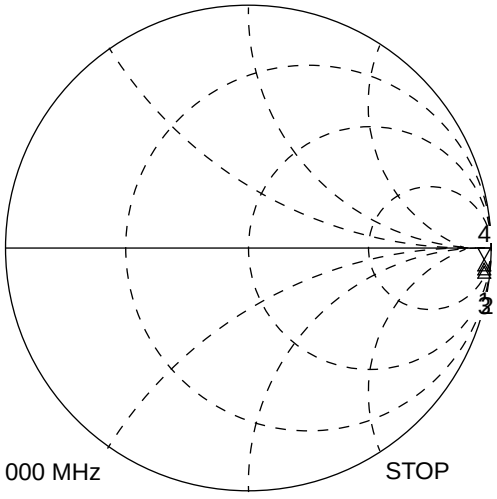
Input Impedance

Input Impedance

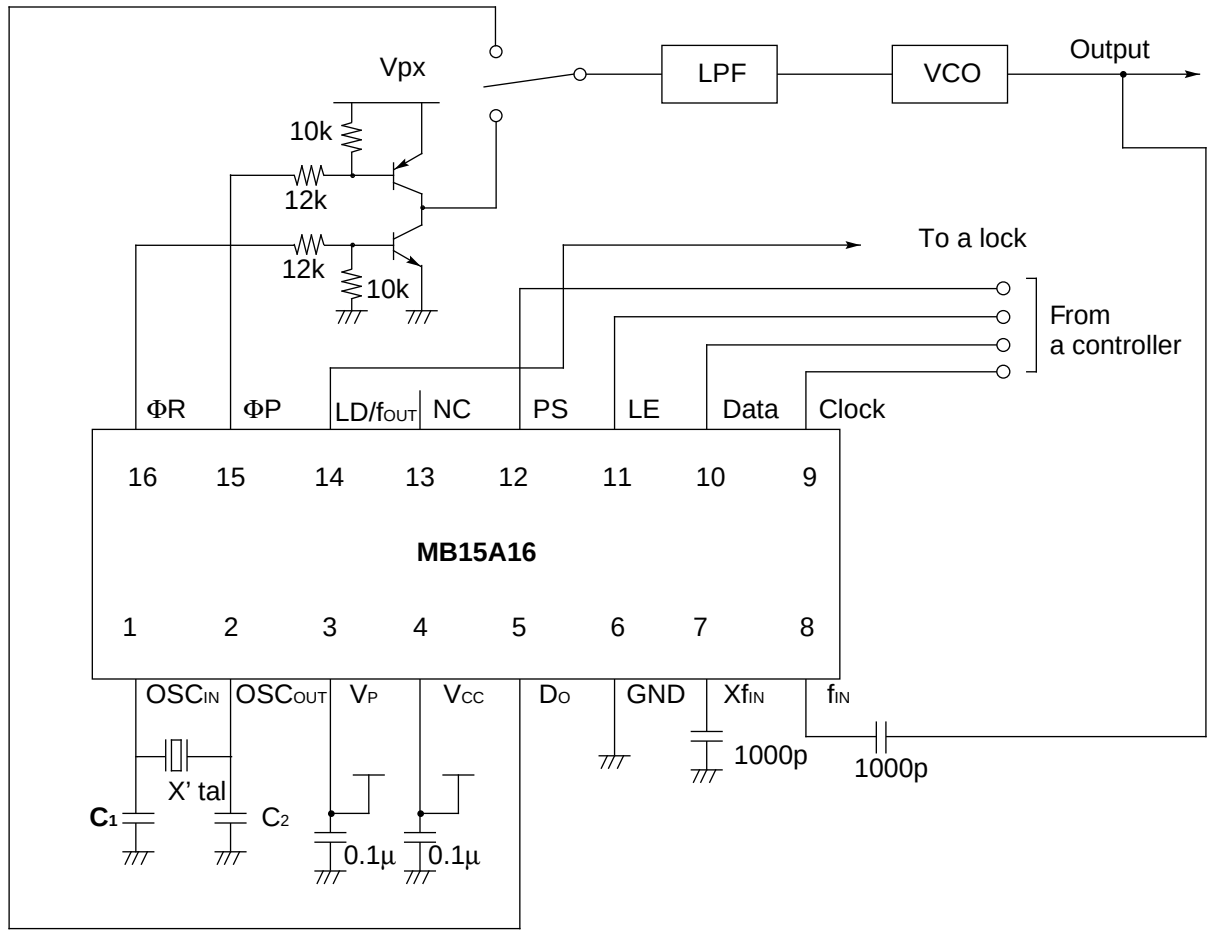
fin_{RF} Pin



OSCin Pin



■ APPLICATION EXAMPLE

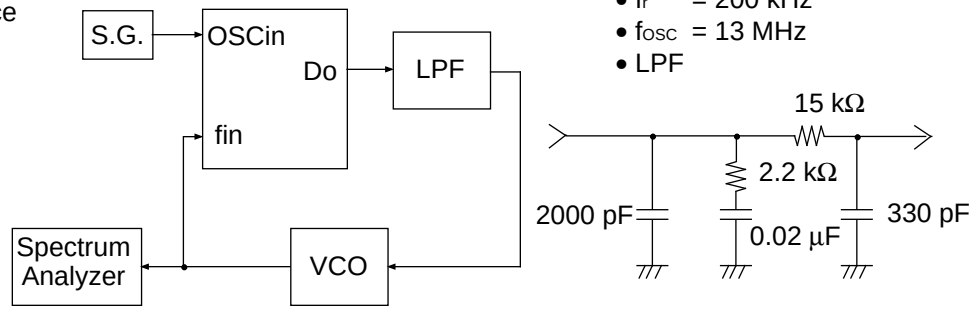


V_{PX} : Maximum 6 V
C_1, C_2 : Depend on the crystal parameters
ΦP : N-ch open drain output
ΦR : C-MOS output

■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plots shows lock up time, phase noise, and reference leakage.

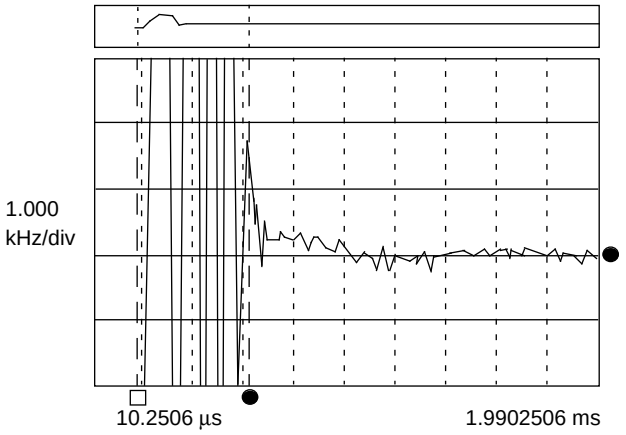
Test Circuit



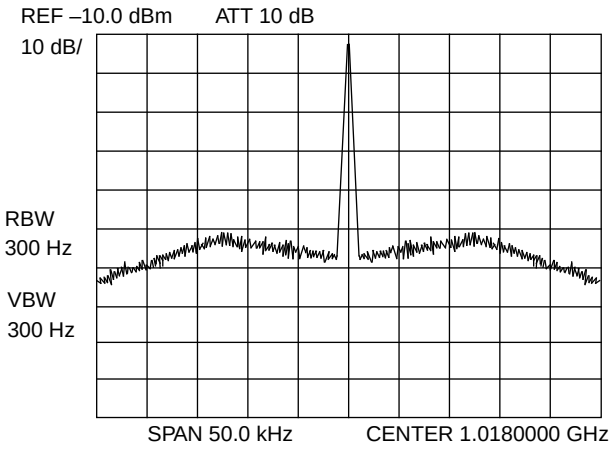
- f_{VCO} = 1018 MHz
- K_V = 20 MHz/V
- f_r = 200 kHz
- f_{OSC} = 13 MHz
- LPF

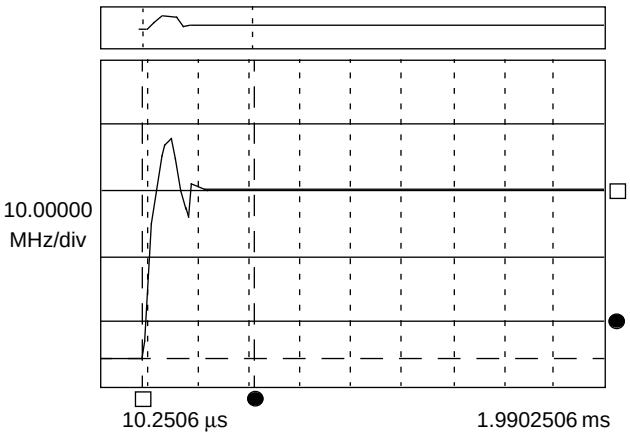
PLL Lock Up Time

1005.000MHz → 1031.000MHz, within ± 1kHz
Lch → Hch 420µs

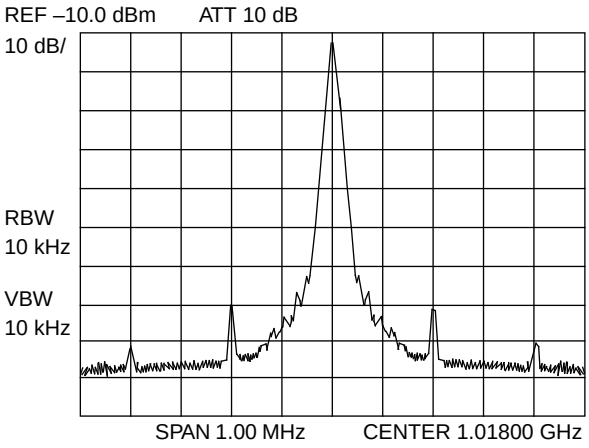


PLL Phase Noise
@ within loop band = 74dBc/Hz





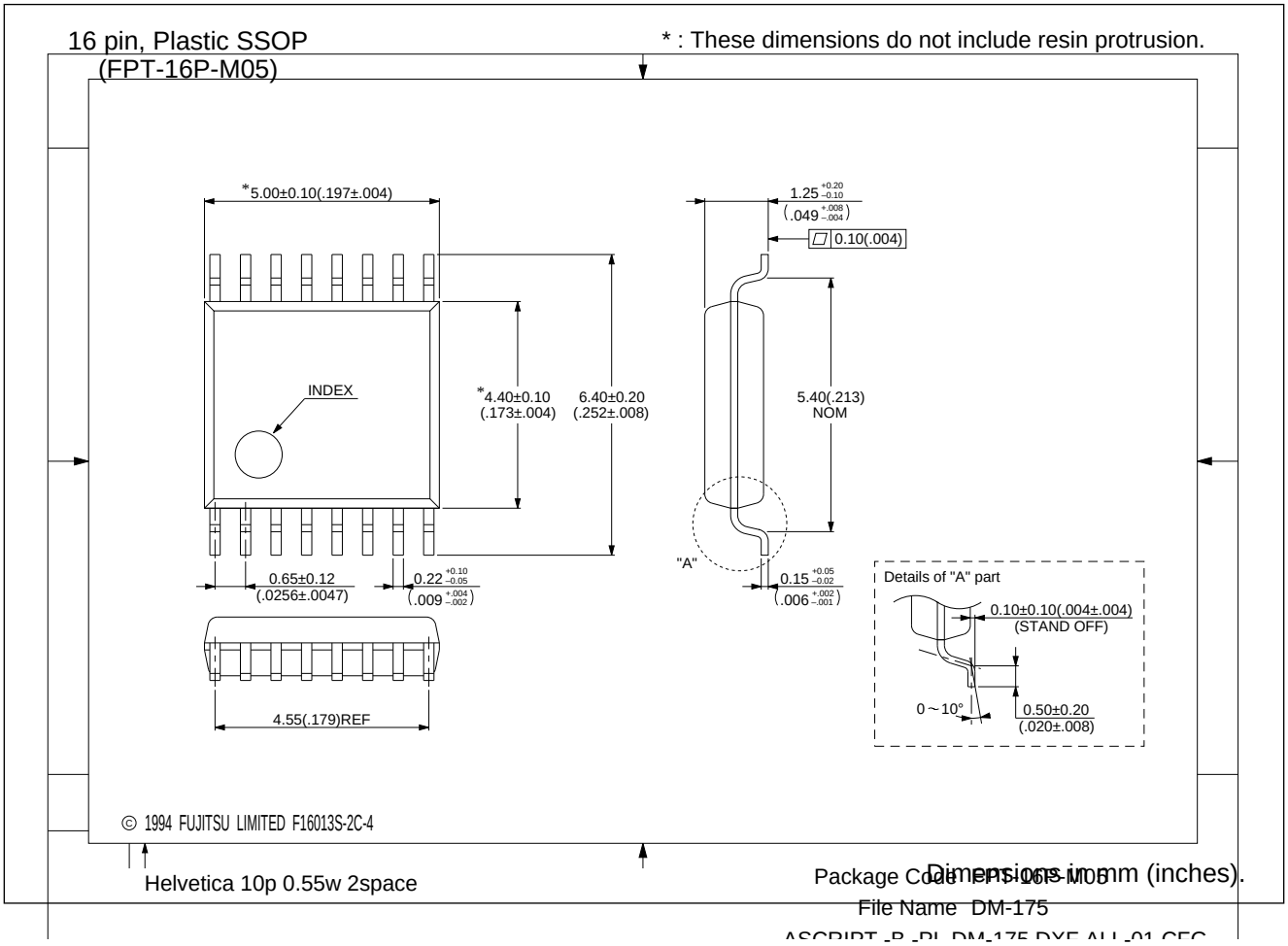
PLL Reference Leakage
@ 200kHz offset = 68dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15A16 PFV	16-pin Plastic SSOP (FPT-16P-M05)	

■ PACKAGE DIMENTION



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