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FUJITSU

PRODUCT PROFILE SHEET

MB85343C-60/-70

CMOS 1M x 32 Hyper Page Mode DRAM Module

CMOS 1,048,576 x 32 Bit Hyper Page Mode DRAM Module

The Fujitsu MB85343C is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of eight MB814405C devices. The MB85343C is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85343C are the same as the MB814405C which features hyper page mode operation providing extended valid time for data output and higher speed random access of upto 1,024 x 32bits of data within the same row than the fast page mode. For ease of memory expansion, the MB85343C is offered in a 72–pad Single In–line Memory Module package (SIMM).

Parameter		MB85343C-60	MB85343C-70
$\overline{RAS}$ Access Time		60ns max.	70ns max.
Random Cycle Time		104ns min.	119ns min.
Address Access Time		30ns max.	35ns max.
$\overline{CAS}$ Access Time		15ns max.	20ns max.
Hyper Page Mode Cycle Time		25ns min.	30ns min.
Power Dissipation	Operating Mode	2688mW max.	2376mW max.
	Hyper Page Mode	2904mW max.	2424mW max.
	Standby Mode	88mW max.	88mW max.
	Self Refresh Mode	44mW max.	44mW max.

- Organization : 1,048,576 words x 32 bits
- Memory : MB814405C, 8 pcs
- Decoupling Capacitor : 8 pcs
- 5.0V ± 10% Supply Voltage
- 1,024 Refresh Cycles / 16.4ms
- Hyper page mode operation (EDO)
- Package and Ordering Information:
  72–pad SIMM, order as
  MB85343C–xxPJPBK
  (PJPBK = Gold Pad)
  MB85343C–xxPJPB
  (PJPB = Solder Pad)

ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8	W
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

See page 7.
MSS–72P–P29

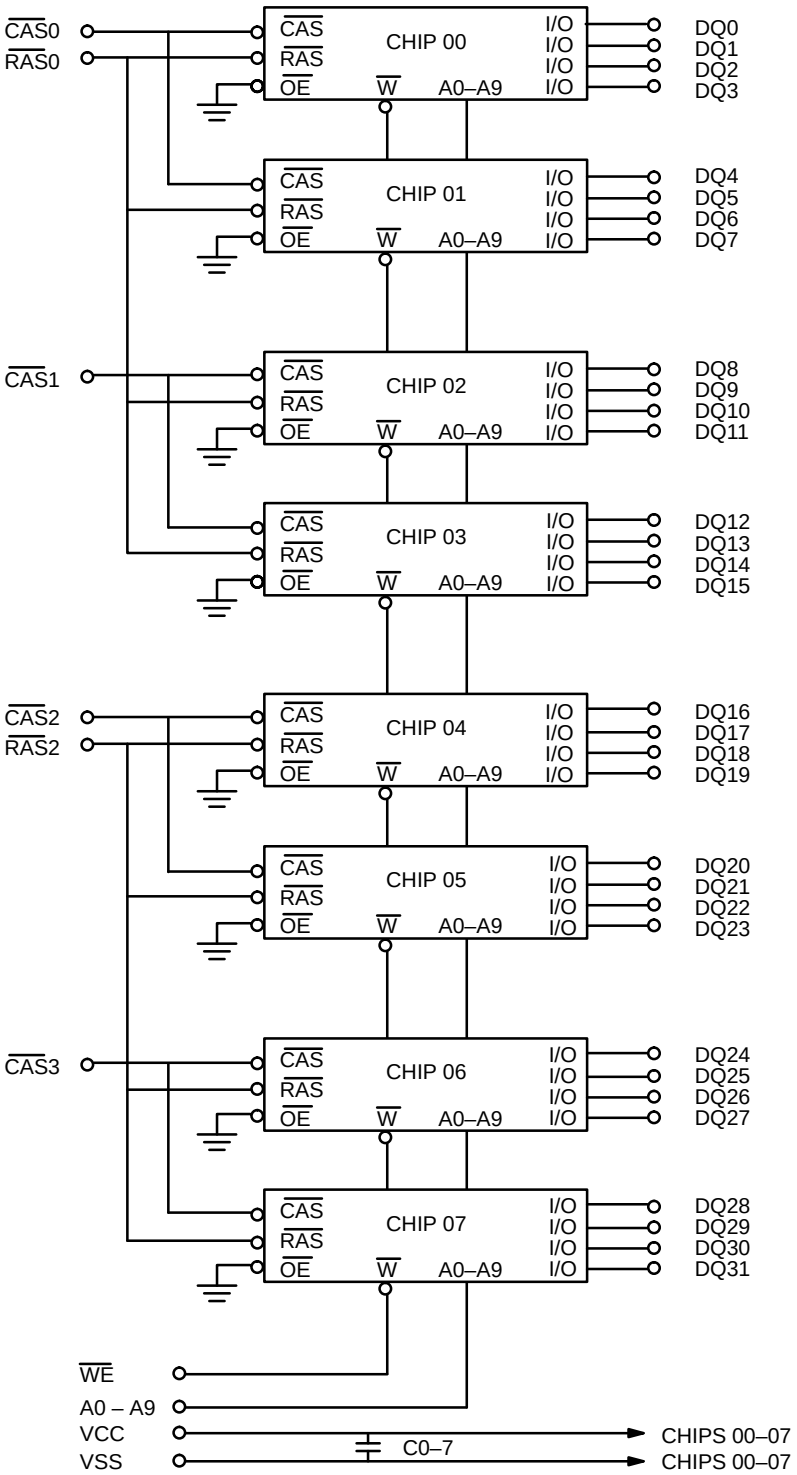
See page 8.
MSS–72P–P48

DQ0	2	1	VSS
DQ1	4	3	DQ16
DQ2	6	5	DQ17
DQ3	8	7	DQ18
VCC	10	9	DQ19
A0	12	11	NC
A2	14	13	A1
A4	16	15	A3
A6	18	17	A5
DQ4	20	19	NC
DQ5	22	21	DQ20
DQ6	24	23	DQ21
DQ7	26	25	DQ22
A7	28	27	DQ23
VCC	30	29	NC
A9	32	31	A8
$\overline{RAS}$2	34	33	NC
NC	36	35	NC
NC	38	37	NC
$\overline{CAS}$0	40	39	VSS
$\overline{CAS}$3	42	41	$\overline{CAS}$2
$\overline{RAS}$0	44	43	$\overline{CAS}$1
NC	46	45	NC
NC	48	47	$\overline{WE}$
DQ24	50	49	DQ8
DQ25	52	51	DQ9
DQ26	54	53	DQ10
DQ27	56	55	DQ11
DQ28	58	57	DQ12
DQ29	60	59	VCC
DQ30	62	61	DQ13
DQ31	64	63	DQ14
NC	66	65	DQ15
PD2	68	67	PD1
PD4	70	69	PD3
VSS	72	71	NC

Pin #	Symbol	-60	-70
67	PD1	V_{SS}	V_{SS}
68	PD2	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}
70	PD4	NC	NC

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}		0		V
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V
Input Low Voltage, all inputs *	V_{IL}	–0.3		0.8	V
Ambient Temperature	T_A	0		70	°C

Note: * Undershoots of up to –2.0volts with a pulse width not exceeding 20ns are acceptable.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Test Condition	Symbol	Min	Max	Unit
Output High Voltage *1		I_{OH} = –5mA	V_{OH}	2.4		V
Output Low Voltage *1		I_{OL} = 4.2mA	V_{OL}		0.4	V
Input Leakage Current	$\overline{RAS}$	0V ≤ V_{IN} ≤ 5.5V, 4.5V ≤ V_{CC} ≤ 5.5V, V_{SS} = 0V, all other pins not under test = 0V	$I_{I(L)}$	–30	30	µA
	$\overline{CAS}$			–20	20	
	Address, $\overline{WE}$			–60	60	
Output Leakage Current		0V ≤ V_{OUT} ≤ 5.5V, Data out disabled	$I_{O(L)}$	–10	10	µA
Operating Current *2 (Average power supply current)	MB85343C-60	$\overline{RAS}$ & $\overline{CAS}$ cycling, t_{RC} = min.	I_{CC1}		488	mA
	MB85343C-70				432	
Standby Current (Power supply current)	TTL Level	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	I_{CC2}		16	mA
	CMOS Level	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC}–0.2V			8	
Refresh Current #1 *2 (Average power supply current)	MB85343C-60	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, t_{RC} = min.	I_{CC3}		488	mA
	MB85343C-70				432	
Hyper Page Mode Current *2	MB85343C-60	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{HPC} = min.	I_{CC4}		528	mA
	MB85343C-70				440	
Refresh Current #2 *2 (Average power supply current)	MB85343C-60	$\overline{RAS}$ = cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min.	I_{CC5}		392	mA
	MB85343C-70				352	
Refresh Current #3 (Average power supply current)	MB85343C-60	$\overline{RAS}$ = $\overline{CAS}$ ≤ 0.2V, Self refresh	I_{CC9}		8	mA
	MB85343C-70				8	

Notes: *1 Referenced to V_{SS}.

*2 I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > –0.3V.
I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC4} is specified at one time of address change during one Page cycle.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9	C_{IN1}	—	61	pF
Input Capacitance, $\overline{RAS}$0 and $\overline{RAS}$2	C_{IN2}	—	34	pF
Input Capacitance, $\overline{CAS}$0 to $\overline{CAS}$3	C_{IN3}	—	23	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	55	pF
I/O Capacitance, (DQ0-31)	C_{DQ}	—	11	pF

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85343C-60		MB85343C-70		Unit	Notes
			Min	Max	Min	Max		
1	Time Between Refresh	tREF	—	16.4	—	16.4	ms	
2	Random Read/Write Cycle Time	tRC	104	—	119	—	ns	
3	Access Time from $\overline{RAS}$	tRAC	—	60	—	70	ns	**4, 7**
4	Access Time from $\overline{CAS}$	tCAC	—	15	—	20	ns	**5, 7**
5	Column Address Access Time	tAA	—	30	—	35	ns	**6, 7**
6	Output Hold Time	tOH	5	—	5	—	ns	
7	Output Hold Time from $\overline{CAS}$	tOHC	5	—	5	—	ns	
8	Output Buffer Turn On Delay Time	tON	0	—	0	—	ns	
9	Output Buffer Turn Off Delay Time	tOFF	—	15	—	15	ns	**8**
10	Output Buffer Turn Off Delay Time from $\overline{RAS}$	tOFR	—	15	—	15	ns	**8**
11	Transition Time	tT	1	50	1	50	ns	
12	$\overline{RAS}$ Precharge Time	tRP	40	—	45	—	ns	
13	$\overline{RAS}$ Pulse Width	tRAS	60	100000	70	100000	ns	
14	$\overline{RAS}$ Hold Time	tRSH	15	—	20	—	ns	
15	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	0	—	0	—	ns	
16	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	50	ns	**9, 10**
17	$\overline{CAS}$ Pulse Width	tCAS	10	10000	10	10000	ns	
18	$\overline{CAS}$ Hold Time	tCSH	40	—	50	—	ns	
19	$\overline{CAS}$ Precharge Time (Normal)	tCPN	10	—	10	—	ns	**15**
20	Row Address Setup Time	tASR	0	—	0	—	ns	
21	Row Address Hold Time	tRAH	10	—	10	—	ns	
22	Column Address Setup Time	tASC	0	—	0	—	ns	
23	Column Address Hold Time	tCAH	10	—	10	—	ns	
24	$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	**11**
25	Column Address to $\overline{RAS}$ Lead Time	tRAL	30	—	35	—	ns	
26	Column Address to $\overline{CAS}$ Lead Time	tCAL	23	—	28	—	ns	
27	Read Command Setup Time	tRCS	0	—	0	—	ns	
28	Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	—	0	—	ns	**12**
29	Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	—	0	—	ns	**12**
30	Write Command Setup Time	tWCS	0	—	0	—	ns	**13**
31	Write Command Hold Time	tWCH	10	—	10	—	ns	
32	$\overline{WE}$ Pulse Width	tWP	10	—	10	—	ns	
33	Write Command to $\overline{RAS}$ Lead Time	tRWL	15	—	18	—	ns	
34	Write Command to $\overline{CAS}$ Lead Time	tCWL	10	—	10	—	ns	
35	DIN Setup Time	tDS	0	—	0	—	ns	
36	DIN Hold Time	tDH	10	—	10	—	ns	

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85343C-60		MB85343C-70		Unit	Notes
			Min	Max	Min	Max		
37	Data Hold Time from $\overline{RAS}$	tDHR	50	—	55	—	ns	
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	tRPC	5	—	5	—	ns	
39	$\overline{CAS}$ Setup Time (C–B–R Refresh)	tCSR	0	—	0	—	ns	
40	$\overline{CAS}$ Hold Time (C–B–R Refresh)	tCHR	10	—	10	—	ns	
41	$\overline{WE}$ Setup Time from $\overline{RAS}$	tWSR	0	—	0	—	ns	**17**
42	$\overline{WE}$ Hold Time from $\overline{RAS}$	tWHR	10	—	10	—	ns	**17**
43	DIN to $\overline{CAS}$ Delay Time	tDZC	0	—	0	—	ns	
44	$\overline{WE}$ to Data In Delay Time	tWED	15	—	15	—	ns	
45	$\overline{RAS}$ to Data In Delay Time	tRDD	15	—	15	—	ns	
46	$\overline{CAS}$ to Data in Delay Time	tCDD	15	—	15	—	ns	
47	$\overline{RAS}$ to Column Address Hold Time	tAR	26	—	26	—	ns	
48	Write Command Hold time Referenced to $\overline{RAS}$	tWCR	24	—	24	—	ns	
49	Data Input Hold Time Referenced to $\overline{RAS}$	tDHR	24	—	24	—	ns	
50	Hyper Page Mode $\overline{RAS}$ Pulse Width	tRASP	—	200000	—	200000	ns	
51	Hyper Page Mode Read/Write Cycle Time	tHPC	25	—	30	—	ns	
52	Access Time from $\overline{CAS}$ Precharge	tCPA	—	35	—	40	ns	**7, 14**
53	Hyper Page Mode $\overline{CAS}$ Precharge Time	tCP	10	—	10	—	ns	
54	Hyper Page Mode $\overline{RAS}$ Hold Time from CAS Precharge	tRHCP	35	—	40	—	ns	
55	$\overline{RAS}$ Pulse Width for Self Refresh	tRASS	100	—	100	—	µs	**16**
56	$\overline{RAS}$ Precharge Time for Self Refresh	tRPS	104	—	119	—	ns	**16**
57	$\overline{CAS}$ Hold time for Self refresh	tCHS	–50	—	–50	—	ns	**16**

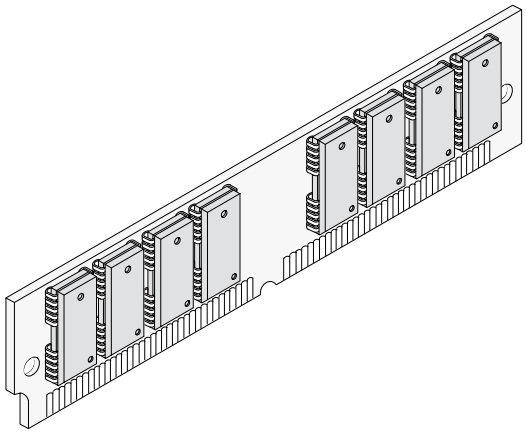
Notes:

1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles or eight $\overline{CAS}$ – before–$\overline{RAS}$ refresh cycles ($\overline{WE}$ = V_{IH}) before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$ – before–$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.
2. AC characteristics assume t_T = 2ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} and/or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} – t_{CAC} – t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} – t_{CAC} – t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} and t_{OFR} are specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min).
11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
14. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} become long, t_{CPA} also become longer than t_{CPA} (max).
15. Assumes $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle.
16. Assumes $\overline{CAS}$ -before- $\overline{RAS}$ self refresh cycle.
17. Assumes test mode function.

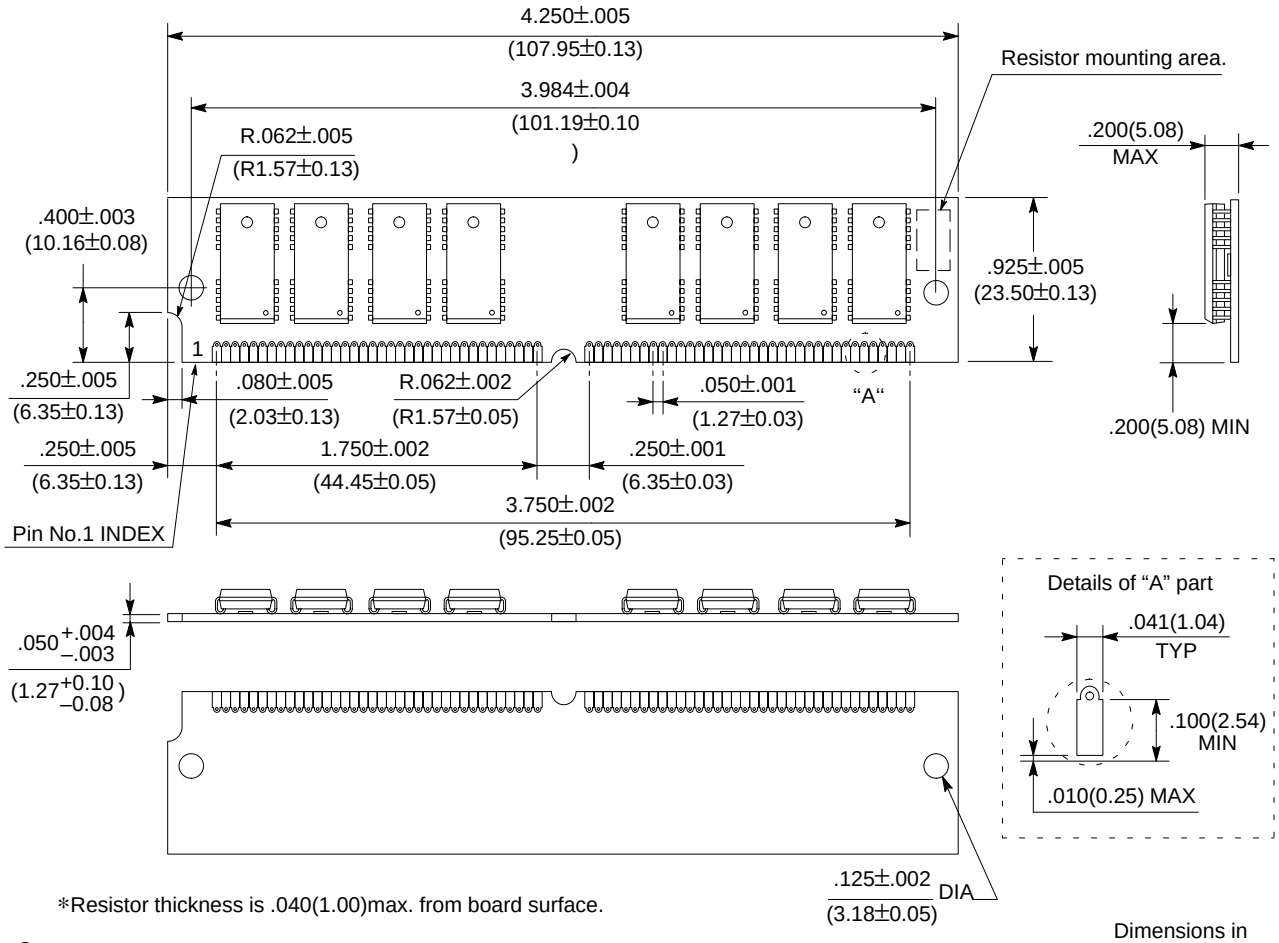
*Source: See MB814405C Data Sheet for details on the electricals.

PACKAGE DIMENSIONS

(Suffix: PJPBK)



72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P29)

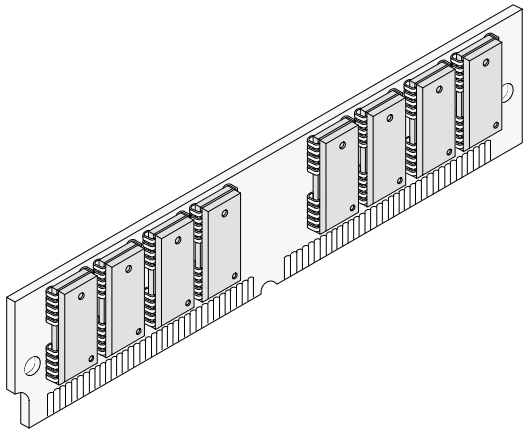


*Resistor thickness is .040(1.00)max. from board surface.

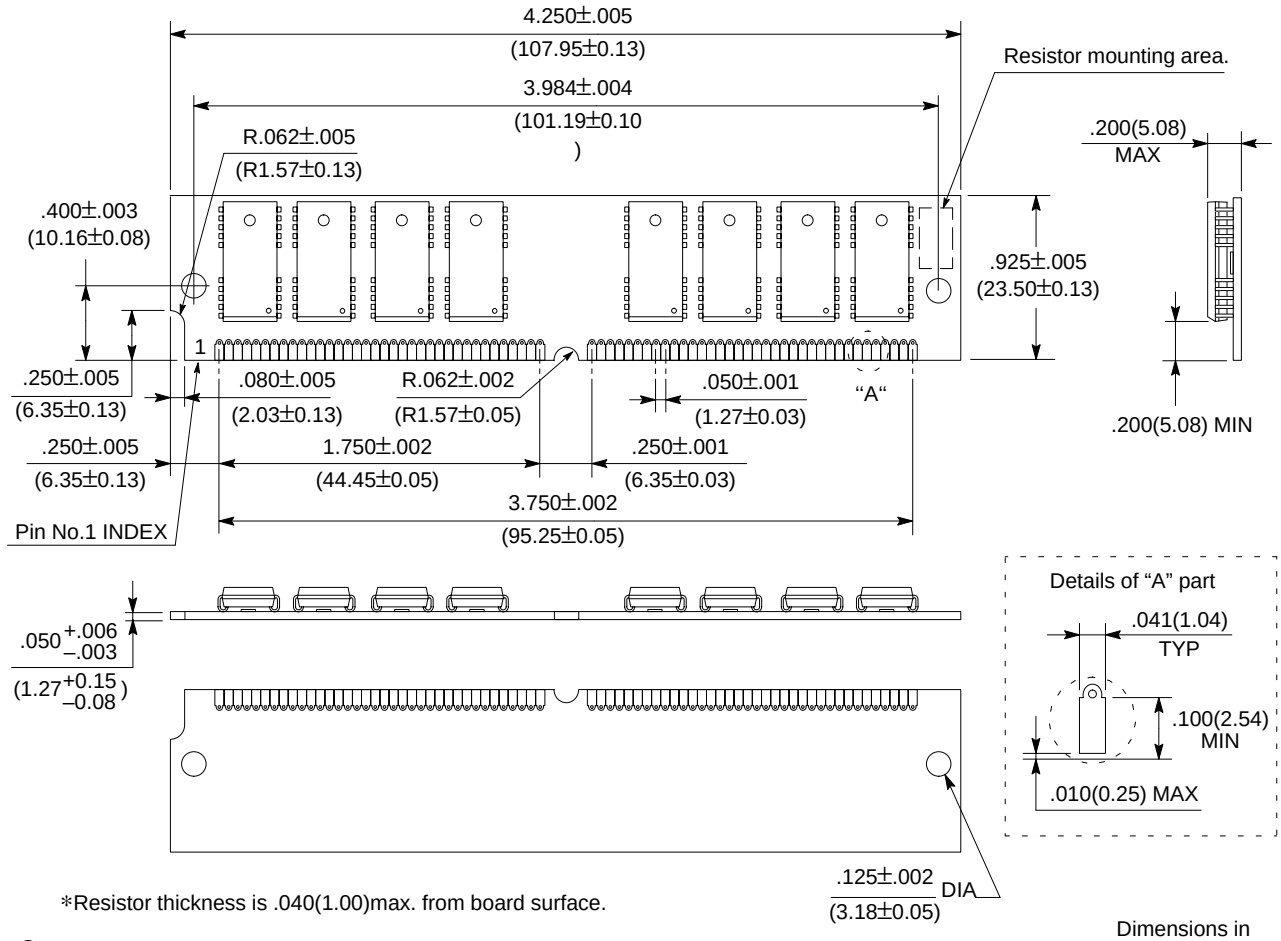
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PJPB)



72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P48)



*Resistor thickness is .040(1.00)max. from board surface.

Dimensions in
inches (millimeters)