July 1994
Edition 2.0

FUJITSU

DATA SHEET

FPF21C8060UA-92
FULL COLOR PLASMA DISPLAY

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DESCRIPTION

The Fujitsu plasma display unit consists of an AC-type gas discharge plasma panel with memory function based on Fujitsu's unique panel technologies and its driving circuit.

The black faced panel provides a clear image, even in high ambient lighting environments. The memory function provides an easy-to-view, flicker free screen, with the newly developed panel yielding a high brightness display.

FEATURES

- High brightness of 180 cd/m^2
- High contrast: 60 : 1
- Easy-to-use flicker free display
- Easy-to-use interface conforming to digital VGA interface
- UL 1950 Recognized

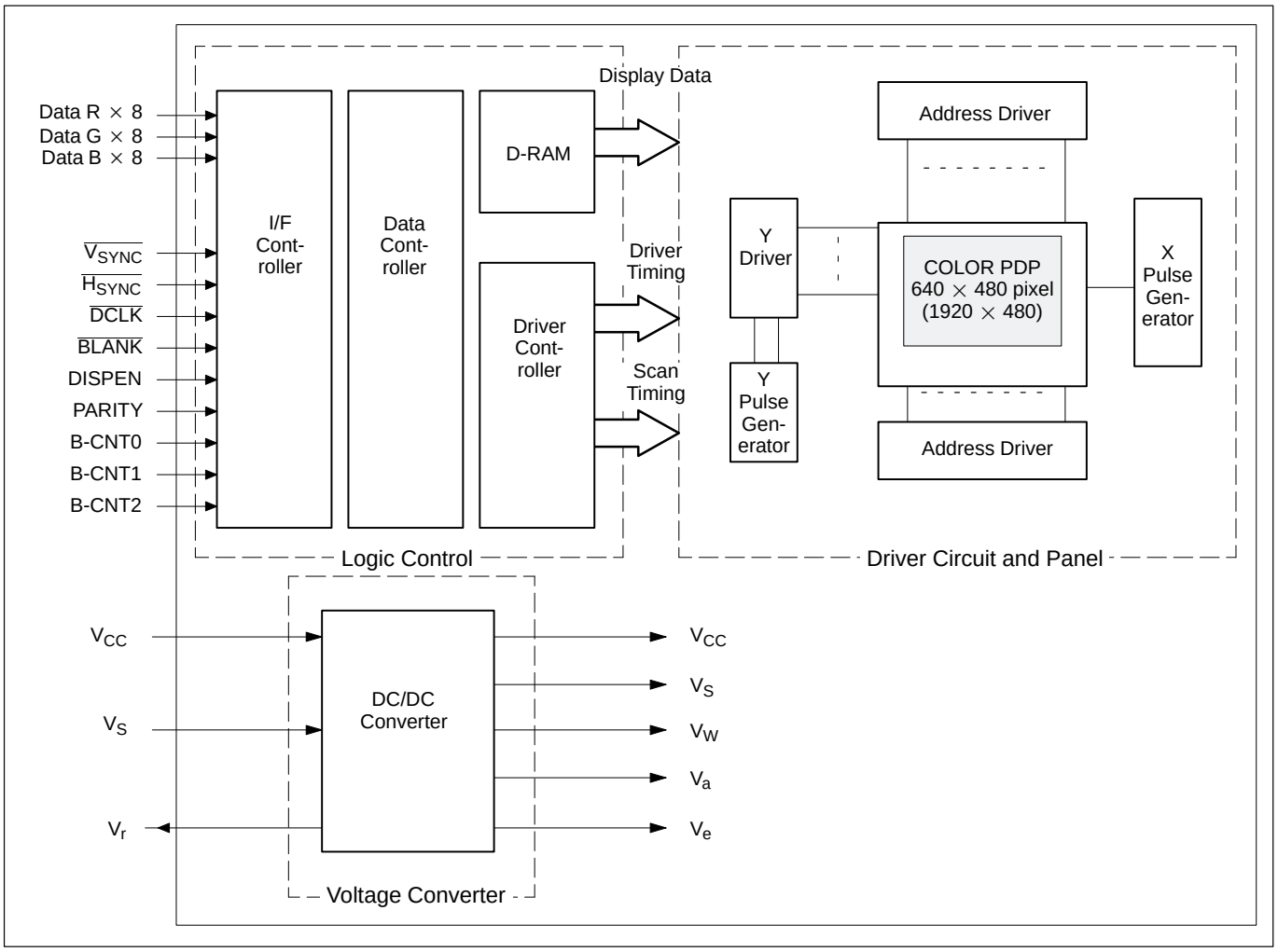


Figure 1. Block Diagram of Display

SPECIFICATIONS

DISPLAY PERFORMANCE

No.	Item	Rating
1	Display Pixels	Horizontal 640 × Vertical 480 (1 pixel = 3RGB cells)
2	Display Cells	Horizontal 1920 × Vertical 480 cells
3	Pixel Pitch	Horizontal 0.66mm × Vertical 0.66mm
4	Cell Pitch	Horizontal 0.22mm × Vertical 0.66mm
5	Display Pixel Type	RGB Stripe (shown in Figure 2)
6	Effective Display Size	Horizontal 423mm × Vertical 316mm (21” to corners) {16.65” (H) × 12.44” (V)}
7	Number of Colors	260,000 (64 gradations of RGB)
8	Brightness[1] (Average brightness)	White: over 120cd/m^2 (display rate 25%, max. gradations setting, V_{sync} = 16.7msec.)
9	Contrast[2] (in dark room)	over 60:1 (Brightness at max. gradation 25% light/no light brightness)
10	Maximum Viewing Angle[3]	over 140°

NOTES:

1. Brightness is the average of the 9 points, which are uniformly arranged on the panel display area. (Total display rate: 25%, max. gradation.)
2. Contrast is calculated from the display brightness and the non-display brightness is calculated from the values in note 1. Contrast = average brightness/non-display brightness.
3. Viewing angle is the critical angle at which characters can still be read.

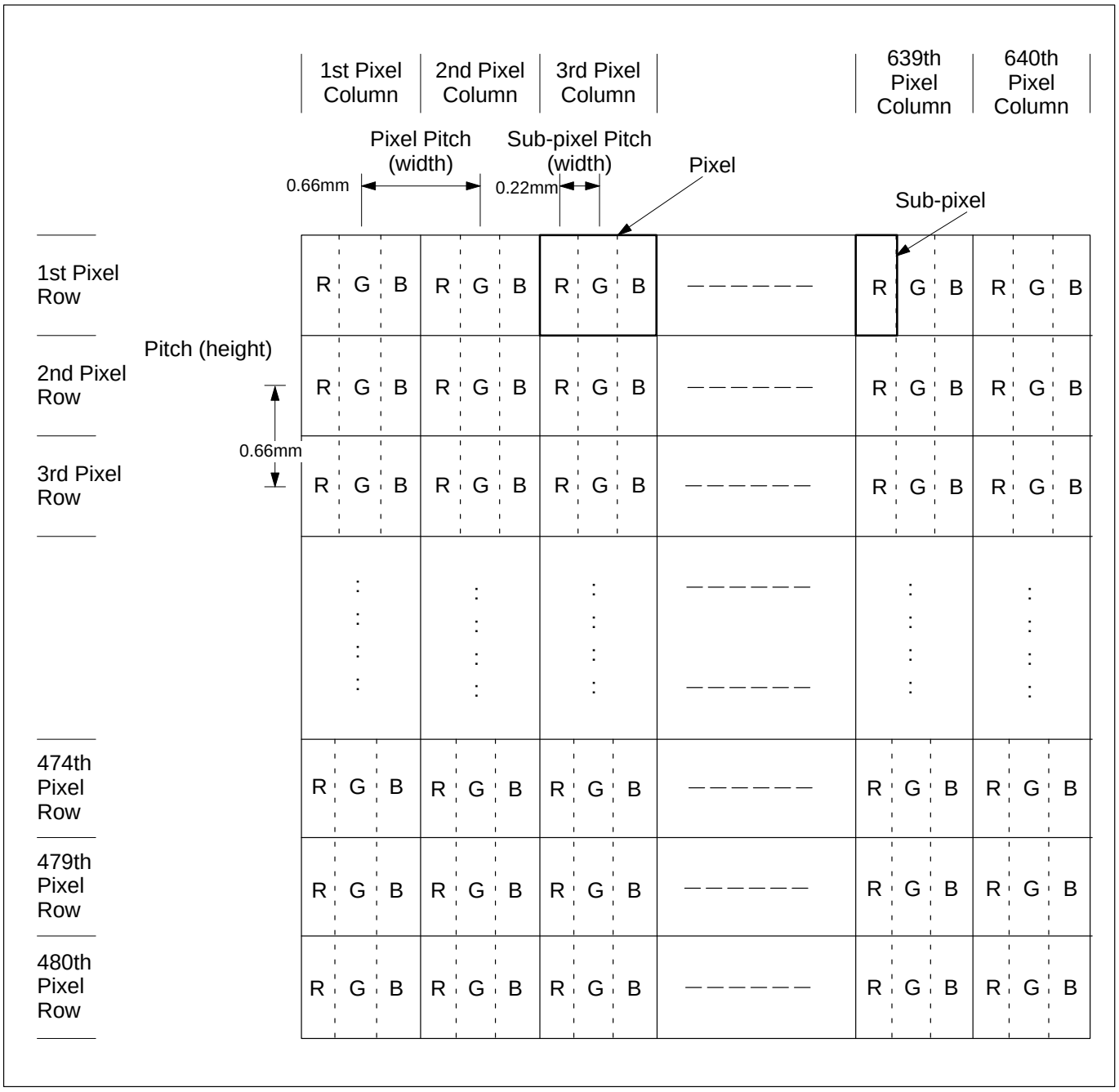


Figure 2. Display Dot Diagram

MECHANICAL SPECIFICATIONS

No.	Item	Rating
1	Max. Outer Dimensions	Width 480mm (18.90”) × Height 400mm (15.75”) × Thickness 32mm (1.26”) (see Package Dimensions)
2	Weight	under 5.0kg (11.16 lbs.)

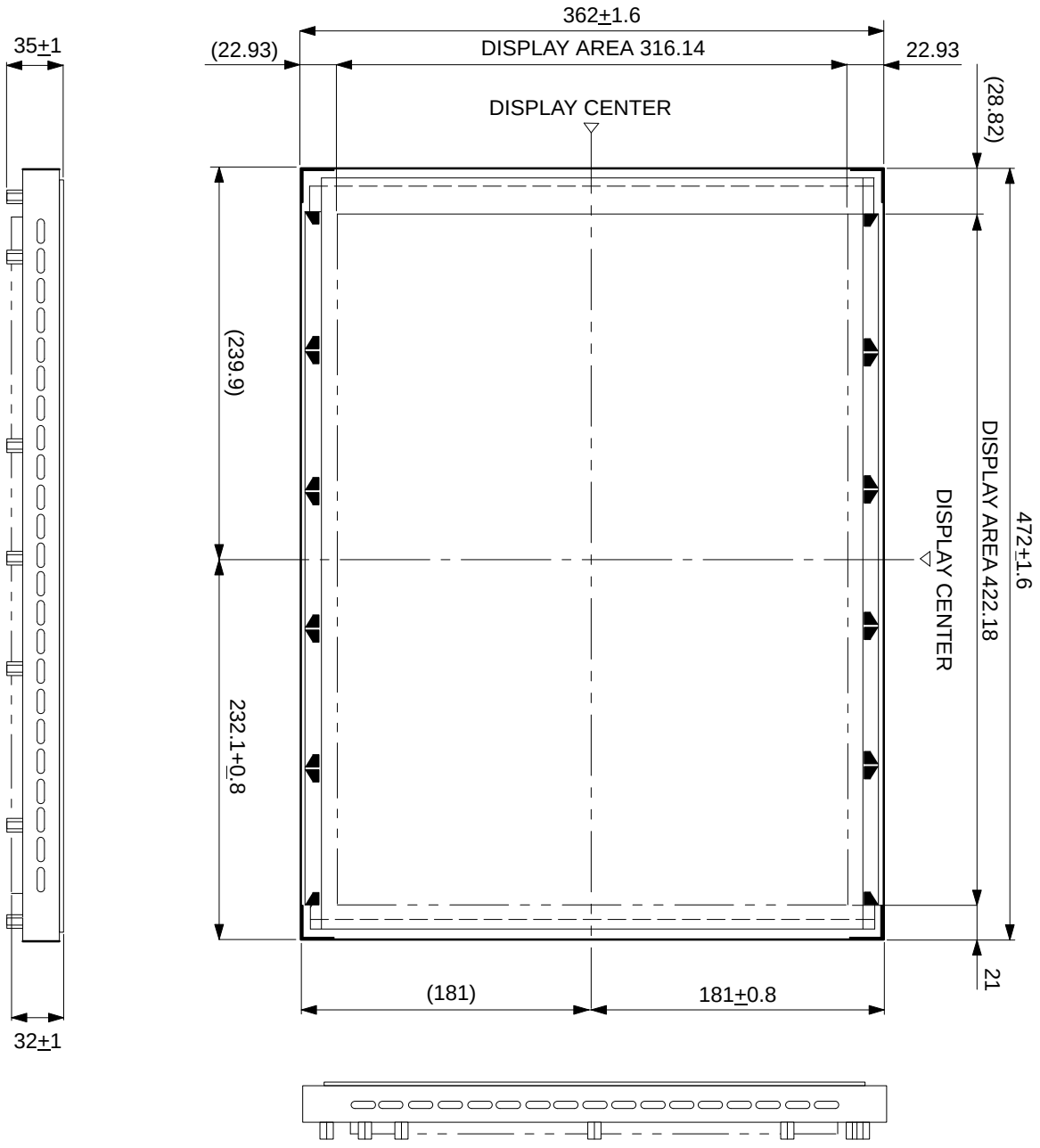
MECHANICAL CHARACTERISTICS

No.	Item	Rating	
1	Vibration	Operational	Acceleration: under 0.5G, Frequency: 10~55Hz Time: 5 minutes (X, Y, Z directions)
		Non-operational	Acceleration: under 0.5G, Frequency 10~55Hz Time: 2 hours (X, Y, Z directions)
2	Impact	Non-operational	Acceleration: under 40G (X, Y direction) under 20G (Z direction) Time: 11msec

ENVIRONMENTAL CHARACTERISTICS

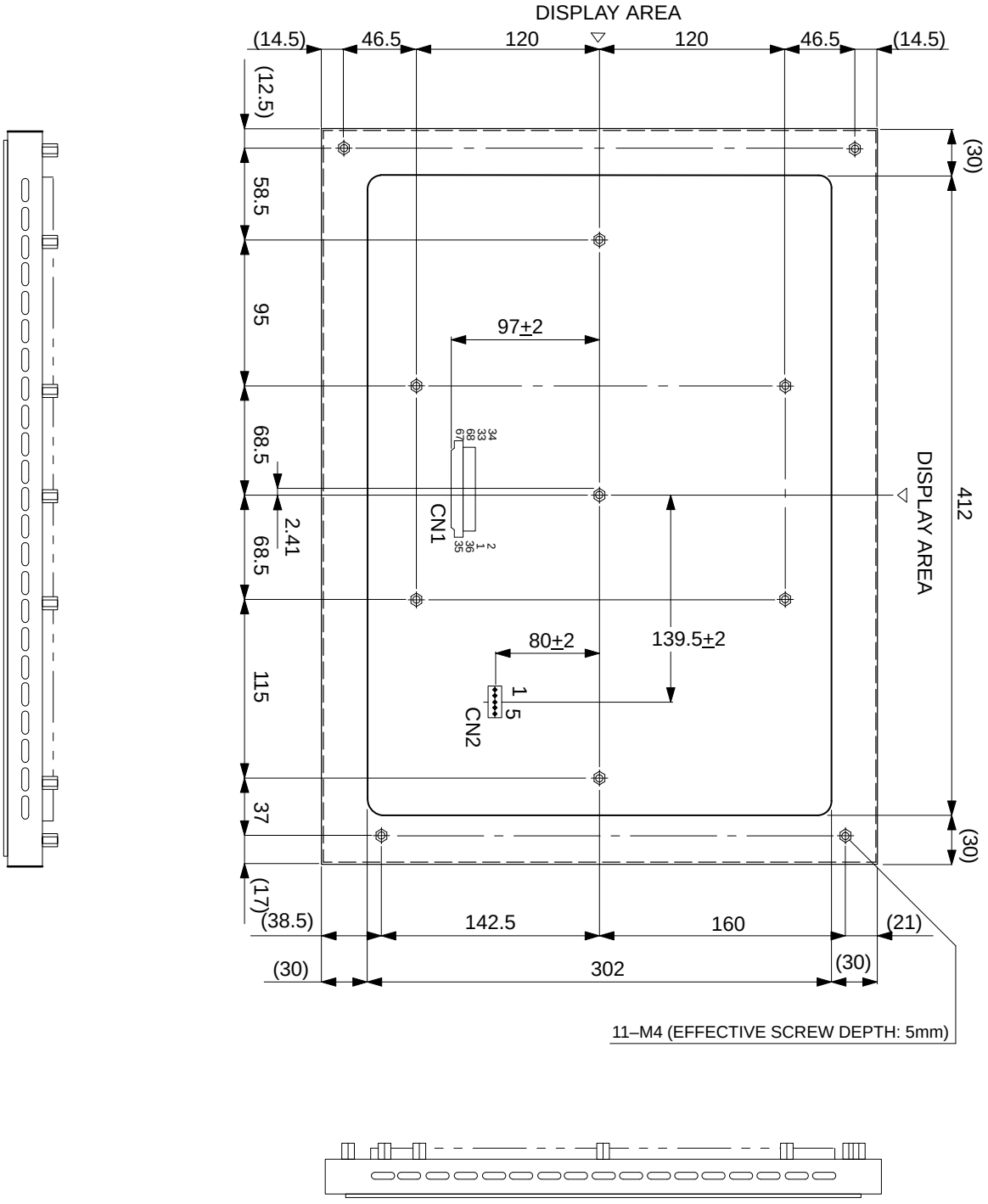
No.	Item	Rating	
1	Temperature	Operational	0°C ~ 45°C (max. glass panel surface temp. under 80°C)
		Non-operational	-20°C ~ 70°C
2	Humidity		20 ~ 85% RH
3	Pressure		800 ~ 1114hPa (Altitude: 0 ~ 2000m)

PACKAGE DIMENSIONS (Front View)



Unit: mm

PACKAGE DIMENSIONS (Back View)



Unit: mm

ELECTRICAL CHARACTERISTICS

MAXIMUM ABSOLUTE VOLTAGE RATING

No.	Item	Symbol	Absolute Max. Rating	Unit
1	Logic Voltage	V_{CC}	7.0	V
2	Panel Driver Voltage	V_S	200	V

INPUT POWER TYPE AND SPECIFICATIONS

No.	Item		Symbol	Term/Condition	Value			Unit
					Min.	Typ.	Max.	
1	Panel Driver Voltage	Voltage	V_S	Auto setting (170 + 10 × Vr)	170		195	V
		Ripple/Noise	V_{NRS}	Load Resistance	–	–	500	mV
		Stability	–	Load Resistance	–	–	± 1.5	%
		Setting Accuracy	–	Deviation from expression (1)	–	–	± 0.5	%
		Current (average)	I_S		100	–	700	mA
		Current (instant)	I_{SP}	Pulse Width: 2.0ms max. (no-pulse: 1.8ms)	–	–	4.0	A
2	Logic Voltage	Voltage	V_{CC}	Fixed	4.75	5.0	5.25	V
		Ripple/Noise	V_{NRS}	Load Resistance			200	mV
		Stability		Load Resistance			±5	%
		Power Flow (average)	I_{CC}		0.4	1.9	2.0	A

NOTES:

1. In V_S Voltage Setting, the V_r signal is output from the unit.
2. V_S Voltage will not be applied to the panel under the following conditions. Also, in this case, the sustain current (I_S) will be less than 50mA.
   1) V_{CC} has not been applied.
   2) 200ms after application of V_{CC}.
   3) V_S Voltage is outside standard range.
   4) No vertical synchronous signal input.
3. V_S is suppressed to about 550mA by the Automatic Power Control function (APC), however, at start up (max. 5 seconds), a max. 1.4A current can be reached. APC setting value = 105W ± 10W. (APC start up display rate is approximately 40%.)

INPUT SIGNAL TYPES AND SPECIFICATIONS

No.	Item	Condition	Symbol	Value			Unit
				Min.	Typ.	Max.	
1	Input Voltage: TTL Level 1) “H” Level 2) “L” Level		 V_{IN} V_{IL}	 2.0 –0.5	 – –	 5.25 0.8	 V V
2	Input Current: TTL Level 1) “H” Level 2) “L” Level	 V_I = 2.75V, V_{CC} = 5.25V V_I = 0.4V, V_{CC} = 5.25V	 I_{IH} I_{IL}	 – –	 – –	 20 –16	 µA mA

OUTPUT SIGNAL TYPES AND MEASUREMENTS (Vr)

No.	Item		Symbol	Condition	Value			Unit
					Min.	Typ.	Max.	
1	V_S Setting	Voltage	V_r	Load 1kΩ	0	–	2.5	V
		Ripple/Noise	V_{NRR}	Load 1kΩ	–	–	±500	mV
		Stability (average)	–	Load 1kΩ	–	–	±0.1	%
		Current (average)	I_{CC}	Load 1kΩ	–	–	3	mA

NOTES:

1. V_r is set at a value obtained from the following formula which is relative to V_S.
   $V_S = 170+10x\ V_r$ (V) expression (1)
   (V_r:0~2.5V)

Ex:V_S=180V → V_r=1.0V

INTERFACE SIGNAL

(1) Signal Definition and Function

Signal Name	Signal	Qty.	Signal Definition and Function
Data Signal (Digital RGB)	DATA–R	8	Display Data Signal: R7, G7 and B7 are the highest brightness data and R1, G1 and B1 are the lowest brightness data. Only the highest 6 bits of data are valid from 8 bits. (64 grayscale)
	DATA–G	8	
	DATA–B	8	
Clock	$\overline{DCLK}$	1	Display Data Timing Signal Data is read in when $\overline{DCLK}$ is turned off. $\overline{DCLK}$ is continuously input.
Blanking signal	$\overline{BLANK}$	1	When BLANKING signal is logical HIGH, data is valid and upper left justified. When BLANKING Signal is logical LOW, data is invalid (not read).
Horizontal Sync Signal	$\overline{Hsync}$	1	Regulates one horizontal line of data. Begins control of the next line when Hsync is turned off.
Vertical sync Signal	$\overline{Vsync}$	1	Screen Start up Control Timing Signal. Begins control of the next screen when Vsync is turned off.
Parity Signal	PARITY	1	For NTSC Image Display Data, this signal applies Even/Odd Field Setting. “H” Level: Odd Field “L” Level: Even Field
Display Enable Signal	DISPEN	1	Display/non–display Control Signal “H” Level: Display “L” Level: non–display
Brightness Control Signal	B–CNT (0) (1) (2)	3	Full Screen Display Brightness Setting Signal: Brightness is controlled continuously by the external resistance. (Variable Resistance: R=5.0kΩ connected to 3 input terminals (0, 1, 2))

Non-interlaced Display Mode

This is the standard mode. When a 480 line non-interlaced signal is received, a 480 line non-interlaced scanned display occurs within the unit. If a full 480 line signal is not received, it is shown in the upper portion of the screen. The lower portion is left blank.

The input signal conditions are shown below. Figure 4 shows the timing.

No.	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
1	T_{vsync}	16.5	16.7	20.0	ms	Frame Frequency: 60Hz average
2	t_{wv}	1	–	–	µs	
3	t_{vh}	0	–	–	µs	
4	t_{hv}	0	–	–	µs	
5	T_{hsync}	31.0	–	–	µs	
6	t_{wh}	0.2	–	(1H–0.2)	µs	
7	t_{hc}	0.2	–	–	µs	
8	t_{ch}	0.2	–	–	µs	
9	t_{clk}	33	39.7	–	ns	
10	t_{wclk1}	16	–	–	ns	
11	t_{wclk2}	16	–	–	ns	$t_{wclk1} + t_{wclk2} = t_{clk}$
12	t_{sub}	5	–	–	ns	$t_{sub} \leqq t_{hc}$
13	t_{hb}	10	–	–	ns	$t_{hb} \leqq t_{ch}$
14	t_{sud}	5	–	–	ns	
15	t_{hd}	10	–	–	ns	

Interlaced Display Mode

In NTSC standard timing display mode (RGB 8-bit TTL Signal), when the PARITY Signal (toggle signal) is input, the interlaced display mode is automatically activated. By displaying the same data on the adjoining two scanning lines, 480 lines non–interlaced scanning is done. However, the display position of odd fields and even fields are offset one line on the screen.

Field	Input Signal Line	On–screen display line
odd field	n	2n–1, 2n line
even field	n	2n, 2n+1

NOTE: n:1~240

Input signal conditions are shown below. Figure 5 shows the timing.

No.	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
1	T_{vsync}	16.5	16.7	20.0	ms	Frame Frequency: 60Hz average
2	t_{wv}	1	1,333.5	–	µs	
3	t_{vh}	0	–	–	µs	
4	t_{hv}	0	–	–	µs	
5	T_{hsync}	31.0	63.5	–	µs	
6	t_{wh}	0.2	–	(1H–0.2)	µs	
7	t_{hc}	0.2	–	–	µs	
8	t_{ch}	0.2	–	–	µs	
9	t_{clk}	33	69.83	–	ns	f_{clk} = 14.32MHz
10	t_{wclk1}	16	–	–	ns	
11	t_{wclk2}	16	–	–	ns	$t_{wclk1} + t_{wclk2} = t_{clk}$
12	t_{sub}	5	–	–	ns	$t_{sub} \leqq t_{hc}$
13	t_{hb}	10	–	–	ns	$t_{hb} \leqq t_{ch}$
14	t_{sud}	5	–	–	ns	
15	t_{hd}	10	–	–	ns	

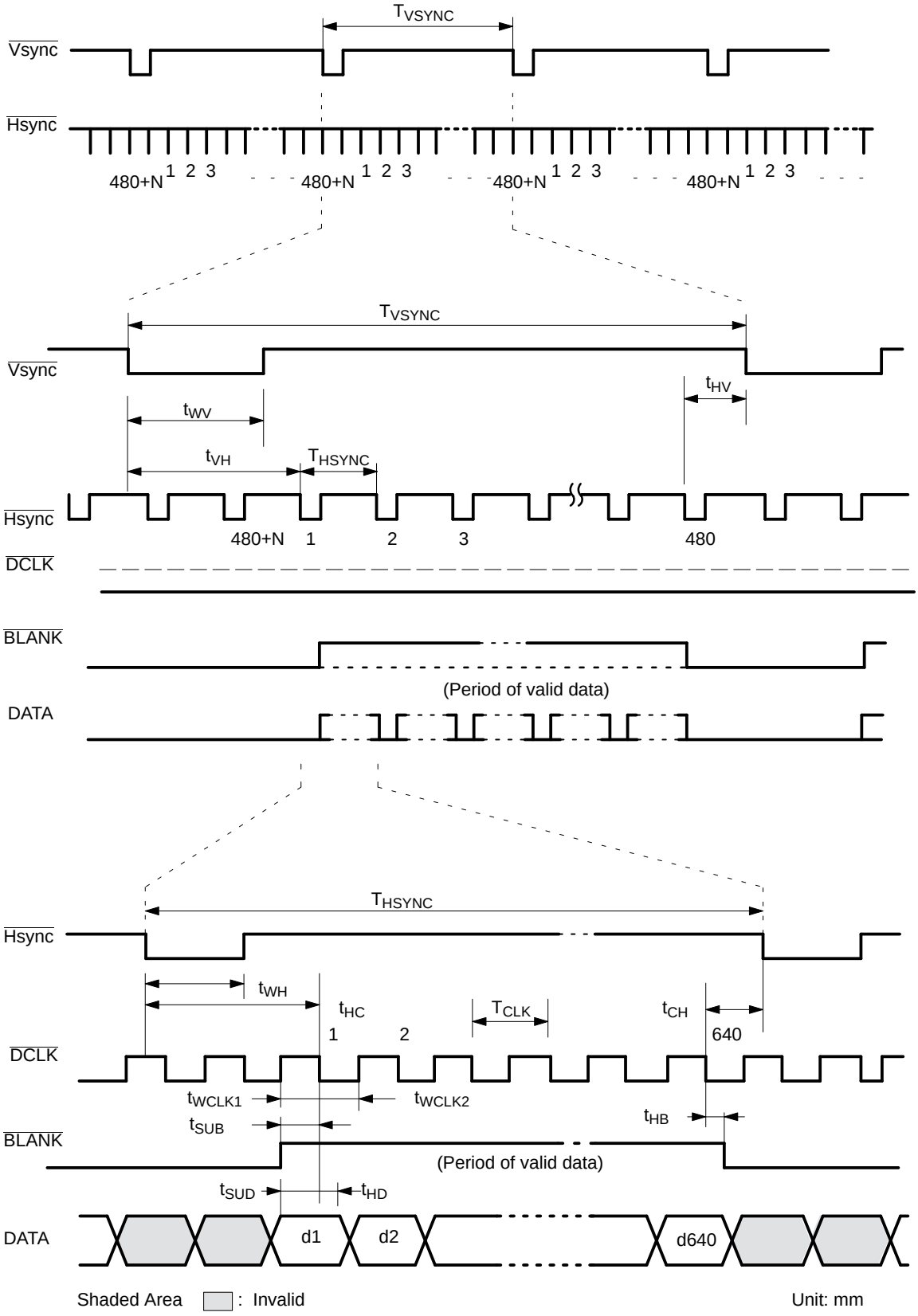


Figure 4. Input Signal Timing (Non-interlaced Mode)

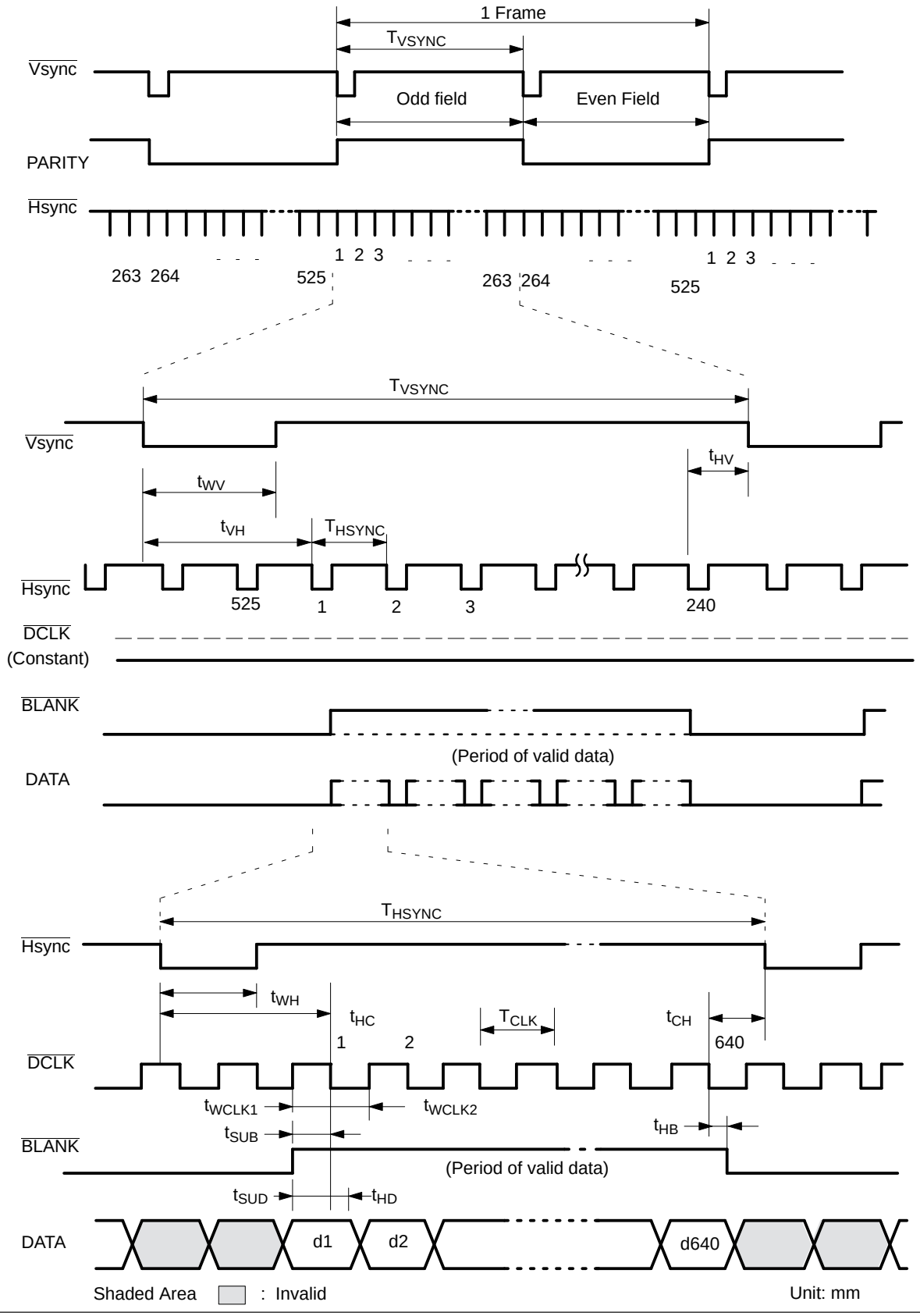


Figure 5. Input Signal Timing (Interlaced Mode)

CONNECTORS AND CONNECTIONS

(1) Signal Connectors (Hirose Denki: FX2B–68P 1.27DS)

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	DATA-R 7	2	S. GND	35	DATA-B 7	36	S. GND
3	DATA-R 6	4	S. GND	37	DATA-B 6	38	S. GND
5	DATA-R 5	6	S. GND	39	DATA-B 5	40	S. GND
7	DATA-R 4	8	S. GND	41	DATA-B 4	42	S. GND
9	DATA-R 3	10	S. GND	43	DATA-B 3	44	S. GND
11	DATA-R 2	12	S. GND	45	DATA-B 2	46	S. GND
13	DATA-R 1	14	S. GND	47	DATA-B 1	48	S. GND
15	DATA-R 0	16	S. GND	49	DATA-B 0	50	S. GND
17	DATA-G 7	18	S. GND	51	$\overline{\text{Vsync}}$	52	S. GND
19	DATA-G 6	20	S. GND	53	$\overline{\text{Hsync}}$	54	S. GND
21	DATA-G 5	22	S. GND	55	$\overline{\text{BLANK}}$	56	S. GND
23	DATA-G 4	24	S. GND	57	$\overline{\text{DCLK}}$	58	S. GND
25	DATA-G 3	26	S. GND	59	PARITY	60	S. GND
27	DATA-G 2	28	S. GND	61	DISPEN	62	S. GND
29	DATA-G 1	30	S. GND	63	N.C.	64	B–CNT0
31	DATA-G 0	32	S. GND	65	B-CNT2	66	B–CNT1
33	N.C.	34	N.C.	67	N.C.	68	N.C.

NOTE: N.C. indicates No Connection at this terminal.

Mating connector: FX2B 68S 1.27R.

(2) Power Source Connector (Nippon Atchaku Tanshi: B5P VH)

Pin No.	Symbol
1	V_{CC}
2	GND
3	V_S
4	GND
5	V_R

Mating connectors:

Housing	VHR 5N
Contact	SVH 21T P 1.1

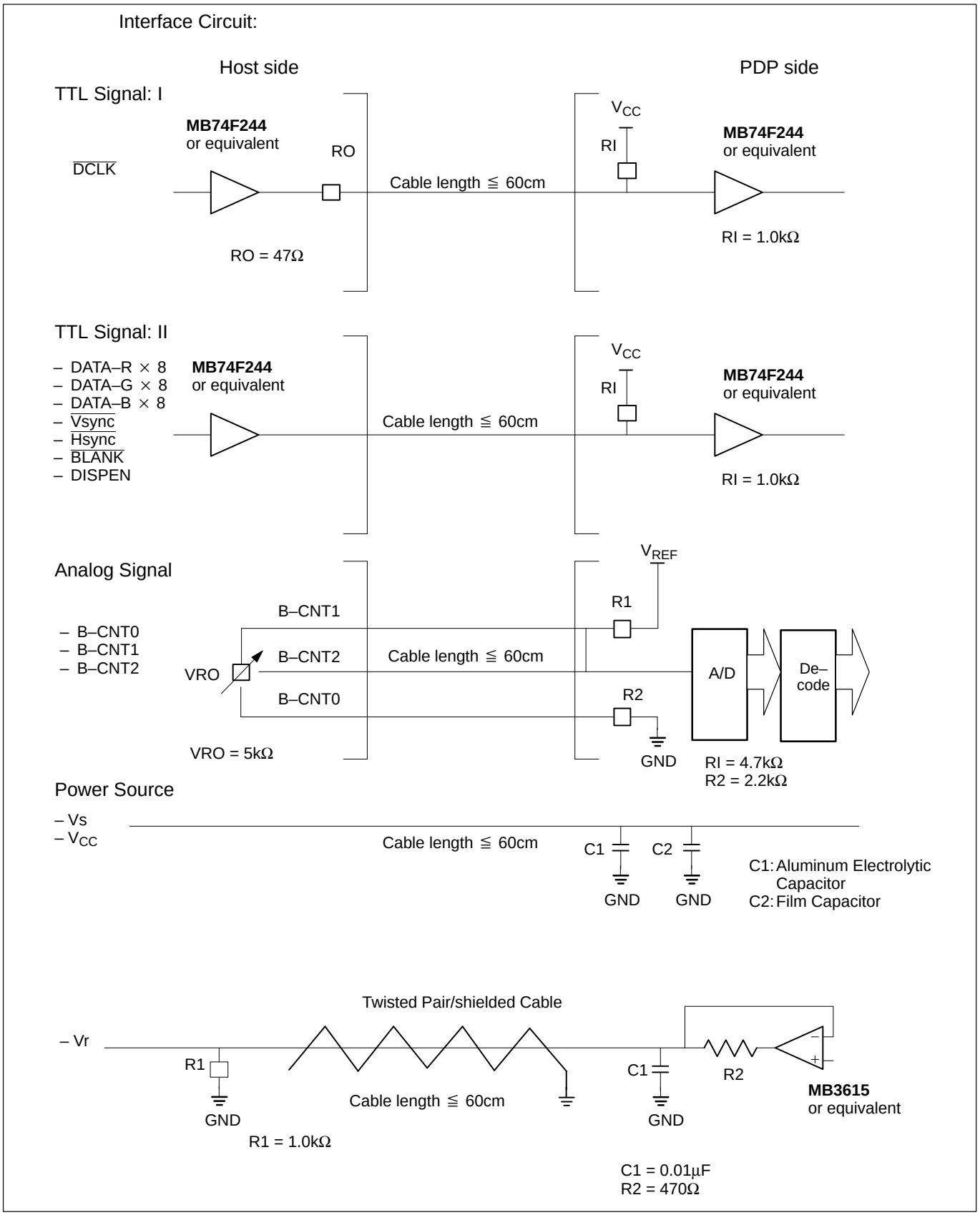


Figure 6. Interface Circuit

MTBF VALUE

Average failure time based on design: 23,500 hours (environmental temperature: 35°C).

The anticipated failure time is an estimate only. This is not a guarantee for each individual produce. Failure due to wear is not included.

ANTICIPATED AVERAGE LIFE SPAN

Anticipated Average life: 10,000 hours

Anticipated average life is the time when the brightness level becomes half of its initial value. This value cannot be guaranteed for each individual product.

LABEL

The following are shown on the unit's label:

1)	Part No.	FPF21C8060UA-02
2)	Manufacturer	FUJITSU LIMITED
3)	Mfr. No.	Yr-Mo No. Rev No.
4)	Mfr. Yr-Mo	Yr Mo

WARNINGS

(1) Screen

1. Do not display the same pattern for an extended period of time. It is ideal that control of display should be designed so that accumulative lit time of each pixel is the same. If the same pattern is shown for an extended period of time, the brightness of that area will be decreased over areas due to the degradation of phosphor or the brightness will be increased due to the fact that the electrode surface will be activated more than other areas.

(2) Power Source Connection and Interruption

1. Do not connect or disconnect any of the DC input lines such as V_{CC}, V_S when certain voltage exists on it.
2. Even if the AC input is cut, there is still residual power. After 1 minute, disconnect the PDP input connector.
3. To connect and disconnect the PDP unit power source, follow the sequences below:
   – Connect: Connect Vcc → Connect Vs
   – Disconnect: Disconnect Vs → Disconnect Vcc

(3) Connecting and Disconnecting the Control Signal

Use the following sequences to connect and disconnect the PDP unit's power source and input control signal.

For safety's sake, if the control signal has not been input, the high voltage circuit interrupt function will start. (For instance, if Vsync is interrupted, the display will disappear.)

If the control signal is re–input, operations will begin again.

Connecting power source, control signal:
– Connect input control signal →
  Connect input power source

Disconnecting power source, control signal:
– Disconnect input power source →
  Disconnect input control signal

(4) Mounting an IF Card Near the Unit

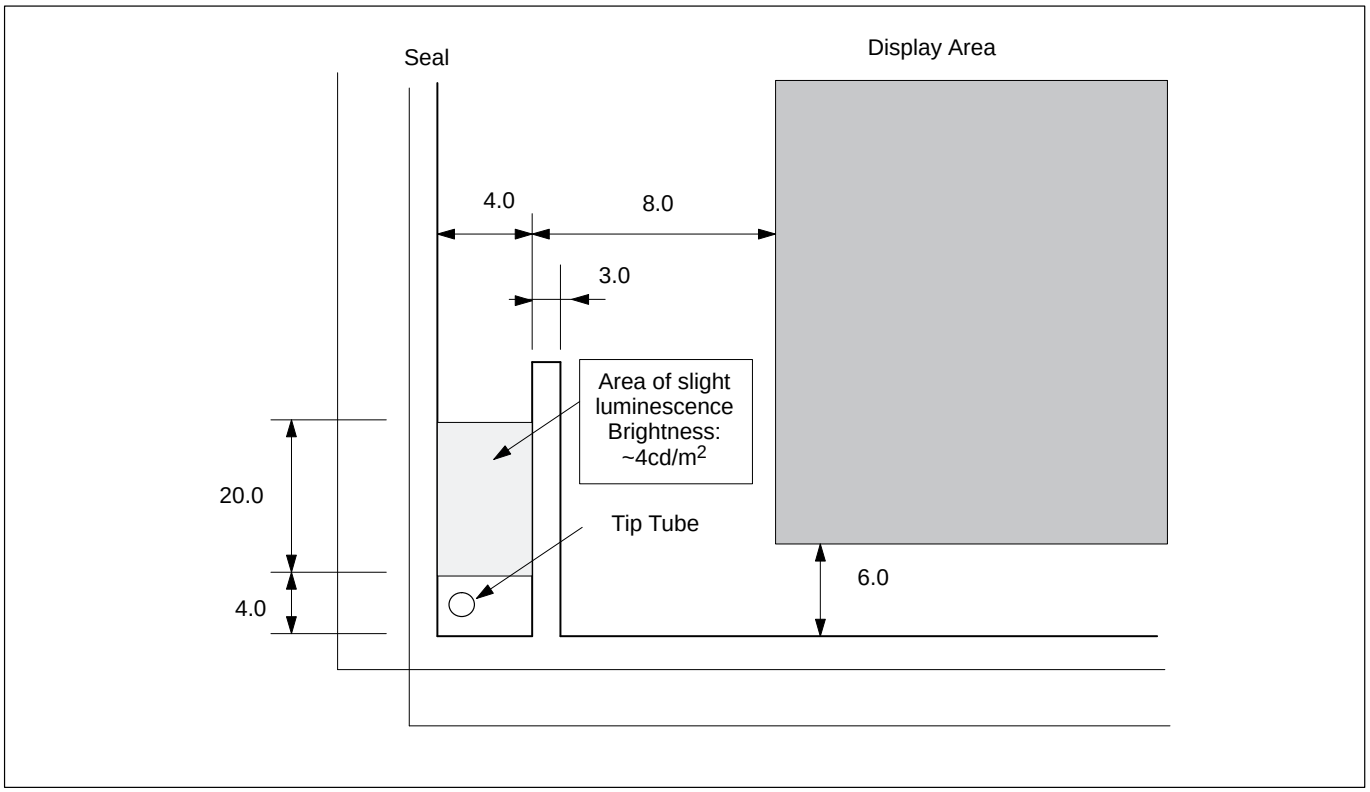
Screen noise will occur if an IF card is placed near the PDP unit. Place it away from the PDP unit.

(5) Changing Brightness and Color

Depending on the type of usage, there may be a slight change in the brightness and color over time. There may be an increase of both X–value and Y–value by 0.05 in chromaticity. In this case, adjust it by using external data signal.

(6) Luminosity Outside the Display Area

There is a slight (brightness approx. 3~4cd/m^2) neon luminescence shown outside the display area on the panel shown below. Mask this part so that it may not be seen on the display surface.


Seal
Display Area
4.0
8.0
3.0
Area of slight luminescence Brightness: ~4cd/m2
20.0
Tip Tube
6.0
4.0

1. REFERENCE

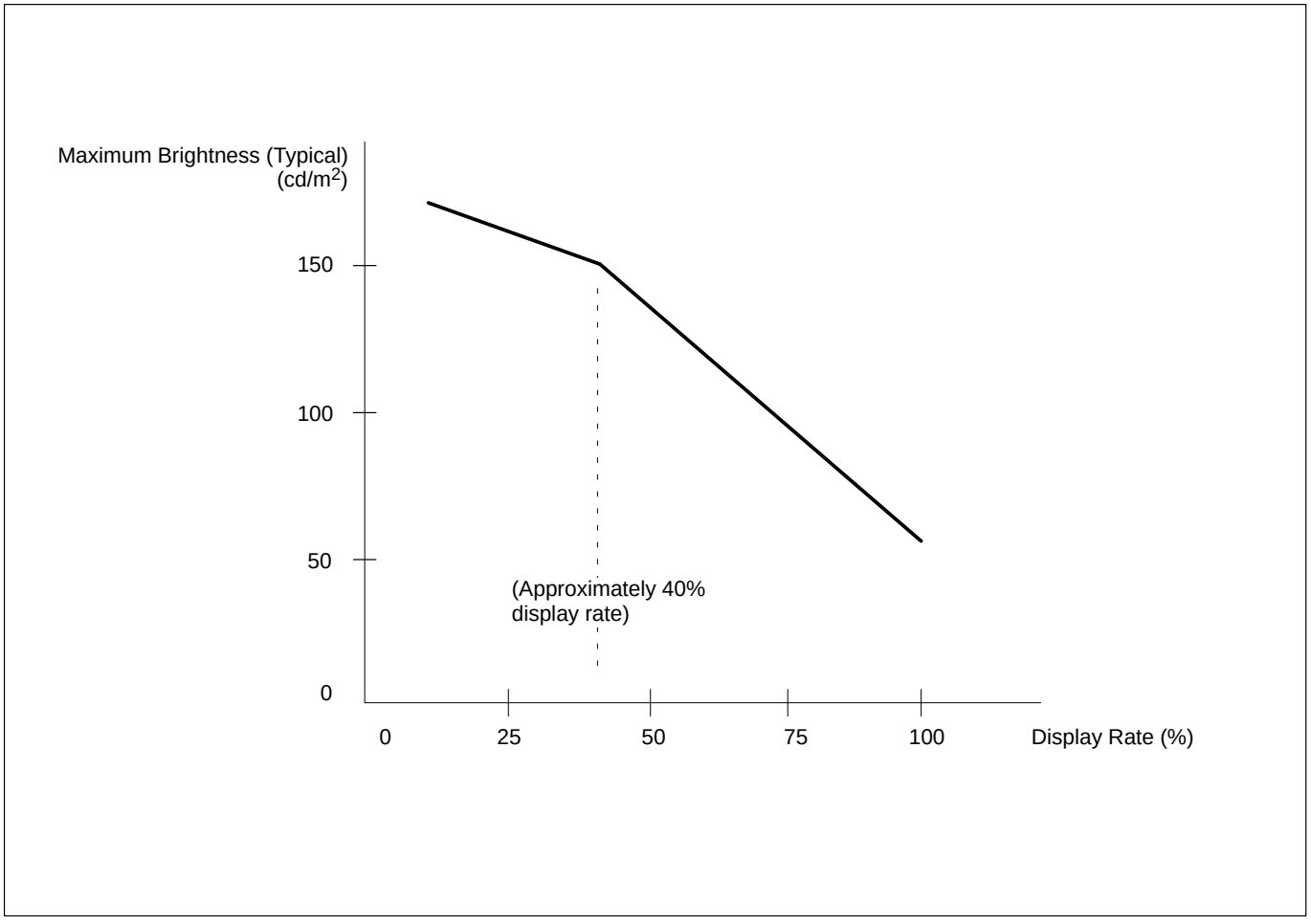
1.1. DISPLAY RATE AND BRIGHTNESS SPECIAL FEATURES

This unit has an automatic power control function for V_S power source.

If the Vs power source exceeds 550mA (display rate over 40%), brightness will gradually decline.

If a display rate increases over about 40%, the display brightness will be decreased gradually from the “APC non–operation level” to the “APC operation level” (max. 5 seconds).

Note: Definition of “Display Rate”
Display Rate 100% =
Every sub–pixel is lit at the maximum brightness.



1.2. ZIGZAG PATTERN AND GRAYSCALE FEATURES

This unit has an automatic power control function for address power source arranged in the unit. If the display rate of zigzag pattern increases over about 80%, grayscale level decreases from 64 (260K colors) to 32 (32K colors). If the rate is over about 90%, grayscale level is 16 (4K colors).

2. Display Quality Specifications

2.1. Display Cell Defect Specifications

This color, plasma display panel (color–PDP) has 1920 horizontal (640 x 3 [three colors: red, green, blue]) x 480 vertical color cells. These color cells are made to display color through on/off and brightness controls.

In some cases, a panel may have defective cells that cannot be controlled. These defective cells can be categorized into three types:

(1) Non–lighting cell defect: Defect in which the cell is always off

(2) Non–extinguishing cell defect: Defect in which the cell is always on

(3) High intensity cell defect: Defect in which the cell lights excessively brighter than other cells of the same color

The display cell defect specifications define the allowed limits for display cell defects and are used as the criteria in determining whether a panel is shipped.

Item	Definition	Specification	
Non–lighting cell defect (*1)	When all cells of a single RGB color are lit, a cell that remains unlit is considered a non–lightning cell defect. Cells that flicker on and off and cells in which at least 50% of the total size is lit do not fall in this defect category.	Total number of defects: Defect density: Continuous defects:	12 cells/screen or less for each color 5 cells/cm^2 or less for each color 5 cells or less horizontally 3 cells or less vertically
Non–extinguishing cell defect (*1)	When all cells of a single RGB color are lit, a cell of a different color that remains lit is considered a non–extinguishing cell defect. Cells that flicker on and off and cells in which at least 50% of the total size is unlit do not fall in this category.	Total number of defects: Defect density: Continuous defects:	12 cells/screen or less for each color 5 cells/cm^2 or less for each color 5 cells or less horizontally 3 cells or less vertically
High intensity cell defect	When all cells of a single RGB color are lit or all cells are unlit, a cell that illuminates two or more times brighter than other cells of the same color is considered a high intensity cell defect.	Total number of defects: Defect density: Continuous defect:	2 locations or less 1 location/50 Φ or less 4 cells/location or less horizontally 2 cells/location or less vertically

NOTES:

*1 Cells may flicker in the boundary areas of lit and unlit patterns of a display; however, the flickering is not abnormal.

This phenomenon is rare and occurs only with certain combinations of display pattern and gradient brightness level. Because this phenomenon cannot be eliminated with the lighting control method used, it will not be considered a display cell defect.

2.2. Brightness Variation Specifications

The color–PDP uses ultraviolet light produced by gas discharge to illuminate fluorescent units and displays color using color–coated fluorescent units. Uneven coating among the fluorescent units and inconsistent discharge characteristics cause slight differences in brightness among the sections in a panel. These differences in brightness among the panel sections produce brightness variations, which can be categorized into two types:

(1) Full–screen brightness variation: Slight differences in brightness that occur over the entire screen

(2) Localized brightness variation: Sharp differences in brightness that occur in adjacent sections of the screen

The brightness variation specifications define the allowed limits for these brightness differences and are used as the criteria in determining whether a panel is shipped.

Item	Definition	Specification
Full–screen brightness variation	The panel display area is divided into nine equal blocks (3x3), and the white display brightness at maximum intensity is measured for each block. The brightness variation is then calculated from the following equation: $\text{Brightness variation} = \frac{\text{max. brightness} - \text{min. brightness}}{\text{max. brightness}} \%$	30% or less
Localized brightness variation (*2)	If a localized sharp difference in brightness is recognized, the white display brightness is measured at 2 points, 20 mm apart, in that area. The brightness variation is the calculated from the following equation: $\text{Brightness variation} = \frac{\text{max. brightness} - \text{min. brightness}}{\text{max. brightness}} \%$	10% or less

*2 Some scan lines may appear brighter than other scan lines. However, this is not abnormal. Brightness variations in lines, bands, or stripes are governed by the localized brightness variation specification.

2.3. Color Specification

The color–PDP produces a white display by mixing the light produced by red, green, and blue fluorescent units. Consequently, the variation in light emitted from the individual fluorescent units in a panel produces slight differences in degree of whiteness.

The color specification defines the allowed limits for the degree of whiteness and is used as the criterion in determining whether a panel is shipped.

Item	Definition	Specification
Whiteness	The panel display area is divided into nine equal blocks (3x3), and the color at maximum intensity white display is measured for each block. The allowed whiteness is determined by the X and Y values on the CIE standard color chart.	x: 0.340 ± 0.03 Y: 0.340 ± 0.03

3. Expected Service Life

The service life characteristics of the color–PDP have two facets: the brightness life, which is determined by the fluorescent unit characteristics, and the display defect life, which is determined by the discharge characteristics.

For each facet, the expected service life is expected to be about 10,000 hours (this is not the guaranteed service life).

4. Repair and Maintenance

4.1. Repair and Maintenance Support

The color–PDP unit is a subassembly display module in which the display panel and the drive circuit are integrated into a single unit.

Because of product configuration and contents considerations, Fujitsu is unable to provide any field repair or maintenance services. Consequently, the product prices do not include any service costs.

Repair and maintenance for the color–PDP unit is limited to products that are returned to the Fujitsu factory. Service costs, if any, are determined based on the fault condition. If a service cost is involved, the service will be implemented only after customer approval is received.

4.2. Spare Units

As described in item 4–1, repair and maintenance services are performed only at the factory and require about one month after the product is received at our factory.

Because we are unable to provide immediate service in the field, Fujitsu recommends customers to purchase enough spare PDP units according to the urgency of their operations.

5. Guidelines on Using the Color–PDP

The color–PDP unit is a display device module that consists of a glass panel section and a drive circuit section. The glass panel section is a glass substrate on which electrodes, fluorescent units, and other components are realized through thin–film and thick–film processes. The drive circuit section is a printed circuit board onto which the electric circuits that drive the glass panel section have been incorporated. When designing and handling the color–PDP unit, be sure to follow the guidelines described below.

5.1. General Notes

Considerations and packaging for delivery and transport

When delivering or transporting the unit, take special precautions so that excess vibration or shock is not applied to the unit. If the unit is dropped or if excess vibration or shock is applied, the glass panel section may break and the drive circuit section may become damaged. The unit should be delivered or transported in Fujitsu's shipment packaging or similar packaging.

Static electricity precautions during handling, delivery, and transport

The drive circuit section uses C–MOS integrated circuits that must be protected from static electricity. Therefore when delivering or transporting the unit, be sure to place the unit in an antistatic bag.

When handling a color–PDP unit, take adequate grounding precautions to prevent static electricity buildup.

Instructions on cleaning the glass panel display section

To clean the glass panel display section, apply water or a neutral detergent to a piece of soft cloth (gauze) and wring the cloth tightly before wiping the display. Make sure that no water contacts the terminal connectors on the side of the glass panel display section. Never use chemical solvents, such as paint thinner or benzene, to clean the display section.

Instruction on storing and restarting the color–PDP unit

When storing the color–PDP unit, select an environmentally controlled location. Avoid any environment in which the temperature or humidity becomes too high. If you are storing the unit for a long period of time (over one month), place the unit together with a dehumidifying agent, such as silica gel, in a moisture–proof bag and keep the unit in an environmentally controlled location.

When a unit that has been in storage for a long time is restarted, an operation lag, which is characteristic of PDPs that use electric discharge, may occur. If a lag occurs, operate the unit again without the filter in brightly lit environment. Maintain this condition until the unit operates normally. Once the unit begins to operate normally, the same lag–free operation that took place before the unit was stored will return.

Handling during operation and drive voltage

The color–PDP unit has a section that operates using high voltage (about 340 volts). If you need to handle an operating unit, take the proper precautions against electric shock and never touch the drive circuit section.

The capacitors in the drive circuit section remain temporarily charged even after the unit power is turned off. After turning off the power, be sure to wait at least a minute before touching the unit.

Connecting and disconnecting signal and power connectors during operation

The color–PDP unit is equipped with various protection circuits that automatically stop unit operation if an interface signal or the power voltage becomes abnormal during operation.

Although the protection circuits will operate if a connector is connected or disconnected during operation, the protection circuits were not designed for this purpose. Therefore never connect or disconnect a signal or power connector while the unit is operating.

The capacitors in the drive circuit section remain temporarily charged even after the unit power is turned off. After turning off the power, be sure to wait at least a minute before touching the unit.

Unit modification and warranty

The glass panel display and drive circuit section of the color–PDP unit are closely connected and function as a pair. If the unit is arbitrarily recombined, restructured, or disassembled, Fujitsu will not be responsible for the function, quality, or any other item of the modified unit. Do not recombine, restructure, or disassemble the color–PDP unit.

5.2. Guidelines on Device Design

Fixed display and screen burn–in

Because the color–PDP uses fluorescent units to emit light, the fluorescent units, like a CRT, deteriorate in proportion to display frequency, and brightness decreases.

Thus, if the same pattern is displayed continuously (fixed display), that fluorescent units in that section deteriorates faster (brightness decrease) compared with the other display sections and screen burn–in occurs.

This phenomenon can be reduced effectively by periodically inserting a uniform, full–screen pattern or installing a screen saver–type display software.

When the display pattern is changed, the areas that had been illuminated may appear temporarily (few minutes) brighter. This phenomenon is characteristic of color PDPs and is due to activation of the discharge surface. It does not indicate an abnormal display.

Unit ambient temperature and unit ventilation

In the color–PDP unit, both the glass panel display section and the drive circuit section radiate heat.

The device design should include thorough heat–dissipation measures, like installing the unit in a well–ventilated area. In addition, the unit ambient temperature should be maintained so that it does not exceed 45°C. The temperature of the glass panel display section becomes especially high because of the installed filter and the additional heat that radiates from drive circuit. The device should be designed with ventilation fans and other heat–dissipation measures.

Furthermore, the ventilation should be designed to prevent condensation and adhesion of conductive particles because part of the unit operates at a high voltage (340 volts).

Glass panel cracks and device structure

The devices should be designed so that metal and other hard objects do not contact the glass panel display section and forces due to heat or mechanical distortion are not applied.

Be careful not to break the glass when assembling the device or handling the color–PDP unit. Also, when handling the unit, wear gloves or other hand protection to prevent injuries that can occur if the glass breaks.

Interface signals and external noise

The color–PDP unit displays patterns using display data and synchronizing signals that determine the horizontal/vertical operation timings.

If noise interferes with these signals, it can cause the display to become unstable and, in some case cases, lead to a failure. The unit has protection circuits that operate to prevent noise–induced failures and may stop the display.

Do not place equipment that can act enormous noise sources near the unit interface cables, and keep the cables as short as possible.

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