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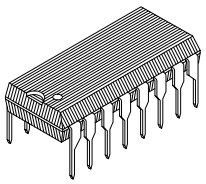
FUJITSU

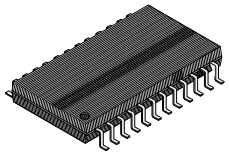
DATA SHEET

MB87032
Two-Channel Electronic Volume Controller

The Fujitsu MB87032 is a highly efficient 2-channel electronic volume controller. It has been fabricated with the CMOS silicon gate process and is available in a 16-pin plastic DIP and a 24-pin plastic SOP. It enables the selection of volume or balance in loudness and tone control modes. The controller is ideal to use in TVs, VCRs, and car stereos.



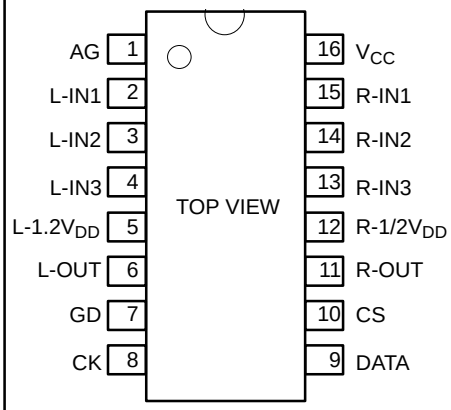
Plastic DIP
(DIP-16P-M03)



Plastic SOP
FPT-24P-M02)

- TTL interface enables microcomputer control
- Volume gain control range:
  0.dB to 78 dB every 1 dB step; (–80 dB Mute mode)
- On-chip 2-channel volume control (L-channel and R-channel) for a balanced control mode
- Tone control in 13 steps (tap point = –20 dB) is achieved by using an external condenser and resistor
- Loudness operation is possible from 0 dB
- Single supply voltage: +8 V
- Package and ordering information:
  – 16-pin plastic DIP, order as MB87032P
  – 24-pin plastic SOP, order as MB87032PF

Pin Assignment



SOP pin assignment on page 13

ABSOLUTE MAXIMUM RATINGS

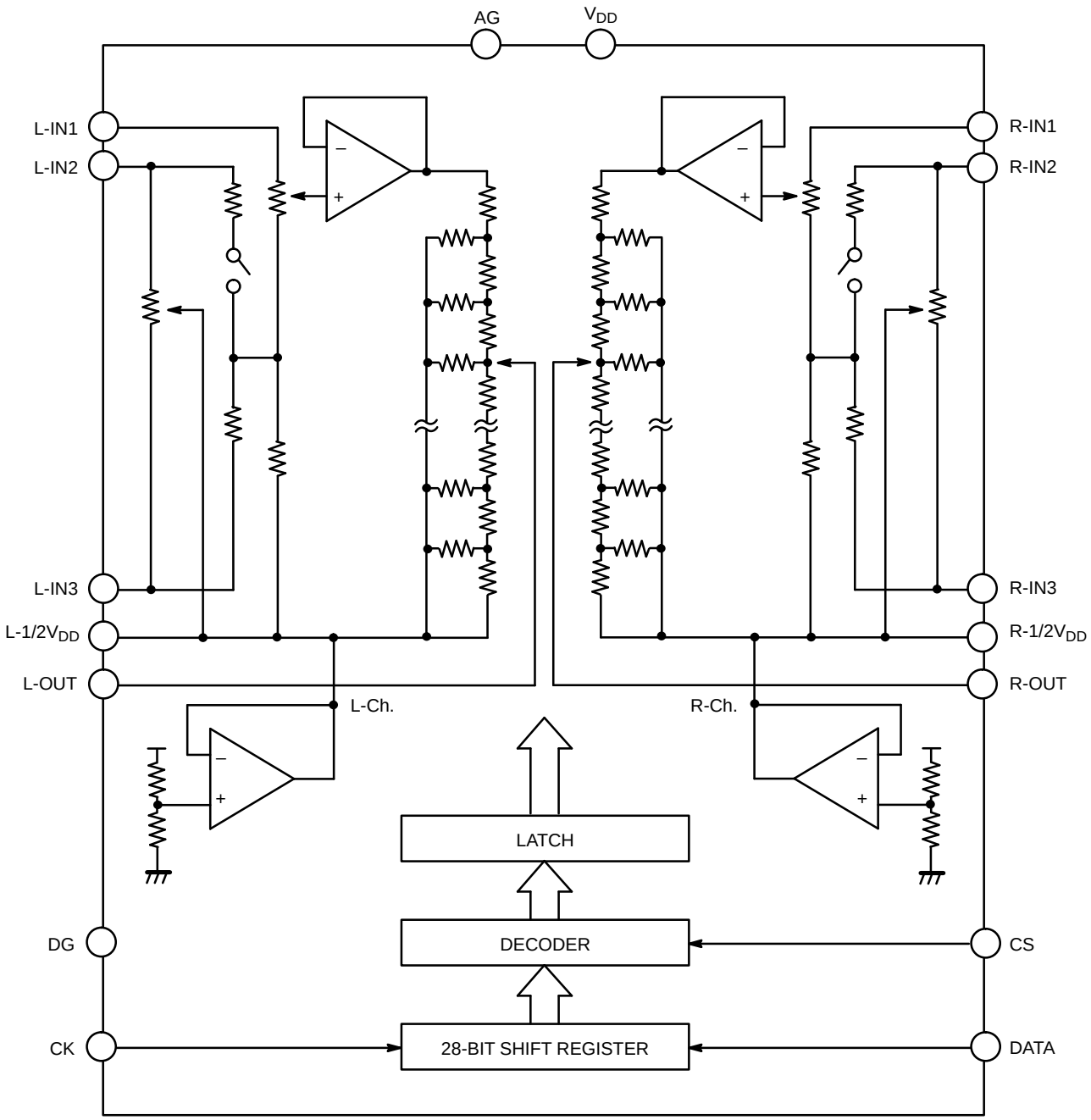
Parameter	Symbol	Pin No.		Value			Unit
		DIP	SOP	Min.	Typ.	Max.	
Supply Voltage	V_{DD}	16	24	–	–	10	V
Input Voltage	V_{IN}	All input pins		GND–0.3	–	V_{DD} +0.3	V
Output Voltage	V_{OUT}	All output pins		GND–0.3	–	V_{DD} +0.3	V
Storage Temperature	T_{STG}	–		–50	–	125	°C

— Note —

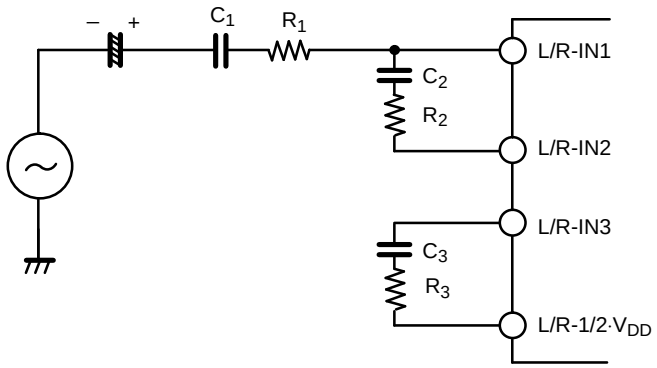
Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Figure 1. MB87032 Block Diagram



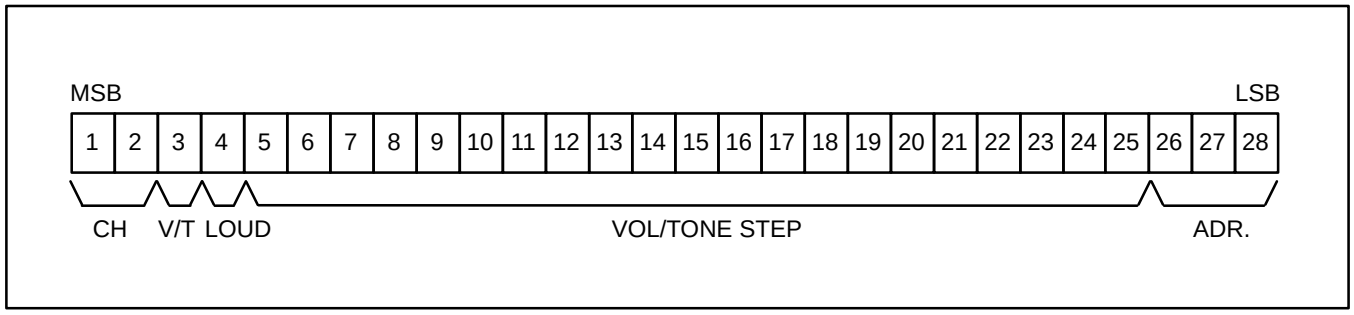
PIN DESCRIPTIONS

Pin No. DIP	Pin No. FPT	Pin Name	I/O	Description	Note
1	1	AG	–	Ground for analog circuit	
2	2	L-IN1	I	**Analog input pins.**These pins should be driven by a low impedance (100 Ω or less). Volume, loundness, and tone modes are selected depending on the value of R_1, R_2, R_3, C_1, C_2, and C_3 (including open and short). Please see Figure 2, for an application example circuit.  **Figure 2. Input Pins Connection Example**	L,R symmetrical analog input
15	23	R-IN1	I		
3	4	L-IN2	I		
14	21	R-IN2	I		
4	5	L-IN3	I		
13	20	R-IN3	I		
5	6	L-1/2·V_{DD}	O	One-half level of supply voltage is output.	L,R symmetrical analog output
12	19	R-1/2·V_{DD}	O		
6	8	L-OUT	O	**Electric volume output pins.** If the following state is low impedance, a step error will occur because these outputs are high impedance. To avoid a step error the state following must be a high impedance of 1 MΩ or greater.	
11	17	R-OUT	O		
7	11	DG	–	**Ground for digital circuit.**	
8	12	CK	I	**Clock signal input.** Data is input from DATA pin by the falling edge of CK signal.	TTL interface Digital input
9	13	DATA	I	**Data input for volume, tone, channel selection.** Data consists of 28-bit data which is serially input by the falling edge of the CK signal.	
10	14	CS	I	**Strobe signal input.** Control data is latched by the falling edge of CS signal unless the strobe signal is input, control data keeps its former condition. Please see Figure 6, timing chart.	
16	24	V_{DD}	–	**Supply voltage, +8 V.**	
–	3, 7 9, 10 15, 16 18, 22	NC	–	No connection.	

FUNCTIONAL DESCRIPTIONS

Data Format

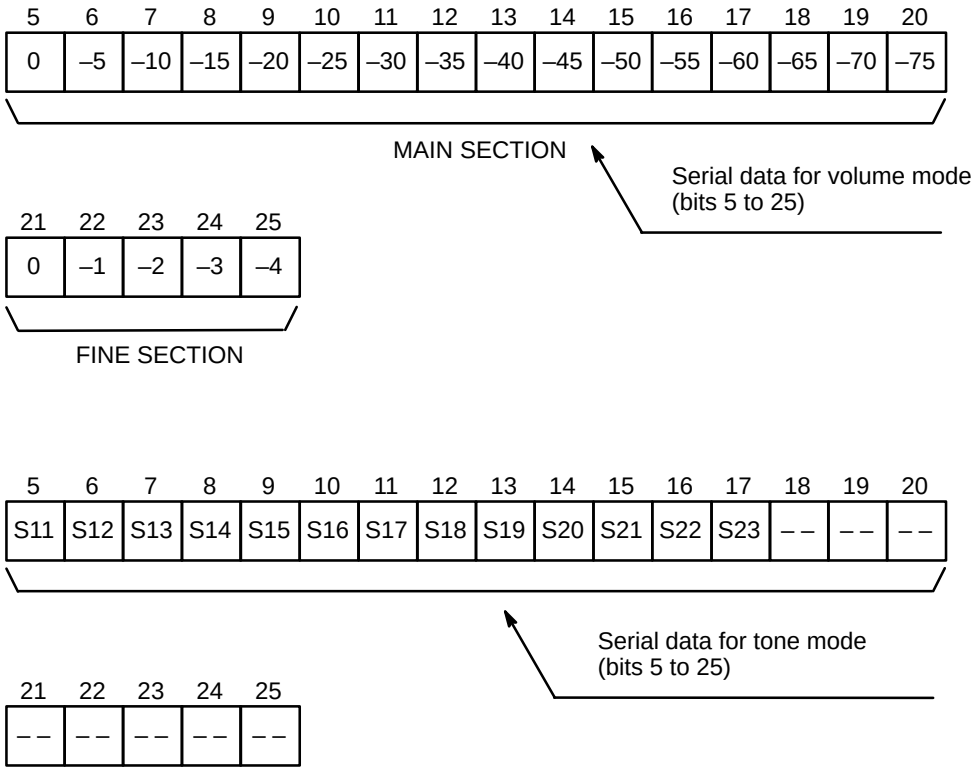
28-bit input data consists of the channel selection data, volume/tone mode selection data, loudness mode selection data, volume step data or tone step data, and address data. Input data format is shown below.



BIT DESCRIPTIONS

Parameter	Bit	Description
CH	1,2	Input data determines which channel is activated. The first bit selects the L-channel and the second bit selects the R-channel. Both channels operate separately. When bits 1 and 2 are high level, data is written. When bits 1 and 2 are low level, the former data is latched. This data is used as right and left balance because R-channel and L-channel can operate respectively.
V/T	3	This bit determines how the 28-bit data is used, as volume control data or as tone control data. When this bit is high level, the 28-bit data is used as volume control data. When this bit is low level, the 28-bit data is used as tone control data.
LOUD	4	Loudness mode selection input. When this bit is high level, the loudness mode is selected. When this bit is low level, loudness mode is not selected.
VOL/TONE STEP	5 to 25	Data input to the V/T bits, specify volume step data or tone step data. When in a volume mode, data to bits 5 to 20 specify the MAIN switch data, and data to bits 21 to 25 specify the FINE switch data. When in a tone mode, data to bits 5 to 17 specify the tone step data. (bits 18 to 25 are ignored and can be set high or low.) The volume step is determined by the combination of MAIN and FINE. Only one arbitrary bit of the MAIN switch (bits 5 to 20) is allowed to be set to high level. Only one arbitrary bit of the FINE switch (bits 21 to 25) is allowed to set high level. No other combination is allowed. When in a tone mode, only one arbitrary bit, of 13 bits (5 to 17 bits) is allowed to be set to high or all bits are set low. No other combination is allowed.

BIT DESCRIPTIONS (Continued)

<table>
<tr><th>Parameter</th><th>Bit</th><th>Description</th></tr>
<tr><td>VOL/TONE STEP</td><td>5 to 25</td><td>


</td></tr>
<tr><td>ADR</td><td>26 to 28</td><td>This data specifies the address bit. Fujitsu uses the address 26 27 28 | 0 | 0 | 1 | as the address of MB87032 . If the address is set as 0, 0, 1, the 28-bit data are acceptable. If other addresses are set, the data will not be accepted.</td></tr>
</table>

VOLUME SECTION SPECIFICATION

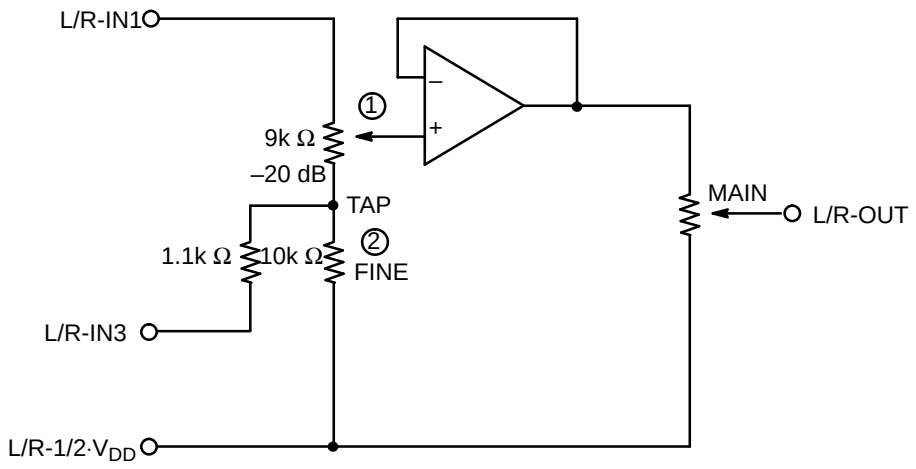
Parameter	Description
Step Number	Attenuation range of 0 to –78 dB every –1 dB step is selected by the combination of the MAIN and FINE sections. The MAIN section varies every –5 dB steps and the FINE section varies every –1 dB step.
– ∞ (Mute)	When volume is set to –79 dB, – ∞ the (Mute) mode is selected.
Volume structure	

Figure 3.

① Attenuation range of 0 to –20 dB; every –1 dB step is selected by ①

② Attenuation range of –20 to –78 dB, – ∞ dB; every –1 dB step is selected by the combination of MAIN and FINE.

TONE SECTION/LOUDNESS SECTION SPECIFICATION

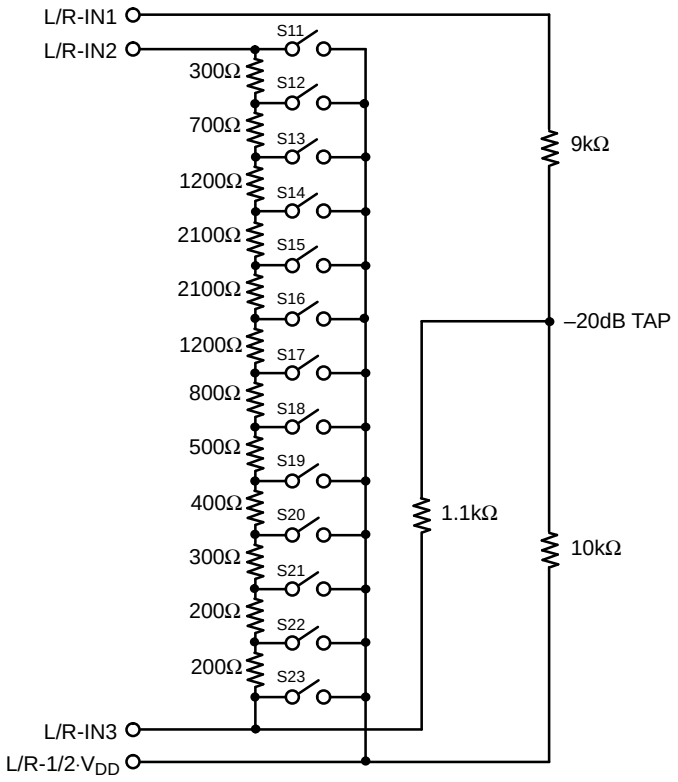
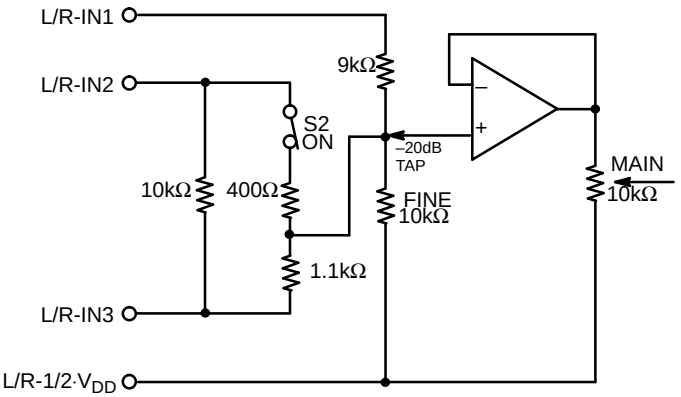
Parameter	Description
Step Number	13 steps
Volune tap	–20 dB
STEP structure (outline)	

Figure 4. Step Structure

LOUDNESS structure (outline)	

When S2 is on, loudness mode is selected. In this case, the tap point is –20 dB.

Figure 5. Loudness Structure

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin No.		Value			Unit
		DIP	FPT	Min	Typ	Max	
Supply Voltage	V_{DD}	16	24	6	8	10	V
Digital Input Voltage	V_{DI}	8, 9, 10	12, 13, 14	0	–	V_{DD}	V
Analog Input Voltage	V_{AI}	2,15	2, 23	–	1	1.4	Vrms
Operating Temperature	T_A	–	–	0	–	70	°C

DC CHARACTERISTICS

(V_{DD} = 8V ± 10%, T_A = 0 to 70°C unless otherwise noted.)

Parameter	Symbol	Pin No.		Value			Unit
		DIP	FPT	Min	Typ	Max	
Reference Voltage	V_{REF}	5,12	6, 19	$1/2 \cdot V_{DD}$–10%	$1/2 \cdot V_{DD}$	$1/2 \cdot V_{DD}$+10%	V
Supply Current*	I_{DD}	16	24	–	6	7	mA
Digital Input High Voltage	V_{IH}	8~10	12~14	2.4	–	V_{DD}	V
Digital Input Low Voltage	V_{IL}	8~10	12~14	0	–	0.4	V

Note: *V_{DD} = 8V

AC CHARACTERISTICS

(V_{DD} = 8V ± 10%, T_A = 0 to 70°C unless otherwise noted.)

Parameter	Symbol	Pin No.		Condition	Value			Unit
		DIP	FPT		Min	Typ	Max	
Analog Input Voltage	V_{AI}	2,15	2, 23		–	1	–	Vrms
Analog Input Frequency	A_f	2,15	2, 23		40	–	20000	Hz
Attenuation	–	6,11	8, 17	Referenced to $1/2 \cdot V_{DD}$ pin	0	–	–78	dB
Attenuation at Mute mode	–	6,11	8, 17	0 dBV = 1Vrms	–	–	–80	dB
Attenuation Differential Error*	ΔATT	6,11	8, 17	Referenced to $1/2 \cdot V_{DD}$ pin	–0.5	–	0.5	dB
L-R Attenuation Differential Error	ΔLR	6,11	8, 17	Referenced to $1/2 \cdot V_{DD}$ pin	–0.5	–	0.5	dB
Total Harmonic Distortion	THD	6,11	8, 17	Output = 100mVrms Attenuation = 0dB	–	0.01	0.05	%
Tone Total Resistance	R_{TONE}	3,14	4, 21		6	10	14	kΩ
Volume Switch ON Resistance	–			T_A = 25°C	–	300	500	Ω
Tone Switch ON Resistance	–			T_A = 25°C	–	200	300	Ω

Note: *Step error (1dB ± 0.5dB) when volume is changed ±1 step.

AC CHARACTERISTICS (Continued)

(V_{DD} = 8V ± 10%, T_A = 0 to 70°C unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Clock/Strobe Signal Pulse Width	t_{CW}	300	-	-	ns
Input Clock Signal Period	t_{CK}	500	-	-	ns
Input Storobe Signal Period	t_{CS}	14500	-	-	ns
Time Between CK(28) and CS	t_{SW1}	500	-	-	ns
Time Between CS and CK(1)	t_{SW2}	500	-	-	ns
Data Set-up Time	t_{SD}	150	-	-	ns
Data Hold Time	t_{HD}	200	-	-	ns
Rise Time	t_r	-	-	50	ns
Fall Time	t_f	-	-	50	ns

Note: Serial 28-bit data is input by the falling edge of CK signal.
Serial 28-bit data is latched in internal latch by the falling edge of CS signal.
Access to the clock and data while CS signal is falling, is prohibited.

Figure 6. Timing Chart

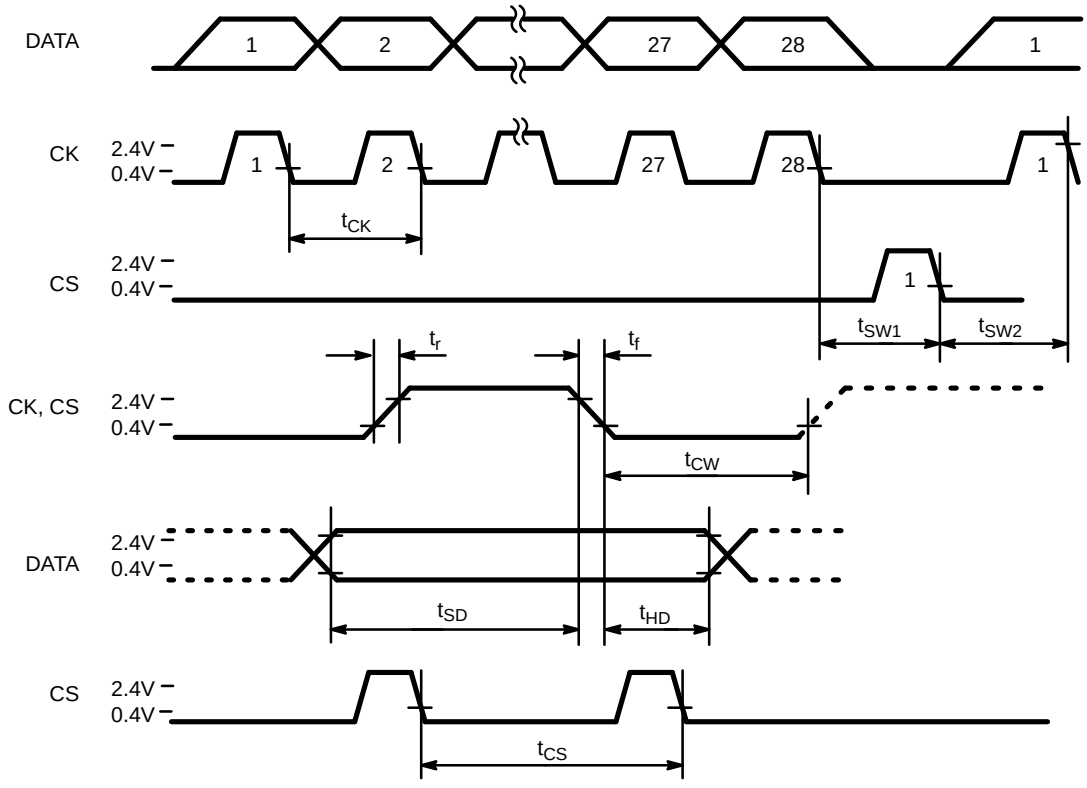
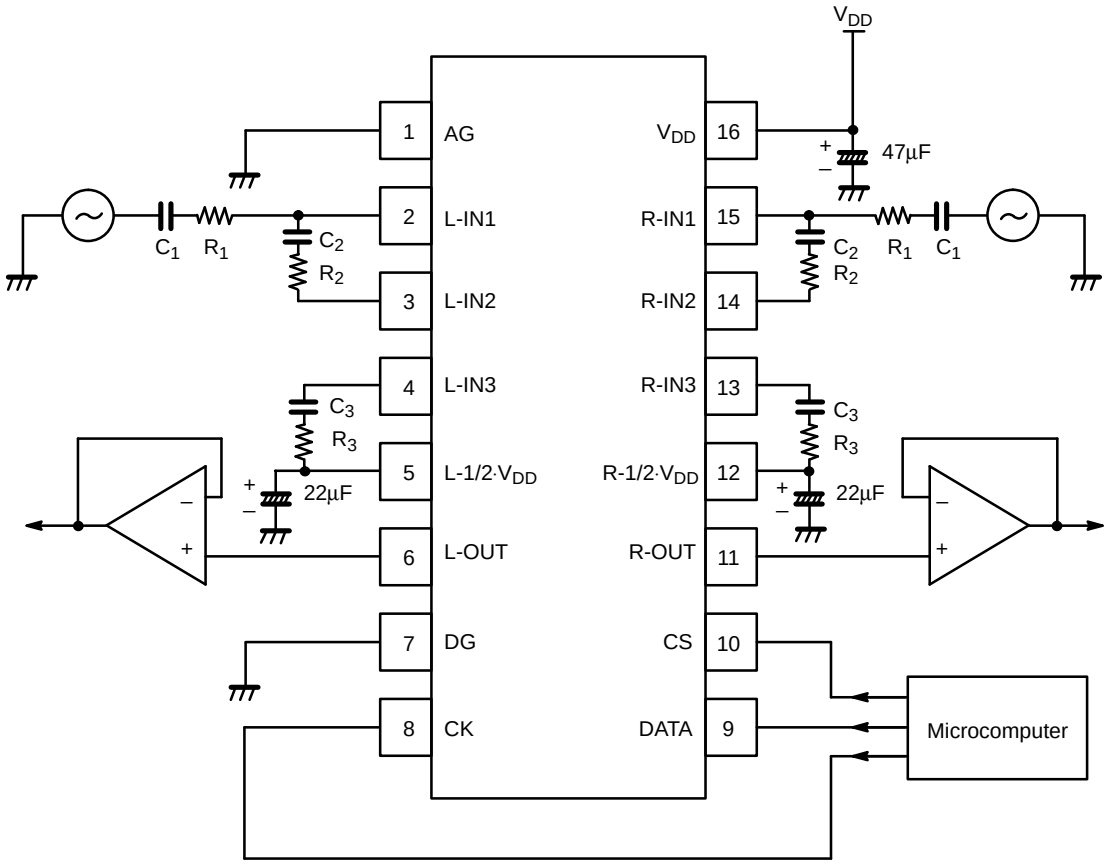


Figure 7. Application Example Circuit (for Dip Package)



Mode	TONE S11 to S23	LOUD S2	R1	R2	R3	C1	C2	C3	Note
VOL. BAL.	OFF	OFF	Short	Open	Short	1µF	Open	Short	Volume, right and left balance
VOL. BAL. LOUD	OFF	ON	Short	2.2kΩ	0.22kΩ	1µF	0.0047µF	0.22µF	Volume, balance, loudness
VOL. BAL. TONE1	One arbitrary bit is set to ON	OFF	4.7kΩ	Short	Short	1µF	0.1µF	1µF	Volume, balance, TONE
VOL. BAL. TONE2	One arbitrary bit is set to ON	OFF	4.7kΩ	Short	Short	1µF	0.1µF	Short	Simple Hi Cut-TONE

TYPICAL CHARACTERISTICS CURVES

Figure 8. Tone Characteristics

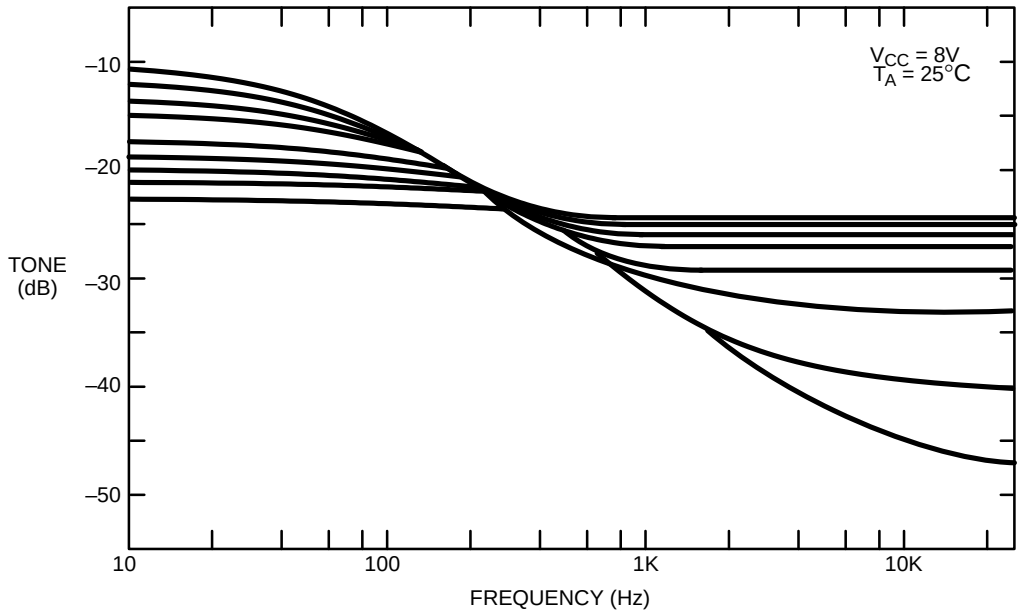
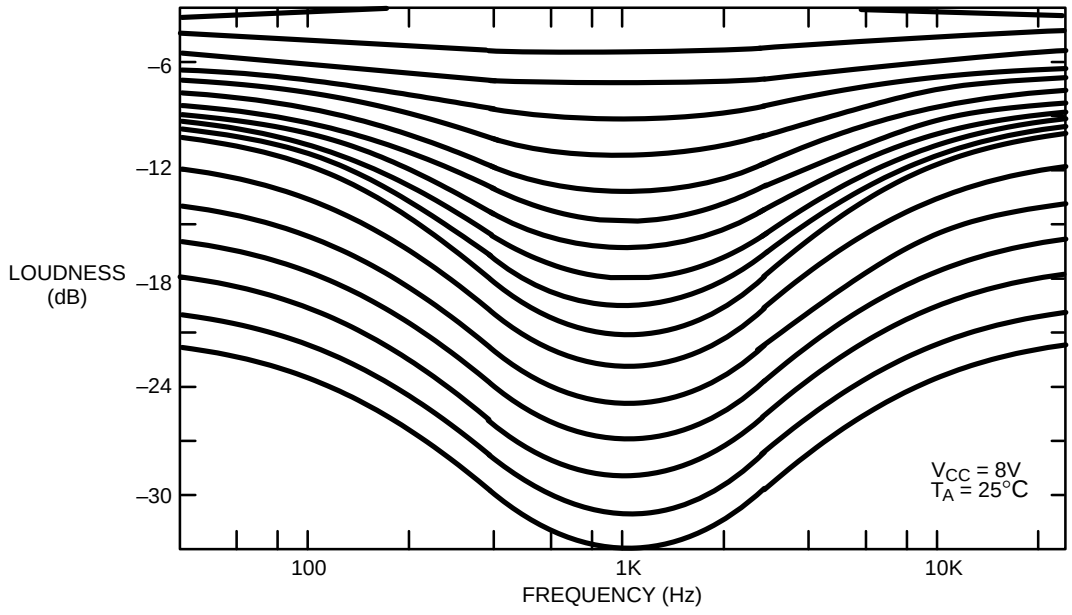


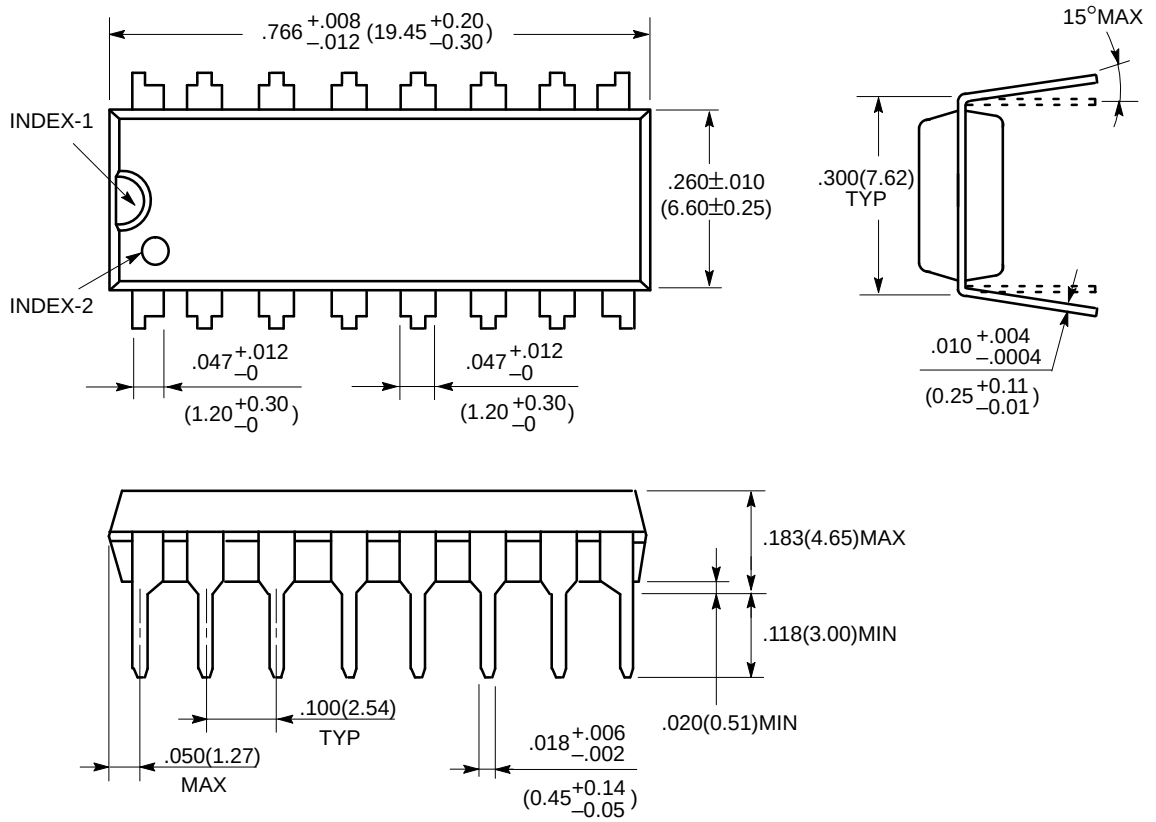
Figure 9. Loudness Characteristics



Note: These curves depend upon the application circuit.

PACKAGE DIMENSIONS

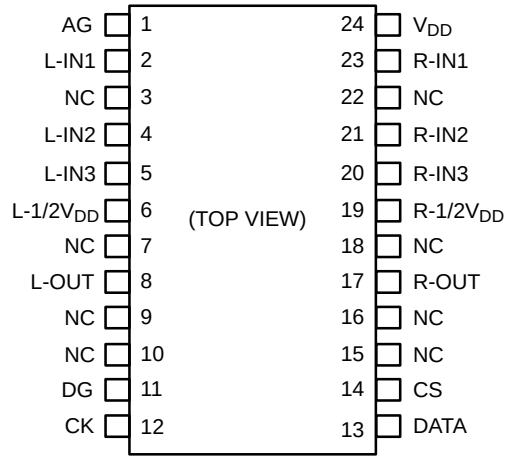
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



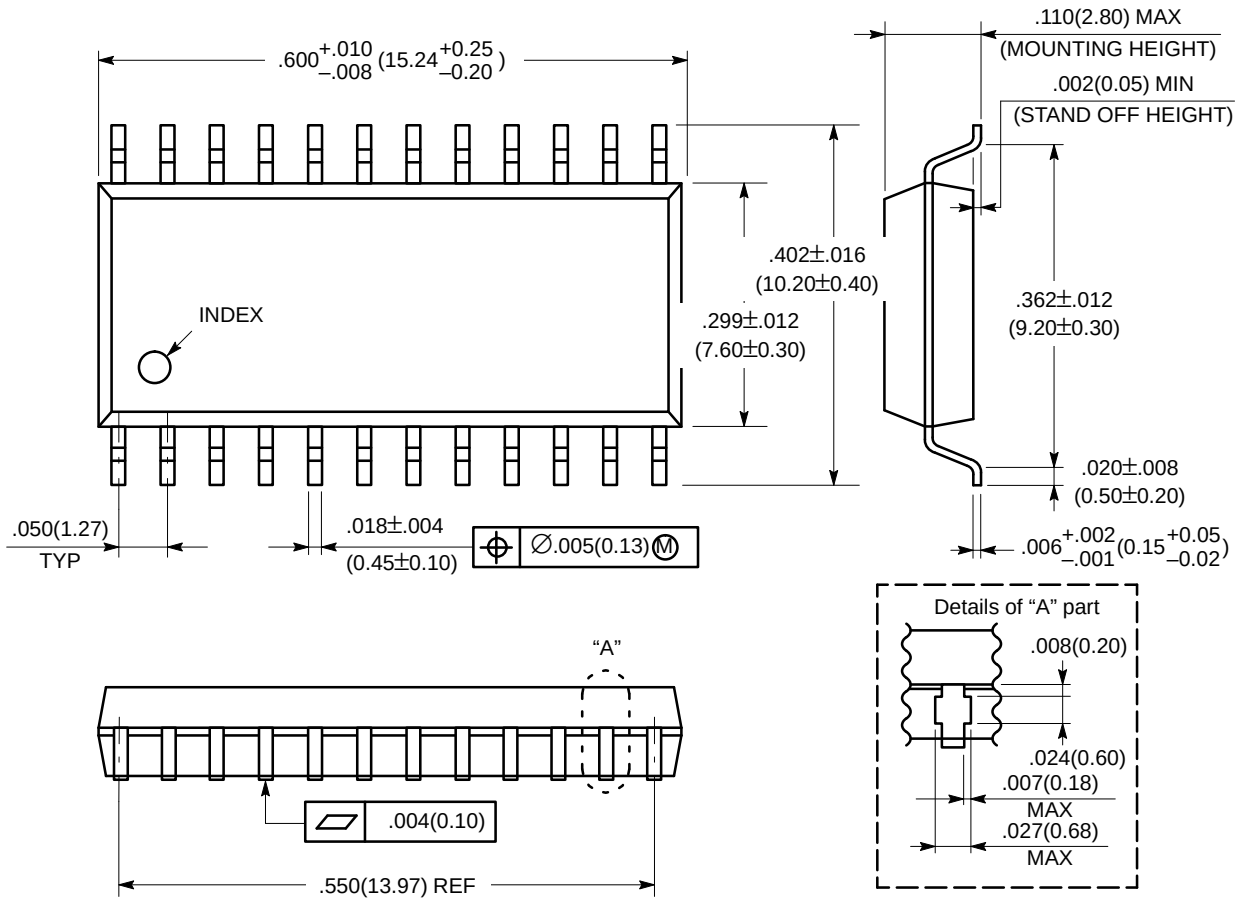
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

Pin Assgnment



24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



Dimensions in
inches (millimeters)

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg., 6–1, Marunouchi 2–chome
Chiyoda–ku, Tokyo 100, Japan
Tel: (03) 216–3211
Telex: 781–2224361
FAX: (03) 216–9771

North and South America
FUJITSU MICROELECTRONICS, INC.
Integrated Circuits Division
3545 North First Street
San Jose, CA 95134–1804 USA
Tel: 408–922–9000
Telex: 910–671–4915
FAX: 408–432–9044

Europe
FUJITSU MIKROELEKTRONIK GmbH
Arabella Centre 9.OG
Lyoner Strasse 44–48
D–6000 Frankfurt 71
F.R. Germany
Tel: (069) 66320
Telex: 411963
FAX: (069) 6632122

Asia
FUJITSU MICROELECTRONICS ASIA PTE LIMITED
51 Bras Basah Road,
Plaza By The Park, #06–04/07,
Singapore 0718
Tel: 336–1600
Telex: 55573
FAX: 336–1609

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