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FUJITSU

PRODUCT PROFILE SHEET

MB85502-010/-012/-015

CMOS 8M x 36 Synchronous DRAM Module

CMOS 8M x 36 Bit Synchronous DRAM Module

The Fujitsu MB85502 is a fully decoded, CMOS Synchronous Dynamic Random Access Memory (SDRAM) module consisting of eighteen MB81116421 devices which organized as two banks of 2,097,152-word x 4-bit. The MB85502 organized as 8,388,608 x 36-bit is optimized for those applications requiring high speed, high performance, large memory shortage, and high density memory organizations.
This module is ideally suited for supercomputers, workstations, laser printers, high resolution graphic adapters, accelerators and other applications where a simple interface is needed.
The all inputs/ outputs are LVTTL compatible, and supply voltage tolerance is ±9%.

See page 8

MSS–72P–P70

DQ0	2	1	VSS
DQ2	4	3	DQ1
DQ4	6	5	DQ3
DQ6	8	7	DQ5
VCC	10	9	DQ7
DQ9	12	11	DQ8
DQ11	14	13	DQ10
DQ13	16	15	DQ12
DQ14	18	17	VSS
NC	20	19	DQ15
$\overline{CS}$1	22	21	$\overline{CS}$0
A2	24	23	A3
VCC	26	25	A1
A10	28	27	A0
NC	30	29	A11
$\overline{RAS}$	32	31	VSS
$\overline{WE}$	34	33	$\overline{CAS}$
A5	36	35	A4
A7	38	37	A6
A9	40	39	A8
VSS	42	41	NC
CKE1	44	43	CKE0
CLK	46	45	CLK-RTN
DQM0	48	47	VCC
DQ16	50	49	DQM1
DQ18	52	51	DQ17
DQ20	54	53	DQ19
VSS	56	55	DQ21
DQ23	58	57	DQ22
DQ25	60	59	DQ24
DQ26	62	61	VCC
DQ28	64	63	DQ27
DQ30	66	65	DQ29
DQ32	68	67	DQ31
DQ34	70	69	DQ33
VSS	72	71	DQ35

PRODUCT LINE & FEATURES

Parameters	MB85502-010	MB85502-012	MB85502-015
Clock Frequency	100 MHz max	83 MHz max	66 MHz max
Burst Mode Cycle Time	10 ns min	12 ns min	15 ns min
$\overline{RAS}$ Access Time	62 ns max	71 ns max	79 ns max
$\overline{CAS}$ Access Time	32 ns max	36 ns max	39 ns max
Output Valid From Clock(CL=3)	12 ns max	13 ns max	14 ns max
Operating Current (Burst Mode)	6757mW max	6199mW max	5641mW max
Power Down Mode Current	436mW max (ADD=L)		

- 8M words x 36 bits (MB81116421 x 18)
- 72 pin socket type (pin pitch 1.27mm)
- 100MHz (Max.) data transfer
- +3.3V±0.3V supply voltage
- 4096 refresh cycles every 65.6 ms
- Dual bank operation
- LVTTL compatible I/O
- Programmable burst type
- Programmable burst length
- Auto and Self–refresh
- CKE power down mode
- Output Enable and Input Data Mask

ABSOLUTE MAXIMUM RATINGS (See NOTE.)

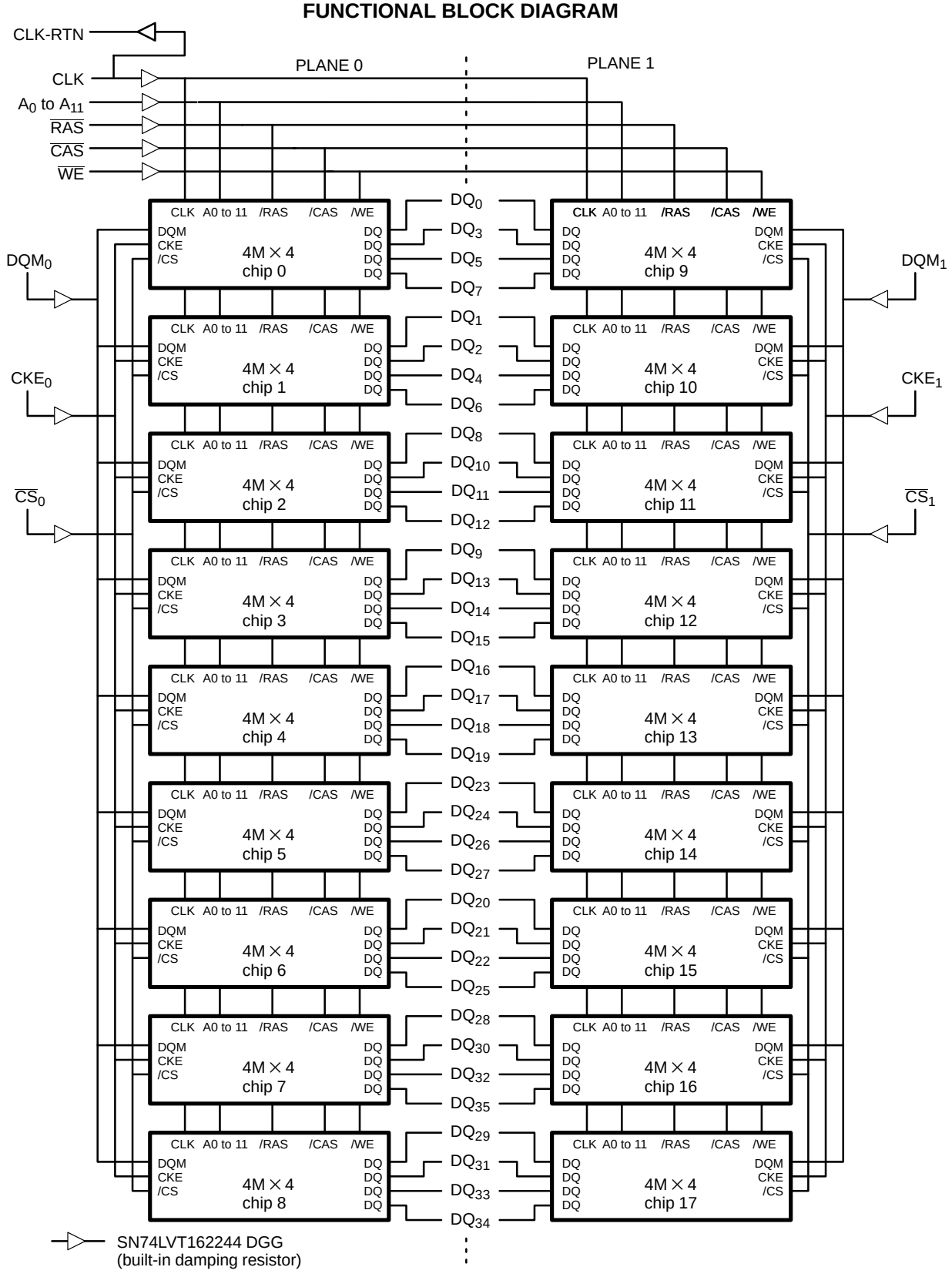
Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +4.6	V *1
Input Voltage	V_{IN}	–0.5 to +4.6	V *1
Output Voltage	V_{OUT}	–0.5 to +4.6	V *1
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	24	W
Storage Temperature	T_{STG}	–55 to +125	°C

*1 VSS=0V

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol		Value			Unit	Ambient Operating Temp.
				Min	Typ	Max		
Supply Voltage	*1	V_{CC}		3.0	3.3	3.6	V	0 °C to + 70 °C
		V_{SS}		0	0	0		
Input High Voltage, all inputs	*1 *2	LVTTL	V_{IH}	2.0	—	VCC+0.3	V	
Input Low Voltage, all inputs	*1 *2		V_{IL}	–0.3	—	0.8	V	

*1 **:** VSS=0V.
*2 : Ambient temp. depend on cycle time and cooling conditions.

NOTE: This figures are recommened value to guarantee LSI's normal operation.
Requirements of electric characteristics (DC/AD) is guaranteed within this value.

CAPACITANCE (TA=25°C, f=1MHz, VCC=3.3V)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A11	C_{IN1}	—	16	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	16	pF
Input Capacitance, CLK	C_{IN3}	—	16	pF
Input Capacitance, DQM0, DQM1	C_{IN4}	—	16	pF
Input Capacitance, CKE0, CKE1	C_{IN5}	—	16	pF
Input Capacitance, $\overline{CS0}$, $\overline{CS1}$	C_{IN6}	—	16	pF
I/O Capacitance, (DQ0-35)	C_{DQ}	—	22	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value		Unit
				Min	Max	
Input Leakage Current	All inputs except DQ	I_{LI}	V_{IN} = 0V	–10	10	µA
			V_{IN} = V_{CC}	–10	10	
Input Hold Current		I_{I} (Hold)	V_{IN} = 0.8V	75	—	µA
			V_{IN} = 2V	—	–75	
Output Leakage Current		I_{LO}	0V ≤ V_{IN} ≤ V_{CC} Output high impedance	–20	20	µA
Output High Voltage [1]	LVTTL	V_{OH}	I_{OH} = –2.0mA	2.4	—	V
Output Low Voltage [1]		V_{OL}	I_{OL} = +2.0mA	—	0.4	V
Operating Current (Average Power Supply Current) [2]	MB85502-010	I_{CC1S}	No Burst : t_{CLK} = min. One bank active	–	1282 (202)	mA
	MB85502-012				1204 (169)	
	MB85502-015				1126 (136)	
	MB85502-010	I_{CC1D}	No Burst : t_{CLK} = min. Two banks active	–	1724 (284)	mA
	MB85502-012				1588 (238)	
	MB85502-015				1451 (191)	
Precharge Standby Current (Power Supply Current) [2]	ADD=Fix ”L”	I_{CC2P}	CKE = V_{IL} Two banks idle t_{CLK} = min. Power down mode	–	121 (103)	mA
	ADD=Fix ”H”				117 (99)	
	ADD=Change				248 (230)	
	ADD=Fix ”L”	I_{CC2N}	CKE = V_{IH} Two banks idle t_{CLK} = min.	–	641 (102)	mA
	ADD=Fix ”H”				639 (99)	
	ADD=Change				770 (230)	
Active Standby Current (Power Supply Current) [2]	ADD=Fix ”L”	I_{CC3P}	CKE = V_{IL} One bank active t_{CLK} = min.	–	642 (103)	mA
	ADD=Fix ”H”				639 (99)	
	ADD=Change				770 (230)	
	ADD=Fix ”L”	I_{CC3N}	CKE = V_{IH} One bank active t_{CLK} = min.	–	912 (102)	mA
	ADD=Fix ”H”				909 (99)	
	ADD=Change				1040 (230)	
Burst Mode Current (Average Power Supply Current) [2]	MB85502-010	I_{CC4}	t_{CLK} = min.	–	1877 (392)	mA
	MB85502-012				1722 (327)	
	MB85502-015				1567 (262)	

DC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value		Unit
				Min	Max	
Refresh Current #1 (Average Power Supply Current) [2]	MB85502-010	I_{CC5S}	One bank active Auto-Refresh; t_{CLK} = min, t_{RC}=min. ADD=Fix Low	–	1198 (118)	mA
	MB85502-012				1134 (99)	
	MB85502-015				1070 (80)	
	MB85502-010	I_{CC5D}	Two banks active Auto-Refresh; t_{CLK} = min. t_{RC}=min. t_{RRD} = min. ADD=Fix Low	–	1575 (145)	mA
	MB85502-012				1463 (113)	
	MB85502-015				1351 (91)	
Refresh Current #2 (Average Power Supply Current) [2]		I_{CC6}	Self-Refresh; CKE = V_{IL} ADD=Fix Low	–	382 (103)	mA

1. VSS=0V
2. ICC depends on output pin, load condition and number of clock cycle.

Note: All figures except for I_{CC2P} are value for one side (stand by = I_{CC2N}) operation.
( ) shows supply consumption of driver, V_{IH} = V_{CC}.
ADD = Change is the value of change at burst mode 100MHz.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) **Note 1, 2, 3**

Parameter	Notes	Symbol	MB85502-010		MB85502-012		MB85502-015		Unit
			Min	Max	Min	Max	Min	Max	
Clock Period	CAS latency=3	tCLK	10	100	12	100	15	100	ns
	CAS latency=2		15		17.5		20		ns
	CAS latency=1 [4]		30		35		40		ns
Clock High Time		tCH	4	–	4	–	4	–	ns
Clock Low Time		tCL	4	–	4	–	4	–	ns
$\overline{CS}$ Setup Time		tSC	3	–	3	–	3	–	ns
$\overline{CS}$ Hold Time		tHC	3	–	3	–	3	–	ns
Input Setup Time		tSI	3	–	3	–	3	–	ns
Input Hold Time		tHI	3	–	3	–	3	–	ns
Data Input Setup Time *		tSID	0	–	0	–	0	–	ns
Data Input Hold Time *		tHID	7	–	7	–	7	–	ns
Output Valid from Clock (tCLK=min.) [5, 6]	CAS latency=3	tAC	–	12	–	13	–	14	ns
	CAS latency=2			17		18.5		20	ns
	CAS latency=1			32		36		39	ns
Output in Low-Z		tOLZ	5	–	5	–	5	–	ns
Output in High-Z		tOHZ	4	15	4	17	4	20	ns
Output Hold Time [7]		tOH	4	–	4	–	4	–	ns
Time between Refresh		tREF	–	65.6	–	65.6	–	65.6	ms
Transition Time		tT	0.5	2	0.5	2	0.5	2	ns
Power Down Exit Time		tPDE	13	–	15	–	18	–	ns

* DQ0 to DQ35 (DIN input)

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.) Note 1, 2,3

BASE VALUES FOR CLOCK COUNT / LATENCY

Parameter	Notes	Symbol	MB85502-010		MB85502-012		MB85502-015		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{RAS}$ Cycle Time	8	tRC	100	–	110	–	120	–	ns
$\overline{RAS}$ Access Time	9	tRAC	–	62	–	71	–	79	ns
$\overline{CAS}$ Access Time	10, 12	tCAC	–	32	–	36	–	39	ns
$\overline{RAS}$ Precharge Time		tRP	40	–	40	–	40	–	ns
$\overline{RAS}$ Active Time		tRAS	60	10000	70	10000	80	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11	tRCD	30	–	35	–	40	–	ns
Write Recovery Time		tWR	20	–	20	–	25	–	ns
$\overline{RAS}$ to $\overline{CAS}$ Bank Active Delay Time		tRRD	30	–	35	–	40	–	ns

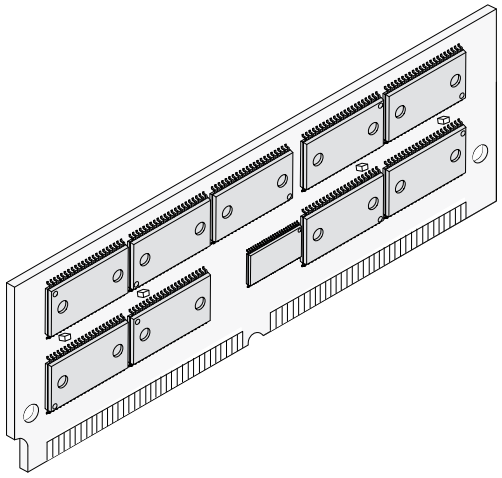
Notes:

1. An initial pause (DESL on NOP) of 200µs is required after power-up followed by a minimum of eight Auto-Refresh cycles.
2. 1.4V or VREF is the reference level for measuring timing of input signals. Transition times are measured between VIH (min) and VIL (max).
3. AC characteristics assume tT = 1ns and 30pF of capacitive load.
4. Maximum value is a reference value.
5. Assumes tRCD and tCAC are satisfied.
6. tAC also specifies the access time at burst mode except for first access.
7. Specified where output buffer is no longer driven.
8. Actual clock count of tRC (lRC) will be sum of clock count of tRAS (lRAS) and tRP (lRP).
9. tRAC is a reference value. Maximum value is obtained from the sum of tRCD (min) and tCAC (max).
10. Assumes tRAC and tAC are satisfied.
11. Operation within the tRCD (min) ensures that tRAC can be met; if tRCD is greater than the specified tRCD (min), access time is determined by tCAC or tAC.
12. ICAC is programmed at mode register.

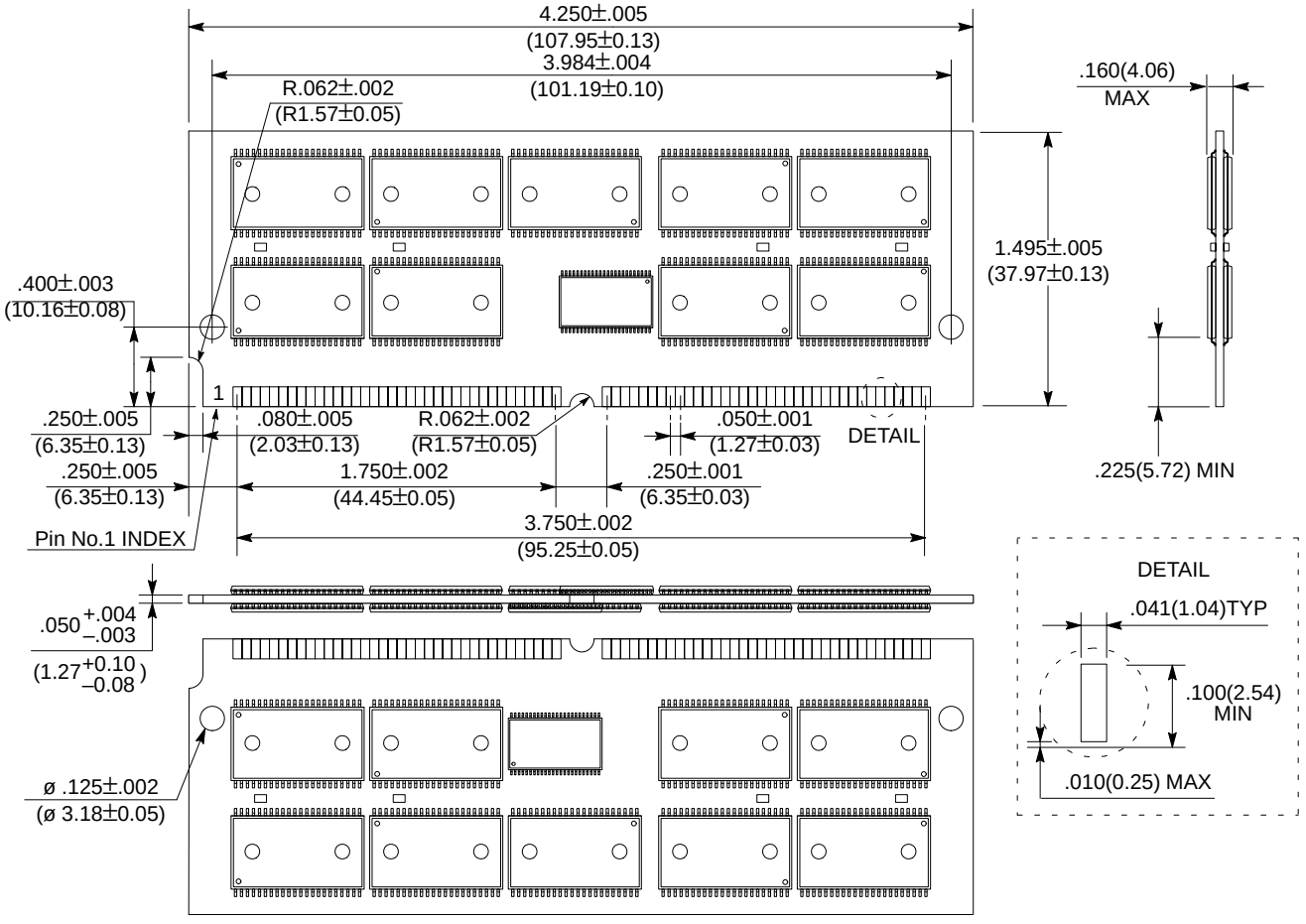
*Source: See MB81116421 Data Sheet for detailes on the electricals.

PACKAGE DIMENSIONS

(Suffix: PTPBK)



72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P70)



Dimensions in
inches (millimeters)