– PRELIMINARY –

Nov. 1994
Edition 2.0

PRODUCT PROFILE SHEET

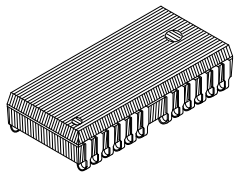
MB8116100A-50/-60/-70/-80

CMOS 16M x 1 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 16,777,216 x 1 Bit Fast Page Mode Dynamic RAM

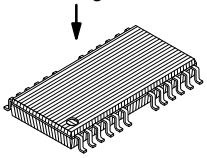
The Fujitsu MB8116100A is a fully decoded CMOS Dynamic RAM (DRAM) that contains a total of 16,777,216 memory cells in a x1 configuration. The MB8116100A features a "fast page" mode of operation whereby high–speed random access of up to 4,096–bits of data within the same row can be selected. The MB8116100A DRAM is ideally suited for mainframe, buffers, hand–held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB8116100A is very small, the device can be used as a non–volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB8116100A is fabricated using silicon gate CMOS and Fujitsu's advanced four–layer polysilicon and two layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB8116100A are not critical and all inputs are TTL compatible.



Plastic SOJ Package
(LCC–26P–M09)

Marking side



Plastic TSOP Packages
(FPT–26P–M05)
(Normal Bend)

PRODUCT LINE & FEATURES

Parameter	MB8116100A -50	MB8116100A -60	MB8116100A -70	MB8116100A -80
$\overline{RAS}$ Access Time	50ns max.	60ns max.	70ns max.	80ns max.
Randam Cycle Time	90ns min.	110ns min.	130ns min.	150ns min.
Address Access Time	25ns min.	30ns max.	35ns max.	40ns max.
$\overline{CAS}$ Access Time	13ns max.	15ns max.	17ns max.	20ns max.
Fast Page Mode Cycle Time	35ns min.	40ns min.	45ns min.	50ns min.
Low Power Dissipation • Operating current	550mW max.	467.5mW max.	385mW max.	330mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)			

- 16,777,216 words x 1 bit organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are TTL compatible
- 4096 refresh cycles every 65.6ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read–Modify–Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN} , V_{OUT}	–0.5 to + 7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	–0.5 to + 7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Operating Temperature	T_{OPE}	0 to 70	°C
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package and Ordering Information

– 26–pin plastic (300mil) SOJ,
order as MB8116100A–xxPJ

– 26–pin plastic (300mil) TSOP–II
with normal bend leads,
order as MB8116100A–xxPFTN

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.