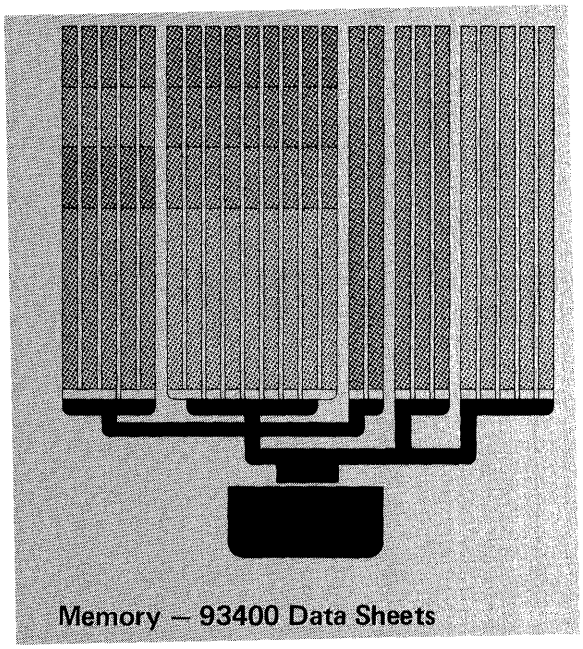


Memory – 93400 Data Sheets

TTL MEMORY 93400 • 93400B • 93401

256-BIT READ/WRITE MEMORY & DECODER/DRIVER

FORMERLY 4100 • 4100B • 4101

DESCRIPTION – The 93400 256-Bit Read/Write Memory and the 93401 Decoder/Driver are components for use in high speed memory systems. The 93400 is a fast 256 x 1 random access read/write memory which is addressed with a partially decoded x-y coincident selection scheme. There are two device grades, with the 93400B having a slower access time than the 93400. The companion decoder and buffer driver, 93401, converts binary addresses into the partially decoded form required by the 93400, and provides sufficient drive to connect to 32 93400's. Both devices are supplied in 16-lead Dual In-Line Packages.

93400/93400B

- TTL COMPATIBLE
- 16-LEAD PACKAGE
- OUTPUT WIRED–OR CAPABILITY
- 70 ns TYPICAL ACCESS TIME (93400)
- 125 ns TYPICAL ACCESS TIME (93400B)
- LOW INPUT LOADING

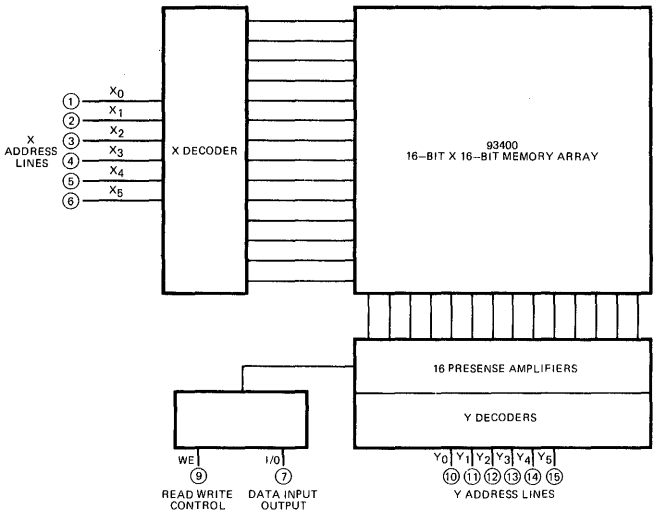
93401

- TTL COMPATIBLE
- 16-LEAD PACKAGE
- 20 ns TYPICAL THROUGH DELAY
- LOW INPUT LOADING
- 4 ENABLE INPUTS FOR CHIP SELECTION
- DRIVES UP TO 32 93400's

ABSOLUTE MAXIMUM RATINGS

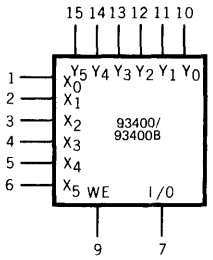
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
Input Voltage	–0.5 V to +5.25 V
Voltage Applied to Output when Output is HIGH	–0.5 V to +V_{CC}
Current into Output when Output is LOW	+25 mA
Storage Temperature	–65°C to +150°C

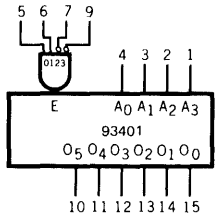
LOGIC DIAGRAM



○ = PIN NUMBERS

LOGIC SYMBOLS

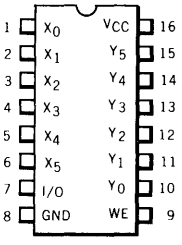




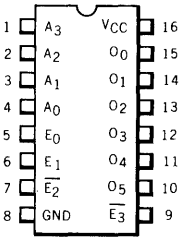
V_{CC} = Pin 16
Gnd = Pin 8

CONNECTION DIAGRAMS
(TOP VIEWS)

93400/93400B



93401



9

FUNCTIONAL DESCRIPTIONS

The 93400 and 93400B contain 256 bipolar storage cells arranged in a 16 by 16 format. Any one of the 256 cells may be accessed by supplying an address code on the X address inputs and the Y address inputs. Internal decoders decode the X and Y addresses into one of 16 rows and one of 16 columns in the matrix of storage cells. Data may be written into or read out from the cell lying at the intersection of the selected row and column.

The X and Y addresses supplied to the 93400 and 93400B are partially decoded in a "3 of 6" code. Of the six X address lines and the six Y address lines there are always three lines HIGH and three lines LOW. There are 20 such combinations, 16 are decoded by the internal row and column decoders. The four unused combinations of 3 of 6 will not select any row or column. If there are more than three lines HIGH in either the X or Y address, then multiple row or column selection will occur. The sixteen 3 of 6 codes used by the 93400 and 93400B are generated by the 93401 decoder/driver.

Data enters and leaves the memory on a single input/output (I/O) line (pin 7). The I/O line is an open collector output, so many 93400 I/O lines can be connected together in a wired-OR configuration. Input data must be applied to the I/O lines through an open collector gate. Each I/O line requires a pull-up resistor to V_{CC}. The magnitude of the pull-up resistor is determined by the number of 93400 I/O lines tied together. The I/O of a 93400 which is not addressed will be HIGH.

Read/Write selection is determined by the state of pin 9, the active HIGH write enable. When WE is HIGH, the data on the I/O line will be written into the selected address in the 93400. When the Write Enable line is LOW, data will be read out of the addressed location.

The 93401 is a partial decoder and driver for the 93400. It accepts a 4-bit binary code on the address inputs (A_0–A_3) and produces a 3 of 6 code on the six output pins (O_0–O_5). The decoder also features four separate enables, two active HIGH and two active LOW. All four enables must be active before the decoder will produce a 3 of 6 code. Since two of the enables are HIGH and two are LOW, it is possible to route two binary coded lines to four different 93401's to get two additional bits of decoding with no extra packages.

Ordinarily in memory systems, 93400 memory devices will be arranged in a matrix of rows and columns. Each column will store a particular bit and each row of 93400's will be 256 words. A 93401 driver will be used for each row and each column in the matrix. One 93401 can drive up to 32 93400 X or Y address lines. The usual driving scheme is to connect the four LSB's of address to each of the column decoders. The next four bits of address are connected to each of the row decoders. Additional address bits are decoded to the chip selects on the row decoders. Each column decoder drives the Y address lines on up to 32 93400's in a column. Each row decoder drives the address lines on up to 32 93400's in a row.

THE THREE OF SIX CODE

The "3 of 6" code used in the 93400 and produced by the 93401 is a tradeoff between memory chip complexity and pin count. The simplest 256-bit memory chip would be a 16 by 16 matrix of storage cells, with all 16 rows and 16 column select lines brought off chip. The lowest pin count for a 256-bit memory chip would be achieved by fully decoded X and Y select lines reducing the 32 lines of the simple scheme to only 8 lines. However, full binary decoding of the X and Y lines on chip significantly increases to complexity of the memory chip. The 93400 and 93401 are designed to gain the good features of both alternatives. The 16 X and Y lines are decoded into 6 lines each, allowing the memory to fit into a 16-lead package and still keeping the memory chip fairly simple, since the 3 of 6 code does not require a complex decoder. The table on the right below shows the conversion of 4-bit binary to 3 of 6 code by the 93401, and also the internal column or row selected by the 3 of 6 to 1 of 16 decoder inside the 93400.

TTL LOAD AND DRIVE FACTORS

93400 • 93400B

INPUT	LOAD
X Lines Y Lines WE	0.33/0.125
OUTPUT	**DRIVE FACTOR**
Output I/O	Open Collector 3.1

93401

INPUT	LOAD
E_0, E_1 E_2, E_3 A_0, A_1, A_2, A_3	0.33/0.25
OUTPUT	**DRIVE FACTOR**
0_0, 0_1, 0_2, 0_3, 0_4, 0_5	16/6

Numerator = HIGH level load
(1 load = 0.06 mA)
Denominator = LOW level load
(1 load = 1.6 mA)

CODE CONVERSION EQUATIONS

$$O_0 = \overline{A_3}$$

$$O_1 = \overline{(A_1 + A_0)\,(\overline{A_3} + A_1)\,(\overline{A_2} + A_0)}$$

$$O_2 = \overline{(A_1 + \overline{A_0})\,(\overline{A_3} + \overline{A_0})\,(A_2 + \overline{A_1})}$$

$$O_3 = \overline{(\overline{A_1} + A_0)\,(\overline{A_3} + A_0)\,(\overline{A_2} + \overline{A_1})}$$

$$O_4 = \overline{(\overline{A_1} + \overline{A_0})\,(\overline{A_3} + \overline{A_1})\,(\overline{A_2} + \overline{A_0})}$$

$$O_5 = \overline{A_2}$$

TRUTH TABLE

BINARY INPUT TO 93401				3 OF 6 CODE OUTPUT OF 93401; INPUT TO 93400 (L = O OR X OR Y)						93400 93400B INTERNAL X OR Y ADDRESS
A_3	A_2	A_1	A_0	L_0	L_1	L_2	L_3	L_4	L_5	Row or Column
L	L	L	L	H	H	L	L	L	H	0
L	L	L	H	H	L	H	L	L	H	1
L	L	H	L	H	L	L	H	L	H	2
L	L	H	H	H	L	L	L	H	H	3
L	H	L	L	H	H	H	L	L	L	4
L	H	L	H	H	L	H	L	H	L	5
L	H	H	L	H	H	L	H	L	L	6
L	H	H	H	H	L	L	H	H	L	7
H	L	L	L	L	H	L	H	L	H	8
H	L	L	H	L	H	H	L	L	H	9
H	L	H	L	L	L	L	H	H	H	10
H	L	H	H	L	L	H	L	H	H	11
H	H	L	L	L	H	H	H	L	L	12
H	H	L	H	L	H	H	L	H	L	13
H	H	H	L	L	H	L	H	H	L	14
H	H	H	H	L	L	H	H	H	L	15

NOTE: Enables on 93401 must be LLHH. Any other state on the enable inputs causes 93401 outputs to go LOW, and addresses no internal row or column in the 93400 memory matrix.

93400 • 93400B ELECTRICAL CHARACTERISTICS (T_C = 0°C to 75°C in operation; V_{CC} = 5.0 V ±5%) (Part No. 93400XC/93400BXC)*

SYMBOL	PARAMETER	LIMITS 0°C MIN.	MAX.	25°C MIN.	TYP.	MAX.	75°C MIN.	MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OL}	Output LOW Voltage		0.45		0.20	0.45		0.45	Volts	I_{OL} = 5 mA; V_{CC} = 4.75 V,
								0.55		I_{OL} = 10 mA; See Figure 3.
I_{CE}	Output Leakage Current		100			100		100	μA	V_{CC} = 5.25 V, V_{CE} = 4.5 V All Inputs Grounded
V_{IL}	Address, Write Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed LOW Input Threshold
V_{IH}	Address, Write Input HIGH Voltage	2.0		2.0			2.0		Volts	Guaranteed HIGH Input Threshold
I_{FI}	Data Input Forward Current		-250			-250		-250	μA	V_{CC} = 5.25 V, V_F = 0.45 V
I_{FX}	X Address Input Forward Current		-250			-250		-250	μA	V_F = 0.45 V, V_{CC} = 5.25 V 2 other X Lines. 3 Y Lines @ 4.5 V Remaining X and Y Lines @ .45 V
I_{FY}	Y Address Input Forward Current		-250			-250		-250	μA	V_F = 0.45 V, V_{CC} = 5.25 V 2 other Y Lines. 3 X Lines @ 4.5 V Remaining X and Y Lines @ .45 V
I_{RX}	Address Input		20			20		20	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{RY}	Leakage Current		20			20		20		Other X and Y inputs grounded
I_{FW}	Write Input Forward Current		-250			-250		-250	μA	V_{CC} = 5.25 V, V_F = 0.45 V
I_{RW}	Write Input Leakage Current		20			20		20	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{CC}	Power Supply Current				100	140			mA	V_{CC} = 5.0 V, all inputs at ground

93401 ELECTRICAL CHARACTERISTICS (T_C = 0°C to 75°C in operation; V_{CC} = 5.0 V ±5%) (Part No. 93401XC)*

SYMBOL	PARAMETER	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = 1.0 mA V_{IL} = value indicated below on this table
V_{OL}	Output LOW Voltage		0.45		0.3	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 10 mA
V_{IH}	Input HIGH Voltage	2.0		2.0			2.0		Volts	Guaranteed input HIGH threshold for all inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed input LOW threshold for all inputs
I_{FA}	Add. Input Load Current		-0.4			-0.4		-0.4	mA	V_{CC} = 5.25 V; V_F = 0.45 V, V_R =
I_{FE}	Enable Input Load Current		-0.4			-0.4		-0.4	mA	V_{CC} = 5.25 V; 4.5 V on other inputs
I_{RA} & I_{RE}	Input Leakage Current		20			20		20	μA	V_{CC} = 5.25 V, V_R = 4.5 V, Gnd. on other inputs
I_{CC}	Power Supply Current		140		120	140		140	mA	V_{CC} = 5.25 V, all inputs at ground

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

93401 SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C) (See Fig. 2)

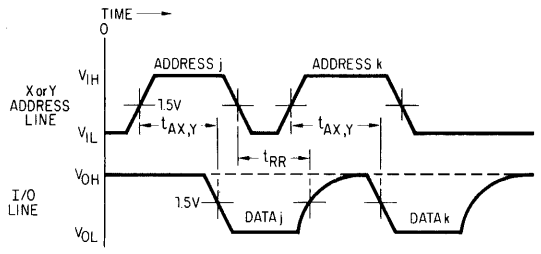
SYMBOL	PARAMETER	LIMITS C_L = 90 pF (Equiv. to 32 X Lines) TYP.	MAX.	C_L = 500 pF (Equiv. to 32 Y Lines) TYP.	MAX.	UNITS
t_A^{++}, t_A^{+-} t_A^{-+}, t_A^{--}	Delay from address going LOW or HIGH to output going LOW or HIGH	20	25	30	40	ns
t_E^{++}, t_E^{+-} t_E^{-+}, t_E^{--}	Delay from enable going active or inactive to output going HIGH or LOW	20	25	30	40	ns

93400 • 93400B SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C.) C_L = 47 pF; Equivalent to eight OR–tied 4100 outputs

SYMBOL	PARAMETER	93400 LIMITS			93400B LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{AX}	Read Access Time. Time from good X address to good data at output	30	70	100	30	100	200	ns
t_{AY}	Read Access Time. Time from good Y address to good data at output	15	45	65		45	100	ns
t_{RR}	Read Recovery Time. Time for output to go HIGH after removal of address.			100			150	ns
t_{WP}	Write Pulse Width. Width of pulse on WE required to write data into memory.	80			100			ns
t_{SH}	Data Setup Time. Time HIGH or LOW data must be present before end of write pulse to write proper data into memory.			t_{WP}+10			100	ns
t_{SL}				70 (Note 2)			70 (Note 3)	ns
t_{RH}	Data Release Time. This is the minimum set-up time. Removal of data after the release time will not affect the data written into the memory. See note 1.	0			0			ns
t_{RL}		10			10			ns
C_O	Output Capacitance		7.0			7.0		pF
C_{AX}	Input Capacitance for X address line		3.0			3.0		pF
C_{AY}	Input Capacitance for Y address line		15			15		pF
t_{AS}	Address Set Up Time. Time address must be good before end of write pulse during write operation. (See Fig. 3b)	80			80			ns
t_{AP}	Address Pulse Width. Time that address must remain good for write operation. (See Fig. 3b)	100			100			ns
t_{WR}	Write Recovery Time. Time in write-read cycle from end of write pulse to valid output data.			120			120	ns

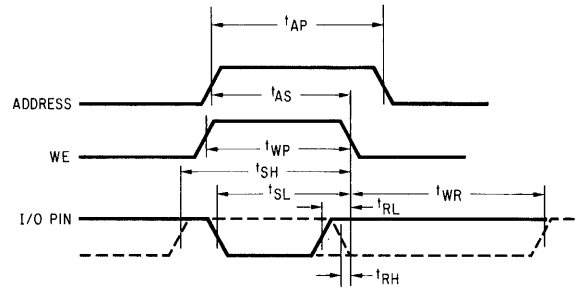
NOTES:
(1) The set up and release times define a window during which devices are responding to the data and/or address. Inputs must remain good at all times in between the set up and release time limits.
(2) Applies for write pulse less than 150 ns.
(3) Applies for write pulse more than 160 ns.

Fig. 1a–93400 TYPICAL READ CYCLE



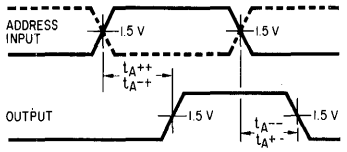
$t_{AX, Y}$ is the time from a good address to good data on the output. Note that the access time may be overlapped with the recovery time to improve speed on consecutive read operations.

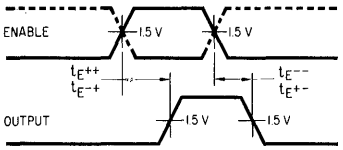
Fig. 1b–93400 WRITE CYCLE



The address must be maintained for 100 ns. The simplest write cycle is achieved by applying the data, then simultaneously raising the address and write pulses for 100 ns. If the write pulse width is less than 100 ns, then the address should come up at about the same time as the write pulse and should be held on after the write pulse. The address should not be applied more than 25 ns before the write pulse, because an early address will cause a read operation to begin disrupting data on the I/O lines (see t_{RR}). For a longer write pulse the address pulse may appear anytime as long as it starts before t_{AS} and lasts at least t_{AP}.

Fig. 2–93401 SWITCHING WAVEFORMS AND TEST LOAD CONDITIONS





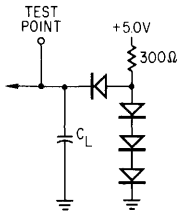
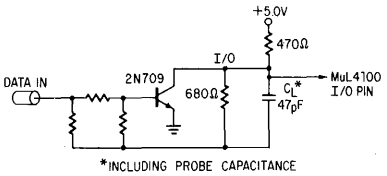


Fig. 3
93400
TEST LOAD CONDITIONS



LOW Level ≤ 0.45 V
HIGH Level ≥ 3.0 V
Rise, Fall Time = 10 ±5 ns

Fig. 4
93400 STANDARD
INPUT PULSE

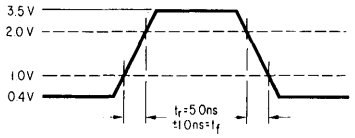
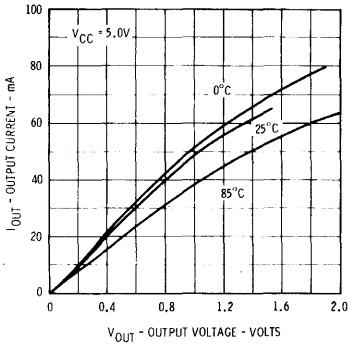


Fig. 5
93400 • 93400B
OUTPUT CHARACTERISTICS



The timing curves in Figures 8 through 13 are obtained using the pulse shape in Figure 6 and the loading in Figure 5. In Figures 12 and 13 the C_L value in the load is varied.

Fig. 6
INPUT THRESHOLD VOLTAGE
VERSUS TEMPERATURE

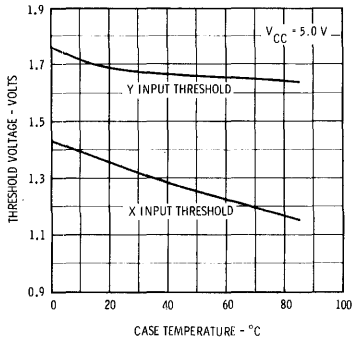


Fig. 7
X ACCESS TIME
VERSUS TEMPERATURE

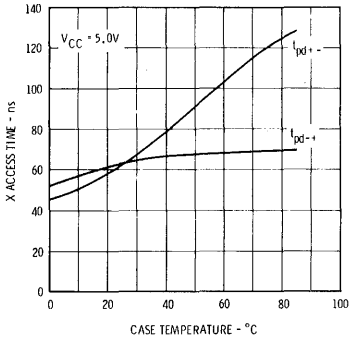


Fig. 8
Y ACCESS TIME
VERSUS TEMPERATURE

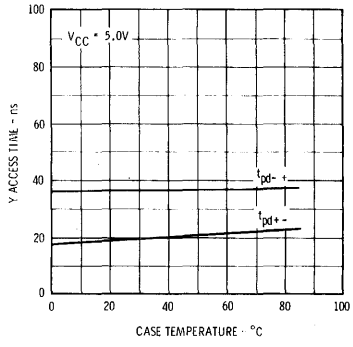


Fig. 9
MINIMUM WRITE PULSE
WIDTH VERSUS TEMPERATURE

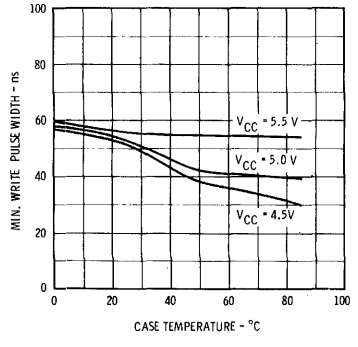


Fig. 10
X ACCESS TIME VERSUS
LOAD CAPACITANCE

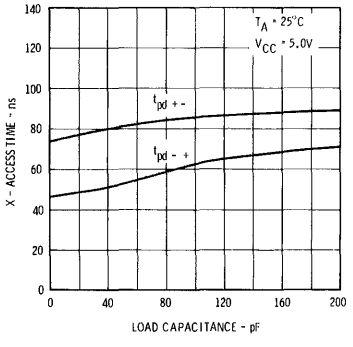
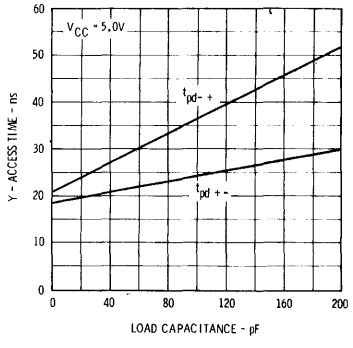


Fig. 11
Y ACCESS TIME VERSUS
LOAD CAPACITANCE



TTL MEMORY 93402

16-BIT ASSOCIATIVE/CONTENT ADDRESSABLE MEMORY

FORMERLY 4102

DESCRIPTION – The 93402 is a high speed 16-Bit Associative Random Access Memory. It is a linear select 4-word by 4-bit array which performs the equality search on all bits in parallel. The 93402 is TTL compatible.

With the bit enable lines ($\overline{E}_0 - \overline{E}_3$) LOW, the outputs ($M_0 - M_3$) go HIGH if associated stored data matches the descriptor bits ($\overline{D}_0 - \overline{D}_3$). If a bit enable line is held HIGH, a match is forced on the corresponding bit in all the words regardless of the state of the descriptor bit ($\overline{D}_0 - \overline{D}_3$). An inverter is connected to the match output M_0 to give its negation $\overline{M}_0$.

A word is addressed by having an active LOW on the appropriate address line ($\overline{A}_0 - \overline{A}_3$). Any number of words may be addressed simultaneously.

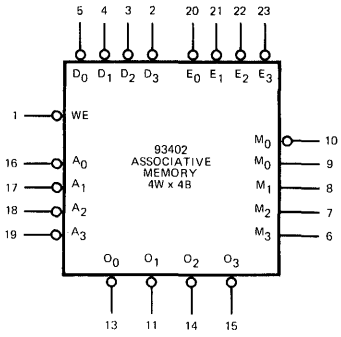
Data can be written into the memory through the data inputs ($\overline{D}_0 - \overline{D}_3$) under control of the address inputs and the appropriate bit enable ($\overline{E}_0 - \overline{E}_3$) when the write enable ($\overline{WE}$) is LOW.

Reading can occur either during an equality search or a write operation. If a single word is addressed that word will appear at the data outputs ($\overline{O}_0 - \overline{O}_3$). If multiple addressing is used, the word appearing at the data output is the AND (positive logic) or the OR (negative logic) of the addressed words.

All outputs are uncommitted collectors allowing maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93402's can be tied together. In other applications, the wired-OR is not used. In either case an external pull up resistor must be used to attain a HIGH at an output.

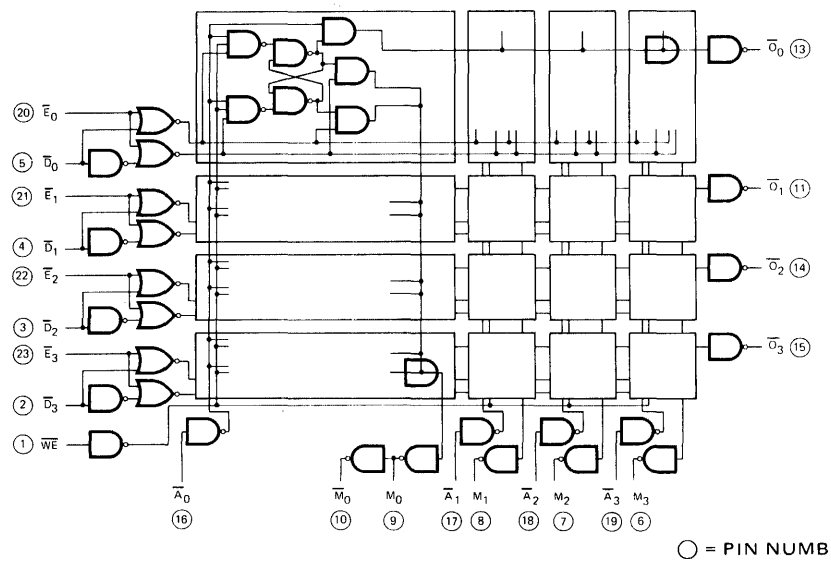
- **25 ns TYPICAL MATCH TIME**
- **MULTIPLE MATCHING AND ADDDRESSING**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR CAPABILITY**
- **LINEAR SELECT ADDRESSING**
- **BIT MASKING**

LOGIC SYMBOL

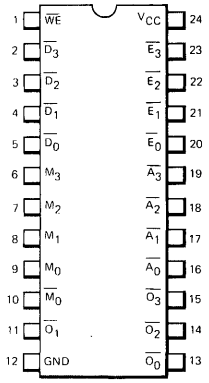


V_{CC} = Pin 24
Gnd = Pin 12

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



LOADING RULES

	HIGH LEVEL (TTL Unit Loads)	LOW LEVEL (TTL Unit Loads)
Address	1.0	1.0
Bit Enable	1.5	1.5
Write Enable	1.5	1.5
Data Input	1.0	1.0
Data Output	Open Collector	6.2
Match Output	Open Collector	6.2

1 Unit Load (U.L.) = 60 μA HIGH/1.6 mA LOW.

The external pull-up resistor R is selected to lie in the range as shown.

$$\frac{5.1}{10 - \text{F.O. } (1.6)} \leq R \leq \frac{2.1}{NL + \text{F.O. } (0.06)}$$

R is in kΩ
N = number of wired-OR outputs
F.O. = number of TTL loads driven
L = Sum of all I_{CEX} of wired-OR outputs

The minimum value of R is limited by output current sinking ability. The maximum value of R is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

F.O.	Maximum number of Wired-OR's
1	66
2	52
3	38
4	24
5	10
5.7	0

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +7.0 V
Input Pin Voltage	−0.5 V to +5.5 V
Current into Output Terminal	50 mA
Output Voltage	−0.5 V to +8.0 V

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested) (Part No. 93402XC)*

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FB}	Bit Enable Load Current		−2.4		−2.4		−2.4	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V
I_{FWE}	Write Enable Load Current		−2.4		−2.4		−2.4	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FI}	Data Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RBE}	Bit Enable Input Leakage Current		90		90		90	μA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		90		90		90	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RI}	Data Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current (Note 4)		50		50		50	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25 V
$I_{CEX\ M_0}$	Output Leakage Current for M_0		110		110		110	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25 V
V_{OL}	Output LOW Voltage (Note 5)		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 10 mA One Word Addressed
V_{IL}	Input LOW Voltage (Note 6)		0.85		0.85		0.85	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input HIGH Voltage (Note 6)	2.0		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{CC}	Supply Current		125		125		125	mA	V_{CC} = 5.25 V, Worst Case

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
(4) For all outputs except M_0.
(5) For all outputs.
(6) For all inputs

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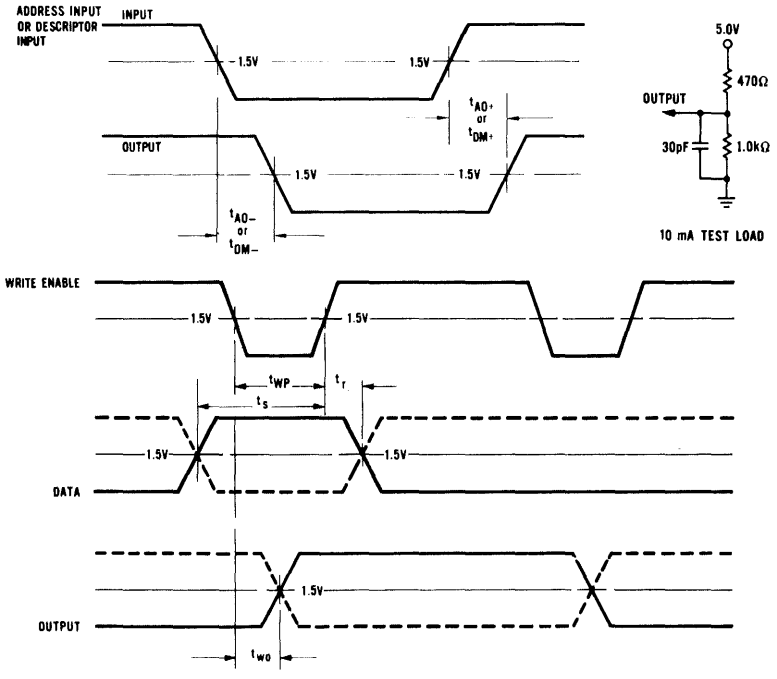
SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

SYMBOL	PARAMETER	LIMIT (ns)		LOAD	CONDITIONS	NOTE
		TYP.	MAX.		C	
t_{AO-}	Address to Output Turn-On Delay	20	30	10 mA	30 pF	1
t_{AO+}	Address to Output Turn-Off Delay	25	35	10 mA	30 pF	1
t_{DM+}	Descriptor to Output Match Turn-On Delay	25	35	10 mA	30 pF	2
t_{DM-}	Descriptor to Output Match Turn-Off Delay	30	40	10 mA	30 pF	2
t_{WP}	Write Pulse Width Required to Write	33	40	10 mA	30 pF	
t_{WO}	Write Delay	50	80	10 mA	30 pF	
t_s	Maximum Set-up Time on Data Input	33	40	10 mA	30 pF	3
t_r	Release Time (Minimum Set-up Time) on Data Input	0	19	10 mA	30 pF	3

NOTES:
(1) To test t_{AO+} and t_{AO-} a LOW must be stored in the cell under test.
(2) To test t_{DM-} and t_{DM+}, a mismatch must occur in at least one bit of the word under test
(3) Setup and release times are measured with respect to the rising edge of the Write enable. To guarantee writing in the correct data, the data input must be good by t_s and remain good until after t_r.

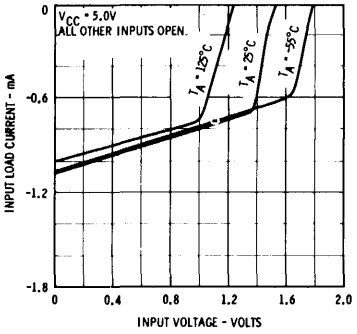
The typical capacitance of one 93402 output is 7.0 pF.

SWITCHING WAVEFORMS

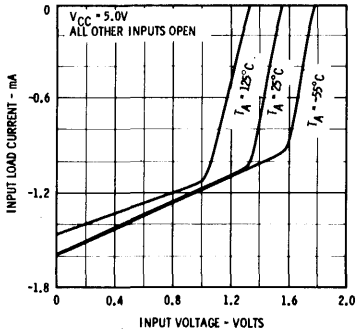


TYPICAL ELECTRICAL CHARACTERISTICS

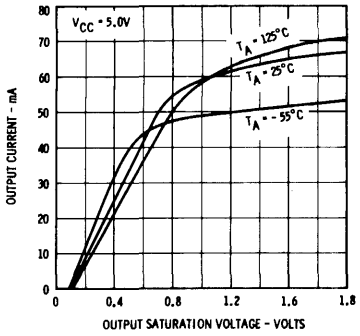
DATA AND ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



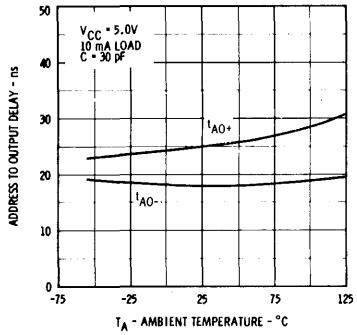
WRITE ENABLE AND BIT ENABLE INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



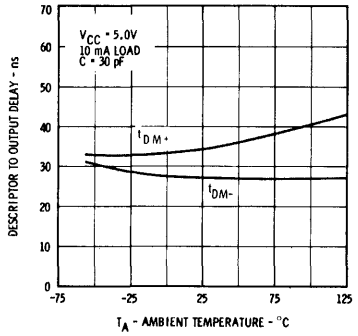
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE ALL OUTPUTS



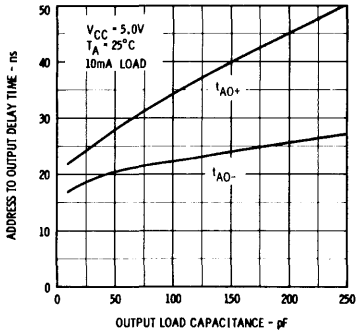
ADDRESS TO OUTPUT DELAY TIME VERSUS AMBIENT TEMPERATURE



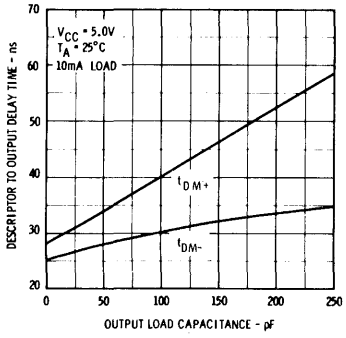
DESCRIPTOR TO OUTPUT DELAY TIME VERSUS AMBIENT TEMPERATURE



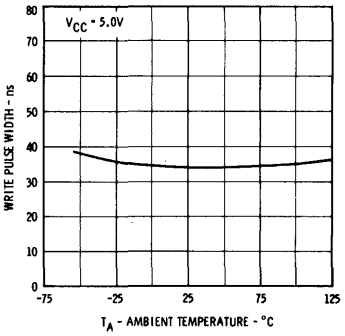
ADDRESS TO OUTPUT DELAY TIME VERSUS LOAD CAPACITANCE



DESCRIPTOR TO OUTPUT DELAY TIME VERSUS LOAD CAPACITANCE



WORST CASE WRITE PULSE WIDTH VERSUS AMBIENT TEMPERATURE



9

TTL MEMORY 93403

64-BIT FULLY DECODED READ/WRITE MEMORY

FORMERLY 4103

DESCRIPTION – The 93403 is a high speed 64-Bit Read/Write Memory organized 16 words by four bits. Four address lines are buffered and decoded "on chip" for word selection. The 93403 is made with TTL circuitry and all inputs are equivalent to one TTL load.

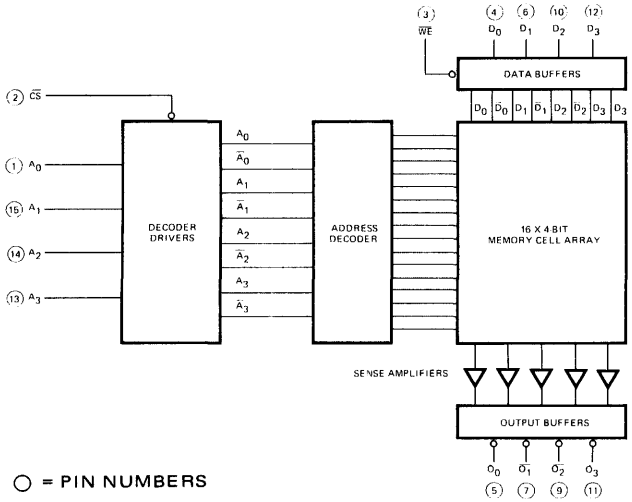
OPERATION – When the 93403 receives a LOW at the Chip Select ($\overline{CS}$) input, the binary address (A_0, A_1, A_2 and A_3) is decoded to select one of sixteen 4-bit words. If the Write Enable ($\overline{WE}$) is at a HIGH level, the contents of the selected word are non-destructively read out and the sense amplifier outputs ($\overline{O_0}$, $\overline{O_1}$, $\overline{O_2}$ and $\overline{O_3}$) reflect the state of the stored data in the four bits of the selected word. If the Write Enable is LOW, the data present on the Data Input lines (D_0, D_1, D_2 and D_3) is written into the four bits of the selected word. Note that there is inversion through the device in a read operation.

- **OUTPUT WIRED-OR CAPABILITY**
- **ON CHIP DECODING**
- **NON-DESTRUCTIVE READOUT**
- **CHIP SELECT FOR SYSTEM WORD EXPANSION**
- **TTL COMPATIBLE**

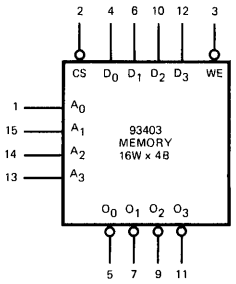
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to + 150°C
Temperature (Case) Under Bias	-55°C to + 125°C
V_{CC} Pin Potential to Ground	-0.5 V to + 8.0 V
Input Pin Voltage	-1.5 V to + 5.5 V
Current Into Output Terminal	100 mA
Output Voltage (external circuit dependent)	-0.5 V to + 8.0 V

BLOCK DIAGRAM

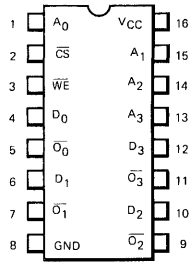


LOGIC SYMBOL

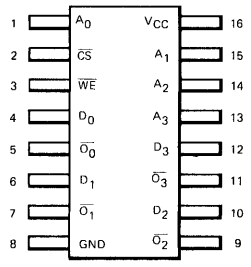


V_{CC} = Pin 16
Gnd = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



ELECTRICAL CHARACTERISTICS (T_{case} = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested) (Part No. 93403XC)

SYMBOL	TEST	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FCS}	Chip Select Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V
I_{FWE}	Write Enable Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FD}	Date Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25V 3.0 on Chip Select
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 16 mA $\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IH}
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{CC}	Supply Current		110		110		110	mA	V_{CC} = 5.25 V, Write Enable = 3.0 V, other inputs Grounded
V_{CD}	Clamp Diode Voltage, All Inputs		-1.0		-1.0		-1.0	V	I_{CD} = -5.0 mA
BV_X	Breakdown Voltage, All Inputs	5.5		5.5		5.5		V	I_X = 1.0 mA

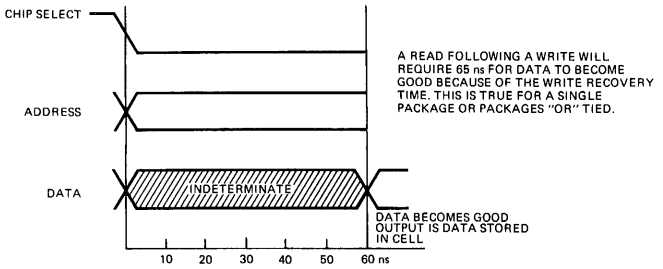
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

SWITCHING CHARACTERISTICS

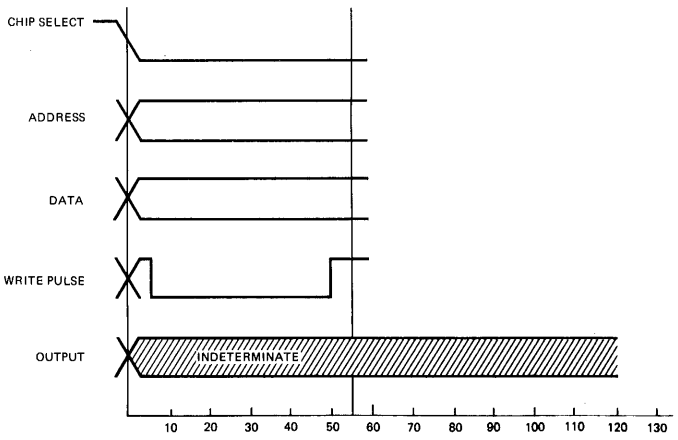
SYMBOL	CHARACTERISTIC	DEFINITION	LIMITS 25°C MIN.	25°C TYP.	25°C MAX.	UNITS
t_A	Read Access Time	Time From Switching Address Or Chip Select To Data At Output		45	60	ns
t_{SR}	Sense Recovery Time	Time From Switching Address Or Chip Select To Output HIGH		45	60	ns
t_{WP}	Write Pulse	Write Pulse Width - Width of Pulse Guaranteed to Write	45	30		ns
t_{WR}	Write Recovery Time	Time From Write Pulse Going HIGH to Output LOW			65	ns
t_{DH}	Data Hold Time	Time From Write Pulse Going HIGH to Change Data Or Address			5.0	ns
t_{DS}	Data Set-Up Time	Time Data Must Be Present Before Write Pulse	5.0	0		ns
t_{AS}	Address Strobe Time	Time Address Must Be Present in Order to Write	5.0	10	45	ns

WAVEFORMS

READ MODE



WRITE MODE



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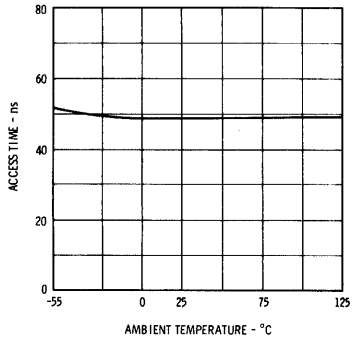
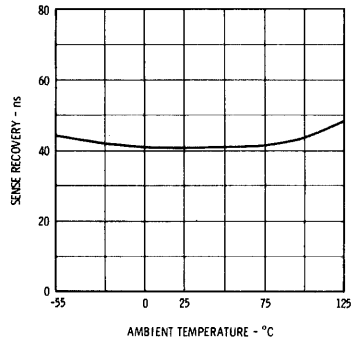
TYPICAL ELECTRICAL CHARACTERISTICS

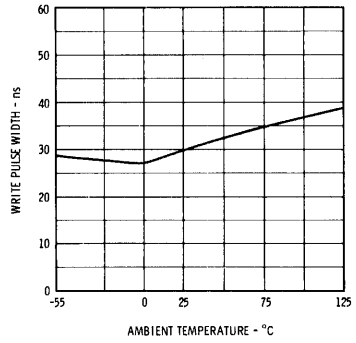
ACCESS TIME (t_A) VERSUS TEMPERATURE



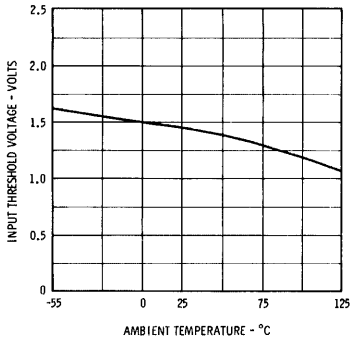
SENSE RECOVERY TIME (t_{SR}) VERSUS TEMPERATURE



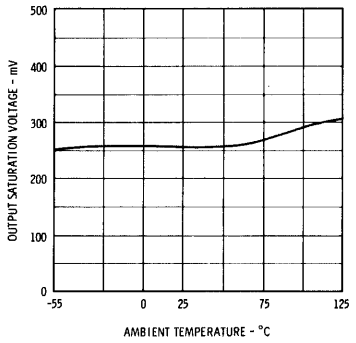
WRITE PULSE WIDTH (t_{WP}) VERSUS TEMPERATURE



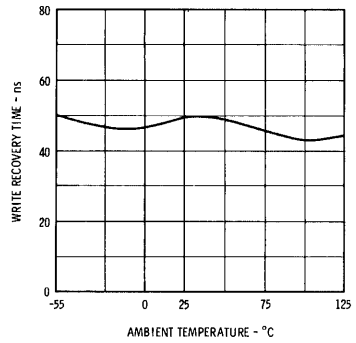
INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



OUTPUT SATURATION VOLTAGE VERSUS TEMPERATURE



WRITE RECOVERY TIME (t_{WR}) VERSUS TEMPERATURE



TTL LOADING RULES

	HIGH LEVEL	LOW LEVEL
Address	1 U. L.	1 U. L.
Chip Select	1 U. L.	1 U. L.
Write Enable	1 U. L.	1 U. L.
Data Input	1 U. L.	1 U. L.
Data Output	Open Collector	10 U. L.

1 LOW Level TTL Unit Load (U.L.) = 1.6 mA
1 HIGH Level TTL Unit Load (U.L.) = 60 μA

Uncommitted collector outputs are provided on the 93403 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93403 can be tied together. In other applications the wired-OR is not used. In either case an external pullup resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{5.05}{16 - \text{F.O.}(1.6)} \leq R_L \leq \frac{2.1}{N(0.1) + \text{F.O.}(0.06)}$$

R_L is in kΩ
N = number of wired-OR outputs
F.O. = number of TTL loads driven
V_{CC} = 5.0 V ±10%

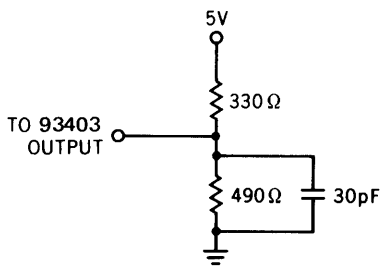
The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

TRUTH TABLE

WE	CS	OUTPUT	MODE
H	H	HIGH No Glitches	Not Read
L	H	Indeterminate Output	Not Write
H	L	Function of Data Stored in Cell	Read
L	L	Indeterminate Output	Write

SWITCHING TEST CIRCUIT

15 mA LOAD



TTL MEMORY 93406
1024-BIT READ ONLY MEMORY

DESCRIPTION – The Fairchild 93406 is a 1024-bit Bipolar Read Only Memory organized 256 words by four bits. An 8-bit binary address is used to select the desired word. The four outputs are uncommitted collectors which permit "OR" tying of the outputs for expanding the memory in the word direction. The customer can specify the active level of the 2-input chip select gate. $\overline{CS}_1$ and $\overline{CS}_2$ both will be active LOW unless otherwise specified by the customer. The programmable enable feature allows expansion of the memory to 1024 words without any external gates.

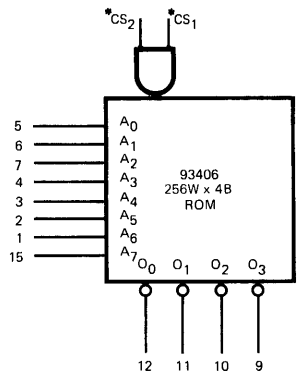
The contents of the memory are mask programmed to the customers specification. The customer can specify the desired ROM code on either the 93406 Coding Form(s) or by punched cards using the 93406 Data Card Format.

- **DTL AND TTL COMPATIBLE**
- **ACCESS TIME – 50 ns MAX**
- **FULLY DECODED – ON CHIP ADDRESS DECODER AND BUFFER**
- **2 CHIP SELECT INPUTS PROVIDING EASY MEMORY EXPANSION**
- **PROGRAMMABLE CHIP SELECTS**
- **OR-TIE CAPABILITY**
- **STANDARD 16-LEAD DUAL IN-LINE PACKAGE**

PIN NAMES

A_0 to A_7	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
$\overline{O}_0$ to $\overline{O}_3$	Data Outputs

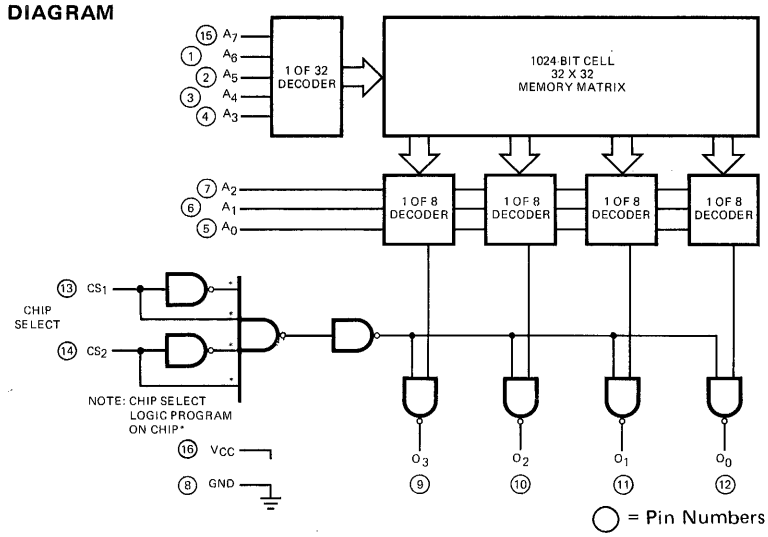
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

*Chip selects active level may be programmed per customer requirements. If not specified both CS will be active low.

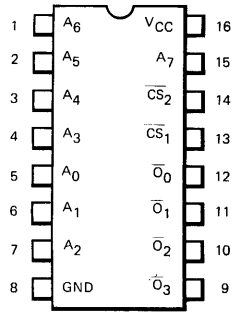
LOGIC DIAGRAM



○ = Pin Numbers

*Per customer request. Unless otherwise specified CS_1 and CS_2 will be active low.

CONNECTION DIAGRAM
DIP (TOP VIEW)



93406 DATA CARD FORMAT

The most efficient method of ordering the 93406 is to punch the desired truth table on a punched card in the format described below. Fairchild will generate mask and test program data directly from these inputs. This eliminates the chance of error when transcribing inputs from a hand written truth table.

Data should be provided on a deck of 34 standard 80 column cards containing the following information.

CARD NO. 1 – Customer Identification

Column	Content
1	Blank
2–28	Customer Name, Drawing or Specification control number.
29–32	Blank
33–39	FAIRCHILD PART NUMBER. This part number is supplied by the factory through your Fairchild sales representative.
40–64	Blank
65–72	Date
73–80	Blank

CARD NO. 2 – Chip Select Option

Column	Content
1–11	Punch "Chip Select"
12	Blank
13, 14	Punch Charts '00', '01', '10' or '11', depending on the chip select code option. (First bit represents CS_1 input, second bit represents CS_2 input. '0' = LOW, '1' = HIGH.)
15–32	Blank
33–39	Repeat FAIRCHILD PART NUMBER (This is used for positive identification).
40–80	Blank

CARDS NO. 3 through 34 – Truth Table Deck

Each card will contain instructions for the output levels for 8 input words.

Column	Content
1–7	Punch the numerals representing the first and last words on that card (i.e.: 000-007, 008-015, 016-023. . .248-255). Word order is determined by the value of the binary address – A_7 = MSB, A_0 = LSB.
8–9	Blank
10–13	Punch the desired combination of "1's" and "0's" representing the output levels for outputs O_3, O_2, O_1 and O_0 (in that order), for the first word on the card, '0' = LOW, '1' = HIGH.
14	Blank
15–18	Punch the desired combination of "1's" and "0's" representing the output levels for the second word on the card.
19	Blank
20–23	Punch the desired combination of "1's" and "0's" representing the output levels for the third word on the card.
24	Blank
25–28	Punch the desired combination of "1's" and "0's" representing the output levels for the fourth word on the card.
29	Blank
30–33	Punch the desired combination of "1's" and "0's" representing the output levels for the fifth word on the card.
34	Blank

CARDS NO. 3 through 34 – Truth Table Deck (cont'd)

Column	Content
35–38	Punch the desired combination of "1's" and "0's" representing the output levels for the sixth word on the card.
39	Blank
40–43	Punch the desired combination of "1's" and "0's" representing the output levels for the seventh word on the card.
44	Blank
45–48	Punch the desired combination of "1's" and "0's" representing the output levels for the eighth word on the card.
49	Blank
50–51	Repeat chip select code option as in columns 13 and 14 of card number 2.
52–59	Blank
60–66	Repeat FAIRCHILD PART NUMBER (this number is used for positive identificaiton).
67	Blank
68–80	Use optional.

93406 Address Scheme

The 93406 is organized 256 words by 4-bits. The words are numbered 0 through 255 and are addressed using sequential addressing of address inputs A_0 through A_7, with A_0 as the least significant digit.

	INPUTS							
WORD	Pin 15	Pin 1	Pin 2	Pin 3	Pin 4	Pin 7	Pin 6	Pin 5
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
WORD 0	0	0	0	0	0	0	0	0
WORD 1	0	0	0	0	0	0	0	1
WORD 2	0	0	0	0	0	0	1	0
WORD 3	0	0	0	0	0	0	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
WORD 255	1	1	1	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to V_{CC} Value

D C ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
I_{CEX}	Output Leakage Current			40	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25V Address any HIGH output
V_{OL}	Output LOW Voltage			0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 15 mA Address any LOW output
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.85	Volts	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current				mA	V_{CC} = 5.25 V, V_F = 0.45 V
	I_{FA} (Address Inputs)			0.8		
	I_{FCS} (Chip Select Inputs)			0.8		
I_R	Input HIGH, Current				μA	V_{CC} = 5.25 V, V_R = 4.5 V
	I_{RA} (Address Inputs)			40		
	I_{RCS} (Chip Select Input)			40		
I_{CC}	Power Supply Current		114	130	mA	V_{CC} = 5.25 V, Outputs open Inputs Grounded and Chip Selected
C_O	Output Capacitance		6.5		pF	V_{CC} = 5.0 V, V_O = 5.0 V, f = 1.0 MHz
V_{CD}	Input Clamp Diode Voltage		−0.8	−1.0	Volts	V_{CC} = 4.75 V, I_A = −5.0 mA

TTL LOADING RULES

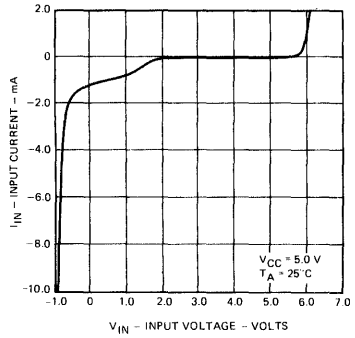
INPUT	LOADING	
	HIGH	LOW
A_7 to A_0	1 U.L.	0.5 U.L.
CS_1, CS_2	1 U.L.	0.5 U.L.

1 U.L. = 40 μA HIGH/1.6 mA LOW

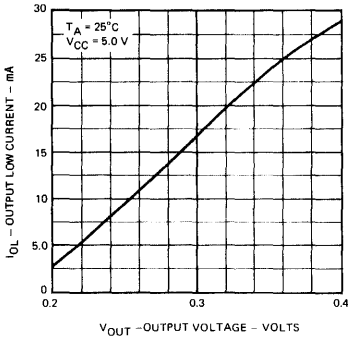
OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
O_0 to O_3	OPEN COLLECTOR	9.3

TYPICAL ELECTRICAL CHARACTERISTICS

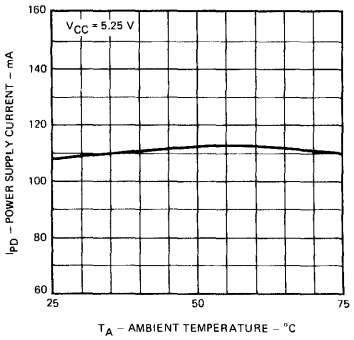
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT LOW CURRENT VERSUS OUTPUT VOLTAGE



POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 0°C to +75°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION
t_{pd++}	Propagation Delay Time, LOW to HIGH Output from Chip Select (or Address) LOW to HIGH		30	50	ns	C_L = 30 pF R_{L1} = 300Ω R_{L2} = 600Ω See Fig. 1
t_{pd+-}	Propagation Delay Time, HIGH to LOW Output from Chip Select (or Address) LOW to HIGH		30	50	ns	
t_{pd-+}	Propagation Delay Time, LOW to HIGH Output from Chip Select (or Address) HIGH to LOW		30	50	ns	
t_{pd--}	Propagation Delay Time, HIGH to LOW Output from Chip Select (or Address) HIGH to LOW		30	50	ns	

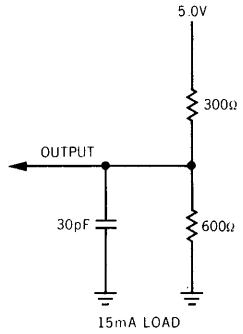
NOTE:
First + or – of t_{pd} indicates change in chip select, or address line. Second + or – indicates change in output.

"+" ≡ Low Voltage to High Voltage

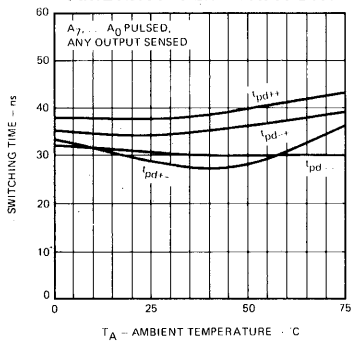
"–" ≡ High Voltage to Low Voltage

NOTES:
(1) To test CS delay, apply input pulse to CS input. The word selected must contain a '0' in the bit under test.
(2) To test t_{pd++} and t_{pd--} delay, apply input pulse to the address input under test. The word selected must contain '0' when the input pulse is LOW, and a '1' when the input pulse is HIGH in the bit under test.
(3) To test t_{pd+-} and t_{pd-+} delay, apply input pulse to the address input under test. The word selected must contain a '1' when the input pulse is LOW, and a '0' when the input pulse is HIGH in the bit under test.

SWITCHING TEST OUTPUT LOAD



SWITCHING TIME VERSUS AMBIENT TEMPERATURE



CHIP SELECT DELAY TIME VERSUS AMBIENT TEMPERATURE (CS_1 TO O_0)

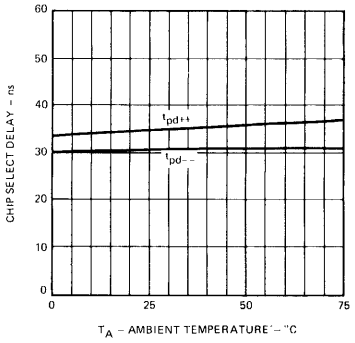
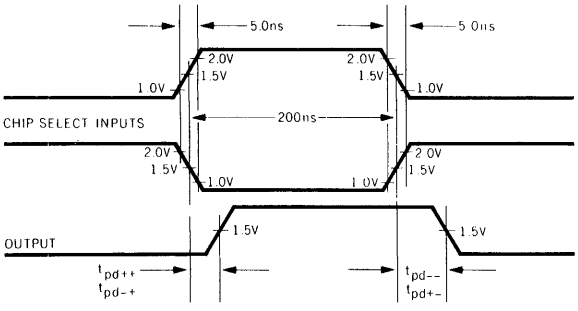
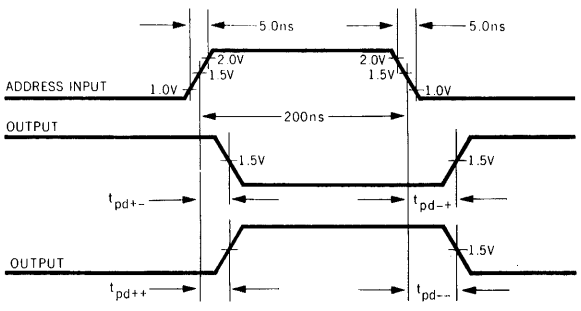


Fig. 1

SWITCHING WAVEFORMS





9

TTL MEMORY 93406

1024-BIT READ ONLY MEMORY

CUSTOMER CODING FORM

CUSTOM ROM TRUTH TABLE

CUSTOMER _____ Location _____

Cust. P/N _____ Cust. Dwg. # _____

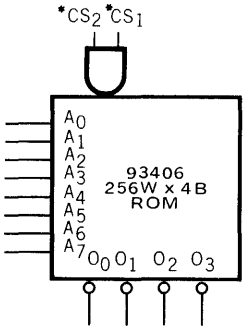
Function _____ SL # _____

Chip Select Code – CS_1 (13) = ___, CS_2 (14) = ___.*

*If not specified, ship select code will be '00'. Package pin numbers are shown in parenthesis.

Input									Output			
MSB								Word	MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0				
0	0	0	0	0	0	0	1	1				
0	0	0	0	0	0	1	0	2				
0	0	0	0	0	0	1	1	3				
0	0	0	0	0	1	0	0	4				
0	0	0	0	0	1	0	1	5				
0	0	0	0	0	1	1	0	6				
0	0	0	0	0	1	1	1	7				
0	0	0	0	1	0	0	0	8				
0	0	0	0	1	0	0	1	9				
0	0	0	0	1	0	1	0	10				
0	0	0	0	1	0	1	1	11				
0	0	0	0	1	1	0	0	12				
0	0	0	0	1	1	0	1	13				
0	0	0	0	1	1	1	0	14				
0	0	0	0	1	1	1	1	15				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

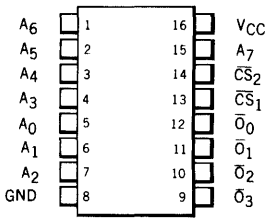
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

*Chip selects active level may be programmed per customer requirements. If not specified both CS will be active low.

CONNECTION DIAGRAM



TTL MEMORY 93406

Input MSB A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Word #	Output MSB O_3	O_2	O_1	O_0
0	0	0	1	0	0	0	0	16				
0	0	0	1	0	0	0	1	17				
0	0	0	1	0	0	1	0	18				
0	0	0	1	0	0	1	1	19				
0	0	0	1	0	1	0	0	20				
0	0	0	1	0	1	0	1	21				
0	0	0	1	0	1	1	0	22				
0	0	0	1	0	1	1	1	23				
0	0	0	1	1	0	0	0	24				
0	0	0	1	1	0	0	1	25				
0	0	0	1	1	0	1	0	26				
0	0	0	1	1	0	1	1	27				
0	0	0	1	1	1	0	0	28				
0	0	0	1	1	1	0	1	29				
0	0	0	1	1	1	1	0	30				
0	0	0	1	1	1	1	1	31				
0	0	1	0	0	0	0	0	32				
0	0	1	0	0	0	0	1	33				
0	0	1	0	0	0	1	0	34				
0	0	1	0	0	0	1	1	35				
0	0	1	0	0	1	0	0	36				
0	0	1	0	0	1	0	1	37				
0	0	1	0	0	1	1	0	38				
0	0	1	0	0	1	1	1	39				
0	0	1	0	1	0	0	0	40				
0	0	1	0	1	0	0	1	41				
0	0	1	0	1	0	1	0	42				
0	0	1	0	1	0	1	1	43				
0	0	1	0	1	1	0	0	44				
0	0	1	0	1	1	0	1	45				
0	0	1	0	1	1	1	0	46				
0	0	1	0	1	1	1	1	47				
0	0	1	1	0	0	0	0	48				
0	0	1	1	0	0	0	1	49				
0	0	1	1	0	0	1	0	50				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

Input MSB A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Word #	Output MSB O_3	O_2	O_1	O_0
0	0	1	1	0	0	1	1	51				
0	0	1	1	0	1	0	0	52				
0	0	1	1	0	1	0	1	53				
0	0	1	1	0	1	1	0	54				
0	0	1	1	0	1	1	1	55				
0	0	1	1	1	0	0	0	56				
0	0	1	1	1	0	0	1	57				
0	0	1	1	1	0	1	0	58				
0	0	1	1	1	0	1	1	59				
0	0	1	1	1	1	0	0	60				
0	0	1	1	1	1	0	1	61				
0	0	1	1	1	1	1	0	62				
0	0	1	1	1	1	1	1	63				
0	1	0	0	0	0	0	0	64				
0	1	0	0	0	0	0	1	65				
0	1	0	0	0	0	1	0	66				
0	1	0	0	0	0	1	1	67				
0	1	0	0	0	1	0	0	68				
0	1	0	0	0	1	0	1	69				
0	1	0	0	0	1	1	0	70				
0	1	0	0	0	1	1	1	71				
0	1	0	0	1	0	0	0	72				
0	1	0	0	1	0	0	1	73				
0	1	0	0	1	0	1	0	74				
0	1	0	0	1	0	1	1	75				
0	1	0	0	1	1	0	0	76				
0	1	0	0	1	1	0	1	77				
0	1	0	0	1	1	1	0	78				
0	1	0	0	1	1	1	1	79				
0	1	0	1	0	0	0	0	80				
0	1	0	1	0	0	0	1	81				
0	1	0	1	0	0	1	0	82				
0	1	0	1	0	0	1	1	83				
0	1	0	1	0	1	0	0	84				
0	1	0	1	0	1	0	1	85				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

TTL MEMORY 93406

Input									Output				Input									Output			
MSB								Word	MSB				MSB								Word	MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
0	1	0	1	0	1	1	0	86					0	1	1	1	1	0	0	1	121				
0	1	0	1	0	1	1	1	87					0	1	1	1	1	0	1	0	122				
0	1	0	1	1	0	0	0	88					0	1	1	1	1	0	1	1	123				
0	1	0	1	1	0	0	1	89					0	1	1	1	1	1	0	0	124				
0	1	0	1	1	0	1	0	90					0	1	1	1	1	1	0	1	125				
0	1	0	1	1	0	1	1	91					0	1	1	1	1	1	1	0	126				
0	1	0	1	1	1	0	0	92					0	1	1	1	1	1	1	1	127				
0	1	0	1	1	1	0	1	93					1	0	0	0	0	0	0	0	128				
0	1	0	1	1	1	1	0	94					1	0	0	0	0	0	0	1	129				
0	1	0	1	1	1	1	1	95					1	0	0	0	0	0	1	0	130				
0	1	1	0	0	0	0	0	96					1	0	0	0	0	0	1	1	131				
0	1	1	0	0	0	0	1	97					1	0	0	0	0	1	0	0	132				
0	1	1	0	0	0	1	0	98					1	0	0	0	0	1	0	1	133				
0	1	1	0	0	0	1	1	99					1	0	0	0	0	1	1	0	134				
0	1	1	0	0	1	0	0	100					1	0	0	0	0	1	1	1	135				
0	1	1	0	0	1	0	1	101					1	0	0	0	1	0	0	0	136				
0	1	1	0	0	1	1	0	102					1	0	0	0	1	0	0	1	137				
0	1	1	0	0	1	1	1	103					1	0	0	0	1	0	1	0	138				
0	1	1	0	1	0	0	0	104					1	0	0	0	1	0	1	1	139				
0	1	1	0	1	0	0	1	105					1	0	0	0	1	1	0	0	140				
0	1	1	0	1	0	1	0	106					1	0	0	0	1	1	0	1	141				
0	1	1	0	1	0	1	1	107					1	0	0	0	1	1	1	0	142				
0	1	1	0	1	1	0	0	108					1	0	0	0	1	1	1	1	143				
0	1	1	0	1	1	0	1	109					1	0	0	1	0	0	0	0	144				
0	1	1	0	1	1	1	0	110					1	0	0	1	0	0	0	1	145				
0	1	1	0	1	1	1	1	111					1	0	0	1	0	0	1	0	146				
0	1	1	1	0	0	0	0	112					1	0	0	1	0	0	1	1	147				
0	1	1	1	0	0	0	1	113					1	0	0	1	0	1	0	0	148				
0	1	1	1	0	0	1	0	114					1	0	0	1	0	1	0	1	149				
0	1	1	1	0	0	1	1	115					1	0	0	1	0	1	1	0	150				
0	1	1	1	0	1	0	0	116					1	0	0	1	0	1	1	1	151				
0	1	1	1	0	1	0	1	117					1	0	0	1	1	0	0	0	152				
0	1	1	1	0	1	1	0	118					1	0	0	1	1	0	0	1	153				
0	1	1	1	0	1	1	1	119					1	0	0	1	1	0	1	0	154				
0	1	1	1	1	0	0	0	120					1	0	0	1	1	0	1	1	155				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12	15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

Input									Output					Input									Output			
MSB								Word	MSB					MSB								Word	MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
1	0	0	1	1	1	0	0	156						1	0	1	1	1	1	1	1	191				
1	0	0	1	1	1	0	1	157						1	1	0	0	0	0	0	0	192				
1	0	0	1	1	1	1	0	158						1	1	0	0	0	0	0	1	193				
1	0	0	1	1	1	1	1	159						1	1	0	0	0	0	1	0	194				
1	0	1	0	0	0	0	0	160						1	1	0	0	0	0	1	1	195				
1	0	1	0	0	0	0	1	161						1	1	0	0	0	1	0	0	196				
1	0	1	0	0	0	1	0	162						1	1	0	0	0	1	0	1	197				
1	0	1	0	0	0	1	1	163						1	1	0	0	0	1	1	0	198				
1	0	1	0	0	0	0	0	164						1	1	0	0	0	1	1	1	199				
1	0	1	0	0	1	0	1	165						1	1	0	0	1	0	0	0	200				
1	0	1	0	0	1	1	0	166						1	1	0	0	1	0	0	1	201				
1	0	1	0	0	1	1	1	167						1	1	0	0	1	0	1	0	202				
1	0	1	0	1	1	0	0	168						1	1	0	0	1	0	1	1	203				
1	0	1	0	1	0	0	1	169						1	1	0	0	1	1	0	0	204				
1	0	1	0	1	0	1	0	170						1	1	0	0	1	1	0	1	205				
1	0	1	0	1	0	1	1	171						1	1	0	0	1	1	1	0	206				
1	0	1	0	1	1	0	0	172						1	1	0	0	1	1	1	1	207				
1	0	1	0	1	1	0	1	173						1	1	0	1	0	0	0	0	208				
1	0	1	0	1	1	1	0	174						1	1	0	1	0	0	0	1	209				
1	0	1	0	1	1	1	1	175						1	1	0	1	0	0	1	0	210				
1	0	1	1	0	0	0	0	176						1	1	0	1	0	0	1	1	211				
1	0	1	1	0	0	0	1	177						1	1	0	1	0	1	0	0	212				
1	0	1	1	0	0	1	0	178						1	1	0	1	0	1	0	1	213				
1	0	1	1	0	0	1	1	179						1	1	0	1	0	1	1	0	214				
1	0	1	1	0	1	0	0	180						1	1	0	1	0	1	1	1	215				
1	0	1	1	0	1	0	1	181						1	1	0	1	1	0	0	0	216				
1	0	1	1	0	1	1	0	182						1	1	0	1	1	0	0	1	217				
1	0	1	1	0	1	1	1	183						1	1	0	1	1	0	1	0	218				
1	0	1	1	1	0	0	0	184						1	1	0	1	1	0	1	1	219				
1	0	1	1	1	0	0	1	185						1	1	0	1	1	1	0	0	220				
1	0	1	1	1	0	1	0	186						1	1	0	1	1	1	0	1	221				
1	0	1	1	1	0	1	1	187						1	1	0	1	1	1	1	0	222				
1	0	1	1	1	1	0	0	188						1	1	0	1	1	1	1	1	223				
1	0	1	1	1	1	0	1	189						1	1	1	0	0	0	0	0	224				
1	0	1	1	1	1	1	0	190						1	1	1	0	0	0	0	1	225				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12		15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

TTL MEMORY 93406

Input									Output			
MSB								Word	MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
1	1	1	0	0	0	1	0	226				
1	1	1	0	0	0	1	1	227				
1	1	1	0	0	1	0	0	228				
1	1	1	0	0	1	0	1	229				
1	1	1	0	0	1	1	0	230				
1	1	1	0	0	1	1	1	231				
1	1	1	0	1	0	0	0	232				
1	1	1	0	1	0	0	1	233				
1	1	1	0	1	0	1	0	234				
1	1	1	0	1	0	1	1	235				
1	1	1	0	1	1	0	0	236				
1	1	1	0	1	1	0	1	237				
1	1	1	0	1	1	1	0	238				
1	1	1	0	1	1	1	1	239				
1	1	1	1	0	0	0	0	240				
1	1	1	1	0	0	0	1	241				
1	1	1	1	0	0	1	0	242				
1	1	1	1	0	0	1	1	243				
1	1	1	1	0	1	0	0	244				
1	1	1	1	0	1	0	1	245				
1	1	1	1	0	1	1	0	246				
1	1	1	1	0	1	1	1	247				
1	1	1	1	1	0	0	0	248				
1	1	1	1	1	0	0	1	249				
1	1	1	1	1	0	1	0	250				
1	1	1	1	1	0	1	1	251				
1	1	1	1	1	1	0	0	252				
1	1	1	1	1	1	0	1	253				
1	1	1	1	1	1	1	0	254				
1	1	1	1	1	1	1	1	255				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

Customers Authorizing Signature _____

Date _____

Qualified FSC Representative _____

Date _____

TTL MEMORY 93407 • 93433

16-BIT COINCIDENT SELECT READ/WRITE MEMORY

FORMERLY 5033 • 9033

DESCRIPTION – These devices are Planar* epitaxial integrated 16-bit, bit-oriented, non-destructive readout memory cells, compatible with Fairchild TTL. These memory cells, organized as 16 words by one bit, are designed for high speed scratch-pad memory applications. The 93407 and 93433 are electrically identical, but with different pin configurations. Both devices are available in two fan out options, 40 mA (A) and 20 mA (B) for Industrial/Commercial temperature range.

OPERATION – The memory cell consists of 16 RS flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "H" level (>2.1 volts) and holding the non-selected address lines at logic "L" level (<0.7 volts). As many as four locations may be addressed simultaneously without destroying stored information. The stored data and its complement at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the $\overline{S_1}$ output will be LOW and the $\overline{S_0}$ output will be HIGH. If the addressed bit location contains a "0", the $\overline{S_1}$ otuput will be HIGH and the $\overline{S_0}$ output will be LOW.

Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a HIGH level. To write a "0", the input of the "write zero" (W_0) amplifier is raised to a HIGH Level.

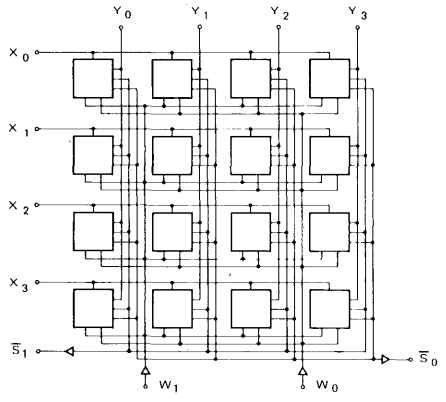
The outputs are open-collector, which may be wired OR for word expansion. (The output transistors are off when none of the bits are selected.) An external resistor should be returned to V_{CC} to pull-up the wired OR outputs.

- **TTL COMPATIBLE**
- **OUTPUT WIRED-OR CAPABILITY**
- **TRUE AND COMPLEMENTARY OUTPUTS ARE PROVIDED**
- **NON DESTRUCTIVE READ OUT**
- **FAN OUT AVAILABLE IN TWO GRADES: A = 40 mA, B = 20 mA FOR INDUSTRIAL/ COMMERCIAL TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to +5.5 V
Current Into Output Terminal	100 mA
Output Voltage	−0.5 V to +8.0 V

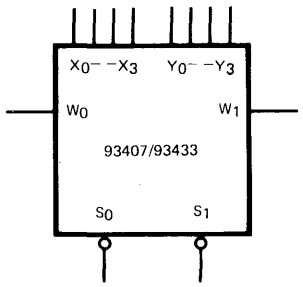
LOGIC DIAGRAM



X,Y – Address
W – Write Input
S – Sense Output

Each square represents one bit of storage.

LOGIC SYMBOL

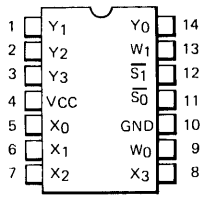


93407
V_{CC} = Pin 4
GND = Pin 10

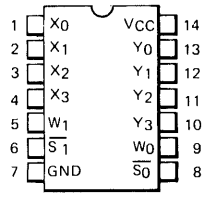
93433
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)*

93407



93433



X, Y – ADDRESS
W – WRITE INPUT
S – SENSE OUTPUT

*Pin connection is same for all packages.

*Planar is a patented Fairchild process.

9

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%) (Part No. 93407/BXM, 93433/BXM)**

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	V_{CC} = 5.5 V, V_X = 0V, V_Y = 4.5 V, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	V_{CC} = 5.5 V, V_Y = 0 V, V_X = 4.5 V, other Y inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	V_{CC} = 5.5 V, V_X = 4.5 V, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	V_{CC} = 5.5 V, V_Y = 4.5 V, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	V_{CC} = 5.5 V, V_W = 0 V
I_{RW}	Write Input Leakage Current		100	μA	V_{CC} = 5.5 V, V_W = 4.5 V
I_{CC}	Power Supply Current		65	mA	V_{CC} = 5.5 V, All Inputs Grounded
I_{BV}	Power Supply Current at V_{CC} = 7 V		84	mA	V_{CC} = 7.0 V, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	V_{CC} = 5.5 V, V_{CEX} = 5.5 V, all inputs grounded
V_{OL}	Output LOW Voltage		0.40	V	V_{CC} = 4.5 V, One Bit Selected I_{OL} = 20 mA
$V_{XY(W)}$	Address Input Threshold to Prevent Writing		0.75	V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{XY(W)}$	Address Input Threshold to Insure Writing	2.1		V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{XY(R)}$	Address Input Threshold to Prevent Reading		0.8	V	V_{CC} = 5.0 V, other inputs grounded. Both outputs must be on HIGH state.
$V_{XY(R)}$	Address Input Threshold to Insure Reading	2.1		V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		0.8	V*	V_{CC} = 5.0 V, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume LOW state. If W_1 is pulsed, S_1 will assume LOW state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.1		V*	V_{CC} = 5.0 V, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume LOW state. If W_1 is pulsed, S_0 will assume LOW state.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (Part No. 93407/AXC, 93407/BXC, 93433/AXC, 93433/BXC)**

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	V_{CC} = 5.25 V, V_X = 0V, V_Y = 4.5 V, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	V_{CC} = 5.25 V, V_Y = 0 V, V_X = 4.5 V, other X inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	V_{CC} = 5.25 V, V_X = 4.5 V, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	V_{CC} = 5.25 V, V_Y = 4.5 V, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	V_{CC} = 5.25 V, V_W = 0 V
I_{RW}	Write Input Leakage Current		100	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{CC}	Power Supply Current		65	mA	V_{CC} = 5.25 V, All Inputs Grounded
I_{BV}	Power Supply Current at V_{CC} = 7 V		95	mA	V_{CC} = 7.0 V, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	V_{CC} = 5.25 V, V_{CEX} = 5.5 V, all inputs grounded
V_{OL}	Output LOW Voltage		0.45	V	V_{CC} = 4.75 V, One bit selected I_{OL} = 20 mA for IND grade. I_{OL} = 40 mA for IND A grade.
$V_{XY(W)}$	Address Input Threshold to Prevent Writing		0.8	V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{XY(W)}$	Address Input Threshold to Insure Writing	2.0		V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{XY(R)}$	Address Input Threshold to Prevent Reading		1.0	V	V_{CC} = 5.0 V, other inputs grounded. Both outputs must be on HIGH state.
$V_{XY(R)}$	Address Input Threshold to Insure Reading	2.0		V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		1.0	V*	V_{CC} = 5.0 V, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume LOW state. If W_1 is pulsed, S_1 will assume LOW state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.0		V*	V_{CC} = 5.0 V, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume LOW state. If W_1 is pulsed, S_0 will assume LOW state.

*Amplitude of the pulse ≥2.5 V, pulse width ≥100 ns. The cell state is determined 35 ns after pulse disappears.

**X = package type; F for Flatpak, D for Ceramic Dip. See Packaging Information Section for packages available on this product.

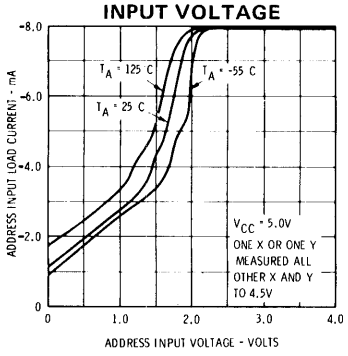
TTL LOADING RULES

	HIGH LEVEL	LOW LEVEL
Address Input	6.5 U.L.	6.5 U.L.
Write Input	1.5 U.L.	0.9 U.L.
Sense Output	Open Collector	IND A grade = 25 U.L. MIL or IND B grade = 12.5 U.L.

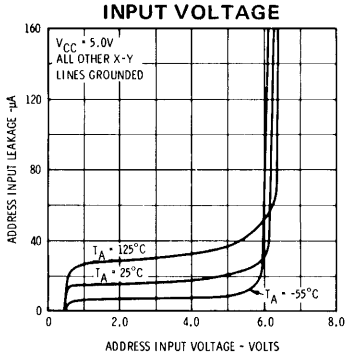
1 Unit Load (U.L.) = 60 μA HIGH/1.6 mA LOW

TYPICAL ELECTRICAL CHARACTERISTICS

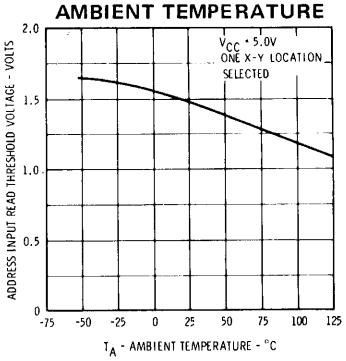
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



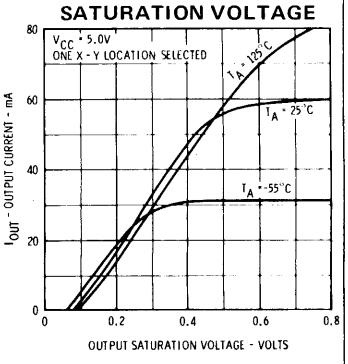
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



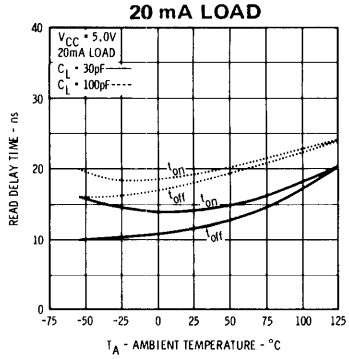
ADDRESS INPUT READ THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



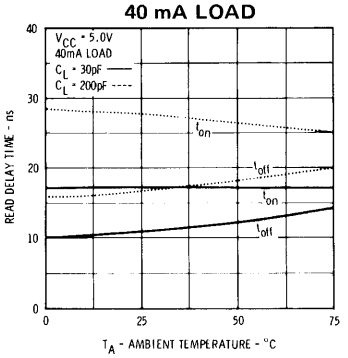
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



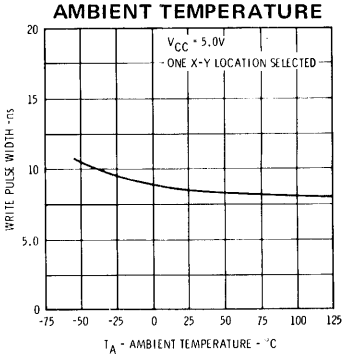
READ DELAY VERSUS AMBIENT TEMPERATURE 20 mA LOAD



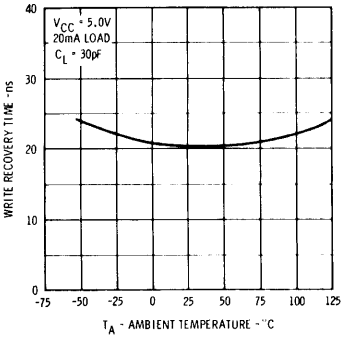
READ DELAY VERSUS AMBIENT TEMPERATURE 40 mA LOAD



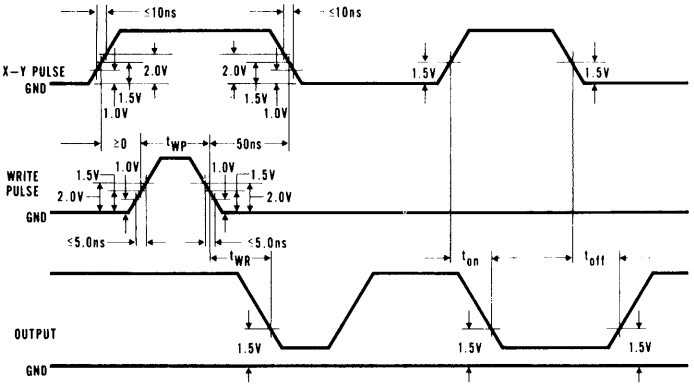
WRITE PULSE WIDTH VERSUS AMBIENT TEMPERATURE

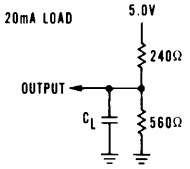


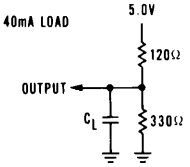
WRITE RECOVERY TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS







SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, One X-Y Location Selected.)

SYMBOL	PARAMETER	MIL B GRADE MIN.	MIL B GRADE MAX.	IND A GRADE MIN.	IND A GRADE MAX.	IND B GRADE MIN.	IND B GRADE MAX.	UNITS	CONDITIONS LOAD (mA)	CONDITIONS C_L (pF)
t_{WP}	Write Pulse Width	25		25		25		ns	40	
									20	
t_{WR}	Write Recovery Time		40		35		35	ns	40	30
									20	30
t_{on}	Turn On Delay		25	20			20	ns	40	30
				30					40	200
			35				30		20	30
									20	100
t_{off}	Turn Off Read Delay		25	20			20	ns	40	30
				30					40	200
			35				30		20	30
									20	100

9

APPLICATION:

A memory utilizing these memory cells may have any desired word length. The number of words in the memory is a multiple of four words. The following example of a 64 word memory illustrates how a number of 16-bit memory cells may be used to construct a typical memory.

The 64 word memory as shown in Figure A consists of groups of four memory cells. Each of the groups of four memory cells supplies one bit for each of the 64 words stored in the memory. All bits belonging to one word are stored in the same address location. Therefore, the address of a word in the memory is the address of each bit of the addressed word in the groups of four memory cells. The equal outputs of the four memory cells are tied together so that each group of four memory cells has one HIGH and one LOW level output.

The six memory address lines from an external source are decoded at the first level with two 9301 decoders. The fourth input to each of the two decoders can be used as an enable control input to the 64 word memory. If the address enable is at a LOW logic level, one and only one of the eight outputs, 0 to 7, in the illustration assumes a LOW logic level. If the address enable is at a HIGH logic level, the outputs 0 to 7 of the two decoders assume a HIGH logic level, thus none of the 64 words stored in the memory is addressed. The outputs, 0 to 7, of the two decoders serve as X-and-Y address lines. The output signals of the decoders are connected to driving transistors which provide the necessary current to address the memory cells.

The example given above is only one of the many organizations and is presented as an illustration. Obviously many address decoding schemes may be utilized depending on memory size, driver fan out, decoder fan out, wiring, heat dissipation, etc.

Figures B through D show alternative schemes to enter data into the memory cell.

64 WORD MEMORY

Fig. A

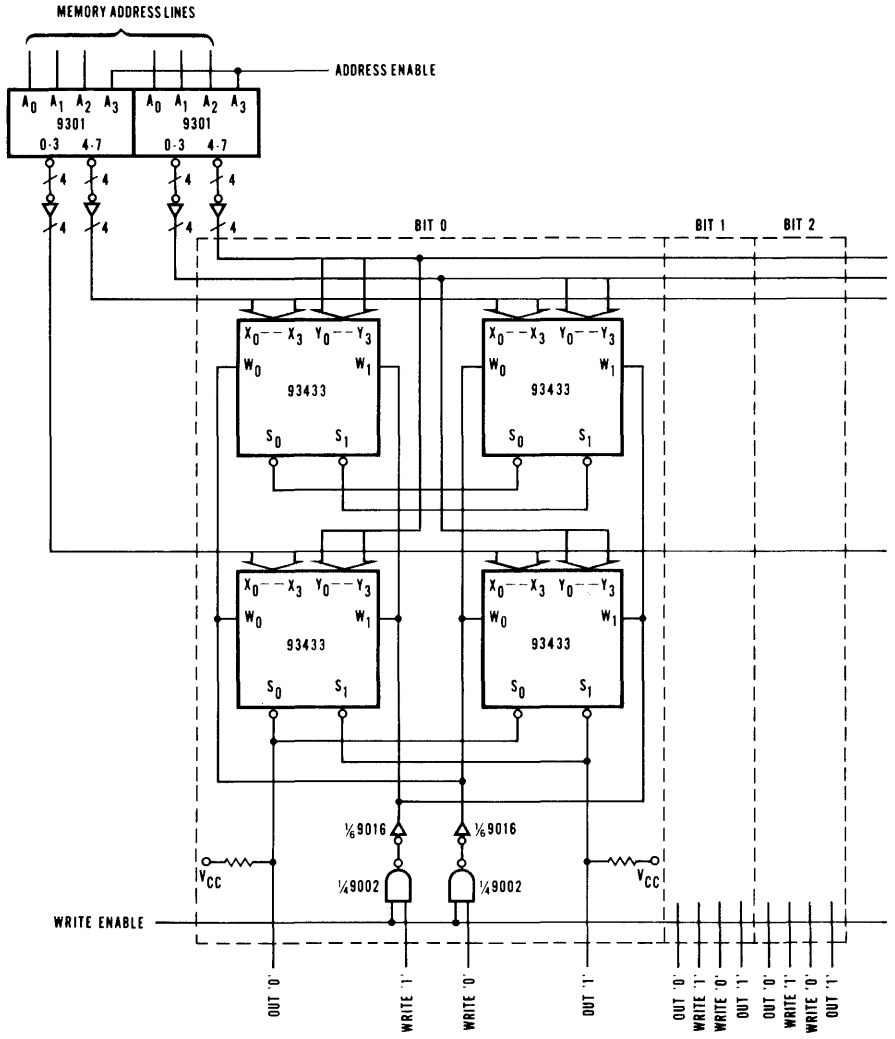


Fig. B
DOUBLE RAIL ACTIVE
LOW INPUTS AND ENABLE

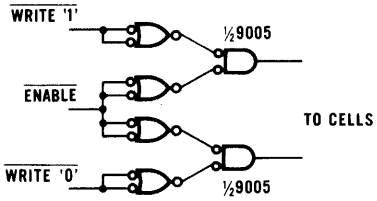


Fig. C
SINGLE RAIL ACTIVE
HIGH INPUT AND ENABLE

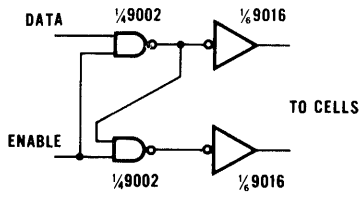
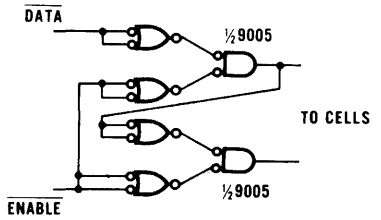


Fig. D
SINGLE RAIL ACTIVE
LOW INPUT AND ENABLE



TTL ISOPLANAR MEMORY 93410 • 93410A

256-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION — The 93410 and 93410A are high speed 256 Bit TTL Random Access Memories with full decoding on chip. Each memory, organized as 256 words x 1 bit, is designed for scratch pad, buffer and distributed main memory applications. Both devices have three chip select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.

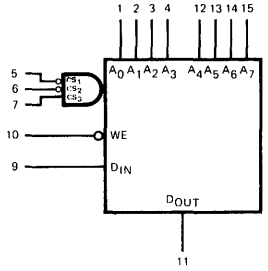
The 93410A is a high speed version of the 93410, offering a 35 ns access time.

- **ORGANIZATION - 256 WORDS X 1 BIT**
- **THREE HIGH SPEED CHIP SELECT INPUTS**
- **TYPICAL ACCESS TIME**

93410A	**Commercial**	**35 ns**
93410	**Commercial**	**45 ns**
93410	**Military**	**45 ns**

- **NON INVERTED DATA OUTPUT**
- **ON CHIP DECODING**
- **POWER DISSIPATION - 1.8 mW/BIT**
- **POWER DISSIPATION DECREASES WITH TEMPERATURE**

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

PIN NAMES

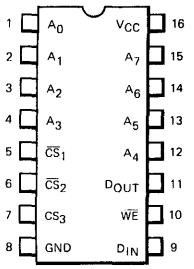
		LOADING (Notes a & b)
$\overline{CS}_1$ $\overline{CS}_2$ CS_3	Chip Select Input	0.5 U.L.
A_0 thru A_7	Address Inputs	0.5 U.L.
D_{IN}	Data Input	0.5 U.L.
D_{OUT}	Data Output	10 U.L.
$\overline{WE}$	Write Enable	0.5 U.L.

NOTES:

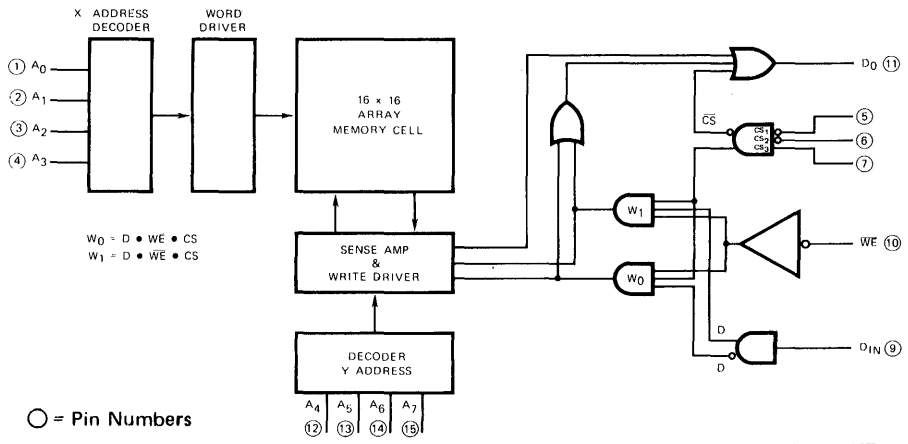
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW

b. 10 U.L. is the output LOW drive factor. An external pull up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at V_{out} = 0.45 V.

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM



9

FUNCTIONAL DESCRIPTION

The 93410 and 93410A are fully decoded 256-bit Random Access Memories organized 256 words by 1 bit. Bit selection is achieved by means of an 8-bit address, A_0 thru A_7.

Three chip select inputs are provided, two are active LOW ($\overline{CS}_1$ and $\overline{CS}_2$) and the third active HIGH (CS_3) for maximum logic flexibility. This permits memory array expansion up to 2048 words without the need for additional external decoders. For larger memories the fast chip select access time permits the decoding of chip select, CS, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable $\overline{WE}$ (pin 10). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93410s or 93410As can be tied together. In other applications the wired-OR is not used. In either case an external pull up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}\,(MAX)}{16 - F.O.\,(1.6)} \leqslant R_L \leqslant \frac{V_{CC}\,(MIN) - V_{OH}}{N\,(I_{CEX}) + F.O.\,(0.04)}$$

R_L is in kΩ
N = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current in mA
V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	MODE
CS			$\overline{WE}$	DI	DO	
PIN 5	PIN 6	PIN 7				
H	X	X	X	X	H	Not Selected
X	H	X	X	X	H	Not Selected
X	X	L	X	X	H	Not Selected
L	L	H	L	L	H	Write "0"
L	L	H	L	H	H	Write "1"
L	L	H	H	X	DO	Read data from addressed location

H = HIGH Voltage
L = LOW Voltage
X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	0.5 V to +5.50 V
Output Current (dc) (Output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE[4]
	MIN.	TYP.	MAX.	
93410XC, 93410AXC	4.75 V	5.0 V	5.25 V	0°C to 75°C
93410XM	4.75 V	5.0 V	5.25 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE[1] (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS[2] MIN.	LIMITS[2] TYP.[3]	LIMITS[2] MAX.	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed input logical HIGH voltage for all inputs	
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed input logical LOW voltage for all inputs	
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX., V_{IN} = 0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX., V_{IN} = 4.5 V	
I_{CEX}	Output Leakage Current			1.0	50	μA	V_{CC} = MAX., V_{OUT} = 4.5 V	
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX., I_{IN} = −10 mA	
I_{CC}	Power Supply Current	93410XC		90	135	mA	$T_A \geq 25°C$	V_{CC} = MAX. All inputs grounded See Power Supply vs Temp. Curve
				100	140		$T_A < 25°C$	
		93410XM		90	135		$T_A \geq 25°C$	
				100	145		$T_A < 25°C$	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

SYMBOL	PARAMETER	93410AXC MIN.	93410AXC TYP.	93410AXC MAX.	93410XC MIN.	93410XC TYP.	93410XC MAX.	93410XM MIN.	93410XM TYP.	93410XM MAX.	UNITS	CONDITIONS
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Access Time		20	24		25	30		25	40	ns	See Test
t_{RCS}	Chip Select Recovery Time		20	25		25	32		25	40	ns	Circuit 5
t_{AA}	Address Access Time		35	45		45	60		45	70	ns	
WRITE MODE	DELAY TIMES											
t_{WS}	Write Disable Time	10	20	35	10	20	40	10	20	50	ns	
t_{WR}	Write Recovery Time		25	35		25	40		25	50	ns	
	INPUT TIMING REQUIREMENTS											
t_W	Minimum Write Pulse Width	30	20		30	25		40	25		ns	
t_{WSD}	Data Set-up Time Prior to Write	5	0		5	0		5	0		ns	
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		ns	See Test
t_{WSA}	Address Set-up Time	5	0		5	0		5	0		ns	Circuit
t_{WSCS}	Chip Select Set-up Time	5	0		5	0		5	0		ns	
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		ns	
C_{IN}	Input Pin Capacitance			4.0			4.0			4.0	pF	Measured with a
C_{OUT}	Output Pin Capacitance			8.0			8.0			8.0	pF	pulse technique

NOTES:

(1) Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.

(2) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(3) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

(4) Guaranteed with transverse airflow exceeding 400 linear F.P.M. and 2 minute warm up.

Typical thermal resistance values of the package are:

θ_{JA} (Junction to Ambient) = 50°C/W (at 400 F.P.M. Airflow)
θ_{JA} (Junction to Ambient) = 90°C/W (Still Air)
θ_{JL} (Junction to Case) = 25°C/W

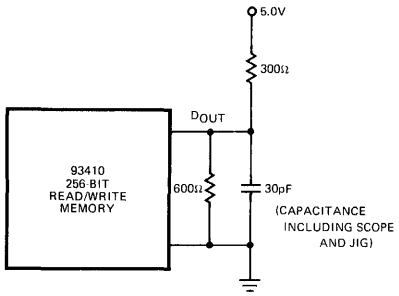
The −55°C Operating Temperature relates to a −30°C worst case cold Junction Temperature.

(5) The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudo random testing pattern.

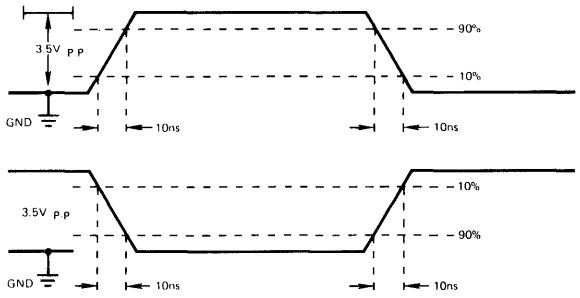
9

93410 AC TEST LOAD AND WAVEFORM

LOADING CONDITION



INPUT PULSES

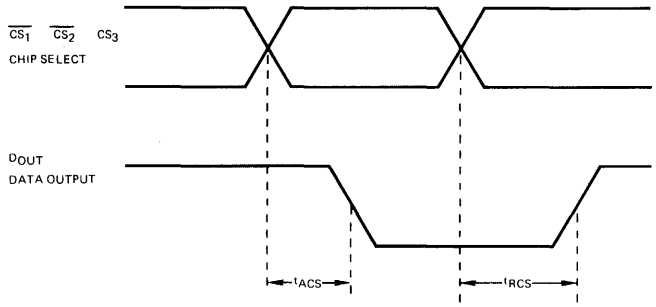


(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

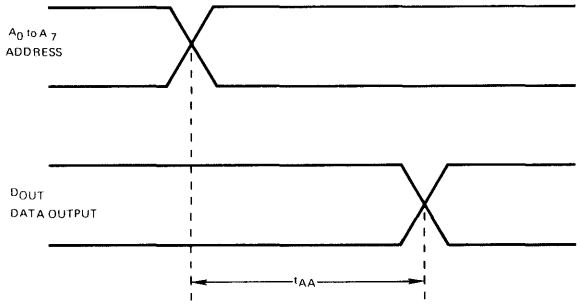
SWITCHING WAVEFORMS

READ MODE

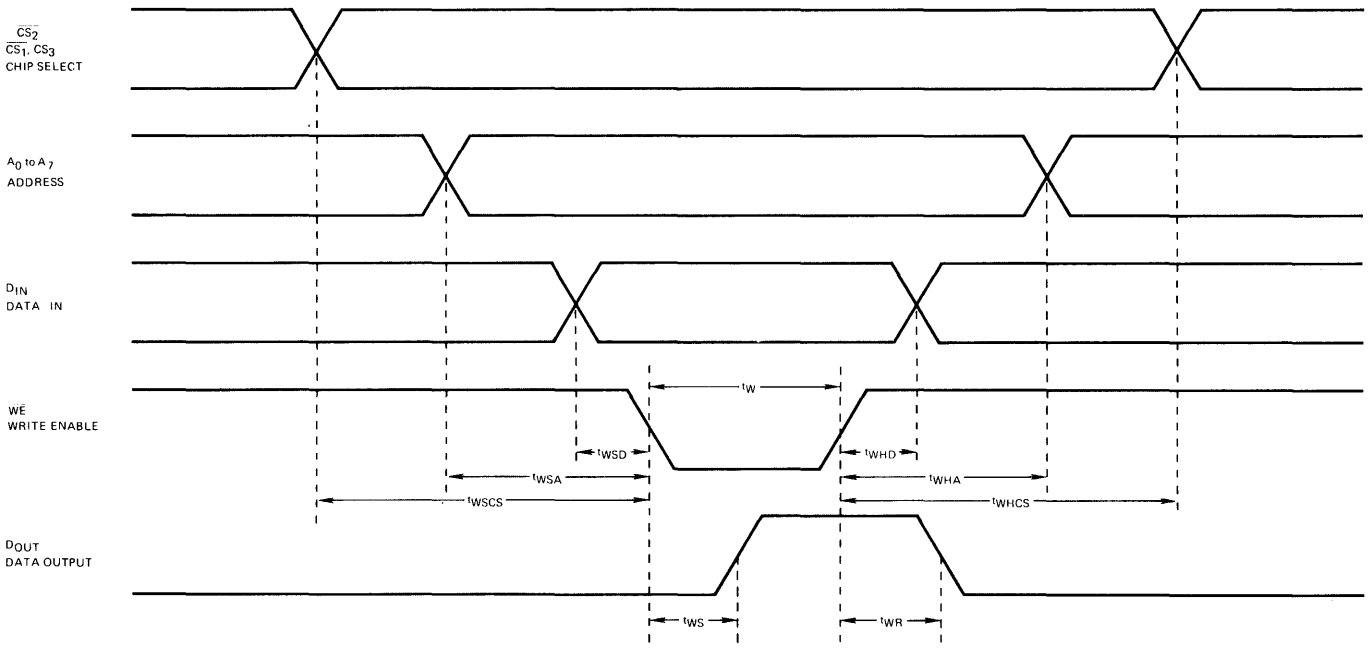
PROPAGATION DELAY FROM CHIP SELECT



PROPAGATION DELAY FROM ADDRESS

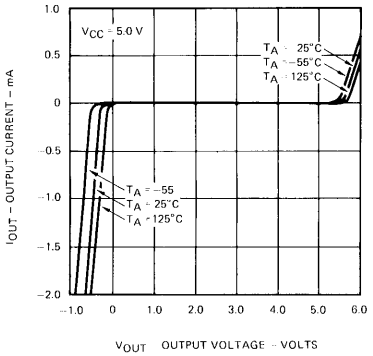


WRITE MODE

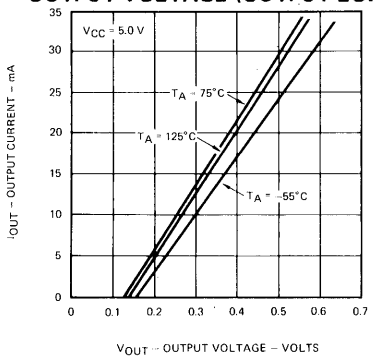


TYPICAL ELECTRICAL CHARACTERISTICS

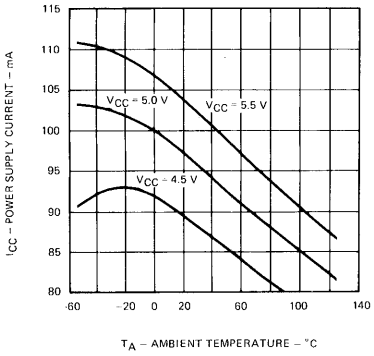
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



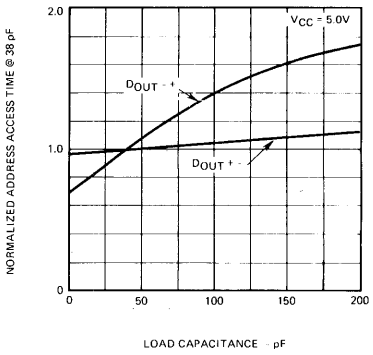
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



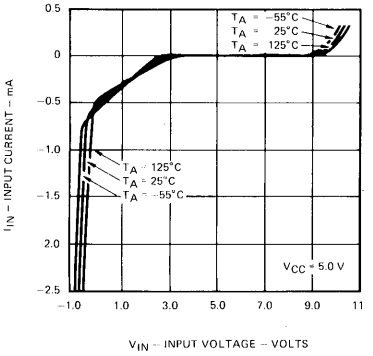
POWER SUPPLY CURRENT VERSUS TEMPERATURE



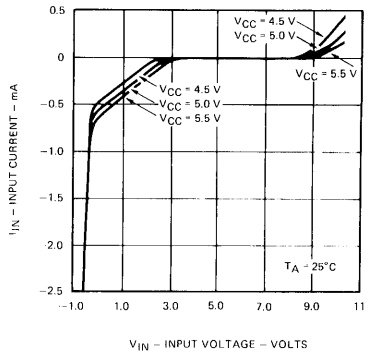
NORMALIZED ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE



9

TTL ISOPLANAR MEMORY 93415

1024-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93415 is a 1024-Bit Read/Write Random Access Memory organized 1024 words x 1-bit. It has a typical access time of 60 ns and is designed for buffer and control storage and high performance main memory applications.

The 93415 includes full decoding on the chip, has separate data input and data output lines and an active LOW chip select line.

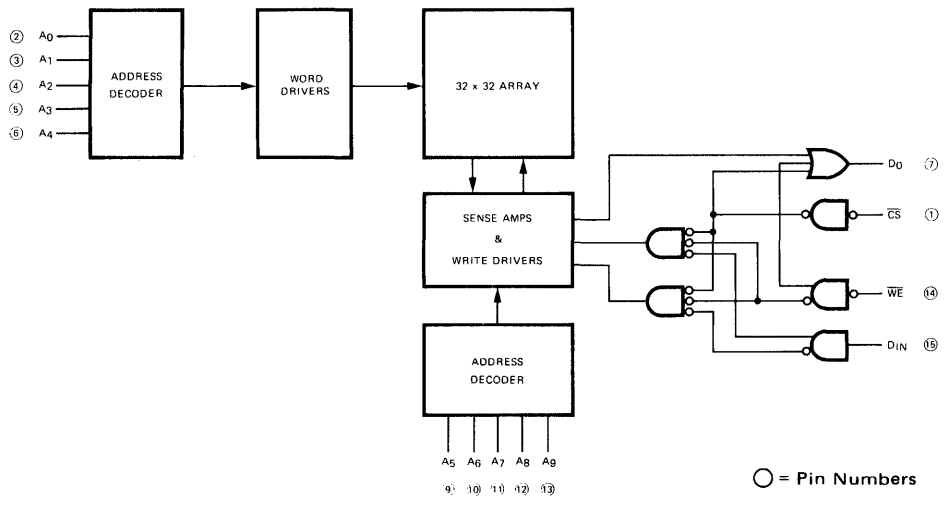
The device is fully compatible with standard DTL and TTL logic families and has an uncommitted collector output for ease of memory expansion.

- **NON-INVERTING DATA OUTPUTS**
- **ORGANIZED 1024 WORDS X 1-BIT**
- **READ ACCESS TIME 60 ns TYP.**
- **CHIP SELECT ACCESS TIME 30 ns TYP.**
- **POWER DISSIPATION 0.5 mW/BIT TYP.**
- **INPUT LOADING 0.25 TTL UNIT LOADS**
- **UNCOMMITTED COLLECTOR OUTPUT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **TTL COMPATIBLE**

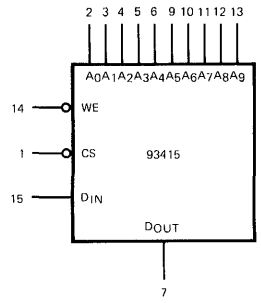
PIN NAMES		LOADING
$\overline{CS}$	Chip Select	0.25 U.L.
A_0 to A_9	Address Inputs	0.25 U.L.
$\overline{WE}$	Write Enable	0.25 U.L.
D_{IN}	Data Input	0.25 U.L.
D_{OUT}	Data Output	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

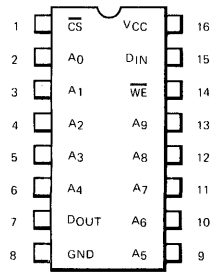


LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by 1-bit. Bit selection is achieved by means of a 10-bit address A_0 to A_9.

One chip select input is provided for memory array expansion with the need for one additional external decoder. For larger memories the fast chip select access time permits the decoding of chip select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable $\overline{WE}$ (pin 14). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

Uncommitted collector outputs are provided on the 93415 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415 can be tied together. In other applications the wired-OR is not used. In either case an external pull up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}\ (min)}{I_{OL} - F.O.\ (1.6)} \leqslant R_L \leqslant \frac{V_{CC}\ (min) - V_{OH}}{N\ (I_{CEX}) + F.O.\ (0.04)}$$

R_L is in kΩ
N = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

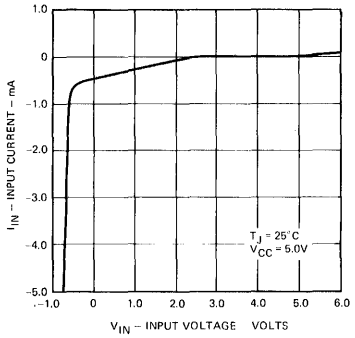
TABLE I – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DI	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_0	READ

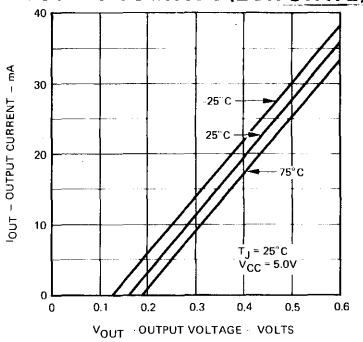
H = HIGH Voltage
L = LOW Voltage
X = Don't Care (HIGH or LOW)

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to + 75°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
*Input Voltage (dc)	−0.5V to +5.5V
*Input Current (dc)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	0.5 V to +4.50V
Output Current (dc) (Output LOW)	+20 mA

*Either input voltage or input current limit is sufficient to protect the input.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN.	TYP.	MAX.	(Note 4)
93415XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

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TO BE ANNOUNCED

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP. (Note 3)	MAX.			
V_{OL}	Output LOW Voltage		0.3	0.45	Volts	V_{CC} = MIN., I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		Volts	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	Volts	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	20	μA	V_{CC} = MAX., V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	50	μA	V_{CC} = MAX., V_{OUT} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	Volts	V_{CC} = MAX., I_{IN} = −10 mA	
I_{CC}	Power Supply Current		90	130	mA	$T_A \geq 25°C$	V_{CC} = MAX.,
			110	150	mA	$T_A < 25°C$	All inputs grounded

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
4. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 fpm air flow)
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JC} (Junction to Case) = 25°C/Watt
   The 100°C Operating Temperature relates to a "worst case" junction temperature of 125°C.
5. The maximum address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.

SWITCHING CHARACTERISTICS – OVER OPERATING TEMPERATURE AND VOLTAGE RANGES

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ MODE	**DELAY TIMES**					
t_{ACS}	Chip Select Access Time		30	55		
t_{RCS}	Chip Select Recovery Time		30	55	ns	See Test Circuit and
t_{AA}	Address Access Time		60	90		Waveforms on page 9-30 (Note 5)
WRITE MODE	**DELAY TIMES**					
t_{WS}	Write Disable Time		35	45	ns	
t_{WR}	Write Recovery Time		45	65		See Test Circuit and Waveforms on page 9-30
	INPUT TIMING REQUIREMENTS					
t_W	Minimum Write Pulse Width		30	55		
t_{WSD}	Data Set-Up Time Prior to Write		0	5		
t_{WHD}	Data Hold Time After Write		0	5		
t_{WSA}	Address Set-Up Time		20	35	ns	
t_{WHA}	Address Hold Time		0	5		
t_{WSCS}	Chip Select Set-Up Time		0	5		
t_{WHCS}	Chip Select Hold Time		0	5		
C_{IN}	Input Pin Capacitance		4	5	pF	
C_{OUT}	Output Pin Capacitance		7	8		

TTL MEMORY 93434

256-BIT READ-ONLY MEMORY

FORMERLY 9034

DESCRIPTION – The Fairchild 93434 is a 256-Bit bipolar TTL Read-Only Memory. The memory is organized as 32 words of eight bits each. The words are selected through five address lines. The eight outputs of the words are uncommitted collectors which may be wired-OR with the outputs of other ROMs. An Enable input is provided for additional decoding flexibility. A HIGH on the Enable input forces all outputs to be HIGH.

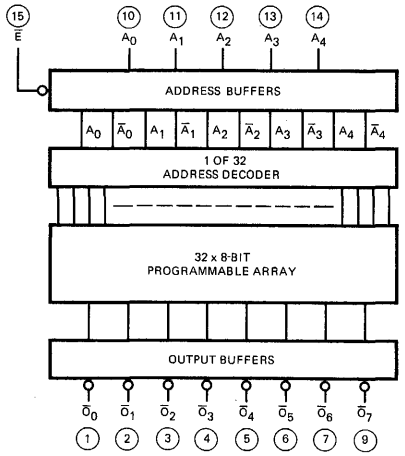
The contents of the memory are permanently programmed to customer order. A customer order form is available on request.

- **TTL COMPATIBLE**
- **OUTPUT WIRED-OR CAPABILITY**
- **SINGLE TTL LOAD INPUTS**
- **INPUT CLAMP DIODES**

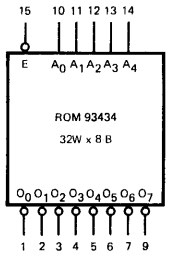
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5V to +8.0V
Input Pin Voltage	−1.5V to 5.5V
Current Into Output Terminal	100 mA
Output Voltages	−0.5 V to V_{CC} Value

LOGIC DIAGRAM

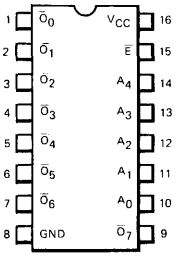


LOGIC SYMBOL

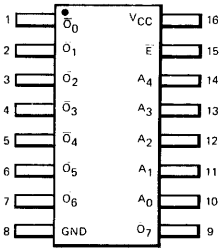


V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



9

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%) (units are pulse tested) (Part No. 93434XM)*

SYMBOL	PARAMETER	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	TEST CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V V_A = 0.4 V
I_{FE}	Enable Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V V_E = 0.4 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.5 V V_A = 4.5 V
I_{RE}	Enable Input Leakage Current		100		100		100	μA	V_{CC} = 5.5 V V_E = 4.5 V
I_{CEX}	Output Leakage Current		200		200		200	μA	V_{CC} = 5.5 V V_{CEX} = 5.5 V Enable input to 2.0V
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V I_{OUT} = 10 mA The word containing a "0" bit is selected when performing this test.
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	V	V_{CC} = 5.5 V Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	V_{CC} = 4.5 V Enable input grounded. Monitor appropriate output to guarantee this test.
I_{CC}	Power Supply Current		80		80		80	mA	V_{CC} = 5.5 V All inputs grounded

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested) (Part No. 93434XC)*

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	TEST CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V V_A = 0.45 V
I_{FE}	Enable Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V V_E = 0.45 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.25 V V_A = 4.5 V
I_{RE}	Enable Input Leakage Current		100		100		100	μA	V_{CC} = 5.25 V V_E = 4.5 V
I_{CEX}	Output Leakage Current		200		200		200	μA	V_{CC} = 5.25 V V_{CEX} = 5.25 V Enable input to 2.0 V
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V I_{OUT} = 10 mA The word containing a "0" bit is selected when performing this test.
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	V_{CC} = 5.25 V Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	V_{CC} = 4.75 V Enable input grounded. Monitor appropriate output to guarantee this test.
I_{CC}	Power Supply Current		80		80		80	mA	V_{CC} = 5.25 V All inputs grounded

*X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

SWITCHING TIME CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
t_{++}	Enable and Address Delay		*	50	ns	10 mA load. See Note 1.
t_{--}	Enable and Address Delay		*	50	ns	10 mA load. See Note 1.
t_{+-}	Address Delay		*	50	ns	10 mA load. See Note 2.
t_{-+}	Address Delay		*	50	ns	10 mA load. See Note 2.

*See Typical Electrical Characteristics curves.

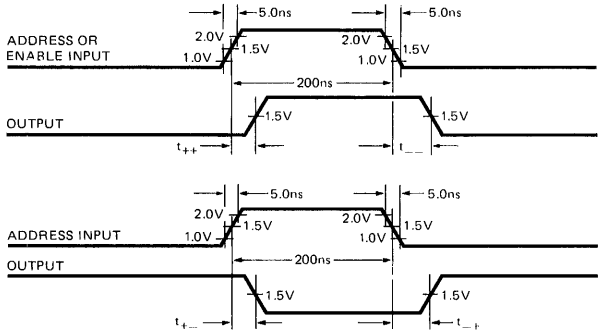
NOTES:

(1) To test Enable delay, apply input pulse to Enable input. The word selected must contain a "0" in the bit under test.

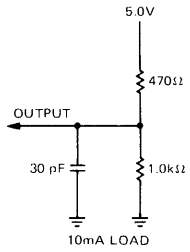
To test Address delay, the enable input must be low. Apply the input pulse to the Address input under test. The words selected must contain a "1" when input pulse is low and a "0" when input pulse is high in the bit under test.

(2) To test Address delay, the Enable input must be low. Apply the input pulse to the Address input under test. The words selected must contain a "0" when input pulse is low and a "1" when input pulse is high in the bit under test.

SWITCHING TIME TEST CONDITIONS AND WAVEFORMS



SWITCHING TEST OUTPUT LOAD



LOADING RULES

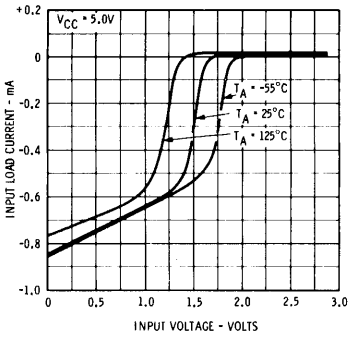
TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOADING	OUTPUTS	DRIVE FACTOR
LOW Level HIGH Level	1.7 U.L. 1.0 U.L.	All outputs	$\frac{\text{Open Collector}}{6.25}$ U.L.

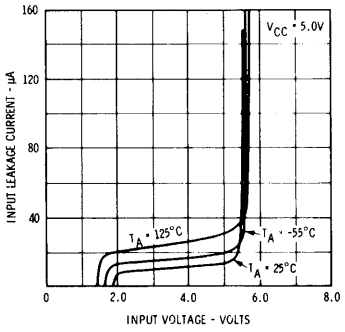
1 LOW Level TTL Unit Load (U.L.) = 1.6 mA
1 HIGH Level TTL Unit Load (U.L.) = 60 μA

TYPICAL ELECTRICAL CHARACTERISTICS

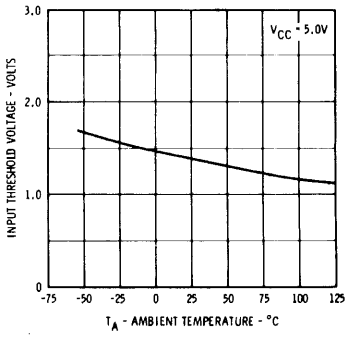
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



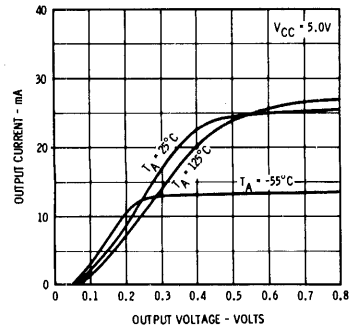
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



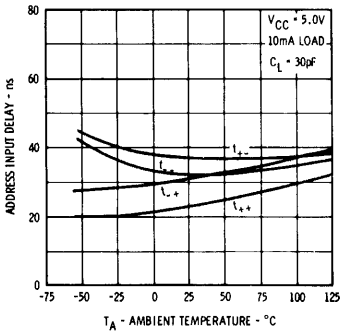
INPUT THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



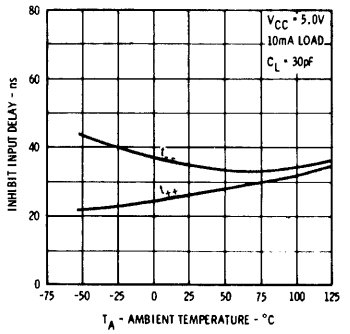
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



ADDRESS INPUT DELAY VERSUS AMBIENT TEMPERATURE



ENABLE INPUT DELAY VERSUS AMBIENT TEMPERATURE



9

TTL MEMORY 93435

64-BIT LINEAR SELECT READ/WRITE MEMORY

FORMERLY 9035

DESCRIPTION – The 93435 is a high speed 64-Bit Read/Write Memory Cell designed for use in high speed scratch pad memories. It is a linear select 16 word by 4-bit array.

The 93435 is available in the hermetically sealed 36-lead ceramic Dual In-Line package and will operate over the temperature range from –55°C to +125°C.

OPERATION – In addition to 16 address inputs, 4 data outputs, and 4 data inputs, the 93435 has a chip select and a write enable. When the chip select is HIGH, a word may be addressed by a HIGH on one of the address inputs. Data is written into the addressed word location only when the write enable is held LOW. While the address is present, the outputs continuously show the contents of the word selected. Readout is non-destructive.

Up to four words may be addressed and read simultaneously with the OR function of each bit appearing at the outputs. Data can be written into two locations simultaneously.

Uncommitted collector outputs are provided on the 93435 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93435's can be tied together. In other applications the wired-OR is not used. In either case an external pullup resistor of value R must be used to provide a HIGH at the output when it is off. Any value of R within the range specified below may be used.

$$\frac{5.1}{10 - \text{F.O. } (1.6)} \leq R \leq \frac{2.1}{N(0.1) + \text{F.O. } (0.06)}$$

R is in kΩ
N = number of wired-OR outputs
F.O. = number of TTL loads driven

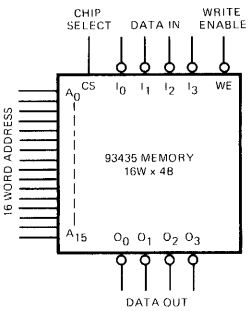
The minimum value of R is limited by output current sinking ability. The maximum value of R is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

- **35 ns MAXIMUM ACCESS TIME – 20 ns TYPICAL**
- **CHIP SELECT AND WRITE ENABLES**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR CAPABILITY**
- **LINEAR SELECT**
- **ON CHIP ADDRESS LINE BUFFERING**
- **TTL COMPATIBLE**

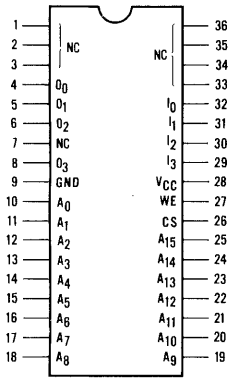
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground	–0.5 V to +7.0 V
Input Pin Voltage	–0.5 V to +5.5 V
Current into Output Terminal	50 mA
Output Voltage	–0.5 V to +8.0 V

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

LOADING RULES

	HIGH LEVEL (TTL Unit Loads)	LOW LEVEL (TTL Unit Loads)
Address	1.67	1
Chip Select	26.7	1 (see note 1)
Write Enable	1.67	1
Data Input	3.34	2
Data Output	Open Collector	6.2

1 LOW Level TTL Unit Load = 1.6 mA
1 HIGH Level TTL Unit Load = 60 μA

ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C, V_{CC} = 5.0 V ±10%) (units are pulse tested) (Part No. 93435XM)*

SYMBOL	PARAMETER	LIMITS -55°C MIN.	LIMITS -55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_A = 0.4 V
I_{FCS}	Chip Select Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_{CS} = 0.4 V See Note 1
I_{FWE}	Write Enable Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_W = 0.4 V
I_{FD}	Data Input Load Current		-3.2		-3.2		-3.2	mA	V_{CC} = 5.5 V, V_D = 0.4 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.5 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.5 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.5 V Write Enable Input Grounded
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 10 mA One Word Addressed
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	Volts	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input HIGH Voltage	2.1		2.0		2.0		Volts	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		118		118		118	mA	V_{CC} = 5.5 V, One Word Addressed

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested) (Part No. 93435XC)*

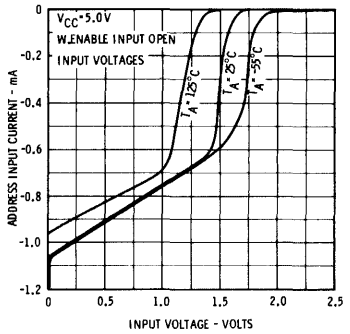
SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FCS}	Chip Select Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V See Note 1
I_{FWE}	Write Enable Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FD}	Data Input Load Current		-3.2		-3.2		-3.2	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25 V Write Enable Input Grounded
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 10 mA One Word Addressed
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	Volts	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		Volts	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		124		124		124	mA	V_{CC} = 5.25 V, One Word Addressed

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

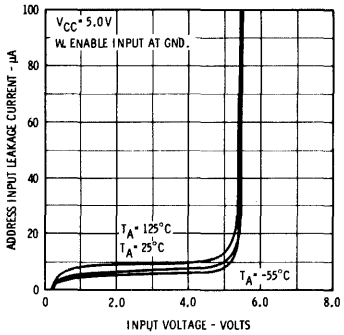
NOTE:
(1) I_{FCS} increases by 1.6 mA for each address input held at a logic 1.

TYPICAL ELECTRICAL CHARACTERISTICS

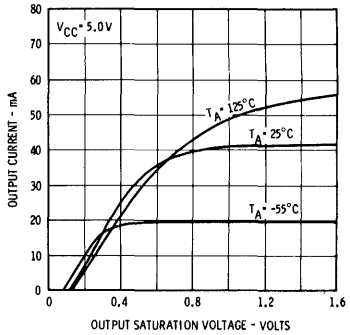
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



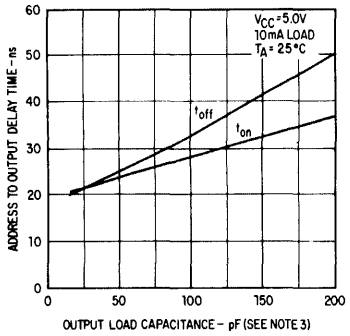
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



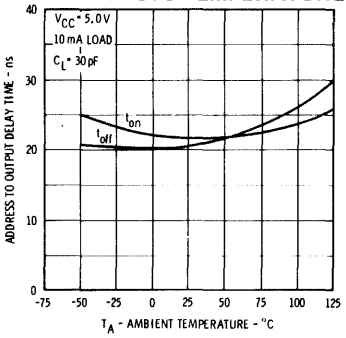
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



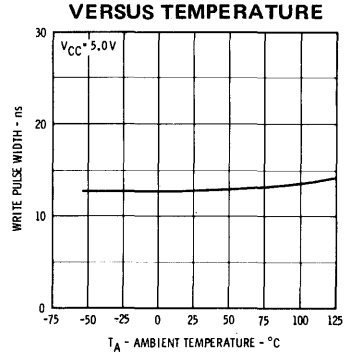
ADDRESS TO OUTPUT DELAY TIME VERSUS OUTPUT LOAD CAPACITANCE



ADDRESS TO OUTPUT DELAY TIME VERSUS TEMPERATURE



WRITE PULSE WIDTH VERSUS TEMPERATURE



SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

SYMBOL	PARAMETER	LIMIT (ns)			CONDITION		
		MIN.	TYP.	MAX.	LOAD	C	NOTE
t_{on}	Address to Output Turn-On Delay	10	22	35	10 mA	30 pF	1
t_{off}	Address to Output Turn-Off Delay	10	20	35	10 mA	30 pF	1
t_{WP}	Write Pulse Width Required to Write	25	15		10 mA	30 pF	2
t_{WD}	Write Delay	10	30	50	10 mA	30 pF	2

NOTES:
(1) To test t_{on} and t_{off}, a LOW must be stored in the cell under test.
(2) One word is selected during the test.
(3) The typical capacitance of one 93435 output is 7.0 pF.