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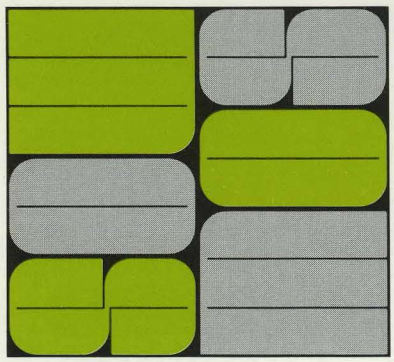

FAIRCHILD OPTIMOS

The promise of MOS/LSI is being fulfilled — inexpensive monolithic circuits can replace entire electronic assemblies today. MOS large scale integration processes can provide a subsystem of several hundred to more than a thousand gates at a cost around $10. Such arrays are now being designed into many more types of digital signal-processing systems than in the past because MOS circuit performance has quadrupled in the past few years.

Nevertheless, MOS/LSI presents risks as well as rewards to the equipment manufacturer. If MOS devices are applicable, all competing equipment manufacturers are virtually compelled to use them. Only the most cost-effective designs, obviously, will be successful. In every instance, since MOS/LSI is a subsystem rather than a component technology, the difference between success and failure will be the ability of the MOS manufacturer to support the cost and design goals of the system planner.

No single approach to MOS/LSI design covers all needs. Striking the right balance among standard MOS products, custom MOS development and bipolar support functions, for example, demands meticulous evaluation of MOS products, design alternatives, and development costs and timing.

This guidebook will examine those planning factors as they relate to MOS/LSI in general and to OPTIMOS in particular. OPTIMOS, a Fairchild acronym for optimum MOS in terms of capability and application is a method of exercising all major MOS cost and design options. It encompasses all Fairchild resources in standard and custom MOS development and production.

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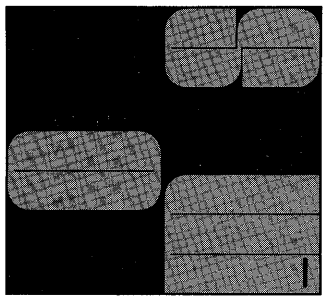
The OPTIMOS process is graphically represented in the form of a flow chart at the back of this manual.

Where MOS Makes Sense Today



The equipment designer's task of choosing between MOS and bipolar circuits used to be relatively simple. MOS/LSI reigned supreme in low power applications while bipolar SSI/MSI (small-to-medium scale integration) was uncontested wherever high circuit speed was essential. As a result of advances in both MOS and bipolar processing, however, the performance attributes attainable through each have moved closer together. In fact, many systems being designed today can tolerate both MOS speeds and bipolar power requirements as well.

So it almost always makes sense to consider MOS/LSI totally or in part, where there is digital signal processing to be performed. Even where medium-to-high circuit speeds are required, the innovative implementation of MOS/LSI with bipolar SSI/MSI may provide a more economical solution than conventional bipolar designs. Now more than ever, the system planner must carefully analyze design alternatives before settling on any single semiconductor process or combination of processes.

MOS/LSI Lowers Digital Signal Processing Costs

In digital processing applications that do not require critically high circuit speeds or drive capability, MOS/LSI more than bipolar SSI/MSI can potentially lower the overall system development cost. Not only is the MOS transistor smaller than the bipolar transistor, but it is self-isolating as well. This combination of smaller transistor area and virtual elimination of isolation area is a major contributor to the cost-savings realizable through MOS because functional density per unit area on a given chip is far greater than that attainable in bipolar MSI/LSI. Moreover, MOS/LSI more readily lends itself to dynamic circuit techniques, and therefore requires fewer components per function.

MOS/LSI should thus be considered for any digital circuit design, unless the speed performance of bipolar logic is essential. Medium speed systems are sometimes produced at unnecessarily high costs with bipolar logic assemblies because the designer did not realize that in large scale arrays, silicon gate MOS/LSI can equal DTL speed.

The overall system design should be studied to determine which portions must work at bipolar speed and drive levels and which can tolerate MOS speed (up to 3 MHz for random logic and up to 8 MHz for structured logic clock rates such as shift registers). Computer peripheral interface logic and storage functions typically operate at or below MOS speed.

There is also the possibility of employing parallel processing to achieve high throughput with relatively low clock rates. This approach can be highly effective because of extremely low cost per gate of MOS/LSI.

The Buck Stops Here

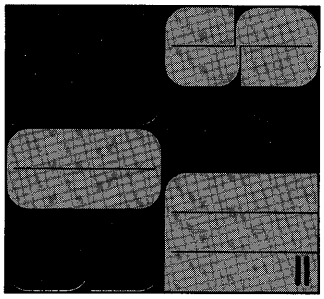
If you are considering your first MOS/LSI system, be prepared to make some hard decisions. To get the best results from the technology may involve some pioneering and some risk.

The conservative approach is not always practical or safe. A small logic system of 300 to 500 gates can be converted to one large scale integrated circuit at a cost of about $10 per circuit in large production quantities. Beyond that, it starts to get sticky because MOS/LSI makes its own rules about large systems and how they should be sliced.

A system partitioned along lines which have grown to be industry standards will no doubt be more economical than the same system assembled with custom packaged logic — assuming MOS is suitable for the system.

While a system that wholly or partially uses standard parts may provide economics over one designed with custom parts, there always exists the possibility that a competitive manufacturer using a totally custom approach may achieve a product of equal or superior performance at a reduced cost.

Furthermore, MOS technology is still in a state of flux. The rules are not fixed. They change from application to application and with each introduction of a new standard circuit, a new set of custom design cells, or an improvement in wafer fabrication processes.



II MOS Economics: An Overview

At one time, MOS circuits were employed in avionics and portable military equipment primarily to achieve small size and low power consumption as well as improved reliability through minimum use of failure-prone component interconnections. The early MOS/LSI circuits were expensive because of poor manufacturing yields.

Now lower manufacturing cost, due to improved yields, is the overriding factor in the phenomenal growth of MOS applications in commercial, industrial, automotive and consumer electronics equipment. User costs have dropped to considerably less than 1¢ per gate in many standard MOS products. In large production quantities, custom MOS circuits can approach standard MOS costs.

Before the prospective MOS user decides how to structure and partition his system — or which process and vendor to use — he should first understand MOS economics. The cost of using MOS typically ranges from purchasing standard products such as a 1024-bit random access memory (RAM) for under $10 for 1000 pieces to $100 for a custom design (including amortized design cost) for the same quantity. The user must decide where in this economic range he will derive the maximum benefit from MOS implementation.

Production Volume Governs Custom Cost

The cost of an MOS custom circuit development is governed primarily by the volume of circuits purchased. In other words, the larger the production run, the smaller the development cost per circuit. Accompanying this cost/volume relationship is the proverbial learning curve. As the production volume increases, the manufacturer becomes more familiar with the circuit. Accordingly, fewer processing errors and higher yields can be expected to further drive down the unit cost.

The potential economics of using custom MOS/LSI versus standard bipolar SSI/MSI can be readily demonstrated through a direct comparison. Consider, for example, a subsystem designed with 300 TTL gates. In assorted MSI and SSI functions, this represents about 30 dual in-line packages. While actual field figures show that the *indirect* cost per bipolar package averages about $2.00, let's make a conservative comparsion and assume this cost to be only $1.00. This indirect per package cost which covers component insertion, PC board, testing and documentation thus totals $30 for the bipolar implemented system. To be even more conservative, let's ignore the unit cost of the bipolar devices and assume the total subsystem cost to be $30.

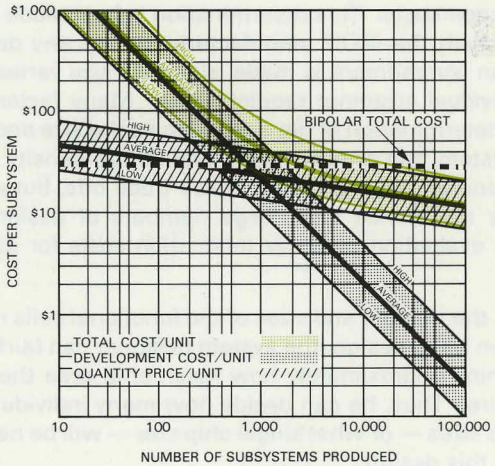
Now if the same subsystem were designed with a single custom MOS circuit, the one-time development charge would be about $20,000 and the unit cost would be about $15 in quantities of 10,000. As shown in *Figure 1,* MOS implementation becomes a more economical approach at a production level that is greater than 2100 subsystems. At the 15,000 subsystem level, a two times advantage is held by MOS. Beneath 2100 subsystems, bipolar MSI/SSI is more economical.

The graph in *Figure 1* also depicts a cost spread on the MOS implementation representing higher and lower complexity levels than the 300 gate example. The one-time

development charges could range from $10,000 to $50,000. This will depend on the design effort required for logic circuit and layout implementation and test pattern generation. The unit cost could vary from $10 to $30 in production quantities of 10,000 depending on the size and complexity of the chip.

The higher cost for smaller quantities of custom MOS subsystems stems chiefly from the need of the MOS manufacturer to amortize custom development and manufacturing start-up costs through either front-end charges to the customer or by a contractual commitment for a large volume of units. In the past, MOS manufacturers were frequently willing to underwrite much of the start-up cost as a means of winning customers. Besides, some of the start-up costs could not be distinquished from the MOS manufacturer's own investments necessary to initiate MOS development and processing.

Since these costs are now well established and the direct result of individual development projects, MOS manufacturers are generally reluctant to undertake a custom development order without a firm commitment regarding payment of costs or a production volume sufficient to amortize the costs. For these reasons, the system manufacturer is advised to make sure before making a decision to go custom that the right custom approach is started — indeed, that a custom approach is more economical for the volume of subsystems required.



The COMPARATIVE COSTS OF A 300-GATE SUBSYSTEM are depicted for both custom MOS/LSI and standard bipolar SSI/MSI approaches. Assuming the total cost of a bipolar implemented subsystem to be $30, the custom MOS/LSI implementation which is assumed to have a one-time development charge of $20,000 becomes more economical as the production volume exceeds 2100 subsystems. In an increasing number of cases, the subsystem functions can be performed with standard MOS/LSI circuits, thereby eliminating custom development cost. For example, Fairchild's Digital Voltmeter Logic (3814) is a standard MOS/LSI device that provides a complex measurement function — and yet costs less than the bipolar equivalent at *all production levels.*

Figure 1. Comparative Costs of a 300-Gate Subsystem

Optimum Die Size Growing Larger

Determining the optimum die size in MOS/LSI requires a parallel effort in system partitioning and in evaluation of production costs. This determination is best made by consultation with the MOS manufacturer before any design or production commitment is made, since die size varies widely with individual customer requirements. Many factors enter into the determination of die size, such as the size and nature of the system, the process used, and circuit density. There are no general rules governing these trade offs, but a manufacturer's experience with large numbers of designs does allow an evaluation of wafer fabrication costs for given die sizes.

Knowing the number and sizes of the functional cells required for a given MOS design, the system designer can fairly rapidly determine approximately how much chip area the design will require. Thus, he can decide how many individual chips of various sizes — or what single chip size — will be needed to fabricate this design.

Consider now the equation for determining die cost:

$$\text{Die Cost} = \frac{\text{Wafer Fabrication Cost}}{(\text{Gross Dice/Wafer})\,(\text{Probe Yield})}$$

The *gross dice/wafer* represents the number of potentially good dice, and is dependent on wafer area and die size. The relationship of die size to the number of potentially good dice garnered from a 2-inch diameter wafer is shown below:

Die Size (Mils)	Gross Dice/ 2" Wafer	Die Size (Mils)	Gross Dice/ 2" Wafer
120 x 120	166	200 x 200	47
140 x 140	115	220 x 220	36
160 x 160	84	240 x 240	28
180 x 180	62		

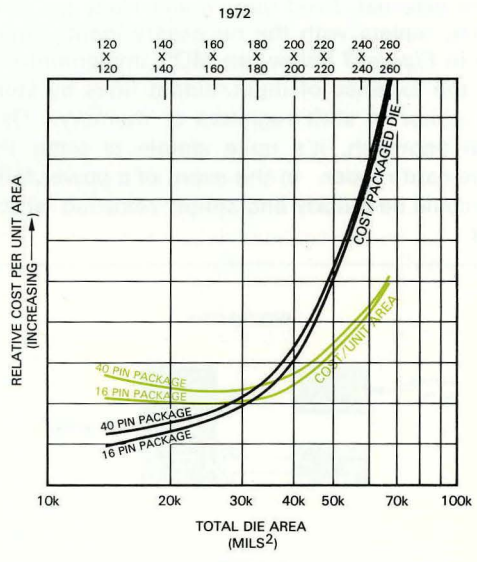
The *probe yield* in the die cost equation is also related to die size as it is the product of two parameters:

- the percentage of semiconductor material that is processed within specifications and independent of die size (typically ranges from 60% to 80%); and
- the defect-limited functional yield that is governed by both the die size and the active area density on the die; this parameter represents the probability that a failure-causing defect will *not* occur on any given die.

Thus as die size increases, the probability that a failure-causing defect will occur on any given die also increases. Accordingly, the probe yield decreases, thereby causing the die cost to increase.

While the die cost equation is helpful in placing the range of die sizes in perspective, it only approximates the cost per function, which, in the final analysis, is the major determinant of optimum die size. *Figure 2a* graphically relates die size to cost per unit of functional area. This analysis concludes that the most functions per dollar would be derived from a die size between 140 x 140 mils and 160 x 160 mils. Of course the curves in *Figure 2a* will change with time; *Figure 2b* projects this change through 1975.

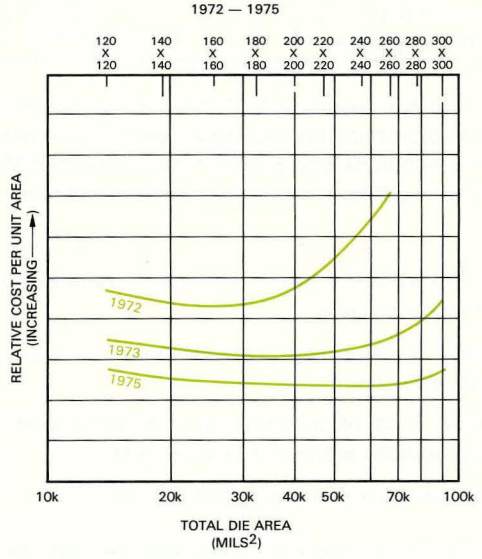
If a subsystem function is too large to fit on an optimum size chip, it may not necessarily be wise to partition the function to operate on two or more smaller chips. Such partitioning



PRESENT OPTIMUM MOS DIE SIZE lies between 140 x 140 mils and 160 x 160 mils.

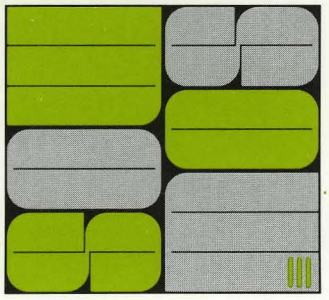
Figure 2a. Present Optimum MOS Die Size

can sometimes complicate the interconnection and logic design or cause performance degradation. Moreover, if the subsystem is to be in production for several years, it is probably wise to choose a die size that is larger than the current optimum range. The optimum die size has been increasing year by year. By 1975, the optimum die size will likely be 240 x 240 mils. The increasing size of an optimum die coupled with increases in MOS circuit density may entirely eliminate the need to partition a subsystem, indeed an entire system, into two or more smaller dice. Accordingly, the MOS cost per function may drop by a factor of 7 by 1975.



PROJECTED OPTIMUM MOS DIE SIZE will shift toward larger areas,reaching 240 x 240 mils by 1975.

Figure 2b. Projected Optimum MOS Die Size



The Critical MOS Decisions

Before tackling the important judgements that must be made when pursuing MOS/LSI implementation, consider the following tabular summary of MOS economic factors.

If This Parameter Increases ↑ / Then This Parameter	Gross Dice/Wafer	Die Size	Probability of Defect	Probe Yield	COSTS: Per Unit	COSTS: Development	COSTS: Per Unit of Functional Area
Production Volume	→	→	→	↑	↓	↓	↓
Complexity	↓	↑	↑	↓	↑	↑	↑
Die Size	↓	↑	↑	↓	↑	↓→	↑→
Number of Functions	↓	↑	↑	↓	↑	↑	↑→
Input/Output Interconnections	↓	↑	↑	↓	↑	↑	↓
Vendor Experience in Manufacturing Dice	↑	↑→	↓	↑	↓	↓	↓

Assuming that the evaluation of the tabular parameters, as they relate to a proposed design of a digital signal processing system, has been done and that it is concluded that MOS/LSI is economically justified, some very critical decision must be made.

- Is the system design optimally structured for MOS implementation?
- What is the proper balance between standard and custom usage?
- What kind of partitioning will avoid performance degradation while minimizing cost?
- Which MOS process is best to use?
- Which semiconductor manufacturer has the appropriate experience and capabilities to support the design and cost objectives?

Let us now consider each of these key decisions in greater detail.

Structuring A System Design For MOS/LSI

To fully exploit the benefits of MOS/LSI, a system should be structured for what MOS/LSI does best, namely, *repetitive logic with few input/output lines.*

Of course, the most common repetitive logic is the memory function. More than any other approach, MOS/LSI can perform the memory function in smaller packages at lower cost. Unlike its magnetic counterpart, for example, MOS memory can be inexpensively distributed throughout the system.

When using MOS/LSI it is possible to reduce system development cost by replacing input/output lines with distributed memory. To illustrate this cost-saving approach, consider a proposed design for a system that would first read variable data from punched cards, then process these data with other external fixed data — and then finally generate output on command. If bipolar circuits were used to implement the system, the external, fixed data would likely be stored in a diode matrix, replete with the necessary input/output lines. As shown in *Figure 3* below, an MOS implemented system can avoid the expense of input/output lines by storing the fixed data either in shift registers or memory. Using this economical approach, it's quite simple to enter the fixed data via the card reader. In the event of a power failure, the fixed data could be quickly and simply reloaded when power is restored.

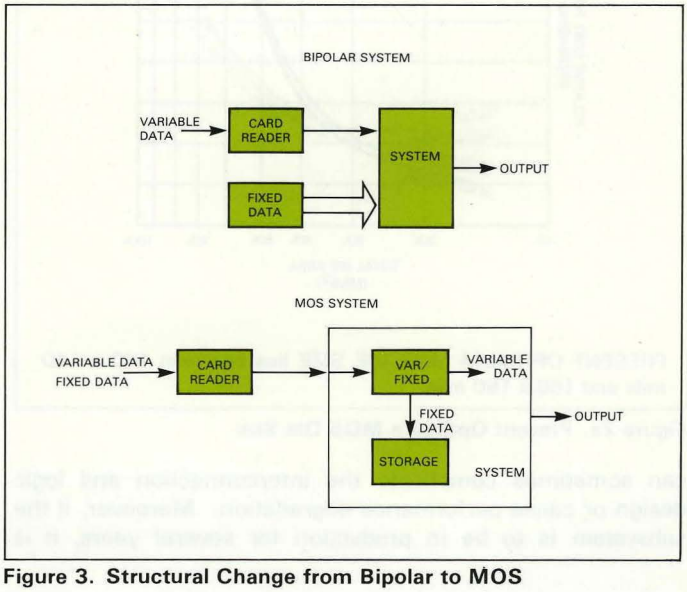


Figure 3. Structural Change from Bipolar to MOS

Another way to reduce the number of input/output lines is through MOS matrix techniques. In an MOS keyboard encoder circuit, for example, only 22 leads are required to determine which of 120 keys are depressed. This is accomplished with a 12 x 10 MOS scanning matrix which can also be used in any system employing switches for external data input.

Multiplexing with MOS/LSI presents yet another method for reducing input/output connections. MOS circuits facilitate the economical use of logic for interleaving both input and output signals on a single input/output line.

The ultimate structure of any proposed system design will greatly depend on the task to be performed. Wherever possible, however, an effort should be made to restructure the proposed design to make maximum use of repetitive logic while reducing the number of input/output lines. This effort will be well worth the cost savings realized.

The Standard Versus Custom Question

Very few system designs should be implemented with all custom or all standard circuits. The optimum approach generally combines both custom and standard circuit functions. In choosing the proper balance between custom and standard usage, the key factors to remember are:

- standard circuits are usually less expensive as their development cost has been amortized through a large production volume for many customers;
- an increasing number of standard, complex MOS circuits are being produced in large enough quantities to make them cost competitive with equivalent implementations in standard bipolar circuits;
- a proprietary total custom approach can provide a significant edge in the marketplace, but not without risks and a substantially large initial investment;
- standard circuits are immediately available while custom circuits have a long lead time, typically six months from the time the system partitioning is finalized; and
- custom circuits should be avoided if it appears that standard circuits will soon emerge to perform the required function.

Leading the list of versatile standard circuits are the memory elements — ROMs, RAMs and Registers. Through microprograming these circuits can be combined with data processing logic to form a dedicated processor for applications in calculators, machine tool control, process control and instrumentation. An increasing number of standard circuits are emerging to perform very complex specialized functions; these include keyboard encoders, calculator and data processing arrays, TV sync generators, DVM logic and data rate buffers. Properly exploited, many of these new generalized standards can replace expensive specialized custom designs. They are now economical to use because the high production volume has not only amortized their development cost, but improved their yields as well. The system planner should always strive to use standard circuits when they will not compromise his competitive market posture.

As pointed out earlier in the MOS Economics section, the high cost of developing proprietary custom circuits stems from low production volume and high engineering content. While the low production volume inherently slows the improvement in yield, the high engineering content represents a substantial commitment of a MOS vendor's resources. This commitment must be matched by the customer in the form of a high initial development cost. In the maturing semiconductor industry, the MOS vendor is having to become increasingly efficient in maximizing the profitable return from his resources. Accordingly, the MOS vendor will engage in custom development contracts only when the customer is prepared to share the potential risks.

Optimum Partitioning: A Moving Target

Partitioning, the task of optimally dividing a system function into sub-functions, must take into account several factors including die size, pin-to-gate ratio and operating speed. Optimum partitioning will generally result through the maximum use of standard building blocks with common designs. On a much finer scale, the goal of partitioning is basically the same as that of structuring the system design, namely low cost. In other words, the goal of partitioning is to divide the system function into sub-functions (i.e., die sizes) that are small enough to provide good yields — yet large enough to minimize the cost per integrated function. Technology is advancing so rapidly that the achievement of this objective compares to hitting a moving target.

The most favorable system partitioning will often require using die sizes that are larger than what is currently considered optimum. From the time partitioning is finalized to the time production commences, it is very likely that the optimum die size will grow larger. Moreover, a larger non-

optimum die size, in spite of its lower yield is often less costly than using two smaller optimum sized dice.

The economic advantages of minimizing the number of input/output lines has already been discussed with regard to structuring the system design. These same advantages should be exploited when performing the partitioning task. In addition to those techniques previously discussed, the designer should consider duplicating local functions (e.g., decode, count, etc.) on each chip and using serial data transfer between chips. While serializing data flow compromises speed, other partitioning techniques can be exploited to mitigate this impact. These include minimizing the number of chips in a critical speed path to reduce speed delays in buffering interconnections as well as using on chip parallelism and bipolar MSI/SSI for those portions requiring high speed performance. Moreover, higher power, higher speed MOS circuit elements could be used in critical paths.

An effective partitioning technique for reducing both engineering and inventory costs is bit slicing where a system is divided into parallel paths. As shown in *Figure 4* below, this technique does not follow a functional division—but rather a division of parallel paths. The bit slice partition reduces the number of different designs and increases the production (hence yield) of a single design.

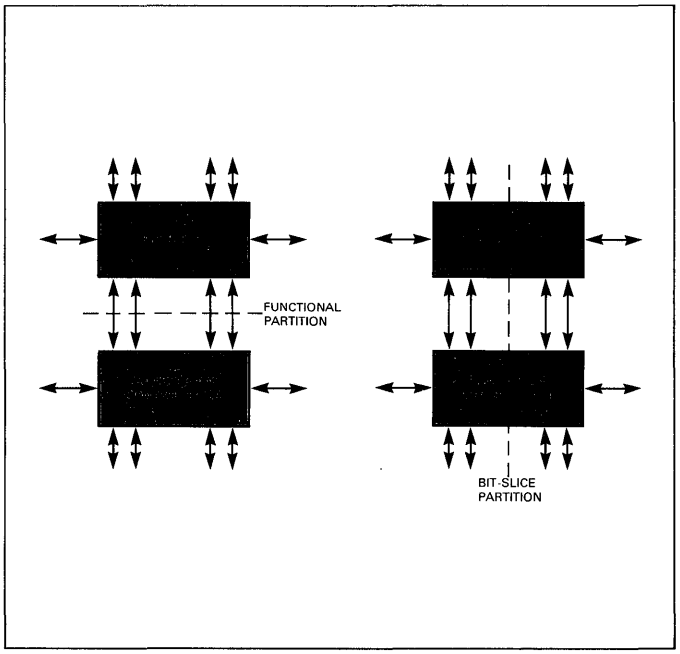


Figure 4. Bit Slice and Functional Partitioning

At first blush, the partitioning task appears to be rather complicated. However, the designer should be comforted by the fact that even a less-than-perfect MOS partitioning job will almost always result in a system cost that is lower than an equivalent bipolar SSI/MSI design. This assumes, of course, that the required production volume justifies the custom MOS approach in the first place.

Proven Processes Better Your Odds

As the prospective MOS user faces an increasingly wider choice of MOS processes, he must take greater care in evaluating the relation of price/performance factors to his design objective. Yesterday's P-channel metal gate MOS/LSI has been virtually eclipsed by P-channel silicon gate MOS/LSI which now boasts a far superior speed power product. However, high-threshold metal gate devices still remain uncontested where high noise immunity is a vital requirement.

Complementary MOS/LSI has emerged as a good choice for applications requiring low power—while N-channel silicon gate MOS/LSI brings the promise of high speed. Although new processes with cost and performance advantages will continually emerge, the prudent designer will stay with a proven process unless his design lead time is long enough to allow a new process to reach production maturity.

Evaluating An MOS Vendor's Capabilities

To properly evaluate an MOS vendor's capabilities, it is first necessary to fully understand the services that are required. The fold-out flow chart on the back page of this book depicts the services required from conceptual design to completed system. It is recommended that this flow chart be folded out and referred to while reading the remainder of this section.

The required services are:

- LOGIC DESIGN — After the system has been partitioned as to what each chip will do in terms of its black box terminal characteristics, it is necessary to select the specific logic functions to be used on the chip itself. These logic functions can either be custom designed for the specific task or selected from a library of pre-designed function cells or a combination of both. Pre-designed cells give three advantages; reduced design time and cost and proven performance.

- LOGIC SIMULATION — To ensure that the logic design performs the desired function, it is necessary to either breadboard the system or use some form of computer logic simulation. The advantage of computer logic simulation is time and cost. Breadboarding in some cases may be an attractive adjunct (but not a replacement) to simulation.

- PERFORMANCE SIMULATION — Once you have a logic design and know that it will perform your function, you should do an analysis of speed performance, determining if this implementation is fast enough on all critical paths. As in the previous step, this can be achieved manually or with a computer program. The advantages of a computer speed simulation are time and cost.

- CHIP LAYOUT (PLACEMENT AND ROUTING) — The custom designed logic functions using predesigned cells must be placed in a location related to their position on the final chip and their interconnections must be routed. This again can be accomplished manually or with a computer program. A combination of both seems to be best as a manual approach takes too long and an all-computer method is not flexible enough. A man interacting with the computer offers an optimum in speed and flexibility.

- MASK MAKING — Each step in the list of services discussed so far permits the customer to perform the task himself if he so desires. However, very few equipment manufacturers have the facilities required to make masks. Here the artwork for chip layout is converted to 1:1 photographic plates that will be used in the actual production of MOS devices.

- TEST GENERATION — The importance of the MOS vendor's capability in test generation cannot be overemphasized. If all input combinations and sequences were tested, a single part could take a century to test. Conversely, a part must be tested thoroughly enough to guarantee its performance. Available computer programs can generate test patterns that select those key tests which most fully check a device within a practical time frame. Often the investment in engineering and computer time required for test pattern generation equals the chip layout investment.

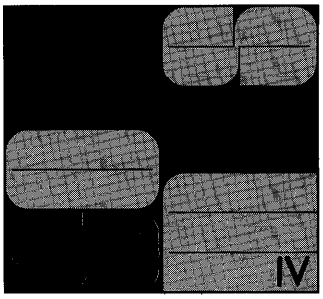
- WAFER FABRICATION — The photomasks are brought together with all other materials to produce a subsystem on a small square or rectangular chip of silicon.

- TESTING — Testing is normally accomplished at both the wafer and packaged unit levels. The good units are selected from the entire population; testing is both parametric and functional. An MOS vendor's capital investment in test equipment should be on a par with that of wafer fabrication.

- ASSEMBLY — The silicon chip is then assembled into a package to provide a form factor for incorporation into the system.

The selection of an MOS vendor should be based on how comprehensively and cost-effectively the above services can be provided. While some *low bids* turn out satisfactorily, many do not as they result in deliveries so late that any savings on parts cost is negated.

Underlying the effective MOS program is a close customer/vendor relationship where the customer requires a reasonably high production volume — and the vendor provides a *proven, total capability.* The most successful MOS programs are based on a business arrangement which mutually commits both the customer and the vendor to share the risks as well as the rewards.



What OPTIMOS Has To Offer

A technology as diverse as MOS/LSI is optimally used only when its diversity is properly exploited. The Fairchild program for the efficient and cost-effective exploitation of MOS/LSI has been named OPTIMOS, an acronym for optimum MOS in terms of capability and application. OPTIMOS lives up to its name by offering prospective MOS users not only two proven MOS processes — silicon gate and metal gate, but also the flexibility to blend custom and/or standard MOS designs with bipolar SSI/MSI. Moreover, reliable packaging is tailored for unique applications.

The wide and expanding selection of standard OPTIMOS circuits offers a broad range of applications. These vary from industry standards like the 3534/1103 1K RAM and the 3514 4K ROM to new areas like the 3814 Digital Voltmeter Logic and the 3261 TV Sync Generator. This manual also includes a full complement of devices which constitute a Programmable Processor System (PPS 25). They are capable of performing in scientific calculators, cash register terminals, process controls, medical instrumentation and virtually all areas that require processor control.

In performing custom design, OPTIMOS derives its efficiency from libraries of predesigned cells for each process (Micromosaic™ Libraries) — and highly developed computer-aided design (CAD) software for design simulation (FAIRSIM) and corresponding test generation (FAIRGEN). The maturity of the OPTIMOS program has been well established, as even first-time MOS designers have been able to rapidly and inexpensively achieve their design objective through custom MOS/LSI.

OPTIMOS allows a completely flexible customer/vendor relationship. The customer is invited to do as much of the logic design and implementation using our standard cells as he chooses, with the commensurate benefits of higher value added and reduced vendor costs. The preliminary design can be performed with or without a computor, on or off the Fairchild premises. Fairchild has even offered to make its software available to customers who have large requirements for custom circuits and a desire to do their own logic and test sequence design.

The fold-out flow chart at the back of the book shows the major design and production steps that are involved in the OPTIMOS program. Within the past three years, Fairchild has generated 40 standard product designs and 200 custom designs. Throughput of the OPTIMOS program now averages eight to ten new designs each month.

OPTIMOS: A Brief History

The OPTIMOS methods used today stem from R & D conducted at Fairchild during the 1960's. Then, as now, the emphasis was on reducing costs, design time, and testing difficulties associated with large scale integration.

As an alternative to the "master slice" techniques popular in the 1960's, Fairchild pursued extremely microminiaturized cellular designs as a means of retaining design flexibility while improving circuit yields. Most MOS manufacturers use this approach today. With process improvements, the technique has become very efficient.

Computer-aided design and testing systems were developed as a parallel effort. These systems have been improved through several years of increasing use and now eliminate most of the laborious, error-prone manual design and testing once required.

Balancing Standard and Custom

Only the customer can define his system and determine the correct mix of standard and custom devices. Our applications engineering staff is available to systems planners, however, for consultation and recommendations on all MOS-associated design problems. The staff should be consulted as early as possible in the planning cycle since early decisions, such as system structuring, involve parallel decisions in product and MOS process selection. Cost quotes for MOS/LSI and other system semiconductor component requirements can also be made available at this time.

In general, we follow the standard/custom product tradeoff recommendations discussed in Section III. A broad and expanding line of standard MOS/LSI is available from Fairchild as alternatives to custom design. These vary from RAMs, ROMs and registers through Digital Voltmeters, TV Sync Generators and Buffer Memories to the PPS 25 Processor Set.

The PPS 25 is a set of MOS/LSI computer building blocks and is described in Appendix B. This system of devices represents a major breakthrough in the application of MOS/LSI to minicomputers and processors. Equipment engineers have long recognized the flexibility of equipment design afforded them if a minicomputer could be employed at the heart of the system. Such a design permits microprogramming of the system function and is ready tailored to fit a specified equipment need.

In system designs where a built-in minicomputer would be desirable, but cost and size are limiting factors, the Fairchild PPS 25 Processor Set offers an order of magnitude reduction in cost and several orders of magnitude reduction in size, provided that the system design can accomodate MOS performance and speeds. Virtually all small control and calculating systems can be economically designed from this set of components.

The SPRINT Accounting Calculator Set, described in Appendix C, is a low cost memory calculator for accounting purposes. Unlike the low cost algebraic calculator sets presently on the market, the SPRINT can perform a grand total operation on the extra memory. Many business problems such as invoicing, chain discounts and payroll problems can be solved without a copy and re-enter step.

Custom designs that have standard product potential offer mutual advantages to the customer and the vendor. Often, it is possible to give the customer both the economy of standard circuits and the competitive lead time of custom circuits. There remain, however, many applications for which there are no standard components. In these, a custom design is definately needed. At Fairchild, considerable investment has been made in the methods and software programs required for successful custom programs. Whether the outcome of such a program is a proprietary product or whether it eventually becomes a standard product is a decision that must be made by the customer. The basis for this decision is the potential economical advantages to all in allowing the design to become standard. The custom development charge and possibly the volume quantity cost would be lower if the product had potential as a standard to the vendor.

Optimum Partitioning: A Matter of Experience

Partitioning an MOS design is not fundamentally different from partitioning a large system assembly into modules. The designer is chiefly concerned with organization of the functions so that each unit is as complete as possible to optimize both performance and gate-to-pin ratio within the most economical number and size of chips.

If the system manufacturer is hesitant about his engineering staff's ability to partition an MOS design, he can consider interfacing with Fairchild's design group closer to the front end of the design process. (See fold-out chart in the back of this manual) The experience gained through working with Fairchild designers may allow the interface to be chosen farther down the line on the next project.

Micromosaic: A Better Way

Micromosaic custom design is covered in detail in Appendix D, but a few points pertinent to engineering management should be stressed here.

- The software required for Micromosaic design is comprehensive and readily understandable to any logic designer.
- Little knowledge of MOS is required.
- No computer programming knowledge is required.
- Depending upon the customer's in-house expertise, he can select the point at which the design responsibility is transferred to Fairchild. See the design interface points in the flow chart at the back of the book.

At the core of the Micromosaic System is the cell library and the powerful CAD software related to it. While the Micromosaic concept is not new, it has been greatly expanded under the OPTIMOS program. The cells, which are predesigned logic functions, are available for both silicon gate and metal gate designs.

These predesigned cells are thoroughly characterized and are represented by familiar bipolar positive logic symbols. As such, they enable the designer with very little knowledge of MOS technology to easily convert his design into MOS/LSI.

Assume a conventional logic diagram has been prepared (or a TTL breadboard). The designer selects the appropriate cells from the Micromosaic set, decides which cell connections are required and calculates logic path delays using the constants in the design appendix. The cell selections and connections are then listed in a simple code. If any delay problems are anticipated, delays are adjusted by substituting low speed or high speed cells for standard speed cells. Handwork on the design is now largely completed. The list, entered into the design computer, calls out the cell descriptions from a cell software library and the computer models the network. Then, the computer simulates circuit operation.

The cell library, which is fully specified in Appendix D, comprises all functions available in bipolar logic. These include gates and flip-flops as well as numerous other functions which can be combined to form long counter chains, sequential access memories, output buffers, clock generators and the like. In addition to these standard cells which perform specific functions, the Micromosaic library also contains composable cells which permit the designer to simulate a host of unique logic operations through a look-up table approach. In other words, the designer can specify input conditions to arrive at desired sets of output conditions. One version of a composable cell, for example, is similar to a read-only memory that is programmed to perform a unique logic operation. Thus composable cells not only provide an abundance of gates in a relatively small chip area — but they also simplify the design task by enabling the designer to work directly from truth tables.

CAD Weaves Cells Into Subsystem Arrays

Each of the Micromosaic cells (at this writing there are over 200 ranging in complexity from simple inverters to composable cells including both dynamic and static logic) is completely characterized in CAD software. This characterization includes a precise description of each cell's logic function, delay equations and associated photomask layout. When a cell is chosen for a design, its "vital statistics" can therefore be easily accessed and manipulated via the design computer.

These cells have a fixed height and variable width depending on logic complexity. During layout, the cells are arranged on the chip area in rows. Then they are systematically interconnected by thin-film wiring patterns routed between the cell rows. They are powered through supply and ground lines running over the rows. With the aid of the computer, the designer may rearrange the cells until the most suitable interconnection pattern is achieved.

The height of the wiring alleys between cell rows is also flexible to accomodate different wiring densities. Output buffers,

input level translators (if required) and bonding pads are then added to interface the chip with the package and the external system or another OPTIMOS circuit.

To further simplify the design process, the elements within the cells have standard geometries so that all logic cells have equivalent dc input/output transfer characteristics. Thus, signal propagation speeds within the array of cells can be automatically calculated from the nodal capacitances. These capacitances are computed using the data base of the completed computer-aided layout.

Interactive CAD Permits Fine Tuning

Fairchild has 12 computer-aided design programs that fit together in an integrated package to carry both standard and custom designs from concept to finished product. See flow chart at back of book.

MMAP — Transient and dc MOS circuit analysis

FAIRSIM — Logic simulation and verification

FAIRGEN — Functional test generation and verification

SENTRY — Merges parameter tests with output of FAIRSIM for Fairchild testers.

FAST — Calculates path speeds using cell and predicted interconnect capacitances

SPEED — Calculates path speeds using cell and actual interconnect capacitances

LAYOUT — Cell placement, wiring and verification

RETGEN — Converts LAYOUT output for use in reticle generator for mask making

NDRAW — Plots LAYOUT output plus general purpose plotting

V-MACRO — Hand digitizer

ROMCODE — Converts customer ROM pattern to RETGEN

PROSIM — Simulates ROM codes for PPS 25 (Programmed Processor System).

The major programs that the customer becomes directly involved with are FAIRSIM and FAIRGEN.

These CAD programs constitute a complete design system, and not just a collection of independent programs aiding in different aspects of the design process. All major components of the CAD system interface directly with one another via computer-generated data sets, thus eliminating many time consuming and error prone manual data preparation steps.

The FAIRSIM logic simulation program is used to check both silicon gate and metal gate MOS designs. The logic is exercised, within the computer, after the network assembly has been checked against the Netlist requirements. Use of the program is not difficult to learn, so the customer may run his own simulations and performance verifications if he prefers. And as discussed earlier, Fairchild's CAD programs are interactive; the layouts implemented through FAIRSIM can therefore be easily optimized by designer inputs.

FAIRSIM includes an array speed analysis program which predicts actual propagation delays within the cell array. It is used to examine critical logic paths so that possible race conditions can be detected and avoided. Moreover, these parameters can be evaluated for the parameter spreads produced by process variations and tolerances.

In effect, the simulation phase of CAD is a first order approximation of a thorough test of a prototype array. The computer output documents become a basic part of the array performance specifications. They give the customer and Fairchild a precise, detailed analysis of the array's functional behavior. Very few arrays checked with this program have required more than minor modification when the actual prototypes were made and tested. Just recently, a series of 24 arrays were put into production without one correction required. This is not to suggest that CAD is infallible, but it has certainly proved much more effective than conventional debugging.

Proper use of the FAIRSIM program eliminates any necessity to breadboard in most cases. It will almost invariably give a more accurate picture of array performance. Furthermore, when partitioning and laying out the arrays, the designer may find it convenient to implement logic functions with different cell groupings than a 1:1 translation of a bipolar logic breadboard. Some examples of useful cell groupings are given in the applications section of the cell library (Appendix D).

FAIRGEN is a CAD program for automatically generating functional tests. It also performs verification on proposed sequences to ensure that all possible faults are detectable. Another feature of FAIRGEN is establishing initial conditions in sequential circuits. If this task requires too much testing or the circuit cannot be initialized, FAIRGEN interacts with FAIRSIM to provide extra inputs for initializing.

As a circuit is being designed, it may be necessary to modify its design to make it testable. In general, the most important requirement is that the array must be capable of initialization to a known state after a predetermined input sequence is applied. Test points are sometimes added to reduce the test length, or to force initialization, or both. The undefined output state of FAIRSIM is very useful in identifying a logic path that cannot be initialized. More detailed information on testing is available in Fairchild's FAIRSIM and FAIRGEN program manuals. Most of the programs allow a large degree of designer interaction and interaction between each other. Thus, the designers have complete flexibility to use the computer as a tool to try out new design arrangements and then verify if they work.

Artwork Generation

Fairchild maintains an automated photomask generation facility. Unless hand optimization is desirable, computer controlled plotters or a reticle generator prepare the wafer fabrication patterns from the output of the LAYOUT program. The reticle generator prepares 10X plates directly.

The mask generation program closes the computer-aided design loop by fetching the functional pattern descriptions from the cell software library. All the computer generated data that might be needed to replicate or modify the design at some future time is stored away in a universal format.

Testing Sets the Pace

Testing difficulty skyrockets between medium scale integration (MSI) and LSI. Adequate test facilities have to be assured in advance because the typical lead time of an MOS/LSI design is shorter than the lead time for developing a computer controlled test capability.

The testing — both at the wafer probe and packaged device stages — is done with Sentry 400 and Super Sentry 600 test systems. Each Sentry 400 is capable of testing four arrays simultaneously at rates up to 286,000 tests per second. The Sentry 600 tests two arrays simultaneously at rates up to 5,000,000 tests per second. FAIRGEN effectively amplifies these rates by minimizing the number of test patterns used in functional testing. Other special diagnostic equipment is on-line for engineering analysis.

Dynamic tests (ac or "speed" testing) should not be specified unless essential. These take more test system time than dc and functional tests and usually do little more than increase the total cost once a device has been simulated and the prototype thoroughly tested. With good process control, dynamic performance of devices passing the normal tests will be consistent. The dc tests verify process control (also verified independently by the Quality Control department).

Varible Interface: A Balance of Resources

The high complexity of large scale integration (LSI) has placed Fairchild in the business of designing and fabricating subsystems, blurring the distinction between a component supplier and a systems engineering and consulting firm. Where the customer formerly interfaced mainly with circuit and component engineers, he must now communicate with system engineers, logic designers and package engineers as well. Thus the LSI customer must be more aware of key aspects of process technology such as economic chip sizes, testing methods, etc. Since each customer has different levels of expertise and manpower, as well as varying design schedules, no single interface program will be optimum for all customers.

In general, the interface should divide and identify responsibilities as clearly and thoroughly as possible. The flow chart in the back of this manual illustrates the key steps and the interface options available. The extensive use of computer-aided design lowers costs and ensures quick turnaround.

The system design phase clearly must be performed by the customer. The areas of partitioning, logic design and test generation are flexible and may be performed either by Fairchild or by the customer. Mask generation, fabrication and testing must be done by Fairchild.

Many working interface relationships are possible, each of which encompasses three basic elements: design data, design verification and customer involvement.

A DESIGN DATA OPTIONS

1. *Performance Specifications:* Customer performs system design and generates performance specifications. Fairchild performs partitioning and logic design.
2. *Performance Specification with Partitioning:* The customer performs enough initial design to partition the system into arrays. Logic design is done by Fairchild.
3. *Logic Diagram, Unpartitioned:* The customer provides logic diagrams of the required function, with no partitioning. Unfortunately, it is usually impractical to perform partitioning without a thorough knowledge of the system, since the logic implementation is likely to change radically during partitioning.
4. *Non-Micromosaic Logic Diagram, Partitioned:* The customer provides logic diagrams of partitioned arrays. Fairchild converts the logic into Micromosaic cells with logic minimization wherever possible.
5. *Partitioned Micromosaic Logic Diagram:* The customer provides the logic diagram of partitioned arrays, converted to Micromosaic cells. Fairchild checks logic design for minimization, testing requirements, etc.
6. *Design Ready for Layout:* The customer provides logic diagrams and/or FAIRSIM network descriptions of partitioned arrays ready for layout without further simulation.

B DESIGN VERIFICATION OR TEST DATA OPTIONS

Because of the economic incentive to get an LSI design right the first time, extensive checking of a design before mask design is mandatory.

1. *Performance Specification:* The customer provides complete performance specifications for the system. Fairchild simulates all arrays and accepts responsibility for the operation of the system. Fairchild also generates individual functional tests for all arrays.
2. *Customer Analysis of Fairchild Tests:* Fairchild simulates the proposed design to its own input sequences. The customer analyzes the simulation output for correct operation. Fairchild generates production func-

tional tests for all arrays. This method is practical for arrays with an easily understood operation, such as counters, buffers, etc., but is impractical for complex control logic.

3. *Customer Supplied Input Sequence:* The customer supplies input sequences in truth table or timing diagram form. Fairchild simulates and provides simulated output for customer analysis. Fairchild generates production functional tests.

4. *Customer Supplied Input and Output Specifications:* The customer supplies input and output data in truth table or timing diagram form. This method allows Fairchild to simulate and verify a design directly. Fairchild generates production functional tests.

5. *Customer Supplied Functional Tests:* The customer supplies input/output sequences of production test length. Fairchild uses tests to verify design and for production testing.

6. *Customer Supplied FAIRSIM Input:* The customer supplies input sequences in FAIRSIM format for simulation of the design. Fairchild performs simulation and presents the simulated operation to the customer for approval. Fairchild performs production functional test generation.

7. *Customer Supplied Functional Tests in FAIRSIM:* The customer provides design verification sequences and production functional test sequences in FAIRSIM format.

C PHYSICAL INTERFACE

1. *Mail, Telephone, and Telecopier:* All design data is communicated via mail, telephone, and/or telecopier. This interface is used primarily when little customer involvement is required, as in the case of performance specifications.

2. *Fairchild Team at Customer's Plant:* This approach is most commonly used in the initial stages of system design, when a large degree of customer involvement is anticipated. A one-day seminar is presented on partitioning and on use of the Micromosaic cell set.

3. *Customer Team at Fairchild:* This is the most common and useful interface, since it allows instant communication and on-line use of the CAD system. It is most commonly used during the detailed design and simulation phase.

Obviously, the working relationship between Fairchild and the Micromosaic customer is often complex. However, the optimum tradeoff among cost, scheduling, and design confidence can be obtained by selecting various options from each of the basic interface elements — design data, design verification and testing, and the amount of customer involvement.

Fairchild Uses Proven MOS Processes

Fairchild is presently producing custom circuits with the two proven P-channel MOS processes silicon gate and high-threshold metal gate. Currently, silicon gate is being used in the majority of standard and custom MOS designs at Fairchild because of its advantages in most applications.

When compared to the metal gate process, the silicon gate approach is generally more economical as it provides higher circuit densities, greater operating speeds and, in many instances, requires fewer off chip components. The basic silicon gate and metal gate processes are compared in greater detail in Appendix G. The two processes are compatible and have been effectively combined in specific custom applications. Moreover, the superior noise immunity inherent in high-threshold metal gate circuits can often be a welcome adjunct to silicon gate designs.

Fairchild is continually performing research on new MOS and bipolar processes, offering them only when they have proven their viability in a production environment. Ion implantation, for example, has recently demonstrated its capability as a production process, and Fairchild will soon be offering ion implanted silicon gate devices — both standard and custom. Fairchild's Isoplanar process has proven itself in the bipolar arena, and will soon be commercially applied to P-channel MOS after further refinements. With Isoplanar P-channel MOS, Fairchild can reduce the size of silicon gate devices by about 40%. This dramatic size reduction is made possible because of two factors: the Isoplanar process moves active elements closer together by lateral oxide isolation and self-aligned contacts — and the oxide surface without steps allows a proportional improvement in interconnection density through higher resolution photomasking. The Isoplanar process combined with ion implantation will also offer higher speeds due to decreased capacitances of both cells and interconnections.

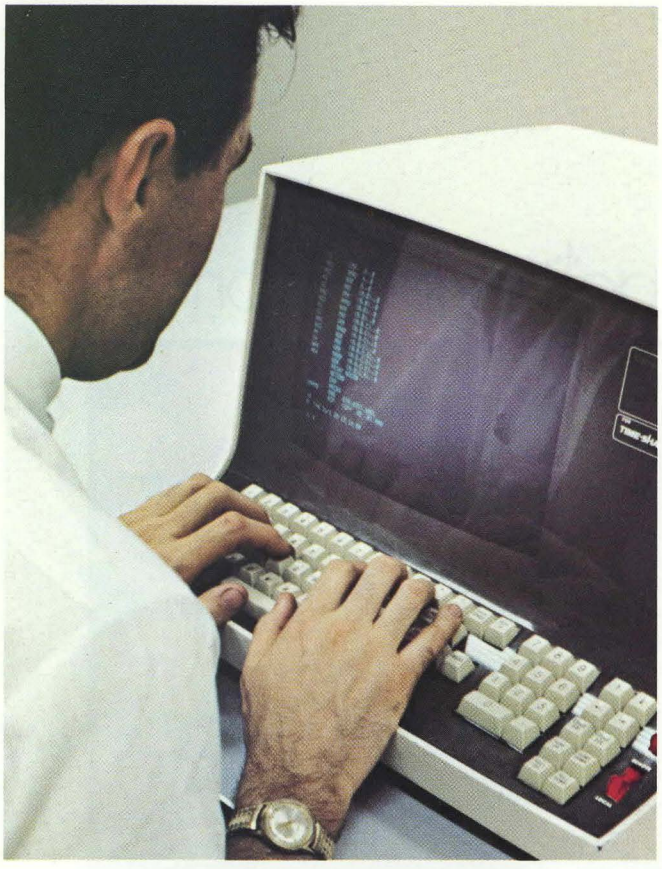
The Fairchild Capability in Review

Fairchild offers strength in the areas of both standard and custom MOS/LSI. The broad selection of 51 standard circuits covers a wide range of applications. The computer-aided design programs ensure the custom user of workable "first time" custom results, regardless of his level of expertise. The proven silicon gate process ensures the MOS user of a reliable economic product. The Isoplanar process offers lower cost circuits with higher performance in the future. The heavy investment in test equipment and test pattern generation programs ensures that the product is what the user wants. The photo section offers a plant tour of the Fairchild MOS facilities.

Before choosing a vendor, the wise MOS user will visit the facilities for a review of vendor capabilities. At Fairchild we invite comparison.

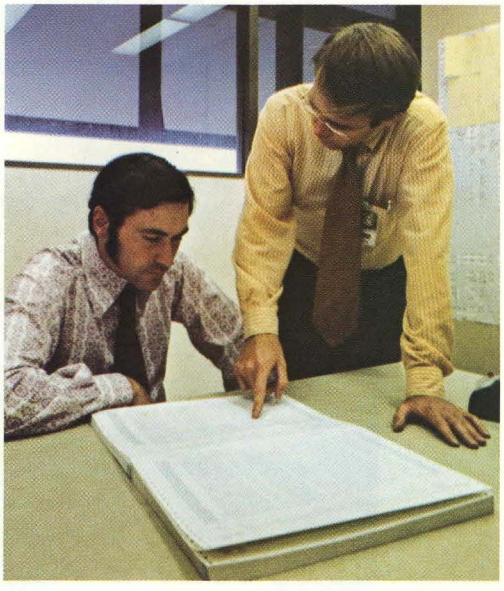
OPTIMOS Facilities In Action

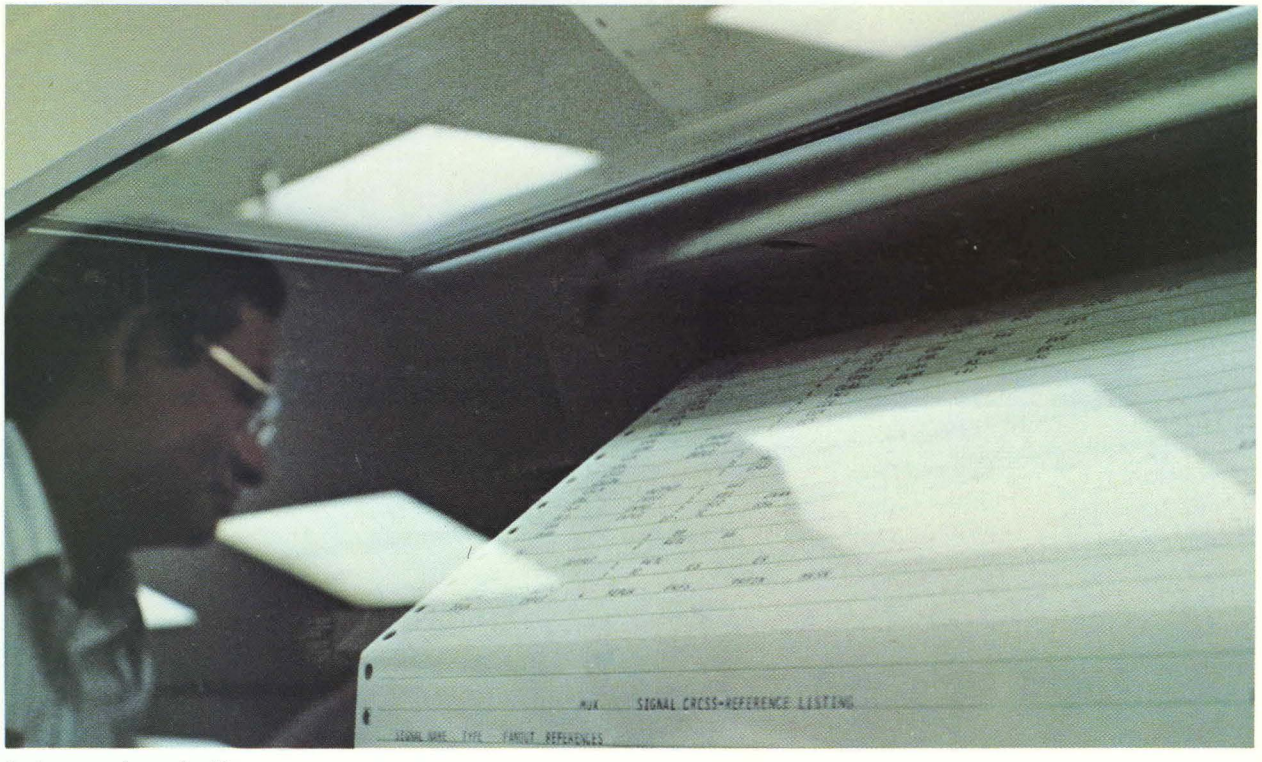
Designer interfacing with computer programs in a logic simulation problem.



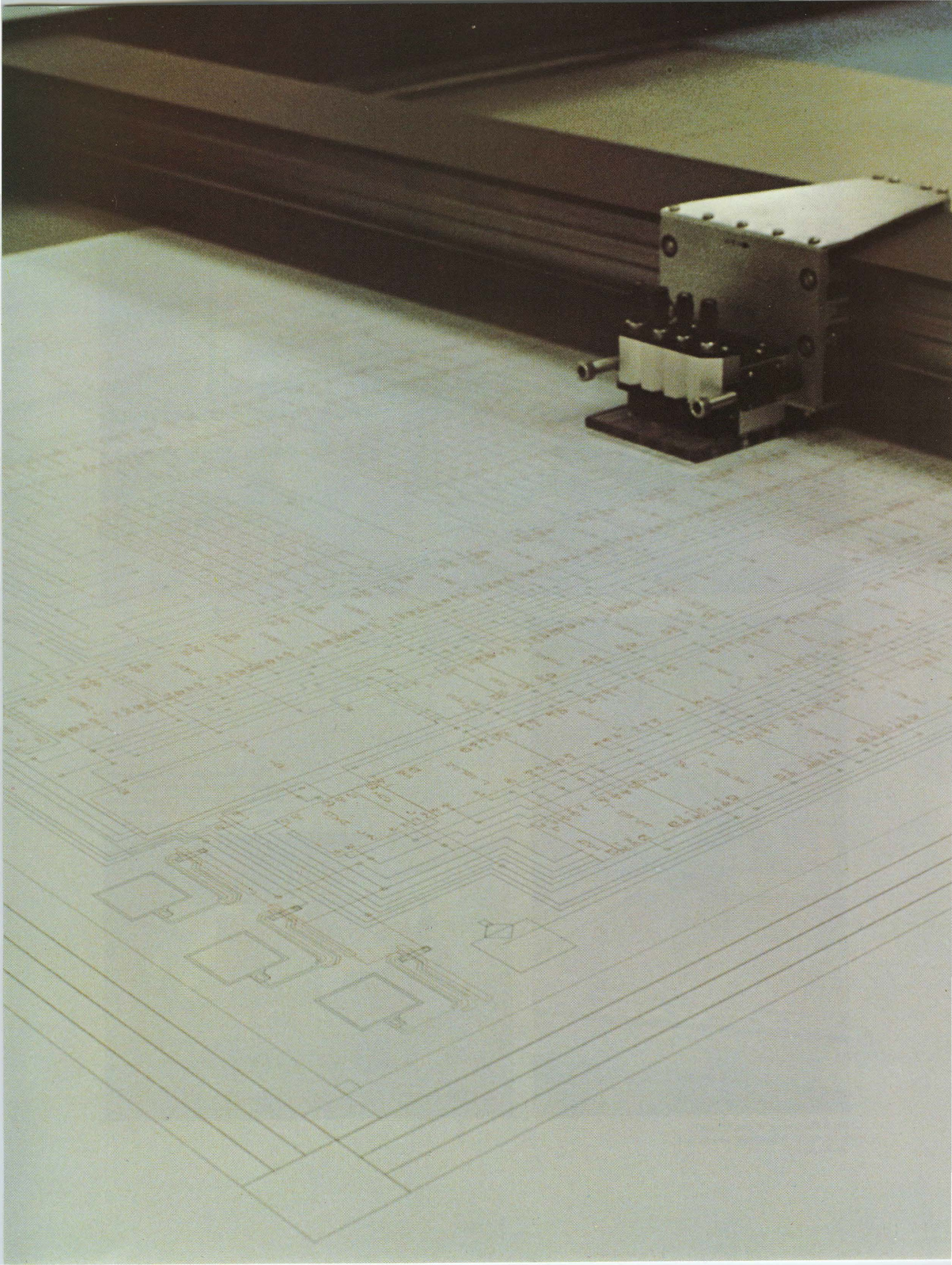
Calcomp stick plot of the 3261 TV Sync Generator using Micromosaic cells. The cells are shown box outlines and metal and silicon interconnects are shown as lines.

Designers checking FAIRSIM Netlist.

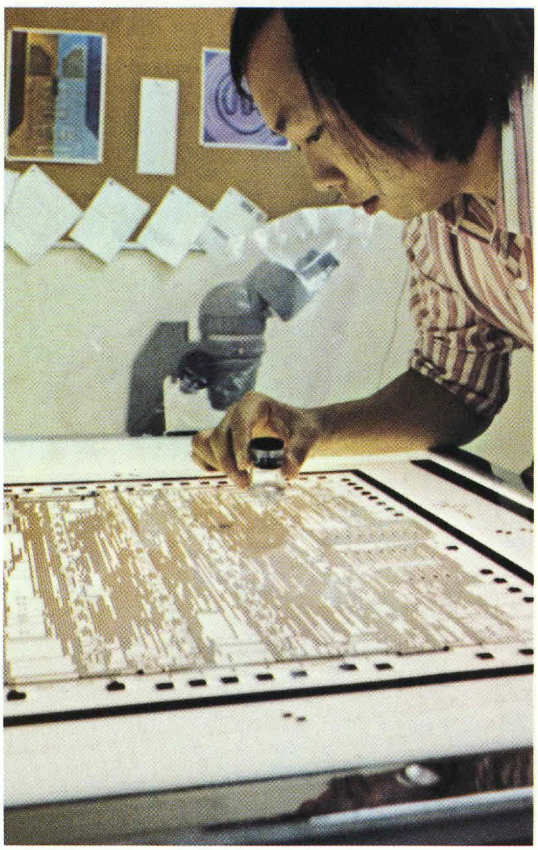




Customer engineer checking FAIRSIM listing.

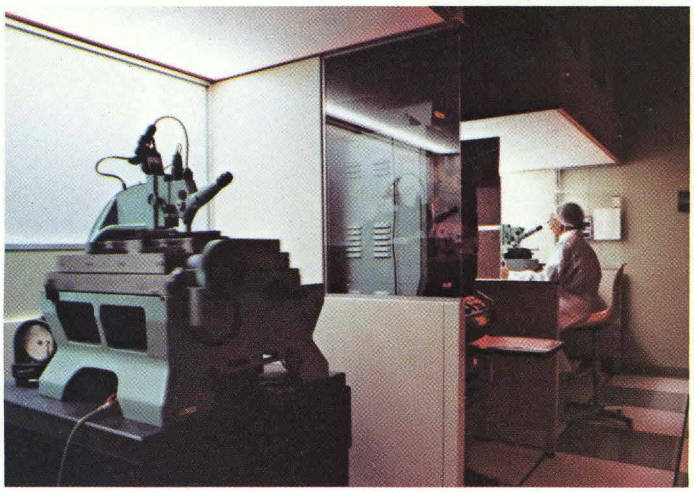


The RETGEN program converts the LAYOUT output to a David Mann Reticle Generator. This system eliminates the rubylith cut and peel step by exposing photographic plates (reticles) with a 10 to 1 image.



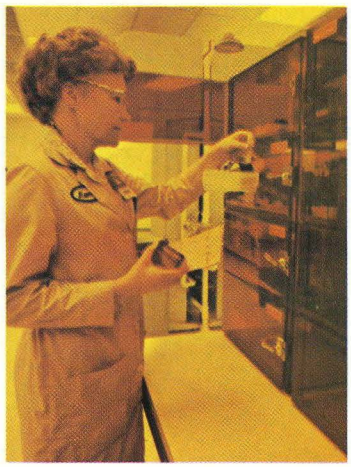
An 80X blowup of the artwork, is made for alignment and circuit verification.

The 10X reticle is converted to a 1X master by exposing a photographic plate with repeated images in rows and columns. Working plates are made from the master plates.

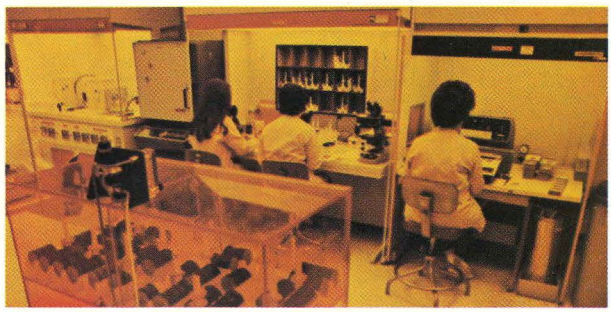


Silicon wafers become photographic plates after being coated with a layer of etch resist. The resist is then baked. These photo steps are all performed in a room with controlled lighting.

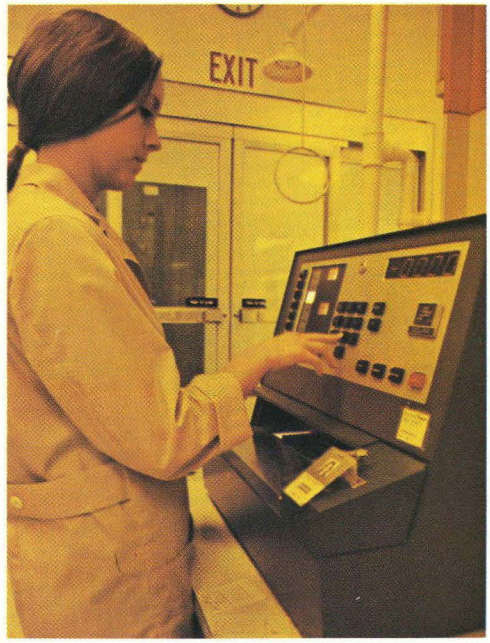
The coated wafers are stored in light-filtered boxes prior to exposure.



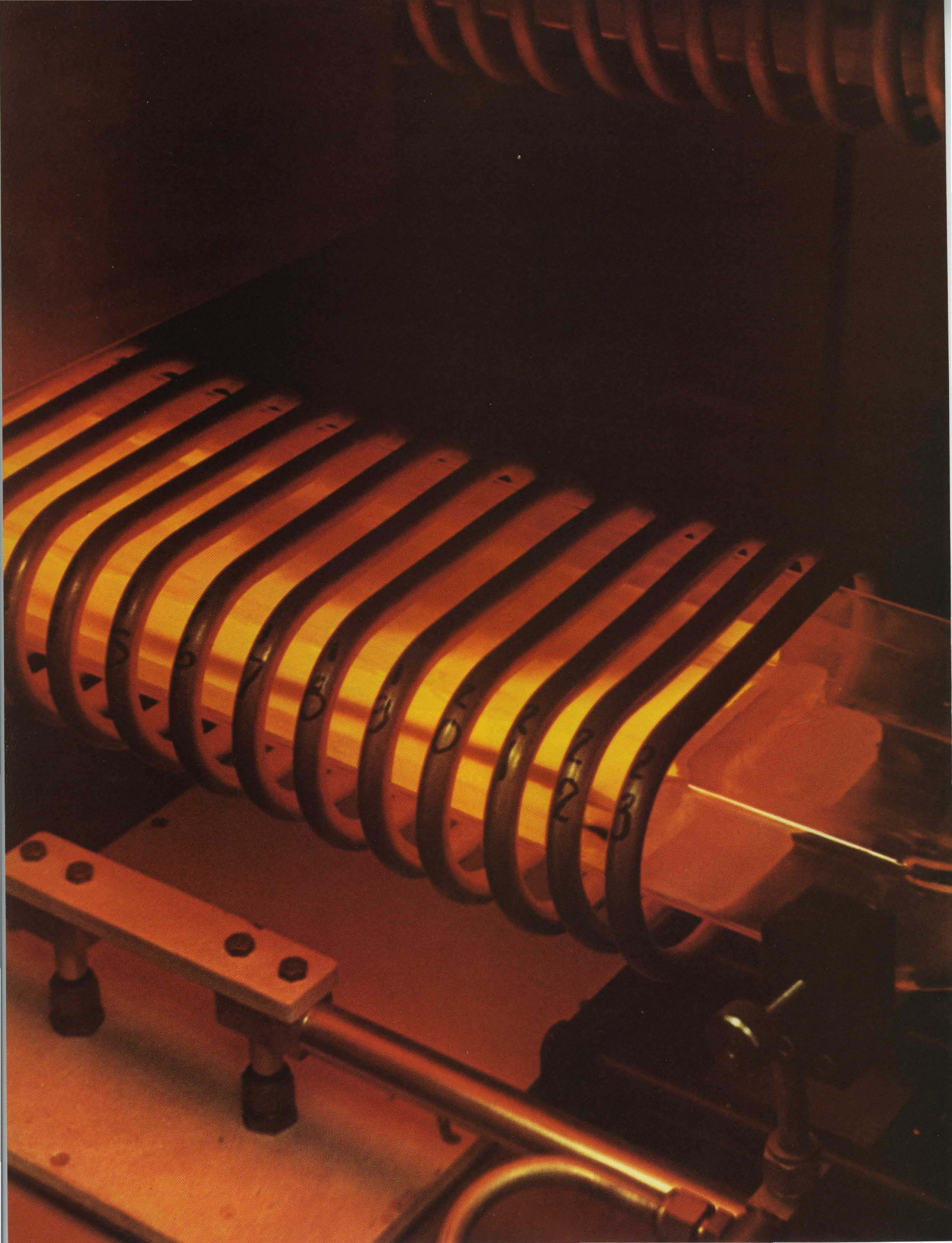
The exposed wafers are developed in the right-hand station. A rinse removes the unexposed etch resist exposing the surface for future chemical action. The center station is an in-process inspection station. The light-filtered box in the foreground stores exposed wafers until they are developed.



In these mask aligners, new mask patterns (from working plate) are aligned to the existing pattern on the wafer. A box of working plates is shown in foreground.



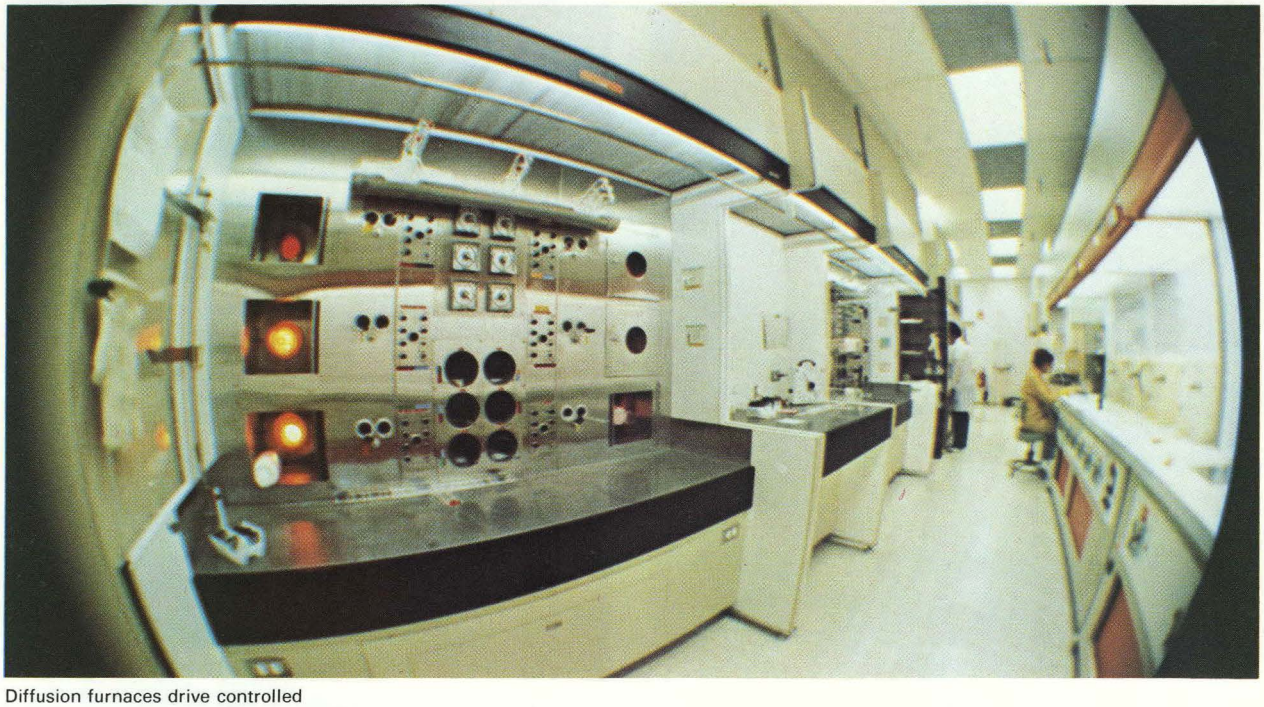
Wafer movement is recorded in a production control terminal that maintains control of all material in the production flow.



Wafers are loaded into a silicon reactor which deposits polysilicon metal in the gate and interconnection areas.

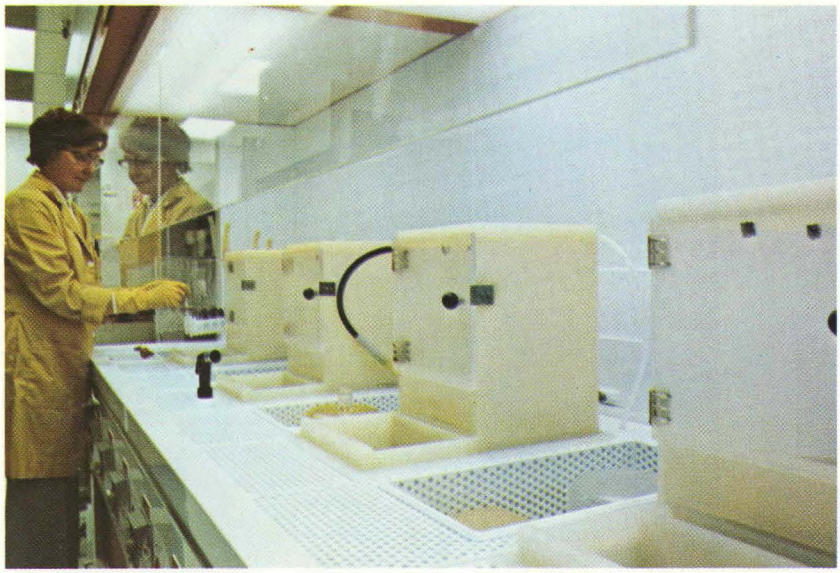
Loading a diffusion furnace.

Wafers being unloaded from silicon reactor.



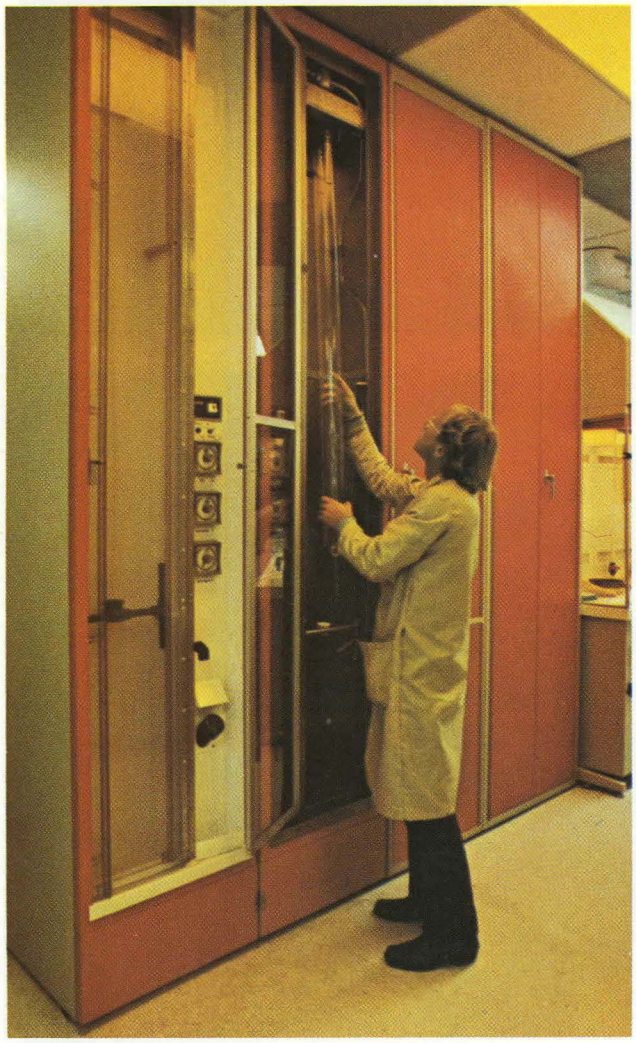
Diffusion furnaces drive controlled impurities into silicon to form parts of the MOS transistors.

Rinse stations used in cleaning steps.

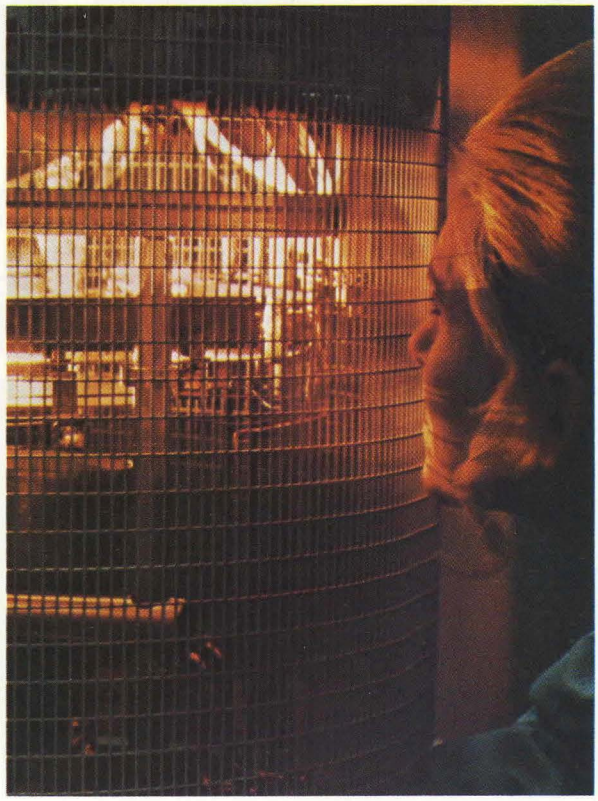


Finished wafers are functionally tested before committing a die to a package. The reject units are marked by a pen located in the middle of the probes.

Film thickness measurements are made on an interferometer. Thickness can also be monitored on an ellipsometer (see chart on wall).

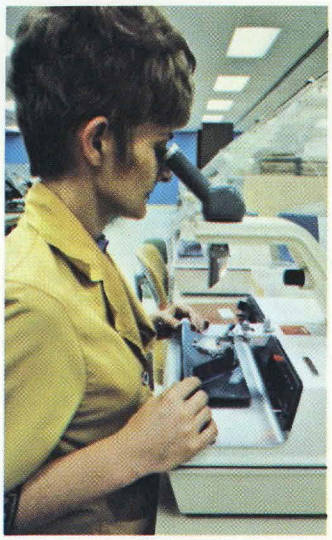


The diffusion furnace tubes are regularly cleaned by flushing with HF (hydrofloric acid), rinsed with DI water and dried with N2.

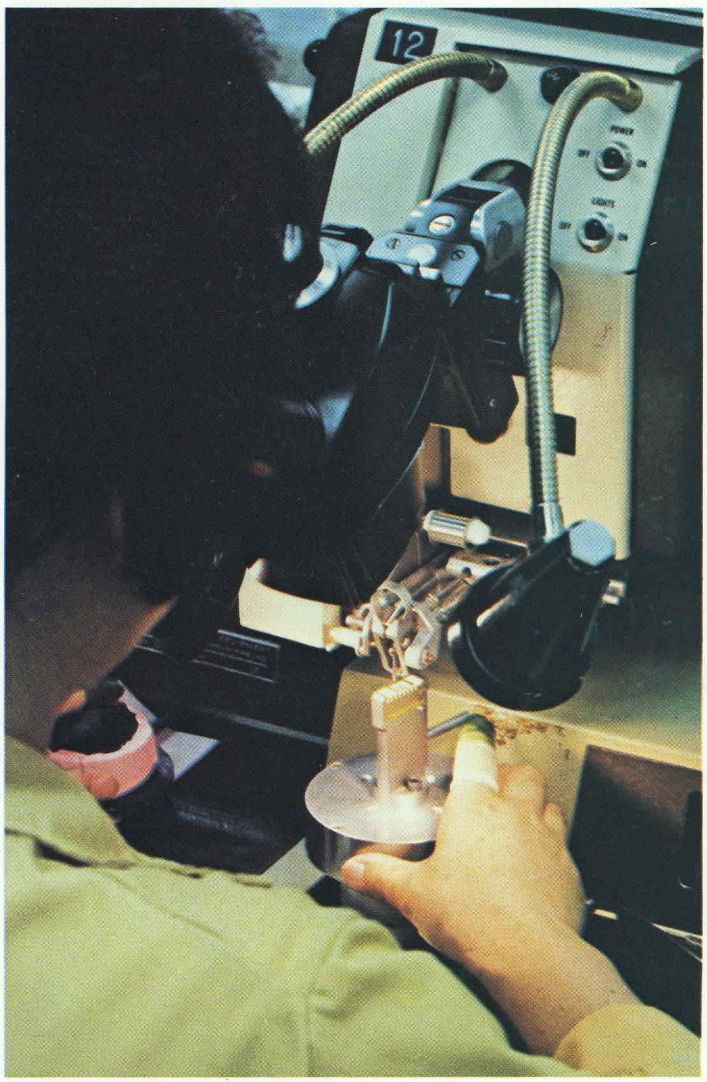


Aluminum metal is deposited in vacuum chambers. A planatary gear arrangement insures that the metal forms evenly over the steps in the oxide surface.

Tested wafers are scribed with a diamond scriber. The wafers are then fractured along these scribe marks and separated into dice.



Die bonding welds acceptable dice into a package for interconnection purposes.

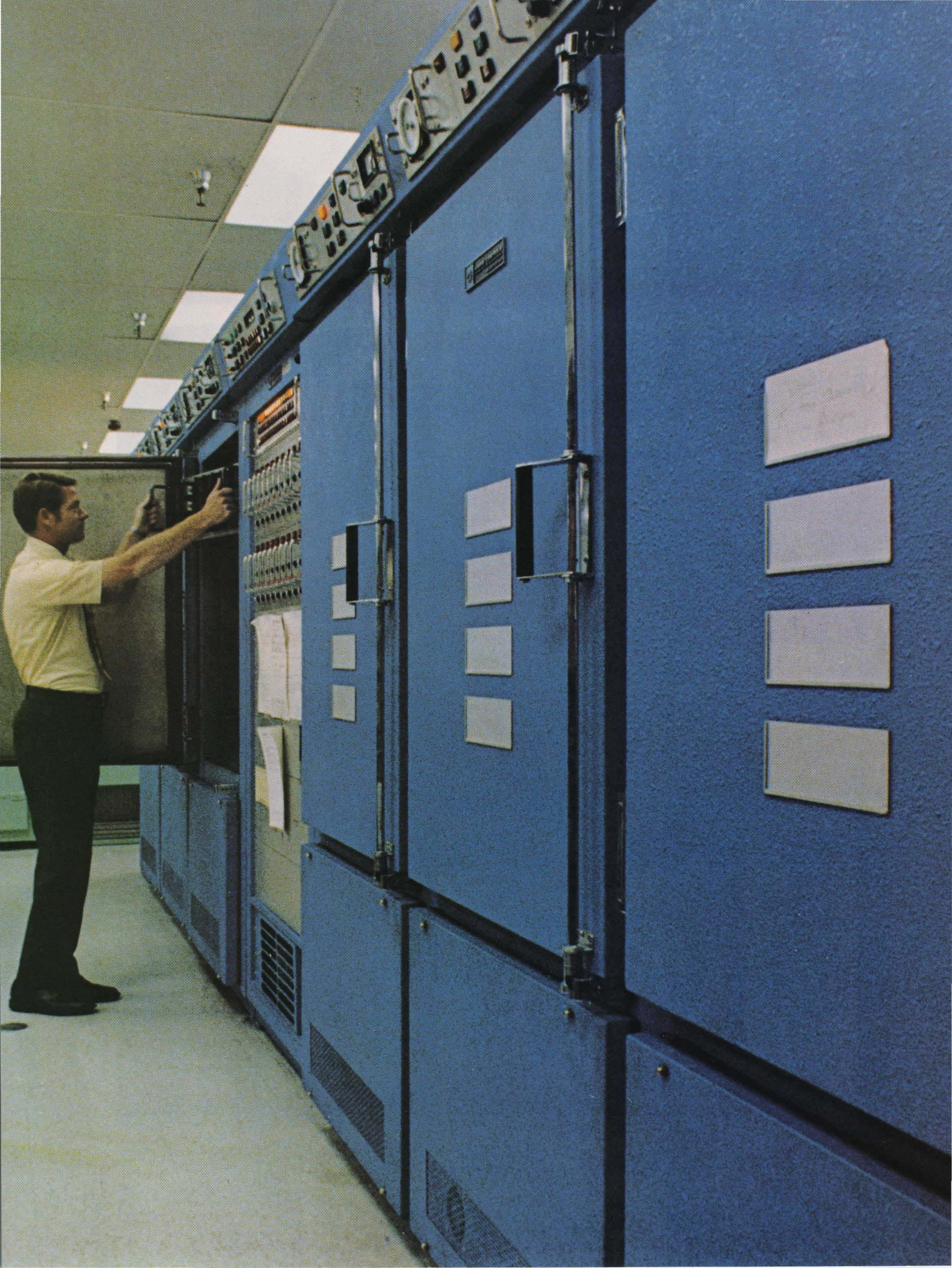


Wire bonding connects the pads on the die to the leads of the package.

The packages are sealed with a lid to provide environmental and mechanical protection to the die.

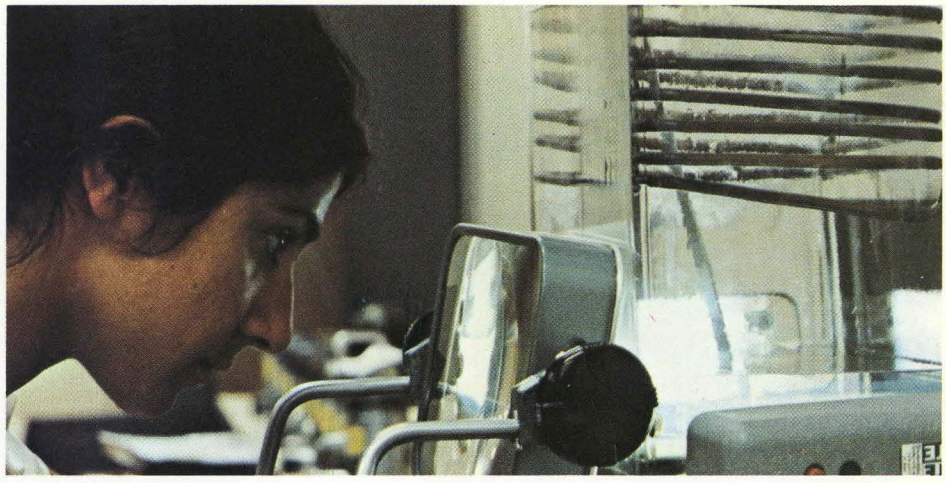
Fairchild's testing capabilities include a Super Sentry 600 and several Sentry 400 test systems. Each Sentry 400 can handle 4 stations and the Super Sentry can handle 2 stations.

Packaged unit testing on a Super Sentry station.

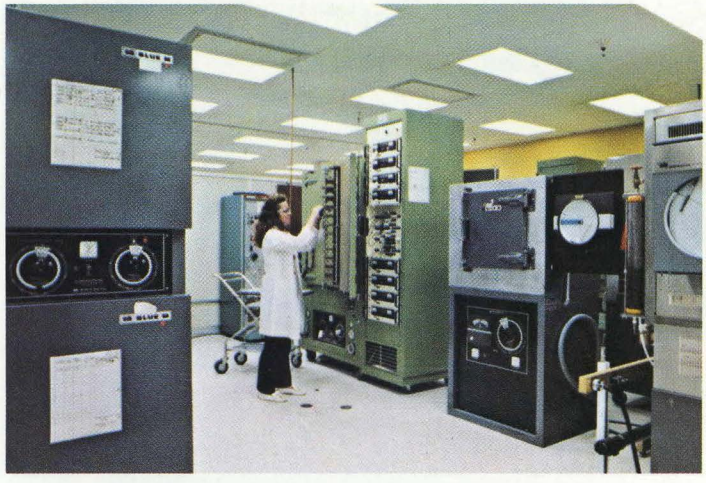


Production burn-in racks.

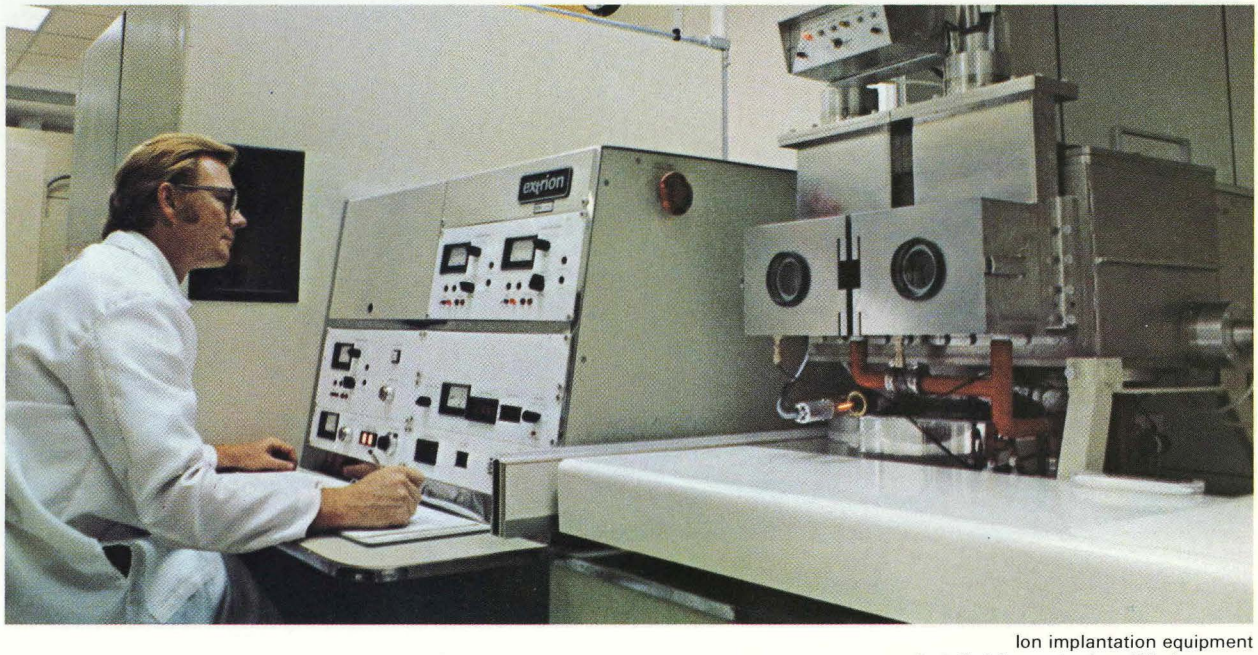
Gross leak testing ensures the quality of the seal.



R & QA environmental processing area for high reliability processing.

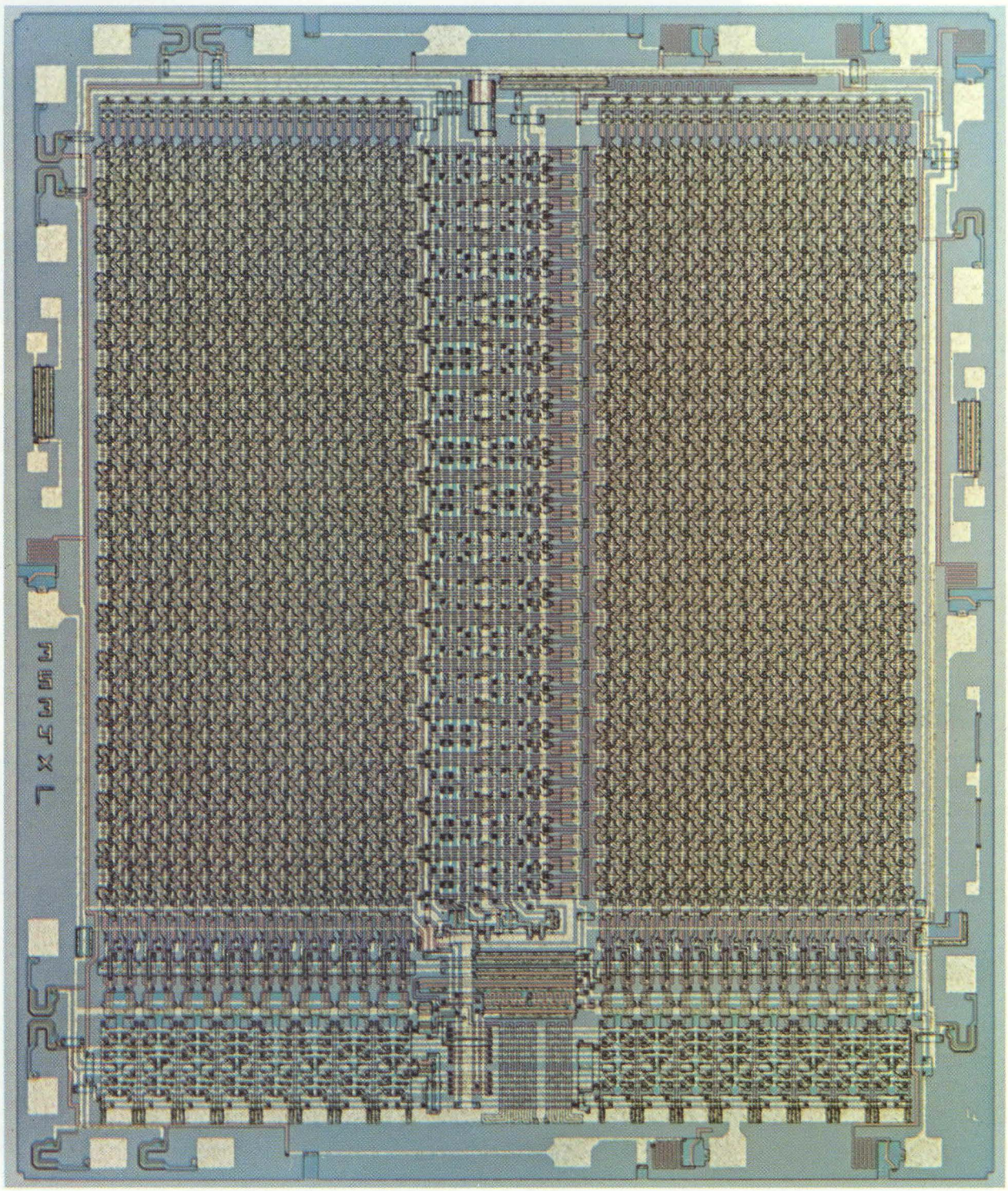


R & QA lab provides both routine inspections and failure analysis.

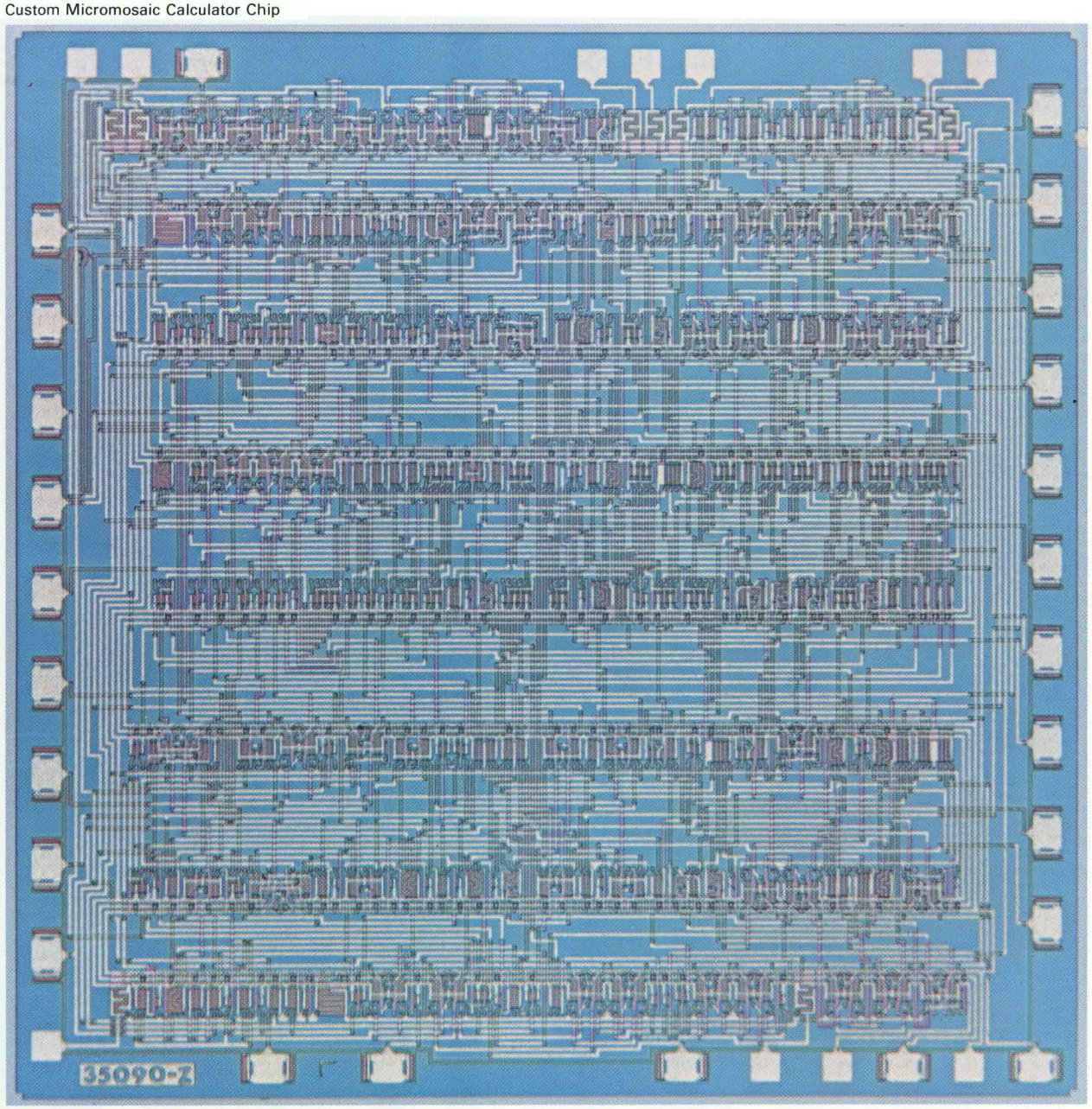


Ion implantation equipment installed in production diffusion room for use with Isoplanar to provide superior density and performance.

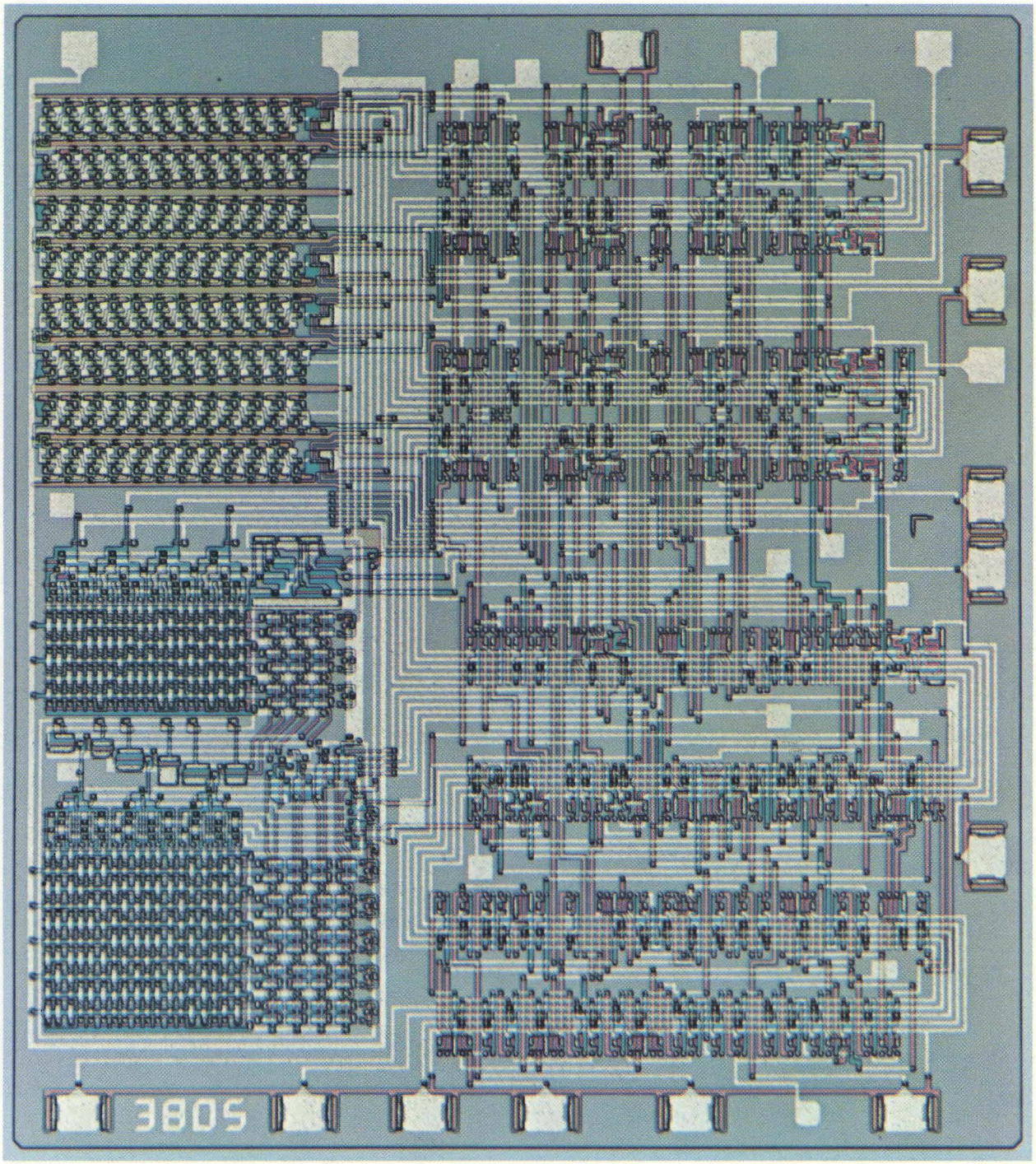
3534 – 1024-Bit
Random Access Memory



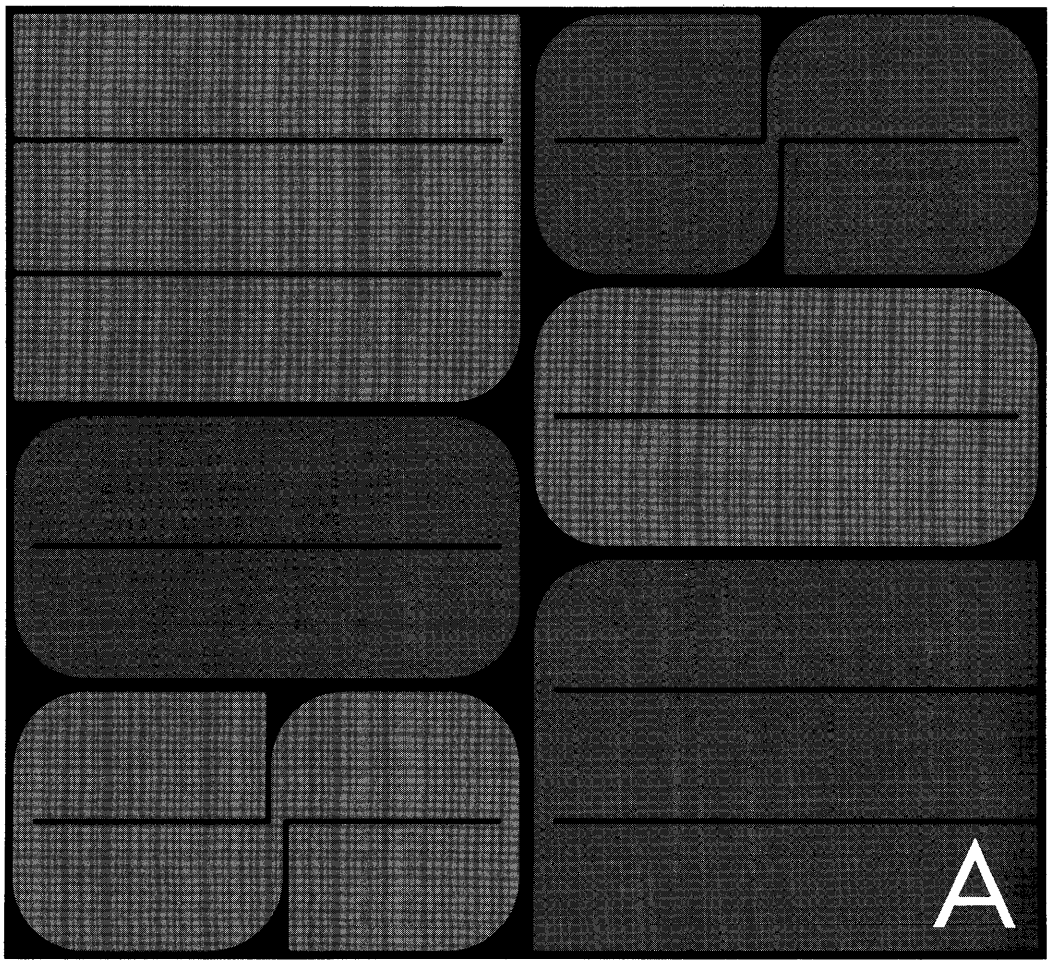
Custom Micromosaic Calculator Chip



3805 – PPS 25 Arithmetic Unit



Standard Product Data Sheets And Application Notes



APPENDIX A

STANDARD PRODUCT DATA SHEETS AND APPLICATION NOTES

This device type and description list delineates the standard product data sheets included in this portion of the appendices. The silicon gate products proceed the metal gate devices. Application notes for the 3341 FIFO, 3532 512-Word by 1-Bit RAM, 3534/1103 1K ROM and 3814 DVM are also included. They are located with the corresponding data sheet. There is also a hybrid device included — the SH0013 2-Phase MOS Dual Clock Driver. It is useful in many MOS applications.

SILICON GATE

Device	Description	Page	Device	Description	Page
3257	64 x 5 x 7 Out Character Generator, Custom or ASCII Font	35	3349	Hex 32-Bit Static Shift Register	86
3258	64 x 7 x 5 Out Character Generator, Custom or ASCII Font	42	3383	256-Bit Dynamic Shift Register	88
3260	64 x 9 x 7 Out Character Generator, Custom or ASCII Font	48	3512	256 x 8 (2048-Bit) Read-Only Memory, Custom Pattern	92
3261	TV Sync Generator	56	3512A	256 x 8 (2048-Bit) Read-Only Memory, Selectric to ASCII/ASCII to Selectric	96
3325	Quad 64-Bit Dynamic Shift Register	60	3513	256 x 10 (2560-Bit) Read-Only Memory, Custom Pattern	98
3329	512-Bit Dynamic Shift Register	64	3514	512 x 8 (4096-Bit) Read-Only Memory, Custom Pattern	103
3330	480-Bit Dynamic Shift Register	64	3514A	512 x 8 (4096-Bit) Read-Only Memory, ASCII-EBCDIC/EBCDIC-ASCII	107
3331	500-Bit Dynamic Shift Register	64	3532	512 x 1 Static Read/Write Memory	109
3341	64 x 4 First-In First-Out Memory	68	3534/1103	1024 x 1 Dynamic Read/Write Memory, 300 ns Access Time	120
3341	Application Note	74	3534/1103	Application Note	127
3342	Quad 64-Bit Static Shift Register	80	3708	8-Channel Decoded Multiplexer	150
3343	Dual 128-Bit Static Shift Register	82	3814	Digital Voltmeter Logic	154
3344	Dual 132-Bit Static Shift Register	82	3814	Application Note	158
3345	Dual 136-Bit Static Shift Register	82	*3815	5-Decade Counter	163
3346	Dual 144-Bit Static Shift Register	82	*3816	÷3 to 261,145 Programmable Counter	163
3347	Quad 80-Bit Static Shift Register	84			
3348	Hex 32-Bit Static Shift Register with Buffer Enable	86			

*To be announced.

METAL GATE

Device	Description	Page	Device	Description	Page
3100	5-Input Gate	164	3700	4-Channel Multiplexer	180
3101	Dual JK Flip-Flop	166	3701	6-Channel Multiplexer	184
3102	3-Input Gate	168	3705	8-Channel Decoded Multiplexer	186
3300	25-Bit Static Shift Register	171	3750	10-Bit D to A Converter	190
3326	Triple 66-Bit Dynamic Shift Register	173	3751	12-Bit A to D Converter	194
3501	128 x 8 (1024-Bit) Read-Only Memory, Custom Pattern	176	3800	8-Bit Parallel Accumulator	200
			3801	16-Bit S-P,P-S Converter	205

HYBRID

Device	Description	Page
SH0013	2-Phase MOS Dual Clock Driver	208

3257
DOT MATRIX
CHARACTER GENERATOR 64 CHARACTERS 5×7 BITS
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3257 is a Character Generator designed to display 64 characters in a 5 x 7 font. An on chip column select counter sequences through the five columns of each character. The seven output buffers will each drive one TTL/DTL load directly at a 1 MHz input address rate making the 3257 an ideal device for vertical scan CRT displays. The chip enable allows wired-OR capability if more than 64 characters are required.

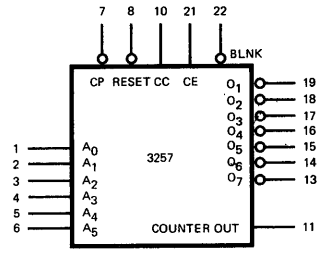
- **PROGRAMMABLE WITH A CUSTOM CHARACTER FONT**
- **500 ns TYPICAL ACCESS TIME**
- **STANDARD PRODUCT ASCII ENCODED**
- **DIRECT INTERFACING WITH TTL/DTL (FIGURE 8)**
- **WIRED - OR CAPABILITY**

ABSOLUTE MAXIMUM RATINGS — (Above which useful life may be impaired)

Storage Temperature T_S	−65° C to +150° C
Operating Temperature T_A	0° C to +70° C
Voltage on any Pin Relative to V_{SS}	−20 V to +0.3 V

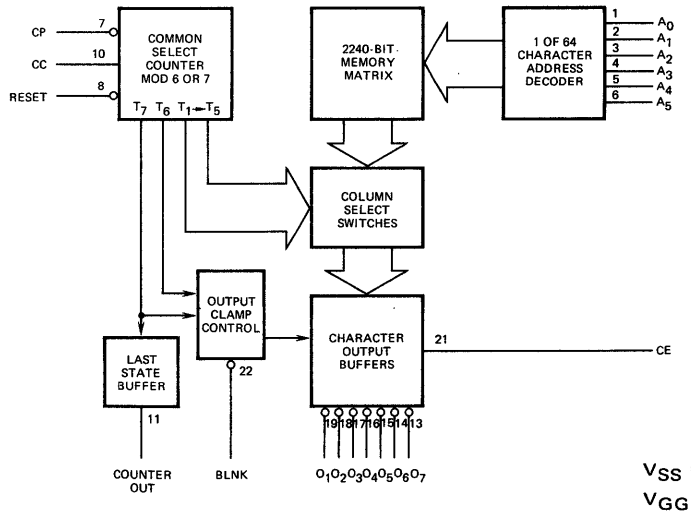
APPLICATIONS:
CRT Displays
Billboard Displays
LED Matrix Displays

LOGIC SYMBOL



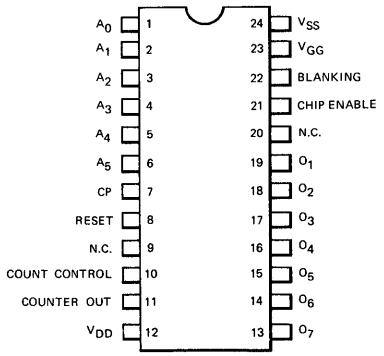
V_{SS} = Pin 24
V_{GG} = Pin 23
V_{DD} = Pin 12

BLOCK DIAGRAM



V_{SS} = Pin 24
V_{GG} = Pin 23
V_{DD} = Pin 12

CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION – A Reset pulse (~GND) is required to set the counter to the last state. A 6-bit binary word presented to the character address inputs is decoded to select 1 of 64 characters in the memory. Information, representing the first column of the character is available the next clock time after Reset returns HIGH ($\sim V_{SS}$). The remaining four columns are sequentially selected by the next four states of the counter. The last state of the counter clamps the outputs HIGH ($\sim V_{SS}$) to provide 1 or 2 space blanking between characters (Count Control $\sim V_{SS} \Rightarrow$ MOD 7, Count Control ~ GND $\Rightarrow$ MOD 6). When the last state (6th or 7th) of the counter is reached, the Counter Output goes HIGH ($\sim V_{SS}$). When Chip Enable goes HIGH ($\sim V_{SS}$), the chip is activated while a LOW (~ GND) at this lead floats the outputs to allow common output bussing. A LOW (~ GND) on the Blanking input pulls the outputs HIGH ($\sim V_{SS}$), providing blanking independent of the counter state or the character address.

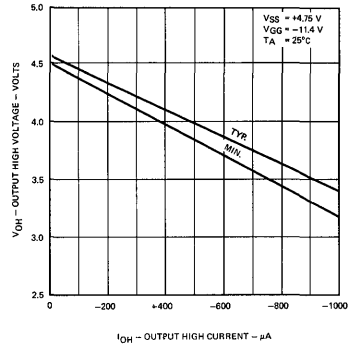
DC CHARACTERISTICS:

V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0°C to +70°C (Standard operating conditions unless otherwise specified)

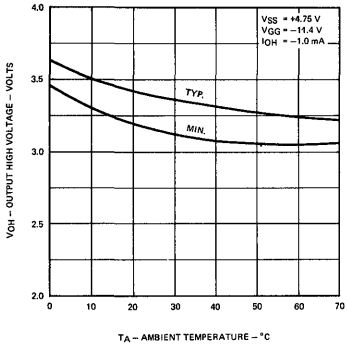
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS} −1		V_{SS}	V	Note 1
V_{IL}	Input Voltage LOW	V_{GG}	0	0.8	V	Note 1
V_{OH}	Output Voltage HIGH	V_{SS} −0.5 2.4	 3.0	V_{SS} V_{SS}	V V	I_{OH} = −10 μA I_{OH} = −0.5 mA
V_{OL}	Output Voltage LOW	0	0.3	0.4	V	I_{OL} = 1.6 mA
I_{LI}	Input Leakage Current			−1.0	μA	V_{SS} = 0 V, V_{IN} = −18 V, Note 1
I_{LO}	Output Leakage Current			1.0	μA	V_{SS} = 0 V, V_{OUT} = −6 V, Note 2
I_{SS}	V_{SS} Current		20	40	mA	V_{SS} = 5.25 V, V_{GG} = −12.6 V Outputs Open
P_D	Power Dissipation		360	715	mW	

NOTES:
1. Inputs include Character Address, Count Control, Clock and Reset.
2. Chip Enable = LOW.
3. $I_{SS} = -I_{GG}$ (V_{GG} Supply Current)

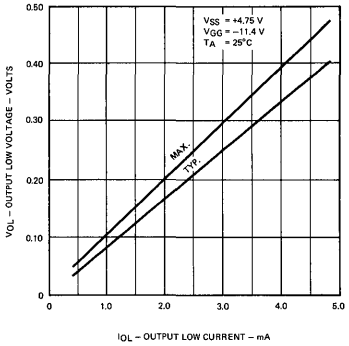
OUTPUT VOLTAGE HIGH VERSUS OUTPUT CURRENT



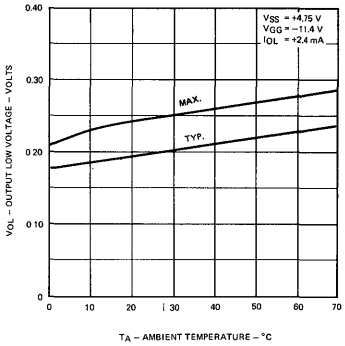
OUTPUT VOLTAGE HIGH VERSUS AMBIENT TEMPERATURE



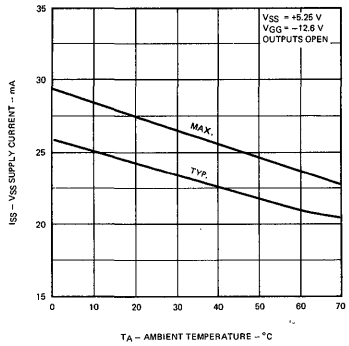
OUTPUT VOLTAGE LOW VERSUS OUTPUT CURRENT



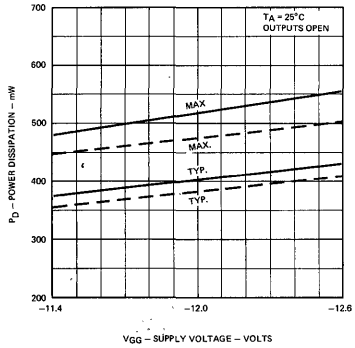
OUTPUT VOLTAGE LOW VERSUS AMBIENT TEMPERATURE



WORST CASE V_{SS} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



POWER DISSIPATION VERSUS SUPPLY VOLTAGE

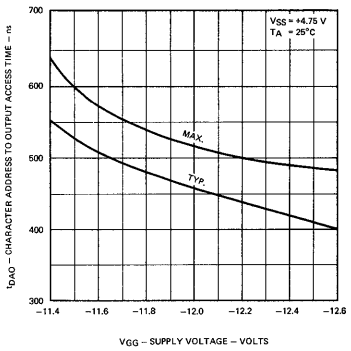


AC CHARACTERISTICS: V_{SS} = +5 V ±0.25 V, V_{GG} = −12 V ±0.6 V, V_{DD} = 0 V, C_L = 10 pF, T_A = 0°C to +70°C.

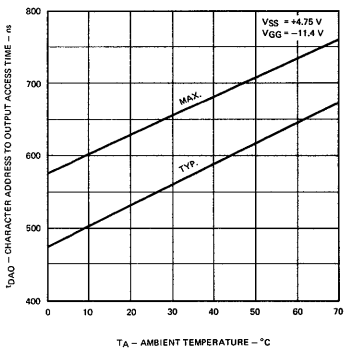
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Clock Frequency	dc		1.0	MHz	
$t_{PW\phi}$	Clock Pulse Width	500			ns	
t_r, t_f	Clock Rise & Fall Time (10%-90%)			2.0	μs	
t_{PWR}	Reset Pulse Width	500			ns	
t_{RS}	Reset to Clock Set Up Time	100	300		ns	Fig. 5
t_{DAO}	Character Address to Output Access Time		500	1000	ns	Notes 4 & 5, Fig. 1
$t_{D\phi O}$	Clock to Output Access Time		500	1000	ns	Notes 4 & 5, Fig. 2
t_{DRO}	Reset to Output Time Delay		300	600	ns	Notes 4 & 5, Fig. 3
t_{DBO}	Blanking to Output Time Delay		300	1000	ns	Notes 4 & 5, Fig. 6
$t_{D\phi C}$	Clock to Counter Output Time Delay		300	500	ns	Notes 4 & 5, Fig. 2
t_{DRC}	Reset to Counter Output Time Delay		300	500	ns	Notes 4 & 5, Fig. 3
t_{DOE}	Output Enable Delay Time		300	600	ns	Notes 4 & 5, Fig. 4
t_{DOD}	Output Disable Delay Time		300	600	ns	Notes 4 & 5, Fig. 4
C_I	Input Capacitance		5.0	1.0	pF	f = 1.0 MHz, 0 V Bias Note 1

4. AC Output LOW level is defined as 0.4 V @ 1.6 mA, current sinking (i.e., 1 TTL load).
5. AC Output HIGH level is defined as 2.4 V @ −0.6 mA, current sourcing (i.e., 1 TTL load).

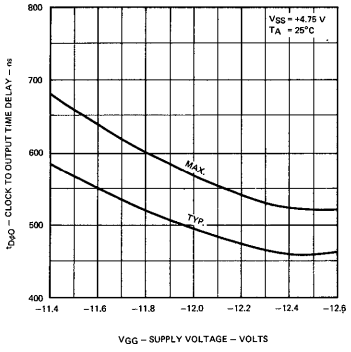
CHARACTER ADDRESS TO OUTPUT ACCESS TIME VERSUS SUPPLY VOLTAGE



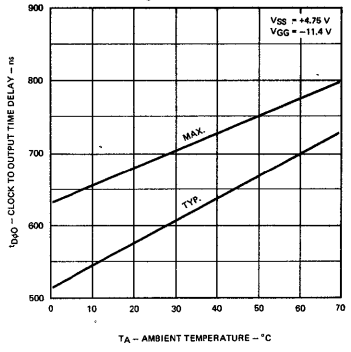
CHARACTER ADDRESS TO OUTPUT ACCESS TIME VERSUS AMBIENT TEMPERATURE



CLOCK TO OUTPUT TIME DELAY VERSUS SUPPLY VOLTAGE



CLOCK TO OUTPUT TIME DELAY VERSUS AMBIENT TEMPERATURE



TIMING DIAGRAM

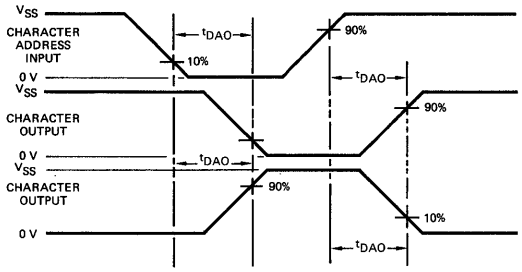


Fig. 1

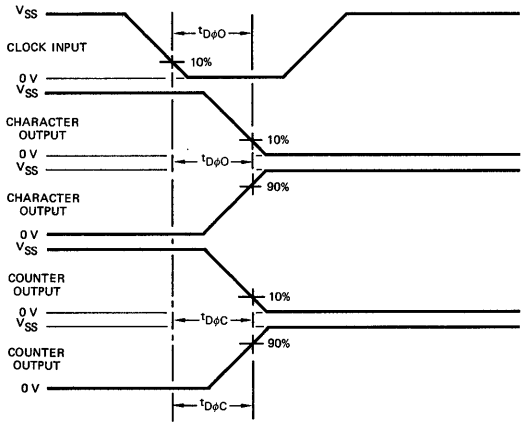


Fig. 2

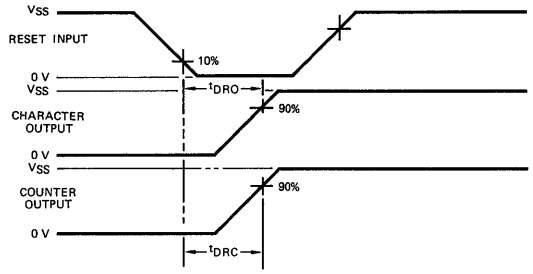


Fig. 3

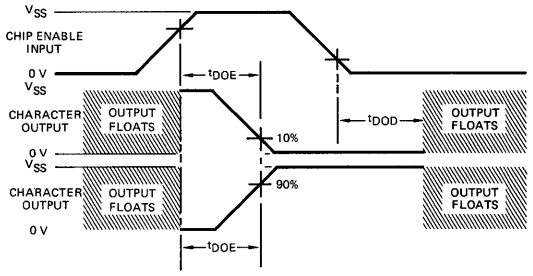


Fig. 4

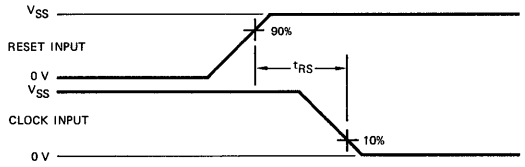


Fig. 5

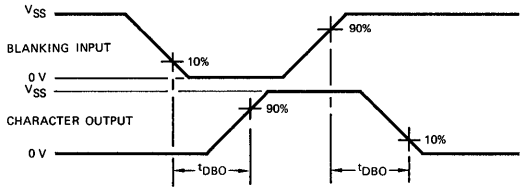
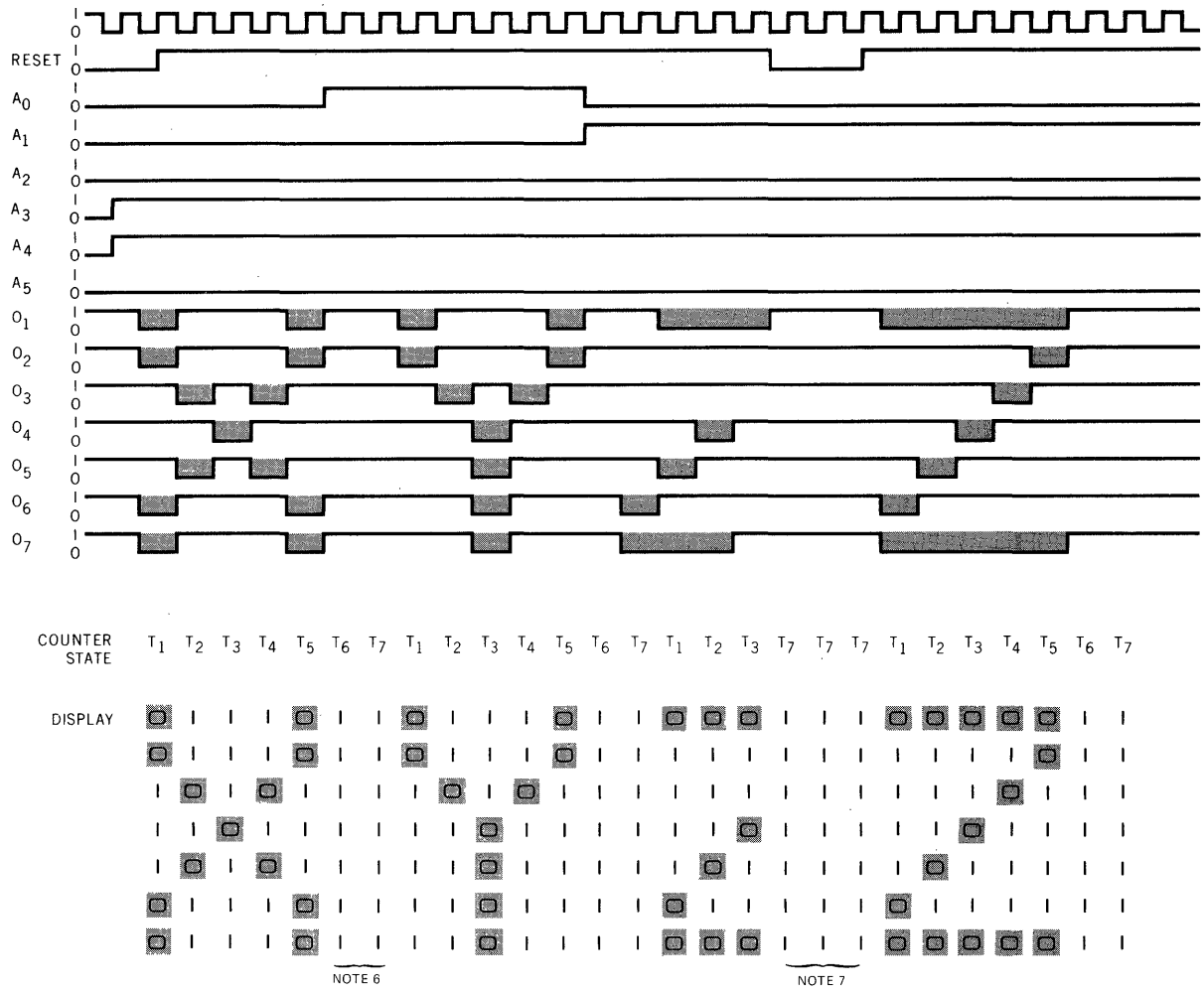


Fig. 6

GLOSSARY OF TERMS

1.	V_{SS}	The most positive voltage applied to the device.
2.	V_{GG}	The most negative voltage applied to the device
3.	V_{DD}	The next most negative voltage applied to the device.
4.	t_{RS}	Reset to clock set up time — reset must return to a logical HIGH within the period t_{RS}, before a positive to negative clock transition to insure character output levels during that clock time.
5.	t_{DAO}	Time for a character output to change logic levels after a character input changes logic levels.
6.	$t_{D\phi O}$	Time for a character output to change logic levels after the clock input reaches a logic LOW level.
7.	t_{DRO}	Time for a character output to reach a logic HIGH after reset reaches a logic LOW.
8.	t_{DBO}	Time for a character output to change logic levels after the blanking input changes logic levels.
9.	$t_{D\phi C}$	Time for the counter output to change logic levels after the clock input reaches a logic LOW level.
10.	t_{DRC}	Time for the counter output to reach a logic HIGH level after the reset input reaches a logic LOW level.
11.	t_{DOE}	Time before information is available at the character outputs after the chip enable input reaches a logic HIGH level.
12.	t_{DOD}	Time before the character outputs are disabled after the chip enable input reaches a logic LOW level.

TYPICAL FUNCTIONAL TIMING DIAGRAM



NOTES:
6. Last two counter states (count mode control = HIGH ⇒ MOD 7) provide blanking.
7. Counter is Reset to the last state.

Fig. 7

INTERFACING

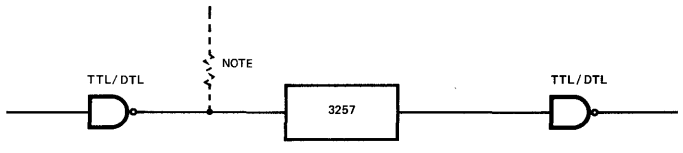
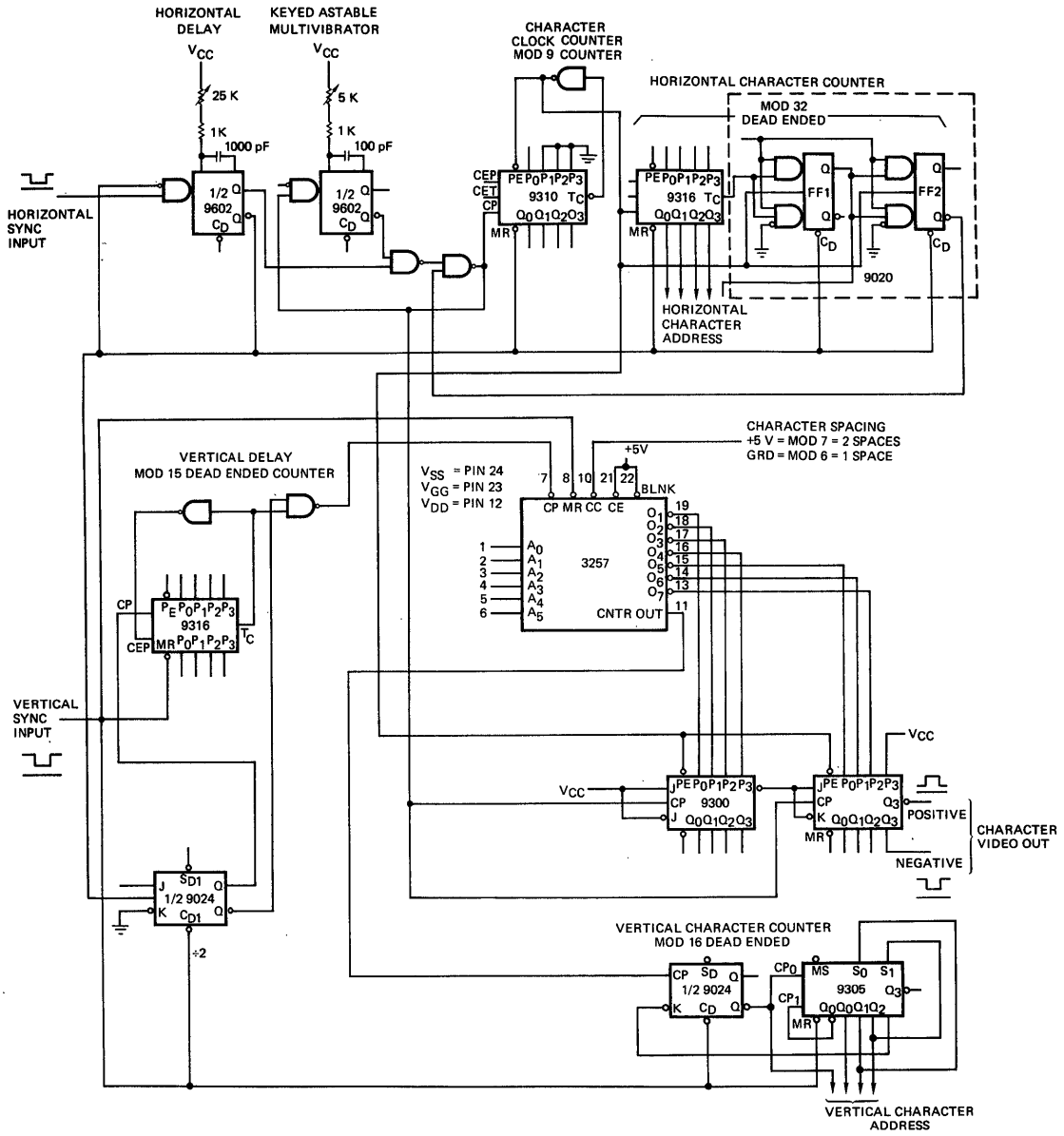


Fig. 8

Note: Directly compatible at outputs with TTL/DTL. Inputs directly compatible with DTL. When being driven by TTL, no pullup resistor needed if TTL output swings to (V_{SS} −1) volts.



NOTE:
Horizontal and vertical are referred to as in a standard TV type raster.
16 characters per line, 32 character lines in system.
Each character 10 raster lines wide.

Fig. 9 TYPICAL VERTICAL RASTER SCAN APPLICATION

CUSTOM FONT

ORDERING INFORMATION

Additional patterns may be made available upon request. The 3257 is programmed on IBM cards or IBM forms in the coding format shown below:

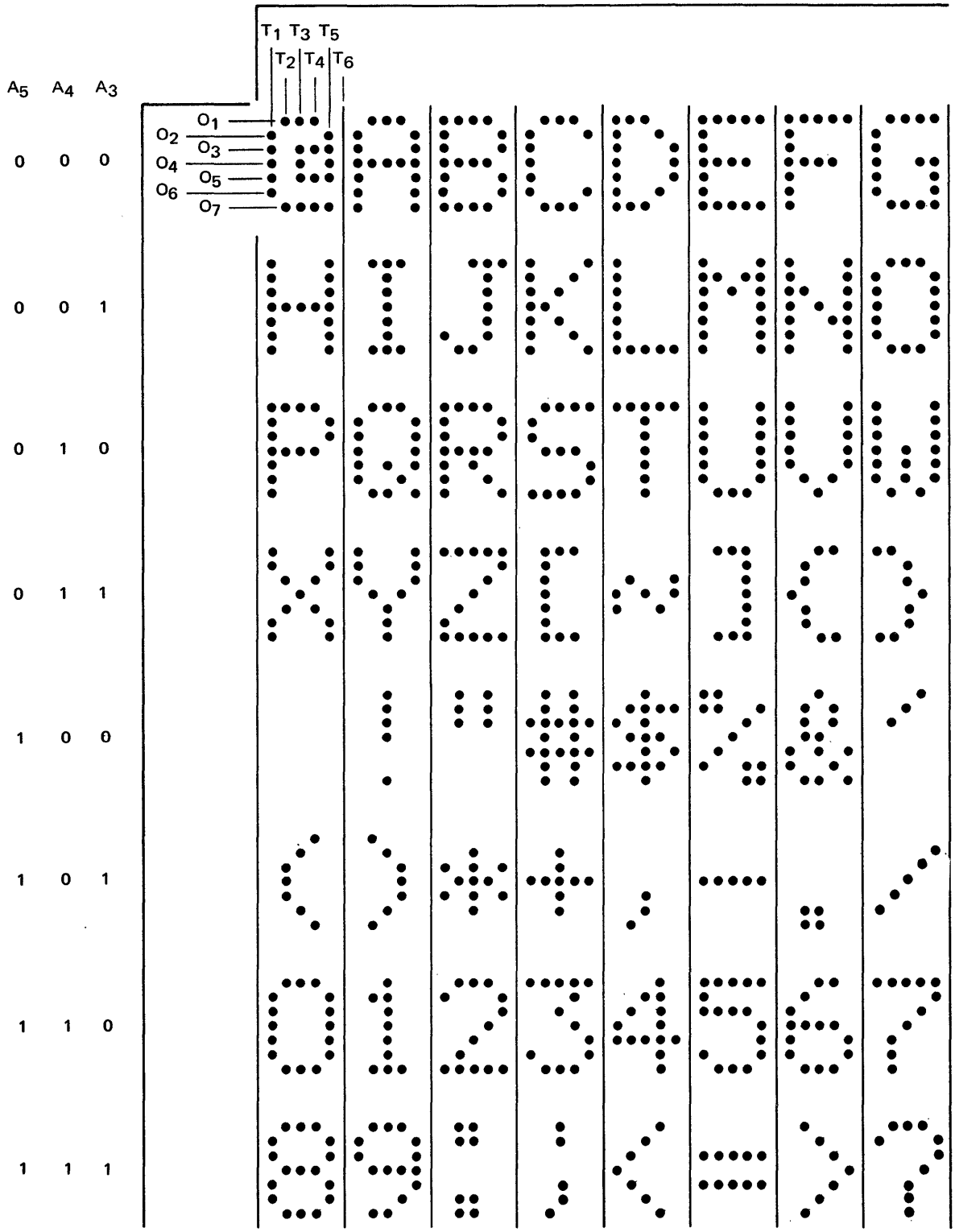
A logic "1" = A more positive voltage nominally +5 V
A logic "0" = A more negative voltage nominally 0 V
The character "dots" are defined as logic "0"

6, 7, 8, 9, 10, 11	Character address input code. The most significant bit (A5) is in column 11.
22, 23, 24, 25, 26, 27, 28	The first column of the character addressed. The most significant bit (07) is in Column 28.
30, 31, 32, 33, 34, 35, 36	The next column of the character addressed. The most significant bit (07) is in Column 36.
38, 39, 40, 41, 42, 43, 44	The next column of the character addressed. The most significant bit (07) is in Column 44.
46, 47, 48, 49, 50, 51, 52	The next column of the character addressed. The most significant bit (07) is in Column 52.
54, 55, 56, 57, 58, 59, 60	The last column of the character addressed. The most significant bit (07) is in Column 60.
73, 74, 75, 76, 77, 78, 79, 80	Coding these columns is not essential and may be used for card identification purpose.

3257A – STANDARD ASCII CHARACTER FONT

COUNT MODE CONTROL ≅ GND ⇒ MOD 6

A_0	0	1	0	1	0	1	0	1
A_1	0	0	1	1	0	0	1	1
A_2	0	0	0	0	1	1	1	1



NOTE: Order 3257ADC for character font shown.

3258

DOT MATRIX CHARACTER GENERATOR

64 CHARACTERS 5 × 7 BITS
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3258 is a Character Generator designed to display 64 characters in a 5 x 7 dot matrix. An on chip row select counter sequences through the seven rows of each character. The five output buffers will each drive one TTL/DTL load directly at a 1.6 MHz input address rate making the 3258 an ideal device for CRT displays. Special input amplifiers on the Clock, Master Reset, and Address lines have eliminated the need for pull up resistors and allow direct operation at TTL/DTL logic levels.

- **PROGRAMMABLE WITH A CUSTOM CHARACTER FONT**
- **500 ns TYPICAL ACCESS TIME**
- **STANDARD PRODUCT ASCII ENCODED**
- **16-LEAD DUAL IN-LINE PACKAGE**
- **DIRECT TTL/DTL INTERFACE AT INPUTS AND OUTPUTS**
- **ON CHIP ROW SELECT COUNTER**

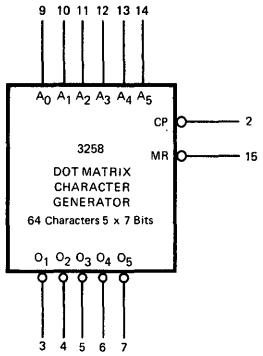
ABSOLUTE MAXIMUM RATINGS – (Above which useful life may be impaired)

Storage Temperature T_S	−65° to +150°C
Operating Temperature T_A	0°C to +70°C
Voltage on any Pin Relative to V_{SS}	−20 V to +0.3 V

APPLICATIONS:

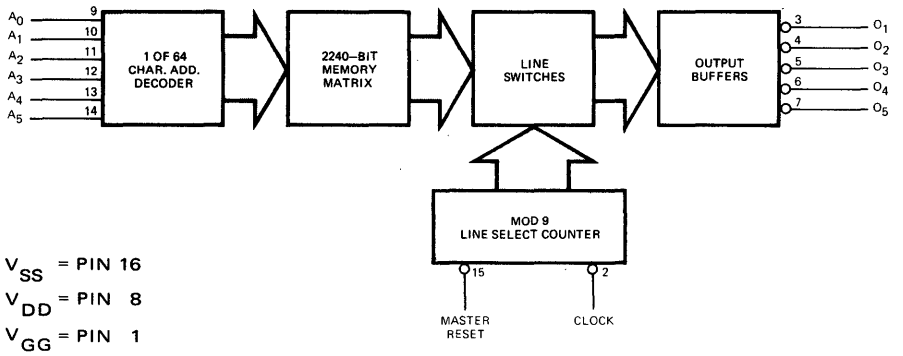
CRT Displays
Billboard Displays
LED Matrix Displays

LOGIC SYMBOL



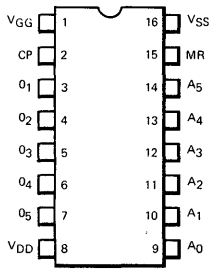
V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

LOGIC BLOCK DIAGRAM



V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION – A Master Reset pulse (≅ GND) is required to set the Modulo 9 counter to the first state. A 6-bit binary word present at the address inputs is decoded to select 1 of 64 characters in the memory. Information, representing the first row of the character, will be available at the five outputs the next clock time after the Master Reset goes HIGH (≅ V_{SS}). The next six rows of the character are sequentially selected by the counter. The last state of the counter, like the first state, clamps the outputs HIGH (≅ V_{SS}) which provides 2-space blanking between lines. The counter dead ends at the last state and the outputs will remain HIGH (≅ V_{SS}) providing blanking, until another Master Reset pulse is provided.

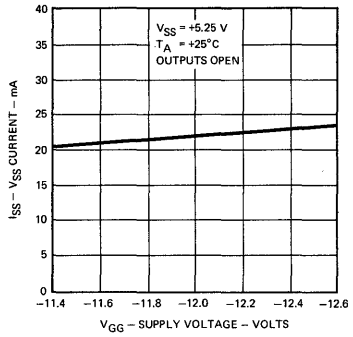
DC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0°C to 70°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS} −2.75		V_{SS}	V	Note 1
V_{IL}	Input Voltage LOW	V_{GG}	0	0.55	V	Note 1
V_{OH}	Output Voltage HIGH	2.4	3.5	V_{SS}	V	I_{OH} = −0.5 mA
V_{OL}	Output Voltage LOW	0	0.3	0.4	V	I_{OL} = 2.4 mA
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = −13 V (Note 1)
I_{SS}	V_{SS} Current		23	28	mA	V_{SS} = +5.25 V, V_{GG} = −12.6 V Outputs Open
I_{GG}	V_{GG} Current		−23	−28	mA	V_{SS} = +5.25 V, V_{GG} = −12.6 V Outputs Open
P_D	Power Dissipation		410	500	mW	

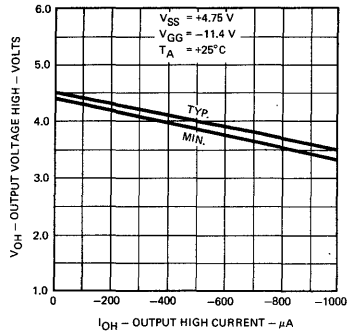
NOTE 1: Inputs include Character Address, Count Control, Clock, and Master Reset.

TYPICAL ELECTRICAL CHARACTERISTICS

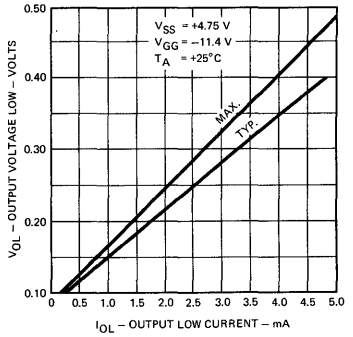
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



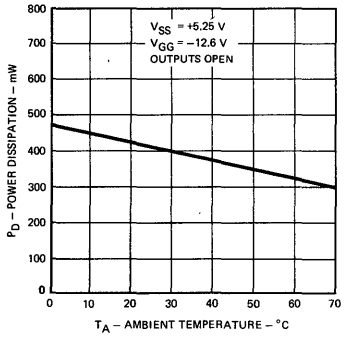
OUTPUT VOLTAGE HIGH VERSUS OUTPUT HIGH CURRENT



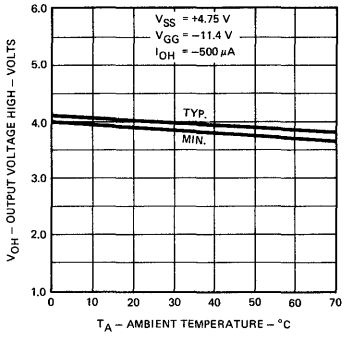
OUTPUT VOLTAGE LOW VERSUS OUTPUT LOW CURRENT



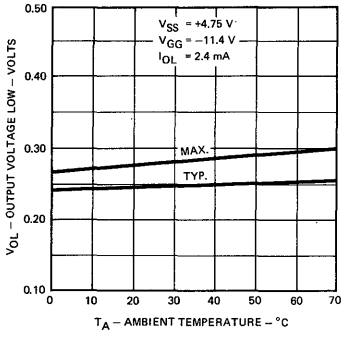
POWER DISSIPATION VERSUS TEMPERATURE



OUTPUT VOLTAGE HIGH VERSUS TEMPERATURE



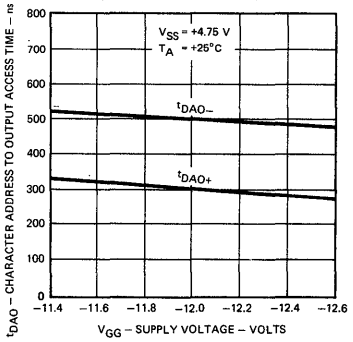
OUTPUT VOLTAGE LOW VERSUS TEMPERATURE



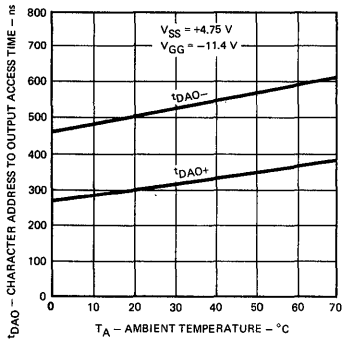
AC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, C_L = 10 pF, T_A = 0°C to +70°C.

SYMBOL	CHARACTERISTIC		MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Clock Frequency		0		500	kHz	
$t_{\phi W}$	Clock Pulse Width		1.0			μs	
t_r, t_f	Clock Rise and Fall Time				2.0	μs	
t_{RW}	Reset Pulse Width		500			ns	
t_{CRD}	Clock to Reset Time Delay		200			ns	
t_{AO}	Character Address to Output Time Delay	3258A			625	ns	Figure 1 & 2
		3258B			695	ns	
		3258C			780	ns	
		3258D			1	μs	
t_{CO}	Clock to Output Time Delay				2.0	μs	Figure 1 & 3
t_{RO}	Reset to Output Time Delay				2.0	μs	Figure 1 & 4

CHARACTER ADDRESS TO OUTPUT ACCESS TIME VERSUS SUPPLY VOLTAGE



CHARACTER ADDRESS TO OUTPUT ACCESS TIME VERSUS AMBIENT TEMPERATURE



ACCESS TIME TEST CIRCUIT

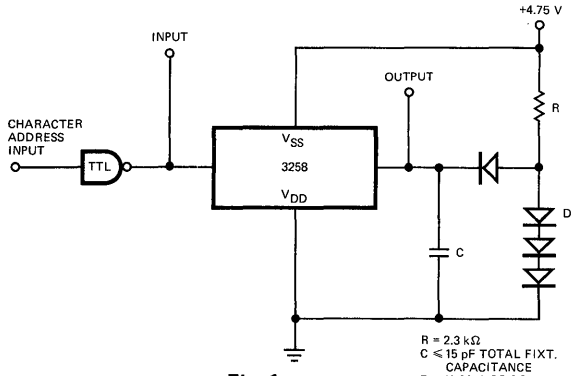


Fig. 1

TIMING DIAGRAMS

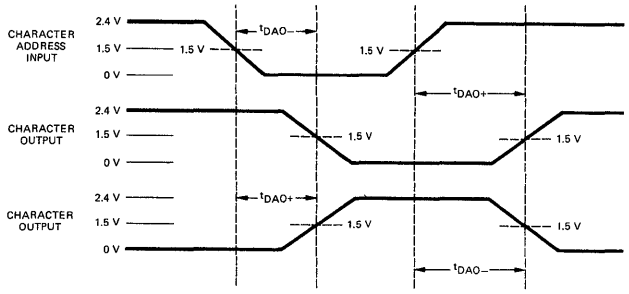


Fig. 2

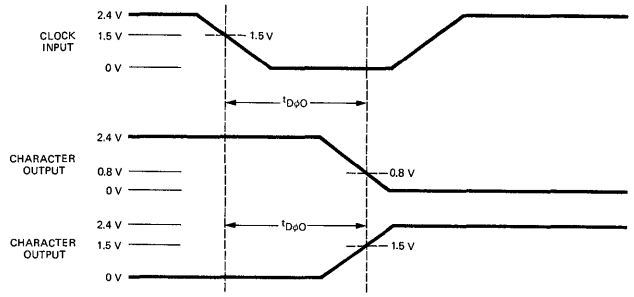


Fig. 3

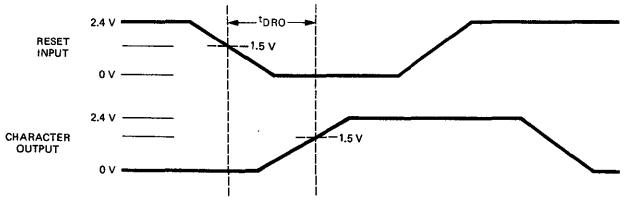
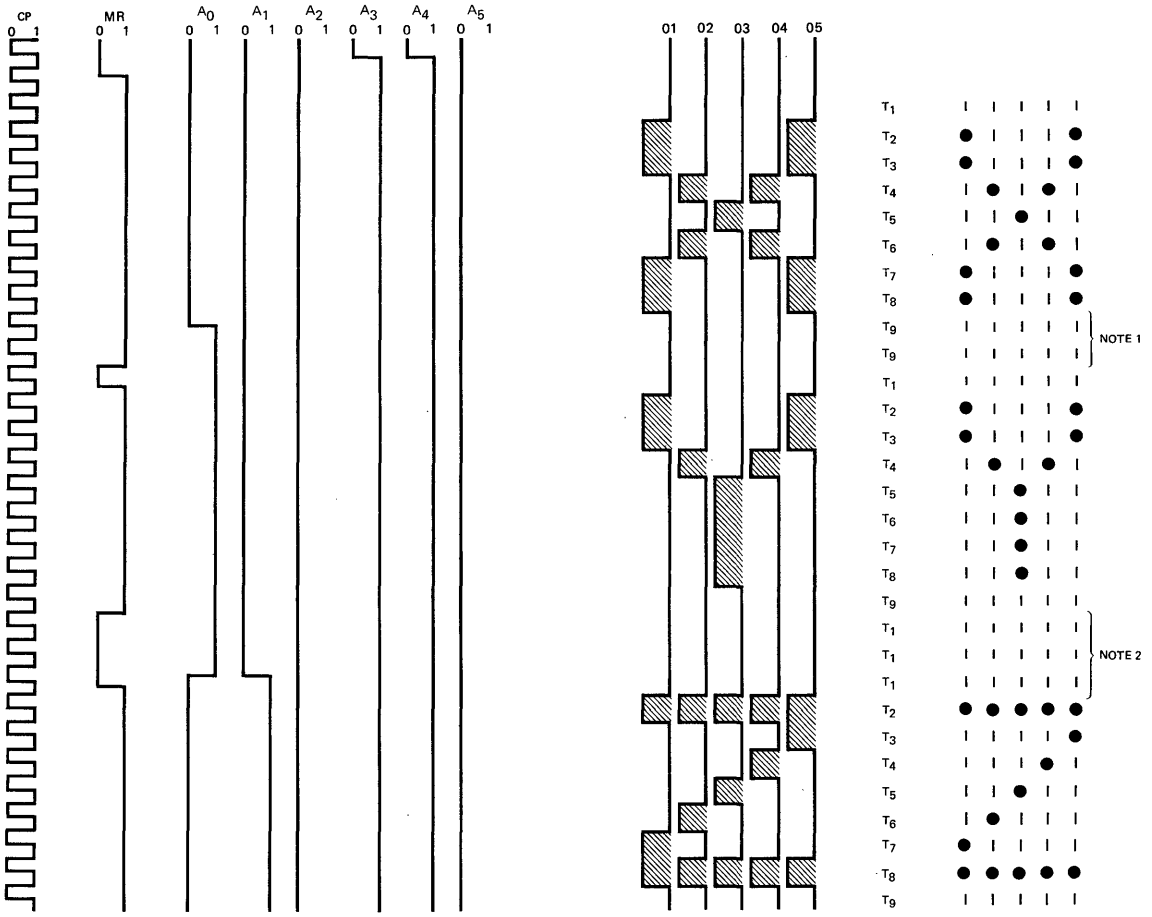


Fig. 4

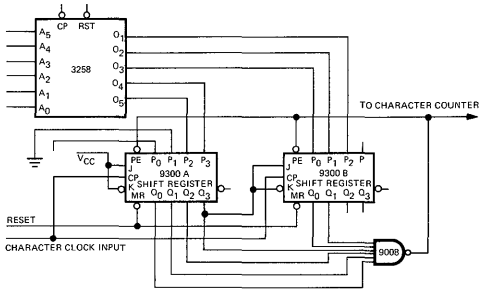
GLOSSARY OF TERMS

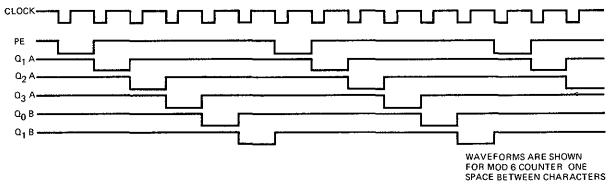
1. V_{SS} — The most positive voltage applied to the device.
2. V_{GG} — The most negative voltage applied to the device.
3. V_{DD} — The next most negative voltage applied to the device.
4. t_{RS} — To reset clock set up time — reset must return to a logical HIGH within the period t_{RS}, before a positive to negative clock transition to insure character output levels during that clock time.
5. t_{DAO} — Time for a character output to change logic levels after a character input changes logic levels.
6. $t_{D\phi O}$ — Time for a character output to change logic levels after the clock input reaches a logic LOW level.
7. t_{DRO} — Time for a character output to reach a logic HIGH after reset reaches a logic LOW.

FUNCTIONAL TIMING DIAGRAM



APPLICATIONS





OPERATION:

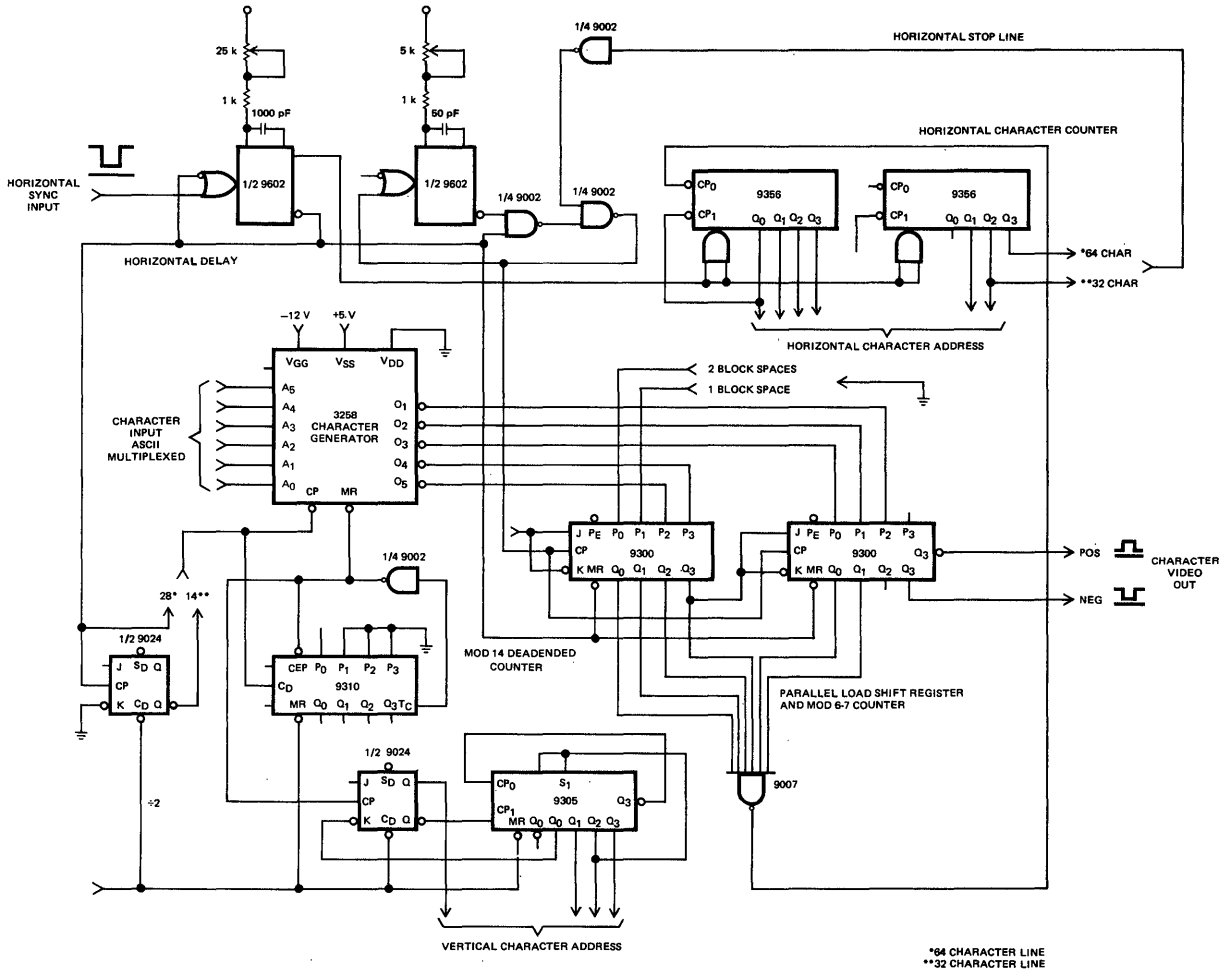
The two 9300 registers and the 9008, eight-input gate combine to form the character clock counter and the parallel to serial converter required for the outputs of the 3258 character generator.

When all the gate inputs are HIGH, the gate output is LOW which enables the parallel load (PE) of the shift registers. On the next clock pulse, positive edge after PE goes LOW, the contents of the 3258 character generator and the LOW on P_0 (A) are transferred into the registers. This LOW is shifted down the registers followed by all HIGH's from the JK input. On reaching Q_2 (B) all the outputs to the gates are once again HIGH, therefore reloading the shift registers again. The modulo count of the system can easily be changed to Modulo 7 by loading in a zero on P_0 (A).

The shift counter is reset at the beginning of each horizontal raster line to ensure that it has the correct time phase.

APPLICATIONS (cont'd)

HORIZONTAL RASTER SCAN CHARACTER GENERATOR



CUSTOM FONT

ORDERING INFORMATION

Additional character fonts are available on request. The 3258 is programmed on IBM cards or IBM coding forms in the coding format shown below:

A logic "1" = A more positive voltage nominally +5 V
A logic "0" = A more negative voltage nominally 0 V

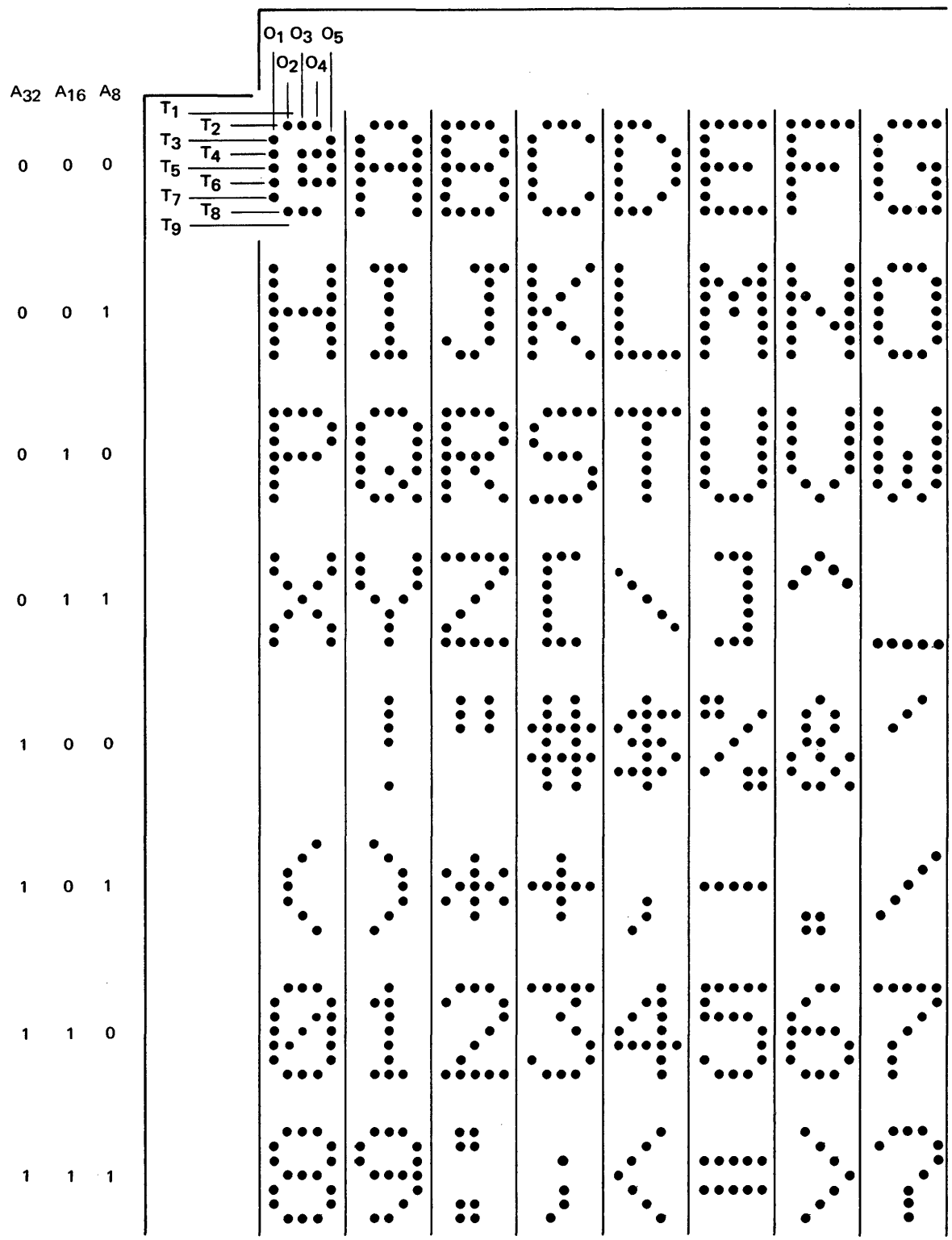
The character must be defined by a logic "0". The background by a logic "1". Each character is programmed on one IBM card or a single line on the coding form.

COLUMN NUMBER	DESCRIPTION
6,7,8,9,10,11	Character address input code. The most significant bit (A32) is in Column 11.
22,23,24,25,26	The top line of the character addressed. The most significant bit (05) is in Column 26.
28,29,30,31,32	The next line of the character addressed. The most significant bit (05) is in Column 32.
34,35,36,37,38	The next line of the character addressed. The most significant bit (05) is in Column 38.
40,41,42,43,44	The next line of the character addressed. The most significant bit (05) is in Column 44.
46,47,48,49,50	The next line of the character addressed. The most significant bit (05) is in Column 50.
52,53,54,55,56	The next line of the character addressed. The most significant bit (05) is in Column 56.
58,59,60,61,62	The bottom line of the character addressed. The most significant bit (05) is in Column 62.
73,74,75,76,77,78,79,80	Coding these columns is not essential and may be used for card identification purpose.

3258 – STANDARD ASCII CHARACTER FONT

STANDARD FONT ORDER NO.	ACCESS TIME
3258ADC	625 ns
3258BDC	695 ns
3258CDC	780 ns
3258DDC	1.0 μs

A_1	0	1	0	1	0	1	0	1
A_2	0	0	1	1	0	0	1	1
A_4	0	0	0	0	1	1	1	1



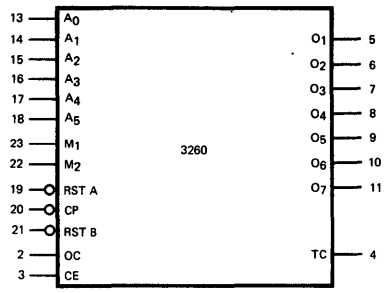
3260
DOT MATRIX CHARACTER GENERATOR
64 CHARACTERS 7×9 BITS

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3260 is a Character Generator designed to display 64 characters in a 7 x 9 dot matrix. An on chip row select counter sequences through the nine rows of each character. Each of the seven output buffers will directly drive one TTL/DTL load. A unique 2-pin programming feature is provided enabling the user (if using a 7 x 16 display matrix) to select one of four display modes: Normal, Normal with Underline, Superscript, and Subscript.

- **SUPERSCRIPT, SUBSCRIPT, & UNDERLINE CAPABILITY**
- **OUTPUT COMPLEMENT CONTROL**
- **DIRECT TTL/DTL INTERFACING**
- **3-STATE OUTPUT CAPABILITY**
- **ASCII ENCODED**

LOGIC SYMBOL



V_{SS} = PIN 24
V_{GG} = PIN 1
V_{DD} = PIN 12

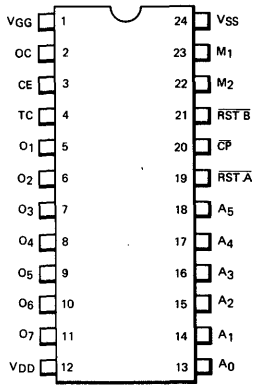
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Voltage on Any Input (V_{SS} = GND)	−20 V to +0.3 V
Voltage on V_{DD} (V_{SS} = GND)	−7 V to +0.3 V
Voltage on Outputs (V_{SS} = GND, Output Current @ +10 mA)	−7 V to +0.3 V

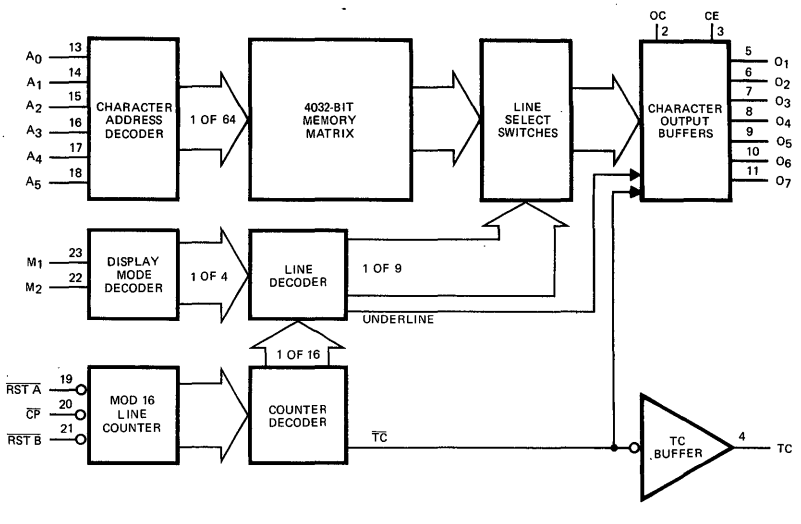
APPLICATIONS

CRT Displays
Billboard Displays

CONNECTION DIAGRAM
(TOP VIEW)



LOGIC BLOCK DIAGRAM



OPERATIONAL DESCRIPTION – A 6-bit binary word present at the address inputs ($A_1 - A_{32}$) is decoded to select one of 64 characters in the memory. Information, representing a horizontal line of the character addressed, will be available at the 7 outputs ($O_1 - O_7$) within t_{AO} after the address is present. The MOD 16 line counter sequences through the rows of the character with the application of a clock pulse (CP). A HIGH (~V_{SS}) on both RSTA and RSTB allows the counter to be free running. A LOW (~GND) on RSTA will cause the counter to dead end at T_{16} when reached. T_1 will again be reached the next clock time after RSTA returns HIGH. A LOW applied to RSTB sets the counter to T_7 independent of its previous state. This is useful when implementing a 9-line display.

To select the display mode for a specific character (this mode may be changed as often as the character address with no loss in access time), M_1 and M_2 are used. For normal operation (the character displayed during $T_4 - T_{12}$) M_1 and M_2 must both be LOW. For underline operation (character displayed during $T_4 - T_{12}$ underlline displayed during T_{14}), M_1 must be HIGH and M_2 must be LOW. For subscript operation (character displayed during $T_7 - T_{15}$), M_1 must be LOW and M_2 must be HIGH; and for superscript operation (character displayed during $T_1 - T_9$), both M_1 and M_2 must be HIGH (See Figure 1). When the counter reaches T_{16}, the Terminal Count (TC) output will go HIGH and will remain there until another counter state (T_1 or T_7) is reached, at which time TC returns LOW.

If the Output Complement (OC) pin is held HIGH, the resulting display will be a character of "0"s on a field of "1"s. A LOW on OC will produce the opposite effect.

The Chip Enable (CE) pin is provided to enable the user to common the outputs of two or more 3260's; if, for example, a 128-character font is desired.

On chip input pull up circuits will bring a normal TTL output to the desired level (at least $V_{SS}-1$ V) while the output buffers are capable of driving 1.5 TTL loads each.

DC CHARACTERISTICS: V_{SS} = +5 V ± 5%, V_{DD} = 0 V, V_{GG} = −12 V ± 5%, T_A = 0°C to +70°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	$V_{SS}-1$ V		V_{SS}	V	Note 1
V_{IL}	Input Voltage LOW	0		0.8	V	
V_{OH}	Output Voltage HIGH	2.4		V_{SS}	V	I_{OH} = 0.5 mA
		$V_{SS}-1$ V		V_{SS}	V	I_{OH} = 10 μA
V_{OL}	Output Voltage LOW	0		0.4	V	I_{OL} = 2.4 mA
I_{IH}	Input Pull-up Current HIGH	100	200		μA	$V_{IN} = V_{SS} - 1$ V
I_{IL}	Input Current LOW		390	615	μA	V_{IN} = 0 V
I_{LI}	Input Leakage Current			1.0	μA	$V_{IN} = V_{SS} - 6$ V, Note 2
I_{LO}	Character Output Leakage Current			1.0	μA	$V_{OUT} = V_{SS} - 6$ V, Note 3
I_{DD}	V_{DD} Current		24	36	mW	CE = Disable Code
I_{GG}	V_{GG} Current		15	24	mA	Outputs disabled
I_{SS}	V_{SS} Current		54	68	mA	Outputs Open
P_D	Power Dissipation		450	660	mW	Remaining Inputs = 0 V

NOTES:
1. Input pull up resistors to V_{SS} are provided on all inputs. The minimum V_{IH} is the level the resistors will pull a TTL input high voltage with 100 μA into the TTL output.
2. All pins at V_{SS} except pin under test.
3. Character outputs disabled. TC output is not three state.

3260 DISPLAY MODE TRUTH TABLE

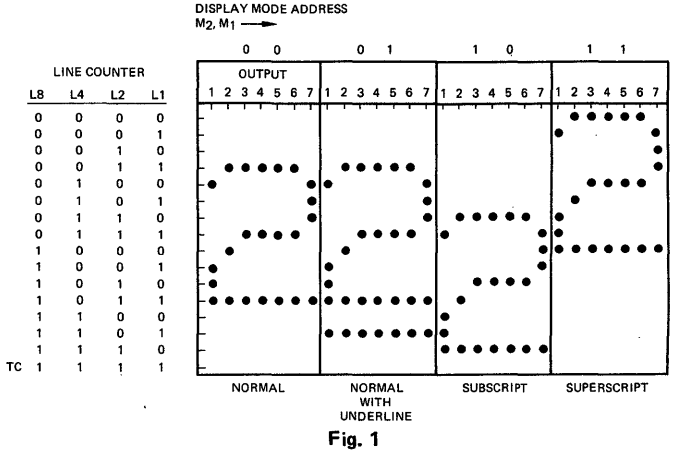
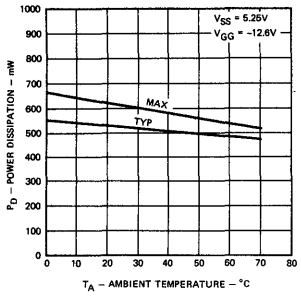


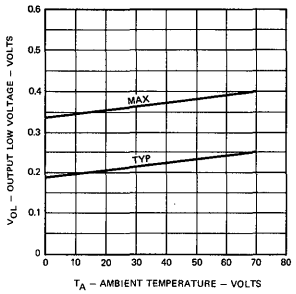
Fig. 1

ELECTRICAL CHARACTERISTICS

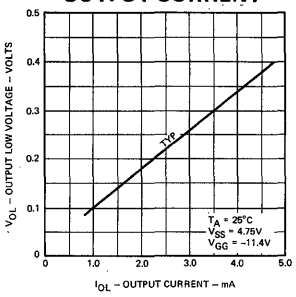
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



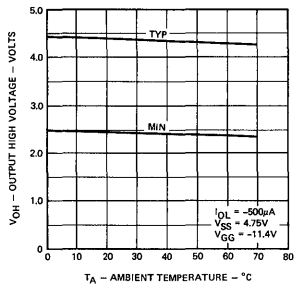
OUTPUT VOLTAGE LOW VERSUS AMBIENT TEMPERATURE



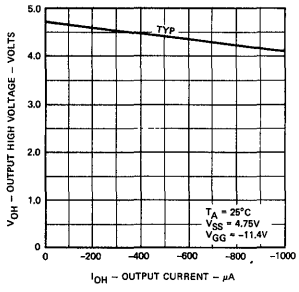
OUTPUT VOLTAGE LOW VERSUS OUTPUT CURRENT



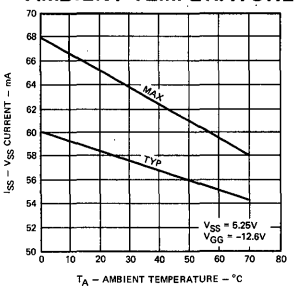
OUTPUT VOLTAGE HIGH VERSUS AMBIENT TEMPERATURE



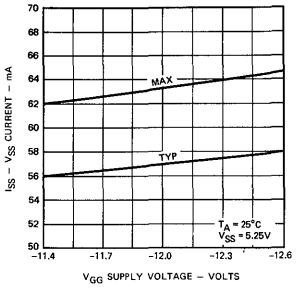
OUTPUT VOLTAGE HIGH VERSUS OUTPUT CURRENT



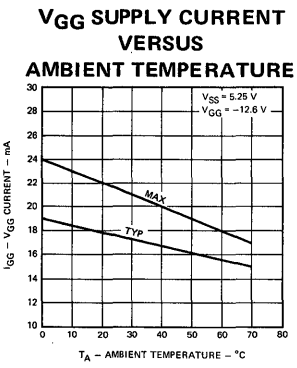
V_{SS} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



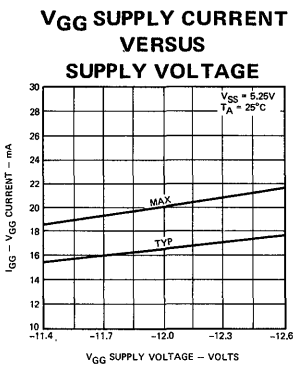
V_{SS} SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



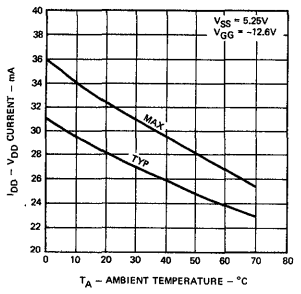
V_{GG} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



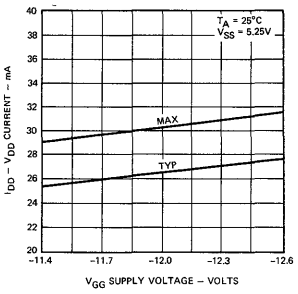
V_{GG} SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



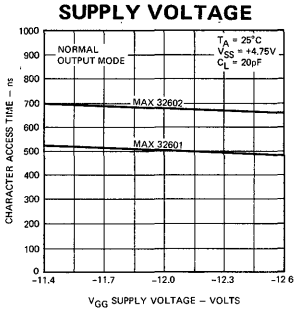
V_{DD} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



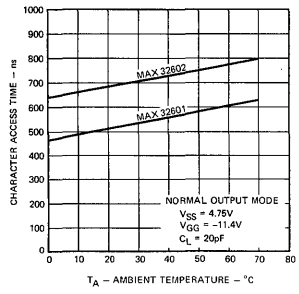
V_{DD} SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



CHARACTER ACCESS TIME VERSUS SUPPLY VOLTAGE



CHARACTER ACCESS TIME VERSUS AMBIENT TEMPERATURE



AC CHARACTERISTICS: V_{SS} = +5 V ± 5%, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, T_A = 0°C to 70°C, C_L = 20 pF (Fig. 9)

SYMBOL		MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Clock Frequency	0		250	kHz	
$t_{PW\phi}$	Clock Pulse Width	2.0			μs	Fig. 2
t_r, t_f	Clock Rise and Fall Time			2.0	μs	10% to 90% Points
t_{PWR}	Reset Pulse Width	2.0			μs	Fig. 3
t_{RS}	Reset to Clock Set-up Time Delay	500			ns	Fig. 4
t_{DAO}	Character Address to Character Output Time Delay					
	3260A	200		625	ns	Fig. 5, Note 1
	3260B	200		800	ns	
t_{DMO}	Display Mode Address to Character Output Time Delay					
	3260A	200		625	ns	Fig. 6, Note 1
	3260B	200		800	ns	
t_{DCO}	Output Control to Character Output Time Delay					
	3260A	200		625	ns	Fig. 7, Note 1
	3260B	200		800	ns	
t_E	Character Output Enable Time Delay					
	3260A			625	ns	Fig. 8, Note 1
	3260B			800	ns	
$t_{\overline{E}}$	Character Output Disable Time Delay					
	3260A			625	ns	Fig. 8, Note 1
	3260B			800	ns	
$t_{D\phi O}$	Clock to Output Time Delay			2.0	μs	Fig. 2
$t_{D\phi T}$	Clock to Terminal Count Output Time Delay			2.0	μs	Fig. 2
t_{DRO}	Reset "B" to Character Output Time Delay			2.0	μs	Fig. 3
C_I	Input Capacitance			8.0	pF	f = 1 MHz, 0 V Bias
C_O	Output Capacitance			10	pF	f = 1 MHz, 0 V Bias

Note 1: Output complement input a logic "1", add 150 ns to access time for complement.

TIMING DIAGRAMS

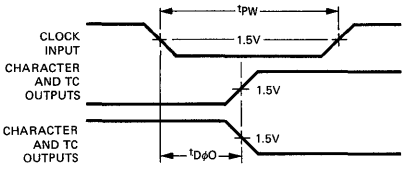


Fig. 2

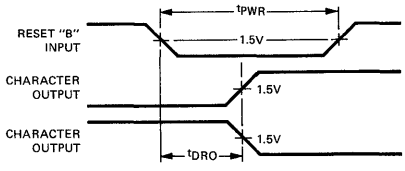


Fig. 3

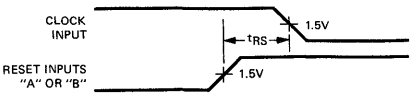


Fig. 4

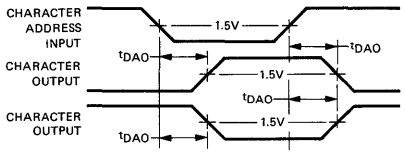


Fig. 5

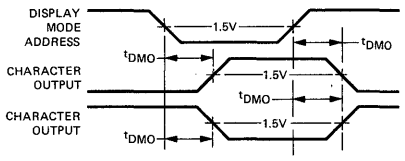


Fig. 6

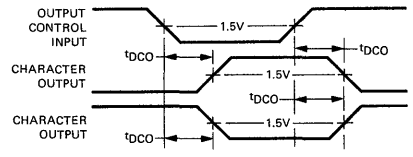


Fig. 7

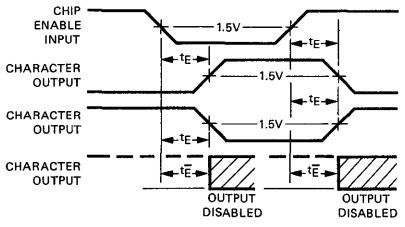


Fig. 8

SWITCHING TIME TEST CIRCUIT

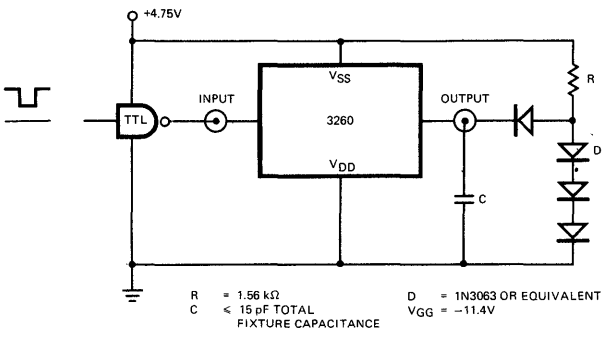


Fig. 9

FUNCTIONAL TIMING DIAGRAM

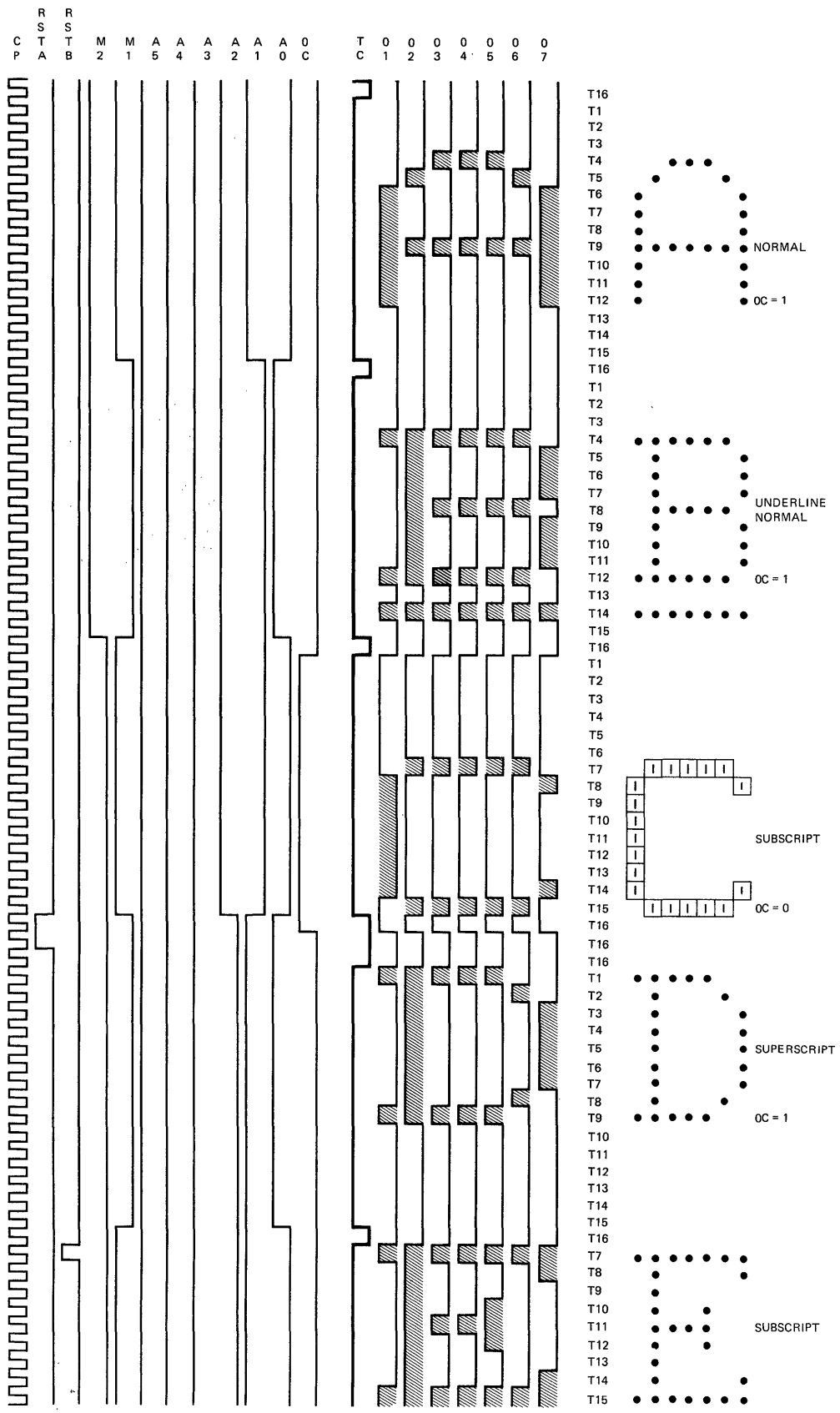
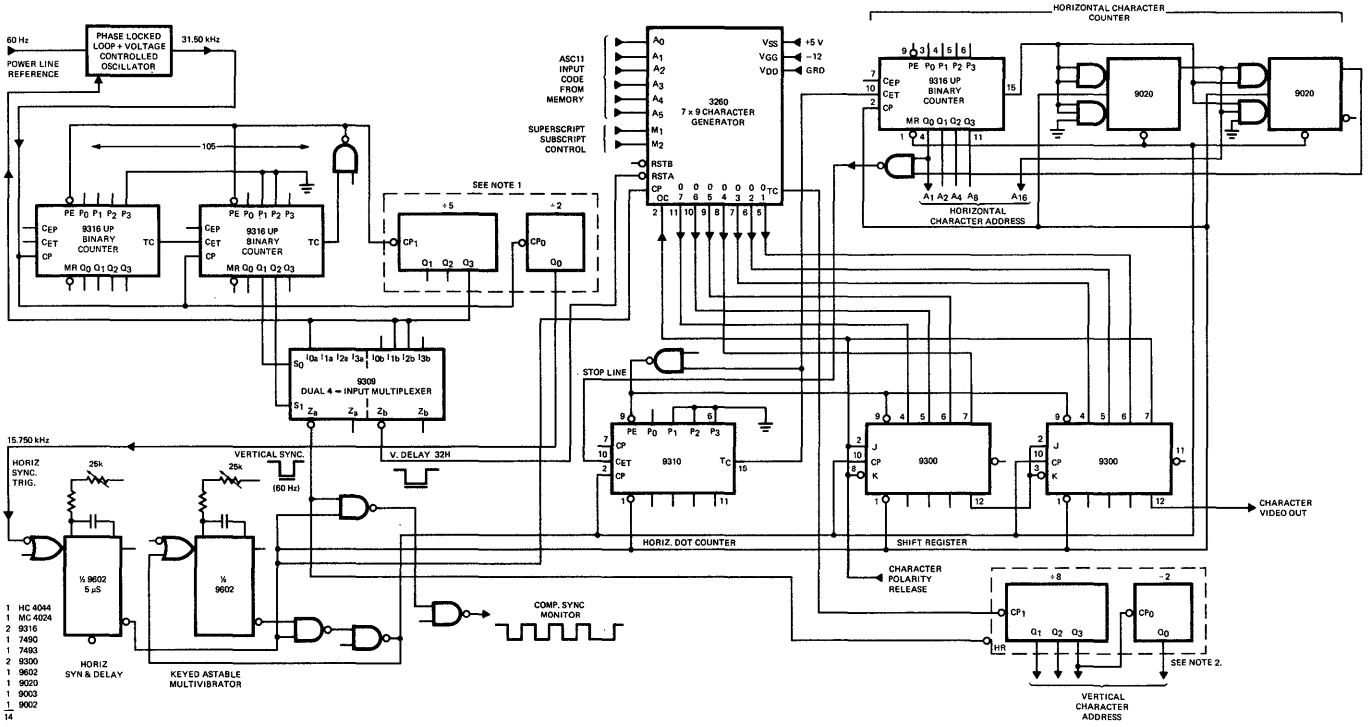


Fig. 10

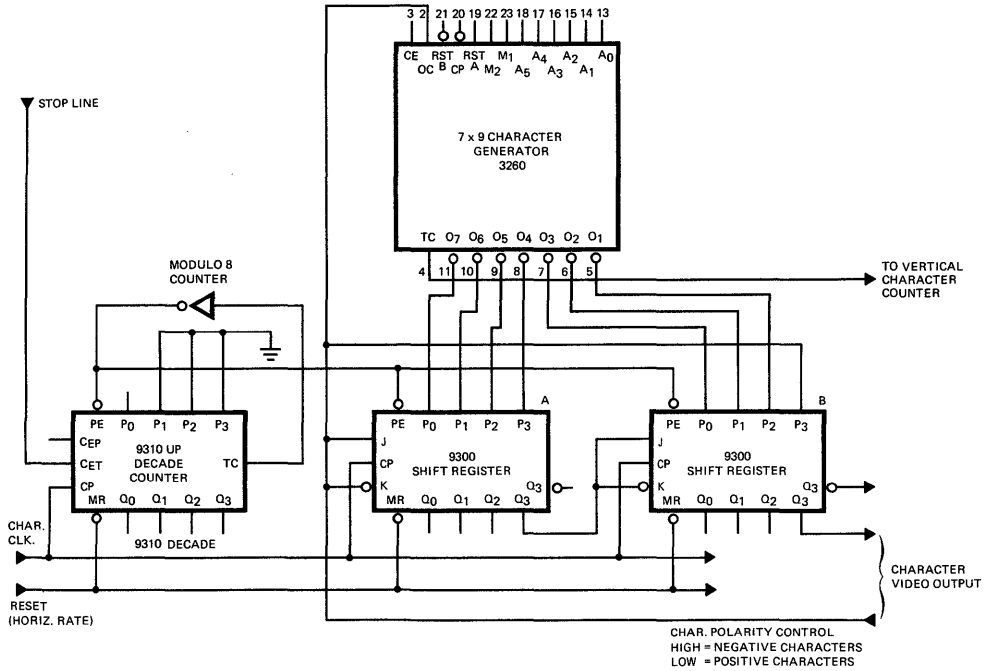
APPLICATIONS

CRT CHARACTER GENERATOR USING 7x9 DOT MATRIX CHARACTER GENERATOR (CIRCUIT INCLUDES 525 SYNC GENERATOR, NON EIA)



NOTES:

1. CAN BE EITHER 7490/9390 OR 9350 DECADE COUNTER OR 9305 VARIABLE MOD COUNTER.
2. CAN BE EITHER 7493/9393 OR 9392 (REQUIRED INVERSION FOR MR) BINARY COUNTER OR 9305 VARIABLE MOD. COUNTER.



OPERATION

Serial to parallel operation can be performed with two 9300 shift registers and a 9310 decade counter with feedback for modulo 9 count. This provides one space before and after the seven horizontal dots. The inverted terminal count output of the 9310 is LOW for one clock pulse out of every nine, thus parallel loading both 9300's with character data and loading itself with a BCD one (0001). By controlling the JK 9300 P3 9300 and OC 3260 horizontal framing can be provided.

GLOSSARY OF TERMS

1. V_{SS} The most positive voltage applied to the device, nominally +5 V.
2. V_{GG} The most negative voltage applied to the device, nominally −12 V.
3. V_{DD} The next most negative voltage applied to the device, nominally 0.
4. I_{IH} Current out of input at $V_{IN} = V_{SS} - 1$ V.
5. I_{IL} Current out of input at $V_{IN} = 0$ V.
6. I_{OH} Current out of output.
7. I_{OL} Current into output.
8. t_{DAO} Time for a character output to change logic levels after a character address input changes logic levels.
9. t_{DMO} Time for a character output to change logic levels after a display mode input changes logic levels.
10. t_{DCO} Time for a character output to change logic levels after the output control input changes logic level.
11. t_E Time before information is available at the character outputs after the chip enable input reaches the logic level required to enable the chip.
12. $t_{\bar{E}}$ Time before the character outputs are disabled after the chip enable input reaches the logic level required to disable the chip.
13. $t_{D\phi T}$ Time for the character outputs and the terminal count output to change logic levels after the clock input reaches a logic "0" level.
14. t_{DRO} Time for a character output to change logic levels after reset input "B" returns to a logic "1" level.
15. t_{RS} Reset to Clock Set Up time delay — reset "A" or "B" must not return to a logic "1" level within the period t_{RS} to assure proper character outputs during the next clock cycle.

CUSTOM FONT ORDERING INFORMATION

Custom patterns may be made available upon request. The coding format is shown below.

Specify access time desired on Purchase Order.

A Logic "1" = A more positive voltage, nominally + 5 V

A Logic "0" = A more negative voltage, nominally 0 V

Character outline dots must be programmed Logic "0", field Logic "1", for maximum access rate.

FIRST CARD:

COLUMN NUMBER	DESCRIPTION
29	Logic level at chip enable input required to enable chip.

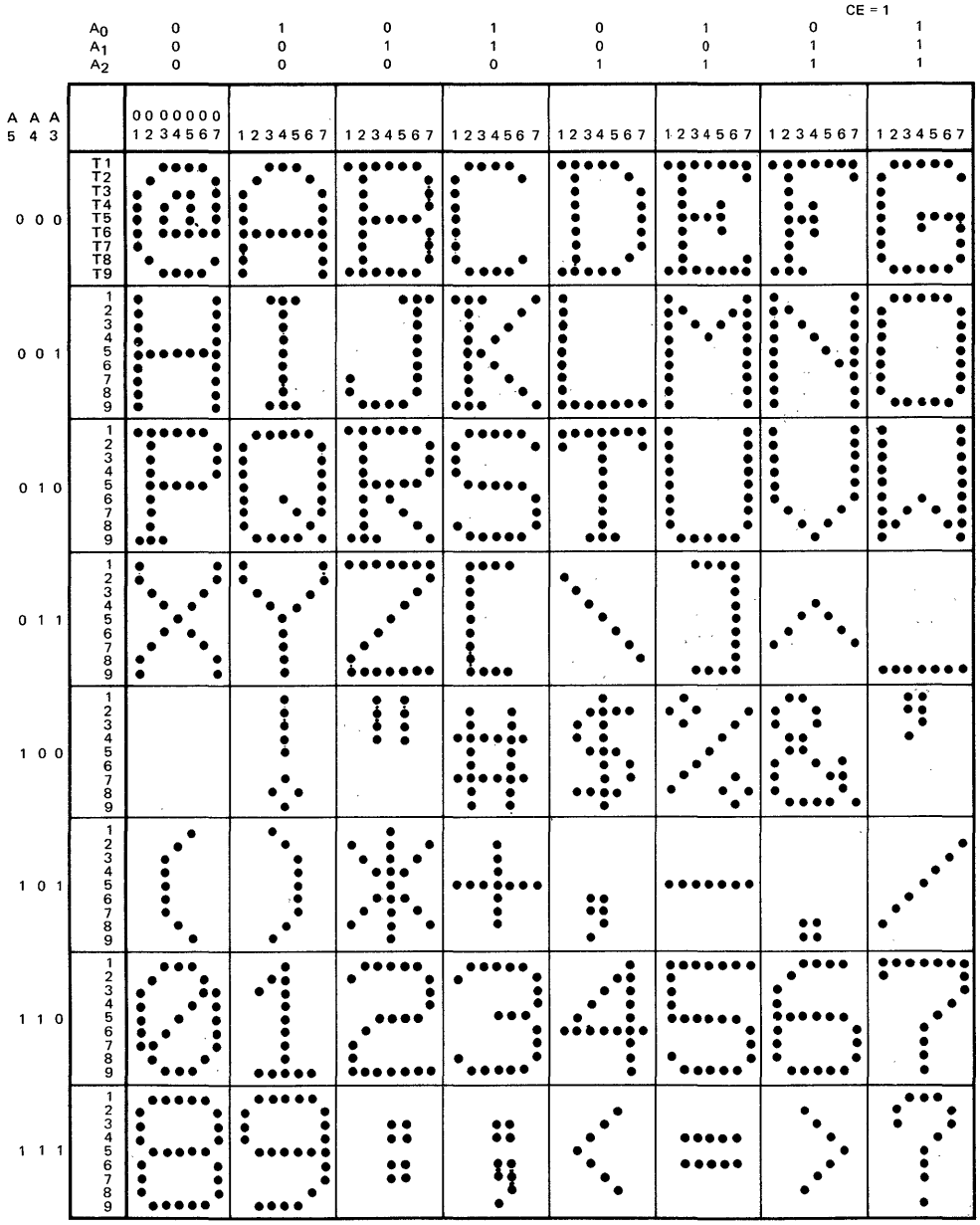
REMAINING 64 CARDS:

COLUMN NUMBER	DESCRIPTION
1, 2, 3, 4, 5, 6	Character address input code, the MSB (A5) is in Column 6.
8, 9, 10, 11, 12, 13, 14	The top line of the character addressed, the MSB O_7 is in Column 14.
15, 16, 17, 18, 19, 20, 21	The next line of the character addressed, the MSB O_7 is in Column 21.
22, 23, 24, 25, 26, 27, 28	The next line of the character addressed, the MSB O_7 is in Column 28.
29, 30, 31, 32, 33, 34, 35	The next line of the character addressed, the MSB O_7 is in Column 35.
36, 37, 38, 39, 40, 41, 42	The next line of the character addressed, the MSB O_7 is in Column 42.
43, 44, 45, 46, 47, 48, 49	The next line of the character addressed, the MSB O_7 is in Column 49.
50, 51, 52, 53, 54, 55, 56	The next line of the character addressed, the MSB O_7 is in Column 56.
57, 58, 59, 60, 61, 62, 63	The next line of the character addressed, the MSB O_7 is in Column 63.
64, 65, 66, 67, 68, 69, 70	The bottom line of the character addressed, the MSB O_7 is in Column 70.
73, 74, 75, 76, 77, 78, 79, 80	Coding these columns is not essential and may be used for card identification purpose.

EXAMPLE: Letter G

	L S B						M S B	
	0	0	0	0	0	0	0	
	1	2	3	4	5	6	7	
Top Line	1	0	0	0	0	0	1	T1
	0	1	1	1	1	1	0	T2
	0	1	1	1	1	1	1	T3
	0	1	1	1	1	1	1	T4
	0	1	1	0	0	0	0	T5
	0	1	1	0	1	1	0	T6
	0	1	1	1	1	1	0	T7
	0	1	1	1	1	1	0	T8
Bottom Line	1	0	0	0	0	0	1	T9

CHARACTER FONT



STANDARD FONT ORDER NO.	ACCESS TIME
3260 ADC	625 ns
3260 BDC	800 ns

3261
TV SYNC GENERATOR
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3261 Color Television Sync Generator provides several waveforms including all the necessary RS170 EIA standard output signals. These are the Horizontal Drive, Vertical Drive, Composite Sync, Composite Blanking, $\phi = 0°$ Color Subcarrier, Color Burst Flag, Even Field and Odd Field. All waveforms are directly decoded from a LOW voltage 2-phase clock running at 14.31818 MHz. All output buffers, except for the $\phi = 0°$ Color Subcarrier, are capable of driving a bipolar load directly without external components. The $\phi = 0°$ Color Subcarrier output is designed to drive a capacitive load. The 3261 is a monolithic integrated circuit with P-channel enhancement mode silicon gate MOS technology.

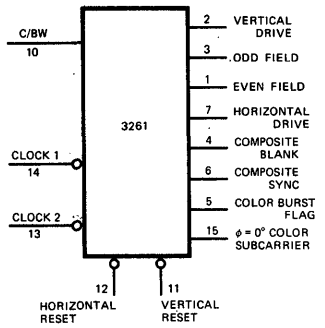
- **14.31818 MHz COLOR OPERATION —2.0475 MHz BLACK/WHITE OPERATION**
- **ALL COUNTERS SYNCHRONOUS**
- **ALL FIXED PULSE WIDTHS**
- **LOW POWER DISSIPATION**
- **DIRECT TTL COMPATIBILITY EXCEPT FOR $\phi = 0°$, $\phi = 90°$ COLOR SUBCARRIERS**
- **SEPARATE VERTICAL AND HORIZONTAL RESET CAPABILITY FOR GEN-LOCK APPLICATIONS**
- **SILICON GATE TECHNOLOGY**

ABSOLUTE MAXIMUM RATINGS

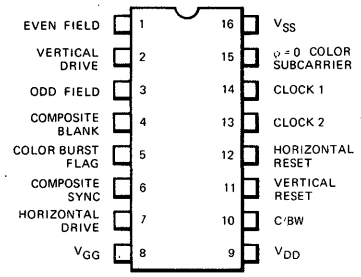
All Inputs (Note 1)	−24 V to +0.3 V
V_{GG}	−24 V to +0.3 V
V_{DD} and Outputs	−7 V to +0.3 V
DC Output Current (When Output LOW)	⩽ 10 mA
Storage Temperature	−55°C to 150°C
Operating Temperature	0°C to 70°C
Maximum Power Dissipation	750 mW

NOTES:
1. All inputs with respect to V_{SS}.

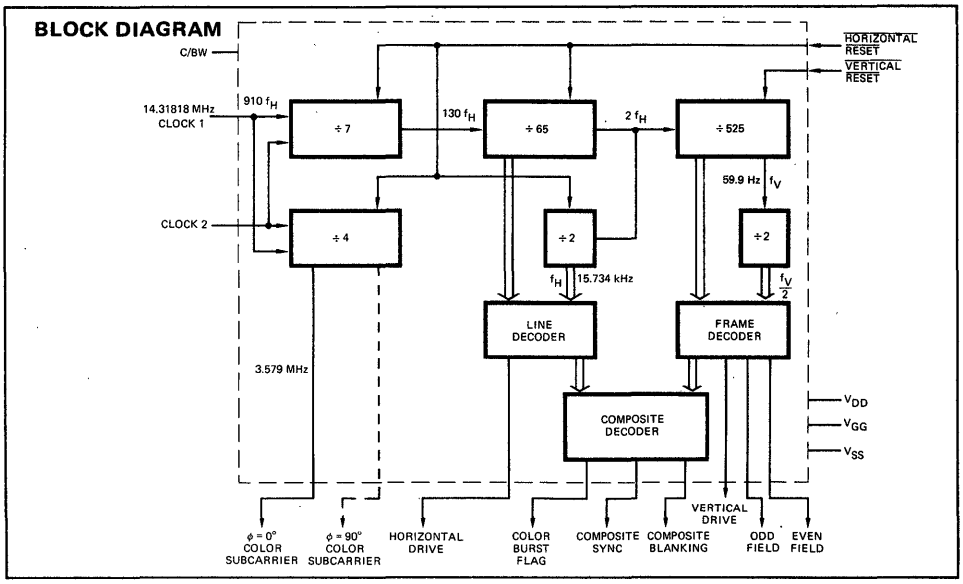
LOGIC SYMBOL



CONNECTION DIAGRAM
(TOP VIEW)



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – The 3261 block diagram shows the counting and decoding scheme used to generate all output waveforms. The clock frequency is divided down in three steps (÷7, ÷65, ÷2) and decoded to generate the horizontal drive. A signal at twice the horizontal frequency is divided by 525 to generate the vertical drive. The $\phi = 0^\circ$ Color Subcarrier is generated by a ÷4 Johnson counter driven directly from the input clock. This is a nonsinusoidal signal which can be used to generate the Color Subcarrier. Pulses at the horizontal and vertical frequencies are combined in the composite decoder to generate the Composite Sync, Composite Blanking, and Color Burst Flag.

For use in special applications, the 3261 provides a 30 Hz pulse at the start of the field (Odd Field) and again at the start of the next field (Even Field).

Separate Horizontal and Vertical Reset input pins are provided to allow the 3261 to be used in systems requiring gen-lock operation.

The C/BW input is used to select either color or black and white operation. A logic HIGH applied to C/BW will select color operation; if C/BW is LOW, the ÷7 and ÷4 counters will be bypassed for black and white operation. In addition, the only clock needed for black and white operation is Clock 1. The input frequency should be 2.0475 MHz for normal operation.

Upon special request, a $\phi = 90^\circ$ Color Subcarrier is available.

DC CHARACTERISTICS: V_{SS} = +5.5 V to +6.5 V, V_{GG} = −20.0 V to −21.0 V, V_{DD} = 0 V, T_A = 0°C to +70°C, (Note 1)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS}−1.0		V_{SS} +0.3	V	
V_{IL}	Input Voltage LOW			0.8	V	
V_{OH}	Output Voltage HIGH	2.4			V	I_{OH} = −0.1 mA
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 1.6 mA
$V_{\phi H}$	Clock Input Voltage HIGH	V_{SS}−1.0		V_{SS} +0.3	V	
$V_{\phi L}$	Clock Input Voltage LOW			0.8	V	
$V_{SUBCARRIER}$	Subcarrier Output Voltages	1.0			V	C = 10 pF
					(Peak to Peak)	R = 10 kΩ
I_{LI}	Input Leakage Current		1.0		μA	V_{IN} = 0 V
I_{DD}	V_{DD} Current		20		mA	
I_{GG}	V_{GG} Current		15		mA	
I_{SS}	V_{SS} Current		35		mA	

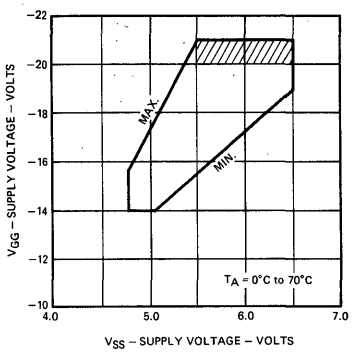
AC CHARACTERISTICS:

V_{SS} = +5.5 V to +6.5 V, V_{GG} = −20.0 V to −21.0 V, V_{DD} = 0 V, C_L = 10 pF, 1 TTL Load (1.6 mA), T_A = 0°C to +70°C, (Note 1)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Input Frequency Color			14.31818	MHz	See Fig. 3, t_r, $t_f \leq$ 5 ns
						t_{PW} = 35 ±5 ns, $t_{OV} \leq$ ± 10 ns
f_I	Input Frequency Black/White			2.0475	MHz	See Fig. 4, t_r, $t_f \leq$ 50 ns
						t_{PW1} = 250 +85 −15 ns
$t_{HR\ PW}$	Horizontal Reset Pulse Width	200			ns	t_r, $t_f \leq$ 50 ns
$t_{VR\ PW}$	Vertical Reset Pulse Width	200			ns	t_r, $t_f \leq$ 50 ns
$t_{H\ DRIVE}$	Propagation Delay From Horizontal Reset to Horizontal Drive			300	ns	
$t_{V\ DRIVE}$	Propagation Delay From Vertical Reset to Vertical Drive			300	ns	

NOTE 1. These voltage ranges may be relaxed for Black/White operation (See Fig. 1).

PERMISSIBLE OPERATING VOLTAGES



COLOR OPERATION (pin 10 = V_{SS})
32611 Cross Hatched Area

BLACK/WHITE OPERATION (pin 10 = V_{DD})
32611, 32612 } Enclosed Area

Fig. 1.

TIMING DIAGRAMS

RESET

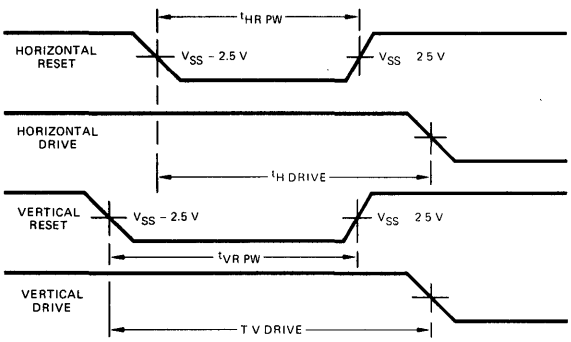


Fig. 2.

COLOR CLOCKS

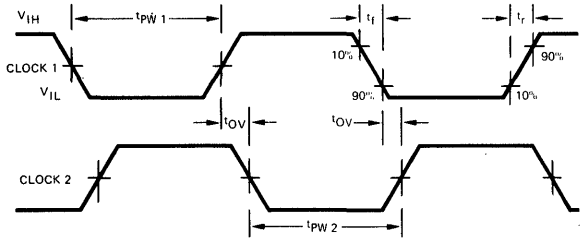


Fig. 3.

BLACK AND WHITE CLOCK

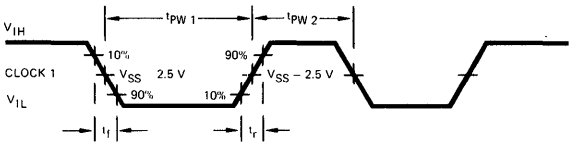


Fig. 4.

SYSTEM TIMING DETAILS

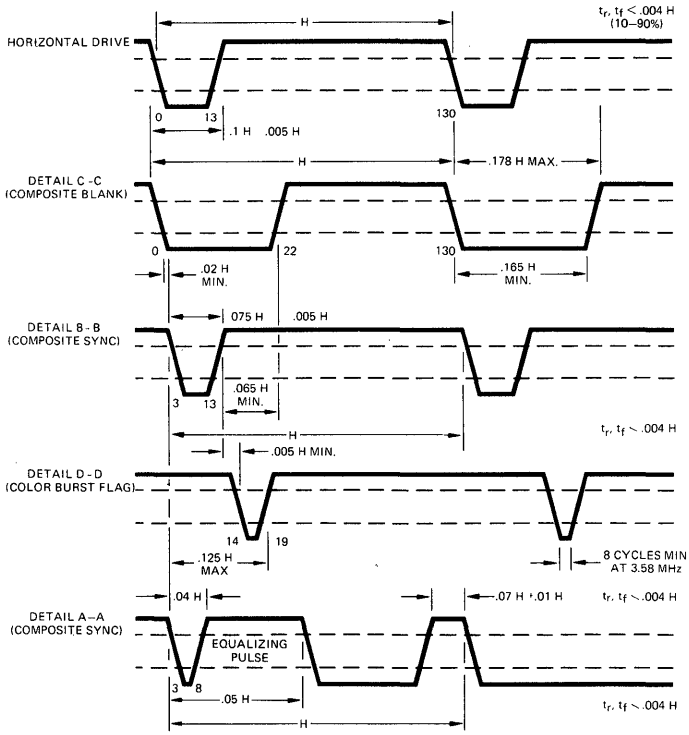


Fig. 5.

NOTE:
H = Time from start of one line to next line.
V = Time from start of one field to next field.
Leading and trailing edges of vertical blanking are complete in less than .004 H.
Equalizing pulse area is between 0.45 and 0.5 of area of horizontal sync pulse.
Numbers on waveforms show decoding edges where 1 H = 130 pulses.

R5170 EIA
SYSTEM TIMING DIAGRAM

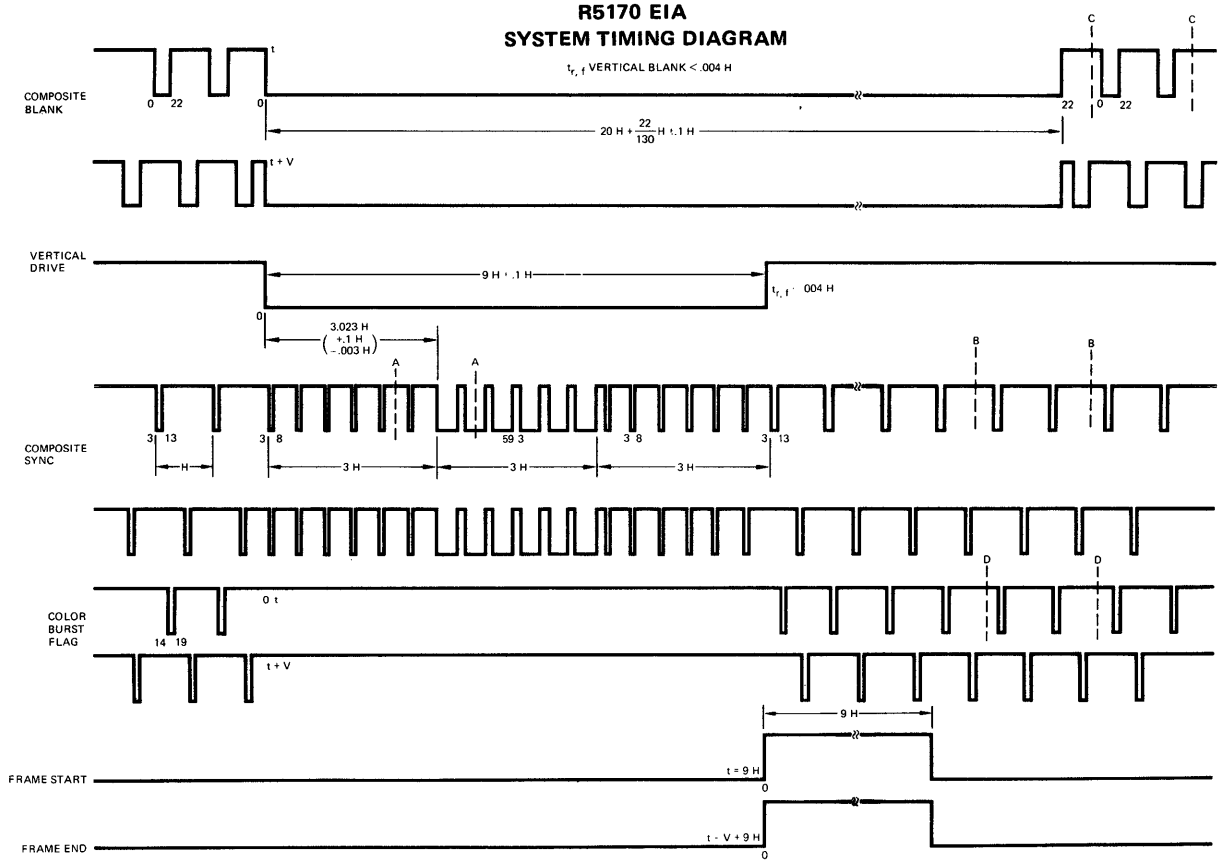


Fig. 6.

COLOR CLOCK GENERATOR CIRCUIT

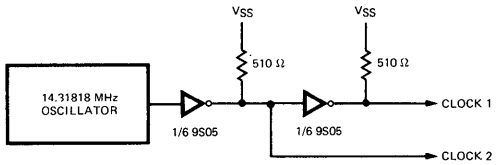


Fig. 7.

APPLICATIONS
TV SYSTEM

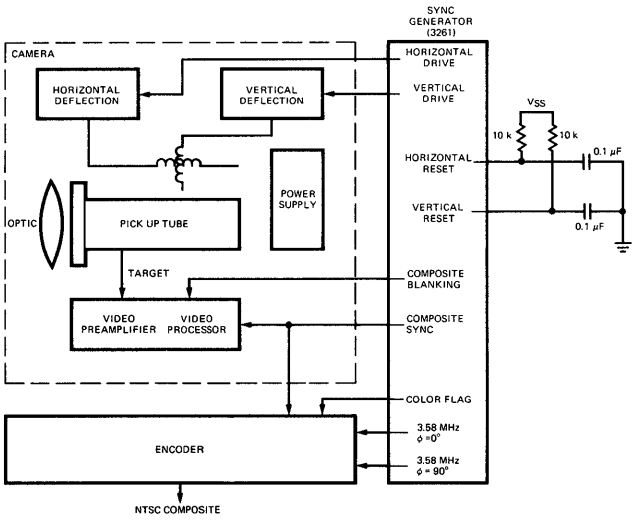


Fig. 8.

3325

QUAD 64-BIT DYNAMIC SHIFT REGISTER

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3325 contains four individual MOS 2-Phase Dynamic Shift Registers of 64-bits each. It is a monolithic P channel enhancement mode integrated circuit which is fabricated using low threshold silicon gate technology. All inputs are protected against static charge through diode protection. The 3325 is bipolar compatible and can be driven and drive bipolar integrated circuits (TTL, DDL) directly without using interface level converters.

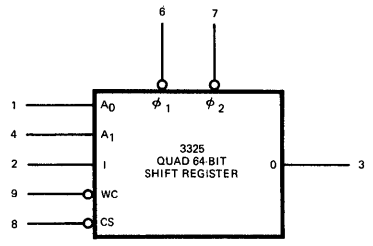
- **DIRECT BIPOLAR COMPATIBILITY**
- **35 pF TYP. CLOCKLINE CAPACITANCE**
- **0.45 mW/BIT POWER DISSIPATION (TYP. AT 30% DUTY CYCLE)**
- **COMPLETE DECODING, MULTIPLEXING, CHIP SELECTION**
- **OUTPUT PUSH/PULL CIRCUITRY**
- **INPUT OVERVOLTAGE PROTECTION**
- **10-LEAD TO-100 PACKAGE**

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired) Note 1

Supply Voltage (V_{DD})	-20 V to +0.3 V
Clock Input Voltage	-20 V to +0.3 V
All Data Input (data line, address chip select and write control) Voltages	-10 V to +0.3 V
Storage Temperature	-55°C to +150°C
Operating Temperature	-55°C to +85°C

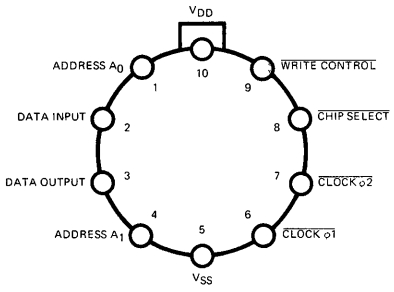
Note 1: All voltages are measured with V_{SS} @ GND.

LOGIC SYMBOL

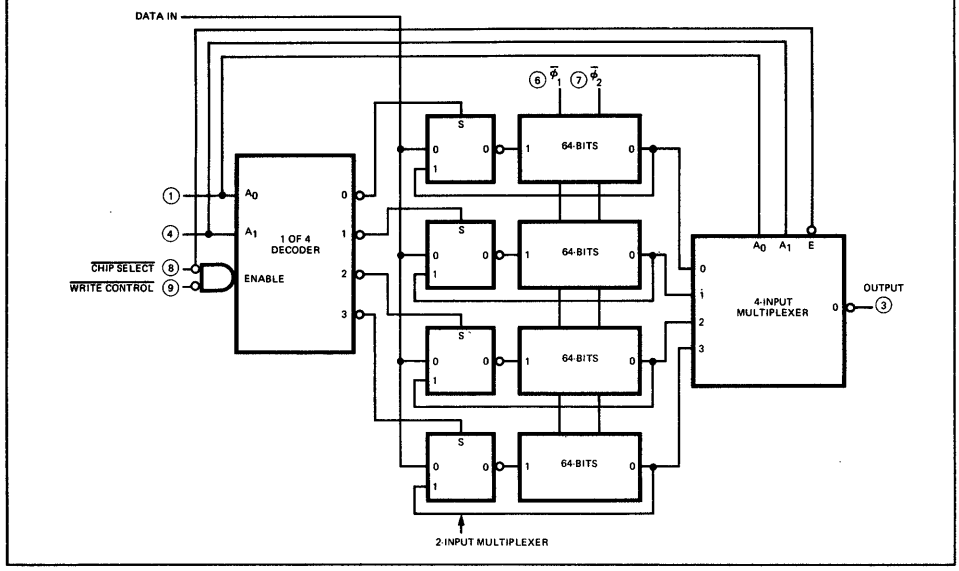


V_{DD} = Pin 10
V_{SS} = Pin 5

CONNECTION DIAGRAM
(TOP VIEW)



LOGIC DIAGRAM



H = HIGH = Most Positive Voltage
L = LOW = Most Negative Voltage

OUTPUT LEVEL			
Chip Select		Input	Output
H	Chip Not Selected	H	H
		L	H
L	Chip Selected	H	H
		L	L

LOOP NO.	ADDRESS		WRITE CONTROL	
	A_0	A_1	Write	Recirculate
1	L	L	L	H
2	L	H	L	H
3	H	L	L	H
4	H	H	L	H

FUNCTIONAL DESCRIPTION — The 3325 contains four 64-bit two-phase dynamic shift registers with complete input decoding, multiplexing, output selection and push/pull output driver circuitry. One out of four shift registers is selected by addressing to address lines A_0 and A_1. Any one of the four registers recirculates continuously if no new data is being written in. Old information is being erased automatically if new data is entering into the shift register. While one shift register is selected for either read or write, the other three recirculate continuously. LOW level of Write Control is defined as writing, while HIGH level as reading and recirculating. When Write Control line is at HIGH, all four shift registers are in the recirculating mode. When the Write Control line is at LOW, only the addressed shift register can receive new data while the other three shift registers recirculate. Chip is selected for the normal operation when Chip Select is set at LOW. When Chip Select is at HIGH, the output voltage goes to HIGH and information is being recirculated on all four shift registers.

Data writing in is accomplished by simultaneously selecting Chip Select at LOW, Write Control at LOW, Address lines, and applying data at input. When Write Control is at HIGH, data appears at output and recirculates, and no data can enter the shift register.

Data is entering the shift register when clock ϕ_1 is going to LOW. Data is appearing at the output when clock ϕ_2 is going to LOW.

For operation, the most positive voltage is defined as HIGH and the most negative voltage as LOW.

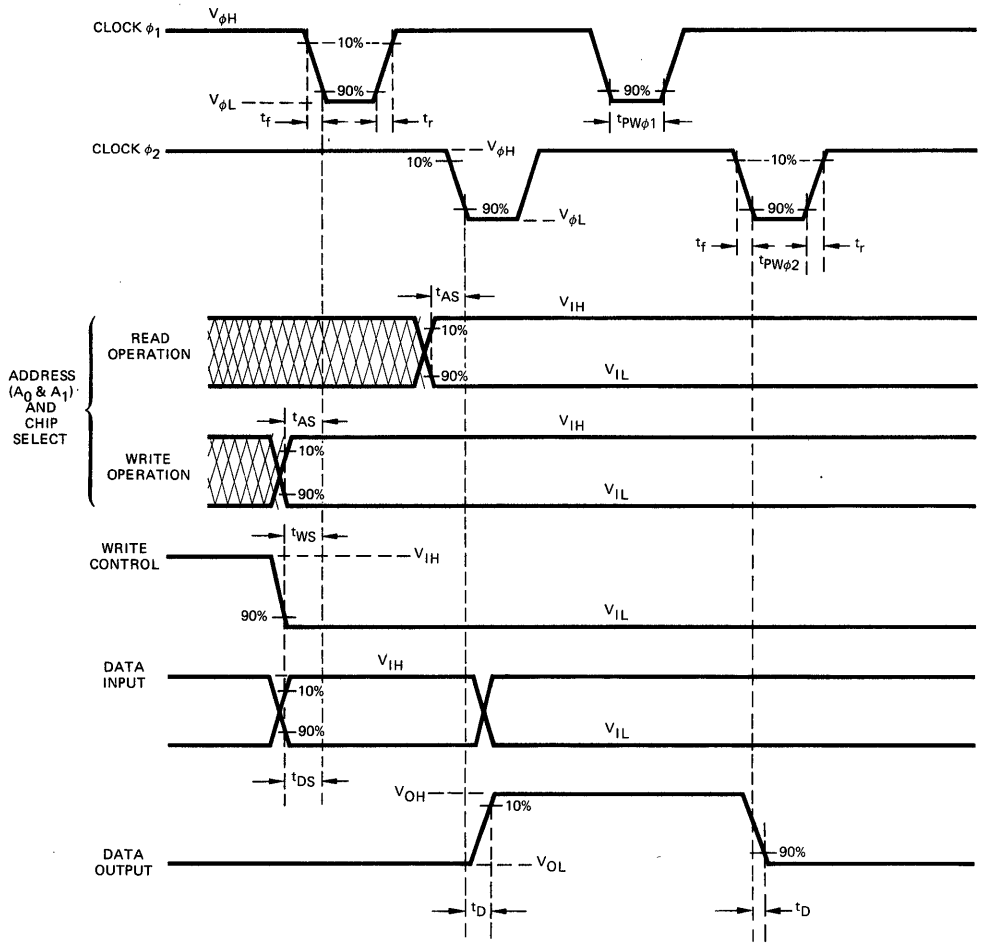
DC CHARACTERISTICS: V_{DD} = −12 V ±10%, V_{SS} = 5.0 V ±10%, T_A = 25°C, Load = 1 TTL Load with I_L = 1.6 mA.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Data Input Voltage HIGH	V_{SS} −1.0		V_{SS}	V	
V_{IL}	Data Input Voltage LOW	−1.0		0.8	V	
$V_{\phi H}$	Clock Pulse Voltage HIGH	V_{SS} −1.0		V_{SS}	V	
$V_{\phi L}$	Clock Pulse Voltage LOW		V_{DD} +2.0		V	
V_{OH}	Output Voltage HIGH	V_{SS} −0.6		V_{SS}	V	
V_{OL}	Output Voltage LOW			0.4	V	
	Leakage Current					
$I_{L\phi}$	Clock Input Leakage Current		50	500	nA	@ −15 V; all other pins at GND
I_I	Data Input (data, chip select, write control, address) Leakage Current		50	500	nA	@ −15 V; all other pins at GND
I_{LO}	Output Leakage Current		50	500	nA	@ −15 V; all other pins at GND
R_I	Input Pull Up Resistance	3.5	5.0	10	kΩ	V_{SS} = +5.0 V V_{DD} = −12 V V_{IN} = +0.4 V
I_{DD}	V_{DD} Current		6.0	10	mA	V_{SS} = +5.5 V V_{DD} = −13.2 V Clock Amplitude = +4.5 to −12 V Clock Duty Cycle = 30%
P_D	Power Dissipation		115	190	mW	

AC CHARACTERISTICS: V_{DD} = −12 V ±10%, V_{SS} = +5.0 V ±10%, T_A = 25°C, Load = 1 TTL Load with I_L = 1.6 mA.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Clock Frequency	0.001	1.0	3.0	MHz	
$t_{PW\phi}$	Clock Pulse Width	0.30		10	μs	
t_r, t_f	Clock Pulse Rise and Fall Time		0.1	1.0	μs	
t_D	Output Delay Times		40	70	ns	
t_{AS}	Address Set Up Time to ϕ_1	10	20		ns	
t_{WS}	Write Control Set Up Time to ϕ_1	10	20		ns	
t_{DS}	Data Set Up Time to ϕ_1	10	10		ns	
C_ϕ	Clock Capacitance		35	60	pF	$V_{\frac{}{\phi}} = V_{SS}$, f = 1 MHz
C_I	Data Input Capacitance		3.5	5.5	pF	$V_{\frac{}{\phi}} = V_{SS}$, f = 1 MHz

TIMING DIAGRAM



TYPICAL ELECTRICAL CHARACTERISTICS

POWER DISSIPATION VERSUS POWER SUPPLY VOLTAGE

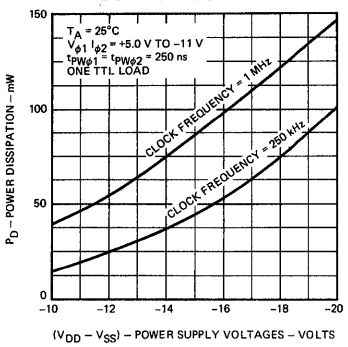


Fig. 1

POWER DISSIPATION VERSUS OPERATING CLOCK FREQUENCY

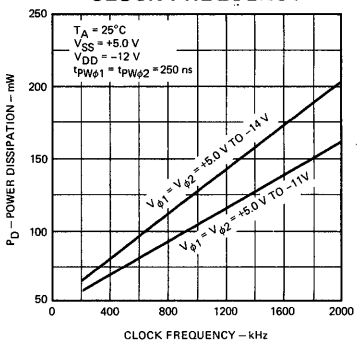


Fig. 2

POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

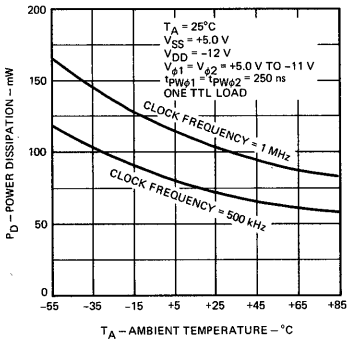


Fig. 3

TYPICAL ELECTRICAL CHARACTERISTICS

MINIMUM CLOCK PULSE WIDTH VERSUS CLOCK AMPLITUDE

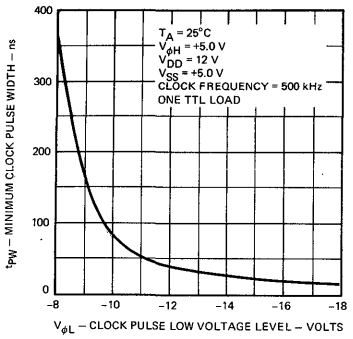


Fig. 4

MINIMUM CLOCK FREQUENCY VERSUS AMBIENT TEMPERATURE

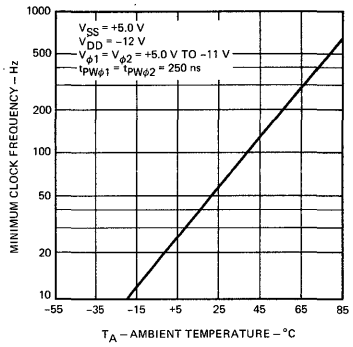


Fig. 5

POWER SUPPLY VOLTAGE VERSUS CLOCK AMPLITUDE

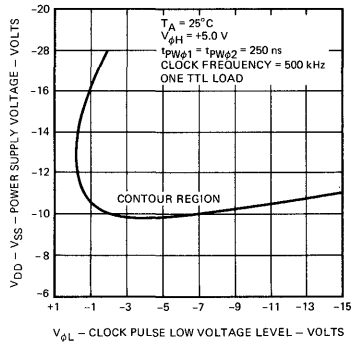


Fig. 6

OUTPUT DELAY TIMES VERSUS LOAD CAPACITANCE

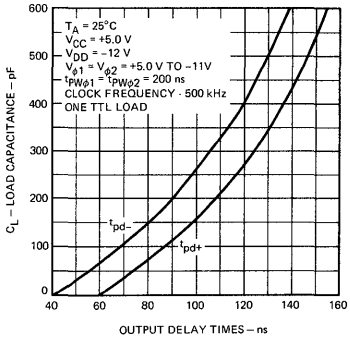


Fig. 7

CLOCK AMPLITUDE VERSUS CLOCK FREQUENCY

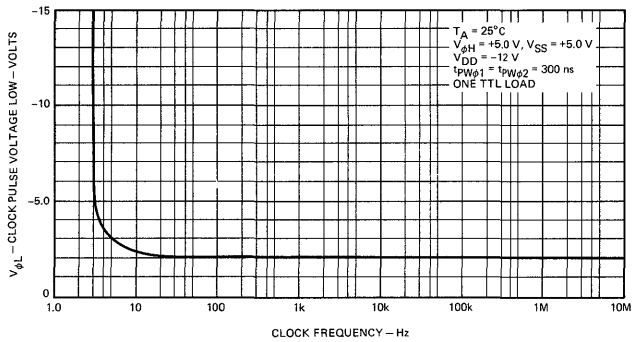


Fig. 8

3329(512-BIT)•3330(480-BIT)•3331(500-BIT)
DYNAMIC SHIFT REGISTERS
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3329, 3330 and 3331 are single 512-bit, 480-bit and 500-bit respectively, 2-Phase Dynamic Shift Registers. They are monolithic integrated circuits utilizing P-channel enhancement mode silicon gate MOS technology. An on chip input resistor allows direct bipolar compatibility by tying the V_P pin to V_{DD}. The output buffer is capable of driving both low level MOS and bipolar loads directly without addition of an external resistor.

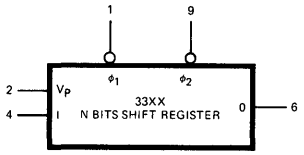
- **DIRECT BIPOLAR COMPATIBILITY**
- **2 MHz OPERATION GUARANTEED (TYPICALLY FROM 1 kHz to 4 MHz)**
- **45 pF CLOCKLINE CAPACITANCE (MAX.)**
- **0.5 mW/BIT POWER DISSIPATION (MAX.) AT 2 MHz**
- **INPUT OVERVOLTAGE PROTECTION**
- **10-LEAD TO-100 PACKAGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

All Inputs Including ϕ_1, ϕ_2 and V_P (Notes 1 & 3)	−24 V to +0.3 V
V_{GG} (Note 3)	−24 V to +0.3 V
V_{DD} and Output (Note 3)	−7.0 V to +0.3 V
Output Current when Output is LOW (Note 2)	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

NOTES:
1. V_P must be tied to V_{SS} if data input is between −7 V and −24 V.
2. LOW logic level is most negative level and HIGH logic level is most positive level.
3. All voltages with respect to V_{SS}.

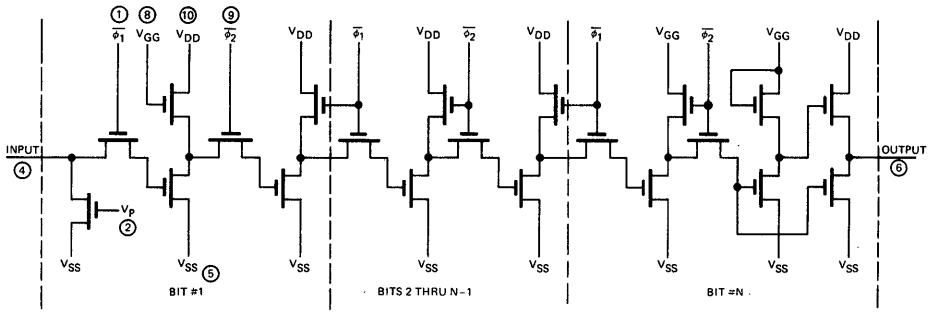
LOGIC SYMBOL



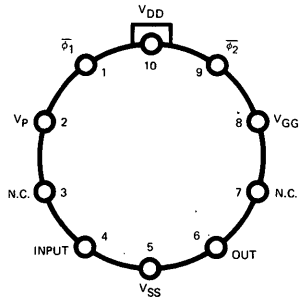
XX	N
29	512
30	480
31	500

V_{SS} = PIN 5
V_{DD} = PIN 10
V_{GG} = PIN 8

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION — The 3329, 30 and 31 are straight pipe line 2-phase dynamic shift registers. The functions ϕ_1 and ϕ_2 are non-overlapping and negative as illustrated in Figure 1. Data is accepted at the input when ϕ_1 is negative and data is available at the output after negative going transition of ϕ_2. The input is connected by a MOS transistor to V_{SS}; this transistor acts as an externally controlled pull up resistor allowing complete TTL compatibility. The output stage is push/pull, and can sink 1 TTL load to V_{DD} (1.6 mA at 0.4 V). Bipolar compatible operation is achieved by connecting V_{SS} to +5.0 V, V_{DD} to 0 V, and V_{GG} to −12 V, with V_P, the control pin to the input pull up resistor tied to V_{DD}.

DC CHARACTERISTICS: V_{SS} = 5.0 V ±10%, V_{DD} = 0 V, V_{GG} = −12 V ±10%, T_A = 0°C to +70°C.

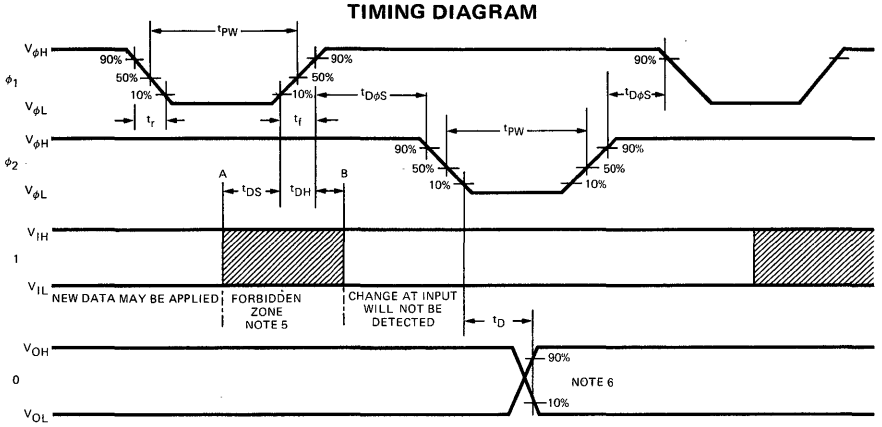
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS} −1.0			V	
V_{IL}	Input Voltage LOW	V_{GG}		0.8	V	$V_P = V_{SS}$ if V_I is Negative
$V_{\phi H}$	Clock Voltage HIGH	V_{SS} −1.0		V_{SS}	V	
$V_{\phi L}$	Clock Voltage LOW	−6.5		−4.5	V	
V_{OH}	Output Voltage HIGH	V_{SS} −0.6		V_{SS}	V	I_{OH} = −0.5 mA
V_{OL}	Output Voltage LOW	0	0.24	0.4	V	I_{OL} = 1.6 mA
I_{IH}	Input Current HIGH	0.17			mA	$V_I = V_{SS}$ −1, $V_P = V_{DD}$
I_{IL}	Input Current LOW		1.0	1.60	mA	V_I = 0.4 V, $V_P = V_{DD}$
I_{IL}	Input Current LOW			1.0	μA	V_I = −5.0 V, $V_P = V_{SS}$, T_A = 25°C
$I_{L\phi}$	Clock Input Leakage			1.0	μA	V_ϕ = −10 V, T_A = 25°C
R_{OH}	Impedance of Output HIGH		0.7	1.0	kΩ	$V_{OUT} = V_{SS}$ −0.5 V
R_{OL}	Impedance of Output LOW		150	250	Ω	$V_{OUT} = V_{OL}$
I_{GG}	V_{GG} Current		−2.4	−3.0	mA	V_{SS} = 5.5 V, V_{GG} = −13.2 V
I_{DD}	V_{DD} Current		−28	−35	mA	$V_{\phi L}$ = −6.5 V
I_{SS}	V_{SS} Current		30.4	38	mA	T_A = 25°C, f = 2.0 MHz
P_D	Power Dissipation		200	250	mW	t_{PW} = 200 ns

AC CHARACTERISTICS: V_{SS} = 5.0 V ±10%, V_{DD} = 0 V, V_{GG} = −12 V ±10%, T_A = 0°C to +70°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Operating Frequency	0.01		2.0	MHz	
t_{PW}	Clock Pulse Width	0.2		100	μs	Note 4
$t_{D\phi S}$	Time Between Clocks	0		100	μs	Note 4
t_r,t_f	Clock Rise & Fall Times (10% — 90%)			1.0	μs	
C_ϕ	Clock Capacitance (Each clockline)			45	pF	$V_\phi = V_{SS}$ f = 1.0 MHz
t_{DS}	Input Set Up Time	100			ns	
t_{DH}	Input Hold Time	0			ns	
t_D	Delay from ϕ_2 to Output			150	ns	C_L = 10 pF Load = 1 TTL Input

Note 4: Maximum cycle time (2 t_{PW} + 2 $t_{D\phi S}$) = 100 μs.

Fig. 1 **TIMING DIAGRAM**

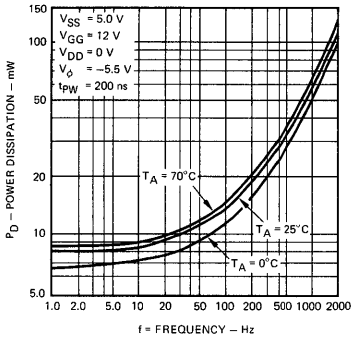


NOTES:

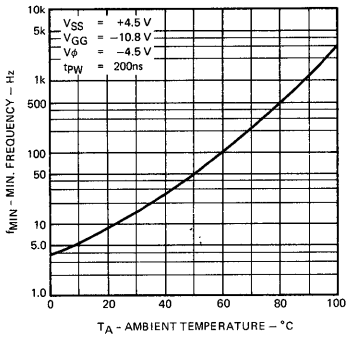
5. A and B define a window during which the input to the shift register is setting up. If the input data changes during this window, the change may or may not be detected. To avoid this ambiguous operation, the input data must remain good between A and B.
6. The outputs remain good until a new output appears.

TYPICAL ELECTRICAL CHARACTERISTICS

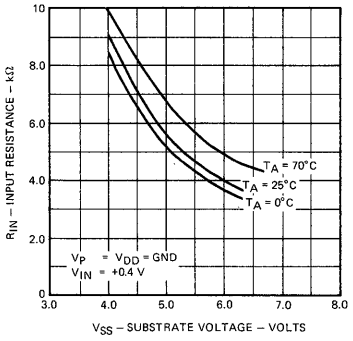
POWER DISSIPATION VERSUS FREQUENCY



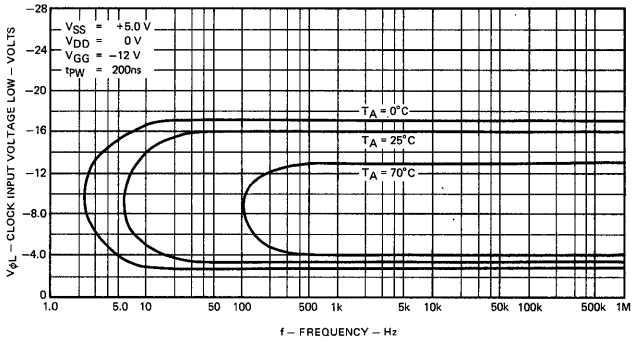
MINIMUM FREQUENCY VERSUS AMBIENT TEMPERATURE



INPUT RESISTANCE VERSUS SUBSTRATE VOLTAGE



CLOCK INPUT VOLTAGE LOW VERSUS FREQUENCY



APPLICATIONS

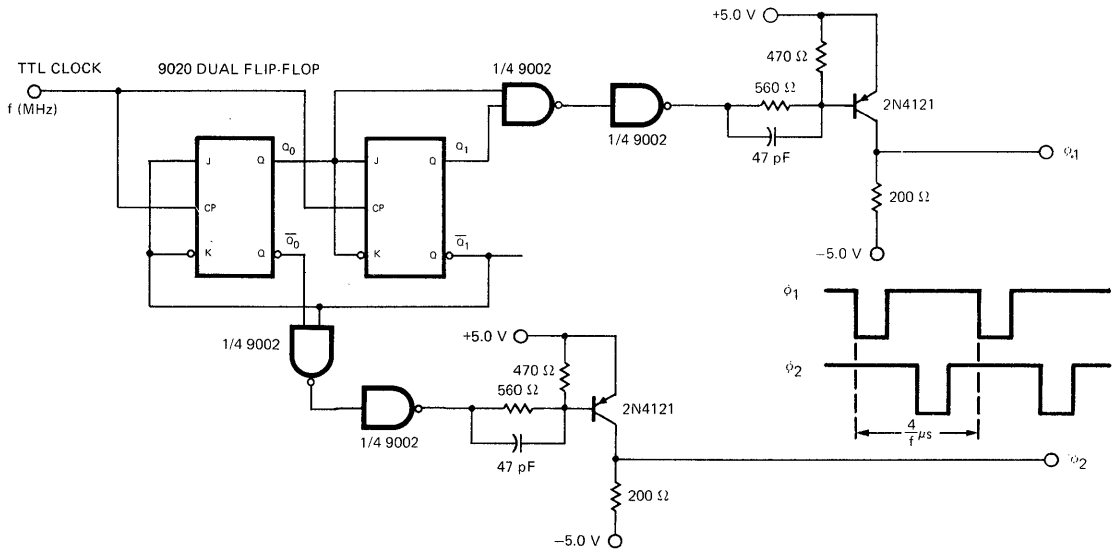


Fig. 2
2-PHASE NON-OVERLAPPING CLOCK GENERATOR

The counter states 11 and 00 are decoded to produce −5 V clock pulses.

APPLICATIONS

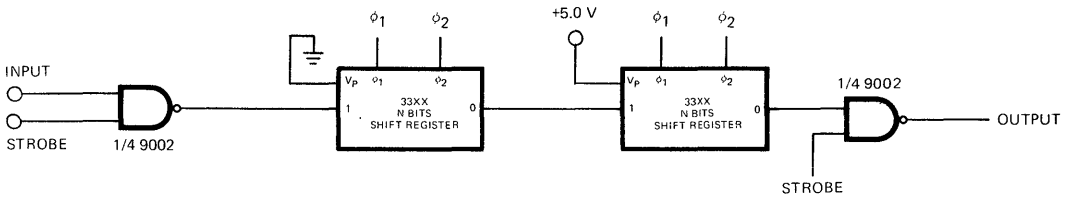


Fig. 3
SHIFT REGISTER INTERFACE

The shift register inputs may be connected directly to a TTL or DTL output if V_P is tied to ground. If the input is to be driven by a MOS output, V_P is tied to V_{SS}. The output can drive TTL or DTL directly. No external components are required.

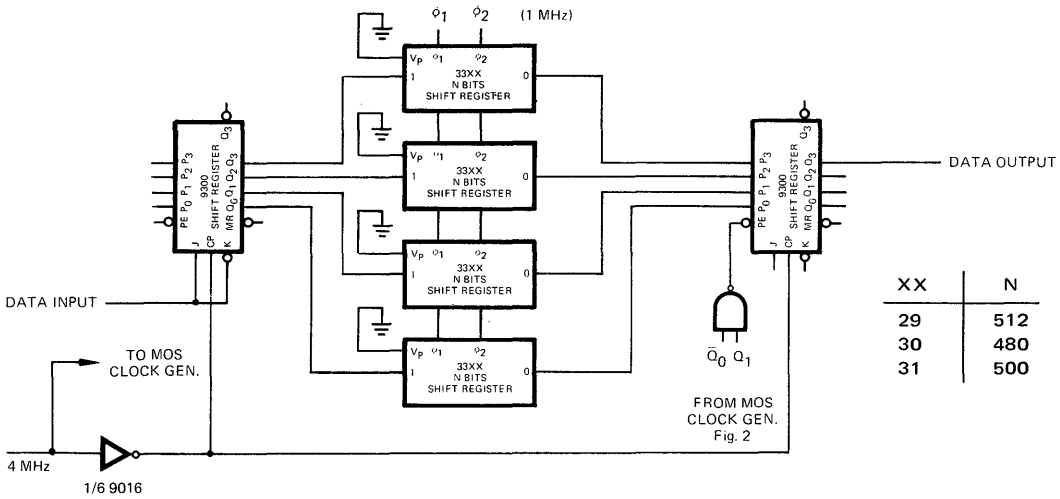


Fig. 4
HIGH SPEED SHIFT REGISTER

Four shift registers may be connected as shown in the figure above to simulate one long high speed shift register. The 9300 MSI shift register on the left is used as a serial to parallel converter. Data is clocked into the 9300 at four times the clock rate of the silicon gate shift registers. When four bits have been clocked in, they are loaded into the four long shift registers. At the output of the silicon gate registers, another 9300 is used to re-serialize the data at the higher clock rate. Because the 9300's add several bits of delay, the system illustrated looks like a high speed 4N + 5-bit register, where N is the length of each of the silicon gate registers.

Note that the clock period of the 9300's must be greater than the input set up time on the silicon gate registers.

3341

64-WORD × 4-BIT FIRST-IN FIRST-OUT SERIAL MEMORY

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3341 is a 64-word x 4-bit memory that operates in a first-in first-out (FIFO) mode. Inputs and the output are completely independent (no common clocks) making the 3341 ideal for asynchronous buffer applications.

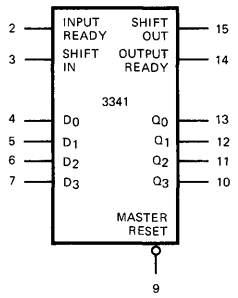
Special on chip input pull up circuits and bipolar compatible output buffers provide direct bipolar interfacing with no external components required. Control signals are provided so that both vertical and horizontal cascading may be easily achieved.

- **1 MHz SHIFT-IN SHIFT-OUT RATE**
- **DIRECT TTL/DTL INTERFACE AT INPUTS & OUTPUTS**
- **16-LEAD DUAL IN-LINE PACKAGE**
- **READILY EXPANDABLE IN EITHER DIRECTION**
- **ASYNCHRONOUS OR SYNCHRONOUS OPERATION**
- **CONVENIENT LEAD ORIENTATION FOR EASY BREADBOARDING**
- **UNIQUE TTL INPUT STAGE**

ABSOLUTE MAXIMUM RATINGS

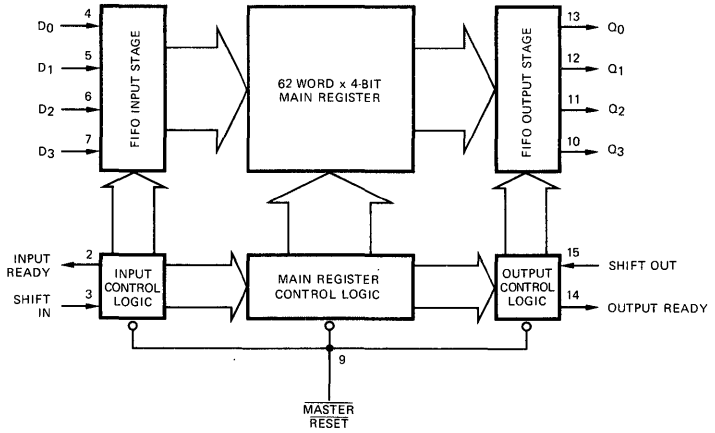
Storage Temp (T_S)	−65° C to +150° C
Operating Temp (T_A)	0° to +70° C
Voltage on all pins except outputs + V_{DD}	V_{SS} −24V to V_{SS} +0.3V
Voltage on V_{DD}	V_{SS} −7V to V_{SS} +0.3V

LOGIC SYMBOL

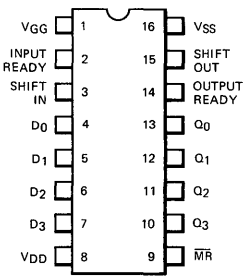


V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

LOGIC BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION:

DATA INPUT:

The four bits of data on the D_0 . . . D_3 inputs are entered into the first bit location when both Input Ready (IR) and Shift In (SI) are HIGH ($\approx V_{SS}$). This causes IR to go LOW ($\approx$GND), but data will stay locked in the first bit location until both IR and SI are brought LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

DATA TRANSFER:

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel, from input to the output of a previously empty device.

DATA OUTPUT:

When data has been transferred into the last cell, Output Ready (OR) goes HIGH, indicating the presence of valid data at the output pins Q_0 . . . Q_3. The transfer of data is initiated when both the Output Ready (OR) output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

SPECIAL INPUT CHARACTERISTICS:

The 3341 uses a TTL compatible input pull up circuit. When going HIGH, the TTL driver must only provide 2.2V minimum which is then internally pulled up to V_{SS}.

When going LOW, the TTL driver must overcome a current barrier of $\leqslant$1.6mA at 2V. Once this is overcome, the input current drops to zero.

Unused inputs are stable in the HIGH state, but must be terminated when LOW, e.g., 1MΩ to V_{GG}.

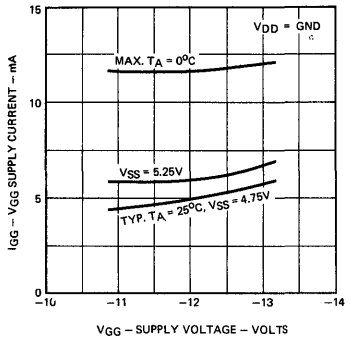
DC CHARACTERISTICS: V_{SS} = +5V ±5%, V_{GG} = −12V ±5%, V_{DD} = 0V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS}−1.0			V	Notes 1 and 2
V_{IL}	Input Voltage LOW			0.8	V	Note 1
V_{OH}	Output Voltage HIGH	V_{SS}−1.0			V	I_{OH} = 0.3mA
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 1.6mA
V_{PUP}	Input Pull Up Initiation Voltage			2.0	V	V_{SS} = 4.75V
V_{PUP}	Input Pull Up Initiation Voltage			2.2	V	V_{SS} = 5.25V
V_{BAR}	Peak Input Barrier Current Voltage Point			V_{SS}−1.5	V	
I_{IH}	Input Current HIGH	250			μA	Note 1, V_{IH} = V_{SS}−1.0 V
I_{LI}	Input Leakage Current			1.0	μA	Note 1, V_{IN} = 0V
I_{BAR}	Input Barrier Current			1.6	mA	Note 1
I_{GG}	V_{GG} Current		7.0	12	mA	
I_{DD}	V_{DD} Current		30	45	mA	
P_D	Power Dissipation			450	mW	

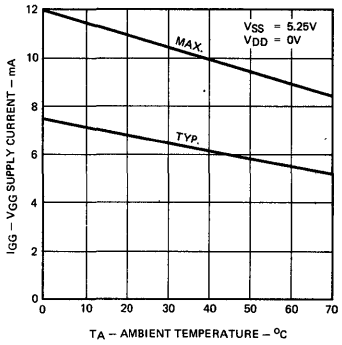
NOTES:
1. Inputs include D_0 — D_3. $\overline{\text{Master Reset}}$, Shift In, and Shift Out.
2. Internal pull up circuits are provided on all inputs to insure proper HIGH level.

ELECTRICAL CHARACTERISTICS

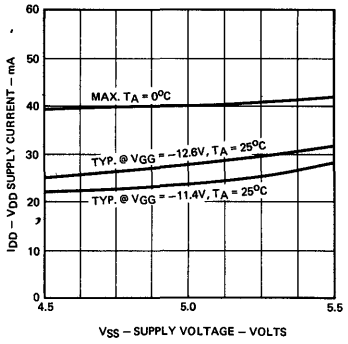
V_{GG} SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



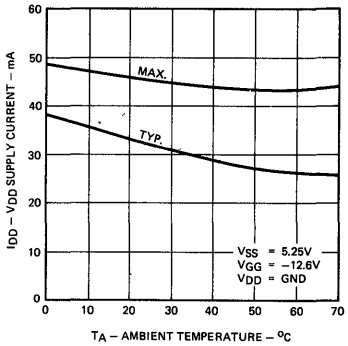
V_{GG} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



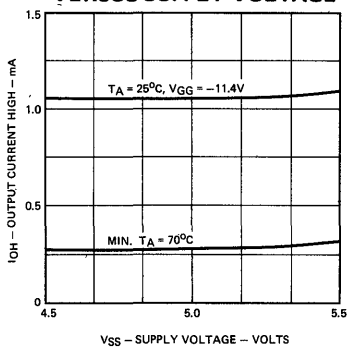
V_{DD} SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



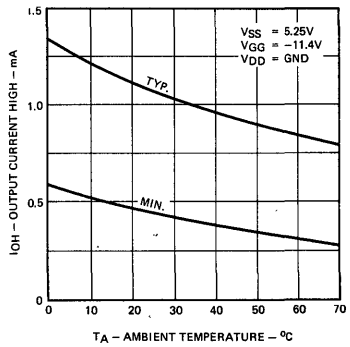
V_{DD} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



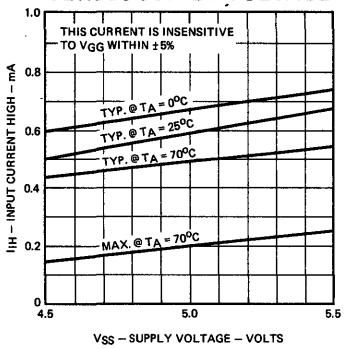
OUTPUT CURRENT HIGH VERSUS SUPPLY VOLTAGE



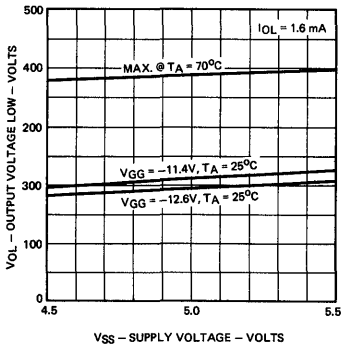
OUTPUT CURRENT HIGH VERSUS AMBIENT TEMPERATURE



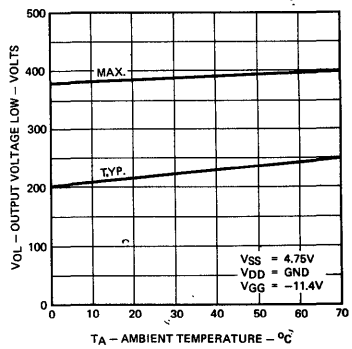
INPUT CURRENT HIGH VERSUS SUPPLY VOLTAGE



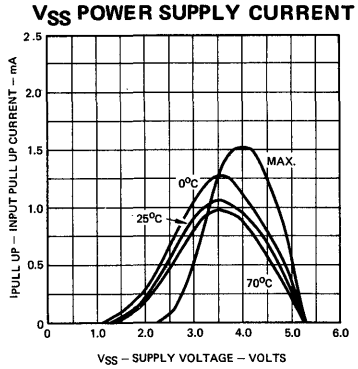
OUTPUT VOLTAGE LOW VERSUS SUPPLY CURRENT



OUTPUT VOLTAGE LOW VERSUS AMBIENT TEMPERATURE



INPUT PULL UP CURRENT VERSUS V_{SS} POWER SUPPLY CURRENT



AC CHARACTERISTICS: V_{SS} = +5V ± 5%, V_{DD} = 0V, V_{GG} = 12V ±5%, T_A = 0°C to 70°C

SYMBOL	CHARACTERISTIC	0°C			70°C			UNITS	CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{IR+}	Input Ready HIGH Time	90	200		155	300	550	ns	Fig. 1, Note 6
t_{IR-}	Input Ready LOW Time	138	250			300	550	ns	Fig. 1, Note 6
t_{0V+}	Control Overlap HIGH Time	70			100			ns	Figs. 1 and 2, Note 3
t_{0V-}	Control Overlap LOW Time	70			100			ns	Figs. 1 and 2, Note 3
t_{DSI}	Data Input Stable Time	400			400			ns	Fig. 1
t_{DD}	Data Input Delay Time	25						ns	Fig. 1, Note 5
t_{OR+}	Output Ready HIGH Time	90	200		155	300	500	ns	Fig. 2, Note 5
t_{OR-}	Output Ready LOW Time	170	300			450	850	ns	Fig. 2, Note 5
t_{PT}	Data Through-Put Time		10			10	32	μs	Note 4
t_{DH}	Data Hold Time	75						ns	Fig. 2, Note 5
t_{MRW}	Master Reset Pulse Width				400			ns	
t_{DA}	Data Output Available Time	0	30					ns	Fig. 2
C_I	Input Cap. of Data and Control Lines			7.0			7.0	pF	
C_{MR}	Input Cap. of $\overline{MR}$			15			15	pF	

NOTES:
3. Control signals include Input Ready, Shift In, Output Ready, and Shift Out.
4. This parameter defines total time from the time data is present at $D_0 - D_3$ to the time it is available at $O_0 - O_3$ with FIFO initially empty.
5. 1 TTL load +20 pF.

TIMING DIAGRAMS

INPUT TIMING

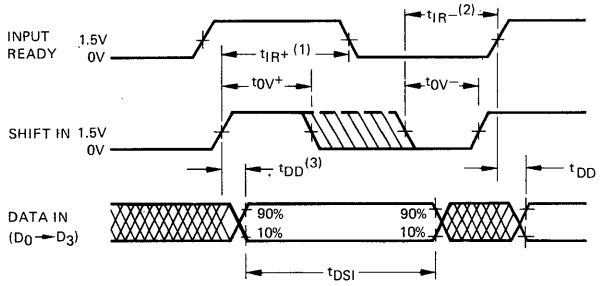


FIG. 1

Input data must remain stable during timing window t_{DSI}. Both SI and IR must be HIGH for $t_{0V}+$. Similarly, both SI and IR must be LOW for $t_{0V}-$.

NOTES:
1. $t_{IR}+$ is referenced to the positive going edge of IR or SI, whichever occurs later.
2. $t_{IR}-$ is referenced to the negative going edge of IR or SI, whichever occurs later.
3. t_{DD} is referenced to the positive going edge of IR or SI, whichever occurs later.
4. $t_{0V}+$ is referenced to the positive going edge of IR or SI, whichever occurs later.
5. $t_{0V}-$ is referenced to the negative going edge of IR or SI, whichever occurs later.
6. Data must be stable for t_{SDI} or t_{IR+}, whichever is shorter.

OUTPUT TIMING

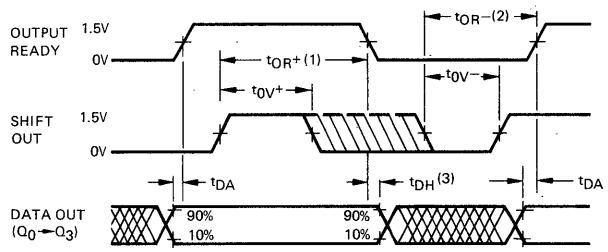


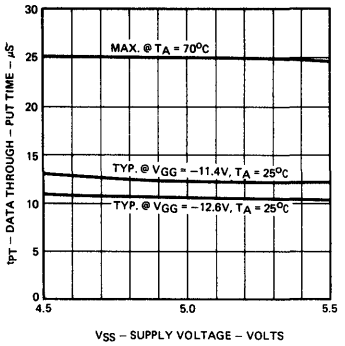
FIG. 2

Both SO and OR must be HIGH for $t_{0V}+$. Similarly both SO and OR must be LOW for $t_{0V}-$. Data will remain stable for t_{DH} after both SO and OR are LOW.

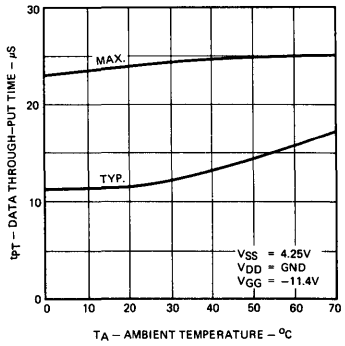
NOTES:
1. $t_{OR}+$ is referenced to the positive going edge of OR or SO, whichever occurs later.
2. $t_{OR}-$ is referenced to the negative going edge of OR or SO, whichever occurs later.
3. t_{DH} is referenced to the negative going edge of OR or SO, whichever occurs later.
4. $t_{0V}+$ is referenced to the positive going edge of IR or SI, whichever occurs later.
5. $t_{0V}-$ is referenced to the negative going edge of IR or SI, whichever occurs later.

ELECTRICAL CHARACTERISTICS

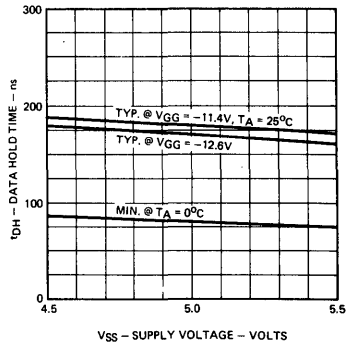
DATA THROUGH-PUT TIME VERSUS SUPPLY VOLTAGE



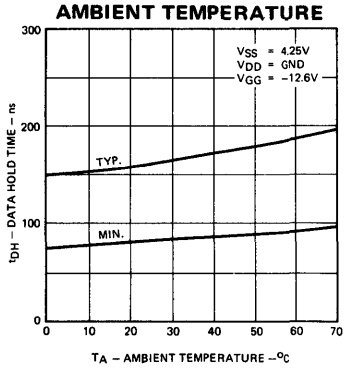
DATA THROUGH-PUT TIME VERSUS AMBIENT TEMPERATURE



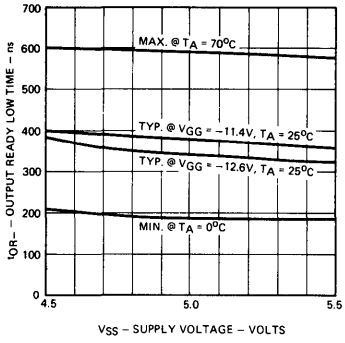
DATA HOLD TIME VERSUS SUPPLY VOLTAGE



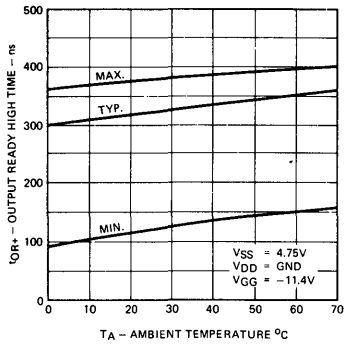
DATA HOLD TIME VERSUS AMBIENT TEMPERATURE



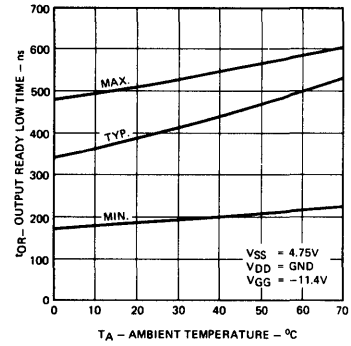
OUTPUT READY LOW TIME VERSUS SUPPLY VOLTAGE



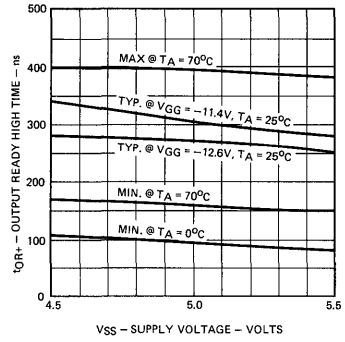
OUTPUT READY HIGH TIME VERSUS AMBIENT TEMPERATURE



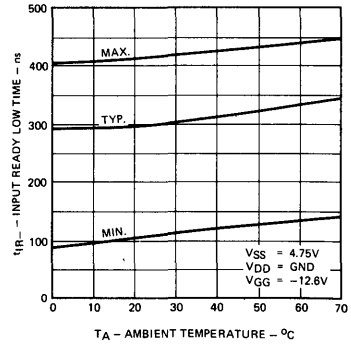
OUTPUT READY LOW TIME VERSUS AMBIENT TEMPERATURE



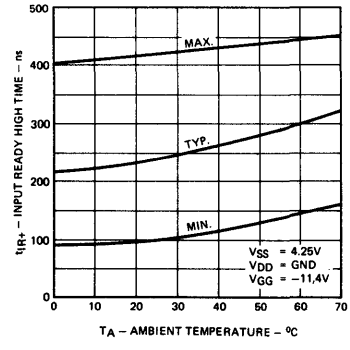
OUTPUT READY HIGH TIME VERSUS SUPPLY VOLTAGE



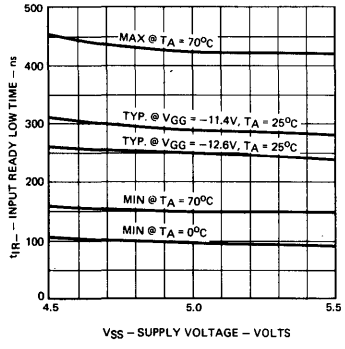
INPUT READY LOW TIME VERSUS AMBIENT TEMPERATURE



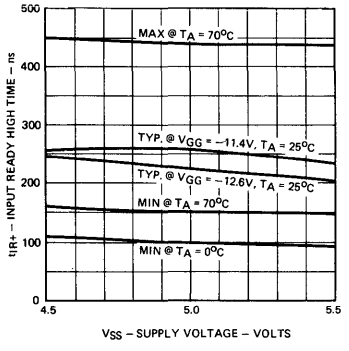
INPUT READY HIGH TIME VERSUS AMBIENT TEMPERATURE



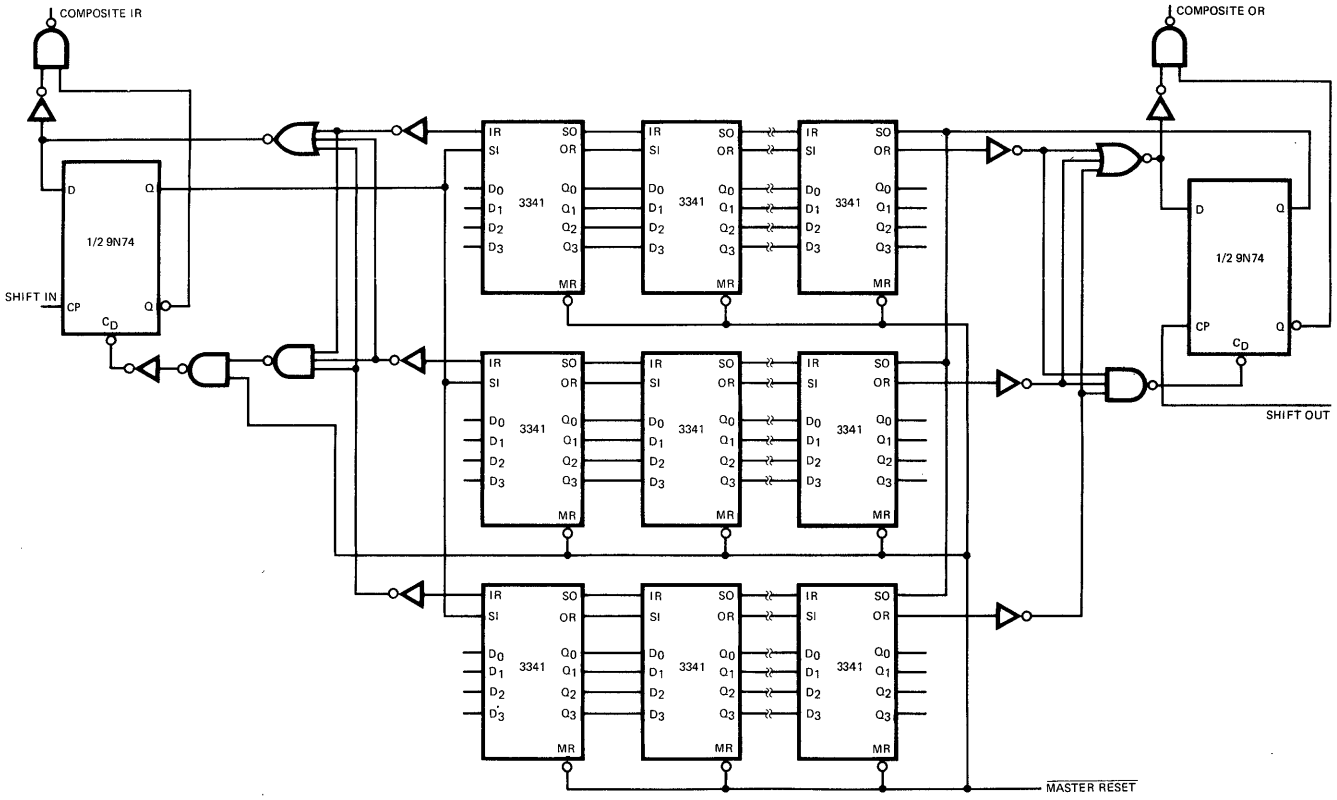
INPUT READY LOW TIME VERSUS SUPPLY VOLTAGE



INPUT READY HIGH TIME VERSUS SUPPLY VOLTAGE



EXPANSION OF 3341 TO N-WORD BY 12-BIT FIFO



NOTE: Composite Shift In should be LOW when Master Reset goes HIGH. Input data may be changed after Composite IR goes LOW. Composite IR will not go HIGH until Composite Shift In goes LOW. When Composite IR goes HIGH FIFO's will accept new data. 3341's will operate at their highest natural speeds if these rules are followed.

THE 3341
FIRST IN/FIRST OUT SERIAL MEMORY

INTRODUCTION

THE 3341 FIRST IN/FIRST OUT SERIAL MEMORY

The term First In/First Out (FIFO) is almost self explanatory. The first data in is the first data available at the memory outputs. A simple analogy of the FIFO principle is a pipe which accepts, stores, and disperses tennis balls, on demand, (*Figure 1*).

The tennis balls enter the pipe at the top and immediately travel to the bottom; a spring clip retains them until one or more balls are needed. The first tennis ball loaded is the first available for use. When balls are removed from the pipe, the storage capacity increases in accord with the number removed, and new balls can then be added at the top. In merchandising, many versions of FIFO systems are evident; consider, for example, cigarette and other vending machines.

A FIFO data memory operates in basically the same manner. Data is entered at the loading point and the first data entered is available for removal first, regardless of the quantity of data stored. Consider a shift register in which data is entered at the left and removed from the right. In a conventional shift register, data entered at the left remains there until additional data enters the register and forces the data already entered to the right. In a FIFO, the data is also entered at the left, but instead of remaining, it shifts to the right immediately. *Figure 2* illustrates the basic difference between conventional shift registers and FIFO memories. The major advantage of data appearing at the output automatically is to allow buffering of two systems that operate at differing data rates.

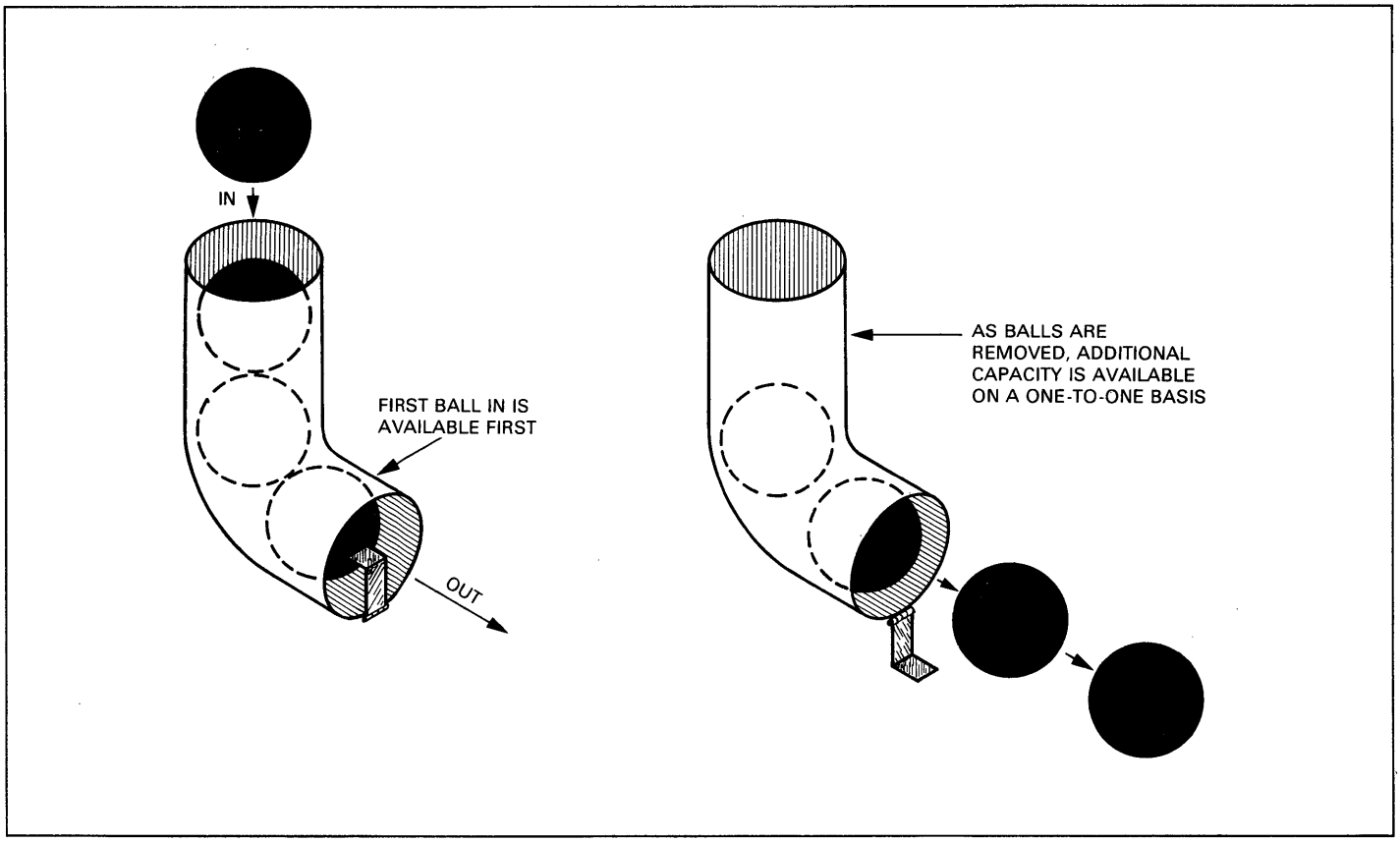


Figure 1. The FIFO Principle, First Input In is Available First

INPUT	X	X	X	X	OUTPUT
0	0	X	X	X	→
1	1	0	X	X	→
1	1	1	0	X	→
0	0	1	1	0	→

X = unknown data

In a conventional shift register, data if forced through by additional data — stays left.

INPUT	–	–	–	–	OUTPUT
0	–	–	–	0	→
1	–	–	1	0	→
1	–	1	1	0	→
0	0	1	1	0	→

– = empty positions

In a FIFO shift register, data falls through — goes right.

Figure 2. Input Data Storage in Conventional Shift Register Compared to FIFO Shift Registers

There are synchronous and asynchronous FIFOs. Both types use a clock to determine data entry and data withdrawal. Synchronous FIFO memories, however, can never enter data without losing data, even with high clock rates. This synchronous operation problem can be overcome with a split clock; the input command becomes the input clock and the output command becomes the output clock, or asynchronous operation. With asynchronous operation, data can be entered and withdrawn at different rates as long as the FIFO is neither empty on an output clock pulse nor full on an input clock pulse. The 3341, completely asynchronous, is ideal for independent data entry and exit.

FUNCTIONAL DESCRIPTION

Figure 3 is a logic diagram of the 3341 64-word x 4-bit First In/First Out serial memory. The 3341 has four serial 64-bit data registers and a 64-bit marker register. When data is entered by a Shift In command, it moves automatically under control of the marker register to the empty word position closest to the output. The marker register contains a "1" for an occupied position and a "0" for an empty position. Data words, of course, can not advance into an occupied position, (a marker bit of "1"); however, as soon as the next position's marker bit changes to a "0", the data automatically shifts toward the output.

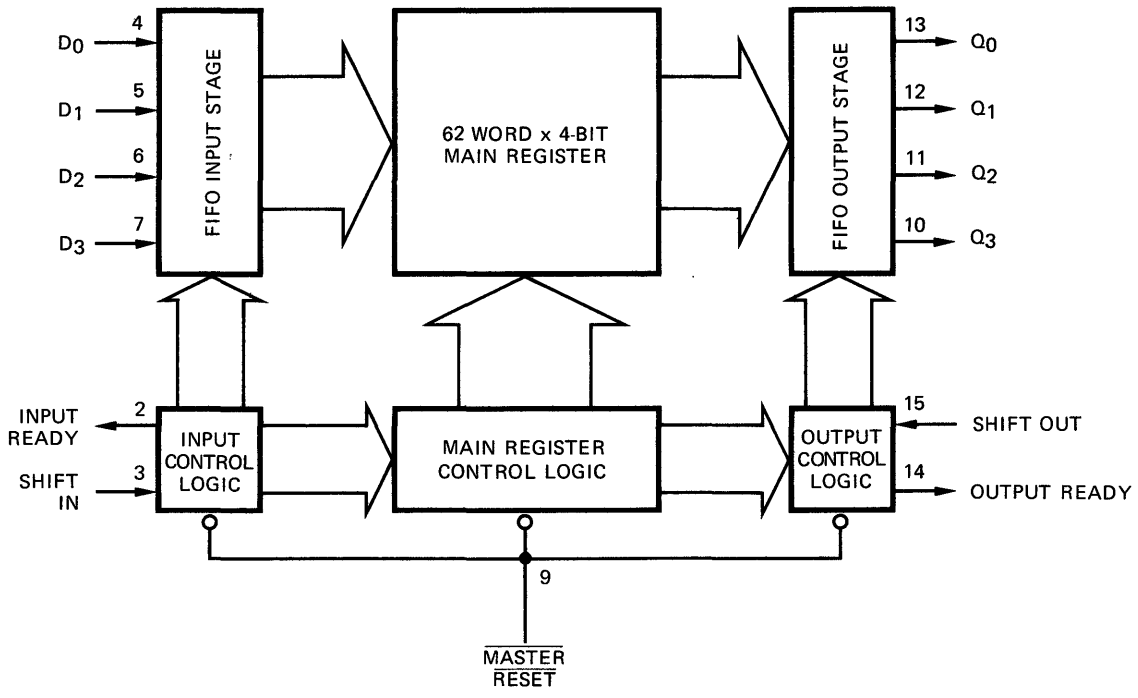


Figure 3. The 3341 Logic Block Diagram

The 3341 can simultaneously contain operational combinations of data exiting, data stacking, motion to the right, and data entry. The 3341 is totally asynchronous with completely independent inputs and outputs, simultaneous Shift In and Shift Out commands are also possible.

A unique advantage of the 3341 is that it can control system speed. In most memories, specifications must be carefully examined with regard to system speed. The 3341 has status indicators on both input and output stages, Input Ready and Output Ready. A High level on Input Ready indicates that the input is empty and can accept data. A High level on Output Ready indicates that the output has data and can accept a Shift Out command.

Input Operation

The set up time on the 3341 is actually negative in that data can change during a 25 ns period following a Shift In command. This allows the Shift In command to be used as a trigger to load data into a TTL latch and have the data stable in time for entry into the 3341. Reliable operation, however, uses the Input Ready Low-to-High transition as an indication that data can be safely entered.

The 3341 memory is self timing; the Input and Output Ready signals indicate that it is ready to accept a command. Systems wait until the Input Ready goes High and then initiate a Shift In command applied for the minimum High time (100 ns or longer). When the Input Ready goes Low, the FIFO has accepted the data and it may be changed. The input Ready can not go High again until the Shift In first goes Low for a minimum time (100 ns). This minimum time encompasses both Input Ready, and Shift In, low periods. New Shift In commands can be applied as soon as Input Ready goes High.

The Shift In command can be applied before Input Ready goes High if the minimum overlap times of Input Ready Low and Shift In Low have been satisfied. In such case, data is not entered until Shift In goes High. The minimum High period for Shift In is actually simultaneous with the High period for Input Ready. A special condition requiring a prior Shift In command occurs after a Master Rest command. When Master Reset goes Low, the FIFO is cleared. When Master Reset returns High and Shift In is High, data is entered as soon as Input Ready goes High. It is recommended that Shift In be Low when Master Reset is returned High.

Output Operation

The timing requirements are basically the same for output operation as with input operation in that Output Ready and Shift Out both have minimum simultaneous High and Low times (100 ns). However, one important point; when Output Ready is Low for an extended time, indicating an empty FIFO, and Shift Out is High, data is shifted out as soon as it enters if Output Ready goes High. It is also important to note that if only one word is left in the FIFO after a Shift Out command, this word remains on the output leads even though Output Ready stays Low. Such data must be forced out of the FIFO by data in the preceding position.

A Unique Input Pullup Circuit

All 3341 inputs, D_0 — D_3, Master Reset, Shift In and Shift Out, use a unique input circuit providing direct compatibility with TTL logic. Without this circuit, a resistor (internal or external), would be required to pull the TTL High (2.4 V) output above the minimum input High voltage (VSS −1 V). This presents a loading problem to a TTL gate in the Low state. With the pull up circuit on the 3341, the resistor is effectively connected only when the TTL output is High and presents no load to the TTL Low output. The input current versus input voltage relationship is shown in *Figure 4.* This unique circuit also eliminates switch bounce using the circuit shown in *Figure 5.*

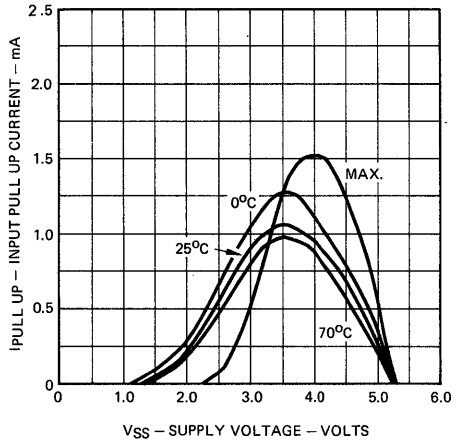


Figure 4. Input Characteristics of the 3341

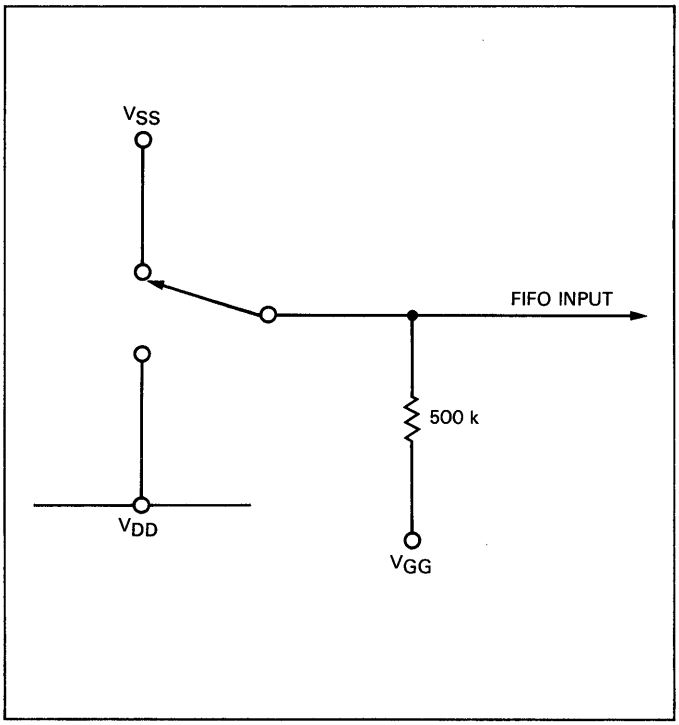
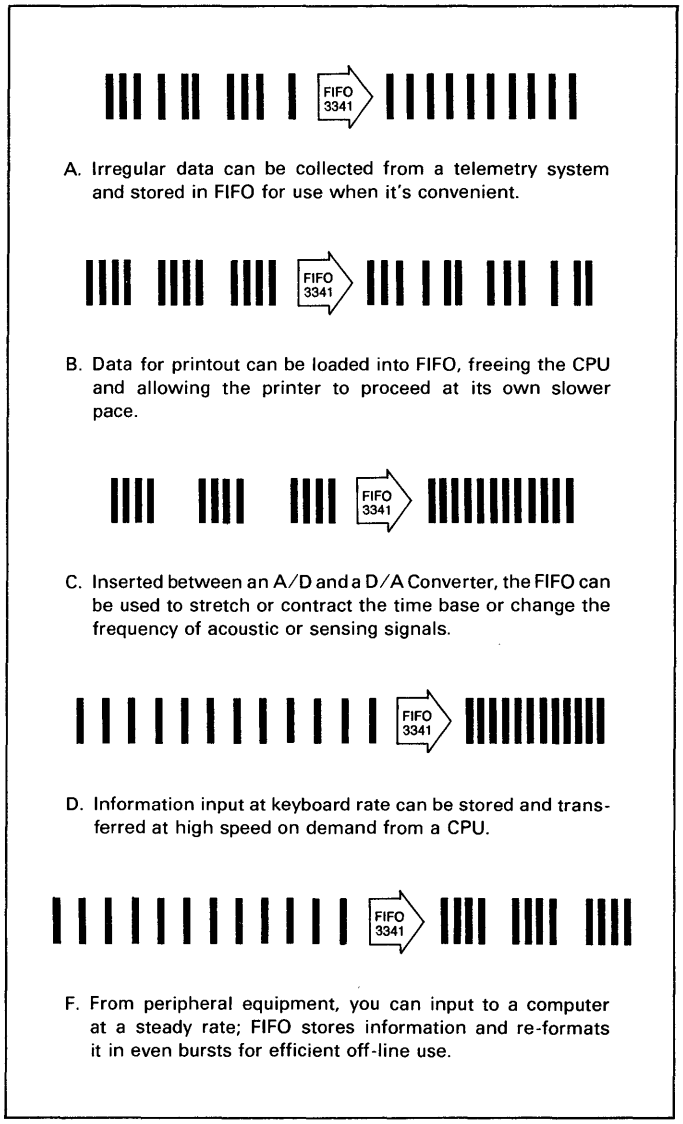


Figure 5. Switch Bounce Eliminator Using 3341 Unique Input Pullup Circuit

APPLICATIONS

An ideal use of the 3341 FIFOs is with two systems or subsystems of differing data or unsynchronized data rates that must talk to each other. Data can be entered or removed in steady streams, bursts, or irregular patterns, or a combination of these. Some example of differing or unsynchronized data rates are shown in *Figure 6.*



A. Irregular data can be collected from a telemetry system and stored in FIFO for use when it's convenient.

B. Data for printout can be loaded into FIFO, freeing the CPU and allowing the printer to proceed at its own slower pace.

C. Inserted between an A/D and a D/A Converter, the FIFO can be used to stretch or contract the time base or change the frequency of acoustic or sensing signals.

D. Information input at keyboard rate can be stored and transferred at high speed on demand from a CPU.

F. From peripheral equipment, you can input to a computer at a steady rate; FIFO stores information and re-formats it in even bursts for efficient off-line use.

Figure 6. Examples of FIFO Handling of Differing Data Rates

Expanding the FIFO System

The 3341 timing allows device stacking by tieing inputs to outputs; Input Ready to Shift Out, and Shift In to Output Ready. *Figure 7* shows this stacking method.

If a word longer than four bits is desired, the FIFOs are paralleled with external logic to insure that all inputs and outputs are ready before entry or removal of data is requested. *Figure 8* shows a 3341 expansion for more words with more bits per word. Loading is accomplished after the Low-to-High transistion of Shift In and removal is accomplished on the High-to-Low transistion of Shift Out. Shift In should not go High while Composite Input Ready is Low because the automatic lock feature could be defeated by time delay differences. It should be noted that the Composite Input Ready Low transistion can not be used to indicate that it is safe to

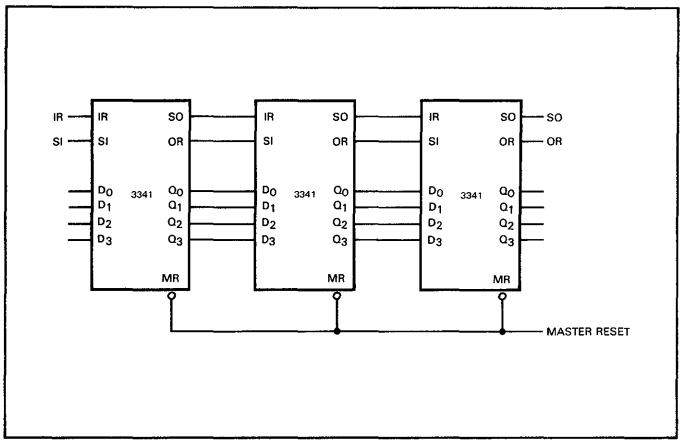


Figure 7. Stacking of the 3341 for Longer Words

remove data since it goes Low when the last 3341 Input Ready goes Low. In this application the user should meet data sheet timing requirements.

Edge Triggering

Edge triggering allows a rising or falling edge to initiate and complete the FIFO peration on either the input or the output. *Figure 9* shows a positive edge trigger circuit. For negative edge triggering, simply change the flip-flop to one that triggers on the negative edge (9H106). The string of non-parallel FIFOs uses a 2-input AND gate to connect IR and MR to the input flip-flop. It is also possible to mix edges, e.g., positive edge in and negative edge out.

Content Indicator

In some applications, it is desirable to know how much data is stored in the FIFO memory. The circuit in *Figure 10* detects simultaneous Shift In and Shift Out pulses and inhibits the count. The counters increment on the Low-to-High transition. The Count Up and Count Down lines must be connected directly to the Shift In or Shift Out of the 3341 FIFO whether or not edge triggering is used.

The 9360 is a decade counter and the 9366 is a binary counter. The counters can be loaded with preset numbers to provide either full or empty indications. If a full indication is desired, the Count Up and Count Down lines are reversed and a number corresponding to the cascaded length of the FIFO is loaded into the counter during Master Reset Low. Load is tied to Master Reset and MR lines of the counters are disconnected. The TC_D goes Low to indicate a full FIFO. The circuit as is indicates an empty FIFO when TC_D is low.

Automatic Loading

In some applications it is necessary to dump data to make room for new data. A simple method to automatically dump one word from a full FIFO is shown in *Figure 11.* One word is dumped if the FIFO is full after new data has been entered. In effect, the FIFO has been shortened by one word as there is always one empty word position to accept new data. The one word automatic dump operation takes 32 µs.

Other Applications

The FIFO can be used to store either data sources or destinations by expanding the word size. If 9-bit-wide words are loaded from eight different sources randomly, the address of the source can be stored in the FIFO by widening the word to 12 bits as shown in *Figure 12.*

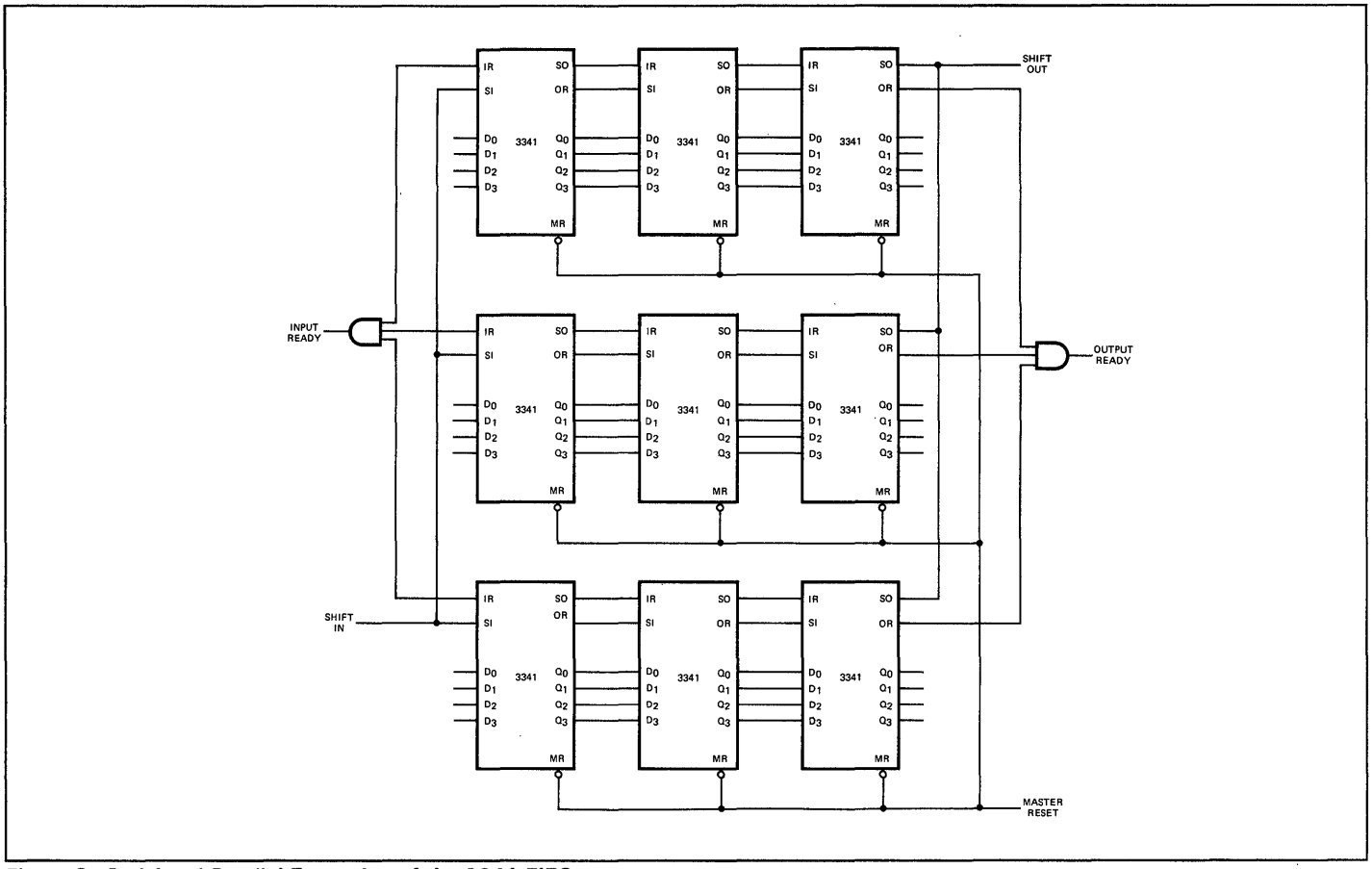


Figure 8. Serial and Parallel Expansion of the 3341 FIFO

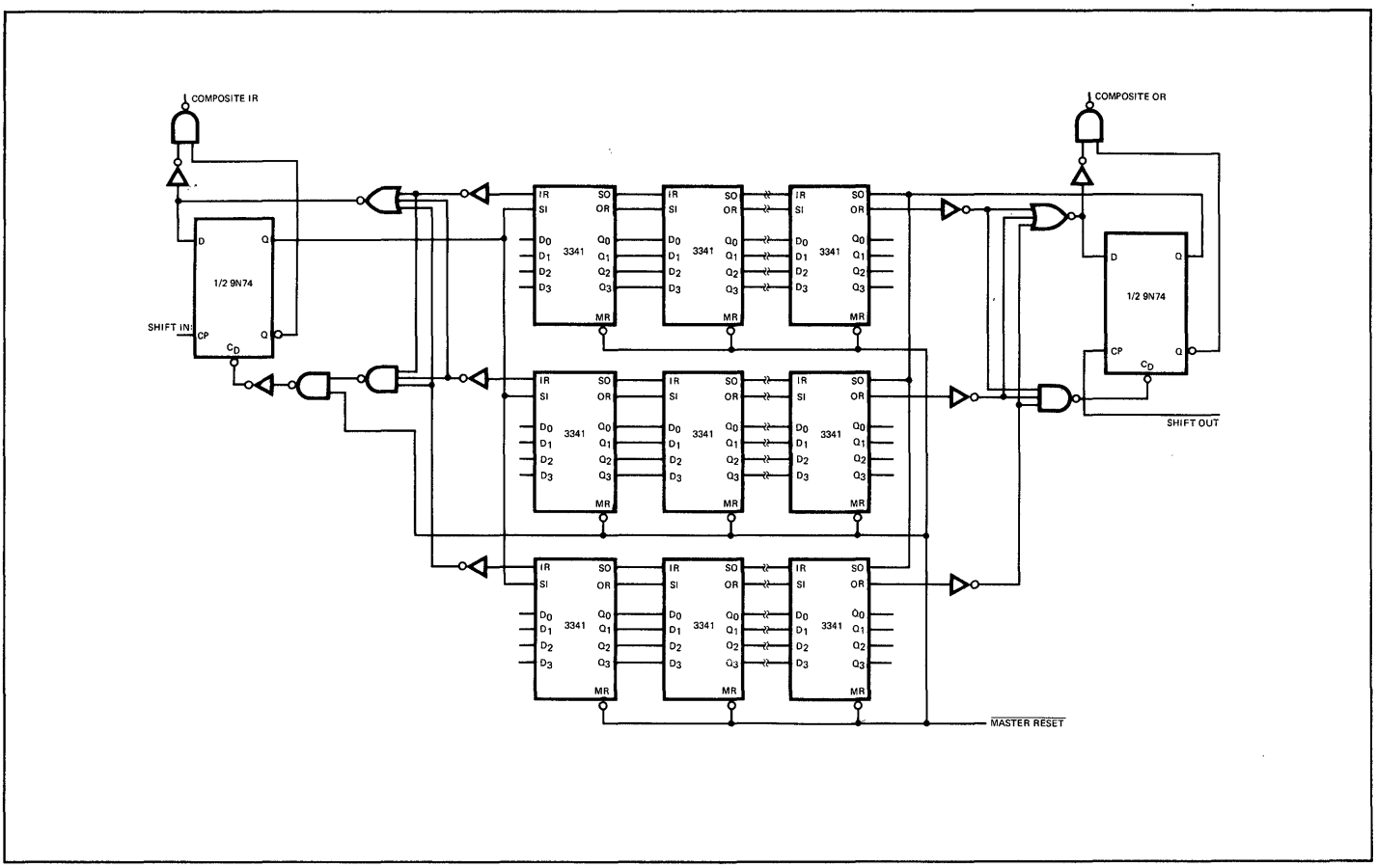


Figure 9. Positive Edge Triggering

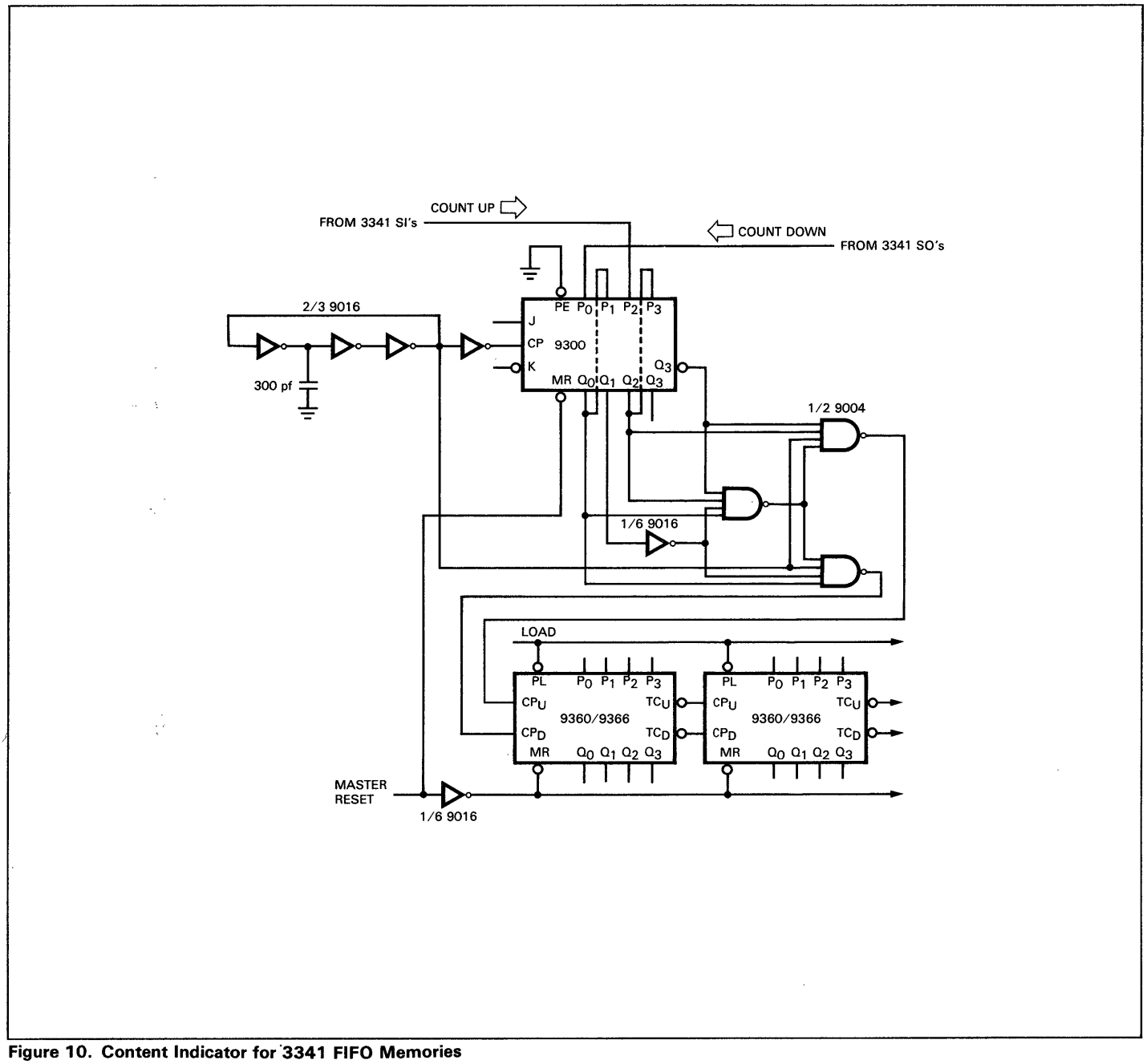


Figure 10. Content Indicator for 3341 FIFO Memories

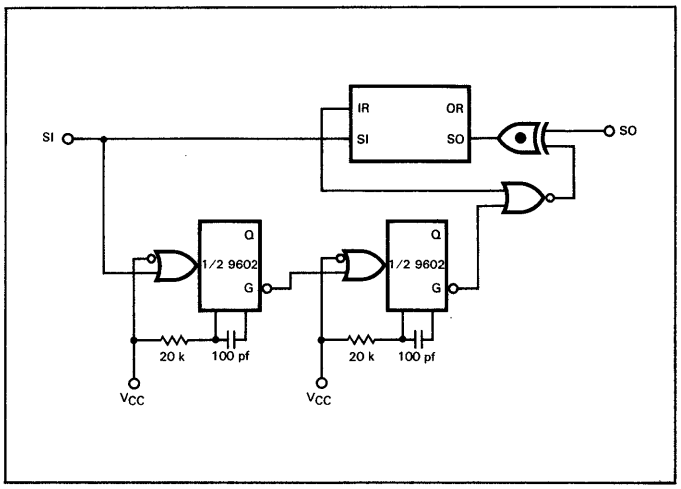


Figure 11. Automatic Dump of One Word from a Full FIFO

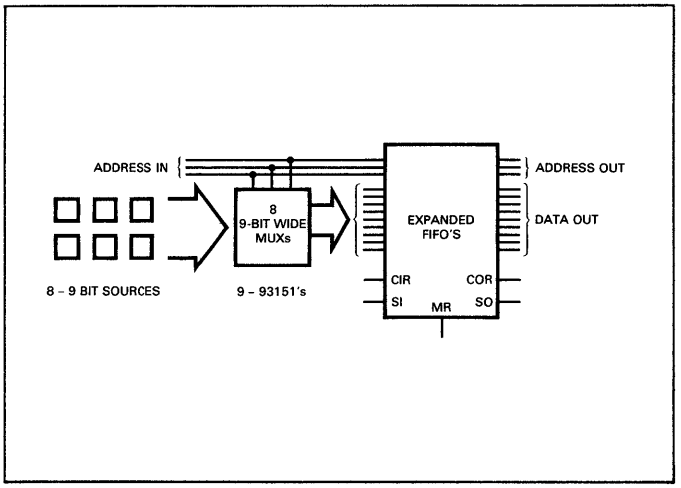


Figure 12. Adding an Address to Each Word

3342

QUAD 64-BIT STATIC SHIFT REGISTER

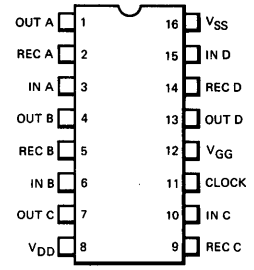
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3342 is a Quad 64-Bit Static Shift Register. It is a monolithic integrated circuit utilizing a P-channel enhancement mode silicon gate MOS technology. An on chip clock generator provides internal clock phases from a single external TTL clock. On chip input resistors on all inputs allow direct bipolar compatibility. The output buffers are capable of driving low level MOS and bipolar loads directly without the addition of external components.

- **SINGLE PHASE (1ϕ) DTL/TTL COMPATIBLE EXTERNAL CLOCK**
- **DIRECT BIPOLAR COMPATIBILITY**
- **2 MHz OPERATION GUARANTEED**
- **LOW CLOCKLINE CAPACITANCE**
- **INPUT OVERVOLTAGE PROTECTION**
- **EXTERNAL RECIRCULATE CONTROL**

CONNECTION DIAGRAM

DIP (TOP VIEW)

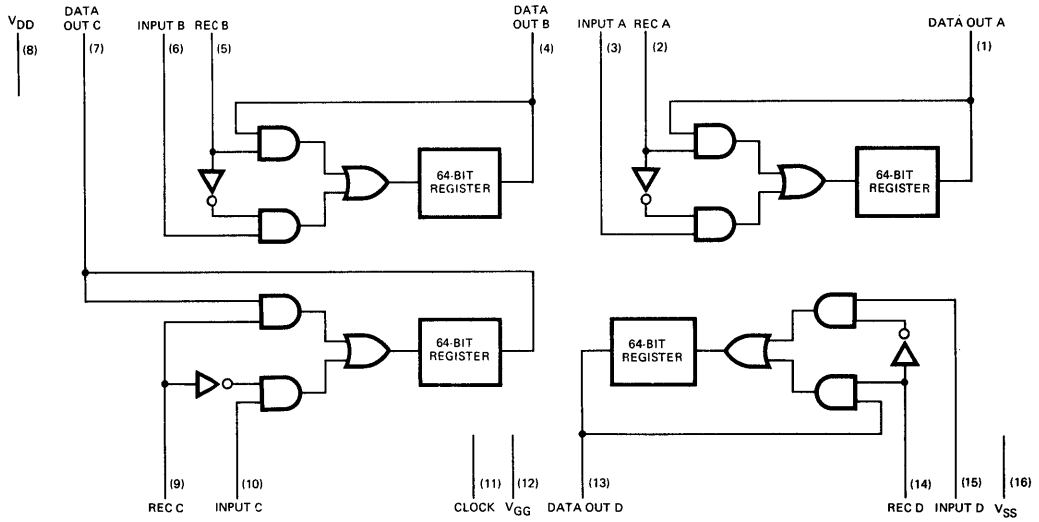


ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired):

All Inputs Including Clock	−20 V to +0.3 V
V_{GG} (Note b)	−20 V to +0.3 V
V_{DD} and Outputs (Note b)	−7.0 V to +0.3 V
Output Current When Output is LOW (Note a)	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

NOTES:
a. LOW logic level is most negative level and HIGH logic level is most positive
b. All voltages with respect to V_{SS}.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The 3342 is a single phase static shift register. Data is accepted at the inputs after the positive transition of the external clock. Data is available at the outputs after the negative clock transition as illustrated in Figure 1. All inputs are connected by an MOS transistor to V_{SS} allowing complete TTL compatibility. The recirculate input allows data to be entered externally (HIGH logic level) or internally recirculated in the registers (LOW logic level). The output stages are push/pull and can sink one TTL load to V_{DD} (1.6 mA at 0.4 V).

DC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = -12 V ±5%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS} - 1.0			V	Note 1 & 2
V_{IL}	Input Voltage LOW	V_{GG}		0.80	V	Note 1
V_{OH}	Output Voltage HIGH	2.4		V_{SS}	V	I_{OH} = -0.5 mA
V_{OL}	Output Voltage LOW	0	0.24	0.4	V	I_{OL} = -1.6 mA
I_{IH}	Input Current HIGH	-0.10			mA	$V_{IN}=V_{SS}$ -1.0V, Note1
I_{IL}	Input Current LOW		1.0	-1.6	mA	V_{IN} = 0.4V, Note 1
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = -5.0V, Note 1 All other pins at V_{SS}
I_{DD}	V_{DD} Current		20	28	mA	
I_{GG}	V_{GG} Current		8.0	12	mA	
I_{SS}	V_{SS} Current		28	40	mA	
P_D	Power Dissipation		280	380	mW	t_{PW} = 250ns, f = 2.0MHz

NOTES:
1. These parameters apply to all inputs including data inputs, recirculate inputs, and clock inputs.
2. On chip pull up resistors are provided on all inputs to effect the proper logic level when driving with TTL/DTL.
3. Outputs remain valid until negative going edge of next pulse.

AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = -12 V ±5%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
f	Operating Frequency	0		2.0	MHz	
t_{PW}	Clock Pulse Width	0.20		10	μs	Note 3
t_r, t_f	Clock Rise and Fall Times (10% to 90%)			1.0	μs	
t_{DS}	Data Input Setup Time	150			ns	
t_{DH}	Data Input Hold Time	100			ns	
t_D	Delay to Output		100	200	ns	C_L = 10 pF Load = 1 TTL Input
t_{RS}	Recirculate Set-Up Time	150			ns	
t_{RH}	Recirculate Hold Time	100			ns	
C	Capacitance (All Inputs Including Clock)		3.0	5.0	pF	V_ϕ=V_{SS}, f=1.0MHz

WAVEFORM

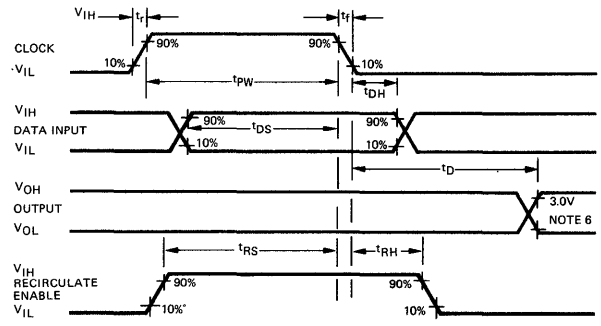


Fig. 1

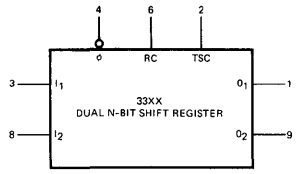
3343 (DUAL 128-BIT) • 3344 (DUAL 132-BIT)
3345 (DUAL 136-BIT) • 3346 (DUAL 144-BIT)
STATIC SHIFT REGISTERS
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3343, 3344, 3345, and 3346 are Dual 128-Bit, 132-Bit, 136-Bit and 144-Bit Static Shift Registers respectively. They are monolithic integrated circuits utilizing P-channel enhancement mode silicon gate MOS technology. An on chip clock generator provides all internal clock phases from a single external TTL clock pulse. On chip input resistors on all inputs allow direct bipolar compatibility. The output buffers are capable of driving low level MOS and bipolar loads directly without the addition of external components. The 3-State Control allows the outputs to be left floating if desired. The Data Select allows the user to either enter data from the outside or internally recirculate the contents of the registers.

FUNCTIONAL DESCRIPTION — The 3343, 3344, 3345 and 3346 are single phase static shift registers. Data is accepted at the inputs after the negative going transition of the external clock. Data is available at the outputs after the positive going transition as illustrated in Figure I. All inputs are connected by an MOS transistor to V_{SS} which acts as a pull up resistor allowing complete TTL compatibility. The recirculate control (RC) input allows data to enter externally (HIGH logic level) or internally recirculate in both registers (LOW logic level). The output stages are push/pull and can sink one TTL load to V_{DD} (1.6 mA at 0.4V). In addition, the Tri-State Control (TSC) allows the user to turn off both devices of the push/pull output in effect creating a wired-OR. The output control disables the outputs when it is LOW.

- **SINGLE TTL EXTERNAL CLOCK**
- **DIRECT BIPOLAR COMPATIBILITY**
- **2 MHz OPERATION GUARANTEED**
- **LOW CLOCKLINE CAPACITANCE (5 pF max)**
- **3-STATE OUTPUT**
- **INPUT OVERVOLTAGE PROTECTION**
- **EXTERNAL RECIRCULATION CONTROL**
- **10-LEAD TO-100 PACKAGE**

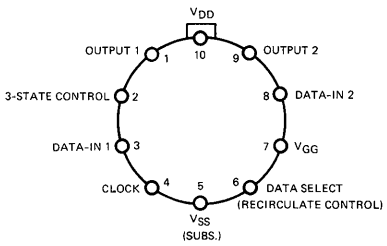
LOGIC DIAGRAM
(DUAL N-BIT SHIFT REGISTERS)



XX	N
43	128
44	132
45	136
46	144

RC - RECIRCULATE CONTROL
TSC - TRISTATE CONTROL
V_{GG} - 7
V_{SS} - 5
V_{DD} - 10

CONNECTION DIAGRAM
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

All Inputs including Clock, Select and TSC (Note 2)	−22V to +0.3V
V_{GG} (Note 2)	−22V to +0.3V
V_{DD} and Outputs (Note 2)	−7.0V to +0.3V
Output Current when Output is LOW (Note 1)	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to + 70°C

NOTES: 1. LOW logic level is most negative level and HIGH logic level is most positive level.
2. All voltages with respect to V_{SS}.

DC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12.0 V ±5%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
*V_{IH}	Input Voltage HIGH	V_{SS} − 1.0			V	
*V_{IL}	Input Voltage LOW	V_{GG}		0.8	V	
V_{OH}	Output Voltage HIGH	2.4V		V_{SS}	V	I_{OH} = −0.5 mA
V_{OL}	Output Voltage LOW	0	0.24	0.4	V	I_{OL} = 1.6 mA
*I_{IH}	Input Current HIGH	−0.10			mA	V_{IN} = V_{SS} −1.0V
*I_{IL}	Input Current LOW		1.0	−1.6	mA	V_{IN} = 0.4V
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = −5.0V All other pin at V_{SS}
I_{GG}	V_{GG} Current		8	12	mA	T_A = 25°C t_{PW} = 250 ns f = 2.0 MHz
I_{DD}	V_{DD} Current		20	28	mA	
I_{SS}	V_{SS} Current		28	40	mA	
P_D	Power Dissipation		280	380	mW	

*These parameters apply to all inputs including data inputs, recirculate inputs, and clock input.

AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
f	Operating Frequency	0		2.0	MHz	
t_{PW}	Clock Pulse Width	0.25		10	μs	Note 3
t_r, t_f	Clock Rise and Fall Times (10% to 90%)			1.0	μs	
t_{DS}	Input Setup Time	200			ns	
t_{DH}	Input Hold Time	100			ns	
t_D	Delay to Output		100	150	ns	C_L = 10pF, Load = 1 TTL Load
t_{DOE}	Output Enable Time			200	ns	
t_{DOD}	Output Disable Time			200	ns	
C	Capacitance (All Inputs Including Clock)		3	5.0	pF	V_ϕ = V_{SS} f = 1.0 MHz

NOTE 3 The outputs remain good until a new output appears.

WAVEFORM

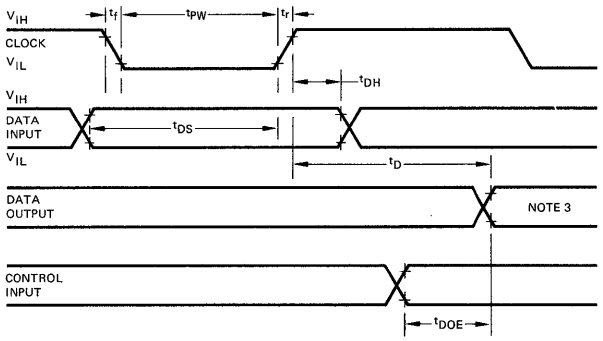


Fig. 1

3347

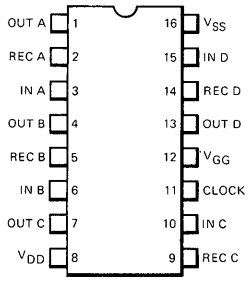
QUAD 80—BIT STATIC SHIFT REGISTER

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3347 is a Quad 80-Bit Static Shift Register. It is a monolithic integrated circuit utilizing a P-channel enhancement mode silicon gate MOS technology. An on chip clock generator provides all internal clock phases from a single external TTL clock pulse. On chip input resistors on all inputs allow direct bipolar compatibility. The output buffers are capable of driving low level MOS and bipolar loads directly without the addition of external components.

- **SINGLE TTL EXTERNAL CLOCK**
- **DIRECT BIPOLAR COMPATIBILITY**
- **2 MHz OPERATION QUARANTEED**
- **LOW CLOCKLINE CAPACITANCE (5 pF MAX)**
- **INPUT OVERVOLTAGE PROTECTION**
- **EXTERNAL RECIRCULATION CONTROL**
- **16-LEAD DUAL IN-LINE PACKAGE**

CONNECTION DIAGRAM
DIP (TOP VIEW)

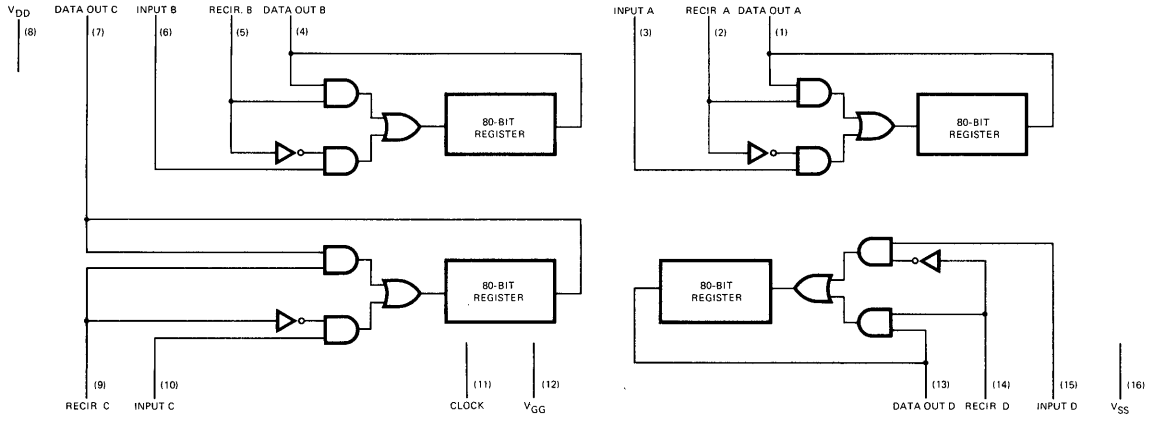


ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired):

All Inputs Including Clock	−20V to +0.3V
V_{GG} (Note 2)	−20V to +0.3V
V_{DD} and Outputs (Note 2)	−7.0V to +0.3V
Output Current when Ouptut is LOW (Note 1)	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

NOTES:
1. LOW logic level is most negative level and HIGH logic level is most positive.
2. All voltages with respect to V_{SS}.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 3347 is a single phase static shift register. Data is accepted at the inputs after the positive going transition of the external clock. Data is available at the outputs after the negative going transition as illustrated in Figure 1. All inputs are connected by an MOS transistor to V_{SS} which acts as a pull up resistor allowing complete TTL compatibility. The select input allows data to enter externally (HIGH logic level) or internally recirculate in both registers (LOW logic level). The output stages are push/pull and can sink one TTL load to V_{DD} (1.6 mA at 0.4V).

DC CHARACTERISTICS: V_{SS} = +5.0V ±5%, V_{DD} = 0 V, V_{GG} = -12V ±5%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS} - 1.0			V	Note 3 & 4
V_{IL}	Input Voltage LOW	V_{GG}		0.80	V	Note 3
V_{OH}	Output Voltage HIGH	2.4		V_{SS}	V	I_{OH} = -0.5 mA
V_{OL}	Output Voltage LOW	0	0.24	0.4	V	I_{OL} = 1.6 mA
I_{IH}	Input Current HIGH	-0.10			mA	V_{IN} = V_{SS} -1.0V, Note 3
I_{IL}	Input Current LOW		1.0	-1.6	mA	V_{IN} = 0.4V Note 3
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = -5.0V, Note 3 All other pin at V_{SS}
I_{DD}	V_{DD} Current		25	35	mA	
I_{GG}	V_{GG} Current		10	15	mA	
I_{SS}	V_{SS} Current		35	50	mA	
P_D	Power Dissipation		325	450	mW	

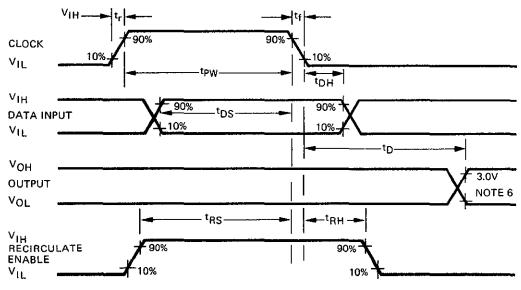
AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
f	Operating Frequency	0		2.0	MHz	
t_{PW}	Clock Pulse Width	0.20		10	μs	Note 5
t_r,t_f	Clock Rise and Fall Times (10% to 90%)			1.0	μs	
t_{DS}	Data Input Setup Time	150			ns	
t_{DH}	Data Input Hold Time	100			ns	
t_D	Delay to Output		100	200	ns	C_L = 10 pF Load = 1 TTL Input
t_{RS}	Recirculate Set-Up Time	150			ns	
t_{RH}	Recirculate Hold Time	100			ns	
C	Capacitance (All inputs Including Clock)		3.0	5.0	pF	V_ϕ = V_{SS}, f=1.0MHz

NOTES:

3. These parameters apply to all inputs including data inputs, recirculate inputs, and clock input.
4. On chip pull up resistors are provided on all inputs to effect the proper logic level when driving with TTL/DTL.
5. The outputs remain good until a new output appears.
6. Outputs remain valid until negative going edge of next pulse.

WAVEFORM



3348
HEX 32-BIT STATIC SHIFT REGISTER (WITH OUTPUT ENABLE)
3349
HEX 32-BIT STATIC SHIFT REGISTER

GENERAL DESCRIPTION — The 3348 and the 3349 contain six separate 32-Bit Static Shift Registers constructed in a single chip using P-channel enhancement mode silicon gate MOS technology. Only two power pins, V_{SS} and V_{GG}, are needed for circuit operation.

An on chip clock generator provides all internal clock phases from a single TTL clock pulse. All inputs are directly TTL compatable without the addition of external components. Each output is a bare drain, and therefore requires a 7.5 kΩ pull down resistor to V_{GG}.

A recirculate data input allows the user to either enter data from the outside (LOW logic level) or to internally recirculate the contents of the registers (HIGH logic level).

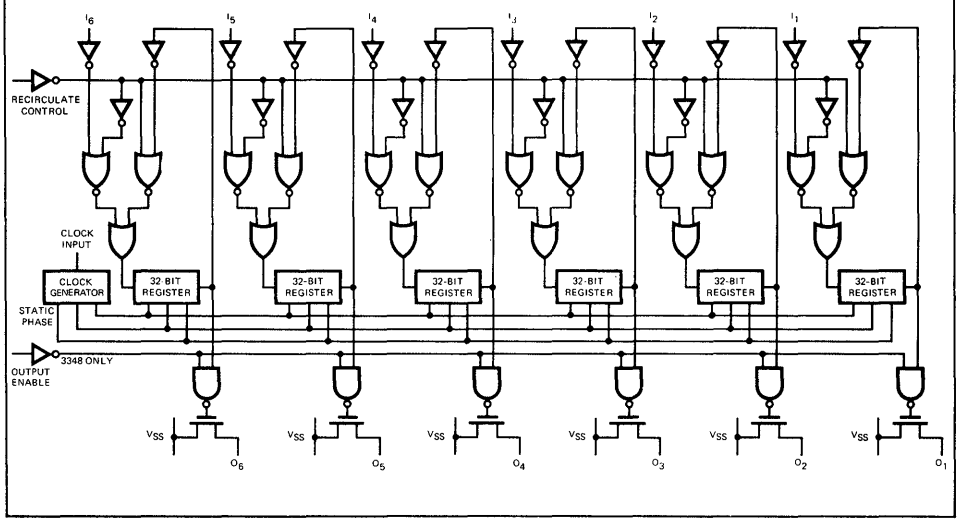
The 3349 is available in a 16-lead and the 3348 is available in a 24-lead Dual In-Line package. The 3348 option provides an output disable pin for wired-OR operation. The outputs are disabled when this pin is at a HIGH level.

- **SINGLE TTL EXTERNAL CLOCK**
- **SINGLE POWER SUPPLY OPERATION**
- **INTERNAL RECIRCULATION CONTROL**
- **DC TO 1 MHz OPERATION GUARANTEED**
- **INPUT OVERVOLTAGE PROTECTION**
- **DUAL PACKAGE OPTION**
- **OUTPUT DISABLE CONTROL – 3348**
- **LOW CLOCKLINE CAPACITANCE**
- **SINGLE ENDED (BARE DRAIN) BUFFERS**
- **DTL/TTL COMPATABLE INPUTS**
- **CASCADE CAPABILITY**

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

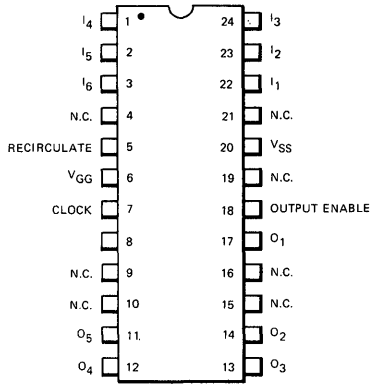
All Inputs	V_{SS} −22 V to V_{SS} + 0.3 V
V_{GG}	V_{SS} −22 V to V_{SS} + 0.3 V
Output Current	+10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +85°C

FUNCTIONAL BLOCK DIAGRAM

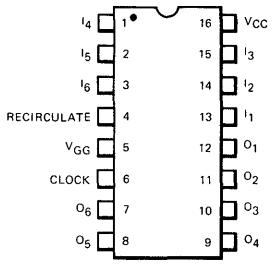


CONNECTION DIAGRAMS
(TOP VIEWS)

3348



3349



FUNCTIONAL DESCRIPTION — The 3348/3349 is a 2-phase static shift register. The single external clock phase generates two shift phases as well as a static operation phase via the on chip clock generator. Data is accepted at the inputs after the negative going transition of the external clock. Output information is available after the positive clock transition as illustrated in Figure 1. For long term storage, the external clock should be held HIGH.

DC CHARACTERISTICS: V_{SS} = 5 V ± 5%, V_{GG} = −12 ± 1 V, T_A = 0°C to 85°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS}−1.7			V	All Inputs Including Clocks
V_{IL}	Input Voltage LOW			0.6	V	All Inputs Including Clocks
V_{OH}	Output Voltage HIGH	4.0			V	7500Ω load to V_{GG}
						V_{SS} = 4.75 V, V_{GG} = −11 V
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = 0 V
I_{GG}	V_{GG} Current			27	mA	V_{GG} = −12 V, V_{SS} = 5 V
R_L	Output Load Resistor to V_{GG}	7500			Ω	

AC CHARACTERISTICS: V_{SS} = 5 V ± 5%, V_{GG} = −12 ± 1 V, T_A = 0°C to 85°C

SYMBOL		MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Shift Frequency			1.0	MHz	
$t_{\phi PWL}$	Clock LOW Level Width	0.35			μs	
$t_{\phi WH}$	Clock HIGH Level Width	0.6			μs	
t_r, t_f	Clock Rise Time and Fall Time			5.0	μs	
t_{DS}	Input Data Set Up Time	180			ns	
t_{DH}	Input Data Hold Time	50			ns	
t_{RPW}	Recirculate Pulse Width	350			ns	
t_{RS}	Recirculate Set Up Time	225			ns	
t_{RH}	Recirculate Hold Time	100			ns	
t_D	Clock to Data Out Delay	50		520	ns	C_L = 0 to 20 pF, R_L = 7.5 kΩ
t_{DOE}	Output Enable Time (3348 Only)			200	ns	C_L = 20 pF, R_L = 7.5 kΩ to V_{GG}
t_{DOD}	Output Disable Time (3348 Only)			200	ns	

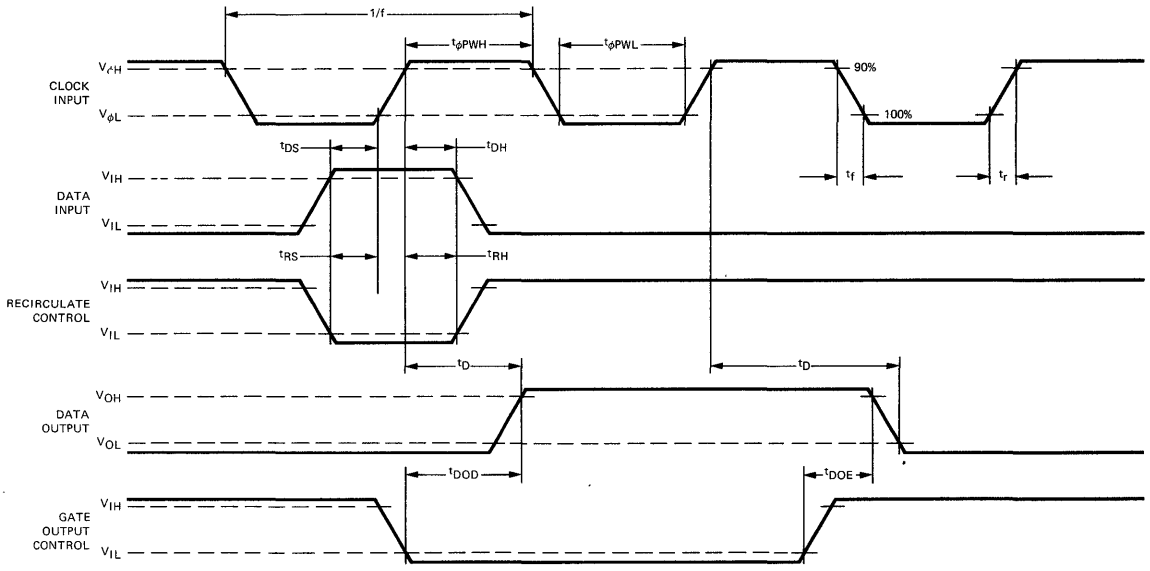


Fig. 1. 3348/3349 I/O TIMING DIAGRAM AND VOLTAGE WAVEFORMS

3383

256-BIT DYNAMIC SHIFT REGISTER WITH RECIRCULATE

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3383 is a single 256-Bit 2-Phase Dynamic Shift Register. It is a monolithic integrated circuit utilizing P-channel enhancement mode silicon gate MOS technology. Data select (pin 3) allows data to be either entered externally or recirculated from the device output without external wiring. On chip input resistors allow direct bipolar compatibility by tying the V_P pin to V_{DD}. The output buffer is capable of driving both MOS and bipolar loads directly without addition of an external resistor.

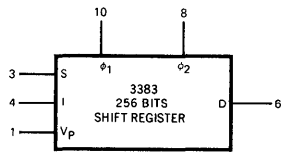
- **DIRECT BIPOLAR COMPATIBILITY**
- **2 MHz OPERATION**
- **25 pF CLOCKLINE CAPACITANCE**
- **0.6 mW/BIT MAX. POWER DISSIPATION AT 2 MHz**
- **INPUT OVERVOLTAGE PROTECTION**
- **10-LEAD TO-100 PACKAGING**

ABSOLUTE MAXIMUM RATINGS

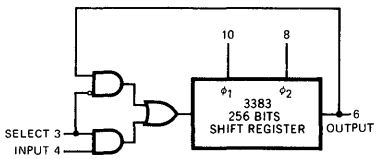
All Inputs [ϕ_1, ϕ_2, V_P, Input, Select] (Notes 1 & 3)	−24 V to +0.3 V
V_{GG} (Note 3)	−24 V to +0.3 V
V_{DD} and Data Output (Note 3)	−7.0 V to +0.3 V
Output LOW Current (Note 2)	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

Note 1. V_P must be tied to V_{SS} if data input or select is between −7.0 V and −24 V.
2. LOW logic level is the most negative level and HIGH logic level is the most positive level.
3. All Voltages with respect to V_{SS}.

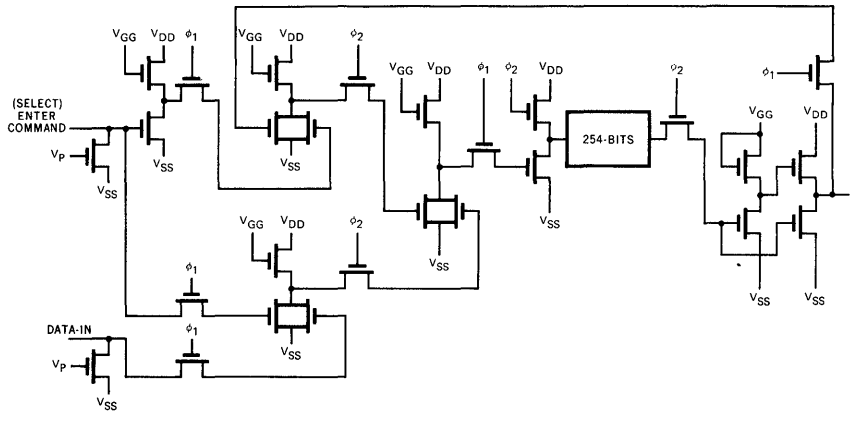
LOGIC SYMBOL



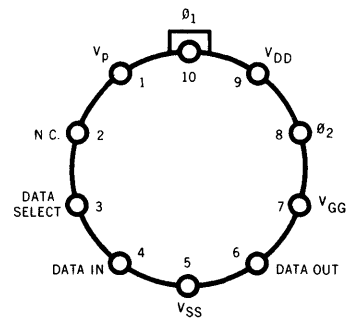
LOGIC DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION – The 3383 is a straight pipeline 2-phase dynamic shift register with a recirculate control. The clock functions ϕ_1 and ϕ_2 are non-overlapping negative pulses as illustrated in Figure 1. Data is accepted on the input and select lines when ϕ_1 is negative and data is available at the output when ϕ_2 is negative. The data in and select lines are connected by an MOS transistor to V_{SS}; these transistors act as externally controlled pull up resistors allowing complete TTL compatibility. The output stage is push/pull and can sink one TTL load to V_{DD} (1.6 mA at 0.4 V). Bipolar compatible opeation is achieved by connecting V_{SS} to +5.0 V, V_{DD} to 0 V, and V_{GG} to −12 V, with V_P, the control pin to the pull up resistors, tied to V_{DD}. For driving the input with MOS, the V_P pin should be connected to V_{SS}.

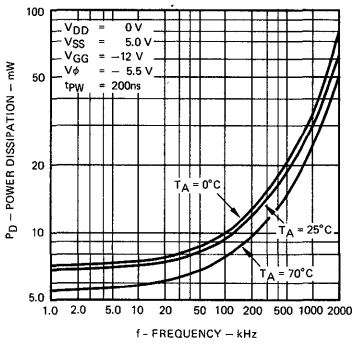
DC CHARACTERISTICS: V_{SS} = +5.0 V ± 10%, V_{DD} = 0 V, V_{GG} = −12.0 V ± 10%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}*	Input (Select) Voltage HIGH	V_{SS}−1		V_{SS}	V	$V_P = V_{SS}$ if V_{IH} is negative
V_{IL}*	Input (Select) Voltage LOW	V_{GG}		+0.8	V	
$V_{\phi H}$	Clock Voltage HIGH	V_{SS}−1		V_{SS}	V	
$V_{\phi L}$	Clock Voltage LOW	−6.5		−4.5	V	
V_{OH}	Output Voltage HIGH	V_{SS}−0.6		V_{SS}	V	V_{SS} = +4.5 V, I_{OH} = −0.5 mA
V_{OL}	Output Voltage LOW	0	0.24	+0.4	V	V_{SS} = +5.5 V, I_{OL} = 1.6 mA
I_{IH}*	Input (Select) Current HIGH	0.17			mA	$V_I = V_{SS}$ −1, $V_P = V_{DD}$
I_{IL}*	Input (Select) Current LOW		1.0	1.6	mA	V_I = +0.4 V, $V_P = V_{DD}$
$I_{IL(ISL)}$	Input (Select) Current LOW			1.0	μA	V_I = −5 V, $V_P = V_{SS}$, T_A = 25°C
$I_{L\phi}$	Clock Input Leakage			1.0	μA	V_ϕ = −10 V, T_A = 25°C
R_{OH}	Output Impedance HIGH		0.7	1.0	kΩ	$V_O = V_{SS}$ −0.5 V
R_{OL}	Output Impedance LOW		150	250	kΩ	$V_O = V_{OL}$
I_{GG}	V_{GG} Current		2.4	3.0	mA	V_{SS} = +5.5 V
I_{DD}	V_{DD} Current		14.0	18.0	mA	V_{GG} = −13.2 V
I_{SS}	V_{SS} Current		16.4	21.0	mA	V_{OL} = −6.5 V
P_D	Power Dissipation		125	155	mW	T_A = +25°C, f = 2.0 MHz t_{PW} = 200 ns

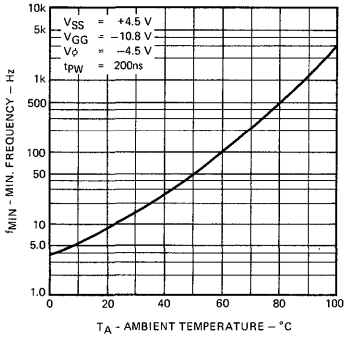
*All input voltages and currents pertain both to the data select pin and the data input.

TYPICAL ELECTRICAL CHARACTERISTICS

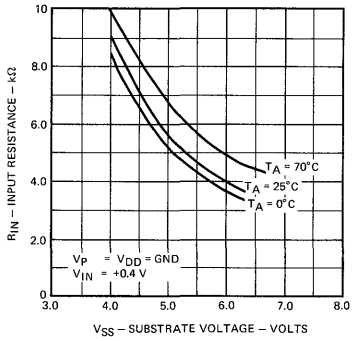
POWER DISSIPATION VERSUS FREQUENCY



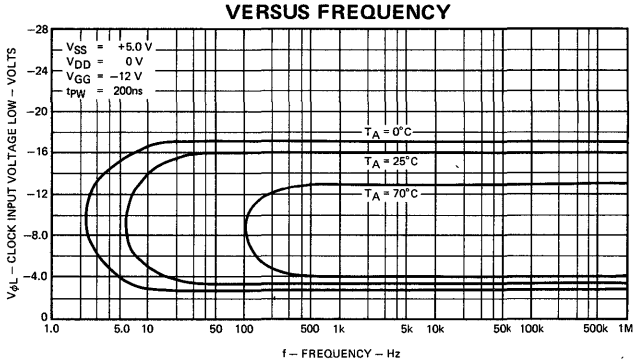
MINIMUM FREQUENCY VERSUS AMBIENT TEMPERATURE



INPUT RESISTANCE VERSUS SUBSTRATE VOLTAGE



CLOCK INPUT VOLTAGE LOW VERSUS FREQUENCY



AC CHARACTERISTICS: V_{SS} = +5.0 V ± 10%, V_{DD} = 0 V, V_{GG} = −12.0 V ± 10%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Max. Operating Frequency	.010		2.0	MHz	
t_{PW}	Clock Pulse Width	0.2		100	μs	Note 4
$t_{D\phi}$	Time Between Clocks	0		100	μs	Note 4
t_r, t_f	Clock Rise and Fall Times (10% - 90%)			1.0	μs	
t_{DS}**	Data Set-Up Time	100			ns	
t_{DH}**	Data Hold Time	0			ns	
t_D	Delay from ϕ_2 to Output			150	ns	C_L = 10 pF Load = 1 TTL Input
$C\phi$	Clock Capacitance (Each Clock Line)			25	pF	$V\phi = V_{SS}$, f = 1 MHz

**All input timing conditions also pertain to the data select pin.
Note 4: Maximum cycle time ($2\ t_{PW} + 2\ t_{D\phi S}$) = 100 μs.

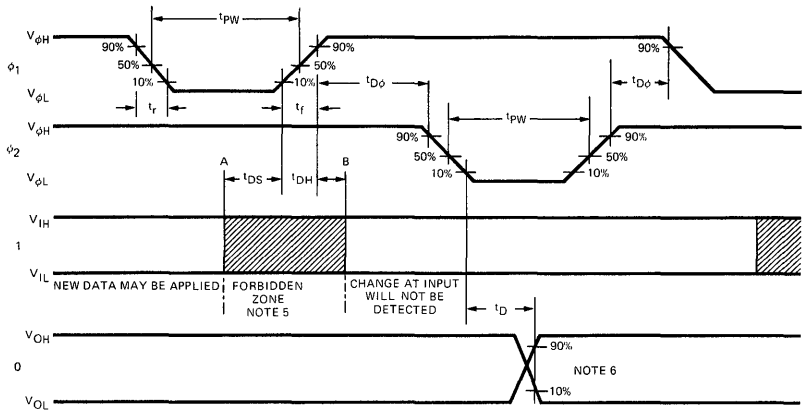


Fig. 1 TIMING DIAGRAM

Note 5: A and B define a window during which the input to the shift register is setting up. If input or select data changes during this window, the change will not be detected. To avoid this condition, information must remain good between A and B.

Note 6: The outputs remain good until a new output appears.

APPLICATIONS

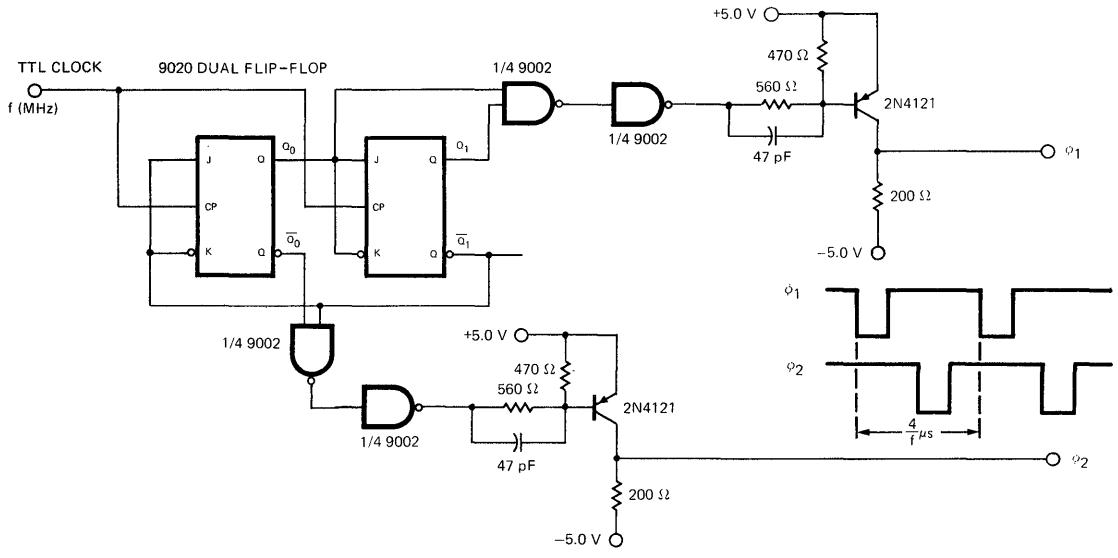


Fig. 2 2-PHASE NON-OVERLAPPING CLOCK GENERATOR

The counter states 11 and 00 are decoded to produce −5 V clock pulses.

APPLICATIONS (Cont'd)

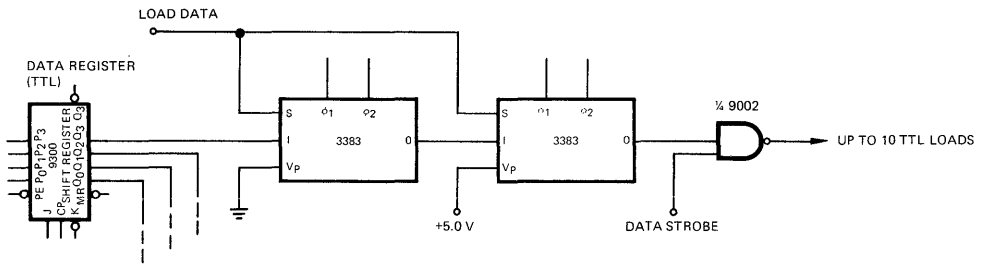


Fig. 3 SHIFT REGISTER INTERFACE

The shift register inputs may be connected directly to a TTL or DTL output if V_P is tied to ground (V_{DD}). If the inputs are to be driven by a silicon gate MOS output, V_P is tied to V_{SS}. The output can drive TTL or DTL directly without external components.

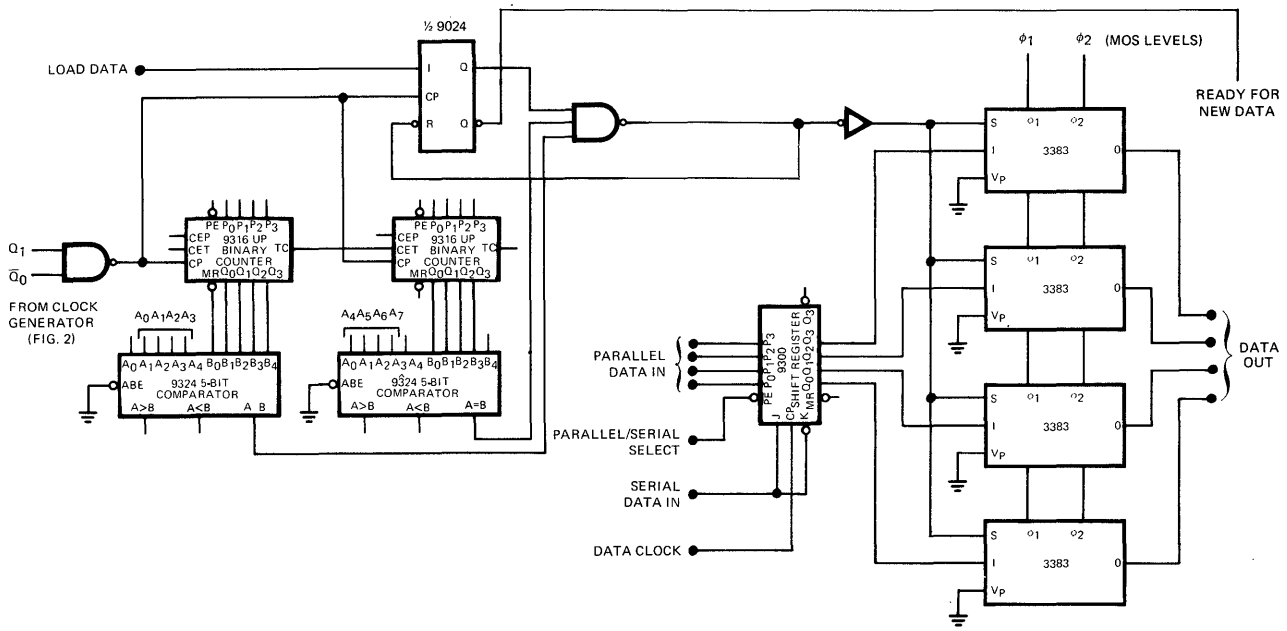


Fig. 4 256W X 4B SEQUENTIAL MEMORY

256 4-bit words are stored in the shift registers. The two 9316's keep track of address locations in the shift registers. New data is loaded into the 9300 data register, either in serial or parallel. When the data is ready in the 9300, the Data Ready line is HIGH for one cycle, setting the 9024 flip-flop. The address for the new data is applied at A_0 - A_7 on the comparator. When the address comes up on the counters, the shift register select input switches to accept the new data, and the data flip-flop is reset.

3512
2048-BIT READ ONLY MEMORY
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3512 is a 2048-bit Read Only Memory organized in a 256-word by 8-bit format. It is an MOS monolithic integrated circuit utilizing P-channel enhancement mode silicon gate technology.

- **STATIC – NO CLOCK REQUIRED**
- **INTERFACES DIRECTLY WITH TTL – NO EXTERNAL COMPONENTS**
- **400 ns TYPICAL ACCESS TIME**
- **4-BIT PROGRAMMABLE CHIP SELECT CODE**
- **WIRED–OR CAPABILITY ON OUTPUTS**

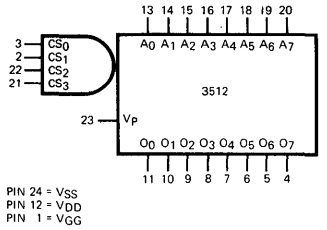
APPLICATIONS

Code Conversion
Micro Programming
Table Lookup
Control Logic

ABSOLUTE MAXIMUM RATINGS

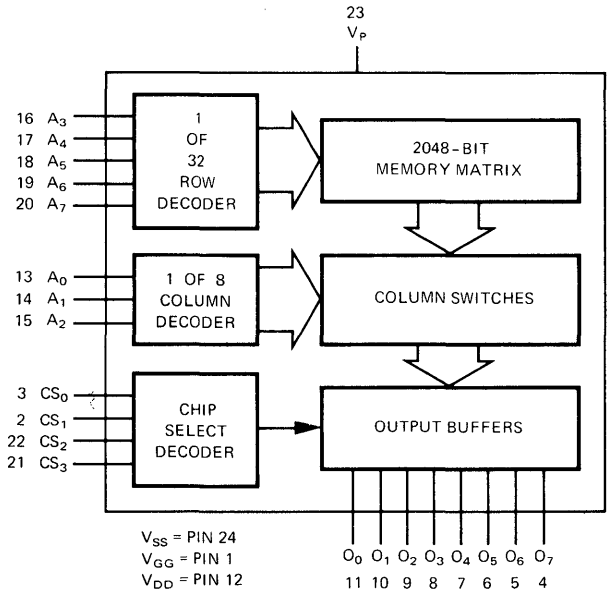
Storage Temperature (T_S)	–65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C
Voltage on any Pin (V_{SS} = GND)	–20 V to +0.3 V

LOGIC SYMBOL

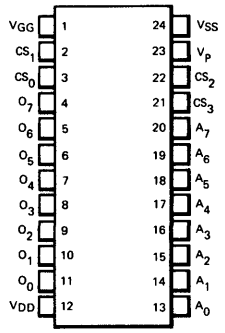


V_{SS} = Pin 24
V_{GG} = Pin 1
V_{DD} = Pin 12

LOGIC BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – An 8-bit binary address presented at the address inputs (A_0–A_7) will cause a corresponding 8-bit word to appear on the data outputs (O_0–O_7). The 4-bit programmable chip select allows expansion up to sixteen memories with no additional gates. When a chip is not selected, its outputs turn off, i.e., go to a high dc impedance state. This feature allows up to 16 devices to be wired–OR without adding any external pull up resistors. The outputs of the device can drive 1.5 TTL loads, so one standard TTL input or 6 low power TTL inputs may be driven directly by the silicon gate output.

Internal pull up resistors are provided on all the input lines to the 3512. These pull the inputs up to V_{IH} in the HIGH state. For the Chip Select inputs, the internal resistors are controlled by pin V_P. There is an MOS transistor connected between each Chip Select input and V_{SS}. The transistor gates are connected to V_P, so when $V_P = V_{GG}$ the transistors are on, providing a pull up impedance of around 10 kΩ to V_{SS}.

When $V_P = V_{SS}$, the transistors are off and the Chip Select inputs are at a high impedance, presenting virtually no dc load. Ordinarily a set of lines will go to the chip selects of a number of devices in parallel. The V_P on one will be tied to V_{GG} and the V_P on the others will be tied to V_{SS}. This scheme provides a single internal pull up resistor for each chip select line so that dc loading does not increase when chip select inputs are paralleled. There is a programmed option for the internal pull up resistors on the address inputs. If the option is chosen, then pull ups on the address inputs are enabled whenever the chip is selected. That is, the chip select controls the gates of the pull up transistors on the address lines. If this option is not requested, the address lines will be ordinary silicon gate inputs, with no pull up resistors.

Three types of information are to be provided by the customer when ordering the 3512. First, the bit patterns to be stored in the 256 words of memory; second, the state of the 4-chip select inputs which enable the chip; third, whether or not the address inputs are to be pulled up when the chip is selected.

DC CHARACTERISTICS: V_{SS} = +5.0 V ± 5%, V_{DD} = 0 V, T_A = 0°C to 70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS}–1V		V_{SS}	V	I_{IH} Address Inputs = –100 μA I_{IH} Chip Select Inputs = –50 μA See Note 1 & Figs. 11 & 12
V_{IL}	Input Voltage LOW	V_{GG}	0.3	0.8	V	I_{IL} Address Inputs = –24 mA I_{IL} Chip Select Inputs = –1.0 mA See Note 2 & Figs. 11 & 12
V_{OH}	Output Voltage HIGH	2.4	4.0	V_{SS}	V	I_{OH} = –0.5 mA, Note 3
		V_{SS}–1V			V	I_{OH} = –10 μA, Note 3
V_{OL}	Output Voltage LOW	0	0.3	0.4	V	I_{OL} = 2.4 mA, Note 4
I_{LI}	Input Leakage Current		0.02	1.0	μA	V_{IN} = –10 V, $V_P = V_{SS}$, Note 5
I_{LO}	Output Leakage Current		0.02	1.0	μA	V_{OUT} = 0 V, Note 6
I_{DD}	V_{DD} Current		–15	–22	mA	Outputs Open Inputs 0 V
I_{GG}	V_{GG} Current		–30	–43	mA	
I_{SS}	V_{SS} Current		60	88	mA	
P_D	Power Dissipation		700	1000	mW	

NOTES:
1. I_{IH} = Current out of the input at $V_{IN} = V_{SS}$–1V
2. I_{IL} = Current out of the input at V_{IN} = 0 V
3. I_{OH} = Current out of output.
4. I_{OL} = Current into output
5. All pins at V_{SS} except pin under test
6. Chip not selected

AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{GG} = –12 V ±5%, V_{DD} = 0 V, T_A = 0°C to 70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{DAO+}	Access Time Address to Output HIGH		400	600	ns	Notes 1 & 2
t_{DAO-}	Access Time Address to Output LOW		350	600	ns	Notes 1 & 2
t_E	Chip Select Enable to Output Access Time		350	500	ns	Notes 1 & 2
$t_{\overline{E}}$	Chip Select Disable to Output Access Time		350	500	ns	Notes 1 & 2
C_I	Input Capacitance		10	15	pF	f = 1.0 MHz, 0 V Bias
C_O	Output Capacitance		10	15	pF	f = 1.0 MHz, 0 V Bias

NOTES:
1. See access time test circuit, Fig. 14
2. See timing diagram and characteristic curves.

ELECTRICAL CHARACTERISTICS

ACCESS TIME VERSUS SUPPLY VOLTAGE

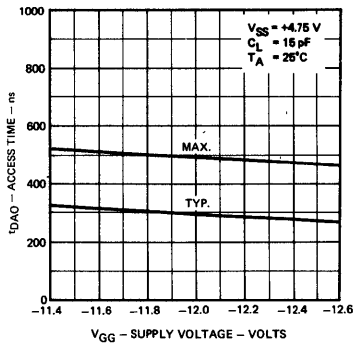


Fig. 1

ACCESS TIME VERSUS AMBIENT TEMPERATURE

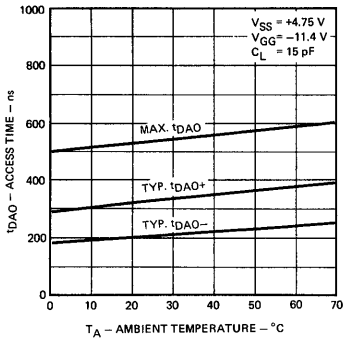


Fig. 2

ACCESS TIME VERSUS LOAD CAPACITANCE

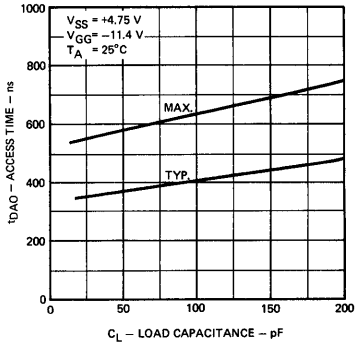


Fig. 3

V_{SS} CURRENT VERSUS AMBIENT TEMPERATURE

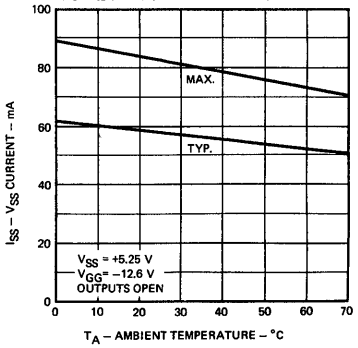


Fig. 4

V_{GG} CURRENT VERSUS AMBIENT TEMPERATURE

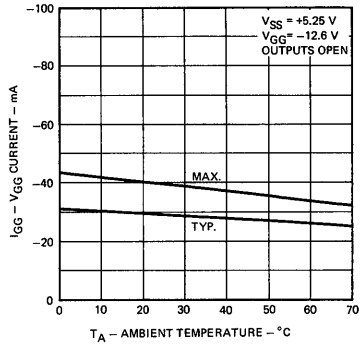


Fig. 5

V_{DD} CURRENT VERSUS AMBIENT TEMPERATURE

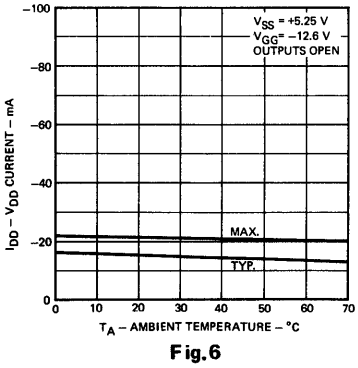


Fig. 6

OUTPUT VOLTAGE HIGH VERSUS OUTPUT HIGH CURRENT

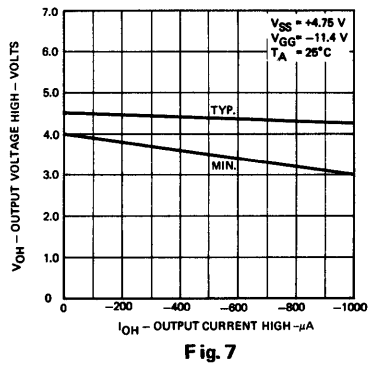


Fig. 7

OUTPUT VOLTAGE HIGH VERSUS AMBIENT TEMPERATURE

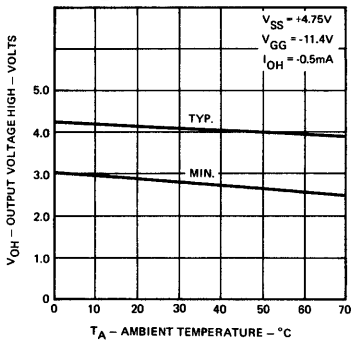


Fig. 8

OUTPUT VOLTAGE LOW VERSUS OUTPUT LOW CURRENT

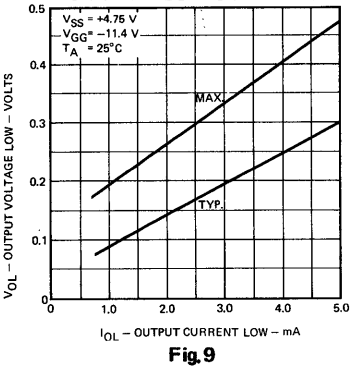


Fig. 9

OUTPUT VOLTAGE LOW VERSUS AMBIENT TEMPERATURE

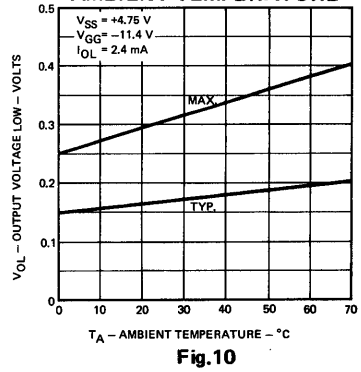
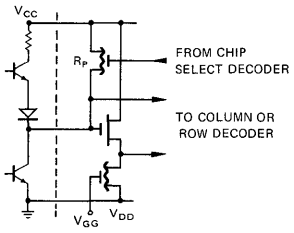


Fig. 10

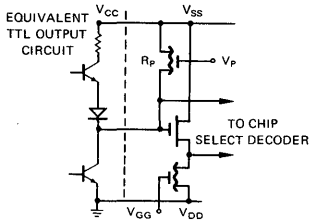
TYPICAL ADDRESS INPUT



R_P is enabled if the input pull up option is chosen and if chip is selected.
R_P is disabled if the input pull up option is not chosen or if the input pull up is chosen and the chip is not selected.

Fig. 11

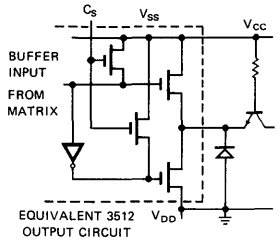
TYPICAL CHIP SELECT INPUT



R_P is enabled if $V_P = V_{GG}$, disabled if $V_P = V_{SS}$.

Fig. 12

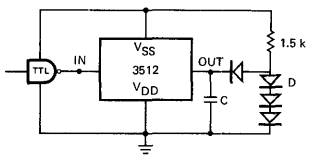
EQUIVALENT 3512 OUTPUT CIRCUIT



If chip is selected voltage $C_S = V_{SS}$, output = the programmed bit.
If chip is not selected, voltage $C_S = V_{GG} - VT$ removing the gate voltage from both output devices causing the output to float.

Fig. 13

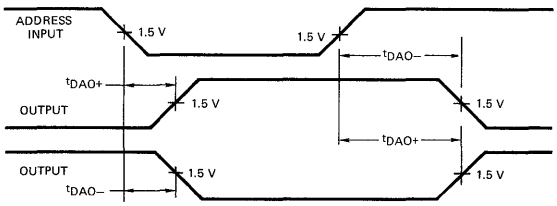
ACCESS TIME TEST CIRCUIT

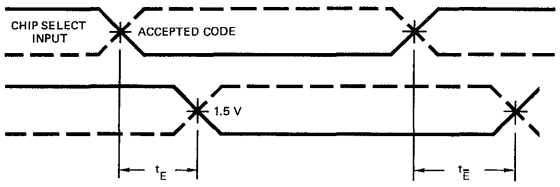


$C \leq 15$ pF TOTAL FIXTURE CAPACITANCE.
D = 1N3063 OR EQUIVALENT.

Fig. 14

TIMING DIAGRAM





CUSTOM PATTERN ORDERING INFORMATION — The 3512 is programmed on IBM cards or IBM coding form in the coding format shown below.
A logic "1" = a more positive voltage, nominally +5 V
A logic "0" = a more negative voltage, normally 0 V

FIRST CARD

Column Number	Description
29	CS_3 input required to select chip
31	CS_2 input required to select chip
33	CS_1 input required to select chip
35	CS_0 input required to select chip
37	Address input pull up enable. A logic "1" in this column will enable a 4K MOS pull up device to V_{SS} whenever the chip is selected by the chip select code above.

REMAINING 256 CARDS

Column Number	Description
10, 12, 14, 16, 18, 20, 22, 24	Address input pattern. The most significant bit (A_7) is in column 10.
40, 42, 44, 46, 48, 50, 52, 54	Output pattern. The most significant bit (O_7) is in column 40.
73, 74, 75, 76, 77, 78, 79, 80	Coding these columns is not essential and may be used for card identification purpose.

GLOSSARY OF TERMS:

1. V_{SS}: The most positive voltage applied to the device.
2. V_{GG}: The most negative voltage applied to the device.
3. V_{DD}: The next most negative voltage applied to the device.
4. Address access time:
   - t_{DAO+} The time delay from an address input logic HIGH or logic LOW state to an output logic HIGH state.
   - t_{DAO-} The time delay from an address input logic HIGH or logic LOW state to an output logic LOW state.
5. t_E: Chip eanble time. The time delay from valid code at Chip Select inputs to an output logic HIGH or logic LOW state.
6. $t_{\bar{E}}$: Chip disable time. The time delay from removal of a valid chip select input code to a high impedance state on outputs.
7. T_A: Still air ambient temperature.

3512A

SELECTRIC TO ASCII/ASCII TO SELECTRIC CODE CONVERTER

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3512A is a preprogrammed version of the 3512 Read Only Memory containing the complete code conversion matrix necessary to convert from both ASCII to Selectric Line code and Selectric Line code to ASCII. Upon application of any 7-bit address of either code, the corresponding 7-bit word appears at the ROM outputs. The eighth output O_7 is the odd parity bit for the seven address inputs.

- **STATIC – NO CLOCK REQUIRED**
- **INTERFACES DIRECTLY WITH TTL – NO EXTERNAL COMPONENTS**
- **400 ns TYPICAL ACCESS TIME**
- **WIRED–OR CAPABILITY ON OUTPUTS**

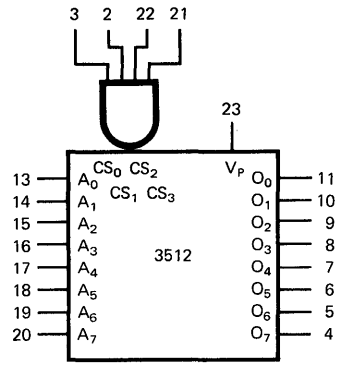
ABSOLUTE MAXIMUM RATINGS

Storage Temperature (T_S)	−65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C
Voltage on any Pin (V_{SS} = GND)	−20 V to +0.3 V

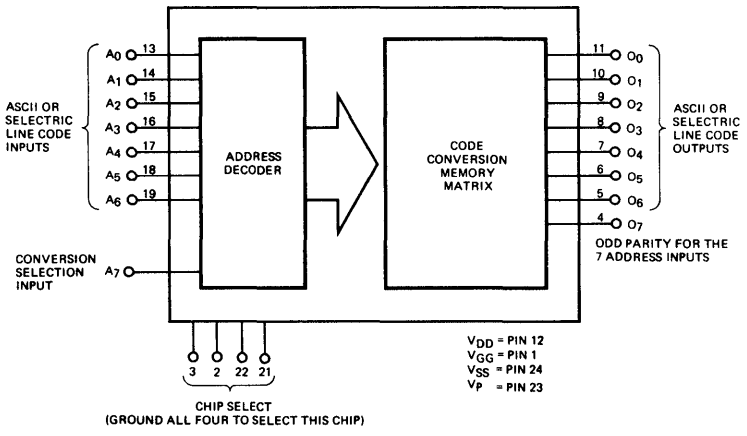
APPLICATIONS

Code Conversion

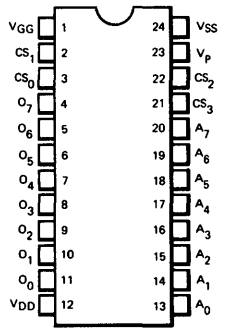
LOGIC SYMBOL



LOGIC BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION – The 3512A contains the complete code conversion bit pattern to convert any 7-bit ASCII or Selectric Line code input to its corresponding Selectric Line code or ASCII 7-bit output. Addresses A_0 through A_6 and outputs O_0 through O_6 correspond to the 2 basic codes as follows:

ROM ADDRESS INPUT	ASCII BIT	SELECTRIC BIT	ROM OUTPUT
A_0	b_1	1	O_0
A_1	b_2	2	O_1
A_2	b_3	4	O_2
A_3	b_4	8	O_3
A_4	b_5	A	O_4
A_5	b_6	B	O_5
A_6	b_7	S	O_6

Address input A_7 establishes which code conversion is to be performed:
A_7 = Logic 0 – Selectric Line code input to ASCII output
A_7 = Logic 1 – ASCII input to Selectric Line code output

Output O_7 gives the odd parity for the eight address input lines. V_P (Pin 23) tied to ground as are the four chip selects (Pins 2, 3, 22, 21).

ASCII TO SELECTRIC LINE CODE A_7 = "0"

A	SL	A	SL	A	SL	A	SL	A	SL	A	SL	A	SL	A	SL
NUL	IL1	DLE	PRE2	SPACE	SPACE1	0	0	@	@	P	P	\	1	p	p
SOH	b	DC1	RS2	!	!	1	1	A	A	Q	Q	a	a	q	q
STX	9	DC2	PN1	"	"	2	2	B	B	R	R	b	b	r	r
ETX	E0B1	DC3	RS1	#	#	3	3	C	C	S	S	c	c	s	s
EOT	E0T1	DC4	PF1	$	$	4	4	D	D	T	T	d	d	t	t
ENQ	UC2	NAK	!	%	%	5	5	E	E	U	U	e	e	u	u
ACK	-	SYN	IL2	&	&	6	6	F	F	V	V	f	f	v	v
BEL	LC1	ETB	E0B2	1	1	7	7	G	G	W	W	g	g	w	w
BS	BS1	CAN	!	(	(	8	8	H	H	X	X	h	h	x	x
HT	HT1	EM	RES1	)	)	9	9	I	I	Y	Y	i	i	y	y
LF	LF1	SUB	BY1	*	*	!	!	J	J	Z	Z	j	j	z	z
VT	②	ESC	PRE1	+	+	;	;	K	K	[	±	k	k	[	±
FF	⑤	FS	BY2	,	,	<	0	L	L	\	±	l	l	:	±
CR	NL1	GS	RES2	-	-	=	=	M	M	]	±	m	m	}	±
SO	UC1	RS	RES2	.	.	>	¢	N	N		±	n	n	~	±
SI	LC2	US	BY2	/	/	?	?	O	O	–	–	o	o	DEL	DEL 1

SELECTRIC LINE CODE TO ASCII A_7 = "1"

SL	A	SL	A	SL	A	SL	A	SL	A	SL	A	SL	A	SL	A
SPACE 1	SPACE	+	+	!	!	j	j	SPACE 2	SPACE	T	T	°	<	J	J
1	1	x	x	m	m	g	g	±	]	X	X	M	M	G	G
2	2	n	n	.	.	=	=	@	@	N	N	.	.	+	+
3	3	u	u	v	v	f	f	#	#	U	U	V	V	F	F
5	5	e	e	1	/	p	p	%	%	E	E	"	"	P	P
7	7	d	d	r	r	;	;	&	&	D	D	R	R	:	:
6	6	k	k	i	i	q	q	¢	>	K	K	I	I	Q	Q
8	8	c	c	a	a	'	'	*	*	C	C	A	A	'	'
4	4	l	l	o	o	/	/	$	$	L	L	O	O	?	?
0	0	h	h	s	s	y	y	)	)	H	H	S	S	Y	Y
z	z	1	RS	2	VT	3	RS	Z	Z	4	RS	5	FF	6	RS
9	9	b	b	w	w	-	-	(	(	B	B	W	W	-	-
PN1	DC2	BY1	SUB	RES1	EM	PF1	DC4	PN2	DC2	BY2	FS	RES2	GS	PF2	DC4
RS1	DC3	LF1	LF	NL1	CR	HT1	HT	RS2	DC1	LF2	LF	NL2	CR	HT2	HT
UC1	SO	EOB	ETX	BS1	BS	LC1	BEL	UC2	ENQ	EOB2	ETB	BS2	BS	LC2	SI
EOT1	EOT	PRE	ESC	IL1	NUL	DEL1	DEL	EOT2	EOT	PRE2	DLE	IL2	NUL	DEL2	NUL

3513

2560-BIT READ ONLY MEMORY

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3513 is a mask programmable, static, Read Only Memory, organized 256 words by ten bits. Both inputs and outputs are compatible with bipolar logic devices. There is also a customer programmable 3-bit Chip Select which allows simple expansion of the system. The 3513 is fabricated with P-channel enhancement mode silicon gate MOS technology.

- **INTERFACE DIRECTLY WITH TTL – NO EXTERNAL COMPONENTS**
- **500 ns TYPICAL ACCESS TIME**
- **3-BIT PROGRAMMABLE CHIP SELECT CODE**
- **WIRED-OR CAPABILITY ON OUTPUTS**

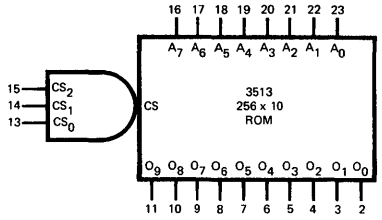
ABSOLUTE MAXIMUM RATINGS

Storage Temperature (T_S)	−55°C to +150°C
Operating Temperature (T_A)	0°C to +70°C
Voltage on Any Pin Relative to V_{SS}	−25 V to +0.3 V

APPLICATIONS

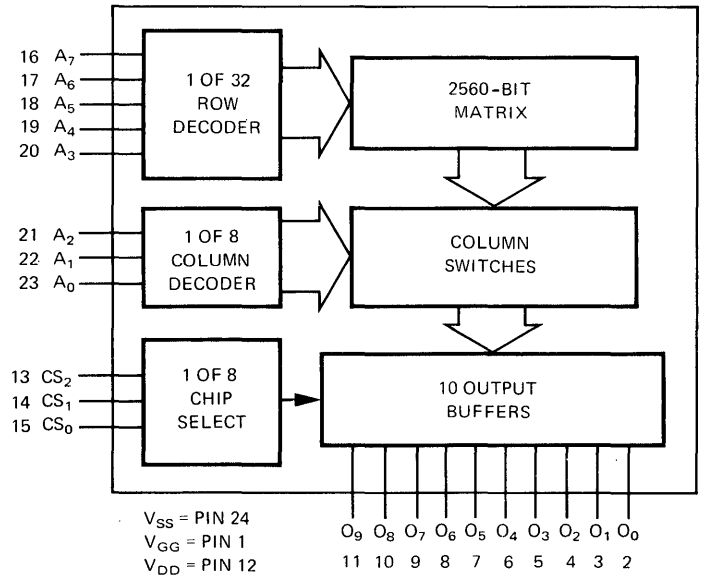
- Code Conversion
- MICRO Programming
- Table Look up
- Control Logic

LOGIC SYMBOL



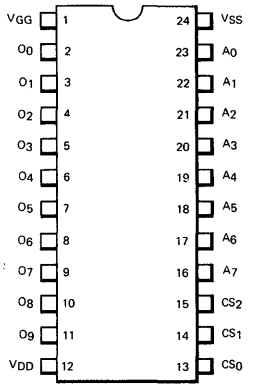
V_{SS} = PIN 24
V_{GG} = PIN 1
V_{DD} = PIN 12

LOGIC BLOCK DIAGRAM



V_{SS} = PIN 24
V_{GG} = PIN 1
V_{DD} = PIN 12

CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION – The 3513 decodes an 8-bit address (A_0–A_7) into 256 addresses, each of which access ten bits of stored information. The first three bits of the input address turn on one of eight column switches to each of the ten matrix segments containing the stored information for each output bit. The remaining addresses (A_3 through A_7) select the row (1 of 32) which contains the specific bits. The active level of the chip select inputs (CS_0 through CS_2) may be programmed with a custom pattern for use in multichip memories. When the chip is not selected, the output goes to a high impedance state thereby allowing OR tying.

DC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0°C to 70°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS} −2.75		V_{SS}	V	
V_{IL}	Input Voltage LOW	V_{GG}		0.55	V	
V_{OH}	Output Voltage HIGH	2.4		V_{SS}	V	I_{OH} = −90 μA
V_{OL}	Output Voltage LOW	0		0.15	V	I_{OL} = 10 μA
V_{OL}	Output Voltage LOW	0		0.40	V	I_{OL} = 2.4 mA
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = −10 V, Notes 1 and 2
I_{LO}	Output Leakage Current			1.0	μA	V_{OUT} = −6 V, Notes 1 and 2
I_{DD}	V_{DD} Current		1.0	3.0	mA	Output Open
I_{GG}	V_{GG} Current		39	57	mA	
I_{SS}	V_{SS} Current		40	60	mA	
P_D	Power Dissipation		680	1070	mW	See Fig. 2

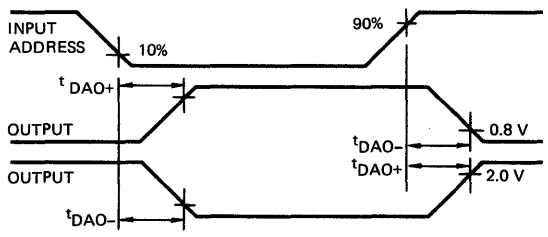
NOTES:
1. All pins at zero volts except that under test.
2. Chip not selected.

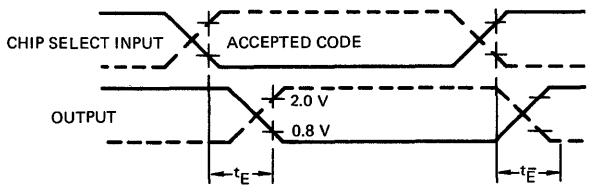
AC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0°C to 70°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{DAO+}	Access Time from Address to Output HIGH	200	500	850	ns	Notes 3 and 4
t_{DAO-}	Access Time from Address to Output LOW	200	500	850	ns	Notes 3 and 4
t_E	Chip Select Enable to Output	200	500	850	ns	Notes 3 and 4
$t_{\overline{E}}$	Chip Select Disable to Output Disable	200	500	850	ns	Notes 3 and 4
C_I	Input Capacitance			8.0	pF	$V_I = V_{IH}$,
C_O	Output Capacitance			15	pF	$V_O = V_{OH}$,

NOTES:
3. A standard load of one TTL.
4. See timing diagram and characteristic curves.

TIMING DIAGRAM





TYPICAL ELECTRICAL CHARACTERISTICS

Fig. 1
ACCESS TIME VERSUS SUPPLY VOLTAGE

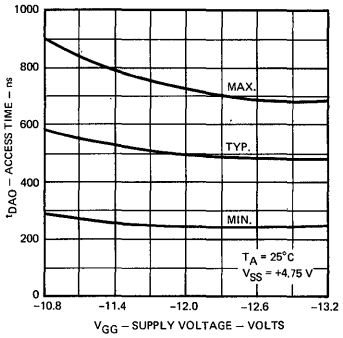


Fig. 2
ACCESS TIME VERSUS AMBIENT TEMPERATURE

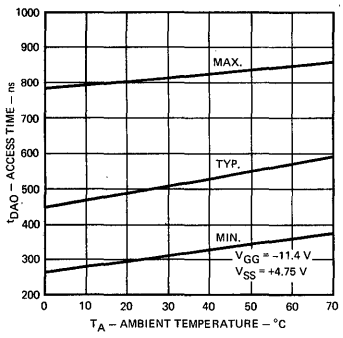


Fig. 3
SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE

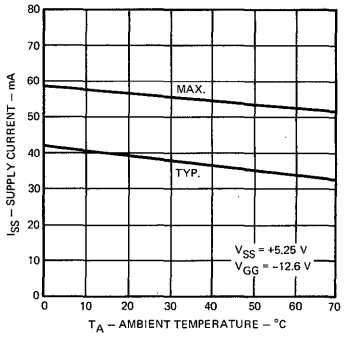


Fig. 4
ACCESS TIME VERSUS LOAD CAPACITANCE

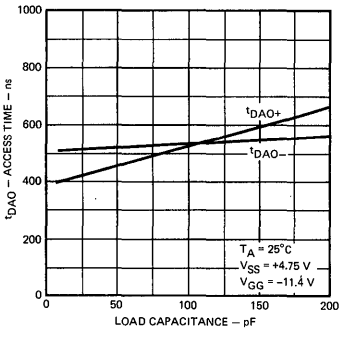


Fig. 5
OUTPUT VOLTAGE HIGH VERSUS OUTPUT CURRENT

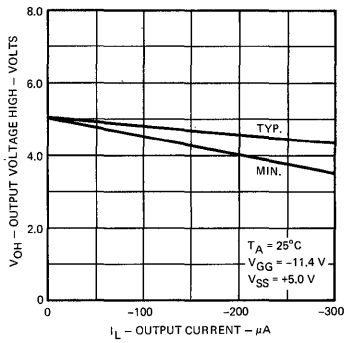


Fig. 6
OUTPUT VOLTAGE LOW VERSUS OUTPUT CURRENT

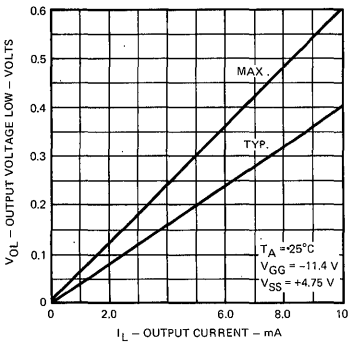


Fig. 7
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE

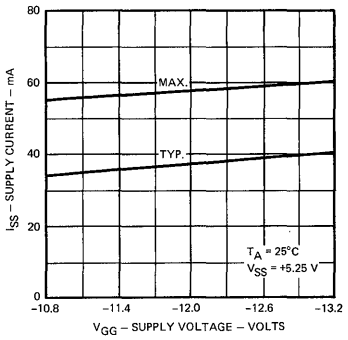


Fig. 8
OUTPUT VOLTAGE HIGH VERSUS AMBIENT TEMPERATURE

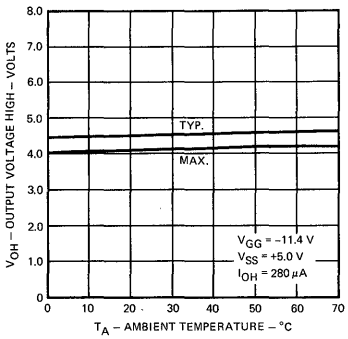
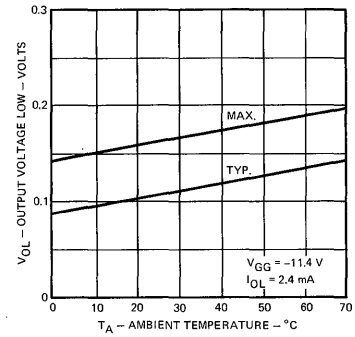


Fig. 9
OUTPUT VOLTAGE LOW VERSUS AMBIENT TEMPERATURE



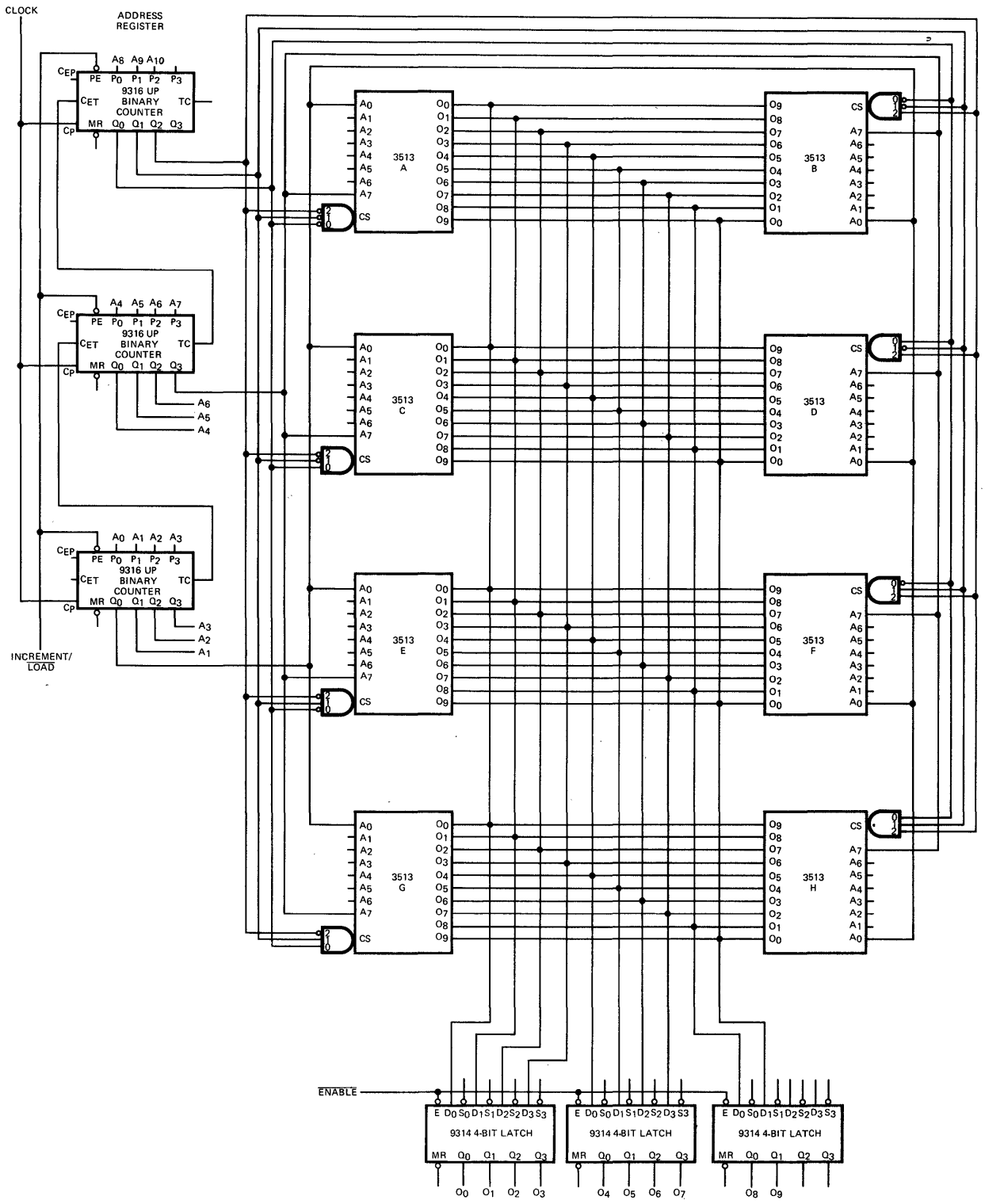


Fig. 10. 2K BY 10-BIT READ ONLY MEMORY SYSTEM

This 2048-word by 10-bit system uses eight 3513 ROMs. The address is stored in the 9316 counters. New addresses may be obtained by parallel loading the counters or by incrementing the current address. Chip selects 0, 1, and 2 have been programmed on the devices to decode three bits of the address. Layout is simplified by turning over the right hand column so that all the outputs lie between the devices, as shown. The wired-OR data outputs can be connected directly to the inputs of the TTL MSI 9314 4-bit latch.

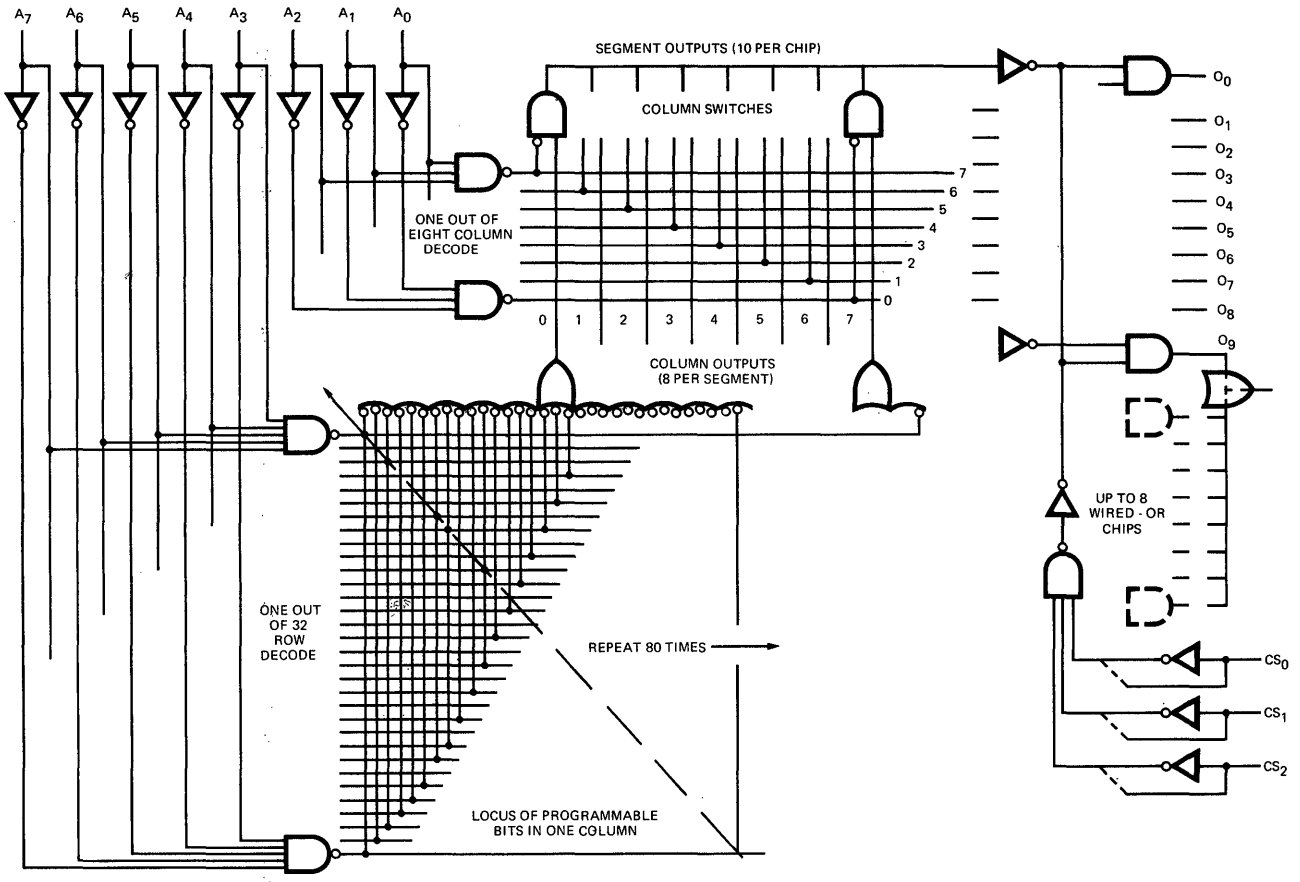


FIG. 11. ABBREVIATED LOGIC DIAGRAM

ORDERING INFORMATION – The 3513 is programmed on IBM cards or IBM coding forms in the format shown below.

A logic "1" = a more positive voltage (normally +5 V)
A logic "0" = a more negative voltage (normally 0 V)

	Column Number	Description
FIRST CARD		
	29	CS_2 input required to select chip
	31	CS_1 input required to select chip
	33	CS_0 input required to select chip
REMAINING 256 CARDS		
	10, 12, 14, 16, 18, 20, 22, 24	Address input pattern. The most significant bit (A_7) is in column 10.
	40, 42, 44, 46, 48, 50, 52, 54, 56, 58	Output pattern. The most significant bit (O_9) is in column 40.
	73, 74, 75, 76, 77, 78, 79,80	Coding these columns is not essential but may be used for card identification purpose.

GLOSSARY OF TERMS:

1. V_{SS}: The most positive voltage applied to the device.
2. V_{GG}: The most negative voltage applied to the device.
3. V_{DD}: The next most negative voltage applied to the device.
4. Address access time:
   - t_{DAO+} The time delay from an address input HIGH or LOW state to an output HIGH state.
   - t_{DAO-} The time delay from an address input HIGH or LOW state to an output LOW state.
5. t_E: Chip enable time. The time delay from valid code at chip select inputs to an output HIGH or LOW state.
6. $t_{\overline{E}}$: Chip disable time. The time delay from removal of a valid chip select input code to a HIGH state of the output when driving a standard TTL load.
7. T_A: Still air ambient-temperature.

3514
4096-BIT READ ONLY MEMORY
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3514 is a 4096-Bit Read Only Memory. It is organized in a 512-word by 8-bit format. There are four programmable chip selects to provide for OR wiring up to 16 chips. The 3514 is an MOS monolithic integrated circuit utilizing P-channel enhancement mode silicon gate technology.

- **INPUT AMPLIFIER ELIMINATES ALL PULL UP RESISTORS**
- **INTERFACE DIRECTLY WITH TTL – NO EXTERNAL COMPONENTS**
- **500 ns TYPICAL ACCESS TIME**
- **4-BIT PROGRAMMABLE CHIP SELECT CODE**
- **WIRED–OR CAPABILITY ON OUTPUTS**
- **STATIC – NO CLOCKS REQUIRED**

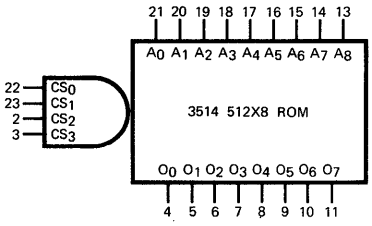
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C
Voltage on Any Input Pin (V_{SS} = GND)	−20 V to +0.3 V
Voltage on V_{DD} (V_{SS} = GND)	−7 V to +0.3 V
Voltage on Output Pin (V_{SS} = GND, Output Current @ ±10 mA)	−7 V to +0.3 V

APPLICATIONS

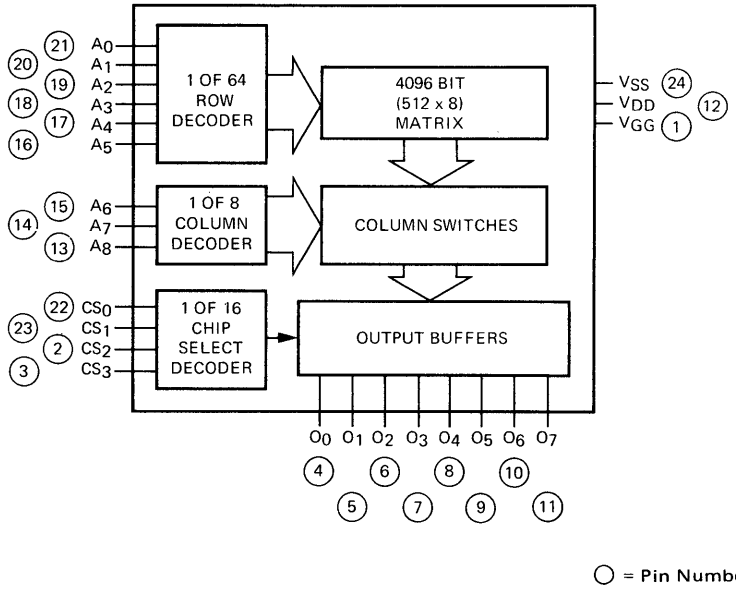
Code Conversion
Microprogramming
Table Lookup
Control Logic

LOGIC SYMBOL

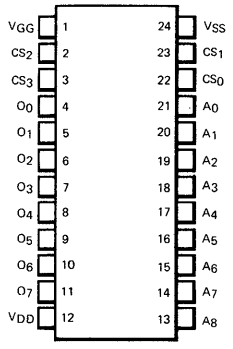


Pin 24 = V_{SS}
Pin 12 = V_{DD}
Pin 1 = V_{GG}

LOGIC BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION – A 9-bit binary address applied to the address inputs (A_0–A_8) will cause a corresponding 8-bit word to appear on the outputs (O_0–O_7). A 4-bit programmable chip select (CS_0–CS_3) allows selection of one-of-sixteen memories without external gating. When a chip is not selected, its outputs are turned off, i.e., a high impedance to both V_{SS} and V_{DD}. This feature allows expansion of up to 16 memories without external components, either for chip select decoding or for output gating. Each output of the device will drive 1.5 unit TTL loads, either one standard TTL device and two low power TTL devices or six low power devices.

Each input to the 3514 drives a special input amplifier stage which eliminates all pull up resistors (either on or off chip).

Two types of information are to be supplied when ordering the 3514. First, the bit pattern to be stored in the 512-word locations of memory, and second, the 4-bit chip enable code which will activate the chip.

DC CHARACTERISTICS: V_{GG} = -12 V ±5%, V_{DD} = 0 V, V_{SS} = ±5%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS}–2.75 V		V_{SS}	V	
V_{IL}	Input Voltage LOW	V_{GG}	0	0.55	V	
V_{OH}	Output Voltage HIGH	2.4		V_{SS}	V	I_{OH} = 0.5 mA
V_{OL}	Output Voltage LOW	0		0.4	V	I_{OL} < 2.4 mA
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = V_{SS} –6 V, Note 1
I_{LO}	Output Leakage Current			1.0	μA	V_{OUT} = V_{SS} –6 V, Note 2
I_{DD}	V_{DD} Current		19	25	mA	
I_{GG}	V_{GG} Current		19	25	mA	
I_{SS}	V_{SS} Current		38	50	mA	
P_D	Power Dissipation		450	580	mW	

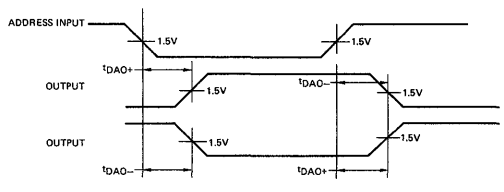
NOTES: 1. All pins at 0 V except those under test.
2. Output floating (chip not selected)

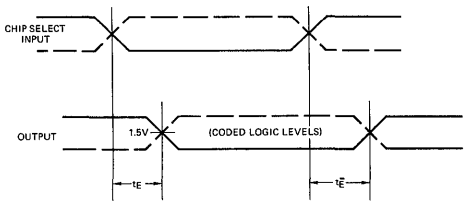
AC CHARACTERISTICS: V_{GG} = -12 V ±5%, V_{DD} = 0 V, V_{SS} = ±5 V ±5%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{DAO+}	Access Time Address to Output HIGH					Notes 1 and 2
	35141		500	700	ns	
	35142		.600	1.0	μs	
t_{DAO-}	Access Time Address to Output LOW					Notes 1 and 2
	35141		500	700	ns	
	35142		.600	1.0	μs	
t_E	Access Time Chip Select Enable to Output					Note 2
	35141		450	500	ns	
	35142		750	900		
$t_{\bar{E}}$	Access Time Chip Select Disable to Output					Note 2
	35141		550	600	ns	
	35142		750	900		
C_I	Input Capacitance		3.0	8.0	pF	
C_O	Output Capacitance		7.0	12	pF	Note 3

NOTES: 1. 1.5 TTL load
2. See timing diagram and characteristic curves.
3. Output floating (chip not selected)

TIMING DIAGRAM





TYPICAL ELECTRICAL CHARACTERISTICS

Fig. 1
ACCESS TIME VERSUS SUPPLY VOLTAGE

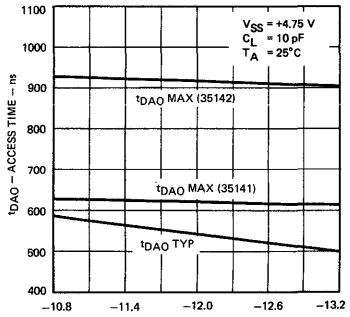


Fig. 2
ACCESS TIME VERSUS SUBSTRATE VOLTAGE

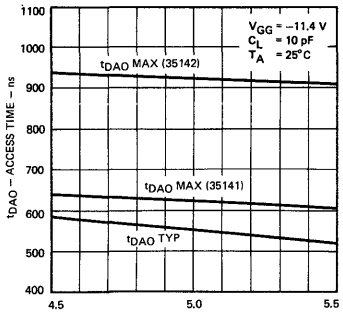


Fig. 3
ACCESS TIME VERSUS AMBIENT TEMPERATURE

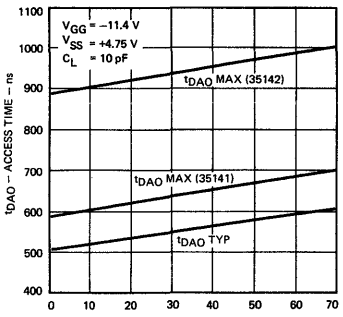


Fig. 4
ACCESS TIME VERSUS LOAD CAPACITANCE

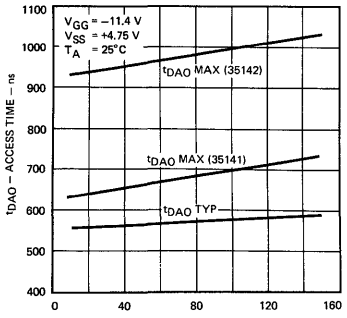


Fig. 5
V_{GG} CURRENT VERSUS AMBIENT TEMPERATURE

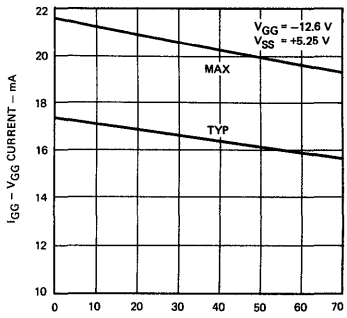


Fig. 6
V_{DD} CURRENT VERSUS AMBIENT TEMPERATURE

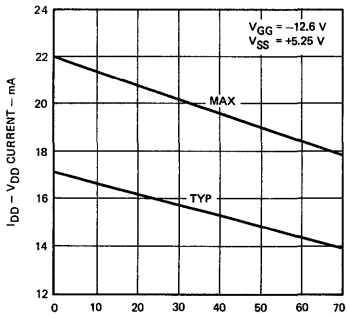


Fig. 7
V_{GG} CURRENT VERSUS SUPPLY VOLTAGE

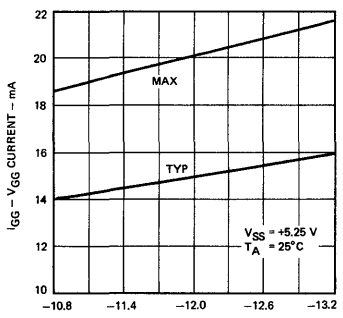
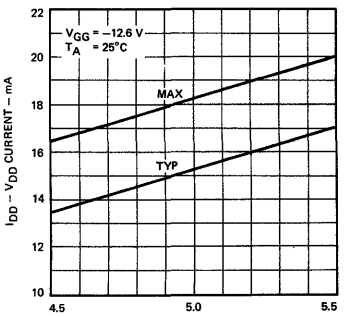


Fig. 8
V_{DD} CURRENT VERSUS SUBSTRATE VOLTAGE



CUSTOM PATTERN ORDERING INFORMATION – The 3514 is programmed on IBM cards or IBM coding form in the format as shown below. (Specify access time desired on Purchase Order).

Logic "1" = a more positive voltage (normally +5 V)
Logic "0" = a more negative voltage (normally o V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
50 thru 62	35141 or 35142
65 thru 72	Date

SECOND CARD

Column Number	Description
29	CS_3 input required to select chip
31	CS_2 input required to select chip
33	CS_1 input required to select chip
35	CS_0 input required to select chip

REMAINING 512 CARDS

Column Number	Description
10, 12, 14, 16, 18, 20, 22, 24, 26	Address input pattern. The most significant bit (A_8) is in column 10
40, 42, 44, 46, 48, 50, 52, 54	Output pattern. The most significant bit (O_7) is in column 40
73 through 80	Coding these columns is not essential and may be used for card identification purposes.

GLOSSARY OF TERMS

1. V_{SS}: The most positive voltage applied to the device.
2. V_{GG}: The most negative voltage applied to the device.
3. V_{DD}: The next most negative voltage applied to the device.
4. Address access time:
   - t_{DAO+} The time delay from an address input logic HIGH or logic LOW state to an output logic HIGH state.
   - t_{DAO-} The time delay from an address input logic HIGH or logic LOW state to an input logic LOW state.
5. t_E Chip enable time: The time delay from Valid Code at chip select inputs to an output logic HIGH or logic LOW state.
6. $t_{\bar{E}}$ Chip disable time: The time delay from removal of a valid chip select input code to a high state on outputs when driving a standard TTL load.
7. T_A: Still air ambient temperature.

3514A/3514B

ASCII TO EBCDIC/EBCDIC TO ASCII CODE CONVERTER

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3514A and 3514B are preprogrammed versions of the 3514 Read Only Memory containing the complete code conversion matrix necessary to convert from both ASCII to EBCDIC and EBCDIC to ASCII. Upon application of any 7-bit address of either code, the corresponding 7 (ASCII) or 8 (EBCDIC) bit word appears at the ROM outputs. The eighth output bit in the ASCII word is the even parity for the ASCII outputs.

Address bit A_8 is the conversion select input; a logic "0" selects ASCII to EBCDIC and a logic "1" selects EBCDIC to ASCII.

- **INPUT AMPLIFIER ELIMINATES ALL PULL UP RESISTORS**
- **INTERFACE DIRECTLY WITH TTL – NO EXTERNAL COMPONENTS**
- **500 ns TYPICAL ACCESS TIME**
- **WIRED–OR CAPABILITY ON OUTPUTS**
- **STATIC – NO CLOCKS REQUIRED**

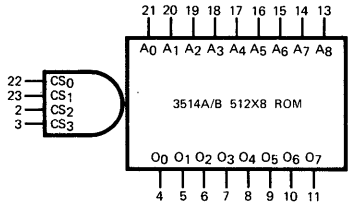
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C
Voltage on Any Input Pin (V_{SS} = GND)	–20 V to +0.3 V
Voltage on V_{DD} (V_{SS} = GND)	–7.0 V to +0.3 V
Voltage on Output Pin (V_{SS} = GND, Output Current @ ±10 mA)	–7.0 V to +0.3 V

APPLICATIONS

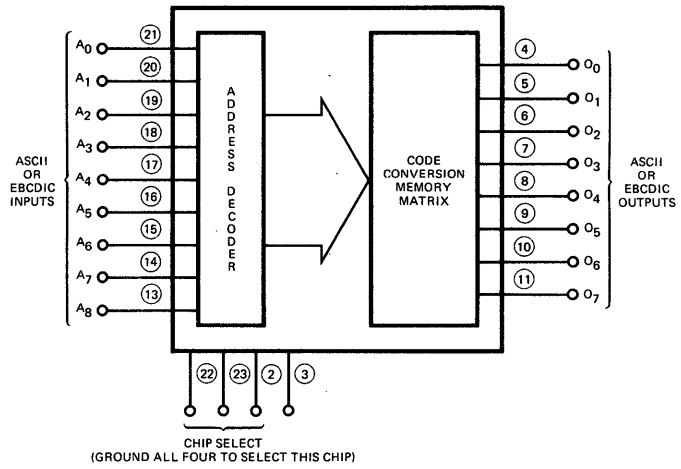
Code Conversion

LOGIC SYMBOL

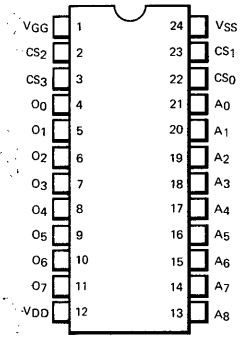


PIN 24 = V_{SS}
PIN 12 = V_{DD}
PIN 1 = V_{GG}

LOGIC BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION – The 3514A and 3514B, Note 1, contain the complete code conversion bit pattern to convert any 7-bit ASCII code to EBCDIC or any 8-bit EBCDIC code to ASCII. Address A_0 through A_6 and outputs O_0 through O_6 correspond to the two basic codes as follows:

Note 1: 3514A has an access time of 700 ns while 3514B has an access time of 1 μs.

CORRESPONDENCE OF CODES

ASCII TO EBCDIC

ROM Address Input	ASCII Bit	EBCDIC Bit	ROM Output
A_0	b_1 (LSB)	7 (LSB)	O_0
A_1	b_2	6	O_1
A_2	b_3	5	O_2
A_3	b_4	4	O_3
A_4	b_5	3	O_4
A_5	b_6	2	O_5
A_6	b_7 (MSB)	1	O_6
A_7	b_8 (odd or even parity)	0 (MSB)	O_7

A_8 = Logic "0"

EBCDIC TO ASCII

ROM Address Input	EBCDIC Bit	ASCII Bit	ROM Output
A_0	7 (LSB)	b_1 (LSB)	O_1
A_1	6	b_2	O_2
A_2	5	b_3	O_3
A_3	4	b_4	O_4
A_4	3	b_5	O_5
A_5	2	b_6	O_6
A_6	1	b_7 (MSB)	O_7
A_7	0 (MSB)	b_8 (odd parity)	O_8

A_8 = Logic "1"

ASCII(A) TO EBCDIC(E)

A	E	A	E	A	E	A	E	A	E	A	E	A	E	A	E
NUL	NUL	DLE	DLE	SP	SP	0	0	@	@	P	P	`	`	p	p
SOH	SOH	DC1	DC1	!	!	1	1	A	A	Q	Q	a	a	q	q
STX	STX	DC2	DC2	"	"	2	2	B	B	R	R	b	b	r	r
ETX	ETX	DC3	TM	#	#	3	3	C	C	S	S	c	c	s	s
EOT	EOT	DC4	DC4	$	$	4	4	D	D	T	T	d	d	t	t
ENQ	ENQ	NAK	NAK	%	%	5	5	E	E	U	U	e	e	u	u
ACK	ACK	SYN	SYN	&	&	6	6	F	F	V	V	f	f	v	v
BEL	BEL	ETB	EOB	'	'	7	7	G	G	W	W	g	g	w	w
BS	BS	CAN	CAN	(	(	8	8	H	H	X	X	h	h	x	x
HT	HT	EM	EM	)	)	9	9	I	I	Y	Y	i	i	y	y
LF	LF	SUB	SUB	*	*	:	:	J	J	Z	Z	j	j	z	z
VT	VT	ESC	PRE	+	+	;	;	K	K	[	(	k	k	{	(
FF	FF	FS	IFS	,	,	<	<	L	L	\	/	l	l	:	|
CR	CR	GS	IGS	–	–	=	=	M	M	]	)	m	m	}	)
SO	SO	RS	IRS	.	.	>	>	N	N	^	¬	n	n	~	¢
SI	SI	US	IUS	/	/	?	?	O	O	–	–	o	o	DEL	DEL

EBCDIC(E) TO ASCII(A)

E	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A
NUL	NUL	DLE	DLE	DS		–	–	SP	SP	&	&	–	–		
SOH	SOH	DC1	DC1	SOS		–	–					/	/		
STX	STX	DC2	DC2	FS		SYN	SYN								
ETX	ETX	TM	DC3	–	–	–	–								
PF		RES		BYP		PN									
HT	HT	NL		LF	LF	RS									
LC		BS	BS	EOB	ETB	UC				NOTHING IN THIS AREA					
DEL	DEL	IL		PRE	ESC	EOT	EOT								
✓		CAN	CAN	–	–	–	–								
–	–	EM	EM	–	–	–	–								
SMM		CC		SM		–	–	¢		!	!			:	:
VT	VT	CU1		CU2		CU3		.	.	$	$	,	,	#	#
FF	FF	IFS	FS	–	–	DC4	DC4	<	<	*	*	%	%	@	@
CR	CR	IGS	GS	ENQ	ENQ	NAK	NAK	(	(	)	)	–	–	'	`
SO	SO	IRS	RS	ACK	ACK	–	–	+	+	;	;	>	>	=	=
SI	SI	IUS	US	BEL	BEL	SUB	SUB	|	:	¬	^	?	?	"	"
–	–	–	–	–	–			–	–	–	–	–	–	0	0
a	a	j	j	–	–			A	A	J	J	–	–	1	1
b	b	k	k	s	s			B	B	K	K	S	S	2	2
c	c	l	l	t	t			C	C	L	L	T	T	3	3
d	d	m	m	u	u			D	D	M	M	U	U	4	4
e	e	n	n	v	v			E	E	N	N	V	V	5	5
f	f	o	o	w	w			F	F	O	O	W	W	6	6
g	g	p	p	x	x			G	G	P	P	X	X	7	7
h	h	q	q	y	y			H	H	Q	Q	Y	Y	8	8
i	i	r	r	z	z			I	I	R	R	Z	Z	9	9

3532
512 × 1 RANDOM ACCESS MEMORY
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

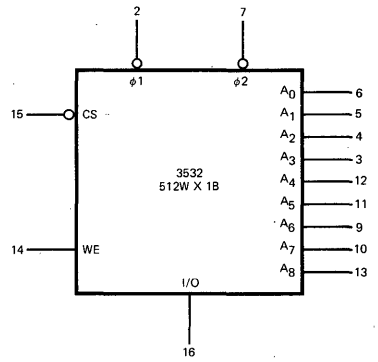
GENERAL DESCRIPTION – The 3532 is a 512-word X 1-bit non-destructive read out static Random Access Memory. It uses static circuitry for its memory cells. The decoding and sensing are accomplished by dynamic circuitry, resulting in low peripheral power consumption. This product is manufactured using P-channel enhancement mode silicon gate technology.

- **LOW POWER DISSIPATION – TYPICAL** { **0.3 mW/BIT – OPERATING** / **30 μW/BIT – STANDBY**
- **BIPOLAR COMPATIBLE (WITH EXTERNAL RESISTORS)**
- **WRITE/READ CYCLE TIME – 600 ns/1 μs**
- **STATIC MEMORY CELLS**
- **WIRED-OR CAPABILITY**
- **FULLY DECODED**
- **16-LEAD DUAL IN-LINE**
- **INPUT PROTECTION**

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

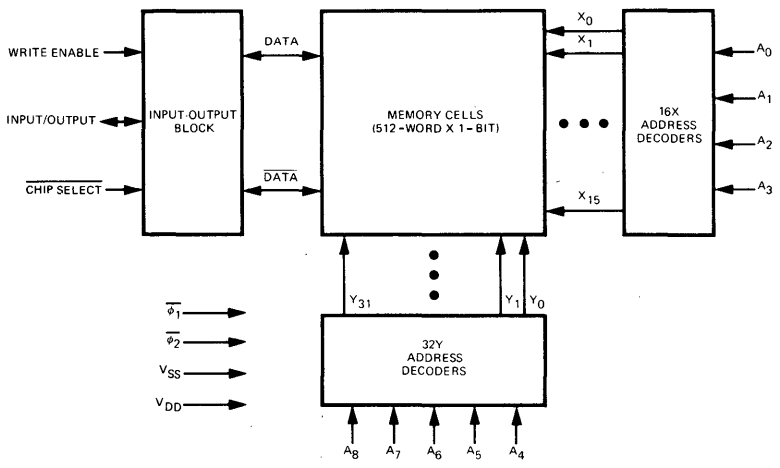
Storage Temperature	–65°C to +150°C
Operating Temperature	0°C to +70°C
All pins except I/O (V_{SS} = GND)	–24 V to +0.3 V
I/O Pin	–13 V to +0.3 V

LOGIC SYMBOL

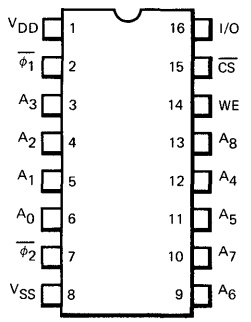


V_{DD} = Pin 1
V_{SS} = Pin 8

BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION – The 3532 is designed for easy system implementation. All logic signals (not including the clocks) are bipolar compatible with external pull up resistors. For the on chip peripheral circuitry (address decoding and input/output), a 2-phase clock system (ϕ_1 and ϕ_2) is required. However, because of the static nature of the memory cells, the two clocks can be turned off indefinitely during the standby condition and power consumption of the device would then be reduced considerably. To facilitate system expansion, data input and output of the device, which share one common device pin (I/O), have wired-OR capability.

For write operation, the I/O pin is unconditionally precharged to a LOW level when ϕ_1 clock is LOW. After ϕ_1 is HIGH, the voltage level of the I/O pin will either remain LOW, if the system input signal (DI) is LOW, or, after some internal delay, will change to a HIGH, if the system data input signal (DI) is HIGH. After the ϕ_2 clock is LOW and after some internal delay, data input information will be stored into the addressed memory cell. (See Figures 4 and 5.)

For read operation the I/O pin is also unconditionally precharged to a LOW level when ϕ_1 is LOW. The voltage level of the I/O pin will then remain LOW until ϕ_2 is LOW. After ϕ_2 clock is LOW and after some internal delay, the stored logic level will define the output state. (See Figures 4 and 5.)

For memory system implementation, several 3532 packages can be wired-OR and each of the wired-OR packages can be either selected or inhibited with the Chip Select (CS) signal as shown in Figure 5. Interface of the I/O pin with system data input (DI) and system data output (DO) is also shown in Figure 5. During the read operation, the write driver connected to the I/O pin must be inhibited.

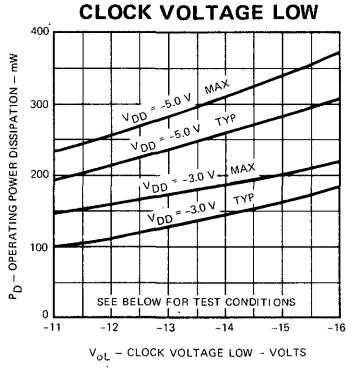
Appropriate timing for the two clocks and the logic signals are shown in Figure 3.

DC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = −3 V ±10%, T_A = 0°C to 75°C.

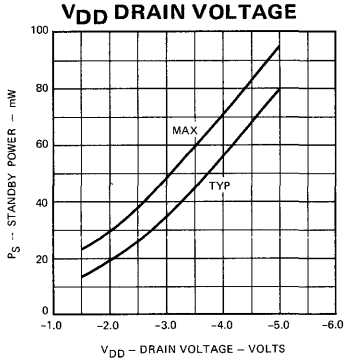
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS} −1.0		V_{SS} +0.3	V	
V_{IL}	Input Voltage LOW			+0.8	V	
$V_{\phi H}$	Clock Voltage HIGH	V_{SS} −1.0		V_{SS}	V	
$V_{\phi L}$	Clock Voltage LOW	−16.0		−13.5	V	
V_{OH}	Output Voltage HIGH	2.4			V	One TTL and 680 Ω resistor to V_{SS}
V_{OL}	Output Voltage LOW			+0.40	V	
I_{OL}	Output Current LOW	9.0	11.5	14	mA	$V_{\phi H}$ = +4.5 V, $V_{\phi L}$ = −16 V V_{OUT} = 0.40 V
I_{LI}	Input Leakage Current			1.0	μA	$V_{SS} - V_{IN}$ = 6.0 V
$I_{DD\phi1}$	V_{DD} Supply Current, ϕ_1 LOW		27	35	mA	$V_{\phi1}$ = −16 V (dc), $V_{\phi2}$ = +4.5 V I/O Pin Tied to +0.4 V
$I_{DD\phi2}$	V_{DD} Supply Current, ϕ_2 LOW		5.5	8.0	mA	$V_{\phi1}$ = +4.5 (dc), $V_{\phi2}$ = −16 V
I_{DDS1}	V_{DD} Supply Current, Standby Condition 1 (See Note 4 of Timing)		4.8	6.5	mA	$V_{\phi1} = V_{\phi2}$ = +4.5 V
I_{DDS2}	V_{DD} Supply Current, Standby Condition 2 (See Note 4 of Timing)		2.5	3.5	mA	$V_{\phi1} = V_{\phi2}$ = +4.5 V, V_{DD} = −1.5 V
I_{DDO}	Average V_{DD} Supply Current, Operating Condition		23.0	28.5	mA	(i) $V_{\phi H}$ = +4.5 V, $V_{\phi L}$ = −16 V (ii) $t_{\phi1}$ = 130 ns, $t_{\phi D1}$ = 150 ns $t_{\phi2}$ = 280 ns, $t_{\phi D2}$ = 40 ns (iii) Alternating Write-Read Operations (iv) Alternating HIGH-LOW data Pattern for Write Operation
P_D	Operating Power Dissipation		180	230	mW	

DC CHARACTERISTIC CURVES

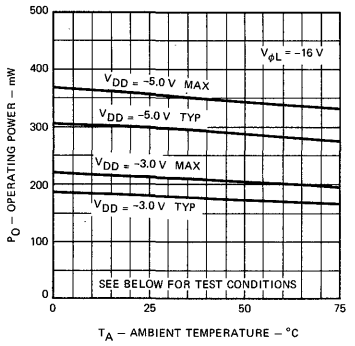
OPERATING POWER VERSUS* CLOCK VOLTAGE LOW



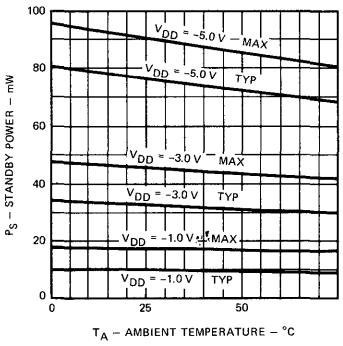
STANDBY POWER VERSUS V_{DD} DRAIN VOLTAGE



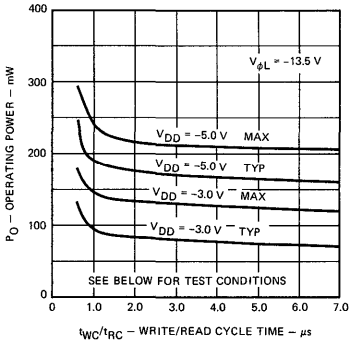
OPERATING POWER VERSUS* AMBIENT TEMPERATURE



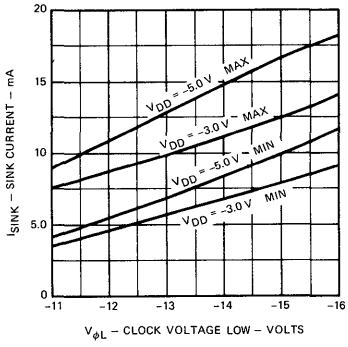
STANDBY POWER VERSUS AMBIENT TEMPERATURE



OPERATING POWER VERSUS* WRITE/READ CYCLE TIME



OUTPUT SINK CURRENT VERSUS CLOCK VOLTAGE LOW



OPERATING POWER TEST CONDITIONS

$t_{\phi 1}$ = 130 ns, $t_{\phi D1}$ = 150 ns, $t_{\phi s}$ = 280 ns, $t_{\phi D2}$ = 40 ns

Alternating Write/Read Operation (50% Write Time and Read Time)

R_L adjusted to V_{OL} = +0.40 V

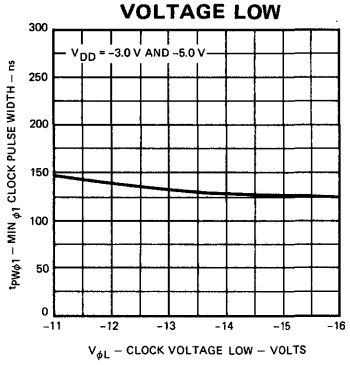
*Alternating HIGH — LOW data pattern for write operation.

AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = −3 V ±10%, T_A = 0°C to 75°C.

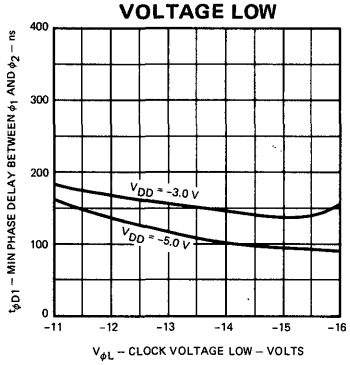
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
C_ϕ	Clock Capacitance		50	65	pF	Measuring frequency = 1 MHz All other device pins grounded
C_D	Data Input Capacitance		5.0	7.0	pF	
C_A	Address Capacitance		3.0	5.0	pF	
C_{CS}	Chip Select Capacitance		3.0	5.0	pF	
C_{WE}	Write Enable Capacitance		4.5	6.0	pF	
(35321)						
t_r	Clock Rise Time, 10% to 90%	0.04		1	μs	$V_{\phi L}$ = −13.5 V $V_{\phi H}$ = +4.5 V $t_r = t_f \cong 40$ ns C_L = 45 pF, R_L = 680 Ω and 1 TTL Load
t_f	Clock Fall Time, 10% to 90%	0.02		1	μs	
$t_{PW\phi1}$	ϕ_1 Clock Pulse Width	0.13		10	μs	
$t_{PW\phi2}$	ϕ_2 Clock Pulse Width	0.28		10	μs	
$t_{\phi D1}$	Phase Delay Between ϕ_1 and ϕ_2	0.15		10	μs	
$t_{\phi D2}$	Phase Delay Between ϕ_2 and ϕ_1	40			ns	
$t_{D\phi O}$	Output Delay			270	ns	
t_{WC}	Write Cycle Time (= $t_{PW\phi1} + t_{\phi D1} + t_{PW\phi2} + t_{\phi D2}$)			600	ns	
t_{RA}	Read Access Time (= $t_{PW\phi1} + t_{\phi D1} + t_{D\phi O}$)			550	ns	
t_S	Input Set Up Time	130			ns	
t_H	Address Hold Time	30			ns	

ELECTRICAL CHARACTERISTICS
(35321)

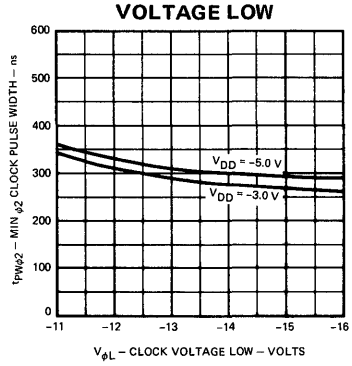
MINIMUM ϕ_1 CLOCK PULSE WIDTH VERSUS CLOCK VOLTAGE LOW



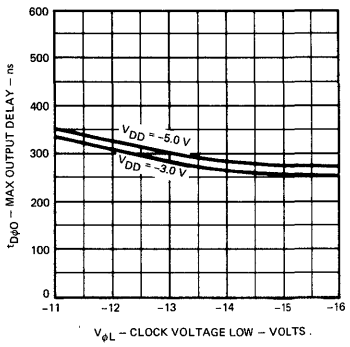
MINIMUM PHASE DELAY BETWEEN ϕ_1 AND ϕ_2 VERSUS CLOCK VOLTAGE LOW



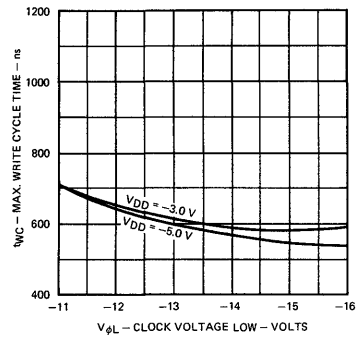
MINIMUM ϕ_2 CLOCK PULSE WIDTH VERSUS CLOCK VOLTAGE LOW



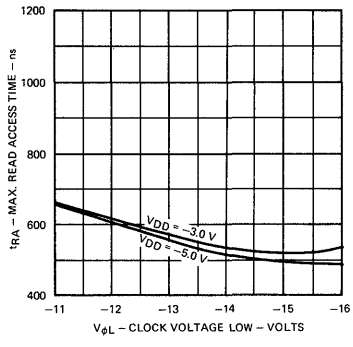
MAXIMUM OUTPUT DELAY VERSUS CLOCK VOLTAGE LOW



MAXIMUM WRITE CYCLE TIME VERSUS CLOCK VOLTAGE LOW



MAXIMUM READ ACCESS TIME VERSUS CLOCK VOLTAGE LOW

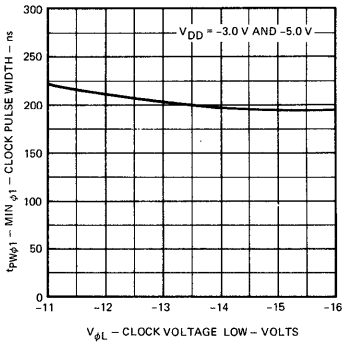


(35322) AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = −3 V ±10%, T_A = 0°C to 75°C (Cont'd)

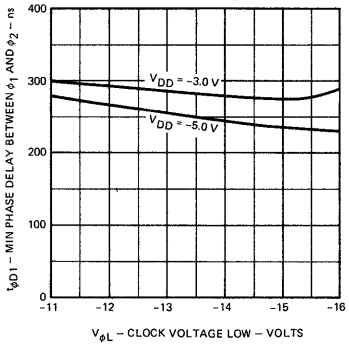
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_r	Clock Rise Time, 10% to 90%	0.04		1	μs	
t_f	Clock Fall Time, 10% to 90%	0.02		1	μs	
$t_{PW\phi1}$	ϕ_1 Clock Pulse Width	0.2		10	μs	
$t_{PW\phi2}$	ϕ_2 Clock Pulse Width	0.46		10	μs	$V_{\phi L}$ = −13.5 V
$t_{\phi D1}$	Phase Delay Between ϕ_1 and ϕ_2	0.28		10	μs	$V_{\phi L}$ = +4.5 V
$t_{\phi D2}$	Phase Delay Between ϕ_2 and ϕ_1	60			ns	$t_r = t_f \cong 40$ ns
$t_{D\phi O}$	Output Delay			440	ns	C_L = 45 pF, R_L = 680 Ω and
t_{WC}	Write Cycle Time (= $t_{PW\phi1} + t_{\phi D1} + t_{PW\phi2} + t_{\phi D2}$)			1.0	μs	1 TTL Load
t_{RA}	Read Access Time (= $t_{PW\phi1} + t_{\phi D1} + t_{D\phi O}$)			920	ns	
t_S	Input Set Up Time	200			ns	
t_H	Address Hold Time	30			ns	

ELECTRICAL CHARACTERISTICS
(35322)

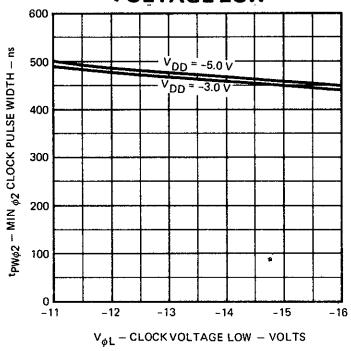
MINIMUM ϕ_1 CLOCK PULSE WIDTH VERSUS CLOCK VOLTAGE LOW



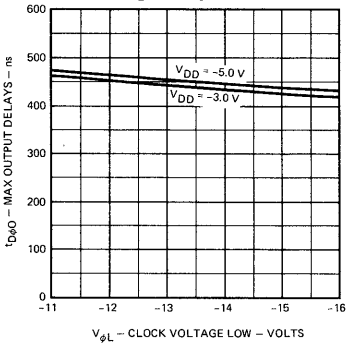
MINIMUM PHASE DELAY BETWEEN ϕ_1 AND ϕ_2 VERSUS CLOCK VOLTAGE LOW



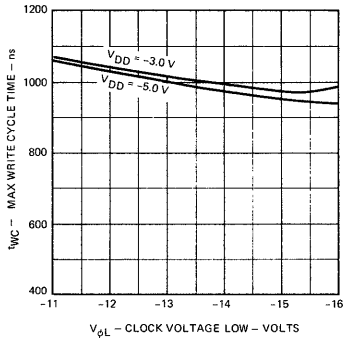
MINIMUM ϕ_2 CLOCK PULSE WIDTH VERSUS CLOCK VOLTAGE LOW



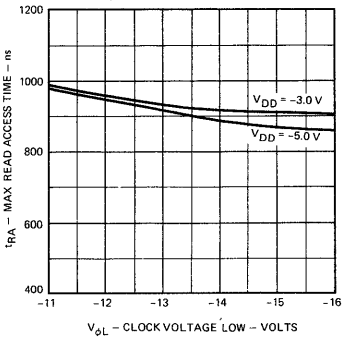
MAXIMUM OUTPUT DELAY VERSUS CLOCK VOLTAGE LOW



MAXIMUM WRITE CYCLE TIME VERSUS CLOCK VOLTAGE LOW



MAXIMUM READ ACCESS TIME VERSUS CLOCK VOLTAGE LOW



TIMING DIAGRAM

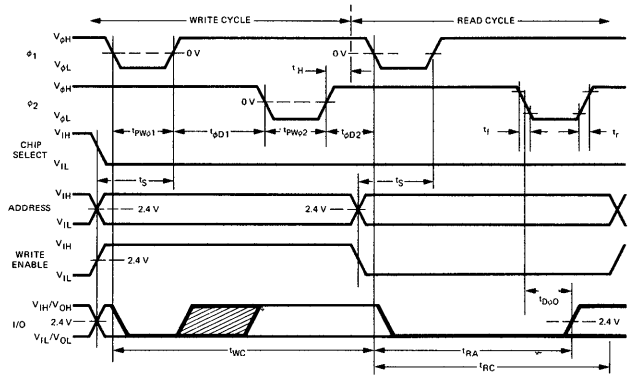


Fig. 3

NOTES:
1. Data input driver must be disabled during read.
2. Output is an MOS device returned to V_{DD}.
3. For I/O waveform, thick line shows levels controlled by the memory itself while thin line indicates appropriate input levels. Whenever ϕ_1 is LOW ($V_{\phi L}$), I/O voltage level will be pulled down to LOW regardless of Write or Read Cycle. Shaded area indicates RC delay determined by output capacitance, output impedance and external pull up resistance.
4. During Standby, data information for individual cells will not be lost even if V_{DD} is decreased to −1.5 V. Accordingly, standby power can be reduced if V_{DD} power supply is reduced to −1.5 V during standby condition.

LOGIC-CIRCUIT SCHEMATIC DIAGRAM

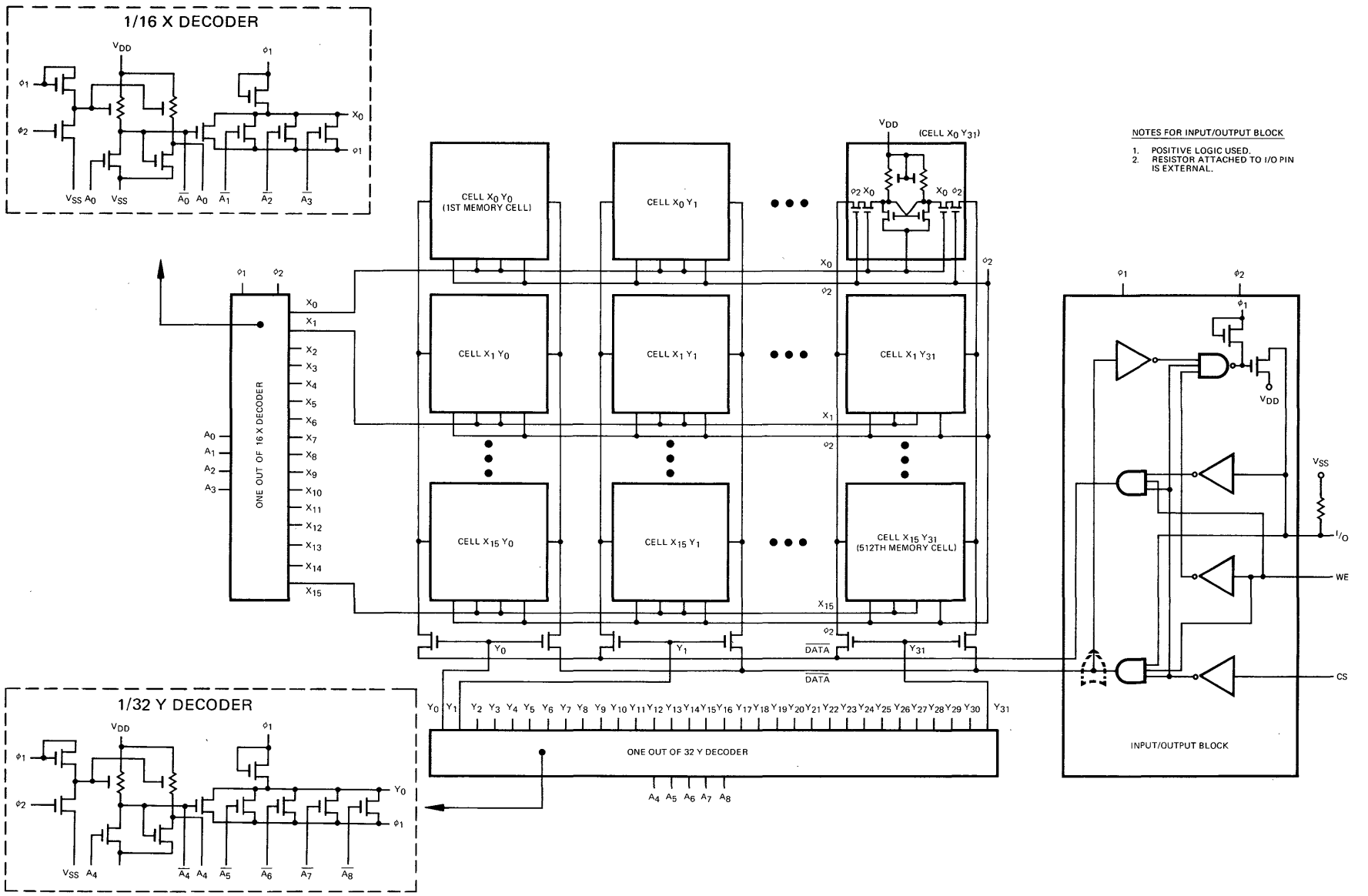


Fig. 4

MULTICHIP MEMORY PLANE
(2048 WORDS BY M BITS)

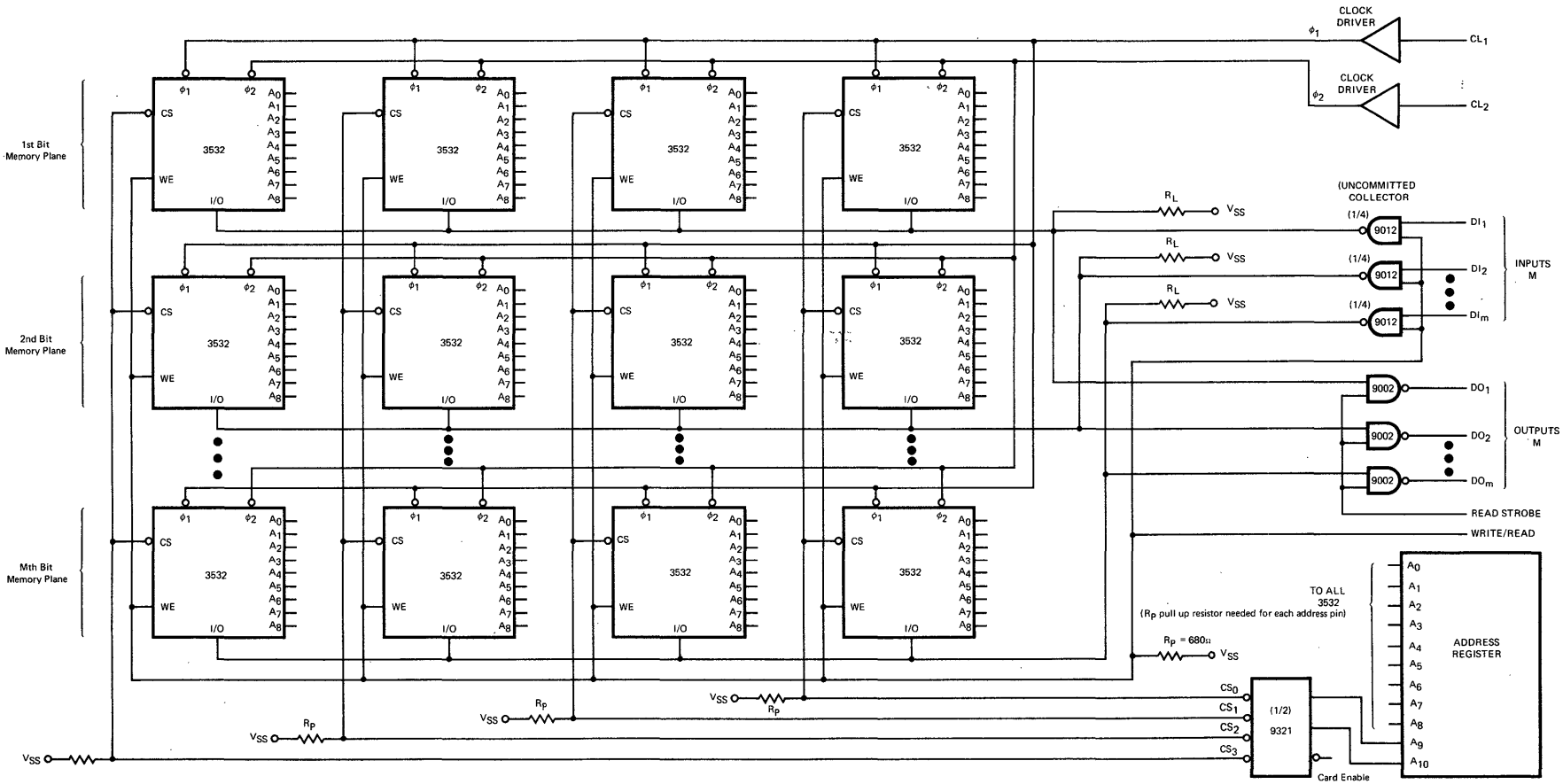


Fig. 5

MEMORY SYSTEM DESIGN USING FAIRCHILD'S 3532 STATIC RAM

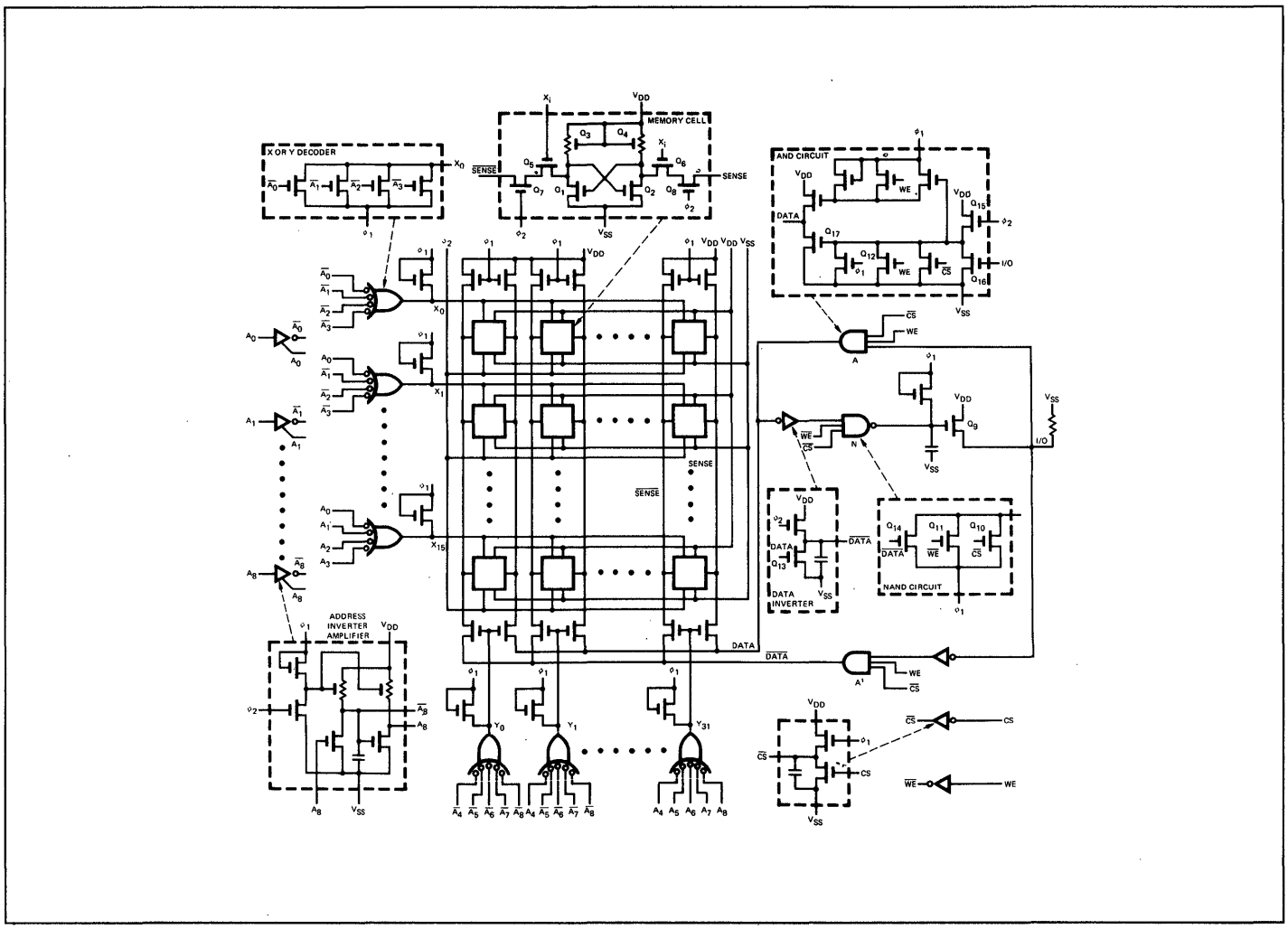
INTRODUCTION

The Fairchild 3532 is a 512-word by 1-bit static MOS random access memory featuring nondestructive read out and TTL compatibility. The 3532 uses a two phase clocking scheme and much dynamic circuitry for address decoding and cell sensing; both features minimize power dissipation. No refresh operations are required because the memory cells are static. A general description of the device with special attention to the interface timing and I/O circuitry follows. Also, system considerations and a 256 X 8 as well as a 2,048 X 8 memory array are discussed.

FUNCTIONAL DESCRIPTION

Figure 1 shows the basic layout and circuit details of the 3532. The memory cells are organized in a 16-row by 32-column matrix. Each memory cell is two cross-coupled MOS devices (Q_1, Q_2), load devices (Q_3, Q_4) and additional MOS devices for access to the memory cell ($Q_5 - Q_8$). Information is stored in the static flip-flop circuit (Q_1, Q_2, Q_3 and Q_4). Either Q_1 or Q_2 always conducts depending on the state of the latch.

To select one of the 512 cells, dynamic on-chip decoders are provided. One of the 16 rows (X) and one of the 32 columns (Y) are selected by 1-of-16 and 1-of-32 decoders respectively by the input address. The logic levels required at the address inputs are DTL/TTL compatible. The minimum logic "1" required is 3.75 V, which means that pull up resistors and uncommitted collector devices are used as drivers for the Address, Chip Select and Write Enable functions. A common I/O line simplifies interconnection of 3532s in arrays and allows the use of a 16-lead package. Read or Write cycles are determined by the state of the Write Enable. Also, Chip Select allows easy word expansion of the memory array.



Schematic Diagram 3532

The use of a 2-phase clocking scheme minimizes power dissipation and interface timing requirements. Maximum standby dissipation when ϕ_1 and ϕ_2 are off ($V_{\phi 1} = V_{\phi 2} = 4.5$ V, $V_{SS} = 5.25$ V, $V_{DD} = -3.3$ V) is less than 56 mW. Typically, standby power is less than 38 mW. Significant power is dissipated only when ϕ_1 is on ($V_{\phi 1} = -14.75 \pm 1.25$ V). The average operating power depends on the duty cycles of ϕ_1 and ϕ_2, and under worst case conditions does not exceed 250 mW.

OPERATION

The schematic diagram of Figure 1 and the Read and Write cycle timing diagrams of Figures 2 and 3 clarify the basic operation of the 3532. A memory cycle begins with the leading (negative going) edge of the ϕ_1 clock, (1) . When ϕ_1 is LOW ($t_{\phi 1}$), the address inputs $A_0 - A_8$ are inverted, row select lines $X_0 - X_{15}$ and column select lines $Y_0 - Y_{31}$ are precharged to a negative potential near V_{OL} (clock LOW voltage), and the memory sense and data lines are precharged to a negative potential near V_{DD}. In addition, Q_9 (output device) is turned on and the I/O line is unconditionally forced to a logic "0" ($V_{OL} = 0.4$ V max). To allow sufficient time to invert the address inputs and thus allow proper decoding, inputs A_0 through A_8 must be valid at least t_s ns before the trailing (positive going) edge of ϕ_1. Similarly, to properly condition the I/O circuitry and invert Chip Select and Write Enable, CS and WE must be stable t_s ns prior to the trailing edge of ϕ_1.

The second phase of the cycle begins when ϕ_1 goes positive, (2) . During the interval between ϕ_1 and ϕ_2, the row and column decoders stabilize and only one row and one column decoder remain precharged at a negative potential near V_{OL}. The remaining decoders discharge to a positive potential near V_{OH} (clock HIGH voltage) and inhibit access to any memory cells in their respective rows or columns. To allow sufficient time to discharge the unselected decoders, the leading (negative going) edge of ϕ_2 must not occur until $t_{\phi D1}$ ns after the positive excursion of ϕ_1. Furthermore, when ϕ_1 goes positive,

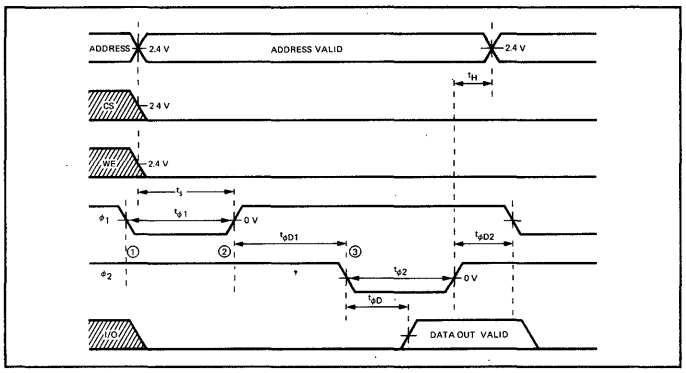


Fig. 2 Read Cycle 3532

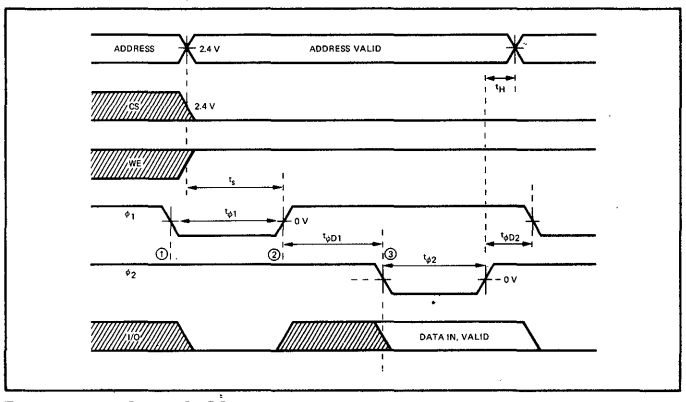


Fig. 3 Write Cycle 3532

the I/O circuitry interrogates the status of the Chip Select and Write Enable inputs and determines the type of cycle to perform. If the chip has not been selected, Q_{10} conducts and the capacitance associated with Q_9 is discharged. Q_9 then turns off and the I/O line effectively becomes an open circuit. If the chip has been selected (CS = 0.4 V max), the state of Write Enable controls the I/O line.

Up to this point, both Read and Write cycles are identical. For a clear understanding of the balance of the Read and Write cycles, each is discussed separately. For a Read cycle, (See Figure 2), Write Enable is LOW ($V_{IL} \leq 0.4$ V) and the capacitance associated with the gate of Q_9 remains precharged to a negative potential near V_{OL} so Q_9 remains on. The two data input AND circuits A and A^1 are disabled and the DATA and DATA lines remain at a negative potential near V_{DD}.

The third phase, (3) of the Read cycle begins with the leading (negative going) edge of ϕ_2 and it is during $t_{\phi 2}$ that the information stored in the selected memory cell is sensed. ϕ_2 turns on Q_7 and Q_8 and the 32 cells corresponding to the decoded row are sampled. If Q_2 is conducting (Q_1 off), the SENSE line is discharged to a positive potential near V_{SS}. Conversely, if Q_2 is not conducting (Q_1 on), the SENSE line remains at the precharged potential. Because the column decoders have enabled one of the array columns, the DATA line assumes the potential of the SENSE line of the selected column. Hence the SENSE and DATA lines are conditionally discharged depending on the state of the selected memory cell. Q_{13} in the data inverter circuits is initially conducting and prevents Q_{14} from turning on. If the DATA line remains precharged (Q_2 off), Q_{13} remains on and the output (I/O line) remains at the logic "0" level. However, if Q_2 is conducting, Q_{13} turns off and Q_{14} turns on. The capacitance associated with the node of Q_9 discharges and Q_9 turns off. The I/O line is then pulled up to the logic "1" level by an external resistor. The I/O line may be strobed by the control logic $t_{\phi D}$ ns after the leading edge of ϕ_2.

When Q_2 returns to the positive level (near V_{SS}), the cells in the selected row are disabled since Q_7 and Q_8 turn off and the chip returns to the standby mode. The delay between the trailing edge of ϕ_2 and the leading edge of ϕ_1 (or the next cycle) is required to allow Q_7 and Q_8 to completely turn off and thus prevent the cells from being perturbed when ϕ_1 precharges the SENSE and SENSE lines.

The I/O line maintains the correct logic level even after ϕ_2 terminates. Since the capacitance associated with the gates of Q_{14} and Q_9 remains charged for a few microseconds, Q_9 remains on if a logic "0" was read and Q_{14} remains on if a logic "1" was read. This means that for many applications, data output registers may not be required if the data can be processed before the charge on the gate of Q_9 begins to decay. Of course this assumes that the I/O buss interconnecting other 3532s is not disturbed by external logic. Specifically, the Write gates must be disabled.

The Write cycle is shown in Figure 3 and is similar to a Read Cycle in that information is processed as the conditional discharging of the SENSE and DATA lines. For a Write cycle, however, WE is at a logic "1". On the trailing edge, (2) of ϕ_1 (positive going), Q_9 turns off since its gate capacitance is discharged by Q_{11} which is conducting. Thus the output driver is disabled. The I/O line now assumes the logic level determined by the external data input driver as is seen in Figure 3. An on chip inverter provides the compliment of the I/O logic level for AND gate A^1.

On the leading edge of ϕ_2, (3) Q_{15} turns on in gates A and A^1. If the I/O line is at a logic "0" (LOW), Q_{16} is on in gate A and the DATA and SENSE lines remain at a negative potential

near V_{DD}. In Gate A^1, however, Q_{16} is off and Q_{17} turns on, discharging the DATA and SENSE lines to a positive potential. If the I/O line was at a logic "1", the SENSE and DATA lines would have been discharged. ϕ_2 also turns on Q_7 and Q_8 in the selected cell, and the gates of Q_1 and Q_2 assume the potential of the SENSE and SENSE lines respectively. Thus if the SENSE line was precharged (near V_{DD}), Q_1 turns on, (or remains conducting) and Q_2 turns off, (or remains off) since the SENSE line is discharged. When ϕ_2 terminates, the selected cells are disabled and another cycle may begin after $t_{\phi D2}$ ns.

Memory Systems

There are many advantages when using the 3532 for memory applications ranging in word size from 128 to 8092 words. during operation and standby has been minimized to permit the use of low cost power supplies in the memory system. Standby power is particularly low, critical in applications where data must be retained by auxiliary methods (i.e., battery pack) during periods of main power failure.

To illustrate the flexibility and ease of design characteristic of the 3532, the 256 X 8 memory system of Figure 4 has been designed using only four RAMS. Ten additional integrated circuits are required for timing and control functions with two performance options available. The system operation is asynchronous, thus eliminating the requirement for a high frequency clock. A data output register is provided to facilitate data handling by the memory controller.

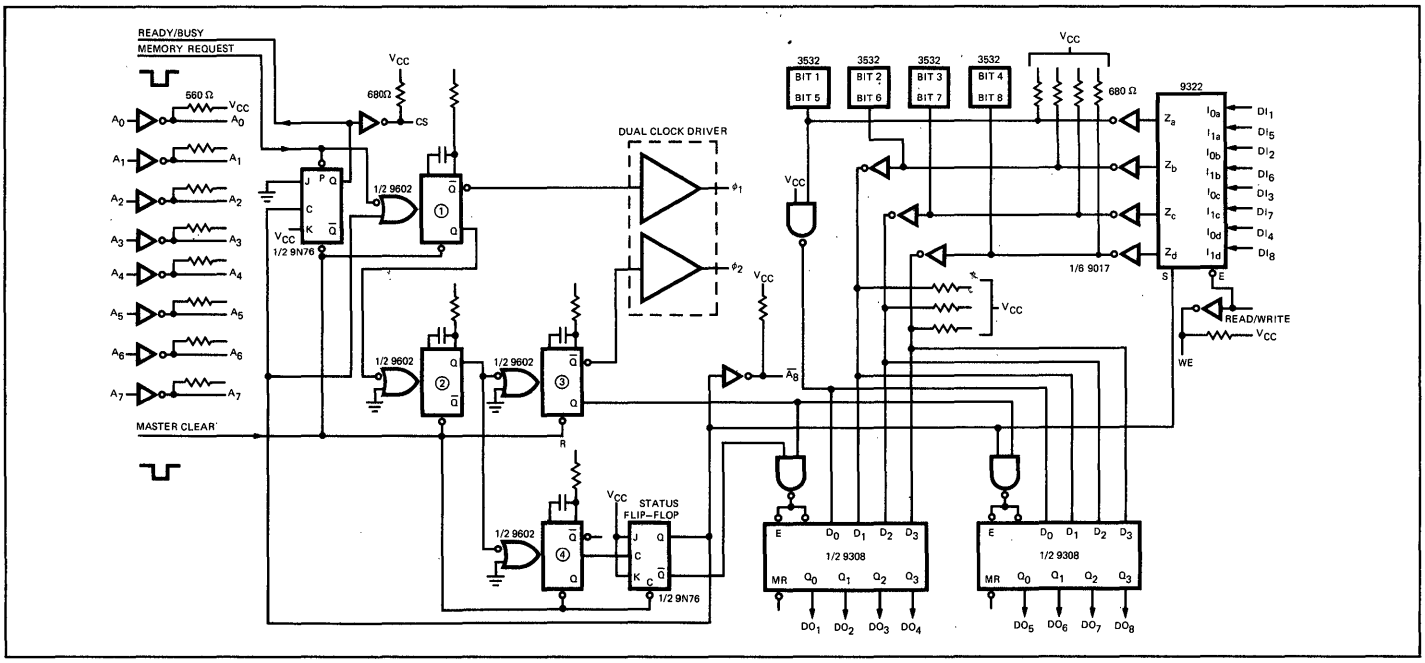


Fig. 4 Memory System 256x8

Among the most important advantages is that the 3532 is a static memory and does not require the additional logic and address circuitry necessary for the operation of dynamic RAMS. TTL compatible inputs further reduce the complexity of the driver circuitry and a common I/O line permits easy interconnection of the devices in the word dimension. Furthermore, the timing requirements for the 3532 clocks are easily generated with inexpensive devices (9602s). Power dissipation

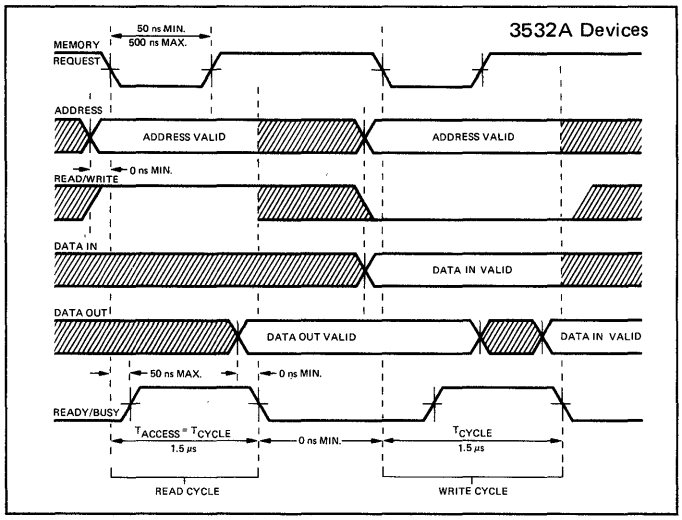


Fig. 5 Memory Interface Timing 256x8

A memory cycle begins with the MEMORY REQUEST pulse as indicated in the Interface timing diagram of Figure 5. The input ADDRESS, READ/WRITE and DATA IN (Write cycle only) lines must be firm. The BUSY signal is sent to the controller and the ϕ_1 and ϕ_2 clocks are generated by the 9602 one-shots. Since two accesses to the 3532s are required to read or write an 8-bit word, a status flip-flop determines which half-word is being processed.

The status flip-flop is a 1-bit counter and allows bits 1 through 4 to be processed during the first half cycle. During a Read cycle, the data read from the 3532s is latched on the trailing edge (negative going) of the Q output of the ϕ_2 one-shot. During a Write cycle, the multiplexer (9322) is enabled by the READ/WRITE control and bits 1 through 4 are written into the memory. Notice that input data is also latched in the output register during a Write cycle. Hence the reflected data can be checked for errors by the memory controller if desired.

An appropriate time after the trailing edge of ϕ_2, the status flip-flop is toggled. This inverts the A_8 input, conditions the multiplexer and output register for bits 5 through 8 and retriggers the ϕ_1 one-shot. The second half of the word is then processed. When the status flip-flop is toggled again, the circuitry is conditioned for bits 1 through 4, and the BUSY line is cleared. This indicates to the controller that the output data is valid and that the Read or Write cycle has been completed. The memory is now available for another request. Figure 6 illustrates the detailed internal timing.

The 256 X 8 system may use 3532 class A or class B devices. The class A system allows higher performance with worst case access and cycle times less than 1.5 μs. With class B devices, worst case cycle times are less than 2.5 μs. Power dissipation for class A or class B systems is very low. Maximum dissipation for the 256 X 8 system with worst case data and address patterns is less than 4 W excluding clock drivers. Allowing 1.5 W maximum for clock drivers brings the maximum worst case dissipation to less than 5.5 W. Maximum standby power, assuming all address and data input inverters disabled, is less than 1500 mW. The system described offers an excellent power/performance tradeoff and is very easy to interface to a memory controller.

Another application utilizing the 3532 is illustrated in Figure 7. The memory system shown is organized as a 2048-word by 8-bit array. The memory requires 32 RAMS and 14 integrated circuits for timing and control functions. As in the 256 X 8 system, two performance options are available. Class A devices will permit worst case system cycles of 850 ns. Class B systems will require 1.3 μs maximum cycles.

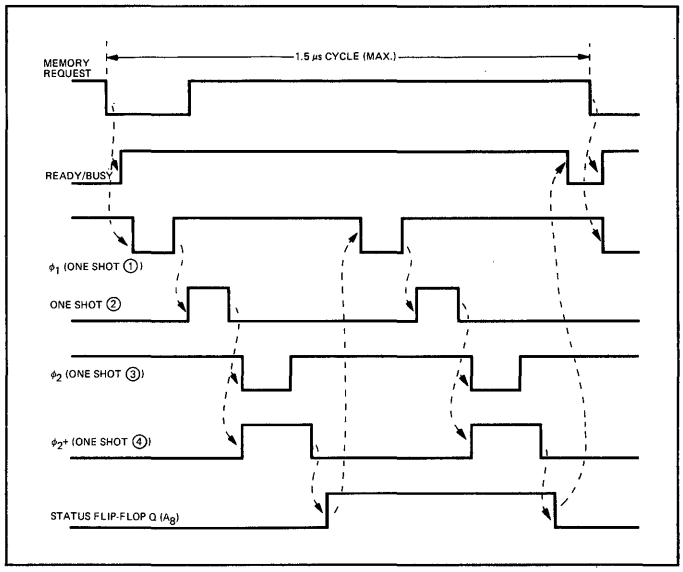


Fig. 6 Memory Internal Timing 256x8

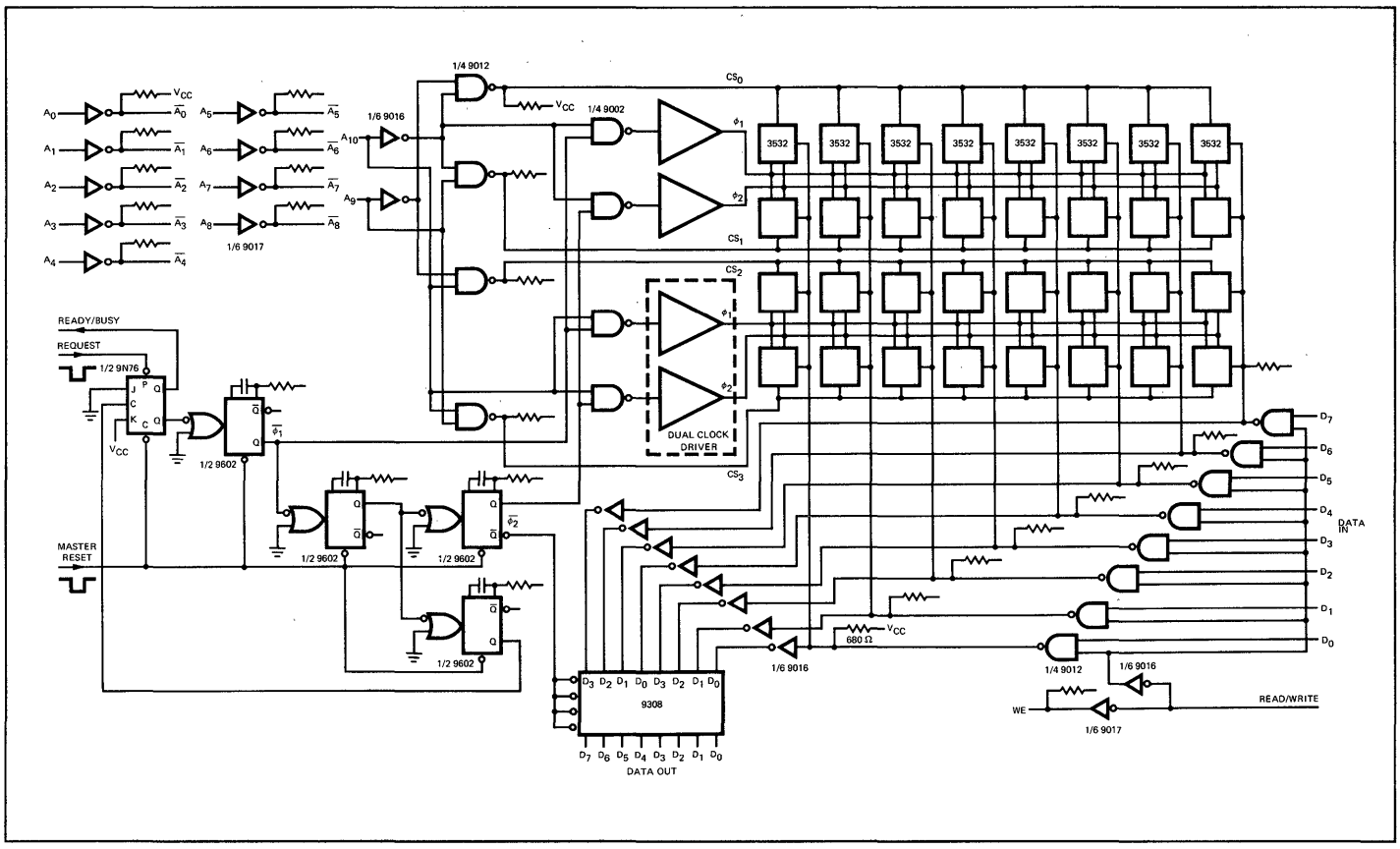


Fig. 7 Memory System 2048x8

The timing circuitry for the 2,048 X 8 system is very similar to that described for the 256 X 8 memory. It differs in that only one sequence of $\phi 1$ and $\phi 2$ pulses is generated before the BUSY signal is cleared and the cycle completed. The CHIP SELECT signals are generated from the two most significant address bits, A9 and A10. In order to reduce power dissipation and the capacitive loading on the clock drivers, $\phi 1$ and $\phi 2$ are partially decoded by A10 to determine which half of the array receives the clocks. Hence, during a cycle, 16 RAMS and one clock driver are always in the standby mode. Maximum dissipation for the 2,048 X 8 system assuming worst case address and data patterns is less than 8.5 W excluding clock drivers. With clock drivers included, maximum power will not exceed 11 W. Worst case standby power with address and data disabled is less than 3 W.

As these examples show, the 3532 is very versatile and can be organized in memory arrays ranging upward from 128 words by n-bits. A 128 word system is possible using the same approach illustrated in Figure 4. An increase in word dimension beyond 2048 can be realized by expanding the design of Figure 7. In any design, the 3532 offers many advantages including ease of operation, very low operating and standby power, minimum support circuitry and a choice of performance ranges.

3534/1103

FULLY DECODED 1024-BIT RANDOM ACCESS DYNAMIC MEMORY

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3534 is a fully decoded 1024 X 1 dynamic Random Access Memory, especially suited for main memory applications. The circuitry is designed for maximum speed and low standby power dissipation. Unlike other memories, the 3534 does not have critical clock overlap requirements. Furthermore, the write cycle can be of the same duration as the read cycle. Readout is non-destructive and the data out line may be wired-OR for ease of expansion. Exercise of the 32 row addresses is required for refresh every two milliseconds. This product is manufactured using p-channel enhancement mode silicon gate MOS technology.

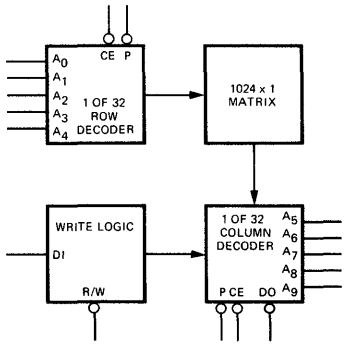
Fairchild P/N	35342	35343	35344	35345
Industry P/N	1103	1103S146	1103-1	1103-2
Access Time (ns)	300	220	180	150
Cycle Time (ns)	480	350	300	250

- **FULLY DECODED**
- **NO CLOCK OVERLAPPING REQUIRED**
- **NO CRITICAL WRITE TIMING REQUIRED**
- **FOUR SPEED RANGES**
- **ACCESS TIME – 150 TO 300 ns MAX.**
- **CYCLE TIME – 250 TO 480 ns MAX.**
- **REFRESH PERIOD – 2 ms**
- **EQUAL READ AND WRITE CYCLES**
- **CHIP ENABLE FOR EXPANSION**
- **WIRED-OR CAPABILITY**
- **18-LEAD DUAL IN-LINE PACKAGE**
- **STANDBY POWER – 2 mW MAX.**

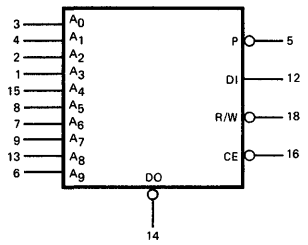
ABSOLUTE MAXIMUM RATINGS

Storage Temperature		−65°C to +150°C
Operating Temperature		0°C to +70°C
All Pins with Respect to V_{BB}	(35342)	−25 V to +0.3 V
	(35343) (35344) (35345)	−28 V to +0.3 V
Power Dissipation (package rating)		1.0 W

BLOCK DIAGRAM

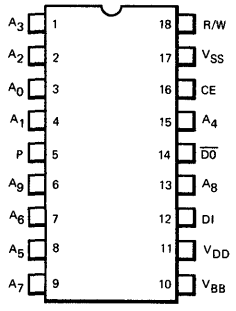


LOGIC SYMBOL



V_{BB} - Pin 10
V_{SS} - Pin 17
V_{DD} - Pin 11

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – The block diagram indicates the functions of various inputs and outputs. Inputs A_0 through A_9 select the memory cell to be accessed during a particular cycle. Precharge (P) powers the access circuitry and array columns. Chip Enable (CE) activates the row drivers and data input/output circuitry. Read/Write (RW) enables the write circuitry of the chip if the chip has been selected by CE. Data-In (DI) determines whether a HIGH or LOW level is written into the cell during the write time. V_{SS}, V_{BB} and V_{DD} are dc bias supplies. The circuit diagram (Figure 13) indicates in greater detail the circuits used for the various functions.

35342

DC CHARACTERISTICS: V_{SS} = 16 V ±5%, $V_{BB} - V_{SS}$ = 3.5 V ±0.5 V, V_{DD} = 0V, T_A = 0°C to 70°C, Note 1

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITION
V_{IL1}	Input Voltage LOW (A_0 thru A_9 and DI)	V_{SS}–17		V_{SS}–14.2	V	T_A = 0°C
V_{IL2}	Input Voltage LOW (A_0 thru A_9 and DI)	V_{SS}–17		V_{SS}–14.5	V	T_A = 70°C
V_{IL3}	Input Voltage LOW (P, CE and R/W Inputs)	V_{SS}–17		V_{SS}–14.7	V	T_A = 0°C
V_{IL4}	Input Voltage LOW (P, CE and R/W Inputs)	V_{SS}–17		V_{SS}–15.0	V	T_A = 70°C
V_{IH1}	Input Voltage HIGH (All Inputs)	V_{SS}–1.0		V_{SS}+1.0	V	T_A = 0°C
V_{IH2}	Input Voltage HIGH (All Inputs)	V_{SS}–0.7		V_{SS}+1.0	V	T_A = 70°C
V_{OH1}	Output Voltage HIGH	60	90	400	mV	T_A = 25°C, R_L = 100Ω
V_{OH2}	Output Voltage HIGH	50	80	400	mV	T_A = 70°C, R_L = 100Ω
I_{OL}	Output Current LOW			10	μA	
I_{OH1}	Output Current HIGH	0.6	0.9	4.0	mA	T_A = 25°C, R_L = 100Ω
I_{OH2}	Output Current HIGH	0.5	0.8	4.0	mA	T_A = 70°C, R_L = 100Ω
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = 0 V
I_{LO}	Output Leakage Current			1.0	μA	V_{OUT} = 0 V
I_{BB}	V_{BB} Current			100	μA	
I_{DD1}	V_{DD} Current During Precharge		37	56	mA	Note 2
I_{DD2}	V_{DD} Current During Overlap		38	59	mA	Note 2
I_{DD3}	V_{DD} Current During Chip Enable		5.5	11	mA	P = V_{SS}, CE = 0 V T_A = 25°C
I_{DD4}	V_{DD} Current Between Chip Enable and Precharge (Standby Current) Note 3			100	μA	R/W = V_{SS}, P = V_{SS} CE = V_{SS}, T_A = 25°C
I_{DD5}	Write Circuit V_{DD} Current (Note 5)			4.0	mA	P = V_{SS}, CE = V_{SS} R/W = V_{DD}, DI = V_{DD}
I_{DD}(AVG)	Average V_{DD} Current (Notes 4 & 6)		17	25	mA	Cycle Time = 580 ns tp = 190 ns, T_A = 25°C

35343, 35344, 35345 PRELIMINARY

DC CHARACTERISTICS: V_{SS} = 19 V ±1 V, $V_{BB} - V_{SS}$ = 3.5 V ±0.5 V, V_{DD} = 0 V, T_A = 0°C to 70°C, Note 1

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITION
V_{IL1}	Input Voltage LOW (A_0 thru A_9 and D1)	V_{DD}–1		V_{DD}+1	V	T_A = 0°C
V_{IL2}	Input Voltage LOW (A_0 thru A_9 and D1)	V_{DD}–1		V_{DD}+1	V	T_A = 70°C
V_{IL3}	Input Voltage LOW (P, CE and R/W Inputs)	V_{DD}–1		V_{DD}+1	V	, T_A = 0°C
V_{IL4}	Input Voltage LOW (P, CE and R/W Inputs)	V_{DD}–1		V_{DD}+1	V	T_A = 70°C
V_{IH1}	Input Voltage HIGH (All Inputs)	V_{SS} - 1.0		V_{SS} + 1.0	V	T_A = 0°C
V_{IH2}	Input Voltage HIGH (All Inputs)	V_{SS} - 1.0		V_{SS} + 1.0	V	T_A = 70°C
V_{OH1}	Output Voltage HIGH	100		600	mV	T_A = 25°C, R_L = 100Ω
V_{OH2}	Output Voltage HIGH	100		600	mV	T_A = 70°C, R_L = 100Ω
I_{OL}	Output Current LOW			10	μA	
I_{OH1}	Output Current HIGH	1.0		6.0	mA	T_A = 25°C, R_L = 100Ω
I_{OH2}	Output Current HIGH	1.0		6.0	mA	T_A = 25°C, R_L = 100Ω
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = 0 V
I_{LO}	Output Leakage Current			1.0	μA	V_{OUT} = 0 V
I_{BB}	V_{BB} Current			100	μA	

35343, 35344, 35345 PRELIMINARY

DC CHARACTERISTICS: V_{SS} = 19 V ±1 V, $V_{BB} - V_{SS}$ = 3.5 V ±0.5 V, V_{DD} = 0 V, T_A = 0°C to 70°C, Note 1 (Cont'd)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITION
I_{DD1}	V_{DD} Current During Precharge					Note 2
	35343			60	mA	
	35344			68	mA	
	35345			70	mA	
I_{DD2}	V_{DD} Current During Overlap					Note 2
	35343			68	mA	
	35344			70	mA	
	35345			75	mA	
I_{DD3}	V_{DD} Current During Overlap		5.5	11	mA	P = V_{SS}, CE = 0 V, T_A = 25°C
I_{DD4}	V_{DD} Current Between Chip Enable and Precharge (Standby Current) Note 3			100	μA	R/W = V_{SS}, P = V_{SS} CE = V_{SS}, T_A = 25°C
I_{DD5}	Write Circuit V_{DD} Current (Note 5)			4.0	mA	P = V_{SS}, CE = V_{SS} R/W = V_{DD}, DI = V_{DD}

ELECTRICAL CHARACTERISTICS
35342

Fig. 1 SUPPLY CURRENT DURING PRECHARGE VERSUS AMBIENT TEMPERATURE

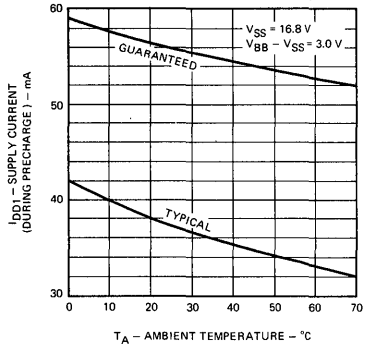


Fig. 2 SUPPLY CURRENT DURING OVERLAP VERSUS AMBIENT TEMPERATURE

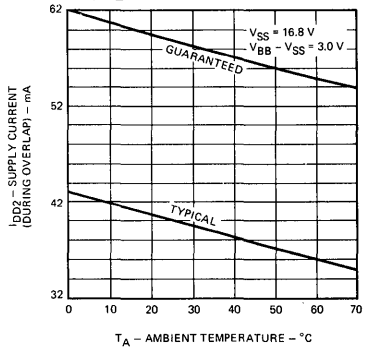


Fig. 3 SUPPLY CURRENT DURING CHIP ENABLE VERSUS AMBIENT TEMPERATURE

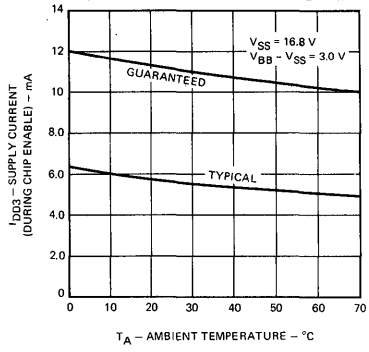
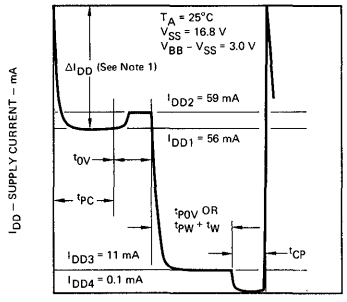


Fig. 4 SUPPLY CURRENT VERSUS TIME



(see Notes 7,8,9)

Fig. 5 OUTPUT CURRENT HIGH VERSUS SUPPLY VOLTAGE

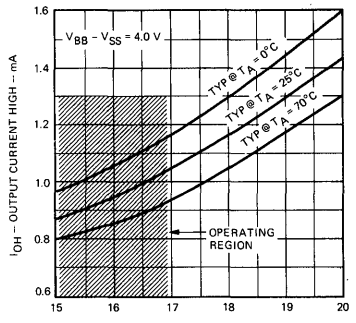
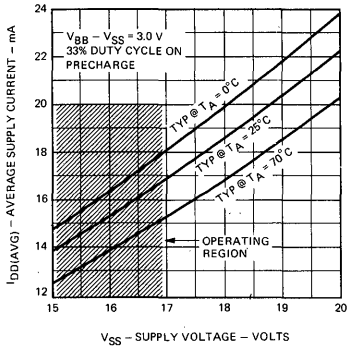


Fig. 6 AVERAGE SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



NOTES:

(1) V_{BB} supply should be applied at or before V_{SS}.

(2) A_0 through A_9 = 0, P = 0 V, T_A = 25°C. CE = V_{SS} for I_{DD1} and CE = 0 V for I_{DD2}.

(3) Total standby power for chip is: $(V_{SS} - V_{DD})\left(I_{DD4} + \frac{t_P}{t_{ref}} I_{DD1} + \frac{t_C}{t_{ref}} I_{DD3}\right)$

(4) This parameter is tested on a sample basis.

(5) I_{DD5} will be drawn only when both R/W and DI are LOW.

(6) $I_{DD\,(AVG)} = \frac{t_P}{t_{cycle}} I_{DD1} + \frac{t_C}{t_{cycle}} I_{DD3} + \frac{t_{cycle} - t_C - t_P}{t_{cycle}} I_{DD4}$

(Notes 7, 8, & 9 refer to Figure 4).

(7) ΔI_{DD} is due to charging of internal device node capacitance at precharge.

(8) These values are taken from a single pulse measurement.

(9) t_{0V} is not a required parameter, but when it occurs, current will be drawn as shown above.

AC CHARACTERISTICS: V_{SS} = 16 ±0.8 V for 35342, V_{SS} = 19 ±1.0 V for 35343, 35344 and 35345
$V_{BB} - V_{SS}$ = 3.5 ±0.5 V, $t_{rise} = t_{fall}$ + 20 ns, T_A = 0°C to 70°C

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNITS	CONDITIONS
READ, WRITE AND READ/WRITE CYCLE						
t_{ref}	Time Between Refresh Cycles			2.0	ms	
t_{AC}	Address to Chip Enable Time	35342	115		ns	
		35343	70		ns	
		35344	60		ns	
		35345	50		ns	
t_{CA}	Chip Enable to Address Time	35342, 35343	20		ns	
		35344, 35345	10		ns	
t_{PC}	Precharge to Chip Enable Time	35342	125		ns	
		35343	70		ns	
		35344	60		ns	
		35345	50		ns	
t_{CP}	Chip Enable to Precharge Delay	35342	85		ns	
		35343	40		ns	
		35344, 35345	30		ns	
t_{AP}	Address to Precharge Time	35342	115		ns	
		35343	90		ns	
		35344	80		ns	
		35345	70		ns	
t_C	Chip Enable Width	35342	210	850	ns	
		35343	180	700	ns	
		35344	150	600	ns	
		35345	110	500	ns	
t_P	Precharge Width	35342	170		ns	
		35343	90		ns	
		35344	80		ns	
		35345	70		ns	
READ CYCLE						
t_{RC}	Read Cycle Time	35342	480		ns	
		35343	350		ns	
		35344	300		ns	
		35345	250		ns	
t_{CO}	Chip Enable to Output Delay	35342		165	ns	
		35343		130	ns	
		35344		100	ns	
		35345		80	ns	
t_{ACC1}	Address to Output Access	35342	300		ns	R_L = 100Ω, C_L = 100 pF
		35343	220		ns	Note 10
		35344	180		ns	
		35345	150		ns	
t_{ACC2}	Precharge to Output Access	35342	310		ns	R_L = 100Ω, C_L = 100 pF
		35343	220		ns	Note 10
		35344	180		ns	
		35345	150		ns	
WRITE CYCLE						
t_{WCY}	Write Cycle	35342	480		ns	
		35343	350		ns	
		35344	300		ns	
		35345	250		ns	

AC CHARACTERISTICS: (Cont'd) V_{SS} = 16 ±0.8 V for 35342, V_{SS} = 19 ±1.0 V for 35343, 35344 and 35345
$V_{BB} - V_{SS}$ = 3.5 ±0.5 V, $t_{rise} = t_{fall}$ + 20 ns, T_A = 0°C to 70°C

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNITS	CONDITIONS
WRITE CYCLE (Cont'd.)						
t_{CR}	Chip Enable to End of Write	35342	210		ns	Note 11
		35343	180		ns	
		35344	150		ns	
		35345	110		ns	
t_{WP}	Write Pulse Width	35342	80		ns	
		35343, 35344	50		ns	
		35345	40		ns	
t_{DW}	Data Setup Time	35342	105		ns	Note 12
		35343, 35344	60		ns	
		35345	50		ns	
t_{DH}	Data Hold Time		10		ns	Note 12
t_W	Write Setup Time	35342	80		ns	
		35343, 35344	50		ns	
		35345	40		ns	
READ/WRITE CYCLE						
t_{RWC}	Read/Write Cycle	35342	580		ns	Note 13
		35343	400		ns	
		35344	360		ns	
		35345	320		ns	
t_{DOW}	Data Out to Read/Write Delay		0		ns	
CAPACITANCE						
C_A	Address Capacitance			7.0	pF	$V_{IN} = V_{SS}$, $V_{BB} = V_{SS}$ + 3.0 V
C_P	Precharge Capacitance			20	pF	
C_{CE}	Chip Enable Capacitance			20	pF	
C_{RW}	Read/Write Capacitance			15	pF	
C_{I1}	Data Input Capacitance			10	pF	CE = 0 V
C_{I2}	Data Input Capacitance			5.0	pF	CE = V_{SS}
C_O	Data Output Capacitance			4.0	pF	V_{OUT} = 0 V

NOTES:
(10) V_{ref} is 40 mV for 35342, and 70 mV for 35343, 35344 and 35345.
(11) t_{CR} is referenced to the rising (positive going) edge of CE or R/W, whichever occurs first.
(12) t_{DW} and t_{DH} are referenced to the rising (positive going) edge of CE or R/W, whichever occurs first.
(13) t_{RWC} assumes a t_{DOW} of 45 ns for the 35342 and 30 ns for the 35343/4/5. This is to allow for changing of data if data is ready. This cycle time can be shorter by 40 ns for the 35342 and 30 ns for the 35343/4/5. If longer t_{DOW} is required, the cycle time till increase proportionally.

TIMING DESCRIPTION — When CE is HIGH (CE is LOW) and Precharge goes LOW, the column precharge enable switches are turned on and allow precharging of the columns. All row address decoders and half of the column decoders (determined by A_8), are also charged LOW. Addresses must then stabilize and all but one row decoder and one column decoder will be pulled HIGH. A_8 is redundantly decoded and ANDed with the load device of the column decoders such that only 16 of the 32 decoders draw power when Precharge is LOW. This reduces the power dissipation of the column decoders.

Precharge can go HIGH when all the decoders are stabilized, imposing no critical Precharge and Chip Enable timing requirement. The only requirement is that Precharge remain in the LOW state long enough to precharge the columns and to power up the decoders and address inverters. Chip Enable drives one of 32 rows that is selected by the row decoders, thus selecting all 32 cells in that row. The cells are cross coupled latches with no load devices. Depending on the state of the bit (HIGH or LOW), one of the columns will be discharged and the other one remains charged. The charge stored on the columns refresh the storage node in the cell. This is due to charge sharing between column capacitance and the storage node. Since the capacitance of the column is much larger than the capacitance of the storage node, the storage node voltage is refreshed almost to the same voltage as the precharged column. Also, due to the regenerative action and the fact that the cell is being refreshed while accessed, the access time of the memory is short, consistent and insensitive to time between refresh.

The column and write switches selected by the column decoders and Read/Write direct data in and out of the selected column. Because of the nature of the cell, data is inverted on chip. The inverter, however, consumes power only when Read/Write is LOW.

Since no refresh amplifiers are necessary, the Read/Write timing is not critical (see Write Cycle timing diagram), and need not be a pulse.

The timing diagrams show three basic cycles; Read, Write and Read/Write. As shown, the Read and Write cycles are the same length and the Read/Write cycle is somewhat longer. It is apparent that the critical times are minimized in order to facilitate ease of system implementation.

When R/W, CE and P are all HIGH, there will only be leakage current flowing into V_{DD}, thus reducing standby power to practically zero.

TIMING DIAGRAMS

READ CYCLE

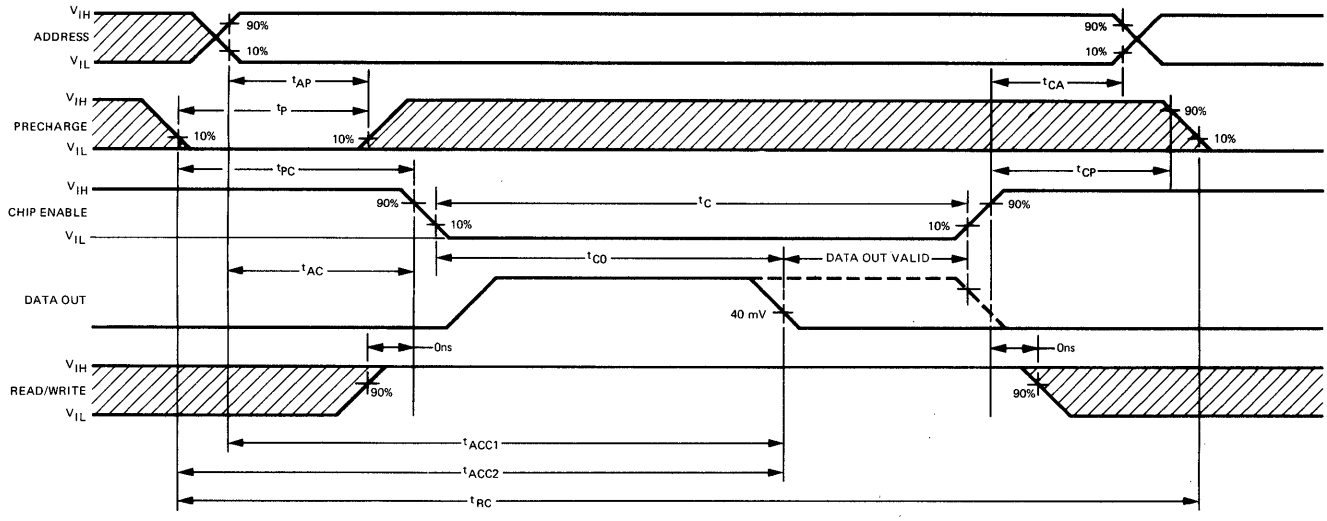


Fig. 7

WRITE CYCLE

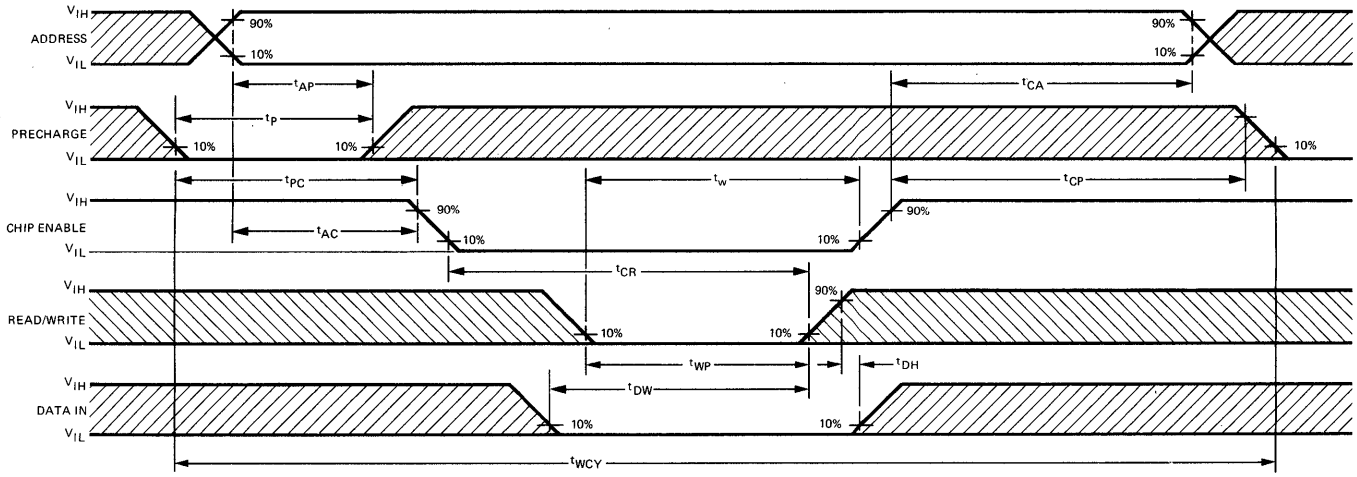


Fig. 8

READ/WRITE CYCLE

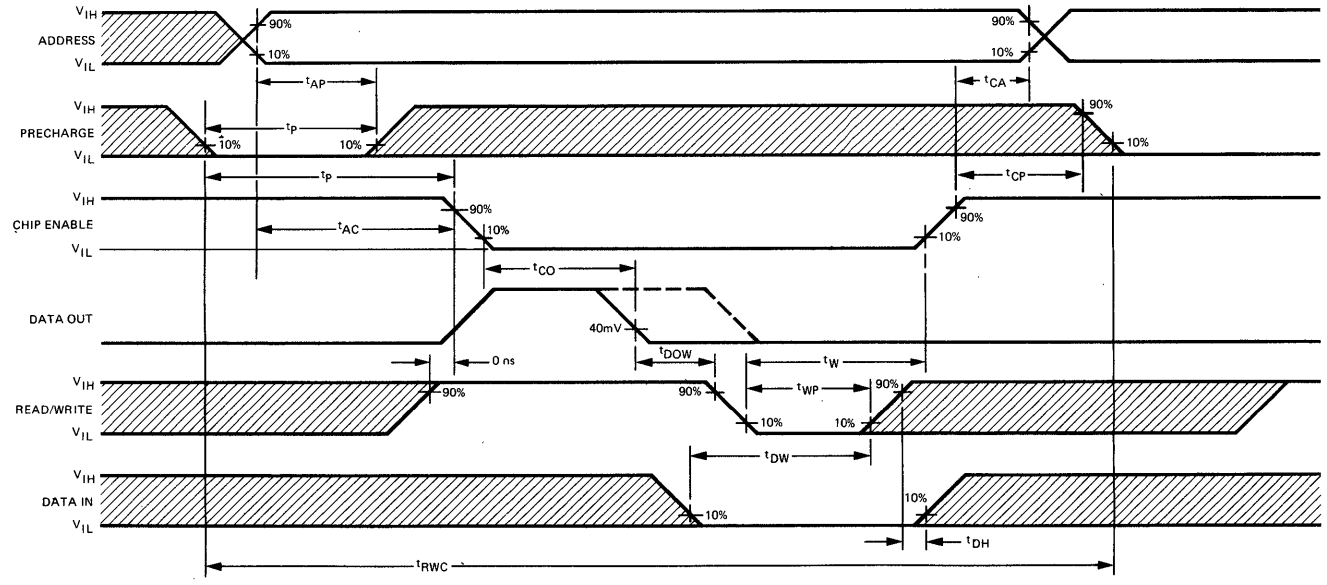


Fig. 9

PARTIAL SCHEMATIC DIAGRAM

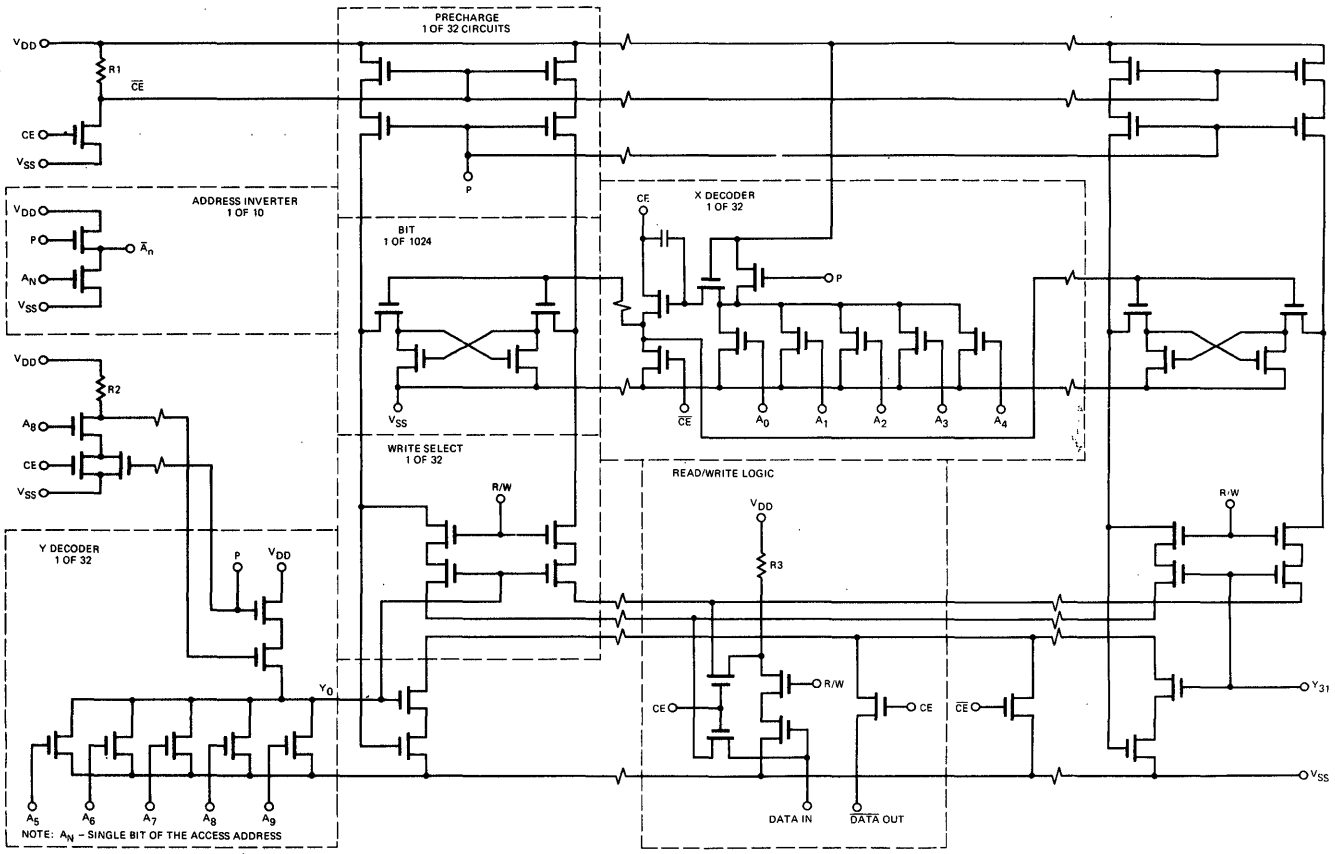


Fig. 10

GLOSSARY OF TERMS

P	Precharge
CE	Chip Enable
R/W	Read/Write
DI	Data In
DO	Data Out Complemented
V_{BB}	Substrate Bias
V_{SS}	Positive Circuit Bias
V_{DD}	Negative Circuit Bias
A_n	Single Bit of the Access Address.

MEMORY SYSTEM DESIGN WITH THE 3534/1103 DYNAMIC MOS RAM

There are several Silicon-Gate MOS Random Access Memory devices available to memory system designers, both static and dynamic. The most popular SiGate MOS RAM is the 1103, standard and improved versions. This device is becoming an industry standard because it is available and it offers high performance potential, despite some difficulties with its use in memory systems.

The Fairchild interpretation of the 1103 is a fully decoded, dynamic 1024 x 1-bit MOS random access memory. This circuit has been designed to minimize the design and operational difficulties of memory systems and does this as an exact, lead-for-lead functional equivalent of the 1103. Although the 3534/1103 can be considered functionally identical to the 1103, a number of unique characteristics can provide superior performance, lower power dissipation, lower cost and easier use in new system designs as well as in existing 1103 systems. These unique characteristics and their ramifications at the system level offer design, cost and performance benefits to the memory system manufacturer and user.

This design guide is partitioned into four sections, each discussing different aspects of memory system design with the 3534/1103. Section I describes the operation and characteristics of the Fairchild 3534/1103, the internal circuitry (memory cell, decoders, drivers and control logic), the unique interface characteristics, and the inherent advantages of the design approach.

The system implications of the 3534 with respect to system access time, cycle time and power dissipation are considered and compared to 1103 performance in Section II. The superior performance of a 3534 system, basically a result of reduced clock skew and the elimination of many timing constraints, is documented. The reduced dependence on level shifting circuits is explained. Very low power dissipation, characteristic of 3534 systems, is also discussed.

3534/1103 basic storage board design considerations, performance improvements, and/or cost reductions attributable to the 3534 are examined in Section III. Interface circuit requirements are determined and examples of peripherals are shown. The "hows" of minimizing storage board power dissipation and PC board layout are considered.

In Section IV, typical approaches to memory system timing and control logic design are illustrated. The refresh requirements of the 3534/1103 and associated circuitry are illustrated. Examples of timing and control circuitry are also shown with attention to the component reduction possible in a 3534 system.

Since system cost and performance are the fundamental factors influencing MOS memory system design, the additional advantages of the 3534 compared to the 1103 are emphasized. Many applications do not have well-defined cost or performance boundaries. Thus the memory system designer should examine a number of alternate designs before committing to one which optimizes his system. This handbook illustrates that the best memory device for use in small, medium or large memory systems is the Fairchild 3534/1103.

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I FUNCTIONAL CHARACTERISTICS AND DESCRIPTION

INTRODUCTION

The Fairchild 3534/1103 can be considered as having two modes of operation. Operated in the 3534 mode, significant reductions in system cost and/or increases in performance are possible when compared to an equivalent 1103 type system. In this mode, the full advantages of the unique characteristics and improvements designed into the 3534/1103 are realized.

In its alternate mode, the device can be operated with the identical timing and interface requirements characteristic of the 1103. The 3534 can therefore be used in existing 1103 systems without modification to the system timing, control, or interface circuitry. Operation in this mode in fact enhances the existing system's timing tolerances and for most designs, also reduces power dissipation at the system level. Furthermore, many 1103 systems can improve worst case access times simply by sampling output data earlier in the cycle.

IMPROVEMENTS IN THE 3534/1103

The improvements in the 3534/1103 are basically the reduction of standby power and the elimination of many external timing constraints. The interface characteristics and some of the system advantages that result are listed below and examined in detail in the chapter covering System Implications.

1. PRECHARGE and CHIP ENABLE overlap requirements are eliminated. This feature leads to simplified timing, control, and interface circuitry and faster access and cycle times.
2. Output data is referenced to the negative-going edge of CHIP ENABLE, not to the positive-going edge of PRECHARGE. This feature permits faster access times since precharge clock skew is eliminated and level shifter rise times are not a factor.
3. Read and write cycle times are equal (480 ns max). System timing is simplified since only one timing chain is required for optimum read and write cycle times.
4. READ/WRITE is specified as a level, not as a pulse. The timing circuitry and decoder logic associated with the write pulse are not required, resulting in fewer components and faster write cycles.
5. Standby current is reduced from 4 mA to 100 μA. System power is reduced significantly.

DYNAMIC MEMORY CELL DESIGN

The high bit densities required for an MOS memory chip have resulted in a number of dynamic memory cell designs which capitalize on the near zero input current requirements of an MOS transistor. In these designs, information is stored as the presence or absence of charge on a gate capacitor and then sensed when the cell is accessed. Internal or external cell sensing is possible and the procedure may be destructive or regenerative. In any case, the cell must be periodically accessed to replenish the stored charge which decays due to junction leakage associated with the access and sense devices. This is why MOS memories using these types of cells are referred to as dynamic and must be "refreshed". This refreshing procedure varies with different cell designs and in most cases, refreshing must occur approximately every two milliseconds (at 70° C) to insure data is maintained. At lower temperatures, refresh cycles may not be required for hundreds of milliseconds (typically).

Memory cell design for a dynamic MOS RAM has a considerable effect on the circuit design at the chip level and on the logic design at the system level. At the system level, the performance of the memory device and easy incorporation in a memory system are two important considerations. The 3534/1103 memory cell has been carefully designed to maximize system performance and minimize interface requirements.

Basically, there are three approaches to dynamic memory cell design. The first, shown in Figure 1.1, is a 1-transistor cell representing the minimum component design approach to the memory cell. A single capacitor is charged to a "1" or a "0" level by the column line when it is accessed during a write cycle (row select enabled). During a read cycle, the charge on the capacitor modifies the voltage on the floating column line. This modified voltage is then sensed by an internal amplifier. To sense the state of the cell externally, the internal amplifier must provide significant power gain. The magnitude of this gain is inversely related to the size of the capacitor, implying that a large capacitor is desirable. However, to achieve high bit densities, the size of this capacitor must be minimized. For an optimum design, the resulting capacitance turns out to be smaller than the parasitic capacitance of the column line. As a result, destructive readout occurs and the cell contents must be rewritten after every read cycle.

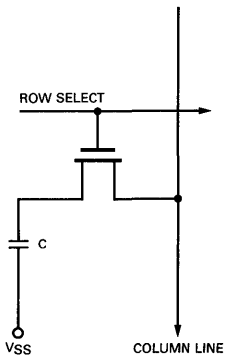


Fig. 1.1 1-Transistor Cell

To restore the data, additional peripheral logic and a clock phase are required within the memory chip, causing more complex timing requirements at the system level. In addition, the magnitude of the column parasitics may necessitate redundant decoding and a division of the column lines to reduce the number of cells sharing the line. This type of cell does not use to advantage the inherent voltage gain capability of an active device and does not lend itself to a simplified chip interface.

A 3-transistor cell can be designed (Figure 1.2) employing active voltage gain within the cell. Although this cell has more components and access lines than the single transistor cell, its size is comparable because the storage capacitor can be much smaller due to the power gain provided by the active device (Q_1). This is the type of cell used in conventional 1103 memory designs.

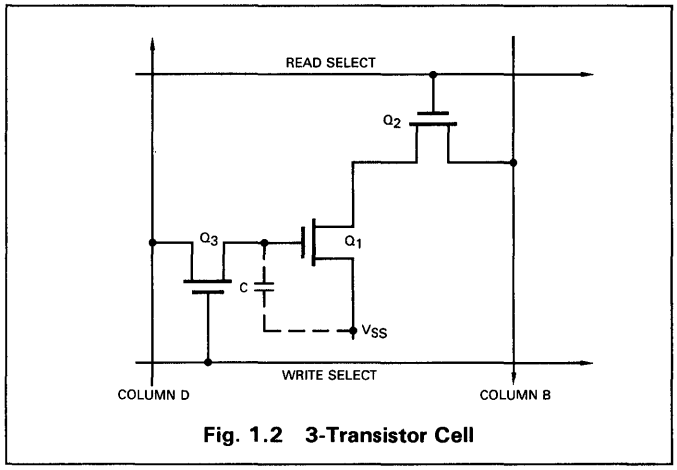


Fig. 1.2 3-Transistor Cell

Information is stored as charge on a capacitor which, in this case, is the capacitance associated with the gate of a relatively large active device (Q_1). To access the cell, Columns B and D are first precharged to some negative potential near V_{DD} at the beginning of a cycle. The read select line is then enabled and transmission device Q_2 can conduct. If the voltage on the gate of Q_1 exceeds device threshold, Q_1 conducts and Column B discharges to a potential near V_{SS}. If the potential on the gate of Q_1 (charge on C) is not sufficient to turn Q_1 on, Column B remains precharged at the negative potential. The condition of Column B is then sensed by an on-chip amplifier.

To refresh this type of cell, information on Column B must be inverted and rewritten into the cell. This is achieved by an on-chip "refresh" or "column" amplifier which discharges Column D if Column B remains precharged. If Column B is discharged by the memory cell, Column D remains precharged. The write select line is then enabled and the gate of Q_1 assumes a potential near that of Column D, refreshing the cell. For a write cycle, new information is placed on Column D and stored in the cell.

As can be appreciated, precise timing is required to perform this operation. In the 1103, the potential of Column D is critically related to the overlap time between the PRECHARGE and CHIP ENABLE controls. The information stored in the cell can be adversely affected if that overlap time violates a minimum or maximum limit. This overlap timing constraint presents difficulties to the system designer because of the restrictions it places on system timing tolerances and interface circuits. Furthermore, on-chip power dissipation is increased in the standby mode as a result of the internal logic used to control the refresh amplifiers.

Figure 1.3 illustrates a third alternative for a dynamic memory cell design — the alternative chosen for the 3534. This cell design interconnects four transistors to form a latch very similar to the flip-flop circuits used in static memories. The cell is dynamic, however, since no load devices (resistors) are used. Information is stored on the gate capacitance of Q_1 and Q_2. Because two devices are used, both the information and its complement are available to the internal sensing logic. Although the cell area has been increased and another interconnection is required, a very significant reduction of on-chip peripheral circuitry and simplified operation are obtained.

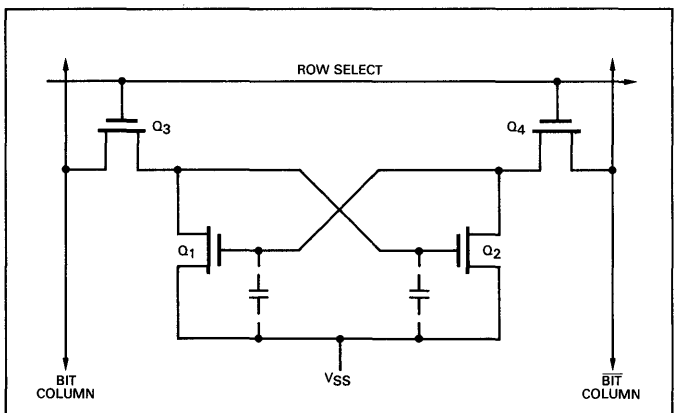


Fig. 1.3 4-Transistor Cell

At the start of a cycle, the column lines (BIT and $\overline{BIT}$) are precharged to a potential near V_{DD}. The row select line is then enabled and transistors Q_3 and Q_4 can conduct. If the potential at the gate of Q_1 is sufficient, Q_1 conducts and the BIT line discharges to a potential near V_{SS}. Simultaneously, the gate of Q_1 is "refreshed" to the potential of the $\overline{BIT}$ line because Q_2 is not conducting. The gate of Q_2 is also "refreshed" as the potential of the BIT line discharges toward V_{SS}. If Q_2 were initially conducting, the procedure is reversed. The state of the cell is then sensed after the conditional discharge of the BIT line. For a write cycle, new data and its complement are placed on the BIT and $\overline{BIT}$ lines, and the gates of Q_1 and Q_2 assume their respective potentials.

The refresh procedure and cell access are identical. This design requires neither special refresh amplifiers nor the timing constraints associated with them. The cell access is regenerative and the active gain capabilities of the MOS devices are used to full advantage. In addition, the potential on the gate of the conducting device in each cell need not exceed threshold voltage since accessing the cell refreshes the node charged to the higher potential. This increases the internal safety margin; with the 1103 3-device cells, the storage node potential must exceed threshold to maintain a logic "1".

These features improve reliability and simplify chip timing requirements to permit easy implementation in a memory system. Specifically, there is no requirement for a PRECHARGE/CHIP ENABLE overlap during operation. Even if this overlap occurs, it does not affect the operation of the device. On-chip standby power is also minimized since the refresh amplifier control circuits required with a 3-device cell design are eliminated.

3534/1103 INTERFACE SIGNALS

The 3534 uses three external control signals in conjunction with address and data to direct the cell operation and control the internal circuitry. Two positive voltages (V_{SS} and V_{BB})

are also required. The input and output signals are defined as follows:

1. PRECHARGE (PCHG or P) — This signal is required at the start of a memory cycle to pre-condition the memory array columns and peripheral circuitry. Because of the dynamic design of the internal logic, this signal may be considered a "power-enable" or power-on switch.
2. CHIP ENABLE (CE or CENBL) — This signal enables the outputs of the row decoders permitting a row of cells to be accessed. Also, CE gates data into or out of the device and controls the precharging of the memory array columns.
3. READ/WRITE (R/W) — This signal specifies a read or write cycle and permits new data to enter the memory.
4. ADDRESSES A_0 - A_4 — These are the addresses that specify one of the 32 rows of the memory array. For refreshing, these five address bits must be cycled through their 32 combinations every two milliseconds.
5. ADDRESSES A_5 - A_9 — These addresses select one of the memory array's 32 columns.
6. DATA IN — This is the logical information to be stored at the memory location specified by the address.
7. $\overline{\text{DATA}}$ OUT — This is the logical information read from the specified memory location during a read cycle. Data is indicated by the presence or absence of a 500 μA current. A LOW level (near V_{DD}) written into the 3534 results in the high current output.

3534 ORGANIZATION AND PERIPHERAL CIRCUITRY

The 3534/1103 block diagram (Figure 1.4) depicts the organization of the memory chip. The memory cells are partitioned into two 32-row by 16-column matrices to minimize the time constant of the row select lines. Each column of memory cells is associated with a precharging circuit and a column decoder. In addition, control logic and inverter circuits are indicated. Because the basic 4-transistor cell design requires minimum internal support circuitry, a very favorable ratio of memory to peripheral circuit area results.

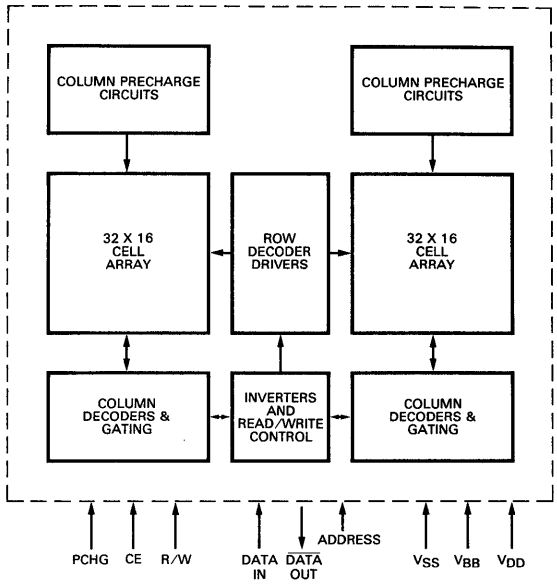


Fig. 1.4 3534/1103 Memory Chip Organization

The peripheral circuits must perform a number of functions including address inversion, control signal inversion, address decoding, row and column selection, read/write cycle control, and data input/output buffering. Figure 1.5 is a partial schematic diagram of the 3534/1103 and identifies the memory cell and its interconnection with this support circuitry. A description of the function and operation of the peripheral circuits follows.

1. MATRIX PRECHARGE CIRCUIT (one of 32) — These circuits charge the BIT and $\overline{\text{BIT}}$ lines of the memory array columns to a potential near V_{DD} when the CE control is HIGH (near V_{SS}) and the PCHG control is LOW. The column lines are thus pre-conditioned prior to cell selection. When CE is LOW, the circuit is disabled and the BIT and $\overline{\text{BIT}}$ lines are isolated from V_{DD}.
2. ADDRESS INVERTER (one of 10) — The address inverters generate the complement of the 10 address bits required for decoding. When PCHG is LOW, the address complements are generated as the voltages at the $\overline{A_n}$ nodes stabilize. When PCHG goes HIGH, the inverter outputs remain at the correct logic levels if the input address does not change. The inverter circuits do not dissipate power when PCHG is HIGH.
3. ROW DECODER/DRIVER (one of 32) — The row decoder/drivers (X-decoders) select one of the 32 array rows to be accessed. These circuits have two stages of operation; the first is decoding which occurs when PCHG is LOW. Each decoder is equivalent to a 5-input NAND gate with a LOW output only when all five address inputs are HIGH. Thus, for any cycle, only one decoder output can be LOW. When PCHG goes HIGH, the logic level at the decoder output remains stable and power is no longer dissipated by the circuit.

   The actual selection of a row of cells occurs after the negative excursion of CHIP ENABLE. For the decoder with a LOW output, the gate of the drive transistor is forced to a potential near V_{DD}. When CE goes LOW, the decoupling transistor of the selected row turns off, the row select line corresponding to the decoded row is driven LOW, and the row of cells is enabled.
4. COLUMN DECODE (one of 32) — The column or Y-decoders select one of the 32 columns of the memory array. Since the Y-decoder outputs do not drive a significant load, the driver stage used with the X-decoder is not necessary. To reduce power dissipation, A_8 and $\overline{A_8}$ enable alternate halves of the column decoders, so only 16 of the decoders dissipate power during a cycle. During standby, PCHG and CE are HIGH and disable the A_8 inverter to eliminate power dissipation.
5. READ/WRITE LOGIC — The read/write control logic generates the complement of the data on the Data In line when R/W is LOW. When CE goes LOW, the DATA buss assumes the logic level of the Data In line and the $\overline{\text{DATA}}$ buss is forced to a potential near V_{DD}. When R/W goes LOW, the $\overline{\text{DATA}}$ buss is placed at a potential near V_{SS} only if the Data In line is LOW. Since a load resistor (R_3) has been provided to generate the required level on the $\overline{\text{DATA}}$ buss, the R/W control may go LOW before or during CE and Data In may change while CE and R/W are LOW. This technique eliminates timing constraints on the R/W signal and permits faster write cycle times at the system level.

6. WRITE SELECT (one of 32) — The write select circuits are extensions of the column decoders. During a write cycle, the decoded column is accessed for writing when R/W goes LOW and the new data and its complement (potentials on DATA and $\overline{DATA}$ lines) are placed on the BIT and $\overline{BIT}$ lines. The circuit is disabled during a read cycle.
7. OUTPUT CIRCUIT (one of 32) — Each BIT column drives its own sensing transistor to minimize the capacitive loading on the column. Each sensing device is gated by the Y-decoders and CE, allowing only one BIT line to control the output. When CE goes LOW, an output current appears indicating that the BIT line of the selected column (and all the other columns) has been precharged. If the BIT line is then discharged by the cell, the output current is terminated, indicating a logic "0".

OPERATION OF THE 3534/1103

The operation and sequence of control signals required by the 3534 is explained by the read cycle diagram (Figure 1.6) and the ac characteristics in Table 1.1. A memory cycle normally begins with the negative excursion of PCHG. PRECHARGE must remain in the LOW state for at least t_P (170 ns) to insure that the array, decoders and inverters are properly pre-conditioned. If PCHG is held LOW for a number of cycles, this condition is automatically satisfied. After this interval elapses, PCHG can go HIGH at any time, independent of CE. The ten address inputs must be stable at least t_{AP} (115 ns) before PCHG goes HIGH.

After the array circuitry has been precharged for at least t_{PC} (125 ns), CHIP ENABLE can go LOW. The address must be firm t_{AC} (115 ns) prior to this transition. When CE goes LOW, the column precharging is disabled, the selected row decoder/driver is enabled, and the 32 cells in that row are accessed. The selected cells are automatically refreshed and the BIT line is sensed. Data is available for a read cycle t_{CO} (165 ns max) from the CE transition. For a read cycle, the R/W line must be high before the CE transition to prevent the selected cell from being perturbed by the read/write logic.

To guarantee proper refresh and access, CE must be LOW for at least t_C (210 ns). CE can then go HIGH to begin precharging the array columns for the next cycle. The address must remain firm for at least t_{CA} (20 ns) after the positive transition to prevent the decoder outputs from changing. To generate $\overline{CE}$ on chip, t_{CP} (85 ns max) is required before PCHG can again activate the pre-conditioning circuits. If for some reason CE is terminated early, the row of selected cells may not be completely refreshed. However, the state of each cell is not altered because of the inherently stable flip-flop circuit used in the cell design. The fact that data cannot be altered in this case is important when refresh cycles are abandoned in favor of memory cycles to guarantee access times at the system level.

For a write cycle (Figure 1.7), R/W must be LOW for t_{WP} (80 ns) while CE is LOW to perform the write operation. R/W can go LOW at any time during the cycle and can stay low if consecutive write cycles are being executed. R/W can thus be considered a level. The actual writing of new information is dependent upon the positive-going edge of CE or R/W, whichever occurs first. Therefore, data is referenced to the positive edge of CE or R/W and must be stable at least t_{DW} (105 ns) before the positive transition of either. After the transition, data must be held for t_{DH} (10 ns) to permit the read/write logic to isolate the DATA and $\overline{DATA}$ busses from the Data In line. The write cycle is then completed in the same manner as the read cycle.

The diagram of Figure 1.8 characterizes a read-modify-write cycle. New data can be written into the same memory location immediately after a read operation by elongating CE and bringing R/W LOW. After satisfying the write cycle requirements, the cycle can be terminated.

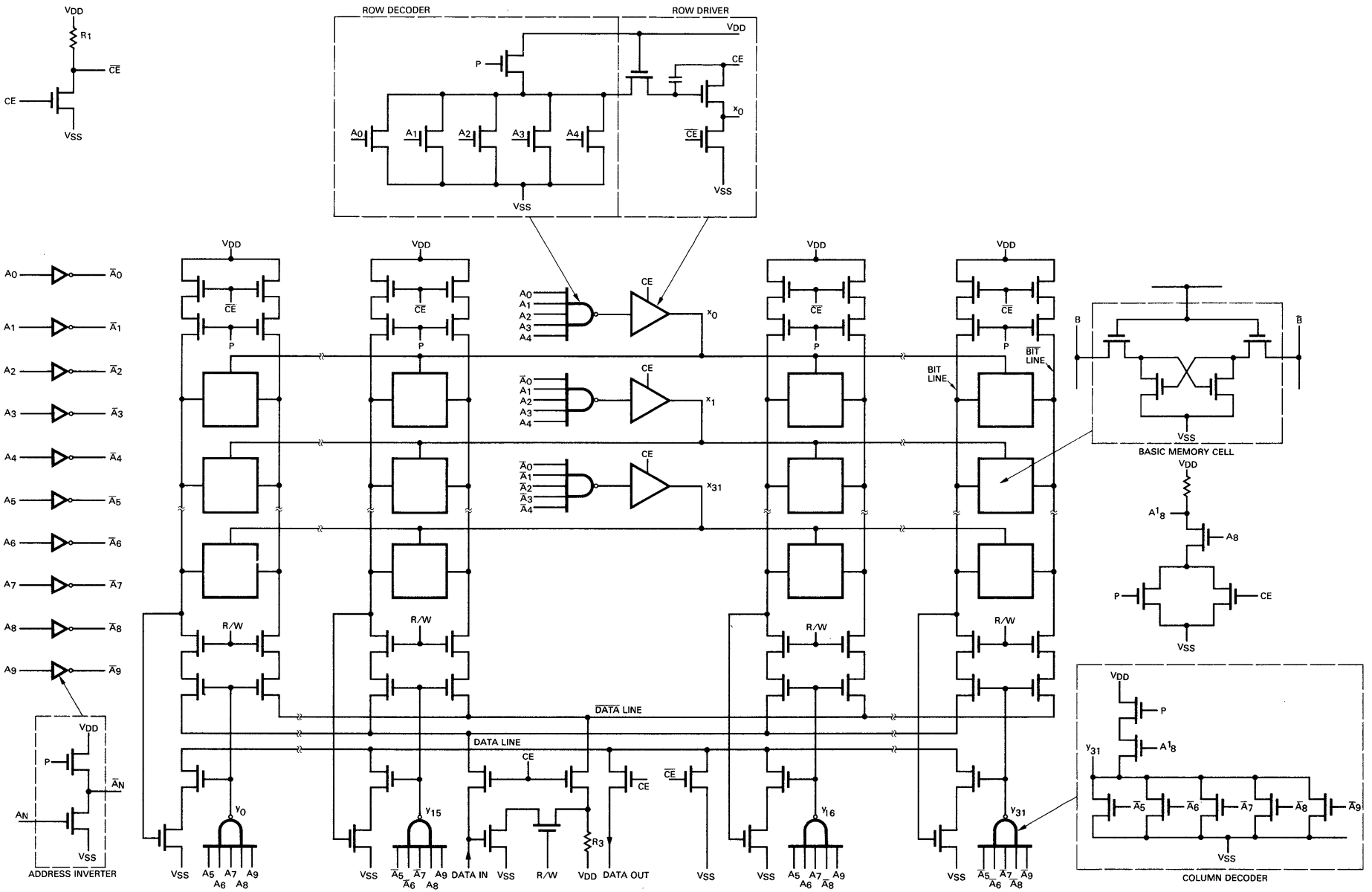


Fig. 1.5 3534/1103 Partial Schematic Diagram

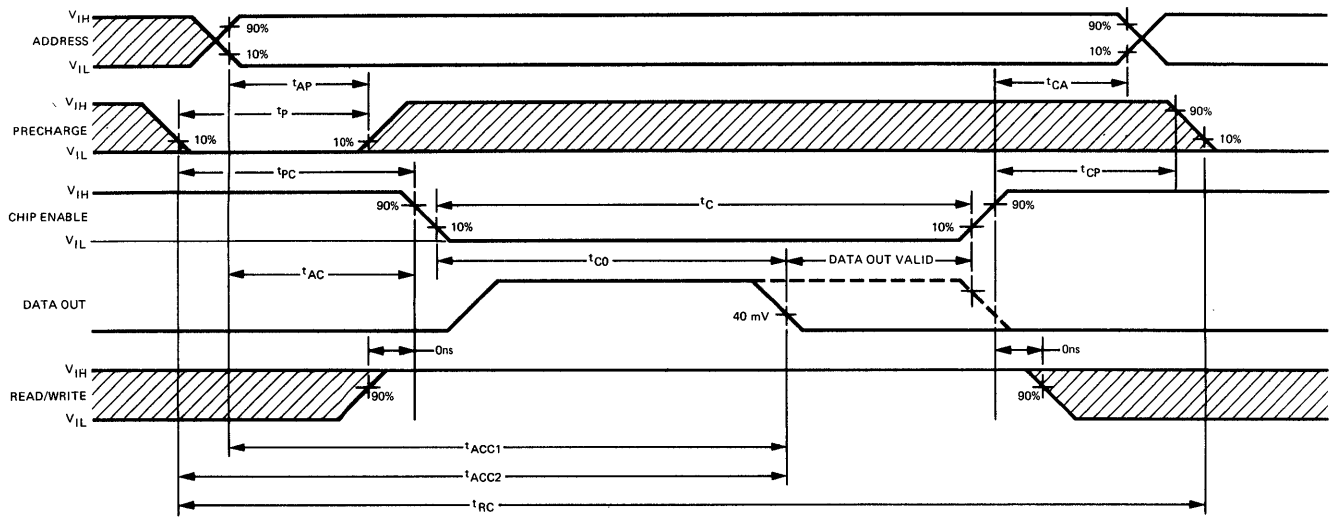


Fig. 1.6 3534 Read Cycle

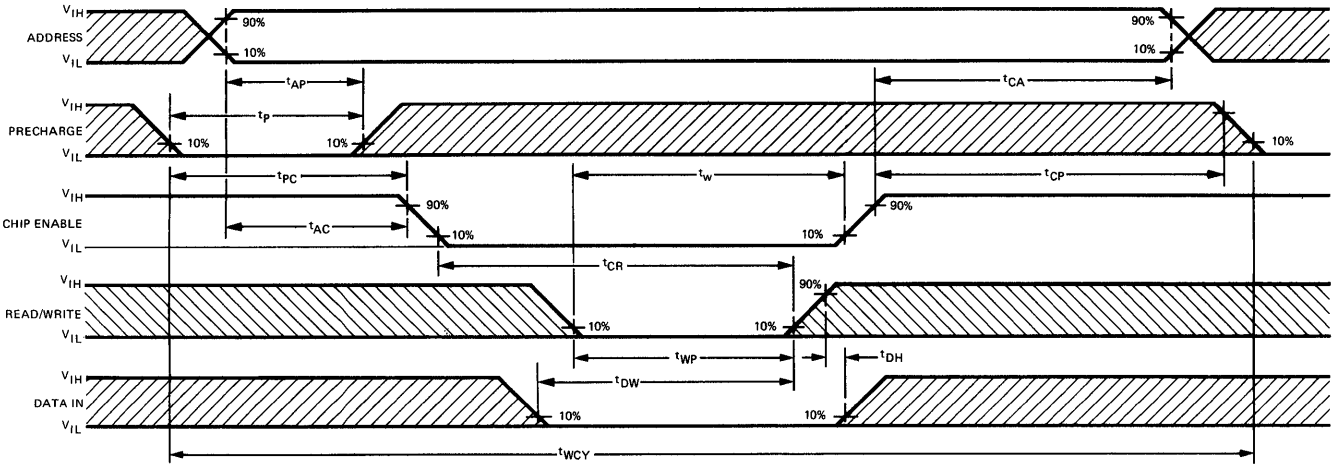


Fig. 1.7 3534 Write Cycle

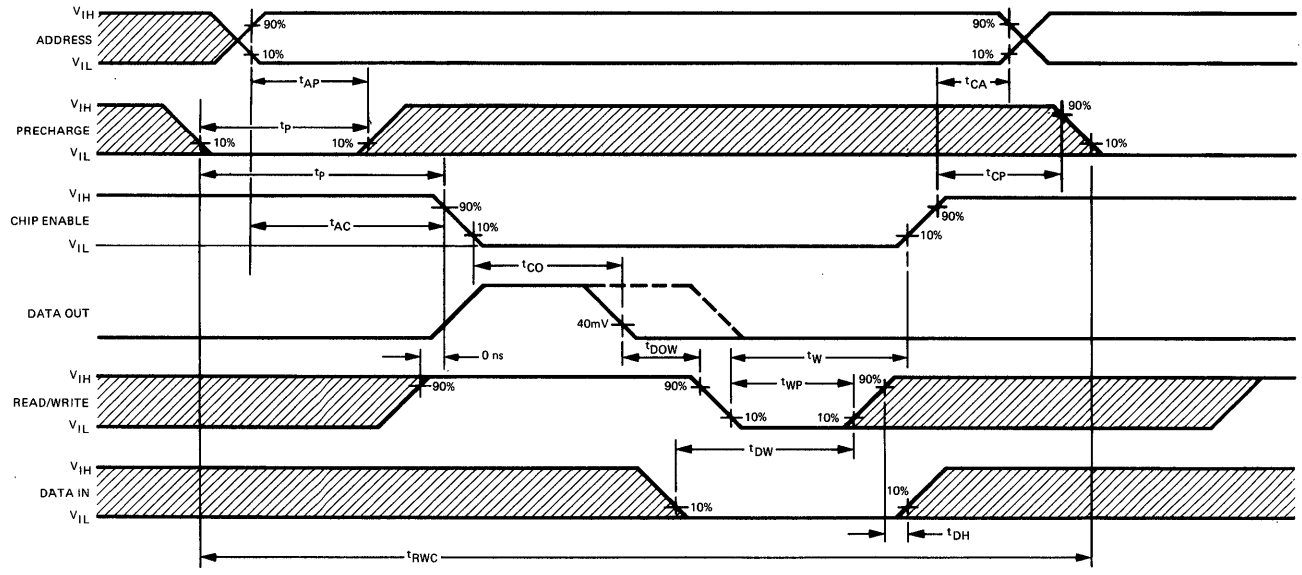


Fig. 1.8 3534 Read/Write Cycle

AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{SS} = 16 V ±5%, V_{BB} - V_{SS} = 3.5V±0.5V, V_{DD} = 0 V, t_{rise} = t_{fall} = 20 ns

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	READ, WRITE, AND READ/WRITE CYCLE					
t_{ref}	Time Between Refresh Cycles			2	ms	
t_{AC}	Address to Chip Enable Time	115			ns	
t_{CA}	Chip Enable to Address Time	20			ns	
t_{PC}	Precharge to Chip Enable Time	125			ns	
t_{CP}	Chip Enable to Precharge Delay	85			ns	
t_{AP}	Address to Precharge Time	115			ns	
t_C	Chip Enable Width	210		850	ns	
t_P	Precharge Width	170			ns	
t_{RC}	Read Cycle Time	480			ns	
t_{CO}	Chip Enable to Output Delay			165	ns	
t_{ACC1}	Address to Output Access	300			ns	R_L = 100 , C_L = 100 pF
t_{ACC2}	Precharge to Output Access	310			ns	R_L = 100 , C_L = 100 pF
	WRITE CYCLE					
t_{WCY}	Write Cycle	480			ns	
t_{CR}	Chip Enable to End of Write	210			ns	Note 7
t_{WP}	Write Pulse Width	80			ns	
t_{DW}	Data Set Up Time	105			ns	Note 8
t_{DH}	Data Hold Time	10			ns	Note 8
t_W	Write Setup Time	80			ns	
	READ/WRITE CYCLE					
t_{RWC}	Read/Write Cycle	580			ns	Note 9
	CAPACITANCE					
C_{AD}	Address Capacitance		5	7	pF	V_{IN} = V_{SS}, V_{BB} = V_{SS} + 3
C_{PR}	Precharge Capacitance		17	20	pF	V_{IN} = V_{SS}, V_{BB} = V_{SS} + 3
C_{CE}	Chip Enable Capacitance		17	20	pF	V_{IN} = V_{SS}, V_{BB} = V_{SS} + 3
C_{RW}	Read/Write Capacitance		11	15	pF	V_{IN} = V_{SS}, V_{BB} = V_{SS} + 3
C_{IN1}	Data Input Capacitance		8	10	pF	CE = 0 V
C_{IN2}	Data Input Capacitance		4	5	pF	CE = V_{SS}
C_{OUT}	Data Output Capacitance		2	3	pF	V_{OUT} = 0 V

NOTES:

(1) V_{BB} supply should be applied at or before V_{SS}.
(2) A_0 through A_8 = 0, P = 0 V, T_A = 25°C, CE = V_{SS} for I_{DD1} and CE = 0 V for I_{DD2}.
(3) Total standby power for chip is: $(V_{SS} - V_{DD})\left(I_{DD4} + \frac{t_P}{t_{ref}} + I_{DD1} + \frac{t_C}{t_{ref}} + I_{DD3}\right)$
(4) This parameter is tested on a sample basis.
(5) I_{DD5} will be drawn only when both R/W and D1 are LOW.
(6) $I_{DDAVG} = \frac{t_P}{t_{cycle}} I_{DD1} + \frac{t_C}{t_{cycle}} I_{DD3} + \frac{t_{cycle} - t_C - t_P}{t_{cycle}} I_{DD4}$
(7) t_{CR} is referenced to the rising (positive-going) edge of CE or R/W, whichever occurs first (t_{CR} = t_C)
(8) t_{DW} and t_{DH} are referenced to the rising (positive-going) edge of CE or R/W, whichever occurs first.
(9) 580 ns read/write cycle time assumes a T_{DOW} of 45 ns. This is to allow for changing of data if data is ready. This cycle time can be shorter by 40 ns. If longer T_{DOW} is required, the cycle time will increase proportionately.

DC CHARACTERISTICS: V_{SS} = 16 V +5%, V_{BB} - V_{SS} = 3.5 V+0.5 V, V_{DD} = 0 V, T_A = 0°C to 70°C Note 1

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Leakage Current			1.0	µA	V_{IN} = 0 V
I_{LO}	Output Leakage Current			1.0	µA	V_{OUT} = 0 V
I_{BB}	V_{BB} Supply			100	µA	
I_{DD1}	Supply Current During Precharge		37	56	mA	Note 2
I_{DD2}	Supply Current During Overlap		38	59	mA	Note 2
I_{DD3}	Supply Current During Chip Enable		5.5	11	mA	P = V_{SS}, CE = 0V
I_{DD4}	Supply Current Between Chip Enable and Precharge (Standby Current) Note 3			100	µA	R/W = V_{SS}, P = V_{SS} CE = V_{SS},
I_{DD5}	Write Circuit Supply Current (Note 5)			4.0	mA	P = V_{SS}, CE = V_{SS} R/W = V_{DD}, DI = V_{DD}
$I_{DD}AVG$	Average Supply Current (Notes 4 & 6)		17	25	mA	Cycle Time = 580 ns t_P = 190 ns, T_A = 25°C
V_{IL1}	Input Voltage LOW (A_0 thru A_8 and D1)	V_{SS} - 17		V_{SS} - 14.2	Volts	T_A = 0°C
V_{IL2}	Input Voltage LOW (A_0 thru A_8 and D1)	V_{SS} - 17		V_{SS} - 14.5	Volts	T_A = 70°C
V_{IL3}	Input Voltage LOW (P, CE and R/W Inputs)	V_{SS} - 17		V_{SS} - 14.7	Volts	T_A = 0°C
V_{IL4}	Input Voltage LOW (P, CE and R/W Inputs)	V_{SS} - 17		V_{SS} - 15.0	Volts	T_A = 70°C
V_{IH1}	Input Voltage HIGH (All Inputs)	V_{SS} - 1.0		V_{SS} + 1.0	Volts	T_A = 0°C
V_{IH2}	Input Voltage HIGH (All Inputs)	V_{SS} - 0.7		V_{SS} + 1.0	Volts	T_A = 70°C
I_{OH1}	Output Current HIGH	0.6	0.9	4.0	mA	T_A = 25°C, R_L = 100Ω
I_{OH2}	Output Current HIGH	0.5	0.8	4.0	mA	T_A = 70°C, R = 100Ω
I_{OL}	Output Current LOW			10	µA	
V_{OH1}	Output Voltage HIGH	60	90	400	mV	T_A = 25°C, R_L = 100Ω
V_{OH2}	Output Voltage HIGH	50	80	400	mV	T_A = 70°C, R_L = 100Ω

II SYSTEM IMPLICATIONS OF THE 3534

INTRODUCTION

One of the most significant factors affecting access and cycle times at an 1103 type memory system level is the skew of the PCHG and CE controls due to the uncertainty in switching times associated with level shifting circuits. There is also skew associated with the timing and control circuitry that generates the discrete timing intervals necessary for device operation. From the system viewpoint, it is very desirable to minimize critical timing intervals and dependence on level shifter switching characteristics. The 3534 was designed to realize these objectives.

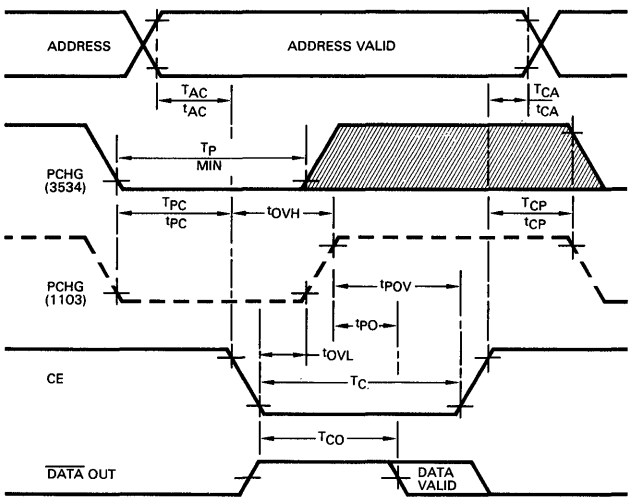
The 3534 4-transistor cell design and the absence of refresh amplifiers eliminate many 1103 timing constraints imposed on the system designer. Table 2.1 lists the improved ac and dc characteristics of the 3534 compared to the 1103. This section focuses on the memory system performance improvements and cost reductions that result when using the 3534.

Table 2.1 Improvements In The 3534 Relative To The 1103

CHARACTERISTIC		3534 MIN	3534 MAX	1103 MIN	1103 MAX
t_{OVL}	PCHG - CE Overlap, Low	Don't Care		25 ns	75 ns
t_{OVH}	PCHG - CE Overlap - High	Don't Care			140 ns
t_{POV}	PCHG to end of CE	t_C		165 ns	500 ns
t_C	CE Pulse Width	210 ns	850 ns	t_{POV}	
t_{PO}	End of PCHG to Data Out	t_{CO}			120 ns
t_{CO}	CE to Data Out		165 ns	t_{PO}	
t_{WC}	Write Cycle Time	480 ns		580 ns	
t_{PW}	PCHG to R/W Delay	Don't Care		165 ns	500 ns
t_{CW}	End of CE to End of R/W	Don't Care			10 ns
I_{DD4}	Standby Current		100 µA		4000 µA

SYSTEM ACCESS TIME

The timing diagram of Figure 2.1 compares 3534 and 1103 (broken line for PCHG) read cycles. The 1103 timing constraint requiring a PCHG and CE overlap has been eliminated in the 3534. The only relationship between PCHG and CE is that their leading (negative-going) edges must be separated by t_{PC} (125 ns). The overlap requirements (t_{OVL} min, t_{OVL} max and t_{OVH}) have been removed, allowing PCHG to return to the HIGH level any time after t_p min (170 ns). This implies that PCHG can remain LOW for extended periods allowing many accesses to the device in rapid succession. This mode of operation can be useful when transferring data blocks because successive access can be faster. Power dissipation will increase in this type of application, however.



NOTE: Broken Lines (. . .) And Lower Case t = 1103
Solid Lines (—) And Capital T = 3534

Fig. 2.1 3534 and 1103 Timing Comparison

The elimination of overlap constraints provides another important system benefit, illustrated by the relationship between the leading edge of CE and valid $\overline{\text{DATA}}$ OUT. Data is available T_{CO} (165 ns max) after CE on the 3534 and is not referenced to the trailing (positive-going) edge of PCHG as in the 1103. At the system level, this eliminates the clock skew associated with the rising edge of PCHG, providing faster access and cycle times in a worst case design.

Access time, referenced from the leading (negative-going) edge of PCHG for the two devices, is:

$$3534\ T_{ACC2} = T_{PC} + T_{cf} + T_{CO}$$

$$= 125 + 20 + 165$$

$$= 310 \text{ ns}$$

$$1103\ t_{ACC2} = t_{pc} + t_{cf} + t_{ovl}\ min + t_{pr} + t_{po}$$

$$= 125 + 20 + 25 + 20 + 120$$

$$= 310\ ns$$

Where T_{cf} = t_{cf} = CE fall time (10-90%)

t_{pr} = PCHG rise time (10-90%)

Access time (t_{ACC2}) of the 1103 is composed of five timing intervals. Three of these are very short and require precise control for maximum performance. Furthermore, the accurate control of these intervals is critical to the fundamental operation of the 1103. However, 3534 maximum performance depends only on controlling CE fall time and the fundamental operation of the 3534 is independent of PCHG and CE overlap requirements. The access times for both devices are equal at the chip level under test conditions. However, worst case performance in a 3534 system will be considerably improved over an equivalent 1103 system.

Figure 2.2 is a simple 3534 memory array illustrating level shifters, sense amplifiers, and the critical interface timing. Array access time depends only on the timing of one critical edge (t_1) relative to $\overline{PCHG}$ and one delay relative to $\overline{CE}$ (t_2); only two timing intervals affect system access times. The level shift circuits shown perform the NAND function.

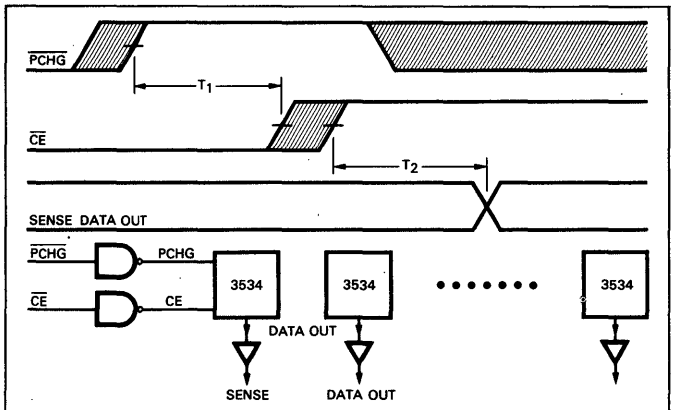
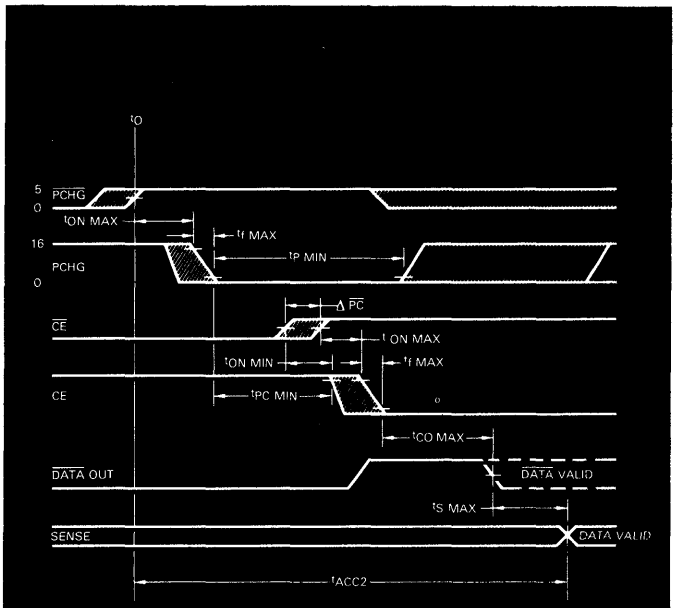


Fig. 2.2 Memory Array And Critical Interface Timing

System level skew considerations and the equation for t_{ACC2} associated with worst case access to this 3534 array are identified in Figure 2.3. The 3534 t_{ACC2} equation has been modified considerably to reflect uncertainties in timing intervals at the system level. This equation includes all factors affecting worst case access time. There are only two level shifter transitions in the critical path and both are negative-going. In most level shifter designs, negative-going transitions are inherently faster and more precise than positive-going transitions. Optimizing the level shifter design for t_{on} and t_f can therefore improve access times because all positive transitions before access have been eliminated.



$3534\ T_{ACC2} = t_{ON\ MAX} + t_{f\ MAX} + (t_{PC\ MIN} - t_{ON\ MIN}) + \Delta\overline{PC}$

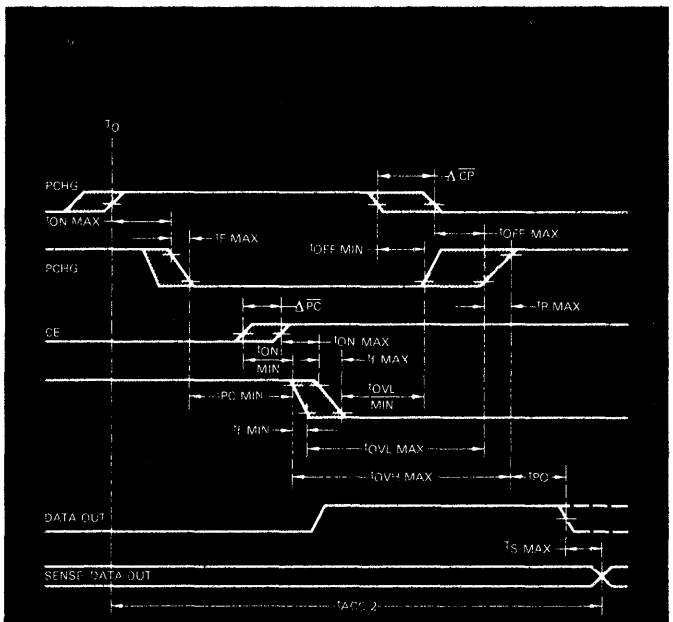
$+ t_{ON\ MAX} + t_{f\ MAX} + t_{CO\ MAX} + t_{S\ MAX}$

WHERE $\Delta\overline{PC}$ = $\overline{CE}$ SKEW RELATIVE TO $\overline{PCHG}$

$t_{S\ MAX}$ = SENSE AMP DELAY

$\Delta\overline{CP}$ = $\overline{PCHG}$ SKEW RELATIVE TO $\overline{CE}$

Fig. 2.3 Worst Case 3534 Access Waveforms



$1103\ T_{ACC2} = t_{ON\ MAX} + t_{f\ MAX} + (t_{PC\ MIN} - t_{ON\ MIN}) + \Delta\overline{PC} +$

$t_{ON\ MAX} + t_{f\ MAX} + t_{OVL\ MIN} + (\Delta\overline{CP} - t_{OFF\ MIN}) +$

$t_{OFF\ MAX} + t_{R\ MAX} + t_{PO} + T_{S\ MAX}$

AND: 1) $T_{OVL\ MAX} = (t_{ON\ MAX} + t_{f\ MAX}) - (t_{ON\ MIN} + t_{f\ MIN}) + t_{OVL\ MIN}$

$+ \Delta\overline{CP} + (t_{OFF\ MAX} - t_{OFF\ MIN}) \leq 75\ ns$

2) $T_{OVH\ MAX} = T_{OVL\ MAX} + t_{f\ MIN} + t_{R\ MAX} \leq 140\ ns$

Fig. 2.4 Worst Case 1103 Type Access Waveforms

The waveforms and equations associated with access to an 1103 memory array are detailed in Figure 2.4. Here also, the 1103 t_{ACC} equation has been modified to reflect system skew considerations. The equation illustrates that considerably more variables must be controlled to optimize access time and guarantee the basic operation of the 1103. The most difficult to control is t_{OVL}, which is very dependent on level shifter switching characteristics. The effects of level shifter switching characteristics are minimized in a 3534 system.

To quantitatively determine the improvement in access time possible with the 3534, the simplified timing generation scheme of Figure 2.5 will be used to compare 3534 and 1103 system access times. Each logic gate shown has a propagation delay of 5 ns min and 10 ns max. In reality, additional gates are required for decoding and controlling the delay line taps. These gates introduce more clock skew and make the 1103 overlap control even more difficult. In conventional 1103 systems, alternate design approaches such as local overlap control must then be used with a resulting increase in cost and component count.

To satisfy the overlap requirements of the 1103 for this example, level shifter characteristics shown in Table 2.2 are used. These switching times correspond to a relatively high performance level shifter and are not required for the basic operation of the 3534. Furthermore, these characteristics may be difficult to attain when driving a large number of devices in a system.

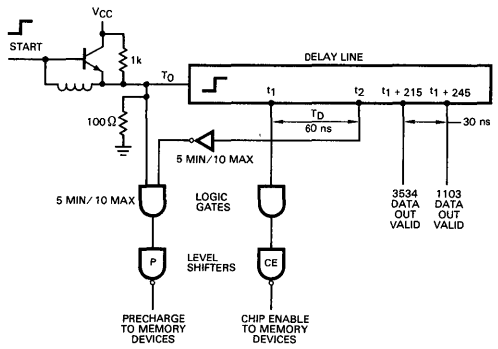


Fig. 2.5 Simplified Delay Line Timing Generator Illustrating Access Time Improvement With The 3534

	t_{ON}	t_F	t_{OFF}	t_R
MIN	5	10	5	10
MAX	15	25	15	30

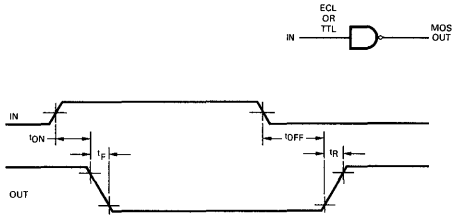


Table 2.2 Level Shifter Switching Characteristics

Assuming that the simplified timing and the level shifter characteristics are feasible, a comparison can be made between the 1103 and the 3534 operating in the same system. A memory cycle begins when a positive level is propagated down the delay line at t_0. At t_1, CHIP ENABLE time occurs and the CE level shifter output is guaranteed to be LOW after a delay. Therefore,

$$\overline{CE}\ \text{MAX} = t_1 + 10 + 15 + 25 = t_1 + 50$$

$$\overline{CE}\ \text{MIN} = t_1 + 5 + 5 + 10 = t_1 + 20$$

Data is available at the output of the 3534 no later than 165 ns after CE MAX. Therefore, with a 3534 inserted in the system,

$$\text{3534 DATA OUT} = (t_1 + 50) + 165 = t_1 + 215 \text{ ns}$$

With an 1103 inserted in the system, data is available 120 ns max after PRECHARGE returns to the HIGH level. To generate t_{OVL} min, the delay line is tapped at t_2. The earliest PRECHARGE can begin to go high is thus,

$$\text{PCHG}^+ \text{ MIN} = t_2 + 5 + 5 + 5 = t_1 + t_D + 15$$

Minimum overlap is then

$$\text{PCHG}^+ \text{ MIN} - \overline{CE}\ \text{MAX} = t_{OVL}\ \text{MIN}$$

To find the delay time, t_D, the specified minimum overlap time of 25 ns is assumed.

$$t_{OVL}\ \text{MIN} = 25 = (t_1 + t_D + 15) - (t_1 + 50)$$

$$25 = t_D - 35$$

$$t_D = 60 \text{ ns}$$

With a t_D of exactly 60 ns, the t_{OVL} max requirement (75 ns) can just be met. The latest that PRECHARGE can reach the HIGH level is derived by adding all worst case delays in the path. Therefore,

$$\text{PCHG}^+ \text{ MAX} = t_2 + 10 + 10 + 15 + 30$$

$$= (t_1 + t_D) + 65$$

$$= t_1 + 125 \text{ ns}$$

Data is then available at

$$\text{PCHG}^+ \text{ MAX} + 120 = t_1 + 245 \text{ ns}$$

$$\text{1103 DATA OUT} = t_1 + 245 \text{ ns}$$

The difference between access times (ΔA) with a 3534 or an 1103 in the system is then

$$\Delta A = t_{ACC}\,1103 - t_{ACC}\,3534 = (t_1 + 245) - (t_1 + 215)$$

$$\Delta A = 30 \text{ ns}$$

Therefore, for the simplified assumptions of this analysis, worst-case output data is available 30 ns earlier with the 3534. The system with a 3534 can then load the data out register 30 ns earlier, approximately a 10% improvement in access time. As system size and complexity increase, it becomes more difficult and expensive to guarantee the timing requirements of the 1103. However, 3534 timing requirements remain very straightforward. Depending upon the interface circuits and the resolution of the timing circuitry, a 30 to 70 ns improvement in worst case system access time is possible.

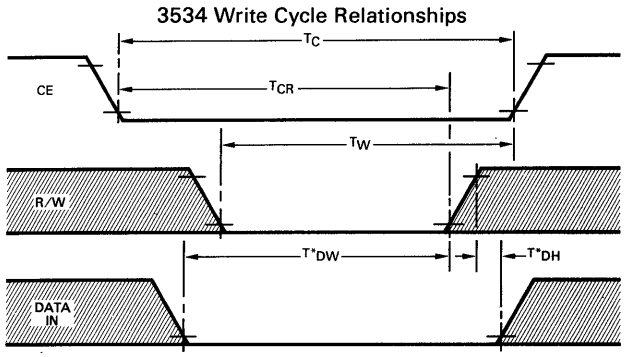
This example shows that the fundamental operation of the 1103 and the total array access time depend on the timing of two critical edges (CE and PCHG), three level shifter transitions, and constraints on t_{OVL} min, t_{OVL} max and t_{OVH} max. Because one of the critical level shifter transitions is positive-going (PCHG), level shifter designs must

be more symmetrical with respect to switching times. This can cause additional degredation of access time if t_{on} and t_f times are increased to satisfy the overlap constraints. Hence, level shifter switching characteristics and the ability of the system timing to generate very accurate intervals are critical to both optimum performance and basic operation of the 1103.

By contrast, the 3534 is independent of level shifter switching characteristics for fundamental operation. The control of only one clock edge relative to PCHG is necessary and there are no constraints on PCHG and CE overlap for optimum system access. When optimum access time is not critical, less costly and complex level shifters and timing circuitry can be used and the system still maintains the performance of more sophisticated 1103 type system designs. Another alternative with the 3534 is increased level shifter loading which reduces the number of support circuits required by the memory devices to achieve the same access time as an 1103 type system.

SYSTEM CYCLE TIMES

Improved system cycle times and increased data rates can of course result from improved access times. To further enhance memory systems, the 3534 decreases the write cycle times to 480 ns and eliminates the Read/Write pulse required with the 1103. Figure 2.6 illustrates the relationship of R/W to CE and PCHG for the 3534 and the 1103. With the 3534, the trailing edge of R/W is referenced to the leading edge of CE (t_{CR}) and the leading edge of R/W is referenced to the trailing edge of CE (t_W). This effectively removes R/W from the critical timing path since R/W may go LOW very early in the cycle. Thus, write and read cycles are only critically dependent upon t_{PC}, t_C and t_{CP} from a system point of view (Figure 2.7).



*T_{DH} and T_{DW} are referenced to the rising edge of R/W or CE, whichever occurs first.

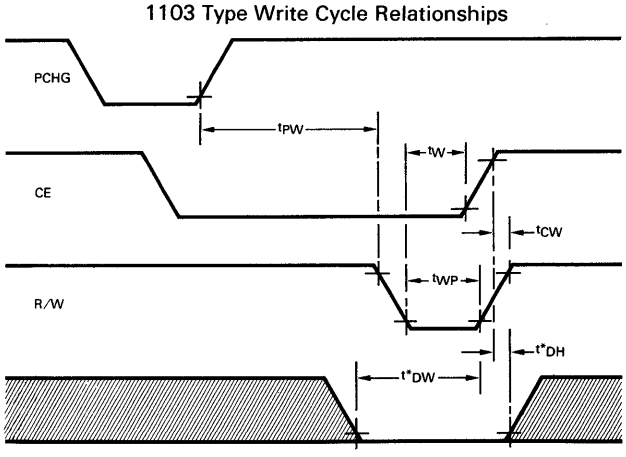


Fig. 2.6

With the 1103, the leading edge of R/W is referenced to the trailing edge of PCHG (t_{PW}). There is a minimum R/W pulse width (t_{WP}), and the leading edge of R/W is referenced to the trailing edge of CE (t_W). In addition, the rising edges of R/W on CE are critically related by t_{CW}. This requires the memory system to control three additional timing intervals for a write cycle. Furthermore, since the write cycle time (580 ns) is longer than the read cycle time (480 ns), the system timing generator must be able to generate two different timing sequences for read and write cycles if optimum read cycles are desired. Without two timing sequences, the read cycle time must be increased at the system level to allow both cycles to use the same timing chain.

The 3534, however, uses an identical critical timing chain for both cycles since the R/W level is not in the critical path. Therefore, read cycle time can be optimized at the system level without additional timing and control circuitry. This facilitates the design of a simplified, more efficient and less costly controller. Figure 2.7 compares the number of critical timing intervals required at the interface of a 3534 and an 1103 memory array. Obviously, the 3534 provides a simplified interface for application in any memory system.

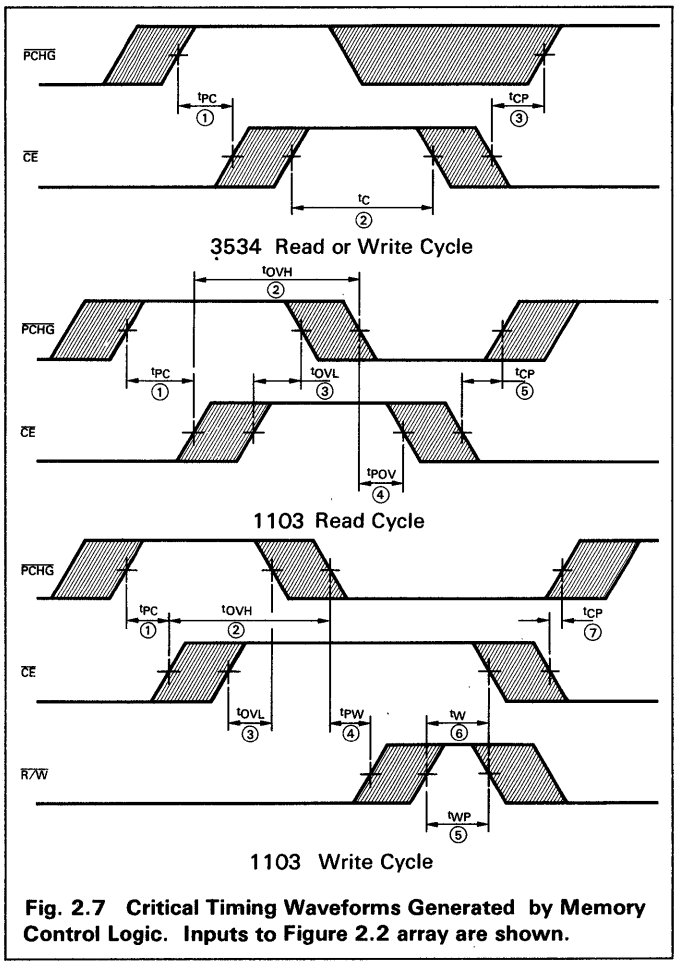


Fig. 2.7 Critical Timing Waveforms Generated by Memory Control Logic. Inputs to Figure 2.2 array are shown.

SYSTEM POWER

In addition to the performance improvements possible with the 3534, significant power savings can be realized since standby power is less than 2 mW. By constrast, 1103 standby power is a maximum of 65 mW. Consider a 16k x 36 memory system organized with 4k x 18 basic storage boards. During a memory cycle, assume that only two of the eight storage boards are selected and that only 18 memory devices per board dissipate maximum power since PCHG, CE and R/W

are decoded. In this situation, 540 of the 576 memory devices are always in the standby mode.

The worst case power dissipated by the memory devices in a 3534 system is approximately 15.48 watts.

$$P_{3534} = (36)(.4W) + (540)(.002W)$$

$$= 14.4W + 1.08W = 15.48W$$

With 1103 type devices, worst case power dissipation is approximately 49.5 watts.

$$P_{1103} = (36)(.4W) + (540)(.065)$$

$$= 14.4W + 35.1W = 49.5W$$

This clearly illustrates that the 1103 memory devices have a worst case power dissipation more than three times greater than an equivalent number of 3534s for the system described. The system implications of this power differential are obvious. They include lower cost power supplies, lower system operating temperatures, higher reliability and minimum cooling requirements. Many systems can realize a significant reduction in power dissipation by simply replacing 1103s with 3534s.

CONCLUSIONS

Depending upon the application, the 3534 can improve system performance or reduce costs relative to an equivalent 1103 system. These improvements are applicable in existing 1103 systems with or without modifications as well as new system designs using the 3534.

Existing 1103 Type Systems

When replacing 1103s in existing systems with 3534s, two distinct improvements arise. First, a large safety margin is introduced in the system timing since the critical t_{OV} and t_{CW} requirements are eliminated. Deviations in t_{OV} and t_{CW} timing tolerances with component age and varying ambient conditions that might adversely affect 1103 operation will not affect the 3534. Second, power in larger systems is appreciably reduced due to the low standby current of the 3534. The system can operate at lower temperatures leading to enhanced reliability.

Upgrading Existing 1103 Type Systems

Existing systems can be modified to either improve performance or decrease costs. For improved performance, the timing can be adjusted in several ways. The easiest modification is to adjust the output register strobe to occur earlier in the cycle. The worst case access time improvement obtained is dependent upon the existing level shifters but should be approximately 30 to 70 ns in a standard system. More extensive changes in the timing section can result in reduced read and write cycle times. By optimizing level shifters for t_{on} and t_f, access time can be further improved.

To maintain existing performance and reduce system costs, several approaches are possible. Lower performance level shifters can be used with existing timing to reduce components and costs. Alternately, a slightly redesigned storage board might reduce the number of level shifters used to drive the 3534/1103 array. If the existing level shifters are maintained, the output sensing circuits can be simplified and/or their noise immunity can be increased. This is because worst case data will be valid earlier with a 3534 and the additional time can be used to allow the output "0" current to decay well beyond the 400 μA level used as a reference point. Timing and control boards can also be modified to eliminate the logic associated with overlap control and the R/W pulse to reduce costs. Lower power operation and increased safety margins are again applicable. Also, 1103 systems with local t_{OV} control can eliminate that circuitry.

New System Designs

New designs can fully exploit the cost/performance advantages available with the 3534. Performance oriented systems can optimize level shifter designs for t_{on} and t_f and minimize storage board access. At the system level, only two timing intervals are of concern when optimizing access time, minimizing the timing and control requirements and expense. To guarantee system access, refresh cycles may be abandoned at any time without altering the stored data (Section IV). Maximum data rates are also obtained as a result of the equal read and write cycle times, and only one timing chain is required.

For applications where optimum performance is not necessary, a number of techniques can be used to minimize costs. First, since the basic operation of the 3534 is independent of level shifter switching times, any circuit which satisfies the performance goals of the system can be used. By contrast, the 1103 timing constraints necessitate high performance level shifters even in systems operating with longer access and cycle times. In addition, each level shifter may be used to drive more 3534s since the t_{OV} and R/W pulse constraints are eliminated. As in the performance oriented design, timing and control requirements are minimal and a low or medium speed logic family can be used depending on the system requirements. Since power dissipation is lower than in an equivalent 1103 systems, power supply and cooling costs can be minimized.

1103 Compatibility

In realizing these improvements, 1103 compatibility can be maintained at any of three levels. First, of course, is the chip level where the 3534 can be inserted in place of the 1103 with a resulting improvement in timing tolerances and power dissipation. At the next level, the storage board can be modified by reducing the number or complexity of the interface circuits, and the 3534 can be used to considerable advantage to reduce storage board costs or improve performance. In this second case, 1103 compatibility is maintained at the storage board interface and either the 1103 board or the 3534 board can operate in the system. In this way, many of the advantages of the 3534 can be utilized without sacrificing compatibility.

At the third level of compatibility, the memory system interface remains intact and the internal timing and control is vastly simplified to optimize the system for the 3534. With careful partitioning, only the timing and the storage board need be modified to greatly reduce system costs and/or increase performance. Conversion to an 1103 system can then be realized simply by interchanging the timing boards since the back-plane is identical in either system. The additional boards, containing perhaps the input and output data registers, address register and additional common logic remain identical for both systems. In this case, maximum benefit can be derived from the 3534 while maintaining a viable 1103 system.

III BASIC STORAGE BOARD DESIGN

INTRODUCTION

Defining the design and organization of the basic 3534/1103 storage board may be very straight forward or may constitute the focal point for all system design tradeoffs. In smaller systems, memory timing and control logic can usually be placed on a PC board with the 3534/1103s, simplifying the design. As memory size increases, the system must be partitioned into a number of PC boards, each PC board type performing a specific function. Packaging constraints and expansion requirements become increasingly important and can have a considerable effect on the design and organization of the memory board and the timing control boards. The system then evolves around the fundamental memory unit, the basic 3534/1103 storage board.

Many factors influence the organization and design of the basic storage board and include:

- Capacitive drive ability of level shift circuits
- The number of sense circuits required
- Power dissipation limits
- PC board size
- Number of PC boards and connectors required for a given size memory
- Complexity of back-plane wiring and power distribution network
- TTL or ECL compatiblity
- System error correction capabilities

The significance assigned to these factors influences the cost and performance of the resulting memory system. In addition, to these considerations, it is very important to maximize the ratio of MOS to bipolar circuits on the storage board. This is true because the peripheral circuitry is less costly per bit when it is amortized over many 3534/1103s. To minimize costs, the storage board should contain the largest number of 3534s capable of interfacing with one set of support circuits. The performance improvements and cost reductions made possible by the 3534 and the details of a storage board design are examined here.

TYPICAL MEMORY ARRAY

A memory organization typical of a small system which can easily be expanded for larger memory applications is used to illustrate the advantages of using the 3534 in a memory array. Since PC board sizes vary considerably, it is assumed that sufficient area is available for the 3534 array, level shifters and sense amplifiers. In addition, it is assumed that the storage board is required to have a TTL interface.

Figure 3.1 is a logic diagram of a 4 k x 9, TTL compatible storage board complete with level shifters and sense amplifiers. The 3534s are arranged in a 4-row by 9-column matrix, providing a 4096 x 9 bit memory array. The DATA IN and DATA OUT leads of the devices in each column are respectively wired-OR to form one of the nine bits of the array. CHIP ENABLE inputs C_1 through C_4 are externally decoded and permit the selection of one of the four memory rows. Address lines A_0 through A_9 are distributed to all 36 memory devices during a cycle. The Read/Write signal is distributed to rows 1 and 2 or to rows 3 and 4 during a write cycle, reducing the number of level shifters required.

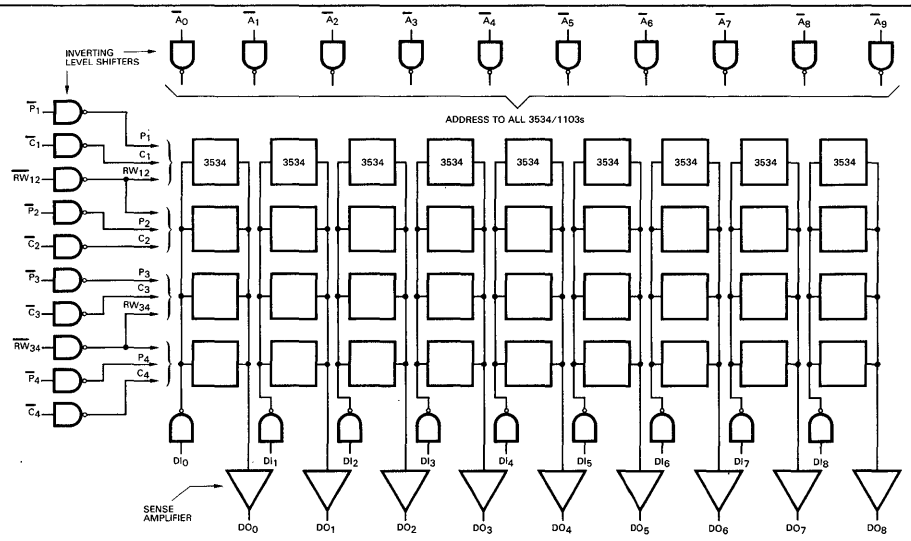
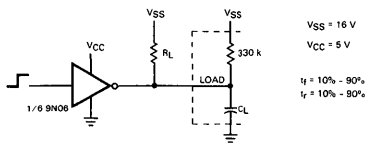


Fig. 3.1 Fully Bufferred 4 k x 9 Basic Storage Board

To reduce power dissipation on the board, PRECHARGE is decoded and inputs P_1 and P_4 select the memory row to be precharged. This allows a memory design in which only the accessed devices dissipate power during a cycle. For a refresh cycle, the storage board is refreshed by enabling all of the PRECHARGE and CHIP ENABLE inputs, simultaneously refreshing all four rows.

LEVEL SHIFTERS

Because the 3534 interface requirements are simplifed, the basic operation of a 3534/1103 storage board does not depend on level shifter switching characteristics. The design considerations are the cost/performance tradeoffs available since even simple and inexpensive level shifter designs permit the 3534 to operate properly at increased cycle times. This is quite different from the level shifter constraints in 1103 type systems where even low cost/low performance systems must use more expensive and sophisticated techniques to guarantee the precharge-chip enable overlap requirement. Figures 3.2, 3.3, and 3.4 illustrate level shifter configurations capable of driving the capacitive loads of the 4 k x 9 array. Each figure includes typical switching data at 25°C.



TYPICAL CHARACTERISTICS AT 25°C

		TYPICAL TIMES IN ns				TYPICAL		WORST CASE SUPPLY LIMITS	
R_L	C_L	t_f	t_{d+f}	t_r	t_{d+r}	V_{OL}	V_{OH}	P_{ON}	P_{OFF}
470 Ω	26 pF	19	31	34	48	.5 V	≈ 16 V	650 mW max	35 mW max
	48 pF	24	36	60	74				
	93 pF	34	49	102	120				
	215 pF	58	80	200	240				
1 kΩ	26 pF	16	26	78	95	25 V	≈ 16 V	320 mW max	35 mW max
	48 pF	20	32	115	133				
	93 pF	29	43	210	230				
	215 pF	52	72	500	535				

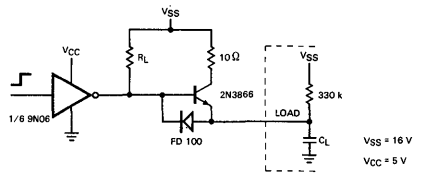
Fig. 3.2 Resistive Pull-Up Level Shifter

Figure 3.2 illustrates a simple, inexpensive level shifter circuit using the 9N06 high voltage hex inverter and a pull up resistor (R_L). Typical switching characteristics at R_L = 470 and R_L = 1 k clearly show the asymmetry of t_r and t_f. This circuit can be used to drive all inputs of a 3534 array with only moderate degradation of system access time since only negative going transitions (t_f) are in the critical path. The memory cycle time however, is increased to near 1.5 us, but this may be acceptable in many applications.

In an equivalent 1103 type system, this circuit could not be used for PCHG, CE or R/W because the long rise and fall times do not permit adequate control of t_{OV} and t_{CW}. Since the 3534 R/W signal is a level (not a pulse), this circuit can also be used as a R/W driver with only moderate degradation of cycle time. Thus, a designer using the 3534 has this level shifter available for all signals, not just for data as with the 1103.

The power dissipation and rise and fall times of this circuit depend upon the value of R_L. Decreasing R_L to a minimum value near 400 Ω improves t_r and t_f but increases power dissipation. The designer should carefully analyze the power/performance/cost trade offs when using this or any level shifter circuit to optimize his system for access and cycle time.

For higher performance applications, the level shifters shown in Figures 3.3 and 3.4 can be used. The circuit of Figure 3.3 uses active pull up to greatly increase drive capability and thus improve rise times. Fall times increase and rise times decrease as R_L is lowered toward 1 kΩ. The diode provides a low impedance path to ground (through the 9N06) when the capactive load is discharged. The dc power dissipation is again dependent on R_L.



TYPICAL CHARACTERISTICS AT 25°C

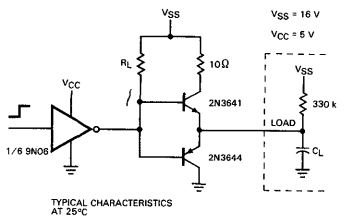
		TYPICAL TIMES IN ns				TYPICAL		WORST CASE SUPPLY LIMITS	
R_L	C_L	t_f	t_{d+f}	t_r	t_{d+r}	V_{OL}	V_{OH}	P_{ON}	P_{OFF}
2 kΩ	STRAY	12	19	32	45	7 V	15.6 V	170 mW max	35 mW max
	100 pF	28	41	35	50				
	200 pF	46	61	41	60				
	300 pF	57	75	46	64				
1 kΩ	STRAY	13	20	27	43	.7 V	15.6 V	320 mW max	35 mW max
	100 pF	32	45	29	46				
	200 pF	50	68	30	48				
	300 pF	62	81	33	51				

Fig. 3.3 Active Pull-Up Level Shifter

One consideration when using this circuit concerns the low level output voltage, V_{OL}. The 3534/1103 specifies the low level input voltage for PCHG, CE and R/W at V_{SS} - 15V at 70°C. Thus, the supply voltage tolerances must be such that at the lowest V_{SS}, it is still possible to maintain the required logic level for optimum performance. The drop across the diode (FD100) is approximately .45 V at the input load current levels provided by the 3534 because the diode is operating near the knee of its V-I characteristic. Hence, the low output level is about .85 V. The V_{SS} supply can range between 15.85 and 16.8 volts and still satisfy the logic level requirements for PCHG, CE and R/W at higher (70°C) temperatures. When maximum performance is not critical, the input logic levels can be relaxed with resulting increases in access and cycle times, (40 ns). The input level requirements should be analyzed for each application with regard to operating temperature ranges, power supply tolerances and performance requirements.

The circuit of Figure 3.4 employs a complimentary pair with a 9N06 to improve capacitive drive capability while minimizing power dissipation. The fast turn on and fall times are particularly suited to a performance oriented 3534 system. The low voltage offset condition discussed previously is also applicable to this circuit since the V_{BE} of the 2N3644 ranges between .65 and .7 V. The V_{OL} value can approach 1.1 V for a worst case output level from the 9N06. Again, it is possible to compensate for this effect by restricting the supply voltage tolerances and/or the operating temperature ranges of the system.

With each of these level shifter circuits, a clamp diode from the output to V_{SS} might be necessary. This prevents the V_{OH} level from exceeding specified limits during transitions of neighboring level shifters due to capacitive coupling. A ground plane or careful layout of signal and ground lines may eliminate this diode clamp requirement. Specifically, level shifter outputs driving heavy loads with fast transition times should not be run adjacent to another similar level shifter output for more than a few inches.



TYPICAL CHARACTERISTICS AT 25°C

TYPICAL CHARACTERISTICS
AT 25°C

		TYPICAL TIMES IN ns				TYPICAL	
R_L	C_L	t_f	t_{d+f}	t_r	t_{d+r}	V_{OL}	V_{OH}
470 Ω	STRAY	12	25	16	32	9 V	15.6 V
	100 pF	13	26	16	33		
	200 pF	13	28	19	37		
	300 pF	14	29	21	40		
1 kΩ	STRAY	11	24	32	55	8 V	15.6 V
	100 pF	11	25	33	57		
	200 pF	13	28	35	58		
	300 pF	14	28	37	60		

Fig. 3.4 Level Shifter with Booster Stage

The mutual inductance associated with the PC tracks may cause ringing on the level shifter outputs due to the high peak currents. Typical inductance ranges from 10 to 20 nH/inch with 15 mil tracks. Therefore, current limiting resistors in the level shifter output stage or external series damping resistors may be required. Short line lengths and careful layout practices should minimize this effect.

LEVEL SHIFTER POWER DISSIPATION

There are two elements of total level shifter power dissipation to consider when analyzing storage board power. The first is the static or dc power associated with the level shifter circuit and the second is the transient or ac dissipation associated with charging and discharging the capacitive load. Hence,

$$P_{TOTAL} = P_{dc} + P_{ac}$$

P_{dc} is determined by the maximum current drain in the level shifter corresponding to each output state. If a level shifter operates at a 40% duty cycle (output low 40% of the time) the dc power will be

$$P_{dc} = (.4)\,(P_{OL}) + (1-.4)\,(P_{OH})$$

where P_{OL} is the maximum dc power with the output LOW and P_{OH} is the maximum dc power with the output HIGH. Since the power dissipated by the level shifters and sensing circuits on a storage board may exceed the dissipation of the 3534/1103s, it is very desirable to have one output state of these circuits associated with low power dissipation. This is particularly important in a larger system where most of the devices are in a standby mode during a memory cycle. By making the HIGH output state correspond to low power, system power requirements can be minimized in most applications.

The transient or ac portion of total power dissipation results because the level shifter must source and sink current during the charging and discharging of a capacitive load. Power is dissipated by the level shifter when charging the load since charge flows into the load capacitor from the power supply for a short period of time, thus transferring energy to the capacitor. Similarly, when a capacitor is discharged (negative-going edge), charge flows from the capacitor into the level shifter pull down transistor and power is dissipated. The total dissipation associated with this energy transfer is given by

$$P_{ac} = \frac{CV^2}{T}$$

Where P = power in mW

Where P = power in mW

C = load capacitance in pF

V = supply voltage in volts

T = cycle time in ns

As a typical example, when C = 200 pF, V = 16.8 V and T = 600 ns, the power dissipation associated with both transitions (positive and negative) is 94 mW.

DRIVING THE 3534/1103

The drive requirements of a level shifter in an array depend upon the number of devices driven and the capacitive load per device. Each 3534/1103 input should be analyzed to determine the best type of circuit for the particular function. The capacitance at each input is listed in Table 1.1.

Address

For the 4 k x 9 storage board, 36 devices must be driven by each address level shifter. Each level shifter must drive 252 pF (36 x 7 pF) plus stray capacitance associated with the level shifter circuit and the printed circuit board track. Level shifter output capacitance may range from 1 to 5 pF depending on the type of circuit. PC track capacitance usually ranges from .5 to 1.5 pF per inch with a track width of 10 to 15 mils. Since the address lines must interconnect all of the 3534s, the worst case line length will range between 20 and 35 inches depending upon the density of the array packaging. A more realistic estimate of the worst case address driver load capacitance is 275 to 300 pF. Since the effect of track capacitance and inductance can be considerable, line lengths should be kept to a minimum in the layout of the storage board.

The power dissipation associated with one address level shifter transition (C_L = 275 pF, V = 16.8 V, T = 600 ns) is approximately 64 mW. By allowing the address lines to change only once each cycle, the transient power can be reduced to a worst case of 10 x 64 mW or 640 mW. If an inexpensive level shifter with a long rise time is used (Figure 3.2), it may be necessary to return all ADDRESS inputs to the HIGH level at the end of each cycle to achieve faster access times. Faster circuits allow the designer to minimize transient power by permitting only one transition per cycle, but this can be offset by increased dc power dissipation and level shifter cost.

Precharge, Chip Enable, Read/Write

Since the positive-going edge of PCHG is not associated with any critical timing, the level shifter for a performance oriented 3534 memory only needs a fast fall time. The capacitive load seen by PCHG and CE (ceramic package) is 9 x 20 pF = 180 pF. With compensation for PC track, etc., the load capacitance is approximately 190 pF. With this load, the driver circuits suggested allow fall times in the 15 to 50 ns range to satisfy most cost/performance requirements. Since cycle time is affected by the rise time of CE, applications requiring minimum cycle times (550-650 ns) must use level shifters with both fast rise and fall times for CE. As previously noted, the R/W signal is independent of rise and fall times. If desired, one level shifter can drive the entire array even on high performance system. In this case, the R/W capacitance is approximately 575 pF which can be adequately driven by the level shifters in Figures 3.3 and 3.4.

Data In

The capacitive load of the DATA IN lines is very low (3 x 5 pF + 1 x 10 pF = 25 pF) and including stray effects, total capacitance should not exceed 30 pF. The level shifter of Figure 3.2 is more than adequate to drive this load. Power dissipation can be minimized by keeping the data level shifters off except during the Write cycle.

SENSING OUTPUT DATA

The 3534/1103 provides an output current level to indicate the logic state of the addressed memory cell. When CE goes LOW, a current appears on the output line ranging between 500 µA minimum and 4 mA maximum. This range defines a logic "1" output and corresponds to LOW level data written into the selected cell during a write cycle. If a HIGH level had been written into the cell (near V_{SS} on the DATA IN line) the current decays to 10 µA or less, representing a logic "0". Since a HIGH level written in results in a LOW level out (no current), the nomenclature $\overline{\text{DATA}}$ OUT is used.

The access time for the 3534/1103 is referenced to the 400 µA level on the DATA OUT line. The voltage developed across a sense resistor is, of course, proportional to the resistor value since the output current is essentially constant. Higher load resistor values result in higher voltages and longer time constants. For maximum system performance, it is desirable to sense the output current at low voltage levels.

In a performance oriented system, a comparator (µA710) or a line receiver (75107, 75108) can be used to sense the output differential as shown in Figure 3.5. Lower load resistor values are possible with the µA710 because of its low bias current requirements and guaranteed differential voltage tolerance of 6.5 mV. The 75108, however, has an open collector output, making it desirable in applications using an output or input/output data buss. Additional circuits that can be used include the 7524 and 7525 dual sense amplifiers.

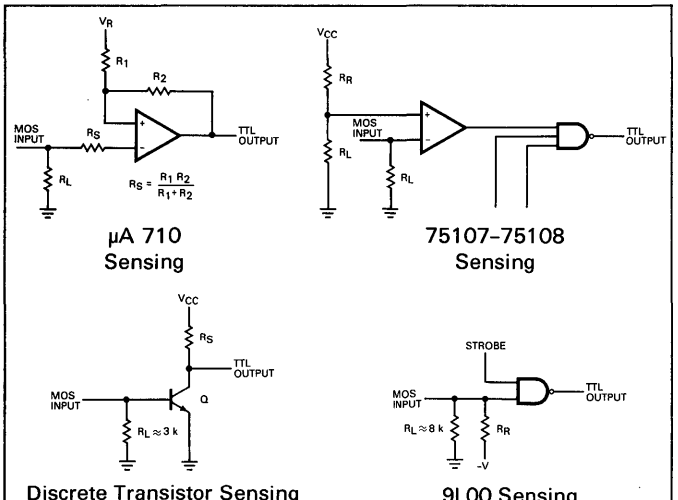


Fig. 3.5 3534/1103 Sense Amplifier Circuits

A discrete transistor may be used for applications where increased access time is acceptable. Because the time required for the transistor to turn off (output current decaying) depends upon the time constant of the $\overline{\text{DATA}}$ OUT line, the load resistor should be kept as small as possible. Although this approach results in longer access times, a negative power supply is not required as with the µA710 and the 75108. A low power TTL gate (9L00) can also be used as a sense amplifier but access time will be increased.

When "wire-ORing" a number of 3534/1103s to the same sense amplifier input, care should be taken to analyze worst case input currents occurring during refresh cycles. For a 4 k x 9 organization, each 3534/1103 may contribute a maximum of 4 mA to the total worst case input current of 16 mA. Under these conditions, the sense resistor must not allow the input voltage to exceed device limits. In designs where many DATA outputs are "OR'd" together, part of the memory may be refreshed during any refresh cycle to eliminate this problem. This approach will increase the number of refresh cycles required by the system.

DECOUPLING CAPACITORS AND PC BOARD LAYOUT

Because of the current surges associated with the charging and discharging of the memory array during operation, consideration must be given to power supply decoupling and ground line impedance. To provide this energy, V_{SS} and V_{BB} should be adequately by-passed as near as possible to the memory devices. At least 50,000 pF (.05 µF) should be placed between V_{SS} and V_{DD} for each 3534 in the form of a high frequency, low inductance ceramic capacitor. Level shifter circuits, particularly those driving heavy loads should be similarly by-passed. The V_{BB} supply should be by-passed to both V_{SS} and V_{DD} and approximately 20,000 pF (.02 µF) per device should be provided. The V_{CC} supply should also be decoupled according to the number of TTL packages (.1 µF for every 3 or 4 packages) and their placement on the board.

To reduce the number of capacitors in a large array, several 3534s may be serviced by a larger (.1 µF or .2 µF) capacitor. However, no device should be more than one or two inches from the decoupling capacitor. In addition to this local decoupling, each power supply should be by-passed as it enters the storage board. Electrolytic (solid tantalum) capacitors ranging in value between 20 µF and 40 µF should be adequate for a 4 k x 9 storage board.

To minimize system noise generation and to provide very low ground impedances, ground planes have proven very effective. For memory designs employing double-sided boards there are a number of layout guidelines that should be followed to minimize potential problems. To begin, an effective ground plane can be formed by interconnecting ground lines to form a grid like network. Grid spacings on the order of one to two inches should be satisfactory. In addition, ground tracks should be made as wide as possible and should be expanded to fill available area on the PC board. To facilitate voltage distribution and minimize noise, a similar approach should be taken for the V_{SS}, V_{BB}, and V_{CC} lines. By distributing the decoupling capacitors throughout the array, the voltage grids are more easily formed.

The physical placement of all memory, level shifting, and sensing circuits should be carefully considered. The 3534 array should be as dense as possible to minimize line lengths. Level shifter outputs and sense amplifier inputs should be on opposite sides of the card and these circuits should be as close to the array as feasible. A dummy line may be incorporated with the sense amplifiers (µA710 or 75108) to improve noise immunity. The TTL or ECL inputs to the board should be contained as near as possible to the connector. This reduces capacitance on these lines and can improve system performance. Although particular PC board sizes may require some compromises of the above guidelines, general adherance will result in satisfactory storage board operation.

IV SYSTEM LOGIC DESIGN

INTRODUCTION

When designing a 3534/1103 memory system, it is necessary to define a basic, repeatable memory module which is self contained and capable of refreshing itself. For smaller systems, this module may comprise one or two PC boards. In larger systems the basic memory module may be quite large.

A number of factors influence the memory module design, including

- Memory expansion requirements
- PC board size
- Minimizing PC board types
- Density requirements
- Number of interconnections required
- Power supply requirements and regulation
- Cooling requirements and local heating
- Cost and performance

Even though the priorities assigned to these factors greatly affect the final module definition, certain functions are almost always performed by the module's timing and control logic. This section identifies those basic functions and indicates typical circuitry that can be used by the designer. In addition, the reduction of components that results when using the 3534 is illustrated.

CONTROL LOGIC BLOCK DIAGRAM

The diagram of Figure 4.1 identifies the functional blocks generally required for the timing and control circuitry of a 3534/1103 memory system. Specific memory applications may take advantage of available registers and clocks to reduce or eliminate certain functional blocks (Address Register, Data Register, Refresh Clock). However, the functions shown usually must exist somewhere in the overall system. The basic storage board (4 k x 9) described previously is assumed to be the fundamental memory unit of the system. Certainly, other storage board organizations will allow flexibility and expansion in the word and bit dimensions and the block diagram can be modified accordingly.

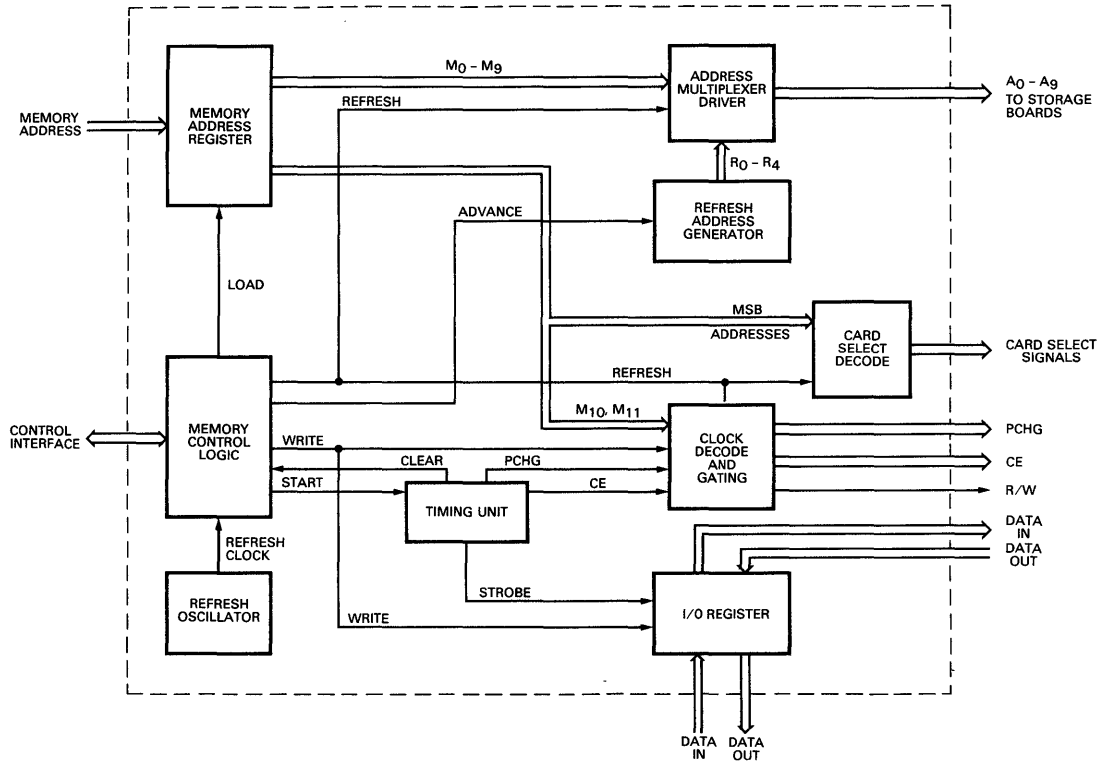


Fig. 4.1 Memory Control Logic Block Diagram

When implementing the timing and control logic for a 3534 dynamic memory system, the designer may emphasize either cost or performance. The effect of this emphasis is more important in smaller memory systems since the cost of this overhead logic must be considered relative to the number of memory devices. In larger systems, the cost of the memory devices usually predominates since the timing and control circuitry represents only a small portion of the total system cost. Therefore, the size of the memory system and its performance goals should be carefully evaluated when selecting a logic family and timing techniques. Logic families presently offering a large number of SSI and MSI devices include 9000 series TTL, 9300 series TTL, 9S00 series Schottky TTL and 9500 series ECL.

REFRESH REQUIREMENTS AND CIRCUITRY

Independent of the logic family and timing techniques chosen for the memory system, the refresh requirements for each 3534/1103 must be satisfied. Refreshing requires that at least 32 read cycles are performed in a 2 ms period corresponding to the 32 combinations of address bits A_0 through A_4. During the execution of these cycles, Address bits A_5 through A_9 may assume either state, but they must be stable. Forcing them to a HIGH level (corresponding to low level shifter power) usually permits lower power operation at the system level.

In some applications, it may be possible to guarantee the refresh requirements during normal operation without additional circuitry. This can be true of 3534/1103s used to maintain CRT displays or in other applications where a minimum number of accesses can be guaranteed to refresh the memory. In general, however, the memory control logic must provide the refresh addresses and the appropriate refresh intervals.

There are two basic approaches that can guarantee at least 32 refresh cycles every 2 ms. The first is to execute 32 consecutive refresh cycles at the start of every 2 ms interval. The second approach is to evenly distribute the 32 refresh cycles throughout the 2 ms period. These approaches assume, of course, that all of the memory devices in the system are refreshed simultaneously.

There are several reasons why it is usually more desirable to distribute refresh cycles. By distributing the cycles at approximately 60 µs intervals, the response to an external memory request is delayed at most by one refresh cycle. Furthermore, the probability of conflicting refresh and memory requests is minimized and the effective memory availability is thus greater.

Another consideration concerns the ability of the power supplies to respond to the current surges resulting from consecutively accessing all memory devices. Local energy storage (electrolytic capacitors) on each storage board must then be sufficient to maintain regualtion until the power supplies can respond. Depending upon the supplies, the power distribution network, and the memory size, each storage board may have to maintain regulation from 10 to 50 µs. Distributing the refresh cycles can thus reduce the amount of local energy storage required.

Typical examples of the circuitry required to satisfy the refresh requirements of the 3534/1103 are described below.

Refresh Oscillator

To generate refresh requests at the selected interval, the circuit in Figure 4.2 can be used. The 9601 monostable multivibrator (one-shot) shown has been connected as a free running oscillator which provides a clock pulse approximately every 60 µs. If a system clock is available, a counter or shift register can be used to generate refresh requests at the appropriate interval.

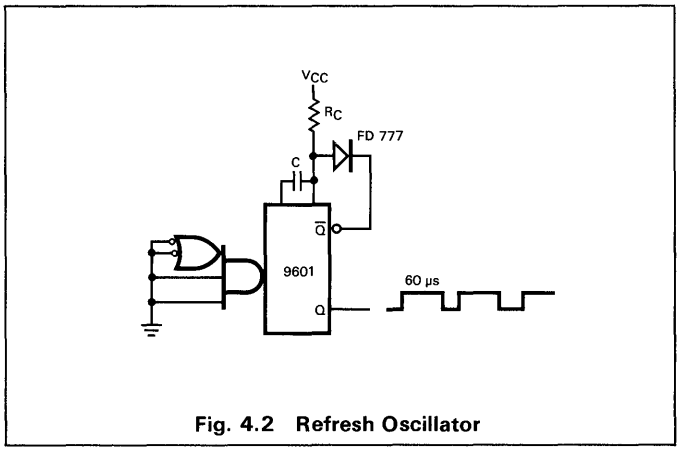


Fig. 4.2 Refresh Oscillator

Refresh Address Generator

The refresh address generator can be configured as a 5-bit ripple counter as shown in Figure 4.3. The counter is advanced after the completion of a refresh cycle and high speed operation is, therefore, not necessary when executing refresh cycles at 60 µs intervals. For applications where consecutive refresh cycles are executed, higher frequency counters can be used to reduce refresh address delays.

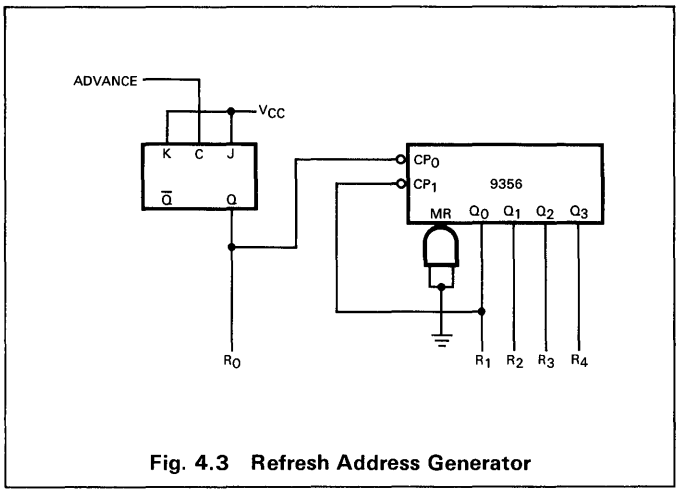


Fig. 4.3 Refresh Address Generator

Address Multiplexer

Figure 4.4 illustrates two multiplexers capable of selecting either the normal memory address or the refresh address. For cost oriented applications or in systems where the memory address is available prior to a memory request, the multiplexer using the 9322 may be used to minimize components and cost. For performance oriented systems, high speed logic (9500 series ECL or 9S00 series TTL) may be used to maximize system performance.

As memory size increases, these multiplexers may no longer be adequate to drive the load on each address line. This load depends upon the input current requirements and input capacitance of the address level shifters. For example, an 8 k x 36 system using 4 k x 9 storage boards presents 8 current loads to the multiplexer outputs and 40 to 70 pF. To optimize performance, it may be necessary to add buffer gates (9009) or replace the 9S00 output gates with 9S40 or 9S140 line drivers.

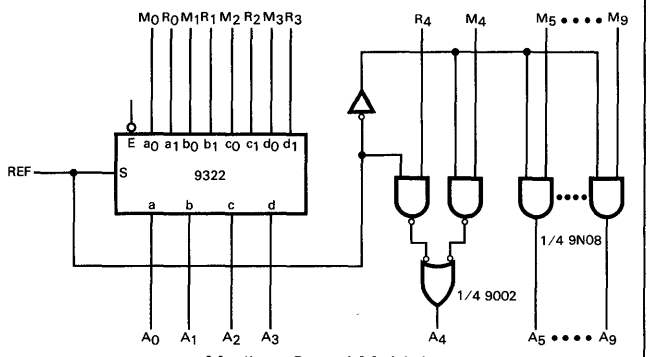


Fig. 4.4 Address Multiplexers

During memory operation, particularly in high speed systems, multiple transitions or "glitches" on the multiplexer outputs should be prevented. Addresses should be changed only once during each cycle to minimize transient dissipation in the address level shifters and prevent device limits from being exceeded. This is accomplished in the circuits shown by enabling the memory address from the address register except during refresh. Multiple transitions preceding a refresh cycle are allowable since they can only occur every 60 μs.

Since Addresses A_5 through A_9 are not needed during refresh, (they must be stable) they need not be multiplexed. These addresses can remain at the last memory address or can be locked out during a refresh cycle. If the address register can change during a refresh cycle (memory cycle requested), A_5 through A_9 must be locked out as shown.

MEMORY CYCLE CONTROL

The memory Cycle Control logic is responsible for the logical interface between the 3534/1103 system and the memory controller. This logic must also resolve any conflict between refresh and memory requests, clock the address register, control the multiplexer and refresh address generator, and indicate to the timing unit when a cycle should be started. In addition, the type of cycle requested (read, write, or read/modify/write) is determined and the data-in register (if included) is loaded.

The diagram of Figure 4.5 illustrates a logic design which can perform the above functions. Since specific interface requirements may vary considerably, Figure 4.5 depicts only one possible implementation of an asynchronous cycle control logic design. The logic requires only a MEMORY REQUEST pulse, a read or write indication, addresses, and data for basic operation.

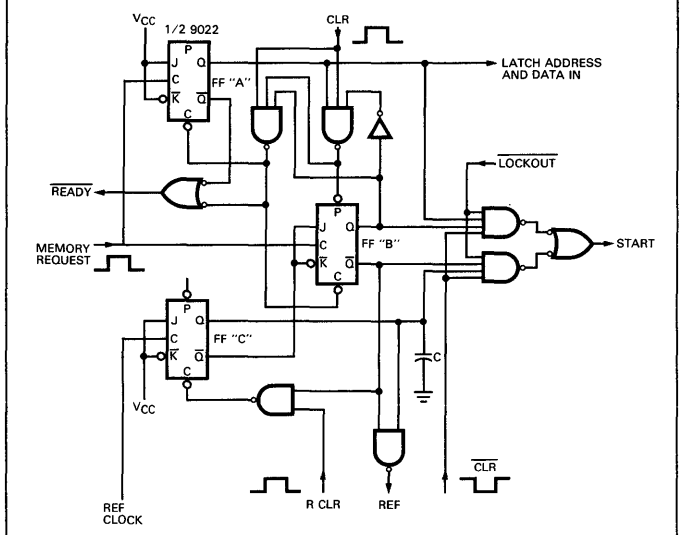


Fig. 4.5 Memory Cycle Control Logic

A normal cycle begins when MEMORY REQUEST simultaneously clocks flip-flop A and B. Initially, the three flip-flops were cleared. Flip-flop A is set and a BUSY signal ($\overline{\text{READY}}$) is sent to the logic responsible for controlling the memory. Addresses and input data may also be latched at this time. Flip-flop B sets only if a refresh cycle is not in progress or about to begin. A START signal is then generated to initiate the timing logic. Near the end of any memory cycle, a clear pulse (CLR) is provided by the timing unit and for a normal memory cycle, flip-flops A and B are then cleared. On the trailing edge of the clear pulse, the logic indicates READY and can accept another request.

When a refresh clock pulse occurs flip-flop C is set and flip-flop B is inhibited. If flip-flop B is clear (no normal cycle in progress), the START signal is generated after a delay (determined by C) and the refresh cycle begins. The refresh addresses are also enabled at this time. The delay allows sufficient time for flip-flop B to set if a MEMORY REQUEST were received immediately after the J K inputs to flip-flop B changed. If a normal cycle is in progress when flip-flop C sets, the refresh cycle is delayed and can begin only after the normal cycle is completed (flip-flop B is cleared and CLR goes high).

Near the completion of a refresh cycle, RCLR and CLR are generated, flip-flop C is cleared, and the refresh address counter is incremented. If a memory request had been received during the refresh cycle, flip-flop B is set by CLR and the normal cycle can begin when $\overline{\text{CLR}}$ goes high. This logic has effectively hidden the refresh cycles from the controller and only occasional increases in memory access and cycle times are noticed.

In applications where uncertainties in access and cycle times are not desirable, two techniques may be used. First, the basic memory cycle can be increased to permit a refresh cycle to occur as part of the normal cycle. In this case, each memory cycle allows sufficient time for a normal cycle and a refresh cycle. Another alternative possible with the 3534 is to abandon or "abort" a refresh cycle at any time. This is true even when CE is active on the 3534s and is possible because of the absence of refresh amplifiers on chip. Therefore, a memory request can be processed immediately and the refresh cycle can be restarted at a later time. If this technique is employed, care must be taken to insure that each refresh cycle can be completed somewhere in its 60 μs window.

The circuit shown in Figure 4.5 requires a maximum of 44 ns to translate a memory request into the START signal. This delay can be considerably reduced using higher speed logic in a similar design. In systems where a high frequency clock is available to the memory, synchronous operation of the control and/or timing logic may also be desirable. Furthermore, depending upon the technique used to generate the timing intervals, the control logic can be suitably modified to improve performance.

TIMING UNIT

The timing unit is responsible for generating PCHG, CE and the internal memory signals (CLEAR PULSE, DATA STROBE) required for system operation. Because R/W is a level in a 3534 system, a R/W pulse and its associated logic can be eliminated. If the memory is required to perform a read/modify/write cycle, R/W can be placed at the low level on chip as soon as the data output register has been loaded. This type of cycle can then be completed (after the new data has been valid for the specified time) by terminating CE.

There are many techniques available for generating the required memory signals including delay lines, counters, shift registers and one-shots. Depending upon the performance required, each of these approaches can be used with the 3534. This differs considerably from an 1103 type memory where a worst case design requires very precise control of the timing intervals as shown earlier. In applications where it is possible to adjust the timing after the system is operating (vary one-shot pulses, adjust clock frequencies, change delay line laps), access and cycle times can be optimized for that particular system. As an example of this type of timing, Figure 4.6 illustrates pulse generation using 9602 one-shots with adjustable pulse widths. The number of one-shots can be reduced if longer access and cycle times are acceptable.

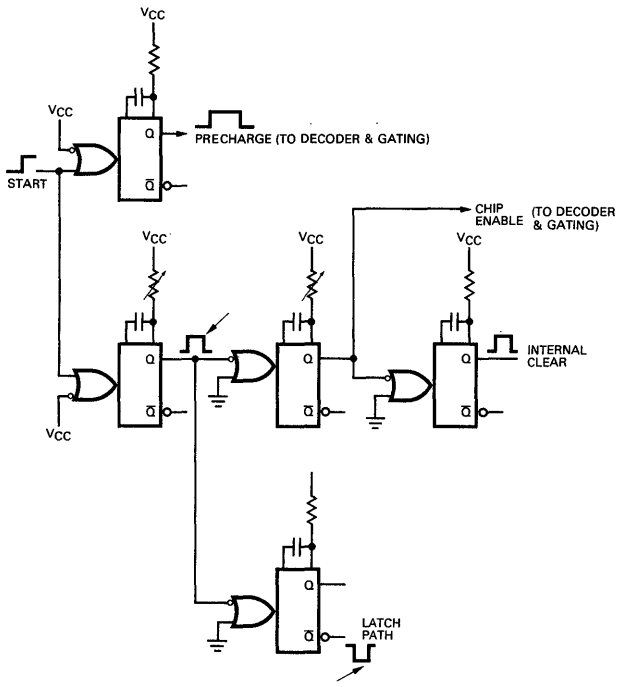


Fig. 4.6 Timing Generation Using Adjustable 9601 or 9602 One-Shots

The block diagram of Figure 4.7 depicts a Grey Code or Johnson counter with the necessary decoder logic circuitry. As the counter changes state, the outputs are decoded to generate the desired timing intervals. This particular type of counter is used to prevent "glitches" or "sliver pulses" from occuring at the decoder outputs as the counter changes state since only one bit can change on each clock pulse. The counter may be clocked by an available system clock, or an oscillator can be constructed as shown. Depending upon the resolution required and the logic family employed, the counter can be operated at frequencies ranging from 10 to 50 MHz or higher. Resolution can also be improved by using both the clock and its complement to enable the decoder. At the end of each cycle, the counter is cleared in preparation for the next request. The 3534 permits the use of a lower frequency clock (less resolution) in this technique because of its relaxed timing requirements.

Another approach to timing generation was illustrated in the Section covering system implications (II). The delay line shown in Figure 2.5 is tapped at the proper intervals to provide precise control of each signal. At each tap, the signals may be gated as shown or they may be latched. Faster cycle times can result if a latch is used because a narrow pulse (approximately 50 ns) can then be propogated. The latch can be set at one tap and cleared at a later time. With either approach, the pulse width is determined by locking out the delay line input as shown in the control logic diagram of Figure 4.5.

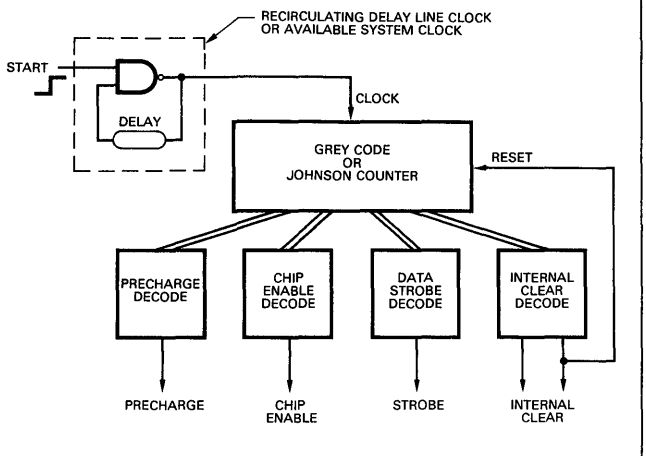


Fig. 4.7 Timing Generation Using a Grey Code or Johnson Counter

REGISTERS AND DECODER LOGIC

The remaining system logic is composed of address and data registers and the decoder logic used to distribute PCHG and CE to the selected areas of the memory.

Address and Data Registers

Depending on the system requirements, an address register similar to those of Figure 4.8 may be required. In applications where longer cycles are acceptable or where the address path is not critical, registers employing the 9308, 9314, 9375, or 9377 may be used. These MSI devices can reduce the register package count considerably. For higher speed TTL systems, the 9S74 or 9S112 may be used to minimize delays in the address path. High speed MSI circits include the 93H00 and the 93H72 4-bit registers.

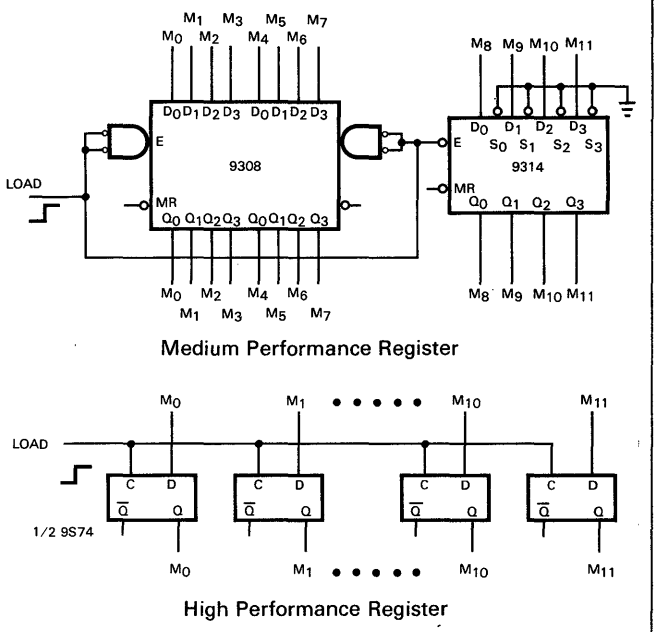


Fig. 4.8 12-Bit Memory Registers

A register is usually required for output data and may also be required to latch input data. The device types used for the address register may also be used to construct data registers. With some additional gating, one register can be used for both input and output data.

Decoder Logic

For the 4 k x 9 basic storage board assumed, address bits A_{10} and A_{11} are decoded to select one of the four rows on a storage board. The logic shown in Figure 4.9 decodes both CE and PCHG. During a refresh cycle, all four rows are enabled. For small systems, PCHG need not be decoded and the decoding logic can be reduced. For larger systems where many storage boards are driven, two or more 9002 gates or a single 9009 gate can be used for the output stage. MSI decoder available include the 9321 (Dual 1-of-4) and the 9311 (1-of-16).

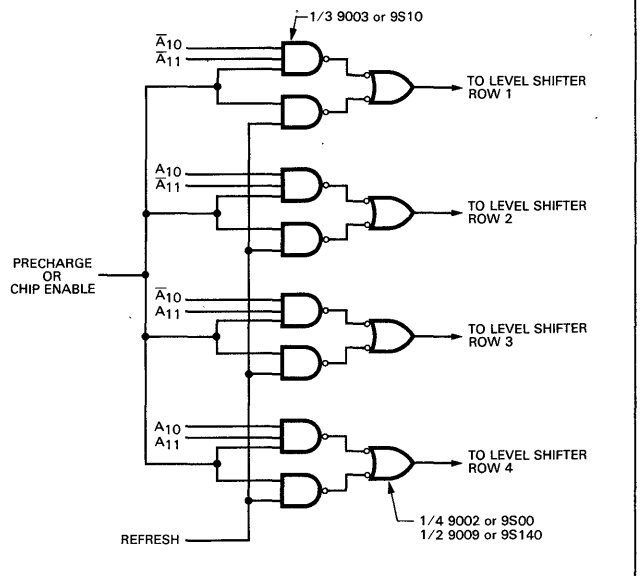


Fig. 4.9 Precharge or Chip Enable Decoder/Driver

As the memory system size increases, it may also be desirable to generate card select signals from the most significant address bits. This permits all but the selected storage boards to remain in a low power mode. Addresses A_0 through A_9 can then be gated and are active only on the selected storage boards.

DESIGN ADVANTAGES OF THE 3534

As a result of the 3534 simplified interface requirements and ease of system implementation, the system logic designer may select from many performance improvements and/or cost reductions. Regarding the selected logic family for example, many high speed gates and flip-flops can be replaced by slower and less expensive gates, flip-flops, or MSI packages and the resulting system will still have performance equal to that of more expensive 1103 designs. Specificially, the data registers, decoder logic, timing unit, and the cycle control logic can be affected. Conversely, by maintaining the higher speed logic, system performance can be increased.

Since overlap control is not required with 3534s, the resolution of the timing unit may be decreased. This can result in a smaller counter or shift register (fewer bits) and less decoder logic. Since a pulse is not required for R/W, the associated timing and decoding logic can also be eliminated. More significantly, only one timing chain is required for optimum read, write, and refresh cycles thus eliminating multiple paths through the timing and decoding logic. The system logic is simplified and still permits optimum performance. At the system operation level, the uncertainty in access and cycle times due to refresh cycles can often be eliminated by abandoning refresh cycles at any time. Hence, the memory availability can be maximized.

There are numerous other advantages of a 3534 system that arise from the simplicity of the device operation. These include the ease of debugging, testing, manufacturability, and maintenance. These somewhat intangible factors can greatly affect the final cost of any memory system. A Fairchild 3534/1103 system will minimize these costs as well as those more directly related to the memory design.

3708

MOS MONOLITHIC 8-CHANNEL MULTIPLEX SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3708 is an 8-Channel Multiplex Switch with output enable control and one-out-of-eight decoder included on the chip. It is manufactured using P-channel enhancement mode silicon gate technology. The logic input lines of the 3708 are NPN bipolar compatible and can be used directly with TTL 5.0 V logic levels with no level shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

- **ONE-OUT-OF-EIGHT DECODER ON THE CHIP**
- **HIGH ON/OFF RATIO**
- **OUTPUT ENABLE CONTROL**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**
- **FAST SWITCHING TIME 0.8 μs (TYP) AT T_A = +85°C**
- **TTL COMPATIBLE INPUT LOGIC LEVELS**

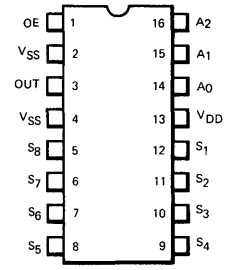
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any Pin	+0.3 V
Negative Voltage on Digital and Analog Input Pins	−30 V
Negative Voltage on Digital and Analog Output Pins	−30 V
Negative Voltage on V_{DD} Pin	−30 V
Total Power Dissipation in Package (T_A = 25°C)	200 mW

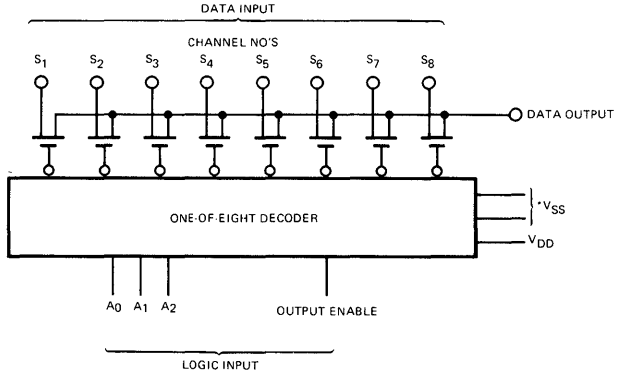
The 3708 is available for use in two signal ranges
−5.0 to +5.0 V signal applications, 37082
0 to +5.0 V signal applications, 37083

NOTES:
1. These ratings are limiting values above which the serviceability of the device may be impaired.
2. Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

CONNECTION DIAGRAM
DIP (TOP VIEW)



SCHEMATIC DIAGRAM



*Both V_{SS} lines are internally connected; either one or both may be used.

TTL TRUTH TABLE

LOGIC INPUTS				CHANNEL
A_0	A_1	A_2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

DC CHARACTERISTICS

For 37082: V_{OUT} = −5.0 V to +5.0 V, V_{DD} = −19 ±1 V, V_{SS} = 5.5 V ± 0.5 V, T_A = 25°C.
For 37083: V_{OUT} = 0 V to +5.0 V, V_{DD} = −19 ±1 V, V_{SS} = 5.5 V ±0.5 V, T_A = 25°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
*V_{IH}	Input Voltage HIGH	V_{SS} −1.5		V_{SS}	V	
*V_{IL}	Input Voltage LOW	V_{DD}		+0.2	V	
I_{LI}	Logic Input Leakage Current			1.0	μA	$V_{SS} - V_{LOGIC\text{-}IN}$ = 15 V
I_{LD}	Data Input Leakage Current					
	37082			3.0	nA	$V_{SS} - V_{IN}$ = 15 V
	37083			2.0	nA	$V_{SS} - V_{IN}$ = 10 V
I_{LO}	Output Leakage Current		2.0	10	nA	$V_{SS} - V_{OUT}$ = 15 V
I_{LO}(85°C)	Output Leakage Current		100	500	nA	$V_{SS} - V_{OUT}$ = 15 V
R_{ON}	Data Channel "ON" Resistance					
	37082		250	400	Ω	V_{OUT} = −5.0 V, I_{OUT} = −100 μA
	37083		190	350	Ω	V_{OUT} = 0 V, I_{OUT} = −100 μA
R_{ON}	Data Channel "ON" Resistance		125		Ω	V_{DD} = −20 V, V_{SS} = +5.0 V I_{OUT} = −100 μA
R_{OFF}	Data Channel "OFF" Resistance	1.5	5.0		GΩ	$V_{SS} - V_{OUT}$ = 15 V
P_D	Power Dissipation		130		mW	V_{DD} = −26 V, V_{SS} = 0 V

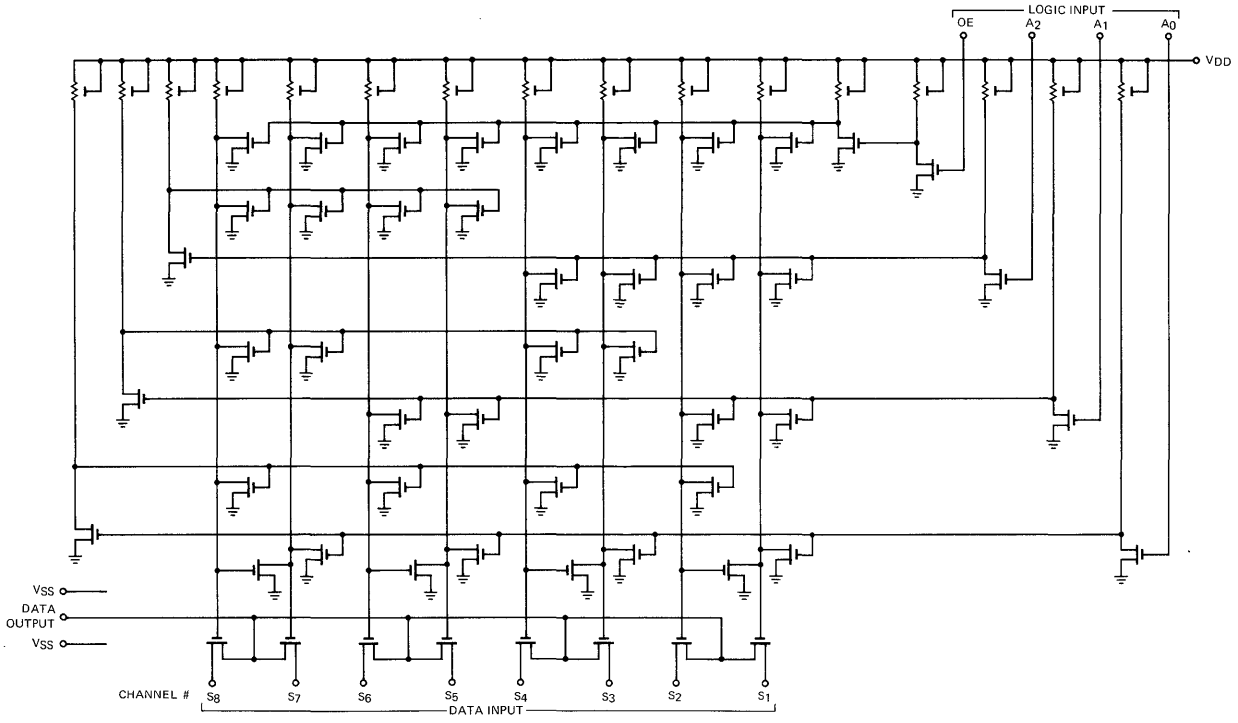
AC CHARACTERISTICS:

For 37082: V_{OUT} = −5.0 V to +5.0 V, V_{DD} = −19 ± 1 V, V_{SS} = 5.5 ±0.5 V, T_A = 25°C.
For 37083: V_{OUT} = 0 V to +5.0 V, V_{DD} = −19 ±1 V, V_{SS} = 5.5 ±0.5 V, T_A = 25°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_S	Channel Switching Time (See Fig. 1)		0.45		μs	
t_S(85°C)	Channel Switching Time (See Fig. 1)		0.8	1.5	μs	
t_D	Channel Switching Time (See Fig. 1)		1.0	2.5	μs	
C_D	Data Input Capacitance		4.5		pF	$V_{SS} - V_{IN}$ = 0 V, f = 1.0 MHz
C_I	Logic Input Capacitance		3.0	175	pF	$V_{SS} - V_{LOGIC\text{-}IN}$ = 0 V, f = 1.0 MHz
C_O	Output Capacitance		25		pF	$V_{SS} - V_{OUT}$ = 0 V, f = 1.0 MHz

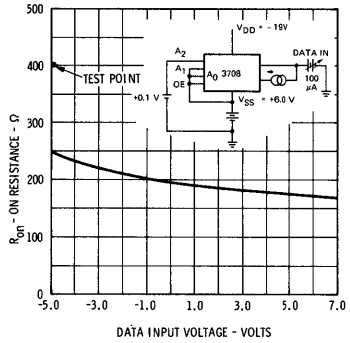
*When driven by TTL elements, avoid excessive dc loading of TTL elements to insure 3708 logic levels under maximum fan out conditions. Analog input signal swing should not exceed V_{SS} (= V_{CC}).

SCHEMATIC DIAGRAM

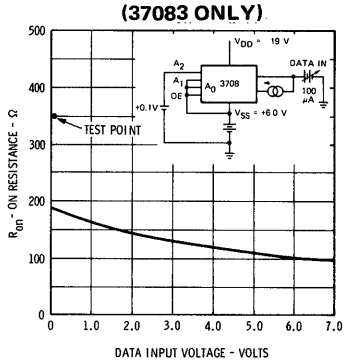


TYPICAL DEVICE CHARACTERISTICS

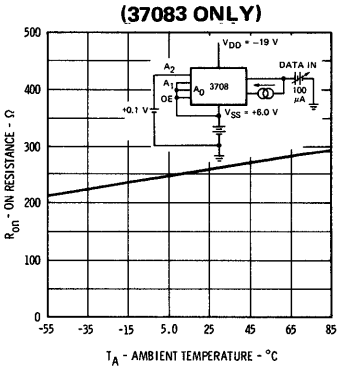
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (37082 ONLY)



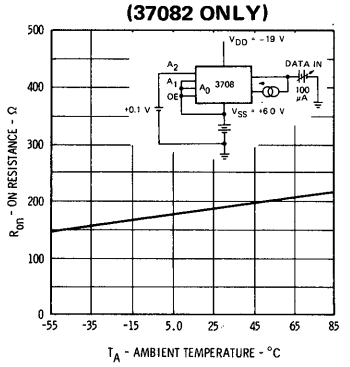
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (37083 ONLY)



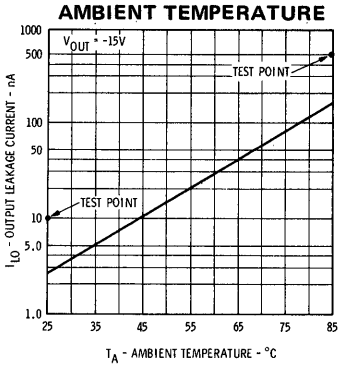
ON RESISTANCE VERSUS AMBIENT TEMPERATURE (37083 ONLY)



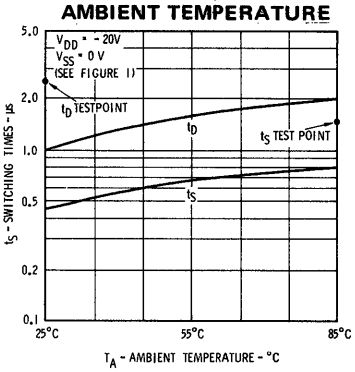
ON RESISTANCE VERSUS AMBIENT TEMPERATURE (37082 ONLY)



OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT

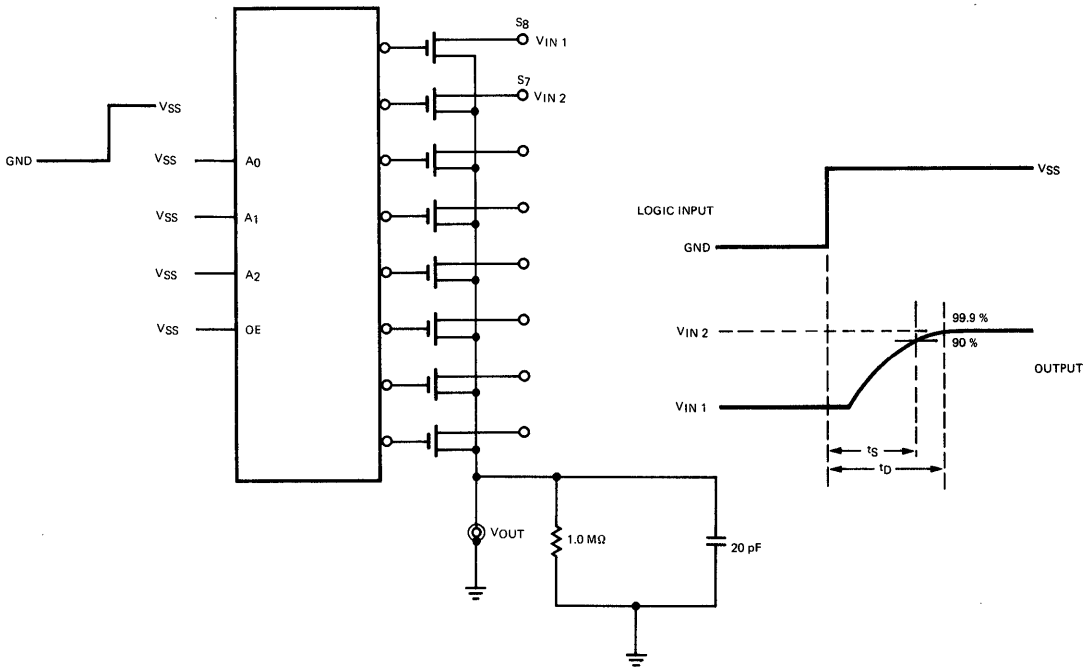
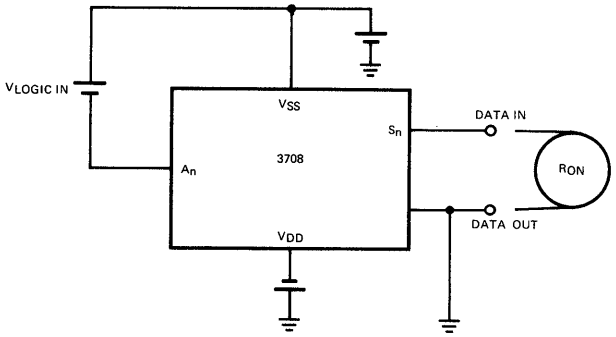


Fig. 1

POWER SUPPLY TRANSLATION CIRCUIT

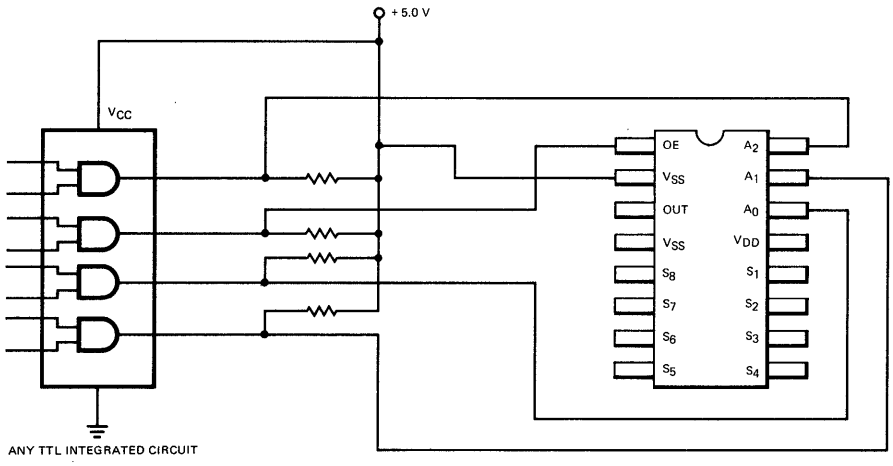


The following sets of power supplies are equivalent:

	CONDITION 1	CONDITION 2
DATA IN	+5.0 V	0 V
V_{SS}	+6.0 V	+1.0 V
V_{DD}	−18 V	−23 V
LOGIC IN		
LOW Level	+0.2 V	−4.8 V
HIGH Level	+5.5 V	+0.5 V

Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body or V_{SS}). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the ON resistance of the data channel accurately, the data output is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

TYPICAL CONTROL CIRCUIT



3814
DIGITAL VOLTMETER LOGIC ARRAY
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3814 provides the logic required to implement a 4 1/2-Decade Digital Voltmeter. In addition to four full decade counters and two overflow latches, the device is designed to drive a multiplexed display providing a Binary Coded Decimal output (to drive a BCD converter) and five decoded outputs to strobe the display.

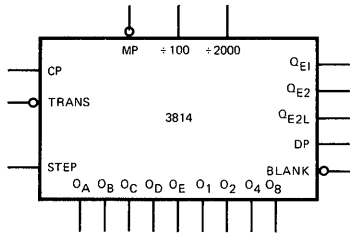
Automatic leading zero blanking is simply accomplished, and a separate input is provided to blank the entire display. Other outputs provide counter overflow information and auto-ranging control signals. The 3814 is manufactured using silicon gate P-channel enhancement mode technology.

- **DIRECT TTL/DTL COMPATIBILITY – NO EXTERNAL COMPONENTS**
- **DC TO 600 kHz OPERATION**
- **BCD OUTPUT – COMPATIBLE WITH DISPLAY DECODERS**
- **EXTERNAL CONTROL MULTIPLEX FREQUENCY – ACCOMMODATES LED DISPLAYS**
- **UNDER RANGE AND OVER RANGE OUTPUTS**
- **10-COUNT DELAY TO MASK ANALOG SWITCHING NOISE**

ABSOLUTE MAXIMUM RATINGS

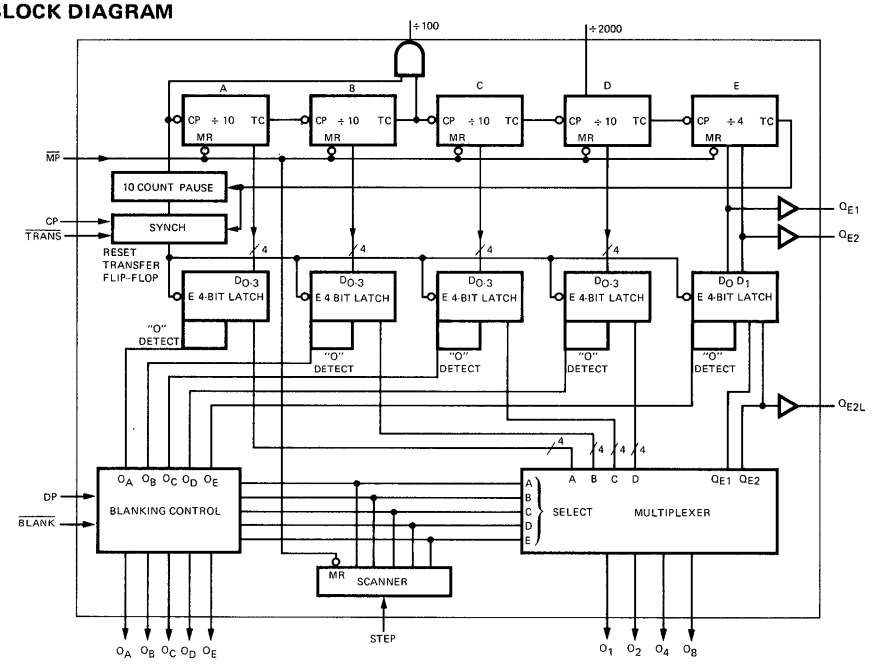
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to 70°C
V_{GG}	+0.3 to -24V
All Other Inputs	+0.3 to -16V
Outputs	+0.3 to -8V (I_L < 10 mA)

LOGIC SYMBOL

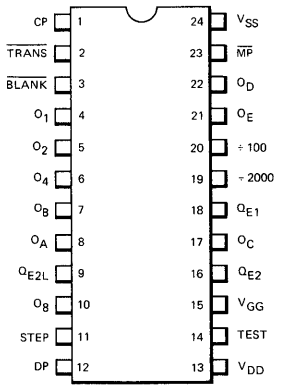


V_{SS} = PIN 24
V_{GG} = PIN 15
V_{DD} = PIN 13

BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION: The 3814 is intended for use as the digital logic portion of digital voltmeter systems. An input clock (CP) drives 4-1/2 decades of BCD counters, with the counters changing state on the LOW to HIGH clock transition. The output of the second decade is gated with the input clock (CP) and brought off chip (÷100) for use as an additional clock. This clock may be used to drive the multiplexer input (Step).

A clock input following a LOW state on Master Preset ($\overline{MP}$) will set the counters to 30,000. The 3814 will then count the next 10,000 clock pulses, and be in the 00,000 state. At this count the device will ignore the next 10 clock inputs. This feature is useful when the device is used in systems where the current switching associated with analog to digital conversion generates transients which might cause false triggering. This 10 count correction requires a small current (equal to the integral of 10 counts of the standard current) be added to the unknown current. Thus, even if the current to be measured is zero, the integrator output voltage is moved off zero, eliminating comparator transient triggering. Following this 10 count pause, the 3814 continues to count; in normal operation the A/D circuitry will provide a transfer input, causing the count to be loaded into the latches. The count stored (and present at the output multiplexer) will be proportional to the ratio of the unknown current to the standard current. The counter will continue to accept clock pulses, and at 20,000 the Q_{E1} output will go LOW and the Q_{E2} output will go HIGH. This state may be decoded and used to reset the analog circuitry. Since current switching associated with this reset may again cause false triggering, only one transfer command is accepted during the interval from 00,000 to 39,000.

In typical operation, the states of the two overflow flip-flops (Q_{E1} and Q_{E2}) may be used to control system operation.

COUNT	Q_{E1}	Q_{E2}
30,000 to 00,000	1	1
00,000 to 10,000	0	0
10,000 to 20,000	1	0
20,000 to 30,000	0	1

In addition, the Q_{E2} output is latched and brought out as Q_{E2L}. If a system utilizing a full scale count of 19,999 is implemented with the 3814, the HIGH state of Q_{E2L} will indicate an over-range condition. The divide by 2,000 output (÷2,000) is intended for use as an under-range indicator. If this output has not gone HIGH when a transfer command is received, the total count is less than 10% of full scale.

DATA OUTPUTS – The state of one of the 4 1/2 decade counters is presented as a BCD multiplexed output (O_1, O_2, O_4, O_8). One of the five decoded outputs (O_A, O_B, O_C, O_D, O_E) will be HIGH, indicating which decade's count is present at the BCD outputs. The multiplexer is clocked by a separate input (Step) which may be driven at 1/100 of the clock frequency by directly connecting the ÷ 100 output to the Step input.

BLANKING – Automatic leading zero blanking is simply accomplished by directly wiring two pins of the 3814. One of the decade outputs (O_A through O_E) when wired to the decimal point (DP) input will cause all leading zeros to the left of the feedback decade to be automatically blanked. For example if the count is 00120 and decade "A" (O_A) is connected to DP, the display will be "120". With the same count, and decade "D" (O_D) connected to DP, the display will be 0120. When the $\overline{Blank}$ input is LOW all outputs (O_A thru O_E) go LOW.

TEST INPUT – This pin is used during the testing of the 3814 and must be wired to V_{SS} for operation.

DC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS}−1.0		V_{SS}+0.3	V	All Inputs Including CP
V_{IL}	Input Voltage LOW	−2		+0.8	V	All Inputs Including CP
V_{OH1}	Output Voltage HIGH	2.4		V_{SS}	V	a) Sourcing 200 μA for Outputs; Q_{E1}, Q_{E2}, Q_{E2L}, ÷2000, C_L <20 pF. b) Sourcing 400 μA for outputs; O_1, O_2, O_4, O_8; C_L <30 pF.
V_{OH2}	Output Voltage HIGH	V_{SS}−1.0		V_{SS}	V	Sourcing 200 μA for outputs O_A, O_B, O_C, O_D, O_E, ÷ 100; C_L <20 pF
V_{OL}	Output Voltage LOW			0.4	V	a) Sink 1.6 mA on outputs Q_{E1}, Q_{E2}, Q_{E2L}, O_A, O_B, O_C, O_D, O_E, ÷ 100, ÷ 2000; C_L <20 pF. b) Sink 2.0 mA on outputs O_1, O_2, O_4, O_8, C_L <30 pF.
R_{IN1}	Input Resistor Returned to V_{SS}	1	2.5	5	kΩ	Inputs: CP, $\overline{Blank}$, $\overline{MP}$, $\overline{Trans.}$
R_{IN2}	Input Resistor Returned to V_{SS}	10	25	50	kΩ	Inputs: Step, DP
I_{GG}	V_{GG} Supply Current	3	5	15	mA	
I_{SS}	V_{SS} Supply Current	20	30	50	mA	

AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to 70°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	COMMENTS
f	Operating Frequency	DC		1.667	μs	Figure 1
$t_{PW\phi}$	Clock Pulse Width	300	220		ns	Figure 1
t_{TS}	TRANS Set Up Time	250			ns	Figure 2
t_{TH}	TRANS Hold Time	50			ns	Figure 2
t_{DHL}	HIGH to LOW Transistion for Outputs					
	÷100		320	1000	ns	Figure 3
	÷2000		375	1000	ns	Figure 3
	Q_{E1}, Q_{E2}		400	800	ns	Figure 3
	O_1, O_2, O_4, O_8		450	1000	ns	Figure 4
t_{DLH}	LOW to HIGH Transition for Outputs					
	÷100,		350	1000	ns	Figure 3
	÷2000,		450	1000	ns	Figure 3
	Q_{E1}, Q_{E2}		425	800	ns	Figure 3
	O_1, O_2, O_4, O_8		550	1000	ns	Figure 4
t_{PDC}	Clock		60	200	ns	Figure 1

TIMING DIAGRAMS

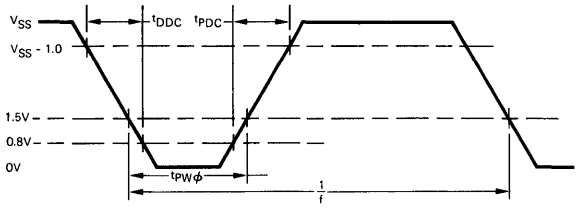


Fig. 1. Input clock waveform

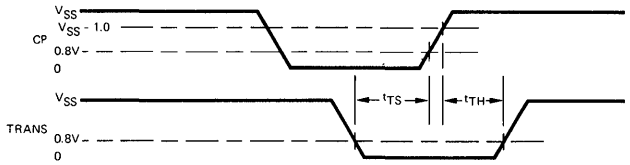


Fig. 2. Transfer setup and hold times

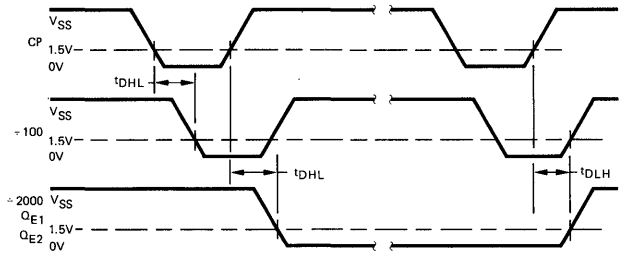


Fig. 3. Propagation delay-outputs

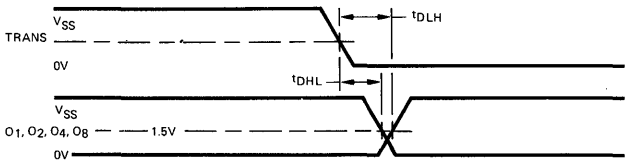
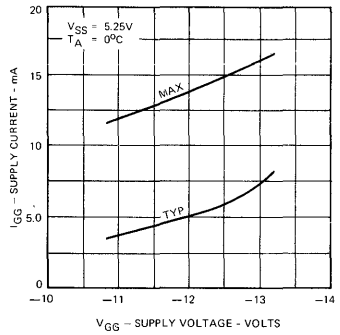


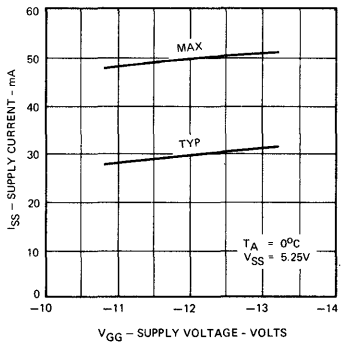
Fig. 4. Propagation delay - BCD outputs

ELECTRICAL CHARACTERISTICS

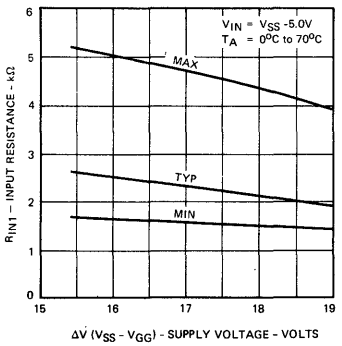
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



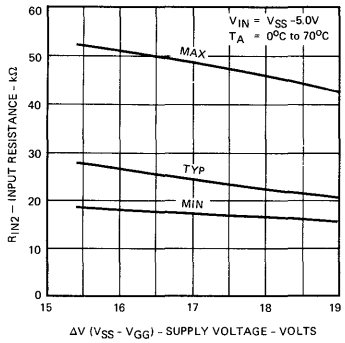
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



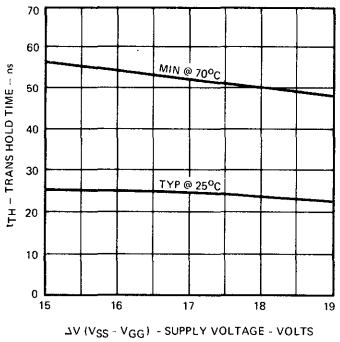
INPUT RESISTANCE VERSUS SUPPLY VOLTAGE (CP, $\overline{\text{BLANK}}$, $\overline{\text{MP}}$ AND $\overline{\text{TRANS}}$ INPUTS)



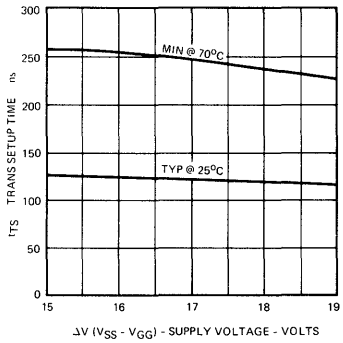
INPUT RESISTANCE VERSUS SUPPLY VOLTAGE (STEP AND DP INPUTS)



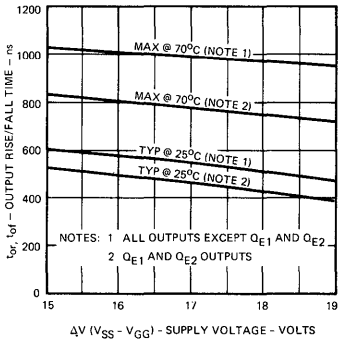
TRANSFER HOLD TIME VERSUS SUPPLY VOLTAGE



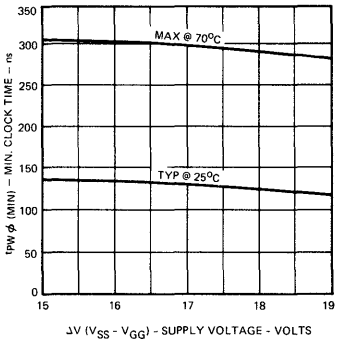
TRANSFER SET-UP-TIME VERSUS SUPPLY VOLTAGE



OUTPUT RISE/FALL TIME VERSUS SUPPLY VOLTAGE



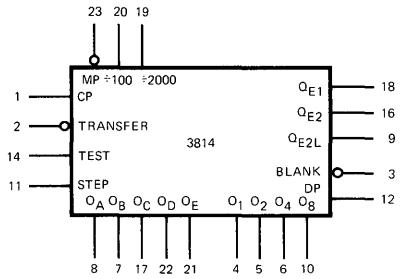
MINIMUM CLOCK TIME VERSUS SUPPLY VOLTAGE



THE 3814 DIGITAL VOLTMETER LOGIC ARRAY

INTRODUCTION

Fairchild Semiconductor has developed a silicon gate device that contains most of the logic required for a 4 1/2 decade digital voltmeter. All necessary BCD counters, latches and the display multiplexing logic is on chip. In addition, the control signals necessary for dual slope integration techniques are generated by the 3814 device. The BCD outputs can directly drive a 9315 BCD to 1-of-10 decoder or 9307 BCD to 7-segment decoder. Zero suppression is generated on chip by feeding back the DIGIT SELECT output. Outputs are also provided for indicating over range and under range. A unique feature of the 3814 is the incorporation of a 10-count pause at the start of an integration cycle to mask noise generated when switching the external analog circuits, such as the reference current source.



V_{SS} = LEAD 24
V_{DD} = LEAD 13
V_{GG} = LEAD 15

LEAD	
CP	CLOCK INPUT
TEST	TEST INPUT
MP	MASTER PRESET
TRANSFER	SYNCHRONOUS TRANSFER
DP	DECIMAL POINT INPUT
BLANK	BLANK INPUT
STEP	STEP INPUT
÷100	CLOCK OUTPUT CP/100
÷2000	SQUARE WAVE OUTPUT CP/2000
Q_{E1}	LSB DECADE 5
Q_{E2}	MSB DECADE 5
Q_{E2L}	Q_{E2} LATCHED
O_1, O_2, O_4, O_8	BCD OUTPUTS
O_A, O_B, O_C, O_D, O_E	DECODED DIGIT SELECT

Fig. 1. Logic symbol and lead designation.

DUAL SLOPE INTEGRATION

A reliable and accurate DVM circuit must be insensitive to long term changes of such factors as supply voltage, time base, and passive and active component values. For the short term, it must be able to reject 60 Hz line perturbations. Dual Slope Integration achieves a high degree of accuracy by causing the effect of changes in these parameters to cancel.

One method of Dual Slope Integration involves integrating a current directly related to the unknown voltage (V_X) for a fixed period of time, followed by the integration of a standard current (I_S) until the integrator output returns to zero. The amount of time required to null the integrator is directly proportional to the ratio of I_X to I_S and therefore to V_X. Since the same system power supply, time base and components are used for integrating the known and unknown currents, their absolute values are not extremely critical.

3814 BLOCK DIAGRAM

The 3814 provides 4 1/2 decades of BCD counters, with a modulus of 40,000, clocked by the CP input, (Figure 2). The CP input is TTL compatible and requires a low time of 300 ns minimum and a high time of 500 ns minimum. The counters change state on the low-to-high CP transition.

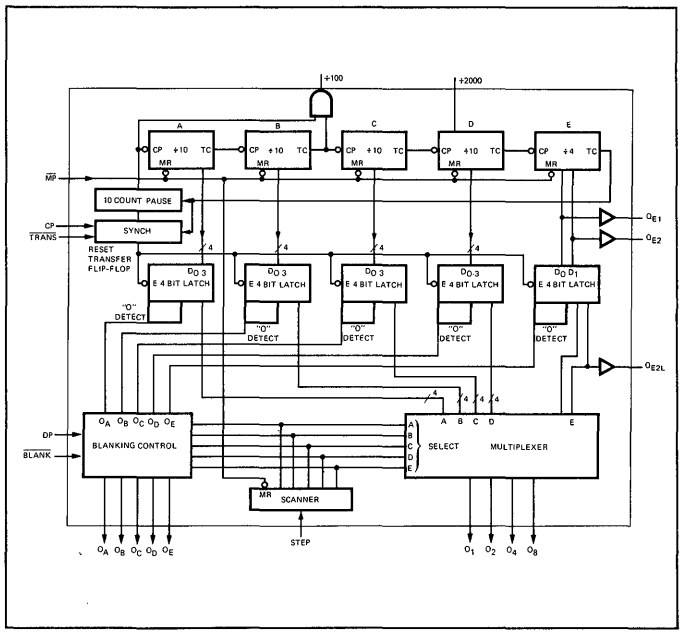


Fig. 2. Block diagram.

The second decade output is gated with the clock and brought off chip to provide a clock pulse output for every 100 input clocks ("÷100 output"). The output of the first flip-flop of the thousands decade is buffered and brought directly off chip as "÷2000". The outputs of both flip-flops of the fifth "half decade" are available as outputs Q_{E1} and Q_{E2}. The latched state of the most significant bit (Q_{E2L}) is also brought off chip.

A TRANSFER input causes the data in the counters to be stored in the latches. This input is edge sensitive and is synchronized internally with the clock. When the TRANSFER input changes from high to low the circuit is enabled, so that when CP goes low, data is stored. A TRANSFER command is permitted only once during a count cycle by an internal flip-flop which is set when the first transfer occurs, and remains set until the next terminal count (counters advancing from 39,999 to 00,000). Transfers are ignored when this flip-flop is set.

The latched state of each decade is multiplexed out as BCD data on outputs O_1, O_2, O_4 and O_8. The multiplexer is driven by a scanner counter with outputs O_A, O_B, O_C, O_D and O_E available. This counter is clocked by the STEP input causing the stored data to appear, decade by decade, on the O_1, O_2, O_4 and O_8 outputs. One of the O_A through O_E outputs will be high indicating the decade displayed. The BLANK input (active low) causes all five of these outputs to go low. Because outputs O_A through O_E can drive display lamps in a multiplexed system the display will blank when they are low.

FUNCTIONAL DESCRIPTION

Figure 3 is a simplied schematic of a digital voltmeter using a 3814 with an integrator and comparator front-end. Figure 4 shows the output waveforms of the integrator and comparator for a typical cycle when some unknown voltage is applied to the input of the integrator (V_x). During the time interval from 30,000 to 39,999, a current I_x ($\approx V_x/R_x$) is integrated. When the counter reaches 40,000 (or 00,000), the input to the integrator is switched to integrate the standard current I_s. Integration of the standard current continues until the integrator crosses the null point. At this time, the comparator output switches states to a LOW and this signal is used to cause a transfer of the count into the latches in the 3814. The stored count is then directly proportional to the ratio I_x/I_s. When the count reaches 20,000, the analog circuitry can be reset to zero.

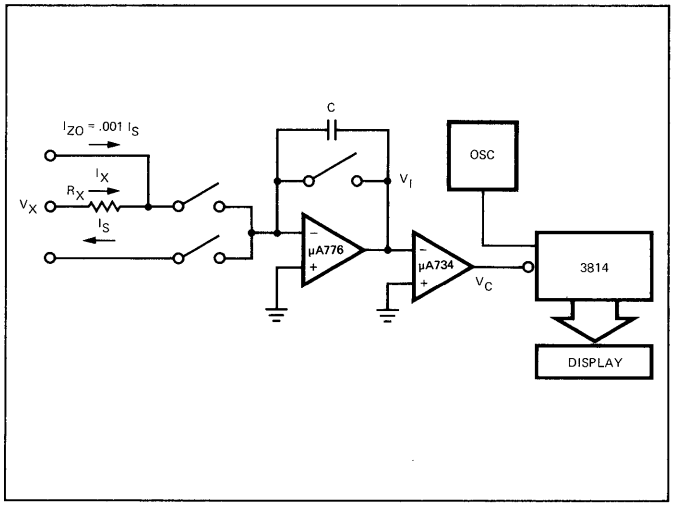


Fig. 3. Simplified schematic of front end.

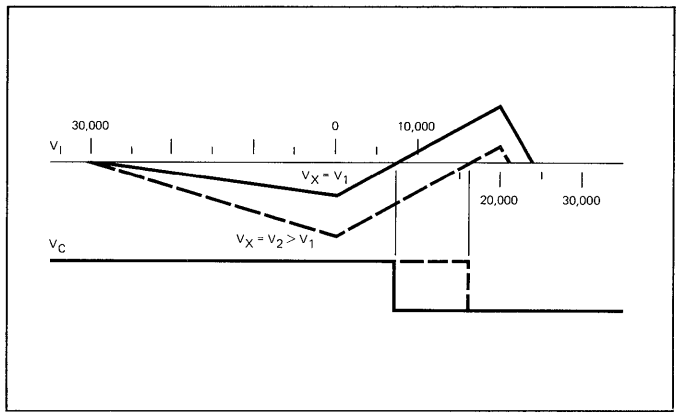


Fig. 4. Integrator and comparator waveforms.

A glitch may occur in the null detector output when it changes state or during an analog reset. To prevent false loading of a count into the storage latches, the transfer input is accepted only once during the interval 00,000 to 39,999. Any transfer commands after the first one are ignored.

The control for the various periods of integration can be obtained from the Q_{E1} and Q_{E2} outputs of the 3814. A "11" state means the unknown should be integrated, an "XO" means the standard should be integrated and a "01" means the reset period is present. (The circuitry need not be reset here if a DVM capable of displaying 0, 1 or 2 in the most significant decade is desired. In this case, the analog signals must be rapidly reset at count = 30,000.) If only a 0 or a 1 in the most significant decade is required, a transfer occuring during the interval 20,000 to 30,000 indicates overflow. This can be detected by the Q_{E2L} output, which will be high if a count greater than 19,999 was stored in the latches. This can be used to indicate overflow, to automatically up-range, and to blank the display by means of the BLANK input. Forcing MASTER PRESET (MP) sets the internal counters to 30,000 on the next clock pulse.

The ÷2000 output can be used to down range in an autoranging instrument. If this output has not yet gone high when the transfer is received, then the count is less than 10% of full scale (count <1000).

The data outputs are designed to drive a multiplexed display system. A single decoder/driver (such as the 9315 BCD to 1-of-10, or the 9327 BCD to 7-segment) is connected to the O_1, O_2, O_4 and O_8 outputs. The outputs of the decoder drive *all* the display devices. The O_A, O_B, O_C, O_D and O_E outputs drive transistors which select the desired digit. The BCD will have one quarter unit load left over which can be used to drive a low power TTL latch (93L00) or register if parallel BCD data is desired as an additional output of the DVM.

The STEP input, which drives the output multiplexer, can be driven directly from the ÷100 output or can be driven by a separate oscillator.

ZERO OFFSET

An analog glitch also occurs when the integrator input is switched from I_x to I_s. If the input voltage is near zero, the integrator output is close to the null line at the end of the integration. The glitch might cause false triggering of the null detector. For this reason I_{ZO} adds a quantity of charge equal to ten counts of I_s during the integration of the unknown voltage V_x as shown in Figure 3 and Figure 5. This fixed offset guarantees that the integrator output moves away

from the null even if the input voltage is zero. When the counter on the 3814 reaches 40,000 (00,000) the counter remains at zero for ten counts, thus subtracting out the extra ten units of current added during the integration of the unknown voltage.

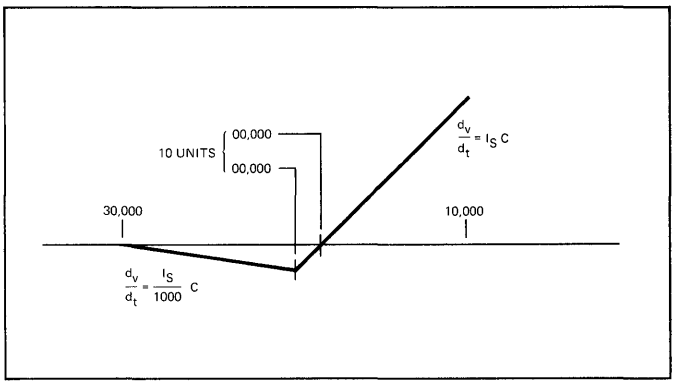


Fig. 5. Integrator output when $V_X = 0$ showing desired zero offset.

LINE REJECTION

Line rejection is important for measuring voltages from high impedance sources. As shown in Figure 6, any 60 Hz components contained in the unknown voltage have an average voltage of zero only if the sample period is some harmonic of 60 Hz. Since the sample period of the 3814 is 10,000 clocks, a suitable clock frequency would be 600,000 Hz for good line rejection. This would give a sample rate of 15 Hz and an output multiplex rate of 6 kHz if the ÷100 output is used as the STEP input.

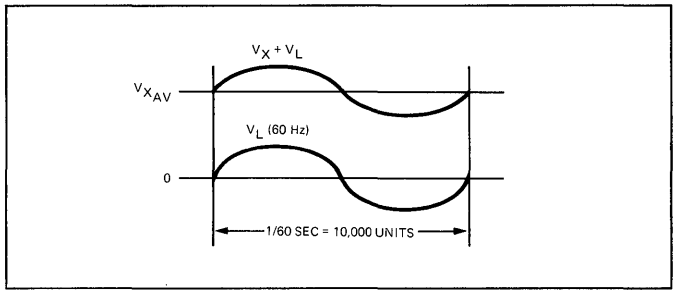


Fig. 6. Line rejection.

DECIMAL POINT

The position of the decimal point in the display is selected by an external switch. For zero suppression, the DP input of the 3814 must be driven by one of the five DIGIT SELECT outputs. This feedback inhibits the zero suppression for that decade and all remaining decades to the right. If the DP input is tied to V_{SS}, all digits are displayed. Tying DP to V_{DD} has the same effect as tying it to output O_E. The different possibilities are shown in Figure 7.

DIGIT FED BACK	COUNT	DISPLAY *
A, or DP = V_{SS}	00000	0
A, or DP = V_{SS}	00120	120
B	00120	12.0
C	00120	1.20
D	00120	0.120
E, or DP = V_{DD}	00120	0.0120
		E DCBA

*The decimal point itself in the display is not controlled by the 3814.

Fig. 7. Decimal point positioning.

EXPANSION TO 5 1/2 DECADES

To increase accuracy, additional decades can be added using standard MSI components. Figure 8 shows the extra devices needed to realize a 5 1/2 digit system.

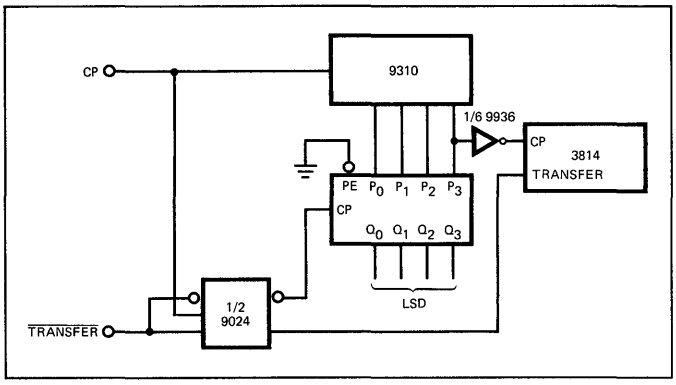


Fig. 8. Modification for 5-1/2 decades.

UNDER RANGE INDICATOR

For input voltages less than 10% of full scale, an under range signal can be generated by gating Q_{E1}, Q_{E2}, the ÷2000 output and the analog comparator output. Figure 9 shows circuitry required for a constant output which can be used to turn on a Light Emitting Diode or as a control signal for auto-ranging circuitry. A pulsed output is shown in Figure 10.

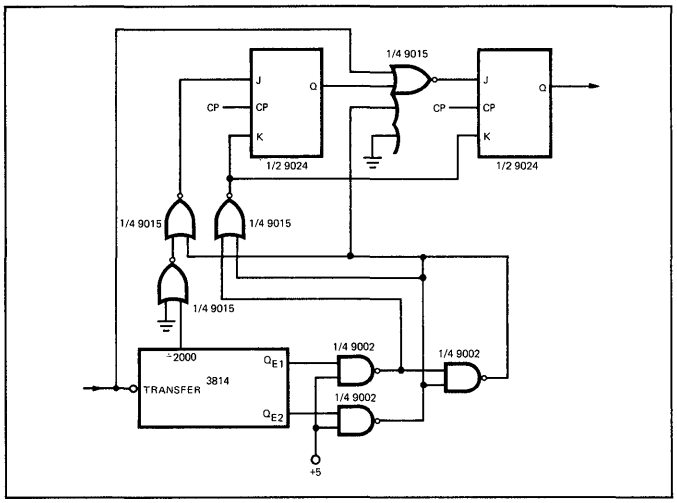


Fig. 9. Under range indicator.

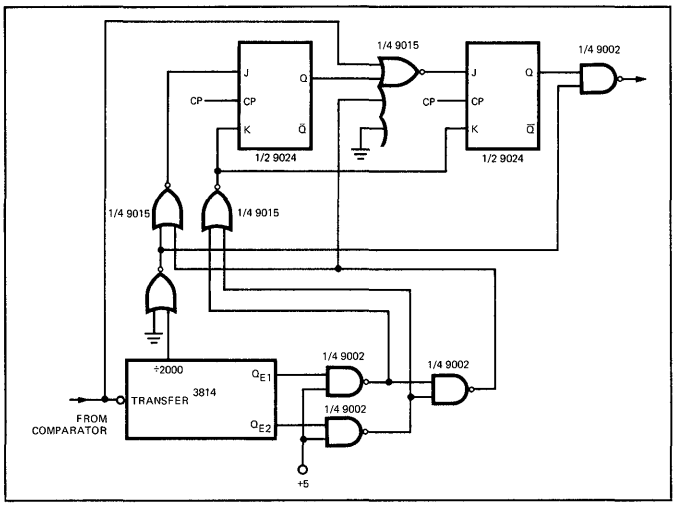


Fig. 10. Blinking under range indicator.

BLANKING BETWEEN DIGITS

While the outputs are multiplexed to the various digits, interference may appear depending on the type of display and the multiplex rate. Figure 11 shows a self-driven blanking scheme to assure that the segment select inputs are stable prior to digit select

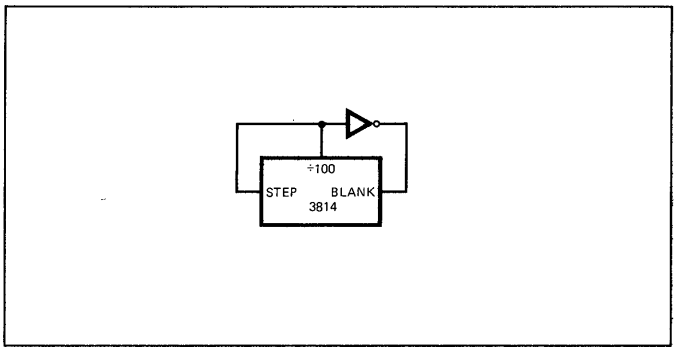


Fig. 11. Self-driven multiplexer with blanking between digits.

GAS DISCHARGE DISPLAY

The BCD outputs of the 3814 will directly drive the 9315 1-of-10 decoder for systems using NIXIE* display tubes. Figure 12 shows the circuit required. For detailed information, see Fairchild Application Note 212 on digital display systems.

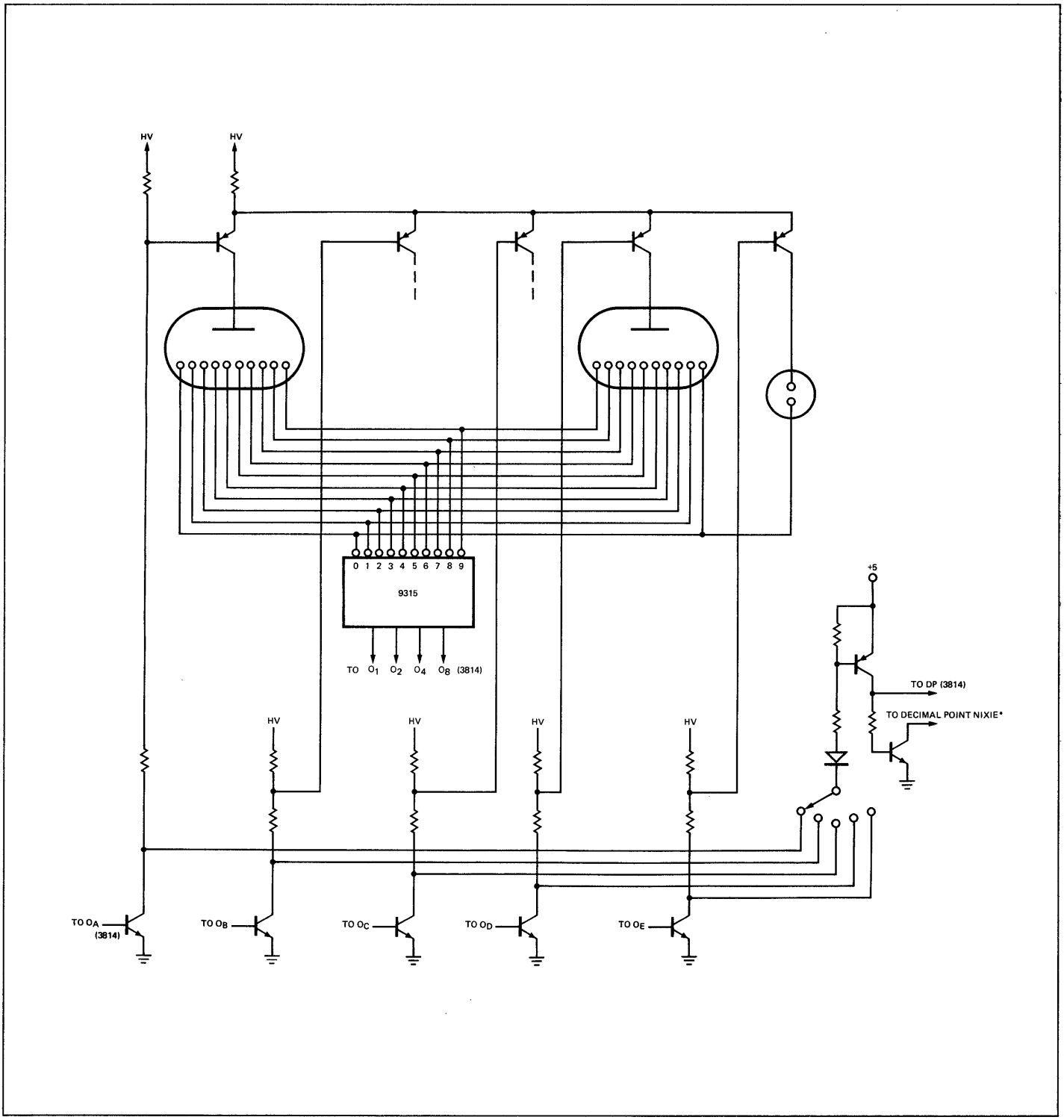


Fig. 12. NIXIE* output.

*NIXIE is a registered trademark of the Burroughs Corp.

LOW COST DVM

Figure 13 shows one version of the basic DVM shown in Figure 3. An input buffer, such as μA776, could have been added to boost the input resistance to 400 MΩ and provide isolation of the unknown from the action of the current sources. If source resistance is low, the buffer may not be needed. The I_{ZO} and I_S current sources have been implemented with discrete components. Also, temperature compensation has been added to the I_S circuit as this is most critical to system accuracy. As designed, only positive inputs are properly integrated. If negative input capability is also desired, additional current sources and gating are needed.

Ideally, SW_1 and SW_2 have zero resistance when on, infinite resistance when off and no offset voltage. For an accurate system then, bipolar transistors cannot be used because of offset. P-Channel or N-Channel FETs ably satisfy all three of the switch criteria. To avoid gate-to-source debiasing, P-Channel devices should be used for negative input voltages and N-Channel devices for positive inputs. The versatile μA776 is used again as the integrator amplifier; the μA734 comparator receives the integrator signal and upon a null crossing, generates the transfer command to the 3814. All gating for mode control to SW_1, SW_2 and SW_3 is obtained from the Q_{E1} and Q_{E2} output. The FND21 LED Display Module and the associated decoder and drivers are also shown. For flexibility of decimal point location and zero suppression, a five position SPST switch has been added to appropriately gate the DIGIT SELECT outputs to the DP inputs.

This DVM can be built with a total of *only six integrated circuits; seven* if input buffering is required.

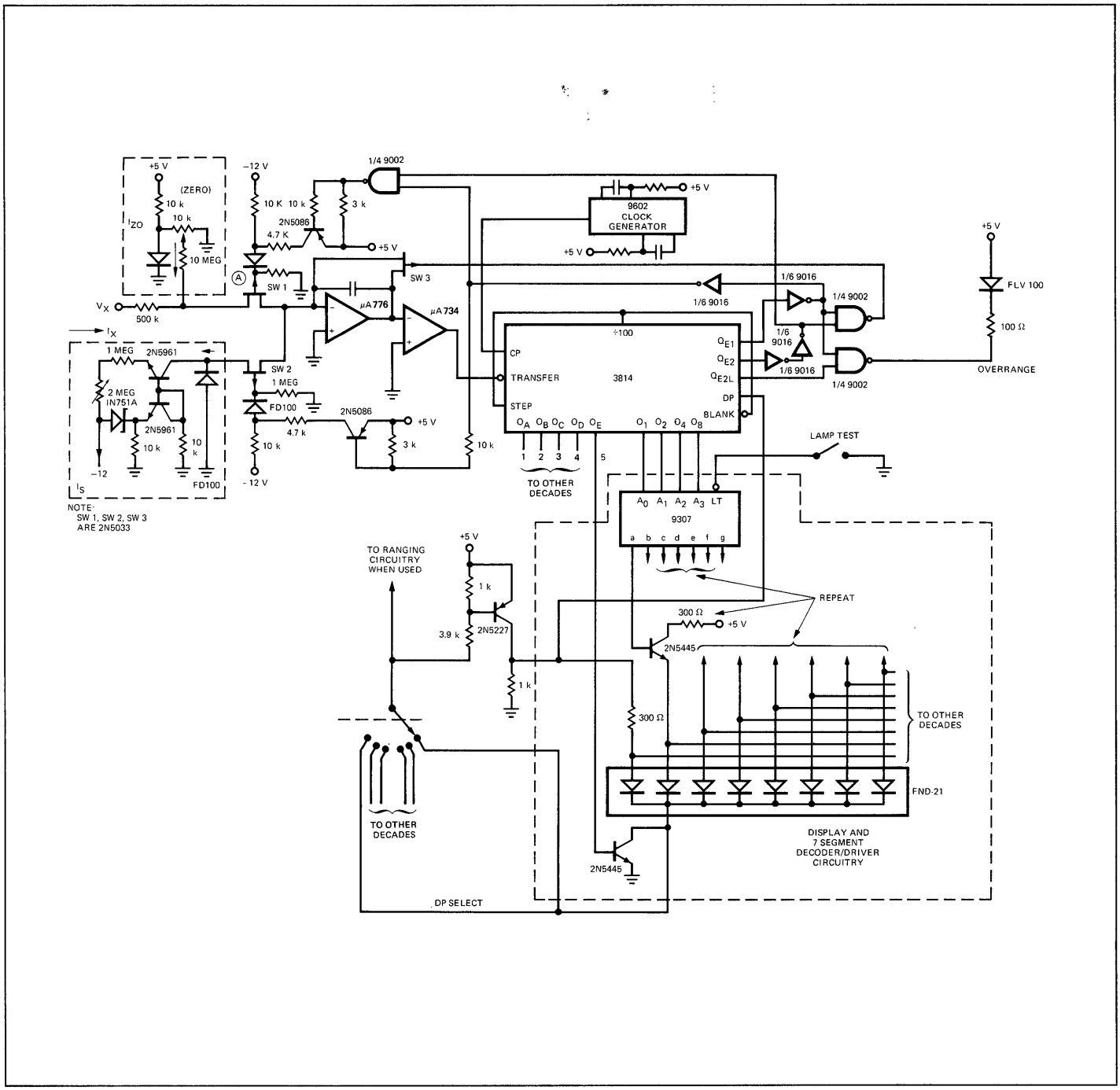


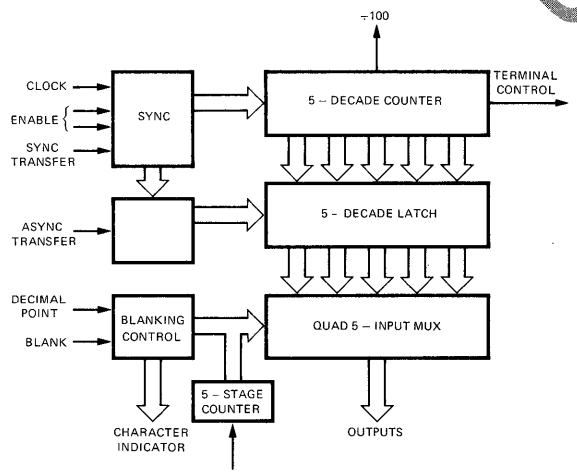
Fig. 13.

3815
5-DECADE COUNTER

GENERAL DESCRIPTION—The 3815 consists of five decades of clocked BCD counters. A master reset line asynchronously sets the counters to all zeros. The outputs of the counters are either synchronously or asynchronously transferred to latches. The latched state of each decade is multiplexed out by character with an indication of which character is being read out.

- **TRANSFERS IN EITHER SYNCHRONOUS OR ASYNCHRONOUS MODE WITH NO EXTERNAL GATING**
- **OUTPUTS MULTIPLEXED TO REDUCE PIN COUNT**
- **MASTER RESET**
- **LEADING ZERO BLANKING**
- **SILICON GATE TECHNOLOGY**
- **DTL/TTL COMPATIBLE INPUTS AND OUTPUTS**
- **24-LEAD DUAL IN-LINE PACKAGE**

FUNCTIONAL DIAGRAM

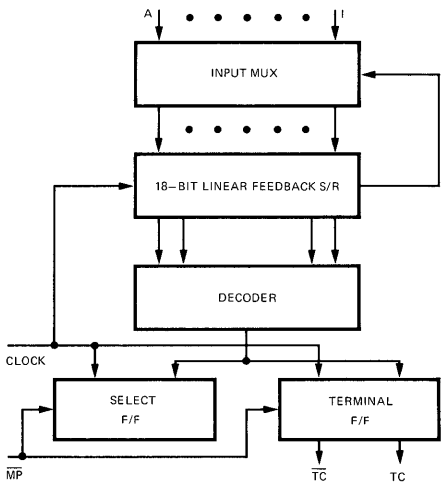


3816
18-BIT PROGRAMMABLE COUNTER

GENERAL DESCRIPTION – The 3816 is an 18-bit programmable counter capable of dividing by any modulo from 3 to 262,145. All logic driven inputs and DTL/TTL compatible.

- **STATIC TO 1MHz OPERATION**
- **FULL 18-BIT PROGRAMMABLE COUNTER IN 16-LEAD DUAL IN-LINE PACKAGE**
- **DTL/TTL COMPATIBLE INPUTS AND OUTPUTS**
- **SILICON GATE TECHNOLOGY**

FUNCTIONAL DIAGRAM



3100
5-INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3100 Dual 5-Input Gate is a MOS monolithic integrated circuit. This device can be used as a logic block in an all MOS system, or as a breadboarding gate in designing customer integrated circuits. Input protection is provided on all inputs.

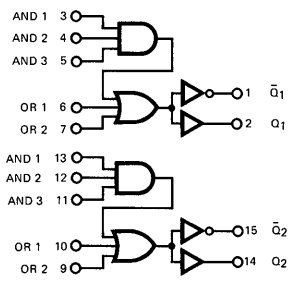
- **GATE PROTECTION**
- **INVERTED AND NON-INVERTED OUTPUT BUFFERS**
- **AND/OR, NAND/NOR CAPABILITY**

ABSOLUTE MAXIMUM RATINGS (Notes 2 & 3)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any Pin	+0.3 V
Negative Voltage on any Pin	−30 V

NOTES:
1. These ratings are limiting values above which serviceability may be impaired.
2. Voltage levels are with respect to GND Pin.

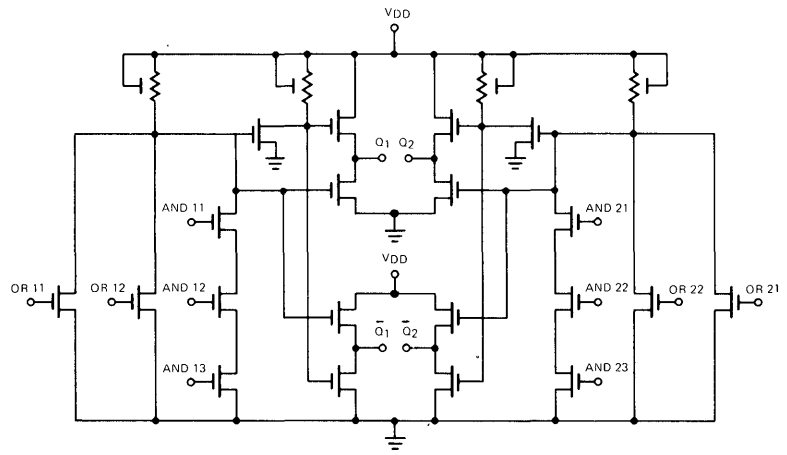
LOGIC SYMBOL



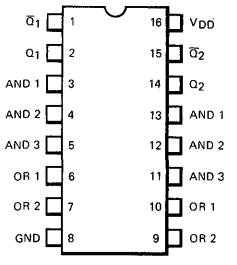
GND = Pin 8

V_{DD} = Pin 16

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



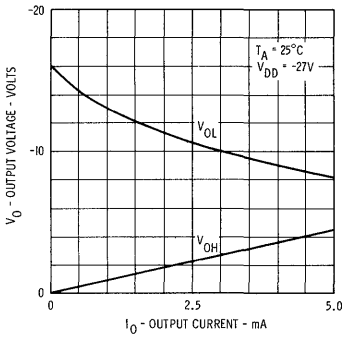
DC CHARACTERISTICS: V_{DD} = −27 ±2 V, Load = 10 MΩ, C_L = 10 pF, T_A = +25°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	−2.0		0	V	
V_{IL}	Input Voltage LOW			−9.0	V	
V_{OH}	Output Voltage HIGH	−1.0			V	
V_{OL}	Output Voltage LOW			−10	V	
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = −20 V
R_O	Output Impedance to Ground		1.0	1.5	kΩ	I_{OUT} = 100 μA
P_D	Power Dissipation		60		mW	

AC CHARACTERISTICS: V_{DD} = −27 ±2 V, Load = 10 MΩ, C_L = 10 pF, T_A = +25°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{PW}	Input Data Pulse Width	0.5			μs	
t_{D+} (Q)	Output Delay Time		0.4		μs	
t_{D-} (Q)			0.4		μs	
t_{D+} ($\overline{Q}$)			0.4		μs	
t_{D-} ($\overline{Q}$)			0.6		μs	
C_I	Input Capacitance		5.0		pF	V_{IN} = 0 V

TYPICAL OUTPUT CHARACTERISTIC



TRUTH TABLE

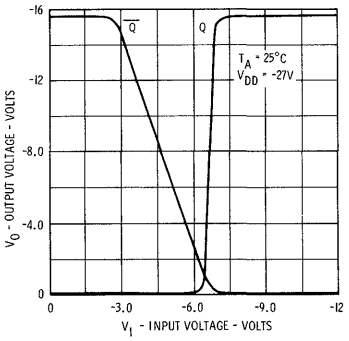
A OR$_1$	B OR$_2$	C AND$_1$	D AND$_2$	E AND$_3$	Q	$\overline{Q}$
0	0	0	0	0	0	1
0	0	0	0	1	0	1
0	0	0	1	0	0	1
0	0	0	1	1	0	1
0	0	1	0	0	0	1
0	0	1	0	1	0	1
0	0	1	1	0	0	1
0	0	1	1	1	1	0
0	1	X	X	X	1	0
1	0	X	X	X	1	0
1	1	X	X	X	1	0

Logic '1' is more negative than −9.0 V
Logic '0' is more positive than −2.0 V and ≤0 V
X is either '1' or '0'

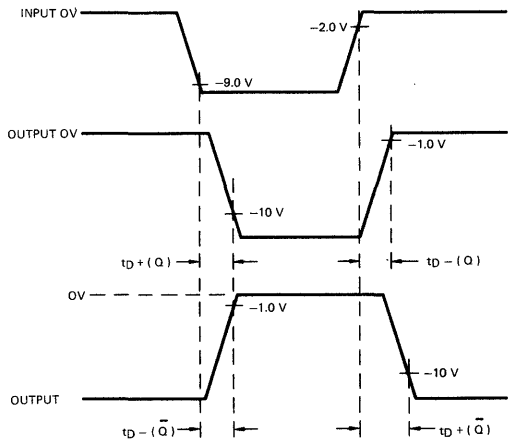
BOOLEAN FUNCTION: $Q = \overline{A + B + C \cdot D \cdot E}$

$\overline{Q} = A + B + C \cdot D \cdot E$

TYPICAL TRANSFER CHARACTERISTICS



TYPICAL PROPAGATION DELAY



3101

DUAL JK FLIP-FLOP

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3101 Dual JK Flip-Flop is a MOS monolithic integrated circuit utilizing P-channel enhancement technology. This device can be used as a logic block in an all MOS system, or as a breadboarding flip-flop in designing custom integrated circuits. Input protection is provided on all inputs.

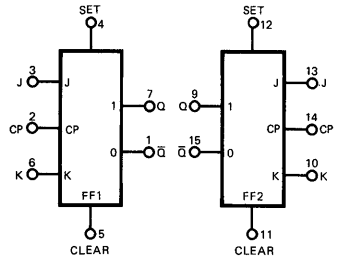
- **INPUT PROTECTION**
- **BUFFERED OUTPUTS**
- **ASYNCHRONOUS SET AND CLEAR**
- **SEPARATE CLOCK LINES**

ABSOLUTE MAXIMUM RATINGS (Notes 1 & 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any Pin	+0.3 V
Negative Voltage on any Input Pin	−30 V

NOTES:
1. These ratings are limiting values above which serviceability may be impaired.
2. Voltage levels are with respect to the GND Pin.

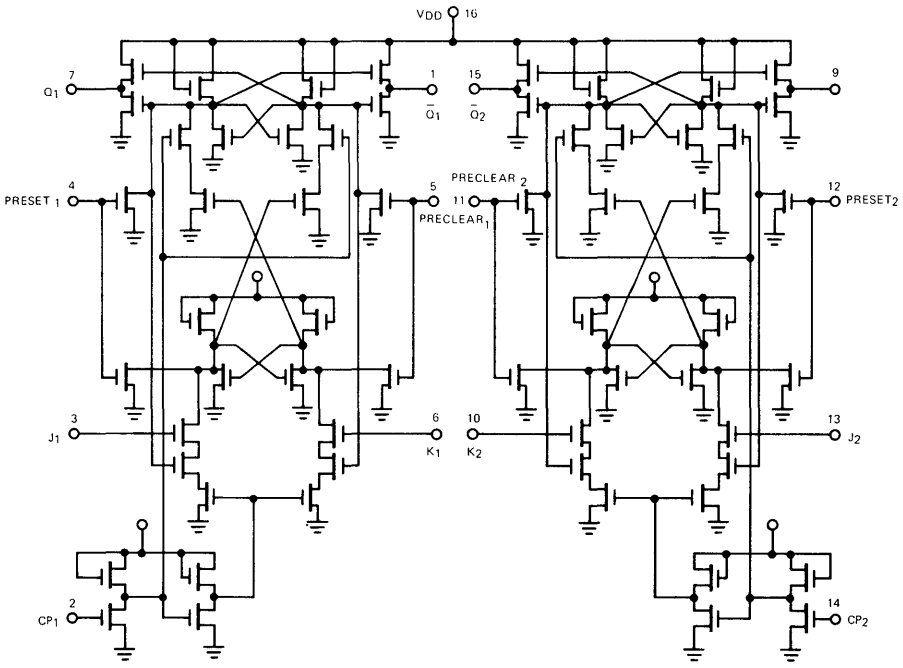
LOGIC SYMBOL



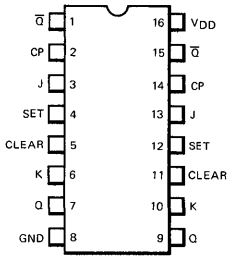
GND = Pin 8

V_{DD} = Pin 16

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



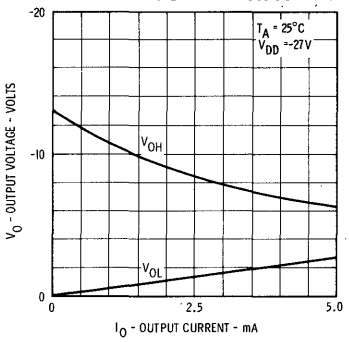
DC CHARACTERISTICS: $V_{DD} = -27 \pm 2$ V, $T_A = 25°C$.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	−2.0		0	V	
V_{IL}	Input Voltage LOW			−9.0	V	
$V_{\phi L}$	Clock Input Voltage LOW			−9.0	V	
V_{OH}	Output Voltage HIGH	−1.0			V	
V_{OL}	Output Voltage LOW			−10.0	V	
I_{LI}	Input Leakage Current			1.0	μA	$V_{IN} = -20$ V
R_O	Output Impedance to Ground			1.0	kΩ	
P_D	Power Dissipation		75		mW	

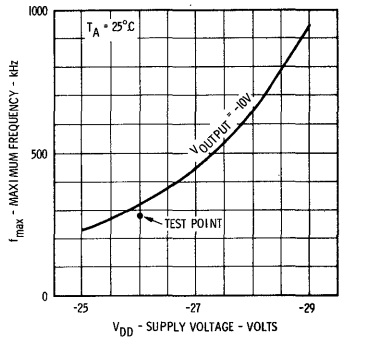
AC CHARACTERISTICS: $V_{DD} = -27 \pm 2$ V, $T_A = 25°C$.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Clock Frequency	dc		250	kHz	$V_{DD} = -26$ V
$t_{PW\phi}$	Clock Pulse Width	1.0			μs	
t_{PWD}	Input Data Pulse Width	1.0			μs	
t_S	Set Up Time		0.5		μs	
t_H	Hold Time		0.5		μs	
t_{D+}	Delay Time		1.0		μs	
t_{D-}	Delay Time		0.5		μs	
C_I	Input Capacitance		5.0		pF	$V_{IN} = 0$ V

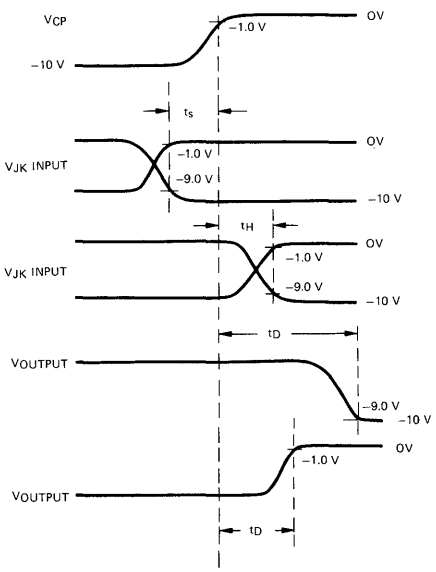
TYPICAL SWITCHING WAVEFORMS



MAXIMUM FREQUENCY VERSUS SUPPLY VOLTAGE



TYPICAL OUTPUT CHARACTERISTICS



TRUTH TABLE

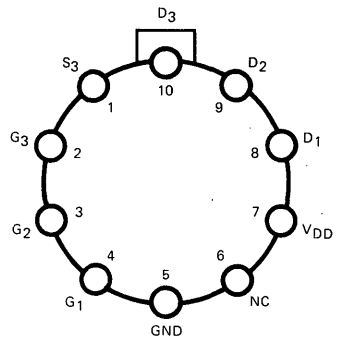
J t = n	K t = n	Q t = n + 1
0	0	X^n
0	1	0
1	0	1
1	1	X^n

Logic '1' is more negative than −9.0 V
Logic '0' is more positive than −2.0 V and ≤0
X^n is the output state at time n

3102
3-INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3102 is a MOS Monolithic 3-Input Gate integrated circuit. This device can be used as a vehicle in gaining familiarity with MOS integrated circuit logic versatility, as a building block in an all MOS system, or as a breadboarding gate in designing complex custom integrated circuits. Input protection is provided on all gate inputs.

CONNECTION DIAGRAM
(TOP VIEW)

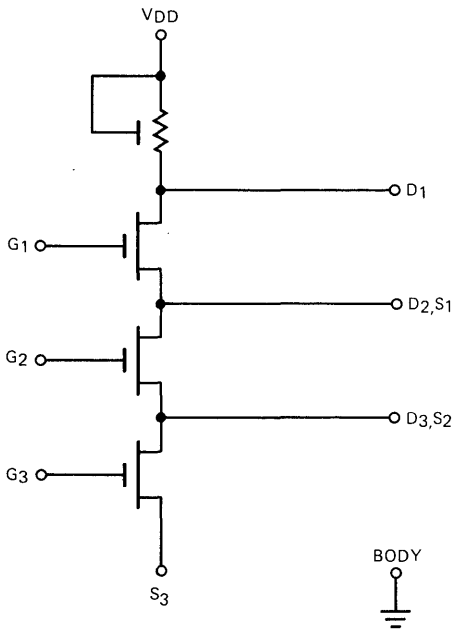


ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any Pin (V_{BODY} = 0)	+0.3 V
Negative Voltage on any Pin (V_{BODY} = 0)	−35 V
Power Dissipation at T_A = 25°C	⩽200 mW

NOTES:
1. These ratings are limiting values above which serviceability of the device may be impaired.

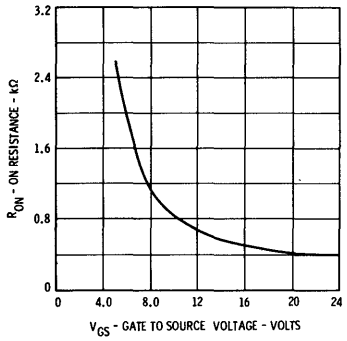
SCHEMATIC DIAGRAMS



DC CHARACTERISTICS: $V_{Body} = 0$; $T_A = 25°C$.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{TH}	Threshold Voltage	−5.5		−2.0	V	$V_D = V_G$, $I_D = -10\ \mu A$
I_{LI}	Input Leakage Current			1.0	μA	$V_{IN} = -25$ V
R_{Load}	Pull Up Resistance		140		kΩ	$V_{DD} = -27$ V ±2.0 V
R_{ON}	ON Resistance (See Fig. 1)		500		Ω	$V_{IN} = -20$ V
P_D	Power Dissipation		6.0		mW	$V_{DD} = -30$ V, $V_{IN} = -10$ V
C_I	Input Capacitance		4.0		pF	

Fig. 1
TYPICAL ON RESISTANCE



RESISTANCE CHARACTERISTIC

PARAMETERS	CONDITIONS	TYP.
R_{Load}	$V_{DD} = -25$ V $V_{D1} = 0$ V	140 kΩ
R_{ON}	$V_{GS} = -20$ V $V_{DS} \leqslant -1.0$ V $V_{D2} = 0$ V	500 Ω
R_{ON}	$V_{GS} = -9.0$ V $V_{DS} \leqslant -1.0$ V $V_{D2} = 0$ V	800 Ω

Fig. 2
TYPICAL DRAIN TO SOURCE CHARACTERISTICS

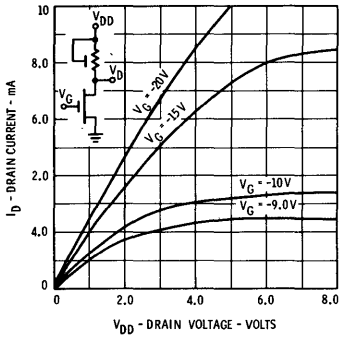
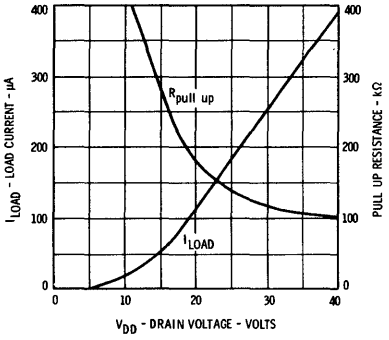
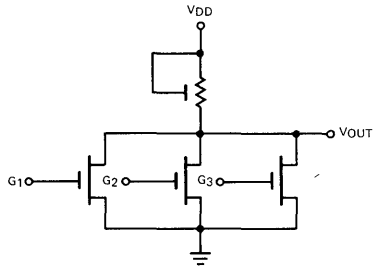


Fig. 3
TYPICAL PULL UP RESISTANCE



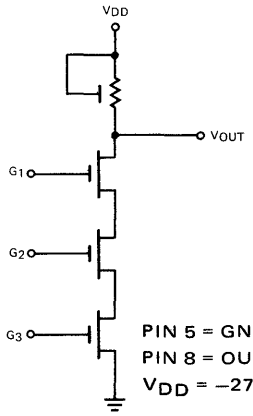
NAND GATE CONFIGURATION



PIN 8 = PIN 10 = V_{OUT}
PIN 1 = PIN 9 = GND
$V_{DD} = -27$ V ±2.0 V

	LOGIC LEVEL	VOLTAGE LEVEL MIN.	MAX.
V_{IH}	HIGH		−2.0 V
V_{IL}	LOW	−9.0 V	
V_{OH}	HIGH		−1.0 V
V_{OL}	LOW	−10 V	

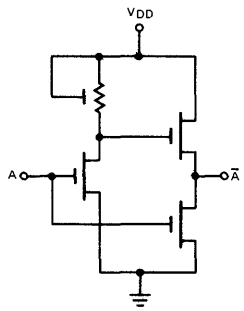
NOR GATE CONFIGURATION



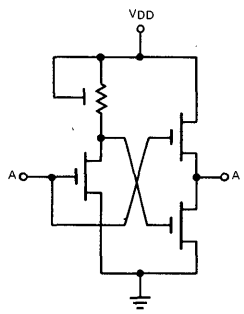
PIN 5 = GND
PIN 8 = OUTPUT
$V_{DD} = -27$ V ±2.0 V

APPLICATIONS – MOS logic will provide the versatility to build many different functions. The following circuits show how to build the functions using one or two 3102 packages.

INVERTING BUFFER

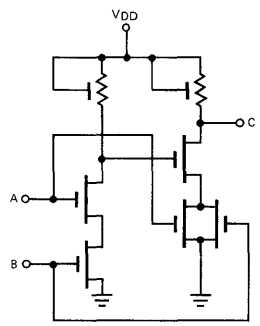


NON-INVERTING BUFFER



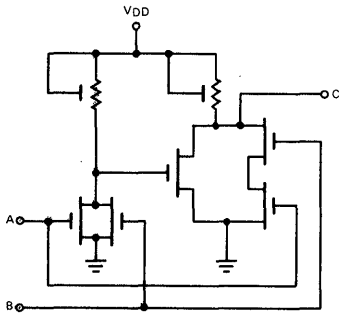
EXCLUSIVE NOR

$C = AB + \overline{A}\,\overline{B}$



EXCLUSIVE OR

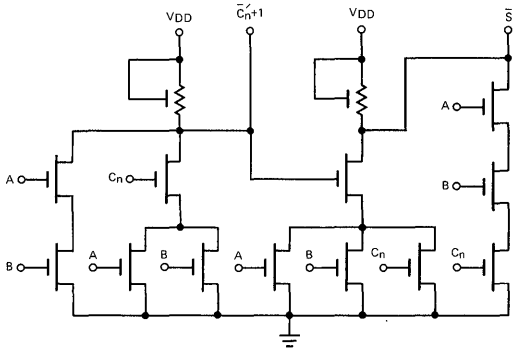
$C = \overline{A}B + \overline{B}A$



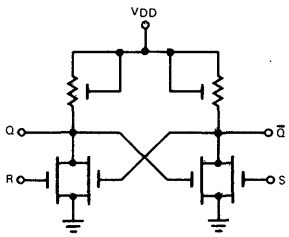
FULL ADDER

$C'_{n+1} = AB + C_n(A + B)$

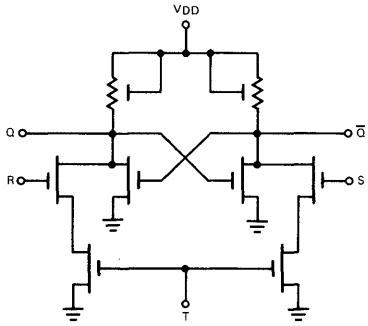
$S = (A+B+C_n)\,C'_{n+1} + ABC_n$



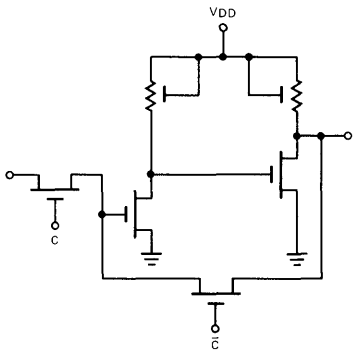
RS FLIP-FLOP



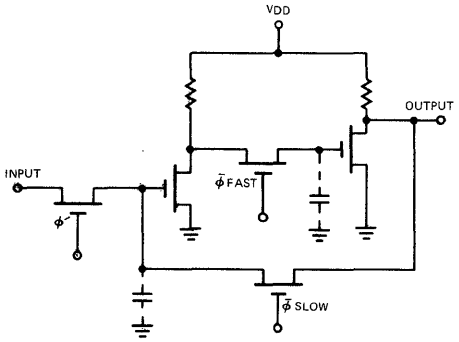
RST FLIP-FLOP



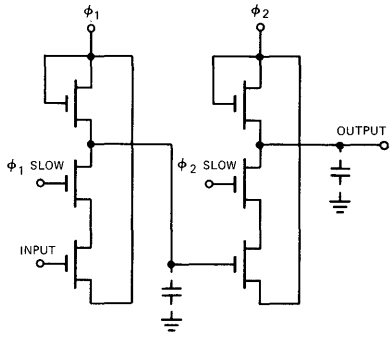
TYPE D FLIP-FLOP



STATIC (DC) SHIFT REGISTER BIT



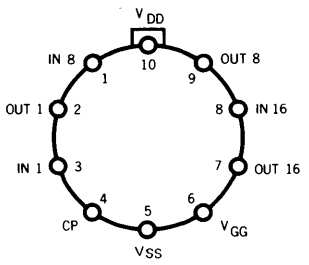
DYNAMIC 4-PHASE (4_ϕ) SHIFT REGISTER BIT



3300
25-BIT STATIC SHIFT REGISTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3300 is a 25-Bit Static Shift Register. It is a monolithic integrated circuit utilizing P-channel mode MOS technology. Input and output access is made available in 16, 8 and 1-bit increments. This device was designed for use in single phase clock sequential digital systems as a delay line or memory element.

CONNECTION DIAGRAM
(TOP VIEW)



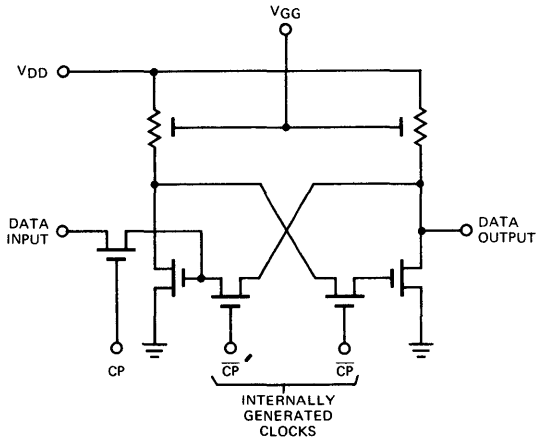
ABSOLUTE MAXIMUM RATINGS (See Note 1)

Storage Temperature (T_S)	−65°C to +150°C
Operating Temperature (T_A)	−55°C to +85°C
Power Dissipation at T_A = 25°C	200 mW
Voltage on Clock, Inputs and Supply Pins	−35 V to +0.3 V

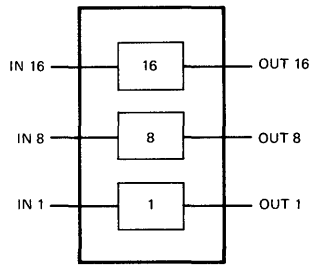
Note 1: These ratings are limiting values above which the serviceability of the device may be impaired.

SCHEMATIC DIAGRAM

(ONE BIT)



BLOCK DIAGRAM



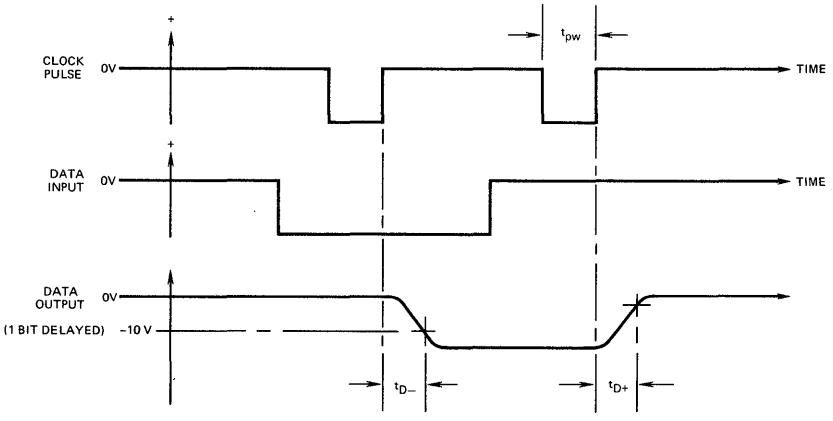
DC CHARACTERISTICS: V_{GG} = −27 ±2 V, V_{DD} = −13 ±2 V, V_{SS} = GND, T_A = 25°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	−2.0			V	
V_{IL}	Input Voltage LOW			−9.0	V	
$V_{\phi H}$	Clock Input Voltage HIGH	−2.0			V	
$V_{\phi L}$	Clock Input Voltage LOW			−9.0	V	
V_{OH}	Output Voltage HIGH	−1.0			V	I_{OUT} = −10 μA
V_{OL}	Output Voltage LOW			−10.0	V	I_{OUT} = −10 μA
I_{LI}	Input Leakage Current			−1.0	μA	V_{IN} = −20 V
$I_{L\phi}$	Clock Leakage Current			−1.0	μA	V_ϕ = −20 V
P_D	Power Dissipation		50		mW	V_ϕ = 0 V

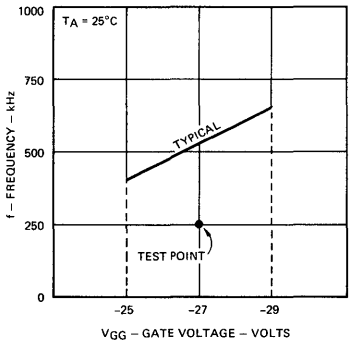
AC CHARACTERISTICS: V_{GG} = −27 ±2 V, V_{DD} = −13 ±2 V, V_{SS} = GND, T_A = 25°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Operating Frequency	0		250	kHz	V_{GG} = −27 V
$t_{PW\phi}$	Clock Pulse Width	1.0		100	μs	
t_r, t_f	Clock Rise and Fall Time			10	μs	
t_{D+}	Delay Time		1.2		μs	
t_{D-}	Delay Time		1.0		μs	
C_ϕ	Clock Capacitance		3.0		pF	V_ϕ = 0 V
C_I	Input Capacitance		2.5		pF	V_{IN} = 0 V

TIMING DIAGRAM



TYPICAL OPERATING FREQUENCY VERSUS GATE VOLTAGE



3326

TRIPLE 66-BIT DYNAMIC SHIFT REGISTER

FAIRCHILD MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 3326 contains three independent 2-Phase Dynamic Shift Registers of 66 bits each. It is a MOS P-channel enhancement mode integrated circuit. Each shift register has independent input and output but power supply and clock lines are common. The inputs are protected against static charge through diode protection. The 3326 is compatible with both MOS and bipolar integrated circuits (TTL and DTL). See Bipolar Interface configurations on following pages.

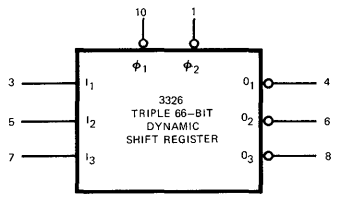
- **3 MHz OPERATION GUARANTEED**
- **BIPOLAR COMPATIBLITY**
- **INPUT OVERVOLTAGE PROTECTION**
- **10-LEAD TO-100 PACKAGE**

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired) (Note 1)

Drain Voltage (V_{DD})	−30 V to +0.3 V
Data and Clock Input Voltage	−30 V to +0.3 V
Data Output	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

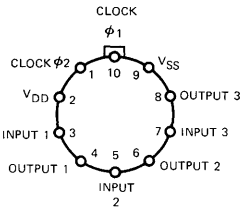
Note 1: All voltages are referenced with PIN 9 @ GND.

LOGIC SYMBOL

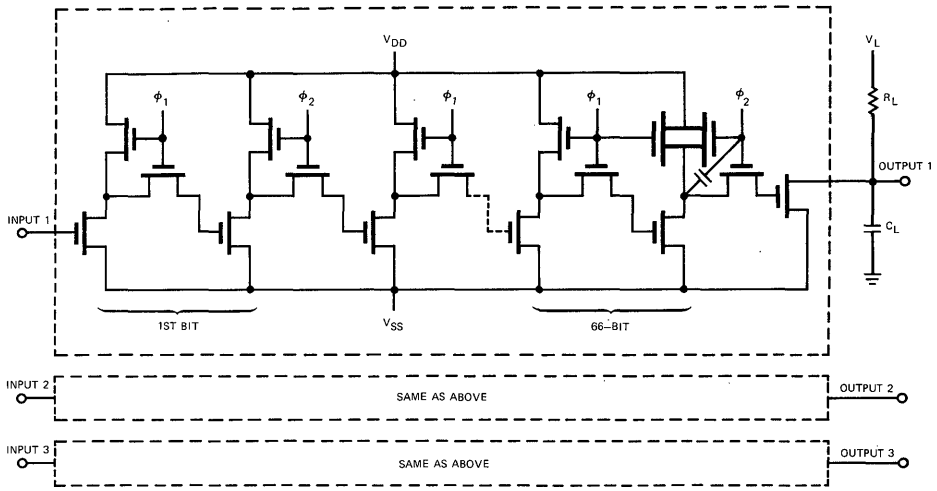


V_{SS} = PIN 9
V_{DD} = PIN 2

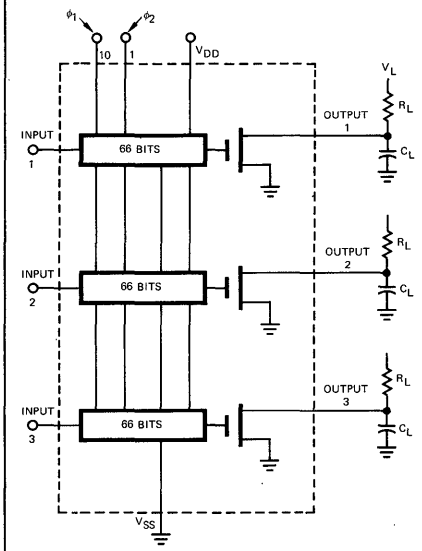
CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



BLOCK DIAGRAM



Each output device requires an external pull up resistor R_L and power supply V_L.

FUNCTIONAL DESCRIPTION – Each of the three shift register outputs is open drain. The output is delayed 66-bit times from the input and is inverted. The shift registers can be cascaded but each output must be connected to an external power supply through a pull up resistor. Data is entering the shift register when ϕ_1 goes LOW. Data is appearing at the output when ϕ_2 goes LOW.

DC CHARACTERISTICS: V_{DD} = –13 V ±10%, V_{SS} = GND, Clock Amplitude = –24 V to –27 V
R_L = 8kΩ ±10%, V_L = –13 V ±10%, C_L = 20 pF, T_A = 25°C.

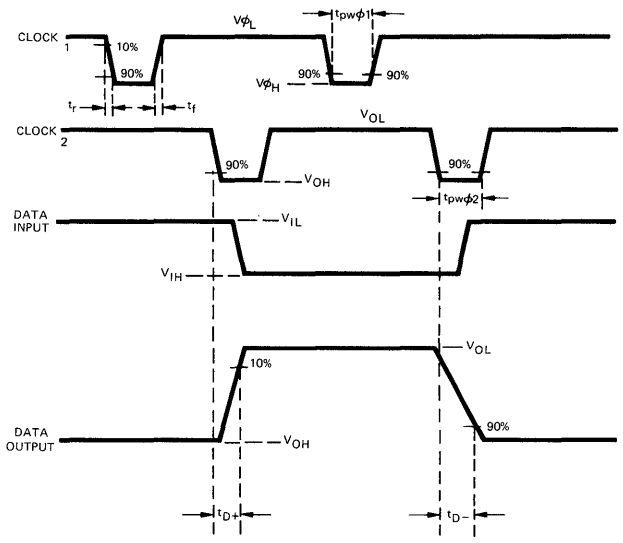
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	–3.0		0	V	
V_{IL}	Input Voltage LOW			–9.0	V	
$V_{\phi H}$	Clock Voltage HIGH	–2.0		0	V	
$V_{\phi L}$	Clock Voltage LOW	–27		–24	V	
V_{OH}	Output Voltage HIGH	–2.0	–1.2		V	
V_{OL}	Output Voltage LOW	V_L	–12.5		V	
$I_{L\phi}$	Clock Leakage Current			10	μA	at –27 V
I_{LI}	Input Leakage Current			0.5	μA	at –13 V
I_{LO}	Output Leakage Current			0.5	μA	at –13 V
I_{DD}	V_{DD} Current		8.0	14	mA	V_{DD} = –13 V Clock Amplitude = –27 V Clock Duty Cycle = 20%
P_D	Power Dissipation		105	180	mW	

AC CHARACTERISTICS: V_{DD} = –13 V ±10%, V_{SS} = GND, Clock Voltages = –24 V to –27 V
R_L = 8 kΩ ±10%, C_L = 20 pF, V_L = –13 V ±10%, T_A = 25°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Clock Repetition Rate	0.001		3.0	MHz	
t_{PW}	Clock Pulse Width	0.15		50	μs	
t_r, t_f	Rise and Fall Times		100		ns	
t_{D+}	Output Delay Time		50		ns	See Note 3
t_{D-}			200		ns	
C_ϕ	Clock Capacitance		35	50	pF	
C_I	Input Capacitance		3.5	5.0	pF	

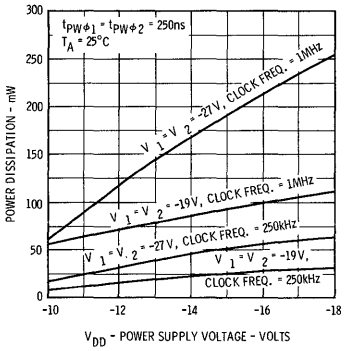
Note 3: Output delay time t_{D-} is essentially determined by the output load time constant R_L C_L.

TYPICAL WAVEFORMS

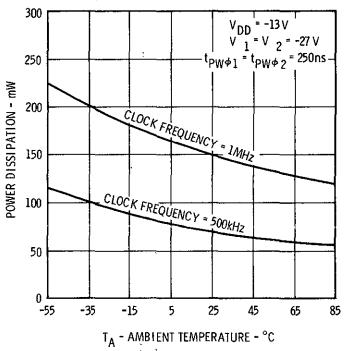


TYPICAL ELECTRICAL CHARACTERISTICS

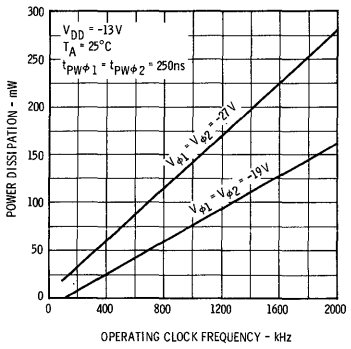
POWER DISSIPATION VERSUS POWER SUPPLY VOLTAGE



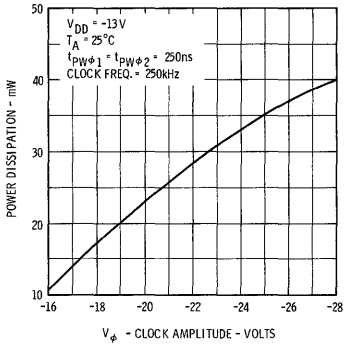
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



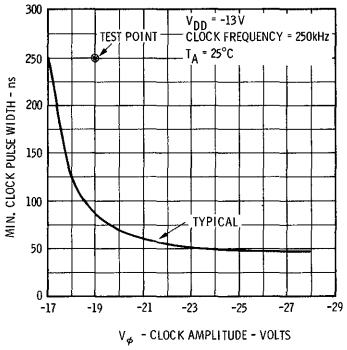
POWER DISSIPATION VERSUS OPERATING CLOCK FREQUENCY



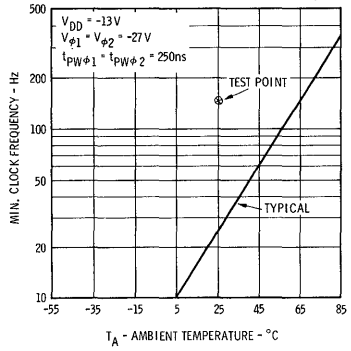
POWER DISSIPATION VERSUS CLOCK AMPLITUDE



MINIMUM CLOCK PULSE WIDTH VERSUS CLOCK AMPLITUDE



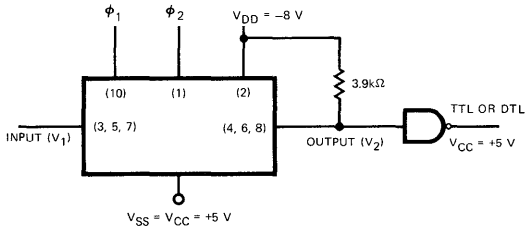
MINIMUM CLOCK FREQUENCY VERSUS TEMPERATURE



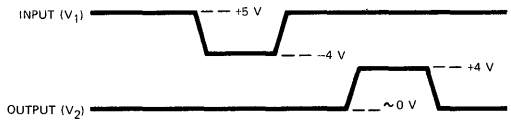
BIPOLAR INTERFACE

(A). OUTPUT COMPATIBILITY

The 3326 can drive bipolar integrated circuits (TTL, DTL, etc.) directly without using additional interface circuitry. One scheme is shown below:

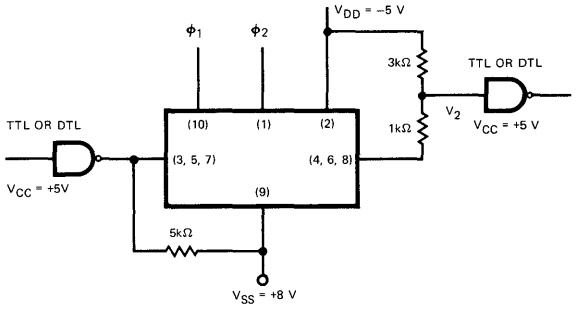


Clock amplitude $V_\phi = +5$ V to -19 V.
Clock pulse width $t_{PW} \geq 150$ ns.

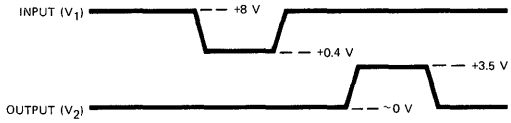


(B). INPUT/OUTPUT BIPOLAR COMPATIBILITY

For both input and output compatibility with bipolar integrated circuits (TTL, DTL) the following circuit scheme is suggested:



Clock amplitude $V_\phi = +8$ V to -16 V.
Clock pulse width $t_{PW} \geq 150$ ns.



3501

1024-BIT STATIC READ-ONLY MEMORY

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3501 is a 1024-Bit Read Only Memory in a 128-word by 8-bit format. It is a MOS monolithic integrated circuit utilizing P-channel enhancement mode technology. The fixed program memory is specified by the customer and customized by modifying one mask in the fabrication process. This results in a fast turn around, low cost custom memory.

- **CHIP SELECT**
- **ACCESS TIME – 3.6 μs**
- **STATIC OPERATION**
- **LOW POWER CONSUMPTION – 150 mW TYP.**
- **BIPOLAR COMPATIBLE OUTPUTS**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

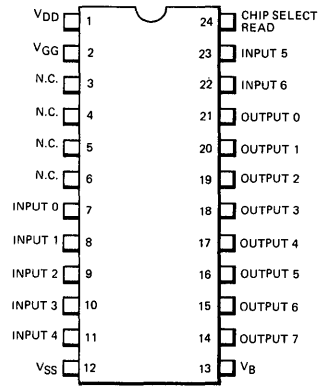
All Voltages and Data Input Lines		−30 V to +0.3 V
Power Dissipation		250 mW
Storage Temperature		−55°C to +150°C
Operating Temperature	(3501XDL)	−55°C to +85°C
	(3501XDC)	0°C to +70°C

Note: X = ROM code.

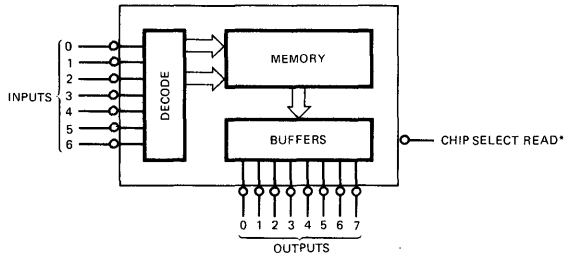
APPLICATIONS

Micro Programming
Code Conversion
Table Lookup
Control Logic

CONNECTION DIAGRAM
(TOP VIEW)



LOGIC DIAGRAM (MIL STD 806B)



*When chip select read is at ground the outputs are floating.

DC CHARACTERISTICS: $V_{DD} = -13\ V \pm 1\ V$, $V_{GG} = -27\ V$, $V_{SS} = 0\ V$, $V_B = -27\ V \pm 2\ V$, $T_A = 0°C$ to $70°C$ (Note 8)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	−2.0		0	V	
V_{IL}	Input Voltage LOW			−9.0	V	
V_{OH}	Output Voltage HIGH	−1.0		0	V	$I_L = -10\ \mu A$
V_{OL}	Output Voltage LOW			−10.0	V	$I_L = +10\ \mu A$
I_{OH}	Output Current HIGH	.15	.24		μA	$V_{OUT} = -1.0\ V$ (forced), Note 7
I_{OL}	Output Current LOW	.30	.85		μA	$V_{OUT} = -10\ V$ (forced), Note 7
I_{LI}	Input Leakage Current			1.0	μA	$V_{IN} = -15\ V$, Note 6
I_{LO}	Output Leakage Current			−1.0	μA	$V_{OUT} = -15\ V$
I_{DD}	V_{DD} Current			6.5	mA	$V_{DD} = -14\ V$, $V_{GG} = -29\ V$
I_{GG}	V_{GG} Current			4.0	mA	Note 2
P_D	Power Dissipation		150	215	mW	Note 1,2

AC CHARACTERISTICS: $V_{DD} = -13\ V \pm 1\ V$, $V_{GG} = -27\ V$, $V_{SS} = 0\ V$, $V_B = -27\ V \pm 2\ V$, $T_A = 0°C$ to $70°C$ (Note 8)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_E	Output Enable Time		1.9	3.6	μs	$R_L = 1\ M\Omega$, $C_L = 10\ pF$
$t_{\overline{E}}$	Output Disable Time		2.9	4.5	μs	Note 2, 4, Fig. 1
t_{D+}	Access Time		3.6	4.25	μs	Note 2, 4, Fig. 1
t_{D-}	Access Time		2.3	3.1	μs	$R_L = 1\ M\Omega$, $C_L = 10\ pF$
C_I	Input Capacitance		7.0		pF	Note 5
C_O	Output Capacitance		5.0		pF	Note 5

NOTES:
(1) Exclusive of I_B (load current)
(2) $T_A = +25°C$
(3) Fairchild will furnish complete test spec's upon request
(4) Sample tested
(5) Guaranteed by design
(6) Address and chip select inputs, all pins grounded except the one under test
(7) $V_{DD} = -12\ V$, $V_{GG} = -25\ V$ (worst case condition of measurement)
(8) $-55°C$ to $+85°C$ and $-55°C$ to $+125°C$ operation, performance, parameter limits etc., furnished upon request.

GLOSSARY OF TERMS

V_{GG} The most negative voltage applied to the device
V_{DD} An intermediate negative voltage applied to the device
V_B The voltage applied to the output buffers
V_{SS} The most positive voltage, applied to the device (substrate)

ACCESS TIME:
The delay time from the −9 V level (or the −2 V level respectively) of the input square wave to a valid output level reflecting the new logic state (see timing diagram) under standard load conditions ($R_L = 1\ M\Omega$, $C_L = 10\ pF$).

CHIP SELECT TIME:
The delay time from a valid chip select input to a valid wired-OR output of the selected device under standard load conditions.

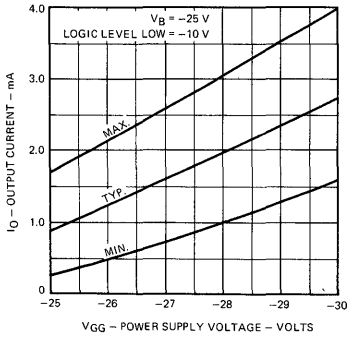
CUSTOM BIT PATTERN ORDERING PROCEDURE

To order a custom bit pattern matrix

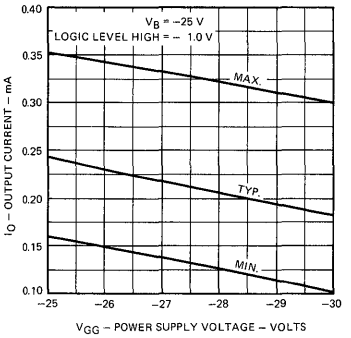
1. Customer will be furnished a Read Only Memory Coding Form from Fairchild representative. This form, when completed, will list each input and output bit pattern. From this information Fairchild will generate a truth table print out for verification, a custom mask, and a final test program for each custom device, or
2. Customer will provide Fairchild with a truth table in the Coding Form format, or
3. Customer will provide Fairchild with prepunched computer cards in the coding form format.

ELECTRICAL CHARACTERISTICS

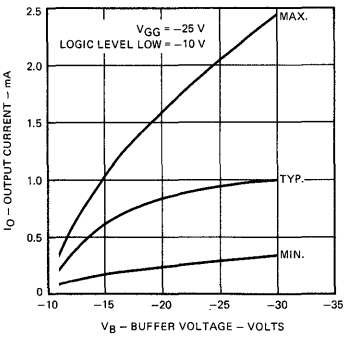
OUTPUT CURRENT VERSUS POWER SUPPLY VOLTAGE



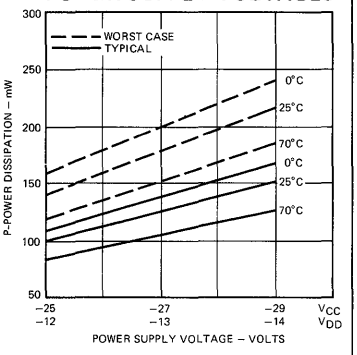
OUTPUT CURRENT VERSUS POWER SUPPLY VOLTAGE



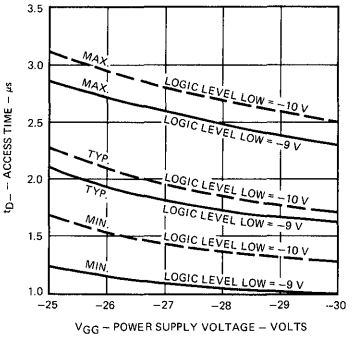
OUTPUT CURRENT VERSUS BUFFER VOLTAGE



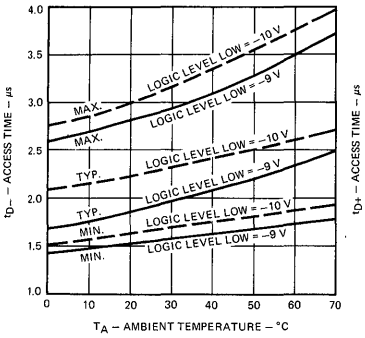
POWER DISSIPATION VERSUS POWER SUPPLY VOLTAGES



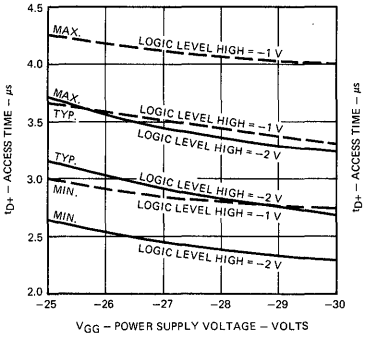
ACCESS TIME (t_{D-}) VERSUS POWER SUPPLY VOLTAGE



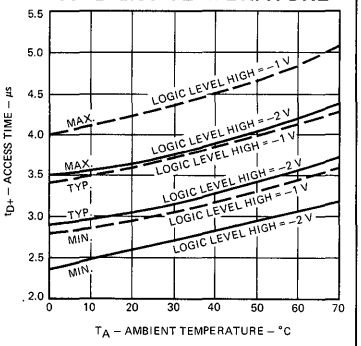
ACCESS TIME (t_{D-}) VERSUS AMBIENT TEMPERATURE



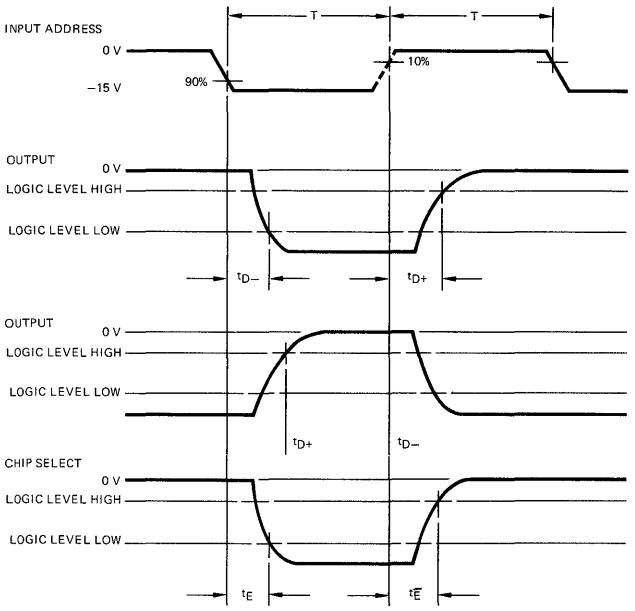
ACCESS TIME (t_{D+}) VERSUS POWER SUPPLY VOLTAGE



ACCESS TIME (t_{D+}) VERSUS AMBIENT TEMPERATURE



TYPICAL TIMING DIAGRAM



T = 8-10 µs
Rise and fall time ~ 50 ns

Standard load R_L = 1 MΩ
C_L = 10 pF

Fig. 1 — ACCESS AND CHIP SELECT TIMES

NOTE: The logic HIGH and LOW levels may be taken to be (−1 V, −10 V) or (−2 V, −9 V) respectively. Both versions are reflected in the graphs. Guaranteed limits are at −1 V and −10 V.

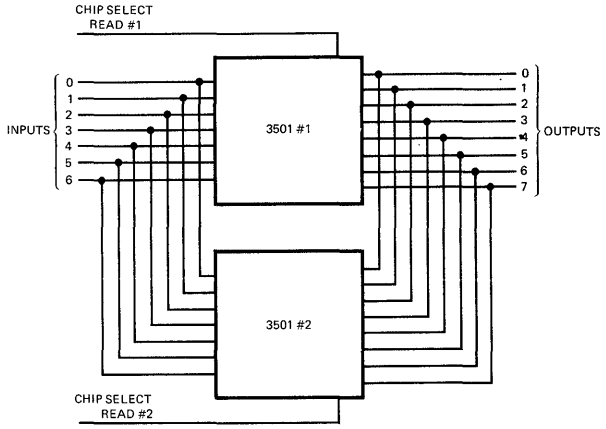


Fig. 2 — TYPICAL EXPANDED MEMORY
(CONNECTION FOR 256-WORDS BY 8-BITS)

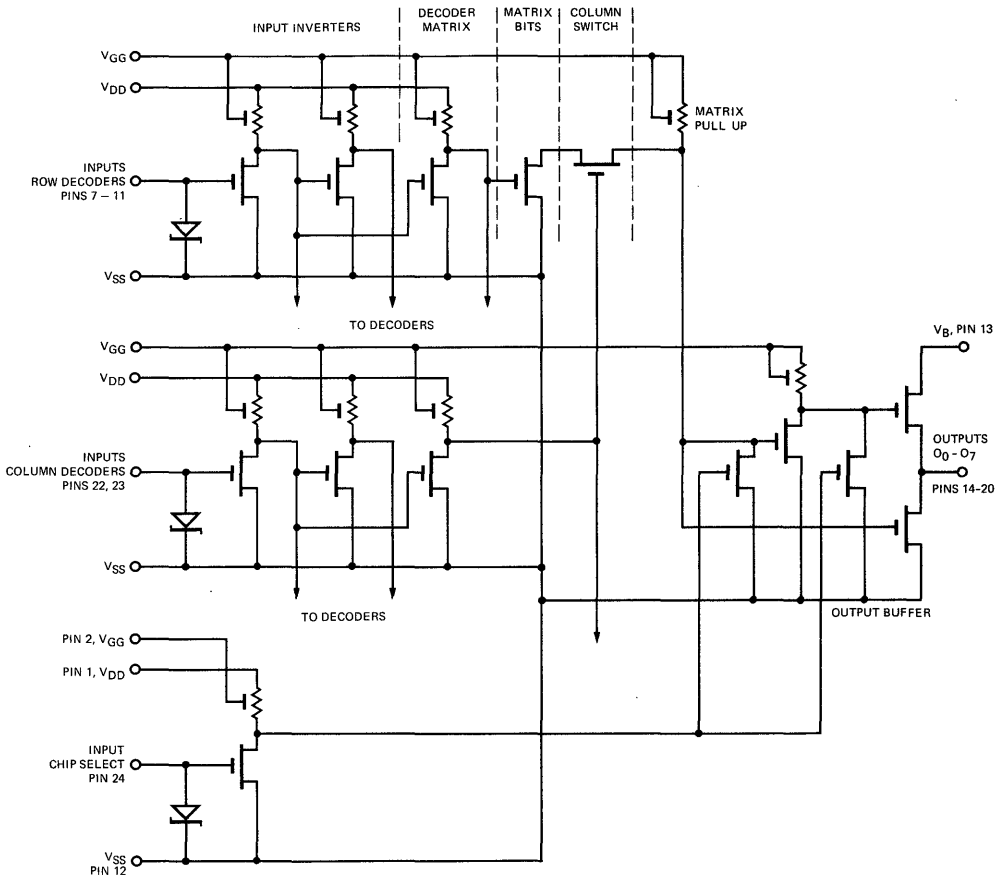


Fig. 3 — REPRESENTATIVE SCHEMATIC DIAGRAM

3700

MOS MONOLITHIC 4-CHANNEL SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3700 is a 4-Channel Multiplex Switch with all channel blanking. It is a monolithic integrated circuit using P-channel enhancement mode MOS technology. Control logic has been included on the chip to make the 3700 NPN bipolar compatible. The DTL 9112 High Level Hex Inverter can be used to directly interface the 3700 with TTL logic levels. This device is intended for use in A/D Converters, Multiplexing, Analog or Digital Data Transmission Systems, and other airborne or ground instrumentation signal routing applications.

- **BIPOLAR COMPATIBLE INPUT LOGIC LEVELS**
- **HIGH ON/OFF RATIO**
- **ALL CHANNEL BLANKING CONTROL**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**

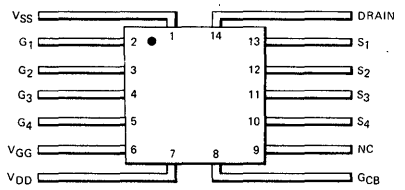
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature	−65°C to +150°C
Operating Temperature 3700XFM	−55°C to +125°C
Operating Temperature 3700XFC	0°C to + 70°C
Positive Voltage on Any Pin	+0.3 V
Negative Voltage on Digital and Analog Input pins	
Analog Output pins	−30 V
Negative Voltage on V_{DD} and V_{GG} pins	
37002	−50 V
37003	−35 V
Total Power Dissipation in package (T_A = 25°C)	200 mW

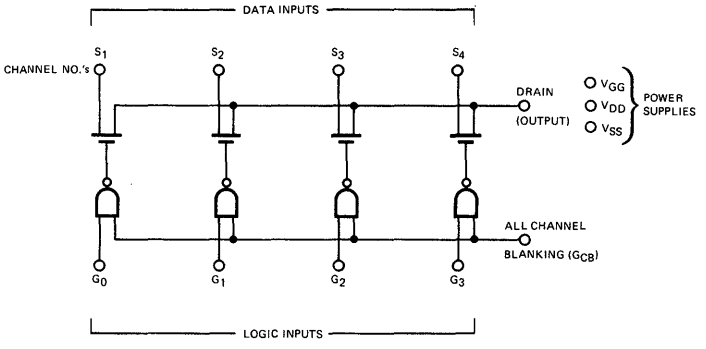
The 3700 is available for use in two signal ranges. (See electrical characteristics for supply voltage requirements.)

+5.0 to −5.0 volts signal applications, 37002
0 to +5.0 volts signal applications, 37003

CONNECTION DIAGRAM



LOGIC DIAGRAM



NOTES:

1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Voltage ratings are all referenced to pin 1 (V_{SS}).

DC CHARACTERISTICS:

FOR 37002: V_{OUT} = −5.0 V to +5.0 V, V_{DD} = −35 V ± 10%, V_{GG} = −35 V ± 10%, V_{SS} = +8.0 V ± 10%, T_A = 25°C unless otherwise specified.

FOR 37003: V_{OUT} = 0 V to +5.0 V, V_{DD} = −21 V ± 10%, V_{GG} = −21 V ± 10%, V_{SS} = +8.0 V ± 10%, T_A = 25°C unless otherwise specified.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS	
V_{IH}	Input Voltage HIGH	V_{SS}−1.5		V_{SS}	V		
V_{IL}	Input Voltage LOW	V_{SS}−30		V_{SS}−7.5	V		
I_{IL}	Data Input Leakage Current			1.5	nA	$V_{SS} - V_{IN}$ = 15 V	V_{GG} = Gnd
	3700XFM @ +125°C			200	nA	$V_{SS} - V_{IN}$ = 15 V	V_{GG} = Gnd
I_{LO}	Output Leakage Current						
	3700XFM			2.0	nA	$V_{SS} - V_{OUT}$ = +15 V	V_{GG} = Gnd
	3700XFC			10	nA	$V_{SS} - V_{OUT}$ = +15 V	V_{GG} = Gnd
	3700XFM @ +125°C			700	nA	$V_{SS} - V_{OUT}$ = +15 V	V_{GG} = Gnd
R_{ON}	Channel ON Resistance			270	Ω	$V_{OUT} = V_{SS}$	I_{OUT} = −100 μA
	37002FM			400	Ω	V_{OUT} = −5.0 V	I_{OUT} = −100 μA
	37003FM			400	Ω	V_{OUT} = 0 V	I_{OUT} = −100 μA
	37002FC			600	Ω	V_{OUT} = −5.0 V	I_{OUT} = −100 μA
	37003FC			600	Ω	V_{OUT} = 0 V	I_{OUT} = −100 μA
	37002FM @ +125°C			650	Ω	V_{OUT} = −5.0 V	I_{OUT} = −100 μA
	37003FM @ +125°C			650	Ω	V_{OUT} = 0 V	I_{OUT} = −100 μA
R_{OFF}	Channel OFF Resistance	1.5			GΩ	$V_{SS} - V_{OUT}$ = 15 V	V_{GG} = Gnd
	3700XFM @ +125°C	2.1			MΩ	$V_{SS} - V_{OUT}$ = 15 V	V_{GG} = Gnd

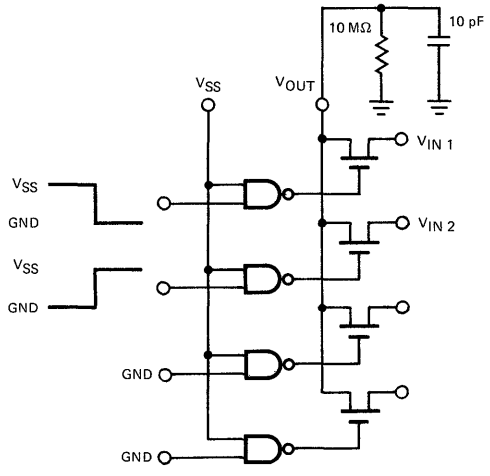
AC CHARACTERISTICS

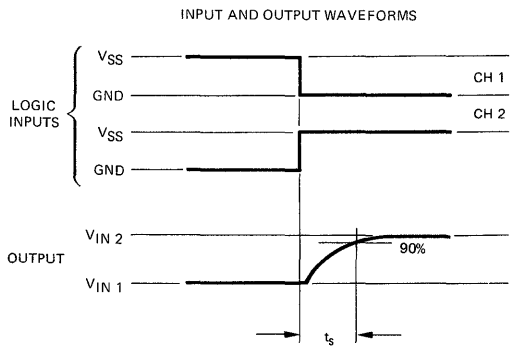
FOR 37002: V_{OUT} = −5.0 V to +5.0 V, V_{DD} = −35 V ± 10%, V_{GG} = −35 V ± 10%, V_{SS} = +8.0 V ± 10%, T_A = 25°C

FOR 37003: V_{OUT} = 0 V to +5.0 V, V_{DD} = −21 V ± 10%, V_{GG} = −21 V ± 10%, V_{SS} = +8.0 V ± 10%, T_A = 25°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS	
t_s	Channel Switching Time (see Fig. 1)		1.0		μs		
C_O	Output Capacitance		25		pF	$V_{SS} - V_{OUT}$ = 0 V	f = 1.0 MHz
C_D	Data Input Capacitance		9.0		pF	$V_{SS} - V_{IN}$ = 0 V	f = 1.0 MHz
C_L	Logic Input Capacitance		3.5		pF	$V_{SS} - V_G$ = 0 V	f = 1.0 MHz
C_B	Channel Blanking Input Capacitance		10		pF	$V_{SS} - V_G$ = 0 V	f = 1.0 MHz

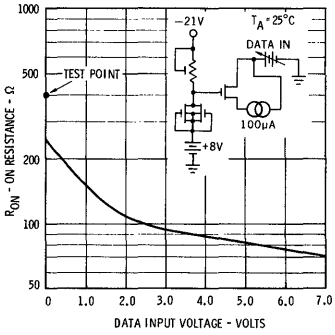
Fig. 1 SWITCHING TIME TEST CIRCUIT



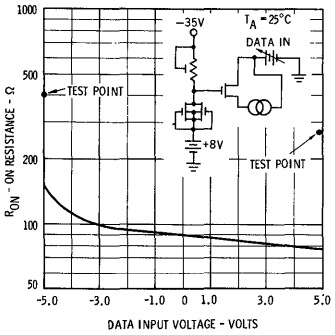


TYPICAL CHARACTERISTICS

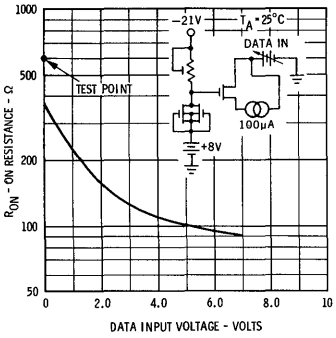
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (37003FM ONLY)



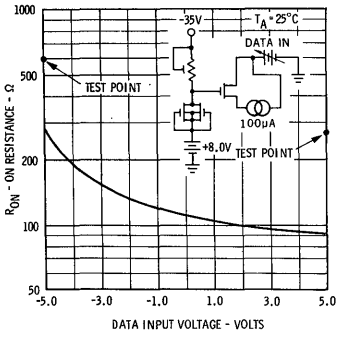
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (37002FM ONLY)



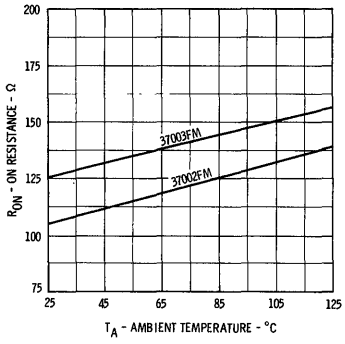
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (37003FC ONLY)



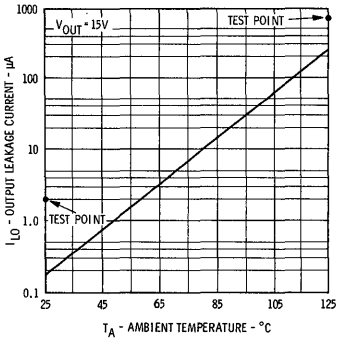
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (37002FC ONLY)



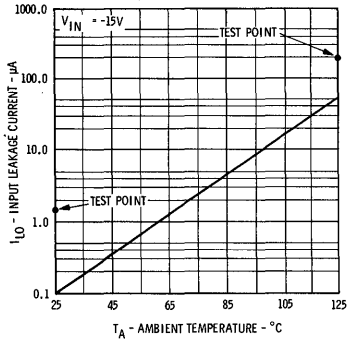
ON RESISTANCE VERSUS AMBIENT TEMPERATURE

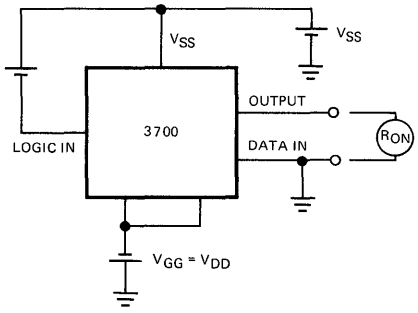


OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE (3700XFM)



DATA INPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE (3700XFM)





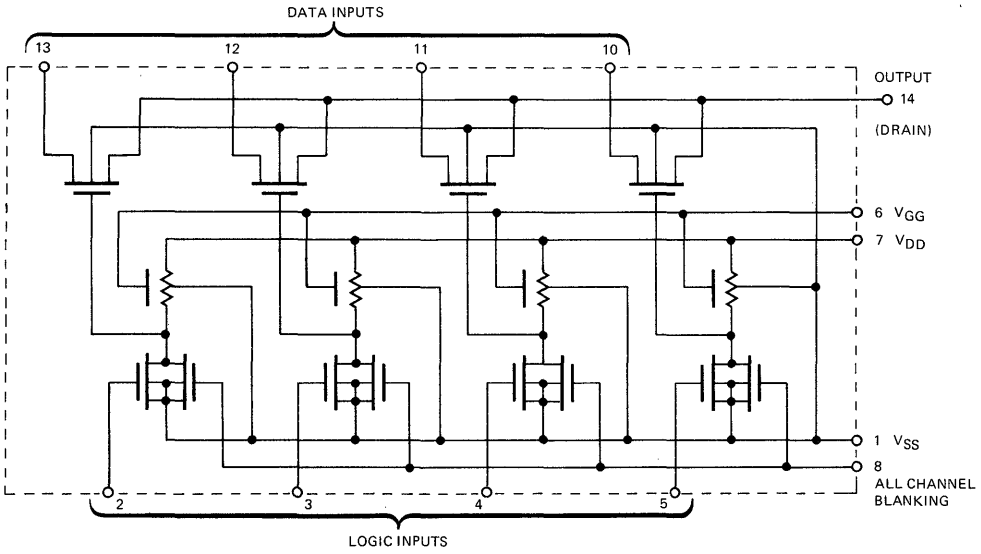
Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the ON resistance of the data channel accurately, the data input is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

The following sets of bias conditions are equivalent

	Condition 1	Condition 2	Condition 3
Data in	+5.0 V	−3.0 V	0 V
V_{SS}	+8.0 V	0 V	+3.0 V
$V_{DD} = V_{GG}$	−21 V	−29 V	−26 V
Logic in			
HIGH Level	+7.0 V	−1.0 V	+2.0 V
LOW Level	+1.5 V	−6.5 V	−3.5 V

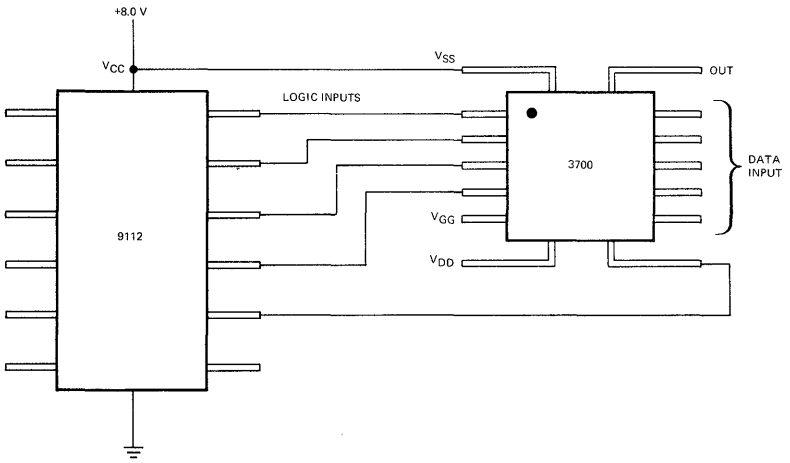
The logic input levels are V_{SS} - 30 V < LOW level < V_{SS} - 7.5 V to turn a data channel off
V_{SS} - 1.5 V < HIGH level < V_{SS} to turn a data channel on.

SCHEMATIC DIAGRAM



TYPICAL CIRCUIT CONFIGURATION

Typical circuit configuration showing the 3700 driven by bipolar DTL such as the Fairchild 9112.



3701
MOS MONOLITHIC 6-CHANNEL SWITCH
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3701 is a P-channel enhancement mode monolithic MOS 6-channel single output switch. This device can be used as a basic switching element for airborne or ground instrumentation, telemetry or other signal routing applications.

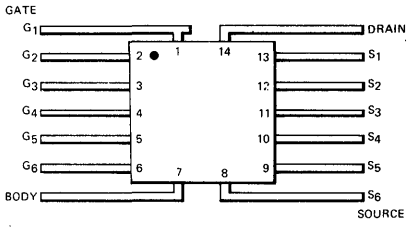
- **GATE PROTECTION**
- **ZERO OFFSET VOLTAGE**
- **LOW LEAKAGE CURRENT**
- **GUARANTEED OPERATIONS OVER –55°C TO +125°C**

ABSOLUTE MAXIMUM RATINGS (Note 1)

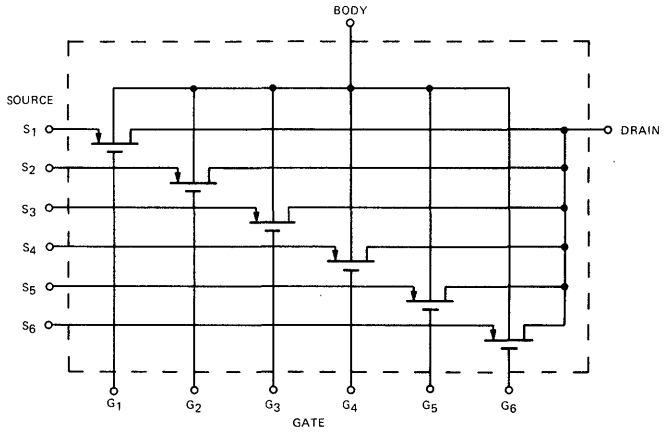
Storage Temperature		–65°C to +150°C
Operating Temperature	3701FM	–55°C to +125°C
	3701FC	0°C to + 70°C
Power Dissipation at +25°C		200 mW
Positive Voltage on any pin (V_{BODY} = 0)		+0.3 V
Negative Gate Voltage (V_{BODY} = 0)		–35 V
Negative Source or Drain Voltage (V_{BODY} = 0)		–30 V

NOTE:
1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



DC CHARACTERISTICS: $V_B = 0$ V, $T_A = 25°C$ unless otherwise specified

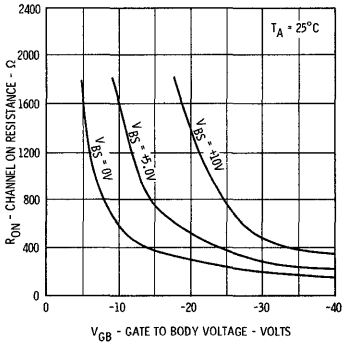
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(TH)}$	Gate Threshold Voltage	−5.5			V	$V_{SS} = 0$ V, $V_{GG} = V_{DD}$, $I_{DD} = -10$ μA
I_{LI}	Input Leakage Current					
	3701FM			1.0	nA	$V_{SS} = -20$ V, $V_{DD} = 0$ V, $V_{GG} = 0$ V
	3701FM (125°C)			150	nA	$V_{SS} = -20$ V, $V_{DD} = 0$ V, $V_{GG} = 0$ V
	3701FC			1.0	nA	$V_{SS} = -20$ V, $V_{DD} = 0$ V, $V_{GG} = 0$ V
I_{LO}	Output Leakage Current					
	3701FM			2.0	nA	$V_{DD} = -20$ V, $V_{SS} = V_{GG} = 0$ V
	3701FM (125°C)			200	nA	$V_{DD} = -20$ V, $V_{SS} = V_{GG} = 0$ V
	3701FC			5.0	nA	$V_{DD} = -20$ V, $V_{SS} = V_{GG} = 0$ V
I_{LG}	Gate Leakage Current			1.0	nA	$V_{GG} = -20$ V, $V_{DD} = V_{SS} = 0$ V
R_{ON}	Channel ON Resistance					
	3701FM		210	375	Ω	$V_{SS} = 0$ V, $V_{GG} = -30$ V, $I_{DD} = -100$ μA
	3701FM (125°C)		310	550	Ω	$V_{SS} = 0$ V, $V_{GG} = -30$ V, $I_{DD} = -100$ μA
	3701FC		300	500	Ω	$V_{SS} = 0$ V, $V_{GG} = -30$ V, $I_{DD} = -100$ μA
R_{OFF}	Channel OFF Resistance					
	3701FM	10	200		GΩ	$V_{DD} = -20$ V, $V_{GG} = 0$ V, $V_{SS} = 0$ V
	3701FM (125°C)	100	250		MΩ	$V_{DD} = -20$ V, $V_{GG} = 0$ V, $V_{SS} = 0$ V
	3701FC	4.0	200		GΩ	$V_{DD} = -20$ V, $V_{GG} = 0$ V, $V_{SS} = 0$ V

AC CHARACTERISTICS: $V_B = 0$ V, $T_A = 25°C$ unless otherwise specified

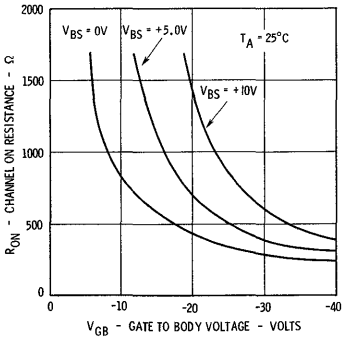
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
C_I	Input Capacitance		4.0		pF	$V_{SS} = 0$ V, $V_{DD} = 0$ V, $V_{GG} = 0$ V
C_I	Input Capacitance		3.0		pF	$V_{SS} = -10$ V, $V_{DD} = 0$ V, $V_{GG} = 0$ V
C_O	Output Capacitance		13		pF	$V_{SS} = 0$ V, $V_{DD} = 0$ V, $V_{GG} = 0$ V
C_O	Output Capacitance		7.0		pF	$V_{SS} = 0$ V, $V_{DD} = -10$ V, $V_{GG} = 0$ V
C_G	Gate Capacitance		4.0		pF	$V_{SS} = 0$ V, $V_{DD} = 0$ V, $V_{GG} = 0$ V
C_{GS} or C_{GD}	Gate-Source or Gate-Drain Capacitance		1.0		pF	$V_{SS} = 0$ V, $V_{DD} = 0$ V, $V_{GG} = 0$ V

TYPICAL CHANNEL ON RESISTANCE VERSUS GATE TO BODY VOLTAGE WITH BODY TO SOURCE VOLTAGE AS PARAMETER

3701FM

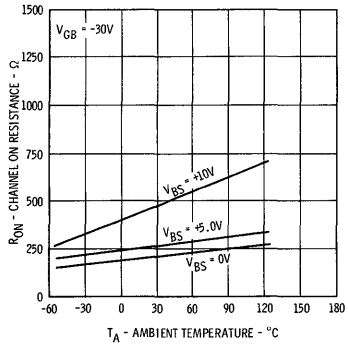


3701FC

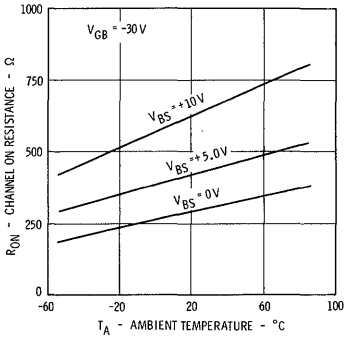


TYPICAL CHANNEL ON RESISTANCE VERSUS AMBIENT TEMPERATURE WITH BODY TO SOURCE VOLTAGE AS PARAMETER

3701FM



3701FC



3705

MOS MONOLITHIC 8-CHANNEL MULTIPLEX SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3705 is an 8-Channel Multiplex Switch with output enable control and one-of-eight decoder included on the chip. It is a monolithic integrated circuit utilizing P-channel enhancement mode MOS technology. The logic input lines of the 3705 are NPN bipolar compatible and can be used directly with DTL & TTL 5.0 V logic levels with no level shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

- **TTL COMPATIBLE INPUT LOGIC LEVELS**
- **ONE-OF-EIGHT DECODER ON CHIP**
- **HIGH ON/OFF RATIO**
- **OUTPUT ENABLE CONTROL**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**

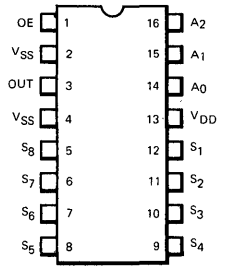
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any pin	+0.3 V
Negative Voltage on digital and analog input pins	−35 V
Negative Voltage on digital and analog output pins	−35 V
Negative Voltage on V_{DD} pin	−35 V
Total power dissipation in package (T_A = 25°C)	200 mW

The 3705 is available for use in two signal ranges
−5.0 to +5.0 V signal applications, 37052
0 to +5.0 V signal applications, 37053

NOTES:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.
(2) Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

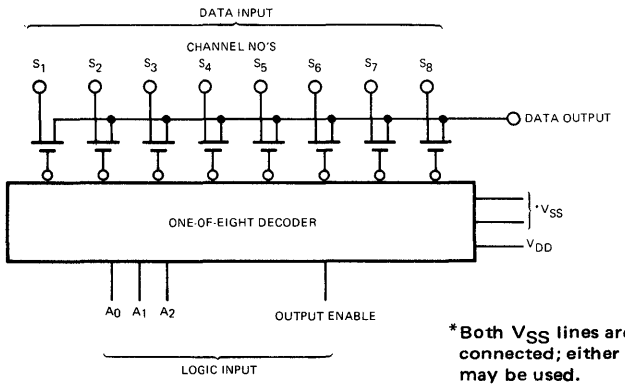
PIN CONFIGURATION
(16-Lead DIP)
TOP VIEW



TRUTH TABLE

LOGIC INPUTS				CHANNEL
A_0	A_1	A_2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

SYMBOLIC DIAGRAM
(MIL STD 806B)



*Both V_{SS} lines are internally connected; either one or both may be used.

DC CHARACTERISTICS

For 37052: V_{OUT} −5.0 V to +5.0 V, V_{DD} = −22 ±2 V, V_{SS} = +6 ±1 V, T_A = 25°C.
For 37053: V_{OUT} = 0 V to +5.0 V, V_{DD} = −22 ±2 V, V_{SS} = +6 ±1 V, T_A = 25°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS} −1.5		V_{SS}	V	
V_{IL}	Input Voltage LOW	V_{DD}		+0.2	V	
I_{LI}	Input Leakage Current			1.0	μA	$V_{SS} - V_{LOGIC\text{-}IN}$ = 15 V
I_{LO} (85°C)	Output Leakage Current			500	nA	$V_{SS} - V_{OUT}$ = 15 V
I_{LO}	Output Leakage Current			10	nA	$V_{SS} - V_{OUT}$ = 15 V
I_{LD}	Data Input Leakage Current					
	37052			3.0	nA	$V_{SS} - V_{IN}$ = 15 V
	37053			2.0	nA	$V_{SS} - V_{IN}$ = 10 V
R_{ON}	Data Channel ON Resistance					
	37052		250	400	Ω	V_{OUT} = −5.0 V, I_{OUT} = −100 μA
	37053		190	350	Ω	V_{OUT} = 0 V, I_{OUT} = −100 μA
R_{OFF}	Data Channel OFF Resistance	1.5			GΩ	$V_{SS} - V_{OUT}$ = 15 V
P_D	Power Dissipation		130	175	mW	V_{DD} = −31 V, V_{SS} = 0 V

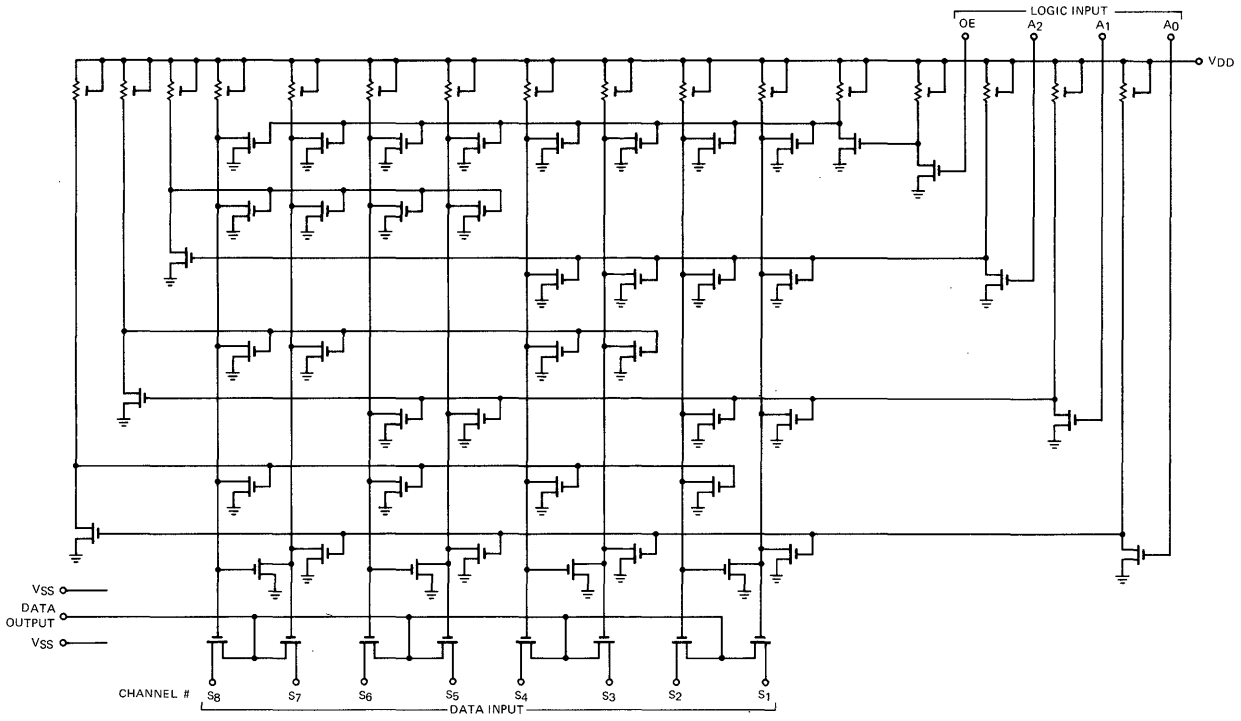
AC CHARACTERISTICS

For 37052: V_{OUT} = −5.0 V to +5.0 V, V_{DD} = −22 ±2 V, V_{SS} = +6 ±1 V, T_A = 25°C.
For 37053: V_{OUT} = 0 V to +5.0 V, V_{DD} = −22 ±2.V, V_{SS} = +6 ±1 V, T_A = 25°C.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_S	Channel Switching Time		1.0		μs	See Fig. 1
C_I	Data Input Capacitance		7.5		pF	$V_{SS} - V_{IN}$ = 0 V, f = 1.0 MHz
C_O	Output Capacitance		40		pF	$V_{SS} - V_{OUT}$ = 0 V, f = 1.0 MHz
C_L	Logic Input Capacitance		5.5		pF	$V_{SS} - V_{LOGIC\text{-}IN}$ = 0 V, f = 1.0 MHz

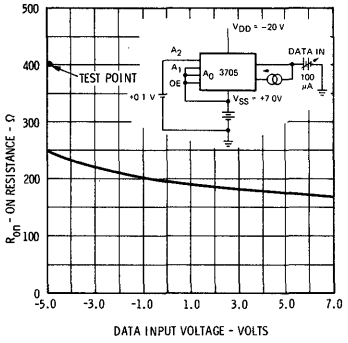
*When driven by TTL elements, avoid excessive dc loading of TTL elements to insure 3705 logic levels under maximum fan out conditions.

SCHEMATIC DIAGRAM

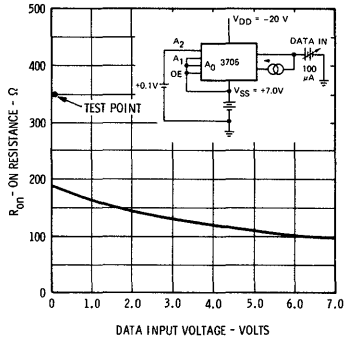


TYPICAL DEVICE CHARACTERISTICS

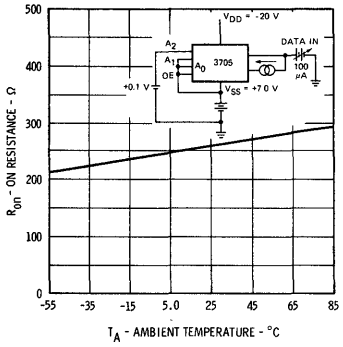
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (37052 ONLY)



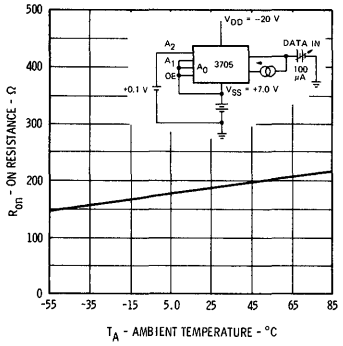
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (37053 ONLY)



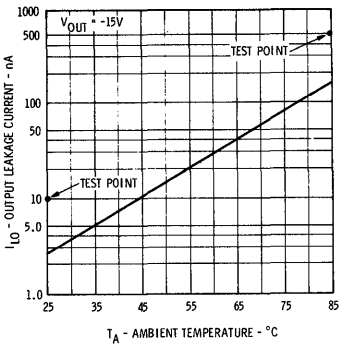
ON RESISTANCE VERSUS AMBIENT TEMPERATURE (37052 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (37053 ONLY)



OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT

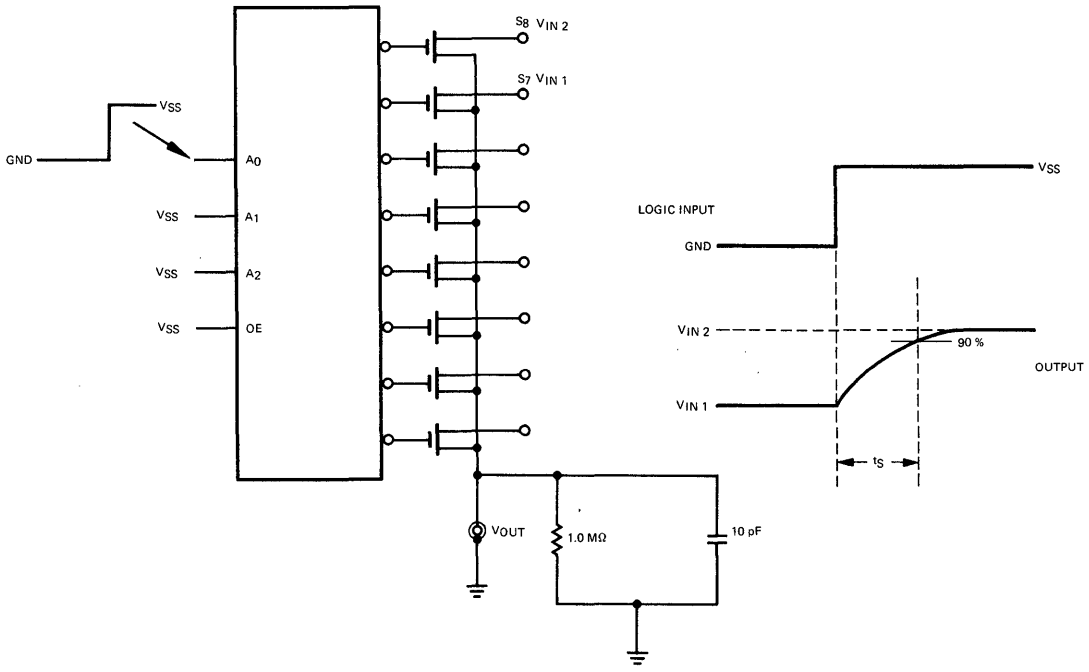
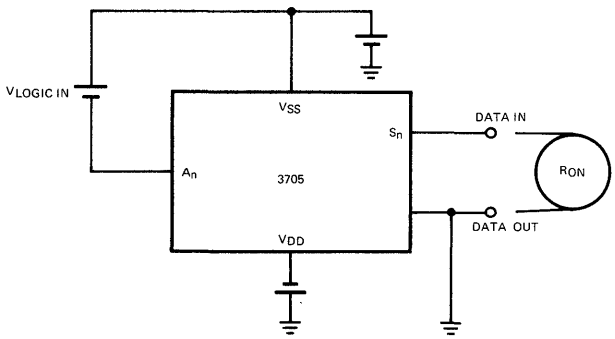


FIG. 1

POWER SUPPLY TRANSLATION CIRCUIT

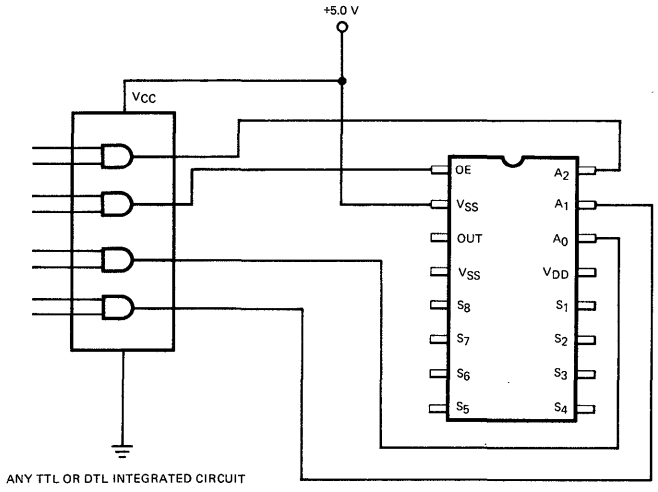


The following sets of bias conditions are equivalent:

	CONDITION 1	CONDITION 2
DATA IN	+5.0 V	0 V
V_{SS}	+7.0 V	+2.0 V
V_{DD}	−20 V	−25 V
LOGIC IN		
LOW Level	+0.2 V	−4.8 V
HIGH Level	+5.5 V	+0.5 V

Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body or V_{SS}). Voltages can be translated to a equivalent level and referenced to another electrode. In order to measure the ON resistance of the data channel accurately, the data output is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

TYPICAL CONTROL CIRCUIT



3750

10-BIT D/A CONVERTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3750 is a monolithic MOS/LSI 10-bit digital to analog converter using P-channel enhancement mode MOS technology. The digital word can be entered serially or in parallel. If desired, the word is available in serial form through an output buffer in either an 8 or 10-bit format. The converter output data is available thru 10 single pole double throw (SPDT) MOS switches. The holding register retains the state of the previous digital input word and drives the output switches. Transfer gates are used to isolate the holding register from the input register while new data is being entered. The on resistance of the MOS switches is weighted to provide the necessary accuracy and stability for a 10-bit conversion.

- **8 AND 10-BIT DATA LENGTHS**
- **SERIAL AND PARALLEL OPERATION**
- **250 kHz SERIAL BIT RATE**
- **500 kHz PARALLEL WORD RATE**
- **250Ω TYPICAL ON RESISTANCE OF TWO MSB's**
- **500Ω TYPICAL ON RESISTANCE OF REMAINING EIGHT BITS**
- **110 mW POWER DISSIPATION**
- **ZERO AND FULL SCALE CALIBRATION LOGIC**

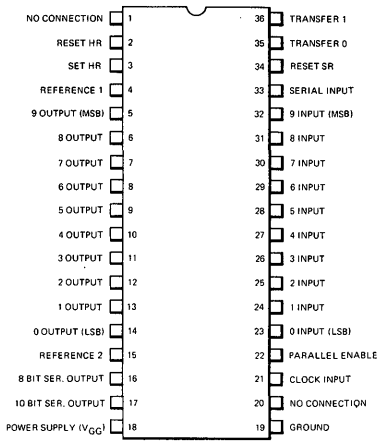
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages		-30 to +0.3 V
Power Supply		-29 V
Storage Temperature		-55°C to +150°C
Operation Temperature	3750DL	-55°C to +85°C
	3750DC	0°C to +70°C

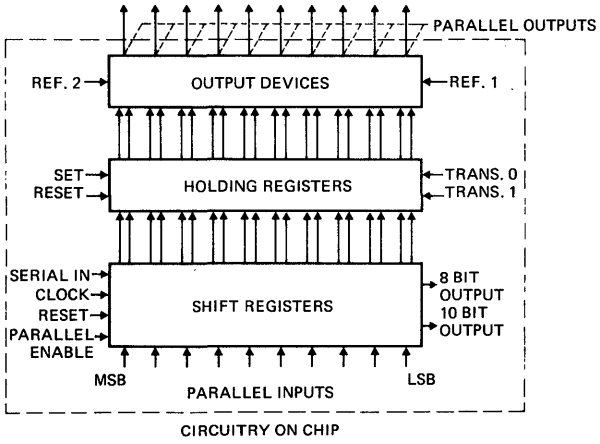
APPLICATIONS

D/A Converters
- Telemetry
- Analog data plotters
- Industrial process control
- Servo systems

CONNECTION DIAGRAM
(TOP VIEW)



BLOCK DIAGRAM



DC CHARACTERISTICS: $V_{GG} = -27 \pm 2.0$ V, $R_L = 10$ MΩ, $C_L = 10$ pF

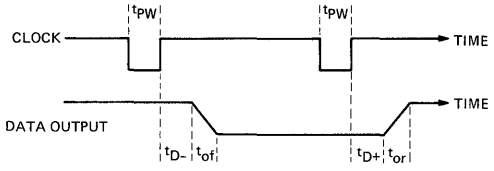
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	−2.0		0	V	
V_{IL}	Input Voltage LOW	−30		−9.0	V	
V_{OH}	Output Voltage HIGH	−1.0		0	V	
V_{OL}	Output Voltage LOW	−30		−10	V	
$V_{\phi L}$	Clock Voltage LOW	−30		−9.0	V	
I_{LI}	Input Leakage Current			5.0	μA	$V_{IN} = -20$ V
θ_T-Switch	Temperature Coefficient of Switches		0.3		%/°C	
θ_T-Tracking	Temperature Coefficient Tracking		0.03		%/°C	
I_{GG}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
R_{ON}	MOS Switch Resistance					
	"9"	150	250	500	Ω	$V_{REF} = -5.0$ V
	"8"	150	250	500	Ω	$V_{GG} = -27$ V
	"7" thru "0"	325	550	1000	Ω	
ΔR_{ON}	Switch Mismatch					
	"9"		70	150	Ω	$V_{REF2} = -5.0$ V
	"8"		70	150	Ω	$V_{REF1} = 0$ V
	"7" thru "0"		120	250	Ω	
P_D	Power Dissipation		120	190	mW	$V_{GG} = -27$ V

AC CHARACTERISTICS: $V_{GG} = -27 \pm 2.0$ V, $R_L = 10$ MΩ, $C_L = 10$ pF

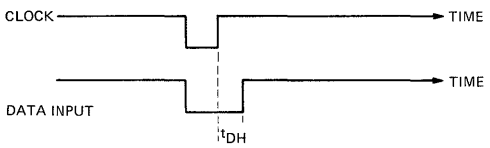
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Operating Frequency					
	Serial	dc		250	kHz	
	Parallel	dc		500	kHz	
t_{PW}	Clock Pulse Width	1.0		10	μs	
t_{DH}	Data Hold Time	250			ns	
	Serial Delay,					
t_{D-}			0.6		μs	
t_{of}	Rise and Fall Times		0.2		μs	
t_{D+}			0.5		μs	
t_{or}			0.5		μs	
	Parallel Delay,					
t_{D-}			0.55		μs	
t_{of}	Rise and Fall Times		0.35		μs	
t_{D+}			0.4		μs	
t_{or}			0.3		μs	
C_I	Data and Control Input Capacitance		7.0		pF	

TIMING DIAGRAM

OUTPUT DELAY, RISE AND FALL TIMES

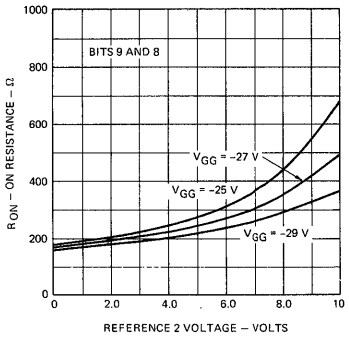


DATA BIT TIMING

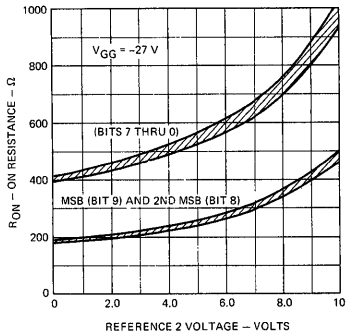


TYPICAL ELECTRICAL CHARACTERISTICS

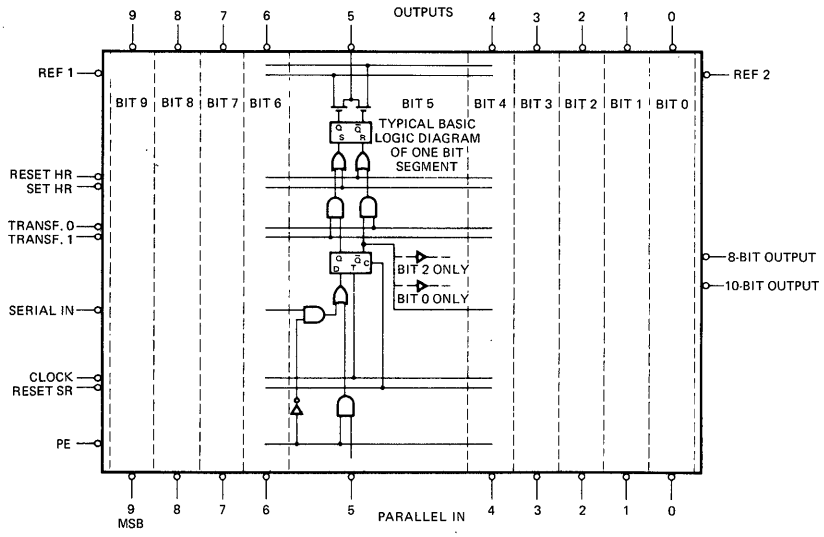
ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)



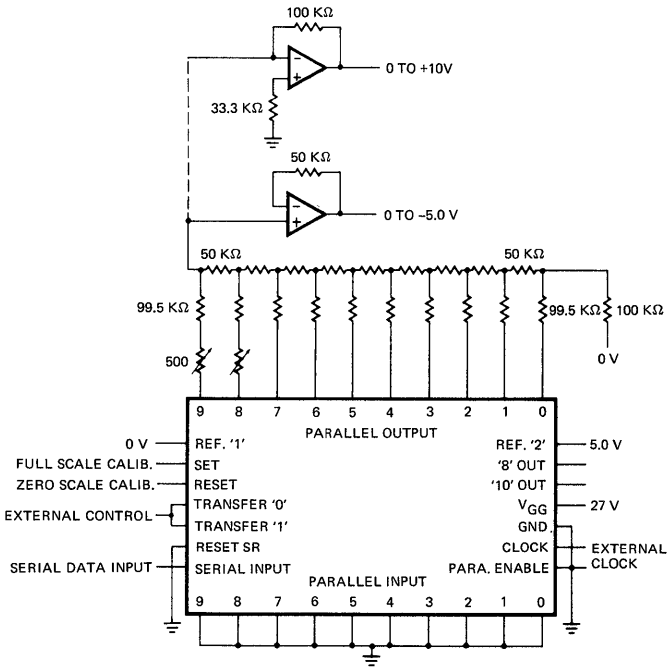
ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)



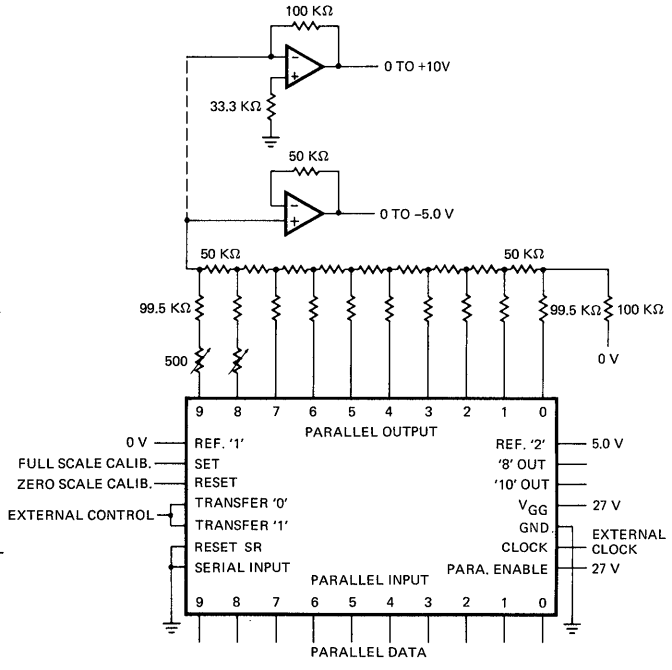
LOGIC DIAGRAM



SERIAL OPERATION

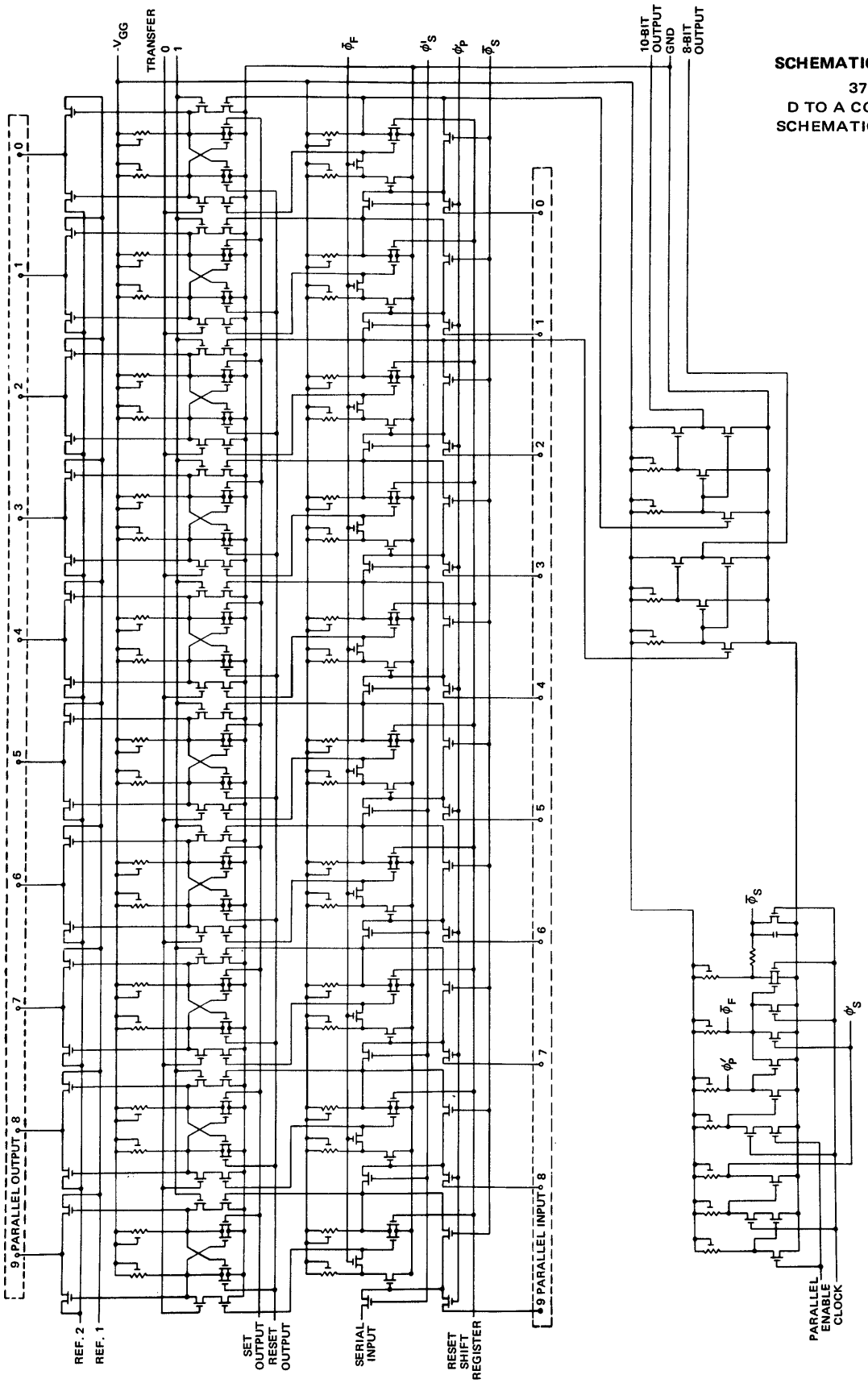


PARALLEL OPERATION



SCHEMATIC DIAGRAM

3750
D TO A CONVERTER
SCHEMATIC DIAGRAM



3751

12-BIT A/D CONVERTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3751 is a 12-Bit A/D Converter using P-channel enhancement mode MOS/LSI technology. The conversion is accomplished by the successive approximation technique. The word length is variable for eight, nine, ten or twelve bits by applying a dc potential to each of two control pins. The 3751 provides all the A/D system control functions such as: master timing, automatic start and recycle, and RZ or NRZ format control. By choosing the appropriate ladder network, the output will be in either a binary or binary coded decimal digital format.

- **8, 9, 10, OR 12-BIT WORD LENGTH**
- **RZ OR NRZ DIGITAL FORMAT**
- **COMPLETE LOGIC AND SYSTEM TIMING CIRCUITS INCLUDED ON CHIP**
- **BCD OVERVOLTAGE FLAG**
- **200Ω TYPICAL ON RESISTANCE FOR THE TWO MSB**
- **500Ω TYPICAL ON RESISTANCE FOR THE REMAINING TEN SWITCHES**
- **150 mW POWER DISSIPATION**
- **AUTOMATIC RESTART CIRCUITS**

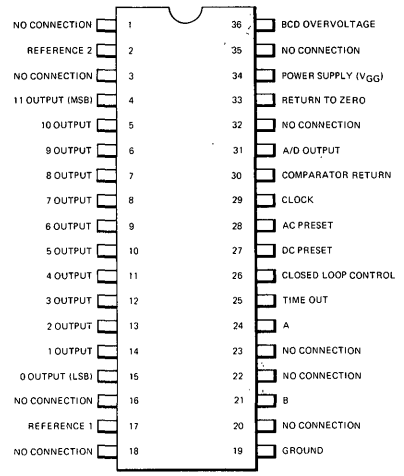
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages		−30 to +0.3 V
Power Supply		−30 V
Storage Temperature		−55°C to +150°C
Operation Temperature	(3751DL)	−55°C to +85°C
	(3751DC)	0°C to +70°C

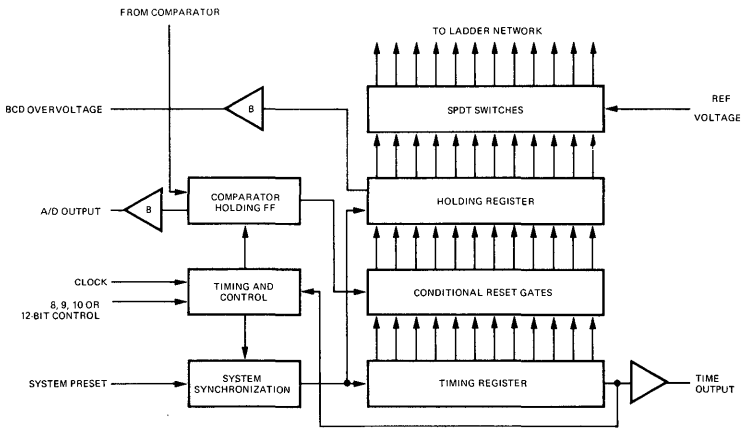
APPLICATIONS

A/D Converters
Three Digit DVM's
Telemetry
Industrial Control
Computer Interface

CONNECTION DIAGRAM
(TOP VIEW)



BLOCK DIAGRAM



DC CHARACTERISTICS: V_{GG} = –27 ±2.0V, R_L = 10 MΩ, C_L = 10 pF

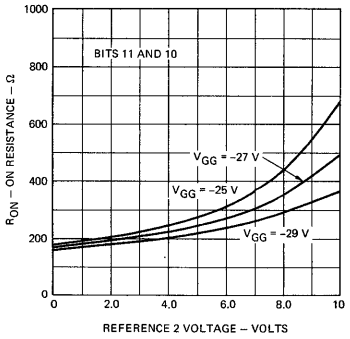
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	–2.0		0	V	
V_{IL}	Input Voltage LOW	–30		–9.0	V	
V_{OH}	Output Voltage HIGH	–1.0		0	V	
V_{OL}	Output Voltage LOW	–30		–10	V	
$V_{\phi L}$	Clock Voltage LOW	–9.0		–30	V	
I_{LI}	Input Leakage Current			5.0	μA	V_{IN} = –20 V
I_{GG}	V_{GG} Current		4.5	9.0	mA	V_{GG} = –27 V
R_{ON}	MOS Switch Resistance					
	"11"	150	250	500	Ω	
	"10"	150	250	500	Ω	
	"9" thru "0"	325	550	1000	Ω	
ΔR_{ON}	Switch Mismatch					
	"11"		70	150	Ω	
	"10"		70	150	Ω	
	"9" thru "0"		120	250	Ω	
P_D	Power Dissipation		120	190	mW	V_{GG} = –27 V

AC CHARACTERISTICS: V_{GG} = –27 ±2.0V, R_L = 10 MΩ, C_L = 10 pF

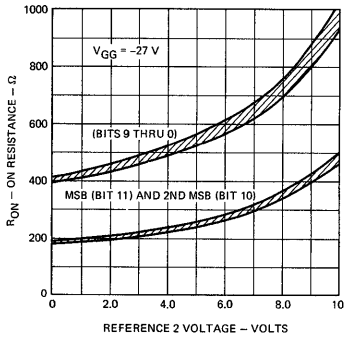
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Bit Frequency	DC		250	kHz	
t_{PW}	Clock Pulse Width	1.0		10	μs	
t_S	Temperature Coefficient of Switches		0.3		%/°C	
t_T	Temperature Coefficient of Tracking		0.03		%/°C	
t_{D-}	Analog Switch Delay		0.7		μs	V_{GG} = –27 V
t_{D+}	Analog Switch Delay		1.1		μs	
t_{of}	Analog Switch Fall Time		0.5		μs	
t_{or}	Analog Switch Rise Time		0.25		μs	
C_I	Data and Control Input Capacitance		7.0		pF	

TYPICAL ELECTRICAL CHARACTERISTICS

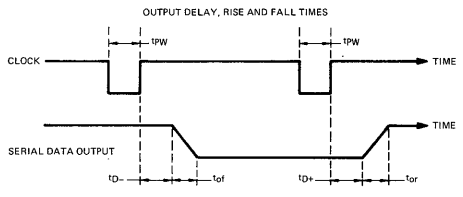
ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)



ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)



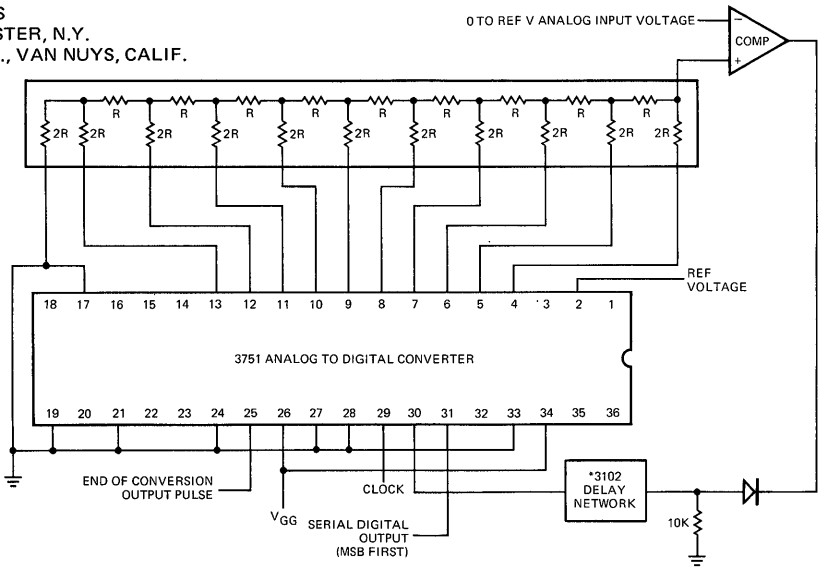
TIMING DIAGRAM



12-BIT A/D CONVERTER

NO. OF BITS	R VALUE
8	12.5k
9	25k
10	50k
12	200k

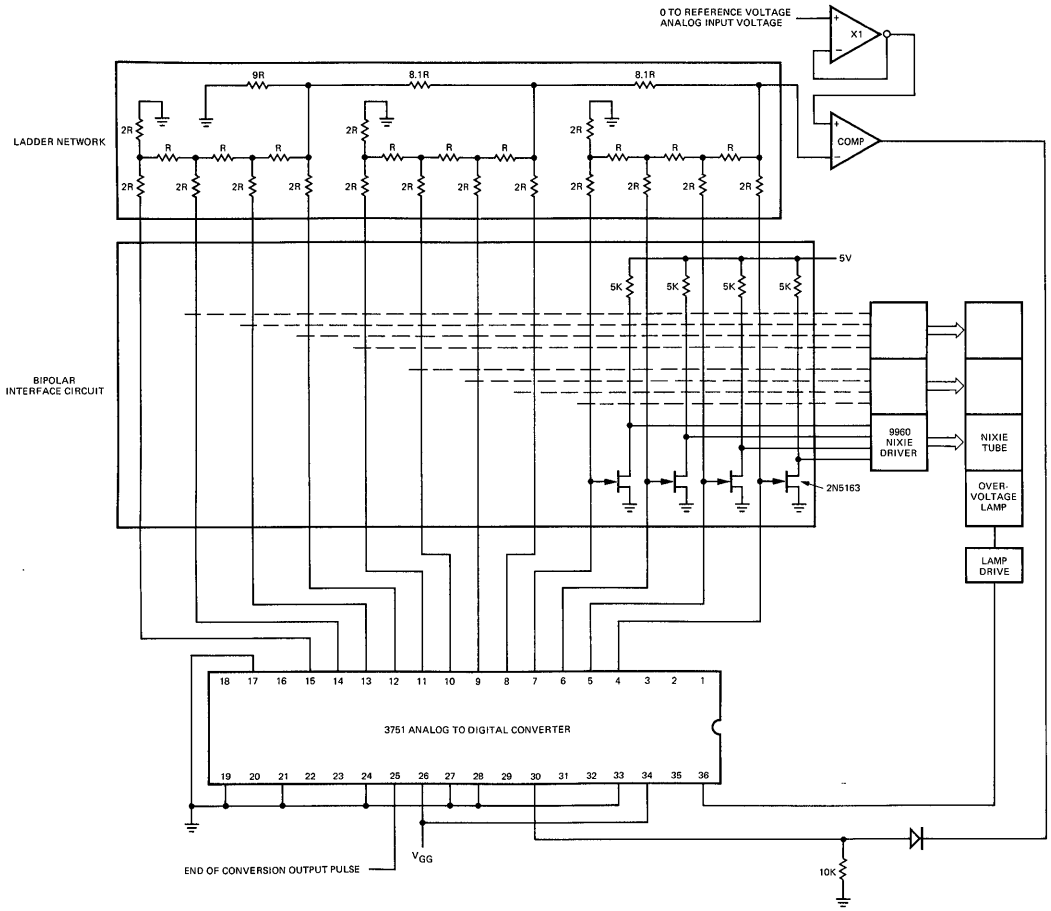
LADDER NETWORK MFGR'S
NEGADYNE CORP., ROCHESTER, N.Y.
ANGSTROM PRECISION INC., VAN NUYS, CALIF.



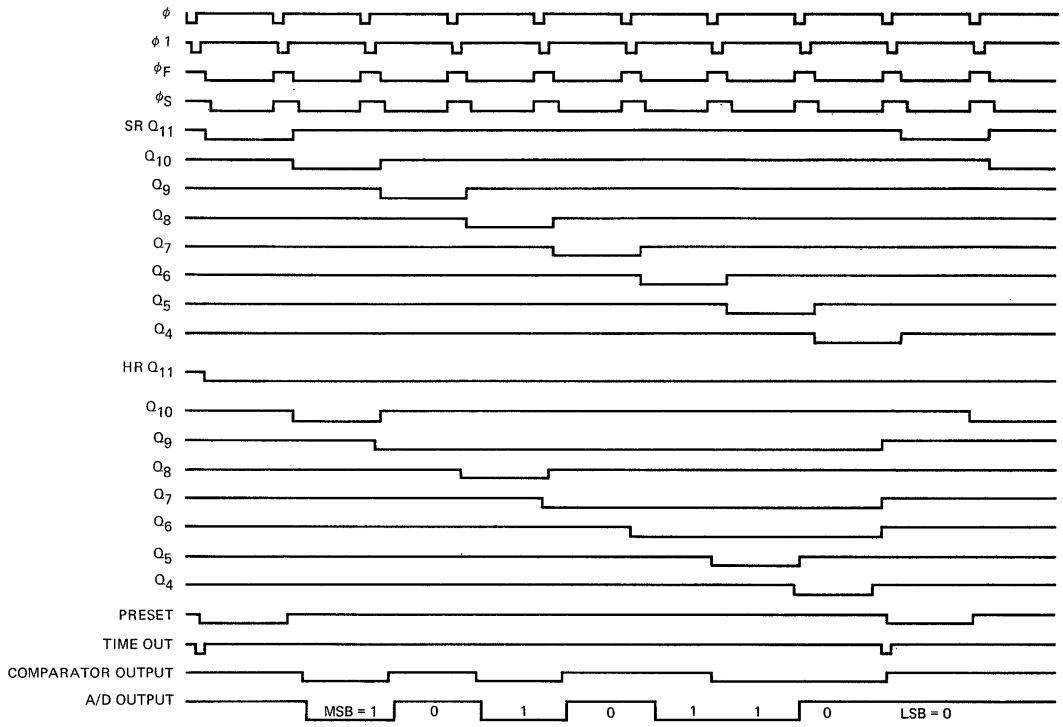
When the serial digital output is used, a delay network is required between the comparator output and the converter as shown. This is to inhibit any change of the comparator return signal at the input of the converter during a clock pulse.

*Dual 3102 as Type D Flip-Flop

3-DIGIT BCD A/D CONVERTER



TYPICAL TIMING DIAGRAM



8-BIT FORMAT
ANALOG INPUT = –3.369 V = 10101100
REFERENCE VOLTAGE = –5.000 V

DESCRIPTION OF PIN FUNCTION

PIN NO.

24, 21 A, B: These two leads are connected as shown in the truth table below to control the length of the digital word.

	8	9	10	12
A	1	0	1	0
B	1	1	0	0

25 TIME OUT: A synchronous pulse with the clock is applied at this output at the end of each conversion. This pulse may be used to step a multiplexer br otherwise notify the system of the readiness of the A/D to start another conversion.

26 CLOSED LOOP CONTROL: A '1' voltage level continuously applied to this input will put the A/D in an automatic mode of operation. The time output pulse is internally gated to cause a preset at the end of each conversion and initiate a new conversion. The automatic start circuitry presets the circuit and restarts the conversion if a bit has been dropped in this mode of operation.

27 DC PRESET: A '1' voltage level applied to this input will cause an immediate preset and the unit will stay preset until this input is returned to a '0' voltage level.

28 AC PRESET: When a '1' level is applied to this input, the A/D is preset on the next clock pulse. The unit will continue to be preset on each clock pulse until the '1' level is removed from the input.

31 A/D OUTPUT: The serial digital conversion is available at this pin in a most significant bit (MSB) first format. The data output is delayed by one bit time.

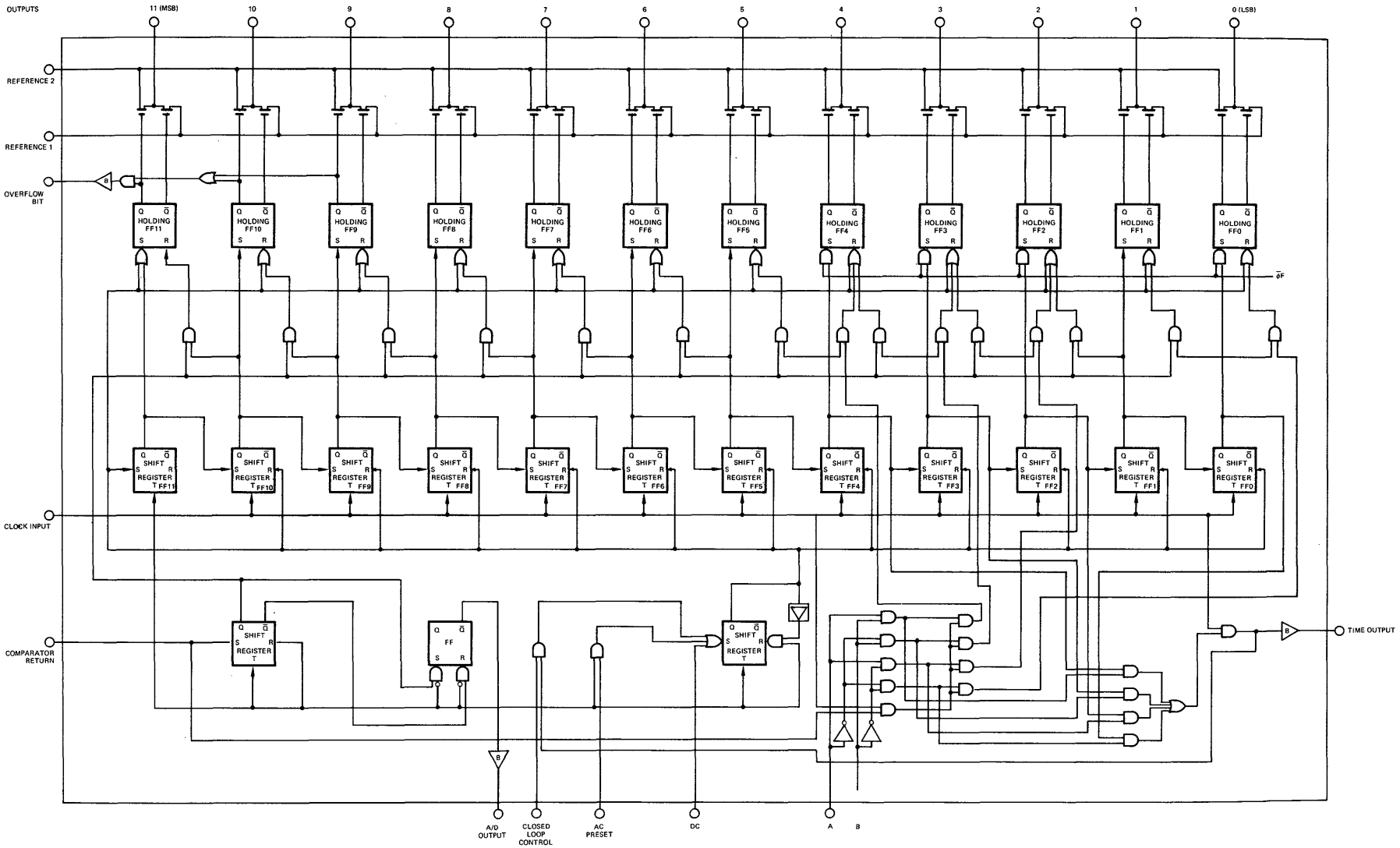
36 BCD OVERVOLTAGE: This output is used when a three digit analog to binary coded decimal (BCD) conversion is being made. If the binary equivalent of the most significant digit is greater than 9, a '1' voltage level is applied on this output.

33 RETURN TO ZERO: This input modifies the digital code format from non return to zero (NRZ) to return to zero (RZ) if used. When tied to the clock line, the digital output will return to zero during each clock pulse. The RZ duty cycle can be varied by controlling the length of time that a '1' level is applied to this input.

30 COMPARATOR RETURN: The comparator output should be connected to this input. The input must be prevented from going positive with respect to substrate (ground). The output SPDT MOS switches are successively toggled to the reference voltage. This input will cause these switches to be conditionally reset if the ladder network output voltage is greater than the signal voltage.

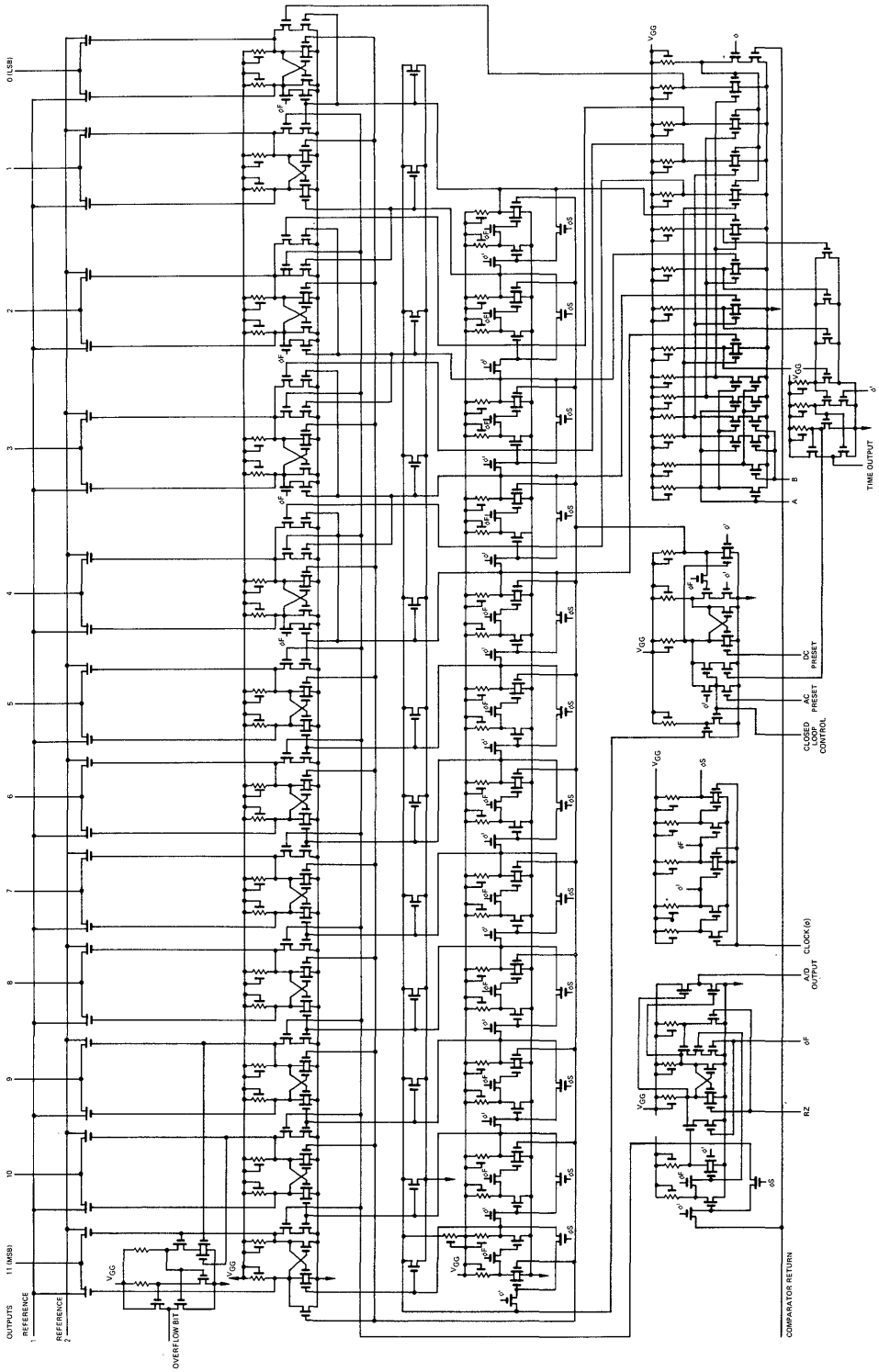
2, 17 REFERENCES 1 & 2: Reference 1 is normally connected to ground and reference 2.0 to –5.0 V. However, they may each be connected anywhere between 0 and –5.0 V dc for special applications.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (0) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈ −10 V and 1.0 = "0" ≈ Gnd.

SCHEMATIC DIAGRAM



3800
8-BIT PARALLEL ACCUMULATOR
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3800 is an LSI/MOS integrated circuit containing approximately 200 gates. It functions as an 8-bit slice of an arithmetic unit, which may be connected to form any word length. It is capable of parallel addition and subtraction, and by simultaneously shifting the sum or difference right or left, multiplication and division algorithms. A direct subtraction capability eliminates the need for the usual carry input to the LSB during subtraction, thus allowing operands to be located anywhere in the truly variable word length accumulator. The parallel data organization of the 3800 improves speed and greatly reduces the amount of random control logic when compared to the same function performed serially.

- **DIRECT SUBTRACTION USED TO PROVIDE VARIABLE WORD LENGTH CAPABILITY**
- **STROBED OUTPUTS FOR HARD WIRE COMMON BUSS SYSTEMS**
- **DC TO 200 kHz ADD AND SHIFT RATE**
- **3.0 μs, 8-STAGE CARRY PROPAGATION TIME**
- **LOW POWER—180 mW**

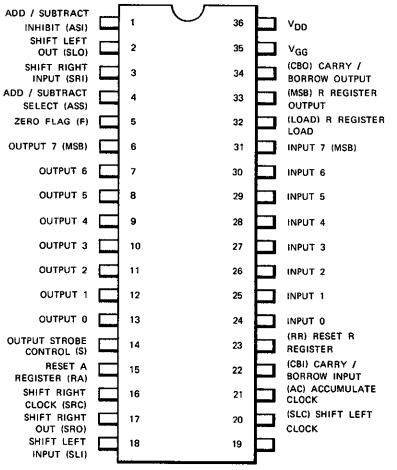
APPLICATIONS

Basic Accumulator Block
Index Register
>,=,<Comparator
General Logic Control
Up/Down Counter
Divide By N Counter

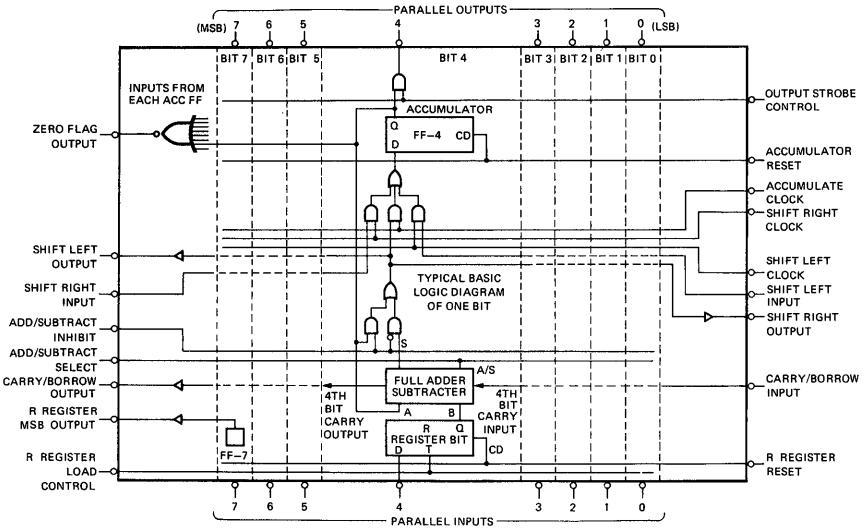
ABSOLUTE MAXIMUM RATINGS

Input Voltages		−30 V to +0.3 V
V_{GG} and V_{DD} Supply Lines		−30 V to +0.3 V
Storage Temperature		−55°C to +150°C
Operating Temperature	(3800DL)	−55°C to +85°C
	(3800DC)	0°C to +70°C

CONNECTION DIAGRAM
(TOP VIEW)

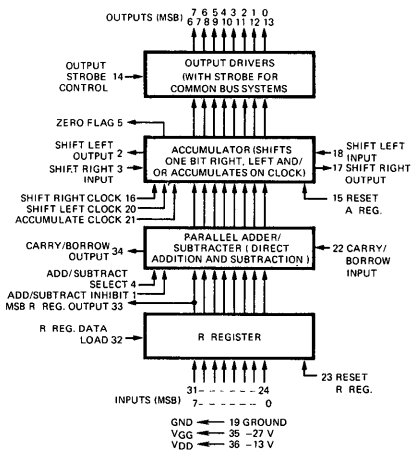


LOGIC BLOCK DIAGRAM



NOTE:
Polarity indicators (○) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box conventional MOS polarities are used, where "1" ≈ −10 V and "0" ≈ GND.

BLOCK DIAGRAM



DC CHARACTERISTICS: $V_G = -27 \pm 1$ V, $V_{DD} = -13 \pm 1$ V, $R_L = 10$ MΩ, $C_L = 10$ pF, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	−2.0		0	V	$V_{GG} = -27$ V
V_{IL}	Input Voltage LOW	−30		−10	V	$V_{GG} = -27$ V
V_{OH}	Output Voltage HIGH	−1.0	−0.5	0	V	
V_{OL}	Output Voltage LOW		−12	−11	V	
V_{OL}	Output Voltage LOW		−11	−10	V	$R_L = 40$ kΩ
$V_{\phi L}$	Clock Voltage LOW	−30		−10	V	
I_{LI}	Input Leakage Current			5.0	μA	$V_{IN} = -20$ V
I_{DD}	V_{DD} Current			7.0	mA	$V_{GG} = -27$ V, $V_{DD} = -13$ V
I_{GG}	V_{GG} Current			5.0	mA	$V_{GG} = -27$ V, $V_{DD} = -13$ V
P_D	Power Dissipation		180		mW	

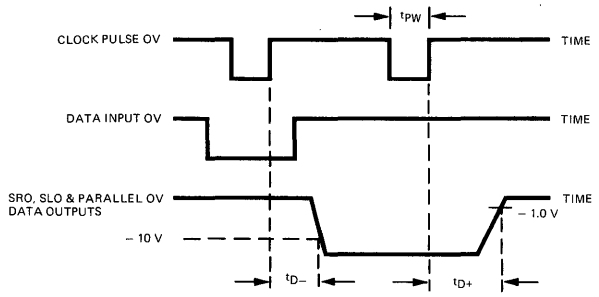
AC CHARACTERISTICS: $V_{GG} = -27 \pm 1$ V, $V_{DD} = -13 \pm 1$ V, $R_L = 10$ MΩ, $C_L = 10$ pF, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Shift Frequency	dc		300	kHz	
f_{SA}	Shift & Add Frequency	dc		200	kHz	
$t_{PW\phi}$	Clock Pulse Width	1.0		10	μs	
t_{DC}	Carry Delay Time		3.0	5.0	μs	See Figure 1
t_{DO}	Output Delay Time		1.0	3.0	μs	

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTIONS
1	Add/Subtract inhibit	ASI	When ASI is a logic "1", no addition or subtraction will occur when the ACC, SRC or SLC clock are pulsed. The accumulator register will shift right or left normally however. The carry/borrow through line is not affected, allowing numbers to be shifted and compared when the subtract mode is selected.
2	Shift left output	SLO	SLO is the MSB output of the ACC and may be connected directly to the SLI input of the next 8-bit section of the accumulator. Shift and add function normally.
3	Shift right input	SRI	SRI accepts the SRO output of a highter order, 8-bit slice. Shift and add function normally.
4	Add/Subtract select	ASS	When ASS is a logic "1", addition is performed and when ASS is a logic "0", subtraction is performed.
5	Zero flag	F	The zero flag output is a logic "1" only if the accumulator register contains all zeros. This output is independent of the strobe control.
6-13	Outputs	7-0	When the strobe control STR is a logic "0", all outputs represent the contents of the accumulator register.
14	Output strobe control	STR	When STR is a logic "1", all parallel outputs, 0-7, are disconnected from the power and ground lines allowing them to float. Thus several similar outputs may be hard wired together for a common buss system.
15	Reset Accum. register	RA	When RA = logic "1", the accumulator is reset to zero. This asynchronous signal overrides all others.
16	Shift right clock	SRC	Pulsing the SRC with a logic "1" shifts the contents of the accumulator one bit position to the right. If the add/subtract controls are enabled, the sum or difference of the accumulator register and the R register is shifted one bit to the right and written into the accumulator.
17	Shift right output	SRO	SRO is the LSB end of the 8-bit accumulator and may be connected directly to the SRI of an adjacent 8-bit slice.
18	Shift left input	SLI	The SLI accepts the SLO output from a lower order, 8-bit slice.
19	Ground	GND	Circuit common and substrate ground are both connected to this pin.
20	Shift left clock	SLC	Pulsing the SLC with a logic "1" shifts the contents of the accumulator one bit position to the left. If the add/subtract controls are enabled, the sum or difference of the accumulator and the R register is shifted one bit to the right and written into the accumulator.
21	Accumulate clock	AC	Pulsing the ac input adds the contents of the accumulator and the R register if ASS = logic "1". The R register is subtracted from the accumulator if ASS = "0". If ASI = "1", no action occurs.
22	Carry/borrow input	CBI	A logic "1" on CBI enters a carry or borrow into the LSB position of the add/subtract logic.
23	Reset R register	RR	Placing a logic "1" on RR asynchronously resets the R register.
24-31	Inputs	0-7	Inputs are entered into the R register asynchronously when R_L is activated.
32	R register data load	R_L	When R_L is a logic "1", data presented at the inputs are loaded into the R register. R_L may be permanently a logic "1", effectively bypassing the R register during normal operation. Note that RR overrides the data inputs regardless of the load command.
33	MSB R register output	MSB	It shows the MSB of the R register. When the R register is used to temporarily hold operands during multiply, divide, etc., the MSB output indicates the sign of the stored operand.
34	Carry/borrow output	CBO	The CBO is the asynchronous carry or borrow output from the MSB of the add/subtract logic. It is not effected by the ASI control.
35	V_{GG} power supply	V_{GG}	−27 V supply.
36	V_{DD} power supply	V_{DD}	−13 V supply.

SHIFT COMMAND TIMING DIAGRAM



CARRY/BORROW 8-STAGE PROPAGATION TIME

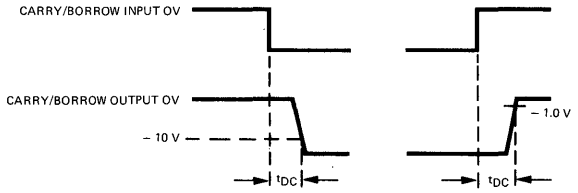
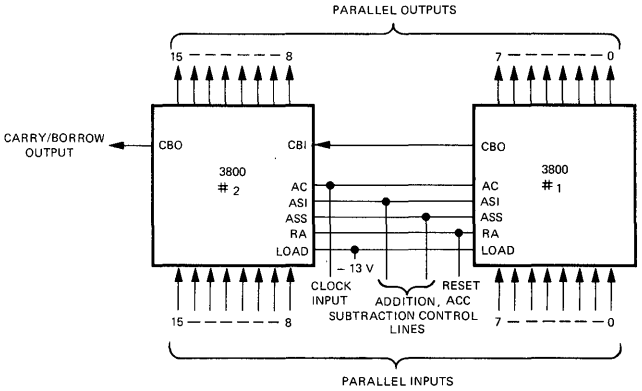


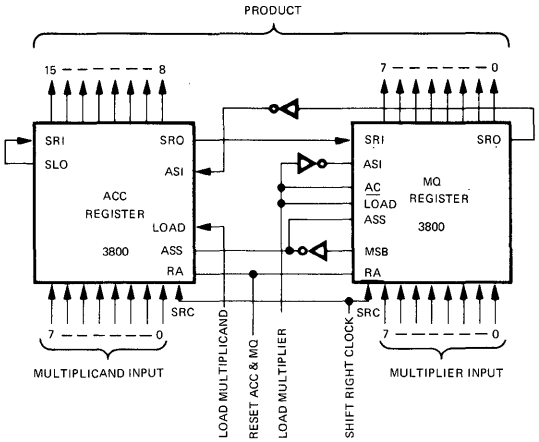
Fig. 1

STANDARD CONNECTIONS FOR ADDITION AND SUBTRACTION

16-BIT PARALLEL ADDITION (SUBTRACTION)*: The addition (subtraction) operation begins by resetting the accumulator, then transferring the augend (subtrahend) through the R register into the accumulator by pulsing the ac clock line. The operation is completed by loading the addend (minuend) into or through the R register, then adding to (or subtracting from if ASS = logic "0") the accumulator by again pulsing the ac clock. Multiple addition and subtraction or combinations of both operations may be performed by repeating the last operation. Thus a running total may be kept in the accumulator.



STANDARD CONNECTIONS FOR MULTIPLICATION



MULTIPLICATION: The multiplication operation, shown above, begins by clearing the ACC and MQ registers, then loading the multiplier into the MQ R register. If the MSB of the MQ's R register is a "1", i.e., the multiplier is negative, the ACC and MQ subtract lines are enabled before the multiplier is transferred into the MQ. Thus the multiplier in the MQ is always positive. However, the multiplicand, which has been loaded into the ACC R register for temporary storage, will be subtracted from the partial product in the ACC if the multiplier were negative. The multiplicand is added to or subtracted from the partial product and shifted one bit to the right each time the LSB of the MQ register is a "1". If it is a "0", only a shift right occurs. Neither the multiplicand nor the resulting product require any further sign corrections as the answers will automatically be in two's complement.

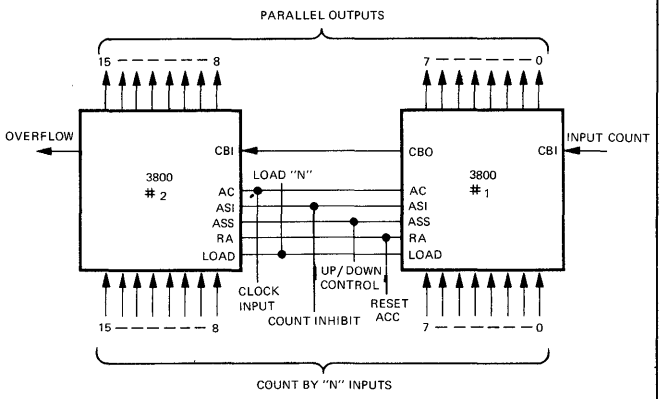
DIVISION: The division algorithm is similar to the multiply and is described in detail in The Logic of Computer Arithmetic by Flores. The most straightforward way to perform division is to convert both the divisor and dividend to sign magnitude numbers the same way the multiplier was converted in multiplication. Then proceed through a successive subtraction division. The resulting positive quotient must however then be corrected to two's complement rotation if the signs of the dividend and the divisor were not the same.

NOTES:
1. Input logic levels may be selected by referring to the list of Pin Function Description.
2. All unused input or control pins should be grounded.
3. All operands are in two's complement notation.
4. All diagrams are BASIC BLOCK DIAGRAMS and no electrical levels are indicated. See Logic Diagram for correct 806B notation.

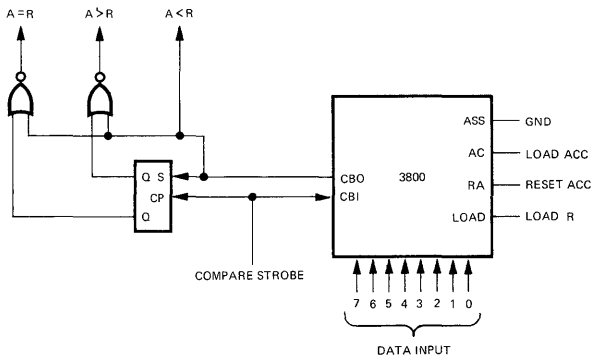
APPLICATIONS

UP/DOWN COUNTER

16-STAGE UP/DOWN COUNTER: Operation begins by resetting the registers and enabling ASS, which determines the count direction. Counting by one may be accomplished by enabling CBI or INPUT "0". To count by n, set n into the R register.

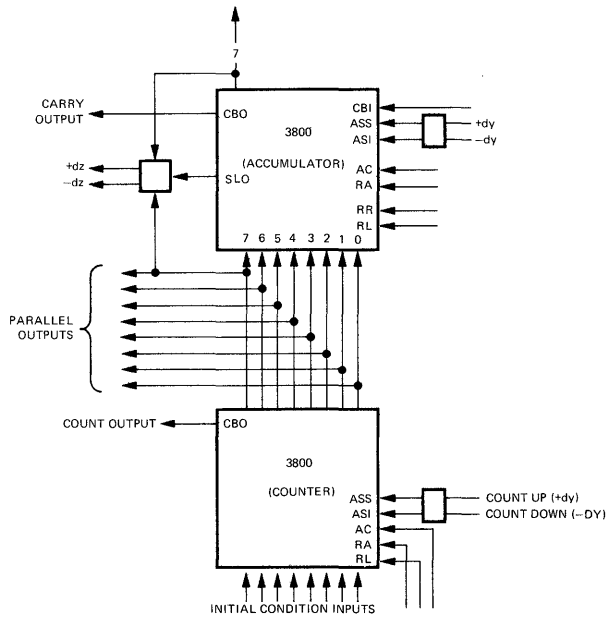


L, = > COMPARATOR



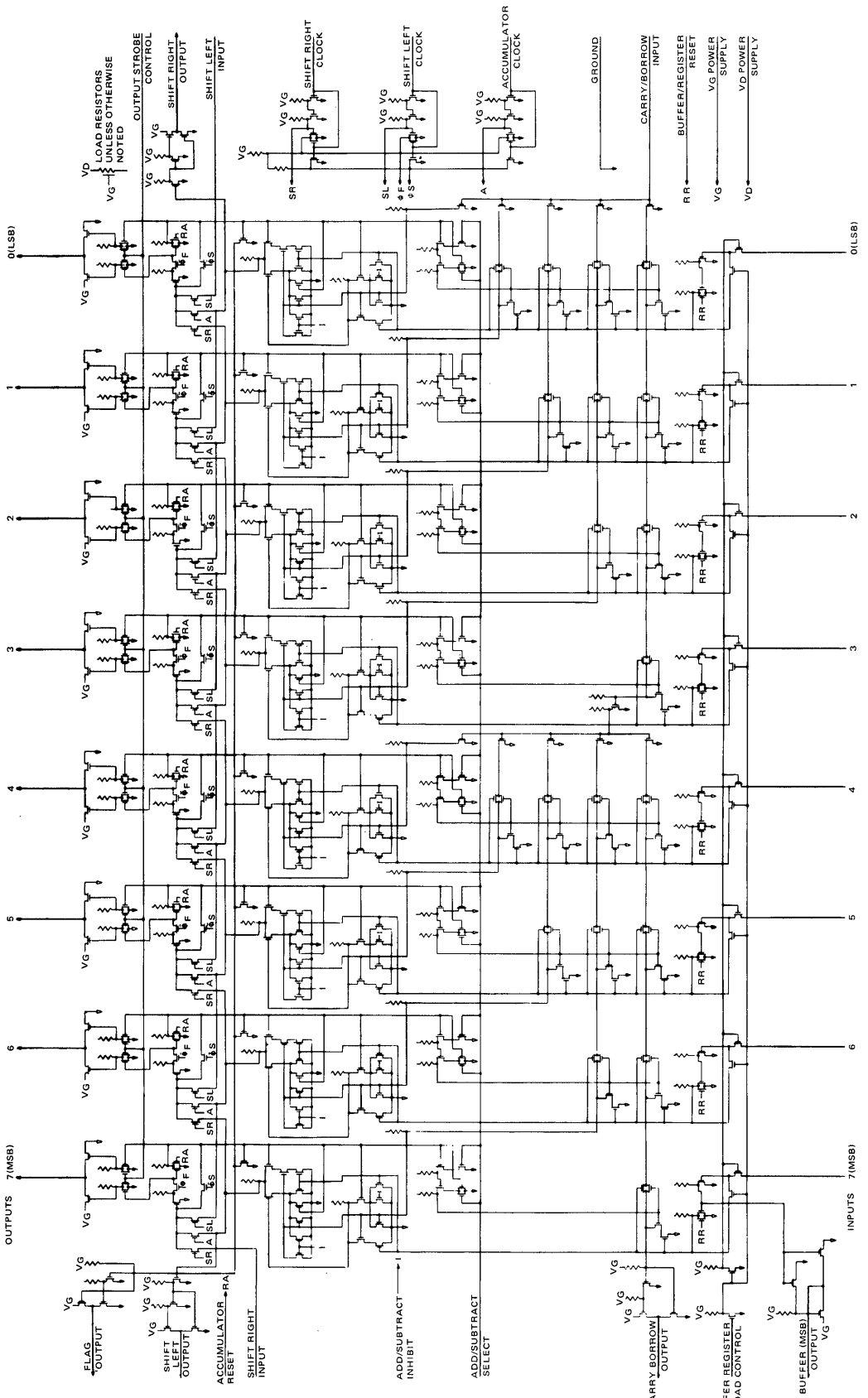
COMPARE OPERATION: To compare two numbers, simply insert the first into a previously cleared accumulator by pulsing ac. Enabling the subtract control will immediately indicate whether R>A, as a borrow output will appear. If the borrow output follows a pulse on the borrow input, the numbers are equal. If neither, then R<A. The logic is shown to the left.

DDA CONNECTIONS



The DDA shown above utilizes one 3800 for a remainder register and a second 3800 for a y accumulator counter.

SCHEMATIC DIAGRAM



3801

10-BIT SERIAL/PARALLEL-PARALLEL/SERIAL CONVERTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3801 is a monolithic MOS/LSI 10-bit serial/parallel – parallel/serial converter utilizing P-channel enhancement mode MOS technology. The device has the capability of serial or parallel input and serial or parallel output. A holding register included on the chip is isolated from the shift register by transfer gates. In serial to parallel applications data may be stored in the holding register while new data is being entered into the shift register.

- **8 AND 10-BIT SERIAL OUTPUT**
- **250 kHz SERIAL TO PARALLEL OPERATION**
- **500 kHz PARALLEL TO PARALLEL OPERATION**
- **120 mW POWER DISSIPATION**
- **INPUT GATE PROTECTION**
- **SET AND RESET OF HOLDING REGISTER**
- **OUTPUT STROBE CONTROL**
- **SINGLE PHASE CLOCK**
- **RESET OF SERIAL REGISTER**

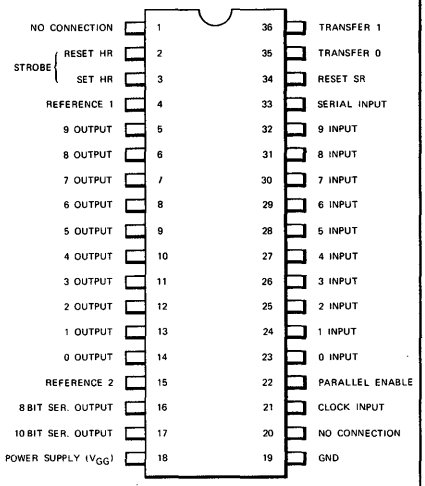
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages	−30 V to +0.3 V
Power Supply	−30 V
Storage Temperature	−55°C to +150°C
Operation Temperature (3801DL)	−55°C to +85°C
(3801DC)	0°C to +70°C.

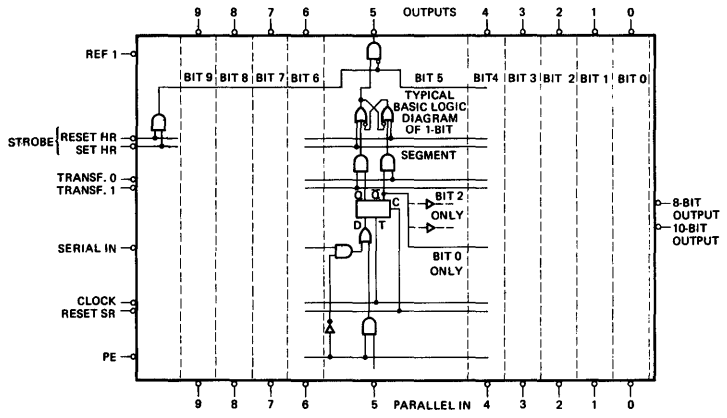
APPLICATIONS

Serial and Parallel Data Converion in:
- Process Control
- Data Terminals
- Computer Peripheral Equipment
- Data Acquistion

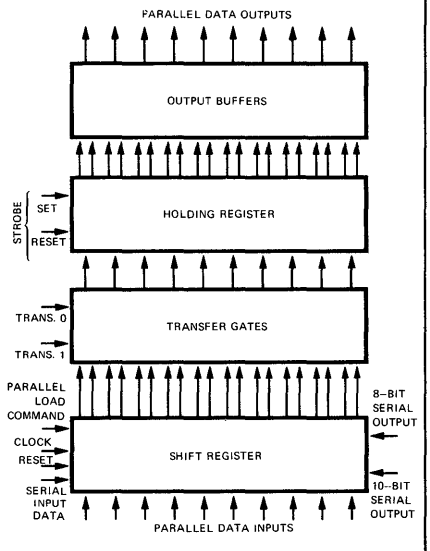
CONNECTION DIAGRAM
(TOP VIEW)



LOGIC DIAGRAM



BLOCK DIAGRAM



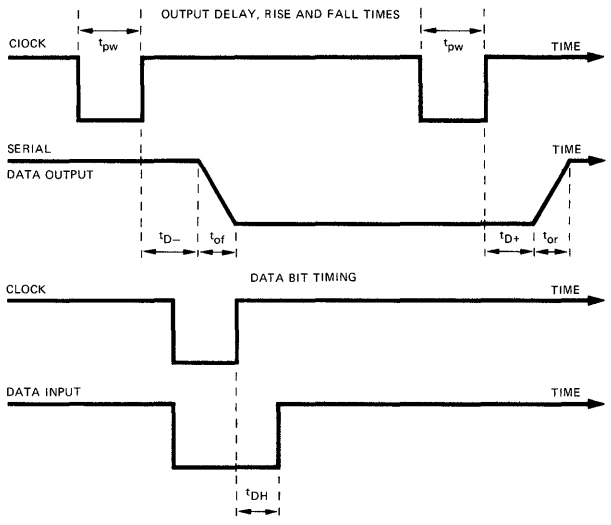
DC CHARACTERISTICS: V_{GG} = −27 ±2.0 V, R_L = 10 MΩ, C_L = 10 pF.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	−2.0		0	V	
V_{IL}	Input Voltage LOW	−30		−9.0	V	
V_{OH}	Output Voltage HIGH	−1.0		0	V	
V_{OL}	Output Voltage LOW		−11	−10	V	R_L = 40 kΩ
V_{OL}	Output Voltage LOW		−12	−11	V	
$V_{\phi L}$	Clock Voltage LOW	−30		−9.0	V	
I_{LI}	Input Leakage Current			5.0	μA	V_{IN} = −20 V
I_{GG}	V_{GG} Current		4.5	7.0	mA	V_{GG} = −27 V
P_D	Power Dissipation		120	190	mW	V_{GG} = −27 V

AC CHARACTERISTICS: V_{GG} = −27 ±2.0 V, R_L = 10 MΩ, C_L = 10 pF.

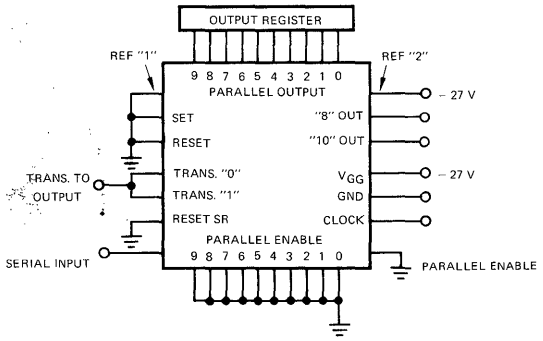
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Operating Frequency					
	Serial	dc		250	kHz	
	Parallel	dc		500	kHz	
$t_{PW\phi}$	Clock Pulse Width	1.0		10	μs	
t_{D-}	Serial Delay, Rise and Fall Times		0.6		μs	
t_{of}			0.2		μs	
t_{D+}			0.5		μs	
t_{or}			0.5		μs	
t_{D-}	Parallel Delay, Rise and Fall Times		0.55		μs	
t_{of}			0.35		μs	
t_{D+}			0.4		μs	
t_{or}			0.3		μs	
t_{DH}	Data Hold Time	250			ns	
C_I	Data and Control Input Capacitance		7.0		pF	

TIMING DIAGRAM

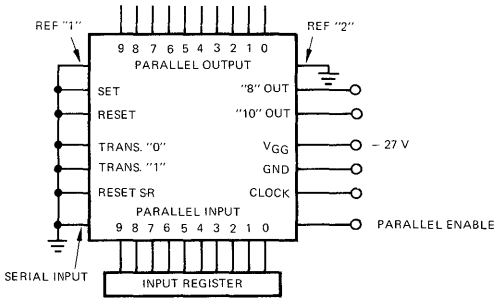


APPLICATIONS (Basic Logic Representation)

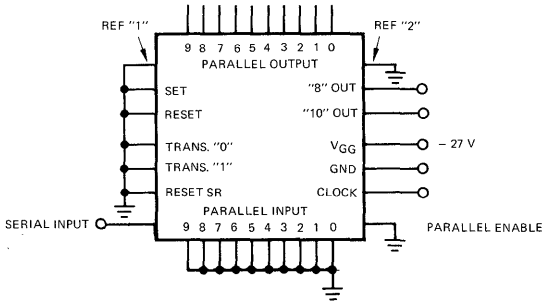
SERIAL TO PARALLEL CONVERTER



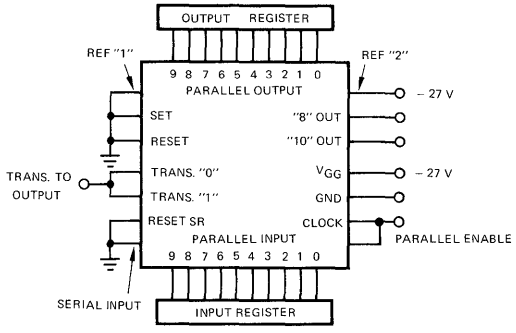
PARALLEL TO SERIAL CONVERTER



SERIAL TO SERIAL BUFFER REGISTER



PARALLEL TO PARALLEL BUFFER REGISTER



SH0013
2-PHASE MOS CLOCK DRIVERS
FAIRCHILD INTEGRATED MICROSYSTEM CIRCUIT

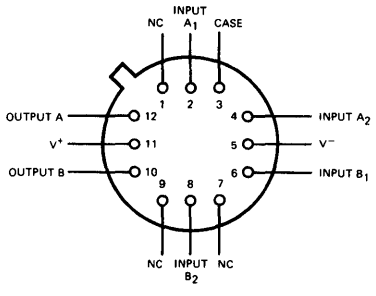
GENERAL DESCRIPTION – THE SH0013, designed for driving 2-phase MOS clock lines, is a dual high voltage driver capable of driving large capacitive loads at computer speeds. The SH0013 was designed to be driven by TTL circuits having moderate output current capability, such as TTL buffers (9009, 9N40, 9H40, 9S40) or TTL line drivers (μA9614). The circuit may also be driven by standard TTL circuits, such as the 9002, with slight degradation in rise time. Capacitive coupling from the driving TTL circuitry to the SH0013 provides independent fixed width output pulses. DC level shifting may also be employed and is especially simple for +5V, -12V MOS systems.

The device is supplied in a 12-pin TO-8 type package, capable of dissipating 1.0 W at 70°C or 0.5 W at 125°C. Use of an efficient fin radiator extends allowable dissipation to 1.66 W at 70°C or 0.8 W at +125°C.

- **30 V OUTPUT VOLTAGE SWING**
- **±600 mA OUTPUT CURRENT CAPABILITY**
- **5 MHz REPETITION RATE**
- **CAPACITIVE LEVEL SHIFTING**
- **INDEPENDENT FIXED WIDTH OUTPUT PULSES**
- **"ZERO" QUIESCENT POWER DISSIPATION**

CONNECTION DIAGRAM
(BOTTOM VIEW)

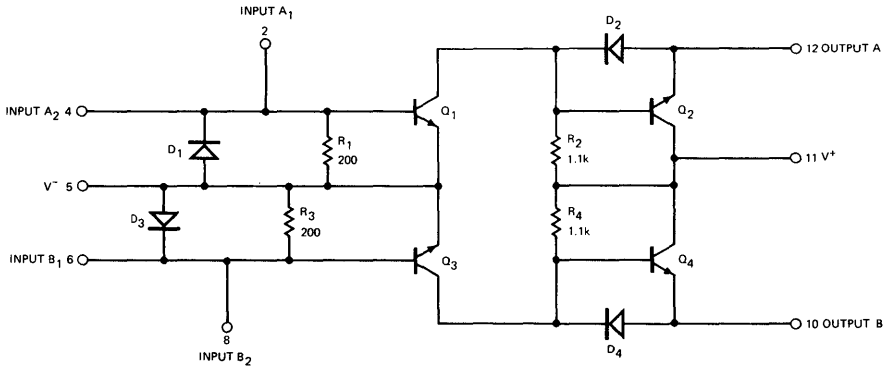
12-Lead TO-8 Type Package



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Difference (Pin 11 to Pin 5)		30V
Input Current (Pins 2, 4, 6, 8)		±75 mA
Peak Output Current (Pins 10, 12)		±600 mA
Power Dissipation at 25°C (No Heat-Sink – See Figure 10)		1.5 W
Storage Temperature		-65°C to +150°C
Operating Temperature	SH0013C1	-55°C to +125°C
	SH0013C9	0°C to +85°C
Lead Temperature (1/16" from case for 60 seconds)		300°C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Note 1) (Figures 14, 16)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Logical "0" Output Voltage	I_{OUT} = –50 mA I_{IN} = 1 mA	$V^+ - 3.0$	$V^+ - 1.0$		V
	I_{OUT} = –100 μA I_{IN} = 1 mA	$V^+ - 0.9$	$V^+ - 0.7$		V
Logical "1" Output Voltage	I_{OUT} = 50 mA I_{IN} = 10 mA		$V^- + 1.5$	$V^- + 2.0$	V
	I_{OUT} = 100 μA I_{IN} = 10 mA		$V^- + 0.7$	$V^- + 0.9$	V
Power Supply Leakage Current	$V^+ - V^-$ = 30 V				
	$I_{OUT} = I_{IN} = 0$		<1.0	100	μA
Negative Input Voltage Clamp	I_{IN} = –10 mA	$V^- - 1.2$	$V^- - 0.7$		V
t_d(on)	C_{IN} = 2200 pF R_{IN} = 0 $V^+ - V^-$ = 20V C_L = 1000 pF		15	30	ns
t_{rise} (Note 3)			35	50	ns
t_d(off) (Note 2)			15	30	ns
t_{fall} (Note 2)		40	50	80	ns
t_{fall} (Note 3)		40	70	120	ns
t_{pw}		340	420	490	ns
t_{rise}	C_{IN} = 500 pF R_{IN} = 0 $V^+ - V^-$ = 20V C_L = 200 pF		15		ns
t_{fall}			20		ns
t_{pw}			110		ns
Positive Output Swing	I_{OUT} = 0		$V^+ - 0.7$		V
Negative Output Swing			$V^- + 0.7$		V

NOTES:
(1) V^+ = 20V, V^- = 0V unless otherwise specified. Typicals are for 25°C; minimum and maximum values are for $0°C \leq T_A \leq 85°C$ for the SH0013C1, and $-55°C \leq T_A \leq +125°C$ for the SH0013C9.
(2) Values shown are for output pulse width determined by input pulse width. (Figure 16, V_{IN} 2).
(3) Output rise and fall times vary depending upon input capacitance and resistance. Refer to Figures 7 and 8.

TABLE 1. TYPICAL DRIVE CAPABILITY OF SH0013 DRIVEN BY μA9614 at 70°C ambient (No Heat Sink)

$V^+ - V^-$	FREQUENCY 50% DUTY CYCLE	PULSE WIDTH	R_{IN}	C_{IN}	C_L (MAX)	RISE TIME (MIN)
28V					50 pF	
20V	4 MHz	100 ns	0	700 pF	200 pF	7 ns
16V					350 pF	10 ns
28V					100 pF	5 ns
20V	2 MHz	200 ns	10Ω	1800 pF	400 pF	14 ns
16V					700 pF	19 ns
28V					400 pF	19 ns
20V	1 MHz	200 ns	0	2300 pF	1000 pF	34 ns
16V					1700 pF	45 ns
28V					2800 pF	130 ns
20V	0.5 MHz	500 ns	10Ω	4800 pF	5500 pF	183 ns
16V					9300 pF	248 ns

ELECTRICAL CHARACTERISTICS

Fig. 1 PULSE WIDTH AS A FUNCTION OF R_{IN} AND C_{IN} FOR SH0013 AND μA9614 LINE DRIVER

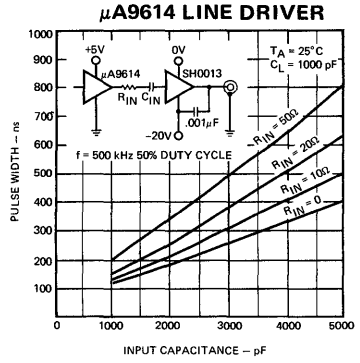


Fig. 2 PULSE WIDTH AS A FUNCTION OF R_{IN} AND C_{IN} FOR SH0013 AND 9009 DUAL BUFFER

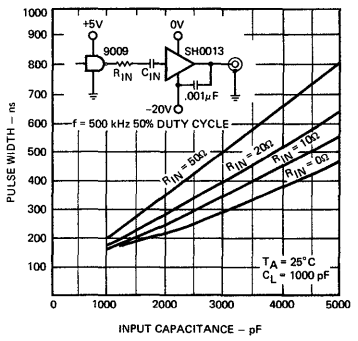
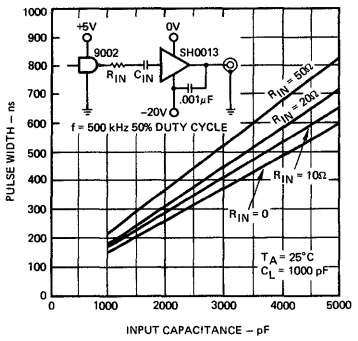


Fig. 3 PULSE WIDTH AS A FUNCTION OF R_{IN} AND C_{IN} FOR SH0013 AND 9002 NAND GATE



ELECTRICAL CHARACTERISTICS (Cont'd)

Fig. 4 PULSE WIDTH VERSUS AMBIENT TEMPERATURE

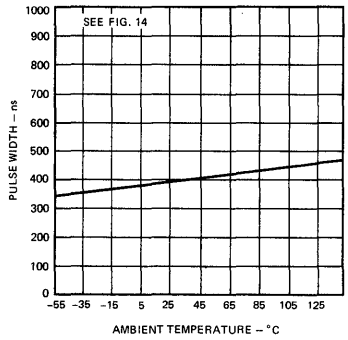


Fig. 5 PULSE WIDTH VERSUS TTL SUPPLY VOLTAGE

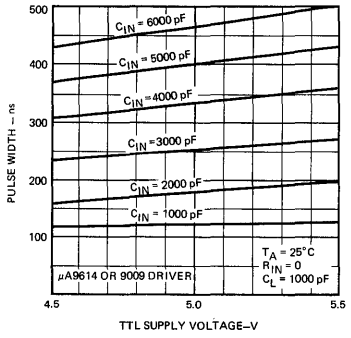


Fig. 6 ABSOLUTE MINIMUM RISE/FALL TIME AS A FUNCTION OF OUTPUT LOAD CAPACITANCE AND VOLTAGE SWING

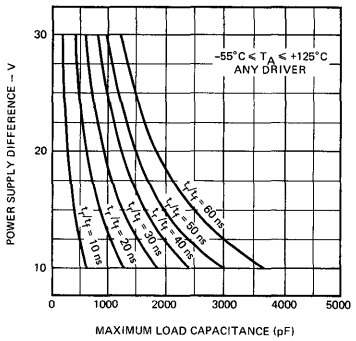


Fig. 7 RISE TIME VERSUS INPUT RESISTANCE

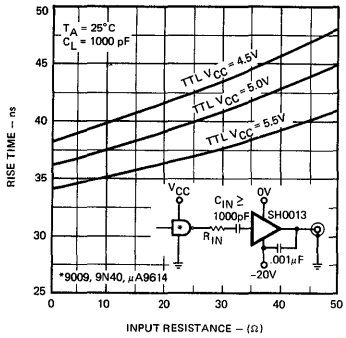


Fig. 8 FALL TIME VERSUS INPUT CAPACITANCE

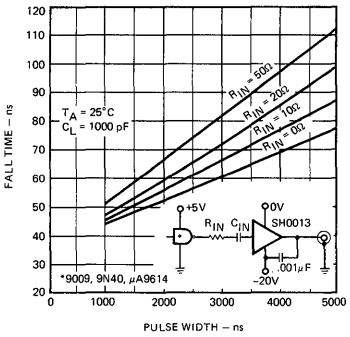


Fig. 9 TRANSITION TIMES VERSUS AMBIENT TEMPERATURE

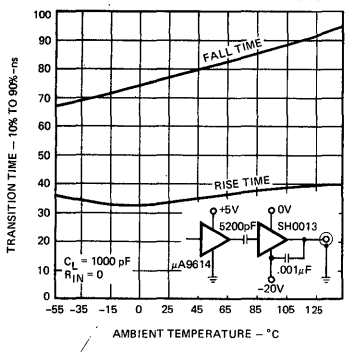


Fig. 10 MAXIMUM ALLOWABLE POWER DISSIPATION (12 LEAD TO-8 PACKAGE)

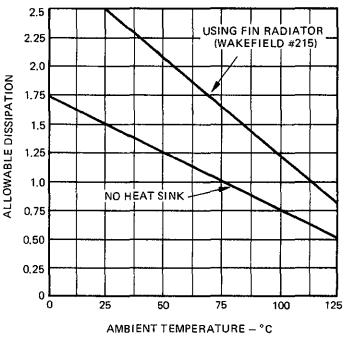


Fig. 11 AVERAGE INTERNAL POWER (PER DRIVER) AS A FUNCTION OF SUPPLY DIFFERENCE AND DUTY CYCLE

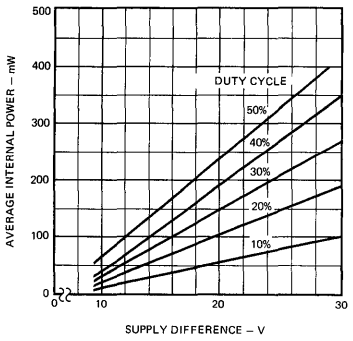


Fig. 12 TRANSIENT POWER VERSUS FREQUENCY FOR 16 VOLT SUPPLY DIFFERENCE

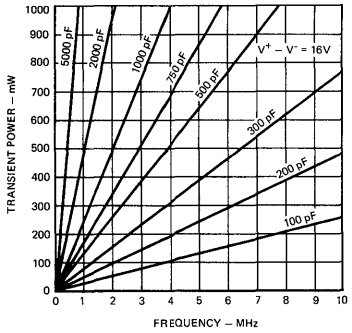
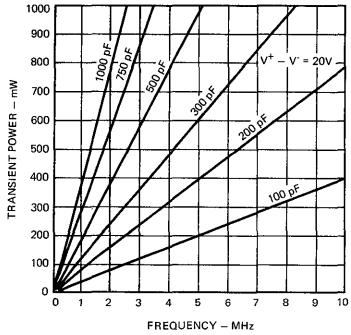
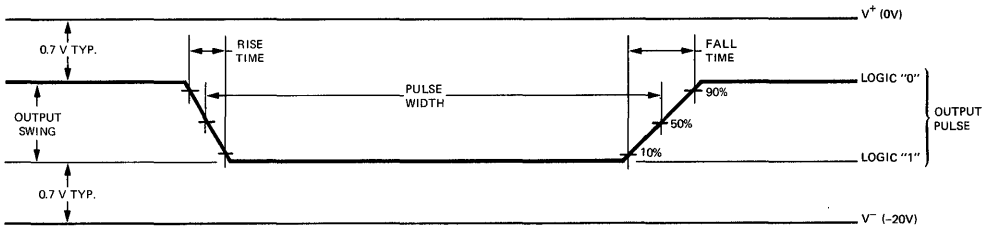


Fig. 13 TRANSIENT POWER VERSUS FREQUENCY FOR 20 VOLT SUPPLY DIFFERENCE



APPLICATIONS

WAVEFORM DEFINITIONS



Logic "0" = Most positive output voltage
Logic "1" = Most negative output voltage
Output Swing = Clock pulse amplitude

V^+ = MOS V_{SS} Supply
V^- = MOS V_{DD} Supply
$V^+ = V^-$ — Power Supply Difference
$V^+ - V^-$ = Power Supply Difference

PULSE CHARACTERISTICS

All output pulse characteristics (rise time, fall time, pulse width) are determined by the input circuitry (R_{IN}, C_{IN}) and the driving element. In operation, the driving element, such as a μA9614 line driver, delivers a positive voltage through the coupling elements to the SH0013 input transistor. As the input voltage reaches approximately 0.6 V, the input transistor (Q_1) begins to turn on and discharge the load capacitance in some rise time (t_r). If $R_{IN} = 0$ and $C_{IN} > 1000$ pF, the rise time is determined by the input current available from the driver. For the μA9614, the available current is ~ 90 mA, causing the SH0013 to deliver a peak output current of ~ 550 mA. Adding input resistance lowers the available input current, increasing the rise time. When the output is fully ON (Logic "1"), the input capacitor will continue to discharge; the driver output impedance, coupling resistor (if any) and the SH0013 input impedance combine in series to determine the output pulse width. When the input current has decayed to a level which is insufficient to keep the input transistor saturated, it begins to turn off and the upper output transistor (Q_2) begins to charge the load capacitor in some fall time (t_f). Fall time is affected by the load capacitance and the input coupling components (R_{IN}, C_{IN}).

Typical pulse widths are shown in Figures 1–5 for various drivers versus coupling capacitance and resistance.

RISE TIME/FALL TIME LIMIT

The maximum transient output current that the SH0013 may conduct is ±600 mA. More current than this might cause permanent damage or shorten the life of the device. The transient output current is given by

$$I_{peak} = \frac{\Delta V}{t} \times 0.8 \times C_L \qquad \text{Eq. 1}$$

where ΔV = output swing, $t = t_r$ or t_f (10% to 90%), C_L = load capacitance, 0.8 = fraction of output swing from 10% to 90%.

Refer to Figure 6 for absolute minimum computed rise/fall times; see Figure 7 for typicals. Fall time is affected somewhat by the coupling elements as shown in Figure 8. See Figure 9 for rise/fall time variations with temperature.

MAXIMUM CAPACITIVE LOADING

The maximum capacitive load is determined by the maximum allowable dissipation of the TO-8 type Package, output swing, frequency and duty cycle. Duty cycle and supply difference determine the average internal power dissipated in the 1100Ω resistors (P_{dc}).

$$P_{dc} = \frac{(V^+ - V^-)^2}{1100} \times (\text{Duty Cycle}) \qquad \text{Eq. 2}$$

where duty cycle refers to the fraction of the cycle spent in the logical "1" state.

Figure 11 shows computed average internal power as a function of duty cycle and supply difference. Frequency, output swing and load capacitance determine the transient power dissipated in Q_1, and Q_2 due to charging and discharging the load capacitance. Transient power (P_{ac}) may be computed as

$$P_{ac} = C\,(\Delta V)^2\, f \qquad \text{Eq. 3}$$

where ΔV = output swing. For 16V or 20V supplies, see Figures 12 or 13.

For other supply voltages, use Eq. 3. The maximum allowable power dissipation versus ambient temperature for the TO-8 type Package is shown in Figure 10. The sum of the average internal power (P_{dc}) and the transient power (P_{ac}) is limited by the maximum allowable package dissipation.

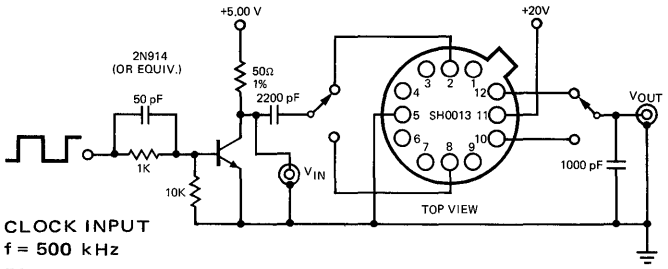
$$P_{TOTAL} = P_{ac} + P_{dc} \leq P_{max} \qquad \text{Eq. 4}$$

The maximum load capacitance may be easily determined using Eqs. 1, 2, 3, and 4.

APPLICATION CIRCUITS

Figures 17 and 18 show typical application circuits. Figure 17 shows a full two-phase system, where the coupling resistance and capacitance set the pulse width. Figure 18 shows a method of dc level shifting for +5V, –12V MOS systems. Note that in this circuit the SH0013 output waveform is identical to the waveform applied to the 9002.

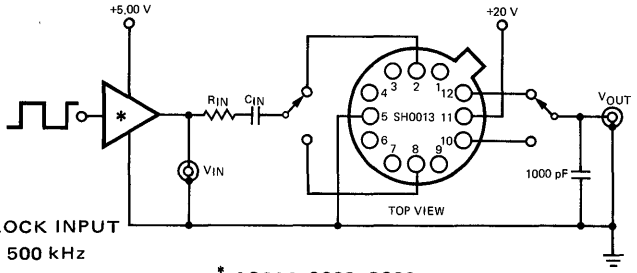
STANDARD AC TEST CIRCUIT



CLOCK INPUT
f = 500 kHz
50% DUTY CYCLE
AMPLITUDE = 5V
$t_r = t_f \leqslant 10$ ns

Fig. 14

TYPICAL APPLICATION AC TEST CIRCUIT

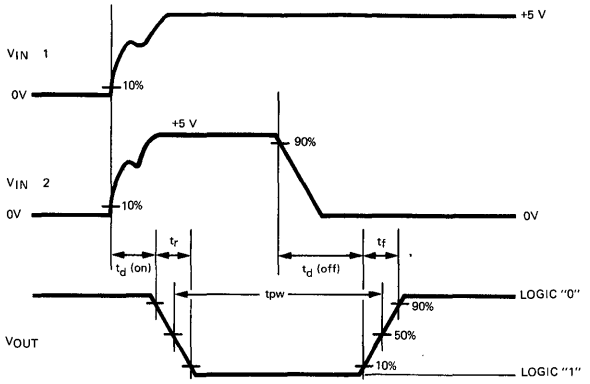


CLOCK INPUT
f = 500 kHz
50% DUTY CYCLE
AMPLITUDE = 5 V
$t_r = t_f \leqslant 10$ ns

*μA9614, 9009, 9002

Fig. 15

TIMING DIAGRAM

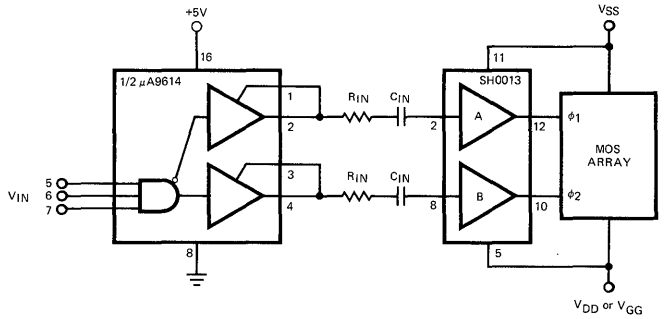


V_{IN1}: RC INPUT NETWORK DETERMINES t_{pw}. ALL PARAMETERS APPLICABLE EXCEPT t_d off.
V_{IN2}: INPUT PULSE WIDTH DETERMINES t_{pw}.

Fig. 16

TWO-PHASE MOS CLOCK DRIVER

CIRCUIT



WAVEFORMS

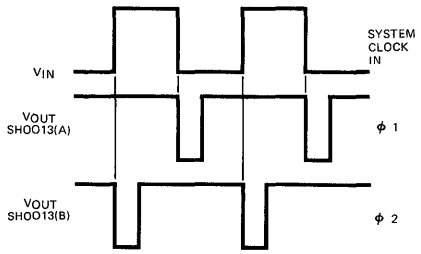


Fig. 17

DC LEVEL SHIFTING

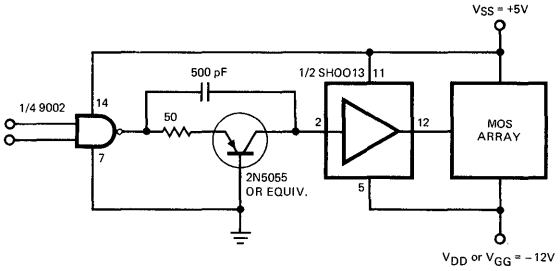
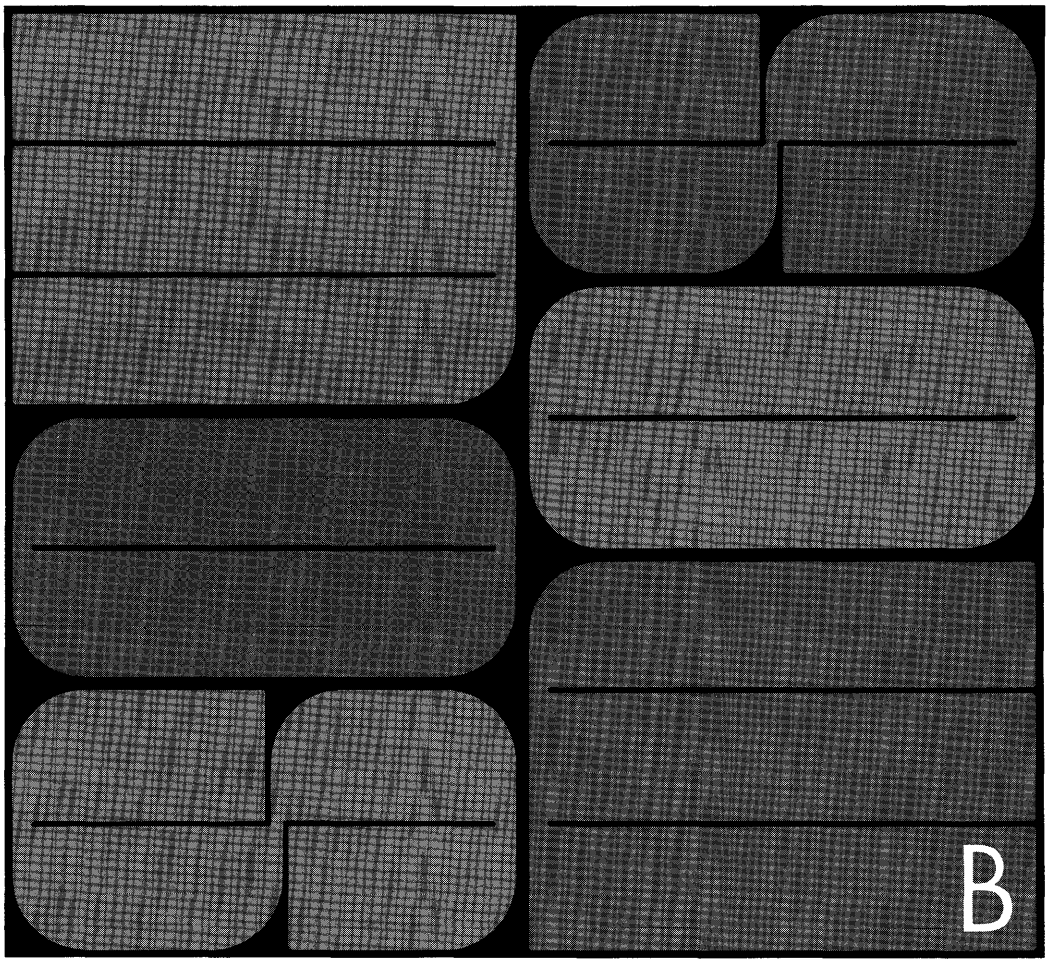


Fig. 18

PPS 25–Programmed Processor System



APPENDIX B

PPS 25 — PROGRAMMED PROCESSOR SYSTEM

INTRODUCTION

MOS/LSI technology was first applied commercially in electronic desk top calculators. In the late 1960's, virtually every calculator manufacturer had new electronic designs on the market that utilized MOS/LSI chips. The low cost potential of MOS/LSI made possible what is now acknowledged to be a revolution in calculator system design.

The advances of MOS/LSI technology in the 1970's have made possible both increased circuit complexity and performance. In this decade a similar equipment revolution is foreseen in the minicomputer and data processor systems field where required computational speed and logic density are higher than in most calculator systems.

To meet the needs of this market, Fairchild developed a family of micro-programmed MOS/LSI processor blocks called the PPS 25 (Programmable Processor System).

Equipment engineers have long recognized the desirability and flexibility of designing digital systems using a micro-programmed processor as the heart of the design. Such systems are very practical in that they can be readily programmed around specific system requirements. Unfortunately, the size and cost of minicomputers to date have limited their application to relatively large systems. However, with the availability of the PPS 25, small systems can be readily and economically designed. In fact, it is now possible for the equipment designer to develop small programmable digital processing systems for under $50.

The PPS 25 is a buss-oriented system which can be used in a wide variety of ways in data processors. The heart of the system (see *Figure B-1*) is the 3805 Arithmetic Unit and the 3806 Function and Timing Unit, which together perform all timing, control and arithmetic functions. Auxiliary to these chips is the 3810 ROM which stores micro-programs and data look-up tables. The 3808 and 3809 shift register memory devices store data. Keyboards can be attached by using the 3803 and 3807 input devices while data output for displays or other communication equipment is provided by the 3811.

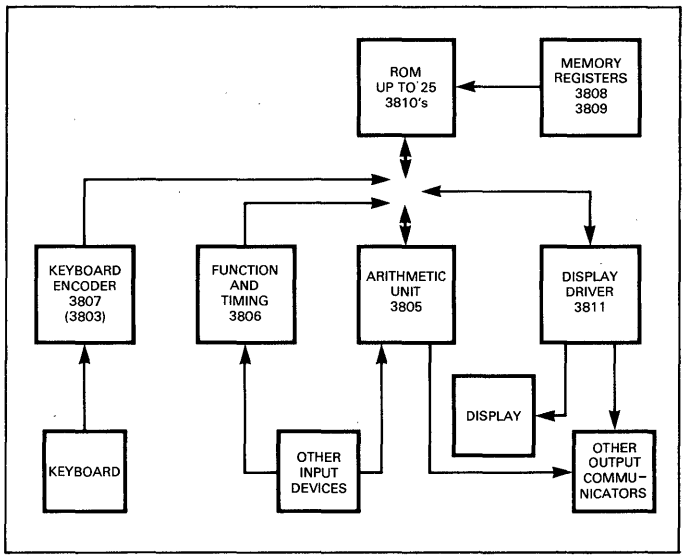


Fig. B-1. PPS-25 Micro-Programmed Processor System

Although the set is comprised of standard devices, it can be personalized to meet unique systems needs by micro-programming the 3810 ROM. The result is system and design economy through the use of standard components, but with customized design through the customer's proprietary ROM code patterns.

FEATURES OF THE PPS 25 SYSTEM

The PPS 25 system was designed to fill the gap between intermediate to upper-end calculators and minicomputers. It substitutes a few MOS/LSI packages where normally several hundred TTL MSI or SSI packages would be required.

The PPS 25 system has a versatile instruction set which permits the system to perform a wide variety of different functions. The basic operating features of the set are summarized below.

- BCD Serial/Parallel Processing Unit with 95 Instructions
- 25-Digit Serial, 4-Bit Parallel Organization
- 62.5 μs Word Time
- 2.5 μs Bit Time
- Programmable Time Enable Patterns Provide Versatile Data Field Selection Within the 25-Digit Word
- 4-Level Subroutine Nesting
- Both 2 and 3-Way Conditional Branch Structure
- External Interrupt Capability
- High Speed Operation Assured by
  - — Basic Serial/Parallel Arithmetic Unit
  - — Overlapped Fetch and Execute Instruction Cycle
  - — Separate Micro-instruction and Data Busses
- Up to Seven 25-Digit Memory Registers Available with Arbitrary Expansion Provided
- Up to 26 Programmable ROMs — 256 x 12 Bits Each
- Input Keyboard Capability for Up to 61 Keys and 32 Mode Switches
- Standard Output Display Chip Available for 16-Digit Display or Communications Interface with Provision for Other Custom Outputs
- Versatile Data Buss Structure Provides Flexible I/O Interface Expansion

APPLICATIONS OF THE PPS 25 SYSTEM

The PPS 25's flexible set of 95 instructions permits the system to perform a wide variety of functions. Examples of systems where the PPS 25 can be employed are:

Upper-End Scientific Calculators

Scientific calculators formed with these MOS/LSI blocks handle up to 25-digit numbers. They can be programmed to handle either fixed point, floating point, or scientific notation, and, in their basic form, will add, subtract, multiply, divide and take square root. They also can perform complex arithmetic functions such as sine, cosine, and log. The programmable ROMs provide a great number of different capa-

bilities. Multiply, for example, can be performed with any one of a number of algorithms. Furthermore, the word length need not be 25 digits. The blocks can be used to build a calculator with any number of digits up to 25.

Internally, the chips handle 25-digit words (stored in four parallel 25-bit shift registers). The word length actually used and the format within the word are entirely optional. A possible format for a calculator with scientific notation would be to devote three digits to the exponent and its sign, leaving 21 digits for the mantissa and one digit for its sign.

All numbers are stored and processed in binary coded decimal form. These four bits are processed in parallel fashion, while the digits are processed in series. The system can be clocked at a maximum rate of 400 kHz. At this rate the digit and word times are 2.5 and 62.5 μs respectively.

Up to 61 keys and 32 mode switches can be handled by the standard keyboard interface circuit, and up to 16 digits of display can be controlled by the 3811 output chip.

Control Systems

Because of the micro-program flexibility, the PPS 25 system can be used in process control systems, vending machine systems, medical instrumentation, numerical machine control, traffic light controllers, and in virtually all medium speed programmed control systems.

Computer Systems

The PPS 25 system is also organized for high speed calculations and data processing. Basic features — serial/parallel word structure, overlapped fetch and execute, and separate data and micro-instruction busses — were designed-in. This was done to extend the application of the set into the fields of electronic point-of-sale terminals, cash registers banking terminals, small business machines, etc. For example, the addition of two 25-digit numbers can be executed in 62.5 μs, and the multiplication of similar numbers can be accomplished in less than 50 ms.

Peripheral Systems

This micro-programmed system is also ideally configured for many peripheral applications. If keyboard entry is required, the 3803 and 3807 devices provide a direct interface, with full n-key rollover and anti-bounce on up to 61 keys, plus 32 mode switches. Other forms of input data can be fed directly into the data source buss. If digit display of up to 16 digits is required, the 3811 device provides the necessary interface; or multiple 3811 devices can serve as a general output communication link.

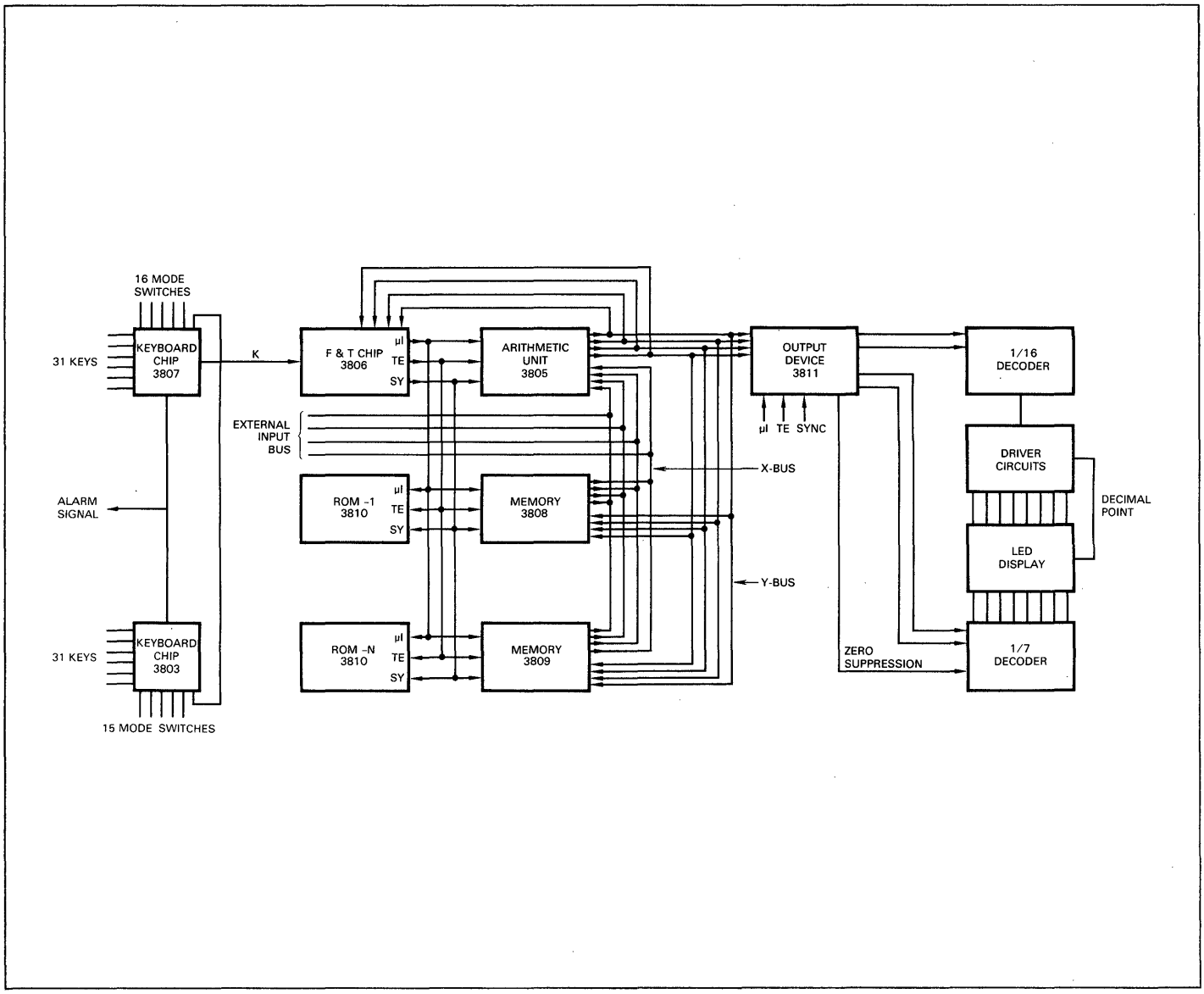


Fig. B-2. Typical Processor System

If special interfaces are required, such as printers or mag card readers, custom interfaces can be provided directly from the destination buss or ROMs can be utilized to emulate the desired interface within the structure of the system.

DESCRIPTION OF THE PPS 25 SYSTEM

The basic MOS/LSI building blocks used in the PPS 25 System are listed in *Table B-1*, along with their pinouts. All of these devices are manufactured with P-channel silicon gate technology. There are 2-phase dynamic logic circuits incorporated. Standard +5 V, -10 V and ground supplies are required. Full TTL compatibility is provided at all external I/O interfaces.

The building blocks are all designed as buss-oriented devices. *Figure B-2* shows how they are connected together to form a typical processor system. As this figure shows, there are two data busses. The X-data buss is the source (or input) data buss. It is four bits wide (BCD), and provides the input for each 25-digit word being processed. The Y-data buss is the destination (or output) data buss. The micro-instruction buss is used to fetch a 12-bit micro-instruction from the selected ROM. Timing for the fetch and execute cycle are provided from the 3806 function and timing chip.

The time enable signal (TE) provides a data field selection within the 25-digit word, as specified by the customer time enable patterns. The K line completes the system. This is the keyboard buss which connects scanned data from the keyboard devices into the 3806 device.

The simplified operation of each of the devices is as follows:

3807/3803 Keyboard Devices

The basic keyboard device is the 3807. The 3803 extends the keyboard capabilities beyond 32 keys. The function of the 3807 device is to generate a 5-bit code for each key that makes a transition from an inactive state to an active state. This 5-bit code is stored on the chip until a command occurs in the program, instructing the chip to supply the 5-bit code to the addressing register in the 3806 function and tuning chip. An anti-bounce feature is provided by a sample and hold circuit in the keyboard scanner.

The keyboard is full "legato", provided that an external diode is used with each key. That is, new entries can be made without having to release previously depressed keys, and up to two key strokes can be stored in their proper sequence by the keyboard during the time the system is processing previous data.

3805 Arithmetic Chip

This chip contains the adder/subtractor plus a 25-digit memory register. The 3805 device, along with auxiliary memory devices 3808 and 3809, receive micro-instructions from the 3810 ROMs. These micro-instructions contain a data source address, a data result destination address, and an operation code. The instructions allow subtractions, additions, or transfers to take place between registers. Incrementing, decrementing, complementing, and clearing of any of the seven registers and other operations can also be performed. Data can be entered either externally or created internally by the use of a "load immediate" micro-instruction.

3806 Function and Timing Unit

This device provides the address and control logic for the PPS 25 system. Included functionally on this device are the following:

- Instruction address register
- Micro-instruction address adder
- Program branch decision logic
- Two 25-bit status registers
- Pointer and status counters
- Time enable pattern generator
- Master timing circuit
- 4-level nested subroutine linkage

This logic provides the traffic control function for the entire PPS 25 system, in that it contains the master timing counter and generates the sync signal.

For example, the time enable portion of the instruction is used to select the portion of the word upon which a given command is to be executed. There are six programmable time enable patterns available, each called up by a different code.

The status registers are used for storing return addresses for subroutine calls, storing program flags, and storing mode control switch status.

3808/3809 Memory Registers

These devices each contain three 4-bit BCD parallel, 25-digit serial register memories. The registers, which can be directly addressed by the arithmetic instructions, work in conjunction with the 3805 arithmetic unit described above.

3810 ROM

The micro-instructions for the PPS 25 are contained in the 3810 read-only memory device. As many as 25 of these devices may be incorporated in parallel in a single system. All ROMs in a system simultaneously receive an 8-bit address, and the selected ROM shifts out the selected 12-bit instruction. Each 3810 device contains 256 x 12 bits, and are mask programmable.

Data (including binary) stored in the ROM program can be transferred to the accumulator. This data is useful in the generation of constants, addresses, etc.

3811 Output Device

The 3811 device provides the necessary latches for receiving, storing, and transmitting the BCD representation of a character. A position counter provides an output code for 1 of 16 positions, necessary to multiplex up to 16 display elements. Decimal point, sign, and general purpose programmed flag outputs are also provided as shown. Leading zero suppression and blanking control are also provided within the logic of the 3811.

Instruction Set

Micro-instructions are classified into three types in the PPS 25 systems: arithmetic, control, and input/output. Arithmetic instructions relate to data movement and manipulation under field selection control of the time enable patterns. Control instructions relate to status conditions affecting ROM address selection and branch structure. There are 64 I/O instructions, many of which are available for customer specified interface requirements.

TABLE B - 1

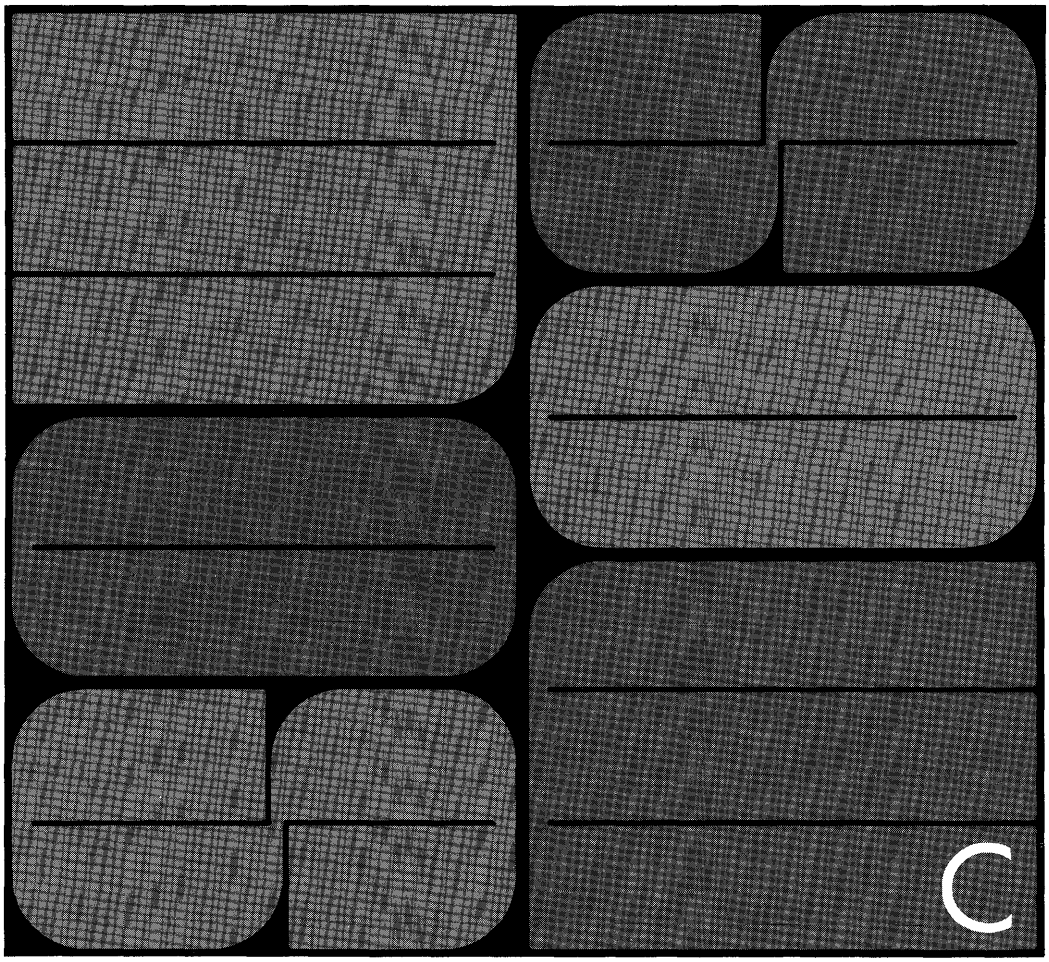
PPS 25 DEVICE PINOUTS

DEVICE	3803 KEYBOARD	3807 KEYBOARD	3805 ARITHMETIC	3806 F & T	3808 MEMORY	3809 MEMORY	3810 ROM	3811 DISPLAY
PKG. TYPE	7Q	7Q	7T	7R	7K	7K	7K	7R
NO. PINS	40	40	18	24	16	16	16	24
1	D_2	D_2	Y_3	V_{SS}	X_0	X_0		A_1
2	D_1	D_1	X_3		V_{SS}	V_{SS}		A_0
3	V_{SS}	V_{SS}	V_{SS}	V_{GG}	V_{GG}	V_{GG}	V_{SS}	P_1
4	V_{GG}	V_{GG}	X_2	P_2	V_{DD}	V_{DD}	MI	V_{GG}
5	V_{DD}	V_{DD}	X_1	TEN	Y_0	Y_0	MIO	P_2
6			X_0	V_{DD}	Y_2	Y_2		V_{DD}
7	R_5	R_5	V_{DD}	FLAG	SYNC	SYNC	V_{DD}	MI
8	R_4	R_4	P_2	F_1	TEN	TEN		TEN
9	R_6	R_6	V_{GG}	BOROW	P_2	P_2		SYNC
10	R_3	R_3	P_1	TENIN	P_1	P_1		V_{SS}
11	R_7	R_7	MI	MI	X_2	X_2		Y_0
12	R_2	R_2	BOROW	P_1	MI	MI	P_2	Y_1
13	R_8	R_8	SYNC		X_3	X_3	V_{GG}	Y_2
14	R_1	R_1	FLAG	BSTN	Y_3	Y_3	P_1	Y_3
15			TEN	SFT	Y_1	Y_1	SYNC	BN
16	TEST	TEST	Y_0	PFTN	X_1	X_1		K_0
17			Y_1	S25TN				K_1
18	MI	MI	Y_2					K_2
19				Nu				K_3
20				TSY				S
21				KN				M
22	P_1	P_1		MIO				DP
23	P_2	P_2		SYNC				A_3
24				TEST				A_2
25								
26								
27	SYNC	SYNC						
28	S_8	S_8						
29	S_7	S_7						
30	S_6	S_6						
31	S_5	S_5						
32	S_3	S_3						
33	S_4	S_4						
34	S_2	S_2						
35	S_1	S_1						
36								
37	K	K						
38	A	A						
39	D_4	D_4						
40	D_3	D_3						

ARITHMETIC INSTRUCTION TABLE

MNEMONIC	FUNCTION	OPERATION DESCRIPTION
ADD	BCD Addition	The contents of the source register are added to the accumulator and the result is stored in the destination register.
SUB	BCD Subtraction	The contents of the source register are subtracted from the accumulator and the result is stored in the destination register.
MOV	Move	The contents of the accumulator are transferred to the destination register. The contents of the source register replace the original contents of the accumulator.
COM	BCD Complementation	The contents of the source register are complemented (subtracted from zero) and the result is stored in the destination register.
INC	Increment	The contents of the source register are incremented by one and the result is stored in the destination register.
DEC	Decrement	The contents of the source register are decremented by one and the result is stored in the destination register.
LSH	Left Shift	The contents of the selected register are shifted left one digit. The least significant digit position is cleared to zero.
CLR	Clear	The contents of the selected register are cleared.
RSH	Right Shift	The contents of the selected register are shifted right one digit. The most significant digit position is cleared to zero.
SLI	Shift Load Immediate	The contents of the accumulator are shifted left one digit. A 4-bit character from the micro-instruction is loaded into the low digit position. The result is stored in the accumulator.
CR	Change ROM	This command selects a unique ROM for program execution.
BOC	Conditional Branch	When the branch instruction is preceded by a test or an interrogate instruction, conditional branching is provided.
BRU	Unconditional Branch	When the branch instruction is not preceded by a test or an interrogate instruction, the branch instruction acts as an unconditional branch.
NOP	No Operation	No Operation.
SSB	Set Status Bit	Specifies which status bit is to be set to a "1".
RSB	Reset Status Bit	Specifies which status bit is to be reset to a "0".
CSR	Clear Status Register	This execution resets all 25 status bits to "0".
ISB	Interrogate Status Bit	This instruction is used to determine the status ("1" or "0") of a particular bit in the status register.
CSB	Complement Status Bit	Causes the addressed status bit to be conditionally complemented.
EXS	Exchange Status	Exchanges the contents of the two status registers with each other.
STM	Store Modes	This instruction causes the function and timing chip to accept and store mode switch data.
SPT	Set Pointer	Causes pointer counter to be forced to a selected one of 25 positions.
IPT	Interrogate Pointer	Interrogates position of pointer.
PLF	Pointer Left	Moves pointer one position to left
PRT	Pointer Right	Moves pointer one position to right.
SA2	Store Address #1	Causes current address A in addressing register to be stored.
RA1	Recall Address #1	Fetches eight bits stored by SA1 and places them back in addressing register.
SA1	Store Address #2	Causes current address A in addressing register to be stored.
RA2	Recall Address #2	Fetches eight bits stored by SA2 and places them back in addressing register.
BR3	Branch 3	Causes 3-way conditional branch mode to occur.
BR2	Branch 2	Causes 2-way conditional branch mode to occur.
XI/O	Input/Output Commands	There are up to 64 I/O commands available to control customer input/output devices.

SPRINT Accounting Calculator Set



APPENDIX C

SPRINT ACCOUNTING CALCULATOR SET

SPRINT ACCOUNTING CALCULATOR SET

Introduction

The SPRINT Calculator Set provides the logic for a low cost calculator which performs basic accounting functions. This set's calculating (accounting) capability is far stronger than basic 4-rule calculators on the market today. It performs basic arithmetic functions (add, subtract, divide, multiply) plus a rounded percentage function that eliminates the need for floating point operation.

Three registers permit invoicing, discount and net amounts, chain discounts, gross weights of shipments and payroll problems without any intermediate copy steps. Most low cost calculator sets require intermediate copy and re-enter steps to perform a grand total (sum of products) calculation. The third register also allows the constant to be used with all functions instead of just multiply and divide.

A special recall key permits reviewing a number previously displayed. A second depression of the recall key restores the original display. The remainder key allows the user to view the remainder following a division, the product following a percentage, the unrounded percentage following a multiplication and the first operand following an addition or a subtraction. A second depression of the remainder key restores the original display. Use of the recall or remainder key allows a new display to be used as an operand (e.g., sum of remainders of multiple divisions which is useful in residue theory).

FEATURES

- 5 Rules + - X ÷ %
- One memory (sum of products without intermediate copy steps)
- Locked constant on all functions
- 74 total parts required to build working calculator (Everything but power supply and pc card)
- Special keys %, REMainder, RECall, DP(decimal point), LOCK, DUPlicate
- Negative sign for true credit balance
- Chain calculations
- Register exchange function
- Power on clear input
- 00 key for fast entry
- Accounting type operation
- Leading zeros are small size
- Remainder register can be used as fourth register in certain applications (looking at previous accumulation)
- Automatic scaling of any displayed number by entering zero or double zero

OPERATING INSTRUCTIONS

1. *CLR* — Depress once — Clears entry
   Depress twice — Clears calculator before each new application

2. *ADD, SUBSTRACT, MULTIPLY, DIVIDE, PERCENT* —
   Set first number — Depress ENTER
   Set second number — Depress + - X ÷ %

3. *REM* — Depress once — Displays REMAINDER in DIVISION, UNROUNDED % in MULTIPLICATION, PRODUCT in PERCENTAGE, FIRST OPERAND in ADDITION or SUBTRACTION

4. *REC* — Depress once — Recalls previous number displayed
   Depress twice — Recalls number displayed before REC

5. *ACCUMULATE* — Depress +

6. *DP* — Fixes decimal point

7. *CONSTANTS* —
   Set number to be used as constant
   Depress DUP to duplicate entry
   Engage LOCK switch to lock constant

   (Constant can now be used in + - X ÷ %. Be sure to disengage LOCK switch after using LOCKED CONSTANT mode.) A double depression of CLR will clear everything but the LOCKED CONSTANT

NOTE: Blinking display — indicates batteries need recharging.

FUNCTIONAL CONTROL DESCRIPTION

1. *ON/OFF SWITCH*

2. *FUNCTIONAL KEYBOARD* — Includes a double zero key for fast entry.

3. *CLEAR KEY (CLR)* — One depression clears the entry or the number displayed.
   Two depressions clear the calculator before each new application.

4. *ENTER KEY* — Used to enter the first number of any calculation.

5. *PLUS KEY (+)* — Adds the first number set into the machine to second number indexed on the keyboard.

6. *MINUS KEY (-)* — Subtracts the second number indexed on the keyboard from the first number set into the keyboard.

7. *MULTIPLICATION (X)* — Multiplies the first number set into the machine by the second number indexed on the keyboard.

8. *PERCENT KEY (%)* — Computes an automatic rounded percentage after indexing a percent factor.

9. *DIVISION KEY (÷)* — Divides the first number set into the machine by the second number indexed on the keyboard.

10. *REMAINDER KEY (REM)* — After division, one depression displays the remainder; two depressions display the quotient agan.

11. *RECALL KAY (REC)* — *One* depression recalls the previous number displayed. Two depressions recall the number displayed before recalling.

12. *LOCKED CONSTANT MODE (LOCK)* — Locks in a constant number which can be used in addition, subtraction, multiplication, division, and percentages. Be sure to disengage LOCK switch after using LOCKED CONSTANT MODE. A double depression of CLR will clear everything but the LOCKED CONSTANT.

13. *DUPLICATE KEY (DUP)* — Duplicates the number displayed.

14. *DECIMAL POINT KEY (DP)* — Fixes a decimal point in any position in the display at the discretion of the user.

15. *DISPLAY* — Solid state 9-digit capacity display.

16. *OVERFLOW LIGHT* — Indicates a function or entry exceeding the capacity of the unit.

17. *SIGN INDICATOR* — Indicates a negative result.

OPERATING CONTROLS

1. *OVERFLOW* — If a number is entered beyond the capacity of the machine, or if the results of a calculation exceed the capacity of the machine, the overflow indicator is automatically activated.

2. *CLEAR KEY* — There is only one Clear Key. When you begin an operation, you must clear the machine by depressing the Clear Key twice. To clear an entry, it is necessary to depress the Clear Key only once.

3. *CHANGE SIGN* — The capacity of the machine is nine digits and a sign. As soon as the machine obtains a credit balance (or negative total), a minus sign will indicate the credit amount.

4. *ENTER KEY* — When the first number of a calculation is indexed on the keyboard, the Enter Key must be depressed to register the displayed digits into the calculator.

5. *DUPLICATE KEY* — The most common applications utilizing this feature are problems involving squaring, chain discounts, and compound interest.

6. *RECALL* — This key enables you to view the previous number displayed. This number will either be the second operand of a prior arithmetic calculation (+-X÷%) or the result of a prior entry or arithmetic calculation which has been followed by a new entry.

7. *REMAINDER* — In a division problem, the REM Key enables you to view the remainder. In a percentage problem, you can obtain more accuracy by viewing the product of your calculation carried out more decimal places. In a multiplication problem, the REM Key allows you to view the unrounded percentage. In addition and subtraction, the REM Key allows you to view the first operand of each calculation.

8. *LOCK FEATURE* — The Lock Switch enables you to lock in a number and use it as a constant in a calculation involving addition, subtraction, multiplication, division, and percentages.

   Procedure: a. Set number
   b. Depress Enter Key
   c. Set percent digits
   d. Depress Percent Key

9. *PERCENT KEY* — To calculate a percentage problem, enter the percent digit and then depress the Percent Key. The machine will then compute the percentage and automatically round it off.

10. *PLUS KEY* — By depressing the Plus Key, the calculator adds the first number set into the machine to the second number indexed on the keyboard (the number currently on display). For subsequent numbers, it is necessary to repeat the operation.

    Procedure: a. Set first number
    b. Depress Enter Key
    c. Set second number
    d. Depress Plus Key

11. *MINUS KEY* — A touch of the Minus Key causes the calculator to subtract the second number indexed on the keyboard (the number currently on display) from the first number set into the machine.

    Procedure: a. Set first number
    b. Depress Enter Key
    c. Set second number
    d. Depress Minus Key

12. *MULTIPLICATION KEY* — The Multiplication Key causes the calculator to multiply the first number set into the machine by the second number indexed on the keyboard (the number currently on display).

    Procedure: a. Set first number
    b. Depress Enter Key
    c. Set second number
    d. Depress Multiplication Key

13. *DIVISION KEY* — The Division Key causes the calculator to divide the first number set into the machine by the second number indexed on the keyboard (the number currently on display).

    Procedure: a. Set first number
    b. Depress Enter Key
    c. Set second number
    d. Depress Division Key

14. *DECIMAL POINT MARKER* — The decimal point marker is a convenience for the user. It can be set for any calculation at the discretion of the user.

15. *KEYBOARD* — The SPRINT is equipped with nine keys to set digits 1 - 9 and with two keys to set single and double zeros. The double zero key speeds figure entry.

KEYSTROKE EXAMPLES

ARITHMETIC OPERATIONS

TABLE C-1

PROBLEM	KEY	DISPLAY
Addition	CLR	00
123 + 15 = 138	CLR	00
	123	123
	ENTER	123
	15	15
	+	138
Addition with Constant	CLR	00
120 + 142 = 262	CLR	00
195 + 142 = 337	142	142
	DUP	142
	set LOCK	142
	120	120
	+	262
	195	195
	+	337
Subtraction	CLR	00
321 - 301 = 20	CLR	00
	321	321
	ENTER	321
	301	301
	-	20
Subtraction with Constant	CLR	00
450 - 256 = 194	CLR	00
200 - 256 = -56	256	256
	DUP	256
	set LOCK	256
	450	450
	-	194
	200	200
	-	-56

KEYSTROKE EXAMPLES (Continued)

PROBLEM	KEY	DISPLAY
Multiplication	CLR	00
12 X 1234 = 14,808	CLR	00
	12	12
	ENTER	12
	1234	1234
	X	14808
Multiplication with Constant	CLR	00
	CLR	00
1234 X 189 = 233, 226	189	189
1597 X 189 = 301, 833	DUP	189
	set LOCK	189
	1234	1234
	X	233226
	1597	1597
	X	301833
Division	CLR	00
6055 ÷ 42 = 144 (Remainder 7)	CLR	00
	6055	6055
	ENTER	6055
	42	42
	÷	144
	REM	7
Division by Constant	CLR	00
555 – 25 = 22 (Remainder 5)	CLR	00
	25	25
250 – 25 = 10	DUP	25
	set LOCK	25
	555	555
	÷	22
	REM	5
	250	250
	÷	10

KEYSTROKE EXAMPLES (Continued)

PROBLEM	KEY	DISPLAY
Percentage	CLR	00
700 X 25% = 175	CLR	00
	700	700
	ENTER	700
	25	25
	%	175
Percentage with Constant	CLR	00
640 X 75% = 480	CLR	00
360 X 75% = 270	75	75
	DUP	75
	set LOCK	75
	640	640
	%	480
	360	360
	%	270
Squaring	CLR	00
	CLR	00
122 = 144	12	12
	ENTER	12
	DUP	12
	X	144
Cubing	CLR	00
123 = 1728	CLR	00
	12	12
	DUP	12
	X	144
	X	1728

KEYSTROKE EXAMPLES (Continued)

PROBLEM	KEY	DISPLAY
Sum of Products (Grand Total)	CLR	00
25 X 6 = 150	CLR	00
32 X 7 = 224	25	25
Sum = 374	ENTER	25
	6	6
	X	150
	+	150
	32	32
	ENTER	32
	7	7
	X	224
	+	374
Square Root	CLR	00
987654321≈31427	CLR	00
	987654321	987654321
	DUP	987654321
	DUP	987654321
Guess	30000	30000
	÷	32921
	REC	30000
	+	62921
	2	2
	÷	31460
	÷	31393
	REC	31460
	+	62852
	2	2
	÷	31426
	÷	31427
Stop when results of two divisions agree within by one in the least significant digit		

COMMERCIAL APPLICATIONS

TABLE C-2

Invoicing

Example:	Qty	Price	Extension
	24	$2.50	$ 60.00
	52	1.75	91.00
	39	1.50	58.50
		Gross Total	$209.50
		6% Discount	12.57
		Net Total	$196.93
		5% Tax	9.85
		TOTAL	$206.78

KEY	DISPLAY	RESULT
CLR	00	
CLR	00	
24	24	
ENTER	24	
250	250	
X	6000	Extension
+	6000	Accumulation
52	52	
ENTER	52	
175	175	
X	9100	Extension
+	15100	Accumulation
39	39	
ENTER	39	
150	150	
X	5850	Extension
+	20950	Gross Total
6	6	
%	1257	Discount
−	19693	Net Total
5	5	
%	985	Sales Tax
+	20678	TOTAL

TABLE C-3

Chain Discounts

Example:	Amount	Discounts	Net Amount
	$370.15	15-10-5	$269.01

KEY	DISPLAY	KEY	DISPLAY
[CLR]	00	[%]	31463
[CLR]	00	90	90
37015	37015	[%]	28317
[ENTER]	37015	95	95
85	85	[%]	26901

TABLE C-4

Total Gross Weight of a Shipment — Freight Cars

Example:

Net Weight	Tare	Gross Weight
36,040	+ 18,255	= 54,295
118,095	+ 18,255	= 136,350
240,315	+ 18,255	= 258,570

TOTAL GROSS WEIGHT = 449,215

KEY	DISPLAY	KEY	DISPLAY
[CLR]	00	[+]	54295
[CLR]	00	118,095	118095
18255	18255	[+]	136350
[DUP]	18255	[+]	190645
[LOCK]	18255	240,315	240315
36040	36040	[+]	258570
[+]	54295	[+]	449215

TABLE C-5

Payroll — Gross Pay, Total Deductions, and Net Pay

Example:

Hours Worked		44
Straight Time	$2.65 x 40 =	$106.00
Overtime	2.65 x 6 =	15.90
Gross Pay		$121.90
Deductions: Withholding		$ 18.40
FICA		2.44
Hospitalization		1.50
Union Due		.55
Total Deductions		$ 22.89
NET PAY		$ 99.01

KEY	DISPLAY	KEY	DISPLAY
[CLR]	00		
[CLR]	00	[+]	12190
265	265	1840	1840
[ENTER]	265	[ENTER]	1840
40	40	244	244
[X]	10600	[+]	2084
[+]	10600	150	150
265	265	[+]	2134
[ENTER]	265	55	55
6	6	[+]	2289
[X]	1590	[-]	9901

GENERAL DESCRIPTION

The SPRINT Calculator Set consists of five Micromosaic MOS/LSI chips. These chips provide the entire electronics logic required to implement a 9-digit desk top or hand-held battery powered portable electronic calculator. The set allows duplication of a previous entry for squaring or making copies of the currently displayed number, the recall of any previously displayed number, and a full general constant. It also includes one memory (accumulator) which makes grand total accumulation possible. Any arithmetic operation may be performed in 30 ms due to the 100 kHz clock frequency.

The input/output circuitry allows the user/designer a wide choice of data entry mechanisms (e.g., keyboards) and 7-segment displays to achieve a truly custom housing design.

The circuits are packaged in three 40-pin, one 24-pin and two 16-pin Dual In-Line hermetic packages. Two process technologies are used to produce the set — four low threshold P-channel metal gate devices and one standard P-channel silicon gate shift register. The set's electrical parameters have been designed and tested to provide direct compatibility to all devices under worst case conditions. The interconnections, inputs and outputs of the five chips are shown in *Figure C-1.*

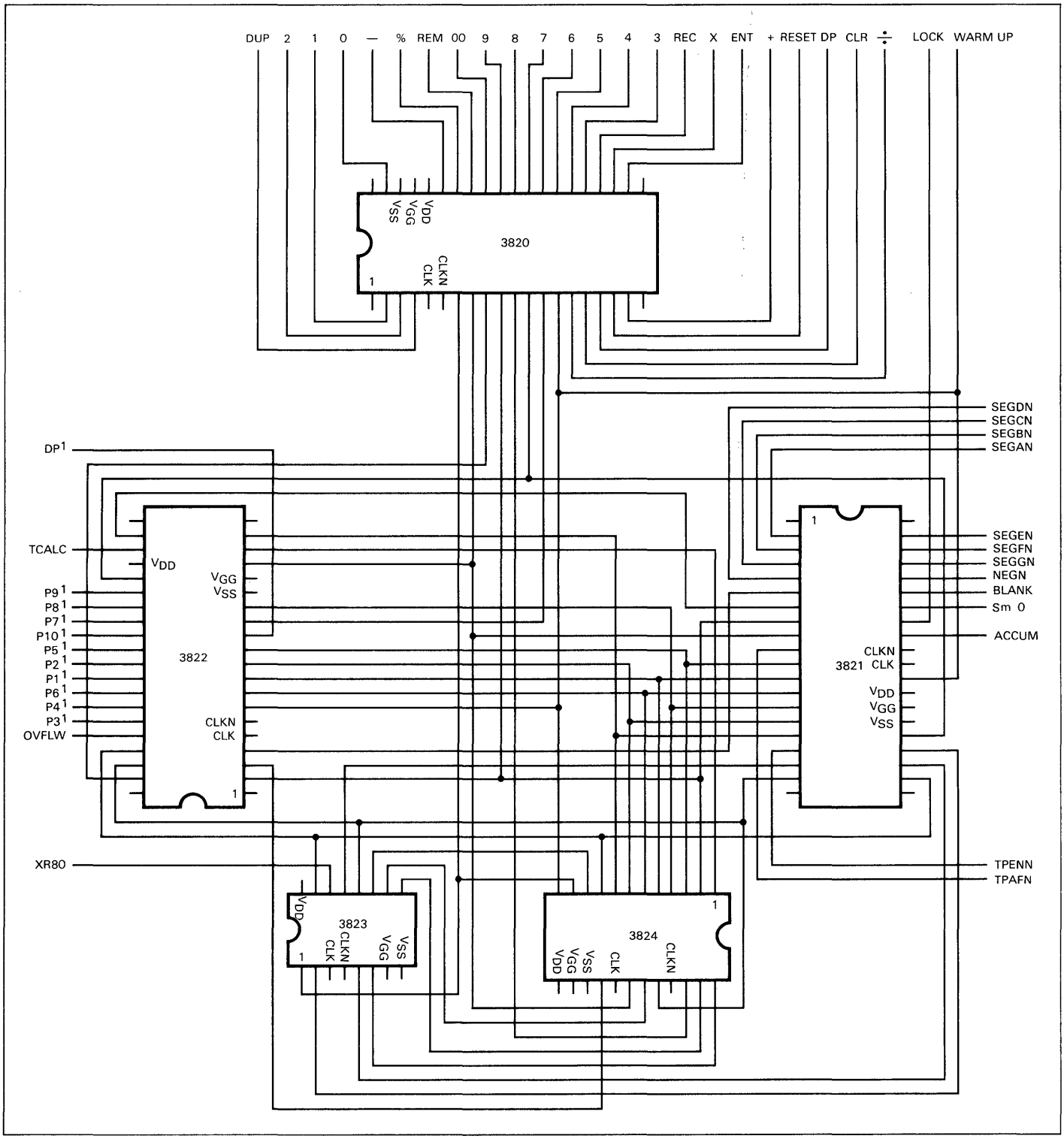


Fig. C-1. SPRINT Calculator Set Connection Diagram

KEYBOARD INTERFACE

The SPRINT can use keyboard switches that are single pole double throw or single pole single throw. The interconnection diagrams for both types of switches are shown in *Figures C-2, 3* and *4*. When using single pole single throw switches, it is necessary to generate the reset signal with external logic as shown.

In both systems, the logic accepts the first key depressed and displays that entry. All keys must be released before a second entry can be accepted by the logic. Contact bounce is not a problem since input data is latched internally and the latches and strobe generator are not reset again until all switches are released.

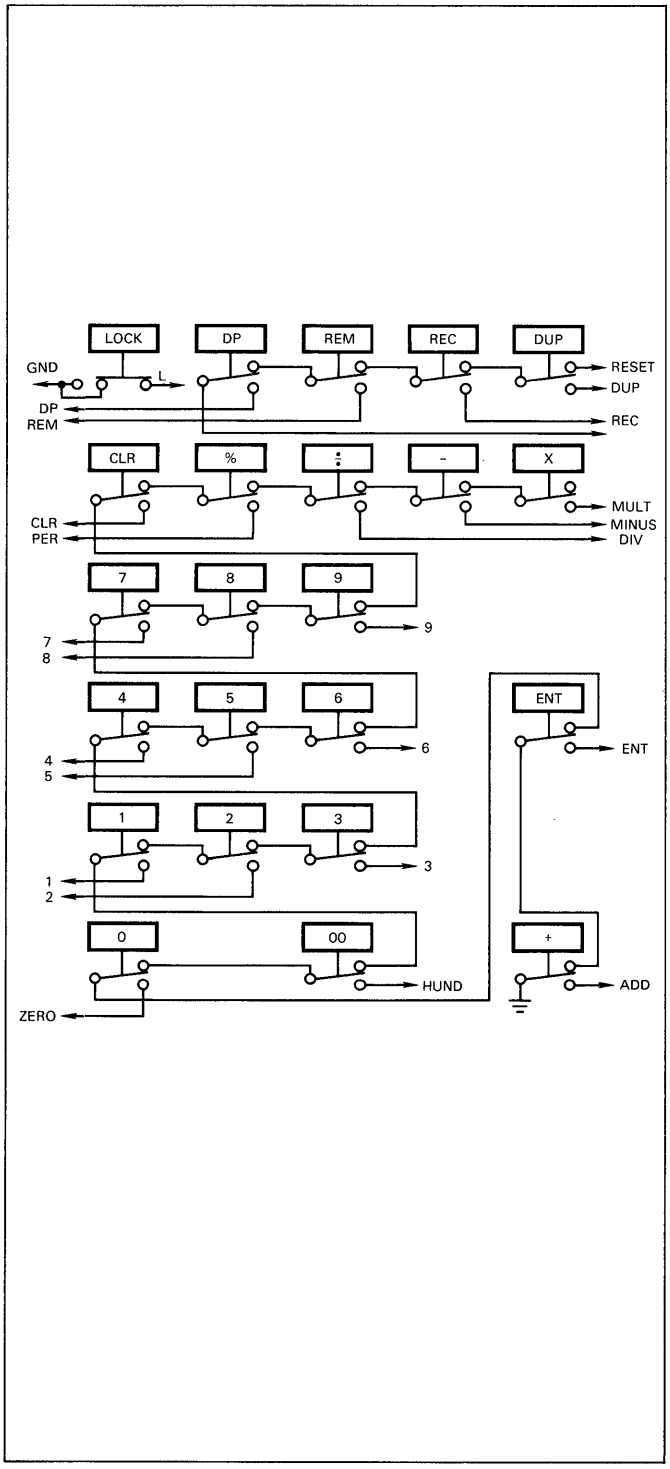


Fig. C-2. Keyboard Switch Schematic Single Pole Double Throw Switches

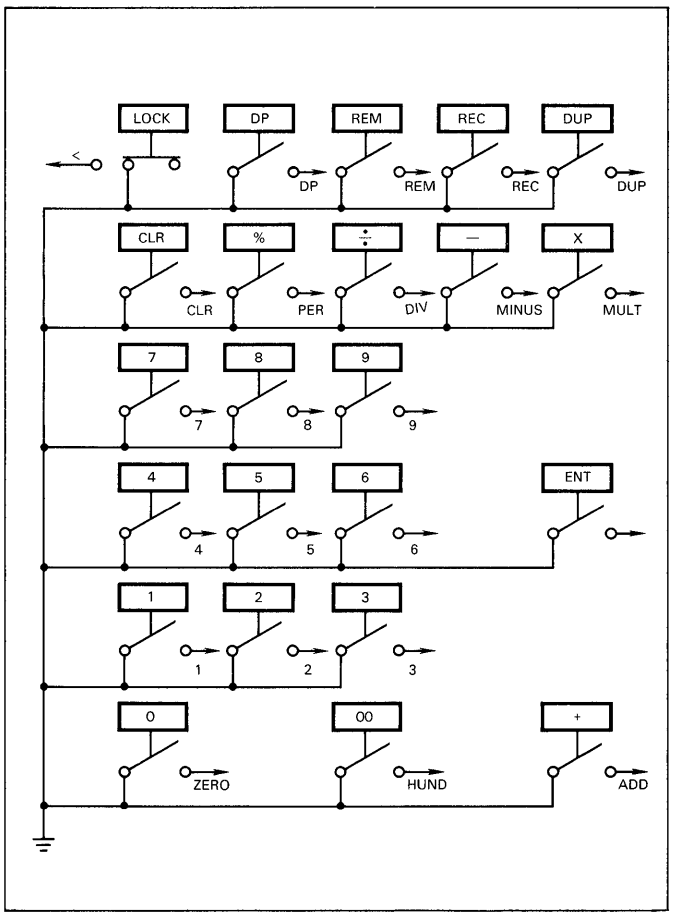


Fig. C-3. Keyboard Switch Schematic Single Pole Single Throw Switches

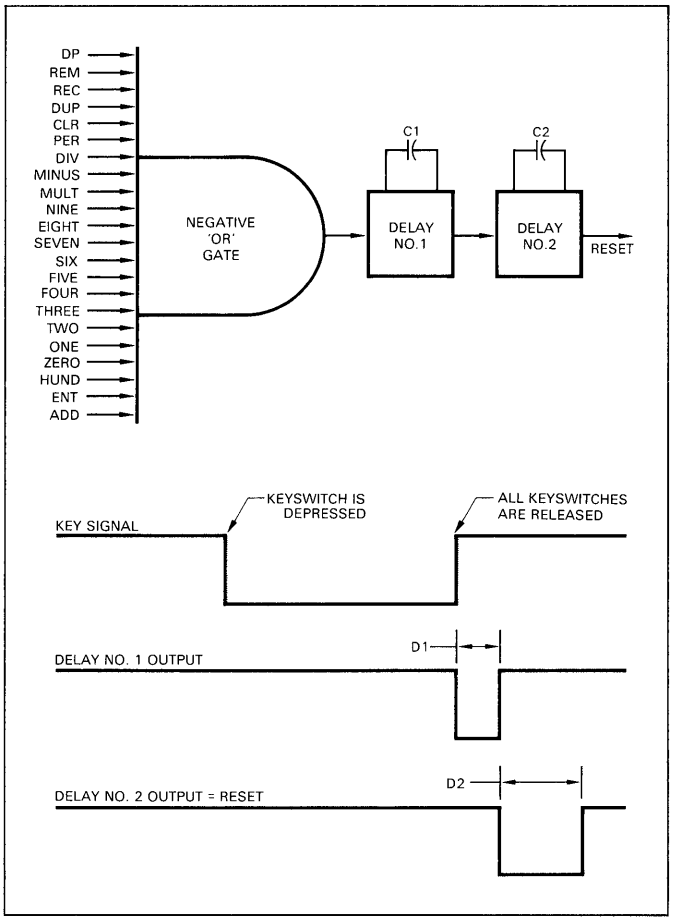


Fig. C-4. Logic Required for Single Pole Single Throw Switches

TYPICAL DISPLAY DRIVE CIRCUITS

The schematic diagram for a complete light emitting diode display system is shown in *Figure C-5*. This system can be constructed by using discrete resistors and transistors with the Fairchild MOD FND-10 single character LED digit as shown. If a complete display with drivers is desired, the same schematic has been implemented in the Fairchild MOD FND-40 display module which interfaces directly with the MOS/LSI calculator set.

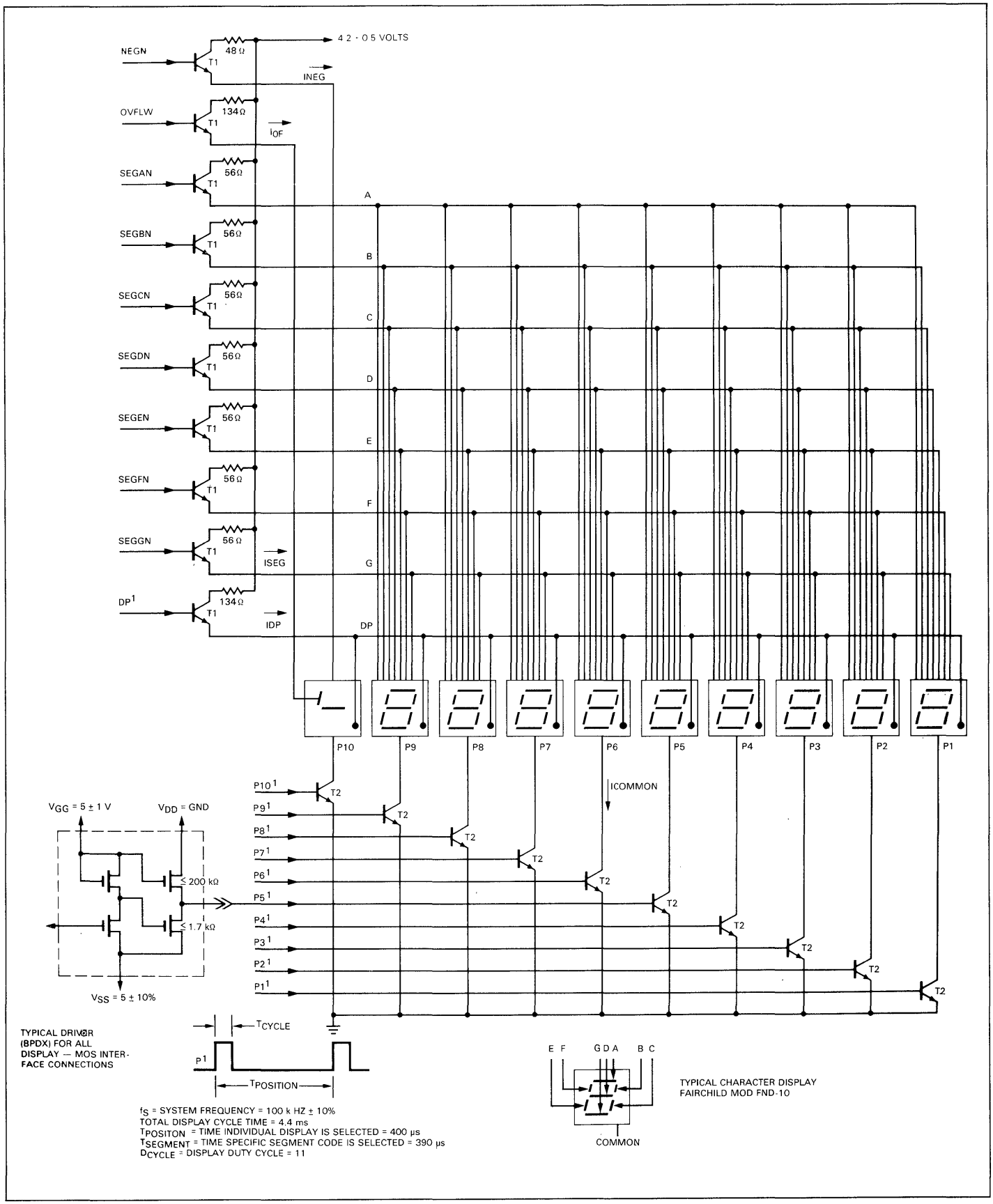


Fig. C-5. Light Emitting Diode Display System Schematic

TYPICAL DESK TOP CALCULATOR APPLICATION

By connecting the power, keyboard display, 2-phase clock, SPRINT set and warm-up network, and leaving BLANK, SMALL ZERO, ACCUM, and TEST TCALC disconnected, it is possible to have a completely operational calculator that can be functionally tested in accordance with the functional test sequence. See *Figure C-6.*

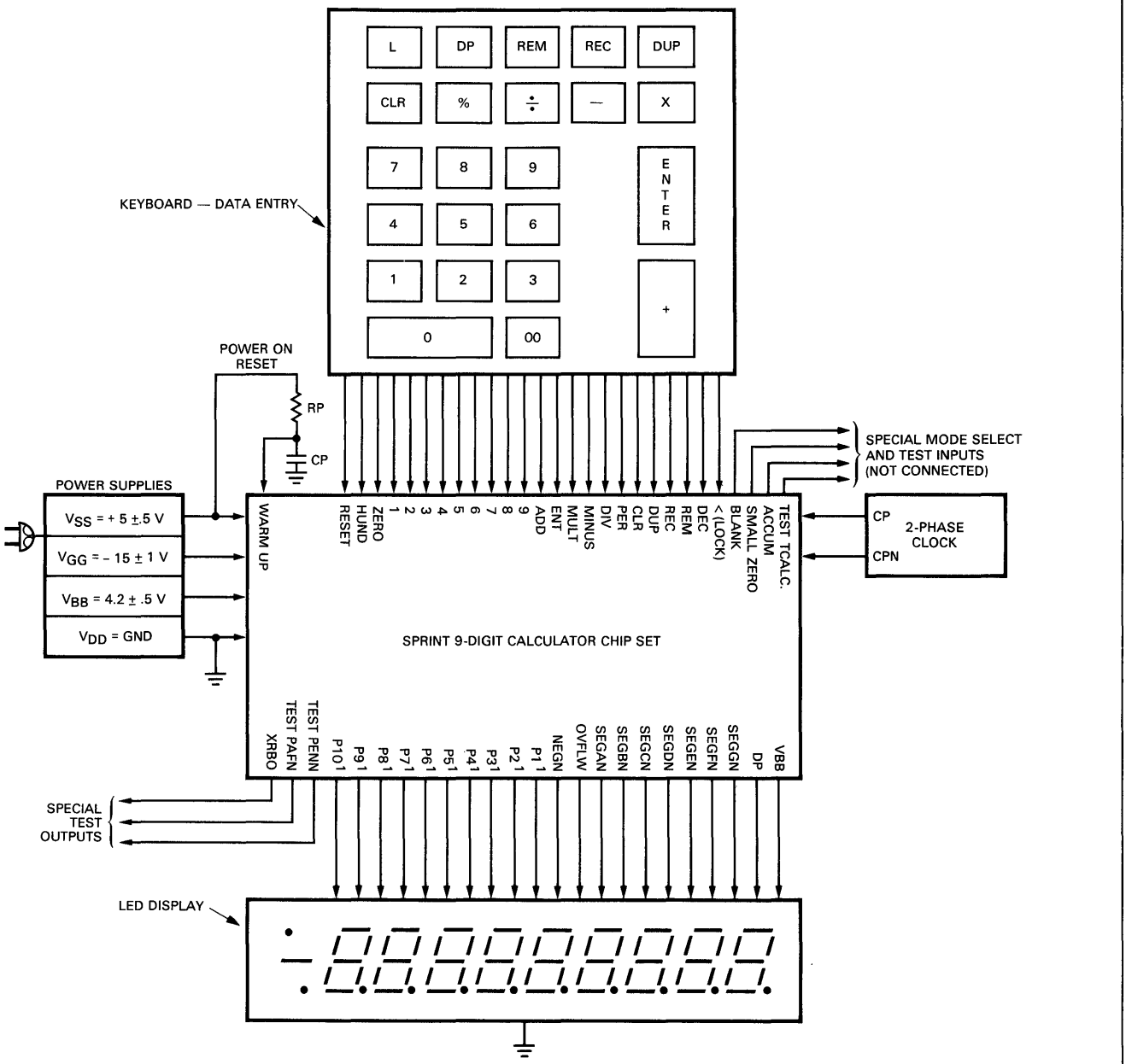


Fig. C-6. Desk Top Calculator Application Example

Functional Test Sequence

The functional test sequence shown in *Table C-6* ensures that the entire calculator system, including the keyboard and display, is functioning correctly. There are three starting points (at steps 1, 38, and 90) in the sequence where testing may be correctly initiated.

The first 37 steps of the test sequence represent the keyboard/display functional testing. These tests ensure that the lock switch and all of the input keys function correctly, and that all of the display segments (including minus sign, overflow, and all decimal points) function correctly when "on" and "off".

The first 50 steps of the test sequence comprise the master test sequence. This sequence is sufficient to ensure that the calculator is functioning correctly with a very high degree of probability, estimated to be well over 99%.

The remaining 50 steps of the test sequence are provided to ensure a total verification for the calculator system functionally. As an example, the total verification sequence will test all possible combinations of positive and negative numbers in addition and subtraction, whereas the master test sequence does not.

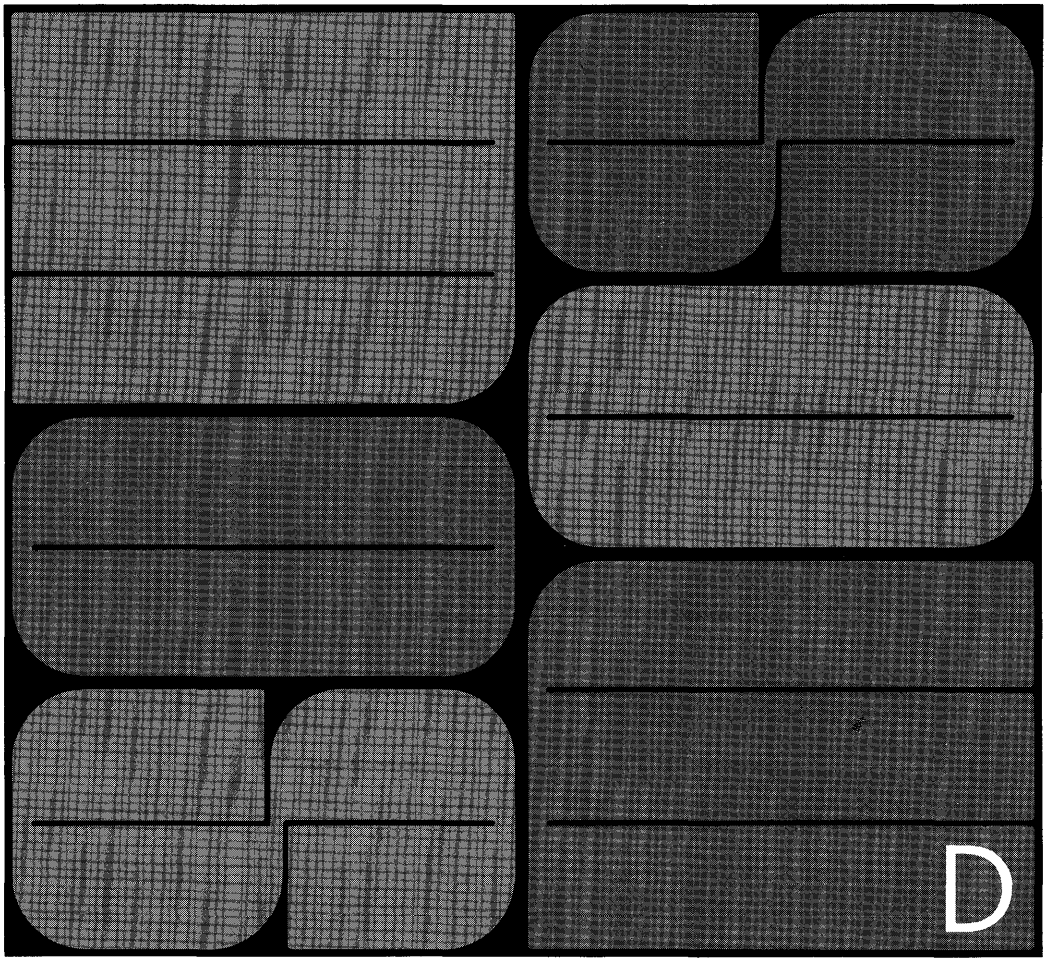
FUNCTIONAL TEST SEQUENCE

* Return Starting Position — 00 Double Zero Key

1-37 Keyboard/Display Test Sequence
1-50 Master Test Sequence
1-100 Total Verification Test Sequence
Dot in leading display segment indicates overflow

	INPUT	DISPLAY		INPUT	DISPLAY
*1	9	0 0 0 0 0 0 0 0 0 9	51	3 1	0 0 0 0 0 0 0 3 1
2	DP	0 0 0 0 0 0 0 0 0 9.	52	−	−0 0 0 0 0 0 0 2 4
3	DP	0 0 0 0 0 0 0 0.9	53	+	−0 0 0 0 0 0 0 1 7
4	DP	0 0 0 0 0 0 0.0 9	54	DUP	−0 0 0 0 0 0 0 1 7
5	DP	0 0 0 0 0 0.0 0 9	55	−	0 0 0 0 0 0 0 0 0 0
6	DP	0 0 0 0 0.0 0 0 9	56	÷	•−0 0 0 0 0 0 0 3 5
7	11 { DP	0 0 0 0.0 0 0 0 9	57	1 00	• 0 0 0 0 0 0 1 0 0
8	DP	0 0 0.0 0 0 0 0 9	58	LOCK	• 0 0 0 0 0 0 1 0 0
9	DP	0 0.0 0 0 0 0 0 9	59	÷	•−0 0 0 0 0 0 0 0 2
10	DP	0.0 0 0 0 0 0 0 9	60	%	• 0 0 0 0 0 0 0 0 1
11	DP	• 0 0 0 0 0 0 0 0 9	61	REM	• 0 0 0 0 0 0 0 7 0
12	DP	0 0 0 0 0 0 0 0 0 9	62	REC	• 0 0 0 0 0 0 0 7 0
13	ENT	0 0 0 0 0 0 0 0 0 9	63	REC	• 0 0 0 0 0 0 0 7 0
14	10	0 0 0 0 0 0 0 0 1 0	64	−	•−0 0 0 0 0 0 0 8 7
15	REC	0 0 0 0 0 0 0 0 0 9	65	0	• 0 0 0 0 0 0 8 7 0
16	1 2 3 4 5 6 7 8 9	1 2 3 4 5 6 7 8 9	66	−	• 0 0 0 0 0 0 9 0 5
17	X	• 1 1 1 1 1 1 1 1 0 1	67	CLR	−0 0 0 0 0 0 0 3 5
18	REM	• 0 0 1 1 1 1 1 1 1 1	68	CLR	0 0 0 0 0 0 0 0 0 0
19	REM	• 1 1 1 1 1 1 1 1 0 1	69	50	0 0 0 0 0 0 0 5 0
20	+	• 1 1 1 1 1 1 1 1 1 1	70	DUP	0 0 0 0 0 0 0 5 0
21	DUP	• 1 1 1 1 1 1 1 1 1 1	71	+	0 0 0 0 0 0 0 0 1 5
22	+	• 2 2 2 2 2 2 2 2 2 2	72	%	−0 0 0 0 0 0 0 0 0 5
23	−	•−1 1 1 1 1 1 1 1 1 1	73	−	0 0 0 0 0 0 0 0 0 5
24	LOCK	•−1 1 1 1 1 1 1 1 1 1	74	X	−0 0 0 0 0 0 1 7 5
25	+	•−2 2 2 2 2 2 2 2 2 2	75	CLR	−0 0 0 0 0 0 0 3 5
26	ENT	•−2 2 2 2 2 2 2 2 2 2	76	UNLOCK	−0 0 0 0 0 0 0 3 5
27	−	•−4 4 4 4 4 4 4 4 4 4	77	28	0 0 0 0 0 0 0 2 8
28	+	•−6 6 6 6 6 6 6 6 6 6	78	+	−0 0 0 0 0 0 0 0 7
29	÷	•−0 0 0 0 0 0 0 0 3	79	−	−0 0 0 0 0 0 0 2 8
30	%	•−0 0 6 6 6 6 6 6 7	80	REM	−0 0 0 0 0 0 0 3 5
31	00	• 6 6 6 6 6 6 7 0 0	81	−	0 0 0 0 0 0 0 2 8
32	UNLOCK	• 6 6 6 6 6 6 7 0 0	82	REC	−0 0 0 0 0 0 0 3 5
33	CLR	2 2 2 2 2 2 2 2 2 2	83	CLR	0 0 0 0 0 0 0 2 8
34	−	−8 8 8 8 8 8 8 8 8 8	84	+	0 0 0 0 0 0 0 0 0 0
35	+	•−5 5 5 5 5 5 5 5 5 4	85	456	0 0 0 0 0 0 0 4 5 6
36	CLR	−8 8 8 8 8 8 8 8 8 8	86	ENT	0 0 0 0 0 0 0 4 5 6
37	CLR	0 0 0 0 0 0 0 0 0 0	87	12	0 0 0 0 0 0 0 0 1 2
*38	7	0 0 0 0 0 0 0 0 0 7	88	%	0 0 0 0 0 0 0 0 5 5
39	ENT	0 0 0 0 0 0 0 0 0 7	89	−	0 0 0 0 0 0 0 4 0 1
40	44556	0 0 0 0 0 4 4 5 5 6	*90	44 00 00 00 00	• 4 0 0 0 0 0 0 0 0 0
41	DUP	0 0 0 0 0 4 4 5 5 6	91	DUP	• 4 0 0 0 0 0 0 0 0 0
42	X	• 9 8 5 2 3 7 1 3 6	92	DUP	• 4 0 0 0 0 0 0 0 0 0
43	%	• 0 0 8 9 6 6 6 0 0	93	+	• 8 0 0 0 0 0 0 0 0 0
44	ENT	• 0 0 8 9 6 6 6 0 0	94	÷	• 0 0 0 0 0 0 0 0 0 0
45	÷	• 0 0 0 0 0 0 0 1 0 9	95	REM	• 4 0 0 0 0 0 0 0 0 0
46	CLR	0 0 8 9 6 6 6 0 0	96	÷	• 0 0 0 0 0 0 0 0 2
47	REM	0 0 7 8 7 7 7 7 3 6	97	X	• 8 0 0 0 0 0 0 0 0 0
48	−	−0 0 7 8 7 7 7 2 9	98	DUP	• 8 0 0 0 0 0 0 0 0 0
49	REC	0 0 7 8 7 7 7 3 6	99	÷	• 0 0 0 0 0 0 0 0 1
50	+	0 0 0 0 0 0 0 0 0 7	100	REM	• 0 0 0 0 0 0 0 0 0 0

Micromosaic™ Logic Design



APPENDIX D

MICROMOSAIC™ LOGIC DESIGN

INTRODUCTION

Appendix D discusses custom circuit design phases between system structuring and computer-aided design, namely, partitioning the custom Micromosaic subsystem and selecting the cell functions that implement the circuits.

The cells are functional blocks such as gates, flip-flops, buffers, modular stages of shift registers, memory matrices, interface elements, etc. At this writing, the Micromosaic static silicon gate cell library contains some 108 cells. Most of these static functions are duplicated in a dynamic logic cell family. There are also bonding pads, input protection and special composable cells for RAMs, ROMs and combinatorial logic, as well as shift registers. A complete Micromosaic metal gate cell library is also available.

Only 97 of the most frequently used cells are detailed in this appendix. The other cells are described in additional Fairchild literature. There is a brief note on dynamic cells at the end of this appendix; however, Fairchild should be consulted on the operation and application of dynamic and all specialized cells.

General Specifications

General specifications for Micromosaic static silicon gate circuits (and circuits with compatible cells) are given in *Table D-1*. Additional performance parameters are in tabular and graphical forms in the chip size and delay estimates section that follows the cell descriptions. The designer may gain further insight into MOS characteristics by reviewing Appendix G on MOS processes.

TABLE D-1

DC ELECTRICAL CHARACTERISTICS (V_{SS} = +5 V +5%, V_{DD} = 0 V, V_{GG} = -12 V +5%)

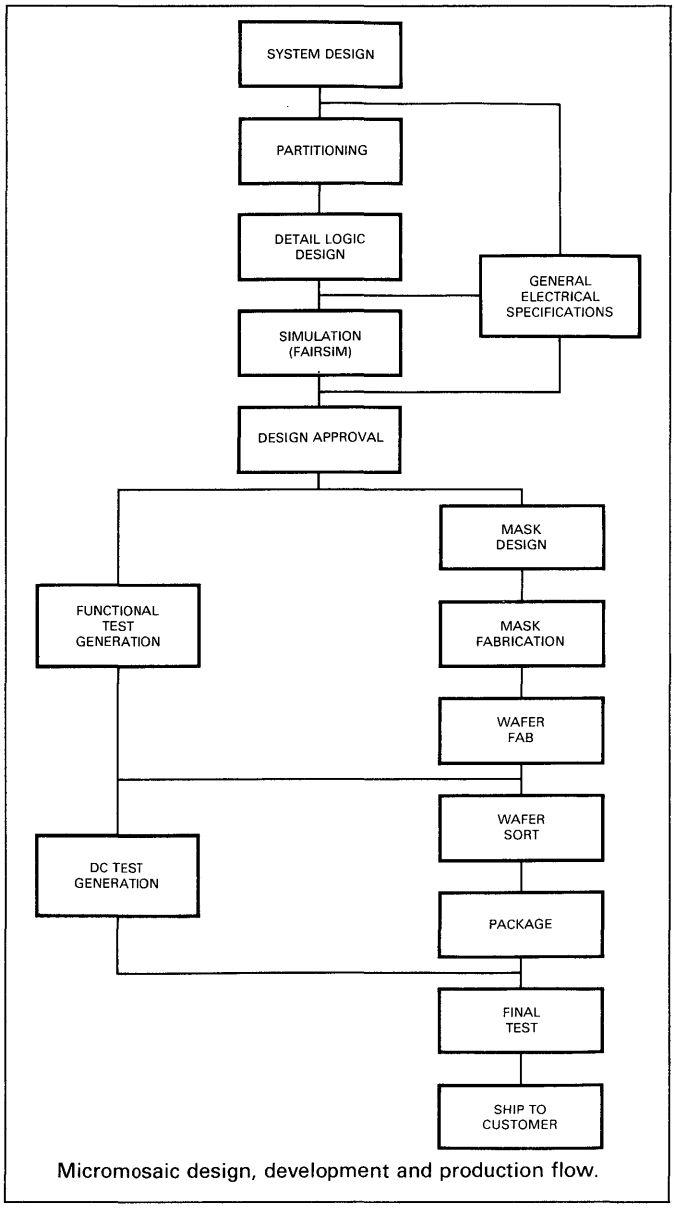
Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input Voltage HIGH	V_{SS}-1*	V_{SS}+0.3	V
V_{IL}	Input Voltage LOW	0	V_{SS}-4.2	V
V_{OH}	Clock Voltage HIGH	V_{SS}-1	V_{SS}+0.3	V
V_{OL}	Clock Voltage LOW	-10	-4	V
V_{OHI}	Output Voltage HIGH $\frac{TTL}{Buffer}$	+2.4	V_{SS}	V
V_{OH2}	Output Voltage HIGH $\frac{SGT}{Buffer}$	V_{SS}-1	V_{SS}	V
V_{OLI}	Output Voltage LOW $\frac{TTL}{Buffer}$	0	+0.4	V
V_{OL2}	Output Voltage LOW $\frac{SGT}{Buffer}$	0	+0.5	V

*NOTE: If input is driven by a TTL gate, a pull up resistor to V_{SS} is required. This pull up resistor can be incorporated on the chip with the input gate.

GENERAL DESIGN PROCEDURES

Figure D-1 illustrates the Micromosaic development and production flow. The end result will be cell arrays resembling *Figure D-2*. The fold out chart at the back of the book should be referenced while reading this appendix. Steps normally involved in partitioning and circuit design are:

1. Prepare conventional logic design of the MOS subsystem and support devices
2. Partition the custom logic into Micromosaic chips
3. Select Micromosaic cells for the individual chip designs
4. Diagram the Micromosaic logic (or logic and memory)
5. Estimate and adjust logic path delays (e.g., by substituting low power or high speed cells for standard speed cells)
6. List cells, their interconnections and delays for preliminary simulation with the FAIRSIM computer program



Micromosaic design, development and production flow.

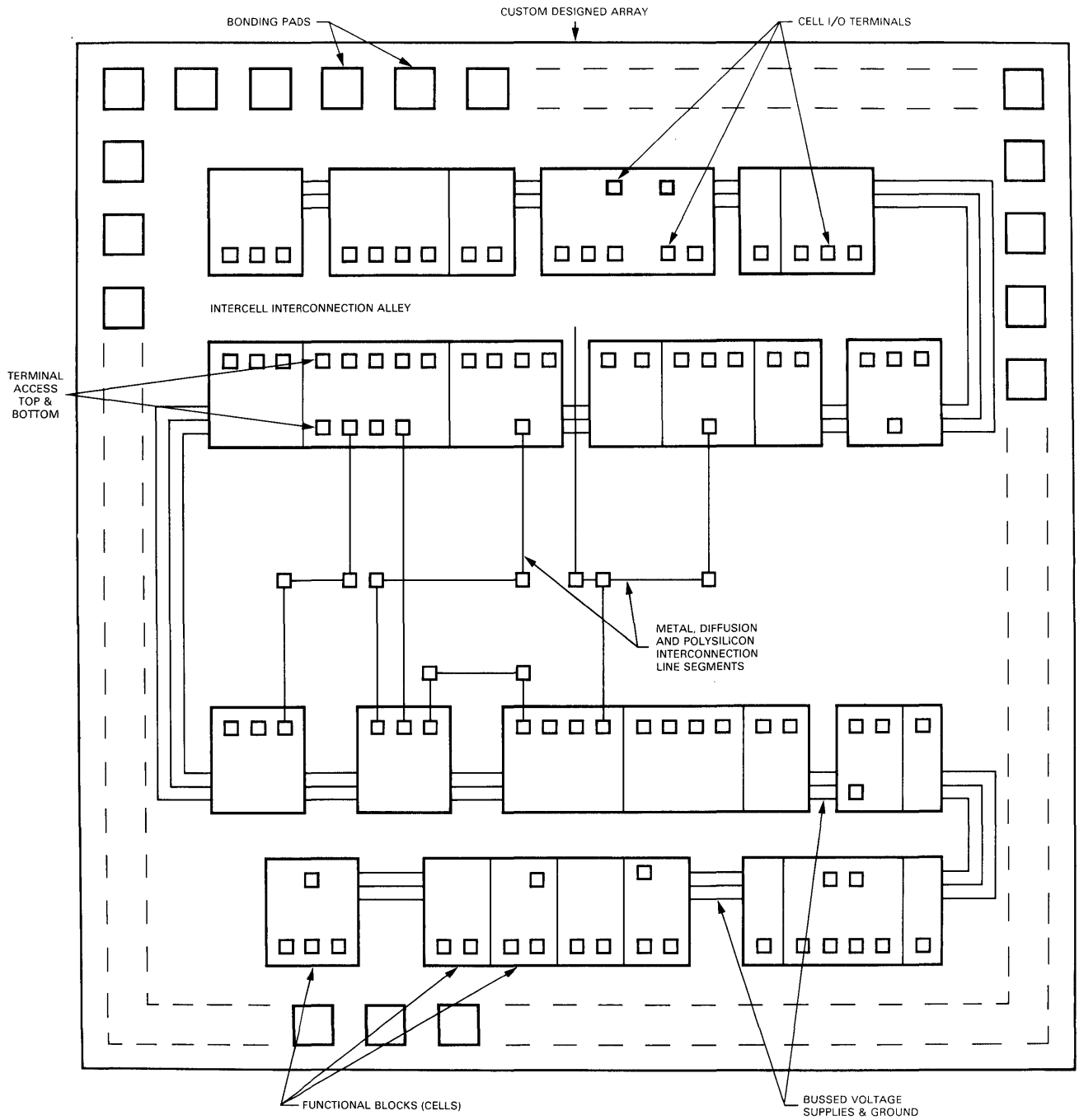
Fig. D-1. Micromosaic Flow

The use of FAIRSIM and other computer-aided design (CAD) programs is outlined in Appendix E. Customers who do their own circuit design need not be concerned with placement of cells and arrangement of interconnections on the chip. This is accomplished at Fairchild with a layout program. Customers are urged to inform Fairchild of critical timing areas prior to layout. This information proves valuable in the selection of layout alternatives.

Micromosaic Arrays and Cells

As shown in *Figure D-2,* the arrays are analogous to multilayer circuit board assemblies and the cells to packaged bipolar logic functions. The supply and ground "layers" are busses running through the cell rows. General logic signal wiring occupies the interconnection alleys. Alley widths are variable with interconnection density — there may be no alleys in highly modular storage arrays.

Bipolar input/output logic levels are generally specified and the cells are defined by their positive logic functions (see cell descriptions). Thus, cell designs may be breadboarded with TTL circuits if desired. A breadboard is sometimes useful in simulating the switching functions of logic cell groups, but cannot simulate their dynamic performance since the MOS capacitances can not be simulated. As a rule, computer simulation makes conventional breadboarding and debugging of the MOS designs unnecessary.



Typical arrangement of cells and interconnections on Micromosaic custom logic circuit (storage and register arrays may have little or no alley interconnection area).

Fig. D-2. Micromosaic Cell Arrangement

Logic Minimization

Conventional logic minimization techniques apply. However, the prime minimization goal is reducing chip area rather than the absolute number of functions. Chip area and circuit cost are directly related. The rule of thumb is to use complex functions or the Composable Logic Matrix (CLM), whenever possible, rather than large groups of simple gates or inverters. Complex cells usually occupy much less chip area per gate and require fewer interconnections, thereby saving both row and alley area and improving speed. Compared with combinatorial logic implemented with random interconnected gates, the composable matrix saves as much as 50% in area and 25% in path delays.

The designer should also search for ways to take advantage of the flexibility of MOS cellular design, such as using wire-OR connections, positive and negative logic, and generating AND and OR functions with NOR and NAND gates. Such techniques can remove inverters and expanders from the chip and the delay paths.

A 1:1 conversion of a bipolar design to a Micromosaic design is not nearly as efficient as it might be with departures from conventional design.

PARTITIONING

As discussed above, departures from conventional logic subsystem partitioning may be highly beneficial. The basic goal is familiar — to divide the subsystem into groups with efficient gate/pin ratios. The designer need not be concerned with standardizing to some particular card size and number of pins since he is designing circuits rather than subassemblies. It is most important to divide the functions into natural groupings that optimize the costs (die size and package cost) of each individual group.

Optimum Die Size

As indicated by the charts in the main text, optimum die size is at the null in die processing and packaging costs. However, for custom MOS/LSI being designed today, the optimum range is more likely to be 180 x 180 to 220 x 220 mils than 140 x 140 to 160 x 160 mils. The larger size dice are frequently more efficient when a fairly long production life is anticipated or a single larger-than-optimum die substitutes for two smaller-than-optimum dice.

Large dice tend to reduce package cost per function particularly when slicing the system further would require additional pins as well as packages. Also, development costs may be lower when subsystem functions are divided more naturally.

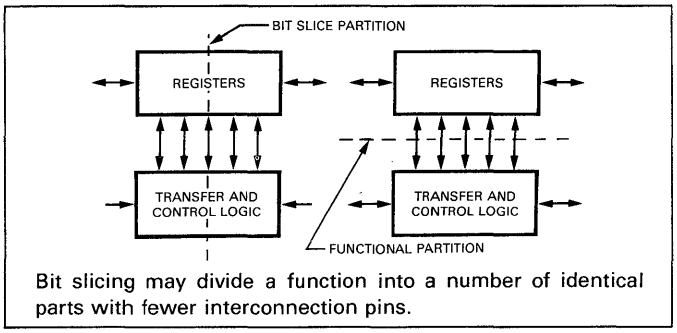
Chip size must vary with the number of cell interconnections, I/O bonding pads and buffers, and number of critical paths. These are maximum in highly random logic designs.

Over-partitioning to reduce die size may be self-defeating. The gate pin ratio may suffer — and pins include such costs as chip area used by bonding pads and buffers. In some cases, the number of pads dictates chip size rather than logic density, since the pads must be adequately spaced on the chip periphery.

Improving Gate/Pin Ratios

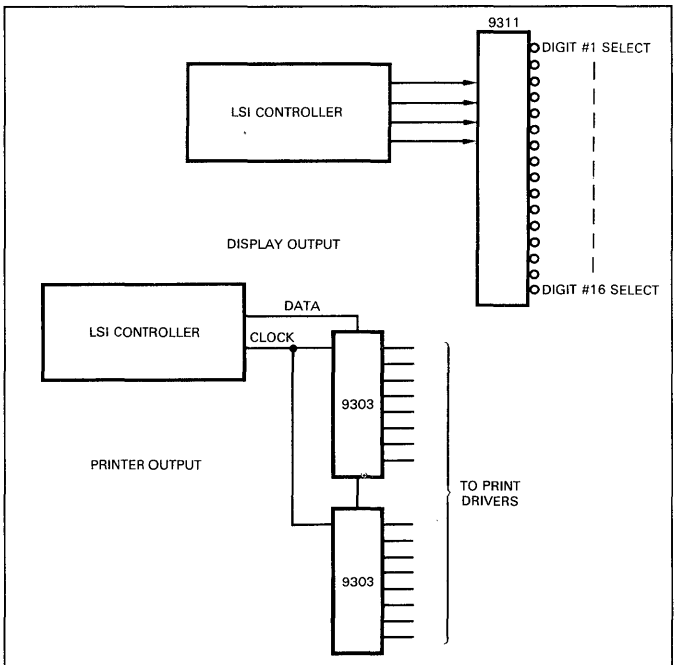
Standard available packages should be considered when designing a custom product. It is wasteful when all the pins are not used, but, conversely, too many pins may force expensive custom package development.

1. *SINGLE-RAIL TRANSFER BETWEEN CHIPS.* If both signal levels are needed at the receiving chips, send one level and invert it locally.
2. *LOCAL DECODING.* If chips require many decodes of a counter, decode at the receiving chips instead of distributing numerous signals.
3. *LOCAL COUNTERS.* These may be synchronized to source counters.
4. *SIGNAL BUSSING.* One line will serve for signals not required at the same time.
5. *BIT SLICING.* Partition a system by bits rather than functions (*Figure D-3*).
6. *ILLEGAL INPUT CODES.* Implement input test points or test mode selection with an input combination that cannot occur in the normally operating system.
7. *SERIAL TRANSFER.* Do not use parallel transfer unless serial transfer is too slow.
8. *BIPOLAR AUGMENTATION.* Besides reducing pin counts, external bipolar logic simplifies drive circuitry. Two examples are given in *Figure D-4*.
9. *CONCEPTUAL DESIGN CHANGES.* For example, employ time multiplexing to enhance serial transfer and signal bussing.



Bit slicing may divide a function into a number of identical parts with fewer interconnection pins.

Fig. D-3. Bit Slicing



Bipolar output logic devices may minimize pins while improving drive. At the top, the 9311 is the digit selector of a scanned display. The 9303 registers at the bottom save 14 controller pins.

Fig. D-4. MOS with Bipolar Augmentation

Operating Speed

Minimum pin configurations such as serial transfer affect operating speeds. Speed may be restored by:

1. *ON CHIP CRITICAL PATHS.* Do not partition such that package-to-package buffer and wiring delays are added to logic delays. These are large compared with on chip wiring delays.

2. *PARALLELISM.* Use lookahead adders, etc.

3. *CELL SELECTION.* If necessary, use high speed cells (generally larger than standard cells). Complex functions also improve speed. For example, the CLM can multiplex at much higher speed than standard logic cells, a master/slave flip-flop replaces two latches without wiring runs, and so forth.

4. *EXTERNAL BIPOLAR CIRCUITS.* Use TTL MSI for high speed logic. Also use external clock generators and drivers to improve rise and fall times.

MICROMOSAIC 3402 CELL DESCRIPTIONS

The tables that follow identify the most commonly used cells in the static silicon gate library, define the nomenclature, and provide data used to estimate chip size, power and path delays. When reading the detailed cell descriptions, the following definitions are useful.

GRID — Grid numbers indicate the length of standard cells in the cell row direction. One grid length is 0.9 mil. The standard cell height is 8 grids.

LOGIC SYMBOL — Positive logic is assumed. Logic symbols are in accordance with MIL-STD-806B and functions with MIL-STD-806B combination table in *Figure D-5.*

LOGIC EQUATION — The cell's positive logic Boolean function.

Z — This is an unique name in the FAIRSIM format. Z is assigned by the designer.

SCHEMATIC — Conventional schematic of the cell.

FAIRSIM MODEL — Model used in computer simulation.

FAIRSIM MACRO — A computer description of the FAIRSIM model. The macro replaces Z.

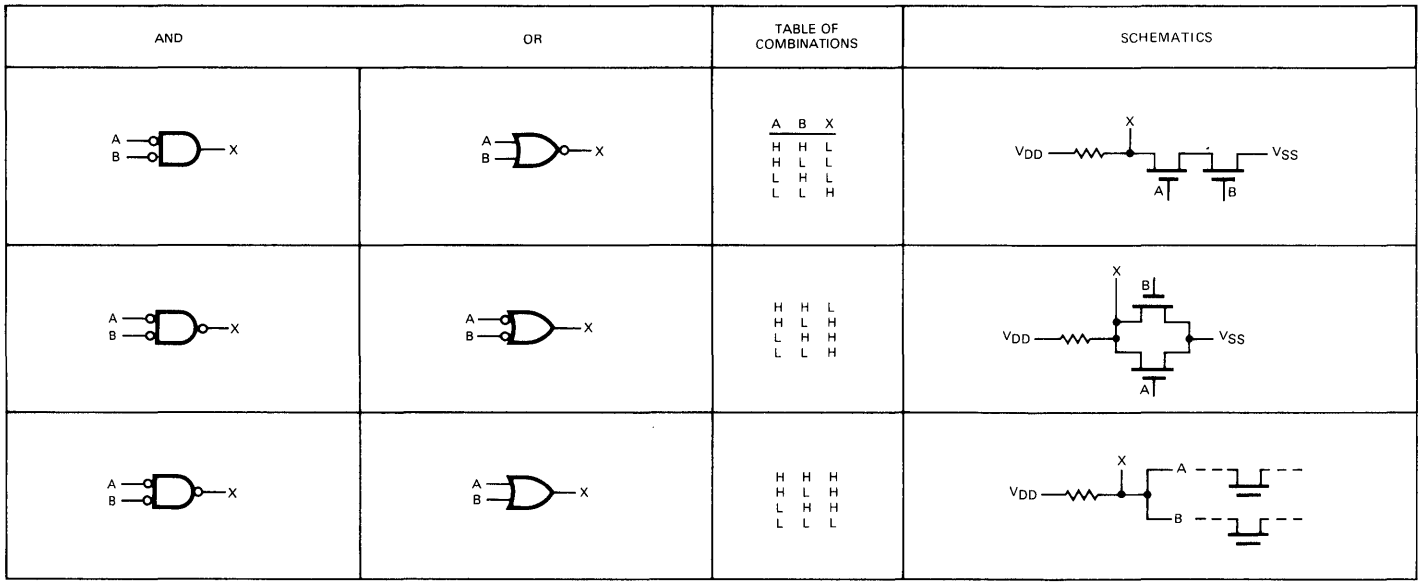


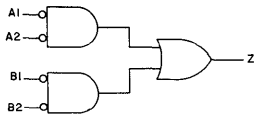
Fig. D-5. Combination Tables from MIL-STD-806B

A01 A01X
A01H A01HX

The AND-OR function for complemented 2-wide minterms is provided with a load resistor A01/A01H for normal gate use, or without a resistor A01X/A01HX for expansion of other cells of equal power level. Cell length is 5 grids except A01H is 7 grids.

A01
A01H

LOGIC SYMBOL



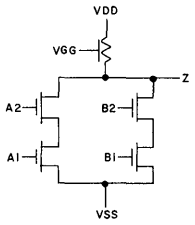
LOGIC EQUATION

$$Z = \overline{A1} \cdot \overline{A2} + \overline{B1} \cdot \overline{B2}$$

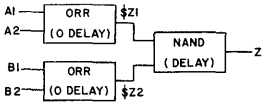
FAIRSIM FORMAT

```
Z * A01   A1,A2,B1,B2,DEL
```

SCHEMATIC



FAIRSIM MODEL



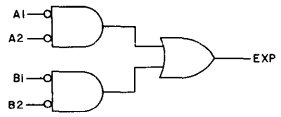
FAIRSIM MACRO

```
&Z      * A01     &A1,&A2,&B1,&B2,&DEL
&Z        CELL    A01
$&Z.1     ORR     (&A1,&A2),,0
$&Z.2     ORR     (&B1,&B2),,0
&Z        NAND    ($&Z.1,$&Z.2),,&DEL
          MEND
```

*OR A01H

A01X
A01HX

LOGIC SYMBOL



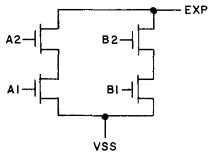
LOGIC EQUATION

$$EXP = \overline{A1} \cdot \overline{A2} + \overline{B1} \cdot \overline{B2}$$

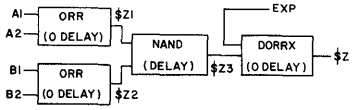
FAIRSIM FORMAT

```
Z * A01X   A1,A2,B1,B2,EXP,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z      * A01X    &A1,&A2,&B1,&B2,
                  &EXP,&EXP,&DEL
&Z        CELL    A01X
$&Z.1     ORR     (&A1,&A2),,0
$&Z.2     ORR     (&B1,&B2),,0
$&Z.3     NAND    ($&Z.1,$&Z.2),,&DEL
$&Z       DORRX   ($&Z.3,&EXP),,0
          MEND
```

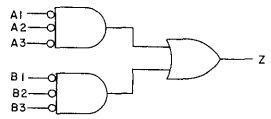
*OR A01HX

A02 A02X

The AND-OR function for complemented 3-wide minterms is provided with a load resistor (A02) for normal gate use, or without a resistor (A02X) for expansion of other cells of equal power level. The cell length is 7 grids.

A02

LOGIC SYMBOL



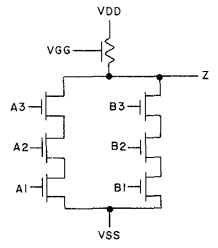
LOGIC EQUATION

$$Z = \overline{A1} \cdot \overline{A2} \cdot \overline{A3} + \overline{B1} \cdot \overline{B2} \cdot \overline{B3}$$

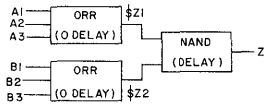
FAIRSIM FORMAT

Z A02 A1,A2,A3,B1,B2,B3,DEL

SCHEMATIC



FAIRSIM MODEL

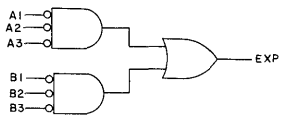


FAIRSIM MACRO

```
&Z      A02     &A1,&A2,&A3,&B1,&B2,&B3,&DEL
&Z      CELL    A02
$&Z.1   ORR     (&A1,&A2,&A3),,0
$&Z.2   ORR     (&B1,&B2,&B3),,0
&Z      NAND    ($&Z.1,$&Z.2),,&DEL
        MEND
```

A02X

LOGIC SYMBOL



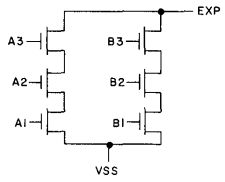
LOGIC EQUATION

$$EXP = \overline{A1} \cdot \overline{A2} \cdot \overline{A3} + \overline{B1} \cdot \overline{B2} \cdot \overline{B3}$$

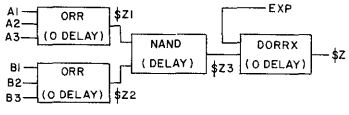
FAIRSIM FORMAT

Z A02X A1,A2,A3,B1,B2,B3,EXP,DEL

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

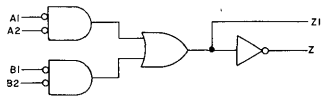
```
&Z      A02X    &A1,&A2,&A3,&B1,&B2,&B3,&EXP,&DEL
&Z      CELL    A02X
$&Z.1   ORR     (&A1,&A2,&A3),,0
$&Z.2   ORR     (&B1,&B2,&B3),,0
$&Z.3   NAND    ($&Z.1,$&Z.2),,&DEL
$&Z     DORRX   ($&Z.3,&EXP),,0
        MEND
```

A03

The A03 provides the AND-OR function for complemented inputs. Both true and complemented outputs are available. The cell length is 6 grids.

A03

LOGIC SYMBOL



LOGIC EQUATION

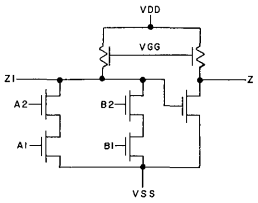
$$Z = (A1+A2)\cdot(B1+B2)$$

$$Z1 = \overline{A1}\cdot\overline{A2} + \overline{B1}\cdot\overline{B2}$$

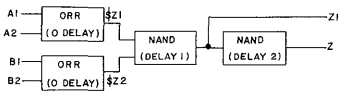
FAIRSIM FORMAT

```
Z   A03   A1,A2,B1,B2,DEL1,DEL2
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

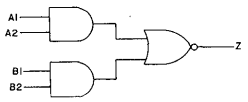
```
&Z      A03     &A1,&A2,&B1,&B2,&DEL1,&DEL2
&Z      CELL    A03
$&Z.1   ORR     (&A1,&A2),,0
$&Z.2   ORR     (&B1,&B2),,0
&Z.1    NAND    ($&Z.1,$&Z.2),,&DEL1
&Z      NAND    ($$&Z.1),,&DEL2
        MEND
```

A04
A04H

The A04 provides the AND-OR-INVERT function for all inputs. The cell length is 6 grids.

A04
A04H

LOGIC SYMBOL



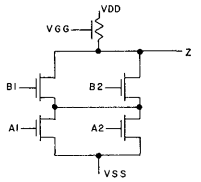
LOGIC EQUATION

$$Z = A1\cdot A2 + B1\cdot B2$$

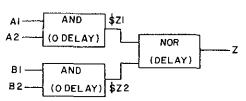
FAIRSIM FORMAT

```
&Z  *A04   &A1,&A2,&B1,&B2,&DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z      *A04    &A1,&A2,&B1,&B2,&DEL
&Z      CELL    A04
$&Z.1   AND     (&A1,&A2)),,0
$&Z.2   AND     (&B1,&B2),,0
&Z      NOR     ($&Z.1,$&Z.2),,&DEL
        MEND
```

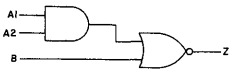
*OR A04H

A05

The A05 provides the function $Z = (\overline{A1} + \overline{A2})\,B$. The cell length is 4 grids.

A05

LOGIC SYMBOL



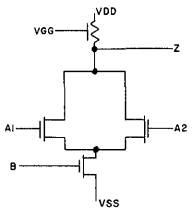
LOGIC EQUATION

$$\overline{Z} = A1 \cdot A2 + B$$

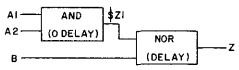
FAIRSIM FORMAT

```
Z   A05   A1,A2,B,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z      A05     &A1,&A2,&B,&DEL
&Z      CELL    A05
$&Z.1   AND     (&A1,&A2)),,0
&Z      NOR     ($&Z.1,&B),,&DEL
        MEND
```

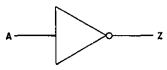
BUFB1 BUFB3 BUFB5 BUFB2 BUFB4

The BUFB is a series of inverting push/pull buffers intended for driving bipolar logic–DTL and TTL.

	Cell Length	Cell Width
BUFB1	17 Grids	17 Grids
BUFB2	16 Grids	8 Grids
BUFB3	26 Grids	17 Grids
BUFB4	16 Grids	17 Grids
BUFB5	22 Grids	8 Grids

LOGIC SYMBOL

BUFB1
BUFB2
BUFB3
BUFB4
BUFB5



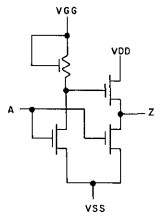
LOGIC EQUATION

$$Z = \overline{A}$$

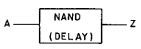
FAIRSIM FORMAT

```
Z   *BUFB1   A,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z   *BUFB1   &A,&DEL
&Z    CELL    BUFB1
&Z    NAND    &A,,&DEL
      MEND
```

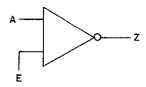
*OR BUFB2, BUFB3, BUFB4, BUFB5

BUFG1

The BUFG1 is an Inverting Push/Pull Buffer with an enable input which causes a high impedance output when LOW. The BUFG1 is designed for driving other silicon gate arrays. The cell length is 19 grids while the width is 17 grids.

BUFG1

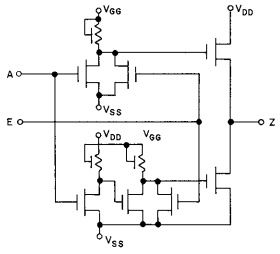
LOGIC SYMBOL



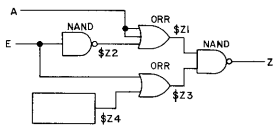
FAIRSIM FORMAT

```
Z   BUFG1   A,E,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z      BUFG1   &A,&E,&DEL
&Z      CELL    BUFG1
$&Z.1   ORR     (&A,&A,$&Z.2),,0
$&Z.2   NAND    &E,,0
$&Z.3   ORR     ($$&E,$&Z.4),,0
$&Z.4   AND     $&Z.4,,0
&Z      NAND    ($&Z.1,$&Z.3),,&DEL
        MEND
```

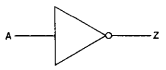
BUFM1 BUFM3 BUFM6 BUFM2 BUFM4

The BUFM is a series of inverting push/pull buffers intended for driving other silicon gate arrays.

	Cell Length	Cell Width
BUFM1	15 Grids	8 Grids
BUFM2	8 Grids	8 Grids
BUFM3	13 Grids	17 Grids
BUFM4	5 Grids	17 Grids
BUFM6	4 Grids	8 Grids

BUFM1 BUFM2 BUFM3 BUFM4 BUFM6

LOGIC SYMBOL



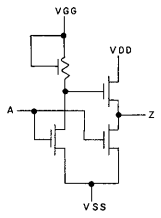
LOGIC EQUATION

$$Z = \overline{A}$$

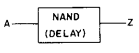
FAIRSIM FORMAT

```
Z   *BUFM1   A,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z  *BUFM1   &A,&DEL
&Z   CELL    BUFM1
&Z   NAND    &A,,&DEL
     MEND
```

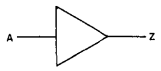
*OR BUFM2, BUFM3, BUFM4, BUFM6

BUFT1

The BUFT1 is a Non-Inverting Buffer with a low impedance switch to VSS and a standard resistor load to VDD. Cell length is 6 grids.

BUFT1

LOGIC SYMBOL



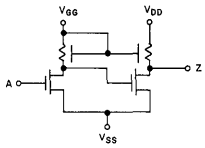
LOGIC EQUATION

Z = A

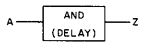
FAIRSIM FORMAT

```
Z   BUFT1  A,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

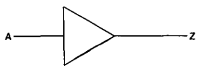
```
&Z  BUFT1  &A,&DEL
&Z  CELL   BUFT1
&Z  AND    &A,,&DEL
    MEND
```

BUFX1

The BUFX1 is a Non-Inverting Buffer with no internal pull down. When connected with other uncommitted buffers and an external load resistor, an off chip wired-OR is produced. The BUFX1 may be used to drive a DTL-TTL load with the use of an external resistor returned to VGG. The cell length is 6 grids.

BUFX1

LOGIC SYMBOL



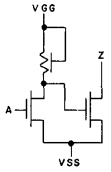
LOGIC EQUATION

Z = A

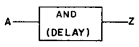
FAIRSIM FORMAT

```
Z   BUFX1  A,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

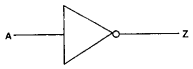
```
&Z  BUFX1  &A,&DEL
&Z  CELL   BUFX1
&Z  AND    &A,,&DEL
    MEND
```

BUFX2

The BUFX2 is an Inverting Buffer with a single ended drive to VSS only. When connected with other uncommitted buffers and an external load resistor, an off chip wired-OR is produced. The BUFX2 may be used to drive a load which is returned to VSS -20 volts. The cell length is 4 grids.

BUFX2

LOGIC SYMBOL



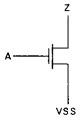
LOGIC EQUATION

$Z = \overline{A}$

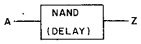
FAIRSIM FORMAT

```
Z    BUFX2   A,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

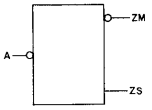
```
&Z    BUFX2   &A,&DEL
&Z    CELL    BUFX2
&Z    NAND    &A,,&DEL
      MEND
```

CG1

The CG1 is a 2-Phase On Chip Clock Generator. The ZM being high voltage, for driving 64 2-phase quasi-static flip-flops at 1 MHz. Be aware that a worst case delay of 5 µs after power is applied is required before the cell can be considered to be operative. The cell length is 24 grids.

CG1

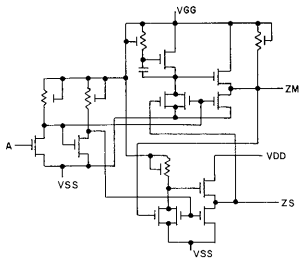
LOGIC SYMBOL



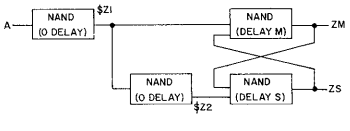
FAIRSIM FORMAT

```
Z    CG1    A,DELI,DELM,DELS
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

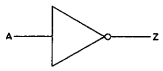
```
&Z     CG1     &A,&DELI,&DELM,&DELS
&Z     CELL    CG1
$&Z.1  NAND    &A,,&DELI
$&Z.2  NAND    $&Z.1,,0
&Z.M   NAND    ($&Z.1,$$&Z.S),,&DELM
&Z.S   NAND    ($&Z.2,$$&Z.M),,&DELS
       MEND
```

CG2

The CG2 provides a 1-Phase On Chip High Voltage Clock Generator. An input logic signal swing between VDD and VSS provides an output inverted signal swing between VSS and VGG VT. The cell length is 6 grids.

CG2

LOGIC SYMBOL



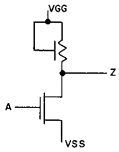
LOGIC EQUATION

$Z = \overline{A}$

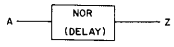
FAIRSIM FORMAT

```
Z   CG2   A,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

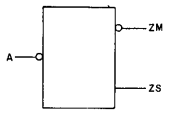
```
&Z   CG2    &A,&DEL
&Z   CELL   CG2
&Z   NOR    &A,,&DEL
     MEND
```

CG3

The CG3 is a 2-Phase On Chip Clock Generator. The ZM being high voltage, for driving 2-phase quasi-static flip-flops. The cell length is 17 grids.

CG3

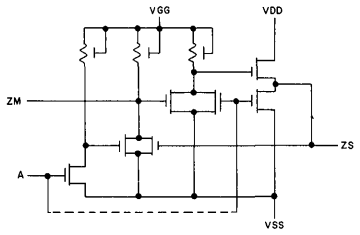
LOGIC SYMBOL



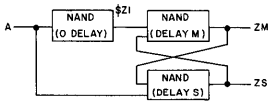
FAIRSIM FORMAT

```
Z   CG3   A,DELI,DELM,DELS
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

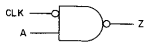
```
&Z     CG3     &A,&DELI,&DELM,&DELS
&Z     CELL    CG3
$&Z.1  NAND    &A,,&DELI
&Z.M   NAND    ( $&Z.1,$$&Z.S),,&DELM
&Z.S   NAND    (&A,$$&Z.M),,&DELS
       MEND
```

CG4

The CG4 provides a gated output of the high voltage input signal CLK, producing a high voltage output which can only go LOW when the enable signal A is HIGH. Cell length is 7 grids.

CG4

LOGIC SYMBOL



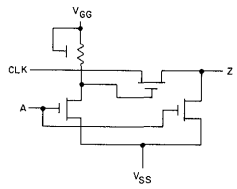
LOGIC EQUATION

$$Z = \overline{A}+CLK$$

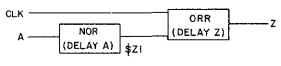
FAIRSIM FORMAT

```
Z  CG4   CLK,A,DELEN,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

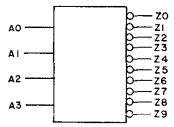
```
&Z      CG4     &CLK,&A,&DELEN,&DEL
&Z      CELL    CG4
$&Z.1   NOR     &A,,&DELEN
&Z      ORR     ($&Z.1,&CLK),,&DEL
        MEND
```

DEC1
DEC2

The DEC1 is an optimized BCD decoder cell which accepts four inputs and provides ten mutually exclusive outputs. It is logically identical to the 9301 MSI Decoder. The cell length is 25 grids.

DEC1
DEC2

LOGIC SYMBOL



FAIRSIM FORMAT

```
                A0,A1,A2,A3,&DELI,&DELO
                        OR
Z   *DEC1   A0,A1,A2,A3,E,F,G,H,J,K,L,M,N,
            P,Q,R,S,T,U,V,W,X,Y,ZZ,DELI,DELO
                        OR  OR
(DELI1,DELI2,DELI3,DELI4)   (DELO0,DEL01,DELO2,.....,DELO9)
```

TRUTH TABLE

A0	A1	A2	A3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
X	X	H	H	H	H	H	H	H	H	H	H	H	H
X	H	X	H	H	H	H	H	H	H	H	H	H	H

FAIRSIM MACRO

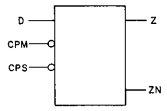
```
&Z      *DEC1   &A0,&A1,&A2,&A3,&E,&F,&G,&H,
                &J,&K,&L,&M,&N,&P,&Q,&R,&S,
                &T,&U,&V,&W,&X,&Y,&ZZ,&DELI,&DELO
&Z      CELL    DEC1
&Z.AN   NAND    &A3,,&DELI1
&Z.BN   NAND    &A2,,&DELI2
&Z.CN   NAND    &A1,,&DELI3
&Z.DN   NAND    &A0,,&DELI4
&E1     SETC    '&A1'
&F1     SETC    '&Z.AN'
&G1     SETC    '&Z.BN'
&H1     SETC    '&A0'
&J1     SETC    '&Z.AN'
&K1     SETC    '&Z.CN'
&L1     SETC    '&A2'
&M1     SETC    '&Z.DN'
&N1     SETC    '&Z.AN'
&P1     SETC    '&A1'
&Q1     SETC    '&Z.AN'
&R1     SETC    '&Z.BN'
&S1     SETC    '&Z.CN'
&T1     SETC    '&Z.DN'
&U1     SETC    '&A3'
&V1     SETC    '&Z.BN'
&W1     SETC    '&Z.CN'
&X1     SETC    '&A0'
&Y1     SETC    '&Z.AN'
&Z1     SETC    '&A2'
&Z.0    NAND    ($$&Q1,$$&R1,&S1,&T1),,&DEL0
&Z.1    NAND    ($$&G1,$$&H1,&J1,&K1),,&DEL1
&Z.2    NAND    ($$&M1,$$&P1,&Q1,&R1),,&DEL2
&Z.3    NAND    ($$&E1,$$&F1,&G1,&H1),,&DEL3
&Z.4    NAND    ($$&J1,$$&K1,&L1,&M1),,&DEL4
&Z.5    NAND    ($$&W1,$$&X1,&Y1,$$&Z1),,&DEL5
&Z.6    NAND    ($$&L1,$$&M1,&N1,&P1),,&DEL6
&Z.7    NAND    ($$&X1,$$&Z1,$$&E1,&F1),,&DEL7
&Z.8    NAND    ($$&S1,$$&T1,&U1,&V1),,&DEL8
&Z.9    NAND    ($$&U1,$$&V1,&W1,&X1),,&DEL9
*OR DEC2 MEND
```

DFQA

DFQA, the D Flip-Flop, utilizes a 2-phase clock and stored charge effects which allows small size and power. CPM must have a larger than normal signal swing, which may be provided by an on chip clock generator or externally. CPS is a normal logic level. The period of CPM must not exceed a worst case limit typically 0.5 ms at 0° to 70°C. The cell length is 8 grids.

DFQA

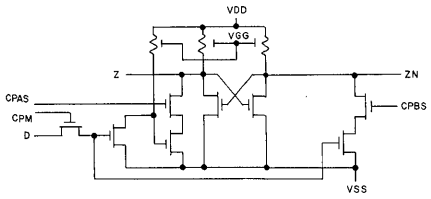
LOGIC SYMBOL



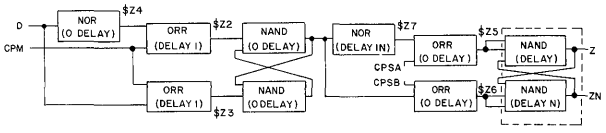
FAIRSIM FORMAT

```
Z   DFQA  D,CPM,CPS,DEL1,DEL1N,DEL,DELN
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

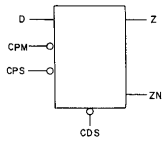
```
&Z      DFQA   &D,&CPM,&CPS,&DEL1,&DEL1N,&DEL,&DELN
&Z      CELL   DFQA
*              CPS(1) - CPAS   CPS(2) - CPBS
$&Z.1   NAND   ($&Z.2,$&Z.1N),,0
$&Z.1N  NAND   ($&Z.3,$&Z.1),,0
$&Z.4   NOR    &D,,0
$&Z.2   ORR    ($&Z.4,&CPM),,&DEL1
$&Z.3   ORR    ($$&D,$$&CPM),,&DEL1
$&Z.5   ORR    ($&Z.7,&CPS(1)),,0
$&Z.6   ORR    ($&Z.1,&CPS(2)),,0
$&Z.7   NOR    $&Z.1,,&DEL1N
&Z      CCNA   $&Z.5,$&Z.5,$&Z.6,$&Z.6,,,&DEL,&DELN
       MEND
```

DFQB

DFQB, the D Flip-Flop, utilizes a 2-phase clock and stored charge effects which allows small size and power. CP must have a larger than normal signal swing, which may be provided by an on chip clock generator or externally. CPS is a normal logic level. The period of CPM must not exceed a worst case limit, typically 0.5 ms. At 0° to 70°C. The CD input resets the slave only. The cell length is 8 grids

DFQB

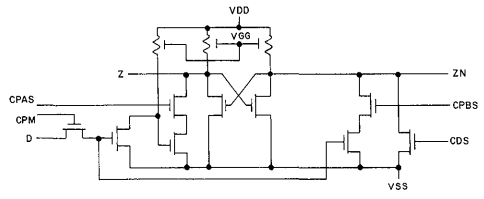
LOGIC SYMBOL



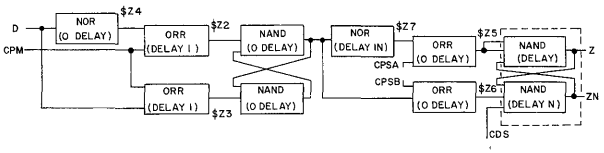
FAIRSIM FORMAT

```
Z   DFQB  D,CDS,CPM,CPS,DEL1,DEL1N,DEL,DELN
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

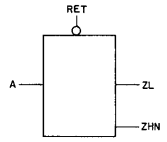
```
&Z      DFQB   &D,&CDS,&CPM,&CPS,&DEL1,&DEL1N,&DEL,
               &DELN
&Z      CELL   DFQB
*              CPS(1) - CPAS   CPS(2) - CPBS
$&Z.1   NAND   ($&Z.2,$&Z.1N),,0
$&Z.1N  NAND   ($&Z.3,$&Z.1),,0
$&Z.4   NOR    &D,,0
$&Z.2   ORR    ($&Z.4,&CPM),,&DEL1
$&Z.3   ORR    ($$&D,$$&CPM),,&DEL1
$&Z.5   ORR    ($&Z.7,&CPS(1)),,0
$&Z.6   ORR    ($&Z.1,&CPS(2)),,0
$&Z.7   NOR    $&Z.1,,&DEL1N
&Z      CCNA   $&Z.5,$&Z.5,&CDS,$&Z.6,,,&DEL,&DELN
       MEND
```

DISC1

The DISC1 is a Dual Threshold Voltage Discriminator which may also be used as an oscillator, retriggerable one shot or schmidt trigger. Input A should never be driven negative of VSS -15 V (VDD -5 V IF RET is LOW) without suitable current limiting. Cell length is 17 grids.

DISC1

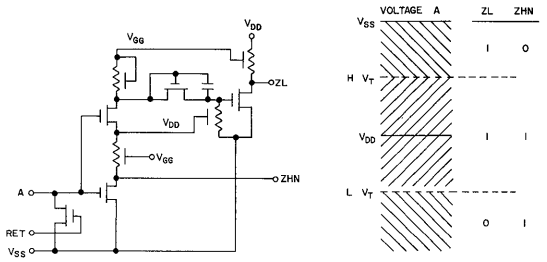
LOGIC SYMBOL



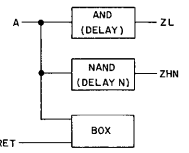
FAIRSIM FORMAT

```
Z  DISC1 A,RET,DEL,DELN
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

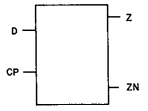
```
&Z      DISC1   &A,&RET,&DEL,&DELN
&Z      CELL    DISC1
$&Z.1   BOX     (&A,&RET)
&Z.L    AND     $$&A,,&DEL
&Z.HN   NAND    $$&A,,&DELN
        MEND
```

DLA

DLA provides a single bit of storage. CPA and CPB are normally commoned as the clock input. When the clock is LOW, the output will follow the input. When the clock goes HIGH, the latch will hold the information. The cell length is 7 grids.

DLA

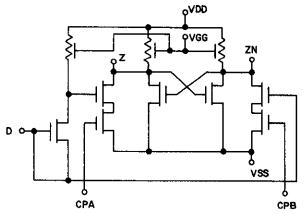
LOGIC SYMBOL



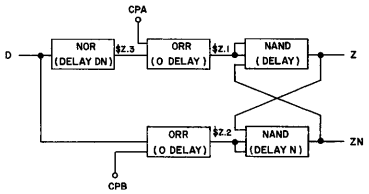
FAIRSIM FORMAT

```
Z  DLA  &D,&CP,&DELDN,&DEL,&DELN
```

SCHEMATIC



FAIRSIM MODEL

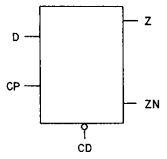


DLB

DLB provides a single bit of storage, CPA and CPB are normally commoned as the clock input. When the clock is LOW, the output will follow the input. When the clock goes HIGH, the latch will hold the information. CD provides an asynchronous clear when LOW. The cell length is 7 grids.

DLB

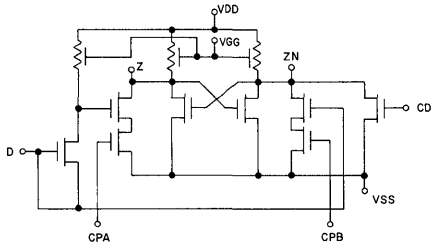
LOGIC SYMBOL



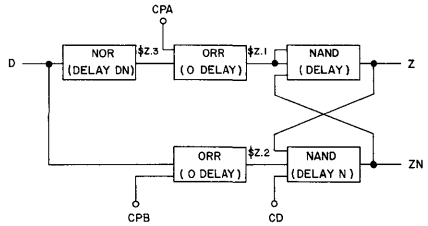
FAIRSIM FORMAT

```
Z   DLB   &D,&CD,&CP,&DELDN,&DEL,&DELN
```

SCHEMATIC



FAIRSIM MODEL

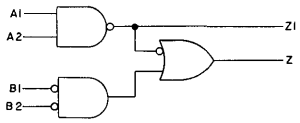


EO1

The EO1 provides the not-exclusive OR (compare) function at Z when A1=B1 and A2=B2. This corresponds to Z being the inverted sum. Z1 the inverted carry of a half adder. The cell length is 6 grids.

EO1

LOGIC SYMBOL



LOGIC EQUATION

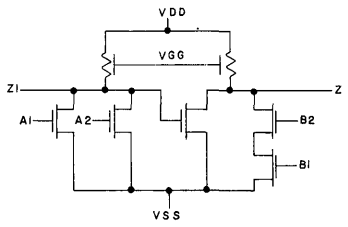
$$Z1 = \overline{A1 \cdot A2}$$

$$Z = A1 \cdot A2 + \overline{B1} \cdot \overline{B2}$$

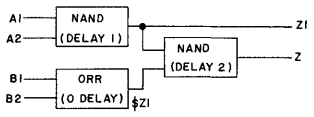
FAIRSIM FORMAT

```
Z   EO1   A1,A2,B1,B2,DEL1,DEL2
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

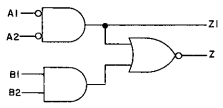
```
&Z      EO1     &A1,&A2,&B1,&B2,&DEL1,&DEL2
&Z      CELL    EO1
&Z.1    NAND    (&A1,&A2),,&DEL1
$&Z.1   ORR     (&B1,&B2),,0
&Z      NAND    ($$&Z.1,$&Z.1),,&DEL2
        MEND
```

EO2 EO2X

The exclusive OR function of two terms is provided at Z when A1=B1 and A2=B2. This corresponds to Z being the sum, Z1 being the carry of a half adder for complemented inputs. The cell length is 6 grids.

EO2

LOGIC SYMBOL



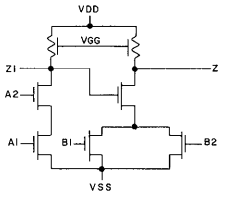
LOGIC EQUATION

$$Z1 = \overline{A1 \cdot A2}$$
$$Z = \overline{A1 \cdot A2 + B1 \cdot B2}$$

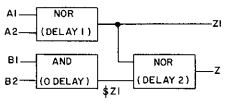
FAIRSIM FORMAT

```
Z   EO2   A1,A2,B2,B2,DEL1,DEL2
```

SCHEMATIC



FAIRSIM MODEL

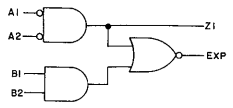


FAIRSIM MACRO

```
&Z      EO2     &A1,&A2,&B1,&B2,&DEL1,&DEL2
&Z      CELL    EO2
&Z.1    NOR     (&A1,&A2),,&DEL1
$&Z.1   AND     (&B1,&B2),,0
&Z      NOR     ($$&Z.1,$&Z.1,,&DEL2
        MEND
```

EO2X

LOGIC SYMBOL



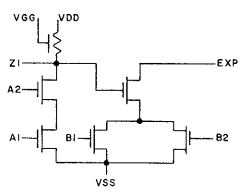
LOGIC EQUATION

$$Z1 = \overline{A1 \cdot A2}$$
$$EXP = \overline{A1 \cdot A2 + B1 \cdot B2}$$

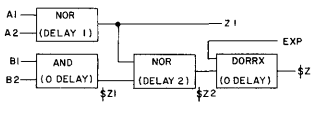
FAIRSIM FORMAT

```
Z   EO2X   A1,A2,B1,B2,EXP,DEL1,DEL2
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

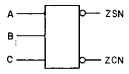
```
&Z      EO2X    &A1,&A2,&B1,&B2,&EXP,&DEL1,&DEL2
&Z      CELL    EO2X
&Z.1    NOR     (&A1,&A2),,&DEL1
$&Z.1   AND     (&B1,&B2),,0
$&Z.2   NOR     ($$&Z.1,$&Z.1),,&DEL2
$&Z     DORRX   ($&Z.2,&EXP),,0
        MEND
```

FA

The FA is an Inverting Full Adder producing $\overline{SUM}$ and $\overline{CARRY}$ functions of the A,B,C inputs. The cell length is 13 grids.

FA

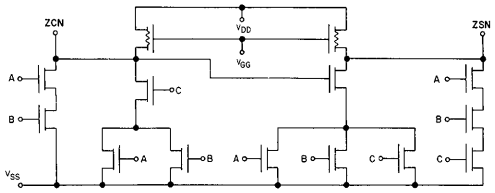
LOGIC SYMBOL



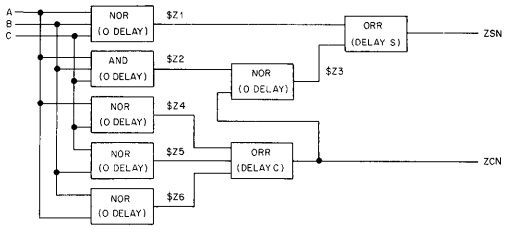
FAIRSIM FORMAT

```
Z   FA   A,B,C,DELSN,DELCN
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

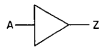
```
&Z      FA      &A,&B,&C,&DELSN,&DELCN
&Z      CELL    FA
$&Z.1   NOR     (&A,&B,&C),,0
$&Z.2   AND     ($$&A,$$&B,$$&C),,0
$&Z.3   NOR     ($&Z.2,$$&Z.C),,0
$&Z.4   NOR     ($$&A,$$&C),,0
$&Z.5   NOR     ($$&B,$$&C),,0
$&Z.6   NOR     ($$&A,$$&B),,0
&Z.SN   ORR     ($&Z.1,$&Z.3),,&DELSN
&Z.CN   ORR     ($&Z.4,$&Z.5,$&Z.6),,&DELC
        MEND
```

ICB

The ICB is a Non-Inverting Input Interface Circuit for DTL or TTL bipolar input levels. The circuit has a nominal threshold hysteresis of 0.4 V. It may be used only with a -12 V VGG. The cell length is 12 grids.

ICB

LOGIC SYMBOL



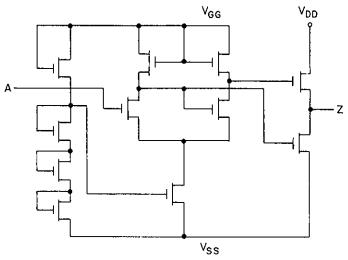
LOGIC EQUATION

$$Z = A$$

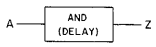
FAIRSIM FORMAT

```
Z   ICB   A,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

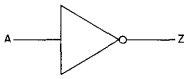
```
&Z   ICB     &A,&DEL
&Z   CELL    ICB
&Z   AND     &A,,&DEL
     MEND
```

INR INRX
INRH INRHX
INRS

The circuits provide logic inversion. The cell length is 2 grids.

INR
INRH
INRS

LOGIC SYMBOL



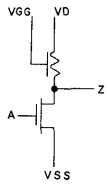
LOGIC EQUATION

$Z = \overline{A}$

FAIRSIM FORMAT

```
Z   *INRX   A,EXP,DEL
```

SCHEMATIC



FAIRSIM MODEL

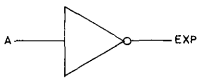
FAIRSIM MACRO

```
&Z  *INR     &A,&DEL
&Z   CELL    INR
&Z   NOR     &A,,&DEL
     MEND
```

*OR INRH, INRS

INRX
INRHX

LOGIC SYMBOL



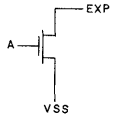
LOGIC EQUATION

$EXP = \overline{A}$

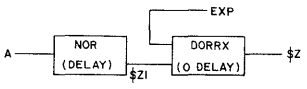
FAIRSIM FORMAT

```
Z   *INR   A,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z     *INRX    &A,&EXP,&DEL
&Z      CELL    INRX
$&Z.1   NOR     &A,,&DEL
$&Z     DORRX   ($&Z.1,&EXP),,0
        MEND
```

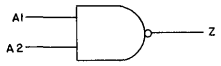
*OR INRHX

ND2 ND2X
ND2H ND2HX

The 2-Input NAND Gate is available with a load resistor (ND2) for normal gate use or without a resistor (ND2X) for expansion of other cells of equal power level. The cell length is 3 grids.

ND2
ND2H

LOGIC SYMBOL



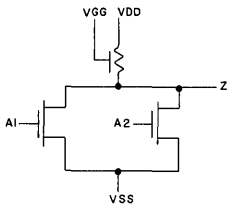
LOGIC EQUATION

$$Z = \overline{A1 \cdot A2}$$

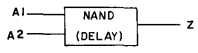
FAIRSIM FORMAT

```
Z  *ND2   A1,A2,DEL
```

SCHEMATIC



FAIRSIM MODEL



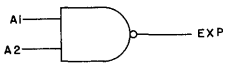
FAIRSIM MACRO

```
&Z  *ND2      &A1,&A2,&DEL
&Z   CELL     ND2
&Z   NAND     (&A1,&A2),,&DEL
     MEND
```

*OR ND2H

ND2X
ND2HX

LOGIC SYMBOL



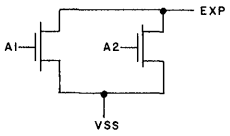
LOGIC EQUATION

$$EXP = \overline{A1 \cdot A2}$$

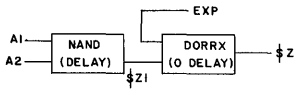
FAIRSIM FORMAT

```
Z *ND2X  A1,A2,EXP,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z    *ND2X     &A1,&A2,&EXP,&DEL
&Z     CELL     ND2X
$&Z.1  NAND     (&A1,&A2),,&DEL
$&Z    DORRX    ($&Z.1,&EXP),,0
       MEND
```

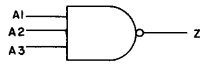
*OR ND2HX

ND3 ND3X
ND3H ND3HX

The 3-Input NAND Gate, ND3, ND3X, is available with a load resistor (ND3) for normal gate use, or without a resistor (ND3X) for expansion of other cells. The cell length is 4 grids.

ND3
ND3H

LOGIC SYMBOL



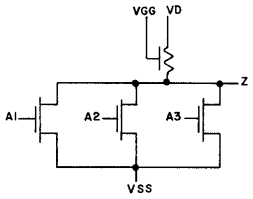
LOGIC EQUATION

$$Z = \overline{A1 \cdot A2 \cdot A3}$$

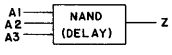
FAIRSIM FORMAT

```
Z  *ND3   A1,A2,A3,DEL
```

SCHEMATIC



FAIRSIM MODEL



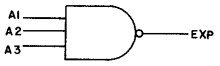
FAIRSIM MACRO

```
&Z  *ND3     &A1,&A2,&A3,&DEL
&Z   CELL    ND3
&Z   NAND    (&A1,&A2,&A3),,&DEL
     MEND
```

*OR ND3H

ND3X
ND3HX

LOGIC SYMBOL



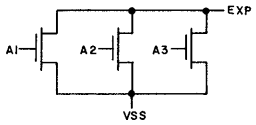
LOGIC EQUATION

$$EXP = \overline{A1 \cdot A2 \cdot A3}$$

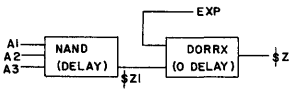
FAIRSIM FORMAT

```
Z  *ND3X   A1,A2,A3,EXP,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z     *ND3X    &A1,&A2,&A3,&EXP,&DEL
&Z      CELL    ND3X
$&Z.1   NAND    (&A1,&A2,&A3),,&DEL
$&Z     DORRX   ($&Z.1,&EXP),,0
        MEND
```

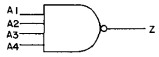
*OR NR3HX

ND4 ND4X
ND4H ND4HX

The 4-Input NAND Gate is available with a load resistor (ND4) for normal gate use, or without a resistor (ND4X) for expansion of other cells. The cell length is 5 grids.

ND4
ND4H

LOGIC SYMBOL



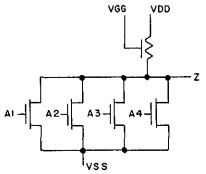
LOGIC EQUATION

$$Z = \overline{A1 \cdot A2 \cdot A3 \cdot A4}$$

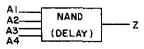
FAIRSIM FORMAT

```
Z  *ND4   A1,A2,A3,A4,DEL
```

SCHEMATIC



FAIRSIM MODEL



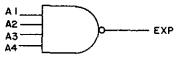
FAIRSIM MACRO

```
&Z  *ND4     &A1,&A2,&A3,&A4,&DEL
&Z   CELL    ND4
&Z   NAND    (&A1,&A2,&A3,&A4),,&DEL
     MEND
```

*OR ND4H

ND4X
ND4HX

LOGIC SYMBOL



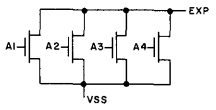
LOGIC EQUATION

$$EXP = \overline{A1 \cdot A2 \cdot A3 \cdot A4}$$

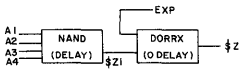
FAIRSIM FORMAT

```
Z  *ND4X  A1,A2,A3,A4,EXP,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z     *ND4X    &A1,&A2,&A3,&A4,&EXP,&DEL
&Z      CELL    ND4X
$&Z.1   NAND    (&A1,&A2,&A3,&A4),,&DEL
$&Z     DORRX   ($&Z.1,&EXP),,0
        MEND
```

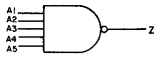
*OR ND4HX

ND5 ND5X
ND5H ND5HX

The 5-Input NAND Gate is available with a load resistor (ND5) for normal gate use, or without a resistor (ND5X) for expansion of other cells. The cell length is 6 grids.

ND5
ND5H

LOGIC SYMBOL



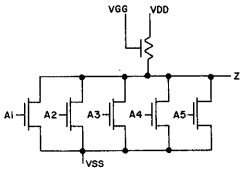
LOGIC EQUATION

$$Z = \overline{A1 \cdot A2 \cdot A3 \cdot A4 \cdot A5}$$

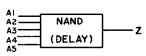
FAIRSIM FORMAT

```
Z  *ND5   A1,A2,A3,A4,A5,DEL
```

SCHEMATIC



FAIRSIM MODEL



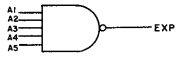
FAIRSIM MACRO

```
&Z  *ND5     &A1,&A2,&A3,&A4,&A5,&DEL
&Z   CELL    ND5
&Z   NAND    (&A1,&A2,&A3,&A4,&A5),,&DEL
     MEND
```

*OR ND5H

ND5X
ND5HX

LOGIC SYMBOL



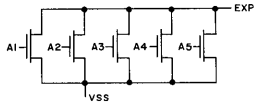
LOGIC EQUATION

$$EXP = \overline{A1 \cdot A2 \cdot A3 \cdot A4 \cdot A5}$$

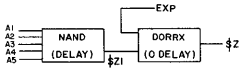
FAIRSIM FORMAT

```
Z  *ND5X  A1,A2,A3,A4,A5,EXP,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z     *ND5X    &A1,&A2,&A3,&A4,&A5,&EXP,&DEL
&Z      CELL    ND5X
$&Z.1   NAND    (&A1,&A2,&A3,&A4,&A5),,&DEL
$&Z     DORRX   ($&Z.1,&EXP),,0
        MEND
```

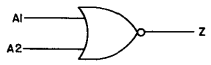
*OR ND5HX

NR2 NR2X
NR2H NR2HX

The 2-Input NOR Gate is available with a load resistor (NR2) for normal logic use, or without a resistor (NR2X) for expansion of other cells of equal power level. The cell length is 3 grids, except NR2H is 4.

NR2
NR2H

LOGIC SYMBOL



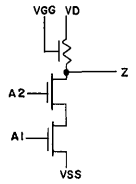
LOGIC EQUATION

$Z = \overline{A1 + A2}$

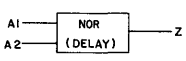
FAIRSIM FORMAT

```
Z *NR2  A1,A2,DEL
```

SCHEMATIC



FAIRSIM MODEL



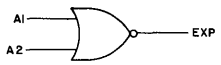
FAIRSIM MACRO

```
&Z   *NR2    (A1,&A2,&DEL
&Z   CELL    NR2
&Z   NOR     (&A1,&A2),,&DEL
     MEND
```

*OR NR2H

NR2X
NR2HX

LOGIC SYMBOL



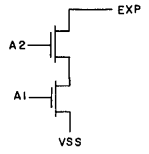
LOGIC EQUATION

$EXP = \overline{A1 + A2}$

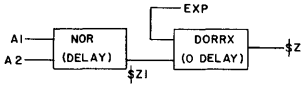
FAIRSIM FORMAT

```
Z  *NR2X  A1,A2,EXP,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z     *NR2X    &A1,&A2,&EXP,&DEL
&Z     CELL     NR2X
$&Z.1  NOR      (&A1,&A2),,&DEL
$&Z    DORRX    ($&Z.1,&EXP),,0
       MEND
```

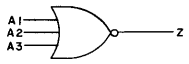
*OR NR2HX

NR3 NR3X
NR3H NR3HX

The 3-Input NOR Gate is available with a load resistor (NR3) for normal logic use, or without a resistor (NR3X) for expansion of other cells. The cell length is 4 grids, except NR3H is 6 grids.

NR3
NR3H

LOGIC SYMBOL



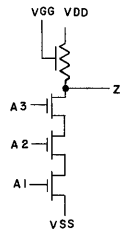
LOGIC EQUATION

$$Z = \overline{A1 + A2 + A3}$$

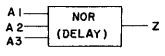
FAIRSIM FORMAT

```
Z   *NR3   A1,A2,A3,DEL
```

SCHEMATIC



FAIRSIM MODEL



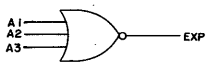
FAIRSIM MACRO

```
&Z   *NR3     &A1,&A2,&A3,&DEL
&Z    CELL    NR3
&Z    NOR     (&A1,&A2,&A3),,&DEL
      MEND
```

*OR NR3H

NR3X
NR3HX

LOGIC SYMBOL



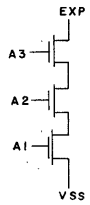
LOGIC EQUATION

$$EXP = \overline{A1 + A2 + A3}$$

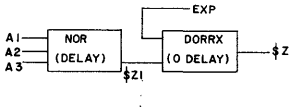
FAIRSIM FORMAT

```
Z *NR3X   A1,A2,A3,EXP,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z    *NR3X     &A1,&A2,&A3,&EXP,&DEL
&Z     CELL     NR3X
$&Z.1  NOR      (&A1,&A2,&A3),,&DEL
$&Z    DORRX    ($&Z.1,&EXP0,,0
       MEND
```

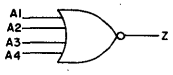
*OR ND3HX

NR4 NR4X
NR4L NR4LX

The 4-Input NOR Gate is available with a load resistor (NR4L or NR4) for normal logic use, or without a resistor (NR4LX or NR4X) for expansion of other cells. The cell length is 6 grids.

NR4
NR4L

LOGIC SYMBOL



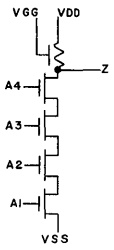
LOGIC EQUATION

$$Z = \overline{A1 + A2 + A3 + A4}$$

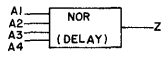
FAIRSIM FORMAT

```
Z  *NR4  A1,A2,A3,A4,DEL
```

SCHEMATIC



FAIRSIM MODEL



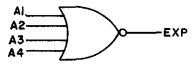
FAIRSIM MACRO

```
&Z     *NR4      &A1,&A2,&A3,&A4,&DEL
&Z      CELL     NR4L
&Z.1    NOR      (&A1,&A2,&A3,&A4),,&DEL
        MEND
```

*OR NR4L

NR4X
NR4LX

LOGIC SYMBOL



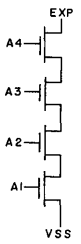
LOGIC EQUATION

$$EXP = \overline{A1 + A2 + A3 + A4}$$

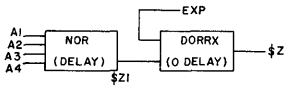
FAIRSIM FORMAT

```
Z  *NR4X  A1,A2,A3,A4,EXP,DEL
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z     *NR4X     &A1,&A2,&A3,&A4,&EXP,&DEL
&Z      CELL     NR4LX
$&Z.1   NOR      (&A1,&A2,&A3,&A4),,&DEL
$&Z     DORRX    ($&Z.1,&EXP),,0
        MEND
```

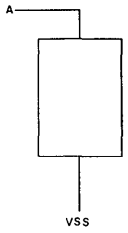
*OR NR4LX

RS1
RS2

The RS provides a controlled geometry device which acts as a load resistor to VSS. It is useful for conditioning inputs from TTL circuitry. The cell length is 2 grids.

RS1
RS2

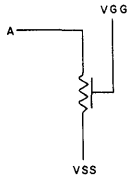
LOGIC SYMBOL



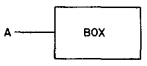
FAIRSIM FORMAT

```
Z  *RS1   A
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z  *RS1    &A
&Z   CELL   RS1
&Z   BOX    &A
     MEND
```

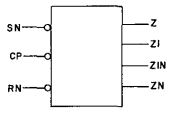
*OR RS2

RSF1A

The Single Phase R-S Master/Slave Flip-Flop, RSF1A, is useful for logic requiring a single phase clock. No asynchronous set or reset inputs are provided. For normal operation CPAM, CPBM, CPAS, and CPBS are commoned as the clock (CP) input. The SN and RN inputs require complemented inputs, i.e., set when SN=0, reset when RN=0. The case SN=RN=0 is not allowed. Both master and slave outputs are available. The slave outputs change state on the positive going clock transition. The cell length is 12 grids.

RSF1A

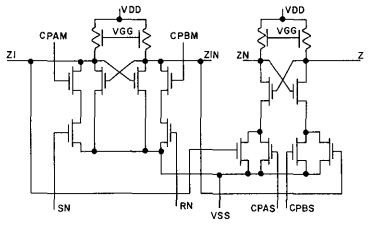
LOGIC SYMBOL



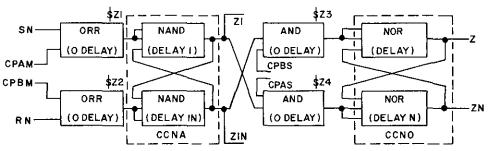
FAIRSIM FORMAT

```
Z  RSF1A  SN,RN,CP,DEL1,DEL1N,DEL,DELN
                    OR
          (CPAM,CPBM,CPAS,CPBS)
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

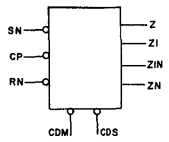
```
&Z      RSF1A       &SN,&RN,&CP,&DEL1,
                    &DEL1N,&DEL,&DELN
&Z      CELL        RSF1A
*       CP(1)=CPAM
        CP(2)=CPBM  CP(3)=CPAS   CP(4)=CPBS
$&Z.1   ORR         (&SN,&CP(1)),,0
$&Z.2   ORR         (&RN,&CP(2)),,0
$&Z.3   AND         ($$&Z.1N,&CP(4)),,0
$&Z.4   AND         ($$&Z.1,&CP(3)),,0
&Z.1    CCNA        $&Z.1,$&Z.1,$&Z.2,$&Z.2,,,&DEL1,&DEL1N
&Z      CCNO        $&Z.4,$&Z.4,$&Z.3,$&Z.3,,,&DEL,&DELN
        MEND
```

RSF1B

RSF1B, the Single Phase R-S Master/Slave Flip-Flop is useful for logic requiring a single phase clock. Asynchronous clear inputs are provided for both master and slave. CDM and CDS are usually commoned to provide a direct clear input. No asynchronous set is provided. For normal operation CPAM, CPBM, CPAS, and CPBS are commoned as the clock (CP) input. The SN and RN inputs require complemented inputs, i.e., set when SN=0, Reset when RN=0. The case SN=RN=0 is not allowed. Both master and slave outputs are available. The slave outputs change state on the positive going clock transition. The cell length is 13 grids.

RSF1B

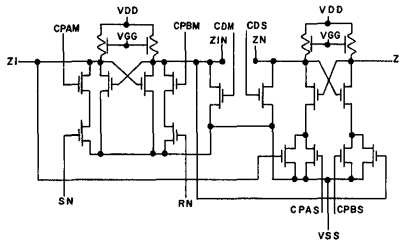
LOGIC SYMBOL



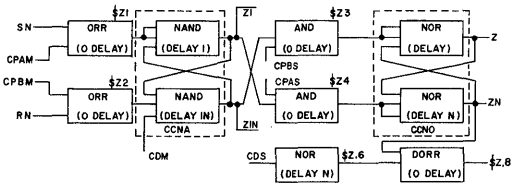
FAIRSIM FORMAT

(CDM,CDS)
OR
Z RSF1B SN,RN,CD,CP,DEL1,DEL1N,DEL,DELN
OR
(CPAM,CPBM,CPAS,CPBS)

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

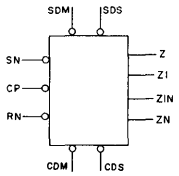
```
&Z      RSF1B     &SN,&RN,&CD,&CP,&DEL1,
                  &DEL1N,&DEL,&DELN
&Z      CELL      RSF1B
*       CP(1)=CPAM CP(2)=CPBM    CP(3)=CPAS    CP(4)=CPBS
*       CD(1)=CDM
        CD(2)=CDS
$&Z.1   ORR       (&SN,&CP(1)),,0
$&Z.2   ORR       (&RN,&CP(2)),,0
$&Z.3   AND       ($$&Z.1N,&CP(4)),,0
$&Z.6   NOR       &CD(2),,&DELN
$&Z.4   AND       ($$&Z.1,&CP(3)),,0
&Z.1    CCNA      $&Z.1,$&Z.1,&CD(1),$&Z.2,,,&DEL1,&DEL1N
&Z      CCNO      $&Z.4,$&Z.4,$&Z.3,$&Z.3,,,&DEL,&DELN
$&Z.8   DORR      ($&Z.6,$$&Z.N),,0
        MEND
```

RSF1C

RSF1C, the Single Phase R-S Master/Slave Flip-Flop is useful for logic requiring a single phase clock. Both asynchronous set and clear inputs are provided to master and slave. CDM and CDS are typically commoned as the SD input. For normal operation CPAM, CPBM, CPAS, and CPBS are commoned as the clock (CP) input. The SN and RN inputs require complemented inputs, i.e., set when SN=0, reset when RN=0. The case SN=RN=0 is not allowed. Both master and slave outputs are available. The slave outputs change state on the positive going clock transition. The cell length is 14 grids.

RSF1C

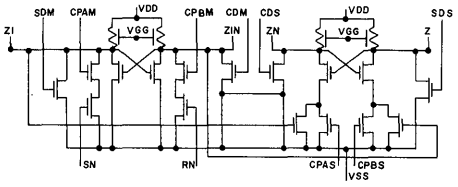
LOGIC SYMBOL



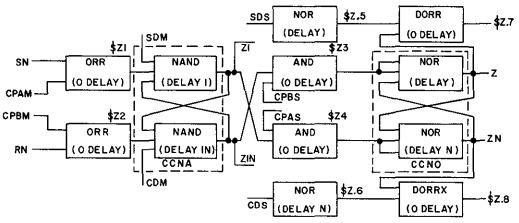
FAIRSIM FORMAT

(SDM,SDS) (CDM,CDS)
OR OR
Z RSF1C SN,RN,SD,CD,CP,DEL1,DEL1N,DEL,DELN
OR
(CPAM,CPBM,CPAS,CPBS)

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

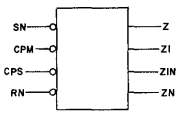
```
&Z      RSF1C     &SN,&RN,&SD,&CD,&CP,&DEL1,&DEL1N,
                  &DEL,&DELN
&Z      CELL      RSF1C
*       CP(1)=CPAM CP(2)=CPBM
        CP(3)=CPAS CP(4)=CPBS
*       SD(1)=SDM  SD(2)=SDS
        CD(1)=CDM  CD(2)=CDS
$&Z.1   ORR       (&SN,&CP(1)),,0
$&Z.2   ORR       (&RN,&CP(2)),,0
$&Z.6   NOR       &CD(2),,&DELN
$&Z.4   AND       ($$&Z.1,&CP(3)),,0
$&Z.5   NOR       $SD(2),,&DEL
$&Z.3   AND       $$&Z.1N,&CP(4)),,0
&Z.1    CCNA      &SD(1),$&Z.1,&CD(1),$&Z.2,,,&DEL1,&DEL1N
&Z      CCNO      $&Z.4,$&Z.4,$&Z.3,$&Z.3,,,&DEL,&DELN
$&Z.7   DORR      ($&Z.5,$$&Z),,0
$&Z.8   DORR      ($&Z.6,$$&Z.N),,0
        MEND
```

RSF2A

RSF2A, the 2-Phase R-S Master/Slave Flip-Flop is useful for logic having a 2-phase clock available. No asynchronous set or reset inputs are provided. For normal operation CPAM and CPBM are commonedas CPM input, CPAS and CPBS are commoned as CPS input. The set operation is performed when SN LOW and RN HIGH and the clock is LOW. CPM and CPJ are not allowed LOW simultaneously in normal operation. Both master and slave outputs are available. The cell length is 11 grids.

RSF2A

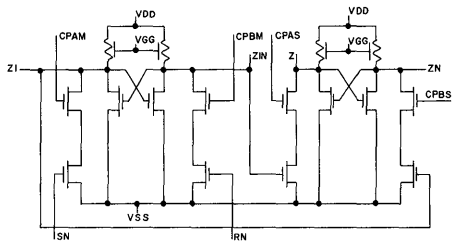
LOGIC SYMBOL



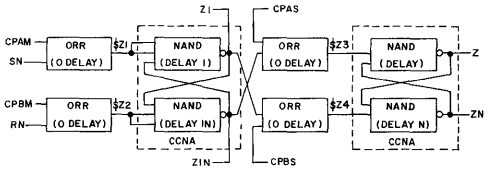
FAIRSIM FORMAT

Z RSF2A SN,RN,CPM,CPS,DEL1,DEL1N,DEL,DELN
OR OR
(CPAM,CPBM) (CPAS,CPBS)

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

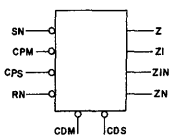
```
&Z      RSF2A   &SN,&RN,&CPM,&CPS,&DEL1,&DEL1N,&DEL,
                &DELN
&Z      CELL    RSF2A
*       CPM(1)=CPAM  CPM(2)=CPBM  CPS(1)=CPAS
                CPS(2)=CPBS
$&Z.1   ORR     (&SN,&CPM(1)),,0
$&Z.2   ORR     (&RN,&CPM(2)),,0
$&Z.3   ORR     ($$&Z.N,&CPS(1)),,0
$&Z.4   ORR     ($$&Z.,&CPS(2)),,0
&Z.1    CCNA    &Z.1,$&Z.1,$&Z.2,$&Z.2,,,&DEL1,&DEL1N
&Z      CCNA    $&Z.3,$&Z.3,$&Z.4,$&Z.4,,,&DEL,&DELN
        MEND
```

RSF2B

RSF2B, the 2-Phase R-S Master/Slave Flip-Flop is useful for logic having a 2-phase clock available. Asynchronous clear inputs are provided for both master and slave. For normal operation CPAM and CPBM are commoned as CPM input, CPAS and CPBS are commoned as CPS input. The set operation is performed when SN=LOW and RN=HIGH and the clock is LOW. CPM and CPS are not allowed LOW simultaneously in normal operation. Both master and slave outputs are available. The cell length is 12 grids.

RSF2B

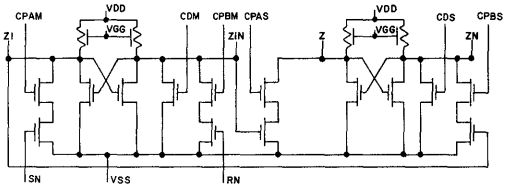
LOGIC SYMBOL



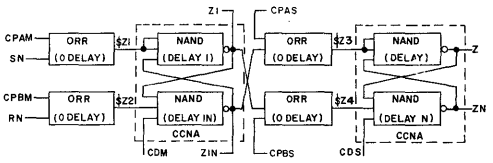
FAIRSIM FORMAT

(CDM,CDS)
OR
Z RSF2B SN,RN,CD,CPM,CPS,DEL1,DEL1N,DEL,DELN
OR OR
(CPAM,CPBM) (CPAS,CPBS)

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

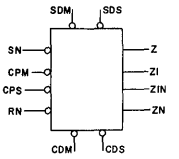
```
&Z      RSF2B   &SN,&RN,&CD,&CPM,&CPS,&DEL1,&DEL1N,
                &DEL, &DELN
&Z      CELL    RSF2B
*       CPM(1)=CPAM  CPM(2)=CPBM  CPS(1)=CPAS
        CPS(2)=CPBS
*       CD(1)=CDM   CD(2)=CDS
$&Z.1   ORR     (&SN,&CPM(1)),,0
$&Z.2   ORR     (&RN,&CPM(2)),,0
$&Z.3   ORR     ($$&Z.N,&CPS(1)),,0
$&Z.4   ORR     ($$&Z.,&CPS(2)),,0
&Z.1    CCNA    $&Z.1,$&Z.1,$&Z.2,&CD(1),,&DEL1,&DEL1N
&Z      CCNA    $&Z.3,$&Z.3,$&Z.4,&CD(2),,&DEL,&DELN
        MEND
```

RSF2C

RSF2C, the 2-Phase R-S Master/Slave Flip-Flop is useful for logic having a 2-phase clock available. Both asynchronous set and clear inputs are provided to master and slave. For normal operation CPAM and CPBM are commoned as CPM input, CPAS and CPBS are commoned as CPS input. The set operation is performed when SN=LOW and RN=HIGH and the clock is LOW. CPM and CPS are not allowed LOW simultaneously in normal operation. Both master and slave outputs are available. The cell length is 13 grids.

RSF2C

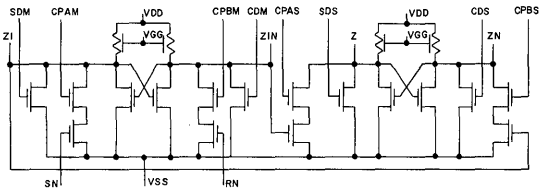
LOGIC SYMBOL



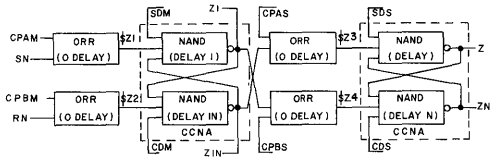
FAIRSIM FORMAT

(SDM,SDS) (CDM,CDS)
OR OR
Z RSF2C SN,RN,SD,CD,CPM,CPS,DEL1,DEL1N,DEL,DELN
OR OR
(CPAM,CPBM) (CPAS,CPBS)

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

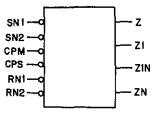
```
&Z      RSF2C       &SN,&RN,&SD,&CD,&CPM,&CPS,
                    &DEL1,&DEL1N,
                    &DEL,&DELN
&Z      CELL        RSF2C
*       CPM(1)=CPAM  CPM(2)=CPBM
        CPS(1)=CPAS  CPS(2)=CPBS
*       SD(1)=SDM   SD(2)=SDS
        CD(1)=CDM   CD(2)=CDS
$&Z.1   ORR         (&SN,&CPM(1)),,0
$&Z.2   ORR         (&RN,&CPM(2)),,0
$&Z.3   ORR         ($$&Z.N,&CPS(1)),,0
$&Z.4   ORR         ($$&Z.,&CPS(2)),,0
&Z.1    CCNA        $&Z.1,&SD(1),$&Z.2,&CD(1),&DEL1,&DEL1N
&Z      CCNA        $&Z.3&SD(2),$&Z.4,&CD(2),,,&DEL,&DELN
        MEND
```

RSF3A

RSF3A, the 2-Phase R-S Master/Slave Flip-Flop is useful for circuits having 2-phase clocks available. No asynchronous inputs are provided. For normal operation CPAM and CPBM are commoned as the master clock, CPAS and CPBS as the slave clock. The flip-flop may be connected as a J K by connecting Z to SN and ZN to RN. The cell length is 15 grids.

RSF3A

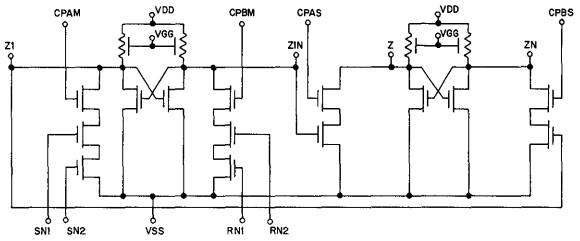
LOGIC SYMBOL



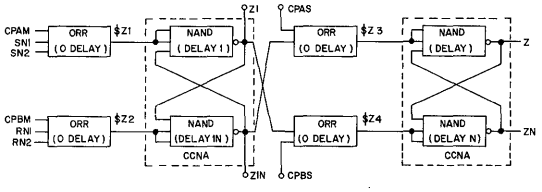
FAIRSIM FORMAT

Z RSF3A SN1,SN2,RN1,RN2,CPM,CPS,DEL1,DEL1N,DEL,DELN
OR OR
(CPAM,CPBM) (CPAS,CPBS)

SCHEMATIC



FAIRSIM MODEL

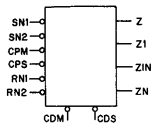


RSF3B
RSF4B

RSF3B, the 2-Phase R-S Master/Slave Flip-Flop is useful for logic having 2-phase clocks available. Asynchronous clear inputs are provided on both master and slave. For normal operation CPAM and CPBM are commoned as the master clock, CPAS and CPBS as the slave clock. It can be connected as a J K flip-flop by connecting Z to SN and ZN to RN. RSF4B has the same description except it has no CDS. The cell length is 15 grids.

RSF3B
RSF4B

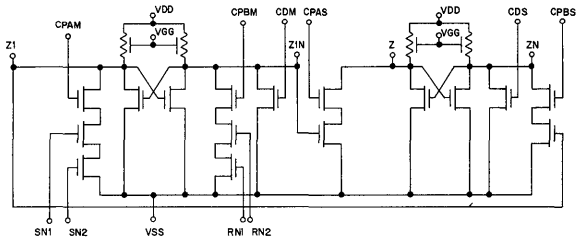
LOGIC SYMBOL



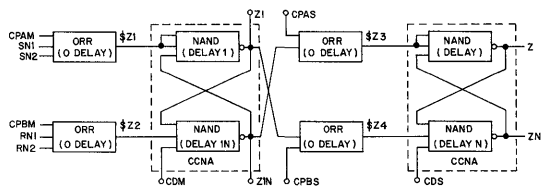
FAIRSIM FORMAT

(CDM,CDS)
OR
Z RSF3B SN1,SN2,RN1,RN2,CD,CPM,CPS,DEL1,
DEL1N,DEL,DELN
OR OR
(CPAM,CPBM) (CPAS,CPBS)

SCHEMATIC



FAIRSIM MODEL

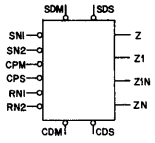


RSF3C
RSF4C

RSF3C, the 2-Phase R-S Master/Slave Flip-Flops are useful for circuits having 2-phase clocks available. Asynchronous set and resets are provided on both master and slave. For normal operation CPAM and CPBM are commoned as the master clock CPAS and CPBS as the slave clock. The flip-flop may be connected as a J K flip-flop by connecting Z to SN to ZN to RN. RSF4C has the same description except it has no SDS nor CDS. The cell length is 15 grids.

RSF3C
RSF4C

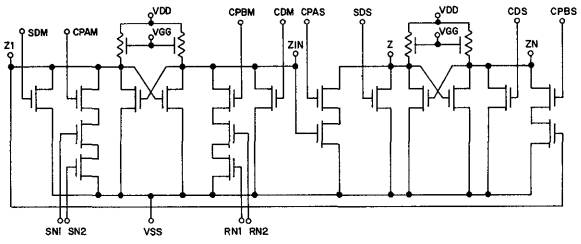
LOGIC SYMBOL



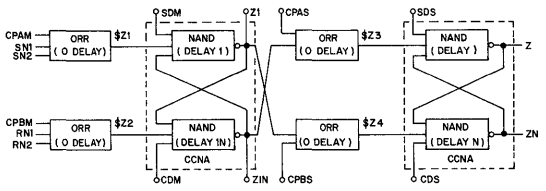
FAIRSIM FORMAT

(SDM,SDS) (CDM,CDS)
OR OR
Z RSF3C SN1,SN2,RN1,RN2,SD,CD,CPM,CPS,DEL1,DEL1N,
DEL,DELN
OR OR
(CPAM,CPBM) (CPAS,CPBS)

SCHEMATIC



FAIRSIM MODEL



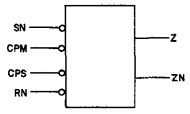
RSFQA
RSFQAH

RSFQA, the R-S Flip-Flop utilizes a 2-phase clock and stored charge effects to provide small size and power. A 2-phase clock is required: CPM must have a larger than normal signal swing, which may be provided by an on chip clock generator or externally. CPS is a normal logic level. The period between the positive going signal transition of CPM and the negative going transition of CPS must not exceed a worst case limit, typically 0.1 ms. At 0°C to 70°C.

RSFQA 7 grids
RSFQAH 9 grids

RSFQA
RSFQAH

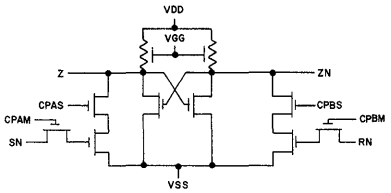
LOGIC SYMBOL



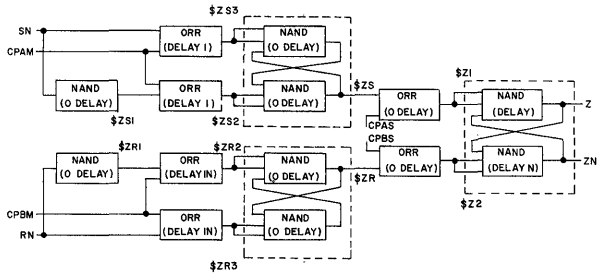
FAIRSIM FORMAT

Z RSFQA SN,RN,CPM,CPS,DEL1,DEL1N,DEL,DELN
OR OR
(CPAM,CPBM) (CPAS,CPBS)

SCHEMATIC



FAIRSIM MODEL



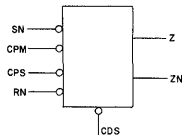
FAIRSIM MACRO

```
&Z      RSFQA   &SN,&RN,&CPM,&CPS,&DEL1,
                &DEL1N,&DEL,&DELN
&Z      CELL    RSFQA
*       CPM(1)=CPAM  CPM(2)=CPBM  CPS(1)=CPAS
        CPS(2)=CPBS
$&Z.S1  NAND    &SN,,0
$&Z.S2  ORR     (&CPM1,$&Z.S1),,&DEL1
$&Z.S3  ORR     ($$&SN,$$&CPM1),,&DEL1
$&Z.$S  NAND    ($&Z.S2,$&Z.$SN),,0
$&Z.$SN NAND    ($&Z.S3,$&Z.$S),,0
$&Z.R1  NAND    &RN,,0
$&Z.R2  ORR     (&CPM2,$&Z.R1),,&DEL1N
$&Z.R3  ORR     ($$&RN,$$&CPM2),,&DEL1N
$&Z.$R  NAND    ($&Z.R2,$&Z.$RN),,0
$&Z.$RN NAND    ($&Z.R3,$&Z.$R),,0
$&Z.1   ORR     ($&Z.$S,&CPS1),,0
$&Z.2   ORR     ($&Z.$R,&CPS2),,0
&Z      CCNA    $&Z.1,$&Z.1,$&Z.2,$&Z.2,,,&DEL,&DELN
        MEND
```

RSFQB
RSFQBH

RSFQB, the R-S Flip-Flop utilizes a 2-phase clock and stored charge effects to provide small size and power. A 2-phase clock is required: CPM must have a larger than normal signal swing, which may be provided by an on chip clock generator or externally. CPS is a normal logic level. The period between the positive going signal transition of CPM and the negative going transition of CPS must not exceed a worst case limit, typically 0.1 ms at 0°C to 70°C. The CD input resets the slave only. Aside from the clock and clear limitations, the RSFQB is logically identical to the RSF2B.
RSFQB 7 grids
RSFQBH 9 grids

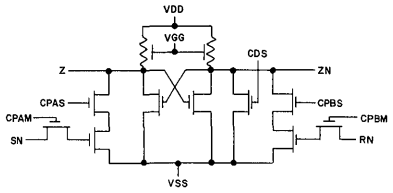
RSFQB
RSFQBH



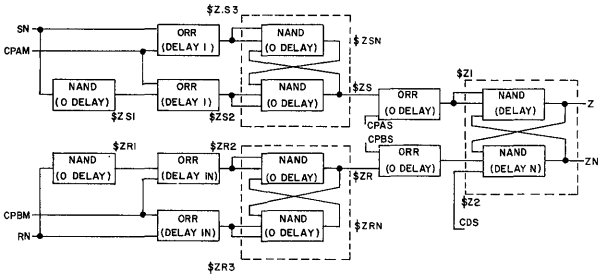
FAIRSIM FORMAT

Z RSFQB SN,RN,CDS,CPM,CPS,DEL1,DEL1N,DEL,DELN

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

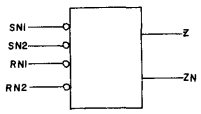
```
&Z      RSFQB   &SN,&RN,&CDS,&CPM,&CPS,&DEL1,
                &DEL1N,&DEL, &DELN
&Z      CELL    RSFQB
*       CPM(1)=CPAM  CPM(2)=CPBM  CPS(1)=CPAS
        CPS(2)=CPBS
$&Z.S1  NAND    &SN,,0
$&Z.S2  ORR     (&CPM1,$&Z.S1),,&DEL1
$&Z.S3  ORR     ($$&SN,$$&CPM1),,&DEL1
$&Z.$S  NAND    ($&Z.S2,$&Z.$SN),,0
$&Z.$SN NAND    ($&Z.3,$&Z.$S),,0
$&Z.R1  NAND    &RN,,0
$&Z.R2  ORR     (&CPM2,$&Z.R1),,&DEL1N
$&Z.R3  ORR     ($$&RN,$$&CPM2),,&DEL1N
$&Z.$R  NAND    ($&Z.R2,$&Z.$RN),,0
$&Z.$RN NAND    ($&Z.R3,$&Z.$R),,0
$&Z.1   ORR     ($&Z.$S,&CPS1),,0
$&Z.2   ORR     ($&Z.$R,&CPS2),,0
&Z      CCNA    $&Z.1,$&Z.1&CDS,$&Z.2,,,&DEL,&DELN
        MEND
```

RSLA

RSLA, this latch provides a single bit of storage. It is set when SN1 and SN2 are at logic "0", reset when RN1 and RN2 are at logic "0". The cell length is 7 grids.

RSLA

LOGIC SYMBOL



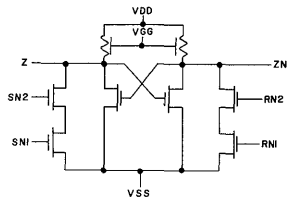
LOGIC EQUATION

$$\text{SET } (Z=1) = \overline{SN1} \cdot \overline{SN2} \cdot (RN1 + RN2)$$
$$\text{RESET } (ZN=1) = (SN1 + SN2) \cdot \overline{RN1} \cdot \overline{RN2}$$

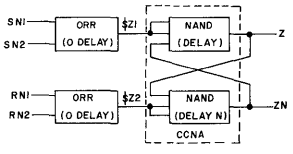
FAIRSIM FORMAT

```
Z  RSLA SN1,SN2,RN1,RN2,DEL,DELN
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

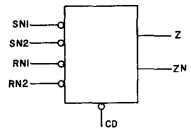
```
&Z      RSLA   &SN1,&SN2,&RN1,&RN2,&DEL,&DELN
&Z      CELL   RSLA
$&Z.1   ORR    (&SN1,&SN2),,0
$&Z.2   ORR    (&RN1,&RN2),,0
&Z      CCNA   $&Z.1,$&Z.2,$&Z.2,,,&DEL,&DELN
        MEND
```

RSLB RSLBS RSLBH

RSLB, this latch provides a single bit of storage. It is set when SN1 and SN2 are at logic "0", reset when RN1 and RN2 are at logic "0" or CD is at logic "0". The cell length is 7 grids.

RSLB
RSLBH
RSLBS

LOGIC SYMBOL



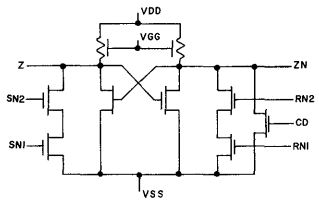
LOGIC EQUATION

$$\text{SET } (Z=1) = \overline{SN1} \cdot \overline{SN2} \cdot CD \cdot (RN1 + RN2)$$
$$\text{RESET } (ZN=1) + (SN1 + SN2) \cdot (\overline{CD} + \overline{RN1} \cdot \overline{RN2})$$

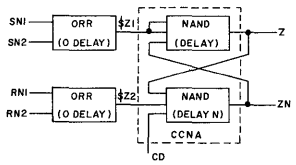
FAIRSIM FORMAT

```
Z  *RSLB SN1,SN2,RN1,RN2,CD,DEL,DELN
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z      *RSLB  &SN1,&SN2,&RN1,&RN2,&CD,&DEL,&DELN
&Z      CELL   RSLB
$&Z.1   ORR    (&SN1,&SN2),,0
$&Z.2   ORR    (&RN1,&RN2),,0
&Z      CCNA   $&Z.1,$&Z.1,$&Z.2,&CD,,,&DEL,&DELN
        MEND
```

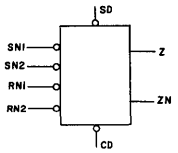
*OR RSLBH, RSLBS

RSLC

RSLC, this latch provides a single bit of storage. It is set when SN1 and SN2 are at logic "0"; reset when RN1 and RN2 are at logic "0" or CD is at logic "0". The cell length is 7 grids.

RSLC

LOGIC SYMBOL



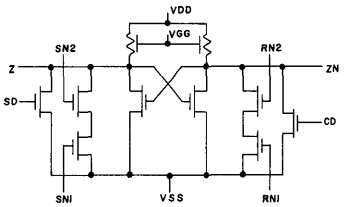
LOGIC EQUATION

$$SET\ (Z=1) = \overline{(SD} + \overline{SN1}\ \overline{SN2)} \cdot CD \cdot (RN1 + RN2)$$
$$RESET\ (ZN=1) = SD\ (SN1 + SN2)\ \overline{CD} = \overline{RN1}\ \overline{RN2)}$$

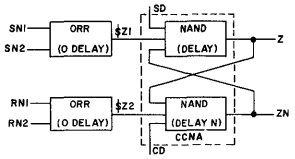
FAIRSIM FORMAT

```
Z   RSLC  SN1,SN2,RN1,RN2,CD,SD,DEL,DELN
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

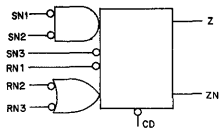
```
&Z      RSLC    &SN1,&SN2,&RN1,&RN2,&CD,&SD,&DEL,&DELN
&Z      CELL    RSLC
$&Z.1   ORR     (&SN1,&SN2),,0
$&Z.2   ORR     (&RN1,&RN2),,0
&Z      CCNA    $&Z.1,&SD,$&Z.2,&CD,,,&DEL,&DELN
        MEND
```

RSL1

RSL1, this latch is a high speed special logic function. SN3 and RN1 should be the critical speed signals. Cell length is 15 grids.

RSL1

LOGIC SYMBOL



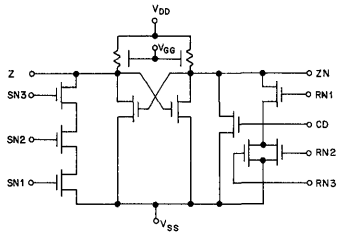
LOGIC EQUATION

$$SET(Z=1) = SN1\ SN2\ SN3\ CD\ RN1\ (RN2+RN3)$$
$$RESET(ZN=1) = CD+RN1\ (RN2+RN3)\ (SN1+SN2+SN3)$$

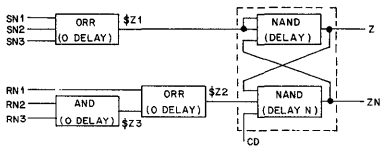
FAIRSIM FORMAT

```
Z   RSL1  SN1,SN2,SN3,RN1,RN2,RN3,CD,DEL,DELN
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

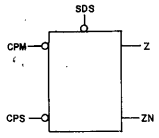
```
&Z      RSL1    &SN1,&SN2,&SN3,&RN1,RN2,&RN3,&CD,
                &DEL,&DELN
&Z      CELL    RSL1
$&Z.1   ORR     (&SN1,&SN2,&SN3),,0
$&Z.2   ORR     (&RN1,$&Z.3),,0
$&Z.3   AND     (&RN2,&RN3),,0
&Z      CCNA    $&Z.1,$&Z.1,$&Z.2,&CD,,,&DEL,&DELN
        MEND
```

TFQBL

TFQBL, the T Flip-Flop utilizes a 2-phase clock and stored charge effects to provide small size and minimum power for ripple counters where speed is not critical. Asynchronous set direct is provided for the slaves only. The ZN output provides a larger output swing to drive the master clock phase or another TFQBL directly. When driving other than another TFQBL, clock timing has the same constraints as the RSFQB. Cell length is 9 grids.

TFQBL

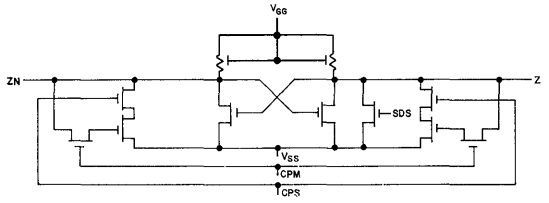
LOGIC SYMBOL



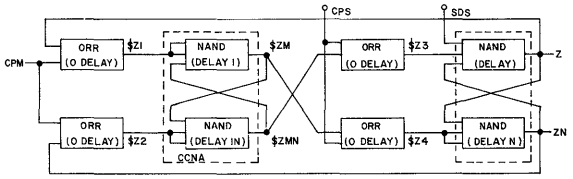
FAIRSIM FORMAT

```
Z   TFQBL SDS,CPM,CPS,DEL1,DEL1N,DEL,DELN
```

SCHEMATIC



FAIRSIM MODEL



FAIRSIM MACRO

```
&Z      TFQBL   &SDS,&CPM,&CPS,&DEL1,&DEL1N,&DEL,
                &DELN
&Z      CELL    TFQBL
$&Z.1   ORR     ($$&Z,&CPM),,0
$&Z.2   ORR     ($$&Z.N,$$&CPM),,0
$&Z.3   ORR     ($&Z.MN,&CPS),,0
$&Z.4   ORR     ($&Z.M,$$&CPS),,0
$&Z.M   CCNA    $&Z.1,$&Z.1,$&Z.2,$&Z.2,,,&DEL1,&DEL1N
&Z      CCNA    &SDS,$&Z.3,$&Z.4,$&Z.4,,,&DEL,&DELN
        MEND
```

COMPOSABLE LOGIC MATRIX (CLM)

A special Micromosaic cell, the Composable Logic Matrix or CLM, saves area and propagation time when used to replace conventional combinatorial logic. It is basically a sum-of-products generator. Any function of the input variables can be generated at the output with only three inverter delays. The CLM's usefulness in on chip ROM and logic applications is enhanced by these features:

1. *UNIQUE INPUTS* — These save input variables, thereby reducing the chip area required for the matrix. Variables that occur only in a single product may be connected to one of the unique inputs at the side of the matrix. If a function of more than one variable is unique to a given product, that function may be generated with a gate cell external to the CLM.
2. *BI-DIRECTIONAL* — Input variables, product terms and sum terms are available at both ends of the matrix and can be used as inputs to other cells on the chip. This places them in more convenient locations. Also, product terms used elsewhere on the chip need only be generated once.
3. *EASILY PROGRAMMED* — Logic programming is concurrent with chip design. The CLM is programmed like a ROM and generates an output sum-of-products with only three inversions.
4. *NO EXTRA PROCESSING STEPS* — The CLM does not require separate mask-programming. It is processed with the other cells on the chip.

Length and width of the CLM are both variable. Dimensional factors are:

I = number of inputs or input variables

P = number of products or ROM words

S = number of outputs or sum terms

The length of the CLM is 41 + 3S + 14 mils while the width is P + 2 mils. The logic and schematic diagram of the CLM is given in *Figures D-6* and *D-7*.

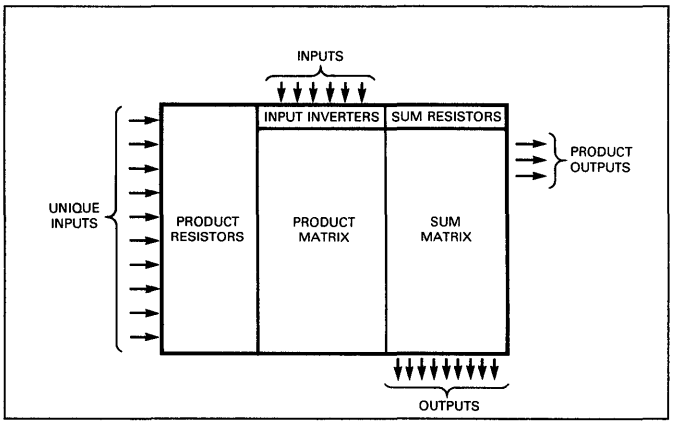


Fig. D-6. CLM Block Diagram

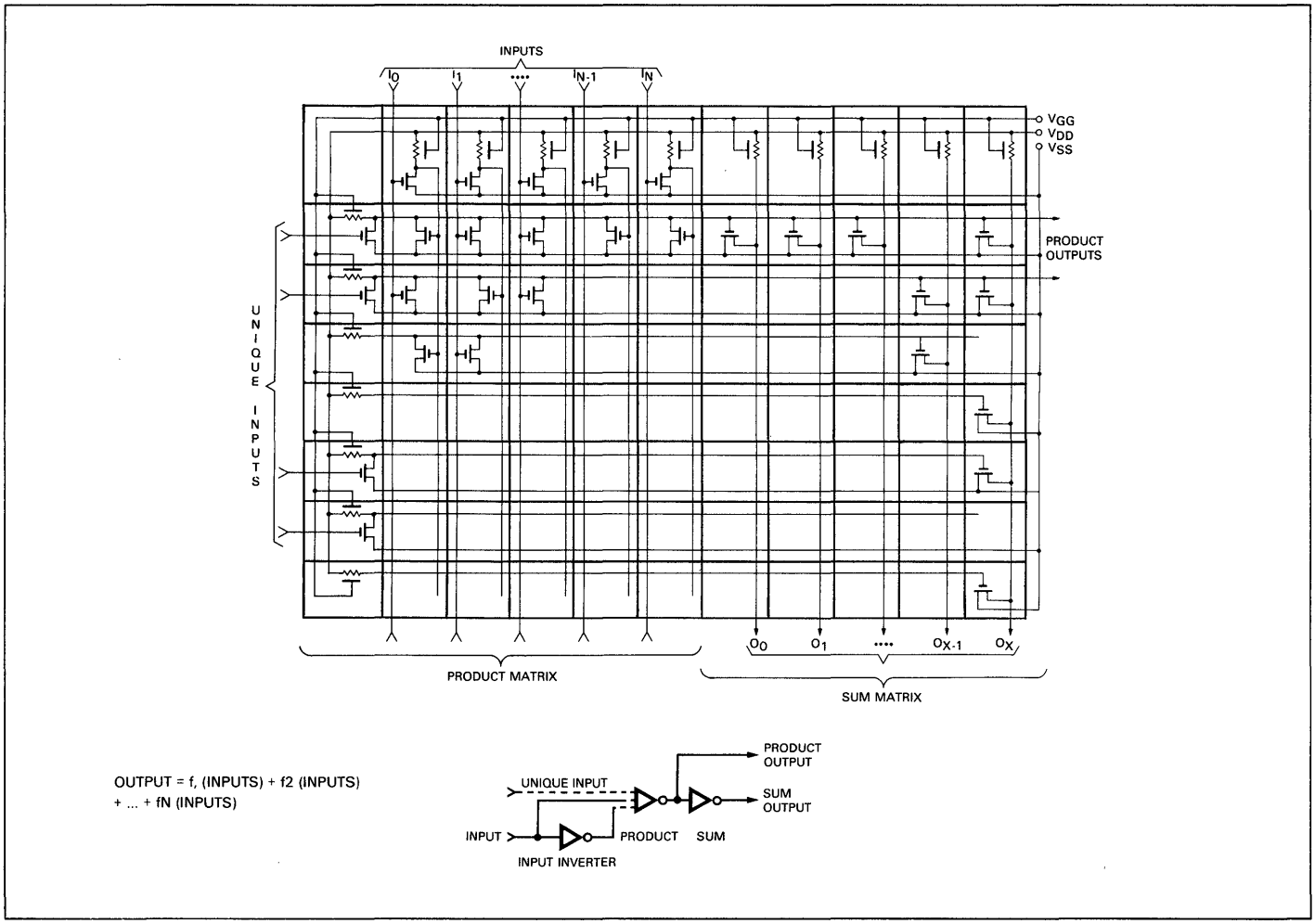


Fig. D-7. CLM Schematic

CHIP SIZE, POWER AND DELAY ESTIMATES

Delay in a string of MOS circuits varies with nodal capacitances and chip temperature, as well as operating levels. Part of the nodal capacitances are interconnect capacitances which are related to chip size. Temperature is related to power dissipation. Thus, it is convenient to estimate size and power first.

These calculations hold only for combinations of gates, complex gates and buffers. Consult Fairchild for details and computer analysis of circuits containing flip-flops, dynamic cells or CLMs. The parameters required for the calculations are given in *Table D-2* for gates and *Table D-3* for buffers.

GATES AND COMPLEX GATES

TABLE D-2

CELL NAME	CELL LENGTH GRIDS	DRIVE FACTOR P	C_{IN} pF	C_{OUT} pF	AVG POWER	CELL NAME	CELL LENGTH GRIDS	DRIVE FACTOR P	C_{IN} pF	C_{OUT} pF	AVG POWER
AO1	5	1	.21	.24	.45	ND3HX	4	1/2	.22	.25	
AO1H	7	1/2	.42	.26	.90	ND3X	4	1	.11	.20	
AO1HX	5	1/2	.42	.26		ND4	5	1	.11	.23	.45
AO1X	5	1	.21	.20		ND4H	5	1/2	.22	.22	.90
AO2	7	1	.28	.25	.45	ND4HX	5	1/2	.22	.22	
AO2X	7	1	.28	.20		ND4X	5	1	.11	.23	
				Z .24		ND5	6	1	.11	.23	.45
AO3	6	1	.21		.45	ND5H	6	1/2	.22	.22	.90
				Z1 .50		ND5HX	6	1/2	.22	.22	
AO4	5	1	.21	.24	.45	ND5X	6	1	.11	.20	
AO4H	7	1/2	.50	.40	.90	NR2	3	1	.21	.24	.45
AO5	4	1	.21	.24	.45	NR2H	4	1/2	.42	.26	.90
INR	2	1	.11	.23	.45	NR2HX	3	1/2	.42	.24	
INRH	2	1/2	.22	.25	.90	NR2X	3	1	.21	.22	
INRHX	2	1/2	.22	.25		NR3	4	1	.28	.25	.45
INRS	3	1/4	.44	.28	1.80	NR3H	6	1/2	.56	.27	.90
INRX	2	1	.11	.22		NR3HX	6	1/2	.38	.25	
ND2	3	1	.11	.23	.45	NR3X	4	1	.28	.20	
ND2H	3	1/2	.22	.22	.90	NR4	6	1	.38	.25	.45
ND2HX	3	1/2	.22	.22		NR4L	5	2	.21	.23	.22
ND2X	3	1	.11	.22		NR4LX	5	2	.21	.20	
ND3	4	1	.11	.23	.45	NR4X	6	1	.38	.20	
ND3H	4	1/2	.22	.25	.90						

BUFFERS

TABLE D-3

BUFFER NAME	CELL LENGTH GRIDS	CELL WIDTH GRIDS	C_{IN} pF	AVG. POWER mw	AVG. DELAY ns	DRIVER GATE	LOAD
BFT2	10	17	1.6	31.5			
BFT2X	10	17	1.6	6.5			
BUFB1	17	17	3.0	24.0	40	INRH	1 TTL + 20 pF
BUFB2	16	8	1.3				
BUFB3	26	17	4.3	24.0	61	INRH	1 TTL + 100 pF
BUFB4	16	17	1.8	12.0			
BUFB5	22	8	1.8	12.0			
			In 1.5				
BUFG1	19	17		26.0	85	INRH	100 pF
			Enable 2.3				
BUFM1	14	8	2.8	9.0	37	INRH	20 pF
BUFM2	8	8	1.75	4.2	50	INR	20 pF
BUFM3	13	17	2.8	9.0	37	INRH	20 pF
BUFM4	18	17	1.75	4.2	50	INR	20 pF
BUFM6	4	8	.45	1.9	53	INR	5 pF
BUFT1	6	8	.4	4.2			
BUFX1	6	8	.4	4.2			
BUFX2	4	8	.7				
BUFX3	14	17	2.3	24.0	48	INRH	1 TTL + 25 pF 4.3 K
BUFX4	18	8	1.15	12.0			

Size Estimates

Chip size may be determined by adding the grid numbers of all the cells to be used on a chip in conjunction with the curve in *Figure D-8.* This curve allows for pads and scribe lines and assumes a normal amount of interconnection (60% of cell area). Interconnection area may be much less if matrices or shift register cells are used. If 400 grids are used, the approximate die size will be 100 x 100 mils.

Power and Temperature

Average cell dissipation is available from the data in *Tables D-2* and *D-3.* The maximum junction temperature will be:

$$T_{j(max)} = P_{D(total)}\,\Theta_{JA} + T_{A(max)}$$

where Θ_{JA} is the specified package thermal resistance in °C/watt and $T_{A(max)}$ is maximum ambient temperature.

Delay Estimates

The variables affecting speed of a Micromosaic logic path have been reduced to three easily determined quantities: K, a speed factor expressed in nanoseconds/picofarad of internal capacitances; C_i, the capacitances of each internal node; and P_i, the power factor of the cells driving the nodes. When multiplied together and added to buffer delay, these give a total path delay:

$$t_{D(path)} = K \Sigma P_i C_i + t_{D(buffer)}$$

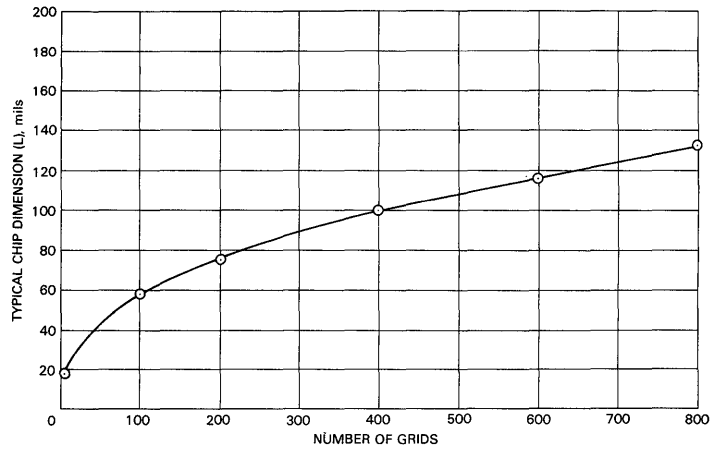
K Factor

The K factor is defined as:

$$K = t_{TYP} F_{VSS} F_{temp}$$

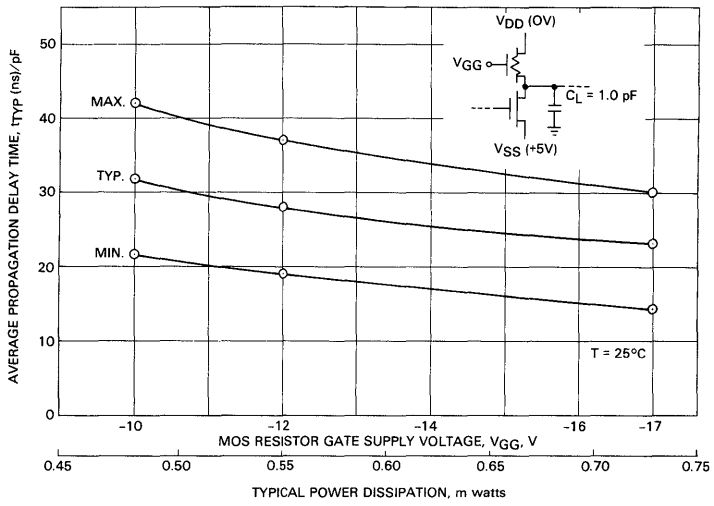
where t_{TYP} is defined by *Figure D-9,* F_{VSS} by *Figure D-10,* and F_{temp} by *Figure D-11.* For example, let us find K for the worst case supply variations and temperature of a circuit operating at:

V_{DD} = 0 V
V_{GG} = −12 V ± 0.5 V
V_{SS} = +5 V ± 5%
$P_{D(avg)}$ = 200 mW
ΘJA = 46°/W
T_A = 0 to 70°C



This curve shows the estimated chip length "L" as function of total number of cell grids. L is in mils, so chip area in square mils equals L^2. A ratio of 40% cells to 60% interconnections is assumed.

Fig. D-8. Estimating Chip Size



These curves show t_{TYP} for 3402 logic cells as a function of V_{GG} and power dissipation. The delay factor t_{TYP} is a nanoseconds/picofarad value, not the actual delay time.

Fig. D-9. t_{TYP} as a Function of V_{GG} and Power Dissipation.

First, t_{TYP} is found at its lowest value with respect to V_{DD}. Since V_{DD} = 0 V, we use the least negative absolute value of V_{GG}, −11.5 V, and *Figure D-9* shows that t_{TYP} will be 37 ns/pF.

Second, at V_{SS} = +4.75 V, we find F_{VSS} = 1.03 with *Figure D-10.*

Third, from the T_j equation:

$$T_{j(max)} = 46°/W\ (200\ mW) + 70°C = 79.2°C$$

Therefore, using *Figure D-11*, F_{temp} = 1.25.

Multiplying:

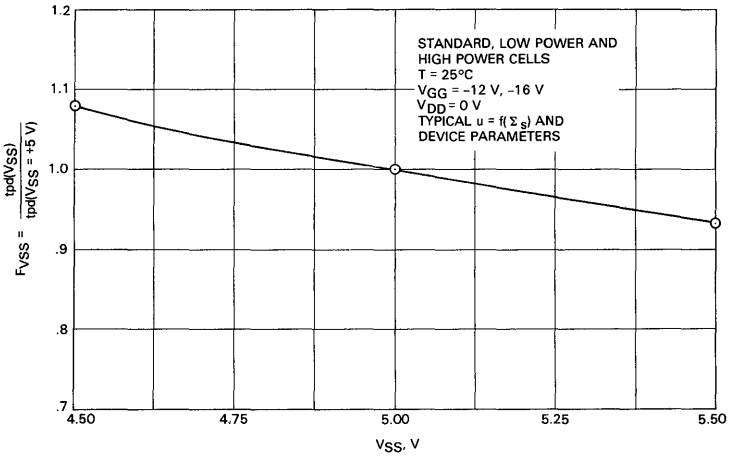
$$K = (37\ ns/pF)\ (1.03)\ (1.25) = 46.7\ ns/pF$$

Nodal Capacitances

The capacitance at each node in the logic path will be the sum of the cell input capacitances C_{in}, the cell output capacitances C_{out} and the interconnect capacitances C_{int} connected to the given node, or:

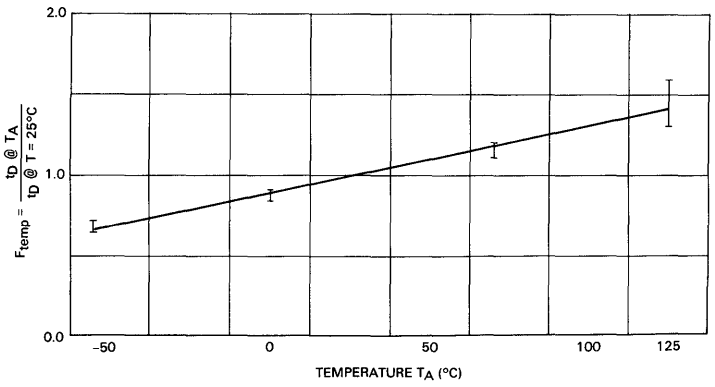
$$C_i = \Sigma\ C_{in} + \Sigma\ C_{out} + \Sigma\ C_{int}$$

Each C_{in} and C_{out} is obtained from *Tables D-2* and *D-3.* Each C_{int} is found in *Figure D-12.* The chip size is estimated as before, the number of interconnect lines connected to the given node is counted to determine fan out, and C_{int} is read from the appropriate fan out curve. The curves assume nominal interconnect lengths for the chip size that was obtained with *Figure D-8.*



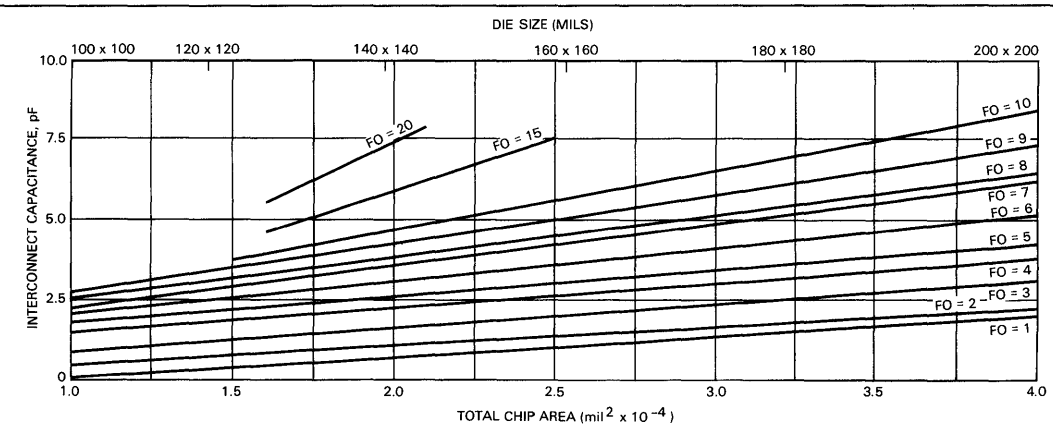
The effect of substrate voltage tolerance over the typical V_{SS} range is normalized to provide a delay factor F_{VSS}.

Fig. D-10. Substrate Voltage Tolerance Curve



The factor F_{temp}, is shown as a function of junction temperature.

Fig. D-11. Variation in Logic Delay Time with Temperature



Mean interconnect capacitance in picofarads as a function of chip area and fan out on the node being considered.

Fig. D-12. Interconnect Capacitance Estimates

Consider the path shown in *Figure D-13* on a 100 X 100 mil chip. The capacitances are tabulated as in *Table D-4*. The P_i factor is the rating for the cell whose output drives the given node.

P_i = 1 for standard power cells
P_i = 2 for low power cells (suffix L)
P_i = ½ for high speed cells (H)
P_i = ¼ for super speed cells (S)

Assuming the same K factor as before and a buffer delay of 50 ns with 20 pF load, the total delay of the path in *Figure D-13* would be:

$$t_{D(path)} = K \Sigma P_i C_i + t_{D(buffer)}$$
$$= (46.7 \text{ ns/pF})(16.35 \text{ pF}) + 50 \text{ ns}$$
$$= 763 \text{ ns}$$

After chip layout, when interconnect lengths are known, speeds, rise and fall times, and other dynamic parameters will be computed accurately with the FAIRSIM simulation program. The above estimates are used in logic design to avoid serious timing problems prior to layout.

GATE APPLICATIONS

Depending on the type of gate selected and the input logic levels, the cell library gates may be used as NOR, NAND, AND or OR functions (see *Figure D-5*).

NAND gates are expanded as in *Figure D-14* and NOR gates as in *Figure D-15*. NAND gates expand to practically any number of inputs since the expander transistors are in parallel with the NAND inputs. NOR gates are limited, in practice, to four inputs by the series resistance.

Expanders can also be used on other cells. The expander should have the same power rating as the cell expanded (the cell with a load resistor) or a higher power rating.

The more complex gates provide many Boolean logic and switching functions, as indicated by *Figures D-16, D-17* and *D-18*. They are also useful as special latches (*Figure D-19*). Substituting complex gates for simple gates, where signal polarities permit, helps minimize chip area (*Figure D-20*).

FULL ADDER

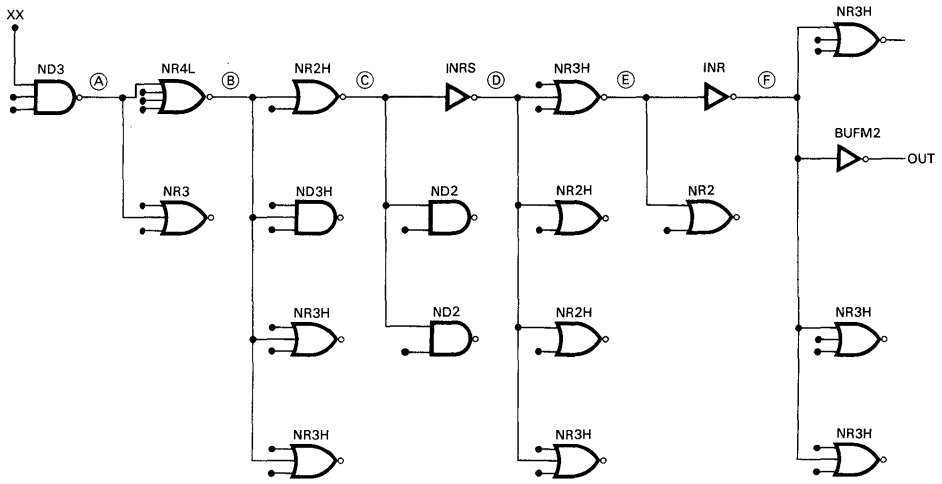
The FA cell is comparable to the 9404 MSI dual adder. Request Applications Bulletin 163 for information on adders of this type.

DECODERS

The DEC1 and DEC2 cells are the same size, but the DEC2 has high power input inverters to increase its speed. Applications are similar to those of the 9301 MSI decade decoder (request Applications Bulletin 160).

Node	P_i	ΣC_{in}	ΣC_{out}	ΣC_{int}	C_i	P_iC_i
A	1	0.49	0.23	0.80	1.52	1.52
B	2	2.10	0.23	1.50	3.83	7.66
C	1/2	0.56	0.26	1.00	1.82	.91
D	1/4	1.96	0.24	1.50	3.74	.94
E	1/2	0.33	0.27	.80	1.40	.70
F	1	2.89	0.23	1.50	4.62	4.62
					P_iC_i	16.35

Table D-4. Capacitance Estimation Table



Propagation delay example showing method of tabulating and adding nodal capacitances.

Fig. D-13. Path Delay Example

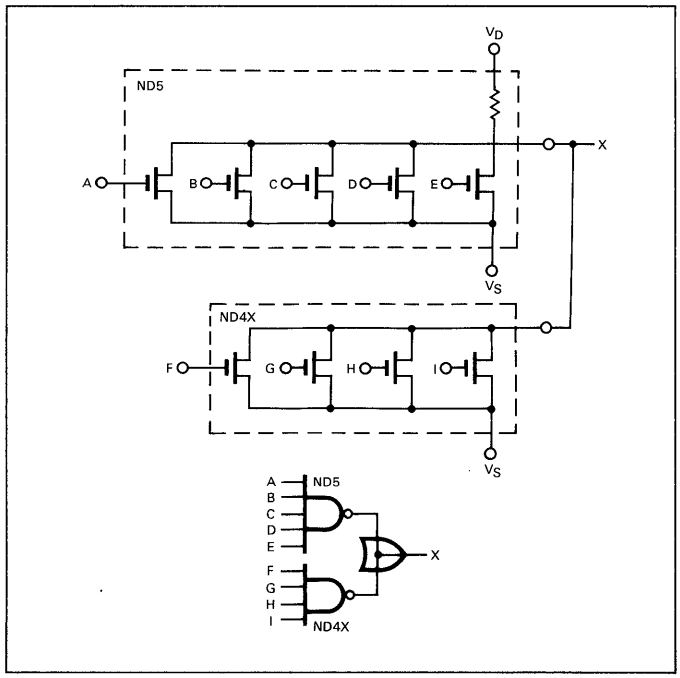


Fig. D-14. NAND Expansion

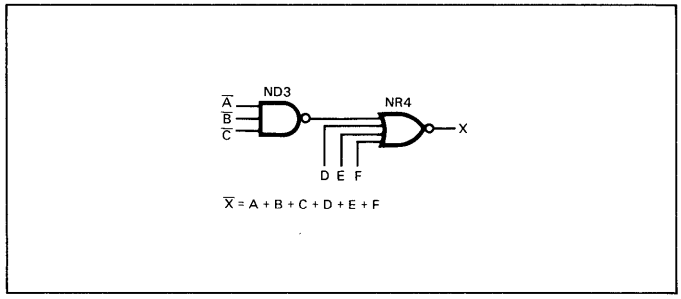


Fig. D-15. NOR Expansion

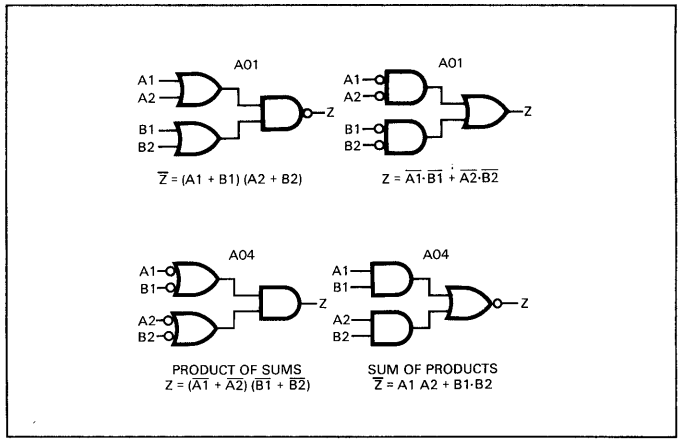


Fig. D-16. Boolean Function of AND-OR Invert Cells

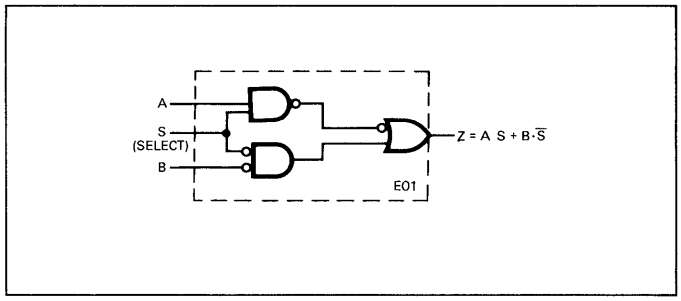


Fig. D-17. EXCLUSIVE-OR Cell Connected as a 2-Input Multiplexer.

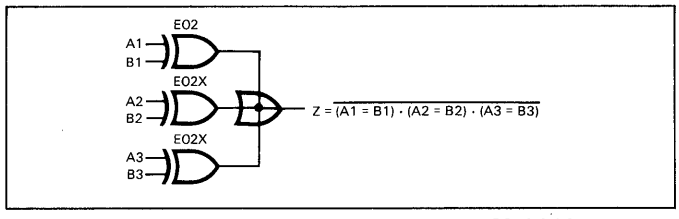


Fig. D-18. Expanded EXCLUSIVE-OR Cells as Multi-bit Comparators

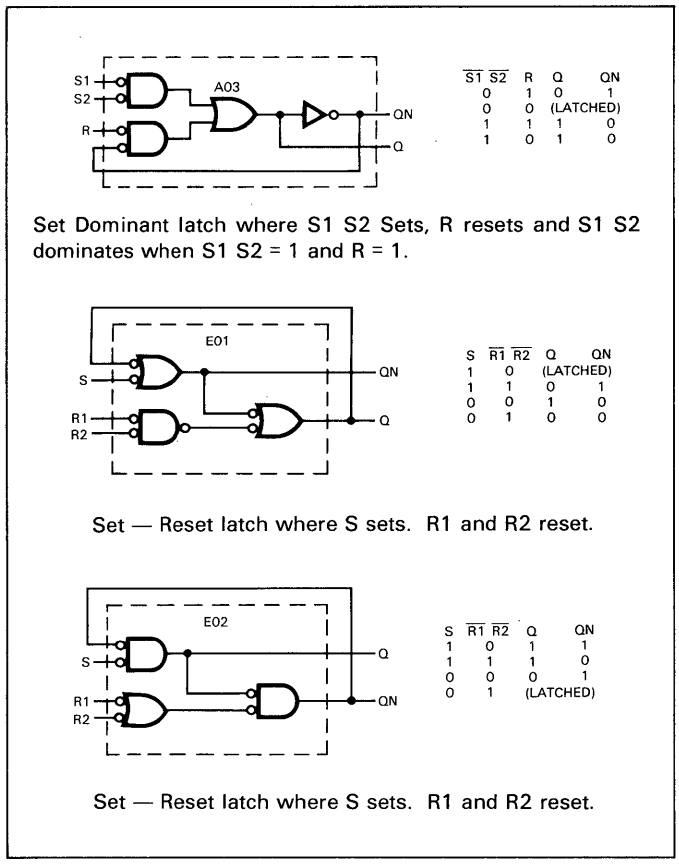


Fig. D-19. Special Latch Implementation Using Complex Gates

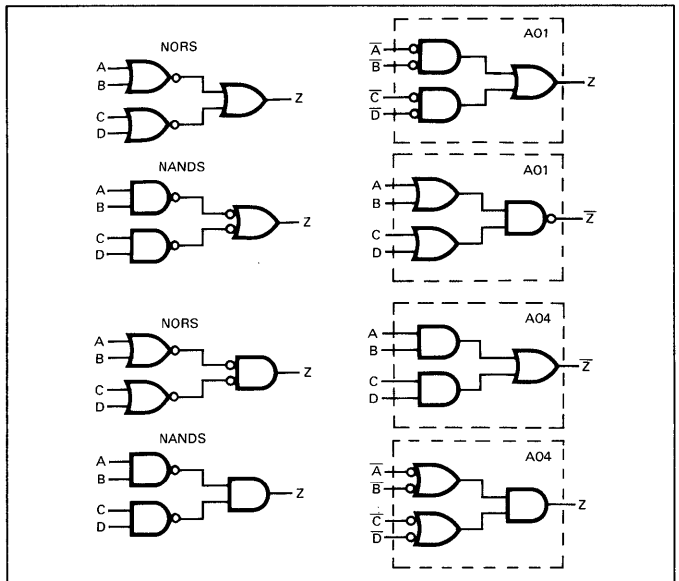


Fig. D-20. Complex Gates Use Less Chip Area

COMPOSABLE LOGIC MATRIX

After logic minimization, the three steps followed in designing a CLM version of a combinatorial logic function are: 1) select combinatorial functions of common inputs, 2) convert the logic functions to a two-level sum of products or complemented products (for the product outputs), 3) determine whether the use of external cells to implement inverse functions would be more efficient.

Karnaugh maps easily generate the product terms if there are less than five input variables. Computers are efficient for 5 to 12 variables. It is generally prohibitive in time and labor to attempt to absolutely minimize more than 12 variables.

Maps were used for the design examples in *Figures D-21* and *D-22*. In the example shown in *Figure D-21*, the area savings in using CLMs against regular gate cells is shown in *Table D-5*. To use the CLM as a ROM, assign the address bits as inputs, words as products and outputs as sums. For example, a 32-word 8-bit ROM (256 bits) requires I = 5, P = 32, and S = 8. A CLM of this size would occupy 110 equivalent grids (see cell description) and have an average propagation delay of 183 ns.

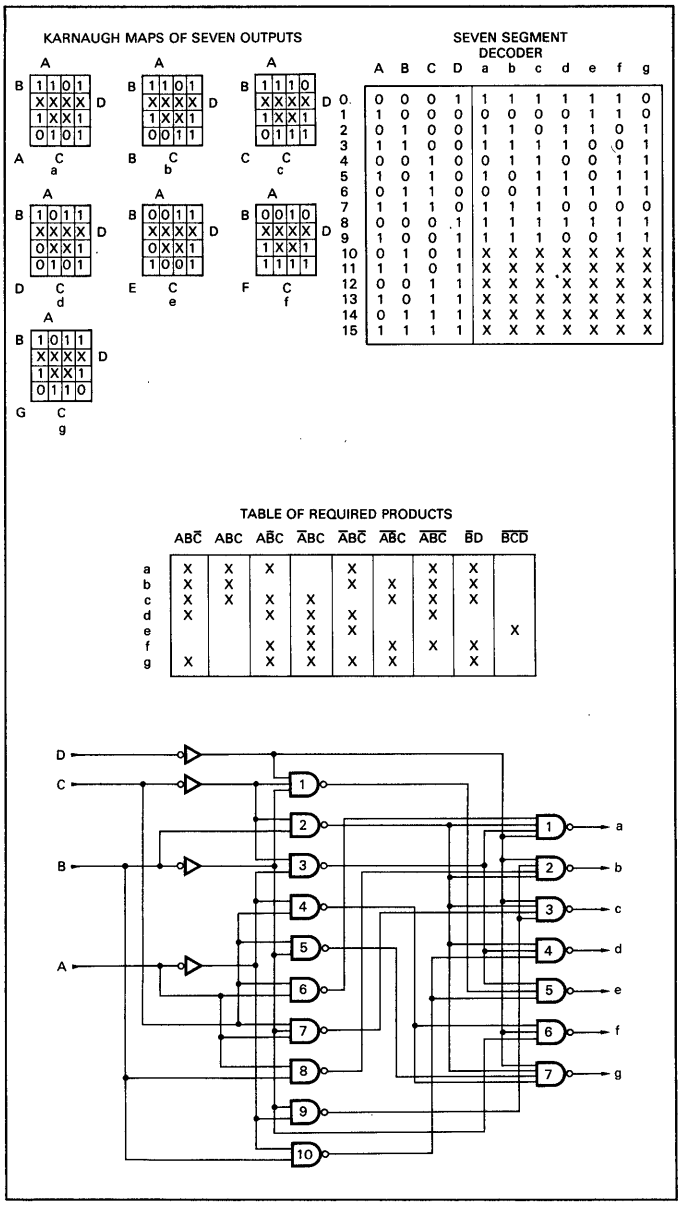


Fig. D-21. CLM Application

Circuit	Std. Logic Grids	CLM Equivelent Grids
Seven Segment Decoder	73	31.2

Table D-5. Equivalent Grid Area of CLM vs. Standard Logic Gates

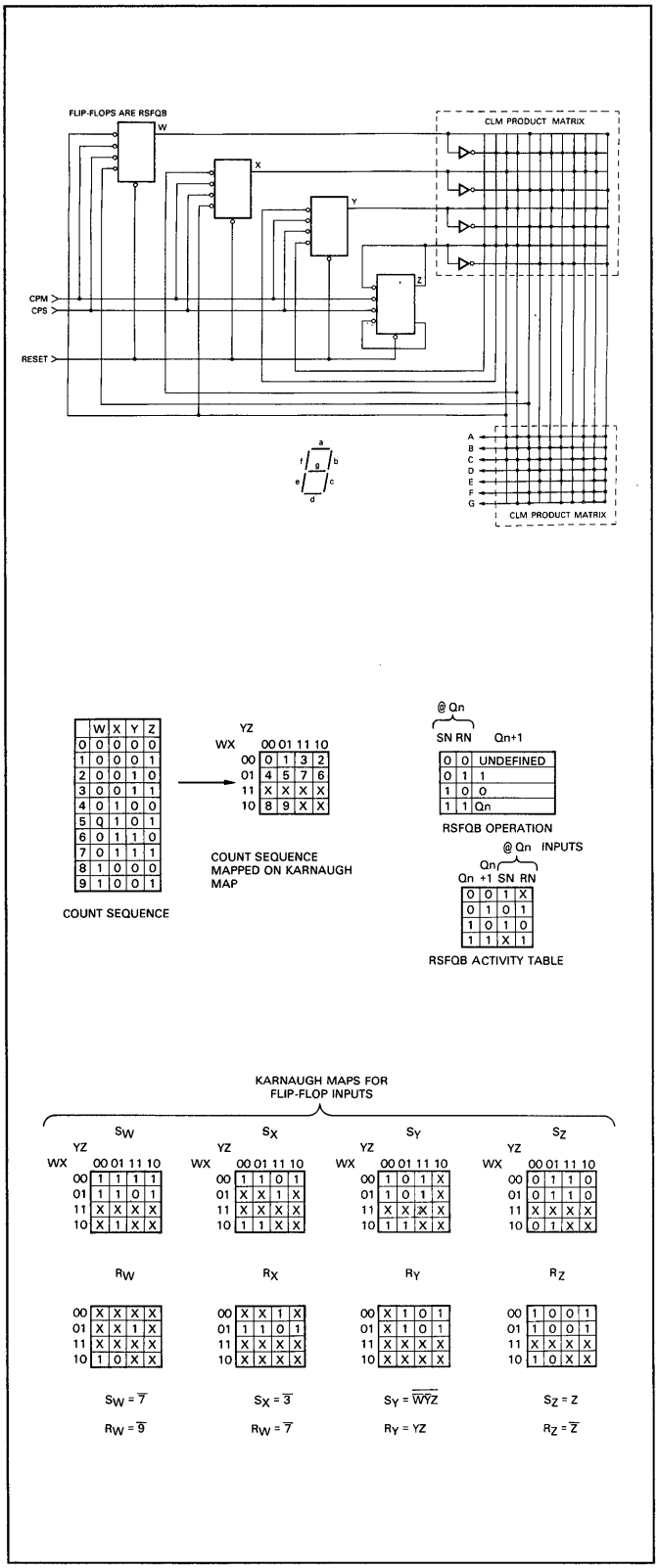


Fig. D-22. CLM Application

LATCHES AND FLIP-FLOPS

Expanders will economically control latch cells (*Figure D-23*). When two interconnected latches are needed, use a master/slave flip-flop to reduce chip area. The master of the RSF1 flip-flop is similar to an RSL latch and the RSF1 slave to the RS2 latch. The RSF2 flip-flop has two RSL stages.

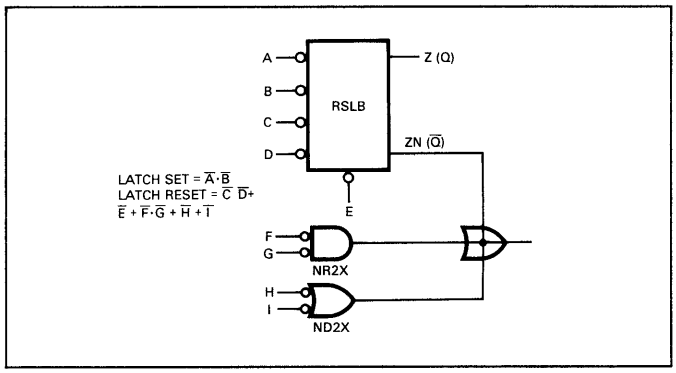


Fig. D-23. Latch Control With Expanders

The RSF cells may be clocked at rates to over 1 MHz in applications such as *Figure D-24* (see also *Figure D-26*). However, quasi-static flip-flops are recommended for long ripple counters since they are smaller. Among the cells provided to support clocked logic are the discriminator, which may be used as a clock oscillator, and the clock generator (CG).

Note that if the RSL latch's set and reset inputs are activated simultaneously, both logic and asynchronous inputs will force their respective outputs HIGH. The RSL types are activated by LOW inputs and the RS2 types by HIGH SN or RN inputs and LOW asynchronous inputs (i.e., they set when direct set is LOW).

Also, an RSF1 flip-flop's output will be arbitrary if SN, RN and CP (common clock) are all false simultaneously. If both RSF2 clocks are false, both master and slave will be sensitive to their inputs and the cell will not function as a master/slave flip-flop.

Q is called Z and $\overline{Q}$ is ZN in the cell diagrams to keep the computer terminology consistent with other cells.

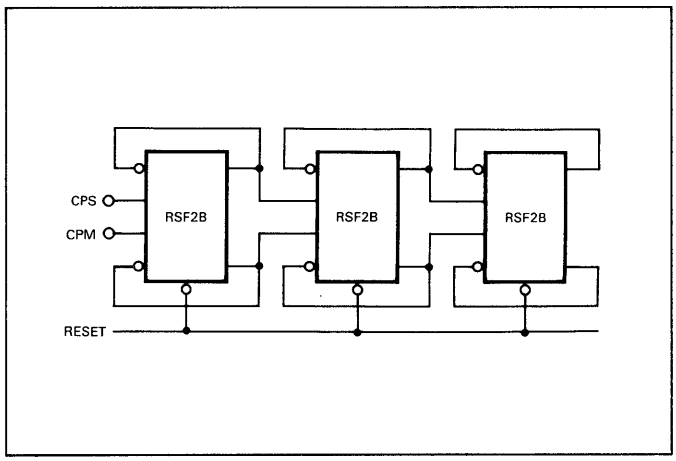
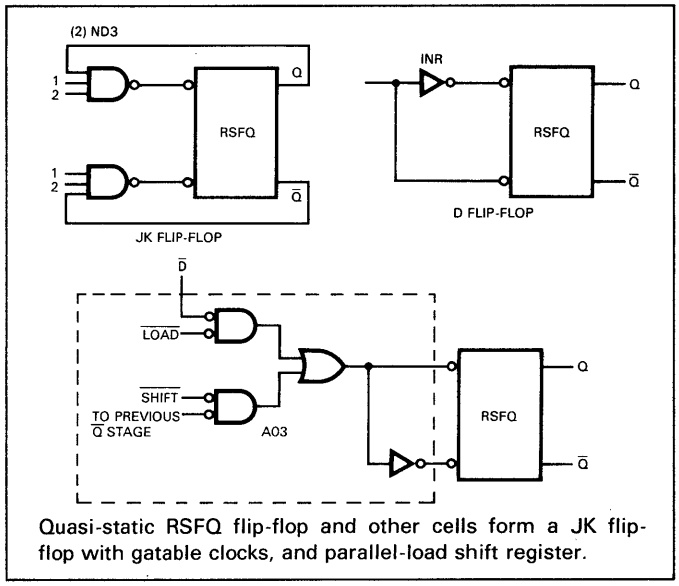


Fig. D-24. HIGH-Level Reset With Inverters

QUASI-STATIC FLIP-FLOPS

The quasi-static flip-flops are popular cells for long static shift registers as well as flip-flop applications (*Figure D-25*) because of their small size.

A unique internal design makes these flip-flops immune to "ones-catching." When CPM is negative, the master follows the slave (CPM is a HIGH level clock, +5 to –5 V). The slave is set after CPM goes positive and CPS goes negative.



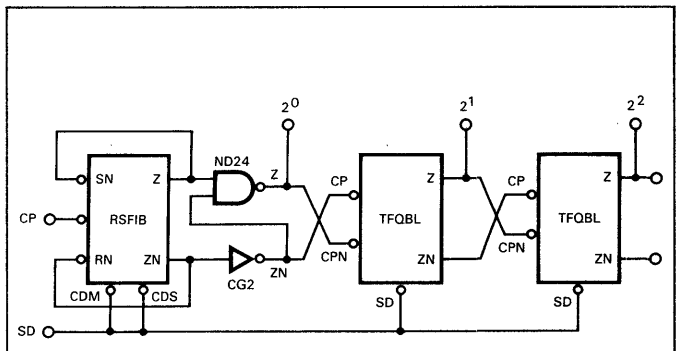
Quasi-static RSFQ flip-flop and other cells form a JK flip-flop with gatable clocks, and parallel-load shift register.

Fig. D-25. RSFQ Applications

Operation is quasi-static since input data is stored as nodal charges until the data is latched into the slave. To retain data, CPS must set the slave within 100 µs after the CPM transition (at 0 to 70°C). Once the slave is set, either or both clocks may be gated off (use the CG4 analog switch to gate the HIGH level clock on the chip).

The slaves of the asynchronous types (B and C) may be cleared directly. When the slave reset goes LOW, ZN will go HIGH, the only guaranteed effect of asynchronous inputs. Output Z will be LOW when CPS is HIGH or when CPS is LOW and the cell is in the static condition. When both CPS and CPM are LOW, data goes directly from input to output.

The D and T flip-flops (DFQ and TFQ cells) are versions of the RSFQ. However, charge leakage will force the DFQ output HIGH if CPM is gated off longer than 100 µs (0 to 70°C). The TFQ is designed for ripple counting and has a HIGH level ZN output so that chains are interconnected within the cell rows (*Figure D-26*). This figure also illustrates on chip clock generation.



Ripple counter with asynchronous reset to all "1"s is clocked by an RSF1 master/slave flip-flop with the aid of NAND and clock generator cells. The RSF1 operates at 1 MHz and the TFQBL to 500 kHz with 0.5-pF loads connected to the counter outputs. Each TFQBL dissipates an average of 0.625 mW.

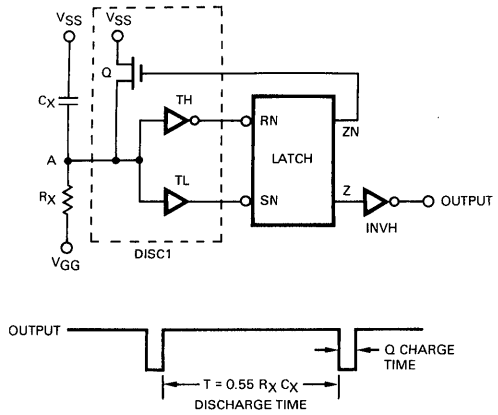
Fig. D-26. Ripple Counter Clocking

DISCRIMINATOR

The DISC1 cell is normally used with a latch as an on chip oscillator or initialization circuit, such as those in *Figures C-27, D-28* and *D-29*. The cell requires an external resistor and capacitor.

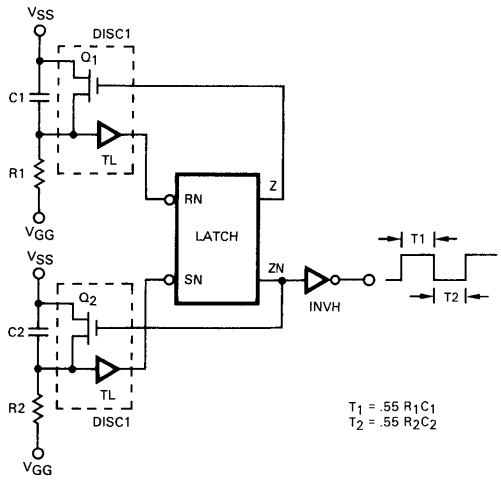
The node between C_X and R_X discharges from the threshold of TH (V_{SS}-V_T) to the threshold of TL (V_{SS}-V_T) in a nominal time of 0.55 C_XR_X. C_X should be at least 15 pF and R_X should be at least 50 kΩ to reduce the voltage caused by leakage of C_X. For accuracy, charge times may be limited to 10% or to 1% of discharge times by making R_X at least 100 kΩ or 1 mΩ respectively.

The maximum frequency is 1 MHz. To maintain good frequency stability at frequencies above 100 kHz, a high power latch is needed.



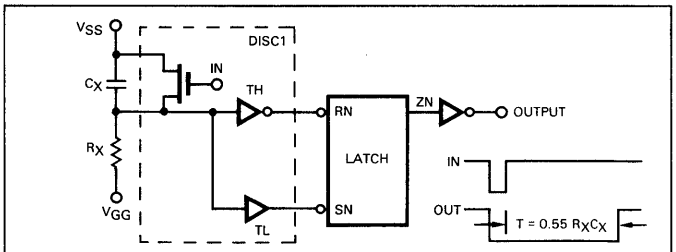
Pulse generated formed with DISC1 and latch. If an RSF1 flip-flop cell, connected as a toggle flip-flop, is used instead of a latch, the circuit becomes a square wave generator. Q is a discharge transistor.

Fig. D-27. DISC1 as Pulse Generator



Two DISC1 cells and a ltach operate as an oscillator with a variable duty cycle.

Fig. D-28. DISC2 as Oscillator



Retriggerable one-shot is controlled with the gate of the DISC1's discharge transistor.

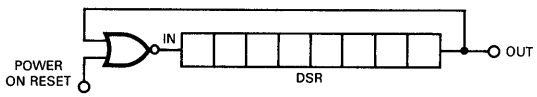
Fig. D-29. DISC1 as One-Shot

DYNAMIC REGISTER CELLS

The dynamic shift register (DSR) series includes many minimum area storage and output cells for "straight-pipe" shift registers such as those in *Figures D-30* and *D-31*. They typically dissipate 0.2 mW/bit and are usually clocked at 10 kHz to 2 MHz.

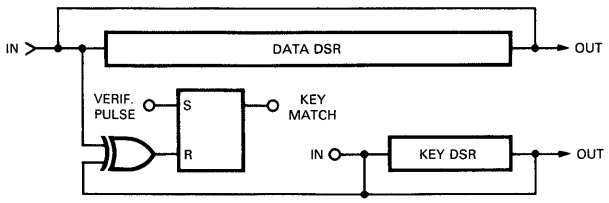
Stages cannot be reset individually, but forcing both clocks LOW will initialize the register.

Many specialized register designs may be implemented with these cells. For instance, to keep track of a recirculating data stream without counters, use two storage bits per data bit and encode the start bit 1-1, the data bits 0-1 and 1-0, and the end bit or an empty register 0-0.



Dynamic shift register connected as a divide-by-16 Johnson counter (clock circuits are not shown).

Fig. D-30. Shift Register Counter



Key search or associative memory accesses all related data words circulating in the long dynamic shift register. The words are stored with a key field and the search made by entering the key word in the short register.

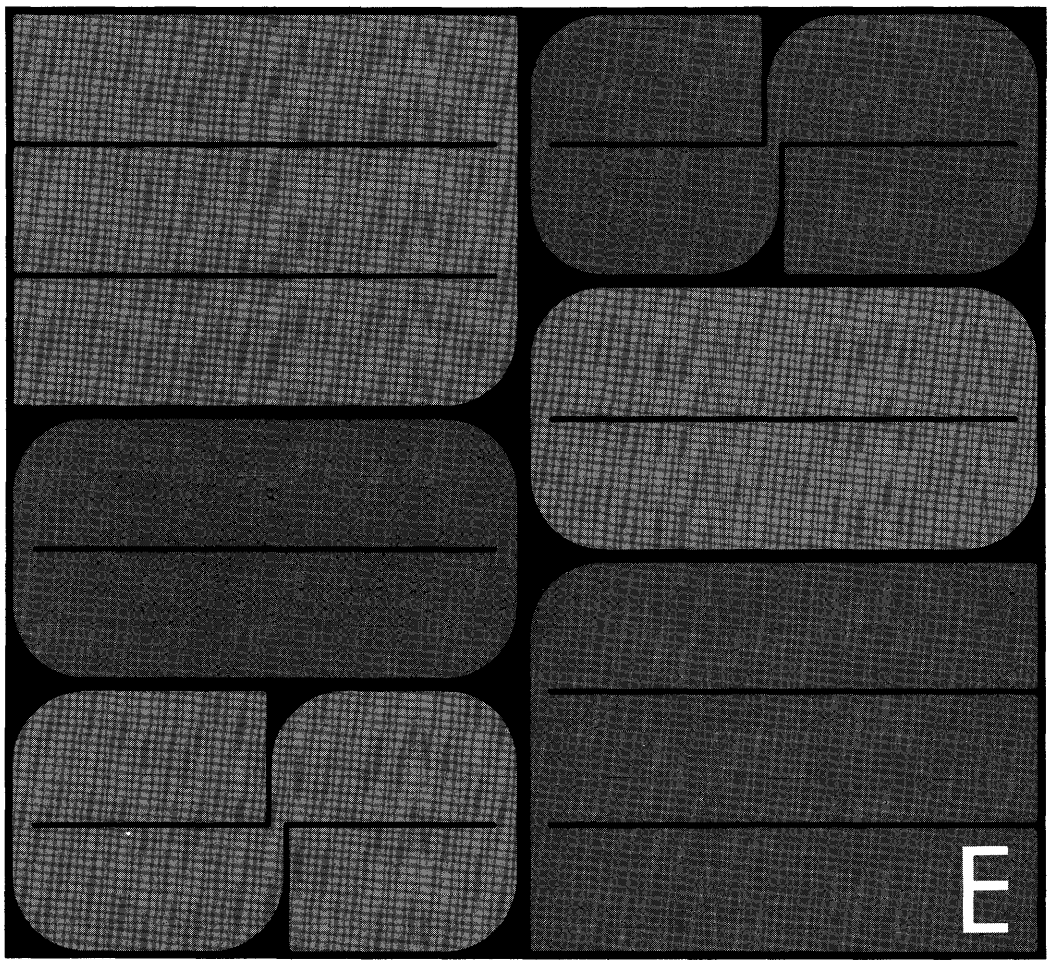
Fig. D-31. Shift Register CAM

Bits in a register need not be functionally related. Large numbers of status bits may be stored and inspected at a low cost with the aid of a comparator and bit address counter, assuming circulation delays are acceptable.

Registers are often used in serial data processing. For instance, a register and adder allow X + 1 to be transferred almost as easily as X alone. Likewise, a "1" may be subtracted from every word during a register circulation. Such vector operations are useful in priority or polling applications where entries made at different times must be counted and sensed periodically.

Precession counter techniques are economical when a system requires long timing intervals of varying lengths. If one bit is precessed with respect to another, an M-bit register can produce N count cycles of M bits duration (N < M-1). Periods are varied by changing the precession distance.

CAD–Computer-Aided Design



APPENDIX E

CAD — COMPUTER-AIDED DESIGN

INTRODUCTION

A large interactive computer-aided design (CAD) software package is employed for MOS development at Fairchild. The CAD system is specialized to a process technology — silicon gate in this case — through the cell "macro" library (Ref-cell set in Appendix D). A macro is a computer description of the cell logic. New technologies may be added to the library by writing new macros.

The cell library for the technology includes the cell patterns and dimensions for the wafer fabrication mask and key electrical parameters. The Fairchild CAD programs can model, simulate, lay out and control the mask making for a complex cell array — under the guidance of a designer familiar with the CAD software.

The two programs most pertinent to Micromosaic logic design are FAIRSIM (simulation) and its support programs and FAIRGEN (test generation and verification). These programs may be made available to a customer depending on contractual divisions of design and verification responsibilities between the customer and Fairchild.

Other programs are employed by Fairchild design specialists before and after simulation and verification. An example of these is MMAP, used to analyze cell operation before the cell description is filed in the computer library. MMAP simulates each cell exhaustively over the range of process parameters so that its dc and transient behavior can be encoded for accurate modeling of the cell with FAIRSIM.

Users of the software can create their own macros for special functions not in the cell set. That is, they simply assemble macros in the set to form the new function (e.g., a counter from several flip-flop macros). This special macro can then be used as often as necessary in the design by repeating the list of cells on the Netlist described below.

Simulation Techniques

Following logic design, the cells and their signal inputs are listed in the Netlist format as shown in *Figure E-1*. Netlist is an input to Fairchild's FAIRSIM simulation program. This program assembles the cell descriptions and makes the connections shown on the Netlist, and thus creates a software model of the logic network. The model is filed in the computer memory. Directions for Netlist preparation are described in a FAIRSIM manual for customers who prefer to prepare their own logic designs and netlists.

```
          MSSGT
          NETSTART
AA        INV     DCE
BA        NR2     AA,DMDN
BB        NR2     DCE,DCDN
CA        NR2     BA,BB
DA        INV     CA
A         RSF1B   DA,CA,MC,CLK
B         RSF1B   AN,A,MC,CLK
EA        ND2     B,AN
FB        NR2X    EA,CB,DN
HA        EO1     BN,AN.BN,AN
F         RSLA    HA,MN,G,M
C         RSF2B   BN,B,MC,KB,KD
RXDN      BUFB2   CN
KB        ND4     KD,G,M,MC
KC        ND3     G,MC,M
KD        ND2     KB,KC
RXTN      BUFB2   KD
AB        INV     FSB
CB        ND3     AB,FSA,FSC
DB        INV     CB
D         RSLB    BC,CB,DB,HA,MC
E         RSLA    HA,JB,M,G
JB        ND2     MN,G
KE        ND4     F,EN,KN,M
KF        ND4     EN,FN,LN,M
KG        ND2     KE,KF
BC        INV     EDCN
BD        ND3     DN,RXR,MC
DC        ND2     BD,EB
EB        ND2     DN,DC
FD        INVX    RXR,EB
FE        INVX    MC,EB
G         RSF2B   M,MN,GC,EB,DC
H         RSF2B   GN,G,GC,EB,DC
I         RSF2B   HN,H,GC,EB,DC
J         RSF2B   IN,I,GC,EB,DC
K         RSF2B   JN,J,GC,EB,DC
L         RSF2B   KN,K,GC,EB,DC
M         RSF2B   LN,L,GC,EB,DC
BE        INV     KG
N         RSF1B   KG,BE,MC,CLK
GB        NR2     CB,BC
GC        NR2     GB,NN
TP1       INV     GN
TP2       INV     HN
DCE       PAD     IN
DMDN      PAD     IN
DCDN      PAD     IN
FSB       PAD     IN
FSA       PAD     IN
FSC       PAD     IN
EDCN      PAD     IN
RXR       PAD     IN
MC        PAD     IN
CLK       PAD     IN
RXDN      PAD     OUT
RXTN      PAD     OUT
TP1       PAD     OUT
TP2       PAD     OUT
VS        PAD
VR        PAD
VD        PAD
          NETEND
          END
```

Cell names at the left are unique names assigned by the designer and those in the center are the names in the cell set descriptions. Inputs to each cell are listed at the right, using the unique names for the cells or pads that transmit the inputs. Delays calculated by the designer may be listed with the inputs (if not, unity delays are assumed).

Figure E-1. Example of encoded Netlist

Cell Cross Reference List

After Netlist preparation, a cross reference list is usually requested as a computer printout. The list identifies each cell, signal interconnections and fan outs. Signals not defined by Netlist are assumed to be outputs if they do not connect to other elements. Other undefined signals are assumed to be inputs. This list enables the designer to check the simulated model against his logic diagram and Netlist to detect any oversights or Netlist encoding errors.

Simulation

Simulation generally starts with a thorough exercising of the model. A simulation control language allows the user to specify the logic testing environment and to trouble-shoot model operation.

Operating characteristics such as rise and fall times of various elements can be simulated. Assuming that encoding errors have been corrected with the cross reference list, the FAIRSIM program may be used at this time to verify logic operation and detect any potential speed problems.

A pre-layout speed analysis program, FAST, gives first-order approximations of the FAIRSIM model's circuit delays. It takes into account normalized interconnect capacitances, cell input and output capacitances, and such variables as temperature, power supply tolerances and MOS process variations within the process tolerances. FAST also predicts network power dissipation and chip sizes. These data may be used by the designer to verify or change his logic design. The changes are entered with a new FAIRSIM Netlist.

After LAYOUT, the SPEED analysis program performs a highly accurate performance simulation. The nominal interconnect lengths are replaced with actual ones providing exact capacitance values.

TEST GENERATION AND VERIFICATION

Functional test generation with FAIRGEN is based on the FAIRSIM model and is usually done at the same time as LAYOUT. Basically, the model is exercised and tested for possible defects. Then FAIRGEN devises tests to detect such defects in the actual circuits. Tests are verified for four classes of defects: gate inputs stuck at 1 or 0, gate outputs stuck at 1 or 0, open interconnections and shorted interconnections. The computer also reports on its ability to detect each defect.

The resulting file of test patterns is then used to program functional tests to be made with the Sentry computer-controlled test systems. The patterns are modified to eliminate any redundant or unnecessary tests, to compensate for undetectable gate defects by testing an associated function with special test points or to incorporate special test sequences requested by the customer.

The FAIRSIM model itself can be tested and the test simulation output given the customer for checking. Among the printouts available are array input and output logic patterns, internal logic patterns analogous to multi-trace oscilloscope displays of logic operation, and a list of output results that a good array should produce when exercised with a given input sequence. Thus, operation of the array in the system can be predicted as exhaustively as required.

LAYOUT AND MASK GENERATION

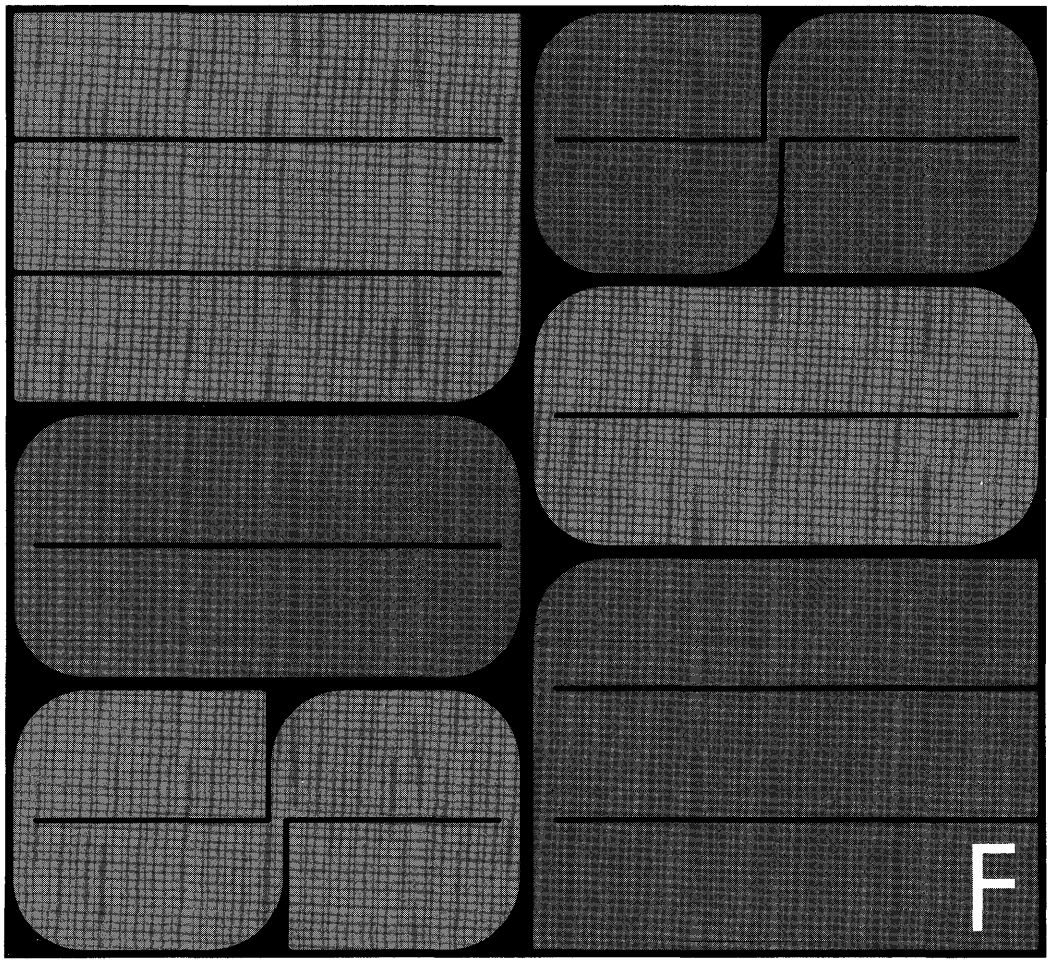
Chip layout and mask generation are performed by Fairchild after the design is approved. Cells are positioned on the chip by a cell placement program. Interconnections defined on the Netlist are routed by an automatic wiring program. These steps are performed in succession so that the layout designer can first improve cell placement (for example, to equalize cell row lengths or distribute buffers to avoid undesirable thermal gradients on the chip). Maps are printed out by a high speed printer with a special character set.

The layout designer may have to generate several different layouts to optimize interconnection density and keep path lengths reasonable. He may use control statements to relocate and rotate cells or vary interconnection alley widths, for example. Trials are kept in the computer file so that several variations on a basic layout may be tried.

All data generated by the computer become part of the design documentation. In addition, the computer-generated layout may be modified by hand to further optimize the wiring pattern or minimize chip size.

Additional information on FAIRSIM and FAIRGEN is available from Fairchild in the form of user's manuals.

Reliability, Quality Assurance And Testing



APPENDIX F

RELIABILITY, QUALITY ASSURANCE AND TESTING

INTRODUCTION

Programs to ensure product quality and reliability are maintained on three levels at Fairchild Semiconductor.

Quality Assurance

Internal standards for product quality and reliability are based on MIL-STD-883. These criteria, set by Fairchild documents FICF-ST-2012 and 2013, apply when no special reliability processing is ordered. All devices receive process testing per *Table F-3* and 100% dc electrical testing, in addition to the sample testing delineated in *Table F-1*. Qualification sample testing per *Table F-2* is performed on all product periodically to further assure product reliability. Reliability and Quality Assurance (R and QA) is responsible for enforcing compliance with these standards and any additional customer specification requirements.

High Reliability

This includes the Unique 38510 high reliability and JAN processing program. The Unique 38510 is an updated version of Unique 883. The present program incorporates Notice 2 of MIL-STD-883, MIL-M-38510, and even goes beyond MIL-M-38510 in detail. The customer specifies this processing. In addition, a number of products are pre-processed and stocked. The stocking program provides high reliability products at considerable cost and time savings particularly when a large volume of devices is not required by the customer.

Quality Control

Provides in-process monitoring of all products. R and QA maintains production quality control gates during and following wafer fabrication, assembly, production test and at plant clearance. R and QA also controls incoming materials.

RELIABILITY AND QUALITY ASSURANCE

The R and QA facilities include the following equipment to generate reliability data on a continuing, or as required, basis by the customer:

1. High temperature (to 150°C) reverse bias and power life testing, 10,000 sockets.
2. High temperature storage life test, four chambers.
3. High temperature (200°C to 300°C) reverse bias and/or operating life tests, two chambers with total capacity of 2,000 sockets.
4. High temperature reverse bias and/or power life test with humidity, four chambers with total capacity of 4,000 sockets.

The R and QA facilities also include a 4-station, computer-controlled automatic test system. The test results are automatically recorded on tape. This test data is then reduced the same day at the Fairchild computer center. Examples of the type of data available through this system are: printouts of individual device performance, comparisons of delta parameters before and after environmental stressing, summaries of lot performance, and printout of data in the format required for customer lot acceptance testing data books.

Failure analysis autopsies are performed in the R and QA laboratories on devices which fail initial or accelerated life tests. Among equipment available are a scanning electron microscope, electron transmission and electron microprobe, and microsection and metallographic equipment. Lot traceability is also maintained by R and QA.

During development of new product designs, packages and processes, reliability engineers support the design groups to ensure that reliability requirements can be met by the

products after development. Additional R and QA monitoring methods are also developed at this time.

HIGH RELIABILITY PROCESSING

MIL-M-38510, the general specification for microcircuits, has not yet been fully implemented with detail specifications for all devices, qualifying agencies, and other functions. Since these may not be fully available for some years, the Fairchild Unique 38510 program was established as a means of permitting advanced products to be designed into military equipment.

The program provides documents allowing devices not yet specified under MIL-M-38510 to be processed, controlled and qualified in the same manner as military standard parts. It will also allow Fairchild to fill requirements immediately when MIL-M-38510 detail specs (slash sheets) are released for such products. Major program features are:

1. Complete general specification covering all aspects of the program in the same format as MIL-M-38510.
2. Complete sets of detail documents in military format available for all products.
3. Fully documented design information on all products available.
4. Process screening to MIL-STD-883 without exception
   a) Preseal visual to Level A or B
   b) Bond pull test
   c) Bake, 24 hours at 150°C
   d) Temperature cycle, 10 cycles at -65°C to +150°C
   e) Centrifuge, 30 kg
   f) Fine leak, 5×10^{-8} cc/s
   g) Gross leak, fluorochemical
   h) Burn-in, per MIL-STD-883
   i) Electrical testing per detail specification
5. Quality conformance per MIL-M-38510 (except life test performed in Group C for all classes)
6. Lot formation per MIL-M-38510. All generic types produced within a six week period may be included in the same lot.
7. Life testing performed every three months.
8. Four "classes" of screening available with options to cover almost any customer requirement. This will reduce or eliminate the requirement to generate internal specifications.

PRODUCTION TESTING

The need for minimum reliability processing of all MOS products, whether commercial or military, is recognized. Consequently, the minimums in *Table F-3* have been established as an internal standard. More exacting tests may be specified by the customer.

As noted in the main text, Fairchild employs high speed Sentry 400 and Super Sentry 600 test systems for functional and electrical testing. The maximum array size that can be tested with these systems is one with 240 pins. For products involving long test sequences, the Super Sentry 600 is used. It can repeat sequences in the range of one to two million tests at low and high frequencies.

Test sequences may be generated from the MOS circuit design with the FAIRGEN program (see Appendix E) or specified by the customer. These are normally interleaved at Fairchild with the specified dc and parameter tests to make the test computer control program more efficient. Test data rates up to 5 MHz and clock rates of at least 20 MHz are presently available (the Super Sentry 600 can be modified for data rates above 5 MHz should that be necessary).

The software required for converting specifications to the test computer format, and for analyzing device responses to test stimuli, is fully developed. In addition, the computer center is available for more extensive analysis of test data, such as trend data for process control. The Sentry systems are used for prototype device, production wafer probe and production final testing of all MOS/LSI products.

TABLE F-1. MINIMUM QUALITY CRITERIA (PER FICF-ST-2013)

Test Subgroup	LTPD	Accept Number
dc functional & dc parametric at 25°C	5%	3
dc parametric at low temperature	15%	2
dc parametric at high temperature	15%	2
ac parametric at data sheet temperatures	15%	2
Visual/Mechanical	7%	2
	AQL	Level
Fine leak per MIL-STD-883, Method 1014, Condition A or B (leak rate per FIFC-2012)	1.5%	11
Gross leak per MIL-STD-883, Method 1014, Condition C1 (leak rate $< 10^{-3}$ cc/s)	0.4%	11

TABLE F-2. MINIMUM RELIABILITY CRITERIA (PER FICF-ST-2013)

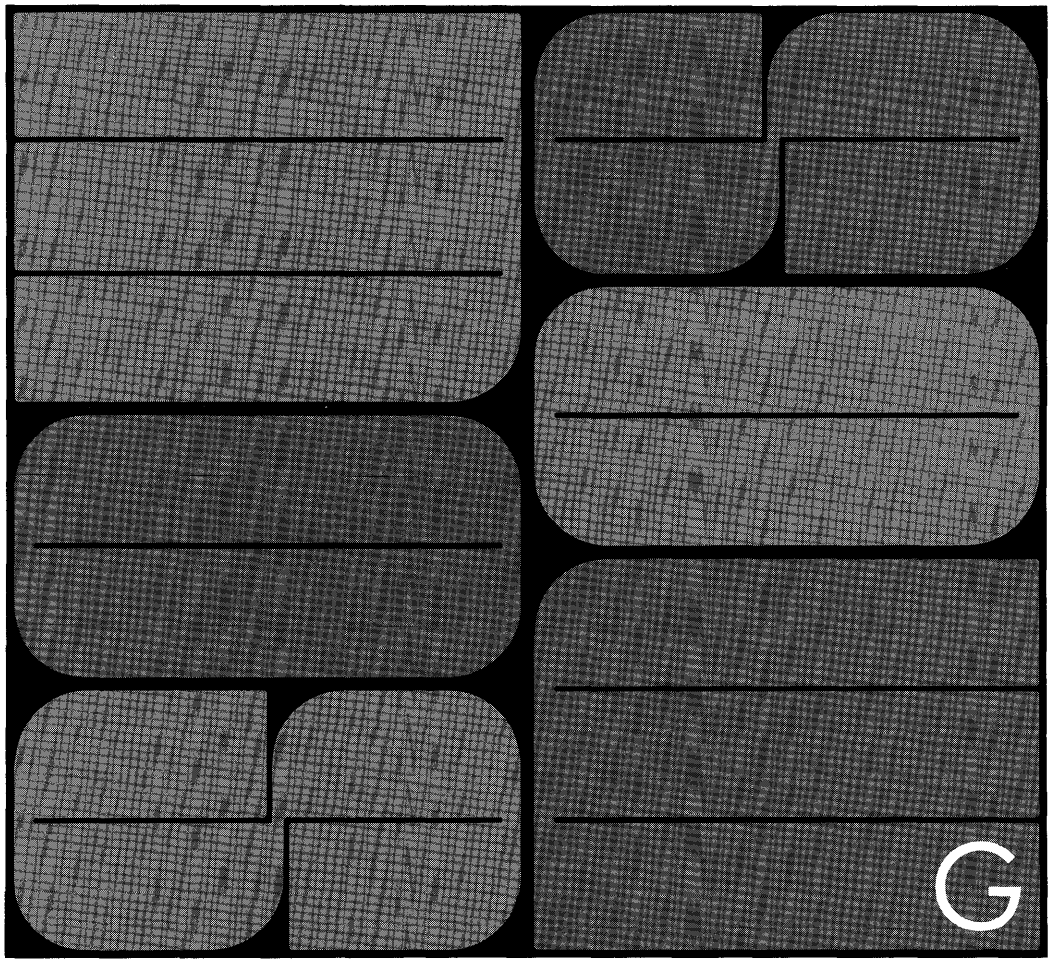
Test Subgroup (Tests per MIL-STD-883; see Note 1)	Method	Conditions	LTPD	Max. Acc. #
B1. Visual/Mechanical	2008	Test condition B (note 2)	15%	2
Marking permanence	2008	Test condition A		
B2. Solderability	2003	Omit ageing	15%	2
Lead integrity	2004	As applicable		
Hermetic seal	1014			
a) Fine		a) Condition A or B (leak rate per FICF-2012)		
b) Gross		b) Condition C1 (leak rate 10^{-3} cc/s)		
B3. Thermal shock	1011	Condition A — 15 cycles	15%	2
Temperature cycle	1010	Condition C — 10 cycles		
Moisture resistance	1004	Condition 1004-1 (note 3)		
Electrical parameters (25°C)		Go/No-Go subgroup A1		
B4. Mechanical shock	2002	Condition B — 1500 g for 0.5 ms	15%	2
Vibration fatigue	2005	Condition A (note 2)		
Vibration, variable frequency	2007	Condition A		
Constant acceleration	2001	Condition D		
Electrical parameters (25°C)		Per subgroup A1		
B5. Salt atmosphere	1009	Condition A (note 4)	15%	2
B6. High temp. storage life	1008	150°C storage 1,000 hrs	10%	2
Electrical parameters (25°C)		Per subgroup A1		
B7. Operational life test and/or reverse bias life test		1,000 hrs (test conditions depend on individual device	10%	2
Electrical parameters		Per subgroup A1		

NOTES:
1. Portions of Paragraph 2.0 may not be applicable due to package limitations (in which case, minimum reliability requirements shall be negotiated)
2. Omit radiographic inspection and delidding
3. Omit applied voltage, final measurement at humidity and initial conditioning
4. Omit initial conditioning

TABLE F-3. MINIMUM 100% PROCESSING (REFERENCE MIL-STD-883)

Processing Step	Method	Condition	Sample
1. Preseal optical	2010.1	FICF-ST-2011	100%
2. Bake	1008	C — 24 hrs at 150°C	100%
3. Temp Cycle	1010	C — 5 cycles, -65°C to +150°C	100%
4. Centrifuge (Y_1 Only)	2001	(performed upon request)	100%
5. Fine leak	1014	A or B — 1×10^{-6} cc/s	1.5 AQL
6. Gross leak	1014	As required — 10^{-3} cc/s	0.4% AQL

Silicon Gate Process



APPENDIX G

SILICON GATE PROCESS

INTRODUCTION

Most new standard MOS products and custom Micromosaic arrays are manufactured using the silicon gate process. In general, the Micromosaic 3402 silicon gate cell set provides superior speed, density (lower cost per function) and bipolar compatibility than the Micromosaic 3401 metal gate cell set. However, the 3401 set remains available because of its advantages in certain applications. Micromosaic 3401 designs have high noise immunity (at least 1 V) and are compatible with older MOS products when manufactured with the high threshold process.

SILICON GATE PROCESS STEPS

Since the silicon gate process is largely responsible for the superior performance of Micromosaic 3402 arrays, let's review the process steps first. Referring to *Figures G-1* and *G-2*, the main steps are:

1. An initial layer of field oxide is thermally grown on the silicon wafer, masked with photoresist and etched to expose the areas of the wafer where transistors and P+ diffused cross-under conductors will be (*Figure G-2A*).
2. A thin oxide layer is then grown on these exposed areas for subsequent use as transistor gate insulation and a layer of polycrystalline silicon is deposited for use as gate electrodes and first layer interconnections (*Figure G-2B*).
3. The polysilicon layer is masked and etched to define the gate electrodes and polysilicon wiring runs. Typically, the polysilicon runs extend from the cells as signal distributing lines. This masking step exposes the source, drain and P+ cross-under areas (*Figure G-2C*).
4. P+ dopants are predeposited on the polysilicon and exposed substrate, and the source, drain and P+ cross-unders are diffused (*Figure G-2D*).
5. Vapor deposited oxide (vapox) containing a getter (for improved stability) is thickly deposited, masked and photoetched to provide contact holes to the diffusions and polysilicon runs. One or two contact masking steps are used, depending on the degree of dimensional control required (*Figure G-2E*).
6. A metal interconnect layer, usually aluminum, is deposited, masked and etched to provide the remainder of the array interconnections. More vapox is deposited as a scratch protection layer (*Figure G-2F*).
7. The top vapox is masked and etched to expose the bonding pads.

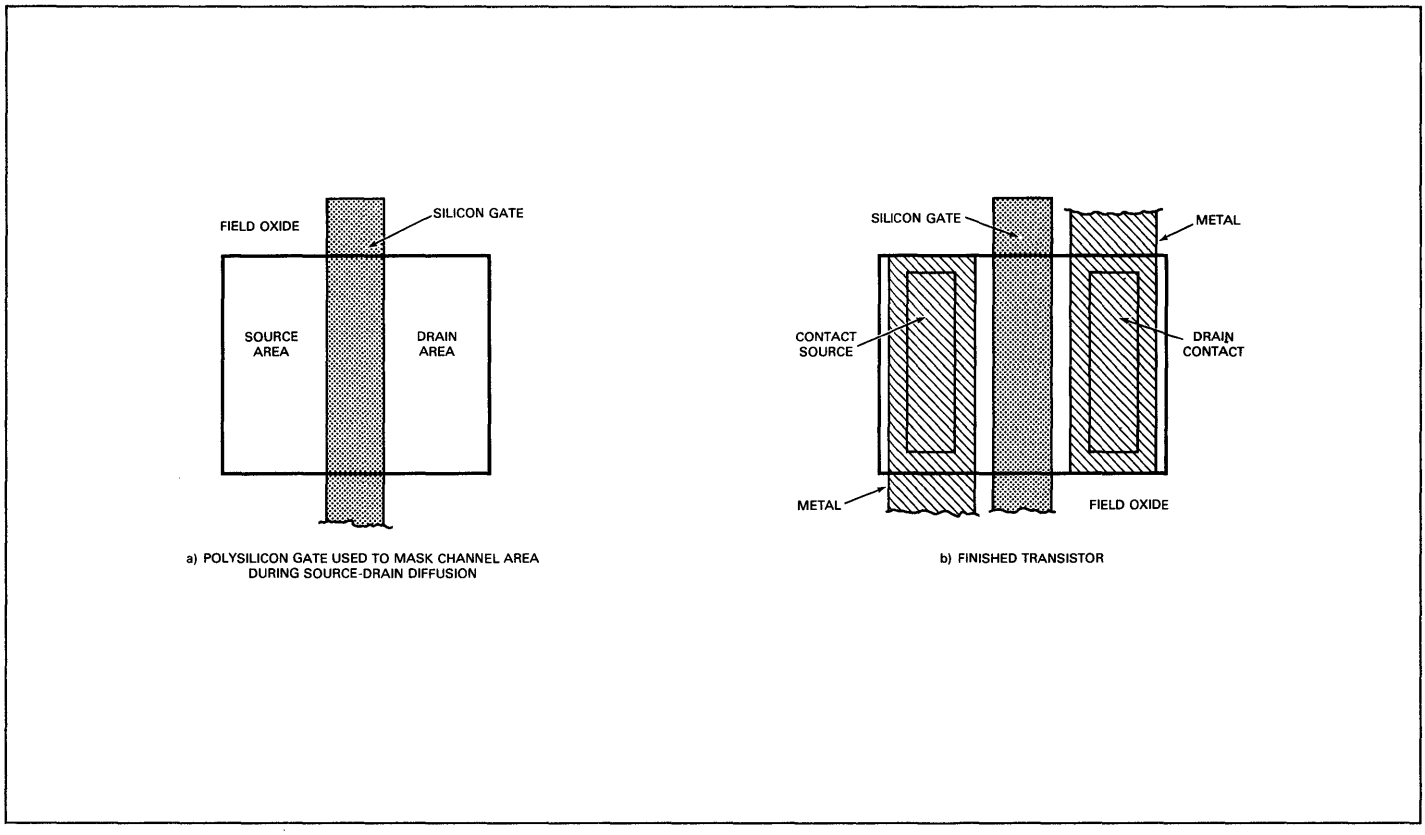


Fig. G-1. Top Views of a Silicon Gate MOS Transistor before and after Diffusion and Metallization

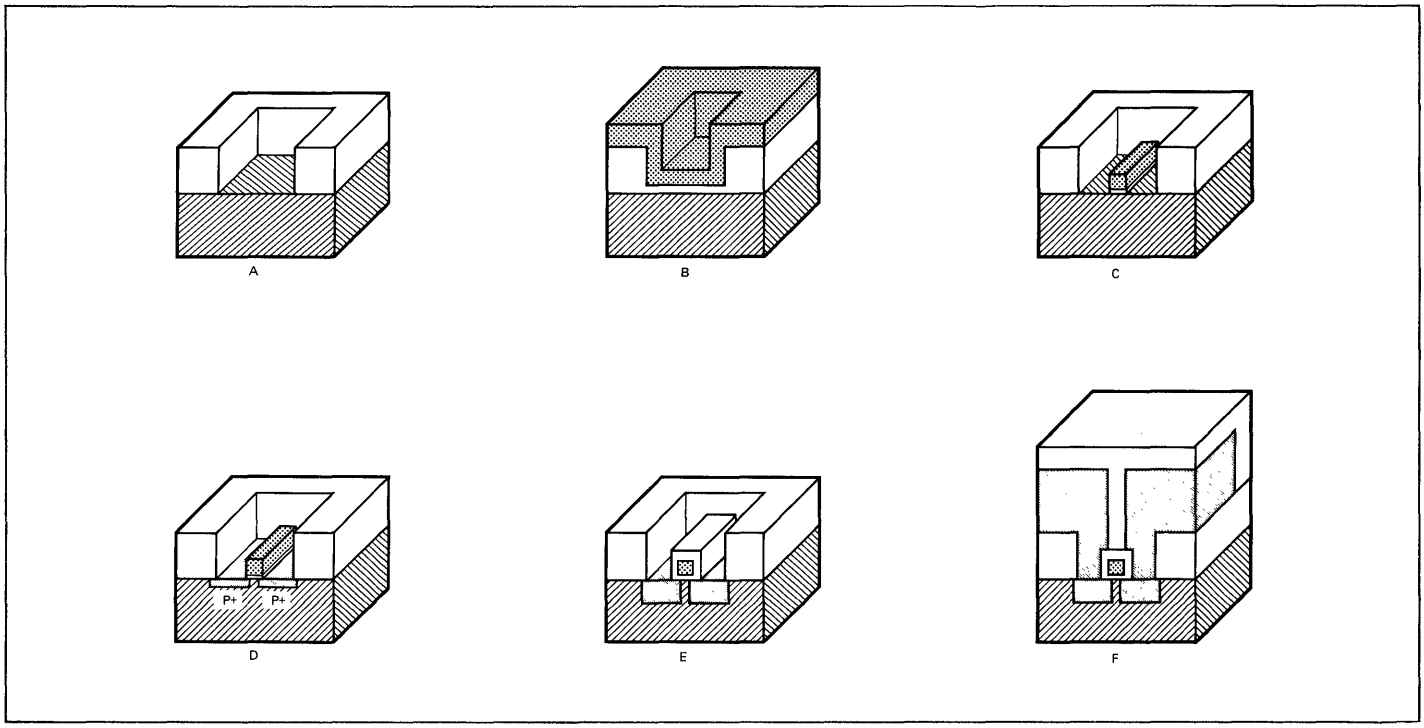


Fig. G-2. Silicon Gate Process Steps

Silicon Gate Process Advantages

The principal advantages of the silicon gate process over conventional metal gate processes are:

1. The gate oxide is grown under conditions which are not influenced by other processing requirements, such as diffusion times, etc.
2. The oxide is immediately covered by the polysilicon layer and is never thereafter exposed to additional processing steps (photoresist and etch).
3. The channel area is defined by the gate, resulting in a self-aligned structure.
4. There may be one less masking step in the silicon gate process if a single contact mask step is used.
5. High temperature processing can be accomplished after the device formation is completed, thus permitting nitride passivation.

TRANSISTOR CHARACTERISTICS

With a silicon crystal substrate having a (111) crystal orientation, the threshold voltage of silicon gate transistors is low. Typically, V_{TO} is 1.5 to 2.0 V. Channel mobility of silicon gate is also better than either low-threshold or high-threshold metal gate because of the low field strength of the silicon gate structure.

Since the silicon gate is self-aligning with the channel and masks the source and drain edges, there is relatively little overlap of these regions thus producing lower Miller capacitances for silicon gate devices.

Also, the channels may be made short enough for transistors only 1.6 mils in cross section with standard dimensional tolerances, versus a minimum of 2.8 mils for metal gate. Channel length control is improved by the shallower silicon gate diffusions, as well. Channels need be only about 0.1 mil long compared with 0.15 mil for metal gate, improving gain at low voltages.

The combined effect of these characteristics is a great improvement in overall performance.

INTERCONNECTION STRUCTURES

Interconnection characteristics are critical to MOS/LSI cost performance ratios. The silicon gate process provides three interconnect layers: polysilicon, metallization, and P+ diffusions. The latter is used sparingly in silicon gate designs because of undersirable electrical characteristics. Occasionally, it is used to avoid the difficult second metal layer just to solve the small number of interconnection problems that may be posed by a complex array.

Silicon gate metal lines may pass freely over the active elements inasmuch as the lines are on top of relatively thick insulation. Thus, the layout designer has great freedom in organizing wiring patterns with the metal and polysilicon layers.

A connection between the polysilicon layer and a P+ crossunder requires large butting contacts. Almost all level-to-level connections are made, however, from the metal to polysilicon or from metal to P+, requiring a smaller contact opening.

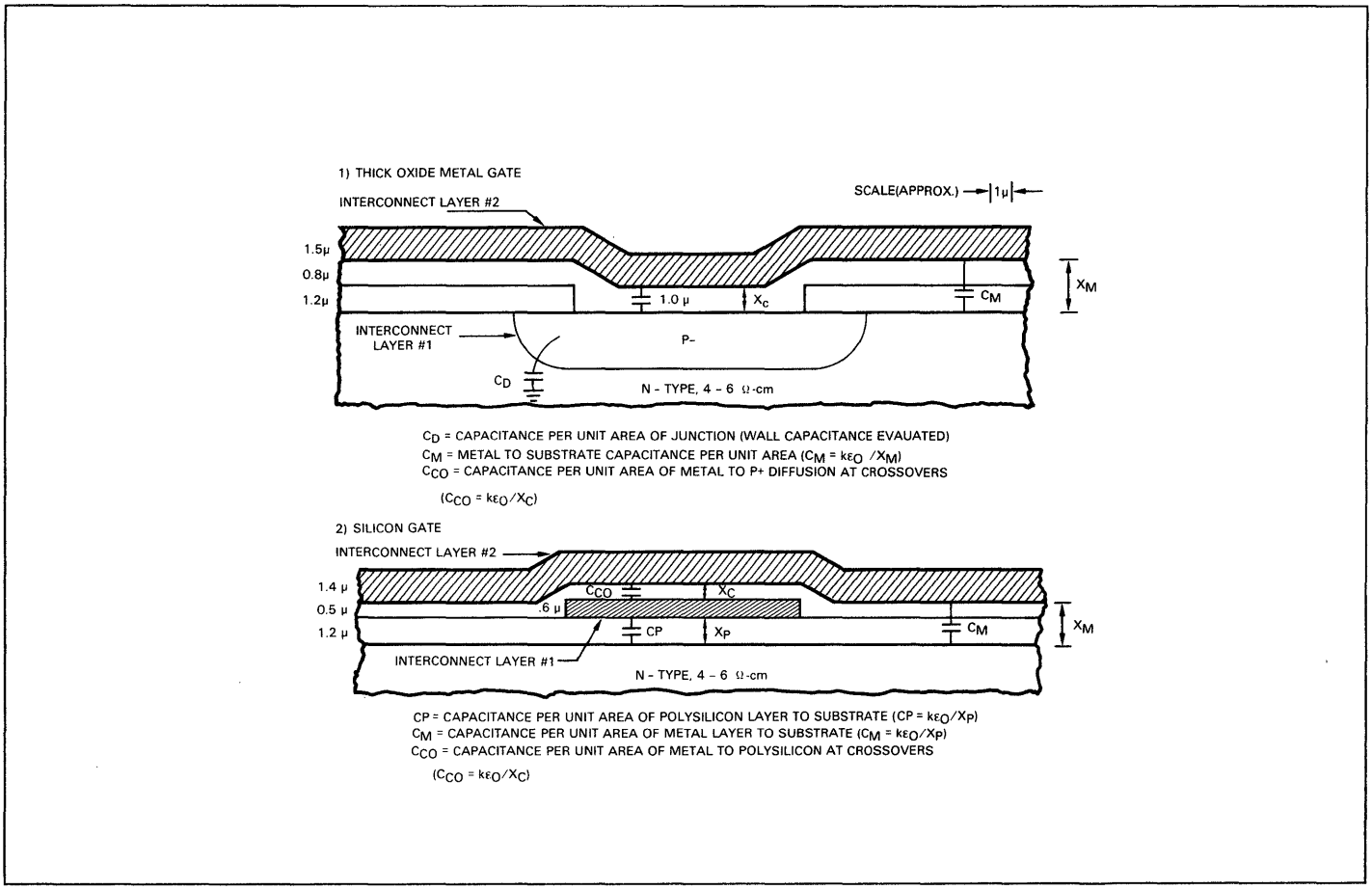


Fig. G-3. Thick Oxide Metal Gate (Top) and Silicon Gate Interconnection Segments and Capacitance Components

INTERCONNECTION CHARACTERISTICS

The silicon gate polysilicon layer is a much better conductor than P+ diffusions. Polysilicon is also a better gate material when doped P+. The aluminum silicon work function of the metal gate structure keeps the transistor threshold high thus lowering its overdrive at 5 V.

Polysilicon interconnect capacitance (see *Figure G-3*) is typically 0.11 pF per 10 mil line segment and line impedance is typically 20 to 80 Ω /sq. (series impedance). The comparable metal gate P+ capacitance is 0.30 pF per segment and series impedance is 100 to 300 Ω /sq.

Moreover, P+ line capacitances are voltage dependent and have nonlinear characteristics that adversely affect circuit performance. The capacitances are smallest when reverse biased, as when the logic is holding at the "1" level. Performance is further affected by the longer metal runs usually required to overcome the larger cell size, to avoid excessive use of P+ diffusions, and to go around active elements.

Silicon gate designs can use long polysilicon runs for signal distribution among cells. If the same is done with long P+ runs in metal gate, the long RC time constants severly degrade pulse characteristics.

The capacitances of silicon gate metal polysilicon and metal P+ crossover intersections are typically less than 0.01 pF. Metal gate metal P+ crossovers have still lower capacitances, about 0.005 pF. However, the large line capacitances still dominate interconnection capacitances.

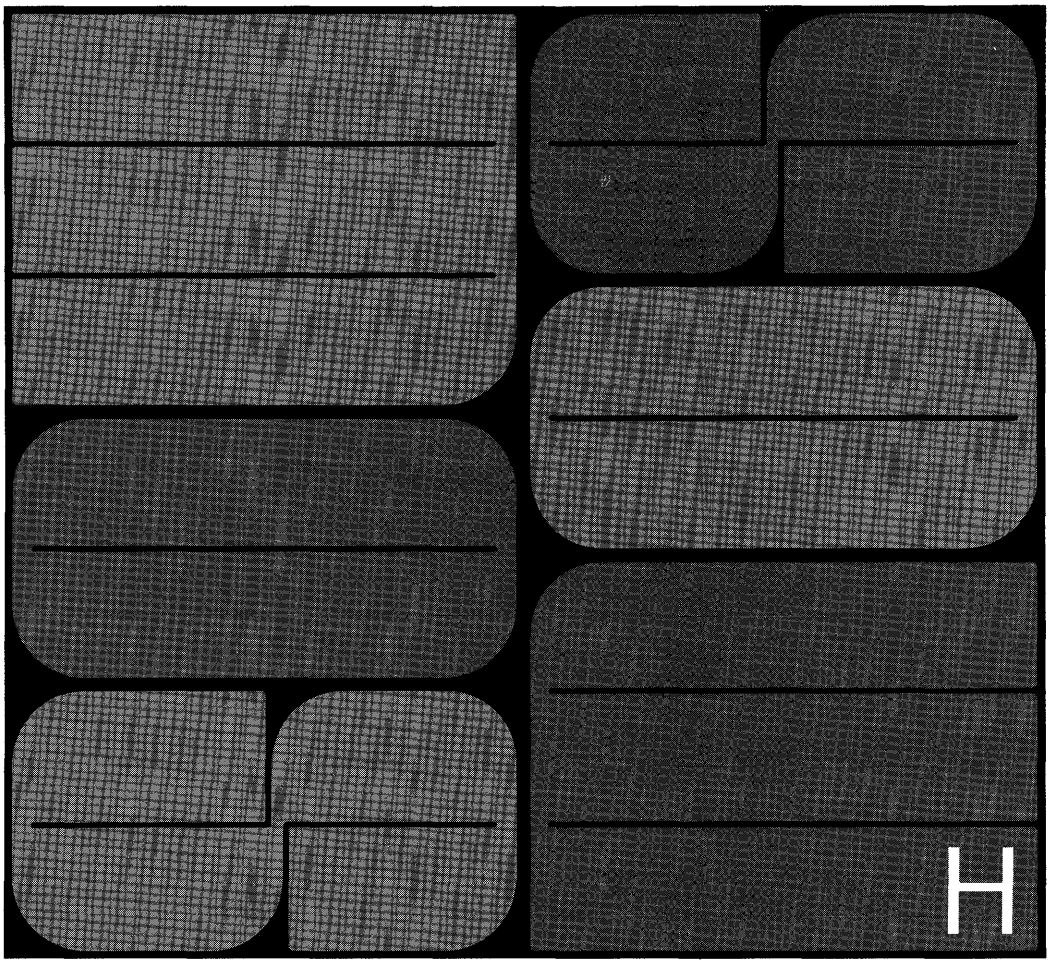
CIRCUIT CHARACTERISTICS

All of the above factors have had a synergistic effect on silicon gate MOS/LSI design. They encourage the use of large, complex, single chip subsystems since they result in an excellent cost/performance ratio per logic or memory function.

Consider just a few of the combinational effects. For example, the compact dimensions of silicon gate elements minimize overall array dimensions, further enhancing performance of a given number of functions. Since the overall loads are lighter, and easily driven, the transistors can be smaller to take advantage of the gate channel alignment. Because of the higher speed, less logic parallelism may be required and more actual functions can be performed per chip.

For a given number of functions, a silicon gate array may be only half the size of a metal gate array. This means smaller chips, or more functions on a given chip size, or larger chips capable of carrying an entire MOS/LSI subsystem. All alternatives lead to reduced system cost. For comparison, a large metal gate chip can carry about 200 random logic gates versus 300 to 500 gates feasible with only a medium size silicon gate chip.

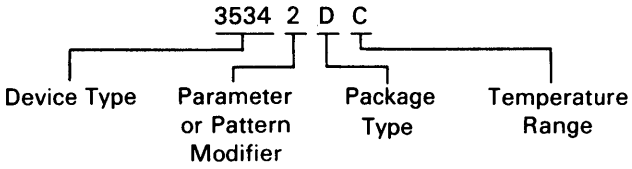
Ordering Information And Packaging



APPENDIX H

ORDERING INFORMATION AND PACKAGING

Device Order Number Format



DEVICE TYPE — Defines the function and electrical characteristics of the product.

PARAMETER OR PROGRAM PATTERN MODIFIER — Describes parameter or programmable change to product. Numbers denote electrical variations. Letters represent pattern or coding variations. If a product has both parameter and pattern variations, letters will be used. Unprogrammed versions of programmable devices have an X in the fifth digit position.

Examples:

Parameter Variations	Pattern Variations	Parameter and Pattern Variations
35342DC	3512XDC	3260XDC
35343DC	3512ADC	3260ADC
35344DC		3260BDC
35345DC		

If there are no parameter or pattern variations, the package style immediately follows the device type and the order number format is a total of 6 digits.

PACKAGE TYPE — Denotes the basic type of package used. The number of pins is described on the device data sheet and in package dimensions section which follows the product listing in this Appendix.

D — Ceramic Dual In-Line
F — Flat Package
H — TO-5 Metal Can

TEMPERATURE RANGE — Defines operating temperature

C — Commercial Grade 0°C to +70°C
L — Limited Military Grade -55°C to +85°C
M — Military Grade -55°C to +125°C

NOTE: No spaces are left in the ordering code. The code is either six positions for products without parameter or pattern variations or seven positions for products with parameter or pattern variations.

Example: 3341DC 3257ADC

PACKAGING INFORMATION

Device Type	Package Outline	Description
3100DL	7K	5-Input Gate
3101DL	7K	Dual J K Flip-Flop
3102HC	5F	3-Input Gate
3102HL	5F	3-Input Gate
3257ADC	7R	64 x 5 x 7 Out Character Generator, ASCII Font
3257XDC	7R	64 x 5 x 7 Out Character Generator, Custom Font
3258ADC	7K	64 x 7 x 5 Out Character Generator, ASCII Font, 625 ns Access Time
3258BDC	7K	64 x 7 x 5 Out Character Generator, ASCII Font, 695 ns Access Time
3258CDC	7K	64 x 7 x 5 Out Character Generator, ASCII Font, 780 ns Access Time
3258DDC	7K	64 x 7 x 5 Out Character Generator, ASCII Font, 1 µs Access Time
3258XDC	7K	64 x 7 x 5 Out Character Generator, Custom Font, Specify Speed
3260ADC	7R	64 x 9 x 7 Out Character Generator, ASCII Font, 625 ns Access Time
3260BDC	7R	64 x 9 x 7 Out Character Generator, ASCII Font, 800 ns Access Time
3260XDC	7R	64 x 9 x 7 Out Character Generator, Custom Font, Specify Speed
32611DC	7K	Color TV Sync Generator
32612DC	7K	Black/White TV Sync Generator
3300FC	3W	25-Bit Static Shift Register
3300FL	3W	25-Bit Static Shift Register
3300HC	5F	25-Bit Static Shift Register
3300HL	5F	25-Bit Static Shift Register
3325HC	5F	Quad 64-Bit Dynamic Shift Register
3326HC	5E	Triple 66-Bit Dynamic Shift Register
3326HL	5E	Triple 66-Bit Dynamic Shift Register
3329HC	5F	512-Bit Dynamic Shift Register
3330HC	5F	480-Bit Dynamic Shift Register
3331HC	5F	500-Bit Dynamic Shift Register

PACKAGING INFORMATION

Device Type	Package Outline	Description
3341DC	7K	64 x 4 First-In First-Out Memory
3342DC	7K	Quad 64-Bit Static Shift Register
3343HC	5F	Dual 128-Bit Static Shift Register
3344HC	5F	Dual 132-Bit Static Shift Register
3345HC	5F	Dual 136-Bit Static Shift Register
3346HC	5F	Dual 144-Bit Static Shift Register
3347DC	7K	Quad 80-Bit Static Shift Register
3348DC	7R	Hex 32-Bit Static Shift Register with Buffer Enable
3349DC	7K	Hex 32-Bit Static Shift Register
3383HC	5F	256-Bit Dynamic Shift Register
3501XDC	7R	128 x 8 (1024-Bit) Read Only Memory, Custom Pattern
3501XDL	7R	128 x 8 (1024-Bit) Read Only Memory, Custom Pattern
3512ADC	7R	256 x 8 (2048-Bit) Read Only Memory, Selectric to ASCII/ASCII to Selectric
3512XDC	7R	256 x 8 (2048-Bit) Read Only Memory, Custom Pattern
3513XDC	7R	256 x 10 (2560-Bit) Read Only Memory, Custom Pattern
3514ADC	7R	512 x 8 (4096-Bit) Read Only Memory, ASCII-EBCDIC/EBCDIC-ASCII,700 ns
3514BDC	7R	512 x 8 (4096-Bit) Read Only Memory, ASCII-EBCDIC/EBCDIC-ASCII, 1 µs
3514XDC	7R	512 x 8 (4096-Bit) Read Only Memory, Custom Pattern, Specify Speed
35321DC	7K	512 x 1 Static Read/Write Memory, 550 ns Access Time
35322DC	7K	512 x 1 Static Read/Write Memory, 920 ns Access Time
35342DC/1103	7T	1024 x 1 Dynamic Read/Write Memory, 300 ns Access Time
35343DC/1103S146	7T	1024 x 1 Dynamic Read/Write Memory, 220 ns Access Time
35344DC/1103-1	7T	1024 x 1 Dynamic Read/Write Memory, 180 ns Access Time
35345DC/1103-2	7T	1024 x 1 Dynamic Read/Write Memory, 150 ns Access Time
37002DC	7K	4-Channel Multiplexer ± 5V Operation
37002DL	7K	4-Channel Multiplexer ± 5V Operation
37002DM	7K	4-Channel Multiplexer ± 5 V Operation
37002FC	3W	4-Channel Multiplexer ± 5 V Operation
37002FL	3W	4-Channel Multiplexer ± 5 V Operation
37002FM	3W	4-Channel Multiplexer ± 5 V Operation
37003DC	7K	4-Channel Multiplexer - 0+5 V Operation
37003DL	7K	4-Channel Multiplexer - 0+5 V Operation
37003DM	7K	4-Channel Multiplexer - 0+5 V Operation
37003FC	3W	4-Channel Multiplexer - 0+5 V Operation
37003FL	3W	4-Channel Multiplexer - 0+5 V Operation
37003FM	3W	4-Channel Multiplexer - 0+5 V Operation
3701FC	3W	6-Channel Multiplexer
3701FM	3W	6-Channel Multiplexer
37052DC	7K	8-Channel Decoded Multiplexer, ±5 V Operation
37052DL	7K	8-Channel Decoded Multiplexer, ±5 V Operation
37053DC	7K	8-Channel Decoded Multiplexer, −0+5 V Operation
37053DL	7K	8-Channel Decoded Multiplexer, −0+5 V Operation
37082DC	7K	8-Channel Decoded Multiplexer, ±5 V Operation
37082DL	7K	8-Channel Decoded Multiplexer, ±5 V Operation
37083DC	7K	8-Channel Decoded Multiplexer, −0+5 V Operation
37083DL	7K	8-Channel Decoded Multiplexer, −0+5 V Operation
3750DC	6H	10-Bit D to A Converter
3750DL	6H	10-Bit D to A Converter
3751DC	6H	12-Bit A to D Converter
3751DL	6H	12-Bit A to D Converter
3800DC	6H	8-Bit Parallel Accumulator
3800DL	6H	8-Bit Parallel Accumulator
3801DC	6H	16-Bit S-P, P-S Converter
3801DL	6H	16-Bit S-P, P-S Converter
3803DC	7Q	PPS 25 Keyboard Expander Unit
3805DC	7T	PPS 25 Arithmetic Unit
3806XDC	7R	PPS 25 Function and Timing Unit, Custom Pattern
3807DC	7Q	PPS 25 Keyboard Unit
3808DC	7K	PPS 25 Memory Register Unit
3809DC	7K	PPS 25 Memory Register Unit
3810XDC	7K	PPS 25 Read-Only Memory Unit, Custom Pattern
3811DC	7R	PPS 25 Output Unit

PACKAGING INFORMATION

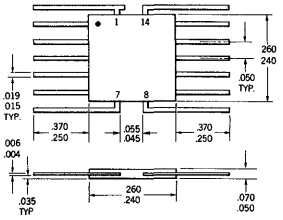
Device Type	Package Outline	Description
3814DC	7R	Digital Voltmeter Logic
3815DC*	7R	5-Decade Counter
3816DC*	7K	÷3 to 261,145 Programmable Counter
3820DC	7Q	SPRINT Keyboard Unit
3821DC	7Q	SPRINT Output Unit
3822DC	7Q	SPRINT Control Unit
3823DC	7K	SPRINT Register Unit
3824DC	7R	SPRINT Arithmetic Unit
Associated Hybrid		
SH0013C1	5V	2-Phase MOS Clock Driver (–55°C to +125°C)
SH0013C9	5V	2-Phase MOS Clock Driver (0°C to +85°C)

*To be announced.

PACKAGE PHYSICAL DIMENSIONS

3W

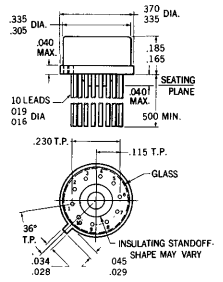
In accordance with JEDEC (TO-86) Outline 14 Lead Flat Pak



NOTES: All dimensions in inches
Base, leads and ring frame are gold-plate kovar, remainder is alumina filled glass
Package weight is approximately 0.26 gram
Cavity size is .110 x .130
Lead 1 orientation may be either tab or dot

5E

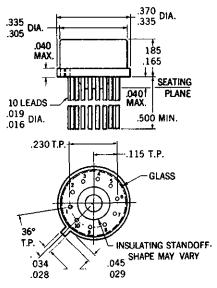
In accordance with JEDEC (TO-100) Outline (15 mil kovar header)



NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
Ten leads through

5F

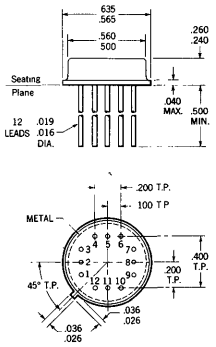
In accordance with JEDEC (TO-100) Outline (15 mil kovar header)



NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
Nine leads through, lead No. 5 is connected to case

5V

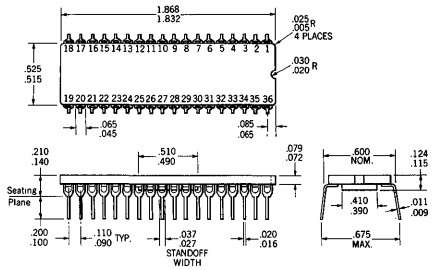
Similar to JEDEC (TO-8) Outline (60 mil kovar header)



NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 2.2 grams

6H

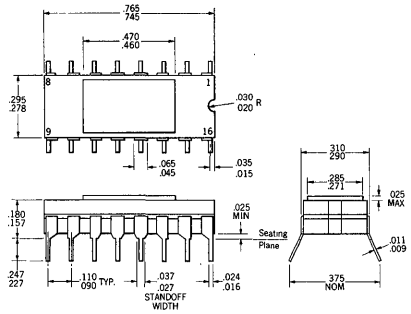
36 Lead Array Package



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated kovar
Package weight is 6.0 grams
Low temperature seal
Package material is alumina
Cavity size is .200 x .200

7K

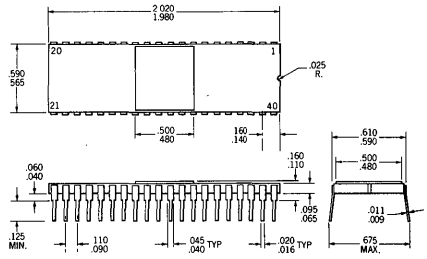
16 Lead Dual In-Line (Metal Cap)



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are gold-plated kovar
Package material is alumina
Low temperature seal
Cavity size is .170 x 215
Package weight is 1 3 grams

7Q

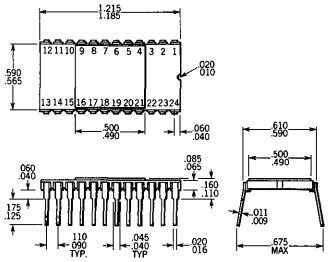
40 Lead Side Brazed Dual In-Line



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated kovar
Package weight is 6.2 grams

7R

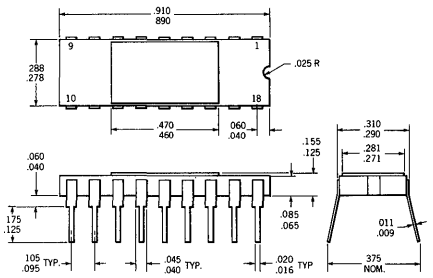
24 Lead Side Brazed Dual In-Line



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated kovar
Package weight is 4.1 grams

7T

18 Lead Side Brazed Dual In-Line



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are gold-plated kovar
Package weight is 1.3 grams

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