Fairchild Semiconductor Integrated Circuit Data Catalog 1970

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The Fairchild Semiconductor Integrated Circuit Data Catalog contains product information on Fairchild's complete line of digital and linear integrated circuits. Comprehensive data sheet specifications are provided for each device, including Medium Scale Integration (MSI) devices. Also included for your convenience: a complete listing of Application Notes and Technical Papers (all available upon request), a preview of new products and reply cards for further information.

Library of Congress Catalog Card 75-87311

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NOTE: Six business reply cards may be found at the back of the book.

HOW TO USE THE DATA CATALOG

The Fairchild Integrated Circuit Data Catalog is divided into five sections by product line: Compatible Current Sinking Logic, Special Circuits, Hybrid Circuits, Linear Circuits, and MOS Circuits.

A comprehensive listing of integrated circuits is provided on page 1-1. This index lists the device type, function, family, and page number of all Fairchild circuits manufactured at the time of publication. In addition, a numerical index by family is provided on page 2-1. Thus, Fairchild's available products in a given category can be checked at a glance, or a particular device can be located even if its generic classification is not known.

In the first two sections, CCSL and Special Circuits, the data sheets appear in numerical order by logic family, i.e., TTμL, DTμL, CμL, RTμL, and CTμL. All products in each family are listed in the index at the beginning of each major section.

In the Hybrid, Linear, and MOS sections the data sheets appear in numerical order and are indexed at the beginning of each section.

For each family of circuits there is a cross reference table listing the packages available for each product category. For instance, the MOS 3750 10 Bit D/A Converter is available in Flat Pak and Dual In-Line packages.

For each category of integrated circuits there is a "Coming Soon" section with new product listings and descriptions. These are products for which there were no firm specifications at publishing date for the catalog. Complete specifications on these new products will be provided in the next edition of the data catalog.

Further information may be obtained by contacting your local Fairchild distributor or by sending in a reply card furnished in this catalog.

Integrated Circuits

INTEGRATED CIRCUITS NUMERICAL INDEX

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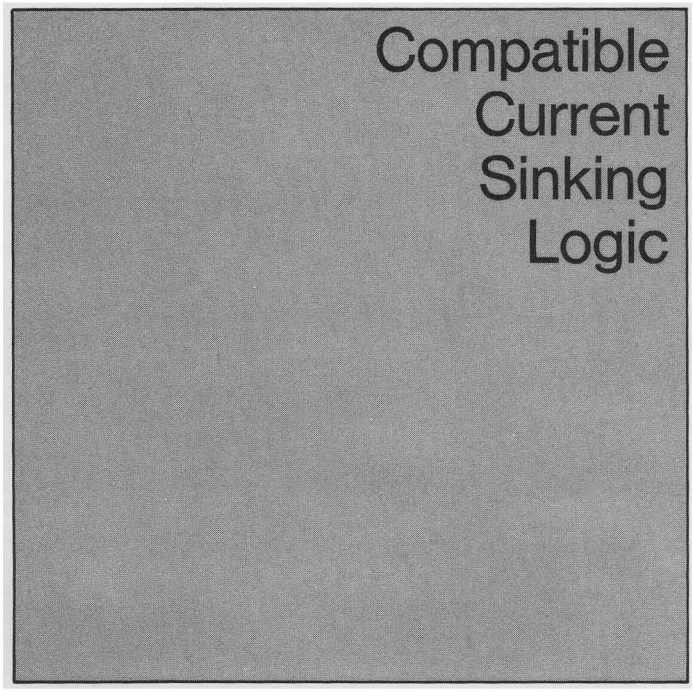
INTEGRATED CIRCUIT INDEX BY FAMILY


Compatible
Current
Sinking
Logic

COMPATIBLE CURRENT SINKING LOGIC NUMERICAL INDEX

CROSS REFERENCE — CCSL AND SPECIAL CIRCUITS

Function	LPDTμL Typ Tpd 65 ns	DTμL Typ Tpd 25 ns	TTμL Typ Tpd 10 ns	CCSL MSI	HLLDTμL	RTμL Typ Tpd 15 ns	LPRTμL Typ Tpd 40 ns	MμL	CTμL Typ Tpd 3.0 ns	CμL	Special
Gate											
Hex Inverter NAND Gate	F, D	F, D, C	FP, F, D		D						
Quad 2-input NAND Gate	F, D	F, D, C	FP, F, D								
Triple 3-input NAND Gate	F, D	F, D, C	FP, F, D								
Dual 4-input NAND Gate	F, D	F, D, C	FP, F, D								
8-input NAND Gate			FP, F, D								
Dual 2-wide Expandable AND/NOR Gate			F, FP, D								
4-wide Expandable AND/NOR Gate			F, FP, D								
Dual 4-input Power Gate	F, C, D	F, C, D	F, FP, D								
3-input NOR Gate						C, F					
4-input NOR Gate						C, F	C				
Dual 2-input NOR Gate						C, F, E	C		D		
Dual 3-input NOR Gate						C, F					
Quad Inverter NOR Gate						C, F					
2-2-3 Input AND Gate									D		
Dual 4-input AND Gate									D		
Dual Output, 8 Input AND Gate									D		
3-3-1 Input AND Gate									D		
Quad 1 AND Gate									D		
3 Output Quad 2 Input AND/OR Gate									D		
2 Output Quad 2 Input AND/OR Gate									D		
Buffer						C, FP, E	C		D		
Dual 2 Input									D		
Dual Buffer							C				
Counter Adapter						F, C					
Decoders						**Typ Tpd 10 ns**			**Typ Tpd 25 ns**	**Typ Tpd 2 ns**	
1 of 10 Decoder				F, D							
1 of 16 Decoder				F, D							
7 Segment Decoder				F, D							
Multiplexers											
Dual 4-input Multiplexer				F, D							
8-input Multiplexer				F, D							
Dual 8-input Multiplexer				F, D							
Counters											
BCD Up/Down Counter				F, D							
Decade Counter				F, D							
Hexidecimal Counter				F, D							
Hexidecimal Up/Down Counter				F, D							
Registers											
4 Bit Shift Register				F		D					
Dual 8 Bit Shift Register				D							
Adders & Comparators											
Dual Full Adder				F, D							
Dual Four-bit Comparator				F, D							
Half Adder						F, C	C				
Adder							C				

Legend: F = Flat Pak FP = Fairpak® D = Dip C = TO-5 E = TO-5 Epoxy

CROSS REFERENCE — CCSL AND SPECIAL CIRCUITS

Function	LPDTμL Typ Tpd 65 ns	DTμL Typ Tpd 25 ns	TTμL Typ Tpd 10 ns	CCSL MSI	HLLDTμL	RTμL Typ Tpd 15 ns	LPRTμL Typ Tpd 40 ns	MμL	CTμL Typ Tpd 3.0 ns	CμL	Special
Memory & Latches											
Dual 4 Input Latch				F, D							
16-bit Memory Cell				F, D							
256 Bit ROM				F, D							
Dual 4-bit Latch									D		
Buffer Memory										D	
Decimal DEC/DR										D	
Micromatrices											
32 Gate Customizable Array		F, D									
48 Gate Customizable Array			F, D								
96 Gate Customizable Array			F, D								
Kit Parts											
4501		D									
4522			D								
Gate Expanders	**Typ Tpd 130 ns**	**Typ Tpd 20 ns**	**Typ Tpd 25 ns**			**Typ Tpd 30 ns**	**Typ Tpd 20 ns**		**Typ Tpd 15 ns**		
Expander	F, C, D	F, C, D	FP, F, D				C				
Binary Elements											
RS Flip Flop							C				
Buffered JK Flip Flop	F, D	F, C, D	FP, F, D			F, C, E	C		D		
Dual Flip Flop		F, D	FP, F, D								
AC Coupled Flip Flop		F, C, D									
Type D Flip Flop							C				
Dual Rank Flip Flop									D		
One Half Shift Register With Inverter						F, C					
One Half Shift Register Without Inverter						F, C					
Interface Functions		**Typ Tpd 100 ns**									**Typ Tpd 2 ns**
Line Receiver											F, D
Line Driver											F, D
CCSL to MOS											F, D
MOS to CCSL											F, D
Multivibrators											
AC Coupled One Shot		F, C, D									
Retriggerable One Shot			F, D								

Legend: F = Flat Pak FP = Fairpak® D = Dip C = TO-5 E = TO-5 Epoxy

CCSL COMPOSITE DATA SHEET

COMPATIBLE CURRENT SINKING LOGIC

MILITARY TEMPERATURE RANGE −55°C TO +125°C

GENERAL DESCRIPTION

Fairchild Compatible Current Sinking Logic refers to all the standard Fairchild logic circuits that operate by sinking current into the outputs in the low state and supplying leakage current from the output in the high state. Current sinking logic is one of the three main forms of logic, the other two being current sourcing logic and current mode logic.

The Fairchild logic families that make up CCSL include Fairchild's 9300 series MSI (Medium Scale Integration), the 4500 DTμL Micromatrix™ array, the 4600 and 4700 TTμL Micromatrix arrays, TTμL (Transistor-Transistor Micrologic), DTμL (Diode-Transistor Micrologic), LPDTμL (Low Power Diode Transistor Micrologic), and other circuits that are not members of any specific logic family. All the circuits that make up CCSL have common power supply voltages and compatible logic levels at the input and output.

Since all the input and output levels are compatible, the system designer can use whichever device suits his application most closely without being limited to any one logic family. This flexibility can be of great advantage by allowing the system designer to achieve greater system optimization. MSI or Micromatrix arrays can be used to decrease package count, improve speed, and cut costs. TTμL offers high speed and good A.C. noise immunity where discrete gates and flip-flops are needed. DTμL has lower power, medium speed, and great flexibility because of wired-OR capability. LPDTμL offers very low power and reasonable speed.

To achieve the CCSL concept, a set of normalized rules had to be generated. These are explained and specified for every device in the CCSL family in the data sheet.

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FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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CCSL LOADING RULES

—55°C TO +125°C TEMPERATURE RANGE

GENERAL INFORMATION

The Fairchild CCSL loading rules were established to give the systems designer exact rules for combining the different families of Fairchild Compatible Current Sinking Logic elements.

In establishing the rules, worst case limits and conditions are guaranteed providing:

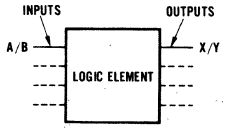
1. The loading rules are obeyed
2. V_{CC} is maintained at 5.0 V ±10% (4.5 V to 5.5 V)
3. The ambient temperature is maintained between —55°C and +125°C.

The worst case limits guaranteed are:

Maximum low level output voltage (V_{OL})	=	0.4 V
Maximum low level input voltage (V_{IL})	=	0.7 V
Minimum high level output voltage (V_{OH})	=	2.5 V
Minimum high level input voltage (V_{IH})	=	2.1 V
High level D.C. noise immunity	=	0.4 V
Low level D.C. noise immunity	=	0.3 V

LOADING RULES

In this data sheet the following notation has been chosen to indicate the input loading and output drive factors for all logic elements.



A (high level input load factor) = maximum normalized input current drawn into an input when the input is at a high level.

B (low level input load factor) = maximum normalized input current drawn out of an input when the input is at a low level.

X (high level output drive factor) = minimum normalized output current which the output can supply at a high level while maintaining $V_{OH} > 2.5$ V

Y (low level output drive factor) = minimum normalized output current which the output can sink at a low level, while maintaining $V_{OL} < 0.4$ V

Any CCSL device can drive any combination of other CCSL devices as long as two conditions are met:

1. The sum of the high level load factors at any node must be less than or equal to the high level drive factor at that node.
2. The sum of the low level load factors at any node must be less than or equal to the low level drive factor at that node.

SHORTED INPUTS

In the case where unused inputs of an AND gate are shorted to a driven input, the high level input load factor for the inputs will be the number of inputs shorted together times the high level input load factor for one input. The low level input load factor for the inputs will be the same as that for a single input.

NORMALIZING FACTORS

The normalizing factors used to derive these loading rules are listed below. They are included in the data sheet primarily as a guideline when working with open collector devices such as the DTμL 9944 or the MμL 9033. They allow the designer to determine:

1. What collector pullup resistor is required to drive the high level loads, and supply the I_{CEX} while maintaining V_{OH}.
2. How much the low level fanout must be reduced because of the pullup resistor.

LOGIC LEVEL	WORST CASE UNIT LOAD/DRIVE FACTOR	V_{CC} SUPPLY VOLTAGE
High	5 μA	4.5 V to 5.5 V
Low	124 μA	4.5 V
	160 μA	5.5 V

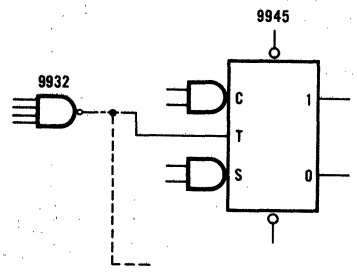
WIRED-OR APPLICATIONS

It is possible to perform the wired-OR function by connecting together the outputs of any of the DTμL circuits, except the 9932 and 9950, or of any circuit that has the words "open collector" rather than a high level output drive factor.

In wired-OR applications each gate must be able to sink the current from all the pullup resistors, as well as the current from the load being driven at the common wired-OR point. To calculate the load driving capability of a wired-OR configuration simply find the equivalent low level load factor for all the excess load resistors and subtract it from each gate's low level drive factor. For DTμL with 6K pullup resistor, the equivalent load factor is 8, for DTμL with 2K pullup, it is 22. For a discrete pullup resistor, the load factor can be calculated from the normalizing factors above. The high level output drive factor of the gates performing the wired-OR function is the sum of the high level drive factors of all the gates in the combination. See Example 3 for an example of a wired-OR application.

EXAMPLE 1:

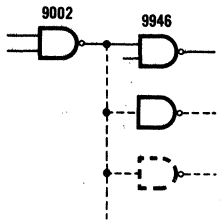
DTμL 9932 driving DTμL 9945 clock lines.
Problem: How many 9945's can be driven by one 9932?



The output drive factor of the 9932 is 800/235. The input load factor of the 9945 is 4/19. First divide the high level input load factor of the 9945 (4) into the high level drive factor of the 9932 (800). This gives 200 as the number of 9945 clock inputs the 9932 may drive in the high state. Then repeat the procedure with the low level load factor and low level drive factor. This gives 12.4 as the number of 9945 inputs a 9932 can drive in the low state. The low state is the lower number, so it is necessary to limit the number of 9945's to 12.

EXAMPLE 2:

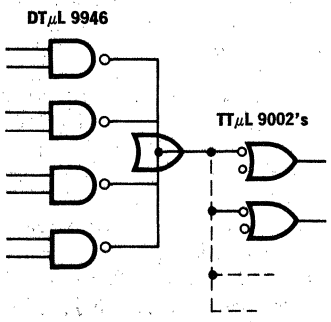
TTμL 9002 driving DTμL gates.
Problem: How many gates can one 9002 drive?



The output drive factor of the 9002 is 264/110. The input load factor of the 9946 is 1/9.4. Dividing the low level input load factor of the 9946 into the low level drive factor of the 9002 gives $\sim$ 11.7. Dividing the high level input load factor into the high level drive factor gives 264. Therefore, the fanout is limited to 11 by the low level load and drive factors.

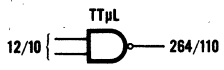
EXAMPLE 3:

4 DTμL 9946's in a wired-OR configuration.
Problem: How many TTμL 9002 inputs will the output drive?

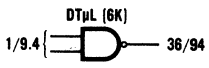


The output drive factor of the DTμL 9946 is 36/94. The output pull-up resistor is 6K, so 8 must be subtracted from the low level drive factor for each extra output tied together in the wired-OR configuration. With four outputs tied together, there are three excess pull-up resistors and 24 must be subtracted from 94 (the low level output drive factor of each 9946) to give an output low level drive factor of 70. The output high level drive is the sum of all the high level drive factors of the four 9946's. Thus the high level load factor of the combination is $36 + 36 + 36 + 36 = 144$. The 9002 inputs have load factors of 12/10, so it can be determined, as in previous examples, that the limiting factors are the low level drive and load factors and that the four gates in the wired-OR will drive seven 9002 inputs.

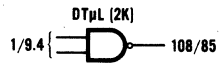
QUAD 2-INPUT NAND GATES



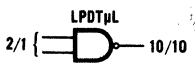
9002



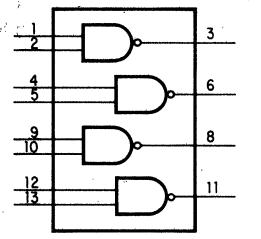
9946



9949

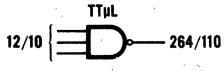


9046

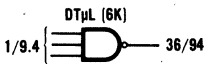


PIN CONFIGURATION

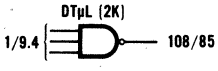
TRIPLE 3-INPUT NAND GATES



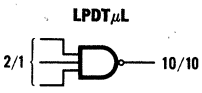
9003



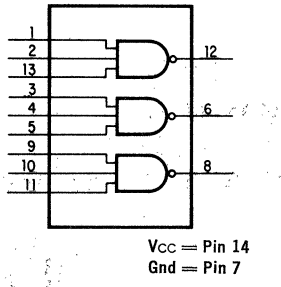
9962



9963

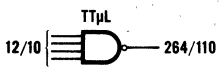


9047

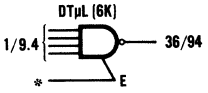


PIN CONFIGURATION

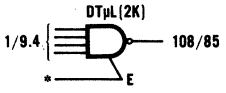
DUAL 4-INPUT NAND GATES



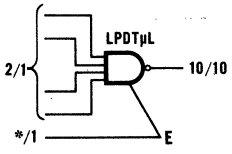
9004



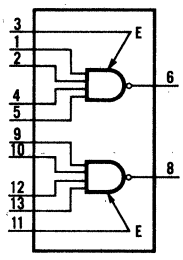
9930



9961



9044

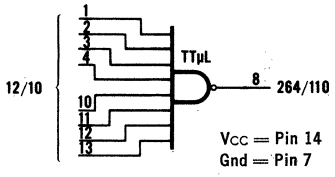


Extenders are not present on 9004

PIN CONFIGURATION

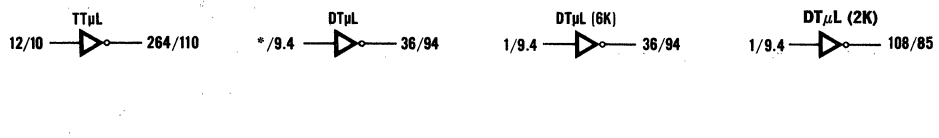
* Extender Inputs, see note on Page 10

8-INPUT NAND GATE

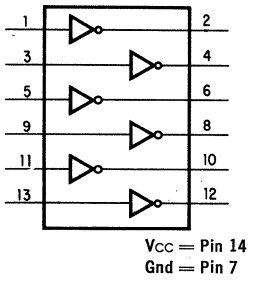


9007

HEX INVERTERS



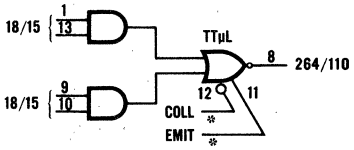
9016 9935 9936 9937



PIN CONFIGURATION

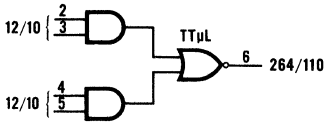
* Extender Inputs, see note on Page 10

AND-OR-INVERT GATES AND EXTENDER

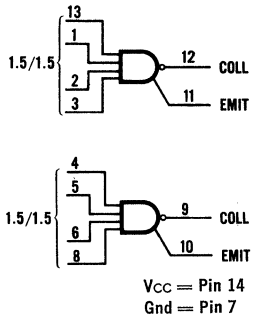


* Up to four 9006 Extenders may be tied to these terminals

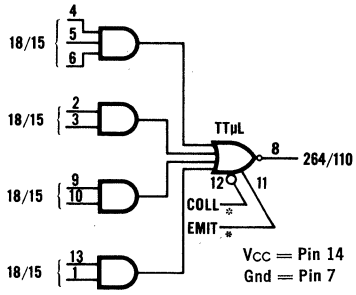
9005 EXTENDABLE HALF



9005 NONEXTENDABLE HALF



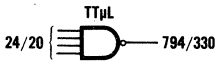
9006



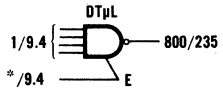
* Up to four 9006 Extenders may be tied to these terminals

9008

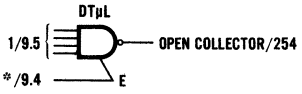
DUAL 4-INPUT NAND BUFFERS



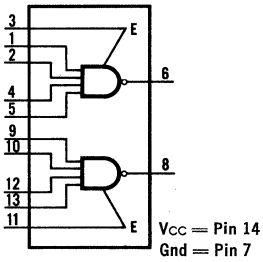
9009



9932



9944

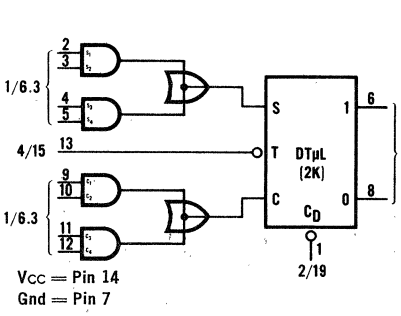


Extender inputs not present on 9009

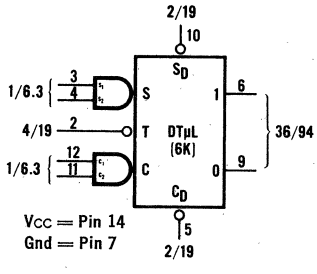
PIN CONFIGURATION

* Extender Inputs, see note on Page 10

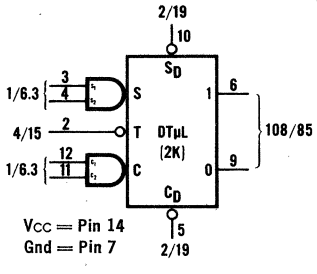
R-S FLIP-FLOPS



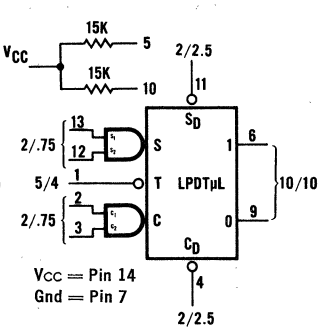
9111



9945

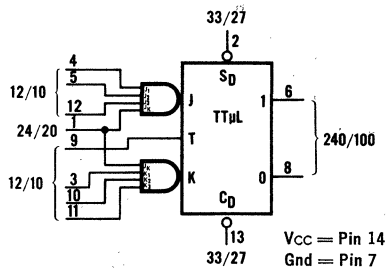


9948

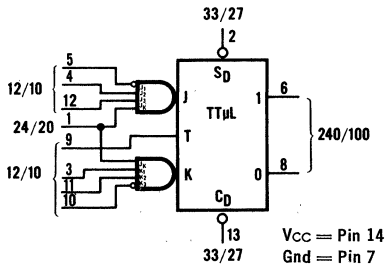


9040

J-K FLIP-FLOPS

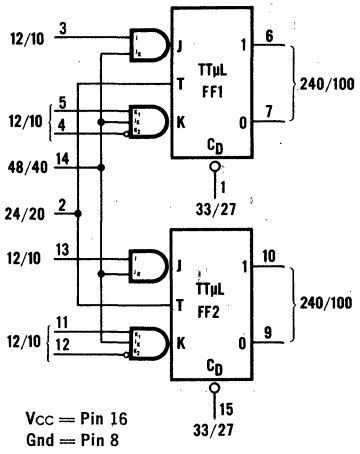


9000

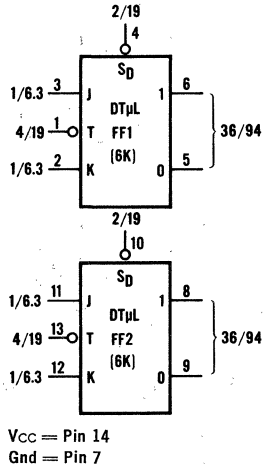


9001

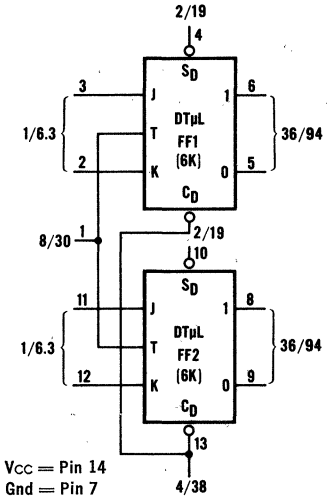
DUAL J-K FLIP-FLOPS



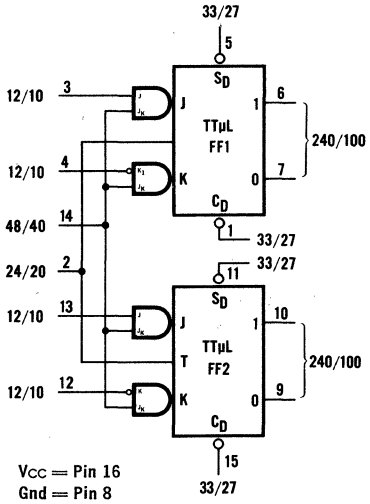
9020



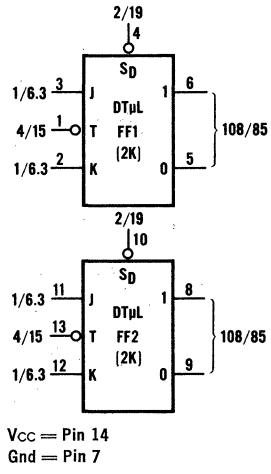
9093



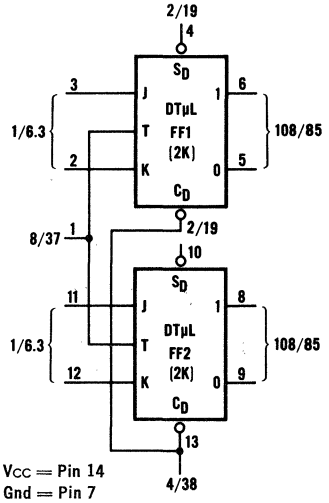
9097



9022

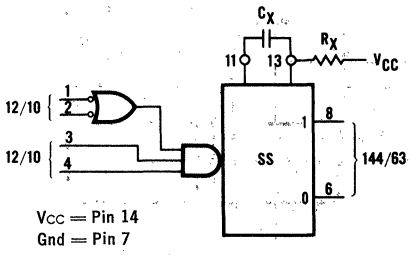


9094

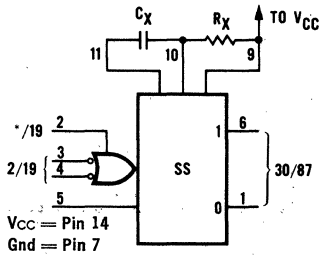


9099

MONOSTABLE MULTIVIBRATORS

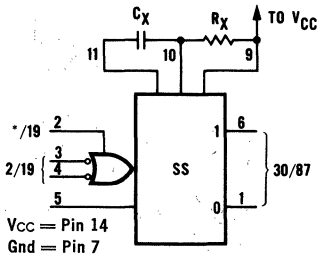


9601



The DTμL 9941 is NOT recommended for new designs; use the 9601.

9941



The DTμL 9951 is NOT recommended for new designs; use the 9601.

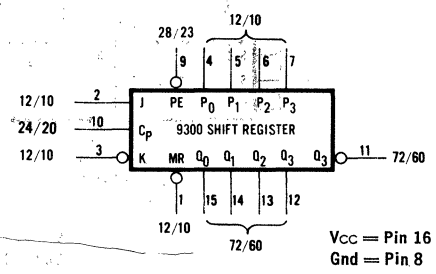
9951

NOTE: The maximum input fall time to trigger is: 25 ns for a 1.0 volt swing; 50 ns for a 2.0 volt swing; 100 ns for a 4.0 volt swing.

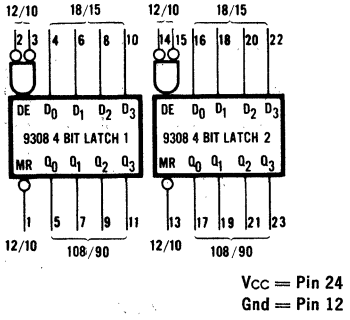
* Extender Inputs, see note on Page 10

MEDIUM SCALE INTEGRATION

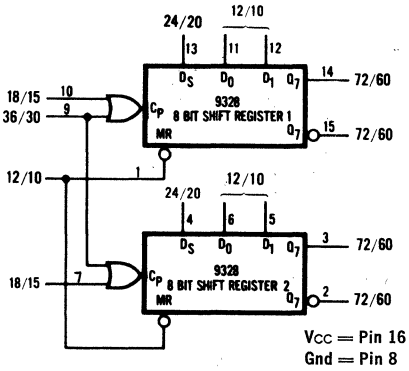
SHIFT REGISTERS AND STORAGE ELEMENTS



9300
4 BIT UNIVERSAL REGISTER

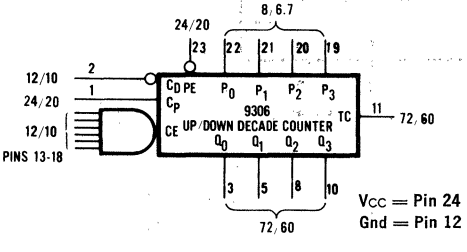


9308
DUAL 4 BIT LATCH

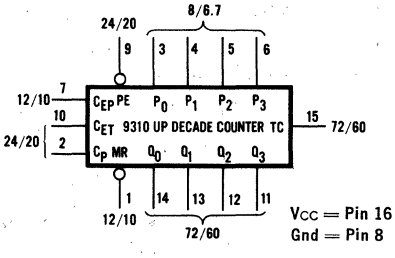


9328
DUAL 8 BIT SHIFT REGISTER

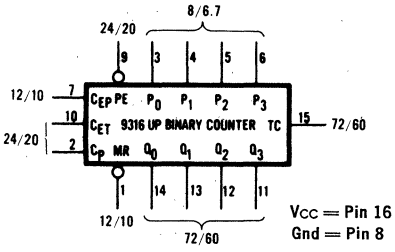
COUNTERS



9306
UP/DOWN DECADE COUNTER



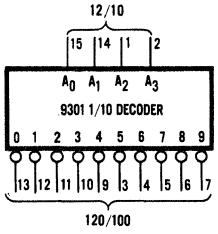
9310
UP DECADE COUNTER



9316
UP BINARY COUNTER

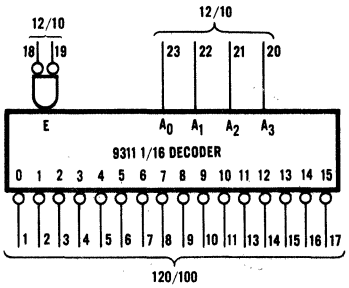
MEDIUM SCALE INTEGRATION (Cont'd.)

COMBINATIONAL LOGIC



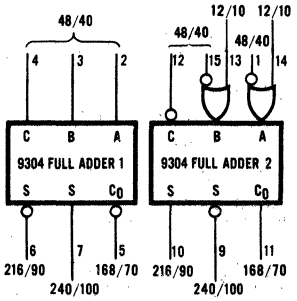
V_{CC} = Pin 16
Gnd = Pin 8

9301
1 OF 10 DECODER



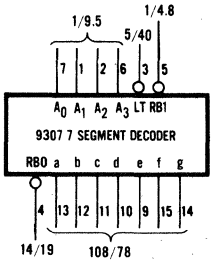
V_{CC} = Pin 24
Gnd = Pin 12

9311
1 OF 16 DECODER



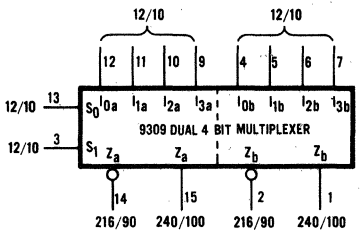
V_{CC} = Pin 16
Gnd = Pin 8

9304
DUAL FULL ADDER



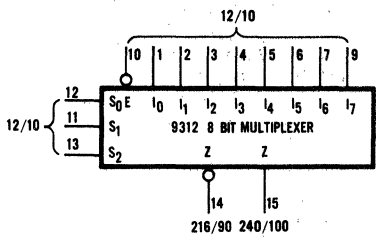
V_{CC} = Pin 16
Gnd = Pin 8

9307
BCD TO 7 SEGMENT DECODER



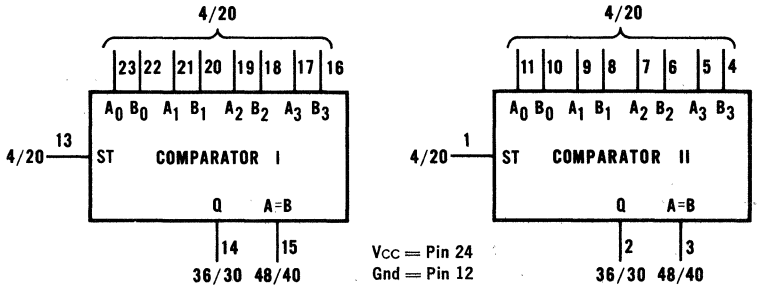
V_{CC} = Pin 16
Gnd = Pin 8

9309
DUAL 4 BIT MULTIPLEXER



V_{CC} = Pin 16
Gnd = Pin 8

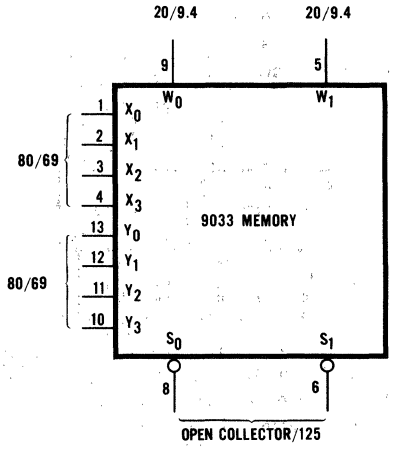
9312
8 BIT MULTIPLEXER



V_{CC} = Pin 24
Gnd = Pin 12

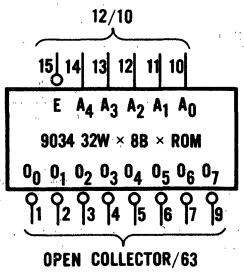
4510
DUAL 4 BIT COMPARATOR

MEMORIES



V_{CC} = Pin 14
Gnd = Pin 7

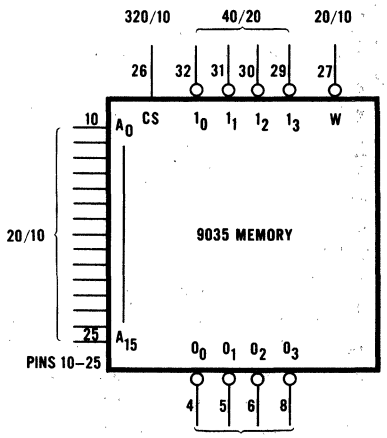
9033
16 Bit Scratch Pad Memory



V_{CC} = Pin 16
Gnd = Pin 8

NOTE: The 9034 is programmed on a custom basis. Contact your Fairchild salesman for more information.

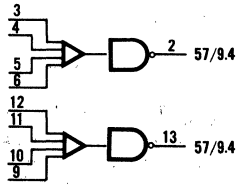
9034
32 Word by 8 Bit Read Only Memory



V_{CC} = Pin 28
Gnd = Pin 9

9035
64 Bit Read/Write Memory Cell

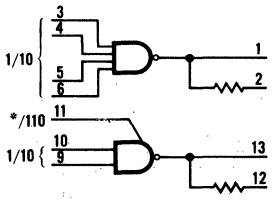
INTERFACE ELEMENTS



Inputs are differential, one pair attenuated, one pair nonattenuated.

V_{CC} = Pin 14
Gnd = Pin 7
+8 V = Pin 8

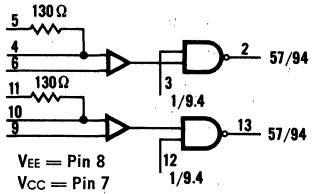
9620
Dual Differential Line Receiver



Outputs are extremely low impedance to drive long lines. Back matching resistors for 130 Ω line are provided.

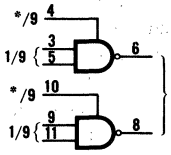
V_{CC} = Pin 14
Gnd = Pin 7
+8 V = Pin 8

9621
Dual Line Driver



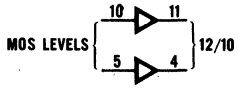
V_{EE} = Pin 8
V_{CC} = Pin 7
Gnd = Pin 14
S_3 = Pin 1
If S_3 = V_{CC}, then output is normally high with inputs open
If S_3 = Gnd 7, then output is normally low with inputs open

9622
Dual Differential Line Receiver (CCSL Threshhold Inputs)



V_{CC} = Pin 14
V_{DD} = Pin 7
Gnd = Pin 1
T_{AP} = Pin 13

9624
CCSL to MOS Converter

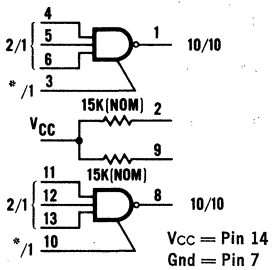


Gnd = Pin 1
V_{DD} = Pin 7
V_{CC} = Pin 14

9625
MOS to CCSL Converter

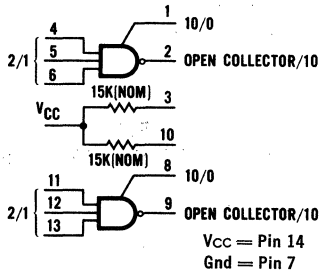
* Extender Inputs, see note on Page 10

SPECIAL LOW POWER GATES



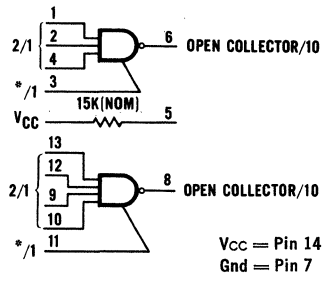
V_{CC} = Pin 14
Gnd = Pin 7

9041



V_{CC} = Pin 14
Gnd = Pin 7

9042



V_{CC} = Pin 14
Gnd = Pin 7

9043

* Extender Inputs, see note on Page 10

EXTENDER INPUTS

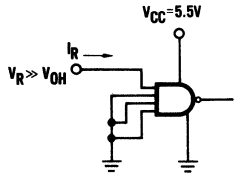
Extender inputs require DTμL 9933 or external silicon diodes in order to be used. Use of extender pins without diodes is not recommended. The low level load factor is determined by the resistor already included in the device. The high level load factor is usually negligible as most discrete silicon diodes have leakages of less than 1.0 μA at +125°C. A leakage of 1.0 μA corresponds to an input high level load factor of 0.2. The normalizing factor given in the introduction can always be used to determine the load factor of a diode. In order to maintain CCSL levels the diode should have <0.65 volt drop at 1.5 mA of current at 25°C.

APPENDIX

The purpose of this appendix is to cover in more detail the testing of CCSL products and thereby show how the logic levels are guaranteed. The testing must guarantee the input loading in both the high and low states and also must guarantee the output drive capability in both the high and low states. Both input and output characteristics must be guaranteed at worst case V_{CC} and input conditions and over the temperature range.

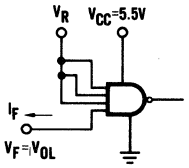
The examples given are for NAND gates. The application of the ideas to more complex devices is very much the same, except that manipulation of the inputs to achieve a required condition is more complex. Testing is always done with the worst case set of inputs.

First, consider the testing of the inputs to guarantee the input load factors. The high state input load current is tested by grounding the other inputs of the gate under test and measuring the input current with a voltage much higher than V_{OH}. Maximum V_{CC} is applied to the device as this has been found to be the worst case for TTμL circuits. The maximum allowed input high current is normalized to give the high level input load factor.



I_R TEST CIRCUIT

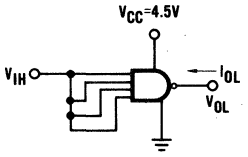
To test the low level input load factor, a voltage equal to V_{OL} is applied to one input and the current flowing out of the input is measured. The other inputs are tied to a high voltage. Maximum V_{CC} is used.



I_F TEST CIRCUIT

This maximum allowed input low current is normalized to give the low level input load factor.

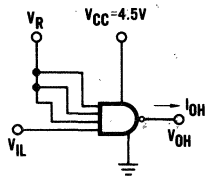
The output must be tested to insure that it meets the required high and low level drive factors, while maintaining the required noise immunity. To test the low level output drive factor, all inputs are maintained at V_{IH}, the minimum high level input voltage. The V_{CC} is maintained at 4.5 Volts and current is forced into the output. This current, I_{OL}, is related to the output low level drive factor by the normalizing factors for 4.5 Volts. The output voltage is measured to insure that it is less than V_{OL}.



I_{OL} TEST CIRCUIT

The test is repeated with $V_{CC} = 5.5$ Volts and the I_{OL} determined by the 5.5 Volts normalizing factor.

The output is then tested for the output high level drive factor. The maximum low level input voltage is applied to one input at a time with the other inputs held high. Current is then pulled out of the output. This current, I_{OH}, is related by normalizing factors to the output high level drive factor. The output voltage is measured to insure that it exceeds V_{OH}.



Each input is tested separately

I_{OH} TEST CIRCUIT

CCSL COMPOSITE DATA SHEET

COMPATIBLE CURRENT SINKING LOGIC

TEMPERATURE RANGE 0°C TO 75°C

GENERAL DESCRIPTION

Fairchild Compatible Current Sinking Logic refers to all the standard Fairchild logic circuits that operate by sinking current into the outputs in the low state and supplying leakage current from the output in the high state. Current sinking logic is one of the three main forms of logic, the other two being current sourcing logic and current mode logic.

The Fairchild logic families that make up CCSL include Fairchild's 9300 series MSI (Medium Scale Integration), the 4500 DTμL Micromatrix™ array, the 4600 and 4700 TTμL Micromatrix arrays, TTμL (Transistor-Transistor Micrologic), DTμL (Diode-Transistor Micrologic), LPDTμL* (Low Power Diode Transistor Micrologic), and other circuits that are not members of any specific logic family. All the circuits that make up CCSL have common power supply voltages and compatible logic levels at the input and output.

Since all the input and output levels are compatible, the system designer can use whichever device suits his application most closely without being limited to any one logic family. This flexibility can be of great advantage by allowing the system designer to achieve greater system optimization. MSI or Micromatrix arrays can be used to decrease package count, improve speed, and cut costs. TTμL offers high speed and good A.C. noise immunity where discrete gates and flip-flops are needed. DTμL has lower power, medium speed, and great flexibility because of wired-OR capability. LPDTμL offers very low power and reasonable speed.

To achieve the CCSL concept, a set of normalized rules had to be generated. These are explained and specified for every device in the CCSL family in the data sheet.

* Since LPDTμL is not manufactured in a 0°C to 75°C temp range, it is not included in this data sheet. The load rules given for it in the −55°C to +125°C temp range CCSL data sheet apply also for 0° to 75°C operation.

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FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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CCSL LOADING RULES
0°C TO 75°C TEMPERATURE RANGE

GENERAL INFORMATION

The Fairchild CCSL loading rules were established to give the systems designer exact rules for combining the different families of Fairchild Compatible Current Sinking Logic elements.

In establishing the rules, worst case limits and conditions are guaranteed providing:

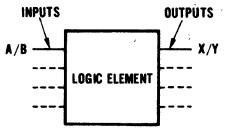
1. The loading rules are obeyed
2. V_{CC} is maintained at 5.0 V ±5% (4.75 V to 5.25 V)
3. The ambient temperature is maintained between 0°C and 75°C.

The worst case limits guaranteed are:

Maximum low level output voltage (V_{OL})	=	0.45 V
Maximum low level input voltage (V_{IL})	=	0.85 V
Minimum high level output voltage (V_{OH})	=	2.4 V
Minimum high level input voltage (V_{IH})	=	2.0 V
D.C. noise immunity	=	0.4 V

LOADING RULES

In this data sheet the following notation has been chosen to indicate the input loading and output drive factors for all logic elements.



A (high level input load factor) = maximum normalized input current drawn into an input when the input is at a high level.

B (low level input load factor) = maximum normalized input current drawn out of an input when the input is at a low level.

X (high level output drive factor) = minimum normalized output current which the output can supply at a high level while maintaining $V_{OH} > 2.4$ V

Y (low level output drive factor) = minimum normalized output current which the output can sink at a low level, while maintaining $V_{OL} < .45$ V

Any CCSL device can drive any combination of other CCSL devices as long as two conditions are met:

1. The sum of the high level load factors at any node must be less than or equal to the high level drive factor at that node.
2. The sum of the low level load factors at any node must be less than or equal to the low level drive factor at that node.

SHORTED INPUTS

In the case where unused inputs of an AND gate are shorted to a driven input, the high level input load factor for the inputs will be the number of inputs shorted together times the high level input load factor for one input. The low level input load factor for the inputs will be the same as that for a single input.

NORMALIZING FACTORS

The normalizing factors used to derive these loading rules are listed below. They are included in the data sheet primarily as a guideline when working with open collector devices such as the DTμL 9944 or the MμL 9033. They allow the designer to determine:

1. What collector pullup resistor is required to drive the high level loads, and supply the I_{CEX} while maintaining V_{OH}.
2. How much the low level fanout must be reduced because of the pullup resistor.

LOGIC LEVEL	WORST CASE UNIT LOAD/DRIVE FACTOR	V_{CC} SUPPLY VOLTAGE
High	5 μA	4.75 V to 5.25 V
Low	141 μA	4.75 V
	160 μA	5.25 V

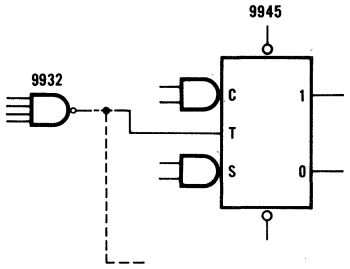
WIRED-OR APPLICATIONS

It is possible to perform the wired-OR function by connecting together the outputs of any of the DTμL circuits, except the 9932 and 9950, or of any circuit that has the words "open collector" rather than a high level output drive factor.

In wired-OR applications each gate must be able to sink the current from all the pullup resistors, as well as the current from the load being driven at the common wired-OR point. To calculate the load driving capability of a wired-OR configuration simply find the equivalent low level load factor for all the excess load resistors and subtract it from each gate's low level drive factor. For DTμL with 6K pullup resistor, the equivalent load factor is 8, for DTμL with 2K pullup, it is 22. For a discrete pullup resistor, the load factor can be calculated from the normalizing factors above. The high level output drive factor of the gates performing the wired-OR function is the sum of the high level drive factors of all the gates in the combination. See Example 3 for an example of a wired-OR application.

EXAMPLE 1:

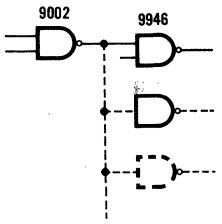
DTμL 9932 driving DTμL 9945 clock lines.
Problem: How many 9945's can be driven by one 9932?



The output drive factor of the 9932 is 600/235. The input load factor of the 9945 is 6/19. First divide the high level input load factor of the 9945 (6) into the high level drive factor of the 9932 (600). This gives 100 as the number of 9945 clock inputs the 9932 may drive to in the high state; Then repeat the procedure with the low level load factor and low level drive factor. This gives 12.4 as the number of 9945 inputs a 9932 can drive in the low state. The low state is the lower number, so it is necessary to limit the number of 9945's to 12.

EXAMPLE 2:

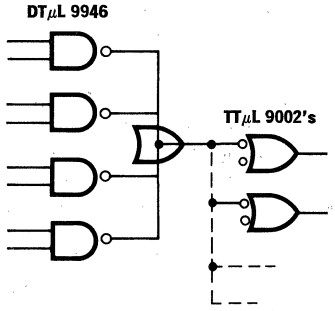
TTμL 9002 driving DTμL gates.
Problem: How many gates can one 9002 drive?



The output drive factor of the 9002 is 240/100. The input load factor of the 9946 is 2/9.4. Dividing the low level input load factor of the 9946 into the low level drive factor of the 9002 gives $\sim$ 10.5. Dividing the high level input load factor into the high level drive factor gives 120. Therefore, the fanout is limited to 10 by the low level load and drive factors.

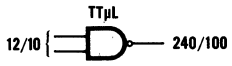
EXAMPLE 3:

4 DTμL 9946's in a wired-OR configuration.
Problem: How many TTμL 9002 inputs will the output drive?

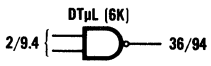


The output drive factor of the DTμL 9946 is 36/94. The output pull-up resistor is 6K, so 8 must be subtracted from the low level drive factor for each extra output tied together in the wired-OR configuration. With four outputs tied together, there are three excess pull-up resistors and 24 must be subtracted from 94 (the low level output drive factor of each 9946) to give an output low level drive factor of 70. The output high level drive is the sum of all the high level drive factors of the four 9946's. Thus the high level load factor of the combination is $36 + 36 + 36 + 36 = 144$. The 9002 inputs have load factors of 12/10, so it can be determined, as in previous examples, that the limiting factors are the low level drive and load factors and that the four gates in the wired-OR will drive seven 9002 inputs.

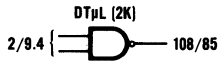
QUAD 2-INPUT NAND GATES



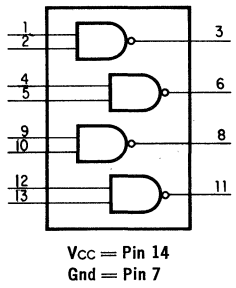
9002



9946

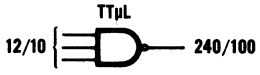


9949

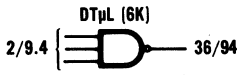


PIN CONFIGURATION

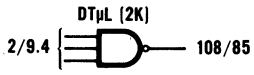
TRIPLE 3-INPUT NAND GATES



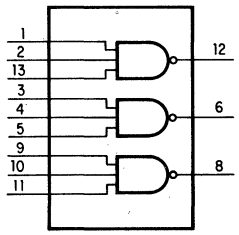
9003



9962

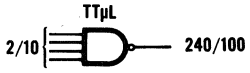


9963



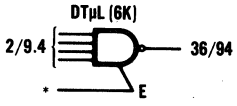
PIN CONFIGURATION

DUAL 4-INPUT NAND GATES

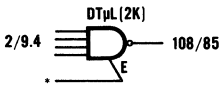


9004

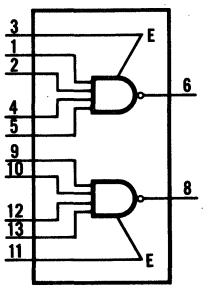
Extender Inputs, see note on Page 10



9930



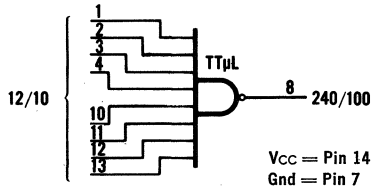
9961



Extenders are not present on 9004

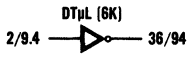
PIN CONFIGURATION

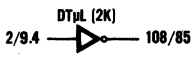
8-INPUT NAND GATE

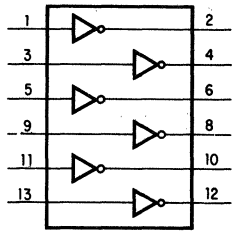


9007

HEX INVERTERS







9016

9935

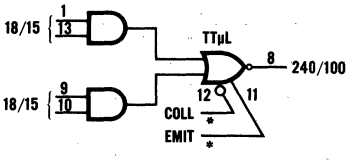
9937

Vcc = Pin 14
Gnd = Pin 7

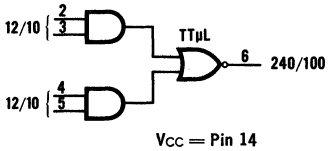
PIN CONFIGURATION

* Extender Inputs, see note on Page 10

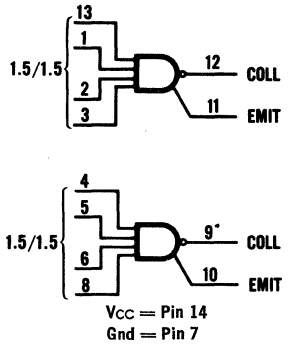
AND-OR-INVERT GATES AND EXTENDER



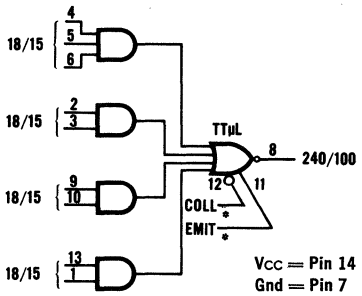
9005 EXTENDABLE HALF



9005 NONEXTENDABLE HALF

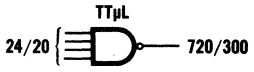


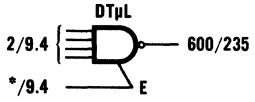
9006

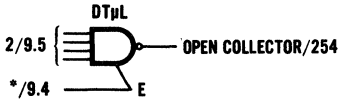


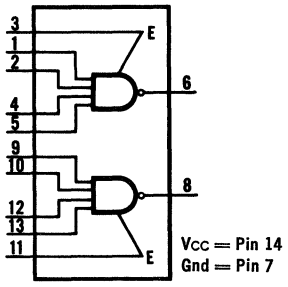
9008

DUAL 4-INPUT NAND BUFFERS









Extender inputs not present on 9009

9009

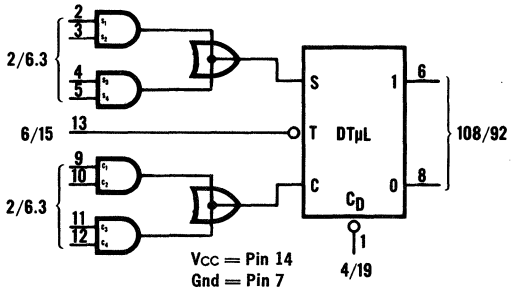
9932

9944

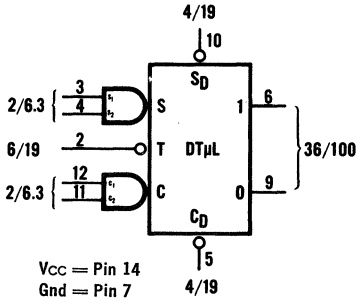
PIN CONFIGURATION

* Extender Inputs, see note on Page 10

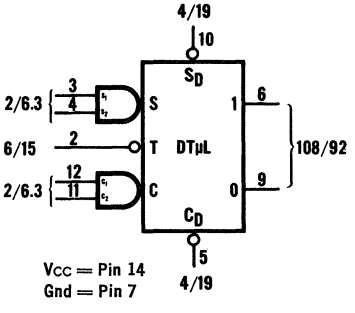
R-S FLIP-FLOPS



9111

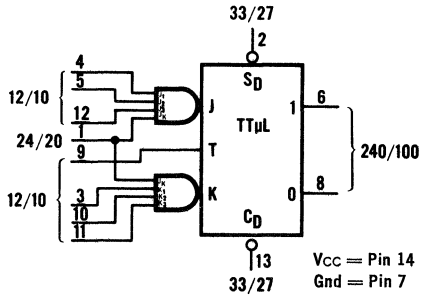


9945

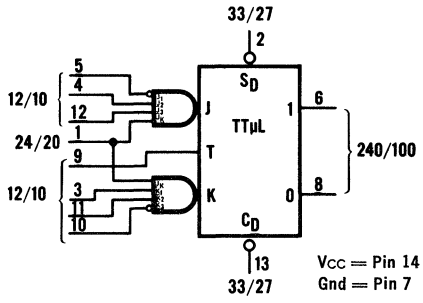


9948

J-K FLIP-FLOPS

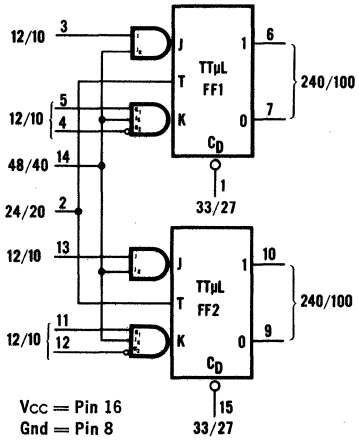


9000

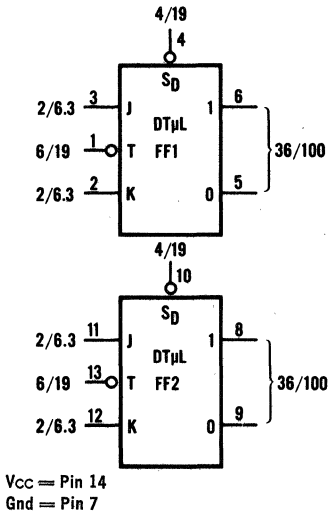


9001

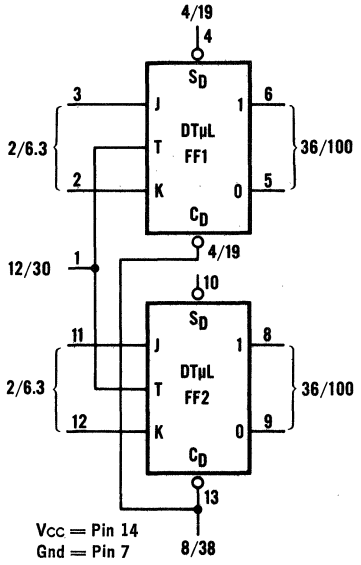
DUAL J-K FLIP-FLOPS



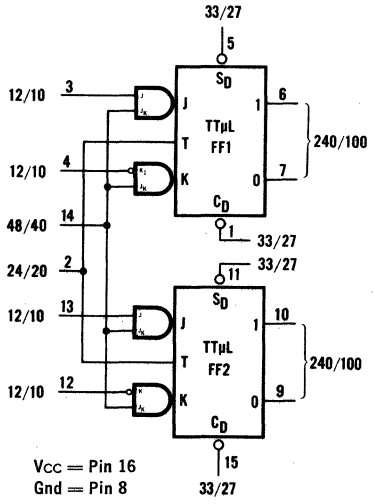
9020



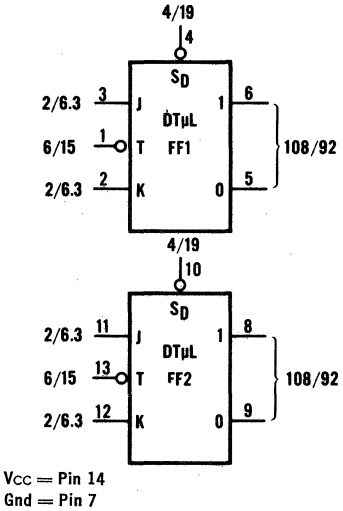
9093



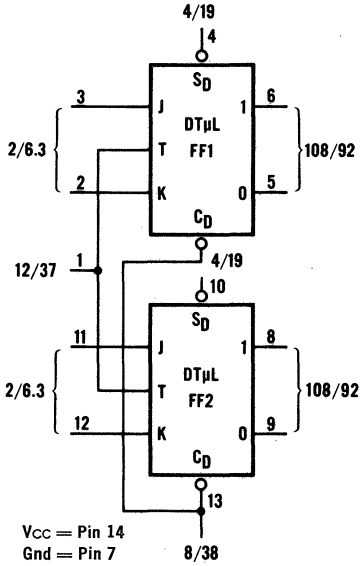
9097



9022

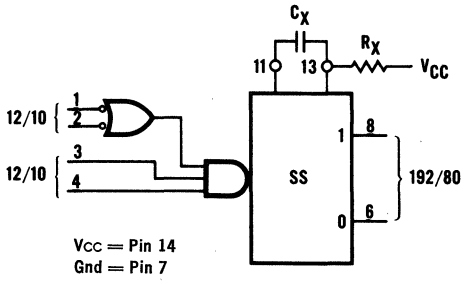


9094



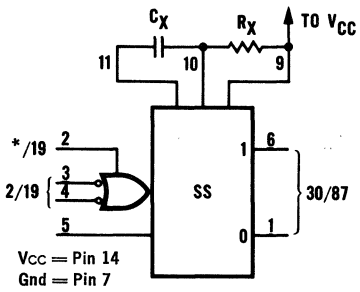
9099

MONOSTABLE MULTIVIBRATORS



V_{CC} = Pin 14
Gnd = Pin 7

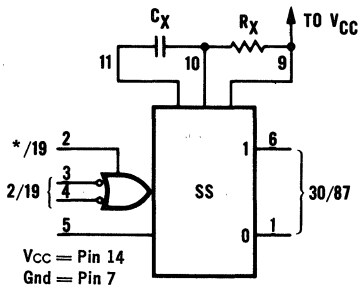
9601



V_{CC} = Pin 14
Gnd = Pin 7

The DTμL 9941 is NOT recommended for new designs; use the 9601.

9941



V_{CC} = Pin 14
Gnd = Pin 7

The DTμL 9951 is NOT recommended for new designs; use the 9601.

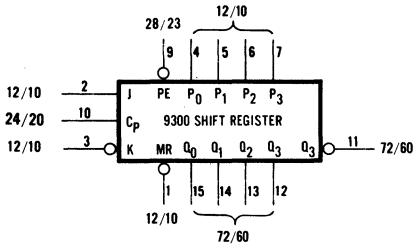
9951

NOTE: The maximum input fall time to trigger is: 25 ns for a 1.0 volt swing; 50 ns for a 2.0 volt swing; 100 ns for a 4.0 volt swing.

* Extender Inputs, see note on Page 10

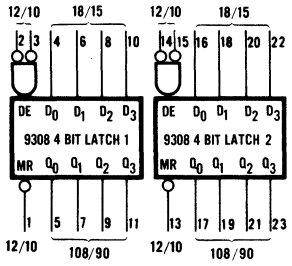
MEDIUM SCALE INTEGRATION

SHIFT REGISTERS AND STORAGE ELEMENTS



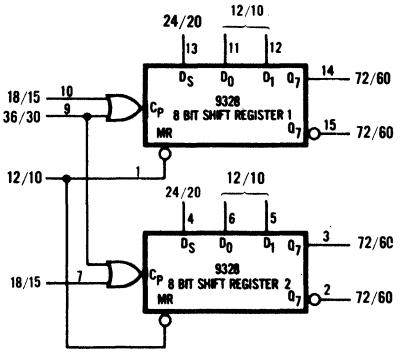
V_{CC} = Pin 16
Gnd = Pin 8

9300
4 BIT UNIVERSAL REGISTER



V_{CC} = Pin 24
Gnd = Pin 12

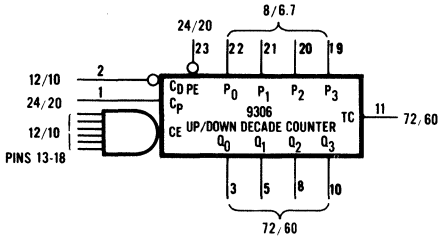
9308
DUAL 4 BIT LATCH



V_{CC} = Pin 16
Gnd = Pin 8

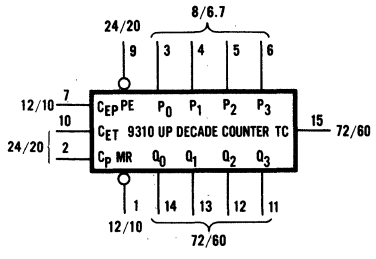
9328
DUAL 8 BIT SHIFT REGISTER

COUNTERS



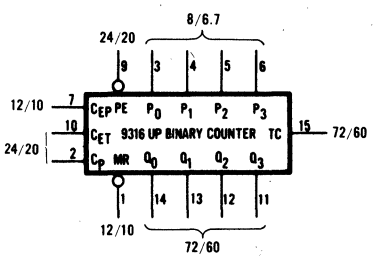
V_{CC} = Pin 24
Gnd = Pin 12

9306
UP/DOWN DECADE COUNTER



V_{CC} = Pin 16
Gnd = Pin 8

9310
UP DECADE COUNTER

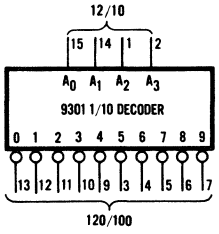


V_{CC} = Pin 16
Gnd = Pin 8

9316
UP BINARY COUNTER

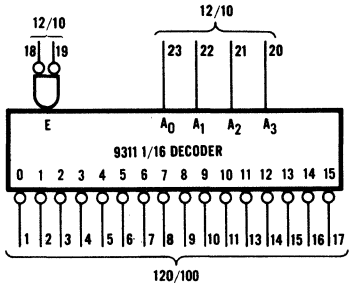
MEDIUM SCALE INTEGRATION (Cont'd.)

COMBINATIONAL LOGIC



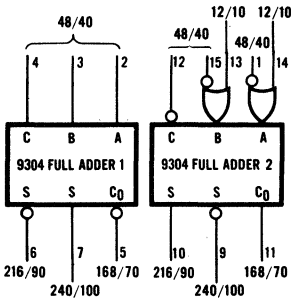
V_{CC} = Pin 16
Gnd = Pin 8

9301
1 OF 10 DECODER



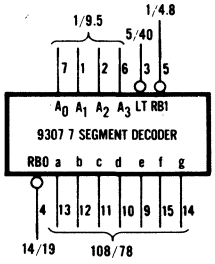
V_{CC} = Pin 24
Gnd = Pin 12

9311
1 OF 16 DECODER



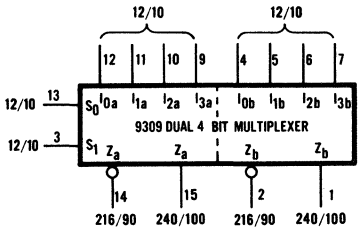
V_{CC} = Pin 16
Gnd = Pin 8

9304
DUAL FULL ADDER



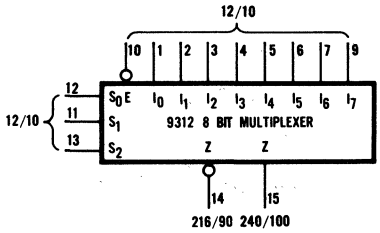
V_{CC} = Pin 16
Gnd = Pin 8

9307
BCD TO 7 SEGMENT DECODER



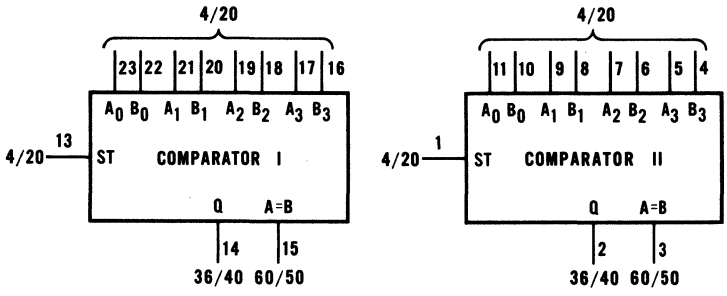
V_{CC} = Pin 16
Gnd = Pin 8

9309
DUAL 4 BIT MULTIPLEXER



V_{CC} = Pin 16
Gnd = Pin 8

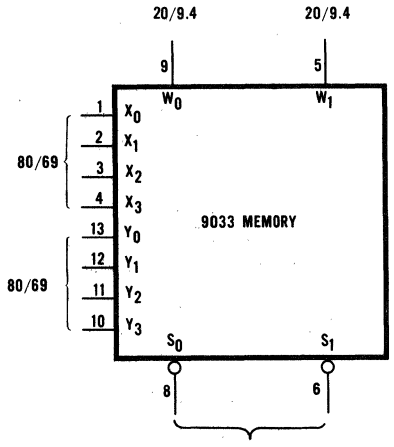
9312
8 BIT MULTIPLEXER



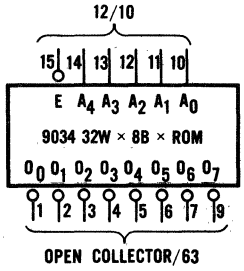
V_{CC} = Pin 24
Gnd = Pin 12

4510
DUAL 4 BIT COMPARATOR

MEMORIES



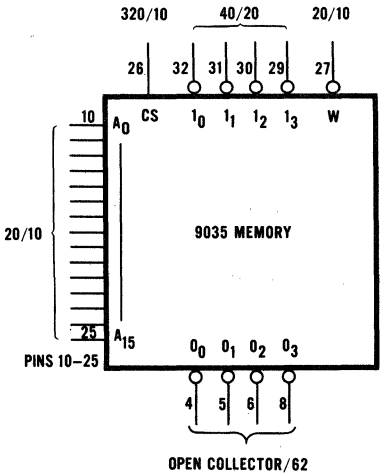
9033
16 Bit Scratch Pad Memory



V_{CC} = Pin 16
Gnd = Pin 8

NOTE: The 9034 is programmed on a custom basis. Contact your Fairchild salesman for more information.

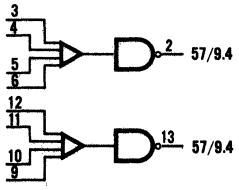
9034
32 Word by 8 Bit Read Only Memory



V_{CC} = Pin 28
Gnd = Pin 9

9035
64 Bit Read/Write Memory Cell

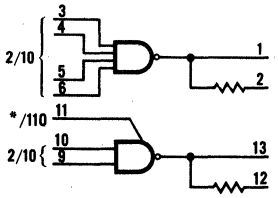
INTERFACE ELEMENTS



Inputs are differential, one pair attenuated, one pair nonattenuated.

V_{CC} = Pin 14
Gnd = Pin 7
+8 V = Pin 8

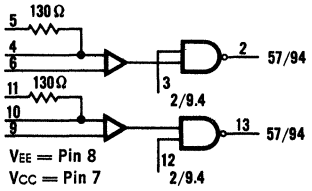
9620
Dual Differential Line Receiver



Outputs are extremely low impedance to drive long lines. Back matching resistors for 130 Ω line are provided.

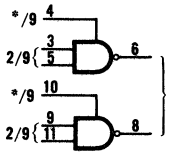
V_{CC} = Pin 14
Gnd = Pin 7
+8 V = Pin 8

9621
Dual Line Driver



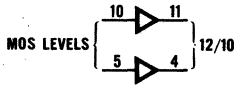
V_{EE} = Pin 8
V_{CC} = Pin 7
Gnd = Pin 14
S_3 = Pin 1
If S_3 = V_{CC}, then output is normally high with inputs open
If S_3 = Gnd 7, then output is normally low with inputs open

9622
Dual Differential Line Receiver (CCSL Threshhold Inputs)



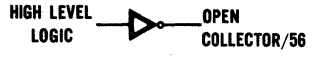
V_{CC} = Pin 14
V_{DD} = Pin 7
Gnd = Pin 1
T_{AP} = Pin 13

9624
CCSL to MOS Converter



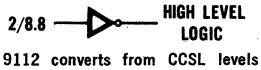
Gnd = Pin 1
V_{DD} = Pin 7
V_{CC} = Pin 14

9625
MOS to CCSL Converter



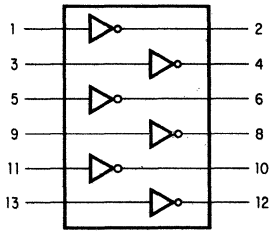
The 9109 converts from HLLDTμL levels (threshold ~ 7.5 Volts) to CCSL levels.

9109
Hex Converter



The 9112 converts from CCSL levels to HLLDTμL levels. (V_{OUT} ~ 12 to 20 Volts depending on V_{CC})

9112
Hex Converter



9112, 9109
PIN CONFIGURATION

EXTENDER INPUTS

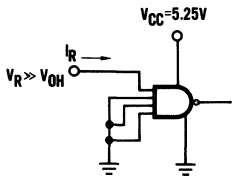
Extender inputs require DTμL 9933 or external silicon diodes in order to be used. Use of extender pins without diodes is not recommended. The low level load factor is determined by the resistor already included in the device. The high level load factor is usually negligible as most discrete silicon diodes have leakages of less than 1.0 μA at 75°C. A leakage of 1.0 μA corresponds to an input high level load factor of 0.2. The normalizing factor given in the introduction can always be used to determine the load factor of a diode. In order to maintain CCSL levels the diode should have <0.65 volt drop at 1.5 mA of current at 25°C.

APPENDIX

The purpose of this appendix is to cover in more detail the testing of CCSL products and thereby show how the logic levels are guaranteed. The testing must guarantee the input loading in both the high and low states and also must guarantee the output drive capability in both the high and low states. Both input and output characteristics must be guaranteed at worst case V_{CC} and input conditions and over the temperature range.

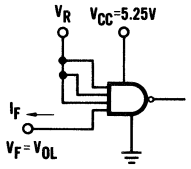
The examples given are for NAND gates. The application of the ideas to more complex devices is very much the same, except that manipulation of the inputs to achieve a required condition is more complex. Testing is always done with the worst case set of inputs.

First, consider the testing of the inputs to guarantee the input load factors. The high state input load current is tested by grounding the other inputs of the gate under test and measuring the input current with a voltage much higher than V_{OH}. Maximum V_{CC} is used as this has been found to be the worst case for TTμL circuits. The maximum allowed input high current is normalized to give the high level input load factor.



I_R TEST CIRCUIT

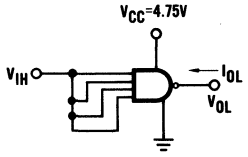
To test the low level input load factor, a voltage equal to V_{OL} is applied to one input and the current flowing out of the input is measured. The other inputs are tied to a high voltage. Maximum V_{CC} is used.



I_F TEST CIRCUIT

This maximum allowed input low current is normalized to give the low level input load factor.

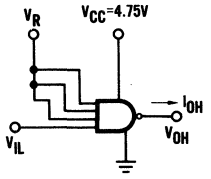
The output must be tested to insure that it meets the required high and low level drive factors, while maintaining the required noise immunity. To test the low level output drive factor, all inputs are maintained at V_{IH}, the minimum high level input voltage. The V_{CC} is maintained at 4.75 Volts and current is forced into the output. This current, I_{OL}, is related to the output low level drive factor by the normalizing factors for 4.75 Volts. The output voltage is measured to insure that it is less than V_{OL}.



I_{OL} TEST CIRCUIT

The test is repeated with $V_{CC} = 5.25$ Volts and the I_{OL} determined by the 5.25 Volts normalizing factor.

The output is then tested for the output high level drive factor. The maximum low level input voltage is applied to one input at a time with the other inputs held high. Current is then pulled out of the output. This current, I_{OH}, is related by normalizing factors to the output high level drive factor. The output voltage is measured to insure that it exceeds V_{OH}.



Each input is tested separately

I_{OH} TEST CIRCUIT

9300

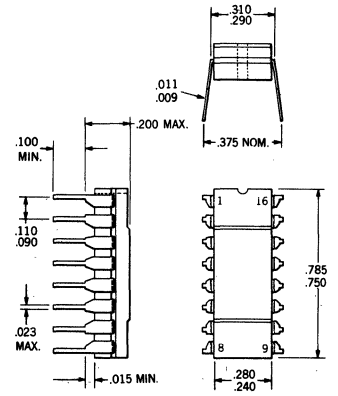
MSI 4-BIT SHIFT REGISTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9300 Four Bit Shift Register is a high speed multi-functional sequential logic block which is useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTμL for high speed and high fanout capability, and is compatible with all devices in the CCSL group of digital integrated circuits.

- **15 MHz shift frequency**
- **Synchronous parallel entry**
- **J, $\overline{K}$ inputs to first stage**
- **Asynchronous common reset**
- **Typical power dissipation of 300 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL, and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16 pin Dual In-Line package.**
- **Input diode clamping**

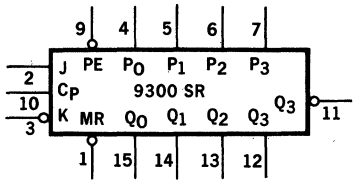
PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Figure 1

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

Figure 2

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION

Specify U6B9300XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FUNCTIONAL DESCRIPTION

The logic symbol of Figure 2 provides an indication of the functional characteristics of the 9300 four bit shift register. Several special logical features of the 9300 design which provide a high degree of general usefulness are described below:

1. A J$\overline{K}$ input is provided to the first flip flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for more general applications and at the same time the simple D type input that is most appropriate for a shift register can be easily obtained by simply tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logical operation — except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is low. With the Parallel Enable input low the element appears as four common clocked D flip flops. When the Parallel Enable is high, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip flops occurs after the low to high transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active high output is provided for all four stages and an active low output is provided for the last stage.
6. A master asynchronous clear input allows the setting to zero of all stages, independent of the condition of any other inputs.

TABLE I — TRUTH TABLE FOR SERIAL ENTRY
(PE = HIGH, MR = HIGH, (n + 1) indicates state after next clock)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II — LOADING RULES (1 U.L. = 1 TTμL Gate Input Load)

INPUTS	LOADING
J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3	1 U.L.
$\overline{PE}$	2.3 U.L.
C_P	4 U.L.
OUTPUTS	**FANOUT**
Q_0, Q_1, Q_2, Q_3 & $\overline{Q}_3$	6 U.L.

TABLE III
ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part #U6B930051X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 9.6 mA V_{CC} = 4.5 V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, K, MR, P_0, P_1, P_2 & P_3		−1.6 −1.24		−1.10 −0.97	−1.6 −1.24		−1.6 −1.24	mA mA	V_{CC} = 5.5 V V_{CC} = 4.5 V V_F = 0.4 V
I_R	Input Leakage Current* J, K, MR, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.5 V, V_R = 4.5 V

TABLE IV
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part #U6B930059X)

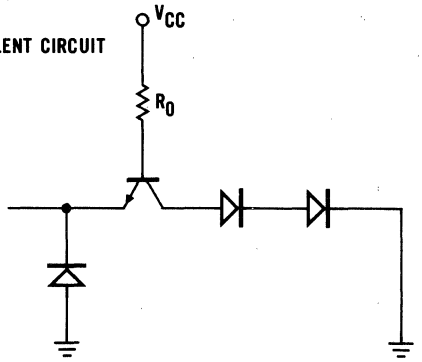
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 9.6 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	V_{CC} = 4.75 V, I_{OL} = 8.5 mA Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, $\overline{K}$, MR, P_0, P_1, P_2 & P_3		−1.6 −1.41		−1.0 −0.9	−1.6 −1.41		−1.6 −1.41	mA mA	V_{CC} = 5.25 V V_{CC} = 4.75 V, V_F = 0.45 V
I_R	Input Leakage Current* J, $\overline{K}$, MR, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V

*For CP and PE input currents, use load factors in Table II

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

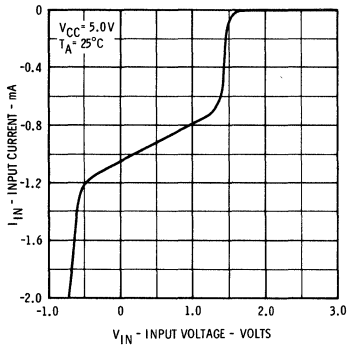
INPUTS

EQUIVALENT CIRCUIT

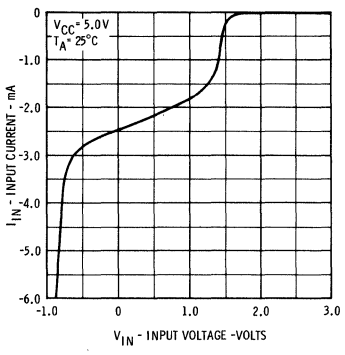


INPUT CURRENT VERSUS INPUT VOLTAGE

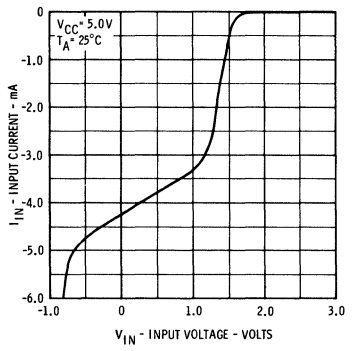
$\overline{MR}$, J, $\overline{K}$, P_0, P_1, P_2 & P_3



$\overline{PE}$

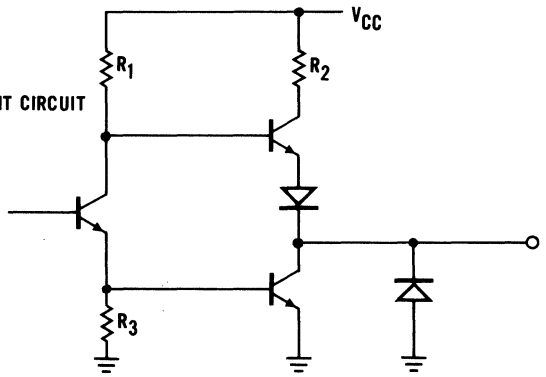


CP



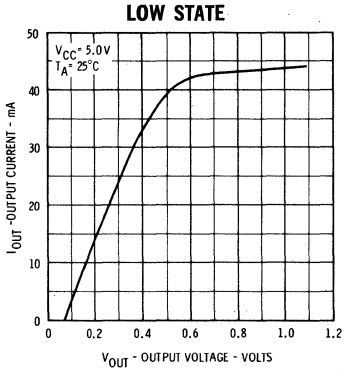
OUTPUTS

EQUIVALENT CIRCUIT

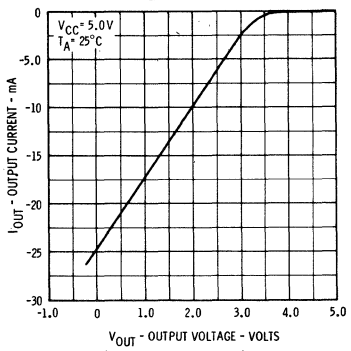


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE
(Q_0, Q_1, Q_2, Q_3 AND $\overline{Q}_3$)

LOW STATE



HIGH STATE



SWITCHING CHARACTERISTICS ($T_A = 25°C$) (Parts #U6B930051X and U6B930059X)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn Off Delay		20	35	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	Turn On Delay		25	45	ns	(See Fig. 5 & 6a)
f_{sr}	Shift Right Frequency	15	25		MHz	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 5 & 6c)
CP_{pw}	Clock Pulse Width	35	15		ns	
t_s	Set-up Time	35	17		ns	$V_{CC} = 5.0$ V
t_r	Release Time		16	0	ns	$C_L = 15$ pF
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$	45	26		ns	(See Figs. 6a & 6b)
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		25	10	ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		35		ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		20		ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		15		ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

RECOVERY TIME FOR $\overline{MR}$: $t_{rec}(\overline{MR})$ is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip-flop(s) to respond to the clock.

Figure 3
PROPAGATION DELAY — CLOCK TO Q_3 OR $\overline{Q}_3$ OUTPUT VS TEMPERATURE

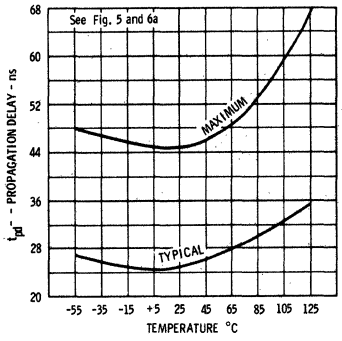
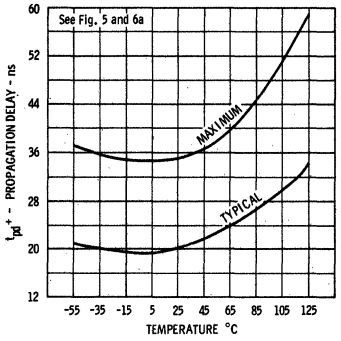
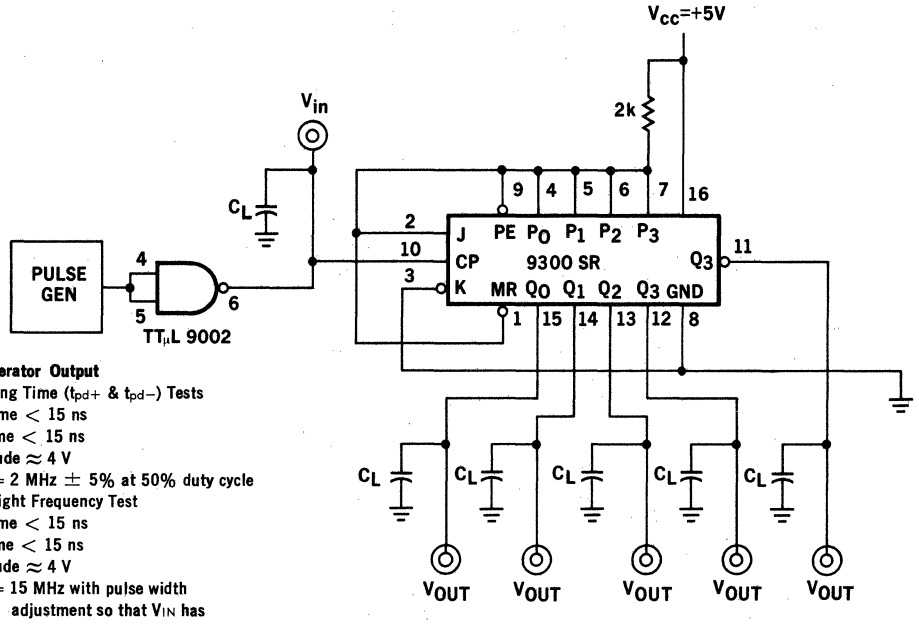


Figure 4
PROPAGATION DELAY — CLOCK TO Q_3 OR $\overline{Q}_3$ OUTPUT VS TEMPERATURE





Pulse Generator Output
1. Switching Time (t_{pd+} & t_{pd-}) Tests
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 2 MHz ± 5% at 50% duty cycle
2. Shift Right Frequency Test
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 15 MHz with pulse width adjustment so that V_{IN} has duty cycle of approx. 50%.

C_L includes probe and jig capacitance

Figure 5 — SWITCHING TIME & SHIFT RIGHT FREQUENCY TEST CIRCUIT

Fig. 6a

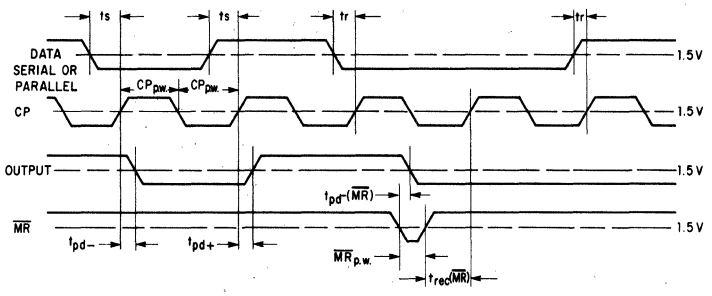


Fig. 6b

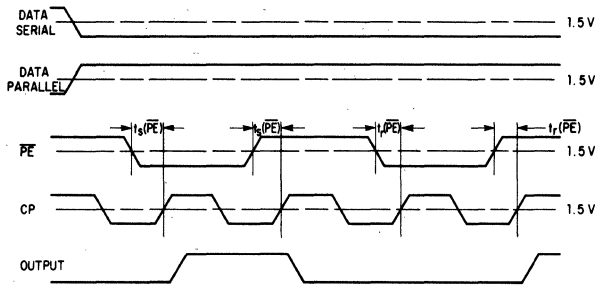
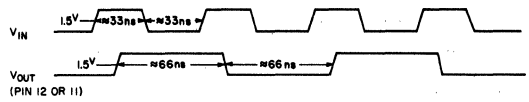


Fig. 6c



VOUT Frequency = ½ X VIN Frequency

Figure 6 — SWITCHING TIME & SHIFT RIGHT FREQUENCY WAVEFORMS

APPLICATIONS — The 9300 has been designed to be useful in a wide variety of applications. The multifunctional capability of the Fairchild 9300 is illustrated by the applications shown below.

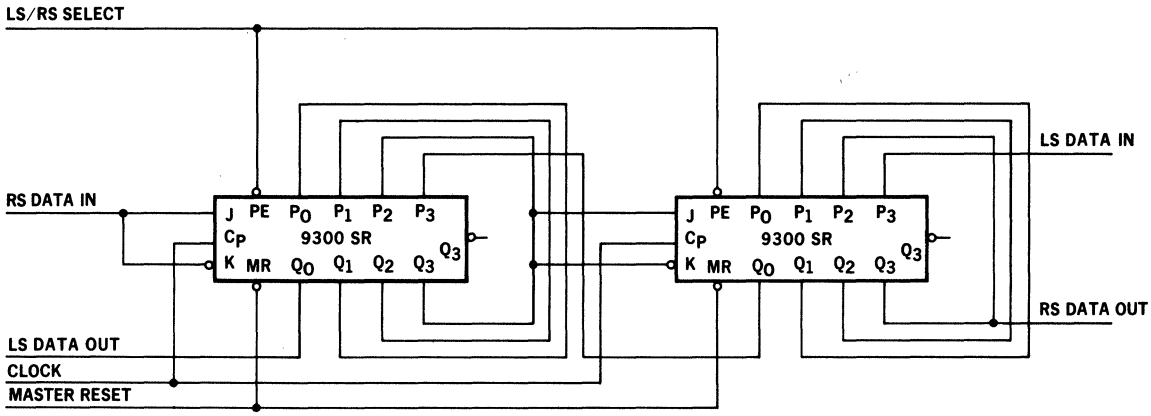


Figure 7 — EIGHT BIT LEFT/RIGHT SHIFT REGISTER

This register shifts Left or Right on each shift clock, depending upon the condition of the LS/RS SELECT input. If this input is high, Right Shift occurs and if low, Left Shift occurs.

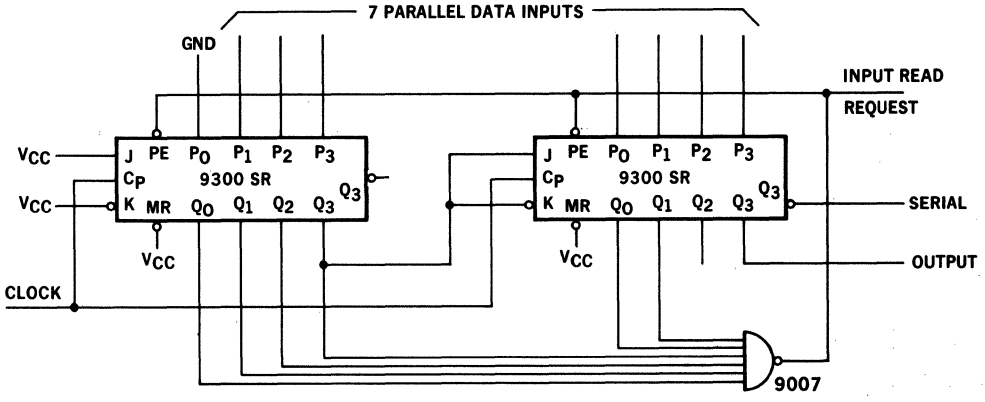


Figure 8 — SEVEN BIT PARALLEL TO SERIAL CONVERTER

This parallel to serial converter uses a marker bit, to count the data bits shifted out, so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.

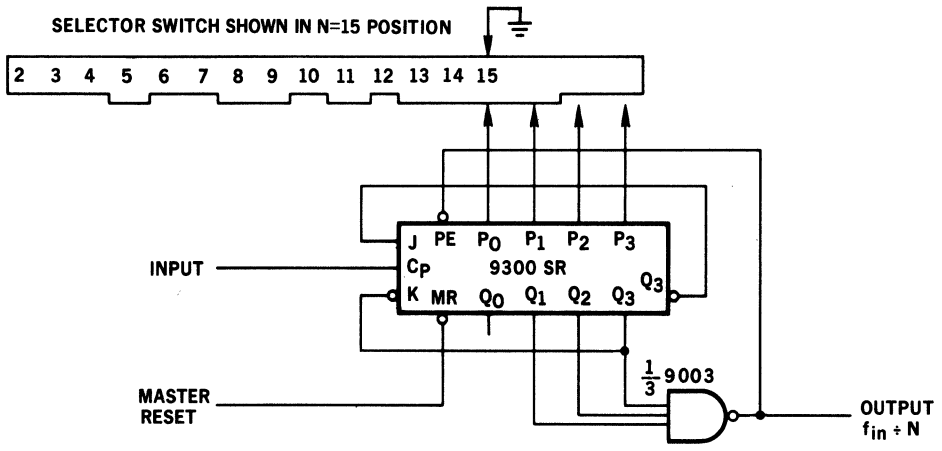
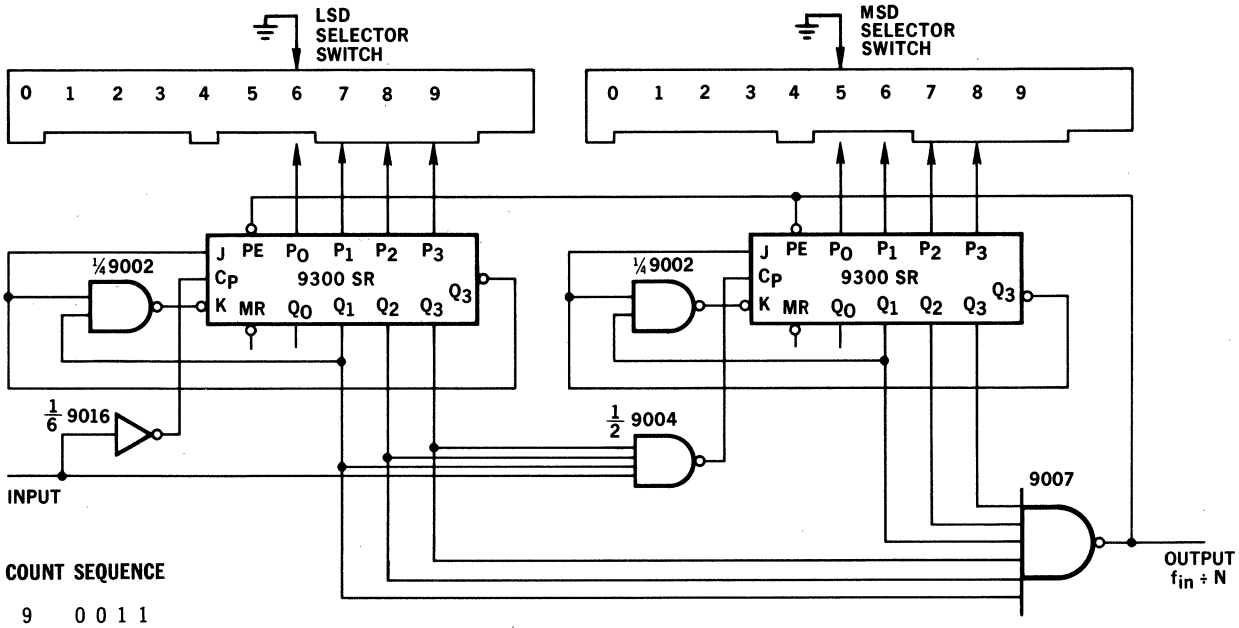


Figure 9 — DIVIDE BY N COUNTER FOR N = 2 to 15

This counter produces an output pulse for every N input pulses, where the number N is determined by the setting of the slide selector switch as shown or by logic inputs to the parallel data lines from an external source.



COUNT SEQUENCE

9	0 0 1 1
8	0 0 0 1
7	0 0 0 0
6	1 0 0 0
5	1 1 0 0
4	0 1 1 0
3	1 0 1 1
2	1 1 0 1
1	1 1 1 0
0	0 1 1 1

Figure 10 — TWO DECADE PROGRAMMABLE DIVIDER

This circuit divides by any number "N" from 1 to 100. The selected N is one greater than is shown on the slide switches. As an example the switches are showing 56, therefore the circuit will divide by 57 with this setting.

9301

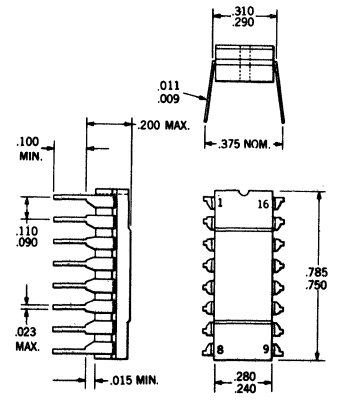
MSI ONE-OF-TEN DECODER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9301 is a multipurpose decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTμL for high speed and high fan out capability, and is compatible with all members of the CCSL group of digital integrated circuits.

- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTμL loads over the full temperature range and supply voltage ranges**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 145 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line* package**
- **Input clamp diodes limit high speed line termination effects**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

Fig. 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC SYMBOL

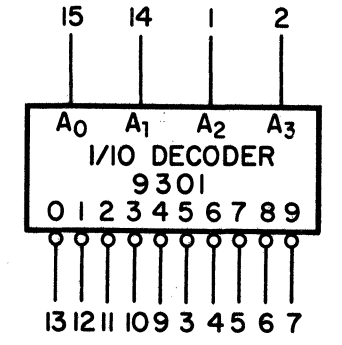


Fig. 2

ORDER INFORMATION

Specify U6B9301XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FUNCTIONAL DESCRIPTION

The 9301 Decoder accepts four active high BCD inputs and provides ten mutually exclusive active low outputs, as shown by Figure 2. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.

The logic design of the 9301 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the 9301 is used as a 1 out of 8 decoder. This is illustrated in the 1 out of 32 decoder shown in Figure 9.

The Truth Table and Loading Rules for the 9301 are shown in Table I and Table II.

TABLE I — TRUTH TABLE

A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —

LOADING RULES (1 U.L. = TTμL Gate Input Load)

INPUTS	LOADING
A_0, A_1, A_2 & A_3	1 U.L.

OUTPUTS	FANOUT
0, 1, 2, 3, 4, 5, 6, 7, 8, & 9	10 U.L.

TABLE III —

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930151X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay Input to Output				20	30			ns	$C_L = 15\ pF$ See Fig. 8

TABLE IV —

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part #U6B930159X)

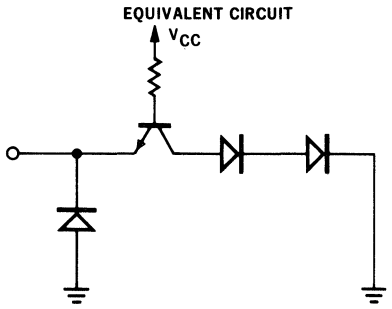
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.6 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16.0 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
			−1.41		−0.9	−1.41		−1.41	mA	V_{CC} = 4.75 V, V_F = 0.45 V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	V_{CC} = 5.0 V
t_{pd-}	Turn On Delay				20	30			ns	C_L = 15 pF See Fig. 8

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Fig. 3

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

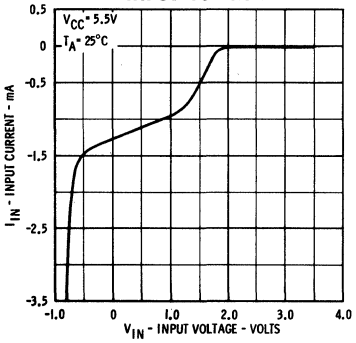
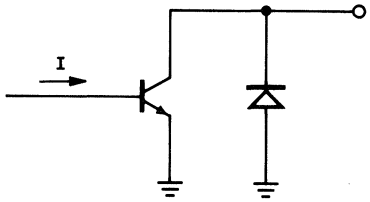


Fig. 4

OUTPUTS

EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

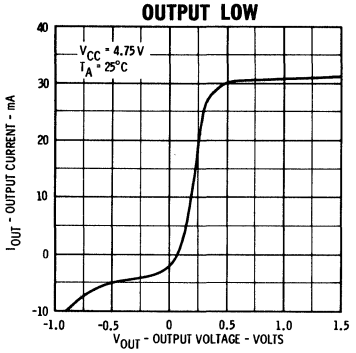
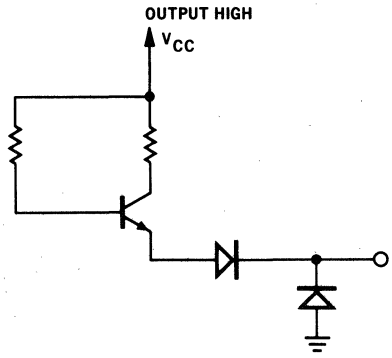
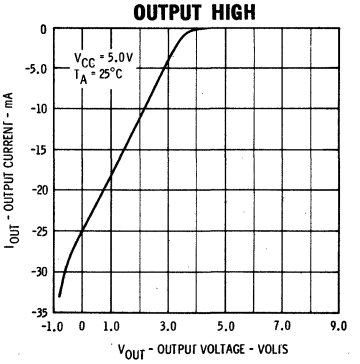


Fig. 5

OUTPUT HIGH



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH



SWITCHING PERFORMANCE

Fig. 6

TYPICAL TURN ON DELAY VERSUS TEMPERATURE

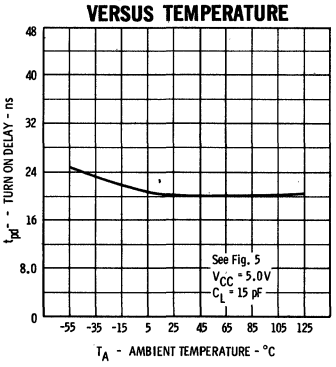
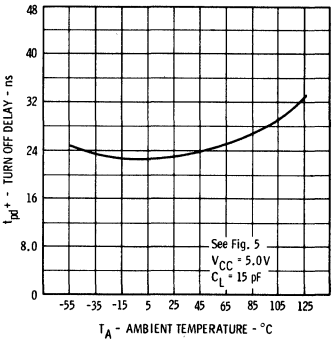
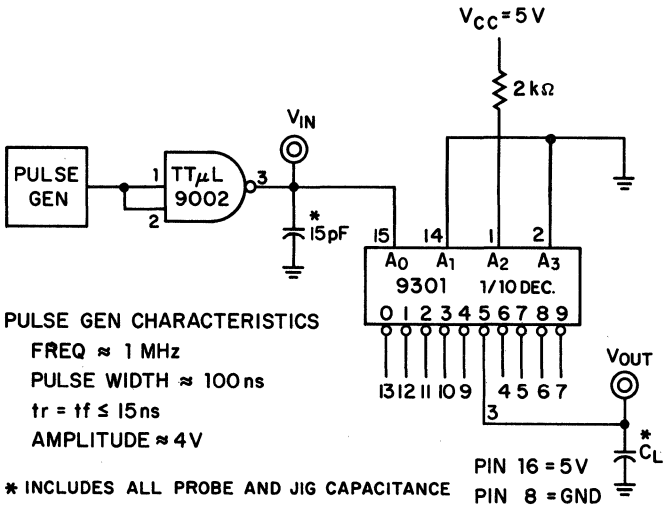


Fig. 7

TYPICAL TURN OFF DELAY VERSUS TEMPERATURE





PULSE GEN CHARACTERISTICS
- FREQ ≈ 1 MHz
- PULSE WIDTH ≈ 100 ns
- tr = tf ≤ 15 ns
- AMPLITUDE ≈ 4 V

* INCLUDES ALL PROBE AND JIG CAPACITANCE

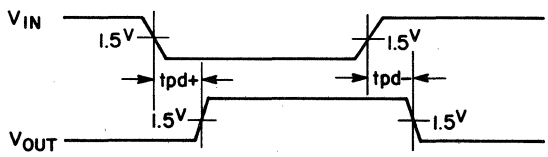


Fig. 8 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The 9301 decoder may be used for BCD to Decimal or 3 bit binary to octal conversion as well as many other applications. The general purpose nature of the 9301 is indicated by its use in the following applications.

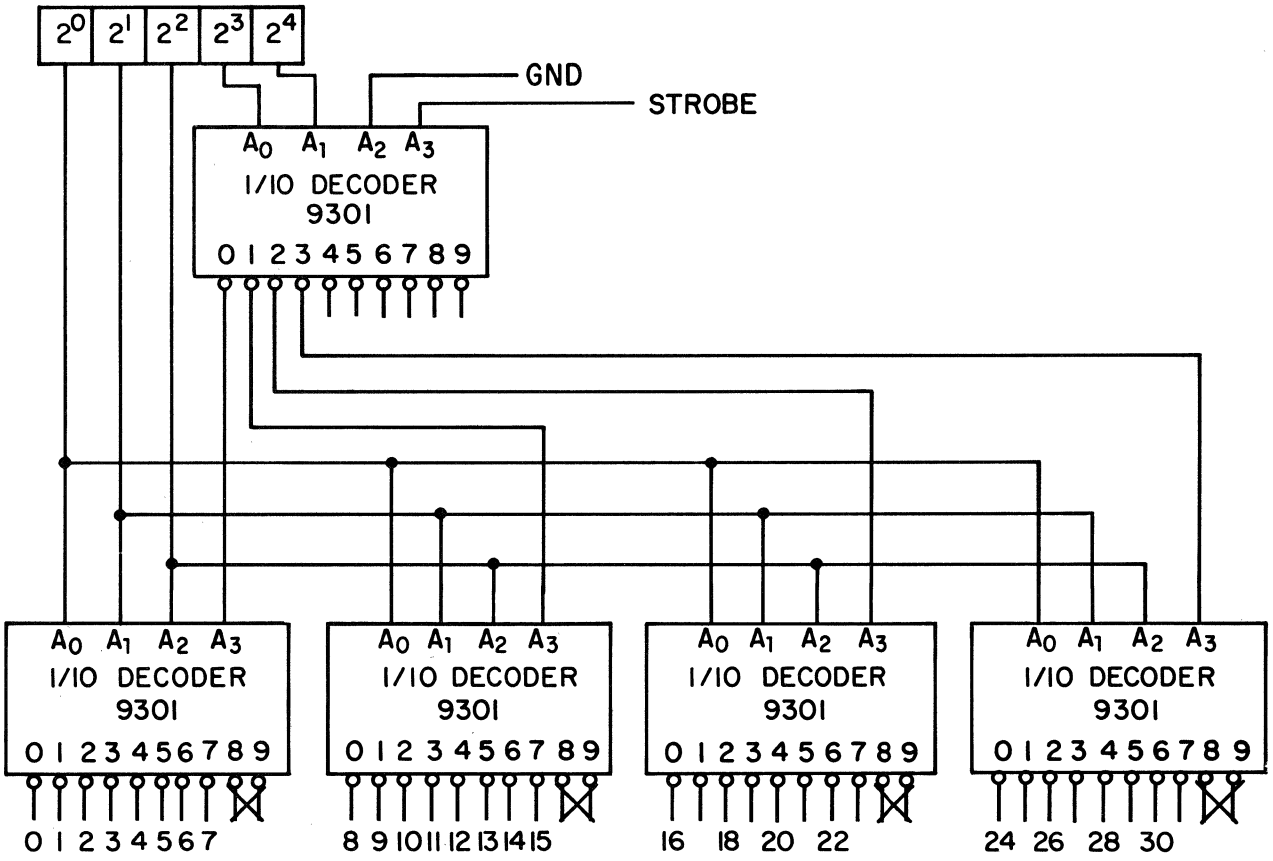
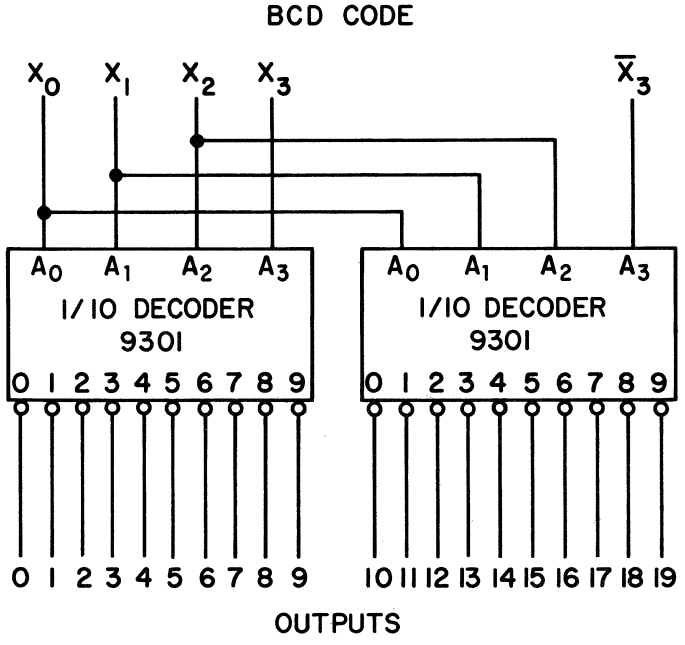


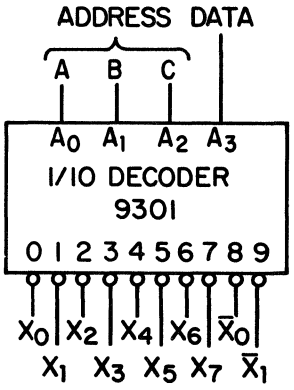
Fig. 9 — ONE-OUT-OF-THIRTY-TWO DECODING



DECIMAL DIGIT	OUTPUT SELECTION BCD CODE 8421	5421	EXCESS 3	4221
0	0, 18	0, 18	3	0, 18
1	1, 19	1, 19	4	1, 19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8, 10	8, 10	9, 11
6	6	9, 11	9, 11	14
7	7	12	12	15
8	8, 10	13	13	16
9	9, 11	14	14	17

Decode any BCD code using two 9301 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

Fig. 10 — DECODE ANY BCD CODE

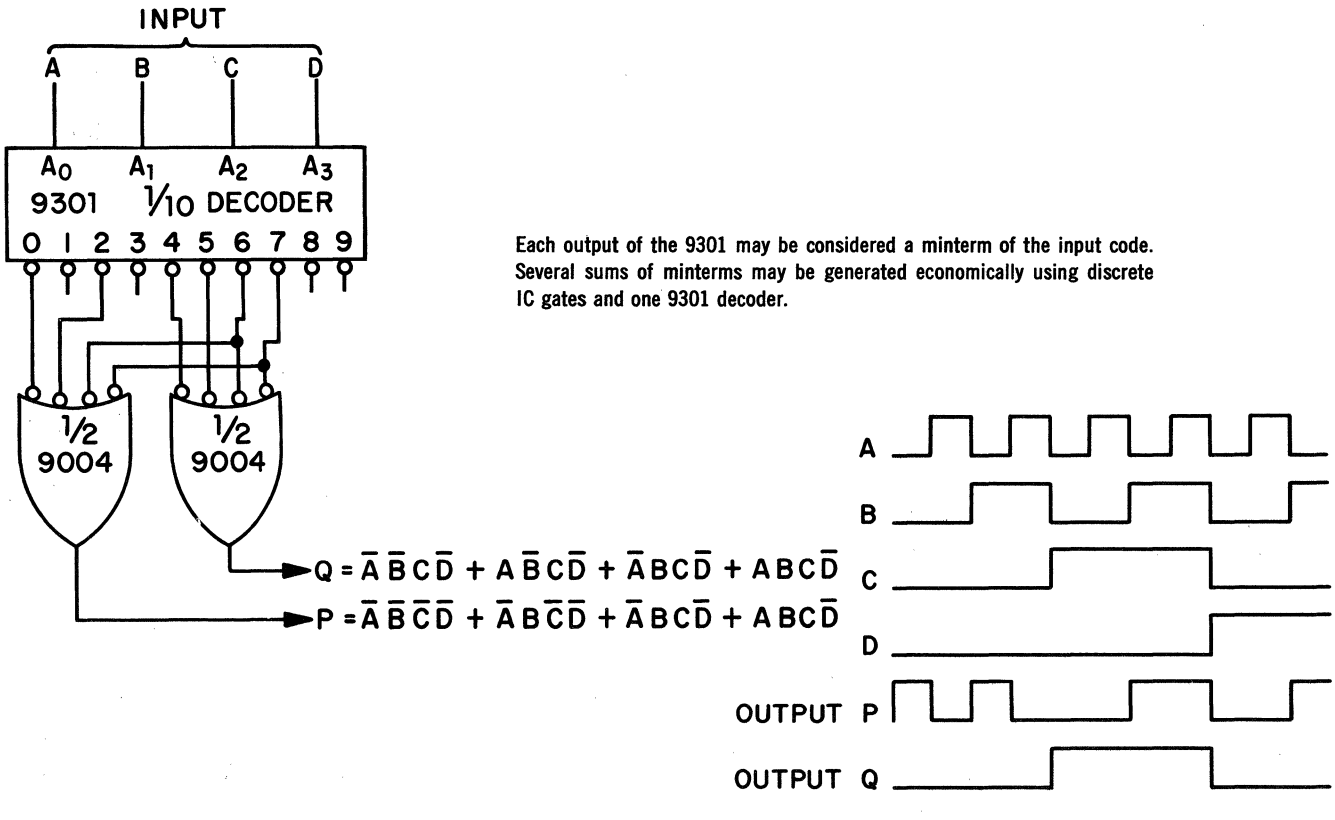


ADDRESS			OUTPUT LINE
A	B	C	
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Data may be routed from a source to any of 8 outputs by addressing that output.
All non-addressed outputs remain high.

Complements of outputs 0 and 1 are available at outputs 8 and 9 respectively.

Fig. 11— DIGITAL DEMULTIPLEXER



Each output of the 9301 may be considered a minterm of the input code. Several sums of minterms may be generated economically using discrete IC gates and one 9301 decoder.

Fig. 12— MINTERM GENERATOR

9304

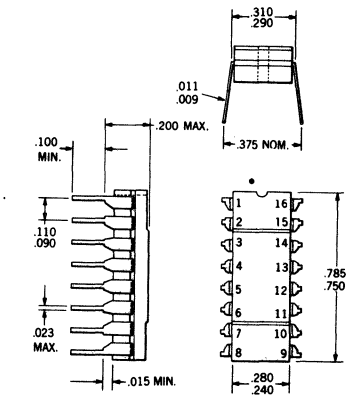
MSI DUAL FULL ADDER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9304 consists of two independent, high speed, binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion, and majority gating. The circuit uses TTμL for high speed, high fanout operation and is compatible with all members of the CCSL group of digital integrated circuits.

- **Multi-function capability**
- **8ns carry propagation delay**
- **Complementary inputs and outputs available**
- **Typical power dissipation of 150 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line* package**
- **Input clamp diodes limit high speed termination effects**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

LOGIC SYMBOL

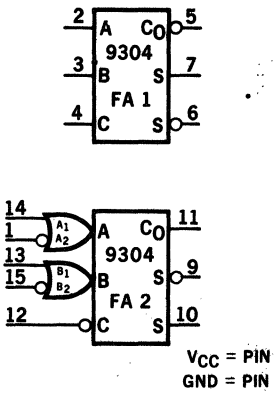


Fig. 2

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION

Specify U6B9304XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

FUNCTIONAL DESCRIPTION

The Fairchild 9304 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active high or active low inputs at the A and B terminals. The adders produce a low carry and both low and high sum with active high inputs, a high carry and both high and low sum when active low inputs are used. This principle of duality is shown in Figure 12, where the adders are drawn as functional blocks.

The Truth Table and Loading Rules for the 9304 are shown in Table I and Table II.

TABLE I — TRUTH TABLES

ADDER 1					
INPUTS			OUTPUTS		
C	B	A	$\overline{C}_O$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

ADDER 2							
INPUTS					OUTPUTS		
$\overline{C}$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_O	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —

LOADING RULES (1 U.L. = TTμL Gate Input Unit Load)

INPUTS		LOADING
FA 1	A, B & C	4 U.L.
FA 2	$\overline{A}_2$, $\overline{B}_2$ & $\overline{C}$	4 U.L.
	A_1 & B_1	1 U.L.

OUTPUTS		FANOUT
FA 1	$\overline{C}_O$	7 U.L.
	$\overline{S}$	9 U.L.
	S	10 U.L.
FA 2	C_O	7 U.L.
	S	9 U.L.
	$\overline{S}$	10 U.L.

TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930451X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.5\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.5\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.5\ V$, $I_{OL} = 12.4$ mA (Pins 7 & 9) $I_{OL} = 11.2$ mA (Pins 6 & 10) $I_{OL} = 8.7$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
4 I_F	Input Load Current		−6.4		−4.4	−6.4		−6.4		
I_F	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
4 I_F	Input Load Current		−4.96		−3.88	−4.96		−4.96		
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$ Ground on other inputs
4 I_R	Input Leakage Current				60	240		240		
t_{pd+}	C to C_O				8	13			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Fig. 11
t_{pd-}	C to C_O				8	13			ns	
t_{pd+}	A_i to $\overline{S}$				28	40			ns	
t_{pd-}	A_i to $\overline{S}$				25	35			ns	

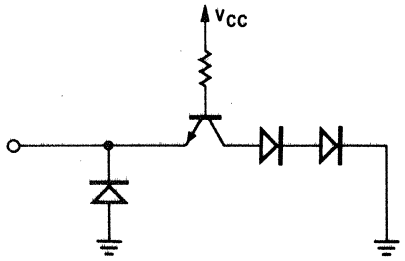
TABLE IV —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U6B930459X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.75\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.75\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.75\ V$, $I_{OL} = 14.1$ mA (Pins 7 & 9) $I_{OL} = 12.7$ mA (Pins 6 & 10) $I_{OL} = 9.85$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
4 I_F	Input Load Current		−6.4		−4.0	−6.4		−6.4		
I_F	Input Load Current		−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
4 I_F	Input Load Current		−5.64		−3.6	−5.64		−5.64		
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$ Ground on other inputs
4 I_R	Input Leakage Current				60	240		240		
t_{pd+}	C to C_O				8.0	15			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Fig. 11
t_{pd-}	C to C_O				8.0	15			ns	
t_{pd+}	A_i to $\overline{S}$				28	45			ns	
t_{pd-}	A_i to $\overline{S}$				25	40			ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VS INPUT VOLTAGE

FIG. 3 PINS 1, 2, 3, 4, 12, 15

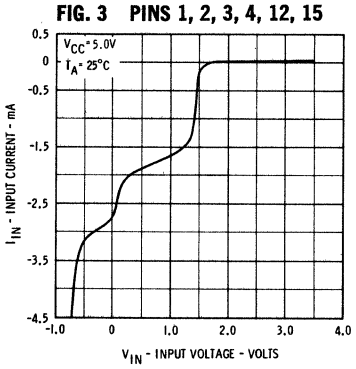
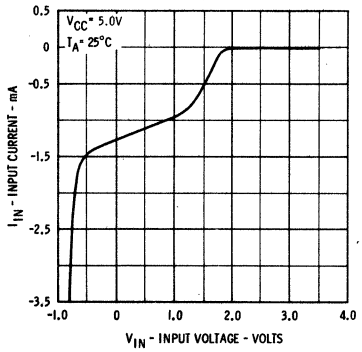
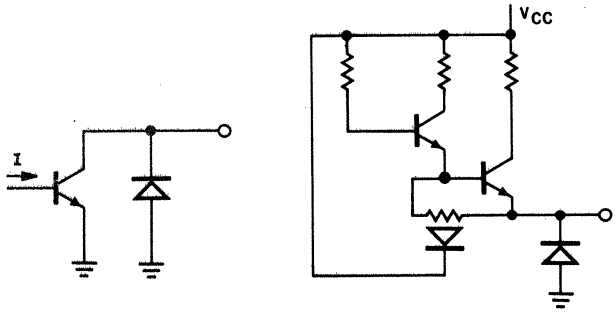


FIG. 4 PINS 13, 14



OUTPUTS

LOW STATE HIGH STATE



OUTPUT CURRENT VS OUTPUT VOLTAGE

FIG. 5 LOW STATE

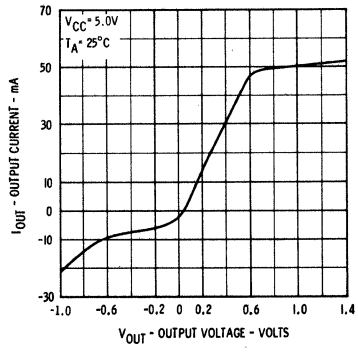


FIG. 6 HIGH STATE

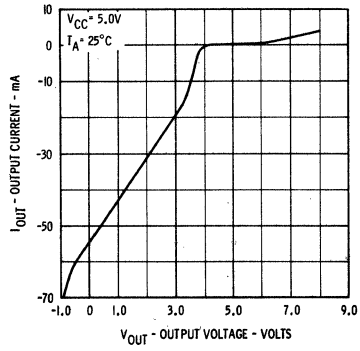


Fig. 7
TYPICAL CARRY TURN ON DELAY TIME VERSUS TEMPERATURE

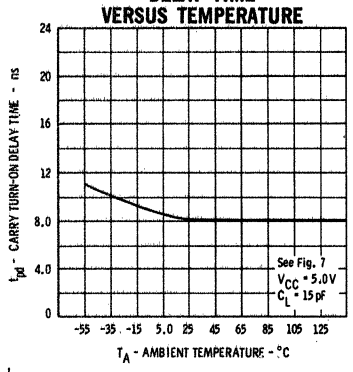


Fig. 8
TYPICAL CARRY TURN OFF DELAY TIME VERSUS TEMPERATURE

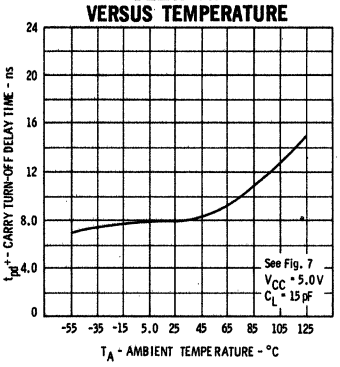


Fig. 9
TYPICAL ADD TURN ON DELAY TIME VERSUS TEMPERATURE

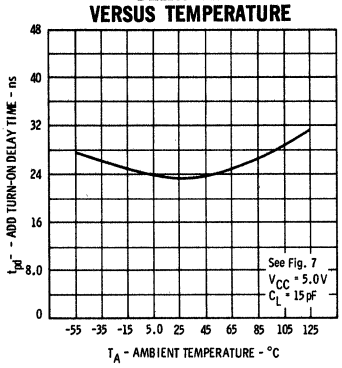
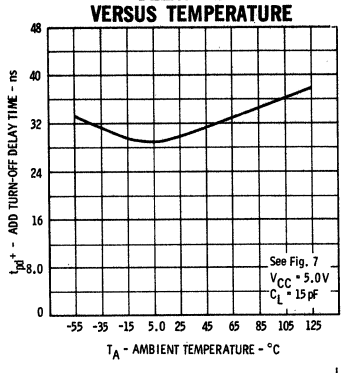
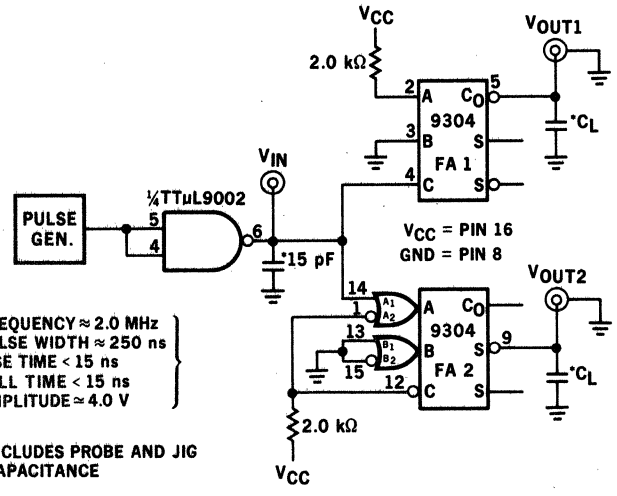


Fig. 10
TYPICAL ADD TURN OFF DELAY TIME VERSUS TEMPERATURE





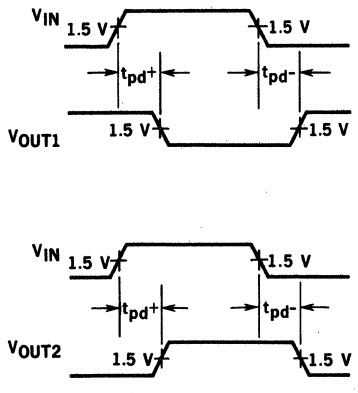


Fig.11— SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The 9304 dual adder has been designed to be useful in a wide variety of applications such as addition, parity generation and checking, code conversion, majority gating and other applications for which this combination of logic gates may be useful. The multifunctional capabilities of the Fairchild dual adder can be seen from reference to the applications shown.

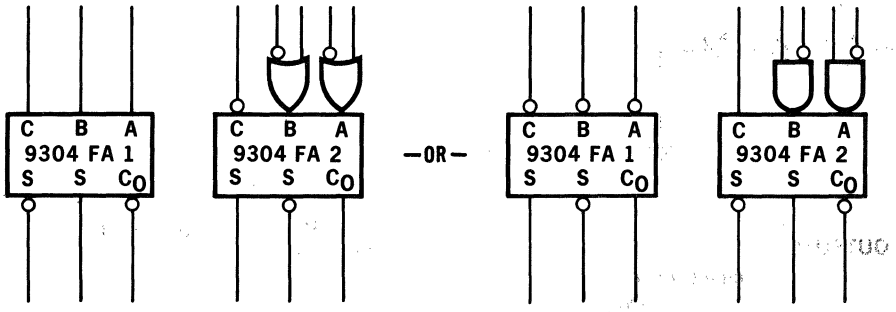


Fig.12— FUNCTIONAL BLOCK REPRESENTATION

The principle of duality allows 2 ways of representing each adder. The circuit is the same in both cases but the logic diagrams differ. The dual diagrams facilitate logic design and allow a greater understanding of the capabilities of the device.

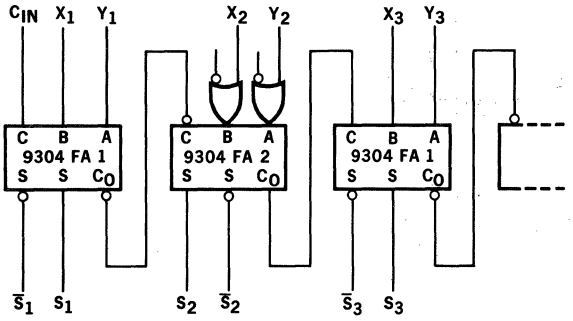


Fig.13— RIPPLE CARRY PARALLEL ADDITION

Shown above is a high speed ripple carry parallel addition scheme. Only one and-or-not gate relay is incurred at each stage allowing a typical addition speed of (N+1) x 8 ns, where N is the number of bits in the word. A similar scheme will work if the negation inputs are used, and the design acts as a subtractor when the complement of one variable is provided.

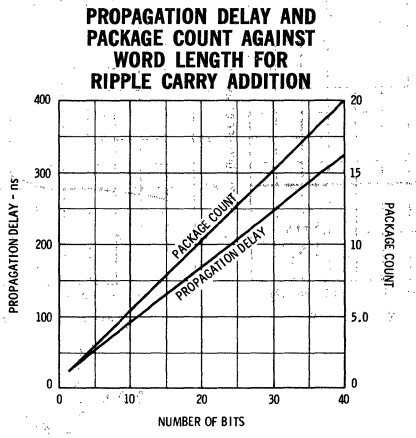


Fig. 14

The curve shows propagation delay of the ripple Carry Adder drawn in Figure 5. Plotted on the same diagram is a curve showing the low package count resulting from this Ripple Scheme.

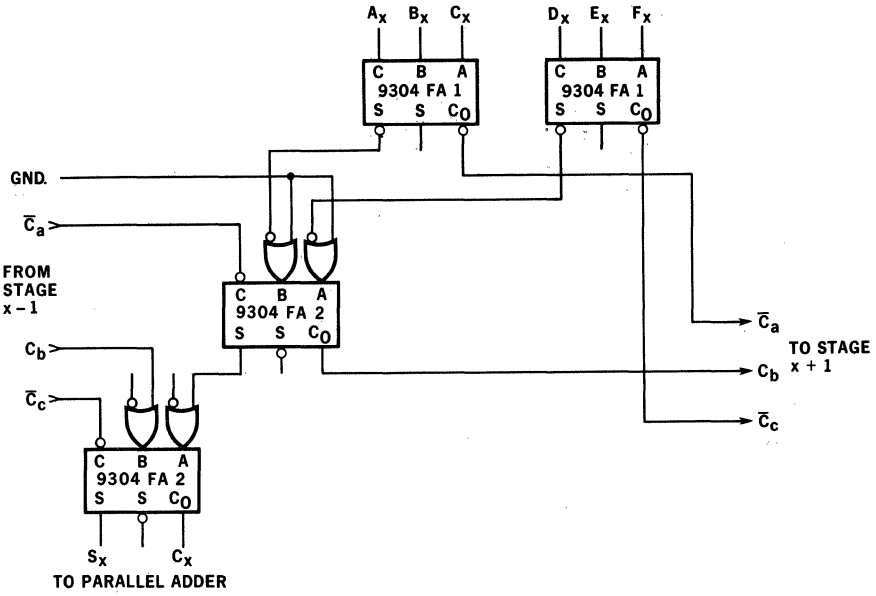


Fig. 15 — ADDITION OF SIX VARIABLES

The above design shows how the 9304 can be used in carry save arithmetic. Six input variable are reduced to two where they can be added in a parallel adder. Delay between inputs and outputs is typically 50 ns, allowing extremely high speed computation. Additional variables may be added or the concept can be extended to multiplication, division, and various other arithmetic operations.

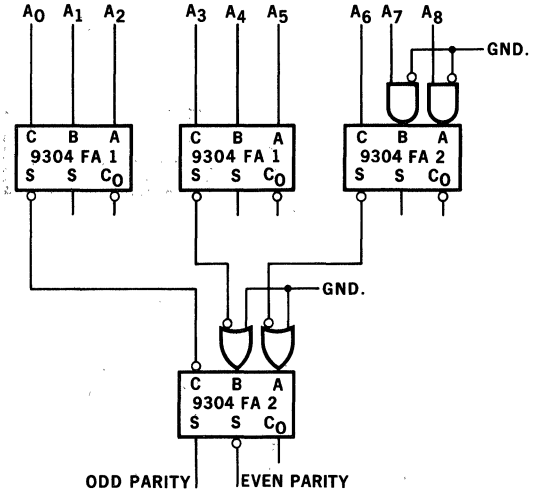


Fig. 16 — BYTE PARITY GENERATION OR CHECKING

The 9304 can be used for parity checking or generating. The above design uses 2 9304's to generate parity for an 8 bit byte or check parity over 9 bits. The delay from input to odd parity is typically 35 ns. Additional adder blocks can be used to generate or check parity over larger word lengths. The concept can also be used for hamming and cyclic code generation and checking.

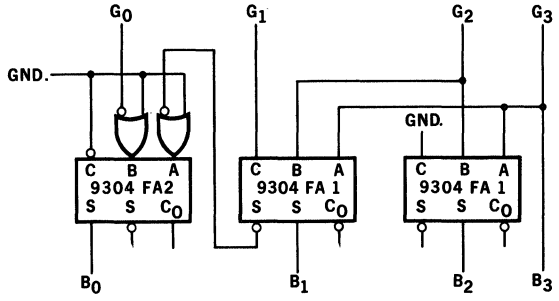


Fig. 17 — 4 BIT PARALLEL GRAY TO BINARY CONVERSION

A 4 bit parallel binary to gray conversion is shown. The adders can also be used for other cyclic code manipulations.

9306

MSI UP/DOWN BCD COUNTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9306 is a high speed synchronous 8421 BCD up/down decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Seven decades of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES:

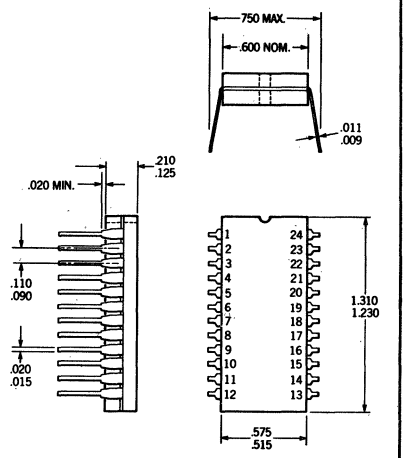
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY/BORROW CIRCUITRY**
- **TYPICAL POWER DISSIPATION OF 350 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC HERMETIC 24 PIN DUAL IN-LINE PACKAGE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

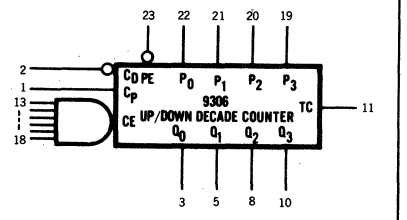
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify U6N9306XXX for 24-pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



V_{CC} — Pin 24
Gnd — Pin 12

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FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Mode selection is accomplished as shown in the table below. However, several restrictions are placed on the manner of selection. First, the transition of CE from high to low or of PE from low to high may only be done when CP is high. Second, any change of CD must be done only when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics."

MODE SELECTION SCHEME

PE	CD	CE	Mode
0	0	0	presetting
0	0	1	presetting
0	1	0	presetting
0	1	1	presetting
1	1	1	count up
1	0	1	count down
1	1	0	no change
1	0	0	no change

Note: $CE = CE_0 \cdot CE_1 \cdot CE_2 \cdot CE_3 \cdot CE_4 \cdot CE_5$

LOADING RULES
(1 U.L. = 1 TTμL input gate load)

INPUT	FAN IN
CD, CE_0, CE_1, CE_2,	1 Unit Load
CE_3, CE_4, CE_5	1 Unit Load
CP, PE	2 Unit Loads
P_0, P_1, P_2, P_3	⅔ Unit Load
OUTPUT	**FAN OUT**
Q_0, Q_1, Q_2, Q_3, TC	6 Unit Loads

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 7.44\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_1, E_2, E_3, E_4, E_5, CD		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−.7	−1.07		−1.07	mA	
I_R	Input Leakage Current E_0, E_1, E_2, E_3, E_4, E_5, CD		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE		120		20	120		120	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7	40		40	μA	

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$ Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $E_0, E_1, E_2, E_3, E_4, E_5, CD$		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−.7	−1.07		−1.07	mA	
I_R	Input Leakage Current $E_0, E_1, E_2, E_3, E_4, E_5, CD$		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE		120		20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7	40		40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		20		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		40		ns	
t_{pd-} (TC)	Turn-On Delay for TC		30		ns	
t_s (CE)	Set-Up Time for CE		25		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 2)
t_r (CE)	Release Time for CE		25		ns	
t_s	Set-Up Time for Data		15		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 3)
t_r	Release Time for Data		15		ns	
t_s (PE)	Set-Up Time for PE		20		ns	
t_r (PE)	Release Time for PE		20		ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

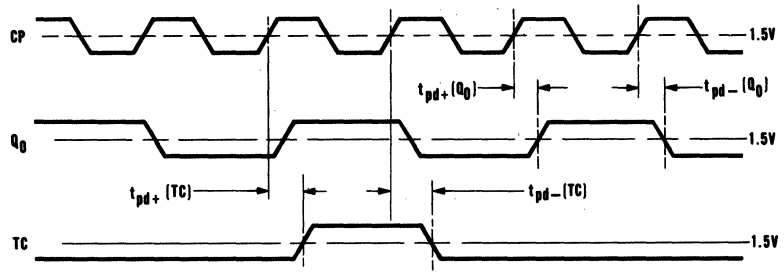


Fig. 1

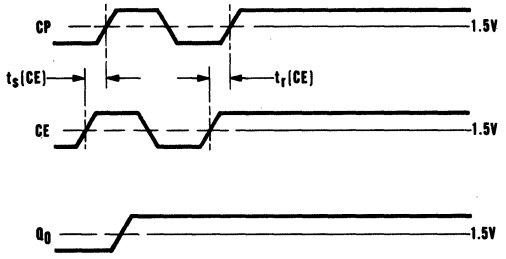


Fig. 2

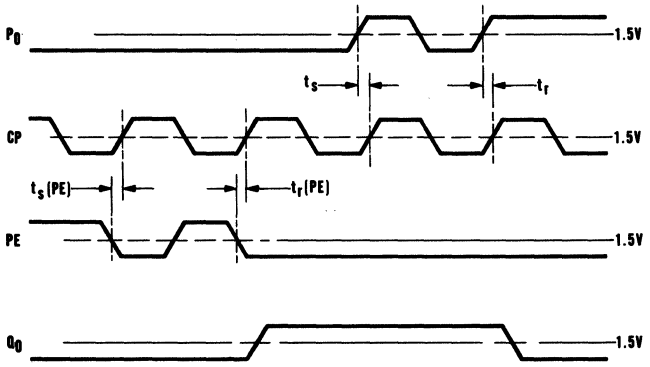


Fig. 3

APPLICATIONS

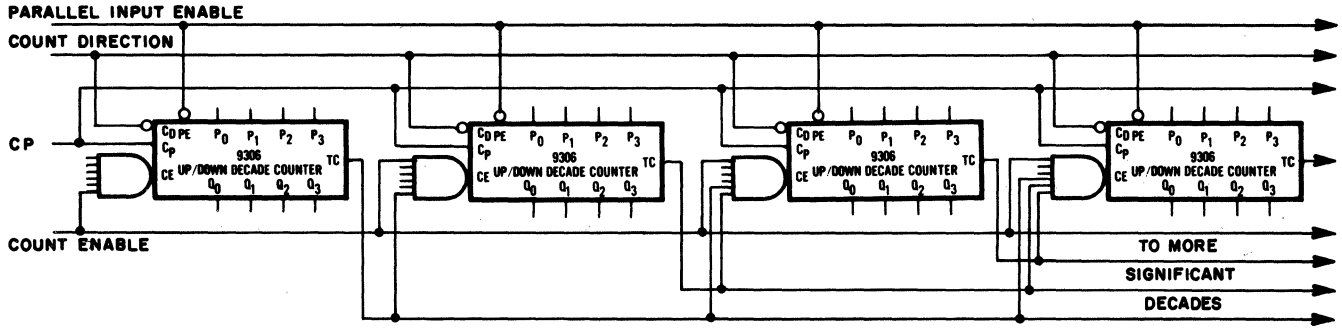


Fig. 4

9307

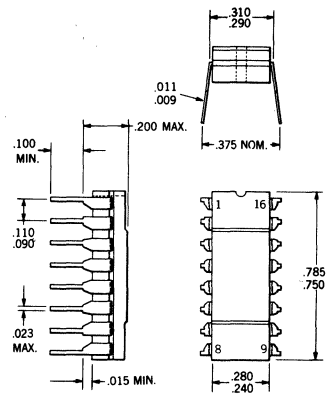
MSI SEVEN SEGMENT DECODER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

ENERAL DESCRIPTION — The 9307 is a Seven Segment Decoder designed to accept our inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment umerical display. The decoder can be used with seven segment incandescent lamp, neon, lectro-luminescent, or CRT numeric displays. The 9307 is compatible with all other Fairchild CSL devices.

- **CCSL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE HIGH OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE* PACKAGE**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

Fig. 1

LOGIC SYMBOL

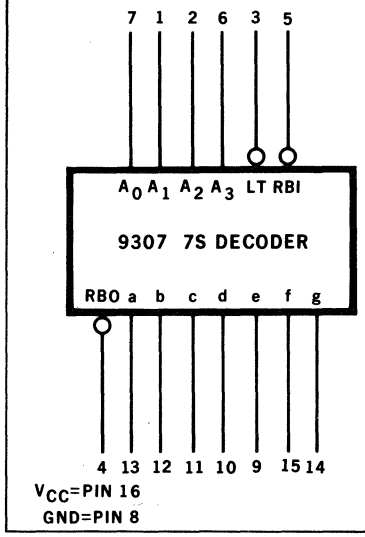


Fig. 2

BSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

RDER INFORMATION

pecify U6B9307XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

Fairchild patent pending.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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The 9307 seven segment decoder accepts a 4 Bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0 - 9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in Figure 3. The numeric designations chosen to represent the decimal numbers are shown in Figure 5, together with the resulting displays for input code configurations in excess of binary nine.

The decoder has active high outputs so that a buffer transistor may be used directly to provide the high currents required for incandescent displays. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. The value of this resistor is constrained by the 10 mA current sinking capability of the output transistors of the circuit.

The device has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display, conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, (0060.0300) would be displayed as (60.03). Leading edge zero suppression is obtained by connecting the Ripple Blanking Output (RBO) of a decoder to the Ripple Blanking Input (RBI) of the next lower stage device. The most significant decoder stage should have the RBI input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the RBI input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active low input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The RBO terminal of the decoder can be OR - tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of DTμL gates.

Fig. 3
SEGMENT DESIGNATION

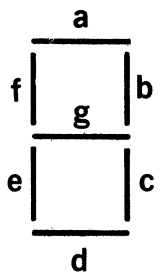


Fig. 4
TRUTH TABLE

LT	RB IN	A_0	A_1	A_2	A_3	a	b	c	d	e	f	g	RB OUT	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
|	X	H	L	L	L	L	H	H	L	L	L	L	H	1
|	|	L	H	L	L	H	H	L	H	H	L	H	H	2
|	|	H	H	L	L	H	H	H	H	L	L	H	H	3
|	|	L	L	H	L	L	H	H	L	L	H	H	H	4
|	|	H	L	H	L	H	L	H	H	L	H	H	H	5
|	|	L	H	H	L	H	L	H	H	H	H	H	H	6
|	|	H	H	H	L	H	H	H	L	L	L	L	H	7
|	|	L	L	L	H	H	H	H	H	H	H	H	H	8
|	|	H	L	L	H	H	H	H	H	L	H	H	H	9
|	|	L	H	L	H	L	L	L	H	H	L	H	H	10
|	|	H	H	L	H	L	L	L	H	L	L	H	H	11
|	|	L	L	H	H	L	H	H	L	L	H	H	H	12
|	|	H	L	H	H	H	L	H	H	L	H	H	H	13
|	|	L	H	H	H	L	L	L	H	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	H	15

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = EITHER HIGH OR LOW VOLTAGE LEVEL

Fig. 5
NUMERICAL DESIGNATIONS

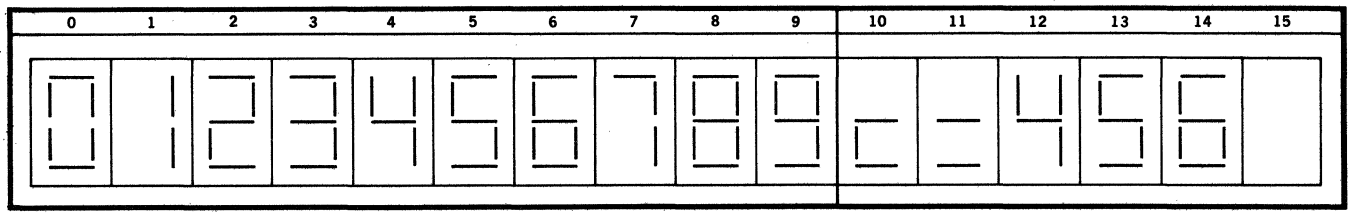


Table 1—Loading Rules (1 U.L. = 1 DTμL Gate Input Load)

Inputs	Loading (51X & 59X)	
	High State	Low State
A_0, A_1, A_2, A_3	1	1
$R_{B(IN)}$	1	½
LT	5	4.3

Outputs	Fan Out	
	51X	59X
a, b, c, d, e, f, g	8	7
$R_{B(OUT)}$	2.0	1.5

TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930751X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	4.3 3.0		4.3 3.0	4.4 4.0		4.4 3.0		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = 0.0\ mA$ (Pins 9-15) $V_{CC} = 4.5\ V$ $I_{OH} = -70\ \mu A$ (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 12.5\ mA$ (Pins 9-15) $I_{OL} = 3.1\ mA$ (Pin 4) $V_{CC} = 4.5\ V$ $I_{OL} = 10\ mA$ (Pins 9-15) $I_{OL} = 2.4\ mA$ (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (Pin 3) I_F (Pins 1, 2, 6, 7) I_F (Pin 5)	Input Load Current Input Load Current Input Load Current		−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ $V_R = 5.5\ V$ on other inputs
I_R (Pin 3) I_R (Pins 1, 2, 5, 6, 7)	Input Leakage Current Input Leakage Current					10 2.0		25 5.0	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Ground on other inputs
I_A (Pins 9-15)	Available Output Current	−1.4		−1.4			−1.0		mA	$V_{OUT} = 0.85\ V$ $V_{CC} = 4.5\ V$ Inputs at threshold voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9-15)	Short Circuit Current					−3.7			mA	$V_{OUT} = 0.0\ V$ $V_{CC} = 5.5\ V$
t_{pd+}	Switching Speed					500			ns	$V_{CC} = 5.0\ V$, See Figure 6
t_{pd-}	Switching Speed					500			ns	

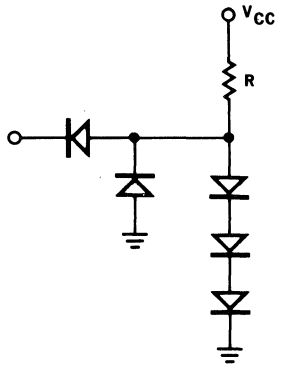
TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U6B930759X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	4.3 2.7		4.3 2.7	4.6 4.0		4.3 2.7		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = 0.0\ mA$ (Pins 9-15) $V_{CC} = 4.75\ V$ $I_{OH} = -70\ \mu A$ (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 11.5\ mA$ (Pins 9-15) $I_{OL} = 2.75\ mA$ (Pin 4) $V_{CC} = 4.75\ V$ $I_{OL} = 10\ mA$ (Pins 9-15) $I_{OL} = 2.4\ mA$ (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{IH}	Input High Voltage	2.0		2.0			2.0		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (Pin 3) I_F (Pins 1, 2, 6, 7) I_F (Pin 5)	Input Load Current Input Load Current Input Load Current		−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ $V_R = 5.25$ on other inputs
I_R (Pin 3) I_R (Pins 1, 2, 5, 6, 7)	Input Leakage Current Input Leakage Current					25 5.0		50 10	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Ground on other inputs
I_A (Pins 9-15)	Available Output Current	−1.4		−1.4			−1.0		mA	$V_{OUT} = 0.75\ V$ $V_{CC} = 4.75\ V$ Inputs at threshold voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9-15)	Short Circuit Current					−4.0			mA	$V_{OUT} = 0.0\ V$ $V_{CC} = 5.5\ V$
t_{pd+}	Switching Speed					500			ns	$V_{CC} = 5.0\ V$, See Figure 6
t_{pd-}	Switching Speed					500			ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

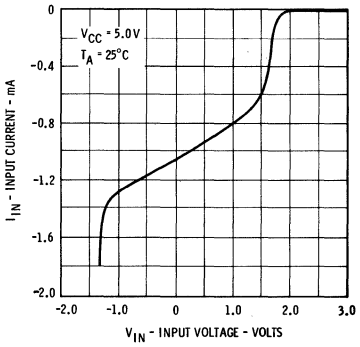
INPUTS

Equivalent Circuit

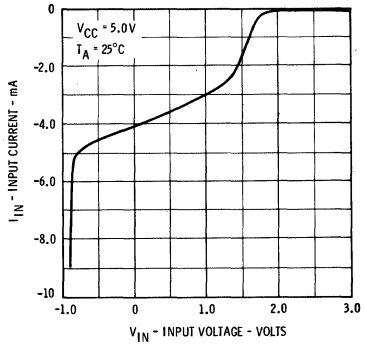


INPUT CURRENT VERSUS INPUT VOLTAGE

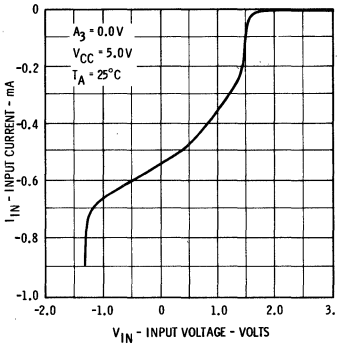
A_0, A_1, A_2, A_3 INPUTS



LT INPUT



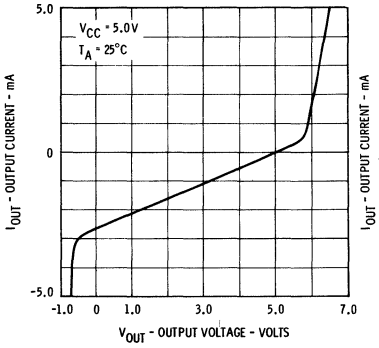
$RB_{(IN)}$ INPUT



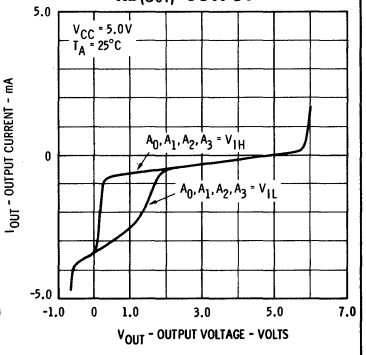
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

U6B930751X (−55°C to +125°C) OUTPUT IN HIGH STATE

a, b, c, d, e, f, g OUTPUTS

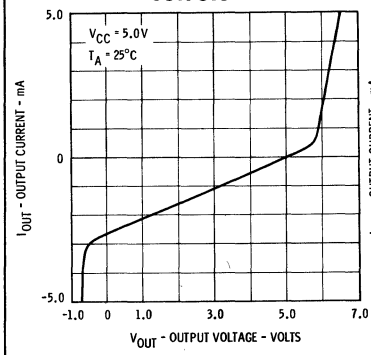


$RB_{(OUT)}$ OUTPUT

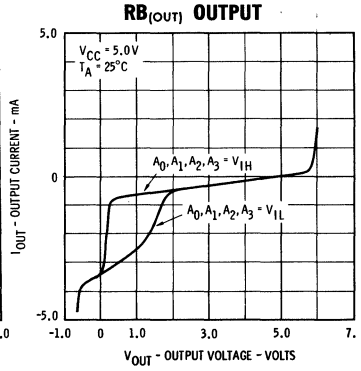


U6B930759X (0°C to +75°C) OUTPUT IN HIGH STATE

a, b, c, d, e, f, g OUTPUTS

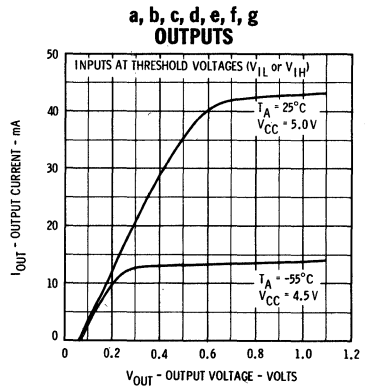


$RB_{(OUT)}$ OUTPUT

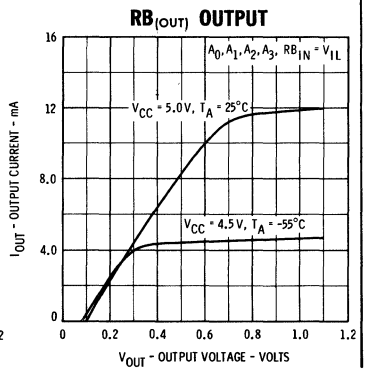


OUTPUT IN LOW STATE

a, b, c, d, e, f, g OUTPUTS

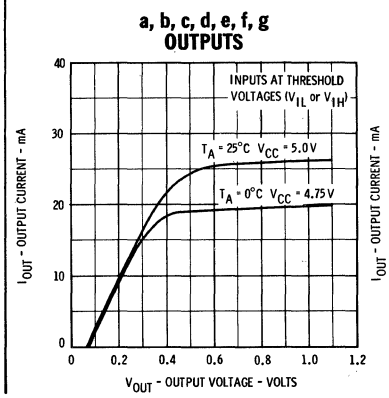


$RB_{(OUT)}$ OUTPUT

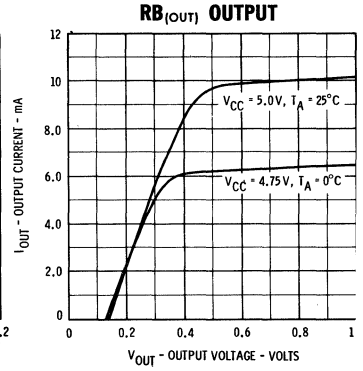


OUTPUT IN LOW STATE

a, b, c, d, e, f, g OUTPUTS



$RB_{(OUT)}$ OUTPUT



OUTPUTS

Equivalent Circuit

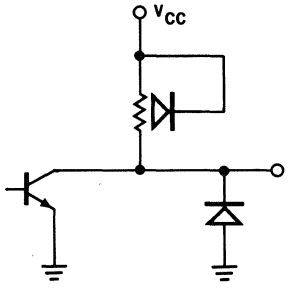
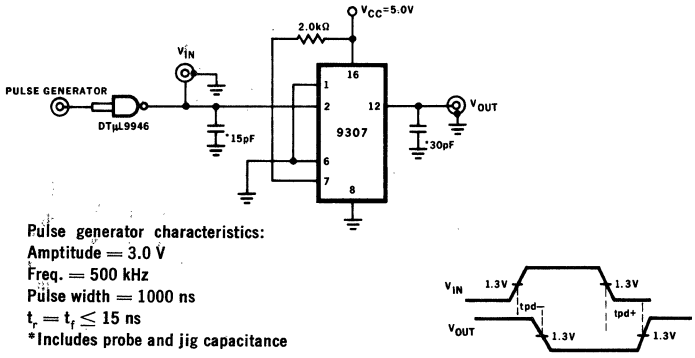


Fig. 6—SWITCHING CIRCUIT AND WAVEFORMS



Pulse generator characteristics:
Amplitude = 3.0 V
Freq. = 500 kHz
Pulse width = 1000 ns
$t_r = t_f \leq 15$ ns
*Includes probe and jig capacitance

APPLICATIONS

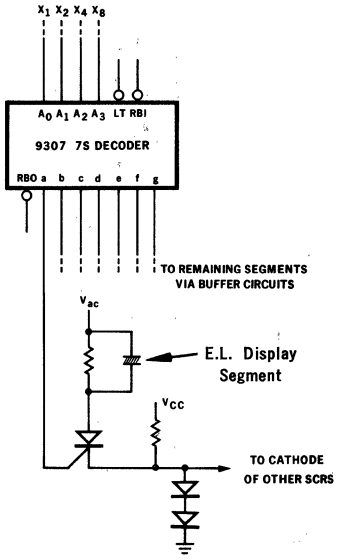


Fig. 7
9307 Seven Segment Decoder driving Electro-Luminescent Display.

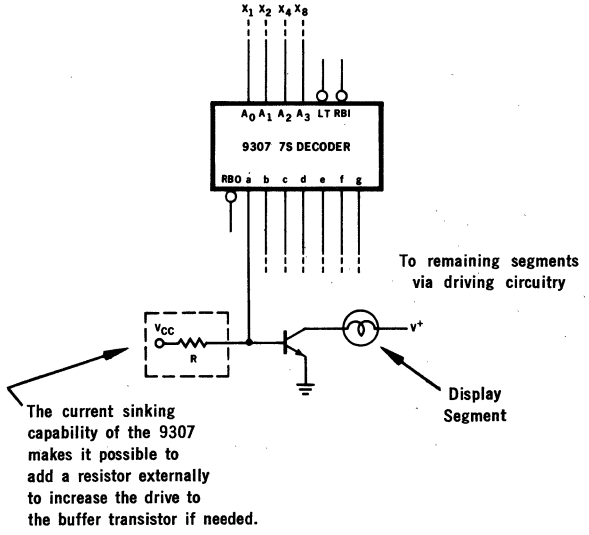


Fig. 8
9307 Seven Segment Decoder driving Incandescent lamp Display.

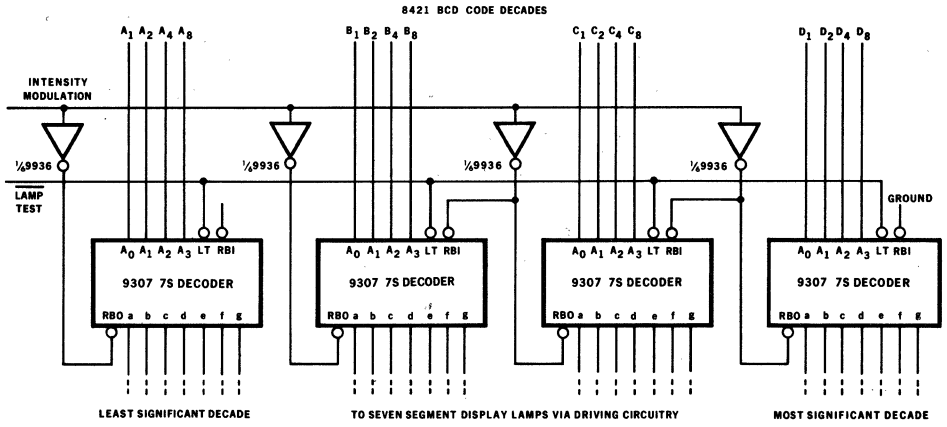


Fig. 9—FOUR DECADE SEVEN SEGMENT INTEGER DISPLAY SCHEME

This scheme incorporates automatic blanking of leading edge zeroes and intensity modulation using an external variable duty cycle signal.

9308

MSI DUAL FOUR-BIT LATCH

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MSI 9308 is a Dual 4-Bit Latch designed for general purpose storage applications in high speed digital systems. The 9308 uses TTμL technology and is CCSL compatible. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good A.C. noise immunity.

FEATURES

- **ACTIVE LEVEL LOW ENABLE GATE INPUTS**
- **OVERRIDING MASTER RESET**
- **25 ns THROUGH DELAY**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE DIRECT INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Input Voltage (D.C.) (See Note 1)	−0.5 V to +5.5 V
Input Current (D.C.) (See Note 1)	−30 mA to +5 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

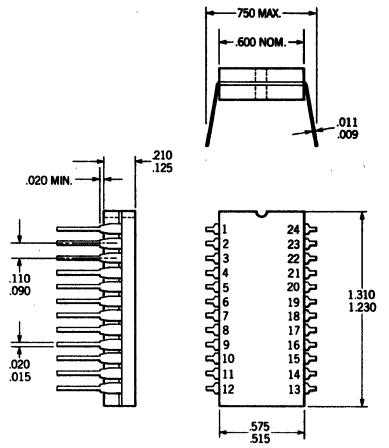
NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

DESCRIPTION OF LATCH OPERATION — Data can be entered into the latch when both of the enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes high, the data present in the latch at that time is held in the latch and is no longer affected by the data input.

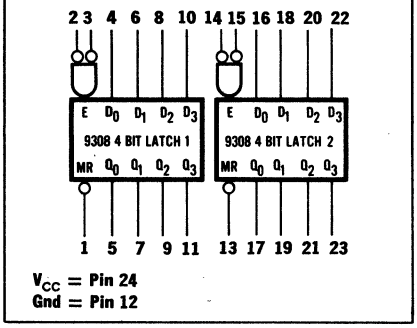
The master reset overrides all other input conditions and forces the outputs of all the latches low when a low signal is applied to the master reset input.

ORDER INFORMATION — Specify U6N9308XXX for 24-pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



V_{CC} = Pin 24
Gnd = Pin 12

Electrical Characteristics on Page 2.

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TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$, See Note 1) (Part #U6N930851X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.8		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 14.4\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 11.2\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_1 and MR Inputs		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
1.5 I_F	Input Load Current D Inputs		−2.7		−1.9	−2.7		−2.7		$V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current E_0, E_1 and MR Inputs				10	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		90		65	90		90	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

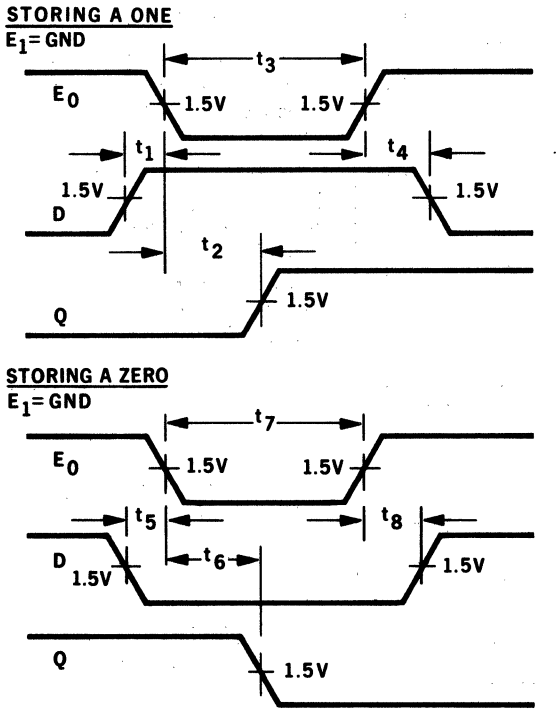
TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$, See Note 1) (Part #U6N930859X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OUT} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OUT} = 14.4\ mA$ $V_{CC} = 4.75\ V$, $I_{OUT} = 12.7\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_1 and MR Inputs		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
1.5 I_F	Input Load Current D Inputs		−2.7		−1.8	−2.6		−2.7		$V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current E_0, E_1 and MR Inputs				10	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		117		65	117		117	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

NOTE 1: Units are pulse tested.
NOTE 2: Output Voltages are guaranteed for either the input enabled or input disabled case.
NOTE 3: This current is measured at $V_{IN} = 0.0\ V$ to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at $V_{IN} = 0.4\ V$ is 2.4 mA.

A.C. CHARACTERISTICS

9308 SWITCHING WAVEFORMS



TIME	DEFINITION	LIMIT (See Note 4) MIN.	TYP.	MAX.	UNITS
t_1	Min. time that data must be present before enable to not increase t_2	X	minus 4	—	ns
t_2	Delay from enable to output turning off	—	22	X	ns
t_3	Min. enable pulse width to store a ONE	X	15	—	ns
t_4	Min. time that data must remain constant after removal of enable	X	5	—	ns
t_5	Min. time that data must be present before the enable to not increase t_6	X	0	—	ns
t_6	Delay from enable to output turning on	—	15	X	ns
t_7	Min. enable pulse width to store a ZERO	X	15	—	ns
t_8	Min. time that data must remain constant after removal of enable	X	2	—	ns

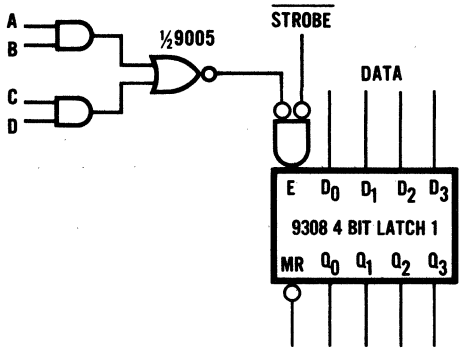
NOTE 4: Limits indicated by X will be shown on final data sheets.

All delays are measured with $V_{CC} = 5.0$ V applied to Pin 24 and Pin 12 grounded. The active input is driven by a 9002 TTμL gate with the output loaded with 15 pF. All outputs are loaded with 15 pF.

LOADING RULES

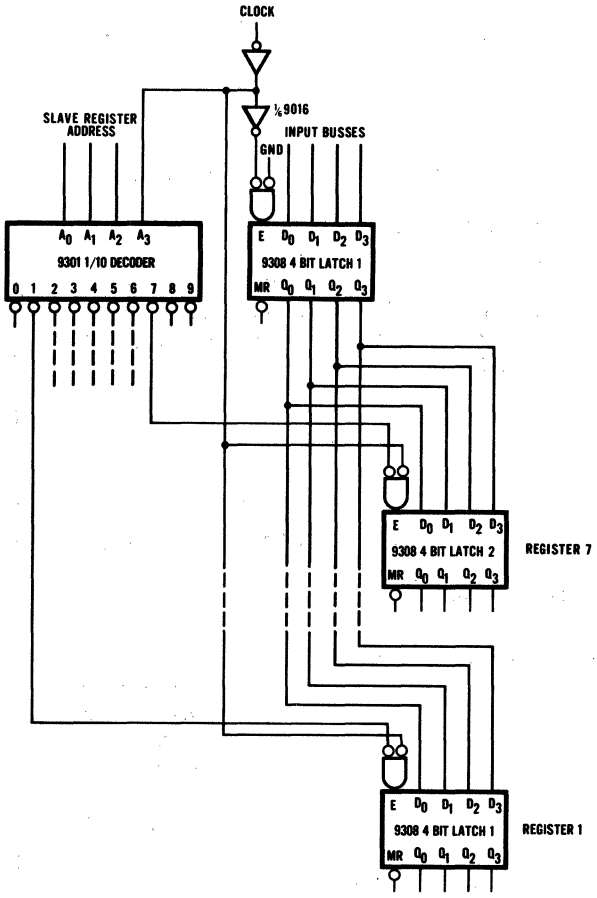
	PIN	LOADING
INPUTS	D_0, D_1, D_2, D_3	1.5
	MR, E_0, E_1	1.0
OUTPUTS	Q_0, Q_1, Q_2, Q_3	9.0

APPLICATIONS

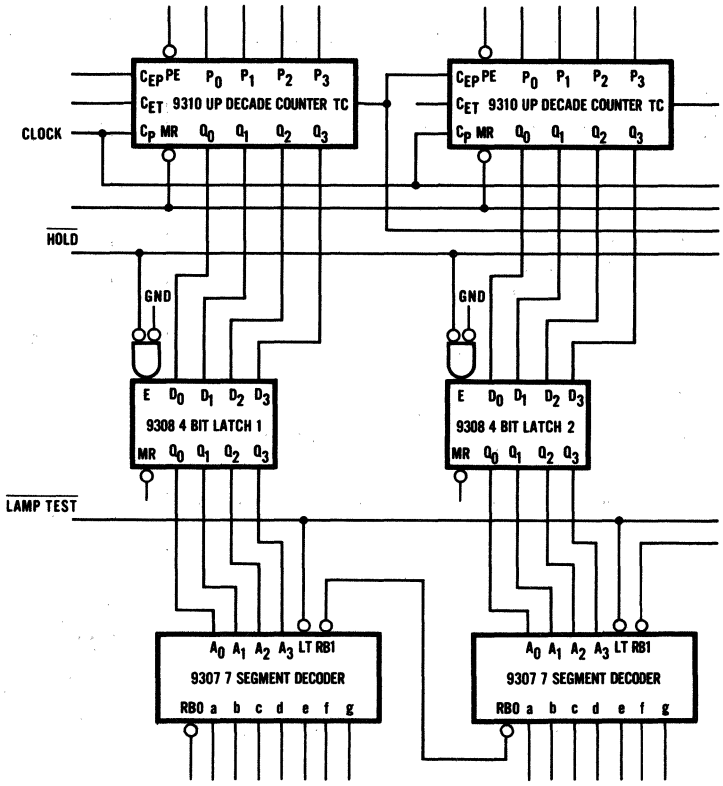


AND-OR ENABLE SHOWING ACTIVE LEVEL
LOW ENABLE GATE UTILITY

SINGLE MASTER/MULTIPLE SLAVE FLIP-FLOP



9308 AS A HOLDING REGISTER IN COUNTING AND DISPLAY APPLICATIONS



9309

MSI DUAL FOUR-INPUT MULTIPLEXER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9309 is a monolithic, high speed, dual four-input digital multiplexer circuit, constructed with the Fairchild Planar* epitaxial process. It consists of two multiplexing circuits with common input select logic, each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the 9309 can generate any two function of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTμL for high speed, high fanout operation and is compatible with all other members of the CCSL family of digital integrated circuits.

FEATURES

- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

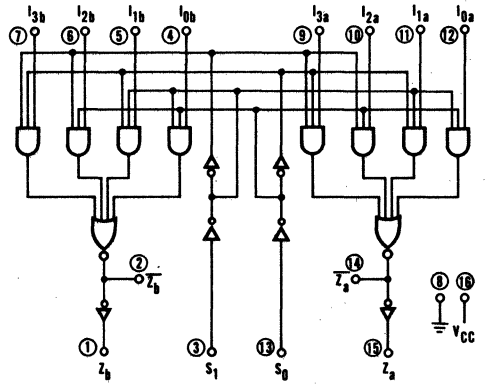
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Output when output is high	0 V to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into Output when output is low	+30 mA

Note 1—either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify U6B9309XXX for 16-pin Dual In-Line package or U3L9309XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

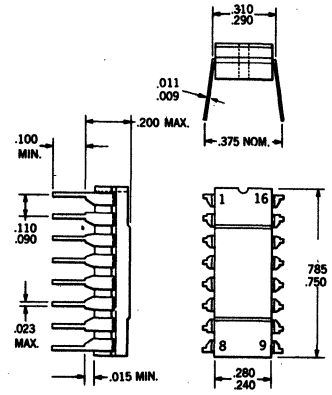
LOGIC DIAGRAM



9309
Dual four input multiplexer
Logic diagram

Fig. 4

DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

Fig. 1

FLAT PACKAGE

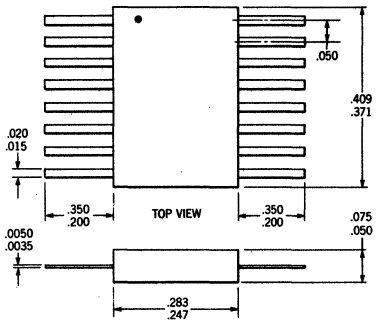
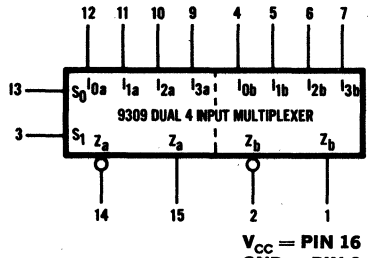


Fig. 2

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 3

*Planar is a patented Fairchild process.

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FUNCTIONAL DESCRIPTION

The 9309 dual four input multiplexer is a member of the Fairchild family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

The 9309 dual four input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Z_a = I_{0a} \cdot S_1 \cdot S_0 + I_{1a} \cdot S_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot S_0 + I_{3a} \cdot S_1 \cdot S_0$$

$$Z_b = I_{0b} \cdot S_1 \cdot S_0 + I_{1b} \cdot S_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot S_0 + I_{3b} \cdot S_1 \cdot S_0$$

A common use of the 9309 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs.

TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	Z_a
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	Z_b
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = either high or low logic level

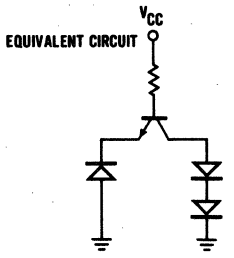
LOADING RULES

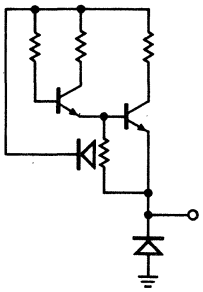
(1 U.L. = 1 TTμL gate input load)

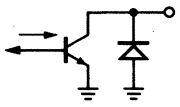
INPUTS	LOADING
I_{0a}, I_{1a}, I_{2a}, I_{3a}, I_{0b}, I_{1b}, I_{2b}, I_{3b}, S_0, S_1	1 U.L.

	FANOUT AT LOGIC LEVEL	
OUTPUTS	HIGH	LOW
Z_a, Z_b	20 U.L.	10 U.L.
Z_a, Z_b	18 U.L.	9 U.L.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS







INPUT CURRENT VERSUS INPUT VOLTAGE

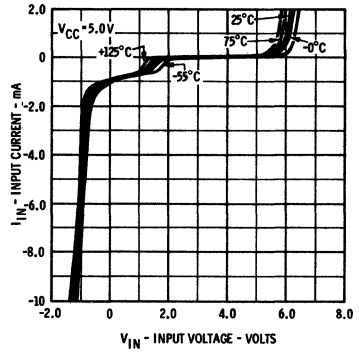


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

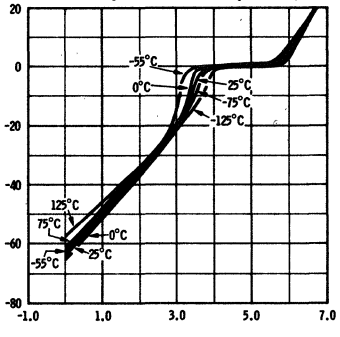


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

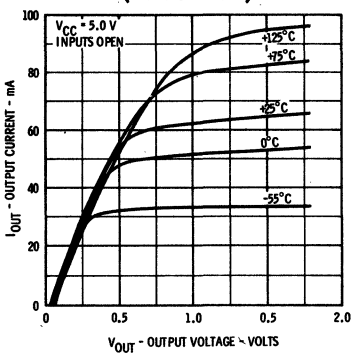


Fig. 7

ELECTRICAL CHARACTERISTICS* ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part No. UXX930951X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2\ mA$ (Pins 1 & 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08\ mA$ (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0\ mA$ (Pins 1 & 15) $I_{OL} = 14.4\ mA$ (Pins 2 & 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4\ mA$ (Pins 1 & 15) $I_{OL} = 11.2\ mA$ (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		30	40		40	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_a)	Switching Speed				24	32			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$, See Figure 5
t_{pd-} (S_0 to Z_a)	Switching Speed				24	32			ns	

*Pulse tested

ELECTRICAL CHARACTERISTICS* ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part No. UXX930959X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2\ mA$ (Pins 1 & 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08\ mA$ (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0\ mA$ (Pins 1 & 15) $I_{OL} = 14.4\ mA$ (Pins 2 & 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1\ mA$ (Pins 1 & 15) $I_{OL} = 12.7\ mA$ (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		30	43		43	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_a)	Switching Speed				24	32			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$, See Figure 5
t_{pd-} (S_0 to Z_a)	Switching Speed				24	32			ns	

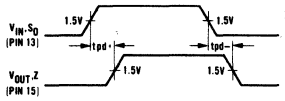
*Pulse tested

SWITCHING WAVEFORMS

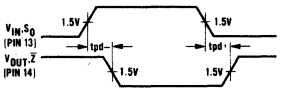
All input waveforms are output of TTμL 9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

Fig. 8 — WAVEFORMS

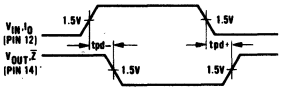
t_{pd}; S_0 to Z_a
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}



t_{pd}; S_0 to Z_a
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}



t_{pd}; I_{a0} to Z_a
CONDITIONS
Pins 3, 13 = GND.



SWITCHING CHARACTERISTICS

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

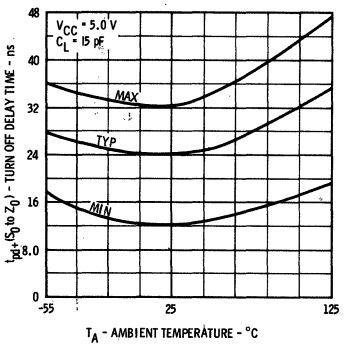


Fig. 9

TURN ON DELAY TIME VERSUS TEMPERATURE (S_0 to Z_a)

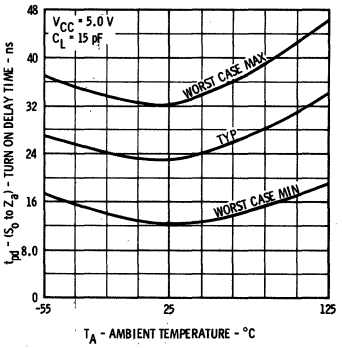


Fig. 10

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to Z_a)

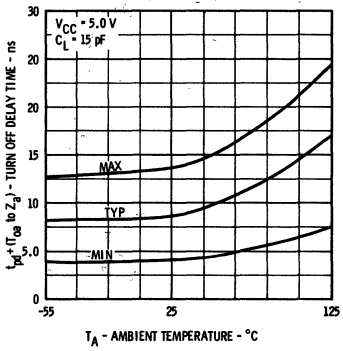


Fig. 11

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to Z_a)

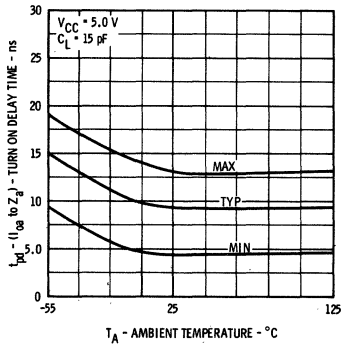


Fig. 12

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

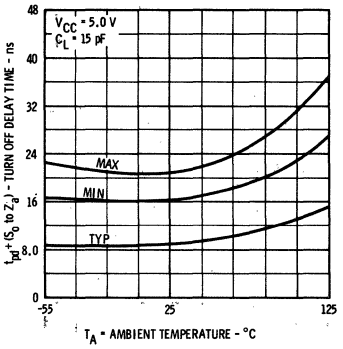


Fig. 13

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

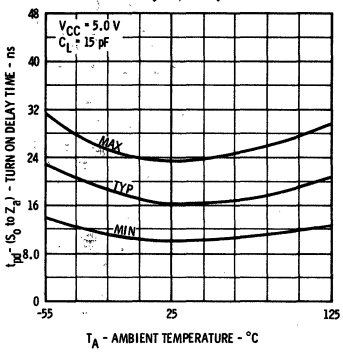


Fig. 14

APPLICATIONS

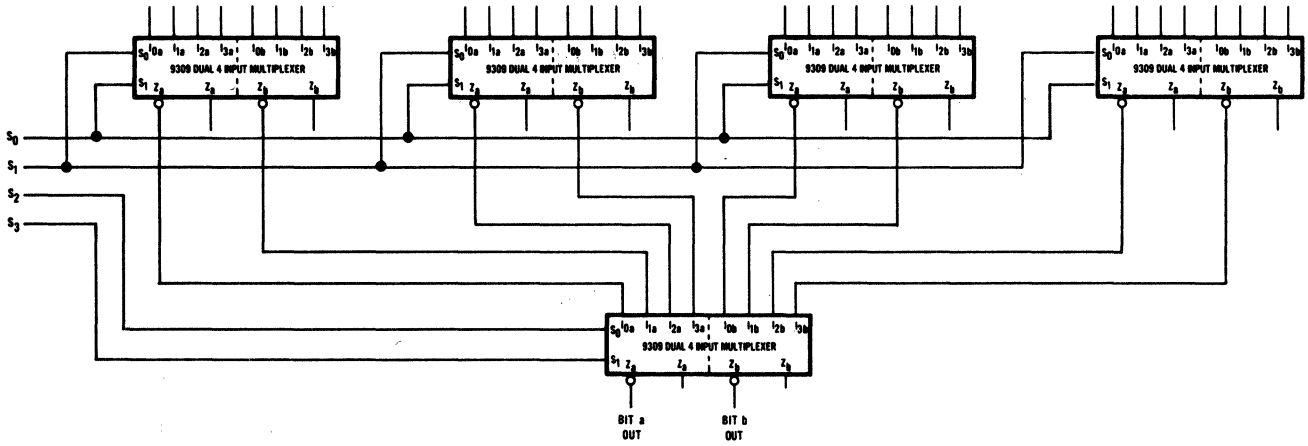


Fig. 12 — MULTIPLEXING TWO BITS FROM SIXTEEN SOURCES

This diagram shows the interconnection of five 9309 dual four bit multiplexers to provide switching of two bits of data from one of sixteen words onto a two bit data buss. The selection of which word will be transferred to the buss is made by the address supplied to the S_0, S_1, S_2 and S_3 inputs. As an example: if twelve bit words are to be transferred to a twelve bit buss, the above diagram would be repeated six times. Notice that the negative outputs are used at both levels resulting in the assertion output (negation of the negation) at a higher speed due to the fact that the through delay is less on the negation output.

If the word selecting address is held in four TTμL flip flops (two dual packages) enough load capability is available to select between sixteen, sixteen bit words.

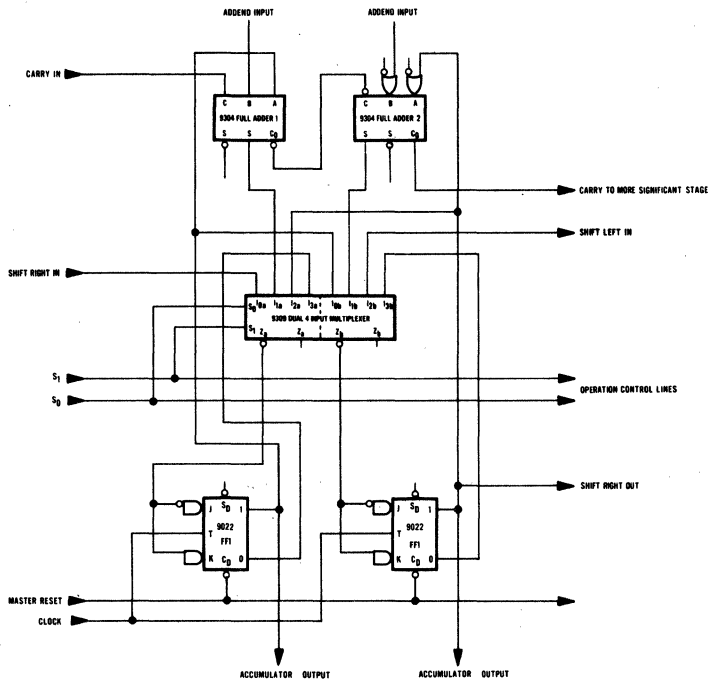


Fig. 13 — GENERAL PURPOSE ACCUMULATOR

A fast, general purpose accumulator for computer applications is capable of: 1) shift left; 2) add; 3) shift right and 4) complement operations. Only three packages are required to construct two stages of the general purpose accumulator (Figure 1).

The D input capability of the 9022 is utilized here to allow each flip flop of the accumulator to accept the data as presented by the 9309 multiplexer.

Under the operation code instructions the multiplexer provides an input to the 9022 from: 1) adjacent stage to the right for a shift left operation; 2) adjacent stage to the left for a shift right operation; 3) output of adders for add operation and 4) Q outputs of 9022 for the complement operation. The operation code at the right of Figure 1 shows the instruction codes to perform the various operations.

The accumulator should be capable of 20 to 25 MHz operation.

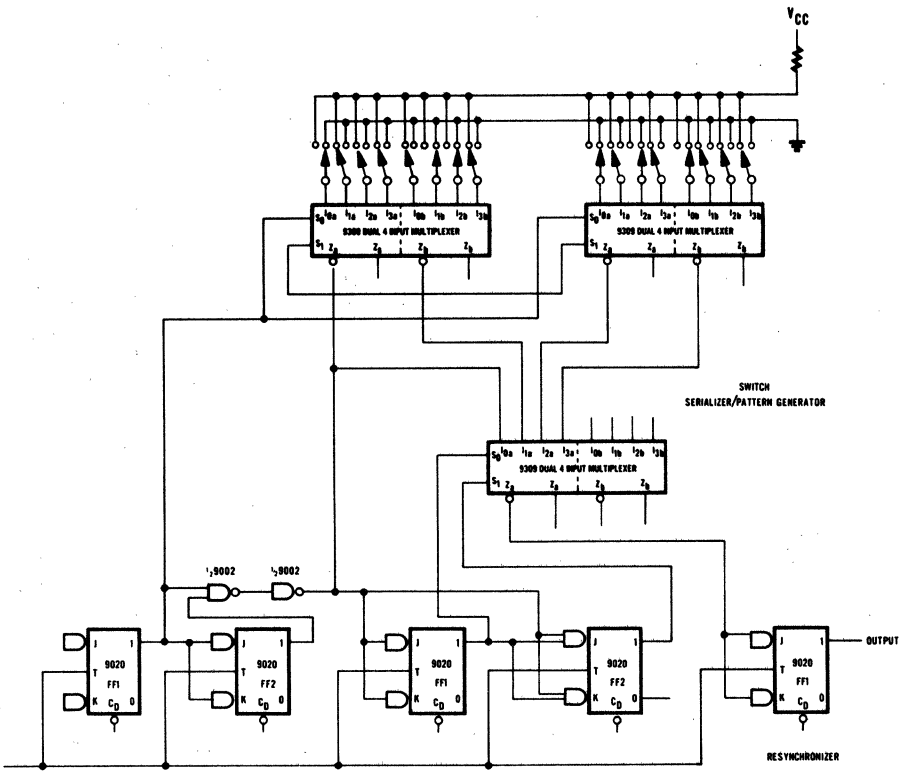
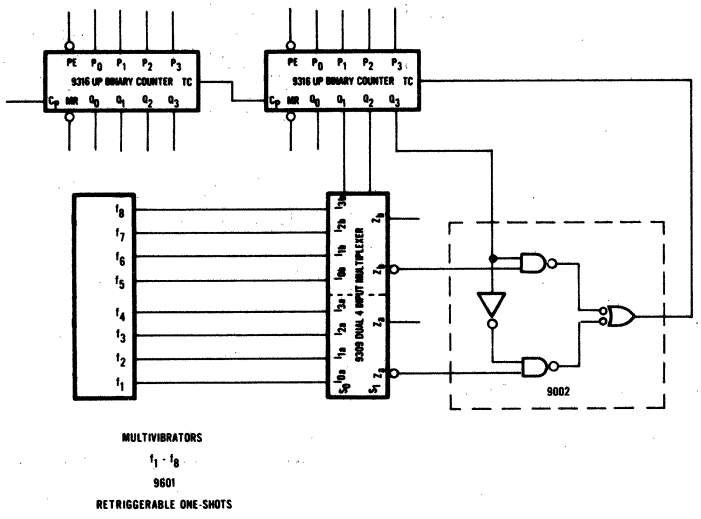


Fig. 14 — 16-BIT PATTERN GENERATOR

This application illustrates the use of 9309 and 9020 in the design of one channel of a 16 bit pattern generator. Each channel requires ½ 9020, ½ 9002 and 2½ 9309. Each channel consists of a switch serializer/pattern generator and resynchronizer sections with a modulo 16 binary counter common to all channels.

The two least significant bits and two most significant bits of the counter control the first and second stages of multiplexing respectively. In this manner four bits are multiplexed on each of the four lines from the first stage to the second stage. Every four clock times a new input line containing four multiplexed bits is selected by the second stage of the serializer thus serializing the 16 input bits from the switches.

The resynchronizer flip flop is used to eliminate decoding spikes.



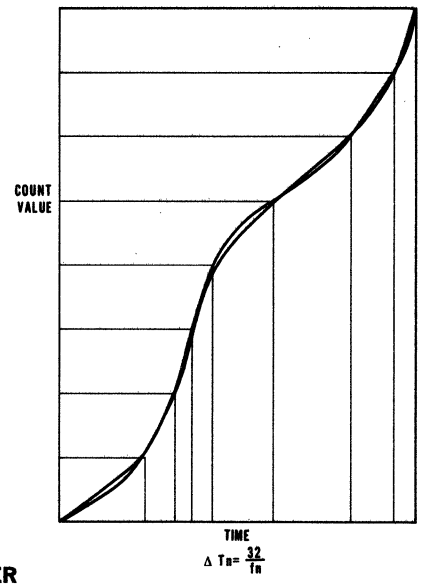


Fig. 15 — NON-LINEAR COUNTER

OPERATION CODE LIST

S_0	S_1	INSTRUCTION
0	0	SHIFT LEFT
1	0	ADD
0	1	SHIFT RIGHT
1	1	COMPLEMENT

H = "1", L = "0"

The rate of the non-linear counter depends on the multivibrator clock frequency selected under control of the three most significant bits of the counter. This makes the count rate a function of both the count value of counter and frequency of clock multivibrator selected.

Clock multiplexing is accomplished by a 9309 dual 4-input multiplexer and one 9002 quad gate. Eight line segments representing clock rates of the multivibrators may be adjusted in slope to approximate a non-linear function.

9310

MSI BCD DECADE COUNTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9310 is a high speed synchronous 8421 BCD decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several decades of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES:

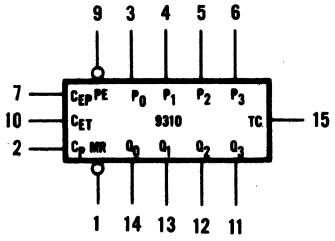
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **TYPICAL POWER DISSIPATION OF 300 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC HERMETIC 16 PIN DUAL IN-LINE PACKAGE AND FLAT PACKAGE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify U6B9310XXX for 16-pin Dual In-Line Package, U3L9310XXX for 16-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

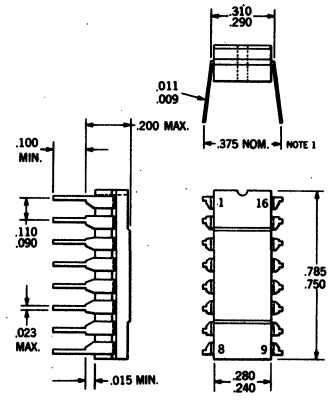
LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

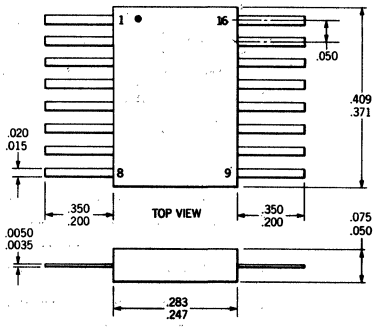
PHYSICAL DIMENSIONS

DUAL IN-LINE PACKAGE



NOTE:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

FLAT PACKAGE



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

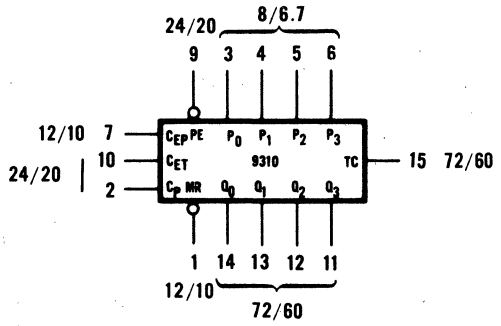
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of CEP or CET from high to low or of PE from low to high may only be done when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics." The asynchronous MR clears the counter independent of any other input.

Note: CE (count enable) = CEP • CET
TC = CET • Q_0 • Q_1 • Q_2 • Q_3

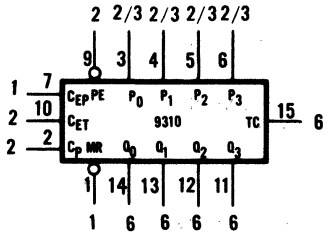
LOADING RULES

CCSL LOAD AND DRIVE FACTORS



Vcc = Pin 16
Gnd = Pin 8

TTμL LOAD AND DRIVE FACTORS



Vcc = Pin 16
Gnd = Pin 8

(1 U.L. = 1 TTμL input gate load)

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 9.6 mA V_{CC} = 4.5 V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
2 I_F	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
⅔ I_F	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
2 I_R	Input Leakage Current CP, PE, CET		120		20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V
⅔ I_R	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 9.6 mA V_{CC} = 4.75 V, I_{OL} = 8.5 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.25 V V_F = 0.4 V
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE, CET		120		20	120		120	μA	V_{CC} = 5.25 V V_R = 4.5 V
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	V_{CC} = 5.0 V C_L = 15 pF (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		15		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		35		ns	
t_{pd-} (TC)	Turn-On Delay for TC		20		ns	
t_s (SE)	Set-Up Time for CE		14		ns	V_{CC} = 5.0 V C_L = 15 pF (Fig.2)
t_r (CE)	Release Time for CE		12		ns	
t_s	Set-Up Time for Data		18		ns	V_{CC} = 5.0 V C_L = 15 pF (Fig. 3)
t_r	Release Time for Data		17		ns	
t_s (PE)	Set-Up Time for PE		30		ns	
t_r (PE)	Release Time for PE		28		ns	
t_{pd-} (MR)	Turn-On Delay for MR		33		ns	V_{CC} = 5.0 V, C_L = 15 pF (Fig. 4)
$t_{p\pm}$	Propagation Delay for CET to TC		14		ns	V_{CC} = 5.0 V, C_L = 15 pF (Fig. 5)

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

Fig. 1

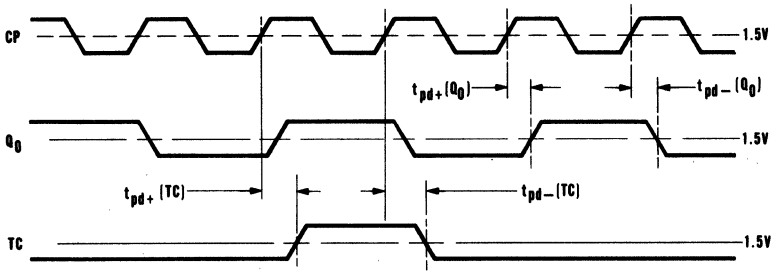


Fig. 2

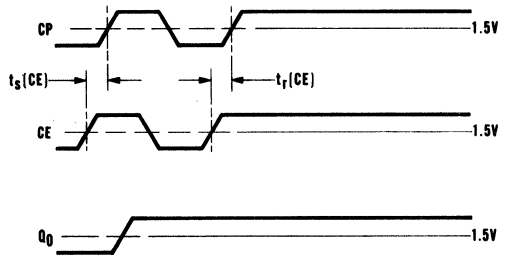


Fig. 3

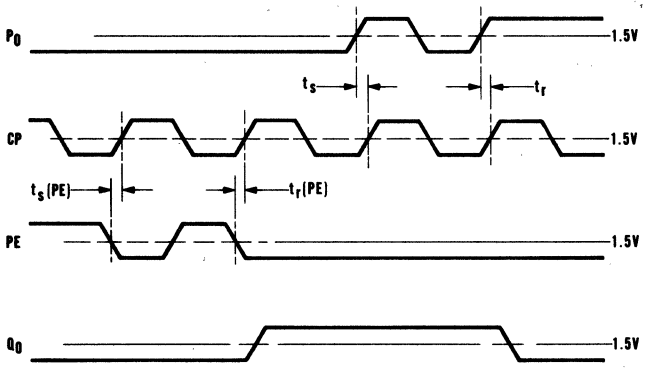


Fig. 4

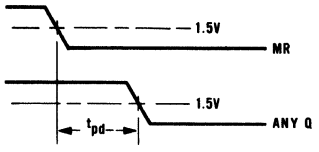
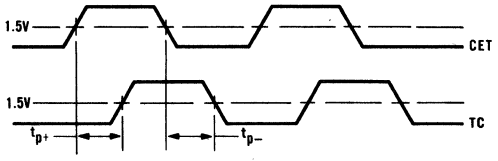
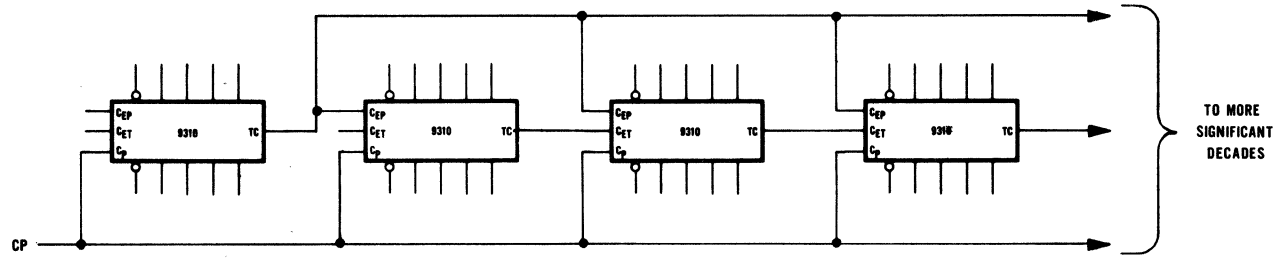


Fig. 5



APPLICATIONS



SYNCHRONOUS COUNTING SCHEME

9312

MSI EIGHT-INPUT MULTIPLEXER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9312 is a monolithic, high speed, eight input digital multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The 9312 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTμL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with all other members of the CCSL family of digital integrated circuits.

FEATURES

- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

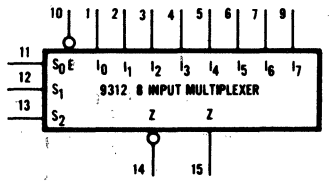
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage applied to output when output is high	0 V to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into output when output is low	+30 mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify U6B9312XXX for 16-pin Dual In-Line package or U3L9312XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

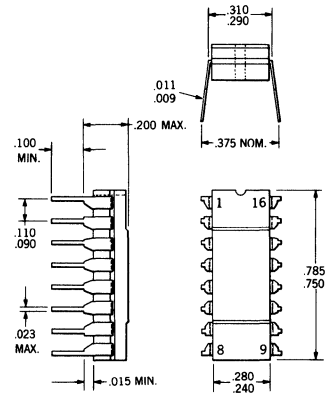
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 1

DUAL IN-LINE PACKAGE



NOTE :
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

Fig. 2

FLAT PACKAGE

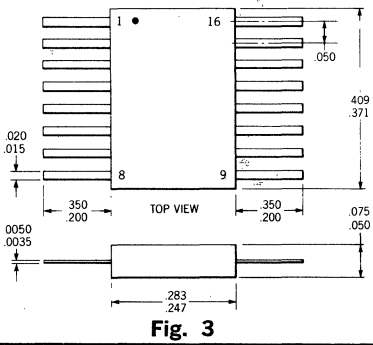


Fig. 3

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FUNCTIONAL DESCRIPTION — The 9312 is a logical implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The logic function provided at the output is:

$$Z = E\cdot(I_0\cdot\bar{S}_0\cdot\bar{S}_1\cdot\bar{S}_2 + I_1\cdot S_0\cdot\bar{S}_1\cdot\bar{S}_2 + I_2\cdot\bar{S}_0\cdot S_1\cdot\bar{S}_2 + I_3\cdot S_0\cdot S_1\cdot\bar{S}_2 + I_4\cdot\bar{S}_0\cdot\bar{S}_1\cdot S_2 + I_5\cdot S_0\cdot\bar{S}_1\cdot S_2 + I_6\cdot\bar{S}_0\cdot S_1\cdot S_2 + I_7\cdot S_0\cdot S_1\cdot S_2).$$

The 9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9312 can provide any logic function of four variables and its negation. Thus any number of random topic elements used to generate unusual truth tables can be replaced by one 9312.

TRUTH TABLE

E	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\bar{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Level does not affect output

Fig. 5

LOADING RULES

INPUTS	LOADING
All Inputs	1 U.L.

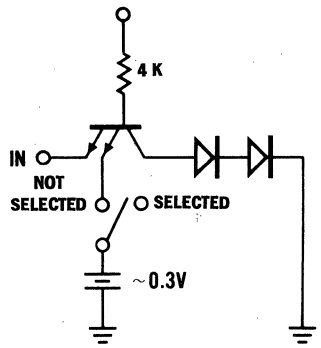
OUTPUTS	FAN-OUT	
	High State	Low State
$\bar{Z}$	18	9
Z	20	10

Fig. 4

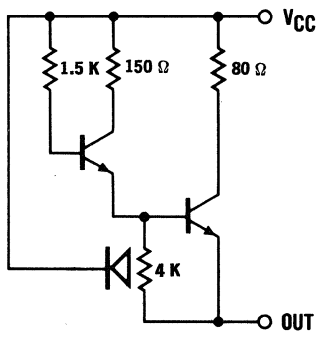
1 U.L. = 1 TTμL Unit Load
1 U.L. is defined by the entries I_R and I_F in the table on page 3.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

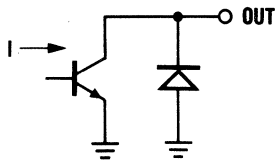
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

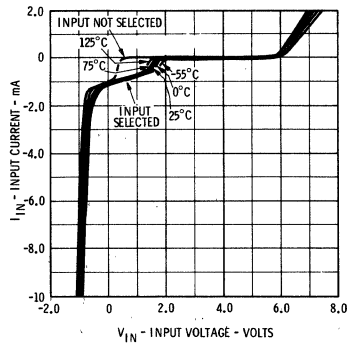


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

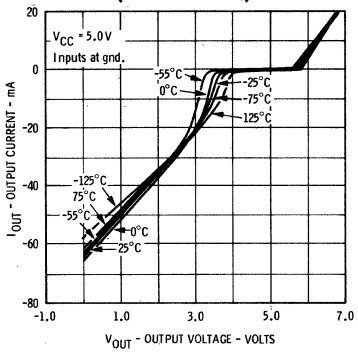


Fig. 7

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

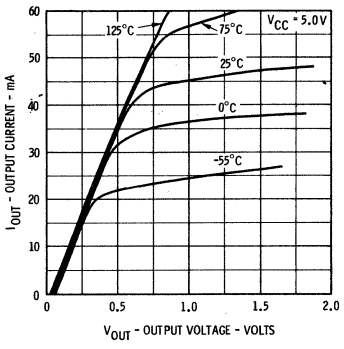


Fig. 8

ELECTRICAL CHARACTERISTICS* ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part No. UXX931251X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2\ mA$ (Pin 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0\ mA$ (Pin 15) $I_{OL} = 14.4\ mA$ (Pin 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4\ mA$ (Pin 15) $I_{OL} = 11.2\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			−1.24		−0.85	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		27	40		40	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15\ pF$

*Pulse tested

ELECTRICAL CHARACTERISTICS* ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part No. UXX931259X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2\ mA$ (Pin 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0\ mA$ (Pin 15) $I_{OL} = 14.4\ mA$ (Pin 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1\ mA$ (Pin 15) $I_{OL} = 12.7\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
			−1.41		−0.91	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		27	43		43	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15\ pF$

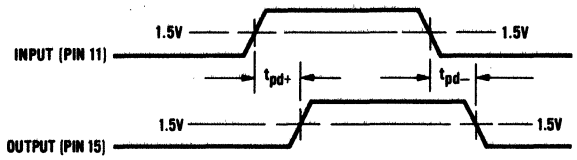
*Pulse tested

A. C. CHARACTERISTICS

A.C. CHARACTERISTICS

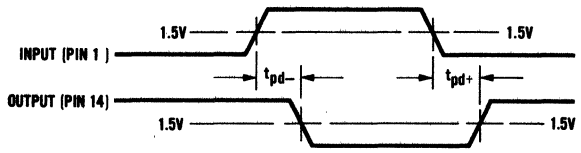
All measurements are made with $V_{CC} = 5.0$ V applied to pin 16 and with pin 8 grounded. The active input is driven by a 9002 TTμL gate with the output loaded with 15 pF. Both outputs of the 9312 are loaded with 15 pF.

t_{pd}: S_0 to Z



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = Vcc through 1.0 kΩ
Pin 16 = Vcc

t_{pd}: I_0 to $\overline{Z}$



Other Conditions: Pins 8, 10, 11, 12, 13 = Gnd
Pin 16 = Vcc

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

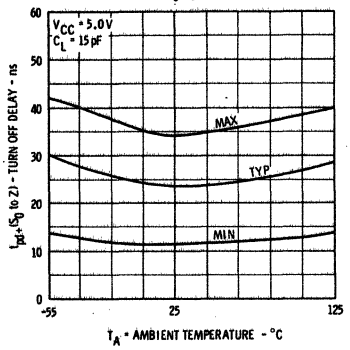


Fig. 9

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

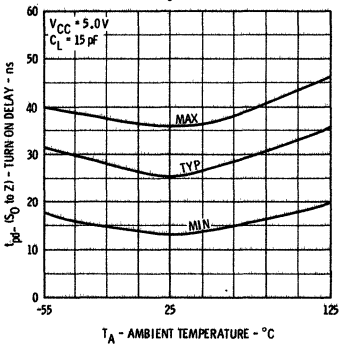


Fig. 10

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

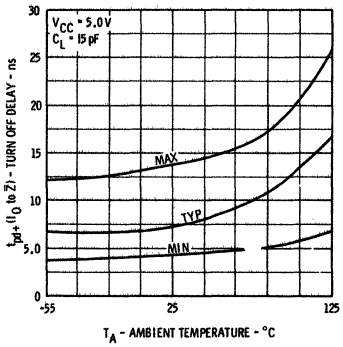


Fig. 11

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

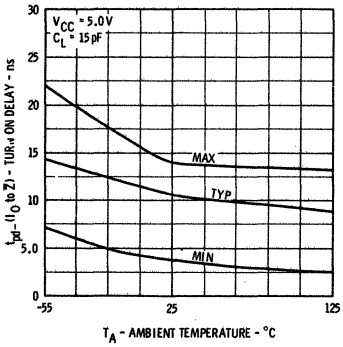
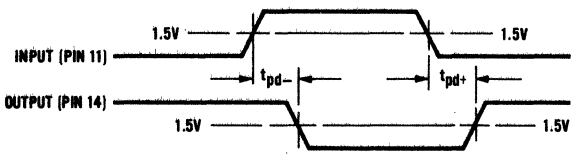


Fig. 12

t_{pd}: S_0 to $\overline{Z}$



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = Vcc through 1.0 kΩ
Pin 16 = Vcc

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

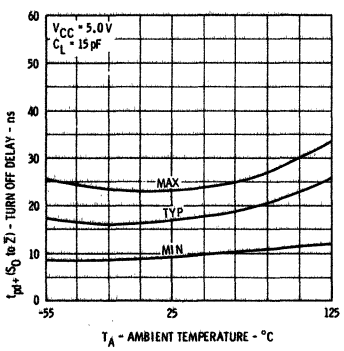


Fig. 13

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

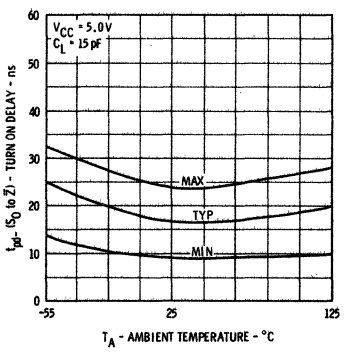
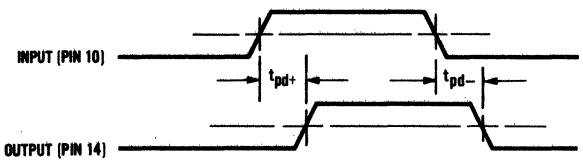


Fig. 14

t_{pd}: E to $\overline{Z}$



Other Conditions: Pins 8, 11, 12, 13 = Gnd
Pin 1 = Vcc through 2.0 kΩ
Pin 16 = Vcc

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; E to $\overline{Z}$

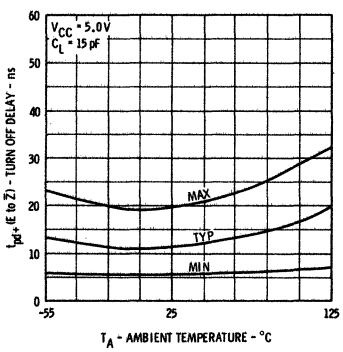


Fig. 15

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; E to $\overline{Z}$

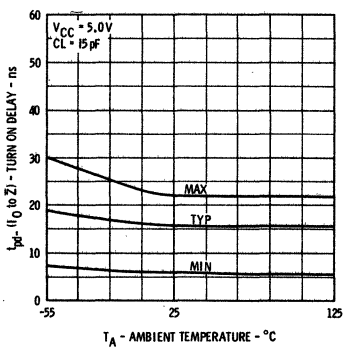


Fig. 16

APPLICATIONS

A MULTI-PORT MEMORY MODULE

The four bit by eight word multi-port memory module shown in the below diagram uses only thirteen MSI packages; four 9308 24 pin dual four bit latches, eight 9312 eight input multiplexers, and one 9301 one-out-of-ten decoder.

The module as shown is capable of simultaneously reading from two independently specified locations and writing into a third independently selected location. The necessary enables are provided so that a number of these modules may be connected together to produce a larger memory. As an example a sixteen bit by sixty-four word memory would require thirty-two of the modules shown below.

By connecting this type of memory to a function generator unit, a processor could be constructed that would execute three address instructions at a very high speed on the data contained in this type of memory. In order to utilize the speed of the memory the instructions would also have to be contained in fast semiconductor memory.

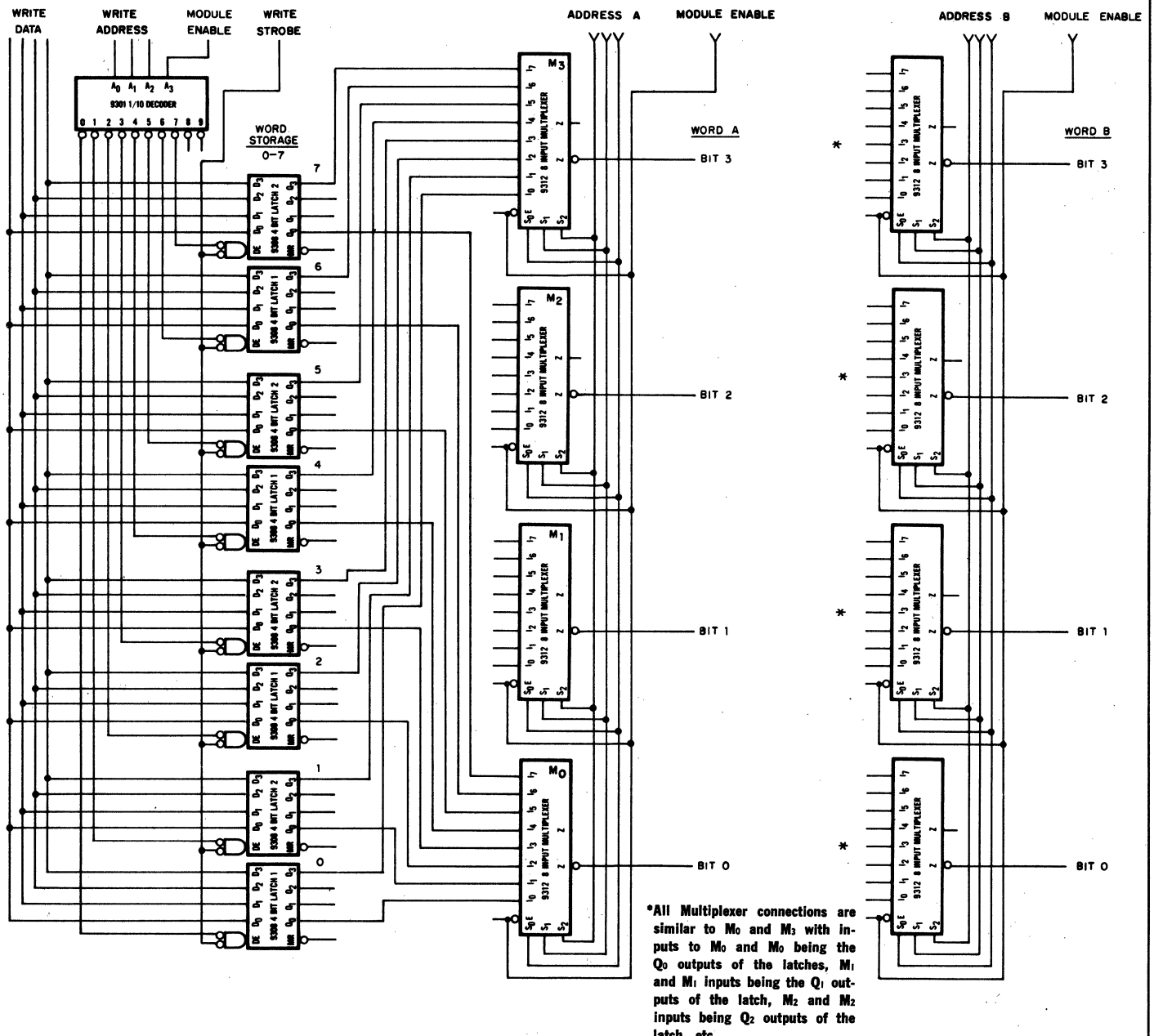


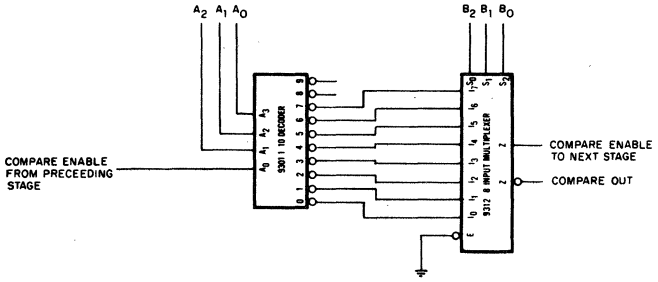
Fig. 17

APPLICATIONS

3 BIT COMPARATOR

Three bits of data to be compared are supplied to the address and select inputs of the 9301 and 9312 respectively. If A_0, A_1, A_2, and B_0, B_1, B_2 compare, the mutually exclusive active low output of the 9301 1/10 decoder and the selected input of the 9312 multiplexer will be coincidental and COMPARE OUT will be high. The COMPARE ENABLE must be low to permit compare operation.

3 BIT COMPARATOR



INTERCONNECTION DIAGRAM FOR 9 BITS

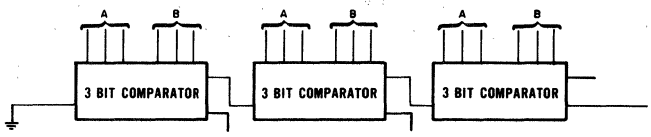


Fig. 18

IMPLEMENTING ANY FOUR-VARIABLE BOOLEAN FUNCTION

The 9312 eight input multiplexer can (in addition to performing its nominal function) produce any Boolean function of four variables without any additional elements if both the assertion and negation of one of the variables are present. If an assertion and negation are not present, one inverter may be required.

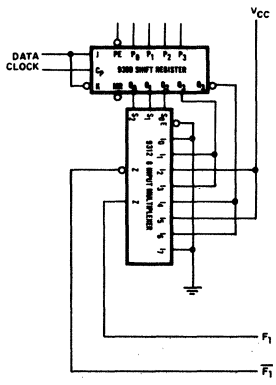
The procedure for implementing a four-variable function, along with an example, is shown in the attached diagram. First, consider the function in terms of a Karnaugh map. If the Q_0, Q_1 and Q_2 variable are connected to the S_0, S_1 and S_2 inputs of the 9312 then the Karnaugh map will be split, as shown, into eight sections, with each section corresponding to an input to the 9312. In order to implement the function each input of the 9312 is connected to one of the following four signals: ground, V_{CC}, the assertion, or negation of the fourth variable.

The contents of the two squares associated with an input, on the Karnaugh map, determine which connection is made to that input. If both squares contain a zero, ground should be connected to the input; if both squares contain a one, the input should be connected to V_{CC}. If the two squares contain a one and a zero then either the assertion or negation of the fourth variable will be required to implement the function. If the single one is located in the square associated with the assertion of the fourth variable then the assertion of the assertion of the fourth variable is connected to that input, and vice versa.

Shown in the illustration below is a 9312 decoding the condition of a 9300, producing a one output whenever the register contains two or more transitions. The truth table, Karnaugh map and the connection to the 9312 for this function are also shown in the illustration.

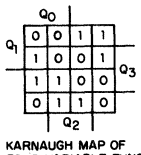
In many applications, using the 9312 to implement general logic functions of four variables will result in a sizeable reduction in package count. In many cases use of the 9312 with additional gates to produce functions of more than four variables will also reduce the package count.

The concept of using the 9312 eight input-multiplexer as a general logic function generator is described by S. S. Yau and C. K. Tang of Northwestern University in a paper presented at the 1968 Spring Joint Computer Conference in Atlantic City, New Jersey.

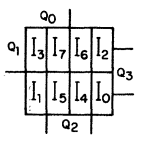


Q_0	Q_1	Q_2	Q_3	F_1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

TRUTH TABLE



KARNAUGH MAP OF FOUR VARIABLE FUNCTION.



MULTIPLEXER INPUT MAP FOR $S_0=Q_0$, $S_1=Q_1$, $S_2=Q_2$

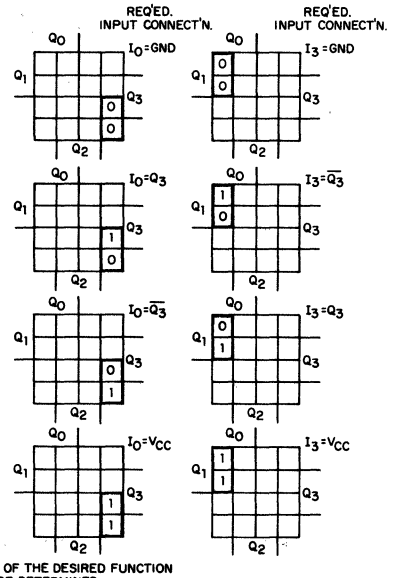


Fig. 19 FROM THE KARNAUGH MAP OF THE DESIRED FUNCTION I_0-I_7 CONNECTIONS CAN BE DETERMINED.

9316

MSI 4-BIT BINARY COUNTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9316 is a high speed synchronous 4-bit binary decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES:

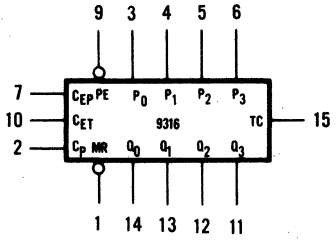
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **TYPICAL POWER DISSIPATION OF 300 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC HERMETIC 16 PIN DUAL IN-LINE PACKAGE AND FLAT PACKAGE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify U6B9316XXX for 16-pin Dual In-Line Package, U3L9316XXX for 16-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

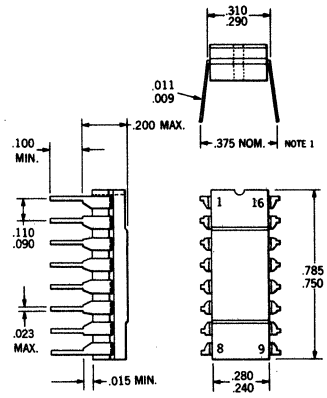
LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

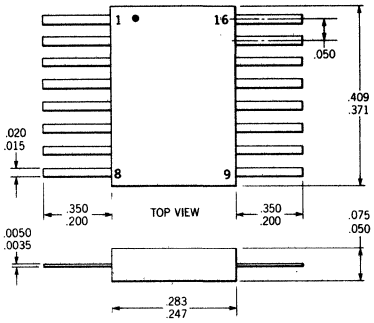
PHYSICAL DIMENSIONS

DUAL IN-LINE PACKAGE



NOTE:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

FLAT PACKAGE



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

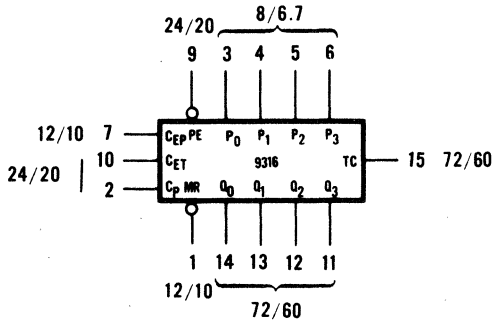
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of CEP or CET from high to low or of PE from low to high may only be done when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics." The asynchronous MR clears the counter independent of any other input.

Note: CE (count enable) = CEP • CET
TC = CET • Q_0 • Q_1 • Q_2 • Q_3

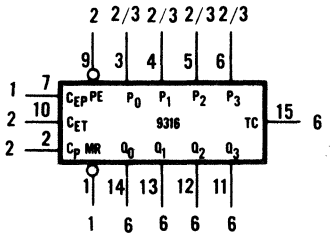
LOADING RULES

CCSL LOAD AND DRIVE FACTORS



Vcc = Pin 16
Gnd = Pin 8

TTμL LOAD AND DRIVE FACTORS



Vcc = Pin 16
Gnd = Pin 8

(1 U.L. = 1 TTμL input gate load)

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 9.6 mA V_{CC} = 4.5 V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
2 I_F	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
⅔ I_F	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
2 I_R	Input Leakage Current CP, PE, CET		120		20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V
⅔ I_R	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE, CET		120		20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		15		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		35		ns	
t_{pd-} (TC)	Turn-On Delay for TC		20		ns	
t_s (SE)	Set-Up Time for CE		14		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig.2)
t_r (CE)	Release Time for CE		12		ns	
t_s	Set-Up Time for Data		18		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 3)
t_r	Release Time for Data		17		ns	
t_s (PE)	Set-Up Time for PE		30		ns	
t_r (PE)	Release Time for PE		28		ns	
t_{pd-} (MR)	Turn-On Delay for MR		33		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 4)
$t_{p\pm}$	Propagation Delay for CET to TC		14		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 5)

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

Fig. 1

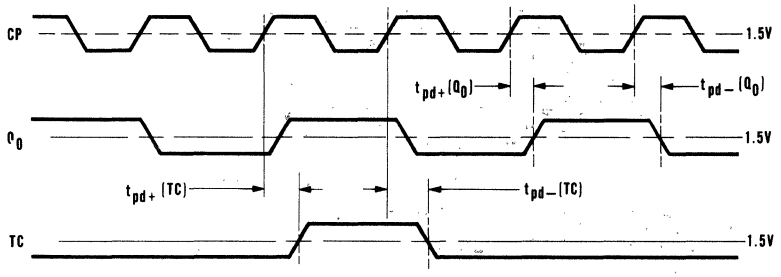


Fig. 2

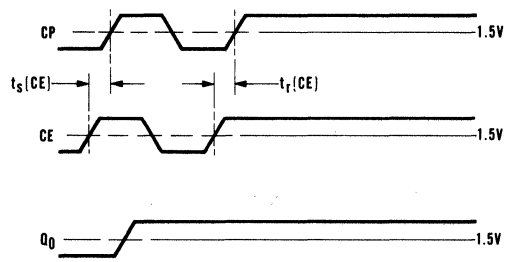


Fig. 3

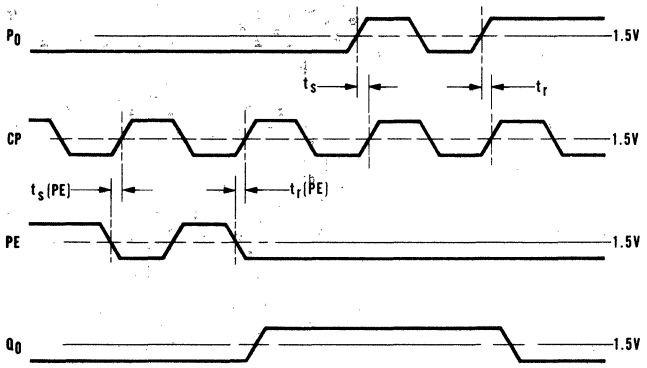


Fig. 4

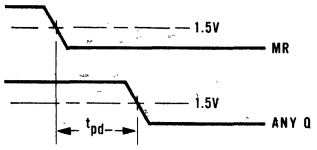
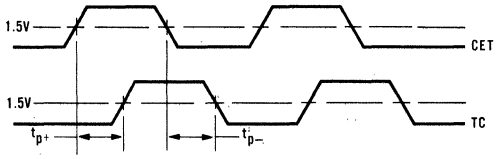
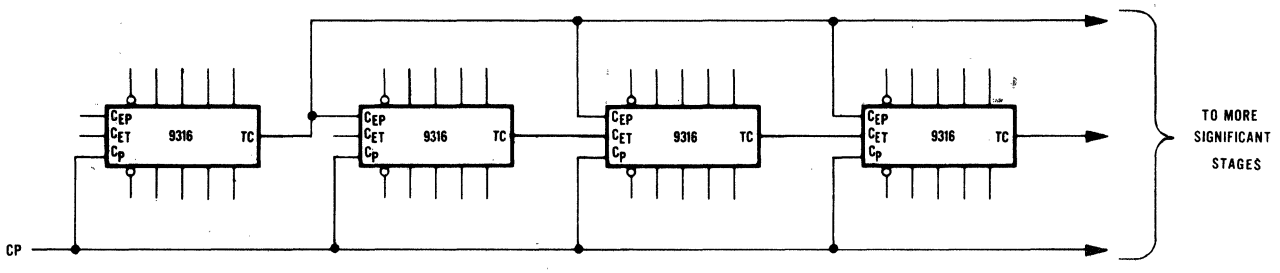


Fig. 5



APPLICATIONS



SYNCHRONOUS COUNTING SCHEME

TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD *COMPATIBLE CURRENT SINKING LOGIC* PRODUCT

MILITARY TEMPERATURE RANGE: −55°C to +125°C

GENERAL DESCRIPTION

The Fairchild 9000 Series of TTμL circuits is designed to be used in any digital system where good noise immunity, high speed, medium power and high fan-out performance is required. The line is characterized by a broad number of functions available in a variety of packages. The basic elements of the family are active low level output AND gates commonly known as NAND gates.

Typical high level noise immunity of every device in the family is 1.9 V and typical low level noise immunity is 0.9 V. Worst case immunity is 400 mV over the entire temperature range. Power dissipation is typically 11 mW per gate function at a 50% duty cycle, and the average propagation delay is 7 nanoseconds per gate function. A single 5 V ±10 per cent power supply is used with the circuits.

The gates were designed to provide low output impedance in both high and low states which results in good capacitive drive capability and good immunity to crosstalk. The output impedance in the low state is about 10 ohms and in the high state, about 20 ohms. To further enhance noise immunity, all inputs of all devices incorporate diode clamps which considerably reduces the ringing which can result from long lines and impedance mismatches. The binary elements are of a JK, DC master slave design and will toggle at 40 MHz, except for the 9000 element. The 9000 has capacitors purposely incorporated in the design to increase its set-up time and provide it with considerable immunity to long clock skew. Due to the longer set-up time the 9000 toggle frequency is 20 MHz. A common JK input is incorporated on all binary elements to provide data entry inhibit/enable. The input to the clock on each element is buffered to reduce the clock input loading.

The V_{CC} and ground terminals of all devices are located on diagonal corners of the package which allows two degrees of freedom in routing of power and ground leads on the PC boards. Special care has been taken in establishing pin-outs for the flip-flop so as to minimize cross-overs when laying out common dynamic functions with these elements. Simple loading rules are incorporated so that the fan-in and fan-out capability of each device will be quickly established.

The 9000 series TTμL is part of the CCSL family and is compatible with all other Fairchild DTμL, Low Power DTμL and MSI devices as well as the more complex functions which will be available in the future.

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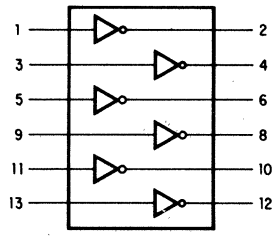
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

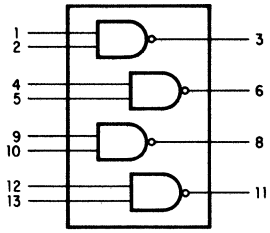
9000 SERIES TTμL INTEGRATED CIRCUITS

NAND GATES

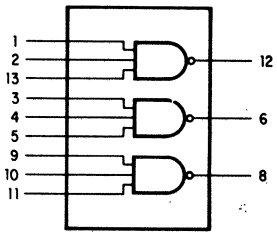
9016



9002

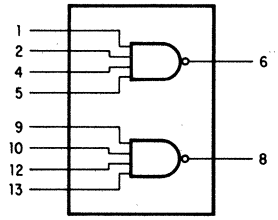


9003

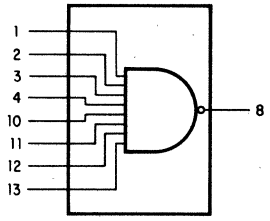


NAND GATES

9004

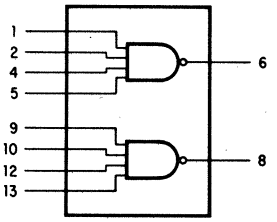


9007



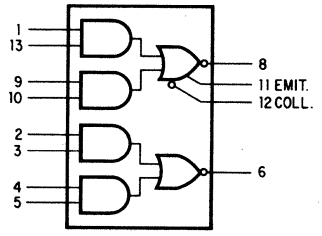
BUFFER

9009

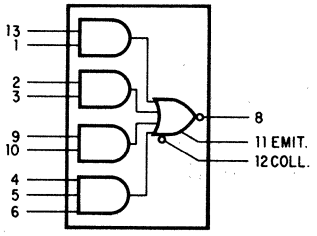


AND-OR-INVERT GATES AND EXTENDER

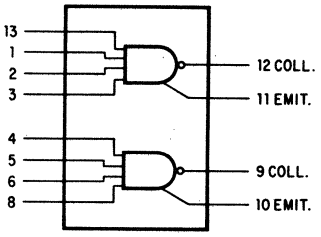
9005



9008



9006



V_{CC} = Pin 14
Gnd = Pin 7

(extender for use with 9005 & 9008)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (D.C.) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Output Voltage, Output Normally High	0 V to +V_{CC} value
Current Into Output Terminal, Output Low (except 9009)	50 mA
Current Into Output Terminal, Output Low 9009	100 mA

NOTE 1

The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 2 V_{BE}'s below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

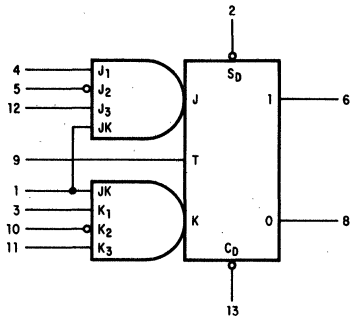
NOTE 2

Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

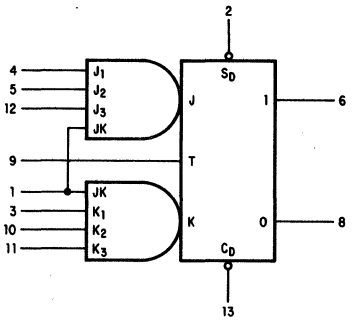
9000 SERIES TTμL INTEGRATED CIRCUITS

SINGLE FLIP-FLOPS

9000



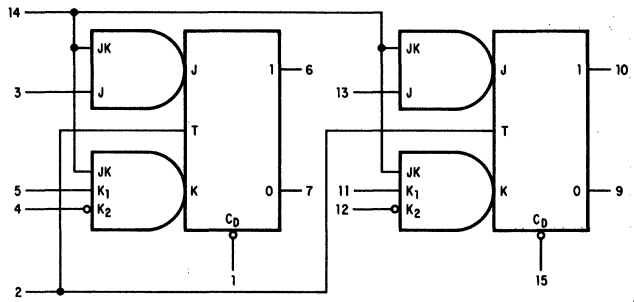
9001



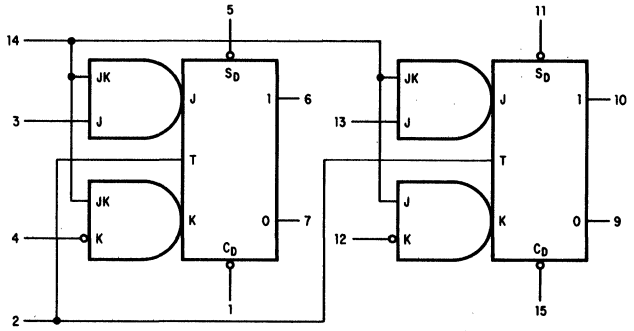
VCC = Pin 16
Gnd = Pin 8

DUAL FLIP-FLOPS

9020



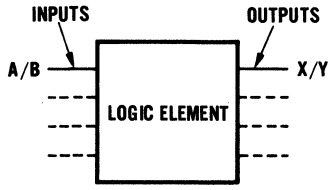
9022



VCC = Pin 14
Gnd = Pin 7

LOADING RULES

In this data sheet the following notation has been chosen to indicate the input loading and output drive for all logic elements.



Where
- A = high logic level input load factor
- B = low logic level input load factor
- X = high logic level output drive factor
- Y = low logic level output drive factor

When checking for loading violations it is only necessary to insure that the sum of the high logic level input load factors at any node does not exceed the high logic level output drive factor at that node. The same is true for low logic level load and drive factors. These rules apply only within the TTμL 9000 series. For loading rules to other Fairchild logic elements refer to the CCSL Composite Data Sheet.

Multiplying the factor with the appropriate current per unit load gives the input loading or output drive in terms of current. For the TTμL circuits of this data sheet, current per unit is −1.6 mA maximum at the low logic level and is 60 μA maximum at the high logic level.

In the case where unused inputs of an AND gate are shorted to a driven input, the high logic level input load factor for the inputs will be the number of inputs shorted together times the high logic input load factor for one input. The low logic level input load factor for the inputs will be the same as that for a single input.

UNUSED INPUTS

Proper termination of unused inputs will result in maximum operating speed. Substantial degradation of turn-on delay may occur if unused inputs are left open.

The following are acceptable ways to terminate unused inputs:

1. Tie the input to a used input on the same gate. The TTμL 9000 series has made special provision for this method by offering extra high level drive factor on all outputs.
2. Tie the input to V_{CC} through a resistor. This resistor should be chosen to keep the input current within absolute maximum ratings for any possible extreme of the V_{CC} supply. More than one input may be terminated through one resistor.
3. Tie inputs to a separate supply between 4.5 and 2.4 V, if one should be available.
4. Tie the inputs to the output of an unused gate. The unused gate must provide a constant high level output.

NAND GATES—9002, 9003, 9004 AND 9007
HEX INVERTER — 9016

The 9002, 9003, 9004 and 9007 are active low level output AND gates commonly known as NAND gates. The 9016 is a hex inverter with input and output characteristics identical to the 9002, 9003, 9004 and 9007. The variety of gate combinations provides the system designer the utmost in logic flexibility and reduces package count.

Figure 1—LOGIC SYMBOL AND PIN CONFIGURATIONS

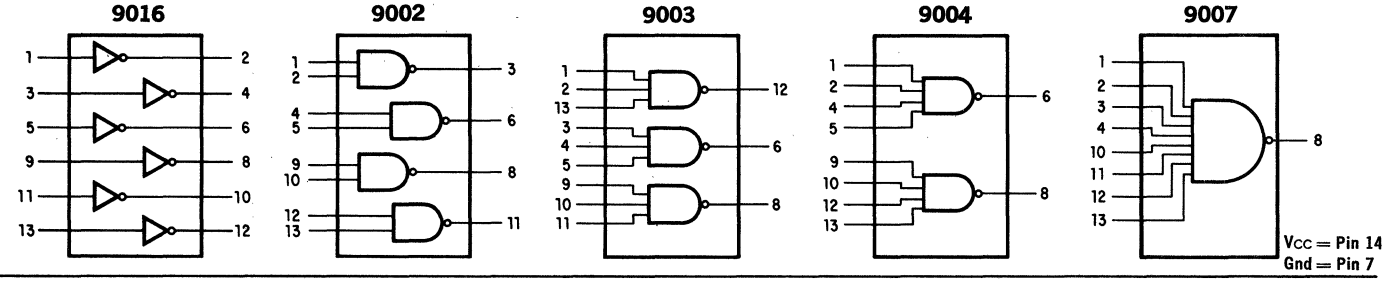
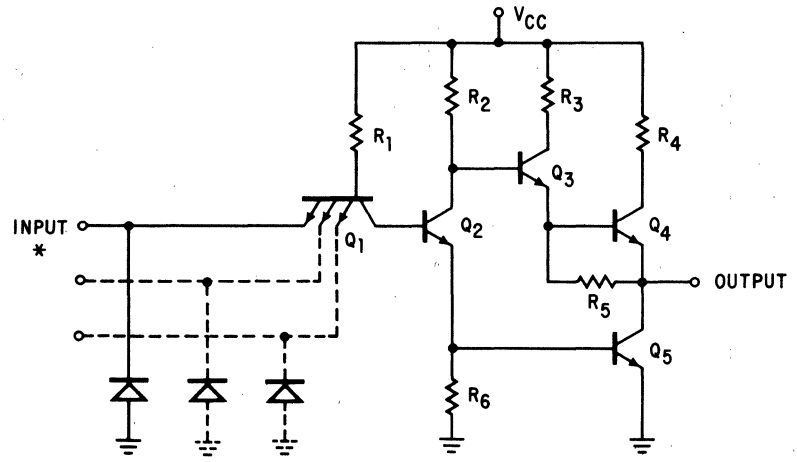


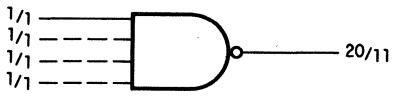
Figure 2—BASIC GATE CIRCUIT



Nominal Resistor Values
$R_1 = R_5 = 4.0\ k\Omega$
$R_2 = 1.5\ k\Omega$
$R_3 = 150\ \Omega$
$R_4 = 80\ \Omega$
$R_6 = 1.25\ k\Omega$

*Number of inputs depends on the gate.

Figure 3—LOADING FACTORS



ELECTRICAL CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016 ($T_A = -55°C$ to $125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.32\ mA$ Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 17.6\ mA$ $V_{IH} = 5.5\ V$
										$V_{CC} = 4.5\ V$ $I_{OL} = 13.6\ mA$ Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			−1.24		−0.87	−1.24		−1.24		$V_{CC} = 4.5\ V$ 5.5 V on other inputs
I_R	Input Leakage Current				10	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		5.5		3.5	5.5		5.5	mA	$V_{CC} = 5.0\ V$ Inputs high
	V_{CC} Current, Gate Off (each gate)		1.6		1.07	1.6		1.6		$V_{CC} = 5.0\ V$ Inputs at gnd
t_{pd+}	Switching Speed				3.0	10			ns	$V_{CC} = 5.0\ V$, See Figure 12
t_{pd-}	Switching Speed				3.0	12			ns	$C_L = 15\ pF$

9002, 9003, 9004, 9007 AND 9016
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

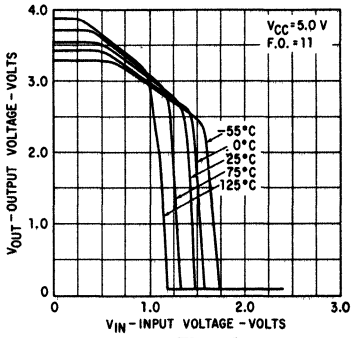


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

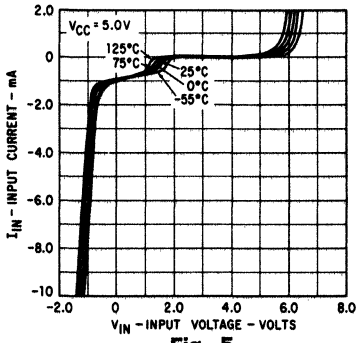


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

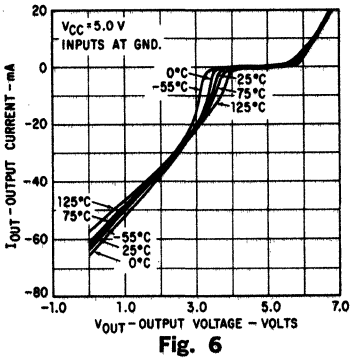


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

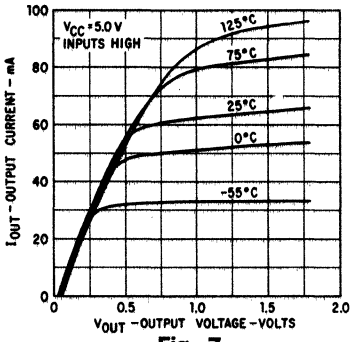


Fig. 7

POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

POWER DISSIPATION VERSUS SUPPLY VOLTAGE

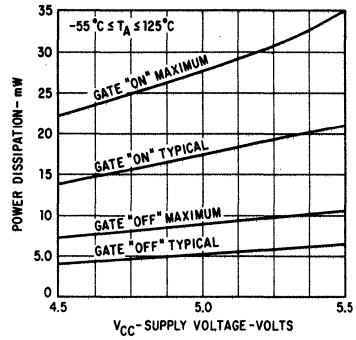


Fig. 8

WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

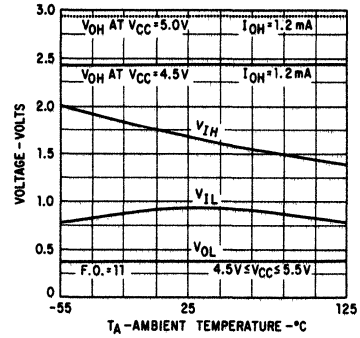


Fig. 9

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

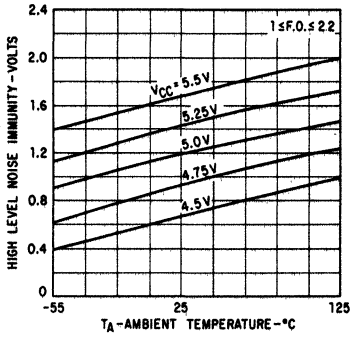


Fig. 10

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

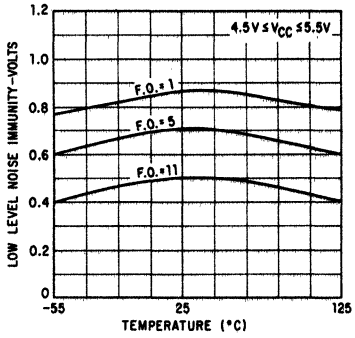
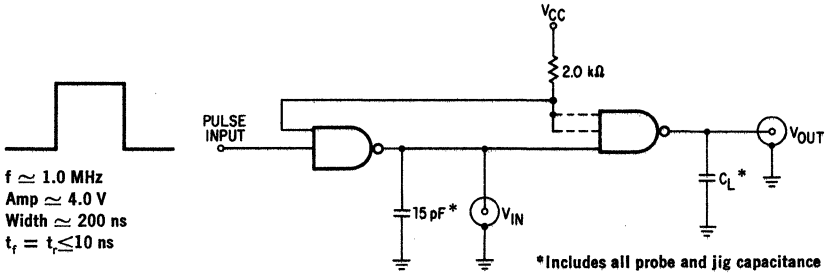


Fig. 11

SWITCHING CHARACTERISTICS

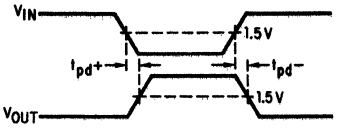
Fig. 12

tpd TEST CIRCUIT



f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

SWITCHING WAVEFORM



WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

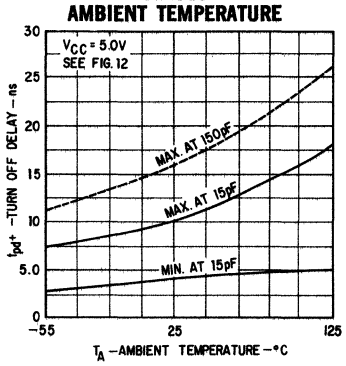


Fig. 13

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

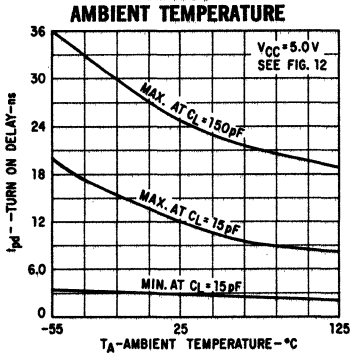


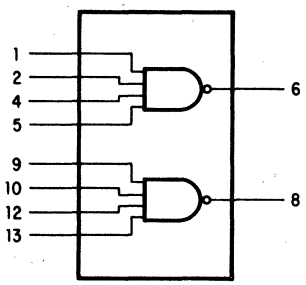
Fig. 14

NAND BUFFER — 9009

The 9009 is a power gate capable of sinking and sourcing large currents for high fanout applications. Logically it is the same as the 9004.

Figure 1

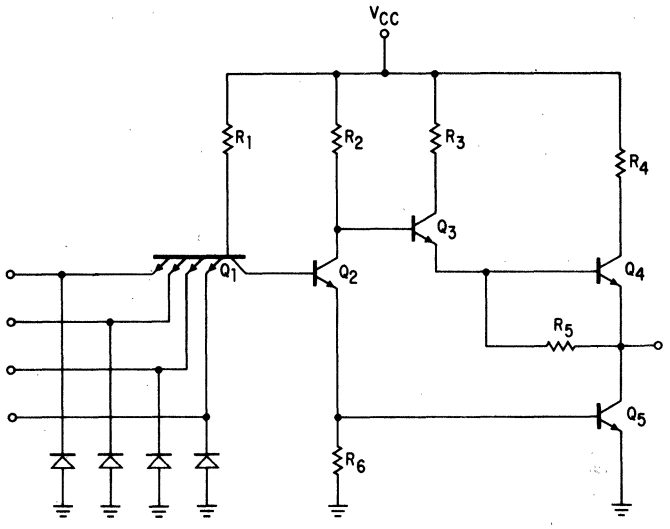
LOGIC DIAGRAM AND PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

Figure 2

CIRCUIT DIAGRAM (One Gate)

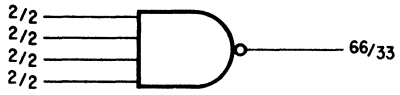


Nominal Resistor Values

R_1 = 2.0 kΩ	R_4 = 50 Ω
R_2 = 560 Ω	R_5 = 4.0 kΩ
R_3 = 150 Ω	R_6 = 500 Ω

Figure 3

LOADING FACTORS



ELECTRICAL CHARACTERISTICS 9009 (T_A = −55°C to 125°C, V_{CC} = 5.0 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = −3.96 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 52.8 mA V_{IH} = 5.5 V
										V_{CC} = 4.5 V I_{OL} = 40.8 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−3.2		−2.2	−3.2		−3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
			−2.48		−1.74	−2.48		−2.48		V_{CC} = 4.5 V 5.5 V on other inputs
I_R	Input Leakage Current				20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		12.9		8.6	12.9		12.9	mA	V_{CC} = 5.0 V Inputs high
	V_{CC} Current, Gate Off (each gate)		3.2		2.15	3.2		3.2		V_{CC} = 5.0 V Inputs grounded
t_{pd+}	Switching Speed				4.0	15			ns	V_{CC} = 5.0 V, See Figure 12
t_{pd-}	Switching Speed				3.0	10			ns	C_L = 15 pF

9009

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

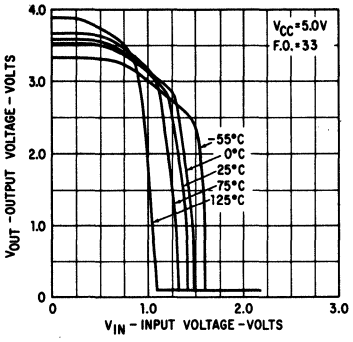


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

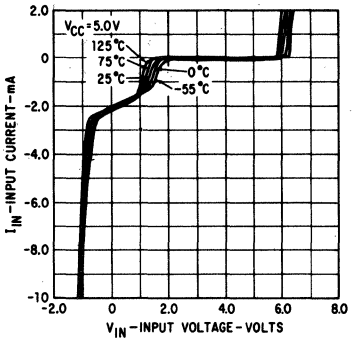


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

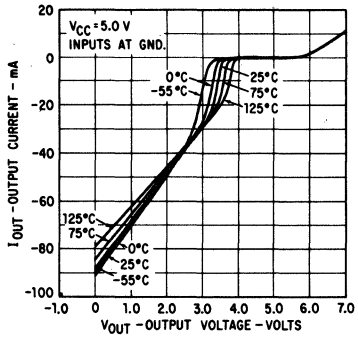


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

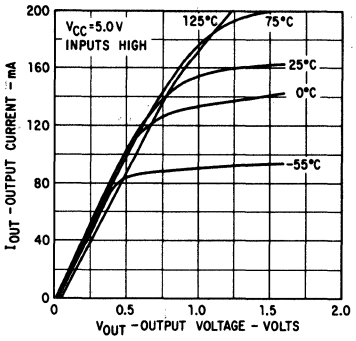


Fig. 7

POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

POWER DISSIPATION VERSUS SUPPLY VOLTAGE

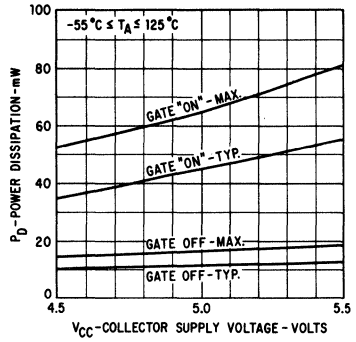


Fig. 8

WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

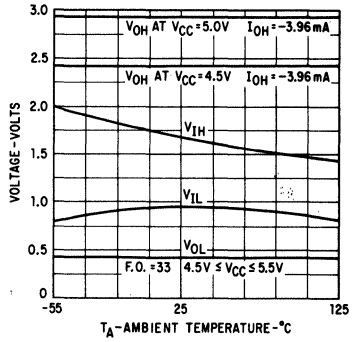


Fig. 9

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

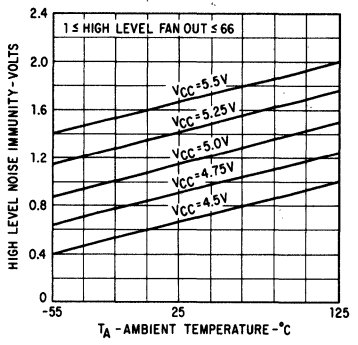


Fig. 10

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

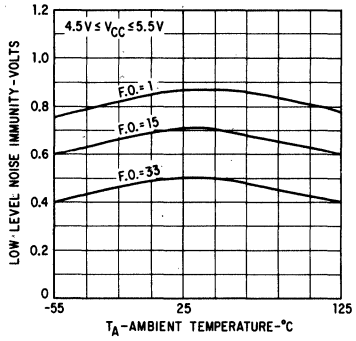
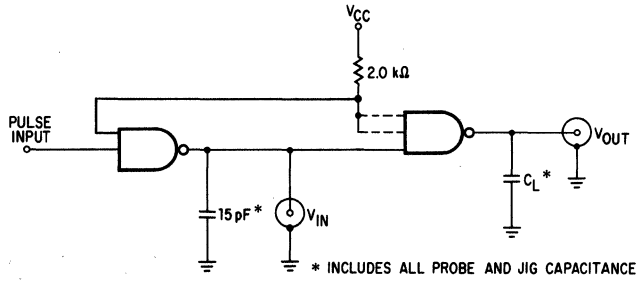


Fig. 11

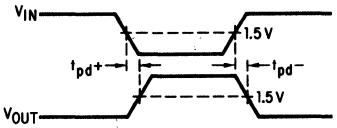
SWITCHING CHARACTERISTICS

Fig. 12

tpd TEST CIRCUIT



SWITCHING WAVEFORM



f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_f = t_r \leq 10$ ns

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

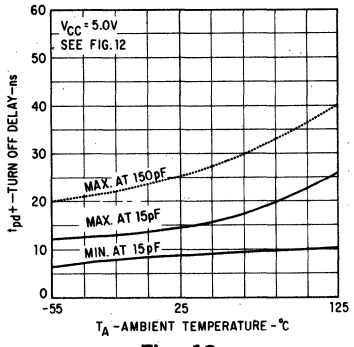


Fig. 13

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

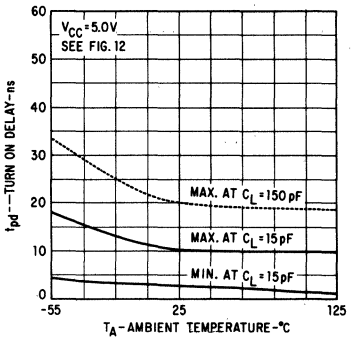


Fig. 14

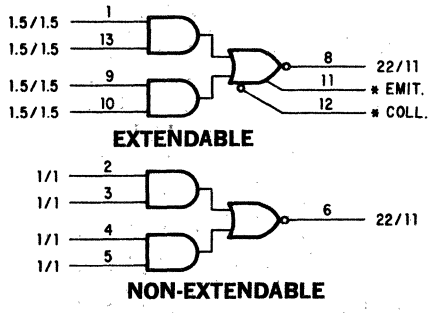
EXTENDABLE AND-OR-INVERT GATES—9005, 9008
EXTENDER—9006

The TTμL 9005 and 9008 are AND-OR-INVERT gates which may be OR extended with the use of the 9006. For noise immunity and operating level curves, refer to the gate section on Page 4 and 5.

Figure 1—LOGIC DIAGRAMS AND LOADING FACTORS

The numbers by each input and output give the input loading and output drive capability. For complete explanation see Page 3.

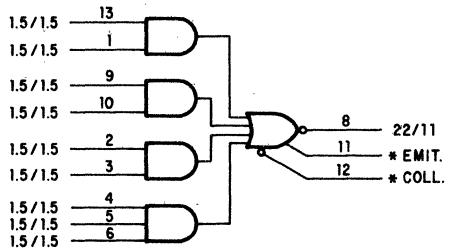
9005



*Four Extenders (9006) may be tied to these terminals

V_{CC} = Pin 14
Gnd = Pin 7

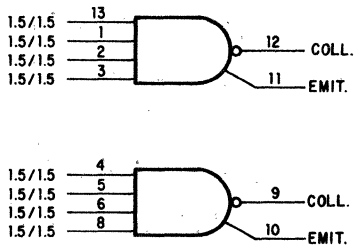
9008



*Four Extenders (9006) may be tied to these terminals

V_{CC} = Pin 14
Gnd = Pin 7

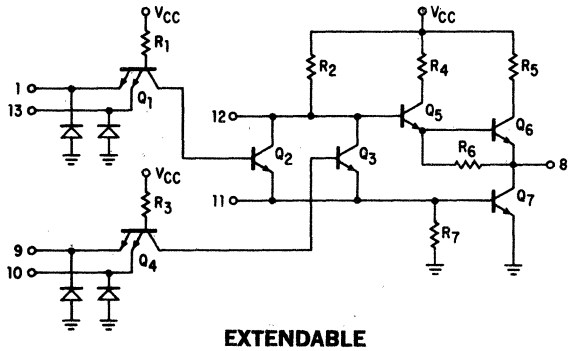
9006

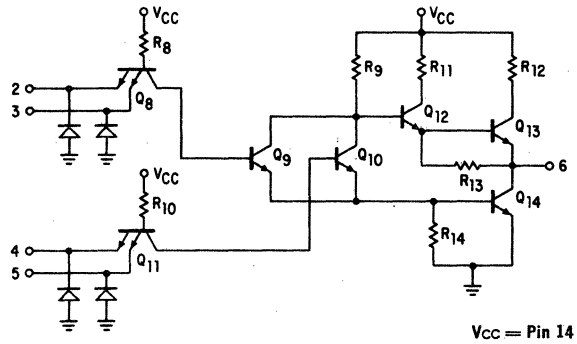


V_{CC} = Pin 14
Gnd = Pin 7

Figure 2—CIRCUIT DIAGRAMS

9005



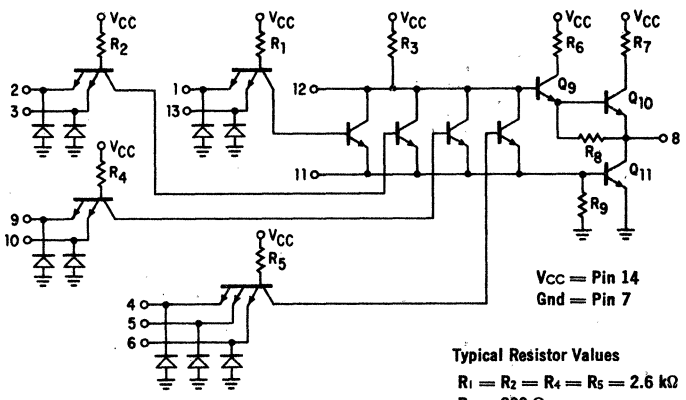


V_{CC} = Pin 14
Gnd = Pin 7

Typical Resistor Values

$R_1 = R_3 = 2.6\ k\Omega$
$R_2 = 800\ \Omega$
$R_4 = R_{11} = 150\ \Omega$
$R_5 = R_{12} = 80\ \Omega$
$R_6 = R_8 = R_{10} = R_{13} = 4.0\ k\Omega$
$R_7 = 665\ \Omega$
$R_9 = 1.5\ k\Omega$
$R_{14} = 1.25\ k\Omega$

9008

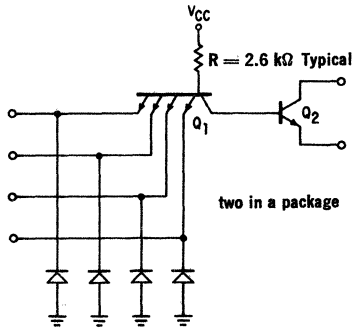


V_{CC} = Pin 14
Gnd = Pin 7

Typical Resistor Values

$R_1 = R_2 = R_4 = R_5 = 2.6\ k\Omega$
$R_3 = 800\ \Omega$
$R_6 = 150\ \Omega$
$R_7 = 80\ \Omega$
$R_8 = 4.0\ k\Omega$
$R_9 = 665\ \Omega$

9006



V_{CC} = Pin 14
Gnd = Pin 7

ELECTRICAL CHARACTERISTICS 9005, 9006 AND 9008 ($T_A = -55°C$ to $125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.32\ mA$ V_{IL} = value indicated below on this table	
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 17.6\ mA$ $V_{IH} = 5.5\ V$	
										$V_{CC} = 4.5\ V$ $I_{OL} = 13.6\ mA$ V_{IH} (see below)	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs	
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$	$V_F = 0.4\ V$, 5.5 V on other inputs
	9005 Nonextendable Gate		−1.24		−0.87	−1.24		−1.24		$V_{CC} = 4.5\ V$	
	Input Load Current		−2.4		−1.5	−2.4		−2.4	μA	$V_{CC} = 5.5\ V$	
	Extendable Gate and Extender		−1.86		−1.31	−1.86		−1.86		$V_{CC} = 4.5\ V$	
I_R	Input Leakage Current 9005 Nonextendable Gate				5.0	60		60	mA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$	Gnd on all other inputs
	Input Leakage Current Extendable Gate and Extender				7.5	90		90			
I_{PD}	V_{CC} Current, Gate "ON" 9005 Nonextendable Gate		6.5		4.5	6.5		6.5	mA	$V_{CC} = 5.0\ V$	All inputs open
	9005 Extendable Gate		11.3		7.6	11.3		11.3			
	9008		12.5		9.3	12.5		12.5			
	V_{CC} Current, Gate "OFF" 9005 Nonextendable Gate		3.1		2.1	3.1		3.1	mA	$V_{CC} = 5.0\ V$	All inputs except extender inputs gnd.
	9005 Extendable Gate		4.7		3.3	4.7		4.7			
	9008		9.4		6.6	9.4		9.4			
ΔI_{PD}	Extra Current Drain from one 9006 Extender Gate "ON"		1.61		1.08	1.61		1.61	mA	$V_{CC} = 5.0\ V$ All inputs high 9006 attached to a 9005	
	Extra Current Drain from one 9006 Extender Gate "OFF"		2.35		1.65	2.35		2.35	mA	$V_{CC} = 5.0\ V$ All inputs grounded 9006 attached to a 9005	

Note: Output characteristics apply to a 9005 (both gates) or a 9008.
Input characteristics apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

9005, 9006, 9008
TYPICAL INPUT-OUTPUT CHARACTERISTICS
(EXTENDABLE GATES*)

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

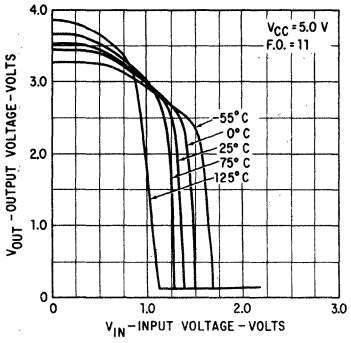


Fig. 3

INPUT CURRENT VERSUS INPUT VOLTAGE

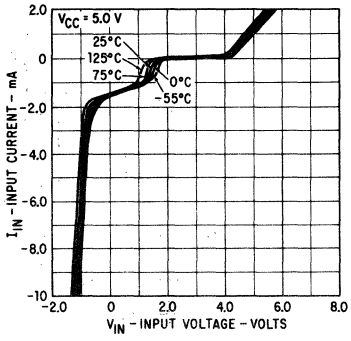


Fig. 4

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

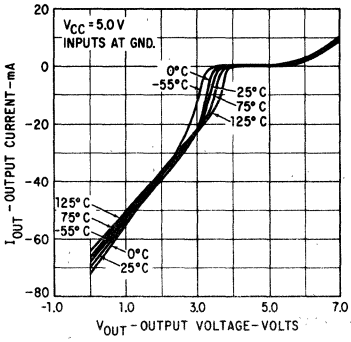


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

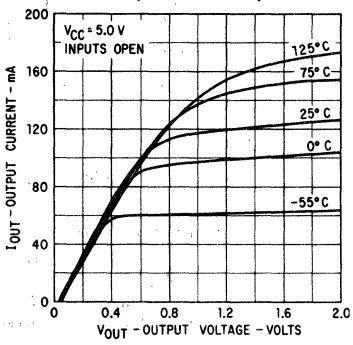


Fig. 6

*Curves on Page 5 apply to 9005 nonextendable gate.

9601

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The TTμL 9601 is a DC level sensitive retriggerable monostable multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components only. The 9601 has excellent immunity to noise on the V_{CC} and ground lines. The 9601 uses TTμL for high speed and high fanout capability and is compatible with all devices in the CCSL family of integrated circuits.

FEATURES:

- **50 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **COMPLEMENTARY D.C. LEVEL SENSITIVE INPUTS**
- **COMPLEMENTARY OUTPUTS**
- **CCSL COMPATIBLE**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (D.C.) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is High	0 V to +V_{CC} value
Current Into Output When Output is Low	50 mA

ORDER INFORMATION:

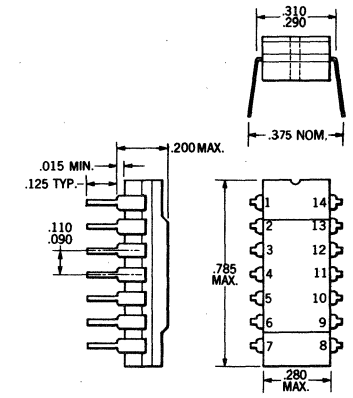
Specify U3I96015XX for flat package and U6A96015XX for Dual-In-Line package, where 5XX is 51X for −55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

NOTES:

1) The maximum Vcc value of 8.0 volts is not the primary factor in determining the maximum Vcc which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the Vcc voltage, so the primary limit on the Vcc is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system Vcc to approximately 7.0 volts.
2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

PHYSICAL DIMENSIONS

Similar to JEDEC (TO-116) Outline



TYPICAL FLAT PACKAGE
(Top View)

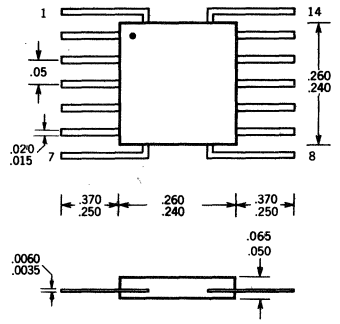
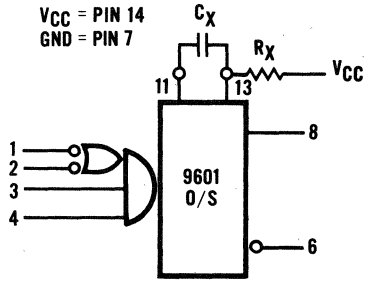


Fig. 1

LOGIC DIAGRAM



NOTE: All dimensions in inches

Fig. 2

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

J-K FLIP-FLOPS-9000, 9001
DUAL J-K FLIP-FLOPS-9020, 9022

GENERAL DESCRIPTION

The TTμL 9000 series has four flip-flops to satisfy the storage requirements of a logic system. All are master-slave JK designs and have the same high speed and high noise immunity as the rest of the 9000 series. As with the gates, all inputs have diode clamps to further enhance the noise immunity.

The JK type flip-flop was chosen for all flip-flop elements in this family because of its inherent logic power. The input function required to produce a given sequency of states for a JK flip-flop will, in general, contain more "don't care" conditions than the corresponding function for an RS flip-flop. These additional "don't care" conditions will, in most cases, reduce the amount of gating elements required to implement the input function.

The master-slave design offers the advantage of a DC threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

Data is accepted by the master while the clock is in the low state. Refer to the truth table for definition of "ONE" and "ZERO" data. Transfer from the master to the slave occurs on the low to high transition of the clock. When the clock is high, the J and K inputs are inhibited.

A joint (JK) input is provided for all flip-flops in this family. This common input removes the necessity of gating the clock signal with an external gate in many applications. This not only reduces package count, but also reduces the possibility of clock skew problems, since with internal gating provided, all flip-flops may be driven from a common clock line. Several TTμL drivers may be used in parallel to drive this common clock line, if the load exceeds the F.O. capability of the 9009 buffer.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided on all flip-flops except the 9020, which because of a logic trade-off has only clear inputs. The set or clear pin being low absolutely guarantees that one output will be high, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the low output may momentarily spike high synchronous with a positive transition of the clock. If the low output of the flip-flop is connected to other flip-flop inputs clocked from the same line, the spike will be masked by the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur. When the spikes can cause problems, a simple solution is to common the joint JK inputs with the synchronous set or reset signal.

Figure 1—LOGIC DIAGRAMS AND LOADING FACTORS

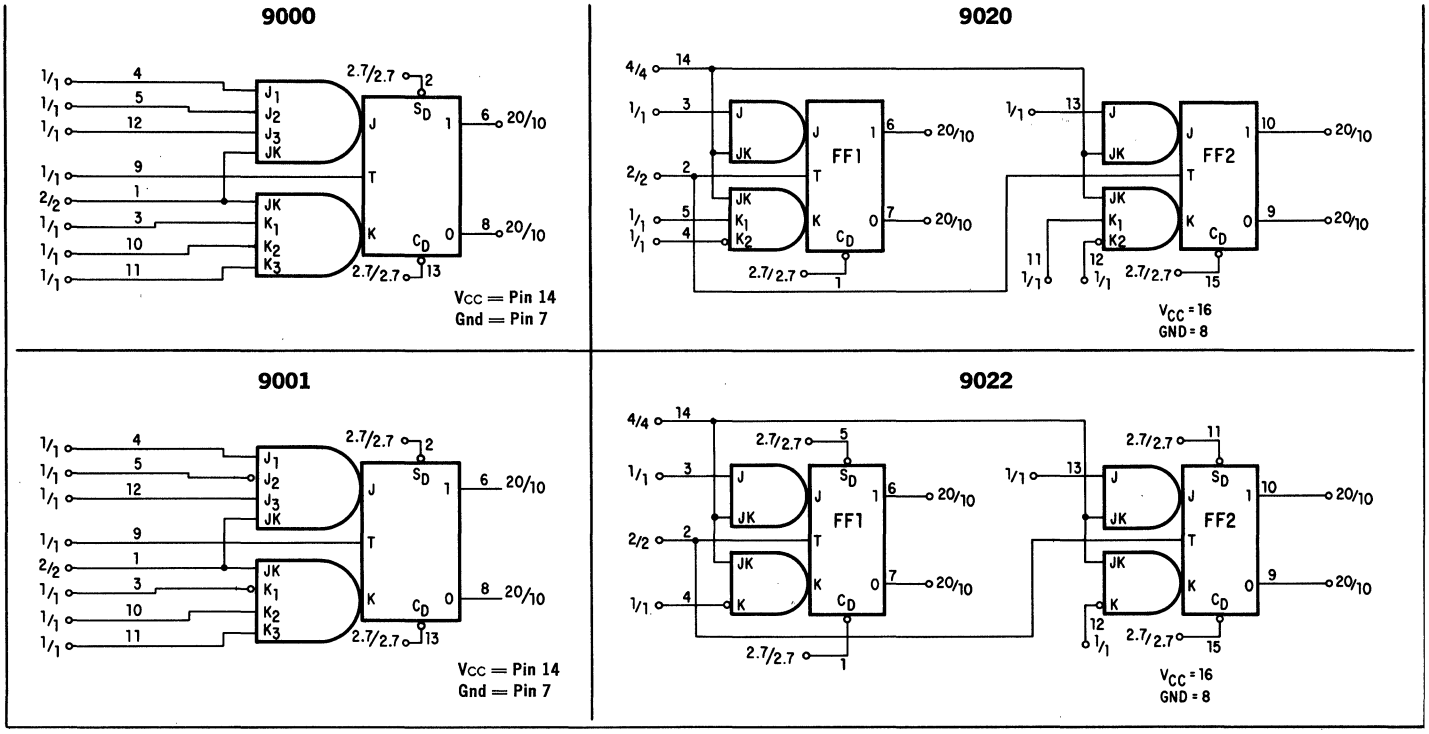
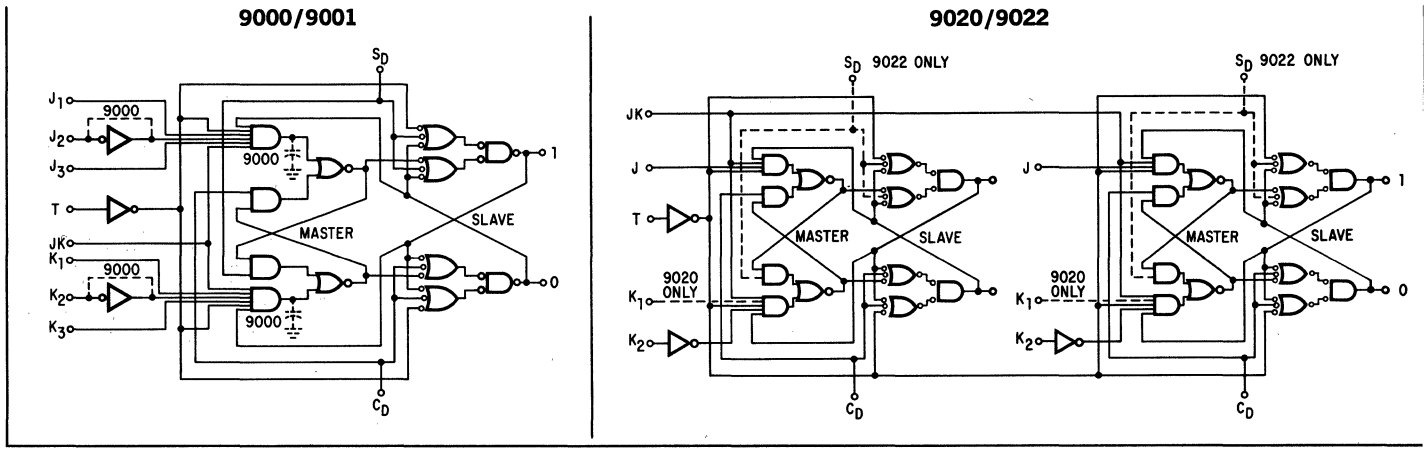


Figure 2—FUNCTIONAL LOGIC DIAGRAMS



TRUTH TABLES

SYNCHRONOUS OPERATION

BEFORE CLOCK OUTPUTS		BEFORE CLOCK INPUTS		OUTPUTS AFTER CLOCK	
ONE	ZERO	J	K	ONE	ZERO
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
S_D	C_D	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	SYNCHRONOUS INPUTS CONTROL	

SYNCHRONOUS OPERATION

The truth table defines the next state of the flip-flop after a low-to-high transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table.

The J and K inputs in the table refer to the basic flip-flop J and K inputs as indicated on the logic diagrams. These internal inputs are for every flip-flop the result of a logic operation on the external J and K inputs. This operation is represented symbolically by AND gates in the logic diagram for each flip-flop. Logic diagrams are in accordance with MIL Standard 806B.

The L* symbol in the J and K input column is defined as meaning that **input does not go high at any time while the clock is low.**

The H* symbol in the J or K input column is defined as meaning that the **input has been high at some time while the clock was low.**

The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state high and low voltage levels, respectively.

UNUSED INPUTS

The 9001, 9020 and 9022 all have active level low synchronous inputs. When not in use they must be grounded. All other unused inputs including asynchronous should be tied high for maximum operating speed. Use one of the methods recommended on Page 3.

ELECTRICAL CHARACTERISTICS 9000, 9001, 9020 AND 9022 ($T_A = -55°C$ to $125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$	$I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 4.5\ V$ $V_{CC} = 5.5\ V$	$I_{OL} = 12.4\ mA$ $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.	
I_R	Input Leakage										
	All J, K inputs; T inputs 9000, 9001				5.0	60		60	μA	$V_{CC} = 5.5\ V$	$V_R = 4.5\ V$
	J, K inputs 9000, 9001; T inputs 9020, 9022				10	120		120		Gnd. on other inputs.	
	JK inputs 9020, 9022				20	240		240			
	S_D, C_D (all flip-flops)				14	160		160			
I_F	Input Current										
	All J, K inputs; T inputs 9000, 9001		−1.60		−1.1	−1.60		−1.60	mA	$V_{CC} = 5.5\ V$	$V_F = 0.4\ V$
	J, K inputs 9000, 9001; T inputs 9020, 9022		−3.20		−2.2	−3.20		−3.20			5.5 V Gnd on other inputs
	JK inputs 9020, 9022		−6.40		−4.4	−6.40		−6.40			
	S_D, C_D (all flip-flops)		−4.32		−2.97	−4.32		−4.32			
I_F	Input Current										
	All J, K inputs; T inputs 9000, 9001		−1.24		−0.87	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$	
	J, K inputs 9000, 9001; T inputs 9020, 9022		−2.48		−1.74	−2.48		−2.48			
	JK inputs 9020, 9022		−4.96		−3.48	−4.96		−4.96			
	S_D, C_D (all flip-flops)		−3.35		−2.35	−3.75		−3.35			
I_{PD}	V_{CC} Current										
	9000		24		13	24		24	mA	S_D at gnd	$V_{CC} = 5.0\ V$
	9001		28		14	28		28		S_D at gnd	
	9020, 9022		27		14	27		27		C_{D1}, C_{D2} at gnd	
	each flip-flop										

TYPICAL INPUT AND OUTPUT CHARACTERISTICS
9000, 9001, 9020 AND 9022

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS

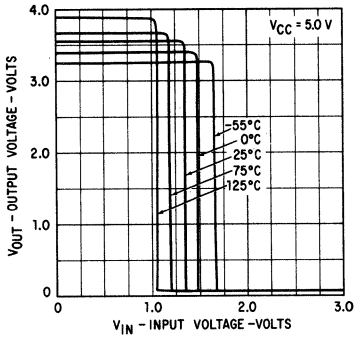


Fig. 3

CLOCK OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

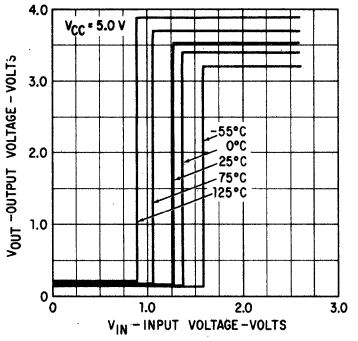


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE 9004

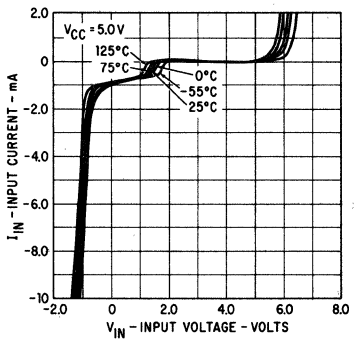


Fig. 5

INPUT CURRENT VERSUS INPUT VOLTAGE 9009

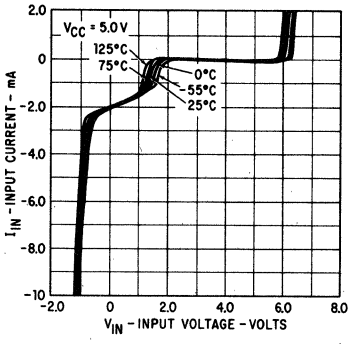


Fig. 6

INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9000, 9001

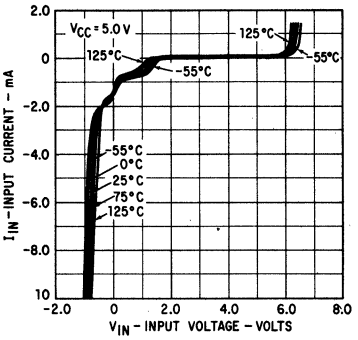


Fig. 7

INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9020, 9022

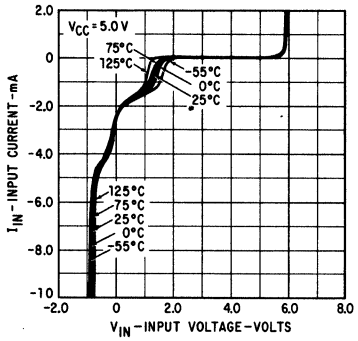


Fig. 8

INPUT CURRENT VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS — ALL FLIP-FLOPS

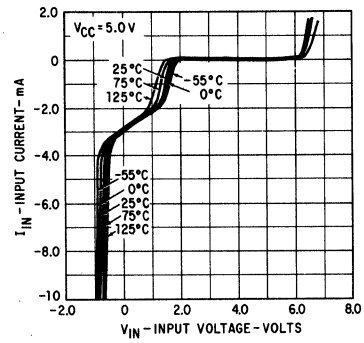


Fig. 9

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

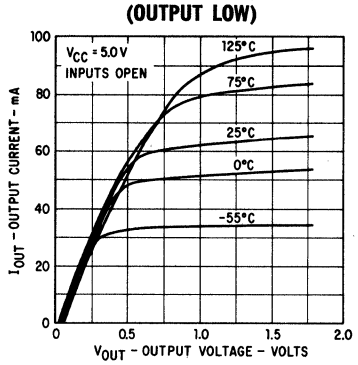


Fig. 10

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = C_l = 15 pF of all flip-flops unless otherwise noted)

CHARACTERISTICS				MIN.	TYP.	MAX.	UNITS	FIGURES
t_{pd+}	Clock-to-Output				12	20	ns	16, 17, 18
	S_D or C_D-to-Output				12	20	ns	16, 17, 18
t_{pd-}	Clock-to-Output				20	30	ns	16, 17, 18
	S_D or C_D-to-Output				25	35	ns	16, 17, 18
t_{set-up}	J, K or JK		9000 Only	30	22		ns	16, 18
	Data Entry			10	8.0		ns	16, 17, 18
	$\overline{J}$ or $\overline{K}$ Data Entry			17	12		ns	16, 17, 18
$t_{release}$	J, K or JK		9000 Only		18	12	ns	16, 18
	Data Entry				7.0	1.0	ns	16, 17, 18
	J or K Data Entry				11	4.0	ns	16, 17, 18
Pulse Widths	Clock	9000 Only	Positive		20		ns	16, 18
			Negative		25		ns	16, 18
			Positive		8.0		ns	16, 17, 18
			Negative		10		ns	16, 17, 18
	S_D or C_D		Negative		25		ns	16, 17, 18
Toggle Frequency			9000 Only		20		MHz	16, 18
					50		MHz	16, 17, 18

MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE T TO OUTPUT

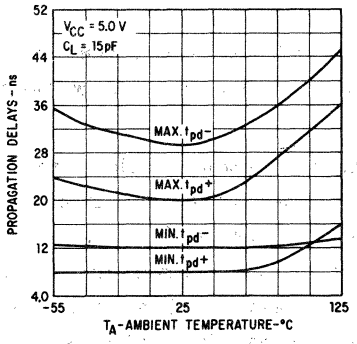


Fig. 11

MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE ASYNCHRONOUS INPUTS TO OUTPUTS

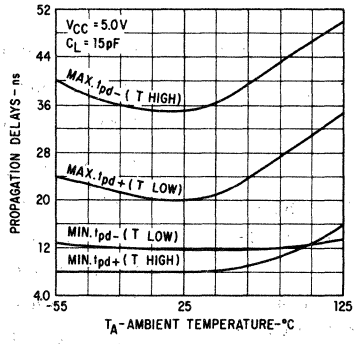


Fig. 12

INCREASE IN ASYNCHRONOUS OR CLOCK INPUT DUE TO OUTPUT CAPACITANCE

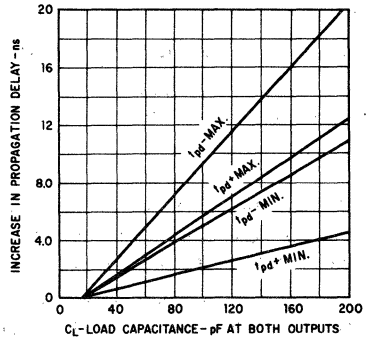


Fig. 13

9001-9020-9022 SET-UP/RELEASE TIME AND NEGATIVE CLOCK PULSE WIDTH VERSUS AMBIENT TEMPERATURE

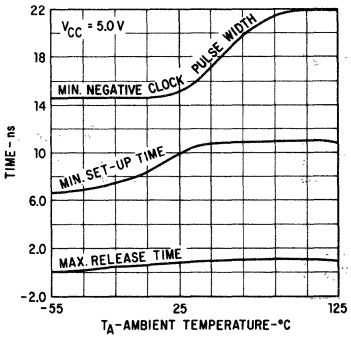


Fig. 14

9000 NEGATIVE CLOCK PULSE WIDTH SET-UP/RELEASE TIME VERSUS AMBIENT TEMPERATURE

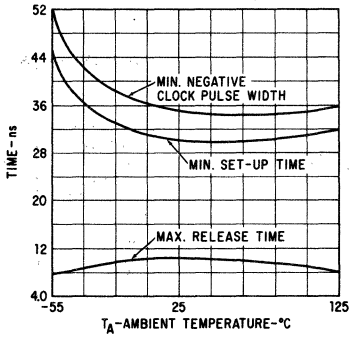
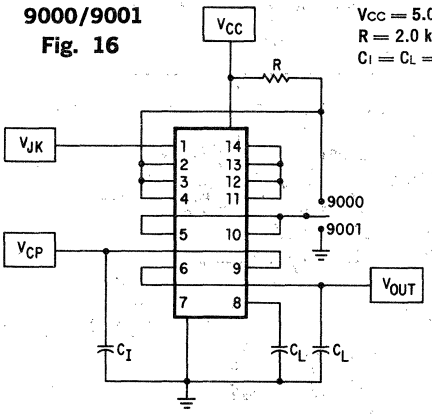


Fig. 15

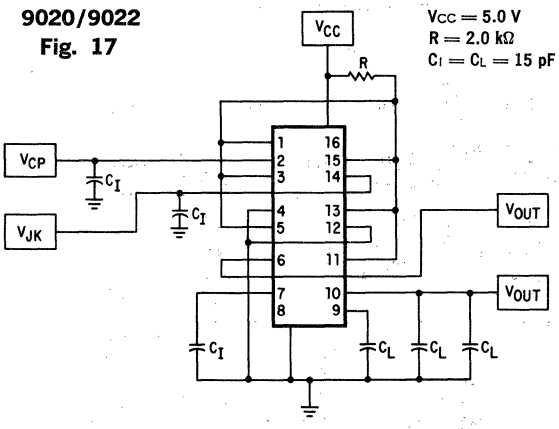
SWITCHING TEST CIRCUITS

9000/9001
Fig. 16



V_{CC} = 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

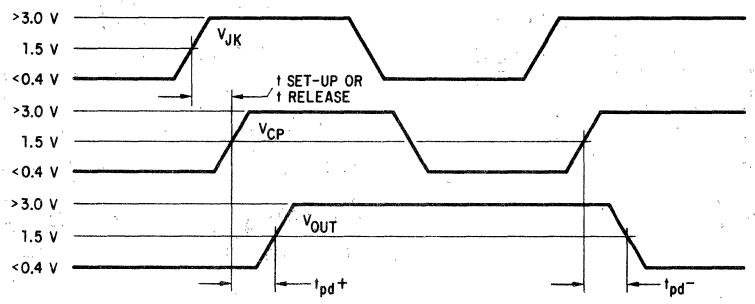
9020/9022
Fig. 17



V_{CC} = 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

Fig. 18

WAVEFORMS



SWITCHING TEST NOTES

t_{pd+} and t_{pd-}

1. V_{JK} should be kept at the high logic level when performing t_{pd} tests.
2. Drive the clock pulse input with a suitable pulse source. t_{pd+} and t_{pd-} delays are as defined in the waveforms.

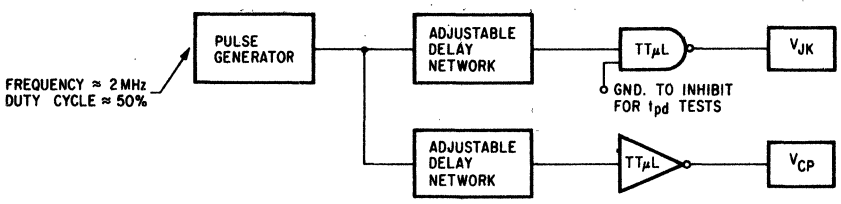
$t_{set\text{-}up}$

1. $t_{set\text{-}up}$ is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the low state of the clock in order for the flip-flop to respond to the data.
2. The test for $t_{set\text{-}up}$ is performed by adjusting the timing relationship between the V_{CP} and V_{JK} inputs to the $t_{set\text{-}up}$ minimum value. A device that passes the test will have the output waveform shown. The output of a device that does not pass the $t_{set\text{-}up}$ test will remain at a static logic level (no switching will occur).

$t_{release}$

1. $t_{release}$ is defined as the maximum time allowed for a HIGH to be present at a synchronous logic input at any time during the low state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

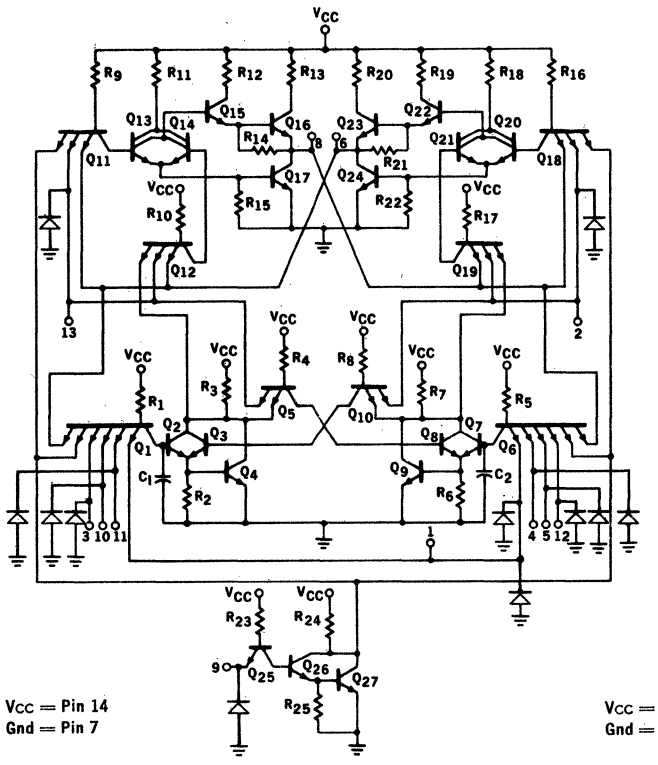
RECOMMENDED INPUT PULSE SOURCES



DTμL9932 gates with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

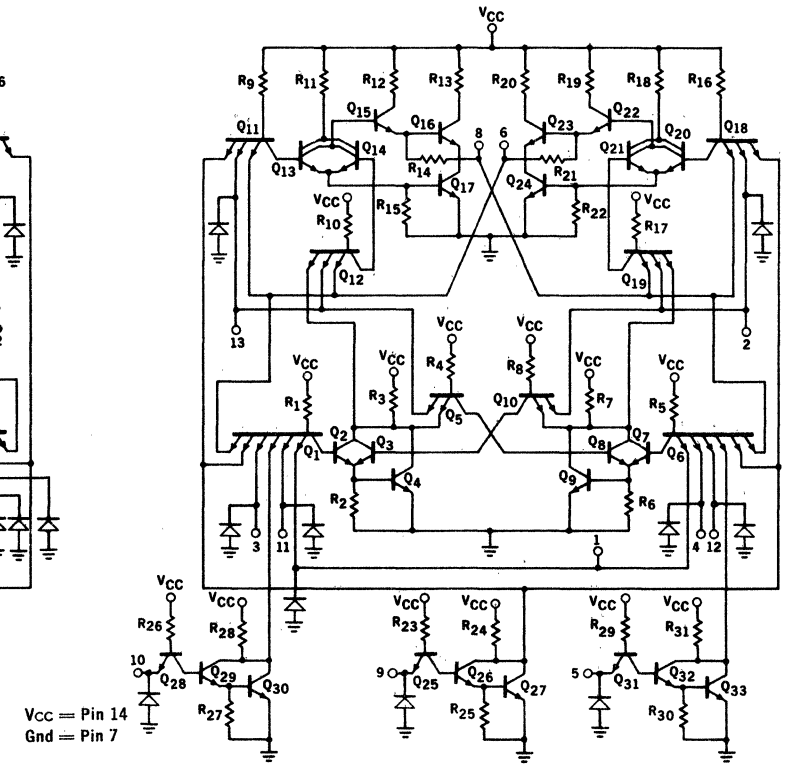
9000 SCHEMATIC DIAGRAM

For resistor values, see page 16

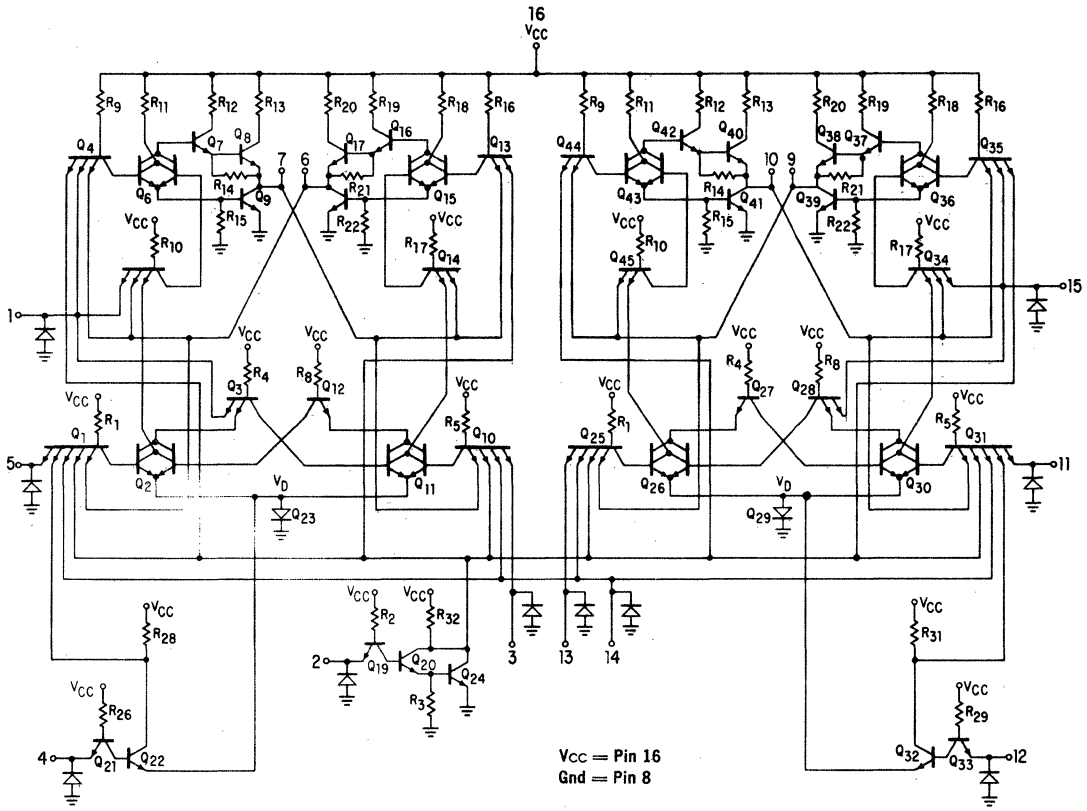


9001 SCHEMATIC DIAGRAM

For resistor values, see page 16



9020 SCHEMATIC DIAGRAM

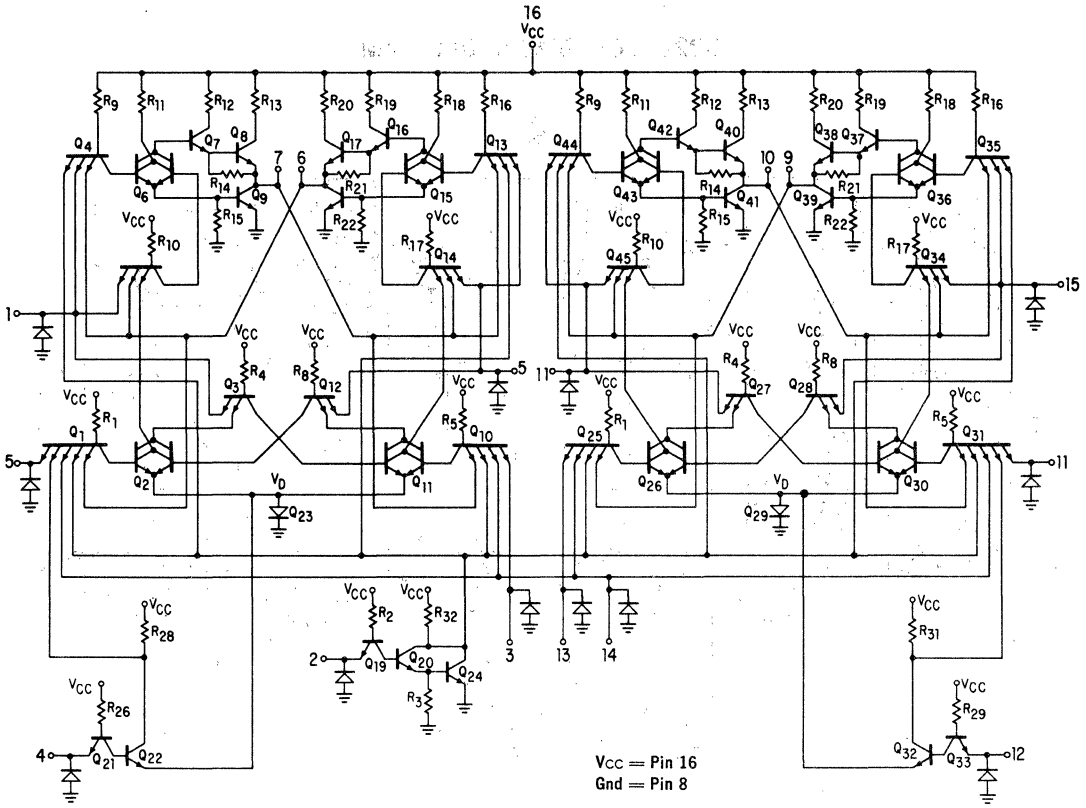


NOMINAL COMPONENT VALUES (ALL FLIP-FLOPS)

R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4.0 kΩ
R_2, R_3, R_6, R_7 = 2.0 kΩ
R_9, R_{16}, R_{28}, R_{31} = 6.0 kΩ
R_{11}, R_{18} = 1.5 kΩ
R_{12}, R_{19} = 150 Ω
R_{13}, R_{20} = 80 Ω
R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25 kΩ
R_{32} = 1.0 kΩ
C_1, C_2 = 10 pF

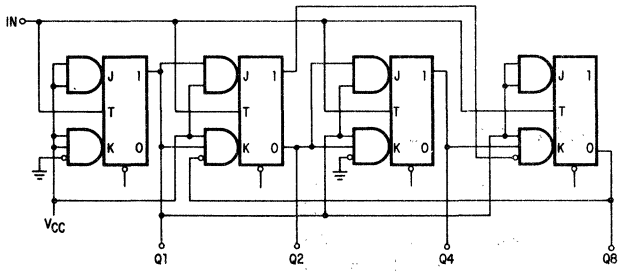
9022 SCHEMATIC DIAGRAM

For resistor values see table on page 16



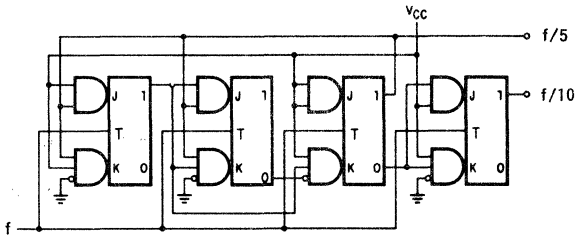
APPLICATIONS

SYNCHRONOUS BCD COUNTER



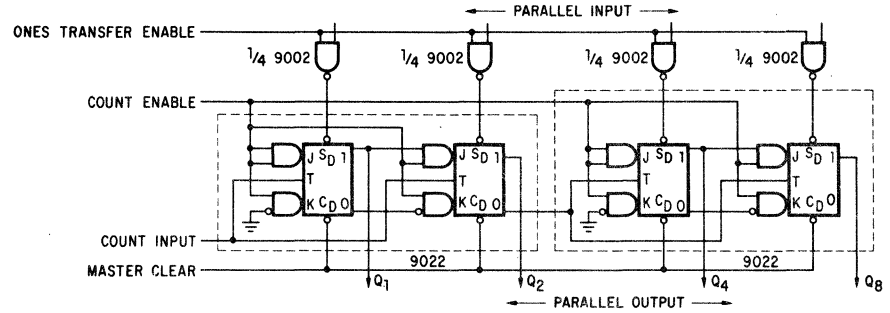
Two TTμL 9020 Dual Flip-Flops require no additional gating to produce a fully synchronous 8421 code BCD Counter.

DIVIDE BY TEN COUNTER



Two TTμL 9020 Dual Flip-Flops require no additional gating elements to produce divide by ten circuit with a square wave divide by ten output and a divide by five output.

BINARY COUNTER WITH ASYNCHRONOUS PARALLEL LOAD AND CLEAR

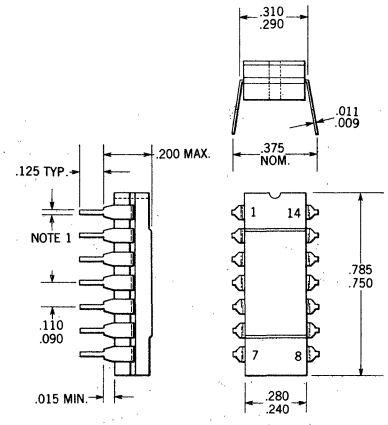


Binary counter using synchronous 2 bit stages with trickle down between stages illustrates method of utilizing dual JK flip-flops having common clocks in counter applications.

PACKAGE OUTLINES

U6A

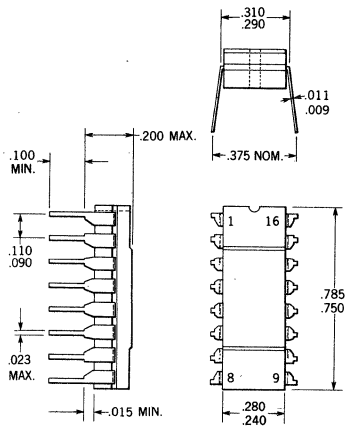
PHYSICAL DIMENSIONS
SIMILAR TO
JEDEC (TO-116) Outline
Dual In-Line Package



NOTE: 1. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

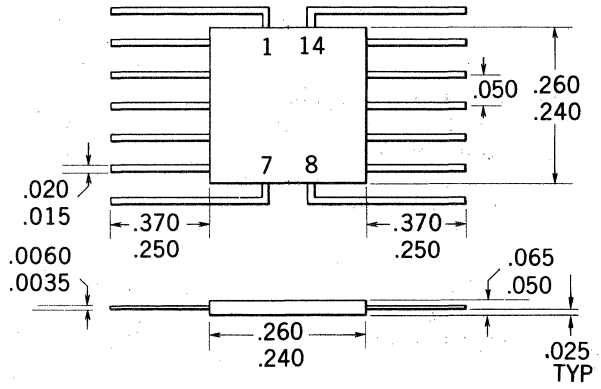
U6B

PHYSICAL DIMENSIONS
16 Lead Dual In-Line



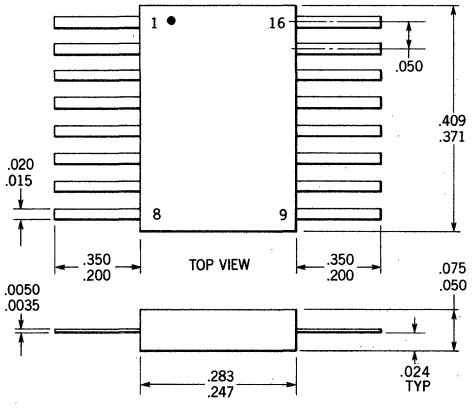
U3I

CERPAK 14 LEAD



U3L

CERPAK 16 LEAD



ORDER INFORMATION

To order Transistor-Transistor Micrologic elements specify

U3IXXXX51X for 14-pin Flat package
U6AXXXX51X for 14-pin Dual In-Line package
U3LXXXX51X for 16-pin Flat package
U6BXXXX51X for 16-pin Dual In-Line package

Where XXXX is the four-digit number denoting the specific element desired and 51X is for −55°C to +125°C temperature.

TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD *COMPATIBLE CURRENT SINKING LOGIC* PRODUCT

TEMPERATURE RANGE: 0°C to 75°C

GENERAL DESCRIPTION

The Fairchild 9000 Series of TTμL circuits is designed to be used in any digital system where good noise immunity, high speed, medium power and high fan-out performance is required. The line is characterized by a broad number of functions available in a variety of packages. The basic elements of the family are active low level output AND gates commonly known as NAND gates.

Typical high level noise immunity of every device in the family is 1.9 V and typical low level noise immunity is 0.9 V. Worst case immunity is 400 mV over the entire temperature range. Power dissipation is typically 11 mW per gate function at a 50% duty cycle, and the average propagation delay is 7 nanoseconds per gate function. A single 5 V ±5 per cent power supply is used with the circuits.

The gates were designed to provide low output impedance in both high and low states which results in good capacitive drive capability and good immunity to crosstalk. The output impedance in the low state is about 10 ohms and in the high state, about 20 ohms. To further enhance noise immunity, all inputs of all devices incorporate diode clamps which considerably reduces the ringing which can result from long lines and impedance mismatches. The binary elements are of a JK, DC master slave design and will toggle at 40 MHz, except for the 9000 element. The 9000 has capacitors purposely incorporated in the design to increase its set-up time and provide it with considerable immunity to long clock skew. Due to the longer set-up time the 9000 toggle frequency is 20 MHz. A common JK input is incorporated on all binary elements to provide data entry inhibit/enable. The input to the clock on each element is buffered to reduce the clock input loading.

The V_{CC} and ground terminals of all devices are located on diagonal corners of the package which allows two degrees of freedom in routing of power and ground leads on the PC boards. Special care has been taken in establishing pin-outs for the flip-flop so as to minimize cross-overs when laying out common dynamic functions with these elements. Simple loading rules are incorporated so that the fan-in and fan-out capability of each device will be quickly established.

The 9000 series TTμL is part of the CCSL family and is compatible with all other Fairchild DTμL, Low Power DTμL and MSI devices as well as the more complex functions which will be available in the future.

TABLE OF CONTENTS

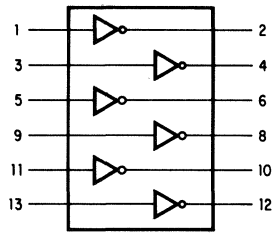
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

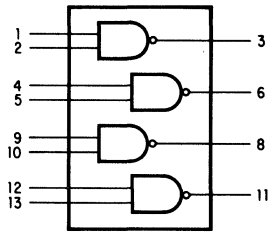
9000 SERIES TTμL INTEGRATED CIRCUITS

NAND GATES

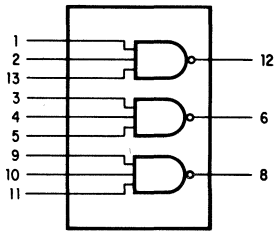
9016



9002

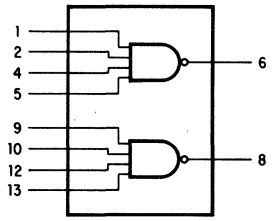


9003

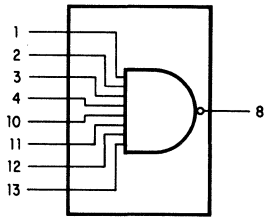


NAND GATES

9004

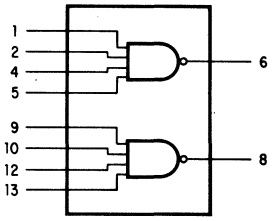


9007



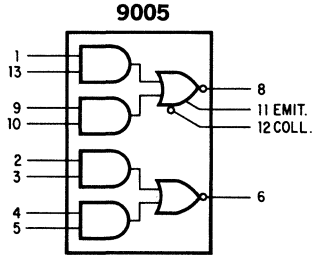
BUFFER

9009

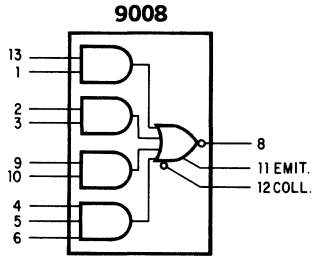


AND-OR-INVERT GATES AND EXTENDER

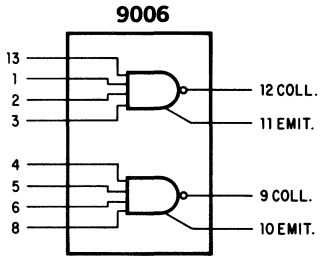
9005



9008



9006



Vcc = Pin 14
Gnd = Pin 7

(extender for use with 9005 & 9008)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (D.C.) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Output Voltage, Output Normally High	0 V to +V_{CC} value
Current Into Output Terminal, Output Low (except 9009)	50 mA
Current Into Output Terminal, Output Low 9009	100 mA

NOTE 1

The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 2 V_{BE}'s below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

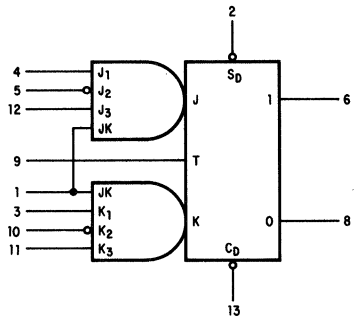
NOTE 2

Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

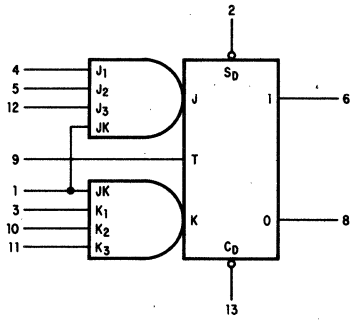
9000 SERIES TTμL INTEGRATED CIRCUITS

SINGLE FLIP-FLOPS

9000



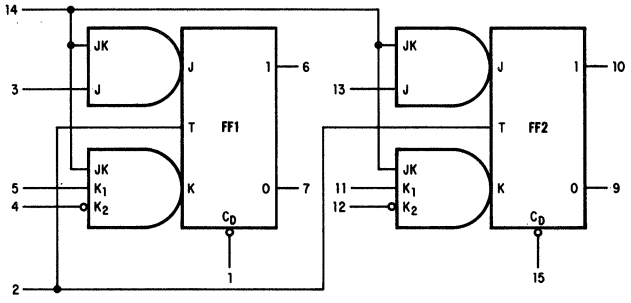
9001



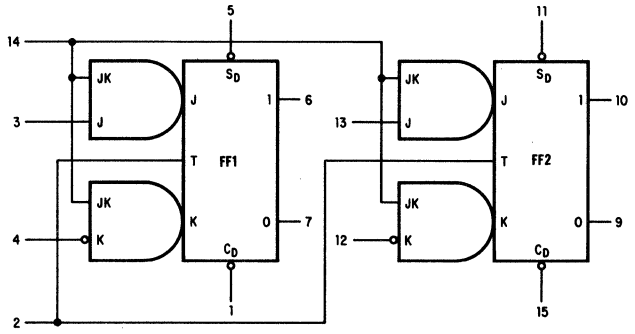
VCC = Pin 14
Gnd = Pin 7

DUAL FLIP-FLOPS

9020



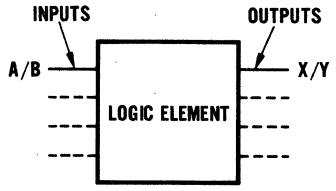
9022



VCC = Pin 16
Gnd = Pin 8

LOADING RULES

In this data sheet the following notation has been chosen to indicate the input loading and output drive for all logic elements.



Where
- A = high logic level input load factor
- B = low logic level input load factor
- X = high logic level output drive factor
- Y = low logic level output drive factor

When checking for loading violations it is only necessary to insure that the sum of the high logic level input load factors at any node does not exceed the high logic level output drive factor at that node. The same is true for low logic level load and drive factors. These rules apply only within the TTμL 9000 series. For loading rules to other Fairchild logic elements refer to the CCSL Composite Data Sheet.

Multiplying the factor with the appropriate current per unit load gives the input loading or output drive in terms of current. For the TTμL circuits of this data sheet, current per unit load is −1.6 mA maximum at the low logic level and is 60 μA maximum at the high logic level.

In the case where unused inputs of an AND gate are shorted to a driven input, the high logic level input load factor for the inputs will be the number of inputs shorted together times the high logic input load factor for one input. The low logic level input load factor for the inputs will be the same as that for a single input.

UNUSED INPUTS

Proper termination of unused inputs will result in maximum operating speed. Substantial degradation of turn-on delay may occur if unused inputs are left open.

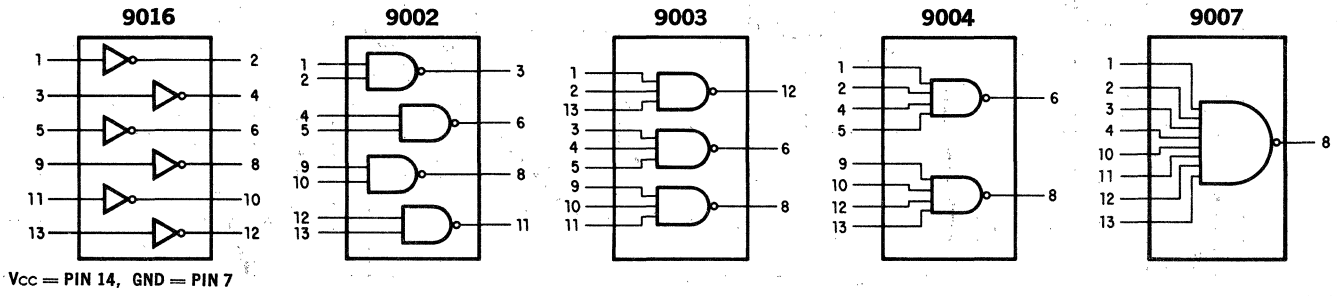
The following are acceptable ways to terminate unused inputs:

1. Tie the input to a used input on the same gate. The TTμL 9000 series has made special provision for this method by offering extra high level drive factor on all outputs.
2. Tie the input to V_{CC} through a resistor. This resistor should be chosen to keep the input current within absolute maximum ratings for any possible extreme of the V_{CC} supply. More than one input may be terminated through one resistor.
3. Tie inputs to a separate supply between 4.5 and 2.4 V, if one should be available.
4. Tie the inputs to the output of an unused gate. The unused gate must provide a constant high level output.

NAND GATES—9002, 9003, 9004 AND 9007
HEX INVERTER—9016

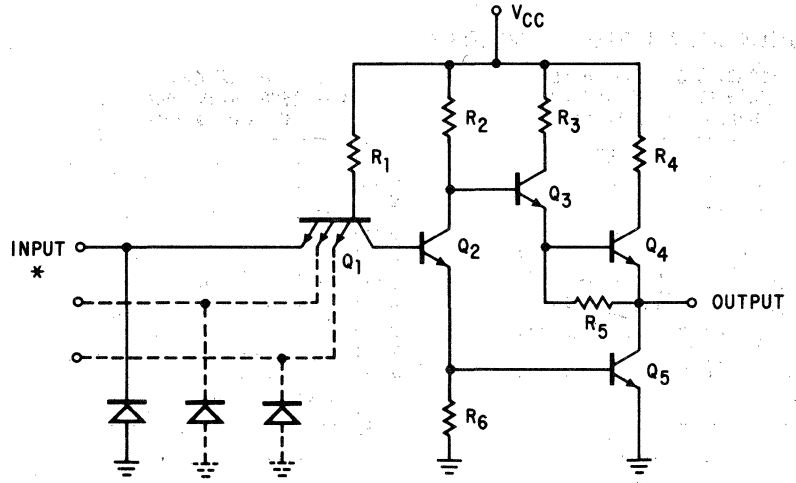
The 9002, 9003, 9004 and 9007 are active low level output AND gates commonly known as NAND gates. The 9016 is a hex inverter with input and output characteristics identical to the 9002, 9003, 9004 and 9007. This variety of gate combinations provides the system designer the utmost in logic flexibility and enables a reduction of package count.

Figure 1—LOGIC SYMBOL AND PIN CONFIGURATIONS



V_{CC} = PIN 14, GND = PIN 7

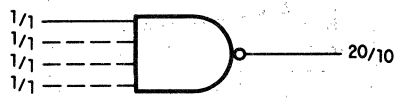
Figure 2—BASIC GATE CIRCUIT



Nominal Resistor Values
$R_1 = R_5 = 4.0\ k\Omega$
$R_2 = 1.5\ k\Omega$
$R_3 = 150\ \Omega$
$R_4 = 80\ \Omega$
$R_6 = 1.25\ k\Omega$

*Number of inputs depends on the gate.

Figure 3—LOADING FACTORS



ELECTRICAL CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016 (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V I_{OH} = −1.2 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 16.0 mA V_{IH} = 5.25 V
										V_{CC} = 4.75 V I_{OL} = 14.1 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V V_F = 0.45 V
			−1.41		−0.91	−1.41		−1.41		V_{CC} = 4.75 V 5.25 V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		6.1		3.6	6.1		6.1	mA	Inputs high
	V_{CC} Current, Gate Off (each gate)		1.7		1.07	1.7		1.7		Inputs at gnd V_{CC} = 5.0 V
t_{pd+}	Switching Speed				3.0	13			ns	V_{CC} = 5.0 V, See Figure 11
t_{pd-}	Switching Speed				3.0	15			ns	C_L = 15 pF

9002, 9003, 9004, 9007 AND 9016
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

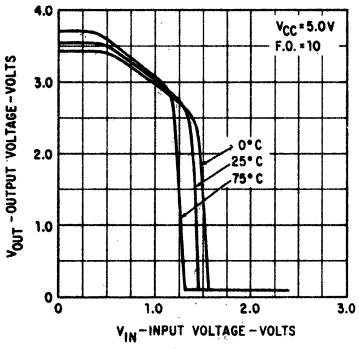


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

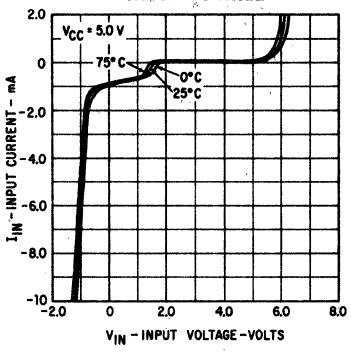


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

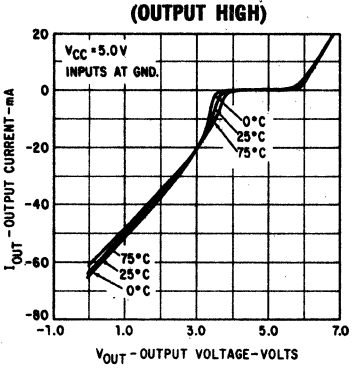


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

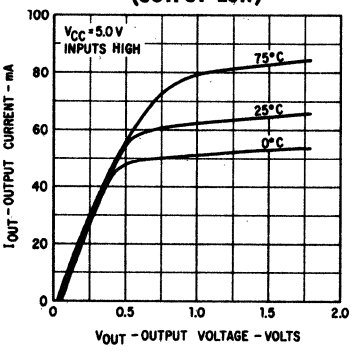


Fig. 7

LOGIC LEVELS AND NOISE IMMUNITY

WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

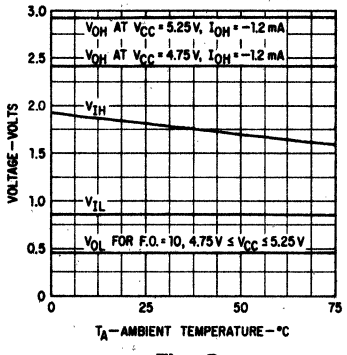


Fig. 8

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

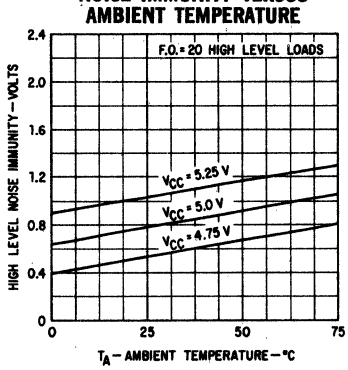


Fig. 9

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS FANOUT

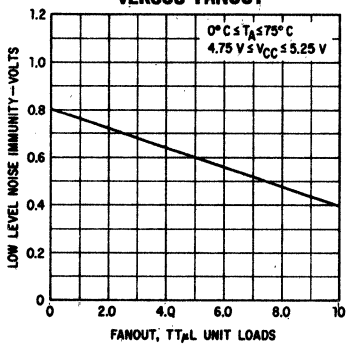
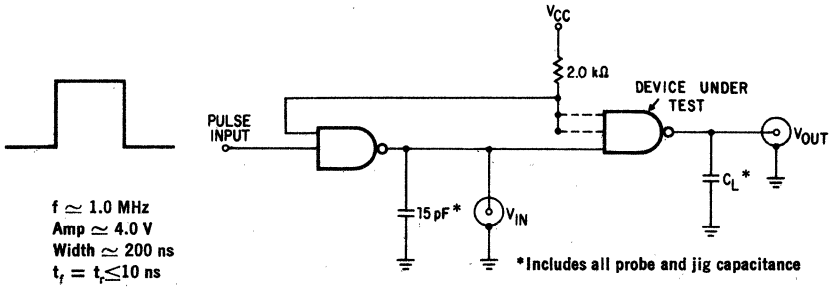


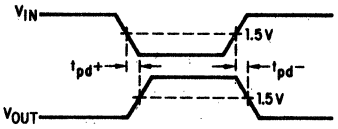
Fig. 10

SWITCHING CHARACTERISTICS

Figure 11—tpd TEST CIRCUIT



SWITCHING WAVEFORM



WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

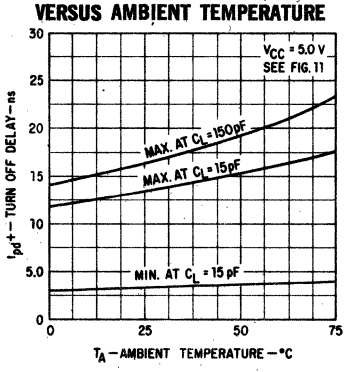


Fig. 12

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

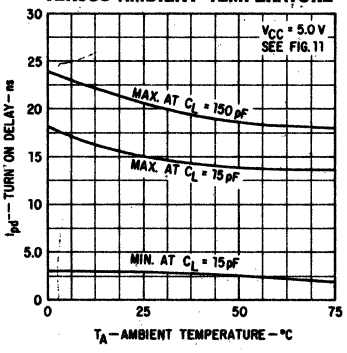


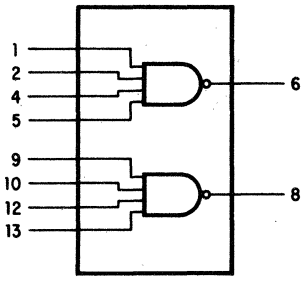
Fig. 13

NAND BUFFER — 9009

The 9009 is a power gate capable of sinking and sourcing large currents for high fanout applications. Logically it is the same as the 9004.

Fig. 1

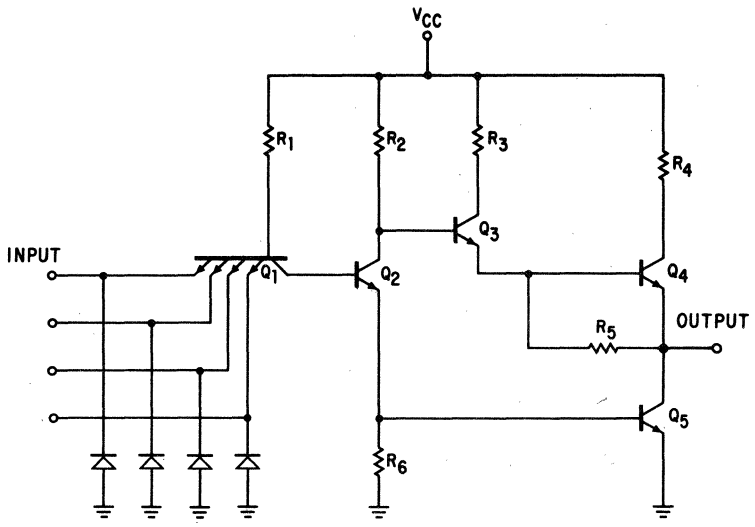
LOGIC DIAGRAM AND PIN CONFIGURATION



V_{CC} = PIN 14
GND = PIN 7

Fig. 2

CIRCUIT DIAGRAM (One Gate)

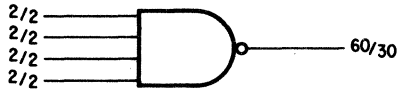


Nominal Resistor Values

$R_1 = 2.0\ k\Omega$ $R_4 = 50\ \Omega$
$R_2 = 560\ \Omega$ $R_5 = 4.0\ k\Omega$
$R_3 = 150\ \Omega$ $R_6 = 500\ \Omega$

Fig. 3

LOADING FACTORS



ELECTRICAL CHARACTERISTICS 9009 ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -3.6\ mA$ Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 48.0\ mA$ $V_{IH} = 5.25\ V$
										$V_{CC} = 4.75\ V$ $I_{OL} = 42.3\ mA$ Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
			−2.82		−1.82	−2.82		−2.82		$V_{CC} = 4.75\ V$ 5.25 V on other inputs
I_R	Input Leakage Current				20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		14.6		8.6	14.6		14.6	mA	Inputs high; $V_{CC} = 5.0\ V$
	V_{CC} Current, Gate Off (each gate)		3.4		2.15	3.4		3.4		Inputs at gnd; $V_{CC} = 5.0\ V$
t_{pd+}	Switching Speed			3.0		17			ns	$V_{CC} = 5.0\ V$, See Figure 11
t_{pd-}	Switching Speed			2.0		13			ns	$C_L = 15\ pF$

9009
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

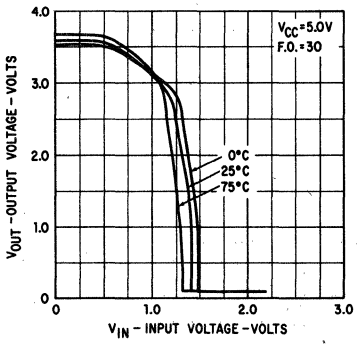


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

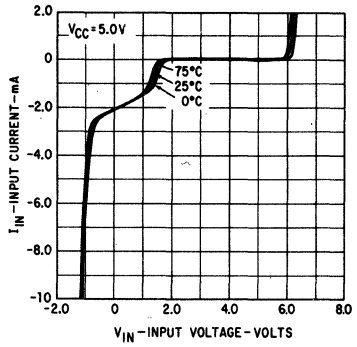


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

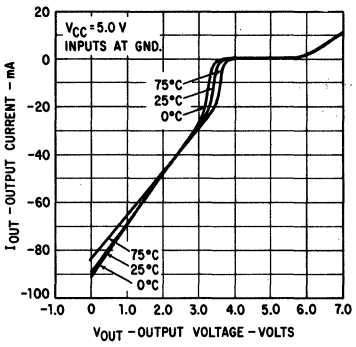


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

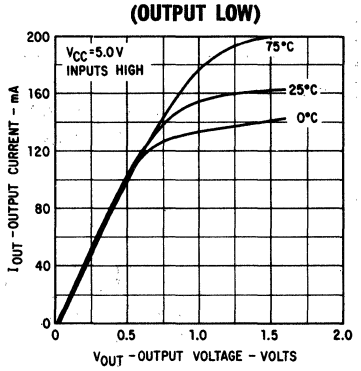


Fig. 7

LOGIC LEVELS AND NOISE IMMUNITY

WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

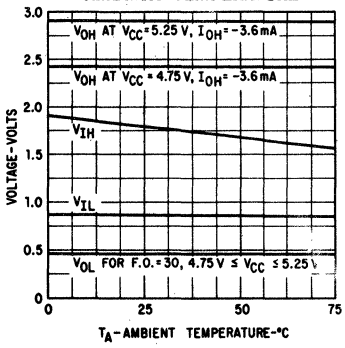


Fig. 8

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

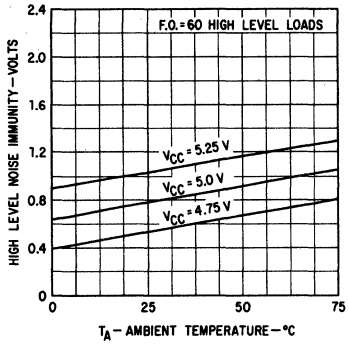


Fig. 9

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS FANOUT

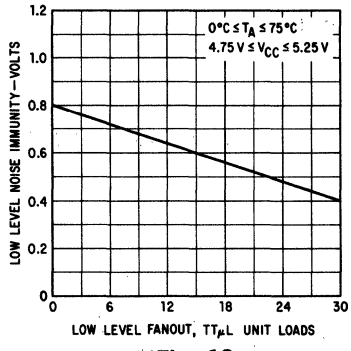
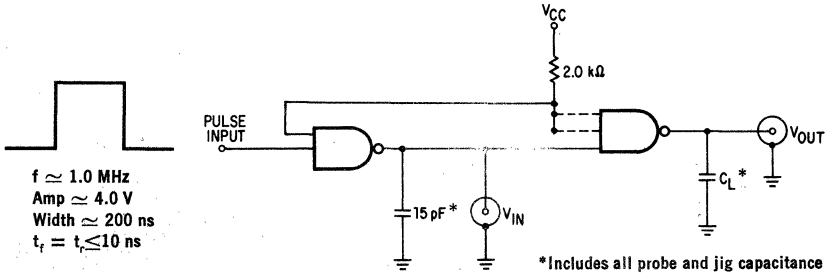


Fig. 10

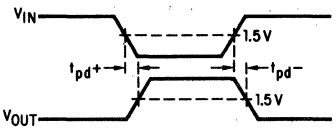
SWITCHING CHARACTERISTICS

Fig. 11

tpd TEST CIRCUIT



SWITCHING WAVEFORM



WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

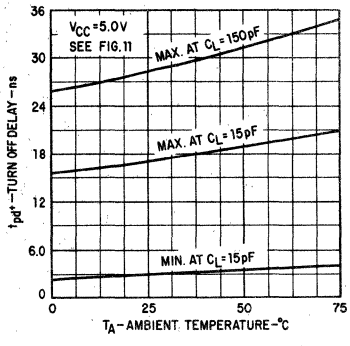


Fig. 12

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

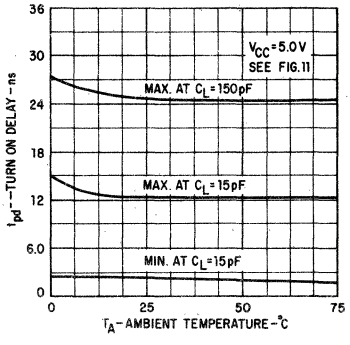


Fig. 13

EXTENDABLE AND-OR-INVERT GATES—9005, 9008
EXTENDER—9006

The TTμL 9005 and 9008 are AND-OR-INVERT gates which may be OR extended with the use of the 9006. For noise immunity and operating level curves, refer to the gate section on Page 4 and 5.

Figure 1—LOGIC DIAGRAMS AND LOADING FACTORS

The numbers by each input and output give the input loading and output drive capability. For complete explanation see Page 3.

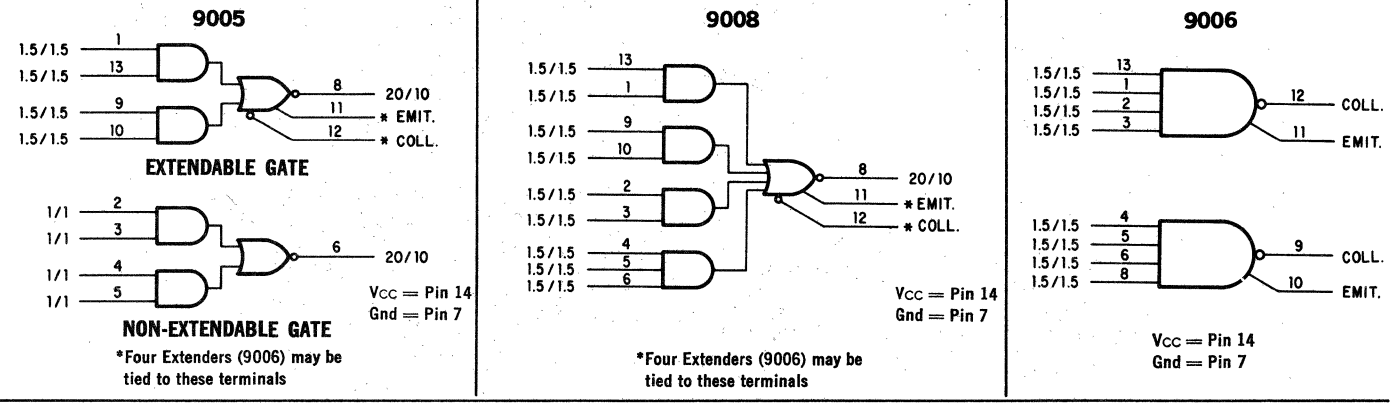
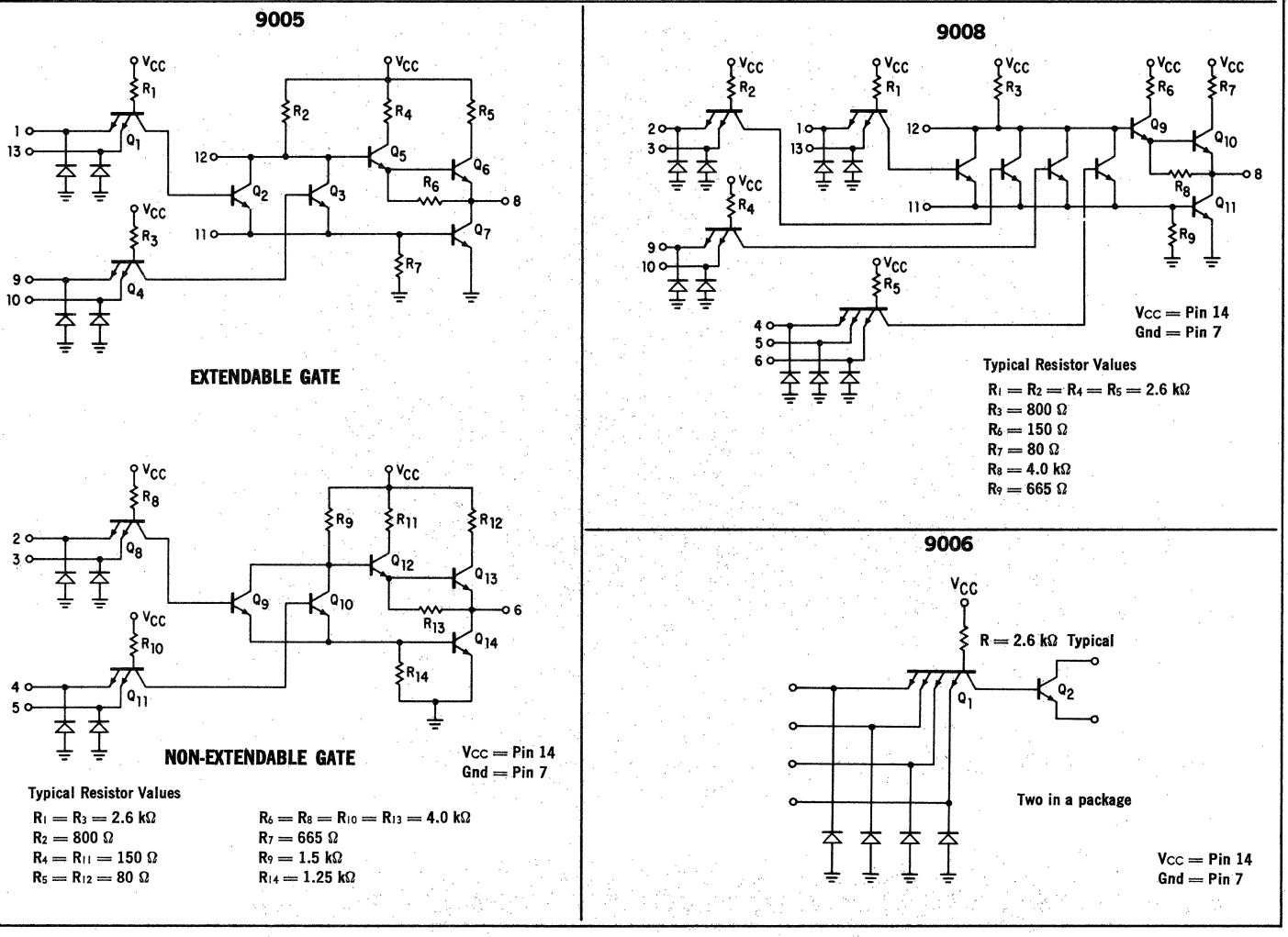


Figure 2—CIRCUIT DIAGRAMS



ELECTRICAL CHARACTERISTICS 9005, 9006 AND 9008 (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA V_{IL} = value indicated below on this table
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 16.0 mA V_{CC} = 4.75 V, I_{OL} = 14.1 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current 9005 Non-Extendable Gate		−1.6		−1.04	−1.6		−1.6	mA	V_{CC} = 5.25 V; V_F = 0.45 V, 5.25 V on other inputs
			−1.41		−0.79	−1.41		−1.41		V_{CC} = 4.75 V
	Input Load Current 9005 Extendable Gates and Extender		−2.4		−1.56	−2.4		−2.4	mA	V_{CC} = 5.25 V
			−2.12		−1.19	−2.12		−2.12		V_{CC} = 4.75 V
I_R	Input Leakage Current 9005 Non-Extendable Gate				5.0	60		60	μA	V_R = 4.5 V V_{CC} = 4.75 V Gnd on all other inputs
	Input Leakage Current Extendable Gates and Extender				7.5	90		90		
I_{PD}	V_{CC} Current, Gate "ON"								mA	V_{CC} = 5.0 V All inputs open
	9005 Non-Extendable Gate		7.7		4.5	7.7		7.7		
	9005 Extendable Gate		13.6		7.6	13.6		13.6		
	9008		17.7		9.3	17.7		17.7		
	V_{CC} Current, Gate "OFF"								mA	V_{CC} = 5.0 V All inputs except extender inputs gnd.
	9005 Non-Extendable Gate		3.4		2.2	3.4		3.4		
	9005 Extendable Gate		5.1		3.3	5.1		5.1		
	9008		10.2		6.6	10.2		10.2		
ΔI_{PD}	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "ON"		2.05		1.08	2.05		2.05	mA	V_{CC} = 5.0 V All inputs high
	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "OFF"		2.54		1.65	2.54		2.54	mA	V_{CC} = 5.0 V All inputs grounded

Note: Output characteristics above apply to a 9005 (both gates) or a 9008.
Input characteristics above apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

9005, 9006, 9008 TYPICAL INPUT-OUTPUT CHARACTERISTICS (EXTENDABLE GATES*)

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

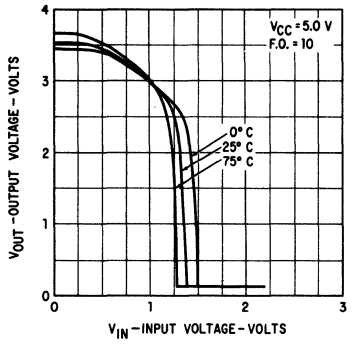


Fig. 3

INPUT CURRENT VERSUS INPUT VOLTAGE

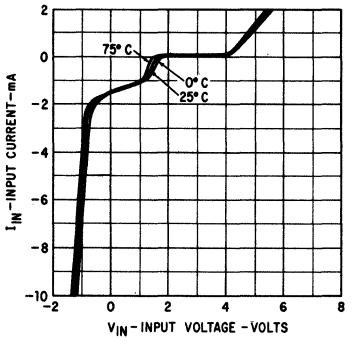


Fig. 4

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

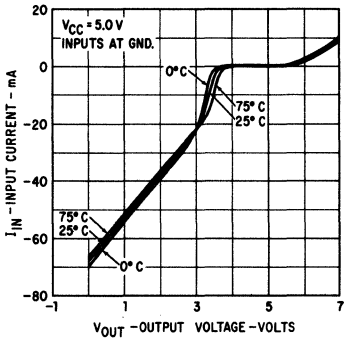


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

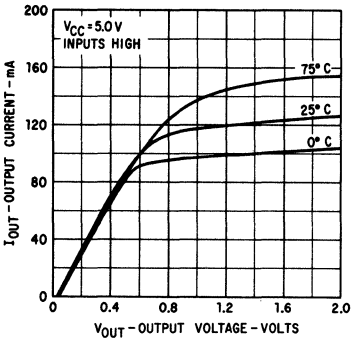


Fig. 6

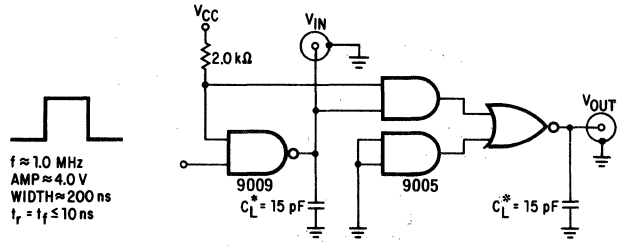
*Curves on Page 5 apply to 9005 nonextendable gate.

AC CHARACTERISTICS

t_{pd} TEST CIRCUITS

9005 NON-EXTENDABLE GATE

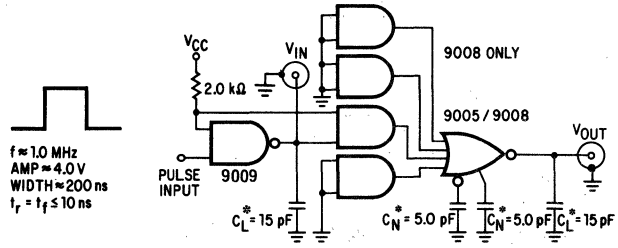
Fig. 7



*Includes all probe and/or jig capacitance.

9005 OR 9008 EXTENDABLE GATE

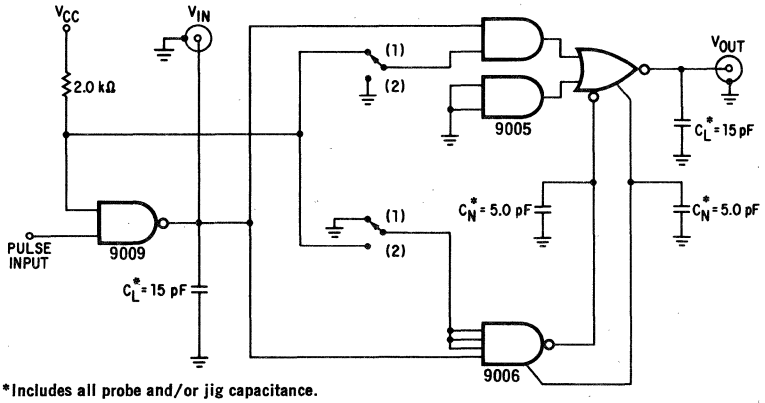
Fig. 8



*Includes all probe and/or jig capacitance.

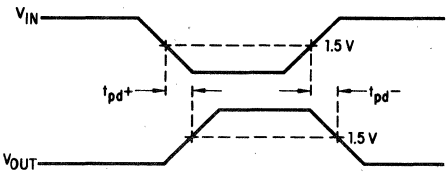
Fig. 9

9006 EXTENDER



*Includes all probe and/or jig capacitance.

SWITCHING WAVEFORM



NOTES:
With switch in position (1) measure tpd of 9005. With switch in position (2) measure tpd (9005) + Δtpd (9006). Capacitances include probe and jig capacitances.

AC CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	3.0	15	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF 9005 Nonextendable gate only, See. Fig. 7
t_{pd-}	3.0	15		
t_{pd+}	3.0	18	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF, $C_N = 5.0$ pF 9005 Extendable gate and 9008, See Fig. 8
t_{pd-}	3.0	13		
Δt_{pd+}	−3.0	5.0	ns	9006 only The 9006 is tested by measuring its propagation time through the 9005. The t_{pd} readings shall not exceed the 9005 readings by the specified amount. See Fig. 9.
Δt_{pd-}	−3.0	5.0		

Symbols are defined in the test circuit.

WORST CASE TURN OFF DELAY OF EXTENDABLE GATE VERSUS TEMPERATURE

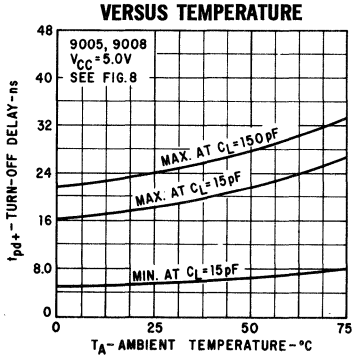


Fig. 10

WORST CASE TURN ON DELAY OF EXTENDABLE GATE VERSUS TEMPERATURE

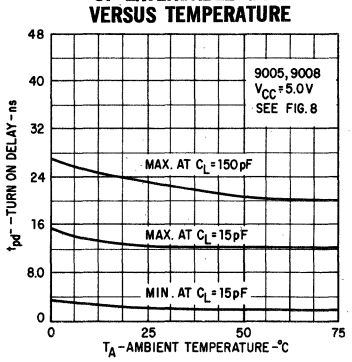


Fig. 11

WORST CASE TURN OFF DELAY OF NONEXTENDABLE GATE VERSUS TEMPERATURE

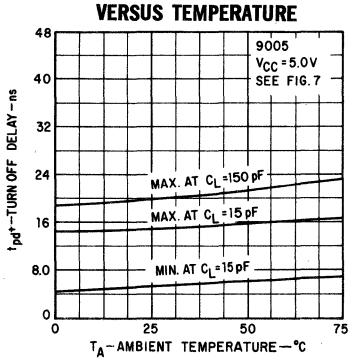


Fig. 12

WORST CASE TURN ON DELAY OF NONEXTENDABLE GATE VERSUS TEMPERATURE

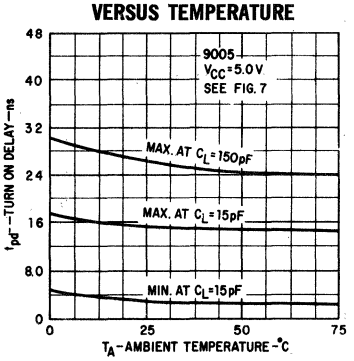


Fig. 13

J-K FLIP-FLOPS–9000, 9001
DUAL J-K FLIP-FLOPS–9020, 9022

GENERAL DESCRIPTION

The TTμL 9000 series has four flip-flops to satisfy the storage requirements of a logic system. All are master-slave JK designs and have the same high speed and high noise immunity as the rest of the 9000 series. As with the gates, all inputs have diode clamps to reduce ringing caused by long lines and impedance mismatches.

The JK type flip-flop was chosen for all flip-flop elements in this family because of its inherent logic power. The input function required to produce a given sequence of states for a JK flip-flop will, in general, contain more "don't care" conditions than the corresponding function for an RS flip-flop. These additional "don't care" conditions will, in most cases, reduce the amount of gating elements required to implement the input function.

The master-slave design offers the advantage of a DC threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

Data is accepted by the master while the clock is in the low state. Refer to the truth table for definition of "HIGH" and "LOW" data. Transfer from the master to the slave occurs on the low to high transition of the clock. When the clock is high, the J and K inputs are inhibited.

A joint (JK) input is provided for all flip-flops in this family. This common input removes the necessity of gating the clock signal with an external gate in many applications. This not only reduces package count, but also reduces the possibility of clock skew problems, since with internal gating provided, all flip-flops may be driven from a common clock line. Several TTμL drivers may be used in parallel to drive this common clock line, if the load exceeds the F.O. capability of the 9009 buffer.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided on all flip-flops except the 9020, which because of a logic trade-off has only clear inputs. The set or clear pin being low absolutely guarantees that one output will be high, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the low output may momentarily spike high synchronous with a positive transition of the clock. If the low output of the flip-flop is connected to other flip-flop inputs clocked from the same line, the spike will be masked by the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur. When the spikes can cause problems, a simple solution is to common the joint JK inputs with the synchronous set or reset signal.

Figure 1—LOGIC DIAGRAMS AND LOADING FACTORS

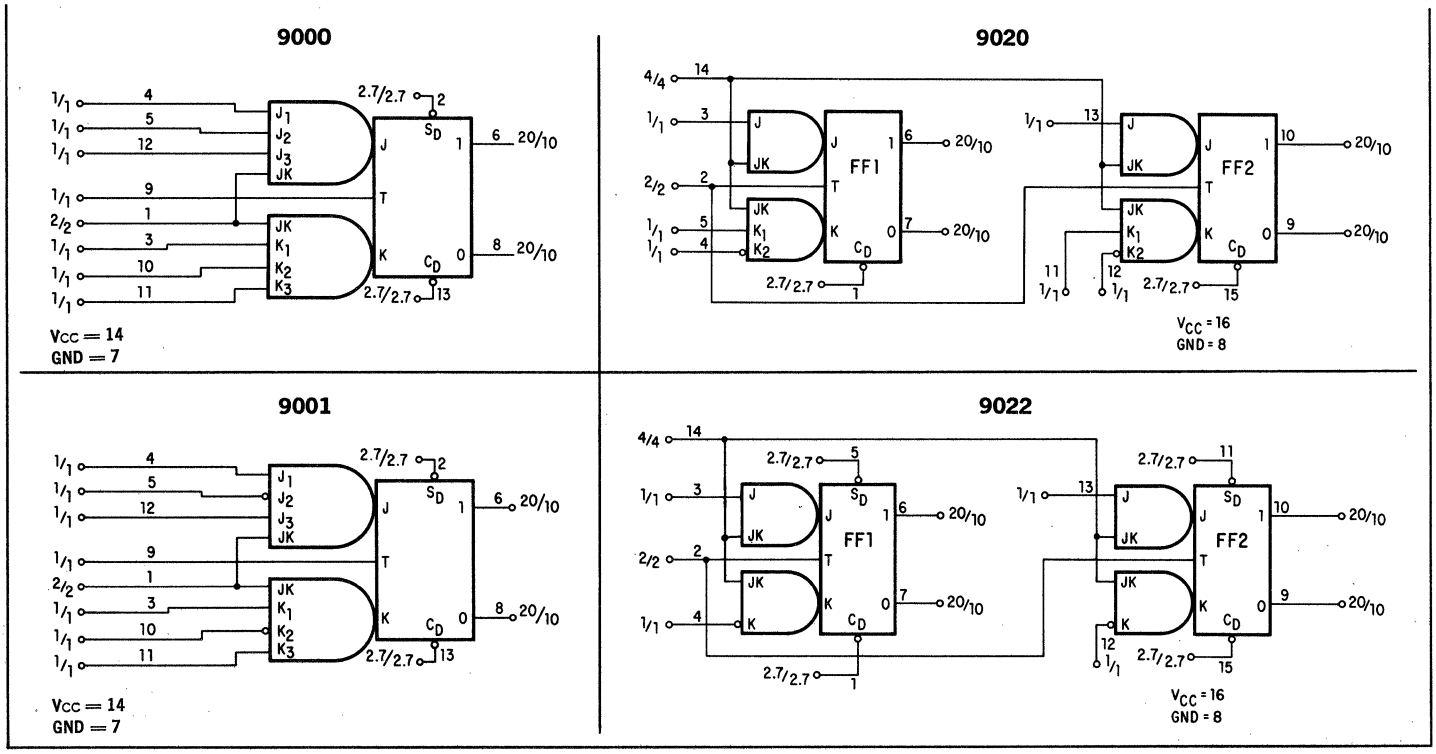
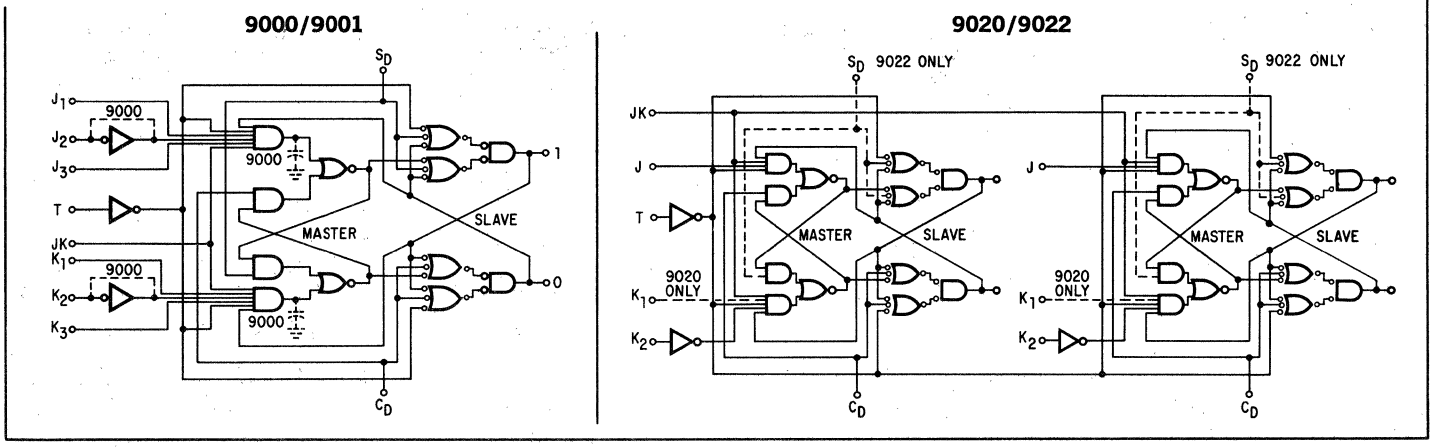


Figure 2—FUNCTIONAL LOGIC DIAGRAMS



TRUTH TABLES

SYNCHRONOUS OPERATION

BEFORE CLOCK				OUTPUTS AFTER CLOCK	
OUTPUTS		INPUTS			
ONE	ZERO	J	K	ONE	ZERO
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
S_D	C_D	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	SYNCHRONOUS INPUTS CONTROL	

SYNCHRONOUS OPERATION

The truth table defines the next state of the flip-flop after a low-to-high transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table.

The J and K inputs in the table refer to the basic flip-flop J and K inputs as indicated on the logic diagrams. These internal inputs are for every flip-flop the result of a logic operation on the external J and K inputs. This operation is represented symbolically by AND gates in the logic diagram for each flip-flop. Logic diagrams are in accordance with MIL Standard 806B.

The L* symbol in the J and K input column is defined as meaning that the **input does not go high at any time while the clock is low.**

The H* symbol in the J or K input column is defined as meaning that the **input is high at some time while the clock is low.**

The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state high and low voltage levels, respectively.

UNUSED INPUTS

The 9001, 9020 and 9022 all have active level low synchronous inputs. When not in use they must be grounded. All other unused inputs including asynchronous should be tied high for maximum operating speed. Use one of the methods recommended on Page 3.

ELECTRICAL CHARACTERISTICS 9000, 9001, 9020 AND 9022 ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$	
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$	
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs.	
I_R	Input Leakage								μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$	
	All J, K inputs				5.0	60		60		Gnd. on other inputs.	
	T inputs 9000, 9001										
	JK inputs 9000, 9001				10	120		120			
	T inputs 9020, 9022										
	JK inputs 9020, 9022				20	240		240			
	S_D, C_D (all flip-flops)				14	160		160			
I_F	Input Current								mA	$V_{CC} = 5.25\ V$	$V_F = 0.45\ V$
	All J, K inputs		−1.60		−1.0	−1.60		−1.60			5.25 V on other
	T inputs 9000, 9001										inputs
	JK inputs 9000, 9001		−3.20		−2.0	−3.20		−3.20			
	T inputs 9020, 9022										
	JK inputs 9020, 9022		−6.40		−4.0	−6.40		−6.40			
	S_D, C_D (all flip-flops)		−4.32		−2.7	−4.32		−4.32			
I_F	Input Current								mA	$V_{CC} = 4.75\ V$	
	All J, K inputs		−1.41		−0.94	−1.41		−1.41			
	T inputs 9000, 9001										
	JK inputs 9000, 9001		−2.82		−1.88	−2.82		−2.82			
	T inputs 9020, 9022										
	JK inputs 9020, 9022		−5.64		−3.76	−5.64		−5.64			
	S_D, C_D (all flip-flops)		−3.78		−2.54	−3.78		−3.78			
I_{PD}	V_{CC} Current								mA		$V_{CC} = 5.0\ V$
	9000		28			28		28		S_D at gnd	
	9001		33			33		33		S_D at gnd	
	9020, 9022		30			30		30		C_{D1}, C_{D2} at gnd	
	each flip-flop										

TYPICAL INPUT AND OUTPUT CHARACTERISTICS
9000, 9001, 9020 AND 9022

OUTPUT VOLTAGE VERSUS ASYNCHRONOUS INPUT VOLTAGE

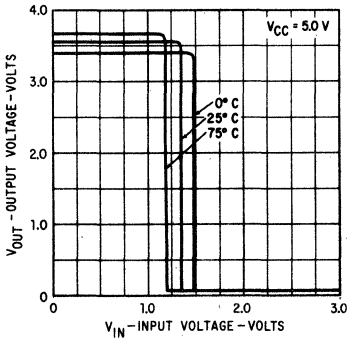


Fig. 3

OUTPUT VOLTAGE VERSUS CLOCK INPUT VOLTAGE

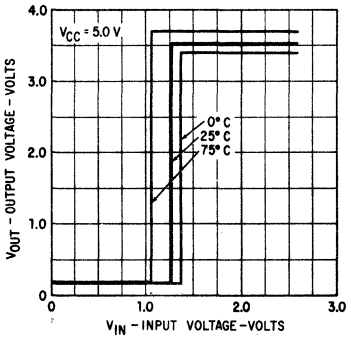


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE CP INPUT 9020, 9022

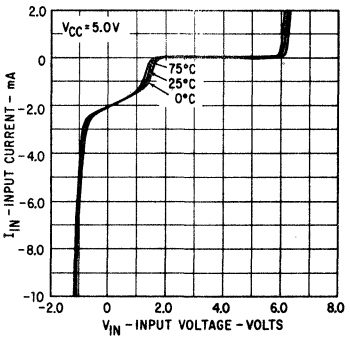


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

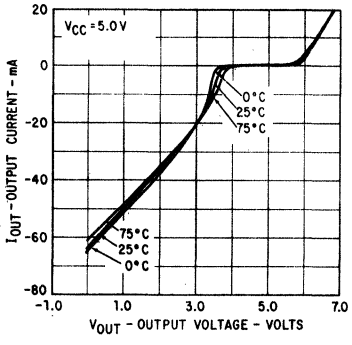


Fig. 6

INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9000, 9001

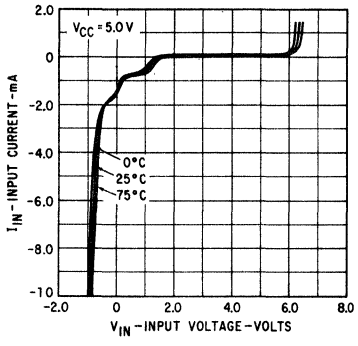


Fig. 7

INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9020, 9022

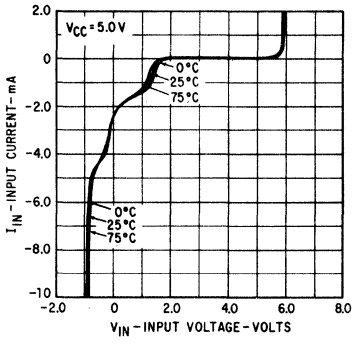


Fig. 8

INPUT CURRENT VERSUS INPUT VOLTAGE, ASYNCHRONOUS INPUTS — ALL FLIP-FLOPS

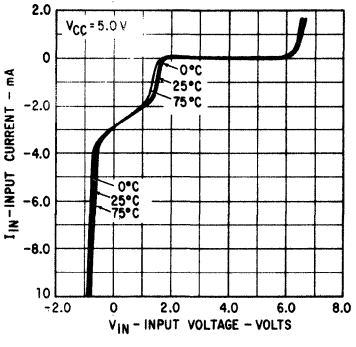


Fig. 9

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

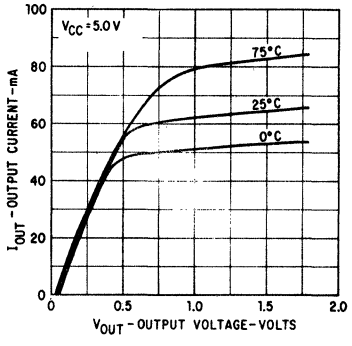


Fig. 10

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = C_l = 15$ pF of all flip-flops unless otherwise noted)

CHARACTERISTICS				MIN.	TYP.	MAX.	UNITS	FIGURES
t_{pd+}	Clock-to-Output				12	20	ns	16, 17, 18
	S_D or C_D-to-Output				12	20	ns	16, 17, 18
t_{pd-}	Clock-to-Output				20	30	ns	16, 17, 18
	S_D or C_D-to-Output				25	35	ns	16, 17, 18
t_{set-up}	J, K or JK		9000 Only	35	22		ns	16, 18
	Data Entry			12	8.0		ns	16, 17, 18
	$\overline{J}$ or $\overline{K}$ Data Entry			17	12		ns	16, 17, 18
$t_{release}$	J, K or JK		9000 Only		18	12	ns	16, 18
	Data Entry				7.0	1.0	ns	16, 17, 18
	$\overline{J}$ or $\overline{K}$ Data Entry				11	4.0	ns	16, 17, 18
Pulse Widths	Clock	9000 Only	Positive		20		ns	16, 18
			Negative		25		ns	16, 18
			Positive		8.0		ns	16, 17, 18
			Negative		10		ns	16, 17, 18
	S_D or C_D		Negative		25		ns	16, 17, 18
Toggle Frequency			9000 Only		20		MHz	16, 18
					50		MHz	16, 17, 18

CLOCK-TO-OUTPUT DELAYS VERSUS AMBIENT TEMPERATURE

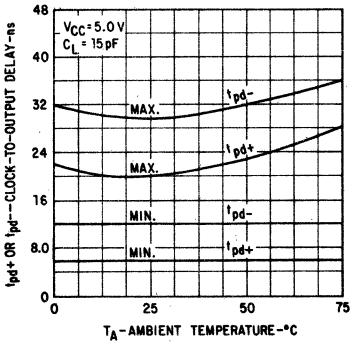


Fig. 11

ASYNCHRONOUS INPUT-TO-OUTPUT DELAYS VERSUS AMBIENT TEMPERATURE

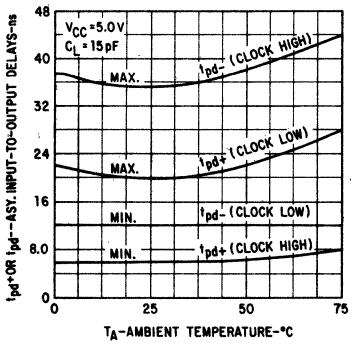


Fig. 12

DELAY INCREASE WITH ADDED LOAD CAPACITANCE

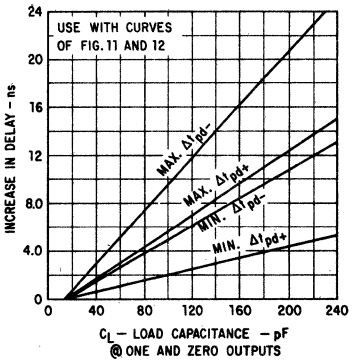


Fig. 13

9000 NEGATIVE CLOCK PULSE WIDTH, SET-UP TIME AND RELEASE TIME VERSUS AMBIENT TEMPERATURE

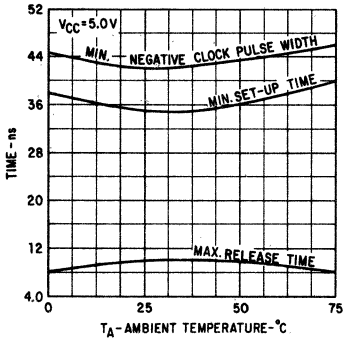


Fig. 14

9001-9020-9022 NEGATIVE CLOCK PULSE WIDTH SET-UP TIME AND RELEASE TIME VERSUS AMBIENT TEMPERATURE

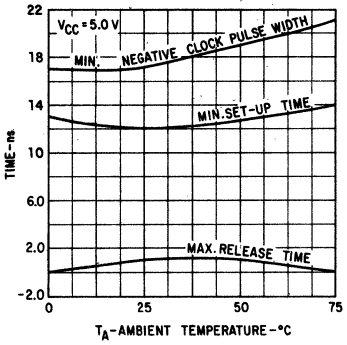
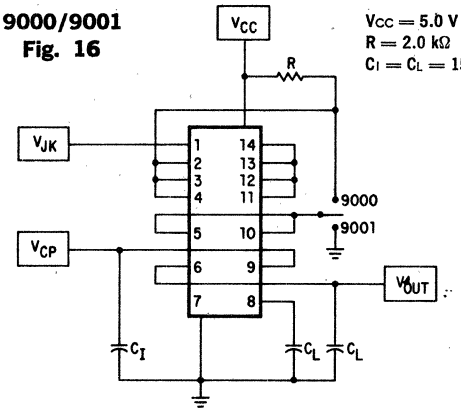


Fig. 15

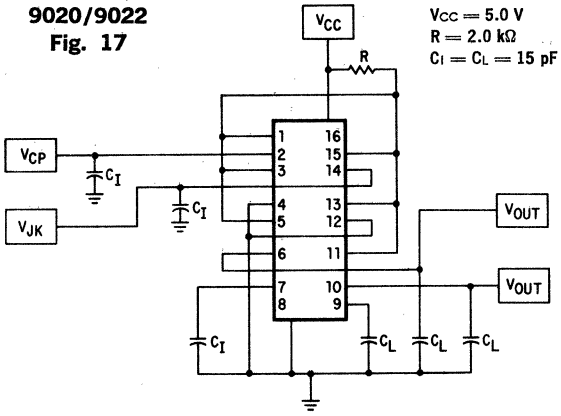
SWITCHING TEST CIRCUITS

9000/9001
Fig. 16



V_{CC} = 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

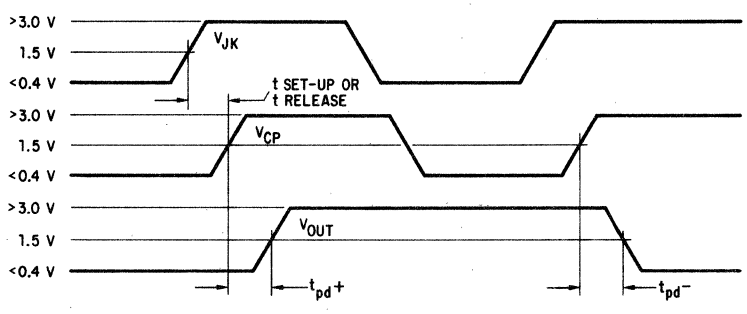
9020/9022
Fig. 17



V_{CC} = 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

WAVEFORMS

Fig. 18



SWITCHING TEST NOTES

t_{pd+} and t_{pd-}

1. V_{JK} should be kept at the high logic level when performing t_{pd} tests.
2. Drive the clock pulse input with a suitable pulse source. t_{pd+} and t_{pd-} delays are as defined in the waveforms.

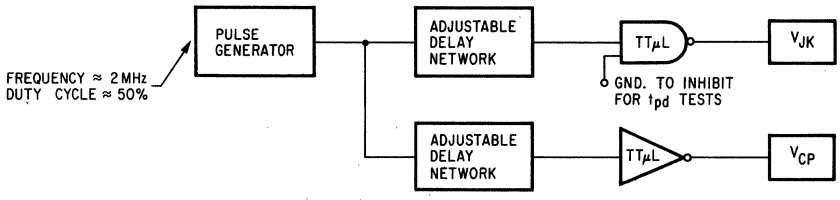
$t_{set\text{-}up}$

1. $t_{set\text{-}up}$ is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the low state of the clock in order for the flip-flop to respond to the data.
2. The test for $t_{set\text{-}up}$ is performed by adjusting the timing relationship between the V_{CP} and V_{JK} inputs to the $t_{set\text{-}up}$ minimum value. A device that passes the test will have the output waveform shown. The output of a device that does not pass the $t_{set\text{-}up}$ test will remain at a static logic level (no switching will occur).

$t_{release}$

1. $t_{release}$ is defined as the maximum time allowed for a HIGH to be present at a synchronous logic input at any time during the low state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

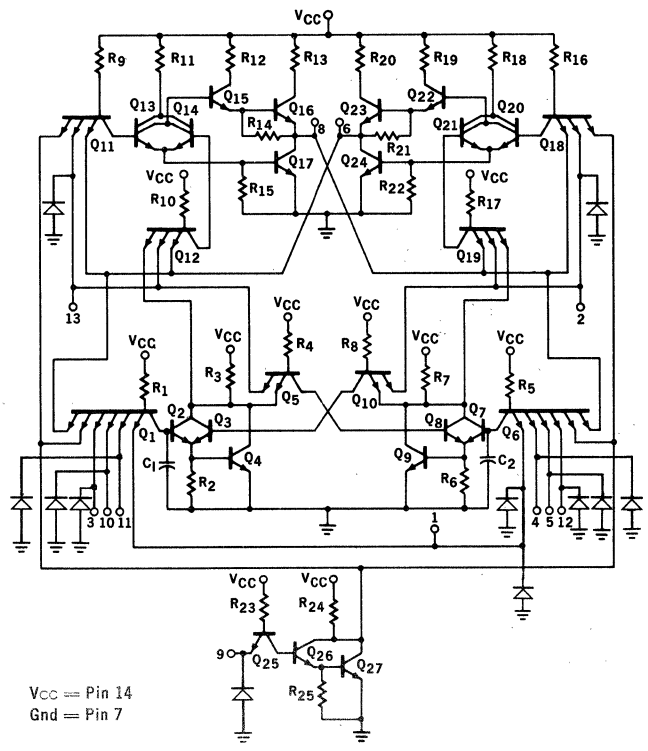
RECOMMENDED INPUT PULSE SOURCES



DTμL 9932 gates with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

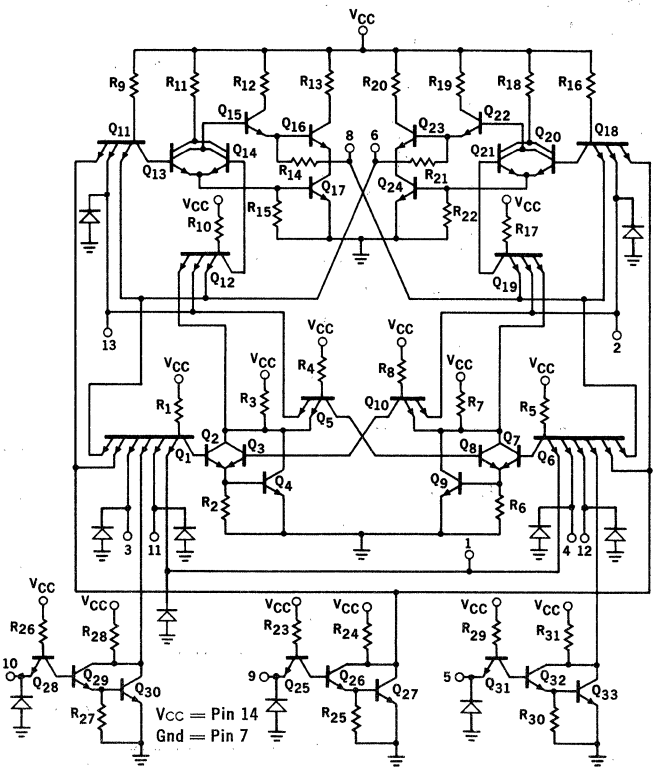
9000 SCHEMATIC DIAGRAM

For resistor values see, page 16

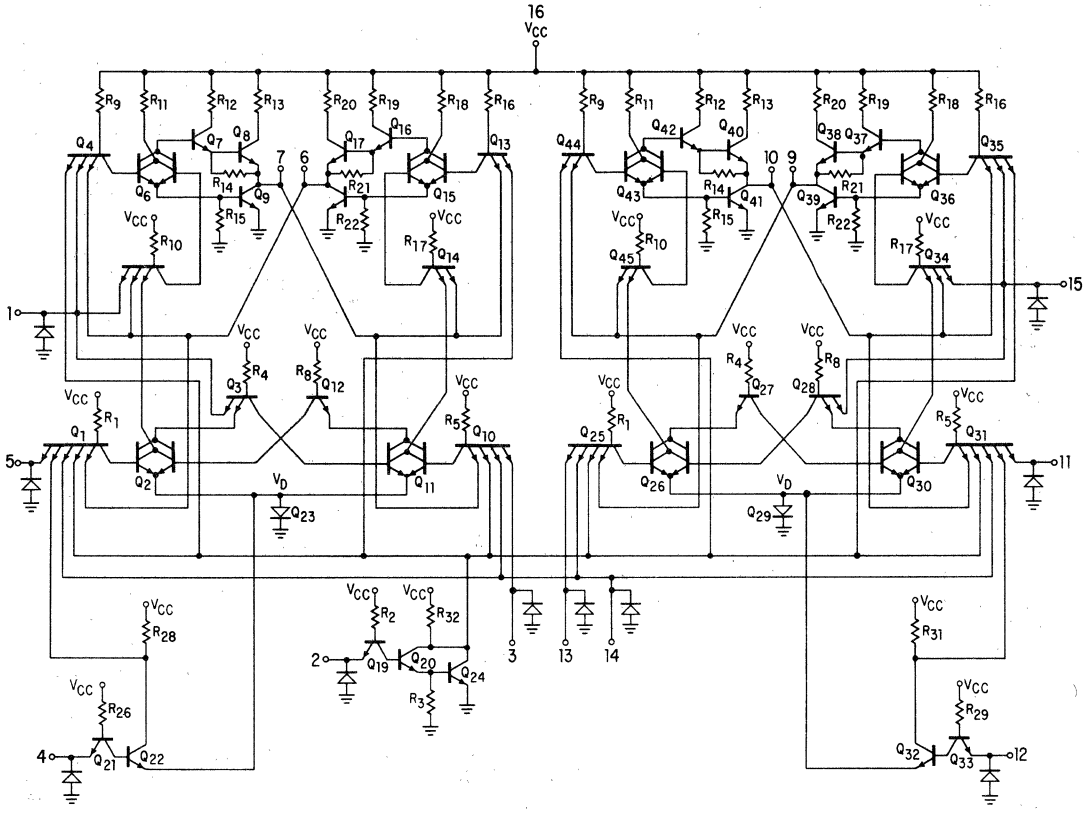


9001 SCHEMATIC DIAGRAM

For resistor values see, page 16



9020 SCHEMATIC DIAGRAM



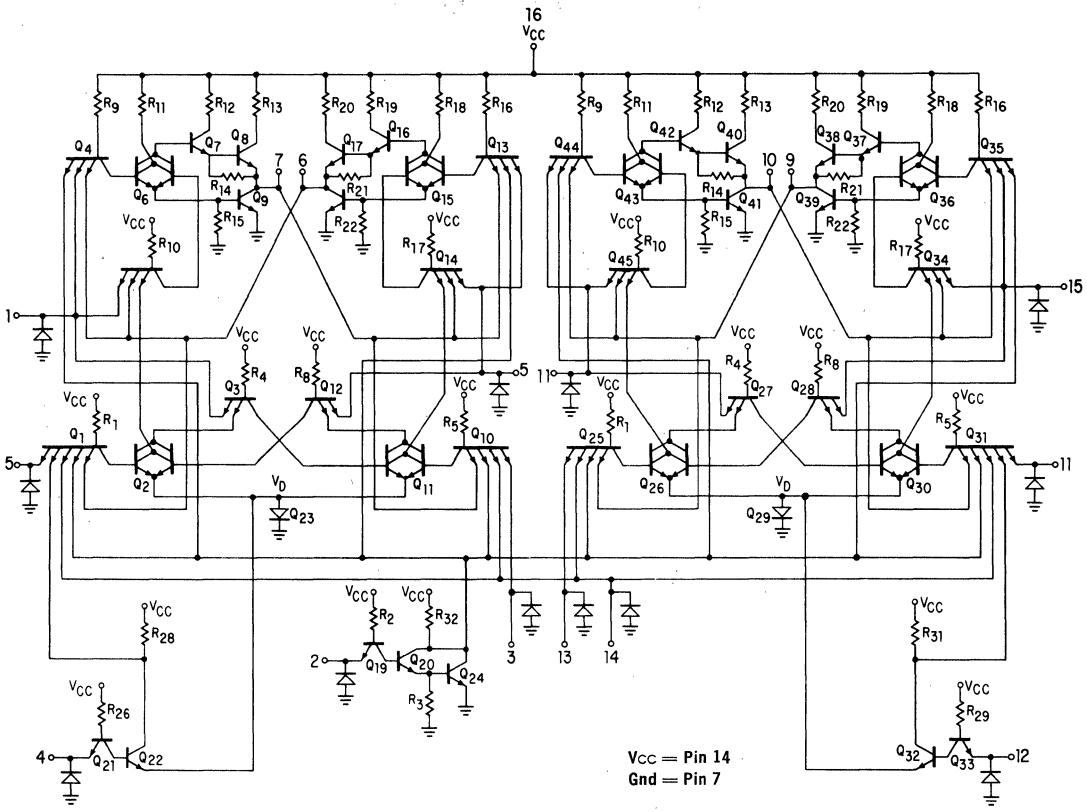
VCC = Pin 16
Gnd = Pin 8

NOMINAL COMPONENT VALUES (ALL FLIP-FLOPS)

R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, $R_{29} = 4.0\ k\Omega$
R_2, R_3, R_6, $R_7 = 2.0\ k\Omega$
R_9, R_{16}, R_{28}, $R_{31} = 6.0\ k\Omega$
R_{11}, $R_{18} = 1.5\ k\Omega$
R_{12}, $R_{19} = 150\ \Omega$
R_{13}, $R_{20} = 80\ \Omega$
R_{15}, R_{22}, R_{25}, R_{27}, $R_{30} = 1.25\ k\Omega$
$R_{32} = 1.0\ k\Omega$
C_1, $C_2 = 10\ pF$

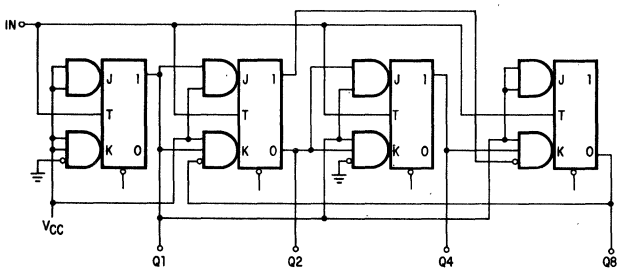
9022 SCHEMATIC DIAGRAM

For resistor values, see table on page 16



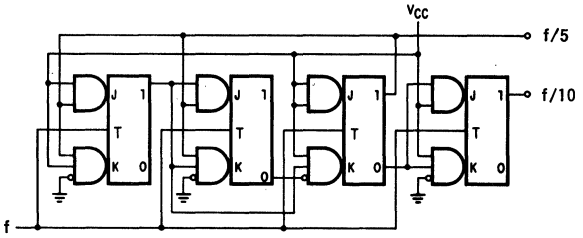
APPLICATIONS

SYNCHRONOUS BCD COUNTER



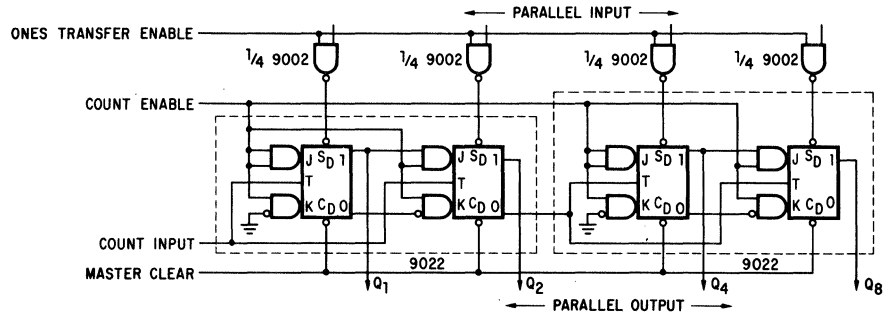
Two TTμL 9020 Dual Flip-Flops require no additional gating to produce a fully synchronous 8421 code BCD Counter.

DIVIDE BY TEN COUNTER



Two TTμL 9020 Dual Flip-Flops require no additional gating elements to produce divide by ten circuit with a square wave divide by ten output and a divide by five output.

BINARY COUNTER WITH ASYNCHRONOUS PARALLEL LOAD AND CLEAR



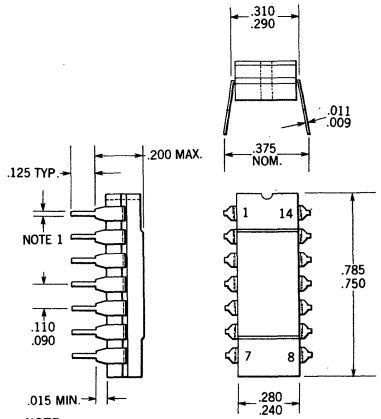
Binary counter using synchronous 2 bit stages with trickle down between stages illustrates method of utilizing dual JK flip-flops having common clocks in counter applications.

PACKAGE OUTLINES

U6A

PHYSICAL DIMENSIONS

SIMILAR TO
JEDEC (TO-116) Outline
Dual In-Line Package

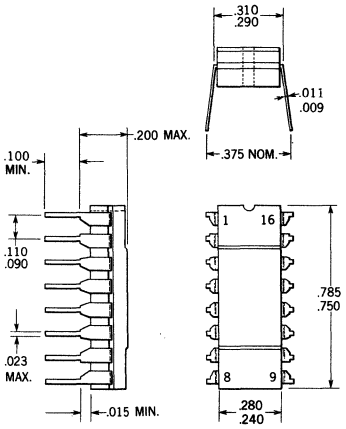


NOTE:
1. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

U6B

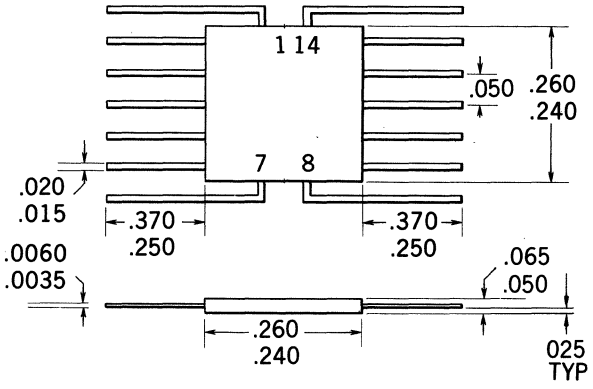
PHYSICAL DIMENSIONS

16 Lead Dual In-Line



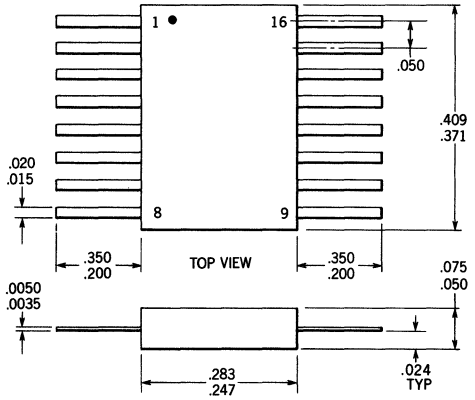
U3I

CERPAK 14 LEAD



U3L

CERPAK 16 LEAD



ORDER INFORMATION

To order Transistor-Transistor Micrologic elements specify
- U3IXXXX59X for 14-pin Flat package
- U6AXXXX59X for 14-pin Dual In-Line package
- U3LXXXX59X for 16-pin Flat package
- U6BXXXX59X for 16-pin Dual In-Line package

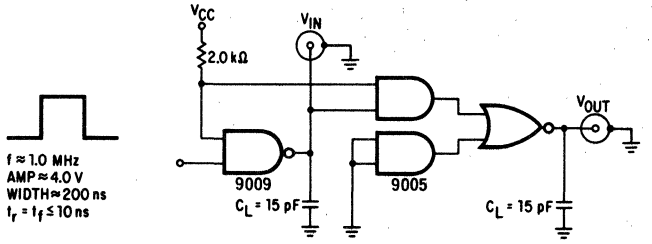
Where XXXX is the four-digit number denoting the specific element desired and 59X is for 0°C to +75°C temperature.

AC CHARACTERISTICS

t_{pd} TEST CIRCUITS

9005 NON-EXTENDABLE GATE

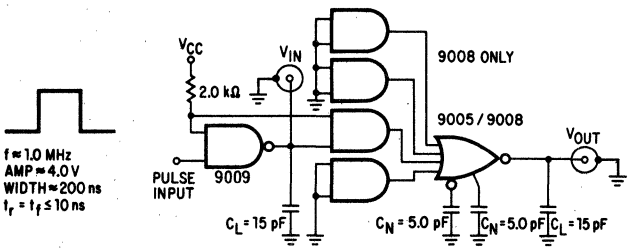
Fig. 7



Note: Capacitance includes probe and jig capacitance

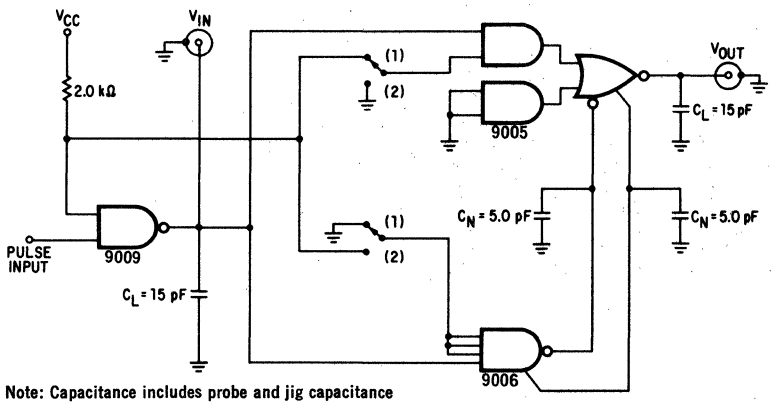
9005 OR 9008 EXTENDABLE GATE

Fig. 8



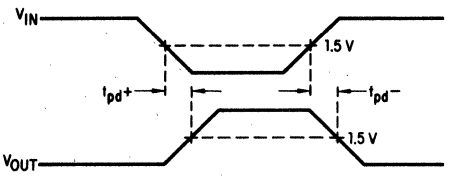
Note: Capacitance includes probe and jig capacitance

Fig. 9 **9006 EXTENDER**



Note: Capacitance includes probe and jig capacitance

SWITCHING WAVEFORM



NOTES:
With switch in position (1) measure tpd of 9005. With switch in position (2) measure tpd (9005) + Δtpd (9006). Capacitances include probe and jig capacitances.

AC CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	3.0	12	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF 9005 Nonextendable gate only, See Fig. 7
t_{pd-}	3.0	14		
t_{pd+}	3.0	15	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF, $C_N = 5.0$ pF 9005 Extendable gate and 9008, See Fig. 8
t_{pd-}	3.0	12		
Δt_{pd+}	−2.0	4.0	ns	9006 only The 9006 is tested by measuring its propagation time through the 9005. The t_{pd} readings shall not exceed the 9005 readings by the specified amount. See Fig. 9.
Δt_{pd-}	−2.0	4.0		

Symbols are defined in the test circuit.

WORST CASE TURN OFF DELAY OF EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

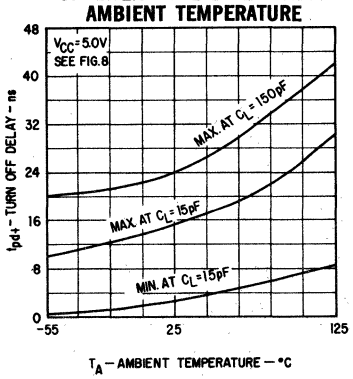


Fig. 10

WORST CASE TURN ON DELAY OF EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

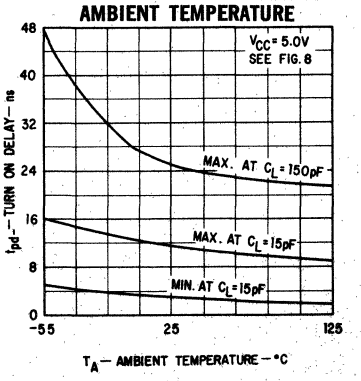


Fig. 11

WORST CASE TURN OFF DELAY OF NONEXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

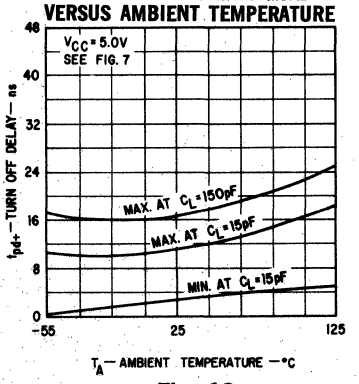


Fig. 12

WORST CASE TURN ON DELAY OF NONEXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

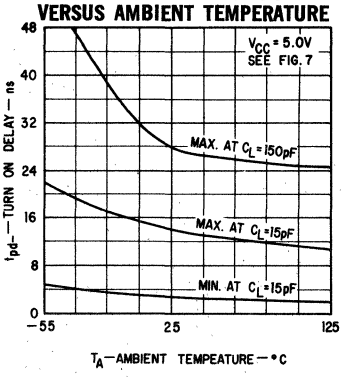


Fig. 13

FUNCTIONAL DESCRIPTION

The 9601 monostable multivibrator has four inputs, two of which are active level high and two active level low. This allows a choice of leading edge or trailing edge triggering. The inputs are D.C. coupled making triggering independent of input transition times.

Each time the input conditions for triggering are met, the external capacitor is discharged in a short time and a new cycle is begun. Successive inputs with a period shorter than the delay time retrigger the 9601 and result in a continuous true output. Retriggering may be inhibited by tying the negation ($\bar{Q}$) output back to an active level high input.

Active pullups are provided for good drive capability into capacitive loads.

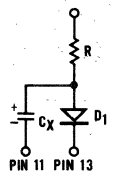
OPERATION RULES

1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 5.0 kΩ to 50 kΩ for 0 to +75°C operation, and 5.0 kΩ to 25 kΩ for −55 to +125°C operation. C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following values are recommended: $R_X = 30$ kΩ for 0 to +75°C operation; $R_X = 10$ kΩ for −55 to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.32\ R_X C_X\ [1 + \frac{0.7}{R_X}]$ (For C_X greater than 10^3 pF)

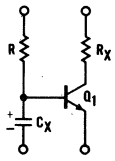
   Where R_X is in kΩ
   C_X is in pF
   T is in ns

   For $C_X < 10^3$ pF, see Fig. 14
4. If electrolytic type capacitors are to be used, the following two arrangements are recommended:



$R < 0.6\ R_X$ (Max)

D_1: any silicon type diode, such as FD700



This circuit also amplifies Cx allowing for longer output pulse width.

$R < R_X\ (0.7)\ (h_{fe}Q_1)$

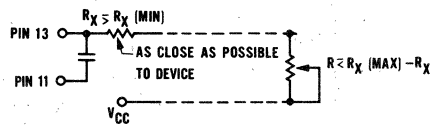
R_X (min) $< R_X < R_X$ (max)

Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

Both circuits prevent reverse voltage across C_X. The pulse width T for the circuits is defined as follows:

$T \approx 0.36\ RC_X\ [1 + \frac{0.7}{R}]$ Where: R is in kΩ
C_X is in pF
T is in ns

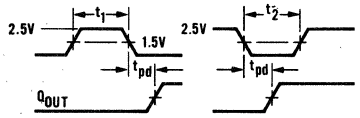
5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:



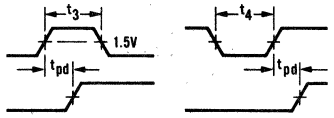
6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules.

Input to Pin 1 (2)
Pins 2, (1), 3 & 4 = 1

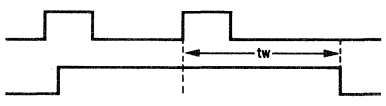
t_1, t_4 = Setup time > 40 ns
t_2, t_3 = Release time > 40 ns



Input to Pin 3 (4)
Pin 4 (3) = 1. Pins 1 or 2 = 0



8. The retrigger pulse width is calculated as shown below:



$tw = tpw + tpd+ = 0.32\ RxCx\ (1 + \frac{0.7}{Rx}) + tpd+$

The retrigger pulse width is equal to the pulse width tpw plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as tpw.

NOTE: Retriggering will not occur if the retrigger pulse comes within $.32\ RxCx\ (\frac{.7}{Rx})$ ns after the initial trigger pulse.

TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $125°C$, $V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS (Note 1)
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4	Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.72\ mA$ (Note 2)
V_{OL}	Output Low Voltage		0.4		0.2	0.4	0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10\ mA$ (Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4	Volts	$V_{CC} = 4.5\ V$ (Note 3)
V_{IL}	Input Low Voltage		0.85			0.90	0.85	Volts	$V_{CC} = 5.5\ V$ (Note 3)
I_F	Input Load Current		−1.6		−1.1	−1.6	−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				15	60	60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40		mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		25			25	25	mA	$V_{CC} = 5.5\ V$
t_{pd+}	Negative Trigger Input to True Output				25	40		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
t_{pd-}	Negative Trigger Input to Complement Output				25	40		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76		μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000\ pF$
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50	50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0 25	kΩ	

TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS (Note 1)
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4	Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.96\ mA$ (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45	0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 12.8\ mA$ (Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6	Volts	$V_{CC} = 4.75\ V$ (Note 3)
V_{IL}	Input Low Voltage		.85			0.85	0.85	Volts	$V_{CC} = 5.25\ V$ (Note 3)
I_F	Input Load Current		−1.6		−1.0	−1.6	−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current				15	60	60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40		mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		25			25	25	mA	$V_{CC} = 5.25\ V$, Ground Pins 1 and 2
t_{pd+}	Negative Trigger Input to True Output				25	40		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
t_{pd-}	Negative Trigger Input to Complement Output				25	40		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76		μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000\ pF$
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50	50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0 50	kΩ	

NOTES:
(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)
(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8.
Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.
(3) Pulse Test to determine V_{IH} and V_{IL} (Min PW 40 ns).

TYPICAL ELECTRICAL CHARACTERISTICS

INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

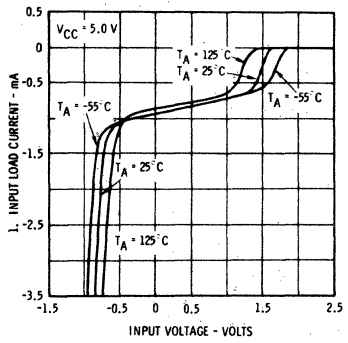


Fig. 3

INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE

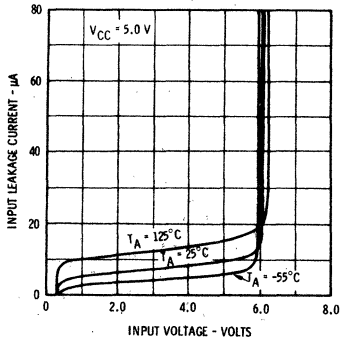


Fig. 4

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

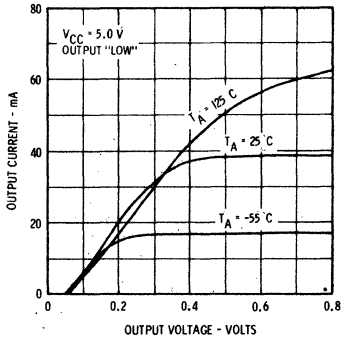


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)

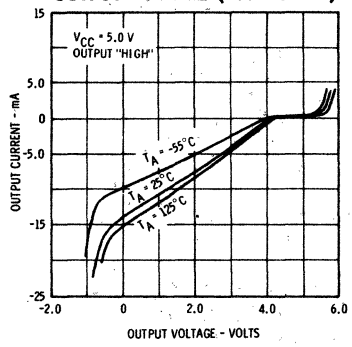


Fig. 6

POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

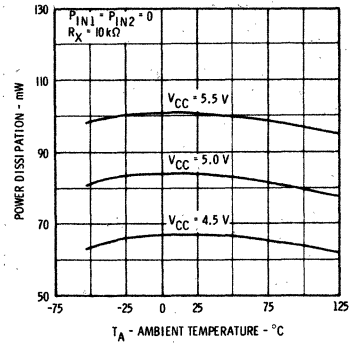


Fig. 7

NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE

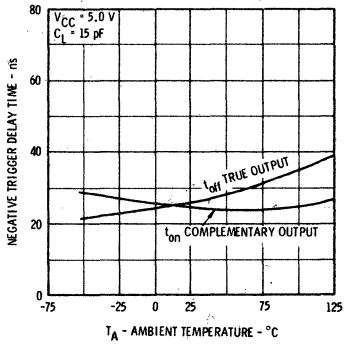


Fig. 8

NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

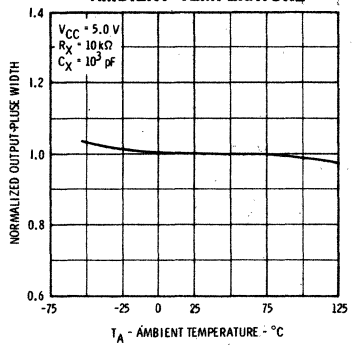


Fig. 9

NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

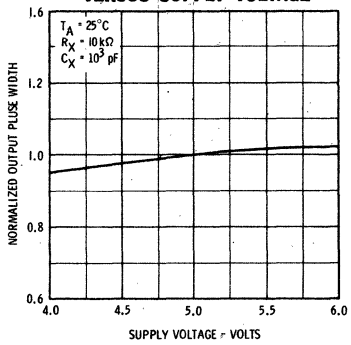


Fig. 10

NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE

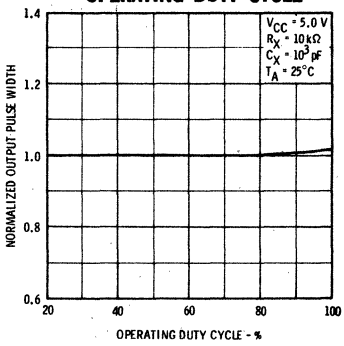


Fig. 11

PULSE WIDTH VERSUS TIMING RESISTANCE

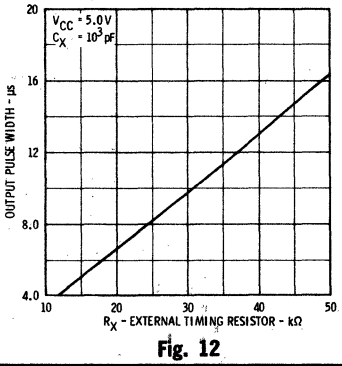


Fig. 12

OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

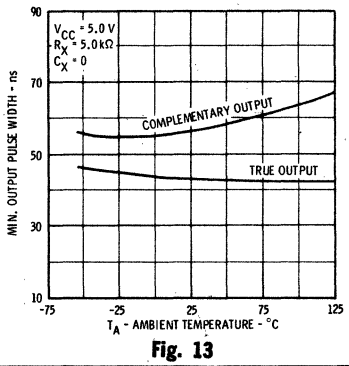


Fig. 13

OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE

For $C_X < 10^3$ pF (For $C_X \geq 10^3$ pF, $t_{pw} = 0.32\, R_X C_X \left(1 + \frac{0.7}{R_X}\right)$

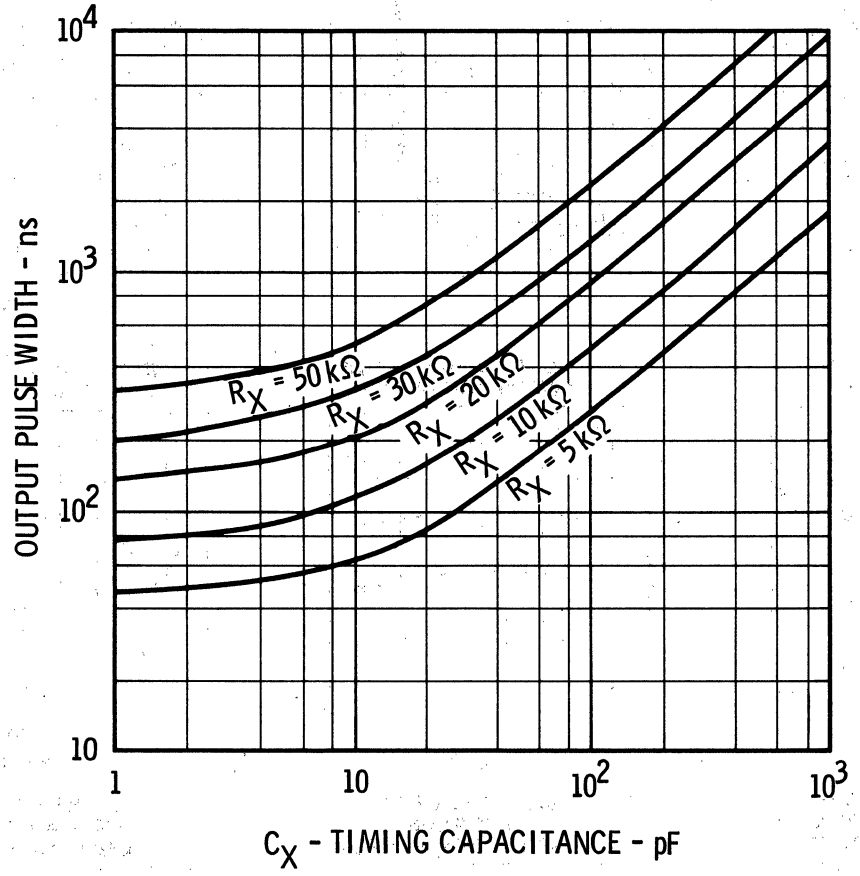
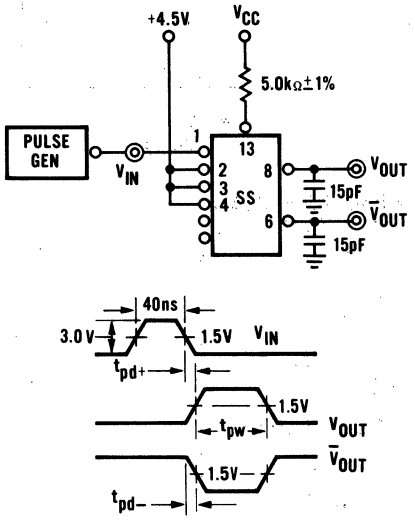


Fig. 14

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: Capacitance includes Jig and Probe

LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

−55°C to +125°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	12
Low	6

0°C to 75°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	16
Low	8

CCSL INPUT LOAD AND DRIVE FACTORS

−55°C to +125°C

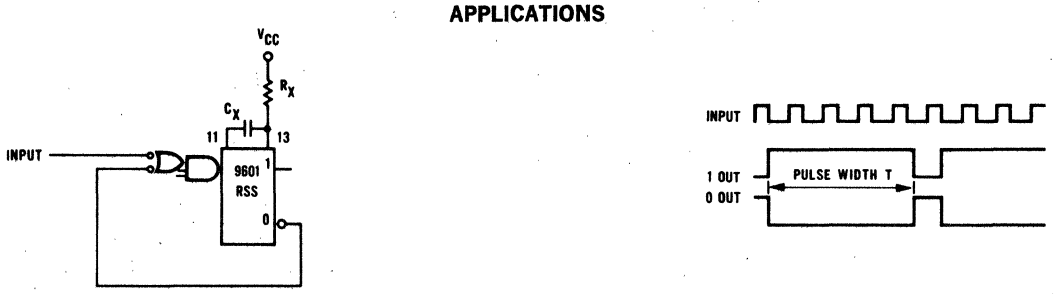
INPUT LEVEL	LOAD FACTOR
High	12
Low	10
OUTPUT STATE	DRIVE FACTOR
High	144
Low	62

0°C to 75°C

INPUT LEVEL	LOAD FACTOR
High	12
Low	10.5
OUTPUT STATE	DRIVE FACTOR
High	192
Low	85

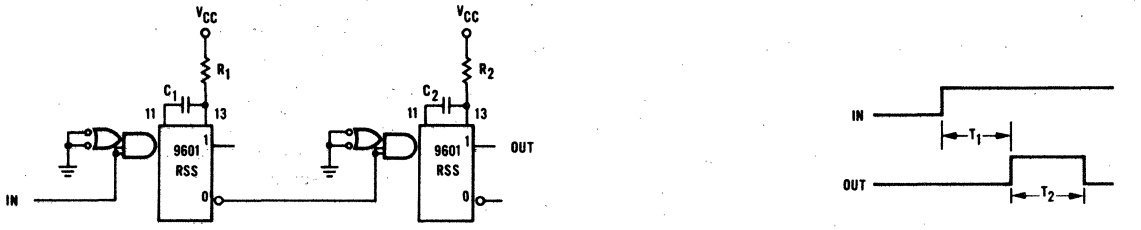
FAIRCHILD RETRIGGERABLE MONOSTABLE MULTIVIBRATOR 9601

APPLICATIONS



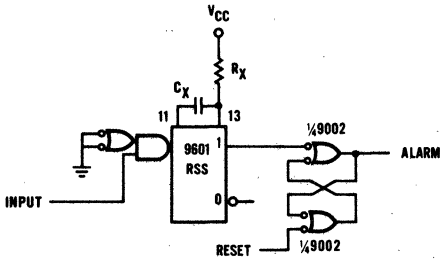
FREQUENCY DIVISION

This configuration makes the 9601 non-retriggerable and capable of frequency division.



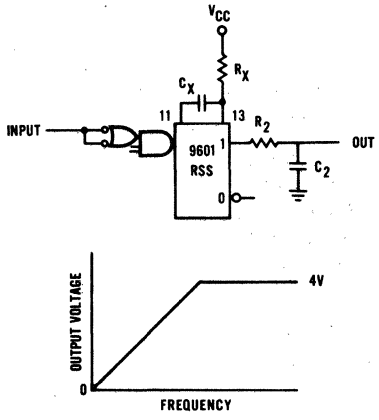
DELAYED PULSE GENERATION

The first 9601 determines the time T_1 before the initiation of the output pulse.
The second 9601 determines T_2, the output pulse width.



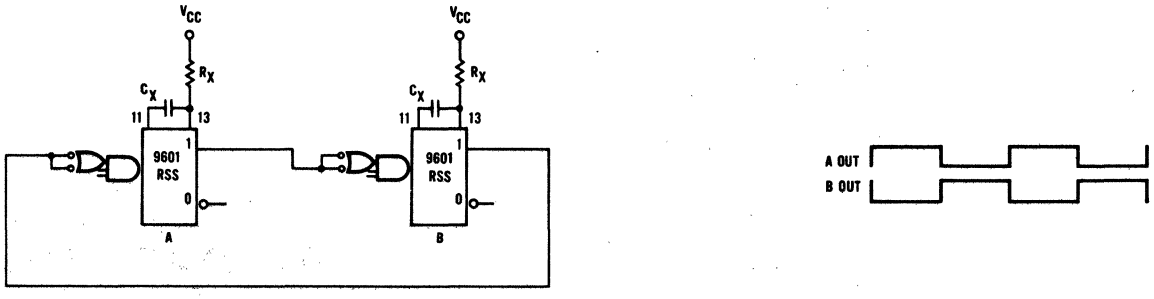
MALFUNCTION INDICATOR

The output of the retriggerable single shot will only remain high if the input frequency is above some fixed value. The input may be a flip flop which normally has a fixed frequency of operation. A system malfunction is indicated when the flip flop frequency drops and retriggering operation of single shot ceases.



DISCRIMINATOR

The 9601 can be used to produce a voltage output proportional to input frequency. For a fixed TC of R_X and C_X, the duty cycle of the output will vary with frequency. This is integrated by R_2 C_2 producing a voltage proportional to frequency.



ASTABLE MULTIVIBRATOR

Frequency of operation is dependent upon value of R_X and C_X.

DIODE-TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS

A FAIRCHILD *COMPATIBLE CURRENT SINKING LOGIC* PRODUCT

MILITARY TEMPERATURE RANGE: −55°C to +125°C

GENERAL DESCRIPTION

The Fairchild 9930 series of Diode Transistor Micrologic is a member of the Compatible Current Sinking Logic (CCSL) family designed for use in systems where good noise immunity, medium speed, medium power, and good fan-out are required. DTμL is available in CERPAK and hermetically sealed Dual In-Line packages over the full military temperature range. Basic members of the family are active low level output AND gates commonly called NAND gates.

Noise immunity is typically 1 volt. Worst case noise immunity over the military temperature range is 400 mV. Power dissipation is typically 8.5 mW per gate function at a 50% duty cycle. The average propagation delay is 30 ns per gate function. A single 5 volt ±10% supply is used.

A variety of gate combinations is available which provides the system designer the utmost in logic flexibility and helps to reduce package requirements to a minimum. Gate outputs may be tied together to perform the wired-OR function. Some gates are provided with 2K pull-up resistors which offer improved propagation delay times. An extender is provided to increase the fan-in for some of the gates.

The 9932 buffer has active pull-up to provide increased capacitive drive and higher fan-out. The 9944 has a bare collector output to allow for wired-OR or driving of low-power lamps. Fan-in for the buffers can be extended with the use of the 9933.

The binary products are direct coupled master-slave flip-flops making operation independent of the clock pulse rise and fall times. The binary products incorporate direct clear, direct set, and buffered outputs to provide output isolation from the slave circuitry.

The V_{CC} and ground terminals of all devices are located on diagonal corners of the package which allow two degrees of freedom in routing of power and ground lines on the P/C boards. Simple loading rules are incorporated so that the fan-in and fan-out capability of each device can be quickly established.

The DTμL 9930 series is compatible with the CCSL devices which include LPDTμL, TTμL, MμL, Medium Scale Integration (MSI), and Micromatrix™ array products.

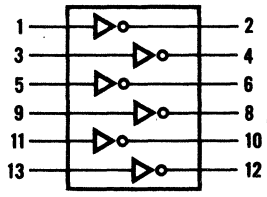
TABLE OF CONTENTS

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

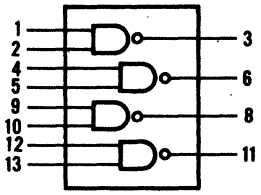
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

9300 SERIES DTμL INTEGRATED CIRCUITS

HEX INVERTERS

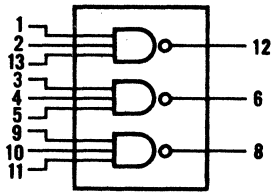


9936, 9937

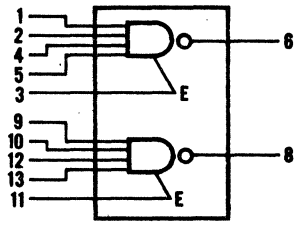


9946, 9949

NAND GATES

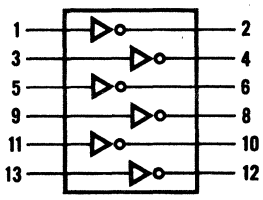


9962, 9963



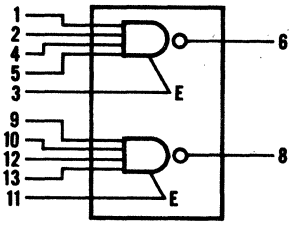
9930, 9961

EXTENDABLE HEX INVERTER



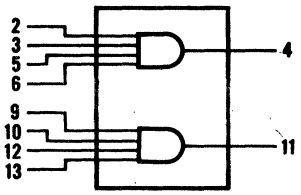
9935

BUFFERS



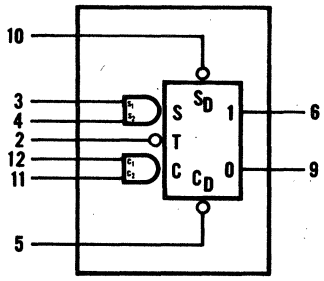
9932, 9944

EXTENDER

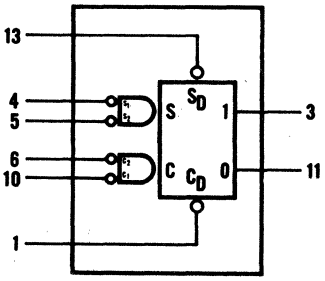


9933

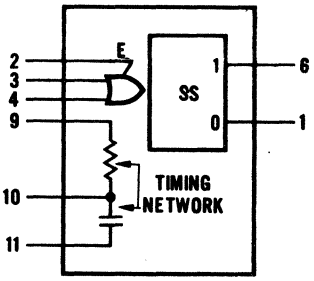
BINARY ELEMENTS



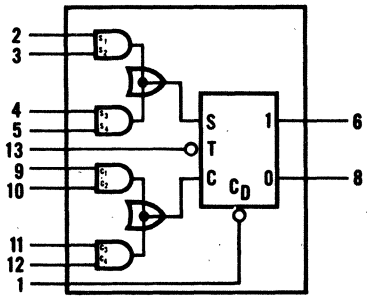
9945, 9948



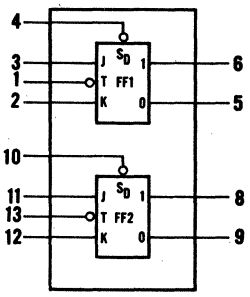
9950



9941, 9951

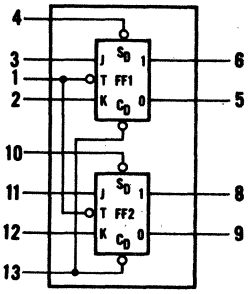


9111



9093, 9094

$V_{CC} = 14$
GND = 7



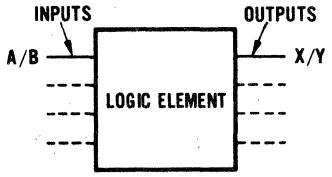
9097, 9099

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65°C to 150°C
Temperature (Ambient) under bias	−55°C to 125°C
V_{CC} pin potential to ground	−0.5 V to +8.0 V
V_{CC}, pulsed 1 second	12 V
Input voltage, applied to input	−1.5 V to 5.5 V
Voltage applied to output when output is high	$+V_{CC}$
Input current, into inputs	1.0 mA
Current into output when output is low (except 9932 & 9944)	30 mA
Current into output when output is low (9932 & 9944)	100 mA
Lead temperature (soldering, 60 seconds)	300°C

LOADING RULES

In this data sheet the following notation has been chosen to indicate the input loading and output drive for all logic elements.



Where
A = high logic level input load factor
B = low logic level input load factor
X = high logic level output drive factor
Y = low logic level output drive factor

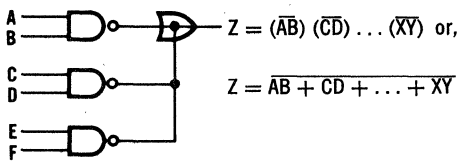
When checking for loading violations it is only necessary to insure that the sum of the high logic level input load factors at any node does not exceed the high logic level output drive factor at that node. The same is true for low logic level load and drive factors. These rules apply only within the DTμL 9930 series. For loading rules to other Fairchild logic elements refer to the CCSL Composite Data Sheet.

Multiplying the factor with the appropriate current per unit load gives the input loading or output drive in terms of current. For the DTμL circuits of this data sheet, current per unit load is -1.5 mA maximum at low logic level and is 5 μA maximum at high logic level.

In the case where unused inputs of an AND gate are shorted to a driven input, the high logic level input load factor for inputs will be the number of inputs shorted together times the high logic level input load factor for one input. The low logic level input load factor for the inputs will be the same as that for a single input.

FANOUT REDUCTION RULES FOR WIRED-OR APPLICATIONS

Each DTμL output has a pull-up resistor connected to the output (except 9932 and 9944 and 9950). In wired-OR applications, any gate must be able to sink the current from all pull-up resistors in addition to the loads connected to the common wired "AND" point. A 6K pull-up resistor represents 0.82 unit loads (U.L.) and a 2K pull-up resistor represents 2.3 U.L. To calculate the load driving capability of a wired-OR configuration simply find the total U.L. contribution of excess pull-up resistors. The FAN-OUT of the wired AND is then the fan-out of the lowest rated fan-out gate in the wired-OR combination minus the excess pull-up resistor contribution.



NAND GATES—9930, 9946, 9949, 9961, 9962, 9963
HEX INVERTERS—9936, 9937

DESCRIPTION

The 9930, 9946 and 9962 are active low NAND gates. The 9936 is a hex inverter with input and output characteristics identical to the NAND gates. The variety of gate combinations provides the system designer the utmost in logic flexibility and reduces package count.

The 9961, 9949, 9937 and 9963 are versions of the 9930, 9946, 9936 and 9962 with 2K collector pullup resistors in place of 6K pullup resistors. These gates have increased speeds and greater high level drive factors over their 6K counterparts.

Fig. 1—LOGIC SYMBOL AND PIN CONFIGURATIONS

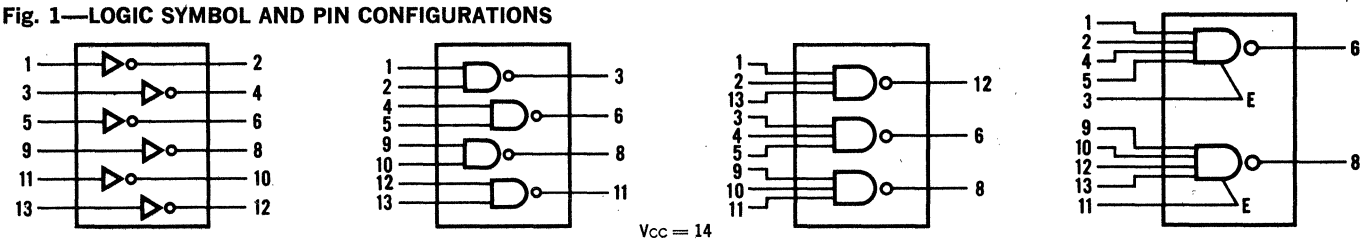
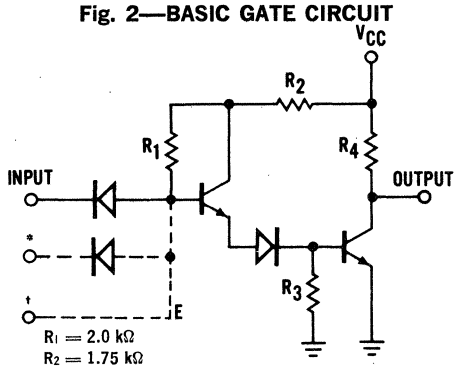


Fig. 2—BASIC GATE CIRCUIT



$R_1 = 2.0$ kΩ
$R_2 = 1.75$ kΩ
$R_3 = 5.0$ kΩ
$R_4 = 6.0$ kΩ (9930, 9936, 9946, 9962)
$R_4 = 2.0$ kΩ (9937, 9949, 9961, 9963)

* Number of inputs depends on the gate.
† 9930 and 9961 only.

Fig. 3—LOADING FACTORS (9930, 9936, 9946, 9962)

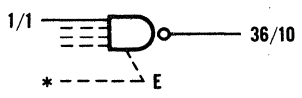
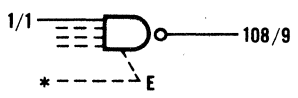


Fig. 4—LOADING FACTORS (9937, 9949, 9961, 9963)



*Extender pin on 9930, 9963 allows increased number of inputs by addition of discrete diodes or extender element DTμL9933.

TABLE I

ELECTRICAL CHARACTERISTICS OF 6K GATES — 9930, 9936, 9946 AND 9962 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$ Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.25	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 15\ mA$ Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5\ V$ | $V_F = 0.4\ V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5\ V$ | 4.0 V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				2.41	3.25			mA	Inputs Open | $V_{CC} = 5.0\ V$
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			25	45	80			ns	$V_{CC} = 5.0\ V$, See Page 6, Fig. 7
t_{pd-}	Turn On Delay			10	20	30			ns	

TABLE II

ELECTRICAL CHARACTERISTICS OF 2K GATES — 9937, 9949, 9961 AND 9963 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.54\ mA$ Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10.8\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 13.5\ mA$ Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5\ V$ | $V_F = 0.4\ V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5\ V$ | 4.0 V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				4.05	5.45			mA	Inputs Open | $V_{CC} = 5.0\ V$
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			10	35	50			ns	$V_{CC} = 5.0\ V$, See Page 6, Fig. 7
t_{pd-}	Turn On Delay			10	20	30			ns	

ELECTRICAL CHARACTERISTICS

Fig. 5a
WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

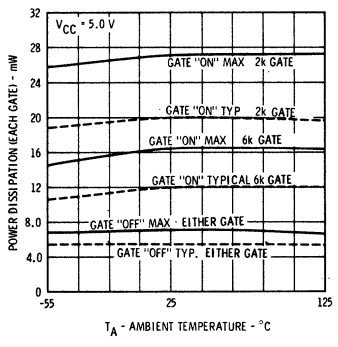


Fig. 5b
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

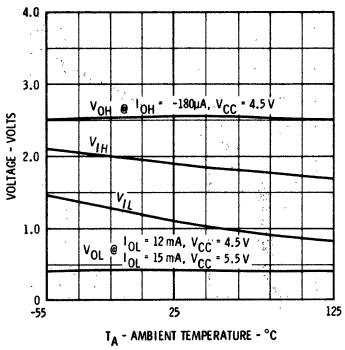


Fig. 5c
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

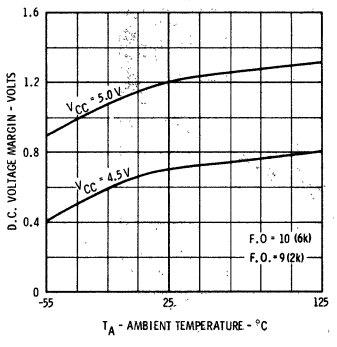


Fig. 5d
WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

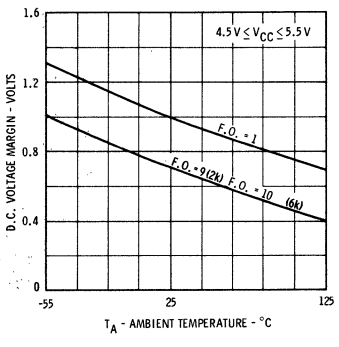


Fig. 5e
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE (6k Gates)

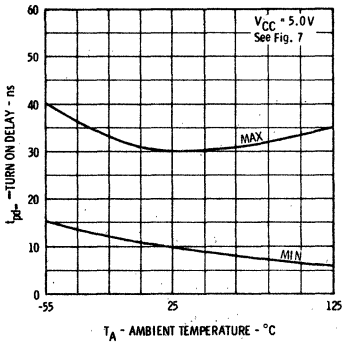


Fig. 5f
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE (6k Gates)

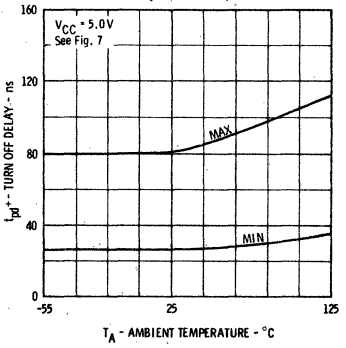


Fig. 5g
INCREASE OF PROPAGATION DELAY VERSUS CAPACITANCE (6k Gates)

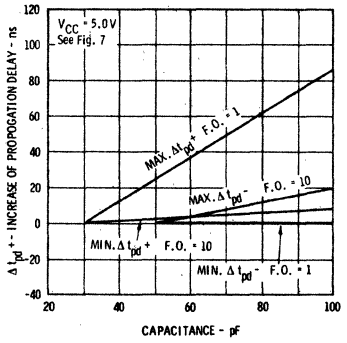


Fig. 5h
DECREASE OF TURN OFF DELAY VERSUS FANOUT (6k Gates)

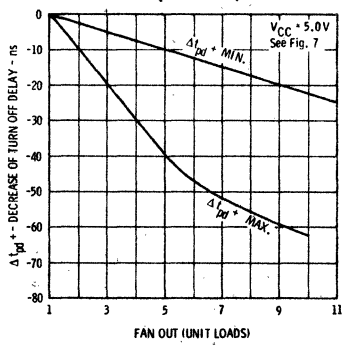


Fig. 5i
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE (2k Gates)

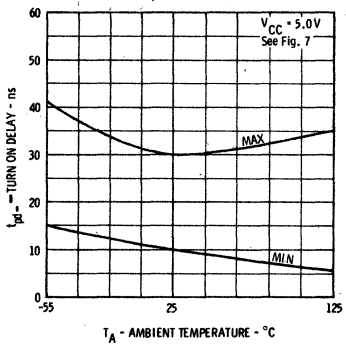


Fig. 5j
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE (2k Gates)

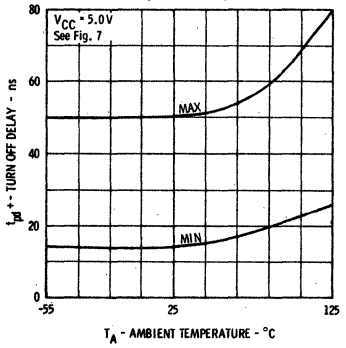


Fig. 5k
INCREASE OF PROPAGATION DELAY VERSUS CAPACITANCE (2k Gates)

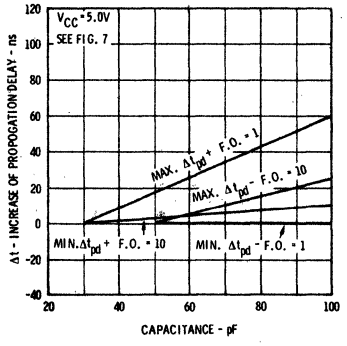
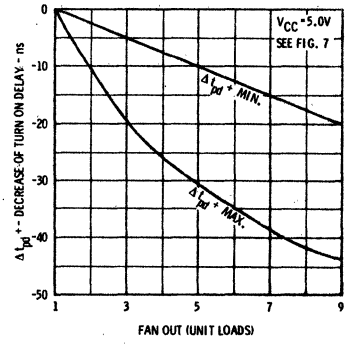


Fig. 5l
DECREASE OF TURN ON DELAY VERSUS FANOUT (2k Gates)



INPUT AND OUTPUT CHARACTERISTICS

Fig. 6a
TYPICAL INPUT CURRENT VERSUS INPUT VOLTAGE (6k & 2k Gates)

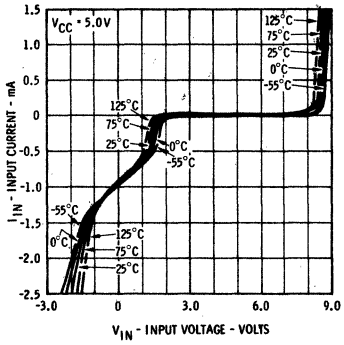


Fig. 6b
TYPICAL OUTPUT VOLTAGE VERSUS INPUT VOLTAGE (6k & 2k Gates)

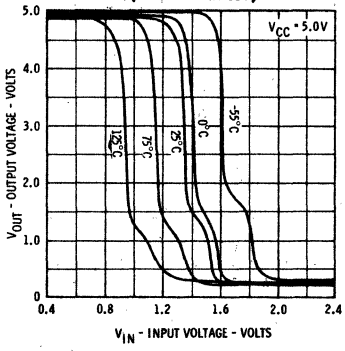


Fig. 6c
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (6k & 2k Gates)

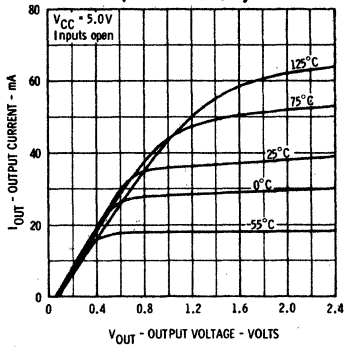


Fig. 6d
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (2k Gates)

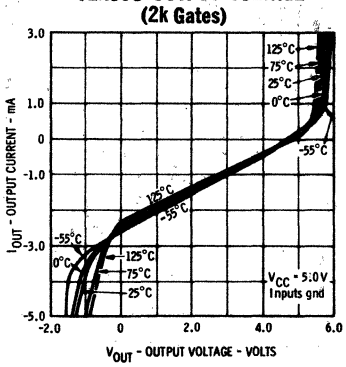


Fig. 6e
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (6k Gates)

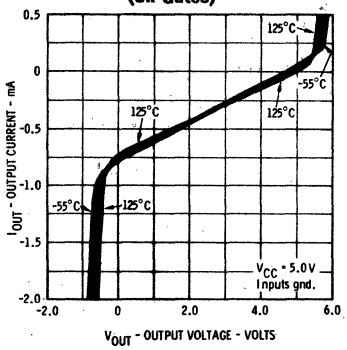
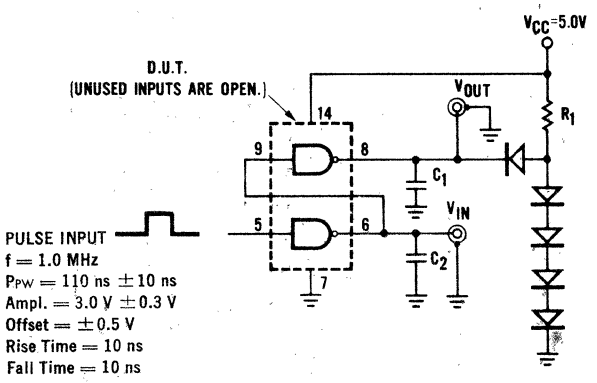
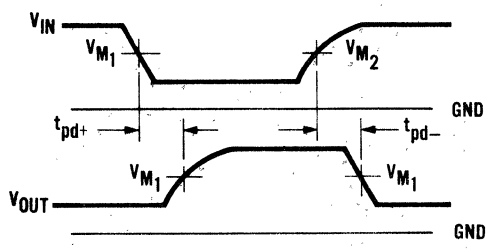


Fig. 7—t_{pd} TEST CIRCUIT AND WAVEFORMS





	t_{pd+}	t_{pd-}
R_1	3.9 kΩ	400 Ω
C_1	30 pF	50 pF
C_2	20 pF	20 pF

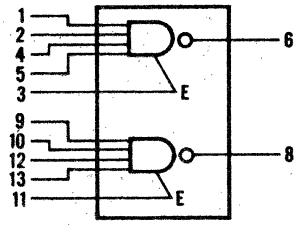
Diodes are FD600.
C_1 and C_2 include all jig and probe capacitance

Temp.	V_{m1} (Volts)	V_{m2} (Volts)
−55°C	1.7	1.5
25°C	1.5	1.3
125°C	1.2	1.0

BUFFER ELEMENTS—9932 AND 9944

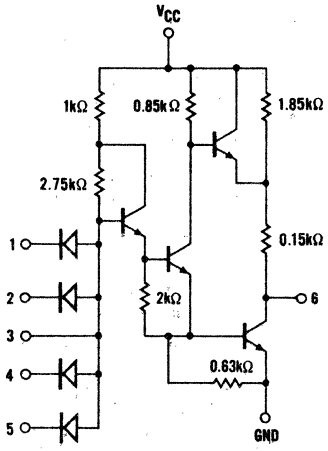
The DTμL 9932 and DTμL 9944 are dual "NAND" power gates capable of driving and sinking large currents for high fan-out applications. The DTμL 9932 features an emitter-follower output pull-up, which provides a high fan-out device with superior capacitance-driving capability. The DTμL 9944 is intended as a high fan-out gate interface driver, or low power lamp driver.

Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION 9932, 9944



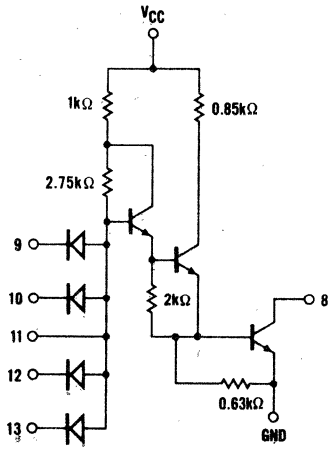
V_{CC} = 14
GND = 7

Fig. 2—SCHEMATIC DIAGRAM OF THE DTμL 9932 ELEMENT (ONE GATE)



V_{CC} = 14
GND = 7

Fig. 3—SCHEMATIC DIAGRAM OF THE DTμL 9944 ELEMENT (ONE GATE)



V_{CC} = 14
GND = 7

Fig. 4—LOADING FACTORS (9932)

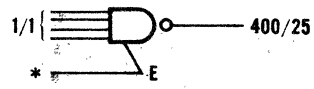
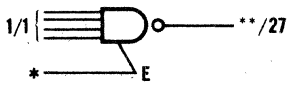


Fig. 5—LOADING FACTORS (9944)



NOTES:

1. Extender pin (*) allows increased number of inputs by addition of discrete diodes or extender element DTμL9933.
2. (**) denotes the need for an external resistor to provide high level drive capability. The use of an external resistor will then detract from the low level drive factor as follows; subtract one (1) fan-out for every 3.4 kΩ path from V_{CC} to output.
3. 9932 outputs cannot be wired-OR.

TABLE I
ELECTRICAL CHARACTERISTICS — 9932 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6	2.8		2.5		Volts	$V_{CC} = 4.5\ V$, Inputs at V_{IL} (See Below); $I_{OH} = -2.0$ mA at −55°C, $= -2.5$ mA at 25°C, $= -4.0$ mA at 125°C
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 36$ mA; $V_{CC} = 5.5\ V$, $I_{OL} = 37.5$ mA; Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current					2.0		5.0	μA	$V_R = 4.0\ V$ Other inputs grounded
I_{PD}	V_{CC} Current "Gate On"				10	13.3			mA	$V_{CC} = 5.0\ V$, Inputs Open
(per gate)	V_{CC} Current "Gate Off"				1.15	1.47			mA	$V_{CC} = 5.0\ V$, Inputs Grounded
t_{pd+}	Turn Off Delay			25	50	80			ns	$V_{CC} = 5.0\ V$, See Page 8, Fig. 7
t_{pd-}	Turn On Delay			15	25	40			ns	

TABLE II
ELECTRICAL CHARACTERISTICS — 9944 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 36$ mA; $V_{CC} = 5.5\ V$, $I_{OL} = 37.5$ mA; Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_{CEX}	Output Leakage		50			100		200	μA	$V_{CEX} = 4.5\ V$ Inputs at V_{IL} (see above)
I_F	Input Load Current		−1.5		−1.3	−1.5		−1.4	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.16		−1.0	−1.16		−1.08	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				0.02	2.0		5.0	μA	$V_R = 4.0\ V$ Other inputs grounded
I_{PD}	V_{CC} Current "Gate On"				7.6	10			mA	$V_{CC} = 5.0\ V$, Inputs Open
(per gate)	V_{CC} Current "Gate Off"				1.15	1.47			mA	$V_{CC} = 5.0\ V$, Inputs Grounded
t_{pd+}	Turn Off Delay			15	35	50			ns	$V_{CC} = 5.0\ V$, See Page 8, Fig. 8
t_{pd-}	Turn On Delay			10	20	35			ns	

9932 AND 9944 ELECTRICAL CHARACTERISTICS

Fig. 6a
WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

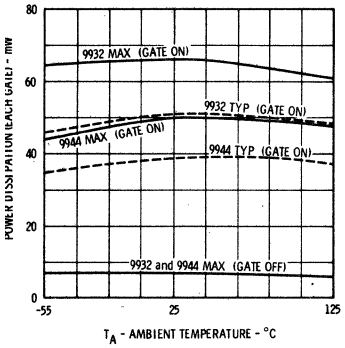


Fig. 6b
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

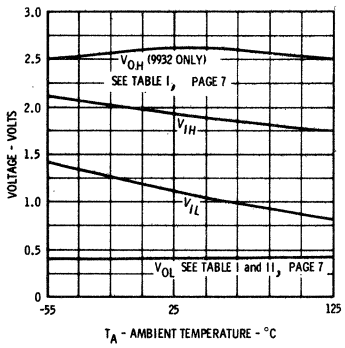


Fig. 6c
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE (9932 ONLY)

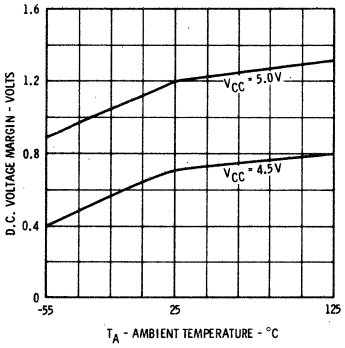


Fig. 6d
WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

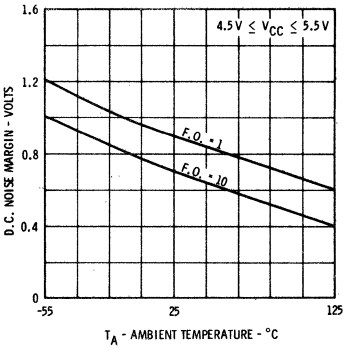


Fig. 6e
TYPICAL INPUT CURRENT VERSUS INPUT VOLTAGE

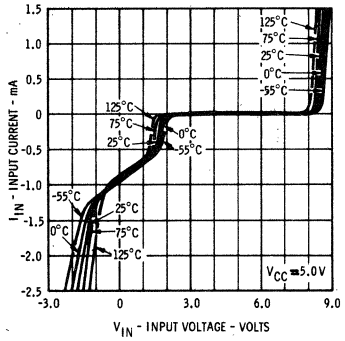


Fig. 6f
TYPICAL OUTPUT VOLTAGE VERSUS INPUT VOLTAGE (9932 ONLY)

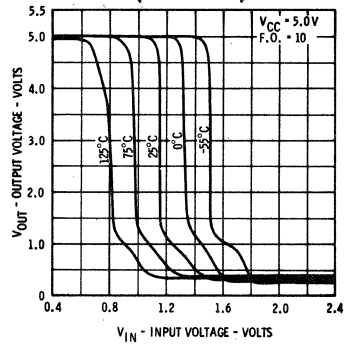


Fig. 6g
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (9932 ONLY)

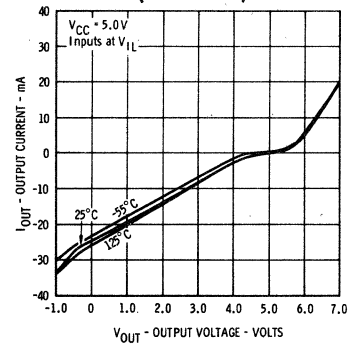
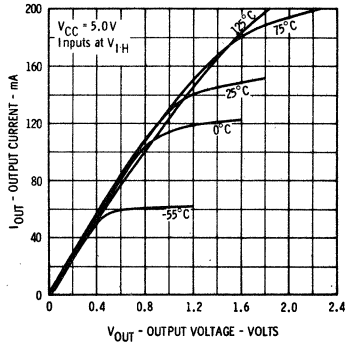
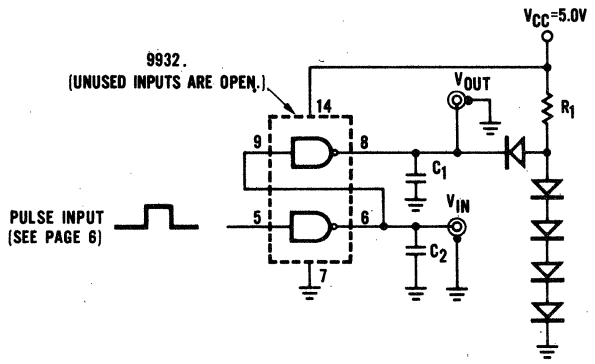


Fig. 6h
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



SWITCHING CHARACTERISTICS

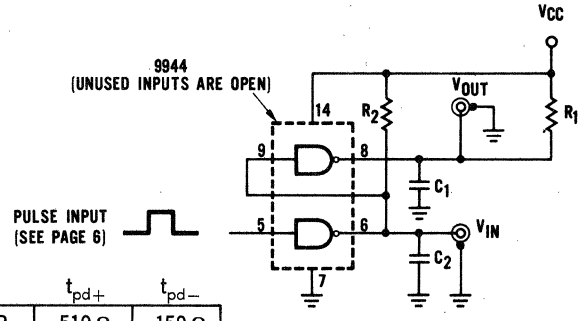
Fig. 7—t_{pd} TEST CIRCUIT FOR DTμL 9932 ELEMENT



	t_{pd+}	t_{pd-}
R_1	510 Ω	150 Ω
C_1	500 pF	500 pF
C_2	20 pF	20 pF

All Diodes are FD600 or Equivalent
C_1 and C_2 include Probe and Jig Capacitance

Fig. 8—t_{pd} TEST CIRCUIT FOR DTμL 9944 ELEMENT



	t_{pd+}	t_{pd-}
R_1	510 Ω	150 Ω
R_2	2 kΩ	2 kΩ
C_1	20 pF	100 pF
C_2	20 pF	20 pF

Fig. 9—WAVEFORMS FOR 9932 AND 9944

Temp.	V_M (Volts)
−55°C	1.7
25°C	1.5
125°C	1.2

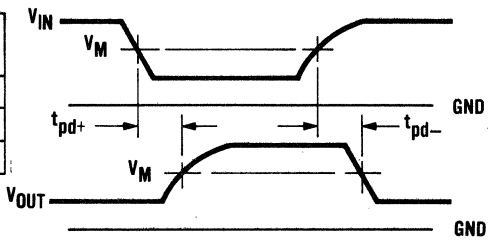


Fig. 10a
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

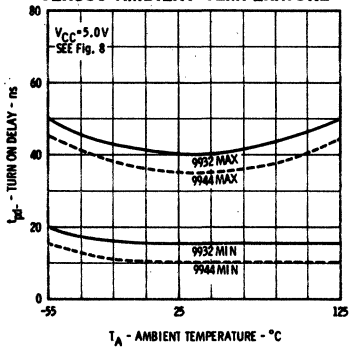


Fig. 10b
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

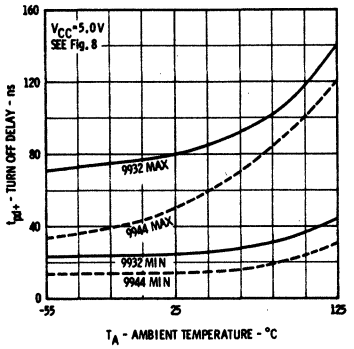
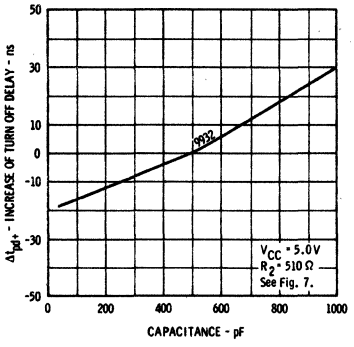


Fig. 10c
INCREASE OF TURN OFF DELAY VERSUS CAPACITANCE



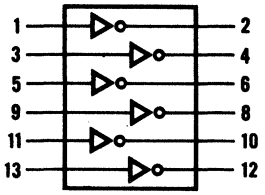
EXTENDABLE HEX INVERTER — 9935

A 9935 inverter is intended for use with discrete diode expansion of the input. Input load and drive factors can be calculated with the aid of the curves on Page 11 and the forward/reverse characteristics of the diode used.

A single 9935 inverter can be driven directly by the outputs of other DTμL elements, with the exception of 9932 and 9950, providing no more than 5 mA is allowed to flow into the input of the 9935. Commoning 9935 inputs is not a recommended configuration.

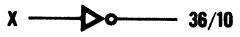
When extending inputs with diodes, care should be taken to minimize capacitance on the input node as turn on delay will be increased by 2 ns per picofarad of stray capacitance at this node.

Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION



V_{CC} = 14
GND = 7

Fig. 3—LOADING FACTORS



X = input to be used with 9933 or discrete diode.

Fig. 2—SCHEMATIC DIAGRAM (ONE INVERTER ONLY)

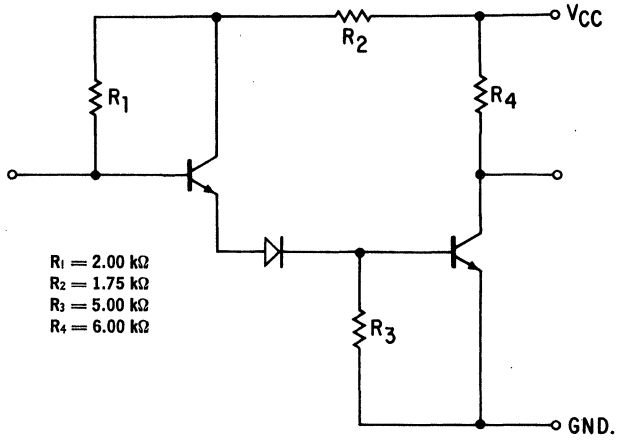


TABLE I

ELECTRICAL CHARACTERISTICS — 9935 (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage		2.5		3.5	2.6		2.5	Volts	V_{CC} = 4.5 V, I_{OH} = −0.18 mA Inputs at V_{IL}
V_{OL}	Output Low Voltage		0.4		0.25	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 12 mA V_{CC} = 5.5 V, I_{OL} = 15 mA Inputs at V_{IH}
V_{IH}	Input High Voltage	2.3		2.0			1.8		Volts	Guaranteed input high threshold with FD600 diode
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold with FD600 diode
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.5	mA	V_{CC} = 5.5 V, V_F = 0.4 V — FD600 Diode
			−1.2		−0.93	−1.2		−1.2	mA	V_{CC} = 4.5 V, V_F = 0.4 V — on input
I_{PD} (per gate)	V_{CC} Current "Gate On"				2.41	3.1			mA	V_{CC} = 5.0 V, Inputs open
	V_{CC} Current "Gate Off"				1.33	1.7			mA	V_{CC} = 5.0 V, Inputs gnd.
t_{pd+}	Turn Off Delay			25	65	80			ns	V_{CC} = 5.0 V, See Page 10, Fig. 5
t_{pd-}	Turn On Delay			10	30	40			ns	

9935 ELECTRICAL CHARACTERISTICS

Fig. 4a
WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE (EACH INVERTER)

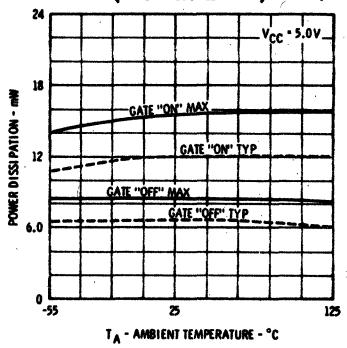


Fig. 4b
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

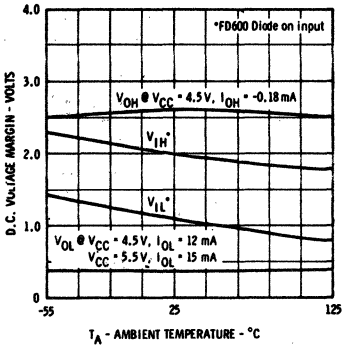


Fig. 4c
HIGH INPUT THRESHOLD VOLTAGE VERSUS FORWARD EXTENDER DIODE VOLTAGE

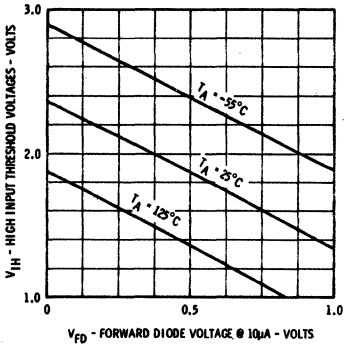


Fig. 4d
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

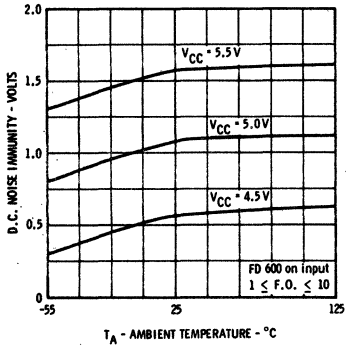


Fig. 4e
WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

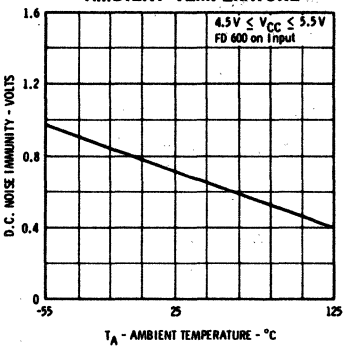


Fig. 4f
LOW INPUT THRESHOLD VOLTAGE VERSUS FORWARD DIODE VOLTAGE

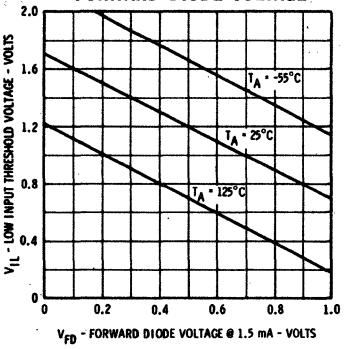


Fig. 4g
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

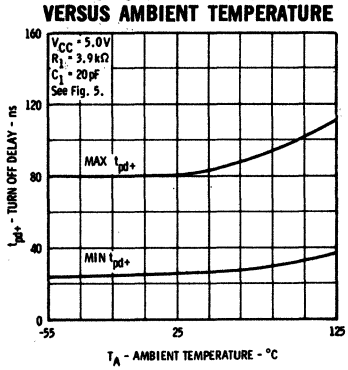


Fig. 4h
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

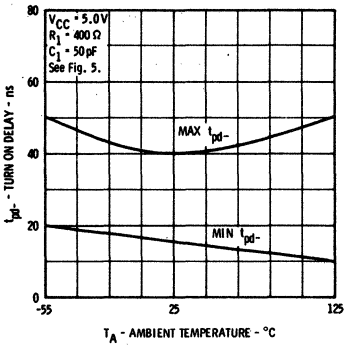
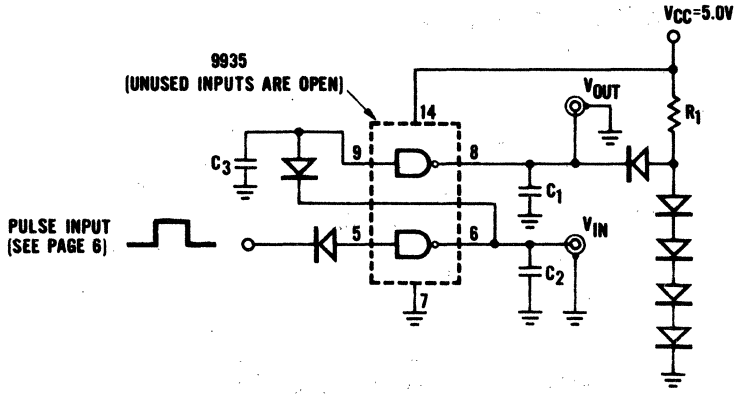


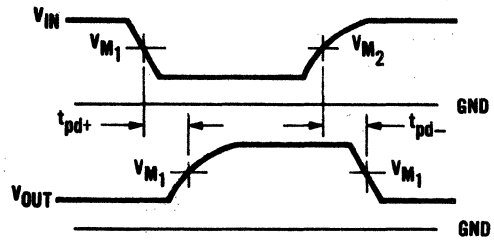
Fig. 5—SWITCHING TIME TEST CIRCUIT



	t_{pd+}	t_{pd-}
R_1	3.9 k	400 Ω
C_1	30 pF	50 pF
C_2	20 pF	20 pF
C_3	5 pF	5 pF

Diodes are FD600 or equivalent

C_1 and C_2 include Jig and Probe Capacitance



Temp.	V_{m1} (Volts)	V_{m2} (Volts)
−55°C	1.7	1.5
+25°C	1.5	1.3
+125°C	1.2	1.0

DTμL EXTENDER ELEMENT—9933

The DTμL 9933 is a dual four-input extender element. DTμL 9933 elements may be used to extend fan-in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the element to which they are connected.
Typical input capacitance of DTμL 9933 is 2.0 pF and output capacitance is 5.0 pF.

Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION

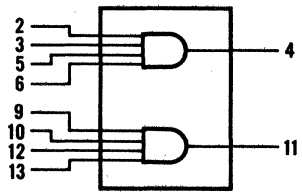
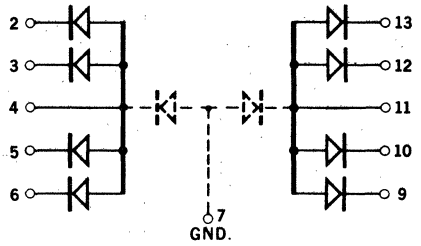


Fig. 2—SCHEMATIC DIAGRAM



9933 ELECTRICAL CHARACTERISTICS

Fig. 3a TYPICAL FORWARD AND REVERSE CHARACTERISTICS (WITH 9933)

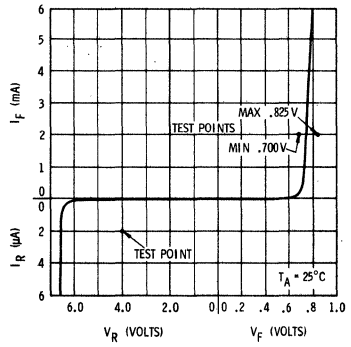


Fig. 4a WORST CASE PROPAGATION DELAY VERSUS EXTENDER PIN CAPACITANCE (WITH 9930, 9935, 9963)

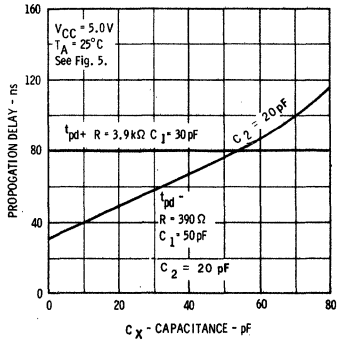


Fig. 4b WORST CASE PROPAGATION DELAY VERSUS EXTENDER PIN CAPACITANCE (WITH 9932)

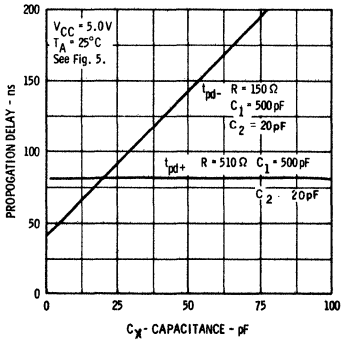
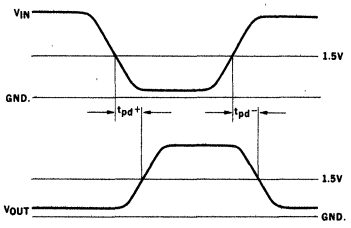
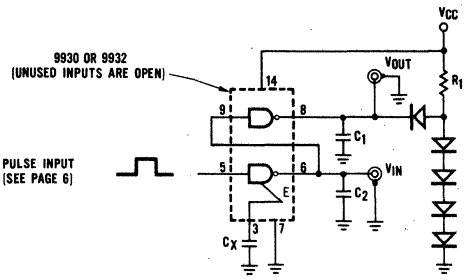


Fig. 5—WAVEFORMS AND TEST CIRCUIT





Diodes are FD600

C_X represents the summation of the DTμL 9933 Dual Extender Element output capacitances (~5.0 pF per output) and associated board, connector and wiring capacitances.

Typical Curves to Show the Effects of Extender Pin Capacitance on Noise Threshold of DTμL9930 Dual Gate

Fig. 6a PULSED GROUND NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE

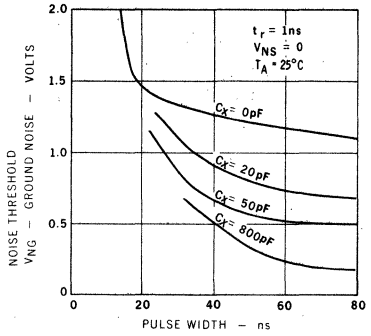


Fig. 6b PULSED SIGNAL LINE NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE

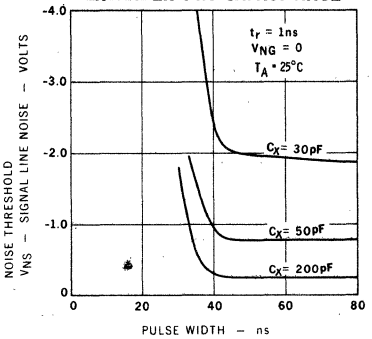
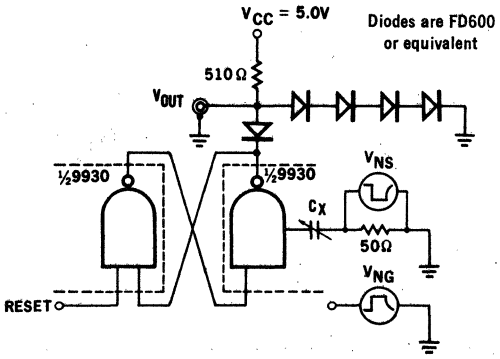


Fig. 6c TEST CONDITIONS



R-S FLIP-FLOPS 9945, 9948 AND 9111
DUAL J-K FLIP-FLOPS 9093, 9094, 9097 AND 9099

GENERAL DESCRIPTION

The DTμL 9930 series has seven flip-flops to satisfy the storage requirements of a logic system. Four flip-flops are dual J-K designs with buffered outputs, allowing the wired-OR configuration to be used. The other three flip-flops operate in the R-S mode and can be converted to J-K operation with external cross-coupled connections. All flip-flops incorporate the master-slave design which offers the advantage of a D.C. threshold on the clock input initiating the transition of the outputs, so that careful control of the clock pulse rise and fall times is not required.

Data is accepted by the master flip-flop while the clock is high. Refer to truth table for definition of "one" and "zero" levels. Transfer from the master flip-flop to the slave flip-flop occurs on the high to low transition of the clock. When the clock is low, the J, K, S, and C inputs are inhibited.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions on the clock and synchronous inputs. Both asynchronous set and clear are provided on the 9945, 9948, 9097 and 9099. The 9093 and 9094 have only asynchronous set inputs, and the 9111 has only asynchronous clear inputs.

LOGIC DIAGRAMS AND LOADING FACTORS

Fig. 1—9945

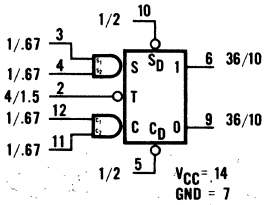


Fig. 2—9093

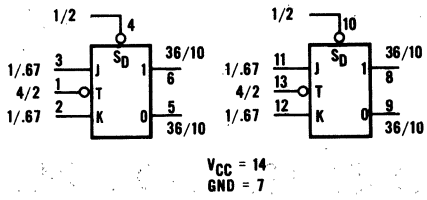


Fig. 3—9948

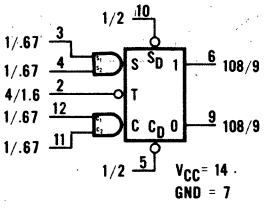


Fig. 4—9094

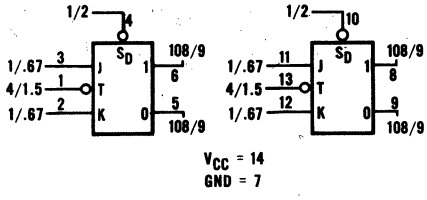


Fig. 5—9111

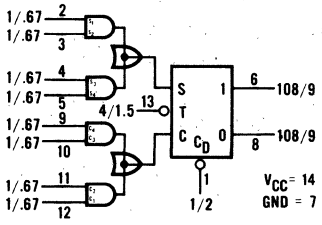


Fig. 6—9097

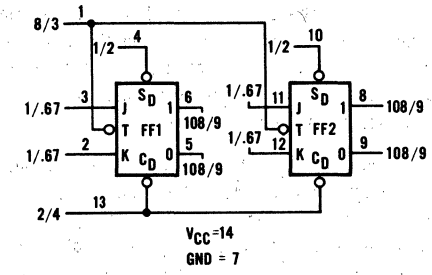


Fig. 7 9945/9948 (J-K MODE)

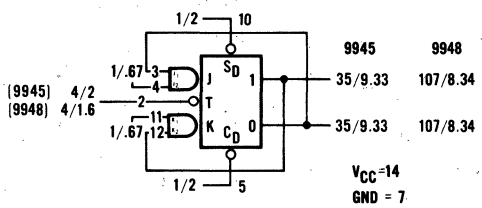
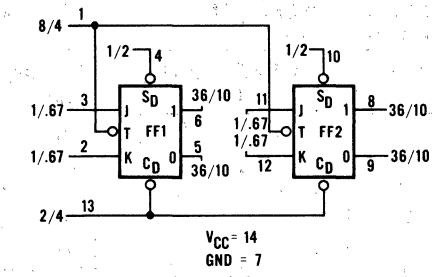


Fig. 8 9099



FUNCTIONAL LOGIC DIAGRAMS

Fig. 9—9945, 9948 AND 9111

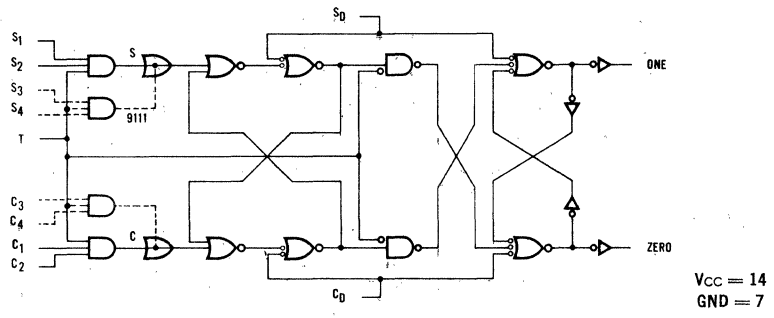
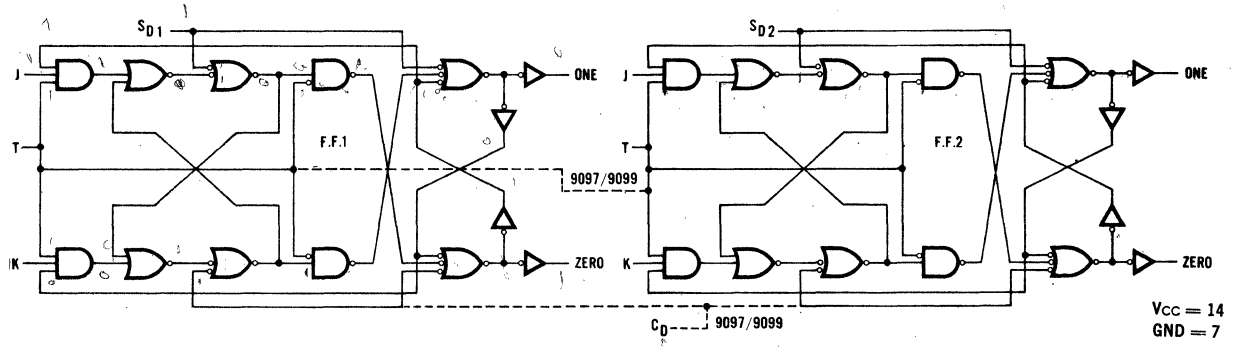


Fig. 10—9093, 9094, 9097 AND 9099



SYNCHRONOUS OPERATION

The truth table defines the next state of the flip-flop after a high to low transition of the clock pulse. The output of all flip-flops operating in the J-K mode is a function of the previous state of the flip-flop and the condition of the inputs prior to a high to low transition of the clock. The output of all flip-flops operating in the R-S mode is a function of the S and C inputs at the time of a high to low clock transition.

The S and C inputs in the table refer to the basic S and C inputs as indicated on the logic diagrams of the 9945, 9948, and 9111. These internal inputs are the result of a logic operation on the external S and C inputs. This operation is represented symbolically by "AND" gates in the logic diagram for each flip-flop. Logic diagrams are in accordance with MIL STANDARD 806B.

The L* symbol in the J, K, C, and S input columns is defined as that input does not go high at any time while the clock is high.

The H* symbol in the J, K, C, and S input columns is defined as that the input is high at some time while the clock is high.

The X symbol indicates that the condition of that input or output has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state high and low voltage levels, respectively.

TABLE I
SYNCHRONOUS OPERATION
R-S FLIP-FLOP

BEFORE CLOCK OUTPUTS		BEFORE CLOCK INPUTS		OUTPUTS AFTER CLOCK	
ONE	ZERO	S	C	ONE	ZERO
L	H	L*	L*	L	H
H	L	L*	L*	H	L
X	X	L	H*	L	H
X	X	H*	L	H	L
X	X	H	H	Undetermined	

TABLE II
SYNCHRONOUS OPERATION
J-K FLIP-FLOP

BEFORE CLOCK OUTPUTS		BEFORE CLOCK INPUTS		OUTPUTS AFTER CLOCK	
ONE	ZERO	J	K	ONE	ZERO
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

TABLE III
ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
S_D	C_D	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	State determined by synchronous inputs and clock input	

ELECTRICAL CHARACTERISTICS—BINARY ELEMENTS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage									
	(9945, 9093, 9099)	2.5		2.5	3.3		2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -180\ \mu A$
	(9948, 9094, 9097, 9111)	2.5		2.5	3.3		2.5			$V_{CC} = 4.5\ V$, $I_{OH} = -540\ \mu A$
V_{OL}	Output Low Voltage		0.4		0.25	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.0\ mA$
	(9945, 9093, 9099)									$V_{CC} = 5.5\ V$, $I_{OL} = 15.0\ mA$
	(9948, 9094, 9097, 9111)		0.4		0.25	0.4		0.4		$V_{CC} = 4.5\ V$, $I_{OL} = 13.0\ mA$ (@ −55°C)
										$V_{CC} = 5.5\ V$, $I_{OL} = 13.6\ mA$
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_R	Input Leakage, all J-K S, C, S_D, C_D inputs (except C_D of 9097, 9099)					2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ Gnd on other inputs
	Input Leakage of C_D (9097, 9099)					4.0		10		
I_{RCP}	Input Leakage, CP inputs									
	(9945, 9948, 9093, 9094, 9111)					10		20		
	(9097, 9099)					20		40		
I_F	Input Current, all J, K, S, C inputs		−.98		−.82	−.98		−.92	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ 4.0 V on other inputs
	Input Current, S_D or C_D (9093, 9094, 9111)		−2.2		−1.8	−2.2		−1.93		
	Input Current, CP inputs									
	(9945, 9093)		−2.93		−2.40	−2.93		−2.57		
	(9948, 9094)		−2.35		−1.93	−2.35		−2.03		
	(9111)		−3.76		−3.00	−3.76		−3.76		
	(9097)		−4.68		−3.84	−4.68		−4.04		
	(9099)		−5.86		−4.81	−5.86		−5.14		
I_F	Input Current, all J, K, S, C inputs		−0.76		−0.62	−0.76		−0.72	mA	$V_{CC} = 4.5\ V$
	Input Current, S_D or C_D inputs (9093, 9094, 9111)		−1.7		−1.39	−1.7		−1.5		$V_F = 0.4\ V$ 4.0 V on other inputs
	Input Current, CP inputs									
	(9945, 9093)		−2.26		−1.85	−2.26		−2.02		
	(9948, 9094)		−1.83		−1.50	−1.83		−1.59		
	(9111)		−2.90		−2.48	−2.90		−2.88		
	(9097)		−3.66		−3.00	−3.66		−3.18		
	(9099)		−4.52		−3.70	−4.52		−4.04		
I_{FSI}	Input Current, C_D, S_D inputs		−2.93		−2.40	−2.93		−2.57	mA	$V_{CC} = 5.5\ V$ | $V_F = 0.4\ V$
	(9945, 9948, 9097, 9099)		−2.26		−1.85	−2.26		−2.20		$V_{CC} = 4.5\ V$ | 4.0 V on other inputs
I_{PD}	V_{CC} Current									
	(9945)				8.3	14.0			mA	$V_{CC} = 5.0\ V$, all inputs open Momentary ground on S_D
	(9948)				9.9	16.2				
	(9111)				12.1	18.0				
	(9093)				16.6	28.0				
	(9094)				19.8	32.4				
	(9097)				19.8	32.4				
	(9099)				16.6	28.0				

INPUT AND OUTPUT CHARACTERISTICS OF BINARY ELEMENTS

Fig. 11
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

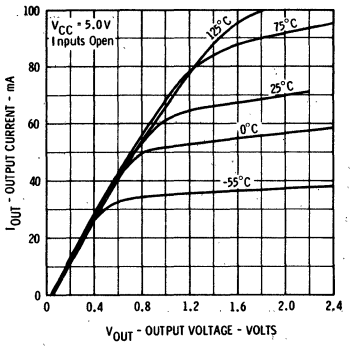


Fig. 12
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

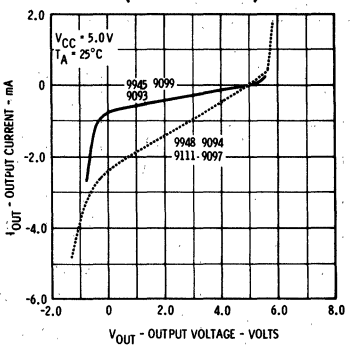


Fig. 13
CLOCK INPUT CURRENT VERSUS CLOCK INPUT VOLTAGE (9945, 9093, 9099)

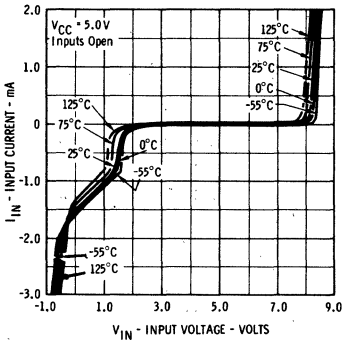


Fig. 14
INPUT CURRENT VERSUS INPUT VOLTAGE - CLOCK INPUT (9948, 9094)

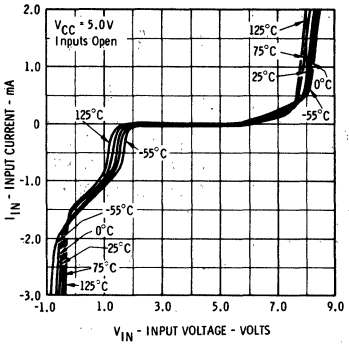


Fig. 15
INPUT CURRENT VERSUS INPUT VOLTAGE CLOCK INPUT (9111)

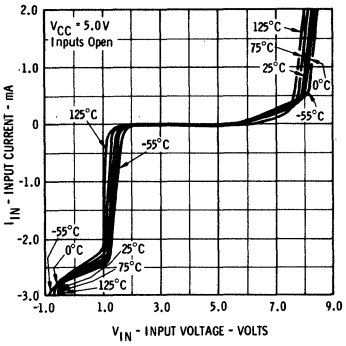


Fig. 16
INPUT CURRENT VERSUS INPUT VOLTAGE CLOCK INPUT (9097)

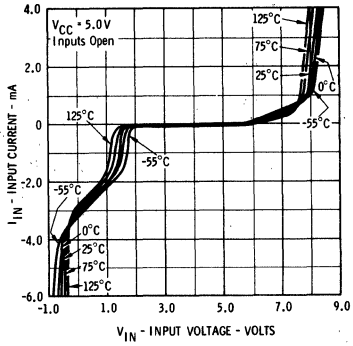


Fig. 17
CLOCK INPUT CURRENT VERSUS CLOCK INPUT VOLTAGE (9099)

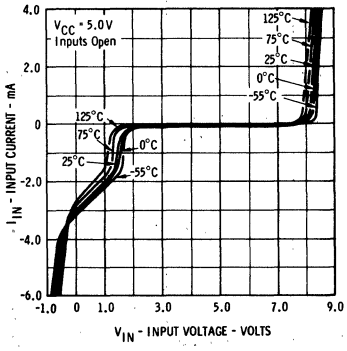


Fig. 18
INPUT CURRENT VERSUS INPUT VOLTAGE SYNCHRONOUS INPUTS

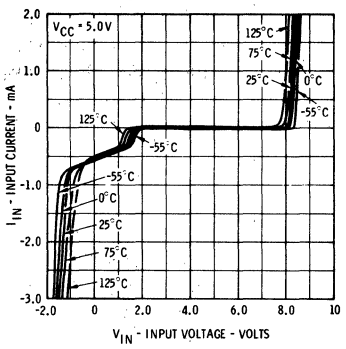


Fig. 19
INPUT CURRENT VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS

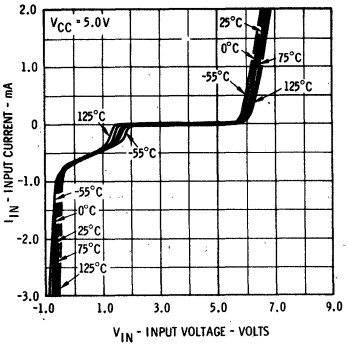


Fig. 20
OUTPUT VOLTAGE VERSUS CLOCK INPUT VOLTAGE (9945, 9093, 9099)

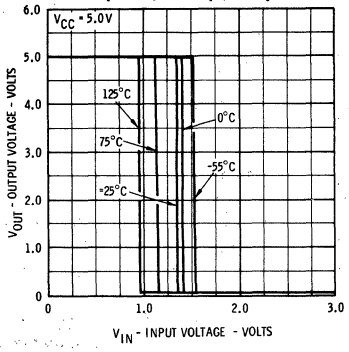


Fig. 21
OUTPUT VOLTAGE VERSUS CLOCK INPUT VOLTAGE (9948, 9094, 9097)

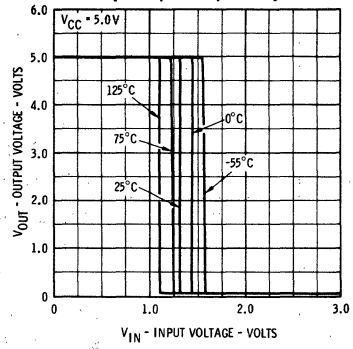
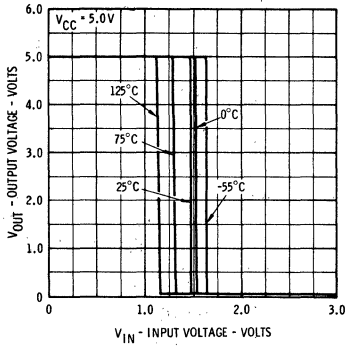


Fig. 22
OUTPUT VOLTAGE VERSUS ASYNCHRONOUS INPUT VOLTAGE



SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

SYMBOL	CHARACTERISTIC	9094, 9097, 9111 and 9948 MIN.	TYP.	MAX.	9093, 9099 and 9945 MIN.	TYP.	MAX.	UNITS	FIGURES
t_{pd+}	Clock to Output	30		65	35		75	ns	28, 29, 30
t_{pd-}	Clock to Output	30		75	30		75	ns	
$t_{set\text{-}up}$		35	22		35	22		ns	
$t_{release}$			14	10		14	10	ns	

Fig. 23
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

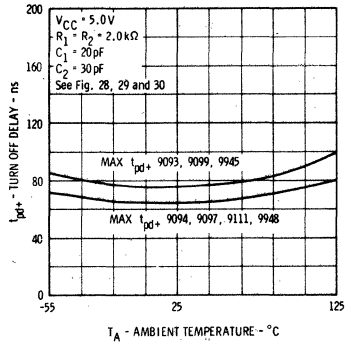


Fig. 24
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

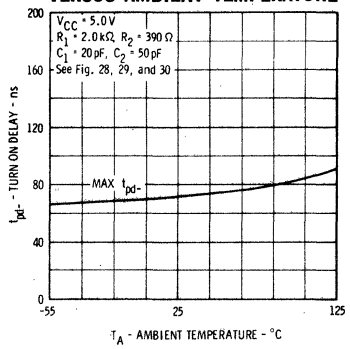


Fig. 25
WORST CASE INCREASE OF PROPAGATION DELAY VERSUS CAPACITANCE

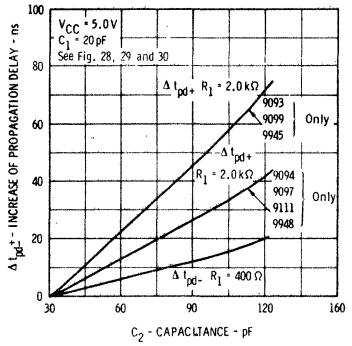


Fig. 26
DECREASE OF TURN OFF DELAY VERSUS FANOUT

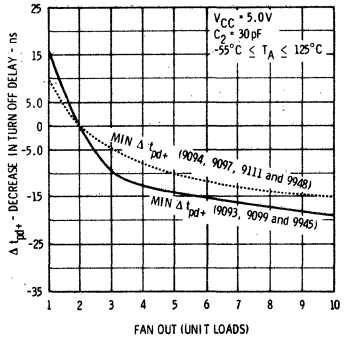
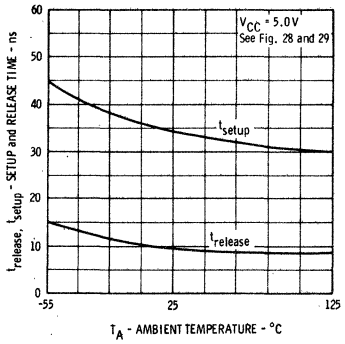


Fig. 27
WORST CASE SET UP AND RELEASE TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TEST CIRCUITS, $T_A = 25°C$, $V_{CC} = 5.0\ V$

Fig. 28—9945 AND 9948

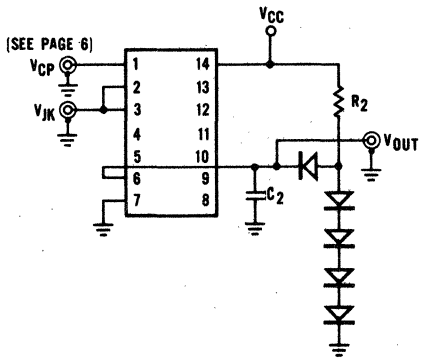


Fig. 29—9093, 9094, 9097 AND 9099

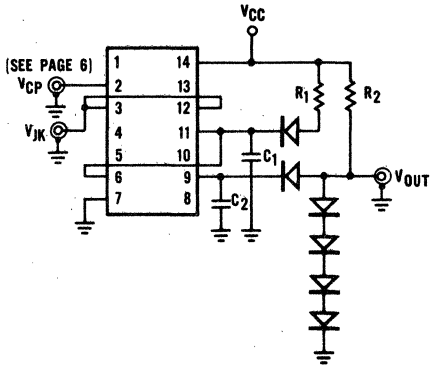


Fig. 30—9111

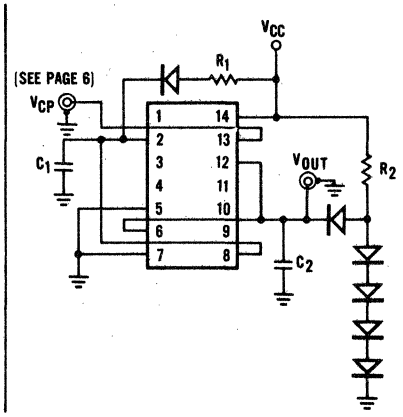


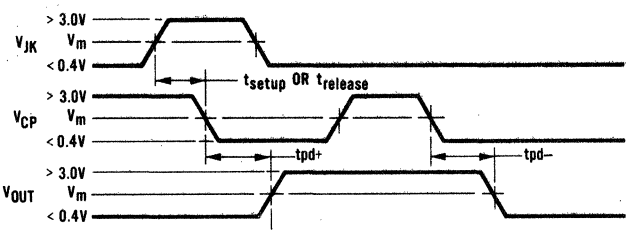
Fig. 31—WAVEFORMS

LOADS

	t_{pd+}	t_{pd-}
R_1	2.0 kΩ	2.0 kΩ
R_2	2.0 kΩ	390 Ω
C_1	20 pF	20 pF
C_2	30 pF	50 pF

MEASURING VOLTAGE THRESHOLDS (V_{in})

Temp	Vm
−55°C	1.7 V
25°C	1.5 V
125°C	1.2 V



All capacitances include probe and jig capacitance
All diodes FD600 or equivalent

SWITCHING TEST NOTES

t_{pd+} and t_{pd-}

Drive the clock pulse input with a suitable pulse source. t_{pd+} and t_{pd-} delays are defined in the waveforms Fig. 31.

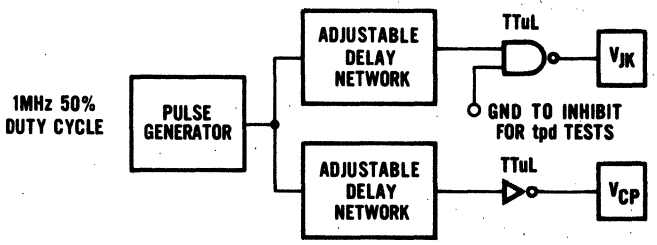
$t_{set\text{-}up}$

1. $t_{set\text{-}up}$ is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the high state of the clock in order for the flip-flop to respond to the data.
2. The test for $t_{set\text{-}up}$ is performed by adjusting the timing relationship between the V_{CP} and V_{JK} pulse to the $t_{set\text{-}up}$ minimum value. A device that passes the test will have the output waveform shown in Fig. 31. The output of a device that does not pass the $t_{set\text{-}up}$ test will remain at a static level (no switching will occur).

$t_{release}$

1. $t_{release}$ is defined as the maximum time allowed for a high to be present at a synchronous logic input at any time during the high state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

Fig. 32—RECOMMENDED INPUT PULSE SOURCES



DTμL9932 buffers with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

Fig. 33—9945 AND 9948 SCHEMATIC DIAGRAM

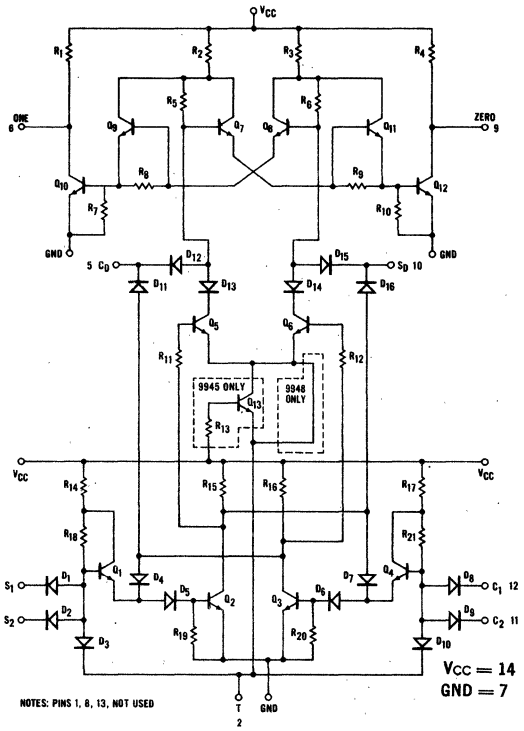
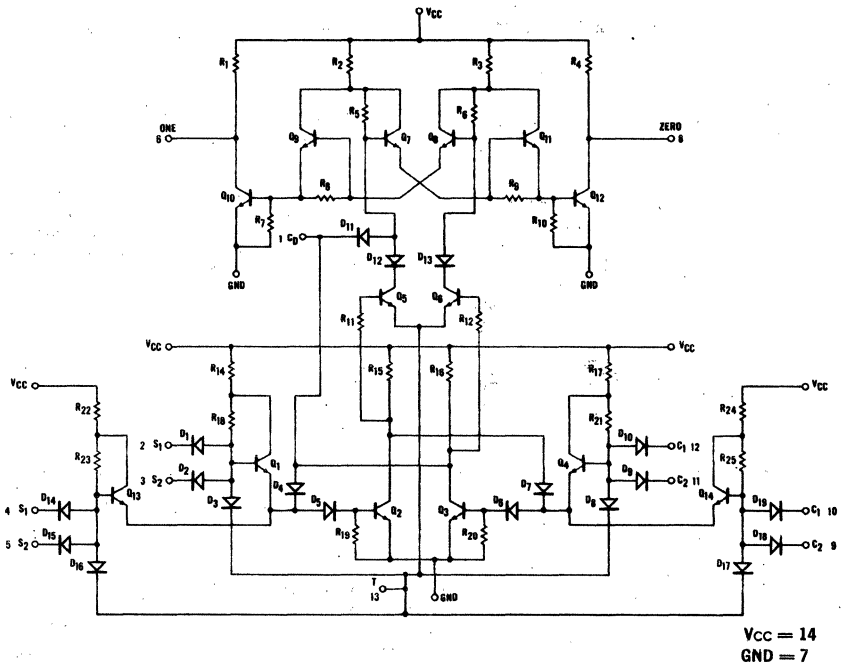


Fig. 34—9111 SCHEMATIC DIAGRAM

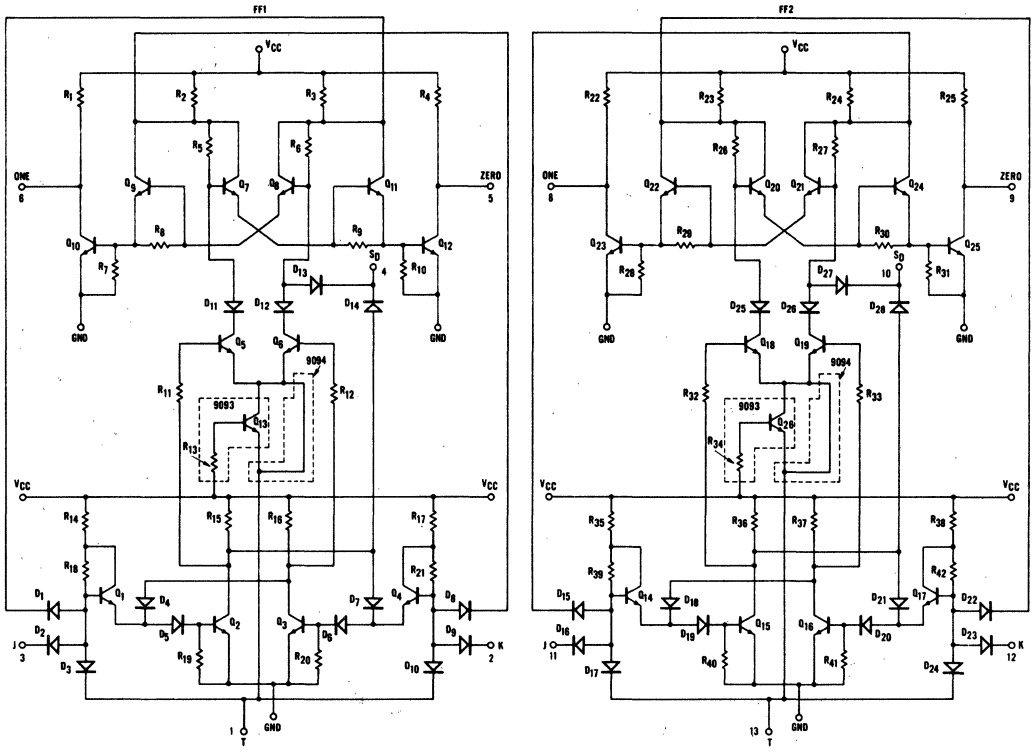


RESISTOR VALUES 9945, 9948 AND 9111

R_1, R_4 = 6.0 kΩ (9945)
= 2.0 kΩ (9948, 9111)
R_2, R_3 = 2.2 kΩ
R_5, R_6, R_{18}, R_{21}, R_{23}, R_{25} = 3.5 kΩ
R_{15}, R_{16} = 3.2 kΩ
R_7, R_{10} = 1.2 kΩ
R_8, R_9 = 3.0 kΩ
R_{11}, R_{12}, R_{19}, R_{20} = 9.0 kΩ
R_{13} = 10 kΩ
R_{14}, R_{17}, R_{22}, R_{24} = 2.5 kΩ

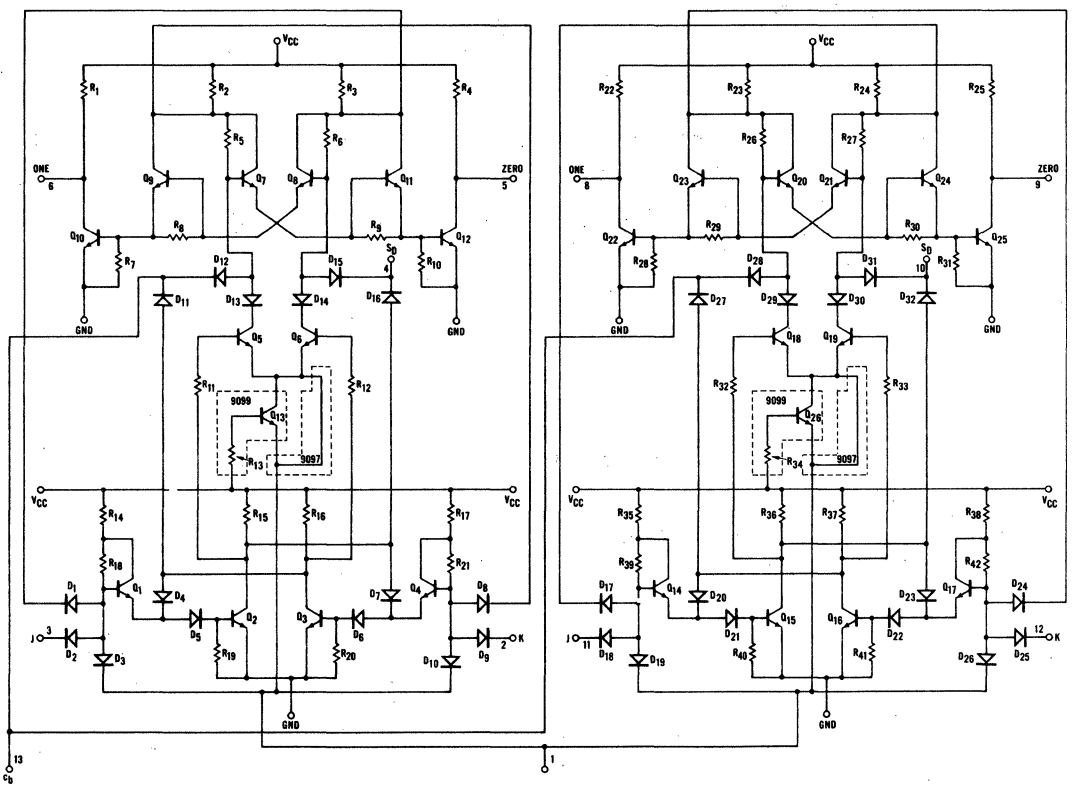
SCHEMATIC DIAGRAMS

Fig. 35—9093 AND 9094



$V_{CC} = 14$
GND = 7

Fig. 36—9097 AND 9099



$V_{CC} = 14$
GND = 7

Resistor Values: 9093, 9094, 9097, 9099

R_1, R_4, R_{22}, R_{25} = 6.0 kΩ (9093, 9099)
= 2.0 kΩ (9094, 9097)
R_2, R_3, R_{23}, R_{24} = 2.2 kΩ

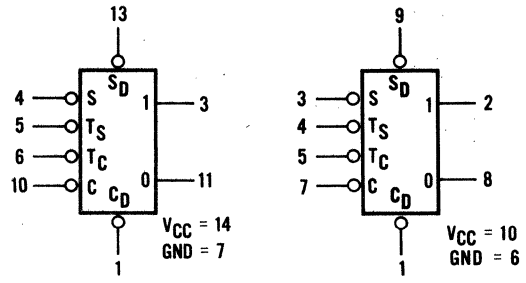
R_5, R_6, R_{18}, R_{21}, R_{26}, R_{27}, R_{39}, R_{42} = 3.5 kΩ
R_7, R_{10}, R_{28}, R_{31} = 1.2 kΩ
R_8, R_9, R_{29}, R_{30} = 3.0 kΩ
R_{11}, R_{12}, R_{19}, R_{20}, R_{32}, R_{33}, R_{40}, R_{41} = 9.0 kΩ

R_{13}, R_{26} = 10 kΩ
R_{14}, R_{17}, R_{35}, R_{38} = 2.5 kΩ
R_{15}, R_{16}, R_{36}, R_{37} = 3.2 kΩ

BINARY ELEMENT — 9950

The DTμL 9950 is an A-C coupled R-S flip-flop.

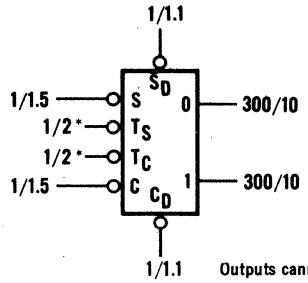
Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION



14 PIN DIP OR FLATPACK

TO-100 PACKAGE

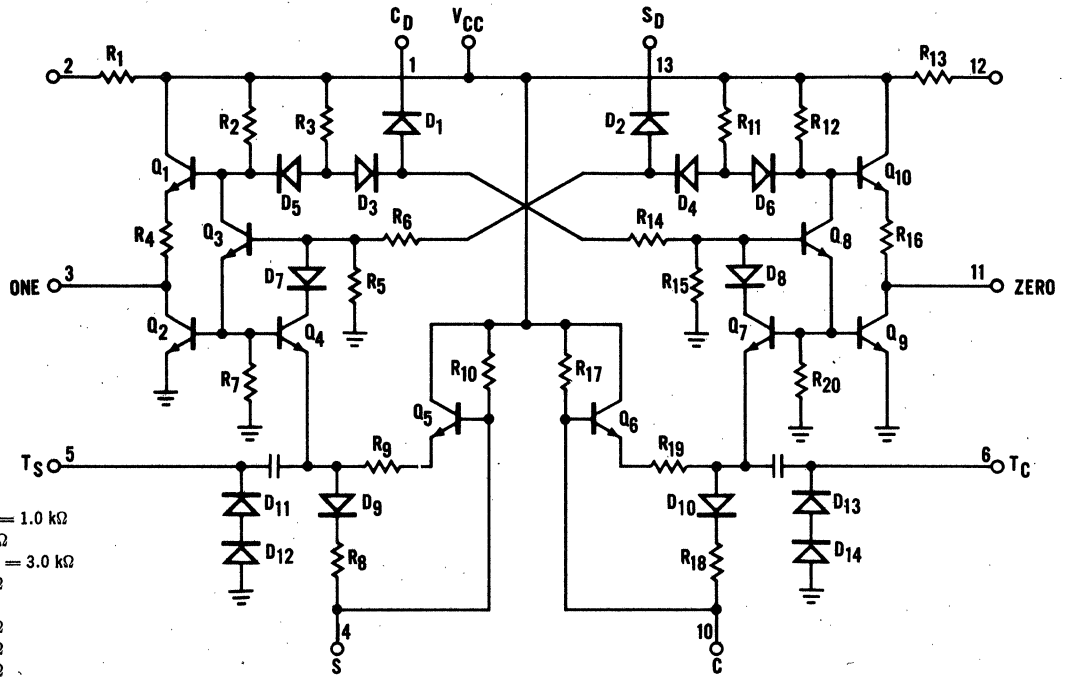
Fig. 2—LOADING RULES



Outputs cannot be wired-OR

* CAPACITIVE INPUTS

Fig. 3—SCHEMATIC DIAGRAM



R_1, R_9, R_{13}, R_{19} = 1.0 kΩ
R_2, R_{12} = 2.0 kΩ
R_3, R_{10}, R_{11}, R_{17} = 3.0 kΩ
R_4, R_{16} = 200 Ω
R_5, R_{15} = 6.5 Ω
R_6, R_{14} = 520 Ω
R_7, R_{20} = 750 Ω
R_8, R_{18} = 100 Ω
C_1, C_2 = 30 pF

V_{CC} = 14
GND = 7

TRUTH TABLE — TABLE I

RESPONSE TO

PULSE INPUTS						DIRECT INPUTS			
INPUTS				OUTPUTS		INPUTS		OUTPUTS	
4	5	6	10	3	11	1	13	3	11
H	X	H	X	NC	NC	H	H	NC	NC
X	H	X	H	NC	NC	L	H	L	H
L	L	X	H	H	L	H	L	H	L
L	L	H	X	H	L	L	L	H	H
H	X	L	L	L	H				
X	H	L	L	L	H				
L	L	L	L	AMBIGUOUS					

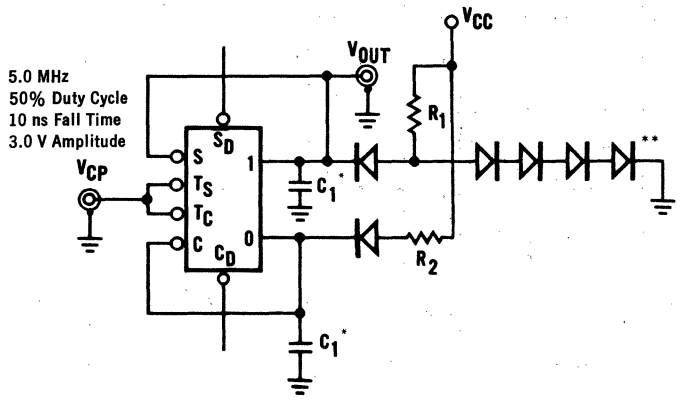
NOTES:

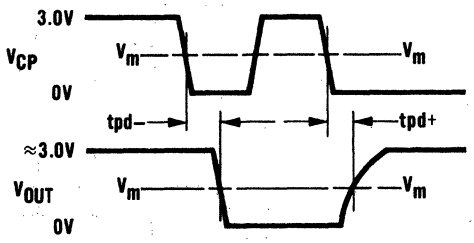
1. Abbreviations used in the body of tables:
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (in all cases, open pins have the same effect as high.)
   X = immaterial, either H or L has equal effect
   NC = no change, the trigger-pulse has no effect on outputs
2. H or L for pins 5 and 6 represent voltage transitions to the level indicated rather than the levels themselves.
3. The tables assume independent use of pulsed inputs and direct inputs. Otherwise, direct inputs will predominate.

TABLE I —
ELECTRICAL CHARACTERISTICS 9950 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.5\ mA$
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 15\ mA$
V_{IHS}	Asynchronous Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed high threshold for asynchronous inputs
V_{ILS}	Asynchronous Input Low Voltage		.95			.80		.605	Volts	Guaranteed low threshold for asynchronous inputs
I_R	Input Leakage					2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ Asynchronous inputs only
I_F	Input Load Current		−2.22			−2.22		−2.09	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_F	Input Load Current		−1.83			−1.83		−1.71	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_{FSI}	Asynchronous Input Load Current		−1.64			−1.64		−1.46	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_{FSI}	Asynchronous Input Load Current		−1.20			−1.24		−1.14	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_{PD}	V_{CC} Current		8.7		6.7	8.7		8.7	mA	$V_{CC} = 5.0\ V$, Input 4 gnd.
t_{pd+}	Turn Off Delay					30			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay					30			ns	See Fig. 4
	Toggling Frequency			20					MHz	

Fig. 4—t_{pd} TEST CIRCUIT





$V_m = 1.5\ V$ @ 25°C
$= 1.2\ V$ @ 125°C
$= 1.7\ V$ @ −55°C

* Includes probe and jig capacitance
** All diodes FD600 or equivalent

	R_1	R_2	C_1
t_{pd+}	3.9 kΩ	2.0 kΩ	100 pF
t_{pd-}	390Ω	2.0 kΩ	100 pF
20 MHz toggle	∞	∞	5.0 pF

MONOSTABLE MULTIVIBRATORS — 9941, 9951

The DTμL 9941 and 9951 are monostable multivibrators designed for use with other members of the DTμL family. They provide complementary output pulses which are typically 100 ns wide. This pulse width is adjustable by the addition of external components.

The TTμL 9601 is a retriggerable one shot having several features which are superior to the 9941 and 9951. It is therefore recommended for new system designs in preference to the 9941 or 9951.

Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION

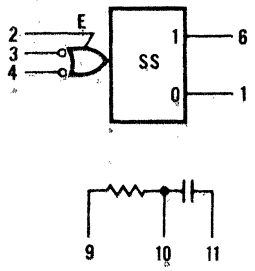
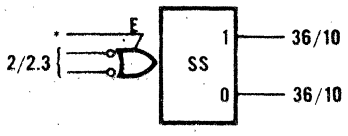
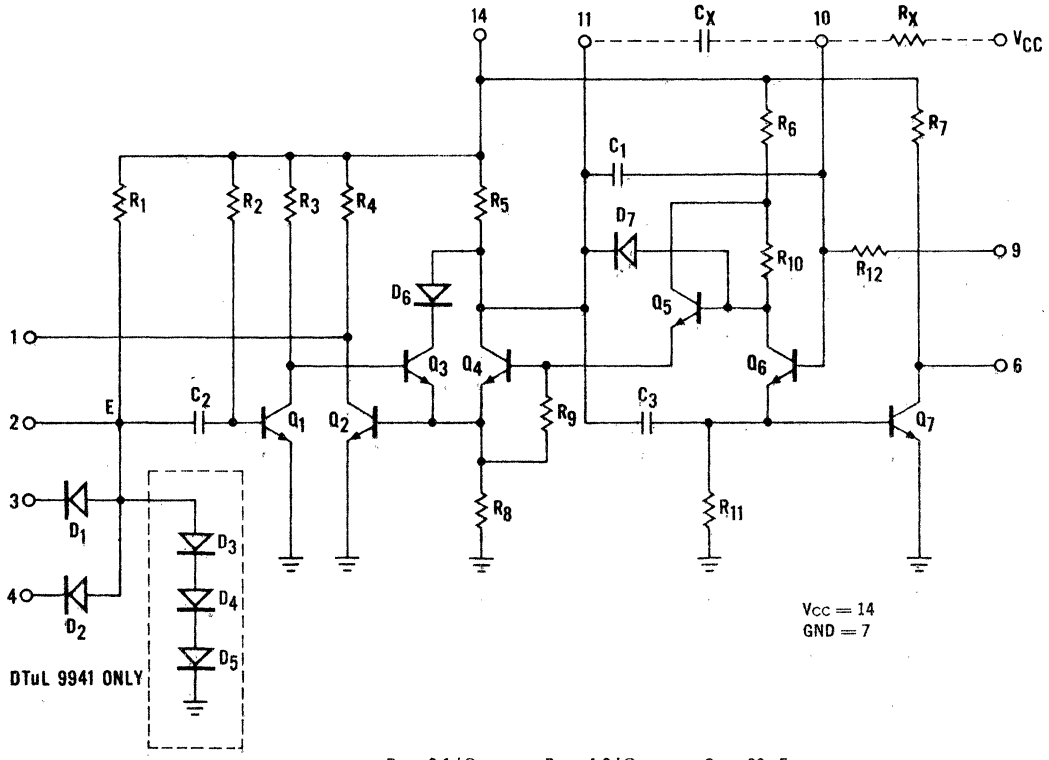


Fig. 2—LOADING FACTORS



1. Outputs can be wire "AND"ed
2. Extender pin allows increased number of inputs by addition of discrete diodes or extender element DTμL9933.

Fig. 3—SCHEMATIC DIAGRAM



$R_1 = 2.1\ k\Omega$	$R_7 = 4.0\ k\Omega$	$C_1 = 20\ pF$
$R_2 = 7.0\ k\Omega$	$R_8 = 1.2\ k\Omega$	$C_2 = 25\ pF$
$R_3 = 2.4\ k\Omega$	$R_9 = 3.6\ k\Omega$	$C_3 = 15\ pF$
$R_4 = 4.0\ k\Omega$	$R_{11} = 24\ k\Omega$	
$R_5 = 2.0\ k\Omega$	$R_{12} = 9.0\ k\Omega$	
$R_6, R_{10} = 1.8\ k\Omega$		

TABLE I

ELECTRICAL CHARACTERISTICS — 9941 AND 9951 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

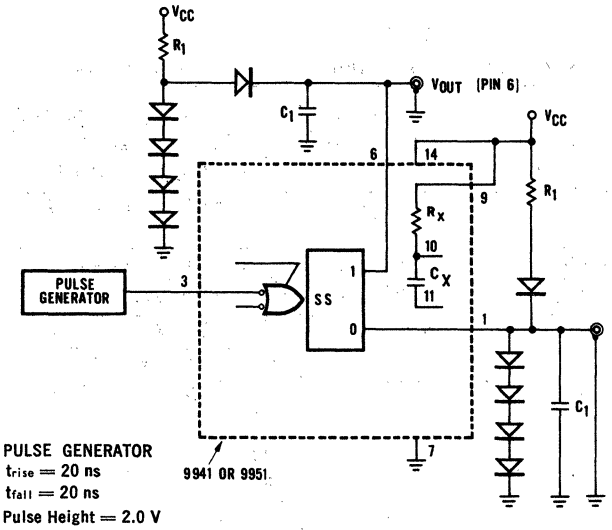
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.5			2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 15\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 15\ mA$
I_{PDL}	Power Dissipation Current with Inputs Grounded				7.2	9.0			mA	$V_{CC} = 5.0\ V$, Inputs = Gnd.
I_F	Input Load Current		−2.93			−2.93		−2.75	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−2.26			−2.26		−2.22	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current		5.0			5.0		10.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$, Pin 2 = Gnd.
t_{pd+}	Turn Off Delay					40			ns	Pin 6 — $V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay					40			ns	Pin 1 — See Figs. 4 & 5 on Page 23
PW	Pulse Width									
	9941			90		330				Pin 1
				70		330				Pin 6
	9951			90		220				Pin 1
				70		160				Pin 6

RULES FOR USE OF 9951

1. With Pin 9 connected to V_{CC} and no external capacitor (C_X), the output pulse width is approximately 100 ns.
2. With Pin 9 connected to V_{CC} and an external capacitor (C_X) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_X + 20)$ with C_X in pF and T in ns.
3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_X) of 9.0 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \approx 0.5\ R_X\ (C_X + 20)$ with R_X in kΩ, C_X in pF and T in ns.
4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2.0 kΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5. The maximum input fall time to trigger: 25 ns for a 1.0 volt swing; 50 ns for a 2.0 volt swing; 100 ns for a 4.0 volt swing.
6. The minimum pulse width at output Pin 1 is approximately 100 ns. This pulse width may be decreased to 50 ns by connecting a 10 kΩ resistor between Pin 5 and V_{CC}. (not applicable to TO-100 package.)
7. For pulse widths greater than 1.0 μs, Pin 1 should be used as the output and inverted if required.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

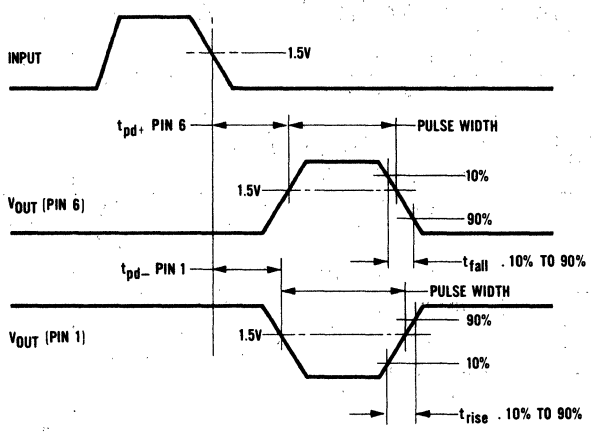
Fig. 4



PULSE GENERATOR
t_{rise} = 20 ns
t_{fall} = 20 ns
Pulse Height = 2.0 V
Pulse Width = 200 ns
Frequency = 1.0 MHz
Capacitance includes probe and jig
All Diodes FD100

C_l = 50 pF
R_l = 330Ω

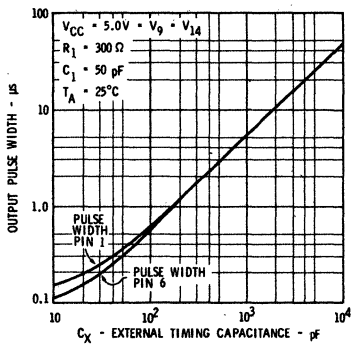
Fig. 5



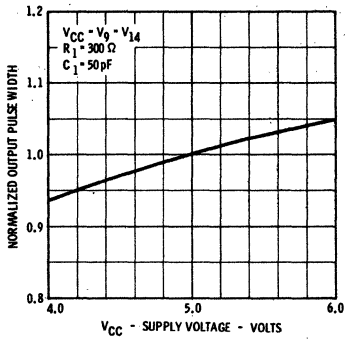
9941 AND 9951 TIMING CHARACTERISTICS

(Test circuit above is used with appropriate modifications where necessary)

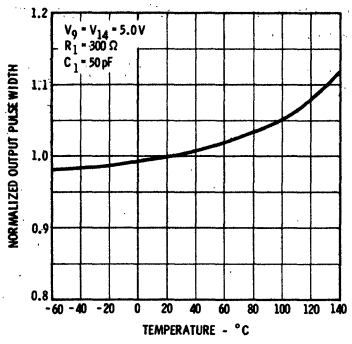
OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



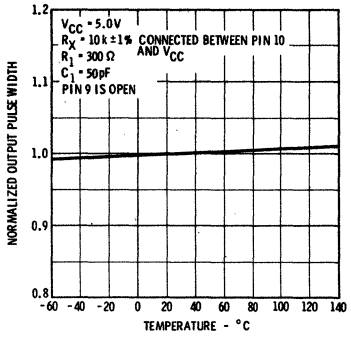
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



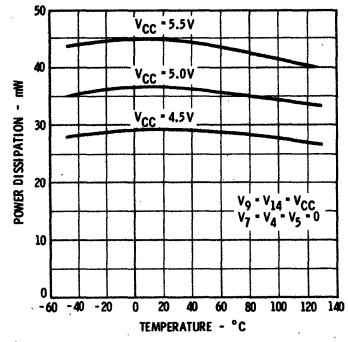
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE



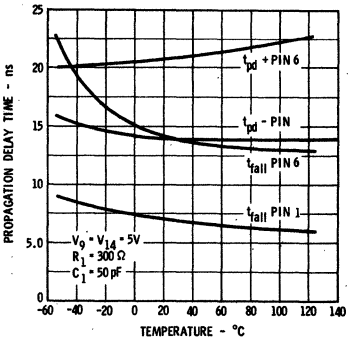
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE USING EXTERNAL TIMING RESISTOR R_X



TYPICAL POWER DISSIPATION VERSUS TEMPERATURE

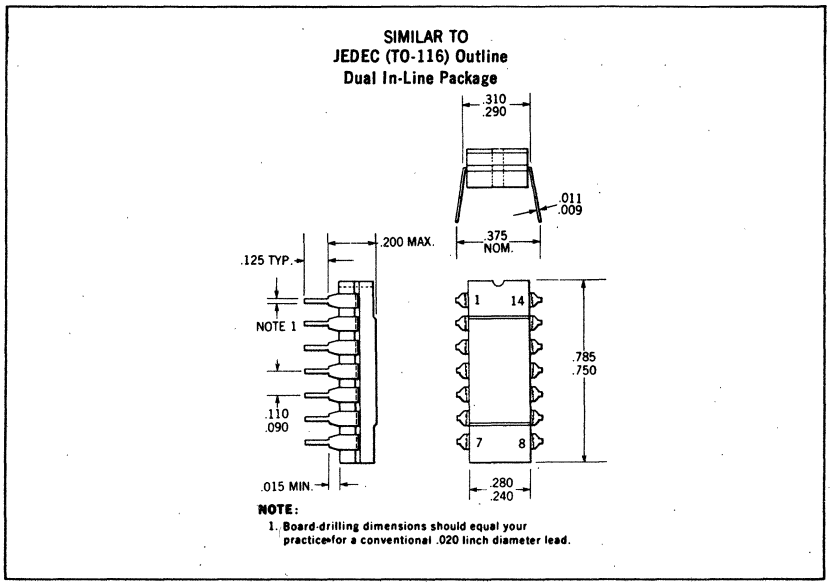


SWITCHING TIMES VERSUS TEMPERATURE

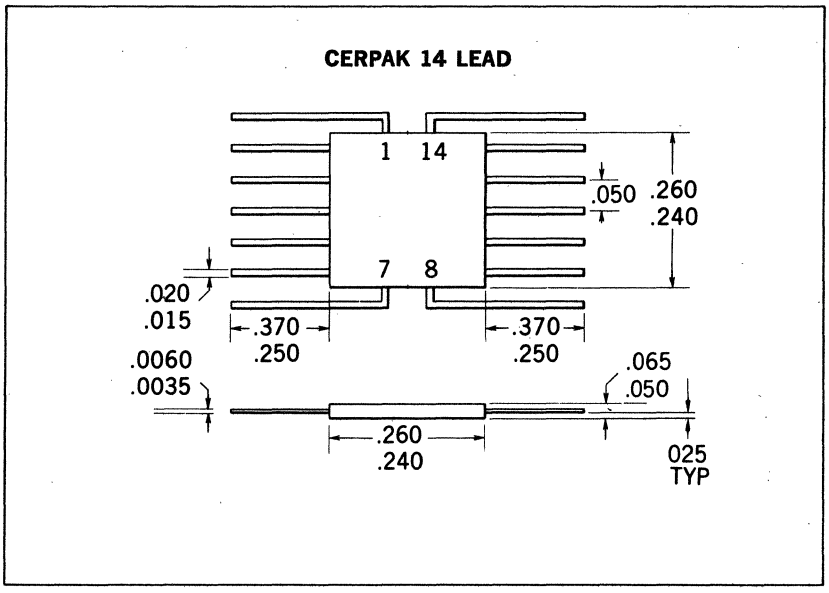


PACKAGE OUTLINES

U6A



U3I



ORDER INFORMATION

To order diode-transistor micrologic elements specify U3IXXXX51X for 14 pin Flat package; U6AXXXX51X for 14 pin Dual In-Line package where XXXX is the four-digit number denoting the specific element desired and 51X is for −55°C to + 125°C.

HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS COMPOSITE DATA SHEET

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

0°C TO 75°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The Fairchild High Level Logic Diode-Transistor Micrologic® Integrated Circuit family (HLLDTμL) consists of three high voltage, high threshold hex inverters which offer extremely good D.C. and A.C. Noise Immunity. These circuits are useful in applications involving a high noise environment or high voltage supply which prohibits the use of CCSL.

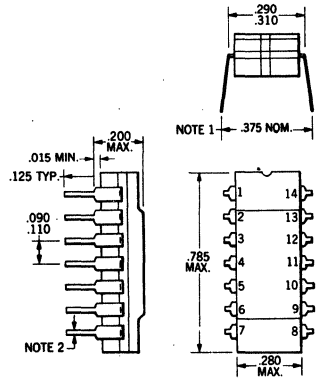
Interfacing from CCSL to HLLDTμL is accomplished with the 9112, shifting from HLLDTμL to CCSL is accomplished with the 9109. The 9112 can also be used to drive the μM3700 MOS Multiplexer.

The circuits are fabricated within a silicon monolithic substrate using standard Fairchild Planar* and Epitaxial processes.

HLLDTμL elements are available in the hermetically sealed ceramic Dual In-Line Package (DIP), designed for automated and low cost insertion techniques.

TYPICAL DUAL IN-LINE PACKAGE

similar to
JEDEC (TO-116) Outline



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

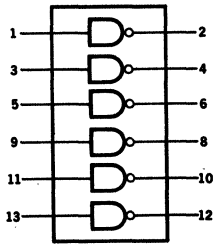
FEATURES

- **High Voltage Operation . . . V_{CC} Range 12 to 20 V.**
- **Utilizes inexpensive external input diodes to facilitate a high density building block approach and very high Logic Fan-In where desired.**
- **High D.C. Noise Immunity . . . 6.5 V minimum**
- **High A.C. Noise Immunity . . . 10 V at 150 ns**
- **Interfaces with CCSL**

ABSOLUTE MAXIMUM RATINGS (above which the reliability of the device may be impaired)

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +75°C
V_{CC} Pin Potential to Gnd Pin	−0.5 V to +25 V
Output Current when output is low	40 mA
Input Current (9109, 9110)	10 mA
Output Voltage	25 V
Input Voltage (9112)	5.5 V

LOGIC DIAGRAM



VCC = Pin 14
GND = Pin 7

ORDERING INFORMATION

To order HLLDTμL elements specify U6AXXXX59X, where XXXX is the four-digit number denoting the specific element desired.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

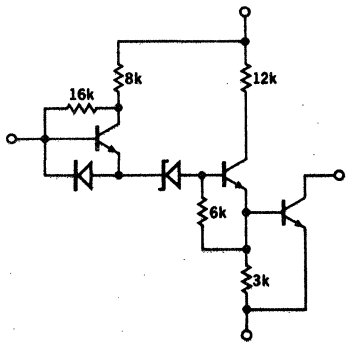
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	DEVICE	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	9110 9112	Note 2		Note 2			Note 2		Volts	V_{CC} = 12 V to 20 V I_{OH} = −0.1 mA @ V_{IL}
I_{CEX}	Output Leakage Current	9109		75		1.0	75		75	μA	V_{CC} = 20 V V_{OH} = 20 V @ V_{IL}
V_{OL1}	Output Low Voltage	9109 9110 9112		0.5		0.25	0.5		0.5	Volts	V_{CC} = 12 V I_{OL} = 10 mA @ V_{IH}
V_{OL2}	Output Low Voltage	9109 9110 9112		1.0		0.5	1.0		1.0	Volts	V_{CC} = 20 V I_{OL} = 20 mA @ V_{IH}
V_{IL}	Input Low Voltage	9109 9110		7.05			7.0		6.8	Volts	Input Low Threshold @ V_{OH}
		9112		1.05			1.0		0.8		
V_{IH}	Input High Voltage	9109 9110	8.6		8.5			8.4		Volts	Input High Threshold @ V_{OL}
		9112	2.1		2.0			1.9			
I_F	Input Load Current	9109 9110 9112		−1.20		−0.80	−1.12		−1.12	mA	V_{CC} = 20 V, V_F = 0.5 V
I_{SC}	Output Short Circuit Current	9110 9112		−17 −2.4		−9.0 −1.65	−16.3 −2.3		−15.6 −2.3	mA	V_{CC} = 20 V, V_{IN} = 0 V V_{OUT} = 0 V
I_{CEX}	Output Leakage Current	9110 9112		75		1.0	75		75	μA	V_{CC} = 20 V, V_{OUT} = 20 V V_{IN} = 0 V
I_{PDH}	Input High Supply Current	9109 9110				19	28			mA	V_{CC} = 20 V, Input Open
		9112				22	34				
I_R	Input Leakage Current	9112					5.0		10	μA	V_{CC} = 20 V, V_R = 4.0 V
I_{max}	Ground Current	9109 9110 9112					15			mA	V_{CC} = V_{OUT} = 25 V, Inputs @ GND
t_{pd+}	Turn Off Delay	9109 9110 9112				145	300			ns	See Fig. 4
t_{pd-}	Turn On Delay	9109 9110				95	200			ns	See Fig. 4
		9112				30	125				
V_{TN}	"0" Level A.C. Noise Immunity	9110				7.0				Volts	See Fig. 5
V_{TP}	"1" Level A.C. Noise Immunity	9110				8.5				Volts	See Fig. 5

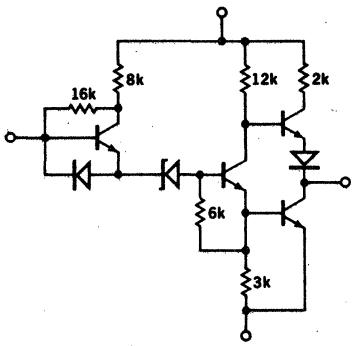
NOTES:
(1) Tests on 9109, 9110 are performed with FDH6 input diodes.
(2) MIN = Vcc −2.0 V for all temperature
TYP = Vcc −1.5 V for 25°C

Fig. 1a



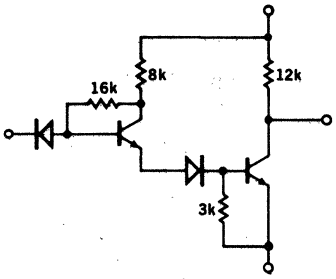
1/6 HLLDTL 9109
HLL → CCSL

Fig. 1b



1/6 HLLDTL 9110
HLL → HLL

Fig. 1c

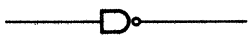


1/6 HLLDTL 9112
CCSL → HLL

Fig. 2a

1*
LOW LEVEL LOAD FACTOR
(see Fig. 3a)

WITH FDH6 INPUT DIODE FOR 9109,9110



9109: OPEN COLLECTOR
9110,9112: 20
LOW LEVEL DRIVE FACTOR
(see Fig. 2b)

Fig. 2b
OUTPUT LOADS
(LOW LEVEL DRIVE FACTOR)
VERSUS SUPPLY VOLTAGE

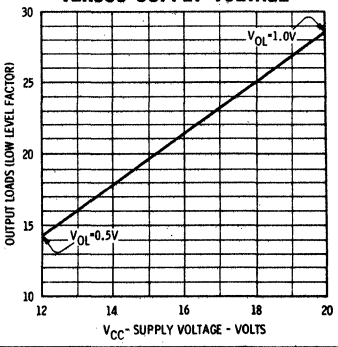


Fig. 3a
WORST CASE INPUT FORWARD
CURRENT AND INPUT LOADS
VERSUS SUPPLY VOLTAGE

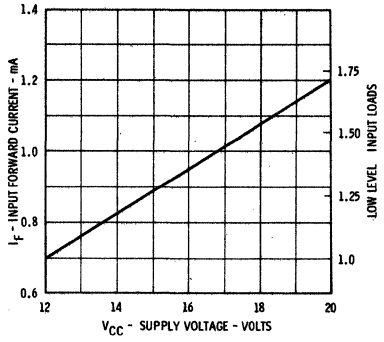


Fig. 3b
WORST CASE POWER DISSIPATION
VERSUS SUPPLY VOLTAGE
(PER GATE)

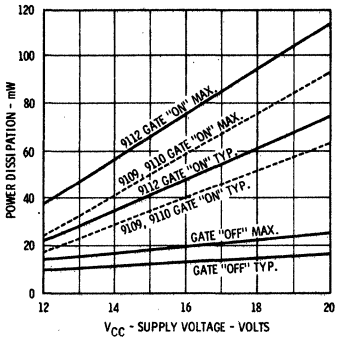


Fig. 3c
WORST CASE HIGH LEVEL
D.C. NOISE IMMUNITY
VERSUS TEMPERATURE

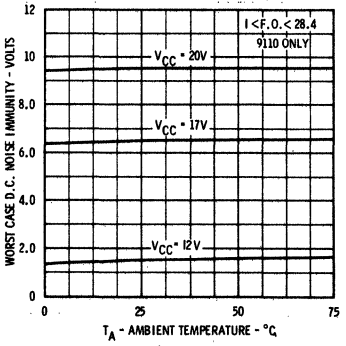


Fig. 3d
WORST CASE HIGH INPUT
THRESHOLD VOLTAGE VERSUS
FORWARD DIODE VOLTAGE

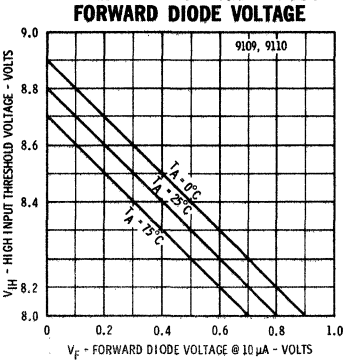


Fig. 3e
WORST CASE LOW THRESHOLD
VOLTAGE VERSUS
FORWARD DIODE VOLTAGE

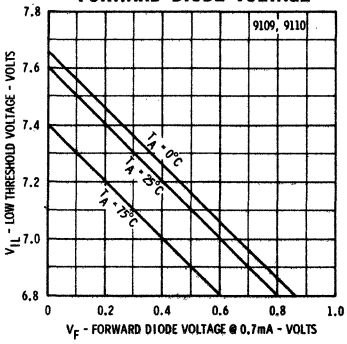


Fig. 3f
WORST CASE LOW LEVEL
D.C. NOISE IMMUNITY
VERSUS AMBIENT TEMPERATURE

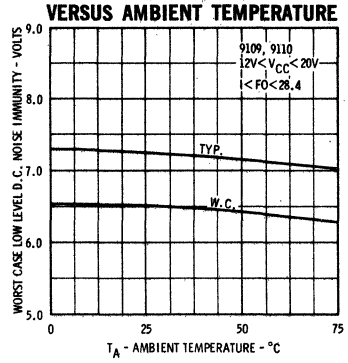


Fig. 3g
TURN OFF DELAY
VERSUS AMBIENT TEMPERATURE

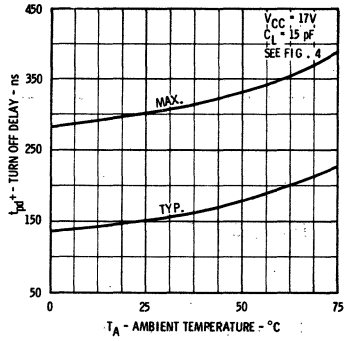


Fig. 3h
TURN ON DELAY
VERSUS AMBIENT TEMPERATURE

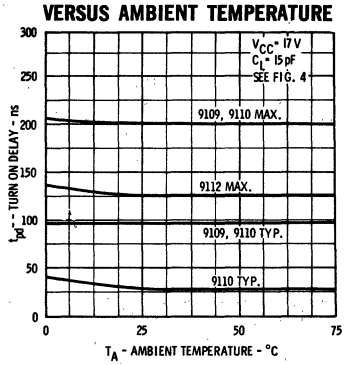


Fig. 3i
TYPICAL A.C. NOISE IMMUNITY
INPUT VOLTAGE VERSUS
PULSE WIDTH

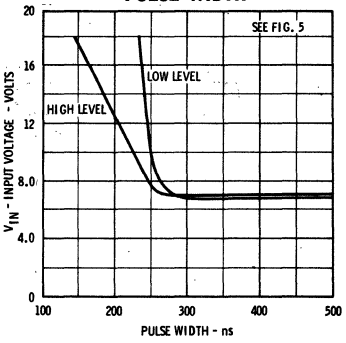
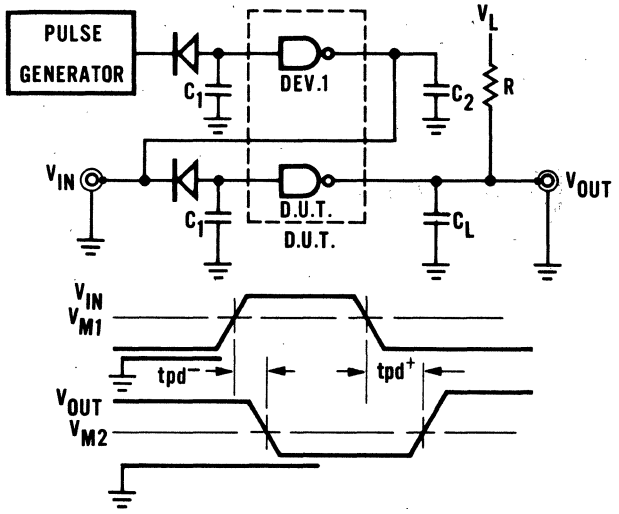


Fig. 4
SWITCHING TIME TEST CIRCUIT
AND WAVEFORMS



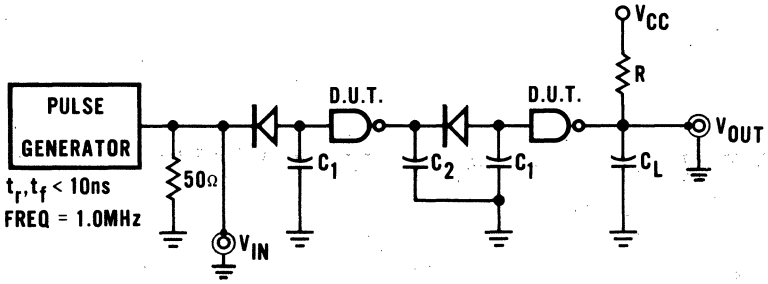
$C_1 = 5.0$ pF Includes all probe
$C_2 = 10$ pF and jig capacitance
$C_L = 15$ pF

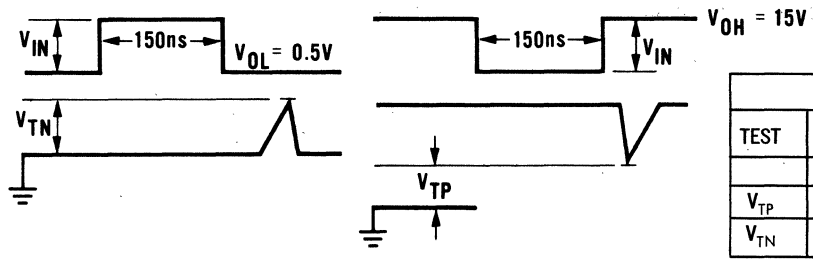
FDH6 Input Diodes are used on 9109, 9110

TEST CONDITIONS

D.U.T.	DEV. 1	V_{m1}(V)	V_{m2}(V)	V_L(V)	R_{tpd-}	R_{tpd+}
9109	9110	7.5	1.5	5.0	510 Ω	3.6 k
9110	9110	7.5	7.5	17.0	2.4 k	24 k
9112	932	1.5	7.5	17.0	2.4 k	24 k

Fig. 5
A.C. NOISE IMMUNITY TEST CIRCUIT



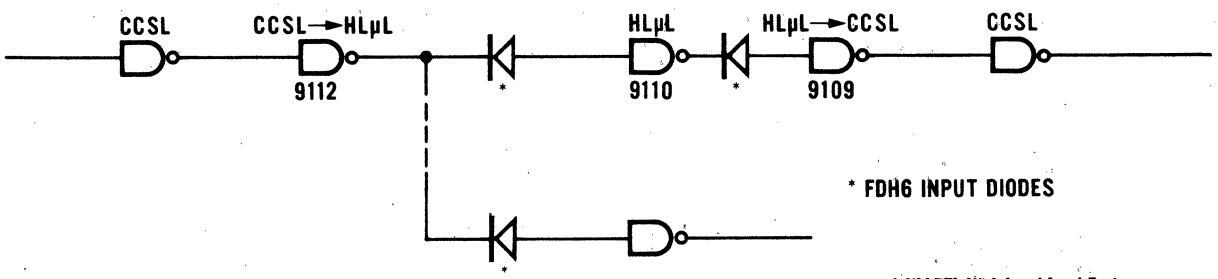


Unused inputs grounded
diodes are FDH6
$C_1 = 5.0$ pF Includes jig and
$C_2 = 10$ pF all probe capacitance
$C_L = 15$ pF

TEST CONDITIONS AND LIMITS						
TEST	LIMIT		V_{CC}	R	T_A	V_{IN}
	MIN.	MAX.	(Volts)	(kΩ)	(°C)	(Volts)
V_{TP}	8.5 V		17	24	25	10
V_{TN}		7.0 V	17	2.4	25	10

APPLICATIONS:

Fig. 6—CCSL INTERFACING



1 HLLDTL High Level Load Factor
= 1 CCSL High Level Load Factor
1 HLLDTL Low Level Load Factor
= 7.5 CCSL Low Level Load Factors

Fig. 7—LAMP DRIVER

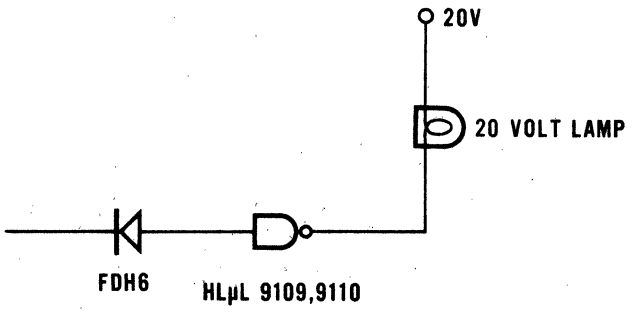
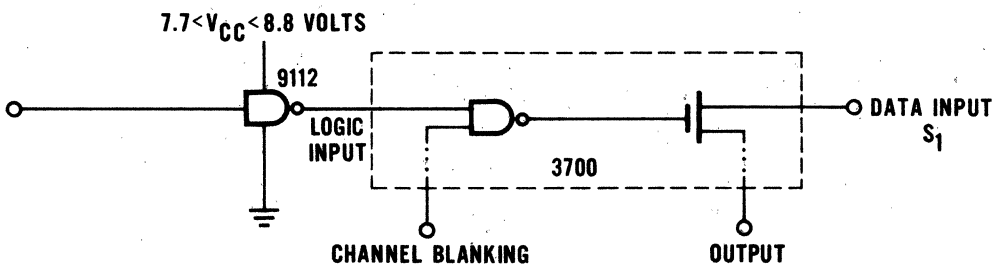
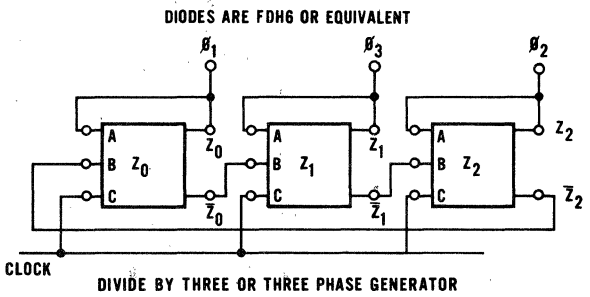


FIG. 8—DRIVING MOS3700 MULTIPLEXER OR EQUIVALENT



Output Levels : min "1" level = V_{CC} —1.5 V
: max "0" level = 0.2 V

Fig. 9—SEQUENTIAL COUNTER



ϕ_1	ϕ_3	ϕ_2	Clock
1	0	0	0
1	0	1	1
0	0	1	0
0	1	1	1
0	1	0	0
1	1	0	1

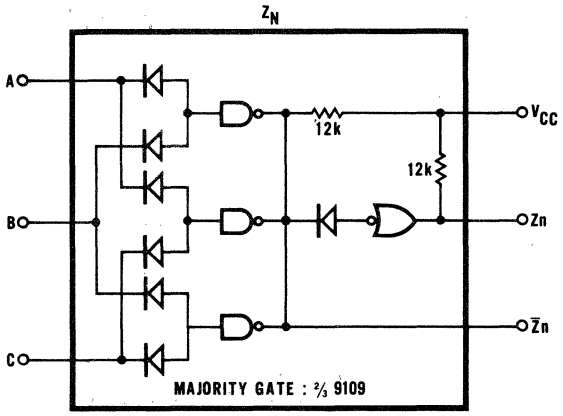
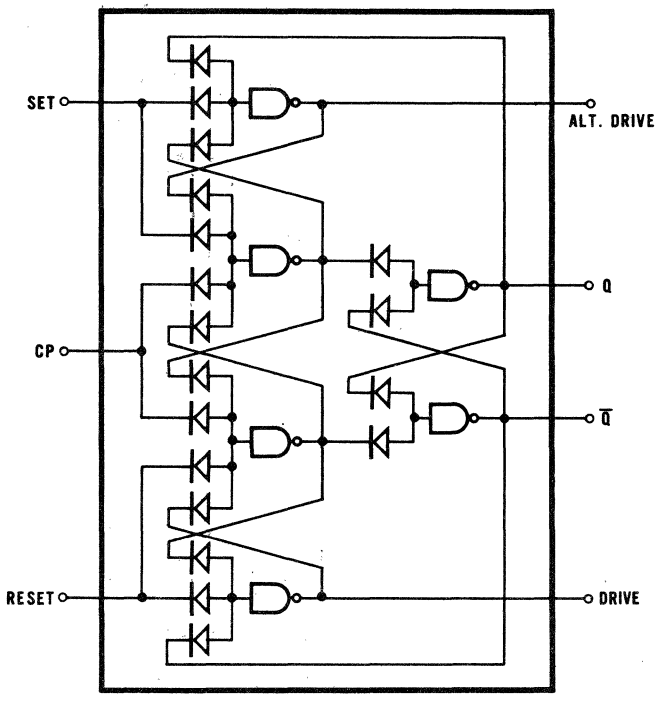
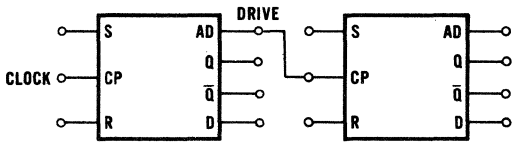
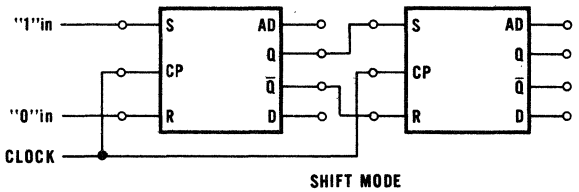


Fig. 10—JK FLIP FLOP





TOGGLE MODE



SHIFT MODE

DIODES ARE FDH6 OR EQUIVALENT

J	K	Qn+1
L	H	L
L	L	Qn
H	H	$\overline{Q}$n
H	L	H

HLLDTμL 9109

HIGH VOLTAGE HEX INVERTER

HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The HLLDTμL9109 is a high voltage, high threshold hex inverter designed for the conversion of high level logic to any logic level from 4V to 20V. The unit is characterized by a 6.5V(min.) DC Noise Immunity and a 20V/100 nsec AC Noise Immunity. The input diode has been left off the circuit so that the input can be expanded to any number of inputs which allows maximum flexibility in use.

The 9109 is available in ceramic Dual In-Line* Package.

FEATURES

CCSL Compatibility

High Voltage Operation 12 to 20 V

Utilizes external input diodes to facilitate high density building block approach

F.O. = 7 CCSL

D.C. Noise Immunity of 6.5V

APPLICATIONS

Interfacing from HLL to CCSL levels.

Line receiver.

General purpose logic level converter

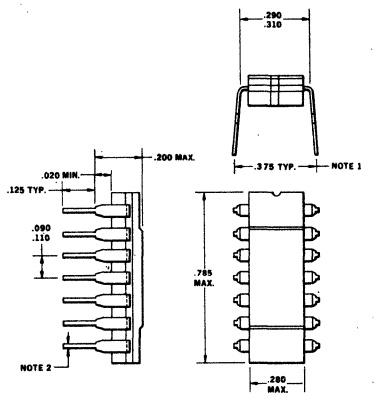
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
Operating temperature	0°C to 75°C
V_{CC}	25 V
Output Voltage	25 V
Output low current	40 mA

*Fairchild patent pending

TYPICAL DUAL IN-LINE PACKAGE

(In accordance with JEDEC TO-116)



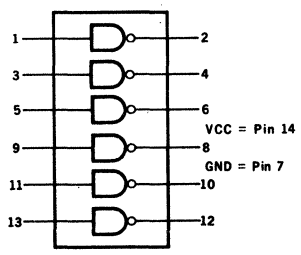
NOTES:

1 Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

2 Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

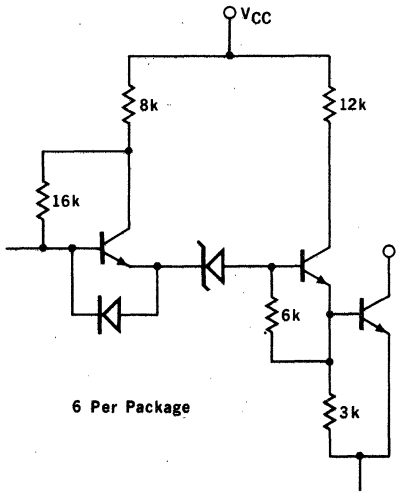
ORDER PART NO. U6A910959X

LOGIC DIAGRAM



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

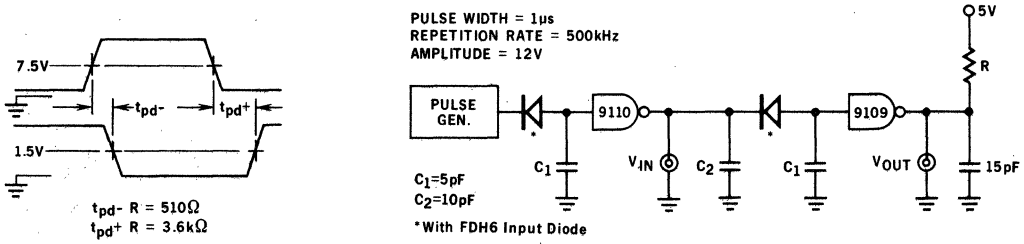


CIRCUIT DIAGRAM

ELECTRICAL CHARACTERISTICS

SYMBOL	LIMITS						UNITS	CONDITIONS AND COMMENTS
	0°C		25°C			75°C		
	MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
I_{OH}		75		0.2	75	75	μA	V_{CC} = 20 V, V_{OH} = 20 V
V_{IL}					7.0	6.8	Volts	
V_{OL1}		0.5		0.25	0.5	0.5	Volts	V_{CC} = 12 V, I_{OL} = 10 mA V_{IH} = Value indicated on this table.
V_{OL2}		1.0		0.5	1.0	1.0		V_{CC} = 20 V, I_{OL} = 20 mA
V_{IH}	8.6		8.5				Volts	
I_F		-1.24		-.81	-1.16		mA	V_{CC} = 20 V, V_F = 0.5 V
I_{PDH}		30		19	28		mA	V_{CC} = 20 V, Inputs open
I_{PDL}		9.5		6.0	9.0		mA	V_{CC} = 25 V, Inputs GnD V_{OUT} = 25 V
t_{pd}^+				145	400		ns	See switching time test circuit
t_{pd}^-				85	200		ns	

NOTE: Tests are performed with FDH6 input diode.



CIRCUIT AND WAVEFORMS FOR SWITCHING TESTS

HLLDTμL 9110

HIGH VOLTAGE HEX INVERTER

HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The HLLDTμL 9110 is a high voltage, high threshold hex inverter with extremely good D.C. and A.C. Noise Immunity. The circuit is useful in applications involving a high noise environment or high voltage supplies which prohibit the use of DTμL.

The 9110 contains six basic logic building blocks from which more complex functions (Flip-Flop, Shift Registers, etc.) can easily be built.
The 9110 is available in the hermetically sealed cermic Dual-In-Line Package (DIP), designed for automated and low cost insertion techniques.

FEATURES

- High Voltage Operation V_{CC} Range 12 to 20 V.
- Utilizes inexpensive external input diodes to facilitate a high density building block approach and a very high logic Fan-In where desired.
- High D.C. Noise Immunity 6.5 V minimum
- High A.C. Noise Immunity 10 V at 150 ns.

APPLICATIONS

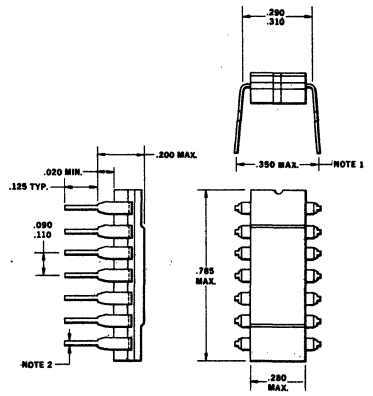
Industrial Control Logic, Automotive Logic, Lamp Driver, Relay Driver

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 75°C
V_{CC}	25 V
Output Voltage	25 V
Output low current	40 mA

TYPICAL DUAL IN-LINE PACKAGE

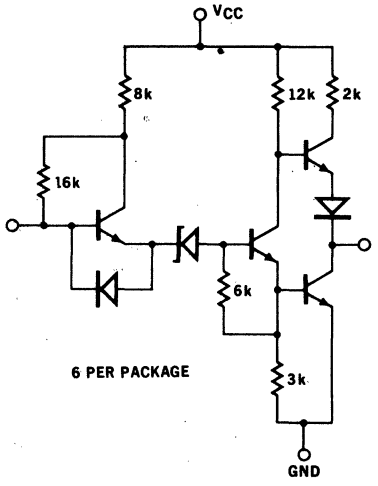
In Accordance With
JEDEC (TO-116) Outline



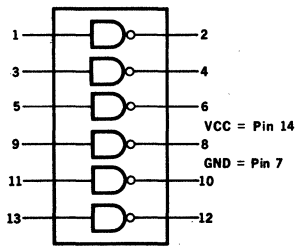
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

ORDER PART NO. U6A911059X

CIRCUIT DIAGRAM



LOGIC DIAGRAM



* Fairchild patent pending

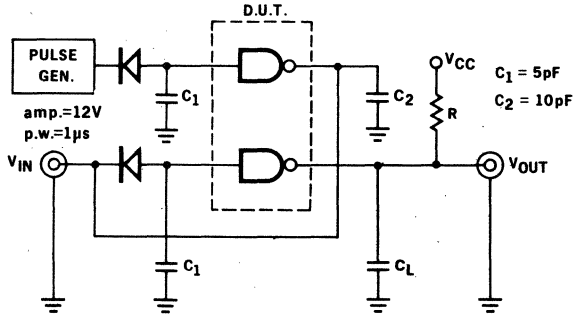
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

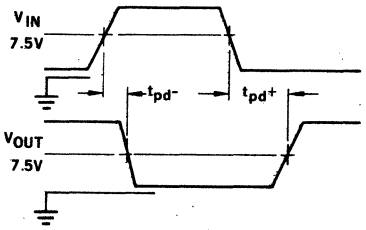
ELECTRICAL CHARACTERISTICS

SYMBOL	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}			$V_{OH\ (min.)} = (V_{CC} - 2.0\,V)$ $V_{OH(typ.)} = (V_{CC} - 1.5\,V)$					Volts	V_{CC} = 12 to 20 V I_{OH} = -0.1 mA @ V_{IL}
V_{IL}					7.0		6.8	Volts	V_{CC} = 12 to 20 V
V_{OL1}		0.5		0.25	0.5		0.5	Volts	V_{CC} = 12 V I_{OL} = 10 mA @ V_{IH}
V_{OL2}		1.0		0.5	1.0		1.0	Volts	V_{CC} = 20 V I_{OL} = 20 mA @ V_{IH}
V_{IH}	8.6		8.5					Volts	V_{CC} = 12 to 20 V
I_F		-1.24		-0.81	-1.16		-1.16	mA	V_{CC} = 20 V V_F = 0.5 V
I_{SC}		17.0		9.0	16.3		15.6	mA	V_{CC} = 20 V V_{out} = 0 V
I_{PDH}		30		19	28		28	mA	V_{CC} = 20 V Inputs open.
I_{PDL}		9.5		6.0	9.0		9.0	mA	V_{CC} = 25 V Inputs GND Outputs = 25 V
t_{pd+}				145	400			ns	See switching
t_{pd-}				100	200			ns	test circuit.

SWITCHING TIME TEST CIRCUIT

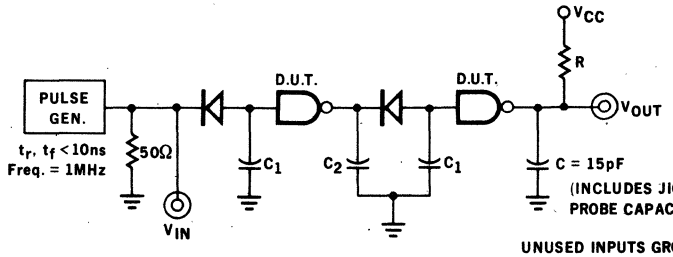


C_L = 15pF
t_{pd^-} : R = 2.4k
t_{pd^+} : R = 24k
*INCLUDES JIG CAPACITANCE
DIODES ARE FDH6
GND UNUSED INPUTS



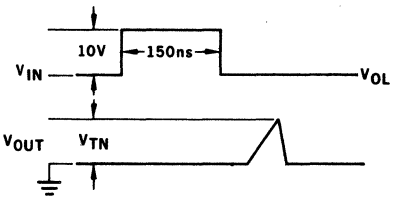
NOTE: TESTS ARE PERFORMED WITH FDH6 INPUT DIODE

A.C. NOISE IMMUNITY TEST CIRCUIT

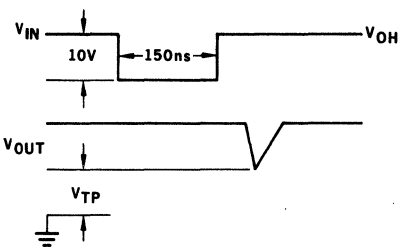


UNUSED INPUTS GROUNDED
DIODES ARE FDH6
C_1 = 5pF
C_2 = 10pF

LOW LEVEL AC NOISE IMMUNITY



HIGH LEVEL AC NOISE IMMUNITY



TEST CONDITIONS AND LIMITS					
TEST	LIMIT MIN.	LIMIT MAX.	V_{CC} (Volts)	R kΩ	T_A °C
V_{TP}	8.5 V		17	24k	25
V_{TN}		7.0 V	17	2.4	25

HLLDTμL 9112

HIGH VOLTAGE HEX INVERTER

HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

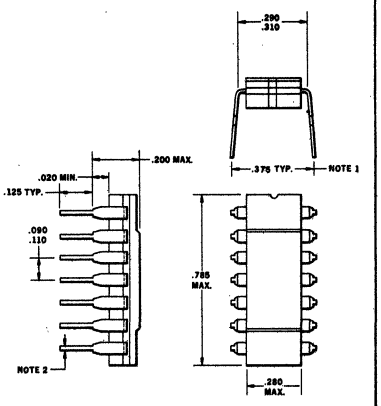
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The HLLDTμL9112 is a CCSL to high level hex interface element, The 9112 consists of six gates suitable for converting from CCSL levels up to high logic levels (10V to 18V.) The 9112 is ideal for driving MOS devices such as the μM3700 element (6 Channel Multiplexer.)

The 9112 is available in ceramic Dual In-Line* Package.

TYPICAL DUAL IN-LINE PACKAGE
(In accordance with JEDEC TO–116)



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

ORDER PART NO. U6A911259X

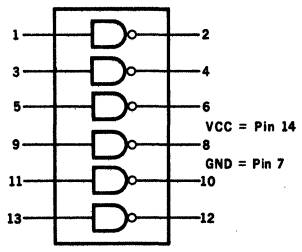
FEATURES

- CCSL Compatibility
- High Voltage Operation — V_{CC} Range 12 to 20 V
- F.O. = 10 HL
- Wired-OR Capability
- Good AC Noise Immunity

APPLICATIONS

- CCSL→HL interface element
- MOS driver

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Storage temperature	-65°C to 150°C
Operating temperature	0°C to 75°C
V_{CC}	25 V
Output Voltage	25 V
Output low current	40 mA

*Fairchild patent pending

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FAIRCHILD SEMICONDUCTOR
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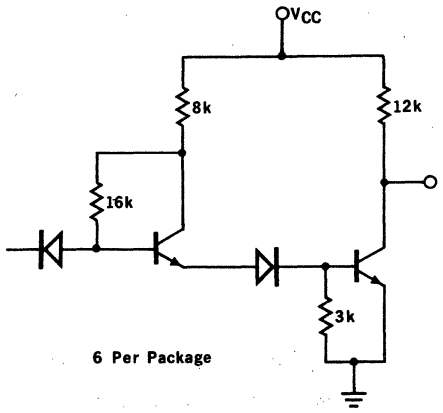
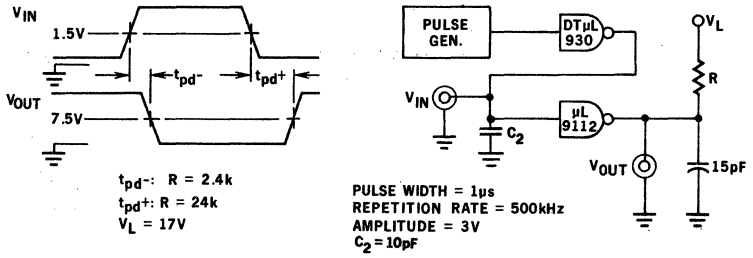


CIRCUIT DIAGRAM

ELECTRICAL CHARACTERISTICS

SYMBOL	LIMITS						UNITS	CONDITIONS AND COMMENTS
	0°C		25°C			75°C		
	MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH} (Output High)			18	18.5			Volts	V_{CC} = 20 V, I_{OH} = 0.1 mA V_{IL} = Value indicated in this table.
V_{IL}					1.0	0.8	Volts	
I_{CEX} (Output Leakage)		75		0.2	75	75	μA	V_{CC} = 20 V, V_{OH} = 20. V V_{IN} = OV
V_{OL1} (Output Low)		0.5		0.25	0.5	0.5	Volts	V_{CC} = 12 V, I_{OL} = 10 mA V_{IH} = Value indicated in this table.
V_{IH}	2.1		2.0			0.8	Volts	
V_{OL2}		1.0		0.5	1.0	1.0	Volts	V_{CC} = 20 V, I_{OL} = 20 mA
I_F (Input Low)		-1.20		-0.8	-1.12	-1.12	mA	V_{CC} = 20 V, V_F = 0.45 V
I_{SC} (Output Shorted)		-2.4		-1.65	-2.3	-2.3	mA	V_{CC} = 20 V, V_{IN} = 0 V V_{OUT} = 0 V
I_{PDH} (Power Diss.)		36		22	34	34	mA	V_{CC} = 20 V, Input open
I_{PDL} (Power Diss.)		9.5		6.0	9.0	9.0	mA	V_{CC} = 25 V, Input GND V_{OUT} = 25 V
t_{pd}^+ (Turn Off)				145	400		ns	See switching time test circuit
t_{pd}^- (Turn On)				25	200		ns	



CIRCUIT AND WAVEFORMS FOR SWITCHING TESTS

LPDTμL 9040, 9041 AND 9042

LOW POWER DIODE TRANSISTOR MICROLOGIC®
INTEGRATED CIRCUITS

GENERAL DESCRIPTION

The Fairchild LPDTμL Micrologic® Integrated Circuit Family consists of a set of compatible, integrated logic circuits specifically designed for low power, medium speed applications.

The circuits are fabricated with a silicon monolithic substrate using standard Fairchild Planar* epitaxial processes.

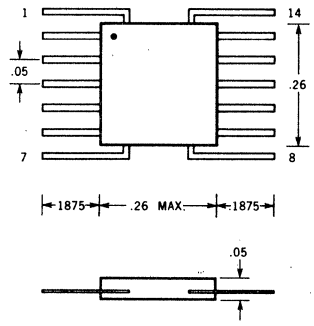
Packaging options include the Flat package and the Dual In-Line package.

Important features of the LPDTμL Micrologic® integrated circuits include the following:

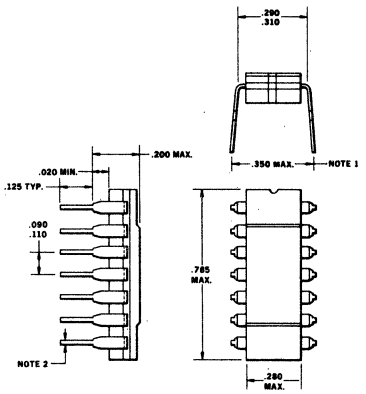
- Reliable operation over the full military temperature range of -55°C to +125°C
- Typical power drains of less than 1 mW per gate (50% duty cycle) for the logic gate elements and less than 4 mW for the clocked flip-flop.
- Single power supply requirement—5 volts optimum, 4.5 to 5.5 volts range.
- Guaranteed fan-out of 10 LPDTμL unit loads or 1 standard Fairchild DTμL unit load, over the full temperature and supply voltage range.
- Guaranteed minimum of 450 mV noise immunity at the temperature extremes.
- Typical logic gate propagation delays of 60 ns and binary clock rate of 2.5 MHz.
- Emitter follower outputs providing good capacitive drive capability.

TYPICAL FLAT PACKAGE

TOP VIEW



TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

*Planar is a patented Fairchild process.

ORDER INFORMATION

To order Low Power Diode Transistor Micrologic® integrated circuit elements specify U31XXXX51X for flat package and U6AXXXX51X for Dual In-Line package where XXXX is 9040, 9041 or 9042.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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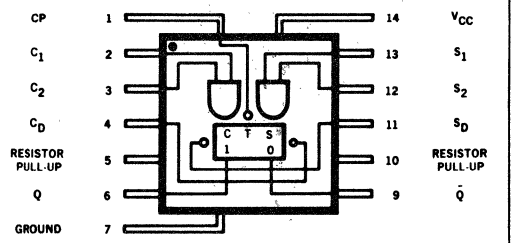
LPDTμL 9040 CLOCKED FLIP-FLOP

DESCRIPTION

The LPDTμL 9040 element is a directly coupled, dual-rank flip-flop suitable for use in counters, shift registers and other storage applications. Either R-S or J-K mode operation is possible. Direct set and clear inputs are provided which override all other data inputs.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN LINE PACKAGE PIN ASSIGNMENT



SYNCHRONOUS ENTRY TRUTH TABLES

R-S MODE OPERATION

INPUTS @t_n				OUTPUTS @t_{n+1}	
S_1	S_2	C_1	C_2	Q	$\overline{Q}$
13	12	2	3	6	9
L	X	L	X	NC	NC
L	X	X	L	NC	NC
X	L	L	X	NC	NC
X	L	X	L	NC	NC
L	X	H	H	L	H
X	L	H	H	L	H
H	H	L	X	H	L
H	H	X	L	H	L
H	H	H	H	AMBIGUOUS	

J-K MODE OPERATION

INPUTS @t_n		OUTPUTS @t_{n+1}	
S_1	C_1	Q	$\overline{Q}$
13	2	6	9
L	L	NC	NC
L	H	L	H
H	L	H	L
H	H	TOGGLES	

ASYCHRONOUS ENTRY TRUTH TABLE

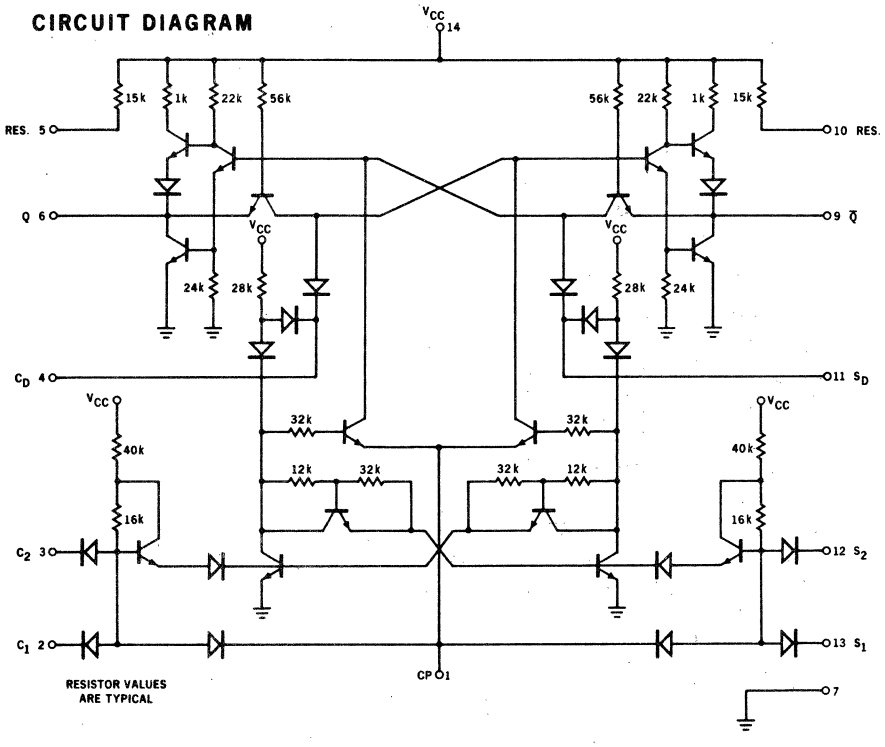
INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
11	4	6	9
H	H	NC	NC
H	L	L	H
L	H	H	L
L	L	H	H

Symbols

H - Most positive logic level
L - Most negative logic level
X - Either H or L can be present
NC - No change in state

NOTES:
1. For J-K mode operation connect Pin 6 to Pin 3 and Pin 9 to Pin 12.
2. Asynchronous entries override all synchronous entries.

CIRCUIT DIAGRAM



LOADING RULES

INPUT	*NORMALIZED UNIT LOADS (U.L.)
$\frac{S_1\ S_2}{C_1\ C_2}$	0.75 U.L.
$S_D\ C_D$	2.5 U.L.
CP	2.5 U.L.
OUTPUT	**FAN-OUT**
Q, $\overline{Q}$	10 U.L. 7 U.L. WITH RESISTOR PULL-UP CONNECTED

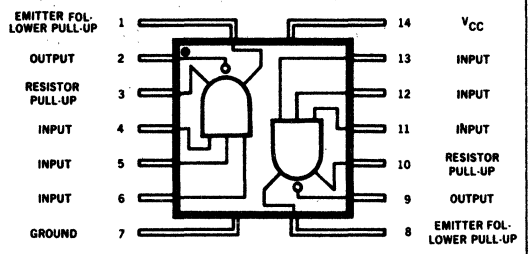
*1 UNIT LOAD EQUALS 1-LPDTμL 9041 OR 9042 INPUT LOAD

LPDTμL 9041 — DUAL 3 INPUT NAND GATE

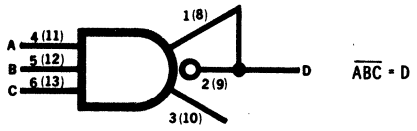
DESCRIPTION

The LPDTμL 9041 element consists of two, 3-input positive logic NAND gates suitable for general logic gate and inverter applications. The unique feature of this gate is that the output transistor collector and the emitter follower pull-up are not internally connected. This allows the user to tie collectors to a common node for the wired "OR" logic function.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN-LINE PACKAGE PIN ASSIGNMENT



POSITIVE LOGIC NAND GATE

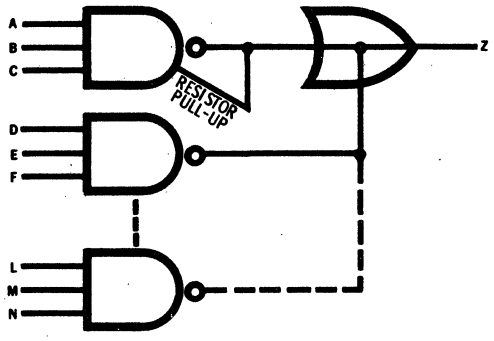


$\overline{ABC} = D$

EACH INPUT = 1 UNIT LOAD
OUTPUT FAN-OUT = 10 UNIT LOADS
= 7 U.L. WITH RESISTOR PULL-UP CONNECTED

EITHER THE EMITTER FOLLOWER OR RESISTOR PULL-UP MUST BE CONNECTED TO THE OUTPUT TO ESTABLISH THE HIGH LEVEL.

WIRED 'OR' APPLICATION

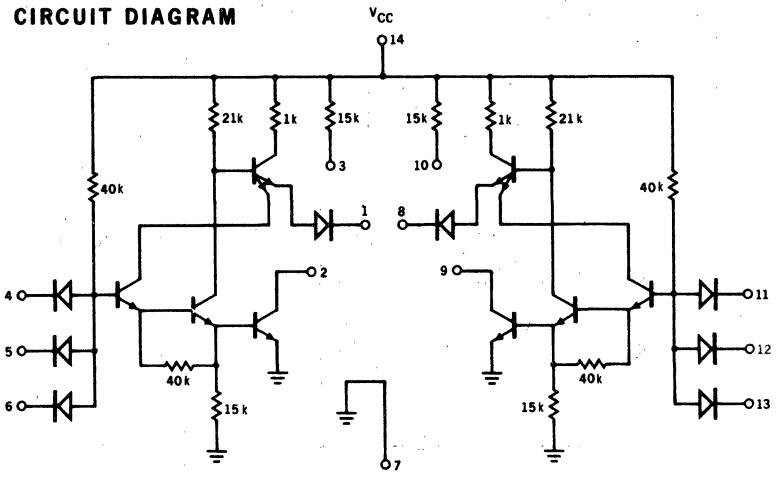


$\overline{ABC + DEF + \cdots + LMN} = Z$

OUTPUT FAN-OUT = 10 - 3 (NO. OF RESISTOR PULL-UPS)

ONE PULL-UP RESISTOR IS REQUIRED FOR EVERY 8 GATES CONNECTED TO THE COMMON "OR" NODE.

CIRCUIT DIAGRAM



RESISTOR VALUES ARE TYPICAL

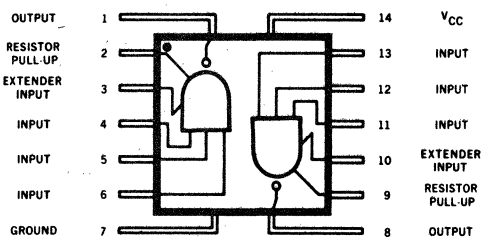
LPDTμL 9042 — DUAL 3 INPUT NAND GATE WITH EXTENDER INPUTS

DESCRIPTION

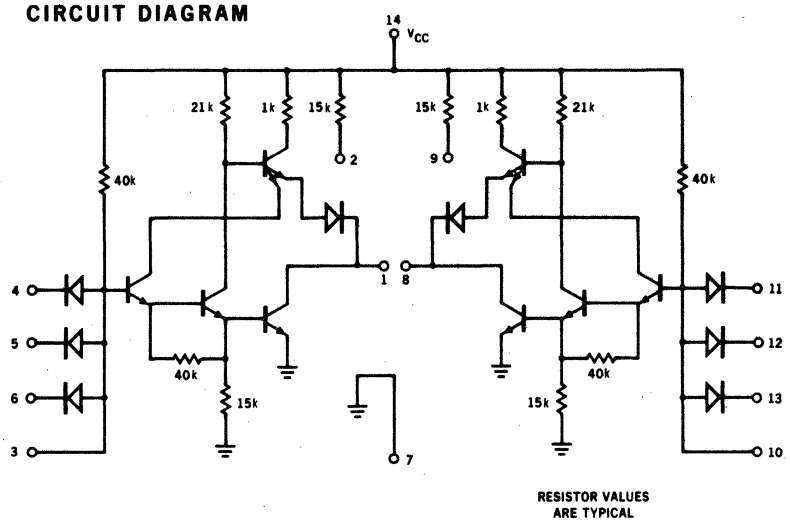
The LPDTμL 9042 element consists of two 3-input positive logic NAND gates with extender inputs. This element in the family allows the user to implement logic applications requiring a gate fan-in exceeding three.

The DTμL 9933 4-input extender element or equivalent—may be used to provide additional diode inputs. Any capacitance added to the extender input will increase the turn-on delay of the LPDTμL 9042 gate. Typically, the increase is 10 ns/pico-farad. Turn-off delay is not affected.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN-LINE PACKAGE PIN ASSIGNMENT

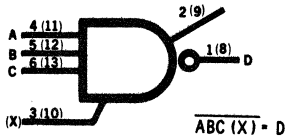


CIRCUIT DIAGRAM



RESISTOR VALUES ARE TYPICAL

POSITIVE LOGIC NAND GATE



$\overline{ABC}$ (X) = D

EACH INPUT = 1 UNIT LOAD

OUTPUT FAN-OUT = 10 UNIT LOADS

= 7 UNIT LOADS WITH RESISTOR PULL-UP CONNECTED

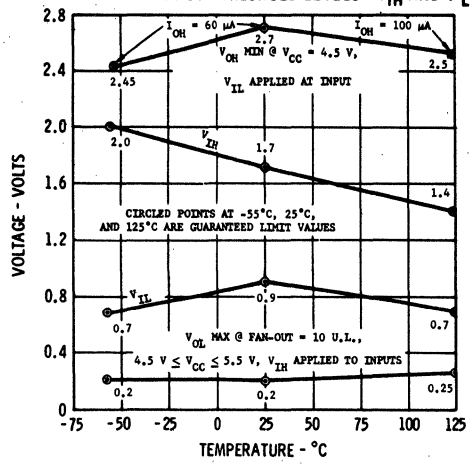
BUFFER ELEMENT

For applications requiring a fan-out exceeding ten, the Fairchild DTμL 9930 Dual 4-Input Gate may be used. The DTμL 9930 will drive 44 LPDTμL unit loads, while maintaining the same output logic levels as the low power circuits.

The input of a DTμL 9930 requires the equivalent of 10 LPDTμL unit loads. Therefore, a low power circuit can drive only one DTμL 9930 input.

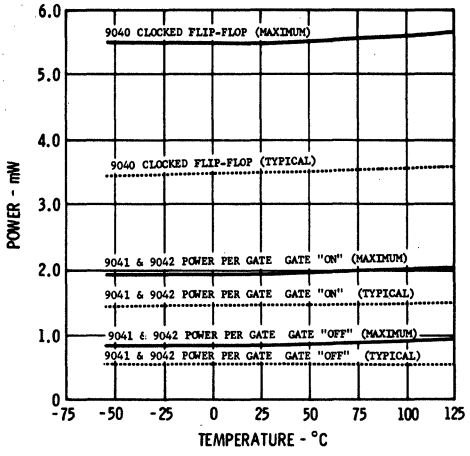
OPERATING VOLTAGE CHARACTERISTICS

WORST CASE OUTPUT LOGIC LEVELS - V_{OH} AND V_{OL}
INPUT THRESHOLD LEVELS - V_{IH} AND V_{IL}

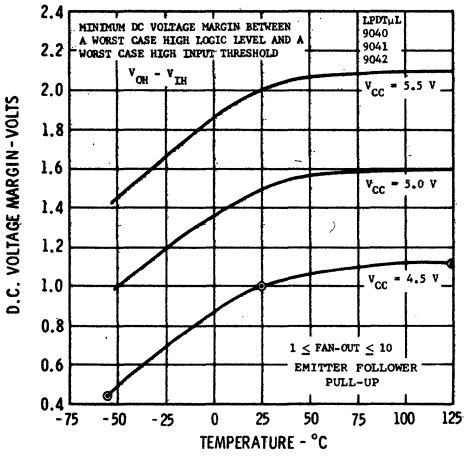


POWER CHARACTERISTICS

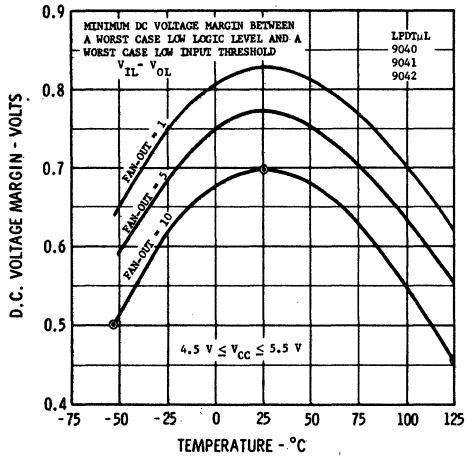
VCC = 5V
EMITTER FOLLOWER PULL-UP



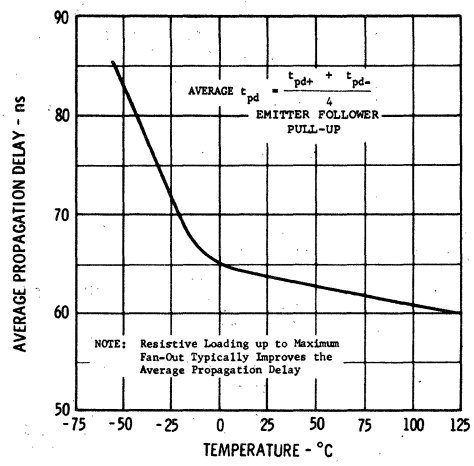
HIGH LEVEL NOISE IMMUNITY



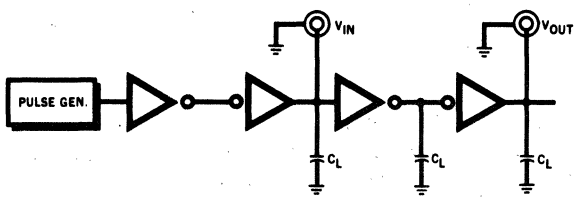
LOW LEVEL NOISE IMMUNITY



TYPICAL AVERAGE PROPAGATION DELAY LPDTμL 9041•9042



TEST CIRCUIT

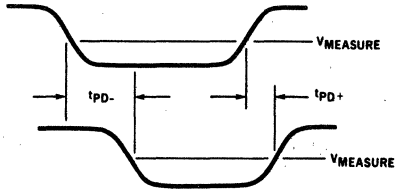


CONDITIONS

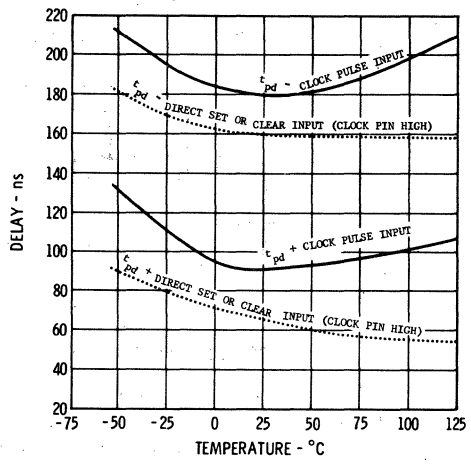
V_{CC} = 5.0V, C_L = 50pf (INCLUDING PROBE AND JIG CAPACITANCE)

$V_{MEASURE}$ = 1.6V @ -55°C
(GND. REF.) 1.3V @ 25°C
0.9V @ 125°C

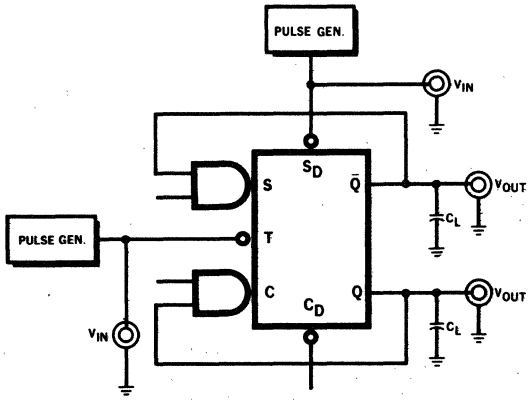
WAVE FORMS



TYPICAL DELAY CHARACTERISTICS LPDTμL 9040



TEST CIRCUIT

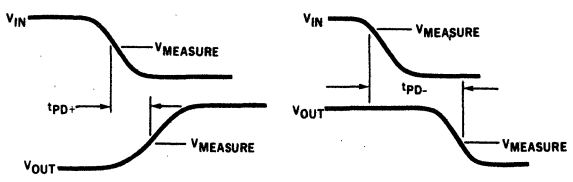


CONDITIONS

V_{CC} = 5.0V, C_L = 50pf (INCLUDING PROBE AND JIG CAPACITY)

$V_{MEASURE}$ = 1.6V @ -55°C
(GND. REF.) 1.3V @ 25°C
0.9V @ 125°C

WAVE FORMS



MμL9033

16-BIT MEMORY CELL

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MμL9033 is a Planar* epitaxial integrated 16-bit, bit-oriented, non-destructive readout memory cell, compatible with Fairchild Transistor-Transistor Micrologic® (TTμL) and other Compatible Current-Sinking Logic (CCSL) integrated circuits. This memory cell, organized as 16 words by one bit, is designed for high-speed scratch-pad memory applications.

OPERATION — The memory cell consists of 16 R-S flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "H" level (>2.1 volts) and holding the non-selected address lines at logic "L" level (<0.7 volts). As many as four locations may be addressed simultaneously without destroying stored information. The stored data and its complement at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the S_1 output will be low and the S_0 output will be high. If the addressed bit location contains a "0", the S_1 output will be high and the S_0 output will be low.

Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a High level. To write a "0", the input of the "write zero" (W_0) amplifier is raised to a High level.

The outputs are open-collector, which may be wire "OR"ed for word expansion. (The output transistors are off when none of the bits are selected.) An external resistor should be returned to V_{CC} to pull-up the wire "OR"ed outputs.

FEATURES

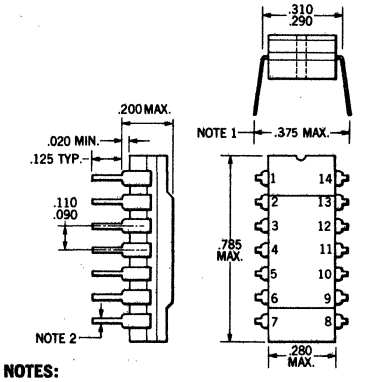
- **CCSL COMPATIBLE**
- **OUTPUT WIRED-OR CAPABILITY**
- **TRUE AND COMPLEMENTARY OUTPUTS ARE PROVIDED**
- **NON DESTRUCTIVE READ OUT**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to +5.5 V
Current Into Output Terminal	100 mA
Output Voltage	−0.5 V to +8.0 V

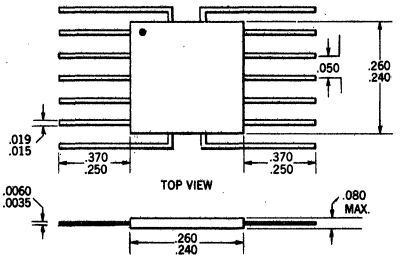
ORDER INFORMATION — Specify A3I9033XXX for Flat Package or A6A9033XXX for Dual In-Line (TO-116) package where XXX is 51X for −55°C to 125°C temperature range or 59X for the 0°C to 75°C range. The last digit in the order code is 1 for 40 mA Fanout and 2 for 20 mA Fanout.

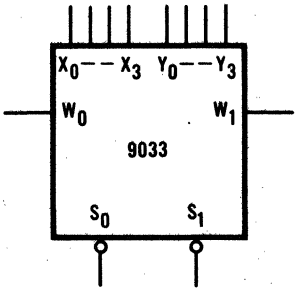
PHYSICAL DIMENSIONS
In Accordance With
JEDEC (TO-116) Outline
Dual In-Line Package



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

PHYSICAL DIMENSIONS
In Accordance With
JEDEC (TO-86) Outline
CERPAK I 14 lead





*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	TEST	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	$V_{CC} = 5.5\ V$, $V_X = 0\ V$, $V_Y = 4.5\ V$, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	$V_{CC} = 5.5\ V$, $V_Y = 0\ V$, $V_X = 4.5\ V$, other Y inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	$V_{CC} = 5.5\ V$, $V_X = 4.5\ V$, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	$V_{CC} = 5.5\ V$, $V_Y = 4.5\ V$, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	$V_{CC} = 5.5\ V$, $V_W = 0\ V$
I_{RW}	Write Input Leakage Current		100	μA	$V_{CC} = 5.5\ V$, $V_W = 4.5\ V$,
I_{CC}	Power Supply Current		65	mA	$V_{CC} = 5.5\ V$, All Inputs Grounded
I_{BV}	Power Supply Current at $V_{CC} = 7\ V$		84	mA	$V_{CC} = 7.0\ V$, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	$V_{CC} = 5.5\ V$, $V_{CEX} = 5.5\ V$, all inputs grounded
V_{OL}	Output Low Voltage		0.45	V	$V_{CC} = 4.5\ V$, One Bit Selected $I_{OL} = 20\ mA$ (A6A9033512 - A3F9033512)
$V_{XY(W)}$	Address Input Threshold to Prevent Writing		0.75	V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{XY(W)}$	Address Input Threshold to insure Writing	2.1		V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{XY(R)}$	Address Input Threshold to Prevent Reading		0.8	V	$V_{CC} = 5.0\ V$, other inputs grounded. Both outputs must be on "high" state.
$V_{XY(R)}$	Address Input Threshold to Insure Reading	2.1		V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		0.8	V*	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume low state. If W_1 is pulsed, S_1 will assume low state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.1		V*	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume low state. If W_1 is pulsed, S_0 will assume low state.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	TEST	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	$V_{CC} = 5.25\ V$, $V_X = 0\ V$, $V_Y = 4.5\ V$, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	$V_{CC} = 5.25\ V$, $V_Y = 0\ V$, $V_X = 4.5\ V$, other X inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	$V_{CC} = 5.25\ V$, $V_X = 4.5\ V$, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	$V_{CC} = 5.25\ V$, $V_Y = 4.5\ V$, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	$V_{CC} = 5.25\ V$, $V_W = 0\ V$
I_{RW}	Write Input Leakage Current		100	μA	$V_{CC} = 5.25\ V$, $V_W = 4.5\ V$
I_{CC}	Power Supply Current		65	mA	$V_{CC} = 5.25\ V$, All Inputs Grounded
I_{BV}	Power Supply Current at $V_{CC} = 7\ V$		95	mA	$V_{CC} = 7.0\ V$, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	$V_{CC} = 5.25\ V$, $V_{CEX} = 5.5\ V$, all inputs grounded
V_{OL}	Output Low Voltage		0.45	V	$V_{CC} = 4.75\ V$, One bit selected $I_{OL} = 20\ mA$ (A6A9033592 - A3F9033592) $I_{OL} = 40\ mA$ (A6A9033591 - A3F9033591)
$V_{XY(W)}$	Address Input Threshold to Prevent Writing		0.8	V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{XY(W)}$	Address Input Threshold to insure Writing	2.0		V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{XY(R)}$	Address Input Threshold to Prevent Reading		1.0	V	$V_{CC} = 5.0\ V$, other inputs grounded. Both outputs must be on "high" state.
$V_{XY(R)}$	Address Input Threshold to Insure Reading	2.0		V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		1.0	V*	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume low state. If W_1 is pulsed, S_1 will assume low state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.0		V*	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume low state. If W_1 is pulsed, S_0 will assume low state.

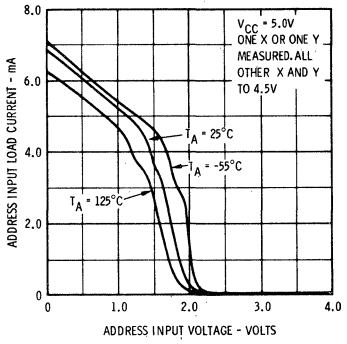
* Amplitude of the pulse $\geq 2.5\ V$, pulse width $\geq 100\ ns$. The cell state is determined 35 ns after pulse disappears.

SWITCHING CHARACTERISTICS

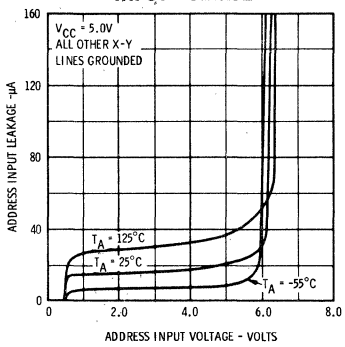
SYMBOL	CHARACTERISTICS	9033511 −55°C to 125°C MIN.	9033511 MAX.	9033591 0°C to 75°C MIN.	9033591 MAX.	9033592 0°C to 75°C MIN.	9033592 MAX.	UNITS	CONDITIONS LOAD (mA)	CONDITIONS C_L (pF)	CONDITIONS INPUT
t_{WP}	Write Pulse Width	25		25				ns	20		$V_{CC} = 5.0\ V$, One X-Y Location Selected
						25			40		
t_{WR}	Write Recovery Time		40		35			ns	20	30	
							35		40	30	
t_{on}	Turn On Delay		25		20			ns	20	30	$V_{CC} = 5.0\ V$, One X-Y Location Switched
			35		30				20	100	
							20		40	30	
							30		40	200	
t_{off}	Turn Off Read Delay		25		20			ns	20	30	
			35		30				20	100	
							20		40	30	
							30		40	200	

TYPICAL ELECTRICAL CHARACTERISTICS

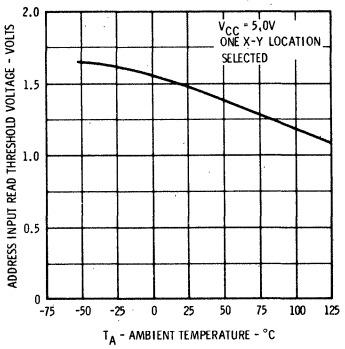
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



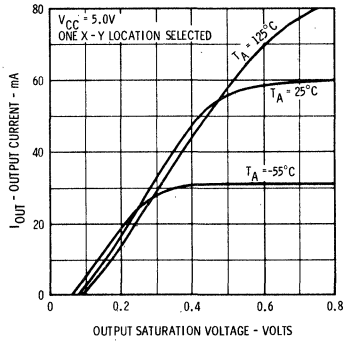
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



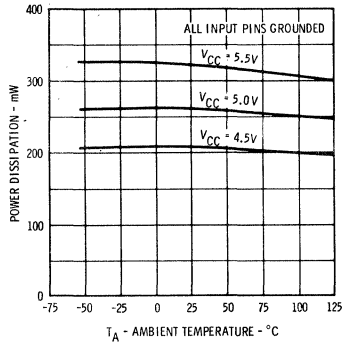
ADDRESS INPUT READ THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



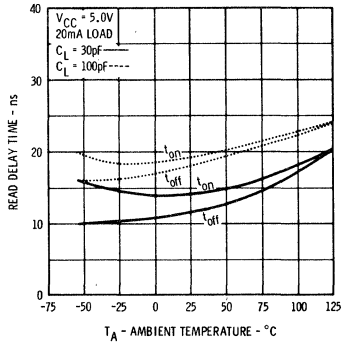
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



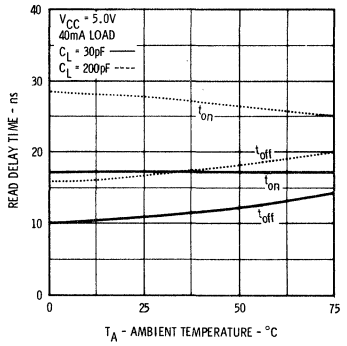
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



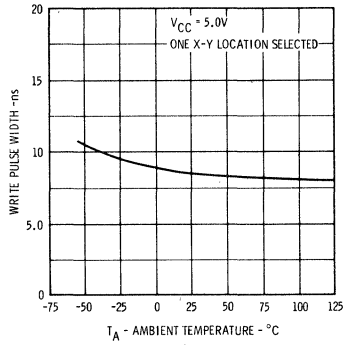
READ DELAY VERSUS AMBIENT TEMPERATURE 20 mA LOAD



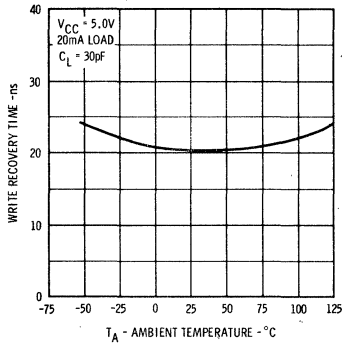
READ DELAY VERSUS AMBIENT TEMPERATURE 40 mA LOAD

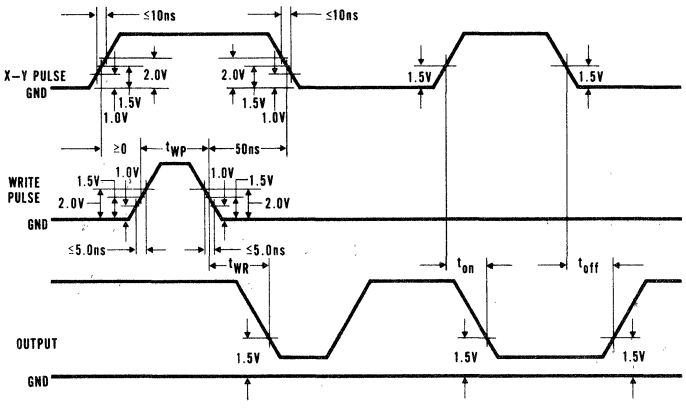


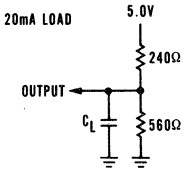
WRITE PULSE WIDTH VERSUS AMBIENT TEMPERATURE

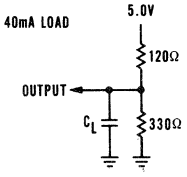


WRITE RECOVERY TIME VERSUS AMBIENT TEMPERATURE









APPLICATION:

A memory utilizing 9033 memory cells may have any desired word length. The number of words in the memory is a multiple of four words. The following example of a 64 word memory illustrates how a number of 16 bit memory cells 9033 may be used to construct a typical memory.

The 64 word memory as shown in Figure A consists of groups of four 9033 memory cells. Each of the groups of four 9033 memory cells supplies one bit for each of the 64 words stored in the memory. All bits belonging to one word are stored in the same address location. Therefore, the address of a word in the memory is the address of each of the bits of the addressed word in the groups of four 9033 memory cells. The equal outputs of the four memory cells are tied together so that each group of four memory cells has one high and one low level output.

The six memory address lines from an external source are decoded at the first level with two 9301 decoders. The fourth input to each of the two decoders can be used as an enable control input to the 64 word memory. If the address enable is at a low logic level, one and only one of the eight outputs, 0 to 7, in the illustration assumes a low logic level. If the address enable is at a high logic level, the outputs 0 to 7 of the two decoders assume a high logic level, thus none of the 64 words stored in the memory is addressed. The outputs, 0 to 7, of the two decoders serve as X-and-Y address lines. The output signals of the decoders are connected to driving transistors which provide the necessary current to address the memory cells.

The example given above is only one of the many organizations and is presented as an illustration. Obviously many address decoding schemes may be utilized depending on memory size, driver fan-out, decoder fan-out, wiring, heat dissipation, etc.

Figures B through D show alternative schemes to enter data into the memory cell.

LOGIC DIAGRAM

Fig. A

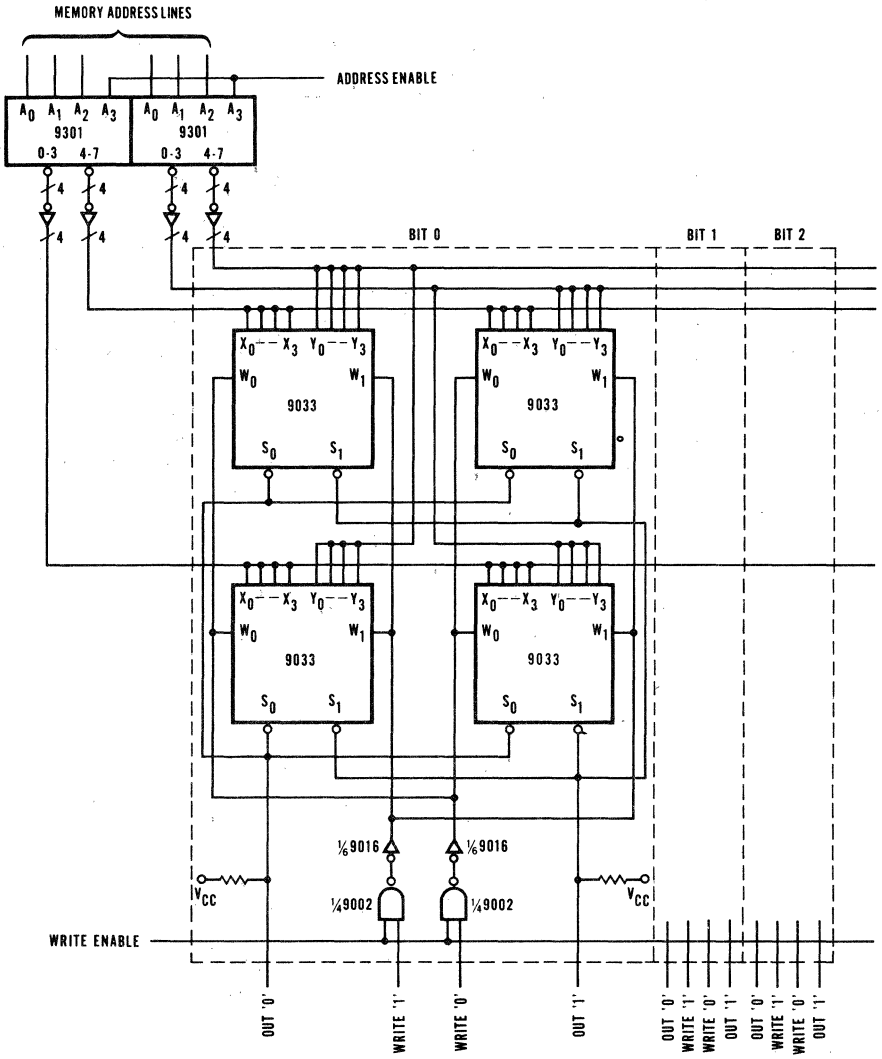


Fig. B
DOUBLE RAIL ACTIVE
LOW INPUTS AND ENABLE

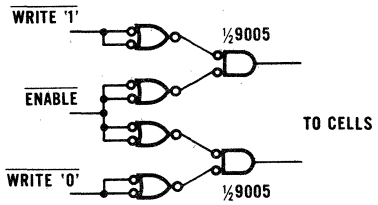


Fig. C
SINGLE RAIL ACTIVE
HIGH INPUT AND ENABLE

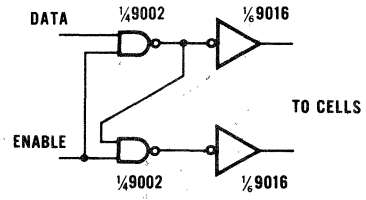
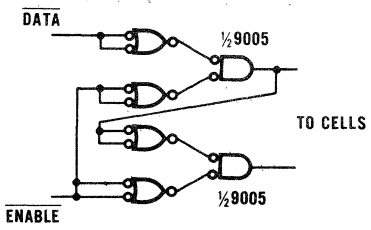


Fig. D
SINGLE RAIL ACTIVE
LOW INPUT AND ENABLE



MμL9034

256-BIT READ-ONLY MEMORY

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The Fairchild MμL9034 is a 256-bit bipolar transistor read-only memory. The memory is organized as 32 words of 8-bits each. The words are selected through 5 address lines. The 8 outputs of the words are uncommitted collectors which may be Wired-OR'd with the outputs of other ROMs. An Enable input is provided for additional decoding flexibility. A high on the Enable input forces all outputs to be high.

The contents of the memory are permanently programmed to customer order.

FEATURES:

- **CCSL COMPATIBLE**
- **OUTPUT WIRED-OR'D CAPABILITY**
- **SINGLE TTL LOAD INPUTS**

ABSOLUTE MAXIMUM RATINGS

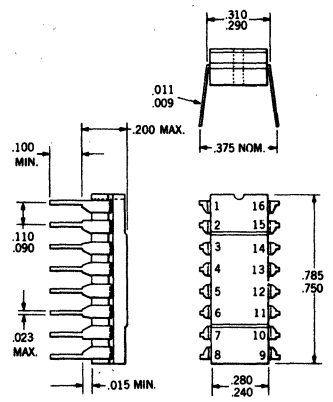
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to 5.5 V
Current Into Output Terminal	100 mA
Output Voltages	−0.5 V to V_{CC} Value

ORDER INFORMATION

Custom Code — Specify A6B9034XXX where X1X is for −55°C to +125°C temperature range or X9X is for 0°C to +75°C temperature range. Remaining X's are to be assigned alphabet letters to customer code.

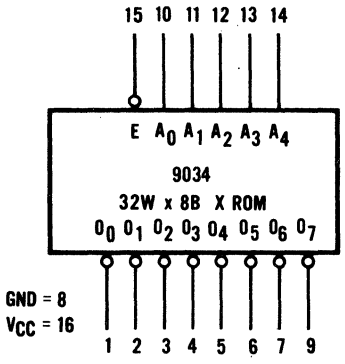
Standard Code Available — Two standard preprogrammed 9034s are available for evaluation purposes. The A6B9034AXA contains the numerals 1 through 6; the A6B9034AXB contains the figures 7 through 0, a comma, and a period. For additional information on these two programmed 9034s refer to their respective data sheets.

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

LOGIC DIAGRAM



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ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	TEST	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	TEST CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_A = 0.4\ V$
I_{FE}	Enable Input Load Current		−1.6		−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_E = 0.4\ V$
I_{RA}	Address Input Leakage Current		100		100		100	μA	$V_{CC} = 5.5\ V$ $V_A = 4.5\ V$
I_{RE}	Enable Input Leakage Current		100		100		100	μA	$V_{CC} = 5.5\ V$ $V_E = 4.5\ V$
I_{CEX}	Output Leakage Current		200		200		200	μA	$V_{CC} = 5.5\ V$ $V_{CEX} = 5.5\ V$ Enable input to 2.0 V
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OUT} = 10\ mA$ The word containing a "1" bit is selected when performing this test.
V_{IL}	Input Low Voltage		0.8		0.9		0.8	V	$V_{CC} = 5.5\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input High Voltage	2.0		1.7		1.4		V	$V_{CC} = 4.5\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
I_{PD}	Power Supply Current		80		80		80	mA	$V_{CC} = 5.5\ V$ All inputs grounded

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	TEST	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	TEST CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_A = 0.45\ V$
I_{FE}	Enable Input Load Current		−1.6		−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_E = 0.45\ V$
I_{RA}	Address Input Leakage Current		100		100		100	μA	$V_{CC} = 5.25\ V$ $V_A = 4.5\ V$
I_{RE}	Enable Input Leakage Current		100		100		100	μA	$V_{CC} = 5.25\ V$ $V_E = 4.5\ V$
I_{CEX}	Output Leakage Current		200		200		200	μA	$V_{CC} = 5.25\ V$ $V_{CEX} = 5.25\ V$ Enable input to 2.0 V
V_{OL}	Output Low Voltage		0.45		0.45		0.45	V	$V_{CC} = 4.75\ V$ $I_{OUT} = 10\ mA$ The word containing a "1" bit is selected when performing this test.
V_{IL}	Input Low Voltage		0.85		0.85		0.85	V	$V_{CC} = 5.25\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input High Voltage	1.9		1.8		1.6		V	$V_{CC} = 4.75\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
I_{PD}	Power Supply Current		80		80		80	mA	$V_{CC} = 5.25\ V$ All inputs grounded

SWITCHING TIME CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	TEST	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
t_{++}	Enable and Address Delay		*	50	ns	10 mA load. See Note 1.
t_{--}	Enable and Address Delay		*	50	ns	10 mA load. See Note 1.
t_{+-}	Address Delay		*	50	ns	10 mA load. See Note 2.
t_{-+}	Address Delay		*	50	ns	10 mA load. See Note 2.

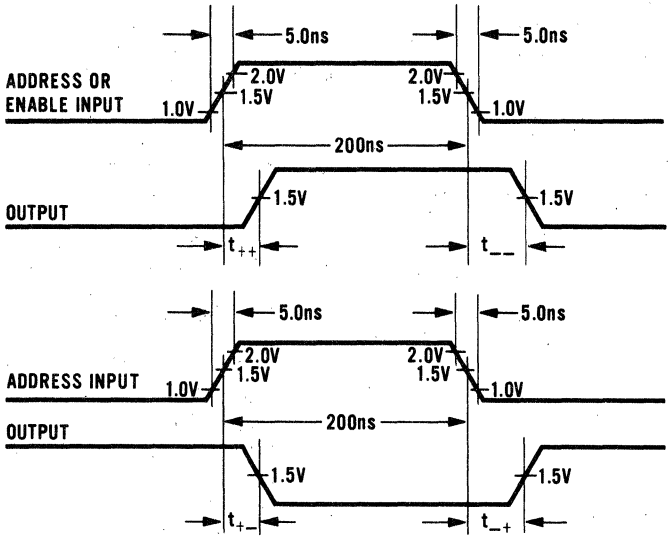
*See Typical Electrical Characteristics curves.

NOTES:

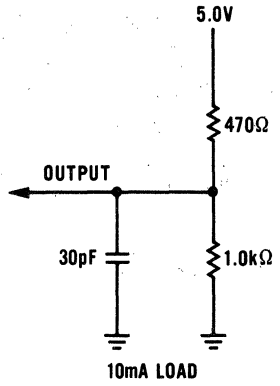
(1) To test Enable delay, apply input pulse to Enable input. The word selected must contain a "1" in the bit under test.
To test Address delay, the Enable input must be low. Apply the input pulse to the Address input under test. The words selected must contain a "1" when input pulse is low and a "0" when input pulse is high in the bit under test.

(2) To test Address delay, the Enable input must be low. Apply the input pulse to the Address input under test. The words selected must contain a "0" when input pulse is low and a "1" when input pulse is high in the bit under test.

SWITCHING TIME TEST CONDITIONS AND WAVEFORMS



SWITCHING TEST OUTPUT LOAD



LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOADING
All inputs	1.7/1 U.L.

OUTPUTS	DRIVE FACTOR
All outputs	Open Collector / 6.25 U.L.

1 U.L. = 1 TTμL Input Load

CCSL INPUT LOAD AND DRIVE FACTORS

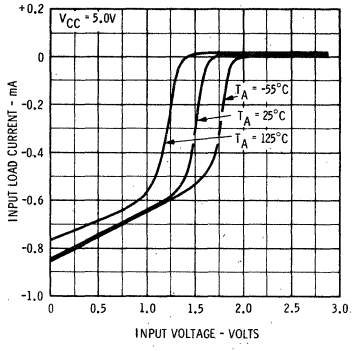
INPUTS	LOADING
All inputs	20/10

OUTPUTS	DRIVE FACTOR
All outputs	Open Collector / 62.5

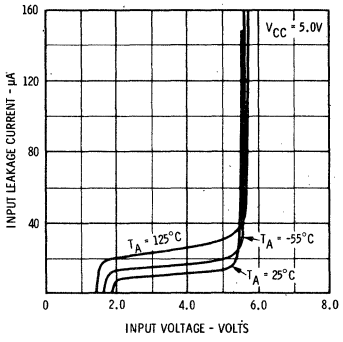
1 CCSL High Level Load Factor = 5.0 μA
1 CCSL Low Level Load Factor = 160 μA

TYPICAL ELECTRICAL CHARACTERISTICS

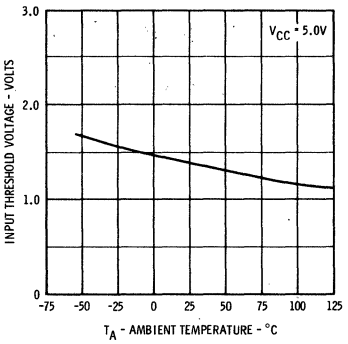
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



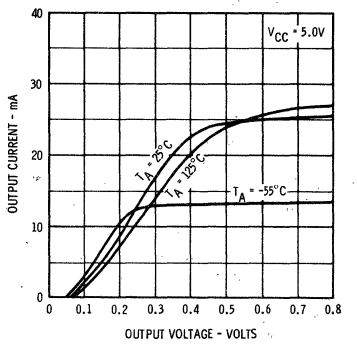
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



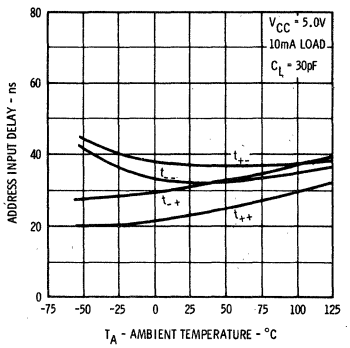
INPUT THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



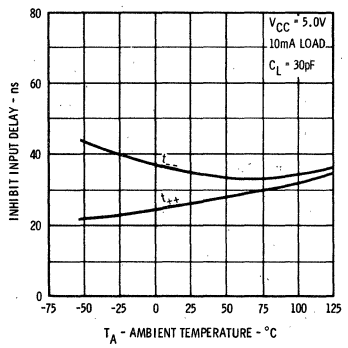
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



ADDRESS INPUT DELAY VERSUS AMBIENT TEMPERATURE



ENABLE INPUT DELAY VERSUS AMBIENT TEMPERATURE



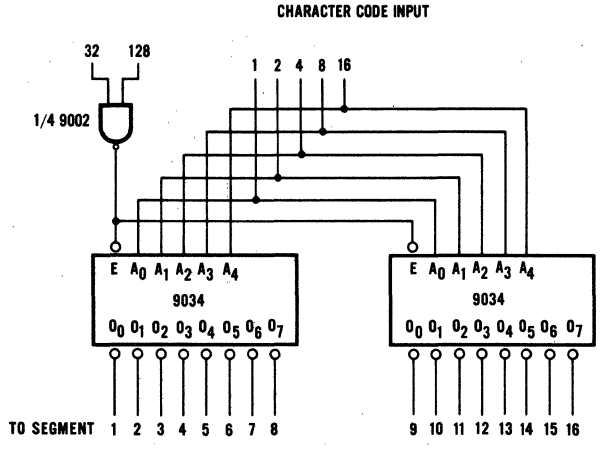
APPLICATIONS:

The Fairchild MμL9034 Read-Only Memory has many storage and display applications. Two main uses of the memory are for microprogrammed subroutines (core replacements) and character generator display systems.

APPLICATION OF THE 9034 READ-ONLY MEMORY IN DIFFERENT TYPES OF DISPLAY SYSTEMS.

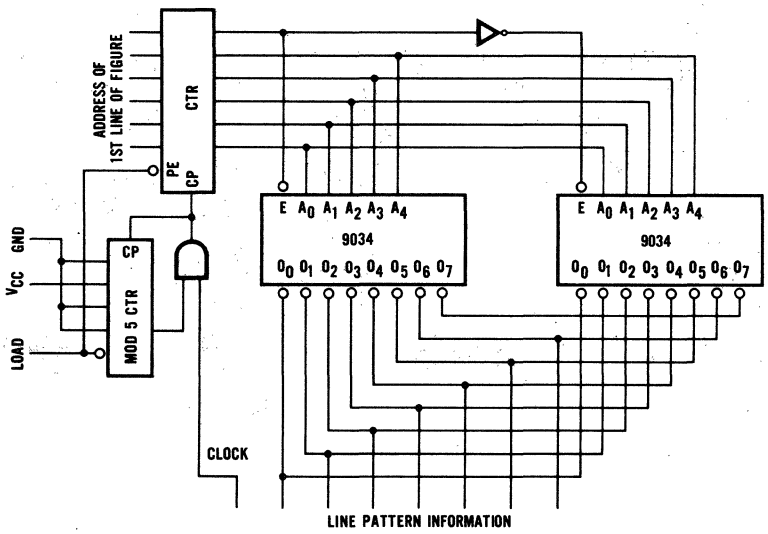
In the application of this ROM as display storage, the Enable input is the most important control, since every display system requires a number of ROM's organized in parallel to each other. The effectiveness of such a character storage system depends on the flexibility in addressing a desired character. Most of the character storage systems will be character code oriented.

16 SEGMENT DECODER



This figure illustrates the use of two 9034 ROMs for driving a 16 segment decoder. The character code is used directly as a control for both ROMs. One additional 3-input gate controlling the enable inputs of the two ROMs is required for selecting the group of codes within the ASCII system which refer to the characters. For uninterrupted control, two ROMs are required for each of the 16 segment display units.

DISPLAY GENERATOR 5 x 8 DOT MATRIX



The five 8-bit words representing the 5 x 8 dot pattern of a figure are stored in sequence. The external source which calls for a figure has to supply the address of the first 8-bit word of this figure. The clock will increment this address by one each time the generated pattern has been displayed until all five 8-bit patterns have been used. The mod. 5 counter calls for the first line address of the next figure automatically.

If these data are used to control a CRT display the outputs of the two 9034 ROMs may be connected to an 8-channel multiplexer (3705) which serves as an interface to the Z modulation input of the display unit. The eight channels are selected in sequence by a mod. 8 counter of which the eight output generates the control pulses for the mod. 5 and the address counter.

MμL9034AXA

256-BIT READ-ONLY MEMORY

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION

The 9034 Read-Only Memory code AXA (9034AXA) is programmed to store information for generating Figures 1 thru 6 on a 5 by 8 dot pattern display. The memory stores the information by using 5 consecutive words of 8 bits for each figure or symbol.

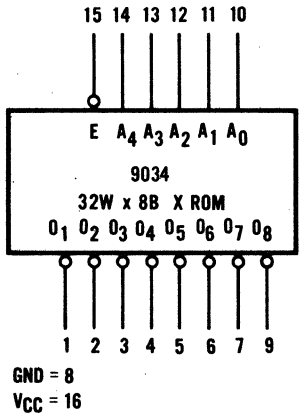
OPERATION AND ELECTRICAL CHARACTERISTICS

Refer to 9034 Data Sheet

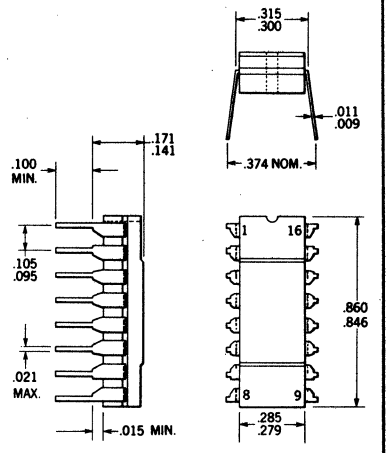
ORDER INFORMATION

Specify A6B9034AXA where A1A is for −55°C to +125°C temperature range or A9A for the 0°C to +75°C temperature range.

LOGIC SYMBOL

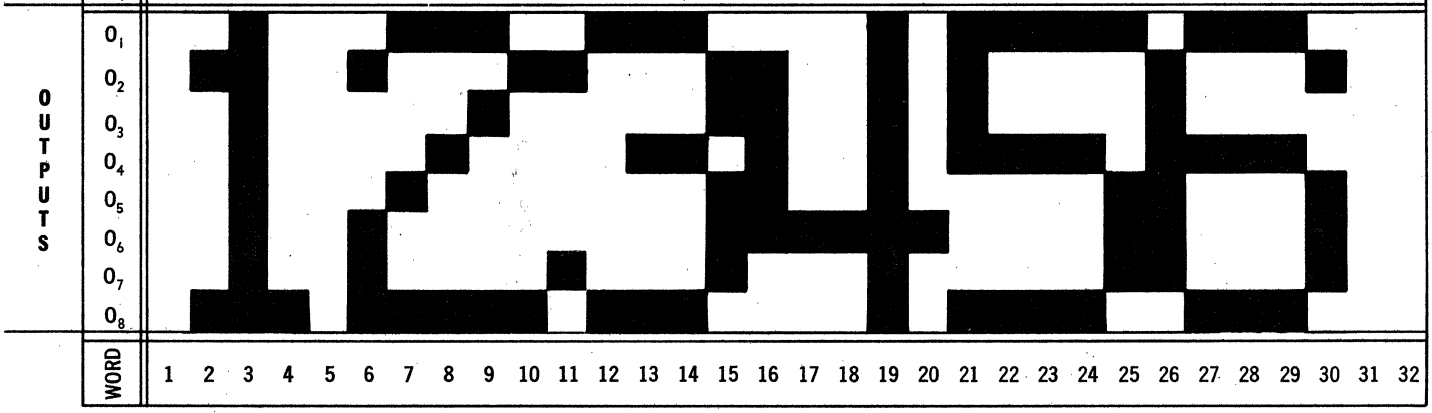


PHYSICAL DIMENSIONS



9034AXA TRUTH TABLE

		WORD 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
OUTPUTS	O_1	H	H	L	H	H	H	L	L	L	H	H	L	L	L	H	H	H	H	L	H	L	L	L	L	L	H	L	L	L	H	H	H
	O_2	H	L	L	H	H	L	H	H	H	L	L	H	H	H	L	L	H	H	L	H	L	H	H	H	H	L	H	H	H	L	H	H
	O_3	H	H	L	H	H	H	H	H	L	H	H	H	H	H	L	L	H	H	L	H	L	H	H	H	H	L	H	H	H	H	H	H
	O_4	H	H	L	H	H	H	H	L	H	H	H	H	L	L	H	L	H	H	L	H	L	L	L	L	H	L	L	L	L	H	H	H
	O_5	H	H	L	H	H	H	L	H	H	H	H	H	H	L	L	H	H	H	L	H	H	H	H	H	L	L	H	H	H	L	H	H
	O_6	H	H	L	H	H	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	H	H	H	H	L	L	H	H	H	L	H	H
	O_7	H	H	L	H	H	L	H	H	H	H	L	H	H	H	L	H	H	H	L	H	H	H	H	H	L	L	H	H	H	L	H	H
	O_8	H	L	L	L	H	L	L	L	L	L	H	L	L	L	H	H	H	H	L	H	L	L	L	L	H	H	L	L	L	H	H	H
INPUTS	A_0	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
	A_1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	A_2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	A_3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	A_4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H



L — Low Voltage H — High Voltage

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MμL9034AXB

256-BIT READ-ONLY MEMORY

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION

The 9034 Read-Only Memory code AXB (9034AXB) is programmed to store information for generating Figures 7 thru 0, a comma and period on a 5 x 8 dot pattern display. The memory stores the information by using 5 consecutive words of 8 bits for each figure or symbol.

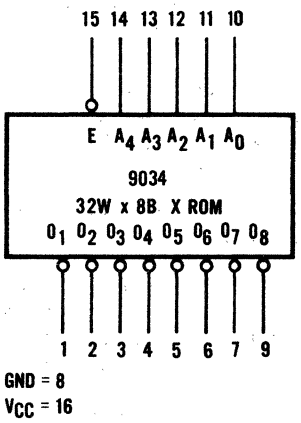
OPERATION AND ELECTRICAL CHARACTERISTICS

Refer to 9034 Data Sheet

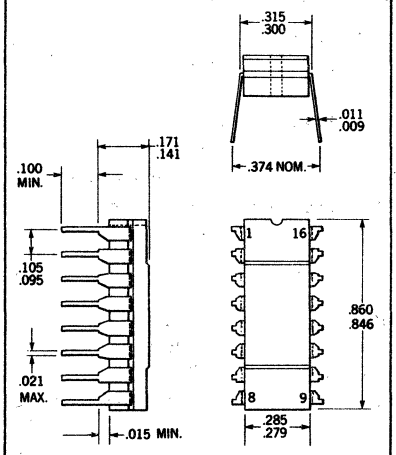
ORDER INFORMATION

Specify A6B9034AXB where A1B is for −55°C to +125°C temperature range or A9A for the 0°C to +75°C temperature range.

LOGIC SYMBOL

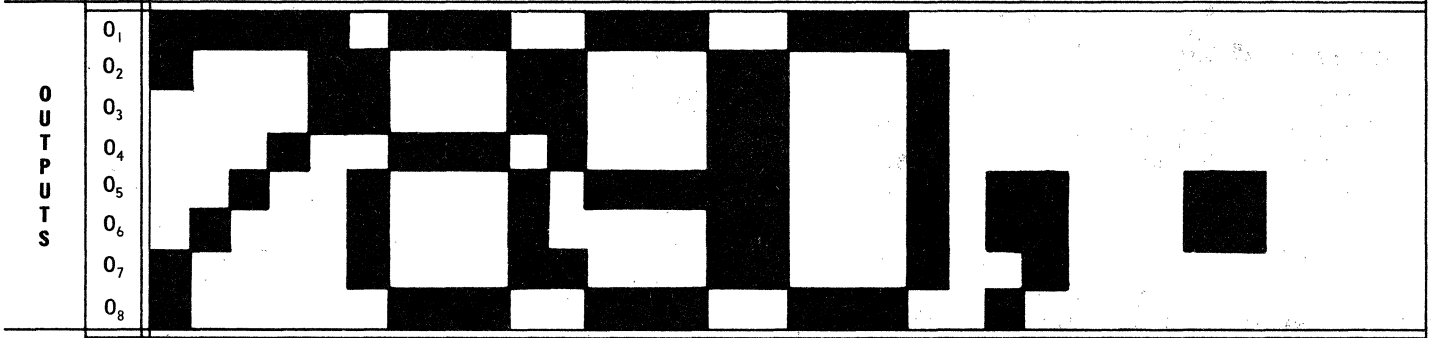


PHYSICAL DIMENSIONS



9034AXB TRUTH TABLE

		WORD	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
OUTPUTS	O_1		L	L	L	L	L	H	L	L	L	H	H	L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H
	O_2		L	H	H	H	L	L	H	H	H	L	L	H	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	O_3		H	H	H	H	L	L	H	H	H	L	L	H	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	O_4		H	H	H	L	H	H	L	L	L	H	L	H	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	O_5		H	H	L	H	H	L	H	H	H	L	H	L	L	L	L	L	H	H	H	L	H	L	L	H	H	H	L	L	H	H	H	H
	O_6		H	L	H	H	H	L	H	H	H	L	H	H	H	H	L	L	H	H	H	L	H	L	L	H	H	H	L	L	H	H	H	H
	O_7		L	H	H	H	H	L	H	H	H	L	L	H	H	H	L	L	H	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H
	O_8		L	H	H	H	H	H	L	L	L	H	H	L	L	L	H	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H
INPUTS	A_0		L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
	A_1		L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	A_2		L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	A_3		L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	A_4		L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H



L — Low Voltage H — High Voltage

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

MµL9035

64-BIT READ/WRITE MEMORY CELL

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9035 is a high speed 64-bit read/write memory cell designed for use in high speed scratch pad memories. It is organized in a linear select 16 word by 4-bit array. The 9035 is made with TTμL circuitry making it CCSL compatible.

The 9035 is available in the hermetically sealed 36-pin ceramic dual in-line package and will operate over the temperature range from −55°C to +125°C.

OPERATION — In addition to 16 address lines, 4 data outputs, and 4 data inputs, the 9035 has a chip select and a write enable. When the chip select is high, a word may be addressed by a high on the address input. Data is written into the addressed word only when the write enable is held low. While the address is present, the outputs continuously show the contents of the word selected. Readout is non-destructive.

Up to four words may be addressed and read simultaneously with the OR function of the words appearing at the output. Data can be written into two locations simultaneously.

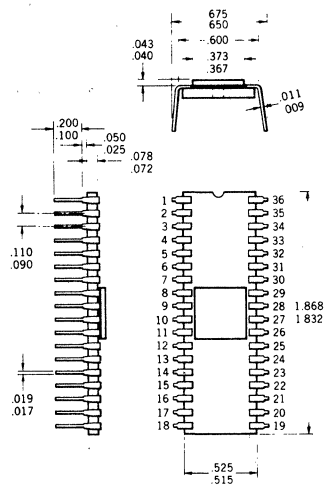
Uncommitted collector outputs are provided on the 9035 to allow maximum flexibility in output connection. In many applications such as word expansion, the outputs of many 9035's are wire-OR'd together. In other applications the wire-OR is not used. In either case an external pullup resistor of value R must be used to provide a high at the output when it is off. Any value of R within the range specified below may be used.

$$\frac{5.1}{10 - \text{F.O.}\,(1.6)} \leq R \leq \frac{2.1}{N(0.1) + \text{F.O.}\,(0.06)}$$

R is in KΩ
N = number of outputs wire-OR'd
F.O. = number of TTμL loads driven

The minimum value of R is limited by output current sinking ability. The maximum value of R is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

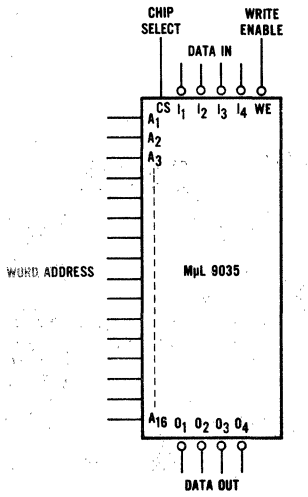
PHYSICAL DIMENSIONS



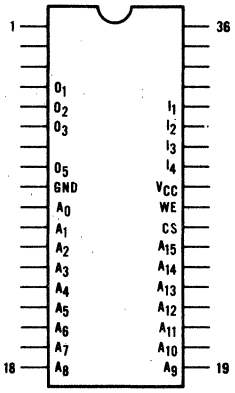
FEATURES:

- **35 ns READ ACCESS TIME**
- **CHIP SELECT AND WRITE ENABLES**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRE OR CAPABILITY**
- **LINEAR SELECT**
- **ON CHIP ADDRESS LINE BUFFERING**
- **CCSL COMPATIBLE**

LOGIC DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltage	−0.5 V to +8.0 V

ORDER INFORMATION — Specify A6H*9035XXX where XXX is 51X for the −55°C to +125°C temperature range or 59X for the 0°C to 75°C temperature range.

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LOADING RULES

	HIGH LEVEL (TTμL Unit Loads)	LOW LEVEL (TTμL Unit Loads)
Address	1.67	1
Chip Select	26.7	1 (see note 1)
Write Enable	1.67	1
Data Input	3.34	2
Data Output	Open Collector	6.2

1 Low Level TTμL Unit Load = 60 μA

1 High Level TTμL Unit Load = −1.6 mA

ELECTRICAL CHARACTERISTICS (T_A = −55°C to 125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	TEST	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_A = 0.4 V
I_{FS}	Chip Select Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_{CS} = 0.4 V See Note 1
I_{FW}	Write Enable Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_W = 0.4 V
I_{FD}	Data Input Load Current		−3.2		−3.2		−3.2	mA	V_{CC} = 5.5 V, V_D = 0.4 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_A = 4.5 V
I_{RS}	Chip Select Input Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.5 V, V_{CS} = 4.5 V
I_{RW}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.5 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		200		200		200	μA	V_{CC} = 5.5 V, V_{CEX} = 5.5 V Enable Input Grounded
V_{OL}	Output "Low" Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 10 mA One Word Selected
V_{IL}	Input "Low" Voltage		0.8		0.8		0.8	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input "High" Voltage	2.1		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		118		118		118	mA	V_{CC} = 5.5 V, One Word Selected

NOTE 1: I_{FE} increases by 1.6 mA for each address enable held at a logical 1.

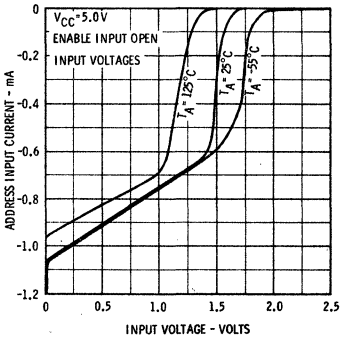
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	TEST	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FS}	Chip Select Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V See Note 1
I_{FW}	Write Enable Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FD}	Data Input Load Current		−3.2		−3.2		−3.2	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RE}	Chip Select Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RW}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		200		200		200	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25 V Enable Input Grounded
V_{OL}	Output "Low" Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 10 mA One Word Selected
V_{IL}	Input "Low" Voltage		0.85		0.85		0.85	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input "High" Voltage	2.0		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		124		124		124	mA	V_{CC} = 5.25 V, One Word Selected

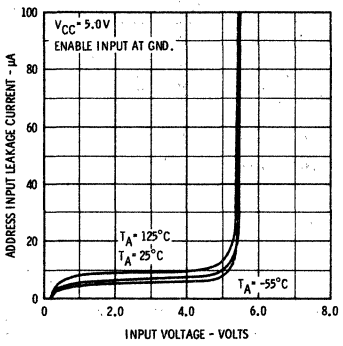
NOTE 1: I_{FE} increases by 1.6 mA for each address enable held at a logical 1.

TYPICAL ELECTRICAL CHARACTERISTICS

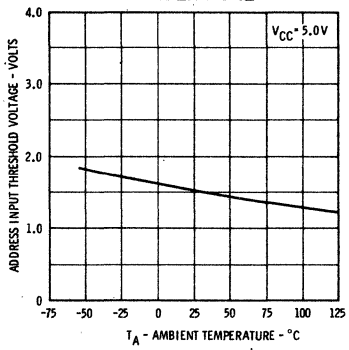
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



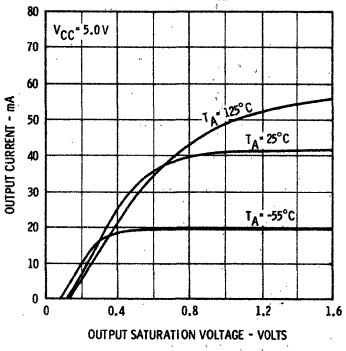
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



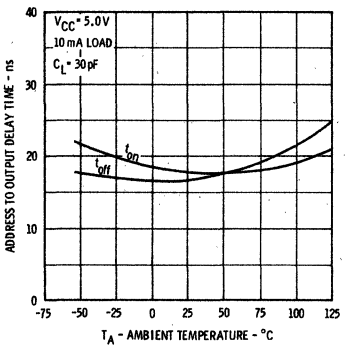
ADDRESS INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



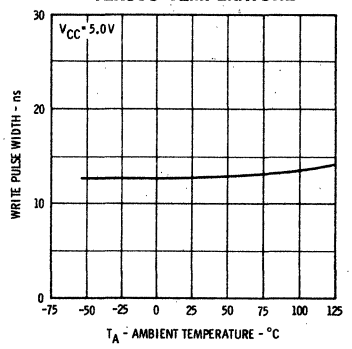
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



ADDRESS TO OUTPUT DELAY TIME VERSUS TEMPERATURE



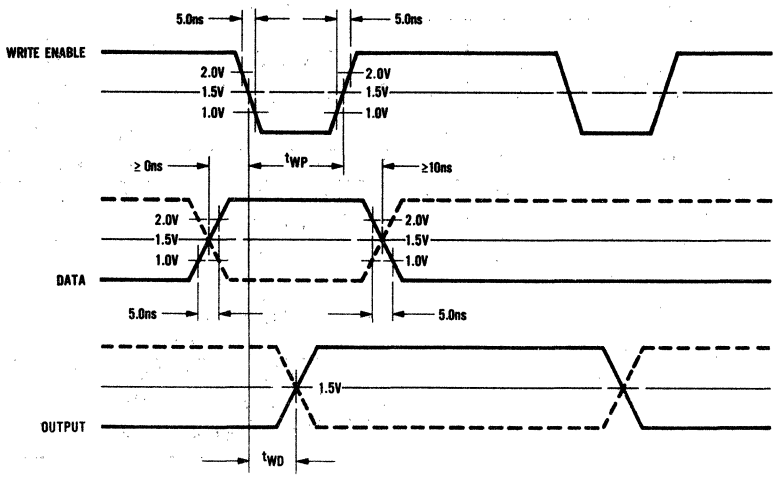
WRITE PULSE WIDTH VERSUS TEMPERATURE

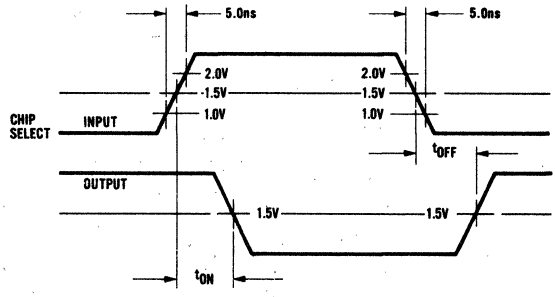


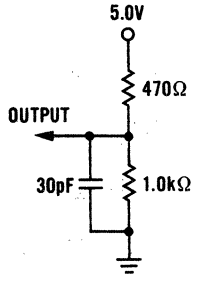
SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

SYMBOL	TEST	LIMIT (ns)			CONDITION		
		MIN.	TYP.	MAX.	LOAD	C	NOTE
t_{on}	Address to Output Turn-On Delay		16	35	10 mA	30 pF	1
t_{off}	Address to Output Turn-Off Delay		18	35	10 mA	30 pF	1
t_{WP}	Write Pulse Width Required to Write	25	15		10 mA	30 pF	2
t_{WD}	Write Delay		30	50	10 mA	30 pF	2

NOTE 1: To test t_{on} and t_{off}, a "Low" must be stored in the cell under test.
NOTE 2: One word is selected during the test.



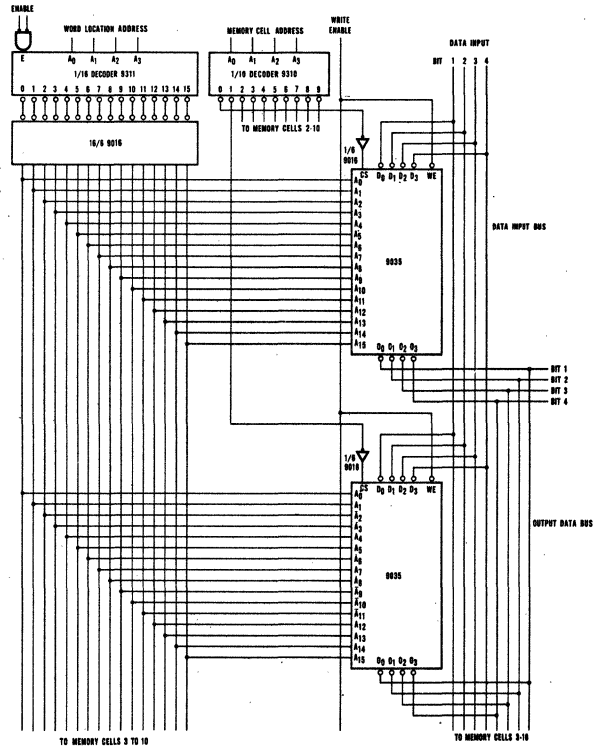




10 mA TEST LOAD

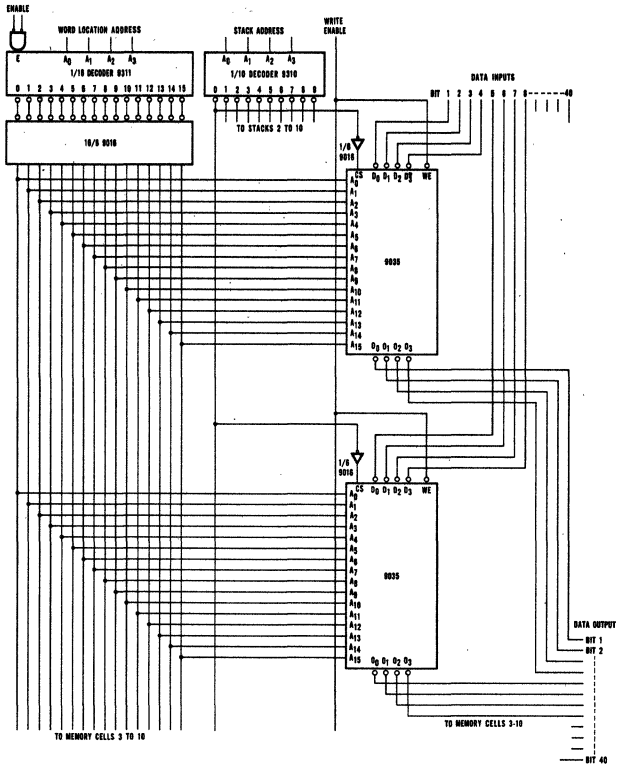
APPLICATIONS

MEMORY EXPANSIONS: N16 WORDS BY 4-BITS



In this application the 9035 memory cells are connected in parallel and two levels of decoding are performed. One of the cells is selected by the 9310 decoder and then a word is addressed by the 9316.

MEMORY STACK 160 WORDS OF 40-BITS



There are 16 words by 40 bits for each stack. The outputs and inputs of all stacks are tied together. Stack 1 contains words 1-16, stack 2, 17-32, and so on through 144-160 for the 10th stack. The stack address decoder tells which word group (1-16 or 17-32, etc.) is addressed while the word location decoder addresses one of the 16 words of the stack addressed. The entire memory has 40 data input lines, 40 data output lines, 8 address lines, and a write enable line.

4501

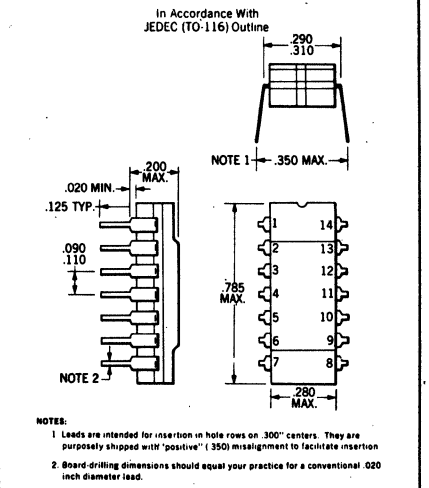
CCSL MICROMATRIX™ QUARTER-CELL

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 4501 consists of a single 4-input DTμL gate designed for use in breadboarding the 4500 Micromatrix™. It corresponds to one of the 32 quarter-cells available in the 4500 Micromatrix array. Logic flexibility is offered with pin options for interconnections of four independent elements. These elements are a) 4-diode cluster, b) non-inverting amplifier, c) common emitter inverting amplifier and d) load resistor.

PHYSICAL DIMENSIONS

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES

- **Offers 4500 Micromatrix breadboarding capability**
- **Compatible with all CCSL devices**

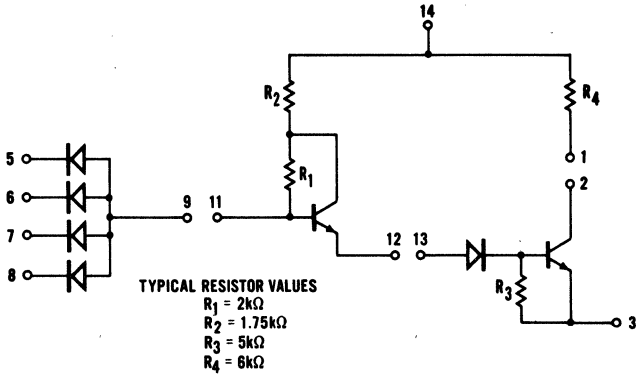
ABSOLUTE MAXIMUM RATINGS

V_{CC} Pin Potential to Ground Pin	−.5 V to +7 V
Input Voltage	−.5 V to +5.5 V
Voltage Applied to Outputs	−.5 V to +V_{CC} Value
Storage Temperature	−65°C to +150°C
Temperature (ambient) under Bias	−55°C to +125°C

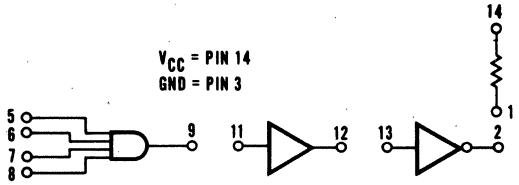
ORDER INFORMATION

Specify A6A45015XX, where 5XX is 51X for −55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.
To order 4500 design kit, specify A6A4501KTX

CIRCUIT SCHEMATIC (PIN NUMBERS)



LOGIC DIAGRAM (PIN NUMBERS)



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FAIRCHILD
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ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V = 10\%$) Connected as NAND gate with pull-up resistor
MILITARY TEMPERATURE RANGE

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.6		2.6	3.4		2.5		Volts	$V_{CC} = 4.5$ V, V_{IL} on any input, $I_{OH} = -180\ \mu A$
V_{OL}	Output Low Voltage		0.4		0.22	0.4		0.4	Volts	$V_{CC} = 5.5$ V, $I_{OL} = 8$ mA $V_{CC} = 4.5$ V, $I_{OL} = 6.2$ mA
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.3			1.0		0.7	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		1.6		1.18	1.6		1.6	mA	$V_{CC} = 5.5$ V, $V_F = 0.4$ V
			1.24		0.91	1.24		1.24	mA	$V_{CC} = 4.5$ V, $V_F = 0.4$ V
I_R	Input Leakage Current					2		10	μA	$V_R = 4$ V, GND on other inputs
P_D	Power Dissipation					15.5			mW	$V_{CC} = 5$ V Inputs open, pull-up connected
						8.8			mW	$V_{CC} = 5$ V Any input grounded

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0$ V = 5%) Connected as NAND gate with pull-up resistor
INDUSTRIAL TEMPERATURE RANGE

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.6		2.6	3.65		2.5		Volts	$V_{CC} = 4.75$ V, V_{IL} on any input, $I_{OH} = -180\ \mu A$
V_{OL}	Output Low Voltage		0.45		0.22	0.45		0.45	Volts	$V_{CC} = 5.25$ V, $I_{OL} = 9.6$ mA $V_{CC} = 4.75$ V, $I_{OL} = 8.5$ mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.1			1.0		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		1.6		1.09	1.6		1.6	mA	$V_{CC} = 5.25$ V, $V_F = 0.45$ V
			1.41		0.96	1.41		1.41	mA	$V_{CC} = 4.75$ V, $V_F = 0.45$ V
I_R	Input Leakage Current					5		10	μA	$V_R = 4$ V, GND on other inputs
P_D	Power Dissipation					16.5			mW	$V_{CC} = 5$ V Inputs open, pull-up connected
						9			mW	$V_{CC} = 5$ V Any input grounded

Loading and interconnections for 4501 are identical to 4500 Micromatrix array except for Note 3.

LOADING RULES

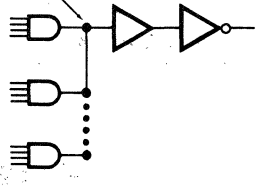
Connected as NAND gate with pull-up resistor

Fan-in 1 DTμL unit load

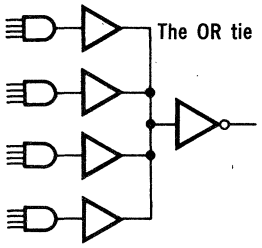
Load	Fan-out 51X	Fan-out 59X
DTL	5	6
TTL	3	3

INTERCONNECTION RULES

Expanding the input



Maximum fan-in — 20 inputs corresponding to 5 diode clusters.
Fan-out — same as NAND gate.



If OR tie is utilized, 4501 fan-out is restricted to 3 unit loads for 51X temperature range operation (4 unit loads for 59X temperature range.) (Note 3.)

Maximum of 4 OR ties allowed.

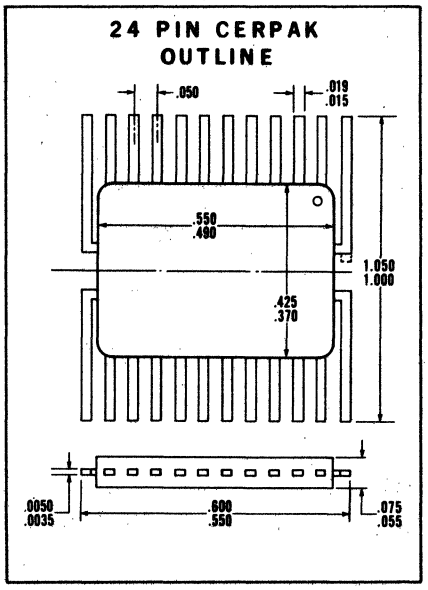
Note 3: Fan-out of 5 (6 for 59X temperature range) with OR tie used, can be maintained if temperature range of operation is limited to +15°C to +125°C (+15°C to +75°C for 59X temperature range.)

4510

CCSL MICROMATRIX™ DUAL 4-BIT COMPARATOR

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 4510 consists of two independent 4-bit comparators useful in many decision making control applications, such as digital printers. Each comparator is capable of accepting two 4-bit inputs and provides a high level output signal when they are identical. An output latch stores the compared output when the strobe pin is high. Outputs may be "Wire ANDed" to expand comparison capability.
The circuit is produced with two layer metal interconnections using the Fairchild 4500 Bipolar Micromatrix™ Array.



FEATURES

- **ASYNCHRONOUS AND SYNCHRONOUS OUTPUTS**
- **OPTIONAL LATCH STORAGE OF OUTPUT**
- **EXPANDABLE IN GROUPS OF 4 BITS**
- **TYPICAL POWER DISSIPATION OF 250 mW**
- **CCSL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" 24 PIN CERPAK**
- **MEMBER OF 4500 MICROMATRIX™ ARRAY FAMILY**
- **TWO LAYER METAL INTERCONNECTIONS**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Voltage Applied to Output for High Output State	−0.5 V to +V_{CC} Value
Output Current Into Low Output State	20 mA
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify A3M45105XX for flat package, where 5XX is 51X for −55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

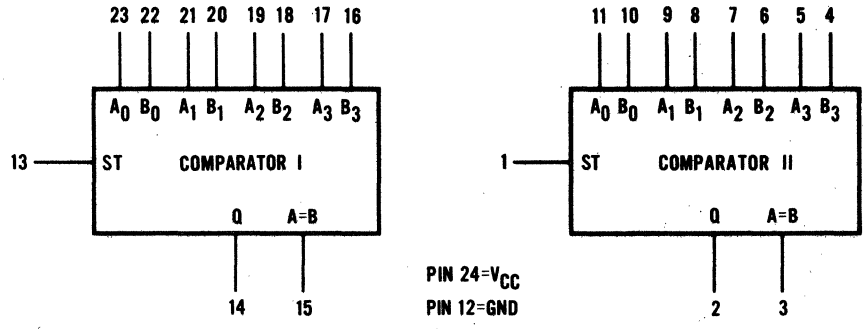


Fig. 1 — 4510 DUAL 4-BIT COMPARATOR LOGIC DIAGRAM

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V = 10\%$)
MILITARY TEMPERATURE RANGE

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+125°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Q Output High Voltage	2.6		2.6	3.4		2.5		Volts	$I_{OH} = -180\ \mu A$ { V_{IL} on any two inputs
	A = B Output High Voltage	2.6		2.6	3.4		2.5		Volts	$I_{OH} = -240\ \mu A$ { $V_{CC} = 4.5\ V$
V_{OL}	Output Low Voltage Q and A = B Output		0.4		0.22	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 6.4\ mA$ { V_{ST} = GND for $V_{CC} = 4.5\ V$ $I_{OL} = 5.0\ mA$ { A = B output only
	Output Low Voltage A = B Output Only		0.4		0.22	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 4.8\ mA$ { $V_{ST} = 4\ V$ $V_{CC} = 4.5\ V$ $I_{OL} = 3.7\ mA$
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.3			1.0		0.7	Volts	Guaranteed input low threshold for all inputs
$2\ I_F$	Input Load Current		3.2		2.36	3.2		3.2	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			2.43		1.82	2.48		2.48	mA	$V_{CC} = 4.5\ V$ $V_F = 0.4\ V$
$1.5\ I_F$	A = B Output Load Current For "Wired AND"		2.4		1.77	2.4		2.4	mA	$V_{CC} = 5.5\ V$ { $V_F = 0.4\ V$
			1.86		1.37	1.86		1.86	mA	$V_{CC} = 4.5\ V$ { V_{ST} = GND
$2.5\ I_F$			4.0		2.95	4.0		4.0	mA	$V_{CC} = 5.5\ V$ { $V_F = 0.4\ V$
			3.1		2.28	3.1		3.1	mA	$V_{CC} = 4.5\ V$ { $V_{ST} = 4\ V$
I_R	Input Leakage Current					20		20	μA	$V_R = 4\ V$, GND on other inputs
t23+ 15+	Comparison Switching Speed				50				ns	$V_{CC} = 5\ V$
t23− 15−	A_O to A = B				50				ns	$C_L = 15\ pF$ @ Pin 15

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V = 5\%$)
INDUSTRIAL TEMPERATURE RANGE

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Q Output High Voltage	2.6		2.6	3.65		2.5		Volts	$I_{OH} = -180\ \mu A$ { V_{IL} on any two inputs
	A = B Output High Voltage	2.6		2.6	3.65		2.5		Volts	$I_{OH} = -300\ \mu A$ { $V_{CC} = 4.75\ V$
V_{OL}	Output Low Voltage Q and A = B Output		0.45		0.22	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 8.0\ mA$ { V_{ST} = GND for $V_{CC} = 4.75\ V$ $I_{OL} = 6.25\ mA$ { A = B output only
	Output Low Voltage A = B Output Only		0.45		0.22	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 6.4\ mA$ { $V_{ST} = 4\ V$ $V_{CC} = 4.75\ V$ $I_{OL} = 5.0\ mA$
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.1			1.0		0.8	Volts	Guaranteed input low threshold for all inputs
$2\ I_F$	Input Load Current		3.2		2.18	3.2		3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
			2.82		1.92	2.82		2.82	mA	$V_{CC} = 4.75\ V$ $V_F = 0.45\ V$
$1.5\ I_F$	A = B Output Load Current For "Wired AND"		2.4		1.65	2.4		2.4	mA	$V_{CC} = 5.25\ V$ { $V_F = 0.4\ V$
			2.11		1.44	2.11		2.11	mA	$V_{CC} = 4.75\ V$ { V_{ST} = GND
$2.5\ I_F$			4.0		2.64	4.0		4.0	mA	$V_{CC} = 5.25\ V$ { $V_F = 0.4\ V$
			3.52		2.4	3.52		3.52	mA	$V_{CC} = 4.75\ V$ { $V_{ST} = 4\ V$
I_R	Input Leakage Current					20		20	μA	$V_R = 4\ V$, GND on other inputs
t23+ 15+	Comparison Switching Speed				50				ns	$V_{CC} = 5\ V$
t23− 15−	A_O to A = B				50				ns	$C_L = 15\ pF$ @ Pin 15

FUNCTIONAL DESCRIPTION

ASYNCHRONOUS — Fig. 2 shows the detailed logic representation of the comparator and latch (½ 4510). Whenever the 4-bit data word on lines A is identical to the 4-bit data word on lines B the A = B output is high. If data word A is not equal to data word B the A = B output is low.

SYNCHRONOUS — The strobe (ST) and the latch output (Q) provide storage capability of the A = B output. This function is shown in Table 1. When ST is high, Q_N equals the A = B output. When ST is low, $Q_N = Q_{N-1}$.

TABLE 1

TRANSITION TABLE FOR LATCH OUTPUT (Q)

ST	Q_N
Low	Q_{N-1}
High	A = B

DETAILED LOGIC DIAGRAM

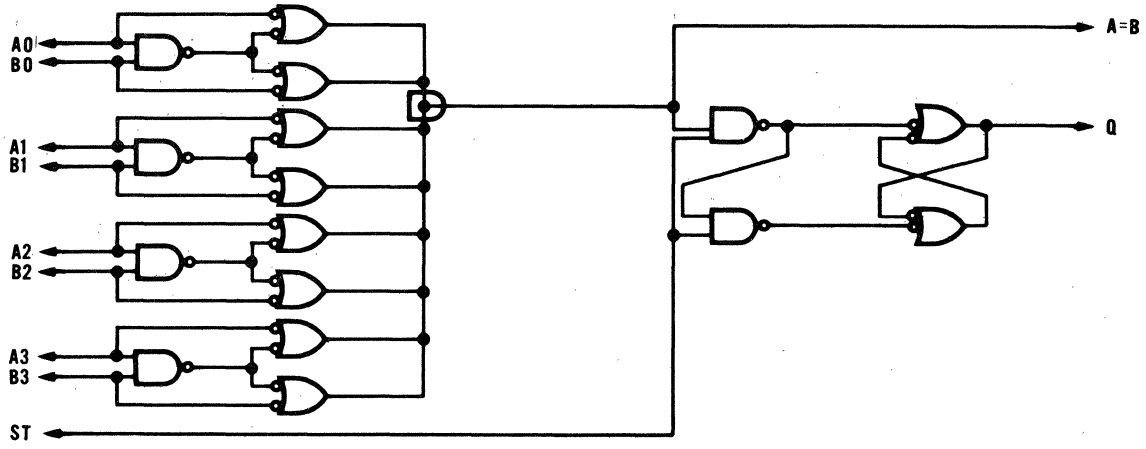
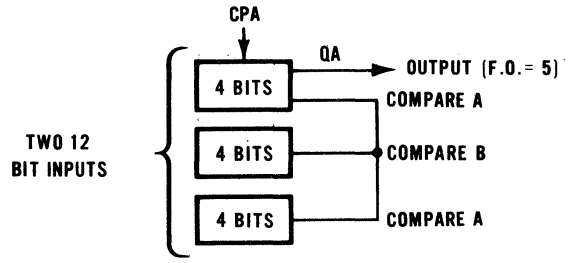


Fig. 2

SUGGESTED COMPARATOR EXPANSION METHODS



The internal "wired OR" COMPARE node uses two pull-up resistors for improved rise time, and drives an internal gate. Two COMPARE outputs may be "wire OR'd" externally to provide a 12 bit comparator as shown in Figure 3. This may be expanded further by using additional gates.

Fig. 3

4510 EQUIVALENT CIRCUITS

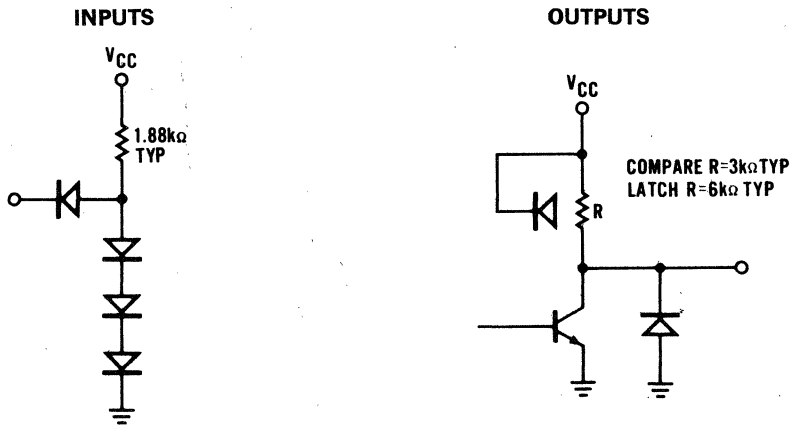


Fig. 4

LOADING RULES

INPUT LOADING RULES (FAN-IN)
DTμL UNIT LOADS

	51X	59X
Data Inputs	2.0	2.0
Strobe Inputs	2.0	2.0
"Wired AND" A = B Outputs (ST GND)	1.5	1.5
A = B Outputs (ST High)	2.5	2.5

OUTPUT DRIVE CAPABILITY (FAN-OUT)

	DTμL LOADS				TTμL LOADS			
	ST = GND		ST = HIGH		ST = GND		ST = HIGH	
	51X	59X	51X	59X	51X	59X	51X	59X
Q OUTPUT	4.0	5.0	4.0	5.0	3.0	3.0	3.0	3.0
A = B Outputs	4.0	5.0	3.0	4.0	4.0	5.0	3.0	4.0
(1) "Wired AND" 2	2.5	3.5	1.5	2.5	2.5	3.5	1.5	2.5
(1) "Wired AND" 3	1.0	2.0	0	1.0	1.0	2.0	0	1.0

(1) "Wired AND" 2 and 3 means the number of compare outputs (A = B) that are connected together. The result of this "Wired AND" connection, logically, is a high level true "AND" gate.

4-BIT COMPARATOR AND LAMP/RELAY DRIVER

One-half of a 4510 dual comparator drives a discrete driver so that when $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, and $A_3 = B_3$ the lamp will light or the relay operate. This circuit might also be used for a digital printer solenoid driver. The ST input is connected through a 2 kΩ resistor to V_{CC} so that Q and A = B may be paralleled for additional driver base current.

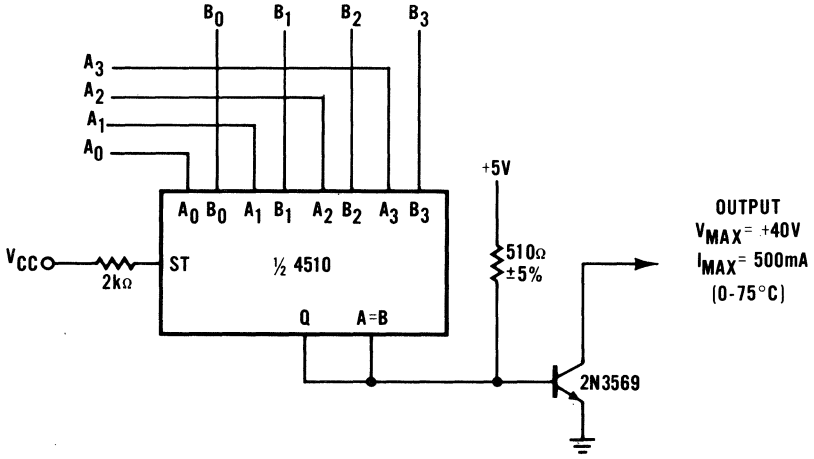


Fig. 5

4601

TTL MICROMATRIX™ ARRAY INTERNAL QUARTER-CELL

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 4601 is a single 4-4 AND-OR-INVERT (AOI) TTμL gate to be used for breadboarding logic designs planned for the 4600 or 4700 Micromatrix™ arrays. The 4601 corresponds to one of the quarter-cell gate elements that are intended for internal (on-chip) usage on the 4600 or 4700 arrays. Standard family TTμL gates such as the 9002 through 9008 may be used to breadboard the quarter-cells having external drive capability. The TTμL 9006 may be used to extend the 4601 at the OR tie points.

FEATURES

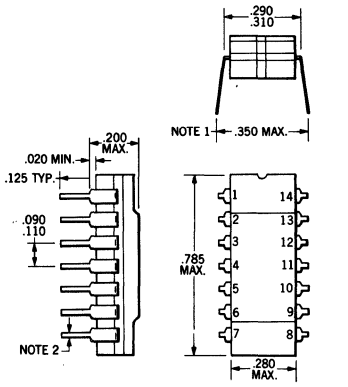
- **"INTERNAL" TYPE LOGIC GATES FOR BREADBOARDING 4600 OR 4700 MICROMATRIX ARRAY DESIGNS**
- **CCSL COMPATIBLE**
- **OR EXTENDABLE WITH TTμL 9006**
- **FANOUT = 7 INTERNAL LOADS OR 4.5 EXTERNAL LOADS**
- **"WIRED-AND" OUTPUT CAPABILITY**
- **INPUT CLAMP DIODES FOR RINGING ATTENUATION**

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential Referenced to Ground	−0.5 V to 7 V
Input Voltage Applied to Input	−0.5 V to 5.5 V
Voltage Applied to Output When Output is High	V_{CC}
Input Current Into Inputs	5 mA
Current Into Output When Output is Low	30 mA
Lead Temperature (soldering, 60 seconds)	300°C

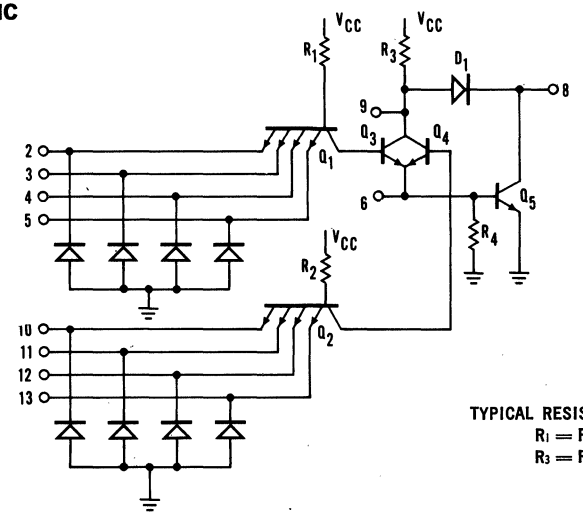
ORDER INFORMATION — Specify A6A46015XX where 5XX is 51X for −55°C to +125°C temperature range and $V_{CC} = 5\ V \pm 10\%$; and 59X for 0°C to 75°C temperature range and $V_{CC} = 5\ V \pm 5\%$.
To order the 4600 Design Kit, specify A6A4600KTX. For the 4700 Design Kit, specify A6A4700KTX.

PHYSICAL DIMENSIONS
TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline



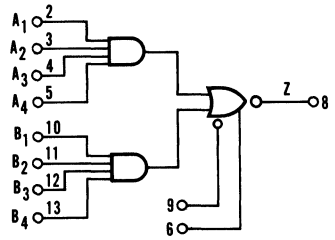
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

CIRCUIT SCHEMATIC



TYPICAL RESISTOR VALUES
$R_1 = R_2 = 4\ K\Omega$
$R_3 = R_4 = 1.5\ K\Omega$

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND
PIN 1 = NOT USED

Logic Equation: $Z = \overline{A_1A_2A_3A_4 + B_1B_2B_3B_4 + \ldots}$ *
* More terms are provided with OR extension

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TTL MICROMATRIX™ ARRAY INTERNAL QUARTER-CELL 4601

ELECTRICAL CHARACTERISTICS:

Temperature Range: 0°C to +75°C
Supply Voltage Range: 5 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage	2.3		2.3	2.8		2.3		V	$V_{CC} = 4.75$ V, $I_{OH} = -600\ \mu A$ V_{IL} On Inputs	
V_{OL}	Output Low Voltage Internal Loading		0.6		0.42	0.6		0.6	V	$V_{CC} = 5.25$ V, $I_{OL} = 10.7$ mA $V_{CC} = 4.75$ V, $I_{OL} = 9.3$ mA	
	Output Low Voltage External CCSL Loading		0.4		0.3	0.4		0.4	V	$V_{CC} = 5.25$ V, $I_{OL} = 7.3$ mA $V_{CC} = 4.75$ V, $I_{OL} = 6.4$ mA	
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed Input High Threshold For All Inputs	
V_{IL}	Input Low Voltage		0.8			0.8		0.8	V	Guaranteed Input Low Threshold For All Inputs	
I_F	Input Load Current Internal V_F Level		−1.52		−1.00	−1.52		−1.52	mA	$V_{CC} = 5.25$ V	$V_F = 0.6$ V
			−1.33		−0.87	−1.33		−1.33	mA	$V_{CC} = 4.75$ V	
	Input Load Current External CCSL V_F Level		−1.60		−1.08	−1.60		−1.60	mA	$V_{CC} = 5.25$ V	$V_F = 0.45$ V
			−1.41		−0.91	−1.41		−1.41	mA	$V_{CC} = 4.75$ V	
I_R	Input Leakage Current				5.0	60		60	μA	$V_{CC} = 5.25$ V, $V_R = 4.5$ V	
P_D	Power Dissipation				21	30			mW	Inputs Open	$V_{CC} = 5.0$ V
					11	16			mW	Inputs Grounded	

ELECTRICAL CHARACTERISTICS:

Temperature Range: −55°C to +125°C
Supply Voltage Range: 5 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage	2.3		2.3	2.55		2.3		V	$V_{CC} = 4.5$ V, $I_{OH} = -600\ \mu A$ V_{IL} On Inputs	
V_{OL}	Output Low Voltage Internal Loading		0.55		0.42	0.55		0.55	V	$V_{CC} = 5.5$ V, $I_{OL} = 10.7$ mA $V_{CC} = 4.5$ V, $I_{OL} = 8.2$ mA	
	Output Low Voltage External CCSL Loading		0.4		0.3	0.4		0.4	V	$V_{CC} = 5.5$ V, $I_{OL} = 7.3$ mA $V_{CC} = 4.5$ V, $I_{OL} = 5.6$ mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		V	Guaranteed Input High Threshold For All Inputs	
V_{IL}	Input Low Voltage		0.8			0.8		0.7	V	Guaranteed Input Low Threshold For All Inputs	
I_F	Input Load Current Internal V_F Level		−1.52		−1.04	−1.52		−1.52	mA	$V_{CC} = 5.5$ V	$V_F = 0.55$ V
			−1.17		−0.8	−1.17		−1.17	mA	$V_{CC} = 4.5$ V	
	Input Load Current External CCSL V_F Level		−1.60		−1.1	−1.60		−1.60	mA	$V_{CC} = 5.5$ V	$V_F = 0.4$ V
			−1.24		−0.85	−1.24		−1.24	mA	$V_{CC} = 4.5$ V	
I_R	Input Leakage Current				5.0	60		60	μA	$V_{CC} = 5.5$ V, $V_R = 4.5$ V	
P_D	Power Dissipation				21	30			mW	Inputs Open	$V_{CC} = 5.0$ V
					11	16			mW	Inputs Grounded	

LOADING RULES

FAN-OUT (See table):

The internal or "on-chip" fan-out of the 4601 is specified with reduced noise margins since on-chip noise is low. If the 4601 is used specifically for off-chip driving, the maximum fan-out must be reduced to maintain CCSL noise margins.

EXTENSION:

Extension at the 4601 OR extender pins 9 and 6 may be accomplished with TTμL 9006 dual 4 input extender elements. A maximum of 10 extenders (5-9006's) may be tied to the 4601 pins. (See Fig. 1)

WIRED "AND":

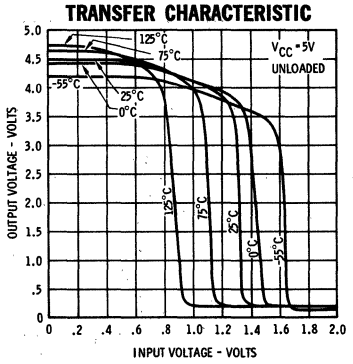
Since the 4601 internal gates have resistive pull-ups, the AND tie of outputs is allowed. (See Fig. 4). Breadboarding of the combined outputs is:
FAN-OUT=7 − (3) (number of outputs tied together − 1)
For "on array" usage optional pull-up resistors allow fan-out as summarized below:

FAN-OUT TABLE

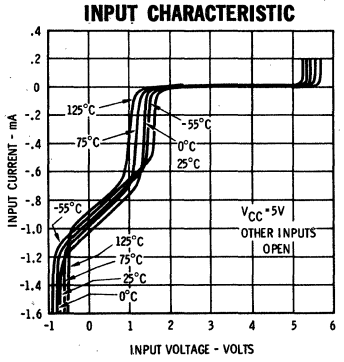
LOADING TYPE	FAN-OUT
INTERNAL	7
TTμL	4.5
DTμL	4.5
LPDTμL	45

TYPICAL INPUT-OUTPUT CHARACTERISTICS

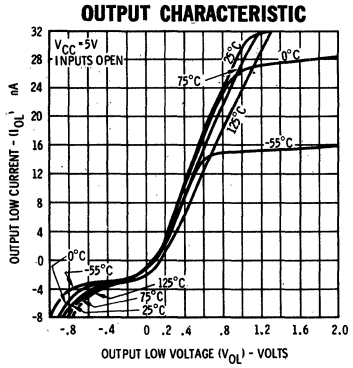
TRANSFER CHARACTERISTIC



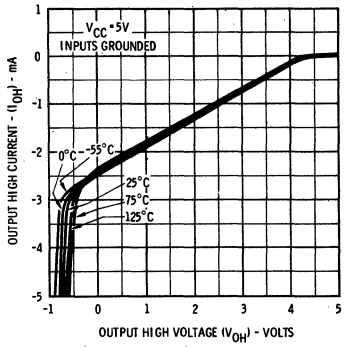
INPUT CHARACTERISTIC



LOW LEVEL OUTPUT CHARACTERISTIC



HIGH LEVEL OUTPUT CHARACTERISTIC



TYPICAL APPLICATIONS

EIGHT INPUT DIGITAL MULTIPLEXER USING "OR" EXTENSION

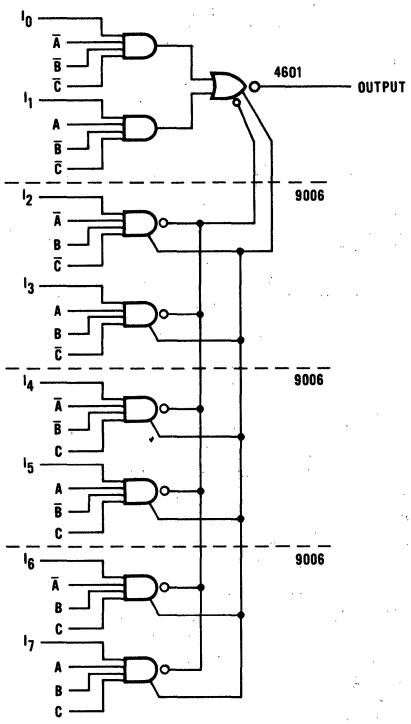


Fig. 1

Three bit address A B C selects an input (I_0, I_1 . . . I_7) which is presented at the output in inverted form. The 4601 is OR-expanded using 3-9006 extender elements.

GATED LATCH USING TWO 4601

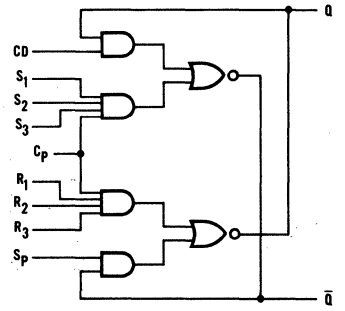
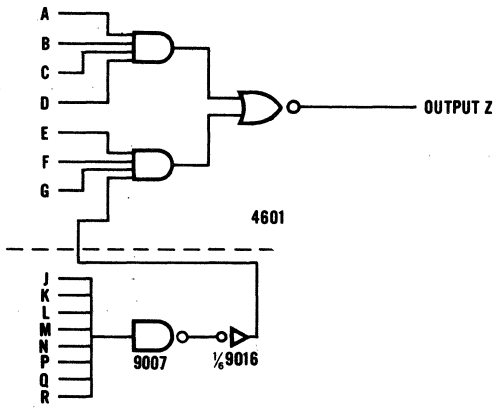


Fig. 2

APPLICATIONS (continued)

INPUT "AND" EXPANSION

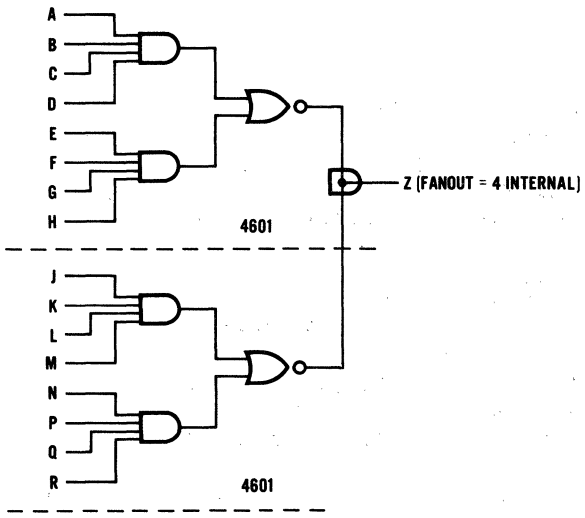


$\overline{Z = ABCD + EFGJKLMNPQR}$

Standard TTμL gates may be used for expansion of "AND" inputs.

*Provision for "AND" expansion is made on the micromatrix array thru "selective bar" options.

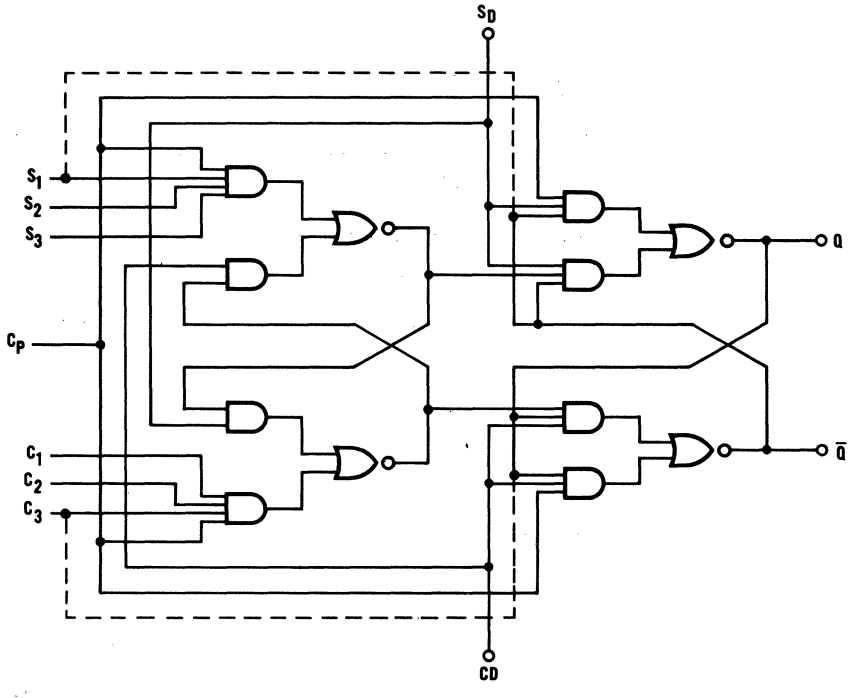
WIRED "AND"



$Z = \overline{[ABCD + EFGH]} \cdot \overline{[JKLM + NPQR]}$

Fig. 4

GENERAL PURPOSE MASTER-SLAVE FLIP-FLOP USING FOUR 4601



For J-K operation, connect as shown in dotted lines. The outputs change on the high to low clock transition.

Fig. 5

4610

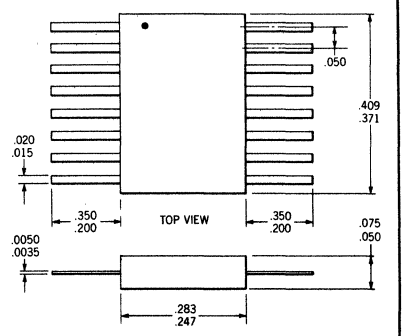
DUAL TWO-VARIABLE FUNCTION GENERATOR

TTL MICROMATRIX™ ARRAY CIRCUIT

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION—The 4610 is a Dual Two-Variable Function Generator useful for non-arithmetic operations and variable decision making control in central processor units. Each circuit, controlled by a common 4-bit word, can select one of 16 possible Boolean functions performed on the two variable inputs. An alternate input select configuration increases circuit flexibility and allows simultaneous generation of two separate output functions from a single pair of variables. **The circuit is produced with two layer metal interconnection using the Fairchild 4600 TTL Micromatrix™ Array.**

FLAT PACKAGE



FEATURES

- **EXPANDABLE IN GROUPS OF 2 BITS**
- **MEMBER OF 4600 MICROMATRIX ARRAY FAMILY**
- **CCSL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" 16-PIN FLAT PACK**
- **TWO LAYER METAL INTERCONNECTIONS**
- **SIMULTANEOUS FUNCTIONS OF 1 PAIR OF VARIABLES**

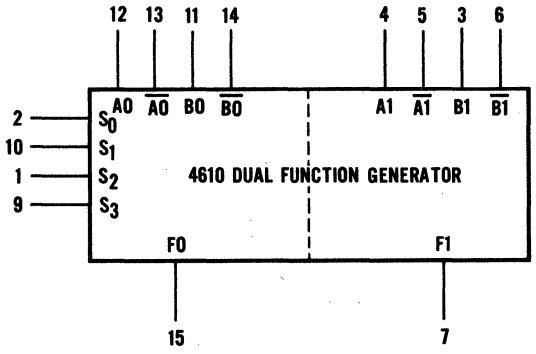
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Case) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs (Output high)	Gnd to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into Output (Output low)	+30 mA

Note 1—either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify A3L46105XX for Flat package, where 51X is for −55°C to +125°C (Case) temperature range or 59X for the 0°C to +75°C (Case) temperature range.

FIG. 1 — 4610 DUAL TWO-VARIABLE FUNCTION GENERATOR



Pin 16 = V_{CC}
Pin 8 = Gnd

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4			2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.45			0.45		0.45	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 12.8\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 9.92\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		.75	Volts	Guaranteed input low threshold for all inputs
I_F (See Loading Rules Note 1)	Input Load Current		−1.60		−1.1	−1.60		−1.60	mA	$V_{CC} = 5.5\ V$ $V_F = 0.45\ V$
	One Low Level Unit Load		−1.24		−0.85	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R (See Loading Rules Note 2)	Input Leakage Current				5.0	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
P_D	Power Dissipation				375	500			mW	$V_{CC} = 5.0\ V$, Inputs open
t_{I2}	Avg. Propagation Delay				20				ns	$V_{CC} = 5.0\ V$ $C_L = 20\ pf$, $R_L = 1\ k$

ELECTRICAL CHARACTERISTICS ($T_C = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Q Output High Voltage	2.4		2.4			2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.45			0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 12.8\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 11.3\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (See Loading Rules Note 1)	Input Load Current		−1.60		−1.08	−1.60		−1.60	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
	One Low Level Unit Load		−1.41		−0.91	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$
I_R (See Loading Rules Note 2)	Input Leakage Current					60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
P_D	Power Dissipation				375	500			mW	$V_{CC} = 5.0\ V$, Inputs open
t_{I2}	Avg. Propagation Delay				20				ns	$V_{CC} = 5.0\ V$ $C_L = 20\ pf$, $R_L = 1\ k$

FUNCTION GENERATOR DESCRIPTION

A detailed logic representation of the common control (S_0, S_1, S_2, S_3) and one of the two output function blocks is shown in Figure 2. The Truth Table implemented by the function generator shows the functions of input variables A and B with the 16 possible combinations of S_0, S_1, S_2, and S_3 (refer to Table 1). Note that any desired output function may be chosen active level high or active level low.

FUNCTION GENERATOR TRUTH TABLE WITH INPUT VARIABLES ACTIVE HIGH

S_0	S_1	S_2	S_3	FUNCTION (ACTIVE LOW)	FUNCTION (ACTIVE HIGH)
L	L	L	L	$A + B$	$\overline{A} \cdot \overline{B}$
L	H	L	L	$A + \overline{B}$	$\overline{A} \cdot B$
H	L	L	L	$\overline{A} + B$	$A \cdot \overline{B}$
H	H	L	L	$\overline{A} + \overline{B}$	$A \cdot B$
L	L	L	H	$\overline{A} \cdot \overline{B}$	$A + B$
L	H	L	H	$\overline{A} \cdot B$	$A + \overline{B}$
H	L	L	H	$A \cdot \overline{B}$	$\overline{A} + B$
H	H	L	H	$A \cdot B$	$\overline{A} + \overline{B}$
L	L	H	L	$A \oplus B$	$A \oplus \overline{B}$
L	H	H	L	$A \oplus \overline{B}$	$A \oplus B$
H	L	H	L	1	0
H	H	H	L	0	1
L	L	H	H	A	$\overline{A}$
L	H	H	H	B	$\overline{B}$
H	L	H	H	$\overline{A}$	A
H	H	H	H	$\overline{B}$	B

TABLE 1

DETAILED LOGIC DIAGRAM

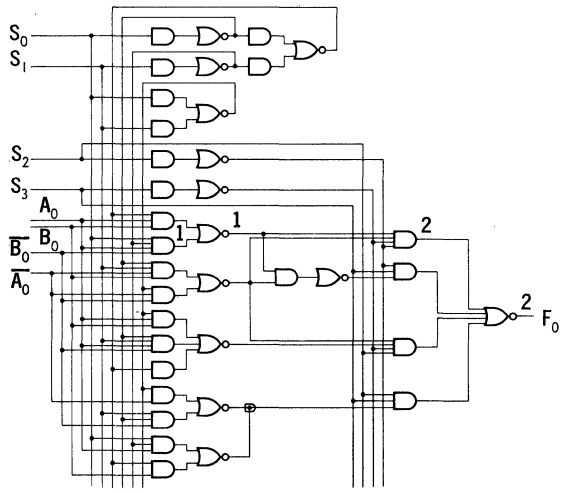


FIG. 2

Circuit flexibility can be increased by using S_2, S_3, A and B inputs as controls and S_0, S_1 as the input variables. In this mode of operation two separate output functions are performed simultaneously on a single pair of variables S_0 and S_1. Refer to Table 2 below for complete truth table.

For example, if it is desired to obtain the active high functions $\overline{S}_0 \cdot S_1$ and $S_0 \cdot \overline{S}_1$ simultaneously, S_2, S_3 are set low, A_0 low, B_0 high, A_1 high, and B_1 low. The function $\overline{S}_0 \cdot S_1$ will appear at the F_0 output; likewise function $S_0 \cdot \overline{S}_1$ will appear at the F_1 output.

FUNCTION GENERATOR TRUTH TABLE WITH INPUT VARIABLES ACTIVE HIGH WHERE A, B, S_2, S_3 ARE USED AS CONTROL INPUTS AND S_0, S_1 ARE INPUT VARIABLES ON WHICH THE FUNCTIONS ARE PERFORMED.

S_2	S_3	A	B	FUNCTION (ACTIVE LOW)	FUNCTION (ACTIVE HIGH)
L	L	L	L	$S_0 + S_1$	$\overline{S}_0 \cdot \overline{S}_1$
L	L	L	H	$S_0 + \overline{S}_1$	$\overline{S}_0 \cdot S_1$
L	L	H	L	$\overline{S}_0 + S_1$	$S_0 \cdot \overline{S}_1$
L	L	H	H	$\overline{S}_0 + \overline{S}_1$	$S_0 \cdot S_1$
L	H	L	L	$\overline{S}_0 \cdot \overline{S}_1$	$S_0 + S_1$
L	H	L	H	$\overline{S}_0 \cdot S_1$	$S_0 + \overline{S}_1$
L	H	H	L	$S_0 \cdot \overline{S}_1$	$\overline{S}_0 + S_1$
L	H	H	H	$S_0 \cdot S_1$	$\overline{S}_0 + \overline{S}_1$
H	L	L	L	$S_0 \oplus S_1$	$S_0 \oplus \overline{S}_1$
H	L	L	H	$\overline{S}_1$	S_1
H	L	H	L	$\overline{S}_1$	S_1
H	L	H	H	$S_0 \oplus S_1$	$S_0 \oplus \overline{S}_1$
H	H	L	L	S_0	$\overline{S}_0$
H	H	L	H	$S_0 \oplus S_1$	$S_0 \oplus \overline{S}_1$
H	H	H	L	$S_0 \oplus \overline{S}_1$	$S_0 \oplus S_1$
H	H	H	H	$\overline{S}_0$	S_0

TABLE 2

Note that by varying control lines S_2, S_3, A and B that any pair of S_0 and S_1 min terms, max terms, or symmetric function can be generated.

LOADING RULES

Input Loading Rules (Fan-in)

1. I_F is defined as one low level unit load. The multipliers to determine low level unit loads for individual inputs are:

INPUT	MULTIPLIER
S_1	8
S_0	6
S_2, S_3	5
A_0, A_1, B_0, B_1, $\overline{B_0}$, $\overline{B_1}$	4
$\overline{A_0}$, $\overline{A_1}$	3

2. I_R is defined as one unit high level load. The multipliers to determine high level unit loads for individual inputs are:

INPUT	MULTIPLIER
S_1	8
S_0	6
A_0, A_1, S_2, S_3	5
$\overline{B_0}$, $\overline{B_1}$, B_0, B_1	4
$\overline{A_0}$, $\overline{A_1}$	3

FAN OUT

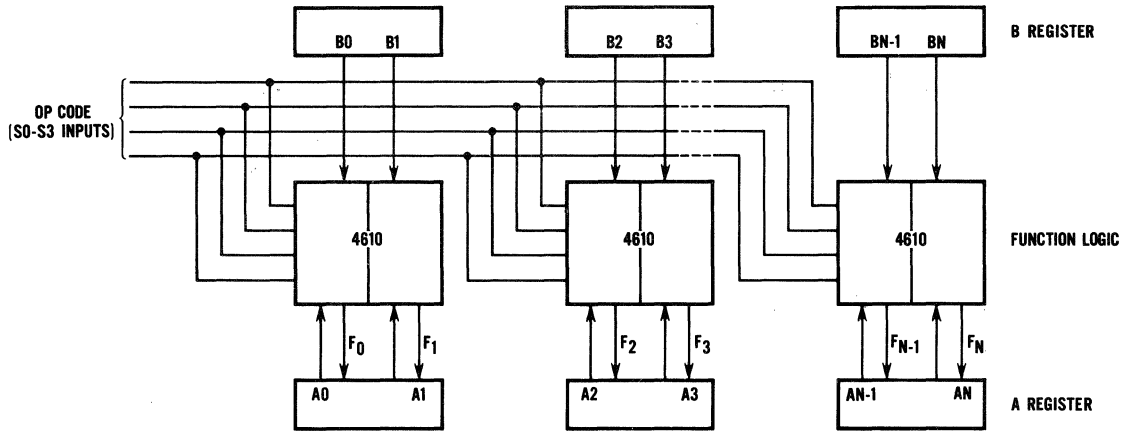
	LEVEL	
OUTPUT	HIGH	LOW
F_0	20	8
F_1	20	8

APPLICATIONS

A Typical Processor Application is the transfer and logical operation control between two registers (A and B). The function generators are controlled by a 4-bit operation code field, S_0, S_1, S_2, and S_3. The operation code repertoire includes the 16 operations listed below.

AND $\overline{A}$ and $\overline{B}$ to A	OR A and B to A
AND $\overline{A}$ and B to A	OR A and $\overline{B}$ to A
AND A and $\overline{B}$ to A	OR $\overline{A}$ and B to A
AND A and B to A	OR $\overline{A}$ and $\overline{B}$ to A
Exclusive OR A and $\overline{B}$ to A	Complement A
Exclusive OR A and B to A	Transfer $\overline{B}$ to A
Reset A	No Operation
Set A	Transfer B to A

FIG. 3



COMPATIBLE CURRENT SINKING LOGIC COMING SOON

Type	Function	Type	Function
9315	One-of-Ten Decoder/Driver	9322	Quad 2-Input Digital Multiplexer
9317	Seven Segment Display Decoder/Driver	9602	Dual Retriggerable/Non-retriggerable One-Shot
9318	Priority 8-Input Encoder	9614	Dual Differential Line Driver
9320	Up/Down BCD Decade Synchronous Counter	9615	Dual Differential Line Receiver
9324	Expandable 5-Bit Comparator	9642	Dual 3-Input NAND High Current, High Voltage Driver
9326	Up/Down Binary Hexidecimal Synchronous Counter	9644	Dual 4-Input NAND High Current, High Voltage Buffer
9338	8-Bit Multi-Access Memory		

9315—One-of-Ten Decoder/Driver designed to accept 8421 BCD inputs and directly drive Nixie* readouts.

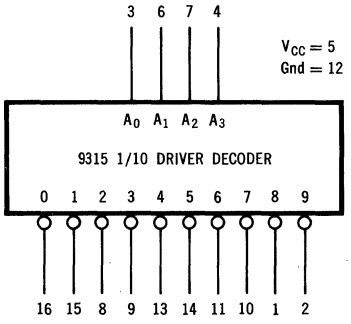
Propagation delay: 250 nsec
Power dissipation: 100 mW
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
A_0, A_1, A_2, A_3	1 UL	12/10

Outputs: 55V on any output, sufficient to drive gas filled readout tubes directly.

*Registered trademark of Burroughs Corp.



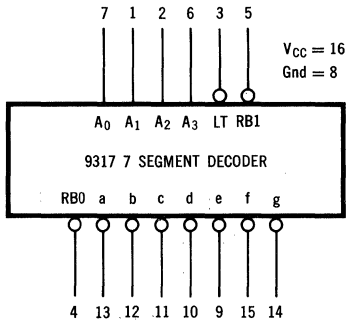
9317—Seven Segment Display Decoder/Driver with over-riding lamp test input and capability for providing automatic blanking of insignificant zeroes in multi-digit displays.

Propagation delay: 200 nsec
Power dissipation: 260 mW
Package: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
A_0, A_1, A_2, A_3	1 UL	2/9.5
LT	4 UL	10/40
RBI	½ UL	2/4.8
RBO	1.5 UL	14/19
Outputs	12 UL	*/120

*Uncommitted Collector Outputs: 30V on any output.

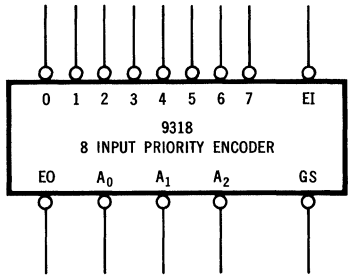


9318—Priority 8-Input Encoder with an input enable and group signal and all zero outputs for expanding to larger input words.

Propagation delay: 25 nsec
Power dissipation: 150 mW
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
All Inputs	1 UL	12/10
All Outputs	10 UL	240/100

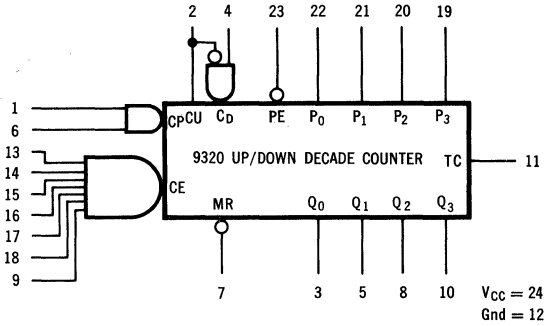


9320—Up/Down BCD Decade Synchronous Counter with parallel presetting synchronous inputs, over-riding master reset, two line up/down control, 2-input clock and carry look-ahead logic for multi-decade operation.

Propagation delay: 20 nsec
Power dissipation: 360 mW
Packages: 3M (Flat) & 6N (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
CD, CE, MR	1 UL	12/10
P_0, P_1, P_2, P_3	⅔ UL	8/6.7
PE, CP, CU	2 UL	24/20
Outputs	6 UL	72/60



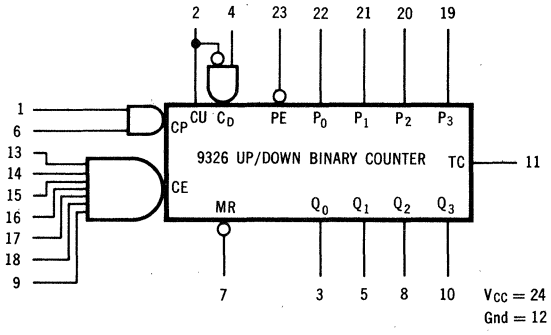
COMPATIBLE CURRENT SINKING LOGIC COMING SOON

9326—Up/Down Binary Hexidecimal Synchronous Counter with parallel presetting synchronous inputs, over-riding master reset, two line up/down control, 2-input clock and carry look-ahead logic for multi-decade operation.

Propagation delay: 20 nsec
Power dissipation: 360 mW
Packages: 3M (Flat) & 6N (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
CD, CE, MR	1 UL	12/10
P_0, P_1, P_2, P_3	⅔ UL	8/6.7
PE, CP, CU	2 UL	24/20
Outputs	6 UL	72/60

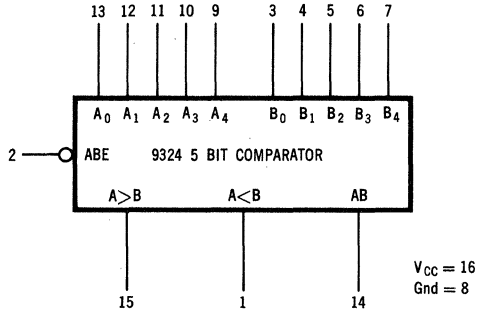


9324—Expandable 5-Bit Comparator with A = B, A > B, A < B outputs. An enable input is also provided for the A and B outputs.

Propagation delay: 15 nsec
Power dissipation: 120 mW
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
All A & B Inputs	1 UL	12/10
ABE	2 UL	24/20
AB & C Outputs	10 UL	240/100

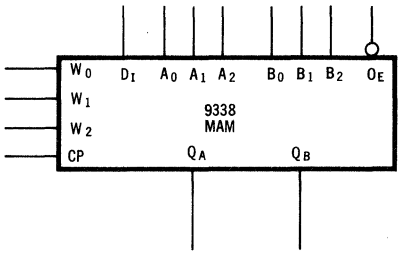


9338—8-Bit Multi-Access Memory (MAM) organized like a master-slave flip-flop that has eight masters and two slaves. The data input (D_I) is connected to the input of the master selected by the write select (W_X) inputs synchronously with the clock pulse (C_P). The two independent outputs are addressed by the read select (A_X & B_X) inputs. The two outputs (Q_A & Q_B) can be read independent of the clock pulse when the output enable (O_E) is low.

Propagation read delay: 35 nsec
Propagation write delay: 35 nsec
Power dissipation: 370 mW
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
All Inputs	1 UL	12/10
Q_A & Q_B	6 UL	

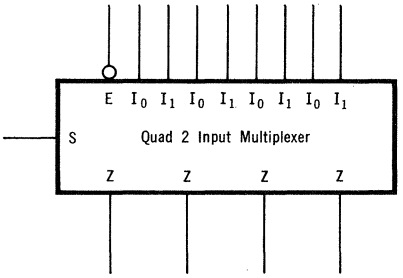


9322—Quad 2-Input Digital Multiplexer with input enabling and single line control input.

Propagation delay: 25 nsec
Power dissipation: 150 mW
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
All Inputs	1 UL	12/10
All Outputs	10 UL	240/100

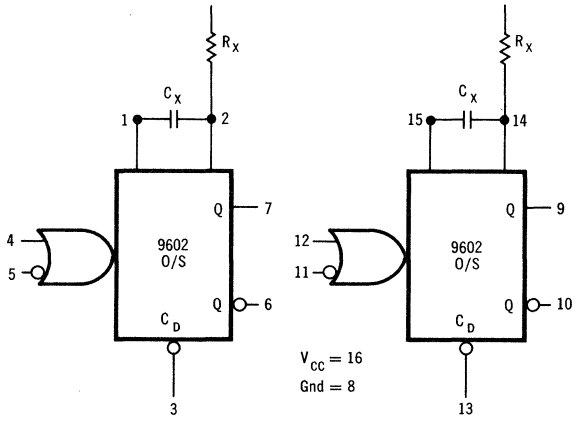


9602—Dual Retriggerable/Non-retriggerable One-Shot, each with two DC level-sensitive inputs, one is active-level High and one is active-level Low. They also have over-riding reset inputs.

Propagation delay: 25 nsec
Power dissipation: 87 mW/function
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
Inputs	1 UL	12/10
Outputs	6 UL	144/63



COMPATIBLE CURRENT SINKING LOGIC COMING SOON

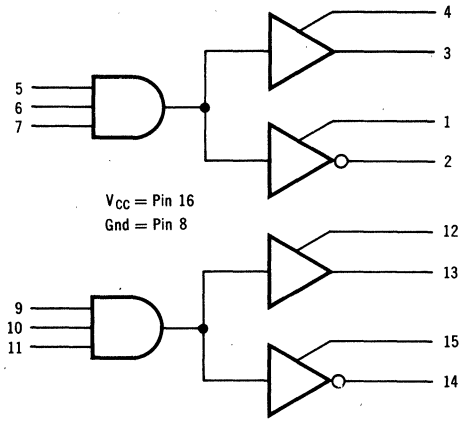
9614—Dual Differential Line Driver with short-circuit and diode protected outputs, input diode clamps and operates from a single 5V supply. It is designed to be used with the 9615 Line Receiver.

Propagation delay: 10 nsec
Power dissipation: 110 mW
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
All Inputs	1 UL	2/10
Differential Outputs (V_{OH} = 2.5 V, V_{OL} = 0.5 V)	I_{OH} = 40 mA I_{OL} = 40 mA	

Supply Voltage: V_{CC} = 5 V



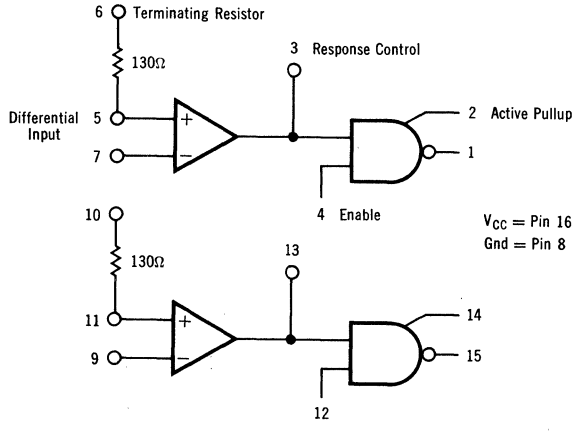
9615—Dual Differential Line Receiver can sense 80 mV differential signals on ±15 volt common mode. The 9615 is designed to operate with the 9614 Line Driver at speeds up to 20 MHz.

Propagation delay: 20 nsec
Power dissipation: 100 mW
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
Differential Inputs	80 mV	threshold
Gate Inputs	1 UL	2/10
Output	6 UL	100/62.5

Supply Voltage: V_{CC} = 5 V



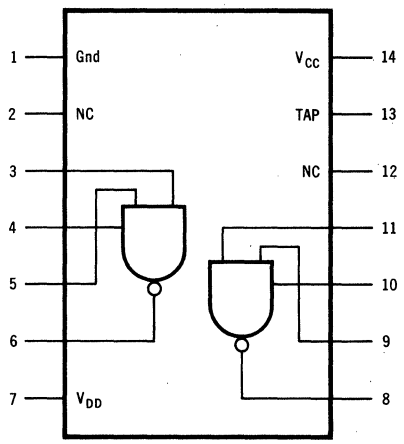
9642—Dual 3-Input NAND High-Current, High-Voltage Driver with expander inputs, designed to drive core, thin film, and plated-wire memories. Either gate can be used to source or sink up to 500 mA.

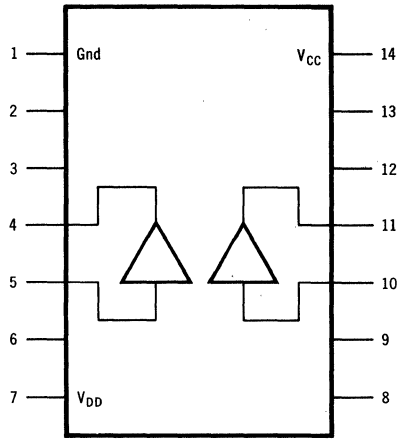
Propagation delay: 35 nsec
Power dissipation: 470 mW/driver gate
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
Gate Inputs	1 UL	2/9.4
Expander Inputs	1 UL	*/9.4
Outputs High	500 mA	
Outputs Low	500 mA	

*A function of input diodes used.





COMPATIBLE CURRENT SINKING LOGIC COMING SOON

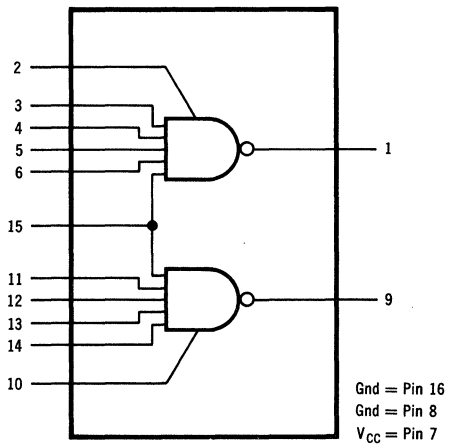
9644—Dual 4-Input NAND High-Current, High-Voltage Buffer with expander inputs and a common enable input. It is to sink up to 500 mA and hold-off up to 30 volts.

Propagation delay: 35 nsec
Power dissipation: 450 mW/buffer gate
Packages: 3L (Flat) & 6B (DIP)

Loading:

Inputs/Outputs	INTRA	CCSL
Common Gate Input	2 UL	4/19
Gate Inputs	1 UL	2/9.4
Expander Inputs	1 UL	*/9.4
Outputs	312 UL	Open collector, sinks 500 mA

*A function of input diodes used.



Special Integrated Circuits

SPECIAL CIRCUITS NUMERICAL INDEX

SPECIAL CIRCUITS CROSS REFERENCE

NOTE: The Special Circuits Cross Reference included in CCSL Cross Reference, page 3-ii.

9620

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9620 is a dual differential line receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed CCSL logic to the output. In addition to line reception the 9620 can perform many functions, a few of which are presented in the applications section. It can interface with nearly all input logic levels including CML, CTμL, HLLDTμL, RTμL and CCSL. HLLDTμL logic can be provided by tieing the output to V_{CC2}(+12 V) through a resistor. The outputs can also be wire OR'ed. The 9620 offers the advantages of logic compatible voltages (+5 V, +12 V), CCSL output characteristics, and a flexible input array with a high common mode range. The direct inputs are provided in addition to the attenuated inputs (normally used) to allow the input attenuation and response time to be changed by use of external components.

FEATURES:

- **CCSL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **WIRED-OR CAPABILITY**
- **DIRECT INPUTS (A_D, B_D)**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

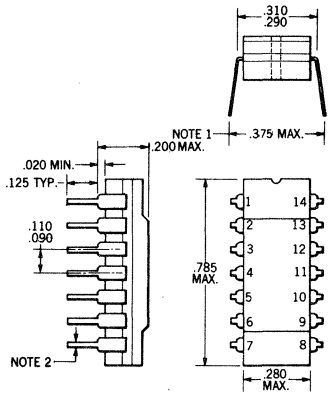
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V
Voltage Applied to Outputs for High Output State	−0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V

ORDER INFORMATION

Specify U6A9620XXX for 14 pin Dual In-Line package or U3I9620XXX for 14 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

TYPICAL DUAL IN-LINE PACKAGE

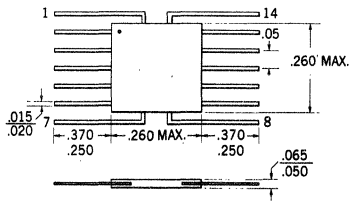
In Accordance With
JEDEC (TO-116) Outline



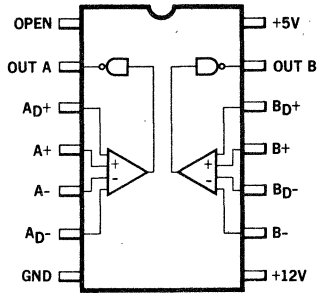
NOTES:

1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

14-PIN FLAT PACKAGE



LOGIC DIAGRAM



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

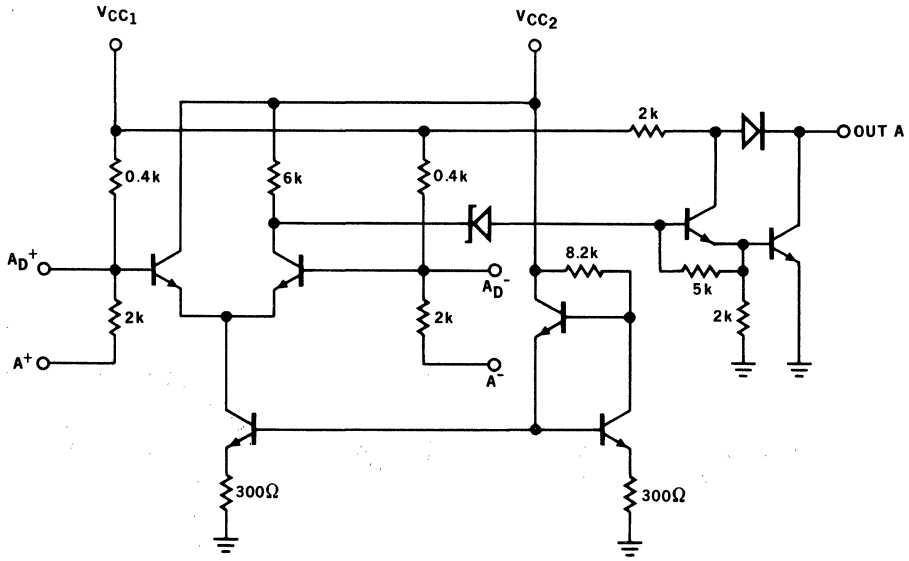
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (Temperature Range −55°C to +125°C, $V_{CC1} = 5.0\ V \pm 10\%$, $V_{CC2} = 12.0\ V \pm 10\%$)

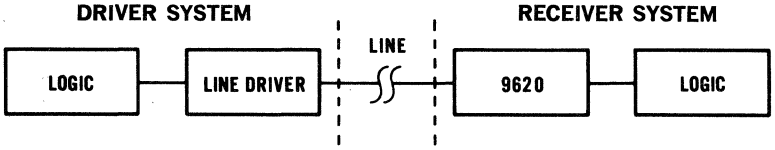
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.40		0.25	0.40		0.45	Volts	$V_{CC1} = 4.5\ V$ $I_{OL} = 15.0\ mA$	$V_{CC2} = 10.8\ V$ $*V_{DIFF} = 0.5\ V$
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		Volts	$V_{CC1} = 4.5\ V$ $I_{OH} = -0.2\ mA$	$V_{CC2} = 10.8\ V$ $*V_{DIFF} = -0.5\ V$
I_{CEX}	Output Leakage Current		50			100		200	μA	$V_{CEX} = 13.2\ V$	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
†V_{TH}	Differential Input Threshold Voltage		500		120	500		500	mV	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
†V_{CM}	Common Mode Voltage	−15	15	−15	±17.5	15	−15	15	Volts	$V_{CC1} = 5.0\ V$ $*V_{DIFF} = 2.0\ V$	$V_{CC2} = 12.0\ V$
I_{VCC1}	5 V Supply Current		13		8.2	13		13	mA	$V_{CC1} = 5.5\ V$ $V_{CC2} = 13.2\ V$	+Input = 5.5 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.0		5.6	8.0		8.0	mA	$V_{CC1} = 5.5\ V$ $V_{CC2} = 13.2\ V$	+Input = 5.5 V −Input = 0 V
t_{pd+}	Turn-off Time				35	50			ns	$R_L = 3.9\ k\Omega$	$C_L = 30\ pF$
t_{pd-}	Turn-on Time				20	50			ns	$R_L = 390\ \Omega$	$C_L = 30\ pF$

†All input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

Fig. 1 — SCHEMATIC DIAGRAM



STANDARD USAGE

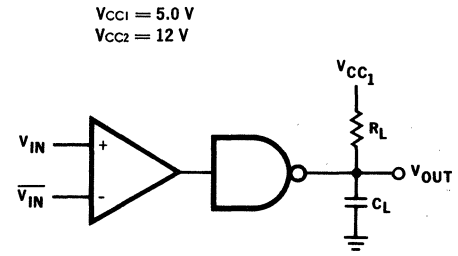


ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, $V_{CC1} = 5.0\ V \pm 5\%$, $V_{CC2} = 12.0\ V \pm 5\%$)

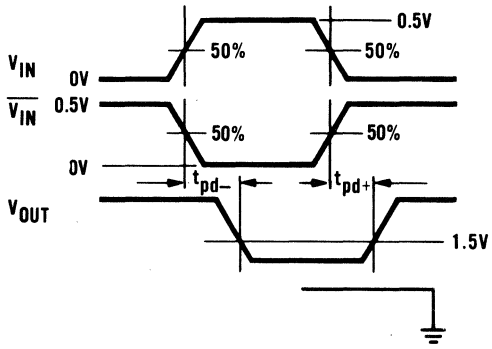
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.50	Volts	$V_{CC1} = 4.75\ V$ $I_{OL} = 15.0\ mA$	$V_{CC2} = 11.4\ V$ $*V_{DIFF} = 0.5\ V$
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		Volts	$V_{CC1} = 4.75\ V$ $I_{OH} = -0.2\ mA$	$V_{CC2} = 12.6\ V$ $*V_{DIFF} = -0.5\ V$
I_{CEX}	Output Leakage Current		50			100		200	μA	$V_{CEX} = 5.25\ V$	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
$\dagger V_{TH}$	Differential Input Threshold Voltage		500		120	500		500	mV	$V_{CC1} = 4.75\ V$	$V_{CC2} = 12.6\ V$
$\dagger V_{CM}$	Common Mode Voltage	−12	12	−12	±17.5	12	−12	12	Volts	$V_{CC1} = 5.0\ V$ $*V_{DIFF} = 2.0\ V$	 $V_{CC2} = 12.0\ V$
I_{VCC1}	5 V Supply Current		13.5		8.2	13.5		13.5	mA	$V_{CC1} = 5.25\ V$ $V_{CC2} = 12.6\ V$	+Input = 5.25 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.5		5.6	8.5		8.5	mA	$V_{CC1} = 5.25\ V$ $V_{CC2} = 12.6\ V$	+Input = 5.25 V −Input = 0 V
t_{pd+}	Turn-off Time				35	75			ns	$R_L = 3.9\ k\Omega$	$C_L = 30\ pF$
t_{pd-}	Turn-on Time				20	75			ns	$R_L = 390\ \Omega$	$C_L = 30\ pF$

†All input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

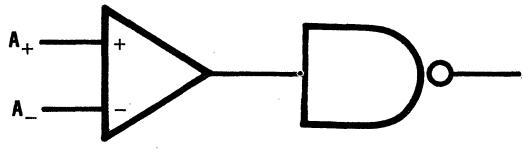
Fig. 2 — SWITCHING TIME TEST CIRCUIT

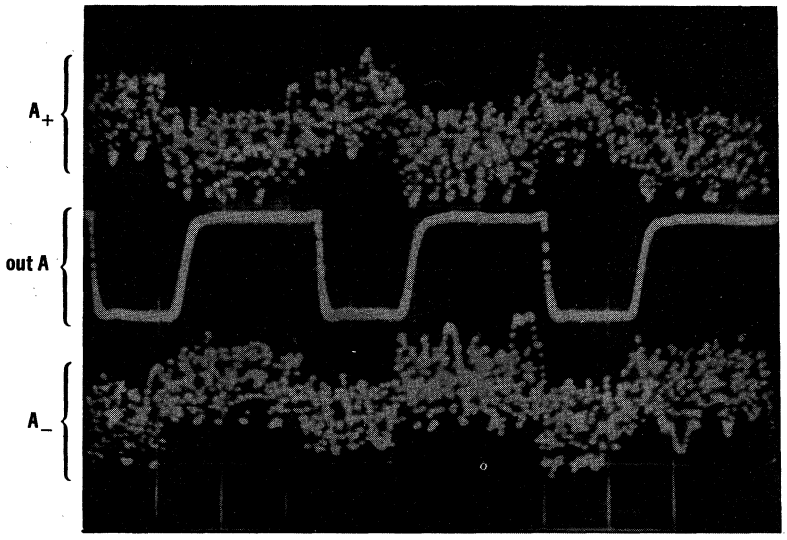


WAVEFORMS



Photograph of a 9620 switching differential data in the presence of high common mode noise.

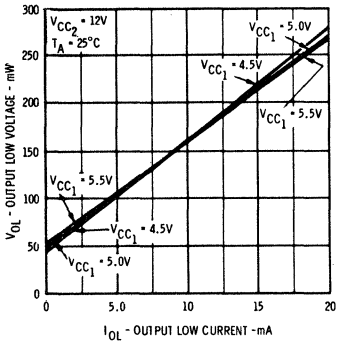




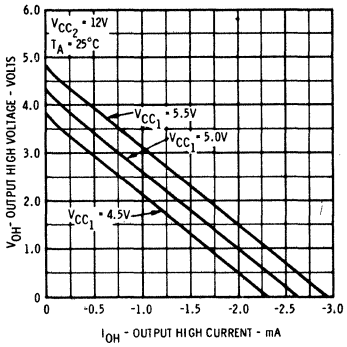
VERT = 2.0 V/div. HORIZ = 50 ns/div.

TYPICAL ELECTRICAL CHARACTERISTICS

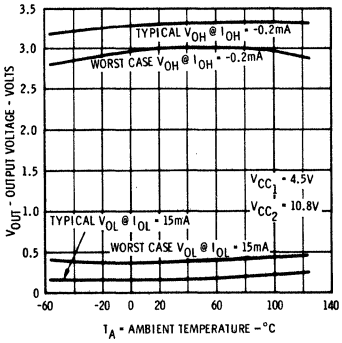
TYPICAL OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



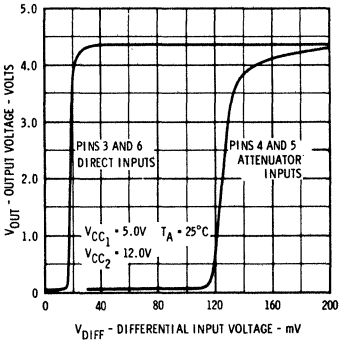
TYPICAL OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



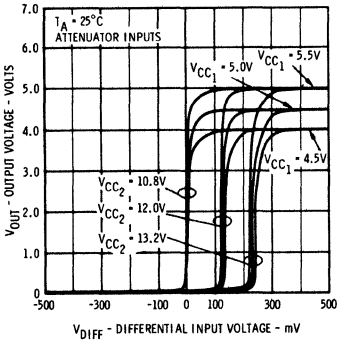
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



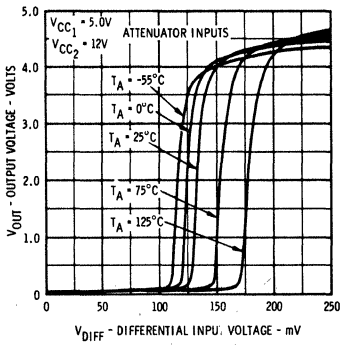
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



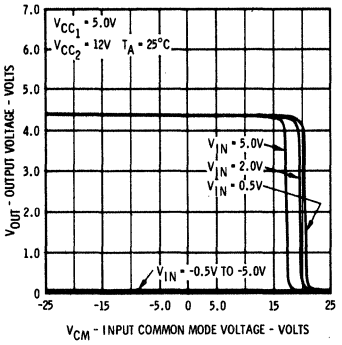
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



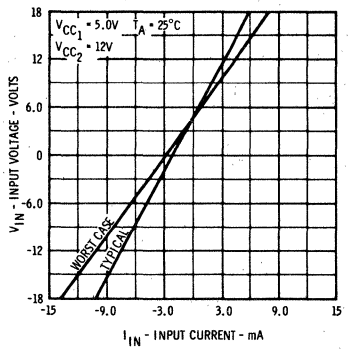
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



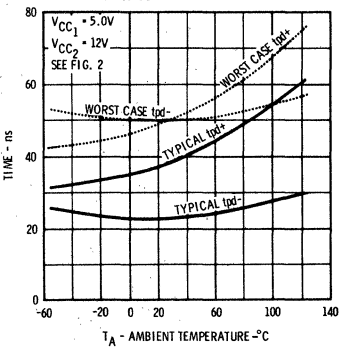
TYPICAL V_{out} VERSUS V_{CM} CHARACTERISTICS



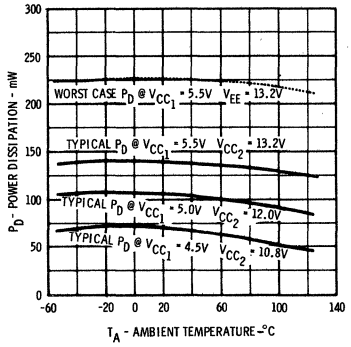
INPUT VOLTAGE VERSUS INPUT CURRENT



SWITCHING TIME VERSUS AMBIENT TEMPERATURE

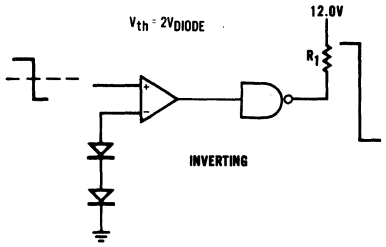


POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



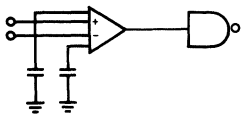
APPLICATIONS

DIGITAL COMPARATOR WITH DIODE REFERENCE AND HIGH LEVEL LOGIC OUT

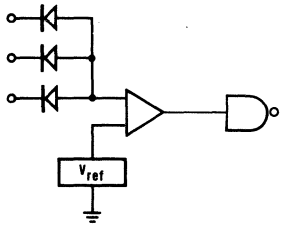


$R_1 \geq 750\ \Omega$

DIGITAL DIFFERENTIAL LINE RECEIVER WITH INPUTS ROLLED OFF

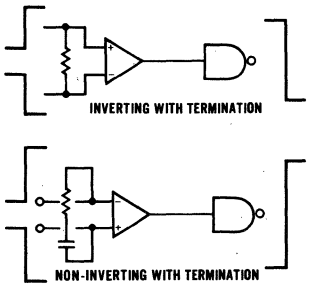


EXPANDED INTERFACE

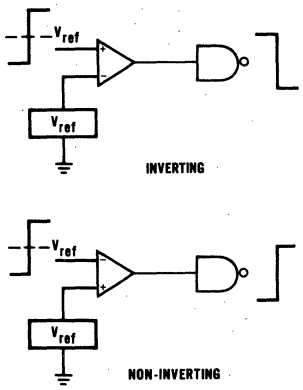


V_{ref} = Resistor, Diodes, or Supply

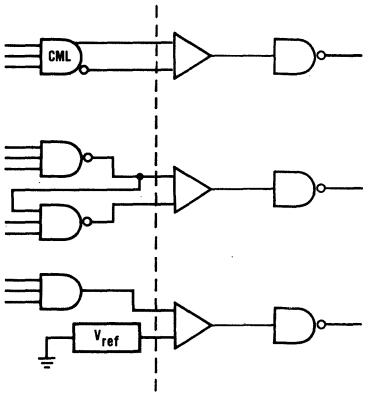
DIGITAL DIFFERENTIAL AMPLIFIER (Line Receiver)



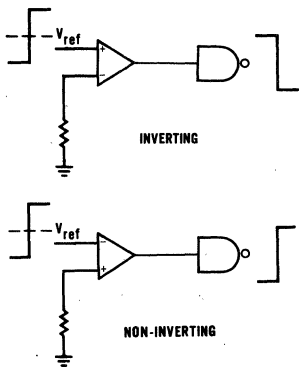
DIGITAL COMPARATOR



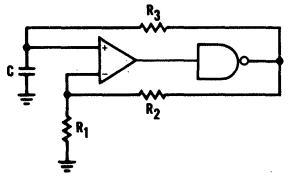
INTERFACING METHODS



DIGITAL COMPARATOR WITH RESISTIVE DIVIDER AS REFERENCE

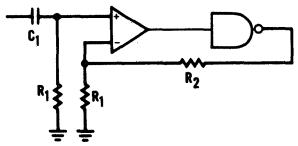


MULTIVIBRATOR



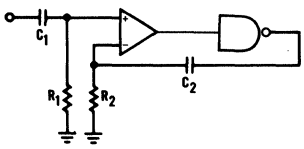
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $T = 1.3\ R_3C$

A.C. COUPLED DIGITAL AMPLIFIER WITH HYSTERESIS



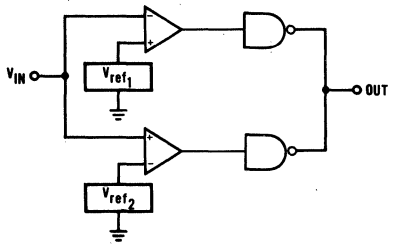
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$

MONOSTABLE MULTIVIBRATOR NEGATIVE EDGE TRIGGERING



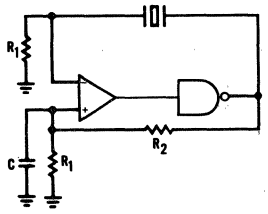
TYPICALLY
$C_1 = 0.1\ \mu F$, $R_1 = 1.2\ k\Omega$, $R_2 = 1.0\ k\Omega$
Pulse Width = 50 ns + 3.15 × $10^3\ C_2$

DOUBLE-ENDED COMPARATOR



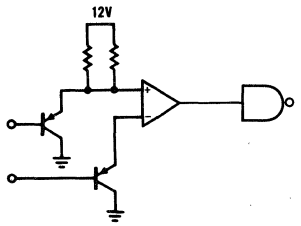
$V_{OH} = V_{Ref1} < V_{IN} < V_{Ref2}$

CRYSTAL CONTROLLED MULTIVIBRATOR



TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $C = \frac{R_2}{1000}$

HIGH INPUT IMPEDANCE LINE RECEIVER (Positive Signals Only)



9621
DUAL-LINE DRIVER
FAIRCHILD INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130Ω twisted pair are provided. The output has the capability of driving high capacitance loads. It can typically switch >200 mA during transients.

FEATURES

- **CCSL COMPATIBILITY**
- **TRANSMISSION LINE BACK-MATCHING**
- **OUTPUT CLAMP DIODES**
- **HIGH CAPACITANCE DRIVE**
- **HIGH OUTPUT VOLTAGE**
- **MILITARY TEMPERATURE RANGE**

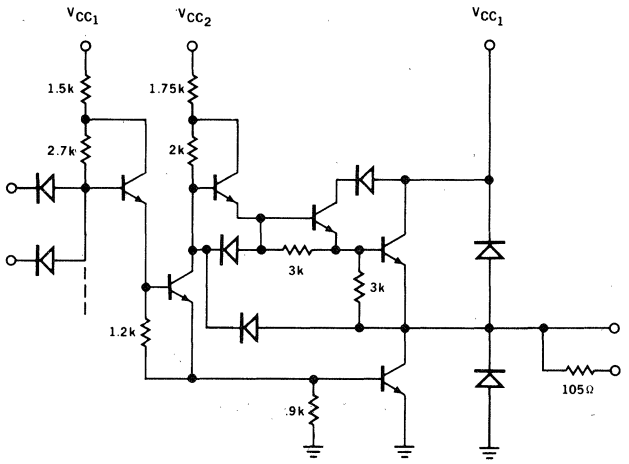
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	+3.8 V to +8 V
Input Voltage	−.5 V to +15 V
Voltage Applied to Outputs	−2 V to +V_{CC1} + 1 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V

ORDER INFORMATION

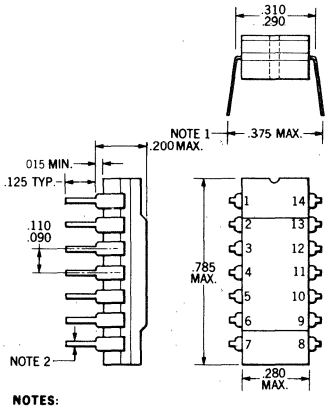
Specify U6A9621XXX for 14 pin Dual In-Line Package or U319621XXX for 14 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

SCHEMATIC DIAGRAM



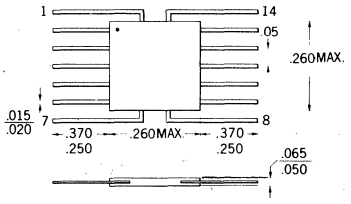
TYPICAL DUAL IN-LINE PACKAGE

Similar to
JEDEC (TO-116) Outline

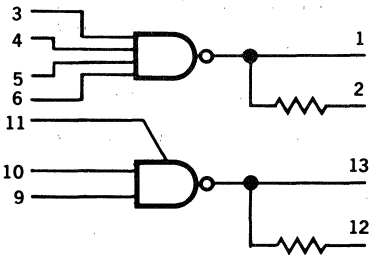


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

14 PIN FLAT PACKAGE



LOGIC DIAGRAM



V_{CC_1}=14

V_{CC_2}=8

GND=7

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS
MILITARY TEMPERATURE RANGE −55°C to +125°C (UXX962151X)

SYMBOL	NOTES	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}		Output Low Voltage		350		200	350		400	mV	I_{OL} = 20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
V_{OH}		Output High Voltage	4.0		4.0	4.3		4.0		V	I_{OH} = −20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{SC}	1	Output "Short Circuit" Current			−180	−300				mA	V_{OUT} = 0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{OL}	1	Output Low Current			150	200				mA	V_{OUT} = 5.0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_F		Input Forward Current		1.8		1.15	1.8		1.8	mA	V_F = 0 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_R		Input Reverse Current		2.0		<1.0	2.0		5.0	μA	V_R = 5.5 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
V_{OLR}	2	Resistive Output Low Voltage				380	500			V	I_{OL} = 2.8 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2				V	I_{OH} = −2.3 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0			V	I_{OL} = −20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0			V	I_{OH} = 20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{pd+}	4	Turn-Off Time				30	150			ns	C_L = 5000 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}	4	Turn-On Time				80	150			ns		
t_{pd+}		Turn-Off Time				13	25			ns	C_L = 30 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}		Turn-On Time				9	25			ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0		0.7	V	V_{CC1} = 5.5 V V_{CC2} = 10.8 V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8		V	V_{CC1} = 4.5 V V_{CC2} = 13.2 V	

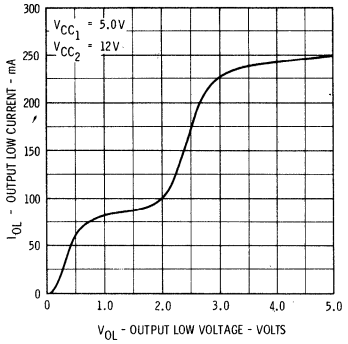
NOTES:
(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) With both sides loaded at T_A = +125°C, maximum frequency = 500 kHz for Dual In-Line package (θ_{JA} = 95°C/W) or 300 kHz for Ceramic Flat Pak (θ_{JA} = 165°C/W).

ELECTRICAL CHARACTERISTICS
INDUSTRIAL TEMPERATURE RANGE 0°C to +75°C (UXX962159X)

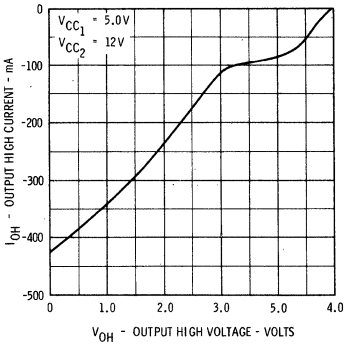
SYMBOL	NOTES	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
			0°C		+25°C			+75°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}		Output Low Voltage		400		200	400		450	mV	$I_{OL} = 20$ mA	$V_{CC1} = 4.75$ V $V_{CC2} = 11.4$ V
V_{OH}		Output High Voltage	4.2		4.2	4.4		4.2		V	$I_{OH} = -20$ mA	$V_{CC1} = 4.75$ V $V_{CC2} = 11.4$ V
I_{SC}	1	Output "Short Circuit" Current			−100	−300				mA	$V_{OUT} = 0$ V	$V_{CC1} = 4.75$ V $V_{CC2} = 11.4$ V
I_{OL}	1	Output Low Current			75	200				mA	$V_{OUT} = 5.0$ V	$V_{CC1} = 4.75$ V $V_{CC2} = 11.4$ V
I_F		Input Forward Current		1.8		1.15	1.8		1.8	mA	$V_F = 0$ V	$V_{CC1} = 5.25$ V $V_{CC2} = 12.6$ V
I_R		Input Reverse Current		5.0		<1.0	5.0		10.0	μA	$V_R = 5.5$ V	$V_{CC1} = 5.25$ V $V_{CC2} = 12.6$ V
V_{OLR}	2	Resistive Output Low Voltage				380	500			V	$I_{OL} = 2.8$ mA	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2				V	$I_{OH} = -2.3$ mA	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0			V	$I_{OL} = -20$ mA	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0			V	$I_{OH} = 20$ mA	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	$V_{CC1} = 5.25$ V $V_{CC2} = 12.6$ V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{pd+}	4	Turn-Off Time				30	200			ns	$C_L = 5000$ pF	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
t_{pd-}	4	Turn-On Time				80	200			ns		
t_{pd+}		Turn-Off Time				13	40			ns	$C_L = 30$ pF	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
t_{pd-}		Turn-On Time				9	40			ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0		0.7	V	$V_{CC1} = 5.25$ V $V_{CC2} = 12.6$ V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8		V	$V_{CC1} = 4.75$ V $V_{CC2} = 11.4$ V	

NOTES:
(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) Maximum frequency = 500 kHz with both sides loaded at $T_A = +75$°C for both Dual In-Line package and Ceramic Flat Pak.

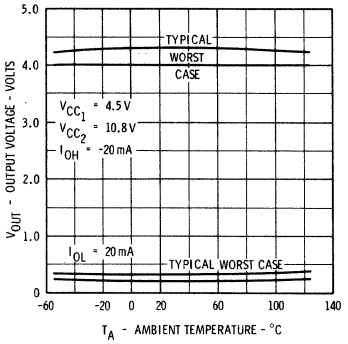
TYPICAL OUTPUT LOW CURRENT VERSUS OUTPUT LOW VOLTAGE



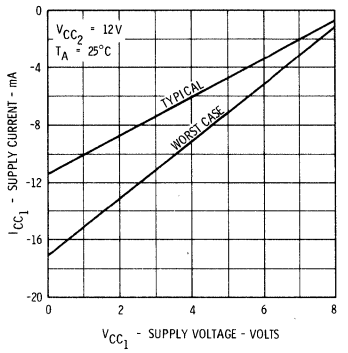
TYPICAL OUTPUT HIGH CURRENT VERSUS OUTPUT HIGH VOLTAGE



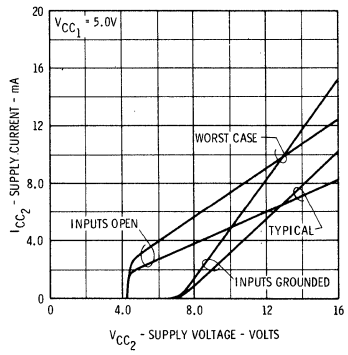
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



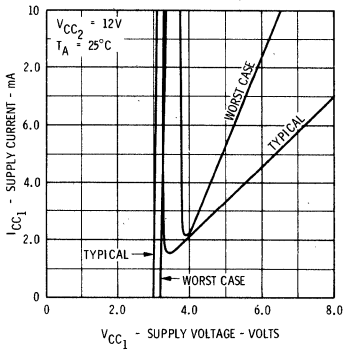
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS GROUNDED



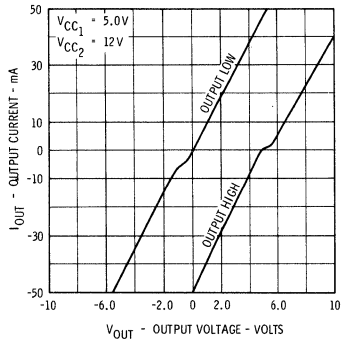
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS OPEN



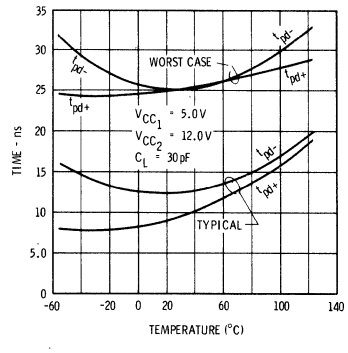
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



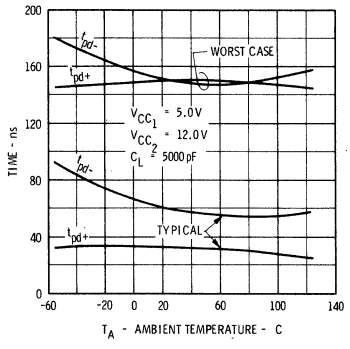
TYPICAL OUTPUT IMPEDANCE WITH BACK MATCHING RESISTORS



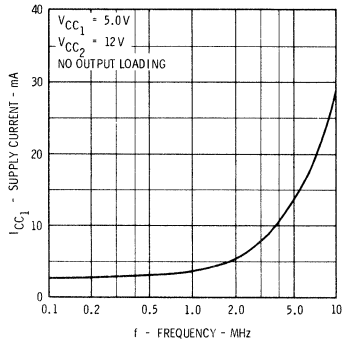
SWITCHING TIME VERSUS TEMPERATURE



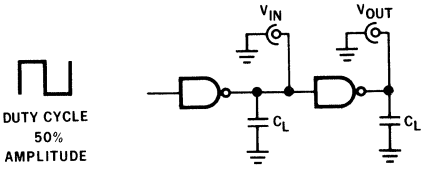
SWITCHING TIME VERSUS TEMPERATURE



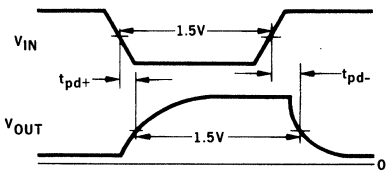
TYPICAL SUPPLY CURRENT VERSUS FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



DESCRIPTION OF REFLECTION DIAGRAM USAGE

The reflections on any line may be found by using the following procedure:

1. Draw the driver output characteristics for both the "high state" and the "low state" on an I - V graph in the same manner as the reflection diagram.
2. Draw the receiver input characteristic on the same graph. The two points of intersection of the receiver and driver characteristics are the two DC operating points.
3. Choose to analyze either the reflections for the output going low or high. In the example chosen the negative transition is analyzed.
4. Draw a line with a slope equal to the impedance of the line to be used, ($Z_0 = 100\Omega$ in the example), from the "high state" operating point (labeled A on our graph) to the "low state" output device characteristic (B_1). B_1 equals the conditions at the driver output immediately after turn-on.
5. Reverse the slope of Z_0 and sketch it from B_1 to the receiver input characteristic (C_1). C_1 equals the conditions at the receiver when the wavefront B_1 first reaches it.
6. By continuing this procedure of reversing the slope of Z_0 at each node all the reflections (B_1, C_1, B_2, C_2, B_3, C_3 - - - B_N, C_N), where B_X is the voltage at the driver and C_X is the voltage at the receiver, can be found.

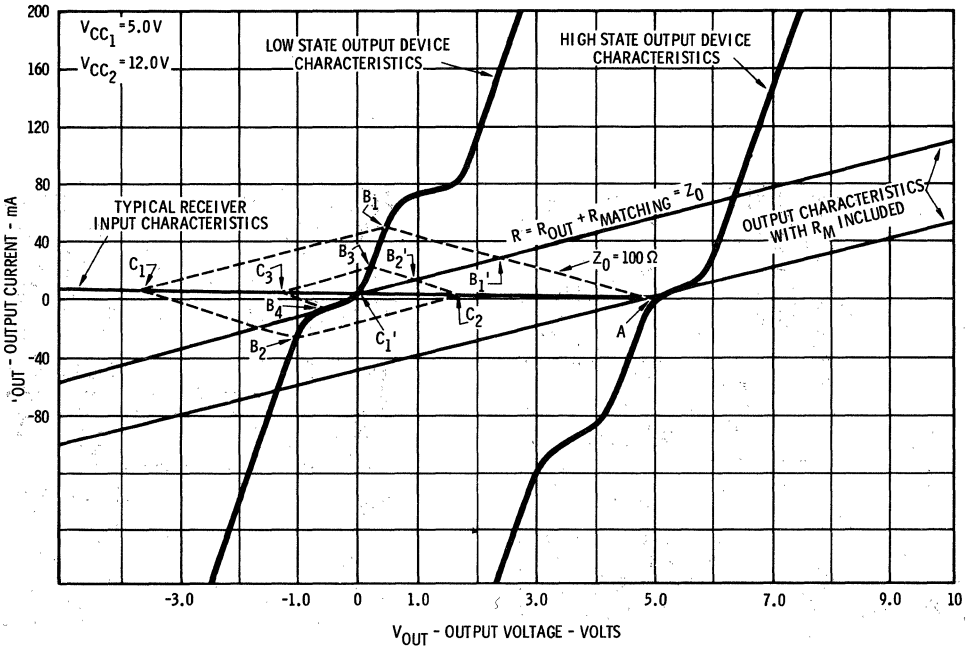
The same procedure is used to check the reflections when switching the output high.

BACK-MATCHING, also referred to as reverse termination, offers several advantages to the user. It reduces the system power by not requiring the high current for resistive termination and it reduces the DC line losses because IR drops in the line become minimum.
To back-match any line (output switching low):

1. Measure the output resistance, R_{out}, from the "low state" operating point to B_1.
2. Subtract R_{out} from Z. ($R_{out} + R_M = Z_0$). This value R_M, is the required back-matching resistance.
3. Place R_M in series with the output of driver.
4. The reflections that occur on the line with R_M inserted can be treated in the same manner as the general case. The results are B_1' and C_1' and the receiver will not see any reflections.

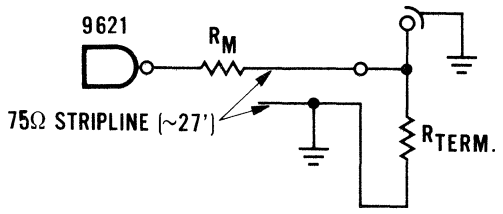
When switching the line differentially $R_M + R_{out} = Z_0/_2$. The matched output characteristics of the 9621 make it possible to back-match effectively and require analysis of switching only one state.

TYPICAL REFLECTION DIAGRAM*



* GRAPHICAL ANALYSIS
First Presented by John B. James of I.C.T. (Eng.) LTD.

REFLECTION TEST CIRCUIT

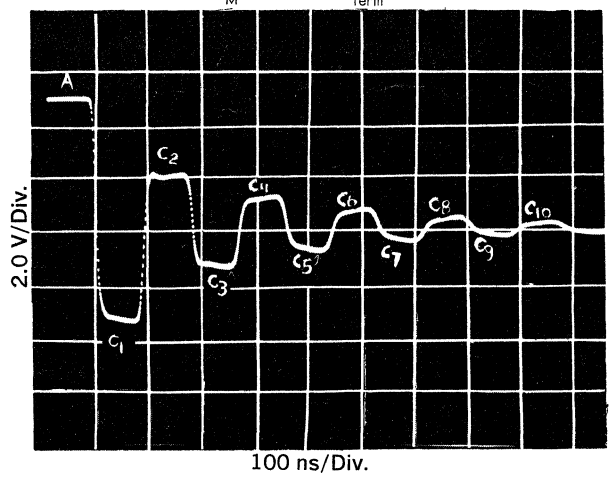


The reflections are two delay's of the line wide. R_{term} is the total impedance seen at the receiving end.

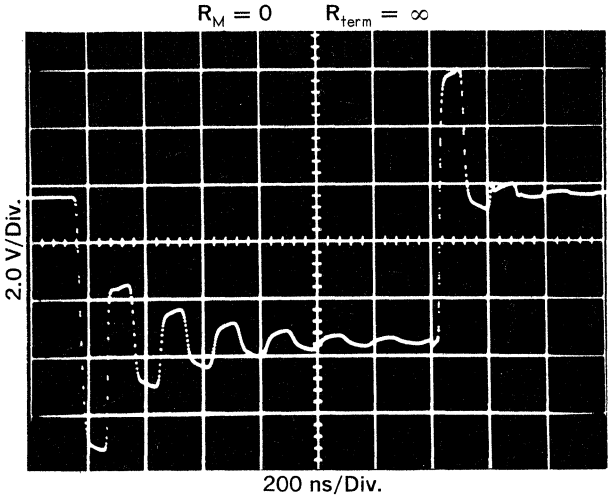
BACK MATCHING TABLE

Z_O	R_M when used single ended	R_M when used differentially
50 Ω	32 Ω	16 Ω
75 Ω	62 Ω	30 Ω
92 Ω	82 Ω	41 Ω
100 Ω	90 Ω	45 Ω
130 Ω	120 Ω	60 Ω
300 Ω	290 Ω	145 Ω
600 Ω	590 Ω	295 Ω

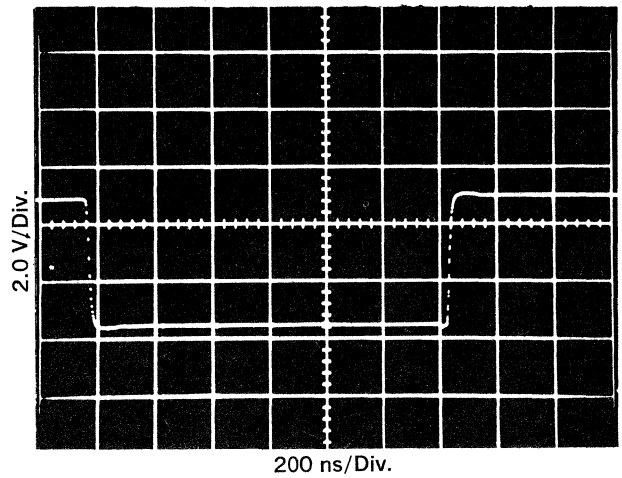
$R_M = 0$ $R_{term} = \infty$



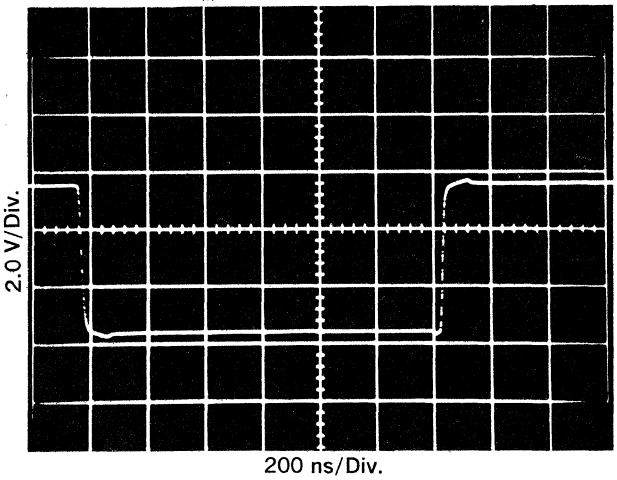
$R_M = 0$ $R_{term} = \infty$



$R_M = 0$ $R_{term} = 75\Omega$



$R_M = 62\ \Omega$ $R_{term} = \infty$



9622

DUAL LINE RECEIVER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9622 is a dual line receiver designed to discriminate a worst case logic swing of 2 volts from a ± 10 volt common mode noise signal or ground shift. A 1.5 volt threshold is built into the differential amplifier to offer a CCSL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only ± 5% (75 mV) over the military and industrial temperature ranges.

The 9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S3. A 130 Ω terminating resistor is provided at the input of the each line receiver. An enable is also provided for each line receiver. The output is CCSL compatible. The output high level can be increased to +12 V by tieing it to a positive supply through a resistor. The outputs can be wire-OR'ed.

FEATURES:

- **CCSL COMPATIBLE THRESHOLD VOLTAGE**
- **INPUT TERMINATING RESISTORS**
- **CHOICE OF OUTPUT STATE WITH INPUTS OPEN**
- **CCSL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE**
- **WIRE-OR CAPABILITY**
- **ENABLE INPUTS**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

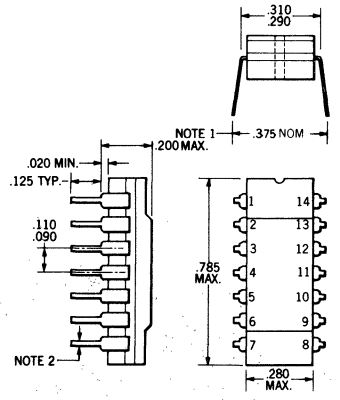
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Input Voltage	±15 V
Voltage Applied to Outputs for High Output State	−0.5 V to +13.2 V
V_{EE} Pin Potential to Ground Pin	−0.5 V to −12 V
Enable Pin Potential to Ground Pin	−0.5 V to +15 V

ORDER INFORMATION

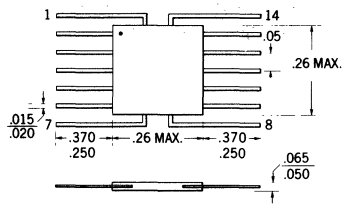
Specify U6A9622XXX for 14 pin Dual In-Line package, U3I9622XXX for 14 pin Flat package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline

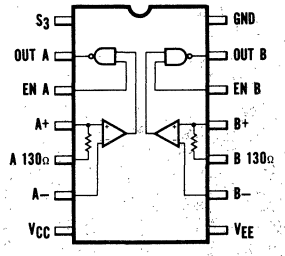


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FLAT PACKAGE
TOP VIEW



LOGIC DIAGRAM



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

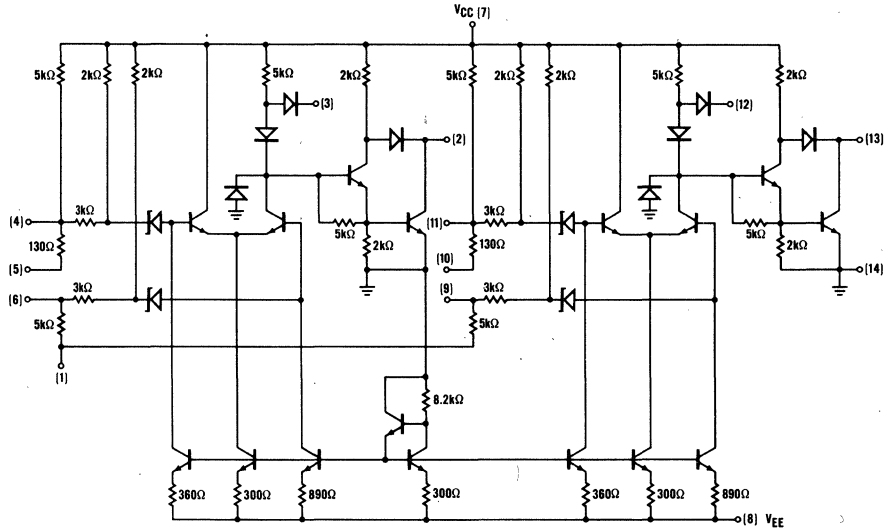
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (Temperature Range −55°C to +125°C, V_{CC} = 5.0 V ±10%, V_{EE} = −10 V ±10%) (Part No. UXX962251X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.40		0.25	0.40		0.40	V	V_{CC} = 4.5 V *V_{DIFF} = 2.0 V	V_{EE} = −11 V I_{OL} = 12.4 mA
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		V	V_{CC} = 4.5 V *V_{DIFF} = 1.0 V	V_{EE} = −9.0 V I_{OH} = −0.2 mA
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CC} = 4.5 V *V_{DIFF} = 1.0 V	V_{EE} = −11 V V_{CEX} = 12 V
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.1	−1.3	−3.1	mA	V_{CC} = 5.0 V *V_{DIFF} = 1.0 V	V_{EE} = −10 V V_{SC} = 0 V
$I_{R(ENABLE)}$	Enable Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V S_3 = 4.5 V	V_{EE} = −11 V V_R = 4.0 V
$I_{F(ENABLE)}$	Enable Input Forward Current		−1.5		−0.96	−1.5		−1.5	mA	V_{CC} = 5.5 V S_3 = 0 V	V_{EE} = −9.0 V V_F = 0 V
$I_{F(+Input)}$	+ Input Forward Current		−2.3		−1.67	−2.1		−2.0	mA	V_{CC} = 5.0 V − Input = Gnd	V_{EE} = −10 V V_F = 0 V
$I_{F(-Input)}$	− Input Forward Current		−2.6		−1.87	−2.4		−2.3	mA	V_{CC}, S_3 = 5.0 V + Input = Gnd	V_{EE} = −10 V V_F = 0 V
$V_{IL(ENABLE)}$	Input Low Voltage		1.3		1.4	1.0		0.7	V	V_{CC} = 5.0 V ±10% V_{EE} = −10 V ±10%	
V_{th}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V	V_{CC} = 5.0 V ±10% V_{EE} = −10 V ±10%	
V_{CM}	Common Mode Voltage			−10	±12	+10			V	V_{CC} = 5.0 V *V_{DIFF} = 1.0 V or 2.0 V	V_{EE} = −10 V
$R_{130}\Omega$	Terminating Resistance			100	130	175			Ω		
I_{CC}	5 V Supply Current				13.7	22.9			mA	V_{CC} = 5.5 V S_3, + Inputs = 5.5 V, − Inputs = 0 V	V_{EE} = −11 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	V_{CC} = 5.5 V S_3, + Inputs = 5.5 V, − Inputs = 0 V	V_{EE} = −11 V
t_{pd+}	Turn-off Time				38	50			ns	V_{CC} = 5.0 V V_{IN} 0→3 V, R_L = 3.9 kΩ, C_L = 30 pF	V_{EE} = −10 V
t_{pd-}	Turn-on Time				35	50			ns	V_{CC} = 5.0 V V_{IN} 0→3.0 V, R_L = 0.39 kΩ, C_L = 30 pF	V_{EE} = −10 V

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

SCHEMATIC DIAGRAM
(LINE RECEIVER)

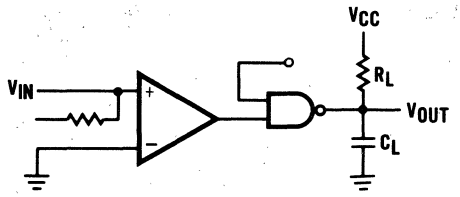


ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, $V_{CC} = 5.0\ V \pm 5\%$, $V_{EE} = -10\ V \pm 5\%$) (Part No. UXX962259X)

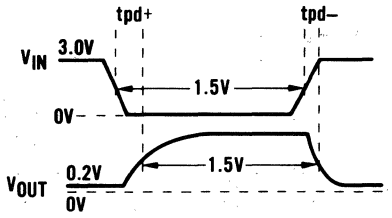
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	$V_{CC} = 4.75\ V$ $*V_{DIFF} = 2.0\ V$	$V_{EE} = -10.5\ V$ $I_{OL} = 14.1\ mA$
V_{OH}	Output High Voltage	2.9		3.0	3.3		2.9		V	$V_{CC} = 4.75\ V$ $*V_{DIFF} = 1.0\ V$	$V_{EE} = -9.5\ V$ $I_{OH} = -0.2\ mA$
I_{CEX}	Output Leakage Current		80			100		200	μA	$V_{CC} = 4.75\ V$ $*V_{DIFF} = 1.0\ V$	$V_{EE} = -10.5\ V$ $V_{CEX} = 5.25\ V$
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.2	−1.3	−3.1	mA	$V_{CC} = 5.0\ V$ $*V_{DIFF} = 1.0\ V$	$V_{EE} = -10\ V$ $V_{SC} = 0\ V$
$I_{R(ENABLE)}$	Enable Input Leakage Current					5		10	μA	$V_{CC} = 4.75\ V$ $S_3 = 4.75\ V$	$V_{EE} = -10.5\ V$ $V_R = 4.0\ V$
$I_{F(ENABLE)}$	Enable Input Forward Current		−1.5		−.96	−1.5		−1.5	mA	$V_{CC} = 5.25\ V$ $S_3 = 0\ V$	$V_{EE} = -9.5\ V$ $V_F = 0\ V$
$I_{F(+Input)}$	+ Input Forward Current		−2.6		−1.67	−2.4		−2.3	mA	$V_{CC} = 5.0\ V$ − Input = Gnd	$V_{EE} = -10\ V$ $V_F = 0\ V$
$I_{F(-Input)}$	− Input Forward Current		−2.9		−1.87	−2.7		−2.6	mA	$V_{CC}, S_3 = 5.0\ V$ + Input = Gnd	$V_{EE} = -10\ V$ $V_F = 0\ V$
$V_{IL(ENABLE)}$	Input Low Voltage		1.2		1.4	1.0		0.85	V	$V_{CC} = 5.0\ V \pm 5\%$ $V_{EE} = -10\ V \pm 5\%$	
V_{th}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V	$V_{CC} = 5.0\ V \pm 5\%$ $V_{EE} = -10\ V \pm 5\%$	
V_{CM}	Common Mode Voltage			−7.5	±12	+7.5			V	$V_{CC} = 5.0\ V$ $*V_{DIFF} = 1.0\ V$ or $2.0\ V$	$V_{EE} = -10\ V$
$R_{130\Omega}$	Terminating Resistance			91	130	185			Ω		
I_{CC}	5 V Supply Current				13.7	22.9			mA	$V_{CC} = 5.25\ V$ S_3, +Inputs = 5.25 V, −Inputs = 0 V	$V_{EE} = -10.5\ V$
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	$V_{CC} = 5.25\ V$ S_3, +Inputs = 5.25 V, −Inputs = 0 V	$V_{EE} = -10.5\ V$
t_{pd+}	Turn-off Time				38	100			ns	$V_{CC} = 5.0\ V$ V_{IN} 0→3.0 V, $R_L = 3.9\ k\Omega$, $C_L = 30\ pF$	$V_{EE} = -10\ V$
t_{pd-}	Turn-on Time				35	100			ns	$V_{CC} = 5.0\ V$ V_{IN} 0→3.0 V, $R_L = 0.39\ k\Omega$, $C_L = 30\ pF$	$V_{EE} = -10\ V$

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

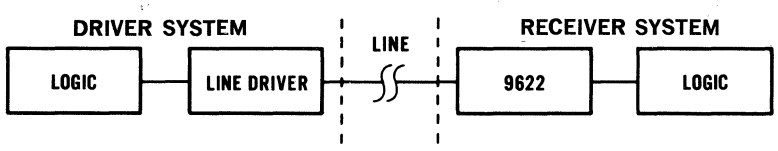
SWITCHING TIME TEST CIRCUIT



WAVEFORMS

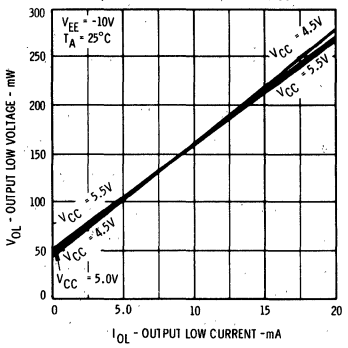


STANDARD USAGE

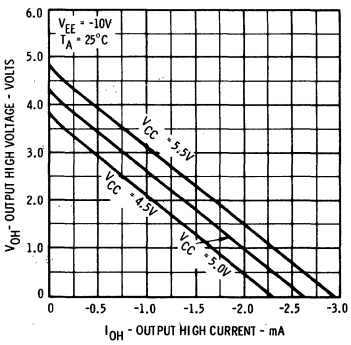


TYPICAL ELECTRICAL CHARACTERISTICS

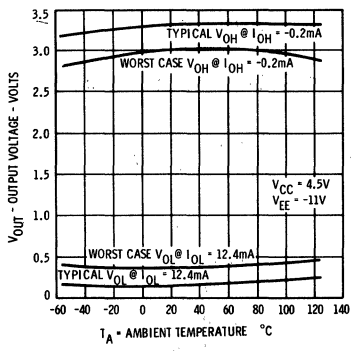
TYPICAL OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



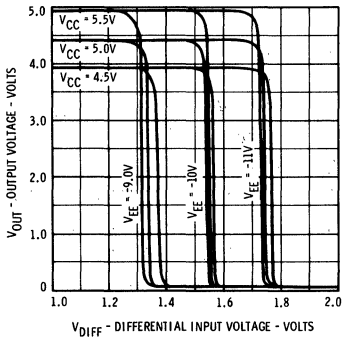
TYPICAL OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



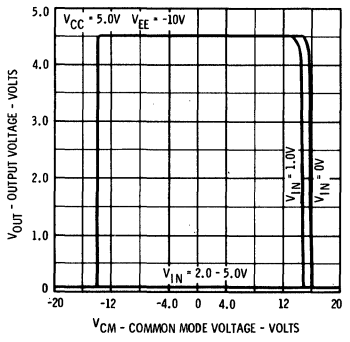
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



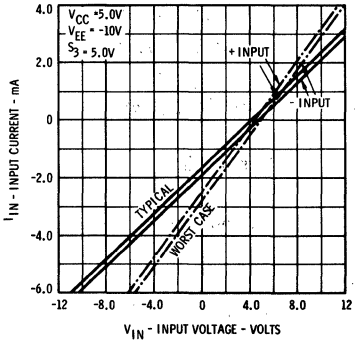
TYPICAL V_{out} - V_{DIFF} TRANSFER CHARACTERISTICS



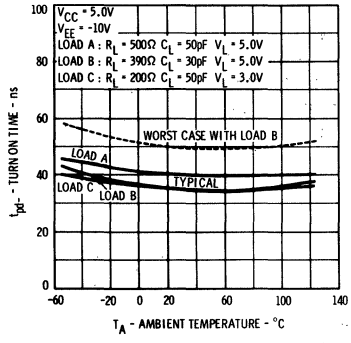
TYPICAL OUTPUT VOLTAGE VERSUS COMMON MODE VOLTAGE



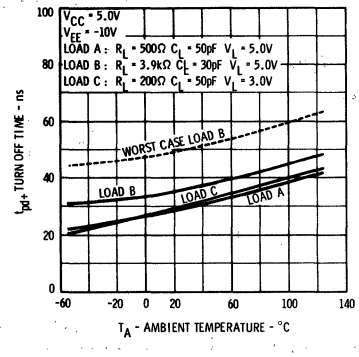
INPUT CURRENT VERSUS INPUT VOLTAGE



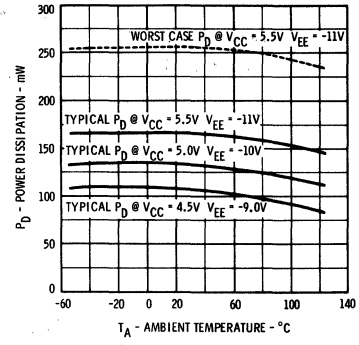
TURN ON TIME VERSUS AMBIENT TEMPERATURE



TURN OFF TIME VERSUS AMBIENT TEMPERATURE



POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



9624 • 9625

DUAL CCSL, MOS INTERFACE ELEMENTS

FAIRCHILD INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 9624 is a dual two-input CCSL compatible interface gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

The 9625 is a dual MOS to CCSL level converter. It is designed to convert standard negative MOS logic levels to CCSL levels. The 9625 features a high input impedance which allows preservation of the driving MOS logic level.

Both the 9624 and 9625 are available in the 14-pin ceramic Dual In-Line package and the ¼ x ¼ Flat Pak.

FEATURES

- **CCSL COMPATIBLE INPUTS/OUTPUT**
- **MOS COMPATIBLE OUTPUT/INPUTS**
- **LOW POWER**

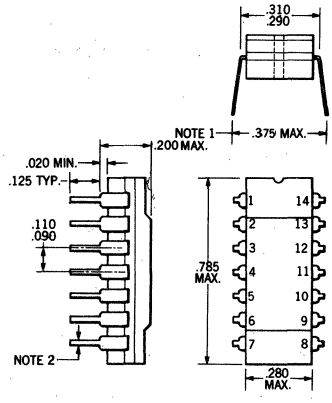
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	V_{DD} to +10 V
Voltage Applied to Outputs for high output state (9624)	V_{DD} to +V_{CC} value
Voltage Applied to Outputs for high output state (9625)	−0.5 V to V_{CC} value
Input Voltage (D.C.) (9624)	−0.5 V to +5.5 V
Input Voltage (D.C.) (9625)	V_{CC} to V_{DD}
V_{DD} Pin Potential to Ground Pin	−30 V to +0.5 V
V_{DD} Pin Potential to Tap Pin (9624)	−30 V to +0.5 V
V_{TAP}	V_{CC} + 0.5 V

ORDER INFORMATION

Specify U6A9624XXX and U6A9625XXX for 14-pin TO-116 Dual In-Line package or U3I9624XXX and U3I9625XXX for 14-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

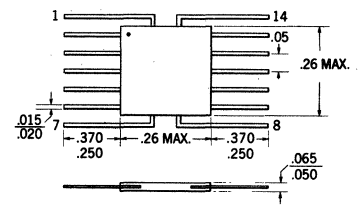
TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline



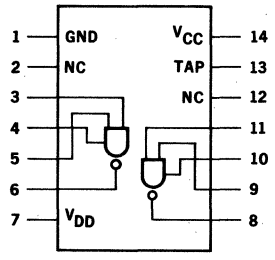
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

14-PIN FLAT PACKAGE

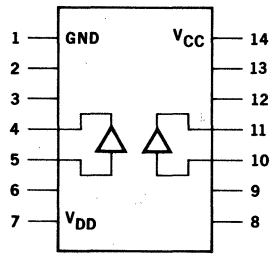
TOP VIEW



9624



9625



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH1}	Output High Voltage	−1.0		−1.0	−0.5		−1.0	Volts	$V_{CC} = 4.5\ V$, $V_{DD} = -28\ V$, $V_{TAP} = 0\ V$ $I_{OH} = -10\ \mu A$
V_{OH2}	Output High Voltage	+3.5		+3.5	+4.0		+3.5		$V_{CC} = 5.5\ V$, $V_{DD} = -20\ V$, $V_{TAP} = 5.5\ V$ Inputs at threshold voltages (V_{IL}) $I_{OH} = -10\ \mu A$
V_{OL}	Output Low Voltage			See Note 1				Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10\ mA$, $V_{DD} = -11$ to $-28\ V$ @ V_{IH}, $0 \leq V_{TAP} \leq V_{CC}$
V_{IH}	Input High Voltage	2.1		1.9			1.7	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1	0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.40			−1.25	−1.13	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$ $V_{DD} = -11$ to $-28\ V$
I_R	Input Leakage Current		2.0			2.0	5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ $V_{DD} = -11$ to $-28\ V$
I_{CEX}	Output Leakage Current					50		μA	$V_{CC} = 5.5\ V$, $V_{TAP} = 0\ V$ $V_{DD} = -28\ V$, $V_{OUT} = 0\ V$
I_{SC}	Output Short Circuit Current	−12	−31	−14		−32	−11 −28	mA	$V_{CC} = 4.5\ V$, $V_{TAP} = 0\ V$, $V_{IN} = 0\ V$ $V_{DD} = -11\ V$, $V_{OUT} = -11\ V$
I_{VCC}	V_{CC} Supply Current					6.1		mA	$V_{CC} = 5.5V$, $V_{DD} = -15\ V$, $V_{TAP} = 0\ V$ Inputs Open
I_{MAX}	Max. Current					10		mA	$V_{CC} = 10\ V$, $V_{DD} = -30\ V$, Inputs Open $V_{TAP} = 0\ V$
t_{pd+}	Switching Speed				190	250		ns	$V_{CC} = 5.0\ V$, See Figure 2
t_{pd-}	Switching Speed				50	100		ns	$V_{DD} = -13\ V$, $V_{TAP} = 0\ V$

Note 1: Max = V_{DD} +1.0 V over Temperature Range
Typ = V_{DD} +0.2 V over Temperature Range

SCHEMATIC DIAGRAM

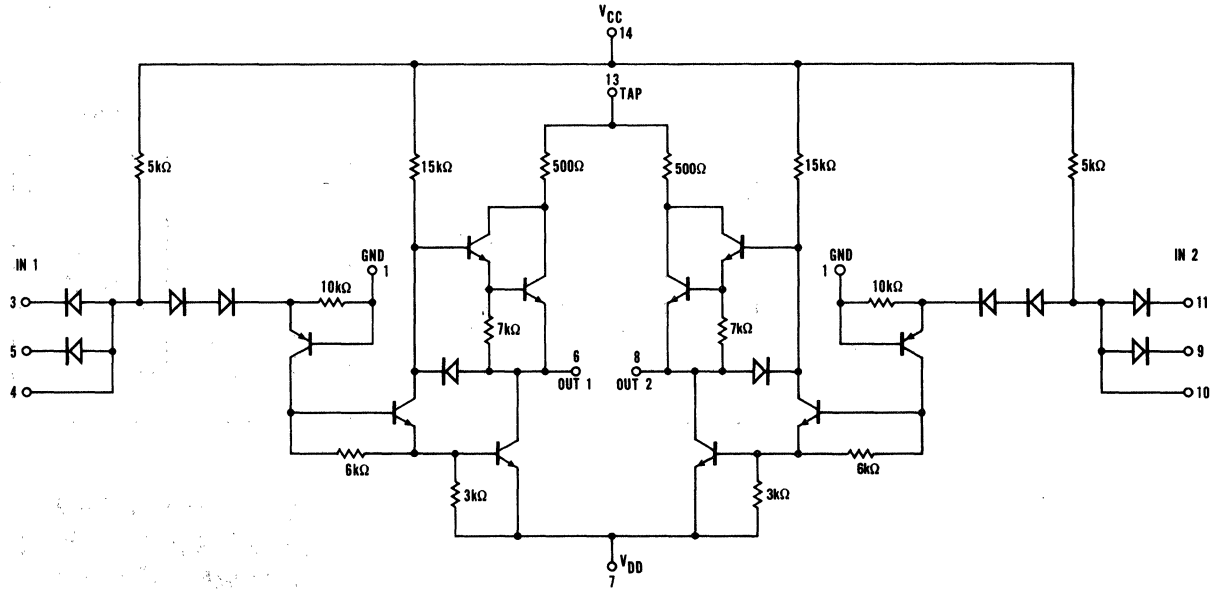


Fig. 1

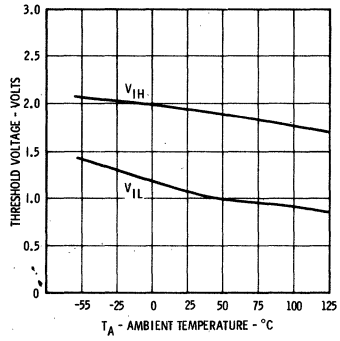
TABLE II —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH1}	Output High Voltage	−1.0		−1.0	−0.5		−1.0		Volts	V_{CC} = 4.75 V, V_{DD} = −28 V, V_{TAP} = 0 V I_{OH} = −10 μA
V_{OH2}	Output High Voltage	+3.25		+3.25	+3.75		+3.25		Volts	V_{CC} = 5.25 V, V_{DD} = −20 V, V_{TAP} = 5.25 V I_{OH} = −10 μA Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage				See Note 1				Volts	V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{DD} = −11 to −28 V @ 0 ≤ V_{TAP} ≤ V_{CC}
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.32			−1.25		−1.20	mA	V_{CC} = 5.25 V, V_F = 0.45 V
I_R	Input Leakage Current		5.0			5.0		10	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = 5.25 V, V_{TAP} = 0 V V_{DD} = −28 V, V_{OUT} = 0 V
I_{SC}	Output Short Circuit Current	−12	−31	−14		−32	−12	−31	mA	V_{CC} = 4.75 V, V_{TAP} = 0 V, V_{IN} = 0 V V_{DD} = −11 V, V_{OUT} = −11 V
I_{VCC}	V_{CC} Supply Current					6.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{TAP} = 0 V Input Open
I_{MAX}	Max. Current					10			mA	V_{CC} = 10 V, V_{DD} = −30 V, V_{TAP} = 0 V Input Open
t_{pd+}	Switching Speed				190	250			ns	V_{CC} = 5.0 V, See Figure 2
t_{pd-}	Switching Speed				50	100			ns	V_{DD} = −13 V, V_{TAP} = 0 V

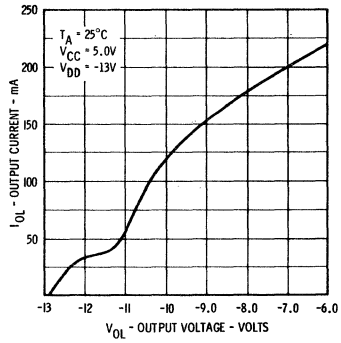
Note 1: Max = V_{DD} +1.0 V over Temperature Range
Typ = V_{DD} +0.2 V over Temperature Range

ELECTRICAL CHARACTERISTICS • 9624

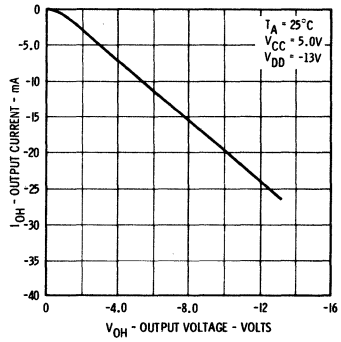
THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



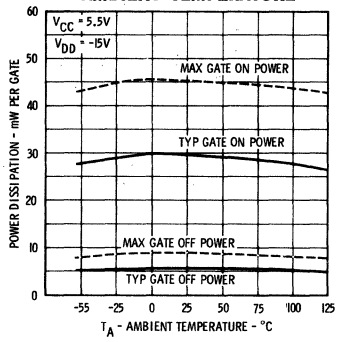
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



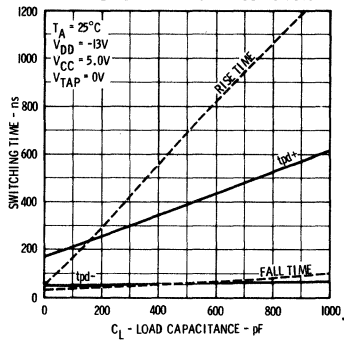
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



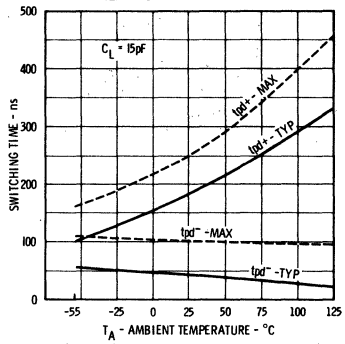
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



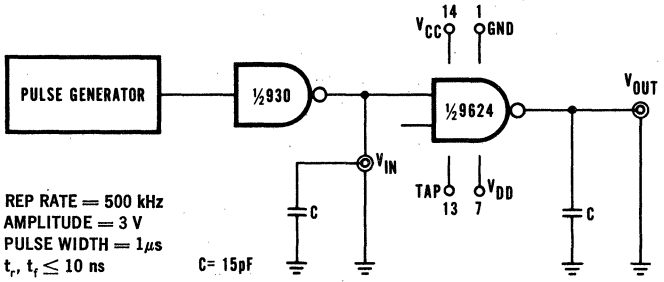
TYPICAL SWITCHING TIME VERSUS LOAD CAPACITANCE

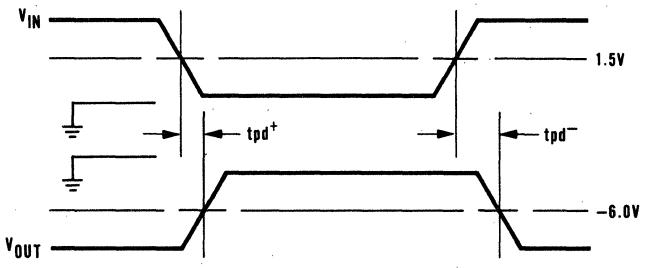


SWITCHING TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
9624





TESTS	CONDITIONS			
	T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	Tap Voltage
t_{pd}^+, t_{pd}^-	25	5.0	−13	0

Fig. 2

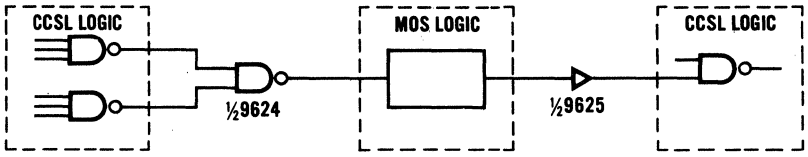
LOADING RULES:

*The extender pin allows the number of inputs to be extended by adding diodes or the DTμL 933 extender.

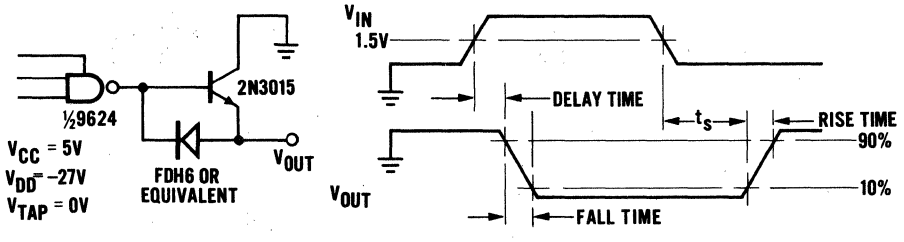
Note 1: Fan out into MOS is limited only by MOS leakage currents.

Note 2: $I_{IN} = +210\ \mu A$

APPLICATION:



CLOCK DRIVING (using a high capacitance drive scheme)



TYPICAL SWITCHING TIMES VERSUS LOAD CAPACITANCE

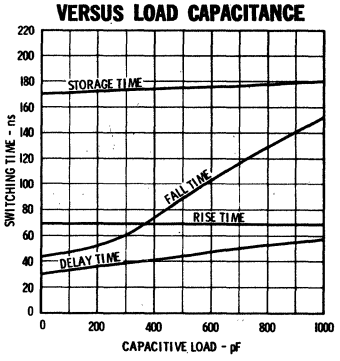


TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	2.5		2.6			2.5	Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -60\ \mu A$ $V_{DD} = -11\ V$ Inputs at threshold voltages (V_{IH})
V_{OL}	Output Low Voltage		0.5			0.5	0.5	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 1.5\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 1.2\ mA$ $V_{DD} = -11\ V$ Inputs at threshold voltages (V_{IL})
V_{IH}	Input High Voltage	−3.0				−3.0	−3.0	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage	−9.0		−9.0			−9.0	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		210			210	210	μA	$V_{CC} = 5.0\ V$, $V_F = -3.0\ V$, $V_{DD} = -13\ V$
I_{CEX}	Output Leakage Current					50		μA	$V_{CC} = V_{CEX} = 4.5\ V$, $V_{DD} = -13\ V$
I_{VCCL}	Supply Current					4.8		mA	$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$, $V_{IN} = -10\ V$
I_{VCCH}	Supply Current					2.1			$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$, $V_{IN} = 0\ V$
I_{VDD}	V_{DD} Supply Current					−9.0		mA	$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$ Input open or gnd
I_{MAX}	Max. V_{DD} Supply Current					−25		mA	$V_{CC} = 8.0\ V$, $V_{DD} = -20\ V$, $V_{IN} = 0\ V$
t_{pd+}	Switching Speed				55	100		ns	$V_{CC} = 5.0\ V$, $V_{DD} = -13\ V$ See Figure 4
t_{pd-}	Switching Speed				90	150		ns	

SCHEMATIC DIAGRAM

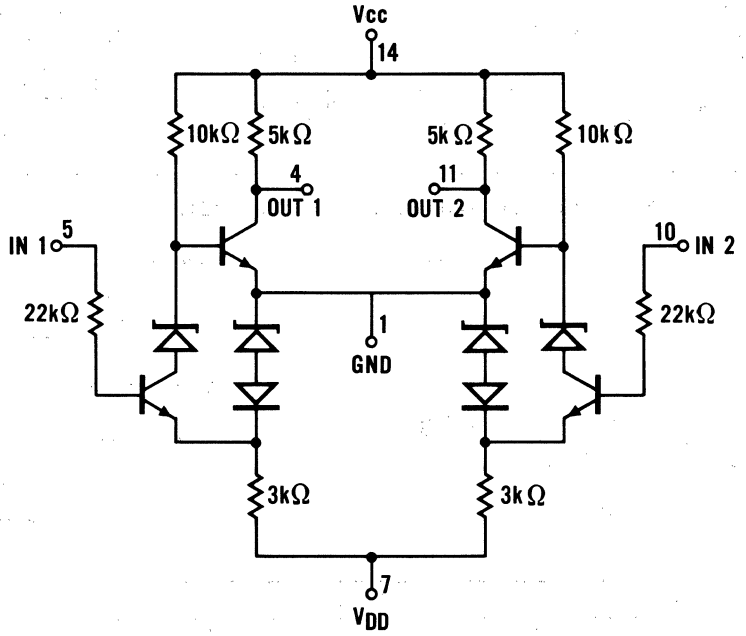
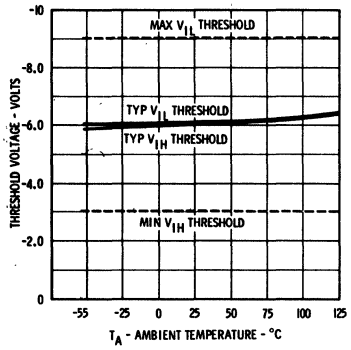


Fig. 3

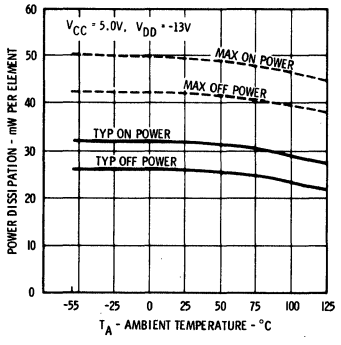
TABLE IV —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	V_{CC} = 4.75 V, I_{OH} = −60 μA V_{DD} = −11 V Inputs at threshold voltages (V_{IH})
V_{OL}	Output Low Voltage		0.5			0.5		0.5	Volts	V_{CC} = 5.25 V, I_{OL} = 1.52 mA V_{CC} = 4.75 V, I_{OL} = 1.33 mA Inputs at threshold voltages (V_{IL})
V_{IH}	Input High Voltage	−3.0		−3.0			−3.0		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		−9.0			−9.0		−9.0	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		210			210		210	μA	V_{CC} = 5.0 V, V_F = −3.0 V, V_{DD} = −13 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 4.75 V, V_{DD} = −13 V
I_{VCCL}	Supply Current					4.8			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = −10 V
I_{VCCH}	Supply Current					2.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = 0 V
I_{VDD}	V_{DD} Supply Current					−9.0			mA	V_{CC} = 5.5 V, V_{DD} = −15 V Input open or gnd
I_{MAX}	Max. V_{DD} Supply Current					−25			mA	V_{CC} = 8.0 V, V_{DD} = −20 V, V_{IN} = 0 V
t_{pd+}	Switching Speed				55	100			ns	V_{CC} = 5.0 V, V_{DD} = −13 V See Figure 4
t_{pd-}	Switching Speed				90	150			ns	

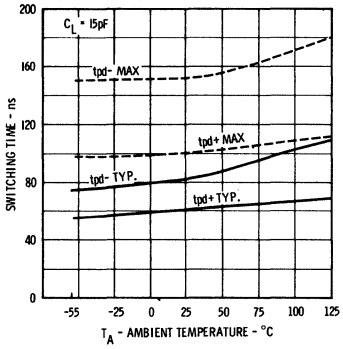
THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

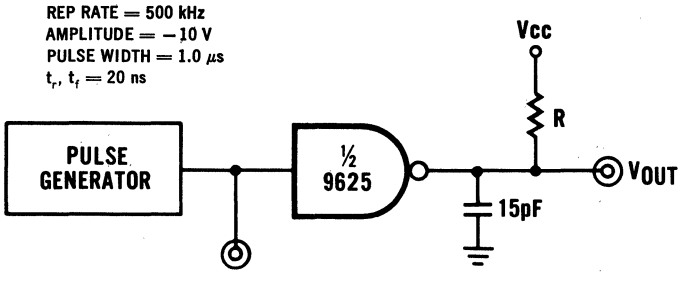


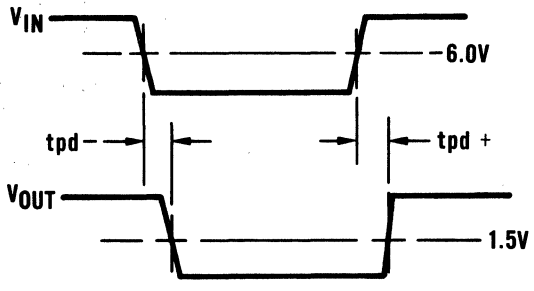
SWITCHING TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

REP RATE = 500 kHz
AMPLITUDE = −10 V
PULSE WIDTH = 1.0 μs
t_r, t_f = 20 ns





TESTS	CONDITIONS T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	R (kΩ)
t_{pd}^+, t_{pd}^-	25	5.0	−13	3.75

Fig. 4

CμL 9958
DECADE COUNTER
COUNTER MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The CμL9958 is a complete Decade Counter consisting of four cascaded binary triggered flip-flops modified by a feedback loop to count in the familiar 8-4-2-1 code. Provision is made for clearing and presetting any one of the possible decimal states. The monolithic structure employs only resistors and transistors and is manufactured with Fairchild Planar* Epitaxial process to assure maximum performance and reliability.

The Decade Counter is designed to operate in the 0° to +75°C temperature range with nominal power supply voltage of 3.3 to 5.5 volts. It is also available in the -55°C to +125°C temperature range with power supply voltage of 4.0 to 4.4 volts.

The CμL9985 is available in the hermetically sealed 14 pin Dual In-line ceramic package, and in the 8 pin modified TO-5 metal can.

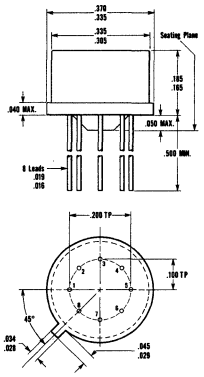
ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	-55°C to +150°C
Voltage at pin 7 (0°C 14 on Dip (0°C to +75°C)	+6.0 V
Count Input Pin Voltage	+4.0 V, -2.0 V
Reset Input Pin Voltage	+4.0 V, -2.0 V
Current into Each Output Terminal	± 5.0 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	3.3		5.5		
Count Input-Low			0.45	V	
Count Input-High	1.2			V	
Count Input Pulse Width-High	150			ns	
Count Input Slope-Positive Going	1.0			V/μs	
Maximum Count Input Frequency			2.0	MHz	
Reset Input-Low			0.45	V	
Reset Input-High	1.2			V	
Output-Low			0.35	V	I_{out} = 0.4 mA V_{CC} = 4.0 V
Output-High	1.4			V	I_{out} = -0.7 mA V_{CC} = 3.6 V
Power Consumption		140		mW	V_{CC} = 4.0 V
Count Input Impedance	2 kΩ in series with a transistor base-emitter diode				
Reset Input Impedance	300 Ω in series with a transistor base-emitter diode				
Maximum Delay from Count Input to Z_8 Output (count 7 to 8)	300 ns (Load: 2 kΩ parallel with 50 pF from each output to ground)				

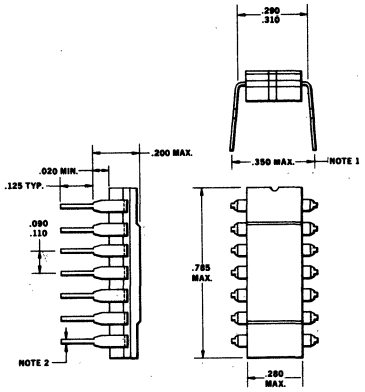
PHYSICAL DIMENSIONS
(SIMILAR TO TO-5)



NOTES: Dimensions as per latest JS-10 committee.
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 1.12 grams.

(PRODUCT CODE: U5B995879X)

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

(PRODUCT CODE: U6A995879X)

*Planar is a patented Fairchild process.

NOTE:
(1) These ratings are limiting values above which serviceability of unit may be impaired.

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RESET/PRESET

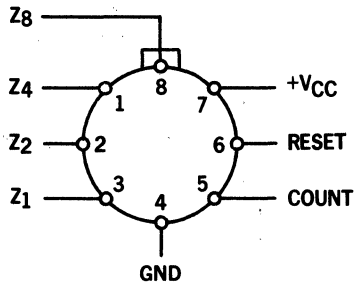
The circuit is reset to count 0 (all outputs high) with a high level at the reset input pin.

To preset an arbitrary count:

1. Reset to count 0 and then return the reset pin to a low level.
2. Ground (below 0.45 V) the appropriate outputs.

TO-5 CONNECTION DIAGRAM

(Top View)



14 PIN DUAL IN-LINE CONNECTION DIAGRAM (TOP VIEW)

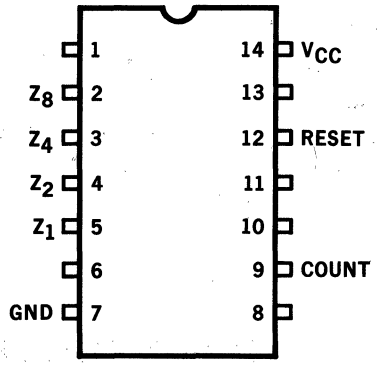
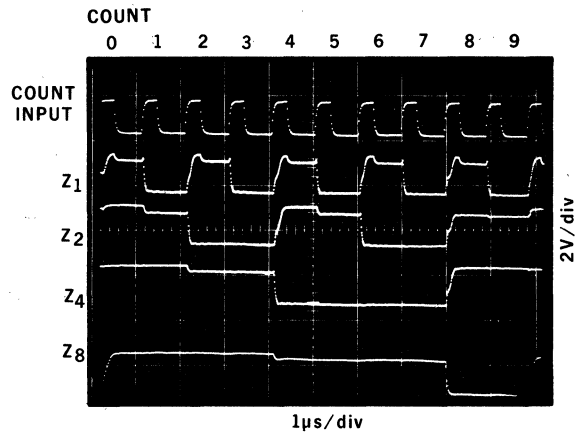


TABLE OF OUTPUT STATES

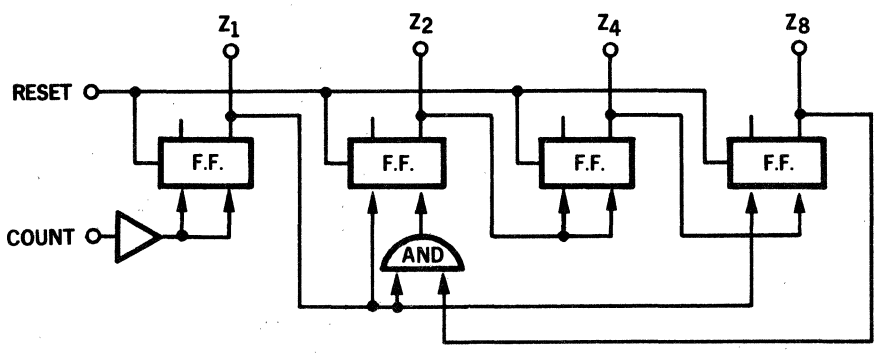
COUNT (H=High, L=Low)

	0	1	2	3	4	5	6	7	8	9
Z_1	H	L	H	L	H	L	H	L	H	L
Z_2	H	H	L	L	H	H	L	L	H	H
Z_4	H	H	H	H	L	L	L	L	H	H
Z_8	H	H	H	H	H	H	H	H	L	L

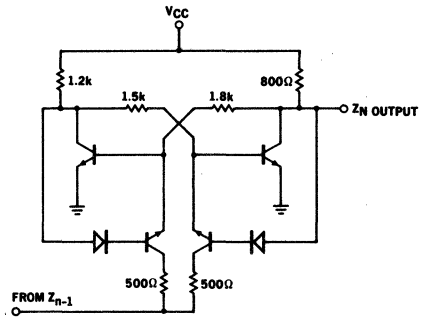
OUTPUT WAVEFORMS



BLOCK DIAGRAM

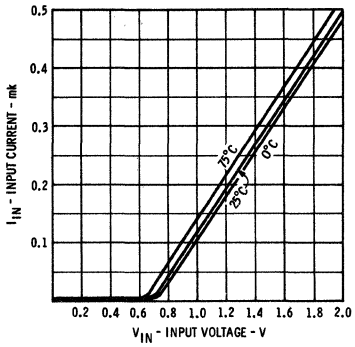


SCHEMATIC DIAGRAM OF DECADE FLIP-FLOP

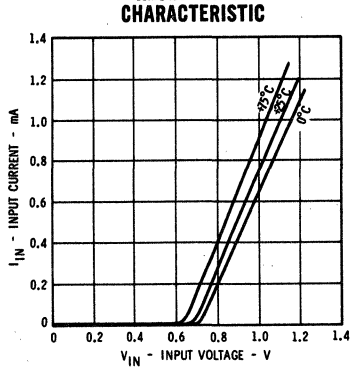


TYPICAL ELECTRICAL CHARACTERISTICS

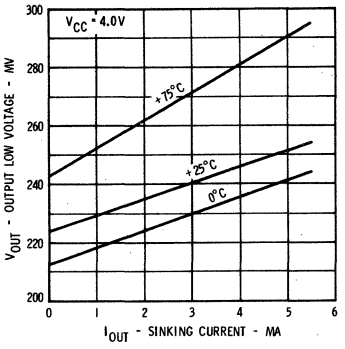
COUNT INPUT CHARACTERISTIC



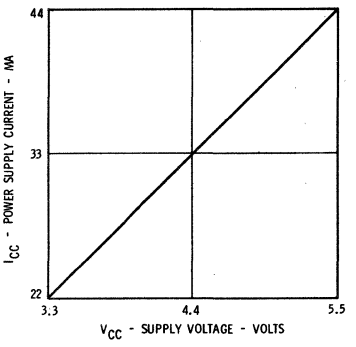
RESET INPUT CHARACTERISTIC



OUTPUT CHARACTERISTICS (OUTPUT LOW)



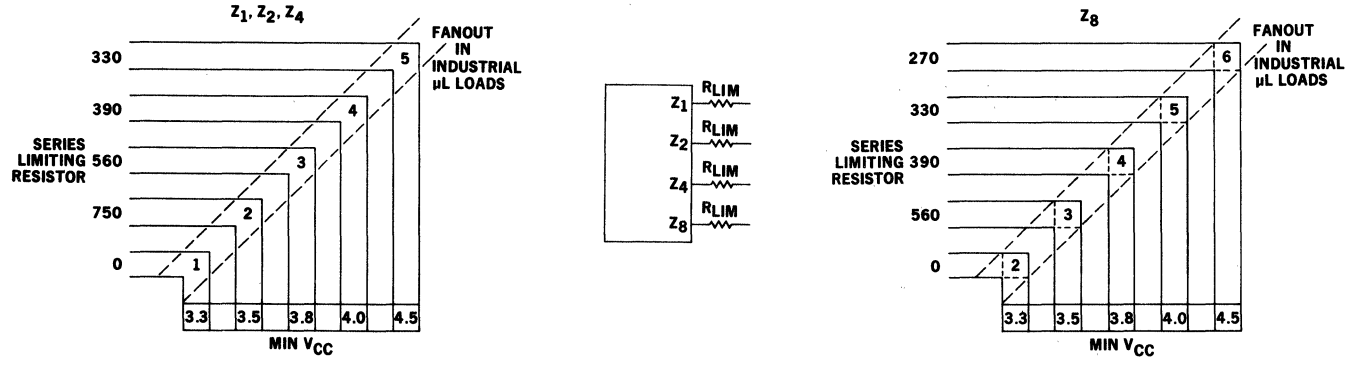
POWER SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



LOADING RULES

DRIVING DEVICE	AT V_{CC} OF	CAN DRIVE
CμL 9958:		
Z_1, Z_2, Z_4	3.3 Min.	1 CμL 9959
Z_8	3.3 Min.	1 CμL9959plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	4.0 Min.	2 CμL 9959
Z_8	4.0 Min.	2 CμL9959plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	4.0 V Min. and one 390 Ω current limiting resistor in series with each output	4 CμL 9959
Z_8	4.0 V Min. and one 330 Ω current limiting resistor in series with Z_8 output	4 CμL9959plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	3.3 Min.	1 CμL 9960
Z_8	3.3 Min.	1 CμL9960plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	4.0 Min.	2 CμL 9960
Z_8	4.0 Min.	2 CμL9960plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	4.0 Min. and one 330 Ω current limiting resistor in series with each output	5 CμL 9960
Z_8	4.0 Min. and one 270 Ω current limiting resistor in series with Z_8 output	5 CμL9960plus 1 CμL 9958 Count Inputs
Industrial Range Milliwatt RTL:	3.6 V ± 10%	1 CμL9958Count Input
Industrial Range RTL:	3.6 V ± 10%	6 CμL9958Count Inputs, or 1 CμL 9958 Reset Input
Industrial Range DTL 6k Family:	4.5 Min.	1 CμL9958Count Input
Industrial Range DTL 2k Family:	4.5 Min.	3 CμL9958Count Inputs, or 1 CμL9958 Reset Input

CμL 9958 FAN-OUT VERSUS V_{CC} AND SERIES LIMITING RESISTORS



CμL9959

BUFFER - STORAGE ELEMENT

COUNTING MICROLOGIC® INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The CμL 9959 Buffer-Storage unit consists of four gated-latch circuits, and a common gate driver, diffused into a single silicon substrate. Information which is present at the four data inputs enters the latches throughout the interval of a load command applied to the gate input terminal. With gate high, information is stored until a subsequent load command permits a change.

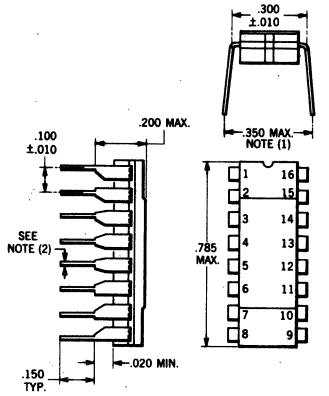
The unit has eight output terminals (both true and complement for each storage position).

RULES FOR USE OF CμL9959

The principal intended use of the CμL9959 is with industrial and ground support systems, with operating V_{CC} from 3.3 to 5.0 volts, and from 0°C to +75°C ambient temperature. This temperature range may be extended to -55°C by raising minimum V_{CC} to 4.0 Volts or it may be extended to +125°C by lowering maximum V_{CC} to 4.4 Volts.

PHYSICAL DIMENSIONS

CμL PACKAGE OUTLINE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	-55°C to +150°C
Supply Voltage (0°C to +75°C)	6.0 V
Gate Input and Data Input Pin Voltage	+4.0 V, -2.0 V
Current into Each Output Terminal	+15 mA
Voltage Applied to an Output Terminal	+6.0 V, -0.3 V

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Characteristic	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	3.3	3.8	5.0	V	
Power Consumption		115		mW	V_{CC} = 3.8 V Gate High
Power Consumption		135		mW	V_{CC} = 3.8 V Gate Low
Gate Input High	1.1			V	
Gate Input Low			0.5	V	
Data Input High	1.0			V	
Data Input Low			0.5	V	
Output Low			0.4	V	I_{OUT} = 3.0 mA, V_{CC} = 5.0 V
Output Low		0.6		V	I_{OUT} = 10 mA
Load Current	-0.4			mA	V_{OUT} = 1.5 V, V_{CC} = 3.3 V
Max. Sampling Rate		>5.0		MHz	
Sampling Pulse Width (Gate)	100			ns	

NOTES:

(1) These ratings are limiting values above which severiceability of unit may be impaired.

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TRUTH TABLE

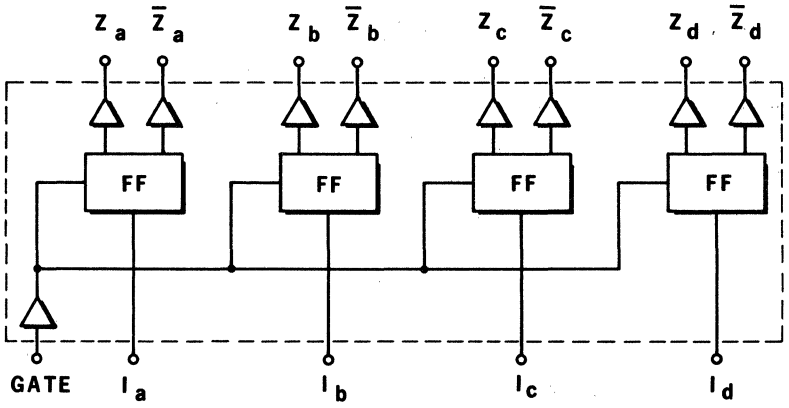
GATE	I	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	ANY	Q	$\overline{Q}$

H = HIGH

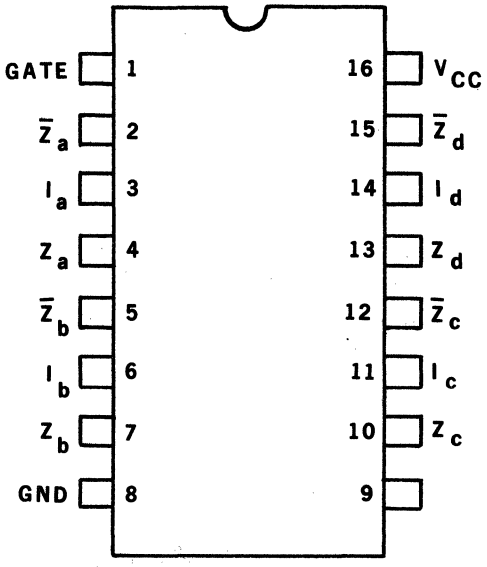
L = LOW

Q = THE STATE ASSUMED PRIOR TO "GATE HIGH" IS MAINTAINED.

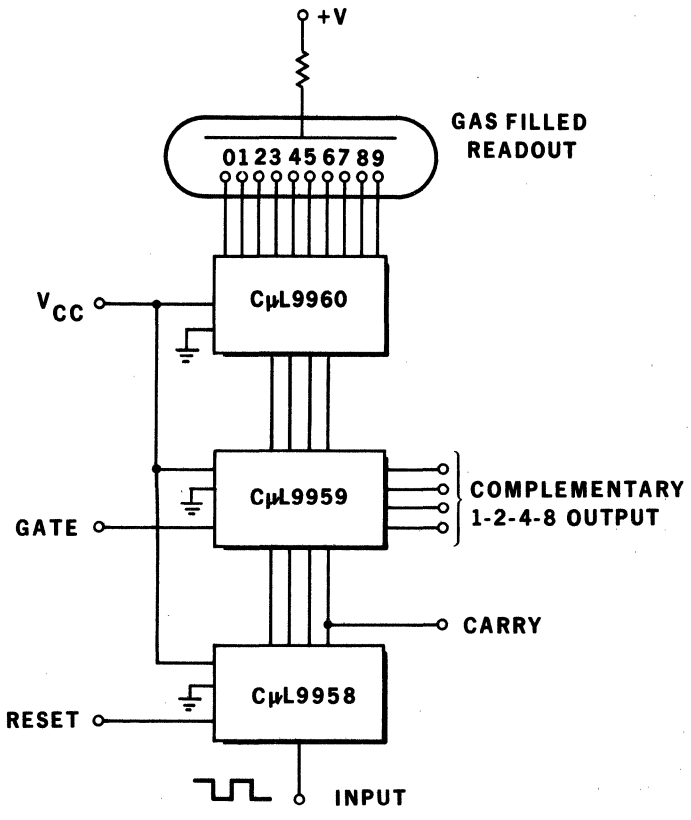
BLOCK DIAGRAM



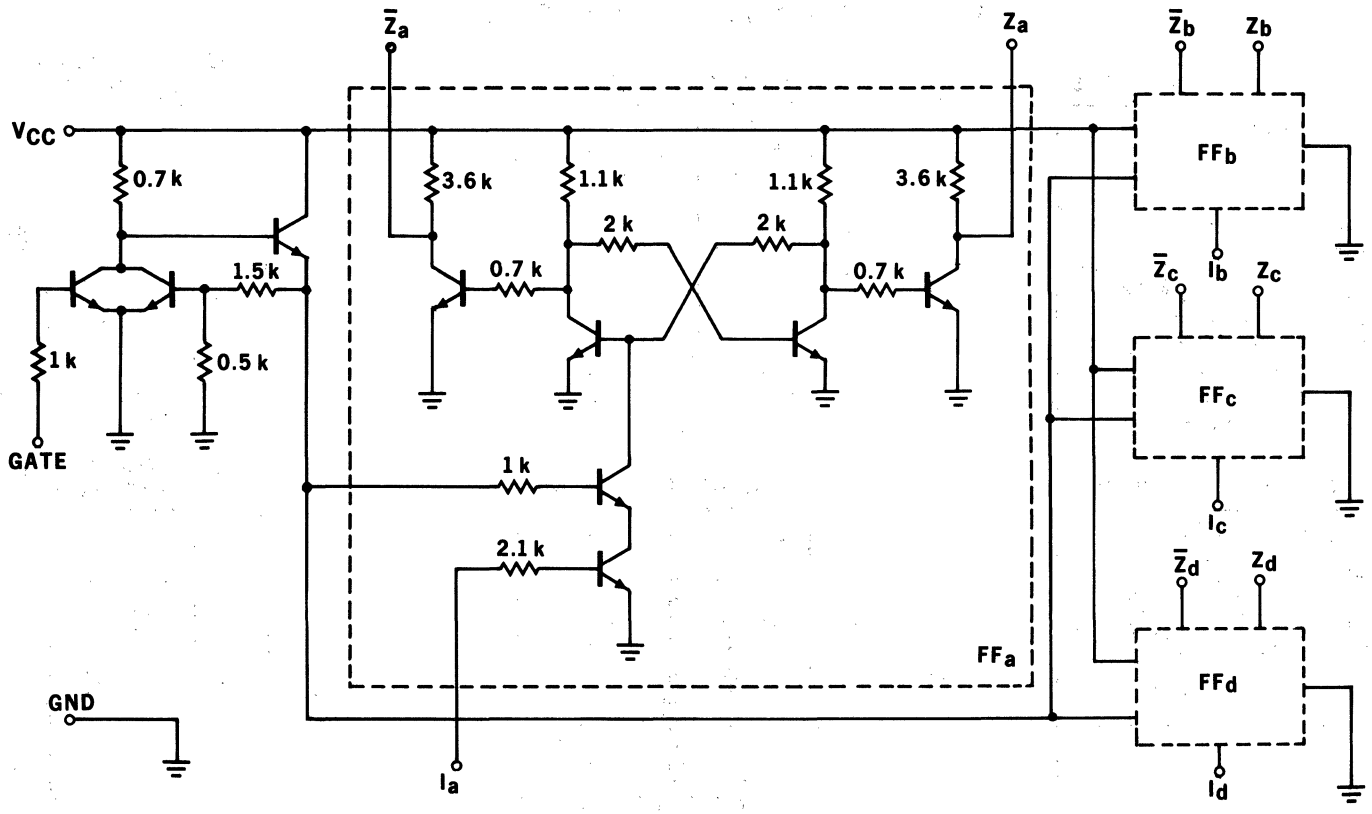
16 PIN DUAL IN-LINE PACKAGE (TOP VIEW)



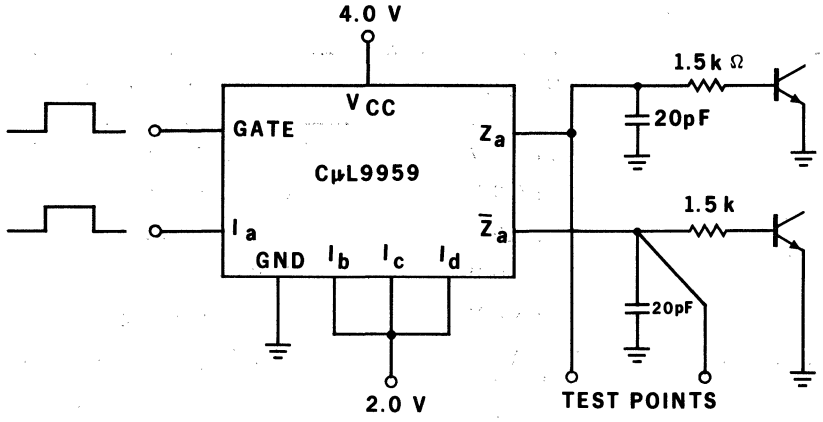
TYPICAL APPLICATION



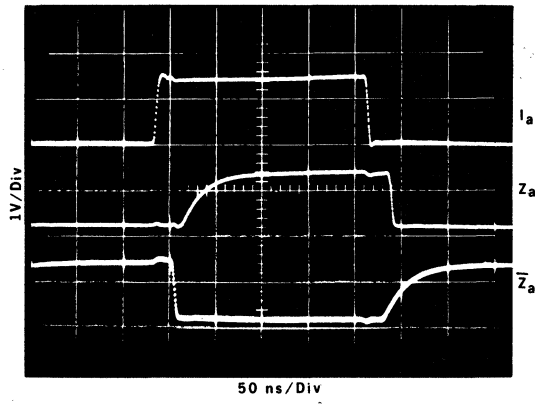
SCHEMATIC DIAGRAM OF BUFFER STORAGE UNIT



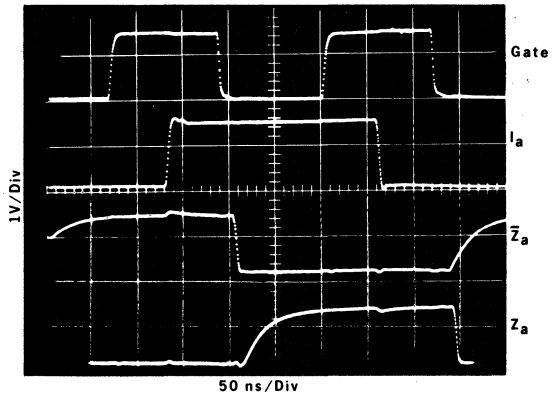
PROPAGATION DELAY



Delay from data Input to Output (Gate input low)

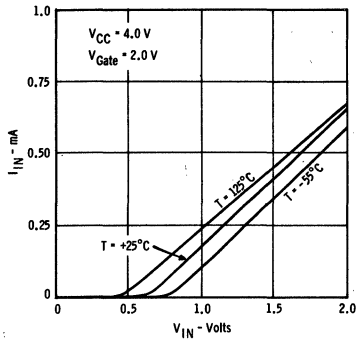


Delay from Gate Input to Output

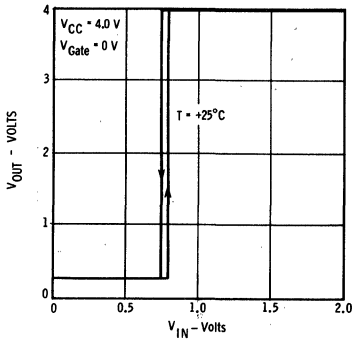


TYPICAL ELECTRICAL CHARACTERISTICS

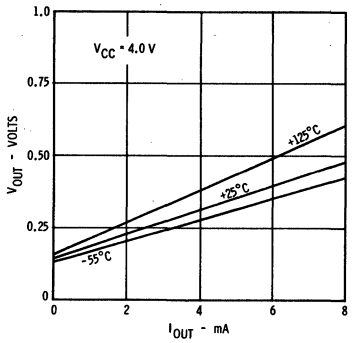
DATA INPUT CHARACTERISTIC



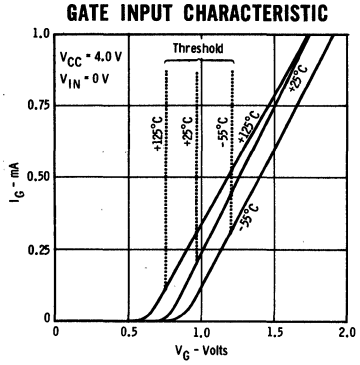
TRANSFER CHARACTERISTIC



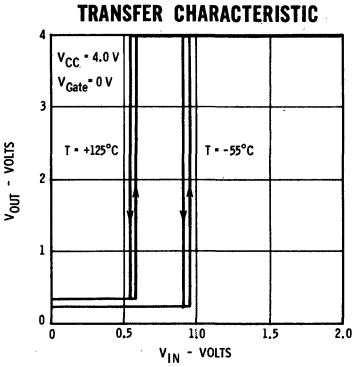
OUTPUT CHARACTERISTIC (OUTPUT LOW)



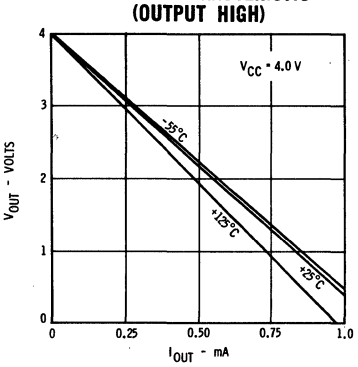
GATE INPUT CHARACTERISTIC



TRANSFER CHARACTERISTIC



OUTPUT CHARACTERISTIC (OUTPUT HIGH)



LOADING RULES FOR CμL9959

Driving Device	At V_{CC} of	Can Drive:
9959	3.3 to 5.0 V	2 9960 inputs ts
9959	3.3 to 5.0 V	4 Low Power RTμL loads
9959	3.3 to 5.0 V	1 RTμL load
9959	3.3 to 5.0 V	2 DTμL loads
9958	3.6 to 4.0 V	2 9959 data inputs
Full Range Low Power RTμL	4.0 V Min. * at -55°C	3 9959 data inputs or 1 9959 gate input
Industrial Range Low Power RTμL	3.6 V ± 10%	2 9959 data inputs
Full Range RTμL	3.0 ± 10%	10 9959 data inputs or 3 9959 gate inputs
Industrial Range RTμL	3.6 ± 10%	13 9959 data inputs or 5 9959 gate inputs
Full Range DTμL 6 K Family	4.5 V Min.	2 9959 data inputs or 1 9959 gate input
Full Range DTμL 2 K Family	4.5 V Min.	6 9959 data inputs or 2 9959 gate inputs

*See Low Power RTμL data sheet for details.

CμL9960

DECIMAL DECODER/DRIVER

COUNTING MICROLOGIC® INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The CμL 9960 Decoder/Driver is a monolithic silicon circuit which accepts 1-2-4-8 binary coded decimal inputs at integrated circuit signal levels and produces ten mutually exclusive outputs which can directly control the ionizing potentials of many gas filled cold cathode indicator tubes. The CμL 9960 is designed specifically for use with the CμL 9958 Decade Counter or CμL 9959 Buffer-Storage, but can be used with other integrated circuit types. Only true values are required as inputs thereby simplifying the connection with counters or other information sources.

RULES FOR USE OF CμL 9960

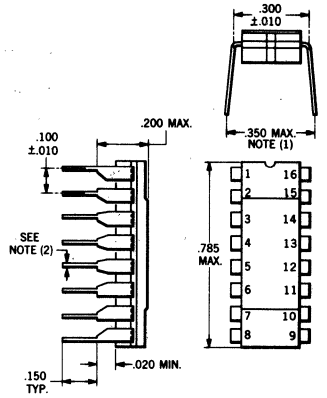
The principal intended use of the CμL 9960 is with industrial and ground support systems, from 0°C to +75°C ambient, and with operating V_{CC} from 3.3 to 5.5 volts. The lower limit of the temperature range may be extended to −55°C by raising the minimum V_{CC} to 4.0 volts.

ABSOLUTE MAXIMUM RATINGS (Note 1)

	Storage Temperature	−55°C to +125°C
	Operating Temperature	0°C to +75°C
	Supply Voltage (0°C to +75°C)	6 V
	Input Voltage	+4 V, −2 V
I_{OL}	Current into each Output Terminal (In the ON State)	15 mA
I_{OH}	Current into each Output Terminal (In the OFF State) (Notes 2 and 3)	0.6 mA

PHYSICAL DIMENSIONS

CμL PACKAGE OUTLINE



NOTES:

1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

PRODUCT CODE: U6B996079X

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Conditions
V_{CC}	Power Supply (Note 4)	3.3		5.5	V	
P_D	Power Consumption		45		mW	V_{CC} = 4.0 V Input High
V_{IH}	Input High	1.0			V	
V_{IL}	Input Low			0.4	V	
V_{OL}	ON Output Voltage (Note 2)			4.0	V	V_{IH} = 1.0 V, I_{OL} = 3 mA
V_{OH}	OFF Output Voltage	55			V	I_{OH} = 0.2 mA
I_{CO}	OFF Output Leakage Current			50	μA	V_{OUT} = 50 V

NOTES:

(1) These ratings are limiting values above which serviceability of unit may be impaired.

(2) Outputs in the OFF state Must not be left floating, they should be tied to V_{CC} through 10 kΩ if they are not connected to the cathodes of a readout tube.

(3) Total current through all 9 outputs in the OFF state must not exceed 1.5 mA.

(4) For operation using gas filled readout tubes requiring 6 to 10mA ON current, V_{CC} Min. = 4.0 V.

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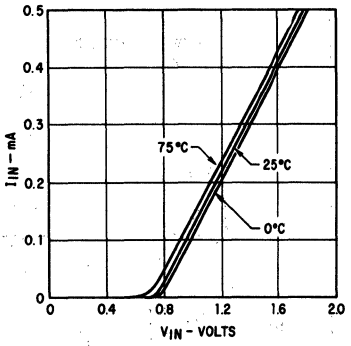
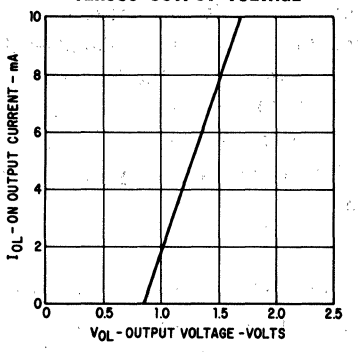
TYPICAL ELECTRICAL CHARACTERISTICS

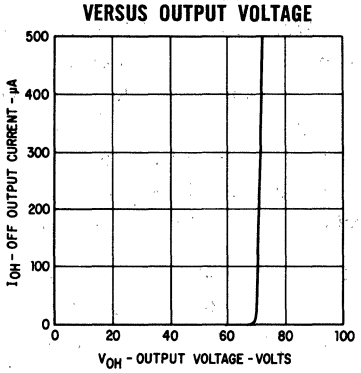
INPUT CHARACTERISTICS



ON OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



OFF OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



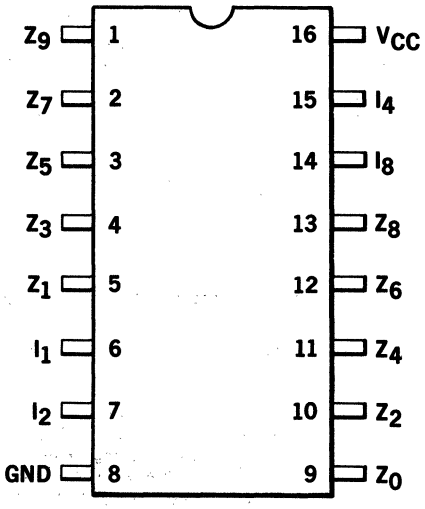
TRUTH TABLE

With the coding shown in the table only one of the outputs will be low or On at any time.

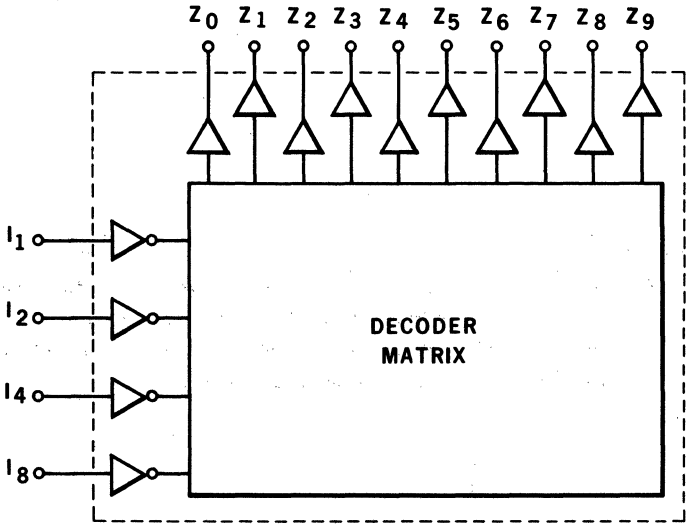
I_1	H	L	H	L	H	L	H	L	H	L
I_2	H	H	L	L	H	H	L	L	H	H
I_4	H	H	H	H	L	L	L	L	H	H
I_8	H	H	H	H	H	H	H	H	L	L
ON Output	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7	Z_8	Z_9

L = Low
H = High

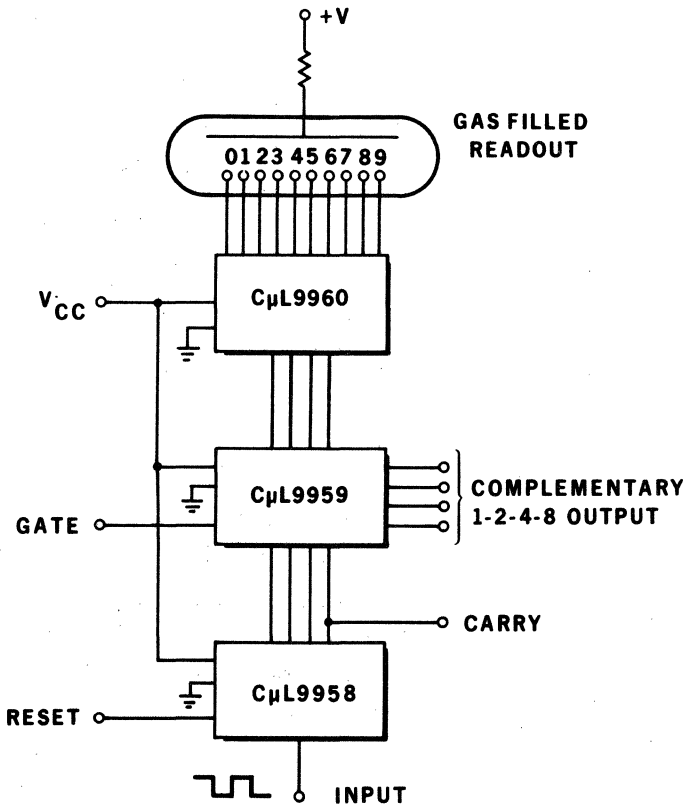
16 PIN DUAL IN-LINE PACKAGE
(Top View)

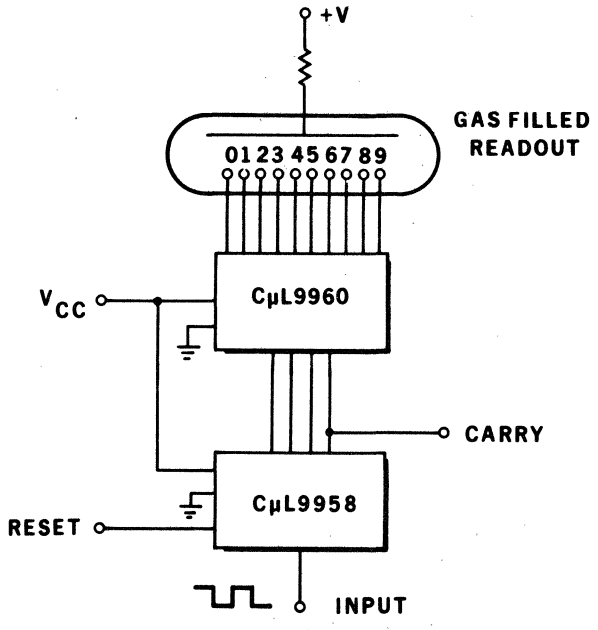


BLOCK DIAGRAM



TYPICAL APPLICATIONS





* The CμL9960 is suitable for driving all commercial available numeric gas filled readout tubes in which ON Cathode current does not exceed 10mA and **total** OFF Cathode leakages do not exceed 1.5mA. The Values of +V and R may be chosen following the readout tube manufacturers' specifications.

LOADING RULES FOR CμL9960

Driving Device	At V_{cc} of	
CμL9959	3.3 to 5.5 V	2 CμL9960 inputs
CμL9958	3.3 to 5.5 V	1 CμL9960 plus 1 CμL9958 Count Input
Industrial Range Milliwatt RTL	3.6 V ±10%	1 CμL9960
Industrial Range RTL	3.6 ±10%	6 CμL9960
Industrial Range DTμL 6K Family	4.5 V Min.	1 CμL9960
Industrial Range DTμL 2K Family	4.5 V Min.	3 CμL9960

CμL9989

4-BIT BINARY COUNTER

COUNTING MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The CμL9989 is a Ripple Counter using 8421 binary weighted count sequence consisting of four cascaded binary triggered flip-flops. Provision is made for clearing and pre-setting any one of the possible binary states. The monolithic structure employs only resistors and transistors and is manufactured with Fairchild Planar* Epitaxial process to assure maximum performance and reliability.

The CμL9989 counter is designed to operate in the 0°C to 75°C temperature range with nominal power supply voltage of 3.6 to 5.5 volts.

The CμL9989 is available in the hermetically sealed 14 pin Dual In-Line ceramic package (TO-116), and in the 8 pin modified TO-5 metal can (TO-99).

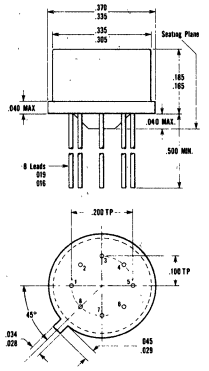
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−55°C to +150°C
Voltage at pin 7 (0°C to +75°C) (TO-99)	+6.0 V
Count Input Pin Voltage	+4.0 V, −2.0 V
Reset Input Pin Voltage	+4.0 V, −2.0 V
Current into Each Output Terminal	±5.0 mA

ELECTRICAL CHARACTERISTICS (0 - 75°C Free Air Temperature unless otherwise stated)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Supply Voltage—V_{CC}	3.6		5.5	Volts	See Loading Rules
Power Dissipation		300	385	mW	V_{CC} = 5.5 Volts, 25°C
Power Dissipation		132		mW	V_{CC} = 4.0 Volts, 25°C
Count Input—Low—V_{ILC}			0.45	Volts	75°C
Count Input—High—V_{IHC}	1.2			Volts	25°C
Count Input Current		210	330	μA	25°C, V_{IHC} = 1.2 Volts
Count Input Pulse Width—High	40			ns	25°C
Count Input Slope—Positive Going		1.0		v/μs	25°C
Max. Freq. of Input Count Pulses	10	15		MHz	Z_1, Z_2, Z_4, One Standard Load Z_8, Two Standard Loads
Reset Input—Low—V_{ILR}			0.45	Volts	75°C
Reset Input—High—V_{IHR}	1.2			Volts	25°C
Reset Input Current		1.45	2.30	mA	25°C, V_{IHR} = 1.2 Volts
Reset Input Pulse Width—High		220		ns	Z_1, Z_2, Z_4, One Standard Load Z_8, Two Standard Loads, V_{CC} = 5.5 Volts
Output—Low—V_{OL}			0.45	Volts	V_{CC} = 5.5 Volts, I_{OL} = 0.4 mA Load
Output—High—V_{OH}	1.2			Volts	V_{CC} = 3.5 Volts, I_{OH} = −0.7 mA
Max. Delay From Count Input To Z_8 Output		90	120	ns	V_{CC} = 4.0 Volts, Z_1, Z_2, Z_4 One Standard Load, Z_8 Two Standard Loads 25°C

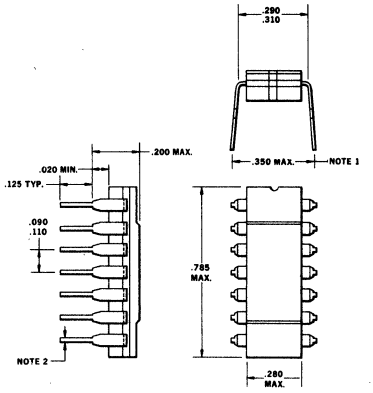
PHYSICAL DIMENSIONS
(TO-99)



NOTES: Dimensions as per latest JS-10 committee.
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 0.95 grams.

(PRODUCT CODE U5B998979X)

TYPICAL DUAL IN-LINE PACKAGE
(TO-116)



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

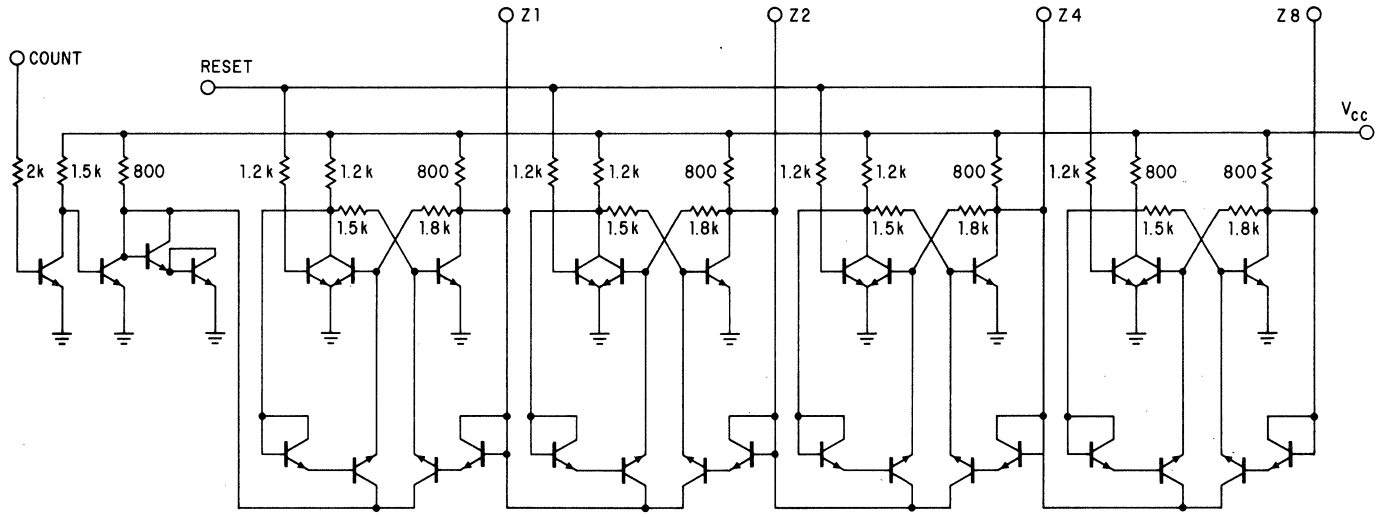
(PRODUCT CODE U6A998979X)

*Planar is a patented Fairchild process.

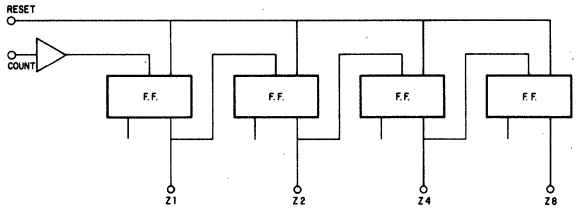
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

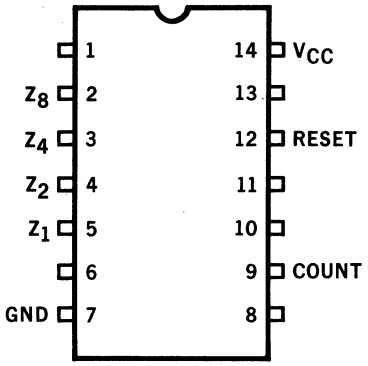
SCHEMATIC DIAGRAM



LOGIC DIAGRAM



14 PIN DUAL IN-LINE CONNECTION DIAGRAM (Top View)



TO-99 CONNECTION DIAGRAM (Top View)

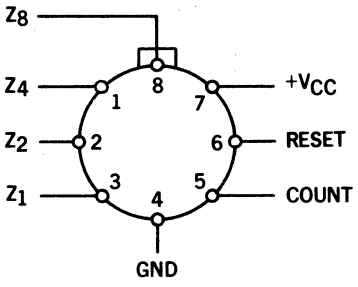
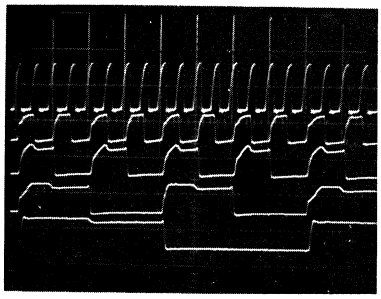


TABLE OF OUTPUT STATES

COUNT (H = High, L = Low)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Z_1	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
Z_2	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L
Z_4	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L
Z_8	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L

INPUT/OUTPUT WAVEFORM



RESET/PRESET

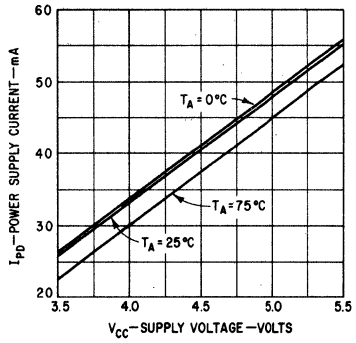
The circuit is reset to count 0 (all outputs high) with a high level at the reset input pin.

To preset an arbitrary count:

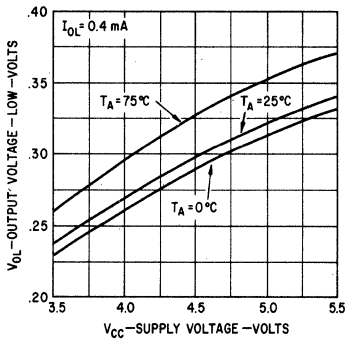
1. Reset to count 0 and then return the reset pin to a low level.
2. Ground (below 0.45 V) the appropriate outputs.

TYPICAL ELECTRICAL CHARACTERISTICS

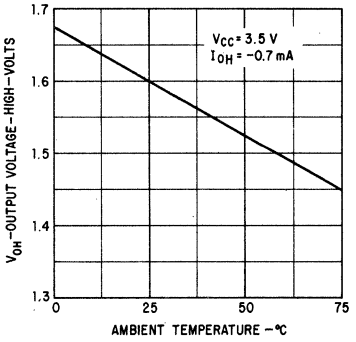
POWER SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



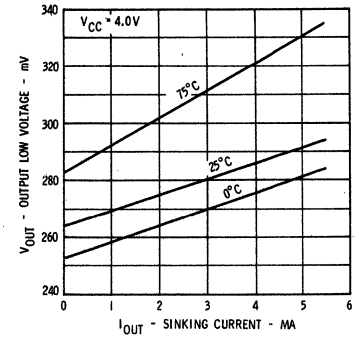
OUTPUT VOLTAGE—LOW VERSUS SUPPLY VOLTAGE



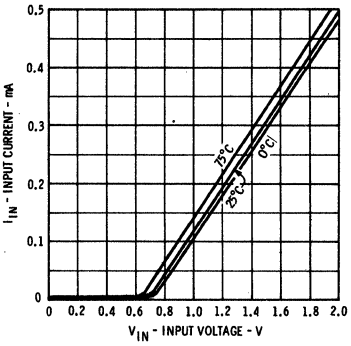
OUTPUT VOLTAGE—HIGH VERSUS TEMPERATURE



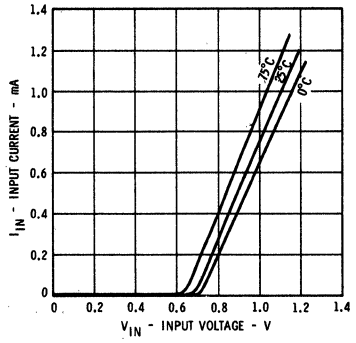
OUTPUT CHARACTERISTICS (OUTPUT LOW)



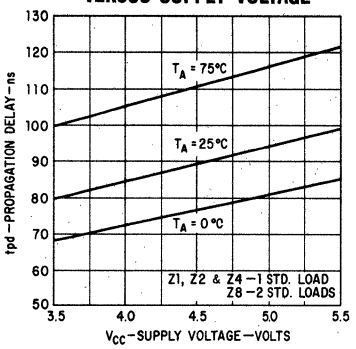
COUNT INPUT CHARACTERISTIC



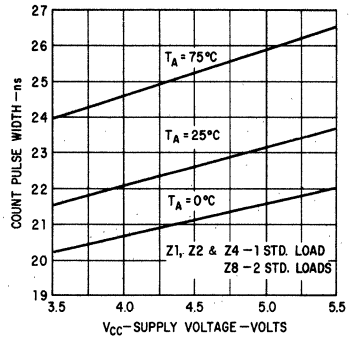
RESET INPUT CHARACTERISTIC



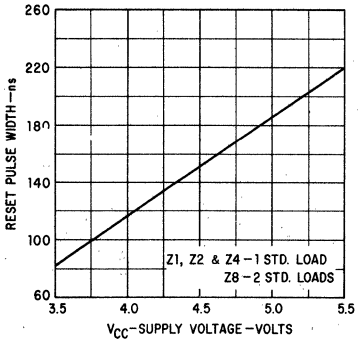
PROPAGATION DELAY—t_{pd} VERSUS SUPPLY VOLTAGE



COUNT PULSE WIDTH VERSUS SUPPLY VOLTAGE



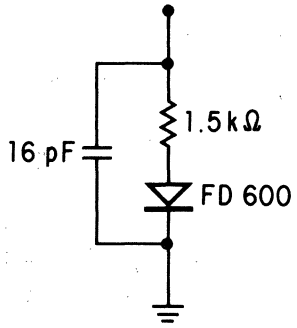
RESET PULSE WIDTH VERSUS SUPPLY VOLTAGE



LOADING RULES

DRIVING DEVICE	CAN DRIVE	AT V_{CC} RANGE OF
CμL9989		
Z_1, Z_2, Z_4	Open	
Z_8	1 Standard Load	3.6 to 5.5 Volts
CμL9989		
Z_1, Z_2, Z_4	1 Standard Load	
Z_8	2 Standard Loads	4.0 to 5.5 Volts
CμL9989		
Z_1, Z_2, Z_4	2 Standard Loads	
Z_8	4 Standard Loads	5.0 to 5.5 Volts
Industrial Range		
Milliwatt RTL	1 CμL9989 Count	3.6 to 3.96 Volts
Industrial Range	6 CμL9989 Count	
RTL	1 CμL9989 Reset	3.6 to 3.96 Volts
Industrial Range		
DTL 6K Family	1 CμL9989 Count	4.5 to 5.5 Volts
Industrial Range	3 CμL9989 Count	
DTL 2K Family	1 CμL9989 Reset	4.5 to 5.5 Volts

One Standard Load, worst case, is defined for testing purposes as shown in the figure below.



The following are defined as One Standard Load:

CμL9989 Count Input
CμL9958 Count Input
CμL9959 Data Input
CμL9960 Data Input
LP-RTL GATE INPUT

CTμL9952

DUAL 2-INPUT NOR GATE

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

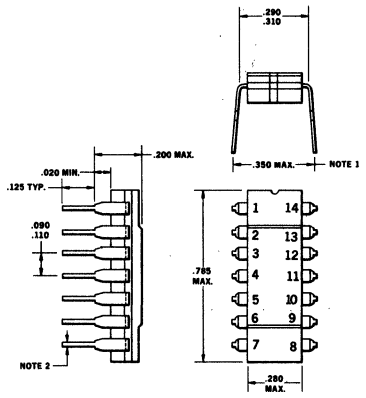
GENERAL DESCRIPTION–The CTμL 9952 Dual 2-Input Inverter Gate provides logic gating at its input and output terminals. Compatible with all other CTμL elements, the output can be tied to any other element to perform the wired OR function.

The 9952 may be used to set and restore the system logic levels; having a high noise immunity, it can drive and be driven by a number of cascaded CTμL AND-OR gates. The following data, stressing worst case conditions, plus 100% testing by Fairchild Semiconductor, will assure the designer of proper worst case performance in his own system.

The CTμL 9952 is designed for general purpose industrial and commercial usage where high speed logic is required. It is packaged in the versatile Dual-In-Line* package, which is a hermetically sealed ceramic package intended for low-cost insertion techniques.

TYPICAL DUAL IN-LINE* PACKAGE

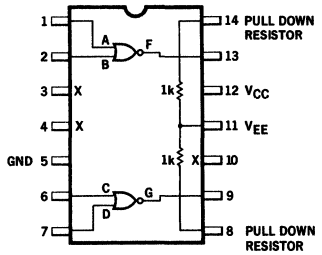
in accord with JEDEC (TO-116) outline



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

CONNECTION DIAGRAM

TOP VIEW



POSITIVE LOGIC $F = \overline{A+B}$
$G = \overline{C+D}$

NOTE: X = NOT CONNECTED

FEATURES

- **POWER SUPPLIES ARE +4.5 V ±10% AND −2.0 V ± 10%**
- **HIGH FAN-OUT CAPABILITY — 12**
- **TEMPERATURE RANGE — +15°C TO +55°C**
- **OPTIONAL PULLDOWN 1.0 k RESISTOR FOR OPTIMUM SPEED**
- **LOW POWER DISSIPATION**
- **LOW PROPAGATION DELAY — 7.0 ns TYPICAL**
- **LOGIC SWING OF 3.0 V**
- **HIGH NOISE IMMUNITY > 1.0 V AT FAN-OUT = 12**

PURCHASING INFORMATION

Use the ten-letter code U6A995279X for ordering purposes.

All units are marked CTμL-995279 and date code unless otherwise specified.

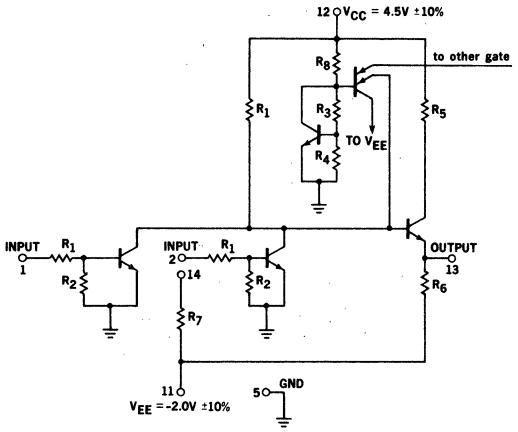
*Fairchild Patent Pending

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

CTμL-9952 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



NOTE: Only one 2-input inverter gate shown.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Maximum Current in or out of a pin	100 mA
Maximum Chip Temperature	+150°C
Maximum Power Dissipation	1.0 Watt
Maximum Voltage Applied to any Input Pin	10 Volts
Maximum Negative Voltage Applied to any Input Pin	−4.0 Volts
Maximum Voltage Applied to Output Pin	6.0 Volts

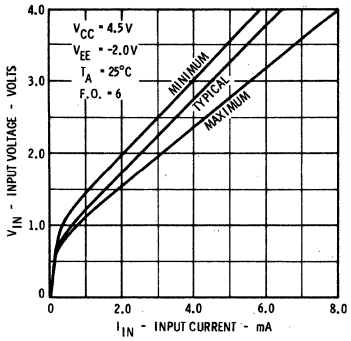
DC TESTS

TEST (at T_A = 25°C)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.(1)	UNITS	V_{CC}	V_{EE}	LOAD TO V_{EE}	COMMENTS
Output ONE Level	2.35	2.50		Volts	4.05 V	−2.20 V	F.O.(2) = 12	Inputs to +0.8 V sequentially. Guarantees input low threshold >0.80 V; and output ONE level >2.35 V.
Output ZERO Level		−0.50	−0.36	Volt	4.95 V	−1.80 V	F.O. = 1	Inputs to 1.25 V sequentially. Guarantees input high threshold <1.25 V; output ZERO level <−0.36 V.
Output ONE Level		2.75	2.90	Volts	4.95 V	−1.80 V	F.O. = 1	Inputs to −0.70 V simultaneously. Guarantees output never more positive than 2.90 V.
Input Current	4.20	5.30	6.86	mA	4.05 V	−1.80 V	No load	Inputs to 3.5 V simultaneously. Guarantees input loading <1.5 AND gate loads.
Output Resistor	1.6 k	2.0 k	2.4 k	Ohms	4.05 V	−2.20 V	No load	Inputs to −0.7 V simultaneously. (Outputs to 3.5 V sequentially.) Guarantees output OR tie <1.0 AND-OR gate loads.
Input Pulldown Resistor	0.8 k	1.0 k	1.2 k	Ohms	4.05 V	−2.20 V	No load	Resistor to 3.50 V sequentially. Guarantees 1 k resistor available for input pulldown is within 20% of nominal value.
Output Falling Delay, t_{df}		6	12	ns	4.50 V	−2.00 V	F.O. = 12	See t_{PD} Test Circuit
Output Rising Delay, t_{dr}		8	14	ns	4.50 V	−2.00 V	F.O. = 12	See t_{PD} Test Circuit
Positive Supply Current	18.5	30	36.2	mA	4.95 V	−2.20 V	No load	Inputs to +3.50 V simultaneously. Tests internal resistors to be no more than ±20% from nominal.
Negative Supply Current	6.75	8	14.8	mA	4.95 V	−2.20 V	No load	Inputs to −0.70 V simultaneously. Test internal resistors to be no more than ±20% from nominal.

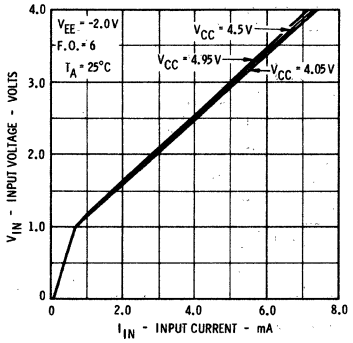
NOTES: (1) "Maximum" means "no more positive than"
(2) F.O. = Fan-Out: F.O. = 12 equivalent to 133 Ω to −2.20 V under worst case conditions.
F.O. = 1 equivalent to 2.4 kΩ to −1.80 V under worst case conditions.

INPUT CHARACTERISTICS

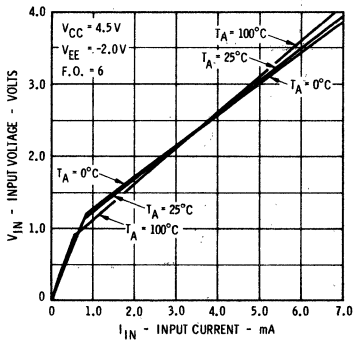
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE

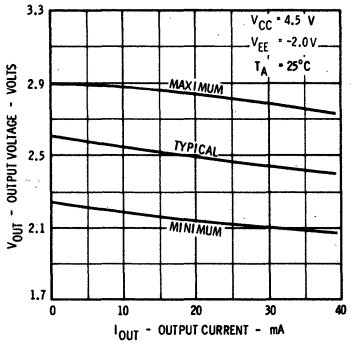


AS A FUNCTION OF TEMPERATURE

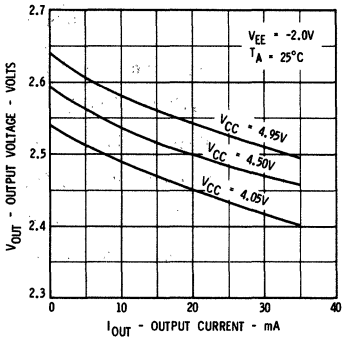


OUTPUT CHARACTERISTICS

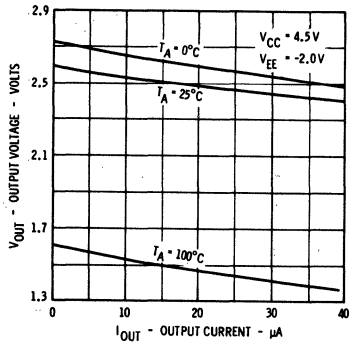
TOLERANCE VARIATION OF PARAMETERS



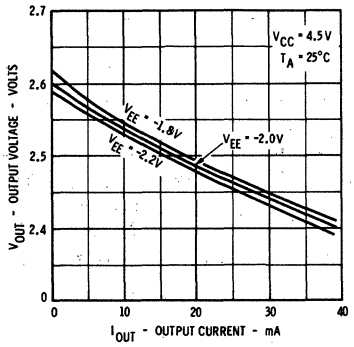
AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE



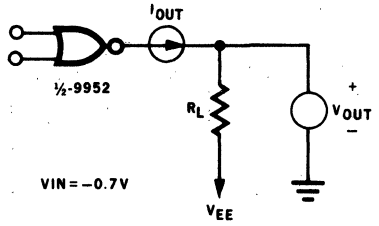
AS A FUNCTION OF TEMPERATURE



AS A FUNCTION OF NEGATIVE SUPPLY VOLTAGE

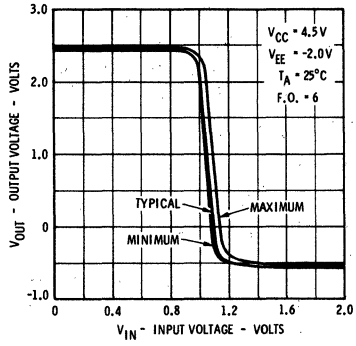


SCHEMATIC DIAGRAM

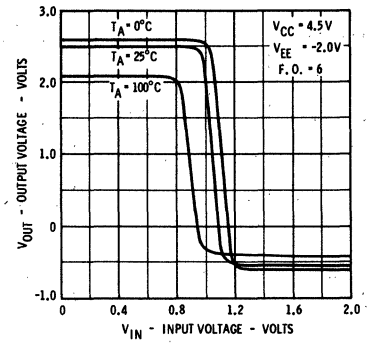


TRANSFER CHARACTERISTICS

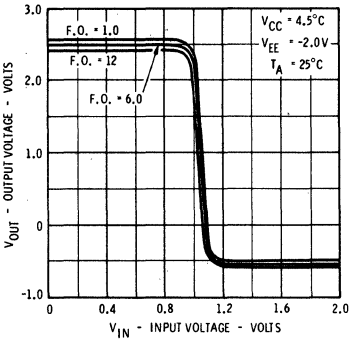
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF TEMPERATURE

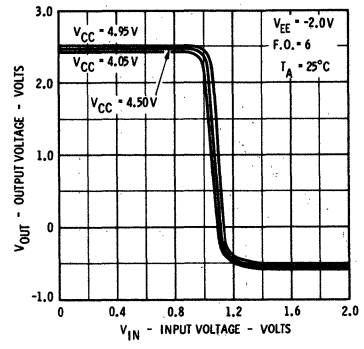


AS A FUNCTION OF FAN-OUT

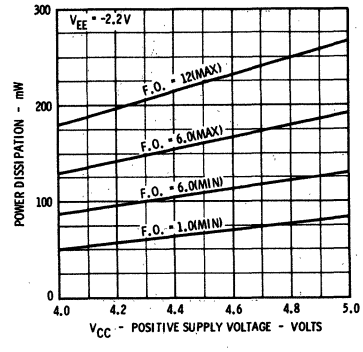


NOTE: Variation of V_{EE} does not alter transfer characteristics.

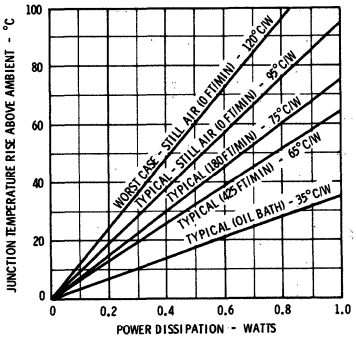
AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE



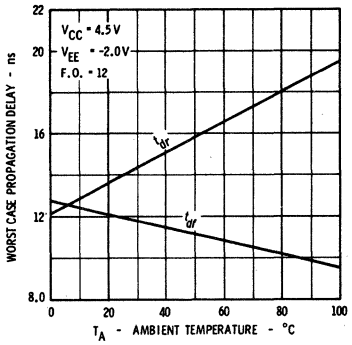
POWER DISSIPATION VERSUS POSITIVE SUPPLY VOLTAGE



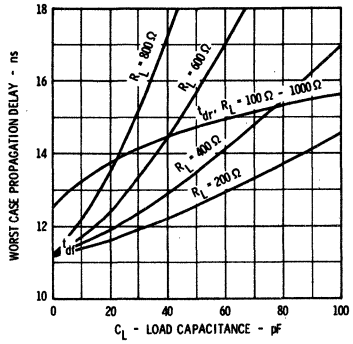
WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION



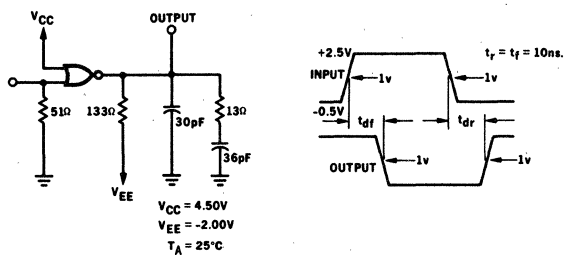
WORST CASE PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



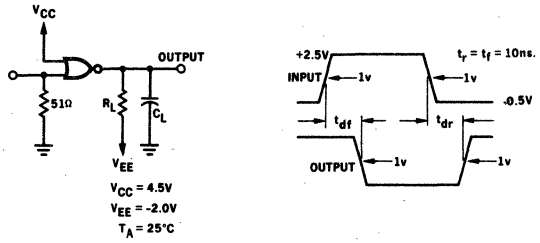
WORST CASE PROPAGATION DELAY VERSUS LOAD CAPACITANCE AS A FUNCTION OF LOAD RESISTANCE



t_{PD} TEST CIRCUIT



t_{PD} TEST CIRCUIT FOR ABOVE



APPLICATION INFORMATION

The electrical specification tests performed under the conditions set, emphasize the worst case results and should be considered as conservative limits. Throughout this data sheet, WORST CASE should be interpreted as using power supplies, internal resistors, transistor parameters and external loads having extreme loads chosen in a manner to guarantee proper operation under worst case conditions.

LOADING RULES: Each input to the CTμL 9952 represents 1.5 unit loads.
(One unit load is defined as an input to the CTμL AND-OR gate.)

a) Connecting the 1.0 kΩ pulldown resistor to the input adds two unit loads to the fan-in.

b) Connecting the 1.0 kΩ pulldown resistor to the output reduces the fan-out by two unit loads.

c) Each wired-OR connection reduces the fan-out by one.

PULLDOWN RESISTOR: Two pulldown 1.0 kΩ resistors are built into the package with one end tied to the negative power supply (V_{EE}). Connecting the 1.0 kΩ resistor to the CTμL 9952 input will improve the turn-off characteristics and speed up the output rising propagation delay. When the input of the CTμL 9952 is driven by four or more AND-OR gates, there is no advantage in connecting the 1.0 kΩ resistor to the same input. The pulldown resistor may also be connected to the CTμL 9952 output. This will improve the output falling propagation delay when low fan-out is used.

WIRED OR: A powerful feature of the CTμL 9952 inverter is that the output may be tied together with the output of any other element in the CTμL family to form the positive OR function at the tie point, thus achieving two logic functions without additional propagation delay.

INTERFACING: The CTμL 9952 inverter gate serves as an excellent interfacing link between external signals coming from other logic forms or peripheral equipment and the CTμL family.

NOISE IMMUNITY: The CTμL 9952, having excellent noise immunity under maximum loading and worst case conditions, is used primarily to restore logic levels degraded after passing through several CTμL AND-OR gates.

HIGH SPEED CONSIDERATIONS: The high-speed logic operation available using CTμL requires that care be exercised in packaging and interconnection techniques. Normally logic circuits using emitter followers as drivers have a tendency to oscillate when driven by high-speed pulse signals. Each CTμL 9952 includes a clamping network so designed that it reduces ringing at high-speed operation. These features eliminate the necessity for the use of strip lines or coaxial cables for all but the longest lines. However, care must still be exercised in the layout of printed circuit boards. Any one line over 12″ in length tied to a gate output should be terminated in a 200 Ω resistor to ground. Such a 200 Ω resistor approximates the characteristic impedance of the back panel wiring and is considered equivalent to a fan-out of 4.

SHORT CIRCUIT PROTECTION: The CTμL 9952 inverter gate output is protected by a limiting resistor at the output and may sustain prolonged short circuit to ground with V_{CC} not greater than 5.0 V. Excessive destructive heat may develop when more than one output in a single package is short circuited to ground. In general, short circuiting the output should be avoided.

CTμL 9953-9955 • 9964-9966 • 9971-9972 AND-OR GATES

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The Fairchild CTμL AND-OR gate is a PNP-NPN complementary logic circuit which provides the system designer with the basic tools for designing extremely fast, proven, low cost synchronous systems.

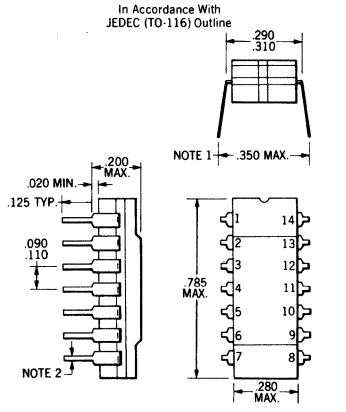
The following data, stressing worst case conditions, plus 100% testing by Fairchild for a minimum fanout of 11 and a maximum propagation delay of 4.5 nseconds at full fanout at 25°C, will assure the designer of proper worst case performance in his own system.

The AND-OR gate is basically a cascade connected PNP-NPN complementary non-saturating transistor pair. The output transistor is an emitter follower having virtually no threshold level. Therefore, there is no delay in output response due to input charging to threshold voltage, no stored charge to remove, negligible emitter-base transition charge and no collector-base transition capacity multiplication. Thus, typically 3 nseconds delays are obtainable at full fanout without the necessity of fast rise and fall time. This means conventional back panel wiring may be used with substantial reduction in inductive and capacitive noise usually generated by threshold circuits. The emitter follower low output impedance coupled with the high input impedance contributes to the large fanout and exceptional performance in the presence of stray capacitance.

CTμL circuits are packaged in the versatile JEDEC TO-116 DUAL-IN-LINE packages which are hermetically sealed ceramic units intended for low cost insertion techniques.

PHYSICAL DIMENSIONS

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES:

- **Power supplies are 4.5 V ±10% and −2.0 V ±10%.**
- **High fanout capability**
- **Temperature range +15°C to +55°C**
- **Low power dissipation**
- **Low propagation delay — 3.0 ns typical**
- **Logic swing of 3.0 V**

PURCHASING INFORMATION:

Description	Code	Marking
CTμL9953 — 2-2-3 Input AND-OR Gate (three gates in one package)	U6A995379X	CTμL95379
CTμL9954 — Dual 4-Input AND-OR Gate (two gates in one package)	U6A995479X	CTμL95479
CTμL9955 — Dual Output 8-Input AND-OR Gate	U6A995579X	CTμL95579
CTμL9964 — 3-3-1 Input AND-OR Gate (three gates in one package)	U6A996479X	CTμL96479
CTμL9965 — Quad 1-Input AND-OR Gate	U6A996579X	CTμL96579
CTμL9966 — Quad 2-Input AND-OR Gate (with three outputs)	U6A996679X	CTμL96679
CTμL9971 — Quad 2-Input AND-OR Gate (with two outputs)	U6A997179X	CTμL97179
CTμL9972 — Quad 2-Input AND-OR Gate (with three outputs, all pull down resistors omitted)	U6A997279X	CTμL97279

Use the ten letter code for ordering purposes.
All units are marked as above unless otherwise specified.

*Planar is a patented Fairchild process.

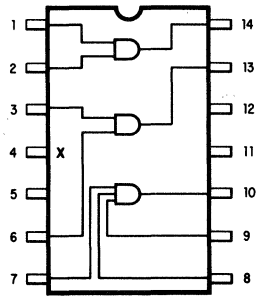
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

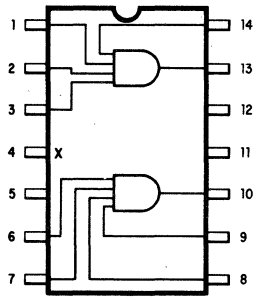
FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

PIN CONFIGURATION AND LOGIC DIAGRAM
(TOP VIEW)

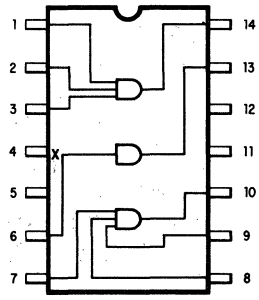
CTμL9953



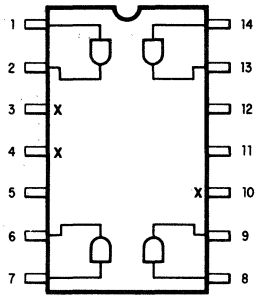
CTμL9954



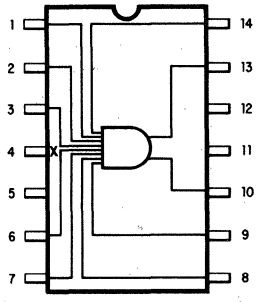
CTμL9964



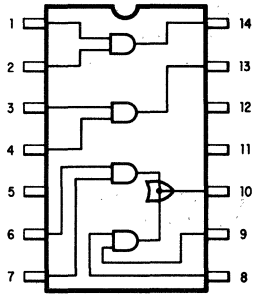
CTμL9965



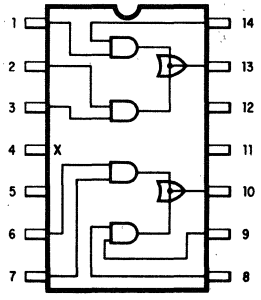
CTμL9955



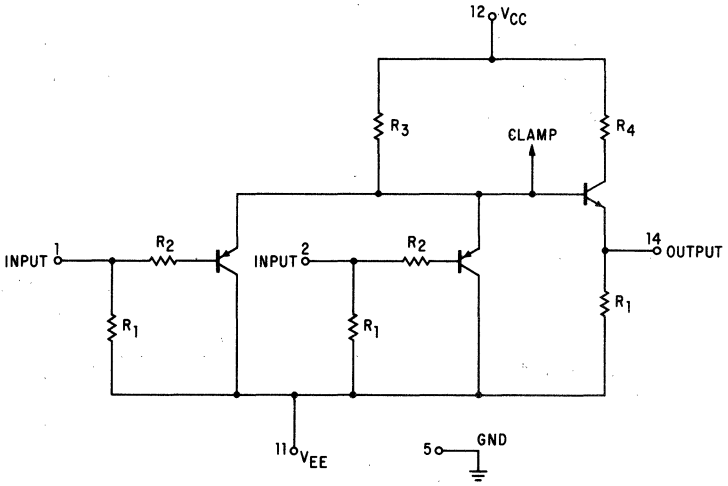
CTμL9966/9972[1]



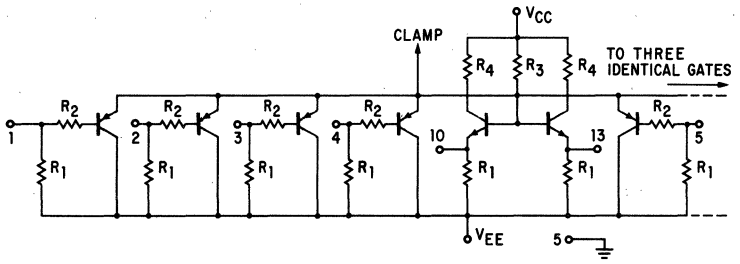
CTμL9971

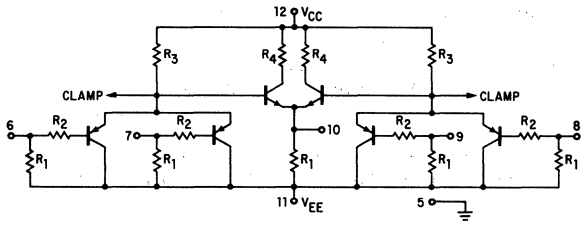


CIRCUIT DIAGRAM

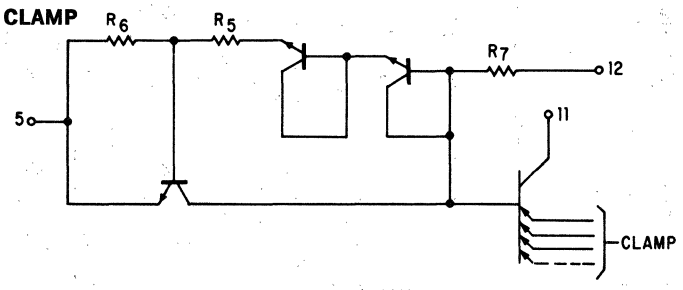


NOTE: Only one representative AND-OR gate shown.





NOTE: One AND/OR gate shown.



NOTES:
(1) R_1 deleted for CTμL 19972
X = Not connected.

Pin 12: $V_{CC} = 4.5\ V \pm 10\%$
Pin 11: $V_{EE} = -2.0\ V \pm 10\%$
Pin 5: Ground

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

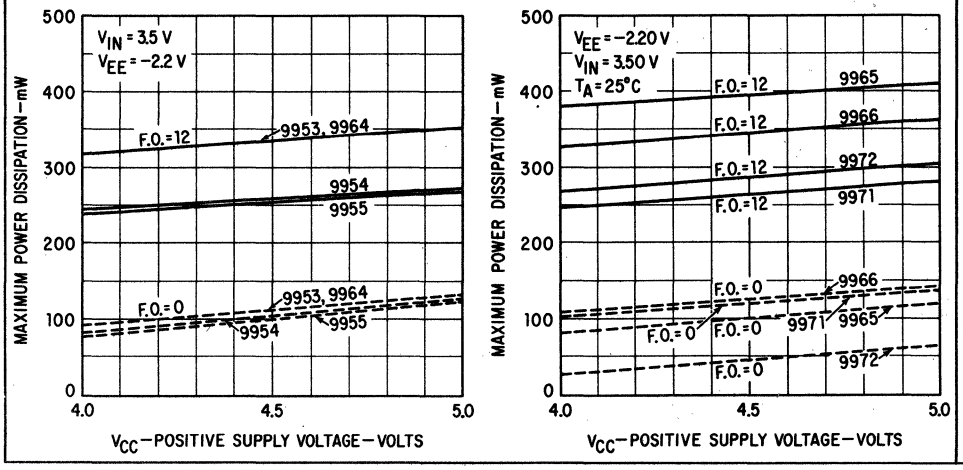
Maximum current in or out of a pin	100 mA	Maximum negative voltage applied to any input pin (output open)	−8.0 Volts
Maximum chip temperature	150°C		
Maximum power dissipation	1.0 Watt	Maximum voltage applied to output pin (input grounded)	5.0 Volts
Maximum voltage applied to any input pin	10 Volts		

D.C. TESTS

TESTS (at $T_A = 25°C$)	LIMITS MIN.	TYP.	MAX.(1)	UNITS	CONDITIONS V_{CC}	V_{EE}	LOAD TO V_{EE}	COMMENTS
ONE level offset		200	270	mV	4.05	−2.20	F.O. = 11(2)	Inputs sequentially to +2.25 V, other inputs to 3.5 V, pin 5 open. Worst case offset assuming ±10% supplies and W.C. parameters. Gates with lower input voltage will have smaller offsets; see fig. 12.
ZERO level offset		−120	−195	mV	4.95	−1.80	F.O. = 1	Worst case offset assuming ±10% supplies and min. fanout. Inputs sequentially to −0.36 V, other inputs to 3.50 V; pin 5 to GND.
Clamp level	2.10	2.30		Volts	4.05	−2.20	F.O. = 11	Inputs simultaneously at 3.5 V, pin 5 to GND. Tests minimum clamp level.
Clamp level		2.60	2.90	Volts	4.95	−1.80	No load	Inputs simultaneously to 3.5 V, pin 5 to GND. Tests max. possible clamp level to check existence of clamp.
Input resistors	1.6 k	2.0 k	2.4 k	Ω	4.05	−1.80	No load	Inputs to 3.5 V sequentially, other inputs to −0.7 V, sense input current. Tests min. R for max. loading, max. R for adequate turn-off and line termination.
Output resistors	1.6 k	2.0 k	2.4 k	Ω	4.05	−1.80	No load	Outputs to 3.5 V sequentially, inputs to −0.7 V, sense output current. Tests min. R for max. wired OR loading, max. R for adequate turn off.
Positive supply current, I_{PS}		I_{PS}	$I_{PS\ max}$	mA	4.95	−2.20	No load	Inputs to −0.7 V simultaneously.
Negative supply current, I_{NS}		$-I_{NS}$	$-I_{NS\ max}$	mA	4.95	−1.80	No load	Inputs to +3.5 V simultaneously.
Rising Propagation Delay, t_{dr}		3.5	4.5	ns	4.50	−2.00	F.O. = 12	See t_{pd} test circuit, page 6.
Falling Propagation Delay, t_{df}		3.0	4.0	ns	4.50	−2.00	F.O. = 12	See t_{pd} test circuit, page 6.

NOTES: (1) "Maximum" means "no more positive than"
(2) F.O. = Fan-Out: F.O. = 11 equivalent to 145 Ω to −2.20 V under worst case conditions
F.O. = 1 equivalent to 2.4 k to −1.80 V under worst case conditions

MAXIMUM POWER DISSIPATION VS. POSITIVE SUPPLY VOLTAGE

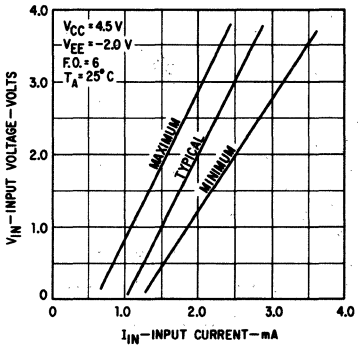


POSITIVE AND NEGATIVE CURRENT DRAIN

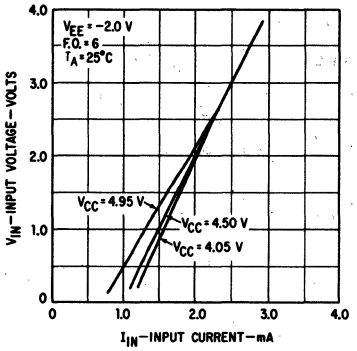
CTμL Element	$I_{PS\ typ}$	$I_{PS\ max}$	$I_{NS\ typ}$	$I_{NS\ max}$	UNITS
9953	22.0	27.7	33.0	41.4	mA
9954	16.5	20.5	33.0	39.6	mA
9955	11.5	14.3	30.0	37.1	mA
9964	22.0	27.7	33.0	41.4	mA
9965	28.0	34.9	29.0	36.0	mA
9966	27.0	33.9	38.0	47.5	mA
9971	26.0	32.9	36.0	44.6	mA
9972	12.0	20.0	5.0	10.0	mA

INPUT CHARACTERISTICS

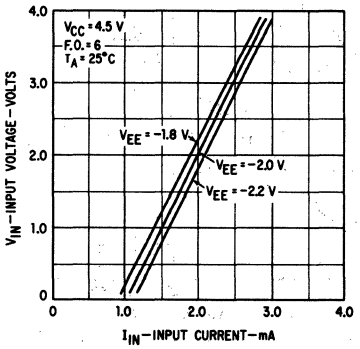
TOLERANCE VARIATION



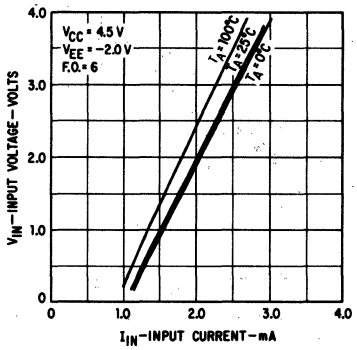
AS A FUNCTION OF V_{CC}



AS A FUNCTION OF V_{EE}

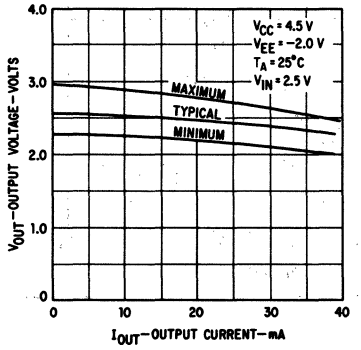


AS A FUNCTION OF TEMPERATURE

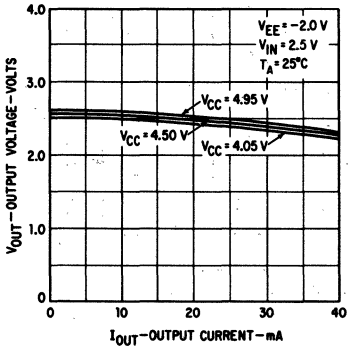


OUTPUT CHARACTERISTICS

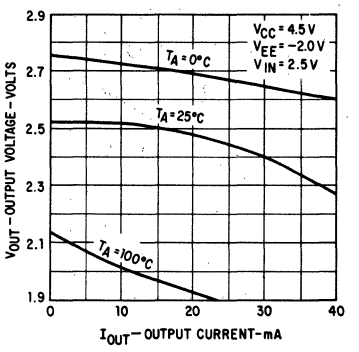
TOLERANCE VARIATION



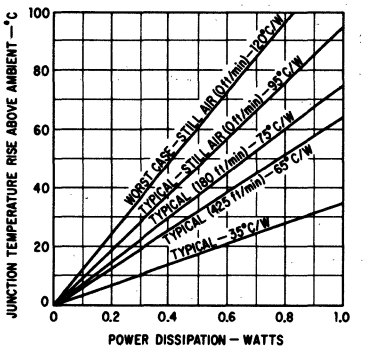
AS A FUNCTION OF V_{CC}



AS A FUNCTION OF TEMPERATURE

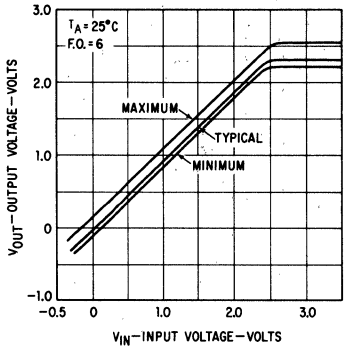


WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION

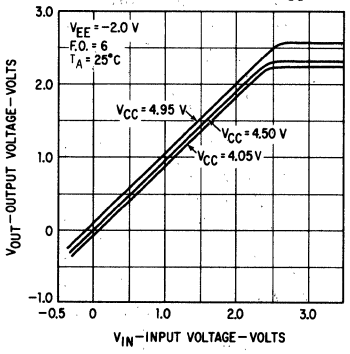


TRANSFER CHARACTERISTICS

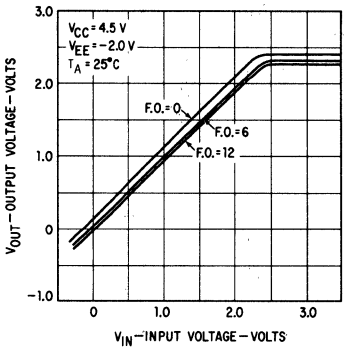
TOLERANCE VARIATION



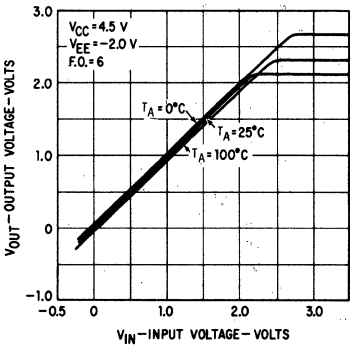
AS A FUNCTION OF V_{CC}



AS A FUNCTION OF FAN OUT

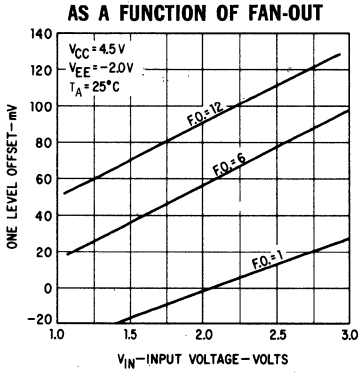


AS A FUNCTION OF TEMPERATURE

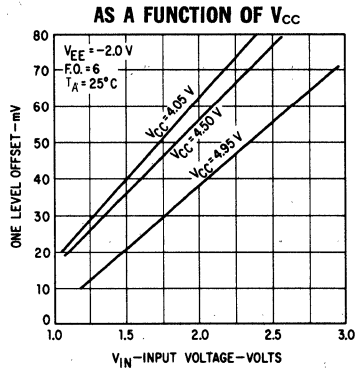


"ONE" LEVEL OFFSET

AS A FUNCTION OF FAN-OUT

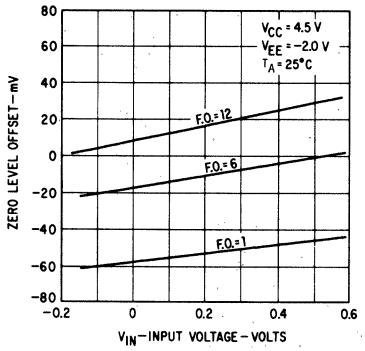


AS A FUNCTION OF V_{CC}

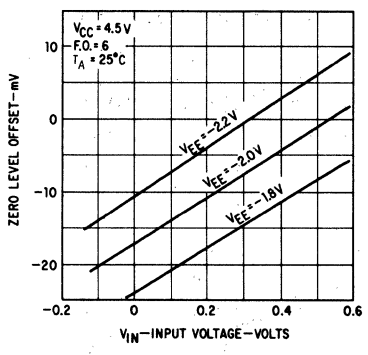


"ZERO" LEVEL OFFSET

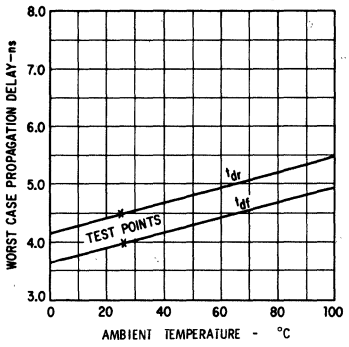
AS A FUNCTION OF FAN-OUT



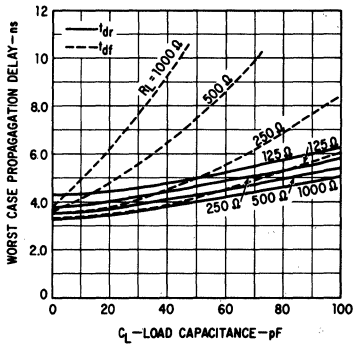
AS A FUNCTION OF V_{EE}



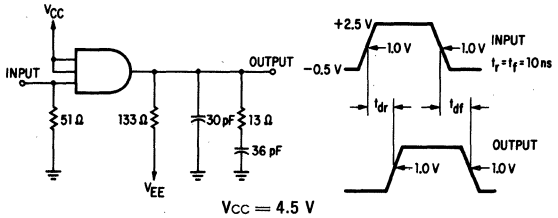
WORST CASE PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



WORST CASE PROPAGATION DELAY VERSUS C_L AS A FUNCTION OF R_L

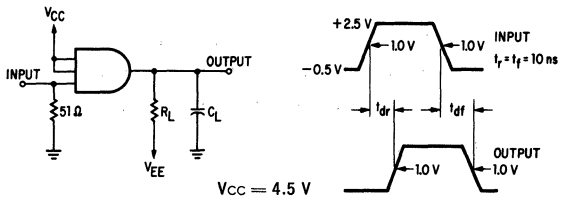


t_{PD} TEST CIRCUIT



$V_{CC} = 4.5$ V
$V_{EE} = -2.0$ V
$T_A = 25°C$

t_{PD} TEST CIRCUIT FOR ABOVE



$V_{CC} = 4.5$ V
$V_{EE} = -2.0$ V
$T_A = 25°C$

APPLICATION INFORMATION:

Greatest system speed will be realized by performing most of the logic with the use of the ultra-fast AND-OR gates. Consideration, however, must be given to level shifting, loading effects, impedance matching and ringing, which are inherent in fast switching systems. The AND-OR gates have built-in capability to overcome these problems. A few rules are outlined below to assist in solving these problems.

The electrical specification tests are performed under conditions chosen to emphasize the worst case results, and could be considered as conservative limits. For initial steps in designing new systems, typical values and data from graphs may be consulted for a realistic design. The different diagrams for each parameter are correlated through the nominal curve. To arrive at the worst case performance under a given set of conditions, deviation from nominal curve must be added or subtracted as the case may be.

INTERFACING — The AND-OR Gate should always be driven from another CTμL element. When interfacing from another logic form, or from a test signal generator, the signal should be introduced via a CTμL inverter, buffer, or flip-flop and then into the AND-OR Gate.

WIRED-OR — A powerful feature of the AND-OR Gates is that two or more outputs may be wired together to form the positive OR function at the output tie point, thus achieving two logic decisions in a maximum of 4.5 ns. Subtract 1 unit fanout for each OR added gate.

OFFSET LEVEL - NOISE IMMUNITY — The AND-OR Gate may be looked upon as a non-inverting amplifier having a gain of less than one. Thus, the output levels are offset from the input. The amount of offset is a function of loading, positive and negative power supplies, temperature, and input voltage and could be determined from the One and Zero level offset curves. When cascading AND-OR Gates, it should be noted that the offset of the first element has the largest offset and is decreasing sequentially on the following elements, due to smaller input level. It is recommended that noise-immunity levels be re-established by inserting such CTμL elements as the 952 Inverter, 956 Buffer, or 967 Flip-Flop after several offsets.

HIGH FREQUENCY RINGING — Each AND-OR Gate is internally equipped with a clamp circuit designed to reduce output ringing at high speed operation, at low fanout and moderate speed, the clamp may be released by leaving pin 5 open.

Any one length over 12" long connected to the output should be terminated with a 200 Ω resistor to ground at the output. The 200 Ω approximates the characteristic impedance of back panel wiring. The 200 Ω termination is considered as a fanout of 4.

Regular equal spacing of AND-OR along a single path should be avoided as they tend to appear to the driving gate as a set of similarly tuned tank circuits and may induce ringing. When unavoidable, 200 Ω resistor to ground along the path will eliminate the ringing.

Large capacitive loads may cause ringing at the AND-OR Gate output and should be driven from a CTμL inverter or buffer.

UNUSED INPUTS — Unused inputs to the AND-OR Gate will effectively inhibit the gate output, and therefore, must be tied to the most positive voltage level. The unused input may be tied directly to $+V_{CC}$ or through a resistor not greater than 600 Ω. Unused inputs may be tied to active inputs at a cost of reduced fanout.

SHORT CIRCUIT PROTECTION — The AND-OR Gate output is protected by a limiting resistor at the output and may sustain prolonged short circuit to ground at V_{CC} not greater than 5 volts. Excessive destructive heat may develop when more than one output in a single package is short circuited to ground. Short circuiting the output to the —2 volts supply should be avoided.

CTμL9956

DUAL 2-INPUT BUFFER

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The CTμL 9956 dual 2-input power AND gate is a low impedance non-inverting level setting circuit intended to drive high fanout, and may be used as a 50Ω line driver. The input threshold and output levels are compatible with any other CTμL elements. The output of the CTμL 9956 may be tied with any other CTμL element to perform the wired OR function.

CTμL 9956 is packaged in the versatile Jedec TO-116 Dual In-Line Package* which is a hermetically sealed ceramic package intended for low cost insertion techniques.

CTμL 9956 is designed to operate over a commercial ambient temperature range of +15 to +55°C. Power supplies are 4.5 volts ± 10% and −2 volts ± 10%. Typical power dissipation per gate is 60 mW and is designed to increase with fanout. Typical propagation delay 14 ns.

*Fairchild patent pending.

FEATURES:

- Power Supplies are +4.50 V ±10% and −2.00 V ±10%.
- High Fan-Out Capability . . . 25.
- Two Optional Pull Down 1.0 k Resistors for Optimum Speed.
- Low Power Dissipation.
- Low Propagation Delay.
- Logic Swing of 3.0 V.

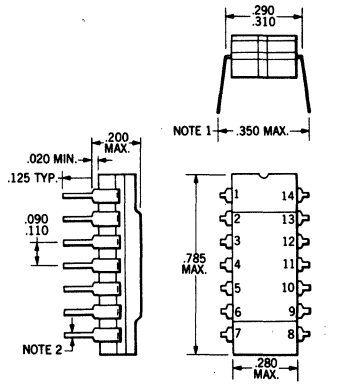
PURCHASING INFORMATION

- Use the ten letter code U6A995679X for ordering purposes.
- All units are marked CTμL 995679 and date code, unless otherwise specified.

PHYSICAL DIMENSIONS

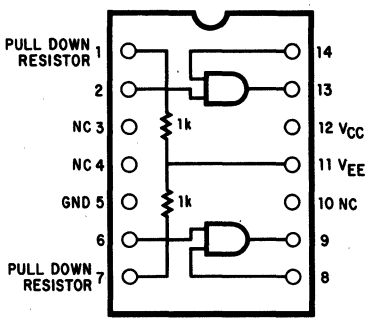
TYPICAL DUAL IN-LINE PACKAGE

In Accordance With
JEDEC (TO-116) Outline



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

CONNECTION DIAGRAM



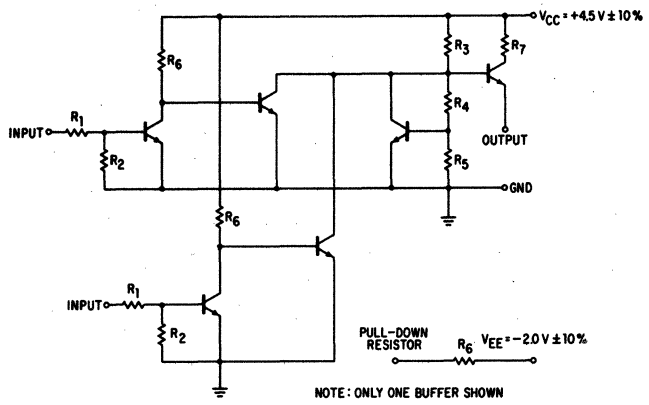
TOP VIEW

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Maximum Current in or out of a Pin	100 mA
Maximum Chip Temperature	150°C
Maximum Power Dissipation	1.0 Watt
Maximum Voltage Applied to any Input Pin	10 Volts
Maximum Negative Voltage Applied to any Input Pin	−4.0 Volts
Maximum Voltage Applied to Output Pin	6.0 Volts

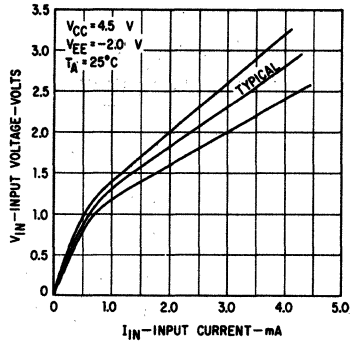
DC TESTS

TEST (at $T_A = 25°C$)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.	UNITS	V_{CC}	V_{EE}	LOAD TO V_{EE}	COMMENTS
ONE Level Output	2.25	2.60		Volts	4.05	Note 1	(2)F.O. = 25	Inputs simultaneously to 1.25 V
ONE Level Output	2.46			Volts	4.95	Note 1	F.O. = 1	Inputs simultaneously to 1.25 V
ONE Level Output		2.70	3.20	Volts	4.95	Note 1	Internal 1 k	Inputs simultaneously to 3.5 V
ZERO Level Output		−0.45	−0.36	Volts	4.05	−1.8 V	F.O. = 1	Inputs to 0.8 V sequentially, unused input to 3.5 V
Input Current		5.30	6.40	mA	4.05	Note 1	No Load	Inputs to 3.5 V simultaneously, guarantees input loading ≤ 1.5 AND-OR gate loads
Input Pull Down Resistor	0.8	1.0	1.2	kΩ	4.05	−2.2 V	No Load	3.5 V applied to pull down resistor
Positive Supply Current			69.2	mA	4.95	−2.2 V	No Load	One input to 3.5 V, other inputs to GND.
Output Rising Delay, t_{dr}		12.0	18.0	ns	4.50	Note 1	F.O. = 25	See t_{pd} test circuit, page 4
Output Falling Delay, t_{df}		12.0	18.0	ns	4.50	Note 1	F.O. = 25	See t_{pd} test circuit, page 4

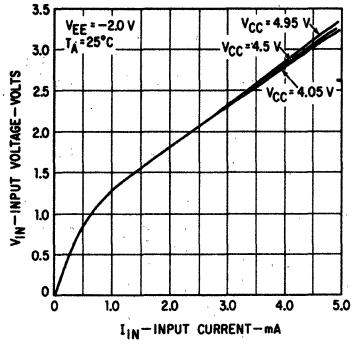
NOTES:
(1) Value of V_{EE} is non-critical: $-2.20\ V \leq V_{EE} \leq -1.80\ V$
(2) F.O. = Fan Out; F.O. = 25 equivalent to 64 Ω to −2.20 V under worst case conditions
F.O. = 1 equivalent to 2.4 kΩ to −1.80 V under worst case conditions

INPUT CHARACTERISTICS

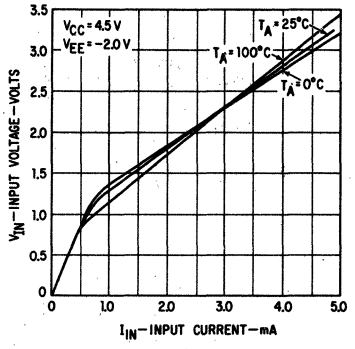
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE

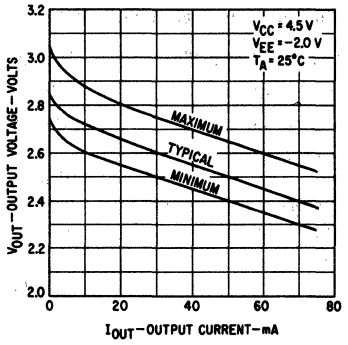


AS A FUNCTION OF TEMPERATURE

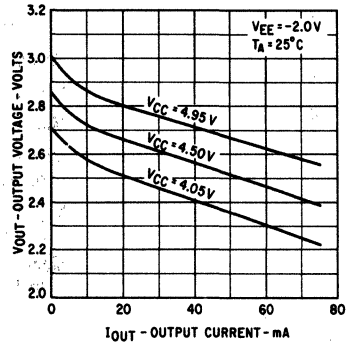


OUTPUT CHARACTERISTICS

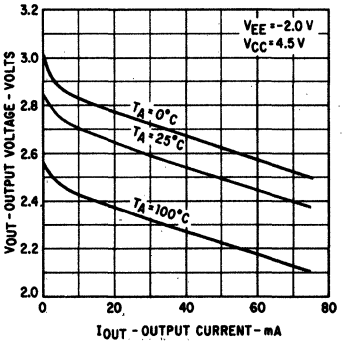
TOLERANCE VARIATION OF PARAMETERS



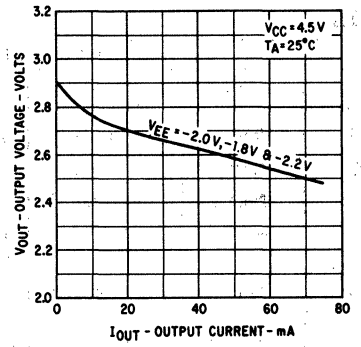
AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE



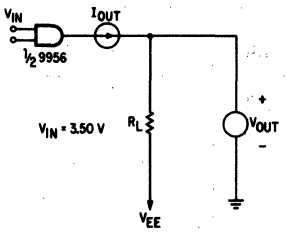
AS A FUNCTION OF TEMPERATURE



AS A FUNCTION OF NEGATIVE SUPPLY VOLTAGE

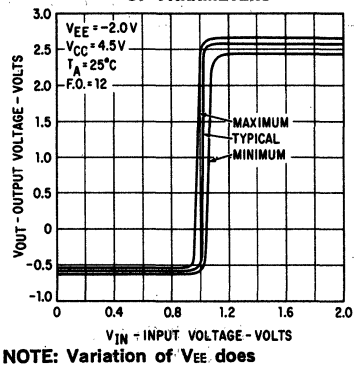


SCHEMATIC DIAGRAM



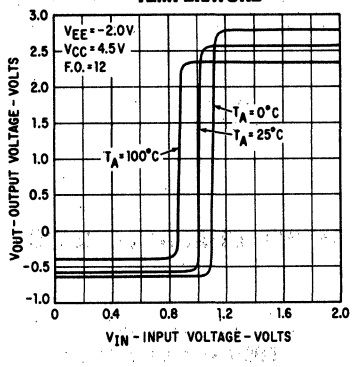
TRANSFER CHARACTERISTICS

TOLERANCE VARIATION OF PARAMETERS

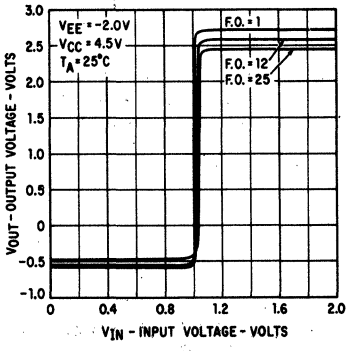


NOTE: Variation of V_{EE} does not alter transfer characteristics.

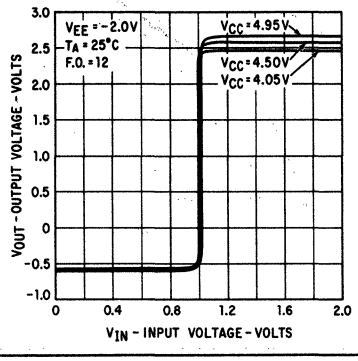
AS A FUNCTION OF TEMPERATURE



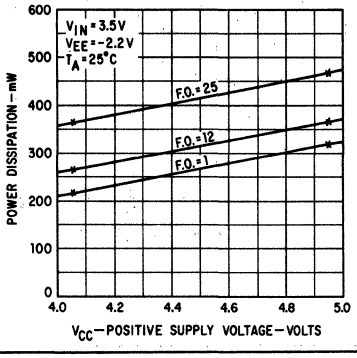
AS A FUNCTION OF FAN-OUT



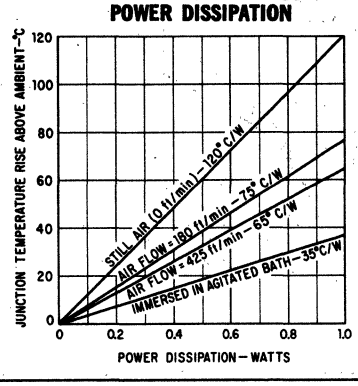
AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE



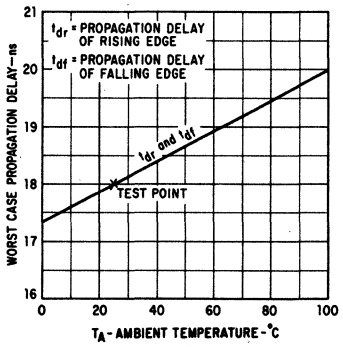
WORST CASE POWER DISSIPATION VERSUS POSITIVE SUPPLY VOLTAGE



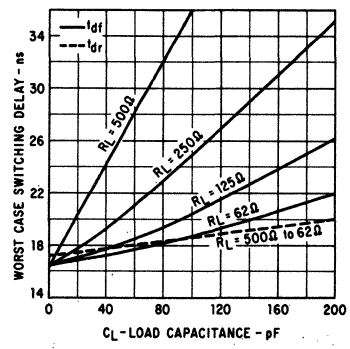
WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION



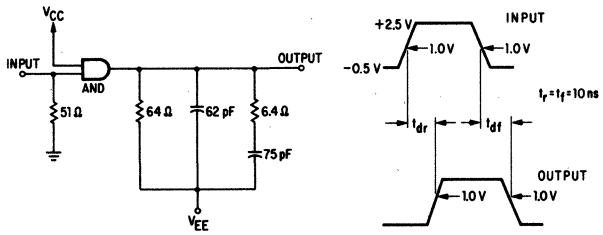
WORST CASE PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



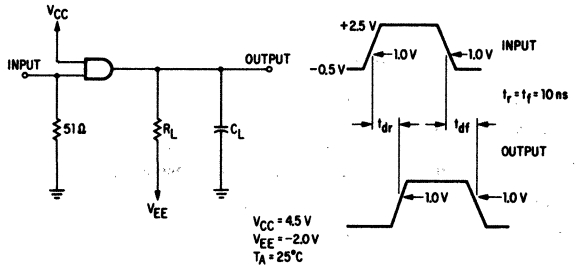
WORST CASE PROPAGATION DELAY VERSUS LOAD CAPACITANCE AS A FUNCTION OF LOAD RESISTANCE



t_{PD} TEST CIRCUIT



t_{PD} TEST CIRCUIT FOR ABOVE



APPLICATION INFORMATION

The electrical specification tests are performed under conditions chosen to emphasize the worst case results and could be considered as conservative limits. The output ONE level at worst case is guaranteed to drive a fanout of 25 AND-OR gates. The maximum input current assures that 9956 input presents a load of not more than 1.5 AND-OR gate input.

INTERFACING — The CTμL 9956 buffer could serve as an excellent interfacing link between external signals coming from other logic forms or peripheral equipments and the CTμL Family logic.

PULL DOWN RESISTORS — Two pull down 1 kΩ resistors are built into the package with one end tied to the negative power supply (V_{EE}). When the 9956 input is driven by a single AND-OR gate, the 1 kΩ resistors should be connected to the same input pin. This will improve the 9956 output rise and fall time. The pull-down resistor may be also connected to the CTμL 9956 output, which will improve the output falling delay when the fanout is low.

LINE DRIVER — The CTμL 9956 could be used as a line driver. To drive a 50 Ω line, a 68 Ω resistor should be connected from the output to ground. This will reduce the fanout capability by 15.

WIRED-OR — A powerful feature of the CTμL 9956 Buffer is that the output may be tied together with the output of any other element in the CTμL family to form the positive OR function at the tie point. When two or more CTμL 9956 outputs are tied for the OR function, a pull-down resistor must be used.

UNUSED INPUTS — Unused inputs to the AND-OR Gate will effectively inhibit the gate output, and therefore, must be tied to the most positive voltage level. The unused input may be tied directly to $+V_{CC}$ or through a resistor not greater than 600 Ω. Tying an unused input to an active input is not recommended.

SHORT CIRCUIT PROTECTION — The CTμL 9956 Gate output is protected by a limiting resistor at the output and may sustain prolonged short circuit to ground at V_{CC} not greater than 5 volts. Excessive destructive heat may develop when more than one output in a single package is short circuited to ground. Short circuiting the output to the −2 volts supply should be avoided.

CTμL 9957•9967
FLIP-FLOPS
COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS
+15°C TO +55°C TEMPERATURE RANGE

CTμL 9967 FLIP-FLOP GENERAL DESCRIPTION

The CTμL 9967 dual rank J-K Flip-Flop is a high speed directly coupled multi-purpose storage element useful for shift registers, counters, and other control functions.

Operation of the CTμL 9967 is based on the "master-slave" principle whereby information is entered into the "master" when the clock pulse goes high and is transferred to "slave" and outputs when the clock pulse goes low. DC coupling throughout makes the Flip-Flop input insensitive to rise and fall times.

The CTμL 9967 employs the PNP-NPN complementary logic to achieve fast response with typical toggling rate of 35 MHz. The emitter follower outputs are compatible with all other elements in the CTμL family.

Two phase clock outputs at half the clock input frequency is available when the CTμL 9967 is operated as a binary counter. Typical power dissipation is 420 mW and is designed to increase with fanout.

CTμL 9957 GENERAL DESCRIPTION

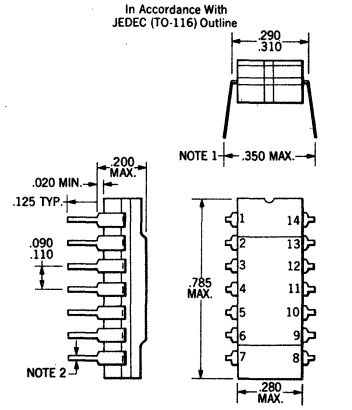
The CTμL 9957 is a basic dual-rank R-S Flip-Flop intended for storage and control function. Logic and clock inputs are omitted for additional flexibility. J-K operation with either two-phase or single-phase clocking can be exercised by adding AND-OR gates to the inputs. Wired OR ties within the flip-flop reduce typical through propagation delays to 14 ns.

The CTμL 9957 is DC coupled throughout. The inputs respond exclusively to voltage levels and are insensitive to rise and fall times. Emitter follower outputs, compatible with all other CTμL elements, provide efficient drive capability into long line and capacitive loads.

The CTμL 9967 and CTμL 9957 are packaged in the versatile Dual In-Line Package which is hermetically sealed ceramic package intended for low cost insertion techniques.

Both flip-flops are designed to operate over a commercial ambient temperature range of +15°C to +55°C. Power supplies are 4.5 volts ±10% and −2 volts ±10%.

PHYSICAL DIMENSIONS
TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

PURCHASING INFORMATION

DESCRIPTION	CODE	MARKING
CTμL 9957	U6A995779X	CTμL 95759
CTμL 9967	U6A996779X	CTμL 96779

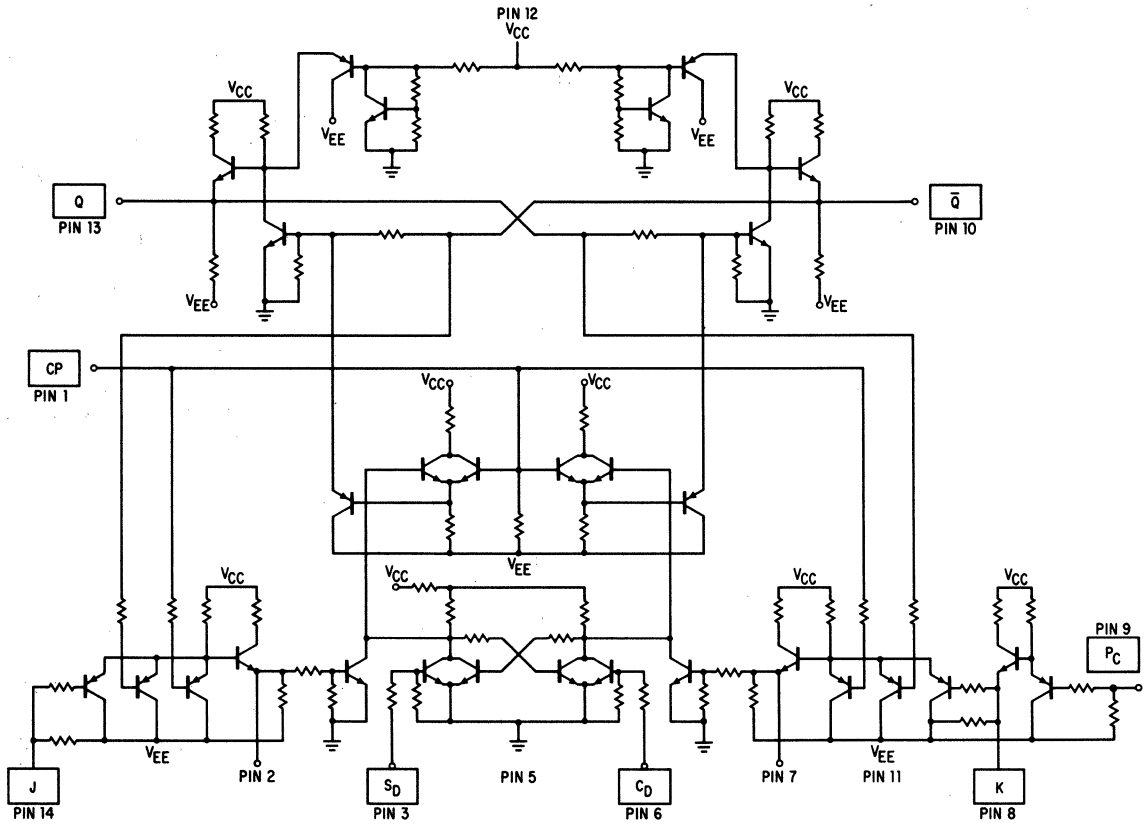
Use the ten letter code for ordering purposes.
All units marked as above unless otherwise specified.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

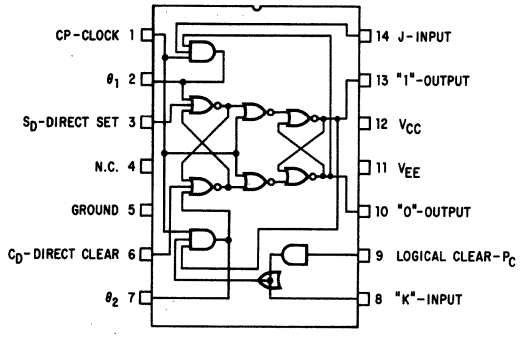
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

CTμL 9967 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



PIN & LOGIC DIAGRAM CTμL9967 - JK FLIP FLOP



V_{CC} = 4.50 V
V_{EE} = −2.00 V
N.C. = NOT CONNECTED

TRUTH TABLE

SYNCHRONOUS ENTRY					ASYNCHRONOUS ENTRY			
		t_n		$t_n + 1$	Inputs		Outputs	
J	K	SD	CD	output (Q)	SD	CD	"1"	"0"
L	L	L	L	Q_n	L	L	NC	NC
L	H	L	L	L	L	H	L	H
H	L	L	L	H	H	L	H	L
H	H	L	L	$\bar{Q}_n$	H	H	H	H
L	L	L	H	H	Clock Input Low			
L	L	H	L	L				
L	L	H	H	Undetermined				

LOADING RULES

FLIP-FLOP INPUTS	LOADING*
CP	2.0
J, K	1.0
S_D, C_D,	1.5
P_C	1.0
OUTPUTS	**FAN OUT**
Q, $\bar{Q}$	12

*1 Load = 1 CTμL AND-OR Gate Input Load

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Maximum current in or out of a pin	100 mA
Maximum chip temperature	150°C
Maximum power dissipation	1.0 Watt
Maximum voltage applied to any input pin	10 Volts
Maximum negative voltage applied to any input pin	−4.0 Volts
Maximum voltage applied to output pin	6.0 Volts

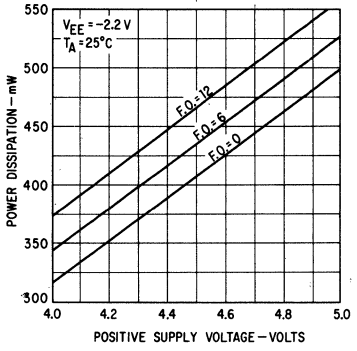
ELECTRICAL CHARACTERISTICS

9967 DC TESTS

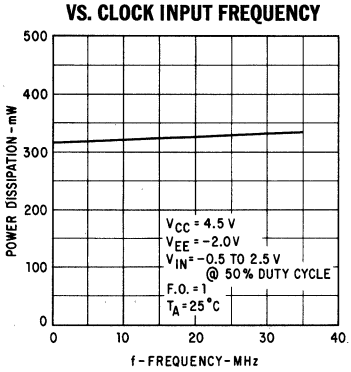
TESTS (at $T_A = 25°C$)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.[5]	UNITS	V_{CC}	V_{EE}	Load to V_{EE}	COMMENTS
ONE Level Output	2.35	2.50		Volts	4.05	NOTE 1	[3]F.O. = 12	Untested output to 3.50 V; logic input to 1.33 V; clock inputs to pulse (Note 4)
ONE Level Output	2.56			Volts	4.95	NOTE 1	No Load	Untested output to 3.50 V; logic input to 1.33 V; clock inputs to pulse (Note 4)
ONE Level Output	2.56			Volts	4.95	NOTE 1	No Load	Untested direct input to 3.50 V; tested direct input to 1.25 V; clock input to −0.70 V.
ONE Level Output			3.20	Volts	4.95	−1.80	F.O. = 1	Corresponding direct input is 3.50 V.
ZERO Level Output		−0.50	−0.36	Volts	NOTE 2	−1.80	F.O. = 1	Direct input to 3.50 V; other direct input to 0.80 V; logic inputs to 3.50 V; clock input to 0.47 V.
ONE Level Offset		200	270	mV	4.05	−2.20	F.O. = 4	Trigger and logic inputs sequentially to 2.25 V; untested inputs and outputs to 3.50 V.
ZERO Level Offset		120	195	mV	4.95	−1.80	F.O. = 1	Clock and logic inputs sequentially to −0.36 V. Untested inputs and outputs to 3.50 V.
Logic Input Pull-down Resistor	1.6 k	2.0 k	2.4 k	Ω	NOTE 2	−1.80	No Load	Logic input is 3.50 V.
Clock Input Pull-down Resistor	0.8 k	1.0 k	1.2 k	Ω	NOTE 2	−1.80	No Load	Clock input to 3.50 V.
Input Current		6.1	7.67	mA	NOTE 2	−1.80	No Load	Terminals 2 and 7 to 3.50 V.
Input Current		2.0	3.27	mA	4.05	−1.80	No Load	Direct set and clear inputs to 3.50 V.
Positive Supply Current		51.0	64.0	mA	4.95	−2.20	No Load	Clock input to −0.47 V.
Negative Supply Current		55.0	68.7	mA	4.95	−2.20	No Load	Clock, logic inputs and "1" outputs to 3.50 V simultaneously.
Clock Pulse Width - t_{PW}	25	16.0		ns	4.50	−2.00	F.O. = 12	Min. required pulse width to trigger 967.
Output Rising Delay - t_{dr}		10.0	15.0	ns	4.50	−2.00	F.O. = 12	See t_{df}, t_{dr} test circuit, page 4
Output Falling Delay - t_{df}		16.0	25.0	ns	4.50	−2.00	F.O. = 12	See t_{df}, t_{dr} test circuit, page 4
Direct Through Rising Delay - t_{sr}		17.0	25.0	ns	4.50	−2.00	F.O. = 12	See t_{sr}, t_{sf} test circuit, page 5
Direct Through Falling Delay - t_{sf}		25.0	38.0	ns	4.50	−2.00	F.O. = 12	See t_{sr}, t_{sf} test circuit, page 5

NOTES:
(1) Value of V_{EE} non-critical, $-1.80\ V \leq V_{EE} < -2.20\ V$.
(2) Value of V_{CC} non-critical, $4.05\ V \leq V_{CC} \leq 4.95\ V$.
(3) F.O. = Fan-Out: F.O. = 12 equivalent to 133Ω to −2.20 V under worst case conditions.
F.O. = 4 equivalent to 400Ω to −2.20 V under worst case conditions.
F.O. = 1 equivalent to 2.4 k to −1.80 V under worst case conditions.
(4) Pulse is a positive pulse of non-critical amplitude and width.
(5) "Maximum" means "no more positive than."

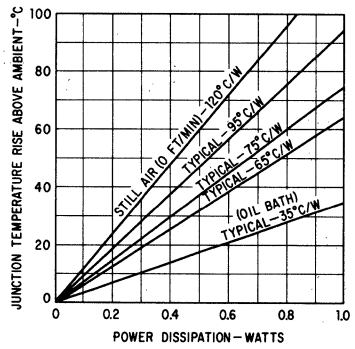
WORST CASE POWER DISSIPATION VS. POSITIVE SUPPLY VOLTAGE



WORST CASE POWER DISSIPATION VS. CLOCK INPUT FREQUENCY



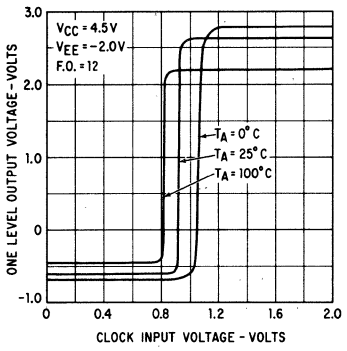
WORST CASE JUNCTION TEMPERATURE VS. POWER DISSIPATION



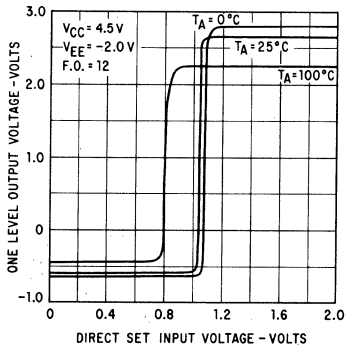
CTμL 9967 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

TRANSFER CHARACTERISTICS

CLOCK-ONE LEVEL VERSUS TEMPERATURE

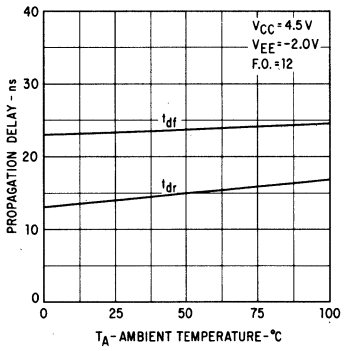


DIRECT SET/DIRECT CLEAR VERSUS TEMPERATURE

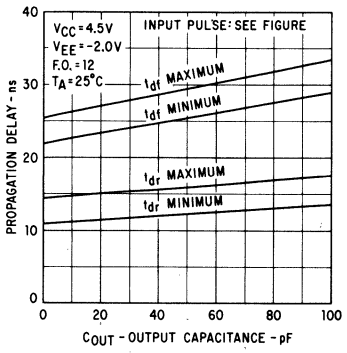


SWITCHING CHARACTERISTICS

PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE

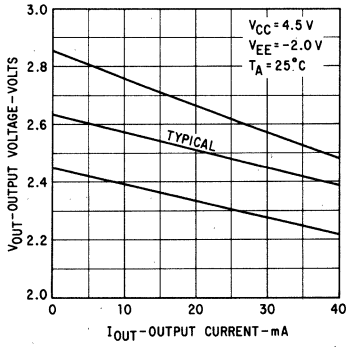


INCREASE IN PROPAGATION DELAY DUE TO OUTPUT CAPACITANCE

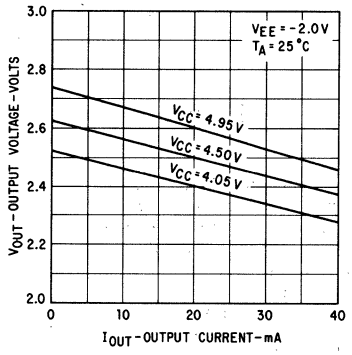


OUTPUT CHARACTERISTICS

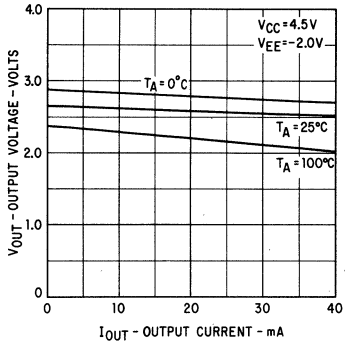
TOLERANCE VARIATION OF PARAMETERS



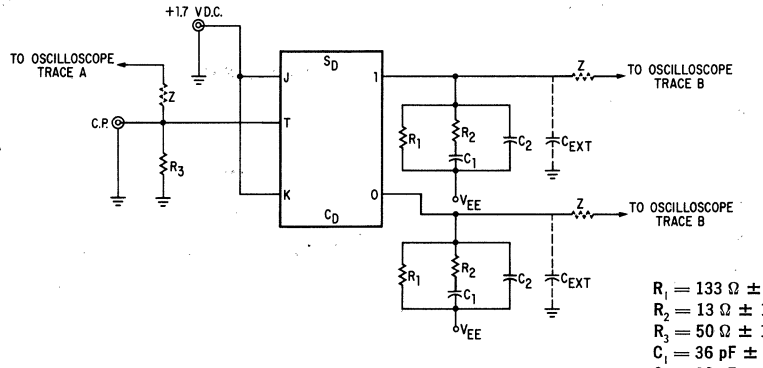
AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE



AS A FUNCTION OF TEMPERATURE



t_{df} and t_{dr} SWITCHING TIME TEST CIRCUIT



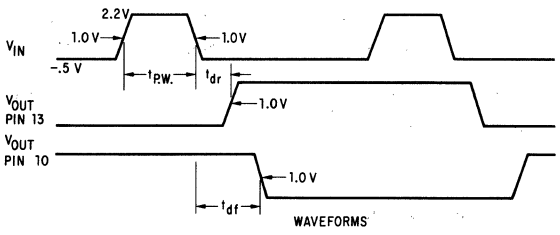
$R_1 = 133\ \Omega \pm 1\%$
$R_2 = 13\ \Omega \pm 1\%$
$R_3 = 50\ \Omega \pm 1\%$
$C_1 = 36$ pF ± 2%
$C_2 = 30$ pF ± 2%
Z = Probe Impedance ≥ 5k

SWITCHING NOTES:

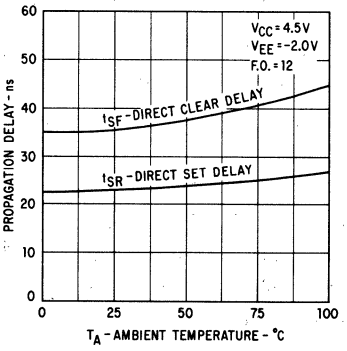
(1) Input Pulse
Frequency: 10 Hz to 10 MHz
Pulse Width (t_{PW}) = 25 ns
Rise Time = 10 ns
Fall Time = 10 ns
at 10% to 90% pts.

(2) The load capacitance indicated in the test circuit includes the capacitance of the probe and jig.

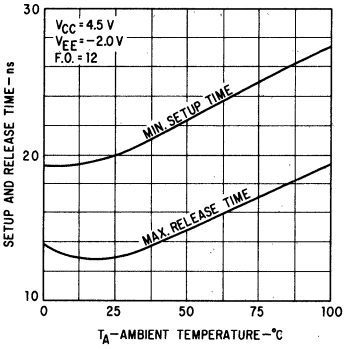
(3) $V_{CC} = 4.50$ V; $V_{EE} = -2.00$ V



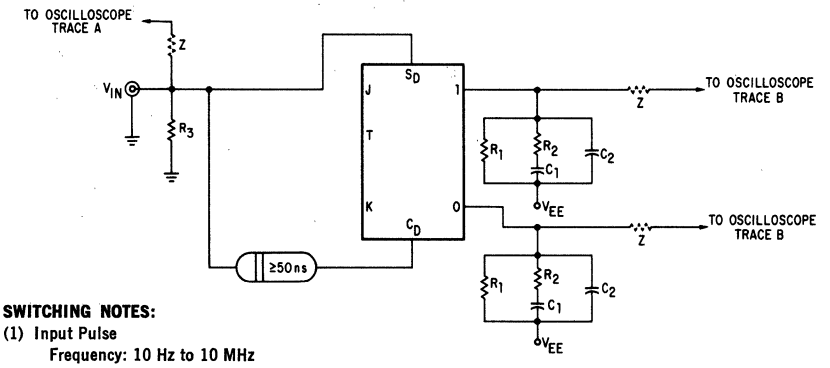
DIRECT SET AND DIRECT CLEAR PROPAGATION DELAY VERSUS TEMPERATURE



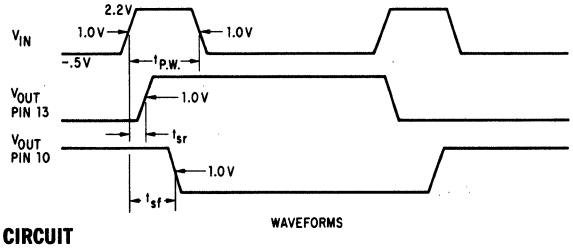
WORST CASE SETUP AND RELEASE TIME VERSUS TEMPERATURE



DIRECT SET & DIRECT CLEAR SWITCHING TIME TEST CIRCUIT



$R_1 = 133\ \Omega \pm 1\%$
$R_2 = 13\ \Omega \pm 1\%$
$R_3 = 50\ \Omega \pm 1\%$
$C_1 = 36$ pF ± 2%
$C_2 = 30$ pF ± 2%
Z = Probe Impedance ≥ 5k



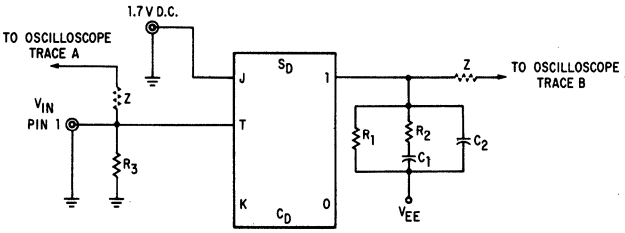
SWITCHING NOTES:

(1) Input Pulse
Frequency: 10 Hz to 10 MHz
Pulse Width = 25 ns
Rise Time = 10 ns
Fall Time = 10 ns
at 10% to 90% pts.

(2) The load capacitance indicated in the test circuit includes the capacitance of the probe and jig.

(3) $V_{CC} = 4.50$ V; $V_{EE} = -2.00$ V

$t_{SET\text{-}UP}$ & $t_{RELEASE}$ SWITCHING TIME TEST CIRCUIT



$R_1 = 133\ \Omega \pm 1\%$
$R_2 = 13\ \Omega \pm 1\%$
$R_3 = 50\ \Omega \pm 1\%$
$C_1 = 36$ pF ± 2%
$C_2 = 30$ pF ± 2%
Z = Probe Impedance ≥ 5k

SWITCHING NOTES:

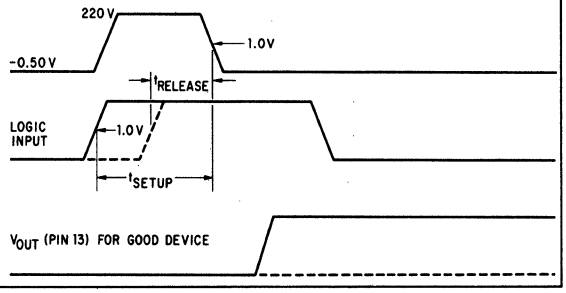
(1) Input Pulse
Rise Time = 10 ns
Fall Time = 10 ns
Amplitude = 2.10 V
at 10% to 90% pts.

(2) The load capacitance indicated in the test circuit includes the capacitance of the probe and the jig.

(3) $V_{CC} = 4.50$ V; $V_{EE} = -2.00$ V.

(4) Similar tests may be made at "O" output if logic input is the "K" input.

(5) $t_{SET\text{-}UP}$ is defined as the minimum time required for a "ONE" to be present at either logic input prior to a clock transition from a high to a low in order for the flip-flop to respond. $t_{RELEASE}$ is defined as the maximum time required for a ONE to be present at either logic input prior to clock transition from a high to a low in order for the flip-flop not to respond.

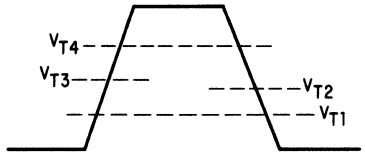


OPERATION OF FLIP-FLOP

The CTμL 9967 is directly coupled throughout and hence, its inputs are not sensitive to rise times. It responds exclusively to input voltage levels with definite, separated thresholds for both high and low voltage levels.

As the clock input rises from ZERO level, above V_{T1}, the transfer gates between the master and the slave are inhibited and the slave is isolated from the master. Above V_{T3}, the logic input gates are enabled and the master is set. Above V_{T4}, the master is sure to be set under the worst case condition and clock input is reaching the ONE level. As the clock input falls from the ONE level below V_{T4}, it inhibits the logic input gates and assures no further change in the master flip-flop. Below V_{T2}, the transfer gates are enabled, the slave and outputs are set according to information stored in the master. Below V_{T1}, the transfer gates are sure to be enabled under the worst case condition. The clock input reaches the ZERO level.

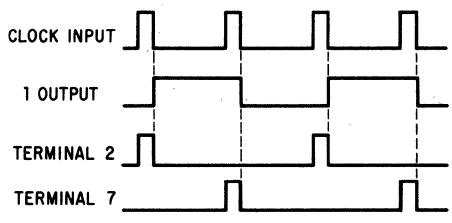
CLOCK INPUT VOLTAGE



Synchronous entry of information is done at the J and K inputs while the clock input is high.

Asynchronous information is entered at the S_D and C_D Direct Set and Direct Clear. A high level ONE is applied to the appropriate asynchronous input while the clock input is at the ZERO (low) level. Sufficient time must be allowed for the flip-flop to change state before the clock goes high.

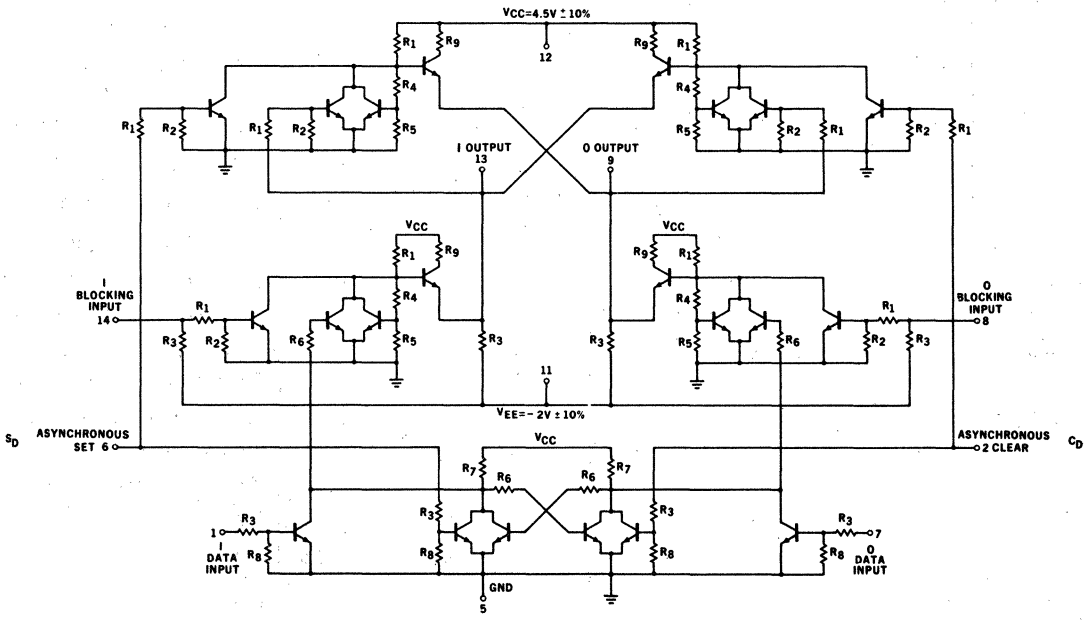
Pins 2 and 7 may serve as an output for a two phase clock having the same pulse duration as the clock input. Each output has a repetition rate of half the clock input frequency. (Fig. 1, Wired OR)



Pin 9, designated as a Logical Clear, may be used to block information from entering the J input without inhibiting the internal AND gate. It may also serve as an additional isolated J input.

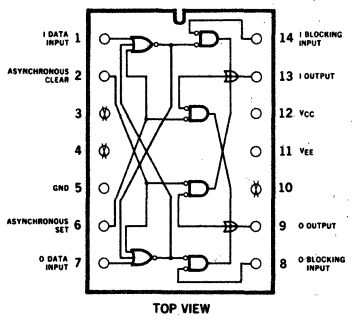
CTμL 9957 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



LOGIC DIAGRAM

(POSITIVE LOGIC)



TOP VIEW

TRUTH TABLE

S_n	C_n	Qnt + 1
0	0	Qn
0	1	0
1	0	1
1	1	Undetermined

NOTES:
(1) Connect pin 1 to pin 14 and pin 7 to pin 8
(2) Flip-Flop changes state on negative transition of input waveforms
(3) For asynchronous entry use pins 2 and 6

LOADING RULES

FLIP-FLOP UNITS	LOADING*
Data	1.0
SA, CA	2.0
Blocking	3.5
OUTPUTS	**FAN OUT**
Q, $\overline{Q}$	9.5

*1 Load = 1 CTμL AND-OR Gate Input Load

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Maximum current in or out of a pin	100 mA
Maximum chip temperature	150°C
Maximum power dissipation	1.0 Watt
Maximum voltage applied to any input pin	10 Volts
Maximum negative voltage applied to any input pin	—4.0 Volts
Maximum voltage applied to output pin	6.0 Volts

DC TESTS

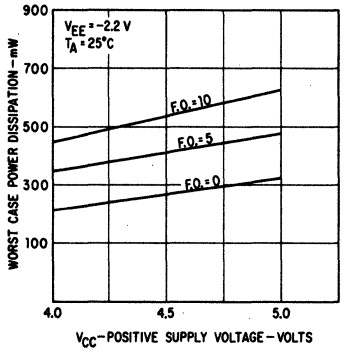
TESTS (at $T_A = 25°C$)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.	UNITS	V_{CC}	V_{EE}	Load to V_{EE}	COMMENTS
ONE Level Output			3.20 V	Volts	4.50	−2.00	No Load	Pulse note (1) to pin 3.
ONE Level Output	2.20			Volts	4.05	−2.20	(2)F.O. = 9.5	0.8 V to Pins 1 and 6, 2.5 V to Pin 8; Pulse to Pin 2. Guarantees min. ONE level output.
ONE Level Output	2.20			Volts	4.05	−2.20	F.O. = 9.5	2.5 V to Pins 2 and 6, 0.8 V to Pin 8.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	Pulse to Pin 6, 1.25 V to Pin 7.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	Pulse to Pin 2, 1.25 V to Pin 6, 2.5 V to Pin 14.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	1.25 V to Pin 8, 2.5 V to Pins 6 and 7.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	2.5 V to Pins 2, 8, 14; 1.25 V to Pin 13.
Input Current Data Input	1.5		2.25	mA	4.50	−2.0	No Load	2.5 V to Pins 1 and 7 sequentially.
Input Current Async. Input			6.75	mA	4.5	−2.0	No Load	2.5 V to Pins 2 and 6 sequentially. Guarantees asynchronous input loading.
Input Current Blocking Input			10.13	mA	4.5	−2.0	No Load	2.5 V to Pins 8 and 14 sequentially.
Output Resistor	6.75		10.13	mA	4.5	−2.0	No Load	2.5 V to Pins 6 and 9, Pins 2 and 13 sequentially.
Propagation Delay, t_{DR}		10	15	ns	4.5	−2.0	F.O. = 9.5	See Fig.
Propagation Delay, t_{DF}		17	30	ns	4.5	−2.0	F.O. = 9.5	See Fig.

NOTES:

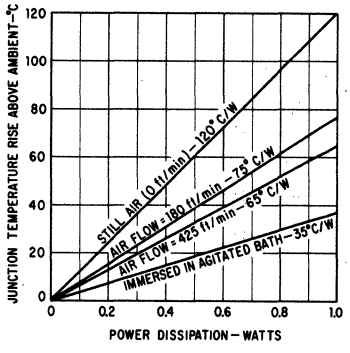
(1) Pulse, positive pulse of non-critical amplitude and width.
(2) F.O. = Fan-Out: F.O. = 9.5 equivalent to 168Ω to −2.20 V under worst case conditions.

ELECTRICAL CHARACTERISTICS

WORST CASE POWER DISSIPATION VERSUS POSITIVE SUPPLY VOLTAGE

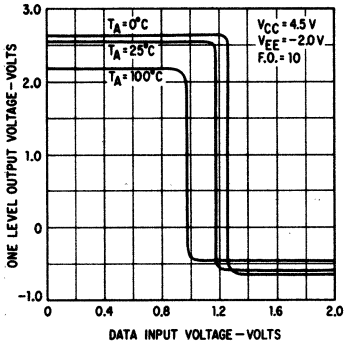


WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION

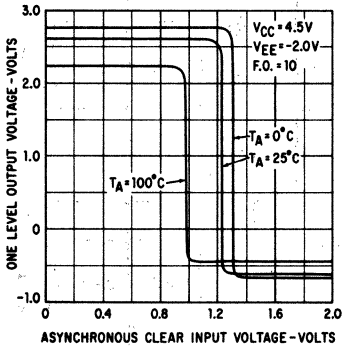


TRANSFER CHARACTERISTICS

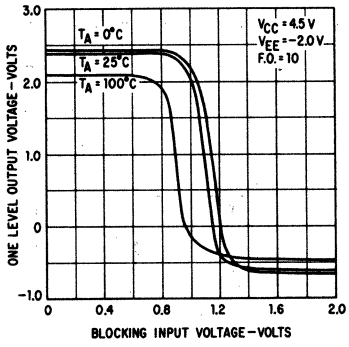
DATA INPUT - ONE LEVEL OUTPUT VOLTAGE VERSUS TEMPERATURE



ASYNCHRONOUS SET/CLEAR-ONE LEVEL OUTPUT VOLTAGE VERSUS TEMPERATURE

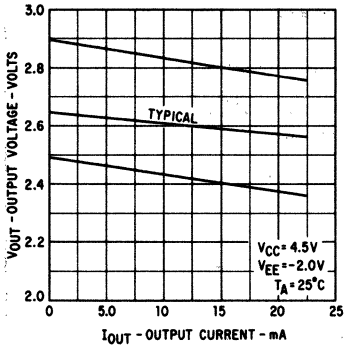


BLOCKING INPUT - ONE LEVEL OUTPUT VOLTAGE VERSUS TEMPERATURE

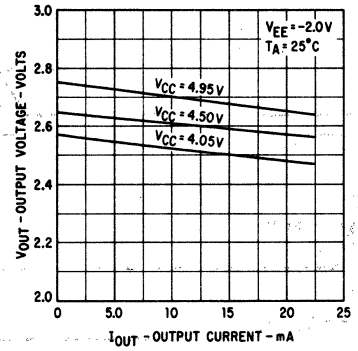


OUTPUT CHARACTERISTICS

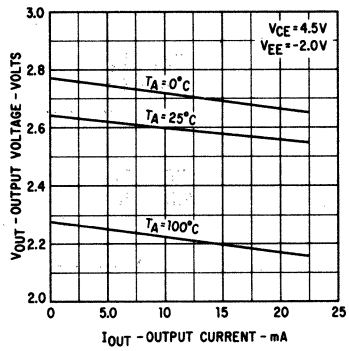
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE

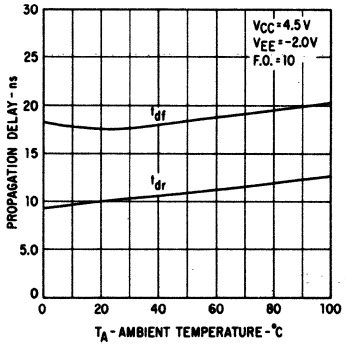


AS A FUNCTION OF TEMPERATURE

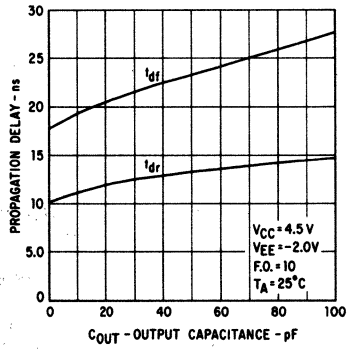


SWITCHING CHARACTERISTICS

PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE

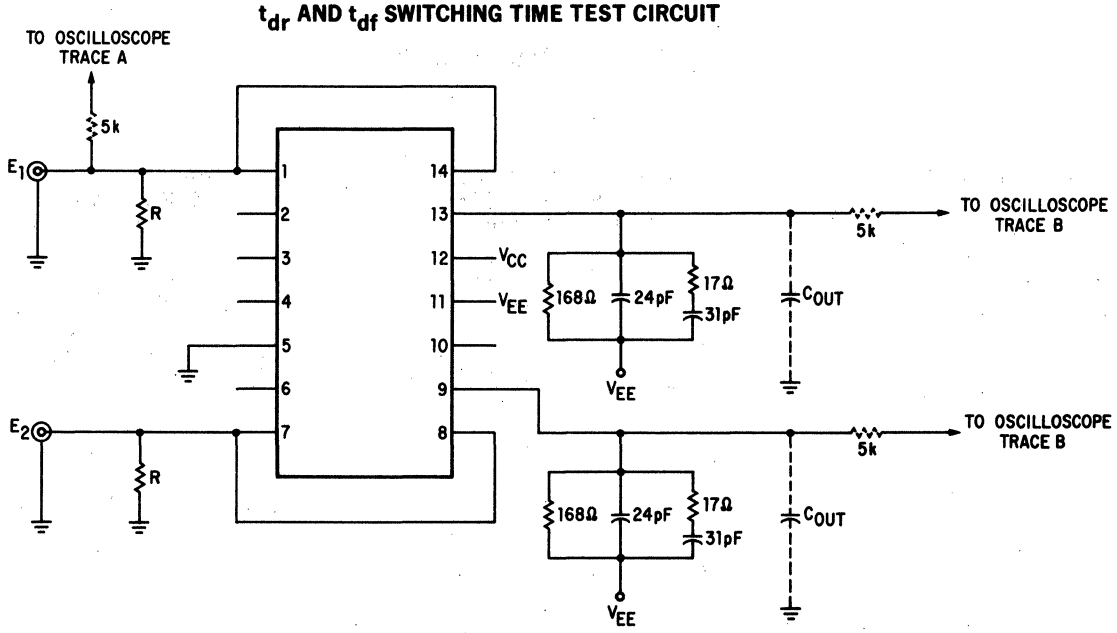


INCREASE IN PROPAGATION DELAY DUE TO OUTPUT CAPACITANCE

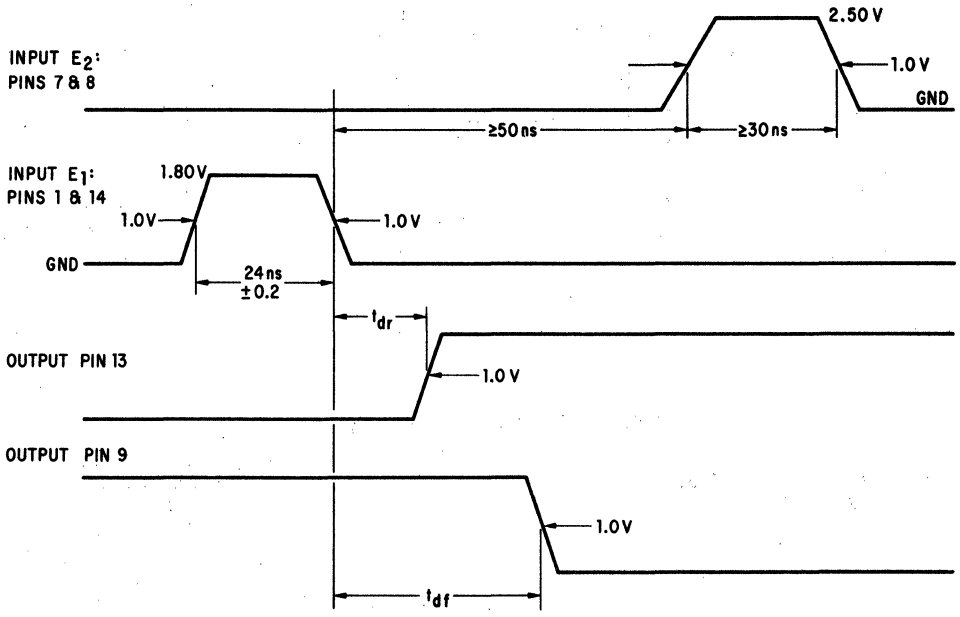


SWITCHING CHARACTERISTICS

t_{dr} AND t_{df} SWITCHING TIME TEST CIRCUIT



WAVEFORMS



SWITCHING NOTES:

(1) $V_{CC} = 4.50\ V \pm 10\%$
$V_{EE} = 2.00\ V \pm 10\%$
Select proper capacitor to provide adequate bypassing.

(2) Select R to provide proper termination for pulse generator used.

(3) Use oscilloscope with at least 5 k input impedance.

(4) Rise & Fall Times:
$t_f = t_r = 5ns$ measured at 10% to 90% points.

OPERATION OF FLIP-FLOP

The CTμL 9957 is a dual-rank directly-coupled R-S Flip-Flop. The first rank or "master" consists of two cross-coupled NOR gates similar to the CTμL 9952. The second rank or "slave" employs OR ties as shown in the functional logic diagram, thereby minimizing through delay. Two NAND gates provide feedback inversion, while the other two provide gating between "master" and "slave."

The primary data inputs to the Flip-Flop are through pins 1 and 7. These inputs work directly from AND gate outputs, allowing OR ties and multiple inputs to each Flip-Flop.

To take advantage of the dual-rank principle, mutually exclusive active inputs should be applied to the gating to "master" and "slave" so that only one or the other can change at any particular instant. This is easily accomplished in the CTμL 9957 due to the difference in active polarity of the two gates. Thus, what appears as a logic 1 to CTμL gates of the Flip-Flop data inputs is a logic 0 to the "slave" gates, and vice versa.

These observations lead to the connection of pin 1 to pin 14 and pin 7 to pin 8 as shown in Fig. 2. Although both "slave" gates are not necessarily inhibited when a change takes place, the output cannot change unless both data inputs are logic 0. Therefore, this connection is the usual one, tending to minimize the loading of timing circuits.

In case phased timing signals are advantageous, pins 8 and 14 may be used independently as long as they are never active (low) while their corresponding data inputs are high.

Direct inputs to both "master" and "slave" appear on pins 2 and 6. A logic (high) on either input sets or resets the "master" and simultaneously inhibits a feedback NAND gate in the "slave." The net effect is that both "master" and "slave" move to the desired condition during the presence of the direct input signal.

The response of the Flip-Flop to concurrent inputs tending to set opposite output conditions is ambiguous. That is, simultaneous logic 1 inputs must be avoided for well-defined operation.

APPLICATION

FIG. 1 DUAL RANK FLIP-FLOP CONNECTED FOR TWO-PHASE CLOCKING, J-K MODE

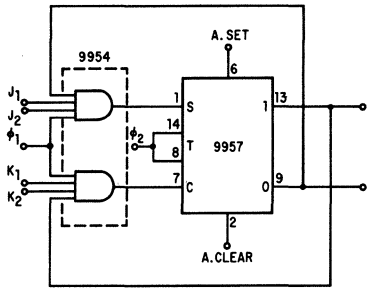


FIG. 2 DUAL RANK FLIP-FLOP CONNECTED FOR SINGLE-PHASE CLOCKING, J-K MODE

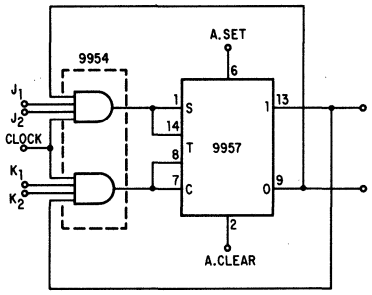


FIG. 3 SERIAL BINARY COUNTER

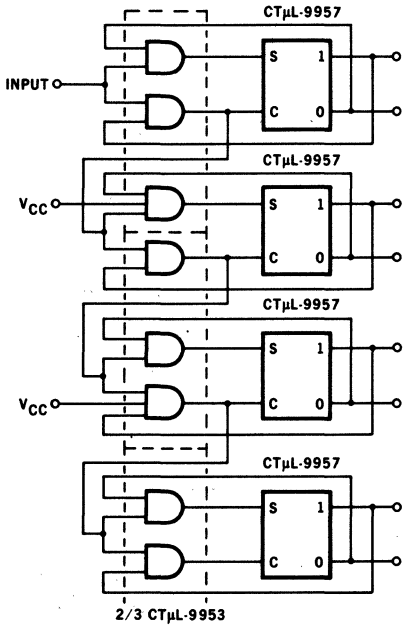
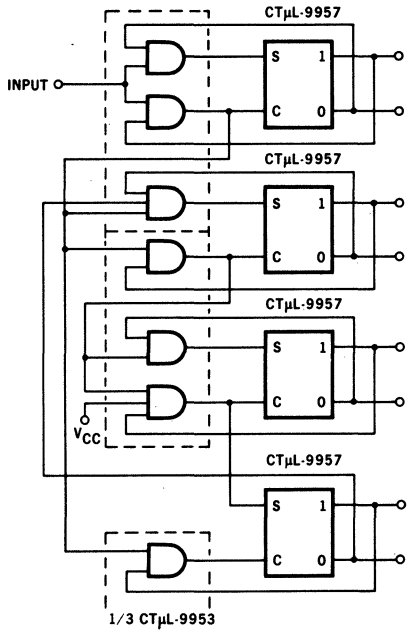


FIG. 4 1-2-4-8 DECADE



NOTES:
1. On all CTμL 9957's, tie pins 1-14 and 7-8.
2. All gates are CTμL 9953's.

9968

DUAL HIGH SPEED LATCH

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The 9968 is a dual gated latch for use as a high speed buffer memory. Compatible with all other CTμL elements, the output can be OR-tied, allowing several latches to connect to a single data line.

The 9968 combines both gating and storage facilities. To ensure that only valid information is entered, a "ONE" must be present at the WRITE input for data at the DATA input to be stored. In the absence of a WRITE signal, the feedback loop maintains the output state caused by the last set of input conditions.

To read out the information, a "ONE" must be present on the READ input. This readout is non-destructive. Output data is one AND gate offset below read level.

Typical delays are Write time 25 ns, Read, 3 ns. For increased storage capacity, where read delays of 25 ns can be tolerated, refer to the 9030 8-Bit Memory Cell data sheet.

The 9968 is packaged in the hermetically sealed ceramic Dual In-Line Package (similar to JEDEC TO-116) intended for low cost insertion techniques.

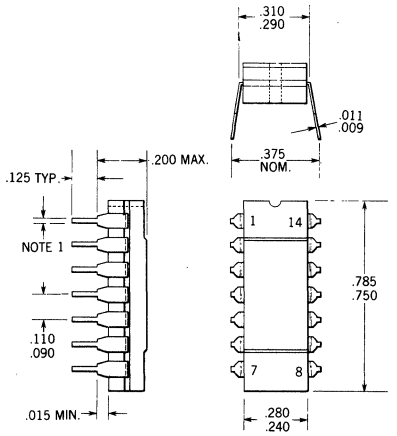
FEATURES:

- **POWER SUPPLIES — +4.5 V ±10% AND −2.0 V ±10%**
- **HIGH FAN-OUT CAPABILITY — 12**
- **TEMPERATURE RANGE — +15°C TO +55°C**
- **INPUT AND OUTPUT GATING**
- **NON-DESTRUCTIVE READ OUT**
- **FAST READ TIME — 3.0 ns**
- **LOGIC SWING OF 3.0 V**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Current in or out of a pin	100 mA
Chip temperature	150°C
Power dissipation	1.0 Watt
Voltage applied to any input pin	10 Volts
Negative voltage applied to any input pin	−4.0 Volts
Voltage applied to output pin	6.0 Volts

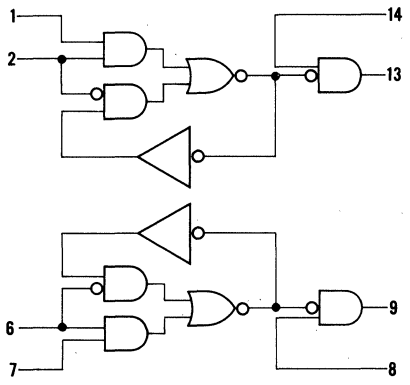
TYPICAL DUAL IN-LINE PACKAGE



NOTE:
1. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

ORDER PART NO. U6A996879X

LOGIC DIAGRAM

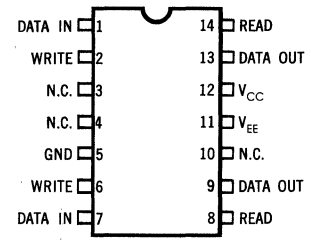


LOADING RULES

INPUTS	LOADING*
DATA	1.0
WRITE	1.0
READ	1.0
OUTPUTS	FAN OUT
DATA	12

*1 Load = 1 CTμL AND-OR Gate Input Load

PIN CONFIGURATION



TOP VIEW

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

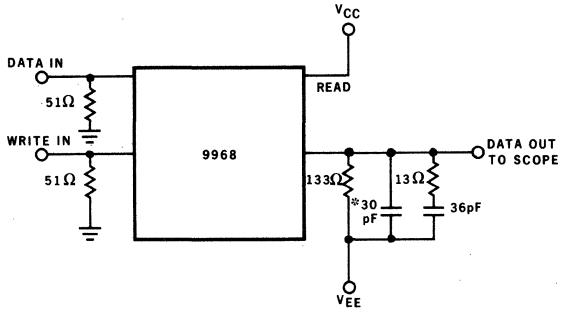
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

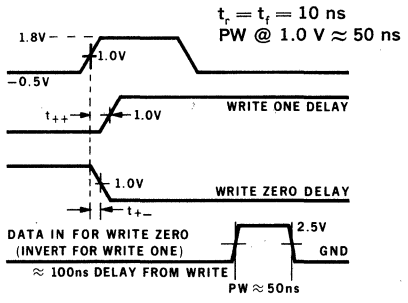
ELECTRICAL CHARACTERISTICS

	LIMITS				CONDITIONS			
TESTS (at $T_A = 25°C$)	MIN.	TYP.	MAX.(1)	UNITS	V_{CC}	V_{EE}	Load to V_{EE}	COMMENTS
ONE Level Output	2.35			Volts	4.95	−2.0	No Load	Data Input = 1.25 V Write Input = 1.8 V Read Input = 2.5 V
ZERO Level Output		−0.50	−0.36	Volts	4.95	−1.8	F.O. = 1	Data Input = 0.8 V Write Input = 1.25 V Read Input = 1.25 V
ONE Level Offset			220	mV	4.05	−2.2	F.O. = 11(2)	Data Input = 1.25 V Write Input = 1.25 V Read Input = 2.25 V
ZERO Level Offset			160	mV	4.95	−1.8	F.O. = 1	Data Input = 2.5 V Write Input = 2.5 V Read Input = −0.36 V
Input and Output Pull-down Resistors	1.6	2.0	2.4	kΩ	4.5	−2.0	No Load	Input or Output to 2.5 V
ONE Latching Threshold	1.25			V	4.95	−2.0	No Load	Min. input level which provides ONE output
ZERO Latching Threshold			0.8	V	4.95	−2.0	No Load	Max. input level which provides ZERO output
Data delay t_{++}			40	ns	4.5	−2.0	F.O. = 12	See test circuit below
t_{--}			40	ns	4.5	−2.0	F.O. = 12	
Write delay t_{+-}			25	ns	4.5	−2.0	F.O. = 12	See test circuit below
t_{++}			30	ns	4.5	−2.0	F.O. = 12	

NOTES: (1) "Maximum" means "no more positive than"
(2) F.O. = Fan-Out: F.O. = 11 equivalent to 145 Ω to −2.20 V under worst case conditions
F.O. = 1 equivalent to 2.4 k to −1.80 V under worst case conditions

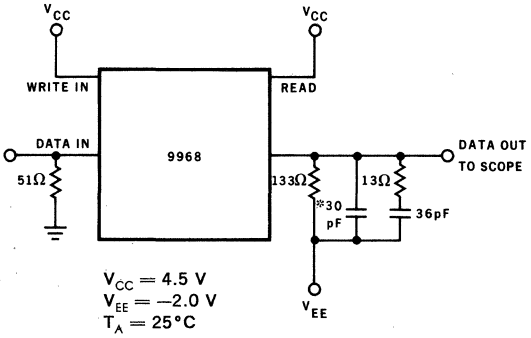
WRITE DELAY TEST CIRCUIT

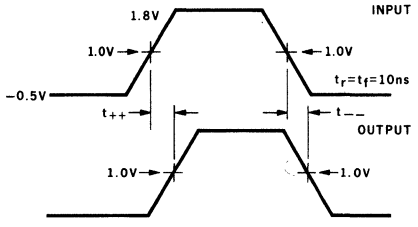




*Includes Probe and Jig Capacitance
$V_{CC} = 4.5$ V
$V_{EE} = -2.0$ V
$T_A = 25°C$

DATA DELAY TEST CIRCUIT





$V_{CC} = 4.5$ V
$V_{EE} = -2.0$ V
$T_A = 25°C$

MμL9030

8-BIT MEMORY CELL

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

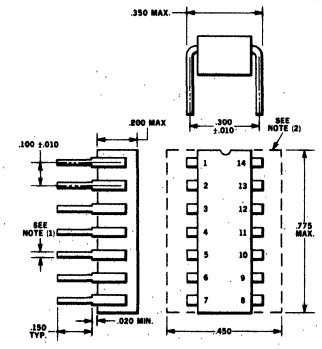
GENERAL DESCRIPTION - The MμL9030 is a Planar* epitaxial integrated 8-bit (non-destructive readout) memory cell consisting of four 2-bit words. The cell is addressable by word. It is permissible to write into one word while reading another. The same information may also be written in two words simultaneously. The "Write" time for a cell is 45 nanoseconds maximum and the "Read" delay is 25 nanoseconds.

The element is fully compatible with Fairchild CTμL Circuits. The "Read" and "Data" inputs are the equivalent of 1.5 CTμL gate loads, and the "Write" inputs, 3 CTμL gate loads. The outputs can drive 3 CTμL gate loads.

For applications where faster "Readout" speed is essential, the users are encouraged to investigate the properties of the CTμL 968 Integrated Dual Latch.

*Planar is a Patented Fairchild Process.

TYPICAL DUAL IN-LINE PACKAGE

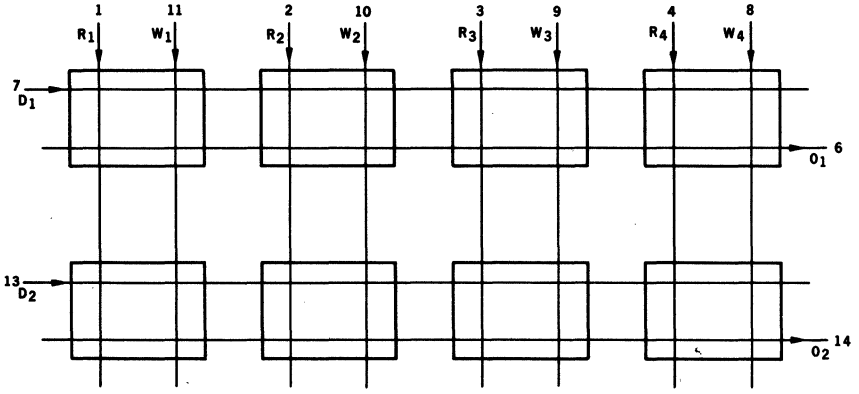


NOTES:
1. Leads are a modified hexagon in cross section. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.
2. Max. envelope for all planned packages of this design family.

LOGIC DIAGRAM AND PIN ARRANGEMENTS

D_1, D_2: DATA INPUTS
R_1, R_2, R_3, R_4: READ INPUTS
W_1, W_2, W_3, W_4: WRITE INPUTS
O_1, O_2: OR–ABLE OUTPUTS

V_{CC} = PIN 12
GND = PIN 5



FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

D.C. TESTS (V_{CC} = 4.5 V, T = 25°C)

DESCRIPTION	TEST	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS	EQUIV CTμL LOAD
Read Input Current	I_1, I_2, I_3, I_4	V_1, V_2, V_3, V_4 = 2.5 V		4.4	mA ea.	1.5
Data Input Current	I_7, I_{13}	V_7, V_{13} = 2.5 V		4.4	mA ea.	1.5
Write Input Current	I_8, I_9, I_{10}, I_{11}	V_8, V_9, V_{10}, V_{11} = 2.5 V		8.8	mA ea.	3
Output Voltage (High State)	V_6, V_{14}	I_6, I_{14} = -10 mA	2.35		V	
Output Voltage (Low State)	V_6, V_{14}	I_6, I_{14} = -1 mA		-0.36	V	
Output Leakage	I_6, I_{14}	V_6, V_{14} = 4 V		5	μA	
Output Capacitance	C_6, C_{14}	V_6, V_{14} = 0 Boonton Bridge		8	pF	

INPUT LEVEL: Maximum permissible "low" level = 0.8 V. Maximum required "high" level: 1.25 V.

RECOMMENDED OPERATING CONDITIONS:

The above test specifications characterize the terminal properties of the circuit under one set of conditions. They in no way limit the circuit to be used under different conditions where certain advantages may be achieved. In general, excessive heat generated in the circuit presents the largest factor in degrading the performance of the circuit. For noise immunity greater than 0.5 V and operating speed within 20% of 25°C speed, junction temperature must be kept within 0-125°C. The circuit dissipates 350 mW with V_{CC} = 4.5 V ± 10% and full load. (F/O = 3 CTμL Gates.)

Maximum thermal resistances of the package from junction to air are:

100°C/W in still air 65°C/W with 200 feet/min air flow 50°C/W with 400 feet/min air flow

For example, the circuit may be operated in still air at T_A = 90°C with V_{CC} = 4.5 V ±10%. Higher ambient temperatures are possible in moving air, as can be calculated from the data above.

The outputs of the MμL 9030 may be "OR-ed" with the outputs of different words. Each output terminal represents 8 pF capacitance and 5 μA leakage current. The limit on OR-tying outputs is the degradation of switching speed that the user can tolerate due to added capacitance.

Fan-out of the MμL 9030 can be increased to 15 with only a slight increase in delay by buffering with the CTμL 965.

SWITCHING TIME:

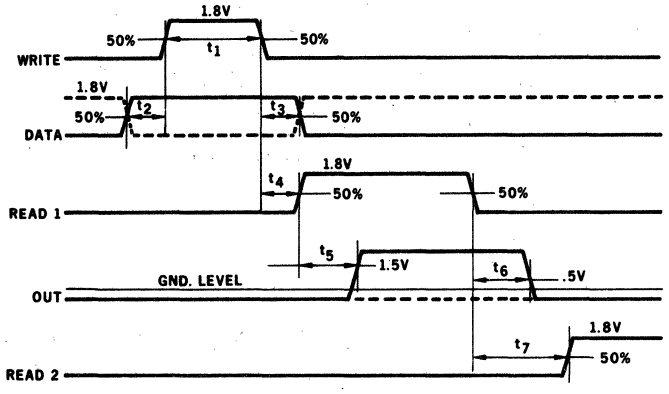
Load Resistance: 1 k to -2 V — Load Capacitance: 10 pF probe and jig capacitance — Input waveform rise and fall time: 6 ns

These tests are for correlations only. While t_1 through t_4 do not change with varied loads, t_5, t_6, and t_7 may differ under different output loading conditions.

SWITCHING TIME:

t_1: 25 ns MIN.
t_2: 10 ns MIN.
t_3: 10 ns MIN.
t_4: 10 ns MIN.
t_5: 25 ns MAX.
t_6: 25 ns MAX.
t_7: 25 ns MIN.

NOTE:
1) DOTTED LINES REPRESENT CELL STORING "LOW" LEVEL.
2) t_7 REPRESENTS TIME INTERVAL BETWEEN READ PULSES FOR ERROR-FREE READOUT.



RTμL COMPOSITE DATA SHEET

INDUSTRIAL MICROLOGIC® INTEGRATED CIRCUITS

OPERATING TEMPERATURE RANGE: 0°C to +70°C (METAL PACKAGE)
15°C to 55°C (EPOXY)

GENERAL DESCRIPTION — The Fairchild Industrial Resistor-Transistor Micrologic® (RTμL) integrated circuit family consists of a number of medium and low power compatible integrated circuits made up by resistor-transistor logic and capable of performing logic functions for use in digital electronic equipment.

The elements of this family are manufactured using the familiar Fairchild Planar* epitaxial process by which all the individual transistors and resistors are diffused into a single silicon wafer, thus assuring a high degree of reliability.

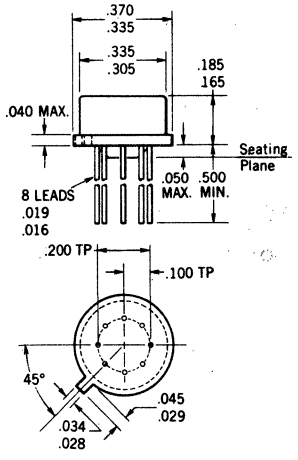
*Planar is a patented Fairchild process.

Some of the important features of the RTμL integrated circuit family are the following:

- Guaranteed operation over the specified temperature range.
- System operates with one power supply (3.6 V±10%).
- Trade-off between fan-out and temperature (permitted).
- RTL uses positive NOR or negative NAND logic.
- High noise immunity — 300 mV.
- Very low propagation delays — typical 12 nanoseconds for medium power gate and 40 nanoseconds for low power gate.
- Power dissipation of typically 2mW per gate for the low power elements.
- Low cost.
- Medium power buffer 9900, dual two-input gate 9914 and JK flip-flop9923 available in epoxy for additional cost advantages.
- Mixing medium and low power elements optimizes fan-out and power dissipation.
- Application briefs, notes and thorough individual data sheets available.

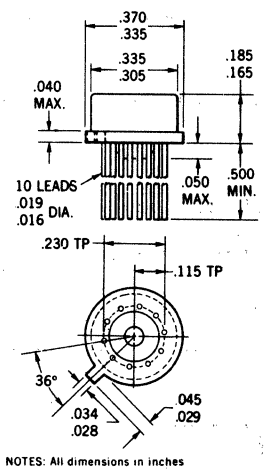
PHYSICAL DIMENSIONS (TO-5 TYPES)

TO-99
(8 pin package)



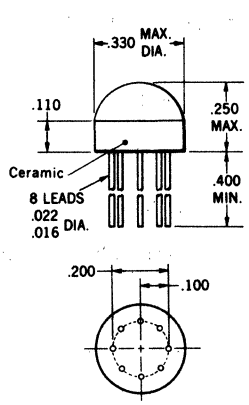
NOTES: All dimensions in inches
Dimensions as per latest J-10 committee
Leads are gold-plated kovar
Weight is 1.12 grams

TO-100
(10 pin package)



NOTES: All dimensions in inches
Leads are gold-plated kovar
Lead No. 1 internally connected to case
Package weight is 1.32 grams

EPOXY PACKAGE
(similar to TO-5)



NOTES: All dimensions in inches
Leads are gold-plated nickel

PURCHASING INFORMATION

Purchasing Agent please note:

To order part, the following numbering system should be used to expedite handling. The complete number will be a nine-digit number with the designations as follows:

A B C D E F G H I

A = U for all elements

BC = 5B for 8-pin (TO-99) pkg.
= 5F for 10-pin (TO-100) pkg.
= 8A for 8-pin epoxy

DEFG = The four-digit number denoting the specific element desired

H = 2 for all elements

I = 9 for 0°C to 70°C for metal packages
= 8 for 15°C to 55°C epoxy pkg.

Note: All elements are available in a metal TO-5 type package, but not necessarily in epoxy. Consult your sales representative for details.

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FAIRCHILD
SEMICONDUCTOR
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LOADING RULES

Industrial Resistor-Transistor Micrologic® (RTμL) integrated circuits consist of low and medium power devices. The primary difference between a low and a medium power element lies in the values of the base and collector resistors associated with each element. The medium power elements have base and collector resistors of 450 Ω and 640 Ω typical, whereas the low power elements have typical base and collector resistors of 1.5 kΩ and 3.6 kΩ respectively.

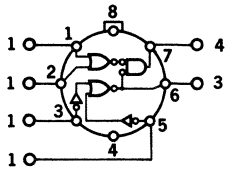
As a result of these differences in resistance values, the input load and output drive factors (maximum input current and minimum output available current) are higher for the medium, and lower for the low power elements.

For purposes of simplification, all input load and output drive factors have been normalized using as a basis the current required to turn on a low-power gate transistor. As a result of this normalization, the input load factor of the 9914 element is 3 and the input load factor of the 9910 element is 1, thus, the 9914 requires three times as much input current. For the output drive factors, the 9910 has an output drive factor four times less than that of the 9914.

The number of elements (bases) that may be driven by an output terminal may consist of any combination of low and medium power elements as long as the sum of all the input load factors does not exceed the output drive factor of the driving element.

LOADING CHART

LOW POWER ELEMENTS:



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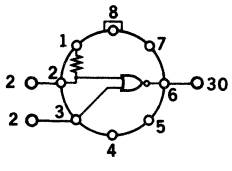

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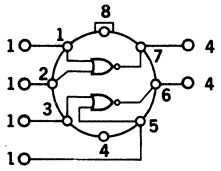

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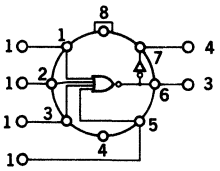

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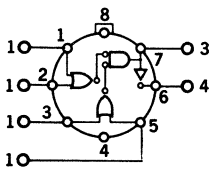

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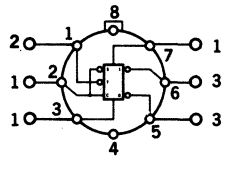

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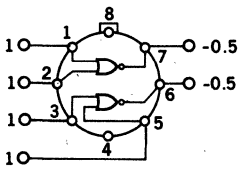
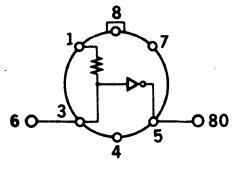


9921

MEDIUM POWER ELEMENTS:



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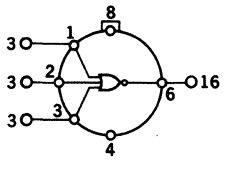

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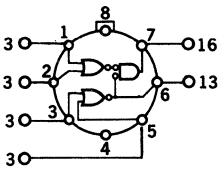

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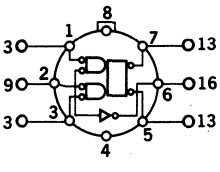

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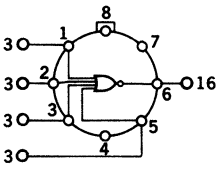

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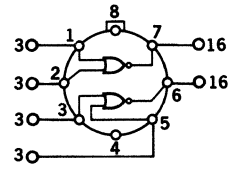

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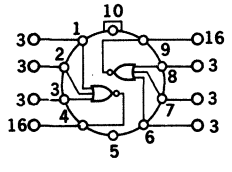

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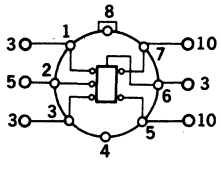

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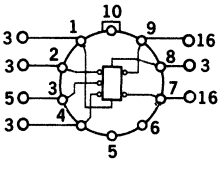

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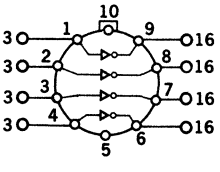


9927

PARALLELING AND OTHER RULES:

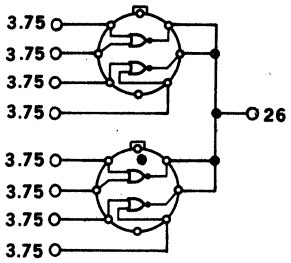
1. All unused input pins should be grounded.

2. On all 8-pin lead devices, V_{CC} is connected to pin 8 and pin 4 is grounded. On 10-pin lead devices, pins 10 and 5 are V_{CC} and Ground pins respectively.

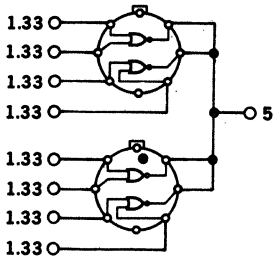
3. For each medium power gate output terminal tied to another medium power gate output terminal (and V_{CC} open on all gates but one) the output drive factor should be reduced by 2 loads.

4. For each low-power gate output terminal tied to another low power gate output terminal (and V_{CC} open on all gates but one) the output drive factor should be reduced by one load.

5. By increasing the input load requirement by 0.75 load for medium power and 0.33 for low power to cover any reduction in base-emitter impedance, any number of gates may be placed in parallel as shown below:



PARALLELING MEDIUM POWER ELEMENTS

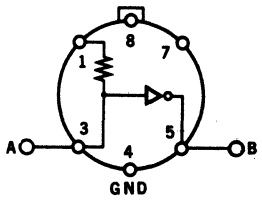


PARALLELING LOW POWER ELEMENTS

● = NO V_{CC} CONNECTED

9900 MEDIUM POWER BUFFER*

The Buffer element is a low-impedance inverting driver circuit. Because of its very low source impedance the element can supply substantially more output current than the basic circuit. As a consequence, the Buffer element is valuable in driving heavily loaded circuits or minimizing rise-time deterioration due to capacitive loading. A resistor is internally connected to the Buffer element input which may be returned to the supply voltage if capacitive coupling is desired. Typical applications of this type connection are astable and monostable multivibrators, and for the differentiation of pulses.

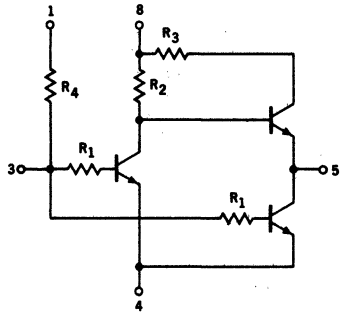


FUNCTIONS

POSITIVE LOGIC:
$B = \overline{A}$

NEGATIVE LOGIC:
$B = \overline{A}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

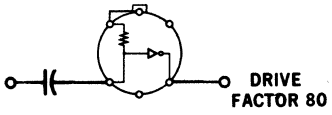
$R_1 = 450\Omega$
$R_2 = 1000\Omega$
$R_3 = 100\Omega$
$R_4 = 1000\Omega$

LOADING RULES

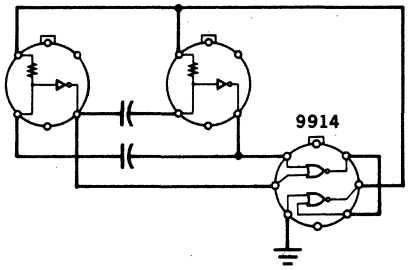
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
3	6	5	80

Note: For more information on loading rules and for parallel combination of elements, see page 2.

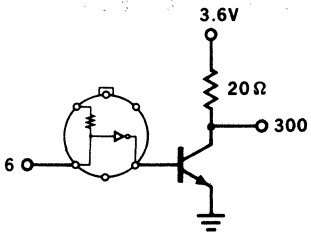
TYPICAL APPLICATIONS



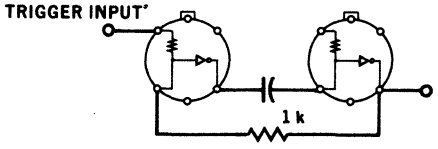
ONE SHOT MULTIVIBRATOR



ASTABLE MULTIVIBRATOR



HIGH FAN-OUT EXTENSION



MONOSTABLE CIRCUIT

* This element also available in the epoxy package.

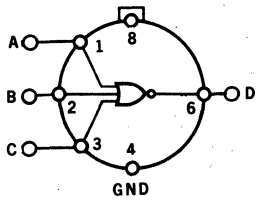
9903 MEDIUM POWER THREE INPUT GATE

The Gate element is a three-input resistor-transistor-logic circuit, one of four similar-basic NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic function through the exclusive use of gate elements. Individual gate elements may be paralleled to increase the number of inputs to a single output node (subject to loading rules), or combined with other Micrologic® integrated circuits to augment their logic functions.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC: $D = \overline{A + B + C}$

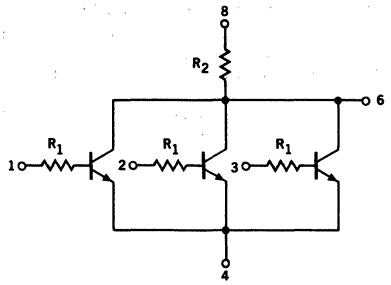
$= \overline{A}\,\overline{B}\,\overline{C}$

NEGATIVE LOGIC: $D = \overline{A\,B\,C}$

$= \overline{A} + \overline{B} + \overline{C}$

Note: Pins 5 and 7 omitted.

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 650\Omega$

TRUTH TABLE

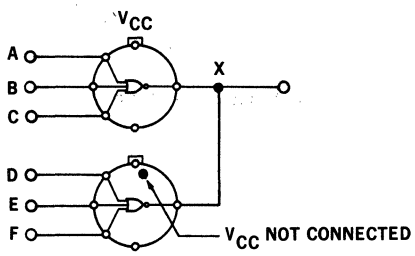
A	B	C	D
H	H	H	L
H	H	L	L
H	L	H	L
H	L	L	L
L	H	H	L
L	H	L	L
L	L	H	L
L	L	L	H

LOADING RULES

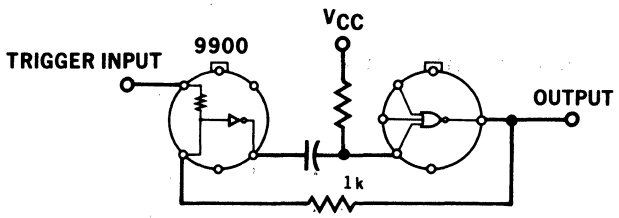
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTORS
1	3	6	16
2	3		
3	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



SIX INPUT GATE



MONOSTABLE CIRCUIT

POSITIVE LOGIC:
$\overline{A + B + C + D + E + F} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F}$

NEGATIVE LOGIC:
$\overline{A \cdot B \cdot C \cdot D \cdot E \cdot F} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F}$

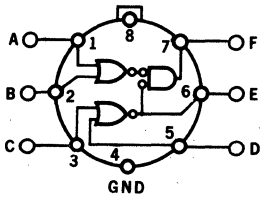
9904 MEDIUM POWER HALF ADDER

The Half-Adder element is a multipurpose combination of three basic circuits. The configuration is well-suited as a complete half-adder, an exclusive OR gate, or any other similar logic construction. Output No. 7 is a noninverting function of the four inputs, whereas output No. 6 may be considered as either a NAND or a NOR gate.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC: $E = \overline{C + D}$, $F = (A + B)(C + D)$

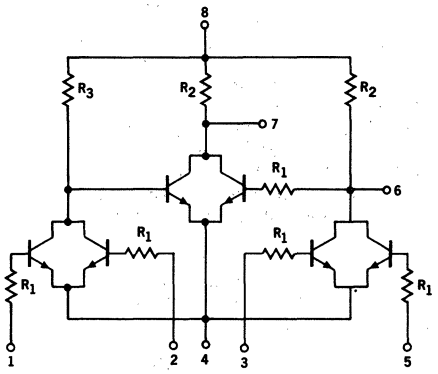
NEGATIVE LOGIC: $E = \overline{C}\,\overline{D}$, $F = AB + CD$

IF $C = \overline{A}$ and $D = \overline{B}$

POSITIVE LOGIC: $E = AB$, $F = A\overline{B} + \overline{A}B$

NEGATIVE LOGIC: $E = A + B$, $F = AB + \overline{C}\,\overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$
$R_3 = 800\Omega$

TRUTH TABLE

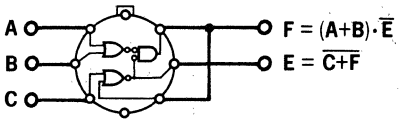
INPUTS				OUTPUTS	
1	2	3	5	7	6
H	H	H	H	H	L
L	H	H	H	H	L
H	L	H	H	H	L
H	H	L	H	H	L
H	H	H	L	H	L
L	L	H	H	L	L
L	H	L	H	H	L
L	H	H	L	H	L
H	L	L	H	H	L
H	L	H	L	H	L
H	H	L	L	L	H
L	L	L	H	L	L
L	H	L	L	L	H
L	L	H	L	L	L
H	L	L	L	L	H
L	L	L	L	L	H

LOADING RULES

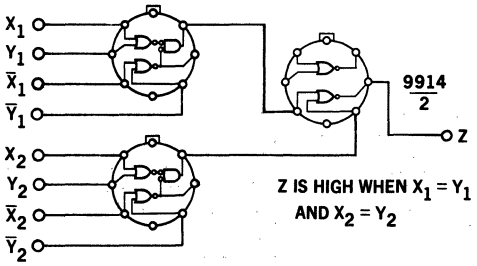
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTORS
1	3	6	16
2	3	7	13
3	3		
5	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



GATED FLIP - FLOP



PARALLEL COMPARISON

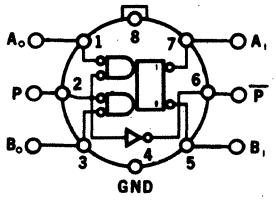
9905 MEDIUM POWER HALF SHIFT REGISTER

The Half Shift Register element is a gated input storage element composed of five basic gate circuits. Internal cross-connection of the two output gate circuits provides memory. The input gating signal is applied to the remaining three gate circuits. Two of these control the logic inputs, while the third provides the complement of the gating signal at an output pin. Because of the two cascaded internal logic levels, the unit changes state in response to near-ground input signals. Consequently, from a terminal standpoint, the unit should be regarded as requiring NAND input logic levels. Concurrent near-ground signals at all three inputs will cause near-ground signals at both outputs.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

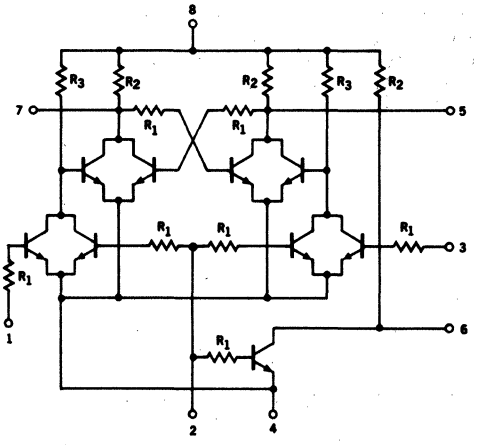


FUNCTIONS

POSITIVE LOGIC: $A_I = \overline{B_I}\,(A_0 + P)$, $B_I = \overline{A_I}\,(B_0 + P)$

NEGATIVE LOGIC: $A_I = \overline{B_I} + A_0P$, $B_I = \overline{A_I} + B_0P$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$
$R_3 = 800\Omega$

TRUTH TABLE

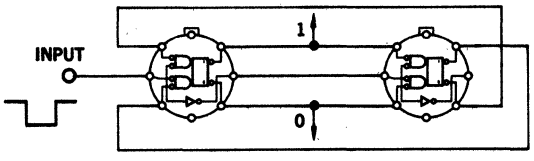
INPUT			OUTPUT	
A_0	P	B_0	A_I	B_I
H	H	H	H	L
H	H	L	H	L
H	L	H	H	L
H	L	L	H	L
L	H	H	L	H
L	H	L	L	H
L	L	H	L	H
L	L	L	L	L

LOADING RULES

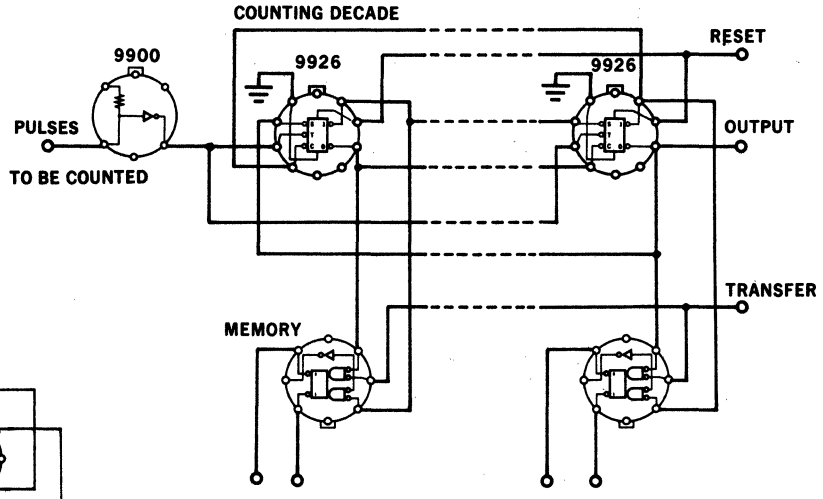
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	3	5	13
2	9	6	16
3	3	7	13

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



COMPLEMENTARY FLIP-FLOP



COUNTING DECADE WITH MEMORY

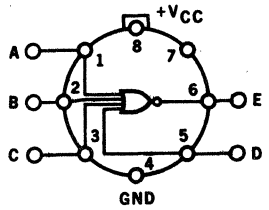
9907 MEDIUM POWER FOUR INPUT GATE

The Four-Input Gate element is a four-input resistor-transistor-logic circuit, one of four similar NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic-function through the exclusive use of four-input gate elements. Individual four-input gate elements may be paralleled to increase the number of inputs to a single output node (subject to loading rules), or combined with other Micrologic® integrated circuits to augment their logic functions. This element performs the AND and exclusive OR function. It is also used to select one of two data streams under control of a single gate signal.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

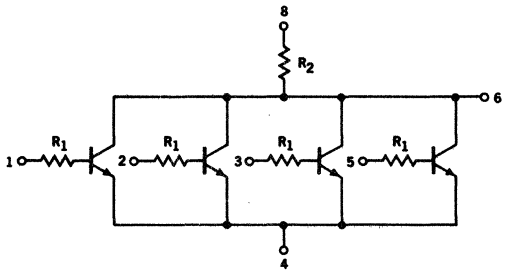


FUNCTIONS

POSITIVE LOGIC: $E = \overline{A + B + C + D}$
$= \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$

NEGATIVE LOGIC: $E = \overline{A\,B\,C\,D}$
$= \overline{A} + \overline{B} + \overline{C} + \overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$

TRUTH TABLE

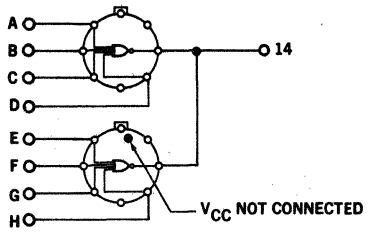
INPUTS				OUTPUT
A	B	C	D	E
H	H	H	H	L
H	H	H	L	L
H	H	L	H	L
H	H	L	L	L
H	L	H	H	L
H	L	H	L	L
H	L	L	H	L
H	L	L	L	L
L	H	H	H	L
L	H	H	L	L
L	H	L	H	L
L	H	L	L	L
L	L	H	H	L
L	L	H	L	L
L	L	L	H	L
L	L	L	L	H

LOADING RULES

INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTORS
1	3	6	16
2	3		
3	3		
5	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



EIGHT INPUT GATE

POSITIVE LOGIC:
$\overline{A + B + C + D + E + F + G + H} = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F}\,\overline{G}\,\overline{H}$

NEGATIVE LOGIC:
$\overline{A\,B\,C\,D\,E\,F\,G\,H} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

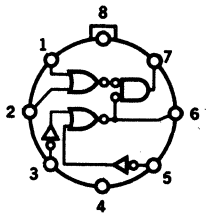
9908 LOW POWER ADDER

This element performs the AND and exclusive OR function. It is also used to select one of two data streams under control of a single gate signal.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

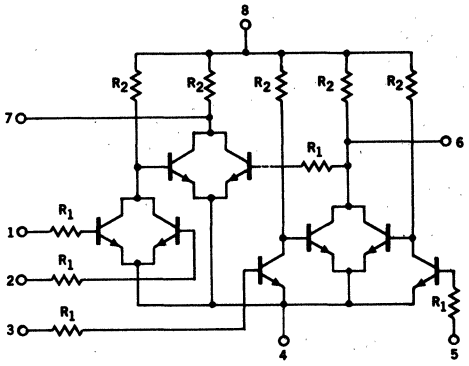


FUNCTIONS

POSITIVE LOGIC:
$6 = (\overline{3} + \overline{5}) = 3 \cdot 5$
$7 = (1 + 2)(\overline{3} + \overline{5})$

NEGATIVE LOGIC:
$6 = (\overline{3} \cdot \overline{5}) = 3 + 5$
$7 = 1 \cdot 2 + \overline{3} \cdot \overline{5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

I, Output "6"

3	5	6
L	L	L
L	H	L
H	L	L
H	H	H

II, Output "7"

1	2	6	7
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

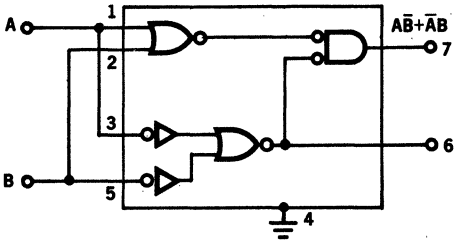
LOADING RULES

INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	3
2	1	7	4
3	1		
5	1		

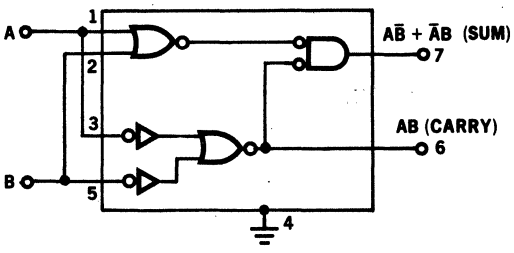
* For loading rule explanations see page 10.

Note: For more information on loading rules and for parallel combination of elements, see page 2.

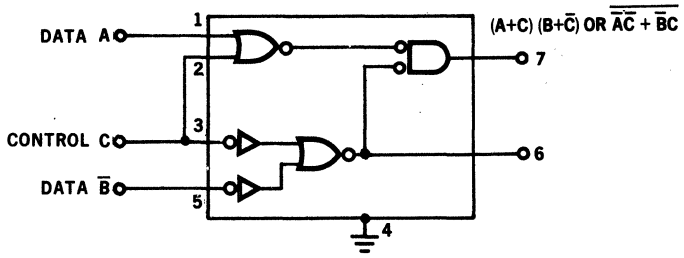
TYPICAL APPLICATIONS (POSITIVE LOGIC)



EXCLUSIVE OR GATE



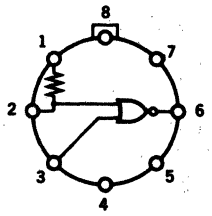
HALF ADDER



DATA STREAM SWITCH

9909 LOW POWER BUFFER

This element is a low-output impedance, two-input inverting driver. It can supply substantially more output current than the basic circuit to provide higher fan-out or drive capacitive loads. A resistor is connected internally to one of the inputs which may be returned to the supply voltage if capacitive coupling is desired.

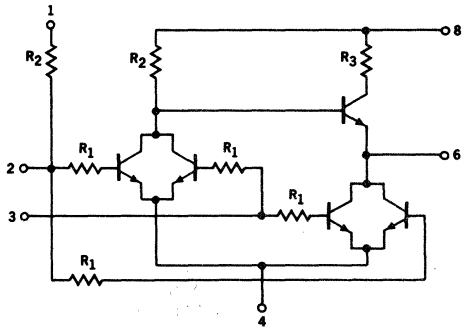


FUNCTIONS

POSITIVE LOGIC:
$6 = \overline{2 + 3}$

NEGATIVE LOGIC:
$6 = \overline{2 \cdot 3}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

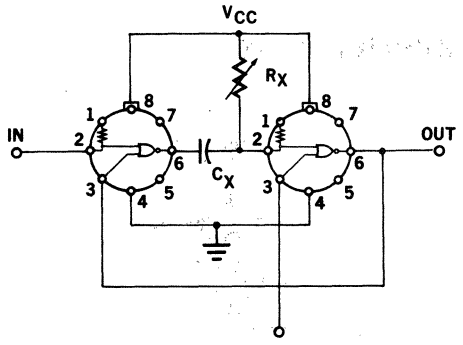
$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$
$R_3 = 100\Omega$

LOADING RULES

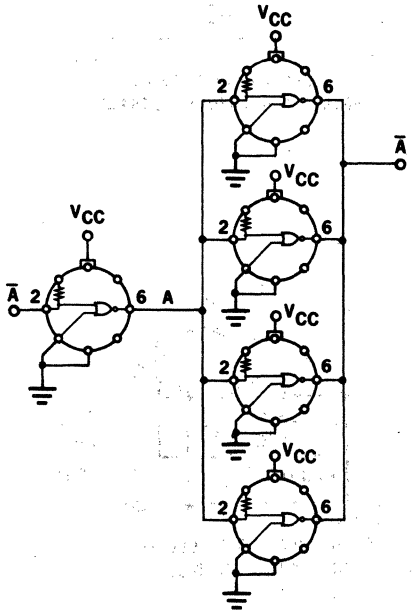
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
2	2	6	30
3	2		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

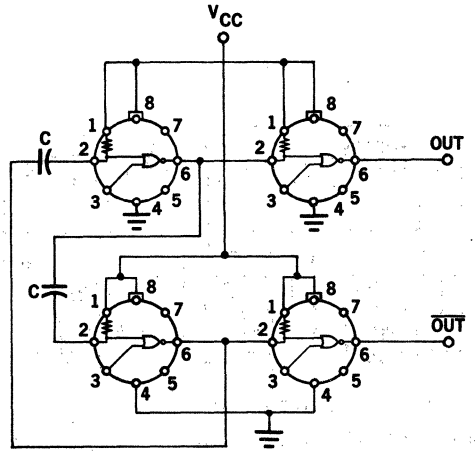
TYPICAL APPLICATIONS



ONE SHOT MULTIVIBRATOR



PARALLEL PULSE DRIVER



FOUR BUFFERS CONNECTED AS FREE RUNNING MULTIVIBRATOR

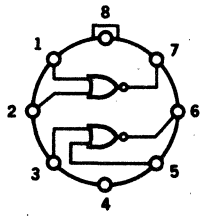
9910 LOW POWER DUAL GATE

This element can be used on a NOR gate, Double Inverter RS flip-flop or as a pair of Inverters. It can also be used with the gate expander to increase its fan-in capacity.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

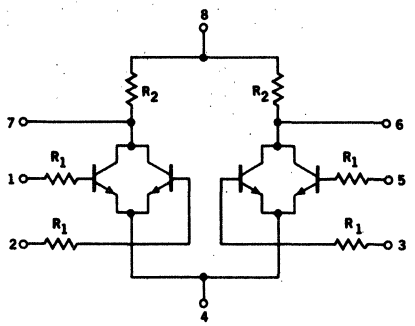


FUNCTIONS

POSITIVE LOGIC:
$7 = \overline{1 + 2}$
$6 = \overline{3 + 5}$

NEGATIVE LOGIC:
$7 = \overline{1 \cdot 2}$
$6 = \overline{3 \cdot 5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

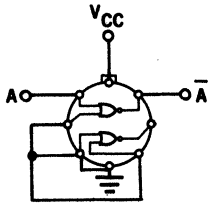
OUTPUT 7			OUTPUT 6		
1	2	7	3	5	6
L	L	H	L	L	H
L	H	L	L	H	L
H	L	L	H	L	L
H	H	L	H	H	L

LOADING RULES

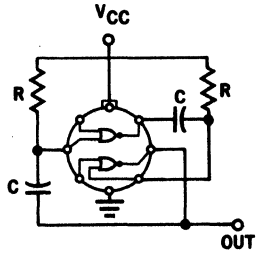
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	4
2	1	7	4
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

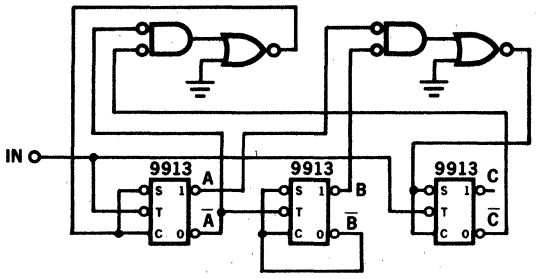
TYPICAL APPLICATIONS



SIMPLE INVERTER

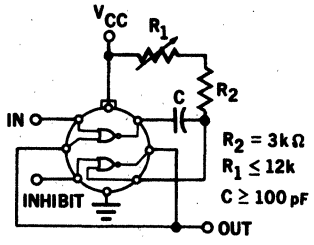


SINGLE DUAL GATE AS
FREE-RUNNING MULTIVIBRATOR



MOD - 5 BINARY COUNTER

Function: To count to a Modulo of 5 using a 1-2-4 code, or to divide an input frequency by a factor of 5.



SINGLE DUAL GATE USED AS
A ONE-SHOT MULTIVIBRATOR

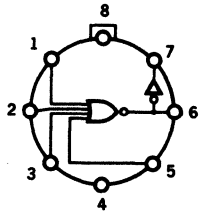
9911 LOW POWER DUAL GATE WITH INVERTER

This element is a general purpose four-input gate with inverter for NOR, OR functions and can also be used as an amplifier-inverter.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC:

$7 = \overline{1 + 2 + 3 + 5}$

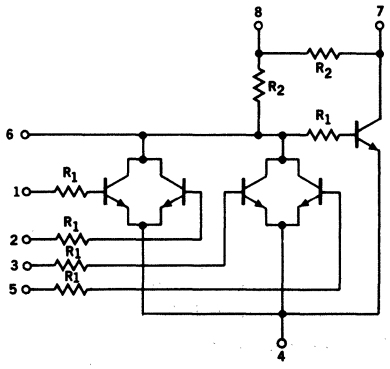
$6 = \overline{1 + 2 + 3 + 5}$

NEGATIVE LOGIC:

$7 = \overline{1 \cdot 2 \cdot 3 \cdot 5}$

$6 = \overline{1 \cdot 2 \cdot 3 \cdot 5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

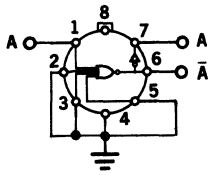
1	2	3	5	6	7
L	L	L	L	H	L
L	L	L	H	L	H
L	L	H	L	L	H
L	L	H	H	L	H
L	H	L	L	L	H
L	H	L	H	L	H
L	H	H	L	L	H
L	H	H	H	L	H
H	L	L	L	L	H
H	L	L	H	L	H
H	L	H	L	L	H
H	L	H	H	L	H
H	H	L	L	L	H
H	H	L	H	L	H
H	H	H	L	L	H
H	H	H	H	L	H

LOADING RULES

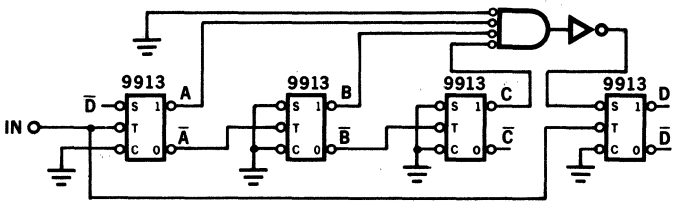
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	3
2	1	7	4
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



CONNECTED AS INVERTER-AMPLIFIER



MODULO 9 BINARY COUNTER

Function: To count to a Modulo of 9 using 1-2-4-8 code, or to divide an input frequency by a factor of 9.

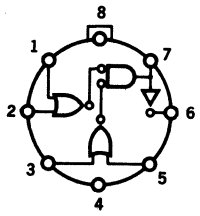
9912 LOW POWER HALF ADDER

This element is a multipurpose combination of three basic circuits that can be used as a complete half adder, an exclusive OR gate, gated-set flip-flop or any other similar logic construction.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC:

$7 = (1 + 2) \cdot (3 + 5)$

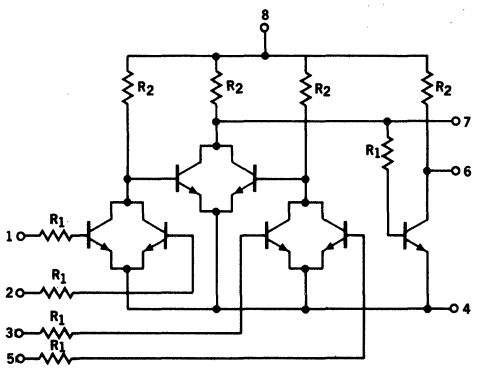
$6 = \overline{1} \cdot \overline{2} + \overline{3} \cdot \overline{5}$

NEGATIVE LOGIC:

$7 = 1 \cdot 2 + 3 \cdot 5$

$6 = (\overline{1} + \overline{2}) \cdot (\overline{3} + \overline{3})$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

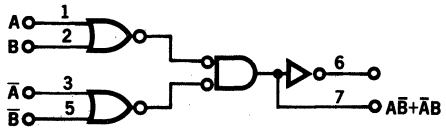
1	2	3	5	6	7
L	L	L	L	H	L
L	L	L	H	H	L
L	L	H	L	H	L
L	L	H	H	H	L
L	H	L	L	H	L
L	H	L	H	L	H
L	H	H	L	L	H
L	H	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	L	H	L	L	H
H	L	H	H	L	H
H	H	L	L	H	L
H	H	L	H	L	H
H	H	H	L	L	H
H	H	H	H	L	H

LOADING RULES

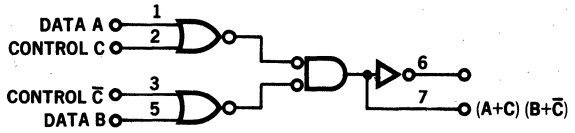
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	4
2	1	7	3
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

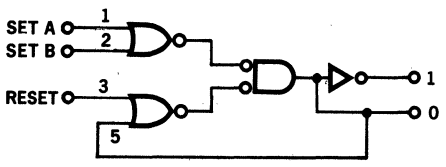
TYPICAL APPLICATIONS (POSITIVE LOGIC)



EXCLUSIVE OR GATE OR HALF ADDER



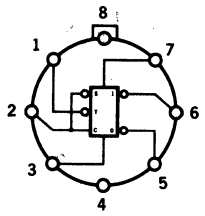
DATA STREAM SWITCH



GATED R-S FLIP-FLOP

9913 LOW POWER TYPE D FLIP FLOP

The 9913 is a gated flip-flop very suitable for shift registers and control circuitry. The state of the input at pin 2 is stored in the element when the input at pin 1 changes from logical "1" to logical "0." The element can be reset only when pin 1 is maintained at a logical "1" during the time that pin 7 undergoes a change from a logical "0" to a logical "1."

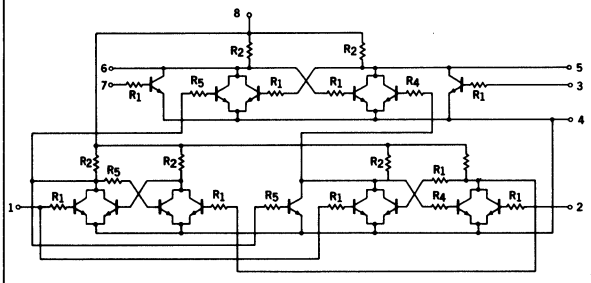


FUNCTIONS

DIRECT INPUTS[1]				GATED INPUT[3]		
				t = n	t = n	t = n + 1
3	7	6	5	2	6	5
L	L	NC	NC[2]	H	H	L
L	H	L	H	L	L	H
H	L	H	L			
H	H	L	L			

(1) Pin 1 must be high.
(2) NC = No change.
(3) Pins 3 and 7 must be low.

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$
$R_4 = 180\Omega$
$R_5 = 480\Omega$

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

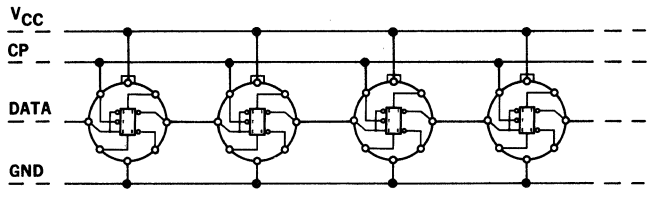
NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

LOADING RULES

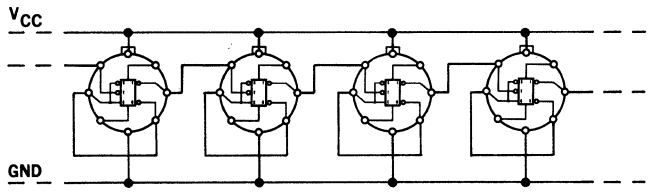
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	2	5	3
2	1	6	3
3	1		
7	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

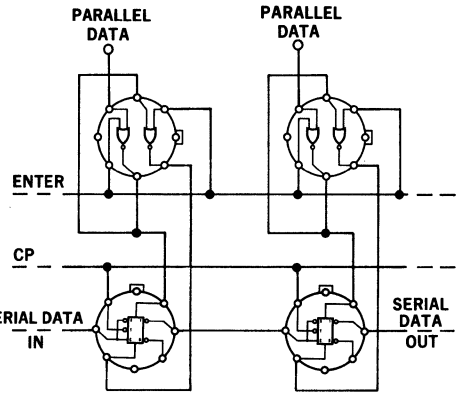
TYPICAL APPLICATIONS



SHIFT REGISTER STAGES USING TYPE D FLIP-FLOP



BINARY RIPPLE CARRY COUNTER STAGES USING TYPE D FLIP-FLOP



METHOD OF PARALLEL ENTRY OF DATA INTO SHIFT REGISTER
V_{CC} AND GROUND CONNECTIONS ARE NOT SHOWN

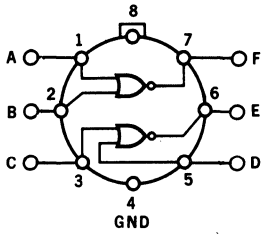
9914 MEDIUM POWER DUAL TWO INPUT GATE*

The Dual Two-Input Gate element is a dual combination of two-input resistor-transistor-logic circuits, one of four similar basic NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic-function through the exclusive use of dual two-input gate elements. In addition to the applications of other gate-type elements, the dual two-input gate element circuits may be cross-connected to form a flip-flop, or in tandem to form noninverting gates.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

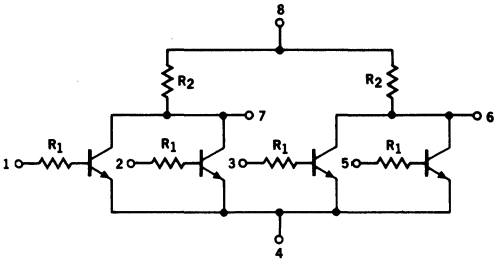


FUNCTIONS

POSITIVE LOGIC:
$F = \overline{A + B} = \overline{A}\,\overline{B}$
$E = \overline{C + D} = \overline{C}\,\overline{D}$

NEGATIVE LOGIC:
$F = \overline{A}\,\overline{B} = \overline{A} + \overline{B}$
$E = \overline{C}\,\overline{D} = \overline{C} + \overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES
$R_1 = 450\Omega$
$R_2 = 640\Omega$

TRUTH TABLE

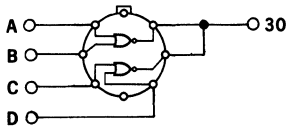
A	B	F
H	H	L
H	L	L
L	H	L
L	L	H

LOADING RULES

INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTOR
1	3	6	16
2	3	7	16
3	3		
5	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

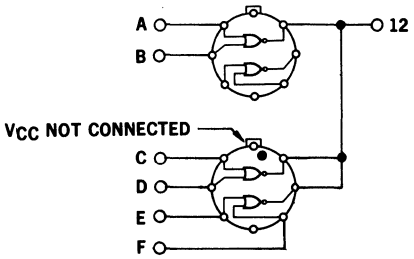
TYPICAL APPLICATIONS



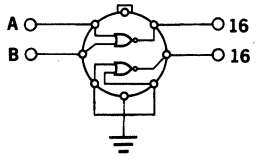
FOUR INPUT GATE

POSITIVE LOGIC:
$\overline{A + B + C + D} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$

NEGATIVE LOGIC:
$\overline{A\,B\,C\,D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$



SIX INPUT GATE



TWO INPUT GATE

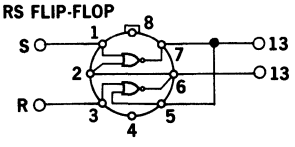
POSITIVE LOGIC:
$\overline{A + B} = \overline{A} \cdot \overline{B}$

NEGATIVE LOGIC:
$\overline{A \cdot B} = \overline{A} + \overline{B}$

PIN NUMBERS			
INPUT		OUTPUT	
1	3	6	7
L	L	NC	NC
L	H	L	H
H	L	H	L
H	H	NOT ALLOWED	

NC = No change.

RS FLIP-FLOP



* This element also available in the epoxy package.

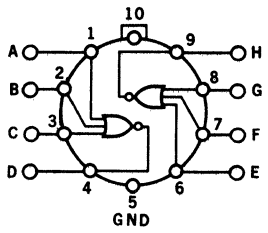
9915 MEDIUM POWER DUAL THREE INPUT GATE

The Dual Three-Input Gate element is a dual combination of three-input resistor-transistor-logic circuits, one of four similar basic NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic-function through the exclusive use of dual three-input gate elements. In addition to the applications of other gate-type elements, the dual three-input gate element circuits may be cross-connected to form a flip-flop with 2 set and 2 reset inputs, or in tandem to form non-inverting gates.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

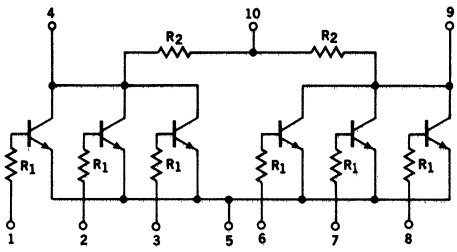


FUNCTIONS

POSITIVE LOGIC:
$D = \overline{A + B + C} = \overline{A}\,\overline{B}\,\overline{C}$
$H = \overline{E + F + G} = \overline{E}\,\overline{F}\,\overline{G}$

NEGATIVE LOGIC:
$D = \overline{A\,B\,C} = \overline{A} + \overline{B} + \overline{C}$
$H = \overline{E\,F\,G} = \overline{E} + \overline{F} + \overline{G}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$

TRUTH TABLE

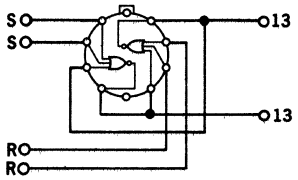
A	B	C	D
H	H	H	L
H	H	L	L
H	L	H	L
H	L	L	L
L	H	H	L
L	H	L	L
L	L	H	L
L	L	L	H

LOADING RULES

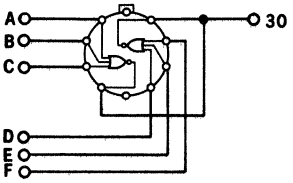
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTORS
1	3	4	16
2	3	9	16
3	3		
6	3		
7	3		
8	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



RS FLIP-FLOP



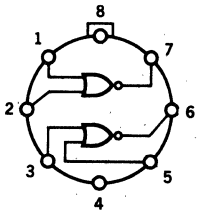
SIX INPUT GATE

POSITIVE LOGIC:
$\overline{A + B + C + D + E + F} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F}$

NEGATIVE LOGIC:
$\overline{A \cdot B \cdot C \cdot D \cdot E \cdot F} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F}$

9921 LOW POWER GATE EXPANDER

This element is a double gate without the node resistors. Its output terminals may be connected in parallel to those of the 9910 or 9911 elements to increase the fan-in capability of the circuit. Pin 8 of the element must always be connected to V_{CC}.



FUNCTIONS

POSITIVE LOGIC:

$7 = \overline{1 + 2}$

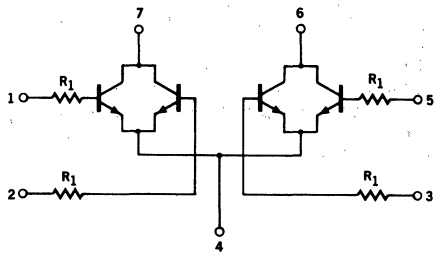
$6 = \overline{3 + 5}$

NEGATIVE LOGIC:

$7 = \overline{1 \cdot 2}$

$6 = \overline{3 \cdot 5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

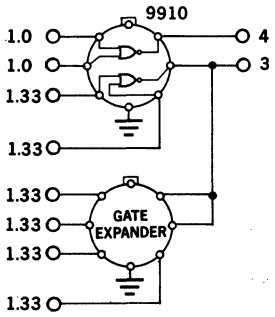
$R_1 = 1.5k\Omega$

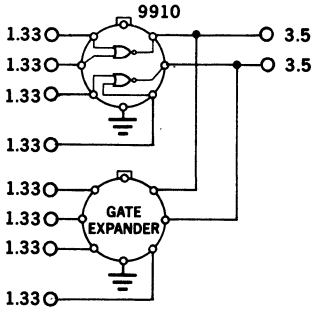
LOADING RULES

INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTORS
1	1	6	–0.5
2	1	7	–0.5
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

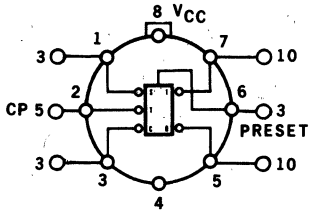
TYPICAL APPLICATIONS





9923 MEDIUM POWER JK FLIP FLOP*

The 9923 Industrial Flip-Flop is a fully integrated, monolithic circuit. This element is designed for use in industrial shift-register and binary counting applications. The 9923 JK Flip-Flop is compatible with the basic Industrial Micrologic® integrated circuit family and is guaranteed to operate at a frequency of 2.0 MHz minimum over the 0°C to 70°C temperature range.

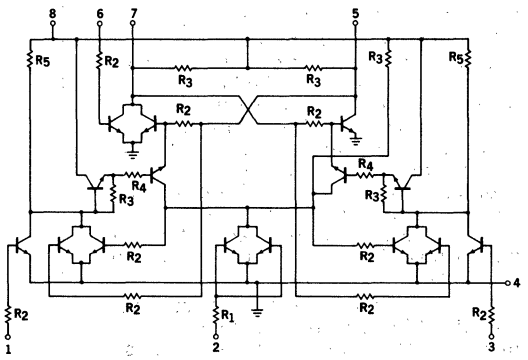


FUNCTIONS

SET (1)	CLEAR (3)	OUTPUT (7)
	t = n	t = n +1
H	H	X^n
H	L	H
L	H	L
L	L	$\overline{X^n}$

H = HIGH
L = LOW
X IS THE OUTPUT STATE AT TIME n
A HIGH ON PIN 6 WILL PRESET OUTPUT PIN 7 LOW

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

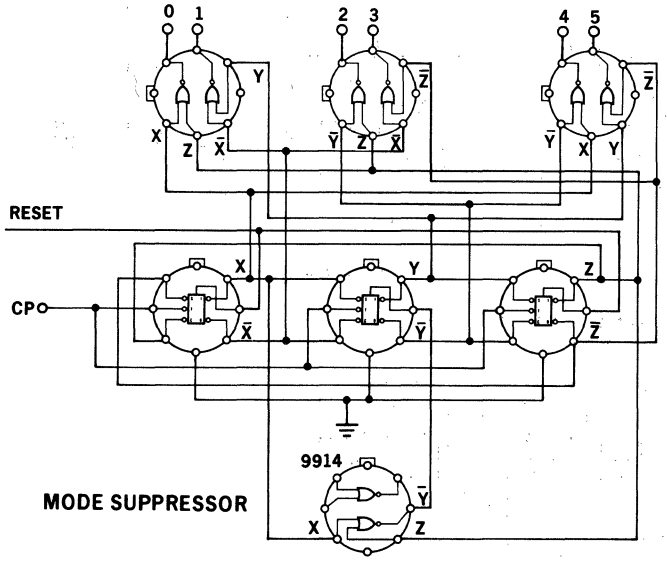
$R_1 = 260\Omega$ $R_4 = 300\Omega$
$R_2 = 450\Omega$ $R_5 = 700\Omega$
$R_3 = 640\Omega$

LOADING RULES

INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	3	5	10
2	5	6	3
3	3	7	10

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



MOD 6 SHIFT REGISTER COUNTER WITH DECODING

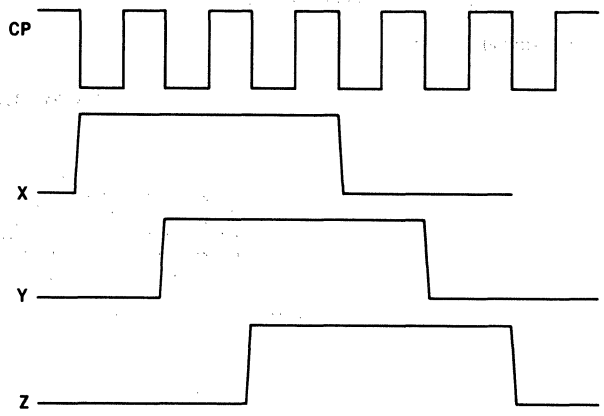
TRUTH TABLE

CT	X	Y	Z
0	L	L	L
1	H	L	L
2	H	H	L
3	H	H	H
4	L	H	H
5	L	L	H

DECODING

1	2
X	Z
$\overline{X}$	Y
$\overline{Y}$	Z
$\overline{X}$	$\overline{Z}$
X	$\overline{Y}$
Y	$\overline{Z}$

TIME DIAGRAM:



* This element also available in the epoxy package.

9926 MEDIUM POWER JK FLIP FLOP

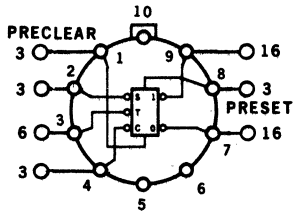
The Fairchild JK Flip-Flop is a complete, general-purpose, storage element suitable for use in shift registers, counters or any type of control function.

The JK Flip-Flop differs from ordinary RS Flip-Flops in that no ambiguous output state can result from simultaneous one inputs. In the JK Flip-Flop simultaneous ones on both the set and clear inputs cause the output state to toggle (reverse). This feature enhances the operation of the JK Flip-Flop in binary counters, as no external feedback connections are required. The toggling action can also be used to advantage for minimizing the logic structure of control units.

The unique input triggering circuit permits the JK Flip-Flop to respond to negative clock pulse transitions as short as 1 nanosecond or as long as 100 nanoseconds.

Asynchronous preset and preclear inputs are included for presetting counters, inserting parallel data in registers, and similar applications.

This element is guaranteed to operate at a frequency of 8.0 MHz minimum (20.0 MHz typical) over the 0°C to 70°C temperature range.

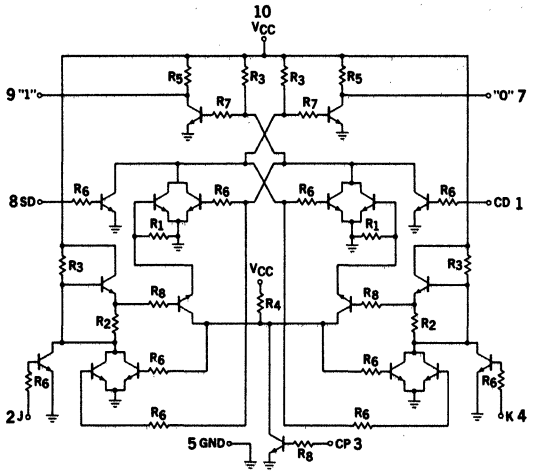


FUNCTIONS

SET (2)	CLEAR (4)	OUTPUT (9)
t = n		t = n +1
H	H	X^n
H	L	H
L	H	L
L	L	$\overline{X^n}$

H = HIGH
L = LOW
X IS THE OUTPUT STATE AT TIME n

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

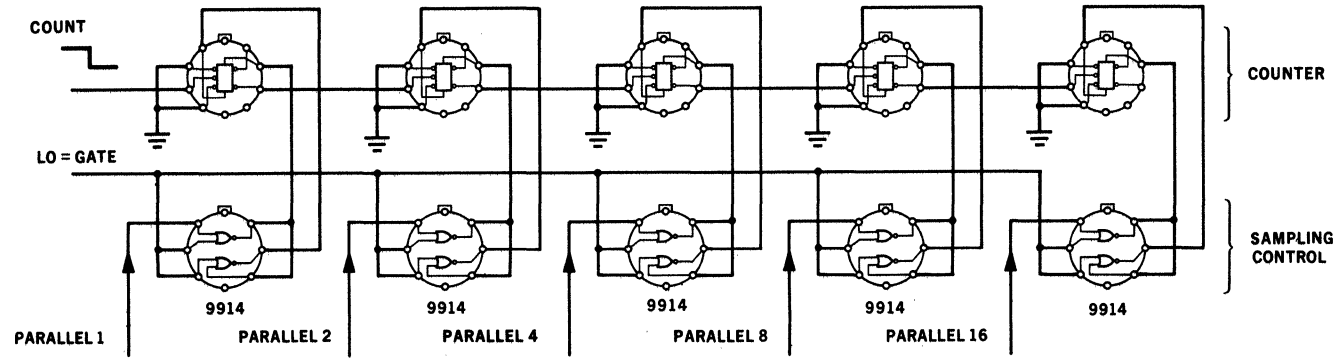
$R_1 = 3k\Omega$ $R_3 = 900\Omega$ $R_5 = 640\Omega$ $R_7 = 550\Omega$
$R_2 = 1.0k\Omega$ $R_4 = 700\Omega$ $R_6 = 600\Omega$ $R_8 = 300\Omega$

LOADING RULES

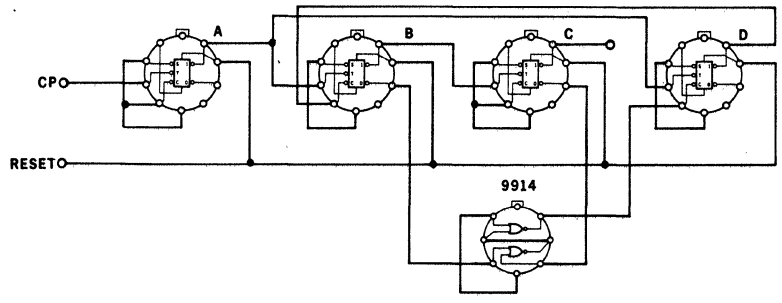
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTOR
1	3	7	16
2	3	8	3
3	6	9	16
4	3		

Pin configurations for TO-5, Cerpak and Flatpack are identical.

TYPICAL APPLICATIONS



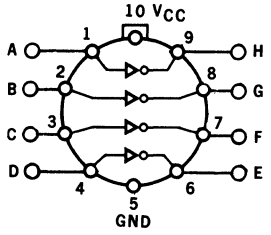
BINARY COUNTER AND SAMPLING CONTROL



1-2-4-8, MOD 10, COUNT UP COUNTER (POSITIVE LOGIC)

9927 MEDIUM POWER QUAD INVERTER

The Quad Inverter element is a four-input resistor-transistor-logic inverter circuit. This circuit is very useful where a complement of several signals is desired simultaneously.

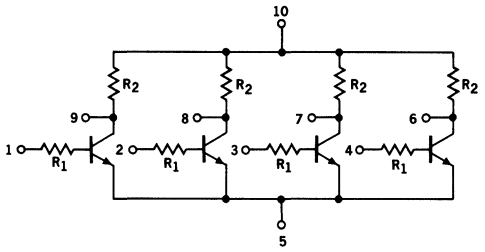


FUNCTIONS

POSITIVE AND NEGATIVE LOGIC:

$H = \overline{A}$
$G = \overline{B}$
$F = \overline{C}$
$E = \overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

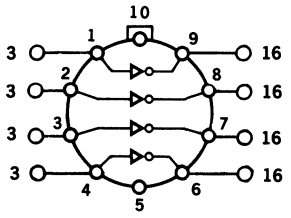
$R_1 = 450\Omega$
$R_2 = 640\Omega$

LOADING RULES

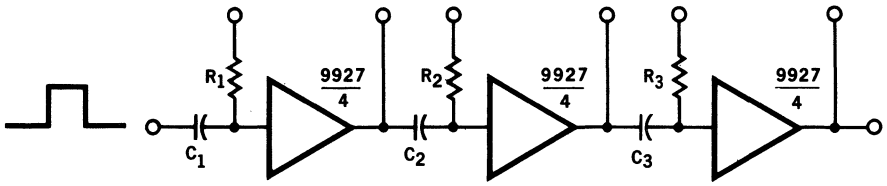
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTOR
1	3	6	16
2	3	7	16
3	3	8	16
4	3	9	16

Note:
For more information on loading rules and for parallel combination of elements, see page 2.

LOADING CHART



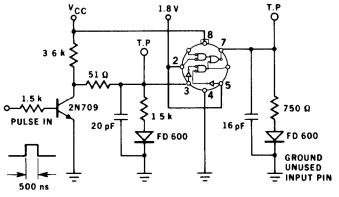
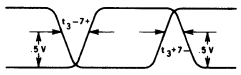
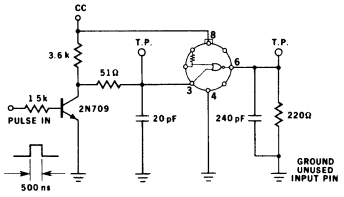
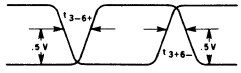
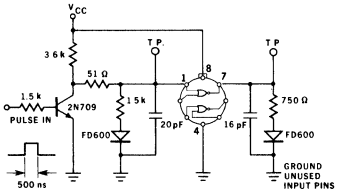
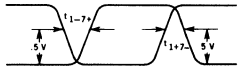
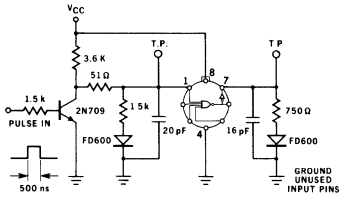
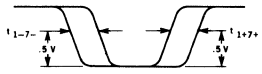
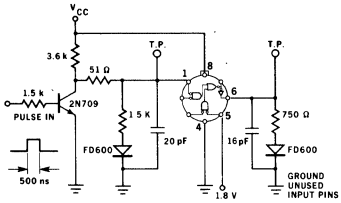
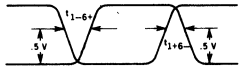
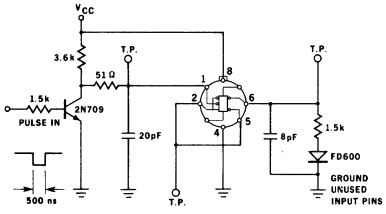
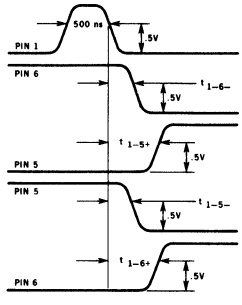
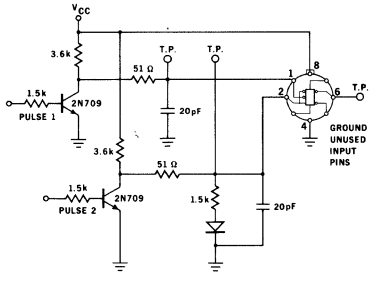
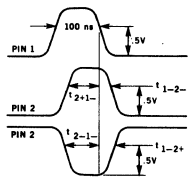
TYPICAL APPLICATIONS



DELAY INTRODUCED IN EACH STAGE IS A FUNCTION OF RC TIME CONSTANT

PULSE DELAY/SHAPER CIRCUIT

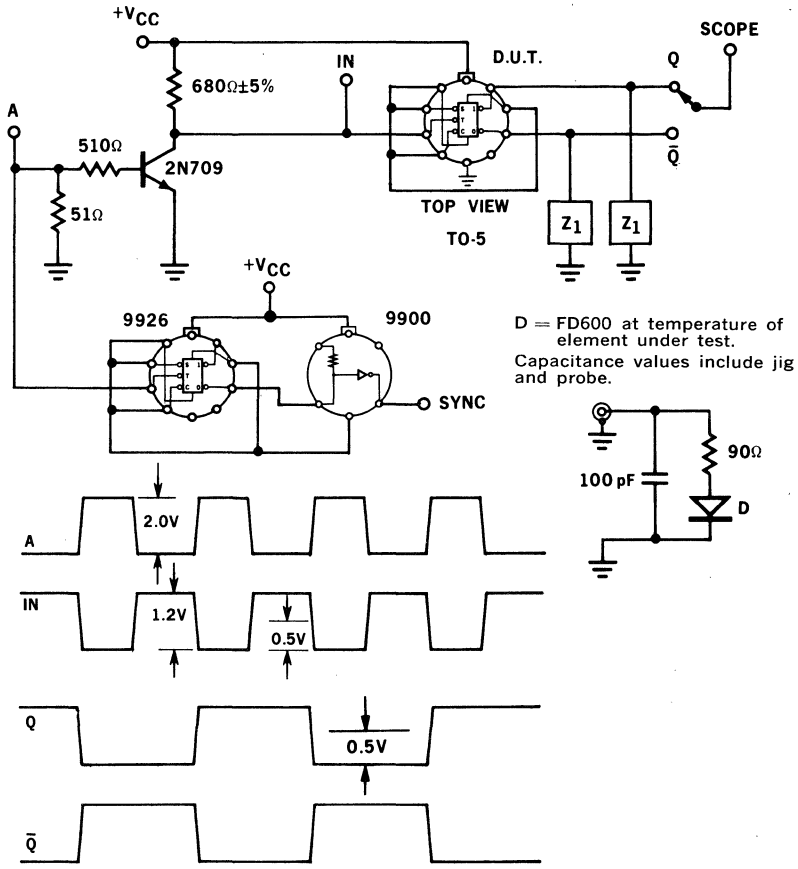
LOW POWER ELEMENTS -- PROPAGATION DELAY GUARANTEED LIMITS

ELEMENT		ns(max)		
9908	t_{3-7+} t_{3+7-}	80 100		
9909	t_{3+6-} t_{3-6+}	90 70		
9910	t_{1-7+} t_{1+7-}	40 50		
9911	t_{1-7-} t_{1+7+}	70 90		
9912	t_{1+6-} t_{1-6+}	100 80		
9913	t_{1-5-}, t_{1-6-} t_{1-5+}, t_{1-6+}	80 120		
	t_{2+1-}, t_{1-2+} t_{1-2-}, t_{2-1-}	60 min 30 min		

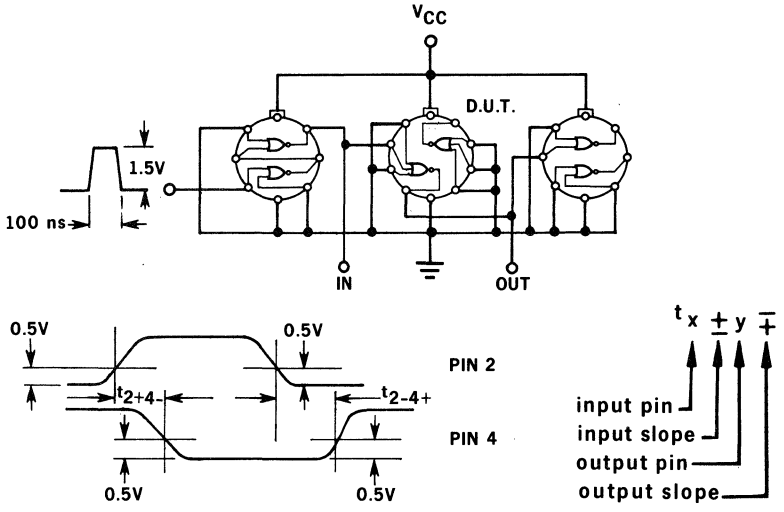
MEDIUM POWER ELEMENTS -- PROPAGATION DELAY GUARANTEED LIMITS

ELEMENT		MAX.
9900	t_{3-5-}	32 ns
	t_{3+5-}	32 ns
9903	t_{2+6-}	20 ns
	t_{2-6+}	32 ns
9905	t_{2+6-}	30 ns
	t_{2-6+}	26 ns
	t_{1+7+}	42 ns
	t_{1-7-}	42 ns
9904	t_{3+6-}	20 ns
	t_{3-6+}	32 ns
	t_{1+7+}	38 ns
	t_{1-7-}	38 ns
9907	t_{2+6-}	20 ns
	t_{2-6+}	32 ns
9914	t_{1+7-}	20 ns
	t_{1-7+}	32 ns
9915	t_{2+4-}	20 ns
	t_{2-4+}	32 ns
9923	t_{2-7+}	80 ns
	t_{2-7-}	50 ns
	t_{2-5+}	80 ns
	t_{2-5-}	50 ns
9926	t_{3-9+}	60 ns
	t_{3-9-}	60 ns
	t_{3-7+}	60 ns
	t_{3-7-}	60 ns
9927	t_{2+8-}	20 ns
	t_{2-8+}	32 ns

PROPAGATION DELAY AND TOGGLE TEST CIRCUIT FOR JK 9923 OR 9926



SWITCHING TIME TEST CIRCUIT: (FOR A GATE TYPE DEVICE)



Switching time test circuit shown above is for μL 9915, but the input and output loading circuit shown is the same for Micrologic 9900, 9903, 9904, 9905, 9907, 9914, and 9927 elements. By appropriately connecting the input and output pins of the device under test (D.U.T.) in the circuit above, switching speeds could be measured in any of the said elements.

9997 FOUR BIT SHIFT REGISTER

INDUSTRIAL MICROLOGIC® INTEGRATED CIRCUIT

OPERATING TEMPERATURE RANGE 0°C TO 70°C

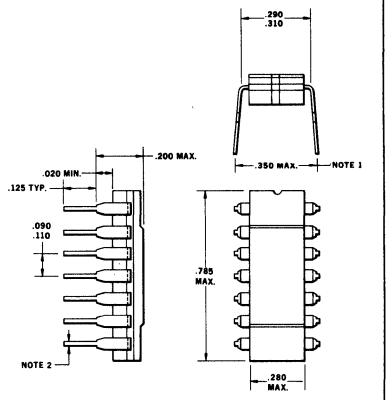
GENERAL DESCRIPTION — The Micrologic® Integrated Circuit Four-Bit Shift Register is a fully integrated, monolithic digital circuit which is manufactured using the patented Fairchild Planar* epitaxial process.

THE 9997 FOUR-BIT SHIFT REGISTER consists of four series connected Flip-Flops and the circuitry required for triggering and resetting the Flip-Flops. Each Flip-Flop has a common reset input, a parallel (asynchronous) input, data input, and a non-inverted, buffered output which receives power from a separate voltage supply (V_{CC}') that is common to all outputs.

The separate voltage supply (V_{CC}') is independent of the V_{CC} terminal, i.e., the circuit will operate with $V_{CC} = 5.5V$ and $V_{CC}' = 3.3V$ or $V_{CC} = 3.3V$ and $V_{CC}' = 5.5V$, etc.

Typical applications include: Serial shifting, parallel shifting (static storage register), serial input-parallel output, parallel input-serial output, and shift counters.

TYPICAL DUAL IN-LINE PACKAGE
(In accordance with JEDEC TO—116)



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

PURCHASING INFORMATION:

To order this device specify U6A999729X.

FEATURES

- **SERIAL OPERATION WITH PARALLEL ENTRY TO ALL BITS**
- **ASYNCHRONOUS GANGED RESET CAPABILITY**
- **WIDE V_{CC} RANGE — COMPATIBLE OPERATION WITH SEVERAL LOGIC FAMILIES**
- **OUTPUTS CAN BE GATED**
- **SINGLE LINE SERIAL INPUT**
- **HANDLES BLOCKS OF FOUR BITS OF DATA COMMON TO MANY PARALLEL/SERIAL AND SERIAL/PARALLEL OPERATIONS**
- **CAN DRIVE 40 CCSL UNIT LOADS**

ELECTRICAL CHARACTERISTICS

Operating Voltage Range	3.3 to 5.5 Volts
Minimum Shifting Rate	D.C. to 5.0 MHz
Typical Shifting Rate	D.C. to 7.0 MHz
Maximum Power Dissipation ($V_{CC}' = V_{CC}$)	380 mW
Maximum Power Dissipation (V_{CC}' = open)	260 mW

NORMAL OPERATION

SERIAL SHIFTING — A high to low voltage transition at the trigger input (T) initiates the following simultaneous state transfers: $D \rightarrow Q_1$, $Q_1 \rightarrow Q_2$, $Q_2 \rightarrow Q_3$, and $Q_3 \rightarrow Q_4$.

RESET AND PARALLEL ENTRY — A high voltage level at the reset input (R) overrides all other inputs and causes all four Flip-Flops to be reset such that the Q_1, Q_2, Q_3, and Q_4 outputs assume a high voltage level and remain high after removal of the reset signal. After removal of the reset signal, a high voltage level at a set input (S_1 through S_4) will cause each Flip-Flop to be set such that its corresponding output (Q_1 through Q_4) will be at a low voltage level. No change of state will occur if a set input is at a low signal level.

Note that since the buffered outputs receive power from a separate voltage supply they can be gated (or enabled) by gating the voltage applied to Pin 13. This feature is useful from a logical viewpoint, as well as a power conservation consideration. The gated emitter-follower circuit shown on the back of this sheet is recommended.

* Planar is a patented Fairchild process.

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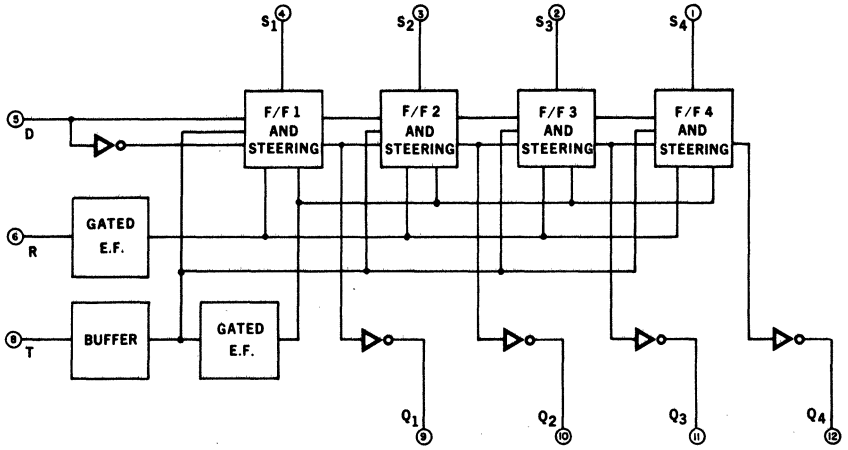
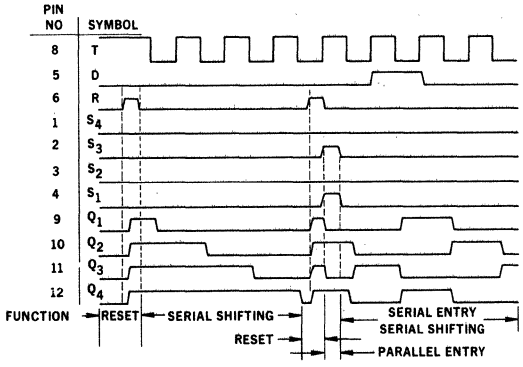
9997 FOUR BIT SHIFT REGISTER

BLOCK DIAGRAM

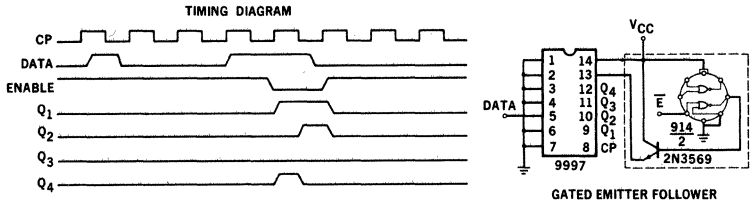


FOUR BIT SHIFT REGISTER (PRODUCT CODE 9997) BLOCK DIAGRAM

TYPICAL TIMING DIAGRAM

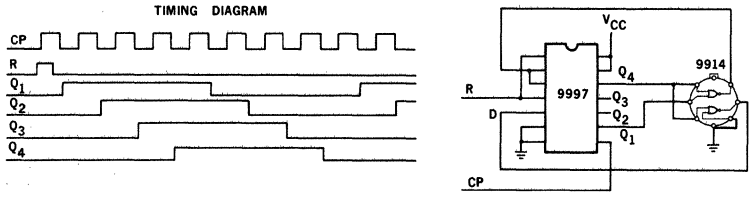


SERIAL SHIFT REGISTER WITH GATED OUTPUTS.



GATED EMITTER FOLLOWER

MODULO 8 SHIFT REGISTER COUNTER
(Shifting Rate Test Circuit)



LOW POWER RTμL

PLANAR* EPITAXIAL LOW POWER RESISTOR—TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

WHAT IS LOW POWER RTμL?

Fairchild Low Power RTμL Integrated Circuits are a set of compatible, integrated logic building blocks. The elements are manufactured using the Fairchild Planar* epitaxial process by which all the necessary transistors and resistors are diffused into a single silicon wafer. The individual RTL gates within the logic blocks are interconnected by metal over oxide.

SPEED AND POWER

Low Power RTμL is characterized by very low propagation delays at low DC power dissipation. Typical propagation delay for the basic RTL circuit is 40 nanoseconds, and its power dissipation is typically 2 mW.

ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature)

Maximum voltage applied to pin 8 (continuous)	8 V
Maximum voltage applied to any input pin	±4.0 volts
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation	250 mW
Maximum Voltage applied to pin 8 (Pulsed, ≤1 second)	12 V

PURCHASING INFORMATION

Purchasing Agent please note:

To order part, the following numbering system should be used to expedite handling. The complete number will be a seven digit number with the designations as follows.

ABCDEFG

A = 9 for all elements.

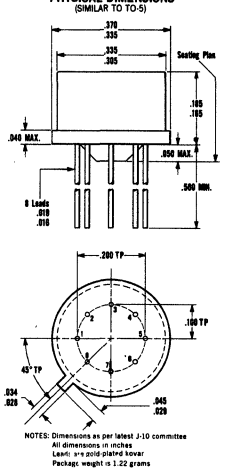
B = 5 for the TO-5 package. 1 for the flat package.

CDE = the four digit number denoting the specific element desired (i.e. the buffer) would be 9909.

F = 2 for Planar epitaxial material.

G = 1 for −55°C to +125°C operation.

PHYSICAL DIMENSIONS
(SIMILAR TO TO-5)



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Lead: ir-s gold-plated kovar
Package weight is 1.22 grams

AMBIENT TEMPERATURE OPERATION

Low Power RTμL Integrated Circuits may be used in accordance with the Loading Chart below through the full military temperature range of −55°C to +125°C. Nominal Supply voltage is 3.00 Volts. The Loading Chart below is valid for V_{CC} = 3.00 Volts ±10%. Improved speed and Noise Immunity will result if V_{CC} is increased above 3.00 Volts to a maximum of 3.66 Volts at +125°C with maximum V_{CC} increasing linearly to 4.5 Volts at −55°C.

ELEMENTS

The 9908 Element (ADDER) performs MOD 2 Addition, the exclusive OR function, and control of 2 data streams (pins 1 and 5) by tying pins 2 and 3 together to control.

The 9909 Element (BUFFER) is a 2 input, high fan-out, inverting gate, with internal timing resistor.

The 9910 Element (DUAL GATE) is a dual, 2 input gate.

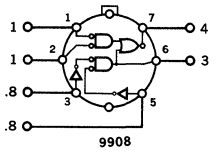
The 9911 Element (GATE) is a 4 input gate with added inverter for the output to generate OR, NOR, AND, and NAND functions.

The 9912 Element (HALF-ADDER) is a two-level AND-OR gate with added output inverter.

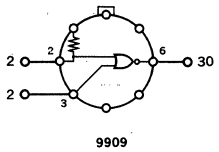
The 9913 Element (TYPE D FLIP-FLOP) is a gated D-Flip-Flop with asynchronous set and reset inputs suitable for shifting and counting. The 9913 was previously known as an R, Register, or Full Shift Register Eelement.

The 9921 Element (EXPANDER) is a dual 2 input gate without node resistors, to be used when increased fan-in is required.

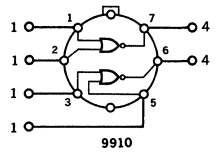
LOW POWER RTμL LOADING CHART valid for system operation from −55°C to +125°C (symbols shown top view)



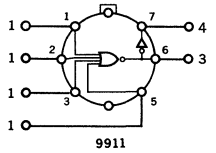
9908



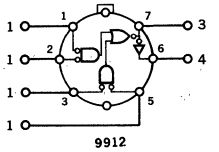
9909



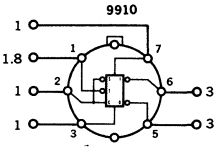
9910



9911



9912



9913

* Planar is a patented Fairchild process.

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GENERAL RULES

The number of elements that may be driven by an output terminal may consist of any combination of elements whose summation of input loading does not exceed the output terminal driving capability.

Unused input pins should be tied to ground.

See expander element (9921) for paralleling.

FIG. 1

TYPICAL POWER DISSIPATION VS. V_{CC}

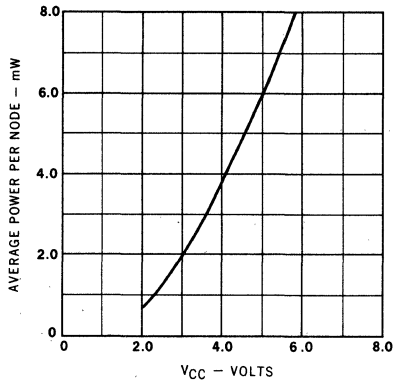


FIG. 2a

TYPICAL SIGNAL LEVEL VS. TEMPERATURE

V_{CC} = 3.0V

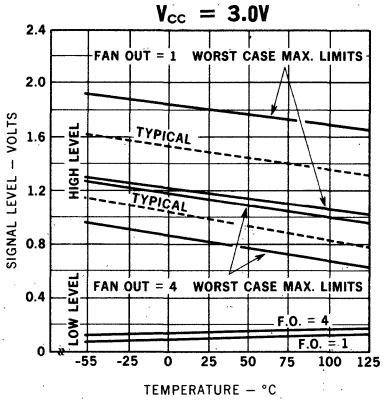


FIG. 2b

TYPICAL SIGNAL LEVEL VS. TEMPERATURE

V_{CC} = 4.0V

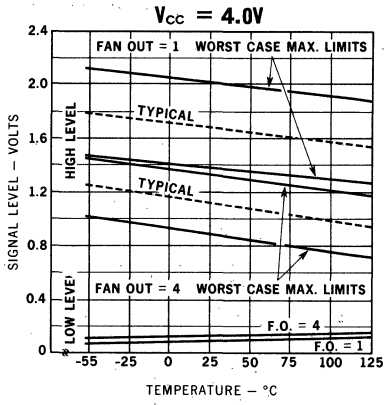


FIG. 3

TYPICAL INPUT CHARACTERISTICS

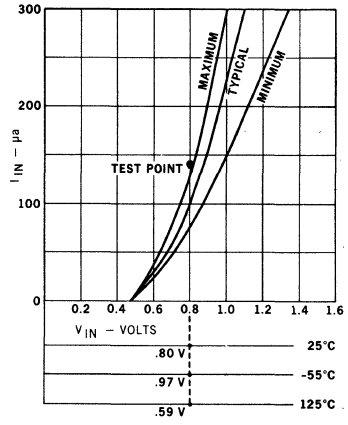
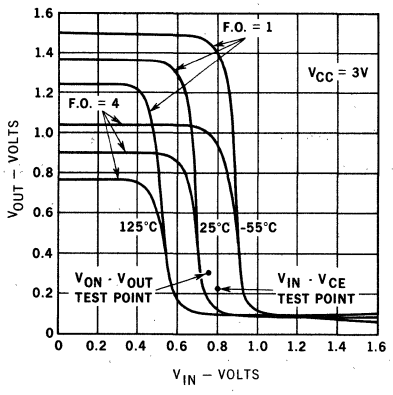


FIG. 4

TRANSFER CHARACTERISTICS

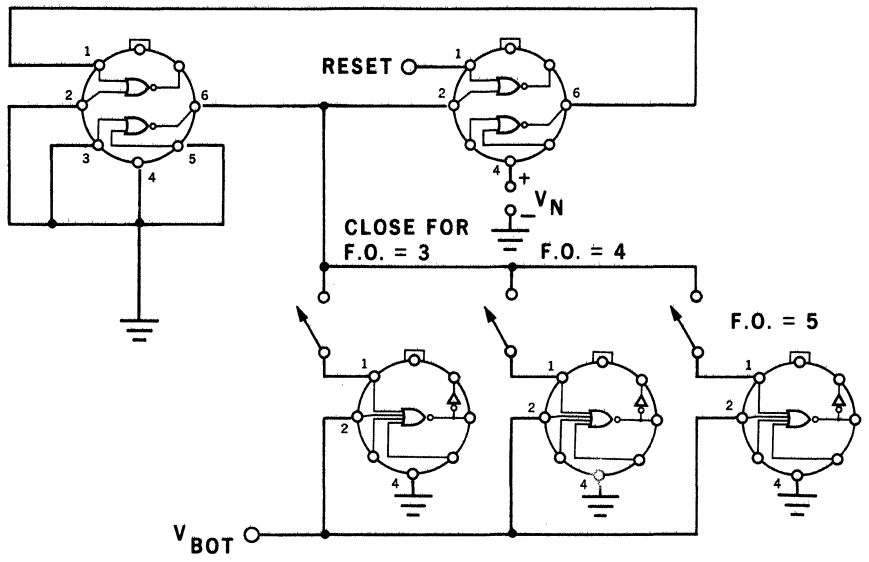


Note: This curve will apply as V_{CC} is increased from 3 V to 5 V with small decrease in I_{IN} for same V_{IN}.

TYPICAL V_{ON} VS. V_{CC}

	–55°C	+25°C	+125°C
V_{CC} = 3 V	.890	.680	.530
V_{CC} = 4 V	.940	.710	.550
V_{CC} = 5 V	.990	.750	.575

FIG. 5 TEST CIRCUIT FOR NOISE THRESHOLD MEASUREMENTS



V_{CC}	V_{BOT}
3 V	1.8 V
4 V	2.0 V
5 V	2.4 V
6 V	2.9 V

Note that elements with specified fan-out = 4 have good immunity to worst case ground noise in a test circuit when used in a fan-out = 5 configuration.

FIG. 6
DC NOISE THRESHOLD VS. V_{CC}

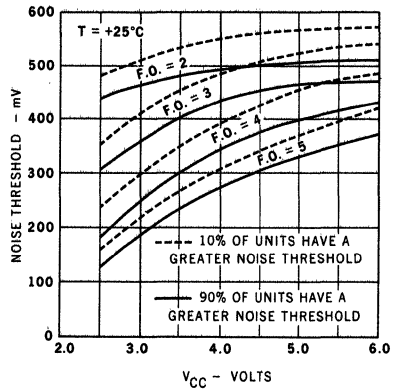


FIG. 7
DC NOISE THRESHOLD VS. V_{CC}

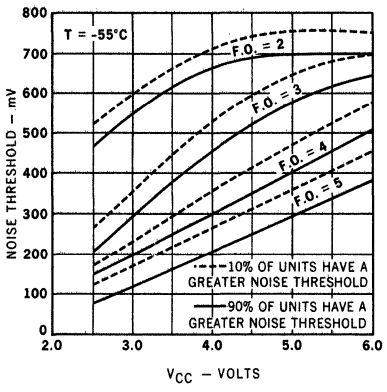


FIG. 8
DC NOISE THRESHOLD VS. V_{CC}

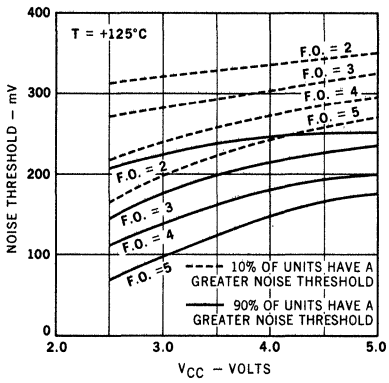


FIG. 9
TYPICAL PULSED NOISE THRESHOLD VERSUS PULSE WIDTH

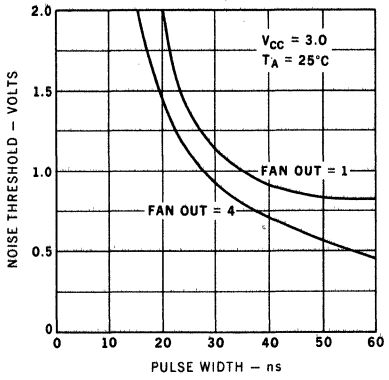


FIG. 10
TYPICAL PULSED NOISE THRESHOLD VERSUS PULSE WIDTH

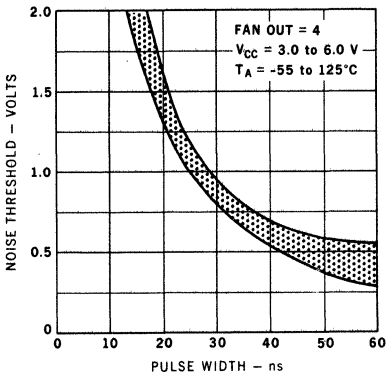
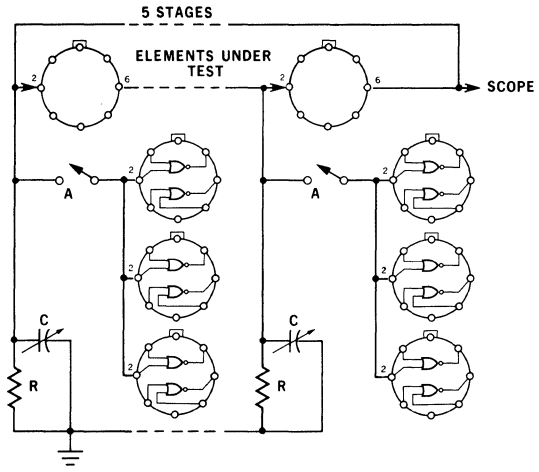


FIG. 11 TEST CIRCUIT AND TABLE FOR TYPICAL t_{pd} MEASUREMENTS



Connect pin 8 to V_{CC}
Connect pin 4 to ground.
Connect all unused input pins to ground

$$\text{AVERAGE } t_{pd} = \frac{1}{f_{osc}} \times \frac{1}{10}$$

ELEMENT	R	INPUT PIN NO.	OUTPUT PIN NO.	OTHER INPUTS	NOTE
9908 ADDER	∞	3	7	PINS 2 & 5 TO 1.8 V	2
9909 BUFFER	220 Ω	3	6	—	1
9910 DUAL GATE	∞	1	7	2, 3, & 5 TO GND	2
9912 HALF ADDER	∞	2	6	PIN 3 TO 1.8 V	2

TEST FOR 9909 ELEMENTS

1. All "A" switches left open in t_{pd} test for 9909 element.
2. For curves shown, fan-out = 1 corresponds to switch "A" open; and for fan-out = 4, switch "A" closed.

AVERAGE PROPAGATION DELAY VERSUS CAPICITANCE

FIG. 12

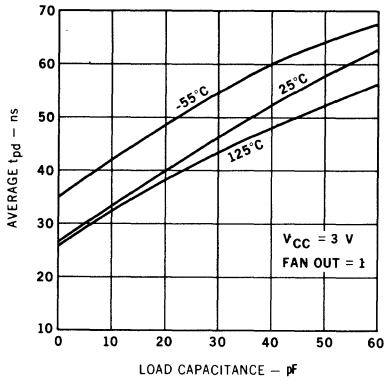


FIG. 13

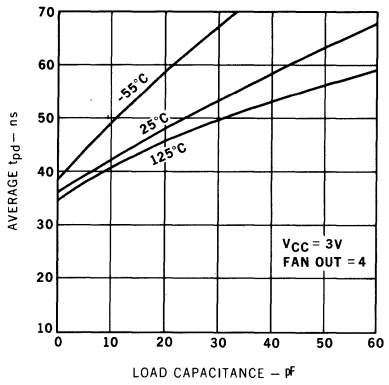


FIG. 14

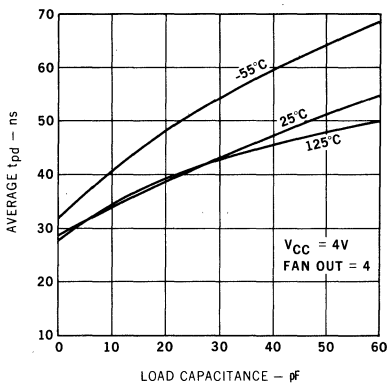


FIG. 15

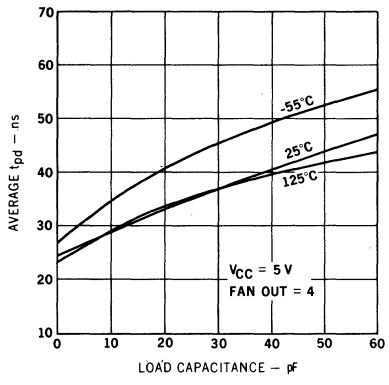


FIG. 16

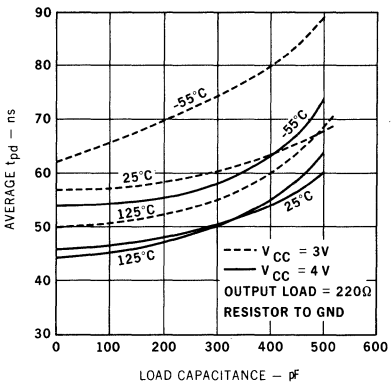
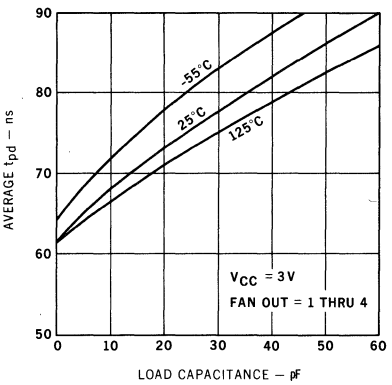


FIG. 17



9908 LOW POWER RTμL ADDER

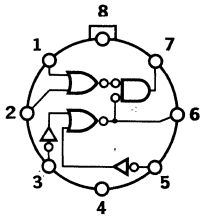
THE LOW POWER RTμL ADDER PERFORMS THE **MOD 2** ADDITION OR EXCLUSIVE **OR** FUNCTION; IT ALSO IS USED TO SELECT ONE OF TWO DATA STREAMS UNDER CONTROL OF A SINGLE GATE SIGNAL.

AVERAGE POWER DISSIPATION (25°C)

10 mW

LOGIC SYMBOL AND FUNCTIONS

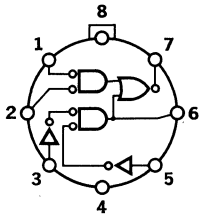
POSITIVE LOGIC



$6 = \overline{(\bar{3}+\bar{5})} = 3 \cdot 5$

$7 = (1+2)\ (\bar{3}+\bar{5})$

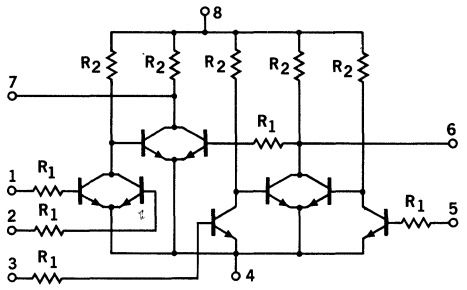
NEGATIVE LOGIC



$6 = \overline{(\bar{3} \cdot \bar{5})} = 3+5$

$7 = 1 \cdot 2 + \bar{3} \cdot \bar{5}$

CIRCUIT DIAGRAM

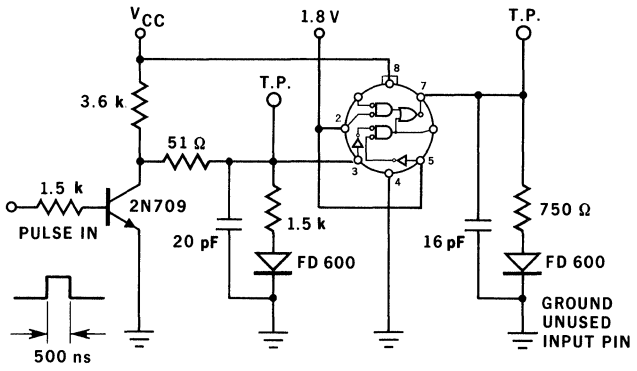


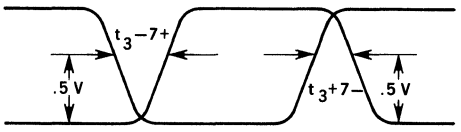
Typical Resistors

$R_1 = 1.5\,k\Omega$

$R_2 = 3.6\,k\Omega$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_3		GND	GND	V_{IN}	GND	GND			V_{CC}		$.81_{IN}$
2	I_5		GND	GND	GND	GND	V_{IN}			V_{CC}		$.81_{IN}$
3	I_1		V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}		I_{IN}
4	I_2		V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}		I_{IN}
5	I_6		GND	GND	V_{ON}	GND	V_{ON}	V_{IN}		V_{CC}	I_{A3}	
6	I_7		V_{ON}	GND	V_{OFF}	GND	V_{OFF}		V_{IN}	V_{CC}	I_{A4}	
7	I_7		GND	V_{ON}	V_{OFF}	GND	V_{OFF}		V_{IN}	V_{CC}	I_{A4}	
8	V_6		GND	GND	V_{BOT}	GND	V_{OFF}			V_{CC}		V_{CE}
9	V_6		GND	GND	V_{OFF}	GND	V_{BOT}			V_{CC}		V_{CE}
10	V_7		V_{OFF}	V_{OFF}	GND	GND	GND			V_{CC}		V_{CE}
11	V_7		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}	V_{IN}		V_{CC}		V_{CE}
12	V_7		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}	V_{ON}		V_{CC}		V_{OUT}
13	I_8		GND	GND	GND	GND	GND			V_{LL}		I_L
14	t_{3-7+}		GND	V_{BOT}	Pulse in	GND	V_{BOT}		Pulse out	V_{CC}		80 ns
15	t_{3+7-}		GND	V_{BOT}	Pulse in	GND	V_{BOT}		Pulse out	V_{CC}		100 ns

9909 LOW POWER RTμL BUFFER

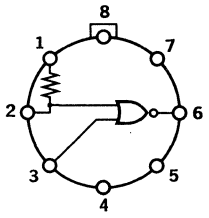
THE LOW POWER RTμL BUFFER IS A LOW IMPEDANCE INVERTING DRIVER CIRCUIT. THE ELEMENT CAN SUPPLY SUBSTANTIALLY MORE OUTPUT CURRENT THAN THE BASIC **RTL** CIRCUIT. A RESISTOR IS INTERNALLY CONNECTED TO THE BUFFER ELEMENT INPUT WHICH MAY BE RETURNED TO THE SUPPLY VOLTAGE IF CAPACITIVE COUPLING IS DESIRED. TYPICAL APPLICATIONS OF THIS TYPE CONNECTION ARE ASTABLE AND MONOSTABLE MULTIVIBRATORS, AND FOR THE DIFFERENTIATION OF PULSES.

AVERAGE POWER DISSIPATION (25°C)
10 mW at 50% Duty Cycle

LOGIC SYMBOL AND FUNCTIONS

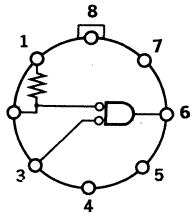
POSITIVE LOGIC

$6 = \overline{2+3}$

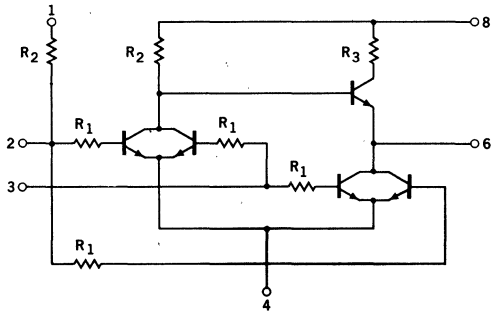


NEGATIVE LOGIC

$6 = \overline{2 \cdot 3}$



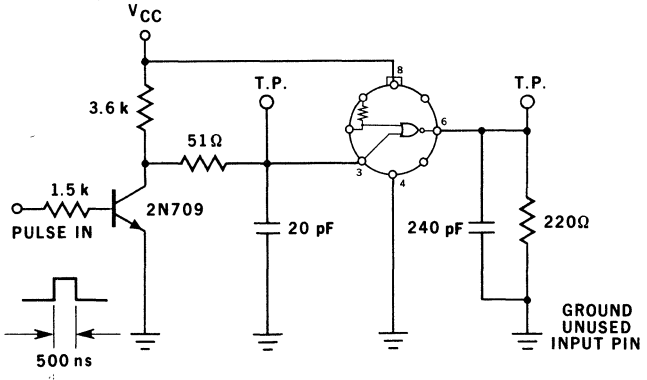
CIRCUIT DIAGRAM

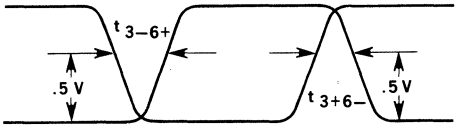


Typical Resistors

$R_2 = 3.6\,k\Omega$
$R_1 = 1.5\,k\Omega$
$R_3 = 100\Omega$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_2			V_{IN}	V_{BOT}	GND				V_{CC}		$2I_{IN}$
2	I_3			V_{BOT}	V_{IN}	GND				V_{CC}		$2I_{IN}$
3	V_6			V_{OFF}	V_{OFF}	GND		V_{IN}		V_{CC}	I_{AB}	
4	V_6			V_{ON}	GND	GND		V_{RH}		V_{CC}		V_{OUT}
5	V_6			GND	V_{ON}	GND		V_{RH}		V_{CC}		V_{OUT}
6	V_6			V_{IN}	GND	GND		V_{RH}		V_{CC}		V_{CE}
7	V_6			GND	V_{IN}	GND		V_{RH}		V_{CC}		V_{CE}
8	I_8			GND	GND	GND				V_{CC}		I_L
9	t_{3+6-}			GND	Pulse in	GND		Pulse out		V_{CC}		90 ns
10	t_{3-6+}			GND	Pulse in	GND		Pulse out		V_{CC}		70 ns

9910 LOW POWER RTμL DUAL GATE

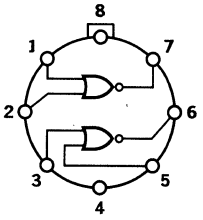
THE LOW POWER RTμL DUAL GATE MAY BE USED AS A PAIR OF NOR GATES, AS AN R-S FLIP-FLOP, AS A PAIR OF INVERTERS, OR AS A DOUBLE INVERTER. IT MAY ALSO BE USED WITH THE LOW POWER RTμL GATE EXPANDER TO INCREASE ITS FAN-IN CAPACITY.

AVERAGE POWER DISSIPATION (25°C)

4 mW

LOGIC SYMBOL AND FUNCTIONS

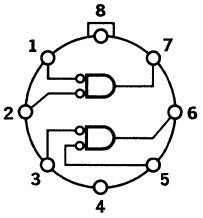
POSITIVE LOGIC



$7 = \overline{1+2}$

$6 = \overline{3+5}$

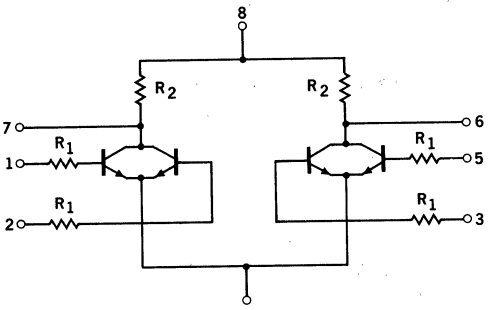
NEGATIVE LOGIC



$7 = \overline{1 \cdot 2}$

$6 = \overline{3 \cdot 5}$

CIRCUIT DIAGRAM

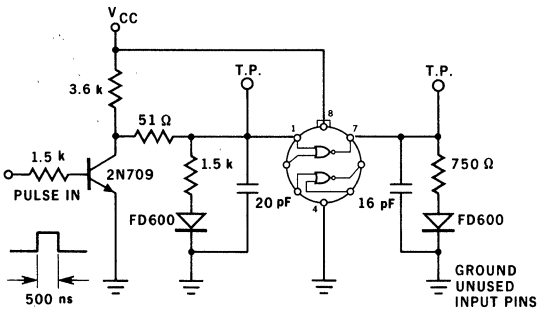


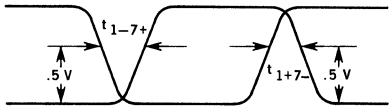
Typical Resistors

$R_1 = 1.5\,k$

$R_2 = 3.6k$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_1		V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}		I_{IN}
3	I_3		GND	GND	V_{IN}	GND	V_{BOT}			V_{CC}		I_{IN}
4	I_5		GND	GND	V_{BOT}	GND	V_{IN}			V_{CC}		I_{IN}
5	I_7		V_{OFF}	V_{OFF}	V_{BOT}	GND	GND		V_{IN}	V_{CC}	I_{A4}	I_{AM}
6	I_6		GND	V_{BOT}	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}	I_{A4}	I_{AM}
7	V_7		V_{ON}	GND	GND	GND	GND			V_{CC}		V_{OUT}
8	V_7		GND	V_{ON}	GND	GND	GND			V_{CC}		V_{OUT}
9	V_6		GND	GND	V_{ON}	GND	GND			V_{CC}		V_{OUT}
10	V_6		GND	GND	GND	GND	V_{ON}			V_{CC}		V_{OUT}
11	V_6		GND	GND	V_{IN}	GND	GND			V_{CC}		V_{CE}
12	V_6		GND	GND	GND	GND	V_{IN}			V_{CC}		V_{CE}
13	V_7		V_{IN}	GND	GND	GND	GND			V_{CC}		V_{CE}
14	V_7		GND	V_{IN}	GND	GND	GND			V_{CC}		V_{CE}
15	I_8		GND	GND	GND	GND	GND			V_{CC}		I_L
16	t_{1-7+}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		40 nsec
17	t_{1+7-}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		50 nsec

9911 LOW POWER RTμL GATE

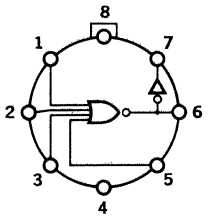
THE LOW POWER RTμL GATE MAY BE USED AS AN **OR** GATE BY APPLYING TRUE INPUTS; THE PIN 7 OUTPUT IS THEN THE TRUE **OR** FUNCTION OF THE INPUTS, AND THE PIN 6 OUTPUT IS THE INVERSE, OR **NOR.**

AVERAGE POWER DISSIPATION (25°C)

4 mW

LOGIC SYMBOL AND FUNCTIONS

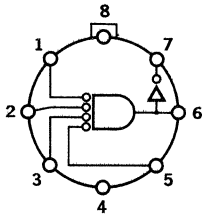
POSITIVE LOGIC



$7 = 1+2+3+5$

$6 = \overline{1+2+3+5}$

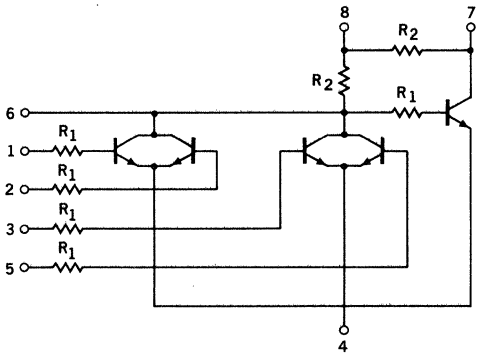
NEGATIVE LOGIC



$7 = 1 \cdot 2 \cdot 3 \cdot 5$

$6 = \overline{1 \cdot 2 \cdot 3 \cdot 5}$

CIRCUIT DIAGRAM

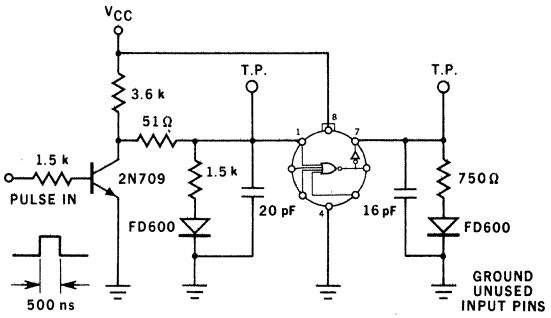


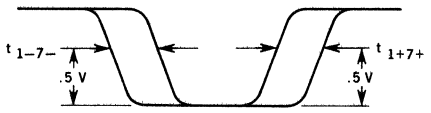
Typical Resistors

$R_1 = 1.5\,k\Omega$

$R_2 = 3.6\,k\Omega$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_1		V_{IN}	V_{BOT}	V_{BOT}	GND	V_{BOT}			V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	V_{BOT}	GND	V_{BOT}			V_{CC}		I_{IN}
3	I_3		V_{BOT}	V_{BOT}	V_{IN}	GND	V_{BOT}			V_{CC}		I_{IN}
4	I_5		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{IN}			V_{CC}		I_{IN}
5	I_6		V_{OFF}	V_{OFF}	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}	I_{A3}	
6	I_7		GND	GND	GND	GND	GND	V_{OFF}	V_{IN}	V_{CC}	I_{A4}	I_{AM}
7	V_6		V_{ON}	GND	GND	GND	GND			V_{CC}		V_{OUT}
8	V_6		GND	V_{ON}	GND	GND	GND			V_{CC}		V_{OUT}
9	V_6		GND	GND	V_{ON}	GND	GND			V_{CC}		V_{OUT}
10	V_6		GND	GND	GND	GND	V_{ON}			V_{CC}		V_{OUT}
11	V_6		V_{IN}	GND	GND	GND	GND			V_{CC}		V_{CE}
12	V_6		GND	V_{IN}	GND	GND	GND			V_{CC}		V_{CE}
13	V_6		GND	GND	V_{IN}	GND	GND			V_{CC}		V_{CE}
14	V_6		GND	GND	GND	GND	V_{IN}			V_{CC}		V_{CE}
15	V_7		GND	GND	GND	GND	GND	V_{ON}		V_{CC}		V_{OUT}
16	V_7		GND	GND	GND	GND	GND	V_{IN}		V_{CC}		V_{CE}
17	I_8		GND	GND	GND	GND	GND			V_{LL}		I_L
18	t_{1-7-}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		70 ns
19	t_{1+7+}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		90 ns

9912 LOW POWER RTμL HALF ADDER

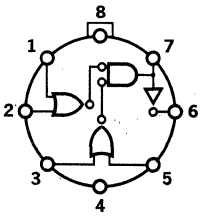
THE LOW POWER RTμL HALF-ADDER IS A MULTI-PURPOSE COMBINATION OF THREE BASIC **RTL** CIRCUITS. THE CONFIGURATION IS WELL SUITED AS A COMPLETE HALF-ADDER, AN EXCLUSIVE **OR** GATE, OR ANY OTHER SIMILAR LOGIC CONSTRUCTION.

AVERAGE POWER DISSIPATION (25°C)

8 mW

LOGIC SYMBOL AND FUNCTIONS

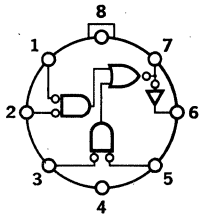
POSITIVE LOGIC



$7 = (1+2)\,(3+5)$

$6 = \bar{1}\cdot\bar{2}+\bar{3}\cdot\bar{5}$

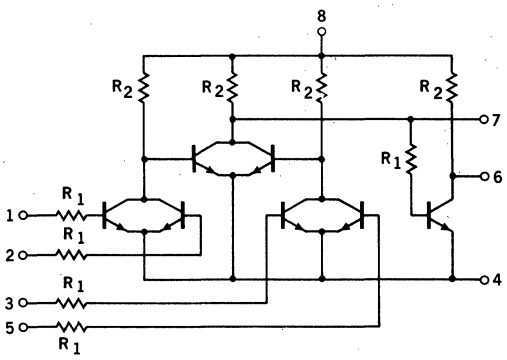
NEGATIVE LOGIC



$7 = 1\cdot2+3\cdot5$

$6 = (\bar{1}+\bar{2})\,(\bar{3}+\bar{5})$

CIRCUIT DIAGRAM

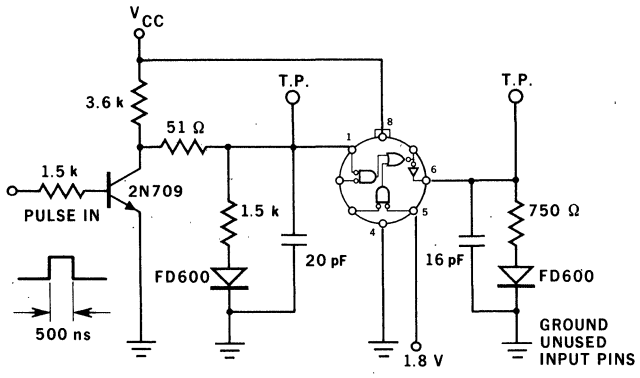


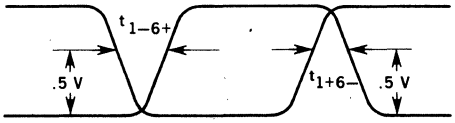
Typical Resistors

$R_1 = 1.5\,k\Omega$

$R_2 = 3.6\,k\Omega$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Notes	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Min.	MAX.
1	I_1		V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}		I_{IN}
3	I_3		GND	GND	V_{IN}	GND	V_{BOT}			V_{CC}		I_{IN}
4	I_5		GND	GND	V_{BOT}	GND	V_{IN}			V_{CC}		I_{IN}
5	I_7		V_{ON}	GND	V_{ON}	GND	GND		V_{IN}	V_{CC}	I_{A3}	
6	I_7		GND	V_{ON}	GND	GND	V_{ON}		V_{IN}	V_{CC}	I_{A3}	
7	I_6		GND	GND	GND	GND	GND	V_{IN}		V_{CC}	I_{A4}	
8	V_6		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}		V_{ON}	V_{CC}		V_{OUT}
9	V_6		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}		V_{IN}	V_{CC}		V_{CE}
10	V_7		V_{OFF}	V_{OFF}	V_{BOT}	GND	V_{BOT}			V_{CC}		V_{CE}
11	V_7		V_{BOT}	V_{BOT}	V_{OFF}	GND	V_{OFF}			V_{CC}		V_{CE}
12	I_8		GND	GND	GND	GND	GND			V_{LL}		I_L
13	T_{1+6-}		Pulse in	GND	GND	GND	V_{BOT}	Pulse out		V_{CC}		100 ns
14	T_{1-6+}		Pulse in	GND	GND	GND	V_{BOT}	Pulse out		V_{CC}		80 ns

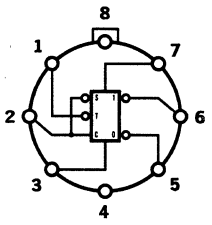
9913 LOW POWER RTμL TYPE D FLIP-FLOP

THE LOW POWER RTμL TYPE D FLIP-FLOP IS A COMPLETE, GENERAL PURPOSE STORAGE ELEMENT. THE STATE OF INPUT 2 IS STORED WHEN INPUT 1 CHANGES FROM HIGH TO LOW. A SUBSEQUENT CHANGE OF INPUT 2 WHILE INPUT 1 IS LOW HAS NO EFFECT. THE 9913 FLIP-FLOP HAS APPLICATION IN SHIFT REGISTERS, COUNTERS, AND CONTROL CIRCUITRY.

AVERAGE POWER DISSIPATION (25°C)

12 mW

LOGIC SYMBOL AND FUNCTIONS



DIRECT INPUTS[1]

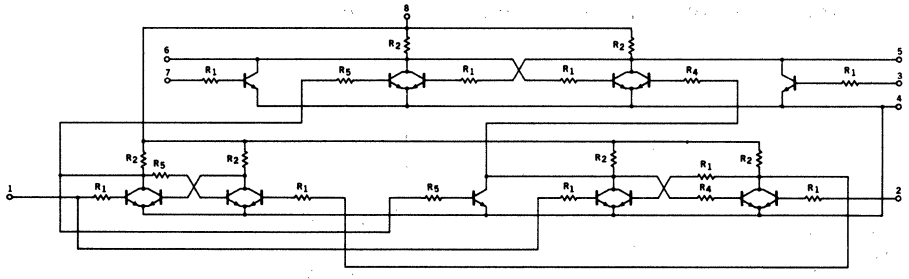
3	7	6	5
L	L	NC	NC[2]
L	H	L	H
H	L	H	L
H	H	L	L

GATED INPUT[3]

t = n	t = n + 1	
2	6	5
H	H	L
L	L	H

1. Pin 1 must be high
2. NC = no change
3. Pins 3 and 7 must be low

CIRCUIT DIAGRAM

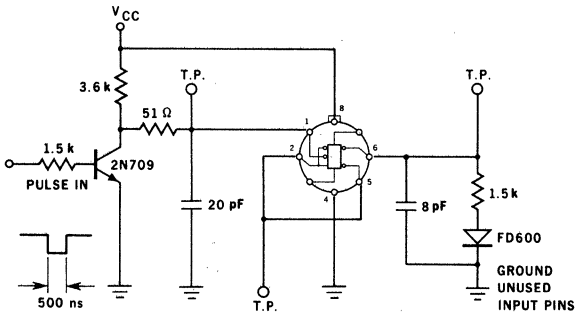


Typical Resistors $R_1 = 1.5k\Omega$ $R_4 = 180\Omega$
$R_2 = 3.6k\Omega$ $R_5 = 480\Omega$

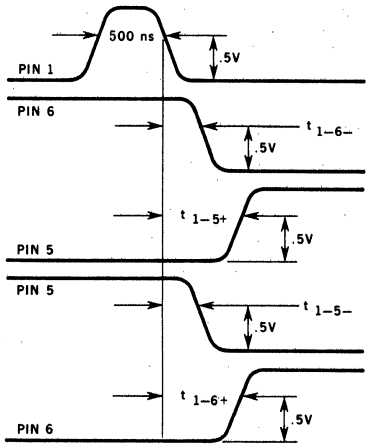
Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	V_5		V_{BOT}	GND	V_{ON}	GND			V_{BOT}	V_{CC}		V_{OUT}
2	V_6		V_{BOT}	GND	V_{BOT}	GND			V_{ON}	V_{CC}		V_{OUT}
3	V_5		V_{BOT}	GND	GND	GND		V_{ON}	GND	V_{CC}		V_{OUT}
4	V_6		V_{BOT}	GND	GND	GND	V_{ON}		GND	V_{CC}		V_{OUT}
5	V_5		V_{BOT}	GND	V_{IN}	GND			V_{BOT}	V_{CC}		V_{CE}
6	V_6		V_{BOT}	GND	V_{BOT}	GND			V_{IN}	V_{CC}		V_{CE}
7	V_5		V_{BOT}	GND	GND	GND		V_{IN}	GND	V_{CC}		V_{CE}
8	V_6		V_{BOT}	GND	GND	GND	V_{IN}		GND	V_{CC}		V_{CE}
9	I_1		V_{IN}	GND	GND	GND			GND	V_{CC}		$1.8\ I_{IN}$
10	I_1		V_{IN}	V_{BOT}	GND	GND			GND	V_{CC}		$1.8\ I_{IN}$
11	I_5		V_{ON}	V_{BOT}	V_{OFF}	GND	V_{IN}		V_{BOT}	V_{CC}	I_{A3}	
12	I_6		V_{ON}	GND	V_{BOT}	GND		V_{IN}	V_{OFF}	V_{CC}	I_{A3}	
13	I_5	1	V_{OFF}	GND	V_{OFF}	GND	V_{IN}		V_{BOT}	V_{CC}	I_{A3}	
14	I_6	1	V_{OFF}	V_{ON}	V_{BOT}	GND		V_{IN}	V_{OFF}	V_{CC}	I_{A3}	
15	I_2	1	V_{OFF}	V_{IN}	GND	GND			GND	V_{CC}		I_{IN}
16	I_3	1	V_{OFF}	V_{BOT}	V_{IN}	GND			GND	V_{CC}		I_{IN}
17	I_7	1	V_{OFF}	GND	GND	GND			V_{IN}	V_{CC}		I_{IN}
18	V_5	1	V_{OFF}	V_{ON}	GND	GND			V_{BOT}	V_{CC}		V_{CE}
19	V_6	1	V_{OFF}	V_{OFF}	V_{BOT}	GND			GND	V_{CC}		V_{CE}
20	I_8		GND	GND	GND	GND			GND	V_{LL}		I_L
21	t_{1-6-}		Pulse In	Tie to Pin 5	GND	GND		Pulse Out	GND	V_{CC}		80 ns
22	t_{1-6+}		Pulse In	Tie to Pin 5	GND	GND		Pulse Out	GND	V_{CC}		120 ns
23	t_{1-5-}		Pulse In	Tie to Pin 5	GND	GND	Pulse Out		GND	V_{CC}		80 ns
24	t_{1-5+}		Pulse In	Tie to Pin 5	GND	GND	Pulse Out		GND	V_{CC}		120 ns
25	t_{2+1-}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	60 ns	
26	t_{1-2-}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	30 ns	
27	t_{2-1-}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	60 ns	
28	t_{1-2+}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	30 ns	

Note 1: Voltage applied to Pin 1 changes from V_{RL} to specified value prior to making measurements.

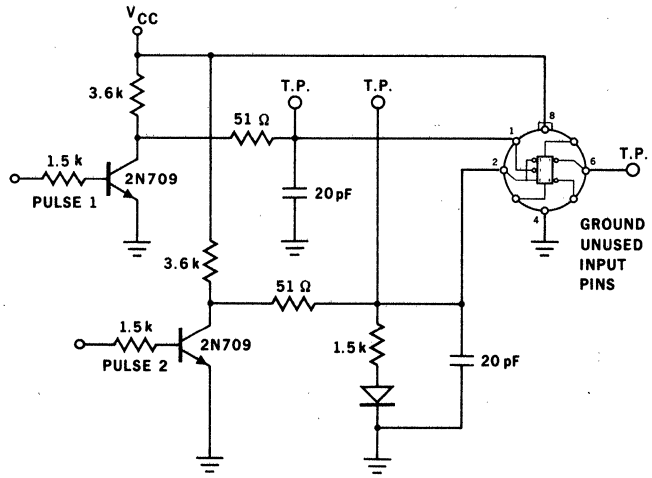
CIRCUIT FOR MEASURING T_{I-6+}, T_{I-6-}, T_{I-5+}, T_{I-5-}



PROPAGATION DELAY

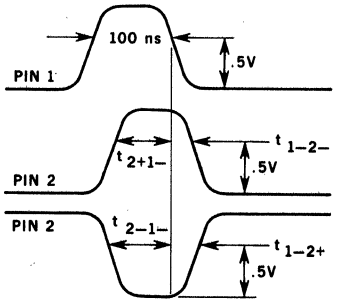


CIRCUIT FOR MEASURING MINIMUM INPUT PULSE WIDTH

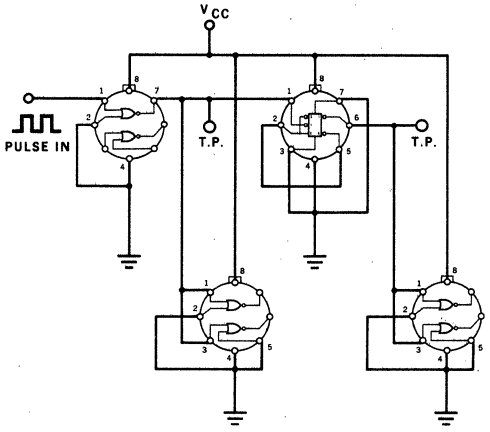


VARIABLE DELAY BETWEEN PULSE 1 AND PULSE 2

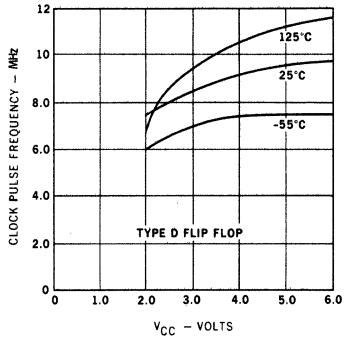
MINIMUM PULSE WIDTH

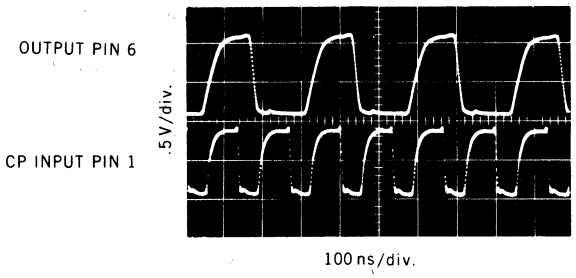


CONNECTED AS BINARY COUNTER



TYPICAL OPERATING CLOCK PULSE FREQUENCY VERSUS V_{CC}





9921 LOW POWER RTμL GATE EXPANDER

THE LOW POWER RTμL GATE EXPANDER IS A DOUBLE GATE WITHOUT THE NODE RESISTORS. ITS OUTPUT TERMINALS MAY BE CONNECTED IN PARALLEL TO THOSE OF A DUAL GATE OR A GATE TO INCREASE THE FAN-IN CAPABILITY OF THE CIRCUITS.

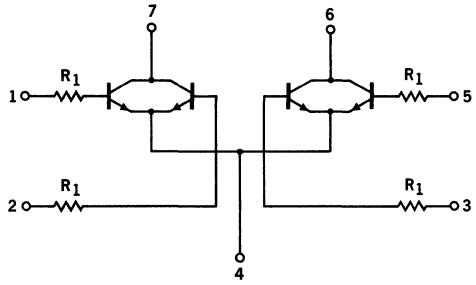
WHEN A DUAL GATE OR A GATE IS USED WITH THE EXPANDER, THE FOLLOWING RULES APPLY.

1) Pin 8 of the Expander must be connected to V_{CC}
2) The input load factor of the expanded gate is 1.33
3) The output drive factor of the expanded gate is decreased by .5 load for every node added.

AVERAGE POWER DISSIPATION (25°C)

No Power Flowing

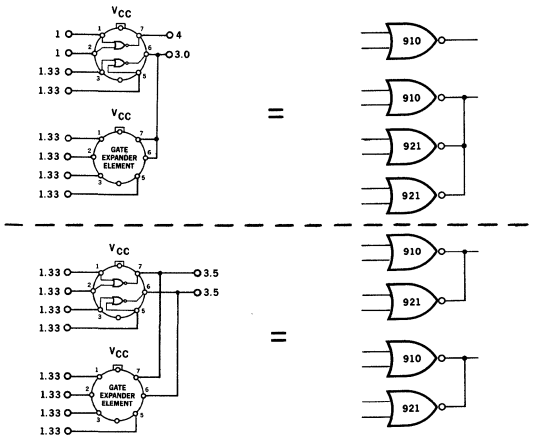
CIRCUIT DIAGRAM



Typical Resistor

$R_1 = 1.5k\Omega$

DIAGRAM FOR USE OF GATE EXPANDER



Example of loading rules and logic symbols

Test No.	Test	Notes	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_1		V_{IN}	V_{BOT}	GND	GND	GND		V_{RH}	V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	GND	GND	GND		V_{RH}	V_{CC}		I_{IN}
3	I_3		GND	GND	V_{IN}	GND	V_{BOT}	V_{RH}		V_{CC}		I_{IN}
4	I_5		GND	GND	V_{BOT}	GND	V_{IN}	V_{RH}		V_{CC}		I_{IN}
5	V_7		V_{ON}	GND	GND	GND	GND		V_{RL}	V_{CC}		V_{OUT}
6	V_7		GND	V_{ON}	GND	GND	GND		V_{RL}	V_{CC}		V_{OUT}
7	V_6		GND	GND	V_{ON}	GND	GND	V_{RL}		V_{CC}		V_{OUT}
8	V_6		GND	GND	GND	GND	V_{ON}	V_{RL}		V_{CC}		V_{OUT}
9	V_6		GND	GND	V_{IN}	GND	GND	V_{RL}		V_{CC}		V_{CE}
10	V_6		GND	GND	GND	GND	V_{IN}	V_{RL}		V_{CC}		V_{CE}
11	V_7		V_{IN}	GND	GND	GND	GND		V_{RL}	V_{CC}		V_{CE}
12	V_7		GND	V_{IN}	GND	GND	GND		V_{RL}	V_{CC}		V_{CE}
13	I_7		V_{OFF}	V_{OFF}	GND	GND	GND		V_{IN}	V_{CC}		I_{CEX}
14	I_6		GND	GND	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}		I_{CEX}
15	$I_{6,7,8}$		GND	GND	GND	GND	GND	V_{CC}	V_{CC}	V_{CC}		I_L

SPECIAL CIRCUITS COMING SOON

Type	Function
Interface Circuits	
9626	Dual CCSL Telephone Line Driver
9627	Dual Telephone to CCSL Line Receiver
9826	Dual CTL Telephone Line Driver
9827	Dual CTL Telephone Line Receiver
RRTTL	
9702	Quad 2-Input NAND Gate
9704	Dual 4-Input NAND Gate
9705	Dual, Dual 2-Input AOI
9708	Quad 2-Input AOI
9711	Flip-Flop — Single D
9774	Flip-Flop — Dual D
9709	Buffer
RRDTL	
9732	Active Pullup Buffer
9744	Uncommitted Output Buffer
9745	R-S Flip-Flop (6K Pullup)
9748	R-S Flip-Flop (2K Pullup)
9762	Triple 3-Input Gate
CTμL II	
9806	Hex Restorer AND Gate
9816	Hex Inverter NOR Gate
9842	Quad 2-Input AND Gate
9852	Dual 2-Input NOR Gate
9853	2-2-3 Input AND Gate
9854	Dual 4-Input AND Gate
9855	Single 8-Input, 2-Output AND Gate
9856	Dual 2-Input AND Buffer Gate
9864	3-1-3 Input AND Gate
9865	Quad Single Input AND Gate
9866	Dual 2-Input AND Gate with 2 Wide, 2-Input AND-OR Gate
9871	Dual 2 Wide, 2-Input AND-OR Gate
9872	As 9866 w/o 2K Load and Pulldown Resistors
9828	J-K, D Flip-Flop
CTμL II Line Interface Circuits	
9819/20	100Ω Line Receivers
9821	100Ω Line Driver
9826	EIA Telephone Line Driver
9827	EIA Telephone Line Receiver
CTμL MSI	
9822	Dual Full Adder/Subtractor
9824	Four-Bit Comparator
9834	Quad Latch
9838	One-of-Eight Decoder
9881	Eight-Input Multiplexer

INTERFACE CIRCUITS

9626 — DUAL CCSL TELEPHONE LINE DRIVER

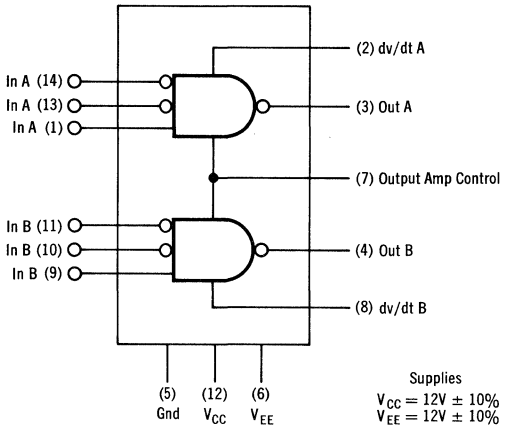
GENERAL

The 9626 is a dual device designed to translate incoming CCSL levels onto either military (MIL-STD 188B) or commercial (RS-232B) equipment. The outputs are single-ended, incorporate short circuit protection, and will have the same output impedance in either the high or low output state. Inputs are CCSL compatible. Rise and fall times are symmetrical and can be controlled by use of an external feedback capacitor connected between dV/dt and output pins. Power dissipation is constant for both frequency and rise and fall time control variations. The product will be released in the 16 pin ceramic dual in-line package.

TARGET SPECIFICATIONS

Supply voltages	$V_{CC} = 12V \pm 10\%$, $V_{EE} = -12V \pm 10\%$
V_{OUT}	$V_{OH} = 6V$, $V_{OL} = -6V$
V_{IN}	$V_{IL} = 1V$, $V_{IH} = 2V$
I_R	$2\mu A$ at $V_{IN} = 4V$
I_F	$50\mu A$ typical (0.5mA maximum) at $V_{in} = 0V$
R_{OUT}	25 ohms typical
I_{SC}	80mA nominal (100mA maximum)
Power dissipation	160mW/gate
Propagation delay	100ns typical (200ns maximum)

LOGIC DIAGRAM AND PIN ASSIGNMENTS



9627 — DUAL TELEPHONE TO CCSL LINE RECEIVER

GENERAL

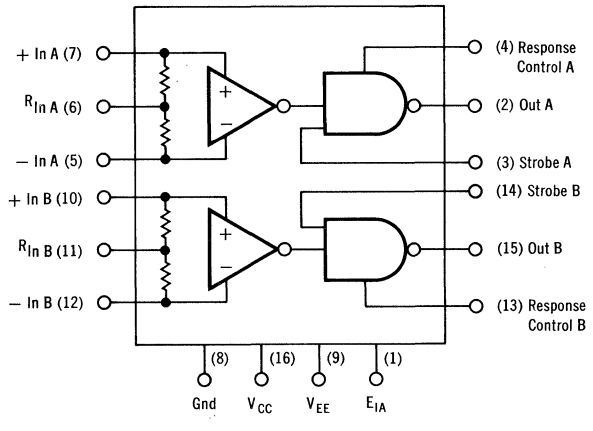
The 9627 is a dual device to receive either military (MIL-STD 188B) or commercial (RS-232B) line signals and translate them to CCSL output levels.

The input features a differential amplifier with hysteresis in order to improve noise immunity and allow single-ended transmission reception. Outputs are CCSL compatible. Provision has been made to independently strobe each receiver and also to control receiver response time by use of an external capacitor tied to ground. The product is planned for release in the 16 pin ceramic dual in-line package.

TARGET SPECIFICATIONS

Supply voltages	$V_{CC} = 12V \pm 10\%$, $V_{EE} = -12V \pm 10\%$
V_{IN} Hysteresis	EIA 6 $\pm$3V (EIA Pin to V_{EE})
	MIL-STD 1.0 $\pm$ 0.5V (EIA Pin OPEN)
R_{IN}	EIA 3K to 7K (R_{IN} to GND)
	MIL-STD $>$ 6K (10.7K nominal with R_{IN} OPEN)
Common Mode Noise Rejection	$\pm$ 25V (referenced to ground)
V_{OUT}	$V_{OL} < 0.4V$ at $I_{OL} = 5mA$
	$V_{OH} > 2.4V$ at $I_{OL} = -0.5mA$
Power Dissipation	160mW/receiver
Propagation Delay	80ns typical (200ns maximum)

LOGIC DIAGRAM AND PIN ASSIGNMENTS



SPECIAL CIRCUITS COMING SOON

CTL 9826 — TELEPHONE LINE DRIVER

The 9826 is a dual device designed to interface CTL levels at the input with equipment meeting military (MIL-STD-188B), or commercial — EIA (RS-232B) telephone line specifications.

Both inverting, and noninverting CTL compatible inputs are provided. Power dissipation remains constant at typically 160mW, for all frequency and rise and fall time variations.

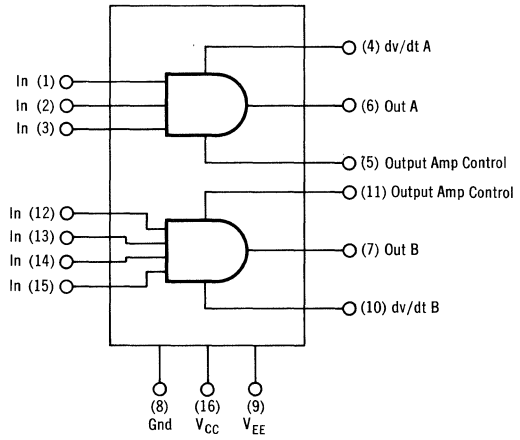
Outputs are single ended, have the same impedance in either high or low output state and incorporate short circuit protection. Rise and fall times are symmetrical and can be controlled by connecting an external feedback capacitor between dV/dt and the output pins.

The 9826 will be available in the 14 pin ceramic Dual In-line Package.

SPECIFICATIONS

V_{IN}	$V_{IL} = 0.8V$, $V_{IH} = 1.25V$
V_{OUT}	$V_{OH} = 6V$, $V_{OL} = -6V$
I_F	2mA at $V_{IN} = 2$ volts
R_{OUT}	25 ohms (typical)
Propagation Delay	100 ns (typ) 200 ns (max)
I_{CC}	80mA (typ) 100mA (max)

LOGIC DIAGRAM



CTL 9827 — TELEPHONE LINE RECEIVER

The 9827 is a dual device designed to interface incoming signals meeting military (MIL-STD-188B) and commercial — EIA (RS-232B) telephone line specifications, with standard CTL logic levels.

The input features a differential amplifier with hysteresis, to improve noise immunity and allow single ended transmission reception. A tapped resistive network is employed to adapt the input to either EIA or MIL requirements.

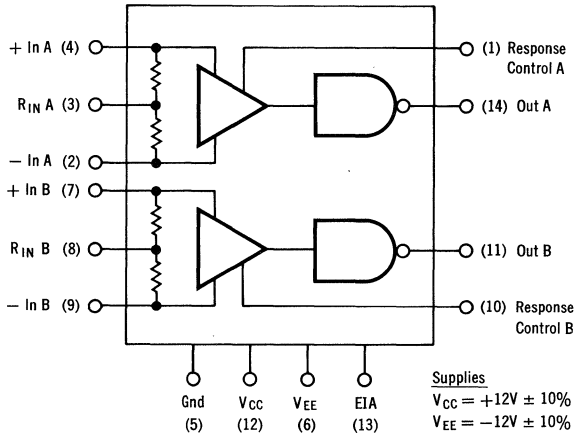
The outputs are CTL compatible. Receiver response time is adjusted by choice of external capacitor.

The 9827 is supplied in the 14 pin ceramic Dual In-line Package.

SPECIFICATIONS

V_{IN} Hysteresis	EIA: 6V (± 3V) (Pin 13 to VEE)
	MIL-STD: 1.0V (± 0.5V)
R_{IN}	EIA: 3K to 7K (R_{IN} to GND)
	MIL-STD: > 6K (10.7K typ)
V_{OUT}	$V_{OL} = 0.7V$ to $-0.3V$
	$V_{OH} > 2.0V$ at 20 mA
Common Mode Noise Rejection	± 25V (referred to ground)
Power Dissipation	160mW/receiver
Propagation Delay	120ns typ (200ns max)

LOGIC DIAGRAM



RRTTL

Fairchild is developing a Radiation Resistant T^2L family which will be manufactured using production proven dielectric isolation and thin film resistor technologies. The family has been specifically designed for low propagation delay times and has been designed for operation and survivability in high radiation environments. Performance to particular categories is available from the factory on a need to know basis. The product line will be available in our 14 lead ¼" x ¼" CERPAK.

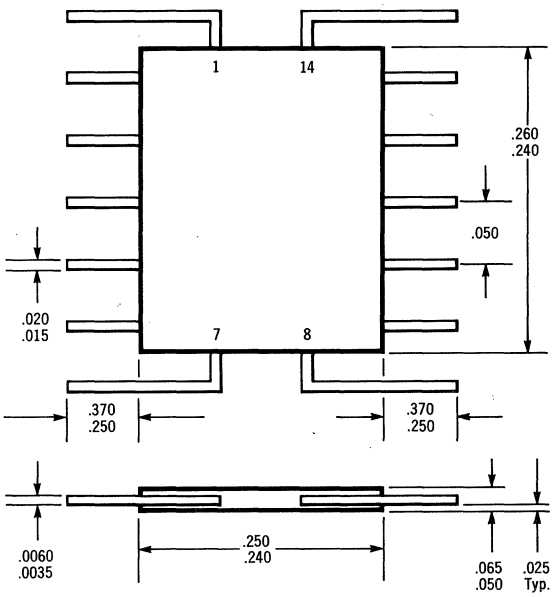
R^2T^2L DESIGN OBJECTIVES

Single power supply: 5.0 volts ± 10%
Temperature range: 0°C to 125°C
Guaranteed fanout of 10 TTL loads over full temperature and supply voltage range
Guaranteed minimum of 0.4 volts noise immunity over temperature. Typical high level noise immunity of 1.3 volts and low level noise immunity of 0.8 volts
Typical power dissipation of 22mW per gate at 50% duty cycle
Typical propagation delays of 6ns for 50pf load

FAMILY ELEMENTS

9702	Quad 2-input NAND Gate
9704	Dual 4-input NAND Gate
9705	Dual, Dual 2-input AND/OR Invert
9708	Single, Quad 2-input AND/OR Invert
9711	Flip-Flop — Single D
9774	Flip-Flop — Dual D

CERPAK DIMENSIONS



SPECIAL CIRCUITS COMING SOON

RRDTL

GENERAL DESCRIPTION

The Fairchild Radiation Resistant series of Diode Transistor Micrologic is a member of the Compatible Current Sinking Logic (CCSL) family designed for use in system where good noise immunity, medium speed, medium power, and good fanout are required. $R^2DT\mu L$ is available in CERPAK package over 0°C to 125°C temperature range.

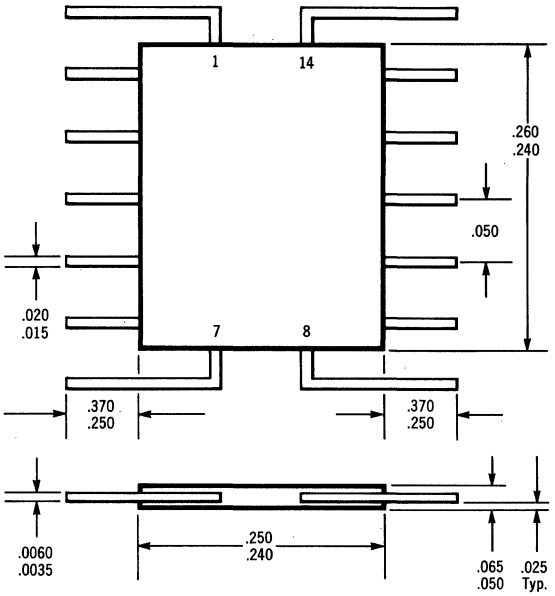
Noise immunity is typically 1 volt. Worst case noise immunity over the military temperature range is 400mV. Power dissipation is typically 8.5mW per gate function at a 50% duty cycle. The average propagation delay is 30ns per gate function. A single 5 volt ± 10% supply can be used. The announced functions are identical in both pinouts and logic to their existing function isolated counterparts.

Fairchild R^2DTL devices incorporate dielectric isolation and thin film resistor manufacturing technologies. All family elements have been designed for operation and survivability in high radiation environments. Performance to particular categories is available from the factory on a need to know basis.

FAMILY ELEMENTS

9732	Active Pull-up Buffer
9744	Uncommitted Output Buffer
9745	R-S Flip Flop (6K pull-up)
9748	R-S Flip Flop (2K pull-up)
9762	Triple Three Input Gate

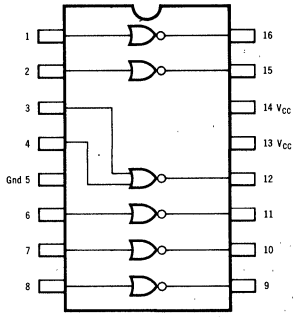
CERPAK DIMENSIONS



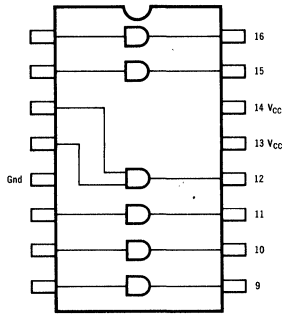
CTμL II

CTμL II is a new high speed version of the CTμL 9952 series circuits. The first elements to be announced will be pin-for-pin replacements for the existing family. The gates will offer tpd 3 nsec (max) and the buffer and inverter 8 nsec (max). Complete circuit listing is:

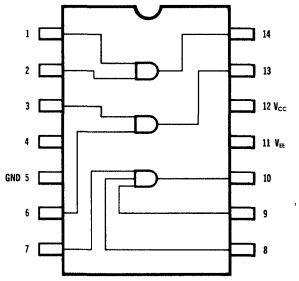
GATES, INVERTERS, AND BUFFERS (RESTORERS)



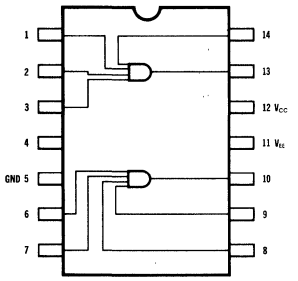
9806
Hex Restorer AND Gate



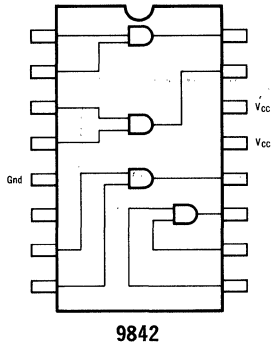
9816
Hex Inverter NOR Gate



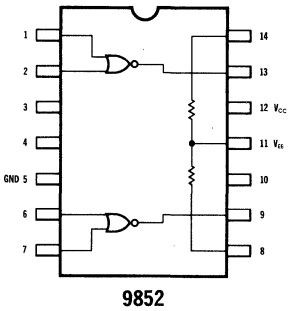
9853
2-2-3 Input AND Gate



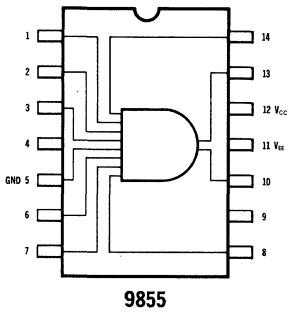
' 9854
Dual 4-Input AND Gate



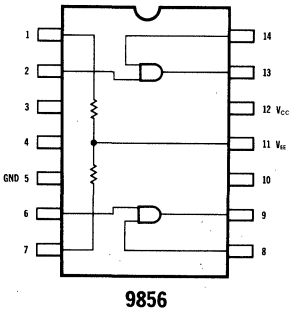
9842
Quad 2-Input AND Gate



9852
Dual 2-Input NOR Gate

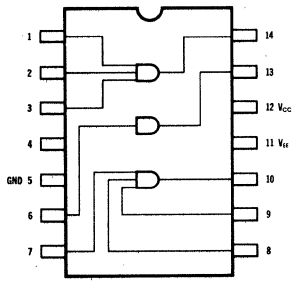


9855
Single 8-Input, 2-Output AND Gate

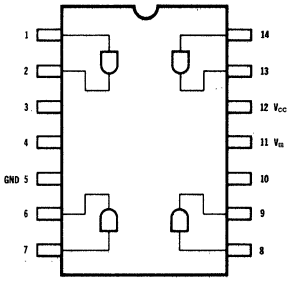


9856
Dual 2-Input AND Buffer Gate

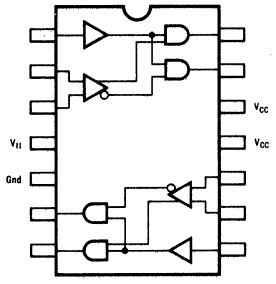
SPECIAL CIRCUITS COMING SOON



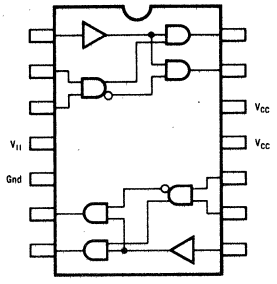
9864
3-1-3 Input AND Gate



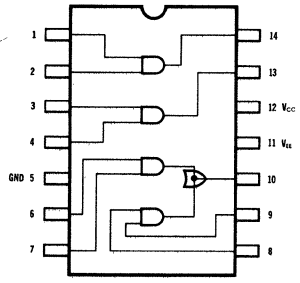
9865
Quad Single Input AND Gate



9819



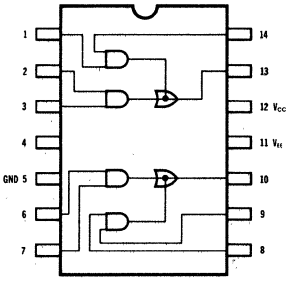
9820



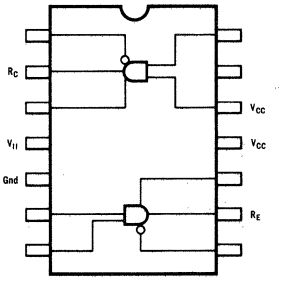
9866 / 9872

9866: Dual 2-Input AND Gate with 2 Wide, 2-Input AND-OR Gate

9872: As 9866 w/o 2K Load and Pulldown Resistors



9871
Dual 2 Wide, 2-Input AND-OR Gate

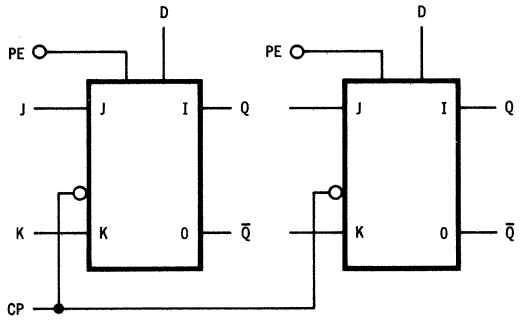


9821

9828 — J-K, D FLIP-FLOP

The 9828 is a dual J-K or D type flip-flop designed for high speed storage, counting and parallel or serial loading shift register applications.

A high input on the Parallel Enable P.E. terminal permits D type operation and a low input enables the J-K. The device is triggered on the clock falling edge and has a common clock line. Toggle frequency will be in excess of 45 MHz.



CTμL II LINE INTERFACE CIRCUITS

9819/20 — 100Ω LINE RECEIVERS

The 9819 and 9820 are dual elements designed for interfacing 100Ω transmission lines, used for peripheral equipment interconnections, with CTμL systems.

The 9819 offers a differential input; 9820 is a two input single ended receiver. Both devices have direct and inverted outputs. An active low level output enable facility permits up to eight drivers and receivers to be connected to a common buss line.

9821 — 100Ω LINE DRIVER

The 9821 is a dual 100Ω line driver designed for use with the 9819 and 20 line receivers. This element accepts single ended CTμL levels, and provides complimentary outputs.

DRIVER/RECEIVER FEATURES

Driver/Receiver pair delay — 12 nsec
Min line noise immunity ± 0.4 volts
14 lead ceramic DIP

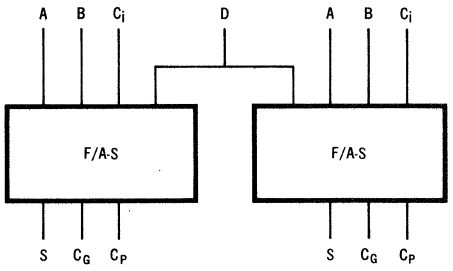
CTμL-MSI

CTμL-MSI elements offer the same advantages as the standard CCSL-MSI functions building blocks at a two to three times speed improvement. All devices have fully restored input and output levels and are clamped to reduce high frequency ringing problems. The elements will be available in the hermetic, 16 lead Dual-In-line-Package.

9822 — DUAL FULL ADDER/SUBTRACTOR

The 9822 is dual element which adds two numbers A and B and carry in C, if the enable function D is low. The sum S is produced, along with Carry Generate Cq and Carry Propagate Cp in 1 nsec. These permit the device to be used in very high speed carry look ahead configurations. If D is high the device acts as a subtractor.

This element is intended for adding or subtracting binary or BCD numbers in series or parallel, parity checking, decoding and cycle encoding applications.

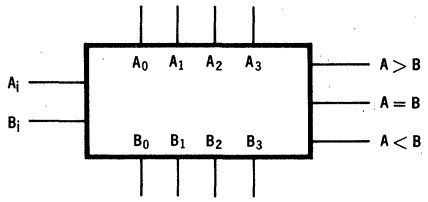


SPECIAL CIRCUITS COMING SOON

9824 — FOUR BIT COMPARATOR

The 9824 is a high speed four bit comparator for data processing and instrumentation applications. The element compares two four bit parallel words and provides a high output at the appropriate terminal A < B, A = B and A > B in 25 nsec.

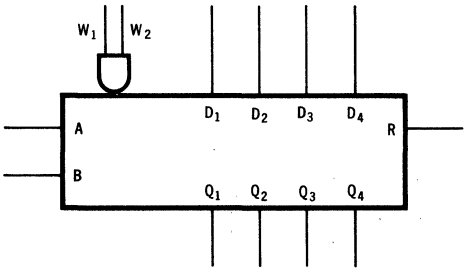
Extension to larger word sizes is achieved with the A < B and A > B inputs. A > B IN to A > B OUT is provided in 12 nsec.



9834 — QUAD LATCH

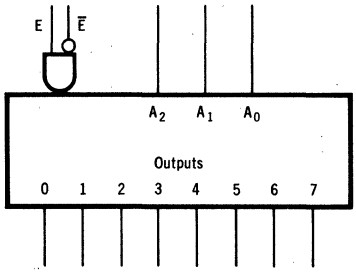
The 9834 is a gated latch circuit for 4 bit parallel data storage. Two write lines W_1 and W_2 provide clock input and clock enable facilities, common read line R presents the fully restored outputs to Q, through Q_4. Write time is 12 nsec, read time 8 nsec.

Synchronous mode controls A and B, common to all four latches determine set, clear, or data transfer function.



9838 — ONE OF EIGHT DECODER

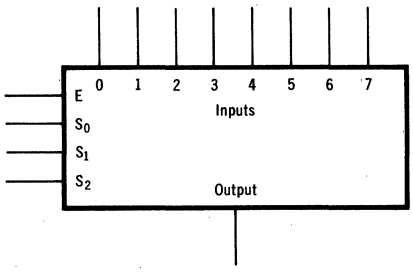
The 9838 is a multi-function decoder designed to convert three digital inputs to one of eight mutually exclusive digital outputs. A gated enable control permits use of the 9838 in many demultiplexing, memory and control decoding applications. The selected output is enabled by a high on E, and low on $\overline{E}$.



9881 — EIGHT INPUT MULTIPLEXER

The 9881 is an eight input digital multiplexer designed for gating information from several sources onto a single buss. Extension of the multiplexing capability and numerous other logic functions are provided by the enable terminal E.

Delay of 15 nsec is obtained from presentation of binary address to A_0, A_1, and A_2 to information available at the output. Device through delay is 10 nsec.



Hybrid Integrated Circuits

HYBRID CIRCUITS NUMERICAL INDEX

HYBRID CROSS REFERENCE

Function	Device	Package
Lamp & Relay Driver	SH2001	TO-100, FP
	SH2002	TO-100, FP
	SH2002-P	Plastic DIP
	SH2100	TO-99, FP
	SH2101	TO-99
	SH2200	Plastic DIP, TO-100, FP
High Impedance Amplifier	SH3000	TO-100
Analog Switch	SH3001	TO-100
	SH3002	TO-100
High Impedance Differential Comparator	SH3005	TO-99, FP
Quad Full Adder	SH2205	Ceramic DIP
Parity Generator	SH2204	FP
Voltage Regulator	SH3200	TO-99
	SH3201	TO-99
Quad Core Drivers	SH6400	FP, Ceramic DIP, Plastic DIP
	SH6401	FP, Ceramic DIP, Plastic DIP
	SH6402	FP, Ceramic DIP, Plastic DIP
	SH6500	FP, Ceramic DIP, Plastic DIP
	SH6501	FP, Ceramic DIP, Plastic DIP
	SH6502	FP, Ceramic DIP, Plastic DIP
4 Bit Arithmetic Unit	SH8080	FP
Dual Operational Amplifier	SH3741	Plastic DIP, Ceramic DIP

SH2001

HIGH-VOLTAGE, HIGH-CURRENT DRIVER

FAIRCHILD HYBRID CIRCUITS

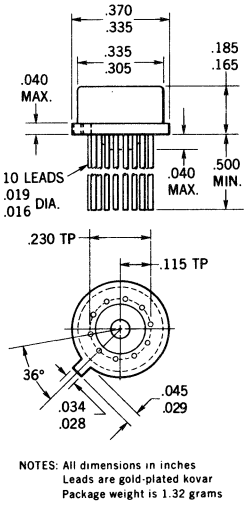
- **INPUTS CCSL COMPATIBLE**
- **USE FOR CORE, CABLE, AND LAMP DRIVER**
- **HIGH CURRENT CAPABILITY . . . 250 mA SINKING CURRENT AT 0.5 VOLT**
- **HIGH VOLTAGE CAPABILITY . . . 40 VOLTS LV_{CEO}**
- **LOGIC FLEXIBILITY . . . . . 4 INPUT NAND WITH INHIBIT (NOR) INPUT**
- **HIGH SPEED . . . . . t_{ON} = 70 ns (TYP) - - t_{OFF} = 110 ns (TYP)**

ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

Voltage Applied to Pin 8	+40 Volts
Voltage Applied to Pin 10	8 Volts
Operating Power	800 mW
Operating Temperature	(See Part Nos.)
Storage Temperature	−65°C to +150°C
Input Reverse Current	1 mA
Current on Pin 8	1 Amp

PHYSICAL DIMENSIONS

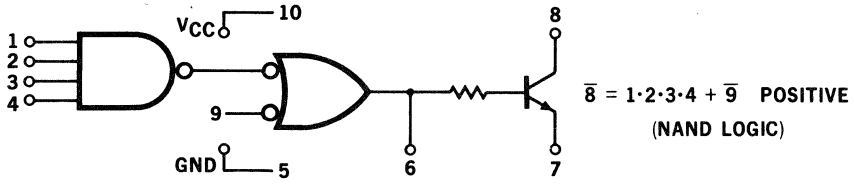
TO-100
(10 pin package)



NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

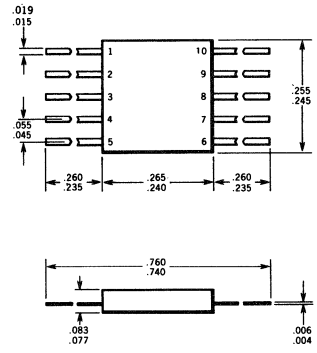
PART NO. —55°C TO +125°C HAG-20011XX
0°C TO + 70°C HAG 20019XX

LOGIC SYMBOLS AND FUNCTIONS



BG - PACKAGE

TOP VIEW



PART NO. —55°C TO +125°C HBG-20011XX
0°C TO + 70°C HBG 20019XX

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

GUARANTEED TEST SEQUENCE SH-2001

TEST NO.	LTPD GROUP	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMIT MIN.	LIMIT MAX.
1	A	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CCL}	V_8		V_{OL}
2	A	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CCL}	V_8		V_{OL}
3	A	V_{IL}				GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
4	A		V_{IL}			GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
5	A			V_{IL}		GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
6	A				V_{IL}	GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
7	A				GND	GND	I_{OL2}			V_{IH}	V_{CCL}	V_6		V_{OL2}
8	B	V_R	GND	GND	GND	GND					V_{CCH}	I_1		I_R
9	B	GND	V_R	GND	GND	GND					V_{CCH}	I_2		I_R
10	B	GND	GND	V_R	GND	GND					V_{CCH}	I_3		I_R
11	B	GND	GND	GND	V_R	GND					V_{CCH}	I_4		I_R
12	B					GND				V_R	V_{CCH}	I_9		I_R
13	C	V_F	V_R	V_R	V_R	GND					V_{CCH}	I_1		$-I_F$
14	C	V_R	V_F	V_R	V_R	GND					V_{CCH}	I_2		$-I_F$
15	C	V_R	V_R	V_F	V_R	GND					V_{CCH}	I_3		$-I_F$
16	C	V_R	V_R	V_R	V_F	GND					V_{CCH}	I_4		$-I_F$
17	C				GND	GND				V_F	V_{CCH}	I_9		$-I_F$
18	D					GND		GND			V_{CCL}	V_6	V_{OH}	
19	E	GND				GND		GND	V_{OX}		V_{CCL}	I_8		I_{OX}
20	F					GND		GND			V_{PD}	I_{10}		I_{PDH}
21	F	GND				GND					V_{MAX}	I_{10}		I_{MAX}
22*	F					GND					V_{PD}			t_{ON}
23*	F					GND					V_{PD}			t_{OFF}

*See Test Conditions and Definitions on Page 3

FORCING FUNCTIONS (Temperature Range −55°C to +125°C)

	UNITS	−55°C	+25°C	+125°C
V_{CCL}	Volts	4.50	4.50	4.50
V_{CCH}	Volts	5.50	5.50	5.50
V_{PD}	Volts		5.00	
V_{MAX}	Volts		8.00	
V_{IL}	Volts	1.40	1.10	0.80
V_{IH}	Volts	2.10	1.90	1.70
V_R	Volts	4.00	4.00	4.00
V_F	Volts	0.00	0.00	0.00
I_{OL1}	Milliamps	250	250	250
I_{OL2}	Milliamps	8.00	8.00	7.50
V_{OX}	Volts	40.0	40.0	40.0

FORCING FUNCTIONS (Temperature Range 0°C to +70°C)

	UNITS	0°C	+25°C	+70°C
V_{CCL}	Volts	5.00	5.00	5.00
V_{CCH}	Volts	5.00	5.00	5.00
V_{PD}	Volts		5.00	
V_{MAX}	Volts		8.00	
V_{IL}	Volts	1.20	1.10	.950
V_{IH}	Volts	2.00	1.90	1.80
V_R	Volts	4.00	4.00	4.00
V_F	Volts	0.45	0.45	0.50
I_{OL1}	Milliamps	250	250	250
I_{OL2}	Milliamps	8.0	8.0	7.5
V_{OX}	Volts	40.0	40.0	40.0

TEST LIMITS (Temperature Range −55°C to +125°C)

		−55°C		+25°C		+125°C	
	UNITS	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
V_{OL1}	Volts		0.45		0.40		0.45
V_{OL2}	Volts		0.45		0.40		0.45
V_{OH}	Volts	2.20		2.00		1.80	
I_R	Microamp				2.0		5.0
$-I_F$	Milliamp		1.60		1.60		1.50
I_{OX}	Microamp				5.0		200
I_{PDH}	Milliamp				30.6		
I_{MAX}	Milliamp				29.6		
t_{ON}	Nanosec.				160		
t_{OFF}	Nanosec.				220		

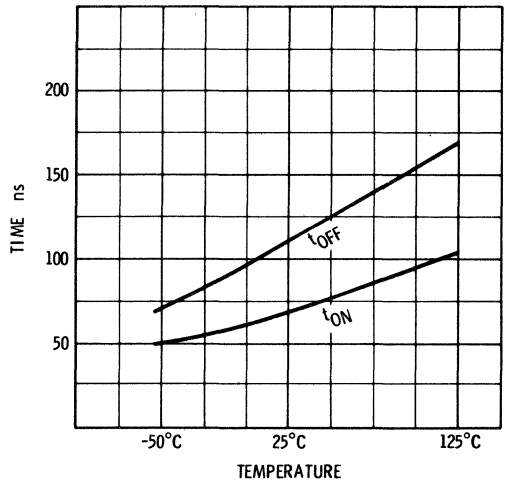
TEST LIMITS (Temperature Range 0°C to +70°C)

		0°C		+25°C		+70°C	
	UNITS	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
V_{OL1}	Volts		0.45		0.45		0.5
V_{OL2}	Volts		0.45		0.45		0.5
V_{OH}	Volts	2.05		1.95		1.85	
I_R	Microamp				5.0		10.0
$-I_F$	Milliamp		1.40		1.40		1.35
I_{OX}	Microamp				5.0		200
I_{PDH}	Milliamp				30.6		
I_{MAX}	Milliamp				34.0		
t_{ON}	Nanosec.				200		
t_{OFF}	Nanosec.				260		

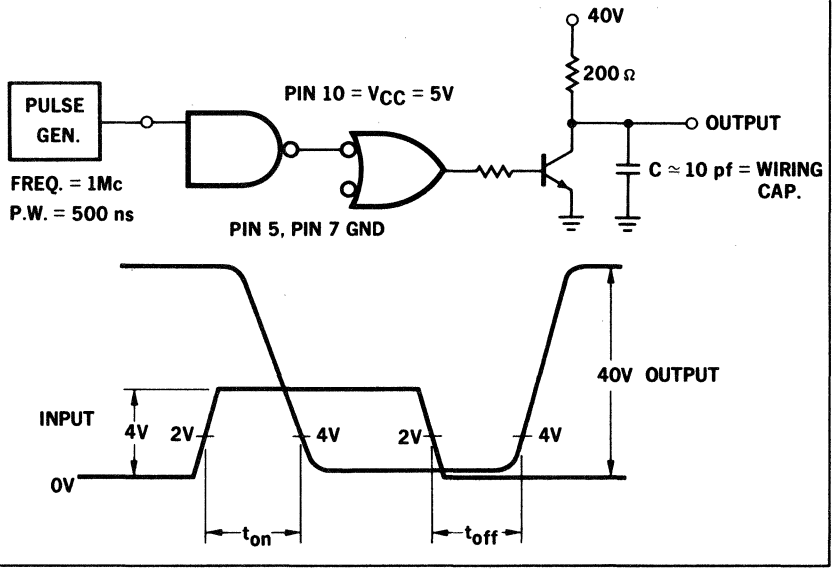
TABLE OF LTPD'S (These apply to test sequence page 2)

GROUP	COLD	25°C	HOT
A	15%	10%	15%
B		10%	15%
C	15%	10%	15%
D	15%	10%	15%
E		10%	15%
F		10%	15%

TYPICAL SWITCHING TIMES

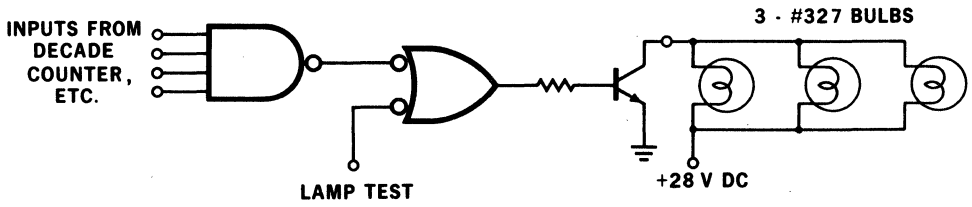


SWITCHING TIME TEST CONDITIONS

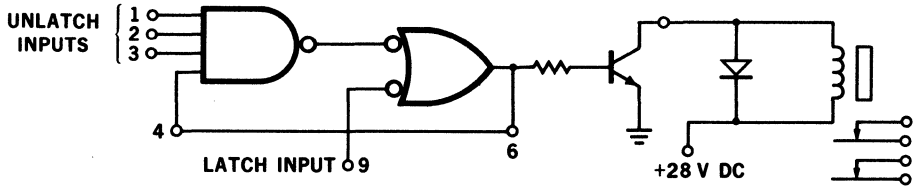


APPLICATIONS

LAMP DRIVER—

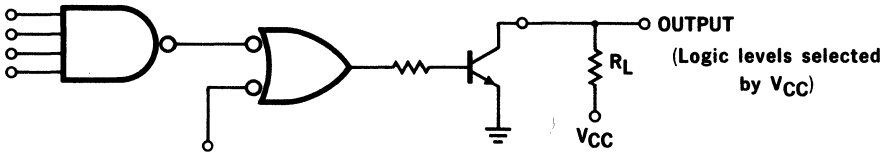


LATCHING RELAY—



Relay will unlatch if any input (1, 2, 3) goes low.

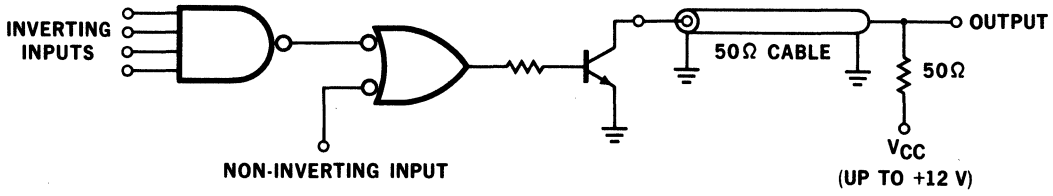
DTμL INTERFACE DRIVER—



$R_L \geq 160\Omega$ at V_{CC} = 40 VOLTS

$R_L \geq 80\Omega$ at V_{CC} = 20 VOLTS

HIGH-CURRENT LINE TRANSMITTER—



NOTE: If only non-inverting input is used, one of the inverting inputs must be grounded.

SH2002

DTμL HIGH POWER DRIVER

FAIRCHILD HYBRID CIRCUITS

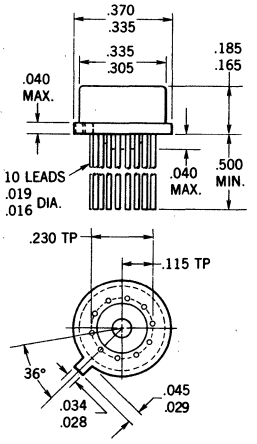
- **LOGIC FLEXIBILITY . . . . . LATCHABLE 4 INPUT NAND WITH INHIBIT (NOR) INPUT**
- **HIGH CURRENT CAPABILITY . . . UP TO 150 mA**
- **HIGH VOLTAGE CAPABILITY . . . 40 VOLTS LV_{CEO}**
- **INPUT COMPATIBLE WITH CCSL PRODUCTS**
- **FULL —55°C TO +125°C TEMPERATURE OPERATION**
- **APPLICATIONS INCLUDE CABLE AND LAMP DRIVER**

ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

Voltage Applied to Pin 10 (continuous)	+8.0 Volts
Input Reverse Current	1.0 mA
Voltage Applied to Pin 8 (continuous)	+40 Volts
Voltage Applied to Pin 10 (pulsed ≤ 1 second)	+12 Volts
Storage Temperature	−65°C to +150°C
Operating Temperature	(See Part Nos.)
Power Dissipation (Derate Linearly to +175°C)	800 mW

PHYSICAL DIMENSIONS

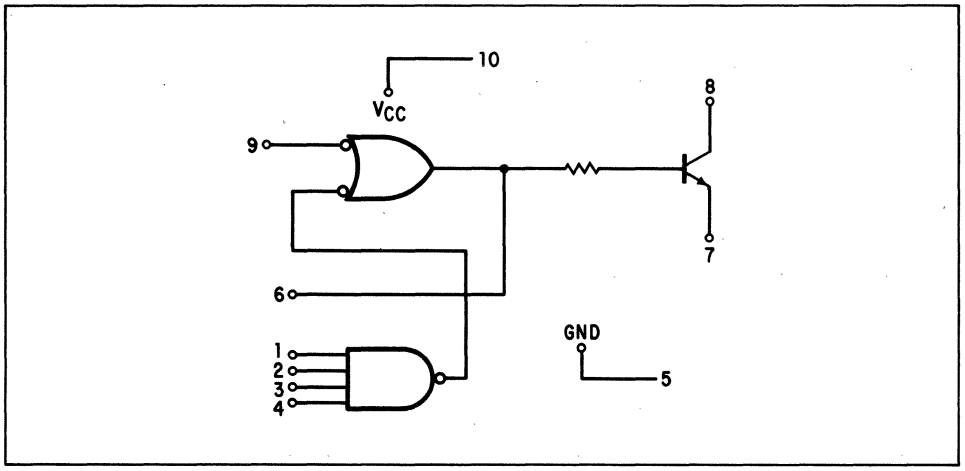
TO-100
(10 pin package)



NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

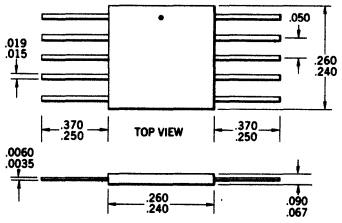
HAG20021XX (—55°C TO +125°C)
HAG20029XX (0°C TO +70°C)

LOGIC SYMBOLS AND FUNCTIONS



BG - PACKAGE

TOP VIEW



NOTES: All dimensions in inches
Alternate marking of dot in upper left hand corner is also acceptable
Package weight is approximately 0.7 gram

HBG20021XX (—55°C TO +125°C)
HBG20029XX (0°C TO +70°C)

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

GUARANTEED TEST SEQUENCE SH2002

TEST NO.	LTPD GROUP	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMIT MIN.	LIMIT MAX.
1	A	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CCL}	V_8		V_{OL}
2	A	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CCL}	V_8		V_{OL}
3	A	V_{IL}				GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
4	A		V_{IL}			GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
5	A			V_{IL}		GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
6	A				V_{IL}	GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
7	A				GND	GND	I_{OL2}			V_{IH}	V_{CCL}	V_6		V_{OL2}
8	B	V_R	GND	GND	GND	GND					V_{CCH}	I_1		I_R
9	B	GND	V_R	GND	GND	GND					V_{CCH}	I_2		I_R
10	B	GND	GND	V_R	GND	GND					V_{CCH}	I_3		I_R
11	B	GND	GND	GND	V_R	GND					V_{CCH}	I_4		I_R
12	B					GND				V_R	V_{CCH}	I_9		I_R
13	C	V_F	V_R	V_R	V_R	GND					V_{CCH}	I_1		$-I_F$
14	C	V_R	V_F	V_R	V_R	GND					V_{CCH}	I_2		$-I_F$
15	C	V_R	V_R	V_F	V_R	GND					V_{CCH}	I_3		$-I_F$
16	C	V_R	V_R	V_R	V_F	GND					V_{CCH}	I_4		$-I_F$
17	C				GND	GND				V_F	V_{CCH}	I_9		$-I_F$
18	D					GND		GND			V_{CCL}	V_6	V_{OH}	
19	E	GND				GND		GND	V_{OX}		V_{CCL}	I_8		I_{OX}
20	F					GND		GND			V_{PD}	I_{10}		I_{PDH}
21	F	GND				GND					V_{MAX}	I_{10}		I_{MAX}

FORCING FUNCTIONS (Temperature Range −55°C to +125°C)

	UNITS	−55°C	+25°C	+125°C
V_{CCL}	Volts	4.50	4.50	4.50
V_{CCH}	Volts	5.50	5.50	5.50
V_{PD}	Volts		5.00	
V_{MAX}	Volts		8.00	
V_{IL}	Volts	1.40	1.10	0.80
V_{IH}	Volts	2.10	1.90	1.70
V_R	Volts	4.00	4.00	4.00
V_F	Volts	0.00	0.00	0.00
I_{OL1}	Milliamps	150	150	150
I_{OL2}	Milliamps	8.00	8.00	7.50
V_{OX}	Volts	40.0	40.0	40.0

FORCING FUNCTIONS (Temperature Range 0°C to +70°C)

	UNITS	0°C	+25°C	+70°C
V_{CCL}	Volts	5.00	5.00	5.00
V_{CCH}	Volts	5.00	5.00	5.00
V_{PD}	Volts		5.00	
V_{MAX}	Volts		8.00	
V_{IL}	Volts	1.20	1.10	.950
V_{IH}	Volts	2.00	1.90	1.80
V_R	Volts	4.00	4.00	4.00
V_F	Volts	0.45	0.45	0.50
I_{OL1}	Milliamps	250	250	250
I_{OL2}	Milliamps	8.0	8.0	7.5
V_{OX}	Volts	40.0	40.0	40.0

TEST LIMITS (Temperature Range −55°C to +125°C)

		−55°C		+25°C		+125°C	
	UNITS	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
V_{OL1}	Volts		0.45		0.40		0.45
V_{OL2}	Volts		0.45		0.40		0.45
V_{OH}	Volts	2.20		2.00		1.80	
I_R	Microamp				2.0		5.0
$-I_F$	Milliamp		1.60		1.60		1.50
I_{OX}	Microamp				5.0		200
I_{PDH}	Milliamp				30.6		
I_{MAX}	Milliamp				29.6		

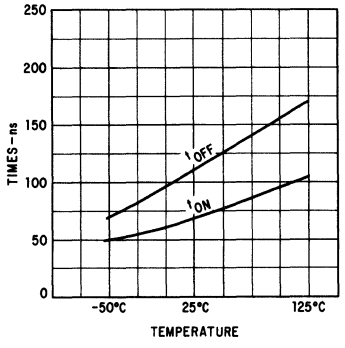
TEST LIMITS (Temperature Range 0°C to +70°C)

		0°C		+25°C		+70°C	
	UNITS	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
V_{OL1}	Volts		0.45		0.45		0.5
V_{OL2}	Volts		0.45		0.45		0.5
V_{OH}	Volts	2.05		1.95		1.85	
I_R	Microamp				5.0		10.0
$-I_F$	Milliamp		1.40		1.40		1.35
I_{OX}	Microamp				5.0		200
I_{PDH}	Milliamp				30.6		
I_{MAX}	Milliamp				34.0		

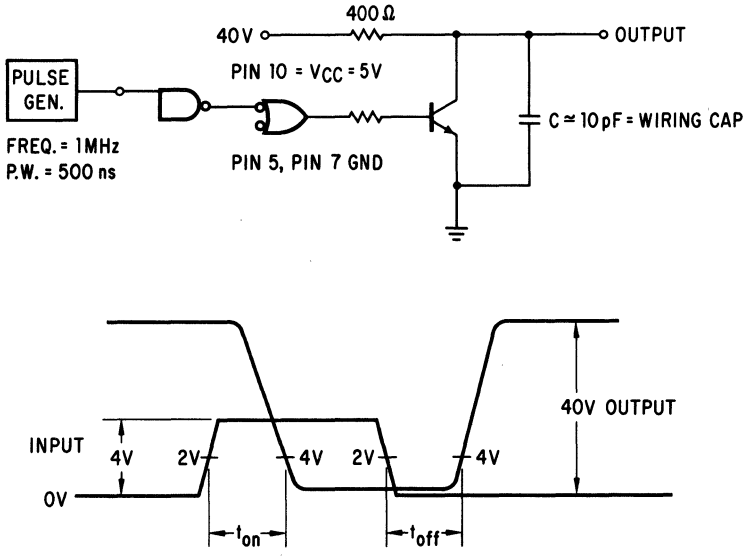
TABLE OF LTPD'S (These apply to test sequence page 2)

GROUP	COLD	+25°C	HOT
A	15%	10%	15%
B		10%	15%
C	15%	10%	15%
D	15%	10%	15%
E		10%	15%
F		10%	15%

TYPICAL SWITCHING TIMES

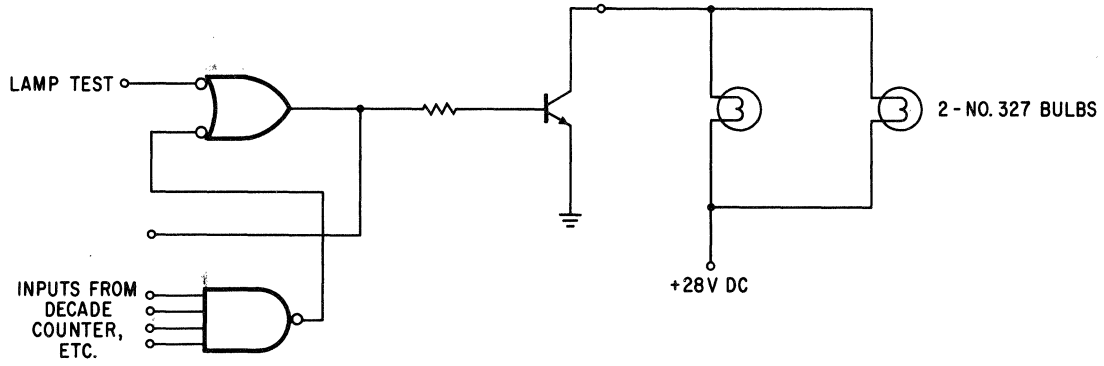


SWITCHING TIME TEST CONDITIONS

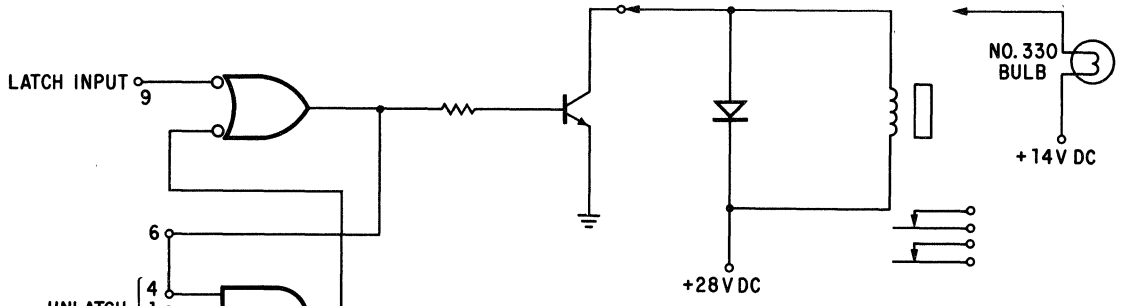


APPLICATIONS

LAMP DRIVER—

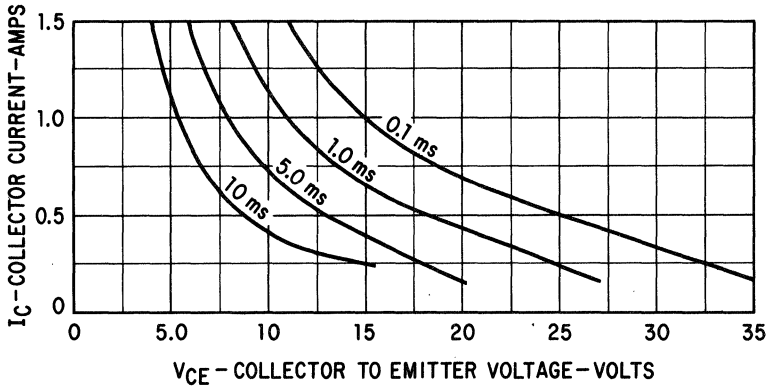


LATCHING RELAY—OR FAULT LAMP DRIVER



RELAY WILL UNLATCH IF ANY INPUT (1, 2, 3) GOES LOW.

OUTPUT TRANSFER PULSE SAFE OPERATING AREA



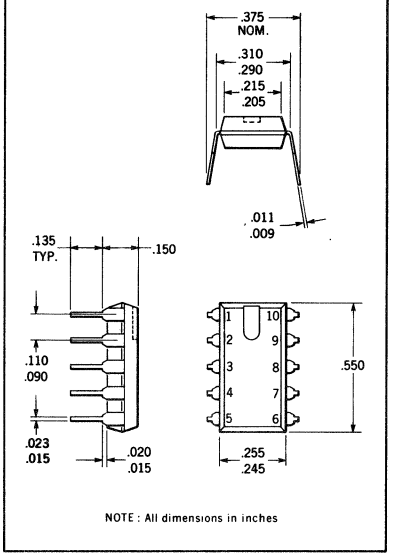
SH2002-P

DTμL HIGH POWER DRIVER

IN PLASTIC DUAL-IN-LINE PACK
FAIRCHILD HYBRID CIRCUITS

- **LOGIC FLEXIBILITY . . . . . LATCHABLE 4 INPUT NAND WITH INHIBIT (NOR) INPUT**
- **HIGH CURRENT CAPABILITY . . . UP TO 150 mA**
- **HIGH VOLTAGE CAPABILITY . . . 40 VOLTS LV_{CEO}**
- **INPUT COMPATIBLE WITH CCSL PRODUCTS**
- **APPLICATIONS INCLUDE CABLE, LAMP, AND RELAY DRIVER**

PHYSICAL DIMENSIONS

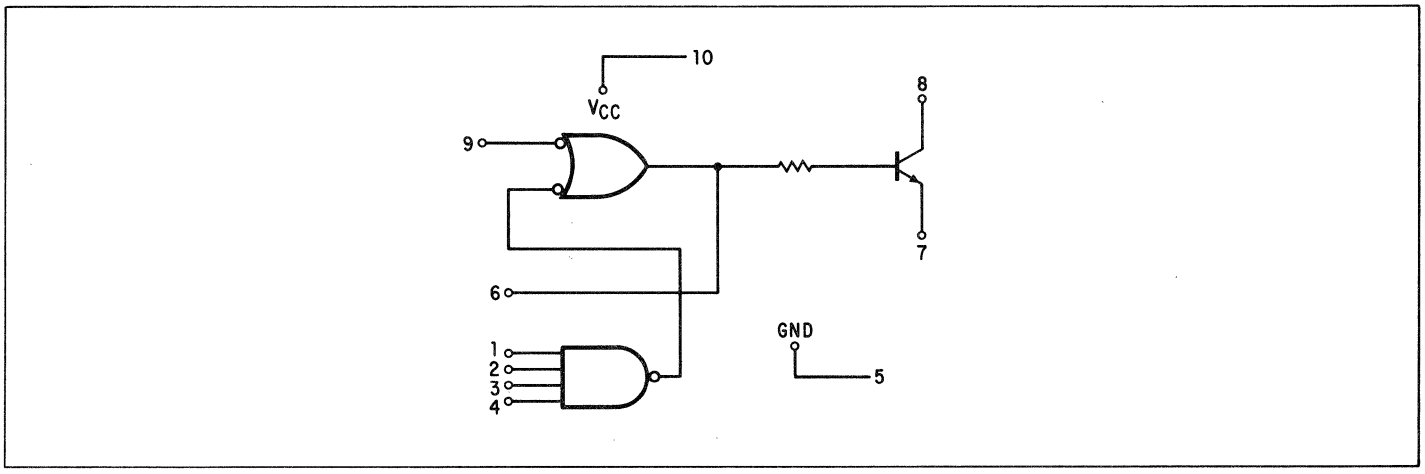


H6F20029XX (0°C TO +70°C)

ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

Voltage Applied to Pin 10 (continuous)	+8.0 Volts
Input Reverse Current	1.0 mA
Voltage Applied to Pin 8 (continuous)	+40 Volts
Voltage Applied to Pin 10 (pulsed $\leq$ 1 second)	+12 Volts
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Power Dissipation (Derate Linearly to +175°C)	800 mW

LOGIC SYMBOLS AND FUNCTIONS



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

FAIRCHILD HYBRID CIRCUIT SH2002-P

GUARANTEED TEST SEQUENCE

TEST NO.	LTPD GROUP	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMIT MIN.	LIMIT MAX.
1	A	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CCL}	V_8		V_{OL}
2	A	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CCL}	V_8		V_{OL}
3	A	V_{IL}				GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
4	A		V_{IL}			GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
5	A			V_{IL}		GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
6	A				V_{IL}	GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
7	A				GND	GND	I_{OL2}			V_{IH}	V_{CCL}	V_6		V_{OL2}
8	B	V_R	GND	GND	GND	GND					V_{CCH}	I_1		I_R
9	B	GND	V_R	GND	GND	GND					V_{CCH}	I_2		I_R
10	B	GND	GND	V_R	GND	GND					V_{CCH}	I_3		I_R
11	B	GND	GND	GND	V_R	GND					V_{CCH}	I_4		I_R
12	B					GND				V_R	V_{CCH}	I_9		I_R
13	C	V_F	V_R	V_R	V_R	GND					V_{CCH}	I_1		$-I_F$
14	C	V_R	V_F	V_R	V_R	GND					V_{CCH}	I_2		$-I_F$
15	C	V_R	V_R	V_F	V_R	GND					V_{CCH}	I_3		$-I_F$
16	C	V_R	V_R	V_R	V_F	GND					V_{CCH}	I_4		$-I_F$
17	C				GND	GND				V_F	V_{CCH}	I_9		$-I_F$
18	D					GND		GND			V_{CCL}	V_6	V_{OH}	
19	E	GND				GND		GND	V_{OX}		V_{CCL}	I_8		I_{OX}
20	F					GND		GND			V_{PD}	I_{10}		I_{PDH}
21	F	GND				GND					V_{MAX}	I_{10}		I_{MAX}

FORCING FUNCTIONS (Temperature Range 0°C to +70°C)

	UNITS	0°C	+25°C	+70°C
V_{CCL}	Volts	5.00	5.00	5.00
V_{CCH}	Volts	5.00	5.00	5.00
V_{PD}	Volts		5.00	
V_{MAX}	Volts		8.00	
V_{IL}	Volts	1.20	1.10	.950
V_{IH}	Volts	2.00	1.90	1.80
V_R	Volts	4.00	4.00	4.00
V_F	Volts	0.45	0.45	0.50
I_{OL1}	Milliamps	150	150	150
I_{OL2}	Milliamps	8.0	8.0	7.5
V_{OX}	Volts	40.0	40.0	40.0

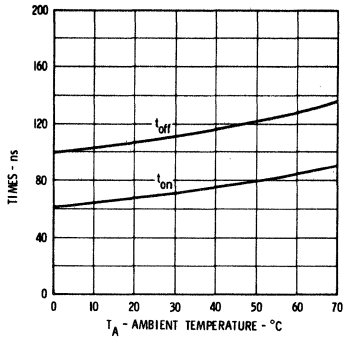
TEST LIMITS (Temperature Range 0°C to +70°C)

	UNITS	0°C MIN.	0°C MAX.	+25°C MIN.	+25°C MAX.	+70°C MIN.	+70°C MAX.
V_{OL1}	Volts		0.45		0.45		0.5
V_{OL2}	Volts		0.45		0.45		0.5
V_{OH}	Volts	2.05		1.95		1.85	
I_R	Microamp				5.0		10.0
$-I_F$	Milliamp		1.40		1.40		1.35
I_{OX}	Microamp				5.0		200
I_{PDH}	Milliamp				30.6		
I_{MAX}	Milliamp				34.0		

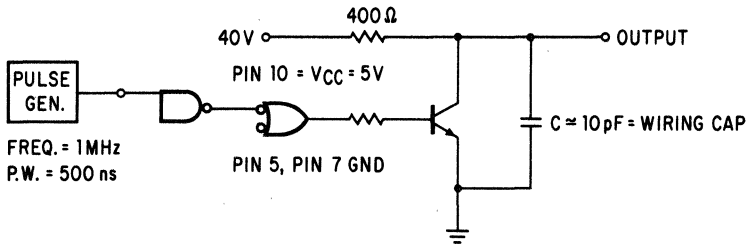
TABLE OF LTPD'S (These apply to test sequence page 2)

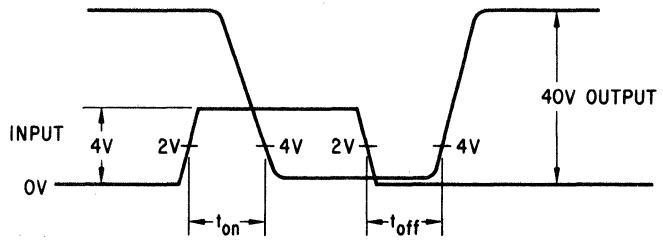
GROUP	0°C	+25°C	+70°C
A	15%	10%	15%
B		10%	15%
C	15%	10%	15%
D	15%	10%	15%
E		10%	15%
F		10%	15%

TYPICAL SWITCHING TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CONDITIONS

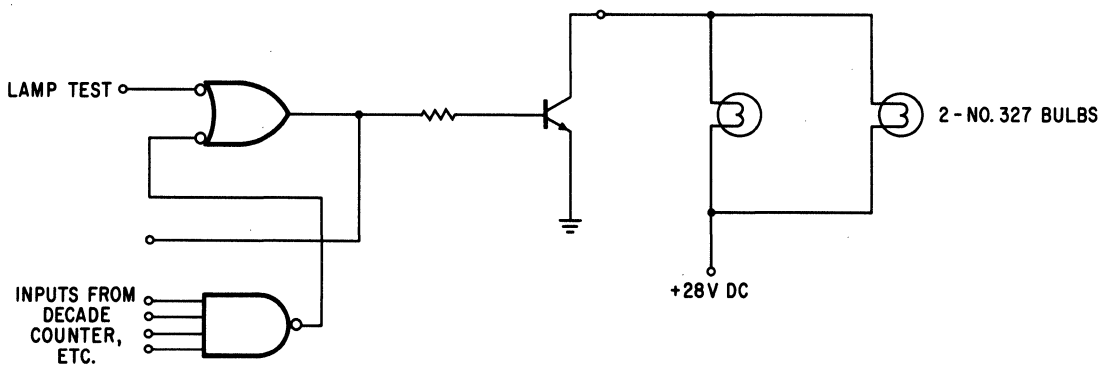




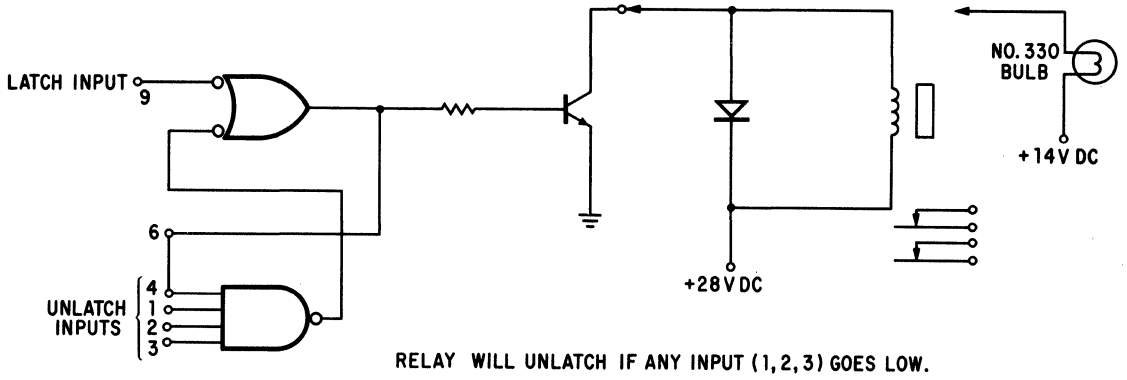
FAIRCHILD HYBRID CIRCUIT SH2002-P

APPLICATIONS

LAMP DRIVER—

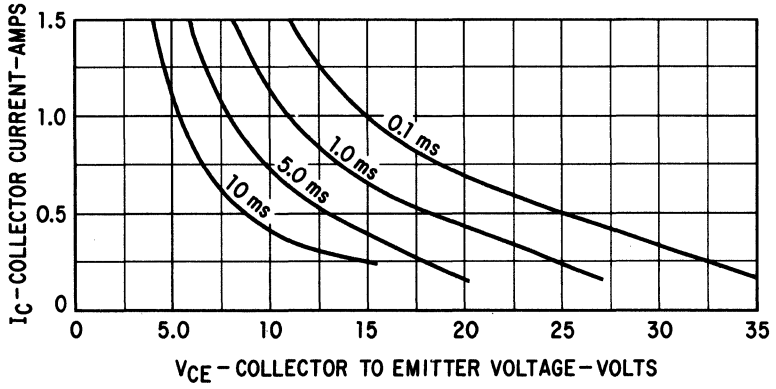


LATCHING RELAY—OR FAULT LAMP DRIVER



RELAY WILL UNLATCH IF ANY INPUT (1, 2, 3) GOES LOW.

OUTPUT TRANSFER PULSE SAFE OPERATING AREA



SH2100
HIGH CURRENT DRIVER
HYBRID CIRCUITS

GENERAL DESCRIPTION - The SH 2100 Hybrid consists of a Buffer Micrologic® Integrated Circuit driving a high-current NPN Planar* Epitaxial Silicon Transistor.

*Planar is a patented Fairchild process.

- **135 mA CURRENT SINK**
- **INPUT COMPATIBLE WITH µL, MWµL, DTµL, AND CTµL**
- **OPERATES AT 12V**
- **FAN-OUT = 200 µLOGIC LOADS**

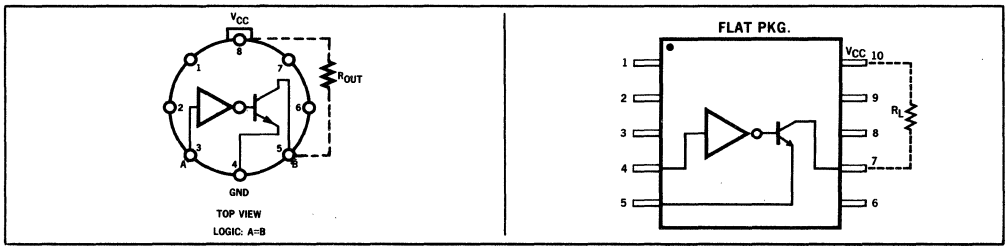
ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

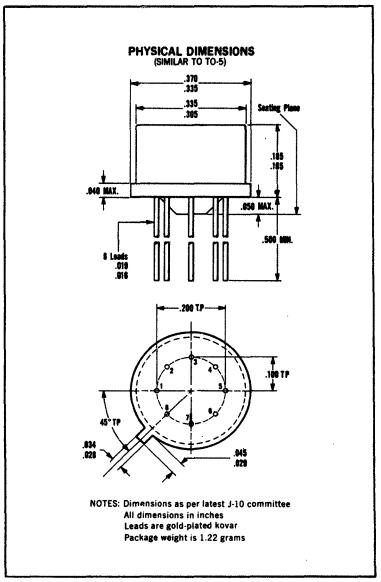
Maximum Temperatures

Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C

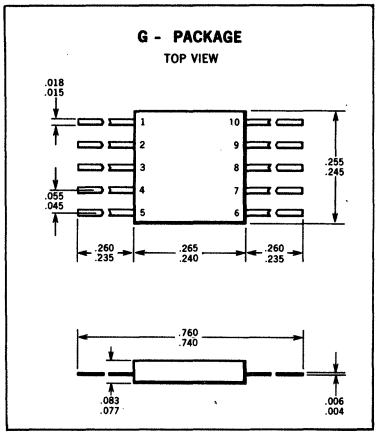
Maximum Voltages

Maximum Voltage Applied to Pin 8		+12 Volts
Maximum Voltage Applied to Pin 3		± 4 Volts
Maximum Voltage Applied to Pin 5	V_{CBO}	+30 Volts
	LV_{CEO}	+12 Volts
Maximum Total Power Dissipation at 25°C Ambient		500 mW
Typical Power Dissipation at 25°C Ambient		65 mW
Maximum Current Applied to Pin 5		500 mA
Maximum Fan-out (R_{out} = 20 Ω ± 5%) into RTL Micrologic		200





PART NO. HXK21001XX -55°C TO +125°C
HXK21009XX 0°C TO +70°C



PART NO. HBG21001XX -55°C TO +125°C
HBG21009XX 0°C TO +70°C

DC ACCEPTANCE TEST CONDITIONS

Test No.	Test Title	Units	Test Conditions Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Test Limits Min.	Typ.	Max.
1	I_3	mA			V_{IN}	GND				V_{CC}			$2I_{IN}$
2	V_5	V			V_{OFF}	GND	V_{R_2}			V_{CC}			V_{out}
3	I_5	mA			V_{ON}	GND	V_{max}			V_{max}			I_{CEX}
4	t_{3+5+}		See Switching Time Test Circuit										30 nsec
5	t_{3-5-}		See Switching Time Test Circuit										70 nsec

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

DC ACCEPTANCE TEST LIMITS

Symbol*	Test Tolerance	-55°C ±2°C	25°C ±2°C	+125°C ±2°C
V_{CC}	±0.010 V	3.00 V	3.00 V	3.00 V
V_{IN}	±0.002 V	1.014 V	0.844 V	0.674 V
V_{ON}	±0.002 V	1.014 V	0.815 V	0.674 V
V_{OFF}	±0.002 V	0.710 V	0.565 V	0.320 V
V_{R_2}	±0.01 Ω	20 Ω	20 Ω	20 Ω
V_{out}		0.710 V	0.300 V	0.320 V
V_{max}	±0.01 V	12.0 V	12.0 V	12.0 V
$2I_{IN}$		0.990 mA	0.870 mA	0.940 mA
I_{CEX}		0.100 mA	0.218 mA	0.235 mA

*For definition of the symbols refer to standard Fairchild Micrologic specification.

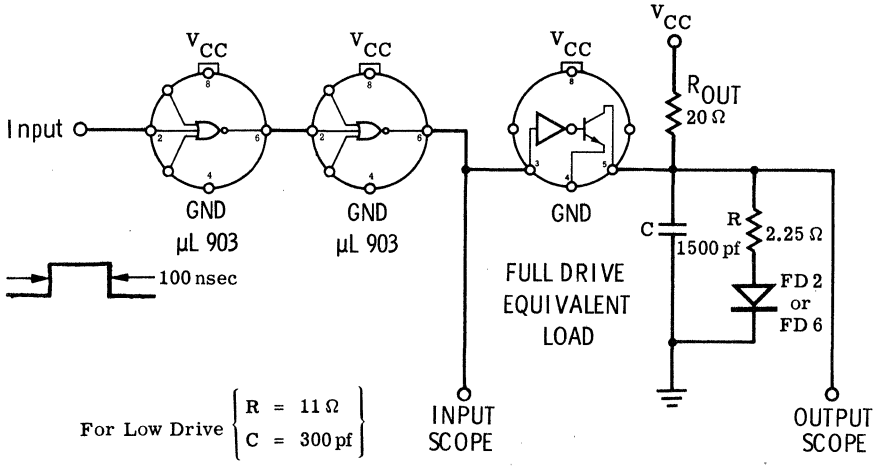
TESTS FOR END POINTS GROUP B 1, 2, 3

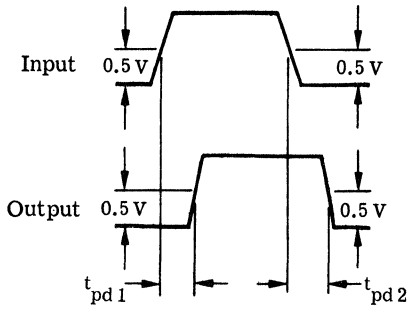
LTPD's	Test 1	10% 25°C	15% -55° & +125°C
Group A	Test 2	10% 25°C	15% -55 & +125°C
	Test 3	10% 25°C	15% -55° & +125°C

NOTE: Fairchild Assured Customer Test Programs are identical to latest issue Epitaxial μLogic Tentative Specifications.

NOTE: Mid-Range (0°C to 70°C) SH2100 Hybrids may be operated over the full military (-55°C to +125°C) temperature range by using a sliding voltage power supply which varies linearly from 4.2 V DC at -55°C to 2.6 V DC at +125°C.

SWITCHING TIME TEST CIRCUIT





NOTE: FULL DRIVE IS EQUIVALENT TO FAN-OUT OF 200 MICROLOGIC GATES.
LOW DRIVE IS EQUIVALENT TO FAN-OUT OF 40 MICROLOGIC GATES.
$T_A = 25°C$

RULES FOR SELECTING VALUES OF R_{OUT}

(Applicable over -55°C to +125°C temperature range.)

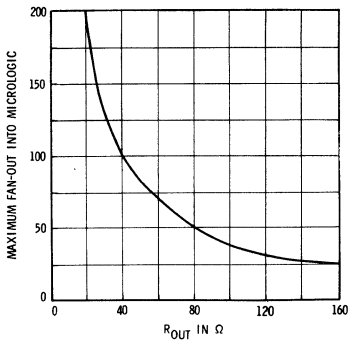
Primary consideration is to minimize overdrive to driven elements and reduce power drain.

A. MICROLOGIC Elements

$$R_{out}(min) = 20\,\Omega \pm 5\%$$

$$R_{out} = \frac{4{,}000}{\text{Max Fan-out Used}}\ \Omega$$

FANOUT MAXIMUM VS. R_{OUT}

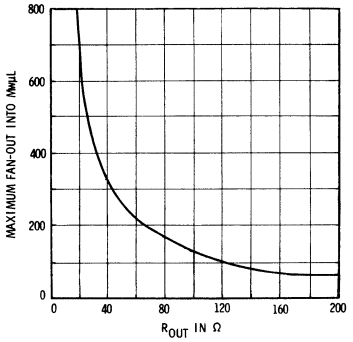


B. MWμL Elements

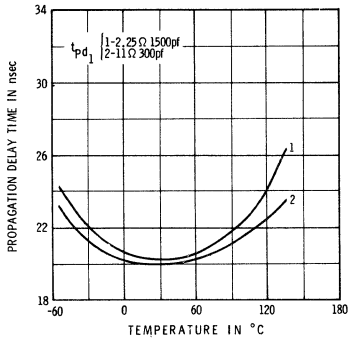
$$R_{out}(min) = 20\,\Omega \pm 5\%$$

$$R_{out} = \frac{13{,}000}{\text{Max. Fan-out Used}}\ \Omega$$

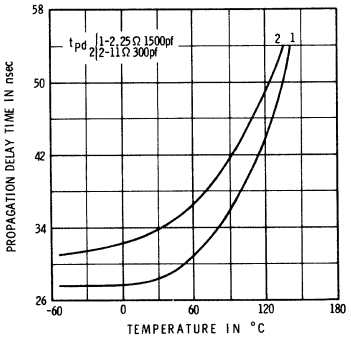
FANOUT MAXIMUM VS. R_{OUT}



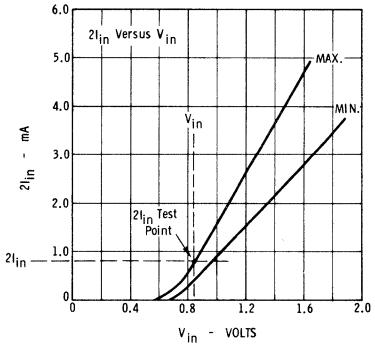
TYPICAL $t_{pd\,1}$ VERSUS TEMPERATURE



TYPICAL $t_{pd\,2}$ VERSUS TEMPERATURE



V_{IN} VERSUS $2I_{IN}$

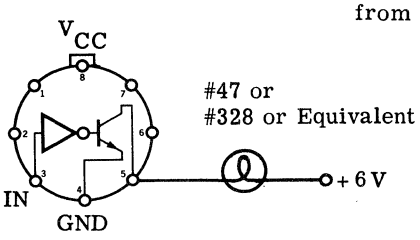


APPLICATIONS-When driven from standard MICROLOGIC

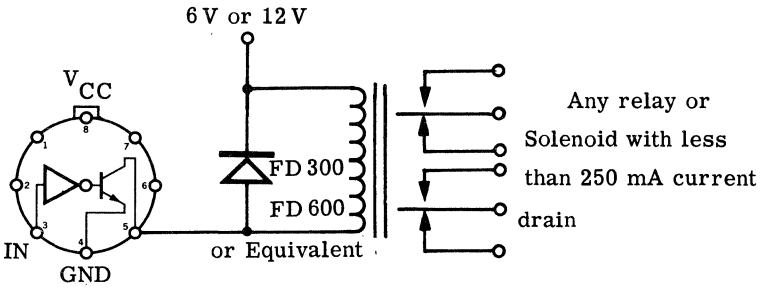
Input Loading Factor = 2 when driven from Micrologic

= 6.0 when driven from MWμL

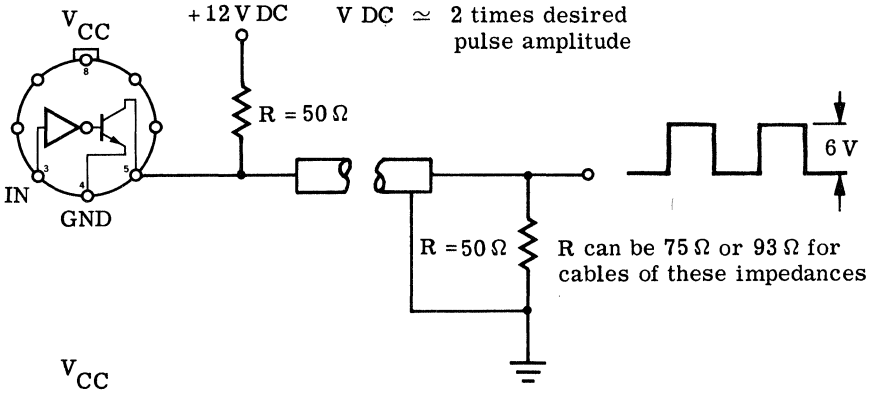
LAMP DRIVER



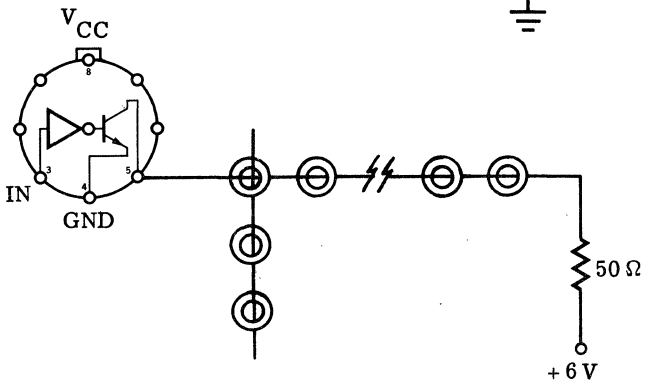
RELAY DRIVER



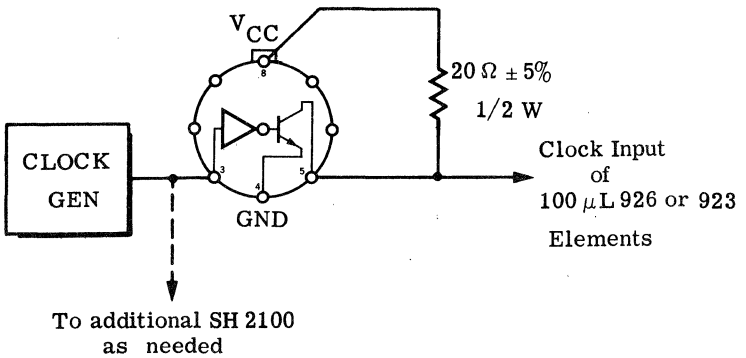
50 Ω LINE DRIVER



CORE MEMORY DRIVER



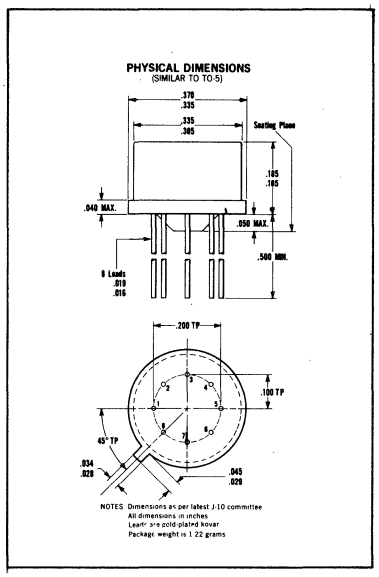
μLOGIC CLOCK DRIVER



SH2101
HIGH VOLTAGE DRIVER
HYBRID CIRCUITS

GENERAL DESCRIPTION - The Fairchild SH 2101 Hybrid High-Voltage Driver consists of an Integrated 4-input Milliwatt RTμL Gate driving a High-Voltage Transistor.

- **100 VOLT OUTPUT-CAN SINK TO 10 mA**
- **INPUT COMPATIBLE WITH µL, MILLIWATT RTµL, DTµL, AND CTµL**
- **FULL -55°C TO +125°C TEMPERATURE OPERATION**
- **APPLICATIONS INCLUDE NEON BULB AND GAS READOUT TUBE DRIVER AND HIGH VOLTAGE INTERFACING**



ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature)

Maximum Voltage Applied to Pin 8 (continuous)	+8.0 Volts
Maximum Voltage Applied to any Input Pin (continuous)	± 4.0 Volts
Maximum Voltage Applied to Pin 6 (continuous)	+100 Volts
Maximum Voltage Applied to Pin 8 (pulsed $\leq$ 1 second)	+12 Volts
Maximum Storage Temperature	-65°C to +150°C
Maximum Operating Temperature	-55°C to +125°C
Maximum Power Dissipation	250 mW

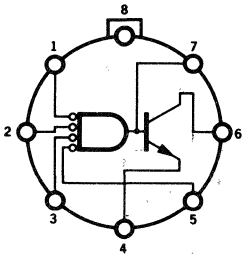
OPERATING VOLTAGE RANGE

V_{CC} (Pin 8) = +3.0 ±10% to +4.0 ±10% Volts

V_H (Pin 6) < +100 Volts

PART NO. HXK2101TXX
T=1 FOR -55°C TO +125°C TEMP. RANGE
T=9 FOR 0°C TO +70°C TEMP. RANGE

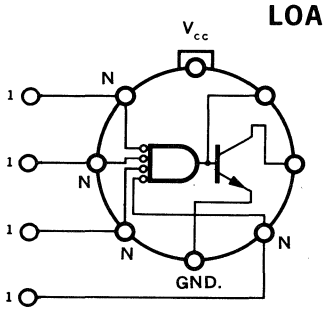
LOGIC SYMBOL



NEGATIVE LOGIC: 6 = 1 • 2 • 3 • 5
POSITIVE LOGIC: 6 = 1+2+3+5

PIN 7 IS AN EXPANDER INPUT. ADDITIONAL PAIRS OF INPUTS MAY BE ADDED USING THE MILLIWATT RTµL EXPANDER, FOLLOWING THE LOADING RULES SHOWN ON THE MILLIWATT RTµL 921 DATA SHEET.

LOAD CHART



DRIVEN BY	N (EQUIV. INPUT LOAD)
MILLIWATT RTµL	1
µL	⅓
CTµL	⅓
DRIVEN BY	**NO. OF SH-2101 ALLOWED**
DTµL GATE	3 MAX WITH NO DTµL FANOUT
BUFFER	10 MAX WITH NO DTµL FANOUT 1 MAX WITH SPECIFIED DTµL FANOUT

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD HYBRID CIRCUIT SH2101

Test No.	Test Title	Units	TEST CONDITIONS Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	TEST LIMITS Min.	Typ.	Max.
1	I_1	mA	V_{IN}	V_{BOT}	V_{BOT}	GND	V_{BOT}			V_{CC}			I_{IN}
2	I_2	mA	V_{BOT}	V_{IN}	V_{BOT}	GND	V_{BOT}			V_{CC}			I_{IN}
3	I_3	mA	V_{BOT}	V_{BOT}	V_{IN}	GND	V_{BOT}			V_{CC}			I_{IN}
4	I_5	mA	V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{IN}			V_{CC}			I_{IN}
5	V_6	mV	V_{OFF}	V_{OFF}	V_{OFF}	GND	V_{OFF}	I_{OL}		V_{CC}			V_{OL}
6	I_6	μA	V_{ON}	GND	GND	GND	GND	V_H		V_{CC}			I_{OX}
7	I_6	μA	GND	V_{ON}	GND	GND	GND	V_H		V_{CC}			I_{OX}
8	I_6	μA	GND	GND	V_{ON}	GND	GND	V_H		V_{CC}			I_{OX}
9	I_6	μA	GND	GND	GND	GND	V_{ON}	V_H		V_{CC}			I_{OX}
10	t_{1-6-}	nsec	Pulse in	GND	GND	GND	GND	Pulse out		V_{CC}			200
11	t_{1+6+}	nsec	Pulse in	GND	GND	GND	GND	Pulse out		V_{CC}			160

DC TEST LIMITS		-55°C	+25°C	+125°C
V_{CC}	V	3.00 ±0.01	3.00 ±0.01	3.00 ±0.01
V_{BOT}	V	1.80 ±0.01	1.80 ±0.01	1.80 ±0.01
V_{IN}	mV	970 ±2	805±2	590±2
V_{ON}	mV	935 ±2	750± 2	555±2
V_{OFF}	mV	650 ±2	450± 2	260±2
I_{IN}	μA	125	130	110
V_H	V	100 ±1	100±1	100±1
V_{OL}	mV	220	220	320
I_{OX}	μA	5	5	40
I_{OL}	mA	10 +0.1	10 + 0.1	10 + 0.1

SYMBOLS AND DEFINITIONS

V_{CC} Supply Voltage

V_{ON} Minimum threshold voltage which will insure an off output transistor.

V_{IN} Input voltage used to measure maximum I_{IN} required to define fan-in.

V_{BOT} Voltage level sufficient to insure full saturation of remaining input transistors for measurement of worst case input loading.

V_{OFF} The maximum voltage which may be applied to an input terminal without turning on the transistor.

I_{IN} The current drawn from the V_{IN} supply by one input of a gate with a fan-in of two or more.

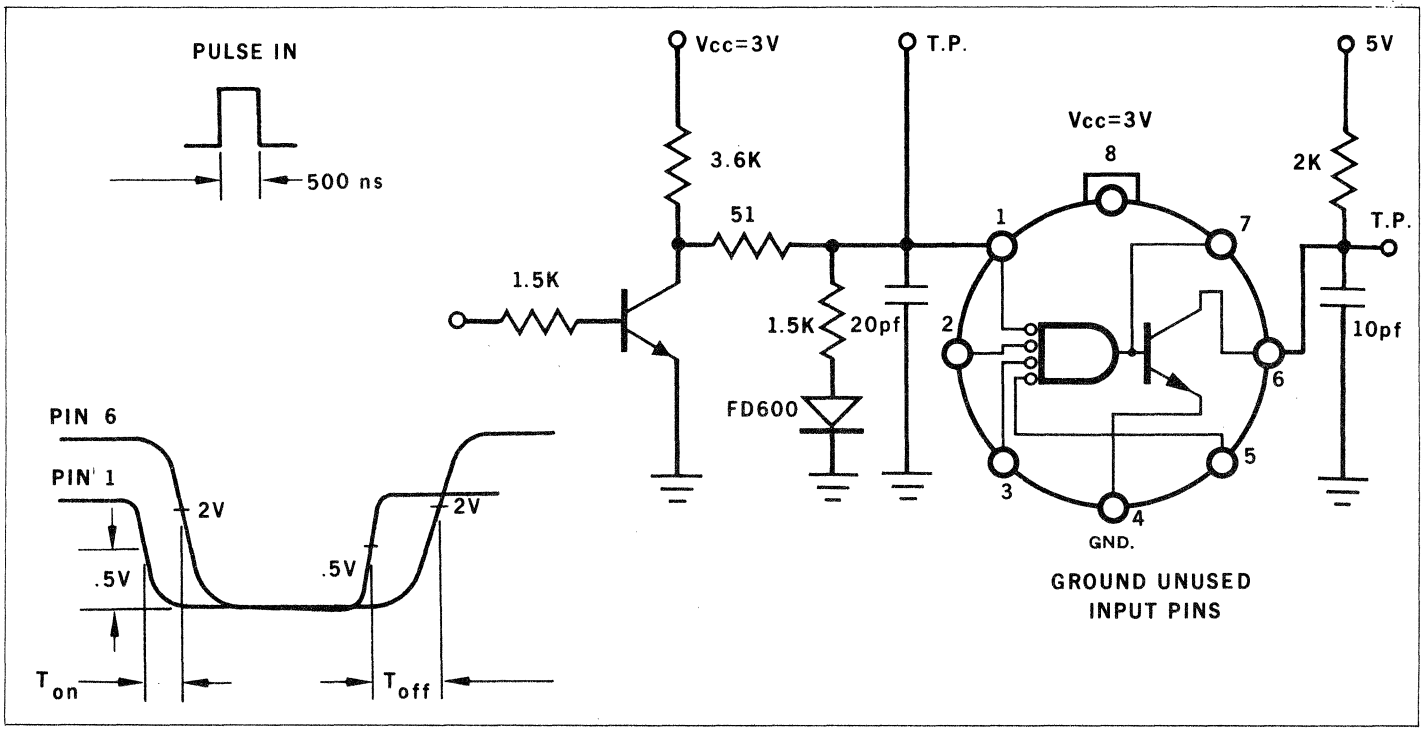
V_{OL} Maximum saturated output voltage when V_{OFF} voltage is applied at all inputs and I_{OL} is supplied to output collector.

I_{OX} Collector leakage current when V_{ON} is applied to one input and V_H is applied to output collector.

I_{OL} Output transistor collector current.

V_H Voltage applied to output collector to measure I_{OX}.

SWITCHING TIME TEST CIRCUIT



TYPICAL ELECTRICAL CHARACTERISTICS

FIG. 1
TYPICAL SWITCHING TIMES

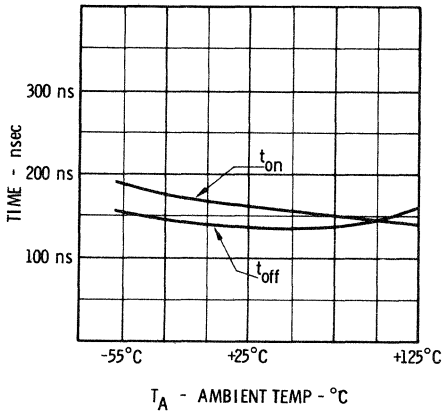
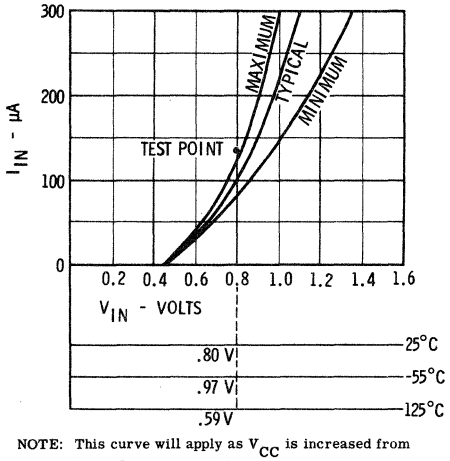
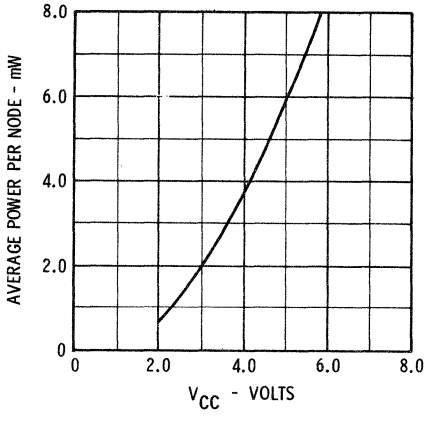


FIG. 2
TYPICAL INPUT CHARACTERISTICS

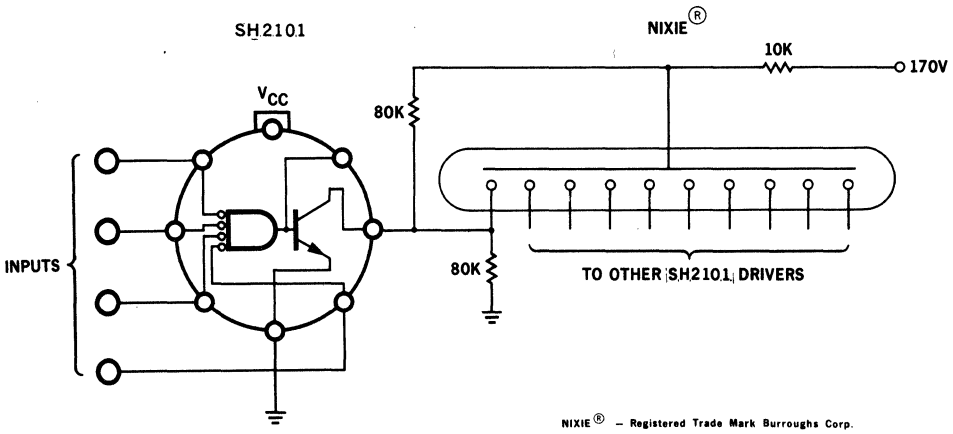


NOTE: This curve will apply as V_{CC} is increased from 3 V to 5 V with small decrease in I_{IN} for same V_{IN}.

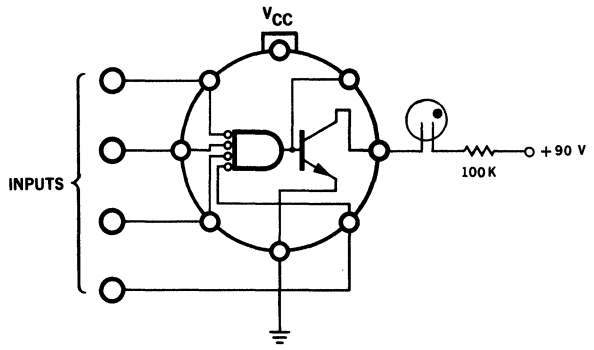
FIG. 3
TYPICAL POWER DISSIPATION VS. V_{CC} (FOR OPEN OUTPUT)



TYPICAL APPLICATION

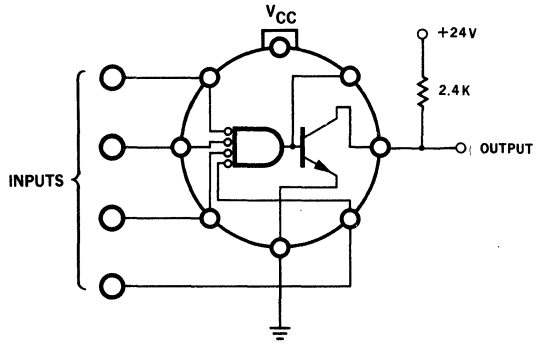


NIXIE® – Registered Trade Mark Burroughs Corp.



NEON GLOW LAMP DRIVER

NOTE: LAMP LIGHTS ONLY
WHEN ALL INPUTS ARE LOW



INTERFACE GATE — MICROLOGIC TO 24 VOLT LOGIC

NOTE: FOR 12 VOLT CIRCUITS —
USE 1.2K RESISTOR AND +12 VOLT SUPPLY
FOR DTμL AND TTμL CIRCUITS
USE 2K RESISTOR AND +5 VOLT SUPPLY

SH2200

HIGH-VOLTAGE, HIGH-CURRENT DRIVER

A FAIRCHILD HYBRID DESIGN SPECIFICATION CIRCUIT

FEATURES

- **INPUT CCSL COMPATIBLE**
- **HIGH SINKING CURRENT CAPABILITY . . . 500 mA AT 0.6 VOLT**
- **HIGH VOLTAGE CAPABILITY . . . . . 50 VOLTS, V_{OX}**
- **LOGIC FLEXIBILITY . . . . . 4 INPUT NAND WITH INHIBIT (NOR) INPUT**

APPLICATIONS

- **RELAY AND LAMP DRIVER WITH LATCHING**
- **TAPE READOUT, TEST EQUIPMENT**
- **SOLENOID DRIVER**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

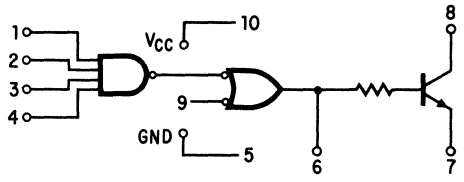
	METAL CAN & FLAT PACK		PLASTIC DIP
Maximum Temperature			
Storage Temperature	−65°C to +200°C		−65°C to +150°C
Operating Temperature	−55°C to +125°C		0°C to +70°C
Maximum Power Dissipation	***METAL CAN**	***FLAT PAK**	**PLASTIC DIP**
At 25°C Ambient Temperature	800 mW	750 mW	455 mW
Maximum Voltages and Currents			
Voltage Applied to Pin 8			+50 Volts
Voltage Applied to Pin 10			8.0 Volts
Input Reverse Current			1.0 mA
Current on Pin 8			1.0 Amp

*Use proper heat sink at temperature above 100°C.

ORDER INFORMATION

Specify H6F22009XX for 10 pin Plastic DIP, $T_A = 0°C$ to $+70°C$
HAG22001XX for pin Metal Can (JEDEC TO-100), $T_A = -55°C$ to $+125°C$
HBG22001XX for 10 pin Flat Pak, $T_A = -55°C$ to $+125°C$

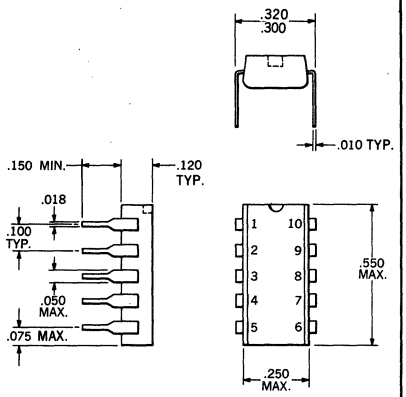
LOGIC SYMBOLS AND FUNCTIONS



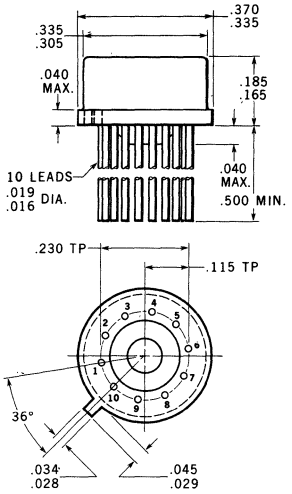
$\overline{8} = 1 \cdot 2 \cdot 3 \cdot 4 + \overline{9}$ POSITIVE (NAND LOGIC)

PHYSICAL DIMENSIONS

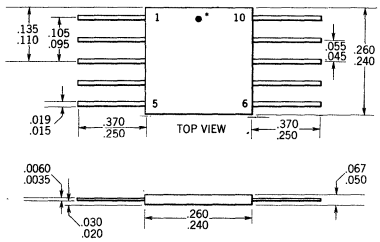
PLASTIC DIP



METAL CAN (JEDEC TO-100)



FLAT PAK



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GUARANTEED TEST SEQUENCE

TEST NO.	LTPD GROUP AT													LIMITS	
	COLD	+25°C	HOT	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	MIN	MAX
2	B	A	C	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CC}	V_8		V_{OL1}
3	B	A	C	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
4	—	—	—		V_{IL}			GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
5	—	—	—			V_{IL}		GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
6	—	—	—				V_{IL}	GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
7	B	A	C	V_{IL}				GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
8	B	A	C		V_{IL}			GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
9	B	A	C			V_{IL}		GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
10	B	A	C				V_{IL}	GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
11	B	A	C				GND	GND	I_{OL2}			V_{IH}	V_{CC}	V_6		V_{OL2}
12		A	C	V_R	GND	GND	GND	GND					V_{CC}	I_1		I_R
13		A	C	GND	V_R	GND	GND	GND					V_{CC}	I_2		I_R
14		A	C	GND	GND	V_R	GND	GND					V_{CC}	I_3		I_R
15		A	C	GND	GND	GND	V_R	GND					V_{CC}	I_4		I_R
16		A	C					GND				V_R	V_{CC}	I_9		I_R
17	B	A	C	V_F	V_R	V_R	V_R	GND					V_{CC}	I_1		$-I_F$
18	B	A	C	V_R	V_F	V_R	V_R	GND					V_{CC}	I_2		$-I_F$
19	B	A	C	V_R	V_R	V_F	V_R	GND					V_{CC}	I_3		$-I_F$
20	B	A	C	V_R	V_R	V_R	V_F	GND					V_{CC}	I_4		$-I_F$
21	B	A	C				GND	GND				V_F	V_{CC}	I_9		$-I_F$
22	B	A	C					GND		GND			V_{CC}	V_6	V_{OH1}	
23	—	A	C	GND				GND	I_{OL3}	GND	V_{OX}		V_{CC}	I_8		I_{OX}
24	—	A	—					GND					V_{PD}	I_{10}		I_{PD}
25	—	A	—	GND				GND				GND	V_{MAX}	I_{10}		I_{MAX}

FORCING FUNCTIONS (Temperature Range 0°C to 70°C)

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{CC}	5.0	5.0	5.0	Volts
V_{PD}		5.0		Volts
V_{MAX}		8.0		Volts
V_{IL}	0.85	0.85	0.85	Volts
V_{IH}	1.9	1.8	1.6	Volts
V_R	4.5	4.5	4.5	Volts
V_F	0.45	0.45	0.45	Volts
V_{OX}		50	50	Volts
I_{OL1}	500	500	500	mA
I_{OL2}	16	16	16	mA
I_{OL3}		8.0		mA

TEST LIMITS (Temperature Range 0°C to 70°C)

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{OL1}	0.6	0.6	0.6	Volts
V_{OL2}	0.45	0.45	0.45	Volts
V_{OH1}	1.95	1.85	1.65	Volts
I_R		60	60	μA
$-I_F$	1.6	1.6	1.6	mA
I_{OX}		5.0	200	μA
I_{PD}		12.2		mA
I_{MAX}		10		mA

FORCING FUNCTIONS (Temperature Range −55°C to +125°C)

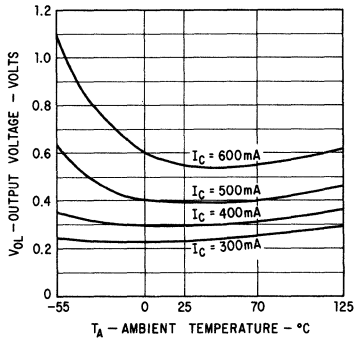
SYMBOL	−55°C	+25°C	+125°C	UNITS
V_{CC}	5.0	5.0	5.0	Volts
V_{PD}		5.0		Volts
V_{MAX}		8.0		Volts
V_{IL}	0.8	0.9	0.8	Volts
V_{IH}	2.0	1.7	1.4	Volts
V_R	4.5	4.5	4.5	Volts
V_F	0.4	0.4	0.4	Volts
V_{OX}		50	50	Volts
I_{OL1}	500	500	500	mA
I_{OL2}	16	16	16	mA
I_{OL3}		8.0		mA

TEST LIMITS (Temperature Range −55°C to +125°C)

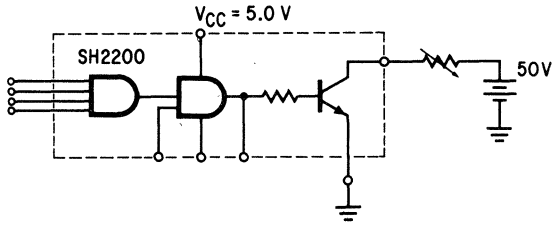
SYMBOL	−55°C	+25°C	+125°C	UNITS
V_{OL1}	0.8	0.6	0.7	Volts
V_{OL2}	0.4	0.4	0.4	Volts
V_{OH1}	2.05	1.75	1.45	Volts
I_R		60	60	μA
$-I_F$	1.6	1.6	1.6	mA
I_{OX}		5.0	200	μA
I_{PD}		11		mA
I_{MAX}		9.0		mA

ELECTRICAL CHARACTERISTICS

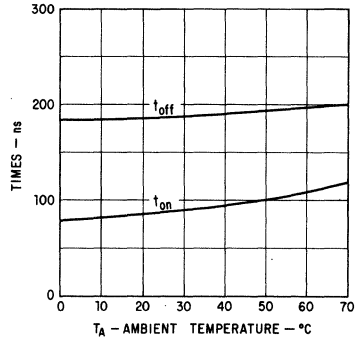
TYPICAL OUTPUT VOLTAGE VERSUS AMBIENT TEMPERATURE



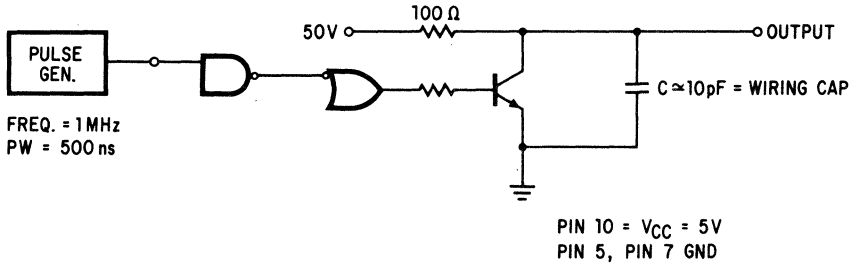
OUTPUT VOLTAGE TEST CIRCUIT



TYPICAL SWITCHING TIME VERSUS AMBIENT TEMPERATURE

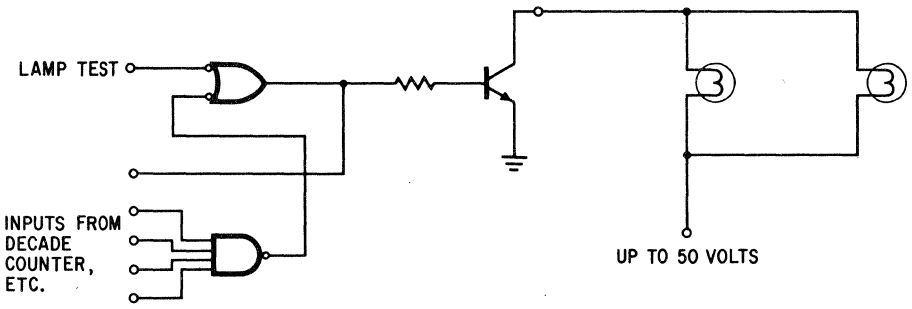


SWITCHING TIME TEST CIRCUIT

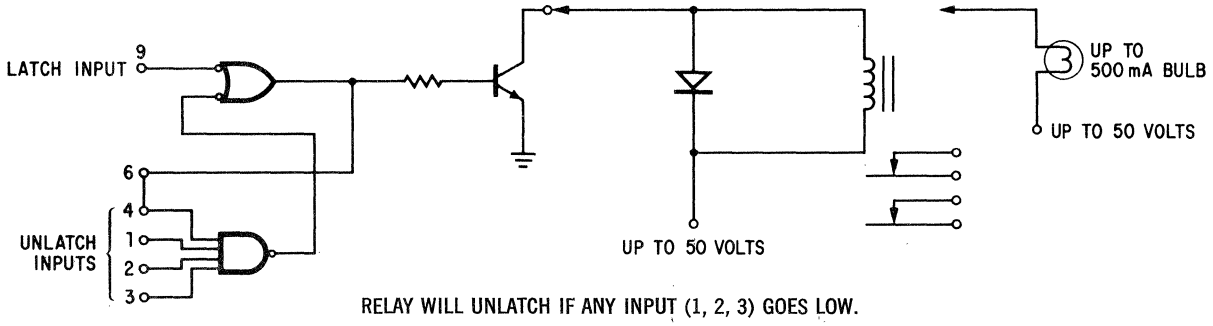


APPLICATION

LAMP DRIVER



LATCHING RELAY OR FAULT LAMP DRIVER



RELAY WILL UNLATCH IF ANY INPUT (1, 2, 3) GOES LOW.

SH2204

BYTE PARITY GENERATOR OR CHECKER

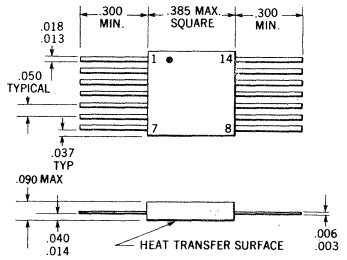
A FAIRCHILD HYBRID DESIGN SPECIFICATION CIRCUIT

GENERAL DESCRIPTION — The SH2204 consists of four high speed binary full adders. The design is two 9304 MSI circuits useful to generate parity for an 8 bit byte or to check parity over 9 bits. Delay from input to odd parity is typically 35 ns. Additional parity units can be connected for larger word lengths.

FEATURES:

- **35 ns TYPICAL INPUT TO ODD PARITY DELAY**
- **ALL INPUT DIODE CLAMPING**
- **CCSL INTERFACE**

PHYSICAL DIMENSIONS

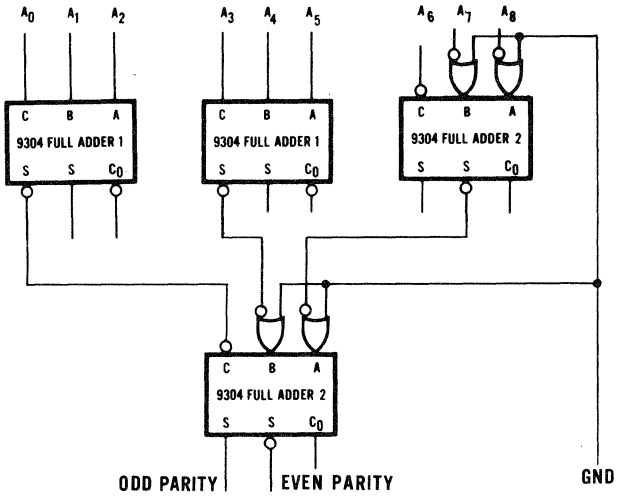


ORDER PART NOS.:
HBK22041XX (−55°C to +125°C)
HBK22049XX (0°C to 70°C)

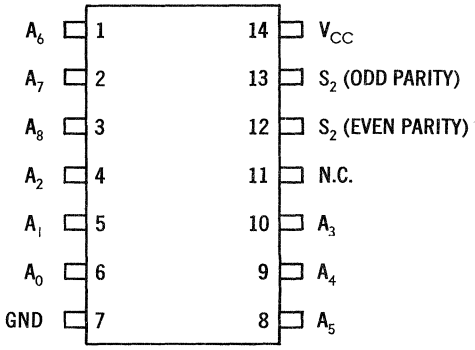
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC DIAGRAM



PIN CONFIGURATION



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ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$ $V_{CC} = 4.5\ V$, $I_{OH} = -1.08\ mA$ $V_{CC} = 4.5\ V$, $I_{OH} = -0.84\ mA$
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16\ mA$ $I_{OL} = 14.4\ mA$ $I_{OL} = 11.2\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $I_{OL} = 11.2\ mA$ $I_{OL} = 8.7\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
$4\ I_F$	Input Load Current		−6.4		−4.4	−6.4		−6.4	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$4\ I_F$	Input Load Current		−4.96		−3.88	−4.96		−4.96	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$4\ I_R$	Input Leakage Current				60	240		240	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$ Ground on other inputs

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +70°C MIN.	LIMITS +70°C MAX,	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$ $V_{CC} = 4.75\ V$, $I_{OH} = -1.08\ mA$ $V_{CC} = 4.75\ V$, $I_{OH} = -0.84\ mA$
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$ $I_{OL} = 14.4\ mA$ $I_{OL} = 11.2\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $I_{OL} = 12.7\ mA$ $I_{OL} = 9.85\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
$4\ I_F$	Input Load Current		−6.4		−4.0	−6.4		−6.4	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
$4\ I_F$	Input Load Current		−5.64		−3.6	−5.64		−5.64	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
$4\ I_R$	Input Leakage Current				60	240		240	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$ Ground on other inputs

SH2205

RIPPLE CARRY ADDER

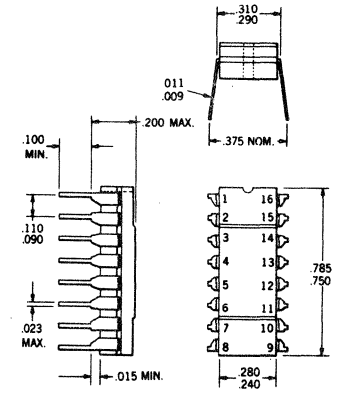
A FAIRCHILD HYBRID DESIGN SPECIFICATION CIRCUIT

GENERAL DESCRIPTION — The SH2205 consists of four, high speed, binary full adders. The adder is useful as ripple carry parallel addition (or subtraction) function blocks. Circuits are TTμL for high speed, high fanout operation and is compatible with all members of the CCSL group of digital integrated circuits.

FEATURES:

- **8.0 ns TYPICAL CARRY PROPAGATION DELAY PER BIT**
- **ALL INPUT DIODE CLAMPING**
- **CCSL INTERFACE**

PHYSICAL DIMENSIONS



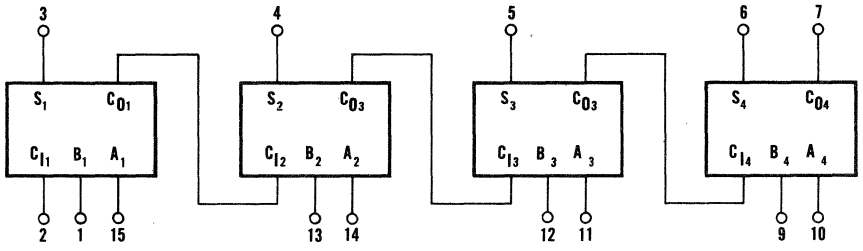
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

ORDER PART NO. H6B2205IXX

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 to+7 V
Voltage Applied to Output when output is high	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to 5.5 V

SCHEMATIC DIAGRAM



$V_{CC} = 16$
GND = 8

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LOADING RULES (1UL = 1.6 mA)

INPUTS	LOADING
A_1, B_1, A_3, B_3, & CI_1	4UL
A_2, B_2, A_4 & B_4	1UL
OUTPUTS	**FAN OUT**
S_1 & S_3	10UL
S_2 & S_4	9UL
CO_4	7UL

TRUTH TABLE
(Each Stage)

INPUTS			OUTPUTS	
C_{In}	A_n	B_n	S_n	CO_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$ (Pins 3 & 5) $V_{CC} = 4.5\ V$, $I_{OH} = -1.08\ mA$ (Pins 4 & 6) $V_{CC} = 4.5\ V$, $I_{OH} = -0.84\ mA$ (Pin 7)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16\ mA$ (Pins 3 & 5) $I_{OL} = 14.4\ mA$ (Pins 4 & 6) $I_{OL} = 11.2\ mA$ (Pin 7) $V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ (Pins 3 & 5) $I_{OL} = 11.2\ mA$ (Pins 4 & 6) $I_{OL} = 8.7\ mA$ (Pin 7)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, 5.5 V on other inputs
$4\ I_F$	Input Load Current		−6.4		−4.4	−6.4		−6.4		
I_F	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, 5.5 V on other inputs
$4\ I_F$	Input Load Current		−4.96		−3.88	−4.96		−4.96		
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
$4\ I_R$	Input Leakage Current				60	240		240		Ground on other inputs
t_{pd+}	C_I to C_{O4}				35	55			ns	$V_{CC} = 5.0\ V$
t_{pd-}	C_I to C_{O4}				35	55			ns	$C_L = 15\ pF$

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$ (Pins 3 & 5) $V_{CC} = 4.75\ V$, $I_{OH} = -1.08\ mA$ (Pins 4 & 6) $V_{CC} = 4.75\ V$, $I_{OH} = -0.84\ mA$ (Pin 7)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$ (Pins 3 & 5) $I_{OL} = 14.4\ mA$ (Pins 4 & 6) $I_{OL} = 11.2\ mA$ (Pin 7) $V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ (Pins 3 & 5) $I_{OL} = 12.7\ mA$ (Pins 4 & 6) $I_{OL} = 9.85\ mA$ (Pin 7)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
$4\ I_F$	Input Load Current		−6.4		−4.0	−6.4		−6.4		5.25 V on other inputs
I_F	Input Load Current		−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$
$4\ I_F$	Input Load Current		−5.64		−3.6	−5.64		−5.64		5.25 V on other inputs
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
$4\ I_R$	Input Leakage Current				60	240		240		Ground on other inputs
t_{pd+}	C_I to C_{O4}				35	55			ns	$V_{CC} = 5.0\ V$
t_{pd-}	C_I to C_{O4}				35	55			ns	$C_L = 15\ pF$

SH3000

HIGH IMPEDANCE, WIDEBAND DC AMPLIFIER

FAIRCHILD HYBRID CIRCUITS

GENERAL DESCRIPTION - The SH 3000 Hybrid consists of a pair of high-gain, matched transistors connected as emitter-followers at the inputs of a μA 702A operational amplifier.

FEATURES

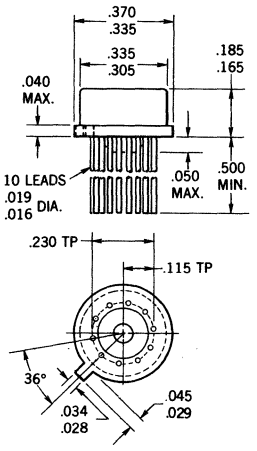
- **5 MΩ TYPICAL INPUT IMPEDANCE**
- **0.3 μA TYPICAL INPUT BIAS CURRENT**
- **DC TO 30 MHz USEFUL BANDWIDTH**
- **LATCH-UP PROTECTED**
- **–55°C TO +125°C TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage Between V^+ and V^- Terminals	21 Volts
Peak Load Current	50 mA
Input Voltage	+0.5 V to -6.0 V
Differential Input Voltage	± 5 Volts
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

TO-100
(10 pin package)

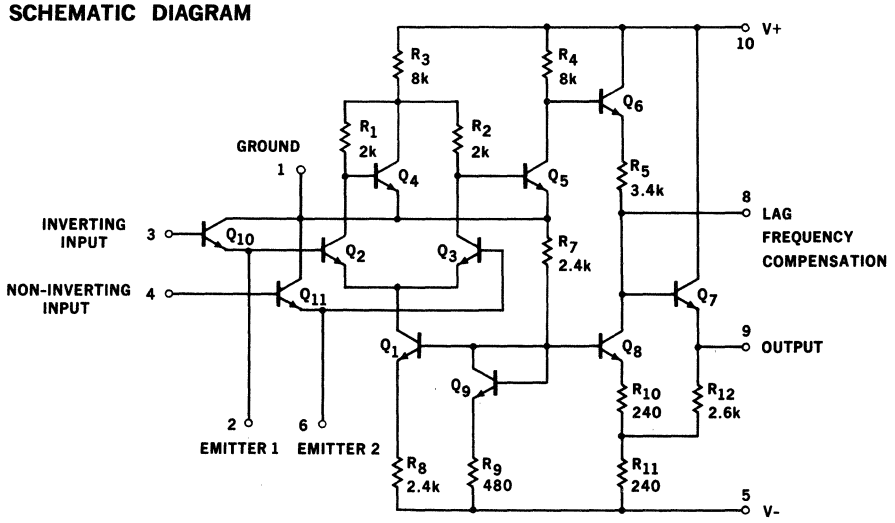


NOTES: All dimensions in inches
Leads are gold-plated kovar

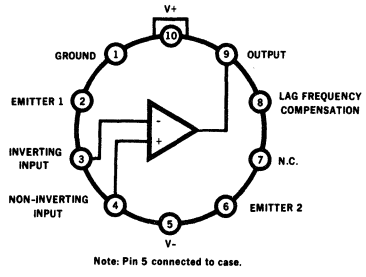
Package weight is 1.32 grams

PART NO. HAG30001XX:
–55°C TO +125°C

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



Note: Pin 5 connected to case.

CONNECTION DIAGRAM
(TOP VIEW)

NOTE 1: Rating applies for case temperatures to +125°C; derate linearity at 5.6 mW/°C for ambient temperatures above +125°C.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

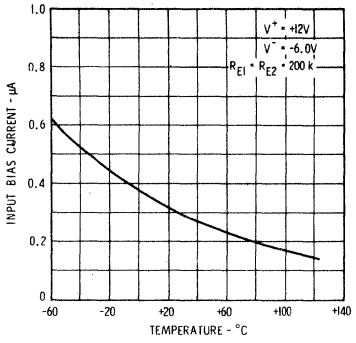
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V^+ = 12 V, V^- = -6.0 V, R_{E1} = R_{E2} = 200 k unless otherwise noted)

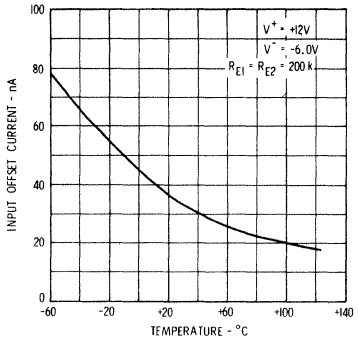
Parameter	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 20$ k		2.0	6.0	mV
Input Offset Current			35	100	nA
Input Bias Current			300	750	nA
Input Resistance		1.0	5.0		m Ω
Input Voltage Range		-3.5		0	V
Common Mode Rejection Ratio	$R_S \leq 20$ k, f ≤ 1 kHz	70	80		dB
Voltage Gain		1400	2600		
Output Voltage Swing	$R_L \geq 100$ k	±5.0	±5.3		V
Supply Voltage Rejection Ratio			75		μV/V
Power Consumption			70	120	mW
The following Specifications apply for -55°C ≤ +125°C:					
Input Offset Voltage	$R_S \leq 20$ k			7.5	mV
Voltage Gain		1000			
Input Offset Current	T_A = +125°C			100	nA
Input Offset Current	T_A = -55°C			200	nA
Input Bias Current	T_A = -55°C			1.0	μA
Average Temperature Coefficient of Input Offset Voltage			7.5		μV/°C

TYPICAL PERFORMANCE CURVES

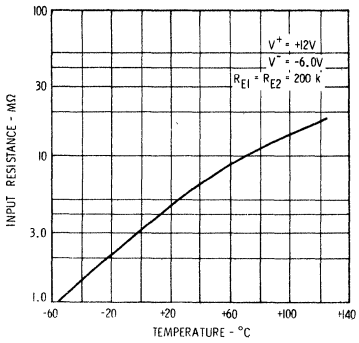
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



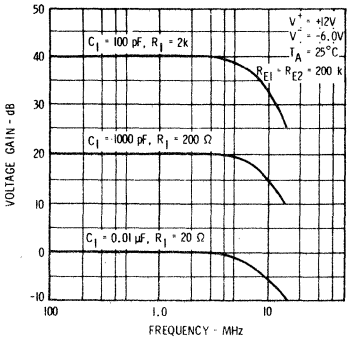
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



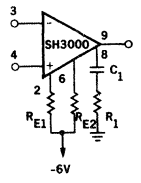
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



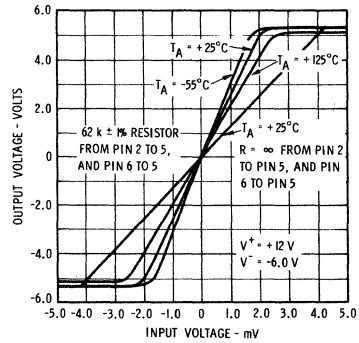
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



FREQUENCY COMPENSATION CIRCUIT



VOLTAGE TRANSFER CHARACTERISTIC

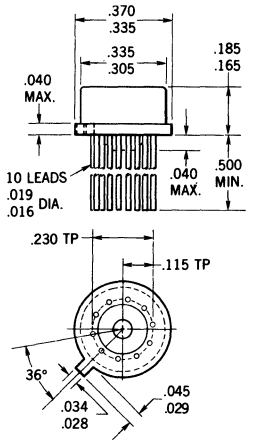


SH 3001
ANALOG SWITCH
FAIRCHILD HYBRID CIRCUITS

- **INPUTS CCSL COMPATIBLE**
- **mW MICROLOGIC AND MICROLOGIC COMPATIBLE INPUTS**
- **LOW FEED THROUGH SPIKES ON THE OUTPUT**
- **TYPICAL t_{on} - - 145 ns LOADED**
- **APPLICATIONS - - SCANNING, MULTIPLEXING, A/D CONVERSION, 4-POLE ST NORMALLY OPEN RELAY OR CHOPPER**

PHYSICAL DIMENSIONS

TO-100
(10 pin package)



NOTES: All dimensions in inches
Leads are gold-plated kovar

Package weight is 1.02 grams

PART NO. HAG30011XX

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

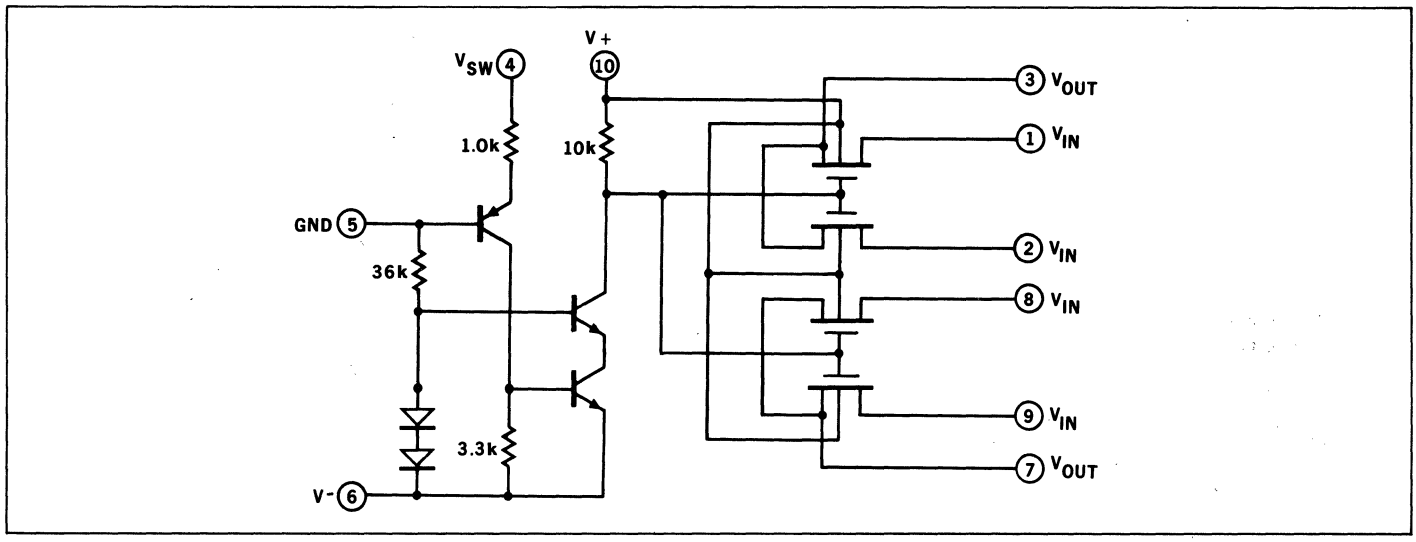
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C

Maximum Power Dissipation

at 25°C Case	500 mW
at 25°C Ambient	350 mW

Maximum Voltages and Current

V_{in} (Pins 1, 2, 8 & 9)	±10 V
V_{out} (Pins 3 & 7)	±10 V
V^+ (Pin 10)	+11 V
V^- (Pin 6)	-22 V
I_{in}, I_{out}	100 mA
V_{switch} (Pin 4)	±6 V



Electrical Characteristics on page 2

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

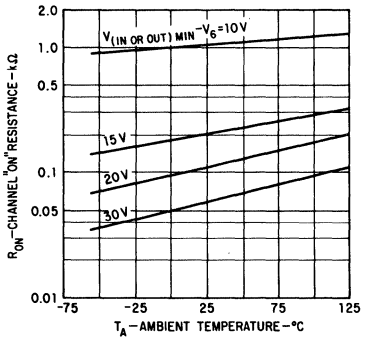
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 10 V, V^- = -20 V Unless Otherwise Specified)

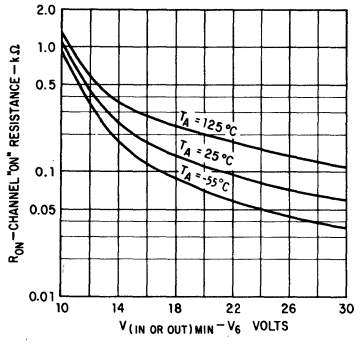
Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Conditions
I_{SWH}	High Switch Drive Current (On)			0.4	mA	T_A = -55°C to +125°C
V_{SWL}	Low Switch Drive Voltage (Off)			0.6	V	T_A = 25°C
V_{SWL}	Low Switch Drive Voltage (Off)			0.5	V	T_A = -55°C, +125°C
$R_{ON/channel}$	Channel On Resistance		120	200	Ω	I_{SW} = 0.4 mA, I_{in} = 1.0 mA, V_{out} = 0.0 V
I_{OFF}	Channel Off Leakage Current			1.0	nA	V_{SW} = 0.6 V
I_{OFF}	Channel Off Leakage Current			1.0	μA	V_{SW} = 0.5 V, T_A = +125°C
V_{IN}	Analog Peak Signal Input			±10	V	I_{IN} = 0, T_A = -55°C to +125°C
$-I_6$	Negative Supply Current		4.4	6.0	mA	I_{SW} = 0.4 mA, T_A = -55°C to +125°C
$C_{IN/channel}$	Channel Input Capacitance		3.5		pF	V_{SW} = 0.0 V V_{IN} = 0.0 V
C_{OUT}	Channel Output Capacitance		5.0		pF	V_{SW} = 0.0 V V_{OUT} = 0.0 V
t_{on}^+	Switch Turn-On Time		145	180	ns	See Figures 1 & 2
t_{on}^-	Switch Turn-On Time		230	280	ns	See Figures 1 & 3
t_{off}^+	Switch Turn-Off Time		580	600	ns	See Figures 1 & 2
t_{off}^-	Switch Turn-Off Time		270	300	ns	See Figures 1 & 3

TYPICAL ELECTRICAL CHARACTERISTICS

CHANNEL "ON" RESISTANCE VERSUS TEMPERATURE



CHANNEL "ON" RESISTANCE VERSUS V (IN OR OUT) MIN MINUS V_6



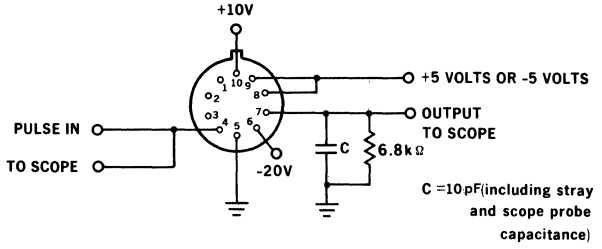


FIGURE 1

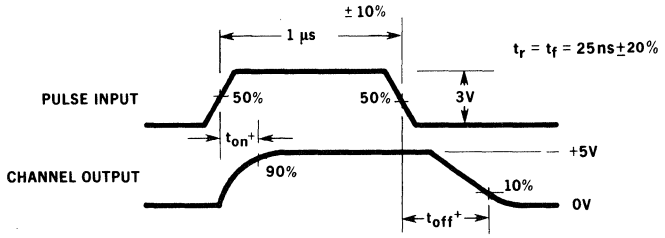


FIGURE 2

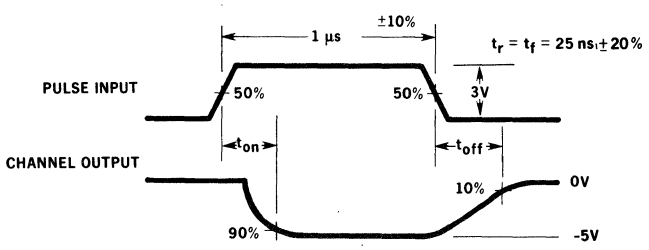


FIGURE 3

SH3002

SPDT ANALOG SWITCH

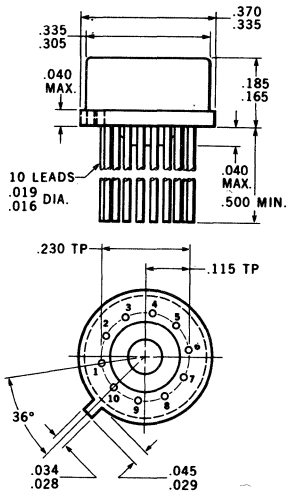
FAIRCHILD HYBRID CIRCUITS

- **INPUTS CCSL COMPATIBLE**
- **MW MICROLOGIC® AND MICROLOGIC® COMPATIBLE INPUTS**
- **LOW FEED THROUGH SPIKES ON THE OUTPUT**
- **TYPICAL t_{on} — 120 ns**
- **APPLICATIONS: SERIES SHUNT CHOPPERS, A/D CONVERSION SINGLE POLE DT RELAYS, MULTIPLEXING OR SCANNING**

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures	
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Maximum Power Dissipation	
at 25°C Case	500 mW
at 25°C Ambient	350 mW
Maximum Voltages and Current	
V_{in} (Pins 1, 2, 8 & 9)	±10 V
V_{out} (Pins 3 & 7)	±10 V
V^+ (Pin 10)	+11 V
V^- (Pin 6)	−22 V
I_{in}, I_{out}	100 mA
V_{switch} (Pin 4)	±6 V

PHYSICAL DIMENSIONS
(in accordance with JEDEC TO-100)



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

PART NO. HAG30021XX

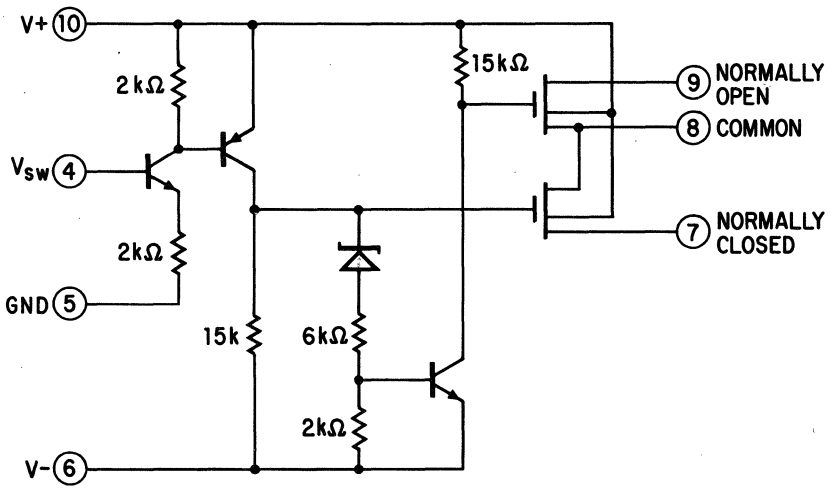


FIG. 1.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

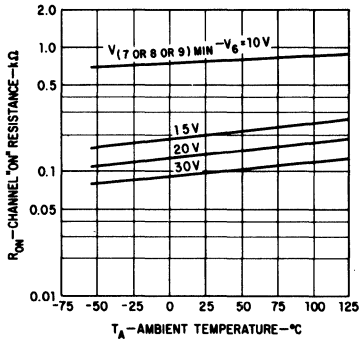
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 10\ V$, $V^- = -20\ V$ unless otherwise specified)

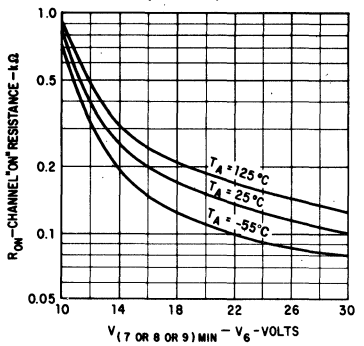
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{SWH}	High Switch Drive Voltage	2.5			V	$T_A = 25°C$, $T_A = 125°C$
V_{SWH}	High Switch Drive Voltage	2.6			V	$T_A = -55°C$
V_{SWL}	Low Switch Drive Voltage			0.8	V	$T_A = 125°C$
V_{SWL}	Low Switch Drive Voltage			1.1	V	$T_A = -55°C$, $T_A = 25°C$
$R_{ON}/_{channel}$	Channel "ON" Resistance		140	200	Ω	$I_{common} = 1.0\ mA$ V_7 or $V_9 = 0.0\ V$
I_{OFF}	Channel "OFF" Leakage Current			1.0	nA	$T_A = 25°C$
I_{OFF}	Channel "OFF" Leakage Current			1.0	μA	$T_A = 125°C$
V_{IN}	Analog Peak Signal Input			±10	V	$I_{CHNL} = 0$, $T_A = -55°C$ to $+125°C$
I_{10}	Positive Supply Current			8.0	mA	$V_{SWH} = 4.0\ V$, $T_A = -55°C$ to $+125°C$
C_{IN}/C_{HWL}	Channel Input Capacitance		3.5		pF	Channel Off, V_7 or $V_9 = 0.0\ V$
C_{OUT}	Channel Output Capacitance		5.0		pF	Channel Off, V_7 or $V_9 = 0.0\ V$
t_{on+}	Switch Turn-on Time (Pin 9)		120	150	ns	See Figures 2 and 3
t_{off+}	Switch Turn-off Time (Pin 7)		430	500	ns	See Figures 2 and 3
t_{on-}	Switch Turn-on Time (Pin 9)		130	160	ns	See Figures 2 and 4
t_{off-}	Switch Turn-off Time (Pin 7)		300	340	ns	See Figures 2 and 4
t_{off+}	Switch Turn-off Time (Pin 9)		1.6	1.9	μs	See Figures 2 and 3
t_{on+}	Switch Turn-on Time (Pin 7)		1.35	2.0	μs	See Figures 2 and 3
t_{off-}	Switch Turn-off Time (Pin 9)		1.5	1.7	μs	See Figures 2 and 4
t_{on-}	Switch Turn-on Time (Pin 7)		1.6	2.5	μs	See Figures 2 and 4

TYPICAL ELECTRICAL CHARACTERISTICS

CHANNEL "ON" RESISTANCE VERSUS TEMPERATURE



CHANNEL "ON" RESISTANCE VERSUS $V_{(7\ or\ 8\ or\ 9)}$ MIN MINUS V_6



SWITCHING TEST CIRCUIT

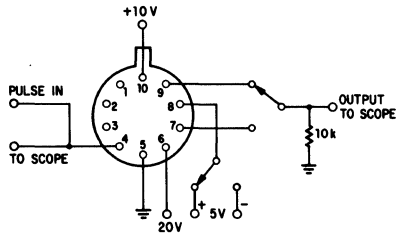
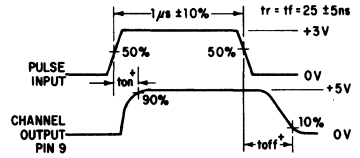


Fig. 2.



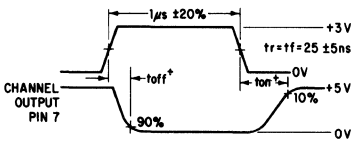
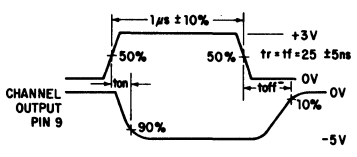


Fig. 3.



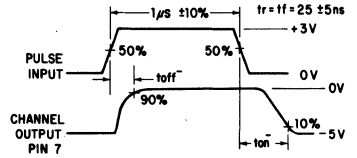


Fig. 4.

SH3005

HIGH IMPEDANCE DIFFERENTIAL COMPARATOR

FAIRCHILD HYBRID CIRCUITS

GENERAL DESCRIPTION - The SH 3005 consists of a pair of high current gain, matched transistors connected as emitter followers at the inputs of a μA 710 comparator.

FEATURES

- **2 MΩ INPUT IMPEDANCE**
- **0.8 μA INPUT BIAS CURRENT**
- **−55°C TO +125°C TEMPERATURE RANGE**

APPLICATIONS

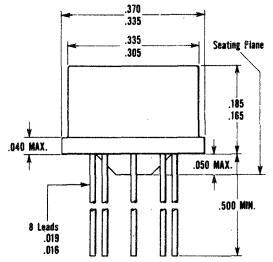
- Variable Threshold Schmitt Trigger
- Pulse Height Discriminator
- High Noise Immunity Line Receiver
- Memory Sense Amplifier

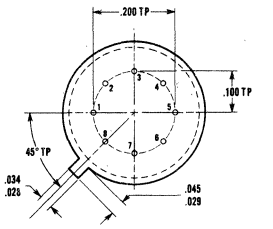
ABSOLUTE MAXIMUM RATINGS (Note 1)

Positive Supply Voltage	+14.0 Volts
Negative Supply Voltage	-7.0 Volts
Peak Output Current	10 mA
Differential Input Voltage	± 5.0 Volts
Input Voltage	± 7.0 Volts
Internal Power Dissipation	
TO-5 (Note 1)	300 mW
Flat Package (Note 2)	200 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

(TO-99)

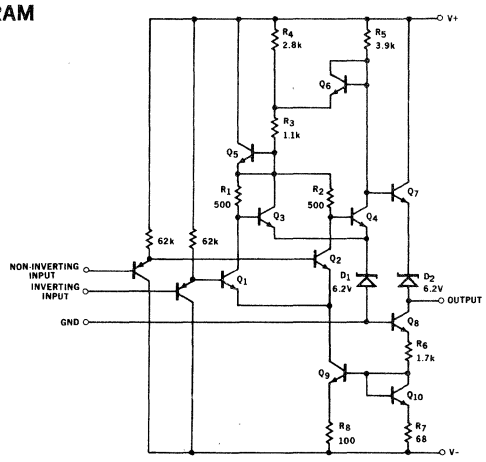




NOTES Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold plated kovar
Package weight is 1.22 grams

PART NO. HXK30051XX: -55°C TO +125°C
PART NO. HXK30059XX: 0°C TO +70°C

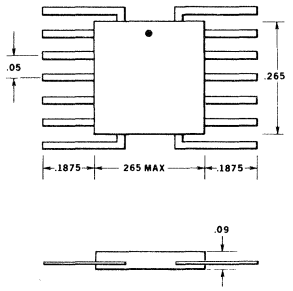
SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS

TYPICAL FLAT PACKAGE

TOP VIEW



PART NO. HBG30051XX: -55°C TO +125°C
PART NO. HBG30059XX: 0°C TO +70°C

Notes on page 2
Electrical Characteristics on page 2

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V Unless Otherwise Specified)

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq$ 20 k			7.0	mV
Input Offset Current	V_{out} = +1.4 V		0.3	0.4	μA
Input Bias Current			0.8	2.0	μA
Voltage Gain		750	1500		
Output Resistance			200		
Input Voltage Range	V^- = -7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Positive Output Level	$V_{in} \geq$ 15 mV, 0 $\leq I_o \leq$ 0.5 mA	+2.5	+3.2	+4.0	V
Negative Output Level	$V_{in} \geq$ 15 mV	-1.0	-0.5	0	V
Output Sink Current	$V_{in} \geq$ 15 mV, $V_{out} \geq$ 0	1.6	2.5		mA
Positive Supply Current	$V_{out} \leq$ 0		6.4		mA
Negative Supply Current			5.5		mA
Power Consumption					
TO-5 Package			110	175	mW
The following specifications apply for -55°C $\leq T_A \leq$ +125°C:					
Input Offset Voltage (Note 4)	$R_S \leq$ 20 k			8.5	mV
Input Offset Current (Note 4)				1.0	μA
Input Bias Current				5.0	μA
Temperature Coefficient of Input Offset Voltage (Note 4)			7.0		μV/°C
Voltage Gain		500			

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperature above +105°C.

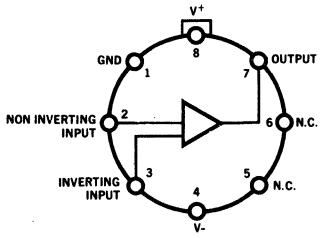
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1.0 V at +125°C.

TO–5 CONNECTION DIAGRAM

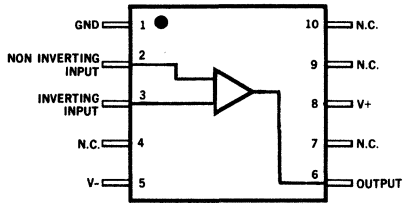
(TOP VIEW)



Note: Pin 4 connected to case

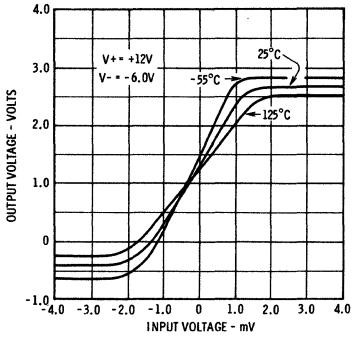
FLAT PACKAGE CONNECTION DIAGRAM

(TOP VIEW)

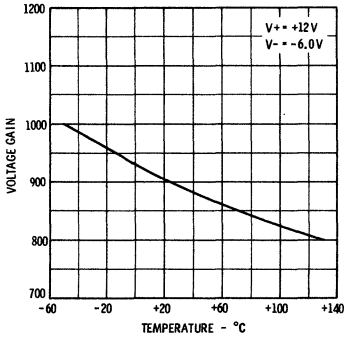


TYPICAL PERFORMANCE CURVES

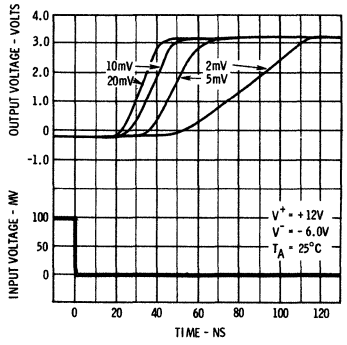
VOLTAGE TRANSFER CHARACTERISTIC



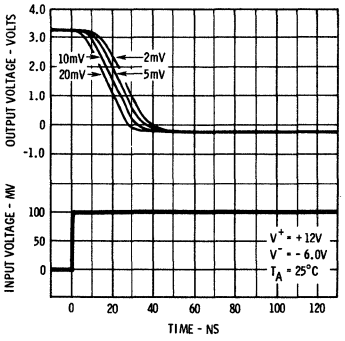
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



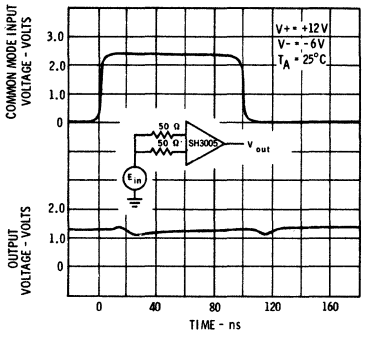
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



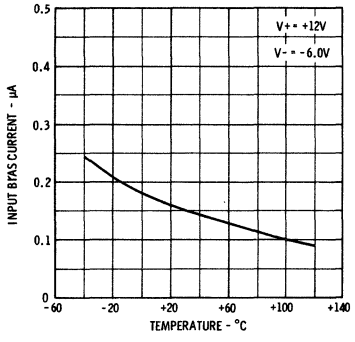
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



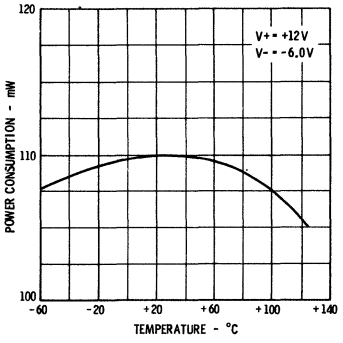
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents.

INPUT VOLTAGE RANGE* - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL* - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

SH3200

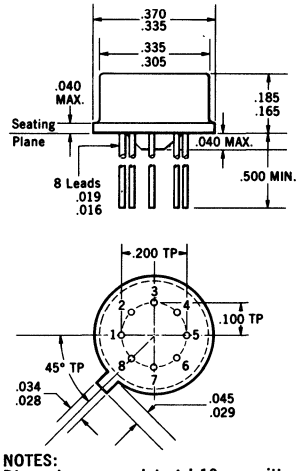
ADJUSTABLE POSITIVE DC VOLTAGE REGULATOR

FAIRCHILD HYBRID CIRCUIT

- **SHORT CIRCUIT PROTECTED**
- **BROAD RANGE OF OUTPUT VOLTAGES . . . 8.5 V TO 30 V**
- **LOAD CURRENTS 0 TO 50 mA AND 5.0 AMPS USING AN EXTERNAL PASS TRANSISTOR**
- **EXCELLENT REGULATION: LINE REGULATION . . . 0.005%/V MAX.**
  LOAD REGULATION . . . 0.05% MAX.
- **APPLICATIONS: SERIES REGULATOR FOR POSITIVE DC POWER SUPPLIES, DIGITAL AND ANALOG INTEGRATED CIRCUITS**
- **A COMPLEMENT SH3201 OF THIS REGULATOR IS ALSO AVAILABLE FOR NEGATIVE VOLTAGE REGULATION**

PHYSICAL DIMENSIONS

in accordance with JEDEC (TO-99) outline



NOTES:
Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.95 grams

PART NO. HXK32001XX

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures	
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Maximum Power Dissipation	
at 25°C Ambient Temperature (Note 1)	780 mW
at −55°C to +125°C Case Temperature	1.0 W
Maximum Voltages and Current	
Input Voltage	+35 V
Output Voltage (Note 2)	+28 V
Input-Output Voltage Differential	+28 V
Output Current (Note 3)	50 mA

SCHEMATIC DIAGRAM

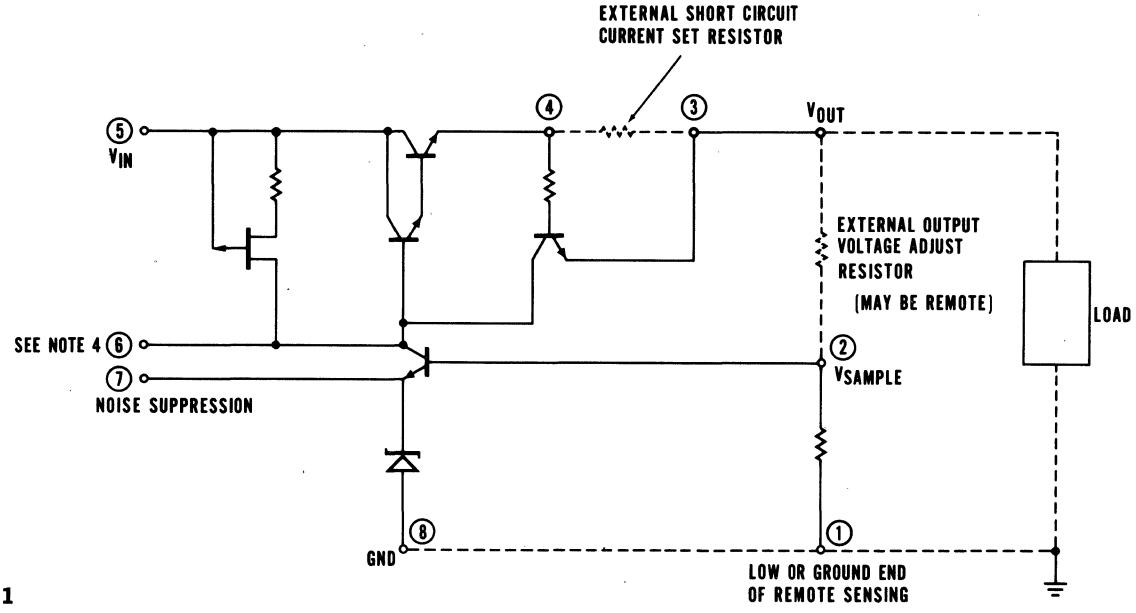


FIGURE 1

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{IN}	Input Voltage Range	12.5		35	Volts	
V_{OUT}	Output Voltage Range (Note 2)	8.5		30	Volts	$35\ V > \lvert V_{IN}\rvert > \lvert V_{OUT}\rvert + 4.0\ V$
$\lvert V_{IN}\text{-}V_{OUT}\rvert$	Input-Output Voltage Differential	4.0		28	Volts	
I_L	Load Current (Note 3)	0		50	mA	
$V_{(NOISE)}$	Uncompensated Output Noise Voltage		30	150	mVp.p.	$8.5\ V \leq \lvert V_{OUT}\rvert \leq 30\ V$ $0 \leq I_L \leq 50\ mA$
$V_{(NOISE)}$	Compensated Output Noise Voltage		3.0	5.0	mVp.p.	$C \geq 0.4\ \mu F$, Pin 7 to Pin 8 $8.5\ V \leq \lvert V_{OUT}\rvert \leq 30\ V$ $0 \leq I_L \leq 50\ mA$
$\frac{\lvert(\Delta V_{OUT}/V_{OUT})\%\rvert}{\Delta V_{IN}}$	Line Regulation		.002	.005	%/V	$35\ V > \lvert V_{IN}\rvert > \lvert V_{OUT}\rvert + 4.0\ V$
$\frac{\lvert(\Delta V_{OUT}/V_{OUT})\%\rvert}{I_L}$	Load Regulation (I_L = 0 to 50 mA)		.02	.05	%	$\lvert V_{IN}\rvert > \lvert V_{OUT}\rvert + 4.0\ V$
$\frac{\lvert(\Delta V_{OUT}/V_{OUT})\%\rvert}{\Delta T}$	Temperature Stability $T_A = -55°C$ to $+125°C$			.01	%/°C	At Package Dissipation $\leq$ 780 mW
$\frac{\lvert(\Delta V_{OUT}/V_{OUT})\%\rvert}{P_D}$	Power Dissipation Stability			.002	%/mW	$4.0\ V \leq \lvert V_{IN} - V_{OUT}\rvert \leq 28\ V$ $0 \leq I_L \leq 50\ mA$

TYPICAL REGULATED OUTPUT VOLTAGE ADJUSTMENT

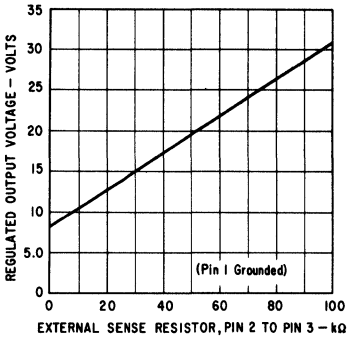


FIGURE 2

TYPICAL SHORT CIRCUIT PROTECTION SETTING CURRENT

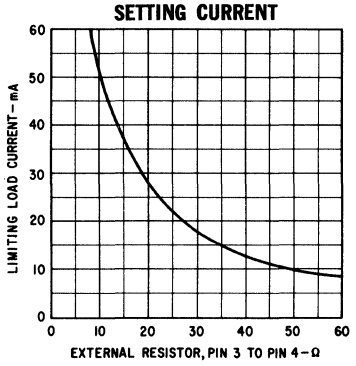


FIGURE 3

MAXIMUM POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

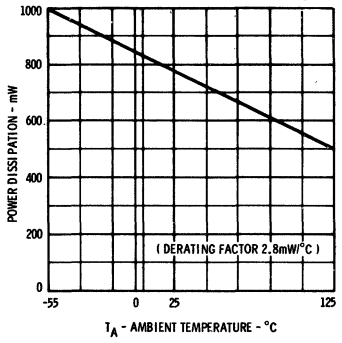


FIGURE 4

NOTES:

(1) Derating factor as shown in Fig. 4 is 2.8 mW/°C.

(2) Selection of Output Voltages: By externally connecting a preselected sense resistor (see figure 2) between pin 2 and pin 3 any desired output voltage in the range of 8.5 V to 30 V is achieved.

(3) Selection of Short Circuit Current: The maximum limit on the internal short circuit protection at any current from 1 to 50 mA can be set by externally connecting a preselected resistor (see figure 3) between pin 3 and pin 4.

(4) This pin is made available for connections to compensating networks which can be used to alter the dynamic response of the regulator to meet unusual load requirements. No connection is necessary for normal operation.

SH3201

ADJUSTABLE NEGATIVE DC VOLTAGE REGULATOR

FAIRCHILD HYBRID CIRCUIT

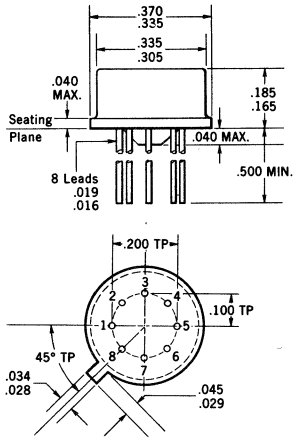
- **SHORT CIRCUIT PROTECTED**
- **BROAD RANGE OF OUTPUT VOLTAGES . . . —8.5 V TO —30 V**
- **LOAD CURRENTS 0 TO 50 mA AND 5.0 AMPS USING AN EXTERNAL PASS TRANSISTOR**
- **EXCELLENT REGULATION: LINE REGULATION . . . 0.005%/V MAX.**
  LOAD REGULATION . . . 0.05% MAX.
- **APPLICATIONS: SERIES REGULATOR FOR NEGATIVE DC POWER SUPPLIES, DIGITAL AND ANALOG INTEGRATED CIRCUITS**
- **A COMPLEMENT SH3200 OF THIS REGULATOR IS ALSO AVAILABLE FOR POSITIVE VOLTAGE REGULATION**

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures	
Storage Temperature	—65°C to +150°C
Operating Temperature	—55°C to +125°C
Maximum Power Dissipation	
at 25°C Free Air Temperature (Note 1)	780 mW
at —55°C to +125°C Case Temperature	1.0 W
Maximum Voltages and Current	
Input Voltage	—35 V
Output Voltage (Note 2)	—28 V
Input-Output Voltage Differential	28 V
Output Current (Note 3)	50 mA

PHYSICAL DIMENSIONS

in accordance with JEDEC (TO-99) outline



NOTES:
Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.95 grams

PART NO. HXK32011XX

SCHEMATIC DIAGRAM

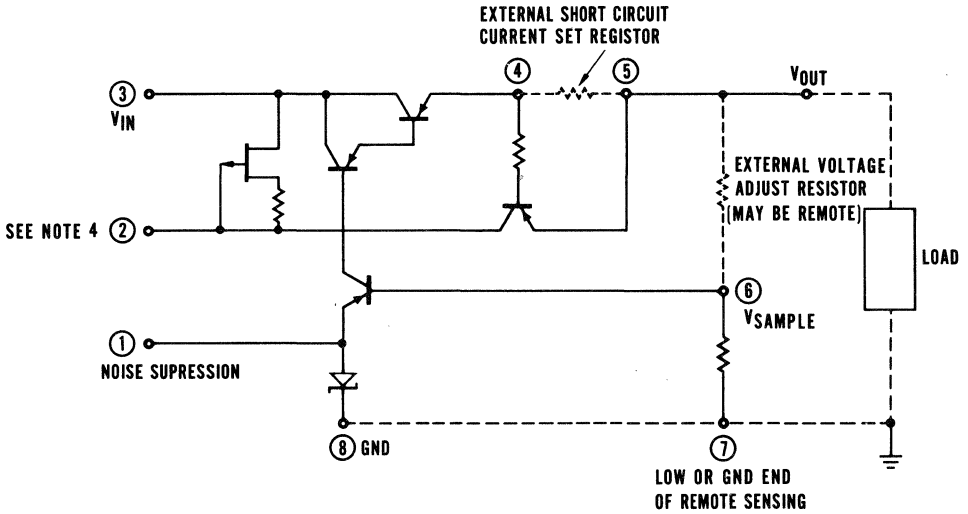


FIGURE 1

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{IN}	Input Voltage Range	−12.5		−35	Volts	
V_{OUT}	Output Voltage Range (Note 2)	−8.5		−30	Volts	$35\ V > \lvert V_{IN}\rvert > \lvert V_{OUT}\rvert + 4.0\ V$
$\lvert V_{IN}\text{-}V_{OUT}\rvert$	Input-Output Voltage Differential	4.0		28	Volts	
I_L	Load Current (Note 3)	0		50	mA	
$V_{(NOISE)}$	Uncompensated Output Noise Voltage		30	150	mVp.p.	$8.5\ V \leq \lvert V_{OUT}\rvert \leq 30\ V$ $0 \leq I_L \leq 50\ mA$
$V_{(NOISE)}$	Compensated Output Noise Voltage		3.0	5.0	mVp.p.	$C \geq 0.4\ \mu F$, Pin 1 to Pin 8 $8.5\ V \leq \lvert V_{OUT}\rvert \leq 30\ V$ $0 \leq I_L \leq 50\ mA$
$\frac{\lvert(\Delta V_{OUT}/V_{OUT})\%\rvert}{\Delta V_{IN}}$	Line Regulation		.002	.005	%/V	$35\ V > \lvert V_{IN}\rvert > \lvert V_{OUT}\rvert + 4.0\ V$
$\frac{\lvert(\Delta V_{OUT}/V_{OUT})\%\rvert}{I_L}$	Load Regulation (I_L = 0 to 50 mA)		.02	.05	%	$\lvert V_{IN}\rvert > \lvert V_{OUT}\rvert + 4.0\ V$
$\frac{\lvert(\Delta V_{OUT}/V_{OUT})\%\rvert}{\Delta T}$	Temperature Stability $T_A = -55°C$ to $+125°C$			.01	%/°C	At Package Power Dissipation ≤ 780 mW
$\frac{\lvert(\Delta V_{OUT}/V_{OUT})\%\rvert}{P_D}$	Power Dissipation Stability			.002	%/mW	$4.0\ V \leq \lvert V_{IN} - V_{OUT}\rvert \leq 28\ V$ $0 \leq I_L \leq 50\ mA$

TYPICAL REGULATED OUTPUT VOLTAGE ADJUSTMENT

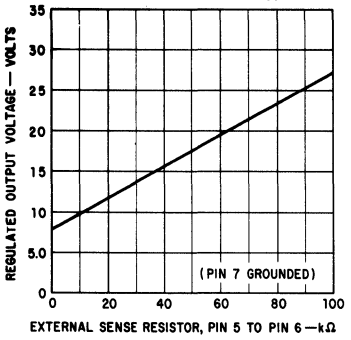


FIGURE 2

TYPICAL SHORT CIRCUIT PROTECTION SETTING CURRENT

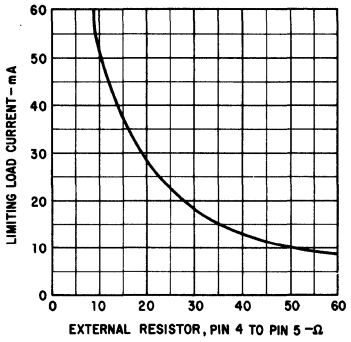


FIGURE 3

MAXIMUM POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

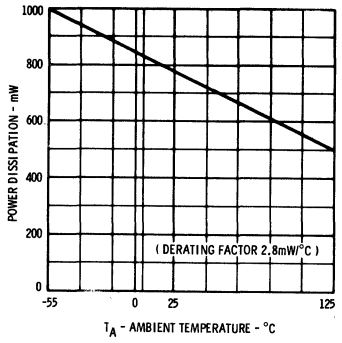


FIGURE 4

NOTES:

(1) Derating factor as shown in Fig. 4 is 2.8 mW/°C.

(2) Selection of Output Voltages: By externally connecting a preselected sense resistor (see figure 2) between pin 5 and pin 6 any desired output voltage in the range of 8.5 V to 30 V is achieved.

(3) Selection of Short Circuit Current: The maximum limit on the internal short circuit protection at any current from 1 to 50 mA can be set by externally connecting a preselected resistor (see figure 3) between pin 4 and pin 5.

(4) This pin is made available for connections to compensating networks which can be used to alter the dynamic response of the regulator to meet unusual load requirements. No connection is necessary for normal operation.

SH3741

DUAL HIGH GAIN OPERATIONAL AMPLIFIER

A FAIRCHILD HYBRID DESIGN SPECIFICATION CIRCUIT

GENERAL DESCRIPTION — The SH3741 is a dual high performance operational amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the SH3741 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier and general feedback applications. The SH3741 is short-circuit protected, is similar to the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/ octave roll-off insures stability in closed loop applications.

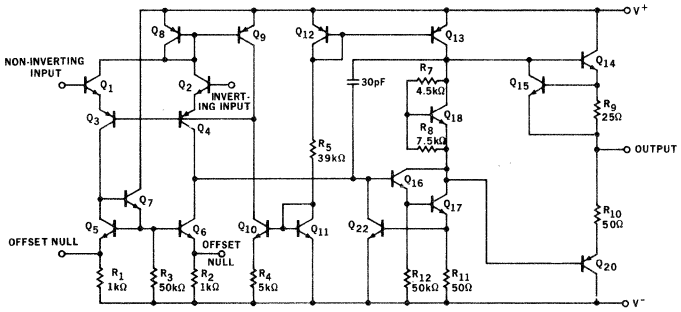
FEATURES

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

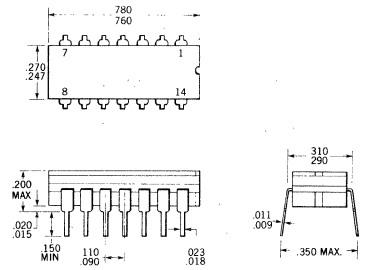
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

	CERAMIC DIP	PLASTIC DIP
Supply Voltage	±22 V	±18 V
Internal Power Dissipation, $T_A = 25°C$	780 mW	600 mW
Differential Input Voltage	±30 V	±30 V
Input Voltage (Note 1)	±15 V	±15 V
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Lead Temperature (Soldering, 60 second)	300°C	300°C
Output Short-Circuit Duration (Note 2)	Indefinite	Indefinite

SCHEMATIC DIAGRAM (EACH AMPLIFIER)

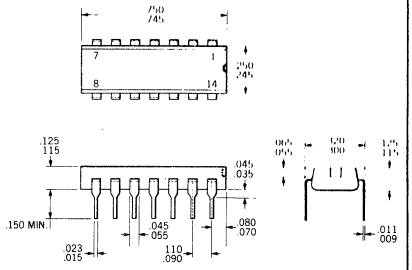


PHYSICAL DIMENSIONS
CERAMIC DUAL IN-LINE



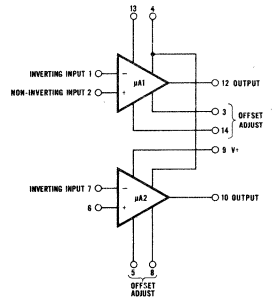
ORDER PART NO. H6K37411XX

PHYSICAL DIMENSIONS
PLASTIC DUAL IN-LINE



ORDER PART NO. H6Q37419XX

PIN CONFIGURATION



NOTES:
(1) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(2) Short circuit may be to ground or either supply.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

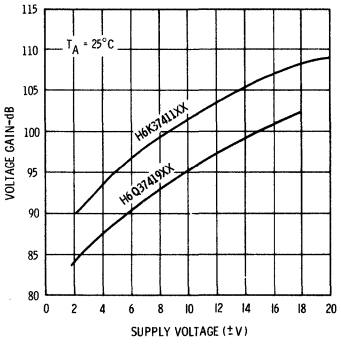
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified) (EACH SIDE)

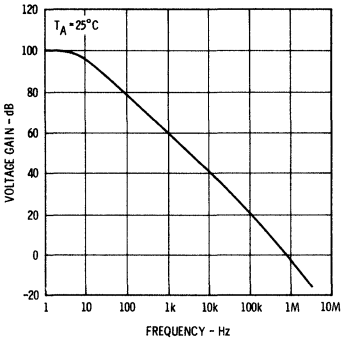
PARAMETER	CONDITIONS	H6K37411XX MIN.	H6K37411XX TYP.	H6K37411XX MAX.	H6Q37419XX MIN.	H6Q37419XX TYP.	H6Q37419XX MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	7.0		3.0	8.0	mV
Input Offset Current			35	375		35	375	nA
Input Bias Current			0.15	1.0		0.15	1.0	μA
Input Resistance		300	800		300	800		kΩ
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	50,000	200,000		20,000	100,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±11	±13		±11	±13		V
	$R_L \geq 2$ kΩ	±9.0	±12		±9.0	±12		V
Input Voltage Range		±11	±12		±11	±12		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	80	100		80	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Power Consumption			50	100		50	100	mW
Transient Response (unity gain)	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		0.5			0.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:								
Input Offset Voltage	$R_S \leq 10$ kΩ			8.5				mV
Input Offset Current				950				nA
Input Bias Current				3.0				μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	25,000						
Output Voltage Swing	$R_L \geq 2$ kΩ	±10						V
The following specifications apply for $0°C \leq T_A \leq +70°C$:								
Input Offset Voltage	$R_S \leq 10$ kΩ						9.5	mV
Input Offset Current							475	nA
Input Bias Current							1.5	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V				15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ				±10			V

TYPICAL PERFORMANCE CURVES

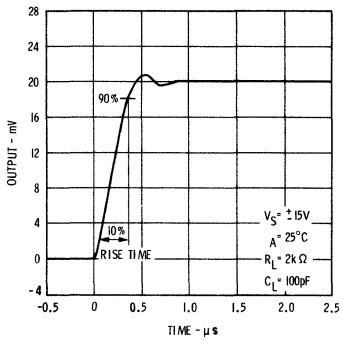
OPEN LOOP VOLTAGE GAIN



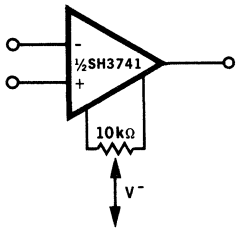
OPEN LOOP FREQUENCY RESPONSE



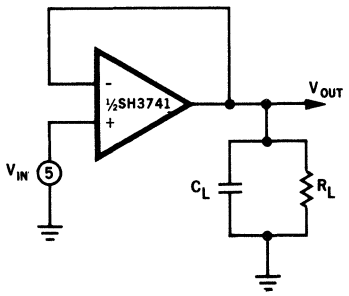
TRANSIENT RESPONSE



VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



SH6400 • SH6401 • SH6402

PNP QUAD CORE DRIVERS

FAIRCHILD HYBRID CIRCUITS

FEATURES

- **HIGH VOLTAGE . . . . . UP TO 50 VOLT LV_{CEO}**
- **HIGH CURRENT . . . . . UP TO 1.0 AMP**
- **FAST SWITCHING . . . . . 25 ns (TYP) t_{on}**
  65 ns (TYP) t_{off}
- **COMPACT PACKAGING . . . 4 TRANSISTORS PER PACKAGE**

ABSOLUTE MAXIMUM RATINGS (Note 1)

	FLAT PACK & CERAMIC DIP	PLASTIC DIP
Maximum Temperature		
Storage Temperature	−65°C to +200°C	−65°C to +150°C
Operating Temperature	−55°C to +125°C	0°C to +70°C
Operating Junction Temperature	+200°C	+150°C
Lead Temperature (Soldering, 60 second time limit)	+300°C	+300°C

Maximum Power Dissipation (Notes 2 & 3)	**FLAT PACK**	**CERAMIC DIP**	**PLASTIC DIP**
25°C Case Temperature	1.2 Watts	1.5 Watts	1.5 Watts
25°C Ambient Temperature	0.5 Watt	0.8 Watt	0.6 Watt

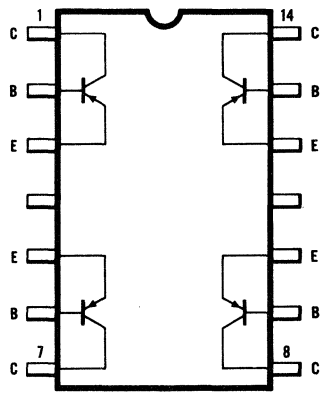
ORDER INFORMATION

Specify HBHXXXX1XX, 9XX for 14-pin Flat Pak
H6A*XXXX1XX, 9XX for 14-pin Ceramic DIP
H6E*XXXX9XX for 14-pin Plastic DIP

Where first XXXX is the four-digit number denoting the specific element desired, 1XX is for −55°C to 125°C and 9XX is for 0°C to 70°C.

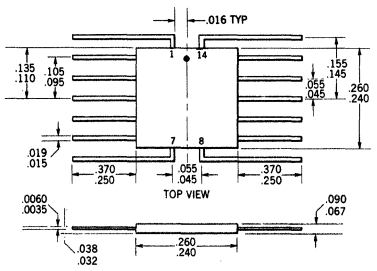
NOTE: The packages 6A* and 6E* are similar to 6A and 6E. For ordering, the asterisk must be included.

CONNECTION DIAGRAM

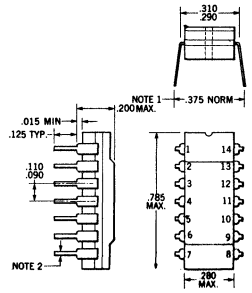


PHYSICAL DIMENSIONS

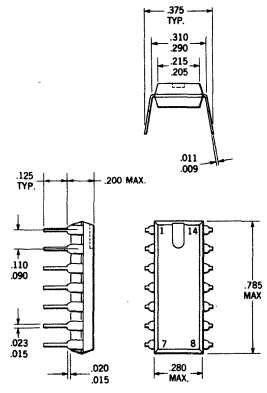
FLAT PAK



CERAMIC DIP



PLASTIC DIP



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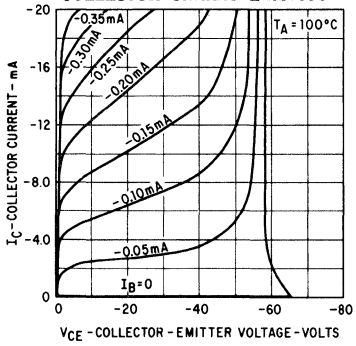
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	SH6400 MIN.	SH6400 TYP.	SH6400 MAX.	SH6401 MIN.	SH6401 TYP.	SH6401 MAX.	SH6402 MIN.	SH6402 TYP.	SH6402 MAX.	UNITS	TEST CONDITIONS
$V_{CEO(sus)}$	Collector to Emitter Sustaining Voltage (Note 4)	−50			−40			−20			Volts	$I_C = 10$ mA $I_B = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	−50			−40			−20			Volts	$I_C = 10\ \mu A$ $I_E = 0$
BV_{CES}	Collector to Base Breakdown Voltage	−50			−40			−20			Volts	$I_C = 10\ \mu A$ $V_{BE} = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			−5.0			−5.0			Volts	$I_E = 10\ \mu A$ $I_C = 0$
I_{CES}	Collector Reverse Current		0.01	1.0							μA	$V_{CE} = -30$ V $V_{BE} = 0$
I_{CES}	Collector Reverse Current					0.01	1.0				μA	$V_{CE} = -25$ V $V_{BE} = 0$
I_{CES}	Collector Reverse Current								0.01	5.0	μA	$V_{CE} = -15$ V $V_{BE} = 0$
I_{CBO}	Collector Cutoff Current		0.01	1.0							μA	$V_{CB} = -30$ V $I_E = 0$
I_{CBO}	Collector Cutoff Current					0.01	1.0				μA	$V_{CB} = -25$ V $I_E = 0$
I_{CBO}	Collector Cutoff Current								0.01	10	μA	$V_{CB} = -15$ V $I_E = 0$
$I_{CBO}(100°C)$	Collector Cutoff Current		0.5	120							μA	$V_{CB} = -30$ V $I_E = 0$
$I_{CBO}(100°C)$	Collector Cutoff Current					0.5	120				μA	$V_{CB} = -25$ V $I_E = 0$
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)		−0.7	−0.8		−0.7	−0.8		−0.7	−0.9	Volt	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)		−0.8	−0.9		−0.8	−0.9		−0.8	−1.0	Volt	$I_C = 100$ mA $I_B = 10$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)	−0.6	−1.0	−1.2	−0.6	−1.0	−1.2		−1.0	−1.5	Volts	$I_C = 500$ mA $I_B = 50$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)		−1.1	−1.7		−1.1	−1.7				Volts	$I_C = 1000$ mA $I_B = 100$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		−0.1	−0.25		−0.1	−0.25		−0.1	−0.3	Volt	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		−0.1	−0.3		−0.1	−0.25		−0.1	−0.3	Volt	$I_C = 100$ mA $I_B = 10$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		−0.3	−0.55		−0.3	−0.5		−0.3	−0.6	Volt	$I_C = 500$ mA $I_B = 50$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		−0.5	−1.0		−0.5	−0.9				Volt	$I_C = 1000$ mA $I_B = 100$ mA
$V_{CE(sat)}(-55°C)$	Pulsed Collector Saturation Voltage (Note 4)			−0.25			−0.25				Volt	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{CE(sat)}(-55°C)$	Pulsed Collector Saturation Voltage (Note 4)			−0.55			−0.5				Volt	$I_C = 500$ mA $I_B = 50$ mA
$V_{CE(sat)}(100°C)$	Pulsed Collector Saturation Voltage (Note 4)			−0.3			−0.3				Volt	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{CE(sat)}(100°C)$	Pulsed Collector Saturation Voltage (Note 4)			−0.65			−0.6				Volt	$I_C = 500$ mA $I_B = 50$ mA
h_{FE}	DC Pulse Current Gain (Note 4)	20	50		20	50		15	50			$I_C = 10$ mA $V_{CE} = -1.0$ V
h_{FE}	DC Pulse Current Gain (Note 4)	50	75		50	75		25	75			$I_C = 100$ mA $V_{CE} = -1.0$ V
h_{FE}	DC Pulse Current Gain (Note 4)	20	70		30	70		10	70			$I_C = 500$ mA $V_{CE} = -1.0$ V
h_{FE}	DC Pulse Current Gain (Note 4)	10	30		15	30						$I_C = 1000$ mA $V_{CE} = -1.0$ V
h_{fe}	High Frequency Current Gain (f = 100 MHz)	1.7	2.8		2.0	2.8		1.5	2.8			$I_C = 50$ mA $V_{CE} = -10$ V
t_{on}	Turn On Time (Note 5)		25	40		25	40		25	50	ns	$I_C \approx 500$ mA $I_{B1} \approx 50$ mA
t_{off}	Turn Off Time (Note 5)		65	90		65	90		65	100	ns	$I_C \approx 500$ mA $I_{B1} \approx -I_{B2} \approx 50$ mA
t_s	Storage Time (Note 5)		50	60		50	60		50	75	ns	$I_C \approx 500$ mA $I_{B1} \approx -I_{B2} \approx 50$ mA
C_{cb}	Collector to Base Capacitance (f = 1.0 MHz)		15	25		15	25		20	25	pF	$V_{CB} = -10$ V $I_E = 0$
C_{eb}	Emitter to Base Capacitance (f = 1.0 MHz)		80	100		80	100		80	100	pF	$V_{EB} = -0.5$ V $I_C = 0$

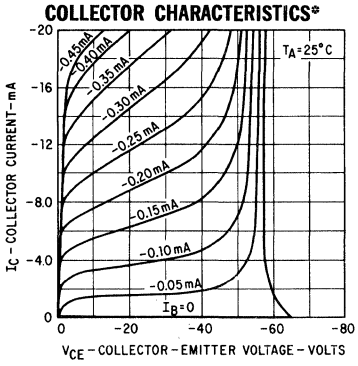
TYPICAL ELECTRICAL CHARACTERISTICS

SH6400

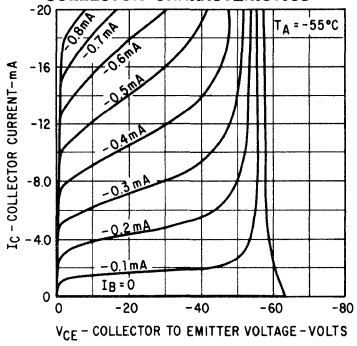
COLLECTOR CHARACTERISTICS*



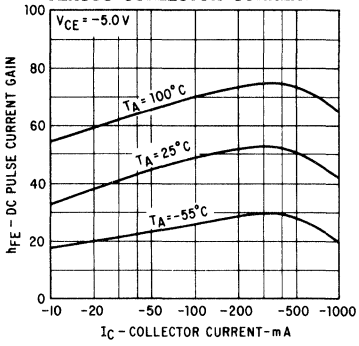
COLLECTOR CHARACTERISTICS*



COLLECTOR CHARACTERISTICS*



DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT



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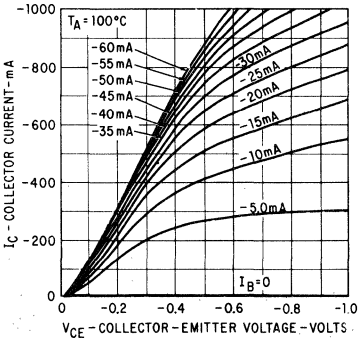

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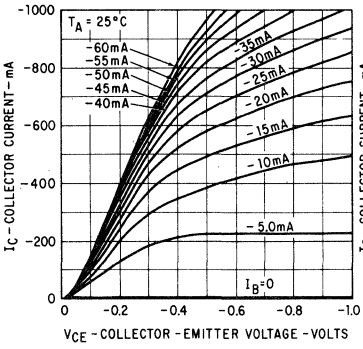
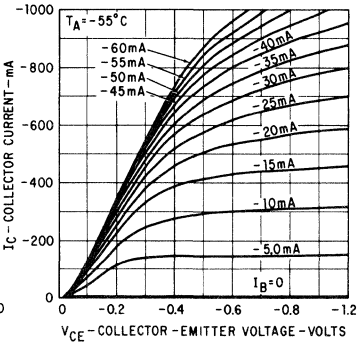
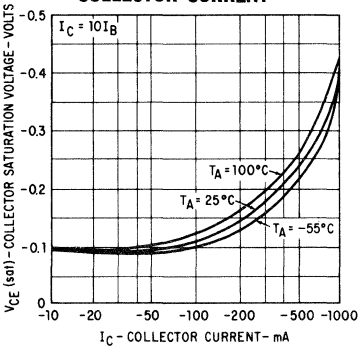


COLLECTOR CHARACTERISTICS*



COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT

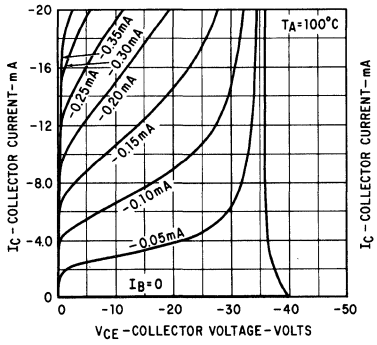


*Single family characteristic on Transistor Curve Tracer.

TYPICAL ELECTRICAL CHARACTERISTICS

SH6401 • SH6402

COLLECTOR CHARACTERISTICS*



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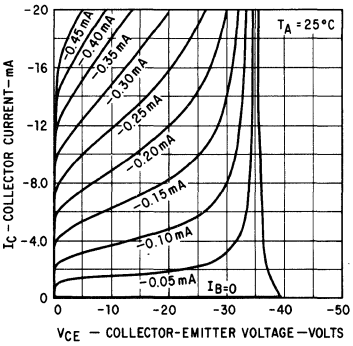

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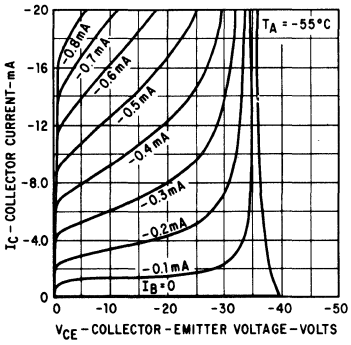
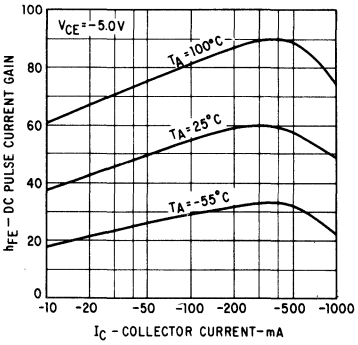


DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT



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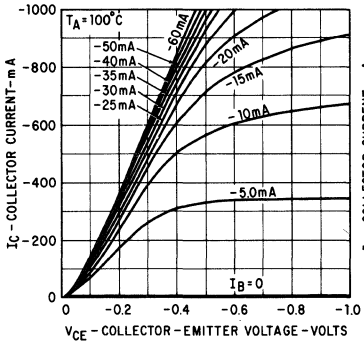

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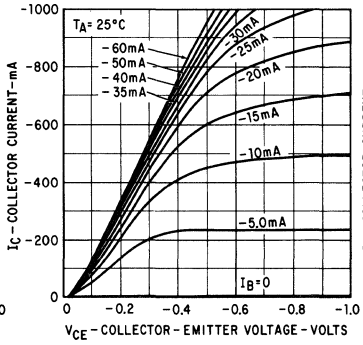
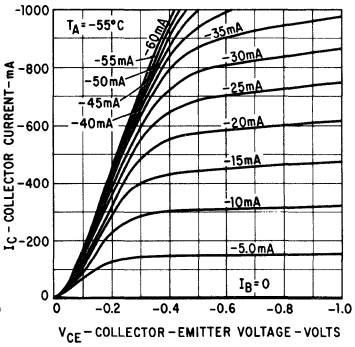
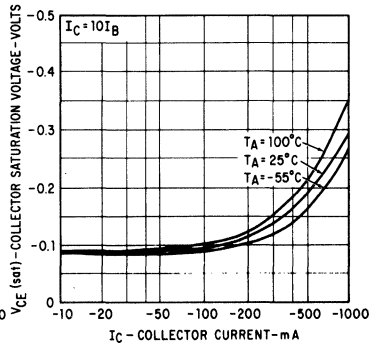


COLLECTOR CHARACTERISTICS*



COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



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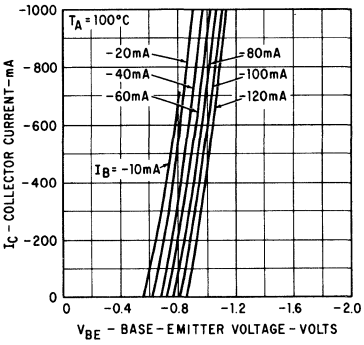
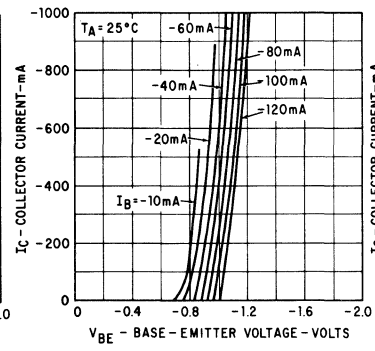
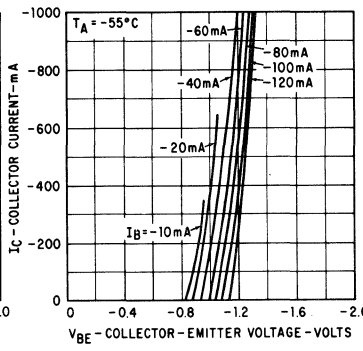
BASE CHARACTERISTIC*



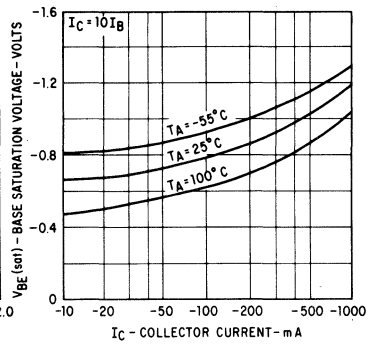
BASE CHARACTERISTIC*



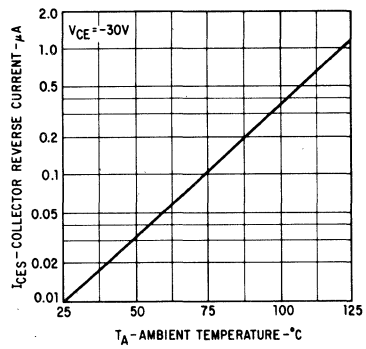
BASE CHARACTERISTIC*



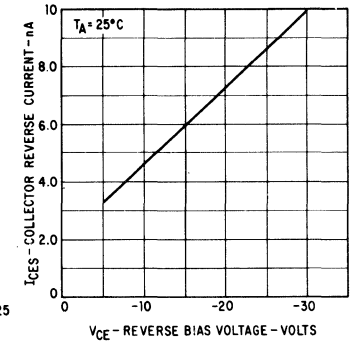
BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



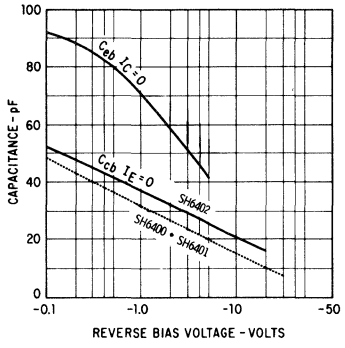
COLLECTOR REVERSE CURRENT VERSUS AMBIENT TEMPERATURE



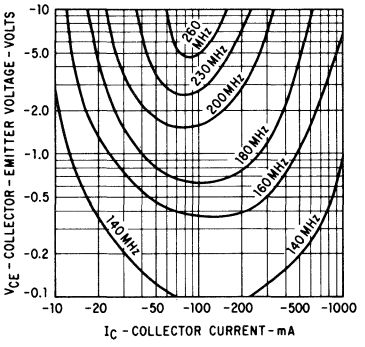
COLLECTOR REVERSE CURRENT VERSUS REVERSE BIAS VOLTAGE



INPUT AND OUTPUT CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



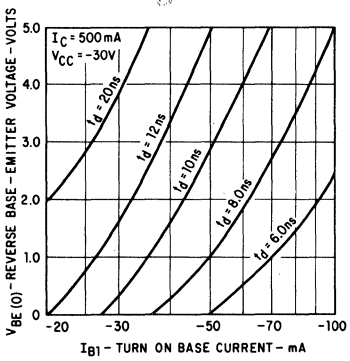
CONTOURS OF CONSTANT BANDWIDTH PRODUCT (f_T)



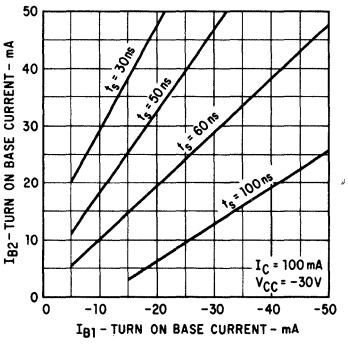
*Single family characteristic on Transistor Curve Tracer.

TYPICAL SWITCHING CHARACTERISTICS

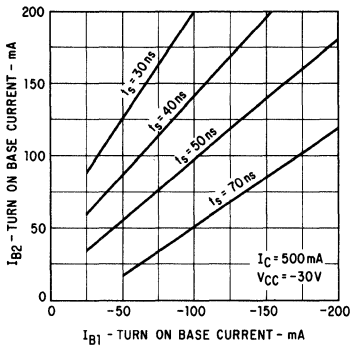
DELAY TIME VERSUS TURN ON BASE CURRENT AND REVERSE BASE EMITTER VOLTAGE



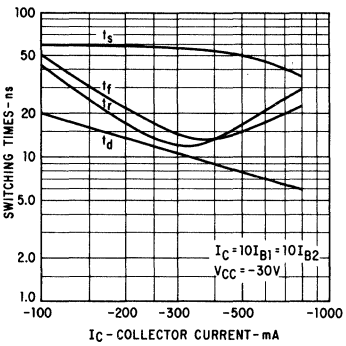
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



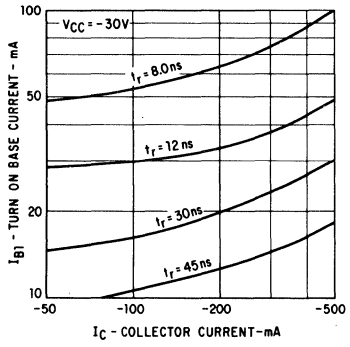
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



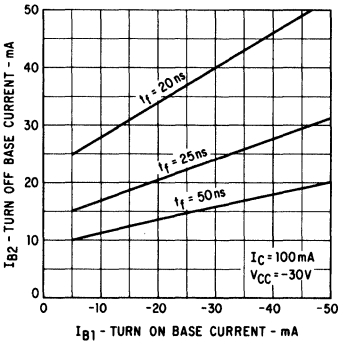
SWITCHING TIMES VERSUS COLLECTOR CURRENT



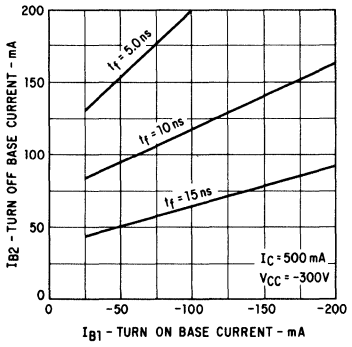
RISE TIME VERSUS COLLECTOR CURRENT AND TURN ON BASE CURRENTS



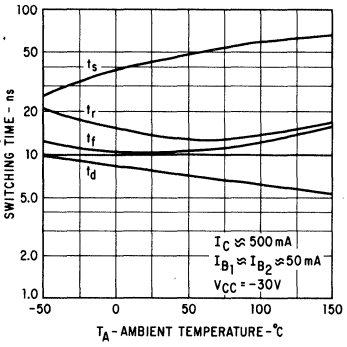
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



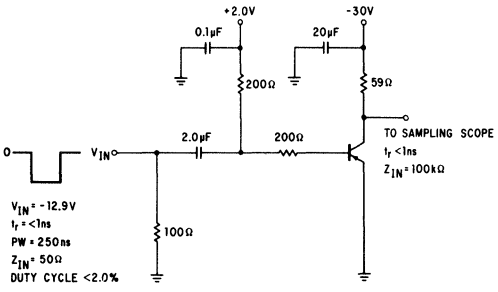
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



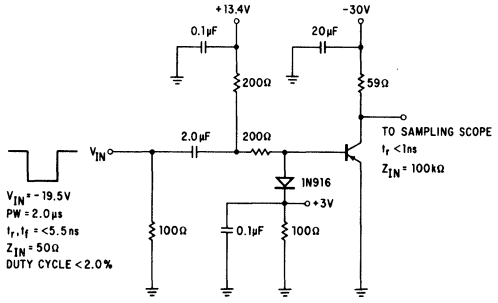
SWITCHING TIMES VERSUS AMBIENT TEMPERATURE



TURN ON CIRCUIT



TURN OFF CIRCUIT



NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction to case thermal resistance of ~135°C/Watt (derating factor of ~7.4 mW/°C) for the Flat package and Ceramic Dual In-Line package. Maximum junction temperature of 150°C and junction to case thermal resistance of ~83°C/Watt (derating factor of ~12 mw/°C) for the Plastic Dual In-Line package.

(4) Pulse Conditions: length = 300 μs; duty cycle = 1%.

(5) See switching circuit for exact value of I_C, I_{B1}, and I_{B2}.

SH6500 • SH6501 • SH6502

NPN QUAD CORE DRIVERS

FAIRCHILD HYBRID CIRCUITS

FEATURES

- **HIGH VOLTAGE . . . . . UP TO 50 VOLT LV_{CEO}**
- **HIGH CURRENT . . . . . UP TO 1 AMP**
- **FAST SWITCHING . . . . . 25 ns t_{on} (TYP)**
  45 ns t_{off} (TYP)
- **COMPACT PACKAGING . . . 4 TRANSISTORS PER PACKAGE**

ABSOLUTE MAXIMUM RATINGS (Note 1)

	FLAT PACK CERAMIC DIP	PLASTIC DIP
Maximum Temperature		
Storage Temperature	−65°C to +200°C	−65°C to +150°C
Operating Temperature	−55°C to +125°C	0°C to +70°C
Operating Junction Temperature	+200°C	+150°C
Lead Temperature (Soldering, 60 second time limit)	+300°C	+300°C

	FLAT PACK	CERAMIC DIP	PLASTIC DIP
Maximum Power Dissipation (Notes 2 & 3)			
Total Dissipation at 25°C Case Temperature	1.2 Watts	1.5 Watts	1.5 Watts
at 25°C Ambient Temperature	0.5 Watt	0.8 Watt	0.6 Watt

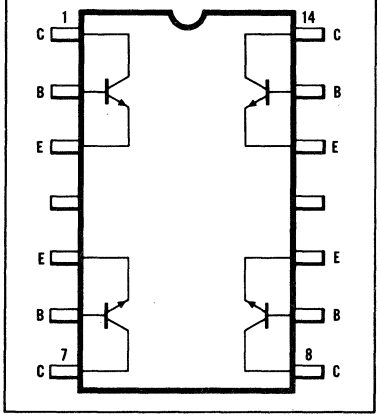
ORDER INFORMATION

Specify HBHXXXX1XX, 9XX for 14-pin Flat Pak
H6A*XXXX1XX, 9XX for 14-pin Ceramic DIP
H6E*XXXX9XX for 14-pin Plastic DIP

Where first XXXX is the four-digit number denoting the specific element desired, 1XX is for −55°C to 125°C and 9XX is for 0°C to 70°C.

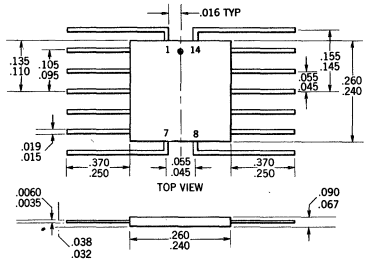
NOTE: The packages 6A* and 6E* are similar to 6A and 6E. For ordering, the asterisk must be included.

CONNECTION DIAGRAM

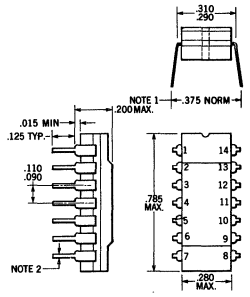


PHYSICAL DIMENSIONS

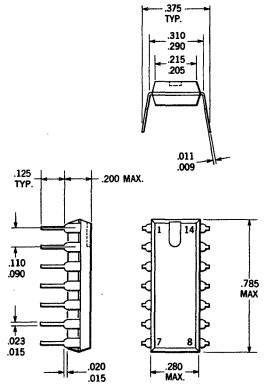
FLAT PACK



CERAMIC DIP



PLASTIC DIP



FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

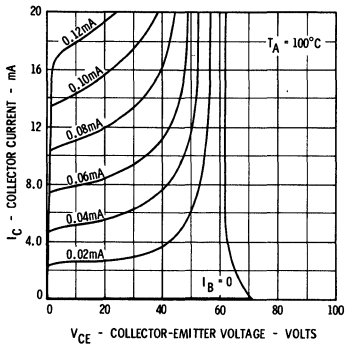
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	SH6500 MIN.	SH6500 TYP.	SH6500 MAX.	UNITS	TEST CONDITIONS	
$V_{CEO(sus)}$	Collector to Emitter Sustaining Voltage (Note 4)	50			Volts	$I_C = 10$ mA	$I_B = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	80			Volts	$I_C = 10\ \mu$A	$I_E = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	80			Volts	$I_C = 10\ \mu$A	$I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			Volts	$I_E = 10\ \mu$A	$I_C = 0$
I_{CES}	Collector Cutoff Current		0.1	1.7	μA	$V_{CE} = 40$ V	$V_{BE} = 0$
I_{CBO}	Collector Cutoff Current		0.1	1.7	μA	$V_{CB} = 40$ V	$I_E = 0$
$I_{CBO}(100°C)$	Collector Cutoff Current		5.0	120	μA	$V_{CB} = 40$ V	$I_E = 0$
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)		0.7	0.8	Volt	$I_C = 10$ mA	$I_B = 1.0$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)		0.8	0.9	Volt	$I_C = 100$ mA	$I_B = 10$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)	0.9	0.95	1.2	Volts	$I_C = 500$ mA	$I_B = 50$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)		1.1	1.7	Volts	$I_C = 1000$ mA	$I_B = 100$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		0.15	0.25	Volt	$I_C = 10$ mA	$I_B = 1.0$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		0.16	0.3	Volt	$I_C = 100$ mA	$I_B = 10$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		0.3	0.55	Volt	$I_C = 500$ mA	$I_B = 50$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		0.5	1.0	Volt	$I_C = 1000$ mA	$I_B = 100$ mA
$V_{CE(sat)}(-55°C)$	Pulsed Collector Saturation Voltage (Note 4)			0.25	Volt	$I_C = 10$ mA	$I_B = 1.0$ mA
$V_{CE(sat)}(-55°C)$	Pulsed Collector Saturation Voltage (Note 4)			0.55	Volt	$I_C = 500$ mA	$I_B = 50$ mA
$V_{CE(sat)}(100°C)$	Pulsed Collector Saturation Voltage (Note 4)			0.3	Volt	$I_C = 10$ mA	$I_B = 1.0$ mA
$V_{CE(sat)}(100°C)$	Pulsed Collector Saturation Voltage (Note 4)			0.65	Volt	$I_C = 500$ mA	$I_B = 50$ mA
h_{FE}	DC Pulse Current Gain (Note 4)	20	65			$I_C = 10$ mA	$V_{CE} = 1.0$ V
h_{FE}	DC Pulse Current Gain (Note 4)	50	90			$I_C = 100$ mA	$V_{CE} = 1.0$ V
h_{FE}	DC Pulse Current Gain (Note 4)	20	50			$I_C = 500$ mA	$V_{CE} = 1.0$ V
h_{FE}	DC Pulse Current Gain (Note 4)	10	20			$I_C = 1000$ mA	$V_{CE} = 1.0$ V
h_{fe}	High Frequency Current Gain (f = 100 MHz)	2.5	4.5			$I_C = 50$ mA	$V_{CE} = 10$ V
t_{on}	Turn On Time		25	35	ns	$I_C = 500$ mA	$I_{B1} = 50$ mA
t_{off}	Turn Off Time		45	60	ns	$I_C = 500$ mA, $I_{B1} = -I_{B2} = 50$ mA	
t_s	Storage Time		35	50	ns	$I_C = 500$ mA, $I_{B1} = -I_{B2} = 50$ mA	
C_{eb}	Emitter to Base Capacitance		40	55	pF	$I_C = 0$	$V_{EB} = 0.5$ V
C_{cb}	Collector to Base Capacitance		5.0	12	pF	$I_E = 0$	$V_{CB} = 10$ V

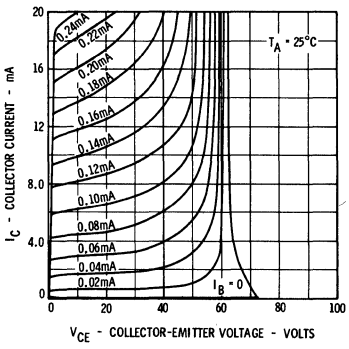
TYPICAL ELECTRICAL CHARACTERISTICS

SH6500

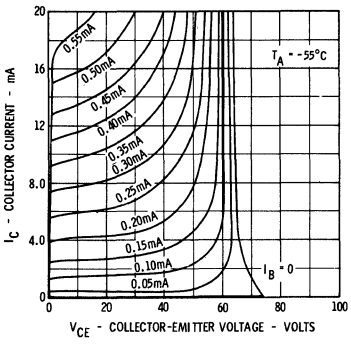
COLLECTOR CHARACTERISTICS*



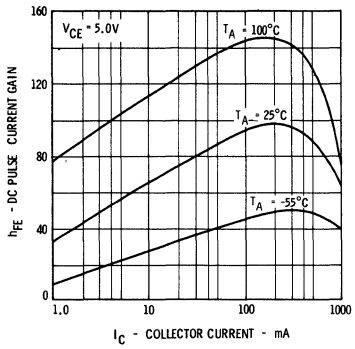
COLLECTOR CHARACTERISTICS*



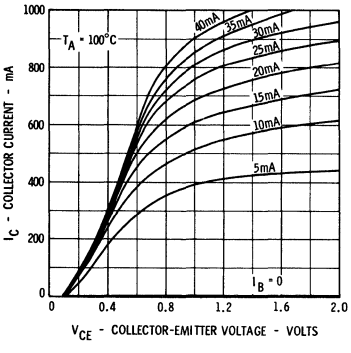
COLLECTOR CHARACTERISTICS*



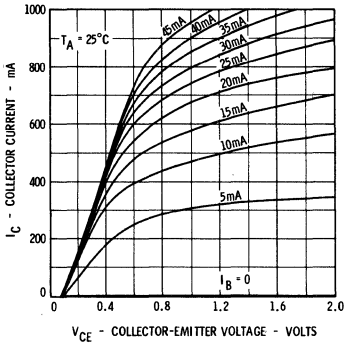
DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT



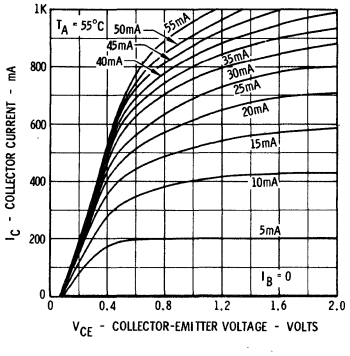
COLLECTOR CHARACTERISTICS*



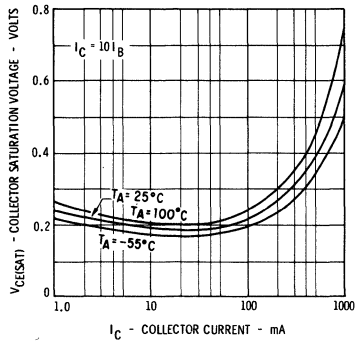
COLLECTOR CHARACTERISTICS*



COLLECTOR CHARACTERISTICS*



COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



* Single family characteristics on Transistor Curve Tracer.

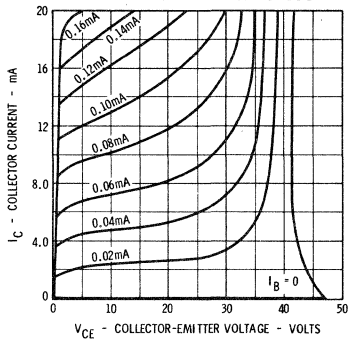
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	SH6501 MIN.	SH6501 TYP.	SH6501 MAX.	SH6502 MIN.	SH6502 TYP.	SH6502 MAX.	UNITS	TEST CONDITIONS
V_{CEO}	Collector to Emitter Sustaining Voltage	40			20			Volts	$I_C = 10$ mA $I_B = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	70			40			Volts	$I_C = 10\ \mu A$ $I_E = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	70			40			Volts	$I_C = 10\ \mu A$ $I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			6.0			Volts	$I_C = 10\ \mu A$ $I_C = 0$
I_{CES}	Collector Cutoff Current		0.1	1.7		0.1	10	μA	$V_{CE} = 40$ V $V_{BE} = 0$
I_{CBO}	Collector Cutoff Current		0.1	1.7		0.1	10	μA	$V_{CB} = 40$ V $I_E = 0$
I_{CBO}(100°C)	Collector Cutoff Current		5.0	120				μA	$V_{CB} = 40$ V $I_E = 0$
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)		0.7	0.8		0.7	0.9	Volt	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)		0.8	0.9		0.8	1.0	Volt	$I_C = 100$ mA $I_B = 10$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)	0.9	0.95	1.2		0.95	1.5	Volts	$I_C = 500$ mA $I_B = 50$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 4)		1.1	1.7				Volts	$I_C = 1000$ mA $I_B = 100$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		0.15	0.25		0.15	0.3	Volt	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		0.16	0.25		0.16	0.25	Volt	$I_C = 100$ mA $I_B = 10$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		0.3	0.5		0.3	0.6	Volt	$I_C = 500$ mA $I_B = 50$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 4)		0.5	0.9				Volt	$I_C = 1000$ mA $I_B = 100$ mA
$V_{CE(sat)}$(−55°C)	Pulsed Collector Saturation Voltage (Note 4)			0.25				Volt	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{CE(sat)}$(−55°C)	Pulsed Collector Saturation Voltage (Note 4)			0.5				Volt	$I_C = 500$ mA $I_B = 50$ mA
$V_{CE(sat)}$(100°C)	Pulsed Collector Saturation Voltage (Note 4)			0.3				Volt	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{CE(sat)}$(100°C)	Pulsed Collector Saturation Voltage (Note 4)			0.6				Volt	$I_C = 500$ mA $I_B = 50$ mA
h_{FE}	DC Pulse Current Gain (Note 4)	30	65		15	65			$I_C = 10$ mA $V_{CE} = 1.0$ V
h_{FE}	DC Pulse Current Gain (Note 4)	50	90		25	90			$I_C = 100$ mA $V_{CE} = 1.0$ V
h_{FE}	DC Pulse Current Gain (Note 4)	30	50		10	50			$I_C = 500$ mA $V_{CE} = 1.0$ V
h_{FE}	DC Pulse Current Gain (Note 4)	15	20						$I_C = 1000$ mA $V_{CE} = 1.0$ V
h_{fe}	High Frequency Current Gain (f = 100 MHz)	2.5	4.5		2.0	4.5			$I_C = 50$ mA $V_{CE} = 10$ V
t_{on}	Turn On Time		25	35		25	50	ns	$I_C = 500$ mA $I_{B1} = 50$ mA
t_{off}	Turn Off Time		45	60		45	75	ns	$I_C = 500$ mA, $I_{B1} = -I_{B2} = 50$ mA
t_s	Storage Time		35	50		35	65	ns	$I_C = 50$ mA, $I_{B1} = -I_{B2} = 50$ mA
C_{eb}	Emitter to Base Capacitance		40	55		40	55	pF	$I_C = 0$ $V_{EB} = 0.5$ V
C_{cb}	Collector to Base Capacitance		5.0	12		5.0	12	pF	$I_E = 0$ $V_{CB} = 10$ V

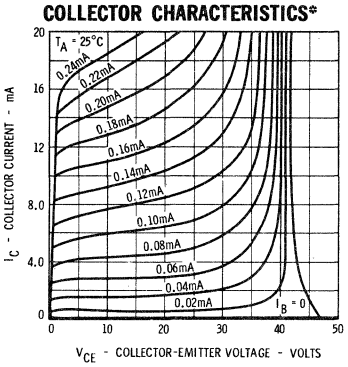
TYPICAL ELECTRICAL CHARACTERISTICS

SH6501 • SH6502

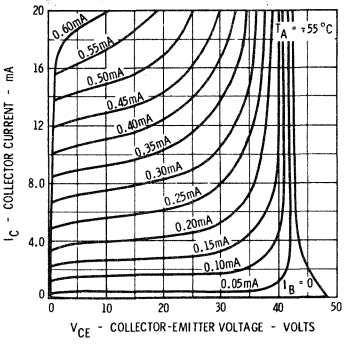
COLLECTOR CHARACTERISTICS*



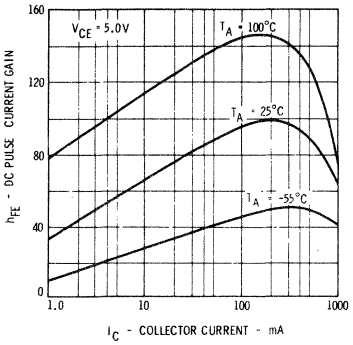
COLLECTOR CHARACTERISTICS*



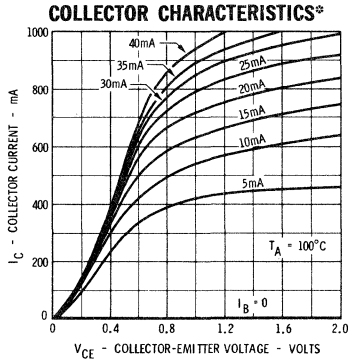
COLLECTOR CHARACTERISTICS*



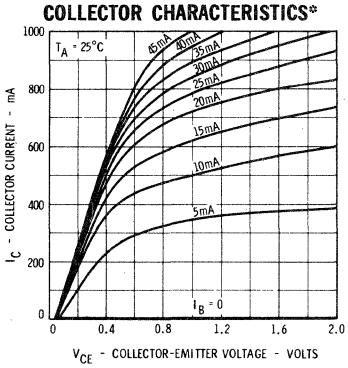
DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT



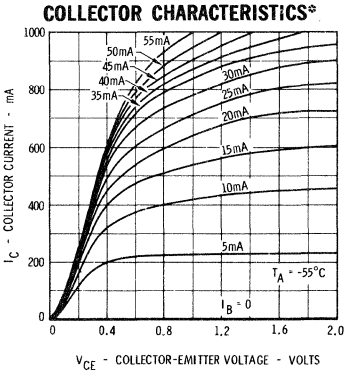
COLLECTOR CHARACTERISTICS*



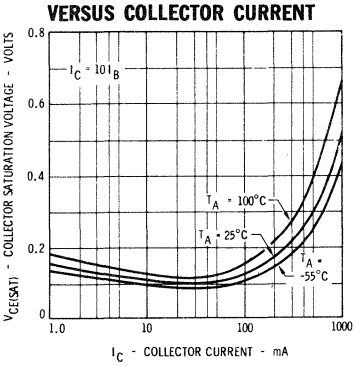
COLLECTOR CHARACTERISTICS*



COLLECTOR CHARACTERISTICS*



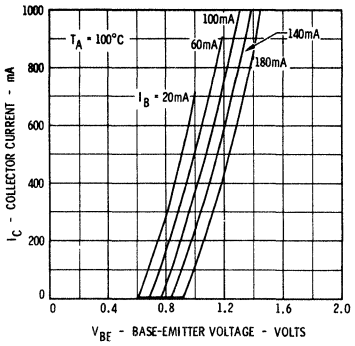
COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



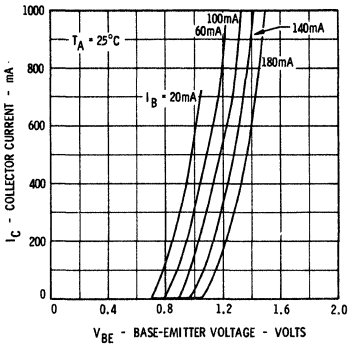
* Single family characteristics on Transistor Curve Tracer.

TYPICAL ELECTRICAL CHARACTERISTICS

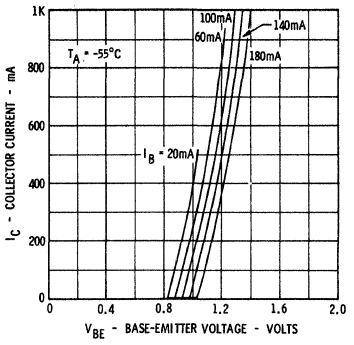
BASE CHARACTERISTICS*



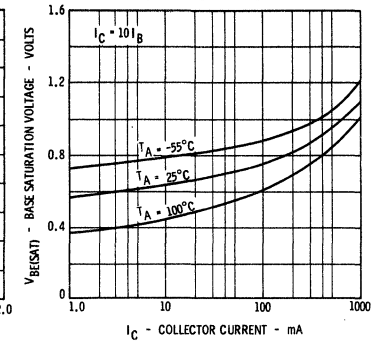
BASE CHARACTERISTICS*



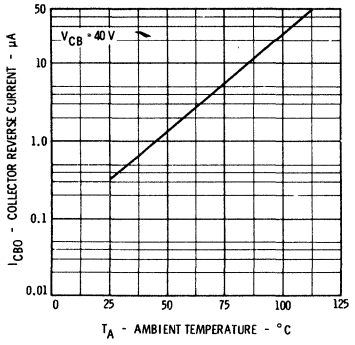
BASE CHARACTERISTICS*



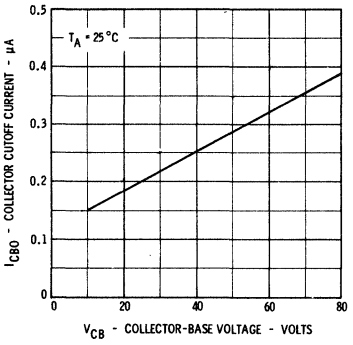
BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



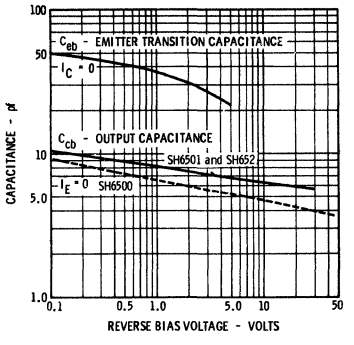
COLLECTOR CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE



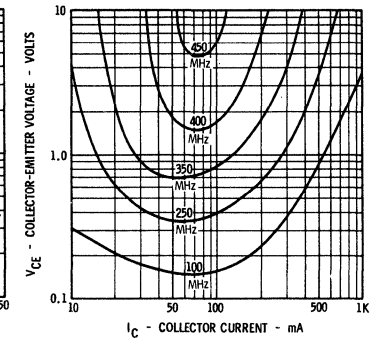
COLLECTOR CUTOFF CURRENT VERSUS REVERSE BIAS VOLTAGE



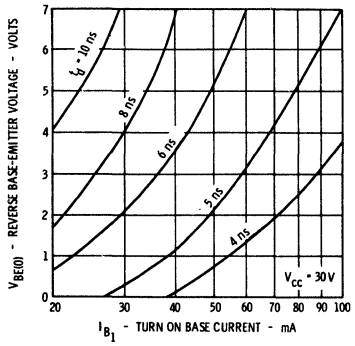
INPUT AND OUTPUT CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



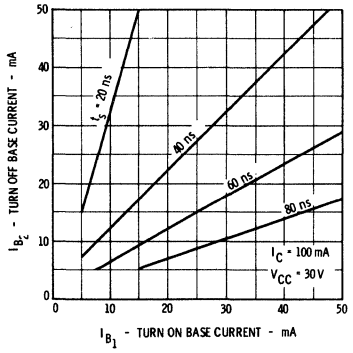
CONTOURS OF CONSTANT BANDWIDTH PRODUCT (f_T)



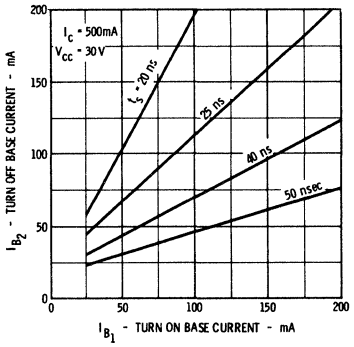
DELAY TIME VERSUS TURN ON BASE CURRENT AND REVERSE BASE EMITTER VOLTAGE



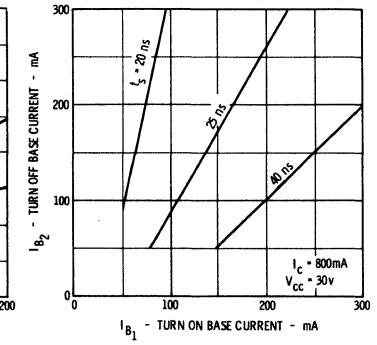
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



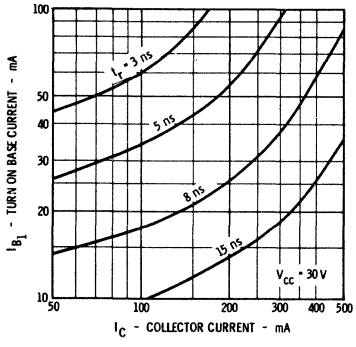
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



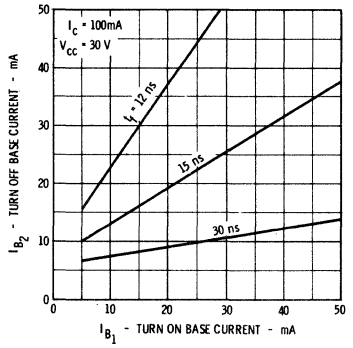
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



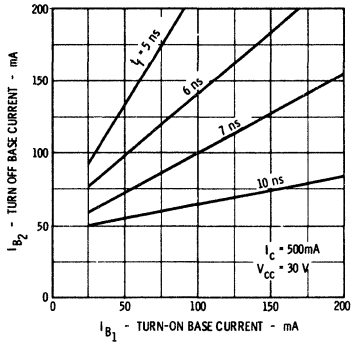
RISE TIME VERSUS COLLECTOR AND TURN ON BASE CURRENTS



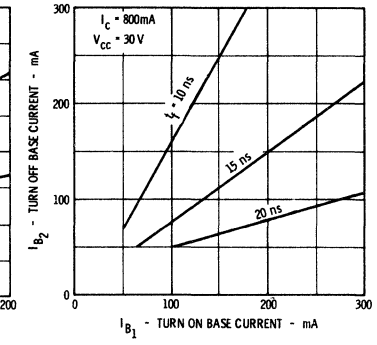
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



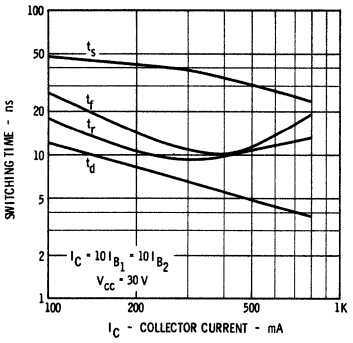
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



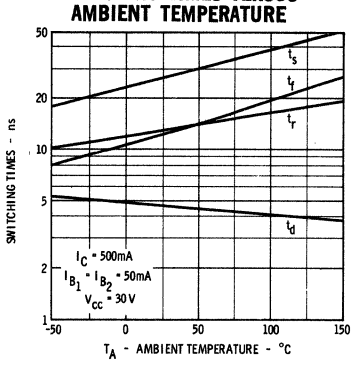
* Single family characteristics on Transistor Curve Tracer.

TYPICAL SWITCHING CHARACTERISTICS

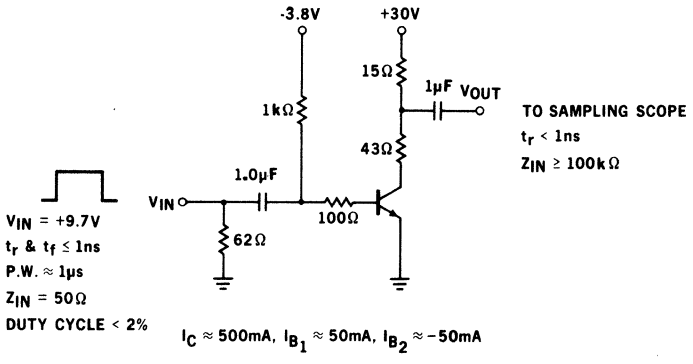
SWITCHING TIMES VERSUS COLLECTOR CURRENT



SWITCHING TIMES VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT



NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction to case thermal resistance of ~135°C/Watt (derating factor of ~7.4 mW/°C) for the Flat package and Ceramic Dual In-Line package. Maximum junction temperature of 150°C and junction to case thermal resistance of ~83°C/Watt (derating factor of ~12 mW/°C) for the Plastic Dual In-Line package.

(4) Pulse Conditions: length = 300 μs; duty cycle = 1%.

(5) See switching circuit for exact value of I_C, I_{B1}, and I_{B2}.

SH8080

4-BIT ARITHMETIC UNIT

FAIRCHILD HYBRID CIRCUITS

GENERAL DESCRIPTION —
The SH8080 is a 4-bit ripple carry adder with holding register included. It consists of MSI chips interconnected on a multi-layer thick-film substrate.

FEATURES

- **4 BIT RIPPLE CARRY ADDITION PLUS 4 BIT HOLDING REGISTER WITH TRUE AND COMPLEMENT OUTPUTS**
- **CCSL COMPATIBLE**
- **32 ns CARRY PROPAGATION TIME (TYP)**
- **1 VOLT NOISE MARGIN**
- **MILITARY AND INDUSTRIAL TEMPERATURE RANGES**
- **HERMETIC PACKAGE**

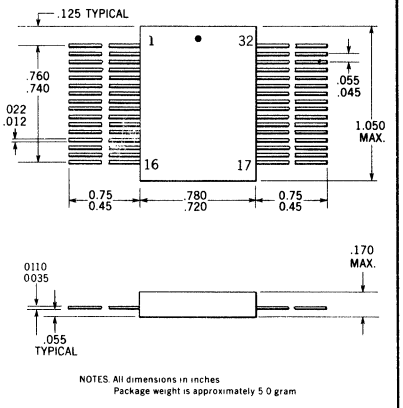
APPLICATION

- **AIRBORNE COMPUTERS**
- **DESK TOP CALCULATORS**
- **HIGH SPEED DATA PROCESSING EQUIPMENT**
- **HIGH SPEED GROUND SUPPORT EQUIPMENT**

ABSOLUTE MAXIMUM RATINGS (25°C unless noted)

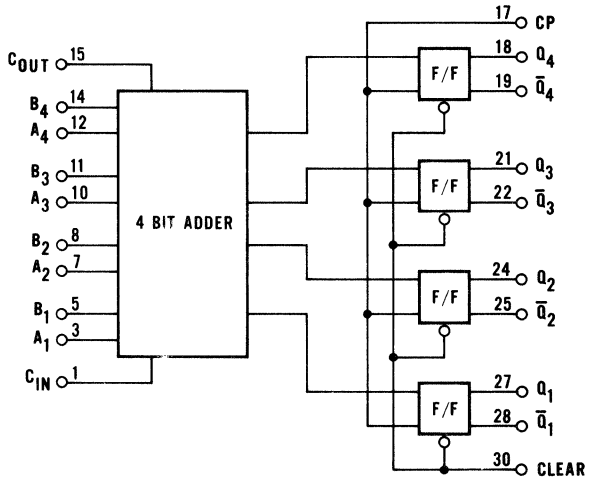
V_{CC} (pin 32) to ground (pin 16)	−0.5 to 8.0 Volts
Inputs	−0.5 to 6.5 Volts
Voltage applied to outputs	−0.5 to V_{CC}
Current into low output	50 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C*
	0°C to +70°C

PHYSICAL DIMENSIONS



HBY80801XX −55°C to +125°C*
HBY80809XX 0°C to +70°C

LOGIC DIAGRAM



*At operating temperatures above +100°C, device must be heat sunk.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

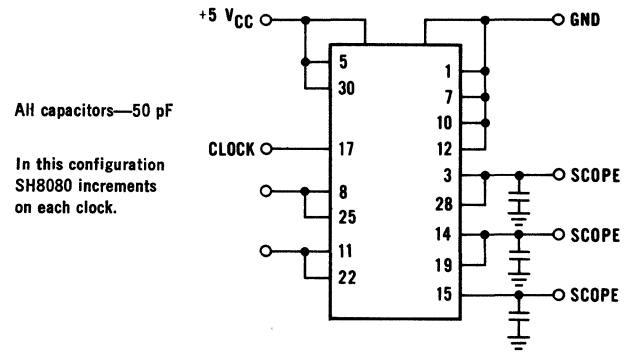
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Volts, Pin 16 Grounded, T_A = 25°C unless otherwise specified)

CHARACTERISTICS		TTμL Load* Factors	CCSL Load* Factors
Input Loading	Pins 1, 3, 5, 10, 11	4	80/48
Input Loading	Pins 7, 8, 12, 14	1	20/12
Input Loading	Pin 30	11	240/144
Input Loading	Pin 17	4	80/48
Output Drive	Pin 15	9	120/72
Output Drive	Pins 18, 19, 21, 22, 24, 25, 27, 28	6	180/108
Typical Power Consumption			840 mW
Typical Carry Propagation Delay			32 ns
Typical Clock Pulse Width			11 ns
Typical Data Setup Time			64 ns
Typical Output Delay Time (t_{pd+})			12 ns
Typical Output Delay Time (t_{pd-})			21 ns

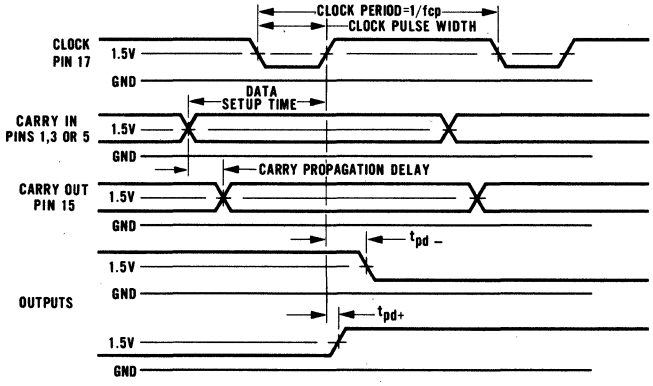
*Based on TTμL standard Load Factors in Fairchild TTμL Data Sheets and on CCSL Load Factors in CCSL Application Note (Application Note #154).

SWITCHING TIME TEST CIRCUIT



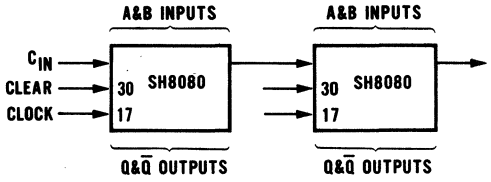
Carry propagation time is measured from pin 19 and/or pin 28 to pin 15 at the appropriate counts.

SWITCHING WAVEFORMS

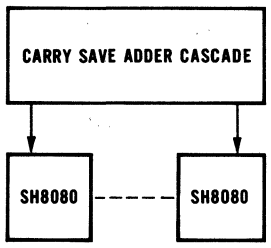


Note 1. Clear is normally held high. Q is reset during high to low transition.

APPLICATIONS



8 Bit Parallel Adder. Typical operating time is given by 32 ns typical carry propagation delay in first stage plus 64 ns data setup time in second stage = 96 ns. By returning true outputs to "A" inputs, the function A — A+B is performed. If B is "1's" complemented and the input carry = 1, then A — A—B is realized.



For high speed multiplication a carry save adder cascade followed by SH8080 as carry propagate adder/accumulator can be used. Refer to App-163 Applications of the CCSL 9304 Dual Adder.

HYBRID INTEGRATED CIRCUITS COMING SOON

Type	Function	Type	Function
SH2005	Quad Power Gate	SH8081	4-Bit Arithmetic Logic Unit
SH3202	Voltage Regulator with Compensation and Foldback Current		

SH2005 — QUAD POWER GATE

The SH2005 is a high speed core, cable or lamp driver. The device features high voltage and high current capability. All inputs are CCSL compatible.

Features:

Inputs CCSL Compatible
Use for Core, Cable and Lamp Driver
High Current Capability . . . 250mA Sinking Current at 0.5 volts.
High Voltage Capability . . . 40 volts LV_{CEO} . . . four 2 input NAND gates
High Speed — t_{on} = 60ns (typ) . . . t_{off} = 50ns (typ) . . . All four gates switching simultaneously

SH3202—Voltage Regulator with Compensation and Foldback Current

The SH3202 is a Hybrid voltage regulator. The device consists of a temperature compensated reference amplifier, power series pass transistor and current limit circuitry.

Features:

Positive or negative supply operation
Series, shunt, switching or floating operation
.01% line and load regulation
Output voltage adjustable from 2 to 27 volts
Output current to 150mA without external pass transistor

SH8081 — 4-Bit Arithmetic Logic Unit

The SH8081 consists of six MSI 9304, dual full adders and two MSI 9309, dual four bit digital multiplexers.

Features;

Multifunction capability
High speed operation
Eight CCSL MSI chips in one 30 pin flat package
Fully buffered complementary outputs

The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL, and TTμL families CCSL

Linear Integrated Circuits

LINEAR INTEGRATED CIRCUIT NUMERICAL INDEX

LINEAR APPLICATIONS/PRODUCTS CROSS REFERENCE

Differential Input, Differential Output Amplifiers	μA727, μA730, μA733, μA751C, μA725
Operational Amplifiers	
General Purpose —	
Summing, Subtracting, Integrating, Differentiating, Impedance Transformers, Analog Computers	μA702, μA709, μA715, μA739, μA740, μA741, μA749
Instrumentation —	
Low drift, Chopper stabilized, Strain gage, Thermocouple	μA726, μA727, μA725
High Input Impedance —	
Active filters, Buffer amps, Transducers, Integrators	μA727, μA740, μA715, μA725
Low Power Consumption —	
Battery powered, Airborne, Spaceborne, portable, low weight systems	μA741, μA749, μA735
High Speed —	
Phase-locked loops, A/D & D/A converters, pulse height analyzers, multiplexed analog gates, sample and holds, integrators, and differentiators	μA702, μA715, μA740
Temperature Stabilized —	
Bridge amplifiers, process control, precision measurements, instrumentation amps.	μA726, μA727, μA725
Power/Driver Amplifiers	
Audio Preamp —	
Low noise, magnetic tape, phono	μA730, μA739, μA749
Medium Power —	
Telephone Sysems, head sets	μA716
Power Driver —	
Servos, Audio	μA716
High Speed Video —	μA715
Comparators	
High Speed —	
Level detectors, Schmitt triggers, Go-No-Go detectors, Window detector, pulse height discriminator, line receivers	μA710, μA711, μA731
Precision —	
Digital volt-meters, A/D and D/A converters, pulse width modulators, phase locked loops, precision measuring equipment.	μA715, μA727, μA740, μA739, μA749
High Frequency/Communications	
IF Amplifiers —	
Microwave, radar, AM & FM IF strips, TV	μA703, μA717, μA719
Video Amplifiers —	μA702, μA715, μA733
Audio Amplifier —	μA716
Demodulators —	μA737, μA746
AGC IF Amps —	μA719

LINEAR APPLICATIONS/PRODUCTS INDEX CROSS REFERENCE

Oscillators	
Audio —	
Telemetry phase detector reference, servo systems	μA709, μA740, μA741, μA739, μA749
High Frequency —	
Radar, communications receivers and transmitters, radio, TV	μA702, μA703, μA715, μA733
Linear-Digital Interface	
Line Receivers —	μA710, μA711, μA731
Analog to Digital —	
Telemetry, Maintenance monitor, process control	μA710, μA715, μA722
Digital to Analog —	
Telemetry, Process Control, displays	μA715, μA722
Television	
Sound —	μA703, μA717, μA716, μA719
Chroma Oscillator —	μA703
IF Amplifiers —	μA703, μA717, μA719
Chroma Demodulator —	μA737, μA746
Digital Computer Systems	
Core Memories —	μA710, μA711, μA731, μA739, μA749, μA751
Other Memories —	
Film, Plated wire, magnetic tape, Disc. file	μA702, μA710, μA733, μA751
Displays —	μA715, μA722
Hybrid Computers —	μA722
Power Supplies	
Series Voltage Regulators —	μA723
Switching Voltage Regulators —	μA710, μA711, μA723, μA742
Precision Low Drift Voltage Reference —	μA726
Active Filters	μA702, μA709, μA715 μA716, μA739, μA740 μA741, μA749
Special Functions	
Digitally Controlled Function Generators —	μA722
Voltage Controlled Function Generator —	μA715, μA722, μA741
D.C. Logarithmic Amp —	μA726
IF Logarithmic Amp —	μA703
Multiplier —	μA726, μA737, μA746
Dividers —	μA726
Product Detector —	μA737, μA746
Scaler —	μA722
Trigonometric Function Generators —	μA709, μA726, μA739 μA740, μA741, μA749
Medical Electronics	μA727, μA739, μA740 μA741, μA725, μA749
Power Control	μA742

μA702A

HIGH GAIN, WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

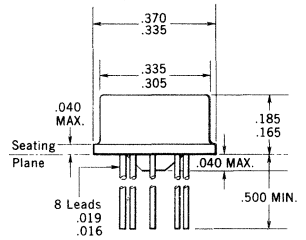
- **IMPROVED SPECIFICATIONS**
- **2 mV MAXIMUM OFFSET VOLTAGE**
- **2500 MINIMUM VOLTAGE GAIN**
- **10 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

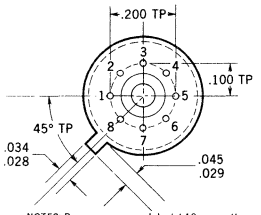
GENERAL DESCRIPTION — The μA702A is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in high speed analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 Volts to −6.0 V
Internal Power Dissipation	
TO-99 [Note 1]	300 mW
Flat Package [Note 2]	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

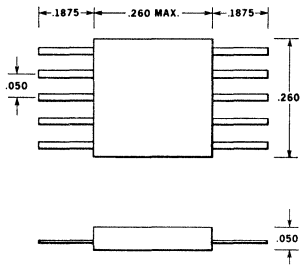




NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

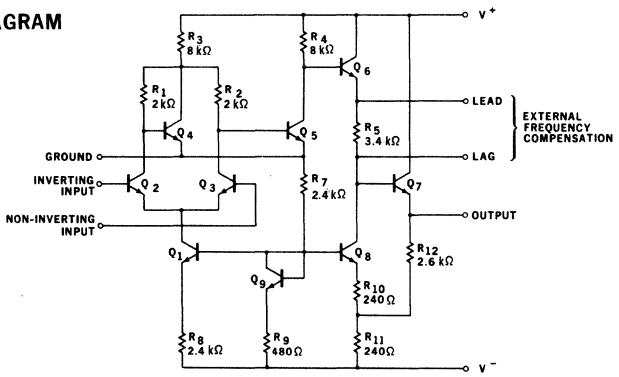
ORDER PART NO. U5B770231X†

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

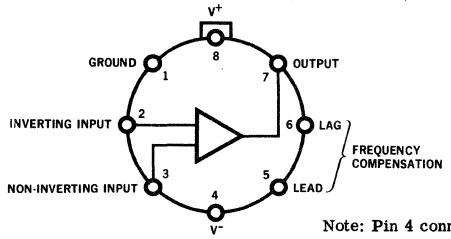


ORDER PART NO. U3H770231X

SCHEMATIC DIAGRAM

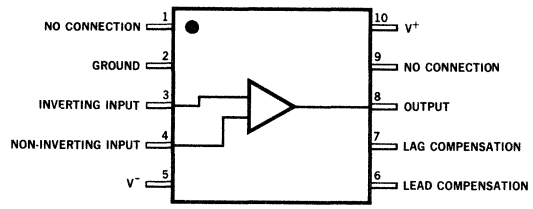


TO-99 CONNECTION DIAGRAM (TOP VIEW)



Note: Pin 4 connected to case.

FLAT PACKAGE CONNECTION DIAGRAM (TOP VIEW)



Notes on page 2

* Planar is a patented Fairchild process.
† Equivalent to U5B77123IX and U3H77123IX

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

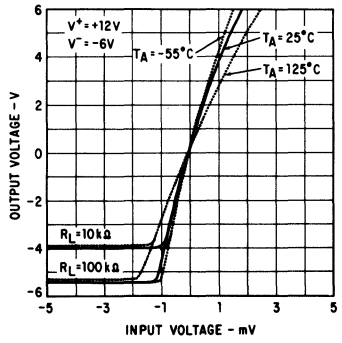
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2\ k\Omega$		0.5	2.0		0.7	3.0	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2.0	5.0		1.2	3.5	μA
Input Resistance		16	40		22	67		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	80	100		80	100		dB
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	2500	3600	6000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				600	900	1500	
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity-gain)	$C_1 = 0.01\ \mu F$, $R_1 = 20\ \Omega$, $R_L \geq 100\ k\Omega$, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_3 = 50$ pF, $R_L \geq 100\ k\Omega$, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			3.0			4.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = +125°C$		2.5	10		3.5	15	μV/°C
	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = -55°C$		2.0	10		3.0	15	μV/°C
Input Offset Current	$T_A = +125°C$		80	500		50	500	nA
	$T_A = -55°C$		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$		1.0	5.0		0.7	4.0	nA/°C
	$T_A = 25°C$ to $T_A = -55°C$		3.0	16		2.0	13	nA/°C
Input Bias Current	$T_A = -55°C$		4.3	10		2.6	7.5	μA
Input Resistance		6.0			8.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = -6$ V to $V^+ = 6$ V, $V^- = -3$ V, $R_S \leq 2\ k\Omega$		75	200		75	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	2000		7000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				500		1750	
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125°C$, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55°C$, $V_{out} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125°C$, $V_{out} = 0$		80	120		15	30	mW
	$T_A = -55°C$, $V_{out} = 0$		90	135		19	35	mW

NOTES:

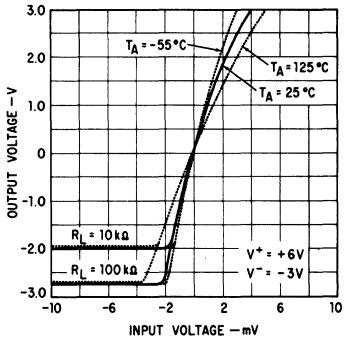
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

TYPICAL PERFORMANCE CURVES

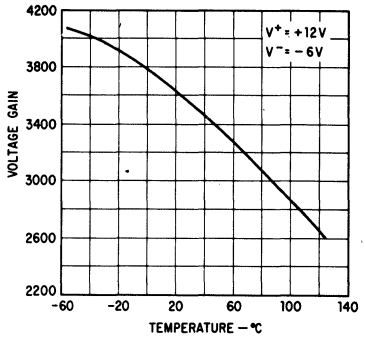
VOLTAGE TRANSFER CHARACTERISTIC



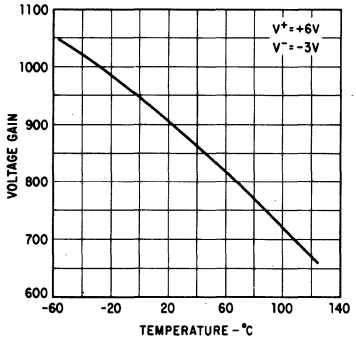
VOLTAGE TRANSFER CHARACTERISTIC



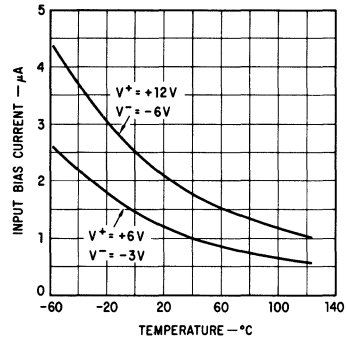
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



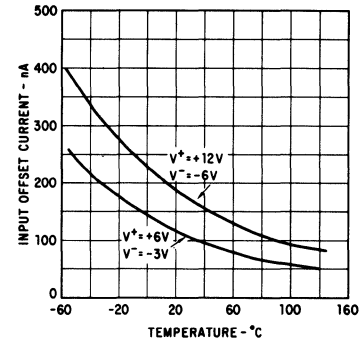
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



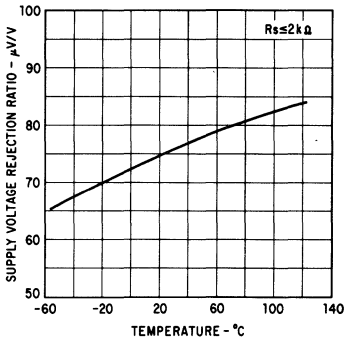
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



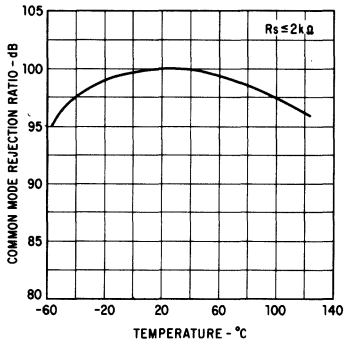
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



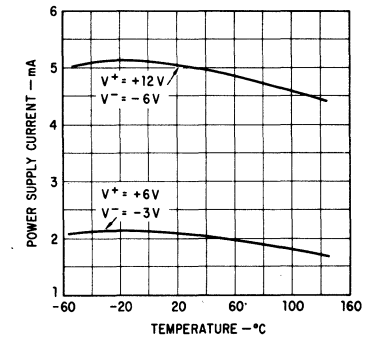
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



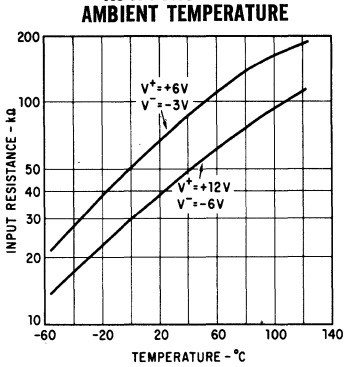
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



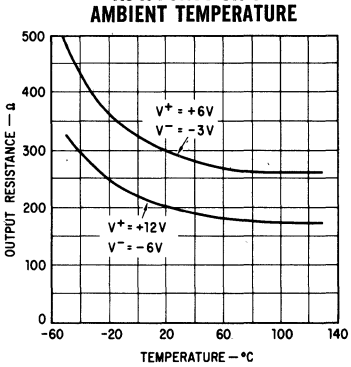
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



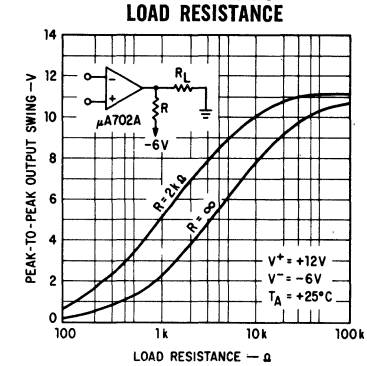
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

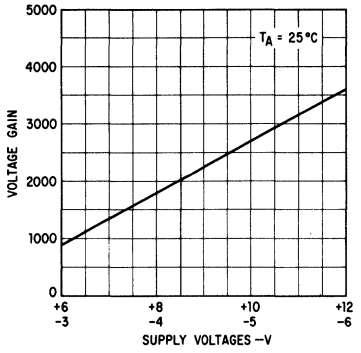


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

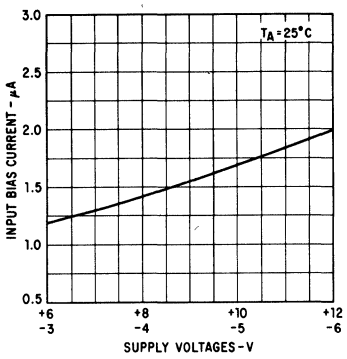


TYPICAL PERFORMANCE CURVES

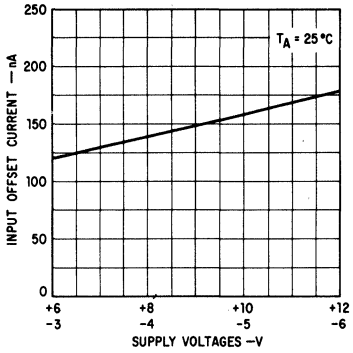
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



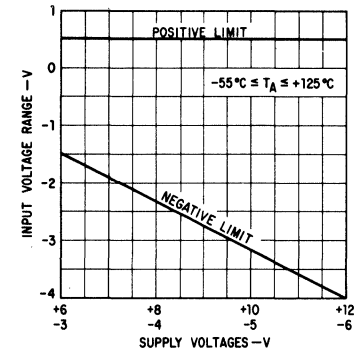
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



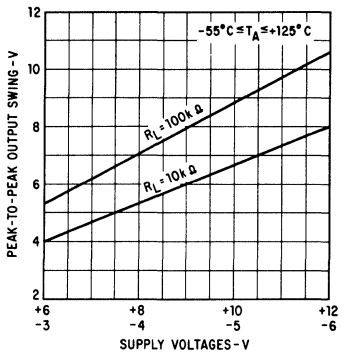
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



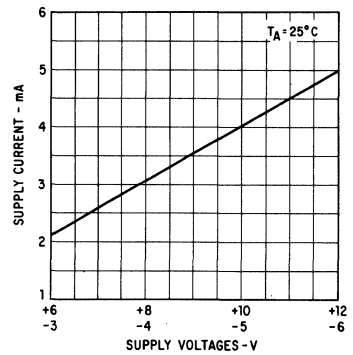
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



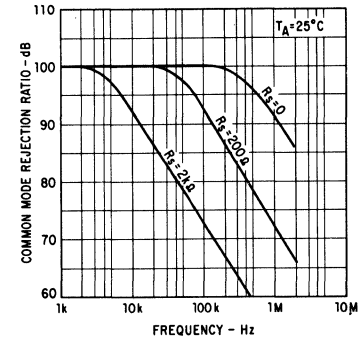
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



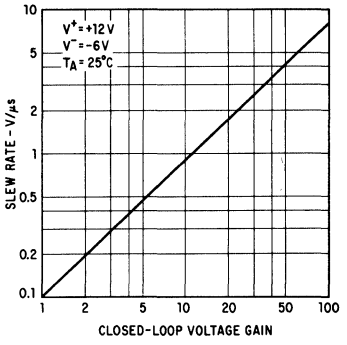
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



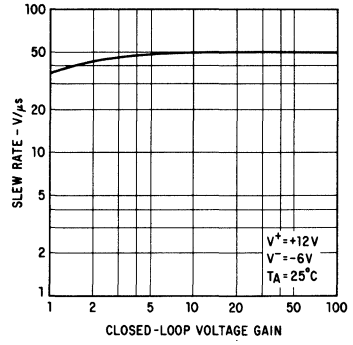
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

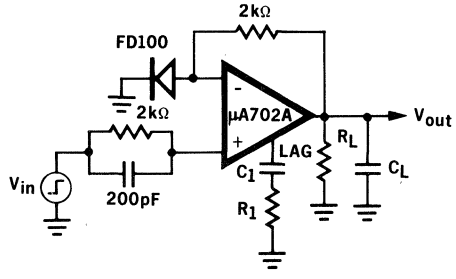


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

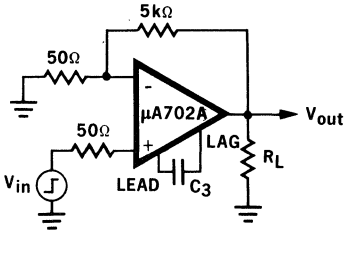


TRANSIENT RESPONSE TEST CIRCUITS

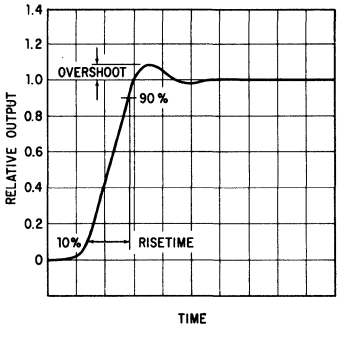
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

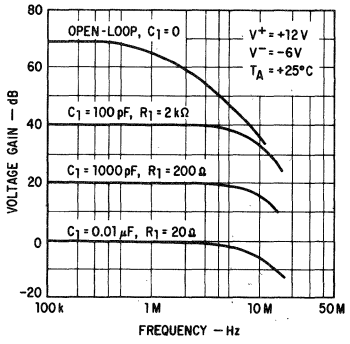
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

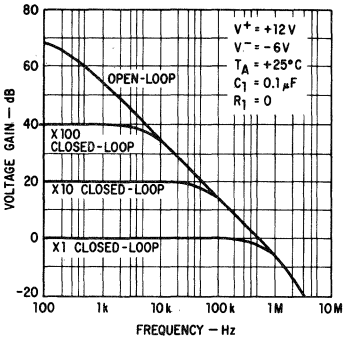
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

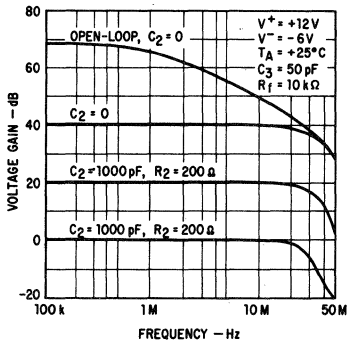
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



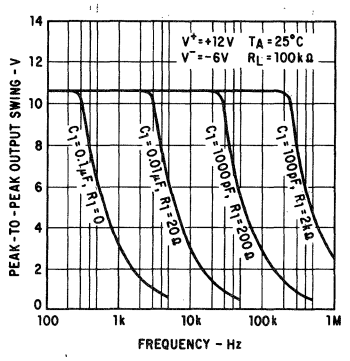
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



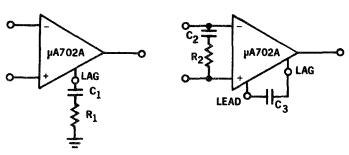
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

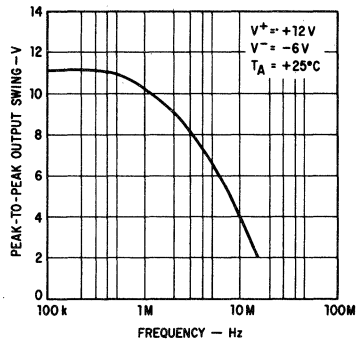


FREQUENCY COMPENSATION CIRCUITS
(Refer to Fairchild APP-117 for further details.)



LAG COMPENSATION **LEAD-LAG COMPENSATION**

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



μA702B

HIGH GAIN, WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **2000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

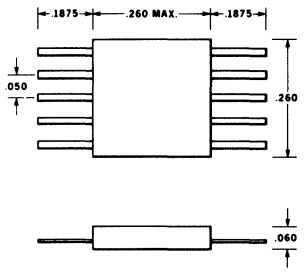
GENERAL DESCRIPTION — The μA702B is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

For improved specifications, see μA702A data sheet.

ABSOLUTE MAXIMUM RATINGS

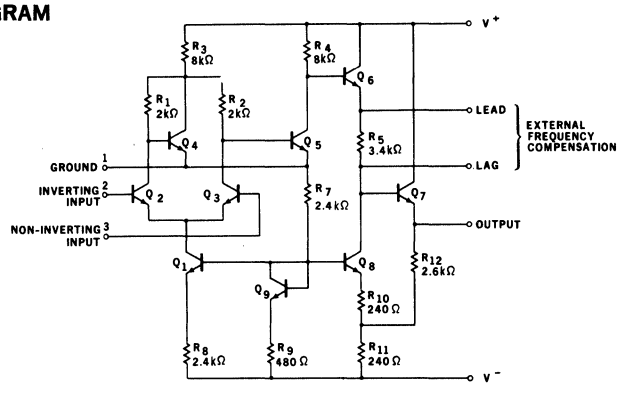
Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	−55° C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

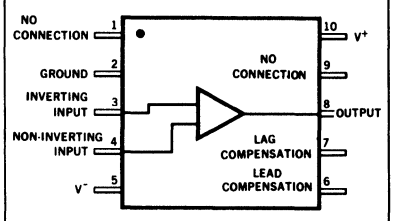


ORDER PART NO.
U3H7702313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

NOTE 1: Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

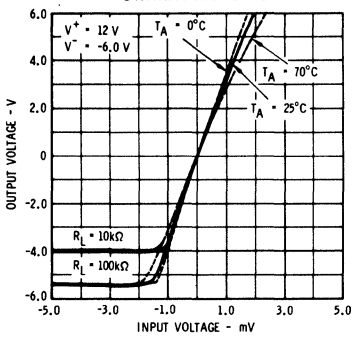
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

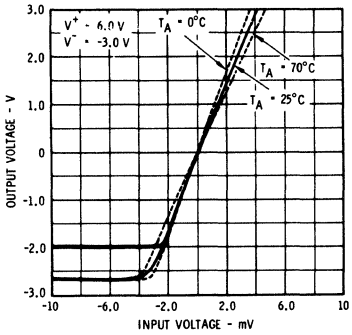
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2\ k\Omega$		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	2000	3400	6000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity gain)	$C_l = 0.01\ \mu F$, $R_l = 20\Omega$, $R_L \leq 100\ k\Omega$, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_3 = 50$ pF, $R_L \geq 100\ k\Omega$, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = +70°C$ to $T_A = 0°C$		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		4.0	10		3.0	8.0	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		6.0	20		5.5	18	nA/°C
Input Bias Current	$T_A = 0°C$		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, f ≤ 1 kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = 6$ V to $V^+ = 6$ V, $V^- = 3$ V, $R_S \leq 2\ k\Omega$		90	300		90	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	1500		7000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				400		1750	
The following specifications apply for −55°C ≤ T_A ≤ +125°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			7.5			8.0	mV
Input Offset Current	$T_A = +125°C$		0.2	2.0		0.14	2.0	μA
	$T_A = -55°C$		1.2	4.0		0.8	4.0	μA
Input Bias Current	$T_A = -55°C$		5.5	20		3.4	15	μA
Input Resistance		3.0			4.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, f ≤ 1 kHz	60	80		60	80		dB
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	1200						
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				300			
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125°C$, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55°C$, $V_{out} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125°C$, $V_{out} = 0$		80	120		15	30	mW
	$T_A = -55°C$, $V_{out} = 0$		90	135		19	35	mW

TYPICAL PERFORMANCE CURVES

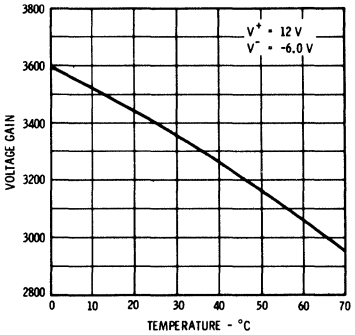
VOLTAGE TRANSFER CHARACTERISTIC



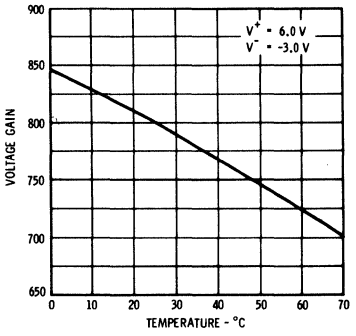
VOLTAGE TRANSFER CHARACTERISTIC



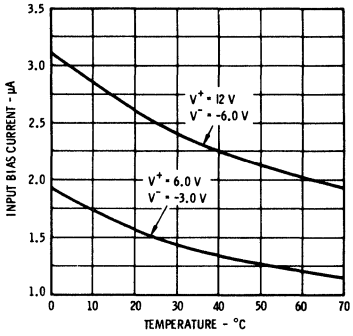
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



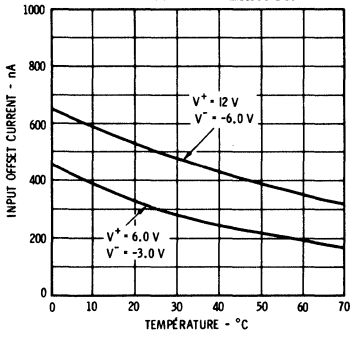
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



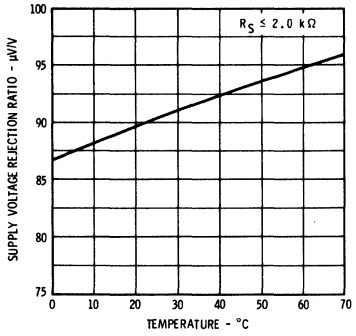
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



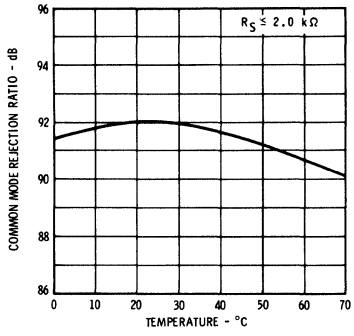
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



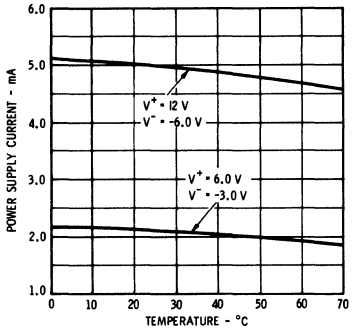
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



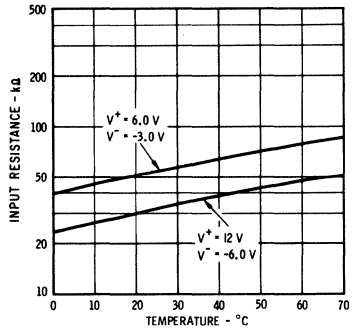
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



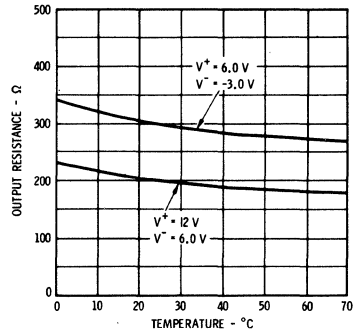
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



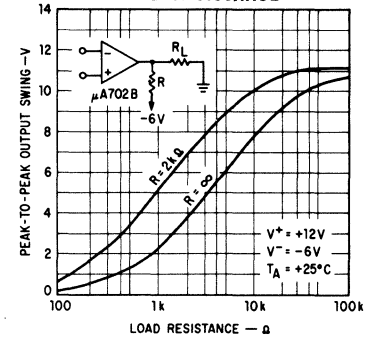
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

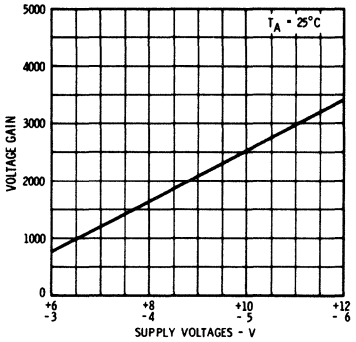


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

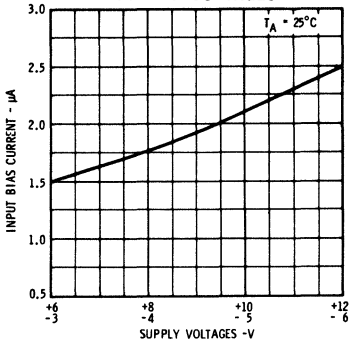


TYPICAL PERFORMANCE CURVES

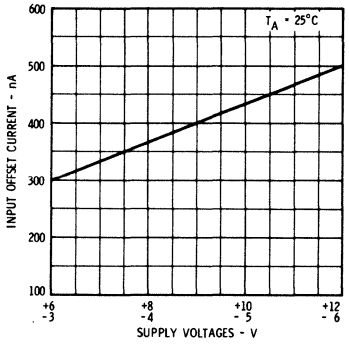
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



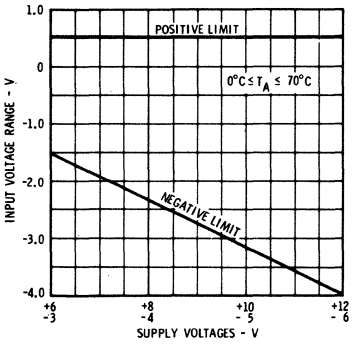
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



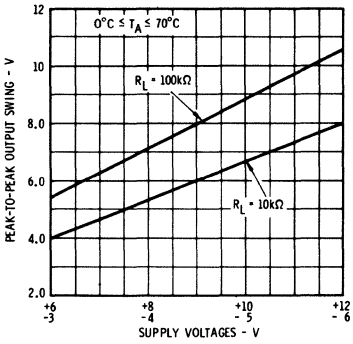
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



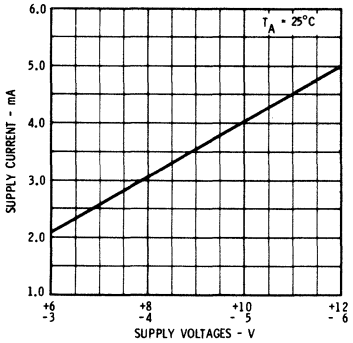
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



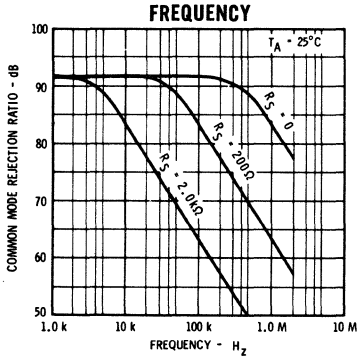
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



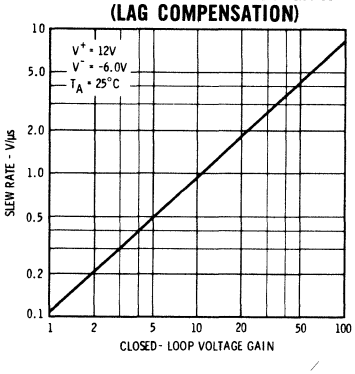
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



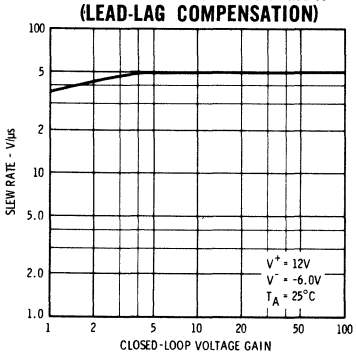
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

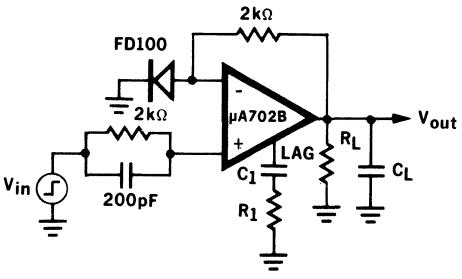


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

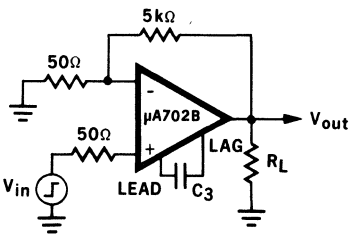


TRANSIENT RESPONSE TEST CIRCUITS

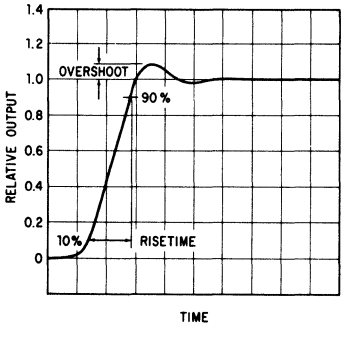
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

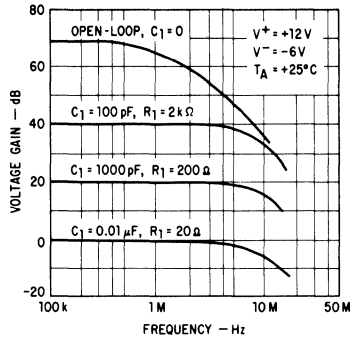
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

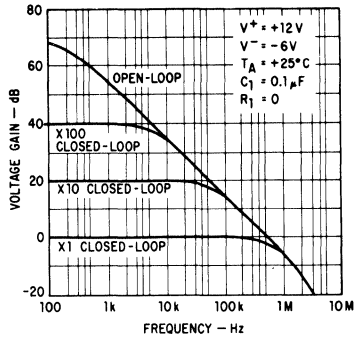
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

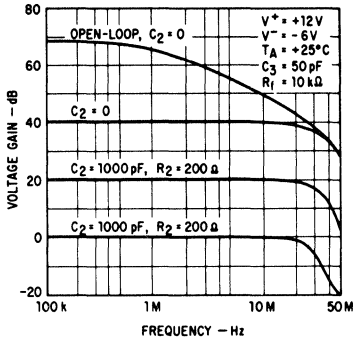
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



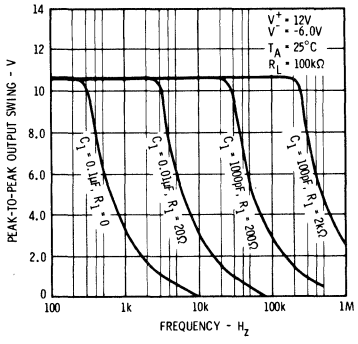
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)

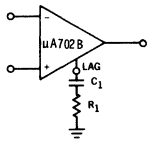


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

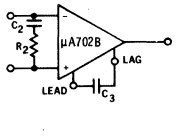


FREQUENCY COMPENSATION CIRCUITS

(Refer to Fairchild APP-117 for further details)

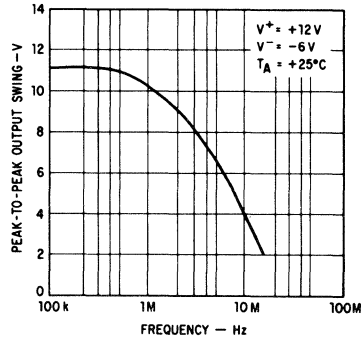


LAG COMPENSATION



LEAD-LAG COMPENSATION

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



μA702C

HIGH GAIN, WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **IMPROVED SPECIFICATIONS**
- **5 mV MAXIMUM OFFSET VOLTAGE**
- **2000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

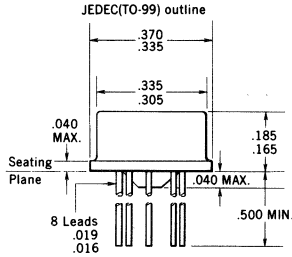
GENERAL DESCRIPTION — The μA702C is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

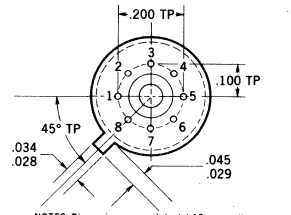
For full temperature range operation (−55°C to +125°C) see μA702A data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation [Note 1]	300 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

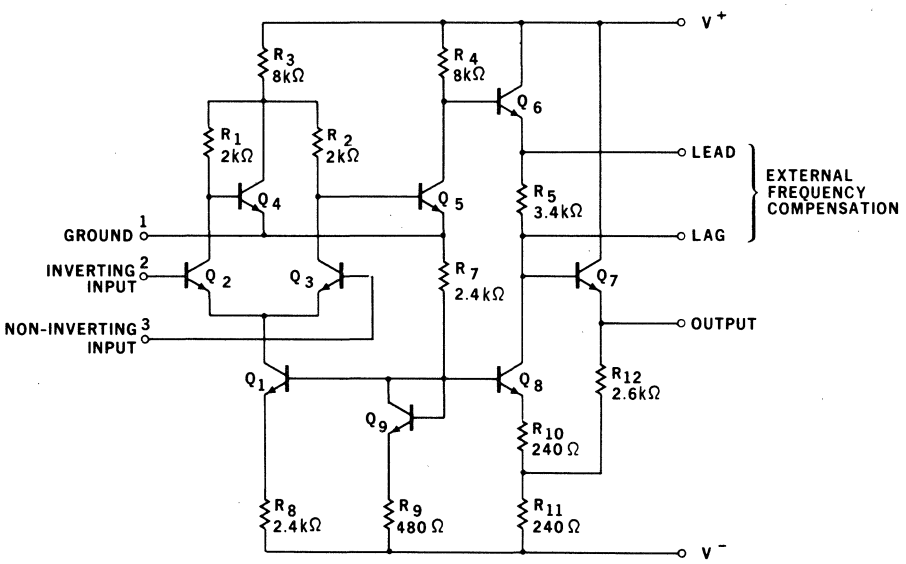




NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

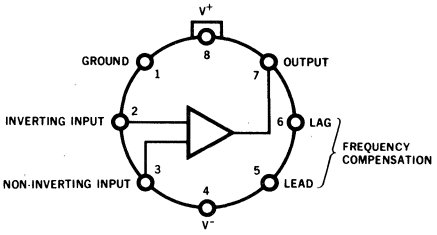
ORDER PART NO. U5B770239X

SCHEMATIC DIAGRAM



TO-99 CONNECTION DIAGRAM

(TOP VIEW)



NOTE: Pin 4 connected to can.

NOTES:
(1) Rating applies for ambient temperatures to +70°C.
(2) For Flat Package see μA702B data sheet.

* Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

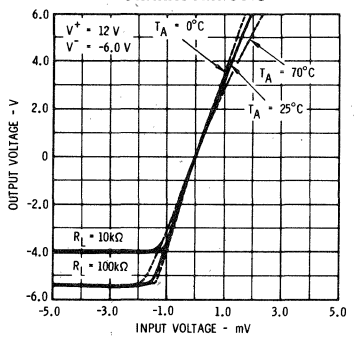
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified)

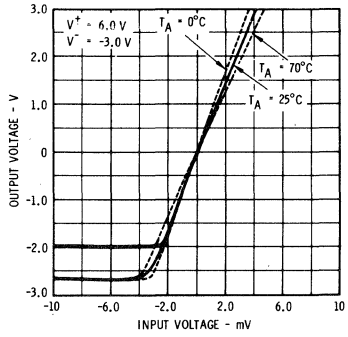
PARAMETER (see definitions)	CONDITIONS	$V^+ = 12.0$ V, $V^- = -6.0$ V MIN.	TYP.	MAX.	$V^+ = 6.0$ V, $V^- = -3.0$ V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2$ kΩ		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, $f \leq 1$ kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	2000	3400	6000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity gain)	$C_1 = 0.01$ μF, $R_1 = 20$Ω, $R_L \leq 100$ kΩ, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_3 = 50$ pF, $R_L \geq 100$ kΩ, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for $0°C \leq T_A \leq +70°C$:								
Input Offset Voltage	$R_S \leq 2$ kΩ			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω, $T_A = +70°C$ to $T_A = 0°C$		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		4.0	10		3.0	8.0	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		6.0	20		5.5	18	nA/°C
Input Bias Current	$T_A = 0°C$		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, $f \leq 1$ kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = 6$ V to $V^+ = 6$ V, $V^- = 3$ V, $R_S \leq 2$ kΩ		90	300		90	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	1500		7000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				400		1750	
Output Voltage Swing	$R_L \geq 100$ kΩ	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10$ kΩ	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$V_{out} = 0$		5.0	7.0		2.1	3.9	mA
Power Consumption	$V_{out} = 0$		90	125		19	35	mW

TYPICAL PERFORMANCE CURVES

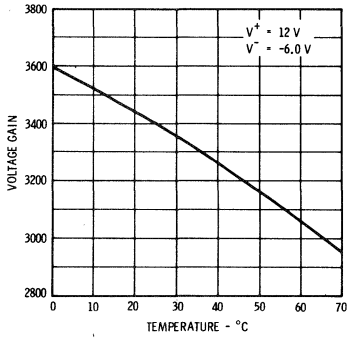
VOLTAGE TRANSFER CHARACTERISTIC



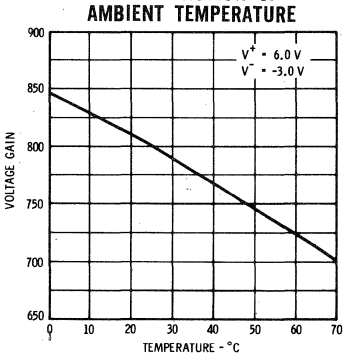
VOLTAGE TRANSFER CHARACTERISTIC



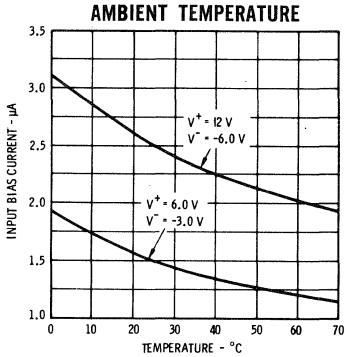
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



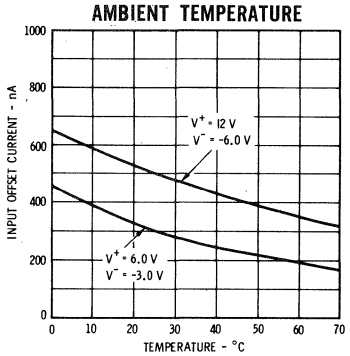
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



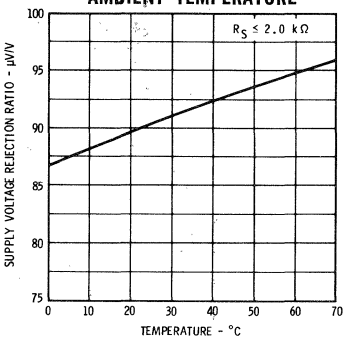
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



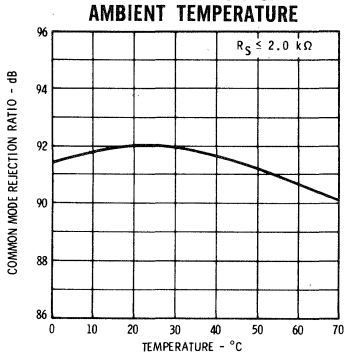
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



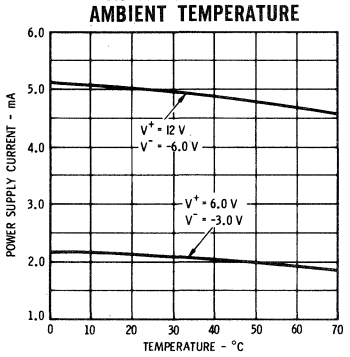
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



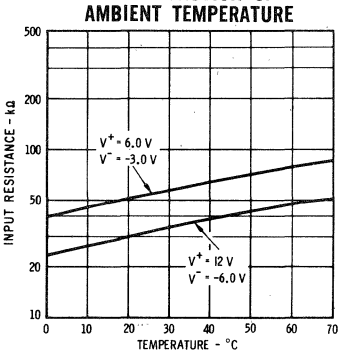
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



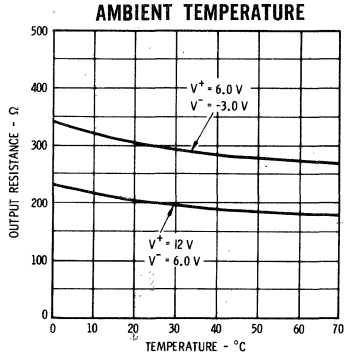
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



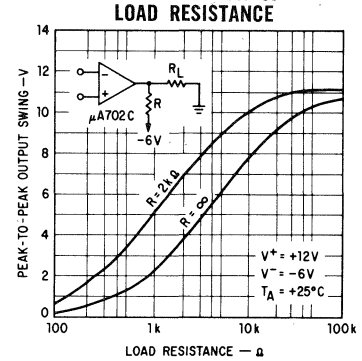
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

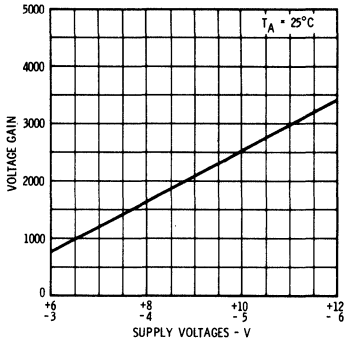


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

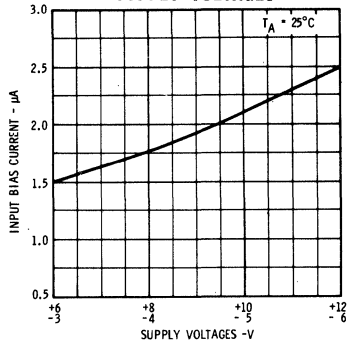


TYPICAL PERFORMANCE CURVES

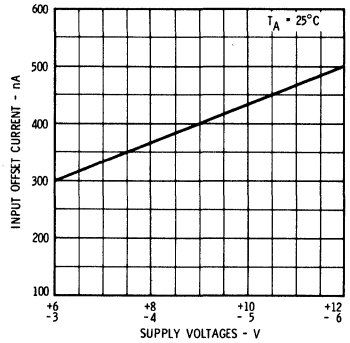
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



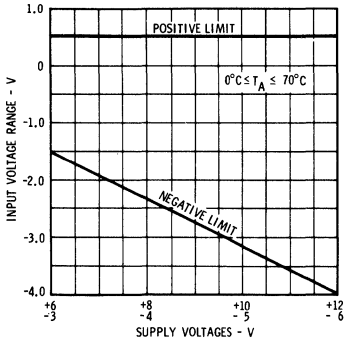
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



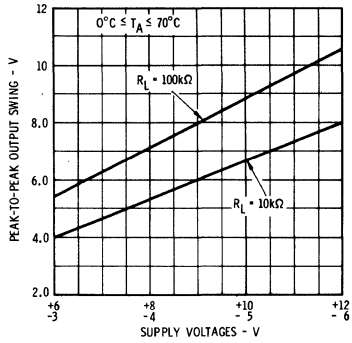
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



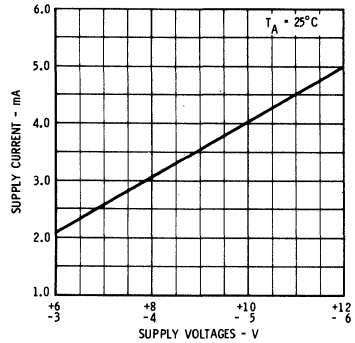
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



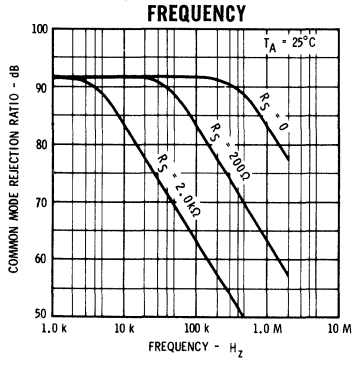
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



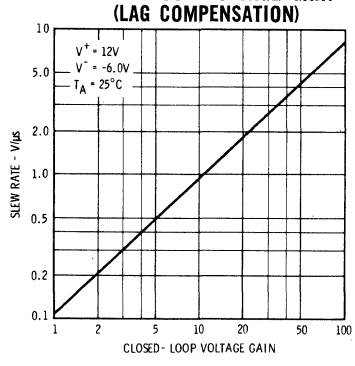
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



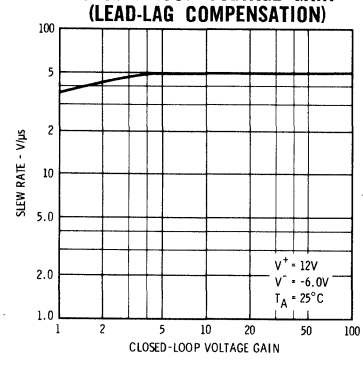
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

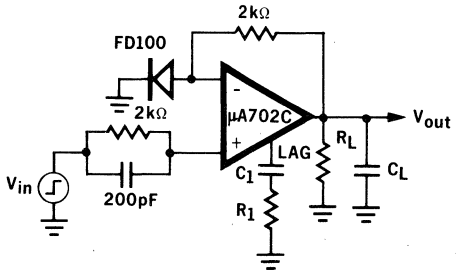


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

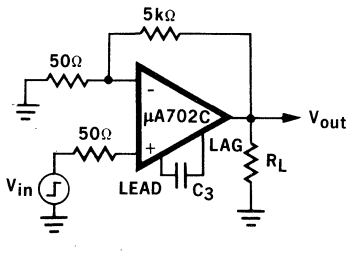


TRANSIENT RESPONSE TEST CIRCUITS

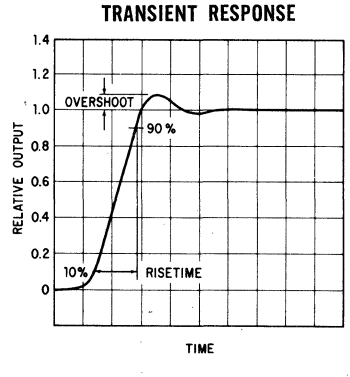
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

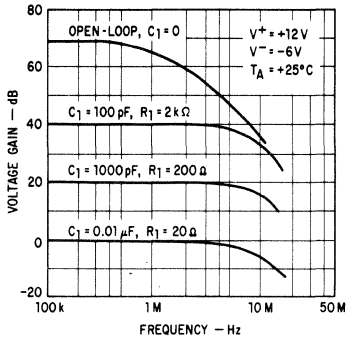
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

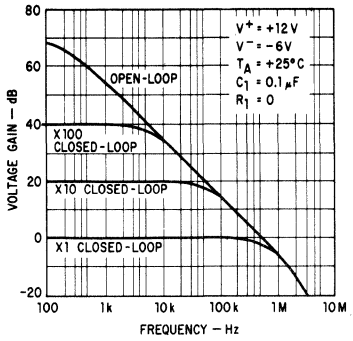
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

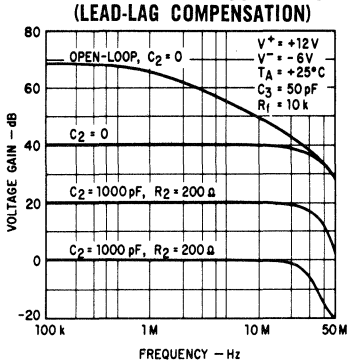
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



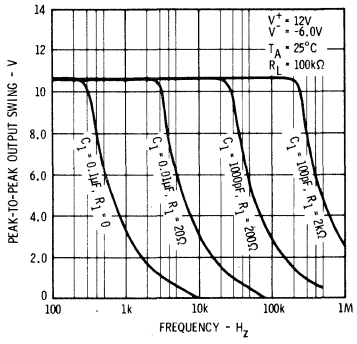
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)

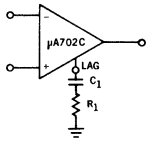


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

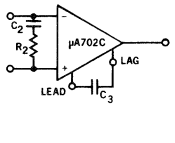


FREQUENCY COMPENSATION CIRCUITS

(Refer to Fairchild APP-117 for further details)

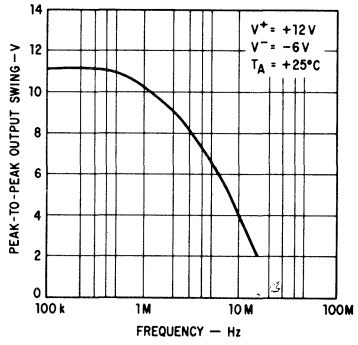


LAG COMPENSATION



LEAD-LAG COMPENSATION

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



μA703

RF-IF AMPLIFIER

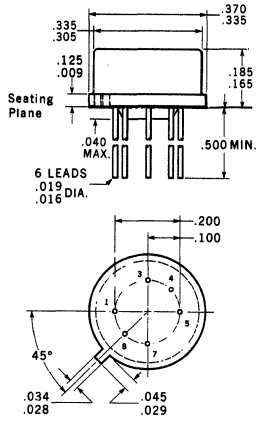
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA703 is an RF-IF amplifier constructed on a single silicon chip and is intended for use as a limiting or nonlimiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	± 5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering - 60 seconds)	300°C

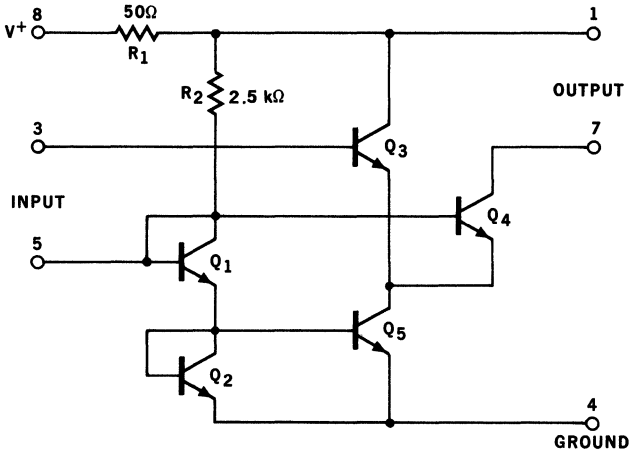
PHYSICAL DIMENSIONS
(in accordance with JEDEC TO-99 outline)



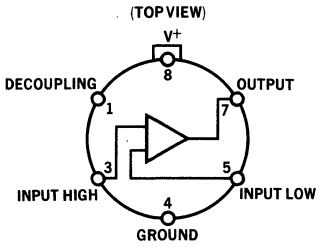
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.27 grams

ORDER PART NO. U5D770331X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 connected to case.

NOTE 1: Rating applies for ambient temperatures to 125°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

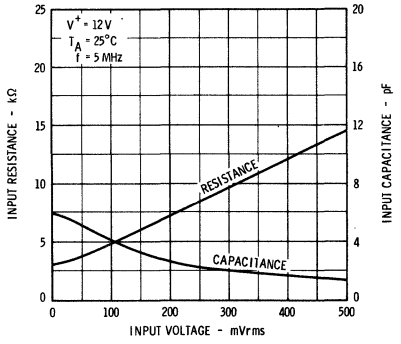
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise specified)

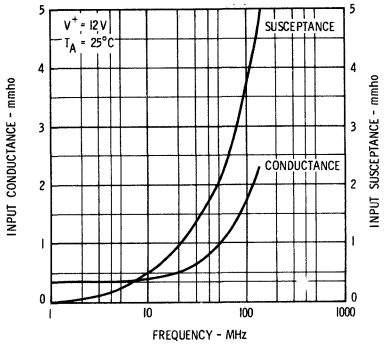
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current	e_{in} = 0	2.1	2.5	3.1	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	4.0			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV rms, f ≤ 1kHz	29	35		mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz		0.30	0.43	mmho
Input Capacitance	e_{in} < 10 mV rms, f ≤ 5 MHz		7.0	16.0	pF
Output Capacitance	f ≤ 5 MHz		2.0	3.0	pF
Output Conductance	e_o ≤ 100mVrms, f ≤ 5MHz		0.02	0.04	mmho
Noise Figure	f = 30 MHz, R_s = 500 Ω		6.5		dB
	f = 100 MHz, R_s = 500 Ω		8.0		dB
The following specifications apply for -55°C ≤ T_A ≤ +125°C					
Quiescent Output Current	e_{in} = 0	1.7		3.1	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV rms, f ≤ 1kHz	21			mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz			1.2	mmho
Output Conductance	e_o ≤ 100mVrms, f ≤ 5MHz			0.05	mmho

TYPICAL PERFORMANCE CURVES

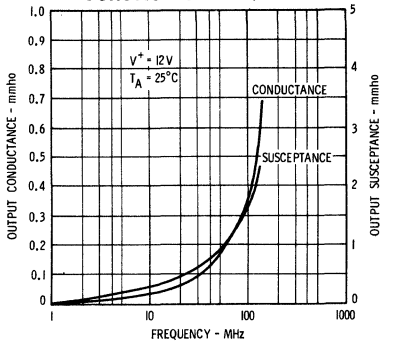
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



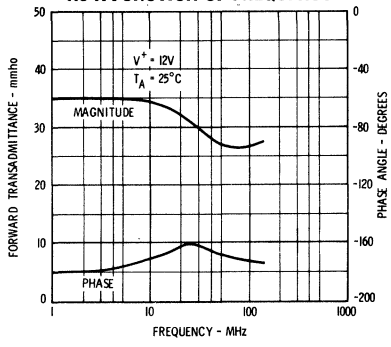
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY

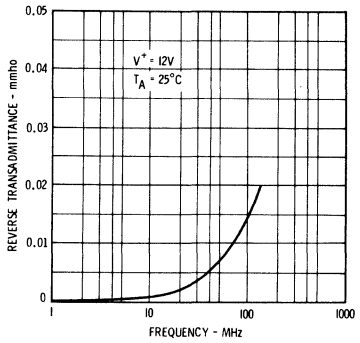


FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

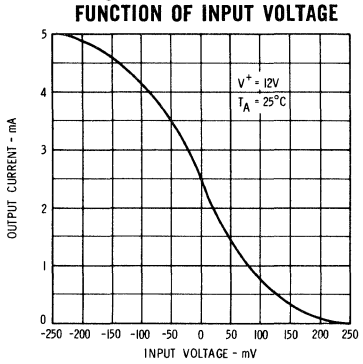


TYPICAL PERFORMANCE CURVES

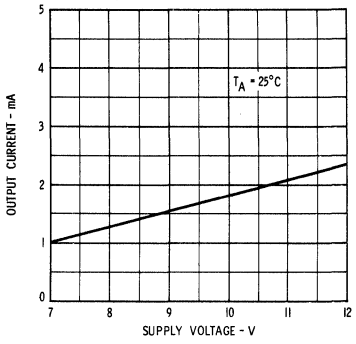
MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



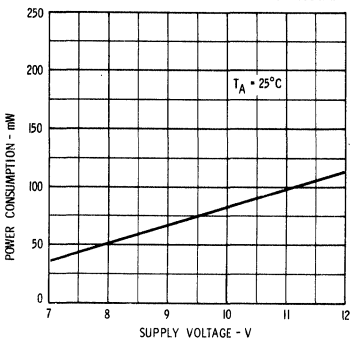
OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



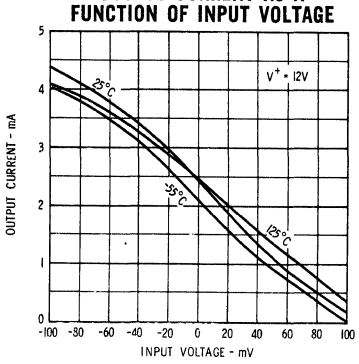
OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



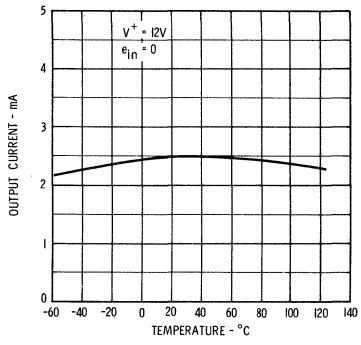
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



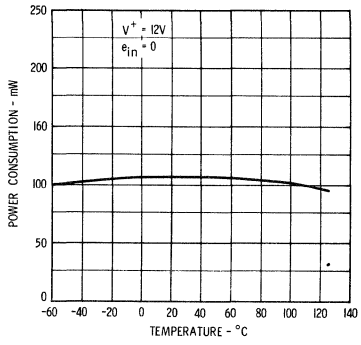
OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



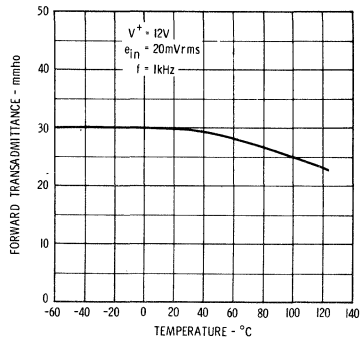
OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



TRANSADMITTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITION OF TERMS

POWER CONSUMPTION - The DC power required to operate the device with no signal applied.

QUIESCENT OUTPUT CURRENT - The DC current delivered to the load with the input terminals short-circuited.

PEAK-TO-PEAK OUTPUT CURRENT - The short-circuit output current excursion for a large-signal input voltage.

OUTPUT SATURATION VOLTAGE - The minimum voltage to which the output collector may be reduced without degrading circuit performance.

TRANSADMITTANCE - The ratio of the output current to the input voltage.

INPUT ADMITTANCE - The admittance between the input terminals with the output short-circuited.

OUTPUT ADMITTANCE - The admittance between the output terminals with the input short-circuited.

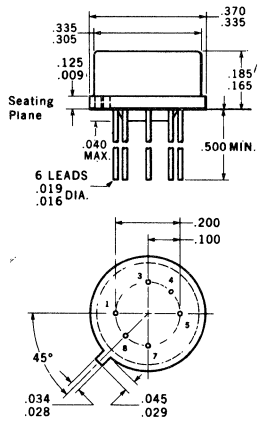
μA703C
RF-IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA703C is an RF-IF amplifier constructed on a single silicon chip and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device. For full range operation (-55°C to +125°C) see μA703 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering - 60 second)	300°C

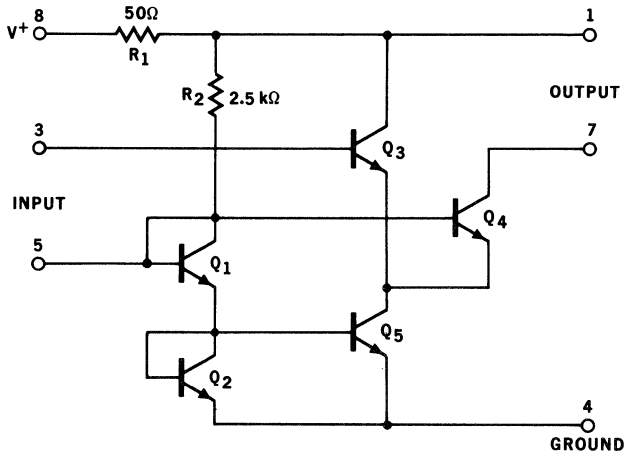
PHYSICAL DIMENSIONS



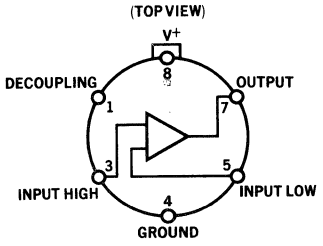
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.27 grams

ORDER PART NO. U5D770339X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 connected to case.

NOTE 1: Rating applies for ambient temperatures to 70°C.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

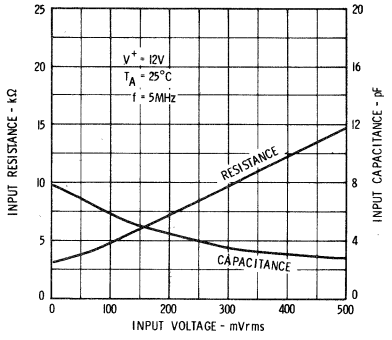
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise specified)

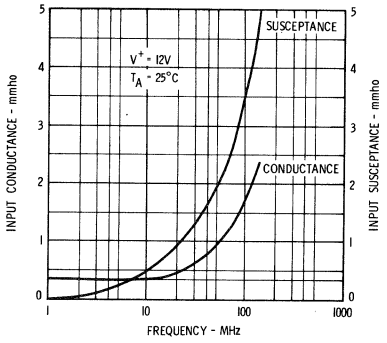
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current	e_{in} = 0	1.9	2.5	3.3	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.6			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV rms, f ≤ 1kHz	23	33		mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz		0.35	0.50	mmho
Input Capacitance	e_{in} < 10 mV rms, f ≤ 5 MHz		9.0	16.0	pF
Output Capacitance	f ≤ 5 MHz		2.0	3.0	pF
Output Conductance	e_o ≤ 100mVrms, f ≤ 5MHz			0.05	mmho
Noise Figure	f = 30 MHz, R_s = 500 Ω		6.5		dB
	f = 100 MHz, R_s = 500 Ω		8.0		dB
The following specifications apply for 0°C ≤ T_A ≤ 70°C:					
Quiescent Output Current	e_{in} = 0	1.7		3.5	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV rms f ≤ 1kHz	22			mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz			0.71	mmho
Output Conductance	e_o ≤ 100mVrms, f ≤ 5MHz			0.06	mmho

TYPICAL PERFORMANCE CURVES

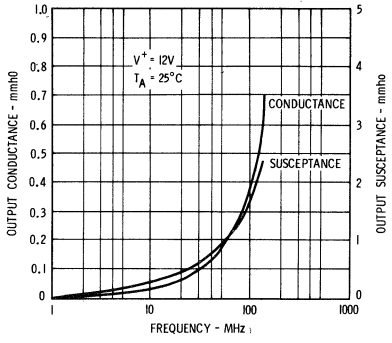
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



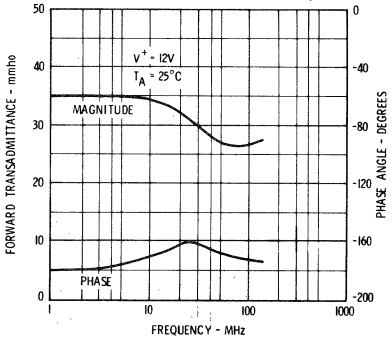
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



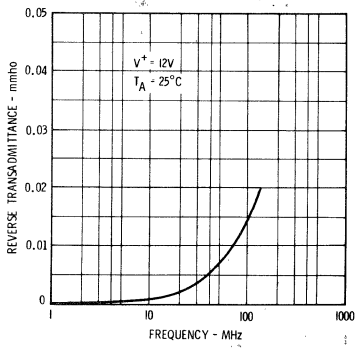
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



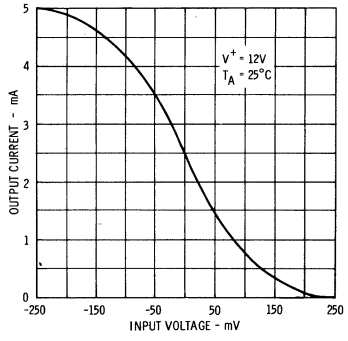
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

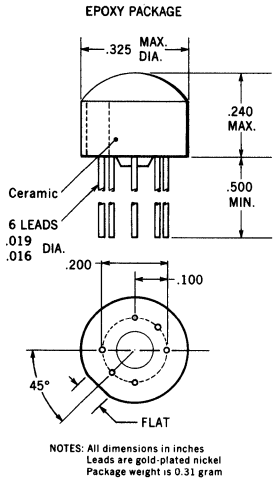


μA703E
RF-IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA703E is a linear integrated circuit with useful unneutralized power gain to frequencies in excess of 100 MHz. It features the capability of nonsaturating limiter operation with a suitable output load, making it ideally suited for FM-IF limiter applications.

Applications include FM-IF limiter-amplifier, TV sound IF amplifier, chroma reference oscillator for color TV, and fixed-gain amplifiers to 100 MHz.

PHYSICAL DIMENSIONS



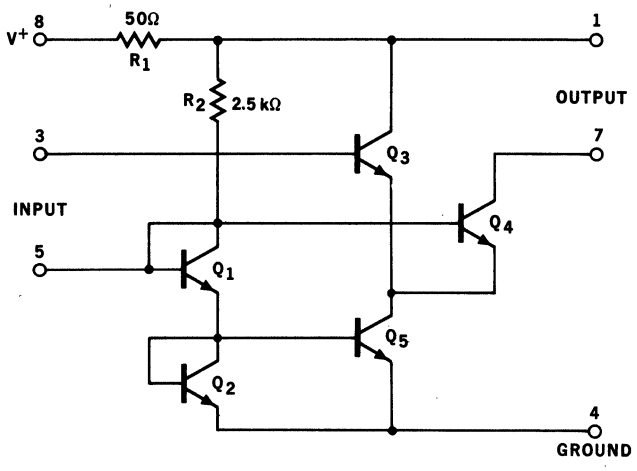
NOTES: All dimensions in inches
Leads are gold-plated nickel
Package weight is 0.31 gram

ORDER PART NO. U8B770339X

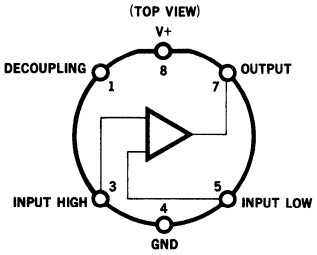
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		20 V
Output Collector Voltage		24 V
Voltage Between Input Terminals		±5.0 V
Internal Power Dissipation	(Note 1)	200 mW
Operating Temperature Range		0°C to +70°C
Storage Temperature Range		-55°C to +125°C
Lead Temperature (Soldering - 10 seconds)		260°C

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE 1: Rating applies for ambient temperatures to +70°C.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

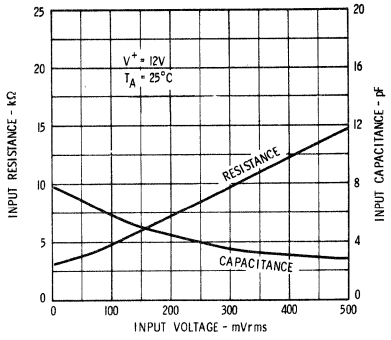
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V, f = 10.7 MHz unless otherwise specified)

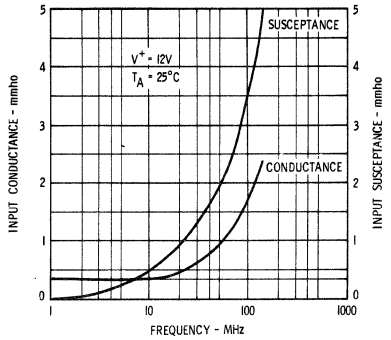
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current			2.5	3.3	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms	3.0	5.0		mA
Output Saturation Voltage			1.4	1.7	Volts
Forward Transadmittance	e_{in} = 10 mV rms	24	35		mmhos
Reverse Transadmittance			0.002		mmho
Input Conductance	e_{in} < 10 mV rms		.33	1.0	mmho
Input Capacitance	e_{in} < 10 mV rms		9.0	18.0	pF
Output Conductance			0.03	0.05	mmho
Output Capacitance			2.6	4.0	pF
Noise Figure	R_S = 500 Ω		6.0		dB
	R_S = 500 Ω, f = 100 MHz		8.0		dB
Maximum Stable Gain			40		dB

TYPICAL PERFORMANCE CURVES

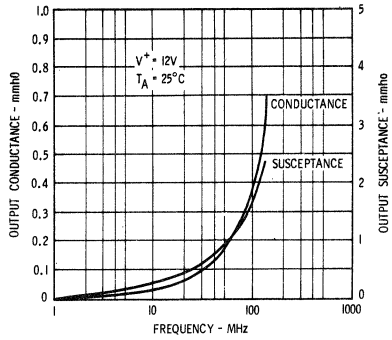
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



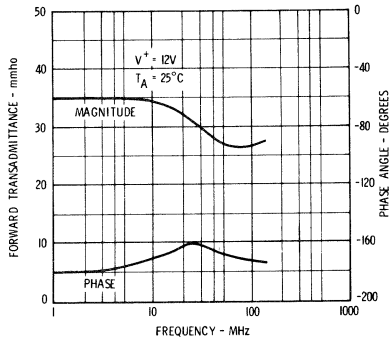
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



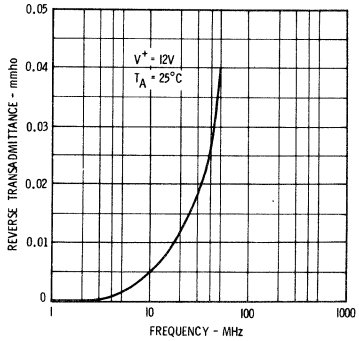
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



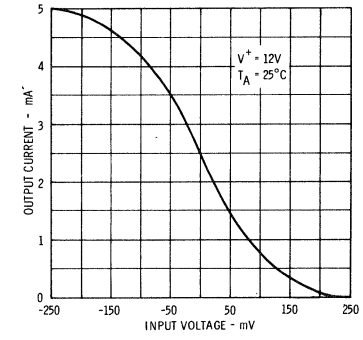
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

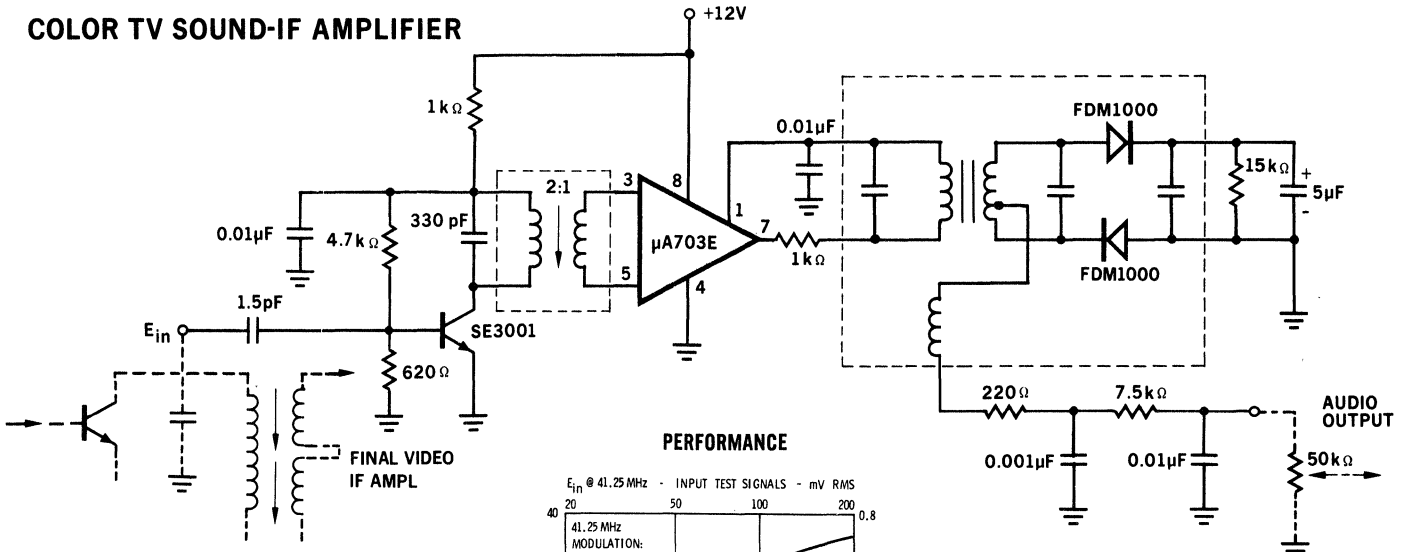


OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

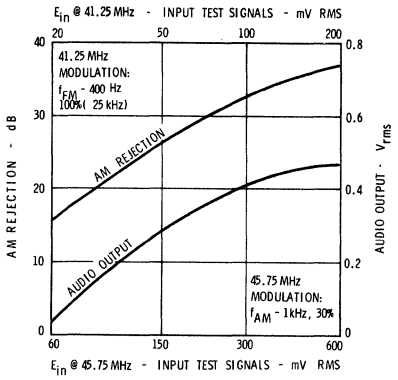


TYPICAL CIRCUIT APPLICATIONS

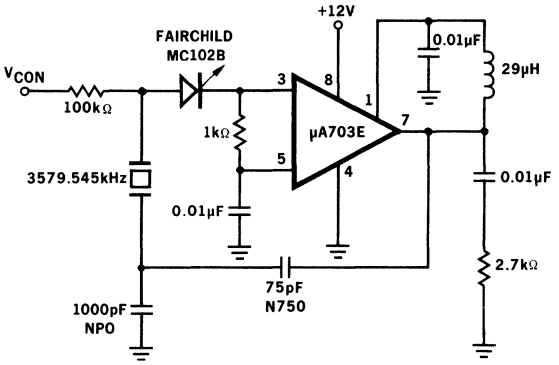
COLOR TV SOUND-IF AMPLIFIER



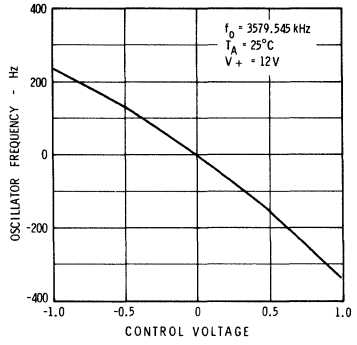
PERFORMANCE



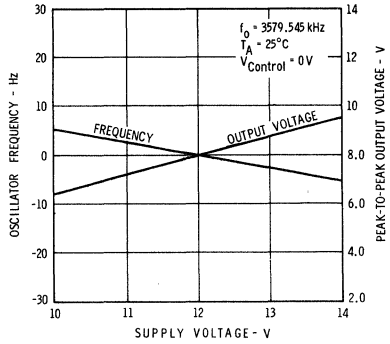
3.58-MHz VOLTAGE-CONTROLLED OSCILLATOR



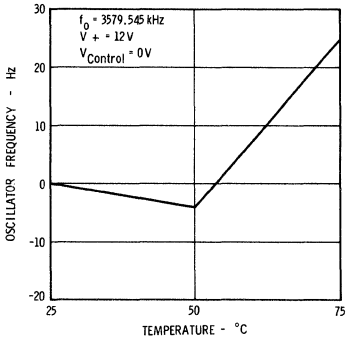
NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE



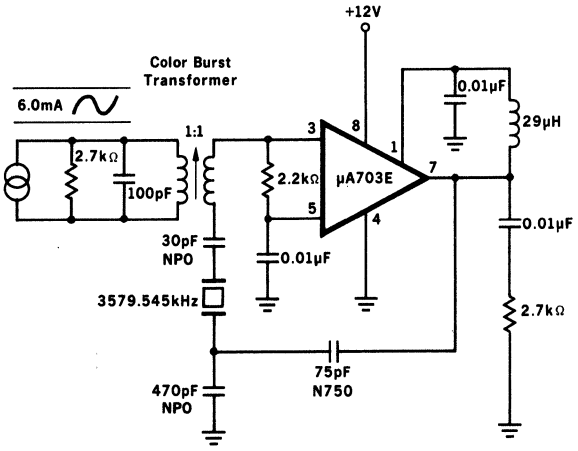
NORMALIZED OSCILLATOR FREQUENCY AND OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

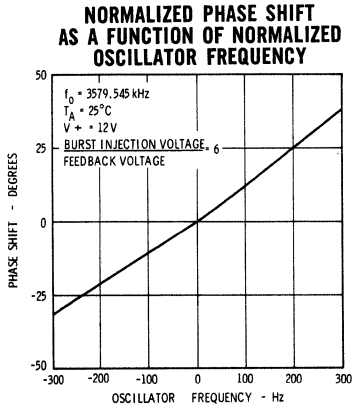


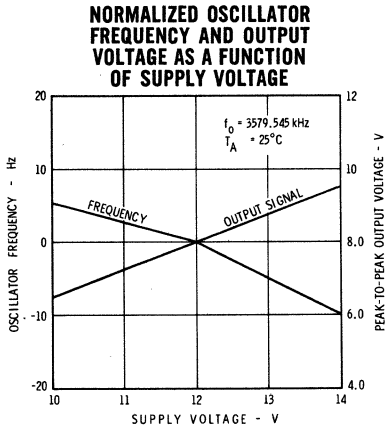
NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF AMBIENT TEMPERATURE

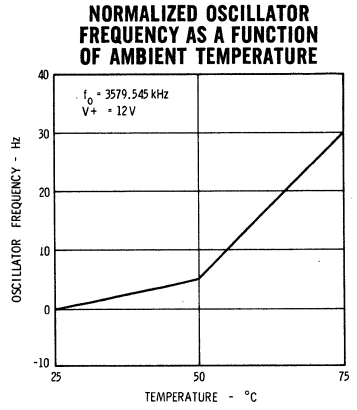


3.58-MHz INJECTION-LOCKED OSCILLATOR

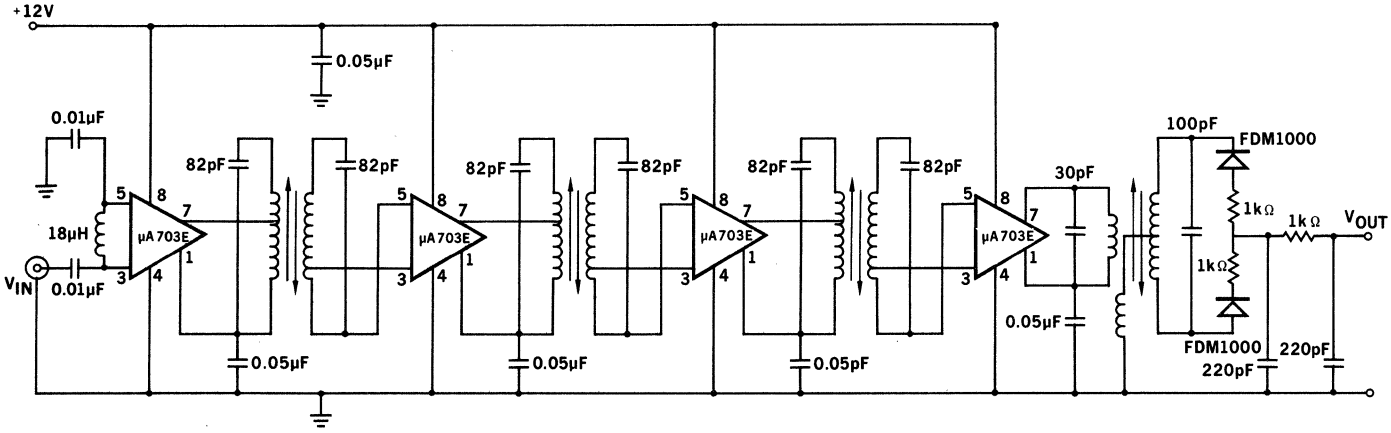








FOUR-STAGE FM-IF AMPLIFIER



Full limiting with $V_{in} < 50\mu V$.

Current consumption 27 mA.

Power gain / stage 26.5 dB.

Peak-to-Peak separation of detector 800 kHz.

THD < 0.8% with ±75 kHz deviation @ 400 Hz.

μA709

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

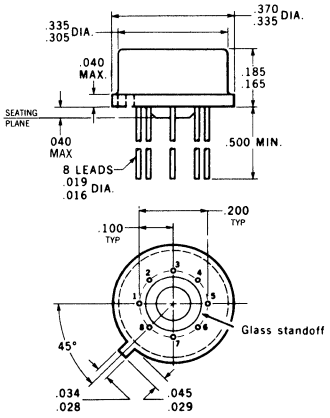
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTIONS - The μA709 is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		± 18 V
Internal Power Dissipation	TO-99 (Note 1)	300 mW
	Dual-In-Line	300 mW
Differential Input Voltage		± 5.0 V
Input Voltage		± 10 V
Output Short-Circuit Duration	(T_A = 25°C)	5 sec
Storage Temperature Range		-65°C to + 150°C
Operating Temperature Range		-55°C to + 125°C
Lead Temperature (Soldering, 60 sec)		300°C

PHYSICAL DIMENSIONS

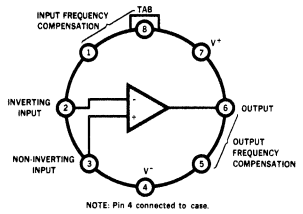


NOTES: All dimensions in inches
Dimensions as per latest J-10 committee
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B770931X

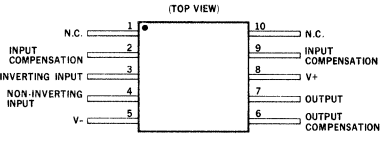
CONNECTION DIAGRAMS

(Top View)



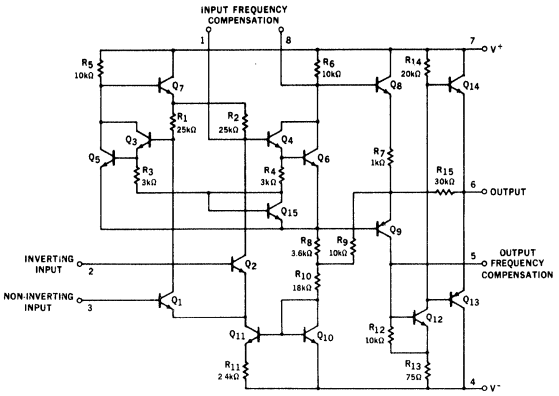
TO-99

(TOP VIEW)

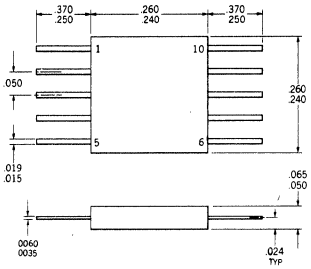


FLAT-PAK

SCHEMATIC DIAGRAM



TYPICAL FLAT PACKAGE



NOTES: All dimensions in inches

ORDER PART NO. U3F770931X

NOTES:

1. Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.
2. Rating applies for case temperatures to +125°C; derate linearly at 2.5 mW/°C for ambient temperatures above +30°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

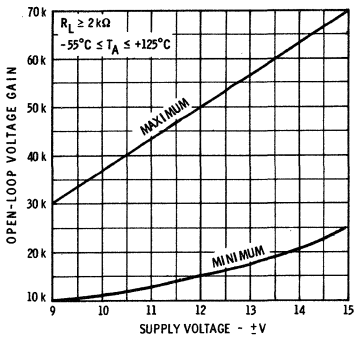
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified)

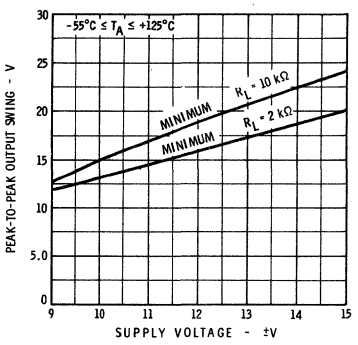
Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10\,k\Omega$		1.0	5.0	mV
Input Offset Current			50	200	nA
Input Bias Current			200	500	nA
Input Resistance		150	400		kΩ
Output Resistance			150		Ω
Power Consumption	V_S = ±15 V		80	165	mW
Transient Response	V_{in} = 20 mV, R_L = 2 kΩ,				
Risetime	C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50 Ω		0.3	1.0	μs
Overshoot	$C_L \leq 100$ pF		10	30	%
The following specifications apply for	-55°C ≤ T_A ≤ +125°C:				
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50 Ω		3.0		μV/°C
	$R_S \leq 10$ kΩ		6.0		μV/°C
Large-Signal Voltage Gain	V_S = ±15 V, $R_L \geq 2$ kΩ, V_{out} = ±10 V	25,000	45,000	70,000	
Output Voltage Swing	V_S = ±15 V, $R_L \geq 10$ kΩ	±12	±14		V
	V_S = ±15 V, $R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range	V_S = ±15 V	±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	150	μV/V
Input Offset Current	T_A = +125°C		20	200	nA
	T_A = -55°C		100	500	nA
Input Bias Current	T_A = -55°C		0.5	1.5	μA
Input Resistance		40	100		kΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

VOLTAGE GAIN

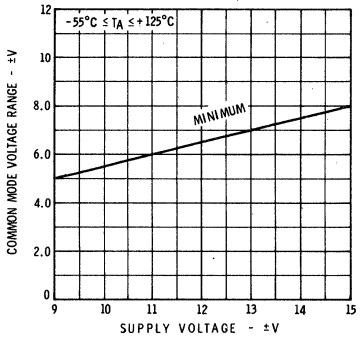


OUTPUT VOLTAGE SWING

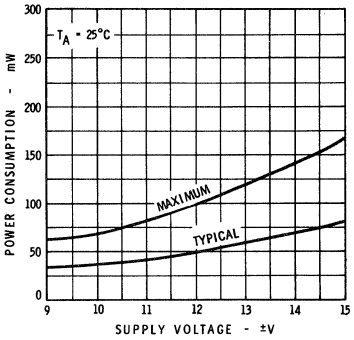


GUARANTEED ELECTRICAL CHARACTERISTICS (CONT'D)

INPUT COMMON MODE VOLTAGE RANGE

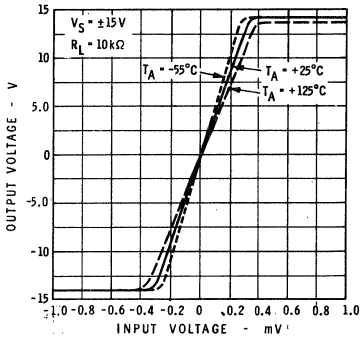


POWER CONSUMPTION

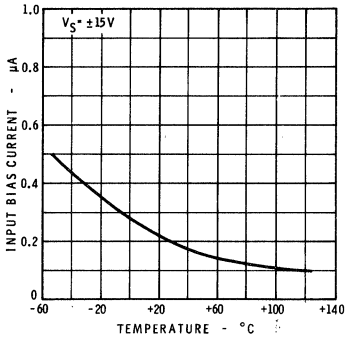


TYPICAL PERFORMANCE CURVES

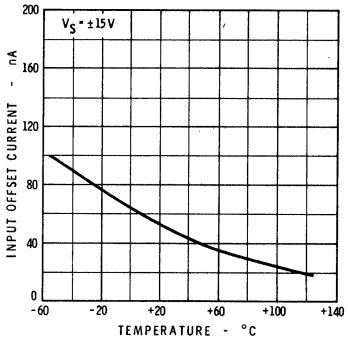
VOLTAGE TRANSFER CHARACTERISTIC



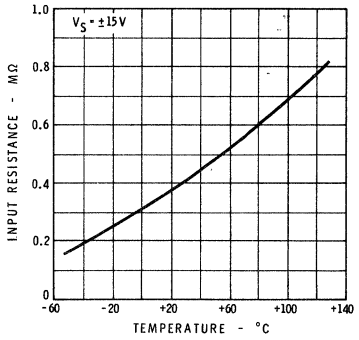
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



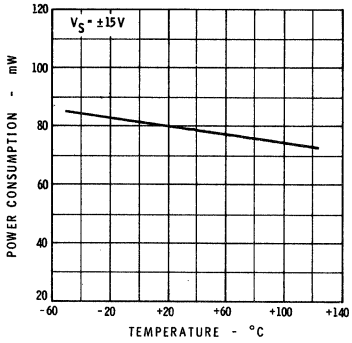
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



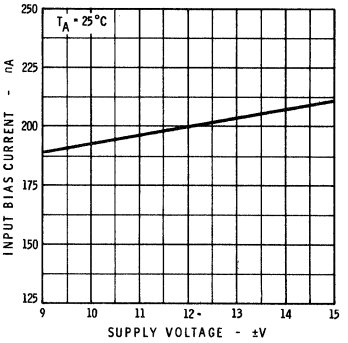
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



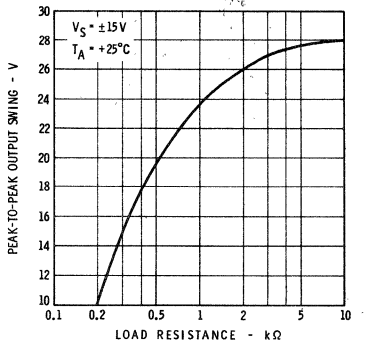
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



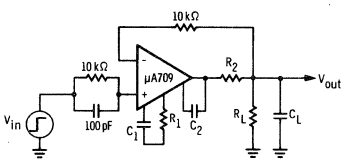
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



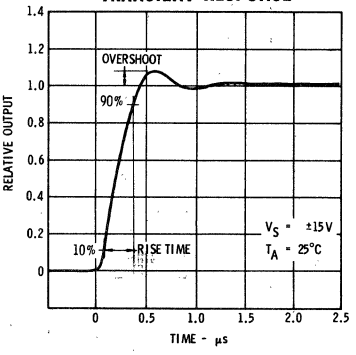
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

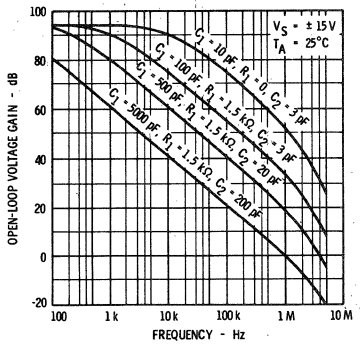
POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

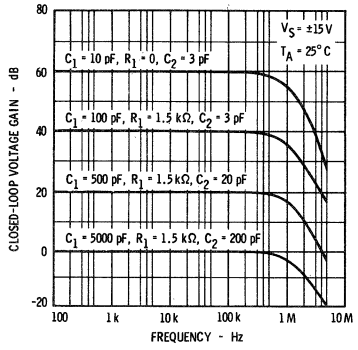
TRANSIENT RESPONSE - The closed-loop step function response of the amplifier under small-signal conditions.

TYPICAL PERFORMANCE CURVES

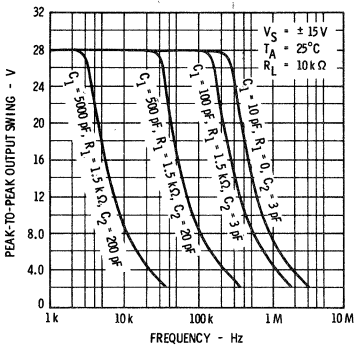
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



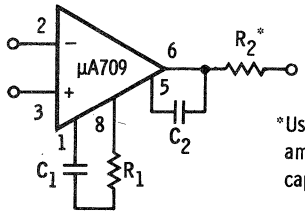
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



FREQUENCY COMPENSATION CIRCUIT



*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

μA709A

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **2 mV MAXIMUM OFFSET VOLTAGE**
- **50 nA MAXIMUM OFFSET CURRENT**
- **GUARANTEED DRIFT CHARACTERISTICS**

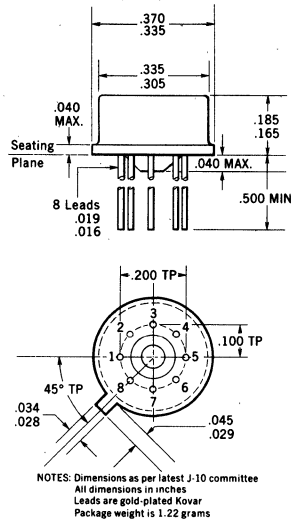
GENERAL DESCRIPTION — The μA709A is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load, and low power consumption. The device displays exceptional temperature stability and will operate over a 14-36 V range of total supply voltage with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, low-level instrumentation applications, and for the generation of special linear and nonlinear transfer functions. Although it features improved performance, the μA709A is a direct plug-in replacement for the μA709 operational amplifier.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage	36 V
Internal Power Dissipation TO-99 (Note 1)	300 mW
Flat Package (Note 2)	300 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Output Short-Circuit Duration ($T_A = +25°C$)	5 sec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

PHYSICAL DIMENSIONS

in accordance with JEDEC(TO-99) outline

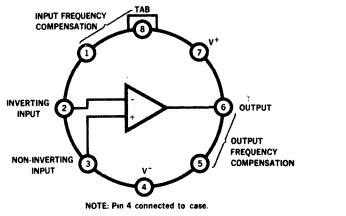


NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7709311

CONNECTION DIAGRAMS

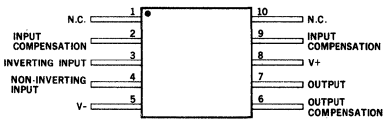
(Top View)



NOTE: Pin 4 connected to case.

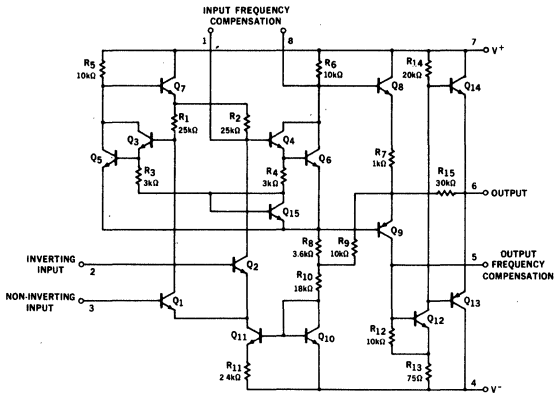
TO-5

(TOP VIEW)

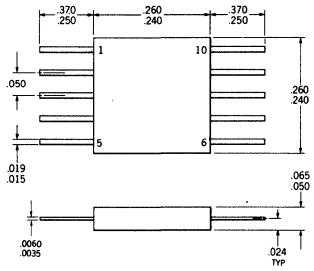


FLAT-PAK

SCHEMATIC DIAGRAM



FLAT PACKAGE



NOTES: All dimensions in inches

ORDER PART NO. U3F7709311

*Planar is a patented Fairchild process.

NOTES:
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.
(2) Rating applies for case temperatures to +125°C; derate linearly for ambient temperatures above +30°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

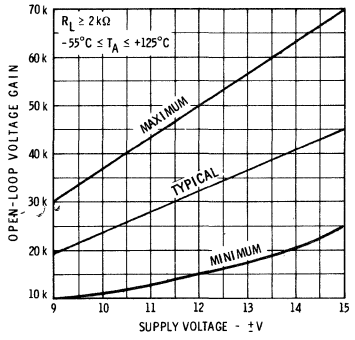
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9\,V \leq V_S \leq \pm 15\,V$ unless otherwise specified)

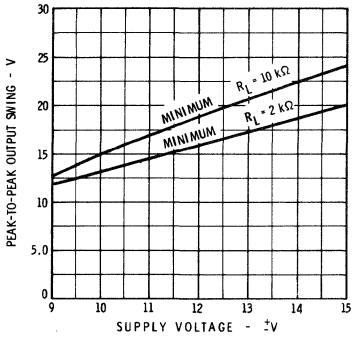
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$		0.6	2.0	mV
Input Offset Current			10	50	nA
Input Bias Current			100	200	nA
Input Resistance		350	700		kΩ
Output Resistance			150		Ω
Supply Current	$V_S = \pm 15\,V$		2.5	3.6	mA
Power Consumption	$V_S = \pm 15\,V$		75	108	mW
Transient Response	$V_S = \pm 15\,V$, $V_{in} = 20\,mV$, $R_L = 2\,k\Omega$, $C_1 = 5\,nF$, $R_1 = 1.5\,k\Omega$, $C_2 = 200\,pF$, $R_2 = 50\,\Omega$				
Risetime				1.5	μs
Overshoot	$C_L \leq 100\,pF$			30	%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\,\Omega$, $T_A = +25°C$ to $T_A = +125°C$		1.8	10	μV/°C
	$R_S = 50\,\Omega$, $T_A = +25°C$ to $T_A = -55°C$		1.8	10	μV/°C
	$R_S = 10\,k\Omega$, $T_A = +25°C$ to $T_A = +125°C$		2.0	15	μV/°C
	$R_S = 10\,k\Omega$, $T_A = +25°C$ to $T_A = -55°C$		4.8	25	μV/°C
Input Offset Current	$T_A = +125°C$		3.5	50	nA
	$T_A = -55°C$		40	250	nA
Average Temperature Coefficient of Input Offset Current	$T_A = +25°C$ to $T_A = +125°C$		0.08	0.5	nA/°C
	$T_A = +25°C$ to $T_A = -55°C$		0.45	2.8	nA/°C
Input Bias Current	$T_A = -55°C$		300	600	nA
Input Resistance	$T_A = -55°C$	85	170		kΩ
Input Voltage Range	$V_S = \pm 15\,V$	±8.0			V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	80	110		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		40	100	μV/ V
Large-Signal Voltage Gain	$V_S = \pm 15\,V$, $R_L \geq 2\,k\Omega$, $V_{out} = \pm 15\,V$	25,000		70,000	
Output Voltage Swing	$V_S = \pm 15\,V$, $R_L \geq 10\,k\Omega$	±12	±14		V
	$V_S = \pm 15\,V$, $R_L \geq 2\,k\Omega$	±10	±13		V
Supply Current	$T_A = +125°C$, $V_S = \pm 15\,V$		2.1	3.0	mA
	$T_A = -55°C$, $V_S = \pm 15\,V$		2.7	4.5	mA
Power Consumption	$T_A = +125°C$, $V_S = \pm 15\,V$		63	90	mW
	$T_A = -55°C$, $V_S = \pm 15\,V$		81	135	mW

GUARANTEED ELECTRICAL CHARACTERISTICS

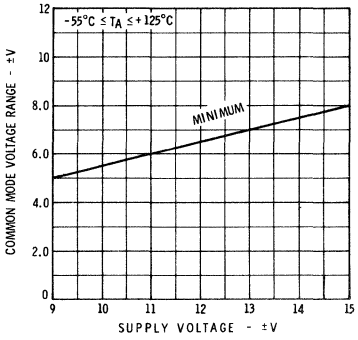
VOLTAGE GAIN



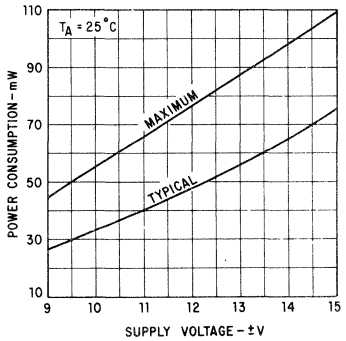
OUTPUT VOLTAGE SWING



INPUT COMMON MODE VOLTAGE RANGE

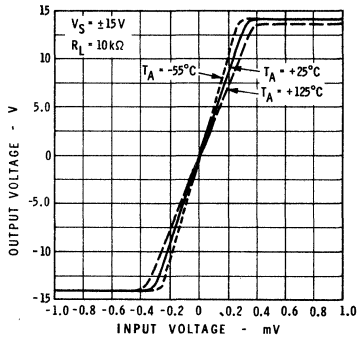


POWER CONSUMPTION

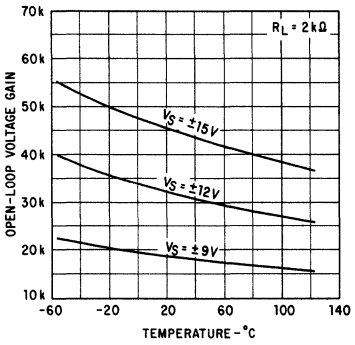


TYPICAL PERFORMANCE CURVES

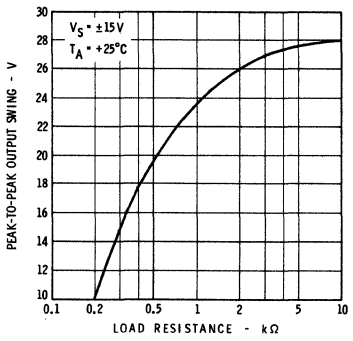
VOLTAGE TRANSFER CHARACTERISTIC



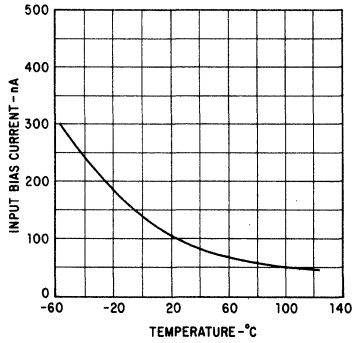
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



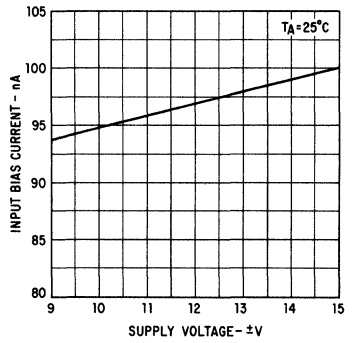
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



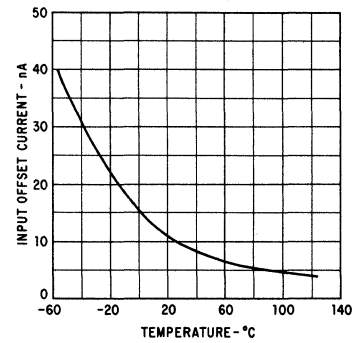
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



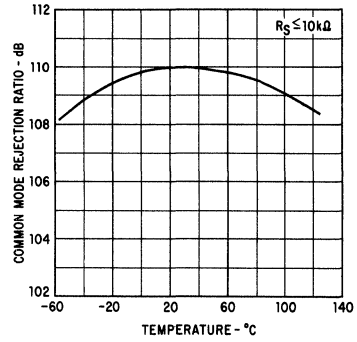
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



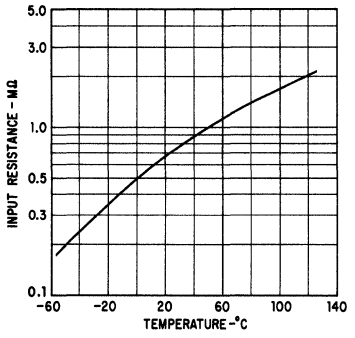
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



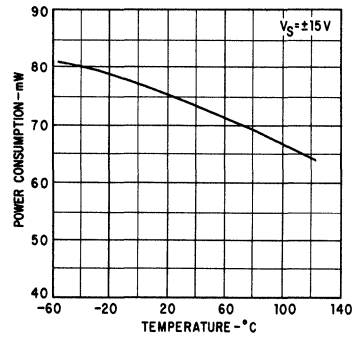
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



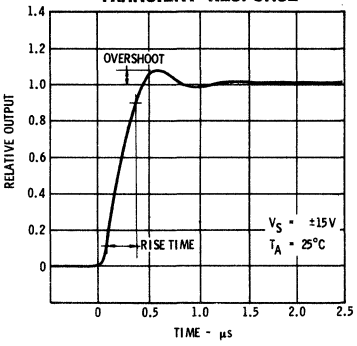
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



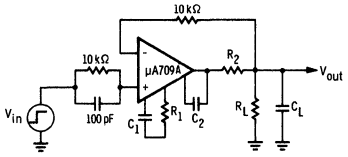
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



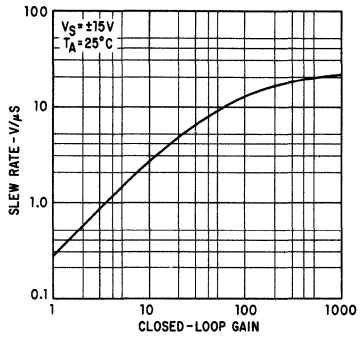
TRANSIENT RESPONSE



TRANSIENT RESPONSE TEST CIRCUIT



SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

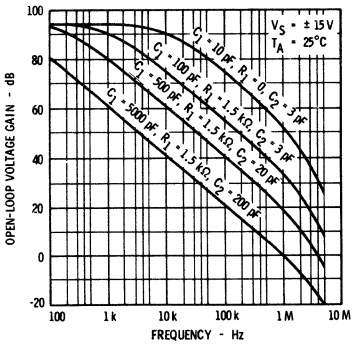
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

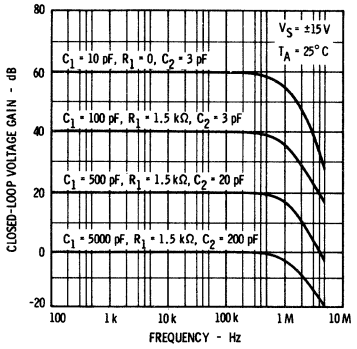
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

TYPICAL PERFORMANCE CURVES

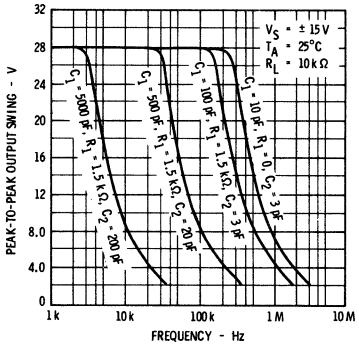
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



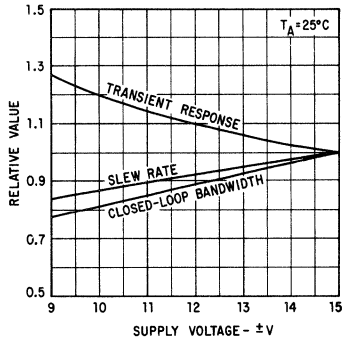
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



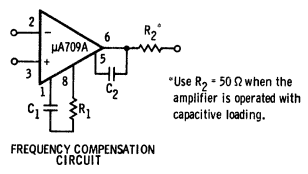
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

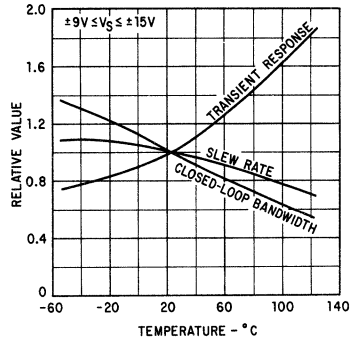


FREQUENCY COMPENSATION CIRCUIT



FREQUENCY COMPENSATION CIRCUIT

FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



μA709B

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

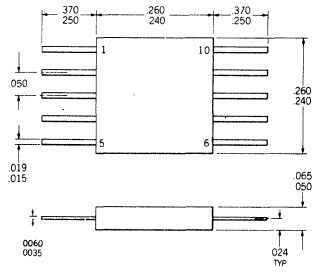
GENERAL DESCRIPTION — The μA709B is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For improved specifications, see μA709A or μA709 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Output Short-Circuit Duration ($T_A = 25°C$)	5 sec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

PHYSICAL DIMENSIONS

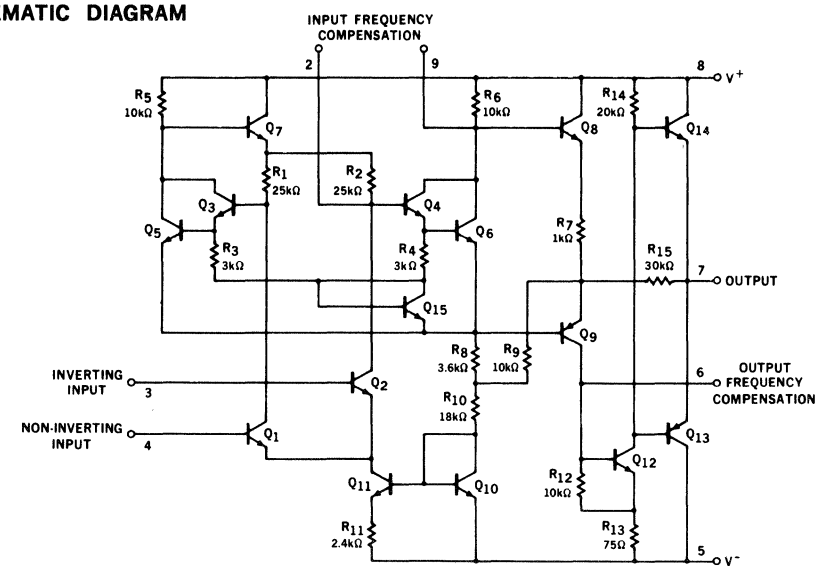
(TYPICAL FLAT PACKAGE)



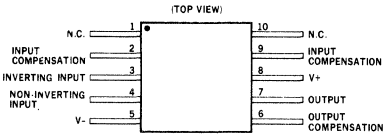
NOTES: All dimensions in inches

ORDER PART NO. U3F7709313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



*Planar is a patented Fairchild process.

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 2.5 mW/°C for ambient temperatures above +60°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

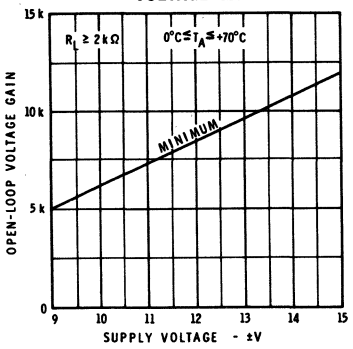
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

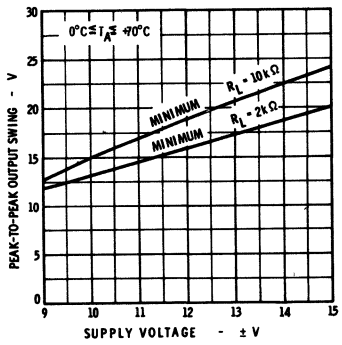
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	200	μV/V
Power Consumption			80	200	mW
Transient Response	$V_{in} = 20$ mV, $R_L = 2$ kΩ,				
Risetime	$C_1 = 5000$ pF, $R_1 = 1.5$ kΩ, $C_2 = 200$ pF, $R_2 = 50$ Ω		0.3		μs
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	12,000			
Input Resistance		35			kΩ
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V			12.5	mV
Input Offset Current				1.2	μA
Input Bias Current				3.0	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	10,000			

GUARANTEED ELECTRICAL CHARACTERISTICS

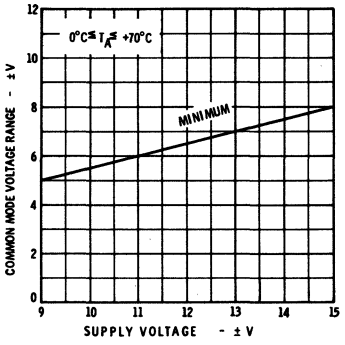
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

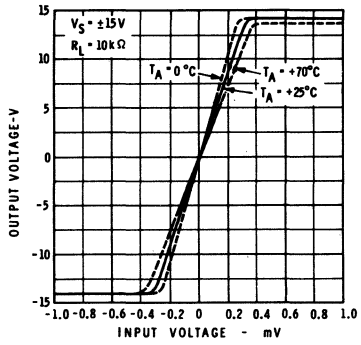


INPUT COMMON MODE VOLTAGE RANGE

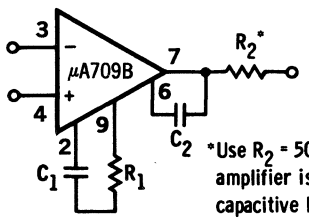


TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

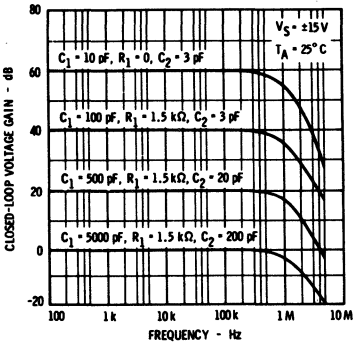


FREQUENCY COMPENSATION CIRCUIT



*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



μA709C

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

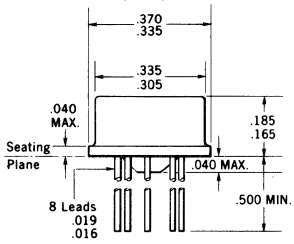
GENERAL DESCRIPTION - The μA709C is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For full temperature range operation (-55°C to +125°C) see μA709 or μA709A data sheet.

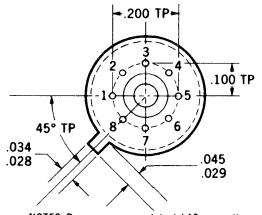
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		± 18 V
Internal Power Dissipation	(Note 1)	250 mW
Differential Input Voltage		± 5.0 V
Input Voltage		± 10 V
Output Short-Circuit Duration	(T_A = 25°C)	5 sec
Storage Temperature Range	TO-99	-65°C to + 150°C
	Dual-In-Line	-55°C to +125°C
Operating Temperature Range		0°C to +70°C
Lead Temperature	TO-99 (Soldering, 60 sec)	300°C
	Dual-In-Line (Soldering, 10 sec)	260°C

PHYSICAL DIMENSIONS

in accordance with JEDEC(TO-99) outline

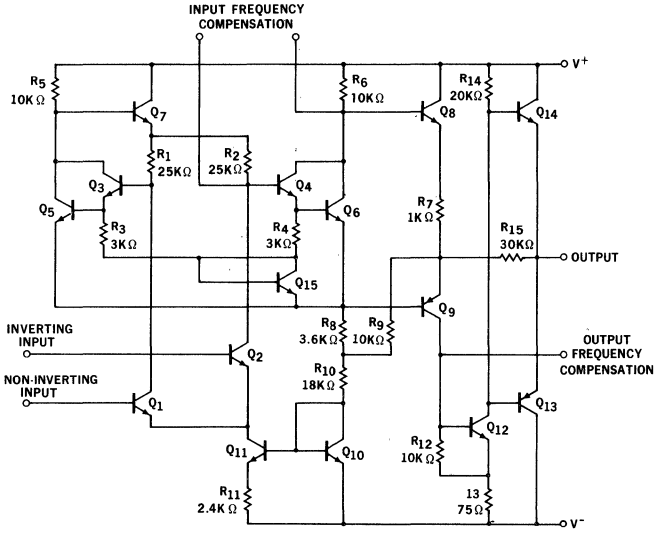




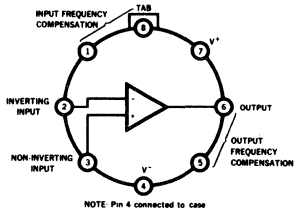
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO.
U5B770939X

SCHEMATIC DIAGRAM

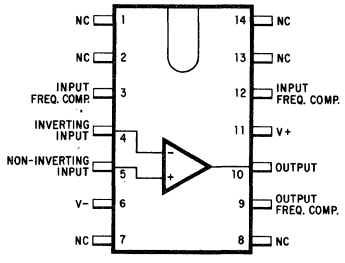


CONNECTION DIAGRAM

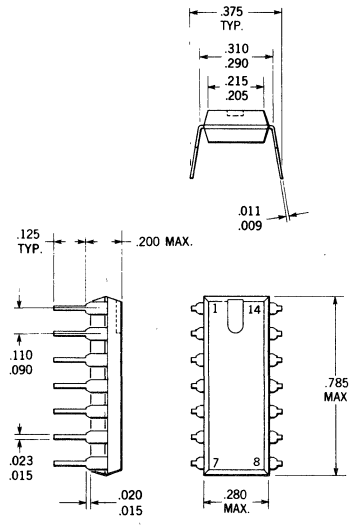


(Top View)

CONNECTION DIAGRAM



PHYSICAL DIMENSIONS



NOTES: All dimensions in inches

ORDER PART NO.
U6E7709393

NOTE 1: Rating applies for ambient temperatures to +70°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

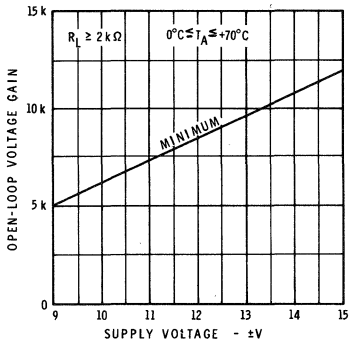
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

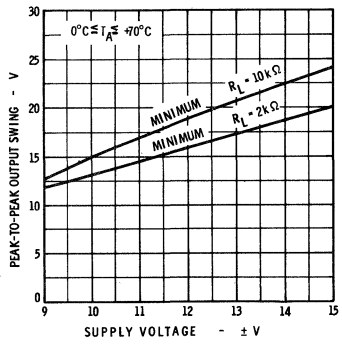
Parameter	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10\,k\Omega$, ±9 V $\leq V_S \leq$ ±15 V		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, V_{out} = ±10 V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10\,k\Omega$	±12	±14		V
	$R_L \geq 2\,k\Omega$	±10	±13		V
Input Voltage Range		±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		25	200	μV/V
Power Consumption			80	200	mW
Transient Response	V_{in} = 20 mV, R_L = 2 kΩ,				
Risetime	C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50 Ω		0.3		μs
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 10k\Omega$, ±9 V $\leq$ ±15 V			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10 V	12,000			
Input Resistance		35			kΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

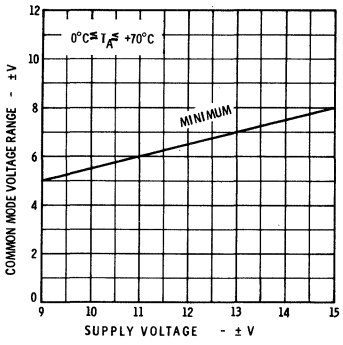
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

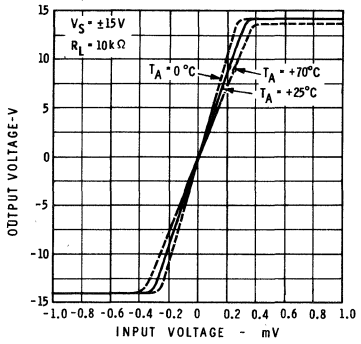


INPUT COMMON MODE VOLTAGE RANGE

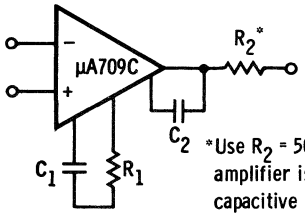


TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

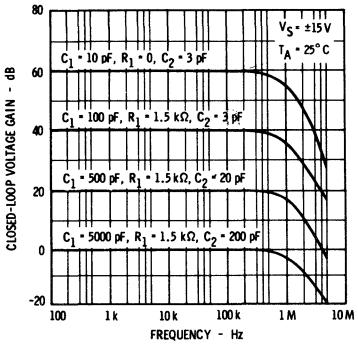


FREQUENCY COMPENSATION CIRCUIT



*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



μA710

HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

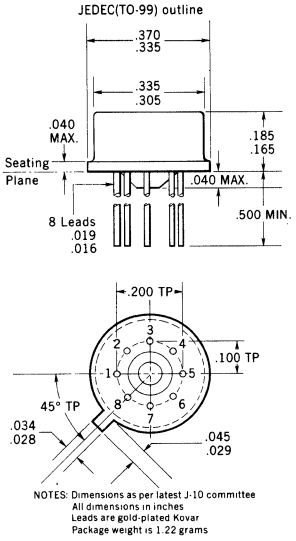
- **IMPROVED SPECIFICATIONS**
- **2 mV MAXIMUM OFFSET VOLTAGE**
- **3 μA MAXIMUM OFFSET CURRENT**
- **1250 MINIMUM VOLTAGE GAIN**
- **10 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION — The μA710 is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage		+14.0 V
Negative Supply Voltage		−7.0 V
Peak Output Current		10 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Internal Power Dissipation		
TO-99	[Note 1]	300 mW
Flat Package	[Note 2]	200 mW
Operating Temperature Range		−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

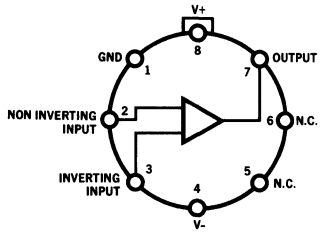
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.22 grams

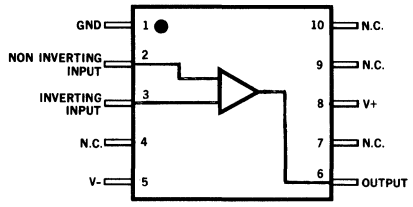
ORDER PART NO.
U5B771031X

TO-99 CONNECTION DIAGRAM
(TOP VIEW)

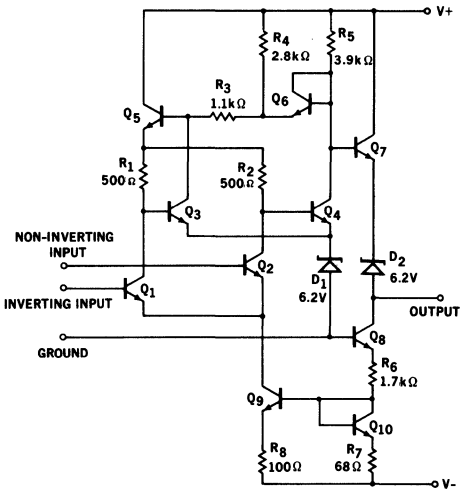


Note: Pin 4 connected to case.

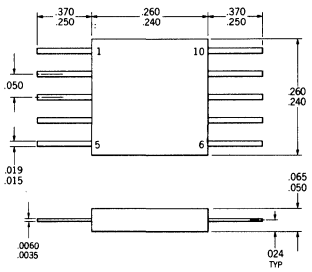
FLAT PACKAGE CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



NOTES: All dimensions in inches

ORDER PART NO. U3F771031X

Notes on page 2

* Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 4)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	2.0	2.5		mA
Response Time [Note 3]			40		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ to $T_A = +125°C$ $R_S = 50\Omega$, $T_A = 25°C$ to $T_A = -55°C$		3.5 2.7	10 10	μV/°C μV/°C
Input Offset Current	$T_A = +125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$ $T_A = 25°C$ to $T_A = -55°C$		5.0 15	25 75	nA/°C nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		1000			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5	1.7		mA
	$T_A = -55°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

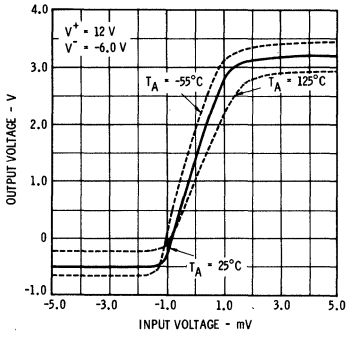
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

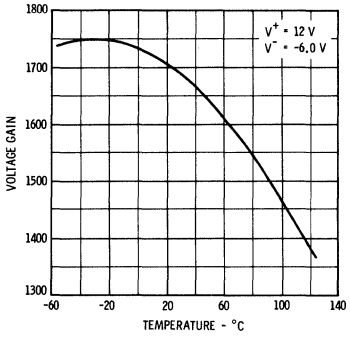
(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

TYPICAL PERFORMANCE CURVES

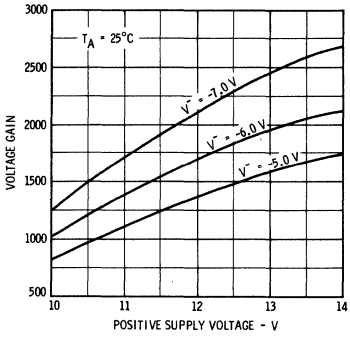
VOLTAGE TRANSFER CHARACTERISTIC



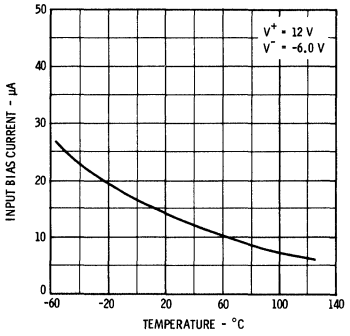
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



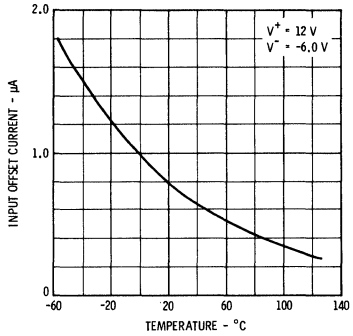
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



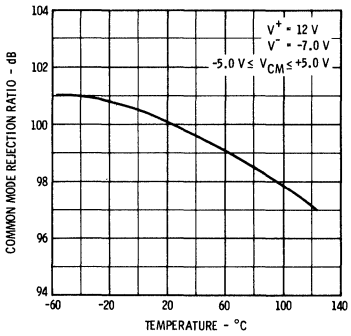
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



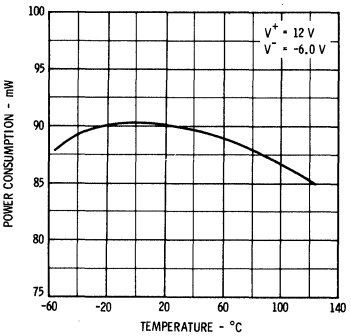
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



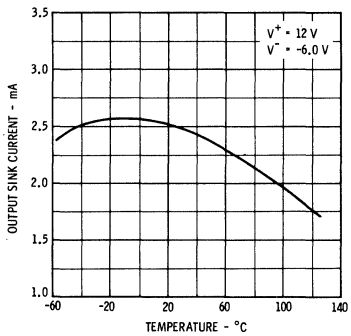
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



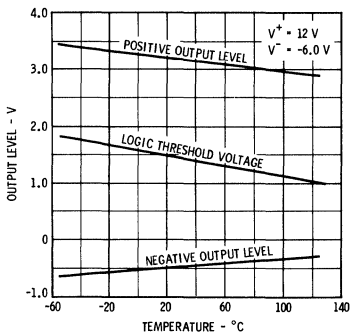
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



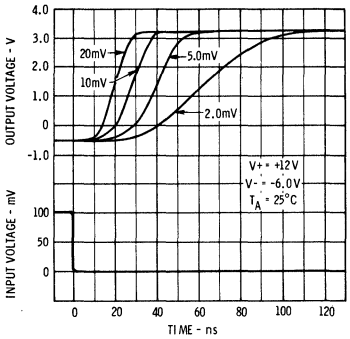
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



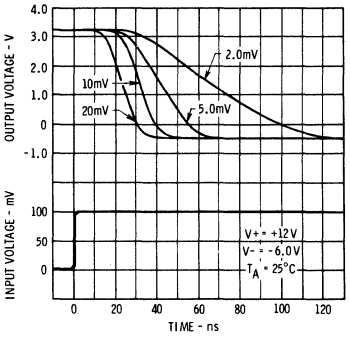
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



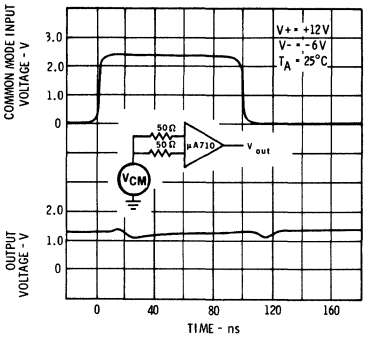
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

μA710B

HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **5 μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

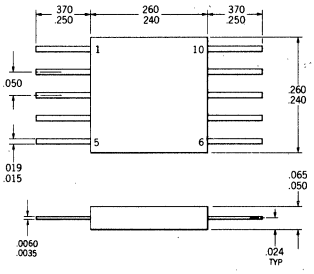
GENERAL DESCRIPTION — The μA710B is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

For improved specifications, see μA710 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

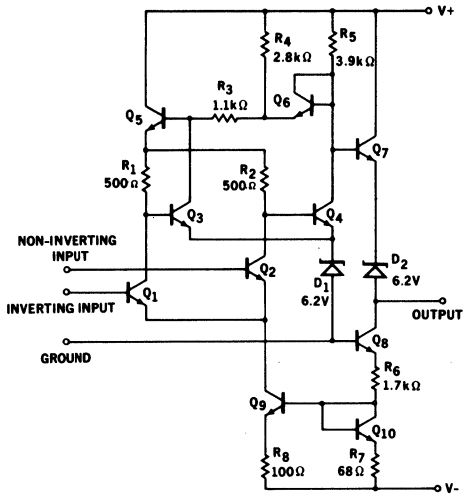
PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



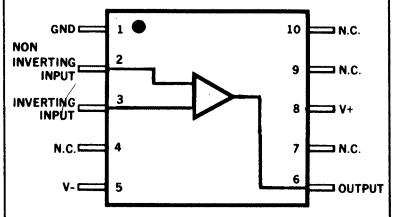
NOTES: All dimensions in inches

ORDER PART NO. U3F7710313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

*Planar is a patented Fairchild process.

Notes on page 2

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ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		15	50	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		24	100	nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Voltage Gain		800			
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5			mA
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			7.5	mV
Input Offset Current	$T_A = +125°C$		0.9	5.0	μA
	$T_A = -55°C$		3.8	15	μA
Input Bias Current	$T_A = -55°C$		34	80	μA
Input Voltage Range	$V^- = -7.0$ V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		500			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

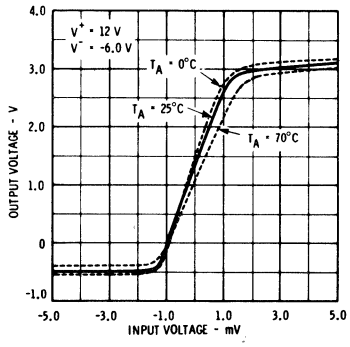
(1) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

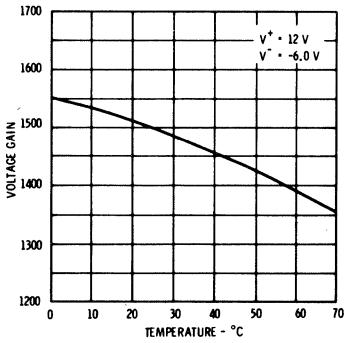
(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C, and 1.0V at +125°C.

TYPICAL PERFORMANCE CURVES

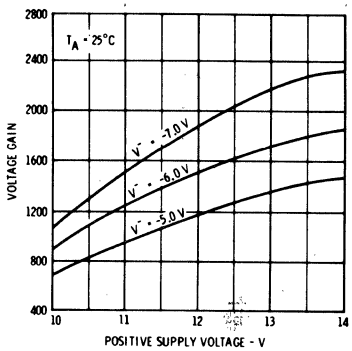
VOLTAGE TRANSFER CHARACTERISTIC



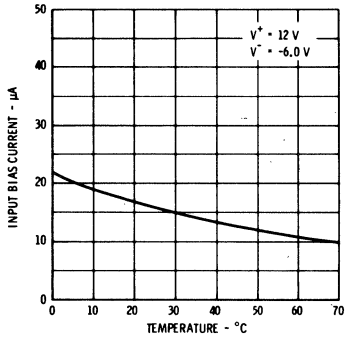
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



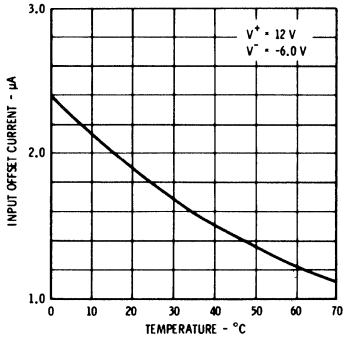
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



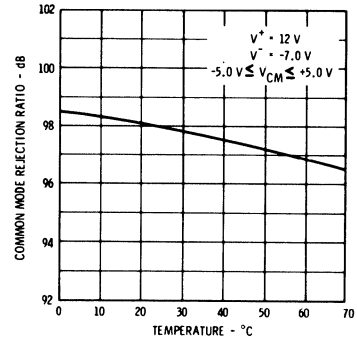
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



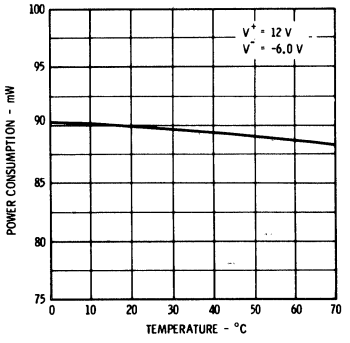
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



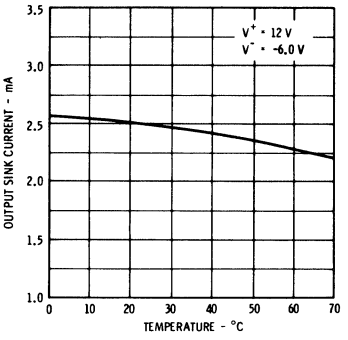
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



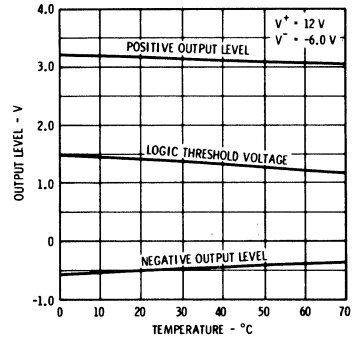
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



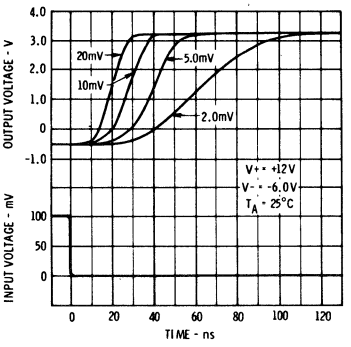
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



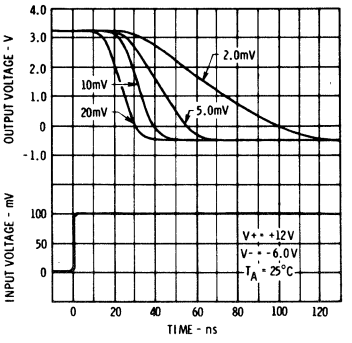
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



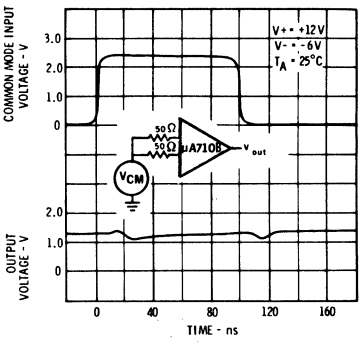
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

μA710C

HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

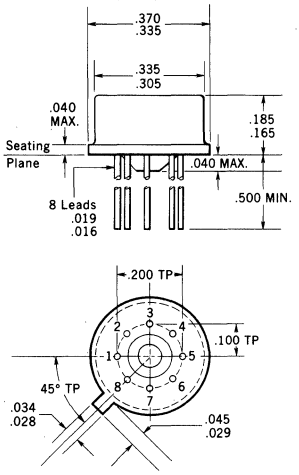
- **IMPROVED SPECIFICATIONS**
- **5mV MAXIMUM OFFSET VOLTAGE**
- **5μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION— The μA710C is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.
For full temperature range operation (−55°C to +125°C) see μA710 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation [Note 1]	300 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range TO-99	−65°C to +150°C
Dual-In-Line	−55°C to +125°C
Lead Temperature TO-99 (Soldering, 60 sec)	300°C
Dual-In-Line (Soldering, 10 sec)	260°C

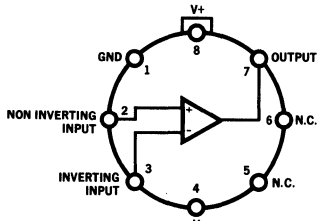
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

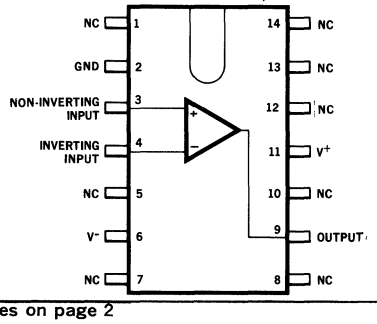
ORDER PART NO.U5B771039X

TO-99 CONNECTION DIAGRAM
(TOP VIEW)

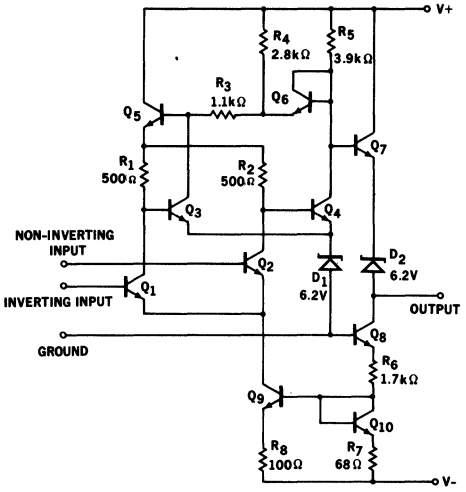


Note: Pin 4 connected to case

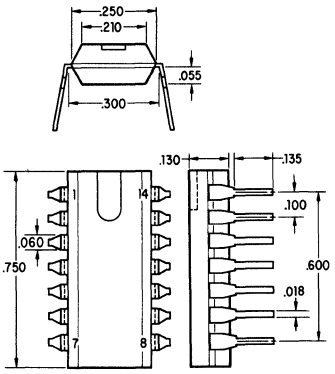
CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

ORDER PART NO.
U6E7710393

Notes on page 2

* Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.6	2.5		mA
Response Time [Note 2]			40		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 200\Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$ $T_A = 25°C$ to $T_A = 0°C$		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5			mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

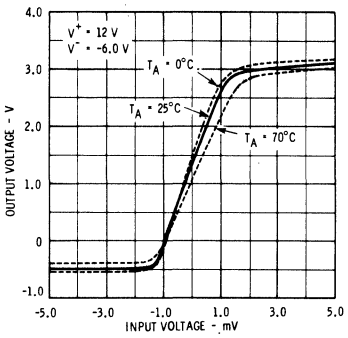
(1) Ratings apply for ambient temperatures to +70°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

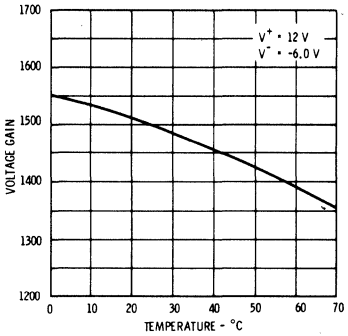
(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

TYPICAL PERFORMANCE CURVES

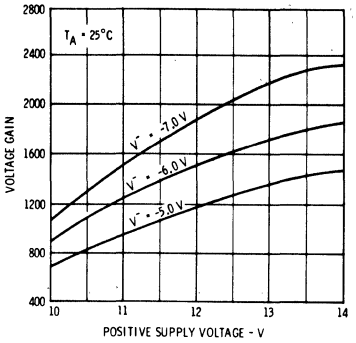
VOLTAGE TRANSFER CHARACTERISTIC



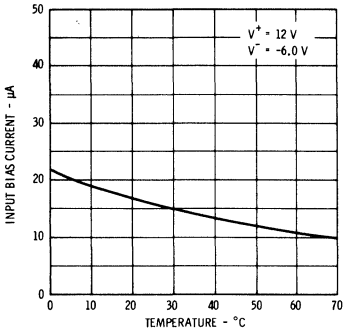
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



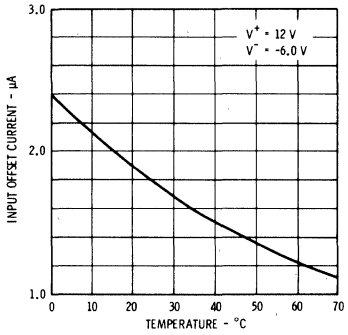
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



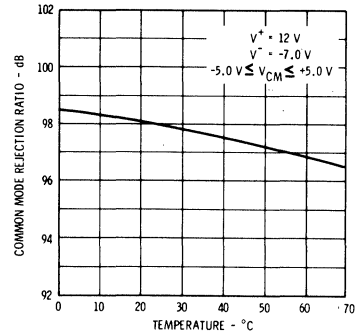
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



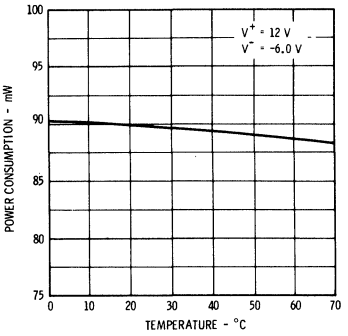
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



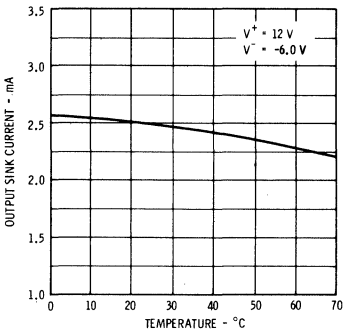
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



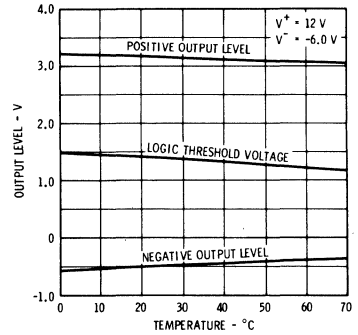
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



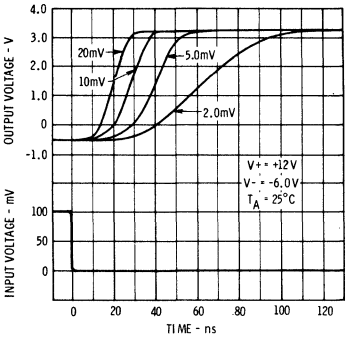
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



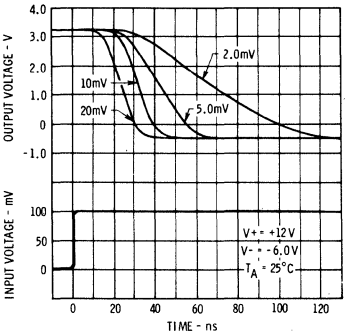
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



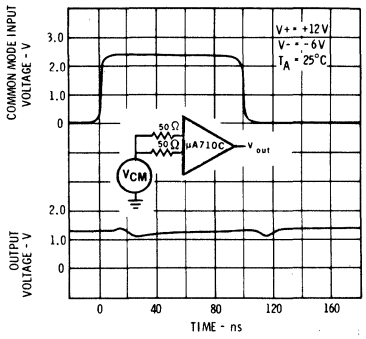
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



DEFINITIONS

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OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

μA711
DUAL COMPARATOR

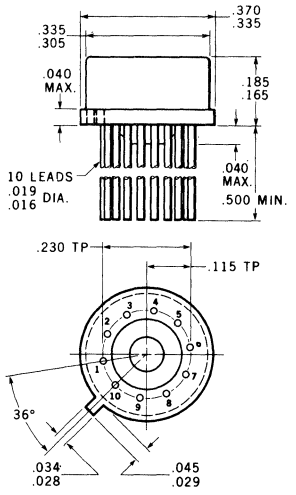
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA711 is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar* epitaxial process.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage		+14.0 V
Negative Supply Voltage		-7.0 V
Peak Output Current		50 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Strobe Voltage		0 to +6.0 V
Internal Power Dissipation TO - 100	(Note 1)	300 mW
Flat-Package	(Note 2)	300 mW
Operating Temperature Range		-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

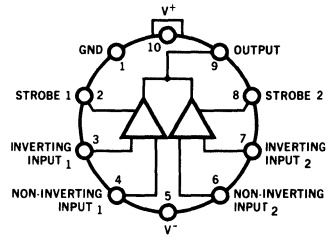
PHYSICAL DIMENSIONS



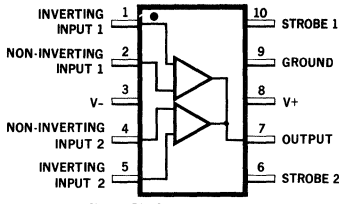
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NO. U5F771131X

CONNECTION DIAGRAM



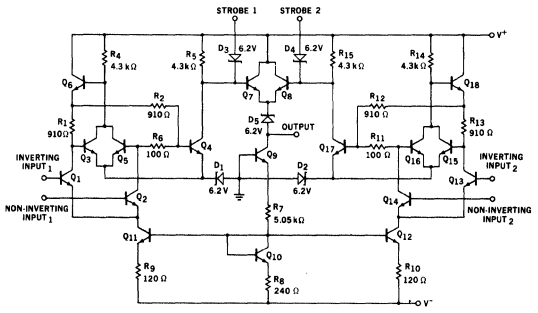
TO-100



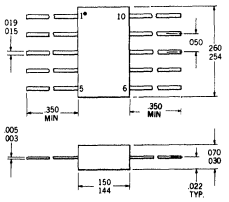
Note: Pin 3 is connected to case.

FLAT-PAK

SCHEMATIC DIAGRAM



FLAT PACKAGE



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Notes on page 2

* Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$, V_{CM} = 0		1.0	3.5	mV
	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$		1.0	5.0	mV
Input Offset Current	V_{out} = +1.4 V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 3)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = -7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 100 mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW
The following specifications apply for -55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage (Note 4)	$R_S \leq 200\,\Omega$, V_{CM} = 0			4.5	mV
	$R_S \leq 200\,\Omega$			6.0	mV
Input Offset Current (Note 4)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

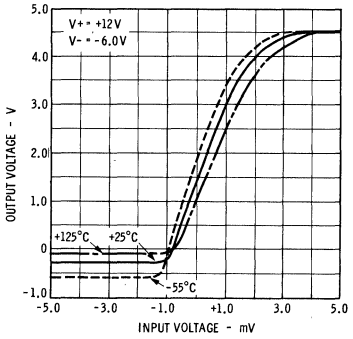
(2) Rating applies for case temperatures to +125°C; derate linearly at 2.5 mW/°C for ambient temperatures above +40°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

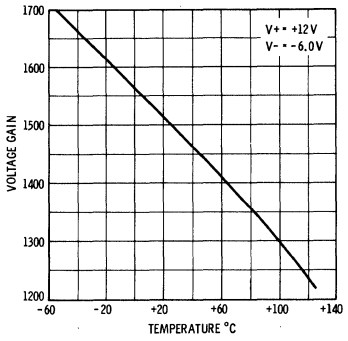
(4) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1.0 V at +125°C.

TYPICAL PERFORMANCE CURVES

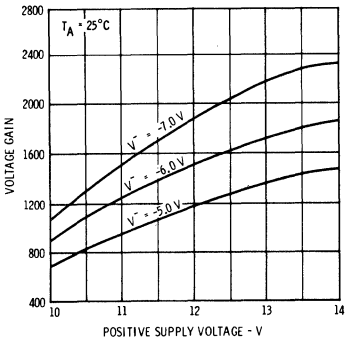
VOLTAGE TRANSFER CHARACTERISTIC



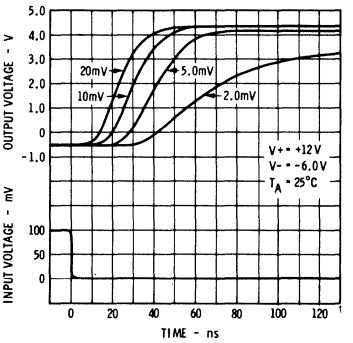
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



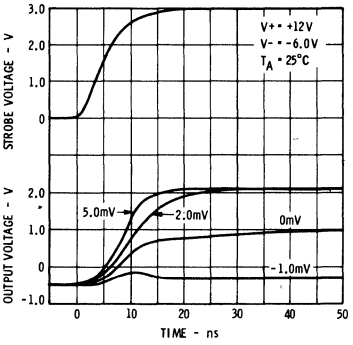
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



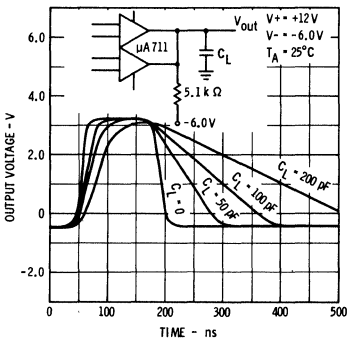
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



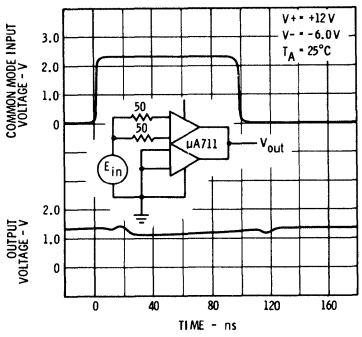
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



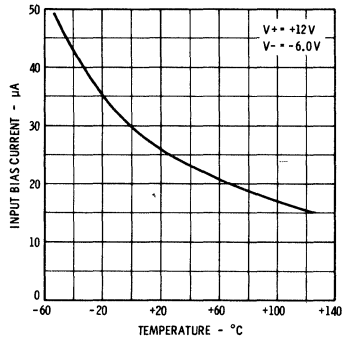
OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



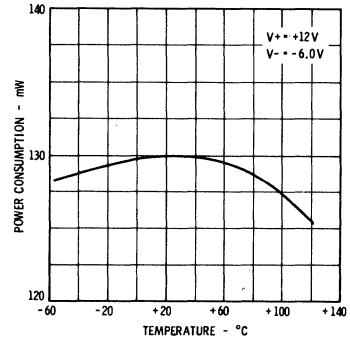
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents.

INPUT VOLTAGE RANGE* - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* - The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* - The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

μA711C
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

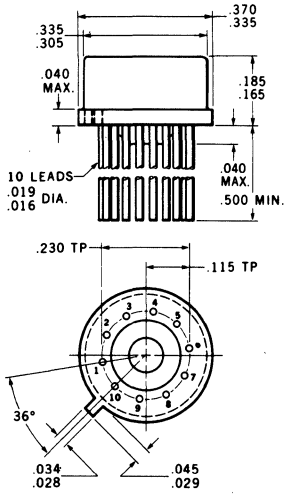
GENERAL DESCRIPTION - The μA711C is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The μA711C, which is similar to the μA710C differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar epitaxial process.

For full temperature range operation (-55°C to +125°C) see μA711 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage		+14.0 V
Negative Supply Voltage		-7.0 V
Peak Output Current		50 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Strobe Voltage		0 to +6.0 V
Internal Power Dissipation	TO - 100 (Note 1)	300 mW
	Flat-Package (Note 2)	300 mW
Operating Temperature Range		0°C to +70°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

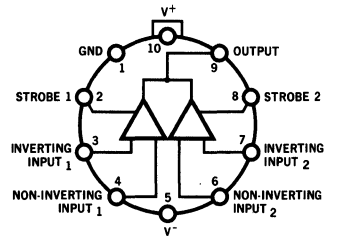
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) outline



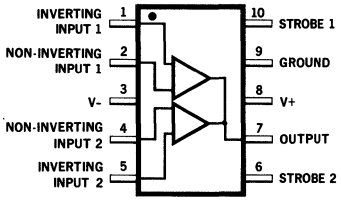
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F771139X

CONNECTION DIAGRAMS



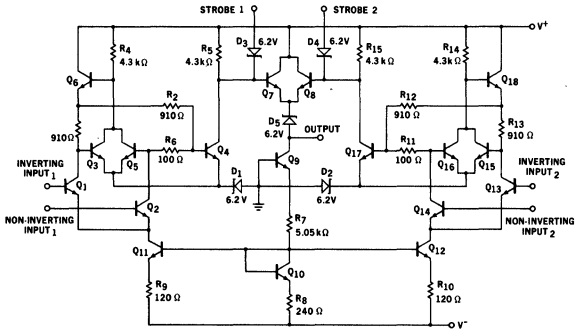
TO-100



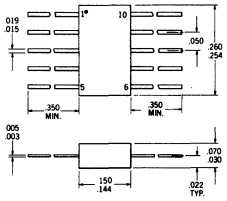
Note: Pin 3 is connected to case.

FLAT-PAK

SCHEMATIC DIAGRAM



FLAT PACKAGE



ORDER PART NO. U3T771139X

Notes on page 2

* Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max	Units
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$, V_{CM} = 0		1.0	5.0	mV
	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$		1.0	7.5	mV
Input Offset Current	V_{out} = +1.4 V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 3)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = -7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 100 mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	230	mW
The following specifications apply for 0°C $\leq T_A \leq$ +70°C:					
Input Offset Voltage (Note 4)	$R_S \leq 200\,\Omega$, V_{CM} = 0			6.0	mV
	$R_S \leq 200\,\Omega$			10	mV
Input Offset Current (Note 4)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

(1) Rating applies for ambient temperatures to +70°C.

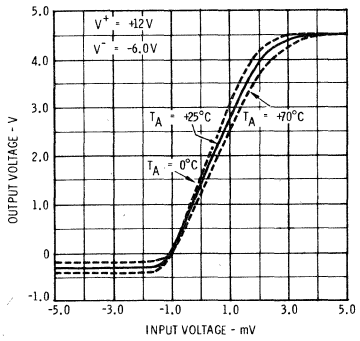
(2) Rating applies for case temperatures to + 70 °C; derate linearly at 2. 5 mW/°C for ambient temperatures above +40°C.

(3) The response time specified is for a 100-mV input step with 5-mV overdrive.

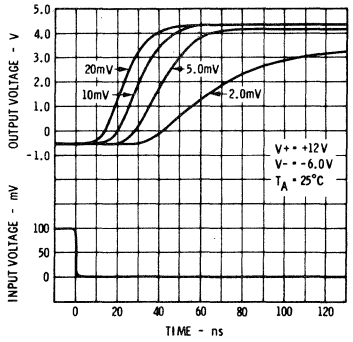
(4) The input offset voltage is specified for a logic threshold voltage of 1.5 V at 0°C, 1.4 V at +25°C and 1.2 V at +70°C.

TYPICAL ELECTRICAL CHARACTERISTICS

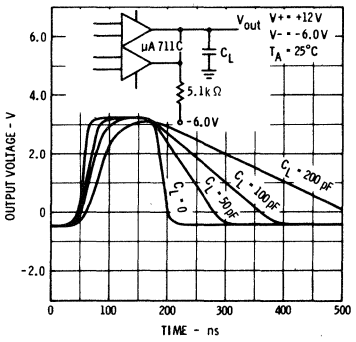
VOLTAGE TRANSFER CHARACTERISTIC



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



μA716

FIXED-GAIN, LOW DISTORTION AMPLIFIER

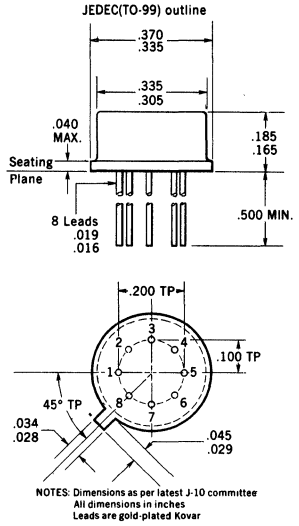
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA716 is a fixed-gain, medium power amplifier intended for use as a telephone system channel amplifier, headset amplifier or a general-purpose audio preamplifier. It provides medium output current capability, low distortion, excellent gain stability, and wide bandwidth. Fixed voltage gains of 10, 20, 100, and 200 are available by selecting external taps.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	27 V
Internal Power Dissipation (Note 1)	400 mW
Input Voltage	± 5 V
Peak Output Current ($T_A = 25°C$)	100 mA
Storage Temperature Range	− 65°C to + 150°C
Operating Temperature Range	− 55°C to + 125°C
Lead Temperature (soldering, 60 seconds)	300°C

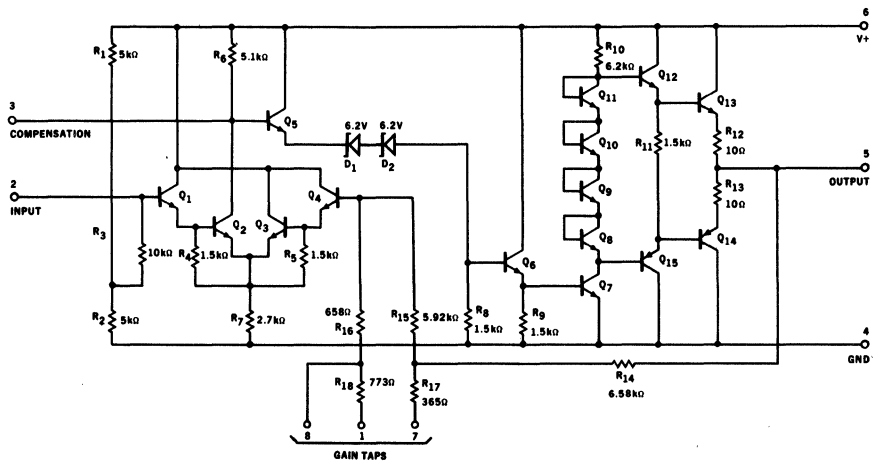
PHYSICAL DIMENSIONS
similar to
JEDEC(TO-99) outline



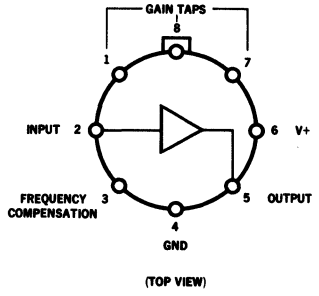
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar

ORDER PART NO. U5K7716312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 internally connected to case.

NOTE 1: Rating applies for case temperatures to +125°C; derate linearly at 8.4 mW/°C for ambient temperature above +110°C.

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FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

DEFINITION OF TERMS

Quiescent Power Consumption — The DC power required to operate the amplifier with no signal applied at the input and the load current equal to zero.

Total Harmonic Distortion — The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

Input Noise Voltage — The noise voltage at the output of the amplifier, divided by the amplifier voltage gain.

Output Voltage Swing — The maximum output voltage that may be obtained at the output of the amplifier before saturation occurs.

Input Resistance — The small-signal resistance seen looking into the input terminal of the amplifier.

Voltage Gain — The ratio of the small-signal output voltage to the input voltage of the amplifier.

Temperature Stability of Voltage Gain — The maximum variation of the voltage gain over the specified temperature range.

μA716C

FIXED-GAIN, LOW DISTORTION AMPLIFIER

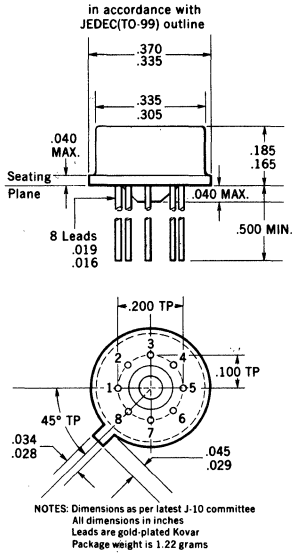
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA716C is a fixed-gain, medium power amplifier intended for use as a telephone system channel amplifier, headset amplifier or general purpose audio amplifier. It provides medium output current capability, low distortion, excellent gain stability, and wide bandwidth. Fixed voltage gains of 10, 20, 100 and 200 are available by selecting external taps.

ABSOLUTE MAXIMUM RATINGS:

Supply Voltage	27 V
Internal Power Dissipation	600 mW
Input Voltage	±5 V
Peak Output Current ($T_A = 25°C$)	100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

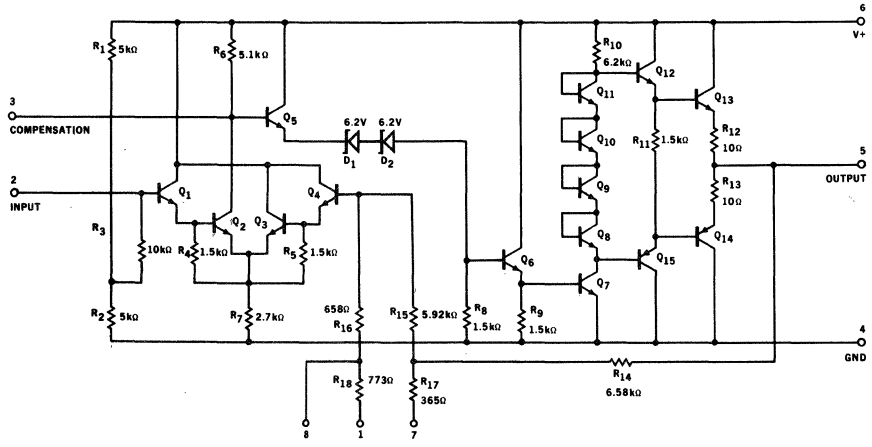
PHYSICAL DIMENSIONS



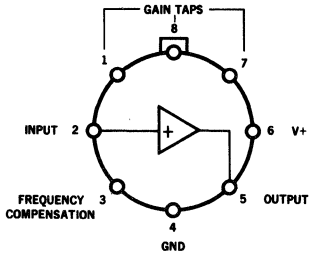
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO.U5B771639X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

NOTE: Lead No. 4 internally connected to case

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

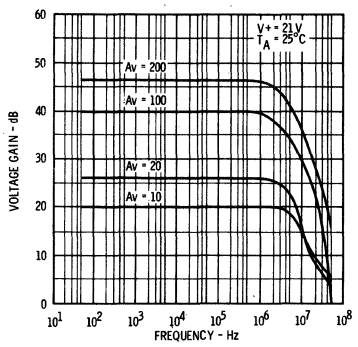
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V^+ = 21V$ unless otherwise specified)

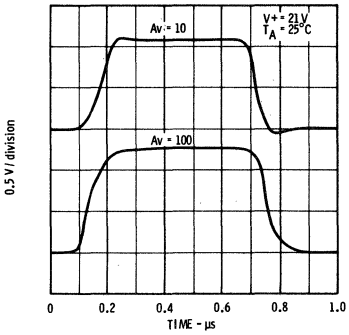
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Quiescent Power Consumption	$T_A = 25°C$		280	350	mW
Total Harmonic Distortion	$A_V = 10$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\ \Omega$		0.01	0.05	%
	$A_V = 100$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\ \Omega$		0.10	0.50	%
Input Noise Voltage	$R_S = 600\ \Omega$, $T_A = 25°C$, $B_n = 16$ Hz to 150 kHz		8.0		μV_{rms}
Output Voltage Swing	$R_L = 150\ \Omega$	10	14		V_{p-p}
	$R_L \geq 5k\ \Omega$	15	17		V_{p-p}
Input Resistance		9.0	11		kΩ
Output Resistance			1.0		Ω
Voltage Gain	See Table I				
10x		9.0	10	11	
20x		18	20	22	
100x		95	105	115	
200x		185	205	225	
Bandwidth	$T_A = 25°C$		2.0		MHz
Temperature Stability of Voltage Gain	$T_{ref} = 25°C$				
10x			±0.02	±0.25	dB
20x			±0.02	±0.25	dB
100x			±0.02	±0.25	dB
200x			±0.05	±0.50	dB

TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

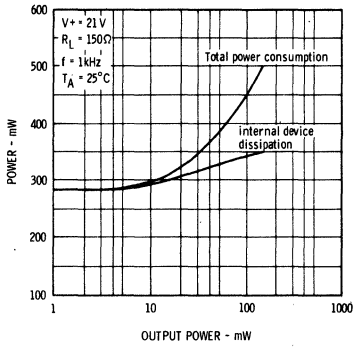


TRANSIENT RESPONSE

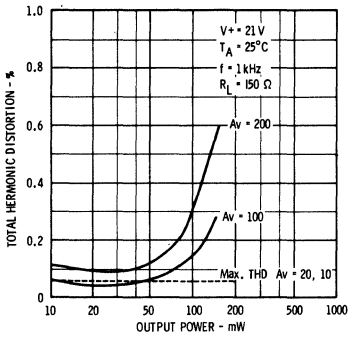


TYPICAL PERFORMANCE CURVES

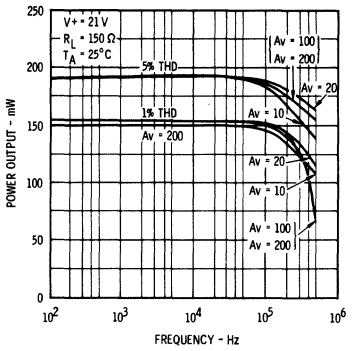
TOTAL POWER CONSUMPTION AND INTERNAL DEVICE DISSIPATION AS A FUNCTION OF OUTPUT POWER



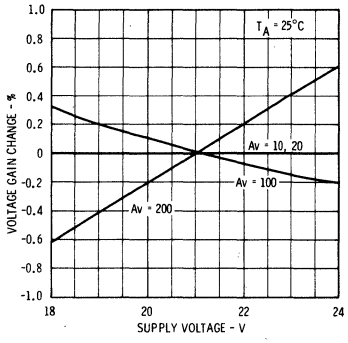
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER



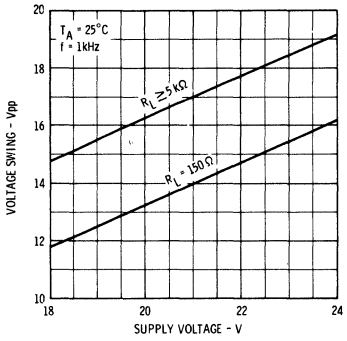
POWER OUTPUT AS A FUNCTION OF FREQUENCY 5% AND 1% THD



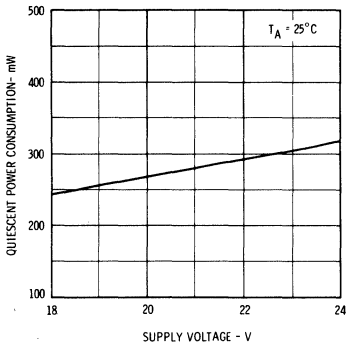
RELATIVE VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



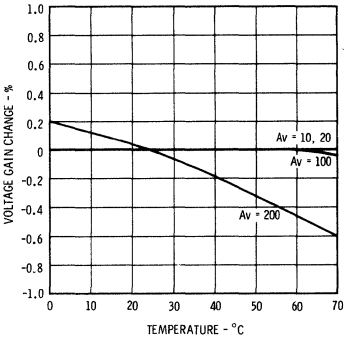
VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



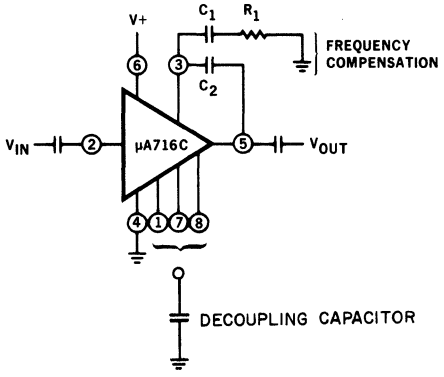
QUIESCENT POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



RELATIVE VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



CONNECTION DIAGRAM AND COMPONENT TABLE FOR AVAILABLE GAIN OPTIONS



Voltage Gain	C_1	C_2	R_1	Decouple Pins:
10	68 pF	39 pF	75 Ω	1
20	50 pF	27 pF	75 Ω	8
100	None	3 pF	None	1, 7
200	None	3 pF	None	7, 8

TABLE I

DEFINITION OF TERMS

Quiescent Power Consumption — The DC power required to operate the amplifier with no signal applied at the input and the load current equal to zero.

Total Harmonic Distortion — The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

Input Noise Voltage — The noise voltage at the output of the amplifier, divided by the amplifier voltage gain.

Output Voltage Swing — The maximum output voltage that may be obtained at the output of the amplifier before saturation occurs.

Input Resistance — The small-signal resistance seen looking into the input terminal of the amplifier.

Voltage Gain — The ratio of the small-signal output voltage to the input voltage of the amplifier.

Temperature Stability of Voltage Gain — The maximum variation of the voltage gain over the specified temperature range.

μA717E

MULTI-PURPOSE AMPLIFIER

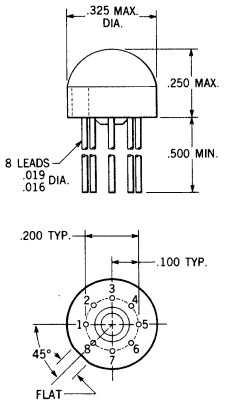
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA717E is a multi-purpose circuit designed primarily for TV sound systems and general FM-audio applications. In TV sound systems it functions as a 4.5 MHz amplifier, limiter and FM detector (simple quadrature type), audio preamplifier and driver. Special features of the μA717E include (a) operation at supply voltages from 6 to 15 volts with simple rebiasing by the use of an external resistor, and (b) the option of using the microcircuit without the quadrature detector as a high gain amplifier from 100 kHz to 50 MHz.

ABSOLUTE MAXIMUM RATINGS:

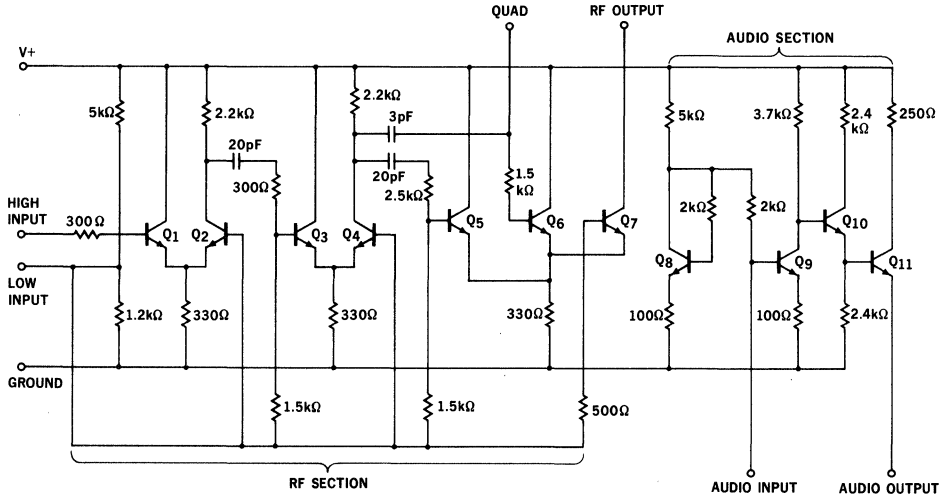
Supply Voltage	15 V
Output Collector Voltage (RF Section)	20 V
Voltage Between "High Input" and "Low Input" Terminals	±5 V
Power Dissipation (Note 1)	350 mW
Maximum Internal Temperature (Note 2)	125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 second time limit)	260°C

PHYSICAL DIMENSIONS

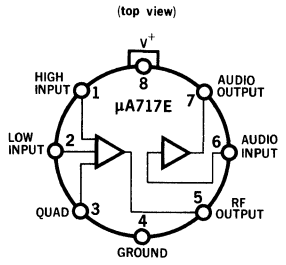


ORDER PART NO.
U8A771739X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTES:
(1) Rating applies for ambient temperatures from 0°C to +70°C.
(2) Derate maximum dissipation by 6.4 mW/°C above 70°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

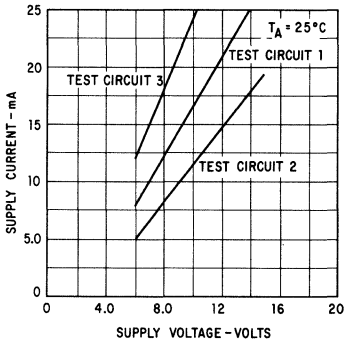
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12V$, Test Circuit 4 unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Total Supply Current			21		mA
Power Consumption	$e_{IN} = 0$		250	350	mW
Audio Output D-C Bias Voltage		2.0	2.6	3.2	V
Voltage Gain of Audio Section			35		
Audio Output Drive Current (clipping)	Audio output load 250Ω applied between pin 7 and ground		20		mA peak
Input Voltage for −3 dB Limiting	f = 4.5 MHz Test Circuit 9		1.5	5.0	mV rms
Noise Figure	$R_S = 1k\Omega$, f = 4.5 MHz Test Circuit 10		7.0		dB
Noise Figure	$R_S = 1k\Omega$, f = 10.7 MHz Test Circuit 10		7.0		dB

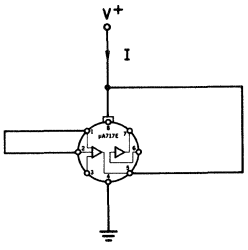
PARAMETER	TEST CONDITION		@ f = 4.5 MHz MIN.	TYP.	MAX.	@ f = 10.7 MHz MIN.	TYP.	MAX.	UNITS
Input Conductance	$e_{in} \leq 20$ mV rms	Test Circuit 5		0.21			0.35		mmho
Input Capacitance	$e_{in} \leq 20$ mV rms	Test Circuit 5		12			10		pF
Output Conductance		Test Circuit 6		0.05			0.1		mmho
Output Capacitance		Test Circuit 6		6.0			5.0		pF
Forward Transadmittance		Test Circuit 8		2200			1200		mmho
Gain Maximum Stable (GMS)		Test Circuit 10		80			80		dB
Gain Maximum Available (GMA)		Test Circuit 10		81			71		dB
Quadrature Conductance	$e_{in} \leq 20$ mV rms	Test Circuit 7		0.22			0.35		mmho
Quadrature Capacitance	$e_{in} \leq 20$ mV rms	Test Circuit 7		9.5			8.0		pF

TYPICAL PERFORMANCE CURVES

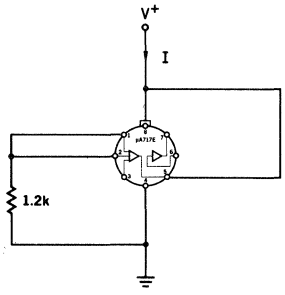
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



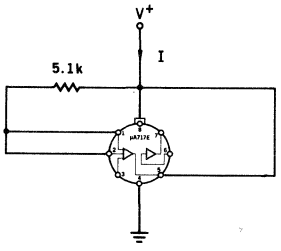
TEST CIRCUIT 1



TEST CIRCUIT 2



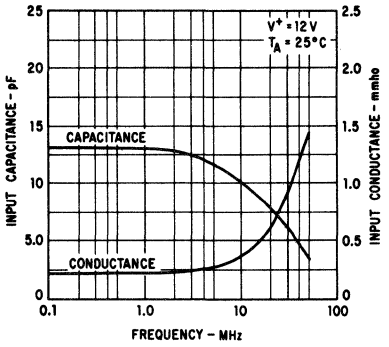
TEST CIRCUIT 3



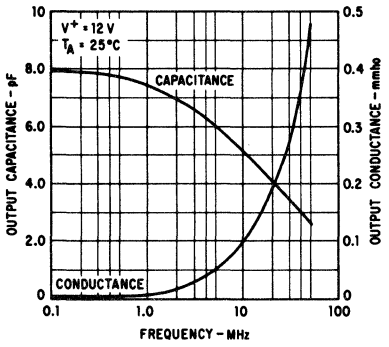
TOTAL SUPPLY CURRENT

TYPICAL PERFORMANCE CURVES

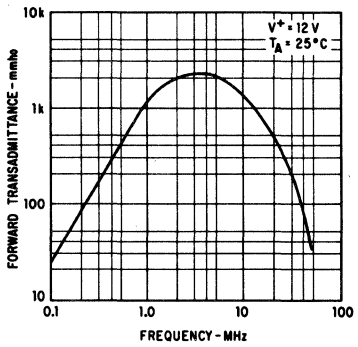
INPUT CONDUCTANCE AND CAPACITANCE AS A FUNCTION OF FREQUENCY



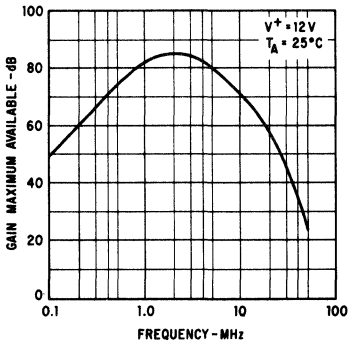
OUTPUT CONDUCTANCE AND CAPACITANCE AS A FUNCTION OF FREQUENCY



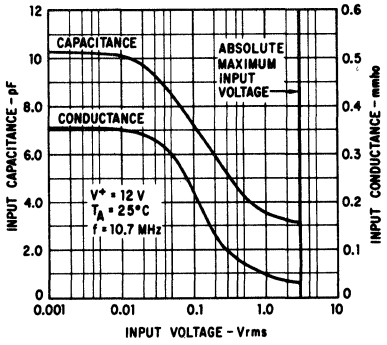
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



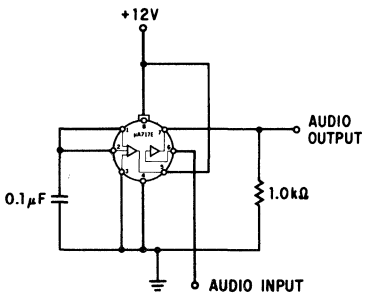
GAIN MAXIMUM AVAILABLE (GMA) AS A FUNCTION OF FREQUENCY



INPUT CONDUCTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE

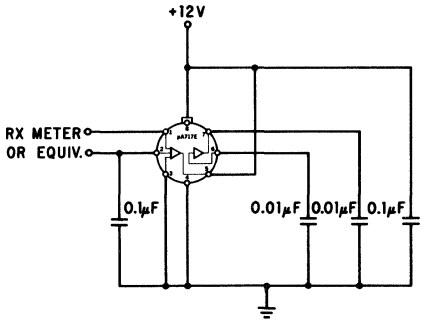


TEST CIRCUIT 4



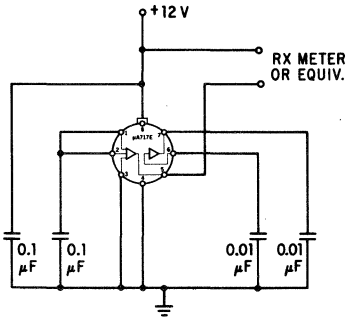
DC AND AUDIO GAIN TEST CIRCUIT

TEST CIRCUIT 5



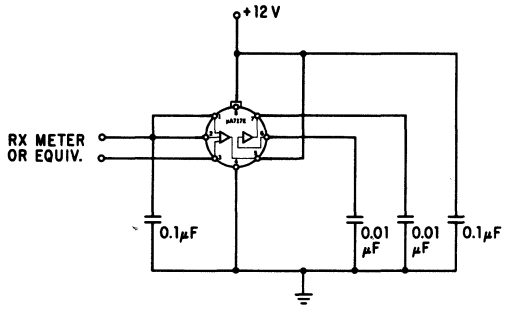
INPUT CONDUCTANCE AND CAPACITANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 6



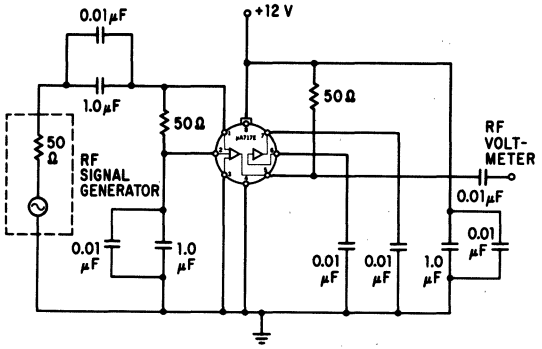
OUTPUT CONDUCTANCE AND CAPACITANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 7



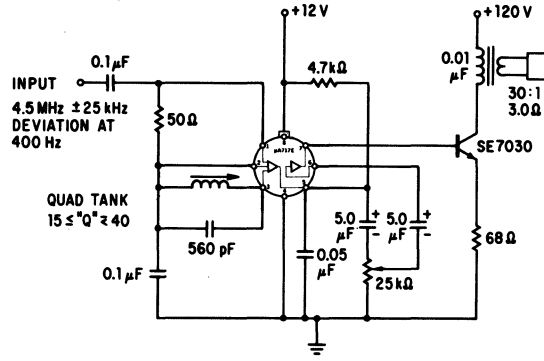
QUADRATURE CONDUCTANCE AND CAPACITANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 8



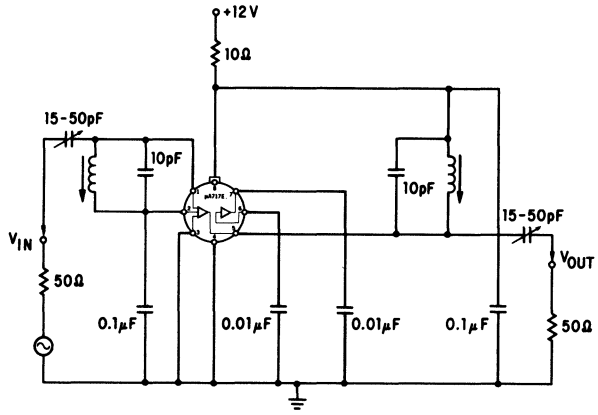
FORWARD TRANSADMITTANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 9



TV SOUND SYSTEM

TEST CIRCUIT 10



MEASUREMENT CIRCUIT

NOISE FIGURE
GAIN MAXIMUM STABLE
GAIN MAXIMUM AVAILABLE

DEFINITION OF TERMS

POWER CONSUMPTION — The total power consumption of Test Circuit 1.

GAIN MAXIMUM STABLE (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum practical power gain realizable based on normal circuit tolerances is either (GMS − 6 dB) or GMA, whichever is smaller.

GAIN MAXIMUM AVAILABLE (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

INPUT LIMITING VOLTAGE — Referring to Test Circuit 9; set 25 kilohm potentiometer to give 1 watt audio output power into speaker with an input signal of 50 mV rms. The −3 dB input limiting voltage is defined as the value of the input voltage when the audio output power has fallen to 0.5 watt. For further information on the μA717E refer to Fairchild Application Bulletin No. 158, — "Two High Performance Monolithic Microcircuits For FM Sound Systems." by David Bingham.

μA719

HIGH GAIN RF AMPLIFIER/FM DETECTOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

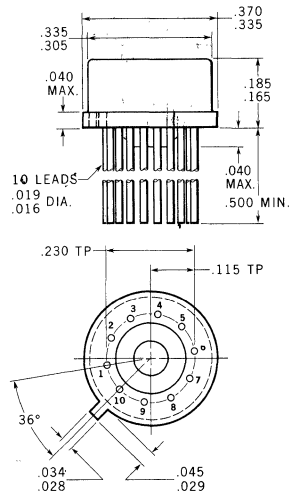
- **HIGH GAIN AT 10.7 MHz**
- **AGC RANGE > 30 dB**
- **TWO SEPARATE AMPLIFIERS**
- **SUPPLY VOLTAGE 5 TO 15 VOLTS**
- **OPTIONAL FM QUADRATURE DETECTOR**

GENERAL DESCRIPTION — The μA719 is a high gain RF amplifier/FM detector which contains two independent amplifier sections designed for IF systems to 50 MHz. Section 1 utilizes three cascaded emitter coupled amplifiers having high gain and a reverse AGC capability. In addition, Section 1 may be used as an amplifier limiter and quadrature detector for FM systems. Section 2 is a single stage amplifier useful from DC to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Output Collector Voltage (Section 1)	20 V
Voltage between "High Input 1" and "Low Input 1" Terminals	±5.0 V
Voltage between "Quad" and "Ground" Terminals	0 to +4.0 V
Voltage between "Input 2" and "Ground" Terminals	±2.0 V
Power Dissipation (Note 1)	350 mW
Maximum Chip Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

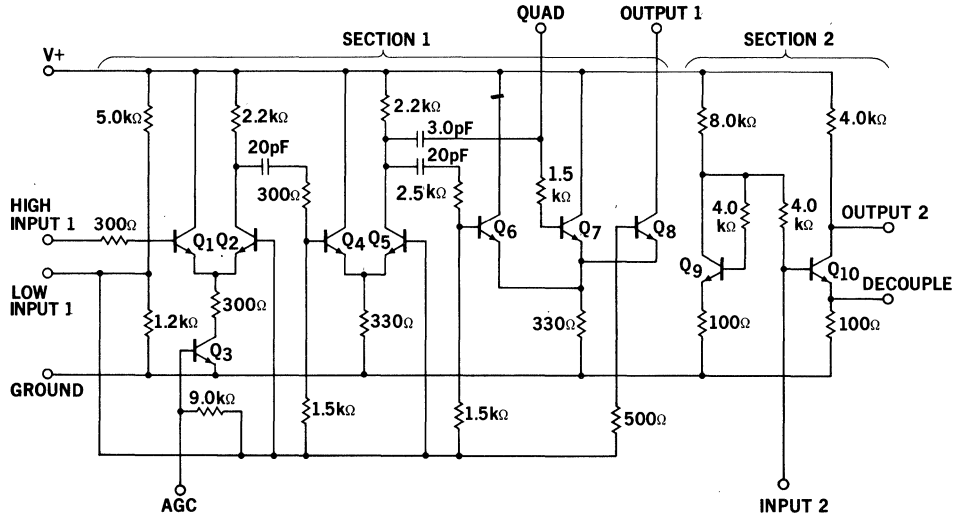
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO–100)



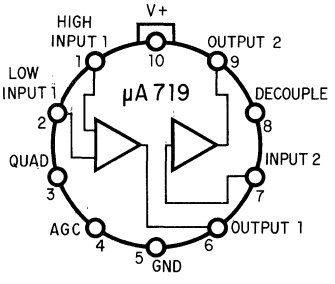
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F7719312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



NOTE:

(1) Rating applies for ambient temperatures to +125°C if the package case to ambient thermal resistance is lowered to 40°C/Watt by the addition of a heat dissipator. Derate linearly 5.6 mW/°C for ambient temperatures above 87°C.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

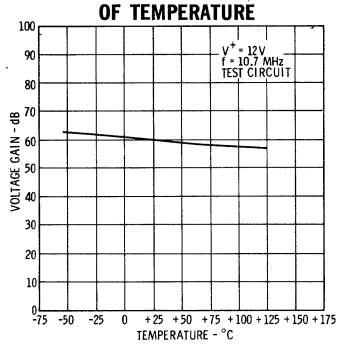
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V, Test Circuit 1 unless otherwise specified)

PARAMETER (See Definitions)	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$T_A = +25°C$	12	18	25	mA
	$T_C = -55°C$		17.5		mA
	$T_C = +125°C$		17		mA
Supply Current	$V^+ = 9.0$ V,	6.0	12.5	18.5	mA
Power Dissipation	$T_A = +25°C$	144	216	300	mW
	$T_C = -55°C$		210		mW
	$T_C = +125°C$		204		mW
Power Dissipation	$V^+ = 9.0$ V,	54	113	167	mW
Section 1 Quiescent Output Current		1.0	2.5	4.0	mA
Section 1 DC Voltage at AGC Terminal		0.55	0.73	1.25	V
Section 1 AGC Current For 30 dB AGC	f = 10.7 MHz, Test Circuit 3		170	250	μA
Section 1 Output Current	f = 1.0 MHz, Test Circuit 8		4.4		mA_{p-p}
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3				
	$T_A = +25°C$	53	60		dB
	$T_C = -55°C$		63		dB
	$T_C = +125°C$		58		dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 9.0$ V		53		dB
Section 1 Input Voltage For −3.0 dB Limiting	f = 4.5 MHz, Test Circuit 4		1.5	4.0	mV
Section 1 Noise Figure	$R_S = 1.0$ kΩ, Test Circuit 5				
	f = 4.5 MHz		7.0		dB
	f = 10.7 MHz		7.0		dB
Section 2 DC Voltage at Output 2		5.2	6.3	7.4	V
Section 2 Voltage Gain	f = 1.0 kHz, Test Circuit 2	22	31		dB
Section 2 Voltage at Output 2 Without Clipping	f = 1.0 kHz, Test Circuit 2		10		V_{p-p}

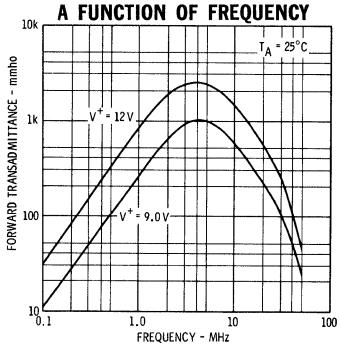
PARAMETERS (See Definitions)	TEST CONDITIONS	f = 4.5 MHz TYP.	f = 10.7 MHz TYP.	UNITS
SECTION 1				
Input Conductance	$e_{IN} \leq 20$ mV Test Circuit 6	170	300	μmho
Input Capacitance	$e_{IN} \leq 20$ mV Test Circuit 6	7.5	6.3	pF
Output Conductance	Test Circuit 7	50	130	μmho
Output Capacitance	Test Circuit 7	6.7	5.4	pF
Forward Transadmittance	Test Circuit 8	2200	1400	mmho
Forward Transadmittance	Test Circuit 8 $V^+ = 9.0$ V	1000	600	mmho
Quad Conductance	Test Circuit 9	200	330	μmho
Quad Capacitance	Test Circuit 9	8.0	7.0	pF
Gain Maximum Available (GMA)	Test Circuit 5	83	71	dB
Gain Maximum Stable (GMS)	Test Circuit 5	85	78	dB
SECTION 2				
Input Conductance	Test Circuit 10			
	Pin #8 Unbypassed	300	300	μmho
	Pin #8 Bypassed	360	460	μmho
Input Capacitance	Test Circuit 10			
	Pin #8 Unbypassed	3.3	3.3	pF
	Pin #8 Bypassed	10.4	8.7	pF
Output Conductance	Test Circuit 11			
	Pin #8 Unbypassed	250	260	μmho
	Pin #8 Bypassed	270	340	μmho
Output Capacitance	Test Circuit 11			
	Pin #8 Unbypassed	5.2	5.2	pF
	Pin #8 Bypassed	8.9	8.0	pF
Forward Transadmittance	Test Circuit 12			
	Pin #8 Unbypassed	8.0	8.0	mmho
	Pin #8 Bypassed	34	34	mmho
Gain Maximum Available (GMA)	Pin #8 Unbypassed	24	24	dB
	Pin #8 Bypassed	35	32	dB

TYPICAL PERFORMANCE CURVES

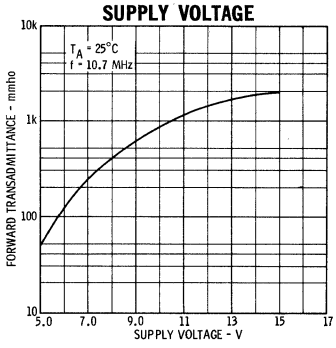
SECTION 1
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



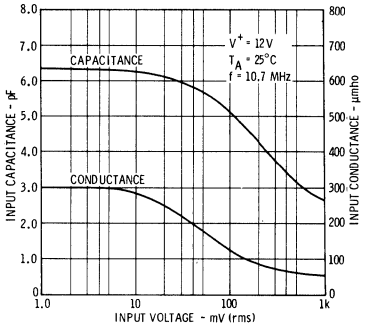
SECTION 1
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



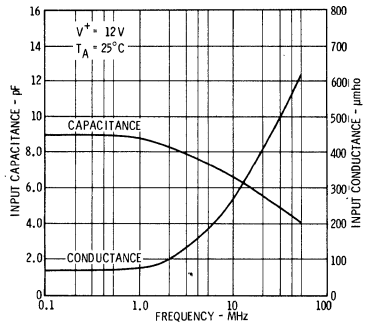
SECTION 1
FORWARD TRANSADMITTANCE AS A FUNCTION OF SUPPLY VOLTAGE



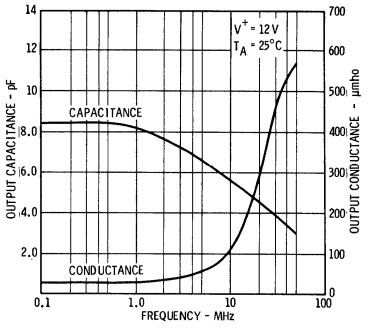
SECTION 1
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE



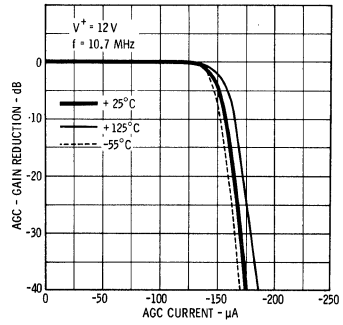
SECTION 1
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



SECTION 1
OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



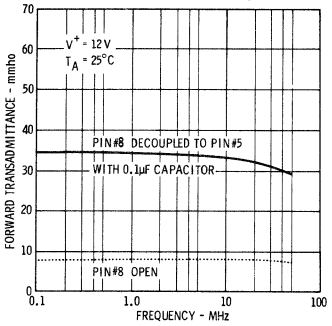
SECTION 1
AGC AS A FUNCTION OF AGC CURRENT



TYPICAL PERFORMANCE CURVES

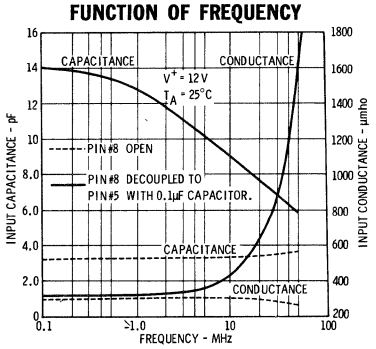
SECTION 2

FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



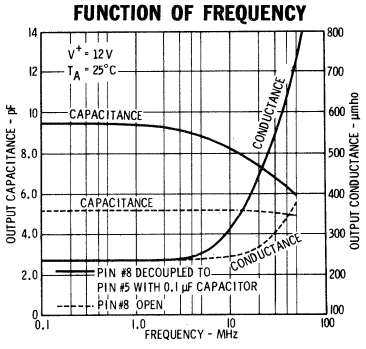
SECTION 2

INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY

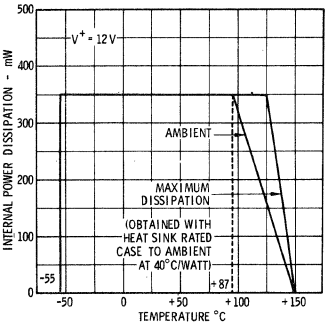


SECTION 2

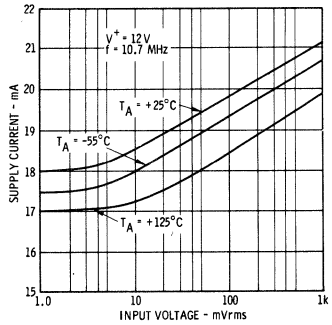
OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



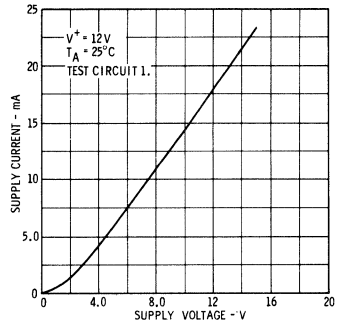
MAXIMUM INTERNAL DISSIPATION AS A FUNCTION OF EITHER AMBIENT OR CASE TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF INPUT 1 SIGNAL VOLTAGE



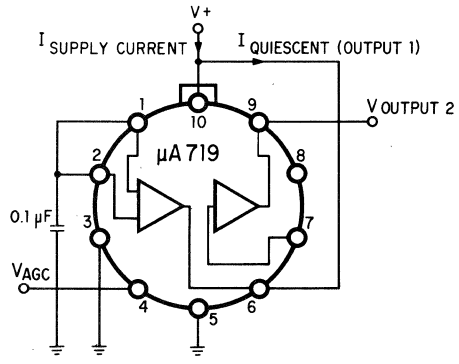
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TEST CIRCUITS

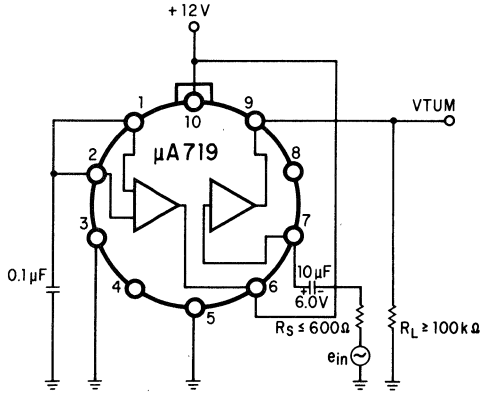
TEST CIRCUIT 1

DC MEASUREMENTS



TEST CIRCUIT 2

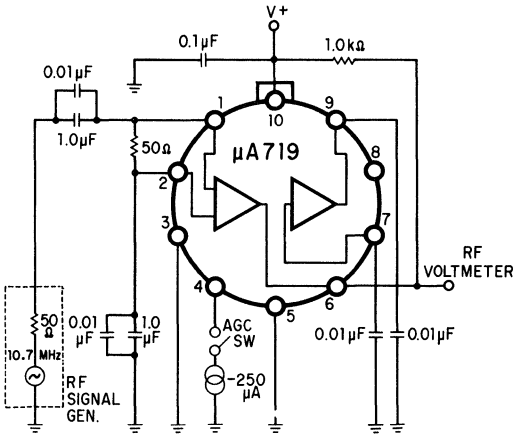
SECTION 2 GAIN AND OUTPUT VOLTAGE SWING



TEST CIRCUITS

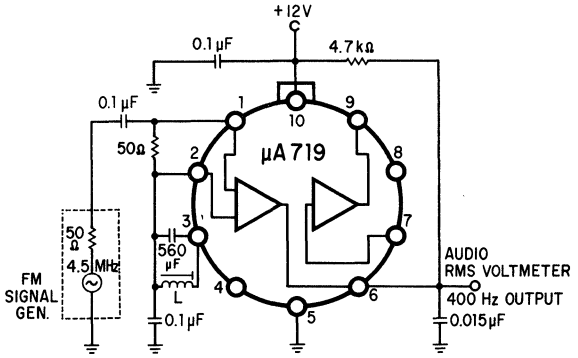
TEST CIRCUIT 3

10.7 MHz VOLTAGE GAIN AND AGC



TEST CIRCUIT 4

-3.0 dB LIMITING AT 4.5 MHz USING A QUADRATURE DETECTOR*

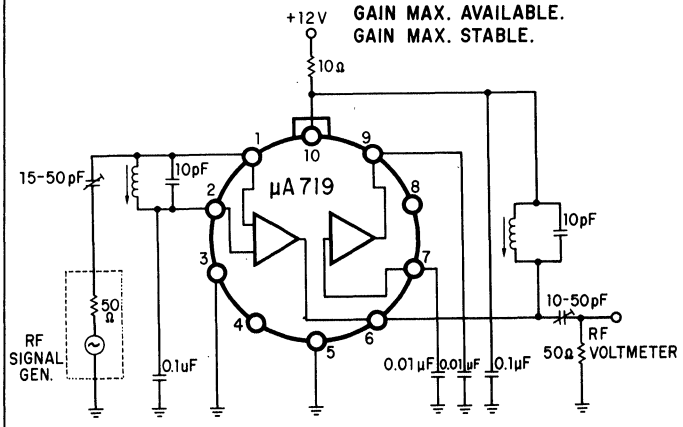


INPUT SIGNAL 4.5 MHz 25kHz DEVIATION AT 400 Hz. UNLOADED QUALITY FACTOR OF QUADRATURE TANK INDUCTOR IS 65.

*SEE DEFINITIONS

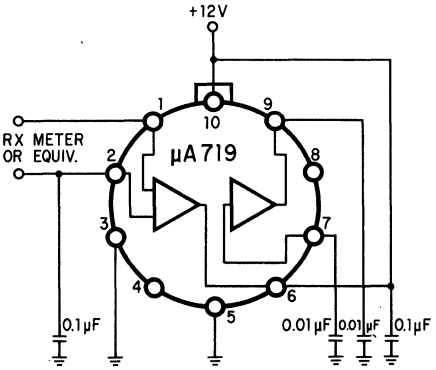
TEST CIRCUIT 5

SECTION 1: NOISE FIGURE.
GAIN MAX. AVAILABLE.
GAIN MAX. STABLE.



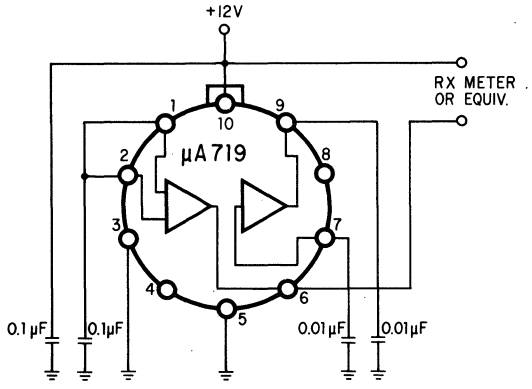
TEST CIRCUIT 6

SECTION 1 INPUT PARAMETERS



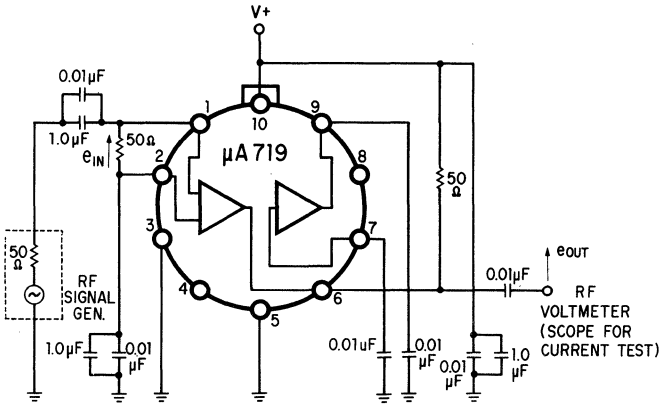
TEST CIRCUIT 7

SECTION 1 OUTPUT PARAMETERS



TEST CIRCUIT 8

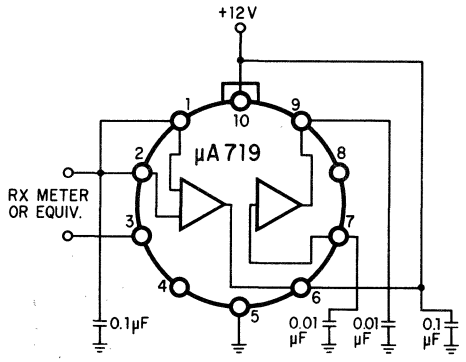
SECTION 1 FORWARD TRANSADMITTANCE OUTPUT CURRENT



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

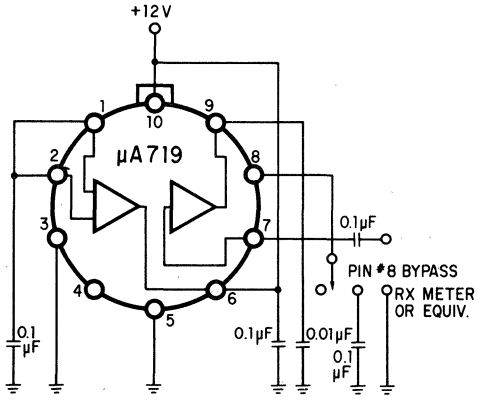
TEST CIRCUIT 9

SECTION 1 QUAD PARAMETERS



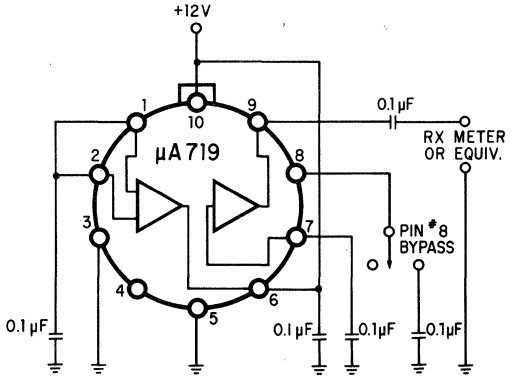
TEST CIRCUIT 10

SECTION 2 INPUT PARAMETERS



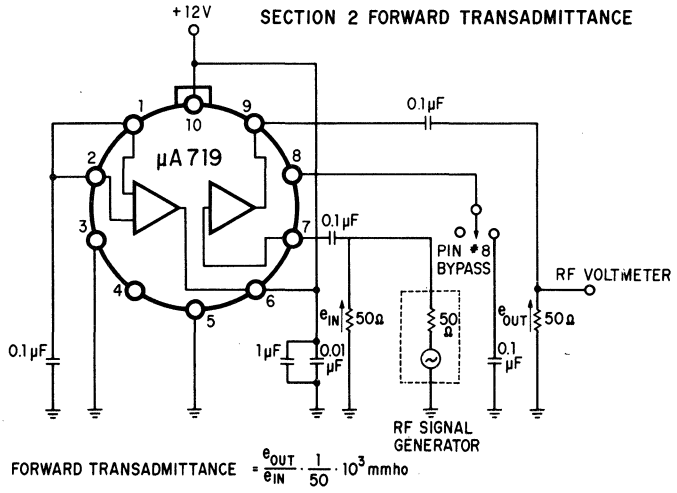
TEST CIRCUIT 11

SECTION 2 OUTPUT PARAMETERS



TEST CIRCUIT 12

SECTION 2 FORWARD TRANSADMITTANCE



FORWARD TRANSADMITTANCE $= \frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

DEFINITION OF TERMS

Gain Maximum Available (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

$$GMA = \frac{|\text{forward transadmittance}|^2}{4 \times \text{input conductance} \times \text{output conductance}}$$

Gain Maximum Stable (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerances is either (GMS - 6.0 dB) or GMA, whichever is smaller.

$$GMS = \frac{|\text{forward transadmittance}|}{|\text{reverse transadmittance}|}$$

Input Voltage For —3.0 dB Limiting — Refer to Test Circuit 4 which shows the μA719 being used as an amplifier, limiter, and FM detector (simple quadrature type with the LC tank circuit connected between pins No. 3 and No. 2). An input FM signal (carrier frequency 4.5 MHz, ±25 kHz deviation at 400 Hz) of 50 mV rms is applied to the μA719 and the value of the recovered audio output signal (400 Hz) at pin No. 6 is noted. The —3.0 dB input limiting voltage is defined as the value of the input voltage to produce an output voltage 3dB below the output level obtained with 50 mV rms of input signal.

μA719C

HIGH GAIN RF AMPLIFIER/FM DETECTOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

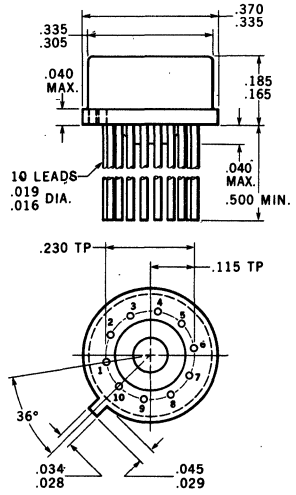
- **HIGH GAIN AT 10.7 MHz**
- **AGC RANGE > 30 dB**
- **TWO SEPARATE AMPLIFIERS**
- **SUPPLY VOLTAGE 5 TO 15 VOLTS**
- **OPTIONAL FM QUADRATURE DETECTOR**

GENERAL DESCRIPTION — The μA719C is a high gain RF amplifier/FM detector which contains two independent amplifier sections designed for IF systems to 50 MHz. Section 1 utilizes three cascaded emitter coupled amplifiers having high gain and a reverse AGC capability. In addition, Section 1 may be used as an amplifier limiter and quadrature detector for FM systems. Section 2 is a single stage amplifier useful from DC to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Output Collector Voltage (Section 1)	20 V
Voltage between "High Input 1" and "Low Input 1" Terminals	±5.0 V
Voltage between "Quad" and "Ground" Terminals	0 to +4.0 V
Voltage between "Input 2" and "Ground" Terminals	±2.0 V
Power Dissipation	350 mW
Maximum Chip Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 second time limit)	300°C

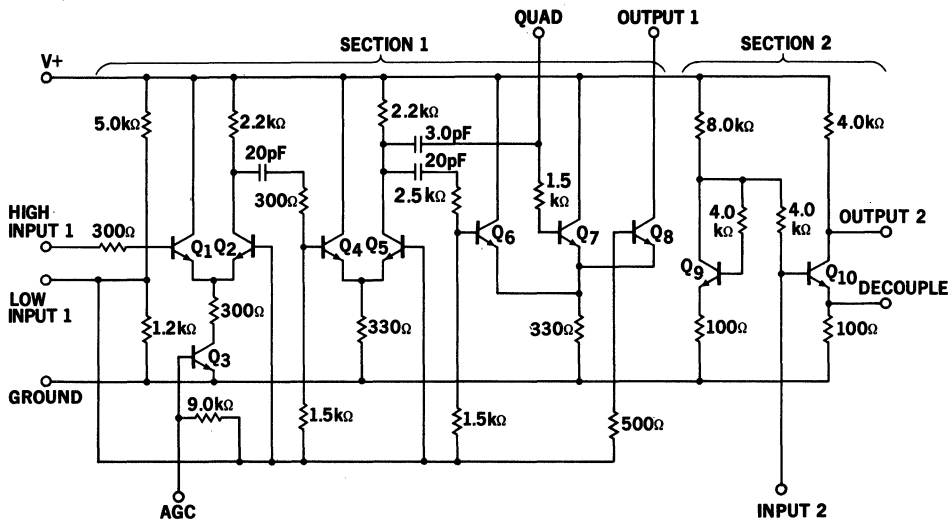
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO–100)



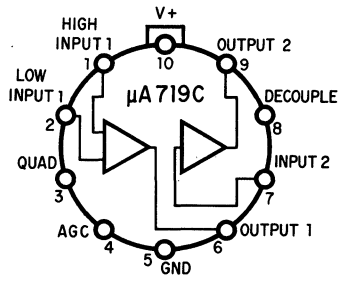
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F7719393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

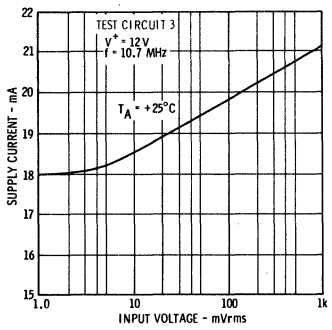
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V, Test Circuit 1 unless otherwise specified)

PARAMETER (See Definitions)	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$T_A = +25°C$	12	18	25	mA
	$T_A = 0°C$	10	17.5	27	mA
	$T_A = +70°C$	10	17	25	mA
Supply Current	$V^+ = 9.0$ V	6.0	12.5	18.5	mA
Supply Current	$V^+ = 6.0$ V, $70°C \leq T_A \leq 0°C$	3.0	6.0	10	mA
Power Dissipation	$T_A = +25°C$	144	216	300	mW
	$T_A = 0°C$	120	210	324	mW
	$T_A = +70°C$	120	204	300	mW
Power Dissipation	$V^+ = 9.0$ V	54	113	167	mW
Power Dissipation	$V^+ = 6.0$ V, $70°C \leq T_A \leq 0°C$	18	36	60	mW
Section 1 Quiescent Output Current		1.0	2.5	4.0	mA
Section 1 DC Voltage at AGC Terminal		0.55	0.73	1.25	V
Section 1 AGC Current For 30 dB AGC	f = 10.7 MHz, Test Circuit 3		170	250	μA
Section 1 Output Current	f = 1.0 MHz, Test Circuit 8		4.4		mA_{p-p}
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3				
	$T_A = +25°C$	50	60	70	dB
	$T_A = 0°C$	50	61	70	dB
	$T_A = +70°C$	48	59	70	dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 9.0$ V		53		dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 6.0$ V		38		dB
Section 1 Input Voltage For −3.0 dB Limiting	f = 4.5 MHz, Test Circuit 4		1.5	6.5	mV
Section 1 Noise Figure	$R_S = 1.0$ kΩ, Test Circuit 5				
	f = 4.5 MHz		7.0		dB
	f = 10.7 MHz		7.0		dB
Sections 1 and 2 Cascaded Voltage Gain	f = 10.7 MHz, Test Circuit 13				
	$V^+ = 6.0$ V, R = 3.0 kΩ				
	Pin #8 Unbypassed		51		dB
	Pin #8 Bypassed		56		dB
Section 2 DC Voltage at Output 2		5.2	6.3	7.4	V
Section 2 Voltage Gain	f = 1.0 kHz, Test Circuit 2	22	31	40	dB
Section 2 Voltage at Output 2 Without Clipping	f = 1.0 kHz, Test Circuit 2	7.0	10	11.5	V_{p-p}

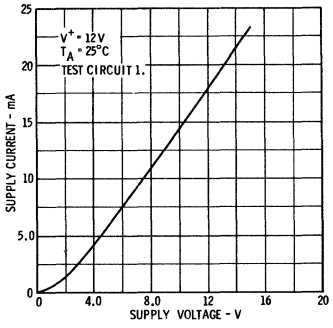
PARAMETERS (See Definitions)	TEST CONDITIONS	f = 4.5 MHz TYP.	f = 10.7 MHz TYP.	UNITS
SECTION 1				
Input Conductance	Test Circuit 6, $e_{IN} \leq 20$ mV	170	300	μmho
Input Capacitance	Test Circuit 6, $e_{IN} \leq 20$ mV	7.5	6.3	pF
Output Conductance	Test Circuit 7	50	130	μmho
Output Capacitance	Test Circuit 7	6.7	5.4	pF
Forward Transadmittance	Test Circuit 8	2200	1400	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 9.0$ V	1000	600	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 6.0$ V	180	100	mmho
Quad Conductance	Test Circuit 9	200	330	μmho
Quad Capacitance	Test Circuit 9	8.0	7.0	pF
Gain Maximum Available (GMA)	Test Circuit 5	83	71	dB
Gain Maximum Stable (GMS)	Test Circuit 5	85	78	dB
SECTION 2	Test Circuit 10			
Input Conductance	Pin #8 Unbypassed	300	300	μmho
	Pin #8 Bypassed	360	460	μmho
Input Capacitance	Test Circuit 10			
	Pin #8 Unbypassed	3.3	3.3	pF
	Pin #8 Bypassed	10.4	8.7	pF
Output Conductance	Test Circuit 11			
	Pin #8 Unbypassed	250	260	μmho
	Pin #8 Bypassed	270	340	μmho
Output Capacitance	Test Circuit 11			
	Pin #8 Unbypassed	5.2	5.2	pF
	Pin #8 Bypassed	8.9	8.0	pF
Forward Transadmittance	Test Circuit 12			
	Pin #8 Unbypassed	8.0	8.0	mmho
	Pin #8 Bypassed	34	34	mmho
Gain Maximum Available (GMA)	Pin #8 Unbypassed	24	24	dB
	Pin #8 Bypassed	35	32	dB

TYPICAL PERFORMANCE CURVES

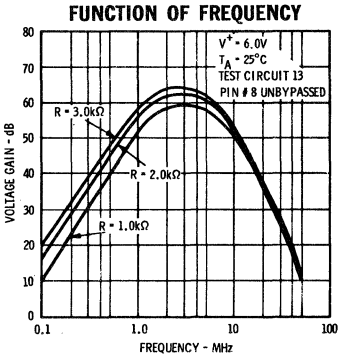
SECTIONS 1 AND 2 SUPPLY CURRENT AS A FUNCTION OF INPUT 1 SIGNAL VOLTAGE



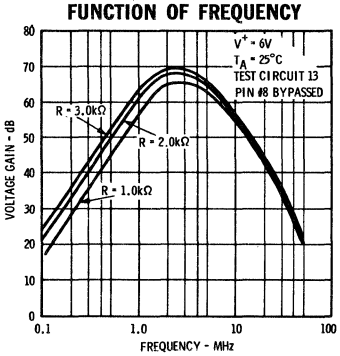
SECTIONS 1 AND 2 SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



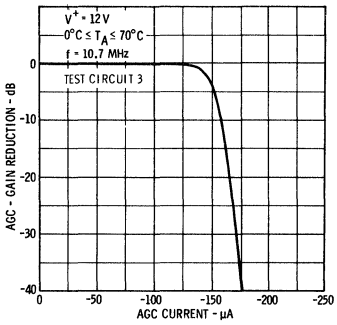
SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



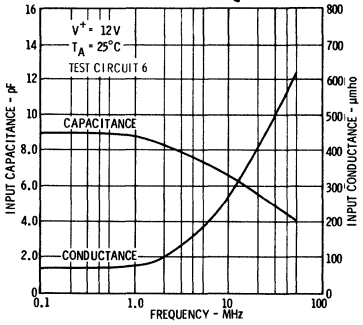
SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



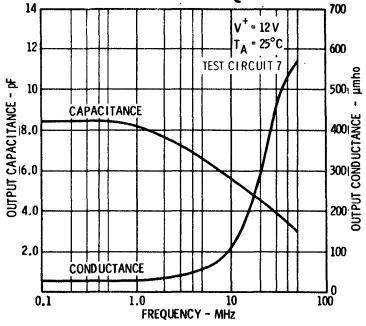
SECTION 1 AGC AS A FUNCTION OF AGC CURRENT



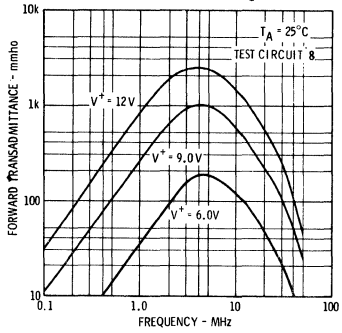
SECTION 1 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



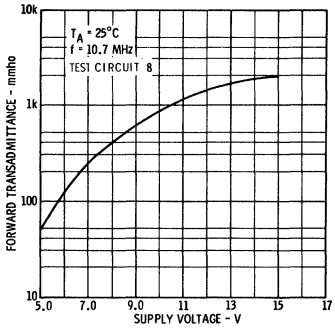
SECTION 1 OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



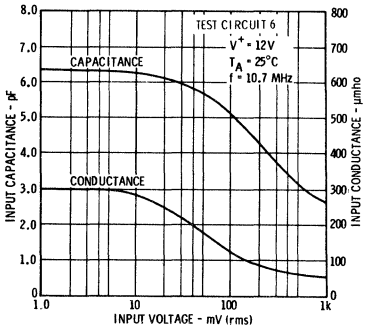
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



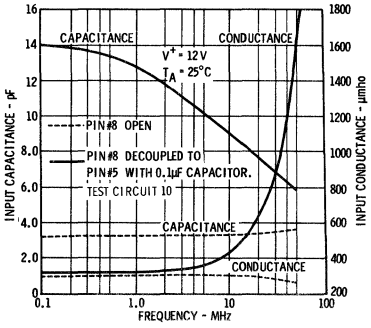
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF SUPPLY VOLTAGE



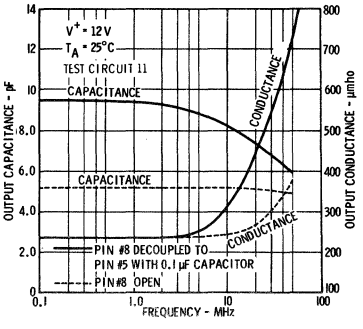
SECTION 1 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE



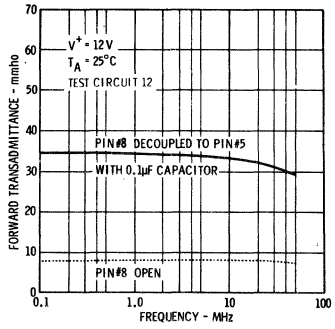
SECTION 2 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



SECTION 2 OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



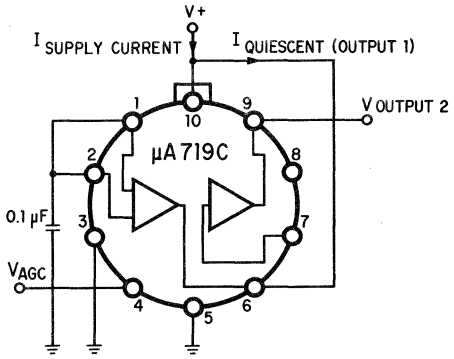
SECTION 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



TEST CIRCUITS

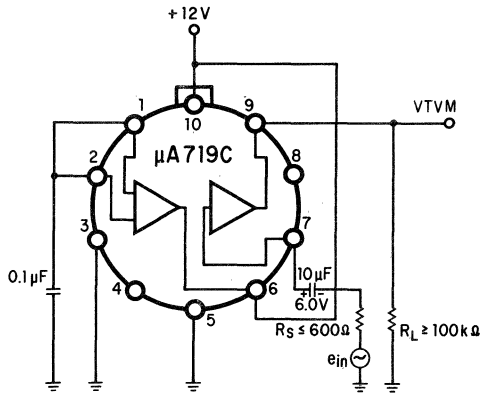
TEST CIRCUIT 1

DC MEASUREMENTS



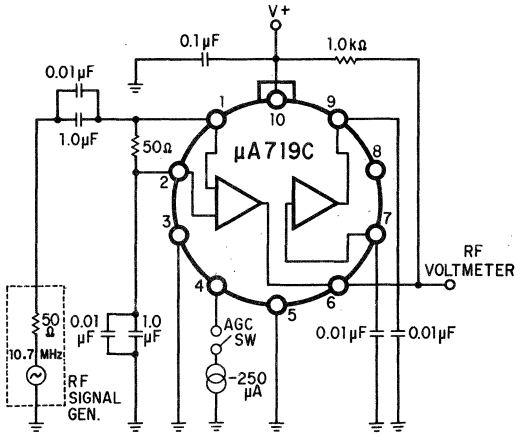
TEST CIRCUIT 2

SECTION 2 GAIN AND OUTPUT VOLTAGE SWING



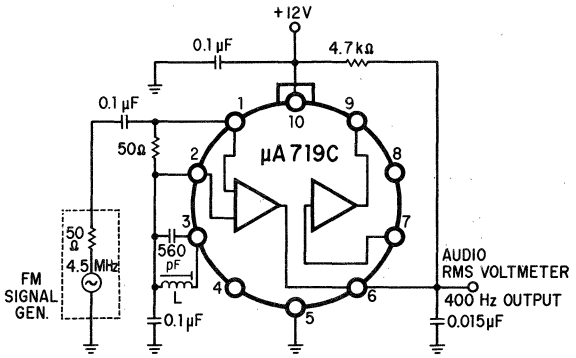
TEST CIRCUIT 3

10.7 MHz VOLTAGE GAIN AND AGC



TEST CIRCUIT 4

-3.0dB LIMITING AT 4.5 MHz USING A QUADRATURE DETECTOR*

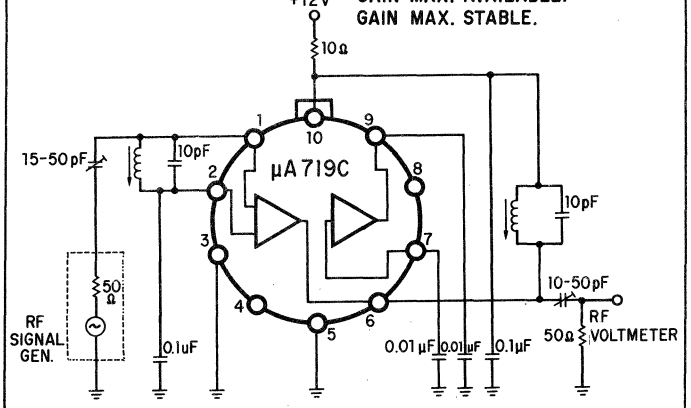


INPUT SIGNAL 4.5 MHz 25kHz DEVIATION AT 400 Hz. UNLOADED QUALITY FACTOR OF QUADRATURE TANK INDUCTOR IS 22.

*SEE DEFINITIONS

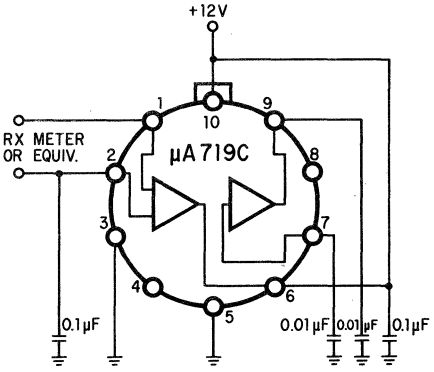
TEST CIRCUIT 5

SECTION 1: NOISE FIGURE.
GAIN MAX. AVAILABLE.
GAIN MAX. STABLE.



TEST CIRCUIT 6

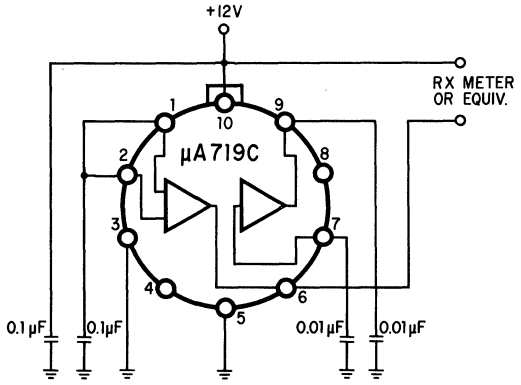
SECTION 1 INPUT PARAMETERS



TEST CIRCUITS

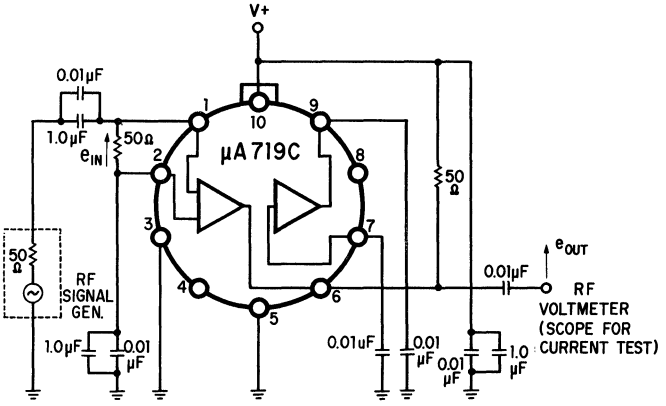
TEST CIRCUIT 7

SECTION 1 OUTPUT PARAMETERS



TEST CIRCUIT 8

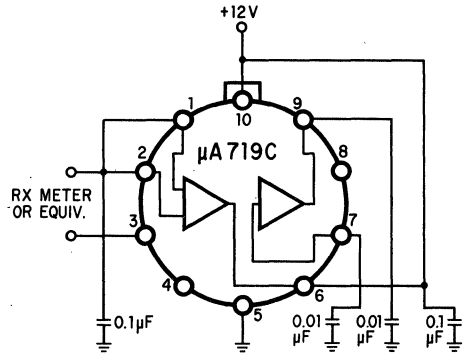
SECTION 1 FORWARD TRANSADMITTANCE OUTPUT CURRENT



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

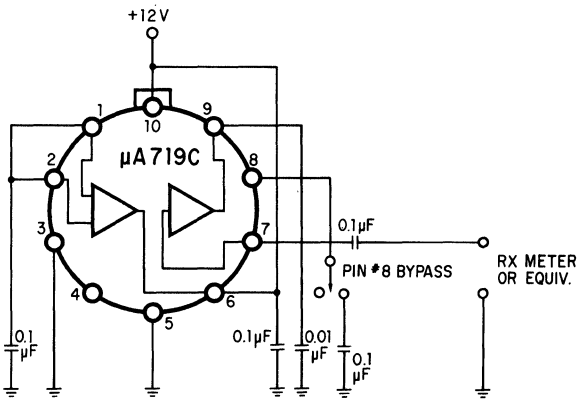
TEST CIRCUIT 9

SECTION 1 QUAD PARAMETERS



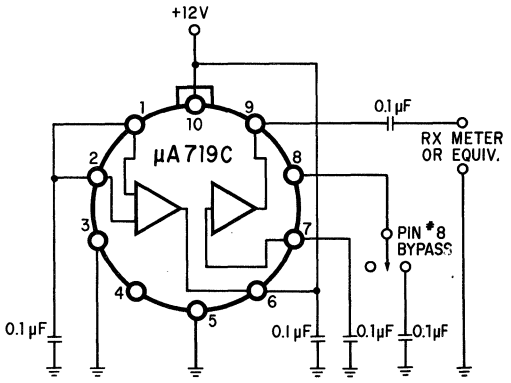
TEST CIRCUIT 10

SECTION 2 INPUT PARAMETERS



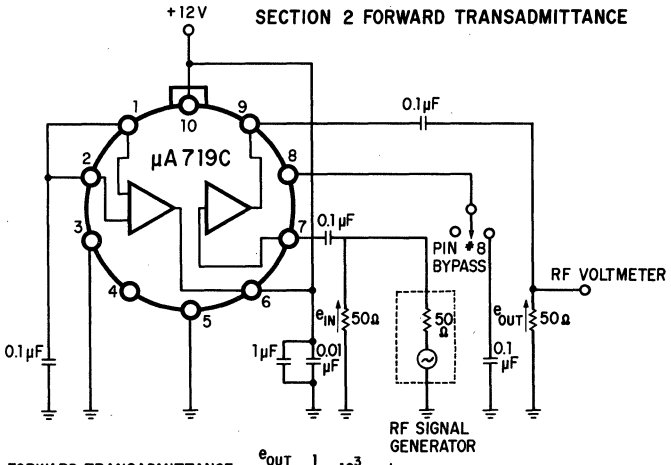
TEST CIRCUIT 11

SECTION 2 OUTPUT PARAMETERS



TEST CIRCUIT 12

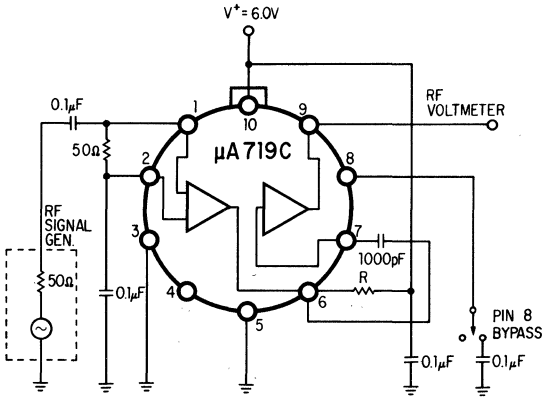
SECTION 2 FORWARD TRANSADMITTANCE



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

TEST CIRCUIT 13

SECTION 1 AND 2 CASCADED VOLTAGE GAIN



DEFINITION OF TERMS

Gain Maximum Available (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

$$GMA = \frac{|\text{forward transadmittance}|^2}{4 \times \text{input conductance} \times \text{output conductance}}$$

Gain Maximum Stable (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerances is either (GMS - 6.0 dB) or GMA, whichever is smaller.

$$GMS = \frac{|\text{forward transadmittance}|}{|\text{reverse transadmittance}|}$$

Input Voltage For —3.0 dB Limiting — Refer to Test Circuit 4 which shows the μA719C being used as an amplifier, limiter, and FM detector (simple quadrature type with the LC tank circuit connected between pins No. 3 and No. 2). An input FM signal (carrier frequency 4.5 MHz, ±25 kHz deviation at 400 Hz) of 50 mV rms is applied to the μA719C and the value of the recovered audio output signal (400 Hz) at pin No. 6 is noted. The —3.0 dB input limiting voltage is defined as the value of the input voltage to produce an output voltage 3dB below the output level obtained with 50 mV rms of input signal.

μA722
10-BIT CURRENT SOURCE
FAIRCHILD LINEAR INTEGRATED CIRCUITS

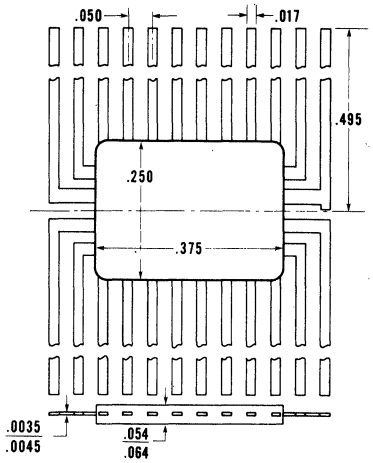
- **8 ± ½ BIT ACCURACY FROM 0°C TO +55°C**
- **7±½ BIT ACCURACY FROM −20°C TO +85°C**
- **600 ns SWITCHING SPEED**
- **INTERNAL PRECISION REFERENCE**
- **CCSL COMPATIBLE**

GENERAL DESCRIPTION — The μA722 is a high-speed, 10-bit precision current source intended for use in current-summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process, and consists of a reference supply, 10 current sources connected to a single output summing line, and associated logic switches. The full-scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μA722 is compatible with the Fairchild families of linear and digital circuits.

ABSOLUTE MAXIMUM RATINGS

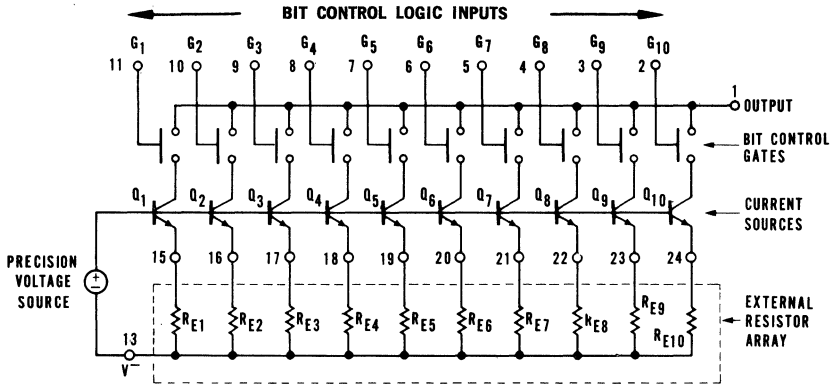
Voltage from V^+ to V^-	−0.5 V to +18 V
Voltage from Output to V^+	−12 V to +6 V
Voltage from Output to V^-	0 V to +12 V
Voltage from Logic Inputs to Output	−9 V to +7 V
Voltage from Logic Inputs to V^+	−18 V to 0 V
Voltage from Logic Inputs to V^-	0 V to +12 V
Internal Power Dissipation (Note 1)	450 mW
Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

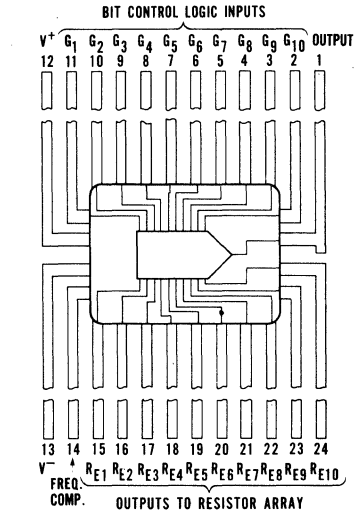


ORDER PART NO. U3M7722333

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 13 INTERNALLY CONNECTED TO CASE.

Notes on Page 2

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS

PARAMETER (See Definitions)	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution				10	Bits
Absolute Error	$T_A = 25°C$		±.07	±.20	%
	$0°C \leq T_A \leq +55°C$		±.10	±.20	%
	$-20°C \leq T_A \leq +85°C$		±.13	±.39	%
Output Current					
Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
Zero-Scale	Logic Inputs = 2.5 V		±.002	±.25	μA
Power Supply Rejection	$\Delta V^+ = \Delta V^- = \pm 5\%$		±.06	±0.1	%/%
Output Resistance		0.2	1.2		MΩ
Switching Speed			600		ns
Logic Input High Voltage		2.1	2.5		V
Logic Input Low Voltage			0.4	0.7	V
Power Consumption			165	250	mW

NOTES:

(1) Rating applies for ambient temperatures to +85°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V^+ = 6.0$ V ±.01 V, $V^- = -6.0$ V ±.01 V, $V_{out} = 0$ V, $C_I = 200$ pF, and external resistor array as per Table 1.
(3) In Table 1, the maximum absolute value tolerance for $R_{E1} = \pm 10\%$.

TYPICAL FULL-SCALE OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

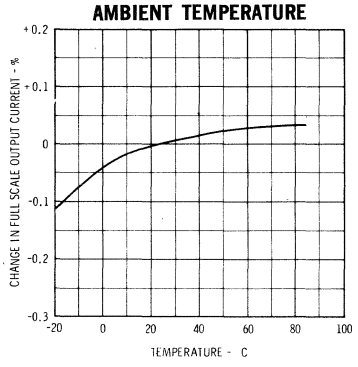
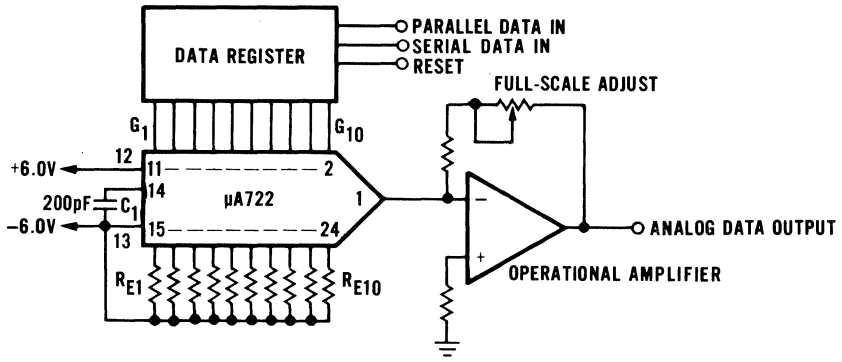


TABLE 1

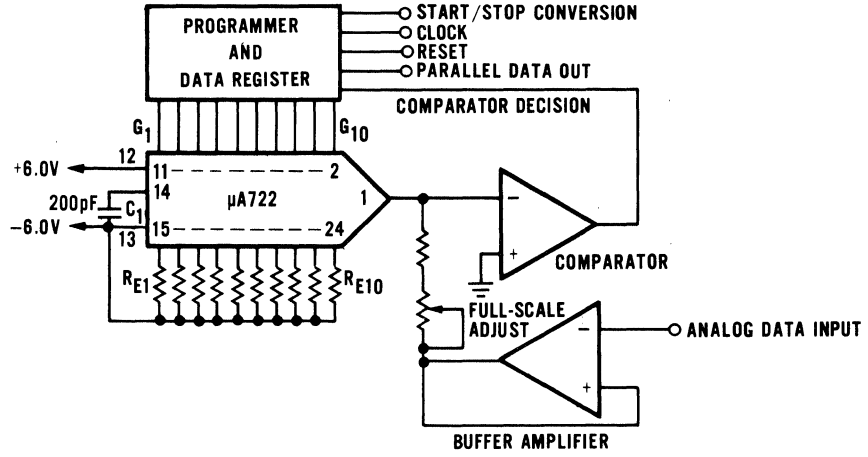
BINARY CODE RESISTOR ARRAY FOR 8 ± ½ BIT ACCURACY

Resistor Number (R_{EJ})	Nominal Value (kΩ)	Nominal Ratio (R_{EJ}/R_{E1})	Max. Ratio Tolerance ($T_A = 25°C$) (%)	Max. Ratio Temp. Coeff. (ppm/°C)
R_{E1}	2.547	1.000	Note 3	±5
R_{E2}	5.094	2.000	±0.02	±5
R_{E3}	10.245	4.022	±0.05	±10
R_{E4}	20.60	8.088	±0.10	±20
R_{E5}	41.43	16.265	±0.20	±20
R_{E6}	81.93	32.17	±0.20	±50
R_{E7}	163.4	64.16	±0.50	±100
R_{E8}	325.7	127.9	±1.0	±200
R_{E9}	644.9	253.2	±2.0	±500
R_{E10}	1275	500.8	±2.0	±500

TYPICAL DIGITAL-TO-ANALOG CONVERTER



TYPICAL ANALOG-TO-DIGITAL CONVERTER



DEFINITION OF TERMS

FULL SCALE OUTPUT CURRENT — The output current for all bits turned on.

ZERO SCALE OUTPUT CURRENT — The output current for all bits turned off.

ABSOLUTE ERROR — The worst-case deviation from a straight line drawn through zero and the 25°C value of the full-scale output current.

POWER SUPPLY REJECTION — The ratio of the percentage change in full-scale output current to the percentage change in supply voltage producing it.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at virtual ground and all bits turned on.

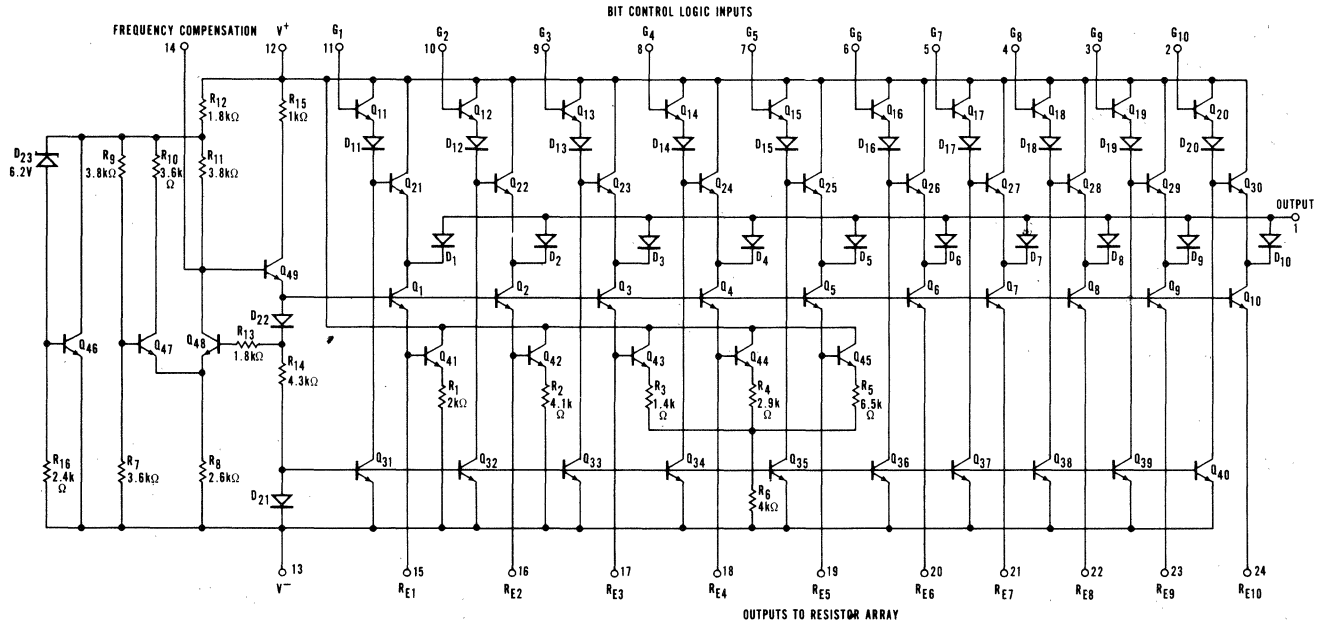
SWITCHING SPEED — The time required to turn on the least significant bit.

LOGIC INPUT HIGH VOLTAGE — The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE — The maximum voltage allowed at a bit control gate to hold the bit on.

POWER CONSUMPTION — The DC power required to operate the device; the power will vary with logic condition, but is specified as a maximum for the entire range of signal conditions.

SCHEMATIC DIAGRAM



μA722B

10-BIT CURRENT SOURCE

FAIRCHILD LINEAR INTEGRATED CIRCUITS

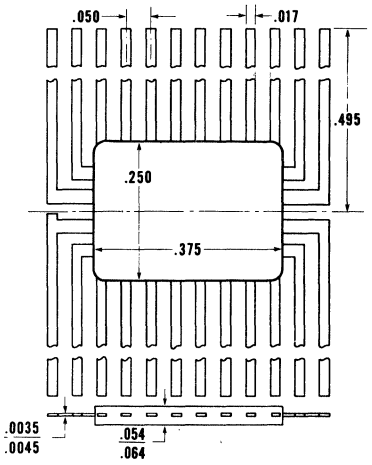
- **7 ±½ BIT ACCURACY FROM 0°C TO +55°C**
- **6 ± ½ BIT ACCURACY FROM −20°C TO +85°C**
- **600 ns SWITCHING SPEED**
- **INTERNAL PRECISION REFERENCE**
- **CCSL COMPATIBLE**

GENERAL DESCRIPTION — The μA722B is a high-speed, 10-bit precision current source intended for use in current-summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process, and consists of a reference supply, 10 current sources connected to a single output summing line, and associated logic switches. The full-scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μA722B is compatible with the Fairchild families of linear and digital circuits. For higher accuracy, see μA722 data sheet.

ABSOLUTE MAXIMUM RATINGS

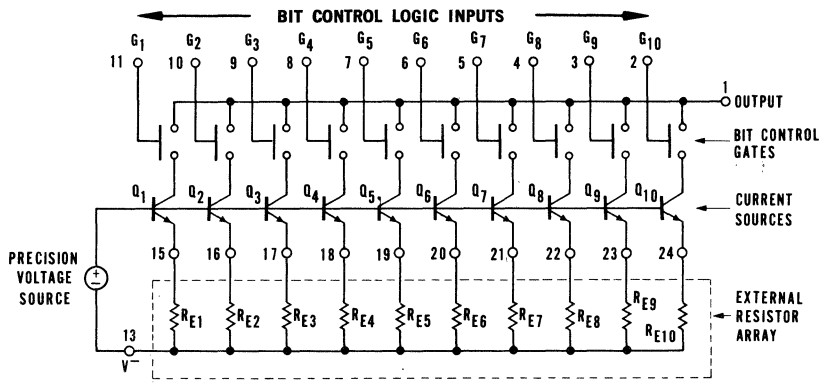
Voltage from V^+ to V^-	−0.5 V to +18 V
Voltage from Output to V^+	−12 V to +6 V
Voltage from Output to V^-	0 V to +12 V
Voltage from Logic Inputs to Output	−9 V to +7 V
Voltage from Logic Inputs to V^+	−18 V to 0 V
Voltage from Logic Inputs to V^-	0 V to +12 V
Internal Power Dissipation (Note 1)	450 mW
Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

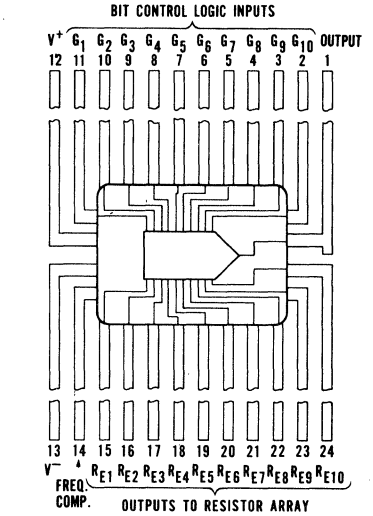


ORDER PART NO. U3M7722334

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 13 INTERNALLY CONNECTED TO CASE.

Notes on Page 2

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS

PARAMETER (See Definitions)	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution				10	Bits
Absolute Error	$T_A = 25°C$		±.08	±.39	%
	$0°C \leq T_A \leq +55°C$		±.17	±.39	%
	$-20°C \leq T_A \leq +85°C$		±.22	±.78	%
Output Current					
Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
Zero-Scale	Logic Inputs = 2.5 V		±.002	±.25	μA
Power Supply Rejection	$\Delta V^+ = \Delta V^- = \pm 5\%$		±.06	±0.1	%/%
Output Resistance		0.2	1.2		MΩ
Switching Speed			600		ns
Logic Input High Voltage		2.1	2.5		V
Logic Input Low Voltage			0.4	0.7	V
Power Consumption			165	250	mW

NOTES:

(1) Rating applies for ambient temperatures to +85°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V^+ = 6.00\ V \pm .01\ V$, $V^- = -6.00\ V \pm .01\ V$, $V_{out} = 0\ V$, $C_I = 200\ pF$, and external resistor array as per Table 1.
(3) In Table 1, the maximum absolute value tolerance for $R_{EI} = \pm 10\%$.

TYPICAL FULL-SCALE OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

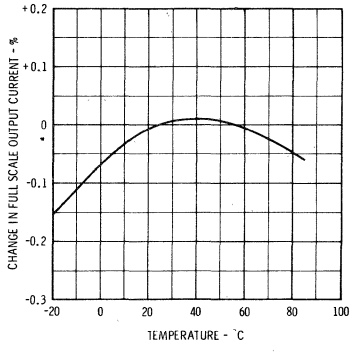
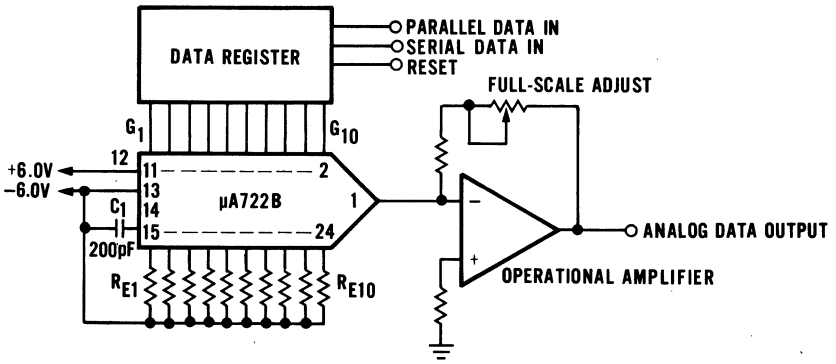


TABLE 1

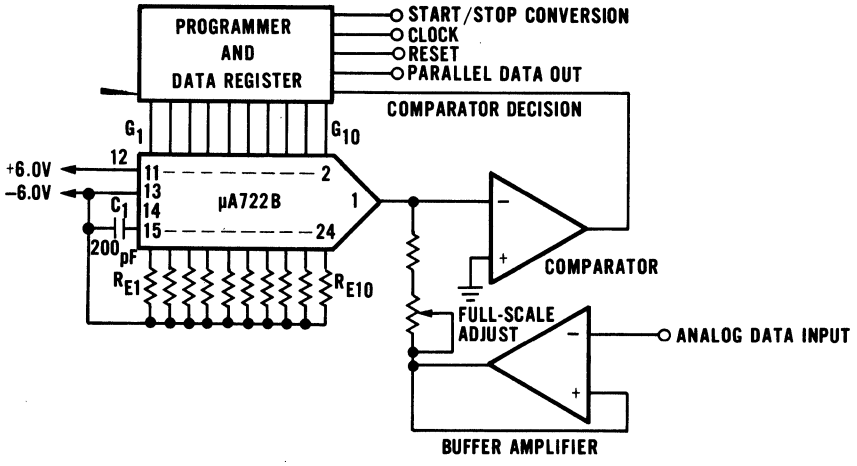
BINARY CODE RESISTOR ARRAY FOR 6 ± ½ BIT ACCURACY

Resistor Number (R_{EJ})	Nominal Value (kΩ)	Nominal Ratio (R_{EJ}/R_{EI})	Max. Ratio Tolerance ($T_A = 25°C$) (%)	Max. Ratio Temp. Coeff. (ppm/°C)
R_{EI}	2.547	1.000	Note 3	±20
R_{E2}	5.094	2.000	±0.10	±20
R_{E3}	10.245	4.022	±0.20	±50
R_{E4}	20.60	8.088	±0.20	±50
R_{E5}	41.43	16.265	±0.50	±100
R_{E6}	81.93	32.17	±0.50	±100
R_{E7}	163.4	64.16	±1.0	±500
R_{E8}	325.7	127.9	±1.0	±500
R_{E9}	644.9	253.2	±5.0	±1000
R_{E10}	1275	500.8	±5.0	±1000

TYPICAL DIGITAL-TO-ANALOG CONVERTER



TYPICAL ANALOG-TO-DIGITAL CONVERTER



DEFINITION OF TERMS

FULL SCALE OUTPUT CURRENT — The output current for all bits turned on.

ZERO SCALE OUTPUT CURRENT — The output current for all bits turned off.

ABSOLUTE ERROR — The worst-case deviation from a straight line drawn through zero and the 25°C value of the full-scale output current.

POWER SUPPLY REJECTION — The ratio of the percentage change in full-scale output current to the percentage change in supply voltage producing it.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at virtual ground and all bits turned on.

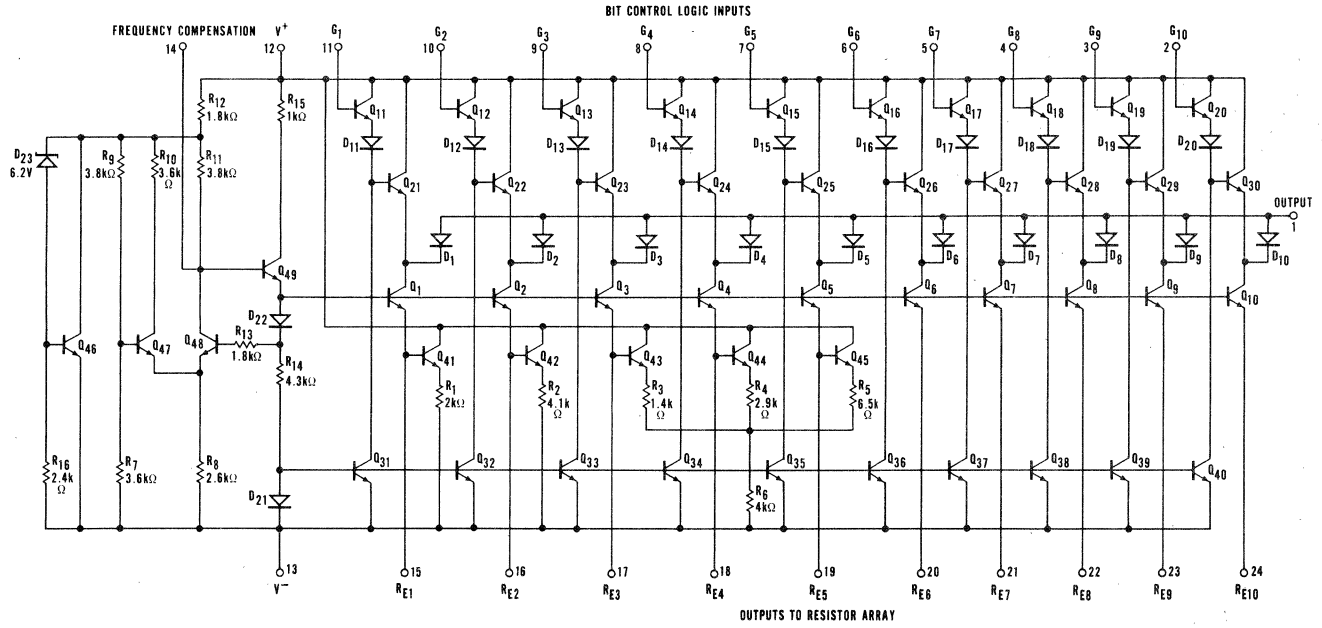
SWITCHING SPEED — The time required to turn on the least significant bit.

LOGIC INPUT HIGH VOLTAGE — The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE — The maximum voltage allowed at a bit control gate to hold the bit on.

POWER CONSUMPTION — The DC power required to operate the device; the power will vary with logic condition, but is specified as a maximum for the entire range of signal conditions.

SCHEMATIC DIAGRAM



μA723

PRECISION VOLTAGE REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

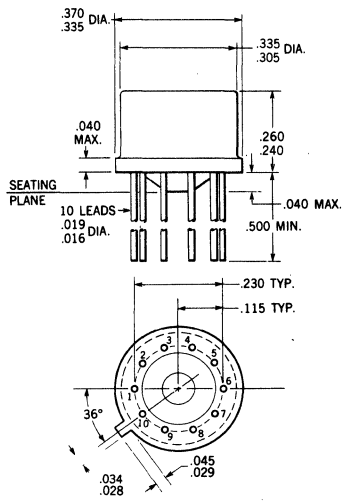
- **POSITIVE OR NEGATIVE SUPPLY OPERATION**
- **SERIES, SHUNT, SWITCHING OR FLOATING OPERATION**
- **.01% LINE AND LOAD REGULATION**
- **OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS**
- **OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR**

GENERAL DESCRIPTION — The μA723 is a monolithic voltage regulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V^+ to V^- (50 msec)	50 V
Continuous Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation Metal Can (Note 1)	800 mW
DIP (Note 1)	900 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

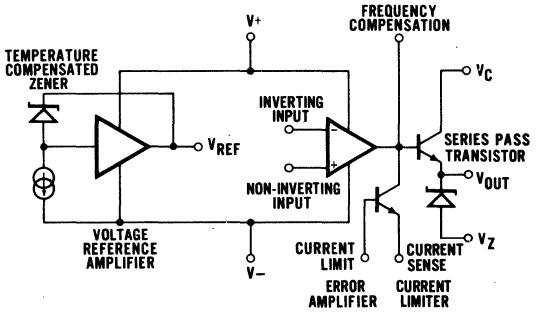
PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

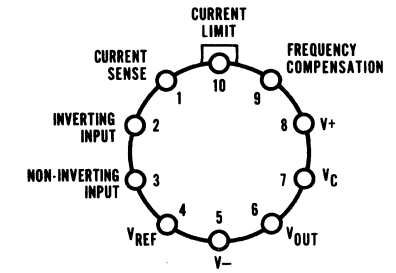
ORDER PART NO. U5R7723312

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

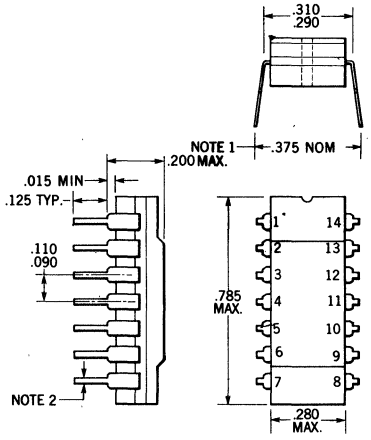
TOP VIEWS



NC	1	14	NC
CURRENT LIMIT	2	13	FREQUENCY COMPENSATION
CURRENT SENSE	3	12	V+
INVERTING INPUT	4	11	V_C
NON-INVERTING INPUT	5	10	V_{OUT}
V_{REF}	6	9	V_Z
V−	7	8	NC

Note: On metal can, pin 5 is connected to case

TYPICAL DUAL IN-LINE PACKAGE



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

ORDER PART NO. U6A7723393

Notes on Page 2.

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12$ V to $V_{IN} = 15$ V		.01	0.1	% V_{OUT}
	$V_{IN} = 12$ V to $V_{IN} = 40$ V		.02	0.2	% V_{OUT}
	$-55°C \leq T_A \leq +125°C$, $V_{IN} = 12$ V to $V_{IN} = 15$ V			0.3	% V_{OUT}
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		.03	0.15	% V_{OUT}
	$-55°C \leq T_A \leq +125°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, $C_{REF} = 0$		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$-55°C \leq T_A \leq +125°C$		.002	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\ \Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30$ V		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

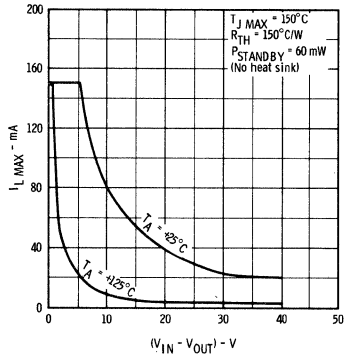
DEFINITION OF TERMS

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.
LOAD REGULATION — The percentage change in output voltage for a specified change in load current.
RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.
AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.
SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.
REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.
OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.
STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.
INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.
INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.
SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.
TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

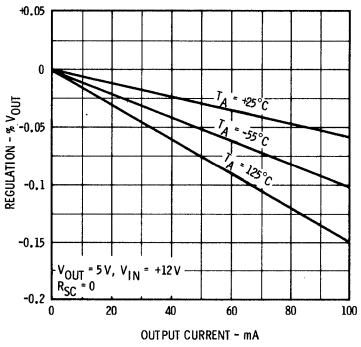
NOTES:
(1) Derate metal can package at 6.8 mW/°C and dual-in-line package at 9 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12$ V, $V^- = 0$, $V_{out} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, $C_1 = 100$ pF, $C_{REF} = 0$ and divider impedance as seen by error amplifier ≤ 10 KΩ connected as shown in Fig. 1.
(3) L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V^+ must be connected to a +3 V or greater supply.

TYPICAL PERFORMANCE CURVES

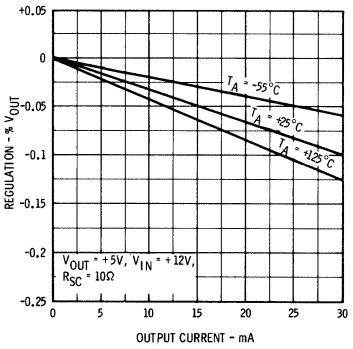
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



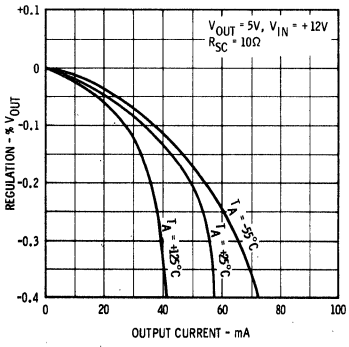
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



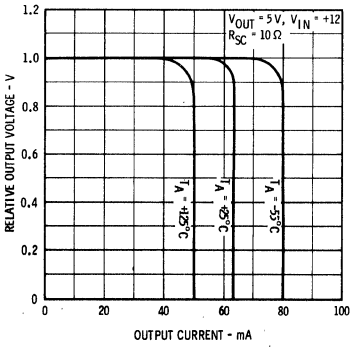
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



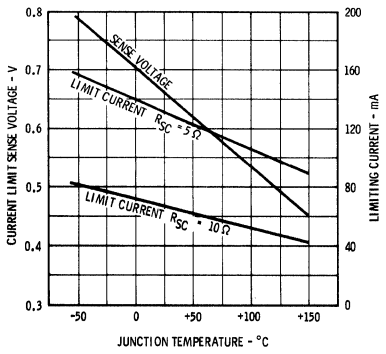
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



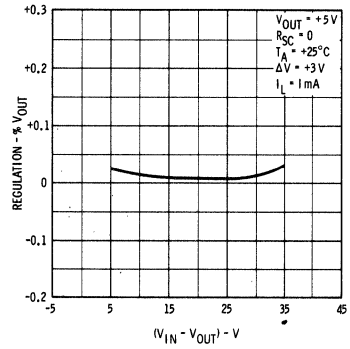
CURRENT LIMITING CHARACTERISTICS



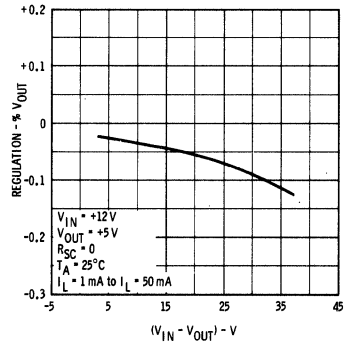
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



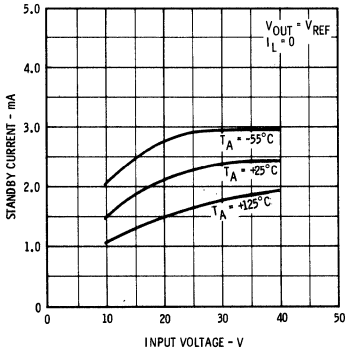
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



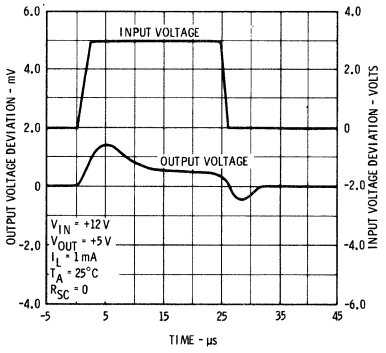
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



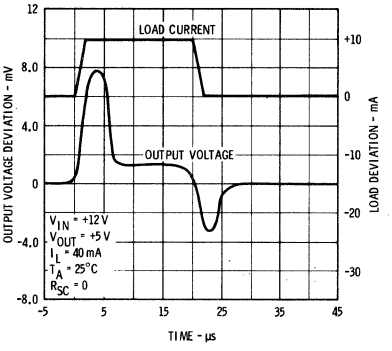
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

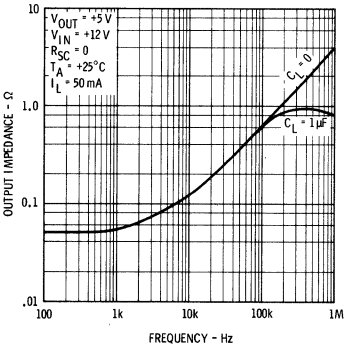


TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]\ ;\ R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]\ ;\ R_3 = R_4$$

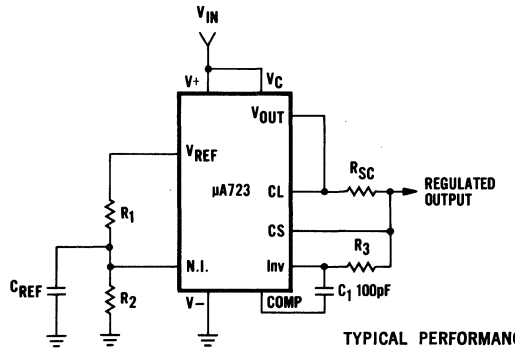
Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT}\, R_3}{R_{sc}\, R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{sc}\, R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$$

Figure 1

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



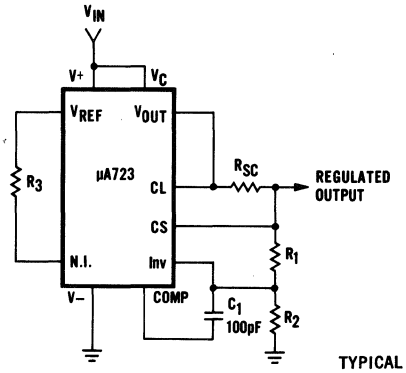
TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.

Figure 2

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



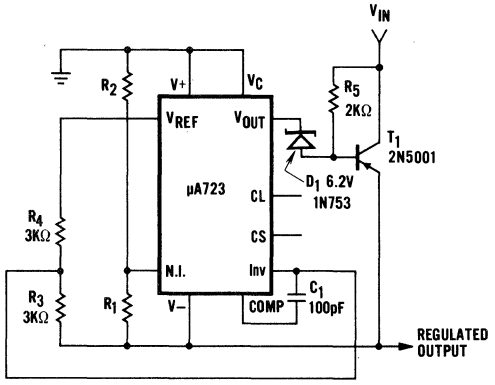
TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 3

NEGATIVE VOLTAGE REGULATOR

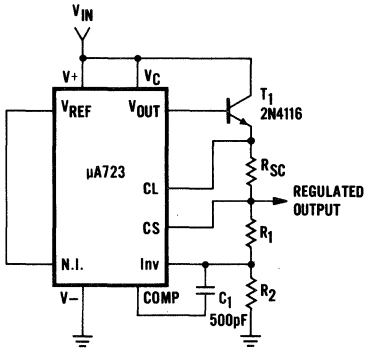


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Figure 4

POSITIVE VOLTAGE REGULATOR (External NPN Pass Transistor)

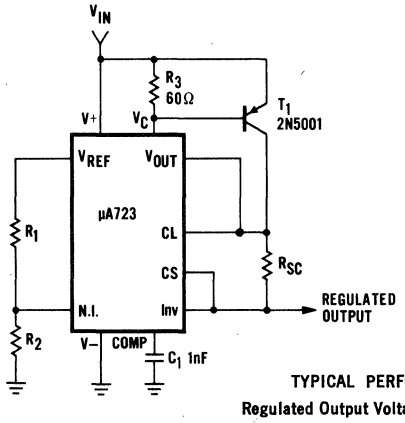


TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ A)	15 mV

Figure 5

POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)

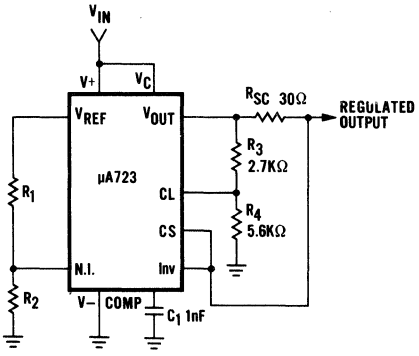


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

Figure 6

FOLDBACK CURRENT LIMITING

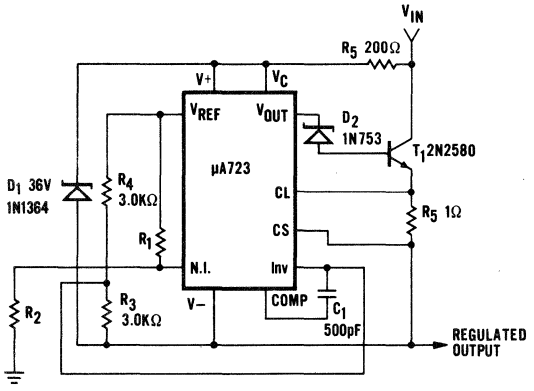


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Current Limit Knee	20 mA

Figure 7

POSITIVE FLOATING REGULATOR

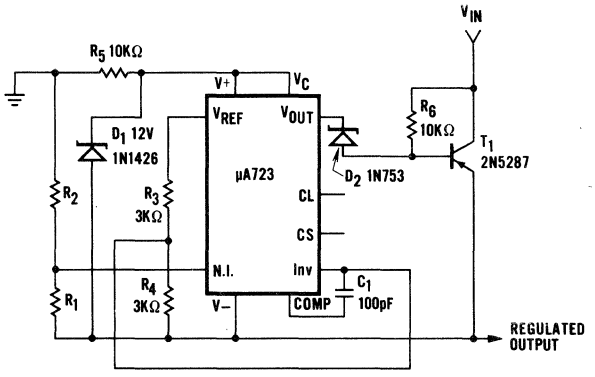


TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

Figure 8

NEGATIVE FLOATING REGULATOR

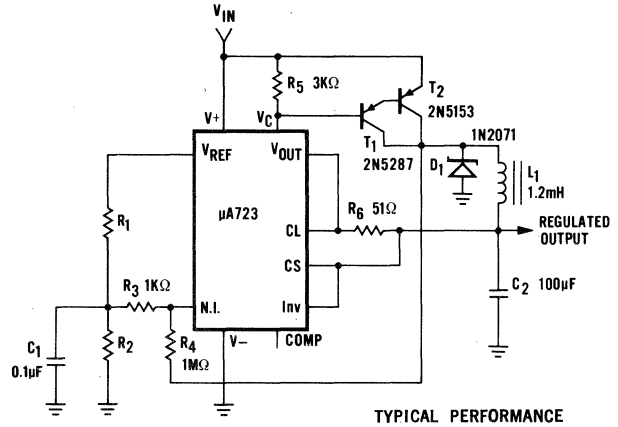


TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Figure 9

POSITIVE SWITCHING REGULATOR



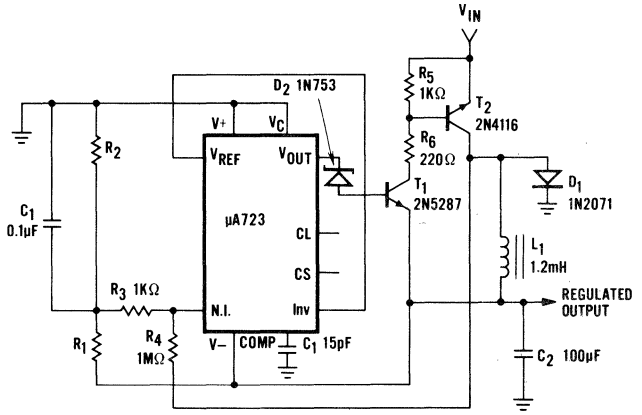
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 30$ V)	10 mV
Load Regulation ($\Delta I_L = 2$ A)	80 mV

Note 3

Figure 10

NEGATIVE SWITCHING REGULATOR



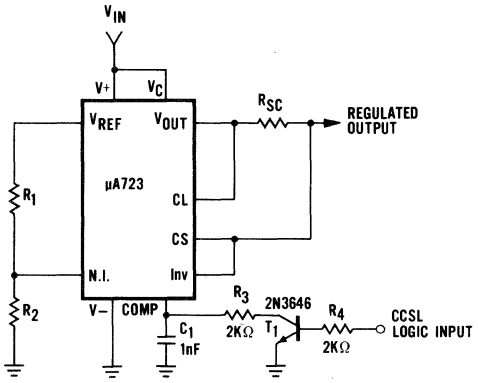
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 20$ V)	8 mV
Load Regulation ($\Delta I_L = 2$ A)	6 mV

Note 3

Figure 11

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



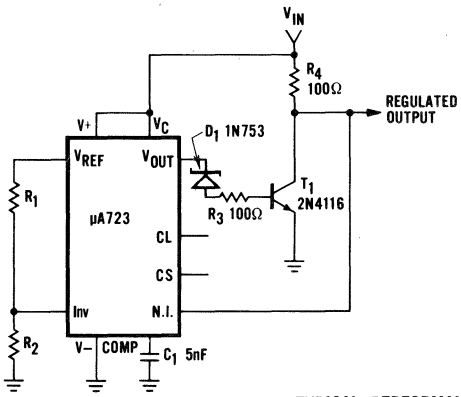
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 12

SHUNT REGULATOR

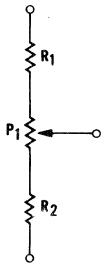


TYPICAL PERFORMANCE

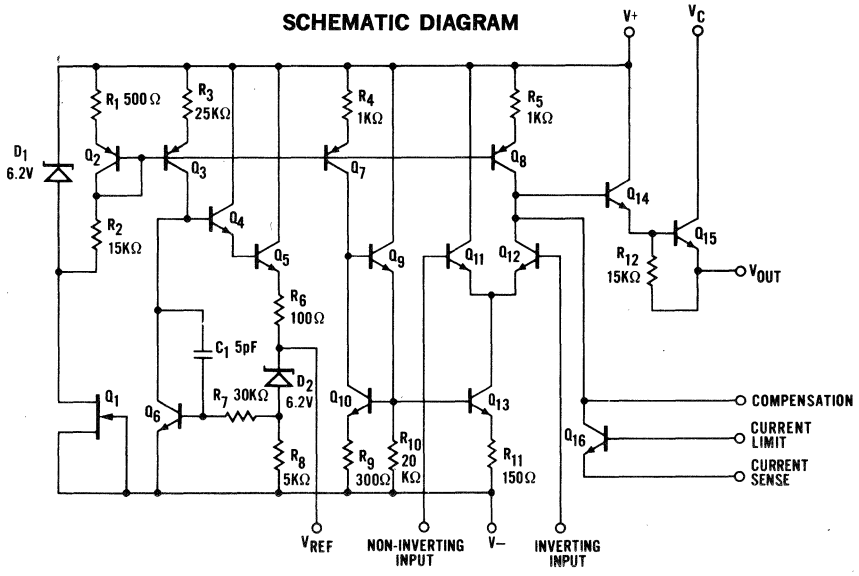
Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 10$ V)	0.5 mV
Load Regulation (ΔI_L=100 mA)	1.5 mV

Figure 13

OUTPUT VOLTAGE ADJUST



SCHEMATIC DIAGRAM



μA723C

PRECISION VOLTAGE REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

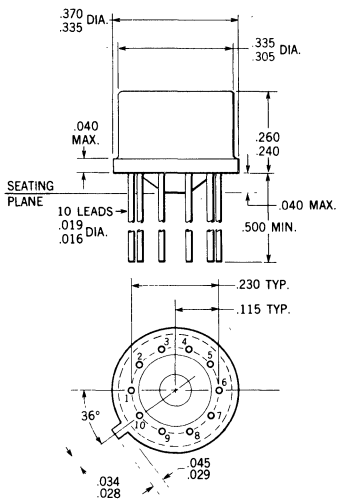
- **POSITIVE OR NEGATIVE SUPPLY OPERATION**
- **SERIES, SHUNT, SWITCHING OR FLOATING OPERATION**
- **.01% LINE AND LOAD REGULATION**
- **OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS**
- **OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR**

GENERAL DESCRIPTION — The μA723C is a monolithic voltage regulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723C is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits. For full temperature range operation (−55°C to +125°C), see μA723 data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation—Metal Can (Note 1)	800 mW
Internal Power Dissipation—DIP (Note 1)	900 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

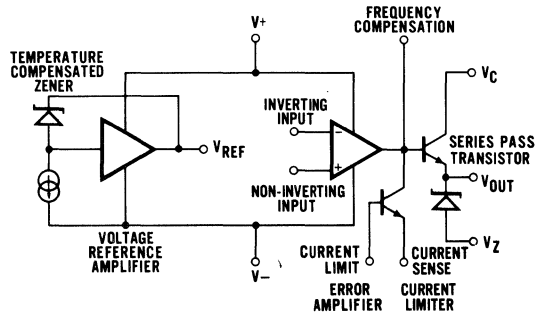
PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

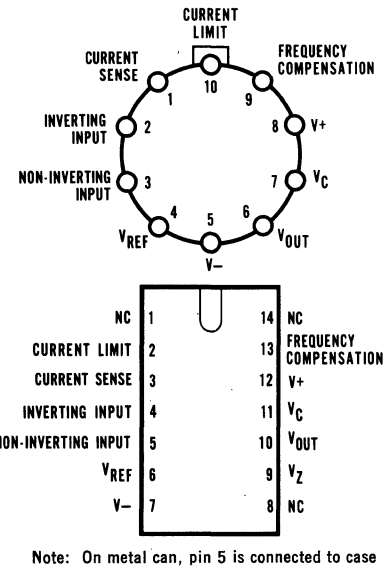
ORDER PART NO. U5R7723393

EQUIVALENT CIRCUIT



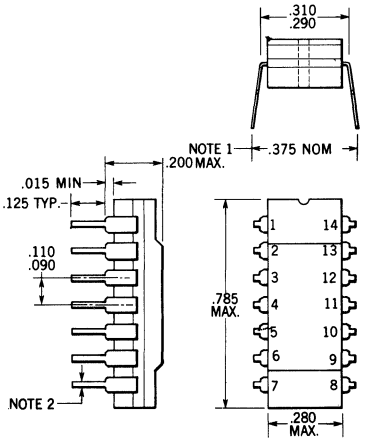
CONNECTION DIAGRAMS

TOP VIEWS



Note: On metal can, pin 5 is connected to case

TYPICAL DUAL IN-LINE PACKAGE



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

ORDER PART NO. U6A7723393

Notes on Page 2.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12$ V to $V_{IN} = 15$ V		.01	0.1	% V_{OUT}
	$V_{IN} = 12$ V to $V_{IN} = 40$ V		0.1	0.5	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $V_{IN} = 12$ V to $V_{IN} = 15$ V			0.3	% V_{OUT}
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		.03	0.2	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, $C_{REF} = 0$		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$0°C \leq T_A \leq 70°C$		.003	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\ \Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30$ V		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

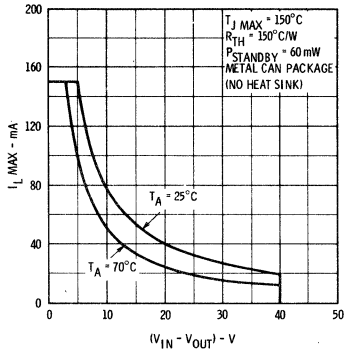
DEFINITION OF TERMS

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.
LOAD REGULATION — The percentage change in output voltage for a specified change in load current.
RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.
AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.
SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.
REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.
OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.
STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.
INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.
INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.
SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.
TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

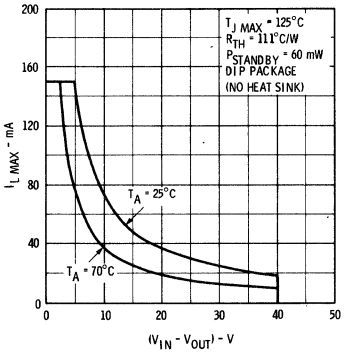
NOTES:
(1) Derate metal can package at 6.8 mW/°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12$ V, $V^- = 0$, $V_{out} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, $C_1 = 100$ pF, $C_{REF} = 0$, divider impedance as seen by error amplifier ≤ 10 kΩ, and connected as shown in Figure 1.
(3) For metal can applications where V_Z is required, an external 6.2 zener should be connected in series with V_{out}.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite side of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V^+ must be connected to a +3 V or greater supply.
(7) L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.

TYPICAL PERFORMANCE CURVES

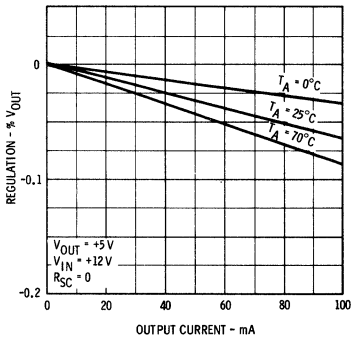
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



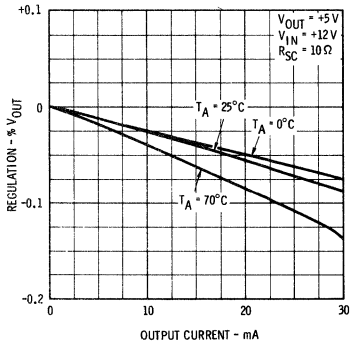
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



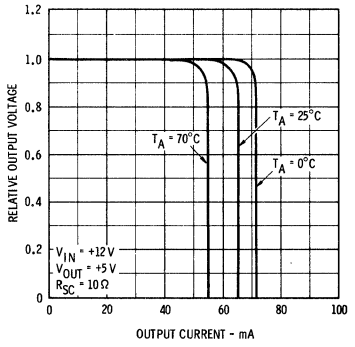
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



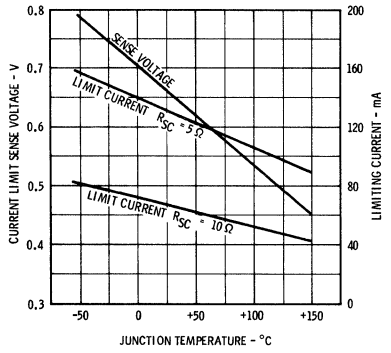
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



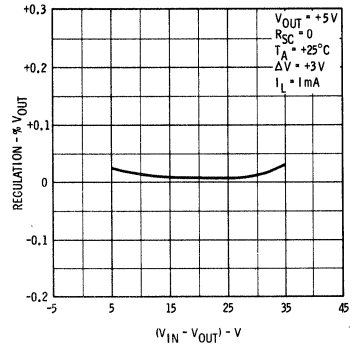
CURRENT LIMITING CHARACTERISTICS



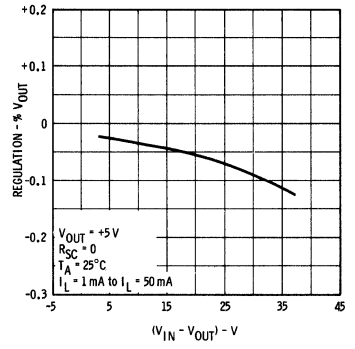
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



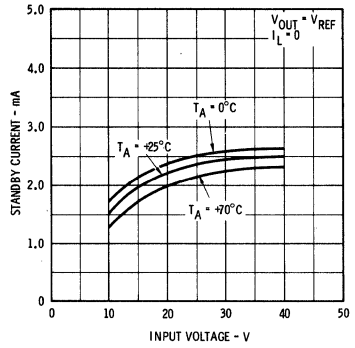
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



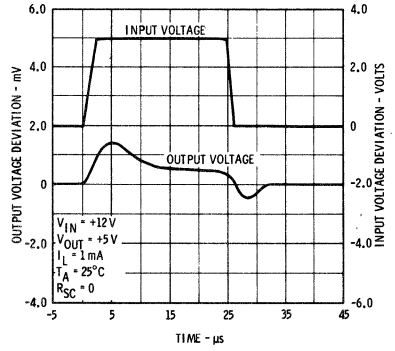
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



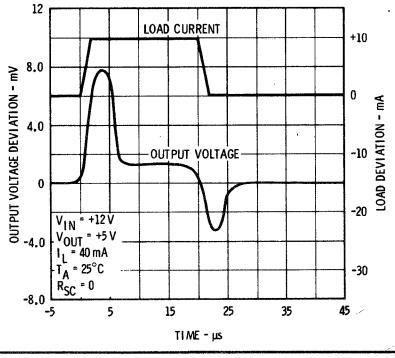
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

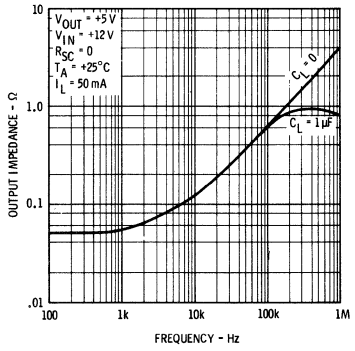


TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]\ ;\ R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

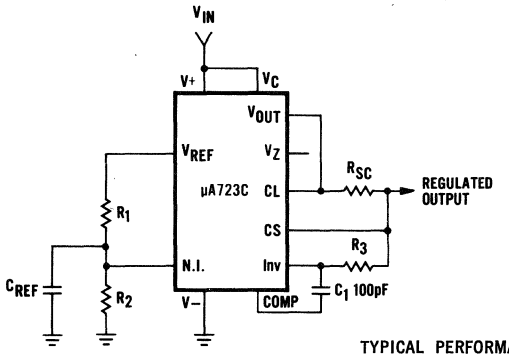
$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]\ ;\ R_3 = R_4$$

Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT}\, R_3}{R_{sc}\, R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{sc}\, R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$$

Figure 1
BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)

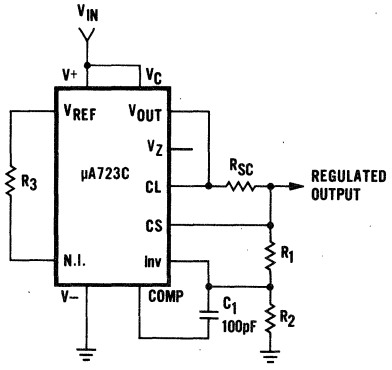


TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 2
BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)

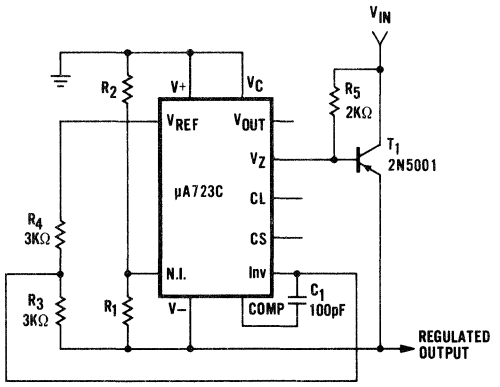


TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 3
NEGATIVE VOLTAGE REGULATOR

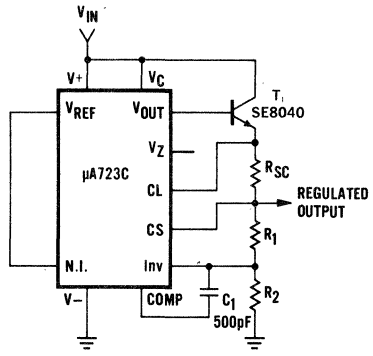


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Note 3

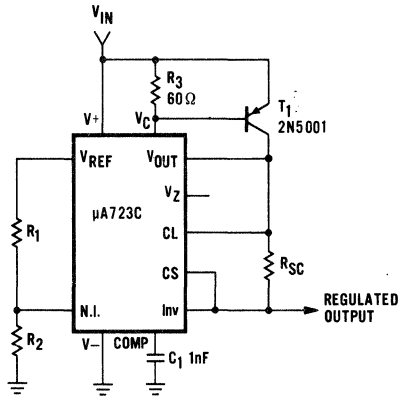
Figure 4
POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ A)	15 mV

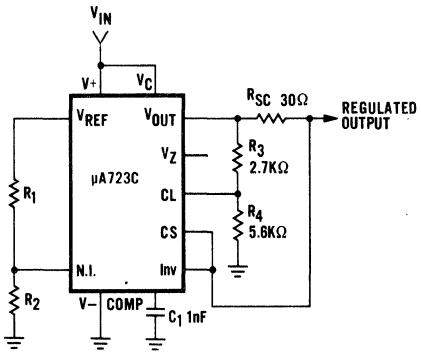
Figure 5
POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

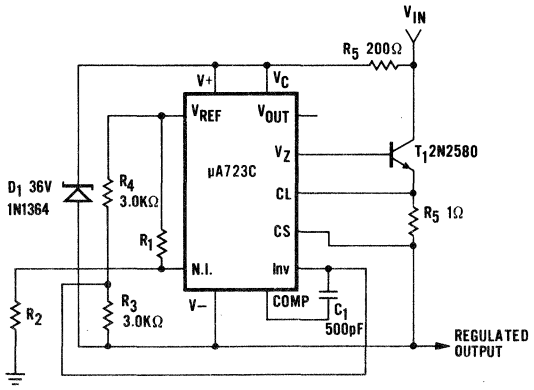
Figure 6
FOLDBACK CURRENT LIMITING



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Current Limit Knee	20 mA

Figure 7
POSITIVE FLOATING REGULATOR

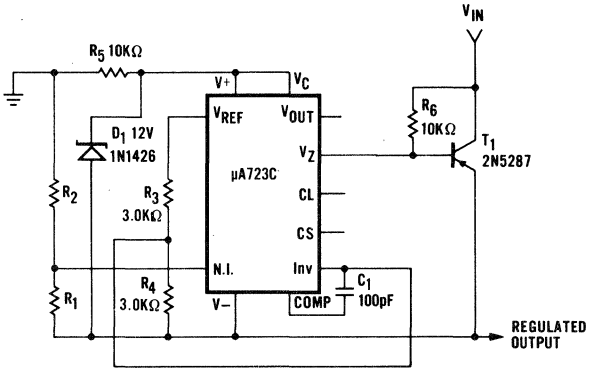


TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

Note 3

Figure 8
NEGATIVE FLOATING REGULATOR

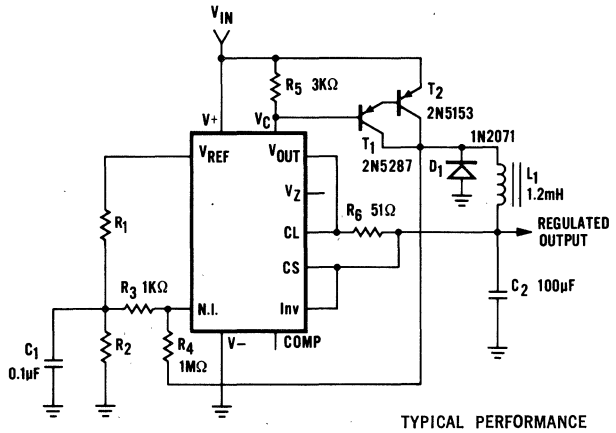


TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Note 3

Figure 9
POSITIVE SWITCHING REGULATOR

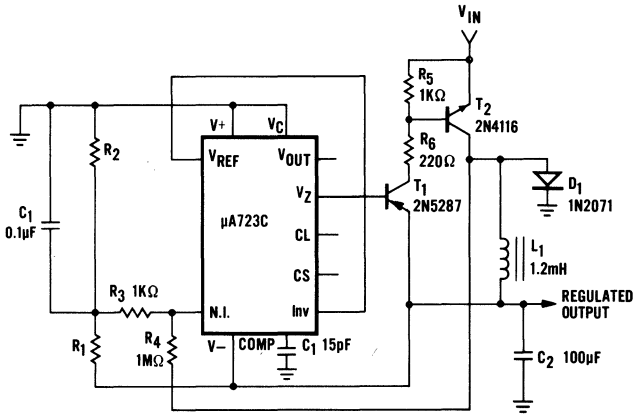


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 30$ V)	10 mV
Load Regulation ($\Delta I_L = 2$ A)	80 mV

Note 7

Figure 10
NEGATIVE SWITCHING REGULATOR

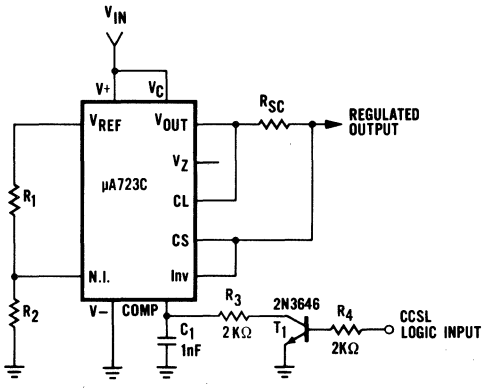


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 20$ V)	8 mV
Load Regulation ($\Delta I_L = 2$ A)	6 mV

Note 3
Note 7

Figure 11
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

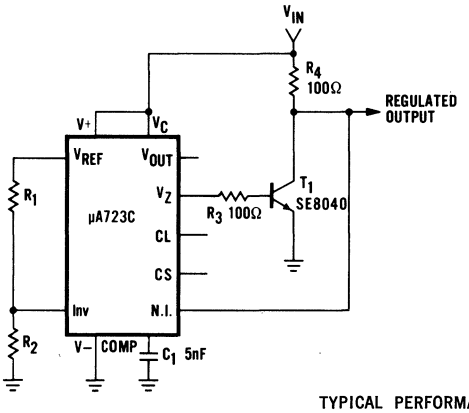


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 12
SHUNT REGULATOR

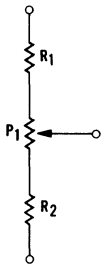


TYPICAL PERFORMANCE

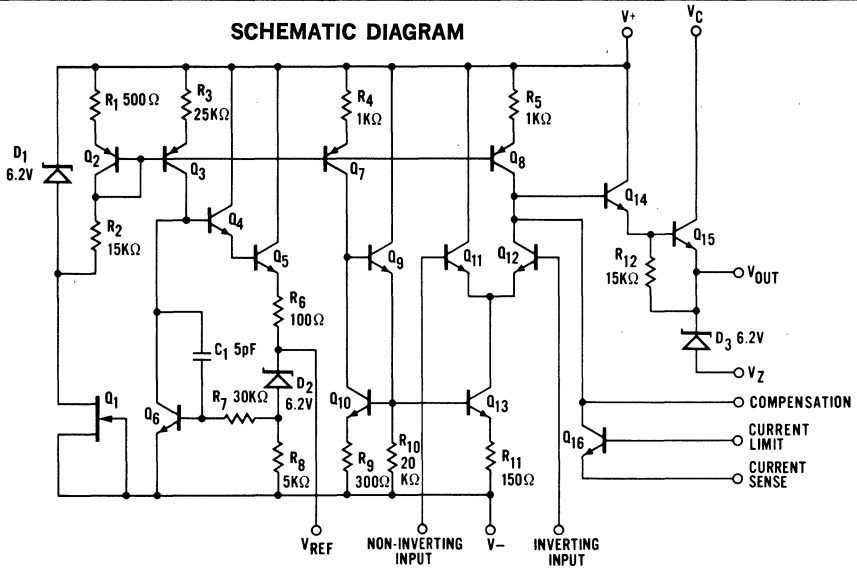
Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 10$ V)	0.5 mV
Load Regulation (ΔI_L=100 mA)	1.5 mV

Note 3

Figure 13
OUTPUT VOLTAGE ADJUST



SCHEMATIC DIAGRAM



μA726

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA726 is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

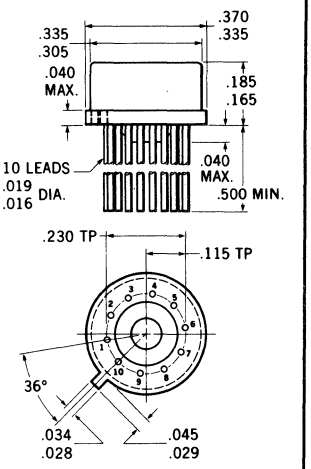
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 seconds)	300°C
Supply Voltage	±18 V

MAXIMUM RATINGS FOR EACH TRANSISTOR

Maximum collector-to-substrate voltage	40 V
BV_{CBO}	40 V
LV_{CEO} [Note 1]	30 V
BV_{EBO}	5 V
Collector Current	5 mA

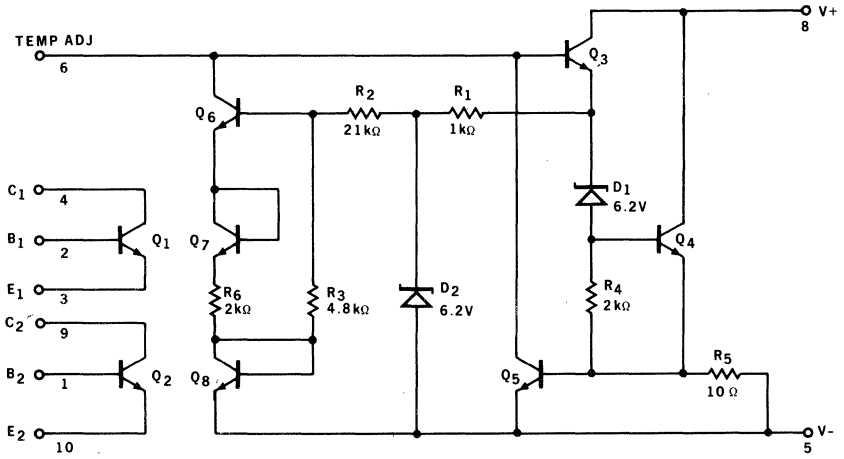
PHYSICAL DIMENSIONS



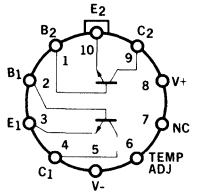
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5J772631X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

Note 1: Measured at 1 mA collector current.

* Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

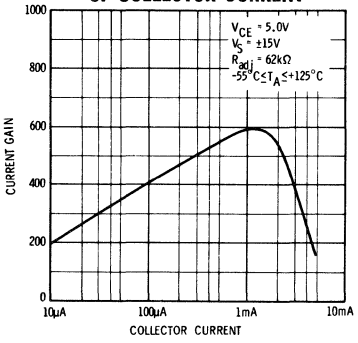
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15$ V, $R_{adj} = 62$ kΩ unless otherwise specified)

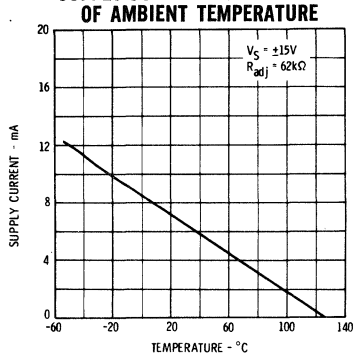
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\ \mu A \leq I_C \leq 100\ \mu A$ $V_{CE} = 5$ V, $R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		10	50	nA
Input Offset Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		50	200	nA
Average Input Bias Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		50	150	nA
Average Input Bias Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		250	500	nA
Offset Voltage Change	$I_C = 10\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 100$ kΩ		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 10$ kΩ		0.3	6.0	mV
Input Offset Voltage Drift	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$		0.2	1.0	μV/°C
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$		0.2	1.0	μV/°C
Input Offset Current Drift	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		10		pA/°C
Input Offset Current Drift	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		30		pA/°C
Supply Voltage Rejection Ratio	$10\mu A \leq I_C \leq 100\ \mu A$, $R_S \leq 50\Omega$,		25		μV/V
Low-Frequency Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$ BW = .001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$ BW = 0.1 Hz to 10 kHz		10		μV pp
Long-term Drift	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	$f = 20$ MHz, $I_C = 100\ \mu A$, $V_{CE} = 5$ V	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5$ V		1.0		pF
Emitter Transition Capacitance	$I_E = 100\ \mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\ \mu A$, $I_C = 1$ mA		0.5	1.0	V

TYPICAL PERFORMANCE CURVES

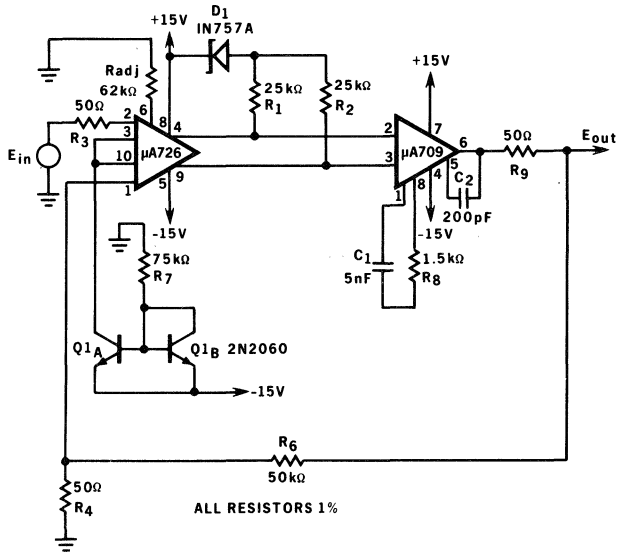
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 CIRCUIT



μA726C

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION—The μA726C is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process. For full temperature range (−55°C to +125°C) see μA726 data sheet.

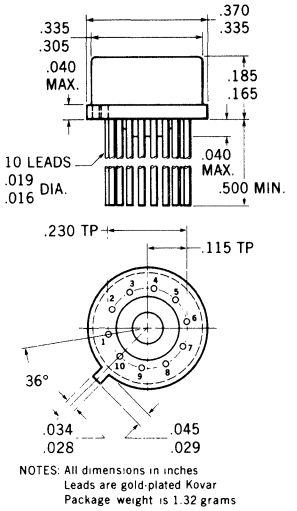
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C
Supply Voltage	±18V

MAXIMUM RATINGS FOR EACH TRANSISTOR

Maximum collector-to-substrate voltage	40V
BV_{CBO}	40V
LV_{CEO} (Note 1)	30V
BV_{EBO}	5V
Collector Current	5 mA

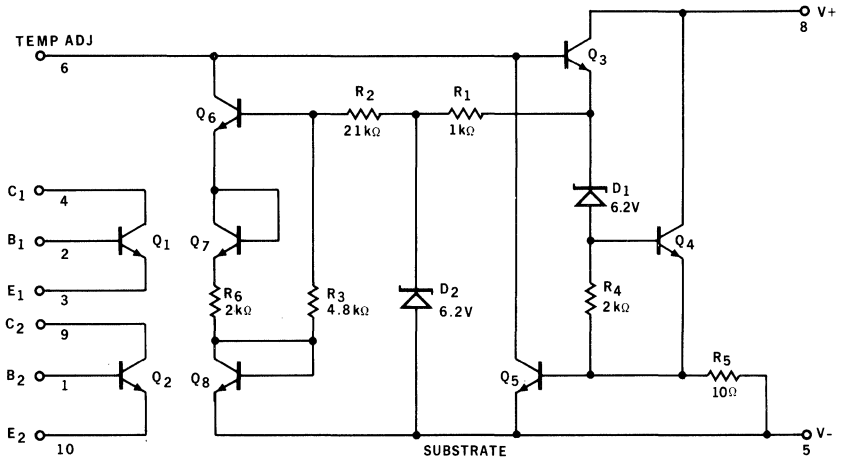
PHYSICAL DIMENSIONS



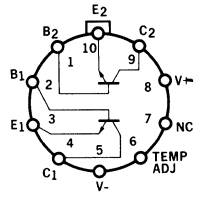
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5J772632X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

NOTE: (1) Measured at 1 mA collector current.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

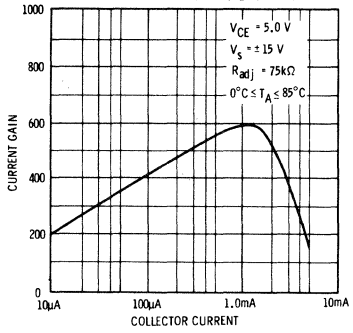
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +85°C$, $V_S = \pm 15V$, $R_{adj} = 75\,k\Omega$ unless otherwise specified)

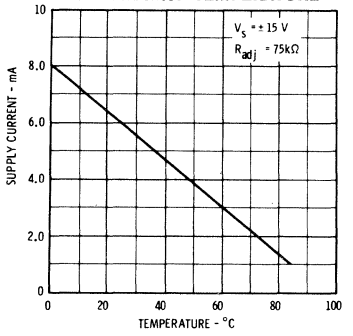
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\,\mu A \leq I_C \leq 100\,\mu A$ $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	3.0	mV
Input Offset Current	$I_C = 10\,\mu A$, $V_{CE} = 5V$		10	100	nA
Input Offset Current	$I_C = 100\,\mu A$, $V_{CE} = 5V$		50	400	nA
Average Input Bias Current	$I_C = 10\,\mu A$, $V_{CE} = 5V$		50	300	nA
Average Input Bias Current	$I_C = 100\,\mu A$, $V_{CE} = 5V$		250	1000	nA
Offset Voltage Change	$I_C = 10\,\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100\,k\Omega$		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\,\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10\,k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$I_C = 100\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		0.2	2.0	μV/°C
Input Offset Current Drift	$I_C = 10\,\mu A$, $V_{CE} = 5V$		10		pA/°C
Input Offset Current Drift	$I_C = 100\,\mu A$, $V_{CE} = 5V$		30		pA/°C
Supply Voltage Rejection Ratio	$I_C = 100\,\mu A$, $R_S = 50\Omega$		25		μV/V
Low-Frequency Noise	$I_C = 10\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	$I_C = 10\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10 kHz		10		μV pp
Long-Term Drift	$I_C = 100\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High-Frequency Current Gain	$f = 20$ MHz, $I_C = 100\,\mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\,\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\,\mu A$, $I_C = 1$ mA		0.5	1.0	V

TYPICAL PERFORMANCE CURVES

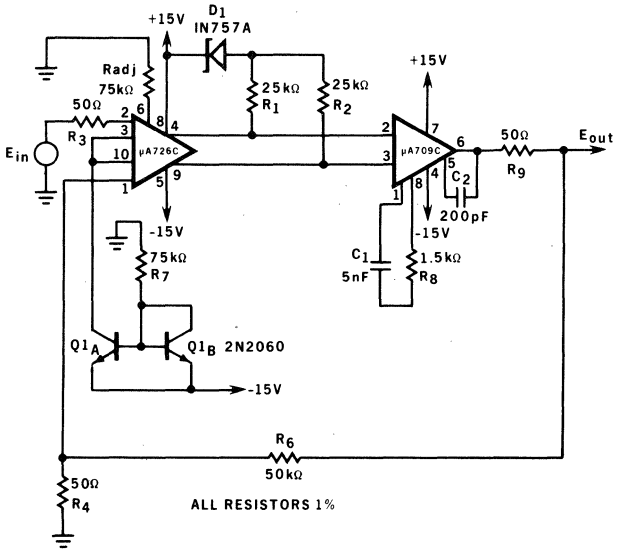
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 CIRCUIT



μA727

TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE**
- **WIDE COMMON MODE RANGE**

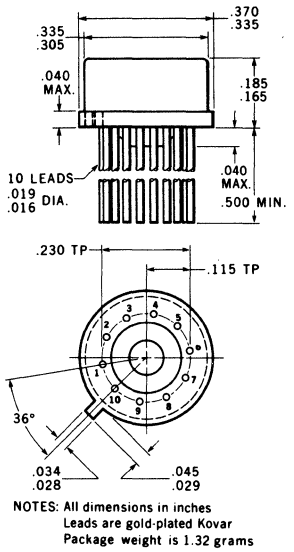
GENERAL DESCRIPTION — The μA727 is a monolithic, fixed gain, differential-input differential-output amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gage transducers, and A to D converters.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

PHYSICAL DIMENSIONS

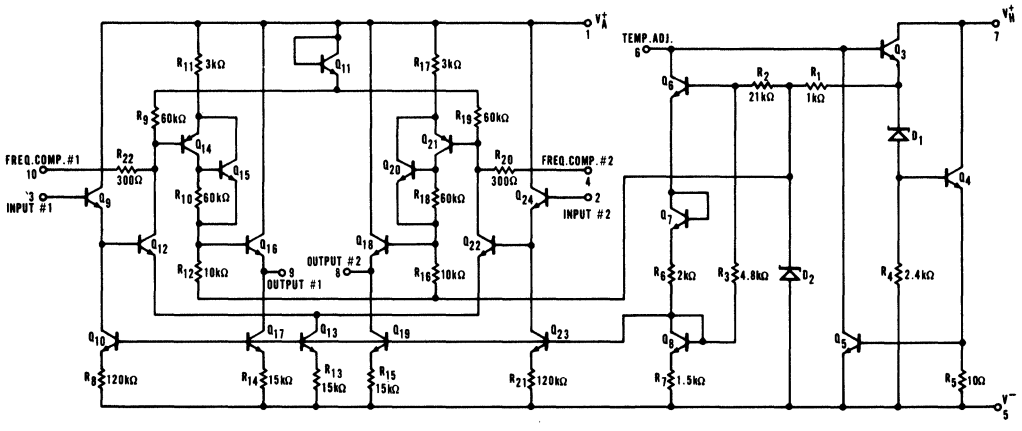
(In accordance with JEDEC TO-100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

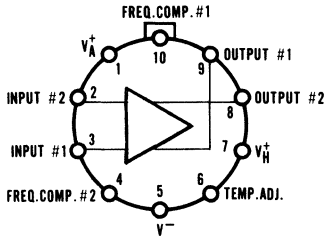
ORDER PART NO. U5J7727312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(Top View)



*Planar is a patented Fairchild process.

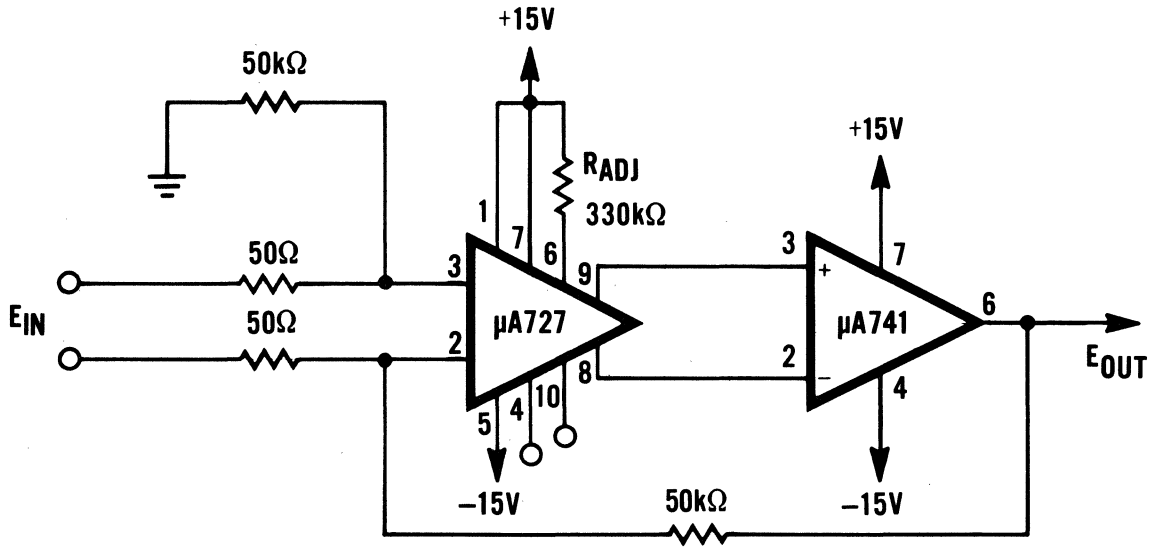
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_H^+ = V_A^+ = +15$ V, $V^- = -15$ V, $R_{ADJ} = 330$ kΩ, unless otherwise specified)

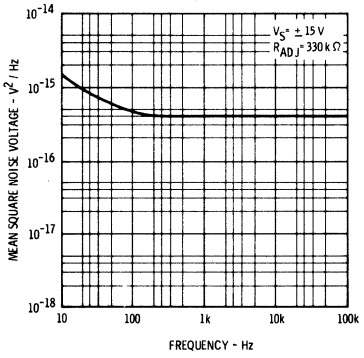
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0	10	mV
Input Offset Current			2.5	15	nA
Input Bias Current			12	40	nA
Input Offset Voltage Drift	$R_S \leq 50\ \Omega$, $+25°C \leq T_A \leq +125°C$		0.6	1.5	μV/°C
	$R_S \leq 50\ \Omega$, $-55°C \leq T_A \leq +25°C$		0.6	1.5	μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		2.0		pA/°C
	$-55°C \leq T_A \leq +25°C$		2.0		pA/°C
Input Bias Current Drift	$-55°C \leq T_A \leq +125°C$		15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ	80	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−6.0	−5.0	−4.0	V
Differential Output Voltage Swing		±5.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	10	μV/μA
Differential Voltage Gain		60	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\ \Omega$		3.0		μVrms
Long Term Drift	$R_S \leq 50\ \Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL X1000 CIRCUIT

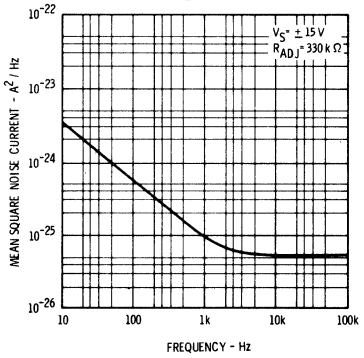


TYPICAL PERFORMANCE CURVES

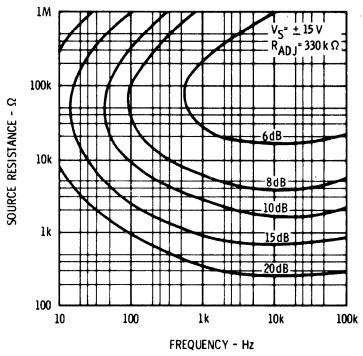
NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



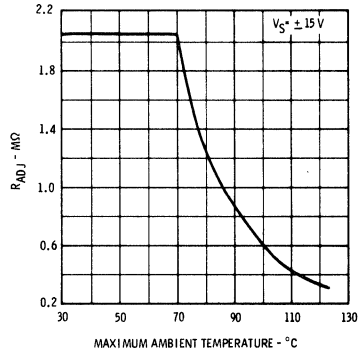
NOISE CURRENT AS A FUNCTION OF FREQUENCY



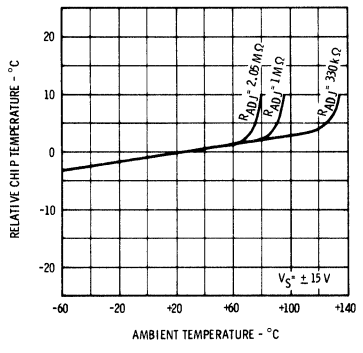
SPOT NOISE FIGURE CONTOURS



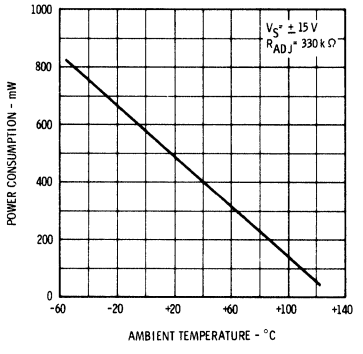
RECOMMENDED R_{ADJ} AS A FUNCTION OF MAXIMUM AMBIENT TEMPERATURE



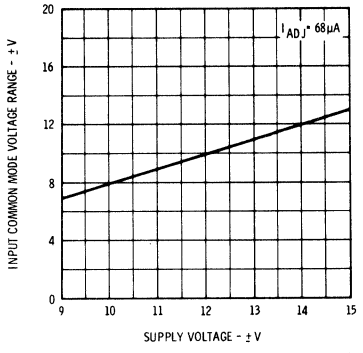
RELATIVE CHIP TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE



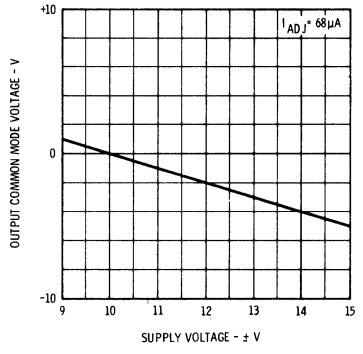
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



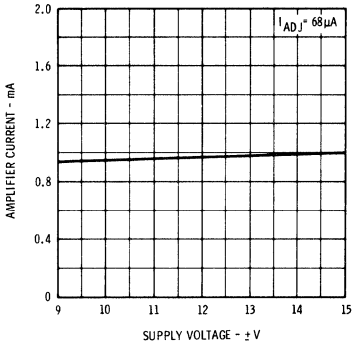
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



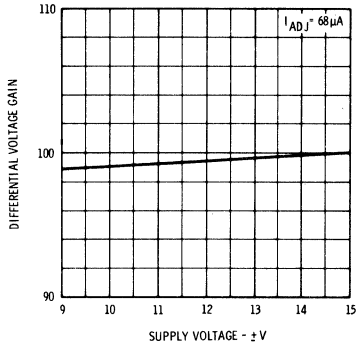
OUTPUT COMMON MODE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



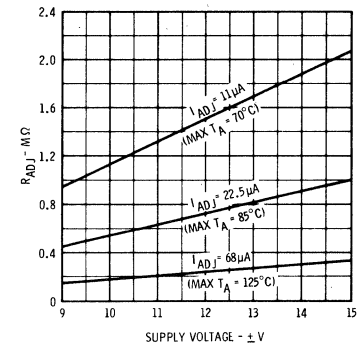
AMPLIFIER CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



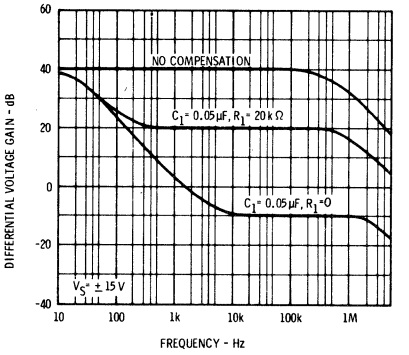
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



REQUIRED R_{ADJ} FOR CONSTANT I_{ADJ} AS A FUNCTION OF SUPPLY VOLTAGE



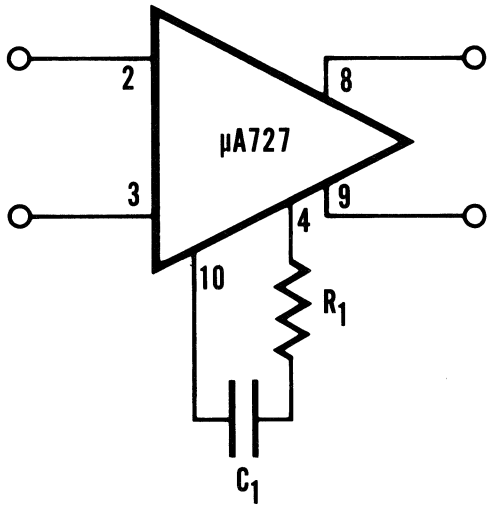
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero differential output voltage.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the differential output at zero.
DIFFERENTIAL INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
COMMON MODE INPUT RESISTANCE — The resistance looking into both inputs tied together.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT VOLTAGE RANGE — A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in differential output voltage to the change in differential input voltage producing it.
DIFFERENTIAL OUTPUT VOLTAGE SWING — The peak differential output swing that can be obtained without clipping.
OUTPUT RESISTANCE — The resistance seen looking into either output terminal with the differential output at zero.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.
OUTPUT COMMON MODE VOLTAGE — The average voltage at the two output terminals referred to ground.
OUTPUT SINK CURRENT — The maximum negative current that can be supplied by each output.
DIFFERENTIAL LOAD REJECTION — The ratio of the change in input offset voltage to the change in differential load current producing it.
I_{ADJ} — The current into terminal 6.

FREQUENCY COMPENSATION CIRCUIT



μA727B

TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE**
- **WIDE COMMON MODE RANGE**

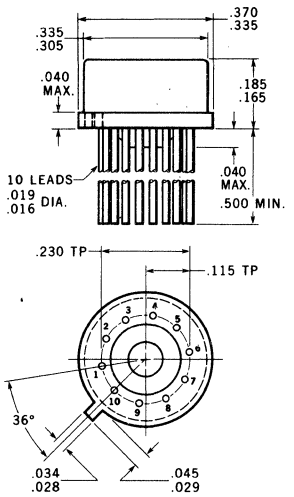
GENERAL DESCRIPTION — The μA727B is a monolithic, fixed gain, differential-input differential-output amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gage transducers, and A to D converters. For full temperature range operation (−55°C to +125°C) see μA727 data sheet.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

PHYSICAL DIMENSIONS

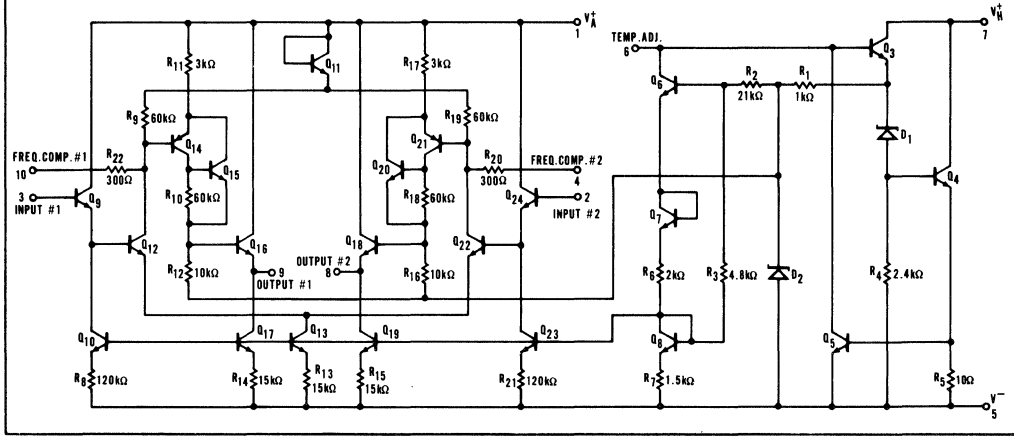
(in accordance with JEDEC TO-100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

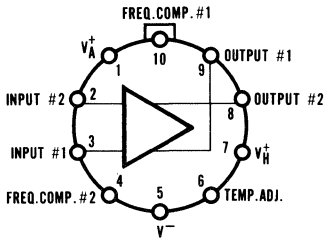
ORDER PART NO. U5J7727333

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(top view)



*Planar is a patented Fairchild process.

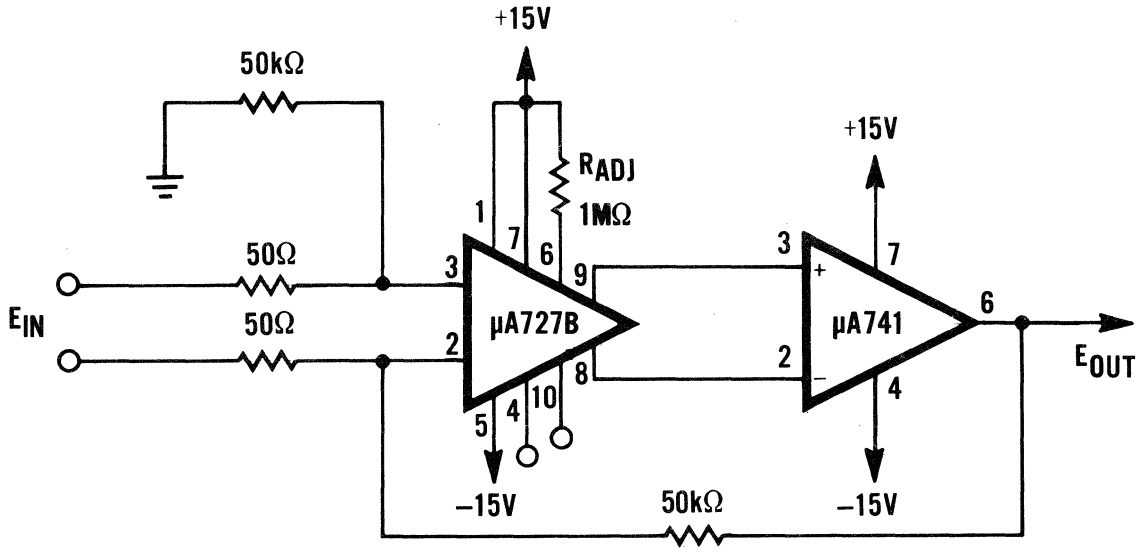
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($-20°C \leq T_A \leq +85°C$, $V_H^+ = V_A^+ = +15$ V, $V^- = -15$ V, $R_{ADJ} = 680$ KΩ, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0	10	mV
Input Offset Current			2.5	25	nA
Input Bias Current			12	75	nA
Input Offset Voltage Drift	$R_S \leq 50\ \Omega$		0.6	3.0	μV/°C
Input Offset Current Drift			2.0		pA/°C
Input Bias Current Drift			15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ	70	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−7.0	−5.0	−4.0	V
Differential Output Voltage Swing		±3.0	±7.0	±10.0	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	15.0	μV/μA
Differential Voltage Gain		50	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\ \Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\ \Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL X1000 CIRCUIT



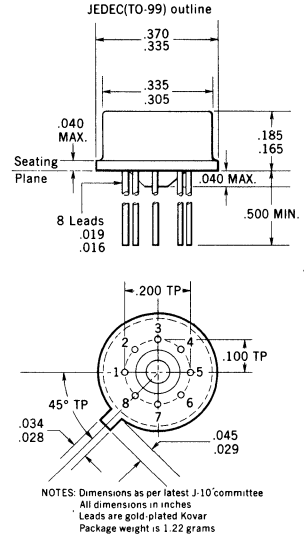
μA730
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA730 is a differential amplifier constructed on a single silicon-chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

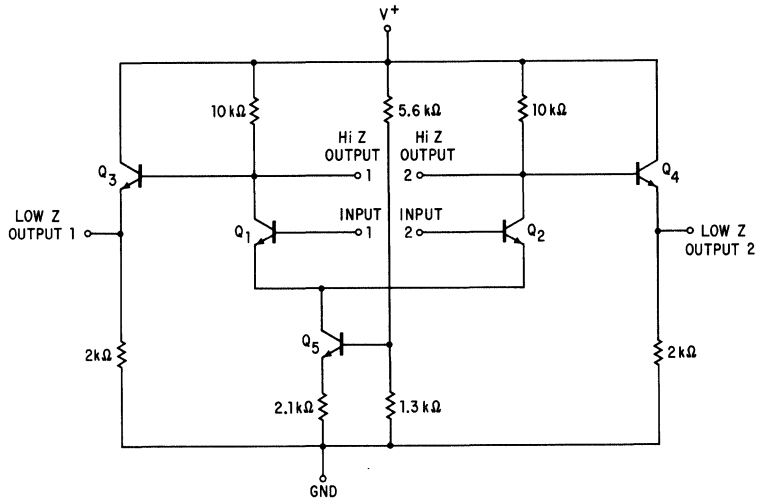
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline



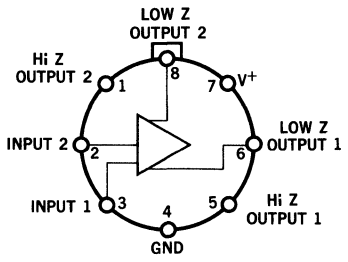
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

Order Part No. U5B773031X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top View)



Note: Pin 4 connected to case

NOTES:
(1) Rating applies for case temperature to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

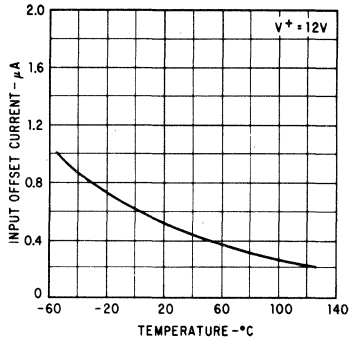
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, V+ = 12.0 V, and $V_{CM} = 3.5$ V unless otherwise specified)

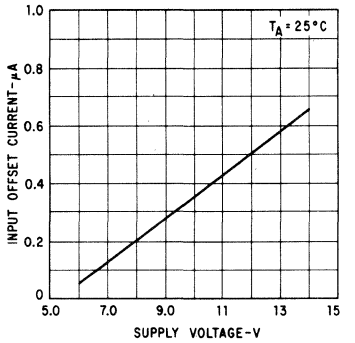
PARAMETER (See Definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current			0.5	1.5	μA
Input Bias Current			3.5	7.5	μA
Input Resistance		5.0	20		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	145	160	
Differential Distortion	$R_L \geq 100$ kΩ		80	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		Vpp
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage	$R_S \leq 50\Omega$			3.5	mV
Input Offset Current	$T_A = +125°C$		0.2	1.5	μA
	$T_A = -55°C$		1.0	3.0	μA
Input Bias Current	$T_A = -55°C$		6.5	15	μA
Input Resistance		0.9			kΩ
Input Voltage Range		3.5		5.2	V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5\,V \leq V_{CM} \leq +5.2\,V$	70	85		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	90		175	
Common Mode Output Voltage		5.5	7.0	7.75	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	6.8		Vpp
Supply Current	$T_A = -55°C$		10	15	mA
	$T_A = 125°C$		8.0	11	mA
Power Consumption	$T_A = -55°C$		120	180	mW
	$T_A = 125°C$		96	121	mW

TYPICAL PERFORMANCE CURVES

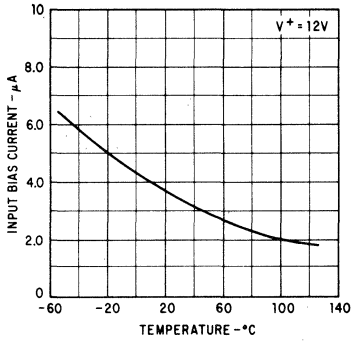
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

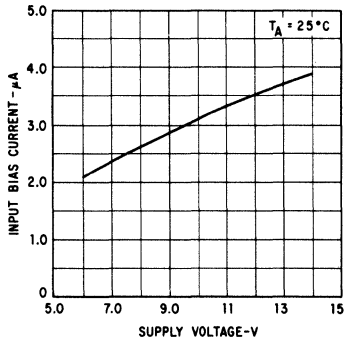


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

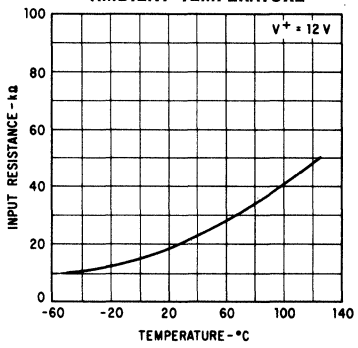


TYPICAL PERFORMANCE CURVES

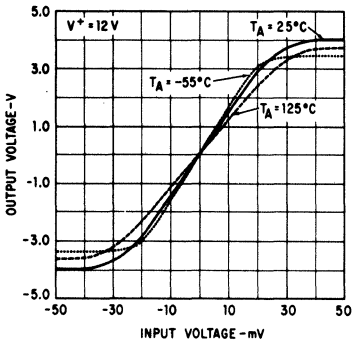
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



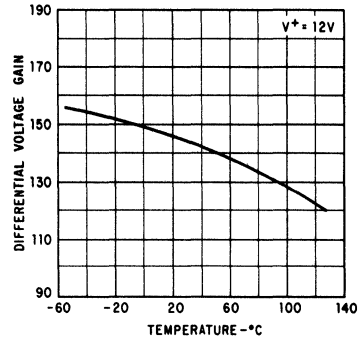
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



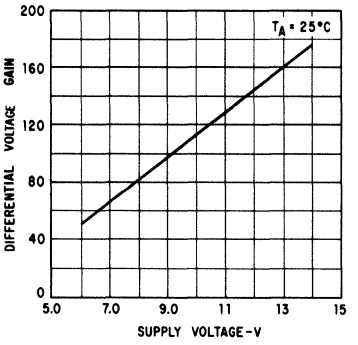
VOLTAGE TRANSFER CHARACTERISTICS



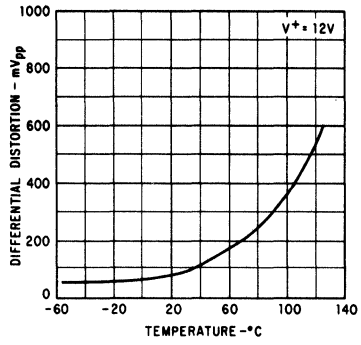
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



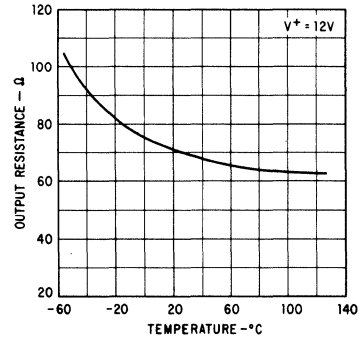
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



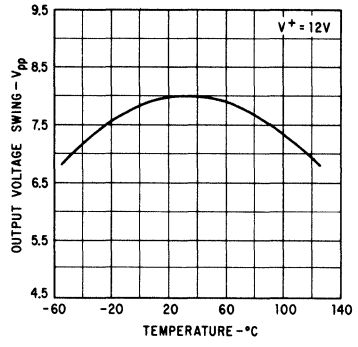
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



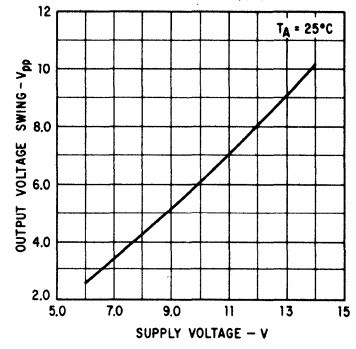
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



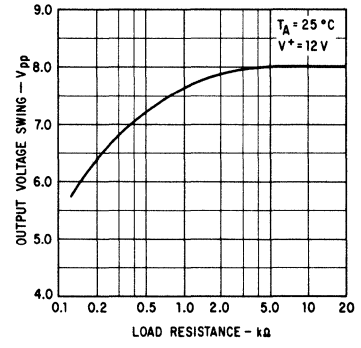
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



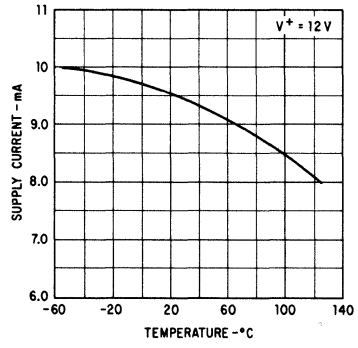
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



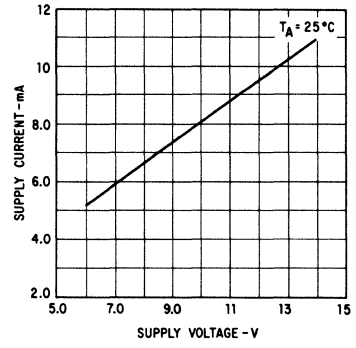
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

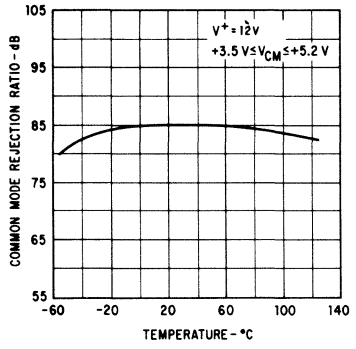


DEFINITION OF TERMS

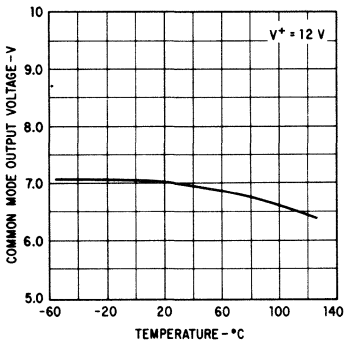
INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero differential output voltage.
INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero differential volts.
INPUT BIAS CURRENT—The average of the two input currents.
INPUT BIAS RESISTANCE—The resistance looking into either input terminal with the other grounded.
INPUT VOLTAGE RANGE—The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.
DIFFERENTIAL VOLTAGE GAIN—The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.
DIFFERENTIAL DISTORTION—The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.
BANDWIDTH—The frequency at which the differential voltage gain is 3 dB below its low frequency value.
OUTPUT RESISTANCE—The resistance seen looking into either output terminal with the output at differential null.
COMMON MODE OUTPUT VOLTAGE—The average voltage at the two output terminals referred to ground.
OUTPUT VOLTAGE SWING—The peak-to-peak output swing that can be obtained without clipping.
SUPPLY CURRENT—The current required from the power supply to operate the device with no load.
POWER CONSUMPTION—The DC power required to operate the amplifier with no load current.

TYPICAL PERFORMANCE CURVES

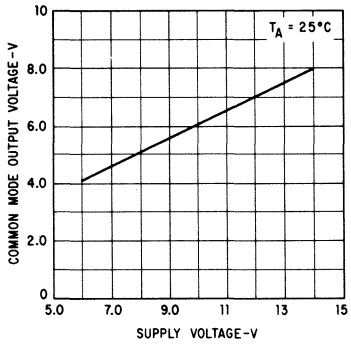
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

μA730C
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

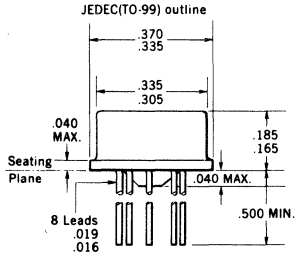
GENERAL DESCRIPTION – The μA730C is a differential amplifier constructed on a single silicon-chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

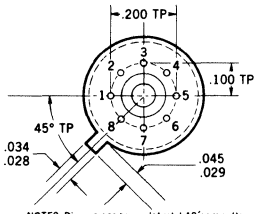
For full temperature range operation (−55°C to +125°C), see μA730 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

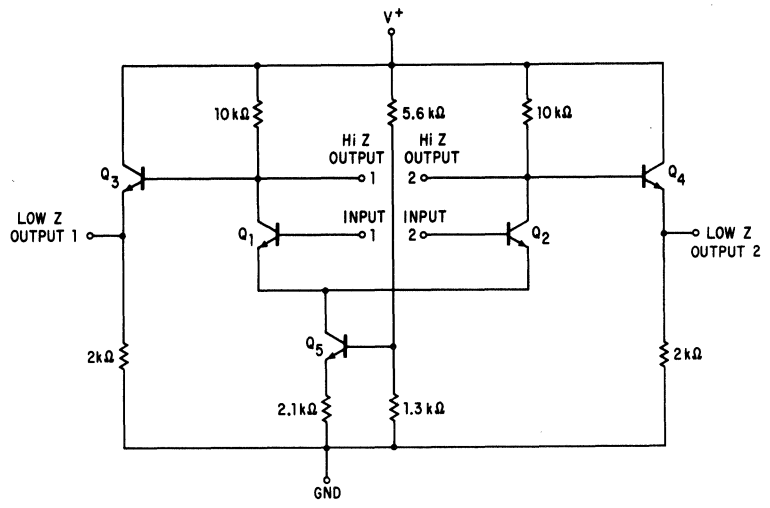




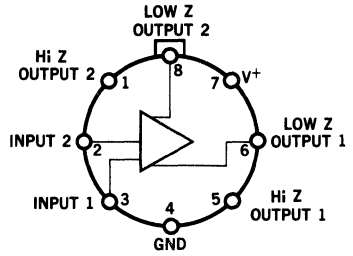
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B773039X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top View)



Note: Pin 4 connected to case

NOTES:
(1) Rating applies for ambient temperatures to +70°C.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
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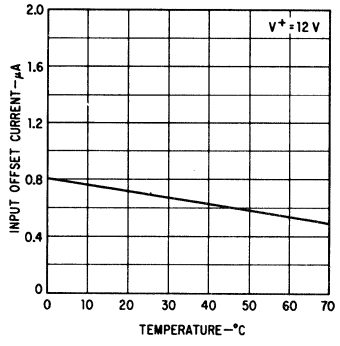
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V+ = 12.0$ V, and $V_{CM} = 3.5$ V unless otherwise specified)

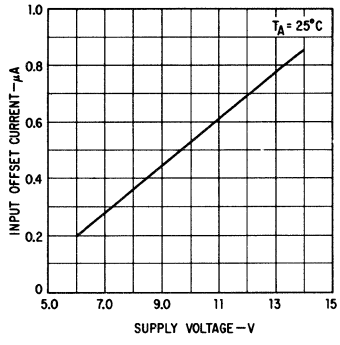
PARAMETER (See Definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	5.0	mV
Input Offset Current			0.7	3.0	μA
Input Bias Current			4.5	16.0	μA
Input Resistance		2.5	15		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	135	160	
Differential Distortion	$R_L \geq 100$ kΩ		85	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		Vpp
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\Omega$			7.5	mV
Input Offset Current	$T_A = +70°C$		0.5	3.0	μA
	$T_A = 0°C$		0.8	5.0	μA
Input Bias Current	$T_A = 0°C$		5.0	20	μA
Input Resistance		1.8			kΩ
Input Voltage Range		+3.5		+5.2	
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5\text{ V} \leq V_{CM} \leq +5.2\text{ V}$	60	80		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	80		190	
Common Mode Output Voltage		5.0	7.0	8.0	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	7.5		Vpp
Supply Current	$T_A = 0°C$		10	15	mA
	$T_A = +70°C$		8.8	13	mA
Power Consumption	$T_A = 0°C$		120	180	mW
	$T_A = +70°C$		106	156	mW

TYPICAL PERFORMANCE CURVES

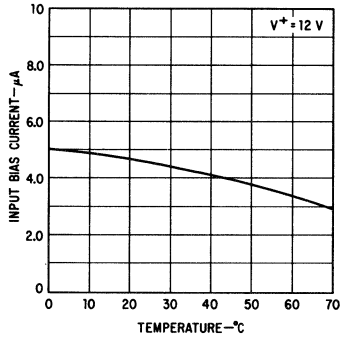
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

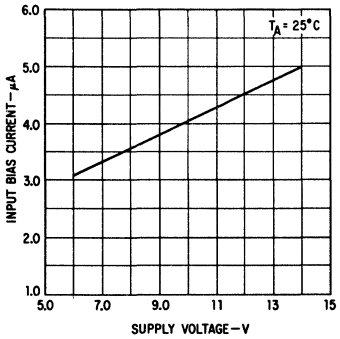


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

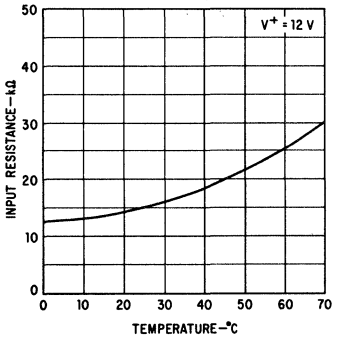


TYPICAL PERFORMANCE CURVES

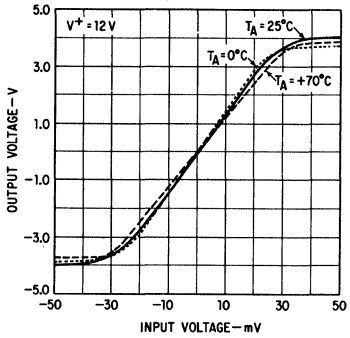
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



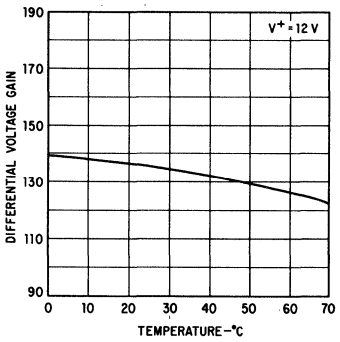
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



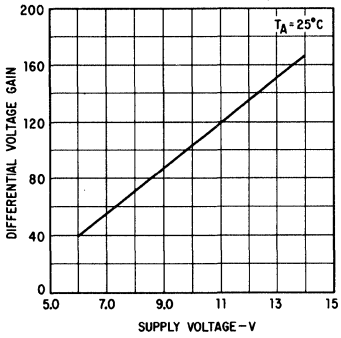
VOLTAGE TRANSFER CHARACTERISTICS



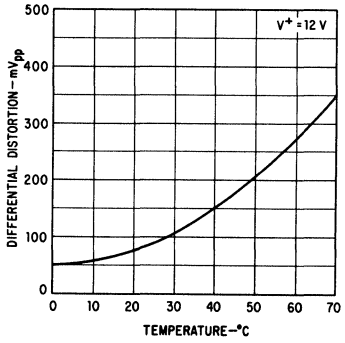
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



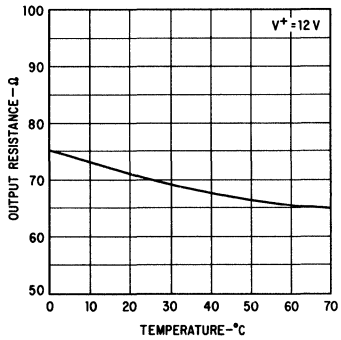
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



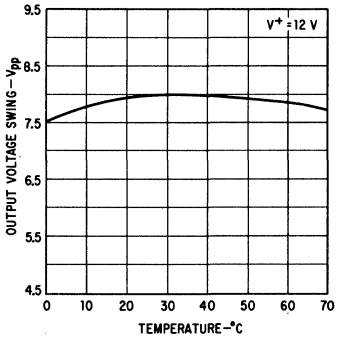
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



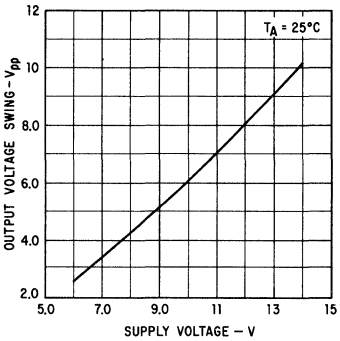
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



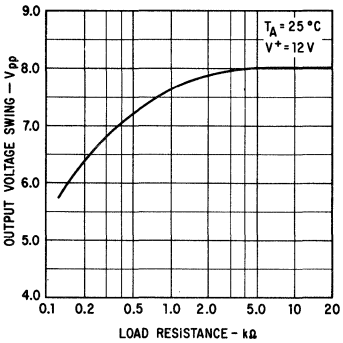
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



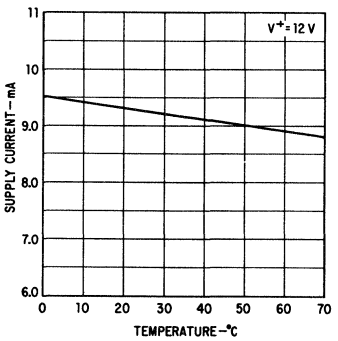
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



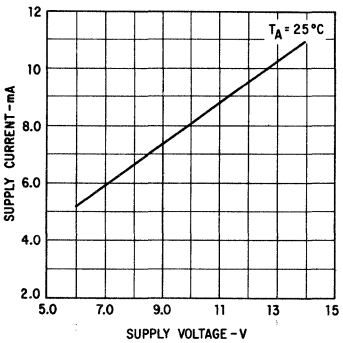
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

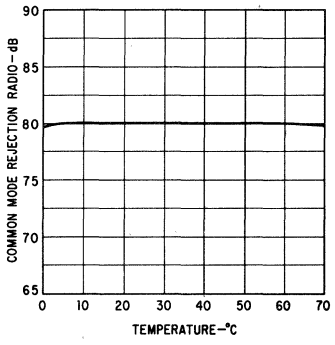


DEFINITION OF TERMS

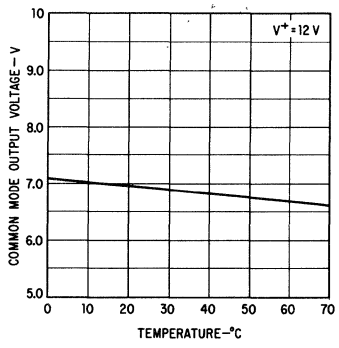
INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero differential output voltage.
INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero differential volts.
INPUT BIAS CURRENT—The average of the two input currents.
INPUT BIAS RESISTANCE—The resistance looking into either input terminal with the other grounded.
INPUT VOLTAGE RANGE—The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.
DIFFERENTIAL VOLTAGE GAIN—The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.
DIFFERENTIAL DISTORTION—The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.
BANDWIDTH—The frequency at which the differential voltage gain is 3 dB below its low frequency value.
OUTPUT RESISTANCE—The resistance seen looking into either output terminal with the output at differential null.
COMMON MODE OUTPUT VOLTAGE—The average voltage at the two output terminals referred to ground.
OUTPUT VOLTAGE SWING—The peak-to-peak output swing that can be obtained without clipping.
SUPPLY CURRENT—The current required from the power supply to operate the device with no load.
POWER CONSUMPTION—The DC power required to operate the amplifier with no load current.

TYPICAL PERFORMANCE CURVES

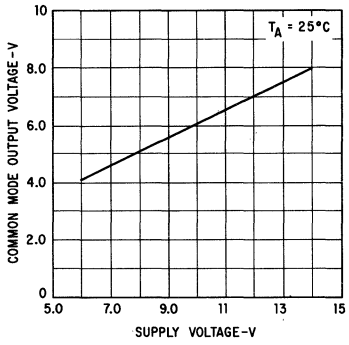
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



μA733

DIFFERENTIAL VIDEO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

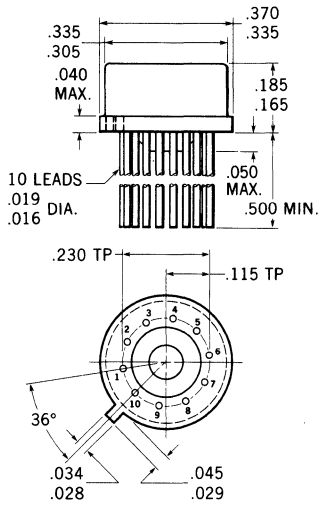
- **120 MHz BANDWIDTH**
- **250 kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100, AND 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

GENERAL DESCRIPTION — The μA733 is a monolithic two-stage differential input, differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high-speed thin film or plated wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation TO-100 (Note 1)	500 mW
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

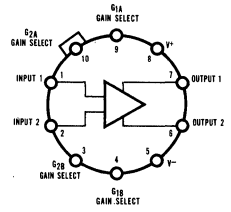
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



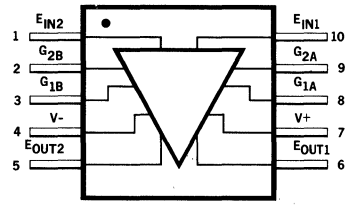
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5F7733312

CONNECTION DIAGRAMS
(TOP VIEW)

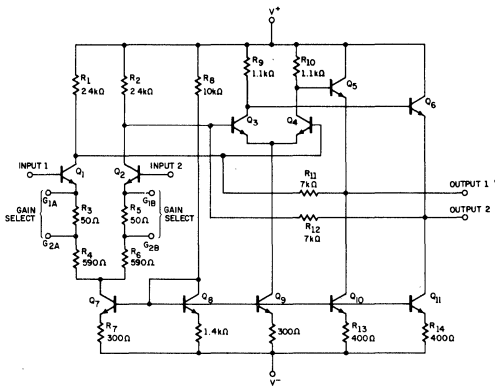


TO-100

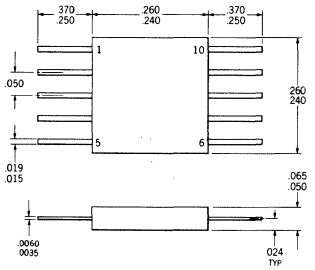


FLAT-PAK

SCHEMATIC DIAGRAM



FLAT PACKAGE



NOTES: All dimensions in inches

ORDER PART NO. U3F7733312

Notes on Page 2

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

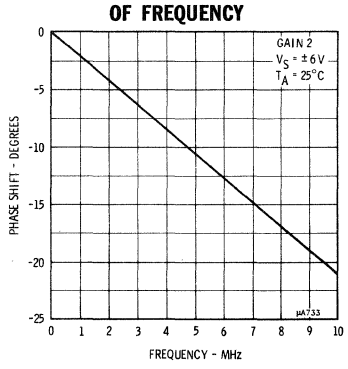
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	$R_S = 50\,\Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\,\Omega$, $V_{out} = 1$ Vpp				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\,\Omega$, $V_{out} = 1$ Vpp				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	$R_S = 50\,\Omega$, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA

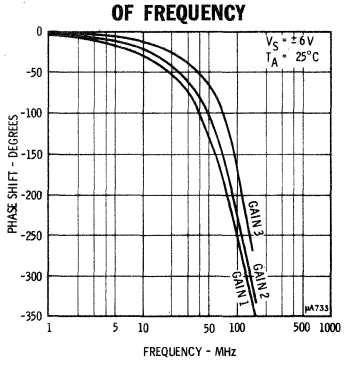
NOTES:
(1) For TO-100 rating applies for case temperature to 125°C; derate linearly at 6.5 mW/°C for ambient temperature above 75°C.
(2) Gain Select pins G_{1A} and G_{1B} connected together.
(3) Gain Select pins G_{2A} and G_{2B} connected together.
(4) All Gain Select pins open.

TYPICAL PERFORMANCE CURVES

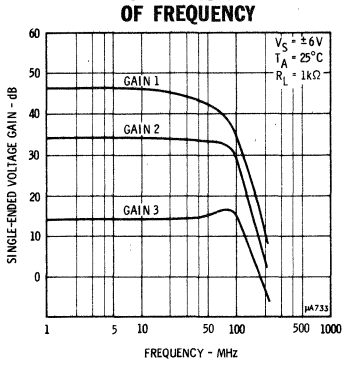
PHASE SHIFT AS A FUNCTION OF FREQUENCY



PHASE SHIFT AS A FUNCTION OF FREQUENCY

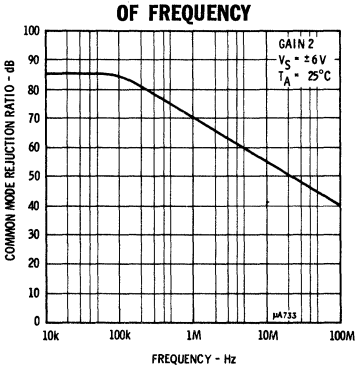


VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

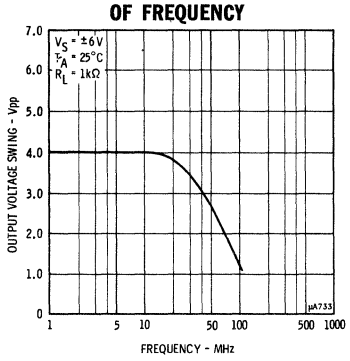


TYPICAL PERFORMANCE CURVES

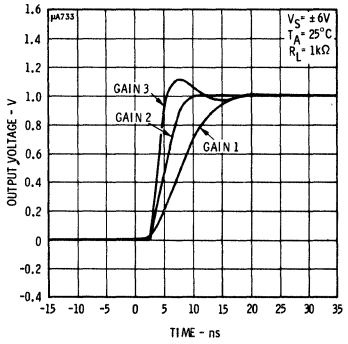
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



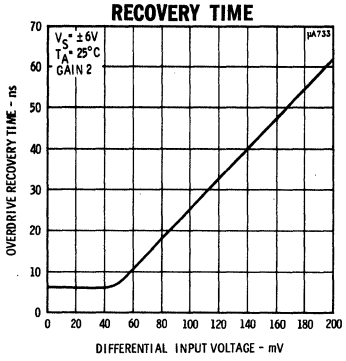
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



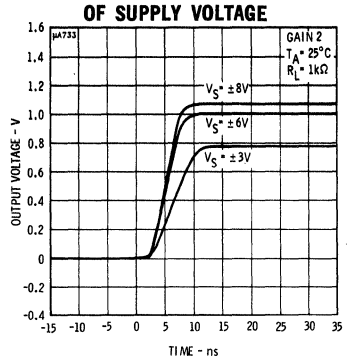
PULSE RESPONSE



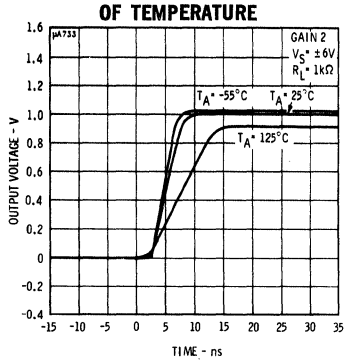
DIFFERENTIAL OVERDRIVE RECOVERY TIME



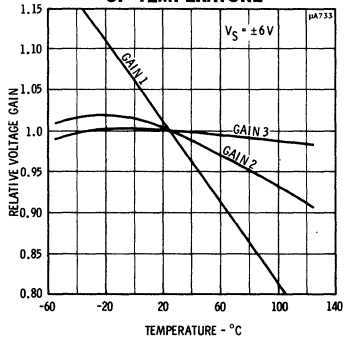
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



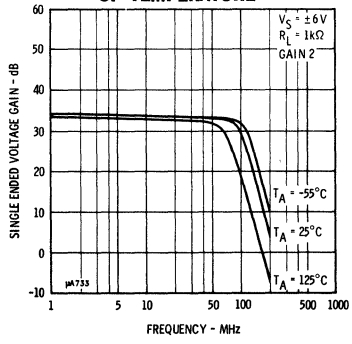
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



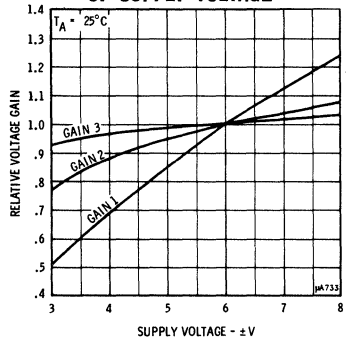
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



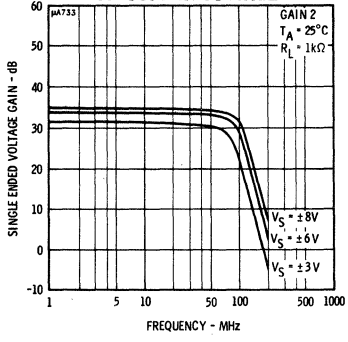
GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE



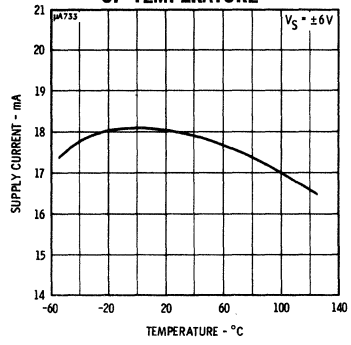
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



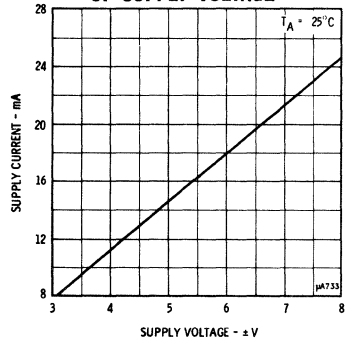
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH — The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE — The resistance seen looking into either input terminal with the other grounded.

INPUT OFFSET CURRENT — The difference between the currents into the two input terminals.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.

OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

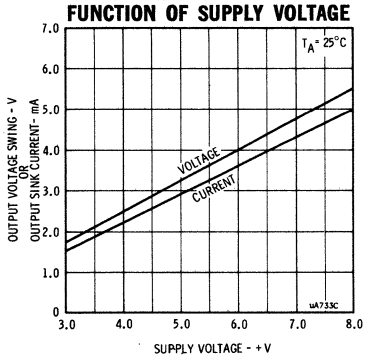
OUTPUT SINK CURRENT — The peak negative current available at either output of the amplifier.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal.

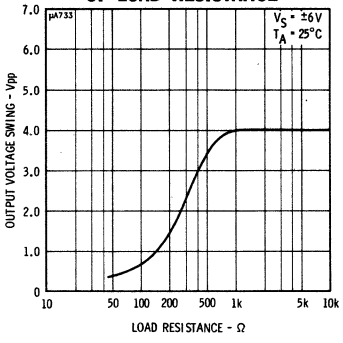
POWER SUPPLY CURRENT — The current required from the power supplies to operate the device with no load.

TYPICAL PERFORMANCE CURVES

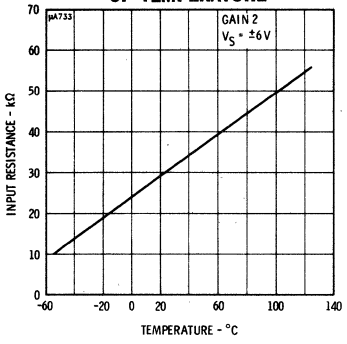
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



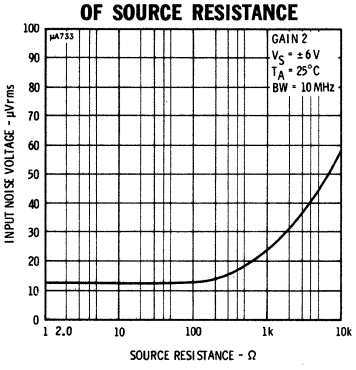
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



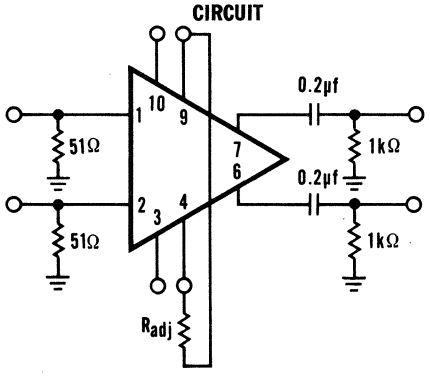
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



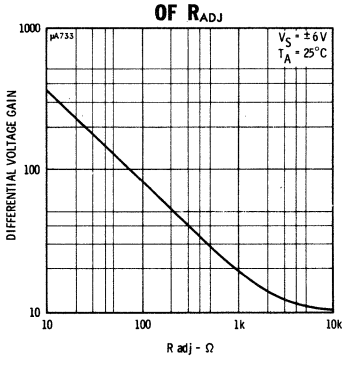
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



VOLTAGE GAIN ADJUST CIRCUIT



VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}



μA733C
DIFFERENTIAL VIDEO AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

- **120 MHz BANDWIDTH**
- **250 kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100, AND 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

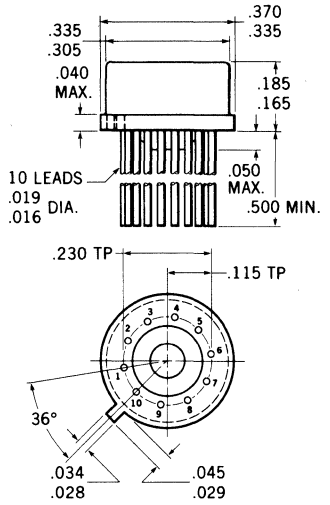
GENERAL DESCRIPTION — The μA733C is a monolithic two-stage differential input, differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high-speed thin film or plated wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

For full temperature range performance (−55°C to 125°C), see μA733 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

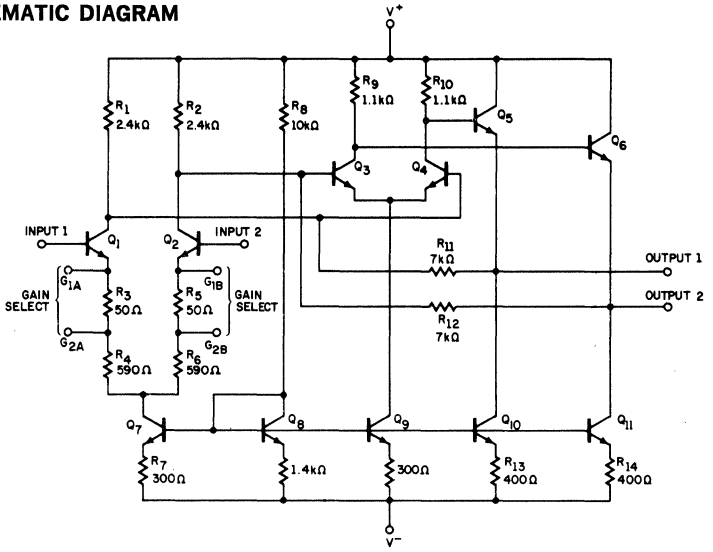
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



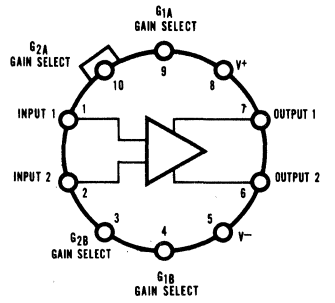
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5F7733393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



Note: Pin 5 connected to case.

Notes on Page 2

*Planar is a patented Fairchild process.

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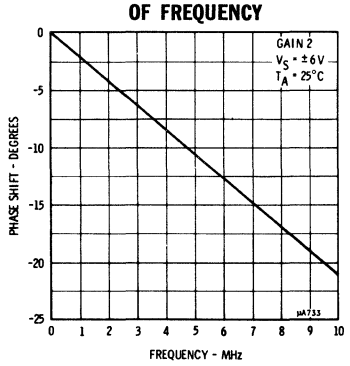
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth	$R_S = 50\ \Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\ \Omega$, $V_{out} =$ 1 Vpp				
Gain 1			10.5		ns
Gain 2			4.5	12	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\ \Omega$, $V_{out} =$ 1 Vpp				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		10	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA

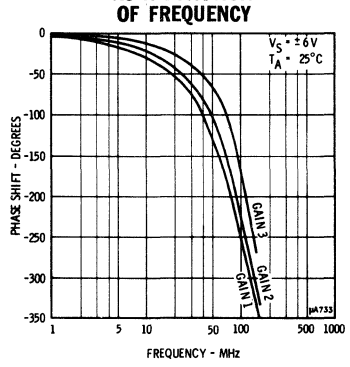
NOTES:
(1) Rating applies for ambient temperatures to 70°C.
(2) Gain Select pins G_{1A} and G_{1B} connected together.
(3) Gain Select pins G_{2A} and G_{2B} connected together.
(4) All Gain Select pins open.

TYPICAL PERFORMANCE CURVES

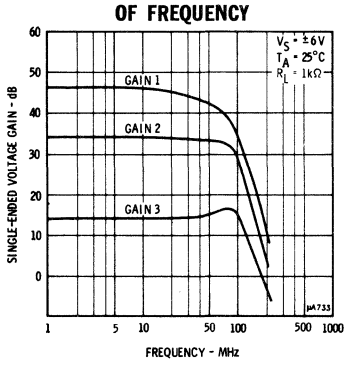
PHASE SHIFT AS A FUNCTION OF FREQUENCY



PHASE SHIFT AS A FUNCTION OF FREQUENCY

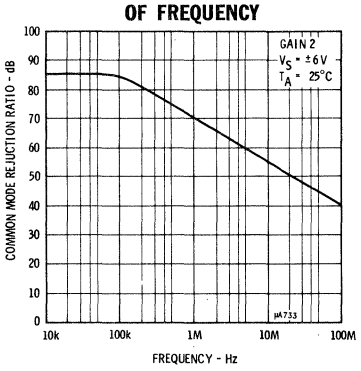


VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

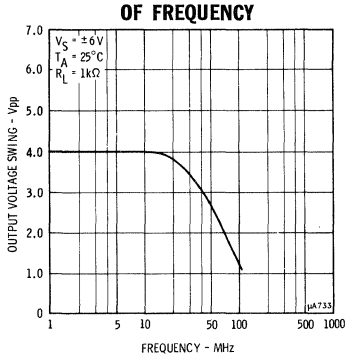


TYPICAL PERFORMANCE CURVES

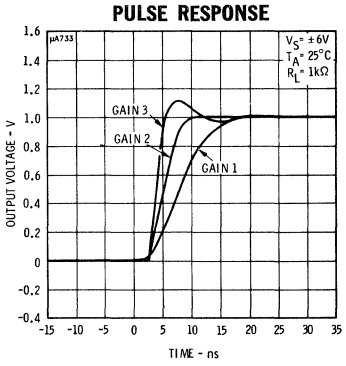
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



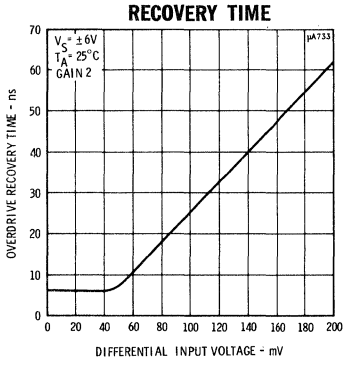
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



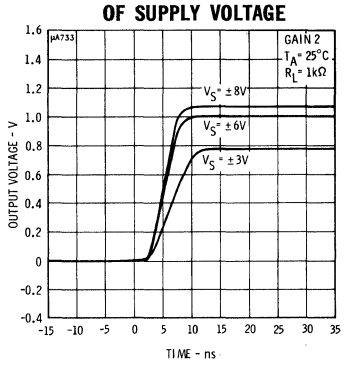
PULSE RESPONSE



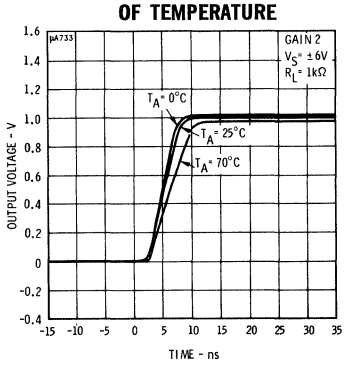
DIFFERENTIAL OVERDRIVE RECOVERY TIME



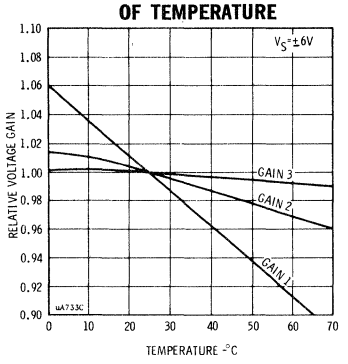
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



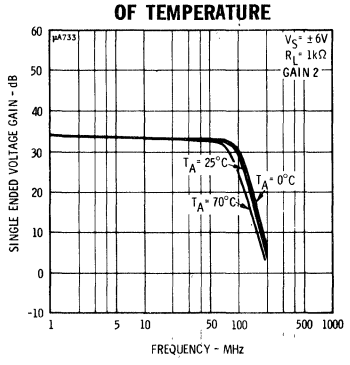
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



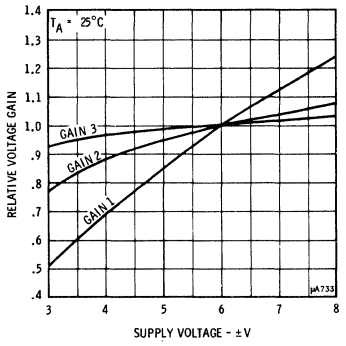
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



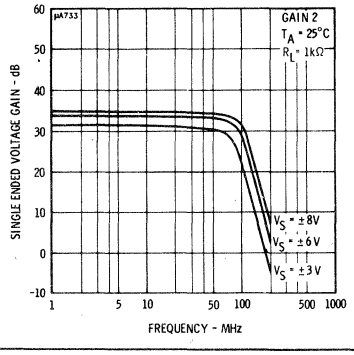
GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE



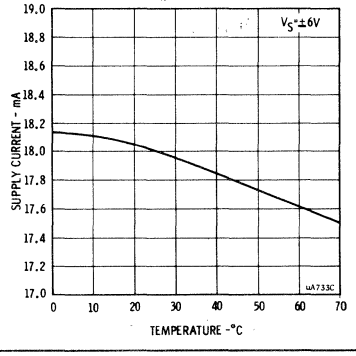
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



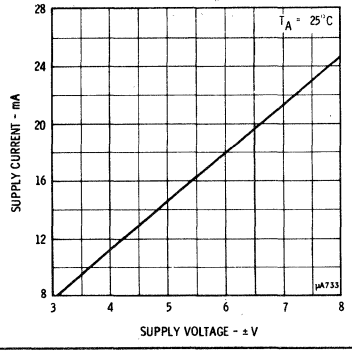
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH — The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE — The resistance seen looking into either input terminal with the other grounded.

INPUT OFFSET CURRENT — The difference between the currents into the two input terminals.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.

OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

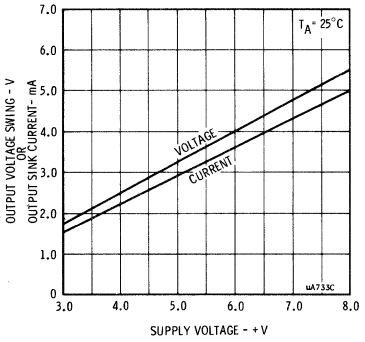
OUTPUT SINK CURRENT — The peak negative current available at either output of the amplifier.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal.

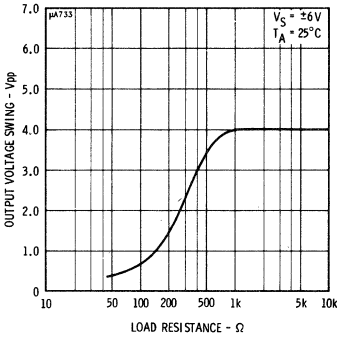
POWER SUPPLY CURRENT — The current required from the power supplies to operate the device with no load.

TYPICAL PERFORMANCE CURVES

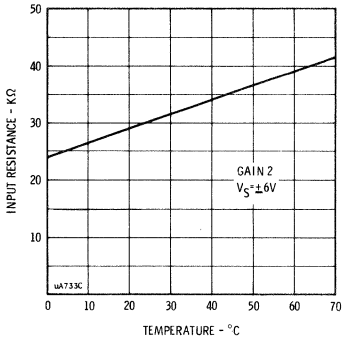
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



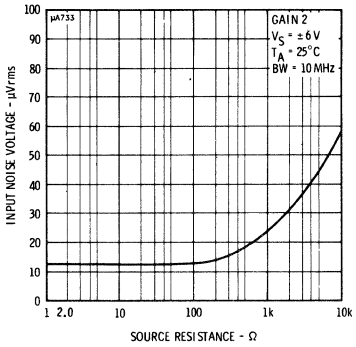
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



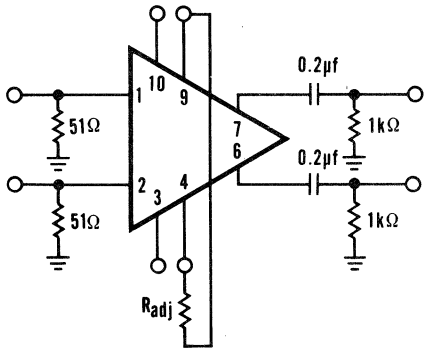
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



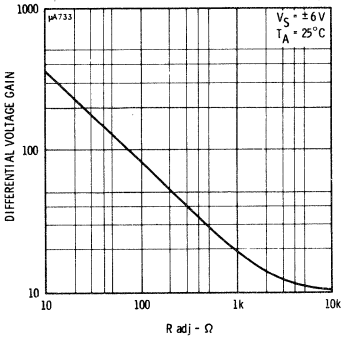
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



VOLTAGE GAIN ADJUST CIRCUIT



VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}



μA737E

COLOR TV CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA737E is a monolithic silicon integrated circuit which demodulates the chroma subcarrier information contained in a color television video signal and provides color-difference signals at the outputs.

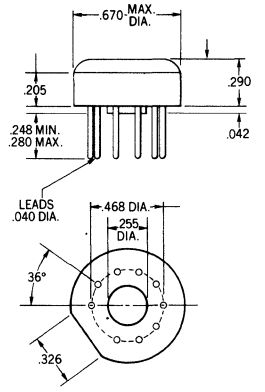
FEATURES

- **DOUBLY BALANCED DEMODULATION**
- **INTERNAL COLOR-DIFFERENCE MATRIX FOR NTSC COLOR TV**
- **10 VOLT PEAK-TO-PEAK E_B - E_Y OUTPUT**
- **PLUGS INTO A STANDARD 9-PIN MINIATURE TUBE SOCKET OR SOLDERS INTO A PRINTED BOARD**

ABSOLUTE MAXIMUM RATINGS

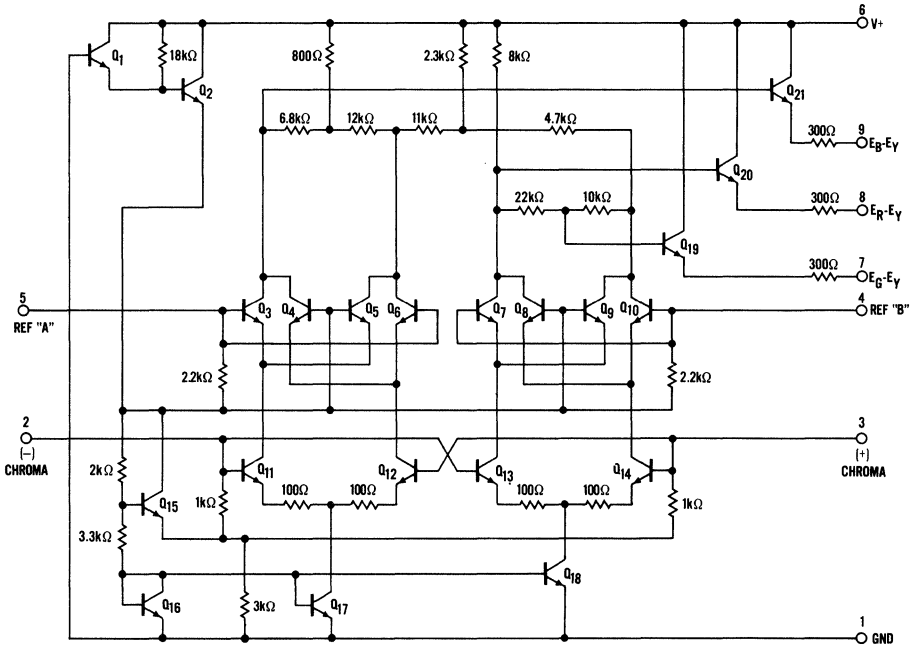
Supply Voltage	+28 V
Minimum Load Resistance	3 kΩ
Peak-to-Peak Reference Input Voltage	5 V
Peak-to-Peak Chroma Input Voltage	5 V
Internal Power Dissipation	450 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	+260°C

PHYSICAL DIMENSIONS

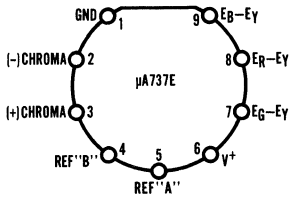


ORDER PART NO. U8F7737394

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



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FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 24$ V, Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$e_C = 0$, $R_L = 1\ M\Omega$	4.5	8.0	11.5	mA
	$e_C = 0$, $R_L = 1\ M\Omega$, $T_A = 70°C$		8.0	12.0	mA
	$e_C = 0$	16.5	21	25.5	mA
	$e_C = 0$, $T_A = 70°C$		21		mA
Internal Power Dissipation	$e_C = 0$		320	410	mW
	$e_C = 0$, $T_A = 70°C$		320	420	mW
DC Voltage at any Output Terminal	$e_C = 0$	12.5	14.7	16.5	V
	$e_C = 0$, $T_A = 70°C$	12.0	14.3		V
Absolute Value of DC Difference Voltage between any Two Outputs	$e_C = 0$		0.2	1.0	V
DC Voltage at either Reference Terminal	$e_A = e_B = e_C = 0$		5.8		V
DC Voltage at either Chroma Terminal	$e_C = 0$		3.2		V
Reference Input Resistance	$e_C = 0$		1.7		kΩ
Reference Input Capacitance	$e_C = 0$		6.0		pF
Chroma Input Resistance			0.8		kΩ
Chroma Input Capacitance			5.0		pF
Peak-to-Peak Chroma Input Voltage	$E_B - E_Y = 5$Vp-p		0.4	0.7	V
Peak-to-Peak $E_R - E_Y$ Output Voltage	$E_B - E_Y = 5$Vp-p	3.5	3.8	4.2	V
Peak-to-Peak $E_G - E_Y$ Output Voltage	$E_B - E_Y = 5$Vp-p	0.75	1.0	1.25	V
Maximum Peak-to-Peak $E_B - E_Y$ Output Voltage	$e_C = 1.5$Vp-p	8.0	10		V
$E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p		3		Degrees
$E_R - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p		109		Degrees
$E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p		259		Degrees
$E_R - E_Y$ Demodulation Angle relative to $E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p	101	106	111	Degrees
$E_B - E_Y$ Demodulation Angle relative to $E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p	96	104	112	Degrees
Highest Peak-to-Peak Demodulator AC Unbalance Voltage at any Output Terminal	$e_C = 0$		0.3	0.8	V

DEFINITIONS

Color-Difference Demodulation Angle — A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

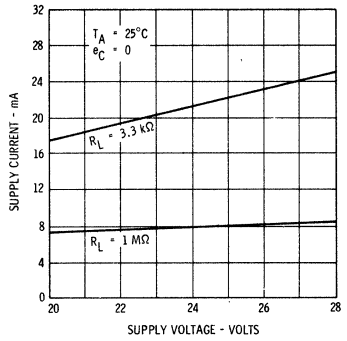
(+) Chroma Input — A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(—) Chroma Input — A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (—) Chroma input.

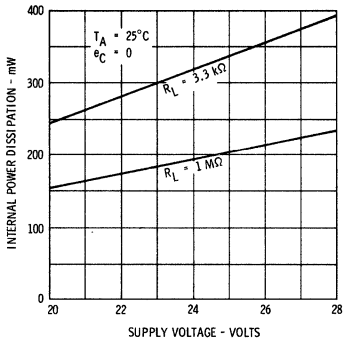
TYPICAL ELECTRICAL CHARACTERISTICS

(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

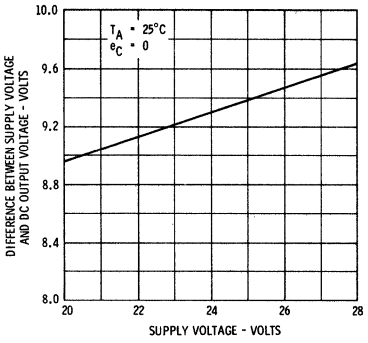
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



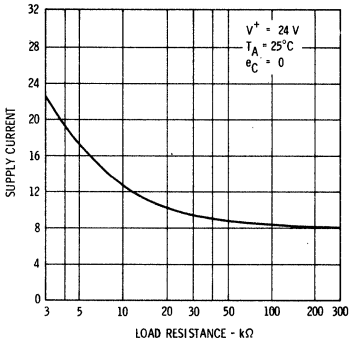
INTERNAL POWER DISSIPATION VERSUS SUPPLY VOLTAGE



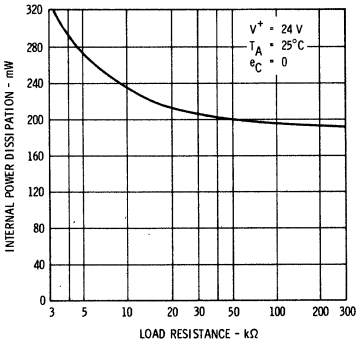
DIFFERENCE BETWEEN THE SUPPLY VOLTAGE AND THE DC VOLTAGE AT ANY OUTPUT VERSUS SUPPLY VOLTAGE



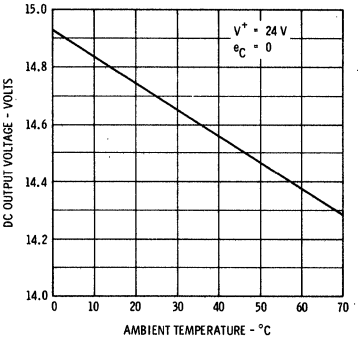
SUPPLY CURRENT VERSUS LOAD RESISTANCE



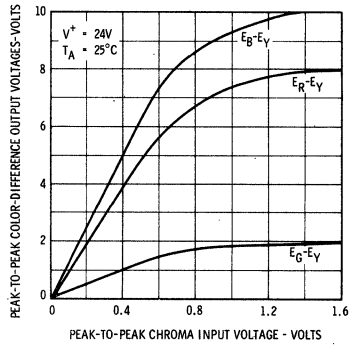
INTERNAL POWER DISSIPATION VERSUS LOAD RESISTANCE



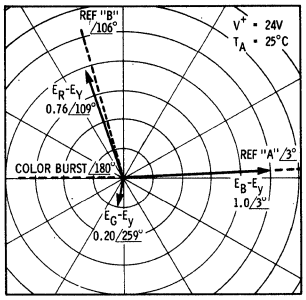
DC VOLTAGE AT ANY OUTPUT VERSUS AMBIENT TEMPERATURE



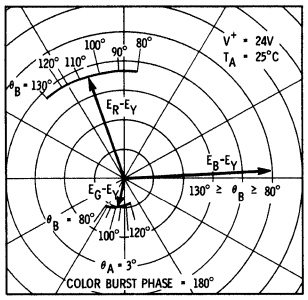
DEMODULATION LINEARITY



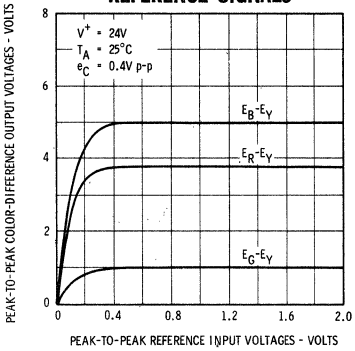
DEMODULATION ANGLES AND RELATIVE GAINS



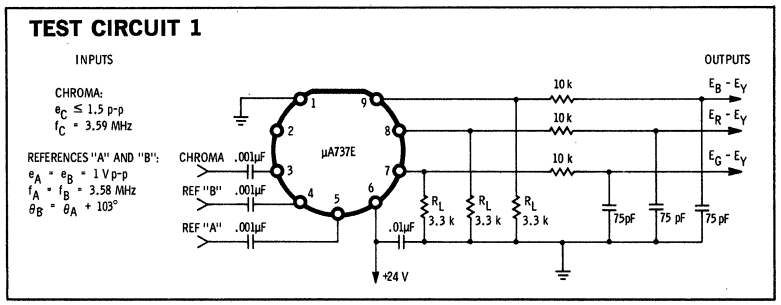
DEMODULATION SENSITIVITY TO RELATIVE PHASING OF REFERENCE SIGNALS



DEMODULATION SENSITIVITY TO AMPLITUDE OF REFERENCE SIGNALS



TEST CIRCUIT 1



μA739C

DUAL LOW-NOISE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA739C consists of two identical operational amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These low-noise, high-gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltage and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.

FEATURES

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW NOISE FIGURE, 2.0 dB**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

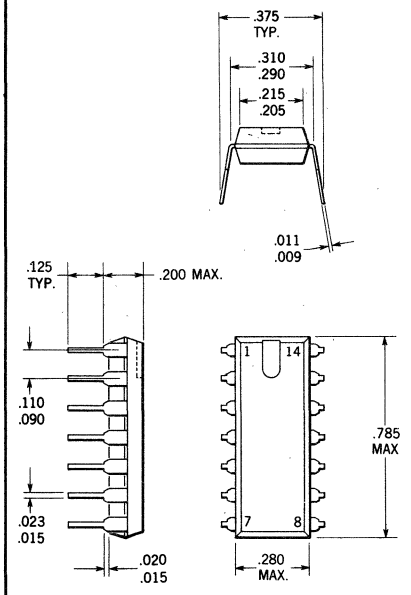
TYPICAL APPLICATIONS

- **DUAL OPERATIONAL AMPLIFIER**
- **PHONO AND TAPE STEREO PREAMPLIFIER**
- **TV REMOTE CONTROL RECEIVER**
- **DUAL COMPARATOR**
- **SENSE AMPLIFIER**
- **OSCILLATOR**
- **ACTIVE FILTER**

ABSOLUTE MAXIMUM RATINGS

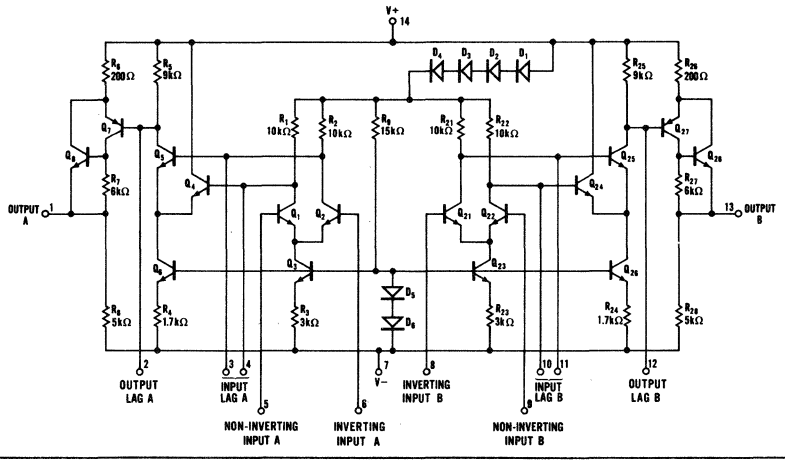
Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	260°C
Output Short-Circuit Duration, $T_A = 25°C$ (Note 3)	30 seconds

TYPICAL DUAL IN-LINE PACKAGE

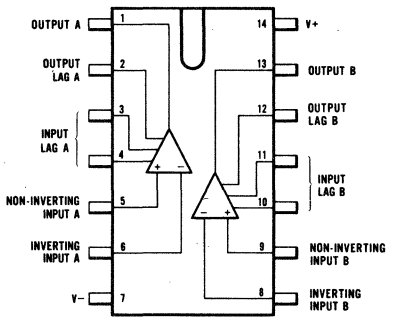


ORDER PART NO. U6E7739393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



Notes on page 2

*Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $R_L = 50$ kΩ to Pin 7, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300	2000	nA
Input Resistance		37	150		kΩ
Large-Signal Voltage Gain	$V_{OUT} = \pm 5.0$ V	6500	20,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Input Voltage Range		±10	±11		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		50		μV/V
Power Consumption	$V_{OUT} = 0$		270	420	mW
Supply Current	$V_{OUT} = 0$		9.0	14	mA
Broadband Noise Figure	$R_S = 10$ kΩ, BW = 10 Hz to 10 kHz		2.0		dB
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.3		μs
Slew Rate (unity gain) (See Figure 2)	$C_1 = 0.1\ \mu$F, $R_1 = 4.7\ \Omega$		1.0		V/μs
Channel Separation (See Figure 3)	$R_S \leq 10$ kΩ, f = 10 kHz		140		dB
The following specifications apply for $V_S = \pm 4.0$ V, $T_A = 25°C$					
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300		nA
Supply Current	$V_{OUT} = 0$		2.5		mA
Power Consumption	$V_{OUT} = 0$		20		mW
Large-Signal Voltage Gain	$V_{OUT} = \pm 1.0$ V	2500	15,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

PULSE RESPONSE WAVEFORMS

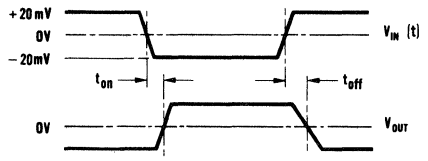


Figure 1

FREQUENCY RESPONSE TEST CIRCUIT

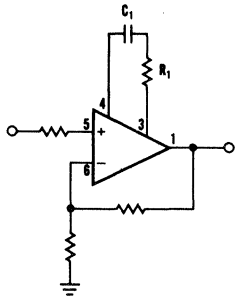


Figure 2

CHANNEL SEPARATION TEST CIRCUIT

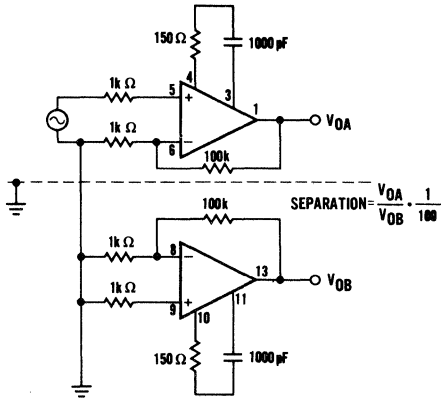


Figure 3

NOTES:

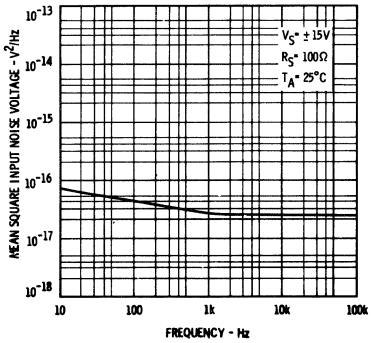
(1) Rating applies at ambient temperature below 60°C. Derate at 7.7 mw/°C above 60°C.

(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

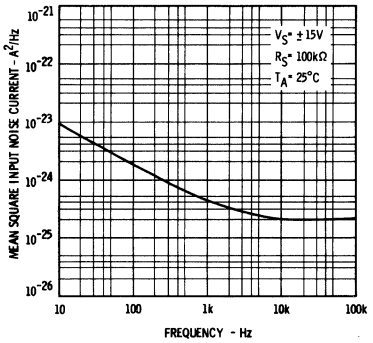
(3) Short circuit may be to ground or either supply.

TYPICAL PERFORMANCE CURVES

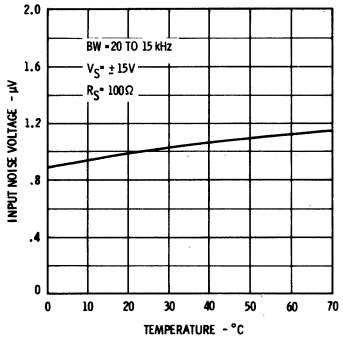
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



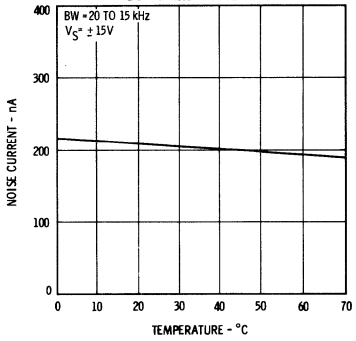
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



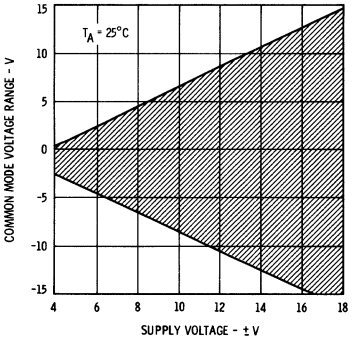
WIDE BAND INPUT NOISE VOLTAGE AS A FUNCTION OF TEMPERATURE



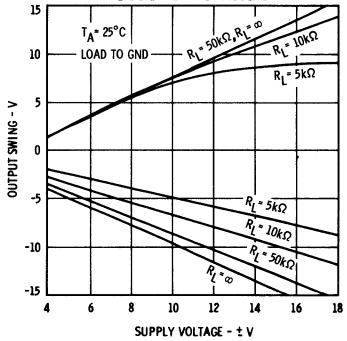
WIDE BAND INPUT NOISE CURRENT AS A FUNCTION OF TEMPERATURE



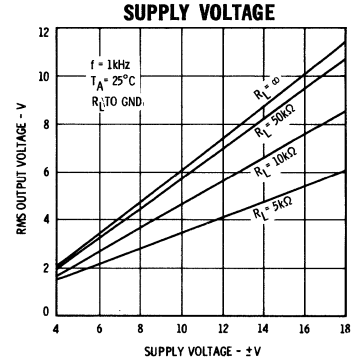
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



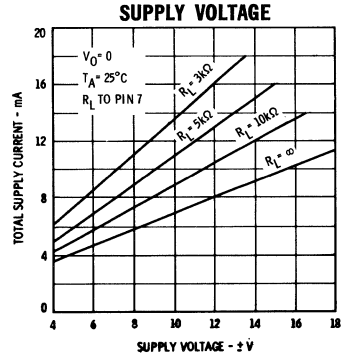
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



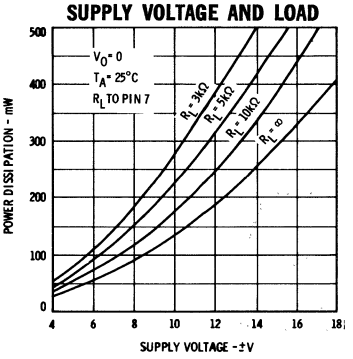
OUTPUT CAPABILITY AS A FUNCTION OF SUPPLY VOLTAGE



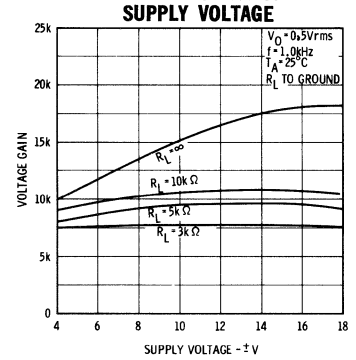
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



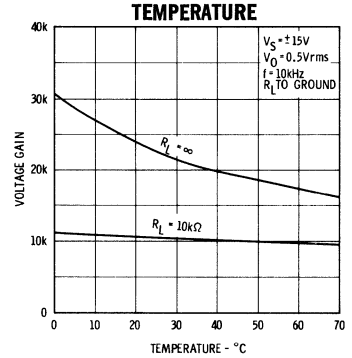
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



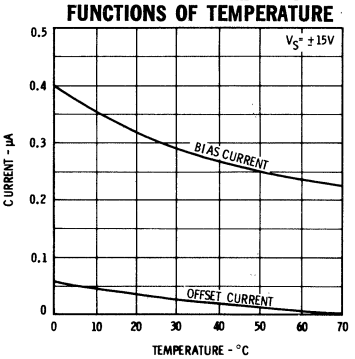
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

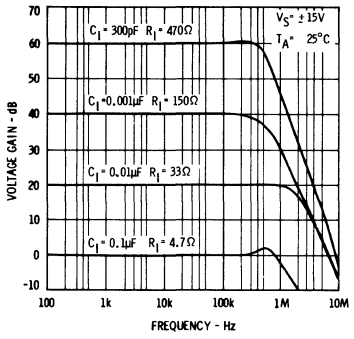


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

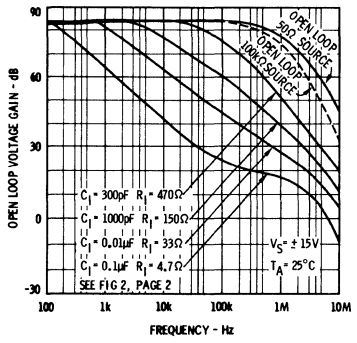


TYPICAL PERFORMANCE CURVES

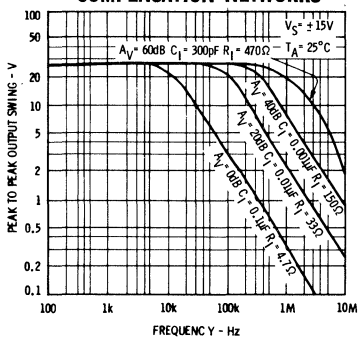
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



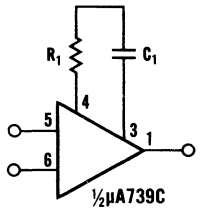
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



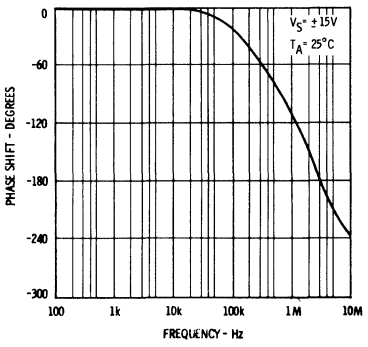
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



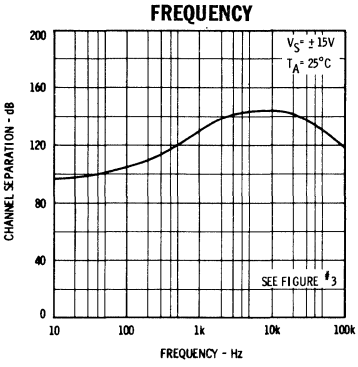
FREQUENCY COMPENSATION NETWORK



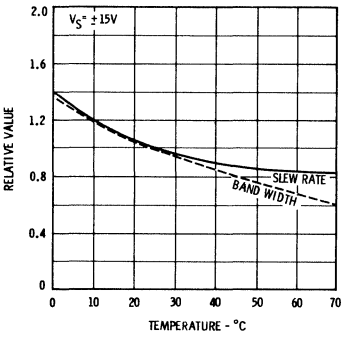
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

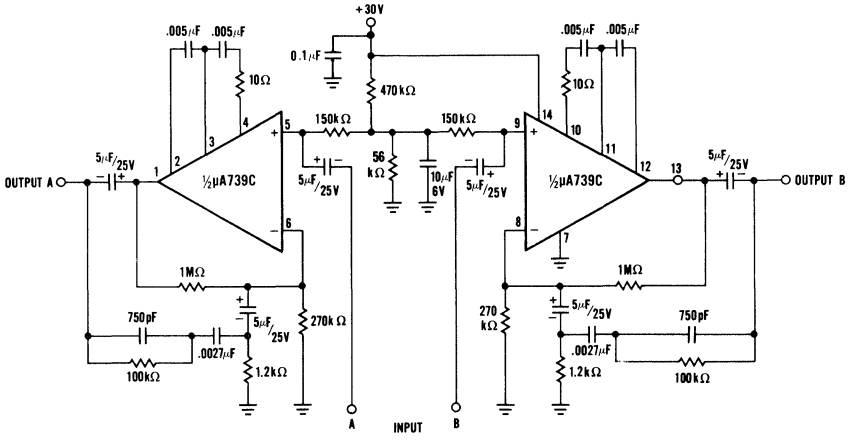


CHANGE OF A.C. CHARACTERISTICS WITH TEMPERATURE



TYPICAL APPLICATION

STEREO PHONO PREAMPLIFIER—RIAA EQUALIZED



TYPICAL PERFORMANCE

Gain 40 dB at 1 kHz, RIAA equalized
Input overload point, 80 mV rms
Noise level, 2μV referred to input
Signal to noise ratio, 74 dB below 10 mV
Channel separation @ 1 kHz, 80 dB

μA741

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

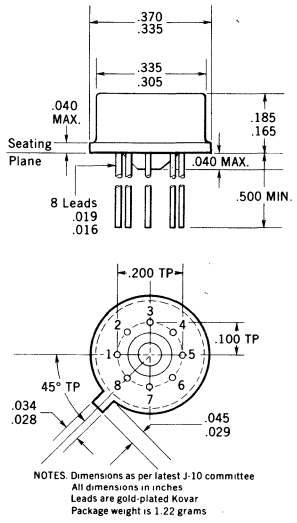
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA741 is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications.

PHYSICAL DIMENSIONS

in accordance with
JEDEC (TO-99) outline



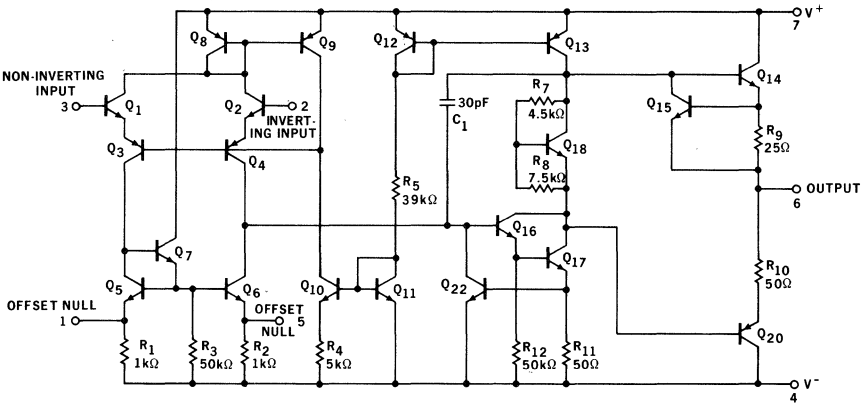
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7741312

ABSOLUTE MAXIMUM RATINGS

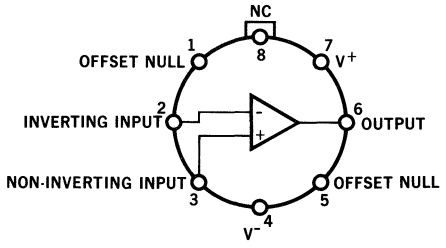
Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(TOP VIEW)



NOTE: PIN 4 CONNECTED TO CASE

NOTES:

(1) Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

*Planar is a patented Fairchild process.

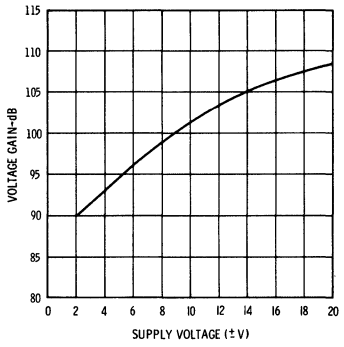
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

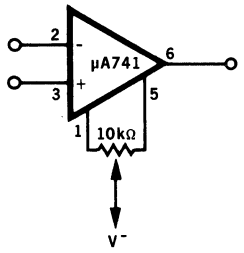
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2$kΩ, $V_{out} = \pm 10$ V	50,000	200,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Input Offset Current				500	nA
Input Bias Current				1.5	μA
Large-Signal Voltage Gain	$R_L \geq 2$kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

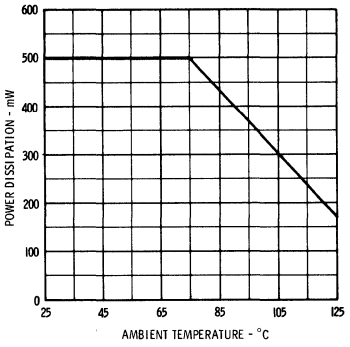
OPEN LOOP VOLTAGE GAIN



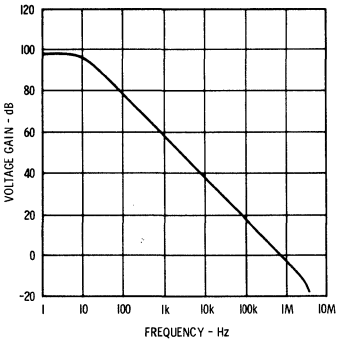
VOLTAGE OFFSET NULL CIRCUIT



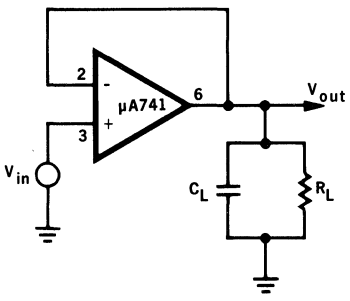
ABSOLUTE MAXIMUM POWER DISSIPATION



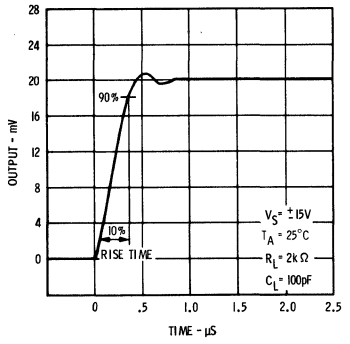
OPEN LOOP FREQUENCY RESPONSE



TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



μA741C

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

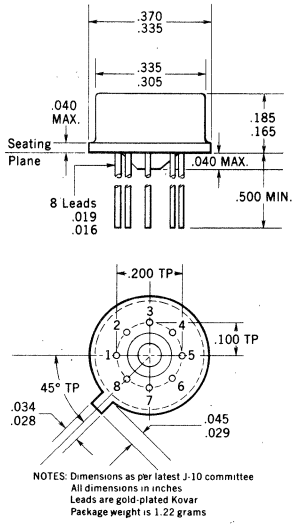
GENERAL DESCRIPTION — The μA741C is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741C ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA741C is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For full temperature range operation (−55°C to +125°C) see μA741 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Storage Temperature Range TO-99	−65°C to +150°C
Dual-In-Line	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 sec) TO-99	300°C
(Soldering, 10 sec) Dual-In-Line	260°C
Output Short-Circuit Duration (Note 2)	Indefinite

PHYSICAL DIMENSIONS

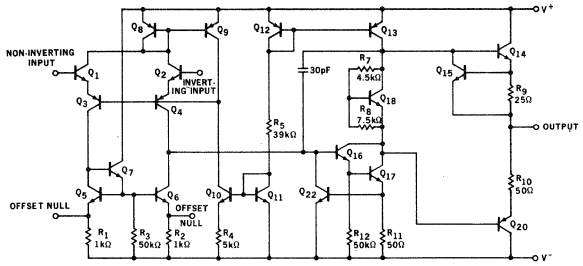
in accordance with JEDEC (TO-99) outline



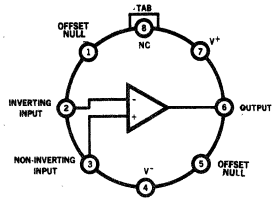
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7741393

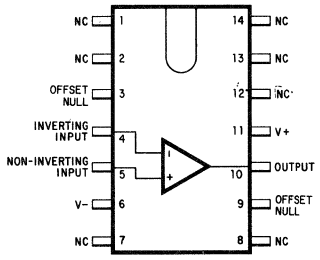
SCHEMATIC DIAGRAM



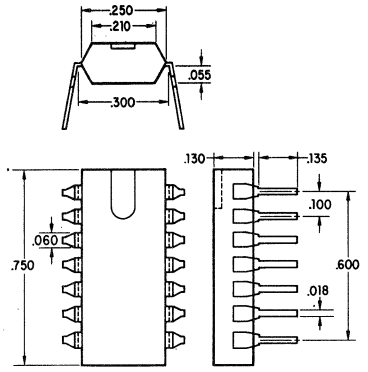
CONNECTION DIAGRAMS



NOTE: Pin 4 connected to case.



TYPICAL DUAL IN-LINE PACKAGE



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

ORDER PART NO. U6E7741393

*Planar is a patented Fairchild process.

NOTES:

(1) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

(2) Short circuit may be to ground or either supply.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

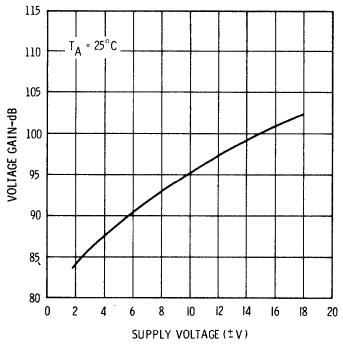
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

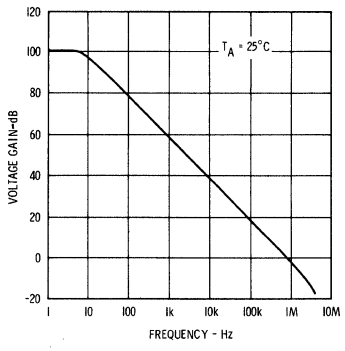
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20,000	100,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ				
	$C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES

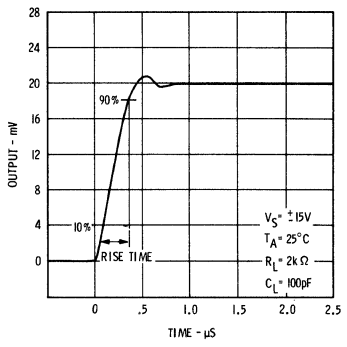
OPEN LOOP VOLTAGE GAIN



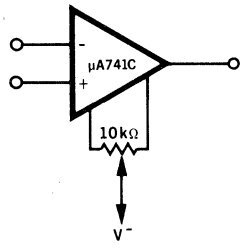
OPEN LOOP FREQUENCY RESPONSE



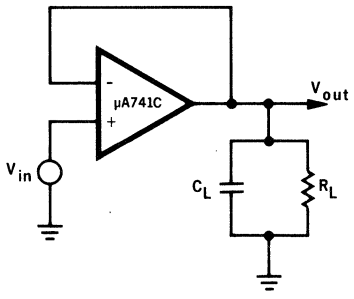
TRANSIENT RESPONSE



VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



μA751C

DIFFERENTIAL VIDEO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

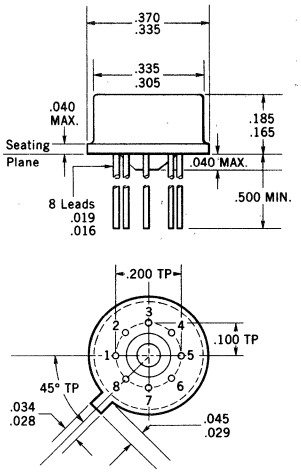
- **VOLTAGE GAIN 600**
- **200Ω INPUT LINE TERMINATION**
- **10 ns TYPICAL PROPAGATION DELAY**
- **NO FREQUENCY COMPENSATION REQUIRED**

GENERAL DESCRIPTION — The μA751C is a monolithic two-stage differential input differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series feedback is used for high gain and excellent gain stability. Internal sense line termination minimizes line reflections and eliminates the need for external termination components. External frequency compensation is not required. The device is particularly useful as a read amplifier in high-speed thin film memories. Other applications include general purpose video and pulse amplifiers where high gain and excellent gain stability are required. For applications where lower gain is required and where input termination is not desirable, see the μA733 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±2 V
Common Mode Input Voltage (Note 1)	±1 V
Output Current	7.5 mA
Internal Power Dissipation (Note 2)	250 mW
Operating Temperature Range	−0° to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 second time limit)	300°C

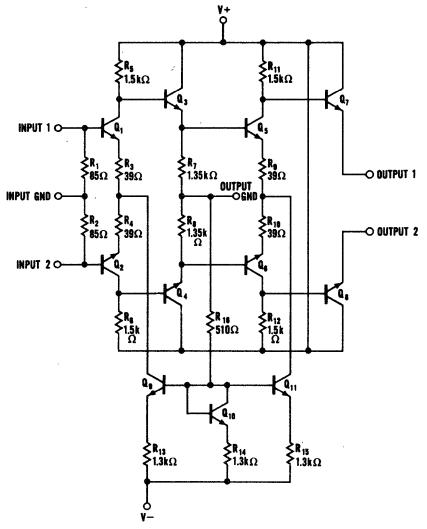
PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-99) outline



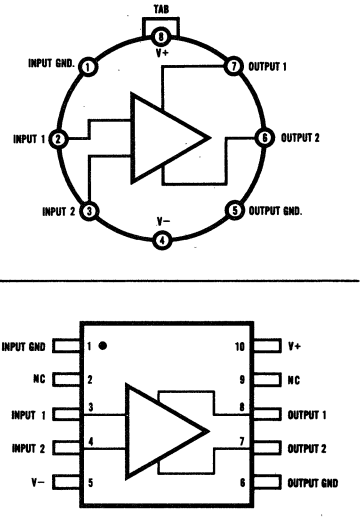
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7751393

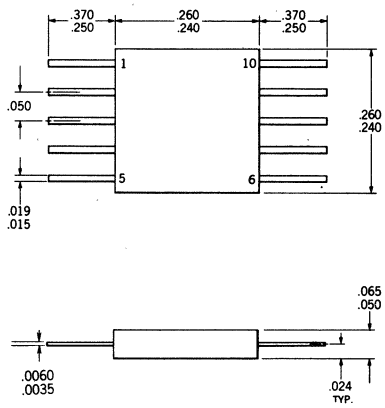
SCHEMATIC DIAGRAM



CONNECTION DIAGRAMS
(TOP VIEW)



PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



ORDER PART NO. U3H7751393

*Planar is a patented Fairchild process.

NOTES:
(1) Input voltage limited due to internal resistor between inputs and ground.
(2) Rating applies for ambient temperatures to 70°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

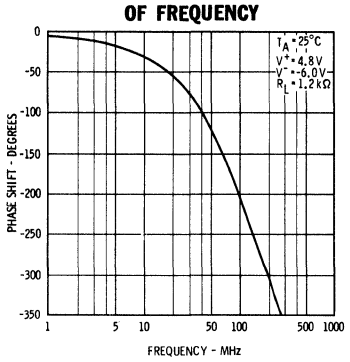
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +4.8$ V, $V^- = -6.0$ V unless otherwise specified)

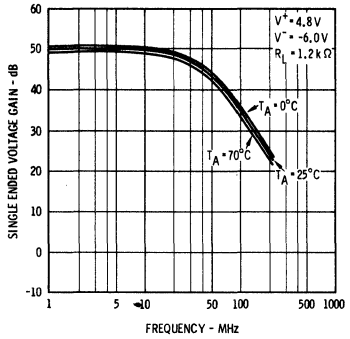
PARAMETER (see definitions, page 4)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain		375	600	825	
Bandwidth			30		MHz
Risetime	$V_{IN} = 1.0$ mV		12	25	ns
Propagation Delay	$V_{IN} = 1.0$ mV		10	20	ns
Differential Input Resistance		140	180	220	Ω
Input Capacitance			2.0		pF
Output Noise Voltage	BW = 20 Hz to 30 MHz		7.5		mVrms
Common Mode Rejection Ratio	$V_{CM} = 20$ mV		46		dB
Supply Voltage Rejection Ratio			60		dB
Output Offset Voltage			0.5	1.5	V
Output Common Mode Voltage		0.9	1.8	3.5	V
Output Voltage Swing			1.2		V_{pp}
Output Resistance			50		Ω
Positive Power Supply Current			11	14	mA
Negative Power Supply Current			9.0	12	mA

TYPICAL PERFORMANCE CURVES

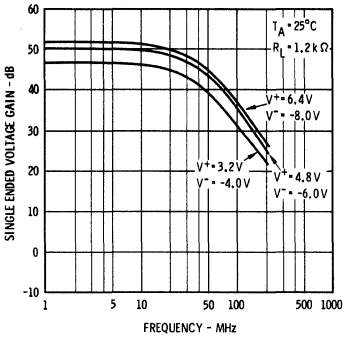
PHASE SHIFT AS A FUNCTION OF FREQUENCY



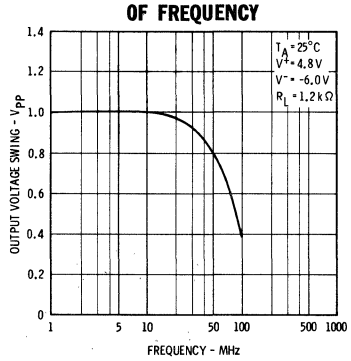
GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE



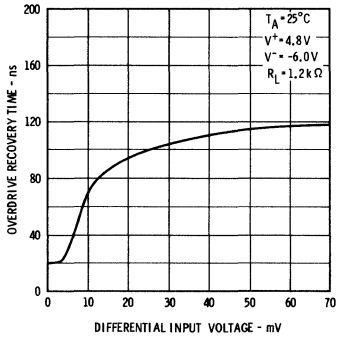
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

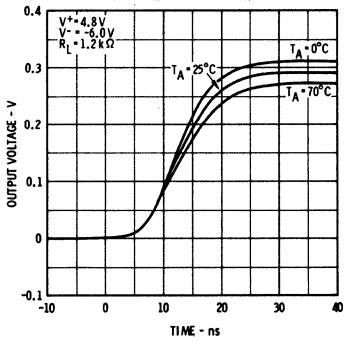


DIFFERENTIAL OVERDRIVE RECOVERY TIME

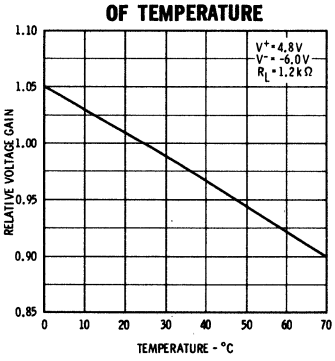


TYPICAL PERFORMANCE CURVES

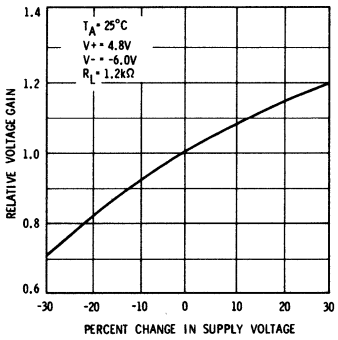
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



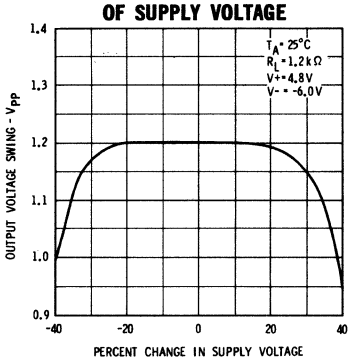
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



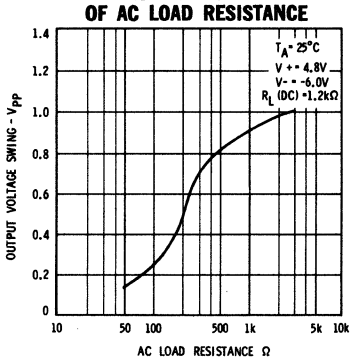
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



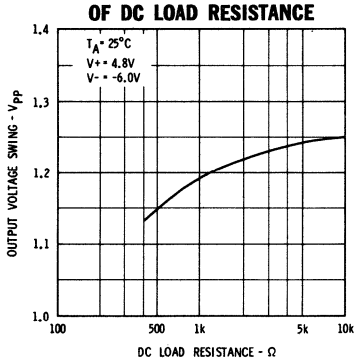
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



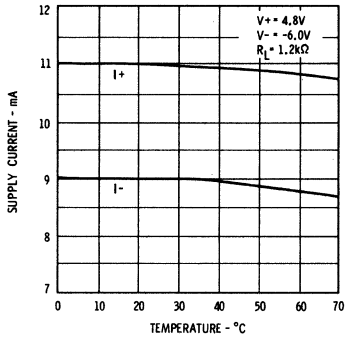
OUTPUT VOLTAGE SWING AS A FUNCTION OF AC LOAD RESISTANCE



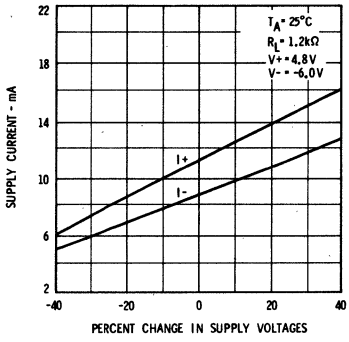
OUTPUT VOLTAGE SWING AS A FUNCTION OF DC LOAD RESISTANCE



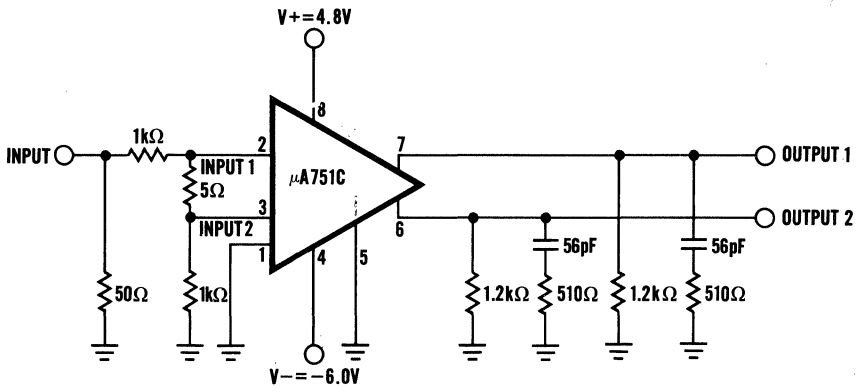
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TEST CIRCUIT



NOTE: Circuit measures device performance with common mode and differential pulses simultaneously applied and typical output loading. Pin numbers are for TO-99 package.

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH — The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE — The resistance seen between the two input terminals.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.

OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without distortion. This includes the unbalance caused by output offset voltage.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal.

POWER SUPPLY CURRENT — The current required from the power supplies to operate the device with each output externally loaded with 1.2 kΩ.

LINEAR INTEGRATED CIRCUITS COMING SOON

Type	Function	Type	Function
μA715	High Speed Operational Amplifier	μA740	Field Effect Operational Amplifier
μA725	Instrumentation Amplifier	μA742	AC Power Control System (Trigac)
μA731	High Speed Dual Channel Sense Amplifier	μA744	Radiation Resistant Operational Amplifier
μA735	Micropower Operational Amplifier	μA749	Dual Operational Amplifier

COMMUNICATIONS CIRCUITS

Second Generation linear circuits will make their biggest impact in the field of communications. Previously limited by high noise, restricted frequency range, and poor dynamic range performance, linear circuits will extend their usefulness into the microwave range with operation above 1 GHz. An entire family of circuits is under development for manpack, mobile, and ground based communication systems as well as for radar, CATV, and telephone systems. These circuits will find use as AM & FM IF amplifiers, balanced modulators and demodulators for suppressed carrier systems, frequency doublers, oscillators, logarithmic amplifiers, variable phase shifters, audio mixers, ultra wide band amplifiers, multiplex decoders, and RF amplifiers.

μA715 — HIGH SPEED OPERATIONAL AMPLIFIER

DESCRIPTION

The μA715 is a monolithic, high speed, high gain, operational amplifier featuring high slew rate, low setting time, low offsets, high input impedance, wide common mode range, high output swing, and zero adjust. It is useful in A to D and D to A converters, phase locked loops, video amplifiers, sample and holds, and multiplexed analog gates where moderate speeds and bandwidths from D.C. to 30 MHz are required.

FEATURES

Input Impedance	10 MΩ
Open Loop Gain	45,000
Slew Rate at Unity Gain	20V/μS
SUPPLY VOLTAGES	±5 to ±18 V
TEMPERATURE RANGES	−55 to +125°C
	0 to +70°C
PACKAGES	TO-5, FLATPACK, and DIP

μA725 — INSTRUMENTATION AMPLIFIER

DESCRIPTION

This operational amplifier is specifically designed for use in low level process control and instrumentation systems. Second generation processing allows the design of the circuit to reach a level of complexity and performance previously attained in discrete designs requiring as many as 100 transistors. Noise levels closely approach thermal noise limits.

FEATURES

Noise Voltage (0.01 to 1 Hz)	$0.5\mu V_{p\text{-}p}$
Open Loop Gain	120 dB
Offset Voltage Drift	0.6μV/°C
Common Mode Rejection	125 dB
Supply Rejection	100 dB
Input Offset Current	3 nA

μA731 — HIGH SPEED DUAL CHANNEL SENSE AMPLIFIER

DESCRIPTION

The μA731 is designed for high speed core memories operating at cycle times down to 400 nS. The device will accept inputs from two sense lines and consists of two preamplifiers OR'd into a thresholding circuit which drives the output logic which can be used as a memory data resistor. The device features fast response time, tight threshold accuracy and CCSL output logic.

FEATURES

Threshold Accuracy	2 mV*
Threshold Range	0 to 50 mV
Propogation Delay	30 nS
Strobe Release Time Variation	±5 nS
SUPPLY VOLTAGES	±6 Volts
TEMPERATURE RANGE	−55 to +125°C
	0 to +70°C
PACKAGES	DIP and FLATPACK

*Worst case for unit to unit, 5% power supplies and 0 to +70°C temperature range.

μA735 — MICROPOWER OPERATIONAL AMPLIFIER

DESCRIPTION

Many applications of operational amplifiers call for minimum power consumption. This amplifier features electrical performance on a par with the μA709 but consumes much less power. Some applications are: missiles, portable military equipment, spacecraft, ordnance and medical electronics.

FEATURES

Power Consumption	100 μW
Operating Supply Voltage Range	±3 V to ±15 V
Open Loop Gain	88 dB
Input Impedance	3 MΩ
Input Offset Current	2 nA
Input Offset Voltage	3 mV
TEMPERATURE RANGE	−55 to +125°C
	0 to +70°C
PACKAGE	TO-5, FLATPACK, and DIP

μA740 FIELD EFFECT OPERATIONAL AMPLIFIER

DESCRIPTION

The μA740 is a monolithic FET input high performance operational amplifier featuring ultra high input impedance, low input current, wide common mode range, short circuit protection, and zero adjust. It is internally compensated for unity gain, and is useful as an integrator, active filter, and other applications requiring high input impedance and low input currents.

FEATURES

Input Impedance	$10^{11}\ \Omega$
Input Offset Current	50 pA
Open Loop Voltage Gain	100 dB
Slew Rate	8 V/μS
Output Swing	±13 V
SUPPLY VOLTAGES	±5 to ±20 V
TEMPERATURE RANGE	−55 to +125°C
	0 to +70°C
PACKAGE	TO-5, FLATPACK, and DIP

μA742 — AC POWER CONTROL SYSTEM (Trigac)

DESCRIPTION

This versatile circuit is designed for a variety of AC power controls where it performs the interface detection and signal translation to trigger pulses for thyristors such as SCR's. The device consists of a voltage regulator, oscillator, differential amplifier, and signal processor. Four layer functions such as integrated gate turn-off SCR's, made possible by second generation technology, permit circuit designs unattainable with either discrete components or first generation integrated circuits.

Firing is accomplished at the zero crossing of load current thus minimizing RFI and allowing operation with leading, lagging, or resistive loads. The circuit also provides adjustable hysterisis set points, operation with either positive or negative temperature coefficient sensors, and time proportioning operation for precision control.

FEATURES

Peak Output Current	2 A
Supply Voltage Operation	DC, or AC to 440 Hz
Supply Voltage Range	24 V and higher
High Common Mode Noise Immunity	
TEMPERATURE RANGE	−55 to +125°C
	0 to +70°C
PACKAGE	DIP

LINEAR INTEGRATED CIRCUITS COMING SOON

μA744 — RADIATION RESISTANT OPERATIONAL AMPLIFIER

DESCRIPTION

This device offers electrical performance similar to the μA709, and is pin compatible. Built using dielectric isolation, the unit is resistant to both gamma and neutron radiation and meets military post irradiation specifications.

FEATURES

Input Offset Voltage	1 mV
Input Offset Current	50 nA
Input Bias Current	200 nA
Open Loop Gain	94 dB
Input Impedance	100 kΩ
Output Voltage Swing	±10 V
SUPPLY VOLTAGE	±9 V to ±15 V
TEMPERATURE RANGE	−55 to +125°C
	0 to 70°C
PACKAGE	TO-5, FLATPACK, and DIP

μA749 — DUAL OPERATIONAL AMPLIFIER

DESCRIPTION

This device consists of two identical differential-input, single-ended output operational amplifiers built on a single chip. These high gain, high output swing amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltages and temperatures. External loads allow high output capability and circuit flexibility.

FEATURES

Input Offset Voltage	1.0 mV
Input Offset Current	50 nA
Voltage Gain	20,000
Output Swing	±13 V
SUPPLY VOLTAGE	±4 V to ±18 V
TEMPERATURE RANGE	−55 to +125°C
	0 to +70°C
PACKAGE	TO-5, FLATPACK, and DIP

MOS Integrated Circuits

MOS INTEGRATED CIRCUIT NUMERICAL INDEX

MOS/LSI CROSS REFERENCE

Part No.	Device Type	PACKAGES		
		DIP	Flat Pack	TO-5
MOS				
3100	Dual 5 Input Gate	6J		
3101	Dual J-K Flip Flop	6J		
3102	Dual 3-Input Gate	6J		5F
3250	CRT Numeric Character Generator	6G		
3300	25-Bit Static Shift Register			5F
3303	Dual 25-Bit Dynamic Shift Register			5F
3304	Dual 16-Bit Static Shift Register			5F
3305	64-Bit Static Shift Register	6J		5F
3320	64-Bit Dynamic Shift Register			5F
3501	1024-Bit Read Only Memory	6G		
3530	64-Bit Static Random Access Memory	6J		
3700	4-Channel Multiplex Switch with all channel blanking	3J		
3701	6-Channel Multiplex Switch	3J		
3705	8-Channel Multiplex Switch CCSL Compatible	6J	3Q	
3750	10-Bit D/A Converter	6H	3V	
3751	12-Bit A/D Converter	6H	3V	
3800	8-Bit Parallel Accumulator	6H		
3801	10-Bit SER/PAR, PAR/SER	6H		

3100
FIVE-INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3100 dual five-input gate is a MOS monolithic integrated circuit. This device can be utilized as a logic block in an all MOS system, or as a breadboarding gate in designing customer integrated circuits. Input protection is provided on all inputs.

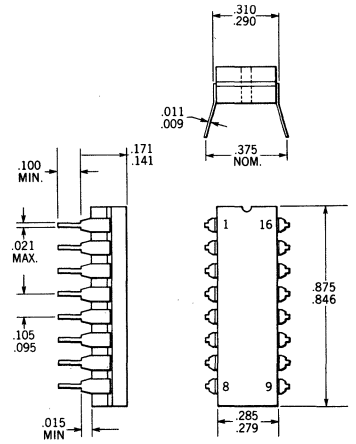
FEATURES

- **GATE PROTECTION**
- **INVERTED AND NON-INVERTED OUTPUT BUFFERS**
- **AND/OR, NAND/NOR CAPABILITY**

ABSOLUTE MAXIMUM RATINGS (Notes 2 & 3)

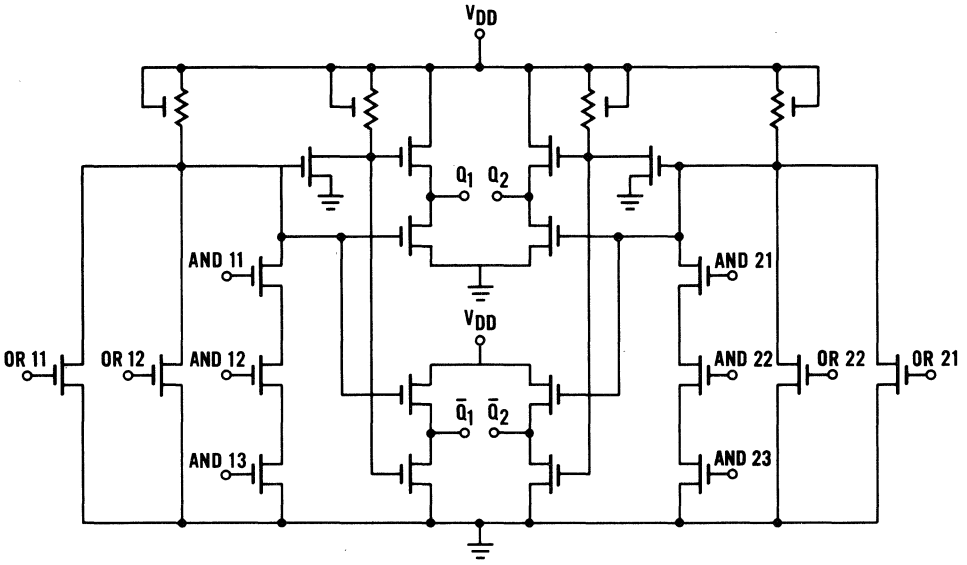
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any pin	+0.3 V
Negative Voltage on any pin	−30 V

PHYSICAL DIMENSIONS
16 Lead Dual In-Line

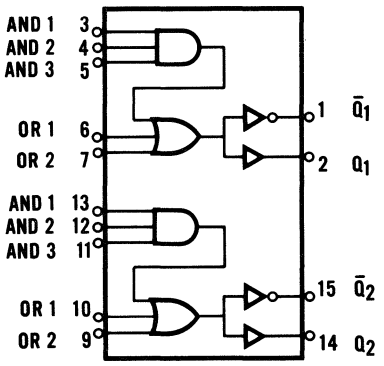


ORDER PART NO. A6J310014X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Polarity indicators (o) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≃ −10V and LO = "0" ≃ Gnd.

NOTES:
(1) These ratings are limiting values above which serviceability may be impaired.
(2) Voltage levels are with respect to GND Pin.

Electrical Characteristics on Page 2

*Planar is a patented Fairchild process.

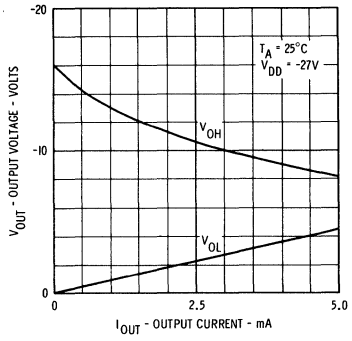
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

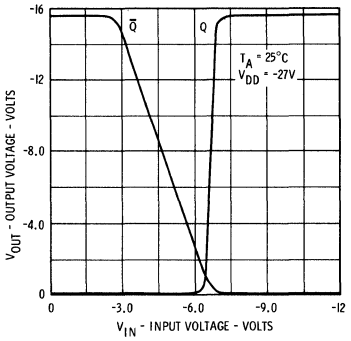
ELECTRICAL CHARACTERISTICS ($V_{DD} = -27 \pm 2$ Volts, Load = 10 MΩ, 10 pF, $T_A = +25°C$ unless otherwise specified)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Output Impedance to Ground		1.0	1.5	kΩ	$I_{OUT} = 100\ \mu A$
Input Leakage Current			1.0	μA	$V_{IN} = -20$ V
Input Capacitance		5.0		pF	$V_{IN} = 0$ V
Input Logic Levels					
"0" Level	0		−2.0	Volts	
"1" Level	−9.0			Volts	
Input Data Pulse Width	0.5			μs	
Output Logic Levels					
"0" Level			−1.0	Volts	
"1" Level	−10			Volts	
t_{pd+} (Q)		0.4		μs	
t_{pd-} (Q)		0.4		μs	
t_{pd+} ($\overline{Q}$)		0.4		μs	
t_{pd-} ($\overline{Q}$)		0.6		μs	
Power Consumption		60		mW	

TYPICAL OUTPUT CHARACTERISTIC



TYPICAL TRANSFER CHARACTERISTICS



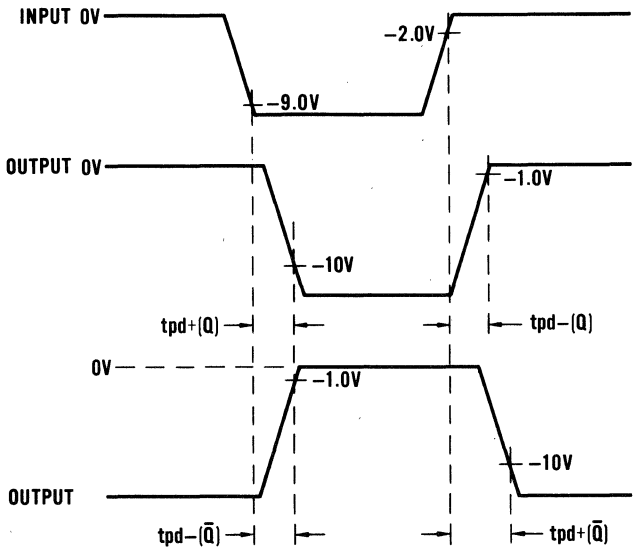
TRUTH TABLE

A OR_1	B OR_2	C AND_1	D AND_2	E AND_3	Q	$\overline{Q}$
0	0	0	0	0	0	1
0	0	0	0	1	0	1
0	0	0	1	0	0	1
0	0	0	1	1	0	1
0	0	1	0	0	0	1
0	0	1	0	1	0	1
0	0	1	1	0	0	1
0	0	1	1	1	1	0
0	1	X	X	X	1	0
1	0	X	X	X	1	0
1	1	X	X	X	1	0

Logical '1' is more negative than −9.0 V
Logical '0' is more positive than −2.0 V and ≤ 0 V
X is either '1' or '0'

BOOLEAN FUNCTION: $\underline{Q = A + B + C \cdot D \cdot E}$
$\overline{Q = A + B + C \cdot D \cdot E}$

TYPICAL PROPAGATION DELAY



3101

DUAL JK FLIP-FLOP

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3101 dual JK flip-flop is a MOS monolithic integrated circuit utilizing P-Channel enhancement technology. This device can be utilized as a logic block in an all MOS system, or as a breadboarding flip-flop in designing custom integrated circuits. Input protection is provided on all inputs.

FEATURES

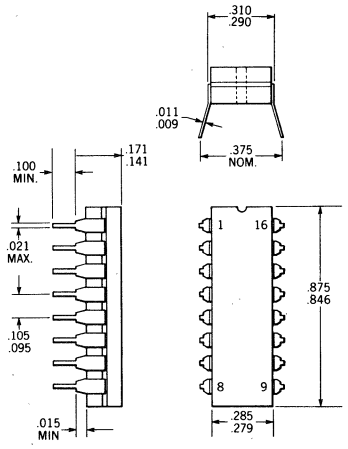
- **INPUT PROTECTION**
- **BUFFERED OUTPUTS**
- **ASYNCHRONOUS SET AND CLEAR**
- **SEPARATE CLOCK LINES**

ABSOLUTE MAXIMUM RATINGS (Notes 1 & 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any pin	+0.3 V
Negative Voltage on any input pin	−30 V

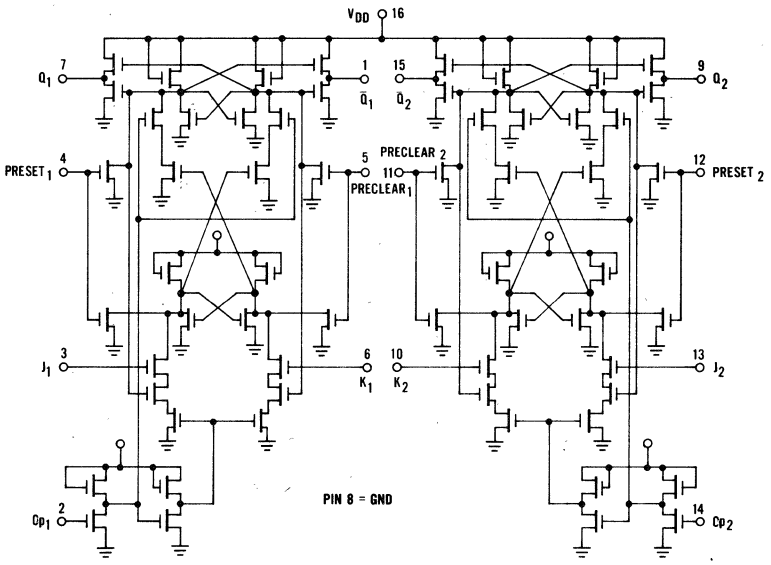
PHYSICAL DIMENSIONS

16 Lead Dual In-Line



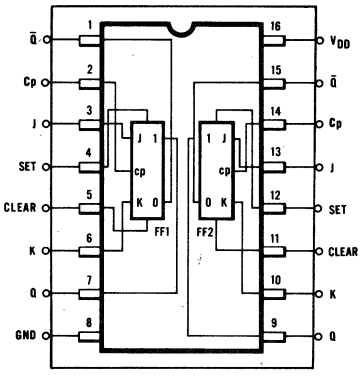
ORDER PART NO. A6J310114X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(TOP VIEW)



NOTE: Polarity indicators (o) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≃ −10V and LO = "0" ≃ Gnd.

NOTES:

(1) These ratings are limiting values above which serviceability may be impaired.

(2) Voltage levels are with respect to the GND Pin.

FAIRCHILD SEMICONDUCTOR

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($V_{DD} = -27 \pm 2$ Volts, $T_A = 25°C$ unless otherwise specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Frequency	DC		250	kHz	$V_{DD} = -26$ V
Clock Amplitude	−9.0			Volts	
Clock Pulse Width	1.0			μs	
Input Leakage Current			1.0	μA	$V_{IN} = -20$ V
Input Capacitance		5.0		pF	$V_{IN} = 0$ V
Input Logic Levels					
"0" Level	0		−2.0	Volts	
"1" Level	−9.0			Volts	
Input Data Pulse Width	1.0			μs	
Output Impedance to Ground			1.0	kΩ	
Output Logic Levels					
"0" Level			−1.0	Volts	
"1" Level	−10			Volts	
t_{setup}		0.5		μs	
$t_{release}$		0.5		μs	
t_{pd+}		1.0		μs	
t_{pd-}		0.5		μs	
Power Consumption		75		mW	

TRUTH TABLE

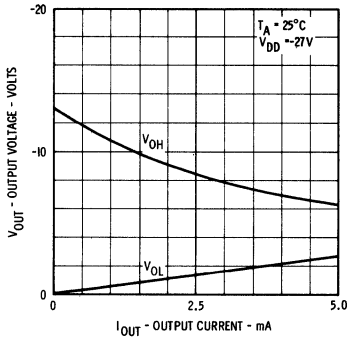
J $t = n$	K $t = n$	Q $t = n + 1$
0	0	X^n
0	1	0
1	0	1
1	1	$\overline{X}^n$

Logical '1' is more negative than −9.0 V

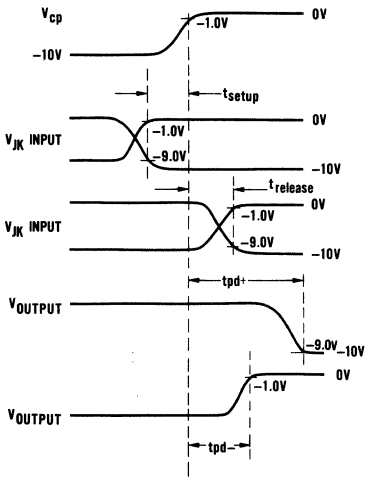
Logical '0' is more positive than −2.0 V and ≤ 0

X^n is the output state at time n

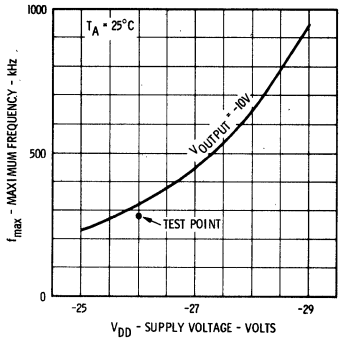
TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SWITCHING WAVEFORMS



MAXIMUM FREQUENCY VERSUS SUPPLY VOLTAGE



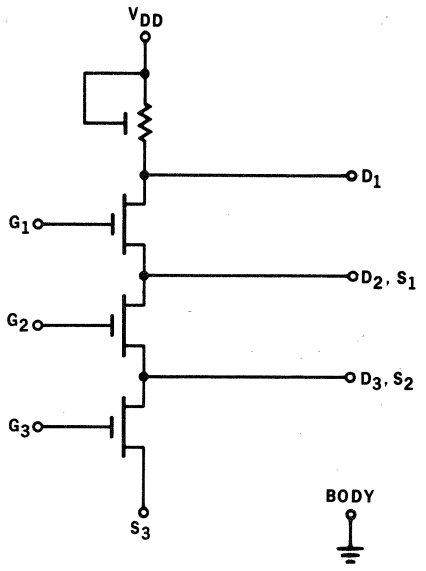
3102
3 INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3102 is a MOS Monolithic 3-Input Gate Integrated Circuit. This device can be utilized as a vehicle in gaining familiarity with MOS integrated circuit logic versatility, as a building block in an all MOS system, or as a breadboarding gate in designing complex custom integrated circuits. Input protection is provided on all gate inputs.

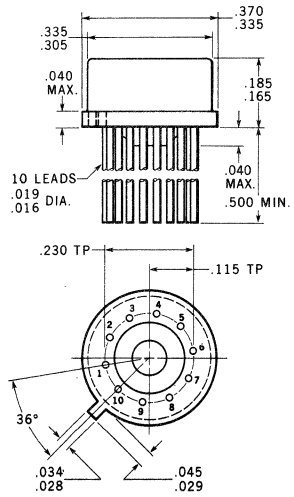
ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any Pin ($V_{Body} = 0$)	+0.3 Volt
Negative Voltage on any Pin ($V_{Body} = 0$)	−35 Volts
Power Dissipation at $T_A = 25°C$	≤200 mW

SCHEMATIC DIAGRAM



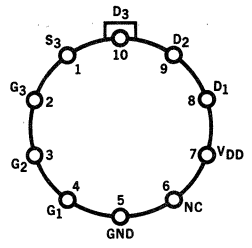
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO. A5F3102XXX

CONNECTION DIAGRAM



TOP VIEW

NOTES:
(1) These ratings are limiting values above which serviceability of the device may be impaired.

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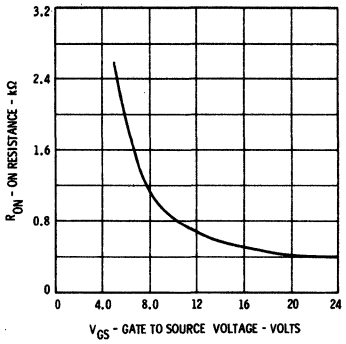
ELECTRICAL CHARACTERISTICS ($V_{Body} = 0$; $T_A = 25°C$)

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
R_{Load}	$V_{DD} = -27\ V \pm 2.0\ V$ $V_{D1} = Gnd$		140		kΩ
R_{ON}(See Figure 1)	$V_{IN} = -20\ V$		500		Ω
Input Leakage Current	$V_{IN} = -25\ V$			1.0	μA
Threshold Voltage (V_{TH})	$V_D = V_G$, $I_D = -10\ \mu A$	−2.0		−5.5	V
Input Capacitance			4.0		pF
Power Consumption	$V_{DD} = -30\ V$, $V_{IN} = -10\ V$		6.0		mW

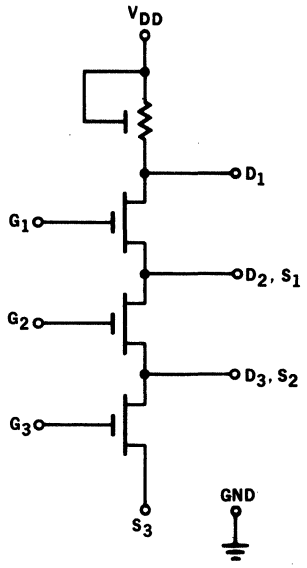
FIG. 1
TYPICAL "ON" RESISTANCE



RESISTANCE CHARACTERISTIC

Parameters	Conditions	TYP.
R_{Load}	$V_{DD} = -25\ V$ $V_{D1} = 0\ V$	140 kΩ
R_{ON}	$V_{GS} = -20\ V$ $V_{DS} \leq -1.0\ V$ $V_{D2} = 0\ V$	500 Ω
R_{ON}	$V_{GS} = -9.0\ V$ $V_{DS} \leq -1.0\ V$ $V_{D2} = 0\ V$	800 Ω

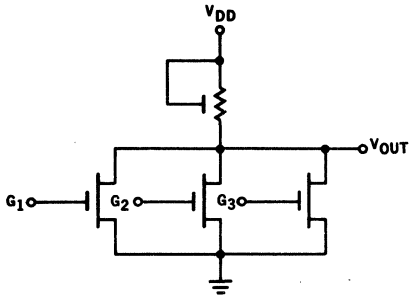
SCHEMATIC DIAGRAM



NOR GATE CONFIGURATION

Pin 8 = Pin 10 = V_{OUT}
Pin 1 = Pin 9 = GND
$V_{DD} = -27\ V \pm 2.0\ V$

	LOGIC LEVEL	VOLTAGE LEVEL MIN.	VOLTAGE LEVEL MAX.
V_{IH}	1	−9.0 V	
V_{IL}	0		−2.0 V
V_{OH}	1	−10 V	
V_{OL}	0		−1.0 V



NAND GATE CONFIGURATION

Pin 5 = GND
Pin 8 = OUTPUT
$V_{DD} = -27\ V \pm 2.0\ V$

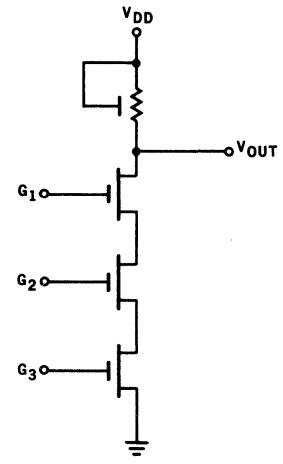


FIG. 2
TYPICAL DRAIN TO SOURCE CHARACTERISTICS

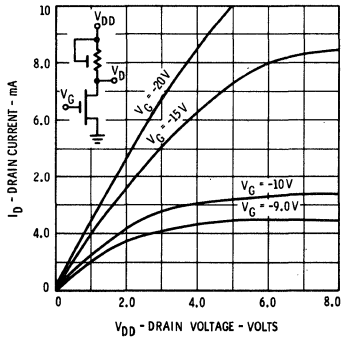
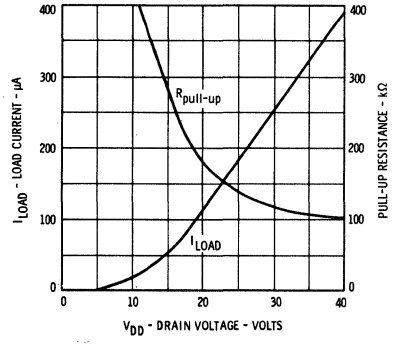
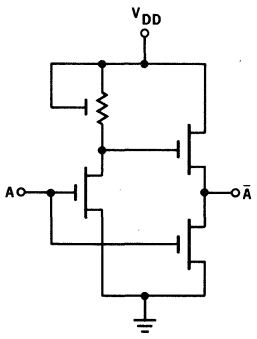


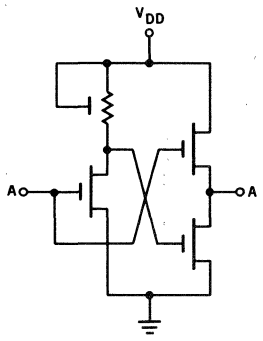
FIG. 3
TYPICAL PULL-UP RESISTANCE



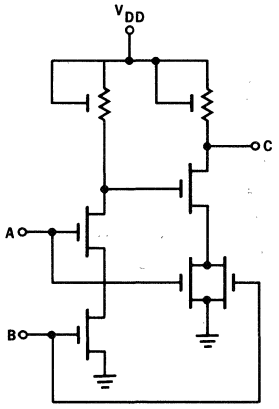
APPLICATIONS — MOS logic will provide the versatility to build many different functions. The following circuits show how to build the functions using one or two 3102 packages.



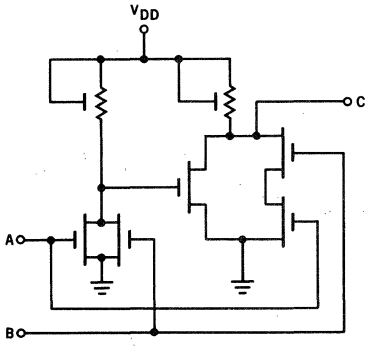
INVERTING BUFFER



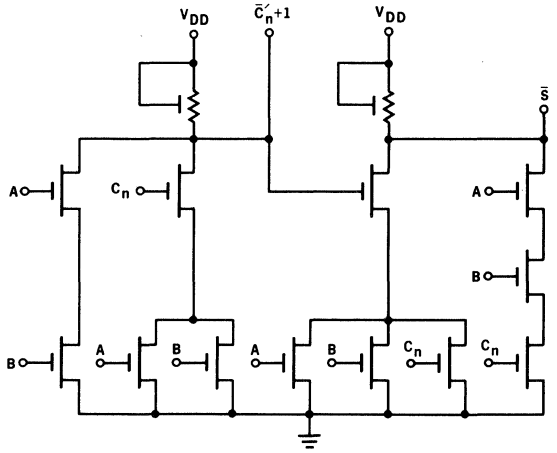
NON-INVERTING BUFFER



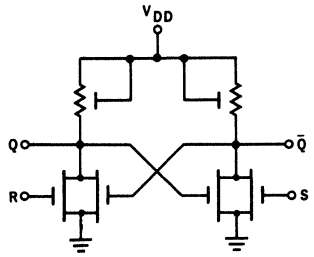
$C = AB + \bar{A}\bar{B}$
EXCLUSIVE NOR



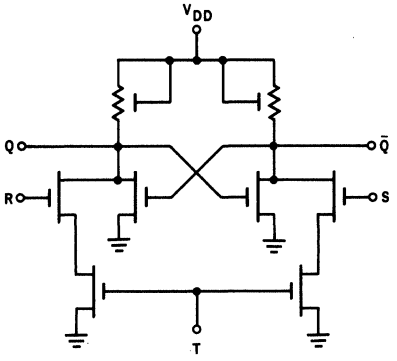
$C = \bar{A}B + \bar{B}A$
EXCLUSIVE OR



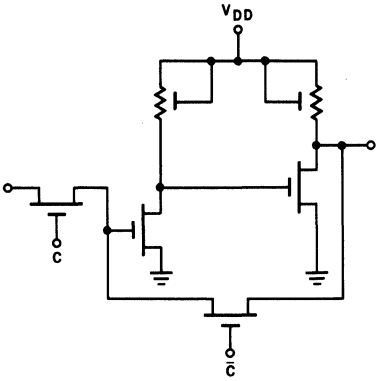
$C'_{n+1} = AB + C_n(A + B)$
$S = (A+B+C_n)\,C'_{n+1} + ABC_n$
FULL ADDER



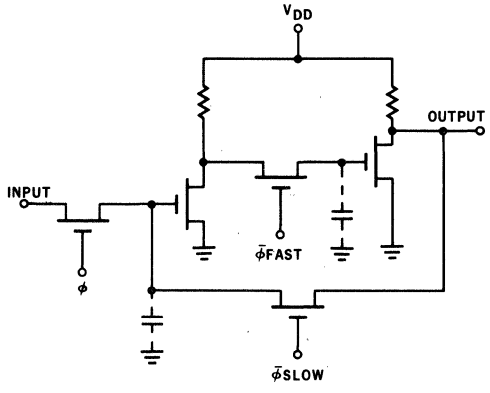
RS FLIP-FLOP



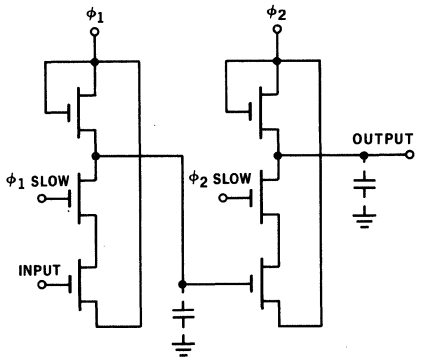
RST FLIP-FLOP



TYPE D FLIP-FLOP



STATIC (DC) SHIFT REGISTER BIT



DYNAMIC 4-PHASE (4ϕ) SHIFT REGISTER BIT

3250

CRT NUMERIC CHARACTER GENERATOR

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3250 is a numeric character generator subsystem on a single chip. It is designed to be used in conjunction with a cathode ray tube to display numeric information. Deflection pulses are provided to sweep the beam through a seven segment character in eight clock pulses. Video pulses synchronized with the deflection pulses, are provided to blank the appropriate segments needed to form numerals. Approximately 520 characters may be displayed at a 60 cps refresher rate. Parallel data from a keyboard may be entered directly into the 3250 thereby simplifying systems applications.

FEATURES:

- **SERIAL OR PARALLEL STORAGE BUFFER ENTRY**
- **DIRECT KEYBOARD ENTRY**
- **250 kHz SEGMENT RATE**
- **BOTH HALF AND WHOLE ZEROS**
- **D/A TYPE OUTPUTS AVAILABLE FOR ±x, ±y CURRENT SUMMING AMPLIFIERS**
- **SPECIAL OUTPUTS FOR "1" OFFSET, DECIMAL POINT, AND OPTIONAL CONTROL USE**
- **INDEPENDENCE BETWEEN CHARACTER DISPLAY AND BUFFER MOTION**
- **160 mW POWER CONSUMPTION**
- **OPTIONAL CUSTOM CHARACTER SHAPES**

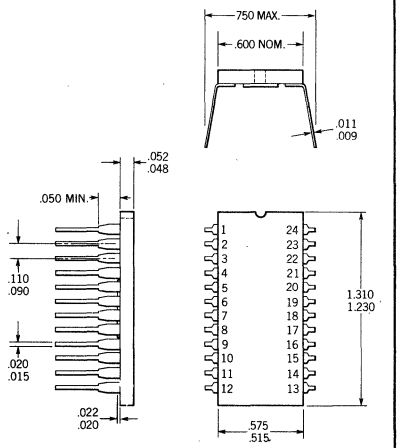
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

All Voltages and Data Input Lines	−30 V to +0.3 V
Power Supply	−30 V
Storage Temperature	−55°C to +150°C
Operating Temperature (A6G325014X)	−55°C to +85°C
(A6G325019X)	0°C to +70°C

APPLICATIONS:

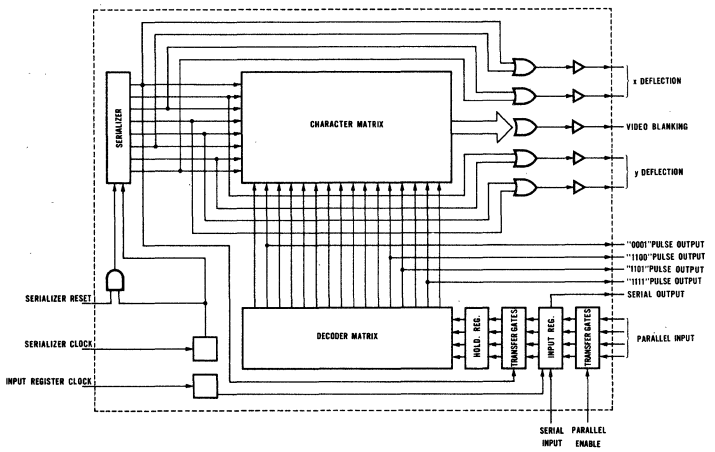
- **CALCULATOR READOUTS**
- **COCKPIT DISPLAYS**
- **TEST EQUIPMENT READOUTS**
- **DATA ACQUISITION SYSTEM READOUTS**
- **NUMERICAL CONTROL MACHINE POSITION READOUTS**
- **PROCESS CONTROL MONITORS**

PHYSICAL DIMENSION



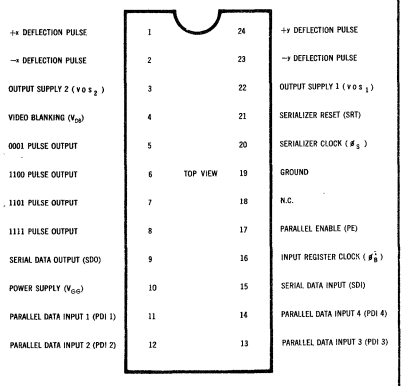
ORDER PART NO. A6G325014X **−55°C to +85°C**
ORDER PART NO. A6G325019X **0°C to 70°C**

BLOCK DIAGRAM



3250 CRT NUMERIC CHARACTER GENERATOR

PIN CONFIGURATION



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ELECTRICAL CHARACTERISTICS $V_{GG} = -27 \pm 1.0$ Volts, $R_L = 10$ MΩ, $C_L = 10$ pF (unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10		−30	Volts	
ϕ_S, ϕ_B	Clock					
	Amplitude	−9.0		−30	Volts	
W_{cp}	Width	1.0		10	μs	
f_{max}	Segment and Input Register Frequency	DC		250	kHz	
C_{IN}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		7.5	9.5	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		200	250	mW	$V_{GG} = -27$ V
I_{LX}	Input Leakage Current			5.0	μA	$V_{IN} = -20$ V
t_{df}			1.2		μs	
t_f	Rise and Fall		0.4		μs	$V_{GG} = -27$ V
t_{dr}	Times		1.0		μs	$f_{max} = 250$ kHz
t_r			1.0		μs	

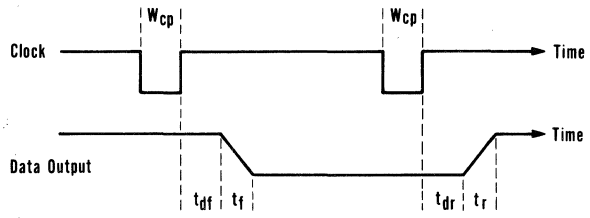
DESCRIPTION OF PIN FUNCTIONS

PIN	SYMBOL	NAME	FUNCTION
1, 2 23 24	−x, +x −y, +y	DEFLECTION PULSES	These pulses are synchronous with the video output. When differentially integrated, they provide the deflection voltages necessary to sweep a CRT beam through the basic figure eight shape.
3 22	V_{OS} 1 & 2	OUTPUT SUPPLY 1 & 2	V_{OS} 1 is normally connected to ground and V_{OS} 2 to −27 volts. However, for special applications, they may be connected anywhere between 0 and −27 volts.
4	VDB	VIDEO BLANKING	Video Blanking pulses, synchronous with the x & y deflections pulses, are supplied to display a character on the CRT.
5, 6 7, 8		SPECIAL PURPOSE OUTPUTS	Special purpose binary codes were brought out through output buffers to be utilized for control purposes. The programmed codes may be used as follows:
	0001		To control a "one offset" circuit which is necessary to center the character ONE within a character position.
	1100 1111		To be utilized at customer option. For example a blank space for decimal point control.
	1101		Character "A" is displayed with this code. An output is provided for external system control to be used at customer discretion.
9	SDO	SERIAL DATA OUTPUT	SDO is the LSB of the 4 bit input register. It may be connected to a larger buffer register.
10	V_{GG}	POWER SUPPLY	= −27 ± 1 V.

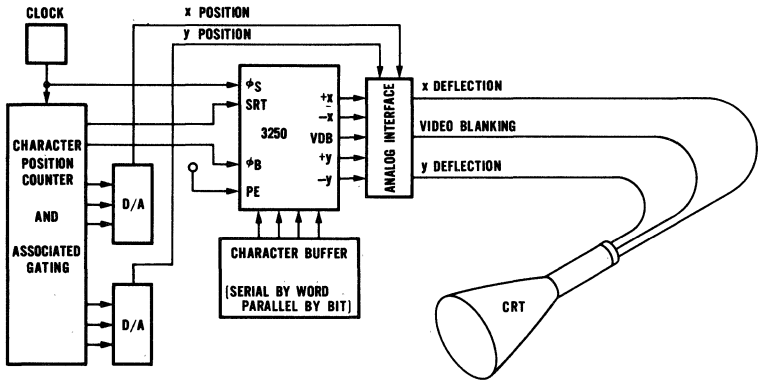
PIN	SYMBOL	NAME	FUNCTION
11— 14	PDI 1-4	PARALLEL DATA INPUTS	Parallel data entry is provided through PDI 1-4 into the input register in synchronous with ϕ_B when PE is a logical "1."
15	SDI	SERIAL DATA INPUT	SDI is shifted into the MSB of the input register when PE is a logical "0" and ϕ_B is pulsed.
16	ϕ_B	INPUT REGISTER CLOCK	ϕ_B is utilized to control the data manipulation of the input register. (See explanation for PE below.)
17	PE	PARALLEL ENABLE	Data manipulation of the input register is synchronous with ϕ_B and depends upon the logical state of PE. If PE is a logical "1," the parallel inputs PDI 1-4 are loaded into the input register (PDI 4 = MSB). If PE is a logical "0," the parallel inputs are disabled and the input register operates in a serial mode.
20	ϕ_S	SERIALIZER CLOCK	ϕ_S is utilized to control the serializer. (See explanation of SRT below.)
21	SRT	SERIALIZER RESET	If SRT is a logical "0" the serializer will shift right one position when ϕ_S is pulsed. Zero's will be inserted into the MSB as the register shifts right. If SRT is a logical "1," then a one is inserted into the first stage and the remaining seven stages are set to zero, when ϕ_S is pulsed.

TIMING DIAGRAM

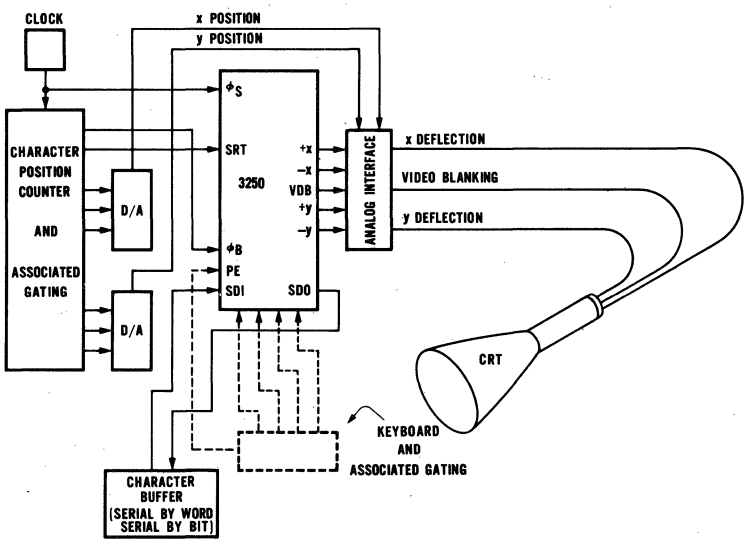
OUTPUT DELAY, RISE AND FALL TIMES



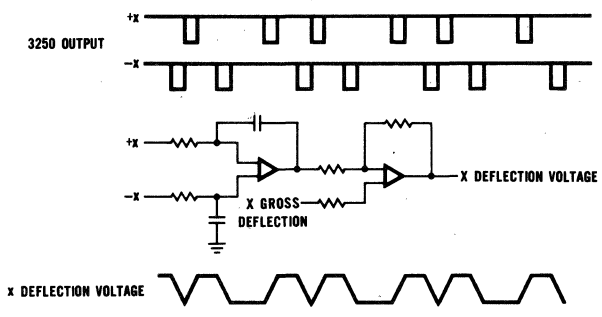
PARALLEL BUFFER APPLICATION



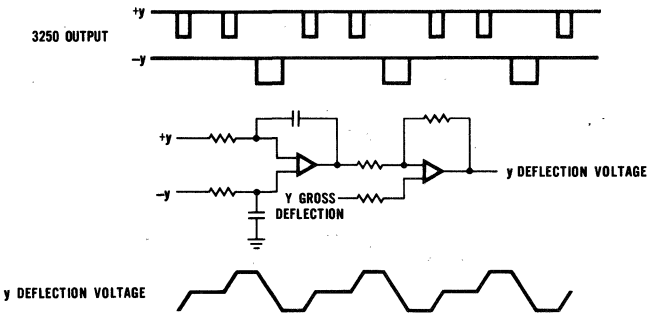
SERIAL BUFFER APPLICATION



DEFLECTION WAVE FORMS



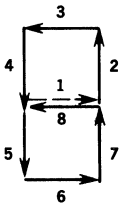
SYNTHESIS OF x DEFLECTION VOLTAGE



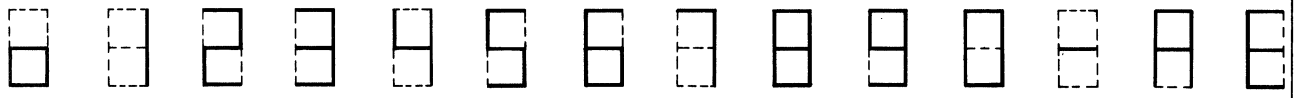
SYNTHESIS OF y DEFLECTION VOLTAGE

CHARACTER FORMATION

A dashed line indicates a blanked segment (segment one is always blanked).



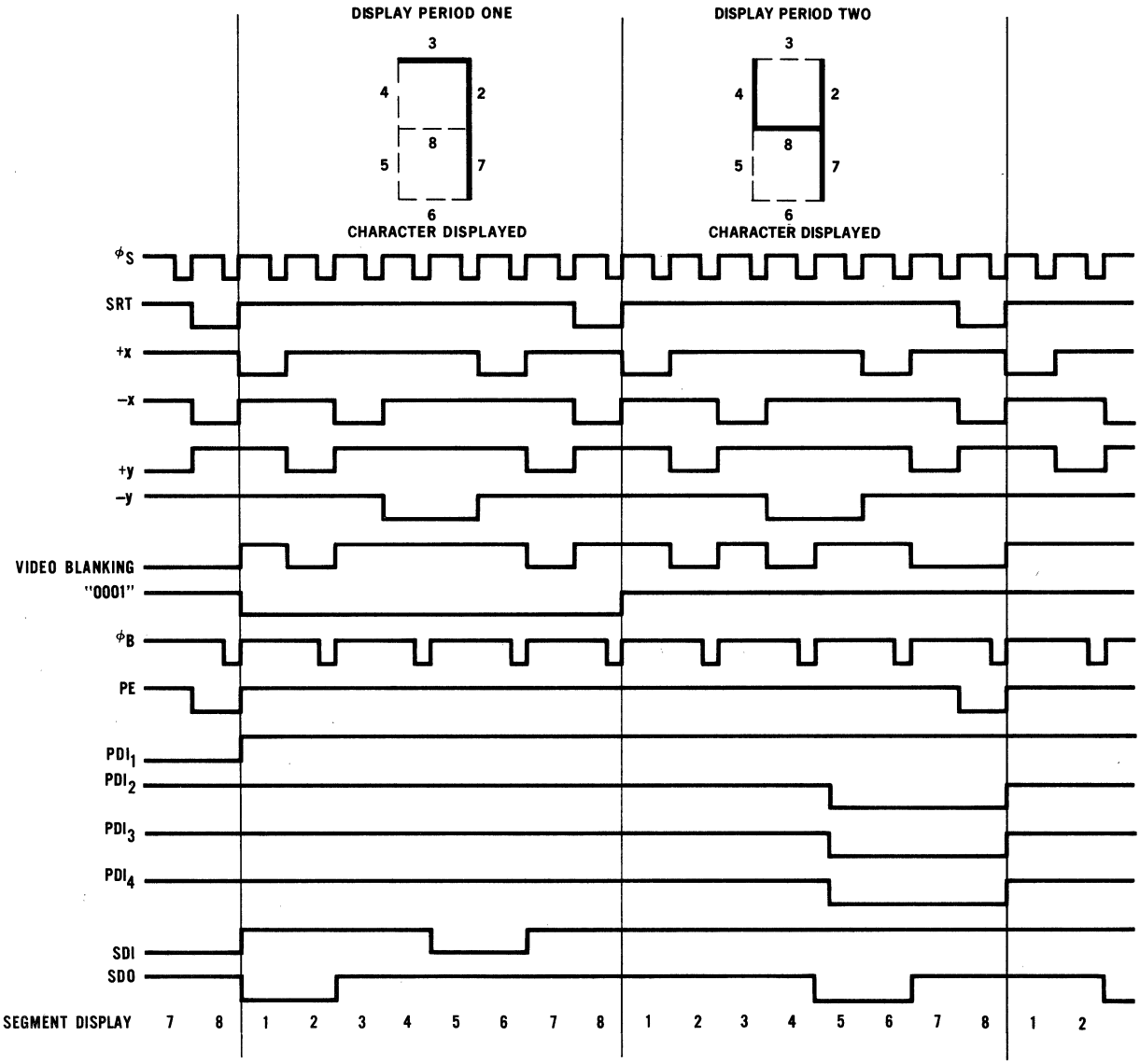
The numbers indicate the order in which segments are displayed.



BINARY* INPUT CODE	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1101	1110

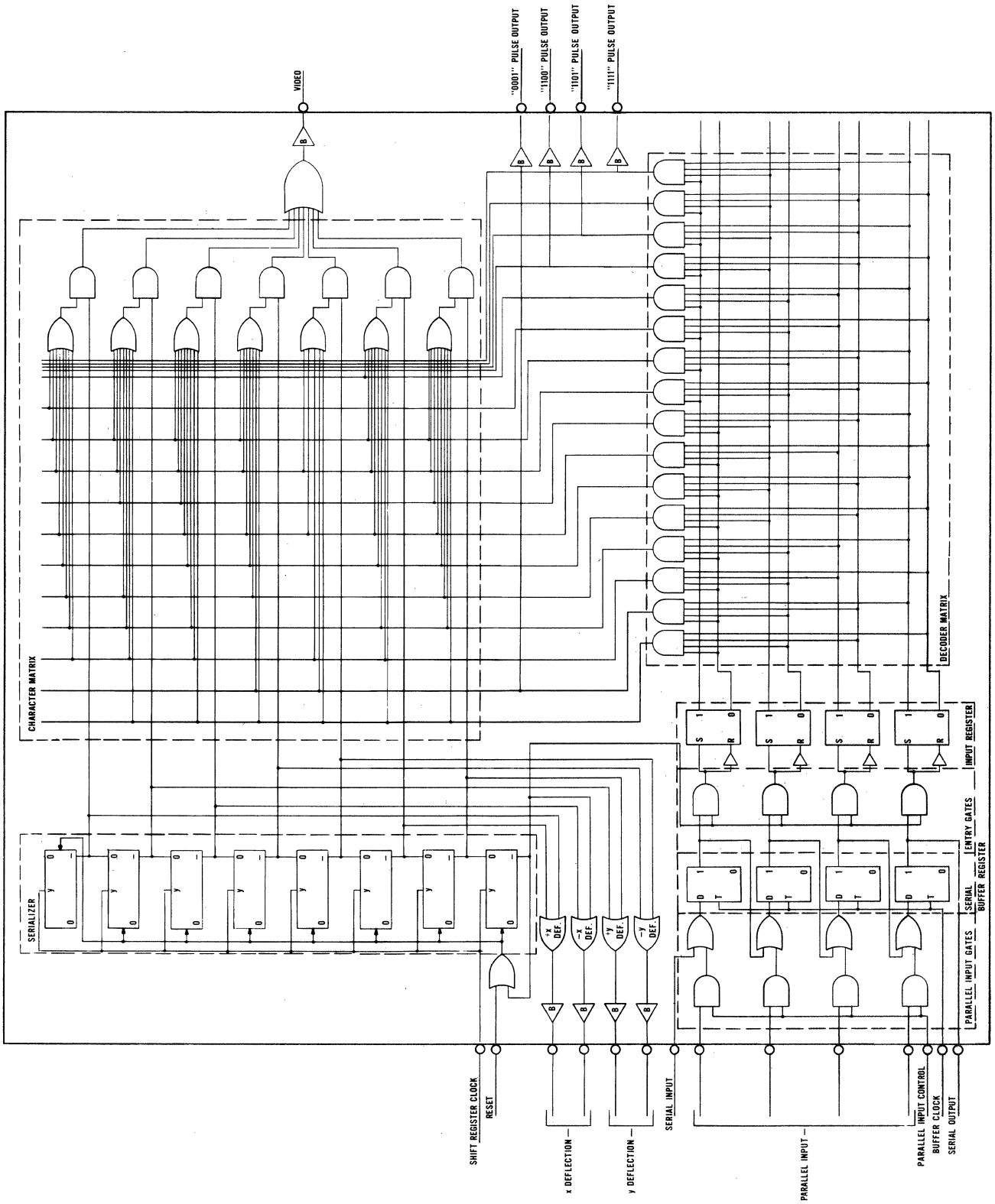
NOTES:
1. The "1100" and "1111" codes are used for special control purposes and create no corresponding display. Characters may be inserted into these positions for special applications.
2. See pin description for special outputs provided with 0001 and 1101 input codes.

TYPICAL TIMING DIAGRAM



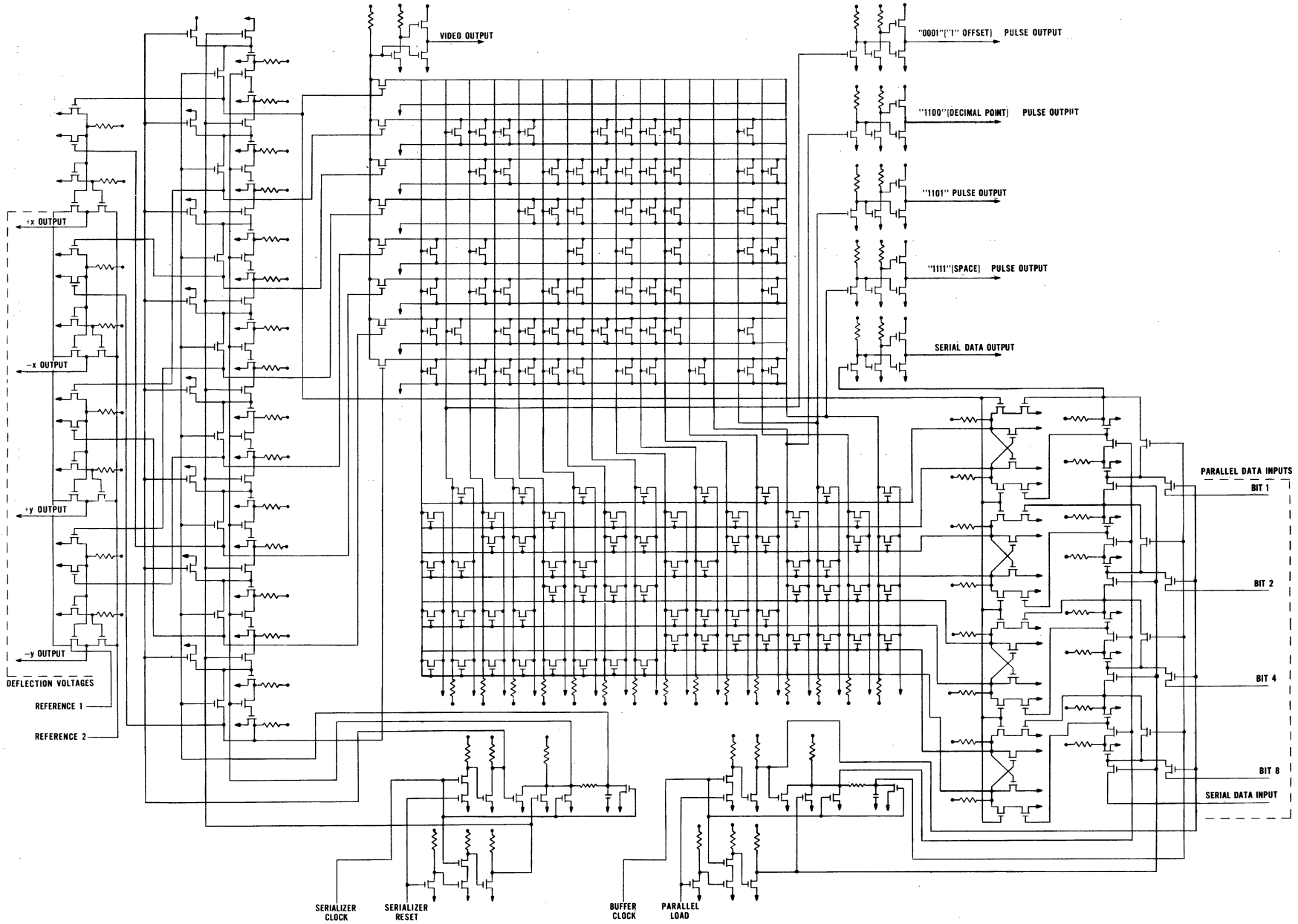
The binary data for the character displayed in period one was available for parallel loading during segment 8 of the previous period. Actual loading occurred at the fall of ϕ_8 during segment one. The binary data for the character displayed during display period two was loaded serially during display period one. The input data must not change during segment two of any display period.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (○) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈ −10 V and 1.0 = "0" ≈ Gnd.

CIRCUIT DIAGRAM



3300

25 BIT STATIC SHIFT REGISTER

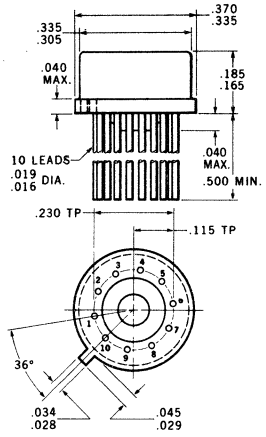
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION—The 3300 is a 25 bit Static Shift Register. It is a monolithic integrated circuit utilizing Planar II*, P-channel enhancement mode MOS technology. Input and output access is made available in 16, 8 and 1 bit increments. This device was designed for use in single phase clock sequential digital systems as a delay line or memory element.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at $T_A = 25°C$	200 mW
Voltage On Clock, Inputs and Supply Pins	−35 V to +0.3 V

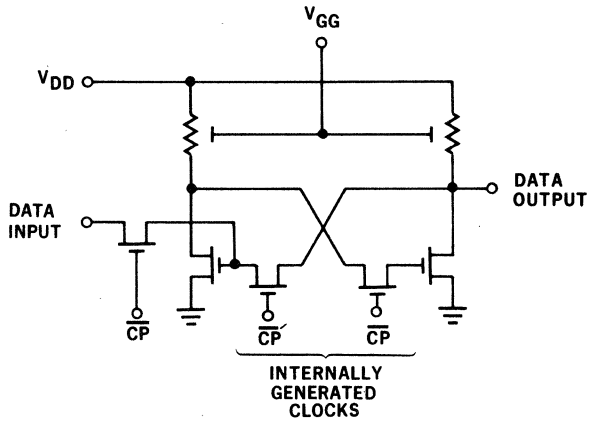
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO–100)



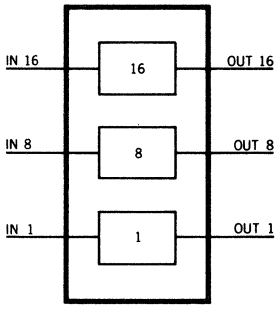
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER CODE A5F330014X

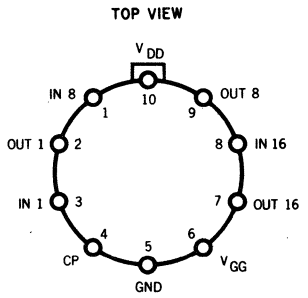
SCHEMATIC DIAGRAM
(ONE BIT)



BLOCK DIAGRAM



CONNECTION DIAGRAM



*Planar is a patented Fairchild process.

NOTE: These ratings are limiting values above which the serviceability of the device may be impaired.

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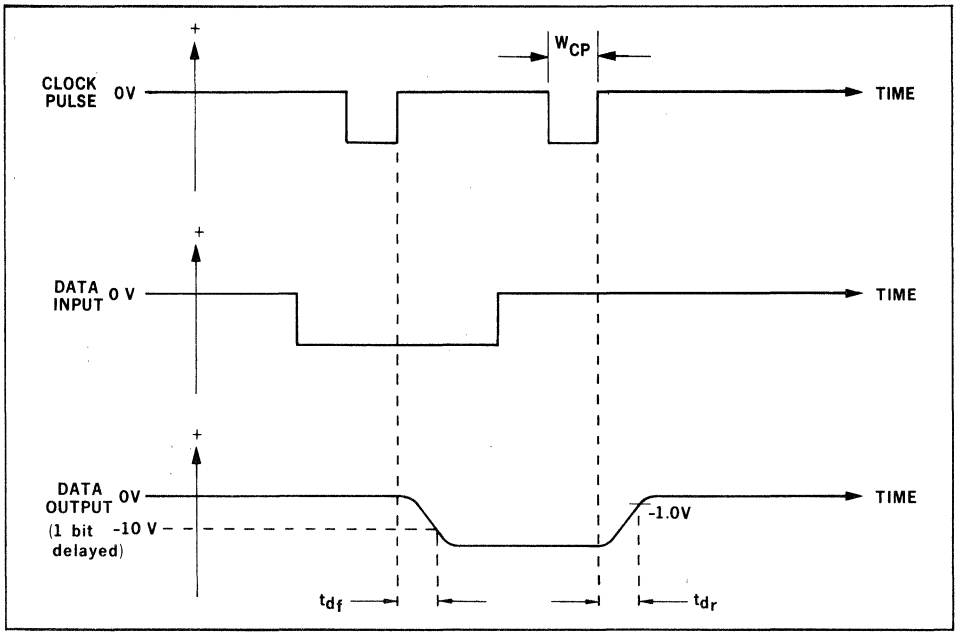
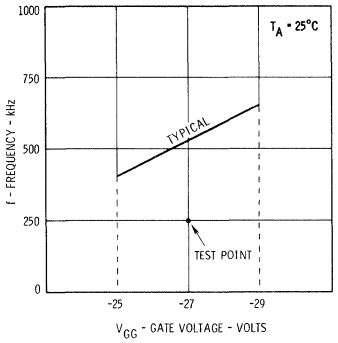
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, V_{GG} (Pin 6) $= -27 \pm 2$ V, V_{DD} (Pin 10) $= -13 \pm 2$ V, unless otherwise specified)

SYMBOL	CHARACTERISTICS		MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
	Power Consumption			50		mW	$V_{clock} = 0$ V
	Operating Frequency		0		250	kHz	$V_{GG} = -27$ V
V_{CP}	Clock Pulse Amplitude	"0" level			−2.0	Volts	
		"1" level	−9.0			Volts	
W_{CP}	Clock Pulse Width		1.0		100	μs	
	Clock Pulse Rise and Fall Time				10	μs	
	Clock Capacitance			3.0		pF	$V_{CP} = 0$ V
I_{CL}	Clock Leakage Current				−1.0	μA	$V_{CP} = -20$ V
V_{IL}	Input Amplitude	"0" level			−2.0	Volts	
V_{IH}		"1" level	−9.0			Volts	
C_{in}	Input Capacitance			2.5		pF	$V_{in} = 0$ V
I_{IL}	Input Leakage Current				−1.0	μA	$V_{in} = -20$ V
V_{OL}	Output Levels	"0" level			−1.0	Volts	$I_{out} = -10$ μA
V_{OH}		"1" level	−10			Volts	$I_{out} = -10$ μA
t_{df}	Time Delay-Fall			1.0		μs	
t_{dr}	Time Delay-Rise			1.2		μs	

TIMING DIAGRAM



TYPICAL OPERATING FREQUENCY VERSUS GATE VOLTAGE



3303

DUAL 25-BIT DYNAMIC SHIFT REGISTER

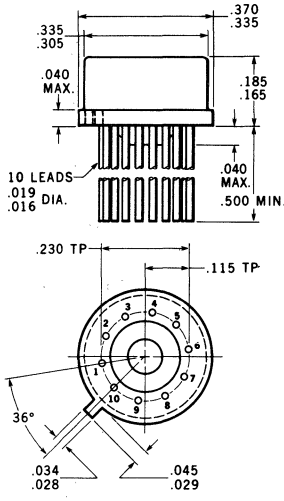
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3303 is a dual 25-bit dynamic shift register. It is a monolithic integrated circuit utilizing Planar* II, P-Channel enhancement mode MOS technology. A two phase clock is used to reduce power consumption and increase speed.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Clock Voltages ($V_{\phi_1} = V_{\phi_2}$)	−30 V to +0.3 V
Data Input Voltage (V_{in})	−30 V to +0.3 V
Supply Voltage	−30 V to +0.3 V
Storage Temperature	−65°C to +150°C
Operating Temperature (330314X)	−55°C to +85°C
Operating Temperature (330319X)	0°C to +70°C

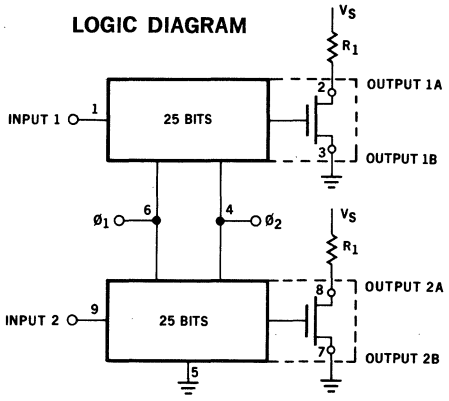
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

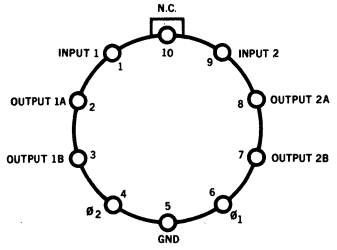
ORDER PART NOS. A5F330314X
A5F330319X

LOGIC DIAGRAM



The output device requires an external resistor (R_1), ground and power supply (V_S) and can be used either as an inverter or source follower (inverter shown).

CONNECTION DIAGRAM



TOP VIEW

NOTE:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.

Electrical Characteristics on Page 2

*Planar is a patented Fairchild process.

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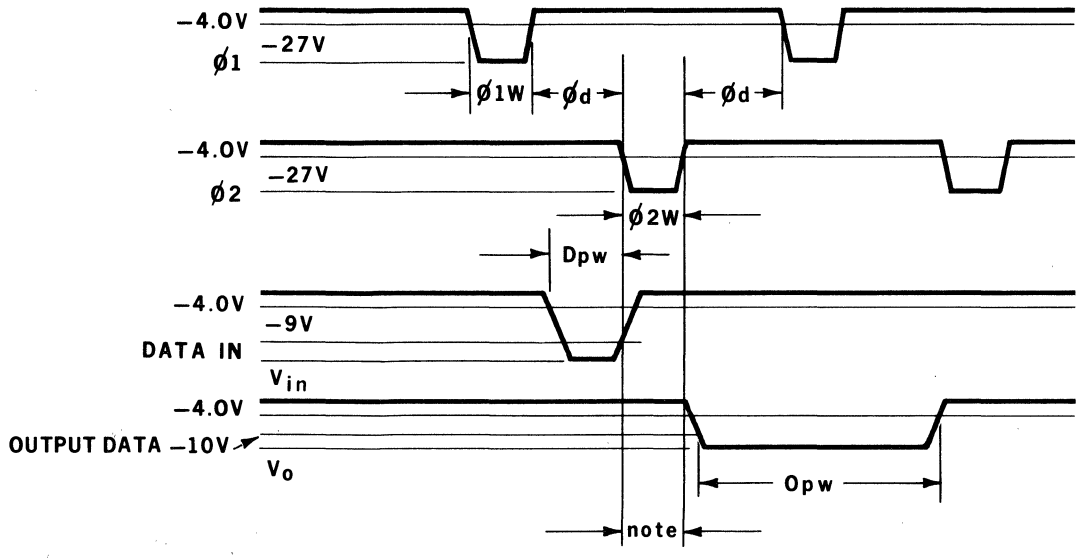
ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified)
Load . . . 10 MΩ and 10 pF
$V_S = -15\ V \pm 1.0\ V, V\phi = -27\ V \pm 1.0\ V$
$R_l = 20\ k\Omega$, $T_A = -55°C$ to $+85°C$

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
ϕ_1, ϕ_2	Clock Repetition Rate	10		500	kHz	
ϕ_{1w}, ϕ_{2w}	Clock Pulse Width	0.4		45	μs	
ϕ_d	Clock Delay	0.4			μs	
$V\phi$	Clock Pulse Amplitude					
	"0" Level	0		−0.5	Volts	
	"1" Level	−26		−28	Volts	
	Clock Pulse Rise and Fall Time (10% - 90%)			100	ns	
V_{in}	Data Input Logic Levels					
	Logic "0"	0		−2.0	Volts	
	Logic "1"	−9.0			Volts	$\phi_1 = 0.4\ \mu s$
D_{pw}	Data Pulse Width	200			ns	$\phi_2 = 0.4\ \mu s$
V_o	Output Logic Levels					
	Logic "0"			−1.0	Volts	
	Logic "1"	−10			Volts	
	Output Fall Time			550	ns	
O_{pw}	Output Pulse Width	1.0			μs	
R_o	Output Impedance to Ground			1000	Ω	
I_{CL}	Clock Input Leakage Current			100	μA	$V\phi = -26\ V$
	Data Input Capacitance		4.0		pF	$V\phi = 0\ V$
	Clock Input Capacitance		20		pF	$V\phi = 0\ V$
	Fan In			1.0		
	Fan Out			5.0		

TYPICAL WAVEFORMS



Note: Delayed 50 Bit Times

3304

DUAL 16-BIT STATIC SHIFT REGISTER

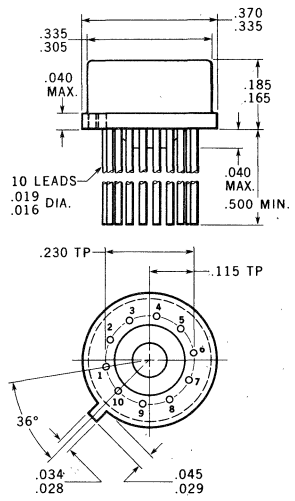
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3304 is a Dual 16-Bit Static Shift Register. It is a monolithic integrated circuit utilizing Planar II*, P-Channel Enhancement Mode MOS Technology. It is designed to operate on a two phase clock in delay line or in serial binary or BCD data storage applications. For DC storage conditions, it is important that ϕ_1 is a logic "0" and ϕ_2 is a logic "1".

ABSOLUTE MAXIMUM RATINGS (Note 1)

Drain Voltage (V_{DD})	−30 V to +0.3 V
Gate Voltage (V_{GG})	−30 V to +0.3 V
Clock and Data Input Voltages	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C
	0°C to +70°C
Power Dissipation at $T_A = 25°C$	200 mW

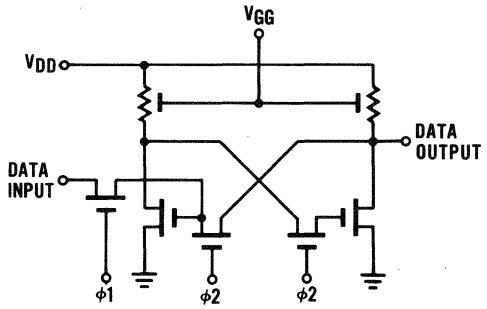
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



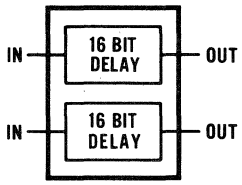
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART # A5F330414X (−55°C to +85°C)
ORDER PART # A5F330419X (0°C to +70°C)

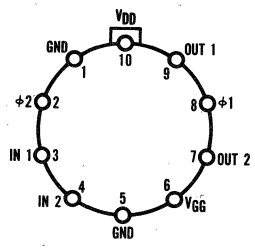
SCHEMATIC DIAGRAM
(ONE BIT)



BLOCK DIAGRAM



CONNECTION DIAGRAM
TOP VIEW



NOTE:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS

(V_{DD} = −13 Volts ±1 Volt, V_{GG} = −27 Volts ± 1 Volt, Load = 10 MΩ and 10 pF, T_A = −55°C to +85°C, unless otherwise specified)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Repetition Rate	D.C.		1.0	MHz	
Clock Pulse Widths					
ϕ_1 pw	0.4		10	μs	See Figure 1
ϕ_2 pw	0.4			μs	See Figure 1
Clock Delay (ϕd)	0.01		10	μs	See Figure 1
Clock Pulse Rise and Fall Time (10% to 90%)			5.0	μs	See Figure 1
Clock Pulse Logic Levels (ϕ_1 & ϕ_2)					
Logic "0"			−2.0	Volts	
Logic "1"	−26		−28	Volts	
Clock Pulse Input Capacitance (ϕ_1 & ϕ_2)		4.0		pF	$\phi_1 = \phi_2 = 0$ Volt
Data Pulse Width (Dpw)	0.4			μs	
Data Input Capacitance		2.0		pF	V_{IN} = 0 Volt
Data Input Logic Levels					
Logic "0"			−2.0	Volts	
Logic "1"	−9.0			Volts	
Data Input Leakage Current			1.0	μA	V_{IN} = −20 Volts
Clock Input Leakage Current			100	μA	V_{IN} = −26 Volts
Clock (ϕ_2) Input Impedance	60			kΩ	ϕ_1 = −26 Volts ϕ_2 = 0 Volt
Output Logic Levels					
Logic "0"		−0.5	−1.0	Volts	
Logic "1"	−10	−11		Volts	
Output Impedance to Ground		2.0	3.0	kΩ	Output at Logic "0"
Output Drive Capability	−5.0			Volts	R_L = 4.0 kΩ to Ground
Power Supply Current Drain V_{DD}			10	mA	V_{DD} = −13 Volts
Power Supply Current Drain V_{GG}			2.0	mA	V_{GG} = −27 Volts

TIMING DIAGRAMS

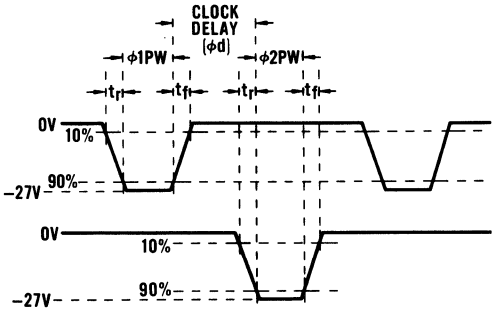


Figure 1

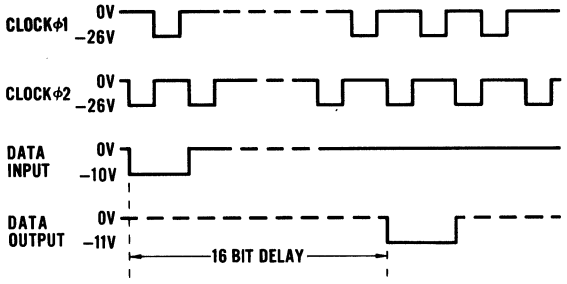
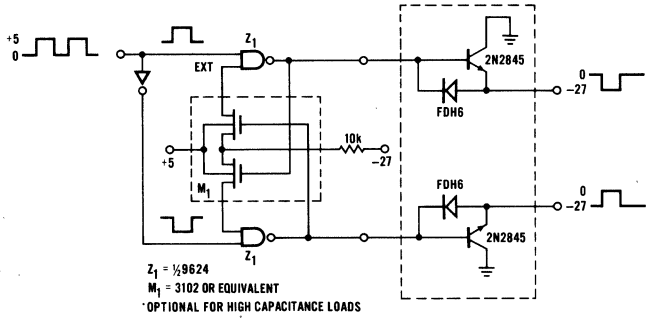


Figure 2



2 PHASE-NON-OVERLAPPING CLOCK DRIVER

3305/6

64-BIT 1Ø STATIC SHIFT REGISTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3305/6 is a 64-bit 1ϕ static shift register. The 3305 is a Quad 16 in a DIP package and the 3306 is a Dual 16, Single 32 in a TO-100 package. It is a monolithic integrated circuit utilizing Planar II*, P-channel Enhancement Mode Technology.

FEATURES:

- **SINGLE PHASE CLOCK**
- **LOW POWER CONSUMPTION — LESS THAN 3 mW/BIT**
- **HIGH SPEED OPERATION — DC TO 1.0 MHz**

APPLICATIONS:

Delay line and binary or BCD storage in:

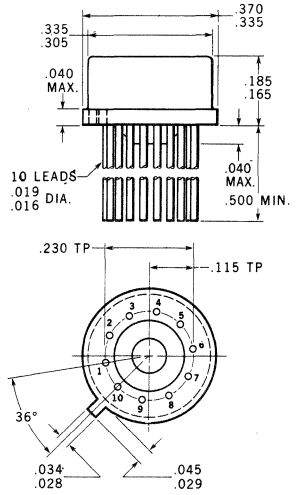
- **Calculators**
- **Peripheral Equipment**
- **Data Acquisition**
- **Telemetry**
- **Computers and Business Machines**
- **Machine Control**

ABSOLUTE MAXIMUM RATINGS (Note 1)

Drain Voltage (V_{DD})	−30 V to +0.3 V
Gate Voltage (V_{GG})	−30 V to +0.3 V
Clock and Data Input Voltages	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C
Power Dissipation at $T_A = 25°C$	300 mW

PHYSICAL DIMENSIONS

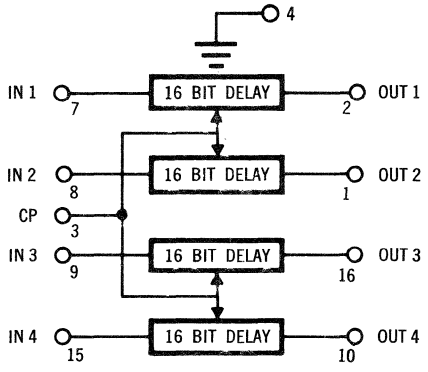
(In accordance with JEDEC TO−100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

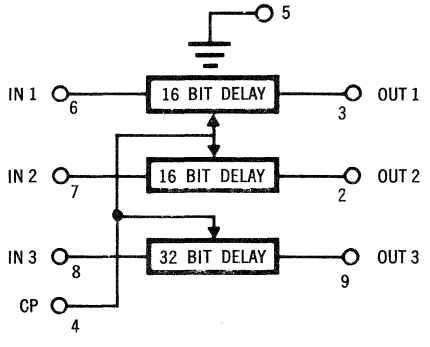
ORDER PART NO. A5F330614X

3305 BLOCK DIAGRAM



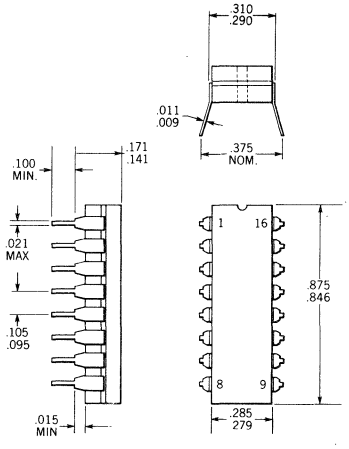
V_{GG} pin 12, V_{DD} pin 13

3306 BLOCK DIAGRAM



V_{GG} pin 10
V_{DD} pin 1
Gnd pin 5

PHYSICAL DIMENSIONS



ORDER PART NO. A6J330514X

*Planar is a patented Fairchild process.

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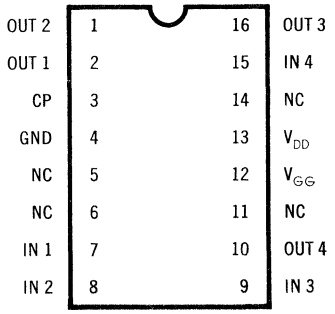
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{GG} = -27 \pm 2$ V, $V_{DD} = -13 \pm 2$ V, unless otherwise specified)

SYMBOL	CHARACTERISTICS		MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
	Power Consumption			200		mW	
	Operating Frequency		d.c.		1.0	MHz	$V_{GG} = -27$ V
V_{CP}	Clock Pulse Amplitude	"0" level			−2.0	Volts	
		"1" level	−9.0			Volts	
W_{CP}	Clock Pulse Width		0.3		100	μs	
	Clock Pulse Rise and Fall Time				10	μs	
	Clock Capacitance			8.0		pF	$V_{CP} = 0$ V
I_{CL}	Clock Leakage Current				−1.0	μA	$V_{CP} = -20$ V
V_{IL}	Input Amplitude	"0" level			−2.0	Volts	
V_{IH}		"1" level	−9.0			Volts	
C_{in}	Input Capacitance			2.5		pF	$V_{in} = 0$ V
I_{IL}	Input Leakage Current				−1.0	μA	$V_{in} = -20$ V
V_{OL}	Output Levels	"0" level			−1.0	Volts	$I_{out} = -10$ μA
V_{OH}		"1" level	−10			Volts	$I_{out} = -10$ μA
t_{df}	Time Delay Fall			0.4	0.5	μs	$V_{GG} = -27$ V
t_{dr}	Time Delay-Rise			0.4	0.5	μs	$V_{GG} = -27$ V

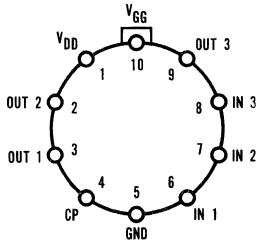
3305 CONNECTION DIAGRAM

TOP VIEW

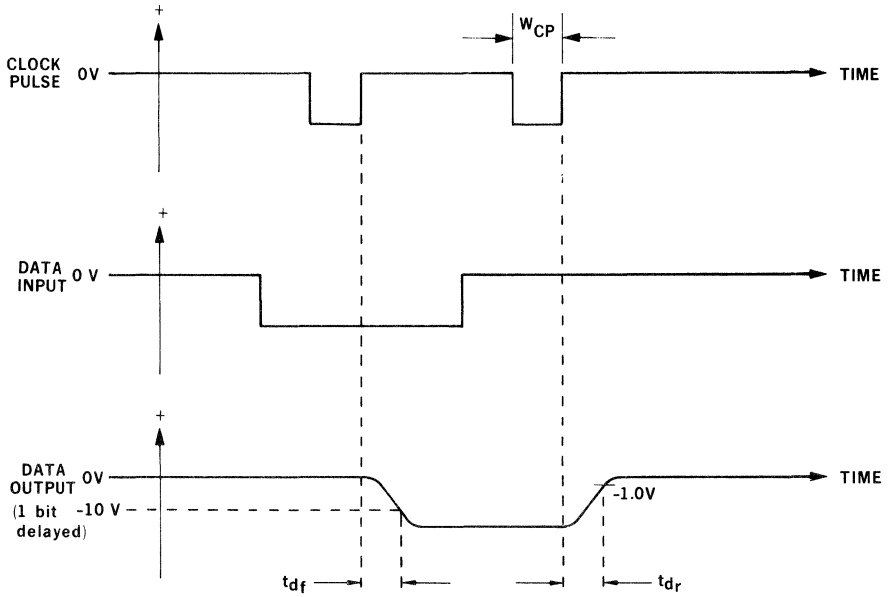


3306 CONNECTION DIAGRAM

TOP VIEW



TIMING DIAGRAM



3320

64 BIT-4Ø-SHIFT REGISTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3320 is a 64 bit dynamic shift register plus logic for loading or recirculating information within the circuit. It is a monolithic integrated circuit utilizing Planar* II, P-channel enhancement mode MOS technology.

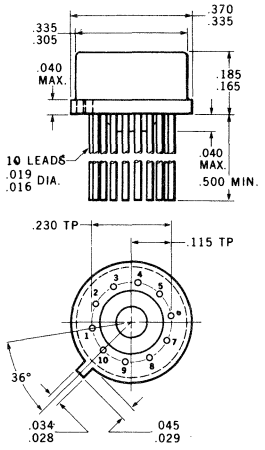
ABSOLUTE MAXIMUM RATINGS

- **CLOCK VOLTAGES (ϕ_1, ϕ_2, ϕ_3, ϕ_4) . . . −30 V to +0.3 V**
- **DATA INPUT AND STORE VOLTAGES . . . −30 V to +0.3 V**
- **STORAGE TEMPERATURE . . . . . −55°C to +150°C**
- **OPERATING TEMPERATURE RANGE . . . −55°C to +85°C**

FEATURES

- **LOW POWER — 200 μW/BIT AT 2.0 MHz**
- **INPUT STORE AND ENTER CONTROL LOGIC**
- **DATA AND DATA COMPLEMENT OUTPUT**
- **INPUT GATE PROTECTION**
- **TYPICALLY 3.0 VOLT NOISE MARGIN**

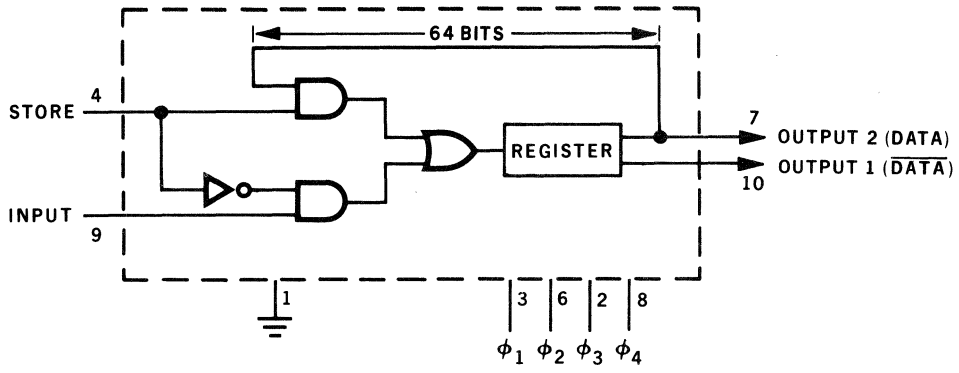
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)

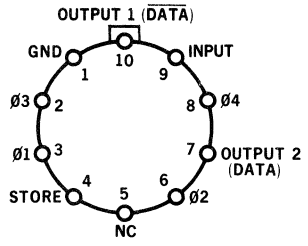


NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO. A5F332014X

CONNECTION DIAGRAM





TOP VIEW

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS Standard Conditions (unless otherwise specified)
Load = 10 MΩ and 10 pF, $T_A = -55°C$ to $+85°C$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Clock Repetition Rate	0.01		2.0	MHz	
	Clock Pulse Width (ϕ_1 & ϕ_3)	100			ns	at −24 Volts } See
	Clock Pulse Width (ϕ_2 & ϕ_4)	200			ns	at −24 Volts } Figure 1
V_{CP}	Clock Logic Levels					
	Logic "0"	+0.3		−1.0	Volts	
	Logic "1"	−24		−27	Volts	
V_{IN}	Data and Store Input Logic Levels					
	Logic "0"	0		−2.0	Volts	
	Logic "1"	−10		−24	Volts	
	Data Input Pulse Width	100			ns	Stable During t_{mp} See Figure 1
	Store Pulse Width	200			ns	Stable During t_{sr} See Figure 1
C_C	Clock Input Capacitance					
	ϕ_1, ϕ_3		15		pF	
	ϕ_2, ϕ_4		10		pF	Plus Output Capacitive Load
C_{IN}	Data and Store Input Capacitance		2.0		pF	
I_{LCP}	Input Leakage to Ground					
	ϕ_1, ϕ_2, ϕ_3, ϕ_4			100	μA	$V_C = -27$ V
I_{LX}	Data and Store Terminals			1.0	μA	$V_{IN} = -20$ V
	Output Logic Levels					
V_{OL}	Logic "0"	0		−2.0	Volts	
V_{OH}	*Logic "1"	−11		−24	Volts	
	Power Per Bit**		0.2		mW	at 2.0 MHz
	Power Per Output Buffer		10		mW	at 2.0 MHz and 10 pF Load

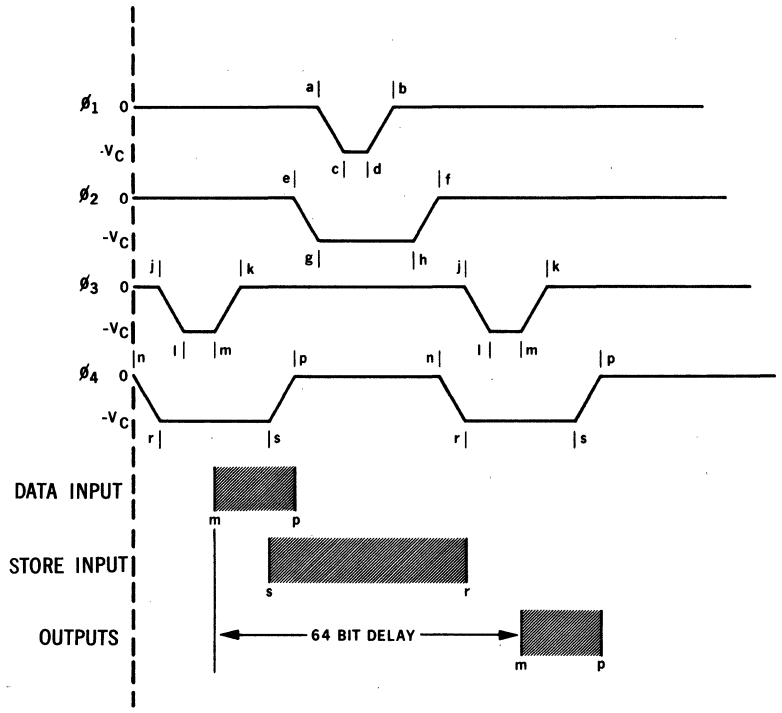
*NOTE: A resistive load to ground will have the effect of discharging the output level (Logic "1") to ground with a time constant equivalent to the RC time constant of the external load.

**NOTE: The power dissipation of each of these stages decreases proportionally with frequency.

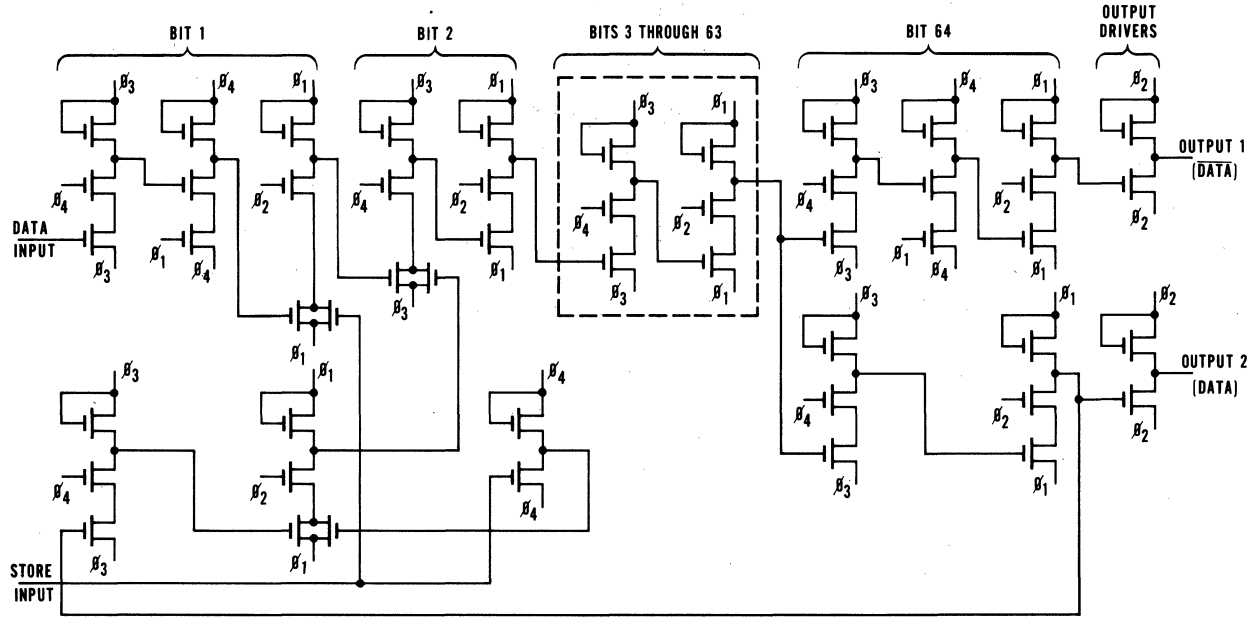
MINIMUM CLOCK REQUIREMENTS

CHARACTERISTIC	SYMBOL	MIN. VALUE (ns)	MAX. VALUE (μs)
ϕ_1 Pulse Width	t_{cd}	100	
ϕ_3 Pulse Width	t_{lm}	100	
ϕ_2 Pulse Width	t_{gh}	200	
ϕ_4 Pulse Width	t_{rs}	200	1.0
Sampling Width 1	t_{bh}	100	
Sampling Width 2	t_{ks}	100	
ϕ_4 - ϕ_1 Overlap	t_{pa}	0	
ϕ_2 - ϕ_3 Overlap	t_{fj}	0	
ϕ_2 - ϕ_4 Overlap	t_{fn}	0	1.0
ϕ_4 - ϕ_2 Overlap	t_{pe}	0	
ϕ_3 Precharge Time	t_{rm}	100	
ϕ_1 Precharge Time	t_{gd}	100	

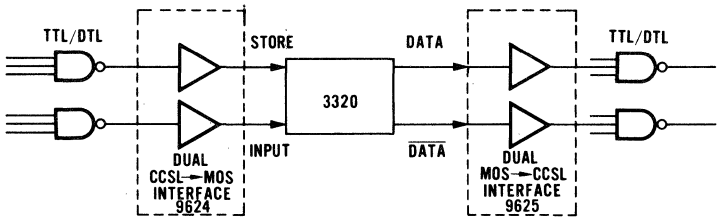
FIG. 1 — TYPICAL WAVEFORMS

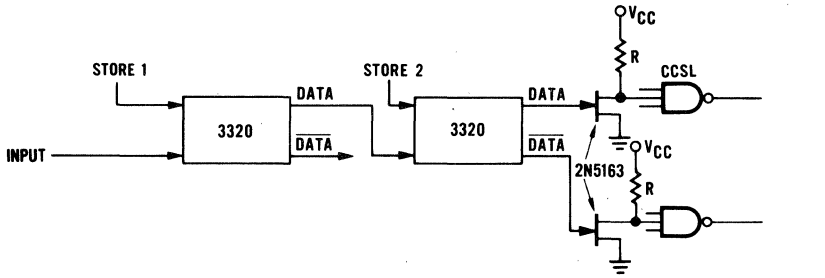


SCHEMATIC DIAGRAM



TYPICAL INTERFACE AND INTERCONNECTION DIAGRAM

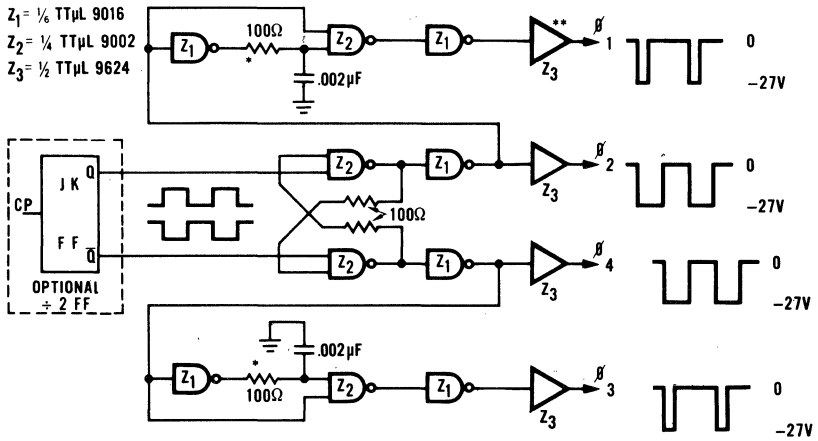




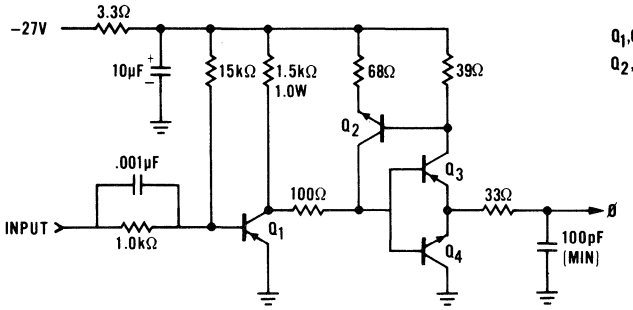
EXTERNAL R≥ 10kΩ
FOR IMPROVED NOISE MARGIN
TO CCSL.

4Ø CLOCK GENERATOR

Z_1= 1/6 TTμL 9016
Z_2= 1/4 TTμL 9002
Z_3= 1/2 TTμL 9624



* PRECHARGE ONE SHOTS WITH R = 100 Ω & C = .002 μF FOR ~ 80 ns PRECHARGE PULSE.



Q_1,Q_3= 2N3644
Q_2,Q_4= 2N3641

**OPTIONAL BIPOLAR TO MOS INTERFACE WHERE HEAVY DRIVE CAPABILITY IS REQUIRED.

3501

1024-BIT STATIC READ-ONLY MEMORY

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3501 is a 1024-bit read-only memory in a 128 word by 8 bit format. It is an MOS monolithic integrated circuit utilizing P-channel enhancement mode technology. The fixed program memory must be specified by the customer and is customized by modifying one mask in the fabrication process. This results in a fast turnaround, low cost custom memory.

FEATURES:

- **CHIP SELECT**
- **ACCESS TIME — 2.5 μs TYP.**
- **STATIC OPERATION**
- **LOW POWER CONSUMPTION — 120 mW TYP.**
- **BIPOLAR COMPATIBLE OUTPUTS**

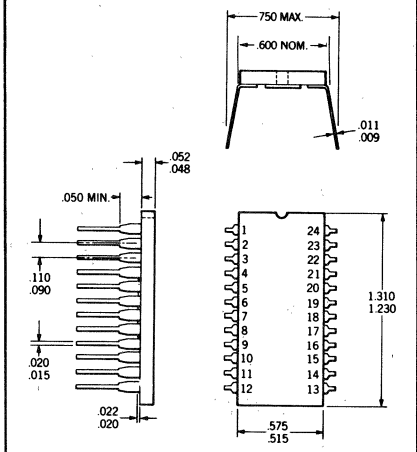
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

All Voltages and Data Input Lines	−30 V to +0.3 V
Power Dissipation	250 mW
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C
	0°C to +70°C

APPLICATIONS:

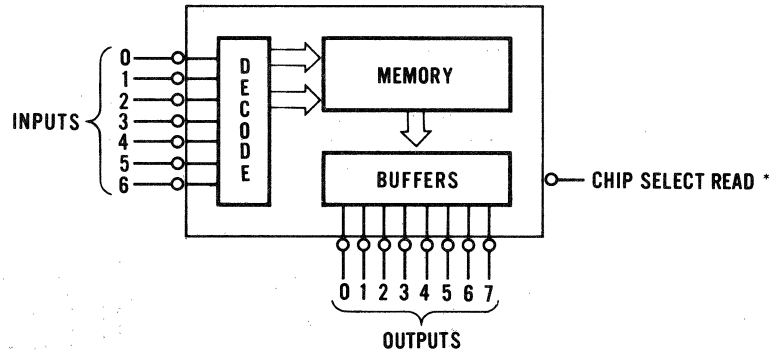
- Micro Programming
- Code Conversion
- Table Lookup
- Control Logic

PHYSICAL DIMENSION



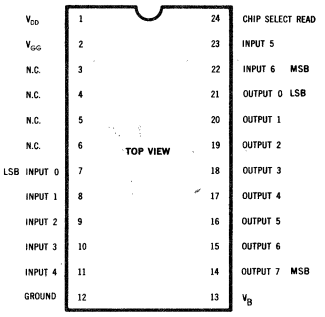
ORDER PART NO. A6G3501X4X (−55°C to +85°C)
A6G3501X9X (0°C to +70°C)

LOGIC DIAGRAM (MIL STD 806B)



*WHEN CHIP SELECT READ IS AT GROUND THE OUTPUTS ARE FLOATING.

PIN CONFIGURATION



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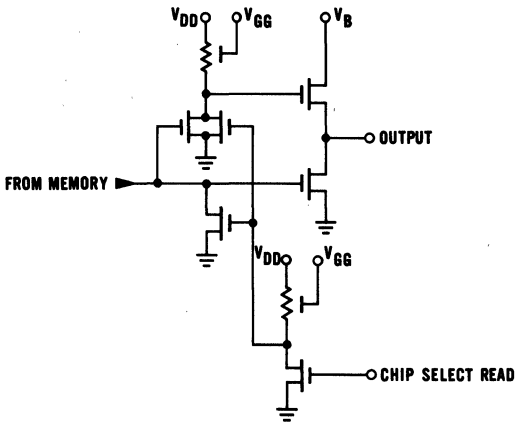
FAIRCHILD MOS INTEGRATED CIRCUIT 3501

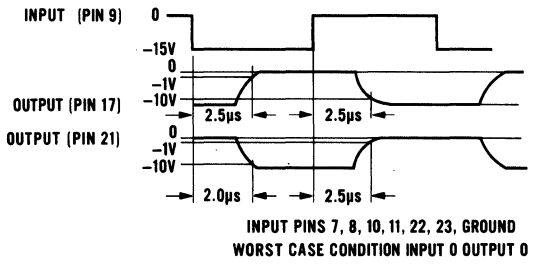
ELECTRICAL CHARACTERISTICS Standard Conditions (unless otherwise specified)
$V_{DD} = -13\,V \pm 1\,V$, $V_{GG} = -27\,V \pm 2\,V$, $V_B = -27\,V \pm 2\,V$
Load 10 MΩ, 10 pF, $T_A = 25°C$

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Logic Levels					
Logic 0	0		−2.0	Volts	
Logic 1	−9.0			Volts	
Output Pulse Delay		2.5	4.0	μs	
Output Logic Levels					
Logic 0	0		−1.0	Volts	
Logic 1	−10			Volts	
Logic 1	−5.0	−7.0		Volts	$R_L = 4.0\,k\Omega$, $V_B = -15\,V$
Output Capacitance		5.0		pF	
Input Capacitance		7.0		pF	
Input Leakage			5.0	μA	$V_{IN} = -20\,V$
Supply Current Drain					
I_{DD}			6.5	mA	
I_{GG}			4.0	mA	
Power Consumption		120		mW	

BUFFER CIRCUIT

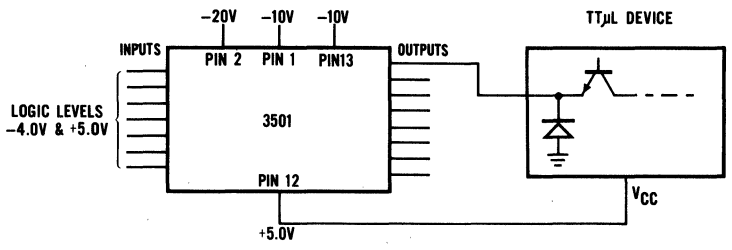


TYPICAL TIMING DIAGRAM



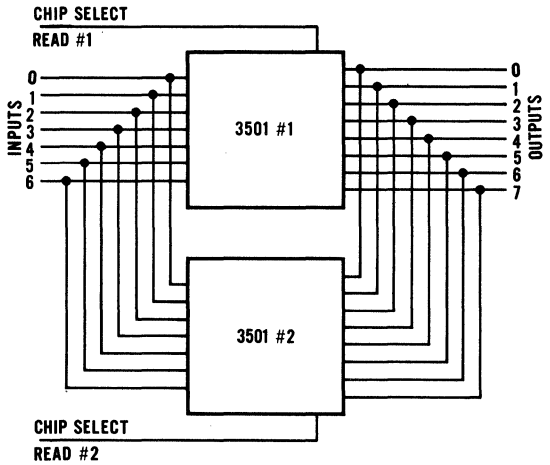
INPUT PINS 7, 8, 10, 11, 22, 23, GROUND
WORST CASE CONDITION INPUT 0 OUTPUT 0

TYPICAL CONNECTION FOR BIPOLAR COMPATIBLE OUTPUT



TYPICAL EXPANDED MEMORY

(CONNECTION FOR 256 WORDS BY 8 BITS)



3530

64-BIT STATIC RANDOM ACCESS MEMORY

MOS/LSI INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3530 is a 64 word by 1 bit Non-Destructive Read Out (NDRO) Static Random Access Memory. It is a P-channel enhancement mode monolithic integrated circuit utilizing Planar II* technology. Bit address is achieved by a 6 line binary decoder included on the chip. Memory system implementation is simplified by providing on chip initiate and chip select control lines for data steering.

FEATURES:

- **LOW POWER CONSUMPTION — 2-3 mW/BIT**
- **COMMON DATA BUSSING — WIRED-OR CAPABILITY**
- **SMALLER SYSTEM SIZE — 16 PIN DIP PACKAGE**
- **SIMPLIFIED SYSTEM DESIGN — ON CHIP CONTROL LOGIC**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

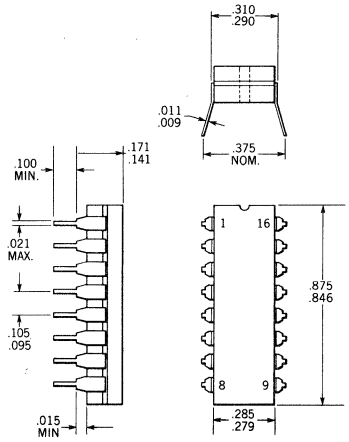
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Voltage on any pin (Pin 8 at GND)	−30 V to +0.3 V
Total power dissipation in package ($T_A = 85°C$)	500 mW

APPLICATIONS:

SCRATCH PAD MEMORY — MOS SYSTEMS
SYSTEM CONTROL
DATA ACCUMULATION
DATA STORAGE

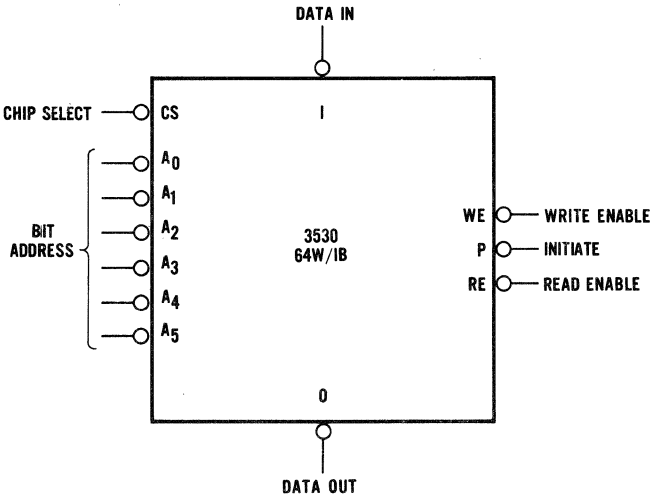
- **CARD READERS**
- **COMPUTER PERIPHERAL EQUIPMENT**
- **AIRBORNE AND MISSILE MEMORY SYSTEMS**
- **DESK CALCULATOR MEMORIES**

PHYSICAL DIMENSIONS
16 Lead Dual In Line

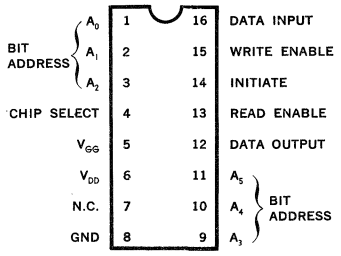


ORDER PART NO. A6J353014X

LOGIC DIAGRAM (MIL STD 806B)



PIN CONFIGURATION



TOP VIEW

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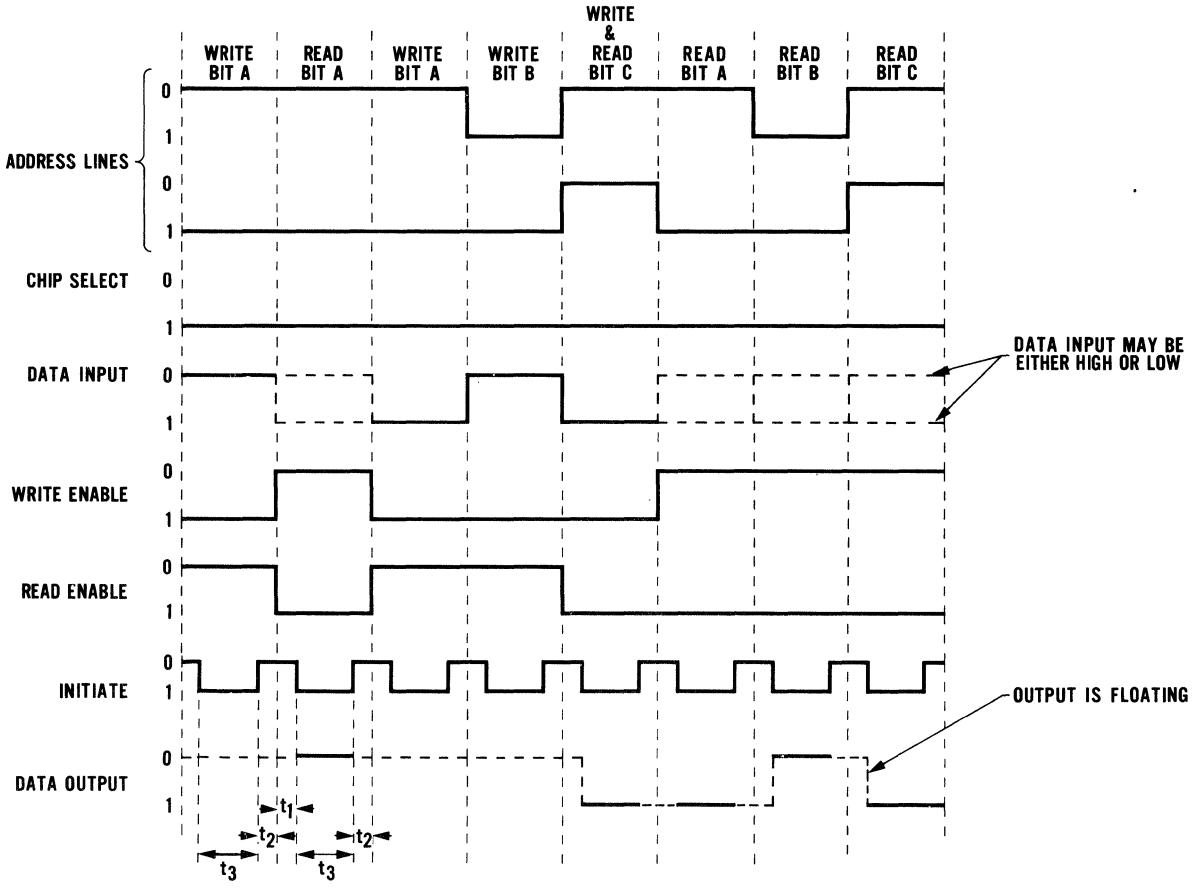
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+85°C$, $V_{DD} = -13$ V ± 2 V, $V_{GG} = -27$ V ± 2V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Input Logic Levels (data and control lines)					
V_{IL}	Logic 0			−2.0	Volts	
V_{IH}	Logic 1	−9.0			Volts	
	Output Logic Levels (data and control lines)					
V_{OL}	Logic 0			−1.0	Volts	$R_L = 10$ MΩ
V_{OH}	Logic 1	−10			Volts	
	Input Leakage (data and control lines)			5.0	μA	$V_{IN} = -15$ V
	Input Capacitance (data and control lines)		5.0		pF	$V_{IN} = 0$ V, f = 1.0 MHz
	Power Supply Current					
I_{DD}	Drain Power Supply Current		7.0		mA	$V_{DD} = -13$ V, $V_{GG} = -27$ V
I_{GG}	Gate Power Supply Current		5.0		mA	$V_{DD} = -13$ V, $V_{GG} = -27$ V
	Power Consumption		225		mW	$V_{DD} = -13$ V, $V_{GG} = -27$ V
Z_{OL}	Output Impedance			2.0	KΩ	$I_{OL} = 100$ μA
	Initiate Pulse Timing					
t_1	See Timing Diagram	0.5			μs	$C_L = 15$ pF
t_2	See Timing Diagram	1.0			μs	$C_L = 15$ pF
t_3	See Timing Diagram	2.0			μs	$C_L = 15$ pF

TIMING DIAGRAM



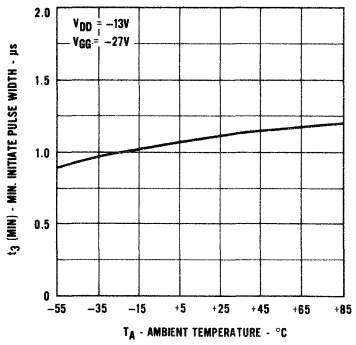
A: The initiate line may function as a chip select if the chip select line is tied permanently to a Logic "1".

B: With the initiate line tied permanently to a Logic "1", the write or read enable line may be used to perform the enable function when they are applied like the initiate line in the above diagram ($t_{3\ MIN}$ usually increases slightly when the memory is operated this way).

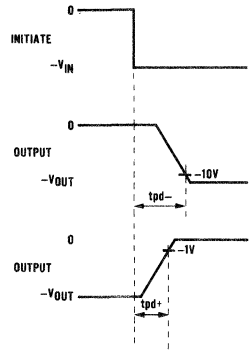
C: t_1, t_2 and t_3 measurements are made from the −3.0 or −8.0 volt levels.

ELECTRICAL CHARACTERISTICS

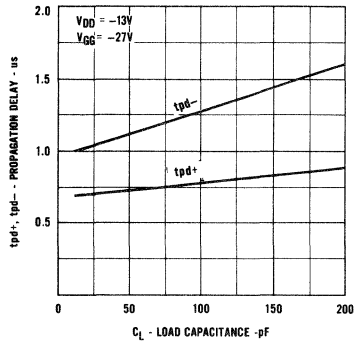
MINIMUM INITIATE PULSE WIDTH VERSUS AMBIENT TEMPERATURE



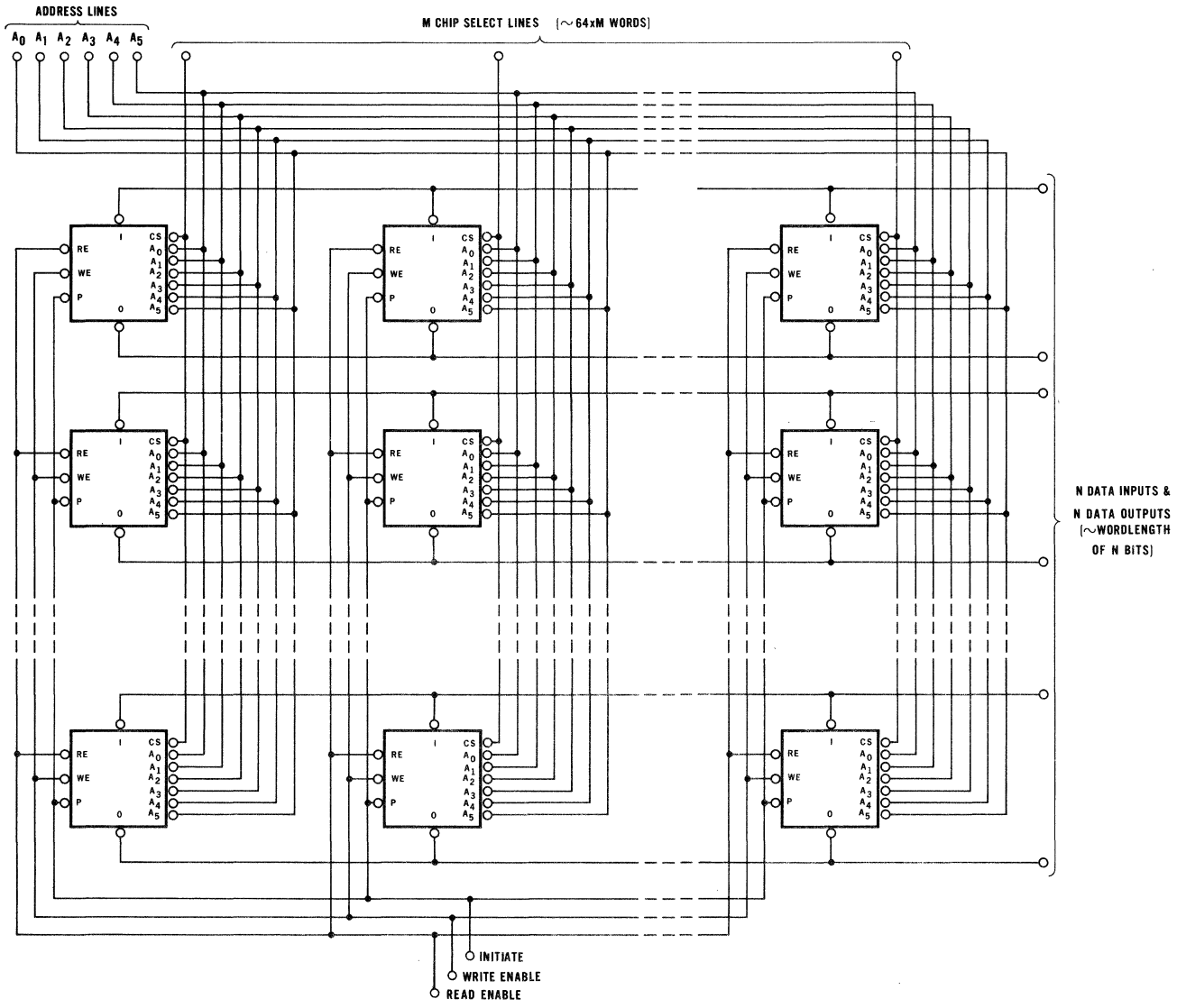
DEFINITION OF PROPAGATION DELAY



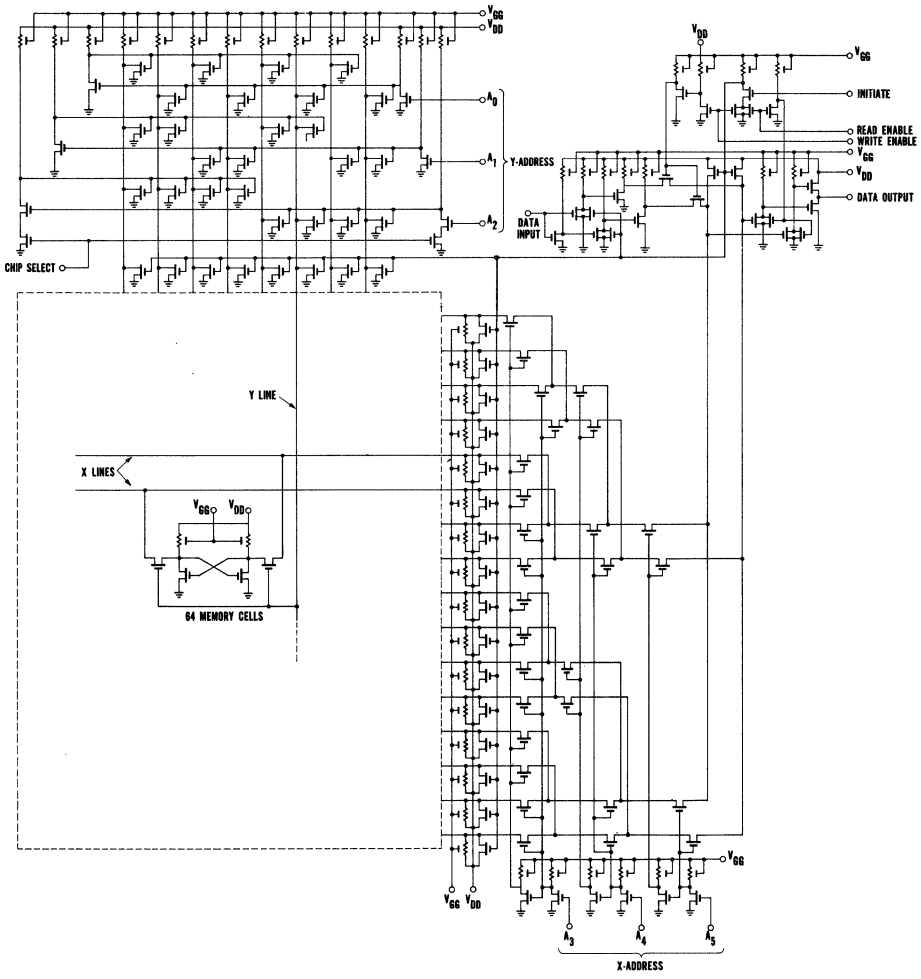
TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE



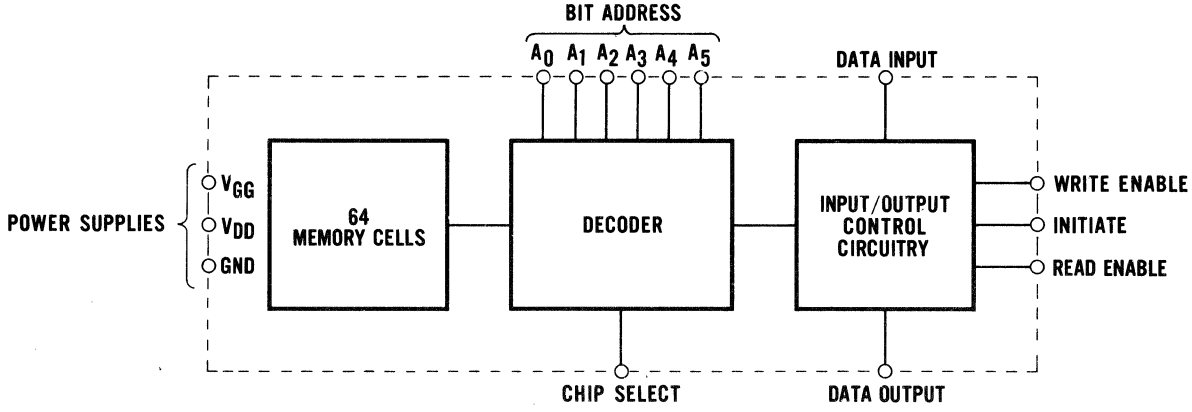
MULTICHIP MEMORY



SCHEMATIC DIAGRAM



BASIC BLOCK DIAGRAM



3700

MOS MONOLITHIC 4 CHANNEL SWITCH

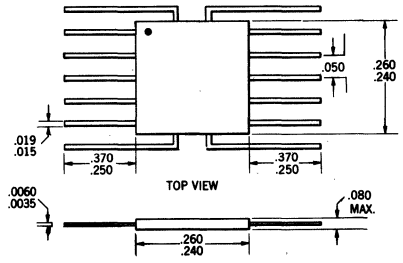
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3700 is a four-channel multiplex switch with all channel blanking. It is a monolithic integrated circuit utilizing Planar* II, P-Channel enhancement mode MOS technology. Control logic has been included on the chip to make the 3700 NPN bipolar compatible. The HLLDTμL 9112 High Level Hex Inverter can be used to directly interface the 3700 with CCSL logic levels. This device is intended for use in A/D Converters, Multiplexing, Analog or Digital Data Transmission Systems, and other airborne or ground instrumentation signal routing applications.

FEATURES:

- **BIPOLAR COMPATIBLE INPUT LOGIC LEVELS**
- **HIGH ON/OFF RATIO**
- **ALL CHANNEL BLANKING CONTROL**
- **PLANAR II STABILITY**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**

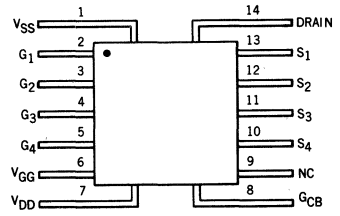
PHYSICAL DIMENSIONS



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature		−65°C to +150°C
Operating Temperature	A3J370011X	−55°C to +125°C
	A3J370019X	0°C to +70°C
Positive Voltage on Any Pin		+0.3 V
Negative Voltage on Digital and Analog Input pins Analog Output pins		−30 V
Negative Voltage on V_{DD} and V_{GG} pins		
	A3J3700112/192	−50 V
	A3J3700113/193	−35 V
Total Power Dissipation in package (T_A = 25°C)		200 mW

PIN CONFIGURATION IN 14 PIN CERPAK II

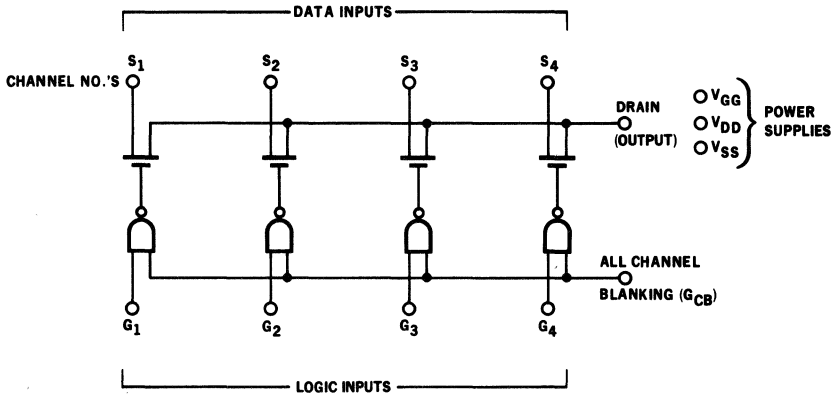


ORDERING INFORMATION — The 3700 is available for use in two signal ranges. (See electrical characteristics for supply voltage requirements.)

+5.0 to −5.0 volts signal applications, Order A3J3700112/192

0 to +5.0 volts signal applications, Order A3J3700113/193

LOGIC DIAGRAM



NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) Voltage ratings are all referenced to pin 1 (V_{SS}).

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
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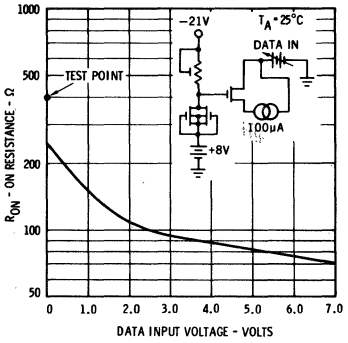
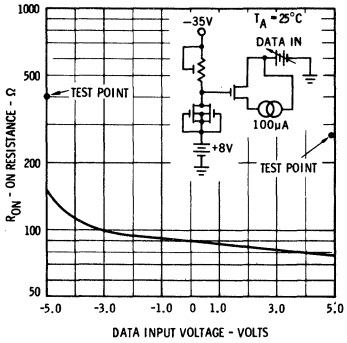
TYPICAL CHARACTERISTICS

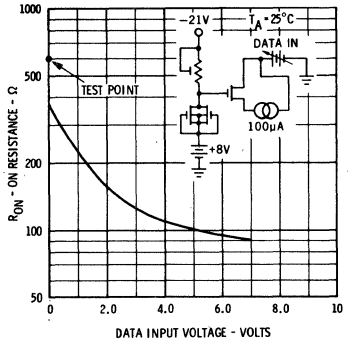
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 113 ONLY)



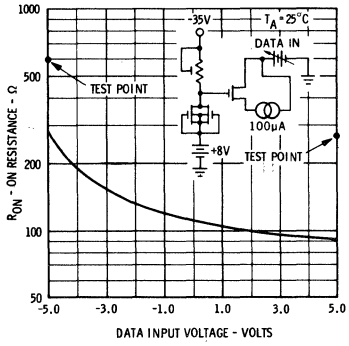
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 112 ONLY)



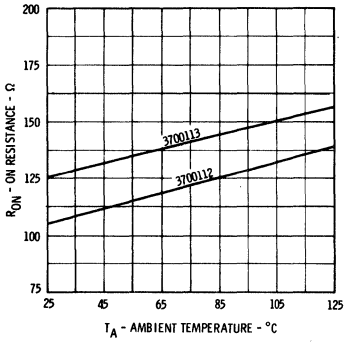
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 193 ONLY)



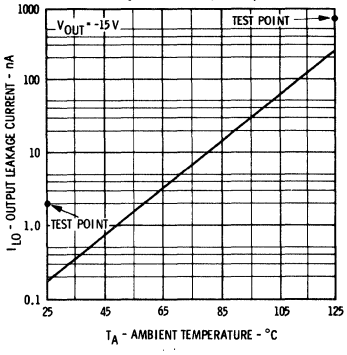
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 192 ONLY)



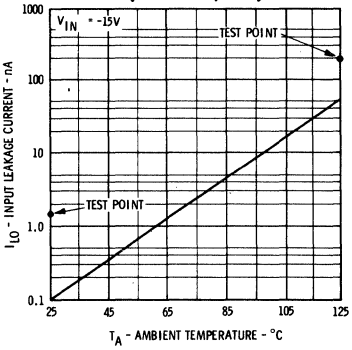
ON RESISTANCE VERSUS AMBIENT TEMPERATURE

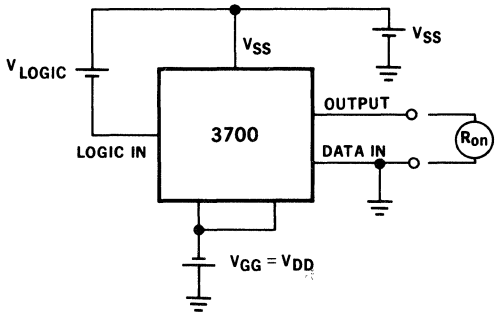


OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE (3700 112/113)



DATA INPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE (3700 112/113)





Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the Substrate (body). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the ON resistance of the data channel accurately, the data input is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

The following sets of bias conditions are equivalent

	Condition 1	Condition 2	Condition 3
Data in	+5.0 V	−3.0 V	0 V
V_{SS}	+8.0 V	0 V	+3.0 V
$V_{DD} = V_{GG}$	−21 V	−29 V	−26 V
Logic in			
1 Level	+7.0 V	−1.0 V	+2.0 V
0 Level	+1.5 V	−6.5 V	−3.5 V

The logic input levels are V_{SS} - 30 V < "0" level < V_{SS} - 7.5 V to turn a data channel off
V_{SS} - 1.5 V < "1" level < V_{SS} to turn a data channel on.

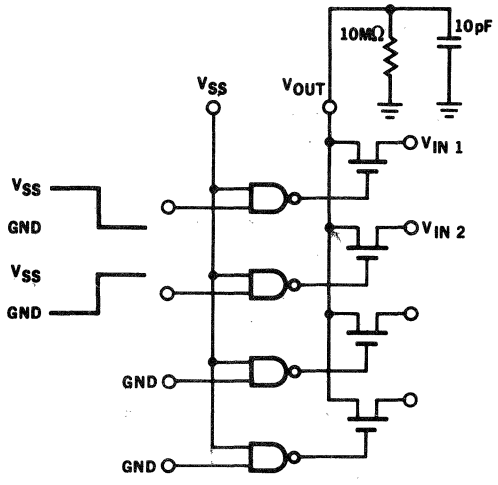
ELECTRICAL CHARACTERISTICS

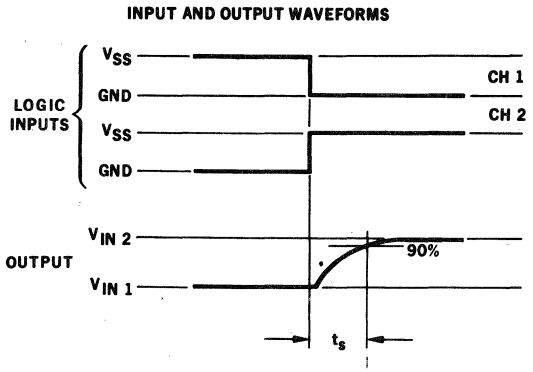
FOR 3700112/192: $-5.0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $V_{DD} = V_{GG} = -35\ V \pm 10\%$, $V_{SS} = +8.0\ V \pm 10\%$ unless otherwise specified.

FOR 3700113/193: $0\ V \leq V_{OUT} \leq +5.0\ V$, $T_A = 25°C$, $V_{DD} = V_{GG} = -21\ V \pm 10\%$, $V_{SS} = +8.0\ V \pm 10\%$ unless otherwise specified.

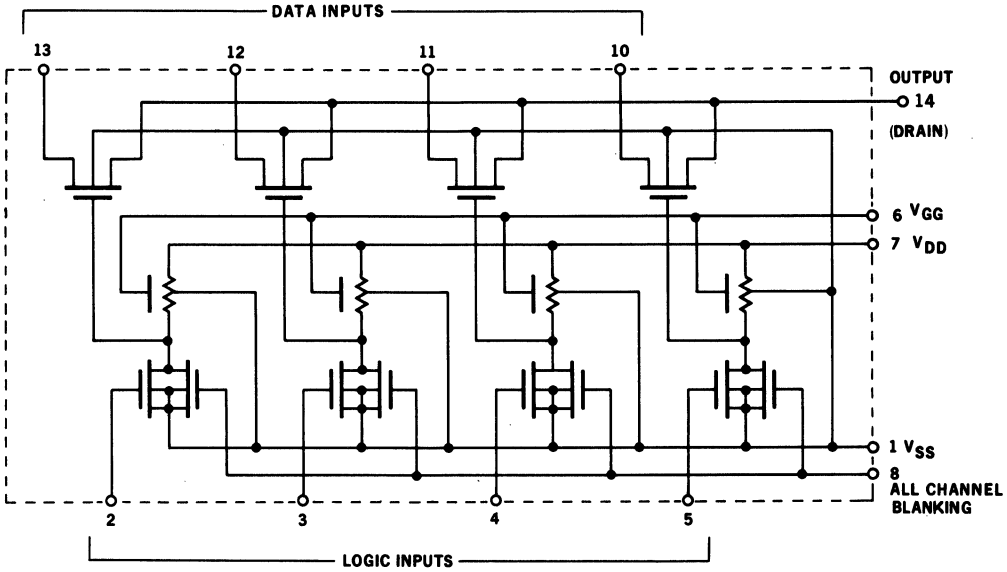
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
R_{ON}	Channel "ON" Resistance			270	Ω	$V_{OUT} = V_{SS}$	$I_{OUT} = -100\ \mu A$
	A3J3700112			400	Ω	$V_{OUT} = -5.0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700113			400	Ω	$V_{OUT} = 0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700192			600	Ω	$V_{OUT} = -5.0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700193			600	Ω	$V_{OUT} = 0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700112 @ +125°C			650	Ω	$V_{OUT} = -5.0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700113 @ +125°C			650	Ω	$V_{OUT} = 0\ V$	$I_{OUT} = -100\ \mu A$
R_{OFF}	Channel "OFF" Resistance	1.5			GΩ	$V_{SS} - V_{OUT} = 15\ V$	$V_G = Gnd$
	A3J3700112/113 @ +125°C	2.1			MΩ	$V_{SS} - V_{OUT} = 15\ V$	$V_G = Gnd$
I_{LO}	Output Leakage Current						
	A3J3700112/113			2.0	nA	$V_{SS} - V_{OUT} = +15\ V$	$V_G = Gnd$
	A3J3700192/193			10	nA	$V_{SS} - V_{OUT} = +15\ V$	$V_G = Gnd$
	A3J3700112/113 @ +125°C			700	nA	$V_{SS} - V_{OUT} = +15\ V$	$V_G = Gnd$
I_{LI}	Data Input Leakage Current			1.5	nA	$V_{SS} - V_{IN} = 15\ V$	$V_G = Gnd$
	A3J3700112/113 @ +125°C			200	nA	$V_{SS} - V_{IN} = 15\ V$	$V_G = Gnd$
V_{IH}	Logic Gate Input "1" Level	$V_{SS} - 1.5$		V_{SS}	V		
V_{IL}	Logic Gate Input "0" Level	$V_{SS} - 7.5$		$V_{SS} - 30$	V		
t_s	Channel Switching Time (see Fig. 1)		1.0		μs		
C_{db}	Output Capacitance		25		pF	$V_{SS} - V_{OUT} = 0\ V$	f = 1.0 MHz
C_{is}	Data Input Capacitance		9.0		pF	$V_{SS} - V_{IN} = 0\ V$	f = 1.0 MHz
C_{ig}	Logic Input Capacitance		3.5		pF	$V_{SS} - V_G = 0\ V$	f = 1.0 MHz
C_{it}	Channel Blanking Input Capacitance		10		pF	$V_{SS} - V_G = 0\ V$	f = 1.0 MHz

FIG. 1
SWITCHING TIME TEST CIRCUIT



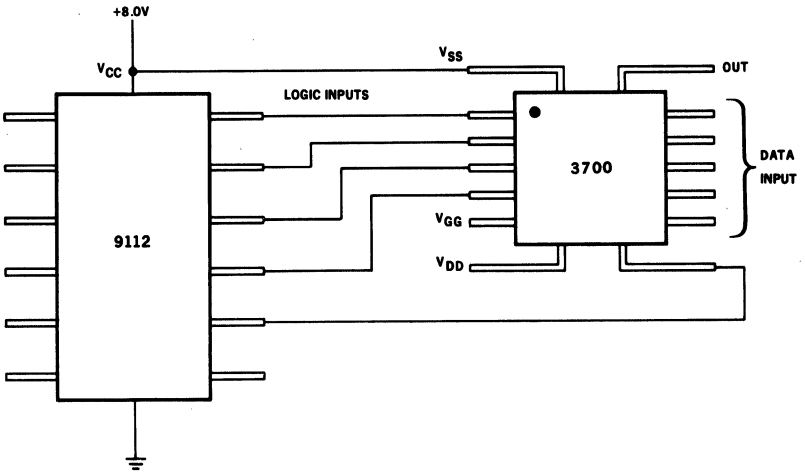


SCHEMATIC DIAGRAM



TYPICAL CIRCUIT CONFIGURATION

Typical circuit configuration showing the 3700 driven by bipolar Diode-Transistor Logic such as the Fairchild HLLDTμL 9112.



3701

MOS MONOLITHIC 6-CHANNEL SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3701 is a P-channel enhancement mode Monolithic MOS six-channel, single output switch. This device can be used as a basic switching element for airborne or ground instrumentation, telemetry or other signal routing applications.

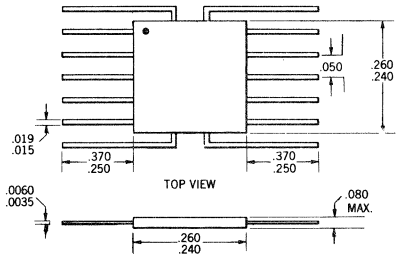
FEATURES

- **GATE PROTECTION**
- **ZERO OFFSET VOLTAGE**
- **LOW LEAKAGE CURRENT**
- **GUARANTEED OPERATIONS OVER —55°C TO +125°C**
- **PLANAR* II STABILITY**

ABSOLUTE MAXIMUM RATINGS (Note 1)

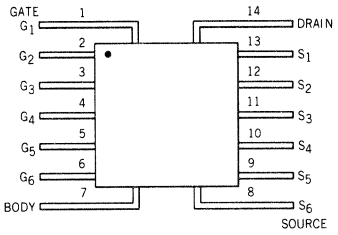
Storage Temperature		—65°C to +150°C
Operating Temperature	A3J370111X	—55°C to +125°C
	A3J370119X	0°C to +70°C
Power Dissipation at +25°C		200 mW
Positive Voltage on any pin ($V_{BODY} = 0$)		+0.3 Volt
Negative Gate Voltage ($V_{BODY} = 0$)		—35 Volts
Negative Source or Drain Voltage ($V_{BODY} = 0$)		—30 Volts

PHYSICAL DIMENSIONS



ORDER PART NO. A3J370111X/19X

PIN CONFIGURATION IN 14 PIN CERPAK II



ELECTRICAL CHARACTERISTICS ($V_{BODY} = 0$ Volt, $T_A = 25°C$ unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Channel "ON" Resistance					
	A3J370111X		210	375	Ω	$V_S = 0$ V, $V_G = -30$ V, $I_D = -100$ μA
	A3J370111X (125°C)		310	550	Ω	$V_S = 0$ V, $V_G = -30$ V, $I_D = -100$ μA
	A3J370119X		300	500	Ω	$V_S = 0$ V, $V_G = -30$ V, $I_D = -100$ μA
R_{OFF}	Channel "OFF" Resistance					
	A3J370111X	10	200		GΩ	$V_D = -20$ V, $V_G = 0$, $V_S = 0$ V
	A3J370111X (125°C)	100	250		MΩ	$V_D = -20$ V, $V_G = 0$, $V_S = 0$ V
	A3J370119X	4.0	200		GΩ	$V_D = -20$ V, $V_G = 0$, $V_S = 0$ V
$V_{GS(TH)}$	Gate Threshold Voltage			—5.5	Volts	$V_S = 0$ V, $V_G = V_D$, $I_D = -10$ μA
I_{SL}	Input Leakage					
	A3J370111X			1.0	nA	$V_S = -20$ V, $V_D = 0$ V, $V_G = 0$ V
	A3J370111X (125°C)			150	nA	$V_S = -20$ V, $V_D = 0$ V, $V_G = 0$ V
	A3J370119X			1.0	nA	$V_S = -20$ V, $V_D = 0$ V, $V_G = 0$ V

*Planar is a patented Fairchild process.

NOTE:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

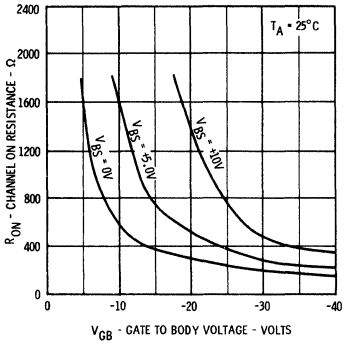
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (V_{BODY} = 0 Volt, T_A = 25°C unless otherwise specified)

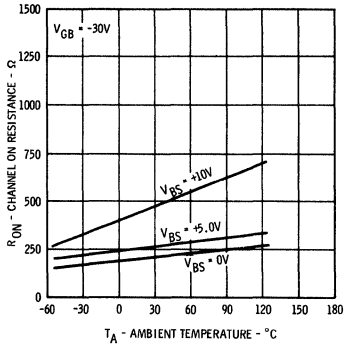
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_{DL}	Output Leakage					
	A3J370111X			2.0	nA	$V_D = -20$ V, $V_S = V_G = 0$ V
	A3J370111X (125°C)			200	nA	$V_D = -20$ V, $V_S = V_G = 0$ V
	A3J370119X			5.0	nA	$V_D = -20$ V, $V_S = V_G = 0$ V
I_{GL}	Gate Leakage			1.0	nA	$V_G = -20$ V, $V_D = V_S = 0$ V
C_S	Input Capacitance		4.0		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V
C_S	Input Capacitance		3.0		pF	$V_S = -10$ V, $V_D = 0$ V, $V_G = 0$ V
C_D	Output Capacitance		13		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V
C_D	Output Capacitance		7.0		pF	$V_S = 0$ V, $V_D = -10$ V, $V_G = 0$ V
C_G	Gate Capacitance		4.0		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V
C_{GS} or C_{GD}	Gate-Source or Gate-Drain Capacitance		1.0		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V

A3J370111X

TYPICAL CHANNEL ON RESISTANCE VERSUS GATE TO BODY VOLTAGE WITH BODY TO SOURCE VOLTAGE AS PARAMETER

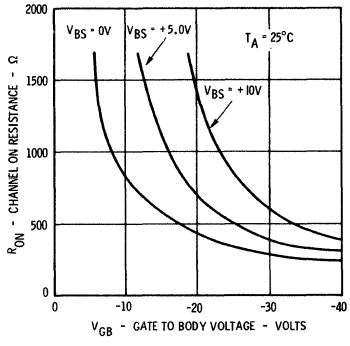


TYPICAL CHANNEL ON RESISTANCE VERSUS AMBIENT TEMPERATURE WITH BODY TO SOURCE VOLTAGE AS PARAMETER

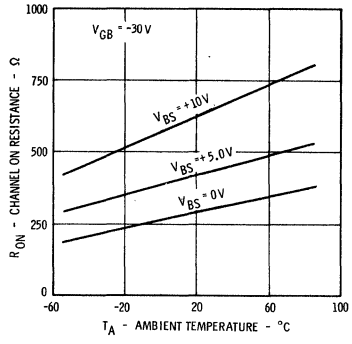


A3J370119X

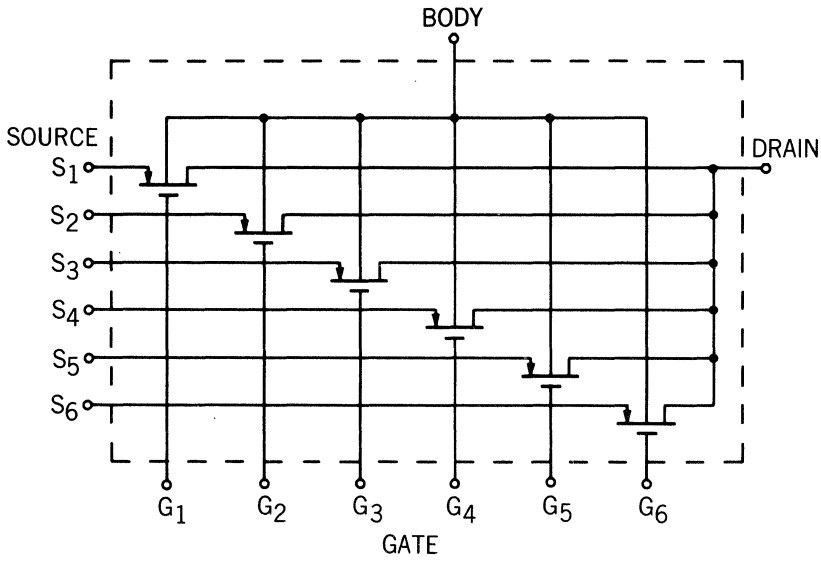
TYPICAL CHANNEL ON RESISTANCE VERSUS GATE TO BODY VOLTAGE WITH BODY TO SOURCE VOLTAGE AS PARAMETER



TYPICAL CHANNEL ON RESISTANCE VERSUS AMBIENT TEMPERATURE WITH BODY TO SOURCE VOLTAGE AS PARAMETER



SCHEMATIC DIAGRAM



3705

MOS MONOLITHIC 8 CHANNEL MULTIPLEX SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3705 is an eight-channel multiplex switch with output enable control and one-out-of-eight decoder included on the chip. It is a monolithic integrated circuit utilizing Planar* II, P-channel enhancement Mode MOS technology. The logic input lines of the 3705 are NPN bipolar compatible and can be used directly with CCSL 5.0 volt logic levels with no level-shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

FEATURES

- **CCSL COMPATIBLE INPUT LOGIC LEVELS**
- **ONE-OUT-OF-EIGHT DECODER ON THE CHIP**
- **HIGH ON/OFF RATIO**
- **OUTPUT ENABLE CONTROL**
- **PLANAR II STABILITY**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**

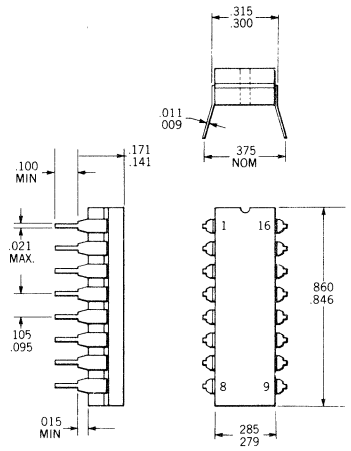
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any pin	+0.3 V
Negative Voltage on digital and analog input pins	−35 V
and analog output pins	−35 V
Negative Voltage on V_{DD} pin	−35 V
Total power dissipation in package ($T_A = 25°C$)	200 mW

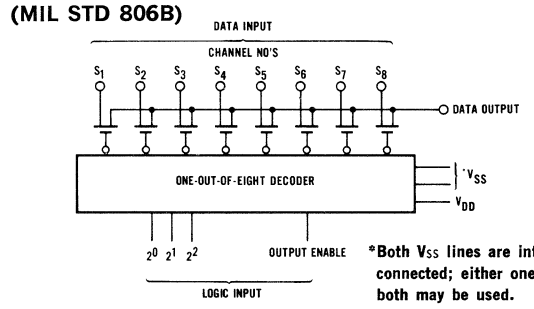
ORDERING INFORMATION — The 3705 is available for use in two signal ranges

−5.0 to +5.0 volts signal applications, Order A6J3705142
0 to +5.0 volts signal applications, Order A6J3705143

PHYSICAL DIMENSIONS
16 Lead Dual In-Line



SYMBOLIC DIAGRAM (MIL STD 806B)

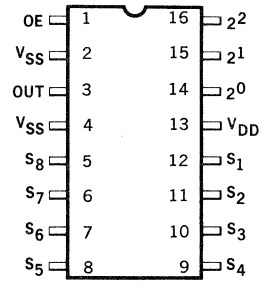


***Both V_{SS} lines are internally connected; either one or both may be used.**

TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

PIN CONFIGURATION
(16 lead DIP)



TOP VIEW

NOTES:

(1) These ratings are limiting values above which the serviceability of the device may be impaired.
(2) Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

*Planar is a patented Fairchild process.

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS

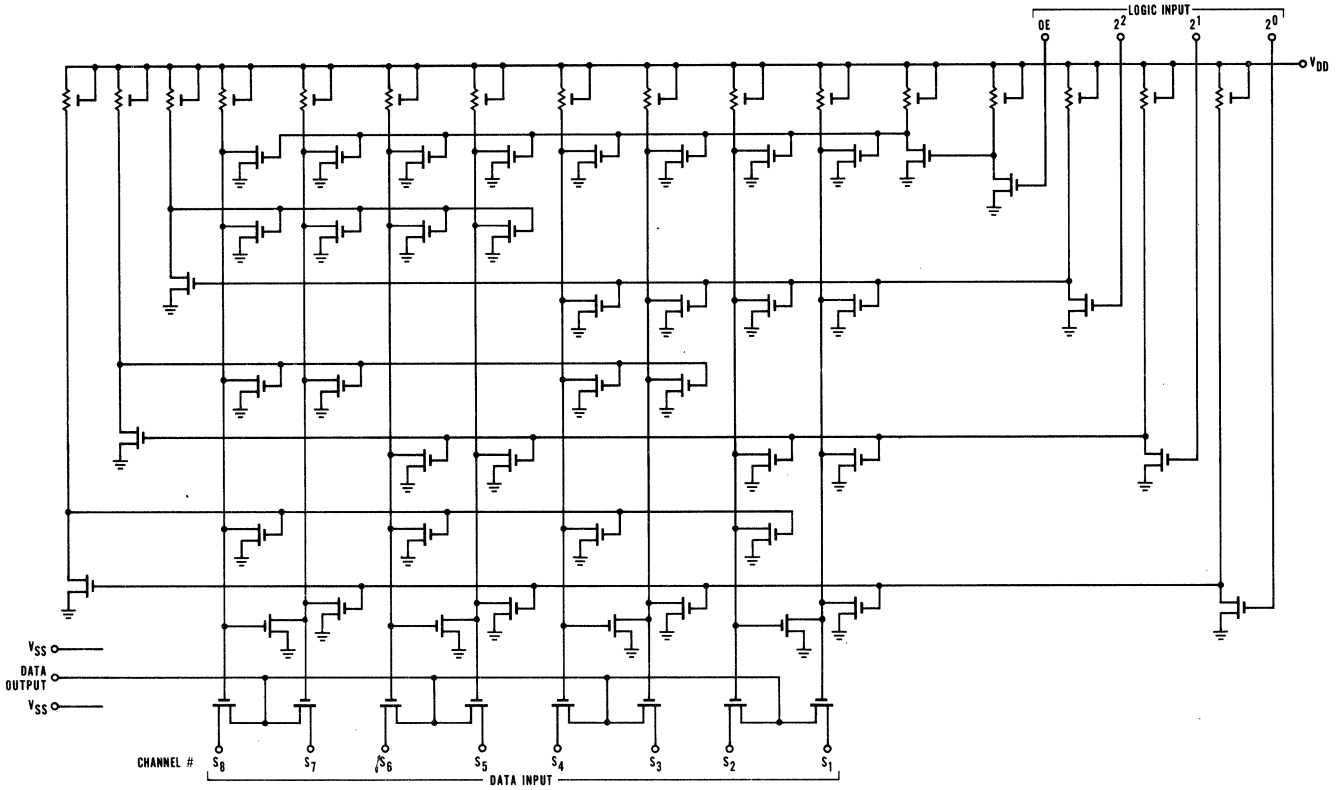
For 3705142: $-5.0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-20\ V < V_{DD} < -24\ V$, $5.0\ V < V_{SS} < 7.0\ V$ unless otherwise specified

For 3705143: $0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-20\ V < V_{DD} < -24\ V$, $5.0\ V < V_{SS} < 7.0\ V$ unless otherwise specified

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Data Channel "ON" Resistance					
	142		250	400	Ω	$V_{OUT} = -5.0\ V$, $I_{OUT} = -100\ \mu A$
	143		190	350	Ω	$V_{OUT} = 0\ V$, $I_{OUT} = -100\ \mu A$
R_{OFF}	Data Channel "OFF" Resistance	1.5			GΩ	$V_{SS} - V_{OUT} = 15\ V$
I_{LO}	Output Leakage Current			10	nA	$V_{SS} - V_{OUT} = 15\ V$
$I_{LO}(85°C)$	Output Leakage Current			500	nA	$V_{SS} - V_{OUT} = 15\ V$
I_{LDI}	Data Input Leakage Current					
	142			3.0	nA	$V_{SS} - V_{IN} = 15\ V$
	143			2.0	nA	$V_{SS} - V_{IN} = 10\ V$
I_{LI}	Logic Input Leakage Current			1.0	μA	$V_{SS} - V_{LOGIC\text{-}IN} = 15\ V$
*V_{IL}	Logic Gate Input "Low" Level	V_{DD}		+0.2	V	
*V_{IH}	Logic Gate Input "High" Level	$V_{SS} - 1.5$		V_{SS}	V	
t_S	Channel Switching Time (See Fig. 1)		1.0		μS	
C_{db}	Output Capacitance		40		pF	$V_{SS} - V_{OUT} = 0\ V$, $f = 1.0\ MHz$
C_{is}	Data Input Capacitance		7.5		pF	$V_{SS} - V_{IN} = 0\ V$, $f = 1.0\ MHz$
C_{ig}	Logic Input Capacitance		5.5		pF	$V_{SS} - V_{LOGIC\text{-}IN} = 0\ V$, $f = 1.0\ MHz$
P_D	Power Dissipation		130	175	mW	$V_{DD} = -31\ V$, $V_{SS} = 0\ V$

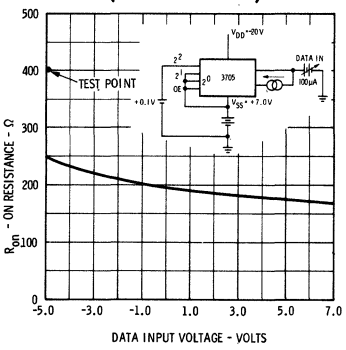
*When driven by CCSL elements, avoid excessive D.C. loading of CCSL elements to insure 3705 logic levels under maximum fan-out conditions.

SCHEMATIC DIAGRAM

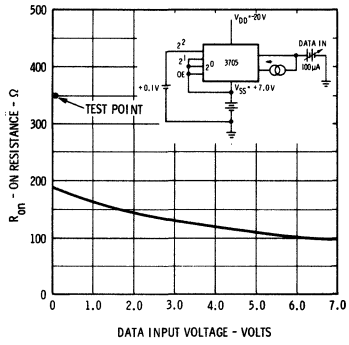


TYPICAL DEVICE CHARACTERISTICS

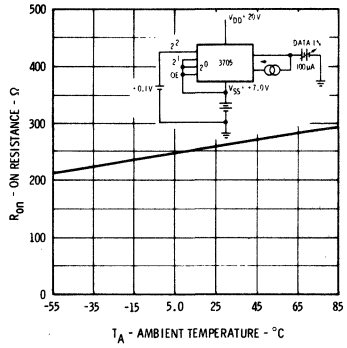
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3705 142 ONLY)



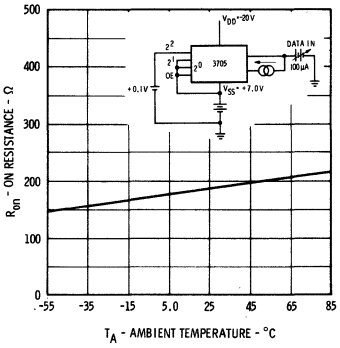
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3705 143 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3705 142 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3705 143 ONLY)



OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE

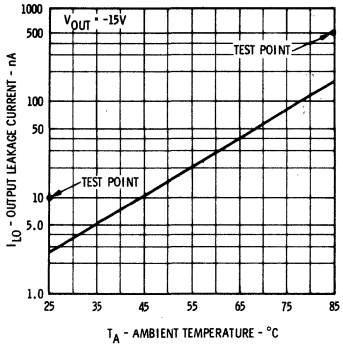
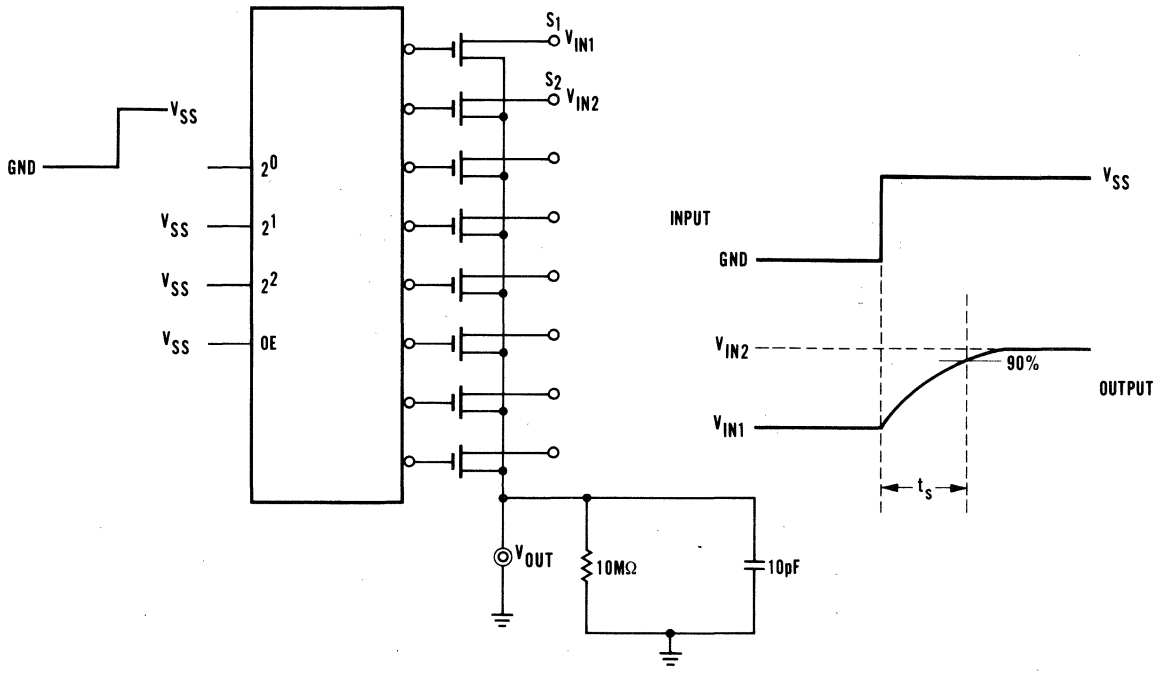
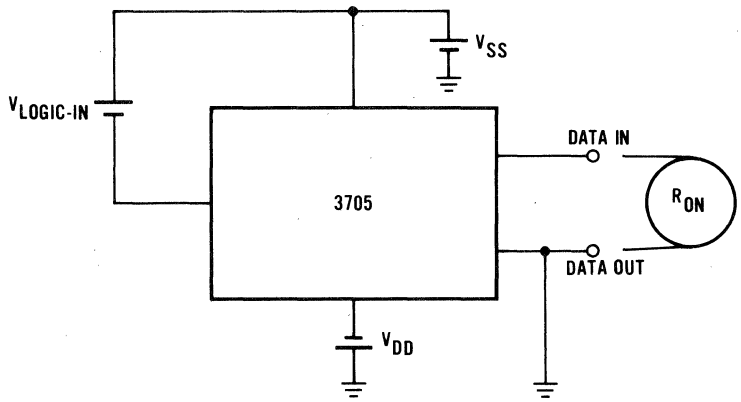


FIG. 1

SWITCHING TIME TEST CIRCUIT



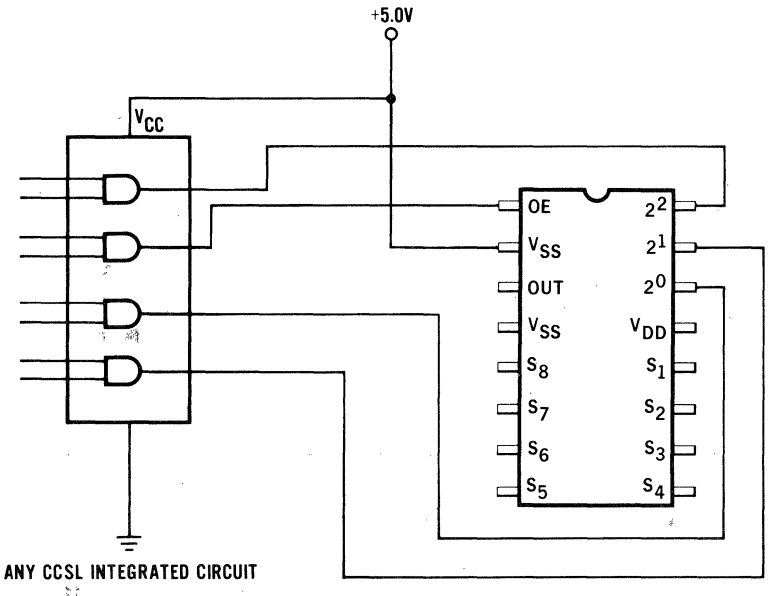


Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body or V_{SS}). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the 'ON' resistance of the data channel accurately, the data output is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

The following sets of bias conditions are equivalent:

	CONDITION 1	CONDITION 2
DATA IN	+5.0 V	0 V
V_{SS}	+7.0 V	+2.0 V
V_{DD}	−20 V	−25 V
LOGIC IN		
"Low" Level	+0.2 V	−4.8 V
"High" Level	+5.5 V	+0.5 V

TYPICAL CONTROL CIRCUIT



3750
10-BIT D/A CONVERTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3750 is a monolithic MOS/LSI ten bit digital to analog converter using P-channel enhancement mode MOS technology. The digital word can be entered serially or in parallel. If desired, the word is available in serial form through an output buffer in either an 8 or 10 bit format. The converter output data is available thru 10 single pole double throw (SPDT) MOS switches. The holding register retains the state of the previous digital input word and drives the output switches. Transfer gates are used to isolate the holding register from the input register while new data is being entered. The 'on' resistance of the MOS switches is weighted to provide the necessary accuracy and stability for a ten bit conversion.

FEATURES

- **8 AND 10 BIT DATA LENGTHS**
- **SERIAL AND PARALLEL OPERATION**
- **250 kHz SERIAL BIT RATE**
- **500 kHz PARALLEL WORD RATE**
- **250 Ω TYPICAL 'ON' RESISTANCE OF TWO MSB's**
- **500 Ω TYPICAL 'ON' RESISTANCE OF REMAINING EIGHT BITS**
- **110 mW POWER DISSIPATION**
- **ZERO AND FULL SCALE CALIBRATION LOGIC**

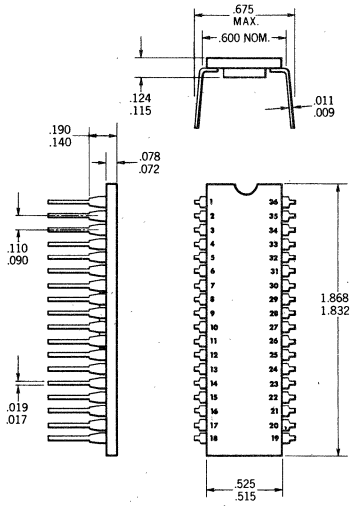
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages	−30 to +0.3 Volts
Power Supply	−29 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature	−55°C to +85°C

APPLICATIONS

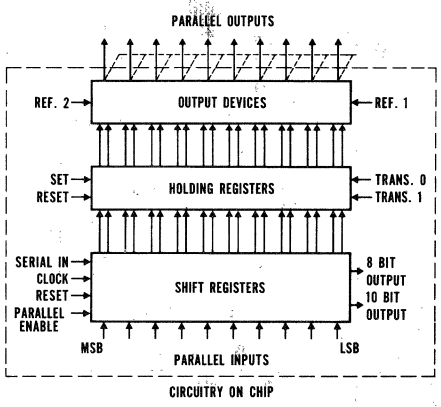
D/A Converters
- Telemetry
- Analog data plotters
- Industrial process control
- Servo systems

PHYSICAL DIMENSION
36 PIN
DUAL IN-LINE PACKAGE

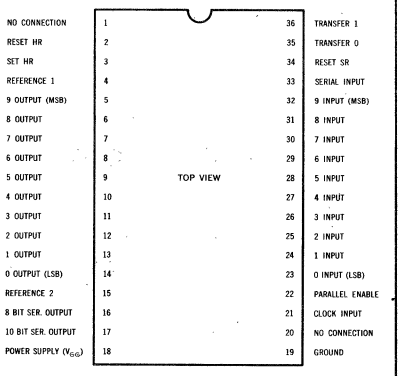


ORDER PART NO. A6H375014X

BLOCK DIAGRAM



PIN CONFIGURATION



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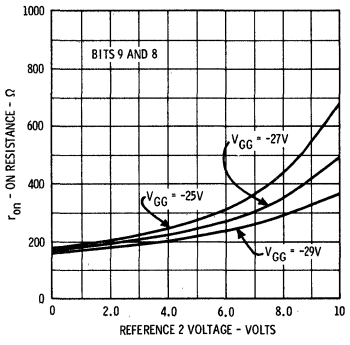
ELECTRICAL CHARACTERISTICS $V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10$ MΩ, $C_L = 10$ pF (unless otherwise specified)

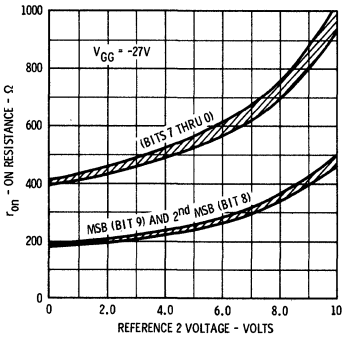
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10		−30	Volts	
	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Frequency					
	Serial	DC		250	kHz	
	Parallel	DC		500	kHz	
r_{on}	MOS Switches					
	"9"	150	250	500	ohms	$V_{REF} = -5.0$ V
	"8"	150	250	500	ohms	$V_{GG} = -27$ V
	"7" thru "0"	325	550	1000	ohms	
Δr_{on}	Switch Mismatch					
	"9"		70	150	ohms	$V_{REF_2} = -5.0$ V
	"8"		70	150	ohms	$V_{REF_1} = 0$ V
	"7" thru "0"		120	250	ohms	
t_{df}	Serial Delay,		0.6		μs	
t_f	rise and fall		0.2		μs	
t_{dr}	times		0.5		μs	
t_r			0.5		μs	
t_{df}	Parallel Delay,		0.55		μs	
t_f	rise and fall		0.35		μs	
t_{dr}	times		0.4		μs	
t_r			0.3		μs	
C_{in}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
	Temperature Coefficient of Switches		0.3		%/°C	
	Temperature Coefficient Tracking		0.03		%/°C	
I_{LX}	Input Leakage Current			5.0	μA	$V_{in} = -20$ V
t_{dd}	Data Delay Time	250			ns	

TYPICAL ELECTRICAL CHARACTERISTICS

ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)

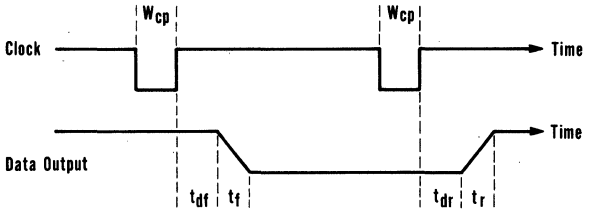


ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)

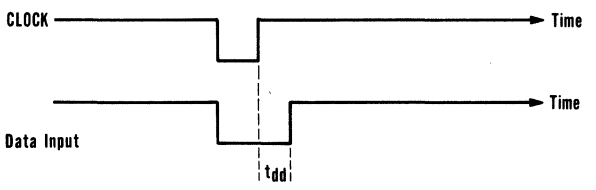


TIMING DIAGRAM

OUTPUT DELAY, RISE AND FALL TIMES

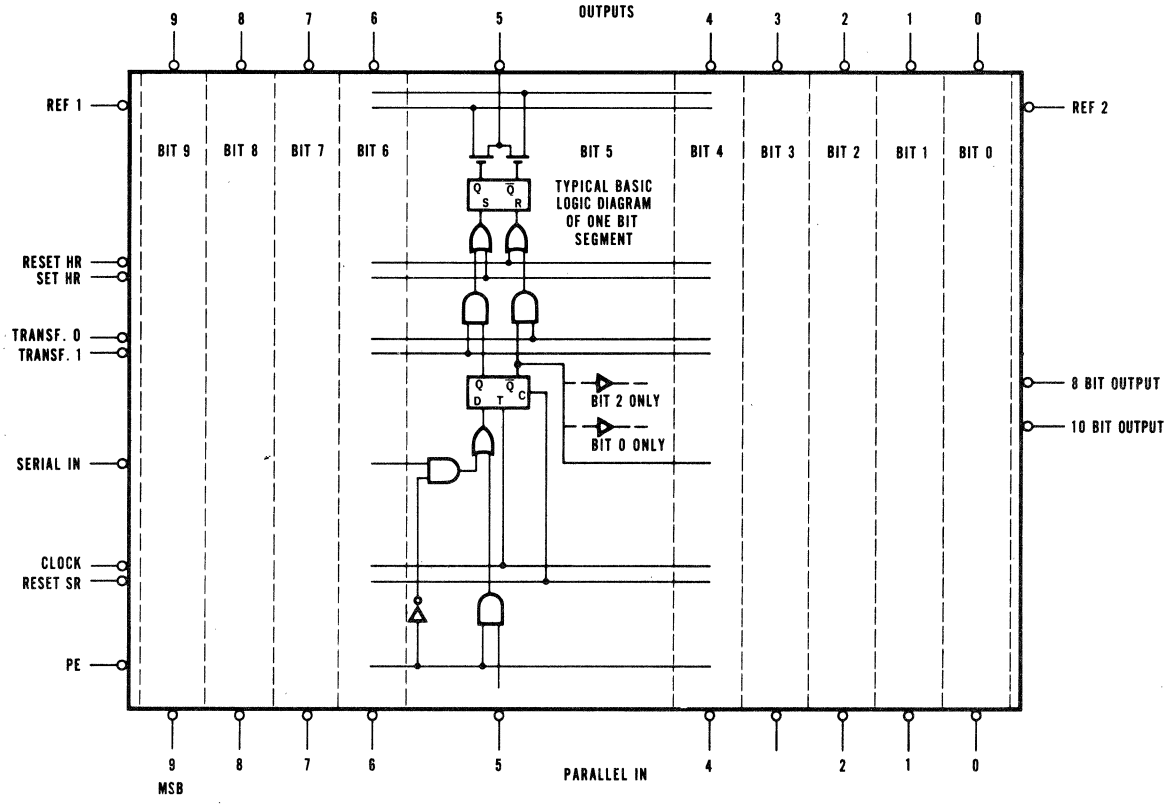


DATA BIT TIMING

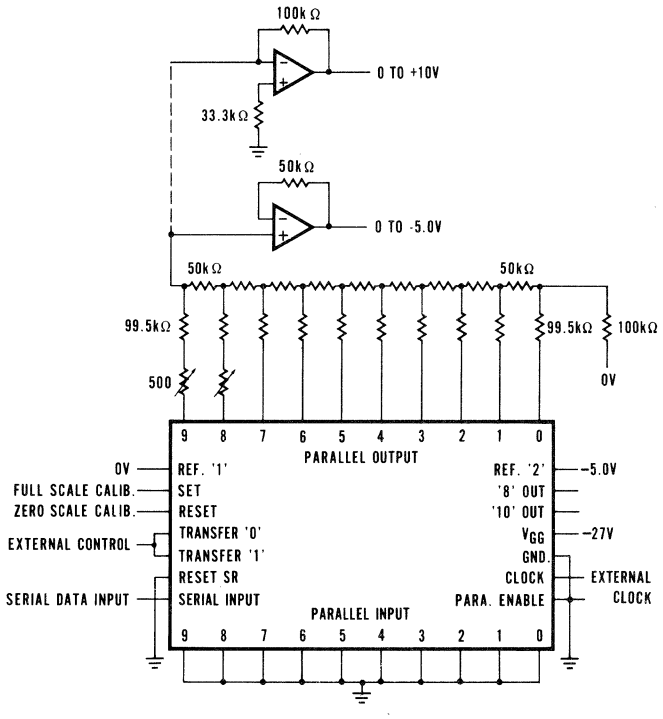


TIMING DIAGRAMS

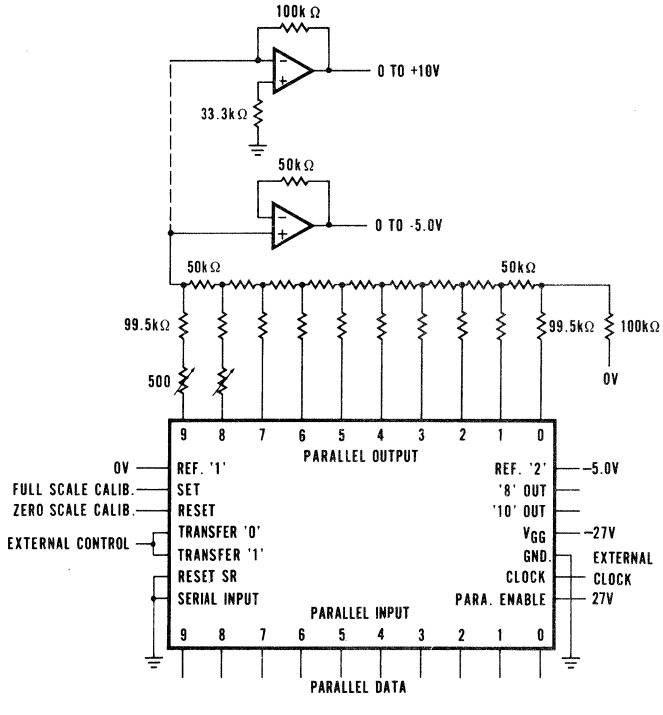
LOGIC DIAGRAM

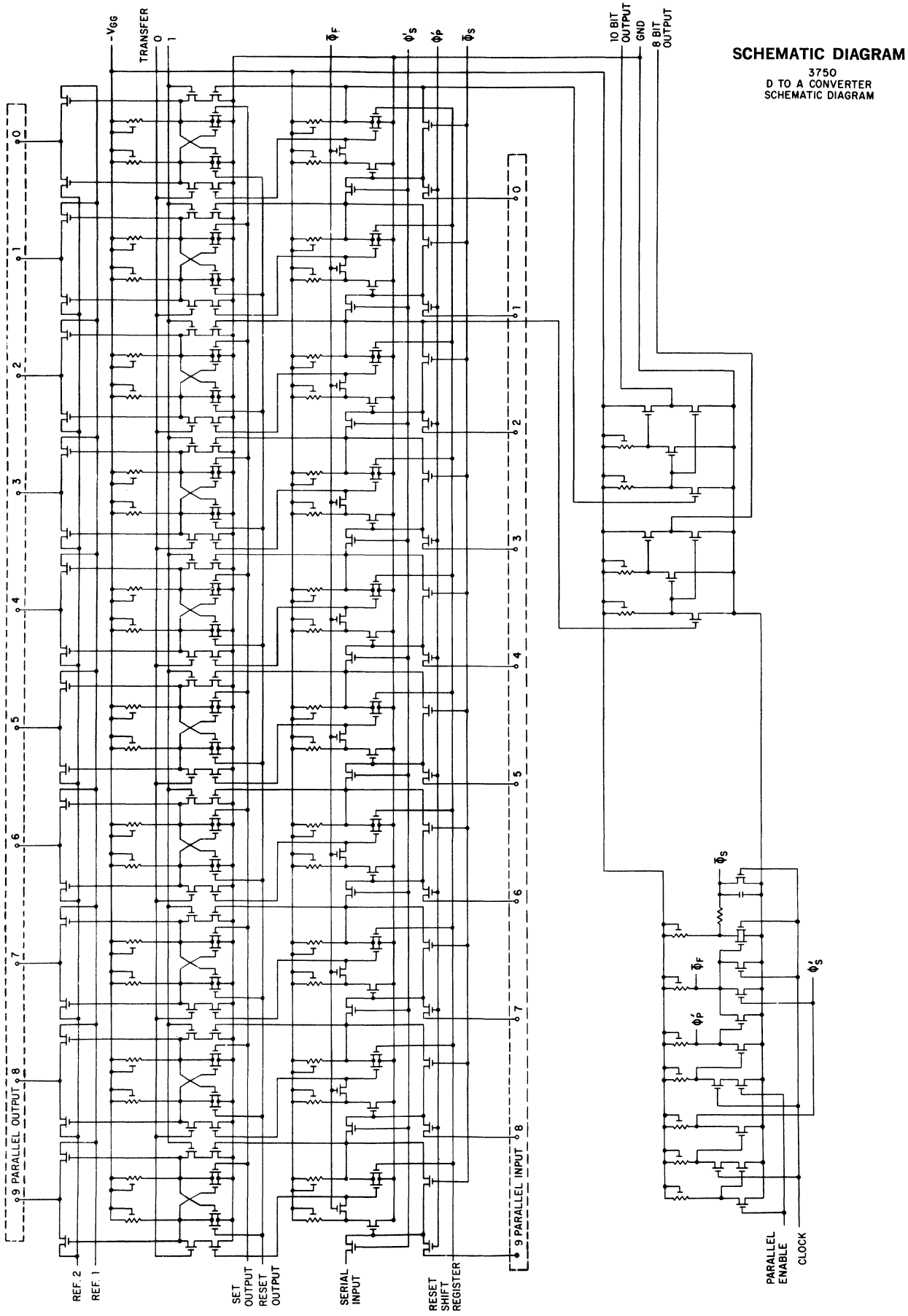


SERIAL OPERATION



PARALLEL OPERATION





SCHEMATIC DIAGRAM

3750
D TO A CONVERTER
SCHEMATIC DIAGRAM

3751
12-BIT A/D CONVERTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3751 is a twelve bit analog to digital converter using P channel enhancement mode MOS/LSI technology. The conversion is accomplished by the successive approximation technique. The word length is variable for eight, nine, ten or twelve bits by applying a DC potential to each of two control pins. The 3751 provides all the A/D system control functions such as: master timing, automatic start and recycle, and RZ or NRZ format control. By choosing the appropriate ladder network, the output will be in either a binary or binary coded decimal digital format.

FEATURES

- **8, 9, 10, OR 12 BIT WORD LENGTH**
- **RZ OR NRZ DIGITAL FORMAT**
- **COMPLETE LOGIC AND SYSTEM TIMING CIRCUITS INCLUDED ON THE CHIP**
- **BCD OVERVOLTAGE FLAG**
- **200 Ω TYPICAL "ON" RESISTANCE FOR THE TWO MSB**
- **500 Ω TYPICAL "ON" RESISTANCE FOR THE REMAINING TEN SWITCHES**
- **150 mW POWER DISSIPATION**
- **AUTOMATIC RESTART CIRCUITS**

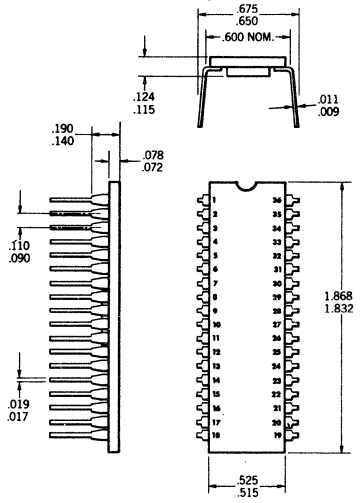
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages	−30 to +0.3 Volts
Power Supply	−30 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature	−55°C to +85°C

APPLICATIONS

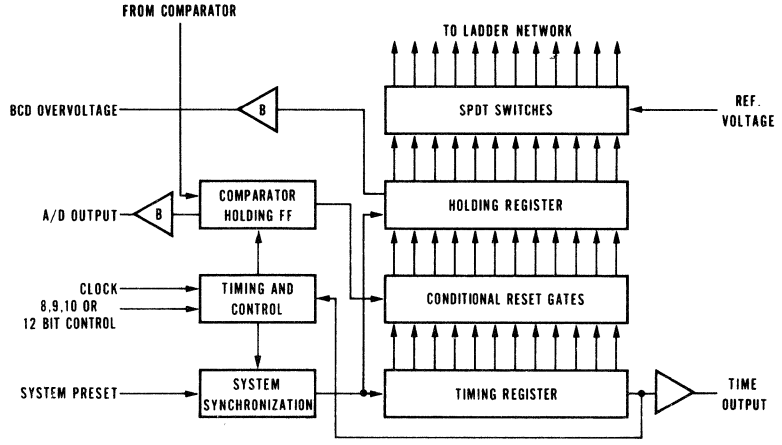
A/D Converters
Three Digit DVM's
Telemetry
Industrial Control
Computer Interface

PHYSICAL DIMENSIONS
36 PIN
DUAL IN-LINE PACKAGE

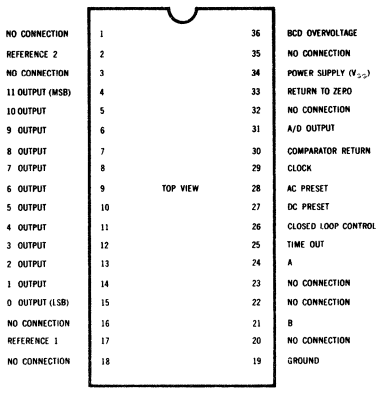


ORDER PART NO. A6H375114X

BLOCK DIAGRAM



PIN CONFIGURATION



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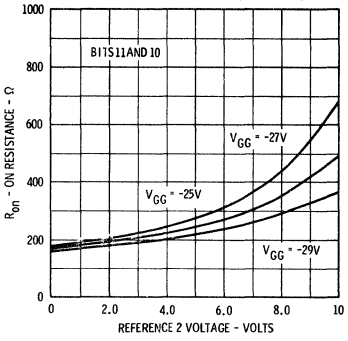
ELECTRICAL CHARACTERISTICS ($V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10$ MΩ, $C_L = 10$ pF unless otherwise specified)

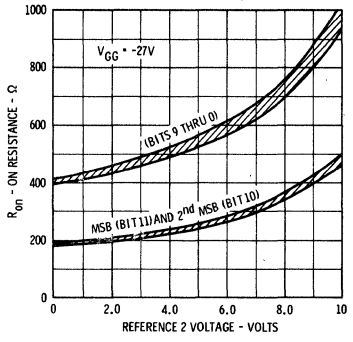
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10		−30	Volts	
W_{cp}	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Bit Frequency	DC		250	kHz	
R_{ON}	MOS Switches					
	"11"	150	250	500	Ω	
	"10"	150	250	500	Ω	
	"9" thru "0"	325	550	1000	Ω	
ΔR_{ON}	Switch Mismatch					
	"11"		70	150	Ω	
	"10"		70	150	Ω	
	"9" thru "0"		120	250	Ω	
C_{IN}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
	Temperature Coefficient of Switches		0.3		%/°C	
	Temperature Coefficient of Tracking		0.03		%/°C	
I_{LX}	Input Leakage Current			5.0	μA	$V_{IN} = -20$ V
	Analog Switch Delay,					
t_{df}	rise and fall times		0.7		μs	
t_f	(10% to 90% points)		0.5		μs	$V_{GG} = -27$ V
t_{dr}			1.1		μs	
t_r			0.25		μs	

TYPICAL ELECTRICAL CHARACTERISTICS

ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)

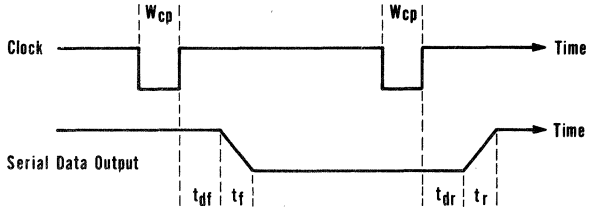


ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)



TIMING DIAGRAM

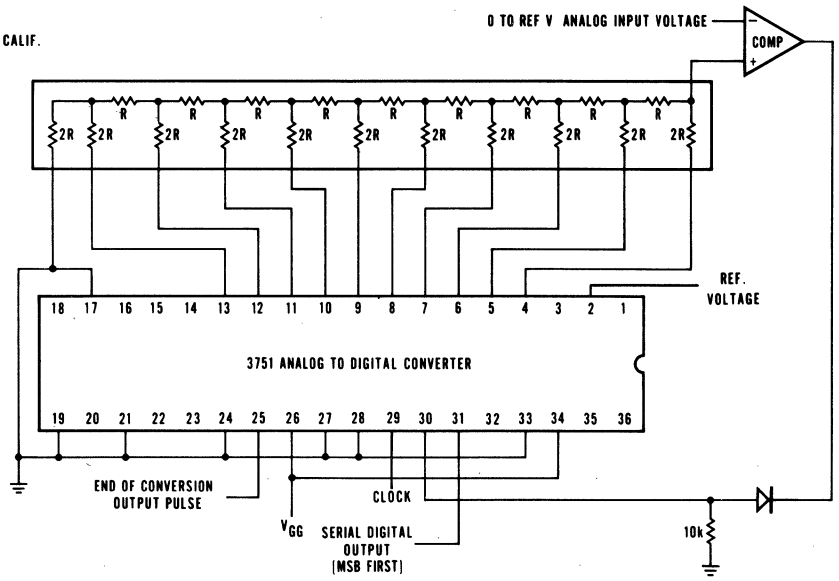
OUTPUT DELAY, RISE AND FALL TIMES



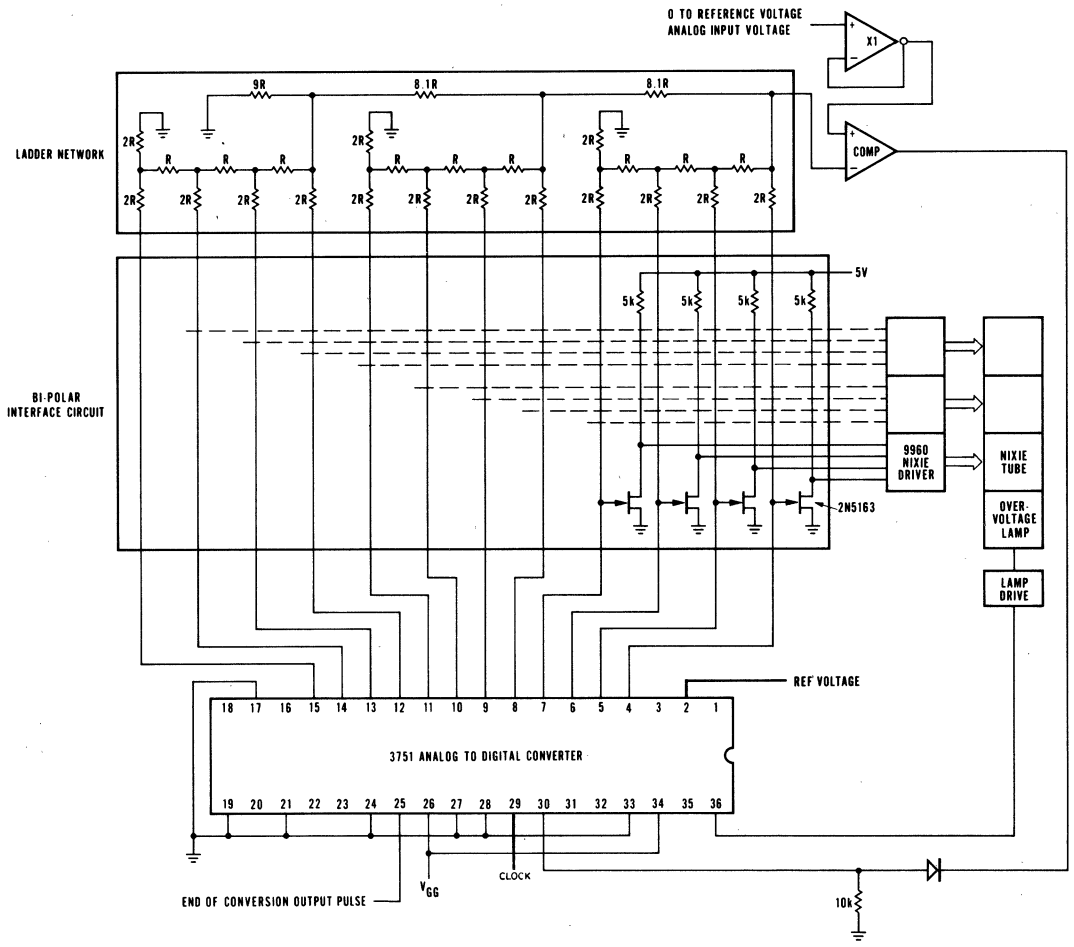
TEN BIT A/D CONVERTER

NO. OF BITS	R VALUE
8	12.5k
9	25k
10	50k
12	200k

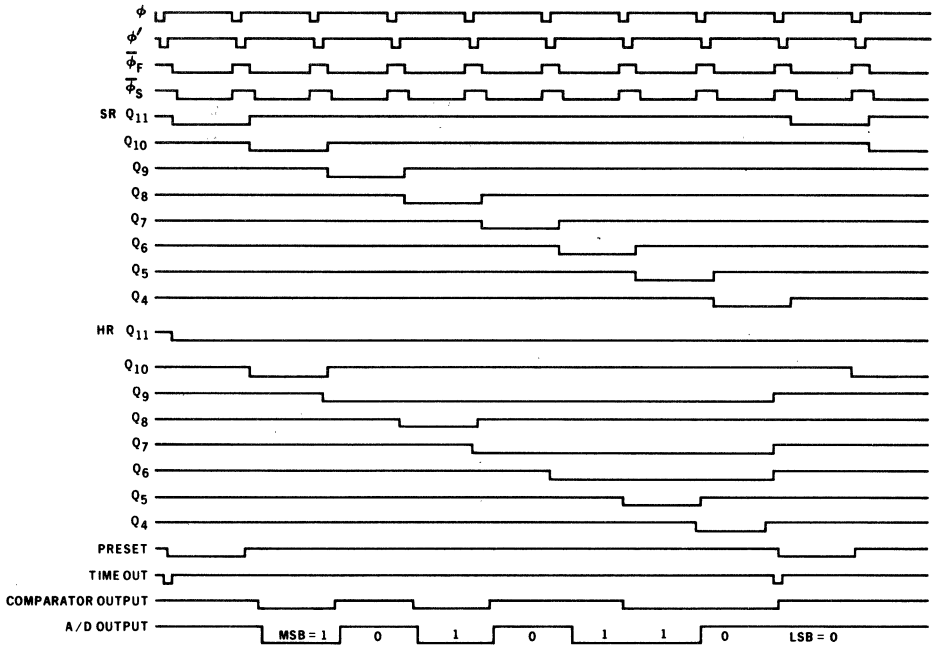
LADDER NETWORK MFGR'S
NEGADYNE CORP., ROCHESTER, N.Y.
ANGSTROM PRECISION INC., VAN NUYS, CALIF.



THREE DIGIT BCD A/D CONVERTER



TYPICAL TIMING DIAGRAM



8 BIT FORMAT
ANALOG INPUT = −3.369 V = 10101100
REFERENCE VOLTAGE = −5.000 V
FIGURE 3

DESCRIPTION OF PIN FUNCTION

PIN NO.

24, 21 A, B: These two pins are connected as shown in the truth table below to control the length of the digital word.

	8	9	10	12
A	1	0	1	0
B	1	1	0	0

25 TIME OUT: A synchronous pulse with the clock is applied at this output at the end of each conversion. This pulse may be used to step a multiplexer or otherwise notify the system of the readiness of the A/D to start another conversion.

26 CLOSED LOOP CONTROL: A '1' voltage level continuously applied to this input will put the A/D in an automatic mode of operation. The time output pulse is internally gated to cause a preset at the end of each conversion and initiate a new conversion. The automatic start circuitry presets the circuit and restarts the conversion if a bit has been dropped in this mode of operation.

27 D.C. PRESET: A '1' voltage level applied to this input will cause an immediate preset and the unit will stay preset until this input is returned to a '0' voltage level.

28 A.C. PRESET: When a '1' level is applied to this input, the A/D is preset on the next clock pulse. The unit will continue to be preset on each clock pulse until the '1' level is removed from the input.

31 A/D OUTPUT: The serial digital conversion is available at this pin in a most significant bit (MSB) first format. The data output is delayed by one bit time.

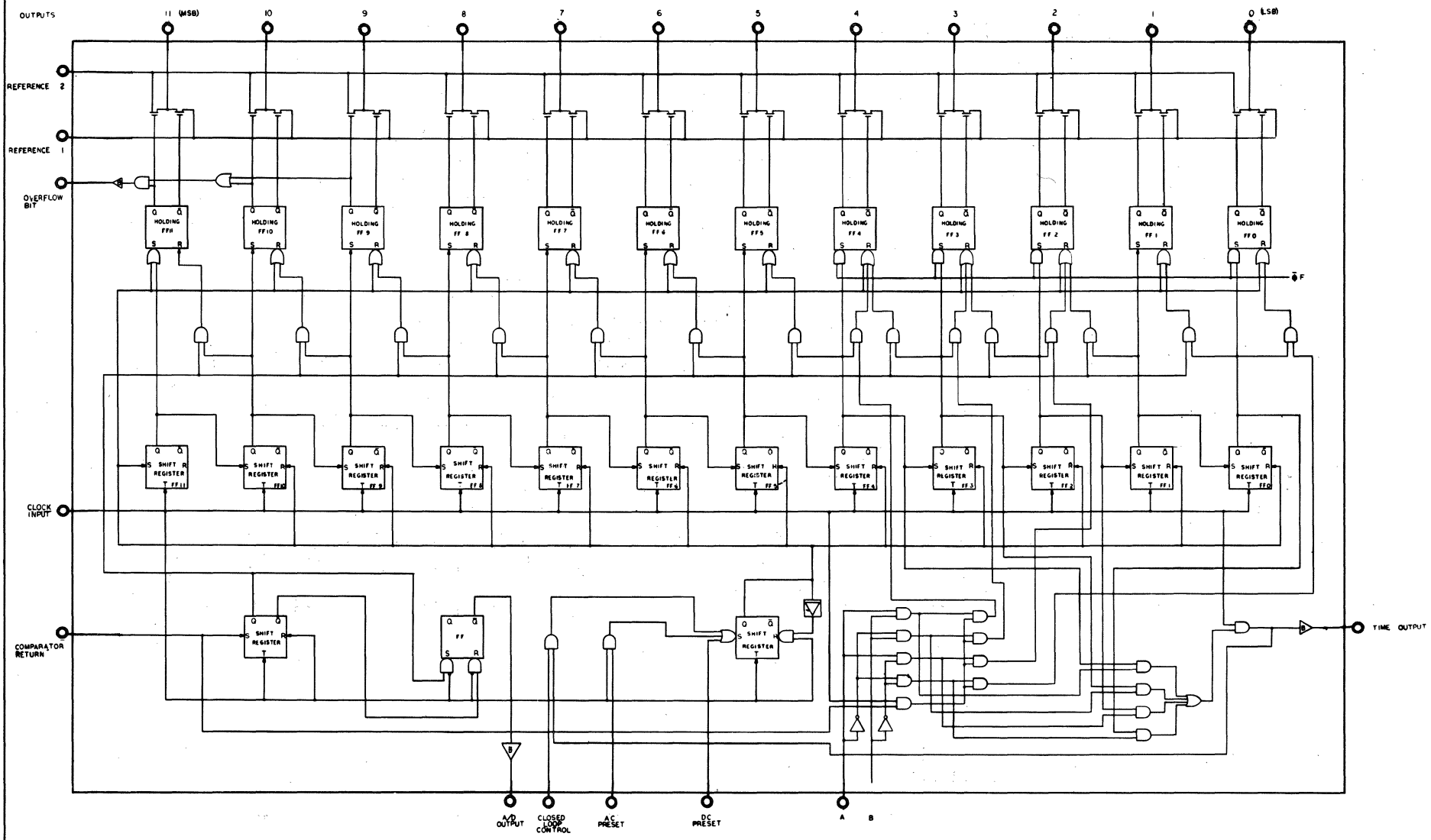
36 BCD OVERVOLTAGE: This output is used when a three digit analog to binary coded decimal (BCD) conversion is being made. If the binary equivalent of the most significant digit is greater than 9, a '1' voltage level is applied on this output.

33 RETURN-TO-ZERO: This input modifies the digital code format from non-return-to-zero (NRZ) to return-to-zero (RZ) if used. When tied to the clock line, the digital output will return to zero during each clock pulse. The RZ duty cycle can be varied by controlling the length of time that a '1' level is applied to this input.

30 COMPARATOR RETURN: The comparator output should be connected to this input. The input must be prevented from going positive with respect to substrate (ground). The output SPDT MOS switches are successively toggled to the reference voltage. This input will cause these switches to be conditionally reset if the ladder network output voltage is greater than the signal voltage.

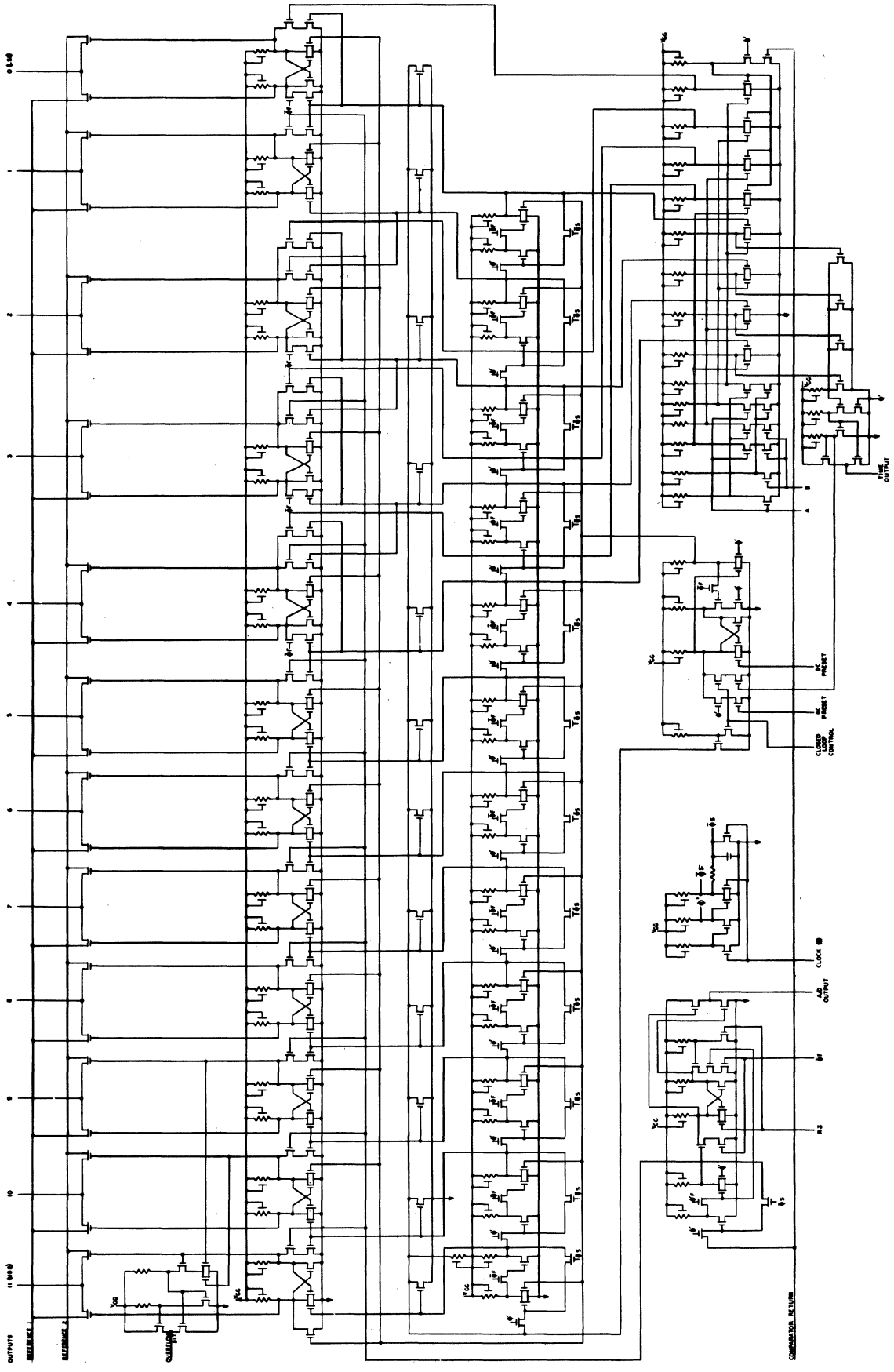
2, 17 REFERENCES 1 & 2: Reference 1 is normally connected to ground and reference 2 to −5.0 volts. However, they may each be connected anywhere between 0 and −5.0 volts D.C. for special applications.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (0) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈ −10 V and 1.0 = "0" ≈ Gnd.

SCHEMATIC DIAGRAM



3800

8-BIT PARALLEL ACCUMULATOR

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3800 is a LSI-MOS integrated circuit containing approximately 200 gates. It functions as an eight bit slice of an arithmetic unit, which may be connected to form any word length. It is capable of parallel addition and subtraction, and by simultaneously shifting the sum or difference right or left, multiplication and division algorithms. A direct subtraction capability eliminates the need for the usual carry input to the LSB during subtraction, thus allowing operands to be located anywhere in the truly variable word length accumulator. The parallel data organization of the 3800 improves speed and greatly reduces the amount of random control logic when compared to the same function performed serially.

FEATURES

- **DIRECT SUBTRACTION USED TO PROVIDE VARIABLE WORD LENGTH CAPABILITY**
- **STROBED OUTPUTS FOR HARD WIRE COMMON BUS SYSTEMS**
- **DC TO 200 kHz ADD AND SHIFT RATE**
- **3.0 μs, 8 STAGE CARRY PROPAGATION TIME**
- **LOW POWER — 180 mW**

APPLICATIONS

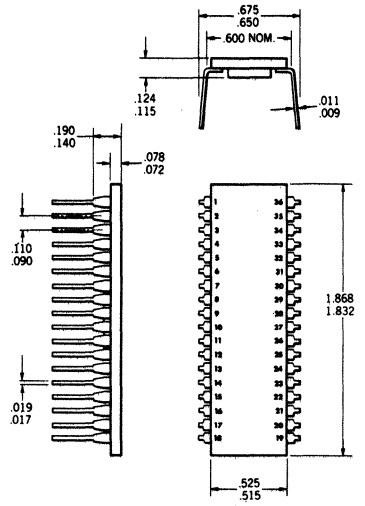
Basic Accumulator Block
Index Register
$>, =, <$ Comparator
General Logic Control
Up-Down Counter
Divide By N Counter

ABSOLUTE MAXIMUM RATINGS

Input Voltages	−30 V to +0.3 V
V_{GG} and V_{DD} Supply Lines	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

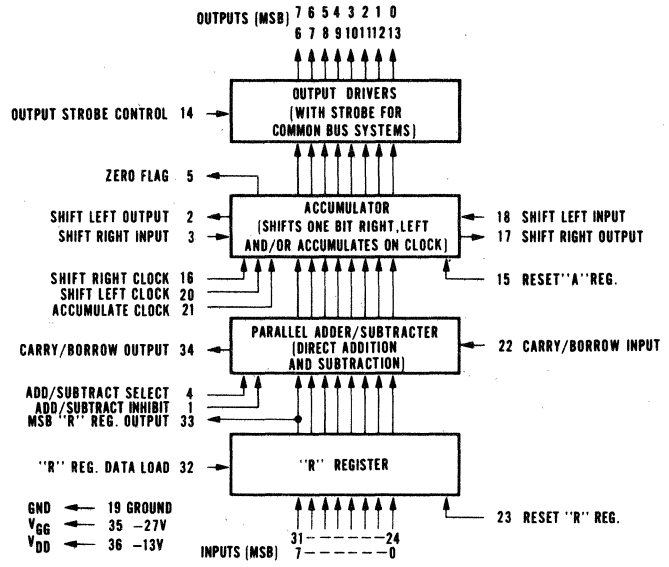
PHYSICAL DIMENSIONS

36-Pin
Dual In-Line Package

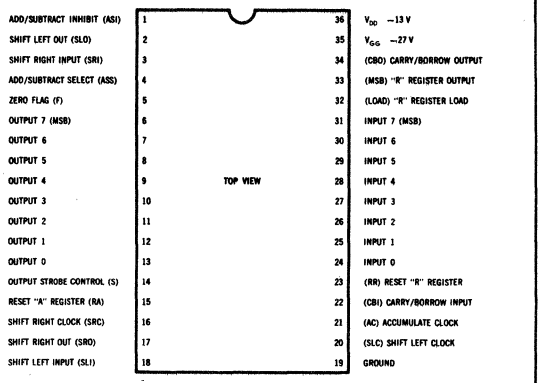


ORDER PART NO. A6H380014X (−55°C to +85°C)
A6H380019X (0°C to 70°C)

BLOCK DIAGRAM



PIN CONFIGURATION



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

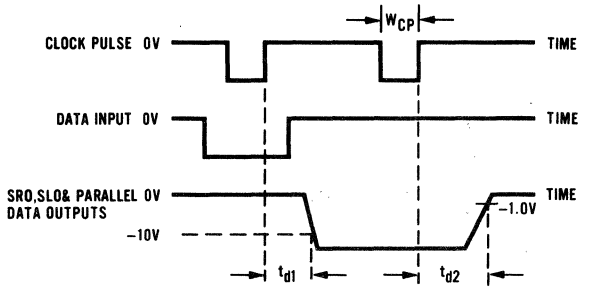
ELECTRICAL CHARACTERISTICS $V_{GG} = -27\ V \pm 1\ V$, $V_{DD} = -13\ V \pm 1\ V$, $R_L = 10\ M\Omega$, $C_L = 10\ pF$ (unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic inputs					
	Logic "0"	0		−2.0	Volts	$V_{GG} = -27\ V$
	Logic "1"	−10		−30	Volts	$V_{GG} = -27\ V$
	Clocks					
	Amplitude	−10		−30	Volts	
	Width	1.0		10	μs	
	Shift frequency	DC		300	kHz	
	Shift & add frequency	DC		200	kHz	
	Delay Times					
t_{CB}	8 stage carry		3.0	5.0	μs	See Figure 1
t_{d1} & t_{d2}	Output delay		1.0	3.0	μs	See Figure 1
I_{LX}	Input leakage current			5.0	μA	$V_{IN} = -20\ V$
	Logic outputs					
	Logic "0"	0	−0.5	−1.0	Volts	
	Logic "1"	−11	−12		Volts	
	Logic "1"	−10	−11		Volts	$R_L = 40\ k\Omega$
	Supply current drain					
	V_{DD}			7.0	mA	$V_{GG} = -27\ V$, $V_{DD} = -13\ V$
	V_{GG}			5.0	mA	$V_{GG} = -27\ V$, $V_{DD} = -13\ V$
	Network dissipation		180		mW	

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Add/subtract inhibit	ASI	When ASI is a logic "1", no addition or subtraction will occur when the ACC, SRC or SLC clock are pulsed. The accumulator register will shift right or left normally however. The carry/borrow through line is not affected, allowing numbers to be shifted and compared when the subtract mode is selected.
2	Shift left output	SLO	SLO is the MSB output of the ACC and may be connected directly to the SLI input of the next eight bit section of the accumulator. Shift and add function normally.
3	Shift right input	SRI	SRI accepts the SRO output of a higher order, 8 bit slice. Shift and add function normally.
4	Add/Subtract select	ASS	When ASS is a logic "1", addition is performed, and when ASS is a logic "0", subtraction is performed.
5	Zero flag	F	The zero flag output is a logic "1" only if the accumulator register contains all zeros. This output is independent of the strobe control.
6-13	Outputs	7-0	When the strobe control STR is a logic "0", all outputs represent the contents of the accumulator register.
14	Output strobe control	STR	When STR is a logic "1", all parallel outputs, 0-7, are disconnected from the power and ground lines allowing them to float. Thus several similar outputs may be hard wired together for a common buss system.
15	Reset Accum. register	RA	When RA = logic "1", the accumulator is reset to zero. This asynchronous signal overrides all others.
16	Shift right clock	SRC	Pulsing the SRC with a logic "1" shifts the contents of the accumulator one bit position to the right. If the add/subtract controls are enabled, the sum or difference of the accumulator register and the "R" register is shifted one bit to the right and written into the accumulator.
17	Shift right output	SRO	SRO is the LSB end of the 8 bit accumulator and may be connected directly to the SRI of an adjacent 8 bit slice.
18	Shift left input	SLI	The SLI accepts the SLO output from a lower order, 8 bit slice.
19	Ground	GND	Circuit common and substrate ground are both connected to this pin.
20	Shift left clock	SLC	Pulsing the SLC with a logic "1" shifts the contents of the accumulator one bit position to the left. If the add/subtract controls are enabled, the sum or difference of the accumulator and the "R" register is shifted one bit to the right and written into the accumulator.
21	Accumulate clock	AC	Pulsing the AC input adds the contents of the accumulator and the "R" register if ASS = logic "1". The "R" register is subtracted from the accumulator if ASS = "0". If ASI = "1", no action occurs.
22	Carry/borrow input	CBI	A logic "1" on CBI enters a carry or borrow into the LSB position of the add/subtract logic.
23	Reset "R" register	RR	Placing a logic "1" on RR asynchronously resets the "R" register.
24-31	Inputs	0-7	Inputs are entered into the "R" register asynchronously when RL is activated.
32	"R" register data load	RL	When RL is a logic "1", data presented at the inputs are loaded into the "R" register. RL may be permanently a logic "1", effectively bypassing the R register during normal operation. Note that RR overrides the data inputs regardless of the load command.
33	MSB "R" register output	MSB	It shows the MSB of the "R" register. When the "R" register is used to temporarily hold operands during multiply, divide, etc., the MSB output indicates the sign of the stored operand.
34	Carry/borrow output	CBO	The CBO is the asynchronous carry or borrow output from the MSB of the add/subtract logic. It is not affected by the ASI control.
35	V_{GG} power supply	V_{GG}	−27 V supply.
36	V_{DD} power supply	V_{DD}	−13 V supply.

SHIFT COMMAND TIMING DIAGRAM



CARRY/BORROW 8 STAGE PROPAGATION TIME

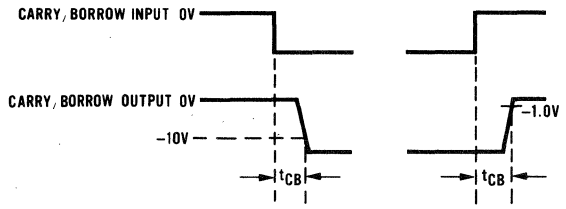
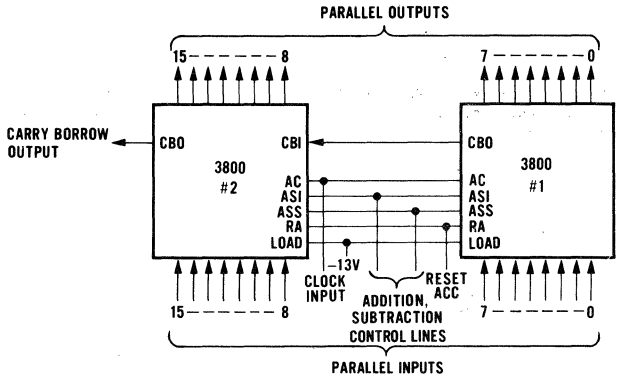


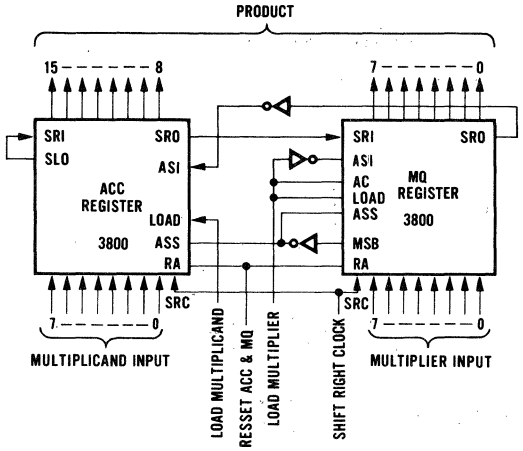
FIGURE 1

STANDARD CONNECTIONS FOR ADDITION AND SUBTRACTION



SIXTEEN BIT PARALLEL ADDITION (SUBTRACTION)*: The addition (subtraction) operation begins by resetting the accumulator, then transferring the augend (subtrahend) through the "R" register into the accumulator by pulsing the AC clock line. The operation is completed by loading the addend (minuend) into or through the "R" register, then adding (or subtracting if ASS = logic "0") it from the accumulator by again pulsing the AC clock. Multiple addition and subtraction or combinations of both operations may be performed by repeating the last operation. Thus a running total may be kept in the accumulator.

STANDARD CONNECTIONS FOR MULTIPLICATION

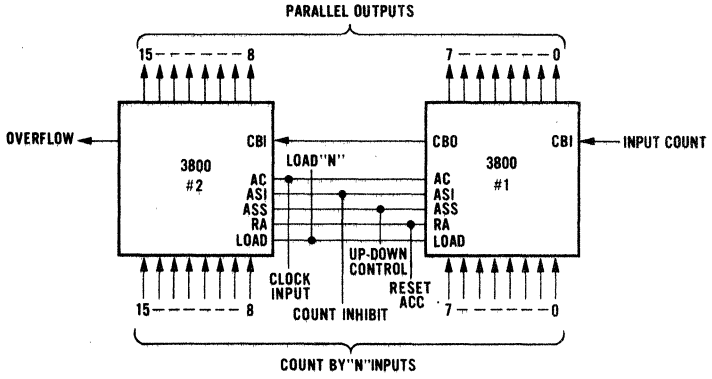


MULTIPLICATION: The multiplication operation, shown above, begins by clearing the ACC and MQ registers, then loading the multiplier into the MQ "R" register. If the MSB of the MQ's "R" register is a "1", ie. the multiplier is negative, the ACC and MQ subtract lines are enabled before the multiplier is transferred into the MQ. Thus the multiplier in the MQ is always positive. However, the multiplicand, which has been loaded into the ACC "R" register for temporary storage, will be subtracted from the partial product in the ACC if the multiplier was negative. The multiplicand is added to or subtracted from the partial product and shifted one bit to the right each time the LSB of the MQ register is a "1". If it is a "0", only a shift right occurs. Neither the multiplicand nor the resulting product require any further sign corrections as the answers will automatically be in two's complement.

DIVISION: The division algorithm is similar to the multiply and is described in detail in The Logic of Computer Arithmetic by Flores. The most straightforward way to perform division is to convert both the divisor and dividend to sign magnitude numbers the same way the multiplier was converted in multiplication. Then proceed through a successive subtraction division. The resulting positive quotient must however then be corrected to two's complement rotation if the signs of the dividend and the divisor were not the same.

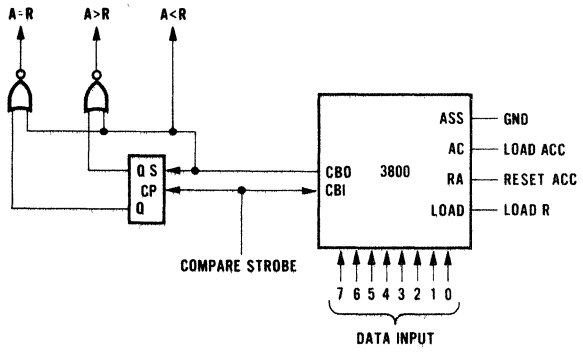
NOTES: 1. Input logic levels may be selected by referring to the list of Pin Function Descriptions.
2. All unused input or control pins should be grounded.
3. All operands are in two's complement notation.
4. All diagrams are BASIC BLOCK DIAGRAMS and no electrical levels are indicated. See Logic Diagram for correct 806B notation.

APPLICATIONS



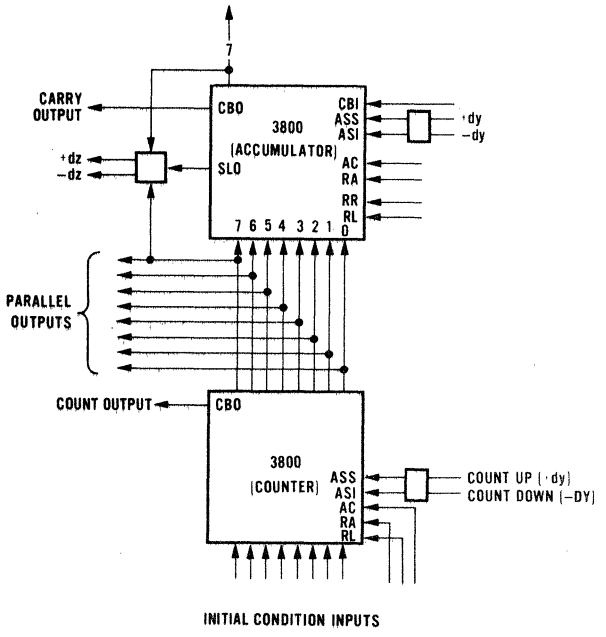
UP-DOWN COUNTER

SIXTEEN STAGE UP-DOWN COUNTER: Operation begins by resetting the registers and enabling ASS, which determines the count direction. Counting by one may be accomplished by enabling CBI or INPUT "0". To count by n, set n into the "R" register.



L, = > COMPARATOR

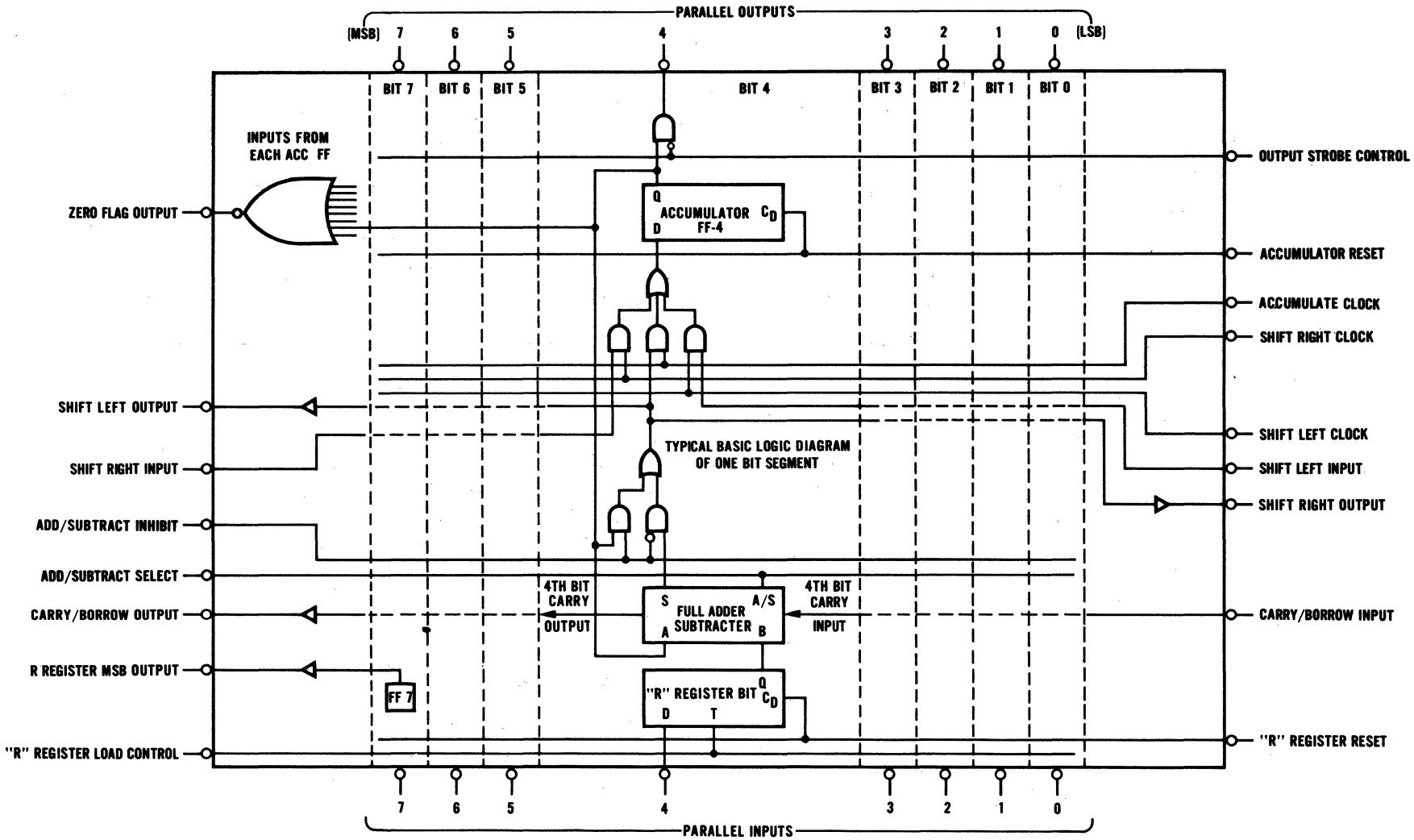
COMPARE OPERATION: To compare two numbers, simply insert the first into a previously cleared accumulator by pulsing AC. Enabling the subtract control will immediately indicate whether R>A, as a borrow output will appear. If the borrow output follows a pulse on the borrow input, the numbers are equal. If neither, then R<A. The logic is shown above.



DDA CONNECTIONS

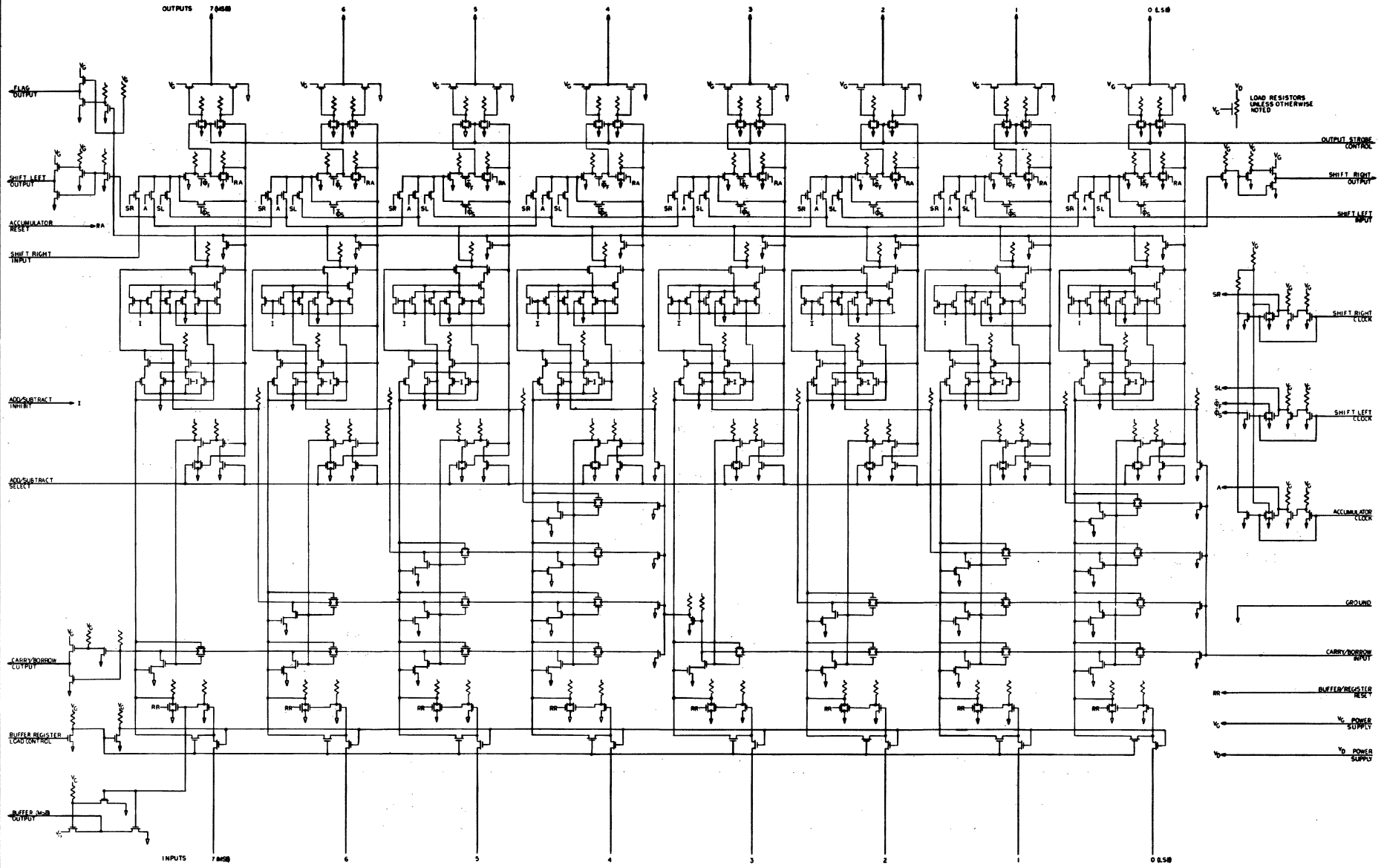
The DDA shown above utilizes one 3800 for a remainder register and a second 3800 for a y accumulator counter.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (0) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈−10 V and LO = "0" ≈ Gnd.

SCHEMATIC DIAGRAM



3801

10-BIT SERIAL/PARALLEL-PARALLEL/SERIAL CONVERTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3801 is a monolithic MOS/LSI ten bit serial/parallel - parallel/serial converter utilizing P-Channel Enhancement mode MOS technology. The device has the capability of serial or parallel input and serial or parallel output. A holding register included on the chip is isolated from the shift register by transfer gates. In serial to parallel applications data may be stored in the holding register while new data is being entered into the shift register.

FEATURES

- **8 AND 10 BIT SERIAL OUTPUT**
- **250 kHz SERIAL TO PARALLEL OPERATION**
- **500 kHz PARALLEL TO PARALLEL OPERATION**
- **120 mW POWER DISSIPATION**
- **INPUT GATE PROTECTION**
- **SET AND RESET OF HOLDING REGISTER**
- **OUTPUT STROBE CONTROL**
- **SINGLE PHASE CLOCK**
- **RESET OF SERIAL REGISTER**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

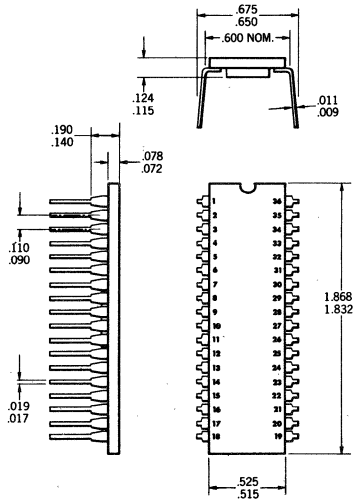
Input Voltages	−30 to +0.3 Volts
Power Supply	−30 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature (A6H380114X)	−55°C to +85°C
(A6H380119X)	0°C to +70°C

APPLICATIONS

Serial and Parallel Data Conversion in

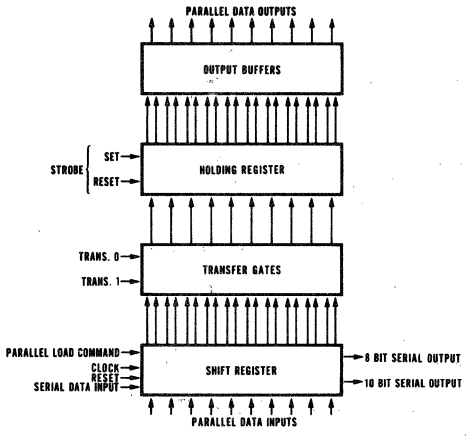
- Process Control
- Data Terminals
- Computer Peripheral Equipment
- Data Acquisition

PHYSICAL DIMENSION
36 PIN
DUAL IN-LINE PACKAGE

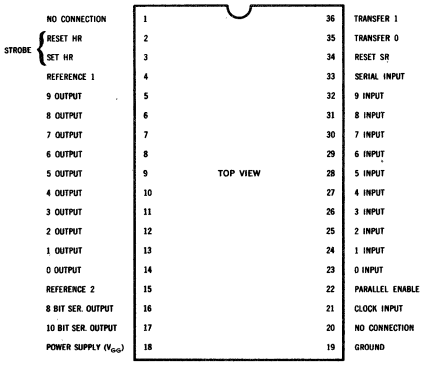


ORDER PART NO. A6H380114X
A6H380119X

BLOCK DIAGRAM



PIN CONFIGURATION



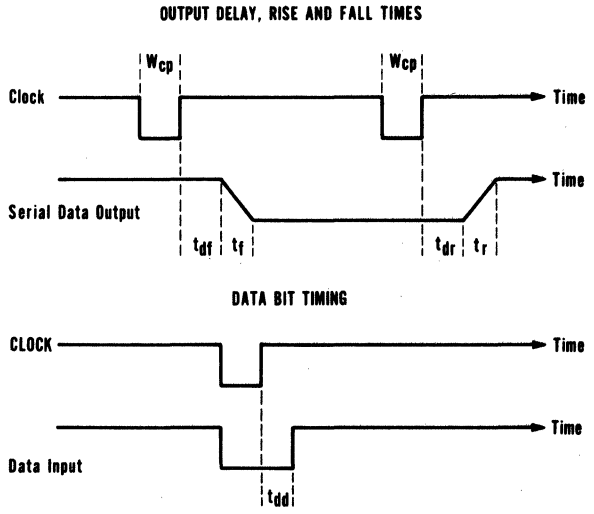
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

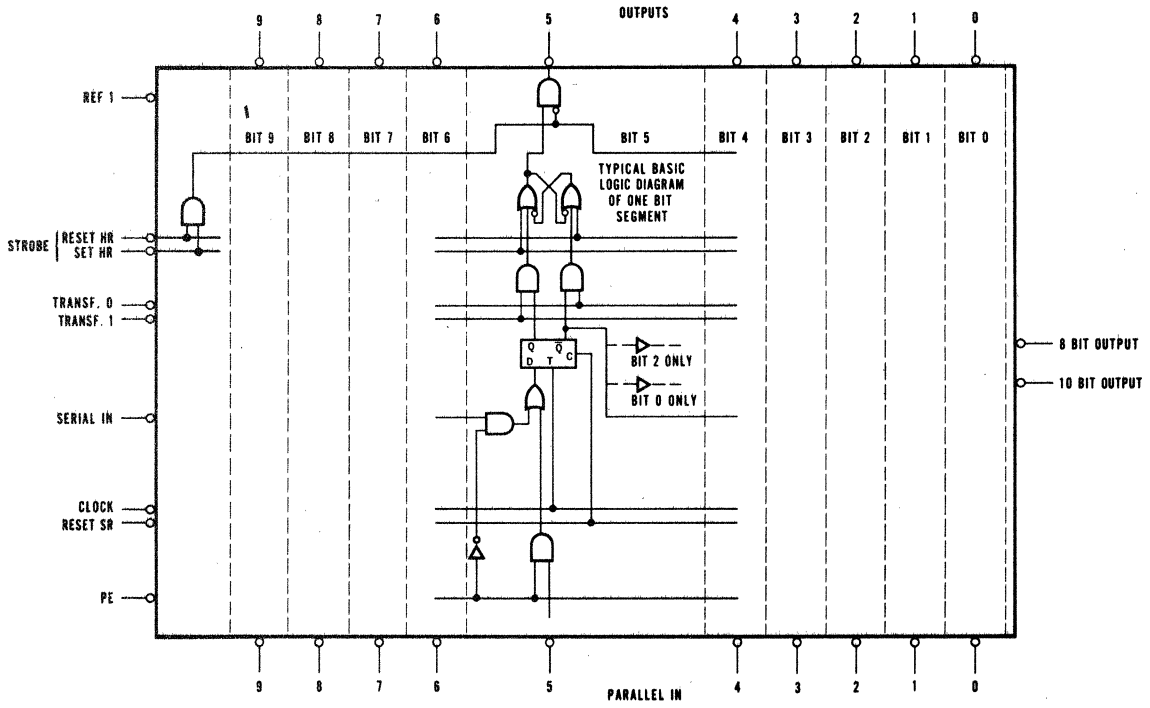
ELECTRICAL CHARACTERISTICS ($V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10M\Omega$, $C_L = 10$ pF unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10	−11		Volts	$R_L = 40$ kΩ
	"1"	−11	−12		Volts	
	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Frequency					
	Serial	DC		250	kHz	
	Parallel	DC		500	kHz	
t_{df}	Serial Delay,		0.6		μs	
t_f	rise and fall		0.2		μs	
t_{dr}	times		0.5		μs	
t_r			0.5		μs	
t_{df}	Parallel Delay,		0.55		μs	
t_f	rise and fall		0.35		μs	
t_{dr}	times		0.4		μs	
t_r			0.3		μs	
C_{in}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
I_{LX}	Input Leakage Current			5.0	μA	$V_{in} = -20$ V
t_{dd}	Data Delay Time	250			ns	

TIMING DIAGRAM

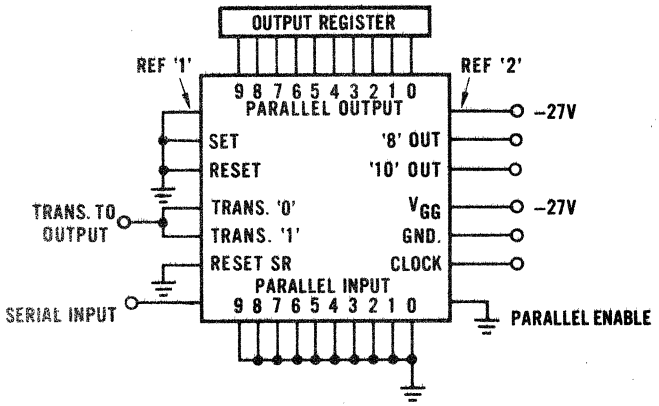


LOGIC DIAGRAM

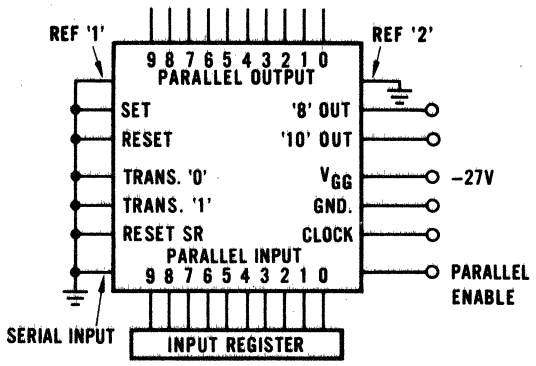


APPLICATIONS (Basic Logic Representation)

SERIAL TO PARALLEL CONVERTER



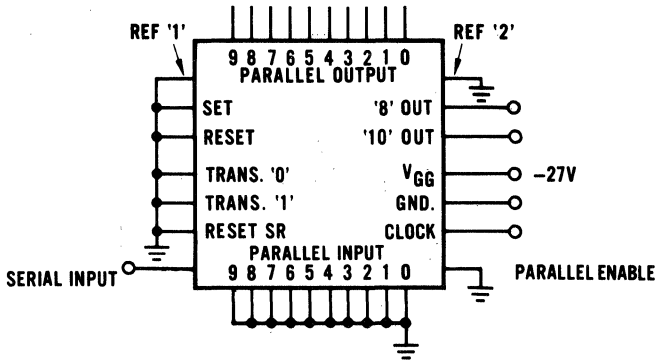
PARALLEL TO SERIAL CONVERTER



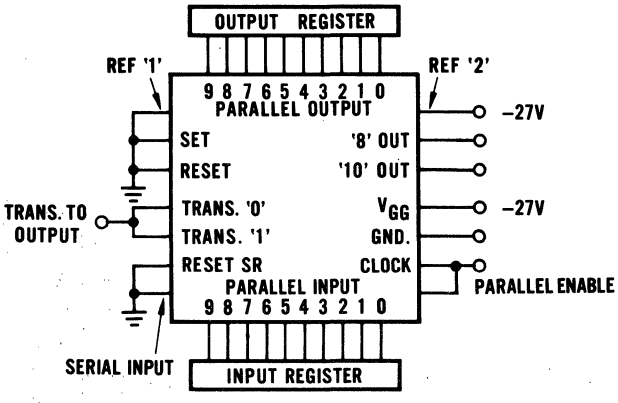
APPLICATIONS

(Basic Logic Representation)

SERIAL TO SERIAL BUFFER REGISTER



PARALLEL TO PARALLEL BUFFER REGISTER

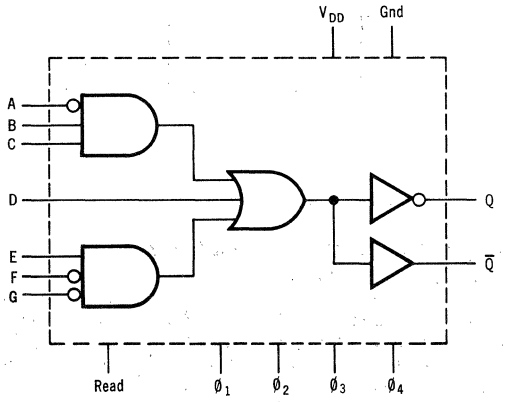


MOS INTEGRATED CIRCUITS COMING SOON

Type	Function	Type	Function
3103	Dynamic Universal Gate	3502	4096-Bit Dynamic Read Only Memory
3104	Dynamic Universal Storage Element	3503-6	2048-Bit Dynamic Read Only Memory
3251	64 Character Raster Scan Character Generator (7 x 9 Matrix)	3511	256-Bit Random Access Memory
3307	Dual 100-Bit Static Shift Register	3531	256-Bit Random Access Memory
3322	Triple 66-Bit Dynamic Shift Register	3716	16 Channel Random Sequential Multiplexer
3323	Triple 64-Bit Dynamic Shift Register	3802	8-Bit S-P, P-S Dynamic Shift Register/Converter
3324	512-Bit Dynamic Shift Register	3804	4-Bit Arithmetic Unit (Basic CPU Element)

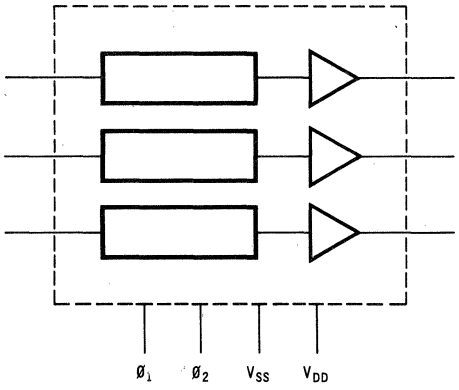
3103 — DYNAMIC 40 UNIVERSAL GATE

The 3103 is a universal gate utilizing P-channel Enhancement Mode MOS technology. It is a dynamic 4ϕ circuit with DC stable outputs and is compatible with the dynamic logic family. Both data and data compliment outputs are available.



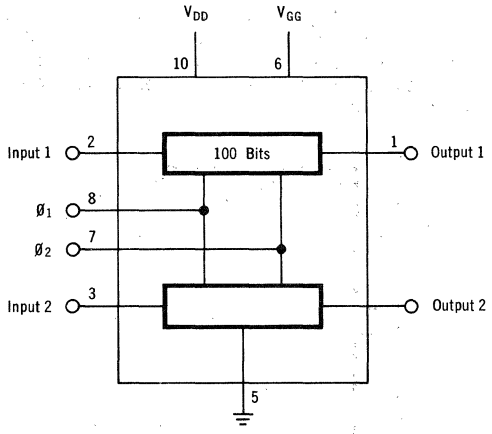
3322/3 — TRIPLE 66/64 BIT 20 DYNAMIC SHIFT REGISTER

The 3322/3 is a triple 66 bit dynamic shift register. It is a monolithic integrated circuit utilizing Planar II* P-channel Enhancement Mode MOS Technology. The 3322 is designed to hold a 64 bit data word and 2 bit sign word. The 3323 is a 64 bit mask option of the 3322.



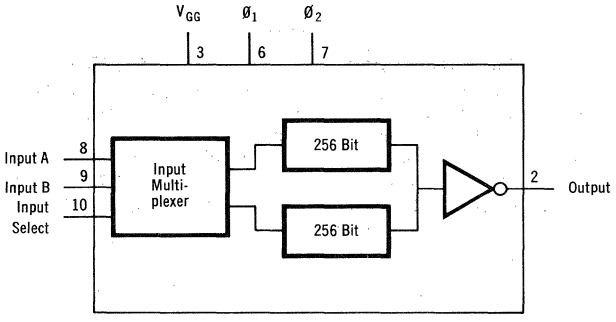
3307 — DUAL 100 BIT STATIC SHIFT REGISTER

The 3307 is a dual 100 bit static serial in-serial out shift register utilizing 2 phase clock capable of operating from DC to 1 MH_3.



3324 — 512 BIT DYNAMIC SHIFT REGISTER

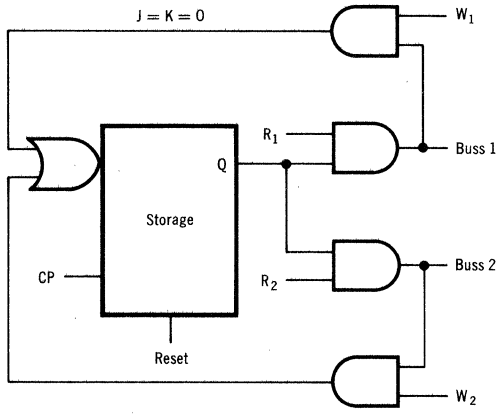
The 3324 is a 512 Bit Dynamic MOS Shift Register. Input logic is provided for multiplexing two data sources or recirculating stored data.



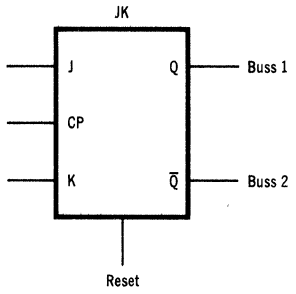
MOS INTEGRATED CIRCUITS COMING SOON

3104 — DYNAMIC 40 UNIVERSAL STORAGE ELEMENT

The 3104 is a Universal Flip-Flop utilizing P-channel Enhancement Mode MOS technology. It is a monolithic dynamic 4ϕ storage element incorporating DC stable output and bi-directional bussing techniques. This provides "write in" or "read out" capability on the same data lines. The 3104 is a member of a compatible dynamic logic family.



LOGIC DIAGRAM

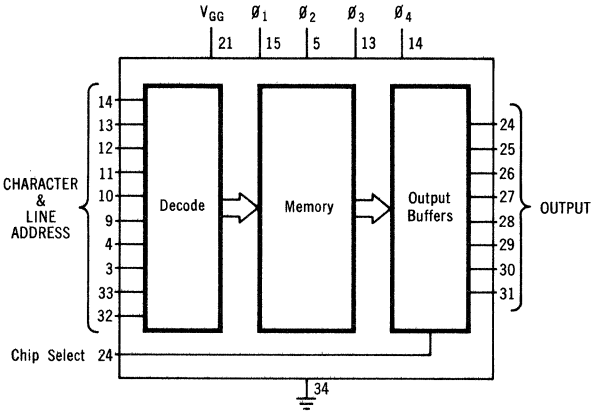


$W_1 = W_2 = 1$
$R_1 = R_2 = 1$

3251 — 64 CHARACTER RASTER SCAN CHARACTER GENERATOR

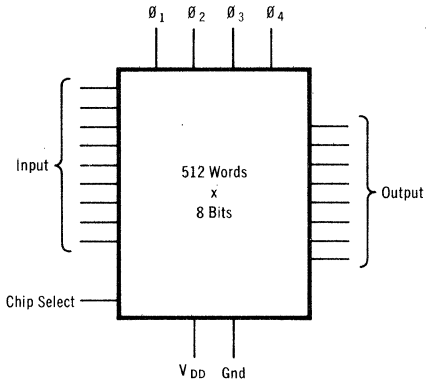
The 3251 is a character generator designed for use with a CRT display utilizing TV type raster. Six input lines are provided to select one of 64 alpha-numeric or special symbol characters for display in an 8 x 10 point pattern (7 x 9 dot matrix). Four additional input lines are provided to select the lines within a character.

NOTE: This device can be used as a 640 word by 8 bit (5120 bit) general purpose Read Only Memory.



3502 — 4096-BIT DYNAMIC READ-ONLY MEMORY

Fairchild will announce a 4096-bit dynamic read-only memory. It will be a monolithic integrated circuit utilizing 4ϕ technology for operation. The output buffers will have static characteristics. The format will be 512 words by 8 bits. The fixed program memory must be specified by the customer and is customized by modifying one mask in the fabrication process. This results in a low cost, fast turn-around custom memory.

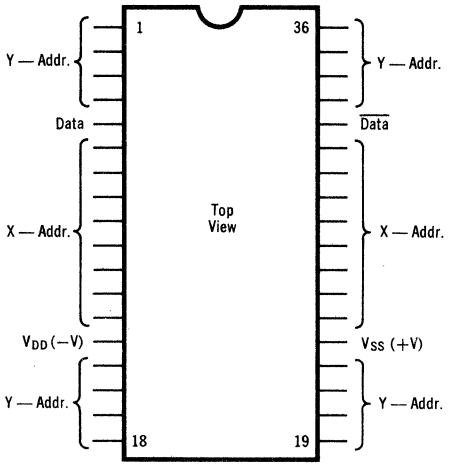


3503-6 — 2048-BIT DYNAMIC READ-ONLY MEMORY

The 2048-bit dynamic read-only memory utilizes P-channel enhancement mode MOS technology. The output buffers feature bipolar compatibility and static characteristics. Metal mask options allow memory formats of 2048 words by 1 bit, 1024 words by 2 bits, 512 words by 4 bits, and 256 words by 8 bits. The fixed program memory must be specified by the customer. The memory is customized utilizing computer aided design techniques to generate the modified gate oxide cut mask. This results in a fast turnaround, low cost custom memory.

3511 — 256 BIT RANDOM ACCESS MEMORY

The 3511 is a 256 bit MOS memory cell designed to operate with bipolar decode drivers and a current mode sense amplifier. The 256-1 bit words are selected by coincident addressing of the X-Y adress lines. Cycle times (read or write) of approximately 200 nanoseconds are achieved.

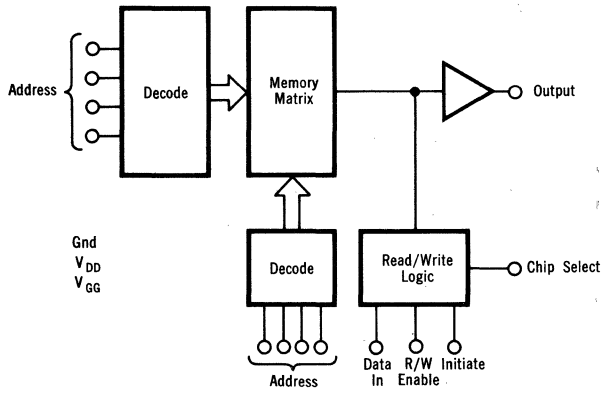


MOS INTEGRATED CIRCUITS COMING SOON

3531 — 256 BIT RANDOM ACCESS MEMORY

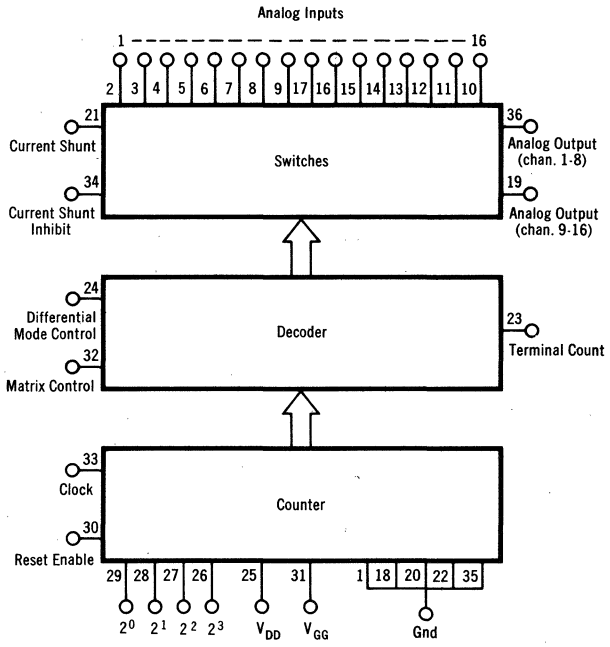
The 3531 is a monolithic MOS/LSI two hundred fifty-six bit random access non-destructive read out (NDRO) memory with decode and output buffers on chip. The memory is arranged as 256 one-bit words, which may be addressed one at a time by means of 8 address lines.

Address:	8 pins
Supplies:	3 pins
Input:	1 pin
Output:	1 pin
Chip select:	1 pin
Read/Write:	1 pin
Strobe:	1 pin
	16 pins



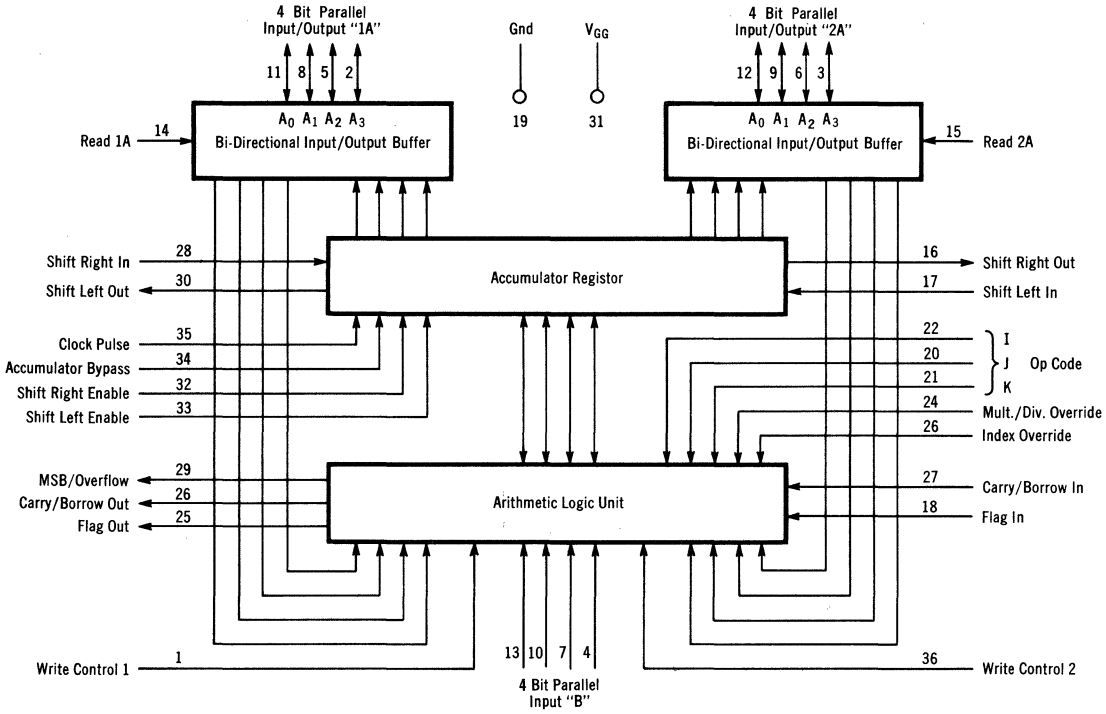
3716 — 16 CHANNEL MULTIPLEXER

The 3716 is an analog or digital multiplexer which may be used as a single 16 channel, a dual 8 channel or a differential 8 channel multiplexer. The 3716 channel selection can be made in a random access, or sequential mode.



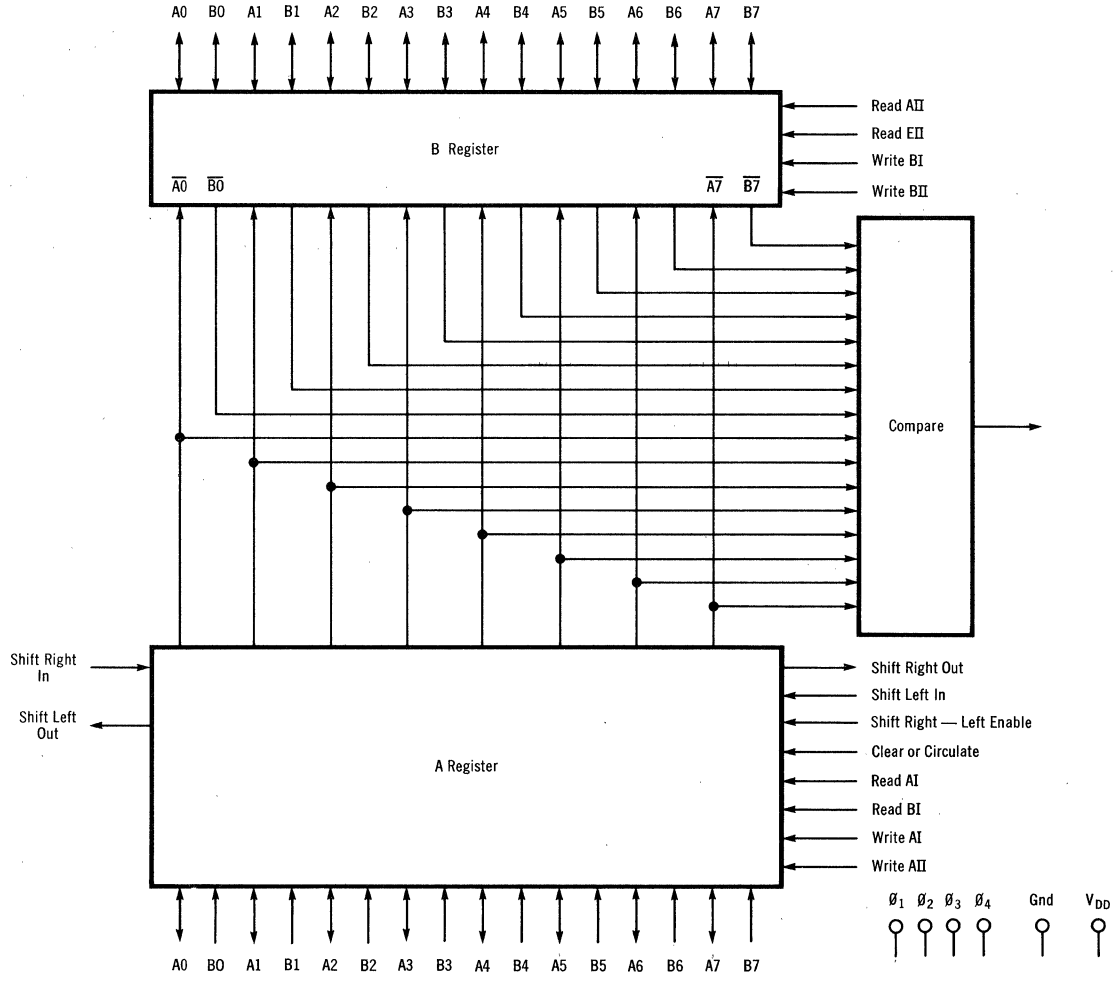
3804 — 4 BIT CPU ELEMENT

The 3804 is an MOS/LSI device that functions as a 4 bit slice of a Central Processing Unit. It is expandable to any word length in 4 bit increments. The 3804 performs the logic functions of OR, AND, Exclusive NOR and Compare, and the arithmetic functions of ADD or Subtract (A-B or B-A). It has the capability of signed or unsigned operation as well as the capability to shift right or left for multiply or divide operation.



3802 — 8 BIT DUAL RANK 4ϕ DYNAMIC BUFFER REGISTER

The 3802 is a Dual Rank Buffer Register featuring bi-directional bussing capability. Data may be entered into register A or B from either one of two common data busses. The data may be transferred between registers but register A can only be read out on Buss I and register B on II.



Application Notes and Technical Papers

APPLICATION NOTES - NUMERIC LISTING

APP-41 Stable Wideband Emitter Followers — Paul J. Beneteau

APP-59 An Improved Emitter-Coupled Multivibrator — P. J. Beneteau and A. Evangeliste

APP-61/2 Long Delay Transistor Timer — P. Alderisio

APP-64 Application of Milliwatt Micrologic® Elements — H. T. Chua

APP-85 Micrologic® Shift Counters — George Powers

APP-87 A Varactor Bias Servo System — Bruce O. Anderson

APP-88 Medium Power Silicon Transistor DC to DC Converters — Thomas B. Mills

APP-93 Transient Response Characteristics of Phototransistors — George T. Daughters

APP-103 Applications of the Silicon Planar* Field-Effect Transistor — Larry Blaser and John MacDougall

APP-105 A Monolithic Operational Amplifier — Robert Widlar

APP-106 Using Fairchild Integrated Circuits as Monostable Multivibrators — Robert Ricks

APP-107 Diode Transistor Micrologic® — George Powers

APP-109 Applications of the Silicon Planar* II MOS FET — John MacDougall

APP-111 The Improved μA702** Wideband DC Amplifier — Robert Widlar

APP-114 μA702** Circuit Design Ideas — (Six Authors)

APP-115 Maximum Integrated Circuit Utilization Through Mixing Compatible Logic Families — Robert Ricks

APP-116 The Operation and Use of a Fast Integrated Circuit Comparator — Robert Widlar

APP-117 Frequency Compensation Techniques for an Integrated Operational Amplifier — James Giles

APP-118 Counter Micrologic® A New Dimension in Multi-Function Integrated Circuits — George Powers

APP-119 Ways to Increase Speed in Large Count Binary Counters — Jack Irwin

APP-120 Using the J-K Flip-Flop in Small Modulo Counters — Jack Irwin

APP-121 A High-Efficiency Power Supply Using Micrologic® Integrated Circuits — Samuel Schwartz

APP-123 Core Memory Sense Amplifier Designs Using an Integrated Dual Comparator — Robert Widlar

APP-124 Designing with Off-the-Shelf Linear Microcircuits — Robert Widlar and James Giles

APP-125 A Versatile Tester for Linear Integrated Circuits — James Giles

APP-128 Complementary Transistor Micrologic® Integrated Circuits — R. C. Ghest

APP-130 Aids for Digital IC Systems — Murray Siegel and Lee Marley

APP-131 Transistor-Transistor Micrologic® Integrated Circuits — John Nichols

APP-132 Single-Phase Control for Cycloconverter — Samuel Schwartz

APP-133 Precision Electronic Digital Clock Uses IC's — B. Jensen and J. Irwin

APP-134 Effect of Integrated Circuits on Systems — Comparative Case — Robert Ricks

APP-135 Performance of the μA703 in 100 MHz and 200 MHz Amplifiers and 100 MHz Harmonic Mixers — David Bingham

APP-139 Multivibrator-Type Vertical-Deflection Circuit for Television — J. S. MacDougall

APP-141 Transistorized TV Horizontal Driver System — Larry Blaser and Hermann Ebenhoech

APP-142 15-Watt Audio Amplifier with Short-Circuit Protection — Don Smith

APP-143 A Horizontal Oscillator for Transistorized TV Set — Larry Blaser and Hermann Ebenhoech

APP-144 Frequency Synthesizer for 27 MHz Citizens' Band Transceiver — Larry Blaser

APP-145 Color Television Chroma Reference Systems Using the μA703 — Larry Blaser and Norm Sturn

APP-146 Color TV Sound System Using the Fairchild μA703 — Larry Blaser

APP-147 Characterization and Application of μA703 in Four-Stage High-Quality FM IF Amplifier — David Bingham

APP-148 25-Watt Audio Amplifier with Short-Circuit Protection — Derek Bray and Wesley Votipka

APP-149 Semiconductor Circuits for 19-inch Black and White Television Receivers — Derek Bray

APP-150 Semiconductor Circuits for Hybrid Color Television — Derek Bray

*Planar is a patented Fairchild process.

**The μA702 is renumbered the μA702A.

APPLICATION NOTES/TECHNICAL PAPERS, NUMERIC LISTING

APP-151 High-Performance Integrated FM IF Strips — Ted Hanna

APP-152 250 MHz Distributed Amplifier Suitable for CATV Truck Line — Larry Blaser and Norman Sturn

APP-153 Logic Designs Using the TTμL9008 — Clive Ghest

APP-154 Compatible Current Sinking Logic — Abe Marder and Ralph Bennett

APP-155 Industrial Code Conversion — Don Femling

APP-156 Designing with the μA703 Monolithic RF-IF Amplifier — G. J. Estep

APP-157 A Fixed-Gain Low-Distortion AF Amplifier — G. J. Estep

APP-158 Two High-Performance Monolithic Microcircuits for FM Sound System — David Bingham

APP-159 A Low-Cost AM-FM Radio Employing an Integrated Circuit Design — David Bingham and John (Ted) Hanna

APP-160 Applications of the CCSL 9301 Decoder — R. Clive Ghest

APP-161 CCSL 9300 Shift Register — John L. Nichols

APP-163 Applications of the CCSL 9304 Dual Adder — R. Clive Ghest

APP-164 Application of the μA722 10-Bit Current Source — M. Rudin, G. Erdi, R. Walker, R. Ricks

APP-165 SH3200-SH3201 Hybrid DC Voltage Regulators — S. K. Leong

APP-166 HLLDTμL Integrated Circuits — R. Repass, O. Lykins

APP-167 MSI 9308 Dual 4-Bit Latch — R. C. Ghest

APP-168 Applications of the 9034 Read-Only Memory — P. F. Schenck

APP-169 CCSL 9306 Up-Down BCD Counter — R. C. Ghest, S. Simonsen

APP-170 Applications of the 9311-One-Out-of-16-Decoder — R. C. Ghest

APP-171 Applications of the μA739 and μA749 Dual Preamplifier Circuits in Home Entertainment Equipment — D. Campbell, et al

APP-172 The 3800 Arithmetic Unit — P. Schenck

APP-173 The 9601 - A Second Generation One-Shot — J. Anderson, T. Gray, R. Walker

APP-174 A Low-Cost Hybrid Color TV Receiver — N. Doyle, D. Smith

APP-175 A Low-Noise Dual Operational Amplifier — D. Long, D. Campbell

APP-176 A Digital Frequency Synthesizer for Airborne Navigation or Communications Transceiver — M. Nichols, J. Stinehelfer

APP-177 The Hot Carrier Mixer Diode — S. Sir

APP-178 A Navigation Receiver Using a Digital Frequency Synthesizer — J. Stinehelfer

APP-179 Line-Operated Phono Circuits Using the PFB 1400 — D. Campbell, R. Westlake

---

TP-24 Overloading and Spurious Responses in Transistor FM Tuners — Earl Cummins

TP-27 Forward AGC Design Considerations in Transistorized Television Receivers — Harry Suzuki

TP-28 Measurement of Transistor High-Frequency Current Gain — Heitor Franco

TP-31 An FM Tuner Using MOS-FET's and Integrated Circuits — John Barrett, Larry Blaser, and Harry Suzuki

TP-32 A Unique Circuit Design for a High-Performance, Operational Amplifier Especially Suited to Monolithic Construction — Robert Widlar

TP-33 Some Circuit Design Techniques for Linear Integrated Circuits — Robert Widlar

TP-35 A Black and White and Color TV Video I-F Output Transistor — Derek Bray and Philip Froess

TP-36 A Low Noise, AGC Silicon Transistor Useful From LF to UHF — David Bingham, Harry Suzuki, and Charles Watson

TP-37 Integrated Circuits in Industrial Control — Donald Femling and Jack Irwin

TP-38 Semiconductor Video Amplifiers for Monochrome and Color Receivers — Derek Bray

TP-39 A New 400-Volt Horizontal Output Transistor — T. B. Mills and E. F. Kiburis

TP-40 Radiation Testing of Linear Microcircuits — J. Darryl Lieux

TP-41 Space and Nuclear Environments and their Effects on Semiconductors — David K. Myers

TP-42 Novel Multi-Purpose LIC's Introduce New Concepts into Circuit Design — David Bingham

TP-43 Color TV Processing Using Integrated Circuits — Larry Blaser and Derek Bray

TP-44 Let's Clarify IC Noise Margins — R. Clive Ghest

TP-46 TTμL Integrated Circuits: High Speed Considerations — R. C. Ghest

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Note: The following publications are obsolete and out of print:
APP's 1-40, 42-58, 60, 62, 63, 65-84, 86, 89-92, 94-102, 104, 108, 110, 112, 113, 122, 126, 127, 129, 138, 140.
TP's 1-23, 25, 26, 29, 30, 34.

Ordering Information

MICROCIRCUITS PRODUCT CODE EXPLANATION

IXING PRIVILEGES:

gital Circuits: (RTμL, LPRTμL, TTμL, CμL and CTμL).

gital circuits may be mixed for price advantage within the following groups gardless of temperature range or package, as long as minimum line item iantity is met.

Group 1:
All RTμL and LPRTμL may be mixed except for epoxy circuits.

Group 2:
Mixing is allowed on all DTμL, TTμL, MSI, CCSL, LPDTμL, HLLDTμL and Dual DTμL device types.

Group 3:
CTμL circuits may be mixed.

Group 4:
CμL circuits may be mixed.

Linear Circuits (LIC):
Linear circuits may not be mixed.

1 integrated circuit purchases, 100 pieces or more of any single product are ways sold at the 100 piece single price.

1 the purchase of more than one product, any quantity under 100 pieces may 3 bought at the 100 piece mixed price if;

a) all the items total 100 pieces or more;
b) Minimum quantity per line item is 10 pieces.

IICROCIRCUITS PRODUCT CODE EXPLANATION

; Fairchild integrated circuits are available in a wide variety of package con-gurations and operating temperature ranges, it is essential that customers)ecify the exact circuit, package, and temperature range desired.

1ere is a ten-digit product code used by all Fairchild distributors and field sales 'fices to identify integrated circuits in a particular package and temperature ıge. Proper use of this product code, explained in detail below, will ensure ıe expeditious handling of all customer orders.

full range RTμL 9900 in a TO-5 package is designated by code number 5D990021X. Breakdown of the code is as follows:

U	5D	9900	21	X
A	B	C	D	E

A. Generic Device Type — U for microcircuits, H for hybrids, A for MOS/IC, and Bipolar Arrays and Memories.
B. Package Code (see table below).
C. Basic Circuit Code.
D. Temperature Range (see table below).
E. This digit is used by LIC to indicate electrical class (see below).

. PACKAGE CODE

FLAT PACKAGES

SIZE	MAXIMUM LEADS	NAME	CODE
1/4 x 3/16	10	Cerpak	3D
1/4 x 3/16	14	Cerpak	3E
1/4 x 1/4	10	Cerpak	3F
1/4 x 1/4	10	Flat Pack	3G
1/4 x 1/4	10	Glass	3H
1/4 x 1/4	14	Cerpak	3I
1/4 x 1/4	14	Flat Pack	3J
1/4 x 3/8	14	Cerpak	3K
1/4 x 3/8	16	Glass	3L
Custom			3S

PLUG-IN PACKAGES

SIZE	MAXIMUM LEADS	NAME	CODE
1/4 x 3/4	14	Dip	6A
1/4 x 3/4	16	Dip	6B
.520 x .850	16	Dip	6D
.255 x .750	14	Dip	6E
.255 x .550	10	Dip	6F
.252 x .767	14	Fairpak™	1A
.300 x .846	16	Dip	6J
.600 x 1.23	24	Dip	6G
.600 x 1.83	36	Dip	6H

TO-5

MAXIMUM LEADS	PINS USED	PINS SHORTED TO CAN	CODE
8	All 8 pins	None	5A
8	All 8 pins	4	5B
8	1, 2, 3, 4, 6 & 8 pins	4	5C
8	1, 3, 4, 5, 7 & 8 pins	4	5D
10	All 10 pins	None	5E
10	All 10 pins	5	5F
12	All 12 pins	None	5G
14	All 14 pins	None	5H
10	1, 2, 3, 4, 5, 6, 8, 9, 19 pins	None	5J
Custom			5S

EPOXY

8	All 8 pins		8A
8	1, 3, 4, 5, 7 & 8 pins		8B
Custom			8S

C. Four digits are used for general product groups.

0000-0099 = Kits and kit parts
1000-1999 = Custom integrated circuits
3000-3900 = MOS Integrated Circuit
5000-5999 = Second source integrated circuits
7000-7999 = Linear integrated circuits
9000-9999 = Digital integrated circuits

D. Two digits are used to indicate process and temperature range respectively.

11 = (−55°C to +125°C)	MOS/Full Range Military
14 = (−55°C to +85°C)	MOS/Intermediate Range
19 = (0°C to +70°C)	MOS/Industrial Range
21 = (−55°C to +125°C)	Full Range Military Equipment
22 = (0°C to +100°C)	Military Ground Support Equipment
28 = (+15°C to +55°C)	Commercial Equipment
29 = (0°C to +70°C)	Industrial Equipment
31 = (−55°C to +125°C)	Full Range Military Equipment (LIC)
32 = (0°C to +85°C)	Industrial Equipment (LIC)
39 = (0° to +70°C)	Industrial Equipment (LIC)
51 = (−55°C to +125°C)	Full Range Military Equipment
56 = (−20°C to +100°C)	Intermediate Range
59 = (0°C to +75°C)	Industrial Equipment (DTμL and CμL)
59 = (+15°C to +55°C)	Commercial Equipment (CTμL)
79 = (+15°C to +55°C)	Commercial Equipment (CTμL) Clamped
79 = (0°C to +75°C)	Counting Family (CμL)

E. This digit is used by LIC to indicate electrical class.

1 = High performance Aerospace and Defense
2 = Standard Aerospace and Defense
3 = Industrial and Ground Aerospace and Defense
4 = Consumer

This digit used by MOS/IC to indicate electrical class.
2 = ±5.0 volt analog input
3 = 0 to 5.0 volt analog input

MICROCIRCUITS FAMILY DESIGNATIONS

CμL	= Counting Micrologic® Integrated Circuits
CTμL	= Complementary Transistor Micrologic®
C/DTμL*	= Diode Transistor Micrologic®
C/LPDTμL*	= Low Power Diode Transistor Micrologic®
RTμL	= Micrologic® Integrated Circuits
LPRTμL	= Low Power Micrologic® Integrated Circuits (Formerly MWμL)
C/TTμL	= Transistor Transistor Micrologic® (T^2)
LIC	= Linear Integrated Circuits (Formerly ALC)
MOS/IC	= Metal over Silicon/Integrated Circuit
*C/XX	= Elements which are part of Fairchild Semiconductor's Compatible Current Sinking Logic (CCSL) family
MSI	= Medium Scale Integration
MμL	= Memory Micrologic®

HYBRIDS PRODUCT CODE EXPLANATION

MINIMUM ORDER $50.00

MIXING PRIVILEGES:

Hybrid circuits may not be mixed.

HYBRIDS PRODUCT CODE EXPLANATION

The product code consists of a ten digit number giving all information necessary to properly identify the part. For example:

Product Code H/AG/2001/1/XX
Group Letter A/B/C/D/E

Group Letter Explanations:

A. This digit indicates general product code. Currently an "H" is used by Hybrids.

B. Two letters are used to indicate the package as follows:

XC = TO-5, 3 lead header
AM = TO-5, 6 lead header
5T = TO-100, 8 lead header
AG = TO-5, 10 lead header
BW = TO-5, 12 lead header
BG = 1/4 x 1/4 Forbes Flat Package, 10 leads
BH = 1/4 x 1/4 Forbes Flat Package, 14 leads
BK = 3/8 x 3/8 Flat Package, 14 leads
BY = 1" x 0.8" Flat Package, 32 leads
CL = Ceramic Channel
6Q = 14 lead Plastic DIP
6F = 10 lead Plastic DIP
6K = 14 lead Ceramic DIP
6R = 16 lead Ceramic DIP
2A = 5/8 x 5/8 Flat Package
2B = 1" x 1" Flat Package (Flat metal lid)

C. Four digits are used for general hybrid product groups.

0000—1999 = Custom Circuit
2000—2999 = Standard Hybrids — Digital
3000—3999 = Standard Hybrids — Linear
6000—6999 = Quads
9000—9999 = Flyer

D. One digit is used to indicate the operating temperature range.

1XX =	(−55°C to +125°C)	Full Range Military Equipment
8XX =	(+15°C to +55°C)	Commercial Equipment
9XX =	(0°C to +70°C)	Industrial Equipment

E. Currently "XX" is used for these digits.

FAIRCHILD SEMICONDUCTOR

TERMS AND CONDITIONS OF SALE

1. **SCOPE** — THE TERMS AND CONDITIONS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. THE SAID TERMS AND CONDITIONS MAY IN SOME INSTANCES CONFLICT WITH SOME OF THE TERMS AND CONDITIONS AFFIXED TO THE FORM OR ORDER BLANK AND/OR SPECIFIED BY THE BUYER. THEREFORE, ACCEPTANCE OF THE BUYER'S ORDER IS MADE ONLY ON THE EXPRESS UNDERSTANDING AND CONDITION THAT INSOFAR AS THE TERMS AND CONDITIONS OF THIS ACCEPTANCE CONFLICT WITH ANY TERMS AND CONDITIONS OF THE BUYER'S ORDER, THE TERMS AND CONDITIONS OF THIS ACCEPTANCE SHALL GOVERN, IRRESPECTIVE OF WHETHER THE BUYER ACCEPTS THESE CONDITIONS BY A WRITTEN ACKNOWLEDGMENT, BY IMPLICATION, OR ACCEPTANCE AND PAYMENT OF GOODS ORDERED HEREUNDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS AND CONDITIONS OF SALE CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY THE GENERAL MANAGER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER.

   All orders or contracts must be approved and accepted by the Seller at its home office.

   The said terms and conditions of sale shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder.

   Prices quoted for the items described above and acknowledged hereby are firm and not subject to audit, price revision, or price redetermination.

2. **TERMS OF PAYMENT** — All invoices are due and payable 30 days from date of invoice. No discounts are authorized.

   F. O. B. POINT — All sales are made F. O. B. point of shipment. Seller's title passes to Buyer and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point in good condition; the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. All shipments will normally be made by Parcel Post, Railway Express, Air Express or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

4. **DELIVERY** — Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any reprocurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control, including but not limited to acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slowdowns, factory or labor conditions, errors in manufacture and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

5. **TAXES** — Unless otherwise specifically provided herein, the amount of any present or future sales, revenue, excise or other tax applicable to the products covered by this order or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authorities.

6. **PATENTS** — The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs or specifications or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

   Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information and assistance (at the Seller's expense) for the defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is in such suit held to constitute infringement and the use of said product or part is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, or replace same with non-infringing product, or modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof.

7. **ASSIGNMENT** — The Buyer shall not assign his order or any interest therein or any rights thereunder without the prior written consent of Seller.

8. **WARRANTY** — The Seller warrants that the articles to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this warranty are limited to replacing or repairing, at its option, at its factory, any of said articles which shall within one (1) year after shipment be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THE IMPLIED WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This warranty shall not apply to any of such articles which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any article which has either been repaired or replaced by Seller.

9. **PAYMENTS** — If, in the judgment of the Seller, the financial conditions of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance, and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

   Each shipment shall be considered a separate and independent transaction, and payment therefor shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer. The Seller reserves the right to ship to its order and make collection by sight draft with bill of lading attached.

10. **GENERAL** — The Seller represents that with respect to the production of the articles and/or the performance of the services covered by this order, it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended.

    In no event shall any claim for consequential or special damages be made by either party.

11. **GOVERNMENT CONTRACT PROVISIONS** — If Buyer's original purchase order indicates, by Contract Number, that it is placed under a Government contract, the following provisions of the current Armed Services Procurement Regulation are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be, i.e., "Contracting Officer" shall mean "Buyer," "Contractor" shall mean "Seller," and the term "Contract" shall mean this order.

    7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.6, Responsibility for Supplies; 7-103.7, Payments; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.10, Federal, State, and Local Taxes; 7-103.13, Renegotiation; 7-103.15, Soviet Controlled Areas; 7-103.16, Contract Work Hours Standards Act — Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government — (only to the extent that Buyer's contract is terminated for the convenience of the Government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-104.3, Buy America Act; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.14, Utilization of Small Business Concerns; 7-104.15, Examination of Records; 7-104.20, Utilization of Concerns in Labor Surplus Areas.

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