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Volume 25 Book 31
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MICROCOMPUTER D.A.T.A.BOOK®

Edition 10 — **January 1981 through June 1981**

8,816 Types — **151 Manufacturers**

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Purpose

This D.A.T.A.BOOK is designed to report comprehensively on what is being produced throughout the world in the field of MICROCOMPUTERS and MICROPROCESSOR devices. Though this book can not provide 100% of the information you might need, its primary aim is to facilitate the selection of devices and systems suitable to your technical requirements, and to direct you to the sources of their manufacture.

Technical Data Acquisition

D.A.T.A. acquires information presented in this D.A.T.A.BOOK with the cooperation of the participating manufacturers who supply us with their latest technical and accessory data. Manufacturers are not charged for the listing of their products. Manufacturers listed include those producing microprocessor chips only, to those producing complete microcomputer systems.

Types Of Data Presented

This D.A.T.A.BOOK defines microcomputer systems as those which use one or a few chips as the basis for the central processing unit, or microprocessor. It presents data on single chip and chip set microprocessors; modular/printed circuit board microprocessors; microcomputer chip and card families – including family memory and input/output devices; computers-on-a-card; computers-on-a-chip (microcontrollers); and pre-packaged stand-alone microcomputer systems. This book lists end-item, general purpose microcomputer devices and systems, not dedicated microprocessor-based equipments.

System/ Software Sections

Microcomputer System Information is emphasized in the system portion of the book. System features and characteristics are compared, hardware and software product lines are listed, instruction sets and formats are given for each system, and system block diagrams provide interconnection data.

Component Sections

Electrical, mechanical and environmental characteristics of microprocessors and family-related memory, input/output and support devices, derived from manufacturers' data sheets, are presented in the component portion of the book. Associated logic, block, connection and outline drawings complete the component information data picture. Detailed outline/package data are limited to chip components.

Price And Availability

Because of the rapidly-changing and complex nature of this field, current price and delivery information should be obtained direct from the manufacturers. The list of manufacturers and the Local Offices Section in the back of the book will assist you in these matters.

Manufacturers' Specifications

This book includes currently-manufactured systems/components and systems/components soon-to-be available with their major characteristics, drawings and manufacturers. Every effort is made to ensure the accuracy of the entries herein; however, the publisher can not be held responsible nor guarantee against the possibility of error or omission. Only the manufacturers or their authorized representatives can provide you with complete technical details.

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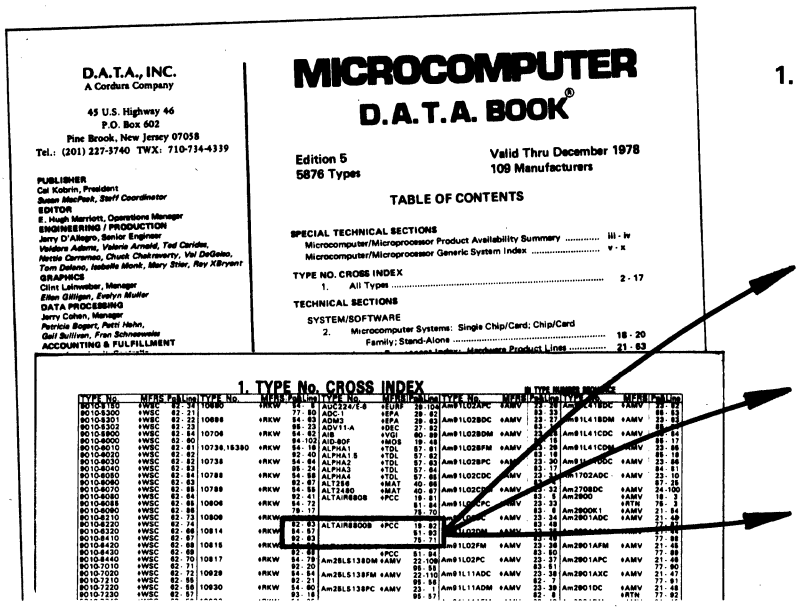

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MICROCOMPUTER D.A.T.A. BOOK®

Edition 5
5876 Types

Valid Thru December 1978
109 Manufacturers

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1. TYPE No. CROSS INDEX

1. KNOWN: Microcomputer System Number - ALTAIR 8800B
UNKNOWN: Information coverage in the Microcomputer D.A.T.A.BOOK

a. In the Type No. Cross Index (Section 1) locate the "known" type number in this alpha-numeric sequenced section. (For example: ALTAIR 8800B).

b. Note the 3-letter manufacturer's code(s) indicated for the "known" type. (PCC for ALTAIR 8800B).

c. Note the "three" Pg. & Line numbers; ie., "19-82, 51-93, 75-71," alongside the type number. Each reference directs you to a specific portion of the total information coverage.

Page 19 Line 82 gives "System Level" data on the ALTAIR 8800B.

2. MICROCOMPUTER SYSTEMS

IN ORDER OF: (1)DATA BITS (2)MANUFACT. CODE & (3)SYSTEM TYPE No.

LINE No.	3 SYSTEM TYPE No.	ORGANIZ-ATION 1 DATA BITS	ARCHI-TECT-URE	SYS. CONFIGURATION ADDRESSABLE MEMORY (RAM/ROM) (BYTES)	I/O DEV @PT WIDTH (D/WDTH)	No. BASIC MICRO INSTR	No. ADDR MODE	INTERR-UPT LEVEL No. & TYPE	INSTRUCT TIME-TYP §CLK CYC *-MIN (s)	No. GEN PUR-POSE REG	STACK LEVEL	SYMBOL: PT-PORT V-VECTORED P-PRIORITY M-MULTIPLE OTHER CAPABILITIES	INSTR SET REF. No.	SYSTEM DWG.	2 MFR. CODE
82♦	ALTAIR8800B	8	SYS	64k	256/8	78	4	8VP	2.0u	6		Uses Intel 8080A CPU	IS21	S61	PCC
83♦	ALTAIR8800B-T	8	SYS	64k	256/8	78	4	8VP	2.0u	6		Turnkey Model Of 8800B	IS21	S61	PCC
84♦	MICROPAC80A	8	SYS	64k	256/16	78	4	M,V	2.0u	6		Uses Intel 8080 MPU	IS21		PCS

Page 51 Line 93 shows the ALTAIR 8800B as part of the manufacturer's ALTAIR 8800 product line.

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP SUB CLASS	TECHNOLOGY	DESCRIPTION	1 MFR. CODE
91♦	680B-MDS	ALTAIR680B	PERIP	UNIT		Minidisk Subsys;125k Bits/Sec Transfer Rate;Access Time 2.9 Sec max	PCC
92♦	680B-BSM	ALTAIR680B	RAM	MOD		16k Static Mem Board;Uses 4 4096x8 Bit Mem Arrays;Access Time215ns Max	PCC
93♦	ALTAIR8800B	ALTAIR8800	COMP	UNIT		8 Bit Gen Purpose Byte Oriented Computer	PCC
94♦	ALTAIR8800B-T	ALTAIR8800	COMP	UNIT		Turnkey Model of ALTAIR 8800B;Front Panel Program Controls Omitted	PCC
95♦	88-DC	ALTAIR8800	DEV	MOD		Diagnostic Card Used W/CRT Display;Incl Decoder for Octal Data Display	PCC
96♦	88-PROM	ALTAIR8800	DEV	UNIT		PROM Programmer Incl Chassis and I/O Card for 1702A PROMS	PCC
97♦	88-VI/RTC	ALTAIR8800	IO-02	MOD		Vector Interrupt/Real Time Clock	PCC
98♦	88-ACR	ALTAIR8800	IO-05	MOD		Audio Cassette Record Interface	PCC
99♦	88-2SIO	ALTAIR8800	IO-20	MOD		Serial Interface Board;Based On ACIA	PCC
100♦	88-SIOB	ALTAIR8800	IO-20	MOD		Serial Interface to Ham RTTY or CW Station	PCC
101♦	88-4PIO	ALTAIR8800	IO-30	MOD		4 Port Parallel I/O Board;Uses 4 6820 ICs	PCC
102♦	88-ADC	ALTAIR8800	IO-41	MOD		8 Chan,12 Bit A/D Conv Card;10V Unipolar-Bipolar Input;Conv Time 65uS	PCC
103♦	88-AD/DA	ALTAIR8800	IO-42	MOD		8 Chan,8 Bit Acquisition Subsys Card;Total Conversion Time 12uS max	PCC
104♦	88-MUX	ALTAIR8800	IO-43	MOD		Analog MUX Card;Used with 88-ADC to Expand Input Capacity to 24 Chan	PCC
105♦	88-PCI	ALTAIR8800	IO-92	MOD		Process Control Interface Card;2 Opto-Isolator Lines;8 Relay 110V,1.0A	PCC
106♦	88-7000	ALTAIR8800	PERIP	UNIT		Graphics Printer;Uses 1 Port of 88-4PIO Board;Req Electrosensitive Paper	PCC
107♦	88-DCDD	ALTAIR8800	PERIP	UNIT		Floppy Disk Unit;Consists Of Disk Controller And Disk Drive	PCC
108♦	88-DISC	ALTAIR8800	PERIP	UNIT		Disk Drive in Cabinet;Uses Pertec FD400 Drive;No Controller Boards	PCC

Page 75, Line 71 refers to expanded technical data on the I/O capability of this microcomputer.

6. SYSTEM INTERFACE

IN ORDER OF: (1)DATA BITS (2)MFR. CODE (3)SYSTEM TYPE No.

LINE No.	3 SYSTEM TYPE No.	1 DATA BITS	ADDRESSING: TYPE	ISOLATED DEVICES @ PORT WIDTH	MEMORY-SPACE DEV @ PT WIDTH	OPERATING MODE: TYPE	No. of OP.	SERIAL BITS	INTERRUPT: V-vectored Pr-priority P-poll TYPE	No LNS	No LEV	S-softw,DMA I-interrupt INITI-ATION	DMA LOC.	I/O LINES: A D R	S E N S	C N T L	F L A G	M I S C	TRANSFER: INSTR TIME (s)	OPER. CAPAB ILITY CODE	MAXIMUM BAUD RATE ASYNC (BPS)	SYNC. (BPS)	SYSTEM DWG.	2 MFR. CODE
67#	uCOM-80F	8	B	512/8	64k	P			V	1		S	EXT	16		9	5		2.0u	A				NECJ
68♦	SC/MP	8	M		64k/8	S	3			1	1	DIS	CPU	16	2	6	3		10u	A			S34	NSC
69	7808	8	I	4/8		P			PrV	2	2	IS	EXT	16					2.0u	A			S86	OEI
70♦	ALTAIR680B	8	M		4/8	PS	8		Pr	1	1	S	NA	16		7			4.0u	AB	9.6k			PCC
71♦	ALTAIR8800B	8	I	256/8		PS			PPrV	1	8	IS		8					2.0u	AB	9.6k		S61	PCC
72	MICROPAC80A	8	M		256/16	PS			P	1		IS	NA	16	8	12	8		2.5u	ABC	640k			PCS

Continued on next page

HOW TO MAKE MAXIMUM USE OF THIS D.A.T.A.BOOK (cont'd)

d. Support software for the ALTAIR 8800 System is grouped by the manufacturer code PCC and listed in the System Software Index (pg. 70 Line 19 thru 37) shown below.

4.SYSTEM SOFTWARE INDEX

IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME	LANGUAGE	AVAILABILITY/COMPATIBILITY	1 MFR. CODE
19♦	SW-ALTAIR8KBASIC#2	6800	ALTAIR680B	LAN	Standard BASIC Sys for Altair 680B;Reg 8k Mem Unit 680B-BSM			PCC
20♦	SW-ALTAIR680ASSMBLR	6800	ALTAIR680B	ASB	Assembly Language Dev Sys for 6800;Incl Editor/Assembler;Reg 8k of Mem			PCC
21♦	SW-88DBLP▼	8080	ALTAIR8080	LOA	DiskBootLoader PROM;Used W/88-PMC to Load Disk Ext BASIC on Flop Disk			PCC
22♦	SW-88MBL▼	8080	ALTAIR8080	LOA	MultiBootLoader PROM;Used W/88-PMC to Load Sftwr on Papertape/Cassette			PCC
23♦	SW-ALTAIR4KBASIC	8080	ALTAIR8800	LAN	Minimum Altair Software Sys Using BASIC Language;Reg 4k of Memory			PCC
24♦	SW-ALTAIR8KBASIC#1	8080	ALTAIR8800	LAN	Standard BASIC Sys;Incl Interrupt,Trig/Other Functions;Reg 8k of Memor			PCC
25♦	SW-ALTAIRA01	8080	ALTAIR8800	BAS	Business System General Ledger Pkg			PCC
26♦	SW-ALTAIRA02	8080	ALTAIR8800	BAS	Business System Inventory Pkg			PCC
27♦	SW-ALTAIRA03	8080	ALTAIR8800	SSS	Word Processing Pkg;Store,Edit/Print Documents Up to 45Pgs or 120 Char			PCC
28♦	SW-ALTAIRA04	8080	ALTAIR8800	BAS	Business System Payables Pkg			PCC
29♦	SW-ALTAIRA05	8080	ALTAIR8800	BAS	Business System Receivables Pkg			PCC
30♦	SW-ALTAIRA06	8080	ALTAIR8800	BAS	Business System Payroll Pkg			PCC
31♦	SW-ALTAIRA08	8080	ALTAIR8800	BAS	Combination Accounting Pkg Consisting of A01,A04,A05, and A06 Pkgs			PCC
32♦	SW-ALTAIRDOS	8080	ALTAIR8800	OPS	Disk Op Sys Pkg to Assemble/Edit 8080 Ass Progr on Disk;Reg 16k Mem			PCC
33♦	SW-ALTAIRDSKBASIC	8080	ALTAIR8800	LAN	Disk BASIC for DiskFile Supp;Incl Utilities to Format Disk;Reg 24k Mem			PCC
34▼	SW-ALTAIRDSKTSBASIC	8080	ALTAIR8800	LAN	Timeshare Disk BASIC;Reg Disk Subsys 88-DCDD,88-PMC PROM and 32k RAM			PCC
35♦	SW-ALTAIREXTBASIC	8080	ALTAIR8800	LAN	Extended BASIC to Run on min Memory of 16k			PCC
36♦	SW-ALTAIRPKGII	8080	ALTAIR8800	MFS	Assembly Lang Dev Sys for 8080;Incl Monitor,Edit,Assem,Debug 8k Mem			PCC
37♦	SW-ALTAIRTSBASIC	8080	ALTAIR8800	LAN	Timeshare BASIC;Up to 8 Simultaneous Progr;PaperTape/Cassette;Reg32kRa			PCC
38▼	SW-PCM12890	6100	PCM-12A	EDT	4k Basic Interpreter.			PCM
39▼	SW-BOS80A	8080	MICROPAC80A	OPS	Basic Operating System			PCS

e. A brief synopsis of the ALTAIR 8800B instruction set is given in the Instruction Set Index.

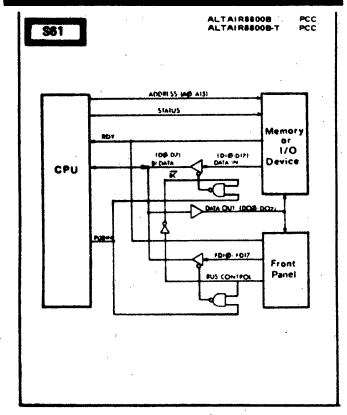
5. INSTRUCTION SET INDEX

IN ORDER OF: (1)MANUFACTURER CODE &(2)SYSTEM TYPE No.

LINE No.	2 SYSTEM TYPE No. (IS-D.A.T.A. PREFIX)	No. BASIC INSTR	TOTAL No. INSTRUCTIONS W/VARIATIONS	SYMBOLS: DESCRIPTION	INSTRUCTION SET REFERENCE No.	INSTRUCT FORMAT DWG.	1 MFR. CODE
28▼	IS-7808	76		2.0us Instruction Cycle;Binary and Decimal Arithmetic	IS20		OEI
29#	IS-PFL16A	33	345	Include Byte Processing,Bit Operation,Decimal Arith,Stack Operation,Etc	IS30	F17	PAFJ
30♦	IS-ALTAIR680B	72		Include Binary,Decimal Arithmetic,Logical,Shift,Rotate,Etc	IS6		PCC
31♦	IS-ALTAIR8800B	78	111	5 Types-Data Transf,Arithm,Log,Branch and Stack,I/O,Etc	IS21	F7	PCC
32♦	IS-ALTAIR8800B-T	78	111	5 Types,Data Transfer,Arithmetic,Logical,Branch And Stack I/O,Etc	IS21		PCC
33▼	IS-PCM-12A	67		12 Bit Work Instructions;3 Classes;Memory Ref,Operate,I/O Transfer	IS3	F1	PCM
34♦	IS-MICROPAC80A	78	111	5 Types-Data Transfer,Arithmetic,Logical,Branch And Stack,I/O,Etc	IS21	F7	PCS
35	IS-PCS1806	78		5 Types-Data Transf,Arithm,Log,Branch and Stack,I/O,Etc	IS21		PCS
36	IS-PCS1810	78		5 Types-Data Transf,Arithm,Log,Branch and Stack,I/O,Etc	IS21		PCS

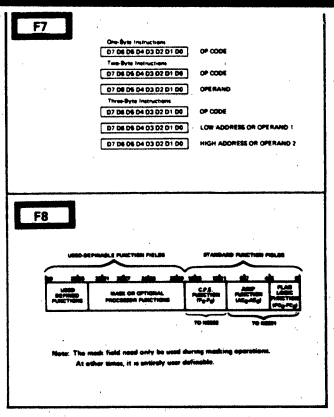
f. Supplementary system data on the ALTAIR 8800B include System Block Drawings, Instruction Format Drawings and complete Instruction Set summaries. Reference to these drawings is made in the various technical sections.

15 SYSTEM BLOCK DRAWINGS



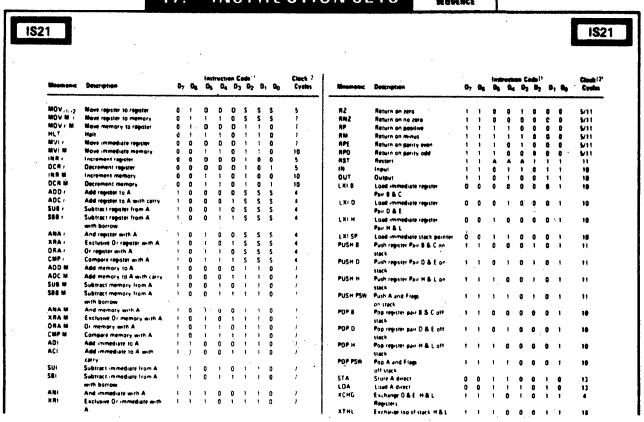
System Block Drawings are referenced in Technical Section 2.

16. INSTRUCTION FORMAT DRAWINGS



Instruction Formats are referenced in Technical Section 5.

17. INSTRUCTION SETS IN DRAWING NUMBER SEQUENCE



Instruction Set summary lists are referenced in Technical Sections 2 & 5.

PORT	INSTR SET REF. No.	2 SYSTEM DWG.	MFR. CODE
PABILITIES			
rol Unit	IS21	S61	PCC
ocomputer,	IS21	S61	PCC
	IS21		PCS

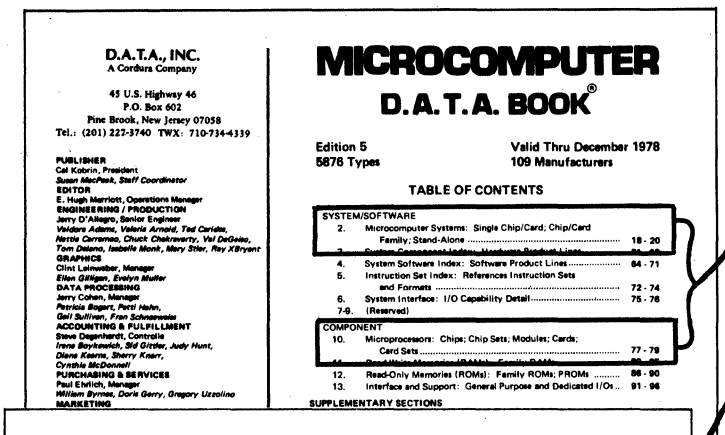
INSTRUCTION SET REFERENCE No.	INSTRUCT FORMAT DWG.	1 MFR. CODE
IS21	F7	PCC
IS21		PCC
IS3	F1	PCM

ORT	INSTR SET REF. No.	2 SYSTEM DWG.	MFR. CODE
ABILITIES			
(Store	IS21	S61	PCC
)0	IS21		PCS

INSTRUCTION SET REFERENCE No.	INSTRUCT FORMAT DWG.	1 MFR. CODE
IS21	F7	PCC
IS21		PCC
IS3	F1	PCM

Continued on next page

HOW TO MAKE MAXIMUM USE OF THIS D.A.T.A.BOOK (cont'd)



D.A.T.A., INC.
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MICROCOMPUTER D.A.T.A. BOOK®

Edition 5
5876 Types

Valid Thru December 1978
109 Manufacturers

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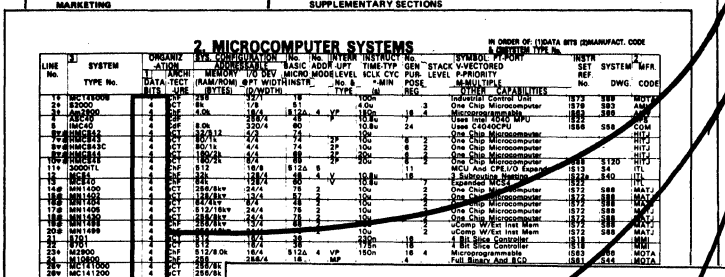
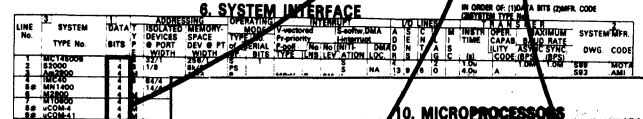
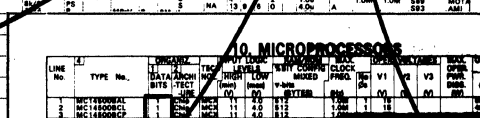


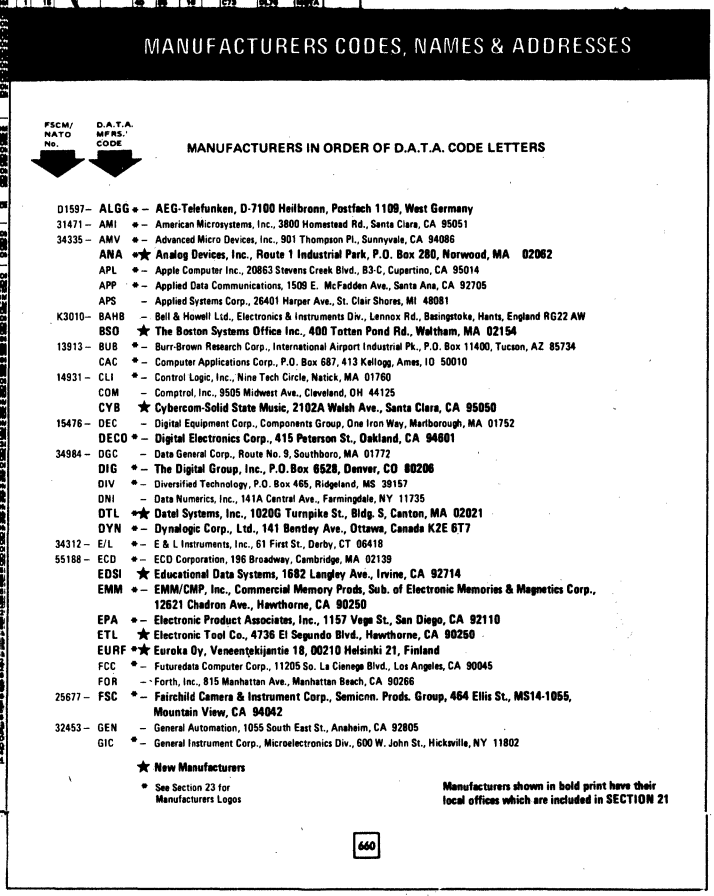
2. MICROCOMPUTER SYSTEMS



6. SYSTEM INTERFACE



10. MICROPROCESSORS



MANUFACTURERS CODES, NAMES & ADDRESSES

FSCM/ NATO No. — D.A.T.A. MFRS.' CODE

MANUFACTURERS IN ORDER OF D.A.T.A. CODE LETTERS

D1597– ALGG ✱– **AEG-Telefunken, D-7100 Heilbronn, Postfach 1109, West Germany**
31471– AMI ✱– American Microsystems, Inc., 3800 Homestead Rd., Santa Clara, CA 95051
34335– AMV ✱– Advanced Micro Devices, Inc., 901 Thompson Pl., Sunnyvale, CA 94086
ANA ✱★ **Analog Devices, Inc., Route 1 Industrial Park, P.O. Box 280, Norwood, MA 02062**
APL ✱– Apple Computer Inc., 20863 Stevens Creek Blvd., B3-C, Cupertino, CA 95014
APP ✱– Applied Data Communications, 1509 E. McFadden Ave., Santa Ana, CA 92705
APS – Applied Systems Corp., 26401 Harper Ave., St. Clair Shores, MI 48081
K3010– BAHB – Bell & Howell Ltd., Electronics & Instruments Div., Lennox Rd., Basingstoke, Hants, England RG22 AW
BSO ★ **The Boston Systems Office Inc., 400 Totten Pond Rd., Waltham, MA 02154**
13913– BUB ✱– Burr-Brown Research Corp., International Airport Industrial Pk., P.O. Box 11400, Tucson, AZ 85734
CAC ✱– Computer Applications Corp., P.O. Box 687, 413 Kellogg, Ames, IO 50010
14931– CLI ✱– Control Logic, Inc., Nine Tech Circle, Natick, MA 01760
COM – Comptrol, Inc., 9505 Midwest Ave., Cleveland, OH 44125
CYB ★ **Cybercom-Solid State Music, 2102A Walsh Ave., Santa Clara, CA 95050**
15476– DEC – Digital Equipment Corp., Components Group, One Iron Way, Marlborough, MA 01752
DECO ✱– **Digital Electronics Corp., 415 Peterson St., Oakland, CA 94601**
34984– DGC – Data General Corp., Route No. 9, Southboro, MA 01772
DIG ✱– **The Digital Group, Inc., P.O.Box 6528, Denver, CO 80206**
DIV ✱– Diversified Technology, P.O. Box 465, Ridgeland, MS 39157
DNI – Data Numerics, Inc., 141A Central Ave., Farmingdale, NY 11735
DTL ✱★ **Datel Systems, Inc., 1020G Turnpike St., Bldg. S, Canton, MA 02021**
DYN ✱– Dynalogic Corp., Ltd., 141 Bentley Ave., Ottawa, Canada K2E 6T7
34312– E/L ✱– E & L Instruments, Inc., 61 First St., Derby, CT 06418
55188– ECD ✱– ECD Corporation, 196 Broadway, Cambridge, MA 02139
EDSI ★ **Educational Data Systems, 1682 Langley Ave., Irvine, CA 92714**
EMM ✱– **EMM/CMP, Inc., Commercial Memory Prods, Sub. of Electronic Memories & Magnetics Corp., 12621 Chadron Ave., Hawthorne, CA 90250**
EPA ✱– **Electronic Product Associates, Inc., 1157 Vega St., San Diego, CA 92110**
ETL ★ **Electronic Tool Co., 4736 El Segundo Blvd., Hawthorne, CA 90250**
EURF ✱★ **Euroka Oy, Veneentekijantie 18, 00210 Helsinki 21, Finland**
FCC ✱– Futuredata Computer Corp., 11205 So. La Cienega Blvd., Los Angeles, CA 90045
FOR – Forth, Inc., 815 Manhattan Ave., Manhattan Beach, CA 90266
25677– FSC ✱– **Fairchild Camera & Instrument Corp., Semicnn. Prods. Group, 464 Ellis St., MS14-1055, Mountain View, CA 94042**
32453– GEN – General Automation, 1055 South East St., Anaheim, CA 92805
GIC ✱– General Instrument Corp., Microelectronics Div., 600 W. John St., Hicksville, NY 11802

★ New Manufacturers

✱ See Section 23 for Manufacturers Logos

Manufacturers shown in bold print have their local offices which are included in SECTION 21

660

2. KNOWN: You wish to review available 4-bit microcomputers and microprocessors

UNKNOWN: Manufacturers of these and comparative characteristics of available types

a. Turn to Technical Section No. 2, MICROCOMPUTER SYSTEMS, and review the data on available 4 bit systems.

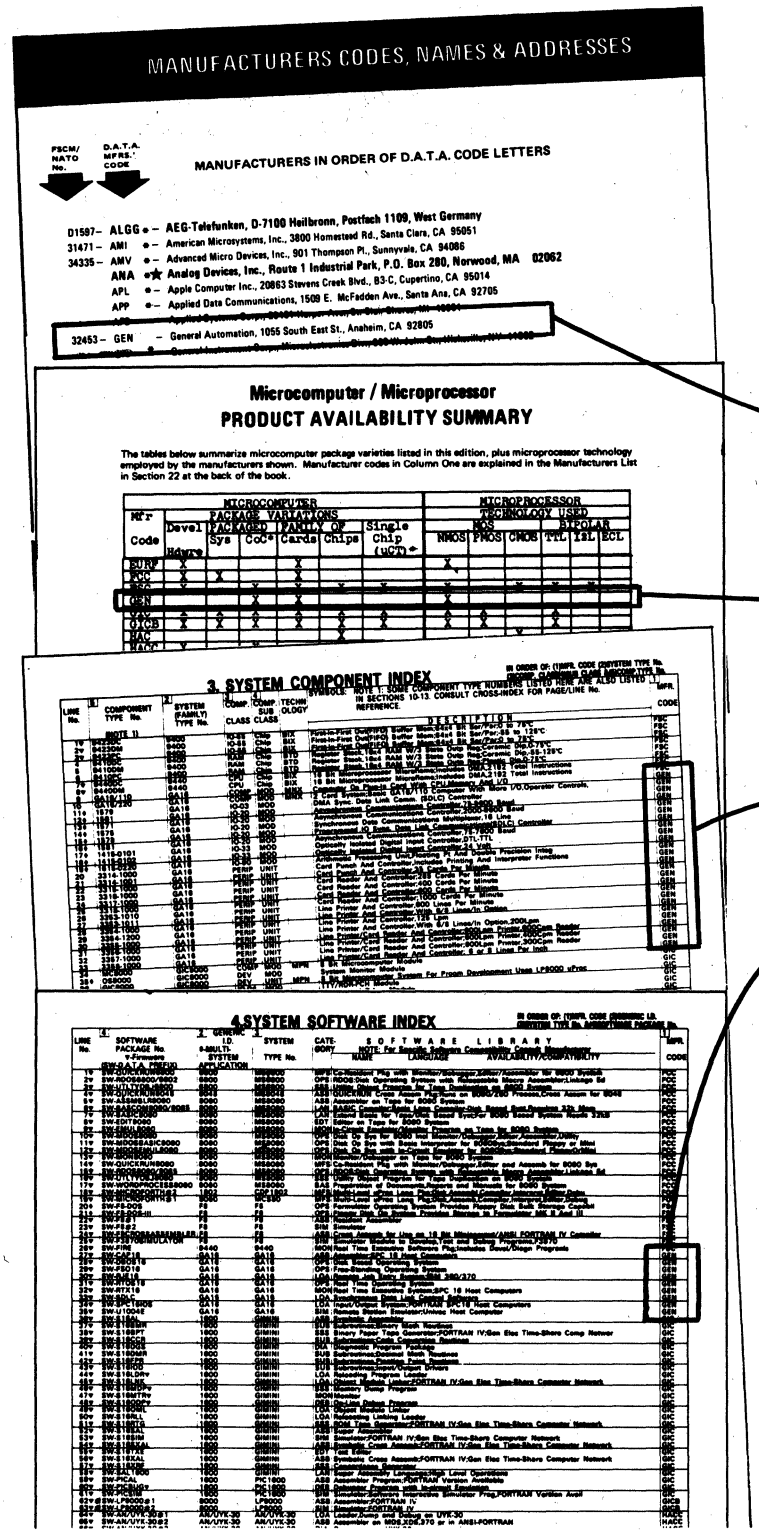
b. Turn to Technical Section No. 6, SYSTEM INTERFACE, for expanded I/O detail for these systems.

c. Detailed characteristics of 4-bit microprocessors are tabulated in Technical Section No. 10, MICROPROCESSORS.

d. Manufacturers of 4-bit systems and components are identified by D.A.T.A. code in the far right column of each of the above-referenced technical sections. Manufacturer code-to-name and address information is provided in Section No. 23, MANUFACTURERS CODES, NAMES & ADDRESSES.

Continued on next page

HOW TO MAKE MAXIMUM USE OF THIS D.A.T.A.BOOK (cont'd)



MANUFACTURERS CODES, NAMES & ADDRESSES

MANUFACTURERS IN ORDER OF D.A.T.A. CODE LETTERS

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31471– AMI – American Microsystems, Inc., 3800 Homestead Rd., Santa Clara, CA 95051
34335– AMV – Advanced Micro Devices, Inc., 901 Thompson Pl., Sunnyvale, CA 94086
ANA – Analog Devices, Inc., Route 1 Industrial Park, P.O. Box 280, Norwood, MA 02062
APL – Apple Computer Inc., 20863 Stevens Creek Blvd., B3-C, Cupertino, CA 95014
APP – Applied Data Communications, 1509 E. McFadden Ave., Santa Ana, CA 92705
32453– GEN – General Automation, 1055 South East St., Anaheim, CA 92805

Microcomputer / Microprocessor
PRODUCT AVAILABILITY SUMMARY

3. SYSTEM COMPONENT INDEX

4. SYSTEM SOFTWARE INDEX

3. KNOWN: Preferred Manufacturer Name – General Automation
UNKNOWN: Scope of Microcomputer Product Line

a. Turn to Section No. 23, MANUFACTURERS, CODES, NAMES & ADDRESSES, and identify the D.A.T.A. code letters for this manufacturer. (For example: GEN).

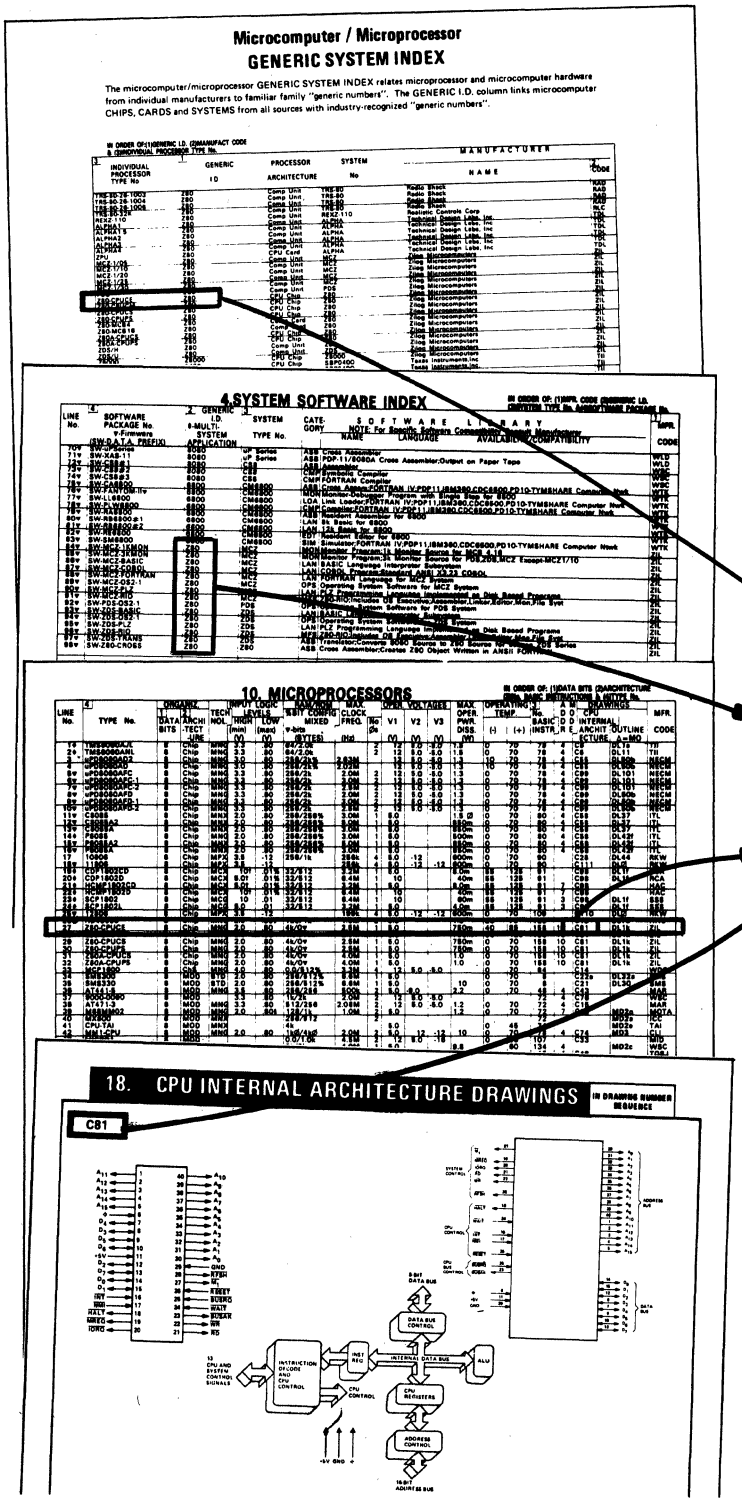
b. To review microcomputer package variations and microprocessor technologies of this manufacturer, turn to the: Microcomputer/Microprocessor PRODUCT AVAILABILITY SUMMARY in the SPECIAL TECHNICAL SECTIONS in the front of the book.

c. Turn to Technical Section No. 3, SYSTEM COMPONENT INDEX, and locate manufacturer code GEN in the far-right column. This is the microcomputer hardware product line.

d. Turn to Technical Section No. 4, SYSTEM SOFTWARE INDEX, and repeat the procedure to find the software product line.

Continued on next page

HOW TO MAKE MAXIMUM USE OF THIS D.A.T.A.BOOK (cont'd)



4. KNOWN: Common (Generic) Microprocessor Number – Z80
   UNKNOWN: Products available using this microprocessor and their sources

a. Turn to the Microcomputer/Microprocessor GENERIC/SYSTEM INDEX in the SPECIAL TECHNICAL SECTIONS in the front of the book.

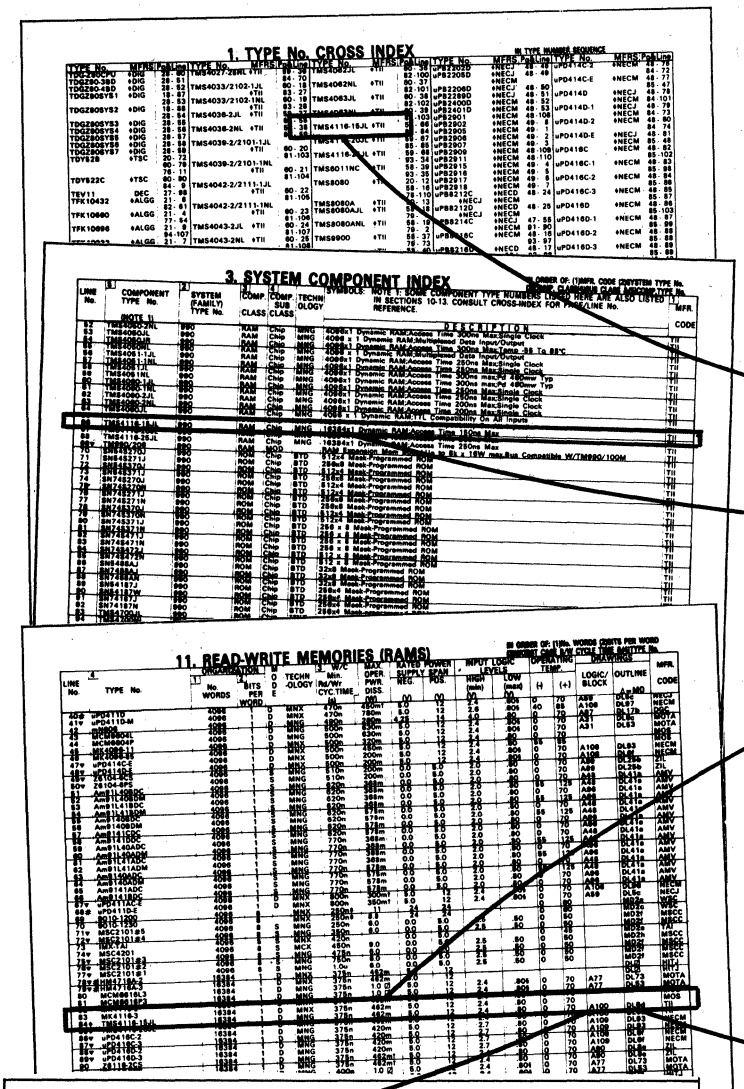
b. In the GENERIC I.D. column locate the generic microprocessor "Z80". (Z80-CPUCE) Microprocessors and systems of separate suppliers are grouped for the generic I.D. "Z80".

c. Software products for the selected manufacturer are grouped by Generic I.D. (Z80) in Technical Section No. 4, SYSTEM SOFTWARE INDEX.

d. CPU internal architecture drawings are given for all microprocessors, referenced in Technical Section 10 - MICROPROCESSORS.

Continued on next page

HOW TO MAKE MAXIMUM USE OF THIS D.A.T.A.BOOK (cont'd)



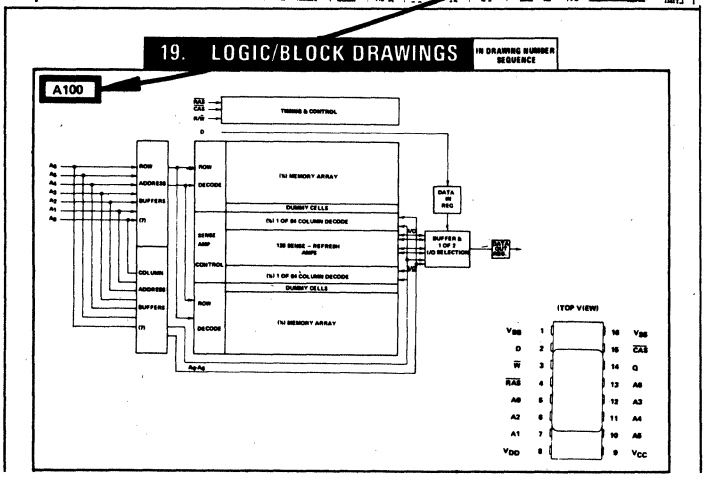
5. **KNOWN:** Microcomputer RAM Type Number – TMS4116-15JL
   UNKNOWN: Electrical Characteristics and Drawing data

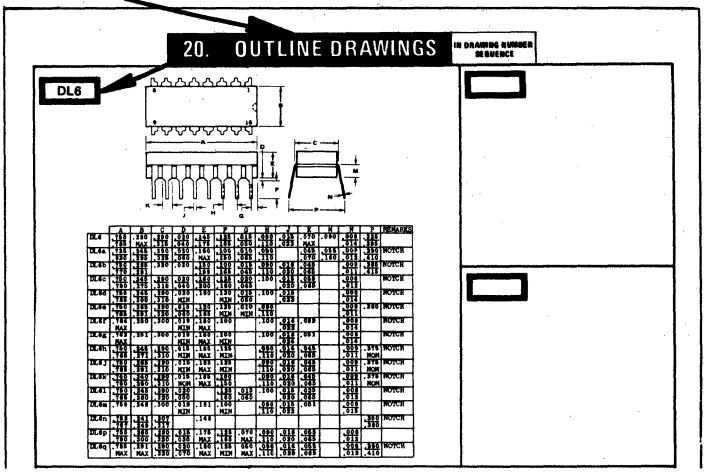
a. In the Type No. Cross Index (Section 1) locate the "known" type number in this alpha-numeric sequenced section. (For example TMS4116-15JL).

b. Note the "two" Pg. & Line references "59-66" refers to descriptive information in the SYSTEM COMPONENT INDEX, "85-84" refers to detail technical data in the READ-WRITE MEMORIES (RAMS) Section.

c. Drawing data are referenced in the LOGIC/BLOCK & OUTLINE drawing columns. Samples shown below.

d. ROMS and I/O chips are covered in the same manner.





Microcomputer / Microprocessor
PRODUCT AVAILABILITY SUMMARY

The tables below summarize microcomputer-related package varieties listed in this edition plus microprocessor technology employed by the manufacturers shown. Manufacturer codes in Column One are explained in the Manufacturers List in Section 23 at the back of the book.

	MICROCOMPUTER						MICROPROCESSOR					
	PACKAGE VARIATIONS						TECHNOLOGY USED					
Mfr Code	Devel Hdwre	PACKAGED Sys	PACKAGED CoC*	FAMILY OF Cards	FAMILY OF Chips	Single Chip (uCT)*	MOS NMOS	MOS PMOS	MOS CMOS	BIPOLAR TTL	BIPOLAR I2L	BIPOLAR ECL
ALGG					X			X				
AMD**	X			X	X	X	X	X		X		
AMI	X	X		X	X	X	X	X				
ANA				X								
APL		X	X	X			X					
APP	X	X	X	X								
APS			X	X			X					
AuC	X	X	X	X		X				X		
BAHB	X	X	X	X								
BEC				X	X	X				X		
BUB				X	X							
CAC	X		X	X			X					
CII				X			X					
CLI	X	X	X	X			X					
COM	X	X		X								
CRO	X	X	X	X								
DEC	X	X	X	X	X		X					
DGC	X	X	X	X	X	X	X			X		
DIG	X	X		X								
DIV	X	X		X					X	X		
DMA	X					X						
DSI	X	X		X			X			X		
DTI				X					X	X		
DTL		X		X		X	X		X	X		
DYB		X	X	X	X							
DYN		X										
E/L	X	X		X			X					
ECD		X										
EDSI			X									
EFCF						X						
EMM		X		X			X			X		
EPA	X	X		X			X			X		
ESI			X	X								
ETL	X	X		X								
EURF	X			X			X					
FCC	X	X		X								
FSC	X	X	X	X	X	X	X		X	X	X	
FSCN							X					
GEN		X	X	X			X					
GIC	X	X	X	X	X	X	X	X		X		
GICB	X	X	X	X	X	X	X	X		X		
HAC	X	X			X				X			
HACC	X	X	X	X						X		
HAS			X		X				X			
HEA		X		X	X							

*CoC – computer-on-a-card
SCC – single component computer (TSC)
uCT – microcontroller/computer-on-a-chip

**AMV replaced by AMD

Continued on next page

Microcomputer / Microprocessor
PRODUCT AVAILABILITY SUMMARY

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	PACKAGE VARIATIONS						TECHNOLOGY USED					
Mfr Code	Devel Hdwre	PACKAGED Sys	PACKAGED CoC*	FAMILY OF Cards	FAMILY OF Chips	Single Chip (uCT)*	MOS NMOS	MOS PMOS	MOS CMOS	BIPOLAR TTL	BIPOLAR I2L	BIPOLAR ECL
HEU	X	X	X	X			X					
HITJ	X			X	X	X	X	X	X	X		
HPA	X											
ICC	X	X		X			X					
IMI	X	X										
IMS	X	X		X								
INF		X		X			X		X			
INL	X	X		X	X				X	X		
ITL	X	X	X	X	X	X	X	X	X	X		
MAR	X	X	X	X			X					
MATC		X		X	X		X					
MATJ	X	X	X		X	X	X	X	X			
MCA			X	X								
MCSS			X									
MCT	X			X								
MDB	X	X			X							
MID		X		X								
MIL					X		X					
MIM				X								
MITC									X			
MITJ		X	X	X	X		X	X		X		
MMI					X	X				X		
MNC				X	X							
MOS	X	X	X	X	X	X	X			X		
MOTA	X	X	X	X	X	X	X		X	X		X
MSCC	X	X	X	X			X		X			
MSS	X	X										
MTY	X			X	X		X	X				
MUL	X	X		X					X			
MULB	X		X	X	X		X			X		
MUP	X	X		X			X					
NASB			X	X			X			X		
NECD			X		X	X	X	X				
NECJ	X			X	X	X	X	X	X	X		
NECM	X	X		X	X	X	X	X	X	X		X
NMS		X										
NOR		X		X								
NSC	X	X	X	X	X	X	X	X	X	X	X	X
OAE		X										
OBJ				X								
OEI			X	X			X					
OHS	X	X	X	X								
PAFJ	X	X	X	X	X		X					
PAR		X		X								

*CoC – computer-on-a-card
SCC – single component computer (TSC)
uCT – microcontroller/computer-on-a-chip

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Microcomputer / Microprocessor
PRODUCT AVAILABILITY SUMMARY

The tables below summarize microcomputer-related package varieties listed in this edition plus microprocessor technology employed by the manufacturers shown. Manufacturer codes in Column One are explained in the Manufacturers List in Section 23 at the back of the book.

	MICROCOMPUTER						MICROPROCESSOR					
	PACKAGE VARIATIONS						TECHNOLOGY USED					
Mfr Code	Devel Hdwre	PACKAGED Sys	PACKAGED CoC*	FAMILY OF Cards	FAMILY OF Chips	Single Chip (uCT)*	MOS NMOS	MOS PMOS	MOS CMOS	BIPOLAR TTL	BIPOLAR I2L	BIPOLAR ECL
PAT	X											
PCM	X	X		X					X			
PCS	X	X	X	X					X			
PHIN	X		X	X	X	X		X			X	
PLM	X	X		X						X		
PRO		X	X	X			X	X	X			
PRT		X	X	X			X					
QUY		X	X	X								
R2E		X										
RAD		X		X								
RCA	X	X		X	X				X			
RCI			X	X								
RKW	X	X	X	X	X	X	X	X				
RTCF					X				X			
RTN					X					X		
SEC		X										
SGAI	X	X	X	X	X	X	X					
SIA		X										
SIC	X	X	X	X	X	X	X			X	X	
SIEG	X	X	X	X								
SMC					X		X	X				
SMS	X	X		X								
SSC				X								
SSM				X								
SSS					X				X			
STP		X	X	X								
SYK	X			X	X	X	X					
TAI		X		X			X					
TEKT	X	X										
TII	X	X	X	X	X	X	X	X		X	X	
TLI		X	X	X			X		X			
TOSJ				X	X	X		X				
TSC		X	X	X	X				X			
UTE		X		X								
VALG	X		X				X			X		
VGI	X	X		X			X					
VIR	X	X										
WDC	X	X	X	X	X	X	X	X				
WLD		X		X								
WTK	X	X	X	X					X			
XIT		X		X								
ZIA	X	X		X								
ZIL	X	X	X	X	X	X	X			X		

*CoC – computer-on-a-card
SCC – single component computer (TSC)
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Microcomputer / Microprocessor
GENERIC SYSTEM INDEX

The microcomputer/microprocessor GENERIC SYSTEM INDEX relates microprocessor and microcomputer hardware from individual manufacturers to familiar family "generic numbers". The GENERIC I.D. column links microcomputer CHIPS, CARDS and SYSTEMS from all sources with industry-recognized "generic numbers".

IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE & (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	[3] INDIVIDUAL PROCESSOR TYPE No.	[1] GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	[2] CODE
1	AN/UYK-30	AN/UYK-30	Comp Cards	AN/UYK-30	Hughes Aircraft Co., Strategic Sys.	HACC
2#	E-6	E-6	Comp Card	E-6	Euroka Oy	EURF
3#	EURO-6	EURO-6	Comp Card	E-6	Euroka Oy	EURF
4	3850	F8	CPU Chip	F8	Fairchild Camera and Instrument Corp.	FSC
5	F38E70DC	F8	Comp Card	F8	Fairchild Camera and Instrument Corp.	FSC
6	F38E70DL	F8	Comp Card	F8	Fairchild Camera and Instrument Corp.	FSC
7	F38E70DM	F8	Comp Card	F8	Fairchild Camera and Instrument Corp.	FSC
8	F38E70PC	F8	Comp Card	F8	Fairchild Camera and Instrument Corp.	FSC
9	F38E70PL	F8	Comp Card	F8	Fairchild Camera and Instrument Corp.	FSC
10	F38E70PM	F8	Comp Card	F8	Fairchild Camera and Instrument Corp.	FSC
11	F3850	F8	CPU Chip	F8	Fairchild Camera and Instrument Corp.	FSC
12	F3870	F8	Comp Chip	F8	Fairchild Camera and Instrument Corp.	FSC
13	MK3850	F8	CPU Chip	F8-MOS	Mostek Corp.	MOS
14	MC3870L	F8	Comp Chip	F8	Motorola Semiconductor Products, Inc.	MOTA
15	MC3870P	F8	Comp Chip	F8	Motorola Semiconductor Products, Inc.	MOTA
16	3850#1	F8	CPU Chip	F8	SGS-ATES Componenti Electtronici(Italy)	SGAI
17#	M3870B1	F8	Comp Chip	F8	SGS-ATES Componenti Electtronici(Italy)	SGAI
18#	M3870D1	F8	Comp Chip	F8	SGS-ATES Componenti Electtronici(Italy)	SGAI
19#	NBF8	F8	Comp Card	F8	SGS-ATES Componenti Electtronici(Italy)	SGAI
20#	NBF8-S	F8	Comp Unit	F8	SGS-ATES Componenti Electtronici(Italy)	SGAI
21	MCPU	F8	CPU Card	MICROLINE	UTEC Corporation	UTE
22	GA16/110	GA16	Comp Card	GA16	General Automation	GEN
23	GA16/220	GA16	Comp Card	GA16	General Automation	GEN
24	IMP16C200	IMP16	CPU Card	IMP16	National Semiconductor Corp.	NSC
25	IMP16C200A	IMP16	CPU Card	IMP16	National Semiconductor Corp.	NSC
26	IMP16C300	IMP16	CPU Card	IMP16	National Semiconductor Corp.	NSC
27	INS8900D	IPC16	CPU Chip	INS8900	National Semiconductor Corp	NSC
28	LSI11/2	LSI11	CPU Card	LSI11	Digital Equipment Corp.	DEC
29	LSI11/23	LSI11	CPU Card	LSI11	Digital Equipment Corp.	DEC
30	H11	LSI11	Comp Unit	H11	Heath Company	HEA
31	MLSI-KD11HA	LSI11	CPU Card	LSI11	MDB Systems, Inc.	MDB
32	MECA43	MECA43	Comp Unit	MECA43	Teledyne Systems Company	TSC
33#	PCA0401	MELCS	Comp Card	MELCS4	Mitsubishi Elect. Corp.	MITJ
34#	PCA0804G01	MELCS	Comp Card	MELCS8/2	Mitsubishi Elect. Corp.	MITJ
35#	PCA0804G02	MELCS	Comp Card	MELCS8/2	Mitsubishi Elect. Corp.	MITJ
36#	PCA8501G01	MELPS	Comp Card	MELPS85/2	Mitsubishi Elect. Corp.	MITJ
37#	PCA8501G02	MELPS	Comp Card	MELPS85/2	Mitsubishi Elect. Corp.	MITJ
38#	MICRAL-M	MICRAL	Comp Unit	MICRAL	R2E-Realisations etudes Electron(France)	R2E
39#	MICRAL-S	MICRAL	Comp Unit	MICRAL	R2E-Realisations etudes Electron(France)	R2E
40	mN601	MICRONOVA	CPU Chip	MICRONOVA	Data General Corp.	DGC
41	mN602	MICRONOVA	CPU Chip	MICRONOVA	Data General Corp.	DGC
42	MBC/1	MICRONOVA	Comp Card	MICRONOVA	Data General Corp.	DGC
43	MICRO1	MICRO1	CPU Card	MICRO1	Microdata Corp.	MID
44	MIPROC16	MIPROC	CPU Card	MIPROC16	Plessey Microsystems	PLM
45	MIPROCF-16	MIPROC	CPU Card	MIPROC16	Plessey Microsystems	PLM
46	MIPROCM-16	MIPROC	CPU Card	MIPROC16	Plessey Microsystems	PLM
47	MPC169	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
48	MPC175	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
49	MPC401	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
50	MPC403	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
51	MPC407	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
52	MPC422	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
53	MPC424	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
54	MPC428	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
55	MPC430	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
56	MPC433	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
57	MPC443	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
58	MPC446	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
59	MPC505	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
60	MPC515	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
61	MPC550	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
62	MPC558	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
63	MPC575	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
64	MPC577	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
65	MPC579	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
66	MPC581	MIPROC	Comp Card	MIPROC16	Plessy Microsystems	PLM
67	MPC641	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
68	MPC725	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
69	MPC818	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
70	MPC862	MIPROC	Comp Card	MIPROC16	Plessy Microsystem	PLM
71#	M58494-XXXP	M58840	CPU Chip	M58840	Mitsubishi Elect. Corp.	MITJ
72#	M58840-XXXP	M58840	CPU Chip	M58840	Mitsubishi Elect. Corp.	MITJ
73	9011-1101	M8	CPU Card	SYSTEM8	Detection Sciences, Inc.	DSI
74	IPC16C100	PACE	CPU Card	IPC16	National Semiconductor Corp.	NSC
75	PBM80M	PBM80	Comp Card	PBM80	Plessy Microsystem	PLM
76#	PMS-500	PM16	Comp Card	PMS-500	Bell and Howell Ltd.(England)	BAHB
77#	TFK10660	PPS4	CPU Chip	PPS4	AEG-Telefunken(West Germany)	ALGG
78	10660	PPS4	CPU Chip	PPS4	Rockwell International Corp.	RKW
79	12660	PPS4	CPU Chip	PPS4	Rockwell International Corp.	RKW
80	MM75	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
81	MM76	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
82	MM76C	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
83	MM76E	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
84	MM76EL2	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
85	MM76EL	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
86	MM76L2	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
87	MM76L	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
88	MM77	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
89	MM77L2	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
90	MM77L	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
91	MM78	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
92	MM78L2	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
93	MM78L	PPS4/1	Comp Chip	PPS4/1	Rockwell International Corp.	RKW
94#	TFK11660	PPS4/2	CPU Chip	PPS4/2	AEG-Telefunken(West Germany)	ALGG
95	11660	PPS4/2	CPU Chip	PPS4/2	Rockwell International Corp.	RKW
96	10806	PPS8	CPU Chip	PPS8	Rockwell International Corp.	RKW
97	11806	PPS8	CPU Chip	PPS8	Rockwell International Corp	RKW
98	12806	PPS8	CPU Chip	PPS8	Rockwell International Corp.	RKW
99	INS8060D	SC/MP	CPU Chip	SC/MP	National Semiconductor Corp	NSC
100	INS8060N	SC/MP	CPU Chip	SC/MP	National Semiconductor Corp	NSC
101	ISP8C100	SC/MP	CPU Card	SC/MP	National Semiconductor Corp.	NSC
102#	ISP-8A/600I#1	SC/MP	CPU Chip	SC/MP-II	N. V. Philips(Netherlands)	PHIN
103	ISP-8A/600I	SC/MP	CPU Chip	SC/MP-II	Signetics Corp.	SIC
104#	ISP-8A/600I#2	SC/MP	CPU Chip	SC/MP-II	Valvo (Germany)	VALG
105#	SYNTE-2	SYNTE-2	Comp Card	SYNTE-2	Euroka Oy	EURF
106	SYSTEM10	SYSTEM10	Comp Unit	SYSTEM10	Tandy Computers	TAN
107	SYSTEM150	SYSTEM150	Comp Unit	SYSTEM150	Tandy Computers	TAN
108	SN54LS481J	S481	CPU Chip	S481	Texas Instruments, Inc.	TII
109	SN74LS481J	S481	CPU Chip	S481	Texas Instruments, Inc.	TII
110	SN74LS481N	S481	CPU Chip	S481	Texas Instruments, Inc.	TII

Microcomputer / Microprocessor
GENERIC SYSTEM INDEX

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IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE & (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	[3] INDIVIDUAL PROCESSOR TYPE No.	[1] GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	[2] CODE
1	SN74S481J	S481	CPU Chip	S481	Texas Instruments, Inc.	TII
2	SN74S481N	S481	CPU Chip	S481	Texas Instruments, Inc.	TII
3	TDY52B	TDY52B	Single Comp	TDY52B	Teledyne Systems Company	TSC
4	TM990/189	TM990	Comp Card	9900	Texas Instruments Inc.	TII
5	TM990/201-41	TM990	Comp Card	9900	Texas Instruments Inc.	TII
6	TM990/201-42	TM990	Comp Card	9900	Texas Instruments Inc.	TII
7	TM990/201-43	TM990	Comp Card	9900	Texas Instruments Inc.	TII
8	TM990/203-21	TM990	Comp Card	9900	Texas Instruments Inc.	TII
9	TM990/203-22	TM990	Comp Card	9900	Texas Instruments Inc.	TII
10	TM990/203-23	TM990	Comp Card	9900	Texas Instruments Inc.	TII
11	TM990/206-41	TM990	Comp Card	9900	Texas Instruments Inc.	TII
12	TM990/206-42	TM990	Comp Card	9900	Texas Instruments Inc.	TII
13	TM990/305	TM990	Comp Card	9900	Texas Instruments Inc.	TII
14	TM990/1001	TM990	Comp Card	9900	Texas Instruments Inc.	TII
15	TM990/1240R	TM990	Comp Card	9900	Texas Instruments Inc.	TII
16	TM990/1241R	TM990	Comp Card	9900	Texas Instruments Inc.	TII
17	TM990/1241S	TM990	Comp Card	9900	Texas Instruments Inc.	TII
18	TM990/1243	TM990	Comp Card	9900	Texas Instruments Inc.	TII
19	XMC360	XMC360	Comp Card	XMC360	Xecon Associates	XEC
20	SyZ8-01MCCCS	Z8	CPU Chip	Z8	Synertek Inc	SYK
21	SyZ8-01MCCPS	Z8	CPU Chip	Z8	Synertek Inc	SYK
22	SyZ8-02MCECS	Z8	CPU Chip	Z8	Synertek Inc	SYK
23	Z8	Z8	Comp Chip	Z8	Zilog Microcomputers	ZIL
24	Z8-01MCCCS	Z8	CPU Chip	Z8	Zilog Microcomputers	ZIL
25	Z8-01MCCPS	Z8	CPU Chip	Z8	Zilog Microcomputers	ZIL
26	Z8-02MPDQS	Z8	CPU	Z8	Zilog Microcomputers A	ZIL
27	Z8-03MCECS	Z8	CPU	Z8	Zilog Microcomputers	ZIL
28	CSS-1143	Z80	Comp Card	CSS-1143	Control Logic, Inc	CLI
29	CS2	Z80	Comp Unit	Z2	Cromemco Inc	CRO
30	CS3	Z80	Comp Unit	Z2	Cromemco Inc	CRO
31	SCC-K	Z80	Comp Card	Z2	Cromemco Inc	CRO
32	SCC-W	Z80	Comp Card	Z2	Cromemco Inc	CRO
33	Z2	Z80	Comp Unit	Z2	Cromemco Inc	CRO
34	Z2D	Z80	Comp Unit	Z2	Cromemco Inc	CRO
35	ZPU-K	Z80	CPU Card	Z2	Cromemco Inc	CRO
36	ZPU-W	Z80	CPU Card	Z2	Cromemco Inc	CRO
37	TDG-Z80CPU	Z80	CPU Card	TDGZ80SYS	The Digital Group, Inc.	DIG
38	TDGMAIN1	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
39	TDGMAIN2	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
40	TDGMAIN3	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
41	TDGMAIN4	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
42	TDGMAIN5	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
43	TDGMASTER1	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
44	TDGMASTER2	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
45	TDGMASTER3	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
46	TDGMASTER4	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
47	TDGSYS1A	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
48	TDGSYS2A	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
49	TDGSYS3A	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
50	TDGSYS4A	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
51	TDGSYS6A	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
52	TDGSYSHAM	Z80	Comp Unit	TDGZ80SYS	The Digital Group, Inc.	DIG
53	BC1-1	Z80	Comp Card	DB8/1	Dynabyte, Inc	DYB
54	DB8/1	Z80	Comp Unit	DB8/1	Dynabyte, Inc	DYB
55	DB8/2-1	Z80	Comp Unit	DB8/1	Dynabyte, Inc	DYB
56	DB8/2-2	Z80	Comp Unit	DB8/1	Dynabyte, Inc	DYB
57	PZ81	Z80	Comp Card	DB8/1	Dynabyte, Inc	DYB
58	PZ81-1	Z80	Comp Card	DB8/1	Dynabyte, Inc	DYB
59	INNOVATOR	Z80	Comp Card	INNOVATOR	Educational Data Systems	EDS
60	MICROCONTROL/10MODZ80	Z80	Comp Unit	MSZ80	Futuredata Computer Corp.	FCC
61	MICROSYSTEM/10MODZ80	Z80	Comp Unit	MSZ80	Futuredata Computer Corp.	FCC
62	MICROSYSTEM/12MODZ80	Z80	Comp Unit	MSZ80	Futuredata Computer Corp.	FCC
63	MICROSYSTEM/15MODZ80	Z80	Comp Unit	MSZ80	Futuredata Computer Corp.	FCC
64	MICROSYSTEM/20MODZ80	Z80	Comp Unit	MSZ80	Futuredata Computer Corp.	FCC
65	MICROSYSTEM/30MODZ80	Z80	Comp Unit	MSZ80	Futuredata Computer Corp.	FCC
66	MICROSYSTEM/31MODZ80	Z80	Comp Unit	MSZ80	Futuredata Computer Corp.	FCC
67	MICROSYSTEM/32MODZ80	Z80	Comp Unit	MSZ80	Futuredata Computer Corp.	FCC
68	MLZ800	Z80	Comp Unit	MLZ80	Heurikon Corp.	HEu
69	ADAM12	Z80	Comp Card	MLZ-DAQ	Heurikon Corp.	HEU
70	ADAM100	Z80	Comp Card	MLZ-DAQ	Hughes Aircraft Corp.	HEU
71	MLZ80	Z80	Comp Card	MLZ80	Heurikon Corp.	HEU
72	MLZ80A	Z80	Comp Card	MLZ80	Heurikon Corp.	HEU
73	MLZ800A	Z80	Comp Unit	MLZ80	Heurikon Corp.	HEU
74	AT481	Z80	CPU Card	MIKE8	Martin Research	MAR
75	MIKE8	Z80	Comp Cards	MIKE8	Martin Research	MAR
76	MD-SBC1	Z80	Comp Card	Z80-MOS	Mostek Corp.	MOS
77	MK77851	Z80	Comp Card	Z80-MOS	Mostek Corp.	MOS
78	MK78121	Z80	Comp Card	Z80-MOS	Mostek Corp.	MOS
79	MK78123	Z80	Comp Card	Z80-MOS	Mostek Corp.	MOS
80	MK78125	Z80	Comp Unit	Z80-MOS	Mostek Corp.	MOS
81	MSC8001-Z80	Z80	Comp Card	MSC8001-Z80	Monolithic Systems Corp.	MSCC
82#	NASCOMI	Z80	Comp Unit	NASCOM I	Nascom Microcomputers Ltd(England)	NASB
83	uPDZ80	Z80	CPU Chip	uCOM-8	NEC Microcomputers Inc.	NECM
84	HORIZON-1	Z80	Comp Unit	HORIZON-1	North Star Computers, Inc.	NOR
85	HORIZON-2	Z80	Comp Unit	HORIZON-1	North Star Computers, Inc	NOR
86	ZPB-A	Z80	CPU Card	HORIZON-1	North Star Computers, Inc	NOR
87	PCS1880	Z80	Comp Card	PCS1880	Process Computer Systems, Inc	PCS
88	PCS1880A	Z80	Comp Card	PCS1880	Process Computer Systems, Inc	PCS
89	7803	Z80	CPU Card	7000	Pro-Log Corp.	PRO
90	QUAY80AI	Z80	Comp Cards	QUAY8000	Quay Corp.	QUY
91	QUAY80AI/TB	Z80	Comp Cards	QUAY8000	Quay Corp.	QUY
92	QUAY90MPS	Z80	Comp Card	QUAY90MPS	Quay Corp.	QUY
93	QUAY94MPS	Z80	Comp Card	QUAY90MPS	Quay Corp.	QUY
94	QUAY8000	Z80	Comp Unit	QUAY8000	Quay Corp.	QUY
95	TRS-80-4K	Z80	Comp Unit	TRS-80	Radio Shack	RAD
96	TRS-80-4KB	Z80	Comp Unit	TRS-80	Radio Shack	RAD
97	TRS-80-16K	Z80	Comp Unit	TRS-80	Radio Shack	RAD
98	TRS-80-26-1001	Z80	Comp Unit	TRS-80	Radio Shack	RAD
99	TRS-80-26-1003	Z80	Comp Unit	TRS-80	Radio Shack	RAD
100	TRS-80-26-1004	Z80	Comp Unit	TRS-80	Radio Shack	RAD
101	TRS-80-26-1006	Z80	Comp Unit	TRS-80	Radio Shack	RAD
102	TRS-80-32K	Z80	Comp Unit	TRS-80	Radio Shack	RAD
103	REXZ-110	Z80	Comp Unit	REXZ-110	Realistic Controls Corp.	RLC
104#	CLZ80-4	Z80	Comp Card	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
105#	CLZ80-4/2	Z80	Comp Card	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
106#	CLZ80-4/8	Z80	Comp Card	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
107#	CLZ80-16	Z80	Comp Card	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
108#	CLZ80-16/2	Z80	Comp Card	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
109#	CLZ80-16/8	Z80	Comp Card	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI

Microcomputer / Microprocessor
GENERIC SYSTEM INDEX

The microcomputer/microprocessor GENERIC SYSTEM INDEX relates microprocessor and microcomputer hardware from individual manufacturers to familiar family "generic numbers". The GENERIC I.D. column links microcomputer CHIPS, CARDS and SYSTEMS from all sources with industry-recognized "generic numbers".

IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE & (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	3 INDIVIDUAL PROCESSOR TYPE No.	1 GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	2 CODE
1#	NBZ80	Z80	Comp Card	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
2#	NBZ80-S	Z80	Comp Unit	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
3#	Z80-CPUB1	Z80	CPU Chip	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
4#	Z80-CPUD1	Z80	CPU Chip	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
5#	Z80A-CPUB1	Z80	CPU Chip	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
6#	Z80A-CPUD1	Z80	CPU Chip	Z80	SGS-ATES Componenti Electtronici(Italy)	SGAI
7	SIA-2350	Z80	Comp Unit	Z80	System Integration Associates	SIA
8	SIA-3500	Z80	Comp Unit	Z80	System Integration Associates S	SIA
9	CB2	Z80	CPU Card	SSM-S100	SSM	SSM
10	VECTORMZ80CPU	Z80	CPU Card	VECTORMZ	Vector Graphic INC	VGI
11	VECTORMZ	Z80	Comp Unit	VECTORMZ	Vector Graphic Inc	VGI
12	ALPHA1	Z80	Comp Unit	ALPHA	Xitan Inc.	XIT
13	ALPHA1.5	Z80	Comp Unit	ALPHA	Xitan Inc.	XIT
14	ALPHA2	Z80	Comp Unit	ALPHA	Xitan Inc.	XIT
15	ALPHA3	Z80	Comp Unit	ALPHA	Xitan Inc.	XIT
16	ALPHA4	Z80	Comp Unit	ALPHA	Xitan Inc.	XIT
17	ALPHA5	Z80	Comp Unit	ALPHA	Xitan Inc.	XIT
18	ALPHA5PLUS	Z80	Comp Unit	ALPHA	Xitan Inc.	XIT
19	ZPU	Z80	CPU Card	ALPHA	Xitan Inc.	XIT
20	MCZ-1/05	Z80	Comp Unit	MCZ	Zilog Microcomputers	ZIL
21	MCZ-1/10	Z80	Comp Unit	MCZ	Zilog Microcomputers	ZIL
22	MCZ-1/20	Z80	Comp Unit	MCZ	Zilog Microcomputers	ZIL
23	MCZ-1/25	Z80	Comp Unit	MCZ	Zilog Microcomputers	ZIL
24	MCZ-1/30	Z80	Comp Unit	MCZ	Zilog Microcomputers	ZIL
25	PDS	Z80	Comp Unit	PDS	Zilog Microcomputers	ZIL
26	Z80-CPUCE	Z80	CPU Chip	Z80	Zilog Microcomputers	ZIL
27	Z80-CPUCM	Z80	CPU Chip	Z80	Zilog Microcomputers	ZIL
28	Z80-CPUCS	Z80	CPU Chip	Z80	Zilog Microcomputers	ZIL
29	Z80-CPUPS	Z80	CPU Chip	Z80	Zilog Microcomputers	ZIL
30	Z80-MCB4	Z80	Comp Card	Z80	Zilog Microcomputers	ZIL
31	Z80-MCB16	Z80	Comp Card	Z80	Zilog Microcomputers	ZIL
32	Z80A-CPUCE	Z80	CPU Chip	Z80	Zilog Microcomputers	ZIL
33	Z80A-CPUCM	Z80	CPU Chip	Z80	Zilog Microcomputers	ZIL
34	Z80A-CPUCS	Z80	CPU Chip	Z80	Zilog Microcomputers	ZIL
35	Z80A-CPUPS	Z80	CPU Chip	Z80	Zilog Microcomputers	ZIL
36	ZDS/H	Z80	Comp Unit	ZDS	Zilog Microcomputers	ZIL
37	ZDS/U	Z80	Comp Unit	ZDS	Zilog Microcomputers	ZIL
38▼#	ZBC80	Z80A	CPU Card	Z80	MATROX ELECTRONIC SYSTEMS	MATC
39▼#	Z8001CPUD1	Z8000	CPU Chip	Z8000	SGS-ATES Componenti Electtronici (Italy)	SGAI
40▼#	Z8002CPUD1	Z8000	CPu Chip	Z8000	SGS-ATES Componenti Electtronici (Italy)	SGAI
41	Z8001CPU	Z8000	CPU	Z8000	Zilog Microcomputers	ZIL
42	Z8002CPU	Z8000	CPU	Z8000	Zilog Microcomputers	ZIL
43	SBP0400ACJ	0400	CPU Chip	SBP0400	Texas Instruments, Inc	TII
44	SBP0400ACN	0400	CPU Chip	SBP0400	Texas Instruments, Inc	TII
45	SBP0400AMJ	0400	CPU Chip	SBP0400	Texas Instruments, Inc	TII
46	SBP0400C	0400	CPU Chip	SBP0400	Texas Instruments, Inc	TII
47	SBP0400M	0400	CPU Chip	SBP0400	Texas Instruments, Inc	TII
48	SBP0401ACJ	0400	CPU Chip	SBP0400	Texas Instruments, Inc	TII
49	SBP0401ACN	0400	CPU Chip	SBP0400	Texas Instruments, Inc	TII
50	SBP0401AMJ	0400	CPU Chip	SBP0400	Texas Instruments, Inc	TII
51	TMS1000	1000	Comp Chip	TMS1000	Texas Instruments, Inc.	TII
52	MDT1004	1004	Comp Unit	MDT1004	Synertek Inc	SYK
53	MDT1008	1008	Comp Unit	MDT1008	Synertek Inc	SYK
54	MDT1016	1016	Comp Unit	MDT1016	Synertek Inc	SYK
55	TMS1070	1070	Comp Chip	TMS1000	Texas Instruments, Inc.	TII
56	MC10800	10800	CPU Chip	M10800	Motorola Semiconductor Products Inc.	MOTA
57	MC10800M	10800	CPU Chip	M10800	Motorola Semiconductor Products Inc.	MOTA
58	TMS1100	1100	Comp Chip	TMS1000	Texas Instruments, Inc.	TII
59	TMS1200	1200	Comp Chip	TMS1000	Texas Instruments, Inc.	TII
60	TMS1270	1270	Comp Chip	TMS1000	Texas Instruments, Inc.	TII
61	TMS1300	1300	Comp Chip	TMS1000	Texas Instruments, Inc.	TII
62#	MN1400	1400	Comp Chip	MN1400	Matsushita Electronics Corp.(Japan)	MATJ
63#	MN1402	1400	Comp Chip	MN1400	Matsushita Electronics Corp.(Japan)	MATJ
64#	MN1403	1400	Comp Chip	MN1400	Matsushita Electronics Corp. (Japan)	MATJ
65#	MN1404	1400	Comp Chip	MN1400	Matsushita Electronics Corp.(Japan)	MATJ
66#	MN1405	1400	Comp Chip	MN1400	Matsushita Electronics Corp.(Japan)	MATJ
67#	MN1430	1400	Comp Chip	MN1400	Matsushita Electronics Corp.(Japan)	MATJ
68#	MN1432	1400	Comp Chip	MN1400	Matsushita Electronics Corp. (Japan)	MATJ
69#	MN1435	1400	Comp Chip	MN1400	Matsushita Electronics Corp. (Japan)	MATJ
70#	MN1450	1400	Comp Chip	MN1400	Matsushita Electronics Corp. (Japan)	MATJ
71#	MN1453	1400	Comp Chip	MN1400	Matsushita Electronics Corp.(Japan)	MATJ
72#	MN1454	1400	Comp Chip	MN1400	Matsushita Electronics Corp (Japan)	MATJ
73#	MN1455	1400	Comp Chip	MN1400	Matsushita Electronics Corp (Japan)	MATJ
74#	MN1498	1400	CPU Chip	MN1400	Matsushita Electronics Corp.(Japan)	MATJ
75#	MN1499	1400	CPU Chip	MN1400	Matsushita Electronics Corp.(Japan)	MATJ
76#	MN1499A	1400	CPU Chip	MN1400	Matsushita Electronics Corp.(Japan)	MATJ
77	MC141000L	141000	Comp Chip	MC141000	Motorola Semiconductor Products, Inc.	MOTA
78	MC141000P	141000	Comp Chip	MC141000	Motorola Semiconductor Products, Inc.	MOTA
79	MC141099L	141099	Comp Chip	MC141099	Motorola Semiconductor Products, Inc	MOTA
80	MC141099P	141099	Comp Chip	MC141099	Motorola Semiconductor Products, Inc	MOTA
81	MC141200L	141200	Comp Chip	MC141000	Motorola Semiconductor Products, Inc.	MOTA
82	MC141200P	141200	Comp Chip	MC141000	Motorola Semiconductor Products, Inc.	MOTA
83	MC14500BAL	14500	CPU Chip	MC14500B	Motorola Semiconductor Products, Inc	MOTA
84	MC14500BCL	14500	CPU Chip	MC14500B	Motorola Semiconductor Products, Inc	MOTA
85	MC14500BCP	14500	CPU Chip	MC14500B	Motorola Semiconductor Products, Inc	MOTA
86#	MN1542	1500	Comp Chip	MN1500	Matsushita Electronics Corp (Japan)	MATJ
87#	MN1544	1500	Comp Chip	MN1500	Matsushita Electronics Corp (Japan)	MATJ
88#	MN1562	1500	Comp Chip	MN1500	Matsushita Electronics Corp (Japan)	MATJ
89#	MN1564	1500	Comp Chip	MN1500	Matsushita Electronics Corp (Japan)	MATJ
90#	MN1599	1500	Comp Chip	MN1500	Matsushita Electronics Corp (Japan)	MATJ
91	CP1600	1600	CPU Chip	1600	General Instrument Corp.	GIC
92	CP1600A	1600	CPU Chip	1600	General Instrument Corp.	GIC
93	CP1610	1600	CPU Chip	1600	General Instrument Corp	GIC
94	GIMINI	1600	Comp Unit	GIMINI	General Instrument Corp	GIC
95	GIMINIII	1600	Comp Unit	GIMINI	General Instrument Corp	GIC
96	MC1600	1600	CPU Card	1600	General Instrument Corp.	GIC
97	MC1610	1600	CPU Chip	GIMINI	General Instrument Corp	GIC
98#	CP1610#1	1600	CPU Chip	1600	General Instrument Corp.(England)	GICB
99#	GIMINI#1	1600	Comp Unit	GIMINI	General Instrument Corp.(England)	GICB
100#	GIMINIII#1	1600	Comp Unit	GIMINI	General Instrument Corp.(England)	GICB
101	MC1600#1	1600	CPU Card	1600	General Instrument Corp.(England)	GICB
102#	MC1610#1	1600	Cpu Chip	GIMINI	General Instrument Corp.(England)	GICB
103	MCP1600	1600	CPU Chips	MCP1600	Western Digital Corp.	WDC
104	MP1600	1600	CPU Chips	MP1600	Western Digital Corp.	WDC
105#	CPUA	1610	CPU Card	PFL16A	Panafacom, Ltd.(Japan)	PAFJ
106#	CPUOPA	1610	CPU Card	PFL16A	Panafacom, Ltd.(Japan)	PAFJ
107#	MN1610	1610	CPU Chip	PFL16A	Panafacom, Ltd.(Japan)	PAFJ
108#	OBC1A	1610	Comp Card	PFL16A	Panafacom, Ltd.(Japan)	PAFJ
109#	OBC2A	1610	Comp Card	PFL16A	Panafacom, Ltd.(Japan)	PAFJ
110#	OBC3A	1610	Comp Card	PFL16A	Panafacom, Ltd.(Japan)	PAFJ

Microcomputer / Microprocessor
GENERIC SYSTEM INDEX

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IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE & (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	[3] INDIVIDUAL PROCESSOR TYPE No.	[1] GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	[2] CODE
1#	PIC1645	1650	Comp Chip	PIC1650	General Instrument Corp.	GIC
2	PIC1650	1650	Comp Chip	PIC1650	General Instrument Corp.	GIC
3	PIC1654	1650	Comp Chip	PIC1650	General Instrument Corp.	GIC
4	PIC1655	1650	Comp Chip	PIC1650	General Instrument Corp.	GIC
5	PIC1670	1650	Comp Chip	PIC1650	General Instrument Corp.	GIC
6#	PIC1645#1	1650	Comp Chip	PIC1650	General Instrument Corp.(England)	GICB
7	PIC1650#1	1650	Comp Chip	PIC1650	General Instrument Corp.(England)	GICB
8	PIC1655#1	1650	Comp Chip	PIC1650	General Instrument Corp.(England)	GICB
9	PIC1670#1	1650	Comp Chip	PIC1650	General Instrument Corp.(England)	GICB
10#	MN1651	1650	CPU Chip	PFL16A	Matsushita Electronics Corp.(Japan)	MATJ
11#	PIC1654#1	1654	COMP Chip	PIC1650	General Instrument Corp.(England)	GICB
12	HCMP1802CD	1800	CPU Chip	HCMP1802	Hughes Aircraft Co.	HAC
13	HCMP1802D	1800	CPU Chip	HCMP1802	Hughes Aircraft Co.	HAC
14	HCMP1836D	1800	CPU Chip	HCMP1836	Hughes Aircraft Co.	HAC
15	UC1800	1800	Comp Unit	UC1800	Infinite, Inc.	INF
16▼	CDP18S602	1800	Comp Card	CDP1800	RCA Corp	RCA
17▼	CDP18S603	1800	Comp Card	CDP1800	RCA Corp	RCA
18▼	CDP18S604	1800	Comp Card	CDP1800	RCA Corp	RCA
19	CDP1802CD	1800	CPU Chip	CDP1800	RCA Corp.	RCA
20	CDP1802D	1800	CPU Chip	CDP1800	RCA Corp.	RCA
21	CDP1804CD	1800	CPU Chip	CDP1800	RCA Corp	RCA
22	CDP1804CE	1800	CPU Chip	CDP1800	RCA Corp	RCA
23	CDP1804D	1800	CPU Chip	CDP1800	RCA Corp	RCA
24	CDP1804E	1800	CPU Chip	CDP1800	RCA Corp	RCA
25	SCP1802	1800	CPU Chip	SCP1802	Solid State Scientific Inc.	SSS
26	SCP1802L	1800	CPU Chip	SCP1802	Solid State Scientific Inc.	SSS
27	CR1872	1872	Comp Chip	CR1872	Western Digital Corp.	WDC
28	CR1872B	1872	Comp Chip	CR1872B	Western Digital Corp.	WDC
29	S2000	2000	Comp Chip	S2000	American Microsystems, Inc.	AMI
30	S2000A	2000	Comp Chip	S2000	American Microsystems, Inc.	AMI
31	S2150	2000	Comp Chip	S2000	American Microsystems, Inc.	AMI
32	S2150A	2000	Comp Chip	S2000	American Microsystems, Inc.	AMI
33	S2152	2000	Comp Chip	S2000	American Microsystems Inc	AMI
34	S2200	2000	Comp Chip	S2000	American Microsystems, Inc.	AMI
35	S2200A	2000	Comp Chip	S2000	American Microsystems, Inc.	AMI
36	S2210	2000	Comp Chip	S2000	American Microsystems Inc	AMI
37	S2400	2000	Comp Chip	S2000	American Microsystems, Inc.	AMI
38	S2400A	2000	Comp Chip	S2000	American Microsystems, Inc.	AMI
39	2650#1	2650	CPU Chip	2650	Intersil	INL
40	2650#2	2650	CPU Chip	2650	Mullard Ltd.(England)	MULB
41	2650#3	2650	CPU Chip	2650	N. V. Philips(Netherlands)	PHIN
42#	2650A-1I#1	2650	CPU Chip	2650	N. V. Philips(Netherlands)	PHIN
43#	2650AI#1	2650	CPU Chip	2650	N. V. Philips(Netherlands)	PHIN
44	2650	2650	CPU Chip	2650	Signetics Corp.	SIC
45	2650A-1I	2650	CPU Chip	2650	Signetics Corp.	SIC
46	2650AI	2650	CPU Chip	2650	Signetics Corp.	SIC
47#	2650A-1I#2	2650	CPU Chip	2650	Valvo(Germany)	VALG
48#	2650AI#2	2650	CPU Chip	2650	Valvo(Germany)	VALG
49▼	Am2901BDC	2901	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
50▼	Am2901BDM	2901	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
51▼	Am2901BFM	2901	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
52▼	Am2901BPC	2901	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
53▼	Am2901CDC	2901	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
54▼	Am2901CDM	2901	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
55▼	Am2901CFM	2901	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
56▼	Am2901CPC	2901	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
57	Am2901ADC	2901	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
58	Am2901ADM	2901	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
59	Am2901AFM	2901	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
60	Am2901APC	2901	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
61	Am2901AXC	2901	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
62	Am2901DC	2901	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
63	Am2901DM	2901	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
64	Am2901FM	2901	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
65	Am2901PC	2901	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
66	9409DC	2901	CPU Chip	F2900	Fairchild Camera and Instrument Corp.	FSC
67	9409DM	2901	CPU Chip	F2900	Fairchild Camera and Instrument Corp.	FSC
68	9409PC	2901	CPU Chip	F2900	Fairchild Camera and Instrument Corp.	FSC
69	F2901ADC	2901	CPU Chip	F2900	Fairchild Camera and Instrument Corp	FSC
70	F2901ADM	2901	CPU Chip	F2900	Fairchild Camera and Instrument Corp	FSC
71	F2901APC	2901	CPU Chip	F2900	Fairchild Camera and Instrument Corp	FSC
72	H18	2901	Comp Cards	H18	Hughes Aircraft Co., Strategic Sys.	HACC
73	H18CPU	2901	CPU Card	H18	Hughes Aircraft Co., Strategic Sys.	HACC
74	2901AFM#1	2901	CPU Chip	2900	Monolithics Memories, Inc.	MMI
75	2901AJC	2901	CPU Chip	2900	Monolithics Memories, Inc.	MMI
76	2901AJM	2901	CPU Chip	2900	Monolithics Memories, Inc.	MMI
77	2901ANC	2901	CPU Chip	2900	Monolithics Memories, Inc.	MMI
78	MC2901AFM	2901	CPU Chip	M2900	Motorola Semiconductor Products, Inc	MOTA
79	MC2901ALC	2901	CPU Chip	M2900	Motorola Semiconductor Products, Inc	MOTA
80	MC2901ALM	2901	CPU Chip	M2900	Motorola Semiconductor Products, Inc	MOTA
81	MC2901LC	2901	CPU Chip	M2900	Motorola Semiconductor Products, Inc	MOTA
82	MC2901LM	2901	CPU Chip	M2900	Motorola Semiconductor Products, Inc	MOTA
83	uPB2901	2901	CPU Chip	uPB2900	NEC Microcomputers Inc.	NECM
84	IDM2901A-1	2901	CPU Chip	IDM2900	National Semiconductor Corp	NSC
85	IDM2901A-1DC	2901	CPU Chip	IDM2900	National Semiconductor Corp	NSC
86	IDM2901A-1DM	2901	CPU Chip	IDM2900	National Semiconductor Corp	NSC
87	IDM2901A-1NC	2901	CPU Chip	IDM2900	National Semiconductor Corp	NSC
88	IDM2901ADC	2901	CPU Chip	IDM2900	National Semiconductor Corp	NSC
89	IDM2901ADM	2901	CPU Chip	IDM2900	National Semiconductor Corp	NSC
90	IDM2901AFM	2901	CPU Chip	IDM2900	National Semiconductor Corp	NSC
91	IDM2901APC	2901	CPU Chip	IDM2900	National Semiconductor Corp	NSC
92#	N2901-1#1	2901	CPU Chip	2900	N. V. Philips(Netherlands)	PHIN
93#	N2901-1I	2901	CPU Chip	2900	N. V. Philips(Netherlands)	PHIN
94	2901ADC	2901	CPU Chip	Am2900	Raytheon Co.	RTN
95	2901ADM	2901	CPU Chip	Am2900	Raytheon Co.	RTN
96	2901AFM	2901	CPU Chip	Am2900	Raytheon Co.	RTN
97	2901APC	2901	CPU Chip	Am2900	Raytheon Co.	RTN
98	Am2901DC#1	2901	CPU Chip	Am2900	Raytheon Co.	RTN
99	Am2901DM#1	2901	CPU Chip	Am2900	Raytheon Co.	RTN
100	Am2901FM#1	2901	CPU Chip	Am2900	Raytheon Co.	RTN
101	Am2901PC#1	2901	CPU Chip	Am2900	Raytheon Co.	RTN
102	N2901-1	2901	CPU Chip	2900	Signetics Corp.	SIC
103	N2901-1I#1	2901	CPU Chip	2900	Signetics Corp.	SIC
104#	N2901-1#2	2901	CPU Chip	2900	Valvo (Germany)	VALG
105#	N2901-1I#2	2901	CPU Chip	2900	Valvo (Germany)	VALG
106▼	Am29203DC	2903	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
107▼	Am29203DM	2903	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
108▼	Am29203FM	2903	CPu Chip	Am2900	Advanced Micro Devices Inc.	AMD
109	Am2903DC	2903	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
110	Am2903DM	2903	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV

Microcomputer / Microprocessor
GENERIC SYSTEM INDEX

The microcomputer/microprocessor GENERIC SYSTEM INDEX relates microprocessor and microcomputer hardware from individual manufacturers to familiar family "generic numbers". The GENERIC I.D. column links microcomputer CHIPS, CARDS and SYSTEMS from all sources with industry-recognized "generic numbers".

IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE & (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	[3] INDIVIDUAL PROCESSOR TYPE No.	[1] GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	[2] CODE
1	Am2903FM	2903	CPU Chip	Am2900	Advanced Micro Devices Inc.	AMV
2	MC2903LC	2903	CPU Chip	M2900	Motorola Semiconductor Products, Inc	MOTA
3	MC2903LM	2903	CPU Chip	M2900	Motorola Semiconductor Products, Inc	MOTA
4	C3001,2	3000	CPU Chips	3000	Intel Corp.	ITL
5	D3001,2	3000	CPU Chips	3000	Intel Corp.	ITL
6	MC3001,2	3000	CPU Chips	3000	Intel Corp.	ITL
7	MD3001,2	3000	CPU Chips	3000	Intel Corp	ITL
8	N3001,2#1	3000	CPU Chips	3000	Mullard Ltd.(England)	MULB
9	N3001,2#2	3000	CPU Chips	3000	N. V. Philips(Netherlands)	PHIN
10#	S3001,2#1	3000	CPU Chips	3000	N. V. Philips(Netherlands)	PHIN
11	N3001,2	3000	CPU Chips	3000	Signetics Corp.	SIC
12	S3001,2	3000	CPU Chips	3000	Signetics Corp.	SIC
13#	S3001,2#2	3000	CPU Chip	3000	Valvo(Germany)	VALG
14#	T3153	3153	CPU Chip	TLCS12	Tokyo Shibaura Electric Co.,Ltd.(Japan)	TOSJ
15#	T3190	3190	CPU Chip	TLCS12A	Tokyo Shibaura Electric Co.,Ltd.(Japan)	TOSJ
16#	T3190-1	3190	CPU Chip	TLCS12A	Tokyo Shibaura Electric Co.,Ltd.(Japan)	TOSJ
17	MK3870	3870	Comp Chip	F8-MOS	Mostek Corp.	MOS
18	MK97400	3870	Comp Chip	F-8 MOS	Mostek Corp.	MOS
19	MK97401	3870	Comp Chip	F-8 MOS	Mostek Corp.	MOS
20	MK97402	3870	Comp Chip	F-8 MOS	Mostek Corp.	MOS
21	MK97403	3870	Comp Chip	F-8 MOS	Mostek Corp.	MOS
22	MK97404	3870	Comp Chip	F-8 MOS	Mostek Corp.	MOS
23	MK97405	3870	Comp Chip	F-8 MOS	Mostek Corp.	MOS
24	MKB3870P	3870	Comp Chip	F-8 MOS	Mostek Corp.	MOS
25	MC3870	3870	Comp Chip	MC3870	Motorola Semiconductor Products, Inc	MOTA
26	MK3872	3872	Comp Chip	F8-MOS	Mostek Corp.	MOS
27	MK3876	3876	Comp Chip	F8-MOS	Mostek Corp.	MOS
28	MK3880	3880	CPU Chip	Z80-MOS	Mostek Corp.	MOS
29#	HMCS42	40 Series	Comp Chip	HMCS40	Hitachi Ltd.(Japan)	HITJ
30#	HMCS42C	40 Series	Comp Chip	HMCS40	Hitachi Ltd(Japan)	HITJ
31#	HMCS43	40 Series	Comp Chip	HMCS40	Hitachi Ltd.(Japan)	HITJ
32#	HMCS43C	40 Series	Comp Chip	HMCS40	Hitachi Ltd.(Japan)	HITJ
33#	HMCS44	40 Series	Comp Chip	HMCS40	Hitachi Ltd.(Japan)	HITJ
34#	HMCS44A	40 Series	Comp Chip	HMCS40	Hitachi Ltd(Japan)	HITJ
35#	HMCS44C	40 Series	Comp Chip	HMCS40	Hitachi Ltd(Japan)	HITJ
36#	HMCS45	40 Series	Comp Chip	HMCS40	Hitachi Ltd.(Japan)	HITJ
37#	HMCS45A	40 Series	Comp Chip	HMCS40	Hitachi Ltd(Japan)	HITJ
38#	HMCS45C	40 Series	Comp Chip	HMCS40	Hitachi Ltd(Japan)	HITJ
39	9007-1100	4004	CPU Card	SYSTEM4	Detection Sciences, Inc.	DSI
40	C4004	4004	CPU Chip	MCS4	Intel Corp.	ITL
41	D4004	4004	CPU Chip	MCS4	Intel Corp.	ITL
42	imm4-42	4004	CPU Card	MCS4,40	Intel Corp.	ITL
43	P4004	4004	CPU Chip	MCS4	Intel Corp.	ITL
44	INS4004	4004	CPU Chip	FIPS	National Semiconductor Corp.	NSC
45	4111	4004	CPU Card	PLS-400	Pro-Log Corp.	PRO
46	COP402	402	Comp Chip	COP400	National Semiconductor Corp	NSC
47	40-000	4040	CPU Card	IMC40	Comptrol Inc.	COM
48	40-001	4040	CPU Card	IMC40	Comptrol Inc.	COM
49	40-002	4040	CPU Card	IMC40	Comptrol Inc.	COM
50	40-003	4040	CPU Card	IMC40	Comptrol Inc.	COM
51	40-004	4040	CPU Card	IMC40	Comptrol Inc.	COM
52	40-005	4040	CPU Card	IMC40	Comptrol Inc.	COM
53	9007-1110	4040	CPU Card	SYSTEM4	Detection Sciences, Inc.	DSI
54	9007-1120	4040	CPU Card	SYSTEM4	Detection Sciences, Inc.	DSI
55	C4040	4040	CPU Chip	MCS40	Intel Corp.	ITL
56	imm4-43	4040	CPU Card	MCS4,40	Intel Corp.	ITL
57	P4040	4040	CPU Chip	MCS40	Intel Corp.	ITL
58	COP410L	410L	Comp Chip	COP400	National Semiconductor Corp	NSC
59	COP411L	411L	Comp Chip	COP400	National Semiconductor Corp	NSC
60	COP420	420	Comp Chip	COP400	National Semiconductor Corp	NSC
61	COP420L	420L	Comp Chip	COP400	National Semiconductor Corp	NSC
62	WD4020A	4200	Comp Chip	WD4200	Western Digital Corporation	WDC
63	WD4020B	4200	Comp Chip	WD4200	Western Digital Corporation	WDC
64	WD4200E	4200	Comp Chip	WD4200	Western Digital Corporation	WDC
65	WD4200F	4200	Comp Chip	WD4200	Western Digital Corporation	WDC
66	WD4210E	4200	Comp Chip	WD4200	Western Digital Corporation	WDC
67	WD4210F	4200	Comp Chip	WD4200	Western Digital Corporation	WDC
68	4705BDC	4705	CPU Chip	4700	Fairchild Camera and Instrument Corp.	FSC
69	4705BDM	4705	CPU Chip	4700	Fairchild Camera and Instrument Corp.	FSC
70	4705BFC	4705	CPU Chip	4700	Fairchild Camera and Instrument Corp.	FSC
71	4705BFM	4705	CPU Chip	4700	Fairchild Camera and Instrument Corp.	FSC
72	4705BPC	4705	CPU Chip	4700	Fairchild Camera and Instrument Corp.	FSC
73#	uPD541C	541	CPU Chip	uCOM-41	Nippon Electric Co., Ltd.(Japan)	NECJ
74#	uPD545C	545	Comp Chip	uCOM-4	NEC Electronics(West Germany)	NECD
75	uPD545C#1	545	Comp Chip	uCOM-4	Nippon Electric Co., Ltd.(Japan)	NECJ
76	uPD546C#1	546	Comp Chip	uCOM-4	NEC Electronics(West Germany)	NECD
77#	uPD546C	546	Comp Chip	uCOM-4	Nippon Electric Co., Ltd.(Japan)	NECJ
78	uPD546C#2	546	Comp Chip	uCOM-4	NEC Microcomputers, Inc.	NECM
79#	uPD547C	547	Comp Chip	uCOM-4	Nippon Electric Co., Ltd.(Japan)	NECJ
80#	uPD547LC	547	Comp Chip	uCOM-4,44	Nippon Electric Co., Ltd.(Japan)	NECJ
81	uPD547C#1	547	Comp Chip	uCOM-4	NEC Microcomputers, Inc.	NECM
82#	uPD548C	548	Comp Chip	uCOM-4	Nippon Electric Co., Ltd.(Japan)	NECJ
83	uPD548C#1	548	Comp Chip	uCOM-4	NEC Microcomputers, Inc.	NECM
84#	uPD550LC	550	Comp Chip	uCOM-45C	Nippon Electric Co., Ltd. (Japan)	NECJ
85	uPD550C	550	Comp Chip	uCOM-4	NEC Microcomputers, Inc.	NECM
86	uPD551C	551	Comp Chip	uCOM-43	NEC Microcomputers, Inc.	NECM
87	uPD552C	552	Comp Chip	uCOM-43	NEC Microcomputers, Inc.	NECM
88	uPD553C	553	Comp Chip	uCOM-43	NEC Microcomputers, Inc.	NECM
89#	uPD554C	554	Comp Chip	uCOM-4,45	Nippon Electric Co., Ltd.(Japan)	NECJ
90#	uPD554LC	554	Comp Chip	uCOM-45C	Nippon Electric Co., Ltd. (Japan)	NECJ
91	uPD557LC	557	CPU Chip	uCOM-43	NEC Microcomputers Inc.	NECM
92	MMI5701	5701	Comp Chip	5701	Monolithics Memories, Inc.	MMI
93	MM57140N	57140	Comp Chip	COPS57100	National Semiconductor Corp	NSC
94	MM57152N	57152	Comp Chip	COPS57100	National Semiconductor Corp	NSC
95	MM5782N	5782	CPU Chip	COPS57100	National Semiconductor Corp	NSC
96	MM5799N	5799	Comp Chip	COPS57100	National Semiconductor Corp	NSC
97	HB6100	6100	Comp Card	HM6100	Harris Semiconductor	HAS
98	HM6100-2	6100	CPU Chip	HM6100	Harris Semiconductor	HAS
99	HM6100-9	6100	CPU Chip	HM6100	Harris Semiconductor	HAS
100	HM6100A-2	6100	CPU Chip	HM6100	Harris Semiconductor	HAS
101	HM6100A-9	6100	CPU Chip	HM6100	Harris Semiconductor	HAS
102	HM6100C-5	6100	CPU Chip	HM6100	Harris Semiconductor	HAS
103	IM6100-1IDL	6100	CPU Chip	6100	Intersil	INL
104	IM6100-1IPL	6100	CPU Chip	6100	Intersil	INL
105	IM6100-1MDL	6100	CPU Chip	6100	Intersil	INL
106	IM6100AIDL	6100	CPU Chip	6100	Intersil	INL
107	IM6100AIPL	6100	CPU Chip	6100	Intersil	INL
108	IM6100AMDL	6100	CPU Chip	6100	Intersil	INL
109	IM6100IPL	6100	CPU Chip	6100	Intersil	INL
110	12010	6100	CPU Card	PCM-12A	PC/M, Inc.	PCM

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GENERIC SYSTEM INDEX

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IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE & (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	[3] INDIVIDUAL PROCESSOR TYPE No.	[1] GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	[2] CODE
1	uPD650C	650	Comp Chip	uCOM-43	NEC Microcomputers, Inc.	NECM
2	Seven-X	6500	Comp Unit	Seven-X	ECD Corp.	ECD
3	SYC6500/1	6500	CPU Chip	SY6500	Synertek Inc	SYK
4	SYC6500/1A	6500	CPU Chip	SY6500	Synertek Inc	SYK
5	SYP6500/1	6500	CPU Chip	SY6500	Synertek Inc	SYK
6	SYP6500/1A	6500	CPU Chip	SY6500	Synertek Inc	SYK
7	SY6500/1	6500/1	Comp Chip	SY6500/1	Synertek, Inc	SYK
8	A2B0004	6502	Comp Card	APPLEII	Apple Computer Inc	APL
9	A2B0016	6502	Comp Card	APPLEII	Apple Computer Inc	APL
10	A2B0032	6502	Comp Card	APPLEII	Apple Computer Inc	APL
11	A2B0048	6502	Comp Card	APPLEII	Apple Computer Inc	APL
12	A2S0004	6502	Comp Unit	APPLEII	Apple Computer Inc	APL
13	A2S0016	6502	Comp Unit	APPLEII	Apple Computer Inc	APL
14	A2S0032	6502	Comp Unit	APPLEII	Apple Computer Inc	APL
15	A2S0048	6502	Comp Unit	APPLEII	Apple Computer Inc	APL
16	TDG6502	6502	CPU Card	TDG6500SYS	The Digital Group, Inc.	DIG
17	ETC1000A	6502	Comp Unit	ETC1000	Electronic Tool Co.	ETL
18	ETC1000B	6502	Comp Unit	ETC1000	Electronic Tool Co.	ETL
19	ETC1000C	6502	Comp Unit	ETC1000	Electronic Tool Co.	ETL
20	ETC1000D	6502	Comp Unit	ETC1000	Electronic Tool Co.	ETL
21	CP110	6502	CPU Card	SUPER JOLT	Microcomputer Associates, Inc.	MCA
22	MCS6502	6502	CPU Chip	MCS6500	MOS Technology Inc.	MTY
23	C2-0	6502	Comp Card	C2#1	Ohio Scientific, Inc	OHS
24	C2-1	6502	Comp Unit	C2#2	Ohio Scientific, Inc	OHS
25	C2-4P	6502	Comp Unit	C2#2	Ohio Scientific, Inc	OHS
26	C2-8P	6502	Comp Unit	C2#2	Ohio Scientific, Inc	OHS
27	C2-8S	6502	Comp Unit	C2#2	Ohio Scientific, Inc	OHS
28	C2-S1S	6502	Comp Unit	C2#2	Ohio Scientific, Inc	OHS
29	C2-S1V	6502	Comp Unit	C2#2	Ohio Scientific, Inc	OHS
30	C2-S2S	6502	Comp Unit	C2#2	Ohio Scientific, Inc	OHS
31	AIM65	6502	Comp Card	R6500	Rockwell International Corp	RKW
32	R6500/1	6502	Comp Chip	R6500	Rockwell International Corp	RKW
33	R6502	6502	CPU Chip	R6500	Rockwell International Corp.	RKW
34	SY6502	6502	CPU Chip	SY6500	Synertek, Inc.	SYK
35	C3-B	6502,8080,Z80	Comp Unit	C3	Ohio Scientific, Inc	OHS
36	C3-S1	6502,8080,Z80	Comp Unit	C3	Ohio Scientific, Inc	OHS
37	MCS6503	6503	CPU Chip	MCS6500	MOS Technology Inc.	MTY
38	R6503	6503	CPU Chip	R6500	Rockwell International Corp.	RKW
39	SY6503	6503	CPU Chip	SY6500	Synertek, Inc.	SYK
40	MCS6504	6504	CPU Chip	MCS6500	MOS Technology Inc.	MTY
41	R6504	6504	CPU Chip	R6500	Rockwell International Corp.	RKW
42	SY6504	6504	CPU Chip	SY6500	Synertek, Inc.	SYK
43	MCS6505	6505	CPU Chip	MCS6500	MOS Technology Inc.	MTY
44	R6505	6505	CPU Chip	R6500	Rockwell International Corp.	RKW
45	SY6505	6505	CPU Chip	SY6500	Synertek, Inc.	SYK
46	MCS6506	6506	CPU Chip	MCS6500	MOS Technology Inc.	MTY
47	R6506	6506	CPU Chip	R6500	Rockwell International Corp.	RKW
48	SY6506	6506	CPU Chip	SY6500	Synertek, Inc.	SYK
49	MCS6507	6507	CPU Chip	MCS6500	MOS Technology Inc.	MTY
50	R6507	6507	CPU Chip	R6500	Rockwell International Corp.	RKW
51	uPD651C	651	Comp Chip	uCOM-44	NEC Microcomputers, Inc.	NECM
52	uPD651G	651	CPU Chip	uCOM-44	NEC Microcomputers Inc.	NECM
53	MCS6512	6512	CPU Chip	MCS6500	MOS Technology Inc.	MTY
54	R6512	6512	CPU Chip	R6500	Rockwell International Corp.	RKW
55	SY6512	6512	CPU Chip	SY6500	Synertek, Inc.	SYK
56	MCS6513	6513	CPU Chip	MCS6500	MOS Technology Inc.	MTY
57	R6513	6513	CPU Chip	R6500	Rockwell International Corp.	RKW
58	SY6513	6513	CPU Chip	SY6500	Synertek, Inc.	SYK
59	MCS6514	6514	CPU Chip	MCS6500	MOS Technology Inc.	MTY
60	R6514	6514	CPU Chip	R6500	Rockwell International Corp.	RKW
61	SY6514	6514	CPU Chip	SY6500	Synertek, Inc.	SYK
62	MCS6515	6515	CPU Chip	MCS6500	MOS Technology Inc.	MTY
63	R6515	6515	CPU Chip	R6500	Rockwell International Corp.	RKW
64	SY6515	6515	CPU Chip	SY6500	Synertek, Inc.	SYK
65	uPD652C	652	Comp Chip	uCOM-45	NEC Microcomputers, Inc	NECM
66	MMI6701	6701	Comp Chip	6701	Monolithics Memories, Inc.	MMI
67	S68A00	6800	CPU Chip	AMI6800	American Microsystems Inc.	AMI
68	S68B00	6800	CPU Chip	AMI6800	American Microsystems Inc.	AMI
69	S6800	6800	CPU Chip	AMI6800	American Microsystems Inc.	AMI
70	S6802	6800	CPU Chip	AMI6800	American Microsystems Inc	AMI
71	S6802P	6800	CPU Chip	AMI6800	American Microsystems Inc	AMI
72	680	6800	CPU Card	MIKUL600	Control Logic, Inc.	CLI
73	DE68C	6800	Comp Unit	DE68	Digital Electronics Corp.	DECO
74	TDG6800	6800	CPU Card	TDG6800SYS	The Digital Group, Inc.	DIG
75#	DMS	6800	Comp Unit	DMS	Dynalogic Corp., Ltd.(Canada)	DYN
76▼#	EF68A00	6800	CPU Chip	EF6800	E.F.C.I.S.	EFCF
77▼#	EF68B00	6800	CPU Chip	EF6800	E.F.C.I.S.	EFCF
78▼#	EF6800	6800	CPU Chip	EF6800	E.F.C.I.S.	EFCF
79▼#	EF6802	6800	CPU Chip	EF6800	E.F.C.I.S.	EFCF
80▼#	EF6805P2	6800	uCT Chip	EF6800	E.F.C.I.S.	EFCF
81▼#	SFF9-68A09	6800	CPU Chip	SFF-6800	E.F.C.I.S.	EFCF
82▼#	SFF9-68B09	6800	CPU Chip	SFF-6800	E.F.C.I.S.	EFCF
83▼#	SFF9-6809	6800	CPU Chip	SFF-6800	E.F.C.I.S.	EFCF
84	MICRO68	6800	Comp Unit	MICRO68	Electronic Product Associates, Inc.	EPA
85	MICRO68B	6800	Comp Unit	MICRO68B	Electronic Product Associates, Inc.	EPA
86	MICRO68K	6800	Comp Unit	MICRO68	Electronic Product Associates, Inc.	EPA
87#	CPU001	6800	CPU Card	EURO-6	Euroka OY,(Finland)	EURF
88#	CPU010	6800	CPU Card	E-6	Euroka OY,(Finland)	EURF
89	MICROCONTROL/10MOD6800	6800	Comp Unit	MS6800	Futuredata Computer Corp.	FCC
90	MICROSYSTEM/10MOD6800	6800	Comp Unit	MS6800	Futuredata Computer Corp.	FCC
91	MICROSYSTEM/12MOD6800	6800	Comp Unit	MS6800	Futuredata Computer Corp.	FCC
92	MICROSYSTEM/15MOD6800	6800	Comp Unit	MS6800	Futuredata Computer Corp.	FCC
93	MICROSYSTEM/20MOD6800	6800	Comp Unit	MS6800	Futuredata Computer Corp.	FCC
94	MICROSYSTEM/30MOD6800	6800	Comp Unit	MS6800	Futuredata Computer Corp.	FCC
95	MICROSYSTEM/31MOD6800	6800	Comp Unit	MS6800	Futuredata Computer Corp.	FCC
96	MICROSYSTEM/32MOD6800	6800	Comp Unit	MS6800	Futuredata Computer Corp.	FCC
97	F68A00	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC
98	F68A00D	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC
99	F68A02D	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC
100	F68B00	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC
101	F68B00D	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC
102	F68B02D	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC

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LINE No.	[3] INDIVIDUAL PROCESSOR TYPE No.	[1] GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	[2] CODE
1	F6800	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC
2	F6800C	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC
3	F6802D	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC
4	F6802P	6800	CPU Chip	F6800	Fairchild Camera and Instrument Corp.	FSC
5▼#	HD68A09	6800	CPU Chip	HD6800	HITACHI, LTD	HITJ
6▼#	HD68B09	6800	CPU Chip	HD6800	HITACHI, LTD	HITJ
7▼#	HD6801	6800	uCT Chip	HD6800	HITACHI, LTD	HITJ
8▼#	HD6809	6800	CPU Chip	HD6800	HITACHI, LTD	HITJ
9#	HD46800D	6800	CPU Chip	HMCS6800	Hitachi, Ltd. (Japan)	HITJ
10#	HD46802	6800	CPU Chip	HMCS6800	Hitachi, Ltd. (Japan)	HITJ
11#	HD46802P	6800	CPU Chip	HMCS6800	Hitachi, Ltd. (Japan)	HITJ
12▼#	HD68000	6800	CPU Chip	HD68000	HITACHI, LTD	HITJ
13	M68MM02	6800	CPU Card	M6800	Motorola Semiconductor Products, Inc	MOTA
14	M68MM07	6800	CPU Card	M6800	Motorola Semiconductor Products, Inc	MOTA
15	JANM38510/40001BQC	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
16	JANM38510/40001CQC	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
17	MC68A00CL	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
18	MC68A00CP	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
19	MC68A00L	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
20	MC68A00P	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
21	MC68B00L	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
22	MC68B00P	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
23	MC6800BQCS	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
24	MC6800CL	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
25	MC6800CP	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
26	MC6800CQCS	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
27	MC6800L	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
28	MC6800P	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
29	MC6802L	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
30	MC6802P	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
31▼	MC6803	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
32▼	MC6805R2L	6800	uCT Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
33▼	MC6805R2P	6800	uCT Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
34▼	MC6805R2S	6800	uCT Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
35▼	MC6805U2L	6800	uCT Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
36▼	MC6805U2P	6800	uCT Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
37▼	MC6805U2S	6800	uCT Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
38▼	MC68000L4	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
39▼	MC68000L6	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
40▼	MC68701L	6800	Comp Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
41▼	MC146805E2P	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
42▼	MC146805E2S	6800	CPU Chip	M6800	Motorola Semiconductor Products, Inc.	MOTA
43	ALTAIR680B	6800	Comp Unit	ALTAIR680B	PCC Microsystems	PCC
44	8611	6800	CPU Card	MPS-800	Pro-Log Corp.	PRO
45	CMC68/15	6800	Comp Card	CMC68/15	RCI/DATA Div of RE-EL Circuits, Inc	RCI
46	CMC68/15B	6800	Comp Card	CMC68/15	RCI/DATA Div. of RE-EL Circuits, Inc.	RCI
47	CMC68/15C	6800	Comp Card	CMC68/15	RCI/DATA Div of RE-EL Circuits, Inc	RCI
48	CMC68/15G	6800	Comp Card	CMC68/15	RCI/DATA Div. of RE-EL Circuits, Inc	RCI
49	MPA	6800	CPU Card	SWTPC6800	Southwest Technical Products Corp.	STP
50	CM6800	6800	Comp Card	WINCE6800	Wintek Corp.	WTK
51	DUALSYSTEM/10-10	6800,02;8080,85	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
52	DUALSTATION/12	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
53	DUALSYSTEM/12-10	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
54	DUALSYSTEM/12-12	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
55	DUALSYSTEM/15-10	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
56	DUALSYSTEM/15-12	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
57	DUALSYSTEM/15-15	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
58	DUALSYSTEM/20-10	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
59	DUALSYSTEM/20-12	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
60	DUALSYSTEM/20-15	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
61	DUALSYSTEM/20-20	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
62	DUALSYSTEM/31-10	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
63	DUALSYSTEM/31-12	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
64	DUALSYSTEM/31-15	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
65	DUALSYSTEM/31-20	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
66	DUALSYSTEM/31-31	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
67	DUALSYSTEM/32-10	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
68	DUALSYSTEM/32-12	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
69	DUALSYSTEM/32-15	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
70	DUALSYSTEM/32-20	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
71	DUALSYSTEM/32-31	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
72	DUALSYSTEM/32-32	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
73	MICROCONTROL/10MOD6802	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
74	MICROSTATION/12	6800,02;8080,85;Z80	DualCompUnit	MICROSYSTEM	Futuredata Computer Corp.	FCC
75▼#	EF68000	68000	CPU Chip	EF68000	E.F.C.I.S.	EFCF
76	MC68000	68000	CPU Chip	MC68000	Motorola Semiconductor Products, Inc	MOTA
77	MC6801	6801	Comp Chip	MC6801	Motorola Semiconductor Products, Inc	MOTA
78	MC6801EL	6801	Comp Chip	MC6801	Motorola Semiconductor Products, Inc	MOTA
79	MC6801L	6801	Comp Chip	MC6801	Motorola Semiconductor Products, Inc	MOTA
80	MICROSYSTEM/10MOD6802	6802	Comp Unit	MS6802	Futuredata Computer Corp.	FCC
81	MICROSYSTEM/12MOD6802	6802	Comp Unit	MS6802	Futuredata Computer Corp.	FCC
82	MICROSYSTEM/15MOD6802	6802	Comp Unit	MS6802	Futuredata Computer Corp.	FCC
83	MICROSYSTEM/31MOD6802	6802	Comp Unit	MS6802	Futuredata Computer Corp.	FCC
84	MICROSYSTEM/32MOD6802	6802	Comp Unit	MS6802	Futuredata Computer Corp.	FCC
85	MC6803EL	6803	Comp Chip	MC6803	Motorola Semiconductor Products, Inc	MOTA
86	MC6803EP	6803	Comp Chip	MC6803	Motorola Semiconductor Products, Inc	MOTA
87	MC6803L	6803	Comp Chip	MC6803	Motorola Semiconductor Products, Inc	MOTA
88	MC6803P	6803	Comp Chip	MC6803	Motorola Semiconductor Products, Inc	MOTA
89	MC6805L	6805	Comp Chip	MC6805	Motorola Semiconductor Products Inc.	MOTA
90	MC6805P2C	6805	Comp Chip	MC6805	Motorola Semiconductor Products, Inc.	MOTA
91	MC6805P2L	6805	Comp Chip	MC6805	Motorola Semiconductor Products, Inc.	MOTA
92	MC6805P2P	6805	Comp Chip	MC6805	Motorola Semiconductor Product	MOTA
93	MC6805P	6805	Comp Chip	MC6805	Motorola Semiconductor Products Inc.	MOTA
94	MC6808L	6808	CPU Chip	M6800	Motorola Semiconductor Products Inc.	MOTA
95	MC6808P	6808	CPU Chip	M6800	Motorola Semiconductor Products Inc.	MOTA
96	MIKUL6008-2	6808	Comp Card	MIKUL6000	TL Industries	TLI
97	MIKUL6008-3	6808	Comp Card	MIKUL6000	TL Industries	TLI
98	MC68A09EL	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
99	MC68A09EP	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
100	MC68A09L	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
101	MC68A09P	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
102	MC68B09EL	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
103	MC68B09EP	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
104	MC68B09L	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA

Microcomputer / Microprocessor
GENERIC SYSTEM INDEX

The microcomputer/microprocessor GENERIC SYSTEM INDEX relates microprocessor and microcomputer hardware from individual manufacturers to familiar family "generic numbers". The GENERIC I.D. column links microcomputer CHIPS, CARDS and SYSTEMS from all sources with industry-recognized "generic numbers".

IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE
& (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	3 INDIVIDUAL PROCESSOR TYPE No.	1 GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	2 CODE
1	MC68B09P	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
2	MC6809EL	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
3	MC6809EP	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
4	MC6809L	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
5	MC6809P	6809	CPU Chip	M6800	Motorola Semiconductor Products, Inc	MOTA
6	MIKUL6809-1	6809	Comp Card	MIKUL6000	TL Industries	TLI
7	MIKUL6809-2	6809	Comp Card	MIKUL6000	TL Industries	TLI
8	MIKUL6809-3	6809	Comp Card	MIKUL6000	TL Industries	TLI
9	uPD7520	7520	CPU Chip	uCOM 7500	NEC Microcomputers Inc.	NECM
10#	uPD755D	755	CPU Chip	uCOM-16	Nippon Electric Co., Ltd.(Japan)	NECJ
11#	uPD766G	766	Comp Chip	uCOM-47	Nippon Electric Co., Ltd.(Japan)	NECJ
12#	uPD767C	767	Comp Chip	uCOM-83	Nippon Electric Co., Ltd.(Japan)	NECJ
13	uPD768B	768	CPU Chip	uCOM-1600	NEC Microcomputers, Inc.	NECM
14#	uPD780D	780	CPU Chip	uCOM-8	Nippon Electric Co. Ltd.(Japan)	NECJ
15#	uPD780D-1	780	CPU Chip	uCOM-8	Nippon Electric Co. Ltd.(Japan)	NECJ
16	uPD780C	780	CPU Chip	uCOM-8	NEC Microcomputers, Inc.	NECM
17	uPD780C-1	780	CPU Chip	uCOM-8	NEC Microcomputers, Inc.	NECM
18	uPD7801B	7801	CPU Chip	8080A	NEC Microcomputers Inc.	NECM
19	N8X300I	8X300	CPU Chip	N8X300	Signetics Corp.	SIC
20	NSC800	800	CPU Chip	NSC800	National Semiconductor Corp	NSC
21▼	Am95/4006/20	8000	UCT Chip	AMZ8000	Advanced Micro Devices Inc.	AMD
22▼	Am95/4006/21	8000	UCT Chip	AMZ8000	Advanced Micro Devices Inc.	AMD
23▼	Am95/4006/22	8000	UCT Chip	AMZ8000	Advanced Micro Devices Inc.	AMD
24▼	Am95/4006/40	8000	UCT Chip	AMZ8000	Advanced Micro Devices Inc.	AMD
25▼	Am95/4006/41	8000	UCT Chip	AMZ8000	Advanced Micro Devices Inc.	AMD
26▼	Am95/4006/42	8000	UCT Chip	AMZ8000	Advanced Micro Devices Inc.	AMD
27▼	Am95/4010	8000	UCT Chip	AMZ8000	Advanced Micro Devices Inc.	AMD
28▼	Am96/4116	8000	UCT Chip	AMZ8000	Advanced Micro Devices Inc.	AMD
29	LP8000#1	8000	CPU Chip	LP8000	General Instrument Corp.	GIC
30#	LP8000	8000	CPU Chip	LP8000	General Instrument Corp.(England)	GICB
31	LCP593	8008	CPU Cards	L SERIES	Control Logic, Inc.	CLI
32	LCP593-1	8008	CPU Cards	L SERIES	Control Logic, Inc.	CLI
33	C8008	8008	CPU Chip	MCS8	Intel Corp.	ITL
34	C8008-1	8008	CPU Chip	MCS8	Intel Corp.	ITL
35	imm8-82	8008	CPU Card	MCS8	Intel Corp	ITL
36	AT441-5	8008	CPU Card	MIKE2	Martin Research	MAR
37	D8021	8021	Comp Chip	MCS48	Intel Corp	ITL
38#	8021I#1	8021	Comp Chip	MP8048	Mullard Ltd.	MULB
39	uPD8021C	8021	Comp Chip	uCOM-8	NEC Microcomputers, Inc.	NECM
40#	8021I	8021	Comp Chip	MP8048	N.V. Philips(Netherlands)	PHIN
41	8021I#2	8021	Comp Chip	MP8048	Signetics Corp.	SIC
42#	8021I#3	8021	Comp Chip	MP8048	Valvo GMBH(West Germany)	VALG
43	uPD8022C	8022	CPU Chip	uPD8022	NEC Microcomputers Inc.	NECM
44	D8035	8035	Comp Chip	MCS48	Intel Corp.	ITL
45	D8035-4	8035	Comp Chip	MCS48	Intel Corp	ITL
46	D8035-8	8035	Comp Chip	MCS48	Intel Corp.	ITL
47	P8035	8035	Comp Chip	MCS48	Intel Corp.	ITL
48	P8035-4	8035	Comp Chip	MCS48	Intel Corp	ITL
49	P8035-8	8035	Comp Chip	MCS48	Intel Corp.	ITL
50#	uPD8035LC	8035	Comp Chip	uCOM-8	NEC Microcomputers	NECJ
51	uPD8035C	8035	Comp Chip	uCOM-8	NEC Microcomputers Inc	NECM
52#	TMP8035P	8035	Comp Chip	TLCS-84	Toshiba Corporation (Japan)	TOSJ
53	uPD8039	8039	Comp Chip	uCOM-8	NEC Microcomputers, Inc.	NECM
54#	TMP8039P	8039	Comp Chip	TLCS-84	Toshiba Corporation (Japan)	TOSJ
55#	TMP8039P-6	8039	Comp Chip	TLCS-84	Toshiba Corporation (Japan)	TOSJ
56	B8741	8041	Comp Chip	UPI41	Intel Corp	ITL
57	B8741-4	8041	Comp Chip	UPI41	Intel Corp	ITL
58	B8741-8	8041	Comp Chip	UPI41	Intel Corp	ITL
59	D8041	8041	Comp Chip	UPI41	Intel Corp.	ITL
60	P8041	8041	Comp Chip	UPI41	Intel Corp	ITL
61	uPD8041	8041	Comp Chip	uCOM-8	NEC Microcomputers, Inc.	NECM
62	D8039-6	8048	Comp Chip	MCS48	Intel Corp	ITL
63	D8048	8048	Comp Chip	MCS48	Intel Corp.	ITL
64	P8021	8048	Comp Chip	MCS48	Intel Corp	ITL
65	P8022	8048	Comp Chip	MCS48	Intel Corp	ITL
66	P8039	8048	Comp Chip	MCS48	Intel Corp	ITL
67	P8039-6	8048	Comp Chip	MCS48	Intel Corp	ITL
68	P8048	8048	Comp Chip	MCS48	Intel Corp.	ITL
69	P8048-8	8048	Comp Chip	MCS48	Intel Corp.	ITL
70	P8049	8048	Comp Chip	MCS48	Intel Corp	ITL
71#	8048-8I#1	8048	Comp Chip	MP8048	Mullard Ltd.	MULB
72#	MP8035L-8I#1	8048	Comp Chip	8048	Mullard Ltd	MULB
73#	MP8035LI#1	8048	Comp Chip	8048	Mullard Ltd	MULB
74#	MP8048I#1	8048	Comp Chip	8048	Mullard Ltd	MULB
75#	uPD8048D	8048	Comp Chip	uCOM-8	NEC Microcomputers	NECJ
76	uPD8048C	8048	Comp Chip	uCOM-8	NEC Microcomputers	NECM
77	INS8035	8048	Comp Chip	48 Series	National Semiconductor Corp	NSC
78	INS8039	8048	Comp Chip	48 Series	National Semiconductor Corp	NSC
79	INS8048	8048	Comp Chip	48 Series	National Semiconductor Corp	NSC
80	INS8049	8048	Comp Chip	48 Series	National Semiconductor Corp	NSC
81	INS8050	8048	Comp Chip	48 Series	National Semiconductor Corp	NSC
82#	8048-8I	8048	Comp Chip	MP8048	N.V. Philips(Netherlands)	PHIN
83#	MP8035-8I	8048	CompChip	8048	N.V. Philips (Netherlands)	PHIN
84#	MP8035LI	8048	CompChip	8048	N.V. Philips (Netherlands)	PHIN
85	8048-8I#2	8048	Comp Chip	MP8048	Signetics Corp.	SIC
86	MP8035LI-8I#2	8048	Comp Chip	8048	Signetics Corp	SIC
87	MP8035LI#2	8048	Comp Chip	8048	Signetics Corp	SIC
88	MP8048I#2	8048	Comp Chip	8048	Signetics Corp SIC	SIC
89#	TMP8048P	8048	Comp Chip	TLCS-84	Toshiba Corporation (Japan)	TOSJ
90#	8048-8I#3	8048	Comp Chip	MP8048	Valvo GMBH(West Germany)	VALG
91#	MP8035L-8I#3	8048	Comp Chip	8048	Valvo GMBH (West Germany)	VALG
92#	MP8035LI#3	8048	Comp Chip	8048	Valvo GMBH (West Germany)	VALG
93#	MP8048I#3	8048	Comp Chip	8048	Valvo GMBH (West Germany)	VALG
94	D8049	8049	Comp Chip	MCS48	Intel Corporation	ITL
95	uPD8049	8049	Comp Chip	uCOM-8	NEC Microcomputers, Inc.	NECM
96	MP8039-6I	8049	Comp Chip	8048	Signetics Corp	SIC
97	MP8039I	8049	Comp Chip	8048	Signetics Corp	SIC
98	MP8049-6I	8049	Comp Chip	8048	Signetics Corp	SIC
99	MP8049I	8049	Comp Chip	8048	Signetics Corp	SIC
100#	TMP8049P	8049	Comp Chip	TLCS-84	Toshiba Corporation (Japan)	TOSJ
101#	TMP8049P-6	8049	Comp Chip	TLCS-84	Toshiba Corporation (Japan)	TOSJ
102	INS8070	8070	Comp Chip	70 Series	National Semiconductor Corp	NSC
103	INS8072	8070	Comp Chip	70 Series	National Semiconductor Corp	NSC
104	70-100	8080	Comp Card	70 SERIES	Applied Data Communications	APP
105	70-130-142	8080	Comp Unit	70 SERIES	Applied Data Communications	APP
106	70-130-161	8080	Comp Unit	70 SERIES	Applied Data Communications	APP
107	70-130-162	8080	Comp Unit	70 SERIES	Applied Data Communications	APP
108	70-131-142	8080	Comp Unit	70 SERIES	Applied Data Communications	APP
109	70-131-161	8080	Comp Unit	70 SERIES	Applied Data Communications	APP
110	EVENT2000	8080	Comp Unit	EVENTSERIES	Applied Data Communications	APP

Microcomputer / Microprocessor
GENERIC SYSTEM INDEX

The microcomputer/microprocessor GENERIC SYSTEM INDEX relates microprocessor and microcomputer hardware from individual manufacturers to familiar family "generic numbers". The GENERIC I.D. column links microcomputer CHIPS, CARDS and SYSTEMS from all sources with industry-recognized "generic numbers".

IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE & (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	3 INDIVIDUAL PROCESSOR TYPE No.	1 GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	2 CODE
1	ASC80#3	8080	CPU Card	ASC80	Applied Systems Corp.	APS
2	7555C	8080	CPU Chip	Series 7555	Beckman Instruments Inc.	BEC
3	7555M	8080	CPU Chip	Series 7555	Beckman Instruments Inc.	BEC
4	7556CB	8080	CPU Chip	Series 7556	Beckman Instruments Inc.	BEC
5	7556CU	8080	CPU Chip	Series 7556	Beckman Instruments Inc.	BEC
6	7556MB	8080	CPU Chip	Series 7556	Beckman Instruments Inc.	BEC
7	7556MU	8080	CPU Chip	Series 7556	Beckman Instruments Inc.	BEC
8	MCP893	8080	CPU Cards	M Series	Control Logic, Inc.	CLI
9	MM1-CPU	8080	CPU Card	MM1	Control Logic, Inc.	CLI
10	TDG8080	8080	CPU Card	TDG8080SYS	The Digital Group, Inc.	DIG
11	DL8A	8080	Comp Unit	DL SERIES	Data Numerics, Inc.	DNI
12	MICROMITE80	8080	Comp Card	DL SERIES	Data Numerics, Inc.	DNI
13	9000-0080	8080	CPU Card	SYSTEM8	Detection Sciences, Inc.	DSI
14	CONCEPT80	8080	Comp Unit	SYSTEM8	Detection Sciences, Inc	DSI
15	M8A	8080	CPU Card	SYSTEM8	Detection Sciences, Inc.	DSI
16	CPIC-80B	8080	CPU Card	MD-1	E and L Instruments, Inc.	E/L
17	MICROCONTROL/10MOD8080	8080	Comp Unit	MS8080	Futuredata Computer Corp.	FCC
18	MICROSYSTEM/10MOD8080	8080	Comp Unit	MS8080	Futuredata Computer Corp.	FCC
19	MICROSYSTEM/12MOD8080	8080	Comp Unit	MS8080	Futuredata Computer Corp.	FCC
20	MICROSYSTEM/15MOD8080	8080	Comp Unit	MS8080	Futuredata Computer Corp.	FCC
21	MICROSYSTEM/20MOD8080	8080	Comp Unit	MS8080	Futuredata Computer Corp.	FCC
22	MICROSYSTEM/30MOD8080	8080	Comp Unit	MS8080	Futuredata Computer Corp.	FCC
23	MICROSYSTEM/31MOD8080	8080	Comp Unit	MS8080	Futuredata Computer Corp.	FCC
24	MICROSYSTEM/32MOD8080	8080	Comp Unit	MS8080	Futuredata Computer Corp.	FCC
25	H8	8080	Comp Unit	H8	Heath Company	HEA
26	MLP8080	8080	Comp Card	MLP8080	Heurikon Corp.	HEU
27	MX800	8080	CPU Card	MX SERIES	Information Control Corp.	ICC
28	I-8080	8080	Comp Unit	I-8080	Imsai Manufacturing Corp.	IMS
29	MPU-A	8080	CPU Card	PCS-80	Imsai Manufacturing Corp.	IMS
30	PCS-80/10	8080	Comp Unit	PCS-80	Imsai Manufacturing Corp.	IMS
31	PCS-80/11	8080	Comp Unit	PCS-80	Imsai Manufacturing Corp.	IMS
32	UC2000	8080	Comp Unit	UC2000	Infinite, Inc.	INF
33	C8080A1	8080	CPU Chip	MCS80	Intel Corp.	ITL
34	C8080A2	8080	CPU Chip	MCS80	Intel Corp.	ITL
35	C8080A	8080	CPU Chip	MCS80	Intel Corp.	ITL
36	D8080A1	8080	CPU Chip	MCS80	Intel Corp	ITL
37	D8080A2	8080	CPU Chip	MCS80	Intel Corp	ITL
38	D8080A	8080	CPU Chip	MCS80	Intel Corp	ITL
39	imm8-83	8080	CPU Card	MCS80	Intel Corp.	ITL
40	JANM38510/42001BQB	8080	CPU Chip	MCS80	Intel Corp.	ITL
41	JANM38510/42001CQB	8080	CPU Chip	MCS80	Intel Corp.	ITL
42	MC8080A	8080	CPU Chip	MCS80	Intel Corp.	ITL
43	MD8080A	8080	CPU Chip	MCS80	Intel Corp	ITL
44	P8080A1	8080	CPU Chip	MCS80	Intel Corp	ITL
45	P8080A2	8080	CPU Chip	MCS80	Intel Corp	ITL
46	P8080A	8080	CPU Chip	MCS80	Intel Corp	ITL
47	SBC80/10A	8080	Comp Card	MCS80	Intel Corp	ITL
48	SBC80/30	8080	Comp Card	MCS80	Intel Corp.	ITL
49	AT471-3	8080	CPU Card	MIKE3	Martin Research	MAR
50	AT476	8080	CPU Card	MIKE3	Martin Research	MAR
51	MIKE3	8080	Comp Cards	MIKE3	Martin Research	MAR
52#	M5L8080AP	8080	CPU Chip	M5L8080A	Mitsubishi Elect. Corp.	MITJ
53#	M5L8080AS	8080	CPU Chip	M5L8080A	Mitsubishi Elect. Corp.	MITJ
54#	M58710S	8080	CPU Chip	MELPS8	Mitsubishi Electric Corp	MITJ
55#	MELCS8/2	8080	Comp Cards	MELCS8/2	Mitsubishi Electric Corp	MITJ
56#	MELPS8	8080	Comp Unit	MELPS8	Mitsubishi Electric Corp	MITJ
57#	PCA0801	8080	Comp Card	MELCS8/2	Mitsubishi Electric Corp	MITJ
58	CPU808A	8080	CPU Card	800 SERIES	Multisonics	MUL
59	muPRO80	8080	Comp Unit	muPRO80	MuPRO Inc	MUP
60	muPRO80-010	8080	CPU Card	muPRO80	MuPRO Inc.	MUP
61	uPD8080AD2	8080	CPU Chip	uCOM-8	NEC Electronics(West Germany)	NECD
62	uPD8080AD#1	8080	CPU Chip	uCOM-8	NEC Electronics(West Germany)	NECD
63	uPD8080AD2#1	8080	CPU Chip	uCOM-8	Nippon Electric Co., Ltd.(Japan)	NECJ
64	uPD8080AD#2	8080	CPU Chip	uCOM-8	Nippon Electric Co., Ltd.(Japan)	NECJ
65#	uPD8080AFC	8080	CPU Chip	uCOM-80F	Nippon Electric Co., Ltd.(Japan)	NECJ
66#	uPD8080AFC-1	8080	CPU Chip	uCOM-80F	Nippon Electric Co., Ltd.(Japan)	NECJ
67#	uPD8080AFC-2	8080	CPU Chip	uCOM-80F	Nippon Electric Co., Ltd.(Japan)	NECJ
68#	uPD8080AFD	8080	CPU Chip	uCOM-80F	Nippon Electric Co., Ltd.(Japan)	NECJ
69#	uPD8080AFD-1	8080	CPU Chip	uCOM-80F	Nippon Electric Co., Ltd.(Japan)	NECJ
70#	uPD8080AFD-2	8080	CPU Chip	uCOM-80F	Nippon Electric Co., Ltd.(Japan)	NECJ
71	uPD8080AD	8080	CPU Chip	uCOM-8	NEC Microcomputers, Inc	NECM
72	uPD8080AFC-1#1	8080	CPU Chip	uCOM-80F	NEC Microcomputers, Inc.	NECM
73	uPD8080AFC-2#1	8080	CPU Chip	uCOM-80F	NEC Microcomputers, Inc.	NECM
74	uPD8080AFC#1	8080	CPU Chip	uCOM-80F	NEC Microcomputers, Inc.	NECM
75	uPD8080AFD-1#1	8080	CPU Chip	uCOM-80F	NEC Microcomputers, Inc.	NECM
76	uPD8080AFD-2#1	8080	CPU Chip	uCOM-80F	NEC Microcomputers, Inc.	NECM
77	uPD8080AFD#1	8080	CPU Chip	uCOM-80F	NEC Microcomputers, Inc.	NECM
78	BLC80/10	8080	CPU Card	Series 80	National Semiconductor Corp	NSC
79	BLC80/11	8080	CPU Card	Series 80	National Semiconductor Corp	NSC
80	BLC80/12	8080	CPU Card	Series 80	National Semiconductor Corp	NSC
81	BLC80/14	8080	CPU Card	Series 80	National Semiconductor Corp	NSC
82	BLC80/204	8080	CPU Card	Series 80	National Semiconductor Corp	NSC
83	INS8080AD	8080	CPU Chip	N8080A	National Semiconductor Corp.	NSC
84	INS8080AD-1	8080	CPU Chip	N8080A	National Semiconductor Corp.	NSC
85	INS8080AD-2	8080	CPU Chip	N8080A	National Semiconductor Corp.	NSC
86	RMC80/10	8080	Comp Cards	Series 80	National Semiconductor Corp	NSC
87	RMC80/14	8080	Comp Cards	Series 80	National Semiconductor Corp	NSC
88	RMC80/204	8080	Comp Unit	Series 80	National Semiconductor Corp.	NSC
89	EQUINOX-100	8080	Comp Unit	EQUINOX-100	Parasitic Engineering Inc.	PAR
90	ALTAIR8800B	8080	Comp Unit	ALTAIR8800	PCC Microsystems	PCC
91	ALTAIR8800B-T	8080	Comp Unit	ALTAIR8800	PCC Microsystems	PCC
92	CM4400	8080	CPU Card	MICROPAC80A	Process Computer Systems, Inc.	PCS
93	SPDS	8080	Comp Unit	SUPERPAC180	Process Computer Systems, Inc	PCS
94#	MP8080AI#1	8080	CPU Chip	MP8080A	N. V. Philips(Netherlands)	PHIN
95	8821	8080	CPU Card	MPS-800	Pro-Log Corp.	PRO
96	SOL20/16	8080	Comp Unit	SOL20	Processor Technology Corp	PTC
97	SOL20/32	8080	Comp Unit	SOL20	Processor Technology Corp	PTC
98	SOLPC	8080	Comp Card	SOL20	Processor Technology Corp	PTC
99	SOLSIA	8080	Comp Unit	SOL20	Processor Technology Corp	PTC
100	SOLSIIA	8080	Comp Unit	SOL20	Processor Technology Corp	PTC
101	SOLSIII	8080	Comp Unit	SOL20	Processor Technology Corp	PTC
102	SOLSIV	8080	Comp Unit	SOL20	Processor Technology Corp	PTC

Microcomputer / Microprocessor
GENERIC SYSTEM INDEX

The microcomputer/microprocessor GENERIC SYSTEM INDEX relates microprocessor and microcomputer hardware from individual manufacturers to familiar family "generic numbers". The GENERIC I.D. column links microcomputer CHIPS, CARDS and SYSTEMS from all sources with industry-recognized "generic numbers".

IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE & (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	3 INDIVIDUAL PROCESSOR TYPE No.	1 GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	2 CODE
1	RCCZ-110-1	8080	Comp Unit	RCCZ-110	Realistic Controls Corp.	RLC
2	RCCZ-110-2	8080	Comp Unit	RCCZ-110	Realistic Controls Corp.	RLC
3	RCCZ-110-3	8080	Comp Unit	RCCZ-110	Realistic Controls Corp.	RLC
4#	MICRAL-C	8080	Comp Unit	MICRAL	R2E-Realisations etudes Electron(France)	R2E
5	SIA3000	8080	Comp Unit	SIA3000	System Integration Associates	SIA
6	MP8080AI	8080	CPU Chip	MP8080A	Signetics Corp.	SIC
7	SMP80	8080	Comp Cards	SMP80	Siemens Aktiengesellschaft,W. Germany	SIEG
8	CB1	8080	CPU Card	SSM-S100	SSM	SSM
9	CPU-TAI	8080	CPU Card	TOKOM80	Toko America, Inc	TAI
10	TMS8080	8080	CPU Chip	TMS8080	Texas Instruments, Inc	TII
11	TMS8080AJL	8080	CPU Chip	TMS8080A	Texas Instruments, Inc	TII
12	TMS8080ANL	8080	CPU Chip	TMS8080A	Texas Instruments, Inc	TII
13	VECTOR1	8080	Comp Unit	VECTOR1	Vector Graphic, Inc.	VGI
14	VECTOR1CPU	8080	CPU Card	VECTOR1	Vector Graphic, Inc.	VGI
15	VECTOR1PLUS	8080	Comp Unit	VECTOR1PLUS	Vector Graphic, Inc.	VGI
16	VGM	8080	Comp Unit	VGM	Vector Graphic, Inc.	VGI
17	CPU1	8080	CPU Card	uP Series	Wyle Computer Products	WLD
18	uPCPU1	8080	CPU Card	uP Series	Wyle Computer Products	WLD
19	Am8085ACC	8085	CPU Chip	Am8085A	Advanced Micro Devices Inc.	AMV
20	Am8085ADC	8085	CPU Chip	Am8085A	Advanced Micro Devices Inc.	AMV
21	Am8085APC	8085	CPU Chip	Am8085A	Advanced Micro Devices Inc.	AMV
22	MICROCONTROL/10MOD8085	8085	Comp Unit	MICROSYSTEM	Futuredata Computer Corp.	FCC
23	MICROSYSTEM/10MOD8085	8085	Comp Unit	MS8085	Futuredata Computer Corp.	FCC
24	MICROSYSTEM/12MOD8085	8085	Comp Unit	MS8085	Futuredata Computer Corp.	FCC
25	MICROSYSTEM/15MOD8085	8085	Comp Unit	MS8085	Futuredata Computer Corp.	FCC
26	MICROSYSTEM/31MOD8085	8085	Comp Unit	MS8085	Futuredata Computer Corp.	FCC
27	MICROSYSTEM/32MOD8085	8085	Comp Unit	MS8085	Futuredata Computer Corp.	FCC
28	MPU-B	8085	CPU Card	PCS-80	Imsai Manufacturing Corp.	IMS
29	PCS-40	8085	Comp Cards	PCS-40	Imsai Manufacturing Corp.	IMS
30	PCS-42	8085	Comp Cards	PCS-40	Imsai Manufacturing Corp.	IMS
31	PCS-44	8085	Comp Cards	PCS-40	Imsai Manufacturing Corp.	IMS
32	PCS-80/15	8085	Comp Unit	PCS-80	Imsai Manufacturing Corp.	IMS
33	PCS-80/30	8085	Comp Unit	PCS-80	Imsai Manufacturing Corp.	IMS
34	PCS-80/34	8085	Comp Unit	PCS-80	Imsai Manufacturing Corp.	IMS
35	PCS-80/35	8085	Comp Unit	PCS-80	Imsai Manufacturing Corp.	IMS
36	PCS-80/100	8085	Comp Unit	PCS-80	Imsai Manufacturing Corp.	IMS
37	PCS-80/200	8085	Comp Unit	PCS-80	Imsai Manufacturing Corp.	IMS
38	VDP-40	8085	Comp Unit	VDP-40	Imsai Manufacturing Corp.	IMS
39	VDP-42	8085	Comp Unit	VDP-40	Imsai Manufacturing Corp.	IMS
40	VDP-44	8085	Comp Unit	VDP-40	Imsai Manufacturing Corp.	IMS
41	VDP-80	8085	Comp Unit	VDP-80	Imsai Manufacturing Corp.	IMS
42	C8085A2	8085	CPU Chip	MCS85	Intel Corp	ITL
43	C8085A	8085	CPU Chip	MCS85	Intel Corp	ITL
44	P8085A2	8085	CPU Chip	MCS85	Intel Corp	ITL
45	P8085A	8085	CPU Chip	MCS85	Intel Corp	ITL
46#	M5L8085AP-20	8085	CPU Chip	M5L8085A	Mitsubishi Elect. Corp.	MITJ
47#	M5L8085AS-20	8085	CPU Chip	M5L8085A	Mitsubishi Elect. Corp.	MITJ
48#	uPD8085AD	8085	CPU Chip	uCOM-8	Nippon Electric Co., Ltd.(Japan)	NECJ
49	uPD8085A-2	8085	CPU Chip	uCOM-8	NEC Microcomputers, Inc.	NECM
50	uPD8085C	8085	CPU Chip	uCOM-8	NEC Microcomputers Inc.	NECM
51	NMS85/AR	8085	Comp Unit	NMS85/P	Northwest Microcomputer Systems	NMS
52	NMS85/GL	8085	Comp Unit	NMS85/P	Northwest Microcomputer Systems	NMS
53	NMS85/P	8085	Comp Unit	NMS85/P	Northwest Microcomputer Systems	NMS
54	NMS85/WP	8085	Comp Unit	NMS85/P	Northwest Microcomputer Systems	NMS
55	7801	8085	CPU Card	7000	Pro-Log Corp.	PRO
56	SKC85	8085	Comp Card	SKC85	Siemens Aktiengesellschaft,W. Germany	SIEG
57	SSM-85/1	8085	Comp Card	SSM-85	System Service Co.	SSC
58	SSM-85/2	8085	Comp Card	SSM-85	System Service Co.	SSC
59#	TMP8085A	8085	CPU Chip	TLCS85AA	Toshiba Corp. (Japan)	TOSJ
60#	TMP8085AP	8085	CPU Chip	TLCS-85A	Toshiba Corporation (Japan)	TOSJ
61	D8086	8086	CPU Chip	MCS86	Intel Corp	ITL
62	D8086-4	8086	CPU Chip	MCS86	Intel Corp.	ITL
63	SDK86	8086	Comp Card	MCS86	Intel Corp	ITL
64	D8088	8088	CPU Chip	MCS88	Intel Corp.	ITL
65	D8741	8741	Comp Chip	UPI41	Intel Corp.	ITL
66	uPD8741	8741	Comp Chip	uCOM-8	NEC Microcomputers, Inc.	NECM
67	B8748	8748	Comp Chip	MCS48	Intel Corp.	ITL
68	B8748-8	8748	Comp Chip	MCS48	Intel Corp.	ITL
69	C8748-4	8748	Comp Chip	MCS48	Intel Corp	ITL
70#	8748-8I#1	8748	Comp Chip	MP8048	Mullard Ltd.	MULB
71#	8748I#1	8748	Comp Chip	MP8048	Mullard Ltd.	MULB
72	uPD8748D	8748	Comp Chip	uCOM-8	NEC Microcomputers, Inc	NECM
73#	8748-8I	8748	Comp Chip	MP8048	N.V. Philips(Netherlands)	PHIN
74#	8748I	8748	Comp Chip	MP8048	N.V. Philips(Netherlands)	PHIN
75	8748-8I#2	8748	Comp Chip	MP8048	Signetics Corp.	SIC
76	8748I#2	8748	Comp Chip	MP8048	Signetics Corp.	SIC
77#	8748-8I#3	8748	Comp Chip	MP8048	Valvo GMBH(West Germany)	VALG
78#	8748I#3	8748	Comp Chip	MP8048	Valvo GMBH(West Germany)	VALG
79	WD9000	9000	CPU Chips	WD9000	Western Digital Corporation	WDC
80	AMC95/4000	9080A	Comp Card	AMC95/4000	Advanced Micro Computers	AuC
81	Am9080A1DC	9080A	CPU Chip	Am9080A	Advanced Micro Devices Inc.	AMV
82	Am9080A1PC	9080A	CPU Chip	Am9080A	Advanced Micro Devices Inc.	AMV
83	Am9080A2DC	9080A	CPU Chip	Am9080A	Advanced Micro Devices Inc.	AMV
84	Am9080A2DM	9080A	CPU Chip	Am9080A	Advanced Micro Devices Inc.	AMV
85	Am9080A2PC	9080A	CPU Chip	Am9080A	Advanced Micro Devices Inc.	AMV
86	Am9080A4DC	9080A	CPU Chip	Am9080A	Advanced Micro Devices Inc.	AMV
87	Am9080ADC	9080A	CPU Chip	Am9080A	Advanced Micro Devices Inc.	AMV
88	Am9080ADM	9080A	CPU Chip	Am9080A	Advanced Micro Devices Inc.	AMV
89	Am9080APC	9080A	CPU Chip	Am9080A	Advanced Micro Devices Inc.	AMV
90	AMC95/1016	9080A	Comp Card	AMC95/1000	Advanced Microcomputers	AUC
91	AMC95/1032	9080A	Comp Card	AMC95/1000	Advanced Microcomputers	AUC
92	AMC95/4005/2	9080A	Comp Card	AMC95/4005	Advanced Microcomputers	AUC
93	AMC95/4005/3	9080A	Comp Card	AMC95/4005	Advanced Microcomputers	AUC
94	AMC95/5032	9080A	Comp Card	AMC95/1000	Advanced Microcomputers	AUC
95#	TMP9080A	9080A	CPU Chip	TLCS80A	Toshiba Corp. (Japan)	TOSJ
96	9405ADC	9400	CPU Chip	9400	Fairchild Camera and Instrument Corp.	FSC
97	9405ADM	9400	CPU Chip	9400	Fairchild Camera and Instrument Corp.	FSC
98	9405APC	9400	CPU Chip	9400	Fairchild Camera and Instrument Corp.	FSC
99	9405FC	9400	CPU Chip	9400	Fairchild Camera and Instrument Corp.	FSC
100	9405FM	9400	CPU Chip	9400	Fairchild Camera and Instrument Corp.	FSC
101	9440DC	9400	CPU Chip	9440	Fairchild Camera and Instrument Corp.	FSC
102	9440DM	9400	CPU Chip	9440	Fairchild Camera and Instrument Corp.	FSC
103	9440PC	9440	CPU Chip	9440	Fairchild Camera and Instrument Corp	FSC
104	SPARK-16	9440	Comp Card	SPARK-16	Fairchild Camera and Instrument Corp	FSC

Microcomputer / Microprocessor
GENERIC SYSTEM INDEX

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IN ORDER OF:(1)GENERIC I.D. (2)MANUFACT CODE & (3)INDIVIDUAL PROCESSOR TYPE No.

LINE No.	[3] INDIVIDUAL PROCESSOR TYPE No.	[1] GENERIC I.D.	PROCESSOR ARCHITECTURE	SYSTEM No.	MANUFACTURER NAME	[2] CODE
1	S9900	9900	CPU Chip	S9900	American Microsystems Inc.	AMI
2	SBP9900	9900	CPU Chip	990	Texas Instruments, Inc	TII
3	SBP9900ACJ	9900	CPU Chip	990	Texas Instruments, Inc	TII
4	SBP9900AEJ	9900	CPU Chip	990	Texas Instruments, Inc	TII
5	SBP9900AMJ	9900	CPU Chip	990	Texas Instruments, Inc	TII
6	SBP9900ANJ	9900	CPU Chip	990	Texas Instruments, Inc	TII
7	TM990/100M-1	9900	Comp Card	990	Texas Instruments, Inc	TII
8	TM990/100M-2	9900	Comp Card	990	Texas Instruments, Inc	TII
9	TM990/100M-3	9900	Comp Card	990	Texas Instruments, Inc	TII
10	TM990/101M-1	9900	Comp Card	9900	Texas Instruments, Inc.	TII
11	TM990/101M-2	9900	Comp Card	9900	Texas Instruments, Inc.	TII
12	TM990/101M-3	9900	Comp Card	9900	Texas Instruments, Inc.	TII
13	TMS9900	9900	CPU Chip	990	Texas Instruments, Inc.	TII
14	TMS9940	9940	Comp Chip	TMS9940	Texas Instruments, Inc.	TII
15	S9980	9980	CPU Chip	S9900	American Microsystems Inc.	AMI
16	TM990/180M-1	9980	Comp Card	990	Texas Instruments, Inc	TII
17	TM990/180M-3	9980	Comp Card	990	Texas Instruments, Inc	TII
18	TMS9980JL	9980	CPU Chip	TMS9980	Texas Instruments, Inc	TII
19	TMS9980NL	9980	CPU Chip	TMS9980	Texas Instruments, Inc	TII
20	TMS9980A	9980A	CPU Chip	9900	Texas Instruments, Inc.	TII
21	TMS9981	9981	CPU Chip	9900	Texas Instruments, Inc.	TII
22	TMS9985	9985	CPU Chip	9900	Texas Instruments, Inc.	TII

USE OF POWERS-OF-TEN MULTIPLIERS

To present a maximum amount of information in a minimum amount of space, use is made in this book of the following data modifiers:

POWERS-OF-TEN MULTIPLERS

The powers-of-ten multipliers shown below are used in numeric columns when the value being entered is many times greater or smaller than the units of measure indicated in the column heading. Usually, the latter are the so-called 'basic' units; such as V (volts), A (amperes) and s (seconds). The multipliers and an explanation of their use are given below:

MULTIPLIERS								
PREFIXES & SYMBOLS Indicating Powers-of-Ten — Recommended by International Committee on Weights and Measures Adopted by National Bureau of Standards								
Power	**Prefix**	**Symbol**	**Power**	**Prefix**	**Symbol**	**Power**	**Prefix**	**Symbol**
10^{12}	tera	T	10	deka	da	10^{-9}	nano	n
10^{9}	giga	G	10^{-1}	deci	d	10^{-12}	pico	p
10^{6}	mega	M	10^{-2}	centi	c	10^{-15}	femto	f
10^{3}	kilo	k	10^{-3}	milli	m	10^{-18}	atto	a
10^{2}	hecto	h	10^{-6}	micro	μ			

EXPLANATION		
Value of Data To Be Entered	Basic Unit In Column Heading	Actual Entry
3 miliamperes	A (amperes)	3.0m
9 megaohms	Ω (ohms)	9.0M
0.5 volt	V (volts)	500m*
10 amperes	A (amperes)	10

* May also be written as 0.5, with no multiplier.

USE OF SYMBOLS, CODES AND ABBREVIATIONS

Symbols: Symbols such as △, *, ϕ, etc. are used in most columns, numeric or otherwise, whenever the data entries differ in some way from the entity described in the column heading. For instance, if a given heading specifies Max. Power (in Watts) and the numeric value being entered for a given type represents the minimum power instead, the variance is denoted by the appearance of a special symbol alongside the numeric entry.

Codes and Abbreviations: Codes and abbreviations are used in some columns as a means to abbreviate the data being entered. The codes or abbreviations may be alphabetic (MOTA - Motorola; V - vectored; ChF - chip family), numeric (1,2,3,etc.), or some combination of both (8VP - 8, vectored, priority.)

Note: Symbols, Codes, Abbreviations used herein are explained on the cards in the back of the book.

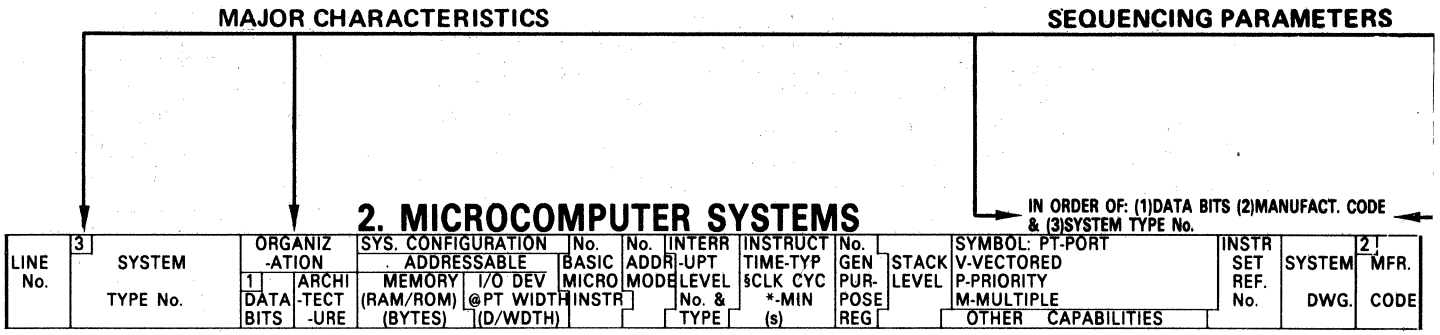
HOW TYPE NUMBERS ARE SEQUENCED IN THE TYPE NUMBER CROSS INDEX

Sequencing of Type Numbers in the Type Number Cross-Index (Section 1) is governed by the following rules:

	EXAMPLES
Rules: 1) Type numbers are listed in numeric-alphabetic sequence; i.e., type numbers beginning with a number (decimal, fraction, or whole) precede type numbers beginning with a letter.	**8M0DB** **70-180VTI** **A05** **DRV22** **imm6-26** **IMP 16C**
2) Zeros are ignored in sequencing except when the zero is the only basis for distinguishing one type number from another. In this case the type number containing the zero is listed first.	**306** **0364** **588** **733** **733ASR**
3) Number and/or letter groupings preceding hyphens or slashes are the controlling factors in sequencing. The hyphens and slashes themselves precede any identically positioned letters also having the same beginning number/letter groupings.	**70-120** **70ASB** **913AVDT** **990/4** **990B3**

HOW TYPE NOS. ARE ARRANGED IN THE TECHNICAL SECTION – SEQUENCING PARAMETERS

The arrangement of types in the technical sections is keyed to a set of special characteristics selected for their importance from among the general group of characteristics tabulated in each section. These selected characteristics, or sequencing parameters, differ from one section to another, and are identified at the top corner of each page, as shown in the sample below.



The different types within a section are first arranged in ascending numeric (or alphabetic) order of the first such parameter. Groups of types having a common value for the first parameter are then arranged in ascending order of the second parameter. This process continues for each parameter in turn, up to and including the last parameter which, in every instance, is the type number itself. The final arrangement, by type number, is done in accordance with the sequencing of type numbers in the cross-index, as explained on the preceding page.

A simplified model of the arrangement as described is shown below.

4 Type Number	Characteristics 1 A	2 B	C	3 D
A13	100		325	
A4	100		1000	20
A9	100	A	20	25
A10	100	A	200	25
A3	100	B	40	15
A1	100	C	80	10
A8	100	C	900	15
A7	100	D	35	30
A11	110	A	60	25
A2	120	A	300	15
A5	120	B	150	20
A6	120	B	200	20
A12	120	B	475	25
	Last Seq. Par.	1st Seq. Par.	2nd Seq. Par.	(Not Seq.)	3rd Seq. Par.

Note that the absence of an entry for any sequencing parameter is regarded as a zero, and precedes any actual entries in the sequencing.

GENERAL TERMS AND DEFINITIONS

MICROCOMPUTER

Abbreviated Addressing
A direct-addressing mode that can access only part of the full memory, but can provide a faster means of processing data because of the shortened code. (See extended addressing.)

Accumulator
(ISO) A register in which the result of an operation is formed. (ANDIP)

Address
(ISO) A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (ANDIP)

Addressing Modes
The methods of specifying the location(s) of data or program segments in memory or other locations.

Architecture
(1) The organizational structure of a computing system, mainly referring to the CPU or microprocessor, but also including other hardware and software.
(2) The specification of the relationships between the parts of a computer system. (ANDIP).

Arithmetic and Logic Unit (ALU)
(ISO) A part of a computer that performs arithmetic operations, logic operations, and related operations. (ANDIP)
NOTE: Along with memory and control, this is an essential microprocessor element.

Assembler
A computer program used to translate symbolic-language statements to machine-language statements. (Abbreviated from ANDIP)

Assembly Language
A computer-oriented language whose instructions are usually in one-to-one correspondence with computer instructions and that may provide facilities such as the use of macroinstructions. (ANDIP)

Baud
A unit of signalling speed equal to the number of discrete conditions or signal events per second. (ANDIP)
NOTE: For example, one baud equals one bit per second in a train of binary signals or one 3-bit value per second in a train of signals each of which can assume one of eight (2^3) different states.

Benchmark Problem
(1) A problem used to evaluate the performance of hardware or software or both. (ANDIP)
(2) A problem used to evaluate the performance of several computers relative to each other, or a single computer relative to system specifications. (ANDIP)

Binary-Coded Decimal (BCD)
A number coding system in which each decimal digit is represented by a binary numeral (usually 4 bits). EXAMPLE: The decimal number 23 becomes the coded number 0010 0011 in BCD using the 8-4-2-1 binary code. (Abbreviated from ANDIP)

Bit
In the pure binary numberation system, either of the digits 0 or 1. (ANDIP)
NOTE: Synonymous with binary digit. (ANDIP)

Bit Slice
A partition of a microprocessor that enables several identical units to be paralled or cascaded and augmented by control logic to realize the CPU.

Bootstrap Program; Bootstrap Loader
An input routine in which simple preset computer operations are used to load instructions that in turn cause further instructions to be loaded until the complete computer program is in storage. (ANDIP)

Branch
(1) A set of instructions that are executed between two successive branch instructions. (ANDIP)
(2) A direct path joining two nodes of a network or graph. (ANDIP)
(3) Loosely, a conditional jump. (ANDIP)
(4) (ISO) In the execution of a computer program, to select one from a number of alternative sets of instructions. (ANDIP)
(5) To select a branch as in (1). (ANDIP)
(6) (ISO) Deprecated term for jump. (ANDIP)

Branch Instruction
(1) (ISO) An instruction that controls branching. Synonymous with decision instruction. (ANDIP)
(2) (ISO) Deprecated term for jump instruction. (ANDIP)

Buffer
(1) A routine or storage used to compensate for a difference in rate of flow of data, or time of occurrence of events, when transferring data from one device to another. (ANDIP)
(2) An isolating circuit used to prevent a driven circuit from influencing the driving circuit. (ANDIP)

Buffer Storage
A storage device used to compensate for a difference in rate of flow of data between components of an automatic data processing or communications system, or time of occurrence of events in the components. (Adapted from ANDIP)

Bus
One or more conductors used for transmitting signals or power from one or more sources to one or more destinations. (Adapted from ANDIP)

Byte
A binary character string operated upon as a unit and usually shorter than a computer word. (ANDIP)
NOTE: A byte is usually 8 bits.

Central Processing Unit (CPU)
A unit of a computer that includes circuits controlling the interpretation and execution of instructions. Synonymous with central processor, main frame. (ANDIP)

MICROCOMPUTER

Chip-Enable Input A control input to an integrated circuit that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced-power standby mode.

NOTE: A chip-enable input is a clock or strobe input that significantly affects the power dissipation of the integrated circuit. For example, it may be the cycle control input of a dynamic memory or a power-reduction input of a static memory.

Chip-Select Input A gating input that when inactive prevents input or output of data to or from the integrated circuit.

Clock (ISO) A device that generates periodic signals from which synchronism may be maintained. (ANDIP)

Closed Subroutine (ISO) A subroutine of which one replica suffices for the subroutine to be linked by calling sequences for use at more than one place in a computer program. (ANDIP)

Compiler A computer program used to translate a computer program expressed in a problem-oriented language (e.g. FORTRAN) into a computer-oriented (machine-oriented) language program. (Abbreviated from ANDIP)

Condition Code A group of flag bits representing the status of program conditions such as carry, borrow, overflow, etc. that are particularly relevant to instruction execution.

Conditional Branch Deprecated term of conditional jump.

Conditional Jump (ISO) A jump that takes place only when the instruction that specifies it is executed and specified conditions are satisfied. (ANDIP)

Conditional Jump Instruction (ISO) An instruction that specifies a conditional jump and the conditions that have to be satisfied for the conditional jump to occur. (ANDIP)

Control Block The circuitry that performs the control functions of the CPU; i.e., decoding microprogrammed instructions and generating the internal control signals that perform the operations requested.

Control Bus A bus carrying the signals that regulate system operations within and without the computer.

Control Program A computer program designed to schedule and supervise the execution of all the programs, routines, and subroutines of a computing system. (ANDIP)

Control Read-Only Memory (CROM) A ROM in the control block of some microprocessors that has been microprogrammed to decode the control logic.

Cross-Assembler A program that translates the symbolic-language statements of one computer into the machine-language statements of another computer.

Cycle (of a Memory) A sequence of operations necessary to perform one or more of the functions of the memory.

NOTE: The end of a cycle is to be understood as the earliest instant at which a subsequent cycle can start with correct functioning of the memory.

Daisy Chain A method of device interconnection for determining interrupt priority by connecting the interrupt sources serially.

Data Bus A bus used to communicate data internally and externally to and from CPU, memory, and peripheral devices.

Data Pointer A register holding the memory address of the operand used by an instruction; i.e., the data pointer "points" to the memory location of the (data) operand.

Data Register Any register that holds data.

Debug Program A computer program designed to aid in detecting, tracing, and eliminating mistakes in microcomputer (or other computer) programs or in other software. (Adapted from ANDIP)

Decrement A program instruction that decreases the contents of a storage location by a single count.

Dedicated Microcomputer A microcomputer that is intended for a specific application.

Diagnostic Program (ISO) A computer program that recognizes, locates, and explains either a fault in equipment or a mistake in a computer program. (ANDIP)

NOTE: Diagnostic programs are typically written for each functional area; e.g., CPU diagnostic for CPU checks, memory diagnostics for memory checks, etc.

Direct Address (ISO) An address that designates the storage location of an item of data to be treated as an operand. Synonymous with one-level address. (ANDIP)

Direct Addressing (ISO) A method of addressing in which the address part of an instruction contains a direct address. (ANDIP)

Direct Memory Access (DMA) A method of inserting input/output data into storage or obtaining input/output data from storage directly, without involving the usual flow of data through the processor.

MICROCOMPUTER

Duplex Transmission Simultaneous independent transmission in both directions on a transmission line. (Adapted from ANDIP)

Dynamic (Read/Write) Memory A read/write memory in which the cells require the repetitive application of control signals generated inside or outside the integrated circuit in order to retain stored data.

NOTE 1: The words "read/write" may be ommitted from the term when no misunderstanding will result.

NOTE 2: Such repetitive application of the control signals is normally called a refresh operation.

NOTE 3: A dynamic memory may use static addressing or sensing circuits.

NOTE 4: Contrast with static (read/write) memory.

Editor Program A computer program designed to perform such functions as the rearrangement, modification, addition, and deletion of data in accordance with prescribed rules. (ANDIP)

Electrically Alterable Read-Only Memory (EAROM) A synonym for an electrically erasable programmable read-only memory.

Electrically Erasable Programmable Read-Only Memory (EEPROM) A reprogrammable read-only memory in which cells may be erased electrically and in which each cell may be reprogrammed electrically.

Emulate To imitate one system with another, primarily by hardware, so that the imitating system accepts the same data, executes the same computer programs, and achieves the same results as the imitated system. (ANDIP)

NOTE: Contrast with simulate. (ANDIP)

Erasable Programmable Read-Only Memory (EPROM) A reprogrammable read-only memory in which all cells may be simultaneously erased using ultraviolet light and in which each cell may be reprogrammed electrically.

Execution Time The time, normally expressed in clock cycles, required to carry out an instruction.

Extended Addressing A direct-addressing mode that can access any storage location in the memory. (See abbreviated addressing)

Fetch To locate and load a quantity of data from storage. (ANDIP)

Field-Programmable Read-Only Memory A read-only memory that, after being manufactured, can have the data content of each memory cell altered.

Firmware The program instructions stored in a read-only memory.

First-In, First-Out (FIFO) Memory A memory from which data bytes or words can be read in the same order, but not necessarily at the same rate, as that of the data entry.

Fixed-Program Read-Only Memory A read-only memory in which the data content of each cell is determined during manufacture and is thereafter unalterable.

Flag Bit An information bit that indicates the occurrence of special conditions such as overflow, carry, and interrupt.

Flowchart (ISO) A graphical representation of the definition, analysis, or method of solution of a problem, in which symbols are used to represent operations, data, flow, equipment, etc. (ANDIP)

Full-Duplex Transmission See duplex transmission.

Half-Duplex Transmission Alternating, one-way-at-a-time, independent transmission on a transmission line. (Adapted from ANDIP)

Handshaking A colloquial term that describes the method used by a modem (or other input-output device) to establish a communication link for eventual data transmission by means of a sequential acknowledgement of offer and acceptance.

Hardware (ISO) Physical equipment used in data processing, as opposed to computer programs, procedures, rules, and associated documentation. (ANDIP)

NOTE: Contrast with software. (ANDIP)

High-Level Language A problem-oriented programming language (e.g., FORTRAN) that does not reflect the structure of any one given computer or that of any given class of computers and in which a single functional statement may translate into a series of instructions in machine language (a low-level language). (Adapted from ANDIP)

Immediate Address (ISO) The contents of an address part that contains the value of an operand rather than an address. Synonymous with zero-level address. (ANDIP)

Immediate Addressing (ISO) A method of addressing in which the address part of an instruction contains an immediate address. (ANDIP)

Immediate Data Data stored in the instruction itself.

Increment A program instruction that increases the contents of a storage location by a single count.

Index Register (ISO) A register whose contents may be used to modify an operand address during the execution of computer instructions, so as to operate as a clock or counter. (ANDIP)

NOTE: An index register may be used to control the execution of a loop, to control the use of an array, as a switch, for the table lookup, as a pointer, etc. (ANDIP)

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Indexed Address An address that is modified by the content of an index register prior to or during the execution of a computer instruction. (ANDIP)

Indexed Addressing A method of addressing in which the address part of the instruction contains an indexed address. (Adapted from ANDIP)

Indirect Address (ISO) An address that designates the storage location of an item of data to be treated as the address of an operand, but not necessarily as its direct address. Synonymous with multilevel address. (ANDIP)
NOTE: Contrast with direct address. (ANDIP)

Indirect Addressing A method of addressing in which the address part of an instruction contains an indirect address. (ANDIP)
NOTE: Contrast with direct addressing. (ANDIP)

Instruction (ISO) In a programming language, a meaningful expression that specifies one operation and identifies its operands, if any. (ANDIP)

Instruction Cycle The process of fetching an instruction from memory and executing it.

Instruction Length The measure of the memory space required to store an instruction.

Instruction Set (of a Microprocessor) All the instructions that can be executed by a given microprocessor.

Interpreter Program A computer program used to translate and to execute each source language statement of a computer program before translating and executing the next statement. (Adapted from ANDIP)

Interrupt Mask A central processing unit (CPU) feature that allows the computer to ignore (mask) an interrupt request until the mask bit is disabled.

Interrupt Mask Register A special register the contents of which designate which interrupt request is enabled.

Interrupt Request An external signal that requests a temporary suspension of the normal program operation in order to permit processing of a higher priority operation.
NOTE: Multiple interrupt capability requires establishment of an interrupt-priority system.

Jump (ISO) In the execution of a computer program, a departure from the implicit or declared order in which instructions are being executed. (ANDIP)
NOTE: This is sometimes referred to as unconditional branch or unconditional jump.

Jump Instruction (ISO) An instruction that specifies a jump. (ANDIP)

K A multiplier equal to 1024 used in describing the size of memories, e.g., a 64K-bit memory contains 65,536 bits.

Last-In, First-Out (LIFO) Memory A memory from which data bytes or words can be read with the order reversed from that of the data entry.

Loader A routine, commonly a computer program, that reads data into main storage. (ANDIP)

Loop (ISO) A set of instructions that may be executed repeatedly while a certain condition prevails. (ANDIP)
NOTE: In some implementations, no test is made to discover whether the condition prevails until the loop has been executed once.

Machine Cycle The basic central processing unit (CPU) cycle in which one basic machine instruction is completed.
NOTE 1: This includes, but is not limited to, operations wherein an address may be sent to memory and one word (data or instruction) may be read or written or in which a fetched instruction may be executed.
NOTE 2: One machine cycle is made up of several clock cycles.

Machine Language The final binary program code that a computer uses directly; i.e., the numeric form of specifying every bit of every instruction in a program.

Macroinstruction (ISO) An instruction in a source language that is to be replaced by a defined sequence of instructions in the same source language. (ANDIP)
NOTE: The macroinstruction may also specify values for parameters in the instructions that are to replace it. (ANDIP)

Main Storage (ISO) A storage device whose storage cells can be addressed by a computer program and from which instructions and data can be loaded directly into registers from which the instructions can be executed or from which the data can be operated upon. (ANDIP)
See mass storage.
NOTE: For microprocessors this is usually internal RAM and/or ROM.

Mask-Programmed Read-Only Memory A fixed-program read-only memory in which the data content of each cell is determined during manufacture by the use of a mask.

Mass Storage (ISO) An auxiliary storage of very large storage capacity used for storage of data to which infrequent reference need be made. (ANDIP)

Memory Address Register The register in the central processing unit (CPU) that contains the address of the storage (memory) location being accessed.

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Memory Cell The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored and from which it can be retrieved.

Memory Integrated Circuit An integrated circuit consisting of memory cells and usually including associated circuits such as those for address selection and amplification.

Microcomputer A computer system whose central processing unit (CPU) is a microprocessor.
NOTE: A basic microcomputer includes a microprocessor, memory, and input/output facility, which may or may not be on one chip.

Microinstruction An elementary function used in a microprogram that is combined with other elementary functions in a closed subroutine to control the execution of a machine instruction.

Microprocessing Unit (MPU) The name sometimes used for the central processing unit (CPU) of a microcomputer.

Microprocessor Integrated Circuit An integrated circuit capable of:
1. operating on coded instructions,
2. carrying out, in accordance with the instructions, all of:
   (a) the acceptance of coded data for processing and/or storage,
   (b) arithmetic and logical operations on the input data together with any relevant data stored in the internal registers of the microprocessor integrated circuit and/or in external memories,
   (c) the delivery of coded data, and
3. accepting and/or delivering signals controlling and/or describing the operation or state of the microprocessor integrated circuit.

NOTE: The instructions may be fed in, built in, or held in an internal memory.

Microprogram (ISO) A sequence of elementary instructions that correspond to a computer operation, that is maintained in special storage, and whose execution is initiated by the introduction of a computer instruction into an instruction register of a computer. (ANDIP)
NOTE: A microprogram is usually implemented by firmware.

Microprogrammable Computer A computer in which the microprogram (microinstructions) in the read-only memory (ROM) used for instruction decoding can be changed, thus changing the computer's instruction set.

Mnemonic Code The symbolic names or abbreviations for instructions, registers, memory locations, etc., suggesting the definition or function thereof, e.g., "MPY" for "multiply".

Modem A device that modulates and demulates signals transmitted over data communication facilities. (ANDIP)
NOTE: The word "modem" was derived from "modulator-demodulator".

Multiprocessing Simultaneous execution of multiple programs by one computer by use of multiple CPUs operating with a common memory.

Nesting A programming technique in which a subroutine is called from a subroutine, or a program loop is enclosed within a larger loop.

Nesting Level (of a Program Loop) The number of program loops enclosing the given program loop.

Nesting Level (of a Subroutine) One less than the number of subroutine calls minus returns encountered between the main program and the given subroutine during the execution of the program.

Nibble A binary character string operated upon as a unit and shorter than a byte.
NOTE: A nibble is usually four bits.

Nonvolatile Memory A memory in which the data content is retained when power is no longer supplied to it.

Object Program (ISO) A fully compiled or assembled program that is ready to be loaded into the computer. (ANDIP)

Operand The data on or with which a mathematical or other operation is performed.

Operating System (ISO) Software that controls the execution of computer programs and that may provide scheduling, debugging, input-output control, accounting, compilation, storage assignment, data management, and related services. (ANDIP)

Operation Code (OP Code)
(1) (ISO) A code used to represent the operations of a computer. (ANDIP)
(2) A part of an instruction that usually contains only an explicit specification of the operation to be performed. (Listed as operation part in ANDIP)

Output Enable A control input to an integrated circuit that, depending on the logic level applied to it, will either permit or prevent the output of data from the device.
NOTE: When disabled the outputs will assume a low level, a high level, or a floating (high-impedance) state, depending on the design of the particular circuit.

Overflow Status Bit A bit in the condition-code register that indicates if the previous operation in the program caused an arithmetic overflow; i.e., caused a quantity to be generated that exceeded the capacity of the results register.

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Page A block of instructions, or data, or both, formed for technical or logic reasons to be treated as an entity and that can be located in main storage or in auxiliary storage; e.g., $2^8 = 256$ consecutive bytes in an 8-bit microcomputer may typically constitute a page of memory. (Adapted from ANDIP)

Parallel Operation The simultaneous execution of operations on all the bits of a byte or word.

Parallel Transmission The simultaneous transmission of all the bits of a byte or word by transmitting on separate channels or bus lines.

Peripheral Equipment (ISO) In a data processing system, any equipment, distinct from the central processing unit, that may provide the system with outside communication or additional facilities. (ANDIP)

Pointer An identifier that indicates the location of an item of data; i.e., a central processor unit (CPU) register that contains a memory address. (Adapted from ANDIP)

NOTE: Examples are a data pointer and a program counter.

Polling (1) A method used to identify the source of an interrupt request in which the interrupt request search is done serially.
(2) Interrogation of devices for purpose such as to avoid contention, to determine operational status, or to determine readiness to send or receive data. (ANDIP)

Priority Interrupt Temporary suspension of a computer program to permit execution of a program or part of a program of higher priority.

Problem Throughput A measure of the average rate of processing a problem or batch of problems.

Program Counter A counter that indicates the location of the next computer instruction to be interpreted. (Listed as instruction counter in ANDIP).

Programmable Logic Array (PLA) An array of logic elements whose interconnections can be programmed (usually mask-programmed, sometimes field-programmed) to perform a specific logic function.

NOTE: The PLA is typically a large AND gate driving a large OR gate.

Programmable Read-Only Memory (PROM) A field-programmable read-only memory that can have the data content of each memory cell altered only once.

Pushdown Stack See stack.

Random-Access Memory (RAM) A memory that permits access to any of its address locations in any desired sequence with similar access time to each location.

NOTE: The term RAM, as commonly used, denotes a read/write memory.

Read (ISO) To acquire or to interpret data from a storage device, from a data medium, or from another source. (ANDIP)

Read-Only Memory (ROM) A memory in which the contents are not intended to be altered during normal operation.

NOTE: Unless otherwise qualified, the term ROM implies that the data content is determined by the structure of the memory and is unalterable.

Read/Write Memory A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other electrical input signals.

Register (ISO) In a computer, a storage device, usually intended for some special purpose, capable of storing a specified amount of data such as a bit or a word. (ANDIP)

Relative Address (ISO) An address expressed as difference with respect to a base address. (ANDIP)

Relative Addressing (ISO) A method of addressing in which the address part of an instruction contains a relative address. (ANDIP)

Reprogrammable Read-Only Memory A field-programmable read-only memory that can have the data content of each memory cell altered more than once.

NOTE: This is a generic term and includes such devices as EAROM, EEPROM, and EPROM.

Scratch Pad Memory Read/write (RAM) memory devices or registers that are used to store temporarily intermediate results (data) or memory addresses (pointers).

Serial Access Memory A memory in which data bits or words may be accessed in a predetermined sequence only.

Serial Operation The sequential execution of operations on the bits of a byte or word.

Serial Transmission The sequential transmission of the bits of a byte or word by transmitting on a single channel or bus line.

Silo Memory Preferred term is first-in, first-out memory.

Simulate To imitate one system with another, primarily by software, so that the imitating system accepts the same data, executes the same computer programs, and achieves the same results as the imitated system. (ANDIP)

NOTE: Contrast with emulate. (ANDIP)

Slice See bit slice.

Software (ISO) Computer programs, procedures, rules, and possibly associated documentation concerned with the operation of a data processing system. (ANDIP)

NOTE: Contrast with hardware. (ANDIP)

Source Program A computer program expressed in a language from which statements are translated. (Adapted from ANDIP)

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Stack A sequence of registers or memory locations accessible in a last-in, first-out (LIFO) basis.

Stack Pointer The counter or register that addresses the current stack location.

Stand-Alone System A system that is complete within itself and does not require connection to another computer system to operate.

Static (Read/Write) Memory
A read/write memory in which the data is retained in the absence of control circuits generated inside or outside the integrated circuit.
NOTE 1: The words "read/write" may be omitted from the term when no misunderstanding will result.
NOTE 2: A static memory may use dynamic addressing or sensing circuits.
NOTE 3: Contrast with dynamic (read/write) memory.

Storage Location (ISO) An area in a storage device, usually one that can be explicitly and uniquely specified by means of an address. (ANDIP)

Subroutine (ISO) A sequenced set of statements that may be used in one or more computer programs and at one or more points in a computer program. (ANDIP)
NOTE: See closed subroutine.

Switch (ISO) In a computer program, a parameter that controls branching and is bound (fixed) prior to the branchpoint being reached. (ANDIP)

Symbolic Language A programming language that uses mnemonics to express addresses and operation codes of instructions in symbols convenient to humans rather than in machine language. (Adapted from ANDIP)

Synchronous Operation
Circuit operation using a common timing source (clock) to time circuit or data transfer operations.

Test Instruction An instruction that checks the condition of data and sets status or overflow flag bits for a subsequent branch instruction.
NOTE: In some instances, test and branch are considered a dual operation within a single instruction.

Unconditional Branch (ISO) Deprecated term for unconditional jump. (ANDIP)

Unconditional Jump (ISO) A jump that takes place whenever the instruction that specified it is executed. (ANDIP)

Universal Asynchronous Receiver Transmitter (UART)
Universal Synchronous Receiver Transmitter (USRT)
Universal Synchronous/Asynchronous Receiver Transmitter (USART)
A circuit used in asynchronous, synchronous, or synchronous/asynchronous, respectively, data communication applications to provide all the necessary logic to recover data in a serial-in, parallel-out fashion and to transmit data in a parallel-in, serial-out fashion.
NOTE: It is usually full-duplex, i.e., can transmit and receive simultaneously with the option to handle various data word lengths.

Utility Program A computer program in general support of the processes of a computer; for instance, a diagnostic program, a trace program, a sort program. Synonymous with service program. (ANDIP)

Vectored Interrupt An interrupt system in which each interrupt can be immediately serviced without having to determine which interrupt has occurred by polling.

Volatile Memory A memory in which the data content is lost when power is no longer supplied to it.

Word A character string or a binary element string that it is convenient for some purpose to consider as an entity. (ANDIP)

Write To make a permanent or transient recording of data in a storage device or on a data medium. (ANDIP)

EXPLANATION OF SYSTEM/SOFTWARE SECTIONS

2. MICROCOMPUTER SYSTEMS

IN ORDER OF: (1)DATA BITS (2)MANUFACT. CODE & (3)SYSTEM TYPE No.

LINE No.	[3] SYSTEM TYPE No.	ORGANIZ-ATION: [1] DATA BITS	ARCHI-TECT-URE	SYS. CONFIGURATION: ADDRESSABLE MEMORY (RAM/ROM) (BYTES)	I/O DEV @PT WIDTH (D/WDTH)	No. BASIC INSTR	No. MICRO ADDR MODE	INTERR-UPT LEVEL No. & TYPE	INSTRUCT TIME-TYP §CLK CYC *-MIN (s)	No. GEN PUR-POSE REG	STACK LEVEL	SYMBOL: PT-PORT V-VECTORED P-PRIORITY M-MULTIPLE OTHER CAPABILITIES	INSTR SET REF. No.	SYSTEM DWG.	[2] MFR. CODE

Purpose: To provide a quick cross-section review of currently available microcomputer systems, where "systems" refers the highest level of general purpose microprocessor-based product produced. A liberal interpretation of the word "system" is used in this section for the express purpose of including each manufacturer's "system-level" features and characteristics, regardless of his level of physical system.

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3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE

Purpose: To present the hardware product line of microcomputer-related components of each manufacturer. Gives the reader a feel for the depth of each manufacturer's involvement in microcomputer hardware production. The absence of a COMP (Computer) component class for some manufacturers simply indicates that some systems are actually custom-specified and thus preclude assignment of specific system type numbers. For additional technical detail on microcomputers, microprocessors, and support chips, consult the TYPE No. CROSS INDEX (Section 1).

4.SYSTEM SOFTWARE INDEX

IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	[4] SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	[2] GENERIC I.D. $-MULTI-SYSTEM APPLICATION	[3] SYSTEM TYPE No.	CATE-GORY	S O F T W A R E L I B R A R Y NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	[1] MFR. CODE

Purpose: To present the software product line and general software support and compatability associated with each manufacturer's microcomputer system(s). Distinguishes between software and firmware packages. Companies that produce microcomputer-compatible software, but no hardware, are listed only in this section.

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5. INSTRUCTION SET INDEX

IN ORDER OF: (1)MANUFACTURER CODE &(2)SYSTEM TYPE No.

LINE No.	[2] SYSTEM TYPE No. (IS-D.A.T.A. PREFIX)	No. BASIC INSTR	TOTAL No. INSTRUCTIONS W/VARIATIONS	SYMBOLS: DESCRIPTION	INSTRUCTION SET REFERENCE No.	INSTRUCT FORMAT DWG.	[1] MFR. CODE

Purpose: To direct the reader to the instruction set associated with the System Type No. of interest. Instruction Sets are listed together in a separate section in order of Instruction Set No.

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6. SYSTEM INTERFACE

IN ORDER OF: (1)DATA BITS (2)MFR. CODE (3)SYSTEM TYPE No.

LINE No.	[3] SYSTEM TYPE No.	[1] DATA BITS	ADDRESSING: TYPE	ISOLATED DEVICES @ PORT WIDTH	MEMORY-SPACE DEV @ PT WIDTH	OPERATING MODE: TYPE of OP.	No. SERIAL BITS	INTERRUPT: V-vectored Pr-priority P-poll TYPE	No LNS	No LEV	S-softw.DMA I-interrupt INITI-ATION	DMA LOC.	I/O LINES: ADRS	SENS	CNTL	FLAG	MISC	TRANSFER: INSTR TIME (s)	OPER. CAPABILITY CODE	MAXIMUM BAUD RATE: ASYNC (BPS)	SYNC. (BPS)	SYSTEM DWG.	[2] MFR. CODE

Purpose: To expand on the information relating to System I/O Capability, briefly noted in the "System Configuration" column of Section 2.

EXPLANATION OF COMPONENT SECTIONS

10. MICROPROCESSORS

IN ORDER OF: (1)DATA BITS (2)ARCHITECTURE (3)No. BASIC INSTRUCTIONS & (4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZ. 1 DATA BITS	ORGANIZ. 2 ARCHI-TECT-URE	TECH NOL.	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RAM/ROM %BIT CONFIG MIXED ▼-bits (BYTES)	MAX. CLOCK FREQ. (Hz)	No Øs	OPER. VOLTAGES V1 (V)	V2 (V)	V3 (V)	MAX. OPER. PWR. DISS. (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	3 No. BASIC INSTR	A M D O D R E	DRAWINGS CPU INTERNAL ARCHIT ECTURE	DRAWINGS OUTLINE	MFR. CODE

Purpose: Provide a detailed cross-section of currently available microprocessor chips, chip sets and cards. Allows quick comparison of important features of each device shown. Tied to system component information (Section 3) through manufacturer's code.

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11. READ-WRITE MEMORIES (RAMS)

IN ORDER OF: (1)No. WORDS (2)BITS PER WORD (3)WORST CASE R/W CYCLE TIME &(4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZATION 1 No. WORDS	ORGANIZATION 2 BITS PER WORD	MODE	TECHN -OLOGY	3 W/C Min. Rd/Wr CYC.TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED POWER SUPPLY SPAN NEG. (V)	RATED POWER SUPPLY SPAN POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE	MFR. CODE

12. READ-ONLY MEMORIES (ROMS)

IN ORDER OF: (1)TYPE CODE (2)No. WORDS (3)BITS/WORD (4)ACCESS TIME & (5)TYPE No.

LINE No.	5 TYPE No.	1 TYPE CODE	ORGANIZATION 2 No. WORDS	ORGANIZATION 3 BITS PER WORD	OP. MODE PCGM	OP. MODE OD E	TECHN OLOGY	4 MAX. ACCESS TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYM:*-MIN Δ-MAX S-STATIC D-DYNAMIC DESCRIPT.	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE	MFR. CODE

Purpose: Master-reference to family-designed memory options for each system. Tied to system component information (Section 3) through manufacturer's code.

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13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE *-MIN %-OUTPUT †-TYPICAL ☑-ABS.MAX. DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE	2 MFR. CODE

Purpose: To give an orderly arrangement of family-designed interface and support components. Grouped in order of Type Code to facilitate evaluation of specific application or interface situations.

EXPLANATION OF FEATURES, CHARACTERISTICS AND RATINGS

Addressing – Isolated Devices (Section 6)

Number of addressable I/O devices (at the stated port width) that are not part of unused memory space.

Addressing – Memory Space Devices (Section 6)

Number of addressable I/O devices (at the stated port width) that are part of unused memory space.

Addressing Type (Section 6)

Type of I/O addressing available with this system. M - memory space; I - isolated; B - memory space and isolated.

Architecture (Section 2)

D.A.T.A. code describing the basic physical makeup of the microcomputer system. Includes custom specified chip family (ChF) and card family (CdF) systems, computers-on-a-card (CoC), microcontrollers (Computers-on-a-chip (μCT), single-component computers (SCC), and pre-packaged stand-alone microcomputers (SYS).

Architecture (Section 10)

D.A.T.A. code describing the basic physical makeup of the functional central processing unit. Includes single chip (CHIP) and chip set (ChS) microprocessors, modular/printed circuit board (MOD) types, plus multi-board card set (CdS) versions.

Component Class (Section 3)

D.A.T.A. code describing the basic functional capability of the hardware products listed. Prepackaged full computing capability is shown by the code COMP, indicating a system architecture of computer-on-a-card or stand-alone system. uCT code indicates single-chip microcontroller and computer-on-a-chip packages. CPU code includes chip plus chip/card set microprocessors. Combinational memory, I/O, and support components are separated into application groups by means of IO-1 . . . IO-n component classification codes. Explanation of these codes is found in the Interpreter Cards at the back of the book. RAM, ROM, PROM memory classes are obvious. Development hardware (DEV) and compatible peripheral unit (PERIP) codes are given for completeness.

Component Sub-Class (Section 3)

D.A.T.A. code indicating the basic physical packaging of the Component Class, (CdS - card set, ChS - chip set, Chip, MOD - Modular/printed circuit card, UNIT - chassis package, stand-alone unit).

CPU Internal Architecture (Section 10)

Logic/architectural drawing of the Central Processing Unit.

Generic I.D. (Generic System Index, Section 4)

In the GENERIC SYSTEM INDEX the Generic I.D. relates microprocessor and microcomputer hardware from individual manufacturers to familiar "generic numbers". In Section 4, microcomputer-compatible software is tied to the same "generic numbers".

Input Logic Levels (Sections 10,11,12,13)

HIGH – The minimum input voltage at which the input is in the "ON" or "1" state.

LOW – The maximum input voltage at which the input is in the "OFF" or "0" state. When input logic levels are not specified, the output levels are, and a symbol is used to indicate this condition. Tri-state devices are noted by a symbol in the HIGH column.

Interrupt – Type, No. Lines, No. Levels, Initiation, DMA (Section 6)

System interrupt capability, method of initiation, and existence (or not) of DMA capability. CPU - DMA on CPU; EXT - external DMA; NA - DMA not available.

EXPLANATION OF FEATURES, CHARACTERISTICS AND RATINGS

Maximum Clock Frequency (Section 10)

Maximum frequency of operation as specified by manufacturer. Number of phases noted in adjacent column.

Maximum Operating Power Dissipation (Sections 10,11,12,13)

Total operating power dissipation for the microprocessor chip, chip set, module or card set, as specified by manufacturer. Also applies to memory and I/O devices.

Mode (Sections 11,12)

Represents the basic storage method of the device; Static (S) or Dynamic (D). Static types use flip-flops that retain their state indefinitely, as long as the supply voltage is maintained. Dynamic types require the repetitive application of control and refresh signals in order to retain stored data.

Number of Basic Instructions (Section 5)

Typically the number of basic instructions as specified by the manufacturer, or the number of separate basic mnemonics availabe for listing.

Operating Mode – No. Serial Bits (Section 6)

Maximum number or range of serial input bits capable of being handled by the system.

Operating Mode – Type Of Operation (Section6)

Operating mode capability of the system. P - parallel; S - serial; PS - parallel and serial.

Operating Voltages – V_1, V_2, V_3 (Section 10)

Rated operating voltages under typical operating conditions. Specified typically as the maximum negative or positive power supply value. Consult logic/block diagram for detail.

Operating Temperature (Sections 10,11,12,13)

The temperature range over which the manufacturer indicates that the device will operate.

Organization (Sections 11,12)

Number of Words and Bits/Word. Represents the capacity of the memory. By connecting the outputs of two or more devices in parallel, the total number of words may be expanded; similarly, by connecting the address inputs in parallel, the number of bits/word can be expanded.

Ram/Rom (Section 10)

Basic RAM and ROM memory increments for the particular microprocessor listed.

Rated Power Supply Span (Sections 11,12,13)

The range of positive and negative supply voltages at which the characteristics are specified by the manufacturer. If more than one negative or positive voltage is necessary for the operation of the device, the maximum negative or positive value is specified. The logic/block drawing should then be consulted for the actual voltages required to operate the device.

EXPLANATION OF FEATURES, CHARACTERISTICS AND RATINGS

System Configuration I/O (Section 2)

Number of addressable I/O devices at a given port width. Symbol ☑ indicates I/O addresses are part of unused memory.

System Configuration Memory (Section 2)

Addressable memory (RAM/ROM) capacity of the system (type no.) listed.

System Drawings (Sections 2,6)

System logic drawings describing any level of physical system, pre-packaged or available in chip/card sets, included to provide information on typical system bus architecture and interconnection capability.

Technology (Sections 3,10,11,12)

Relates the component to the main developing semiconductor technologies for microcomputer devices.

Total Number Of Instructions (Section 5)

Number of basic instructions plus additions resulting from multiple address modes and variations in execution conditions.

Transfer – I/O Capability (Section 6)

Operational capability/compatibility of the system with major logic classes and major interface standards. A - TTL, B - RS232, etc.

Transfer – Instruction Time (Section 6)

Typical register-to-I/O software instruction time.

Type Code (Section 13)

Basic classification of Interface and Support devices, defined by D.A.T.A. Intended to group I/O and Suppor components into typical applications areas. Codes explained in Symbols and Codes at back of book.

Typical Instruction Time (Section 2)

An instruction execution time or range of execution times intended to be indicative of microcomputer/microprocessor speed. Listed as specified by the manufacturer. Typically representative of fastest clock operating frequency.

Worst-Case Minimum, Read/ Write Cycle Time (Section 11)

The shortest time interval between the start of a cycle in which the memory is read and new data are entered, and the end of that cycle. The implication is that the operation is performed correctly.

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Δ-Registered with JEDEC by this manufacturer

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M68SFDU1112E		67 - 72
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M68SFDU2000	MOTA	67 - 73
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M68SP702	MOTA	67 - 81
M68SP703	MOTA	67 - 82
M68SP779	MOTA	67 - 83
M68SP781	MOTA	67 - 84
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M68SXS220	MOTA	67 - 77
M68SXS	MOTA	67 - 78
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M68XAE6812D	MOTA	65-103
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M2900	MOTA	26 - 46
		110 - 6
M3856B1	SGAI	80 - 44
		139-104
M3856D1	SGAI	80 - 46
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M3857B1	SGAI	80 - 45
M3857D1	SGAI	80 - 51
M3870B1	SGAI	80 - 47
M3870D1	SGAI	80 - 48
M6800	MOTA	28 - 25
		110 - 50
M6800B	MOTA	68 - 58
M6809DB	MOTA	63 - 87
M6809EXORD1	MOTA	65 - 31
M6809EXORD2	MOTA	65 - 32
M6809EXORS1	MOTA	65 - 33
M6809EXORS2	MOTA	65 - 34
M6809EXORUD1		65 - 35
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M6809EXORUD2		65 - 36
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M6809EXORUS1		65 - 37
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M6809EXORUS2		65 - 38
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M6809FDS2-2	MOTA	68 - 62
M6809FDS2-3	MOTA	68 - 63
M6809PP	MOTA	65 - 47
M6809TERMD1	MOTA	63 - 88
M6809TERMD2	MOTA	63 - 85
M6809TERMS1	MOTA	63 - 89
M6809TERMS2	MOTA	63 - 86
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	MOTA	59 - 68
		114 - 87
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	ITL	59 - 69
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JANM38510/42001CQB		
	ITL	59 - 70
		115 - 33
M54550P	MITJ	59-102
		137 - 45
M54551K	MITJ	59 - 94
		129 - 74
M54552P	MITJ	59-103
		138 - 27
M58494-XXXP	MITJ	60 - 7
		112 - 12
M58609-04S	MITJ	59 - 96
M58609-XXS	MITJ	59 - 97
		131 - 99
M58620-001S	MITJ	59 - 98
M58620-XXXS	MITJ	59 - 99
		131-100
M58710S	MITJ	59 - 93
		115 - 34
M58730-001S	MITJ	59-104
M58730-XXXS	MITJ	60 - 1
		126 - 79
M58731-001S	MITJ	60 - 2
M58731-XXXP	MITJ	60 - 3
		127 - 27
M58731-XXXS	MITJ	60 - 4
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M58740P	MITJ	59-100
		136 - 28
M58740S	MITJ	59-101
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M58840-XXXP	MITJ	60 - 8
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M58842S	MITJ	60 - 9
M68451	MOTA	68 - 59
MACE29/800	MOTA	64 - 4
MAD835	CLI	37 - 70
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MAI03	WTK	89 - 32
MAI04	WTK	89 - 33
MAI10	WTK	89 - 34
MAI11	WTK	89 - 35
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MAS2A	WLD	89 - 3
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		139 - 14
MAS-842	CLI	37 - 51
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MASM68R	MCT	99 - 97
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MB7	SSM	83 - 54
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MB9	SSM	83 - 48
MB10	SSM	83 - 55
MBC004	MUP	69 - 56
MBC008	MUP	69 - 57
MBC010-65	SYK	84 - 25
MBC010-68	SYK	84 - 72
MBC012	MUP	69 - 58
MBC016	MUP	69 - 59
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MBC016-3	SYK	84 - 60
MBC016L	SYK	84 - 61
MBC016L-3	SYK	84 - 62
MBC020-65	SYK	84 - 26
MBC020-68	SYK	84 - 73
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MBC048	MUP	69 - 61
MBC064	MUP	69 - 62
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MC8T96L	MOTA	66-103
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MC68A00P	MOTA	64-109
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MC68A09EP	MOTA	65 - 1
		114 - 44
MC68A09L	MOTA	65 - 2
		114 - 45
MC68A09P	MOTA	65 - 3
		114 - 46
MC68A21L	MOTA	66 - 87
		136 - 33
MC68A21P	MOTA	66 - 88
		136 - 34
MC68A29L	MOTA	68 - 52
		135 - 69
MC68A29P	MOTA	68 - 53
		135 - 70
MC68A40L	MOTA	66 - 2
		128 - 56
MC68A40P	MOTA	66 - 3
		128 - 57
MC68A44L	MOTA	66 - 13
MC68A44P	MOTA	66 - 14
MC68A50L	MOTA	66 - 41
		133 - 5
MC68A50P	MOTA	66 - 42
		133 - 6
MC68A52CL	MOTA	66 - 43
		133 - 7
MC68A52CP	MOTA	66 - 44
		133 - 8
MC68A52L	MOTA	66 - 45
		133 - 9
MC68A52P	MOTA	66 - 46
		133 - 10
MC68A54CL	MOTA	66 - 47
		133 - 11
MC68A54CP	MOTA	66 - 48
		133 - 12
MC68A54L	MOTA	66 - 49
		133 - 13
MC68A54P	MOTA	66 - 50
		133 - 14
MC68B00L	MOTA	65 - 4
		114 - 92
MC68B00P	MOTA	65 - 5
		114 - 93
MC68B09EL	MOTA	65 - 6
		114 - 47
MC68B09EP	MOTA	65 - 7
		114 - 48
MC68B09L	MOTA	65 - 8
		114 - 49
MC68B09P	MOTA	65 - 9
		114 - 50
MC68B21L	MOTA	66 - 89
		136 - 35
MC68B21P	MOTA	66 - 90
		136 - 36
MC68B29L	MOTA	68 - 54
		135 - 71
MC68B29P	MOTA	68 - 55
		135 - 72
MC68B40L	MOTA	66 - 4
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MC68B40P	MOTA	66 - 5
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MC68B44L	MOTA	66 - 15
MC68B44P	MOTA	66 - 16
MC68B50L	MOTA	66 - 51
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MC68B50P	MOTA	66 - 52
		133 - 16
MC68B52L	MOTA	66 - 53
		133 - 17
MC68B52P	MOTA	66 - 54
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MC68B54L	MOTA	66 - 55
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MC68B54P	MOTA	66 - 56
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MC160-02	WDC	88 - 22
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MC1610	GIC	49 - 53
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MC2901ALM	MOTA	63-109
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MC2901LC	MOTA	63-110
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MC2901LM	MOTA	64 - 1
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MC2902FM	MOTA	64 - 49
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MC2902LM	MOTA	64 - 51
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MC2902PC	MOTA	64 - 52
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1. TYPE No. CROSS INDEX

IN TYPE NUMBER SEQUENCE

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MK9704	MOS	60 - 85
MK30000	MOS	62 - 89
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MK31000P	MOS	62 - 90
		127 - 21
MK32000	MOS	62 - 91
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MK34000P	MOS	62 - 92
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MK36000	MOS	62 - 93
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MK77650	MOS	62 - 33
MK77650-4	MOS	62 - 34
MK77651	MOS	62 - 25
MK77651-4	MOS	62 - 26
MK77652	MOS	61 - 75
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MK77665	MOS	61 - 66
MK77669	MOS	61 - 68
MK77669-4	MOS	61 - 69
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MK77751	MOS	62 - 79
MK77752	MOS	62 - 80
MK77752-4	MOS	62 - 81
MK77753	MOS	62 - 46
MK77753-4	MOS	62 - 47
MK77754	MOS	62 - 82
MK77754-4	MOS	62 - 83
MK77755	MOS	62 - 84
MK77756	MOS	62 - 85
MK77757	MOS	62 - 86
MK77758	MOS	62 - 12
MK77759	MOS	62 - 13
MK77850	MOS	61 - 90
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MK77850-4	MOS	61 - 91
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MK77851	MOS	61 - 83
MK77950	MOS	61 - 94
MK77950-4	MOS	61 - 95
MK77951	MOS	61-101
MK77951-4	MOS	61 - 96
MK77958	MOS	61 - 92
MK77963	MOS	61 - 76
MK77963-4	MOS	61 - 77
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MK78033	MOS	61 - 31
MK78035	MOS	61 - 32
MK78036	MOS	61 - 33
MK78037	MOS	30 - 9
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MK78102	MOS	61-103
MK78103	MOS	61 - 37
MK78104	MOS	61 - 38
MK78106	MOS	61 - 39
MK78107	MOS	62 - 87
MK78108	MOS	62 - 88
MK78109	MOS	61 - 40
MK78110	MOS	61 - 41
MK78111	MOS	62 - 14
MK78112	MOS	61 - 42
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MK78121	MOS	61 - 84
MK78122	MOS	61 - 45
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MK78125-001	MOS	61-105
MK78125-01	MOS	61-106
MK78125-1	MOS	61-107
MK78125-2	MOS	61-108
MK78125-3	MOS	61-109
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MK78146	MOS	61 - 64
MK78155	MOS	61 - 48
MK78157	MOS	61 - 49
MK78158	MOS	61 - 50
MK78164	MOS	61 - 51
MK78166	MOS	61 - 52
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MK78168	MOS	61 - 54
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MK78170	MOS	61 - 56
MK78171	MOS	61 - 57
MK78172-7	MOS	61 - 98
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MK78175-40	MOS	61 - 72
MK78177-26	MOS	61 - 73
MK78192	MOS	61 - 65
MK78962	MOS	61 - 58
MK79001	MOS	61 - 3
MK79002	MOS	61 - 4
MK79003	MOS	61 - 28
MK79030	MOS	61 - 5
MK79032	MOS	61 - 6
MK79052	MOS	62-109
MK79053	MOS	61 - 27
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MK79066	MOS	61 - 23
MK79076	MOS	61 - 7
MK79077	MOS	61 - 8
MK79078	MOS	61 - 9
MK79079	MOS	61 - 99
MK79081	MOS	62 - 38
MK79082	MOS	61-100
MK97400	MOS	28 - 14
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		112-100
MK97401	MOS	28 - 15
		60-101
		112-101
MK97402	MOS	28 - 16
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MK97403	MOS	28 - 17
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MK97404	MOS	28 - 18
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MK97405	MOS	28 - 19
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MKB3870P10	MOS	28 - 20
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MKB3880P14	MOS	61 - 88
MKB3880P34	MOS	61 - 89
		115 - 38
MKB3881P14	MOS	62 - 32
MKB3882P14	MOS	62 - 6
MKB3882P20	MOS	62 - 7
MKB4027F84	MOS	63 - 1
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MKB4027J2	MOS	62 - 61
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MKB4027J3	MOS	62 - 62
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MKB4027J4	MOS	62 - 63
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MKB4027J83	MOS	62 - 64
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MKB4027J84	MOS	62 - 65
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MKB4104J4	MOS	62 - 66
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MKB4104J5	MOS	62 - 67
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MKB4104J6	MOS	62 - 68
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MKB4104J85	MOS	62 - 69
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MKB4104J86	MOS	62 - 70
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MKB4116E84	MOS	122 - 96
MKB4116F84	MOS	62 - 71
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MKB4116J2	MOS	62 - 72
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MKB4116J3	MOS	62 - 73
		122 - 99
MKB4116J4	MOS	62 - 74
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MKB34000P84	MOS	62 - 95
MKB34000P	MOS	62 - 96
MKB36000P80	MOS	62 - 97
MKB36000P84	MOS	62 - 98
MKB36000P	MOS	62 - 99
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MLP8020	HEU	51 - 11
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MLP8030	HEU	51 - 16
MLP8032	HEU	51 - 15
MLP8035	HEU	51 - 9
MLP8040	HEU	51 - 13
MLP8061	HEU	51 - 20
MLP8062	HEU	51 - 21
MLP8065	HEU	51 - 10
MLP8070	HEU	51 - 22
MLP8072	HEU	51 - 23
MLP8080	HEU	27 - 75
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MLP8082	HEU	51 - 18
MLP8084	HEU	51 - 14
MLP8090	HEU	51 - 8
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MLSI2480	MATC	58 - 13
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MLSI-11/23AA	MDB	59 - 1
MLSI-11/23AC	MDB	59 - 2
MLSI-11B	MDB	59 - 6
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MLSI-DLV11E	MDB	59 - 16
MLSI-DLV11J	MDB	59 - 17
MLSI-DR11B	MDB	59 - 39
MLSI-DRV11C	MDB	59 - 19
MLSI-DRV11P	MDB	59 - 7
MLSI-DSD-110	MDB	59 - 30
MLSI-DSD-440	MDB	58 - 97
MLSI-DT-1761	MDB	59 - 23
MLSI-DUV11	MDB	59 - 18
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MLSI-KD11F	MDB	58-105
MLSI-KD11HA	MDB	58-106
MLSI-KD11HB	MDB	58-107
MLSI-KD11HC	MDB	58-108
MLSI-KD11HD	MDB	58-109
MLSI-KEV11	MDB	59 - 28
MLSI-KPV11-A	MDB	58 - 98
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MLSI-MRV-003	MDB	59 - 27
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MLSI-MSV11-DC		59 - 41
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MLSI-MSV11-DD		59 - 42
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MLSI-PC11	MDB	59 - 11
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MLSI-REV11C	MDB	59 - 9
MLSI-RL01AK	MDB	58-101
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MLSI-SMU	MDB	59 - 29
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MLSI-SR-VXSSBA		59 - 4
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MLSI-SR-VXS23BA		59 - 5
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MLZ800A	HEU	51 - 33
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MM1-EEE	CLI	37-104
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MM1-MSC	CLI	37 - 87
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MM1-PCON	CLI	37 - 98
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MM78	RKW	26 - 69
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MM5782/129	NSC	26 - 64
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MM8080A	MIM	59 - 75
MM8080AL	MIM	59 - 76
MM57109	NSC	71-100
MM57126	NSC	71 - 99
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MM57129N	NSC	71 - 96
MM57140N	NSC	26 - 66
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MM57152N	NSC	26 - 67
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MMI57S373J	MMI	60 - 38
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MMI57S374J	MMI	60 - 34
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MMI57S376J	MMI	60 - 35
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MMI57S378J	MMI	60 - 36
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MMI57S380J	MMI	60 - 39
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MMI57S382J	MMI	60 - 40
		140 - 12
MMI67LS315J	MMI	60 - 53
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MMI67LS315N	MMI	60 - 54
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MMI67S373J	MMI	60 - 66
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MMI67S373N	MMI	60 - 67
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MMI67S374J	MMI	60 - 55
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MMI67S374N	MMI	60 - 56
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MMI67S378J	MMI	60 - 59
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MMI67S378N	MMI	60 - 60
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MMI67S380J	MMI	60 - 61
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MMI67S380N	MMI	60 - 62
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R29683DC	RTN	80- 34
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R29683DM	RTN	80- 35
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S6851	AMI	31- 9
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SBP0401AMJ	TII	84- 99
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SN74S271J	TII	86-101
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SN74S373N	TII	85 - 10
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SN74S481N	TII	84-105
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ST-800-ADX48D		44 - 3
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ST-6800B1C	DTL	43 - 84
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SW-26-1504	RAD	104 - 17
SW-26-1505	RAD	104 - 18
SW-26-1551	RAD	104 - 19
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SW-26-1556	RAD	104 - 22
SW-26-1563	RAD	104 - 23
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SW-26-1703	RAD	104 - 30
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SW-26-1711	RAD	104 - 38
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SW-26-1803	RAD	104 - 42
SW-26-1805	RAD	104 - 43
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SW-A6809R	MCT	99-102
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Δ-Registered with JEDEC by this manufacturer

1. TYPE No. CROSS INDEX

IN TYPE NUMBER SEQUENCE

Δ-Registered with JEDEC by this manufacturer

1. TYPE No. CROSS INDEX

IN TYPE NUMBER SEQUENCE

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SW-CRPPS8/10,20,PDP	BSO	92- 19
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SW-CX1802/DGC	BSO	92- 84
SW-CX1804/10,20,PDP	BSO	92- 95
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SW-CX2000/10,20,PDP	BSO	92-107
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SW-CX3870/DGC	BSO	93- 10
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SW-CX4004/DGC	BSO	93- 22
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SW-CX4040/DGC	BSO	93- 34
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SW-CX6500/DGC	BSO	93- 46
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IN TYPE NUMBER SEQUENCE

Δ-Registered with JEDEC by this manufacturer

1. TYPE No. CROSS INDEX

IN TYPE NUMBER SEQUENCE

Δ-Registered with JEDEC by this manufacturer

1. TYPE No. CROSS INDEX

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	NECM	
uPD8255C-E	NECD	70 - 95
		136 - 49
uPD8257C	NECJ	70 - 84
	NECM	130 - 44
uPD8257C-5	NECJ	70 - 2
	NECM	130 - 45
uPD8259-5	NECM	70 - 81
uPD8259C	NECJ	70 - 82
	NECM	129 - 83
uPD8259C-5	NECJ	70 - 1
uPD8259D	NECM	70 - 83
		129 - 84
uPD8279C-5	NECJ	70 - 88
	NECM	
uPD8355C	NECJ	70 -110
	NECM	140 - 98
uPD8355D	NECJ	70 - 8
		140 - 99
uPD8741AC	NECM	70 - 96
		136 - 52
uPD8741AD	NECM	70 - 97
		136 - 53
uPD8748D	NECM	28 - 51
		70 - 67
		115 - 98
uPD8755AD	NECM	71 - 1
uPSeries	WLD	29 - 15
		88 - 84
		110 - 81
uSA	MSS	68 -108
UC1671B	WDC	88 - 28
		133 -109
UC1971A	WDC	88 - 29
		133 -110
UC1971B	WDC	88 - 30
		134 - 1
UPI41	ITL	27 -107
		110 - 47
UPP101	ITL	53 -103
UPP102	ITL	53 -104
UPP103	ITL	53 - 89
UPP-2700	OAE	74 - 57
USC10KIT	ITL	54 -105
USC820	ITL	54 -106
UVS-11E	OAE	74 - 58
VB1B	SSM	83 - 44
VB2	SSM	83 - 45
VDB	XIT	89 - 77
VDI	OBJ	74 - 60
VDP-40	IMS	27 - 85
		52 - 71

Δ-Registered with JEDEC by this manufacturer

1. TYPE No. CROSS INDEX

IN TYPE NUMBER SEQUENCE

Δ-Registered with JEDEC by this manufacturer

2. MICROCOMPUTER SYSTEMS

IN ORDER OF: (1)DATA BITS (2)MANUFACT. CODE & (3)SYSTEM TYPE No.

LINE No.	3 SYSTEM TYPE No.	ORGANIZ -ATION 1 DATA BITS	ARCHI -TECT -URE	SYS. CONFIGURATION ADDRESSABLE MEMORY (RAM/ROM) (BYTES)	I/O DEV @PT WIDTH (D/WDTH)	No. BASIC MICRO INSTR	No. ADDR MODE	INTERR -UPT LEVEL No. & TYPE	INSTRUCT TIME-TYP §CLK CYC *-MIN (s)	No. GEN PUR- POSE REG	STACK LEVEL	SYMBOL: PT-PORT V-VECTORED P-PRIORITY M-MULTIPLE OTHER CAPABILITIES	INSTR SET REF. No.	SYSTEM DWG.	2 MFR. CODE
1	MC14500B	1	ChF	256	32/1	16			100n			Industrial Control Unit	IS73	S89	MOTA
2	S2000	4	uCT	256/8k▼	1/8	51			4.5u		3	Hi-Volt DisplayDr Avail	IS113	*	AMI
3	S2150	4	uCT	320/12k▼	1/8	51			4.5u		3	Hi-Volt DisplayDr Avail	IS113	*	AMI
4	S2400	4	uCT	512/32k▼	1/8	59		2p	4.5u		5	Hi-Volt DisplayDr Avail	IS113	*	AMI
5	Am2900	4	ChF	4.0k	16/4	512△	4	VP	150n	16	4	Microprogrammable	IS63	S66	AMV
6	ASC40	4	CdF		256/4	45		P	10.8u	7		Uses Intel 4040 MPU	IS22		APS
7	IMC40	4	CdF	8.0k	320/4	60			10.8u	24		Uses C4040CPU	IS56	S58	COM
8	SYSTEM4	4	CdF	10k/32k	1024/1	45			12.5u*	24		Uses Intel 4004 CPU	IS14		DSI
9	SYSTEM4A	4	CdF	40k/8.0k	1024/1	60			10.8u*	24		Uses Intel 4040 CPU	IS14		DSI
10	SYSTEM4B	4	CdF	40k/8.0k	1024/1	60			7.0u*	24		Uses Intel 4040CPU	IS14		DSI
11	F2900	4	ChF	16/16	16/4	512△	4		75n*	16	4	Uses 2901CPU;Microprogrm	IS63		FSC
12#	HMCS42	4	uCT	32/512	4/1	51			10u	4	2	One Chip Microcomputer	IS115		HITJ
13#	HMCS42C	4	uCT	32/544	4/1	51			10u	4	2	One Chip Microcomputer	IS115		HITJ
14#	HMCS43	4	uCT	80/1k	1/4	71		2P	10u	6	3	One Chip Microcomputer	IS115a		HITJ
15#	HMCS43C	4	uCT	80/1k	1/4	71		2P	10u	6	3	One Chip Microcomputer	IS115a		HITJ
16#	HMCS44A	4	uCT	160/2k	1/4	71			10u	8	4	One Chip Microcomputer	IS115a		HITJ
17#	HMCS44C	4	uCT	160/2k	1/4	71			10u	8	4	One Chip Microcomputer	IS115a		HITJ
18#	HMCS45A	4	uCT	160/2k	6/4	71			10u	6	4	One Chip Microcomputer	IS115a		HITJ
19#	HMCS45C	4	uCT	160/2k	6/4	71			10u	6	4	One Chip Microcomputer	IS115a		HITJ
20	3000ITL	4	ChF	512	16/8	512△	5			11		MCU And CPE,I/O Expands	IS13	S4	ITL
21	MCS4	4	ChF	32k	128/4	46	4	V	10.8u	16		3 Subroutine Nesting	IS22a	S40	ITL
22	MCS40	4	ChF	64k	128/4	60		V	10.8u		7	Expanded MCS4	IS22		ITL
23#	MN1400	4	uCT	256/8k▼	3/4,1/8	75	2		10u		2	One Chip Microcomputer	IS72	S88	MATJ
24#	MN1402	4	uCT	128/8k▼	4/4,1/5	57	2		10u		2	One Chip Microcomputer	IS72	S147	MATJ
25#	MN1403	4	uCT	64/4k▼	3/4	50	2		10u		2	One Chip Microcomputer	IS72	S148	MATJ
26#	MN1404	4	uCT	64/4k▼	1/4,1/6	48	2		10u		2	One Chip Microcomputer	IS72	S149	MATJ
27#	MN1405	4	uCT	512/16k▼	3/4,1/8	75	2		10u		2	One Chip Microcomputer	IS72	S150	MATJ
28#	MN1430	4	uCT	256/8k▼	3/4,1/8	75	2		10u		2	One Chip Microcomputer	IS72	S88	MATJ
29#	MN1432	4	uCT	128/8k▼	4/4,1/5	58	2		15u		2	One Chip Microcomputer	IS72	S147	MATJ
30#	MN1435	4	uCT	512/16k▼	3/4,1/8	75	2		15u		2	One Chip Microcomputer	IS72	S150	MATJ
31#	MN1450	4	uCT	256/8k▼	3/4,1/8	75	2		10u		2	One Chip Microcomputer	IS72	S88	MATJ
32#	MN1453	4	uCT	256/4k▼	3/4	75	2		10u		2	One Chip Microcomputer	IS72	S148a	MATJ
33#	MN1454	4	uCT	256/4k▼		48			10u		2	One Chip Microcomputer	IS72	S88	MATJ
34#	MN1455	4	uCT	512/16k▼		75			10u		2	One Chip Microcomputer	IS72	S88	MATJ
35#	MN1498	4	uCT	256/8k▼	2/4,1/9	68	2		10u		2	uComp W/Ext Inst Mem	IS72	S151	MATJ
36#	MN1499	4	uCT	256/16k▼	4/4	75	2		10u		2	Sys Evaluator uC Chip	IS72	S152	MATJ
37#	MN1499A	4	uCT	512/16k▼	3/4,1/5	75	2		10u		2	Sys Evaluator uC Chip	IS72	S152a	MATJ
38#	MN1542	4	UCT	152/2k	6/4	124		4M	2.0u		16	See Device Number Sec 3		S172	MATJ
39#	MN1544	4	UCT	256/4k	6/4	124		4M	2.0u		16	See Device Number Sec 3		S173	MATJ
40#	MN1562	4	UCT	152/2k	12/4	124		4M	2.0u		16	See Device Number Sec 3		S172	MATJ
41#	MN1564	4	UCT	256/4k	12/4	124		4M	2.0u		16	See Device Number Sec 3		S173	MATJ
42#	MN1599	4	UCT	256/	6/4	124		5M	2.0u		16	See Device Number Sec 3		S174	MATJ
43#	PCA0401	4	CoC	128/2k	3/			1	15u			Sys Evaluation uCT		S178	MITJ
44	5701	4	uCT	512	16/4	36			230n	16		4 Bit Slice Controller	IS18		MMI
45	6701	4	uCT	512	16/4	36			175n	16		4 Bit Slice Controller	IS18		MMI
46	M2900	4	ChF	512/8.0k	16/4	512△	4	VP	150n	16	4	Microprogrammable	IS63	S66	MOTA
47	M10800	4	ChF	256	256/4	16		MP		4		Full Binary And BCD	IS61	S44	MOTA
48	MC141000	4	uCT	256/8k▼	19/1	43			1.4u§			One Chip Microcomputer	IS90	S122	MOTA
49	MC141200	4	uCT	256/8k▼	24/1	43			1.4u§			One Chip Microcomputer	IS90	S122a	MOTA
50#	uCOM-4	4	ChF	16k/64k▼	120/8	55			7.5u		4	Uses NEC uPD751D CPU	IS60		NECJ
51#	uCOM-41	4	ChF	128/2k	16/4	69		8	6.4u*	2	8	Uses NEC uPD541D CPU	IS59		NECJ
52#	uCOM-42	4	uCT	384/19k▼	31/1	72			10u		4	uPD548C Chip Sys	IS80	S109	NECJ
53#	uCOM-43C	4	uCT	384/16k▼	35/1	80		1V	10u	6	3	uPD546C Chip Sys	IS81	S110	NECJ
54#	uCOM-44C	4	uCT		35/1	80			10u		1	uPD547 Chip Sys	IS81a	S111	NECJ
55#	uCOM-45C	4	uCT	128/5k	21/1	58			10u		1	uPD550C;554C Chip Sys	IS81	S112	NECJ
56#	uCOM-47	4	uCT	32/4k	4/4	103			5.0u		M	uPD766G Chip Sys	IS86	S117	NECJ
57	COP402	4	uCT	128/0	23/1	57	3	2VP	4.0u	1	3	COP420 Without ROM			NSC
58	COP410L	4	uCT	128/4k▼	19/1	43	3	1VP	16u	1	2	5mA,4.5-9.5V Supply			NSC
59	COP411L	4	uCT	128/4k▼	15/1	43	3	1VP	16u	1	2	COP410L In 20 Pin Pkg			NSC
60	COP420	4	uCT	256/8k▼	23/1	57	3	2VP	4.0u	1	3	COP400 Family Software			NSC
61	COP420L	4	uCT	256/8k▼	23/1	57	3	2VP	16u	1	3	7mA,4-9V Supply			NSC
62	IDM2900	4	ChF	16/16	16/4	512△			75n*	16		Microprogrammable	IS63	S130	NSC
63	MM5781/82	4	ChF	512/16k▼	24/1	52	3	2VP	10u*	2	2	Expandable ROM	IS92a		NSC
64	MM5782/129	4	ChF	512/32k▼	24/1	52	3	2V	10u*	2	2	Direct VF/LED Display			NSC
65	MM5799N	4	uCT	384/12k▼	22/1	51	3	1VP	10u*	2	2	LED Drive,Serial I/O	IS92	S124	NSC
66	MM57140N	4	uCT	220/5k▼	24/1	39	3	1VP	15u*	1	2	Direct LED Display Drive	IS91	S123	NSC
67	MM57152N	4	uCT	240/6k▼	24/1	39	3	1VP	15u*	1	2	Direct VF Display Drive	IS91	S123	NSC
68	MM75	4	uCT	48/640	22/1	50				4		PPS 4/1 One Chip Comp	IS100		RKW
69	MM78	4	uCT	128/2.0k	31/1	50				6		PPS 4/1 One Chip Comp	IS101		RKW
70	PPS4/1	4	uCT	4k/4k	31/4	50		2	12.5u	1		Decimal And Binary	IS26	S17	RKW
71	3000SIC	4	ChF	512	16/4	512△	5			11		MCU And CPE	IS13	S4	SIC
72	LS481	4	ChF		2/8	210△		M	100n§		M	Expand,Microprog Slice	IS85	S115	TII
73	S481	4	ChF		2/8	210△		M	60n§		M	Expand,Microprog Slice	IS85	S115	TII
74	SBP0400	4	ChF	512	16/4	76	6		1.0u§	8		Expandable,Microprogram	IS47	S45	TII
75	SBP0400A	4	ChF	512	16/4	76	6		200n§	8		Expandable,Microprogram	IS47	S45	TII
76	TMS1000	4	uCT	256/8.0k▼	23/1	43			15u		1	One Chip Microcomputer	IS7		TII
77	TMS1070	4	uCT	256/8.0k▼	23/1	43			15u		1	One Chip Microcomputer	IS7		TII
78	TMS1100	4	uCT	512/16k▼	23/1	54			15u		1	One Chip Microcomputer	IS8		TII
79	TMS1200	4	uCT	512/16k▼	25/1	43			15u		1	One Chip Microcomputer	IS7		TII
80	TMS1270	4	uCT	256/8.0k▼	27/1	43			15u		1	One Chip Microcomputer	IS7		TII
81	TMS1300	4	uCT	512/16k▼	28/1	54			15u		1	One Chip Microcomputer	IS8		TII
82▼#	TCP4600AC	4	ChF	160/4k▼		52			10u			Evaluator w/External ROM			TOSJ
83▼#	TCP4620AP	4	ChF	96/2k▼		52			10u			34-Bit I/O Ports			TOSJ
84▼#	TCP4630AP	4	ChF	160/3k▼		52			10u			34-Bit I/O Ports			TOSJ
85▼#	TMP4300C	4	ChF	128/2k▼		35			4.0u			Evaluator w/External ROM			TOSJ
86▼#	TMP4310AP	4	ChF	48/1.0k▼		35			4.0u			4 Index/31 Process Instr			TOSJ
87▼#	TMP4310APL	4	ChF	48/1.0k▼		35			4.0u			4 Index/31 Process Instr			TOSJ
88▼#	TMP4315BP	4	ChF	64/1.5k▼		35			4.0u			4 Index/31 Process Instr			TOSJ
89▼#	TMP4320AP	4	ChF	128/2k▼		35			4.0u			4 Index/31 Process Instr			TOSJ
90	CR1872	4	uCT	128/512▼	16/4	20		2Po	10u	5		One Chip Microcontroller	IS89	S53	WDC
91	WD4200	4	uCT	256/8k▼	23/1	49		V	4.0u		3	Internal Counter	IS118	*	WDC
92	AMC95/4000	8	CoC	4k/12k	48/1	74		8V	250n§	7		Uses Am9080A,A-4 CPU	IS57		AuC
93▼	Am95/4006/20	8	MOD	4k/16k				8VP		6	16	48 Prog I/O Lines			AMD
94▼	Am95/4006/21	8	MOD	4k/16k				8VP		6	16				AMD
95▼	Am95/4006/22	8	MOD	4k/16k				8VP		6	16	48 Prog I/O Lines			AMD
96▼	Am95/4006/40	8	MOD	4k/16k				8VP		6	16	48 Prog I/O Lines			AMD
97▼	Am95/4006/41	8	MOD	4k/16k				8VP		6	16	48 Prog I/O Lines			AMD
98▼	Am95/4006/42	8	MOD	4k/16k				8VP		6	16	48 Prog I/O Lines			AMD
99▼	Am95/4010	8	MOD	3k/4k	3/8			8VS		6	16	5-16Bit,Prog Count Timer			AMD
100	S2152	8	uCT	320/12k▼	1/8	51			4.5u		3	IS Compatible w/S2000	IS113	*	AMI
101	S2210	8	uCT	256/8k▼	1/8				4.5u		3	Hi-Volt Display Dr Avail	IS113	*	AMI
102	S6800	8	ChF	65k	64k/8☑	72	7	V	2.0u	6	M	DMA and Mult Processor	IS11	S1	AMI
103▼	S6805	8	uCT	64/1.0k	20/8	59	10	2V	1.0u§	8		8 Lines LED Compatible	IS11	*	AMI
104	Am9080A	8	ChF	64k	256/8	74		V	250n§*	7		DMA,TTL Compatible	IS57		AMV
105	70-100	8	CoC	4k/1k	256/8	78	4	8P	2.0u			Expan Options,Intel 8080	IS57		APP
106	EVENT2000	8	CdF	48k		78	4	8P	2.0-8.5u	7	M	Uses 8080A CPU	IS57		APP
107	ASC80	8	CdF	64k	128/8	78	4	8V	2.0u	6		Uses Intel 8080A MPU	IS57		APS
108	ASCZ80	8	CdF	64k	128/8	158	10	NPV	1.6u	12		Uses Zilog Z80 CPU	IS65		APS
109	AMC95/4005/2	8	CoC	4k/16k	48/1	74		8.0	2.0u	7		Monoboard Computer			AUC
110	AMC95/4005/3	8	CoC	4k/16k	48/1	74		8.0	1.3u	7		Monoboard Computer			AUC

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

2. MICROCOMPUTER SYSTEMS

IN ORDER OF: (1)DATA BITS (2)MANUFACT. CODE & (3)SYSTEM TYPE No.

LINE No.	3 SYSTEM TYPE No.	ORGANIZ-ATION 1 DATA BITS	ARCHI-TECT-URE	SYS. CONFIGURATION ADDRESSABLE MEMORY (RAM/ROM) (BYTES)	I/O DEV @PT WIDTH (D/WDTH)	No. BASIC MICRO INSTR	No. ADDR MODE	INTERR-UPT LEVEL No. & TYPE	INSTRUCT TIME-TYP §CLK CYC *-MIN (s)	No. GEN PUR-POSE REG	STACK LEVEL	SYMBOL: PT-PORT V-VECTORED P-PRIORITY M-MULTIPLE OTHER CAPABILITIES	INSTR SET REF. No.	SYSTEM DWG.	2 MFR. CODE
1	CSB1	8	CoC	8/8	60/1	55	13	3V	3.0u	3	M	2 PIA,1VIA	IS83		CAC
2	CSB2	8	CoC	8/8	40/1	55	13	3V	3.0u	3	M	PIA,VIA,6551	IS83		CAC
3	CSS-1143	8	CoC	1.0k/16k		158	7	M	500n§	12	M	Uses Z80 CPU	IS65	S144	CLI
4	MM1	8	CdF	64k	8/8	78	4	8VP	500n§	6	16	Uses Intel 8080A	IS29	S90	CLI
5	MSERIES	8	CdF	64k	512/8	78		P	5.5-7.0u	6		Intel 8080 3 Card Set	IS29	S21	CLI
6	CS2/2	8	SYS	128kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 5in Fl;2 TS	IS65		CRO
7	CS2/3	8	SYS	192kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 5in Fl;3 TS	IS65		CRO
8	CS2/4	8	SYS	192kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;S 5in Fl;4 TS	IS65		CRO
9	CS2/5	8	SYS	256kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;S 5in Fl;5 TS	IS65		CRO
10	CS2/6	8	SYS	256kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 5in Fl;6 TS	IS65		CRO
11	CS3/2	8	SYS	128kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 8in Fl;2TS	IS65		CRO
12	CS3/2-002	8	SYS	128kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;4 8in Fl;2TS	IS65		CRO
13	CS3/3	8	SYS	192kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 8in Fl;3TS	IS65		CRO
14	CS3/3-002	8	SYS	192kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;4 8in Fl;3TS	IS65		CRO
15	CS3/4	8	SYS	192kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 8in Fl;4TS	IS65		CRO
16	CS3/4-002	8	SYS	192kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;4 8in Fl;4TS	IS65		CRO
17	CS3/5	8	SYS	256kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 8in Fl;5TS	IS65		CRO
18	CS3/5-002	8	SYS	256kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;4 8in Fl;5TS	IS65		CRO
19	CS3/6	8	SYS	256kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 8in Fl;6TS	IS65		CRO
20	CS3/6-002	8	SYS	256kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;4 8in Fl;6TS	IS65		CRO
21	CS3/7	8	SYS	320kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 8in Fl;7TS	IS65		CRO
22	CS3/7-002	8	SYS	320kØ	128/8	158	10	NVP	1.0u*	12	M	Z80A;4 8in Fl;7TS	IS65		CRO
23	CS-2	8	SYS	64k	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 5in Fl;SU	IS65		CRO
24	CS-3	8	SYS	32k	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 8in Fl;SUU	IS65		CRO
25	CS-3-001	8	SYS	32k	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 8in Fl;SUU	IS65		CRO
26	CS-3-001-002	8	SYS	32k	128/8	158	10	NVP	1.0u*	12	M	Z80A;4 8in Fl;SU	IS65		CRO
27	CS-3-002	8	SYS	32k	128/8	158	10	NVP	1.0u*	12	M	Z80A;4 8in Fl;SU	IS65		CRO
28	CS-3-004	8	SYS	64k	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 8in Fl;SUU	IS65		CRO
29	CS-3-004-002	8	SYS	64k	128/8	158	10	NVP	1.0u*	12	M	Z80A;4 8in Fl;SU	IS65		CRO
30	Z2-H	8	SYS	64k	128/8	158	10	NVP	1.0u*	12	M	Z80A;2 5in Fl;11MBHD	IS65		CRO
31	MPS	8	CdF	16k	32/8	48		1M	12u-44u	6	7	Custom System	IS16	S10	DEC
32	TDG6500SYS	8	CdF	64k	512/8	55		1V	1.0u§			Uses 6502CPU;Options	IS83		DIG
33	TDG6800SYS	8	CdF	64k	512/8	72		1V	1.0u§	6		Uses 6800CPU;Options	IS6		DIG
34	TDG8080SYS	8	CdF	64k	512/8	78		8VP	500n§	7		Uses 8080CPU;Options	IS57		DIG
35	TDGZ80SYS1	8	SYS	10k	8/8	78	11	128V	1.0u	16		Packaged Z80 CPU Sys	IS65	S98	DIG
36	TDGZ80SYS2	8	SYS	18k	8/8	78	11	128V	1.0u	16		Z80SYS1 W/Added Mem Bd	IS65	S98	DIG
37	CONCEPT80	8	CdF	64k	64/1	78	4	8PrV	2.0-9.0u	6	M	Uses 8080CPU	IS57		DSI
38	SYSTEM8	8	CdF	64k	240/8	72	4	8V	500n§	8		Uses M80 CPU MOD	IS57		DSI
39	SYSTEM8A	8	CdF	64k	240/8	134	4	7V	250§	8		Uses M8A CPU MOD	IS5		DSI
40	DB8/1	8	SYS	32k/4k	3/8	158	10	NPV		12	M	Uses Z80 CPU	IS65		DYB
41	DMS	8	SYS	64k	64k/8Ø	72	7	MPV	1.0u§	6	M	Uses Motorola 6800 CPU	IS6		DYN
42	INNOVATOR	8	CoC	64k/512	256/8	158	10	2M	1.0u	16	M	Z80A Based Bd,NOVA Host			EDSI
43▼#	EF6805P2C	8	uCT	64/1.1k	20/4	59	10	3SV	1.0u§	8	M	On-Chip Clock	IS114a	S174a	EFCF
44▼#	EF6805P2J	8	uCT	64/1.1k	20/4	59	10	3SV	1.0u§	8	M	On-Chip Clock	IS114a	S174a	EFCF
45▼#	EF6805P2P	8	uCT	64/1.1k	20/4	59	10	3SV	1.0u§	8	M	On-Chip Clock	IS114a	S174a	EFCF
46	ETC1000	8	SYS	64k/8	256/8	55	13	8PV	5.0u		M	Uses 6502 CPU	IS83	S121	ETL
47#	E-6	8	CdF	64k	64k/8Ø	72	7	V	1.0u§	6	M	Uses MOTA 6800 CPU Small	IS6		EURF
48#	EURO-6	8	CdF	64k	64k/8Ø	72	7	V	1.0u§	6	M	Uses MOTA 6800 CPU Large	IS6		EURF
49#	EUROTERM-6	8	Coc	64k	64k/8Ø	72	7	V	1.0m§	6	M	Uses MOTA 6800 CPU	IS6		EURF
50#	SYNTE-2	8	CdF	256/4k								Uses MOTA 6800 CPU			EURF
51	MS6800	8	SYS	64k	256/8	72	7	2PV	1.0u	6	M	Complete 6800 Sys W/CRT			FCC
52	MS8080	8	SYS	64k	256/8	78	4	8PV	5.0u	7	M	Complete 8080 Sys W/CRT			FCC
53	MSZ80	8	SYS	64k	256/8	158	10	NPV	250n	12	M	Complete Z80 Sys W/CRT			FCC
54	F8	8	ChF	64k	256/8	76	8	1P	2.0u	64		DMA, Built In Clock	IS20	S15	FSC
55	F68A00	8	ChF	65k/	65k/8Ø	72	7		667 n	6		F6800 uC Family	IS6	S84	FSC
56	F68B00	8	ChF	65k/	65k/8Ø	72	7		500 n	6		F6800 uC Family	IS6	S84	FSC
57	F3870	8	uCT	64/2.0k	8/8	76	8	1PV	250n§	64		Uses F8 Sys Software	IS20	S108	FSC
58	F6800	8	ChF	65k	65k/8Ø	72	7			6		DMA,16 Bit Address Bus	IS6	S84	FSC
59	F6808	8	ChF			72	7	N		6		MPU W/Clock	1S71		FSC
60	FORMULATORMKI	8	CdF	1.0k	16/8	70	8	3VP	2.0u	64	M	Dev Sys For F8:DMA,Clock			FSC
61	FORMULATORMKII	8	CdF	17k	16/8	70	8	3VP	2.0u	64	M	Dev Sys For F8:DMA,Clock			FSC
62	FORMULATORMKIII	8	CdF	17k	24/8	70	8	3VP	2.0u	64	M	Dev Sys For F8:DMA,Clock			FSC
63	MICROPRO	8	CoC	1.0k	24/8	70	8	2VP	2.0u	64	M	Uses 3850 CPU		S52	FSC
64	OCM-1	8	CoC	1k/4k	128/1	76	8	1PV	2.0u	64		Based On F8	IS20		FSC
65	GIC8000	8	CdF	16k	15/8	48				48		Break Point Facility	IS43	S71	GIC
66	PIC1650	8	uCT	192/6k▼	4/8	31	2		4.0u	1	2	Bit Manipulation;LED Dr	IS74	S114	GIC
67	PIC1654	8	uCT	192/6k▼	20/1	31	2		4.0u	1	2	Bit Manipulation;LED Dr	IS74	S127	GIC
68	PIC1655	8	uCT	192/6k▼	20/1	31	2		4.0u	1	2	Bit Manipulation;LED Dr	IS74	S114a	GIC
69	PIC1670	8	uCT	184/12k▼	4/8	31	2		4.0u	1	4	Bit Manipulation;LED Dr	IS74	S114b	GIC
70#	LP8000	8	ChF	16k	32/16	48				48		Automatic Sub Nesting	IS43	S37	GICB
71	HCMP1802	8	ChF	64k	256/8	91	3	1PV	5.0u	16	M	DMA,Clock,Sep I/O	IS38	S42	HAC
72	H8	8	SYS	64/1k	256/8	78	4	7V	4.9u			Uses 8080A			HEA
73	ADAM12	8	CoC	1k/8k	57k/2	158		128V	340n			Tri-State Lodgic	IS-122		HEU
74	ADAM100	8	CoC	1k/8k	57k/2	158		128V	340n			Acquisition Control	IS-122		HEU
75	MLP8080	8	CoC	64k	64k/8Ø	78	4	8P	2.0u	7		Uses Intel 8080CPU	IS57	S20	HEU
76	MLZ80	8	CoC	64k	512/8	158	10	NPV	4.0u	12		On Card Floppy Disk I/F	IS65	S153	HEU
77▼#	HD6801DC	8	uCT	128/2k	31/4	82	7	S	1.0u§	3		On-Chip Ser. Comm. Inter	IS6a		HITJ
78▼#	HD6801DP	8	uCT	128/2k	31/4	82	7	S	1.0u§	3		On-Chip Ser. Comm. Inter	IS6a		HITJ
79#	HMCS6800	8	ChF	64k	64k/8Ø	125	7	V		6	M	DMA and Multi Processor	IS6	S92	HITJ
80	MX800	8	CdF	64k	64k/8Ø	78	4		2.0u	6		Uses Intel 8080A CPU	IS57	S22	ICC
81	I-8080	8	SYS	64k	256/8	72	4	8P	2.0u	6	M	Uses 8080A CPU	IS57		IMS
82	PCS-40	8	SYS	64k/2k		74	2	4P	500n§			Disk Storage 180k Bytes	IS57a		IMS
83	PCS-42	8	SYS	64k/2k		74	2	4P	500n§			Disk Storage 400k Bytes	IS57a		IMS
84	PCS-44	8	SYS	64k/2k		74	2	4P	500n§			Disk Storage 780k Bytes	IS57a		IMS
85	VDP-40	8	SYS	64k/2k		74	2	4P	500n§			Disk Storage 180k Bytes	IS57a		IMS
86	VDP-42	8	SYS	64k/2k		74	2	4P	500n§			Disk Storage 400k Bytes	IS57a		IMS
87	VDP-44	8	SYS	64k/2k		74	2	4P	500n§			Disk Storage 780k Bytes	IS57a		IMS
88	VDP-80	8	SYS	196k	256/8	113	4	5P	560n§	6	M	Uses 8085 CPU	IS57a		IMS
89	8021	8	uCT	64/1k	21/1	64	5		10-50u§	8	8	8748 Inst Sub Set	IS97	S133	ITL
90	8022	8	uCT	64/2k	28/1	74	5	2	10u	8	8	8048 Inst Sub Set	IS112	S158	ITL
91	8035	8	uCT	64/0	27/1	96	5	1	2.5-5.0u	8	8	2 Bks of 8x8 Work Reg	IS62	S133b	ITL
92	8039	8	uCT	128/0	27/1	96	5	1	2.5-5.0u	8	8	External ROM or EPROM	IS62	S134c	ITL
93	8048	8	uCT	64/1k	27/1	96	5	1	2.5-5.0u	8	8	2 Bks of 8x8 Work Reg	IS62	S133	ITL
94	8049	8	uCT	128/2k	27/1	96	5	1	2.5-5.0u	8	8	Mask ROM	IS62	S134b	ITL
95	8748	8	uCT	64/1k	27/1	96	5	1	2.5-5.0u	8	8	2 Bks of 8x8 Work Reg	IS62	S133a	ITL
96	MCS8	8	ChF	32k	512/8	48	4	M	2.0u	6		7 Subroutine Nesting	IS64	S41	ITL
97	MCS48	8	ChF	320/4k	256/8	96	3		2.5u	16	8	Expanded 1 Chip Sys	IS62	S65	ITL
98	MCS80	8	ChF	64k	512/8	78	4	M	2.0-9.0u	6	M	External Interrupts	IS57	S12	ITL
99	MCS85	8	ChF	64k	256/8	80	4	12V	1.3u	6	16	8080 Compatible	IS57a	S64	ITL
100	SBC80/05	8	CoC	512/4k	22/1	80	4	4V	2.03u	6	M	Uses 8085 CPU	IS57a	S100	ITL
101	SBC80/10	8	CoC	1k/4k	48/1	78	4	1V	1.95u	6	M	Uses 8080A CPU	IS57	S101	ITL
102	SBC80/20	8	CoC	2k/8k	48/1	78	4	8V	1.86u*	6	M	Uses 8080A CPU	IS57	S102	ITL
103	SBC80/20-4	8	CoC	4k/8k	48/1	78	4	8V	1.86u*	6	M	Uses 8080A CPU	IS57	S102	ITL
104	SDK85	8	CoC	256/4k	38/1	80	4	3V	1.3u	6	M	Uses 8085 CPU	IS57a	S105	ITL
105	SYSTEM80/20	8	SYS	2k/4k	48/1	78	4	8V	1.86u*	6	M	Uses SBC80/20 Card	IS57	S103	ITL
106	SYSTEM80/20-4	8	SYS	4k/8k	48/1	78	4	8V	1.86u*	6	M	Uses SBC80/20-4 Card	IS57	S104	ITL
107	UPI41	8	uCT	64/1k	2/8	90		1V	2.5u§	1	8	Peripheral Controller	IS75	S97	ITL
108	MSC8004-Z80A	8	CoC			78	4	8PN	2.0-9.0u	6	M	Uses 8080 CPU	IS57		MCSS
109	MSC8007-Z80A	8	CoC			78	4	8PN	2.0-9.0u	6	M	Uses 8080 CPU	IS57		MCSS
110	MICRO1	8	CdF	64k	32/8	107	8	P	220n	15		DMA,CPU And ROM	IS32		MID

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

2. MICROCOMPUTER SYSTEMS

IN ORDER OF: (1)DATA BITS (2)MANUFACT. CODE & (3)SYSTEM TYPE No.

LINE No.	3 SYSTEM TYPE No.	ORGANIZ -ATION 1 DATA BITS	ARCHI -TECT -URE	SYS. CONFIGURATION ADDRESSABLE MEMORY (RAM/ROM) (BYTES)	I/O DEV @PT WIDTH (D/WDTH)	No. BASIC MICRO INSTR	No. ADDR MODE	INTERR -UPT LEVEL No. & TYPE	INSTRUCT TIME-TYP §CLK CYC *-MIN (s)	No. GEN PUR- POSE REG	STACK LEVEL	SYMBOL: PT-PORT V-VECTORED P-PRIORITY M-MULTIPLE OTHER CAPABILITIES	INSTR SET REF. No.	SYSTEM DWG.	2 MFR. CODE
1#	MELCS8/2	8	CdF	64k	512/8	78	4	M	2.0u	6	M	Uses M58710S CPU	IS57		MITJ
2#	MELPS8	8	ChF	64k	512/8	78	4	M	2.0u	6	M	Uses M58710S CPU	IS57		MITJ
3#	PCA0801	8	CoC	256/2k	4/8	78	4	M	2.0u	6	M	Uses M58710S CPU	IS57		MITJ
4#	PCA0804G01	8	CoC	1k/2k	3/8				2.3u			Color TV Display uCT		S175	MITJ
5#	PCA0804G02	8	CoC	1k/2k	3/8				2.3u			Color TV Display uCT		S176	MITJ
6#	PCA8501G01	8	CoC	1k/4k	6/8			5P	1.6u			Gen Purpose 1-Bd uCT		S177	MITJ
7#	PCA8501G02	8	CoC	1k/4k	6/8			5P	1.6u			Gen Purpose 1-Bd uCT		S177	MITJ
8	AID-80F	8	SYS	64k	256/8	158	10	NVP	1.6u	12	M	Z80 Floppy Disk Dev Sys	IS65		MOS
9	EMU-70	8	SYS	64/2k	4/8	76	8	MPV	2.0u	64	M	MK3870 Emulator	IS20		MOS
10	F8-MOS	8	ChF	64k	256/8	76	8	MPV	2.0u	64	M	Blt-in Clk;I/O Intensive	IS20	S15	MOS
11	MD-SBC1	8	CoC	2k/8k	5/8	78	10	MPV	1.6u	18	M	Uses Z80 CPU	IS65	S156	MOS
12	MK3873	8	uCT	64/2k	4/8	70	4	VS	2.0u	64	M	F8 Software Compatible	IS20	S173	MOS
13	MK3874	8	uCT	64/2k	4/8	70	4	VS	2.0u	64	M	F8 Software Compatible	IS20	S73a	MOS
14	MK97400	8	uCT	64/2K	4/8	70	4	VS	2.0u	64	M	F8 Software Compatible	IS20	S73a	MOS
15	MK97401	8	uCT	64/2K	4/8	70	4	VS	2.0u	64	M	F8 Software Compatible	IS20	S73a	MOS
16	MK97402	8	uCT	64/2K	4/8	70	4	VS	2.0u	64	M	F8 Software Compatible	IS20	S73a	MOS
17	MK97403	8	uCT	64/2K	4/8	70	4	VS	2.0u	64	M	F8 Software Compatible	IS20	S73a	MOS
18	MK97404	8	uCT	64/2K	4/8	70	4	VS	2.0u	64	M	F8 Software Compatible	IS20	S73a	MOS
19	MK97405	8	uCT	64/2k	4/8	70	4	VS	2.0u	64	M	F8 Software Compatible	IS20	S73a	MOS
20	MKB3870P10	8	uCT	64/2k	4/8	76	8	MPV	2.0u	64	M	F8 Software Compatible	IS20	S73	MOS
21	OEM-80	8	SYS	64k	256/8	158	10	NVP	1.6u	12	M	Z80 OEM Computer	IS65		MOS
22	SDB-80	8	SYS	64k	256/8	158	10	NVP	1.6u	12	M	Low Cost Z80 Dev Sys	IS65		MOS
23	M68MM01	8	CoC	1k/8k	64k/8☑	72	7	V	2.0u*	6	M	MC6800 MPU	IS6	S87	MOTA
24	M68MM01A	8	CoC	1k/8k	64k/8☑	72	7	V	2.0u*	6	M	MC6800 MPU	IS6	S91	MOTA
25	M6800	8	ChF	64k	64k/8☑	72	7	V	2.0u*	6	M	DMA and Multi Processor	IS6	S7	MOTA
26	MC3870	8	uCT	64/2k	8/8	76	8		250n§	64	M	F8 Software Compatible	IS20	S73	MOTA
27	MC6801	8	uCT	65k	31/1	82	7	8				On Chip SCI	IS6a	S154	MOTA
28	MC6803	8	uCT	128	13/1	82	7					One Chip Microcomputer	IS6a	S137	MOTA
29	MC6805	8	uCT	64/1.1k	8/2,4/1	61	6	V		5		One Chip Microcomputer	IS114	*	MOTA
30▼	MC6805R2L	8	CHF	64/2K	4/32	59	10	4V				Memory Mapped I/O	IS114		MOTA
31▼	MC6805R2P	8	CHF	64/2K	4/32	59	10	4V				Memory Mapped I/O	IS114		MOTA
32▼	MC6805R2S	8	CHF	64/2K	4/32	59	10	4V				Memory Mapped I/O	IS114		MOTA
33▼	MC6805U2L	8	CHF	64/2K	4/32	59	10	4V				Memory Mapped I/O	IS114		MOTA
34▼	MC6805U2P	8	CHF	64/2K	4/32	59	10	4V				Memory Mapped I/O	IS114		MOTA
35▼	MC6805U2S	8	CHF	64/2K	4/32	59	10	4V				Memory Mapped I/O	IS114		MOTA
36	MC141099	8	uCT	256/8k▼	21/1	43			1.4u§			One Chip Microcomputer	IS90	S122b	MOTA
37	MSC8001-Z80	8	CoC	64k	512/8	158	10	NVP	400n§	12	M	Uses Z80 CPU,3 Intr Mode	IS65	S96	MSCC
38	MCS6500	8	ChF	64k	64k/8☑	55	13		6.0u△			Arith;Dec,Bin;DMA	IS83	S6	MTY
39	808AMULT	8	SYS	2.0M	16k/8☑	72	4	M	2.0-9.0u	7	M	Up To 32 808As Parallel	IS57	S51	MUL
40	MS801	8	SYS	64k	512/8	48		8		7		Uses Intel 8008MPU	IS64		MUL
41	MS808A	8	SYS	64k	512/8	78	4	M	2.0-9.0u	7	M	Uses Intel 8080A MPU	IS57		MUL
42	muPRO80	8	SYS	64k	256/8	78	4	8Pr	500n§	6		Uses 8080A CPU	IS57		MUP
43#	NASCOMI	8	CoC	64k	256/8	158	10	NVP	2.0u	12	M	Uses Z80 CPU	IS65	S140	NASB
44#	TK80	8	CoC	512/768	24/8	78	4	M		7		Training Kit,upd8080A	IS55	S82	NECD
45#	uCOM-80F	8	ChF	64k	512/8	78	4	M	1.28u*	7		Uses uPD8080AFC/D	IS57b		NECJ
46#	uPD8035LC	8	uCT	64/1k	27/1	96	3	1	2.5u*		8	Req Ext Program	IS120		NECJ
47	uPD8048C	8	uCT	64/1k	27/1	96	3	1	2.5u*		8	Stand Alone Computer	IS120	*	NECJ
48	TK-80A	8	CoC	1k/1k	24/1	78			2.0-9.0u			W/Programmable I/O		S165	NECM
49	uCOM-8	8	ChF	64k	512/8	78	4	M		7		Uses NEC uPD8080AD CPU	IS55		NECM
50	uPD780	8	ChF	65k	512/8	158	10	MPV		12	M	Uses uPD780C CPU	IS65		NECM
51	uPD8748D	8	uCT	64/1k	27/1	90	3	1	2.5u*		8	Includes 1k EPROM	IS120	*	NECM
52	NMS85/P	8	SYS	64k	256/8	80	4	12V	1.3u	6	M	Uses 8085A/A2 CPU	IS57a		NMS
53	BLC80/10	8	CoC	1k/4k	48/8	78	4	6	1.9u*	6		Uses N8080A	IS57	S83	NSC
54	N8080A	8	ChF	65k	512/16	78	4	V	2.0u§	6		DMA,Var Stack Length	IS57	S60	NSC
55	SC/MP	8	ChF	64k	64k/8☑	46	4	1V	5.0-23u			Simple/Cost Effective uP	IS70	S132	NSC
56	EQUINOX-100	8	SYS	64k	256/8	78	4	8V		6	M	Uses 8080A CPU	IS57		PAR
57	MICROPAC80A	8	SYS	64k	256/16	78	4	M,V	2.0u	6		Uses Intel 8080 MPU	IS57		PCS
58	PCS1806	8	CoC	64k	256/8☑	78	4	8VP	2.0-9.0u	7	M	Uses 8080A CPU	IS57	S67	PCS
59	PCS1810	8	CoC	64k	256/8☑	78	4	8VP	2.0-9.0u	7	M	Uses 8080A CPU,Batt Back	IS57	S68	PCS
60	PCS1810A	8	CoC	64k	256/8☑	78	4	8VP	2.0-9.0u	7	M	Uses 8080A CPU,1k RAM	IS57		PCS
61	PCS1880	8	CoC	64k	256/8	158	10	5PV		12		Uses Z80A CPU	IS65	S139	PCS
62	SUPERPAC180	8	CdF	64k	256/8☑	78	4	8VP	2.0-9.0u	7	M	Uses 8080A CPU	IS57		PCS
63	PLS-858	8	CoC	2k/8k	64/8	80	4	4V	320n§	6		8085/2716 One Card Sys	IS76		PRO
64	PLS-868	8	CoC	2k/8k	64/8	78	7	1V	1.0u§		M	6800/2716 One Card Sys	IS11	S169	PRO
65	PLS-881	8	CoC	1k/4k	5/8	78	4	1V	488n§	7	M	One 4x6 Card 8080/2708	IS67	S76	PRO
66	PLS-888	8	CoC	2k/8k	64/8	78	4	1P	488n§	7	M	8080/2716 One Card Sys	IS67	S170	PRO
67	PLS-898	8	CoC	2k/8k	64/8	158	10	2P	400n§	12		Z80/2716 One Card Sys	IS65	S156a	PRO
68	SOL20/16	8	SYS	16k	64/8	78	4	8VP	2.0-9.0u	6	M	Uses 8080A CPU	IS57		PRT
69	SOL20/32	8	SYS	32k	64/8	78	4	8VP	2.0-9.0u	6	M	Uses 8080A CPU	IS57		PRT
70	SOLPC	8	CoC	2k/2k	64/8	78	4	8VP	2.0-9.0u	6	M	Uses 8080A CPU	IS57		PRT
71	SOLSIA	8	SYS	16k	64/8	78	4	8VP	2.0-9.0u	6	M	Uses 8080A CPU	IS57		PRT
72	SOLSIIA	8	SYS	32k	64/8	78	4	8VP	2.0-9.0u	6	M	Uses 8080A CPU	IS57		PRT
73	SOLSIIIA	8	SYS	64K	64/8	78	4	8VP	2.0-9.0u	6	M	Uses 8080CPU	IS57		PRT
74	SOLSIVA	8	SYS	64K	64/8	78	4	8VP	2.0-9.0u	6	M	Uses 8080CPU	IS57		PRT
75	QUAY80MCB	8	CoC	1K/8K	256	158	4	128V	1.0u	12	M	S100Comp;Ser,Par Ports	IS65		QUY
76	QUAY90F/MPS	8	CoC	65K/14K	256	158	4	128V	1.0u	12	M	Floppy Disk Contr;DMA	IS65		QUY
77	QUAY90MPS	8	CoC	64k/7k	256/8	158	4	128V	1.0u	12	M	Uses Z80 CPU	IS65		QUY
78	QUAY8000	8	SYS	64k/7k	256/8	158	10	128V	1.0u	12	M	Uses Z80 CPU	IS65		QUY
79	CDP1800	8	ChF	64k	256/8	91		1PV	5.0u	16		DMA;Split P.S. Option	IS38	S42	RCA
80	CMC68/15	8	CoC	64k	4/8	72	7	8V	1.0u§	6	M	Uses 6800 CPU	IS6	S141	RCI
81	CMC68/15B	8	CoC	64k	4/8	72	7	8V	1.0u§	6	M	Uses 6800CPU	IS6	S141	RCI
82	CMC68/15C	8	CoC	64k	2/8	72	7	8V	1.0u§	6	M	6800 CPU,Two 2651 PCI	IS6		RCI
83	CMC68/15G	8	CoC	64k	4/8	72	7	8V	1.0u§	6	M	For GIPB Syst or Environ	IS6	S141	RCI
84	AIM65	8	CoC	65k	28/1	56	13	3V	1.0u*	3	M	6502CPU,On Bd Printer	IS83	S135	RKW
85	R6500	8	ChF	64k	64k☑	56	13	M	1.0u§		M	MOS Tech MCS6500 Sys	IS83	S113	RKW
86	R6500/1	8	uCT	512/16k	32/1	56	13	5V	1.0u*	3	M	Uses 6502 CPU	IS83	S136	RKW
87#	MICRAL-M	8	SYS	512k	2816/8	74	4	64	2.0u	7	M	64 Buffered Channels			R2E
88#	MICRAL-S	8	SYS	64k	352/8	74	4	8	2.0u	7	M	8 Buffered Channels			R2E
89	SIA-2350	8	SYS	32k/16k	4/8	158	4		1.0u	12	M	Complete Disk Management			SIA
90	SIA-3500	8	SYS	80k/24k	4/8	158	4		1.0u	12	M	Uses Z80 CPU		S158	SIA
91	2650	8	ChF	32k	256/8	75	8	V		7	8	Separate Adder	IS12	S3	SIC
92	MP8080AI	8	ChF	65k	256/8	78	4	8PV	2.0u	6	M	External DMA	IS57	S128	SIC
93	N8X300	8	ChF	8k		21			250n	8		Fixed Instruction uComp	IS78	S107	SIC
94#	SKC85	8	CoC	512/4k*	22/8	80	4			6	M	Uses 8085A CPU		S163	SIEG
95#	SMP80	8	CdF	64k	6/8	78	4	M		6	M	Uses 8080A CPU		S164	SIEG
96	SSM-85/1	8	CoC	1280/2k	2/8,1/6	80	4	5P	1.3u§	6		Uses 8085 CPU	IS57a	S161	SSC
97	SSM-85/2	8	CoC	256/1k	2/8,1/6	80	4	3P	1.3u§	6		Uses 8085 CPU	IS57a	S162	SSC
98	SWTPC6800	8	SYS	64k	64k/8☑	72	5			6		Uses MOTA6800,5.5x9 in	IS6		STP
99	MDT1004	8	Sys	5k/20k	64k☑	55	13		1.0u§	3	256	6500 Development Tool	IS83		SYK
100	MDT1008	8	Sys	9k/20k	64k☑	55	13		1.0u§	3	256	6500 Development Tool	IS83		SYK
101	MDT1016	8	Sys	17k/20k	64k☑	55	13		1.0u§	3	256	6500 Development Tool	IS83		SYK
102	SY6500	8	ChF	64k	64k/8☑	55	13	2VP	6.0u△	3	256	Arith;Dec,Bin;DMA	IS83	S6	SYK
103	TOKOM80-01	8	SYS	4.0k	128/8	78	4	1P	2.0u§	7		Uses Intel 8080CPU	IS57	S13	TAI
104	TOKOM80-02	8	SYS	4.0k	128/8	78	4	1P	2.0u§	7		Uses Intel 8080CPU	IS57		TAI
105	TOKOM80-03	8	SYS	8.0k	128/8	78	4	1P	2.0u§	7		Uses Intel 8080CPU	IS57		TAI
106	TOKOM80-04	8	SYS	8.0k	128/8	78	4	1P	2.0u§	7		Uses Intel 8080CPU	IS57		TAI
107	TOKOM80-05	8	SYS	8.0k	128/8	78	4	1P	2.0u§	7		Uses Intel 8080CPU	IS57		TAI
108	TMS8080A	8	ChF	65k	512/8	78	4	V		6		Binary And Decimal	IS9		TII
109	MICROMULE	8	CoC	128/4k	2/8	72	7	MV	2.0u*	9	M	4 Bit BCD Input,1 PIA			TLI
110	MIKUL600	8	CdF	64k	64k/8☑	72	7	MV		6	M	Inds Cont;Uses 6800	IS6		TLI

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

2. MICROCOMPUTER SYSTEMS

IN ORDER OF: (1)DATA BITS (2)MANUFACT. CODE & (3)SYSTEM TYPE No.

LINE No.	[3] SYSTEM TYPE No.	ORGANIZ -ATION [1] DATA BITS	ARCHI -TECT -URE	SYS. CONFIGURATION ADDRESSABLE MEMORY (RAM/ROM) (BYTES)	I/O DEV @PT WIDTH (D/WDTH)	No. BASIC MICRO INSTR	No. ADDR MODE	INTERR -UPT LEVEL No. & TYPE	INSTRUCT TIME-TYP §CLK CYC *-MIN (s)	No. GEN PUR-POSE REG	STACK LEVEL	SYMBOL: PT-PORT V-VECTORED P-PRIORITY M-MULTIPLE OTHER CAPABILITIES	INSTR SET REF. No.	SYSTEM DWG.	[2] MFR. CODE
1	MIKUL6008-2	8	CdF	64k/8k	4/8	72	7	MV	2.0u*	6	M	2PIA,2ACIA			TLI
2	MIKUL6008-3	8	CdF	64k/8k	4/8	72	7	MV	2.0u*	6	M	2PIA,1ACIA,1PTM			TLI
3	MIKUL6809-1	8	CdF	64k/8k	6/8	59	9	MV	2.0u*	9	M	3PIA			TLI
4	MIKUL6809-2	8	CdF	64k/8k	4/8	59	9	MV	2.0u*	9	M	2PIA,2ACIA			TLI
5	MIKUL6809-3	8	CdF	64k/8k	4/8	59	9	MV	2.0u*	9	M	2PIA,1ACIA,1PTM			TLI
6#	EX-80	8		2K/4K											TOSJ
7#	EX-80BS	8		16K/16K/											TOSJ
8#	TDS400	8		48K/16K											TOSJ
9#	TDS800	8		64K/16K											TOSJ
10	MECA43	8	SYS	65k		88	7	16PV	2.7u	16		8 Bit Slice ALU	IS109		TSC
11	MWPS	8	SYS	64k	158	10	10	128PV	1.0u	12		Uses A80,4MHz,630kB Stor	IS65		VGI
12	VECTOR1PLUS	8	SYS	64k	256/8	78	4	8PV		6	M	Uses 8080A CPU,W/FD,S100	IS57		VGI
13	VECTORMZ	8	SYS	64k	256/8	158	10	NPV	1.0u	12		Uses Z80,4MHz,630kB Stor	IS65		VGI
14	MCP1600	8	ChF	64k	8/8	84		7	600n△	26		3 Chip CPU,RAM,ROM,I/O	IS15	S8	WDC
15	uPSeries	8	SYS	64k	128/8	72	4	8		6		Uses Intel 8080A	IS57	S30	WLD
16	CM6800	8	CoC	64k	64k/8☑	72				6		Uses MOTA 6800 MPU	IS6		WTK
17	MCZ	8	CdF	65k	512/8	158	10	NVP	4.0us	12	M	Uses Z80 CPU	IS65		ZIL
18	PDS	8	CdF	65k	512/8	158	10	NVP	4.0us	12	M	Uses Z80 CPU	IS65		ZIL
19	Z80-MCB	8	CoC	4k/4k	2/8	158	10	NVP	1.6u	12		Uses Z80 CPU	IS65	S99	ZIL
20	ZDS	8	CdF	65k	512/8	158	10	MPV	4.0us	12	M	Development System	IS65		ZIL
21	HB61000	12	CoC	256/1k	64/12	67	2		2.5u*	6		Single Cycle	IS3	S146	HAS
22	HM6100	12	ChF	4k/4k	64/12	67	2	2PV	2.5u*	6		DMA,Single Clock	IS3		HAS
23	IM6100	12	ChF	4k	64/12	67	2	2PV	2.5u*	6		5 CPU Perform Classes	IS3	S62	INL
24	PCM-12A	12	CdF	32k	63/12	67	3	MPV	5.0u			Uses IM6100CPU	IS3		PCM
25#	EX-1A	12		4KW											TOSJ
26#	EX-12/5	12	CdF	1KW/1KW											TOSJ
27#	TLCS12	12	ChF	4.0k	4k/12	18		8	30u	7		Microprogrammed	IS49	S47	TOSJ
28#	TLCS12A	12	ChF	4.0k	4k/12	19	7	8MP	20u	8		Microprogrammed	IS50		TOSJ
29▼	Am96/4116	16	MOD	32k/8k	3/8			8P		16		5-16Bit,Up/Down Counters			AMD
30▼	S6801	16	CLF	128/2k	32/4	72	7	2S	1.0u§	6	M	Expand to 65k;Ser Commun	IS11		AMI
31▼	S6801E	16	CLF	128/2k	32/4	72	7	2S	1.0u§	6	M	Periph Con;Expand Multip	IS11		AMI
32▼	S6803	16	CLF	128/2k	32/4	72	7	2S	1.0u§	6	M	S6801 No Rom	IS11		AMI
33▼	S6803NR	16	CLF	128/2k	32/4	72	7	2S	1.0u§	6	M	S6801 No ROM/RAM	IS11		AMI
34	S9900	16	ChF	4k	256/12			16P	12u	16		Mult/Divide Hardware	IS10	S5	AMI
35	S9940	16	uCT	128/2k	256/16	58	7	4P	1.6u*	16		Same as TMS9940	IS69	S81	AMI
36	S9980	16	ChF	16k	256/16	69	8	4P	12u*	16		Same as TMS9980	IS10	S80	AMI
37▼	S9981	16	CLF	16k	256/16	69	8	4P	12u*	16		w/on Chip Crystal Oscill	IS10	S80	AMI
38	AMC95/4016	16	CoC	8k/12k	24/2							Evaluation Board			AUC
39	8562	16	CoC	2k/0k	61/16		5	16P	2.4u	4		mN601CPU,Max Mem 32k			DGC
40	8563	16	CoC	4k/0k	61/16		5	16P	2.4u	4		mN601CPU,Max Mem 32k			DGC
41	MBC/1	16	CoC	2k/4k	32/1	41	5	16P	2.4u	4		Uses mN601 CPU	IS66	S157	DGC
42	MICRONOVA	16	ChF	32k	61/16		5	16P	2.4u	4		Uses mN601CPU	IS66	S59	DGC
43	MP100	16	uCT*	128k	61	41	5	16P	480n§	13	15	Uses MN602CPU	IS117		DGC
44	9445	16	ChF	64k	62/16		7			11		Microflame II			FSC
45	GA16/110	16	CoC	64k	64/16	91	11	VP	500n	16		CPU,Mem I/O,7.75X11in	IS44	S49	GEN
46	GA16/220	16	CdF	64k	64/16	93	11	VP	500n	16		2 Card System	IS44	S50	GEN
47	GIMINI	16	CdF	65k	65k/16☑	87	4	2	1.6-4.8u	8		Uses GIC CP1600CPU	IS36	S55	GIC
48	H18	16	CdF	64k		130	11	8P	5.7u	11		Based On 2900 Family	IS110	S155	HACC
49	H11	16	SYS	32k	4.0k/16	74		1VP		8		Uses LSI11 CPU			HEA
50	MCS86	16	ChF	1M	64k/16	111	24		200n§	12		Uses D8086 CPU	IS108	S142	ITL
51	SDK86	16	CoC	2k/8k			24	256V				Uses D8086 CPU	IS108	S143	ITL
52	MC68000	16	ChF	16M		61	14	8PV	.5-1.5u	16		VLSI	IS104		MOTA
53	IMP16C	16	CdF	64k	64k/16	43	4	1V	7.0u	4		Extended Instr Set Avail	IS42	S69	NSC
54	IMP16L	16	SYS	64k	64k/16	43	4	4	7.0u	4	16	For OEM Applications	IS42	S33	NSC
55	IMP16P	16	SYS	64k	64k/16	43	4	1V	7.0u	4		Dev Sys W/IMP16C Cards	IS42	S35	NSC
56	INS8900	16	ChF	64k	64k☑	45	7	6PV	8.5-17u	4	10	Fixed Inst uProc	IS99	S131	NSC
57	IPC16C	16	ChF	64k	64k/16	45	6	6VP	10u	4	10	8 or 16 Bit Data Word	IS40	S32	NSC
58	IPC16P	16	SYS	64k	64k/16	45	6	6PV	10u	4	10	Sys Mem Size Options	IS40	S32	NSC
59#	LKIT16	16	SYS	16.5k	8/16	33	6	3P	3.0u	5	M	Kit,Uses MN1610CPU	IS30		PAFJ
60#	PFL16A	16	CdF	128k	256/16	33	6	3P	3.5u	5	M	Uses MN1610CPU	IS30	S23	PAFJ
61	MIPROC16	16	CdF	64k	256/16	83	8	256V	350n§	1		Develop,Core,MOS Mem Cds	IS111	S24	PLM
62	MIPROC-16AS	16	CdF	64k/64k	256	170	8	8VP	250n	3	MEM				PLM
63	MIPROC-16F	16	CdF	64k/64k	256	170	8	8VP	250n	3	MEM				PLM
64	MIPROC-16M	16	CdF	64k/64k	64k☑	185	8	8VP	275n	3	MEM				PLM
65	MIK11/2	16	SYS	32k/4k						8		LSI11/2 CPU,Instr Set			SEC
66▼	SyZ8-01MCCCS	16	uCT	128/2k	4/8	43	11	6VP	2.2u			2Prog 8BitCounter/Timers	IS121	C112	SYK
67▼	SyZ8-01MCCPS	16	uCT	128/2k	4/8	43	11	6VP	2.2u			2Prog 8BitCounter/Timers	IS121	C112	SYK
68▼	SyZ8-02MPDQS	16	uCT	128/	4/8	43	11	6VP	2.2u			2Prog 8BitCounter/Timers	IS121	C112	SYK
69	990/4	16	SYS	64k	8k/16	69	5	8VP		16		Ext Stack,Interrupts	IS10	S5	TII
70	TM990/189	16	CoC	2k/4k	32k/8	69	7	16V	4.0u§		M	Uses TMS9980 CPU	IS95		TII
71	TM990/201-41	16	CdF	2k/4k	32k/16k				450n			Memory Expansion MOD			TII
72	TM990/201-42	16	CdF	4k/8k	32k/16k				450n			Memory Expansion MOD			TII
73	TM990/201-43	16	CdF	8k/16k	32k/16k				450n			Memory Expansion MOD			TII
74	TM990/203-21	16	CdF	16k	64k/32k							Microcomputer MOD		TII	TII
75	TM990/203-22	16	CdF	32k	64k/32k							Microcomputer MOD			TII
76	TM990/203-23	16	CdF	64k	64k/32k							Microcomputer MOD			TII
77	TM990/206-41	16	CdF	4k/16					450n			RAM Expansion MOD			TII
78	TM990/206-42	16	CdF	8k/16					450n			RAM Expansion MOD			TII
79	TM990/305	16	CdF	32k								Input/Output Memory MOD			TII
80	TM990/1240R	16	CdF	256/16								Analog I/O Subsystem			TII
81	TM990/1241R	16	CdF	256/16								Analog I/O Subsystem			TII
82	TM990/1241S	16	CdF	256/16								Analog I/O Subsystem			TII
83	TM990/1243	16	CdF	256/16								Analog I/O Subsystem			TII
84	TMS9940	16	uCT	128/2k	256/16	58	7	4P	1.6u*	16		Single Chip	IS69	S81	TII
85	TMS9940E	16	uCT	128/2k	256/16	58	7	4P	2.5u§	16		Single Chip			TII
86	TMS9940M	16	uCT	128/2k	256/16	58	7	4P	2.5u§	16		Single Chip			TII
87	MP1600	16	ChF	65k		112	23	5				4 Ch CPU;Data/Con/MICRON	IS15	S8a	WDC
88	WD900	16	CoC	64k		100		4				Pascal Intermediate Code	IS119		WDC
89	WD9000	16	ChF	*/11k▼		100		4				Pascal Intermediate Code	IS119	S167	WDC
90	Z8-01-MCCPS	16	ChF	128/2k	32/4	43	11	6MPV	2.2u			One Chip Microcomputer	IS121	*	ZIL
91	Z8-02MPDCS	16	ChF	128/2k	32/4	43	11	6MP	2.2u			One Chip Microcomputer	IS121	*	ZIL

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1▼	MFC01		IO-07	MOD		Floppy Controller Module for 1Drive	
2▼	S6805	AMI6800	uCT	CHIP	MNX	8-Bit uComputer;64 Bytes RAM;1100 Bytes ROM;116 Bytes Self Check ROM	
3	MMS1117-36	LSI11	IO-55	MOD		96k PDP-11 UNIBUS Compatible PMOTA DP-11 UNIBUS Compatible PS	
4	MRM-858	M Series	RAM	MOD		4k Static RAM Card CLI atic RAM Card	
5	C8041A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for ITL Peripheral Interface for MM	
6▼	MC146805E2P	M6800	CPU	Chip	MCG	CPU:8 Bit Static w/RAM,I/O,and Timer;Plastic Pkg	
7#	SMP-E2-A1	SMP	CPU	MOD		CPU Serial I/O Card,2MHz 8085A,DMA	
8#	SMP-E207	SMP	IO-33	MOD		Parallel Output w/24 Relays SIEG lel Output w/24 Relays	
9	MK78037	Z80	DEV	MOD		Complete Video Display Unit MOS ete Video Display Unit	
10	MK3885N-4	Z80A-MOS	IO-20	Chip	MNG	Same as MK3885N Except Max CloMOS as MK3885N Except Max CloMOS	
11	SYP6514B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;XtSYK uP;Addressable Mem 8k;Xtase	ase
12	CS2/3	Z2	COMP	UNIT		Z80A 4MHz;1k ROM;192k RAM;3 User;PT I/O;2 5inch Flpys;S-100 Bus;	cro
13	F3852	F8	IO-03	Chip	MNX	Dynamic Memory Interface;40 PiFSC ic Memory Interface;40 Pi	fsc
14	AMC96/4016	AmZ8000	DEV	MOD		Evaluation Board;8k Bytes of RAM Memory w/ROM Monitor	AuC
15	AMC96/4016-KBD	AmZ8000	PE-61	MOD		56-Key Keyboard;20 Character Alpha-Numeric Led Display	AuC
16	SYSTEM29	Am2900	DEV	UNIT	BTD	Complete Microprogrammed System Development Lab	AuC
17	AMC95/4000	Am9080A	COMP	MOD		8 Bit Single Board System;Uses Am9080A,A-4CPU-2 Clock Rates 2 Or 4MHz	AuC
18	AMC95/5032	Am9080A	CROM	MOD		ROM/EPROM/IO Board-to 64KBYTES;24Prog I/O Lines;Timing Contr W/8MHz Xtal	AuC
19	AmSYS8/8	Am9080A	DEV	UNIT		For Z8000,Z80,8080,8085 Proc;32kb R/W Mem;Dual Fl Drives;Multimaster Bus	AuC
20	AMC95/6110	Am9080A	IO-07	MOD		Single-Dens Floppy Contr;Up to 4 Std Drives;Multibus 8 and 16 Bit If	AuC
21	AMC95/6011	Am9080A	IO-90	MOD		Arith Processor Using Am9500;Floating Pt Single,Double Precision Format	AuC
22	AmSYSCRT	Am9080A	PE-23	UNIT		CRT Terminal	AuC
23	AmSYSPTR	Am9080A	PE-24	UNIT		Line Printer	AuC
24	AmSYSPROM	Am9080A	PE-50	UNIT		PROM Programmer	AuC
25	AMC95/1016	Am9080A	RAM	MOD		16kByte Dyn RAM Board W/Refresh(on Card HW),R/W Buffers;Access Time330ns	AuC
26	AMC95/1032	Am9080A	RAM	MOD		32kByte Dyn RAM Board W/Refresh(on Card HW),R/W Buffers;Access Time330ns	AuC
27#	TFK10660	PPS4	CPU	Chip	MPX	4 Bit Parallel Processor;4 Phase Dynamic Logic;Used In PPS4 Syst	ALGG
28#	TFKA17	PPS4	IO-57	Chip	MPX	ROM/RAM/IO;2k Bytes ROM,128x4 Bit Words Ram	ALGG
29#	TFK10432	PPS4	RAM	Chip	MPX	256x4 RAM	ALGG
30#	TFK10932	PPS4	RAM	Chip	MPX	512x4 RAM	ALGG
31#	TFK11660	PPS4/2	CPU	Chip	MPX	4 Bit Parallel Processor With 128/2k Bytes RAM/ROM	ALGG
32#	TFK10696	PPS4,8	IO-33	Chip	MPX	General Purpose Input/Output Device	ALGG
33▼	Am95/5132		IO-57	MOD		PROM,ROM,RAM and I/O;Up to 64k PROM/32k RAM in Multibus Compatible Bd	AMD
34▼	Am96/4116	AmZ8000	uCT	MOD		Monoboard Computer:Uses AmZ8002CPU at 4.0MHz	AMD
35▼	AmZ8073	AmZ8000	IO-01	Chip		Sys Timing Controller:Five-16 Bit Counters:Up/down and Binary BCD Count	AMD
36▼	Am9517A-1PC	AmZ8000	IO-03	Chip	MNG	Multimode DMA Controller:4 Independent DMA Chs each w/Separate Address	AMD
37▼	Am9517A-4DC	AmZ8000	IO-03	Chip	MNG	Multimode DMA Controller:4 Independent DMA Chs each w/Separate Address	AMD
38▼	Am9517A-4PC	AmZ8000	IO-03	Chip	MNG	Multimode DMA Controller:4 Independent DMA Chs each w/Separate Address	AMD
39▼	Am9517ADC	AmZ8000	IO-03	Chip	MNG	Multimode DMA Controller:4 Independent DMA Chs each w/Separate Address	AMD
40▼	Am9517ADM	AmZ8000	IO-03	Chip	MNG	Multimode DMA Controller:4 Independent DMA Chs each w/Separate Address	AMD
41▼	Am9517APC	AmZ8000	IO-03	Chip	MNG	Multimode DMA Controller:4 Independent DMA Chs each w/Separate Address	AMD
42▼	Am95/6120	AmZ8000	IO-07	MOD		Intelligent FD Cont:Inc-Am8085A Proc;FD1793 FD Cont;1k RAM;Am9517A DMA	AMD
43▼	AmZ8163	AmZ8000	IO-11	ChS		Dyn Mem Timing,Rfrsh and EDC Controller;with AmZ8127/64/60/61/62,Opt RAM	AMD
44▼	AmZ8068	AmZ8000	IO-22	Chip	MNG	Data Ciphering Processor:Std Encryption and Decryption Algorithms	AMD
45▼	Am95/3310	AmZ8000	IO-23	MOD		Comm I/O Exp Bd:4 Sync/Async Serial I/O Comm Chs;Prog Baud Rates to 38400	AMD
46▼	AmZ8161	AmZ8000	IO-31	Chip	BTD	4 Bit Error Correction Multiple Bus Buffers;Inverting Data Bus	AMD
47▼	AmZ8162	AmZ8000	IO-31	Chip	BTD	4 Bit Error Correction Multiple Bus Buffers;Non-Inverting Data Bus	AMD
48▼	Am9511A-1DC	AmZ8000	IO-90	Chip	MNG	Arith Processor:Fixed Point 16 and 32 Bit Operations;3.0MHz Clk Freq	AMD
49▼	Am9511A-1DM	AmZ8000	IO-90	Chip	MNG	Arith Processor:Fixed Point 16 and 32 Bit Operations;3.0MHz Clk Freq	AMD
50▼	Am9511ADC	AmZ8000	IO-90	Chip	MNG	Arith Processor:Fixed Point 16 and 32 Bit Operations;2.0MHz Clk Freq	AMD
51▼	Am9511ADM	AmZ8000	IO-90	Chip	MNG	Arith Processor:Fixed Point 16 and 32 Bit Operations;2.0MHz Clk Freq	AMD
52▼	Am9512-1DC	AmZ8000	IO-90	Chip		Floating Point Processor:Single 32-Bit and Double 64 Bit Precision Cap.	AMD
53▼	Am9512-1DM	AmZ8000	IO-90	Chip		Floating Point Processor:Single 32-Bit and Double 64 Bit Precision Cap.	AMD
54▼	Am9512DC	AmZ8000	IO-90	Chip		Floating Point Processor:Single 32-Bit and Double 64 Bit Precision Cap.	AMD
55▼	Am9512DM	AmZ8000	IO-90	Chip		Floating Point Processor:Single 32-Bit and Double 64 Bit Precision Cap.	AMD
56▼	Am95/6012	AmZ8000	IO-90	MOD		Floating Point Processor Board;Concurrent Arith Oper for 8/16 Bit uProc	AMD
57▼	Am96/1032	AmZ8000	RAM	MOD		32k Byte RAM Board without Parity;8 Bit/16 Bit Data Bus Compatibility	AMD
58▼	Am2901BDC	Am2900	CPu	Chip	BTD	4 Bit Slice:Read-Modify-Write Cycle 69ns;0° to 70°C	AMD
59▼	Am2901BDM	Am2900	CPu	Chip	BTD	4 Bit Slice:Read-Modify-Write Cycle 88ns;55° to 125°C	AMD
60▼	Am2901BFM	Am2900	CPu	Chip	BTD	4 Bit Slice:Read-Modify-Write Cycle 88ns;55° to 125°C	AMD
61▼	Am2901CDC	Am2900	CPu	Chip	BTD	4 Bit Slice:25-30% Speed Improvement Over Am2901B;0° to 70°C	AMD
62▼	Am2901CDM	Am2900	CPu	Chip	BTD	4 Bit Slice:25-30% Speed Improvement Over Am2901B;55° to 125°C	AMD
63▼	Am2901CFM	Am2900	CPu	Chip	BTD	4 Bit Slice:25-30% Speed Improvement Over Am2901B;55° to 125°C	AMD
64▼	Am2901CPC	Am2900	CPu	Chip	BTD	4 Bit Slice:25-30% Speed Improvement Over Am2901B;0° to 70°C	AMD
65▼	Am29203DC	Am2900	CPu	Chip	BTD	See Am2903,w/BCD Arith;Improved Byte Handling;2 Bidirectional Data Lines	AMD
66▼	Am29203DM	Am2900	CPu	Chip	BTD	See Am2903,w/BCD Arith;Improved Byte Handling;2 Bidirectional Data Lines	AMD
67▼	Am29116	Am2900	CPU	Chip	BTD	16 Bit Bipolar Microprocessor:100ns max Instr Time	AMD
68▼	Am29203FM	Am2900	CPU	Chip	BTD	See Am2903,w/BCD Arith;Improved Byte Handling;2 Bidirectional Data Lines	AMD
69▼	Am2909ADC	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;High Speed Version of Am2909	AMD
70▼	Am2909ADM	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;High Speed Version of Am2909	AMD
71▼	Am2909AFM	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;High Speed Version of Am2909	AMD
72▼	Am2909APC	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;High Speed Version of Am2909	AMD
73▼	Am2911ADC	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;High Speed Version of Am2911	AMD
74▼	Am2911ADM	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;High Speed Version of Am 2911	AMD
75▼	Am2911APC	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;High Speed Version of Am2911	AMD
76▼	Am2925	Am2900	IO-32	Chip	BTD	Sys Clk Gen and Driver:Oscillator to 31MHz	AMD
77▼	Am2950DC	Am2900	IO-33	Chip		8 Bit Bidirectional I/O Ports;Register Full/Empty Flags	AMD
78▼	Am2950DM	Am2900	IO-33	Chip		8 Bit Bidirectional I/O Ports;Register Full/Empty Flags	AMD
79▼	Am2950FM	Am2900	IO-33	Chip		8 Bit Bidirectional I/O Ports;Register Full/Empty Flags	AMD
80▼	Am2950PC	Am2900	IO-33	Chip		8 Bit Bidirectional I/O Ports;Register Full/Empty Flags	AMD
81▼	Am2951DC	Am2900	IO-33	Chip		8 Bit Bidirectional I/O Ports;Register Full/Empty Flags	AMD
82▼	Am2951DM	Am2900	IO-33	Chip		8 Bit Bidirectional I/O Ports;Register Full/Empty Flags	AMD
83▼	Am2951FM	Am2900	IO-33	Chip		8 Bit Bidirectional I/O Ports;Register Full/Empty Flags	AMD
84▼	Am2951PC	Am2900	IO-33	Chip		8 Bit Bidirectional I/O Ports;Register Full/Empty Flags	AMD
85▼	Am8255A-5DC	Am8080A	IO-30	Chip		Gen Purpose Prog I/O:Direct bit Set/Reset Capability;24 Prog I/O Pins	AMD
86▼	Am8255A-5PC	Am8080A	IO-30	Chip		Gen Purpose Prog I/O:Direct bit Set/Reset Capability;24 Prog I/O Pins	AMD
87▼	Am8255ADC	Am8080A	IO-30	Chip		Gen Purpose Prog I/O:Direct bit Set/Reset Capability;24 Prog I/O Pins	AMD
88▼	Am8255APC	Am8080A	IO-30	Chip		Gen Purpose Prog I/O:Direct bit Set/Reset Capability;24 Prog I/O Pins	AMD
89▼	Am95/4010	Am8085A	uCT	MOD	MNX	Monoboard Computer:Uses Am8085AMPU at 4.0MHz Oper	AMD
90▼	Am95/4006/20	Am9080A	uCT	MOD	MNX	Monoboard Computer:2.0MHz Oper;w/Am9080A CPU	AMD
91▼	Am95/4006/21	Am9080A	uCT	MOD	MNX	Monoboard Computer:2.0MHz Oper;w/Am9511A APU,Am9080A CPU	AMD
92▼	Am95/4006/22	Am9080A	uCT	MOD	MNX	Monoboard Computer:2.0MHz Oper;w/Am9512 AP2,Am9080A CPU	AMD
93▼	Am95/4006/40	Am9080A	uCT	MOD	MNX	Monoboard Computer:4.0MHz Oper;w/9080A CPU	AMD
94▼	Am95/4006/41	Am9080A	uCT	MOD	MNX	Monoboard Computer:4.0MHz Oper;w/Am9511A APU,Am9080A CPU	AMD
95▼	Am95/4006/42	Am9080A	uCT	MOD	MNX	Monoboard Computer:4.0MHz Oper;w/Am9512 APU,Am9080A CPU	AMD
96	S6840	AMI 6800	IO-01	Chip		Programmable Timer;4MHz Input;3 Maskable Outputs	AMI
97	S68047	AMI 6800	IO-09	Chip	MNX	Video Display Generator;Generates 4 Alphanum and 8 Graphic Modes	AMI
98	S6854L	AMI 6800	IO-20	Chip		Advanced Data Link Controller for ADCCP,HDLC,SDLC;f clock 660kHz	AMI
99	S6854P	AMI 6800	IO-20	Chip		Advanced Data Link Controller for ADCCP,HDLC,SDLC;f clock 660kHz	AMI
100	S68488P	AMI 6800	IO-33	Chip		IEEE488 Inst Bus Interface Adapter;S6800 Bus Compatible	AMI
101	S6831	AMI 6800	ROM	Chip	MNG	2048x8 Static ROM;Access Time 450ns max;S6830 Pin Compatible	AMI
102	S6831A	AMI 6800	ROM	Chip	MNG	2048x8 Static ROM;Access Time 450ns max;3 Progm Enables	AMI
103	S6831B	AMI 6800	ROM	Chip	MNG	2048x8 Static ROM;Access Time 450ns max;3 Progm Enables	AMI
104	S6831C	AMI 6800	ROM	Chip	MNG	2048x8 Static ROM;Access Time 450ns max;3 Progm Enables	AMI
105	S68332	AMI 6800	ROM	Chip	MNX	4096x8 Static ROM;Access Time 450ns max;2 Chip Selects	AMI
106	S68A00	AMI6800	CPU	Chip	MNG	Higher Speed Version of S6800 CPU;1.5MHz Clock	AMI
107	S68B00	AMI6800	CPU	Chip	MNG	Higher Speed Version of S6800 CPU;2.0MHz Clock	AMI
108	S6800	AMI6800	CPU	Chip	MNX	Processor	AMI
109	S6802	AMI6800	CPU	Chip	MNX	8-Bit CPU;Same as S6800 Plus Internal Clk,Driver,128 Byte RAM	AMI
110	S6802P	AMI6800	CPU	Chip	MNX	8-Bit CPU;Same as S6800 Plus Internal Clk,Driver,128 Byte RAM	AMI

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1▼	S68A02	AMI6800	CPU	CHIP	MNX	8-Bit CPU;Same as S6800 Plus Internal Clk Driver;128 Byte RAM	AMI
2	S68A50	AMI6800	IO-20	Chip	MNG	Asynchronous Communications Interface;Compatible with S68A00 CPU	AMI
3	S68A54L	AMI6800	IO-20	Chip		Advanced Data Link Controller for ADCCP,HDLC,SDLC;f clock 1.0MHz	AMI
4	S68A54P	AMI6800	IO-20	Chip		Advanced Data Link Controller for ADCCP,HDLC,SDLC;f clock 1.0MHz	AMI
5	S68B50	AMI6800	IO-20	Chip	MNG	Asynchronous Communications Interface;Compatible with S68B00 CPU	AMI
6	S1883	AMI6800	IO-20	Chip	MPX	Universal Asynchronous Receiver/Transmitter	AMI
7	S2350	AMI6800	IO-20	Chip	MNX	Synchronous Receiver/Transmitter	AMI
8	S6850	AMI6800	IO-20	Chip	MNX	Asynchronous Communications Interface	AMI
9	S6851	AMI6800	IO-20	Chip		Syn/Asyn Programmable Communication Interface(PCI);Compatible w/6800 CPU	AMI
10	S6852	AMI6800	IO-20	Chip		Synchronous Serial Data Adapter(SSDA),Simul Xmit/Receive	AMI
11	S68A21	AMI6800	IO-30	Chip	MNG	Peripheral Interface Adapter;Compatible with S68A00 CPU	AMI
12	S68B21	AMI6800	IO-30	Chip	MNG	Peripheral Interface Adapter;Compatible with S68B00 CPU	AMI
13	S6820	AMI6800	IO-30	Chip	MNX	Peripheral Interface Adaptor	AMI
14	S6821	AMI6800	IO-30	Chip	MNG	Peripheral Interface Adapter;Compatible with S6800 MPU	AMI
15▼	S68H21	AMI6800	IO-30	CHIP	MNX	8-Bit Peripheral Adapter;Bidir Bus for Commun w/MPU	AMI
16	S6846	AMI6800	IO-57	Chip	MNG	Combination ROM-IO-Timer;Capability of Interfacing w/S6800 CPU	AMI
17▼	S2811	AMI6800	IO-90	CHIP	MNX	Signal Process Peripheral;(Prog);Adder/Subtracter;Accum and I/O	AMI
18	S6894	AMI6800	IO-92	Chip		Data Encryption Unit	AMI
19▼	S2814	AMI6800	IO-92	CHIP	MNX	FFT XFMR;32 Complex or 64 Real Points;XFMR Expandable	AMI
20▼	S68A52	AMI6800	IO20	CHIP	MNX	Synchronous Serial DATA Adapter (SSDA);Simul Xmit/Receive	AMI
21▼	S68B52	AMI6800	IO20	CHIP	MNX	Synchronous Serial DATA Adapter (SSDA);Simul Xmit/Receive	AMI
22▼	S68B54	AMI6800	IO20	CHIP	MNX	Advanced Data Link Controller for ADCCP, HDLC, SDLC, fclk 1.5MHz	AMI
23	S68A10	AMI6800	RAM	Chip	MNG	128x8 Static RAM;Compatible with S68A00 CPU	AMI
24	S68B10	AMI6800	RAM	Chip	MNG	128x8 Static RAM;Compatible with S68B00 CPU	AMI
25	S6810	AMI6800	RAM	Chip	MNX	128 x 8 RAM	AMI
26	S6810-1	AMI6800	RAM	Chip	MNX	128 x 8 RAM	AMI
27	S6830	AMI6800	ROM	Chip	MNX	1024 x 8 ROM	AMI
28	S6834	AMI6800	ROM	Chip	MPX	512 x 8 Eraseable And Electrically Reprogrammable ROM	AMI
29	S6834-1	AMI6800	ROM	Chip	MNX	512 x 8 Eraseable And Electrically Reprogrammable ROM	AMI
30	S68631	AMI6800	ROM	Chip	MNG	2048 x 8 Static ROM	AMI
31♦	S2000	S2000	uCT	Chip	MNG	4-Bit Single Chip uC;1.0k x 8 ROM,64 x 4 RAM;7-Seg LED Dec/Drv	AMI
32♦	S2000A	S2000	uCT	Chip	MNG	4-Bit Single Chip uC;1.0k x 8 ROM,64 x 4 RAM;Hi-Volt Fluor Drv	AMI
33♦	S2150	S2000	uCT	Chip	MNG	4-Bit Single Chip uC;1.5k x 8 ROM,80 x 4 RAM;7-Seg LED Dec/Drv	AMI
34♦	S2150A	S2000	uCT	Chip	MNG	4-Bit Single Chip uC;1.5k x 8 ROM,80 x 4 RAM;Hi-Volt Fluor Drv	AMI
35♦	S2400	S2000	uCT	Chip	MNG	4-Bit Single Chip uC;4.0k x 8 ROM,128 x 4 RAM;7-Seg LED Dec/Drv;A/D Conv	AMI
36♦	S2400A	S2000	uCT	Chip	MNG	4-Bit Single Chip uC;4.0k x 8 ROM,128 x 4 RAM;Hi-Volt Fluor Drv;A/D Conv	AMI
37	S2152	S2000	uCT	CHIP	MNG	8Bit Single Chip uC;7-Seg LED Dec/Dri;Exten of S2000/S2150 uComp Family	AMI
38	S2210	S2000	uCT	CHIP	MCG	S2000 W/Interrupts,On-Chip A/D D/A Conv;Capable of Multiplex 8 Channels	AMI
39	SES2000	S2000	DEV	MOD	MNG	S2000 Emulator Board	AMI
40	S9900	S9900	CPU	Chip	MNG	16 Bit Microprocessor;Hardware Multiply/Divide Capability	AMI
41	S9980	S9900	CPU	Chip	MNG	16 Bit Microprocessor;8 Bit Data Bus and On-Chip Clock	AMI
42▼	S9981	S9900	CPU	CHIP	MNG	16-Bit uProcessor;8-Bit Data Bus w/on Chip Crystal Oscillator	AMI
43	S9902	S9900	IO-20	Chip	MNG	Asynchronous Communications Controller	AMI
44	S9903	S9900	IO-20	Chip	MNG	Synchronous Communications Controller	AMI
45	S9901	S9900	IO-30	Chip	MNG	Programmable System Interface;Provides Interrupt Control;Incl Clock	AMI
46	Am9517DC		IO-03	Chip		Multimode DMA Controller; 4 DMA Channels;Mem to Mem Transfers;3MHz Clock	AMV
47	Am2901ADC	Am2900	CPU	Chip	BTD	4 Bit Slice;Improved Replacement For Am2901;0 To 70°C;Hermetic DIP	AMV
48	Am2901ADM	Am2900	CPU	Chip	BTD	4 Bit Slice;Improved Replacement For Am2901;-55 To 125°C;Hermetic DIP	AMV
49	Am2901AFM	Am2900	CPU	Chip	BTD	4 Bit Slice;Improved Replacement For Am2901;-55 To 125°C;Flatpack	AMV
50	Am2901APC	Am2900	CPU	Chip	BTD	4 Bit Slice;Improved Replacement For Am2901;0 To 70°C;Molded DIP	AMV
51	Am2901AXC	Am2900	CPU	Chip	BTD	4 Bit Slice;Improved Replacement for Am2901;0 to 70°C,Dice Pkg	AMV
52	Am2901DC	Am2900	CPU	Chip	BTD	4 Bit Slice;Temp 0° To 70°C	AMV
53	Am2901DM	Am2900	CPU	Chip	BTD	4 Bit Slice;Temp -55 To 125°C	AMV
54	Am2901FM	Am2900	CPU	Chip	BTD	4 Bit Slice;Temp -55 To 125°C	AMV
55	Am2901PC	Am2900	CPU	Chip	BTD	4 Bit Slice;Temp 0° To 70°C	AMV
56	Am2903DC	Am2900	CPU	Chip	BTD	4 Bit Expandable Microprocessor Slice SUPERSLICE;o to 70°C	AMV
57	Am2903DM	Am2900	CPU	Chip	BTD	4 Bit Expandable Microprocessor Slice SUPERSLICE;-55 to 125°C	AMV
58	Am2903FM	Am2900	CPU	Chip	BTD	4 Bit Expandable Microprocessor Slice;Temp -55-125°C;Flat Pack Pkg	AMV
59	Am2900K1	Am2900	DEV	MOD	BTD	System Evaluation and Learning Kit	AMV
60	Am2909DC	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;Temp 0 To 70°C	AMV
61	Am2909DM	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;Temp -55 To 125°C	AMV
62	Am2909FM	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;Temp -55 To 125°C	AMV
63	Am2909PC	Am2900	IO-01	Chip	BTD	Microprogram Sequencer;Temp 0 To 70°C	AMV
64	Am2910DC	Am2900	IO-01	Chip	BTD	12 Bit Microprogram Controller,Address Sequencer,0-70°C,Hermetic DIP	AMV
65	Am2910DM	Am2900	IO-01	Chip	BTD	12 Bit Microprogram Controller,Address Sequencer,-55-125°C,Hermetic DIP	AMV
66	Am2910FM	Am2900	IO-01	Chip	BTD	12 Bit Microprogram Controller,Address Sequencer,-55-125°C,Hermetic Flat	AMV
67	Am2910PC	Am2900	IO-01	Chip	BTD	12 Bit Microprogram Controller,Address Sequencer,0 to 70°C,Plastic DIP	AMV
68	Am2911DC	Am2900	IO-01	Chip	BTD	Microprogram Sequencer Used With Am2901 Processor Slice Units	AMV
69	Am2911DM	Am2900	IO-01	Chip	BTD	Microprogram Sequencer Used With Am2901 Processor Slice Units	AMV
70	Am2911PC	Am2900	IO-01	Chip	BTD	Microprogram Sequencer Used With Am2901 Processor Slice Units	AMV
71	Am2930DC	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions,0-70°C,Hermetic DIP	AMV
72	Am2930DM	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions,-55-125°C,HermeticDIP	AMV
73	Am2930FM	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions,-55-125°C,HermeticFlt	AMV
74	Am2930PC	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions,0-70°C,Molded DIP	AMV
75	Am2930XC	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions,0-70°C,Dice	AMV
76	Am2930XM	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions,-55-125°C,Dice	AMV
77	Am2931DC	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;0-70°C,Hermetic DIP	AMV
78	Am2931DM	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;-55-125°C,HermeticDIP	AMV
79	Am2931FM	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;-55-125°C,HermeticFlt	AMV
80	Am2931PC	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;0-70°C,Molded DIP	AMV
81	Am2931XC	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;0-70°C,Dice	AMV
82	Am2931XM	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;-55-125°C,Dice	AMV
83	Am2932DC	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;0-70°C,Hermetic DIP	AMV
84	Am2932DM	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;-55-125°C,HermeticDIP	AMV
85	Am2932FM	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;-55-125°C,HermeticFlt	AMV
86	Am2932PC	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;0-70°C,Molded DIP	AMV
87	Am2932XC	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;0-70°C,Dice	AMV
88	Am2932XM	Am2900	IO-01	Chip	BTD	4 Bit Program Control Unit for Addressing Functions;-55-125°C,Dice	AMV
89	Am29803DC	Am2900	IO-01	Chip	BTD	16 Way Branch Control Used W/Sequencer Am2909;0 To 70°C;Hermetic DIP	AMV
90	Am29803DM	Am2900	IO-01	Chip	BTD	16 Way Branch Control Used W/Sequencer Am2909;-55 To 125°C;Hermetic DIP	AMV
91	Am29803FM	Am2900	IO-01	Chip	BTD	16 Way Branch Control Used W/Sequencer Am2909;-55 To 125°C;Flatpack	AMV
92	Am29803PC	Am2900	IO-01	Chip	BTD	16 Way Branch Control Used W/Sequencer Am2909;0 To 70°C;Molded DIP	AMV
93	Am29811DC	Am2900	IO-01	Chip	BTD	Next Address Control Used W/Sequencer Am2911;0 To 70°C;Hermetic DIP	AMV
94	Am29811DM	Am2900	IO-01	Chip	BTD	Next Address Control Used W/Sequencer Am2911;-55 To 125;Hermetic DIP	AMV
95	Am29811FM	Am2900	IO-01	Chip	BTD	Next Address Control Used W/Sequencer Am2911;-55 To 125;Flatpack	AMV
96	Am29811PC	Am2900	IO-01	Chip	BTD	Next Address Control Used W/Sequencer Am2911;0 To 70°C;Molded DIP	AMV
97	Am2913DC	Am2900	IO-02	Chip	BTD	Priority Interrupt Expander Used With 2914 Priority Interrupt Encoder	AMV
98	Am2913DM	Am2900	IO-02	Chip	BTD	Priority Interrupt Expander Used With 2914 Priority Interrupt Encoder	AMV
99	Am2913FM	Am2900	IO-02	Chip	BTD	Priority Interrupt Expander Used With 2914 Priority Interrupt Encoder	AMV
100	Am2913PC	Am2900	IO-02	Chip	BTD	Priority Interrupt Expander Used With 2914 Priority Interrupt Encoder	AMV
101	Am2914DC	Am2900	IO-02	Chip	BTD	8 Bit Vectored Priority Interrupt Encoder;0-70°C,Hermetic DIP Pkg	AMV
102	Am2914DM	Am2900	IO-02	Chip	BTD	8 Bit Vectored Priority Interrupt Encoder;-55-125°C Hermetic DIP Pkg	AMV
103	Am2914FM	Am2900	IO-02	Chip	BTD	8 Bit Vectored Priority Interrupt Encoder;-55-125°C Hermetic Flat Pkg	AMV
104	Am2914PC	Am2900	IO-02	Chip	BTD	8 Bit Vectored Priority Interrupt Encoder;0-70°C,Molded DIP Pkg	AMV
105	Am2914XC	Am2900	IO-02	Chip	BTD	8 Bit Vectored Priority Interrupt Encoder;0-70°C,Dice Pkg	AMV
106	Am2914XM	Am2900	IO-02	Chip	BTD	8 Bit Vectored Priority Interrupt Encoder;-55-125°C Dice Pkg	AMV
107	Am2940DC	Am2900	IO-03	Chip	BTD	DMA Address Generator,Executes 8 Diff Instrs 0-70°C;Hermetic DIP	AMV
108	Am2940DM	Am2900	IO-03	Chip	BTD	DMA Address Generator,Executes 8 Diff Instrs 55-125°C;Hermetic DIP	AMV
109	Am2940FM	Am2900	IO-03	Chip	BTD	DMA Address Generator,Executes 8 Diff Instrs 55-125°C;Flat Pack	AMV
110	Am2940PC	Am2900	IO-03	Chip	BTD	DMA Address Generator,Executes 8 Diff Instrs 0-70°C;Molded DIP	AMV

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	Am2942DC	Am2900	IO-03	Chip	BTD	Programable Timer/Counter;0-70°C;Hermetic DIP;DMA Address Generator	AMV
2	Am2942DM	Am2900	IO-03	Chip	BTD	Programable Timer/Counter;55-125°C;Hermetic DIP;DMA Address Generator	AMV
3	Am2942FM	Am2900	IO-03	Chip	BTD	Programable Timer/Counter;55-125°C;Flat Package;DMA Address Generator	AMV
4	Am2942PC	Am2900	IO-03	Chip	BTD	Programable Timer/Counter;0-70°C;Molded DIP;DMA Address Generator	AMV
5	Am2904DC	Am2900	IO-12	Chip	BTD	Status and Shift Control Unit;Temp 0-70°C;Hermetic DIP	AMV
6	Am2904DM	Am2900	IO-12	Chip	BTD	Status and Shift Control Unit;Temp -55-125°C;Hermetic DIP	AMV
7	Am2904FM	Am2900	IO-12	Chip	BTD	Status and Shift Control Unit;Temp -55-125°C;Flat Pack Pkg	AMV
8	Am2904PC	Am2900	IO-12	Chip	BTD	Status and Shift Control Unit;Temp 0-70°C;Molded DIP	AMV
9	Am2905DC	Am2900	IO-21	Chip	BTD	Quad 2 Input Bus Transceiver;3 State Receiver;0 To 70°C	AMV
10	Am2905DM	Am2900	IO-21	Chip	BTD	Quad 2 Input Bus Transceiver;3 State Receiver;-55 To 125°C	AMV
11	Am2905FM	Am2900	IO-21	Chip	BTD	Quad 2 Input Bus Transceiver;3 State Receiver;-55 To 125°C	AMV
12	Am2905PC	Am2900	IO-21	Chip	BTD	Quad 2 Input OC Bus Transceiver;3 State Receiver;0 To 70°C	AMV
13	Am2906DC	Am2900	IO-21	Chip	BTD	Quad 2 Input Bus Transceiver;Parity;0 To 70°C	AMV
14	Am2906DM	Am2900	IO-21	Chip	BTD	Quad 2 Input Bus Transceiver;Parity;-55 To 125°C	AMV
15	Am2906FM	Am2900	IO-21	Chip	BTD	Quad 2 Input Bus Transceiver;Parity;-55 To 125°C	AMV
16	Am2906PC	Am2900	IO-21	Chip	BTD	Quad 2 Input Bus Transceiver;Parity;0 To 70°C	AMV
17	Am2907DC	Am2900	IO-21	Chip	BTD	Quad Bus Transceiver;3 State Receiver;Parity;0 To 70°C	AMV
18	Am2907DM	Am2900	IO-21	Chip	BTD	Quad Bus Transceiver;3 State Receiver;Parity;-55 To 125°C	AMV
19	Am2907FM	Am2900	IO-21	Chip	BTD	Quad Bus Transceiver;3 State Receiver;Parity;-55 To 125°C	AMV
20	Am2907PC	Am2900	IO-21	Chip	BTD	Quad Bus Transceiver;3 State Receiver;Parity;0 To 70°C	AMV
21	Am2915ADC	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver W/Interface Logic;Temp 0-70°C;Hermetic DIP	AMV
22	Am2915ADM	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver W/Interface Logic;Temp-55-125°C;Hermetic DIP	AMV
23	Am2915AFM	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver W/Interface Logic;Temp-55-125°C;Flat Pack	AMV
24	Am2915APC	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver W/Interface Logic;Temp 0-70°C;Molded DIP	AMV
25	Am2915DC	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr W/Interface Logic;Temp 0 To 70;Hermetic DIP	AMV
26	Am2915DM	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr W/Interface Logic;Temp-55 To 125;Hermetic DIP	AMV
27	Am2915FM	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr W/Interface Logic;Temp-55 To 125;Flatpack	AMV
28	Am2915PC	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr W/Interface Logic;Temp 0 To 70;Molded DIP	AMV
29	Am2916ADC	Am2900	IO-21	Chip	BTD	Quad High-Speed LSI Bus Transceiver W/Interface Logic;Temp 0-70°C	AMV
30	Am2916ADM	Am2900	IO-21	Chip	BTD	Quad High-Speed LSI Bus Transceiver W/Interface Logic;Temp -55-125°C	AMV
31	Am2916AFM	Am2900	IO-21	Chip	BTD	Quad High-Speed LSI Bus Transceiver W/Interface Logic;Temp -55-125°C	AMV
32	Am2916APC	Am2900	IO-21	Chip	BTD	Quad High-Speed LSI Bus Transceiver W/Interface Logic;Temp 0-70°C	AMV
33	Am2916DC	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr;Interface Logic;Parity;0 To 70;Hermetic DIP	AMV
34	Am2916DM	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr;Interface Logic;Parity;-55 To 125;Hermetic DIP	AMV
35	Am2916FM	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr;Interface Logic;Parity;-55 To 125;Flatpack	AMV
36	Am2916PC	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr;Interface Logic;Parity;0 To 70;Molded DIP	AMV
37	Am2917ADC	Am2900	IO-21	Chip	BTD	Quad 3-State Bus Transceiver W/Interface Logic;Hermetic DIP;Temp 0-70°C	AMV
38	Am2917ADM	Am2900	IO-21	Chip	BTD	Quad 3-State Bus Transceiver W/Interface Logic;Hermetic DIP;Temp-55-125°C	AMV
39	Am2917AFM	Am2900	IO-21	Chip	BTD	Quad 3-State Bus Transceiver W/Interface Logic;Flat Pack;Temp -55-125°C	AMV
40	Am2917APC	Am2900	IO-21	Chip	BTD	Quad 3-State Bus Transceiver W/Interface Logic;Molded DIP;Temp 0-70°C	AMV
41	Am2917DC	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr;Interface Logic;Parity;0 To 70;Hermetic DIP	AMV
42	Am2917DM	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr;Interface Logic;Parity;-55 To 125;Hermetic DIP	AMV
43	Am2917FM	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr;Interface Logic;Parity;-55 To 125;Flatpack	AMV
44	Am2917PC	Am2900	IO-21	Chip	BTD	Quad 3 State Bus Transcvr;Interface Logic;Parity;0 To 70;Molded DIP	AMV
45	Am29LS18DC	Am2900	IO-55	Chip	BTD	4 Bit Regist W/Standard and 3 State Outputs;Temp 0 to 70°C;Hermetic DIP	AMV
46	Am29LS18DM	Am2900	IO-55	Chip	BTD	4 Bit Regist W/Standard and 3 State Outputs;Temp-55 to 125°C;Hermetic DIP	AMV
47	Am29LS18FM	Am2900	IO-55	Chip	BTD	4 Bit Regist W/Standard and 3 State Outputs;Temp -55 to 125°C;Flat Pack	AMV
48	Am29LS18PC	Am2900	IO-55	Chip	BTD	4 Bit Regist W/Standard and 3 State Outputs;Temp 0 to 70°C;Molded DIP	AMV
49	Am2918DC	Am2900	IO-55	Chip	BTD	4 Bit Regist W/Standard And 3 State Outputs;Temp 0 To 70;Hermetic DIP	AMV
50	Am2918DM	Am2900	IO-55	Chip	BTD	4 Bit Regist W/Standard And 3 State Outputs;Temp-55 To 125;Hermetic DIP	AMV
51	Am2918FM	Am2900	IO-55	Chip	BTD	4 Bit Regist W/Standard And 3 State Outputs;Temp-55 To 125;Flatpack	AMV
52	Am2918PC	Am2900	IO-55	Chip	BTD	4 Bit Regist W/Standard And 3 State Outputs;Temp 0 To 70;Molded DIP	AMV
53	Am2919DC	Am2900	IO-55	Chip	BTD	Quad Register W/Dual Three-State Outputs;Temp 0-70°C;Hermetic DIP	AMV
54	Am2919DM	Am2900	IO-55	Chip	BTD	Quad Register W/Dual Three-State Outputs;Temp -55-125°C;Hermetic DIP	AMV
55	Am2919FM	Am2900	IO-55	Chip	BTD	Quad Register W/Dual Three-State Outputs;Temp -55-125°C;Flat Pack	AMV
56	Am2919PC	Am2900	IO-55	Chip	BTD	Quad Register W/Dual Three-State Outputs;Temp 0-70°C;Molded DIP	AMV
57	Am2902DC	Am2900	IO-90	Chip	BTD	Look Ahead Carry Generator For Up To 4 Am2901 Units;0 To 70°C	AMV
58	Am2902DM	Am2900	IO-90	Chip	BTD	Look Ahead Carry Generator For Up To 4 Am2901 Units;-55 To 125°C	AMV
59	Am2902FM	Am2900	IO-90	Chip	BTD	Look Ahead Carry Generator For Up To 4 Am2001 Units;-55 To 125°C	AMV
60	Am2902PC	Am2900	IO-90	Chip	BTD	Look Ahead Carry Generator For Up To 4 Am2901 Units;0 To 70°C	AMV
61	Am29750DC	Am2900	PROM	Chip	BTD	32x8 Field Programmable ROM;Open Coll;Temp 0 To 75;Hermetic DIP	AMV
62	Am29750DM	Am2900	PROM	Chip	BTD	32x8 Field Programmable ROM;Open Coll;Temp -55 To 125;Hermetic DIP	AMV
63	Am29751DC	Am2900	PROM	Chip	BTD	32x8 Field Programmable ROM;Three State;Temp 0 To 75;Hermetic DIP	AMV
64	Am29751DM	Am2900	PROM	Chip	BTD	32x8 Field Programmable ROM;Three State;Temp -55 To 125;Hermetic DIP	AMV
65	Am29760DC	Am2900	PROM	Chip	BTD	256x4 Field Programmable ROM;Open Coll;Temp 0 To 75;Hermetic DIP	AMV
66	Am29760DM	Am2900	PROM	Chip	BTD	256x4 Field Programmable ROM;Open Coll;Temp -55 To 125;Hermetic DIP	AMV
67	Am29760FM	Am2900	PROM	Chip	BTD	256x4 Field Programmable ROM;Open Coll;Temp -55 To 125;Flatpack	AMV
68	Am29761DC	Am2900	PROM	Chip	BTD	256x4 Field Programmable ROM;Three State;Temp 0 To 75;Hermetic DIP	AMV
69	Am29761DM	Am2900	PROM	Chip	BTD	256x4 Field Programmable ROM;Three State;Temp -55 To 125;Hermetic DIP	AMV
70	Am29761FM	Am2900	PROM	Chip	BTD	256x4 Field Programmable ROM;Three State;Temp -55 To 125;Flatpack	AMV
71	Am29700DC	Am2900	RAM	Chip	BTD	16x4 RAM;Non-Invert;Open Collector;Temp 0 To 75;Hermetic DIP	AMV
72	Am29700DM	Am2900	RAM	Chip	BTD	16x4 RAM;Non-Invert;Open Collector;Temp-55 To 125;Hermetic DIP	AMV
73	Am29700FM	Am2900	RAM	Chip	BTD	16x4 RAM;Non-Invert;Open Collector;Temp-55 To 125;Flatpack	AMV
74	Am29700PC	Am2900	RAM	Chip	BTD	16x4 RAM;Non-Invert;Open Collector;Temp 0 To 75;Molded DIP	AMV
75	Am29701DC	Am2900	RAM	Chip	BTD	16x4 RAM;Non-Invert;Three State Temp 0 To 75;Hermetic DIP	AMV
76	Am29701DM	Am2900	RAM	Chip	BTD	16x4 RAM;Non-Invert;Three State Temp-55 To 125;Hermetic DIP	AMV
77	Am29701FM	Am2900	RAM	Chip	BTD	16x4 RAM;Non-Invert;Three State Temp-55 To 125;Flatpack	AMV
78	Am29701PC	Am2900	RAM	Chip	BTD	16x4 RAM;Non-Invert;Three State Temp 0 To 75;Molded DIP	AMV
79	Am29702DC	Am2900	RAM	Chip	BTD	16x4 RAM;Invert;Open Collector;Temp 0 To 75;Hermetic DIP	AMV
80	Am29702DM	Am2900	RAM	Chip	BTD	16x4 RAM;Invert;Open Collector;Temp-55 To 125;Hermetic DIP	AMV
81	Am29702FM	Am2900	RAM	Chip	BTD	16x4 RAM;Invert;Open Collector;Temp-55 To 125;Flatpack	AMV
82	Am29702PC	Am2900	RAM	Chip	BTD	16x4 RAM;Invert;Open Collector;Temp 0 To 75;Molded DIP	AMV
83	Am29703DC	Am2900	RAM	Chip	BTD	16x4 RAM;Invert;Three State Temp 0 To 75;Hermetic DIP	AMV
84	Am29703DM	Am2900	RAM	Chip	BTD	16x4 RAM;Invert;Three State Temp-55 To 125;Hermetic DIP	AMV
85	Am29703FM	Am2900	RAM	Chip	BTD	16x4 RAM;Invert;Three State Temp-55 To 125;Flatpack	AMV
86	Am29703PC	Am2900	RAM	Chip	BTD	16x4 RAM;Invert;Three State Temp 0 To 75;Molded DIP	AMV
87	Am29704DC	Am2900	RAM	Chip	BTD	16x4 Bit 2 Port RAM;Open Collector;Temp 0 To 70;Hermetic DIP	AMV
88	Am29704DM	Am2900	RAM	Chip	BTD	16x4 Bit 2 Port RAM;Open Collector;Temp-55 To 125;Hermetic DIP	AMV
89	Am29704FM	Am2900	RAM	Chip	BTD	16x4 Bit 2 Port RAM;Open Collector;Temp-55 To 125;Flatpack	AMV
90	Am29704PC	Am2900	RAM	Chip	BTD	16x4 Bit 2 Port RAM;Open Collector;Temp 0 To 70;Molded DIP	AMV
91	Am29705DC	Am2900	RAM	Chip	BTD	16x4 Bit 2 Port RAM;Three State Temp 0 To 70;Hermetic DIP	AMV
92	Am29705DM	Am2900	RAM	Chip	BTD	16x4 Bit 2 Port RAM;Three State Temp-55 To 125;Hermetic DIP	AMV
93	Am29705FM	Am2900	RAM	Chip	BTD	16x4 Bit 2 Port RAM;Three State Temp-55 To 125;Flatpack	AMV
94	Am29705PC	Am2900	RAM	Chip	BTD	16x4 Bit 2 Port RAM;Three State Temp 0 To 70;Molded DIP	AMV
95	Am29720DC	Am2900	RAM	Chip	BTD	256x1 Bit RAM;Open Collector;Temp 0 To 75;Hermetic DIP	AMV
96	Am29720DM	Am2900	RAM	Chip	BTD	256x1 Bit RAM;Open Collector;Temp-55 To 125;Hermetic DIP	AMV
97	Am29720FM	Am2900	RAM	Chip	BTD	256x1 Bit RAM;Open Collector;Temp-55 To 125;Flatpack	AMV
98	Am29720PC	Am2900	RAM	Chip	BTD	256x1 Bit RAM;Open Collector;Temp 0 To 75;Molded DIP	AMV
99	Am29721DC	Am2900	RAM	Chip	BTD	256x1 Bit RAM;Three State Temp 0 To 75;Hermetic DIP	AMV
100	Am29721DM	Am2900	RAM	Chip	BTD	256x1 Bit RAM;Three State Temp-55 To 125;Hermetic DIP	AMV
101	Am29721FM	Am2900	RAM	Chip	BTD	256x1 Bit RAM;Three State Temp-55 To 125;Flatpack	AMV
102	Am29721PC	Am2900	RAM	Chip	BTD	256x1 Bit RAM;Three State Temp 0 To 75;Molded DIP	AMV
103	Am9080A1DC	Am9080A	CPU	Chip	MNG	8 Bit Microprocessor;0-70°C,Clock Period 320ns,Hermetic DIP	AMV
104	Am9080A1PC	Am9080A	CPU	Chip	MNG	8 Bit Microprocessor;0-70°C,Clock Period 320ns,Molded DIP	AMV
105	Am9080A2DC	Am9080A	CPU	Chip	MNG	8 Bit Microprocessor;0-70°C,Clock Period 380ns,Hermetic DIP	AMV
106	Am9080A2DM	Am9080A	CPU	Chip	MNG	8 Bit Microprocessor;-55-125°C,Clock Period 380ns,Hermetic DIP	AMV
107	Am9080A2PC	Am9080A	CPU	Chip	MNG	8 Bit Microprocessor;0-70°C,Clock Period 380ns,Molded DIP	AMV
108	Am9080A4DC	Am9080A	CPU	Chip	MNG	8 Bit Microprocessor;0-70°C,Clock Period 250ns,Hermetic DIP	AMV
109	Am9080ADC	Am9080A	CPU	Chip	MNG	8 Bit Microprocessor;0-70°C,Clock Period 480ns,Hermetic DIP	AMV
110	Am9080ADM	Am9080A	CPU	Chip	MNG	8 Bit Microprocessor;-55-125°C,Clock Period 480ns,Hermetic DIP	AMV

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE
1	Am9080APC	Am9080A	CPU	Chip	MNG	8 Bit Microprocessor;0-70°C,Clock Period 480ns,Molded DIP	AMV
2	Am9513CC	Am9080A	IO-01	Chip		Sys Timing Controller;Time of Day Mode Option;Counting Rates 10MHz Max	AMV
3	Am9513DC	Am9080A	IO-01	Chip		Sys Timing Controller;Time of Day Mode Option;Counting Rates 10MHz Max	AMV
4	Am9513DM	Am9080A	IO-01	Chip		Sys Timing Controller;Time of Day Mode Option;Counting Rates 10MHz Max	AMV
5	Am9513PC	Am9080A	IO-01	Chip		Sys Timing Controller;Time of Day Mode Option;Counting Rates 10MHz Max	AMV
6	Am8228DM	Am9080A	IO-02	Chip	MNG	System Controller And Bus Driver;-55-125°C,Hermetic DIP Pkg	AMV
7	Am8228PC	Am9080A	IO-02	Chip	MNG	System Controller And Bus Driver;0-70°C,Molded DIP Pkg	AMV
8	Am8228XC	Am9080A	IO-02	Chip	BTD	System Controller and Bus Driver;0-70°C,Dice	AMV
9	Am8238DM	Am9080A	IO-02	Chip	BTD	System Controller and Bus Driver;-55-125°C,Hermetic DIP	AMV
10	Am8238PC	Am9080A	IO-02	Chip	BTD	System Controller and Bus Driver;0-70°C,Molded DIP	AMV
11	Am8238XC	Am9080A	IO-02	Chip	BTD	System Controller and Bus Driver;0-70°C,Dice	AMV
12	Am9519-1CC	Am9080A	IO-02	Chip		Universal Interrupt Controller;8085A Compatible 8 Maskable Interrups	AMV
13	Am9519-1DC	Am9080A	IO-02	Chip		Universal Interrupt Controller;8085A Compatible 8 Maskable Interrupts	AMV
14	Am9519-1PC	Am9080A	IO-02	Chip		Universal Interrupt Controller;8085A Compatible 8 Maskable Interrupts	AMV
15	Am9519CC	Am9080A	IO-02	Chip		Universal Interrupt Controller;8 Maskable Interrupts	AMV
16	Am9519DC	Am9080A	IO-02	Chip		Universal Interrupt Controller;8 Maskable Interrupts	AMV
17	Am9519DM	Am9080A	IO-02	Chip		Universal Interrupt Controller;8 Maskable Interupts	AMV
18	Am9519PC	Am9080A	IO-02	Chip		Universal Interrupt Controller;8 Maskable Interrupts	AMV
19	D8238	Am9080A	IO-02	Chip	BTD	System Controller and Bus Driver;0-70°C,Hermetic DIP	AMV
20	Am9517-1DC	Am9080A	IO-03	Chip		Multimode DMA Controller;4 DMA Channels;Mem To Mem Transfers;3MHz Clock	AMV
21	Am9517-1PC	Am9080A	IO-03	Chip		Multimode DMA Controller;4 DMA Channels;Mem To Mem Transfers;3MHz Clock	AMV
22	Am9517-4DC	Am9080A	IO-03	Chip		Multimode DMA Controller;4 DMA Channels;Mem To Mem Transfers;3MHz Clock	AMV
23	Am9517-4PC	Am9080A	IO-03	Chip		Multimode DMA Controller;4 DMA Channels;Mem To Mem Transfers;3MHz Clock	AMV
24	Am9517DM	Am9080A	IO-03	Chip		Multimode DMA Controller;4 DMA Channels;Mem To Mem Transfers;3MHz Clock	AMV
25	Am9517PC	Am9080A	IO-03	Chip		Multimode DMA Controller;4 DMA Channels;Mem To Mem Transfers;3MHz Clock	AMV
26	Am9551-4DC	Am9080A	IO-20	Chip	MNG	8 Bit Programmable Communications Interface;0-70°C,Hermetic DIP	AMV
27	Am9551DC	Am9080A	IO-20	Chip	MNG	8 Bit Programmable Communications Interface;0-70°C,Hermetic DIP	AMV
28	Am9551DM	Am9080A	IO-20	Chip	MNG	8 Bit Programmable Communications Interface;-55-125°C,Hermetic DIP	AMV
29	Am8216XC	Am9080A	IO-21	Chip	BTD	4 Bit Parallel Bidirectional Bus Driver;0-70°C,Dice	AMV
30	Am8226XC	Am9080A	IO-21	Chip	BTD	4 Bit Parallel Bidirectional Bus Driver;0-70°C,Dice	AMV
31	MD8216	Am9080A	IO-21	Chip	BTD	4 Bit Parallel Bidirectional Bus Driver;-55-125°C,Hermetic DIP	AMV
32	MD8226	Am9080A	IO-21	Chip	BTD	4 Bit Parallel Bidirectional Bus Driver;-55-125°C,Hermetic DIP	AMV
33	Am9555-4DC	Am9080A	IO-30	Chip	MNG	8 Bit High-Speed Programmable Peripheral Interface;0-70°C,Hermetic DIP	AMV
34	Am9555DC	Am9080A	IO-30	Chip	MNG	8 Bit High-Speed Programmable Peripheral Interface;0-70°C,Hermetic DIP	AMV
35	Am9555DM	Am9080A	IO-30	Chip	MNG	8 Bit High-Speed Programmable Peripheral Interface;-55-125°C,Hermetic DIP	AMV
36	Am25LS240DC	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;0-70°C,Hermetic DIP	AMV
37	Am25LS240DM	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;-55-125°C,Hermetic DIP	AMV
38	Am25LS240PC	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;0-70°C,Molded DIP	AMV
39	Am25LS240XC	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;0-70°C,Dice	AMV
40	Am25LS240XM	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;-55-125°C,Dice	AMV
41	Am25LS241DC	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;0-70°C,Hermetic DIP	AMV
42	Am25LS241DM	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;-55-125°C,Hermetic DIP	AMV
43	Am25LS241PC	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;0-70°C,Molded DIP	AMV
44	Am25LS241XC	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;0-70°C,Dice	AMV
45	Am25LS241XM	Am9080A	IO-31	Chip	BTD	Octal Buffer/Line Driver With 3-State Outputs;-55-125°C,Dice	AMV
46	Am8224DM	Am9080A	IO-32	Chip	MNG	Clock Generator/Driver;-55-125°C,Hermetic DIP Pkg	AMV
47	Am8224PC	Am9080A	IO-32	Chip	MNG	Clock Generator/Driver;0-70°C,Molded DIP Pkg	AMV
48	Am8224XC	Am9080A	IO-32	Chip	BTD	Clock Generator/Driver;0-70°C,Dice	AMV
49	Am8212DM	Am9080A	IO-33	Chip	MNG	8 Bit Input/Output Port;-55-125°C,Hermetic DIP Pkg	AMV
50	Am8212XC	Am9080A	IO-33	Chip	BTD	8 Bit Input/Output Port;0-70°C,Dice	AMV
51	C8212	Am9080A	IO-33	Chip	MNG	8 Bit Input/Output Port;0-70°C,Hermetic DIP Pkg	AMV
52	Am25LS138DM	Am9080A	IO-44	Chip	MNG	3-Line To 8 Line Decoder/Demultiplex;-55-125°c,Hermetic DIP Pkg	AMV
53	Am25LS138FM	Am9080A	IO-44	Chip	MNG	3-Line To 8 Line Decoder/Demultiplex;-55-125°c,Hermetic Flat Pkg	AMV
54	Am25LS138PC	Am9080A	IO-44	Chip	MNG	3-Line To 8 Line Decoder/Demultiplex;0-70°c,Molded DIP Pkg	AMV
55	Am25LS138XC	Am9080A	IO-44	Chip	MNG	3-Line To 8 Line Decoder/Demultiplex;0-70c,Dice Pkg	AMV
56	Am25LS138XM	Am9080A	IO-44	Chip	MNG	3-Line To 8 Line Decoder/Demultiplex;-55-125°c,Dice Pkg	AMV
57	Am25LS139DC	Am9080A	IO-44	Chip	BTD	Dual 2-Line to 4-Line Decoder/Demultiplexer;0-70°C,Hermetic DIP	AMV
58	Am25LS139DM	Am9080A	IO-44	Chip	BTD	Dual 2-Line to 4-Line Decoder/Demultiplexer;-55-125°C,Hermetic DIP	AMV
59	Am25LS139FM	Am9080A	IO-44	Chip	BTD	Dual 2-Line to 4-Line Decoder/Demultiplexer;-55-125°C,Hermetic Flat	AMV
60	Am25LS139PC	Am9080A	IO-44	Chip	BTD	Dual 2-Line to 4-Line Decoder/Demultiplexer;0-70°C,Molded DIP	AMV
61	Am25LS139XC	Am9080A	IO-44	Chip	BTD	Dual 2-Line to 4-Line Decoder/Demultiplexer;0-70°C,Dice	AMV
62	Am25LS139XM	Am9080A	IO-44	Chip	BTD	Dual 2-Line to 4-Line Decoder/Demultiplexer;-55-125°C,Dice	AMV
63	Am1702ADC	Am9080A	PROM	Chip	MPG	256x8 Prog Erasable ROM,0-70°C,Hermetic DIP/Quartz Lid	AMV
64	Am9702AHDL	Am9080A	PROM	Chip	MNG	256x8 Prog Erasable ROM,-55-125°C,Hermetic DIP/Quartz Lid	AMV
65	Am90R16CDC	Am9080A	RAM	Chip	MNG	16k Bit x 1 Dynamic RAM;4ms Refresh Interval;0°-70°C;Access Time 300ns	AMV
66	Am90R16DDC	Am9080A	RAM	Chip	MNG	16k Bit x 1 Dynamic RAM;4ms Refresh Interval;0°-70°C;Access Time 250ns	AMV
67	Am90R16EDC	Am9080A	RAM	Chip	MNG	16k Bit x 1 Dynamic RAM;4ms Refresh Interval;0°-70°C;Access Time 200ns	AMV
68	Am91L01ADC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
69	Am91L01ADM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
70	Am91L01AFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic Flat Pkg	AMV
71	Am91L01APC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Molded DIP Pkg	AMV
72	Am91L01BDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP Pkg	AMV
73	Am91L01BDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
74	Am91L01BFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic Flat Pkg	AMV
75	Am91L01BPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Molded DIP Pkg	AMV
76	Am91L01CDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
77	Am91L01CDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
78	Am91L01CPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Molded DIP Pkg	AMV
79	Am91L02ADC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 500ns,Hermetic DIP Pkg	AMV
80	Am91L02ADM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 500ns,Hermetic DIP Pkg	AMV
81	Am91L02AFM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 500ns,Hermetic Flat Pkg	AMV
82	Am91L02APC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 500ns,Molded DIP Pkg	AMV
83	Am91L02BDC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 400ns,Hermetic DIP Pkg	AMV
84	Am91L02BDM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 400ns,Hermetic DIP Pkg	AMV
85	Am91L02BFM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 400ns,Hermetic Flat Pkg	AMV
86	Am91L02BPC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 400ns,Molded DIP Pkg	AMV
87	Am91L02CDC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 300ns,Molded DIP Pkg	AMV
88	Am91L02CDM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 300ns,Hermetic DIP Pkg	AMV
89	Am91L02CPC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 300ns,Hermetic Flat Pkg	AMV
90	Am91L02DC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 650ns,Hermetic DIP Pkg	AMV
91	Am91L02DM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 650ns,Hermetic DIP Pkg	AMV
92	Am91L02FM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 650ns,Hermetic Flat Pkg	AMV
93	Am91L02PC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 650ns,Molded DIP Pkg	AMV
94	Am91L11ADC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
95	Am91L11ADM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
96	Am91L11AFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic Flat Pkg	AMV
97	Am91L11APC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Molded DIP Pkg	AMV
98	Am91L11BDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Molded DIP Pkg	AMV
99	Am91L11BDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
100	Am91L11BFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic Flat Pkg	AMV
101	Am91L11BPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Molded DIP Pkg	AMV
102	Am91L11CDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
103	Am91L11CDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
104	Am91L11CPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Molded DIP Pkg	AMV
105	Am91L12ADC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
106	Am91L12ADM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
107	Am91L12APC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Molded DIP Pkg	AMV
108	Am91L12BDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP Pkg	AMV
109	Am91L12BDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
110	Am91L12BFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic Flat Pkg	AMV

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE
1	Am91L12BPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Molded DIP Pkg	AMV
2	Am91L12CDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
3	Am91L12CDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
4	Am91L12CPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Molded DIP Pkg	AMV
5	Am91L30ADC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
6	Am91L30ADM	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
7	Am91L30BDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP Pkg	AMV
8	Am91L30BDM	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
9	Am91L30CDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
10	Am91L30CDM	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
11	Am91L30DDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP Pkg	AMV
12	Am91L31ADC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
13	Am91L31ADM	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
14	Am91L31BDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP Pkg	AMV
15	Am91L31BDM	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
16	Am91L31CDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
17	Am91L31CDM	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
18	Am91L31DDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP Pkg	AMV
19	Am91L40ADC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP	AMV
20	Am91L40ADM	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP	AMV
21	Am91L40BDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP	AMV
22	Am91L40BDM	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP	AMV
23	Am91L40CDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP	AMV
24	Am91L40CDM	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP	AMV
25	Am91L40DDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP	AMV
26	Am91L41ADC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
27	Am91L41ADM	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
28	Am91L41BDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP Pkg	AMV
29	Am91L41BDM	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
30	Am91L41CDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
31	Am91L41CDM	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
32	Am91L41DDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP Pkg	AMV
33	Am9016CDC	Am9080A	RAM	Chip	MNG	16k Bit x 1 Dynamic RAM;2ms Refresh Interval;0°-70°C;Access Time 300ns	AMV
34	Am9016DDC	Am9080A	RAM	Chip	MNG	16k Bit x 1 Dynamic RAM;2ms Refresh Interval;0°-70°C;Access Time 250ns	AMV
35	Am9016EDC	Am9080A	RAM	Chip	MNG	16k Bit x 1 Dynamic RAM;2ms Refresh Interval;0°-70°C;Access Time 200ns	AMV
36	Am9050CDC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 300ns,Hermetic DIP Pkg	AMV
37	Am9050CPC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 300ns,Molded DIP Pkg	AMV
38	Am9050DDC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 250ns,Hermetic DIP Pkg	AMV
39	Am9050DPC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 250ns,Molded DIP Pkg	AMV
40	Am9050EDC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 200ns,Hermetic DIP Pkg	AMV
41	Am9050EPC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 200ns,Molded DIP Pkg	AMV
42	Am9060CDC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 300ns,Hermetic DIP Pkg	AMV
43	Am9060CPC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 300ns,Molded DIP Pkg	AMV
44	Am9060DDC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 250ns,Hermetic DIP Pkg	AMV
45	Am9060DPC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 250ns,Molded DIP Pkg	AMV
46	Am9060EDC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 200ns,Hermetic DIP Pkg	AMV
47	Am9060EPC	Am9080A	RAM	Chip	MNG	4096 x 1 Dynamic R/W RAM;Access Time 200ns,Molded DIP Pkg	AMV
48	Am9101ADC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
49	Am9101ADM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
50	Am9101AFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic Flat Pkg	AMV
51	Am9101APC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Molded DIP Pkg	AMV
52	Am9101BDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP Pkg	AMV
53	Am9101BDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
54	Am9101BFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic Flat Pkg	AMV
55	Am9101BPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Molded DIP Pkg	AMV
56	Am9101CDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
57	Am9101CDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
58	Am9101CPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Molded DIP Pkg	AMV
59	Am9101DDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP Pkg	AMV
60	Am9101DPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 250ns,Molded DIP Pkg	AMV
61	Am9101EDC	Am9080A	RAM	Chip	MNG	256x4 Static R/W RAM;0-70°C,Access Time 200ns,Hermetic DIP Pkg	AMV
62	Am9101EPC	Am9080A	RAM	Chip	MNG	256x4 Static R/W RAM;0-70°C,Access Time 200ns,Molded DIP Pkg	AMV
63	Am9102ADC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 500ns,Hermetic DIP Pkg	AMV
64	Am9102ADM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 500ns,Hermetic DIP Pkg	AMV
65	Am9102AFM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 500ns,Hermetic Flat Pkg	AMV
66	Am9102APC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 500ns,Molded DIP Pkg	AMV
67	Am9102BDC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 400ns,Hermetic DIP Pkg	AMV
68	Am9102BDM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 400ns,Hermetic DIP Pkg	AMV
69	Am9102BFM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 400ns,Hermetic Flat Pkg	AMV
70	Am9102BPC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 400ns,Molded DIP Pkg	AMV
71	Am9102CDC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 300ns,Hermetic DIP Pkg	AMV
72	Am9102CDM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 300ns,Hermetic DIP Pkg	AMV
73	Am9102CPC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 300ns,Molded DIP Pkg	AMV
74	Am9102DC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 650ns,Hermetic DIP Pkg	AMV
75	Am9102DDC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 250ns,Hermetic DIP Pkg	AMV
76	Am9102DM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 650ns,Hermetic DIP Pkg	AMV
77	Am9102DPC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 250ns,Molded DIP Pkg	AMV
78	Am9102EDC	Am9080A	RAM	Chip	MNG	1024x1 Static RAM;0-70°C,Cycle Time 200ns,Hermetic DIP Pkg	AMV
79	Am9102EPC	Am9080A	RAM	Chip	MNG	1024x1 Static RAM;0-70°C,Cycle Time 200ns,Molded DIP Pkg	AMV
80	Am9102FM	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;-55-125°C,Cycle Time 650ns,Hermetic Flat Pkg	AMV
81	Am9102PC	Am9080A	RAM	Chip	MNG	1024 x 1 Static RAM;0-70°C,Cycle Time 650ns,Molded DIP Pkg	AMV
82	Am9111ADC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
83	Am9111ADM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
84	Am9111AFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic Flat Pkg	AMV
85	Am9111APC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Molded DIP Pkg	AMV
86	Am9111BDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Molded DIP Pkg	AMV
87	Am9111BDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
88	Am9111BFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic Flat Pkg	AMV
89	Am9111BPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Molded DIP Pkg	AMV
90	Am9111CDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
91	Am9111CDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
92	Am9111CPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Molded DIP Pkg	AMV
93	Am9111DDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP Pkg	AMV
94	Am9111DPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 250ns,Molded DIP Pkg	AMV
95	Am9111EDC	Am9080A	RAM	Chip	MNG	256x4 Static R/W RAM;0-70°C,Access Time 200ns,Hermetic DIP Pkg	AMV
96	Am9111EPC	Am9080A	RAM	Chip	MNG	256x4 Static R/W RAM;0-70°C,Access Time 200ns,Molded DIP Pkg	AMV
97	Am9112ADC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
98	Am9112ADM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
99	Am9112AFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic Flat Pkg	AMV
100	Am9112APC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C Access Time 500ns,Molded DIP Pkg	AMV
101	Am9112BDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP Pkg	AMV
102	Am9112BDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
103	Am9112BFM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic Flat Pkg	AMV
104	Am9112BPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 400ns,Molded DIP Pkg	AMV
105	Am9112CDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
106	Am9112CDM	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
107	Am9112CPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 300ns,Molded DIP Pkg	AMV
108	Am9112DDC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP Pkg	AMV
109	Am9112DPC	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 250ns,Molded DIP Pkg	AMV
110	Am9112EDC	Am9080A	RAM	Chip	MNG	256x4 Static R/W RAM;0-70°C,Access Time 200ns,Hermetic DIP Pkg	AMV

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	Am9112EPC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 200ns,Molded DIP Pkg	AMV
2	Am9130ADC	Am9080A	RAM	Chip	MNG	1024 x 4 Static R/W RAM;0-70°C;Access Time 500ns	AMV
3	Am9130ADM	Am9080A	RAM	Chip	MNG	1024 x 4 Static R/W RAM;-55-125°C;Access Time 500ns	AMV
4	Am9130BDC	Am9080A	RAM	Chip	MNG	1024 x 4 Static R/W RAM;0-70°C;Access Time 400ns	AMV
5	Am9130BDM	Am9080A	RAM	Chip	MNG	1024 x 4 Static R/W RAM;-55-125°C;Access Time 400ns	AMV
6	Am9130CDC	Am9080A	RAM	Chip	MNG	1024 x 4 Static R/W RAM;0-70°C;Access Time 300ns	AMV
7	Am9130CDM	Am9080A	RAM	Chip	MNG	1024 x 4 Static R/W RAM;-55-125°C;Access Time 300ns	AMV
8	Am9130EDC	Am9080A	RAM	Chip	MNG	1024 x 4 Static R/W RAM;0-70°C;Access Time 200ns	AMV
9	Am9131ADC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
10	Am9131ADM	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
11	Am9131BDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP Pkg	AMV
12	Am9131BDM	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
13	Am9131CDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
14	Am9131CDM	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
15	Am9131DDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP Pkg	AMV
16	Am9131EDC	Am9080A	RAM	Chip	MNG	1024x4 Static R/W RAM;0-70°C,Access Time 200ns,Hermetic DIP Pkg	AMV
17	Am9140ADC	Am9080A	RAM	Chip	MNG	4096 x 1 Static R/W RAM;0-70°C;Access Time 500ns	AMV
18	Am9140ADM	Am9080A	RAM	Chip	MNG	4096 x 1 Static R/W RAM;-55-125°C;Access Time 500ns	AMV
19	Am9140BDC	Am9080A	RAM	Chip	MNG	4096 x 1 Static R/W RAM;0-70°C;Access Time 400ns	AMV
20	Am9140BDM	Am9080A	RAM	Chip	MNG	4096 x 1 Static R/W RAM;-55-125°C;Access Time 400ns	AMV
21	Am9140CDC	Am9080A	RAM	Chip	MNG	4096 x 1 Static R/W RAM;0-70°C;Access Time 300ns	AMV
22	Am9140CDM	Am9080A	RAM	Chip	MNG	4096 x 1 Static R/W RAM;-55-125°C;Access Time 300ns	AMV
23	Am9140DDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP	AMV
24	Am9140EDC	Am9080A	RAM	Chip	MNG	4096 x 1 Static R/W RAM;0-70°C;Access Time 200ns	AMV
25	Am9141ADC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
26	Am9141ADM	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;-55-125°C,Access Time 500ns,Hermetic DIP Pkg	AMV
27	Am9141BDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 400ns,Hermetic DIP Pkg	AMV
28	Am9141BDM	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;-55-125°C,Access Time 400ns,Hermetic DIP Pkg	AMV
29	Am9141CDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 300ns,Hermetic DIP Pkg	AMV
30	Am9141CDM	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
31	Am9141DDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 250ns,Hermetic DIP Pkg	AMV
32	Am9141EDC	Am9080A	RAM	Chip	MNG	4096x1 Static R/W RAM;0-70°C,Access Time 200ns,Hermetic DIP Pkg	AMV
33	C2101	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 1.0us,Hermetic DIP Pkg	AMV
34	C2101-1	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
35	C2101-2	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 650ns,Hermetic DIP Pkg	AMV
36	C2111	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 1.0us,Hermetic DIP Pkg	AMV
37	C2111-1	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Hermetic DIP Pkg	AMV
38	C2111-2	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 650ns,Hermetic DIP Pkg	AMV
39	C2112	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 1.0us,Hermetic DIP Pkg	AMV
40	C2112-2	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 650ns,Hermetic DIP Pkg	AMV
41	P2101	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 1.0us,Molded DIP Pkg	AMV
42	P2101-1	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Molded DIP Pkg	AMV
43	P2101-2	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 650ns,Molded DIP Pkg	AMV
44	P2111	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 1.0us,Molded DIP Pkg	AMV
45	P2111-1	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 500ns,Molded DIP Pkg	AMV
46	P2111-2	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 650ns,Molded DIP Pkg	AMV
47	P2112	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 1.0us,Molded DIP Pkg	AMV
48	P2112-2	Am9080A	RAM	Chip	MNG	256 x 4 Static R/W RAM;0-70°C,Access Time 650ns,Molded DIP Pkg	AMV
49	Am2708DC	Am9080A	ROM	Chip	MNG	8,192 Bit,1024x8 Erasable,Programmable ROM;0-70°C	AMV
50	Am9208BDC	Am9080A	ROM	Chip	MNG	1024 x 8 ROM;0-70°C;Access Time 400ns	AMV
51	Am9208BDM	Am9080A	ROM	Chip	MNG	1024 x 8 ROM;-55-125°C;Access Time 400ns	AMV
52	Am9208CDC	Am9080A	ROM	Chip	MNG	1024 x 8 ROM;0-70°C;Access Time 300ns	AMV
53	Am9208CDM	Am9080A	ROM	Chip	MNG	1024x8 ROM;-55-125°C,Access Time 300ns,Hermetic DIP Pkg	AMV
54	Am9208DDC	Am9080A	ROM	Chip	MNG	1024x8 ROM;0-70°C,Access Time 250ns,Hermetic DIP Pkg	AMV
55	Am9214DC	Am9080A	ROM	Chip	MNG	512 x 8 ROM;0-70°C;Access Time 500ns	AMV
56	Am9214DM	Am9080A	ROM	Chip	MNG	512 x 8 ROM;-55-125°C;Access Time 500ns	AMV
57	Am9216BDC	Am9080A	ROM	Chip	MNG	2048 x 8 ROM;0-70°C;Access Time 400ns	AMV
58	Am9216BDM	Am9080A	ROM	Chip	MNG	2048 x 8 ROM;-55-125°C;Access Time 400ns	AMV
59	Am9216CDC	Am9080A	ROM	Chip	MNG	2048 x 8 ROM;0-70°C;Access Time 300ns	AMV
60	Am9217ADC	Am9080A	ROM	Chip	MNG	2048x8 ROM;0-70°C,Access Time 550ns,Hermetic DIP Pkg	AMV
61	Am9217ADM	Am9080A	ROM	Chip	MNG	2048x8 ROM;-55-125°C,Access Time 550ns,Hermetic DIP Pkg	AMV
62	Am9217BDC	Am9080A	ROM	Chip	MNG	2048x8 ROM;0-70°C,Access Time 450ns,Hermetic DIP Pkg	AMV
63	Am9217BDM	Am9080A	ROM	Chip	MNG	2048x8 ROM;-55-125°C,Access Time 450ns,Hermetic DIP Pkg	AMV
64	Am9218BDC	Am9080A	ROM	Chip	MNG	2048x8 ROM;0-70°C,Access Time 450ns,Hermetic DIP Pkg	AMV
65	Am9218BDM	Am9080A	ROM	Chip	MNG	2048x8 ROM;-55-125°C,Access Time 450ns,Hermetic DIP Pkg	AMV
66	Am9218CDC	Am9080A	ROM	Chip	MNG	2048x8 ROM;0-70°C,Access Time 350ns,Hermetic DIP Pkg	AMV
67	Am9702-1DC	Am9080A	ROM	Chip	MNG	256 x 8 Programmable ROM;Access Time 750ns,Quartz Lid Pkg	AMV
68	Am9702-1HDC	Am9080A	ROM	Chip	MNG	256 x 8 Programmable ROM;Access Time 750ns,Hermetic Quartz Lid Pkg	AMV
69	Am9702DC	Am9080A	ROM	Chip	MNG	256 x 8 Programmable ROM;Access Time 1.0us,Quartz Lid Pkg	AMV
70	Am9702HDC	Am9080A	ROM	Chip	MNG	256 x 8 Programmable ROM;Access Time 1.0us,Hermetic Quartz Lid Pkg	AMV
71	Am35141DC	Am9080A	ROM	Chip	MNG	512 x 8 ROM;0-70°C;Access Time 500ns	AMV
72	Am35142DC	Am9080A	ROM	Chip	MNG	512 x 8 ROM;0-70°C;Access Time 500ns	AMV
73	C1702	Am9080A	ROM	Chip	MNG	256 x 8 Programmable ROM;Access Time 1.0us,Quartz Lid Pkg	AMV
74	C1702-1	Am9080A	ROM	Chip	MNG	256 x 8 Programmable ROM;Access Time 750ns,Quartz Lid Pkg	AMV
75	C1702A	Am9080A	ROM	Chip	MNG	256 x 8 Programmable ROM;Erasable And Reprogrammable By UV	AMV
76	C8316E	Am9080A	ROM	Chip	MNG	2048x8 ROM;0-70°C,Access Time 450ns,Hermetic DIP Pkg	AMV
77	AmZ8001	Z8000	CPU	Chip		Segmented 48 Pin CPU;	AMV
78	AmZ8002	Z8000	CPU	Chip		Non Segmented 40 Pin CPU;	AMV
79	AmZ8036	Z8000	IO-01	Chip		CIO:Counter Timer Input/Output	AMV
80	AmZ8050	Z8000	IO-07	Chip		FDC:Floppy Disk Controller	AMV
81	AmZ8030	Z8000	IO-20	Chip		SIO:Serial Input/Output	AMV
82	AmZ8010	Z8000	IO-3	Chip		MMU:Memory Management Unit for Z8000 CPU	AMV
83	AmZ8016	Z8000	IO-3	Chip		DMA:Direct Memory Access for Z8000 CPU	AMV
84	AmZ8038	Z8000	IO-55	Chip		FIO:First In/First Out,Input/Output	AMV
85	AmZ8060	Z8000	IO-57	Chip		FIFO:First In/First Out Buffer	AMV
86	AmZ8052	Z8000	PE-23	Chip		CRT:CRT Controller	AMV
87	Am8085ACC	8085	CPU	Chip		8 Bit uP; 8080 Compat;3MHz Internal Clock,Ceramic	AMV
88	Am8085ADC	8085	CPU	Chip		8 Bit uP; 8080 Compat;3MHz Internal Clock,Side Brazed Ceramic	AMV
89	Am8085APC	8085	CPU	Chip		8 Bit uP; 8080 Compat;3MHz Internal Clock,Plastic	AMV
90	Am8257DC	8085	IO-03	Chip		4 Channel Direct Memory Access Controller;Ceramic	AMV
91	Am8257DM	8085	IO-03	Chip		4 Channel Direct Memory Access Controller;Ceramic;Military Grade	AMV
92	Am8257PC	8085	IO-03	Chip		4 Channel Direct Memory Access Controller;Plastic	AMV
93	Am8279-5CC	8085	IO-10	Chip		Programmable Keyboard/Display Interface;8 Chr FIFO Buffer;Tad 250ns Max	AMV
94	Am8279-5PC	8085	IO-10	Chip		Programmable Keyboard/Display Interface;8 Chr FIFO Buffer;tad 250ns Max	AMV
95	Am8279CC	8085	IO-10	Chip		Programmable Keyboard/Display Interface;8 Chr FIFO Buffer;tad 450ns Max	AMV
96	Am8279PC	8085	IO-10	Chip		Programmable Keyboard/Display Interface;8 Chr FIFO Buffer;Tad 450ns Max	AMV
97	RTI-1252	LSI-11/2	IO-40	MOD		Output Subsystem W/2-4 Ana Outputs Plus 4 Logic Driver Outputs	ANA
98	RTI-1250	LSI-11/2	IO-41	MOD		16 Diff or 32 Single-Ended Channels/12-Bit Resolution/Ana Input Subsys	ANA
99	RTI-1251-R	LSI-11/2	IO-42	MOD		16-Ch Ana In/2-Ch of 12-Bit Ana Out at Up to ±10V I/O Card	ANA
100	RTI-1201	MCS80	IO-40	MOD		Intel Compatible Output Subsystem;SBC80 Compatible;8 Ch Output	ANA
101	RTI-1202	MCS80	IO-41	MOD		Intel Compatible Analog Input Real Time Interface;32 In Ch on Bd	ANA
102	RTI-1200	MCS80	IO-42	MOD		Real Time Analog I/O Interface;SBC80 Compatible;12B ADC/DAC,32 In Ch	ANA
103	RTI-1221	MPS-800	IO-40	MOD		Pro-Log Compatible Real Time Analog I/O Interface;Analog Output Board	ANA
104	RTI-1220	MPS-800	IO-41	MOD		Pro-Log Compatible Real Time Analog I/O Interface;Analog Data Acq in Bd	ANA
105	RTI-1232	M6800	IO-40	MOD		Motorola Compatible Analog I/O Subsys;Ana/Dig Output Subsystem	ANA
106	RTI-1230	M6800	IO-41	MOD		Motorola Compatible Analog I/O Subsys;Analog Input Subsystem	ANA
107	RTI-1231	M6800	IO-42	MOD		Motorola Compatible Analog I/O Subsys;Analog I/O Subsy,10 Bit DAC	ANA
108	RTI-1225	Z80/8085	IO-42	MOD		8 Diff or 16 Single-Ended Op I/O Card Build Around the 10 Bit AD571	ANA
109	RTI-1242	990	IO-40	MOD		TI Compat Real Time I/O Subsys;Output Subsys;Four 12 Bit DAC	ANA
110	RTI-1243	990	IO-40	MOD		TI Compat Real Time I/O Subsys;Output Subsys;Eight 12 Bit DAC	ANA

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	RTI-1240	990	IO-41	MOD		TI Compatible Real Time Analog I/O Subsystems;Analog Input Subsys	ANA
2	RTI-1241	990	IO-42	MOD		TI Compatible Real Time Analog I/O Subsystems;Analog I/O Subsystem	ANA
3▼	Am2901BPC	Am2900	CPu	Chip	BTD	4 Bit Slice:Read-Modify-Write AMD Slice:Read-Modify-Write	AND
4	A2B0004	APPLEII	COMP	MOD	MNG	Single Board Home Comp,4k RAM;ROM-Pes BASIC Interp,Monitor,Assemb,Diass	APL
5	A2B0016	APPLEII	COMP	MOD	MNG	Single Board Home Comp,16k RAM;ROM-Pes BASIC Interp,Monitor,Assemb,Diass	APL
6	A2B0032	APPLEII	COMP	MOD	MNG	Single Board Home Comp,32k RAM;ROM-Pes BASIC Interp,Monitor,Assemb,Diass	APL
7	A2B0048	APPLEII	COMP	MOD	MNG	Single Board Home Comp,48k RAM;ROM-Pes BASIC Interp,Monitor,Assemb,Diass	APL
8	A2S0004	APPLEII	COMP	UNIT	MNG	Video Hookup Hobby Comp W/Full ASCII Keybd;Uses MCS6502 CPU,4k RAM	APL
9	A2S0016	APPLEII	COMP	UNIT	MNG	Video Hookup Hobby Comp W/Full ASCII Keybd;Uses MCS6502 CPU,16k RAM	APL
10	A2S0032	APPLEII	COMP	UNIT	MNG	Video Hookup Hobby Comp W/Full ASCII Keybd;Uses MCS6502 CPU,32k RAM	APL
11	A2S0048	APPLEII	COMP	UNIT	MNG	Video Hookup Hobby Comp W/Full ASCII Keybd;Uses MCS6502 CPU,48k RAM	APL
12	A2B0002	APPLEII	IO-08	MOD		Parallel Printer Interface Card;256x8 PROM on Card,Up to 255 Char/Line	APL
13	A2B0003	APPLEII	IO-20	MOD		Communication Interface Card;110 or 300 Baud;256-Byte PROM on Card	APL
14	A2B0005	APPLEII	IO-20	MOD		Interface Card for Telephone Communication,Printer Control,Or Other Comp	APL
15	A2M0018	APPLEII	IO-21	UNIT		Accoustic Coupler;Links APPLEII to Telephone Network	APL
16	A2M0012	APPLEII	IO-92	UNIT		Remote AC Power Switch;Will Switch Up to 64 Adapters Located at Outlets	APL
17	A2M0015	APPLEII	IO-92	UNIT		Voice Recognition Unit;Up to 32 User-Selected Spoken Words	APL
18	A2M0004	APPLEII	PE-01	UNIT		Floppy Disk II Subsys;300Rpm,100ms Avg Latency,156k Bits/sec,116k Bytes	APL
19	A2M0017	APPLEII	PE-04	UNIT		Cassette Recorder;Operates from Batteries or AC Line;Push Button Control	APL
20	A2M0010	APPLEII	PE-10	UNIT		Elec Discharge;80 Char/Line 150 Lines/Min Full ASCII Set	APL
21	A2M0011	APPLEII	PE-10	UNIT		Impact Printer;132 Char/Line 60 Char/Sec 64 Char Upper Case ASCII	APL
22	A2M0005	APPLEII	PE-15	UNIT		9 Inch Diagonal Video Monitor	APL
23	EVENT2000	EVENTSERIES	COMP	UNIT		8 Bit Computer Using 8080A CPU;Mem Expandable to 64k	APP
24	20-101	LSI11	ROM	MOD		128 Word ROM Board Usable with PDP11 Microcomp Syst	APP
25	20-101S	LSI11	ROM	MOD		128 Word ROM W/Start Switch Option Usable With PDP11 Syst	APP
26	20-102	LSI11	ROM	MOD		256 Word ROM Board Usable with PDP11 Microcomp Syst	APP
27	70-130-142	70 Series	COMP	UNIT		Tape Cartridge,CPU in Enclosure;One 3M Tape Cartridge and CPU	APP
28	70-130-161	70 Series	COMP	UNIT		Disk,CPU in Enclosure;1 IBM Compatible Floppy Disk and 70-100 CPU	APP
29	70-130-162	70 Series	COMP	UNIT		2 Disks,CPU in Enclosure;2 IBM Comp Flop Disc,70-100 CPU	APP
30	70-131-142	70 Series	COMP	UNIT		Tape Cartridge,CPU,Front Panel in Enclosure;One 3M Tape Cart,CPU,Panel	APP
31	70-131-161	70 Series	COMP	UNIT		Disk,CPU,Front Panel in Enclosure;1 IBM Comp Flop Disc,70-100 CPU	APP
32	70-FDF	70 Series	IO-07	MOD		Programmable Multiple Format Floppy Disk Formatter	APP
33	70-151	70 Series	IO-08	MOD		Line Printer Controller	APP
34	70T-300	70 Series	PE-01	UNIT		Programmable Double Density Multiple Format Floppy Disk Test System	APP
35	70-163-10	70 Series	PE-02	UNIT		10 Mbyte Disk Syst;Front Load 5 Mbyte Cart Fixed and Remov Disk	APP
36	70-146-1025	70 Series	PE-04	UNIT		Tape Drive;10 in Reel,25 Ips,9 Track;Tape Drive W/Formatter	APP
37	70-150C700	70 Series	PE-10	UNIT		Line Printer;165 cps,80 Col Matrix Printer;Auto Motor Shut Off	APP
38	70-181	70 Series	PE-42	UNIT		Paper Tape Reader/Punch;3000 cps Reader;75 cps Punch;Fan Fold	APP
39	70-100	70 SERIES	COMP	MOD		8 Bit Computer On A Card With Expansion Options Uses Intel 8080	APP
40	70-173	70 SERIES	DEV	MOD		ROM Programmer	APP
41	70-173L	70 SERIES	DEV	MOD		ROM Eraser;Ultra Violet Light	APP
42	70-120	70 SERIES	IO-03	MOD		ROM Add-On Controller For Expansion Up To 16k	APP
43	70-123	70 SERIES	IO-03	MOD		RAM Add-On Controller For Expansion Up To 16k	APP
44	70-143	70 SERIES	IO-05	MOD		Tape Cartridge Controller	APP
45	70-145	70 SERIES	IO-05	MOD		9 Track Tape Drive Controller And Cable	APP
46	70-175	70 SERIES	IO-06	MOD		Paper Tape Controller	APP
47	70-151T40	70 SERIES	IO-08	MOD		Line Printer Controller And Cable	APP
48	70-152	70 SERIES	IO-08	MOD		Character Printer Controller And Cable	APP
49	70-180KB	70 SERIES	IO-10	UNIT		ASC11 Keyboard Interface	APP
50	70-171SA	70 SERIES	IO-22	MOD		Synchronous/Asynchronous Communication Controller	APP
51	70-174	70 SERIES	IO-32	MOD		Clock;Programmable From 1ms To 100s	APP
52	70-171A4	70 SERIES	IO-33	MOD		Multi-Port Communication Controller	APP
53	70-172	70 SERIES	IO-33	MOD		General Purpose Input/Output Controller	APP
54	70-150C301	70 SERIES	PE-10	UNIT		Line Printer;165cps,80 Column Matrix	APP
55	70-150Q55	70 SERIES	PE-10	UNIT		Character Printer;55cps,132 Column Character	APP
56	70-150T40	70 SERIES	PE-10	UNIT		Line Printer	APP
57	70-150T200	70 SERIES	PE-10	UNIT		Line Printer;200 Line/Min 132 Column Matrix	APP
58	70-180TTY	70 SERIES	PE-10	UNIT		KSR Keyboard Printer	APP
59	70-180VTI12	70 SERIES	PE-23	UNIT		CRT Terminal;80 x 24 Character Screen,12 Line	APP
60	70-180VTI	70 SERIES	PE-23	UNIT		CRT Terminal;80x24 Char Screen,Upper Case;Opt U/L Case	APP
61	70-180VTI-U/L	70 SERIES	PE-23	UNIT		CRT Terminal;80 x 24 Character Screen,Upper/Lower Case	APP
62	70-124	70 SERIES	RAM	MOD		Add-In RAM Module,4k Bytes,8 Chips	APP
63	70-121	70 SERIES	ROM	MOD		Add-In ROM,1k Bytes,Ultra-Violet Erasable	APP
64	ASCZ80	ASCZ80	COMP	MODS	MNG	8 Bit Microcomputer System;Uses Zilog Z80 CPU	APS
65	ASC40	ASC40	COMP	MODS		4 Bit Microcomputer System;Uses Intel 4040 MPU	APS
66	ASC80	ASC80	COMP	MODS	MNX	8 Bit Microcomputer System;Uses Intel 8080A MPU	APS
67	ASC80#3	ASC80	CPU	MOD	MNX	Microprocessor Unit Using 8080 MPU	APS
68	ASC80#1	ASC80	IO-20	MOD	MNX	Programmable Communications Terminal Controller	APS
69	ASC80#2	ASC80	IO-20	MOD	MNX	Binary Synchronous Communication Controller	APS
70	ASC80#7	ASC80	IO-30	MOD	MNX	Peripheral Interface Adapter	APS
71	ASC80#6	ASC80	IO-33	MOD	MNX	Input/Output Circuits,1024 Lines, Up To 4096 Expanded	APS
72	ASC80#5	ASC80	RAM	MOD	MNX	8 Bit RAM System	APS
73	ASC80#4	ASC80	ROM	MOD	MNX	Programmable ROM System;256x8 Non-Volatile Storage	APS
74	AMC95/4016	AmZ8000	PE-15	MOD		Microprocessor Evaluation Unit	AUC
75	AMC95/4005/2	AM9080A	COMP	MOD		Monoboard Computer Instruction Cycle 2.00us Multi-Master	AUC
76	AMC95/4005/3	AM9080A	COMP	MOD		Monoboard Computer Instruction Cycle 1.3us Multi Master	AUC
77	SM-810-001	8041A	PE-16	MOD		40 Character Dot Matrix Display Subsystem	BEC
78	SA252	8748	PE-16	MOD		Alphanumeric Planar Gas Discharge Display System	BEC
79	MP1216	LSI-11	IO-30	MOD		16-Ch Differential (User Strappable as 32-Ch SE);0V Prot to 26VDC	BUB
80	MP1216-PGA	LSI-11	IO-30	MOD		16-Ch Differential (User Strappable as 32-Ch SE);S/H Amp;12 Bit A/D Conv	BUB
81	MP1104	LSI-11	IO-40	MOD		4 Channel Analog Output	BUB
82	MP2216	MCB-Z80	IO-41	MOD		16 Or 32 Channel Analog Input	BUB
83	MP2216-AO	MCB-Z80	IO-42	MOD		16 Or 32 Channel Analog Input,2 Channel Analog Output	BUB
84	MP10	MCS80	IO-40	MOD		2 Channel Analog Output For 8080	BUB
85	MP20	MCS80	IO-41	MOD		16 Channel Analog Input For 8080	BUB
86	MP22	MCS80/M6800	IO-41	MOD		16 Channel Microprocessor Compatible Analog Input;±0.05%	BUB
87	MP701	MICROMODULE	IO-33	MOD		16 Channel Isolated Digital Output	BUB
88	MP702	MICROMODULE	IO-33	MOD		32 Channel Isolated Digital Output	BUB
89	MP710	MICROMODULE	IO-33	MOD		Isolated Digital Input	BUB
90	MP710-NS	MICROMODULE	IO-33	MOD		Isolated Digital Input	BUB
91	MP7504	MICROMODULE	IO-40	MOD		Microcomp Analog Output Syst;4 Ch 8 Bit Isolated Analog Output 4 to 20mA	BUB
92	MP7218	MICROMODULE	IO-41	MOD		16 Channel Analog Input For MOTAs MICROMODULES And EXORciser	BUB
93	MP7408	MICROMODULE	IO-41	MOD		8 Channel Diff Analog Input For MOTAs MICROMODULES And EXORciser	BUB
94	MP7408-NS	MICROMODULE	IO-41	MOD		Same As MP7408 Without DC/DC Converter	BUB
95	MP7432	MICROMODULE	IO-41	MOD		32 Channel Diff Analog Input For MOTAs MICROMODULES And EXORciser	BUB
96	MP7432-NS	MICROMODULE	IO-41	MOD		Same As MP7432 Without DC/DC Converter	BUB
97	MP7608	MICROMODULE	IO-41	MOD		Analog Volt Input Micropheripherial For MOTAs MICROMODULES And EXORciser	BUB
98	MP7608-I	MICROMODULE	IO-41	MOD		Analog Cur Input Micropheripherial For MOTAs MICROMODULES And EXORciser	BUB
99	MP7408-AO	MICROMODULE	IO-42	MOD		Same As MP7408 With 2Channel Analog Output	BUB
100	MP7408-NS-AO	MICROMODULE	IO-42	MOD		Same As MP7408-NS With 2 Channel Analog Output	BUB
101	MP7432-AO	MICROMODULE	IO-42	MOD		Same As MP7432 With 2 Channel Analog Output	BUB
102	MP7432-NS-AO	MICROMODULE	IO-42	MOD		Same As MP7432-NS With 2 Channel Analog Output	BUB
103	SDM853	MPC-165	IO-45	MOD		8 or 16 Channel Acquisition System	BUB
104	SDM858	MPC-165	IO-45	MOD		8- or 16- Channel Data Acquisition System Low Level 12-Bit A/D Converter	BUB
105	MP11	M6800	IO-40	MOD		2 Channel Analog Output For 6800	BUB
106	MP7104	M6800	IO-40	MOD		4 Channel Analog Output For Micromodules	BUB
107	MP7105-NS	M6800	IO-40	MOD		4 Channel Analog Output For Micromodules;W/O DC/DC Converter	BUB
108	MP21	M6800	IO-41	MOD		16 Channel Analog Input For 6800	BUB
109	MP7208	M6800	IO-41	MOD		8 Channel Differential Analog Input For Micromodules	BUB
110	MP7209-NS	M6800	IO-41	MOD		8 Channel Differential Analog Input For Micromodules;W/O DC/DC Converter	BUB

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MP7216	M6800	IO-41	MOD		16 Channel Single-Ended Analog Input For Micromodules	BUB
2	MP7217-NS	M6800	IO-41	MOD		16 Channel Single-Ended Analog Input For Micromodules;W/O DC/DC Converter	BUB
3	MP4102	PLS	IO-40	MOD		2 Channel Analog Output For Pro-Log	BUB
4	MP4216	PLS	IO-41	MOD		16 Channel Differential Analog Input For Pro-Log	BUB
5	MP801	SBC80	IO-33	MOD		Microcomp Digital Output Syst;16 Ch Relay Output Syst;Compatible W/SBC80	BUB
6	MP802	SBC80	IO-33	MOD		Microcomp Digital Output Syst;32 Ch Relay Output Syst;Compatible W/SBC80	BUB
7	MP810	SBC80	IO-33	MOD		Isolated Digitial I/O	BUB
8	MP810-NS	SBC80	IO-33	MOD		Isolated Digitial I/O	BUB
9	SDM856	SBC80	IO-41	Chip	BXX	16 Channel Analog Input Subsystem For All Systems	BUB
10	SDM857	SBC80	IO-41	Chip	BXX	16 Channel Analog Input Subsystem For All Systems	BUB
11	MP8418	SBC80	IO-41	MOD		31 Channel Analog I/O;12-Bit Resolution	BUB
12	MP8418-PGA	SBC80	IO-41	MOD		31 Channel Analog Input/Software Programmable Gain/12-Bit Resolution	BUB
13	MP8418-AO	SBC80	IO-42	MOD		31 Channel In,Plus 2 Channel Out Analog I/O;12-Bit Resolution	BUB
14	MP8418-PGA-AO	SBC80	IO-42	MOD		31 Channel In,2 Channel Out Analog I/O;Programmable Gain/12-Bit Resol	BUB
15	MP8304	SBC80/10	IO-40	MOD		4 Channel Analog Output	BUB
16	MP8408	SBC80/10	IO-41	MOD		8 Channel Differential Analog Input	BUB
17	MP8416	SBC80/10	IO-41	MOD		16 Channel Single-Ended Analog Input	BUB
18	MP8608	SBC80/10	IO-41	MOD		8 Channel Differential Analog Input	BUB
19	MP8616	SBC80/10	IO-41	MOD		16 Channel Single-Ended Analog Input	BUB
20	MP8632	SBC80/10	IO-41	MOD		32 Channel Differential Analog Input	BUB
21	MP8632-AO	SBC80/10	IO-41	MOD		32 Channel Differential Analog Input And 2 Ch Analog Output	BUB
22	MP8608-AO	SBC80/10	IO-42	MOD		8 Channel Differential Analog Input And 2 Ch Analog Output	BUB
23	MP8616-AO	SBC80/10	IO-42	MOD		16 Channel Single-Ended Analog Input And 2 Ch Analog Output	BUB
24▼	MP32BG-CG	8080A,8048	IO-45	CHIP	MNX	Data Aquisition,80 pin Quad-in-line Pkg;Includes A/D Conv;Instrum Amp	BUB
25	CSB1	R6500	COMP	MOD		Single Board Computer;2PIA,1VIA	CAC
26	CSB2	R6500	COMP	MOD		Single Board Computer;PIA,VIA,6551	CAC
27	CSB10	R6500	DEV	MOD		PROM PROG(2716,2732) Card Family	CAC
28	DB/65	R6500	DEV	MOD		Debug Board With In-Circuit Emulator	CAC
29	CSB20	R6500	IO-57	MOD		PROM/RAM Card	CAC
30	64KZ	Z2,CS3	RAM	MOD		64k RAM Board;w/Bank Select;Uses 4116 Dynamic RAMS,Tac 150n	CCRO
31	CI-1103	LSI11	RAM	MOD	MNX	Up to 32k Expansion Memory for the LSI11,LSI11/2,PDP1103,Heath-kit H11 uC	CII
32	CI-6800-2	R6500	10-92	MOD		uProcess Memory Expander;Up to 64k Bytes;16k,32k,48k,64k Configs;	CII
33	CI-S100	Z80	RAM	MOD	MNX	Up to 64k Add-In Expansion Memory for the S100 Bus	CII
34	CI-6800	6800	RAM	MOD	MNX	Up to 64k Expansion Memory for the Motorola Exorciser uC	CII
35	CI-8080	8080	RAM	MOD	MNX	Up to 64k Expansion Memory for Intel MDS800,SBC80/10,BLC80/10 uC	CII
36	CSS-1143	CSS-1143	COMP	MOD		Uses Z80 CPU;1k RAM,16k EPROM(Sockets);2MHz Clock Rate;Serial I/O	CLI
37	LCP593	L Series	CPU	MODS	MNX	Basic 3 Card Set Processor Using Intel 8008 Chip	CLI
38	LCP593-1	L Series	CPU	MODS	MNX	Basic 3 Card Set Processor Using Intel 8008-1 Chip	CLI
39	LRC-531-1	L Series	IO-01	MOD	MNX	Real-Time Clock,Programmable Interval Timer	CLI
40	LDI530	L Series	IO-02	MOD	MNX	Device Interrupt/Control; 2Interrupt, 12Control Ckts,12Inp,4Outp Latches	CLI
41	LPI510	L Series	IO-02	MOD	MNX	Priority Interrupt Control; Logic For 8 Priority Interrupt	CLI
42	LMA595	L Series	IO-03	MOD	MNX	16 Bit Memory Address Storage	CLI
43	LTI513	L Series	IO-04	MOD	MNX	Teletypewriter Interface	CLI
44	LCC514	L Series	IO-10	MOD	MNX	Console Card; Controls For Starting, Single-Stepping The Processor	CLI
45	LSI599	L Series	IO-20	MOD	MNX	Serial Interface For Asynchronous,Serial Data Services	CLI
46	LBA512	L Series	IO-31	MOD	MNX	Buss Amplifier; 12 Non Inverting Drivers,	CLI
47	LIO594-1	L Series	IO-33	MOD	MNX	Input/Output Control	CLI
48	LBU	L Series	PE-60	UNIT	MNX	Battery Backup	CLI
49	LP256	L Series	PROM	MOD	MNX	256 Byte PROM, 256X8 Erasable	CLI
50	LPM596	L Series	PROM	MOD	MNX	PROM Card; Memory Address Decoding And Sockets	CLI
51	MAS-842	M Series		MOD			CLI
52	MAU-846	M Series		MOD		Hardware Floating Point Processor	CLI
53	MCP893	M Series	CPU	CdS	MNX	Basic 3 Card Set Processor Using 8080 Chip	CLI
54	ZCP-890	M Series	CPU	CdS	MNX	Basic 2 Card Set Processor Using Z80 Chip	CLI
55	MDS	M Series	DEV	UNIT	MNX	Development System For Software Development And PROM Programming	CLI
56	LRC-531	M Series	IO-01	MOD	MNX	Real-Time Clock,Programmable Interval Timer;Incl 10MHz Crystal Osc	CLI
57	MPI810	M Series	IO-02	MOD	MNX	Priority Interrupt Control;Logic For 8 Priority Interrupt	CLI
58	LEI-517	M Series	IO-20	MOD	MNX	EIA Interface for Serial Data Communications	CLI
59	MSI-838	M Series	IO-21	MOD	MNX	Serial to Parallel Converter Using U Asynchronous Transceiver	CLI
60	LBD534	M Series	IO-31	MOD		Buss Driver;18 Non-Inverting Drivers	CLI
61	LBI-511	M Series	IO-33	MOD	MNX	Buss Port;24 Single-Input Tri-State Gates,3 Groups,8 Bits	CLI
62	LLO-515	M Series	IO-33	MOD	MNX	Latched Output;24 Latched TTL Outputs,3 Groups,8 Bits	CLI
63	LLR532	M Series	IO-33	MOD		Parallel 24-Bit Presetable Latched TTL OUTPUT Card	CLI
64	LLR532I	M Series	IO-33	MOD		Parallel 24-Bit Presetable Latched TTL Output Card	CLI
65	MEE-888	M Series	IO-33	MOD		Interface Bus;Meets IEEE Standard;Contains Two PROMS	CLI
66	MIV-843	M Series	IO-40	MOD		Current Loop Signal Interface for 16 Channels	CLI
67	MDM895	M Series	IO-43	MOD	MNX	Data Buss/Multiplexer	CLI
68	LDD-503	M Series	IO-44	MOD	MNX	Device Address Decoder;4 Bit to 16	CLI
69	LDD-533	M Series	IO-44	MOD		Device Address Decoder;8 Bit to 16 Output Levels,256 Possible Codes	CLI
70	MAD835	M Series	IO-45	MOD		12-Bit A/D Converter And Anolog Multiplexer On A Single Card	CLI
71	MAS-839	M Series	IO-45	MOD		16 Channel Data Acquisition System;12 Bit;3 State	CLI
72	MDA836-1	M Series	IO-45	MOD		12-Bit D/A Subsystem With One Output On A Single Card	CLI
73	MDA836-2	M Series	IO-45	MOD		12-Bit D/A Subsystem With Two Outputs On A Single Card	CLI
74	MIM894	M Series	IO-57	MOD	MNX	Memory And Input/Output Control	CLI
75	MCC814	M Series	IO-92	MOD	MNX	Console Card; Controls For Starting, Single-Stepping The Processor	CLI
76	MVI-844	M Series	IO-92	MOD		4-20mA Voltage to Current Converter;Driven by MDA-836 D/Aconverter	CLI
77	PPS-M	M Series	PE-50	UNIT		PROM Programmer,Uses Interchangeable Personality Module	CLI
78	MPM896	M Series	PROM	MOD		PROM Card;16-Bit Address Decoding And Sockets	CLI
79	MRM898	M Series	RAM	MOD		1024 Byte RAM;1024x16,Memory Address Decoding	CLI
80	MM1-CPU	MM1	CPU	MOD	MNG	Processor Board Incl 8080A CPU,Plug Programmable PROM and RAM	CLI
81	MM1-PPS	MM1	DEV	UNIT		PROM Programming Unit For Programming Intel 1702A or 2708 PROMS	CLI
82	MM1-MMM	MM1	IO-03	MOD		Maintenance Memory Module Used With Programmers Console For Diagnostics	CLI
83	MM1-OPT	MM1	IO-20	MOD		Options Bd Providing Real Time Clock,Serial I/O,32 Bits Parallel I/O	CLI
84	MM1-DIO	MM1	IO-30	MOD		64 Bit Parallel I/O Organized into 8 Bit Ports	CLI
85	MM1-DAS	MM1	IO-43	MOD		12-Bit A/O Converter, S/H,Analog Multiplexer;64 Single Or 32 Diff Inputs	CLI
86	MM1-AOS	MM1	IO-45	MOD		12-Bit D/A System;Up To 4 Latches And Analog Outputs	CLI
87	MM1-MSC	MM1	IO-45	MOD		Provides Up To 4 Full Duplex 20mA Serial Current Loops And FIFO Buffering	CLI
88	MM1-MONS	MM1	IO-92	MOD		Monitor Start Module For The ODT Software System Monitor/Debug Program	CLI
89	MM1-PFD	MM1	IO-92	MOD		Power Fail Detect Module;Monitors AC Line For Missing Cycles	CLI
90	F715	MM1	PE-01	UNIT		Floppy Disk Sys;Single Drive;Compatible With IBM 3740 Diskette Format	CLI
91	F725	MM1	PE-01	UNIT		Floppy Disk Sys;Dual Drive;Compatible With IBM 3740 Diskette Format	CLI
92	P306	MM1	PE-10	UNIT		Serial Impact Printer;ASCII Char Set;80 Char/Line	CLI
93	P306C	MM1	PE-10	UNIT		Serial Impact Printer;ASCII Char Set;80 Char/Line and 130 Char/Line	CLI
94	CGT	MM1	PE-23	UNIT		Interactive Display Terminal;24 Liner,80 Char/Line;64 Char ASCII Set	CLI
95	MRP	MM1	PE-42	UNIT		Combination Reader/Punch;100 Char/Sec Read,75 Char/Sec Punch	CLI
96	PPS-MM1	MM1	PE-50	UNIT		PROM Programmer,Uses Interchangeable Personality Module	CLI
97	MM1-OCON	MM1	PE-61	UNIT		Operators Console Providing 8 Data And 16 Address Switches	CLI
98	MM1-PCON	MM1	PE-61	UNIT		Programmers Console Providing Octal Displays And System Controls	CLI
99	MM1-PROM	MM1	PROM	MOD	MNG	Board With Up to 16k Erasable PROM;Base Addresses Plug Programmable	CLI
100	MM1-DRAM	MM1	RAM	MOD		Board With Up To 16k Dynamic Memory In Increments OF 4k	CLI
101	MM1-NVRAM	MM1	RAM	MOD		Board With Up To 4k Static Non-volatile Memory In 1k Increments	CLI
102	MM1-RAM	MM1	RAM	MOD	MNG	Board With Up to 4k in 1k Increments;Base Addresses Plug Programmable	CLI
103	MM1-FLP	MM1 Series		MOD		Hardware Floating Point Processor	CLI
104	MM1-EEE	MM1 Series	IO-33	MOD		Interface Bus;Meets IEEE Standard;Contains Two	CLI
105	A801	M800 Series	IO-02	MOD		Series Priority Interrupt Control;Logic For 8 PI Requests	CLI
106	A802	M800 Series	IO-02	MOD		Device Interrupt Control	CLI
107	A808	M800 Series	IO-04	MOD		Standard Industry I/O;For Teletype Writer Interface	CLI
108	A810	M800 Series	IO-20	MOD		Serial And Communications Interface	CLI
109	A807	M800 Series	IO-31	MOD		Bus Amplifier;12 Non-Inverting Drivers	CLI
110	A805	M800 Series	IO-33	MOD		Parallel Input;24 Single-Input Gates In 3 Groups Of 8 Each	CLI

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	A806	M800 Series	IO-33	MOD		Parallel Output;24 Latched TTL Outputs In 3 Groups Of 8 Bit Each	CLI
2	A812	M800 Series	IO-33	MOD		Opto Isolated 220V Input/Output	CLI
3	A814	M800 Series	IO-40	MOD		12 Bit Digital To Analog Converter,W/Selectable Voltage Outputs	CLI
4	A813	M800 Series	IO-41	MOD		12 Bit Analog To Digital Converter;40us Conversion Time	CLI
5	A803	M800 Series	PROM	MOD		Programmable ROM;Mem/Address Decoding In 512 Byte Increments	CLI
6	40-000	IMC40	CPU	MOD		Uses C4040 CPU;Inst Cycle Time 10.8us;Control Gating 12V HI-NIL	COM
7	40-001	IMC40	CPU	MOD		Uses C4040 CPU;Inst Cycle Time 10.8us;Control Gating 15V HI-NIL	COM
8	40-002	IMC40	CPU	MOD		Uses C4040 CPU;Inst Cycle Time 10us;Control Gating 12V HI-NIL	COM
9	40-003	IMC40	CPU	MOD		Uses C4040 CPU;Inst Cycle Time 10us;Control Gating 15V HI-NIL	COM
10	40-004	IMC40	CPU	MOD		Uses C4040 CPU;Inst Cycle Time 8.0us;Control Gating 12V HI-NIL	COM
11	40-005	IMC40	CPU	MOD		Uses C4040 CPU;Inst Cycle Time 8.0us;Control Gating 15V HI-NIL	COM
12	40-700SER	IMC40	DEV	UNIT		Syst Programming Equip(4);700,701(PTR),702(TTY),703(UV Erase)	COM
13	40-750SER	IMC40	DEV	UNIT		Syst Analyzer Equip(3);750,751,752	COM
14	40-100SER	IMC40	IO-01	MOD		Program Storage Modules (5);100,101,102.103,104	COM
15	40-200SER	IMC40	IO-33	MOD		Data Input Interface Mod(5);200,201,202,203,204	COM
16	40-300SER	IMC40	IO-33	MOD		Data Output Interface Mod(9);300,301,302,303,304,305,306,307,308	COM
17	40-450SER	IMC40	IO-40	MOD		Analog Output Modules(2);450,451	COM
18	40-400SER	IMC40	IO-41	MOD		Analog Input Modules(6);400,401,402,403,404,405	COM
19	40-050SER	IMC40	IO-55	MOD		Data Storage Modules(9);050,051,052,053,054,055,056,057,058	COM
20	40-500SER	IMC40	IO-92	MOD		Special Control And Interface Mod(6);500,501,502,503,504,505	COM
21	40-600SER	IMC40	PE-23	UNIT		Peripheral Equip,Display,Keyboard(9);600,601,602,603,604,605,606,607,608	COM
22	D/7A-W		IO-33	MOD		7-Channel uComputer Anolog Interface;8-Bit Parallel I/O Port;Already Assy	CRO
23	CS3/2	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;128k RAM;2 Ser.I/O Port;2 8inch Flpys	CRO
24	CS3/2-002	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;128k RAM;1 CRT I/O Port;4 8inch Flpys	CRO
25	CS3/3	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;192k RAM;3 Ser. I/O Port;2 8inch Flpys	CRO
26	CS3/3-002	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;192k RAM;1 CRT I/O Port;4 8inch Flpys	CRO
27	CS3/4	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;192k RAM;4 Ser. I/O Port;2 8inch Flpys	CRO
28	CS3/4-002	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;192k RAM;1 CRT I/O Port;4 8inch Flpys	CRO
29	CS3/5	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;256k RAM;5 Ser. I/O Port;2 8inch Flpys	CRO
30	CS3/5-002	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;256k RAM; 1 CRT I/O Port;4 8inch Flpys	CRO
31	CS3/6	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;256k RAM;6 Ser. I/O Port;2 8inch Flpys	CRO
32	CS3/6-002	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;256k RAM;1 CRT I/O Port;4 8inch Flpys	CRO
33	CS3/7-002	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;320k RAM;1 CRT I/O Port;4 8inch Flpys	CRO
34	CS-3	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;32k RAM;1 Ser. I/O Port;2 8inch Flpys	CRO
35	CS-3-001	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;32k RAM;1 Ser.I/O Port;2 8inch Flpys	CRO
36	CS-3-001-002	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;32k RAM;1 CRT I/O Port;4 8inch Flpys	CRO
37	CS-3-002	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;32k RAM;1 CRT I/O Port;4 8inch Flpys	CRO
38	CS-3-004	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;64k RAM;1 Ser. I/O Port;2 8inch Flpys	CRO
39	CS-3-004-002	SYSTEMTHREE	COMP	UNIT		8 Bit UCOMP;4MHz Z80;1k ROM;64k RAM;1 CRT I/O Port;4 8inch Flpys	CRO
40	SCC-W	Z2	COMP	MOD		8 Bit Single Card Computer,Assembled:Uses Z80A 4.0MHz CPU	CRO
41	CS2	Z2	COMP	UNIT		8 Bit Microcomputer,Uses 4MHz Z80 CPU,W/2/4 5in Disk Drives	CRO
42	CS2/2	Z2	COMP	UNIT		Z80A 4MHz;1k ROM;128k RAM;2 User;PT I/O;2 5inch Flpys;S-100 Bus;	CRO
43	CS2/4	Z2	COMP	UNIT		Z80A 4MHz;1k ROM;192k RAM;3 User;PT I/O;2 5inch Flpys;S-100 Bus;	CRO
44	CS2/5	Z2	COMP	UNIT		Z80A 4MHz;1k ROM;256k RAM;5 User;PT I/O;2 5inch Flpys;S-100 Bus;	CRO
45	CS2/6	Z2	COMP	UNIT		Z80A 4MHz;1k ROM;256k RAM;5 User;PT I/O;2 5inch Flpys;S-100 Bus;	CRO
46	CS2/7	Z2	COMP	UNIT		Z80A 4MHz;1k ROM;320k RAM;7 User;PT I/O;2 5inch Flpys;S-100 Bus;	CRO
47	CS-2	Z2	COMP	UNIT		Z80A 4MHz;1k ROM;64k RAM;1 User; PT I/O; 2 5inch Flpys;S-100Bus;	CRO
48	Z2-H	Z2	COMP	UNIT		Z80A (4MHz;1k ROM)64k RAM; 2 5in Floppies; 11 MByte Hard Disk; CRT and PT	CRO
49	Z2D	Z2	COMP	UNIT		8 Bit Microcomputer,Uses 4MHz Z80 CPU,W/184k Bytes Disk Memory	CRO
50	ZPU-W	Z2	CPU	MOD		8 Bit CPU Card,Assembled:Uses Z80A 4.0MHz CPU,S-100 Bus Compatible	CRO
51	Z2-W	Z2	DEV	PE-61		21 Slot MotherBoard;ZPU Card S-100 Bus	CRO
52	Z2-WX	Z2	DEV	PE-61		21 Slot MotherBoard S-100 Bus	CRO
53	Z2D-W	Z2	DEV	PE-61		21 Slot MotherBoard;ZPU Card;1k ROM;1 CRT PT;1 5inch Floppy Disk	CRO
54	CGI-W	Z2	GAME	MOD		TV DAZZLER Assembled:2 Cards Plug into Microcomp Syst	CRO
55	JS-1W	Z2	GAME	UNIT		Video Game Joystick Console W/Speaker,Assembled,S100 Compat	CRO
56	4FDC-W	Z2	IO-07	MOD		Disc Controller and IO Interface,Assembled,Up to 4 Drives 8 in	CRO
57	Z2-RPW	Z2	IO-07	MODS		Kit Converts Z-2 System to Z-2D System;All Hardware Necessary	CRO
58	PRI	Z2	IO-08	MOD		Printer Interface Assemb,2 IOs,One for 3779,3703,Other for 3355 Printer	CRO
59	8PIO-K	Z2	IO-30	MOD		8 Port I/O Multichannel Microcomp Parallel Interface,Kit	CRO
60	8PIO-W	Z2	IO-30	MOD		8 Port I/O Multichannel Microcomp Parallel Interface,Assembled	CRO
61	TRT-W	Z2	IO-33	MOD		TU-ART Digital Interface,Assembled,Uses UART 5501,Ser/Par IO Ports	CRO
62	MUB	Z2	IO-92	MOD		Multi-User BASIC Hardware Pkg:Includes Three 16KZ Mem Cards	CRO
63	Z2D-FDD	Z2	PE-01	MOD		Additional Disk Drive for Z2-D Systems	CRO
64	PFD-W	Z2	PE-01	UNIT		Dual 8in Floppy Disk Drive,Assembled,W/PS,W/O Controller	CRO
65	WFD	Z2	PE-01	UNIT		5in Single Disk Drive Assembled W/O Controller	CRO
66	HDD-11	Z2	PE-02	MODS		11 MByte Solid Disk System;Transfer Rate 5.6 MBits/Sec;1 Drive	CRO
67	HDD-22	Z2	PE-02	MODS		22 M Byte Solid Disk System;Transfer Rate 5.6 MBits/Sec;2 Drives	CRO
68	3703	Z2	PE-10	UNIT		Dot Matrix Printer:180 Char/Sec;18in Platen,132 Columns	CRO
69	3779	Z2	PE-10	UNIT		Dot Matrix Printer:60 Char/Sec;12in Platen,Up to 132 Ch/Line	CRO
70	16KPR-W	Z2	PROM	MOD		16k PROM,Assembled W/Add Anticipation/Bank Sel,Uses 2708 PROM	CRO
71	32KBS-W	Z2	PROM	MOD		32k BYTESAVER Mem Bd Assembled W/2716 PROM Programmer,tac 450ns	CRO
72	4KZ-W	Z2	RAM	MOD		4k Static RAM,Assembled W/Add Anticipation/Bank Sel,Uses 21L02,tac 450ns	CRO
73	16KZ-W	Z2	RAM	MOD		16k RAM,Assembled W/Bank Select,Uses 4050-2RAM,tac 200ns	CRO
74	4PIO-W	Z2,CS3	IO-30	MOD		4 Parallel 8 Bit I/O Ports, Isolated,Assn and Tested	CRO
75	DPLUS7A-W	Z2,CS3	IO-45	MOD		D/A A/D Conversion;7 Channel;8Bit resol -2.56 to 2.54V;5.5us/con;Kit	CRO
76	8KBS-W	Z2,CS3	PROM	MOD		8k Bytesaver II,w/2708 Programming Capability;Tac 450ns Kit	CRO
77	KD11-HA	LSI11	CPU	MOD		16-Bit LSI11/2 W/Pwr Fail,Auto Restort,LSI11 Bus IF And Vector Interrupt	DEC
78	KD11-GC	LSI11	CPU	MODS		LSI-11/2 CPU as KD11-HA Plus LSI-11 Multi. Opt. MOD(NXV11-AA)8k Byte-RAM	DEC
79	KD11-GD	LSI11	CPU	MODS		KD11-GC Plus 32k Byte RAM Total RAM 64k Bytes	DEC
80	KD11-GF	LSI11	CPU	MODS		LSI-11/2 CPU as KD11-HA Plus LSI-11 Multi. Opt. Mod(MXV11-AC)32k-Byte RAM	DEC
81	KD11-HB	LSI11	CPU	MODS		KD11-HA CPU Plus 8k x 16 RAM	DEC
82	KD11-HC	LSI11	CPU	MODS		KD11-HA CPU Plus 16k x 16 RAM	DEC
83	KD11-HD	LSI11	CPU	MODS		LSI 11/2 KD11-HA CPU plus 32k x 16 RAM	DEC
84	KD11-HF	LSI11	CPU	MODS		KD11-HA CPU plus 4k x 16 RAM	DEC
85	KD11-HU	LSI11	CPU	MODS		LSI 11/2 KD11-HA CPU plus 256 x 16 RAM;Requires 4k x 16 RAM;Takes 4k x 16	DEC
86	KDF11-GD	LSI11	CPU	MODS		LSI-11/23 CPU with Extended Fixed-Point Inst. Set Add to 64k-Bytes	DEC
87	KDF11-HD	LSI11	CPU	MODS		LSI11/23 CPU;64k Byte RAM;Bus I/O;Vector Interrupt;2 Double Width Bds	DEC
88	KDF11-HF	LSI11	CPU	MODS		KDF11-HD plus 64k Byte RAM(128k Byte total);3 Double Width Bds	DEC
89	KDF11-HH	LSI11	CPU	MODS		KDF11-HF plus 64k Byte RAM(192k Byte total);4 Double Width Bds	DEC
90	KDF11-HK	LSI11	CPU	MODS		KDF11-HF plus 128k Byte RAM(256k Byte total);5 Double Width Bds	DEC
91	KDF11-RE	LSI11	CPU	MODS		LSI-11/23 CPU with Extended Fixed-Point Inst Set and On-Board Memory	DEC
92	KDF11-RG	LSI11	CPU	MODS		KDF11-RE Plus 64k Byte RAM Total RAM 160k Byte	DEC
93	KDF11-RJ	LSI11	CPU	MODS		KDF11-RE Plus 128k Byte RAM Total RAM 224k Byte	DEC
94	KDF11-SE	LSI11	CPU	MODS		LSI-11/23 CPU with Extended Fixed-Point Inst Set and On-Board Memory Capa	DEC
95	KDF11-SG	LSI11	CPU	MODS		KD11-SE Plus 64k Byte RAM Total RAM 160k Byte	DEC
96	KDF11-SJ	LSI11	CPU	MODS		KD11-SE Plus 128k Byte RAM Total RAM 224k Byte	DEC
97	PDP11/03LH	LSI11	DEV	MOD		KD11-F with Power Supply;Rack-Mountable	DEC
98	SR-VXLLB-BA,LA	LSI11	DEV	MOD	MXX	LSI-11 CPU;64k Byte MOS RAM;Two 5.2M Byte Cont Disk Dr and Real Time Sys	DEC
99	SR-VXLLB-BD,LD	LSI11	DEV	MOD	MXX	SR-VLLB-BA;LA 230V Versions	DEC
100	SR-VXSSB-BA,LA	LSI11	DEV	MOD	MXX	LS-11 CPU;64k-Byte MOS RAM Dual Drive Floppy Disk with 1.0m Byte Capacity	DEC
101	SR-VXSSB-BD,LD	LSI11	DEV	MOD	MXX	SRΩVXSSB-BA,LA 230V Versions	DEC
102	KUV11-UH	LSI11	IO-01	MOD		Writable Control Store Field Upgrade Kit;KD11-F W/O Memory;Incl Cable	DEC
103	BC20N-05	LSI11	IO-02	MOD		Nullmodem Cable Used to Connect DLV11-J and MXV11 Directly	DEC
104	BC21B-50	LSI11	IO-02	MOD		Input/Output Cable With DLV11-J and MXV11	DEC
105	BCV1A	LSI11	IO-02	MOD		Buss Expansion Modules And Jumper Cables	DEC
106	BCV1V-25	LSI11	IO-02	MOD		Jumper Cable Assy to Expand Backplane from Second to Third Backplane	DEC
107	DRV11B	LSI11	IO-03	MOD		DMA Interupter	DEC
108▼	RKV11D	LSI11	IO-07	MOD		Disk Drive Controller;Use Up to 8 RK05-J Disk Drives Daisy-Chnd on DR Bus	DEC
109▼	VK170CA	LSI11	IO-09	MOD		Serial Video Module;Displays 80 Characters Per Line and 25 Lines	DEC
110	DLV11	LSI11	IO-20	MOD		Asynchronous Serial Line Interface;50 To 9600 Baud	DEC

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	DLV11-E	LSI11	IO-20	MOD		EIA/CCITT Serial Line Modem Controller W/Programmable Speed	DEC
2	DLV11-F	LSI11	IO-20	MOD		Ser If;Op Isolated 20mA Loop Or RS232C Levels;50-19.2K Band Rate	DEC
3	DLV11-J	LSI11	IO-20	MOD		4-Line Serial Interface Unit;EIA Interface Levels,Comp DLV11,F	DEC
4	DLV11-KA	LSI11	IO-20	MOD		EIA to 20mA in Line Converter Plus 110 Baud Support;Use W/DLV11-J	DEC
5	DUV11-DA	LSI11	IO-20	MOD		Synchronous Line Interface,9600 Baud,Interfaces to Bell 200 Modems	DEC
6	DZV11-B	LSI11	IO-20	MOD		EIA/CCITT 4-Line Asynchronous Multiplexor;Programmable	DEC
7▼	DUV11	LSI11	IO-20	MODD		Line Interface;Buffered,Prog Controlled,Single Line Comm,Interface Dev	DEC
8	KWV11-A	LSI11	IO-32	MOD		Programmable Crystal Clock with Freq from 100Hz-1MHz;60 Cycle,Ext Inp	DEC
9	DRV11	LSI11	IO-33	MOD		General Purpose Parallel Line Interface;Stores,Transmits 8 Or 16 Bits	DEC
10▼	DRV11J	LSI11	IO-33	MOD		High Density Parallel Interface;64 I/O Lines;Bit Interrupt up to 16 Lines	DEC
11	IBV11-A	LSI11	IO-33	MOD		Instrument Interface;Conforms to IEEE Standard 488-1975	DEC
12	AAV11-A	LSI11	IO-40	MOD		12 Bit,4 Channel,D/A Converter;Output Ranges ±2.56V,±5.12V,±10.24V	DEC
13	ADV11-A	LSI11	IO-41	MOD		12 Bit,16 Channel,Single-Ended A/D Converter;Input Ranges ±5.12V,0-10.24V	DEC
14▼	DZV11	LSI11	IO-43	MOD		Async Multiplexer;Connects w/up to 4 Async Serial Data Comm. Channels	DEC
15	MMV11-A	LSI11	IO-55	MOD		4k x 16 Core Memory	DEC
16	MRV11-BA	LSI11	IO-55	MOD		UV PROM/RAM Memory Unit,Up to 4kx16 Bit PROM Memory in 1k Increments	DEC
17	MXV11-A2	LSI11	IO-57	MOD		Bootstrap PROMS for MXV11-AA,-AC with Support for TU58	DEC
18	MXV11-AA	LSI11	IO-57	MOD		Multi-func Mod;ROM/RAM/Ser I/O and Xtal Cl(60Hz);W/8KByte RAM	DEC
19	MXV11-AC	LSI11	IO-57	MOD		Multi-func Mod;ROM/RAM/Ser I/O and Xtal Cl(60Hz);W/32KByte RAM	DEC
20	KEF11-AA	LSI11	IO-90	Chip		Floating Point Inst Set Option for LSI-11/23 CPU 40 Pin Microde Chip	DEC
21	KEV11	LSI11	IO-90	Chip		Fixed,Floating Pt Instr Set Extension for LSC11/2; 40 Pin Chip	DEC
22▼	BDV11-0	LSI11	IO-92	MOD		Dianostic,Bootstrap,Terminater:User Selectable Diagnostic and Boot Pgms	DEC
23	DDV11-B	LSI11	IO-92	MOD		Prewired Backplane for One CPU and 16 I/O and/or Memory Modules	DEC
24	H9270	LSI11	IO-92	MOD		Wired Backplane/Card Guide Assy for One CPU and 6 I/O and/or Mem Modules	DEC
25	H9273-A	LSI11	IO-92	MOD		Nine Slot Backplane/Card Guide Ass/ Required for RLV11 Controller	DEC
26	H9281-BA	LSI11	IO-92	MOD		Housing Assembly for 4 LSI-11/2 Mods with Card Guides,H9281-AA backplane	DEC
27	H9281-BB	LSI11	IO-92	MOD		Housing Assembly for 8 LSI-11/2 Mods with Card Guides,H9281-AA backplane	DEC
28	H9281-BC	LSI11	IO-92	MOD		Housing Assembly for 12 LSI-11/2 Mods with Card Guides,H9281-AA backplane	DEC
29▼	KPV11C	LSI11	IO-92	MOD		See KPV11-C;w/22052 Bus Terminations	DEC
30	TEV11	LSI11	IO-92	MOD		120Ω Termination	DEC
31	RXV21-BA	LSI11	PE-01	UNIT		Dual Drive Double Density Floppy Disk With Interface,1024k Byte Capacity	DEC
32	RL01-AK	LSI11	PE-02	UNIT		Add on 5.2MByte Top Loading Removable Cartridge Disk Drive	DEC
33	RLV11-AK	LSI11	PE-02	UNIT		5.2 MByte Top Loading Subsys(Removable Cart)for all 11/03 LSI-11 Systems	DEC
34	TU58AB	LSI11	PE-04	UNIT		Single Drive Tape-Cartridge Subsystem W/256KByte Capacity	DEC
35	TU58BB	LSI11	PE-04	UNIT		Dual Drive Tape-Cartridge Subsystem W/512kByte Capacity	DEC
36	LA38-GA	LSI11	PE-24	UNIT		Upper/Lower Case Table Top DECwriter 1V Keyboard Printer with Numeric PAD	DEC
37	PB11-AQ	LSI11	PE-50	UNIT		Same as PB11-AY Includes Class C Software on RL01 Disk	DEC
38	PB11-AY	LSI11	PE-50	UNIT		Desk Top PROM Programmer with Class C Software on RX01 Disk	DEC
39	PB11K-AA	LSI11	PE-50	UNIT		Adapter for 825129,825131 Fusible Link PROMS	DEC
40	PB11K-AB	LSI11	PE-50	UNIT		Adapter for 2708 UV PROMS	DEC
41	PB11K-AC	LSI11	PE-50	UNIT		Adapter for 825181,825191 Fusible Link PROMS	DEC
42	PB11K-AD	LSI11	PE-50	UNIT		Adapter For 2716,2732 UV PROMS	DEC
43	BA11-VA	LSI11	PE-60	UNIT		Form Factor PKG Providing Space/Pwr For 4 LSI11/2 or LSI11/23 Family Mods	DEC
44	H780-H	LSI11	PE-60	UNIT		Power Supply for LSI11/H9270 Configurations;With Slave Console	DEC
45	H780-J	LSI11	PE-60	UNIT		Power Supply for LSI11/H9270 Configurations;230V;With Master Console	DEC
46	MSV11-DC	LSI11	RAM	MOD	MXX	16k x 16 RAM;Acc Time 250ns;Cyc Time 545ns;Refr Time 575ns	DEC
47	MSV11-DD	LSI11	RAM	MOD	MXX	32k x 16 RAM;Acc Time 250ns;Cyc Time 545ns;Refr Time 575ns	DEC
48	MSV11-ED	LSI11	RAM	MOD	MXX	32k x 18 RAM with Parity;Acc Time 250ns;Cyc Time 545ns;Refr Time 575ns	DEC
49	MRV11-AA	LSI11	ROM	MOD		4k x 16 PROM/ROM	DEC
50	MRV11-C	LSI11	ROM	MOD		High Dens ROM Mod For LSI11 Bus;8,16,32,or64kByte ROM;18-Bit Addressing	DEC
51	MP200	Micronova	Comp	MOD	BXX	16-Bit Microcomp Inst Time 0.8ns Add,Available as a board,package System	DGC
52	MP100#2	MICRONOVA	uCT	Chip	MNG	16-Bit Microcomp Available As A Box or Package System;Uses mN602 CPU	DGC
53	MBC/1	MICRONOVA	COMP	MOD		16 Bit Board Computer On A 7.5 x 9.5	DGC
54	MP100#1	MICRONOVA	COMP	MOD	MNG	16-Bit Microcomp Available As A Chip,Uses mN602 CPU	DGC
55	mN601	MICRONOVA	CPU	Chip	MNG	16 Bit CPU;4 Gen Purpose Accumulators;1 Stack Pointer,1 Frame Pointer	DGC
56	mN602	MICRONOVA	CPU	Chip	MNG	16-Bit Microprocessor,128kB Mem Capacity,64kB of RAM/PROM/EPROM Support	DGC
57	9040	MICRONOVA	DEV	UNIT	MNG	Fully Packaged Syst For Software Development And Debugging	DGC
58	9041	MICRONOVA	DEV	UNIT	MNG	Fully Packaged Syst For Software Development And Debugging	DGC
59	9042	MICRONOVA	DEV	UNIT	MNG	Fully Packaged Syst For Software Development And Debugging	DGC
60	mN613	MICRONOVA	IO-02	Chip	MNG	I/O Device Controller,Decodes 16.6MHz Data Stream from mN602 mProcessor	DGC
61	mN506	MICRONOVA	IO-03	Chip	BTX	Quad Sense Amplifier(4 Per Mem Array);14 Pin Bipolar	DGC
62	mN633	MICRONOVA	IO-03	Chip	BTX	Octal Memory Address Driver(2 Per Mem Array);20 Pin Bipolar	DGC
63	4220-A	MICRONOVA	IO-06	MOD		Paper Tape Reader Controller Board	DGC
64	4222	MICRONOVA	IO-08	MOD		Digital I/O Interface Board	DGC
65	4207	MICRONOVA	IO-20	MOD		Asynchronous Interface Board	DGC
66	4225	MICRONOVA	IO-20	MOD		Communication Controller	DGC
67	4226	MICRONOVA	IO-20	MOD		Synchronous Interface Board	DGC
68	4227	MICRONOVA	IO-20	MOD		4-Line Asynchronous Interface Board	DGC
69	4228	MICRONOVA	IO-20	MOD		CRC Board	DGC
70	mN629	MICRONOVA	IO-21	Chip	BTX	CPU I/O Transceiver(1 Per CPU);20 Pin Bipolar	DGC
71	mN634	MICRONOVA	IO-21	Chip	BTX	Octal Memory Bus Transceivers;2 Per CPU;20 Pin Bipolar	DGC
72	mN636	MICRONOVA	IO-21	Chip	BTX	I/O Transceiver(1 Per IOC);20 Pin Bipolar	DGC
73	mN638	MICRONOVA	IO-32	Chip	BTX	2 Phase Clock Driver;TTL Input To MOS Output To Drive mN606 RAM	DGC
74	mN640	MICRONOVA	IO-32	Chip	BTX	2 Phase Clock Driver;TTL Input To MOS Output To Drive Between CPU,mN629	DGC
75	4220-B	MICRONOVA	IO-32	MOD		Real Time Clock	DGC
76	mN603	MICRONOVA	IO-33	Chip	MNX	I/O Controller(1 Per Interface);40 Pin NMOS	DGC
77	4300-M	MICRONOVA	IO-40			DG/DAC Controller Board	DGC
78	4221	MICRONOVA	IO-40	MOD		Line Printer Controller Board	DGC
79	4223	MICRONOVA	IO-40	MOD		A/D Converter Board	DGC
80	4224	MICRONOVA	IO-41	MOD		D/A Converter Board	DGC
81	8567	MICRONOVA	PROM	MOD		1k Byte,512 Word PROM Memory Board	DGC
82	8568	MICRONOVA	PROM	MOD		2k Byte,1k Word PROM Memory Board	DGC
83	8569	MICRONOVA	PROM	MOD		4k Byte,2k Word PROM Memory Board	DGC
84	8570	MICRONOVA	PROM	MOD		8k Byte,4k Word PROM Memory Board	DGC
85	mN606	MICRONOVA	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 160ns	DGC
86	8572	MICRONOVA	RAM	MOD		8k Byte,4k Word RAM Memory Board	DGC
87	8573	MICRONOVA	RAM	MOD		16k Byte,8k Word RAM Memory Board	DGC
88	8562	8562	COMP	MOD	MNG	16 Bit Microcomputer On One 7.5 in x 9.5 in Card;2k RAM	DGC
89	8563	8563	COMP	MOD	MNG	16 Bit Microcomputer On One 7.5 in x 9.5 in Card;4k RAM	DGC
90	TDGZ80-3BD	TDGZ80SYS	COMP	MODS		3 Board Set On Mother Board:Z80 CPU,I/O Bd;TV And Tape Interface Board	DIG
91	TDGZ80-4BD	TDGZ80SYS	COMP	MODS		4 Board Set Version Of Z80-3DB With One 8k Mem Board For Total Of 10k	DIG
92	TDG-MAIN1	TDGZ80SYS	COMP	UNIT		Mainframe;Z80 CPU;Aud Cass and 64x16 Vid Intfce;4x8 I/O;PROM;12A Pwr Sup	DIG
93	TDG-MAIN2	TDGZ80SYS	COMP	UNIT		MAIN1 Plus 8k Memory for Total 18k Memory	DIG
94	TDG-MAIN3	TDGZ80SYS	COMP	UNIT		MAIN1;34k Total Memory	DIG
95	TDG-MAIN4	TDGZ80SYS	COMP	UNIT		MAIN1;50k Total Memory	DIG
96	TDG-MAIN5	TDGZ80SYS	COMP	UNIT		MAIN1;64k Total Memory	DIG
97	TDG-MASTER1	TDGZ80SYS	COMP	UNIT		8 Bit Sys W/9 inch CRT,Detached Key Bd,Vid and Aud Interface,Dig Cass,18k	DIG
98	TDG-MASTER2	TDGZ80SYS	COMP	UNIT		8 Bit Sys W/9 inch CRT,Detached Key Bd,Vid and Aud Interface,Dig Cass,34k	DIG
99	TDG-MASTER3	TDGZ80SYS	COMP	UNIT		8 Bit Sys W/9 inch CRT,Detach Key Bd,Vid and Aud Interface,Mini-Disk,18k	DIG
100	TDG-MASTER4	TDGZ80SYS	COMP	UNIT		8 Bit Sys W/9 inch CRT,Detach Key Bd,Vid and Aud Interface,Mini-Disk,34k	DIG
101	TDG-SYS1A	TDGZ80SYS	COMP	UNIT		Includes MAIN2,KEY1,MON9 and Z80-OPSYS	DIG
102	TDG-SYS2A	TDGZ80SYS	COMP	UNIT		Includes MAIN2,KEY1,MON9,PHI2 and PHIMON	DIG
103	TDG-SYS3A	TDGZ80SYS	COMP	UNIT		Includes MAIN2,KEY1,MON9,DSMCOMP2 and DISKMON	DIG
104	TDG-SYS4A	TDGZ80SYS	COMP	UNIT		Includes MAIN3,KEY1,MON9,DSMCOMP2,PT96 and DISKMON	DIG
105	TDG-SYS6A	TDGZ80SYS	COMP	UNIT		Includes MAIN5,KEY1,MON9,PHI2 and PHIMON	DIG
106	TDG-SYSHAM	TDGZ80SYS	COMP	UNIT		Amateur Radio Sys;Includes MAIN2,IOF,HAM1,KEY1,MAXIBASIC and ASSM2	DIG
107	TDGZ80SYS1	TDGZ80SYS	COMP	UNIT		Complete Packaged 4 Board System Including 12 Amp Power Supply	DIG
108	TDGZ80SYS2	TDGZ80SYS	COMP	UNIT		Z80SYS1 With Additional 8k RAM Board For Total Of 18k Memory	DIG
109	TDGZ80SYS3	TDGZ80SYS	COMP	UNIT		Z80SYS2 With Keyboard,9 Inch Monitor,Cassette Drive And Interface Unit	DIG
110	TDGZ80SYS4	TDGZ80SYS	COMP	UNIT		Z80SYS3 With 96 Column Printer, Second I/O Card For Added 16 Ports of I/O	DIG

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	TDGZ80SYS5	TDGZ80SYS	COMP	UNIT		Dual Disk Based 18k Sys Incl Keyboard,Printer,64 Char Video Monitor	DIG
2	TDGZ80SYS6	TDGZ80SYS	COMP	UNIT		Combined Disk-Tape Sys With Z80SYS5 Peripherals Incl Tape Interface Units	DIG
3	TDGZ80SYS7	TDGZ80SYS	COMP	UNIT		Z80SYS6 System With Dual Disk Drive Capabilities	DIG
4	TDG-Z80CPU	TDGZ80SYS	CPU	MOD		8-Bit Processor;Z80CPU,2k Bytes RAM,256 Bytes of 1702A EPROM;2 DMA Chan	DIG
5	TDG-SYS5A	TDGZ80SYS	DEV	UNIT		Includes MAIN3,KEY1,MON9,PHI2,DSSCOMP2,PT96 and DISKMON	DIG
6	TDG-PHIF	TDGZ80SYS	IO-05	MOD		Interface Card For Up To 4 Cassette Drives Including Drive Power	DIG
7	TDG-DSMINT1	TDGZ80SYS	IO-07	MOD		Mini-Disk Interface Card For Up To Four Disk Driver	DIG
8	TDG-DSSINT1	TDGZ80SYS	IO-07	MOD		Standard Disk Interface Card For Up To Four Disk Driver	DIG
9	TDG-GRAPH64	TDGZ80SYS	IO-09	MOD		64x64 Color Graphics Interface Card	DIG
10	TDG-TVC64	TDGZ80SYS	IO-09	MOD		TV and Tape Interface;16 Lines by 64 Char Display;100 Char/Sec Tape Rate	DIG
11	TDG-TVC64UPG	TDGZ80SYS	IO-09	MOD		Upgrade Kit To Convert From TVCF To TVC64	DIG
12	TDG-TVCF	TDGZ80SYS	IO-09	MOD		TV and Tape Interface;16 Lines by 32 Char Display;100 Char/Sec Tape Rate	DIG
13	TDG-TVR96	TDGZ80SYS	IO-09	MOD		96 Char Video Interface;Port Driven;2264 Char,128 ASCII;Requires Monitor	DIG
14	TDG-COMM1	TDGZ80SYS	IO-20	MOD		Single Chan Of Comm Interface In Kit Form	DIG
15	TDG-COMM4	TDGZ80SYS	IO-20	MOD		Four Chan Comm Interface;Sync And Async Modes,Full Duplex	DIG
16	TDG-HAM1	TDGZ80SYS	IO-21	MOD		Amateur Radio Operator Interface Board;Three Output,Two Input Ports	DIG
17	TDG-IOF	TDGZ80SYS	IO-33	MOD		Four 8 Bit Input/Four 8 Bit Output Latching Ports;16 Bit Addressing;TTL	DIG
18	TDG-DSMPWR2	TDGZ80SYS	IO-92	MOD		Power Supply For 2 Mini-Floppy Drivers	DIG
19	TDG-DSSPWR2	TDGZ80SYS	IO-92	MOD		Power Supply For 2 Standard Driver	DIG
20	TDG-VOTRAX1	TDGZ80SYS	IO-92	MOD		Voice Synthesizer;64 Combinable Human Sounds	DIG
21	TDG-DSSDRIN1	TDGZ80SYS	PE-01	MOD		Innovex Standard 8 Inch Floppy Drive	DIG
22	TDG-DSSDRPT1	TDGZ80SYS	PE-01	MOD		Pertec Standard 8 Inch Floppy Drive	DIG
23	TDG-DSSDRSH1	TDGZ80SYS	PE-01	MOD		Shugart Standard 8 Inch Floppy Drive	DIG
24	TDG-DSMDRSH1	TDGZ80SYS	PE-01	UNIT		Shugart Mini-Floppy 5 Inch Drive	DIG
25	TDG-DSMCOMP1	TDGZ80SYS	PE-02	UNIT		Complete Packaged Single Drive Mini Disk Subsystem	DIG
26	TDG-DSMCOMP2	TDGZ80SYS	PE-02	UNIT		Complete Packaged Dual Drive Mini Disk Subsystem	DIG
27	TDG-DSMCOMP3	TDGZ80SYS	PE-02	UNIT		Complete Packaged Three Drive Mini Disk Subsystem	DIG
28	TDG-DSMCOMP4	TDGZ80SYS	PE-02	UNIT		Complete Packaged Four Drive Mini Disk Subsystem	DIG
29	TDG-DSSCOMP1	TDGZ80SYS	PE-02	UNIT		Complete Packaged Single Drive Standard Disk Subsystem	DIG
30	TDG-DSSCOMP2	TDGZ80SYS	PE-02	UNIT		Complete Packaged Dual Drive Standard Disk Subsystem	DIG
31	TDG-DSSCOMP3	TDGZ80SYS	PE-02	UNIT		Complete Packaged Three Drive Standard Disk Subsystem	DIG
32	TDG-DSSCOMP4	TDGZ80SYS	PE-02	UNIT		Complete Packaged Four Drive Standard Disk Subsystem	DIG
33	TDG-PHI1	TDGZ80SYS	PE-04	MOD		Fixture For Single Cassette Drive;5 Inches/Sec	DIG
34	TDG-PHI2	TDGZ80SYS	PE-04	MOD		Fixture for Two Cassette Drive	DIG
35	TDG-PHI4	TDGZ80SYS	PE-04	MOD		Fixture for Four Cassette Drive	DIG
36	TDG-PTTRAC1	TDGZ80SYS	PE-10	UNIT		Tractor-Feed Printer;110 Char/S Max;5x7,64 Char;7 Bit ASCII Parallel Inp	DIG
37	TDG-MON9D	TDGZ80SYS	PE-15	UNIT		9 Inch Monitor;BW 20MHz Min;Lin Error 2% max;Tr,Tf 20ns max,TTL,15V at1A	DIG
38	TDG-MON9J	TDGZ80SYS	PE-23	UNIT		9 Inch Javelin Black And White Monitor	DIG
39	TDG-PT96	TDGZ80SYS	PE-24	UNIT		96 Column Printer And Interface To 8 Bit Parallel Port;120 Characters/s	DIG
40	TDG-PT96PS	TDGZ80SYS	PE-60	MOD		96 Column Printer Power Supply	DIG
41	TDG-KEY1	TDGZ80SYS	PE-61	UNIT		Capacitance Keyboard;76 Keys Incl Numeric Pad;128 Char ASCII;TTL Output	DIG
42	TDG-1702F	TDGZ80SYS	PROM	MOD		Memory Board Including 16 Type 1702A Units For 4k of EPROM	DIG
43	TDG-MEM8	TDGZ80SYS	RAM	MOD		8k RAM;Access Time 500ns;Power 1.6A at 5.0V	DIG
44	TDG-MEM8C	TDGZ80SYS	RAM	MOD		8k Fast,Lo Pwr RAM;Access Time 250ns;Power:1.2A at 5.0V	DIG
45	TDG-MEM16	TDGZ80SYS	RAM	MOD		16k RAM In Kit Form;Access Time 450ns;Power Req:2.0A at 5.0V	DIG
46	TDG-MEM16-32	TDGZ80SYS	RAM	MOD		Kit To Upgrade Memory From 16k To 32k	DIG
47	TDG-MEM32	TDGZ80SYS	RAM	MOD		32k RAM On 12in x 5in Card;Access Time 450ns;Power Req:4.0A at 5.0V	DIG
48	TDG6500SYS	TDG6500SYS	COMP	MODS		8 Bit Microcomputer System;Uses 6502 CPU;Mem Perip,IO Options	DIG
49	TDG6502	TDG6500SYS	CPU	MOD		6502 Processor;2k RAM;1/4k ROM;Compatible With All TDG Systems	DIG
50	TDG6800SYS	TDG6800SYS	COMP	MODS		8 Bit Microcomputer System;Uses 6800 CPU;Mem Perip,IO Options	DIG
51	TDG6800	TDG6800SYS	CPU	MOD		6800 Processor;2k RAM;1/4k ROM;Compatible With All TDG Systems	DIG
52	TDG8080SYS	TDG8080SYS	COMP	MODS		8 Bit Microcomputer System;Uses 8080 CPU;Mem Perip,IO Options	DIG
53	TDG8080	TDG8080SYS	CPU	MOD		8080 Processor;2k RAM;1/4k ROM;Compatible With All TDG Systems	DIG
54	DDS-187	COSMOS	COMP	UNIT		Dual Motion Detector System Reporting on Via Radio or Tele	DIV
55	SC138	COSMOS	COMP	UNIT		Surveillance Camera Instant Color Film Reporting Radio Trans or Telephone	DIV
56	145-2042	COSMOS	CPU	MOD		Bell Compatible Modem 300 or 600 Baud FSK Transmission	DIV
57	145-2050	COSMOS	CPU	MOD		CPU Card W/Optional APU DMA Control Buffered Data, Address,Control	DIV
58	145-2013	COSMOS	DEV	MOD	MCX	2k Byte Mem Uses 256x4 Ram;Battery Option For Non-Volatile Memory	DIV
59	145-2022	COSMOS	DEV	MOD	MCX	2k Byte Mem Uses 1kx1 RAM;Battery Option For Non-Volatile Memory	DIV
60	145-2033	COSMOS	IO-02	MOD	MCX	Real Time Interrupt	DIV
61	145-2023	COSMOS	IO-20	MOD		Serial I/O Card Configurable as Data Terminal or Data Communic Equip	DIV
62	145-2056	COSMOS	IO-20	MOD		Monitors Proper Program Operation Contains Bootstrap, Restart and Test	DIV
63	145-2028	COSMOS	IO-31	MOD		Decoders, Drivers 4 Digit Decimal Points and a Colon	DIV
64	145-2044	COSMOS	IO-31	MOD		Decoders Drivers 8 Digit 6 Decimal Points and 3 Colon	DIV
65	145-2051	COSMOS	IO-31	MOD		32k-Byte Multi Eprom Card Buffered Data Bus Temp -40 to 80	DIV
66	145-2025	COSMOS	IO-33	MOD	MCX	4 Input/Output Ports;8 Bit Each	DIV
67	145-2041	COSMOS	IO-33	MOD		General Purpose Counter Time Base Counter and A Event/Period Counter	DIV
68	145-2020	COSMOS	IO-40	MOD		D/A Converter Card Bipolar or Unipolar Operation	DIV
69	145-2201	COSMOS	IO-45	MOD		Analog Data Acquisition Card Unipolar or Bipolar Input Capability	DIV
70	PI-1/TG-1	COSMOS	IO-92	UNIT		Petroleum Instrumentation and Gauging	DIV
71	145-2047	COSMOS	PE-16	MOD		Led Driver Card Panel Mountingfor up to 12 LEDS w/Drivers	DIV
72	145-3200	COSMOS	PE-60	UNITT		Standard Power Supply w/ 5V (-) 9-15V 115/230 VAC Input	DIV
73	145-2038	COSMOS	PE-61	MOD		Keyboard Card Fully Decode andDebounce 16 Key Hex Keypad	DIV
74	145-2055	COSMOS	PE-61	UNIT		Optically Isolated Discrete I/O Interface w/2500 VRMS Isolation	DIV
75	145-2058	COSMOS	PE-61	UNIT		8 Pulse Outputs w/Direction Control TTL Compatible	DIV
76▼	145-2050A	EiComp	CPU	MOD	MCX	CPU Card w/Optional APU;8 Bit Word Size;16 Bit Mem Addr;64k Bytes Memory	DIV
77▼	145-2041C	EiComp	IO-33	MOD	MCX	General Purpose Counter Card;Time Base-Event/Period Counter;24 Bit Resol	DIV
78▼	145-2072-1	EiComp	IO-40	MOD	MCX	One Channel Analog Output Card;4-20mA Current Loop;12Bit Resolution	DIV
79▼	145-2072-2	EiComp	IO-40	MOD	MCX	Two Channel Analog Output Card;4-20mA Current Loop;12Bit Resolution	DIV
80▼	145-2072-4	EiComp	IO-40	MOD	MCX	Four Channel Analog Output Card;4-20mA Current Loop;12Bit Resolution	DIV
81▼	145-2071	EiComp	IO-41	MOD	MCX	Analog Input Card:16 SE or Pseudo-Diff,or 8 Diff Input Chs;Opt RMS Conv	DIV
82▼	145-2076	EiComp	IO-41	MOD	MCX	8 Ch Resistive Temp Device (RTD):Handles 4 Wire,100ΩRTD s;12 Bit Resol.	DIV
83▼	145-2068	EiComp	IO-92	MOD	MCX	Binary Input Card:16 Opticcally Isolated Inputs;Memory Mapped Operation	DIV
84▼	145-2069	EiComp	IO-92	MOD	MCX	Binary Output Card:16 Optically Isolated Outputs;Memory Mapped Operation	DIV
85▼	145-2022D	EiComp	RAM	MOD	MCX	2K X 8 Bit Static Ram Card:Optional Batt Standby,Write Protect;5Vdc	DIV
86▼	145-2066-2	EiComp	RAM	MOD	MCX	2k X 8Bit Static Ram Card:5Vdc at 1.0mA typ Quiescient;33mA typ at 3.2MHz	DIV
87▼	145-2066-2B	EiComp	RAM	MOD	MCX	2k X 8Bit Static Ram Card:5Vdc at 1.0mA typ Quiescient;With Battery	DIV
88▼	145-2066-4	EiComp	RAM	MOD	MCX	4k X 8Bit Static Ram Card:5Vdc at 1.0mA typ Quiescient;33mA typ at 3.2MHz	DIV
89▼	145-2066-4B	EiComp	RAM	MOD	MCX	4k X 8Bit Static Ram Card:5Vdc at 1.0mA typ Quiescient;With Battery	DIV
90▼	145-2066-8	EiComp	RAM	MOD	MCX	8k X 8Bit Static Ram Card:5Vdc at 1.0mA typ Quiescient;33mA typ at 3.2MHz	DIV
91▼	145-2066-8B	EiComp	RAM	MOD	MCX	8k X 8Bit Static Ram Card:5Vdc at 1.0mA typ Quiescient;With Battery	DIV
92▼	Am9517A-1DC	AmZ8000	IO-03	Chip	MNG	Multimode DMA Controller:4 Independent DMA Chs each w/Separate Address	DMA
93	M8A	CS8	CPU	MOD	BTX	64,8 Bit Regs;24 16 Bit Regs;256 8 Bit I/O Ports	DSI
94	9007-1100	SYSTEM4	CPU	MOD	MPX	CPU Module;Uses Intel 4004	DSI
95	9007-1110	SYSTEM4	CPU	MOD	MPX	CPU Module;Uses Intel 4040	DSI
96	9007-1120	SYSTEM4	CPU	MOD	MPX	CPU Module;Uses Intel 4040	DSI
97	9007-9500	SYSTEM4	DEV	MOD		Diagnostic Equipment;Comstar 4 Tester	DSI
98	9007-9601	SYSTEM4	DEV	MOD		Diagnostic Equipment;Portable Program Analyzer	DSI
99	9007-9610	SYSTEM4	DEV	MOD		Diagnostic Equipment;Front Panel Analyzer	DSI
100	9007-9710	SYSTEM4	DEV	MOD		Diagnostic Equipment;Module Tester	DSI
101	9008-0203	SYSTEM4	DEV	MOD		Machine Language Program Equipment;Keyboard Program Interface Card	DSI
102	9008-0950	SYSTEM4	DEV	MOD		Machine Language Program Equipment;Portable Editor Program Unit	DSI
103	9008-0201	SYSTEM4	DEV	UNIT		Machine Language Program Equipment;Keyboard Program Unit	DSI
104	9008-0210	SYSTEM4	DEV	UNIT		Machine Language Program Equipment;Ultraviolet PROM Erase Unit	DSI
105	9007-1111	SYSTEM4	IO-02	MOD	BTX	Interrupt Control Module	DSI
106	9007-8620	SYSTEM4	IO-05	MOD		Tape Transport Interface Module	DSI
107	9007-8100	SYSTEM4	IO-20	MOD	BTX	Comm Mod;Serial Data Comm Module;Interfaces W/Modem	DSI
108	9007-8101	SYSTEM4	IO-20	MOD	BTX	Comm Mod;Serial Data Comm Module;Interfaces W/Auto Answer	DSI
109	9007-8300	SYSTEM4	IO-20	MOD	BTX	Comm Mod;Serial Data Comm Mod;Interfaces W/Modem	DSI
110	9007-8301	SYSTEM4	IO-20	MOD	BTX	Comm Mod;Base Chandhuri Cyclical Redundancy Check Mod	DSI

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	9007-8310	SYSTEM4	IO-20	MOD	BTX	Programmable Special Communication Module	DSI
2	9007-8350	SYSTEM4	IO-20	MOD	BTX	Asynchronous Communication Modem	DSI
3	9007-8351	SYSTEM4	IO-20	MOD	BTX	Synchronous Communication	DSI
4	9007-275X	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;Multipurpose Module	DSI
5	9007-2100	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;32 Input TTL	DSI
6	9007-2101	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;32 Input TTL,Photo ISO Inputs	DSI
7	9007-2200	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;32 Input HTL	DSI
8	9007-2300	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;32 Output TTL	DSI
9	9007-2400	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;32 Output HTL	DSI
10	9007-2500	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;16x16 I/O TTL	DSI
11	9007-2600	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;16x16 I/O HTL	DSI
12	9007-2700	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;Multiplexer Driver	DSI
13	9007-2800	SYSTEM4	IO-33	MOD	BTX	Digital Interface Module;Diode Board	DSI
14	9007-8200	SYSTEM4	IO-33	MOD	BTX	Comm Mod;Parallel Data Comm Mod;TTL Level	DSI
15	9007-8201	SYSTEM4	IO-33	MOD	BTX	Comm Mod;Parallel Data Comm Mod;HTL Level	DSI
16	9007-8202	SYSTEM4	IO-33	MOD	BTX	Comm Mod;Parallel Data Comm Mod;24V DC	DSI
17	9007-7000	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;4 Ch Sample And Hold Module	DSI
18	9007-7100	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;8 Ch Sample And Hold Module	DSI
19	9007-7200	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;12 Bit Bin D/A Converter Module	DSI
20	9007-7210	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;12 Bit Bin D/A Converter Module	DSI
21	9007-7220	SYSTEM4	IO-40	MOD		Analog Output Mod;12 Bit Bin D/A Converter Module W/Pwr Amp	DSI
22	9007-7230	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;12 Bit Bin D/A Converter W/Pol SW And Pwr Amp	DSI
23	9007-7300	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;3 Digit BCD DAC Module	DSI
24	9007-7310	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;3 Digit BCD DAC Module W/Pol Switching	DSI
25	9007-7320	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;3 Digit BCD DAC W/Pwr Ampl Output	DSI
26	9007-7330	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;3 Digit BCD DAC W/Pol SW And Pwr Amp	DSI
27	9007-7400	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;4 Digit BCD DAC Module	DSI
28	9007-7410	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;4 Digit BCD DAC W/Pol Switching	DSI
29	9007-7420	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;4 Digit BCD DAC W/Pwr Amp	DSI
30	9007-7430	SYSTEM4	IO-40	MOD	BTX	Analog Output Mod;4 Digit BCD DAC W/Pol SW And Pwr Amp	DSI
31	9007-6000	SYSTEM4	IO-41	MOD	BTX	Analog Input Mod;Sense Amplifier Module	DSI
32	9007-6100	SYSTEM4	IO-41	MOD	BTX	Analog Input Mod;Program Gain Amplifier Module	DSI
33	9007-6200	SYSTEM4	IO-41	MOD	BTX	Analog Input Mod;12 Bit Binary A/D Converter Module	DSI
34	9007-6300	SYSTEM4	IO-41	MOD	BTX	Analog Input Mod;3 Digit BCD A/C Converter Module	DSI
35	9007-6400	SYSTEM4	IO-41	MOD	BTX	Analog Input Mod;4 Digit BCD A/C Converter Module	DSI
36	9007-6500	SYSTEM4	IO-41	MOD	BTX	Analog Input Mod;Flying Capacitor Multiplexer Module	DSI
37	9007-6600	SYSTEM4	IO-41	MOD	BTX	Analog Input Mod;Diff Analog Multiplexer Module	DSI
38	9007-6700	SYSTEM4	IO-41	MOD	BTX	Analog Input Mod;Single Ended Analog Multiplexer Module	DSI
39	9007-6800	SYSTEM4	IO-41	MOD	BTX	Analog Input Mod;Thermocouple Ref Junction Module	DSI
40	9007-8905	SYSTEM4	IO-92	MOD		32 Character Alphanum Display;Power Supply	DSI
41	9007-8700	SYSTEM4	PE-01	UNIT		Flexible Disc System	DSI
42	9007-8610	SYSTEM4	PE-04	UNIT		Magnetic Tape Cassette System	DSI
43	9007-8901	SYSTEM4	PE-16	MOD		32 Character Alphanum Display Driver Mod	DSI
44	9008-1100	SYSTEM4	PE-16	MOD		LED Display Module	DSI
45	RT4	SYSTEM4	PE-20	UNIT		4 Bit Remote Intelligent Terminal;Based On uComp Mod Using Intel 4040	DSI
46	9007-8270	SYSTEM4	PE-24	UNIT		Alphanum Line Printer System;Buffered Interface	DSI
47	9007-8800	SYSTEM4	PE-40	UNIT		Card Reader System;Reads 150 CPM	DSI
48	9007-8850	SYSTEM4	PE-40	UNIT		Magnetic Card Reader System;Interface Card	DSI
49	9007-8400	SYSTEM4	PE-42	UNIT		120 CPS Paper Tape Reader System;5 To 8 Ch Sw Selectable	DSI
50	9007-8535	SYSTEM4	PE-42	UNIT		35 CPS Paper Tape Reader System;5 To 8 Ch Capacity	DSI
51	9008-0601	SYSTEM4	PE-61	MOD		16 Key Keyboard W/TTL Level Output	DSI
52	9007-1301	SYSTEM4	PROM	MOD	MNX	PROM 1k x 8 Bit Word Module	DSI
53	9007-1302	SYSTEM4	PROM	MOD	MNX	PROM 2k x 8 Bit Word Module	DSI
54	9007-1311	SYSTEM4	PROM	MOD	MNX	PROM 1k x 8 Bit Word Module;Prerequisite 9007-1302	DSI
55	9007-1312	SYSTEM4	PROM	MOD	MNX	PROM 2k x 8 Bit Word Module;Prerequisite 9007-1302	DSI
56	9007-1322	SYSTEM4	PROM	MOD	MNX	High Performance PROM;2k x 8 Bit Word Module	DSI
57	9007-1381	SYSTEM4	PROM	MOD	MNX	PROM Table Memory Module;1k x 8 Bit Word	DSI
58	9007-1382	SYSTEM4	PROM	MOD	MNX	PROM Table Memory Module;2k x 8 Bit Word	DSI
59	9007-1201	SYSTEM4	RAM	MOD	MPX	1.28k Bit A-RAM;16 Output Lines	DSI
60	9007-1202	SYSTEM4	RAM	MOD	MPX	2.56k Bit A-RAM;32 Output Lines	DSI
61	9007-1281	SYSTEM4	RAM	MOD	MPX	1.28k Bit B-RAM;16 Output	DSI
62	9007-1285	SYSTEM4	RAM	MOD	MNX	8.192k Bit C-RAM Module	DSI
63	9007-1290	SYSTEM4	RAM	MOD	MNX	16k Bit Auxiliary RAM Module	DSI
64	9007-1295	SYSTEM4	RAM	MOD	MCX	8.192k Bit D-RAM Module	DSI
65	CONCEPT80	SYSTEM8	COMP	UNIT		8 Bit Microcomputer System For Industrial Control,Uses 8080CPU	DSI
66	9000-0080	SYSTEM8	CPU	MOD		8 Bit Central Processor For M80 System;Uses 8080 Instruction Set	DSI
67	9010-1101	SYSTEM8	CPU	MOD		M8Z CPU Module;Selectable Inst Set;Interfaces to Mem/IO Through COMBUS	DSI
68	9000-0870	SYSTEM8	IO-01	MOD		M80 Clock Timer Bootstrap Mod:Includes Bootstrap Mod	DSI
69	9000-0871	SYSTEM8	IO-01	MOD		M80 Clock Timer Mod W/O Bootstrap Mem;W/Three 16 Bit Interval Timer	DSI
70	9010-1111	SYSTEM8	IO-01	MOD	BTX	Real Time Control Module;For Timing And Power Status	DSI
71	9010-5300	SYSTEM8	IO-01	MOD	BTX	Bi-Directional Counter Module;Quadrature Input Count x1	DSI
72	9010-5301	SYSTEM8	IO-01	MOD	BTX	Bi-Directional Counter Module;Quadrature Input Count x2	DSI
73	9010-5302	SYSTEM8	IO-01	MOD	BTX	Bi-Directional Counter Module;Quadrature Input Count x4	DSI
74	9010-1140	SYSTEM8	IO-03	MOD	BTX	Program Trap Module;Continually Monitors Memory	DSI
75	9010-1235	SYSTEM8	IO-03	MOD	BTX	CPU Multiport Memory Interface Module	DSI
76	9010-8100	SYSTEM8	IO-20	MOD	BTX	EIA Or Current Loop Serial Data Communications Module	DSI
77	9010-8310	SYSTEM8	IO-20	MOD	BTX	Communications Interface I/O Module	DSI
78	9010-8350	SYSTEM8	IO-20	MOD	BTX	Digital Modem;Data Rate 0 To 1200 Bits/Second	DSI
79	9010-8351	SYSTEM8	IO-20	MOD	BTX	Digital Modem;Data Rate 1200 Bits/Second	DSI
80	9010-8352	SYSTEM8	IO-20	MOD	BTX	Digital Modem;Data Rate 0 To 1200 Bits/Second	DSI
81	9010-8353	SYSTEM8	IO-20	MOD	BTX	Digital Modem;Data Rate 0 To 300 Bits/Second	DSI
82	9010-8354	SYSTEM8	IO-20	MOD	BTX	Digital Modem;Data Rate 0 To 300 Bits/Second	DSI
83	9005-0151	SYSTEM8	IO-31	MOD		Slo-Syn Stepper Driver Module;For Driving Stepper Motors	DSI
84	9010-5150	SYSTEM8	IO-32	MOD	BTX	Variable Freq Output Module; .01Hz To 16772.16Hz	DSI
85	9000-0060	SYSTEM8	IO-33	MOD		Translator Module;Interfaces 9000-0080 CPU Mod To Mem And I/O Modules	DSI
86	9000-0061	SYSTEM8	IO-33	MOD		Translator Module;Interfaces Intel SBC 80/10,20 CPU To Mem,I/O Modules	DSI
87	9003-0262	SYSTEM8	IO-33	MOD		24V DC Output Module;Provides W/4 Drivers,5Amp Switching Current	DSI
88	9003-0452	SYSTEM8	IO-33	MOD		130V DC Output Module;Provides W/4 Drivers,1Amp Switching Current	DSI
89	9010-2100	SYSTEM8	IO-33	MOD	BTX	64 Input TTL Module;For Non Latching Digital Input	DSI
90	9010-2101	SYSTEM8	IO-33	MOD	BTX	32 ISO-Input Module;Non-Latching Optically Isolated Inputs	DSI
91	9010-2102	SYSTEM8	IO-33	MOD	BTX	16 ISO-Input Latching Module;Photo-Isolated Input	DSI
92	9010-2103	SYSTEM8	IO-33	MOD	BTX	16 Input TTL Latching Module;5Vdc,480mA	DSI
93	9010-2150	SYSTEM8	IO-33	MOD	BTX	64 Input TTL Module;For Non Latching Digital Input	DSI
94	9010-2201	SYSTEM8	IO-33	MOD		16 Isolated Input Latching Module;Two 8 Bit Input Ports	DSI
95	9010-2202	SYSTEM8	IO-33	MOD		16 Isolated Input Latching Module;Input 10 to 18V	DSI
96	9010-2203	SYSTEM8	IO-33	MOD		16 Isolated Input Latching Module;Input 21.5 to 29V	DSI
97	9010-2250	SYSTEM8	IO-33	MOD		16 TTL Input Latching Module;Two 8 Bit Input Ports	DSI
98	9010-2300	SYSTEM8	IO-33	MOD	BTX	Output Module;32 Non-Isolated DC Out Channels	DSI
99	9010-2301	SYSTEM8	IO-33	MOD	BTX	Output Module;32 Non-Isolated DC Out Channels	DSI
100	9010-2400	SYSTEM8	IO-33	MOD	BTX	Output Module;32 Non-Isolated DC Out Channels	DSI
101	9010-2401	SYSTEM8	IO-33	MOD	BTX	Output Module;32 Non-Isolated DC Out Channels	DSI
102	9010-2410	SYSTEM8	IO-33	MOD	BTX	16 ISO-Output Module;16 Latching DC Output Channels	DSI
103	9010-2420	SYSTEM8	IO-33	MOD	BTX	16 ISO-Output Module;16 Latching DC Output Channels	DSI
104	9010-2500	SYSTEM8	IO-33	MOD	BTX	32 In/32 Out TTL Module;32 Non-Latch In/32 Latch Out	DSI
105	9010-2550	SYSTEM8	IO-33	MOD	BTX	32 In/32 Out TTL Module;32 Non-Latch In/32 Latch Out	DSI
106	9003-0631	SYSTEM8	IO-40	MOD		120V AC 2 Amp Triac Output Module;6 Switches,Each Rated at 2A	DSI
107	9003-0636	SYSTEM8	IO-40	MOD		120V AC 1 Amp Triac Output Module;Provides 6 Interface Ckts to Driver	DSI
108	9010-3100	SYSTEM8	IO-40	MOD	BTX	120V In/Out Signal Conditioning Subsystems;120V AC Output	DSI
109	9010-5900	SYSTEM8	IO-40	MOD	BTX	Servo Interface Module;Provides Dig To Analog Out To Close Servo Loop	DSI
110	9010-7210	SYSTEM8	IO-40	MOD	BTX	D/A Converter Module;3 Digit BCD	DSI

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	9010-7220	SYSTEM8	IO-40	MOD	BTX	D/A Converter Module;12 Bit Binary	DSI
2	9010-7230	SYSTEM8	IO-40	MOD	BTX	D/A Converter Module;4 Digit BCD	DSI
3	9010-7240	SYSTEM8	IO-40	MOD	BTX	D/A Converter Module;16 Bit Binary	DSI
4	9001-0601	SYSTEM8	IO-41	MOD		120V AC Signal Converter Input Module;Interfaces Bet AC and DC	DSI
5	9010-3000	SYSTEM8	IO-41	MOD	BTX	120V In/Out Signal Conditioning Subsystems;120V AC Input	DSI
6	9010-6000	SYSTEM8	IO-41	MOD	BTX	Analog Input Signal Conditioning Module;Direct V Input	DSI
7	9010-6010	SYSTEM8	IO-41	MOD	BTX	Analog Input Signal Conditioning Module;DC V To V Input	DSI
8	9010-6020	SYSTEM8	IO-41	MOD	BTX	Analog Input Signal Conditioning Module;DC I To V Input	DSI
9	9010-6030	SYSTEM8	IO-41	MOD	BTX	A.C. True RMS Input Conditioning Module	DSI
10	9010-6060	SYSTEM8	IO-41	MOD	BTX	4 Channel Instrumentation Amplifier Module	DSI
11	9010-6080	SYSTEM8	IO-41	MOD	BTX	D.C. Strain Gauge Module	DSI
12	9010-6085	SYSTEM8	IO-41	MOD	BTX	A.C. Strain Gauge Module	DSI
13	9010-6320	SYSTEM8	IO-41	MOD	BTX	Programmable Gain Amplifier Module	DSI
14	9010-6410	SYSTEM8	IO-41	MOD	BTX	Analog To Digital Converter;3 Digit BCD	DSI
15	9010-6420	SYSTEM8	IO-41	MOD	BTX	Analog To Digital Converter;12 Bit Binary	DSI
16	9010-6430	SYSTEM8	IO-41	MOD	BTX	Analog To Digital Converter;4 Digit BCD	DSI
17	9010-6440	SYSTEM8	IO-41	MOD	BTX	Analog To Digital Converter;16 Bit Binary	DSI
18	9010-7010	SYSTEM8	IO-41	MOD	BTX	4 Channel Sample And Hold Module	DSI
19	9010-7020	SYSTEM8	IO-41	MOD	BTX	8 Channel Sample And Hold Module	DSI
20	9010-6210	SYSTEM8	IO-43	MOD	BTX	Relay Multiplexer Module	DSI
21	9010-6220	SYSTEM8	IO-43	MOD	BTX	Solid State Multiplexer Module	DSI
22	9005-0162	SYSTEM8	IO-92	MOD		Solid State Stepper Module;Provides 12 Step Timer Sequence	DSI
23	9010-2600	SYSTEM8	IO-92	MOD		Relay Module;Provides 8 Relay W/Mercury Wetted C Contacts	DSI
24	9010-5100	SYSTEM8	IO-92	MOD	BTX	ISO Pulse Accumulator;Photo Isolated Contains Two 16 Bit Counters	DSI
25	9010-6040	SYSTEM8	IO-92	MOD	BTX	4 Channel Thermocouple Amplifier Module	DSI
26	9010-6050	SYSTEM8	IO-92	MOD	BTX	Excitation Source Module	DSI
27	9010-6070	SYSTEM8	IO-92	MOD	BTX	LVDT Input Module;Used With LVDT Transducers	DSI
28	9010-6090	SYSTEM8	IO-92	MOD	BTX	Frequency To Voltage Converter	DSI
29	9000-0110	SYSTEM8	IO-92	UNIT		M80 Program Analyzer W/Analyzer Interface Mod;Supports M80	DSI
30	9010-8700	SYSTEM8	PE-01	UNIT		Flexible Disk System W/Multiport Memory Interface	DSI
31	9010-8702	SYSTEM8	PE-01	UNIT		Twin Flexible Disk System W/Multiport Memory Interface	DSI
32	9010-8710	SYSTEM8	PE-02	UNIT		Mass Storage Disk Pack System W/40 Megabyte Mem Interface	DSI
33	9010-8720	SYSTEM8	PE-02	UNIT		Mass Storage Disk Pack System W/80 Megabyte Mem Interface	DSI
34	9010-8610	SYSTEM8	PE-04	UNIT		Magnetic Tape Cassette System;W/Interface Module	DSI
35	9010-9946	SYSTEM8	PE-16	MOD		16 Edge Mounted LED Indicators;For Alarm Status Indicator	DSI
36	9010-8900	SYSTEM8	PE-16	UNIT		16 Character Alphanumeric Display System	DSI
37	9010-8901	SYSTEM8	PE-16	UNIT		32 Character Alphanumeric Display System	DSI
38	9010-8650	SYSTEM8	PE-23	UNIT		15 Inch CRT Keyboard/Display System W/Mem Interface	DSI
39	9010-8800	SYSTEM8	PE-40	UNIT		Card Reader System W/Multiport Memory Interface	DSI
40	9010-8400	SYSTEM8	PE-42	UNIT		120 CPS Paper Tape Reader System	DSI
41	9010-9101	SYSTEM8	PE-60	MOD		Regulator Module;Sw Reg,Converts 18-28V DC to 5V DC at 5 Amps	DSI
42	9010-9200	SYSTEM8	PE-60	MOD		150VA Power Supply;Provides 6 Isolated 24V DC,One 32V DC/24V AC Output	DSI
43	9010-9300	SYSTEM8	PE-60	MOD		400VA Power Supply;Provides 6 Isolated 24V DC,One 32V DC/24V AC Output	DSI
44	9010-9500	SYSTEM8	PE-60	MOD		Analog Power Supply;Provides 4 Isolated 24V 100mAmp Unreg Output	DSI
45	9010-1120	SYSTEM8	PE-61	UNIT		Programmer Console;For Data Entry 8 Digit Display	DSI
46	9000-1151	SYSTEM8	PROM	MOD		2048 Byte EPROM Mod,Uses 2716 Chips,UV Erasable,Self Progm	DSI
47	9000-1152	SYSTEM8	PROM	MOD		4096 Byte EPROM Mod,Uses 2716 Chips,UV Erasable,Self Progm	DSI
48	9000-1153	SYSTEM8	PROM	MOD		6144 Byte EPROM Mod,Uses 2716 Chips,UV Erasable,Self Progm	DSI
49	9000-1154	SYSTEM8	PROM	MOD		8192 Byte EPROM Mod,Uses 2716 Chips,UV Erasable,Self Progm	DSI
50	9000-1155	SYSTEM8	PROM	MOD		10240 Byte EPROM Mod,Uses 2716 Chips,UV Erasable,Self Progm	DSI
51	9000-1156	SYSTEM8	PROM	MOD		12288 Bytes EPROM Mod;Uses 2716 Chips,UV Erasable,Self Progm	DSI
52	9000-1157	SYSTEM8	PROM	MOD		14336 Bytes EPROM Mod;Uses 2716 Chips,UV Erasable,Self Progm	DSI
53	9000-1158	SYSTEM8	PROM	MOD		16384 Bytes EPROM Mod;Uses 2716 Chips,UV Erasable,Self Progm	DSI
54	9010-1321	SYSTEM8	PROM	MOD	MNX	1024x8 PROM May Be Erased By UV Light	DSI
55	9010-1322	SYSTEM8	PROM	MOD	MNX	2048x8 PROM May Be Erased By UV Light	DSI
56	9010-1323	SYSTEM8	PROM	MOD	MNX	3072x8 PROM May Be Erased By UV Light	DSI
57	9010-1324	SYSTEM8	PROM	MOD	MNX	4096x8 PROM Erased By UV Light	DSI
58	9000-0150	SYSTEM8	RAM	MOD		4096 Byte RAM,Uses 2104 Chip,W/Write Protection,Battery Support	DSI
59	9000-0151	SYSTEM8	RAM	MOD		8192 Byte RAM,Uses 2108 Upper Chip W/Write Protect,Batt Support	DSI
60	9000-0152	SYSTEM8	RAM	MOD		8192 Byte RAM,Uses 2108 Lower Chip W/Write Protect,Batt Support	DSI
61	9000-0153	SYSTEM8	RAM	MOD		16384 Byte RAM,Uses 2116 Chip W/Write Protection,Batt Support	DSI
62	9010-1200	SYSTEM8	RAM	MOD	MNX	4k x 8 Random Access Memory Module	DSI
63	9010-1210	SYSTEM8	RAM	MOD	MNX	1k x 8 Random Access Memory Module	DSI
64	9010-1230	SYSTEM8	RAM	MOD	MNX	4k x 8 Multiport Random Access Memory Module	DSI
65	9010-1231	SYSTEM8	RAM	MOD	MNX	1k x 8 Multiport Random Access Memory Module	DSI
66	9010-1250	SYSTEM8	RAM	MOD	MNX	1k x 8 CMOS Random Access Memory Module	DSI
67	9010-1332	SYSTEM8	ROM	MOD	MNX	2048x8 ROM 5Vdc,960mA	DSI
68	9010-1334	SYSTEM8	ROM	MOD	MNX	4096x8 ROM 5Vdc,1740mA	DSI
69	DT212	IMP16	IO-45	MOD		Dual 12 Bit D/A Point Plotter Converter for RT Displays (Connector Reqd)	DTI
70	DT820	IMP16	IO-45	MOD		Analog Input Mod:8 Bits,8 Inputs,Throughput 50kHz	DTI
71	DT825	IMP16	IO-45	MOD		Analog Input Mod:8 Bits,16 Inputs,Throughput 50kHz	DTI
72	DT830	IMP16	IO-45	MOD		Analog Input Mod:10 Bits,8 Inputs,Throughput 30kHz	DTI
73	DT835	IMP16	IO-45	MOD		Analog Input Mod:10 Bits,16 Inputs,Throughput 30kHz	DTI
74	DT1722	IMP16	IO-45	MOD		Analog Input Sys;16,32,64 Channels Voltage Input.8,16,32 Channels 4-20mA	DTI
75	DT15150	IMP16	IO-45	MOD		DC/DC Converter,115 at 150MA;EMI/RFI Shielding	DTI
76	DTC02EX	IMP16	IO-45	MOD		48SE or 24DI Strappable Expander for DT57C02 (Connector Reqd)	DTI
77	DTC03EX	IMP16	IO-45	MOD		8DI Expander for DT57C03 (Connector Reqd)	DTI
78	DT1735	LSI Series	IO-45	MOD		8 Ch D/A Output Sys;12 Bit w/Optional 4-20MA Current Loop Output;5V at 2A	DTI
79	DT1738	LSI Series	IO-45	MOD		Isolated Low Level Analog Input Sys.4DI and 12DI Channels	DTI
80	DT1739	LSI Series	IO-45	MOD		Isolated Low Level Analog Input Sys.4DI Input Chan.2 Non.isolated D/A Out	DTI
81	DT2771	LSI-11	IO-03	MOD		Dual 12 Bit D/A Ch;Buffered Out;Individual X and Y Outputs;ZAxis Out	DTI
82	DT2782	LSI-11	IO-03	MOD		35kHz Typ Thruput Self Contained DMA Interface;Hi Level Inputs;±10V Max	DTI
83	DT2784	LSI-11	IO-03	MOD		31kHz Max Thruput Self Contained DMA Interface;Lo Level Inputs;±10V Max	DTI
84	DT2768I	LSI-11	IO-30	MOD		200V Optical Isolation;16Bit Data In;16 Latched Out Lines;Industrial	DTI
85	DT2781	LSI-11	IO-41	MOD		±10V Input Range; 25kHz Thruput;2-12 Bit D/A Conv;1-16 Ch/12 A/D Conv	DTI
86	DT2785	LSI-11	IO-41	MOD		10V Input Range; 25kHz Thruput; 2-12 Bit D/A Conv; 1-16 Ch/12 A/D Conv.	DTI
87▼	DT2772	LSI11	IO-23	MOD		Expander for DT2762:Inputs 0-5V,±5V,0-10V,±10V:	DTI
88▼	DT2774	LSI11	IO-23	MOD		Expander for DT2764;Inputs ±10mV to 10V;Adds 48 SE(24 Diff) Input Ex Chs	DTI
89▼	DT2775	LSI11	IO-23	MOD		Expander for DT2765;Inputs ±10mV to 10V;Adds 56 Diff Ex In Chs;±250V CMV	DTI
90	DT2768	LSI11	IO-30	MOD		Isolated Digital I/O Sys,16 Input/16 Output Programmable Counter	DTI
91	DT1731	LSI11	IO-45	MOD		Analog Input Sys.64SE or 32DI Channels.Input Ranges ±5V,±10V,0 to 10V	DTI
92	DT1732	LSI11	IO-45	MOD		Analog I/O Sys.16SE or 8DI Channels.Input/Output Ranges ±5V,±10V,0 to 10V	DTI
93	DT1733	LSI11	IO-45	MOD		Analog Input Sys.64SE or 32DI Channels.Input Ranges 10mV to 10V	DTI
94	DT1734	LSI11	IO-45	MOD		Analog I/O Sys.16SE or 8DI Channels.Input/Output Ranges 10mV to 10V	DTI
95	DT1761	LSI11	IO-45	MOD		Analog I/O Sys.16SE or 8DI Channels.Input/Output Ranges ±5V,±10V,0 to 10V	DTI
96	DT1762	LSI11	IO-45	MOD		Analog Input Sys.64SE or 32DI Channels.Input Ranges ±5V,±10V,0 to 10V	DTI
97	DT1764	LSI11	IO-45	MOD		Analog Input Sys.64SE or 32DI Channels.Input Ranges 10mV to 10V	DTI
98	DT1765	LSI11	IO-45	MOD		Analog I/O Sys.16SE or 8DI Chan.Input Range 10mV to 10V.Out ±5V,±10V,0-10	DTI
99	DT1768	LSI11	IO-45	MOD		Isolated Analog Input Sys.8DI and 12DI Input Channels	DTI
100	DT1769	LSI11	IO-45	MOD		Isolated Analog Input Sys.4DI Input Channels.2 Non-isolated D/A Outputs	DTI
101	DT2762	LSI11	IO-45	MOD		12 Bit,16 Single Ended or 8 Diff Channel,Input Ranges 0-5V,±5V,±10V,0-10	DTI
102	DT2764	LSI11	IO-45	MOD		12 Bit,16 Single Ended or 8 Diff Channel,Input Range 10mV to 10V	DTI
103	DT2765	LSI11	IO-45	MOD		12 Bit,4 Isolated Diff Channels,Input Range 10mV to 10V,±250V CMV Range	DTI
104	DT2766	LSI11	IO-45	MOD		12 Bit,4 Channel,Output Ranges ±5V,±10V,0 to 10V at 20mA,4 TTL Dig Out	DTI
105	DT2767	LSI11	IO-45	MOD		8 Bit,4 Channel,Output Ranges ±5V,±10V,0 to 10V at 20mA,4 TTL Dig Out	DTI
106	DT2769	LSI11	IO-45	MOD		Programmable Clock I/O Sys,Xtal Controlled,16 Bit	DTI
107	DT3762	MULTIBUS	IO-23	MOD		Multifunction; Expands A and D I/O; Use W/DT3752 Series	DTI
108	DT3752	MULTIBUS	IO-45	MOD		High Level,Analog Input System	DTI
109	DT3754	MULTIBUS	IO-45	MOD		LowLevel,Wide Range Analog Inpput System	DTI
110	DT3755	MULTIBUS	IO-45	MOD		Isolated LowLevel,Wide Range,Analog Input System	DTI

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	DT1723	PACE	IO-45	MOD		Analog Input Sys;16SE or 8DI Channels,12 Bit A/D Converter	DTI
2▼	DT1716	PDP11	IO-04	MOD		Analog Output Sys:8Ch w/12 Bit Resolution;Full 4 Quadrant Mutiplying	DTI
3	DT1759	SBC80	IO-41	MOD		Isolated Analog I/O Sys,4 Ch 12 Bit A/D Converter;2 Ch 12 Bit D/A Conv	DTI
4	DT1741	SBC80	IO-45	MOD		Analog Input Sys. of DT1751. Input Only.Ranges ±5V,±10V,0 to 10V	DTI
5	DT1742	SBC80	IO-45	MOD		Analog Input Sys.64SE or 32DI Channels.Input Ranges ±5V,±10V,0 to 10V	DTI
6	DT1744	SBC80	IO-45	MOD		Analog Input Sys.16SE or 8DI Channels.Input Ranges 10mV to 10V	DTI
7	DT1748	SBC80	IO-45	MOD		Isolated Low Level Analog Input Sys.4DI and 12DI Input Channels	DTI
8	DT1749	SBC80	IO-45	MOD		Isolated Low Level Analog Input Sys.4DI Input Channels.2 Non-isol. D/AOut	DTI
9	DT1751	SBC80	IO-45	MOD		Analog I/O Sys.16SE or 8DI Channels.12 Bit A/D,2 Channel 12 Bit D/A	DTI
10	DT1755	SBC80	IO-45	MOD		Low Level Analog I/O Sys.Same Capability as DT1751 but to Levels of 10mV	DTI
11	DT1841	SBC80	IO-45	MOD		Analog Output Sys. Output Section of the DT1751 Without Analog Input	DTI
12	DT1842	SBC80	IO-45	MOD		Analog Output Sys.Eight 12 Bit D/A Outputs.Ranges ±10V,0 to 10V	DTI
13	DT1843	SBC80	IO-45	MOD		Analog Output Sys.Eight 8 Bit D/A Outputs.Ranges ±10V,0 to 10V	DTI
14	DT1791	SUPERPAC180	IO-45	MOD		Analog I/O Sys;16SE or 8 DI Channels,12 Bit A/D,2 Channel 12 Bit D/A	DTI
15	DT1795	SUPERPAC180	IO-45	MOD		Analog I/O Sys;16SE or 8 DI Channels,Low Level Input,2 Channel 12 Bit D/A	DTI
16	DT2734	Z80	IO-23	MOD		Analog Input Expander for DT2722/24;Expands to 64SE or 32DI Input Chs	DTI
17	DT2735	Z80	IO-23	MOD		Analog Input Expander for DT2725;Expands in 8DI Increments	DTI
18	DT2726	Z80	IO-40	MOD		Analog Output 12 Bit Resolution	DTI
19	DT2727	Z80	IO-40	MOD		Analog Output 8 Bit Resolution	DTI
20	DT2722	Z80	IO-41	MOD		16SE/8Diff Input Ch;±5V Full Scale;12 Bit Resolution;30 kHz Thruput	DTI
21	DT2724	Z80	IO-41	MOD		16SE/8Diff Input Ch;10mV to 5V Full Scale; 12 Bit Resol; 30 kHz Thruput	DTI
22	DT2725	Z80	IO-41	MOD		Analog Input Range 10mV/10V; Rejects up to ±250V CMV	DTI
23	DT1781	Z80	IO-45	MOD		Input Ranges ±10V,0-10V.Outputs 2.8mV,4.8mV.16SE or 8DI Channels	DTI
24	DT1782	Z80	IO-45	MOD		Analog Input Sys.Input Ranges ±10V,0 to 10V.64SE or 32DI Chan.12 Bit D/A	DTI
25	DT1784	Z80	IO-45	MOD		Analog Input Sys.Input Range 10mV to 10V.64SE or 32DI Chan.12 Bit D/A	DTI
26	DT1785	Z80	IO-45	MOD		Input Ranges ±10mV,0-10V Outputs 2.4uV,4.8uV 16SE or 8DI Channels	DTI
27	DT1788	Z80	IO-45	MOD		Isolated Low Level Analog Input Sys.4DI and 12DI Input Channels	DTI
28	DT1789	Z80	IO-45	MOD		Isolated Low Level Analog Input Sys.4DI Input Chan.2 Non.isolated D/A Out	DTI
29	ST-LSI-DA4A	LSI-11	IO-40	MOD		Independent 4 Channel D/A Board with DC/DC Conv	DTL
30	ST-LSI-DA4B	LSI-11	IO-40	MOD		Independent 4 Channel D/A Board with DC/DC Conv	DTL
31	ST-LSI2	LSI-11	IO-41	MOD		16 SE or 8 Diff Analog Input Chs,No D/A Chs,PGA and DC/DC Conv Incl	DTL
32	ST-LSI2-ADX	LSI-11	IO-41	MOD		48 SE or 24 Diff Analog Input A/D Chs,No D/A Chs,No DC/DC Conv	DTL
33	ST-LSI2-DMA	LSI-11	IO-41	MOD		Direct Memory Access for Up to 32,768 16 Bit Words as A/D Data Transfers	DTL
34	ST-LSI16D0D1	LSI-11	IO-41	MOD		16 Diff Analog Input A/D Chs,No D/A Chs,Inst Ampl and DC/DC Conv	DTL
35	ST-LSI16D0D2	LSI-11	IO-41	MOD		16 Diff Analog Input A/D Chs,No D/A Chs,Inst Ampl Incl No DC/DC	DTL
36	ST-LSI16D0P1	LSI-11	IO-41	MOD		16 Diff Analog Input A/D Chs,No D/A Chs,PGA and DC/DC Conv Incl	DTL
37	ST-LSI16D0P2	LSI-11	IO-41	MOD		16 Diff Analog Input A/D Chs,No D/A Chs,PGA Incl,No DC/DC Conv	DTL
38	ST-LSI16S0D1	LSI-11	IO-41	MOD		16 SE Analog Input A/D Chs,No D/A Chs,Inst Ampl and DC/DC Conv Incl	DTL
39	ST-LSI16S0D2	LSI-11	IO-41	MOD		16 SE Analog Input A/D Chs,No D/A Chs,Inst Ampl Incl,No DC/DC Conv	DTL
40	ST-LSI16S0P1	LSI-11	IO-41	MOD		16 SE Analog Input A/D Chs,No D/A Chs,PGA and DC/DC Conv Incl	DTL
41	ST-LSI16S0P2	LSI-11	IO-41	MOD		16 SE Analog Input A/D Chs,No D/A Chs,PGA Incl,No DC/DC Conv	DTL
42	ST-LSI16S0X1	LSI-11	IO-41	MOD		16 SE Analog Input A/D Chs,No D/A Chs,DC/DC Conv Incl	DTL
43	ST-LSI16S0X2	LSI-11	IO-41	MOD		16 SE Analog Input A/D Chs,No D/A Chs,No DC/DC Conv	DTL
44	ST-LSI32S0D1	LSI-11	IO-41	MOD		32 SE Analog Input A/D Chs,No D/A Chs,Inst Ampl and DC/DC Conv Incl	DTL
45	ST-LSI32S0D2	LSI-11	IO-41	MOD		32 SE Analog Input A/D Chs,No D/A Chs,Inst Ampl Incl No DC/DC Conv	DTL
46	ST-LSI32S0P1	LSI-11	IO-41	MOD		32 SE Analog Input A/D Chs,No D/A Chs,PGA and DC/DC Conv Incl	DTL
47	ST-LSI32S0P2	LSI-11	IO-41	MOD		32 SE Analog Input A/D Chs,No D/A Chs,PGA Incl No DC/DC Conv	DTL
48	ST-LSI32S0X1	LSI-11	IO-41	MOD		32 SE Analog Input A/D Chs,No D/A Chs,DC/DC Conv Incl	DTL
49	ST-LSI32S0X2	LSI-11	IO-41	MOD		32 SE Analog Input A/D Chs,No D/A Chs,No DC/DC Conv	DTL
50	ST-LSI-ADX-16D	LSI-11	IO-41	MOD		16 Diff Channel Slave A/D Multiplexer Expander	DTL
51♦	ST-LSI16D2D1	LSI-11	IO-42	MOD		16 Diff Analog Input A/D Chs,2 D/A Chs,Inst Ampl and DC/DC Conv	DTL
52♦	ST-LSI16D2D2	LSI-11	IO-42	MOD		16 Diff Analog Input A/D Chs,2 D/A Chs,Inst Ampl,No DC/DC Conv	DTL
53♦	ST-LSI16D2P1	LSI-11	IO-42	MOD		16 Diff Analog Input A/D Chs,2 D/A Chs,PGA and DC/DC Conv Incl	DTL
54♦	ST-LSI16D2P2	LSI-11	IO-42	MOD		16 Diff Analog Input A/D Chs,2 D/A Chs,PGA Incl,No DC/DC Conv	DTL
55♦	ST-LSI16S2D1	LSI-11	IO-42	MOD		16 SE Analog Input A/D Chs,2 D/A Output Chs,Inst Ampl and DC/DC Conv	DTL
56♦	ST-LSI16S2D2	LSI-11	IO-42	MOD		16 SE Analog Input A/D Chs,2 D/A Output Chs,Inst Ampl Incl,No DC/DC	DTL
57♦	ST-LSI16S2P1	LSI-11	IO-42	MOD		16 SE Analog Input A/D Chs,2 D/A Output Chs,PGA and DC/DC Incl	DTL
58♦	ST-LSI16S2P2	LSI-11	IO-42	MOD		16 SE Analog Input A/D Chs,2 D/A Output Chs,PGA Incl,No DC/DC Conv	DTL
59♦	ST-LSI16S2X1	LSI-11	IO-42	MOD		16 SE Analog Input A/D Chs,2 D/A Output Chs,DC/DC Conv Incl	DTL
60♦	ST-LSI16S2X2	LSI-11	IO-42	MOD		16 SE Analog Input A/D Chs,2 D/A Output Chs,No DC/DC Conv	DTL
61♦	ST-LSI32S2D1	LSI-11	IO-42	MOD		32 SE Analog Input A/D Chs,2 D/A Chs,Inst Ampl and DC/DC Conv Incl	DTL
62♦	ST-LSI32S2D2	LSI-11	IO-42	MOD		32 SE Analog Input A/D Chs,2 D/A Chs,Inst Ampl Incl No DC/DC Conv	DTL
63♦	ST-LSI32S2P1	LSI-11	IO-42	MOD		32 SE Analog Input A/D Chs,2 D/A Output Chs,PGA and DC/DC Conv Incl	DTL
64♦	ST-LSI32S2P2	LSI-11	IO-42	MOD		32 SE Analog Input A/D Chs,2 D/A Chs,PGA Incl,No DC/DC Conv	DTL
65♦	ST-LSI32S2X1	LSI-11	IO-42	MOD		32 SE Analog Input A/D Chs,2 D/A Output Chs,DC/DC Conv Incl	DTL
66♦	ST-LSI32S2X2	LSI-11	IO-42	MOD		32 SE Analog Input A/D Chs,2 D/A Output Chs,No DC/DC Conv Incl	DTL
67♦	ST-LSI-ADX32S	LSI-11	IO-42	MOD		32 SE Channel Slave A/D Multiplexer Expander	DTL
68▼	ST-LSI-RLY	LSI11	IO-41	MOD		Relay-Input A/D Board for DEC Q-Bus Computers;8 Diff A/D Chs;CMR 126dB	DTL
69	ST-6800DA4A	M6800	IO-40	MOD		4 D/A Output Chs,DC/DC Conv Incl	DTL
70	ST-6800DA4B	M6800	IO-40	MOD		4 D/A Output Chs,No DC/DC Conv	DTL
71	ST-6800DA8B	M6800	IO-40	MOD		8 D/A Output Chs,No DC/DC Conv	DTL
72♦	ST-6800A1A	M6800	IO-41	MOD		16 SE Analog Input A/D Chs,No D/A Chs,DC/DC Conv Incl	DTL
73♦	ST-6800A1B	M6800	IO-41	MOD		32 SE Analog Input A/D Chs,No D/A Chs,DC/DC Conv Incl	DTL
74♦	ST-6800A1C	M6800	IO-41	MOD		16 Diff Analog Input A/D Chs,No D/A Chs,DC/DC Conv Incl	DTL
75♦	ST-6800A2A	M6800	IO-41	MOD		16 SE Analog Input A/D Chs,No D/A Chs,No DC/DC Conv	DTL
76♦	ST-6800A2B	M6800	IO-41	MOD		32 SE Analog Input A/D Chs,No D/A Chs,No DC/DC Conv	DTL
77♦	ST-6800A2C	M6800	IO-41	MOD		16 Diff Analog Input A/D Chs,No D/A Chs,No DC/DC Conv	DTL
78	ST-6800ADX32D	M6800	IO-41	MOD		32 Diff Analog Input A/D Ch Expander Board	DTL
79	ST-6800ADX32S	M6800	IO-41	MOD		32 SE Analog Input A/D Ch Expander Board	DTL
80	ST-6800ADX48D	M6800	IO-41	MOD		48 Diff Analog Input A/D Expander Board	DTL
81	ST-6800ADX48S	M6800	IO-41	MOD		48 SE Analog Input A/D Ch Expander Board	DTL
82♦	ST-6800B1A	M6800	IO-42	MOD		16 SE Analog Input A/D Chs,2 D/A Output Chs,DC/DC Conv Incl	DTL
83♦	ST-6800B1B	M6800	IO-42	MOD		32 SE Analog Input A/D Chs,2 D/A Output Chs,DC/DC Conv Incl	DTL
84♦	ST-6800B1C	M6800	IO-42	MOD		16 Diff Analog Input A/D Chs,2 D/A Output Chs,DC/DC Conv Incl	DTL
85♦	ST-6800B2A	M6800	IO-42	MOD		16 SE Analog Input A/D Chs,2 D/A Output Chs,No DC/DC Conv	DTL
86♦	ST-6800B2B	M6800	IO-42	MOD		32 SE Analog Input A/D Chs,2 D/A Output Chs,No DC/DC Conv	DTL
87♦	ST-6800B2C	M6800	IO-42	MOD		16 Diff Analog Input A/D Chs,2 D/A Output Chs,No DC/DC Conv	DTL
88♦	ST-6800C1A	M6800	IO-42	MOD		16 SE Analog Input A/D Input A/D Chs,1 D/A Output Ch,DC/DC Conv Incl	DTL
89♦	ST-6800C1B	M6800	IO-42	MOD		32 SE Analog Input A/D Chs,1 D/A Output Ch,DC/DC Conv Incl	DTL
90♦	ST-6800C1C	M6800	IO-42	MOD		16 Diff Analog Input A/D Chs,1 D/A Output Ch,DC/DC Conv Incl	DTL
91♦	ST-6800C2A	M6800	IO-42	MOD		16 SE Analog Input A/D Chs,1 D/A Output Ch,No DC/DC Conv	DTL
92♦	ST-6800C2B	M6800	IO-42	MOD		32 SE Analog Input A/D Chs,1 D/A Output Ch,No DC/DC Conv	DTL
93♦	ST-6800C2C	M6800	IO-42	MOD		16 Diff Analog Input A/D Chs,1 D/A Output Ch,No DC/DC Conv	DTL
94	DDS32	NOVA/LSI-11	IO-40	UNIT		Data Distribution Section of System 256	DTL
95	DAS256	NOVA/LSI-11	IO-42	UNIT		Stand Alone Data Acquisition Syst for Computer I/O Analog Signals	DTL
96♦	PDAS-250	NOVA/PDP11	IO-45	UNIT		1/4 Megahertz;256 A/D Channels12 Bit Binary Res;Data Acquisition System	DTL
97	PDS-32	NOVA/PDP11	IO-45	UNIT		Co-resident w/PDAS 250;1 to 32 12-Bit D/A Channels	DTL
98	SYSTEM256	NOVA/PDP11	IO-45	UNIT	MCX	256 Expandable A/D and D/A Ch;12-14 Bits 32 Siml. Sample/Holds 100KHz	DTL
99▼	ST-724	SBC80	IO-40	MOD		4-Channel D/A and Current LoopBoard;w/12 Binary Bits of Resolution	DTL
100	ST-711RLY8D	SBC80	IO-41	MOD		Analog I/O Board For SBC80 uComputers;32S/8D A/D Chs Ne D/A Ch	DTL
101	ST-711RLY16D	SBC80	IO-41	MOD		Analog I/O Board For SBC80 uComputers;32S/16D A/D Chs No D/A Ch	DTL
102♦	ST-732	SBC80	IO-42	MOD		Analog I/O Board For SBC80 uComputers;32S/16D A/D Chs,2 D/A Ch	DTL
103	ST-800-DA4	SBC80/10,20	IO-40	MOD		4 D/A Output Chs,DC/DC Incl	DTL
104	ST-800-DA8	SBC80/10,20	IO-40	MOD		8 D/A Output Chs,Requires Ext ±15V at .32A	DTL
105	ST-800-DAX4	SBC80/10,20	IO-40	MOD		4 D/A Output Ch Expander Board	DTL
106	ST-800-DAX8	SBC80/10,20	IO-40	MOD		8 D/A Output Ch Expander Board	DTL
107	ST-800-8D	SBC80/10,20	IO-41	MOD		8 Diff Analog Input A/D Chs,No D/A Chs,DC/DC Incl	DTL
108	ST-800-16D	SBC80/10,20	IO-41	MOD		16 Diff Analog Input A/D Chs,No D/A Chs,DC/DC Incl	DTL
109	ST-800-16S	SBC80/10,20	IO-41	MOD		16 Single Ended Analog Input A/D Chs,No D/A Chs,DC/DC Incl	DTL
110	ST-800-32S	SBC80/10,20	IO-41	MOD		32 Single Ended Analog Input A/D Chs,No D/A Chs,DC/DC Incl	DTL

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	ST-800-ADX32D	SBC80/10,20	IO-41	MOD		32 Diff Analog Input A/D Ch Expander Board	DTL
2	ST-800-ADX32S	SBC80/10,20	IO-41	MOD		32 Single-Ended Analog Input A/D Ch Expander Board	DTL
3	ST-800-ADX48D	SBC80/10,20	IO-41	MOD		48 Diff Analog Input A/D Ch Expander	DTL
4	ST-800-ADX48S	SBC80/10,20	IO-41	MOD		48 Single Ended Analog Input A/D Ch Expander Board	DTL
5	BC1-1	DB8/1	COMP	MOD		Basic Controller:8 Bit Microcomp On a Card For Control,Uses 2.5MHz Z80CPU	DYB
6	PZ81	DB8/1	COMP	MOD		8 Bit Single Board Computer,Z80 CPU,2/4MHz Operation,2 Ser IO Ports	DYB
7	PZ81-1	DB8/1	COMP	MOD		8 Bit Computer On a Card Without RAM, EPROM, Serial Ports	DYB
8	DB8/1	DB8/1	COMP	UNIT		8 Bit Microcomputer System; Z 80 CPU, 32k RAM, 2 Ser /1 Par. Port	DYB
9	DB8/2-1	DB8/1	COMP	UNIT		8 Bit Microcomputer System;Z80 CPU,W/2 DD Single Sided 5in FD Drive/Cont	DYB
10	DB8/2-2	DB8/1	COMP	UNIT		8 Bit Microcomputer System;Z80 CPU,W/2 DD Double Sided 5in FD Drive/Cont	DYB
11	DC81-1	DB8/1	IO-07	MOD		Dual Density Floppy Disk Controller, S 100 Bus Compatible	DYB
12	VT801-1	DB8/1	IO-09	MOD		80 Character Video Terminal Module;S100 Bus Comp;80char x 24Line Format	DYB
13	PZ81-X3	DB8/1	IO-20	Chip		Serial I/O Port	DYB
14	PZ81-X4	DB8/1	IO-20	Chip		Dual Serial I/O Ports	DYB
15	BC1-X1	DB8/1	IO-92	MOD		Power Supply For BC1-1 Controller	DYB
16	DB8/4-1	DB8/1	PE-01	UNIT		DUAL 8in Floppy Disc Syst, W/S100 Disc Cont Mod, 2 Single Sided 8in FD Dr	DYB
17	DB8/4-2	DB8/1	PE-01	UNIT		Dual 8in Floppy Disc Syst, W/S100 Disc Cont Mod, 2 Double Sided 8in FD Dr	DYB
18	PZ81-X2	DB8/1	PROM	Chip		2k EPROM (TMS 2716)	DYB
19	BC1-X3	DB8/1	RAM	Chip		4k RAM	DYB
20	PZ81-X1	DB8/1	RAM	Chip		1k Fully Static RAM	DYB
21	MD161	DB8/1	RAM	MOD		16k Dyn RAM Mod; S 100 Bus Comp, W/DMA Cont, Cycle Time 500ns	DYB
22	MS1625	DB8/1	RAM	MOD		16k Static RAM Mod;S100 Bus Comp,W/4MHz Z80, Access Time 294ns Max	DYB
23	MS1645	DB8/1	RAM	MOD		16k Static RAM Mod;S100 Bus Comp,Access Time 494ns Max	DYB
24	MS3225	DB8/1	RAM	MOD		32k Static RAM Mod;S100 Bus Comp,W/4MHz Z80,Access Time 294ns Max	DYB
25	MS3245	DB8/1	RAM	MOD		32k Static RAM Mod;S100 Bus Comp,Access Time 494ns Max	DYB
26	BC1-X4	DB8/1	ROM	Chip		2k EPROM	DYB
27	DMS	DMS	COMP	UNIT		8 Bit Microcomputer With 2 Floppy Disks;2 RS-232 Ports,1 IEEE 488 Port	DYN
28	MMD-1MI	MMD-1	DEV	MOD		Memory Interface Board For Audio Recorder/Teleprinter;RAM,PROM,Interface	E/L
29	MMD-1	MMD-1	DEV	UNIT	MNG	8 Bit Microcomp Syst Using 8080A CPU;For Training/Devl of Hard/Software	E/L
30	MMD-2	8080A	IO-31	MOD		Fully Buff Control Address,Data Bus Decoded Memory I/O Add Line	E/L
31	Seven-X	6500	COMP	UNIT		Includes Video Processor W/Text and Graphics Modes;CRT Display;Prog. con.	ECD
32	SmartASCII	6500	PE-20	UNIT		Programmable Intelligent Terminal;BASIC is provided for standalone proc	ECD
33	INNOVATOR	INNOVATOR	COMP	MOD		8 Bit Microcomputer on a Card;Uses Z80ACPU,NOVA Host	EDSI
34▼#	EF6805P2C	EF6800	uCT	CHIP	MNG	8-Bit uComputer Unit;w/On-Chip Clock,RAM/ROM,I/O,Timer	EFCF
35▼#	EF6805P2J	EF6800	uCT	CHIP	MNG	8-Bit uComputer Unit;w/On-Chip Clock,RAM/ROM,I/O,Timer	EFCF
36▼#	EF6805P2P	EF6800	uCT	CHIP	MNG	8-Bit uComputer Unit;w/On-Chip Clock,RAM/ROM,I/O,Timer	EFCF
37▼#	EF68A00C	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes of Address:72 Instru	EFCF
38▼#	EF68A00CV	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes of Address;72 Instru	EFCF
39▼#	EF68A00P	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes of Address;72 Instru	EFCF
40▼#	EF68A00PV	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes of Address;72 Instru	EFCF
41▼#	EF68B00C	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes Address;72 Instru	EFCF
42▼#	EF68B00P	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes Address;72 Instru	EFCF
43▼#	EF6800C	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes of Address;72 Instru	EFCF
44▼#	EF6800CV	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes of Address;72 Instru	EFCF
45▼#	EF6800P	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes of Address;72 Instru	EFCF
46▼#	EF6800PV	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessing Unit;Bidir Data Bus;65k Bytes of Address;72 Instru	EFCF
47▼#	EF6802C	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessor w/Clock and RAM;Fo 1.0MHz;Fxtal 4.0MHz;128x8 Bit RAM	EFCF
48▼#	EF6802P	EF6800	CPU	CHIP	MNG	8-Bit MicroProcessor w/Clock and RAM;Fo 1.0MHz;Fxtal 4.0MHz;128x8 Bit RAM	EFCF
49▼#	EF68A21C	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 1.5MHz;Bidir;Prog Registes;	EFCF
50▼#	EF68A21CV	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 1.5MHz;Bidir;Prog Registes;	EFCF
51▼#	EF68A21P	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 1.5MHz;Bidir;Prog Registes;	EFCF
52▼#	EF68A21PV	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 1.5MHz;Bidir;Prog Registes;	EFCF
53▼#	EF68B21C	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 2.0MHz;Bidir;Prog Registes;	EFCF
54▼#	EF68B21P	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 2.0MHz;Bidir;Prog Registes;	EFCF
55▼#	EF6821C	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 1.0MHz;Prog Registes;	EFCF
56▼#	EF6821CV	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 1.0MHz;Bidir;Prog Registes;	EFCF
57▼#	EF6821P	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 1.0MHz;Bidir;Prog Registes;	EFCF
58▼#	EF6821PV	EF6800	IO-30	CHIP	MNX	Peripheral Inter Adapter;Sp 1.0MHz;Bidir;Prog Registes;	EFCF
59▼#	EFF6875C	EF6800	IO-32	CHIP	MNX	Generator/Driver Clock;Fo 2.0MHz max;2 Phase;Schottky Tech;PNP Buffered	EFCF
60▼#	EFF6875P	EF6800	IO-32	CHIP	MNX	Generator/Driver Clock;Fo 2.0MHz max;2 Phase;Schottky Tech;PNP Buffered	EFCF
61▼#	EF68A40C	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 6.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
62▼#	EF68A40CV	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 6.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
63▼#	EF68A40P	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 6.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
64▼#	EF68A40PV	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 6.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
65▼#	EF68B40C	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 8.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
66▼#	EF68B40P	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 8.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
67▼#	EF6840C	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 4.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
68▼#	EF6840CV	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 4.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
69▼#	EF6840P	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 4.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
70▼#	EF6840PV	EF6800	IO-92	CHIP	MNX	Program Timer Module;Time 4.0MHz;16 Bit Binary Counters;3 Contr Reg	EFCF
71▼#	SFF9-68A09E	SFF-6800	CPU	CHIP	MNG	8-Bit uProcessor Unit;Supports modern Prog;Position Indep,Reentrancy	EFCF
72▼#	SFF9-68A09K	SFF-6800	CPU	CHIP	MNG	8-Bit uProcessor;Unit;Supports Modern Prog;Position Indep,Reentrancy	EFCF
73▼#	SFF9-68B09E	SFF-6800	CPU	CHIP	MNG	8-Bit uProcessor;Unit;Supports Modern Prog;Position Indep,Reentrancy	EFCF
74▼#	SFF9-68B09K	SFF-6800	CPU	CHIP	MNG	8-Bit uProcessor;Unit;Supports Modern Prog;Position Indep,Reentrancy	EFCF
75▼#	SFF9-6809E	SFF-6800	CPU	CHIP	MNG	8-Bit uProcessor Unit;Supports modern Prog;Position Indep,Reentrancy	EFCF
76▼#	SFF9-6809K	SFF-6800	CPU	CHIP	MNG	8-Bit uProcessor Unit;Supports modern Prog;Position Indep,Reentrancy	EFCF
77	3000DD	SYSTEM80	RAM	MOD		Single Card Mem;16kx16,18 Or 20 Alterable To 32kx8,9 Or 10 RAM	EMM
78	3000N	SYSTEM80	RAM	MOD	MNX	Single Card Mem;16kx20 Alterable To 32kx10,Access Time 180ns	EMM
79	3400N	SYSTEM80	RAM	MOD	MNX	Single Card Mem;32kx16,18;Access Time 275ns,Cycle Time 450ns	EMM
80	EPAC6880	MICRO68	IO-08	MOD	BTX	Serial Interface Printer;RS232 Interface	EPA
81▼	PROM16		PROM	MOD		16K Prog ROM;Compat w/SBC80 Bus;VCC 5.0V at .31A;Acess Time 475ns max	ESI
82▼	PROM32		PROM	MOD		32K Prog ROM;Compat w/SBC80 Bus;VCC 5.0V at .38A;Acess Time 475ns max	ESI
83▼	RAM4		RAM	MOD		4K Bytes RAM;Compatible SBC80 (Multibus);Low Pwr Read/Write mem;VCC 5.0V	ESI
84▼	RAM4L		RAM	MOD		4K Bytes RAM;Compatible SBC80 (Multibus);Low Pwr Read/Write mem;VCC 5.0V	ESI
85▼	RAM8		RAM	MOD		8K Bytes RAM;Compatible SVC80 (Multibus);Low Pwr Read/Write mem;VCC 5.0V	ESI
86▼	RAM8L		RAM	MOD		8K Bytes RAM;Compatible SBC80 (Multibus);Low Pwr Read/Write mem;VCC 5.0V	ESI
87▼	RAM016		RAM	MOD		16K Byte RAM Bd;On Bd Refresh;8/16 Bit Mode 20 Add Bits;VCC 5.0V at 6.2A	ESI
88▼	RAM048		RAM	MOD		48K Byte RAM Bd;On Bd Refresh;8/16 Bit Mode 20 Add Bits;VCC 5.0V at 3.2A	ESI
89▼	RAM064		RAM	MOD		64K Byte RAM Bd;On Bd Refresh;8/16 Bit Mode 20 Add Bits;VCC 5.0V at 3.2A	ESI
90	PROM-16	SBC80	PROM	MOD		16kx8 PROM Board W/Sockets for Sixteen 2708 PROMS	ESI
91	PROM-32	SBC80	PROM	MOD		32kx8 PROM Board W/Sockets for Sixteen 2716 PROMS	ESI
92	RAM-4	SBC80	RAM	MOD		4kx8 RAM Board with Low Power Static RAMs	ESI
93	RAM-4L	SBC80	RAM	MOD		4kx8 RAM Board with Low Power Static RAMs/Battery Backup Capability	ESI
94	RAM-8	SBC80	RAM	MOD		8kx8 RAM Board with Low Power Static RAMs	ESI
95	RAM-8L	SBC80	RAM	MOD		8kx8 RAM Board with Low Power Static RAMs/Battery Backup Capability	ESI
96	RAM-016	SBC80	RAM	MOD		16kx8 Dynamic RAM Board	ESI
97	RAM-032	SBC80	RAM	MOD		32kx8 Dynamic RAM Board	ESI
98	RAM-048	SBC80	RAM	MOD		48kx8 Dynamic RAM Board	ESI
99	RAM-064	SBC80	RAM	MOD		64kx8 Dynamic RAM Board	ESI
100	ETC1000A	ETC1000	COMP	UNIT		8 Bit Comp Sys;Min Std;Program on ROM,8 Dig Display,KB,For Control	ETL
101	ETC1000B	ETC1000	COMP	UNIT		8 Bit Comp Sys;8k Std;Add 8k Mem;Cassette/Comm Interface,BASIC	ETL
102	ETC1000D	ETC1000	COMP	UNIT		8 Bit Comp Sys;Data Processing Sys;500k Bytes Disk Storage	ETL
103	ETC1000C	ETC1000	DEV	UNIT		8 Bit Comp Sys;16k Program Devel Sys;ETC BUS Expansion,Display	ETL
104	ETC1125	ETC1000	IO-03	MOD		Programmable Write Protection	ETL
105	ETC1046	ETC1000	IO-05	MOD		Hi-Performance Cassette I/O	ETL
106	ETC1524	ETC1000	IO-07	MOD		Dual-Drive IBM Compatible Disk and Controller	ETL
107	ETC1622	ETC1000	IO-09	MOD		ADM-3 24 Line Display Expansion	ETL
108	ETC1041	ETC1000	IO-20	MOD		2 Channel EIA Interface	ETL
109	ETC1001	ETC1000	IO-32	MOD		Precision Crystal Clock	ETL
110	ETC1020	ETC1000	IO-33	MOD		ETCBUS Expansion	ETL

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	ETC1120	ETC1000	IO-55	MOD		8192 Byte Memory	ETL
2	ETC1710	ETC1000	PE-04	UNIT		Audio Cassette Recorder and Cables	ETL
3	ETC1620	ETC1000	PE-15	UNIT		ADM-3 Keyboard Display	ETL
4♦	ETC1621	ETC1000	PE-15	UNIT		ADM-3 Lower Case Character Set	ETL
5	ETC8812	ETC1000	ROM	MOD		Communications Control PROM	ETL
6#	CPU019	E-6	COMP	MOD		One Card Computer;6809 CPU;RAM 2kBytes;ROM 32kBytes;Timer;I/O;Etc.	EURF
7#	CPU010	E-6	CPU	MOD		Processor Module;Uses 6800 CPU;RAM 640 Bytes;ROM 1024 Bytes;Ser Comm Ch	EURF
8#	PTM400/E-6	E-6	IO-01	MOD		Programmable Timer Mod;6 On Board Programmable 16 Bit Counters	EURF
9#	ACIATTY/RS532/E-6	E-6	IO-20	MOD		20mA;RS232C Standard I/O;Selectable Trans Rate 9.6kb max	EURF
10#	ADLC540/E-6	E-6	IO-20	MOD		Advanced Data Link Controller Module	EURF
11#	HP-IB210/E-6	E-6	IO-30	MOD		HP-IB210 Mod for Interface between E-6 and IEEE 488 Instrument Bus	EURF
12#	PIA201WW/E-6	E-6	IO-30	MOD		2 x 8 Bit Parallel I/O Module;Uses PIA Unit MC6820;16 IO Lines	EURF
13#	DOD202/E-6	E-6	IO-31	MOD		Relay Driver Mod;16 Relay Driver Outputs;Drives up to 200mA	EURF
14#	DII203/E-6	E-6	IO-33	MOD		Opto Isolated Input Mod;16 Inputs;10mA Current Loop	EURF
15#	DAC230/E-6	E-6	IO-40	MOD		Quad Analog Output;Vout 10V max;Io 1.0mA max;Accuracy 8 Bit	EURF
16#	ADC224/E-6	E-6	IO-41	MOD		8 Bit Quad ADC;Conversion Delay 18us;Zi 1.5MΩ	EURF
17#	EPROM308/E-6	E-6	ROM	MOD	MNX	8192 x 8 Bit EPROM Module;Eight 1024 x 8 Sockets;Power 5V,12V,-5V	EURF
18#	EPROM332/E-6	E-6	ROM	MOD		32768x8 Bit EPROM Module;Eight Sockets For 4096x8 or 2048x8 EPROMS;Pwr 5V	EURF
19#	CPU001	EURO-6	CPU	MOD		Processor Module;Uses 6800 CPU;RAM 256 Bytes;ROM 2048 Bytes;Clock 1.0MHz	EURF
20#	IOANALYSER	EURO-6	DEV	MOD		Input/Output Analyser;Analyses M6800 System PIA I/O	EURF
21#	PTM400	EURO-6	IO-01	MOD		Programmable Timer Mod;6 On Board Programmable 16 Bit Counters	EURF
22#	ACIATTY/RS532	EURO-6	IO-20	MOD		20mA;RS232C Standard I/O;Selectable Trans Rate 9.6kb max	EURF
23#	ADLC540	EURO-6	IO-20	MOD		Advanced Data Link Controller Module	EURF
24#	HP-IB210	EURO-6	IO-30	MOD		HP-IB210 Mod for Interface between EURO-6 and IEEE 488 Instrument Bus	EURF
25#	PIA201WW	EURO-6	IO-30	MOD		2 x 8 Bit Parallel I/O Module;Uses PIA Unit MC6820;16 IO Lines	EURF
26#	DOD202	EURO-6	IO-31	MOD		Relay Driver Mod;16 Relay Driver Outputs;Drives up to 200mA	EURF
27#	RELAY922	EURO-6	IO-31	MOD		Relay Mod;8 Relays,Input 12V/50mA;Op Temp 0-55°C	EURF
28#	DII203	EURO-6	IO-33	MOD		Opto Isolated Input Mod;16 Inputs;10mA Current Loop	EURF
29#	DAC230	EURO-6	IO-40	MOD		Quad Analog Output;Vout 10V max;Io 1.0mA max;Accuracy 8 Bit	EURF
30#	ADC224	EURO-6	IO-41	MOD		8 Bit Quad ADC;Conversion Delay 18us;Zi 1.5MΩ	EURF
31#	ADC228	EURO-6	IO-41	MOD		ADC Module; 8 Multiplexed Inputs; Dual Slope Conversion	EURF
32#	RAM102	EURO-6	RAM	MOD		2048 x 8 Bit RAM Module;Access Time 500ns;Power 5V at 1.0A	EURF
33#	EPROM308	EURO-6	ROM	MOD	MNX	8192 x 8 Bit EPROM Module;Eight 1024 x 8 Sockets;Power 5V,12V,-5V	EURF
34#	EPROM332	EURO-6	ROM	MOD		32768x8 Bit EPROM Module;Eight Sockets For 4096x8 or 2048x8 EPROMS;Pwr 5V	EURF
35#	CRAM108	EURO-6/E-6	RAM	MOD		8192x8 Bit CMOS RAM Module;Access Time 450nS;Battery Backup;Pwr 5 0.5A	EURF
36#	RAM108	EURO-6/E-6	RAM	MOD		8192x8 Bit RAM Module;Access Time 450nS;Power 5V 1.3A EURF	EURF
37#	CPU001M	EURO-6	CPU	MOD		Processor Module;Uses 6800 CPU;RAM 256Bytes;ROM 8192b;Clock1,oMHz	EURF
38#	SYNTE-2	SYNTE-2	COMP	IO-22		Speech Synthesizer w/unlimited Vocab;2-4k Byte EPROM,256 Byte RAM	EURF
39	DUALSTATION/12	MICROSYSTEM	COMP	UNIT		Multistation Microcomp System;Includes MICRODISK 6 or 8 W/DUALSTATION	FCC
40	DUALSYSTEM/10-10	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 10,10;W/6800,6802,8085,8080	FCC
41	DUALSYSTEM/12-10	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 12,10;W/6800,6802,8080,8085,Z80	FCC
42	DUALSYSTEM/12-12	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 12,12;W/6800,6802,8080,8085,Z80	FCC
43	DUALSYSTEM/15-10	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 15,10;W/6800,6802,8080,8085,Z80	FCC
44	DUALSYSTEM/15-12	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 15,12;W/6800,6802,8080,8085,Z80	FCC
45	DUALSYSTEM/15-15	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 15,15;W/6800,6802,8080,8085,Z80	FCC
46	DUALSYSTEM/20-10	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 20,10;W/6800,6802,8080,8085,Z80	FCC
47	DUALSYSTEM/20-12	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 20,12;W/6800,6802,8080,8085,Z80	FCC
48	DUALSYSTEM/20-15	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 20,15;W/6800,6802,8080,8085,Z80	FCC
49	DUALSYSTEM/20-20	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 20,20;W/6800,6802,8080,8085,Z80	FCC
50	DUALSYSTEM/31-10	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 31,10;W/6800,6802,8080,8085,Z80	FCC
51	DUALSYSTEM/31-12	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 31,12;W/6800,6802,8080,8085,Z80	FCC
52	DUALSYSTEM/31-15	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 31,15;W/6800,6802,8080,8085,Z80	FCC
53	DUALSYSTEM/31-20	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 31,20;W/6800,6802,8080,8085,Z80	FCC
54	DUALSYSTEM/31-31	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 31,31;W/6800,6802,8080,8085,Z80	FCC
55	DUALSYSTEM/32-10	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 32,10;W/6800,6802,8080,8085,Z80	FCC
56	DUALSYSTEM/32-12	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 32,12;W/6800,6802,8080,8085,Z80	FCC
57	DUALSYSTEM/32-15	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 32,15;W/6800,6802,8080,8085,Z80	FCC
58	DUALSYSTEM/32-20	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 32,20;W/6800,6802,8080,8085,Z80	FCC
59	DUALSYSTEM/32-31	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 32,31;W/6800,6802,8080,8085,Z80	FCC
60	DUALSYSTEM/32-32	MICROSYSTEM	COMP	UNIT		Dual Station Microcomp Systems 32,32;W/6800,6802,8080,8085,Z80	FCC
61	MICROSTATION/12	MICROSYSTEM	COMP	UNIT		Multistation Microcomp System;Includes MICRODISK 6 or 8 W/MICROSTATION	FCC
62	DUALSYSTEM/10C	MICROSYSTEM	DEV	MOD		Microsystem to Dualsystem Conversion Pkg;8080,8085,6800,6802,Z80	FCC
63	DUALSYSTEM/12C	MICROSYSTEM	DEV	MOD		Microsystem to Dualsystem Conversion Pkg;8080,8085,6800,6802,Z80	FCC
64	DUALSYSTEM/15C	MICROSYSTEM	DEV	MOD		Microsystem to Dualsystem Conversion Pkg;8080,8085,6800,6802,Z80	FCC
65	DUALSYSTEM/20C	MICROSYSTEM	DEV	MOD		Microsystem to Dualsystem Conversion Pkg;8080,8085,6800,6802,Z80	FCC
66	DUALSYSTEM/31C	MICROSYSTEM	DEV	MOD		Microsystem to Dualsystem Conversion Pkg;8080,8085,6800,6802,Z80	FCC
67	DUALSYSTEM/32C	MICROSYSTEM	DEV	MOD		Microsystem to Dualsystem Conversion Pkg;8080,8085,6800,6802,Z80	FCC
68	M8-41	MICROSYSTEM	DEV	UNIT		EPROM Programmer For 2708/2704 With Additional Debug Aid	FCC
69	MICROANALYZER	MICROSYSTEM	DEV	UNIT		Logic Analyzer;For Real Time Logic Analysis of Microprocessors	FCC
70	M8-41A/2708	MICROSYSTEM	IO-03	MOD		EPROM Programmer Personality Mod;Plugs into M8-41 Debug Mod	FCC
71	M8-41A/2716	MICROSYSTEM	IO-03	MOD		EPROM Programmer Personality Mod;Plugs into M8-41 Debug Mod	FCC
72	M8-51	MICROSYSTEM	IO-08	MOD		Printer Interface Module	FCC
73	M8-24	MICROSYSTEM	IO-20	MOD		Dual Asynchronous/Synchronous Serial I/O Module	FCC
74	M8-23	MICROSYSTEM	IO-33	MOD		Four 8 Bit Parallel I/O Port Module	FCC
75	M8-11	MICROSYSTEM	IO-55	MOD		8k PROM/2k Static RAM Module, Sockets For 2708EPROMS, 2102RAMS	FCC
76	MICRODISK2	MICROSYSTEM	PE-01	UNIT		Dual IBM Compatible Floppy Disk Drive,Formatted Cap 2.5MB/Drive	FCC
77	MICRODISK2M	MICROSYSTEM	PE-01	UNIT		Dual Mini Floppy Disk Drive,Formatted Capacity 80kB/Drive	FCC
78	MICRODISK3	MICROSYSTEM	PE-01	UNIT		Dual Drive 8 in Double Density Floppy Disk Unit;Up to 1025024 Bytes	FCC
79	MICRODISK4	MICROSYSTEM	PE-01	UNIT		Dual Drive 8 in Double Side/Density Floppy Disk Unit;To 2050048 Bytes	FCC
80	MICRODISK6	MICROSYSTEM	PE-01	UNIT		Dual Drive 8 in Double Density Intelligent Floppy Disk Unit	FCC
81	MICRODISK8	MICROSYSTEM	PE-01	UNIT		Dual Drive 8 in Double Sided,Double Density Intelligent Floppy Disk Unit	FCC
82	MICROTAPE2	MICROSYSTEM	PE-04	UNIT		Dual Cassette Tape Unit For Addition To MICROSYSTEM/20, /30	FCC
83	MICROPRINT65-FF	MICROSYSTEM	PE-10	UNIT		Dot Matrix Printer; 80 Column, 65 lpm, Friction Feed	FCC
84	MICROPRINT65-TF	MICROSYSTEM	PE-10	UNIT		Dot Matrix Printer; 80 Column, 65 lpm, Tractor Feed	FCC
85	MICROPRINTER120	MICROSYSTEM	PE-10	UNIT		Line Printer;Tractor Feed 132 Column;120cps Dot Matrix Printer	FCC
86	M8-10	MICROSYSTEM	RAM	MOD		8k Byte Dynamic RAM With Memory Write Protect	FCC
87	M8-12	MICROSYSTEM	RAM	MOD		16k Byte Dynamic RAM Module;Includes 32,4k RAM Chips	FCC
88	M8-14/32K	MICROSYSTEM	RAM	MOD		32k Byte Dynamic RAM Module;Includes 16,16k RAM Chips	FCC

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE
1	M8-14/48K	MICROSYSTEM	RAM	MOD		48k Byte Dynamic RAM Module;Includes 24,16k RAM Chips	FCC
2	M8-14/64K	MICROSYSTEM	RAM	MOD		64k Byte Dynamic RAM Module;Includes 32,16k RAM Chips	FCC
3	MICROCONTROL/10MODZ80	MSZ80	COMP	UNIT		Microcontroller; Z80 CPU Mod, PROM/RAM Mod, Power Supply	FCC
4	MICROSYSTEM/10MODZ80	MSZ80	COMP	UNIT		Complete Tape Based Microcomp Syst Using Z80, 8kB RAM,CRT,Keyboard Etc	FCC
5	MICROSYSTEM/12MODZ80	MSZ80	COMP	UNIT		Complete Tape Based Microcomp Syst Using Z80;16k Byte RAM,CRT,KB	FCC
6	MICROSYSTEM/15MODZ80	MSZ80	COMP	UNIT		Complete Mem. Based Microcomp Syst Using Z80, MICROSYSTEM/10,32k RAM	FCC
7	MICROSYSTEM/20MODZ80	MSZ80	COMP	UNIT		Complete Mini FFloppy Disk Based Microcomp System Using Z80, 16k RAM	FCC
8	MICROSYSTEM/30MODZ80	MSZ80	COMP	UNIT		Complete Floppy Disk Based Microcomp System Using Z80, 16k RAM	FCC
9	MICROSYSTEM/31MODZ80	MSZ80	COMP	UNIT		Floppy Disk Based Syst,Double Density,Using Z80;16k RAM,CRT,KB	FCC
10	MICROSYSTEM/32MODZ80	MSZ80	COMP	UNIT		Floppy Disk Based Syst;Double Density/Sided;Using Z80;16k RAM,CRT,KB	FCC
11	M8-40/Z80	MSZ80	DEV	MOD		In Ckt Emulator With Software; Used With Z80 Based System	FCC
12	M8-Z80C	MSZ80	DEV	MOD		Conversion Pkg W/CPU Mod For Adding Z80 To Existing MICROSYSTEMS	FCC
13	MICROEMULATOR/Z80	MSZ80	DEV	UNIT		Syst. Design Pkg. Incl M8-40 Emulator And M8-41 Debug/E PROM Programmer	FCC
14	MICROCONTROL/10MOD6800	MS6800	COMP	UNIT		Microcontroller; 6800 CPU Mod, PROM/RAM Mod, Power Supply	FCC
15	MICROSYSTEM/10MOD6800	MS6800	COMP	UNIT		Complete Tape Based Microcomp Syst Using 6800,8kB RAM,CRT,Keyboard Etc	FCC
16	MICROSYSTEM/12MOD6800	MS6800	COMP	UNIT		Complete Tape Based Microcomp Syst Using 6800;16k Byte RAM,CRT,KB	FCC
17	MICROSYSTEM/15MOD6800	MS6800	COMP	UNIT		Complete Mem. Based Microcomp Syst Using 6800, MICROSYSTEM/10,32k RAM	FCC
18	MICROSYSTEM/20MOD6800	MS6800	COMP	UNIT		Complete Mini Floppy Disk Based Microcomp System Using 6800, 16k RAM	FCC
19	MICROSYSTEM/30MOD6800	MS6800	COMP	UNIT		Complete Floppy Disk Based Microcomp System Using 6800,16k RAM	FCC
20	MICROSYSTEM/31MOD6800	MS6800	COMP	UNIT		Floppy Disk Based Syst,Double Density,Using 6800;16k RAM,CRT,KB	FCC
21	MICROSYSTEM/32MOD6800	MS6800	COMP	UNIT		Floppy Disk Based Syst;Double Density/Sided;Using 6800;16k RAM,CRT,KB	FCC
22	M8-40/6800	MS6800	DEV	MOD		In Ckt Emulator With Software; Used With 6800 Based System	FCC
23	M8-6800C	MS6800	DEV	MOD		Conversion Pkg W/CPU Mod For Adding 6800 To Existing MICROSYSTEMS	FCC
24	MICROEMULATOR/6800	MS6800	DEV	UNIT		Syst. Design Pkg. Incl M8-40 Emulator And M8-41 Debug/E PROM Programmer	FCC
25	MICROCONTROL/10MOD6802	MS6802	COMP	UNIT		Microcontroller;6802 CPU Mod,PROM/RAM Mod,Power Supply	FCC
26	MICROSYSTEM/10MOD6802	MS6802	COMP	UNIT		Complete Tape Based Microcomp Syst Using 6802;8k Byte RAM,CRT,KB	FCC
27	MICROSYSTEM/12MOD6802	MS6802	COMP	UNIT		Complete Tape Based Microcomp Syst Using 6802;16k Byte RAM,CRT,KB	FCC
28	MICROSYSTEM/15MOD6802	MS6802	COMP	UNIT		Complete Mem Based Microcomp Syst Using 6802;32k RAM,Quickrun Software	FCC
29	MICROSYSTEM/31MOD6802	MS6802	COMP	UNIT		Floppy Disk Based Syst,Double Density,Using 6802;16k RAM,CRT,KB	FCC
30	MICROSYSTEM/32MOD6802	MS6802	COMP	UNIT		Floppy Disk Based Syst;Double Density/Sided;Using 6802;16k RAM,CRT,KB	FCC
31	M8-40/6802	MS6802	DEV	MOD		In Ckt Emulator with Software;Used with 6802 Based Systems	FCC
32	M8-6802C	MS6802	DEV	MOD		Conversion Pkg W/CPU Mod for Adding 6802 to Existing MICROSYSTEMS	FCC
33	MICROEMULATOR/6802	MS6802	DEV	UNIT		Syst Design Pkg Incl M8-40 Emulator and M8-41 Debug Module	FCC
34	MICROCONTROL/10MOD8080	MS8080	COMP	UNIT		Microcontroller; 8080 CPU Mod, PROM/RAM Mod, Power Supply	FCC
35	MICROSYSTEM/10MOD8080	MS8080	COMP	UNIT		Complete Tape Based Microcomp Syst Using 8080,8kB RAM,CRT,Keyboard Etc	FCC
36	MICROSYSTEM/12MOD8080	MS8080	COMP	UNIT		Complete Tape Based Microcomp Syst Using 8080;16k Byte RAM,CRT,KB	FCC
37	MICROSYSTEM/15MOD8080	MS8080	COMP	UNIT		Complete Mem. Based Microcomp Syst Using 8080, Microsystem/10,32k RAM	FCC
38	MICROSYSTEM/20MOD8080	MS8080	COMP	UNIT		Complete Mini Floppy Disk Based Microcomp System Using 8080, 16k RAM	FCC
39	MICROSYSTEM/30MOD8080	MS8080	COMP	UNIT		Complete Floppy Disk Based Microcomp System Using 8080, 16k RAM	FCC
40	MICROSYSTEM/31MOD8080	MS8080	COMP	UNIT		Floppy Disk Based Syst,Double Density,Using 8080;16k RAM,CRT,KB	FCC
41	MICROSYSTEM/32MOD8080	MS8080	COMP	UNIT		Floppy Disk Based Syst;Double Density/Sided;Using 8080;16k RAM,CRT,KB	FCC
42	M8-40/8080	MS8080	DEV	MOD		In Ckt Emulator With Software; Used With 8080 Based System	FCC
43	M8-8080C	MS8080	DEV	MOD		Conversion Pkg W/CPU Mod For Adding 8080 To Existing MICROSYSTEMS	FCC
44	MICROEMULATOR/8080	MS8080	DEV	UNIT		Syst Design Pkg Incl M8-40 Emulator And M8-41 Debug/E PROM Programmer	FCC
45	MICROCONTROL/10MOD8085	MS8085	COMP	UNIT		Microcontroller;8085 CPU Mod,PROM/RAM Mod,Power Supply	FCC
46	MICROSYSTEM/10MOD8085	MS8085	COMP	UNIT		Complete Tape Based Microcomp Syst Using 8085;8k Byte RAM,CRT,KB	FCC
47	MICROSYSTEM/12MOD8085	MS8085	COMP	UNIT		Complete Tape Based Microcomp Syst Using 8085;16k Byte RAM,CRT,KB	FCC
48	MICROSYSTEM/15MOD8085	MS8085	COMP	UNIT		Complete Mem Based Microcomp Syst Using 8085;32k RAM,Quickrun Software	FCC
49	MICROSYSTEM/31MOD8085	MS8085	COMP	UNIT		Floppy Disk Based Syst,Double Density,Using 8085;16k RAM,CRT,KB	FCC
50	MICROSYSTEM/32MOD8085	MS8085	COMP	UNIT		Floppy Disk Based Syst;Double Density/Sided;Using 8085;16k RAM,CRT,KB	FCC
51	M8-40/8085	MS8085	DEV	MOD		In Ckt Emulator with Software;Used with 8085 Based Systems	FCC
52	M8-8085C	MS8085	DEV	MOD		Conversion Pkg W/CPU Mod for Adding 8085 to Existing MICROSYSTEMS	FCC
53	MICROEMULATOR/8085	MS8085	DEV	UNIT		Syst Design Pkg Incl M8-40 Emulator and M8-41 Debug Module	FCC
54	F100220A		CPU	Chip		Address and Data Interface Unit;Negative Voltage	FSC
55	F100220B		CPU	Chip		Address and Data Interface Unit;Negative Voltage	FSC
56	9409DC	F2900	CPU	Chip	BTD	4 Bit CPU Slice;5.0V Supply;Freq 10MHz max;0 to 75°C	FSC
57	9409DM	F2900	CPU	Chip	BTD	4 Bit CPU Slice;5.0V Supply;Freq 10MHz max;-55 to 125°C	FSC
58	9409PC	F2900	CPU	Chip	BTD	4 Bit CPU Slice;5.0V Supply;Freq 10MHz max;0 to 75°C	FSC
59	F2901ADC	F2900	CPU	Chip	BTD	4 Bit CPU Slice; 5.0V Supply; Freq 10 MHZ max; 0 tO 75 C°	FSC
60	F2901ADM	F2900	CPU	Chip	BTD	4 Bit CPU Slice; 5.0V Supply; Freq 10 MHZ max; -55 to 125°C	FSC
61	F2901APC	F2900	CPU	Chip	BTD	4 Bit CPU Slice;5.0V Supply;Freq 10MHz Max;0 to 75°C	FSC
62	F2909/94197Y	F2900	IO-01	Chip	BTD	Microprogram Sequencer,4-Bit Expandable Address Outputs;28 Pin Ceramic Pk	FSC
63	F2909/94199Q	F2900	IO-01	Chip	BTD	Microprogram Sequencer,4-Bit Expandable Address Outputs;28 Pin Plastic Pk	FSC
64	F2910/94204T	F2900	IO-01	Chip	BTD	Microprogram Controller,12-Bit Address (4k Pages);40 Pin Plastic Pkg	FSC
65	F2903/9413	F2900	RAM	Chip	BTD	4-Bit Slice,On Chip Parity,Expandable RAM;48 Pin Pkg	FSC
66	F6801	F6800	uCT	Chip	MNX	Single Chip Computer;with 16-Bit Timer and UART;40 Pin Pkg	FSC
67	F68A00D	F6800	CPU	Chip		8 Bit Microprocessor;MPU,Address,Interrupt;tcyc 667ns	FSC
68	F68A02D	F6800	CPU	Chip		8 Bit Microprocessor;MPU,Address,Interrupt,128x8 RAM,tcyc 667ns	FSC
69	F68B00D	F6800	CPU	Chip		8 Bit Microprocessor;MPU,Address,Interrupt;tcyc 500ns	FSC

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	F68B02D	F6800	CPU	Chip		8 Bit Microprocessor;MPU,Address,Interrupt,128x8 RAM,tcyc 500ns	FSC
2	F6800	F6800	CPU	Chip		8 Bit Microprocessor;16 Bit Address Bus,DMA And Multiple Processor;0-70°C	FSC
3	F6800C	F6800	CPU	Chip		8 Bit Microprocessor;16 Bit Address Bus,DMA Multiple Processor;-40-85°C	FSC
4	F6802D	F6800	CPU	Chip		8-Bit Microprocessor;MPU,AddreFSC Microprocessor;MPU,Addre0us,Ceramic	FSC
5	F6802P	F6800	CPU	Chip		8-Bit Microprocessor;MPU,Address,Interrupt,128x8 RAM,tcyc 1.0us,Plastic	FSC
6	F6808	F6800	CPU	Chip		Microprocessing Unit w/Clock 40 Pin Plastic ir Ceramic Pkg	FSC
7	F6809	F6800	CPU	Chip	MNX	8/16-Bit Central Processing Unit;40 Pin Pkg	FSC
8	F68A40	F6800	IO-01	Chip		Programmable Timer;5.0V Supply;PD 550mW,tcyc 667ns	FSC
9	F68B40	F6800	IO-01	Chip		Programmable Timer;5.0V Supply;PD 550mW,tcyc 500ns	FSC
10	F6840	F6800	IO-01	Chip		Programmable Timer;5.0V Supply;PD 550mW,tcyc 1.0us	FSC
11	F6844	F6800	IO-01	Chip	MNX	Direct Memory Access Controller(4-Channel)	FSC
12	F6845	F6800	IO-09	Chip	MNX	CRT Controller;40 Pin Pkg	FSC
13	F68A50D	F6800	IO-20	Chip		Async Communications Interface Adapter;24 Pin Ceramic Pkg	FSC
14	F68A50P	F6800	IO-20	Chip		Async Data Adapter;5.0V Supply;PD 300mW,tcyc 667ns	FSC
15	F68A52P	F6800	IO-20	Chip		Sync Data Adapter;5.0V Supply;PD 300mW,tcyc 667ns	FSC
16	F68A54	F6800	IO-20	Chip		Advanced Data Link CTL;5.0V Supply;tcyc 667ns	FSC
17	F68B50D	F6800	IO-20	Chip		Async Communications Interface Adapter; 24 Pin Ceramic Pkg	FSC
18	F68B50P	F6800	IO-20	Chip		Async Data Adapter;5.0V Supply;PD 300mW,tcyc 500ns	FSC
19	F68B52P	F6800	IO-20	Chip		Sync Data Adapter;5.0V Supply;PD 300mW,tcyc 500ns	FSC
20	F68B54	F6800	IO-20	Chip		Advanced Data Link CTL;5.0V Supply;tcyc 500ns	FSC
21	F3843	F6800	IO-20	Chip	MNG	USART;Universal Sync/Async Receiver Transmitter	FSC
22	F6850P	F6800	IO-20	Chip		Asynchronous Communications Interface Adapter	FSC
23	F6852P	F6800	IO-20	Chip		Sync Data Adapter;5.0V Supply;PD 300mW,tcyc 1.0us	FSC
24	F6854	F6800	IO-20	Chip		Advanced Data Link CTL;5.0V Supply;tcyc 1.0us	FSC
25	F6856DC	F6800	IO-20	Chip	MNX	Synchronous Protocol Communications Controller,F6800/8080 Compatible	FSC
26	F6856PC	F6800	IO-20	Chip	MNX	Synchronous Protocol Communications Controller,F6800/8080 Compatible	FSC
27	F6860P	F6800	IO-20	Chip		0-600BPS Modem;5.0V Supply;PD 325mW	FSC
28	F6862P	F6800	IO-20	Chip		2400BPS Modulator;5.0V Supply;PD 300mW	FSC
29	F6850D	F6800	IO-21	Chip	MNX	Asynchronous Communications Interface Adapter;24 Pin,Ceramic Pkg	FSC
30	F6852D	F6800	IO-21	Chip	MNX	Synchronous Serial Data Adapter;24 Pin Ceramic Pkg	FSC
31	F68A21D	F6800	IO-30	Chip		Parallel I/O:16 Lines,5.0V Supply;PD 550mW,tcyc 667ns	FSC
32	F68A21P	F6800	IO-30	Chip		Peripheral Interface Adapter;40 Pin Plastic Pkg	FSC
33	F68B21D	F6800	IO-30	Chip		Parallel I/O:16 Lines,5.0V Supply;PD 550mW,tcyc 500ns	FSC
34	F68B21P	F6800	IO-30	Chip		Peripheral Interface Adapter;40 Pin Plastic Pkg	FSC
35	F6820P	F6800	IO-30	Chip		Peripheral Interface	FSC
36	F6821D	F6800	IO-30	Chip		Parallel I/O:16 Lines,5.0V Supply;PD 550mW,tcyc 1.0us	FSC
37	F96LS488	F6800	IO-33	Chip		IEEE488 Instrument Bus Interface,Single 5V Supply	FSC
38	F68488D	F6800	IO-33	Chip		GPIA (IEEE Bus) 5V;Supply 40 Pin Ceramic Pkg	FSC
39	F68488P	F6800	IO-33	Chip		GPIA (IEEE Bus) 5V;Supply 40 Pin Plastic Pkg	FSC
40	F68A46D	F6800	IO-57	Chip		2kx8 ROM,I/O,Timer;5.0V Supply;PD 800mW,tcyc 667ns	FSC
41	F68B46D	F6800	IO-57	Chip		2kx8 ROM,I/O,Timer;5.0V Supply;PD 800mW,tcyc 500ns	FSC
42	F6846	F6800	IO-57	Chip		ROM-I/O-Timer;2048-Bytes Mask Programmable ROM,8-Bit Bi-di Data Port	FSC
43	F6846D	F6800	IO-57	Chip		2kx8 ROM,I/O,Timer;5.0V Supply;PD 800mW,tcyc 1.0us	FSC
44	F6843	F6800	PE-01	Chip	MNX	Floppy Disk Controller;40 Pin Pkg	FSC
45	F6847	F6800	PE-15	Chip	MNX	Video Sync Generator	FSC
46	F68708	F6800	PE-51	Chip	MNX	1024x8-Bit UV EPRON,1k-Bytes ROM;24 Pin Pkg	FSC
47	F68716	F6800	PE-51	Chip	MNX	2048x8-Bit UV EPROM,2k-Bytes ROM;24 Pin Pkg	FSC
48	F68A10D	F6800	RAM	Chip		128x8 Static RAM; 24Pin Ceramic Pkg	FSC
49	F68A10P	F6800	RAM	Chip		128x8 RAM	FSC
50	F68B10D	F6800	RAM	Chip		128x8 Static RAM; 24Pin Ceramic Pkg	FSC
51	F68B10P	F6800	RAM	Chip		128x8 Static RAM;5.0V Supply;PD 400mW;tacc 250ns	FSC
52	F6810-1P	F6800	RAM	Chip		128x8 Static RAM; 5.0V Supply; PD 400 m W; t ac 350ns	FSC
53	F6810P	F6800	RAM	Chip		128x8 Static RAM;5.0V Supply;PD 350mW;tac 450ns	FSC
54	F6814	F6800	RAM	Chip	MNX	1024x4-Bit Random Access Memory(2114 Type)1k-Bytes EX RAM;18Pin Pkg	FSC
55	F6816	F6800	RAM	Chip	MNX	16k x 1-Bit Dynamic Random Access Memory(F16k Type);16k EX RAM;16Pin Pkg	FSC
56	F68A308P	F6800	ROM	Chip		1kx8 Mask Progrm ROM;5.0V Supply;PD 650mW,tacc 360ns	FSC
57	F68A316P	F6800	ROM	Chip		2kx8 Mask Progrm ROM;5.0V Supply;tacc 360ns	FSC
58	F68B308P	F6800	ROM	Chip		1kx8 Mask Progrm ROM;5.0V Supply;PD 650mW,tacc 250ns	FSC
59	F68B316P	F6800	ROM	Chip		2kx8 Mask Progrm ROM;5.0V Supply;tacc 250ns	FSC
60	F68308P	F6800	ROM	Chip		1kx8 Mask Progrm ROM;5.0V Supply;PD 650mW,tacc 500ns	FSC
61	F68316P	F6800	ROM	Chip		2kx8 Mask Progrm ROM;5.0V Supply;tacc 500ns	FSC
62	F38E70DC	F8	uCT	Chip	MNI	8-Bit ucomputer w/2k Bytes EPROM;40 Pin Ceramic Pkg, 0° to 70°C	FSC
63	F38E70DL	F8	uCT	Chip		8-Bit ucomputer w/2k Bytes EPROM;40 Pin Ceramic Pkg,-40° to 85°C	FSC
64	F38E70DM	F8	uCT	Chip		8-Bit ucomputer w/2k Bytes EPROM:40 Pin Ceramic Pkg,-55 to 125°C	FSC
65	F38E70PC	F8	uCT	Chip		8-Bit ucomputer w/2k Bytes EPROM;40 Pin Plastic Pkg, 0° to 70°C	FSC
66	F38E70PL	F8	uCT	Chip		8-Bit ucomputer w/2k Bytes EPROM;40 Pin Plastic Pkg,40 to 85°C	FSC
67	F38E70PM	F8	uCT	Chip		8-Bit ucomputer w/2k Bytes EPROM;40 Pin Plastic Pkg,-55 to 125°C	FSC
68	F3870	F8	uCT	Chip	MNG	8 Bit Microcomputer On A Single MOS Integrated Circuit	FSC
69	F3870DC	F8	uCT	Chip	MNG	8-Bit uComputer w/2048k Bytes of Mask Programmable ROM	FSC
70	F3870DL	F8	uCT	Chip	MNG	8-Bit uComputer w/2048k Bytes of Mask Programmable ROM	FSC
71	F3870DM	F8	uCT	Chip	MNG	8-Bit uComputer w/2048k Bytes of Mask Programmable ROM	FSC
72	F3870PC	F8	uCT	Chip	MNG	8-Bit uComputer w/2048k Bytes of Mask Programmable ROM	FSC
73	F3872	F8	uCT	Chip	MNX	Single Chip Computer;128-Bytes Scratchpad RAM,4k-Bytes ROM;40 Pin Pkg	FSC
74	F3872DC	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
75	F3872DL	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
76	F3872DM	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
77	F3872PC	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
78	F3874	F8	uCT	Chip	MNX	Single Chip Computer;64-Bytes Scratchpad RAM,4k-Bytes ROM;40 Pin Pkg	FSC
79	F3876	F8	uCT	Chip	MNX	Single Chip Computers;128-Bytes Scratchpad RAM,2k-Bytes ROM;40 Pin Pkg	FSC
80	F3876DC	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
81	F3876DL	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
82	F3876DM	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
83	F3876PC	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
84	F3876PL	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
85	F3876PM	F8	uCT	Chip	MNG	Identical to F3870 Except Memory Expansion and the Right Mem Addr Regis	FSC
86	F3878DC	F8	uCT	Chip	MNG	Identical to F3870 Except 4k Bytes of ROM	FSC
87	F3878DL	F8	uCT	Chip	MNG	Identical to F3870 Except 4k Bytes of ROM	FSC
88	F3878DM	F8	uCT	Chip	MNG	Identical to F3870 Except 4k Bytes of ROM	FSC
89	F3878PC	F8	uCT	Chip	MNG	Identical to F3870 Except 4k Bytes of ROM	FSC
90	F3878PM	F8	uCT	Chip	MNG	Identical to F3870 Except 4k Bytes of ROM and the Right Mem Addr Regis	FSC
91	F895089005	F8	uCT	MOD		One Card uC W/CPU,F8 PSU;1k Bytes RAM,2k-Bytes EPROM,2-k-Bytes PROM	FSC
92	F895080303	F8	COMP	MOD		Processor Module;CPU,PSU, Static/Dynamic/1k-Byte Ram Memory	FSC
93	OCM-1	F8	COMP	MOD		Complete Microcomputer System On A Single Board,Based On F8,Formulator	FSC
94	3850	F8	CPU	Chip	MNX	CPU;8 Bit ALU,Interrupt Control	FSC
95	F895080500	F8	CPU	MOD		Processor Module,Uses 3850CPU,3852DMI,3853SMI	FSC
96	F8-ASSEMBLEDKIT	F8	DEV	MOD	MNX	Assembled,Tested uComp Board W/32I/O Bits,2 Int Lev,2 Timers,Control Ckts	FSC
97	FORMULATORMKI	F8	DEV	UNIT		Development System For F8:Hardware/Software Devl;I/O Device/Bit 16/8	FSC
98	FORMULATORMKII	F8	DEV	UNIT		Development System For F8:Hardware/Software Devl;I/O Device/Bit 16/8	FSC
99	FORMULATORMKIIFD	F8	DEV	UNIT		Floppy Disk Based Devl Syst:Hard/Software Development	FSC
100	FORMULATORMKIII	F8	DEV	UNIT		Development System For F8:Hardware/Software Devl;I/O Device/Bit 24/8	FSC
101	FORMULATORMKIIIFD	F8	DEV	UNIT		Floppy Disk Based Devl Syst:Hard/Software Devel,Addl PROM/Comm Mod	FSC
102	3856	F8	IO-01	Chip	MNX	2.0k Program Storage Unit (PSU):16 I/O Lines And Interrupt Level	FSC
103	3857	F8	IO-01	Chip	MNX	2.0k Program Storage Unit (PSU)With Interrupt Level And Add Lines	FSC
104	F3899	F8	IO-01	Chip		Program Storage Unit (PSU);Contains 1024 Byte ROM,Counter,Reg	FSC
105	3852	F8	IO-03	Chip	MNX	Dynamic Memory Interface	FSC
106	3853	F8	IO-03	Chip	MNX	Static Memory Interface	FSC
107	3854	F8	IO-03	Chip	MNX	Direct Memory Access	FSC
108	F3853	F8	IO-03	Chip	MNX	Static Memory Interface;40 PinPkg	FSC

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	F3854	F8	IO-03	Chip	MNX	Direct Memory Access;40 Pin Pkg	FSC
2	F895085004	F8	IO-03	MOD		DMA/DISC Interface Provides DMA Channel To Shugart 3900 Floppy Disk	FSC
3	F895089003	F8	IO-09	MOD		I/O Light Display Board	FSC
4	F3846DC	F8	IO-20	Chip	MNX	Synchronous Protocol Communications Controller,DATA Rate DC To IMB/S	FSC
5	F3846PC	F8	IO-20	Chip	MNX	Synchronous Protocol Communications Controller,DATA Rate DC To IMB/s	FSC
6	F895085001	F8	IO-20	MOD		Communications Module For 3 Serial Microcomputer Peripheral Devices	FSC
7	3861	F8	IO-30	Chip	MNX	Peripheral I/O Device (PIO):Each PIO Adds 16B I/O,Timer	FSC
8	F3861	F8	IO-30	Chip	MNX	Peripheral Input/Output Unit;40 Pin Pkg	FSC
9	F3871	F8	IO-30	Chip		Peripheral I/O Device(PIO);Contains Two 8 Bit I/O Ports	FSC
10	F95050022	F8	IO-33	MOD		Quad I/O Module for F8 I/O,for F3870 Use F895089926 Cable	FSC
11	F895085002	F8	IO-33	MOD		Quad I/O Port Module,Uses Two 3851 PSU Devices	FSC
12	F895085007	F8	IO-33	MOD		Byte Parallel Interface Module,For 8 Or 16 Bit Data	FSC
13	F38T56	F8	IO-55	Chip	MNX	Program Storage Unit with F3870 Timer;40 Pin Pkg	FSC
14	F38T57	F8	IO-55	Chip	MNX	Program Storage Unit/Static Memory Interface;F3870 Timer	FSC
15	F3850	F8	IO-55	Chip	MNX	Program Storage Unit;1k-ROM,2 I/O Ports,40 Pin Pkg	FSC
16	F3856	F8	IO-55	Chip	MNX	Program Storage Unit;2k-Bytes ROM, 2 I/O Ports;40 Pin Pkg	FSC
17	F3856DC	F8	IO-57	Chip	MNX	2k Program Storage Unit;40 Pin Ceramic Pkg, 0° to 79°C	FSC
18	F3856DL	F8	IO-57	Chip	MNX	2k Program Storage Unit;40 Pin Ceramic Pkg,-40° to 85°C	FSC
19	F3856DM	F8	IO-57	Chip	MNX	2k Program Storage Unit;40 Pin Ceramic Pkg,-55 to 125°C	FSC
20	F3856PC	F8	IO-57	Chip	MNX	2k Program Storage Unit;40 Pin Plastic Pkg, 0° to 70°C	FSC
21	F3856PL	F8	IO-57	Chip	MNX	2k Program Storage Unit;40 Pin Plastic Pkg,-40° to 85°C	FSC
22	F3856PM	F8	IO-57	Chip	MNX	2k Program Storage Unit;40 Pin Plastic Pkg,-5° to 125°C	FSC
23	F3857DC	F8	IO-57	Chip	MNX	2k Program Storage Unit/Static Mem Interface;40p Cer Pkg,0° to 70°C	FSC
24	F3857DL	F8	IO-57	Chip	MNX	2k Program Storage Unit/Static Mem Interface; 40p Cer Pkg,-40° to 85°C	FSC
25	F3857DM	F8	IO-57	Chip	MNX	2k Program Storage Unit/Static Mem Interface;40p Cer Pkg,-55° to 125°C	FSC
26	F3857PC	F8	IO-57	Chip	MNX	2k Program Storage Unit/Static Mem Interface;40p Pl Pkg 0° to 70°C	FSC
27	F3857PL	F8	IO-57	Chip	MNX	2k Program Storage Unit/Static Mem Interface;40 Pin Pls Pkg,-40° to 85°C	FSC
28	F3857PM	F8	IO-57	Chip	MNX	2k Program Storage Unit/Static Mem Interface;40 Pin Pls Pkg,-55° to 125°C	FSC
29	F897380300	F8	IO-92	MOD		Formulator Base Board,9 Slots For Formulator Module,4 More Slots	FSC
30	F895082025	F8	PE-01	UNIT		iCOM FD3712 Dual Floppy Disk; European Style	FSC
31	F895082026	F8	PE-01	UNIT		iCOM FD3712 Dual Floppy Disk	FSC
32	F895080778	F8	PE-10	UNIT		Impact Printer,w/Tractor Feed; Centronics Model 799; European Style	FSC
33	F895080779	F8	PE-10	UNIT		Impact Printer, w/Tractor Feed; Centronics Model 799	FSC
34	F895081500	F8	PE-15	UNIT		Hazeltine Model 1500 Video Display Terminal	FSC
35	F895086001	F8	PE-50	MODS		PROM Programmer;Plugs into Quad I/O Module	FSC
36	F895081499	F8	PEΩ15	UNIT		Hazeltine Model 1500 Video Display Terminal; European Style	FSC
37	F895084001	F8	PROM	MOD		4k Byte PROM Module,16 Sockets For 93446 PROM Devices	FSC
38	F895084002	F8	PROM	MOD		16k Byte PROM Module,32 Sockets For 93448 PROM Devices	FSC
39	3538FDC	F8	RAM	Chip	MNX	256 x 4 Static Random Access Memory,Temp 0 To 70°C	FSC
40	3538FDL	F8	RAM	Chip	MNX	256 x 4 Static Random Access Memory,Temp -55 To 85°C	FSC
41	3538FDM	F8	RAM	Chip	MNX	256 x 4 Static Random Access Memory,Temp -55 To 125°C	FSC
42	21021DC	F8	RAM	Chip	MNX	1024 x 1 Static Random Access Memory,Temp 0 To 70°C	FSC
43	21021DL	F8	RAM	Chip	MNX	1024 x 1 Static Random Access Memory,Temp -55 To 85°C	FSC
44	21021DM	F8	RAM	Chip	MNX	1024 x 1 Static Random Access Memory,Temp -55 To 125°C	FSC
45	21022DC	F8	RAM	Chip	MNX	1024 x 1 Static Random Access Memory,Temp 0 To 70°C	FSC
46	21022DL	F8	RAM	Chip	MNX	1024 x 1 Static Random Access Memory,Temp -55 To 85°C	FSC
47	21022DM	F8	RAM	Chip	MNX	1024 x 1 Static Random Access Memory,Temp -55 To 125°C	FSC
48	35381DC	F8	RAM	Chip	MNX	256 x 4 Static Random Access Memory,Temp 0 To 70°C	FSC
49	35381DL	F8	RAM	Chip	MNX	256 x 4 Static Random Access Memory,Temp -55 To 85°C	FSC
50	35381DM	F8	RAM	Chip	MNX	256 x 4 Static Random Access Memory,Temp -55 To 125°C	FSC
51	35382DC	F8	RAM	Chip	MNX	256 x 4 Static Random Access Memory,Temp 0 To 70°C	FSC
52	35382DL	F8	RAM	Chip	MNX	256 x 4 Static Random Access Memory,Temp -55 To 85°C	FSC
53	35382DM	F8	RAM	Chip	MNX	256 x 4 Static Random Access Memory,Temp -55 To 125°C	FSC
54	F895082004	F8	RAM	MOD		4k Byte RAM Module,Uses 2102 Static N-Channel And 74LS-Series Logic Dev	FSC
55	F895083016	F8	RAM	MOD		16k-Byte RAM Module; Compatible w/all Formulator Bus Signals	FSC
56	3516	F8	ROM	Chip	MNX	2k x 8 MOS Read Only Memory	FSC
57	3851	F8	ROM	Chip	MNX	Program Storage Unit(PSU);1024 x 8 ROM,Program Timer	FSC
58	MICROPRO	MICROPRO	COMP	MOD		Assembled Computer On One Card	FSC
59	F2910/94206I	2900	IO-01	Chip	BTD	Microprogram Controller,12-Bit Address (4k Pages);40 Pin Ceramic Pkg	FSC
60	F2911/9421	2900	IO-01	Chip	BTD	Microprogram Sequencer,4-Bit Expandable Address Outputs;20 Pin Pkg	FSC
61	F2914/94244I	2900	IO-02	Chip	BTD	Vectored Priority Interrupt Controller;40 Pin Plastic Pkg	FSC
62	F2914/94244T	2900	IO-02	Chip	BTD	Vectored Priority Interrupt Controller;40 Pin Plastic Pkg	FSC
63	F2914/94246I	2900	IO-02	Chip	BTD	Vectored Priority Interrupt Controller;40 Pin Ceramic Pkg	FSC
64	F2905/94157R	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Ceramic Pkg	FSC
65	F2905/94159N	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Plastic Pkg	FSC
66	F2906/94167R	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Ceramic Pkg	FSC
67	F2906/94169N	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Plastic Pkg	FSC
68	F2907/94177R	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Ceramic Pkg	FSC
69	F2907/94179N	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Plastic Pkg	FSC
70	F2915/94257R	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Ceramic Pkg	FSC
71	F2915/94259N	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Plastic Pkg	FSC
72	F2916/94267R	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Ceramic Pkg	FSC
73	F2916/94269N	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Plastic Pkg	FSC
74	F2917/94277R	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Ceramic Pkg	FSC
75	F2917/94279N	2900	IO-21	Chip	BTD	Quad Transceiver;24 Pin Plastic Pkg	FSC
76	F297057Y	2900	IO-55	Chip	BTD	Dual Port Registor,64-Bit Registor File;28 Pin Plastic Pkg	FSC
77	F297059Q	2900	IO-55	Chip	BTD	Dual Port Registor,64-Bit Register File;28 Pin Plastic Pkg	FSC
78	4702BDC	4700	IO-20	Chip	MCG	Programmable Bit-Rate Generator;Ceramic Dip;-40 to 85°C	FSC
79	4702BDM	4700	IO-20	Chip	MCG	Programmable Bit-Rate Generator;Ceramic Dip;-55 to 125°C	FSC
80	4702BFC	4700	IO-20	Chip	MCG	Programmable Bit-Rate Generator;Flatpack;-40 to 85°C	FSC
81	4702BFM	4700	IO-20	Chip	MCG	Programmable Bit-Rate Generator;Flatpack;-55 to 125°C	FSC
82	4702BPC	4700	IO-20	Chip	MCG	Programmable Bit-Rate Generator;Plastic Dip;-40 to 85°C	FSC
83	4703BDC	4700	IO-55	Chip	MCG	16x4 Bit Ser/Par FIFO Buffer Memory;Ceramic Dip;-40 to 85°C	FSC
84	4703BDM	4700	IO-55	Chip	MCG	16x4 Bit Ser/Par FIFO Buffer Memory;Ceramic Dip;-55 to 125°C	FSC
85	4703BFC	4700	IO-55	Chip	MCG	16x4 Bit Ser/Par FIFO Buffer Memory;Flatpack;-40 to 85°C	FSC
86	4703BFM	4700	IO-55	Chip	MCG	16x4 Bit Ser/Par FIFO Buffer Memory;Flatpack;-55 to 125°C	FSC
87	4703BPC	4700	IO-55	Chip	MCG	16x4 Bit Ser/Par FIFO Buffer Memory;Plastic Dip;-40 to 85°C	FSC
88	4710BDC	4700	RAM	Chip	MCG	Register Stack:16x4 RAM W/Output Latch;Ceramic Dip;-40 to 85°C	FSC
89	4710BDM	4700	RAM	Chip	MCG	Register Stack:16x4 RAM W/Output Latch;Ceramic Dip;-55 to 125°C	FSC
90	4710BPC	4700	RAM	Chip	MCG	Register Stack:16x4 RAM W/Output Latch;Plastic Dip;-40 to 85°C	FSC
91	9405ADC	9400	CPU	Chip	BIX	Arith Logic Reg Stack;4 Bit ALU,8x4 RAM,Cont Logic;Cer Dip;0 to 75°C	FSC
92	9405ADM	9400	CPU	Chip	BIX	Arith Logic Reg Stack;4 Bit ALU,8x4 RAM,Cont Logic;Cer Dip;-55 to 125°C	FSC
93	9405APC	9400	CPU	Chip	BIX	Arith Logic Reg Stack;4 Bit ALU,8x4 RAM,Cont Logic;Plastic Dip;0 to 75°C	FSC
94	9406DC	9400	IO-01	Chip	BTD	16x4 Push-Down Pop-Up Program Stack;Ceramic Dip,0-75°C	FSC
95	9406DM	9400	IO-01	Chip	BTD	16x4 Push-Down Pop-Up Program Stack;Ceramic Dip,-55-125°C	FSC
96	9406PC	9400	IO-01	Chip	BTD	16x4 Push-Down Pop-Up Program Stack;Plastic Dip,0-75°C	FSC
97	9408ADC	9400	IO-01	Chip	BIX	Microprogram Sequencer;10 Bit Program Counter;4 Level Stack;Freq 10MHz	FSC
98	9408ADM	9400	IO-01	Chip	BIX	Microprogram Sequencer;10 Bit Program Counter;4 Level Stack;Freq 10MHz	FSC
99	9408APC	9400	IO-01	Chip	BIX	Microprogram Sequencer;10 Bit Program Counter;4 Level Stack;Freq 10MHz	FSC
100	9408DC	9400	IO-01	Chip	BIX	Microprogram Sequencer;10 Bit Program Counter;4 Level Stack;Freq 7MHz	FSC
101	9408DM	9400	IO-01	Chip	BIX	Microprogram Sequencer;10 Bit Program Counter;4 Level Stack;Freq 7MHz	FSC
102	9408PC	9400	IO-01	Chip	BIX	Microprogram Sequencer;10 Bit Program Counter;4 Level Stack;Freq 7MHz	FSC
103	9404DC	9400	IO-12	Chip	BTD	Data Path Switch,Combinatorial Array;Ceramic Dip,0-75°C	FSC
104	9404DM	9400	IO-12	Chip	BTD	Data Path Switch,Combinatorial Array;Ceramic Dip,-55-125°C	FSC
105	9404PC	9400	IO-12	Chip	BTD	Data Path Switch,Combinatorial Array;Plastic Dip,0-75°C	FSC
106	9401DC	9400	IO-20	Chip	BIX	16 Bit Cyclic Redundancy Generator/Checker;Cer Dip;0 to 75°C	FSC
107	9401DM	9400	IO-20	Chip	BIX	16 Bit Cyclic Redundancy Generator/Checker;Cer Dip;-55 to 125°C	FSC
108	9401PC	9400	IO-20	Chip	BIX	16 Bit Cyclic Redundancy Generator/Checker;Plastic Dip;0 to 75°C	FSC
109	9411DC	9400	IO-20	Chip	BTX	16 Bit Cyclic Redundancy Generator/Checker;Cer Dip;0 to 75°C	FSC
110	9411DM	9400	IO-20	Chip	BTX	16 Bit Cyclic Redundancy Generator/Checker;Cer Dip;-55 to 125°C	FSC

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	9411FM	9400	IO-20	Chip	BTX	16 Bit Cyclic Redundancy Generator/Checker;Flat Pack;-55 to 125°C	FSC
2	9411PC	9400	IO-20	Chip	BTX	16 Bit Cyclic Redundancy Generator/Checker;Plastic Dip;0 to 75°C	FSC
3	9414D	9400	IO-22	Chs	BXD	4-Chip Data Encryption Set	FSC
4	9407DC	9400	IO-55	Chip	BTD	Data Access Register;Three 4 Bit Registers;Ceramic Dip,0-75°C	FSC
5	9407DM	9400	IO-55	Chip	BTD	Data Access Register;Three 4 Bit Registers;Ceramic Dip,-55-125°C	FSC
6	9407PC	9400	IO-55	Chip	BTD	Data Access Register;Three 4 Bit Registers;Plastic Dip,0-75°C	FSC
7	9423DC	9400	IO-55	Chip	BIX	First-In-First Out(FIFO) Buffer Mem;64x4 Bit Ser/Par;0 to 75°C	FSC
8	9423DM	9400	IO-55	Chip	BIX	First-In-First Out(FIFO) Buffer Mem;64x4 Bit Ser/Par;-55 to 125°C	FSC
9	9423PC	9400	IO-55	Chip	BIX	First-In-First Out(FIFO) Buffer Mem;64x4 Bit Ser/Par;0 to 75°C	FSC
10	9410DC	9400	RAM	Chip	BTD	Register Stack,16x4 RAM W/3 State Outp Reg;Ceramic Dip,0-75°C	FSC
11	9410DM	9400	RAM	Chip	BTD	Register Stack,16x4 RAM W/3 State Outp Reg;Ceramic Dip,-55-125°C	FSC
12	9410PC	9400	RAM	Chip	BTD	Register Stack,16x4 RAM W/3 State Outp Reg;Plastic Dip,0-75°C	FSC
13	SPARK-I/O	9440	IO-01	MOD		General Purpose I/O Controller; Interfaces to SPARK-16 Board	FSC
14	SPARK-MEM	9440	IO-33	MOD		Expansion Board;Interfaces Directly to SPARK-16 Microcomputer	FSC
15	9445	9445	CPU	Chip	BIX	16-Bit Bipolar Microprocessor Microflame;Double Word(32-Bit)Inst	FSC
16	F3857	F8	IO-55	Chip	MNX	Program Storage Unit/Static MeFSC am Storage Unit/Static Me I/O Ports	FSCN
17	GA16/110	GA16	COMP	MOD	MNX	Computer On Plug-In Card With CPU,Memory And I/O	GEN
18	GA16/220	GA16	COMP	MOD	MNX	2 Card System;Basic GA16/110 Computer With More I/O,Operator Controls,	GEN
19	1579	GA16	IO-03	MOD		DMA Sync. Data Link Comm. (SDLC) Controller	GEN
20	1561	GA16	IO-20	MOD		Asynchronous Communications Controller,75-9600 Baud	GEN
21	1571	GA16	IO-20	MOD		Asynchronous Communications Controller,2000-9600 Baud	GEN
22	1575	GA16	IO-20	MOD		Synchronous Data Communications Multiplexer,16 Line	GEN
23	1578	GA16	IO-20	MOD		Programmed IO Sync. Data Link Communications(SDLC) Controller	GEN
24	1581	GA16	IO-20	MOD		Asynchronous Communications Controller,75-7600 Baud	GEN
25	1415-0101	GA16	IO-33	MOD		Optically Isolated Digital Input Controller,DTL-TTL	GEN
26	1415-0102	GA16	IO-33	MOD		Optically Isolated Digital Input Controller,24 Volt	GEN
27	1615-0220	GA16	IO-90	MOD		Arithmetic Processing Unit,Floating Pt And Double Precision Integ	GEN
28	3355-1000	GA16	PE-20	UNIT		Line Printer/Card Reader And Controller;600Lpm Printer,600Cpm Reader	GEN
29	3356-1000	GA16	PE-20	UNIT		Line Printer/Card Reader And Controller;600Lpm Printer,400Cpm Reader	GEN
30	3357-1000	GA16	PE-20	UNIT		Line Printer/Card Reader And Controller;600Lpm Printer,300Cpm Reader	GEN
31	3358-1000	GA16	PE-20	UNIT		Line Printer/Card Reader And Controller; 6 or 8 Lines Per Inch	GEN
32	3353-1010	GA16	PE-24	UNIT		Line Printer And Controller,600 Lines Per Minute	GEN
33	3353-1011	GA16	PE-24	UNIT		Line Printer And Controller,With 6/8 Lines/In Option	GEN
34	3354-1000	GA16	PE-24	UNIT		Line Printer And Controller,125 Lpm	GEN
35	3354-1200	GA16	PE-24	UNIT		Line Printer And Controller,With 6/8 Lines/In Option,200Lpm	GEN
36	3314-1000	GA16	PE-40	UNIT		Card Punch And Controller,Includes Printing And Interpreter Functions	GEN
37	3314-1001	GA16	PE-40	UNIT		Card Punch And Controller,35 Cards Per Minute	GEN
38	3315-1000	GA16	PE-40	UNIT		Card Reader And Controller;285 Cards Per Minute	GEN
39	3316-1000	GA16	PE-40	UNIT		Card Reader And Controller;400 Cards Per Minute	GEN
40	3317-1000	GA16	PE-40	UNIT		Card Reader And Controller;600 Cards Per Minute	GEN
41	3318-1000	GA16	PE-40	UNIT		Card Reader And Controller;1000 Cards Per Minute	GEN
42	MC8000	GIC8000	COMP	MOD	MPN	8 Bit Microcomputer Module	GIC
43	OS8000	GIC8000	DEV	MOD		System Monitor Module	GIC
44	GIC8000	GIC8000	DEV	UNIT	MPN	8 Bit Microcomputer System For Progm Development Uses LP8000 uProc	GIC
45	IO8000	GIC8000	IO-04	MOD		TTY/RDR-PCH Module	GIC
46	CC8000	GIC8000	IO-31	MOD		Front Panel Driver Module	GIC
47	GP8000	GIC8000	IO-33	MOD		General Purpose I/O Module	GIC
48	RM8000	GIC8000	RAM	MOD		2kx8 User RAM Module	GIC
49	PM8000	GIC8000	ROM	MOD		2kx8 User PROM Module	GIC
50	GIMINI	GIMINI	COMP	UNIT		16 Bit Microcomputer System	GIC
51	GIMINIII	GIMINI	COMP	UNIT		16 Bit Microcomputer System W/Integral Power Supply	GIC
52	MC1600	GIMINI	CPU	MOD	MNI	Basic Microcomputer Module Uses CP1600,9.75x9.25x.062 In PCB	GIC
53	MC1610	GIMINI	CPU	MOD		CP1610 With Monitor Operating System	GIC
54	PP1610	GIMINI	DEV	MOD		PROM Programmer Module For Two 2708 Or 2716 UV PROMS	GIC
55	CC1600	GIMINI	IO-09	MOD	MNI	Control Panel Module And Operators Console	GIC
56	GP1600	GIMINI	IO-33	MOD	MNI	General Purpose I/O Module,Interfacing Card	GIC
57	I/O1600	GIMINI	IO-33	MOD	MNI	Input/Output Module On 9.75 x 9.25 x .062 In PCB	GIC
58	I/O1610	GIMINI	IO-33	MOD		Floppy Disc If Board;Two Serial,One Parallel I/O Port,W/Interrupt Logic	GIC
59	DA1600	GIMINI	IO-40	MOD		12 Bit 4D/As, ±10Volts	GIC
60	AD1600	GIMINI	IO-41	MOD		Analog To Digital Converter 12 Bit,16 Channel Input	GIC
61	PM1600	GIMINI	PROM	MOD	MNI	4k PROM Card,Sockets For 512 x 8 PROM Chips	GIC
62	RM1601	GIMINI	RAM	MOD	MNI	8k x 16 RAM Module;32 4096 x 1 On 9.75 x 9.25 x .062 In PCB	GIC
63	RM1602	GIMINI	RAM	MOD		8kx16 RAM Memory Module,Read Time 400ns,Cycle Time 500ns	GIC
64	RM1610	GIMINI	RAM	MOD		RAM on Card;Selectable 8k/16k/32k x 16 Memory	GIC
65	PIC1645	PIC1650	uCT	Chip		PIC1650But With Less ROM(256x12),Fewer I/O Lines(4in,4out,4I/O),and Reg	GIC
66	PIC1650	PIC1650	uCT	Chip	MNI	Progm Intelligent Computer:Single Chip uComp W/RAM,ROM,ALU,I/O	GIC
67	PIC1654	PIC1650	uCT	Chip	MNI	8 Bit Single Chip Microcomputer;512 x 12 Program ROM,24 8 Bit Registers	GIC
68	PIC1655	PIC1650	uCT	Chip	MNI	Progm Intelligent Computer:Single Chip uComp W/RAM,ROM,ALU,I/O 20 Lines	GIC
69	PIC1670	PIC1650	uCT	Chip	MNI	Progm Intelligent Computer:Single Chip uComp W/RAM,ALU,I/O,1kx12 ROM	GIC
70	PIC1664	PIC1650	DEV	Chip	MNI	Programmable Intelligent Computer Devel Ckt;PIC 1650 W/O ROM	GIC
71	DB1650	PIC1650	DEV	MOD		PIC Development System;Includes PIC1650 Programmed with PICBUG	GIC
72	FD1664	PIC1650	DEV	MOD		PIC Field Demo System;Includes PIC1664 and Two 74367 Driver Ckts	GIC
73	PICMOSEMULATOR	PIC1650	DEV	MOD	MNX	MOS PIC Emulator;For Debugging PIC Applications Program	GIC
74	PICTTLEMULATOR	PIC1650	DEV	MOD	BTX	TTL PIC Emulator:Provides Hardware Emulation Of PIC 1650	GIC
75	PIC1640	PIC1650	IO-30	Chip	MNI	Programmable Interface Controller:256x12 ROM For U Program	GIC
76	SBA	SBA	DEV	Chip		1 Bit Microcomputer;24 Basic Instructions,1023 Words of ROM Program	GIC
77	SBA-1	SBA	DEV	Chip		SBA Without ROM; For Use With External RAM or PROM	GIC
78	SBA-FD	SBA	DEV	MOD		Field Demo For SBA;Contains SBA-1,Prog.Counter,Demux,5Sockets For 1702A	GIC
79	TZ2001	TZ2001	IO-20	Chip		Telephone Dialler;32Telephone No. Storage,Display 12 Digits	GIC
80	SC1600	1600	COMP	MOD		GIMINI Single Card Microcomputer Module	GIC
81	CP1600	1600	CPU	Chip	MNI	16 Bit Microporcessor;600ns Cycle Time 3.3MHz 2 Phase Clock	GIC
82	CP1600A	1600	CPU	Chip	MNI	16 Bit Microprocessor;400ns Cycle Time 5.0MHz 2 Phase Clock	GIC
83	CP1610	1600	CPU	Chip	MNI	16 Bit Microprocessor;1.0uS Cycle Time	GIC
84	IOB1680	1600	IO-33	Chip	MNI	Input/Output Buffer;Single 1 Bit Port Or Dual 8 Bit Ports	GIC
85	DAC1600	1600	IO-40	Chip		Dual Dig To Analog Converter:Provides Two 10 Bit Pulse Mod Output	GIC
86	MUX1600	1600	IO-43	Chip	MNI	18 Channel Analog Multiplexer	GIC
87	RM1600	1600	RAM	MOD	MNI	2k x 16 RAM Module;32 256 x 4 On 9.75 x 9.25 x .062 In PCB	GIC
88	RO-3-9500	1600	ROM	Chip		2048 x 10 Organization; 5 Bit Chip Select Decode.	GIC
89	RO-3-9501	1600	ROM	Chip		RO-3-9500 with 10 Bit Output Address Latch to Control 1k of External RAM	GIC
90	RO-3-9502	1600	ROM	Chip		RO-3-9500 With 16Bit Output Address Latch	GIC
91	8900	8900	COMP	UNIT		Includes CP1610CPU,AY-3-8900,-1Interface,RO-3-9502,3ROMs,RA-3-9600SysRAM	GIC
92	DB8900	8900	DEV	MOD		Development Sys. Includes all 8900 Sys. Components Plus Osc. And Mod. Cd	GIC
93	8950	8950	COMP	UNIT		Includes CP1610CPU,AY-3-8950,-1Interface,RO-3-9501ProgramROM,2112ASysRAM	GIC
94	DB8950	8950	DEV	MOD		Development Sys. Includes all 8950 Sys. Components Plus Osc. And Mod. Cd	GIC
95#	LP8000	8000	CPU	Chip	MPN	8 Bit Microprocessor,Binary And Decimal Arithmetic Capability	GICB
96#	LP6000	8000	IO-01	Chip	MPN	1k x 8 Bit Program Memory	GICB
97#	LP1000	8000	IO-03	Chip	MPN	Memory Interface Chip,11 Bit Program Counter On 4-Word Hardware Stack	GICB
98#	LP1030	8000	IO-32	Chip	MPN	Clock Generator,800kHz	GICB
99#	LP1010	8000	IO-33	Chip	MPN	Input/Output Buffer,2 Addressable 8 Bit I/O Interfaces	GICB
100	HCMP1851CD,P	HCMP1800	IO-30	Chip	MCG	Programmable Dual Port I/O;Op Range 4-6V;Cer or Plastic Pkg	HAC
101	HCMP1851D,P	HCMP1800	IO-30	Chip	MCG	Programmable Dual Port I/O; Op Range 4-12V; Cer or Plastic Pkg	HAC
102	HCMP1855CD,P	HCMP1800	IO-90	Chip	MCG	Multiply-Divide Unit;8 Bits;Op Range 4-6V; Cer or Plastic Pkg	HAC
103	HCMP1855D,P	HCMP1800	IO-90	Chip	MCG	Multiply-Divide Unit;8 Bits;Op Range 4-12V; Cer or Plastic Pkg	HAC
104	HCMP1802CD	HCMP1802	CPU	Chip	MCG	8 Bit CMOS CPU;Operating Volt Range 4-6V	HAC
105	HCMP1802D	HCMP1802	CPU	Chip	MCG	8 Bit CMOS CPU;Operating Volt Range 3-12V	HAC
106	HCMP1861CD	HCMP1802	IO-09	Chip	MCG	Video Display Controller;Programmable Vertical Resolution	HAC
107	HCMP1854CD	HCMP1802	IO-20	Chip	MCG	CMOS UART;Op Volt Range 4-6V;DC to 200k Baud	HAC
108	HCMP1854D	HCMP1802	IO-20	Chip	MCG	CMOS UART;Op Volt Range 3-12V;DC to 400k Baud	HAC
109	HCMP1856CD	HCMP1802	IO-21	Chip	MCG	4 Bit Non-Invert Bus Buffer/Seperator;Op Volt Range 4-6V	HAC
110	HCMP1856D	HCMP1802	IO-21	Chip	MCG	4 Bit Non-Invert Bus Buffer/Seperator;Op Volt Range 3-12V	HAC

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE
1	HCMP1857CD	HCMP1802	IO-21	Chip	MCG	4 Bit Non-Invert Bus Buffer/Seperator;Op Volt Range 4-6V	HAC
2	HCMP1857D	HCMP1802	IO-21	Chip	MCG	4 Bit Non-Invert Bus Buffer/Seperator;Op Volt Range 3-12V	HAC
3	HCMP1852CD	HCMP1802	IO-33	Chip	MCG	8 Bit Mode Programmable Input/Output Port;Op Volt 4-6V	HAC
4	HCMP1852D	HCMP1802	IO-33	Chip	MCG	8 Bit Mode Programmable Input/Output Port;Op Volt 3-12V	HAC
5	HCMP1853CD	HCMP1802	IO-44	Chip	MCG	N Bit 1 of 8 Decoder;Op Volt Range 4-6V;Direct Control of 14 Ports	HAC
6	HCMP1853D	HCMP1802	IO-44	Chip	MCG	N Bit 1 of 8 Decoder;Op Volt Range 3-12V;Direct Control of 14 Ports	HAC
7	HCMP1858CD	HCMP1802	IO-56	Chip	MCG	4 Bit Latch With Decode;Op Volt Range 4-6V;Controls 32 RAMs 256x4	HAC
8	HCMP1858D	HCMP1802	IO-56	Chip	MCX	4 Bit Latch With Decode;Op Volt Range 3-12V;Controls 32 RAMs 256x4	HAC
9	HCMP1859CD	HCMP1802	IO-56	Chip	MCG	4 Bit Latch With Decode;Op Volt Range 4-6V;Controls 32 RAMs 1kx1	HAC
10	HCMP1859D	HCMP1802	IO-56	Chip	MCG	4 Bit Latch With Decode;Op Volt Range 3-12V;Controls 32 RAMs 1kx1	HAC
11	HCMP1822CD	HCMP1802	RAM	Chip	MCG	256x4 Static RAM;Operating Volt Range 4-6V	HAC
12	HCMP1822D	HCMP1802	RAM	Chip	MCG	256x4 Static RAM;Operating Volt Range 4-10V	HAC
13	HCMP1824CD	HCMP1802	RAM	Chip	MCG	32x8 Static RAM;Operating Volt Range 4-6V	HAC
14	HCMP1824D	HCMP1802	RAM	Chip	MCG	32x8 Static RAM;Operating Volt Range 3-12V	HAC
15	HCMP1831CD	HCMP1802	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-6V	HAC
16	HCMP1831D	HCMP1802	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 3-12V	HAC
17	HCMP1832CD	HCMP1802	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-6V	HAC
18	HCMP1832D	HCMP1802	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 3-12V	HAC
19	HCMP1833CD	HCMP1802	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-6V;Access Time 850ns	HAC
20	HCMP1833D	HCMP1802	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 3-12V;Access Time 350ns	HAC
21	HCMP1834CD	HCMP1802	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-6V;Access Time 850ns	HAC
22	HCMP1834D	HCMP1802	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 3-12V;Access Time 350ns	HAC
23	HCMP1836D	HCMP1802	ROM	Chip	MCG	2048 X 8 Static ROM;Oper Volt Range 4-12V;Access Time 850ns	HAC
24	HMDS-2D	1800	DEV	UNIT		Floppy-Disk Based Product Dev Sys./Double Density Dual 8in Floppy Disk	HAC
25	HMDS-2Q	1800	DEV	UNIT		Floppy-Disk Based Product Dev Sys./Quad Den Dual 5in mini Floppy Disk	HAC
26	HCMP1835D	1800	ROM	CHIP	MCX	Static CMOS Mask Programmable ROM	HAC
27	H18	H18	COMP	MODS		Military 16 Bit Microcomputer;-55 to 125°C,Compiles W/MIL-E-5400	HACC
28	H18CPU	H18	CPU	MOD		Microprocessor Board Based on 2900 Chips,Mil E-5400 Compat	HACC
29	H18IO	H18	IO-33	MOD		IO Controller Board	HACC
30	H18MEM24	H18	IO-57	MOD		24k Memory Board	HACC
31	HB61000	HM6100	COMP	MOD	MCX	Single Board Microcomputer Syst;Incl CPU,Mem,UART,I/O,Mon,Key Bd,Display	HAS
32	HM6100-2	HM6100	CPU	Chip	MCG	Microprocessor;Freg 4.0MHz;Temp.-55 To 125°C	HAS
33	HM6100-9	HM6100	CPU	Chip	MCG	Microprocessor;Freg 4.0MHz;Temp.-40 To 85°C	HAS
34	HM6100A-2	HM6100	CPU	Chip	MCG	Microprocessor;Freg 8.0MHz;Temp.-55 To 125°C	HAS
35	HM6100A-9	HM6100	CPU	Chip	MCG	Microprocessor;Freg 8.0MHz;Temp.-40 To 85°C	HAS
36	HM6100C-5	HM6100	CPU	Chip	MCG	Microprocessor;Freg 3.3MHz;Temp.0 To 70°C	HAS
37	HD6101-2	HM6100	IO-02	Chip	MCG	CMOS Parallel Interface Element;4.0 to 7.0V;-50 To 125°C	HAS
38	HD6101-9	HM6100	IO-02	Chip	MCG	CMOS Parallel Interface Element;4.0 to 7.0V;-40 To 85°C	HAS
39	HD6101A-2	HM6100	IO-02	Chip	MCG	CMOS Parallel Interface Element;4.0 to 11V;-50 To 125°C	HAS
40	HD6101A-9	HM6100	IO-02	Chip	MCG	CMOS Parallel Interface Element;4.0 to 11V;-40 To 85°C	HAS
41	HD1-6402-2	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 125ns Max;55-125°C	HAS
42	HD1-6402-9	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 125ns Max;40-85°C	HAS
43	HD1-6402A-2	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 50ns Max;55-125°C	HAS
44	HD1-6402A-9	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 50ns Max;40-85°C	HAS
45	HD1-6402C-9	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 150ns Max;40-85°C	HAS
46	HD3-6402-2	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 125ns Max;55-125°C	HAS
47	HD3-6402-9	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 125ns Max;40-85°C	HAS
48	HD3-6402A-2	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 50ns Max;55-125°C	HAS
49	HD3-6402A-9	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 50ns Max;40-85°C	HAS
50	HD3-6402C-9	HM6100	IO-20	Chip	MCX	Universal Asynchronous Receiver/Transmitter;tpd 150ns Max;40-85°C	HAS
51	HM1-6611-2	HM6100	PROM	Chip	MXG	256x4 Static FPLA w/3 State Output;Access Time 500ns Max;55-125°C	HAS
52	HM1-6611-9	HM6100	PROM	Chip	MXG	256x4 Static FPLA w/3 State Output;Access Time 500ns Max;40-85°C	HAS
53	HM1-6611A-2	HM6100	PROM	Chip	MXG	256x4 Static FPLA w/3 State Output;Access Time 325ns Max;55-125°C	HAS
54	HM1-6611A-9	HM6100	PROM	Chip	MXG	256x4 Static FPLA w/3 State Output;Access Time 325ns Max;40-85°C	HAS
55	HM1-6611D-5	HM6100	PROM	Chip	MXG	256x4 Static FPLA w/3 State Output;Access Time 800ns Max;0-75°C	HAS
56	HM9-6611-2	HM6100	PROM	Chip	MXG	256x4 Static FPLA w/3 State Output;Access Time 500ns Max;55-125°C	HAS
57	HM9-6611A-2	HM6100	PROM	Chip	MXG	256x4 Static FPLA w/3 State Output;Access Time 325ns Max;55-125°C	HAS
58	HM1-6508-2	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 280ns Min;55-125°C	HAS
59	HM1-6508-9	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 280ns Min;40-85°C	HAS
60	HM1-6508B-2	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cycle Time 220ns Min;55-125°C	HAS
61	HM1-6508B-9	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 220ns Min;40-85°C	HAS
62	HM1-6508D-5	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Cycle Time 380ns Min;0-75°C	HAS
63	HM1-6512-2	HM6100	RAM	Chip	MCG	64x12 Static RAM w/3 State Out;Data Retent;Cycle Time 450ns Min;55-125°C	HAS
64	HM1-6512-9	HM6100	RAM	Chip	MCG	64x12 Static RAM w/3 State Out;Data Retent;Cycle Time 450ns Min;40-85°C	HAS
65	HM1-6512C-9	HM6100	RAM	Chip	MCG	64x12 Static RAM w/3 State Out;Cycle Time 650ns Min;40-85°C	HAS
66	HM1-6518-2	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 280ns Min;55-125°C	HAS
67	HM1-6518-9	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 280ns Min;40-85°C	HAS
68	HM1-6518B-2	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 220ns Min;55-125°C	HAS
69	HM1-6518B-9	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 220ns Min;40-85°C	HAS
70	HM1-6518D-5	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Output;Cycle Time 380ns Min;0-75°C	HAS
71	HM1-6561-2	HM6100	RAM	Chip	MCG	256x4 Static RAM w/3 State Out;Data Retent;Cyc Time 310ns Min;55-125°C	HAS
72	HM1-6561-9	HM6100	RAM	Chip	MCG	256x4 Static RAM W/3 State Out,Data Retent;Cyc Time 310ns Min;40-85°C	HAS
73	HM1-6561B-2	HM6100	RAM	Chip	MCG	256x4 Static RAM w/3 State Out;Data Retent;Cyc Time 230ns Min;55-125°C	HAS
74	HM1-6561B-9	HM6100	RAM	Chip	MCG	256x4 Static RAM w/3 State Out;Data Retent;Cyc Time 230ns Min;40-85°C	HAS
75	HM1-6561D-5	HM6100	RAM	Chip	MCG	256x4 Static RAM w/3 State Out;Cycle Time 430ns Min;0-75°C	HAS
76	HM3-6508-9	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 280ns Min;40-85°C	HAS
77	HM3-6508B-9	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 220ns Min;40-85°C	HAS
78	HM3-6508D-5	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Cycle Time 380ns Min;0-75°C	HAS
79	HM3-6512-9	HM6100	RAM	Chip	MCG	64x12 Static RAM w/3 State Out;Data Retent;Cycle Time 450ns Min;40-85°C	HAS
80	HM3-6512C-9	HM6100	RAM	Chip	MCG	64x12 Static RAM w/3 State Out;Cycle Time 650ns Min;40-85°C	HAS
81	HM3-6518-9	HM6100	RAM	Chip	MCG	1023x1 Static RAM w/3 State Out,Data Retent;Cyc Time 280ns Min;40-85°C	HAS
82	HM3-6518B-9	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Out,Data Retent;Cyc Time 220ns Min;40-85°C	HAS
83	HM3-6518D-5	HM6100	RAM	Chip	MCG	1024x1 Static RAM w/3 State Output;Cycle Time 380ns Min;0-75°C	HAS
84	HM3-6561-9	HM6100	RAM	Chip	MCG	256x4 Static RAM W/3 State Out,Data Retent;Cyc Time 310ns Min;40-85°C	HAS
85	HM3-6561B-9	HM6100	RAM	Chip	MCG	256x4 Static RAM w/3 State Out;Data Retent;Cyc Time 230ns Min;40-85°C	HAS
86	HM3-6561D-5	HM6100	RAM	Chip	MCG	256x4 Static RAM w/3 State Out;Cycle Time 430ns Min;0-75°C	HAS
87	HM6511-2	HM6100	RAM	Chip	MCG	64x12 Static RAM w/3 State Out,Data Retent;Cycle Time 240ns Min;55-125°C	HAS
88	HM6511-9	HM6100	RAM	Chip	MCG	64x12 Static RAM w/3 State Out,Data Retent;Cycle Time 240ns Min;40-85°C	HAS
89	HM6511C-9	HM6100	RAM	Chip	MCG	64x12 Static RAM w/3 State Out;Cycle Time 240ns Min;40-85°C	HAS
90	HM6533-2	HM6100	RAM	Chip	MCG	1024x4 Static RAM w/3 State Out;Data Retent;Cyc Time 475ns Typ;55-125°C	HAS
91	HM6533-9	HM6100	RAM	Chip	MCG	1024x4 Static RAM w/3 State Out;Data Retent;Cycle Time 475ns Typ;40-85°C	HAS
92	HM6533C-9	HM6100	RAM	Chip	MCG	1024x4 Static RAM w/3 State Out;Cycle Time 650ns Min;40-85°C	HAS
93	HM6543-2	HM6100	RAM	Chip	MCG	4096x1 Static RAM w/3 State Out;Data Retent;Cyc Time 475ns Typ;55-125°C	HAS
94	HM6543-9	HM6100	RAM	Chip	MCG	4096x1 Static RAM w/3 State Out;Data Retent;Cyc Time 475ns Typ;40-85°C	HAS
95	HM6543C-9	HM6100	RAM	Chip	MCG	4096x1 Static RAM w/3 State Out;Cycle Time 560ns Min;40-85°C	HAS
96	HM6312-2	HM6100	ROM	Chip	MCG	1024x12 Static ROM w/Programmable RAM;Access Time 560ns Max;55-125°C	HAS
97	HM6312-9	HM6100	ROM	Chip	MCG	1024x12 Static ROM w/Programmable RAM;Access Time 510ns Max;40-85°C	HAS
98	HM6312A-2	HM6100	ROM	Chip	MCG	1024x12 Static ROM w/Programmable RAM;Access Time 220ns Max;55-125°C	HAS
99	HM6312A-9	HM6100	ROM	Chip	MCG	1024x12 Static ROM w/Programmable RAM;Access Time 200ns Max;40-85°C	HAS
100	HM6312C-9	HM6100	ROM	Chip	MCG	1024x12 Static ROM w/Programmable RAM;Access Time 640ns Max;40-85°C	HAS
101	H11	H11	COMP	UNIT		16 Bit Personal Computer Based on LSI11 CPU	HEA
102	H11-2	H11	IO-06	MOD		Parallel Interface for H10 Paper Tape Reader/Punch	HEA
103	H11-5	H11	IO-20	MOD		Serial Interface Between LSI11 Bus and Serial Devices,H9 or LA36 DEC	HEA
104	H11-1	H11	IO-55	MOD		4k Memory Expansion Module;Access Time 500ns max	HEA
105	H11-6	H11	IO-90	Chip		Extended Arith;Fixed Pt Mult,Div,Ext Shifts;Float Pt Add,Sub,Multi,Div	HEA
106	H8	H8	COMP	UNIT		8 Bit Personal Computer Based on 8080A CPU	HEA
107	H8-5	H8	IO-05	MOD		Serial I/O and Cassette Interface;Connects to H9 Terminal,H36 DEC	HEA
108	H8-2	H8	IO-06	MOD		Parallel Interface;Connects H8 to Parallel Devices;Paper Tape Reader,Etc	HEA
109	H36-2	H8	IO-08	MOD		EIA RS232-C or CCITT-V24 Interface for LA36	HEA
110	H36	H8	PE-10	UNIT		10,15,30 Char/Sec Switch Select;128 ASCII Char Set;For H8,H11;Req H36-2	HEA

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	H9	H8	PE-15	UNIT		12 Inch Video Term;12/48 Lines,80/20 Char/Line,ASCII;110-9600 Baud	HEA
2	H10	H8	PE-42	UNIT		50 Char/Sec Read,10 Char/Sec Punch;For H8 or H11	HEA
3	H8-3	H8	RAM	ChS		Kit of Eight 4k Static Memory;Extends H8-1 to 8k	HEA
4	H8-1	H8	RAM	MOD		8k Static RAM Card with 4k Memory;Access Time 450ns max	HEA
5	ADAM12	LSI11	IO-45	MOD		Adaptive Data Acquisition 16/32 Channels MLZ-DAQ Tri-State Logic	HEU
6	ADAM100	LSI11	IO-45	MOD		Adaptive Data Acquisition Control System	HEU
7	MLP8080	MLP8080	COMP	MOD	MNX	8 Bit Computer On A Card 8.5X10.5 in,Uses Intel 8080CPU	HEU
8	MLP8090	MLP8080	DEV	MOD	MNX	Debug Panel For System A	HEU
9	MLP8035	MLP8080	IO-01	MOD		Time Base Option For Inclusion On MLP8030 Board	HEU
10	MLP8065	MLP8080	IO-07	MOD	MNX	IBM Compatable Floppy Disk Controller	HEU
11	MLP8020	MLP8080	IO-09	MOD	MNX	32 Character By 16 Line Display,TV Scan	HEU
12	MLP8022	MLP8080	IO-09	MOD	MNX	80 Character By 16 Line Display,TV Scan	HEU
13	MLP8040	MLP8080	IO-20	MOD	MNX	Quad Synchronous/Asynchronous Communications I/F	HEU
14	MLP8084	MLP8080	IO-20	MOD	MNX	Asynchronous Communication I/F Option	HEU
15	MLP8032	MLP8080	IO-33	MOD	MNX	4 8-Bit Inputs-4 8-Bit Outputs,Parallel	HEU
16	MLP8030	MLP8080	IO-43	MOD	MNX	32 By 1-Bit Inputs-32 By 1-Bit Outputs	HEU
17	MLP8010	MLP8080	IO-55	MOD	MNX	4k RAM-4k ROM Capacity Memory	HEU
18	MLP8082	MLP8080	IO-55	MOD	MNX	2k RAM,2k ROM Capacity Memory Option	HEU
19	MLP8016F	MLP8080	IO-57	MOD		16k ROM With Floppy Disk Interface	HEU
20	MLP8061	MLP8080	PE-01	UNIT		Single Floppy Disk	HEU
21	MLP8062	MLP8080	PE-01	UNIT	MNX	Dual Floppy Disk Drive	HEU
22	MLP8070	MLP8080	PE-10	UNIT	MNX	Printer;Diablo,Qume	HEU
23	MLP8072	MLP8080	PE-10	UNIT	MNX	Printer;Tally,Others	HEU
24	MLP8026	MLP8080	PE-15	UNIT	MNX	12 In CRT Monitor	HEU
25	MLP8026-9	MLP8080	PE-15	UNIT		9 Inch CRT Display, B/W	HEU
26	MLP8026-12	MLP8080	PE-15	UNIT		12 Inch CRT Display, B/W	HEU
27	HIT5000	MLP8080	PE-20	UNIT		Intelligent Terminal Using 80 By 25 Char Display on 9/12 In Screen	HEU
28	MLP8025	MLP8080	PE-61	UNIT	MNX	Keyboard	HEU
29	MLP8016	MLP8080	ROM	MOD	MNX	16k ROM	HEU
30	MLZ80	MLZ80	COMP	MOD		8-Bit Computer On a Card Based On Z80	HEU
31	MLZ80A	MLZ80	COMP	MOD		4MHz Version of MLZ80.	HEU
32	MLZ800	MLZ80	COMP	UNIT		MLZ80 Sys W/Chassis,Triple Volt Switching Supply,Fan,Cage,Monitor	HEU
33	MLZ800A	MLZ80	COMP	UNIT		MLZ80A Sys W/Chassis,Triple Volt Switching Supply,Fan,Cage,Monitor	HEU
34	MLZ-8022B	MLZ80	IO-09	MOD		80 Char By 25 Line CRT Interface Card	HEU
35	MLZ-8/32	MLZ80	IO-55	MOD		8k EPROM Plus 32k Bytes Static RAM Memory Card	HEU
36	MLZ20	MLZ80	PE-15	UNIT		32 Character x 16 Line CRT/KB I/F With BILLBOARD Graphics.	HEU
37	MLZ22	MLZ80	PE-15	UNIT		80 Character x 25 Line CRT/KB I/F. Upper and Lower Case.	HEU
38#	HD468A21P	HD46800D	IO-30	Chip		Universal Peripheral Interface;Dual 8 Bit Bidirectional Data Bus;40Pin	HITJ
39#	HD468B21P	HD46800D	IO-30	Chip		Universal Peripheral Interface;Dual 8 Bit Bidirectional Data Bus;40Pin	HITJ
40#	HMCS42	HMCS40	uCT	Chip	MPX	4 Bit One Chip Microcomputer;10 x 512 ROM; 4 x 32 RAM;IO 4 Bit/1 Ch	HITJ
41#	HMCS42C	HMCS40	uCT	Chip	MCX	4 Bit One Chip Microcomputer;10x(512 plus 32)ROM,4x32 RAM	HITJ
42#	HMCS43	HMCS40	uCT	Chip	MPX	4 Bit One Chip Microcomputer;10 x 1024 ROM;4 x 80 RAM;IO 4 Bit/1 Ch	HITJ
43#	HMCS43C	HMCS40	uCT	Chip	MCX	4 Bit One Chip Microcomputer;10 x 1024 ROM;4 x 80 RAM;IO 4 Bit/1 Ch	HITJ
44#	HMCS44A	HMCS40	uCT	Chip	MPX	4 Bit One Chip Microcomputer;10x(2k plus 128)ROM,4x160 RAM	HITJ
45#	HMCS44C	HMCS40	uCT	Chip	MCX	4 Bit One Chip Microcomputer;10x(2k plus 128)ROM,4x160 RAM	HITJ
46#	HMCS45A	HMCS40	uCT	Chip	MPX	4 Bit One Chip Microcomputer;10x(2k plus 128)ROM,4x160 RAM	HITJ
47#	HMCS45C	HMCS40	uCT	Chip	MCX	4 Bit One Chip Microcomputer;10x(2k plus 128)ROM,4x160 RAM	HITJ
48▼#	HD44770	HMCS40	UCT	CHIP	MNX	4-Bit uComputer;can Drive 16x42 Dot Matrix LCD for Graphic/Alphanumeric	HITJ
49▼#	HD44780	HMCS40	UCT	CHIP	MNX	LCD Contr/Driver;Drives 16-Digit Alphanumeric LC Display;Drives 80 Digit	HITJ
50▼#	HD44790	HMCS40	UCT	CHIP	MNX	4-Bit Can Drive 16 Digit Seven-Segment LCD	HITJ
51#	HD468A00P	HMCS6800	CPU	Chip	MNG	8 Bit Parallel Proc;2 Way Data Bus;16 Bit Addr Bus;40 Pin Plastic Pkg	HITJ
52#	HD468B00P	HMCS6800	CPU	Chip	MNG	8 Bit Parallel Proc;2 Way Data Bus; 16 Bit Addr Bus;40 Pin Plastic Pkg	HITJ
53#	HD46800DP	HMCS6800	CPU	Chip	MNG	8 Bit Microprocessor;6 Internal Registers,1.0MHz Clock,Plastic Pkg	HITJ
54#	HD46802P	HMCS6800	CPU	Chip		HD46802 in Plastic Package	HITJ
55#	HD46504P	HMCS6800	IO-03	Chip	MNX	Direct Memory Access Controller;Max Data Transfer Rate 1.0M Byte/s	HITJ
56#	HD46505RP	HMCS6800	IO-09	Chip	MNX	Same as HD46505R But in Plastic Package	HITJ
57#	HD46850P	HMCS6800	IO-20	Chip	MNG	Asynchronous Communication Interface Adapter,Plastic Pkg	HITJ
58#	HD2681T26P	HMCS6800	IO-21	Chip		Quad Bus Transceiver;Plastic Pkg	HITJ
59#	HD46821P	HMCS6800	IO-30	Chip	MNG	Peripheral Interface Adapter,Plastic Pkg	HITJ
60#	HD26501	HMCS6800	IO-32	Chip	BTD	Clock Pulse Generator/Controller;2 Phase Clock On Chip	HITJ
61▼#	HD46508P1A1	HMCS6800	IO-45	CHIP	MNX	Acquisition Data Analog Unit; Prog A/D Conv;Non-Linear ±LSB;Spd 1.5MHz	HITJ
62▼#	HD46508P1A2	HMCS6800	IO-45	CHIP	MNX	Acquisition Data Analog Unit; Prog A/D Conv;Non-Linear ±1 LSB;Spd 1.5MHz	HITJ
63▼#	HD46508P2A1	HMCS6800	IO-45	CHIP	MNX	Acquisition Data Analog Unit; Prog A/D Conv;Non-Linear ±1 LSB;Spd 2.0MHz	HITJ
64▼#	HD46508P-A1	HMCS6800	IO-45	CHIP	MNX	Acquisition Data Analog Unit;Prog A/D Conv;Non-Linearity ±1 LSB;Spd 1MHz	HITJ
65#	HD46846P	HMCS6800	PROM	Chip		Same as HD46846 But in Plastic Package	HITJ
66#	HN462708	HMCS6800	PROM	Chip	MNG	1024x8 Erasable,Electrically Programmable ROM;Tri-State	HITJ
67#	HN462716	HMCS6800	PROM	Chip		2048x8 Bit PROM;Electrically Programmable,UV Light Erasible	HITJ
68#	HM468A10P	HMCS6800	RAM	Chip	MNG	Same as HM468A10 But in Plastic Package	HITJ
69#	HM4315P	HMCS6800	RAM	Chip	MCX	4096x1 Bit RAM;620nS R/W Cycle Time	HITJ
70#	HM4704L-2	HMCS6800	RAM	Chip	MNX	4096 x 1 Dynamic RAM;Access Time 150ns max	HITJ
71#	HM4704L-3	HMCS6800	RAM	Chip	MNX	4096 x 1 Dynamic RAM;Access Time 200ns max	HITJ
72#	HM4704L-4	HMCS6800	RAM	Chip	MNX	4096 x 1 Dynamic RAM;Access Time 250ns max	HITJ
73#	HM4710	HMCS6800	RAM	Chip	MNX	4096 x 1 Dynamic RAM;Access Time 100ns max	HITJ
74#	HM4711-1	HMCS6800	RAM	Chip	MNG	4096x1 Dynamic RAM;Access Time 130ns max	HITJ
75#	HM4711-2	HMCS6800	RAM	Chip	MNG	4096x1 Dynamic RAM;Access Time 150ns max	HITJ
76#	HM4711-3	HMCS6800	RAM	Chip	MNG	4096x1 Dynamic RAM;Access Time 200ns max	HITJ
77#	HM4716A-2	HMCS6800	RAM	Chip	MNX	16384 x 1 Dynamic RAM;Access Time 150ns max	HITJ
78#	HM4716A-3	HMCS6800	RAM	Chip	MNX	16384 x 1 Dynamic RAM;Access Time 200ns max	HITJ
79#	HM4716A-4	HMCS6800	RAM	Chip	MNX	16384 x 1 Dynamic RAM;Access Time 250ns max	HITJ
80#	HM4816	HMCS6800	RAM	Chip	MNX	16384x1 Bit RAM;200nS R/W Cycle Time	HITJ
81#	HM4847-2	HMCS6800	RAM	Chip	MNX	4096x1 Bit Static RAM;45nS R/W Cycle Time	HITJ
82#	HM4847-3	HMCS6800	RAM	Chip	MNX	4096x1 Bit Static RAM;55nS R/W Cycle Time	HITJ
83#	HM6147	HMCS6800	RAM	Chip	MCX	4096x1 Bit RAM;70nS R/W Cycle Time	HITJ
84#	HM46810	HMCS6800	RAM	Chip	MNX	128 x 8 Static RAM;Access Time 450ns max	HITJ
85#	HM46810P	HMCS6800	RAM	Chip	MNG	Same as HM46810 But in Plastic Package	HITJ
86#	HM435101	HMCS6800	RAM	Chip	MNG	256x4 Static RAM;Access Time 650ns max	HITJ
87#	HM435101-1	HMCS6800	RAM	Chip	MNG	256x4 Static RAM;Access Time 450ns max	HITJ
88#	HM435101P	HMCS6800	RAM	Chip		Same as HM435101 But in Plastic Package	HITJ
89#	HM435101P-1	HMCS6800	RAM	Chip		Same as HM435101-1 But in Plastic Package	HITJ
90#	HM435101V	HMCS6800	RAM	Chip	MCX	256 x 4 Static RAM;Access Time 650ns max	HITJ
91#	HM435101VP	HMCS6800	RAM	Chip		Same as HM435101V But in Plastic Package	HITJ
92#	HM472114-3	HMCS6800	RAM	Chip	MNX	1024 x 4 Static RAM;Access Time 300ns max	HITJ
93#	HM472114-4	HMCS6800	RAM	Chip	MNX	1024 x 4 Static RAM;Access Time 450ns max	HITJ
94#	HM472114AP-2	HMCS6800	RAM	Chip		1024x4 Bit Static RAM;200nS R/W Cycle Time	HITJ
95#	HM472114P-3	HMCS6800	RAM	Chip	MNG	Same as HM472114-3 But in Plastic Package	HITJ
96#	HM472114P-4	HMCS6800	RAM	Chip	MNG	Same as HM472114-4 But in Plastic Package	HITJ
97#	HN35600P	HMCS6800	ROM	Chip	MPX	256x8 Bit Mask Programmable ROM;930nS Access Time	HITJ
98#	HN35800P	HMCS6800	ROM	Chip	MPX	1024x8 Bit Mask Programmable ROM;930nS Access Time	HITJ
99#	HN46532-3	HMCS6800	ROM	Chip	MNG	4096 x 8 Static ROM;Access Time 600ns max;Power Diss 440mW max	HITJ
100#	HN46830	HMCS6800	ROM	Chip	MNX	1024 x 8 Static ROM;Access Time 500ns max;Power Diss 350mW Typ	HITJ
101▼#	HD68A09DC	6800	CPU	CHIP	MNG	8-Bit uProcessor U it;6800 Compat;2-16 Bit Index Reg;	HITJ
102▼#	HD68A09DP	6800	CPU	CHIP	MNG	8-Bit uProcessor U it;6800 Compat;2-16 Bit Index Reg;	HITJ
103▼#	HD68B09DC	6800	CPU	CHIP	MNG	8-Bit uProcessor U it;6800 Compat;2-16 Bit Index Reg;	HITJ
104▼#	HD68B09DP	6800	CPU	CHIP	MNG	8-Bit uProcessor U it;6800 Compat;2-16 Bit Index Reg;	HITJ
105▼#	HD6809DC	6800	CPU	CHIP	MNG	8-Bit uProcessor U it;6800 Compat;2-16 Bit Index Reg;	HITJ
106▼#	HD6809DP	6800	CPU	CHIP	MNG	8-Bit uProcessor U it;6800 Compat;2-16 Bit Index Reg;	HITJ
107▼#	HD68000DC	6800	CPU	CHIP	MNG	16-Bit uProcessing Unit;32 Bit Data/Add Reg;16M Byte Dir Add Range	HITJ
108▼#	HD6801DC	6800	UCT	CHIP	MNG	8-Bit uComputer;Expanded 6800 Instru Set;8x8 Multiply;16-Bit Timer	HITJ
109▼#	HD6801DP	6800	UCT	CHIP	MNG	8-Bit uComputer;Expanded 6800 Instru Set;8X8 Multiply;16-Bit Timer	HITJ
110▼	HDSP2470	HDSP2000	IO-09	MOD		Display Interface Inc 64 Character ASCII Decoder	HPA

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1▼	HDSP2471	HDSP2000	IO-09	MOD		Display Interface Inc 128 Character ASCII Decoder	HPA
2▼	HDSP2472	HDSP2000	IO-09	MOD		Display Interface Without ASCII Decoder;128 Character;1k x8 Prom	HPA
3	MX800	MX SERIES	CPU	MOD	MNX	MPU Module Uses the Intel 8080A	ICC
4	MDS8000	MX SERIES	DEV	MOD	MNX	Commander Microcomputer Development System And Software	ICC
5	MX810	MX SERIES	IO-02	MOD	MNX	System Clock And Control Module	ICC
6	MX840	MX SERIES	IO-02	MOD	MNX	Priority Interrupt Control Module	ICC
7	MX841	MX SERIES	IO-02	MOD	MNX	Extended Priority Interrupt Control Module	ICC
8	MX846	MX SERIES	IO-02	MOD	MNX	System I/O Logic Module	ICC
9	MX700	MX SERIES	IO-03	MOD	MNX	PROM Programmer Module	ICC
10	MX818	MX SERIES	IO-03	MOD		4k Static RAM Memory Driver	ICC
11	MX833	MX SERIES	IO-03	MOD		4k Static RAM Logic;Provides Address Bus Interfacing for MX832	ICC
12	MX850	MX SERIES	IO-05	MOD		Audio Cassette Interface,Motor Control Module	ICC
13	MX851	MX SERIES	IO-05	MOD		Audio Cassette Interface,Receive Control Module	ICC
14	MX852	MX SERIES	IO-05	MOD		Audio Cassette Interface,Transmit Control Module	ICC
15	MX806	MX SERIES	IO-09	MOD	MNX	LED Display Module;Address,Data Bus,Status Bits	ICC
16	MX847	MX SERIES	IO-20	MOD	MNX	Programmable Serial I/O Module	ICC
17	MX848	MX SERIES	IO-20	MOD	MNX	Programmable Baud Rate Generator Module	ICC
18	MX849	MX SERIES	IO-20	MOD		Programmable 24 Bit Parallel I/O Port	ICC
19	MX843	MX SERIES	IO-30	MOD		Programmable 24 Bit Parallel I/O Port with Cable Connector	ICC
20	MX816	MX SERIES	IO-31	MOD		8 Bit Data Bus Buffer/Amplifier	ICC
21	MX817	MX SERIES	IO-33	MOD		16 Bit Data/Address Bus Buffer Amplifier	ICC
22	MX842	MX SERIES	IO-33	MOD	MNX	Commander MDS I/O Logic Module	ICC
23	MX844	MX SERIES	IO-33	MOD	MNX	Single 8 Bit Parallel I/O Port Module	ICC
24	MX845	MX SERIES	IO-33	MOD	MNX	Dual 8 Bit Parallel I/O Port;Address Buffer Module	ICC
25	MX805	MX SERIES	IO-44	MOD	MNX	3 1 Of 8 Address Decode Module	ICC
26	MX815	MX SERIES	IO-56	MOD	MNX	16 D Status Latches	ICC
27	MX890	MX SERIES	IO-92	MOD	MNX	Step Control Module	ICC
28	2224	MX SERIES	PE-24	UNIT	MNX	Printer With RS232C Interface Integrated To Development System	ICC
29	MX820	MX SERIES	PROM	MOD	MNX	512 x 8 PROM Module	ICC
30	MX821	MX SERIES	PROM	MOD	MNX	1024 x 8 PROM Module	ICC
31	MX822	MX SERIES	PROM	MOD	MNX	2048 x 8 PROM Module	ICC
32	MX823	MX SERIES	PROM	MOD	MNX	1536 x 8 PROM Module	ICC
33	MX830	MX SERIES	RAM	MOD	MNX	256 x 8 Static RAM Module	ICC
34	MX831	MX SERIES	RAM	MOD	MNX	512 x 8 Static RAM Module	ICC
35	MX832	MX SERIES	RAM	MOD		Static 4kx4 RAM,Board Pair 4kx8	ICC
36	IM1010		PE-50	UNIT		Universal PROM Programmer W/Full Editing Capability	IMI
37	I-8080	I-8080	COMP	UNIT		8 Bit Microcomputer Sys;Uses 8080A CPU;32/64k RAM;Kit or Assembled	IMS
38	PCS-80/21,22A	I-8080	PE-01	UNIT		Floppy Disk System;Control Up to Four Cal Comp Disk Drives,FIF Controller	IMS
39	PCS-80/21,22C	I-8080	PE-01	UNIT		Floppy Disk System;Control Up to Four Cal Comp Disk Drives,DIO-B Control	IMS
40	PCS-80/22B	I-8080	PE-01	UNIT		Dual Drive Expansion Unit for PCS-80/22A	IMS
41	PCS-80/22D	I-8080	PE-01	UNIT		Dual Drive Expansion Unit for PCS-80/22C	IMS
42	PCS-40	PCS-40	COMP	UNIT		Personal Comp Sys;8085 CPU,Dual Floppy Disk,180k Bytes Disk;32/64 RAM	IMS
43	PCS-42	PCS-40	COMP	UNIT		Personal Comp Sys;8085 CPU,Dual Floppy Disk,400k Bytes Disk;32/64 RAM	IMS
44	PCS-44	PCS-40	COMP	UNIT		Personal Comp Sys;8085 CPU,Dual Floppy Disk,780k Bytes Disk;32/64 RAM	IMS
45	PCS-80/15	PCS-80	COMP	UNIT		8 Bit Microcomputer Sys;With Operators Front Panel;8085 Based;32/64 RAM	IMS
46	MPU-A	PCS-80	CPU	MOD		8080A Microprocessor Board	IMS
47♦	IMDOS	PCS-80	DEV	UNIT		Multi-Disk Operating System Version 2.05, Incl HW/SW	IMS
48	PIC-8	PCS-80	IO-02	MOD		Priority Interrupt/Interval Clock Board	IMS
49	DIO	PCS-80	IO-07	MOD		Non DMA Disk Interface Ordered W/O PCS-80/25A,B;PCS-80/34,35	IMS
50	FIF	PCS-80	IO-07	MOD		Floppy Disk Drive Interface for Use W/142M Drive Ordered W/O FDC2-1,2	IMS
51	VIO	PCS-80	IO-09	MOD		Video Interface Board;1k Refresh Mem,Upper Case,All Formats Except 80x24	IMS
52	SIO2-2	PCS-80	IO-20	MOD		Two Channel Serial I/O Interface Board	IMS
53	MIO	PCS-80	IO-33	MOD		Multiple I/O Board;2 Par/1 Serial Port,1 Control Port,Cass Interface	IMS
54	PIO4-4	PCS-80	IO-33	MOD		4 Port Parallel I/O Board	IMS
55	MD2	PCS-80	PE-01	UNIT		Floppy Mini Disk Syst:40 Track,Single/Double Density,5 1/4 in Disk	IMS
56	MD2E	PCS-80	PE-01	UNIT		Dual Drive Expansion Unit For MD2;Includes Pwr Supply	IMS
57	MD4	PCS-80	PE-01	UNIT		Floppy Mini Disk Syst:77 Track,Single/Double Density,5 1/4 in Disk	IMS
58	MD4E	PCS-80	PE-01	UNIT		Dual Drive Expansion Unit For MD2;Includes Pwr Supply	IMS
59	PCS-80/25	PCS-80	PE-01	UNIT		Floppy Disk Sys;Random Access PerSci Disk Drives;DIO-C Disk Controller	IMS
60	PCS-80/26	PCS-80	PE-01	UNIT		Dual Expansion Unit for PCS-80/25 and VPB-80	IMS
61	HD-10	PCS-80	PE-02	UNIT		Hard Disk System;10M Byte Formatted On-Line Storage;S100 Bus Compat.	IMS
62	HD-10E	PCS-80	PE-02	UNIT		Hard Disk Syst Extension Drive, 10 Mega Byte, Including Power Supply	IMS
63	PTR-45A	PCS-80	PE-10	UNIT		45 cps Hy Type 11 Character Printer	IMS
64	PTR-45A-TF	PCS-80	PE-10	UNIT		45 cps Hy Type 11 Character Printer with Tractor Feed	IMS
65	PTR-300A	PCS-80	PE-10	UNIT		300 lpm Line Printer;80 Characters Per Line	IMS
66	PTR-300B	PCS-80	PE-10	UNIT		300 lpm Line Printer;132 Characters Per Line	IMS
67	PS-28	PCS-80	PE-60	UNIT		Power Supply Unit;28 Amps	IMS
68	1KB-1	PCS-80	PE-61	UNIT		Intelligent Keyboard;Mod Programmable;Upper/Lower Case ASCII Encoded	IMS
69	CP-A	PCS-80	PE-61	UNIT		Front Panel W/Switches and Indicators for Hardware/Software Development	IMS
70	RAM16	PCS-80	RAM	MOD		16k Byte Dynamic RAM	IMS
71	VDP-40	VDP-40	COMP	UNIT		8 Bit Video Data Processor Inc32/64 RAM;180k Bytes Disk Storage Cap	IMS
72	VDP-42	VDP-40	COMP	UNIT		8 Bit Video Data Processor Inc 32/64 RAM;400k Bytes Disk Storage Cap	IMS
73	VDP-44	VDP-40	COMP	UNIT		8 Bit Video Data Processor Inc 32/64 RAM;780k Bytes Disk Storage Cap	IMS
74	RAMIII-32	VDP-40	RAM	MOD		32k Byte Dynamic RAM;Access Time 375nS max.S-100 Bus Compatible.	IMS
75	RAMIII-64	VDP-40	RAM	MOD		64k Byte Dynamic RAM;Access Time 375nS max.S-100 Bus Compatible.	IMS
76	VDP-80	VDP-80	COMP	UNIT		8 Bit Video Data Processor Incl 32/64 RAM;2k ROM;Uses 8085 CPU	IMS
77	MFIO-1	UC1800,2000	IO-57	MOD		Multifunction I/O Board;8 Bit Par Input Port,RAM,EPROM,S100 Bus Compatibl	INF
78	MFIO-1/001	UC1800,2000	IO-57	MOD		Multifunction I/O Board;With 2k,21 Command Firmware Monitor Program	INF
79	6945			MOD		Buffer Board;Compatible w/ICE 48	INL
80	6915	IM6100	RAM	MOD		32k RAM Board;Interfaces Directly to TTL Interceptionz Bus Structure	INL
81	6901-M4KX12	INTERCEPT	DEV	MOD		Nonvolatile CMOS RAM	INL
82	6909-RRELAY	INTERCEPT	DEV	MOD	MCG	Reader Relay For Remote Reader Control And Noise Protection	INL
83	6910-INTERCEPTII	INTERCEPT	DEV	UNIT	MCG	Intercept II;IM6100 DEV Sys;Space for 9 CKT Bds;4k RAM,Expand to 32k	INL
84	6970-IFDOS	INTERCEPT	DEV	UNIT	MCG	Floppy Disk Operating System With Drive Mechanisms,Electronics And Power	INL
85	6950-INTERCEPTJR	INTERCEPTJR	DEV	MOD		Intercept JR Module,Uses IM6100 Training System	INL
86	6957-AUDVIS	INTERCEPTJR	DEV	MOD	MCG	Audio Visual Module With Audible Output and LED Display	INL
87	6953-PIEART	INTERCEPTJR	IO-20	MOD		Jr Serial I/O Module	INL
88	6952-P2KX12	INTERCEPTJR	PROM	MOD		Jr Programmable ROM-PROM Module	INL
89	6951-M1KX12	INTERCEPTJR	RAM	MOD		Jr RAM Module,Uses 12,1024x1 CMOS RAMs IM6518	INL
90	IM6100-1IDL	6100	CPU	Chip	MCG	12-Bit;Oper Volt 5.0V;Oper Freq 3.33MHz;-40 to 85°C;Ceramic Pkg	INL
91	IM6100-1IPL	6100	CPU	Chip	MCG	12-Bit;Oper Volt 5.0V;Oper Freq 3.33MHz;-40 to 85°C;Plastic Pkg	INL
92	IM6100-1MDL	6100	CPU	Chip	MCG	12-Bit;Oper Volt 5.0V;Oper Freq 2.5MHz;-55 to 125°C;Ceramic Pkg	INL
93	IM6100AIDL	6100	CPU	Chip	MCG	12-Bit;Oper Volt 10V;Oper Freq 5.71MHz;-40 to 85°C;Ceramic Pkg	INL
94	IM6100AIPL	6100	CPU	Chip	MCG	12-Bit;Oper Volt 10V;Oper Freq 5.71MHz;-40 to 85°C;Plastic Pkg	INL
95	IM6100AMDL	6100	CPU	Chip	MCG	12-Bit;Oper Volt 10V;Oper Freq 5.0MHz;-55 to 125°C;Ceramic Pkg	INL
96	IM6100IPL	6100	CPU	Chip	MCG	12-Bit;Oper Volt 5.0V;Oper Freq 2.5MHz;-40 to 85°C;Plastic Pkg	INL
97	IM6101-1IDL	6100	IO-02	Chip	MCG	Progr Interface For Contr,Priority Signals to Periph;4-7V;-40 to 85°C	INL
98	IM6101-1IPL	6100	IO-02	Chip	MCG	Progr Interface For Contr,Priority Signals to Periph;4-7V;-40 to 85°C	INL
99	IM6101-1MDL	6100	IO-02	Chip	MCG	Progr Interface For Contr,Priority Signals to Periph;4-7V;-55 to 125°C	INL
100	IM6101AIDL	6100	IO-02	Chip	MCG	Progr Interface For Contr,Priority Signals to Periph;4-11V;-40 to 85°C	INL
101	IM6101AIPL	6100	IO-02	Chip	MCG	Progr Interface For Contr,Priority Signals to Periph;4-11V;-40 to 85°C	INL
102	IM6101AMDL	6100	IO-02	Chip	MCG	Progr Interface For Contr,Priority Signals to Periph;4-11V;-55 to 125°C	INL
103	IM6101IPL	6100	IO-02	Chip	MCG	Progr Interface For Contr,Priority Signals to Periph;4-7V;-40 to 85°C	INL
104	IM6102-1IDL	6100	IO-03	Chip	MCG	Memory Extension/DMA/Interval Time/Controller;-40-85°C;40 Pin Ceramic	INL
105	IM6102-1IPL	6100	IO-03	Chip	MCG	Memory Extension/DMA/Interval Time/Controller;-40-85°C;40 Pin Plastic	INL
106	IM6102-1MDL	6100	IO-03	Chip	MCG	Memory Extension/DMA/Interval Time/Controller;-55-125°C;40 Pin Ceramic	INL
107	IM6102AIDL	6100	IO-03	Chip	MCG	Memory Extension/DMA/Interval Timer/Controller;-40-85°C,40Pin Ceramic	INL
108	IM6102AIPL	6100	IO-03	Chip	MCG	Memory Extension/DMA/Interval Timer/Controller;-40-85°C,40Pin Plastic	INL

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE
1	IM6102AMDL	6100	IO-03	Chip	MCG	Memory Extension/DMA/Interval Timer/Controller;-55-125°C,40Pin Ceramic	INL
2	IM6102IPL	6100	IO-03	Chip	MCG	Memory Extension/DMA/Interval Timer/Controller;-40-85°C,40Pin Plastic	INL
3	IM6402-1IDL	6100	IO-20	Chip	MCG	UART;Clock 2.0MHz Max;3-State Contr Buffers;4 to 7V;-40 to 85°C;Ceramic	INL
4	IM6402-1IPL	6100	IO-20	Chip	MCG	UART;Clock 2.0MHz Max;3-State Contr Buffers;4 to 7V;-40 to 85°C;Plastic	INL
5	IM6402-1MDL	6100	IO-20	Chip	MCG	UART;Clock 2.0MHz Max;3-State Contr Buffers;4 to 7V;-55 to 125°C;Ceramic	INL
6	IM6402AIDL	6100	IO-20	Chip	MCG	UART;Clock 4.0MHz Max;3-State Contr Buffers;4 to 11V;-40 to 85°C;Ceramic	INL
7	IM6402AIPL	6100	IO-20	Chip	MCG	UART;Clock 4.0MHz Max;3-State Contr Buffers;4 to 11V;-40 to 85°C;Plastic	INL
8	IM6402AMDL	6100	IO-20	Chip	MCG	UART;Clock 4.0MHz Max;3-State Contr Buffers;4 to 11V;-55 to 125°C;Ceramic	INL
9	IM6402IPL	6100	IO-20	Chip	MCG	UART;Clock 1.0MHz Max;3-State Contr Buffers;4 to 7V;-40 to 85°C;Plastic	INL
10	IM6403-1IDL	6100	IO-20	Chip	MCG	UART;Ext Xtal 3.58MHz;4,11 Stage Divider;4 to 7V;-40 to 85°C;Ceramic	INL
11	IM6403-1IPL	6100	IO-20	Chip	MCG	UART;Ext Xtal 3.58MHz;4,11 Stage Divider;4 to 7V;-40 to 85°C;Plastic	INL
12	IM6403-1MDL	6100	IO-20	Chip	MCG	UART;Ext Xtal 3.58MHz;4,11 Stage Divider;4 to 7V;-55 to 125°C;Ceramic	INL
13	IM6403AIDL	6100	IO-20	Chip	MCG	UART;Ext Xtal 6.00MHz;4,11 Stage Divider;4 to 11V;-40 to 85°C;Ceramic	INL
14	IM6403AIPL	6100	IO-20	Chip	MCG	UART;Ext Xtal 6.00MHz;4,11 Stage Divider;4 to 11V;-40 to 85°C;Plastic	INL
15	IM6403AMDL	6100	IO-20	Chip	MCG	UART;Ext Xtal 6.00MHz;4,11 Stage Divider;4 to 11V;-55 to 125°C;Ceramic	INL
16	IM6403IPL	6100	IO-20	Chip	MCG	UART;Ext Xtal 2.46MHz;4,11 Stage Divider;4 to 7V;-40 to 85°C;Plastic	INL
17	IM6103AIDL	6100	IO-30	Chip	MCG	Parallel Input-Output Port;-40 to 85°C,4 to 11V,40 Pin Cer Pkg	INL
18	IM6103AIPL	6100	IO-30	Chip	MCG	Parallel Input-Output Port;-40 to 85°C,4 to 11V,40 Pin Plastic Pkg	INL
19	IM6103AMDL	6100	IO-30	Chip	MCG	Parallel Input-Output Port;-55 to 125°C,4 to 11V,40 Pin Cer Pkg	INL
20	IM6103AMDL/883B	6100	IO-30	Chip	MCG	Parallel Input-Output Port;-55 to 125°C,4 to 11V,Mil Std 883B	INL
21	IM6103CPL	6100	IO-30	Chip	MCG	Parallel Input-Output Port;0 to 70°C,4 to 7V,40 Pin Plastic Pkg	INL
22	IM6103IDL	6100	IO-30	Chip	MCG	Parallel Input-Output Port;-40 to 85°C,4 to 7V,40 Pin Cer Pkg	INL
23	IM6103IPL	6100	IO-30	Chip	MCG	Parallel Input-Output Port;-40 to 85°C,4 to 7V,40 Pin Plastic Pkg	INL
24	IM6103MDL	6100	IO-30	Chip	MCG	Parallel Input-Output Port;-55 to 125°C,4 to 7V,40 Pin Cer Pkg	INL
25	IM6103MDL/883B	6100	IO-30	Chip	MCG	Parallel Input-Output Port;-55 to 125°C,4 to 7V,Mil Std 883B	INL
26	ICL8052ACDD/7103ACDI	6100	IO-41	ChS		4 1/2 Digit Precision A/D Pair;MUX BCD Out;Ceramic DIP	INL
27	ICL8052ACPD/7103ACPI	6100	IO-41	ChS		4 1/2 Digit Precision A/D Pair;MUX BCD Out;Plastic DIP	INL
28	ICL8052CDD/7101CDL	6100	IO-41	ChS		3 1/2 Digit A/D Pair;Parall BCD Out For LCDs Or Data Bus;Ceramic DIP	INL
29	ICL8052CDD/7103CDI	6100	IO-41	ChS		3 1/2 Digit Precision A/D Pair;MUX BCD Out;Ceramic DIP	INL
30	ICL8052CPD/7101CPL	6100	IO-41	ChS		3 1/2 Digit A/D Pair;Parall BCD Out For LCDs Or Data Bus;Plastic DIP	INL
31	ICL8052CPD/7103CPI	6100	IO-41	ChS		3 1/2 Digit Precision A/D Pair;MUX BCD Out;Plastic DIP	INL
32	IM56S26CD	6100	PROM	Chip	BTX	1024x4 Electrically Programmable;Tri-State Ceramic Commercial	INL
33	IM56S26CJ	6100	PROM	Chip	BTX	1024x4 Electrically Programmable;Tri-State Cerdip Commercial	INL
34	IM56S26MD	6100	PROM	Chip	BTX	1024x4 Electrically Programmable;Tri-State Ceramic Military	INL
35	IM56S26MJ	6100	PROM	Chip	BTX	1024x4 Electrically Programmable;Tri-State Cerdip Military	INL
36	IM5600CFE	6100	PROM	Chip	BTX	256x1 Programmable ROM;0-75°C,16 Pin Flatpack Pkg	INL
37	IM5603ACFE	6100	PROM	Chip	BTX	256x4 Programmable ROM;Max Access Time 60ns,0-75°C,16 Pin Flatpack	INL
38	IM5603ACPE	6100	PROM	Chip	BTX	256x4 Programmable ROM;Max Access Time 60ns,0-75°C,16 Pin Plastic	INL
39	IM5605ACDG	6100	PROM	Chip	MCS	512x8 Programmable ROM;Max Access Time 55ns,0-75°C,24 Pin Ceramic	INL
40	IM5605ACJG	6100	PROM	Chip	MCS	512x8 Programmable ROM;Max Access Time 55ns,0-75°C,24 Pin Cerdip	INL
41	IM5605AMDG	6100	PROM	Chip	MCS	512x8 Programmable ROM;Max Access Time 70ns,-55-125°C,24 Pin Ceramic	INL
42	IM5605AMJG	6100	PROM	Chip	MCS	512x8 Programmable ROM;Max Access Time 70ns,-55-125°C,24 Pin Cerdip	INL
43	IM5605CDG	6100	PROM	Chip	BTX	512x8 Programmable ROM;Max Access Time 70ns,0-75°C;24 Pin Ceramic	INL
44	IM5605MDG	6100	PROM	Chip	BTX	512x8 Programmable ROM;Max Access Time 80ns,-55-125°C;24 Pin Ceramic	INL
45	IM5610CFE	6100	PROM	Chip	BTX	256x1 Programmable ROM;0-75°C,16 Pin Flatpack Pkg	INL
46	IM5623CFE	6100	PROM	Chip	BTX	256x4 Programmable ROM;Max Access Time 65ns,0-75°C,16 Pin Flatpack	INL
47	IM5623CPE	6100	PROM	Chip	BTX	256x4 Programmable ROM;Max Access Time 65ns,0-75°C,16 Pin Plastic	INL
48	IM5625ACDG	6100	PROM	Chip	MCS	512x8 Programmable ROM;Max Access Time 55ns,0-75°C,24 Pin Ceramic	INL
49	IM5625ACJG	6100	PROM	Chip	MCS	512x8 Programmable ROM;Max Access Time 55ns,0-75°C,24 Pin Cerdip	INL
50	IM5625AMDG	6100	PROM	Chip	MCS	512x8 Programmable ROM;Max Access Time 70ns,-55-125°C,24 Pin Ceramic	INL
51	IM5625AMJG	6100	PROM	Chip	MCS	512x8 Programmable ROM;Max Access Time 70ns,-55-125°C,24 Pin Cerdip	INL
52	IM5625CDG	6100	PROM	Chip	BTX	512x8 Programmable ROM;Max Access Time 70ns,0-75°C;24 Pin Ceramic	INL
53	IM5625MDG	6100	PROM	Chip	BTX	512x8 Programmable ROM;Max Access Time 80ns,-55-125°C;24 Pin Ceramic	INL
54	IM6508-1IJE	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Industrial:-40 To 85°C	INL
55	IM6508A-1IJE	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Industrial:-40 To 85°C	INL
56	IM6508AIJE	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Industrial:-40 To 85°C	INL
57	IM6508CJE	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Commercial:0 To 75°C	INL
58	IM6508IJE	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Industrial:-40 To 85°C	INL
59	IM6512AIDN	6100	RAM	Chip	MCG	64x12 Static RAM;Industrial Ceramic DIP;Operating Voltage:4-11 Volts	INL
60	IM6512AIJN	6100	RAM	Chip	MCG	64x12 Static RAM;Industrial Cerdip Pkg;Operating Voltage:4-11 Volts	INL
61	IM6512AMDN	6100	RAM	Chip	MCG	64x12 Static RAM;Military Ceramic DIP;Operating Voltage:4-11 Volts	INL
62	IM6512AMFN	6100	RAM	Chip	MCG	64x12 Static RAM;Military Flatpack;Operating Voltage:4-11 Volts	INL
63	IM6512AMJN	6100	RAM	Chip	MCG	64x12 Static RAM;Military Cerdip Pkg;Operating Voltage:4-11 Volts	INL
64	IM6518-1IJN	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Industrial:-40 To 85°C	INL
65	IM6518A-1IJN	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Industrial:-40 To 85°C	INL
66	IM6518AIJN	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Industrial:-40 To 85°C	INL
67	IM6518CJN	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Commercial:0 To 75°C	INL
68	IM6518IJN	6100	RAM	Chip	MCG	1024x1 Bit Static RAM;Cerdip Pkg;Industrial:-40 To 85°C	INL
69	IM6523MFE	6100	RAM	Chip	MCG	256Wx1 Bit Static RAM;-55 To 125°C;FE Pkg	INL
70	IM6551AIDF	6100	RAM	Chip	MCG	256Wx4 Bit Static RAM;-40 To 85°C;DF Pkg	INL
71	IM6551AMDF	6100	RAM	Chip	MCG	256Wx4 Bit Static RAM;-55 To 125°C;DF Pkg	INL
72	IM6561AIDN	6100	RAM	Chip	MCG	256Wx4 BIT Static RAM;-40 To 85°C;DN Pkg	INL
73	IM6561AIJN	6100	RAM	Chip	MCG	256x4 Bit Static RAM;Cerdip Pkg;Industrial: -40 To 85°C	INL
74	IM6561AMDN	6100	RAM	Chip	MCG	256Wx4 Bit Static RAM;-55 To 125°C;DN Pkg	INL
75	IM6561CJN	6100	RAM	Chip	MCG	256x4 Bit Static RAM;Cerdip Pkg;Commercial:0 To 75°C	INL
76	IM6561IDN	6100	RAM	Chip	MCG	256Wx4 Bit Static RAM;-40 To 85°C;DN Pkg	INL
77	IM6561IJN	6100	RAM	Chip	MCG	256x4 Bit Static RAM;Cerdip Pkg;Industrial:-40 To 85°C	INL
78	IM6561MDN	6100	RAM	Chip	MCG	256Wx4 Bit Static RAM;-55 To 125°C;DN Pkg	INL
79	IM6312AIJN	6100	ROM	Chip	MCG	1024x12 Bit Static ROM;Cerdip Pkg;Industrial:-40 To 85°C	INL
80	IM6312CJN	6100	ROM	Chip	MCG	1024x12 Bit Static ROM;Cerdip Pkg;Commercial:0 To 75°C	INL
81	IM6312IJN	6100	ROM	Chip	MCG	1024x12 Bit Static ROM;Cerdip Pkg;Industrial:-40 To 85°C	INL
82	C8237		IO-03	Chip		Programmable DMA Controller;Expandable To Any # Channel	ITL
83	C8237-2		IO-03	Chip		Programmable DMA Controller;Expandable to any # Channel	ITL
84	D8237		IO-03	Chip		Programmable DMA Controller;Expandable to any # Channel	ITL
85	D8237-2		IO-03	Chip		Programmable DMA Controller;Expandable to any # Channel	ITL
86	P8237		IO-03	Chip		Programmable DMA Controller;Expandable to any # Channel	ITL
87	P8237-2		IO-03	Chip		Programmable DMA Controller;Expandable to any # Channel	ITL
88	MDS-UPP	INTELLEC800	DEV	UNIT	MNG	Universal PROM Programmer	ITL
89	UPP103	INTELLEC800	DEV	UNIT		Universal PROM Programmer;Includes Power Supply,Software Etc	ITL
90	MDS501	INTELLEC800	IO-03	MOD	MNG	Development DMA Channel Controller	ITL
91	MDS504	INTELLEC800	IO-33	UNIT	MNG	Development General Purpose I/O Module	ITL
92	MDS360	INTELLEC800	PE-02	UNIT		Devl Sgl/Dbl Den Diskette for Editing ASCII Text Under ISIS-II Oper Sys	ITL
93	MDS-2DS	INTELLEC800	PE-02	UNIT		Devel Diskette Operating Syst;Includes 2 Drive Units Etc	ITL
94	MDS-BLD	INTELLEC800	PE-02	UNIT		Devl,Pkg of 10 Blank Diskettes for Use on MDS-DDS	ITL
95	MDS-DDR	INTELLEC800	PE-02	UNIT		Devel Double Density Diskette Add on Drive;115V/220V	ITL
96	MDS-DDS	INTELLEC800	PE-02	UNIT		Devel Double Density Diskette Operating System;115V/220V	ITL
97	MDS-DOS	INTELLEC800	PE-02	UNIT	MNG	Development;Diskette Operating System	ITL
98	MDS-DRV	INTELLEC800	PE-02	UNIT		Devel Diskette Drive;Add on Drive Unit;115V/220V	ITL
99	MDS770	INTELLEC800	PE-10	UNIT		5x7 Dot Matrix Unidir Printer,60 Char/Sec,Line Width Varible	ITL
100	MDS-PRN	INTELLEC800	PE-10	UNIT		Devl,5x7 Matrix Line Buffered Printer	ITL
101	MDS-CRT	INTELLEC800	PE-23	UNIT		Devl,Alpha numeric Keyboard Cathode Ray Tube Display Console	ITL
102	MDS-PTR	INTELLEC800	PE-42	UNIT	MNG	High Speed Paper Tape Reader	ITL
103	UPP101	INTELLEC800	PE-50	UNIT		Universal PROM Programmer;For Programming And Verifying W/16/24 Pin Sock	ITL
104	UPP102	INTELLEC800	PE-50	UNIT		Universal PROM Programmer;For Programming And Verifying W/24/24 Pin Sock	ITL

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MDS406	INTELLEC800	PROM	MOD	MNG	Development;6k PROM	ITL
2	MDS416	INTELLEC800	PROM	MOD	MNG	Development;16k PROM	ITL
3	MDS016	INTELLEC800	RAM	MOD	MNG	Development;16k Dynamic RAM	ITL
4	INTELLEC888	INTELLEC888	DEV	UNIT		Complete INTELLEC Microcomputer Development Center	ITL
5	C4040	MCS40	CPU	Chip	MPG	4 Bit Parallel Central Processor Unit,Ceramic Pkg	ITL
6	P4040	MCS40	CPU	Chip	MPG	4 Bit Parallel Central Processor Unit,Plastic Pkg	ITL
7	4/MOD40	MCS40	DEV	UNIT	MPX	Self Contained Microcomputer Development System	ITL
8	PA4-04	MCS40	DEV	UNIT	MPX	Program Analyzer	ITL
9	D4289	MCS40	IO-03	Chip		Standard Mem Interface;Includes 4 Bit Bidir Port	ITL
10	P4289	MCS40	IO-03	Chip	MPX	Standard Memory Interface,I/O Interface	ITL
11	C4269	MCS40	IO-09	Chip		Programmable Keyboard Display Device;Ceramic Pkg	ITL
12	P4269	MCS40	IO-09	Chip		Programmable Keyboard Display Device;Plastic Pkg	ITL
13	D3226	MCS40	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver/Receiver,Inverted I/O,Cer Dip Pkg	ITL
14	MD3226	MCS40	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver/Receiver,Inverted I/O,Cer Dip Pkg	ITL
15	P3226	MCS40	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver/Receiver,Inverted I/O,Plastic Pkg	ITL
16	D4265	MCS40	IO-30	Chip	MPX	Programmable Gen Purpose IO:Ceramic Pkg	ITL
17	P4265	MCS40	IO-30	Chip	MPX	Programmable I/O Device	ITL
18	C4201	MCS40	IO-32	Chip	MCX	Clock Generator With Crystal Controlled Oscillator,Ceramic Pkg	ITL
19	D4201	MCS40	IO-32	Chip	MCX	Clock Generator With Crystal Controlled Oscillator,Cer Dip Pkg	ITL
20	D4201A	MCS40	IO-32	Chip		Clock Generator;MOS/TTL Level Clock Output;Ceramic Pkg	ITL
21	P4201	MCS40	IO-32	Chip	MCX	Clock Generator With Crystal Controlled Oscillator,Plastic Pkg	ITL
22	P4201A	MCS40	IO-32	Chip		Clock Generator;MOS/TTL Level Clock Output;Plastic Pkg	ITL
23	P4207	MCS40	IO-33	Chip	MPX	I/O Devices,2 4 Bit Output Ports	ITL
24	P4209	MCS40	IO-33	Chip	MPX	I/O Devices,2 4 Bit Output Ports	ITL
25	P4211	MCS40	IO-33	Chip	MPX	I/O Devices,2 4 Bit Input,2 4 Bit Output Ports	ITL
26	C4003	MCS40	IO-55	Chip	MPX	10 Bit Output Expander/Shift Register,Ceramic Pkg	ITL
27	D4003	MCS40	IO-55	Chip	MPX	10 Bit Output Expander/Shift Register,Cer Dip Pkg	ITL
28	P4003	MCS40	IO-55	Chip	MPX	10 Bit Output Expander/Shift Register,Plastic Pkg	ITL
29	C4001	MCS40	IO-57	Chip	MPX	256 x 8 Mask Programmable ROM And 4 Bit I/O Port,Ceramic Pkg	ITL
30	C4002-1	MCS40	IO-57	Chip	MPX	320 Bit RAM And 4 Bit Output Port,Ceramic Pkg	ITL
31	C4308	MCS40	IO-57	Chip		1024x8 Mask Programmable ROM and Four 4 Bit I/O Ports;Cer Pkg	ITL
32	D4001	MCS40	IO-57	Chip	MPX	256 x 8 Mask Programmable ROM And 4 Bit I/O Port,Cer Dip Pkg	ITL
33	D4002-1	MCS40	IO-57	Chip	MPX	320 Bit RAM And 4 Bit Output Port,Cer Dip Pkg	ITL
34	P4001	MCS40	IO-57	Chip	MPX	256 x 8 Mask Programmable ROM And 4 Bit I/O Port,Plastic Pkg	ITL
35	P4002-1	MCS40	IO-57	Chip	MPX	320 Bit RAM And 4 Bit Output Port, Plastic Pkg	ITL
36	P4308	MCS40	IO-57	Chip	MPX	1024 x 8 ROM With 4 I/O Ports	ITL
37	C4101	MCS40	RAM	Chip	MNG	256 x 4 Static RAM With Separate I/O,Ceramic Pkg	ITL
38	P4101	MCS40	RAM	Chip	MNG	256 x 4 Static RAM With Separate I/O,Plastic Pkg	ITL
39	C4302	MCS40	ROM	Chip	MXG	256 x 8 Erasable And Mask Programmable ROM,Ceramic Pkg	ITL
40	C4316A	MCS40	ROM	Chip	MNG	2048 x 8 Static ROM,16384 Bit,Ceramic Pkg	ITL
41	C4702A	MCS40	ROM	Chip	MPG	256x8 Erasable And Electrically Programmable ROM,Ceramic Pkg	ITL
42	P4302	MCS40	ROM	Chip	MXG	256 x 8 Erasable And Mask Programmable ROM,Plastic Pkg	ITL
43	P4316A	MCS40	ROM	Chip	MNG	2048 x 8 Static ROM,16384 Bit,Plastic Pkg	ITL
44	P4702A	MCS40	ROM	Chip	MPG	256x8 Erasable And Electrically Programmable ROM,Plastic Pkg	ITL
45	B8748	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer W/User Program ErasableEPROM;CT2.5us	ITL
46	B8748-8	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer W/User Program Erasable EPROM;CT5us	ITL
47	C8748-4	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;1kx8 EPROM,64x8 RAM,27 IO Lines	ITL
48	D8035	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer Without Program Mem;Cycle Time2.5us	ITL
49	D8035-4	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;Ext ROM/PROM,64x8 RAM,27 IO Lines	ITL
50	D8035-8	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer Without Program Mem;Cycle Time 5us	ITL
51	D8039	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;Ext ROM/PROM,128x8 RAM,27 IO Lines	ITL
52	D8039-6	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;Ext ROM/PROM,128x8 RAM,27 IO Lines	ITL
53	D8048	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer W/Mask Program ROM;Cycle Time 2.5us	ITL
54	D8049	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;2kx8 ROM,128x8 RAM,27 IO Lines	ITL
55	P8021	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;1kx8 ROM,64x8 RAM,CPU,21 IO Lines	ITL
56	P8022	MCS48	uCT	Chip		Single Component 8 Bit Microcomputer;2kx8 ROM,64x8 RAM,8B ADC,28IO Lines	ITL
57	P8035	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer Without Program Mem;Cycle Time2.5us	ITL
58	P8035-4	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;Ext ROM/PROM,64x8 RAM,27 IO Lines	ITL
59	P8035-8	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer Without Program Mem;Cycle Time 5us	ITL
60	P8039	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;Ext ROM/PROM,128x8 RAM,27 IO Lines	ITL
61	P8039-6	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;Ext ROM/PROM,128x8 RAM,27 IO Lines	ITL
62	P8048	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer W/Mask Program ROM;Cycle Time 2.5us	ITL
63	P8048-8	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer W/Mask Program ROM;Cycle Time 5us	ITL
64	P8049	MCS48	uCT	Chip	MNG	Single Component 8 Bit Microcomputer;2kx8 ROM,128x8 RAM,27 IO Lines	ITL
65	MDS-EM1	MCS48	DEV	MOD		8021 Emulation Board;Contains 8748 to Store and Execute 8021 Progm	ITL
66	MDS-EM2	MCS48	DEV	MOD		8022 Emulation Board;W/8022 Emulator Chip and 8755A 2kx8 EPROM Memory	ITL
67	MDS-ICE48	MCS48	DEV	MOD		MCS48 CPU in Ckt Emulator Includes Hardware and Software	ITL
68	MDS-ICE49	MCS48	DEV	MOD		MDS48 CPU In-Ckt Emulator;Static RAM Memory Available	ITL
69	PROMPT48	MCS48	DEV	UNIT	MNG	MCS 48 Design And Development Aid:Contains 8748 Processor	ITL
70	B8243	MCS48	IO-33	Chip	MNG	Input/Ouput Expander;Four 4-Bit I/O Ports	ITL
71	C8243	MCS48	IO-33	Chip	MNG	Input/Output Expander;Four 4-Bit I/O Ports	ITL
72	D8243	MCS48	IO-33	Chip	MNX	Input/Output Expander;Four 4 Bit I/O Ports;Hermetic Pkg	ITL
73	B8741A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for 8-Bit Systems;Prog Mem in EPROM	ITL
74	C8641A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for 8-Bit System;One Time Prog (at Factory)	ITL
75	C8741A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for 8-Bit System;Prog Mem in EPROM	ITL
76	D8041A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for 8-Bit System;Prog Memory in ROM	ITL
77	D8641A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for 8-Bit System;One Time Prog (at Factory)	ITL
78	D8741A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for 8-Bit System;Prog Mem in EPROM	ITL
79	P8041A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for 8-Bit Systems;Prog Mem in ROM	ITL
80	P8641A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for 8-Bit System;One Time Prog (at Factory)	ITL
81	P8741A	MCS48,80	IO-33	Chip		Univ Peripheral Interface for 8-Bit System;Prog Mem in EPROM	ITL
82	D8253-5	MCS48,80,85	IO-01	Chip	MNG	Programmable Interval Timer	ITL
83	C8008	MCS8	CPU	Chip	MNG	8 Bit Microprocessor;Instruction Cycle Time 20us	ITL
84	C8008-1	MCS8	CPU	Chip	MNG	8 Bit Microprocessor;Instruction Cycle Time 1.25us	ITL
85	C8080A1	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit,Instruction Cycle 1.3us	ITL
86	C8080A2	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit,Instruction Cycle 1.5us	ITL
87	C8080A	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit,Instruction Cycle 2.0us	ITL
88	D8080A1	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit;Inst Cycle 1.3us;Cer Pkg	ITL
89	D8080A2	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit;Inst Cycle 1.5us;Cer Pkg	ITL
90	D8080A	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit;Inst Cycle 2.0us;Cer Pkg	ITL
91	MC8080A	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit,Military Temp	ITL
92	MD8080A	MCS80	CPU	Chip		8 Bit Central Processor Unit,Mil Screening Level B,C	ITL
93	P8080A1	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit;Inst Cycle 1.3us;Plastic Pkg	ITL
94	P8080A2	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit;Inst Cycle 1.5us;Plastic Pkg	ITL
95	P8080A	MCS80	CPU	Chip	MNG	8 Bit Parallel Central Processing Unit;Inst Cycle 2.0us;Plastic Pkg	ITL
96	imm8-83	MCS80	CPU	MOD	MNG	Development;Central Processor Module Using 8080 CPU	ITL
97	imm8-61	MCS80	DEV	MOD	MNG	Development;Input/Output Module	ITL
98	imm8-63	MCS80	DEV	MOD	MNG	Development;Output Module,8 8 Bit Latching Output Ports	ITL
99	MDS-ICE80	MCS80	DEV	MOD		8080CPU in Ckt Emulator Includes Hardware and Software	ITL
100	SDK80	MCS80	DEV	MOD		8080 System Design Kit;Uses 8080A CPU	ITL
101	BAREBONES80	MCS80	DEV	UNIT	MNG	Microcomputer Subsystem Using 8080 CPU	ITL
102	MDS800	MCS80	DEV	UNIT		Basic MDS800 Includes 8080 CPU,Universal Bus W/Multiprocessor	ITL
103	PRB80	MCS80	DEV	UNIT		uSCOPE Probe 8080A for Interconn Between 8080A Sys and uSCOPE 820	ITL
104	PROMPT80	MCS80	DEV	UNIT	MNG	MCS80 Design And Development Aid	ITL
105	USC10KIT	MCS80	DEV	UNIT		U Scope Kit Consisting of U SCOPE 820 and Probe 8080A	ITL
106	USC820	MCS80	DEV	UNIT		uSCOPE 820;Portable Sys Console to Evaluate,Debug 8-Bit uC Systems	ITL
107	D8253	MCS80	IO-01	Chip	MNG	Programmable Interval Timer,Cer Dip Pkg	ITL
108	C8228	MCS80	IO-02	Chip	BTD	System Controller And Bi-Directional Bus Driver,Ceramic Pkg	ITL
109	C8238	MCS80	IO-02	Chip	BTD	System Controller and Bus Driver;0-70°C	ITL
110	D8228	MCS80	IO-02	Chip	BTD	System Controller And Bi-Directional Bus Driver,Cer Dip Pkg	ITL

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	D8259	MCS80	IO-02	Chip		Programmable Interrupt Controller	ITL
2	MD8214	MCS80	IO-02	Chip		Interrupt Control Unit,Mil Screening Level B,C	ITL
3	P8228	MCS80	IO-02	Chip	BTD	System Controller And Bi-Directional Bus Driver,Plastic Pkg	ITL
4	P8238	MCS80	IO-02	Chip		System Controller and Bus Driver for 8080A;Plastic Pkg	ITL
5	P8259	MCS80	IO-02	Chip		Programmable Interrupt Controller	ITL
6	C8222	MCS80	IO-03	Chip	BTD	Dynamic Memory Refresh Controller,Ceramic Pkg	ITL
7	D8257	MCS80	IO-03	Chip		Programmable DMA Controller	ITL
8	P8222	MCS80	IO-03	Chip	BTD	Dynamic Memory Refresh Controller,Plastic Pkg	ITL
9	P8257	MCS80	IO-03	Chip		Programmable DMA Controller	ITL
10	MD8228	MCS80	IO-07	Chip		System Controller and Bus Driver;Mil Screening Level B,C	ITL
11	C8275	MCS80	IO-09	Chip		Programmable CRT Controller	ITL
12	D8275	MCS80	IO-09	Chip		Programmable CRT Controller	ITL
13	C8218	MCS80	IO-11	Chip	BXX	uCOMP Bus Controller;Controls Common Bus Sharing Bet CPUs;28-Pin Pkg	ITL
14	D8218	MCS80	IO-11	Chip	BXX	uCOMP Bus Controller;Controls Common Bus Sharing Bet CPUs;28-Pin Pkg	ITL
15	MD8251	MCS80	IO-20	Chip		Programmable Communications Interface;Mil Screen Level B,C	ITL
16	SBC534	MCS80	IO-20	MOD		4 Channel Communication Board;Sync/Async Comm Channels	ITL
17	C8255	MCS80	IO-30	Chip	MXG	Programmable Peripheral Interface,Ceramic Pkg	ITL
18	C8255A	MCS80	IO-30	Chip		Programmable Peripheral Interface (PPI)	ITL
19	C8255A-5	MCS80	IO-30	Chip		Programmable Peripheral Interface (PPI)	ITL
20	D8255A	MCS80	IO-30	Chip		Programmable Peripheral Interface(PPI)	ITL
21	MD8255A	MCS80	IO-30	Chip		Programmable Peripheral Interface;Mil Screening Level B,C	ITL
22	C8224	MCS80	IO-32	Chip	BTD	Clock Generator And Driver Controlled By A Crystal,Ceramic Pkg	ITL
23	D8210	MCS80	IO-32	Chip	MNX	TTL-TO-MOS Level Shifter And High Voltage Clock Driver,Cer Dip Pkg	ITL
24	D8224	MCS80	IO-32	Chip	BTD	Clock Generator And Driver Controlled By A Crystal,Cer Dip Pkg	ITL
25	MD8224	MCS80	IO-32	Chip		Clock Generator/Driver for 8080A;Mil Screening Level B,C	ITL
26	P8224	MCS80	IO-32	Chip	BTD	Clock Generator And Driver Controlled By A Crystal,Plastic Pkg	ITL
27	MD8212	MCS80	IO-33	Chip		8 Bit Input/Output Port,Mil Screening Level B,C	ITL
28	P8210	MCS80	IO-33	Chip	MNX	TTL-TO-MOS Level Shifter And High Voltage Clock Driver,Plastic Pkg	ITL
29	SBC556	MCS80	IO-33	MOD		Optically Isolated I/O Board;48 Op Isolated Data Lines	ITL
30	C8155	MCS80	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer Active Lo CE,400ns Max Access Time	ITL
31	C8156	MCS80	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer Active Hi CE,400ns Max Access Time	ITL
32	P8156	MCS80	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer Active Hi CE,400ns Max Access Time	ITL
33	B8702A-4	MCS80	PROM	Chip		2048 Bit Erasable and Electrically Reprogrammable PROM,Hermetic	ITL
34	C8702A	MCS80	PROM	Chip	MPG	256 x 8 Erasable And Electrically Reprogrammable ROM,Ceramic Pkg	ITL
35	C8704	MCS80	PROM	Chip	MNG	572 x 8 Erasable And Electrically Reprogrammable ROM,Ceramic Pkg	ITL
36	MC8702A	MCS80	PROM	Chip		UV Erasable/Electrically Programmable 2048 Bit PROM;-55 to 100°C	ITL
37	MC8708	MCS80	PROM	Chip		UV Erasable/Electrically Programmable 8096 Bit PROM;-55 to 100°C	ITL
38	C5101	MCS80	RAM	Chip	MCG	256 x 4 Static CMOS RAM,Ceramic Pkg	ITL
39	C5101-3	MCS80	RAM	Chip	MCG	256 x 4 Static CMOS RAM,Ceramic Pkg	ITL
40	C5101L3	MCS80	RAM	Chip	MCG	256 x 4 Static CMOS RAM,Guaranteed Data Retention At 2.0V,Ceramic Pkg	ITL
41	C8101-2	MCS80	RAM	Chip	MNG	256 x 4 RAM With Separate I/O,Ceramic Pkg	ITL
42	C8102-2	MCS80	RAM	Chip	MNG	1024 Bit Fully Decoded Static RAM,Ceramic Pkg	ITL
43	C8102A4	MCS80	RAM	Chip	MNG	1024 Bit Fully Decoded Static RAM,Ceramic Pkg	ITL
44	C8107B4	MCS80	RAM	Chip	MNG	4096 Bit Fully Decoded Dynamic RAM,Ceramic Pkg	ITL
45	C8111-2	MCS80	RAM	Chip	MNG	256 x 4 RAM With Common I/O And Output Disable Ceramic Pkg	ITL
46	MD8102A4	MCS80	RAM	Chip		1024 Bit Fully Decoded Static RAM,Mil Screening Level B,C	ITL
47	MD8111A	MCS80	RAM	Chip		256x4 Bit Fully Decoded Static RAM,Mil Screening Level B,C	ITL
48	P5101-3	MCS80	RAM	Chip	MCG	256 x 4 Static CMOS RAM,Plastic Pkg	ITL
49	P5101L3	MCS80	RAM	Chip	MCG	256 x 4 Static CMOS RAM,Guaranteed Data Retention At 2.0V,Plastic Pkg	ITL
50	P8101-2	MCS80	RAM	Chip	MNG	256 x 4 RAM With Separate I/O,Plastic Pkg	ITL
51	P8102-2	MCS80	RAM	Chip	MNG	1024 Bit Fully Decoded Static RAM,Plastic Pkg	ITL
52	P8102A4	MCS80	RAM	Chip	MNG	1024 Bit Fully Decoded Static RAM,Plastic Pkg	ITL
53	P8107B4	MCS80	RAM	Chip	MNG	4096 Bit Fully Decoded Dynamic RAM,Plastic Pkg	ITL
54	P8111-2	MCS80	RAM	Chip	MNG	256 x 4 RAM With Common I/O And Output Disable,Plastic Pkg	ITL
55	C8302	MCS80	ROM	Chip	MPG	256 x 8 Mask Programmable ROM,Ceramic Pkg	ITL
56	D8316A	MCS80	ROM	Chip		Mask Programmable 16,384 Bit Static ROM	ITL
57	P8302	MCS80	ROM	Chip	MPG	256 x 8 Mask Programmable ROM,Plastic Pkg	ITL
58	C8214	MCS80,48	IO-02	Chip	BTD	8 Level Priority Interrupt Control Unit,Ceramic Pkg	ITL
59	D8214	MCS80,48	IO-02	Chip	BTD	8 Level Priority Interrupt Control Unit,Cer Dip Pkg	ITL
60	P8214	MCS80,48	IO-02	Chip	BTD	8 Level Priority Interrupt Control Unit,Plastic Pkg	ITL
61	C8216	MCS80,48	IO-21	Chip	BTD	4-Bit Parallel Bidirectional Bus Driver	ITL
62	D8216	MCS80,48	IO-21	Chip	BTD	4 Bit Parallel Bidirectional Bus Driver,Cer Dip Pkg	ITL
63	D8226	MCS80,48	IO-21	Chip	BTD	4 Bit Parallel Bidirectional Bus Driver,Cer Dip Pkg	ITL
64	P8216	MCS80,48	IO-21	Chip	BTD	4 Bit Parallel Bidirectional Bus Driver,Plastic Pkg	ITL
65	P8226	MCS80,48	IO-21	Chip	BTD	4 Bit Parallel Bidirectional Bus Driver,Plastic Pkg	ITL
66	B8212	MCS80,48	IO-33	Chip	BTD	8-Bit Input/Output Port;3-State Output;Buffer	ITL
67	D8212	MCS80,48	IO-33	Chip	BTD	8 Bit Input/Output Port,3-State Output Buffer,Cer Dip Pkg	ITL
68	P8212	MCS80,48	IO-33	Chip	BTD	8 Bit Input/Output Port,3-State Output Buffer,Plastic Pkg	ITL
69	P8243	MCS80,48	IO-33	Chip		16 Line I/O Extender For 8035,8048 And 8748 Microcomputers	ITL
70	D8205	MCS80,48	IO-44	Chip	BTD	1 Out Of 8 High Speed Binary Decoder,Cer Dip Pkg	ITL
71	P8205	MCS80,48	IO-44	Chip	BTD	1 Out Of 8 High Speed Binary Decoder,Plastic Pkg	ITL
72	C8708	MCS80,48	PROM	Chip	MNG	1024 x 8 Erasable And Electrically Reprogrammable ROM,Ceramic Pkg	ITL
73	B8101A4	MCS80,48	RAM	Chip	MNG	256x4 Static RAM With Separate I/O;Improved Version;Ceramic Pkg	ITL
74	D8111A4	MCS80,48	RAM	Chip	MNG	256x4 Static RAM With Common I/O;Improved Version;Ceramic Pkg	ITL
75	P5101	MCS80,48	RAM	Chip	MCG	256 x 4 Static CMOS RAM,Plastic Pkg	ITL
76	P8101A4	MCS80,48	RAM	Chip	MNG	256x4 Static RAM With Separate I/O;Improved Version;Plastic Pkg	ITL
77	P8111A4	MCS80,48	RAM	Chip	MNG	256x4 Static RAM With Common I/O;Improved Version;Plastic Pkg	ITL
78	C8308	MCS80,48	ROM	Chip	MNG	1024 x 8 Static Mask Programmable ROM,Ceramic Pkg	ITL
79	C8316A	MCS80,48	ROM	Chip	MNG	2048 x 8 Static ROM,16384 Bit,Ceramic Pkg	ITL
80	P8308	MCS80,48	ROM	Chip	MNG	1024 x 8 Static Mask Programmable ROM,Plastic Pkg	ITL
81	P8316A	MCS80,48	ROM	Chip	MNG	2048 x 8 Static ROM,16384 Bit,Plastic Pkg	ITL
82	C7220	MCS80,85	IO-03	Chip	BTX	Bubble Memory Controller; DMA Handshake Capability; 9-Bit Parallel Bus	ITL
83	C8202	MCS80,85	IO-03	Chip		Dynamic RAM Controller;Can Control 2104A,2116,2117 Mem	ITL
84	D7220	MCS80,85	IO-03	Chip	BTX	Bubble Memory Controller; DMA Handshake Capability;9-Bit Parallel Bus	ITL
85	D8202	MCS80,85	IO-03	Chip		Dynamic RAM Controller;Can Control 2104A,2116,2117 Mem	ITL
86	P7220	MCS80,85	IO-03	Chip	BTX	Bubble Memory Controller; DMA Handshake Capability;9-Bit Parallel Bus	ITL
87	P8202	MCS80,85	IO-03	Chip		Dynamic RAM Controller;Can Control 2104A,2116,2117 Mem	ITL
88	P8218	MCS80,85	IO-11	Chip	BXX	uComputer Bus Controller;Controls Common Bus Sharing Bet CPUs;28 Pin Pkg	ITL
89	P8219	MCS80,85	IO-11	Chip	BXX	uComputer Bus Controller;Controls Common Bus Sharing Bet CPUs;28 Pin Pkg	ITL
90	C7230	MCS80,85	IO-32	Chip	BTX	Current Pulse Generator for Bubble Memories;Direct Interface w/C7220	ITL
91	D7230	MCS80,85	IO-32	Chip	BTX	Current Pulse Generator for Bubble Memories;Direct Interface w/C7220	ITL
92	P7230	MCS80,85	IO-32	Chip	BTX	Current Pulse Generator for Bubble Memories;Direct Interface w/C7220	ITL
93	C8231	MCS80,85	IO-90	Chip	MNG	Arithmetic Processing Unit;Add,Subtract,Multiply and Divide	ITL
94	C8232	MCS80,85	IO-90	Chip	MNG	Floating Point Processor;Single/Double Precision	ITL
95	D8231	MCS80,85	IO-90	Chip	MNG	Arithmetic Processing Unit;Add,Subtract,Multiply and Divide	ITL
96	D8232	MCS80,85	IO-90	Chip	MNG	Floating Point Processor;Single/Double Precision	ITL
97	P8231	MCS80,85	IO-90	Chip	MNG	Arithmetic Processing Unit;Add,Subtract,Multiply and Divide	ITL
98	P8232	MCS80,85	IO-90	Chip	MNG	Floating Point Processor;Single/Double Precision	ITL
99	INTELLEC800	MCS80,85,48	DEV	UNIT	MNG	Microcomputer Development System Using 8080 CPU	ITL
100	MDS210	MCS80,85,48	DEV	UNIT		Intellec Series II Model 210 Microcomp Development System,Options	ITL
101	MDS220	MCS80,85,48	DEV	UNIT		Intellec Series II Model 220 Microcomp Development System,Options	ITL
102	MDS230	MCS80,85,48	DEV	UNIT		Intellec Series II Model 230 Microcomp Development System,Options	ITL
103	C8253	MCS80,85,48	IO-01	Chip	MNG	Programmable Interval Timer,Ceramic Pkg	ITL
104	P8253	MCS80,85,48	IO-01	Chip	MNG	Programmable Interval Timer,Plastic Pkg	ITL
105	C8251	MCS80,85,48	IO-20	Chip	MNG	Programmable Communication Interface,USART,Ceramic Pkg	ITL
106	D8259A	MCS80,85,86	IO-02	Chip	MNX	Programmable Interrupt Controller,Vcc 5V ±10%,8 Level Cont	ITL
107	D8259A-8	MCS80,85,86	IO-02	Chip	MNX	Programmable Interrupt Controller,Vcc 5V ±5%,TWLWH 400ns	ITL
108	P8259A	MCS80,85,86	IO-02	Chip	MNX	Programmable Interrupt Controller,Vcc 5V ±10%,8 Level Cont	ITL
109	P8259A-8	MCS80,85,86	IO-02	Chip	MNX	Programmable Interrupt Controller,Vcc 5V ±5%,TWLWH 400ns	ITL
110	C8295	MCS80,85,86	IO-08	Chip		Dot Matrix Printer Controller;Programmable Character Density	ITL

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	D8295	MCS80,85,86	IO-08	Chip		Dot Matrix Printer Controller;Programmable Character Density	ITL
2	P8295	MCS80,85,86	IO-08	Chip		Dot Matrix Printer Controller,Programmable Character Density	ITL
3	C8226	MCS8048	IO-21	Chip	BTD	4-Bit Parallel Bidirectional Bus Driver	ITL
4	SDK85	MCS85	COMP	MOD		8-Bit Single-Board Microcomputer Kit;W/6 Digit LED,Keyboard	ITL
5	B8085A	MCS85	CPU	Chip	MNX	Single Chip 8-Bit uProcessor; Instr Cycle Time 1.3us	ITL
6	B8085A-2	MCS85	CPU	Chip	MNX	Single Chip 8-Bit uProcessor; Instr Cycle Time .80us	ITL
7	C8085A2	MCS85	CPU	Chip	MNX	Single Chip 8 Bit Microprocessor;Inst Cycle 0.8us;Cer Pkg	ITL
8	C8085A	MCS85	CPU	Chip	MNX	Single Chip 8 Bit Microprocessor;Inst Cycle 1.3us;Cer Pkg	ITL
9	D8085A	MCS85	CPU	Chip	MNX	Single Chip 8-Bit uProcessor; Instr Cycle Time 1.3us	ITL
10	D8085A-2	MCS85	CPU	Chip	MNX	Single Chip 8-Bit uProcessor; Instr Cycle Time .80us	ITL
11	P8085A2	MCS85	CPU	Chip	MNX	Single Chip 8 Bit Microprocessor;Inst Cycle 800ns;Plastic Pkg	ITL
12	P8085A	MCS85	CPU	Chip	MNX	Single Chip 8 Bit Microprocessor;Inst Cycle 1.3us;Plastic Pkg	ITL
13	MDS-ICE85	MCS85	DEV	MOD		MCS85 CPU in Ckt Emulator Includes Hardware and Software	ITL
14	PRB85	MCS85	DEV	UNIT		Provides Connection Bet uScope 820 and Both 8085 and 8085A Systems	ITL
15	C8253-5	MCS85	IO-01	Chip	MNG	Programmable Interval Timer;Hermatic Pkg	ITL
16	P8253-5	MCS85	IO-01	Chip	MNG	Programmable Interval Timer;Plastic Pkg	ITL
17	D8259-5	MCS85	IO-02	Chip	MNG	8 Level Programmable Interrupt Controller;Herm Pkg	ITL
18	P8259-5	MCS85	IO-02	Chip	MNG	8 Level Programmable Interrupt Controller;Plastic Pkg	ITL
19	C8257	MCS85	IO-03	Chip		Prog DMA Controller;4-Channel;Request Logic;128 Outputs	ITL
20	C8257-5	MCS85	IO-03	Chip		Prog DMA Controller;4-Channel;Request Logic;128 Outputs	ITL
21	D8257-5	MCS85	IO-03	Chip	MNG	4 Channel Programmable DMA Controller;Herm Pkg	ITL
22	P8257-5	MCS85	IO-03	Chip	MNG	4 Channel Programmable DMA Controller;Plastic Pkg	ITL
23	C8271	MCS85	IO-07	Chip	MNX	Programmable Floppy Disk Controller	ITL
24	C8271-6	MCS85	IO-07	Chip	MNX	Programmable Floppy Disk Controller	ITL
25	C8271-8	MCS85	IO-07	Chip	MNX	Programmable Floppy Disk Controller	ITL
26	C8272	MCS85	IO-07	Chip		Single/Double Density Floppy Disk Controller;Programmable	ITL
27	D8271	MCS85	IO-07	Chip	MNX	Programmable Floppy Disk Controller,Ceramic Pkg	ITL
28	D8271-6	MCS85	IO-07	Chip	MNX	Programmable Floppy Disk Controller	ITL
29	D8271-8	MCS85	IO-07	Chip	MNX	Programmable Floppy Disk Controller	ITL
30	D8272	MCS85	IO-07	Chip		Single/Double Density Floppy Disk Controller;Programmable	ITL
31	P8271	MCS85	IO-07	Chip	MNX	Programmable Floppy Disk Controller	ITL
32	P8271-6	MCS85	IO-07	Chip	MNX	Programmable Floppy Disk Controller	ITL
33	P8271-8	MCS85	IO-07	Chip	MNX	Programmable Floppy Disk Controller	ITL
34	P8272	MCS85	IO-07	Chip		Single/Double Density Floppy Disk Controller;Programmable	ITL
35	P8275	MCS85	IO-09	Chip	MNX	Programmable CRT Controller;Cursor Control 4 Types	ITL
36	D8278	MCS85	IO-10	Chip		Programmable Keyboard Interface,Also Interfaces to Display	ITL
37	D8279-5	MCS85	IO-10	Chip	MNX	Programmable Keyboard/Display Interface	ITL
38	P8278	MCS85	IO-10	Chip		Programmable Keyboard Interface,Also Interfaces to Display	ITL
39	P8279-5	MCS85	IO-10	Chip	MNX	Programmable Keyboard/Display Interface	ITL
40	C8219	MCS85	IO-11	Chip	BXX	uCOMP Bus Controller;Controls Common Bus Sharing Bet CPUs;28-Pin Pkg	ITL
41	D8219	MCS85	IO-11	Chip	BXX	uCOMP Bus Controller;Controls Common Bus Sharing Bet CPUs;28-Pin Pkg	ITL
42	C8251A	MCS85	IO-20	Chip	MNG	Program Comm Interface USART;Auto Break Detect/Handling;Ceramic Pkg	ITL
43	C8273	MCS85	IO-20	Chip	MNX	Programmable HDLC/SDLC Protocol Controller	ITL
44	C8273-4	MCS85	IO-20	Chip	MNX	Programmable HDLC/SDLC Protocol Controller	ITL
45	C8273-8	MCS85	IO-20	Chip	MNX	Programmable HDLC/SDLC Protocol Controller	ITL
46	CS2657	MCS85	IO-20	Chip	MNG	Programmable Communication Interface	ITL
47	D8251A	MCS85	IO-20	Chip	MNG	Programmable Communication Interface,Ceramic Pkg	ITL
48	D8273	MCS85	IO-20	Chip	MNX	Programmable HDLC/SDLC Protocol Controller,Cer Pkg	ITL
49	D8273-4	MCS85	IO-20	Chip	MNX	Programmable HDLC/SDLC Protocol Controller	ITL
50	D8273-8	MCS85	IO-20	Chip	MNX	Programmable HDLC/SDLC Protocol Controller	ITL
51	DS2657	MCS85	IO-20	Chip	MNG	Programmable Communication Interface	ITL
52	P8251A	MCS85	IO-20	Chip	MNG	Program Comm Interface USART;Auto Break Detect/Handling;Plastic Pkg	ITL
53	P8273	MCS85	IO-20	Chip	MNX	Programmable HDLC/SDLC Protocol Controller,Plastic Pkg	ITL
54	P8273-4	MCS85	IO-20	Chip	MNX	Programmable HDLC/SDLC Protocol Controller	ITL
55	P8273-8	MCS85	IO-20	Chip	MNX	Programmable HDLC/SDLC Protocol Controller	ITL
56	PS2657	MCS85	IO-20	Chip	MNG	Programmable Communication Interface	ITL
57	D8255A-5	MCS85	IO-30	Chip	MNX	Programmable Peripheral Interface;Herm Pkg	ITL
58	P8255A-5	MCS85	IO-30	Chip	MNX	Programmable Peripheral Interface;Plastic Pkg	ITL
59	C8155-2	MCS85	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer;Active Lo CE;330ns Max Access Time	ITL
60	C8156-2	MCS85	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer;Active Hi CE;330ns Max Access Time	ITL
61	C8755A	MCS85	IO-57	Chip		2048Wx8 Bit EPROM with 2 Gen Purpose 8 Bit IO Ports	ITL
62	D8155-2	MCS85	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer;Active Lo CE;330ns Max Access Time	ITL
63	D8156	MCS85	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer Active Hi CE,400ns Max Access Time	ITL
64	D8156-2	MCS85	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer;Active Hi CE;330ns Max Access Time	ITL
65	D8355-2	MCS85	IO-57	Chip		2048x8 Bit ROM,16 I/O Lines for 8085A2,8049,8039 Syst;Cer Pkg	ITL
66	P8155-2	MCS85	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer;Active Lo CE;330ns Max Access Time	ITL
67	P8156-2	MCS85	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer;Active Hi CE;330ns Max Access Time	ITL
68	P8355-2	MCS85	IO-57	Chip		2048x8 Bit ROM,16 I/O Lines for 8085A2,8049,8039 Syst;Plastic Pkg	ITL
69	C8185	MCS85	RAM	Chip	MNG	1024x8 Static RAM;For 8085A;18-Pin DIL Package	ITL
70	C8185-2	MCS85	RAM	Chip	MNG	1024x8 Static RAM;For 8085A-2;18-Pin DIL Package	ITL
71	D8185	MCS85	RAM	Chip	MNG	1024x8 Static RAM;For 8085A;18-Pin DIL Package	ITL
72	D8185-2	MCS85	RAM	Chip	MNG	1024x8 Static RAM;For 8085A-2;18-Pin DIL Package	ITL
73	P8185	MCS85	RAM	Chip	MNG	1024x8-Bit Static RAM;To Interface Directly To 8085A/8088	ITL
74	P8185-2	MCS85	RAM	Chip	MNG	1024x8 Static RAm; for,8085-2;18 Pin DIL	ITL
75	C8279	MCS85,48	IO-10	Chip	MNX	Programmable Keyboard/Display Interface	ITL
76	C8279-5	MCS85,48	IO-10	Chip	MNX	Programmable Keyboard/Display Interface	ITL
77	D8279	MCS85,48	IO-10	Chip	MNX	Programmable Keyboard/Display Interface	ITL
78	P8279	MCS85,48	IO-10	Chip	MNX	Programmable Keyboard/Display Interface	ITL
79	P8255A	MCS85,48	IO-30	Chip	MNX	Programmable Peripheral Interface;24 Programmable I/O Pins	ITL
80	C8355	MCS85,48	IO-57	Chip	MNX	2048x8 Bit ROM w/I/O;2 Gen Purpose 8 Bit I/O Parts	ITL
81	C8355-2	MCS85,48	IO-57	Chip	MNX	2048x8 Bit ROM w/I/O;2 Gen Purpose 8 Bit I/O Parts	ITL
82	C8755	MCS85,48	IO-57	Chip	MNX	2048x8 Bit EPROM With I/O;Internal Address Latch	ITL
83	C8755A-2	MCS85,48	IO-57	Chip	MNX	2048x8 Bit ROM w/I/O;Z Gen Purpose 8 Bit I/O Parts	ITL
84	D8155	MCS85,48	IO-57	Chip		256x8 Bit Static RAM W/IO Ports,Timer Active Lo CE,400ns Max Access Time	ITL
85	D8355	MCS85,48	IO-57	Chip	MNX	2048x8 Bit ROM With I/O;2 Gen Purpose 8 Bit I/O Parts;Cerdip Pkg	ITL
86	D8755A	MCS85,48	IO-57	Chip	MNX	2048x8 Bit ROM w/I/O;Z Gen Purpose 8 Bit I/O Parts	ITL
87	D8755A-2	MCS85,48	IO-57	Chip	MNX	2048x8 Bit ROM w/I/O;Z Gen Purpose 8 Bit I/O Parts	ITL
88	P8155	MCS85,48	IO-57	Chip	MNX	256x8 Bit Static RAM W/IO Ports,Timer Active Lo CE,400ns Max Access Time	ITL
89	P8355	MCS85,48	IO-57	Chip		2048x8 Bit ROM With I/O;2 Gen Purpose 8 Bit I/O Ports;Plastic Pkg	ITL
90	P8755A	MCS85,48	IO-57	Chip	MNX	2048x8 Bit ROM w/I/O;Z Gen Purpose 8 Bit I/O Parts	ITL
91	P8755A-2	MCS85,48	IO-57	Chip	MNX	2048x8 Bit ROM w/I/O;Z Gen Purpose 8 Bit I/O Parts	ITL
92	D8086-2	MCS86	uCT	Chip	MNG	16-Bit HMOS uProcessor;Mulitbus System Compatible Inter;Clock Rate 8.0MHz	ITL
93	SDK86	MCS86	COMP	MOD		16 Bit Single Board Microcomputer Kit,8086 CPU,KB,LED Display	ITL
94	C8086	MCS86	CPU	Chip	MNG	16-Bit HMOS uProcessor;Multibus System Compatible Inter;Clock Rate 5.0MHz	ITL
95	C8086-2	MCS86	CPU	Chip	MNG	16-Bit HMOS uProcessor;Multibus System Compatible Inter;Clock Rate 8.0MHz	ITL
96	C8086-4	MCS86	CPU	Chip	MNG	16-Bit HMOS uProcessor;Multibus System Compatible Inter;Clock Rate 4.0MHz	ITL
97	D8086	MCS86	CPU	Chip	MNG	16 Bit Microprocessor,8/16 Bit Processing Capability,16 Bit Arith/Log Reg	ITL
98	D8086-4	MCS86	CPU	Chip	MNG	16 Bit Microprocessor,8/16 Bit Processing Capability,16 Bit Arith/Log Reg	ITL
99	P8086	MCS86	CPU	Chip	MNG	16-Bit HMOS uProcessor;Multibus System Compatible Inter;Clock Rate 5.0MHz	ITL
100	P8086-4	MCS86	CPU	Chip	MNG	16-Bit HMOS uProcessor;Multibus System Compatible Inter;Clock Rate 4.0MHz	ITL
101	SDK-C86	MCS86	DEV			Sys Design Kit-SW and Cable Interface to Intellec Development System	ITL
102	MDS-ICE86	MCS86	DEV	MOD		8086 CPU In-Ckt Emulator;Trace Capability;2 Breakpoint Registers	ITL
103	SBC957	MCS86	DEV	MODS		INTELLEC-iSBC86/12 Interface and Execution Package	ITL
104	C8288	MCS86	IO-02	Chip	BTX	Bus Controller for 8086 CPU	ITL
105	D8288	MCS86	IO-02	Chip	BTX	Bus Controller for 8086 CPU	ITL
106	P8288	MCS86	IO-02	Chip	BTX	Bus Controller for 8086 CPU	ITL
107	C8289	MCS86	IO-11	Chip	BTX	Bus Arbiter;Provides Multi-Master Sys Bus Protocol;Simple Inter w/8288	ITL
108	D8289	MCS86	IO-11	Chip	BTX	Bus Arbiter;Provides Multi-Master Sys Bus Protocol;Simple Inter w/8288	ITL
109	P8289	MCS86	IO-11	Chip	BTX	Bus Arbiter;Provides Multi-Master Sys Bus Protocol;Simple Inter w/8288	ITL
110	C8286	MCS86	IO-21	Chip	BTX	8-Bit Parallel Bidir Bus Driver;Non Inverting;3State Output	ITL

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	C8287	MCS86	IO-21	Chip	BTX	8-Bit Parallel Bidir Bus Driver;Inverting;3State Output	ITL
2	D8286	MCS86	IO-21	Chip	BTX	8-Bit Parallel Bidir Bus Driver;Non Inverting;3State Output	ITL
3	D8287	MCS86	IO-21	Chip	BTX	8-Bit Parallel Bidir Bus Driver;Inverting;3State Output	ITL
4	P8286	MCS86	IO-21	Chip	BTX	8 Bit Parallel Bidir Bus Driver,Non Inverting,3 State Output	ITL
5	P8287	MCS86	IO-21	Chip	BTX	8 Bit Parallel Bidir Bus Driver,Inverting,3 State Output	ITL
6	C8294	MCS86	IO-22	Chip		Data Encryption Unit;80 Byte/Sec Data Conversion Rate	ITL
7	D8294	MCS86	IO-22	Chip		Data Encryption Unit;80 Byte/Sec Data Conversion Rate	ITL
8	P8294	MCS86	IO-22	Chip		Data Encryption Unit;80 Byte/Sec Data Conversion Rate	ITL
9	C8284	MCS86	IO-32	Chip	BTX	Clock Generator and Driver for 8086 CPU Multibus Compatible	ITL
10	D8284	MCS86	IO-32	Chip	BTX	Clock Generator and Driver for 8086 CPU Multibus Compatible	ITL
11	P8284	MCS86	IO-32	Chip	BTX	Clock Generator and Driver for 8086 CPU,MULTIBUS Compatible	ITL
12	C8282	MCS86	IO-33	Chip	BTX	8-Bit Input/Output Port; Non Inverting; 3 State Output	ITL
13	C8283	MCS86	IO-33	Chip	BTX	8-Bit Input/Output Port;Inverting;3State Output	ITL
14	C8291	MCS86	IO-33	Chip		GBIP Talker/Listener Interface;8-Bit uProcessor to 488 Bus	ITL
15	C8292	MCS86	IO-33	Chip		GBIP Controller;Connects to 8291 to Implement 488 Bus	ITL
16	C8293	MCS86	IO-33	Chip		GBIP Controller;Connects to 8291 to Implement 488 Bus	ITL
17	D8282	MCS86	IO-33	Chip	BTX	8-Bit Input/Output Port; Non Inverting; 3 State Output	ITL
18	D8283	MCS86	IO-33	Chip	BTX	8-Bit Input/Output Port;Inverting 3State Output	ITL
19	D8291	MCS86	IO-33	Chip		GPIB Talker/Listener,Interfaces 8 Bit Microproc to 488 Bus	ITL
20	D8292	MCS86	IO-33	Chip		GPIB Controller:Connects to 8291 to Implement 488 Control	ITL
21	D8293	MCS86	IO-33	Chip		GBIP Controller;Connects to 8291 to Implement 488 Bus	ITL
22	P8282	MCS86	IO-33	Chip	BTX	8 Bit Input/Output Port,Non Inverting,3 State Output	ITL
23	P8283	MCS86	IO-33	Chip	BTX	8 Bit Input/Output Port,Inverting,3 State Output	ITL
24	P8291	MCS86	IO-33	Chip		GPIB Talker/Listener,Interfaces 8 Bit Microproc to 488 Bus	ITL
25	P8292	MCS86	IO-33	Chip		GPIB Controller:Connects to 8291 to Implement 488 Control	ITL
26	P8293	MCS86	IO-33	Chip		GBIP Controller;Connects to 8291 to Implement 488 Bus	ITL
27	C8089	MCS86,88	IO-03	Chip	MNG	8/16-Bit I/O Processor;Local or Remote;Intellegent DMA Func;40 Pin DIL	ITL
28	D8089	MCS86,88	IO-03	Chip	MNG	8/16-Bit I/O Processor;Local or Remote;Intelligent DMA Func;40-Pin DIL	ITL
29	P8089	MCS86,88	IO-03	Chip	MNG	8/16-Bit I/O Processor;Local or Remote;Intellegent DMA Func;40 Pin DIL	ITL
30	C8088	MCS88	CPU	Chip	MNG	8-Bit uProc;16-Bit Internal Arch;DMA to 1MByte;8086 IS;5M CL;40-Pin DIL	ITL
31	D8088	MCS88	CPU	Chip	MNG	8-Bit uProc;16-Bit Internal Arch;DMA to 1 Mbyte;8086 IS;5M CL;40-Pin DIL	ITL
32	P8088	MCS88	CPU	Chip	MNG	8-Bit uProc;16-Bit Internal Arch;DMA to 1MByte;8086 IS;5M CL;40-Pin DIL	ITL
33	iSBC86/12	SBC80	COMP	MOD	MXX	16 Bit Single Board Computer;Uses 8086 CPU,6.75x12 inch PCB	ITL
34	SBC80/04	SBC80	COMP	MOD	MNG	Single Board Microcomputer;8085 CPU,256 Bytes RAM,2k/4k Byte EPROM	ITL
35	SBC80/05	SBC80	COMP	MOD	MNG	Single Board Microcomputer;8085 CPU,512 Bytes RAM,2k/4k Byte EPROM	ITL
36	SBC80/10	SBC80	COMP	MOD	MNG	Single Board Microcomputer;8080A CPU,1k Byte RAM,4k Byte EPROM	ITL
37	SBC80/10A	SBC80	COMP	MOD	MNG	Single Board Microcomputer;8080A CPU,1k Byte RAM,Up to 8k Byte EPROM	ITL
38	SBC80/20	SBC80	COMP	MOD	MNG	Complete Computer Syst On A Card:Includes CPU,Clock,RAM,48I/O Lines,USART	ITL
39	SBC80/20-4	SBC80	COMP	MOD	MNG	Single Board Microcomputer;8080A CPU,4k Byte RAM,8/4k Byte EPROM	ITL
40	SBC80/30	SBC80	COMP	MOD		Single Board Microcomputer,8080A CPU,16k Byte RAM,8k Byte ROM	ITL
41	SYSTEM80/10	SBC80	COMP	UNIT		Fully Packaged Microcomputer Using SBC80/10 Single Board Computer	ITL
42	SYSTEM80/20	SBC80	COMP	UNIT		Fully Packaged Microcomputer Using SBC80/20 Single Board Computer	ITL
43	SBC905	SBC80	DEV	MOD		Universal Prototype Board;Capacity for 95 Sockets	ITL
44	SBC80P05	SBC80	DEV	MODS		Prototype Pkg to Evaluate SBC80/05 Single Board Computer	ITL
45	SBC80P10	SBC80	DEV	MODS		Prototype Pkg To Evaluate SBC 80/10 Single Board Computer	ITL
46	SBC80P20	SBC80	DEV	MODS		Prototype Pkg To Evaluate SBC 80/20 Single Board Computer	ITL
47	SBC80P	SBC80	DEV	MODS		Prototype Pkg To Evaluate SBC80/10 Single Board Computer	ITL
48	SBC501	SBC80	IO-03	MOD		Direct Memory Access Controller;Block Transfer To 1M Words/Sec	ITL
49	SBC530	SBC80	IO-04	UNIT		Teletypewriter Adapter: Used W/SBC 80/20;RS232C To 20mA Loop Intf	ITL
50	SBC201	SBC80	IO-07	MOD		Diskette Controller;Microprogrammed;Complete CRC Data Checking	ITL
51	SBC202	SBC80	IO-07	MOD		Diskette Controller;Microprogrammed;Controls 4 Drives	ITL
52	iSBC544	SBC80	IO-20	MOD		Intelligent Communications Controller:On Board 8085A CPU	ITL
53	SBC517	SBC80	IO-30	MOD		Combination I/O Expansion Board;48 Progm I/O Lines;1ms Int Timer	ITL
54	SBC519	SBC80	IO-30	MOD		Programmable I/O Expansion Board;72 Progm I/O Lines	ITL
55	SBC508	SBC80	IO-33	MOD		I/O Expansion Board;Four 8 Bit Input;8 Bit Output Ports;0-55°C	ITL
56	SBC724	SBC80	IO-40	MOD		Analog Output Board;4 Independent 12 Bit DACs,Bi/Unipolar	ITL
57	SBC711	SBC80	IO-41	MOD		Analog Input Board;12 Bit ADC;8/16 Input Channels;Progm Gain	ITL
58	SBC732	SBC80	IO-42	MOD		Combination Analog I/O Board;In 8/16 Channels;Output 2 Channels	ITL
59	SBC104	SBC80	IO-57	MOD		4k Byte Combination Mem and I/O Board;48 Progm I/O Lines	ITL
60	SBC108	SBC80	IO-57	MOD		8k Byte Combination Mem and I/O Board;48 Progm I/O Lines	ITL
61	SBC116	SBC80	IO-57	MOD		16k Byte Combination Mem and I/O Board;48 Progm I/O Lines	ITL
62	SBC310	SBC80	IO-90	MOD		High Speed Mathematics Unit;Fixed And Floating Arith Functions	ITL
63	SBC901	SBC80	IO-92	MOD		Input Line Terminator in Quad Package	ITL
64	SBC902	SBC80	IO-92	MOD		1kΩ Pull up Input Line Terminators in Quad Pkg	ITL
65	SBC211	SBC80	PE-02	UNIT		Diskette Hardware System;Single Drive;Transfer Rate 250k Bit/Sec	ITL
66	SBC212	SBC80	PE-02	UNIT		Diskette Hardware System;Dual Drive;Storage/Diskette 256k Byte	ITL
67	SBC630	SBC80	PE-60	UNIT		Power Supply Unit;Vo ±5V,±12V,26.5V	ITL
68	SBC635	SBC80	PE-60	UNIT		Power Supply Unit;Heavy Duty;Vo ±5V,±12V	ITL
69	SBC416	SBC80	PROM	MOD		16k Byte PROM Expansion Board;0-55°C	ITL
70	SBC016	SBC80	RAM	MOD		16k Byte RAM Memory Board;Read Cycle 735ns max;0-55°C	ITL
71	SBC032	SBC80	RAM	MOD		32k Byte Dynamic RAM Mem Board;For SBC80 Mem Expansion	ITL
72	SBC048	SBC80	RAM	MOD		8BC 80 Mem Expansion Board;48 Byte Dynamic RAM Memory	ITL
73	SBC064	SBC80	RAM	MOD		8BC 80 Mem Expansion Board;64 Byte Dynamic RAM Memory	ITL
74	SBC094	SBC80	RAM	MOD	MCX	4k Static CMOS RAM,Power Fail Ckt;On Board Battery	ITL
75	C3001,2	3000	CPU	ChS	BTD	Microprogram Control Unit And Central Processing Element,Ceramic Pkg	ITL
76	D3001,2	3000	CPU	ChS	BTD	Microprogram Control Unit And Central Processing Element,Cer DIP Pkg	ITL
77	MC3001,2	3000	CPU	ChS	BTD	Microprogram Control Unit And Central Processing Element,Military Temp	ITL
78	MD3001,2	3000	CPU	ChS	BTD	Microprogram Control Unit and Central Processing Element;-55 to 125°C	ITL
79	MDS-ICE30	3000	IO-01	MOD		3001 Microprogram Control Unit Includes Hardware and Software	ITL
80	C3214	3000	IO-02	Chip	BTD	Interrupt Control Unit,Multi-Level Interrupt Capability,Ceramic Pkg	ITL
81	D3214	3000	IO-02	Chip	BTD	Interrupt Control Unit,Multi-Level Interrupt Capability,Cer Dip Pkg	ITL
82	MD3214	3000	IO-02	Chip	BTD	Interrupt Control Unit,Multi-Level Interrupt Cap,Cer Dip Pkg,Mil Temp	ITL
83	P3214	3000	IO-02	Chip	BTD	Interrupt Control Unit,Multi-Level Interrupt Capability,Plastic Pkg	ITL
84	D3212	3000	IO-33	Chip	BTD	Multi Mode Latch Buffer,8 Bit Latch,Cer Dip Pkg	ITL
85	MD3212	3000	IO-33	Chip	BTD	Multi Mode Latch Buffer,8 Bit Latch,Cer Dip Pkg,Military Temp	ITL
86	P3212	3000	IO-33	Chip	BTD	Multi Mode Latch Buffer,8 Bit Latch,Plastic Pkg	ITL
87	C3003	3000	IO-90	Chip	BTD	Look-Ahead Carry Generator,Ceramic Pkg	ITL
88	D3003	3000	IO-90	Chip	BTD	Look-Ahead Carry Generator,Cer Dip Pkg	ITL
89	MC3003	3000	IO-90	Chip	BTD	Look-Ahead Carry Generator,Ceramic Pkg	ITL
90	MD3003	3000	IO-90	Chip	BTD	Look Ahead Carry Generator;Mil Screening Level B,C	ITL
91	D3216	3000,MCS40	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver/Receiver,Cer Dip Pkg	ITL
92	MD3216	3000,MCS40	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver/Receiver,Cer Dip Pkg,Military Temp	ITL
93	P3216	3000,MCS40	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver/Receiver,Plastic Pkg	ITL
94	B8035L	8048	uCT	Chip	MNG	8-Bit uComputer;CPU Only w/Power Down;Cycle Time 2.5 us;40 Pin	ITL
95	B8039-6	8048	uCT	Chip	MNG	8-Bit uComputer; External ROM or EPROM;Cycle Time 1.36us; 40 Pin	ITL
96	C8035L	8048	uCT	Chip	MNG	8-Bit uComputer;CPU Only w/Power Down;Cycle Time 2.5us;40PinITL	ITL
97	D8035L	8048	uCT	Chip	MNG	8-Bit uComputer;CPU Only w/Power Down;Cycle Time 2.5us;40 Pin	ITL
98	P8035L	8048	uCT	Chip	MNG	8-Bit uComputer;CPU Only w/Power Down;Cycle Time 2.5us;40 Pin	ITL
99	B8080A	8080	uCT	Chip	MNG	8-Bit uProcessor; 64k Bytes Memory; Cycle Time 2.0us;40 Pin	ITL
100	B8080A-1	8080	uCT	Chip	MNG	8-Bit uProcessor; 64k Bytes Memory; Cycle Time 1.3us;40 Pin	ITL
101	B8080A-2	8080	uCT	Chip	MNG	8-Bit uProcessor; 64k Bytes Memory; Cycle Time 1.5us; 40 Pin	ITL
102	I8801	8224/8080A	IO-32			Clock Generator Crystal for 8224/8008A;18.432MHz for 1.95us 8080A Cycle	ITL
103	B8748-6	8748	uCT	Chip	MNG	8-Bit uComputer;User Programmable EPROM;Cycle Time 2.5us;40 Pin	ITL
104	C8748-6	8748	uCT	Chip	MNG	8-Bit uComputer;User Programmable EPROM;Cycle Time 2.5us;40 Pin	ITL
105	C8748-8	8748	uCT	Chip	MNG	8-Bit uComputer;User Programmable EPROM;Cycle Time 4.1us;40 Pin	ITL
106	D8748-6	8748	uCT	Chip	MNG	8-Bit uComputer;User Program- mable EPROM; Cycle Time 2.5us; 40 Pin	ITL
107	D8748-8	8748	uCT	Chip	MNG	8-Bit uComputer;User Programmable EPROM;Cycle Time 4.1us;40 Pin	ITL
108	P8748-6	8748	uCT	Chip	MNG	8-Bit uComputer;User Programmable EPROM;Cycle Time 2.5us;40 Pin	ITL
109	P8748-8	8748	uCT	Chip	MNG	8-Bit uComputer;User Programmable EPROM;Cycle Time 4.1us;40 Pin	ITL
110♦	M68MM09	M6800	RAM	MOD	MCX	4k Static RAM Module:1.5 or 2.0MHz Oper;Batt Backup;EXORbus Compatible	M

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1#	MCH-01	MTX	IO-09	Chip	MNX	Upper/Lower Case/Graphics Character Generator,128 Char Set	MAT
2#	MTX-A1	MTX	IO-09	Chip		Alphanumeric (Dot) Display/Keyboard Controller;Programmable	MAT
3#	MTX-B1	MTX	IO-09	Chip		Alphanumeric Display/KB Controller for 7 to 16 Seg Display,Progm	MAT
4#	ALT256	MTX	IO-09	MOD		Graphic Display Interface;S100 Bus,Resolution 256x256 Dot Raster,Acc3.4us	MAT
5#	ALT512	MTX	IO-09	MOD		TV Graphic Display CRT Controller:512x256 Resol;S100 Bus Compat	MAT
6#	ALT2480	MTX	IO-09	MOD		Alphanumeric Display Interface Bet S100 Bus Microcomp and TV Monitor	MAT
7#	EXO512	MTX	IO-09	MOD		TV Graphics CRT Controller:256x256 Raster;S100 Bus Compatible	MAT
8#	EXO2480	MTX	IO-09	MOD		TV Alphanumeric CRT Controller;24x80 Video RAM,Exorciser Bus Compat	MAT
9#	FG-01	MTX	IO-09	MOD		Frame Grabber Board:Used W/RGB256;SBC80 Compat	MAT
10#	MDC512	MTX	IO-09	MOD		TV Graphics CRT Controller:Variable Resolution;PDP-11 Bus Compat	MAT
11#	MDC2480	MTX	IO-09	MOD		TV Alphanumeric CRT Controller;24x80 Video RAM,PDP-11 Bus Compat	MAT
12#	MLSI512	MTX	IO-09	MOD		TV Graphics CRT Controller:Variable Resolution;LSI-11 Bus Compat	MAT
13#	MLSI2480	MTX	IO-09	MOD		TV Alphanumeric CRT Controller;24x80 Video RAM,LSI-11 Bus Compat	MAT
14#	MMD256	MTX	IO-09	MOD		TV CRT Controller:256x256x1 Graphic Mod;Access Time 1.4us	MAT
15#	MMD2480	MTX	IO-09	MOD		TV CRT Controller:24x80 Display Field Video RAM 4kx8	MAT
16#	MSBC24/320	MTX	IO-09	MOD		Single Board 24x80 Alphanum and 320x24 Graphic Display Controller	MAT
17#	MSBC512	MTX	IO-09	MOD		TV Graphics CRT Controller:Variable Resolution;SBC80 Bus Compat	MAT
18#	MSBC2480	MTX	IO-09	MOD		TV Alphanumeric CRT Controller;24x80 Video RAM,SBC80 Bus Compat	MAT
19#	MSBC-PLL	MTX	IO-09	MOD		SBC -80 Plug in Phase Lock Loop Board;SBC80 Compatible	MAT
20#	MTX256-2	MTX	IO-09	MOD		TV CRT Controller;Graphic Display,256 x 256 Dot Raster	MAT
21#	MTX512	MTX	IO-09	MOD		TV CRT Controller;Variable Resolution Graphics,Compt W/LSI11,SBC80 Bus	MAT
22#	MTX816	MTX	IO-09	MOD		TV CRT Controller;8 x 16 Display Field Video RAM	MAT
23#	MTX1632	MTX	IO-09	MOD		TV CRT Controller;16 x 32 Display Field Video RAM	MAT
24#	MTX1632SL	MTX	IO-09	MOD		TV CRT Controller;16 x 32 Display Field Video RAM,Slave Lock Facility	MAT
25#	MTX1648/64SL	MTX	IO-09	MOD		TV CRT Controller;16x64 Display Field Video RAM Ext Synch	MAT
26#	MTX2064	MTX	IO-09	MOD		TV CRT Controller;20x64 Display Field Video RAM	MAT
27#	MTX2480	MTX	IO-09	MOD		TV CRT Controller:24x80 Display Field Video RAM 4kx9	MAT
28#	MTX-14SD	MTX	IO-09	MOD		Dual (2 Digit) 14 Segment Alphanum LED Display	MAT
29#	MTX-305	MTX	IO-09	MOD		5x7 LED Display	MAT
30#	MTX-A2	MTX	IO-09	MOD		16 Character Alphanum Display,5x7 LED,Single 5V Supply	MAT
31#	MTX-B2	MTX	IO-09	MOD		32 Character Alphanum Display,14 Seg LED,Single 5V Supply	MAT
32#	NSBC512	MTX	IO-09	MOD		TV Graphics CRT Controller:512x512 Graphics W/Vector Plot;SBC80 Bus	MAT
33#	PLL-01	MTX	IO-09	MOD		External Sync Phase Lock Loop Mod for VRAMs	MAT
34#	PV-1	MTX	IO-09	MOD		Progmmable Format Video RAM 8x(12,16,24,32,64) or 16x(16,24,32,48,64)	MAT
35#	RGB256	MTX	IO-09	MOD		Single Board 256x256x4 Color Controller;SBC80 Bus or Gen Purpose	MAT
36#	SG-01	MTX	IO-09	MOD		50/60 Hz TV Sync Generator,Add On for MTX1648/64SL	MAT
37#	SI-ABCD	MTX	IO-09	MOD		Serial Interface Adapter Board,Selectable Baud Rate	MAT
38#	STD256	MTX	IO-09	MOD		TV Graphics CRT Controller:256x256 Display,Prolog STD Bus Compat	MAT
39#	STD2480	MTX	IO-09	MOD		TV Alphanumeric CRT Controller;24x80 Video RAM,Prolog STD Bus Compat	MAT
40#	VEN-01	MTX	IO-09	MOD		Hi Speed 3 Bit,20MHz Gray Scale Video Encoder	MAT
41#	MCRT-9	MTX	PE-15	UNIT		9inch CRT Display W/P4 Phosphor,Also Available in Green Phosphor P39	MAT
42#	MCRT-14	MTX	PE-15	UNIT		14inch CRT Display W/P4 Phosphor,Also Available in Green Phosphor P39	MAT
43#	MCRT-CC19	MTX	PE-15	UNIT		19inch Color TV Monitor W/6MHz BW;RGB/NTSC/PAL/SECAM Convertibility	MAT
44▼#	FFD1		IO-07	MOD		Floppy Disk Contr/RAM Card;w/DM1883 DMA Controller;32k Bytes RAM;2 Ports	MATC
45▼#	RGB-ALPHA		IO-09	MOD		Display Contr;Color Alphanumeric;10/128 Char per Line w/60 Lines;16 Bit	MATC
46	MCTV-15		IO-09	UNIT		Operates as Normal Color TV Receiver;Video Input Mode;RGB Input Mode	MATC
47	FG-01/6	MTX	IO-09	MOD		6-Bit High Speed A/D Converter Card Range -2V to 0.0V	MATC
48	FG-01/8	MTX	IO-09	MOD		8-Bit High Speed A/D Converter Card Range -2V to 0.0V	MATC
49#	RGB-256/3	MTX	IO-09	MOD		4 Bit Single Card Color Grey Scale Imaging System	MATC
50#	RGB-256/4	MTX	IO-09	MOD		8 Bit Single Card Color Grey Scale Imaging System	MATC
51▼#	MEGA1	Z80,8080/85	RAM	MOD		128k Byte Mem Card;Compat w/Multibus;Programable 8/16-Bit Word Size	MATC
52▼#	ZBC80	Z80A	CPU	MOD		Processing Unit;Compat w/Multibus;Clk Rate 4.0MHz;16k/64 Bytes Dyn RAM	MATC
53#	MN1400	MN1400	uCT	Chip	MNG	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
54#	MN1402	MN1400	uCT	Chip	MNG	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
55#	MN1403	MN1400	uCT	Chip	MNX	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
56#	MN1432	MN1400	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
57#	MN1435	MN1400	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
58#	MN1450	MN1400	uCT	Chip	MCX	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
59#	MN1453	MN1400	uCT	Chip	MCX	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
60#	MN1454	MN1400	uCT	Chip	MCX	Single 4 Bit Microcomputer w/RAM-ROM;16-Pin DIP Plastic Pkg	MATJ
61#	MN1455	MN1400	uCT	Chip	MCX	Single 4 Bit Microcomputer w/RAM-ROM;40-Pin DIP Plastic Pkg	MATJ
62#	MN1404	MN1400	CPU	Chip	MNG	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
63#	MN1405	MN1400	CPU	Chip	MNG	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
64#	MN1430	MN1400	CPU	Chip	MPG	Single Chip 4 Bit Microcomputer W/RAM,ROM	MATJ
65#	MN1498	MN1400	DEV	Chip	MNG	Single Chip 4 Bit Microcomputer Evaluator W/RAM External Inst ROM	MATJ
66#	MN1499	MN1400	DEV	Chip	MNG	Single Chip 4 Bit Microcomputer Evaluator W/RAM External Inst ROM	MATJ
67#	MN1499A	MN1400	DEV	Chip	MNG	Single Chip 4 Bit Microcomputer Evaluator With 128x4Bit RAM	MATJ
68#	HS1400	MN1400	DEV	UNIT		Hardware Simulator With Debug Capability for MN1400 Series u Comps	MATJ
69#	MN1205A	MN1400	IO-09	Chip	MCX	Num Displ Dec/Drv;BIN to 4x8 Matrix;Io 13mA,PS5V;22 Pin Pkg	MATJ
70#	MN1205D	MN1400	IO-09	Chip	MCX	Num Displ Dec/Drv;Neg Logic;BCD to 2 Dig,7 Seg;Io 16mA,PS 5V; 28 Pin Pkg	MATJ
71#	MN1205E	MN1400	IO-09	Chip	MCX	Num Displ Dec/Drv;Pos Logic;BCD to 2 Dig,7 Seg;Io 16mA,PS 5V;28 Pin Pkg	MATJ
72#	MN1205F	MN1400	IO-09	Chip	MCX	Num Displ Dec/Drv;BIN to 4x6 Matrix;Io 16mA,PS 5V;18 Pin Pkg	MATJ
73#	MN1205G	MN1400	IO-09	Chip	MCX	Num Displ Dec/Drv;Neg Logic;BCD to 2 Dig,7 Seg;Io 16mA,PS 5V; 28 Pin Pkg	MATJ
74#	MN1205H	MN1400	IO-09	Chip	MCX	Num Displ Dec/Drv;Pos Logic;BCD to 1 Dig,14 Seg;Io 16mA,PS 5V;28 Pin Pkg	MATJ
75#	MN1205P	MN1400	IO-09	Chip	MCX	Num Displ Dec/Drv;Neg Logic;BCD to 2 Dig,7 Seg;Io 30mA,PS 5V;28 Pin Pkg	MATJ
76#	MN1205Q	MN1400	IO-09	Chip	MCX	Num Displ Dec/Drv;Pos Logic;BCD to 2 Dig,7 Seg;Io 30mA,PS 5V;28 Pin Pkg	MATJ
77#	MN1204	MN1400	IO-40	Chip	MNX	Quad D/A Converter:12 Bit Word, 6 Bit and two 4 Bit Words	MATJ
78#	MN1202	MN1400	IO-43	Chip	MCX	Quad 2 Line to 1 Line Multiplexer:Single 5V Supply, 18 Pin Pkg	MATJ
79#	MN1201	MN1400	IO-56	Chip	MCX	Dual 4 Bit Data Latches:Single 5V Supply, 18 Pin Plastic Pkg	MATJ
80#	MN1201A	MN1400	IO-56	Chip	MCX	Dual 4 Bit Data Latches:Single 5V Supply, 16 Pin Plastic Pkg	MATJ
81#	MN1002	MN1400	RAM	Chip	MNG	4096x1 Dynamic RAM;Access Time 200ns	MATJ
82#	MN1101	MN1400	RAM	Chip	MCG	128x9 Static RAM;Access Time 500ns	MATJ
83#	MN1542	MN1500	uCT	Chip	MNX	4 Bit;124 Instr;Instr Size 2k x 8;RAM 152 x 4;16 Level Subroutine Stk	MATJ
84#	MN1544	MN1500	uCT	Chip	MNX	4 Bit;124 Instr;Instr Size 4k x 8;RAM 256 x 4;16 Level Subroutine Stk	MATJ
85#	MN1562	MN1500	uCT	Chip	MNX	4 Bit;124 Instr;Instr Size 2k x 8;RAM 152 x 4;16 Level Subroutine Stk	MATJ
86#	MN1564	MN1500	uCT	Chip	MNX	4 Bit;124 Instr;Instr Size 4k x 8;RAM 256 x 4;16 Level Subroutine Stk	MATJ
87#	MN1599	MN1500	IO-33	Chip	MNX	4 Bit;124 Instr;Instr Size 8k x 8;RAM 256 x 4;16 Level Subroutine Stk	MATJ
88#	MN1651	PFL16A	CPU	Chip		Same as MN1650 But with Single 5V Supply	MATJ
89#	MN1611	PFL16A	IO-02	Chip		Same as MN1610 But with Single 5V Supply	MATJ
90#	MN1631	PFL16A	IO-02	Chip		Same as MN1630 But with Single 5V Supply	MATJ
91	MM100	JOLT	RAM	MOD		4k Static RAM;4096x8 RAM Memory Using Type 2111	MCA
92	CP110	SUPERJOLT	CPU	MOD		Uses JOLT Components;6502 CPU,Clock,28 Bidir I/O,1kx8 RAM,RS 232 IFs	MCA
93	MSC8004-Z80A	8080	COMP	MOD		8-Bit Single Board Computer w/8080 CPU;Multibus	MCSS
94	MSC8007-Z80A	8080	COMP	MOD		8-Bit Single Board Computer w/8080 CPU;Multibus	MCSS
95	P816	MCS80	DEV	MOD		8K/16K PROM Board For Intel SBC or Intellec System	MCT
96▼	MLSI-DLV11-FX	LSI11		MOD		A11 Features of DLV11-F plus RS422/23 Capability/Printer Busy Detection	MDB
97	MLSI-DSD-440	LSI11	COMP	MOD		Double Density Dial Drive Floppy Disk Subsystem (DMA)	MDB
98	MLSI-KPV11-A	LSI11	COMP	MOD		Power Fail/Line Time Clock Generator(LTC))	MDB
99	MLSI-KPV11-B	LSI11	COMP	MOD		Same as MLSI-KPV11-A Plus 120 Ohms Bus Terminator	MDB
100	MLSI-KPV11-C	LSI11	COMP	MOD		Same as MLSI-KPV11-A Plus 220 Ohms Bus Terminator	MDB
101	MLSI-RL01AK	LSI11	COMP	MOD		Add-On 5.2m Byte Disk Drive	MDB
102	MLSI-RLV11AK	LSI11	COMP	MOD		5.2m Byte Hard Disk Subsystem	MDB
103	MLSI-RXV21-BA	LSI11	COMP	MOD		Double Density Dual Drive Floppy Disk Subsystem (DMA)	MDB
104	MLSI-DA11BOI	LSI11	COMP	UNIT		Parallel DMA Interprocessor Link Between A PDP-11 and LSI-11	MDB
105	MLSI-KD11F	LSI11	CPU	MOD		16-Bit CPU,4k RAM;DMA,16Bit I/O;PDP 11/35,40Instr Set Compat;Made by DEC	MDB
106	MLSI-KD11HA	LSI11	CPU	MOD		16 Bit LSI11/2 CPU	MDB
107	MLSI-KD11HB	LSI11	CPU	MODS		16 Bit LSI11/2 CPU,Plus 8k x 16 RAM	MDB
108	MLSI-KD11HC	LSI11	CPU	MODS		16 Bit LSI11/2 CPU,Plus 16k x 16 RAM	MDB
109	MLSI-KD11HD	LSI11	CPU	MODS		16 Bit LSI11/2 CPU,Plus 32k x 16 RAM	MDB
110	MLSI-11/03-LH	LSI11	DEV	UNIT		Microcomp Dev Sys LSI-11/2 32KB RAM Mem Rack Mountable Chassis	MDB

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MLSI-11/23AA	LSI11	DEV	UNIT		Microcomp Dev Sys LSI-11/23 128KB RAM Mem Rack Mountable Chassis	MDB
2	MLSI-11/23AC	LSI11	DEV	UNIT		Microcomp Dev Sys LSI-11/23 256KB RAM Mem Rack Mountable Chassis	MDB
3	MLSI-SR-VXLLBA	LSI11	DEV	UNIT		Microcomp Dev Sys 5.2MB Removable Cartridge Disk Sys LSI-11/2	MDB
4	MLSI-SR-VXSSBA	LSI11	DEV	UNIT		Microcomp Dev Sys DMA Controller IBM Floppy Disk Sys LSI-11/2	MDB
5	MLSI-SR-VXS23BA	LSI11	DEV	UNIT		Microcomp Dev Sys DMA Control ler Expansion Space 10 Dual or 5 Quad	MDB
6	MLSI-11B	LSI11	IO-03	MOD		General Purpose Direct Memory Interface Module,Address Decode Circ	MDB
7	MLSI-DRV11P	LSI11	IO-03	MOD		LSI-11 Bus Foundation Module;Address Decode Circuitry	MDB
8	MLSI-REV11A	LSI11	IO-03	MOD		Bootstrap Refresh/Terminator Option	MDB
9	MLSI-REV11C	LSI11	IO-03	MOD		Bootstrap Refresh Option	MDB
10	MLSI-CR11	LSI11	IO-06	MOD		Card Reader Controller,Parallel Interface	MDB
11	MLSI-PC11	LSI11	IO-06	MOD		Paper Tape Reader/Punch Controller,Parallel Interface	MDB
12	MLSI-LP11	LSI11	IO-08	MOD		Line Printer Controller,Parallel Interface	MDB
13	MLSI-XYV11	LSI11	IO-08	MOD		Incremental Plotter Interface;Includes Differential Drivers	MDB
14	MLSI-IBV11	LSI11	IO-11	MOD		IEEE/488 Bus Interface;Selectable Address and Interrupt VECTOR;5.0 Vdc	MDB
15	MLSI-DLV11	LSI11	IO-20	MOD		Asynchronous Serial Line Interface,Selectable Baud Rate	MDB
16	MLSI-DLV11E	LSI11	IO-20	MOD		Asynchronous Serial Line Interface with Modern Control	MDB
17	MLSI-DLV11J	LSI11	IO-20	MOD		Asynchronous Serial Line Interface(4 Lines)	MDB
18	MLSI-DUV11	LSI11	IO-20	MOD		Synchronous Serial Line Interface,Selectable USART Parameters	MDB
19	MLSI-DRV11C	LSI11	IO-30	MOD		Parallel Line Interface Module;Multiple Interrupt Vector	MDB
20	MLSI-KW11P	LSI11	IO-32	MOD		Programmable Real Time Clock,4 Clock Rates Selectable	MDB
21	MLSI-1710	LSI11	IO-33	MOD		General Purpose Interface Module;Bus Interface,Address Decode Circ	MDB
22	MLSI-TEV	LSI11	IO-33	MOD		Bus Terminator Module;Provides Impedance Termination for LSI Bus	MDB
23	MLSI-DT-1761	LSI11	IO-42	MOD		16 Channel,12 Bit A/D Converter,Rates Up to 100k Characters Per Second	MDB
24	MLSI-MRV-000	LSI11	IO-55	MOD		PROM Mem Modules W/O Mem;For 2704,2708 UV PROMS	MDB
25	MLSI-MRV-001	LSI11	IO-55	MOD		PROM Mem Modules W/O Mem;For 1702 UV PROMS	MDB
26	MLSI-MRV-002	LSI11	IO-55	MOD		PROM Mem Modules W/O Mem;For 5623,5624 PROMS and ROMS	MDB
27	MLSI-MRV-003	LSI11	IO-55	MOD		PROM Mem Modules W/O Mem;For 3625 PROMS and ROMS	MDB
28	MLSI-KEV11	LSI11	IO-90	Chip		Fixed,Floating Point Instr Set Extension for LSI11/2;Made by DEC	MDB
29	MLSI-SMU	LSI11	IO-92	MOD		Monitoring Unit;Dual Module,Power On/Off,Failure Sequencing	MDB
30	MLSI-DSD-110	LSI11	PE-01	MOD		512k Bytes,Dual Floppy Disk System W/Interface	MDB
31	MLSI-LV11	LSI11	PE-10	UNIT		High Speed Electronics Plotter Controller	MDB
32	MDB120-5	LSI11	PE-60	Unit		Plus 5.0Vdc at 12A;110 Vac Input Power Supply	MDB
33	MDB250-5	LSI11	PE-60	Unit		Plus 5.0Vdc at 25A;110/220Vac Input Power Supply	MDB
34	MDB250-D-5/12	LSI11	PE-60	Unit		Dual Power Supply: 5.0Vdc at 12A and 12Vdc at 8A;110/220Vac Input	MDB
35	MDB250-T-5/12-15 LSI11		PE-60	Unit		Switching Power Supply;5.0Vdc at 12A;Plus 12Vdc at 3.5A,110/220VAC Input	MDB
36	MLSI-250-T-5/12S LSI11		PE-60	UNIT		Switching Power Supply SV,25A 12V, 6A;-12V, 1A	MDB
37	MLSI-MRV-004	LSI11	PROM	MOD		Memory Module For 2716 or 2758 PROMS W/On-Board PROM Programmer	MDB
38▼	MLSI-MRV-005	LSI11	PROM	MOD		PROM/RAM Module;for Commercial Ava 2716/2732 UV Erasable PROMs	MDB
39▼	MLSI-DR11B	LSI11	RAM	MOD		Direct Memory Access Module for LSI11 Computer	MDB
40	MLSI-MSV11-DB	LSI11	RAM	MOD		RAM Expansion Memory Module;8k x 16 RAM,Dual Height W/On-board Refresh	MDB
41	MLSI-MSV11-DC	LSI11	RAM	MOD		RAM Expansion Memory Module;16k x 16 RAM,Dual Height W/On-Board Refresh	MDB
42	MLSI-MSV11-DD	LSI11	RAM	MOD		RAM Expansion Memory Module;32k x 16 RAM,Dual Height W/On-board Refresh	MDB
43	MICRO1	MICRO1	CPU	MOD		CPU With ROM;15 Basic Microcommands	MID
44	2600	MICRO1	IO-20	MOD		Duplex Synch Modem Interface Control	MID
45	2610	MICRO1	IO-20	MOD		Asynchronous Communications Controller For 103/202 Data Sets	MID
46	2612	MICRO1	IO-20	MOD		Asynchronous Communications Controller For 8 Dup Sync Channels	MID
47	2612-1	MICRO1	IO-20	MOD		Asynchronous Communications Controller For 4 Duplex Channels	MID
48	2613	MICRO1	IO-20	MOD		Asynchronous Modem Interface For 8 Full Duplex Asynchronous Channels	MID
49	2613-1	MICRO1	IO-20	MOD		Asynchronous Modem Interface For 4 Full Duplex Channels	MID
50	2614	MICRO1	IO-20	MOD		Asynchronous Communications Controller For 8 Dup Asynchronous Channels	MID
51	2614-1	MICRO1	IO-20	MOD		Asynchronous Communications Controller For 4 Dup Channels	MID
52	2510	MICRO1	IO-33	MOD		Byte I/O Controller For 8 Bit Data Transfers	MID
53	2511	MICRO1	IO-33	MOD		Full Word I/O Interface;32 In/32 Out Lines	MID
54	2515	MICRO1	IO-44	MOD		Multiplexer For 4 I/O Devices Via DMA	MID
55	9000	MICRO1	PE-02	UNIT		Disk System;Moving Head Disc Drive,800k Byte/S Transf Rate;Controller	MID
56	2930	MICRO1	PE-04	UNIT		Magnetic Tape System;Controller	MID
57	6000	MICRO1	PE-04	UNIT		Magnetic Tape System;9 Track,Dual Gap Head;Controller	MID
58	0364	MICRO1	PE-10	UNIT		Line Printer;165 lpm;Parallel 5 x 7 Dot Matrix;64 Character Set	MID
59	2733	MICRO1	PE-24	UNIT		Line Printer;132 Column;64 Character Set;300lpm,12 Ch VFU,Controller	MID
60	2734	MICRO1	PE-24	UNIT		Line Printer;132 Column;96 Character Set;200lpm;12 Ch VFU,Controller	MID
61	2720	MICRO1	PE-40	UNIT		Card Reader;Input Controller,80 Column Cards,1000 Cards Hopper Stacker	MID
62	2720-1	MICRO1	PE-40	UNIT		Mark Sense Card Reader;Controller,1000 Card Hopper/Stacker	MID
63	2710	MICRO1	PE-42	UNIT		Paper Tape System;I/O Controller,8 Ch Paper Tape Reader/Punch	MID
64	2710-1	MICRO1	PE-42	UNIT		Paper Tape System;Same As 2710 Except Rolled Paper	MID
65	2711	MICRO1	PE-42	UNIT		Paper Tape Reader System;I/O Controller And 8 Ch Paper Tape Reader	MID
66	2712	MICRO1	PE-42	UNIT		Paper Tape Punch System;75 Cps;8 Ch Paper Punch,I/O Cont	MID
67	JANM38510/40001BQC 6800		CPU	Chip	MNG	8 Bit Microprocessor,Freq of Operation 0.1 to 1MHz;Same Inst Set as 6800	MIL
68	JANM38510/40001CQC 6800		CPU	Chip	MNG	8 Bit Microprocessor,Freq of Operation 0.1 to 1MHz;Same Inst Set as 6800	MIL
69	JANM38510/42001BQB 8080		CPU	Chip	MNG	8 Bit Microprocessor,Freq of Operation 0.5 to 2MHz;Same Inst Set as 8080A	MIL
70	JANM38510/42001CQB 8080		CPU	Chip	MNG	8 Bit Microprocessor,Freq of Operation 0.5 to 2MHz;Same Inst Set AS 8080A	MIL
71	MM16P	IMP16	RAM	MOD		8kx16 RAM Core Mem;Expand To 64k,Address 13 Bits,Access Time 350ns,W/Nat	MIM
72	MM1103	LSI11	RAM	MOD		8kx16 RAM Core Mem;Expand To 32k,Address 13 Bits,Access Time 400ns,W/DEC	MIM
73	MM1103/16	LSI11	RAM	MOD		16kx16 RAM Core Mem;Expand to 32k;Address 14 Bits;Access Time 400ns;W/DEC	MIM
74	MM8080	MCS80	RAM	MOD		8kx8 RAM Core Mem;Expand To 64k,Address 13 Bits,Access Time 350ns,W/Intel	MIM
75	MM8080A	MCS80	RAM	MOD		8kx8 RAM Core Mem;Expand To 64k,Address 13 Bits,Access Time 350ns,W/Intel	MIM
76	MM8080AL	MCS80	RAM	MOD		8kx8 RAM Core Mem;Expand to 64k;Address 13Bits;Access Time 350ns;W/Intel	MIM
77	MM6800	M6800	RAM	MOD		8kx8 RAM Core Mem;Expand To 64k,Address 13 Bits,Access Time 350ns,W/Mot	MIM
78	MMS100	PCS-80	RAM	MOD		8kx8 RAM Core Mem;Expand to 64k;Address 13 Bits;Access Time 350ns;W/IMS	MIM
79	MD68SC02AC	MC6800	CPU	Chip	MCX	On Chip Clock;Standby Pwr 10uW;16 Bit Memory Addr;40 Pin Ceramic Dip	MITC
80	MD68SC02AD	MC6800	CPU	Chip	MCX	On Chip Clock;Standby Pwr 10uW;16 Bit Memory Addr;40 Pin Side Braised Dip	MITC
81	MD68SC02AE	MC6800	CPU	Chip	MCX	On Chip Clock;Standby Pwr 10uW;16 Bit Memory Addr;40 Pin Plastic Dip	MITC
82▼#	M5L8251AP		IO-20	Chip	MNG	Programmable Communication Interface;Univer USART	MITJ
83#	PCA0804G01	MELCS 8/2	uCT	MOD		Enables 8-Color 64 x 64 Dot Matrix Color Display on TV Screen	MITJ
84#	PCA0804G02	MELCS 8/2	uCT	MOD		Consists of PCA0804G01,1 M5L2708k EPROM and Keyboard	MITJ
85#	PCA0401	MELCS4	uCT	MOD		Identical to M58840-XXXP w/Addr Out and Data In for Ext Connect to EPROMS	MITJ
86#	PCA0801	MELCS8/2	COMP	MOD		8 Bit Single Board Computer,Uses M58710S CPU,RAM 256,ROM 2k	MITJ
87#	MELCS8/2	MELCS8/2	COMP	MODS		8 Bit Microcomputer:Card Family Using M58710S CPU	MITJ
88#	PCA0802	MELCS8/2	IO-57	MOD		Memory/IO Expansion Board:Expansion for PCA0801,RAM 1k,ROM 4k	MITJ
89#	PCA0803	MELCS8/2	IO-92	MOD		Program Checker:Conservative Checker for PCA0801,PCA0802	MITJ
90#	PCA8501G01	MELPS 85/2	uCT	MOD		Uses M5L2114LP NMOS RAM;Excluding Batt Backup ct and Wait Signal Gen Ct	MITJ
91#	PCA8501G02	MELPS 85/2	uCT	MOD		Uses M58981S CMOS RAM;Including Batt Backup ct and Wait Signal Gen Ct	MITJ
92#	MELPS8	MELPS8	COMP	UNIT		8 Bit Microcomputer:Chip Family Using M58710S CPU	MITJ
93#	M58710S	MELPS8	CPU	Chip	MNG	8 Bit Microprocessor,Alternative Designation 8080A	MITJ
94#	M54551K	MELPS8	IO-02	Chip	BTD	System Controller and Bus Driver,Alternate Designation 8228	MITJ
95▼#	M5L8257P	MELPS8	IO-03	Chip	MNG	Programmable DMA Controller;4 Channel;Chan Masking Function	MITJ
96#	M58609-04S	MELPS8	IO-10	Chip	MPX	Keyboard Encoder,JIS Code Standard Product	MITJ
97#	M58609-XXS	MELPS8	IO-10	Chip	MPX	Keyboard Encoder,2 Key Rollover/N Key Lockout Operation	MITJ
98#	M58620-001S	MELPS8	IO-10	Chip	MPX	Keyboard Encoder,JIS Code Standard Product	MITJ
99#	M58620-XXXS	MELPS8	IO-10	Chip	MPX	Keyboard Encoder,2 Key Rollover,All Codes Stored in 3640 Bit ROM	MITJ
100#	M58740P	MELPS8	IO-30	Chip	MNG	Programmable Peripheral Interface,Alternative Designation 8255,Plastic Pk	MITJ
101#	M58740S	MELPS8	IO-30	Chip	MNG	Programmable Peripheral Interface,Alternative Designation 8255,Cer Pkg	MITJ
102#	M54550P	MELPS8	IO-32	Chip	BTD	Clock Generator and Driver,Alternate Designation 8224	MITJ
103#	M54552P	MELPS8	IO-33	Chip	BTD	8 Bit Input/Output Port,Alternative Designation 8212	MITJ
104#	M58730-001S	MELPS8	ROM	Chip	MNG	1024x8 Bit Static Mask Progm ROM,Contains Integer Arith Subroutine	MITJ

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1#	M58730-XXXS	MELPS8	ROM	Chip	MNG	1024x8 Bit Static Mask Progm ROM,Alternative Designation 8308	MITJ
2#	M58731-001S	MELPS8	ROM	Chip	MNG	2048x8 Bit Static Mask Progm ROM,Contains MELPS8 Monitor BOM-B	MITJ
3#	M58731-XXXP	MELPS8	ROM	Chip	MNG	2048x8 Bit Static Mask Progm ROM,Alternative Desig 8316A,Plastic Pkg	MITJ
4#	M58731-XXXS	MELPS8	ROM	Chip	MNG	2048x8 Bit Static Mask Progm ROM,Alternative Desig 8316A,Cer Pkg	MITJ
5▼#	M5L8255AP	M5L8085A	IO-30	Chip	MNG	Programmable Peripheral Interface;24 Prog I/O Pins	MITJ
6▼#	M5L8255AP-5	M5L8085A	IO-30	Chip	MNG	Programmable Peripheral Interface;24 Prog I/O Pins	MITJ
7#	M58494-XXXP	M58494	CPU	Chip	MCX	Mask ROM and RAM;4 Bit ALU;C1k Gen;I/O Ports;Interface for uP Sys etc.	MITJ
8#	M58840-XXXP	M58840	CPU	Chip	MPX	8 Bit A/D Conv;15 Bit Analog Input Port;1-Level Interrupt Function	MITJ
9#	M58842S	M58840	DEV	Chip	MPX	Equivalent to M58840-XXXP w/o Mask ROM;MELPS 4 System Evaluation Device	MITJ
10#	M5L8080AP	8080	CPU	Chip	MNG	No I/O Ports;256ea;Multilevel Interrupt;DMA Oper;Outputs TR Compat;Plas	MITJ
11#	M5L8080AS	8080	CPU	Chip	MNG	No I/O Ports;256ea;Multilevel Interrupt;DMA Oper;Outputs TR Compat;CER	MITJ
12#	M5L8228P	8080	IO-11	Chip	BTD	Bidirectional Bus Driver;Status Signal;User Select 1 Level Interrupt Vect	MITJ
13#	M5L8224P	8080	IO-32	Chip	BTD	Clock Generator for M5L 8080P,S CPU;16 Pin Plastic Pkg	MITJ
14#	M5L8085AP-20	8085	CPU	Chip	MNG	SW Compat w/M5L 8080A;Clk Gen (w/external Xtal or RC Ct);Built-in Sys Con	MITJ
15	2901AFM#1	2900	CPU	Chip	BTD	4 Bit Slice;RAM,ALU,Decoding,Mux,Flat-Pack,-55 to 125°C	MMI
16	2901AJC	2900	CPU	Chip	BTD	4 Bit Slice;RAM,ALU,Decoding,Mux,Ceramic Dip,0 to 70°C	MMI
17	2901AJM	2900	CPU	Chip	BTD	4 Bit Slice;RAM,ALU,Decoding,Mux,Ceramic Dip,-55 to 125°C	MMI
18	2901ANC	2900	CPU	Chip	BTD	4 Bit Slice;RAM,ALU,Decoding,Mux,Plastic Dip,0 to 70°C	MMI
19	2909FM	2900	IO-01	Chip		Microprogram Sequencer;4 Bit Slice Cascadable.Flat Pack,-55 to 125°C	MMI
20	2909JC	2900	IO-01	Chip		Microprogram Sequencer;4 Bit Slice Cascadable.Ceramic Dip,0 to 70°C	MMI
21	2909JM	2900	IO-01	Chip		Microprogram Sequencer;4 Bit Slice Cascadable.Ceramic Dip,-55 to 125°C	MMI
22	2909NC	2900	IO-01	Chip		Microprogram Sequencer;4 Bit Slice Cascadable.Plastic Dip,0 to 70°C	MMI
23	2911JC	2900	IO-01	Chip		Microprogram Sequencer;4 Bit Slice Cascadable.Ceramic Dip,0 to 70°C	MMI
24	2911JM	2900	IO-01	Chip		Microprogram Sequencer;4 Bit Slice Cascadable.Ceramic Dip,-55 to 125°C	MMI
25	2911NC	2900	IO-01	Chip		Microprogram Sequencer;4 Bit Slice Cascadable.Plastic Dip,0 to 70°C	MMI
26	29LS18FM	2900	IO-55	Chip	BTD	Low Power Schottky Version of 2918FM	MMI
27	29LS18JC	2900	IO-55	Chip	BTD	Low Power Schottky Version of 2918JC	MMI
28	29LS18JM	2900	IO-55	Chip	BTD	Low Power Schottky Version of 2918JM	MMI
29	29LS18NC	2900	IO-55	Chip	BTD	Low Power Schottky Version of 2918NC	MMI
30	MMI5701	5701	uCT	Chip	BTD	4 Bit Slice;Expandable Bipolar Microcontroller -55 To 125°C	MMI
31	MMI57110D	5701	IO-01	Chip		Microprogram Controller	MMI
32	MMI5051/5052J	5701	IO-09	ChS	BTX	2 Chip Set Char Gen;64 ASCII Char;5x7 Matrix;Row Scan;-55 to 125°C	MMI
33	MMI57LS315J	5701	IO-55	Chip	BTD	Octal Register With I/O;-55 to 125°C;Ceramic Pkg	MMI
34	MMI57S374J	5701	IO-55	Chip	BTD	Octal Register with 32mA Sink;Non-Inverting Tri-State Outputs;-55to125°C	MMI
35	MMI57S376J	5701	IO-55	Chip	BTD	Octal Register with Inverting Tri-State Outputs;-55 to 125°C	MMI
36	MMI57S378J	5701	IO-55	Chip	BTD	Octal Register with Inverting and 32mA Sink Tri-State Outputs;-55to125°C	MMI
37	MMI57401J	5701	IO-55	Chip	BTD	64x4 FIFO Mem;Synchronous/Asynchronous;10MHz Shift Rate;-55 to 125°C	MMI
38	MMI57S373J	5701	IO-56	Chip	BTD	Octal Latch with 32mA Sink;Non-Inverting Tri-State Outputs;-55 to 125°C	MMI
39	MMI57S380J	5701	IO-56	Chip	BTD	Octal Latch with Inverting Tri-State Outputs;-55 to 125°C	MMI
40	MMI57S382J	5701	IO-56	Chip	BTD	Octal Latch with Inverting and 32mA Sink Tri-State Outputs;-55 to 125°C	MMI
41	MMI57558-1D	5701	IO-90	Chip	BTD	8x8 Multiplier;Signed,Unsigned or Mixed Mult,Speed 135ns max	MMI
42	MMI57558-1F	5701	IO-90	Chip	BTD	8x8 Multiplier;Signed,Unsigned or Mixed Mult,42 Pin Flat Pack	MMI
43	MMI57558D	5701	IO-90	Chip	BTD	8x8 Multiplier;Signed,Unsigned,or Mixed Mult;-55 to 125°C	MMI
44	MMI57558F	5701	IO-90	Chip	BTD	8x8 Multiplier;Signed,Unsigned or Mixed Mult,42 Pin Flat Pack	MMI
45	MMI5386-1D	5701	PROM	Chip	BTD	1024x8 PROM;Access Time 125ns;Open Collector;-55 to 125°C;22 Pin Ceramic	MMI
46	MMI5386-1J	5701	PROM	Chip	BTD	1024x8 PROM;Access Time 125ns;Open Collector;-55 to 125°C;22 Pin Cerdip	MMI
47	MMI5387-1D	5701	PROM	Chip	BTD	1024x8 PROM;Access Time 125ns;Tri-State;-55 to 125°C;22 Pin Ceramic	MMI
48	MMI5387-1J	5701	PROM	Chip	BTD	1024x8 PROM;Access Time 125ns;Tri-State;-55 to 125°C;22 Pin Cerdip	MMI
49	MMI5289-2J	5701	ROM	Chip	BTD	1024x8 ROM;Improved Version of MMI5289-1J;Access Time 75ns	MMI
50	MMI6701	6701	uCT	Chip	BTD	4 Bit Slice;Expandable Bipolar Microcontroller 0 To 75°C	MMI
51	MMI67110D	6701	IO-01	Chip		Microprogram Controller	MMI
52	MMI6051/6052J	6701	IO-09	ChS	BTX	2 Chip Set Char Gen;64 ASCII Char;5x7 Matrix;Row Scan;0 to 70°C	MMI
53	MMI67LS315J	6701	IO-55	Chip	BTD	Octal Register With I/O;0 to 70°C;Ceramic Pkg	MMI
54	MMI67LS315N	6701	IO-55	Chip	BTD	Octal Register With I/O;0 to 70°C;Plastic Pkg	MMI
55	MMI67S374J	6701	IO-55	Chip	BTD	Octal Register W/Non-Inverting 32mA Tri-State Out;0 to 70°C;Ceramic Pkg	MMI
56	MMI67S374N	6701	IO-55	Chip	BTD	Octal Register W/Non-Inverting 32mA Tri-State Out;0 to 70°C;Plastic Pkg	MMI
57	MMI67S376J	6701	IO-55	Chip	BTD	Octal Register W/Inverting Tri-State Out;0 to 70°C;Ceramic Pkg	MMI
58	MMI67S376N	6701	IO-55	Chip	BTD	Octal Register W/Inverting Tri-State Out;0 to 70°C;Plastic Pkg	MMI
59	MMI67S378J	6701	IO-55	Chip	BTD	Octal Register W/Inverting 32mA Tri-State Out;0 to 70°C;Ceramic Pkg	MMI
60	MMI67S378N	6701	IO-55	Chip	BTD	Octal Register W/Inverting 32mA Tri-State Out;0 to 70°C;Plastic Pkg	MMI
61	MMI67S380J	6701	IO-55	Chip	BTD	Octal Latch W/Inverting Tri-State Out;0 to 70°C;Ceramic Pkg	MMI
62	MMI67S380N	6701	IO-55	Chip	BTD	Octal Latch W/Inverting Tri-State Out;0 to 70°C;Plastic Pkg	MMI
63	MMI67S382J	6701	IO-55	Chip	BTD	Octal Latch W/Inverting 32mA Tri-State Out;0 to 70°C;Ceramic Pkg	MMI
64	MMI67S382N	6701	IO-55	Chip	BTD	Octal Latch W/Inverting 32mA Tri-State Out;0 to 70°C;Plastic Pkg	MMI
65	MMI67401J	6701	IO-55	Chip	BTD	64x4 FIFO Mem;Synchronous/Asynchronous;10MHz Shift Rate;0 to 70°C	MMI
66	MMI67S373J	6701	IO-56	Chip	BTD	Octal Latch W/Non-Inverting 32mA Tri-State Out;0 to 70°C;Ceramic Pkg	MMI
67	MMI67S373N	6701	IO-56	Chip	BTD	Octal Latch W/Non-Inverting 32mA Tri-State Out;0 to 70°C;Plastic Pkg	MMI
68	MMI67508	6701	IO-90	Chip	BTD	8x8 Multiplier/Divider;Provides Mult/Div of 2s Complement Numbers	MMI
69	MMI67516	6701	IO-90	Chip	BTD	16x16 Multiplier/Divider;Provides Mult/Div of 2s Complement Numbers	MMI
70	MMI67558-1D	6701	IO-90	Chip	BTD	8x8 Multiplier;Signed,Unsigned or Mixed Mult,Speed 125ns max	MMI
71	MMI67558D	6701	IO-90	Chip	BTD	8x8 Multiplier;Signed,Unsigned,or Mixed Mult;0 to 70°C	MMI
72	MMI6384-1D	6701	PROM	Chip	BTD	1024x8 PROM;Access Time 90ns;Open Collector;0 to 70°C;24 Pin Ceramic	MMI
73	MMI6384-1J	6701	PROM	Chip	BTD	1024x8 PROM;Access Time 90ns;Open Collector;0 to 70°C;24 Pin Cerdip	MMI
74	MMI6385-1D	6701	PROM	Chip	BTD	1024x8 PROM;Access Time 90ns;Tri-State;0 to 70°C;24 Pin Ceramic	MMI
75	MMI6385-1J	6701	PROM	Chip	BTD	1024x8 PROM;Access Time 90ns;Tri-State;0 to 70°C;24 Pin Cerdip	MMI
76	MMI6386-1D	6701	PROM	Chip	BTD	1024x8 PROM;Access Time 90ns;Open Collector;0 to 70°C;22 Pin Ceramic	MMI
77	MMI6386-1J	6701	PROM	Chip	BTD	1024x8 PROM;Access Time 90ns;Open Collector;0 to 70°C;22 Pin Cerdip	MMI
78	MMI6387-1D	6701	PROM	Chip	BTD	1024x8 PROM;Access Time 90ns;Tri-State;0 to 70°C;22 Pin Ceramic	MMI
79	MMI6387-1J	6701	PROM	Chip	BTD	1024x8 PROM;Access Time 90ns;Tri-State;0 to 70°C;22 Pin Cerdip	MMI
80	MMI6281-2J	6701	ROM	Chip	BTD	1024x8 ROM;Improved Version of MMI6281-1J;Access Time 55ns	MMI
81	MN5500	Z80,MCS80	IO-41	Chip		12 Bit A/D Converter,Microprocessor Interfaced,Through Put Rate 40kHz	MNC
82	MN2020	6800	IO-92	HYB		Digitally Controlled Programmable Gain Amplifier	MNC
83	RAM68/32	CMC68/15	RAM	MOD		8 Bit, 32k RAM, 15 Address, 75RCI , 32k RAM, 15 Address, 75ime	MOS
84	MK9703	F8	uCT	Chip	BT	MK3874 Version Prom Not Included Standby Power Included	MOS
85	MK9704	F8	uCT	Chip	BT	MK3874 Version Prom and Standby Power Both Included	MOS
86	MKB3870P10	F8	uCT	Chip	MNX	Military 2048x8 ROM Temp -40 to 85	MOS
87	MK3854N	F8	IO-03	Chip	MNX	Direct Memory Access	MOS
88	MK3870N/14X	F8-MOS	uCT	Chip	MNG	8Bit Microcomputer Software Compatibility Plastic	MOS
89	MK3870P/14X	F8-MOS	uCT	Chip	MNG	8Bit Microcomputer Software Compatibility Ceramic	MOS
90	MK3872N/16X	F8-MOS	uCT	Chip	MNX	F8 Compatible Single Chip Microcomputer Non-Standby Device	MOS
91	MK3872N/17X	F8-MOS	uCT	Chip	MNX	Same as MK3872N/16X Except Standby Device	MOS
92	MK3872P/16X	F8-MOS	uCT	Chip	MNX	Same as MK3872N/16X Except Ceramic	MOS
93	MK3872P/17X	F8-MOS	uCT	Chip	MNX	Same as MK3872N/17X Except Ceramic	MOS
94	MK3873	F8-MOS	uCT	Chip	MNX	Capable of Synch or Asynch I/O Software Compatible	MOS
95	MK3874	F8-MOS	uCT	Chip	MNX	P-PROM Single-Chip Microprocessor	MOS
96	MK3876N/16X	F8-MOS	uCT	Chip	MNG	8Bit Microcomputer Single Chip 64Bytes and 32Bits Non Standby Device	MOS
97	MK3876N/17X	F8-MOS	uCT	Chip	MNG	8Bit Microcomputer Single Chip 64Bytes and 32Bits Standby Device	MOS
98	MK3876P/16X	F8-MOS	uCT	Chip	MNG	Same as MK3876N/16X Except Ceramic	MOS
99	MK3876P/17X	F8-MOS	uCT	Chip	MNG	Same as MK3876N/17 Except Ceramic	MOS
100	MK97400	F8-MOS	uCT	Chip	BT	MK3874 Version PROM and Standby Power Not Included	MOS
101	MK97401	F8-MOS	uCT	Chip	BT	MK3874 Version PROM Included Standby Power Not Included	MOS
102	MK97402	F8-MOS	uCT	Chip	BT	Same as MK97400	MOS
103	MK97403	F8-MOS	uCT	Chip	BTX	MK3874 Version PROM Not Included Standby Power Included	MOS
104	MK97404	F8-MOS	uCT	Chip	BTX	MK3874 Version PROM and Standby Power Both Included	MOS
105	MK97405	F8-MOS	uCT	Chip	BTX	Same as MK97403	MOS
106	MK3850	F8-MOS	CPU	Chip	MNX	CPU;8 Bit ALU,Interrupt Control	MOS
107	MK3850N-3	F8-MOS	CPU	Chip	MNX	CPU 8Bit ALU Interrupt Control	MOS
108	MK3850N-13	F8-MOS	CPU	Chip	MNX	CPU 8Bit Alu Interrupt Control Same as MK3850N-3 Except Temp -40 to 85	MOS
109	MK3850P-3	F8-MOS	CPU	Chip	MNX	Same as MK3850N-3 Except Ceramic	MOS
110	MK3850P-13	F8-MOS	CPU	Chip	MNX	Same as MK3850N-13 Except Ceramic	MOS

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MK3850P-23	F8-MOS	CPU	Chip	MNX	CPU 8 Bit ALU Interrupt Control Ceramic Temp -55 to 125	MOS
2	MK3871/90072	F8-MOS	DEV	MOD		EMU-70 Open Drain PIO	MOS
3	MK79001	F8-MOS	DEV	MOD		F8 Survival Kit;Kit Form	MOS
4	MK79002	F8-MOS	DEV	MOD		F8 Survival Kit;Assembled And Tested Unit	MOS
5	MK79030	F8-MOS	DEV	MOD		Emulator (EMU-70) For The Single Chip Microcomputer MK3870	MOS
6	MK79032	F8-MOS	DEV	MOD		Emulator EMU-70 With Two MK2708 PROMs	MOS
7	MK79076	F8-MOS	DEV	MOD		Application Interface Module (AIM-72);Real Time In Ckt Emulation	MOS
8	MK79077	F8-MOS	DEV	MOD		Same as AIM72 Except for Escape Key	MOS
9	MK79078	F8-MOS	DEV	MOD		3870 Series Microcomputer Emulator(EMU-72);Uses MK2716 PROMs	MOS
10	MK3854N-10	F8-MOS	IO-03			Direct Memory Access Temp -40 to 85	MOS
11	MK3854P	F8-MOS	IO-03			Direct Memory Access Ceramic	MOS
12	MK3854P-10	F8-MOS	IO-03			Same as MK3854N-10 Except Ceramic	MOS
13	MK3852N	F8-MOS	IO-03	Chip	MNX	64k Dynamic or Static RAM	MOS
14	MK3852N-10	F8-MOS	IO-03	Chip	MNX	64k Dynamic or Static RAM Temp -40 to 85	MOS
15	MK3852P	F8-MOS	IO-03	Chip	MNX	Same as MK3852N Except Ceramic	MOS
16	MK3852P-10	F8-MOS	IO-03	Chip	MNX	Same as MK3852N-10 Except Ceramic	MOS
17	MK3853N	F8-MOS	IO-03	Chip	MNX	Static Memory Interface	MOS
18	MK3853N-10	F8-MOS	IO-03	Chip	MNX	Static Memory Interface Temp -40 to 85	MOS
19	MK3853N-20	F8-MOS	IO-03	Chip	MNX	Static Memory Interface Temp -55 to 125	MOS
20	MK3853P	F8-MOS	IO-03	Chip	MNX	Same as MK3853N Except Ceramic	MOS
21	MK3853P-10	F8-MOS	IO-03	Chip	MNX	Same as MK3853N-10 Except Ceramic	MOS
22	MK3853P-20	F8-MOS	IO-03	Chip	MNX	Same as MK3853N-20 Except Ceramic	MOS
23	MK79066	F8-MOS	IO-09	MOD		Character Generator ROM(MK34073) for VAB-2(MK79052)	MOS
24	MK3861	F8-MOS	IO-30	Chip	MNX	Peripheral Input/Output Special Versions Available	MOS
25	MK3871N/90X	F8-MOS	IO-30	Chip	MNG	Peripheral I/O 90X Meaning Special Versions Available	MOS
26	MK3871P/90X	F8-MOS	IO-30	Chip	MNG	Same as MK3871N/90X Except Ceramic	MOS
27	MK79053	F8-MOS	IO-33	MOD		AIM-70(MK79031) Adapter Board;Interfaces AIM70 to SDB-50/70 Bus	MOS
28	MK79003	F8-MOS	IO-92	MOD		Power Supply and Teletype Cable for MK79002	MOS
29	MK3851N/12X	F8-MOS	ROM	Chip	MNX	Program Storage Unit (PSU) 1024 x 8 ROM Program Timer	MOS
30	MK3851P/12X	F8-MOS	ROM	Chip	MNX	Same as MK3851N/12X Except Ceramic	MOS
31	MK78033	Z80	DEV	MOD		Universal Serial uDI-S	MOS
32	MK78035	Z80	DEV	MOD		Display Parallel uDI-P	MOS
33	MK78036	Z80	DEV	MOD		Interface Screen Read Option	MOS
34	MK78039	Z80	DEV	MOD		Back-80E Development Station Z80 6 Total Slots Power Supply No Cards	MOS
35	MK78041	Z80	DEV	MOD		Software Development Board 16k Byte	MOS
36	MK78042	Z80	DEV	MOD		Dual Disk System 58k RAM 30x24 Display Terminal	MOS
37	MK78103	Z80	DEV	MOD		SDB-80E OEM-80 DDT-80 ASMB-80 Edit-80 4k Byte RAM	MOS
38	MK78104	Z80	DEV	MOD		Same as MK78103 Except 16k Byte RAM	MOS
39	MK78106	Z80	DEV	MOD		AIM-80E(ICE) In Circuit Emulation	MOS
40	MK78109	Z80	DEV	MOD		RAM-80 16k RAM	MOS
41	MK78110	Z80	DEV	MOD		RAM-80BE 16k RAM 2 PIO	MOS
42	MK78112	Z80	DEV	MOD		FLP-80E Floppy Interface	MOS
43	MK78118	Z80	DEV	MOD		DDT-80 Debug 2k Byte ROM	MOS
44	MK78119	Z80	DEV	MOD		ASMB-80 Edit-80 2k Byte Including Editor	MOS
45	MK78122	Z80	DEV	MOD		Software Development Board OEM-80E 4k Bytes RAM	MOS
46	MK78124	Z80	DEV	MOD		Software Development Board OEM-80E 16k Bytes RAM	MOS
47	MK78128	Z80	DEV	MOD		RIO-80E 16k PROM 2 PIO 1-CTC uART	MOS
48	MK78155	Z80	DEV	MOD		High Level Analog I/O Board	MOS
49	MK78157	Z80	DEV	MOD		Mostek Basic Interpreter Requires 32k Bytes of RAM	MOS
50	MK78158	Z80	DEV	MOD		MOSTEK Fortran 1V Requires 48k Bytes or RAM	MOS
51	MK78164	Z80	DEV	MOD		Twenty-Three Programs for Running Both Source and Binary on Diskette	MOS
52	MK78166	Z80	DEV	MOD		High Level Analog Board	MOS
53	MK78167	Z80	DEV	MOD		Low Level Nonisolated Analog Input Board	MOS
54	MK78168	Z80	DEV	MOD		Low Level Nonisolated Analog I/O Board	MOS
55	MK78169	Z80	DEV	MOD		Analog Output Board	MOS
56	MK78170	Z80	DEV	MOD		Wide Range Isolated Analog Board	MOS
57	MK78171	Z80	DEV	MOD		Wide Range Isolated Analog I/O Board	MOS
58	MK78962	Z80	DEV	MOD		FLP-80DOS/MDX Bootstrap Proms	MOS
59	MK79054	Z80	DEV	MOD		Back-80E Backplane Card 6 Slot	MOS
60	MK79062	Z80	DEV	MOD		PPG-08 Extender Card	MOS
61	MK79063	Z80	DEV	MOD		PPG-08 Wire Wrap Card	MOS
62	RAM-80A	Z80	DEV	MOD		16k Byte RAM Board	MOS
63	RAM-80B	Z80	DEV	MOD		Combination Memory and I/O Expansion Board	MOS
64▼	MK78146	Z80	IO-07	MOD		Disk Controller;Interface w/4 Flex Disk Drive to MOS SW Dev Bd	MOS
65▼	MK78192	Z80	IO-20	MOD		MultiChannel Serial I/O Module;4 Independent Full Duplex Chan	MOS
66▼	MK77665	Z80	IO-40	MOD		12 Bit D/A Converter w/4 Independent Chan	MOS
67▼	MK77655	Z80	IO-41	MOD		12 Bit A/D Converter w/16 Single Ended or 8 Diff In Chan	MOS
68▼	MK77669	Z80	IO-41	MOD		8 Bit A/D Converter w/16 Single Ended Analog Input	MOS
69▼	MK77669-4	Z80	IO-41	MOD		8 Bit A/D Converter w/16 Single Ended Analog Input	MOS
70▼	MK78172-42	Z80	IO-41	MOD		12 Bit A/D Converter 16 Single Ended Input Chan	MOS
71▼	MK78172-56	Z80	IO-41	MOD		12 Bit A/D Converter 32 Differential Input Chan	MOS
72▼	MK78175-40	Z80	IO-41	MOD		12 Bit A/D Converter 16 Single Ended Input Chan	MOS
73▼	MK78177-26	Z80	IO-41	MOD		12 Bit A/D Converter 4 Double Ended Input Chan	MOS
74▼	MK77654	Z80	IO-45	MOD		Analog Data Acquisition and Control Board	MOS
75▼	MK77652	Z80	IO-92	MOD		Provides All Required Controlling/Formatting/Interfacing Logic	MOS
76▼	MK77963	Z80	IO-92	MOD		System Controller/Diagnostic Bd	MOS
77▼	MK77963-4	Z80	IO-92	MOD		System Controller/Diagnostic Bd	MOS
78▼	MK77967	Z80	IO-92	MOD		Interrupt-Timer Expansion Module	MOS
79	MK4027-2	Z80	RAM	Chip	MNX	4096x1 Dynamic RAM Cycle Time 320ns	MOS
80	MK4027-3	Z80	RAM	Chip	MNX	4096x1 Dynamic RAM Cycle Time 375ns	MOS
81	MK4116-4	Z80	RAM	Chip	MNX	16kx1 Dynamic RAM Cycle Time 410ns	MOS
82	MD-SBC1	Z80-MOS	COMP	MOD		8 Bit Microcomputer on a Card,Uses Z80 CPU	MOS
83	MK77851	Z80-MOS	COMP	MOD		MD-SBC1;8 Bit Z80 Single Board Computer,4.5 x 6.5 Inch,56 Pin Connector	MOS
84	MK78121	Z80-MOS	COMP	MOD	MNG	OEM-80(4k) System;Complete Microcomputer W/4k RAM,Up to 5k PROM	MOS
85	MK78123	Z80-MOS	COMP	MOD	MNG	OEM-80(16k) System;Complete Microcomputer W/16k RAM,Up to 5k PROM	MOS
86	MK78125	Z80-MOS	COMP	UNIT	MNG	AID-80F;8 Bit Z80 Microcomputer System,Includes OEM80,RAM80 and FLP-80	MOS
87	MK3880	Z80-MOS	CPU	Chip	MNG	8 Bit Microprocessor With Built-in Dynamic RAM Refresh Circuitry	MOS
88	MKB3880P14	Z80-MOS	CPU	Chip	MNG	Military 8Bit Microprocessor Temp -40 to 85 Frequency 4.0MHz	MOS
89	MKB3880P34	Z80-MOS	CPU	Chip	MNG	Military 8Bit Microprocessor Temp -55 to 100	MOS
90	MK77850	Z80-MOS	CPU	MOD		On Board Memory 256 Bytes of Scratchpad System Clock 2.5MHz	MOS
91	MK77850-4	Z80-MOS	CPU	MOD		Same as MK77850 Except System Clock 4.0MHz	MOS
92	MK77958	Z80-MOS	CPU	MOD		Single Step Capability System Clock Max 4.0MHz	MOS
93	MK3871/90070	Z80-MOS	DEV	MOD		EMU-70 Direct Drive PIO	MOS
94	MK77950	Z80-MOS	DEV	MOD		MDX-DEBUG;Z80 Microcomputer Debug Module,10k Bytes Firmware,Clock 2.5MHz	MOS
95	MK77950-4	Z80-MOS	DEV	MOD		MDX-DEBUG-4;Z80 Microcomputer Debug Module,10k Bytes Firmware,Clock4.0MHz	MOS
96	MK77951-4	Z80-MOS	DEV	MOD		Prototyping Package System Clock 40MHz	MOS
97	MK78132	Z80-MOS	DEV	MOD		Z80 Applications Interface Module (AIM-80);For in Ckt Emulation	MOS
98	MK78172-7	Z80-MOS	DEV	MOD		A/D-80 Family of A/D Converter Cards	MOS
99	MK79079	Z80-MOS	DEV	MOD		FZCASM Relocatable 3870/F8 Cross Assembler to Run on AID-80F	MOS
100	MK79082	Z80-MOS	DEV	MOD		PPG-8/16 PROM Programmer	MOS
101	MK77951	Z80-MOS	DEV	MODS		MDX-PROTO:MD Series Prototyping Pkg for Evaluation of Microcomp Modules	MOS
102	MK78101	Z80-MOS	DEV	UNIT		Stand Alone Microcomputer SDB-80(4k);For Developing Z80 Software	MOS
103	MK78102	Z80-MOS	DEV	UNIT		Stand Alone Microcomputer SDB-80(16k);For Developing Z80 Software	MOS
104	MK78125-0001	Z80-MOS	DEV	UNIT		AID-80F-FQ Floppy Disk Development with 50Hz 220v Option	MOS
105	MK78125-001	Z80-MOS	DEV	UNIT		AID-80F-OS Floppy Disk Development with Double-sided Drive Option	MOS
106	MK78125-01	Z80-MOS	DEV	UNIT		AID-80F-P PPG-8/16 Integrated into AID-80F	MOS
107	MK78125-1	Z80-MOS	DEV	UNIT		AID-80F-16 Floppy Disk Development With 16k Dyn RAM Only	MOS
108	MK78125-2	Z80-MOS	DEV	UNIT		AID-80F-48 Floppy Disk Development With 48 Dyn RAM	MOS
109	MK78125-3	Z80-MOS	DEV	UNIT		AID-80F-64 Floppy Disk Development with 64k Dyn RAM	MOS
110	MK3882N	Z80-MOS	IO-01	Chip	MNG	Counter-Timer Circuit Provides 4 Channels of Timing for MK3880 CPU	MOS

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MK3882N-4	Z80-MOS	IO-01	Chip	MNG	Same as MK3882N Except Clock Freq 4.0MHz	MOS
2	MK3882N-10	Z80-MOS	IO-01	Chip	MNG	Same as MK3882N Except Clock Freq 2.5MHz and Temp -40 to 85	MOS
3	MK3882P	Z80-MOS	IO-01	Chip	MNG	Same as MK3882N Except Ceramic	MOS
4	MK3882P-4	Z80-MOS	IO-01	Chip	MNG	Same as MK3882N-4 Except Ceramic	MOS
5	MK3882P-10	Z80-MOS	IO-01	Chip	MNG	Same as MK3882N-10 Except Ceramic	MOS
6	MKB3882P14	Z80-MOS	IO-01	Chip	MNG	Military 8Bit Counter-Timer 4 8Bit Channels Temp -40 to 85	MOS
7	MKB3882P20	Z80-MOS	IO-01	Chip	MNG	Military 8Bit Counter-Timer 4 8Bit Channels Temp -55 to 125	MOS
8	MK3883N	Z80-MOS	IO-03	Chip	MNG	DMA Controller 1.2M Byte/Sec Data Rate	MOS
9	MK3883N-4	Z80-MOS	IO-03	Chip	MNG	Same as MK3883N Except Max Clock Freq 4.0MHz	MOS
10	MK3883P	Z80-MOS	IO-03	Chip	MNG	Same as MK3883N Except Ceramic	MOS
11	MK3883P-4	Z80-MOS	IO-03	Chip	MNG	Same as MK3883N-4 Except Ceramic	MOS
12	MK77758	Z80-MOS	IO-03	MOD		EPROM Memory 4k Boundary 4MHz Operation	MOS
13	MK77759	Z80-MOS	IO-03	MOD		MDX-UMC 4k Boundary Slower Memories 4MHz	MOS
14	MK78111	Z80-MOS	IO-07	MOD		Floppy Disk Drive Controller Bd(FLP-80);Interfaces SDB-80 to Max of 4FDD	MOS
15	MK3884N	Z80-MOS	IO-20	Chip	MNG	Serial I/O Controller Full Duplex Sync and Async Capability	MOS
16	MK3884N-10	Z80-MOS	IO-20	Chip	MNG	Same as MK3884N Except Temp -40 to 85	MOS
17	MK3884P	Z80-MOS	IO-20	Chip	MNG	Same as MK3884N Except Ceramic	MOS
18	MK3884P-10	Z80-MOS	IO-20	Chip	MNG	Same As MK3884N-10 Except Ceramic	MOS
19	MK3885N	Z80-MOS	IO-20	Chip	MNG	Ser I/O Controller Full Duplex Synch/Asyn A1 Bonding Option to MK3884N	MOS
20	MK3885N-10	Z80-MOS	IO-20	Chip	MNG	Same as MK3885N Except Temp -40 to 85	MOS
21	MK3885P	Z80-MOS	IO-20	Chip	MNG	Same as MK3885N Except Ceramic	MOS
22	MK3887N	Z80-MOS	IO-20	Chip	MNG	A1 Bonding Option to MK3884N Max Clock Freq 25MHz Temp 0 t o 70	MOS
23	MK3887N-10	Z80-MOS	IO-20	Chip	MNG	Same as MK3887N Except Temp -40 to 85	MOS
24	MK3887P	Z80-MOS	IO-20	Chip	MNG	Same as MK3887N Except Ceramic	MOS
25	MK77651	Z80-MOS	IO-20	MOD		MDX-SIO,Serial I/O Module;System Clock 2.5MHz Max,110 to 19.2k Bits/Sec	MOS
26	MK77651-4	Z80-MOS	IO-20	MOD		MDX-SIO-4,Serial I/O Module;System Clock 4.0 MHZ Max	MOS
27	MK3881N	Z80-MOS	IO-30	Chip	MNG	Parallel I/O Controller Programmable 2 Port Device Plastic Temp 0 to 70	MOS
28	MK3881P	Z80-MOS	IO-30	Chip	MNG	Same as MK3881N Except Ceramic Pkg	MOS
29	MK3881P-4	Z80-MOS	IO-30	Chip	MNG	Same as MK3881N-4 Except Ceramic	MOS
30	MK3881P-10	Z80-MOS	IO-30	Chip	MNG	Same as MK3881P-4 Except Max Clock Freq 25MHz and Temp -40 to 85	MOS
31	MK3881P-20	Z80-MOS	IO-30	Chip	MNG	Same as MK3881P-10 Except Temp Range -55 to 125	MOS
32	MKB3881P14	Z80-MOS	IO-30	Chip	MNG	Military 8Bit Parallel I/O Controller Programmable Temp -40 to 85	MOS
33	MK77650	Z80-MOS	IO-33	MOD		MDX-PIO;Programmable I/O Unit,Four 8Bit I/O Ports,System Clock 2.5MHz	MOS
34	MK77650-4	Z80-MOS	IO-33	MOD		MDX-PIO-4;Programmable I/O Unit,Four 8Bit I/O Ports,System Clock 4.0MHz	MOS
35	MK77653	Z80-MOS	IO-41	MOD		MDX-A/D 16 Channel Single Ended System Clock 25MHz	MOS
36	MK77653-4	Z80-MOS	IO-41	MOD		MDX-A/D 16 Channel Single Ended System Clock 40MHz	MOS
37	MK3886	Z80-MOS	IO-57	Chip	MNG	Z80 COMBO Chip:Incl 256x8 RAM,Ser IO Port Progm Timer,4 Ext Interrupts	MOS
38	MK79081	Z80-MOS	PE-50	UNIT		PROM Programmer for 2708/2758/2716 PROMs W/Driver Software(PPG-8/16)	MOS
39	MK2708	Z80-MOS	PROM	Chip	MNX	1024x8 EPROM;Access Time 450ns	MOS
40	MK3602P-1	Z80-MOS	PROM	Chip	MNG	256x8 Bit Electrically Programmable ROM;Access Time 550ns	MOS
41	MK3602P-2	Z80-MOS	PROM	Chip	MNG	256x8 Bit Electrically Programmable ROM;Access Time 750ns	MOS
42	MK3602P-3	Z80-MOS	PROM	Chip	MNG	256x8 Bit Electrically Programmable ROM;Access Time 1.0us	MOS
43	MK3702T-1	Z80-MOS	PROM	Chip	MNG	256x8 Bit Erasable ROM;Acess Time 550ns	MOS
44	MK3702T-2	Z80-MOS	PROM	Chip	MNG	256x8 Bit Erasable ROM;Access Time 750ns	MOS
45	MK3702T-3	Z80-MOS	PROM	Chip	MNG	256x8 Bit Erasable ROM;Access Time 1.0us	MOS
46	MK77753	Z80-MOS	PROM	MOD		MDX-EPROM/UART;EPROM Add-On Module For The STD BUS,Clock 2.5MHz	MOS
47	MK77753-4	Z80-MOS	PROM	MOD		MDX-EPROM/UART-4;EPROM Add-On Module For The STD BUS,Clock 4.0MHz	MOS
48	MK4027	Z80-MOS	RAM	Chip	MNX	4096x1 Dyn RAM;Access Time 150-250ns	MOS
49	MK4027-4	Z80-MOS	RAM	Chip	MNX	Same as MK4027-3	MOS
50	MK4096	Z80-MOS	RAM	Chip	MNX	4096x1 Dyn RAM;Access Time 250-350ns	MOS
51	MK4102N-11	Z80-MOS	RAM	Chip	MNG	1024x1 Bit Static RAM;Access Time 450ns;Plastic Pkg	MOS
52	MK4102N-12	Z80-MOS	RAM	Chip	MNG	1024x1 Bit Static RAM;Access Time 1.0us;Plastic Pkg	MOS
53	MK4104	Z80-MOS	RAM	Chip	MNX	4096X1 Edge Activated RAM;Access Time 200-350ns	MOS
54	MK4104-3	Z80-MOS	RAM	Chip	MNX	4096x1 Edge Activated RAM Cycle Time 310ns	MOS
55	MK4104-4	Z80-MOS	RAM	Chip	MNX	4096x1 Edge Activated RAM Cycle Time 385ns	MOS
56	MK4104-5	Z80-MOS	RAM	Chip	MNX	4096x1 Edge Activated RAM Cycle Time 460ns	MOS
57	MK4114	Z80-MOS	RAM	Chip	MNX	1024x1 Edge Activated RAM;Access Time 200-350ns	MOS
58	MK4116	Z80-MOS	RAM	Chip	MNX	16kx1 Dyn RAM;Access Time 150-250ns	MOS
59	MK4116-2	Z80-MOS	RAM	Chip	MNX	16k x 1 Dynamic RAM Access Time 150-250ns Cycle Time 375ns	MOS
60	MK4116-3	Z80-MOS	RAM	Chip	MNX	Same as MK4116-2	MOS
61	MKB4027J2	Z80-MOS	RAM	Chip	MNX	Military 4kx1 Dynamic RAM Access Time 150ns Temp 0 to 70	MOS
62	MKB4027J3	Z80-MOS	RAM	Chip	MNX	Military 4kx1 Dynamic RAM Access Time 200ns Temp 0 to 70	MOS
63	MKB4027J4	Z80-MOS	RAM	Chip	MNX	Military 4kx1 Dynamic RAM Access Time 250ns Temp 0 to 70	MOS
64	MKB4027J83	Z80-MOS	RAM	Chip	MNX	Military 4kx1 Dynamic RAM Access Time 200ns Temp -55 to 85	MOS
65	MKB4027J84	Z80-MOS	RAM	Chip	MNX	Military 4kx1 Dynamic RAM Access Time 250ns Temp -55 to 85	MOS
66	MKB4104J4	Z80-MOS	RAM	Chip	MNX	Military 4096z1 Edge Activated RAM Temp 0 to 70 Access Time 250ns	MOS
67	MKB4104J5	Z80-MOS	RAM	Chip	MNX	Military 4096z1 Edge Activated RAM Temp 0 to 70 Access Time 300ns	MOS
68	MKB4104J6	Z80-MOS	RAM	Chip	MNX	Military 4096z1 Edge Activated RAM Temp 0 to 70 Access Time 350ns	MOS
69	MKB4104J85	Z80-MOS	RAM	Chip	MNX	Military 4096z1 Edge Activated RAM Temp -55 to 125 Access Time 300ns	MOS
70	MKB4104J86	Z80-MOS	RAM	Chip	MNX	Military 4096z1 Edge Activated RAM Temp -55 to 125 Access Time 350ns	MOS
71	MKB4116F84	Z80-MOS	RAM	Chip	MNX	Military 16kx1 Dynamic RAM Temp -55 to 85 Access Time 250ns 16 Pin Flat	MOS
72	MKB4116J2	Z80-MOS	RAM	Chip	MNX	Military 16k x 1 Dynamic RAM Temp 0 to 70 Access Time 150ns	MOS
73	MKB4116J3	Z80-MOS	RAM	Chip	MNX	Military 16k x 1 Dynamic RAM Temp 0 to 70 Access Time 200ns	MOS
74	MKB4116J4	Z80-MOS	RAM	Chip	MNX	Military 16k x 1 Dynamic RAM Temp 0 to 70 Access Time 250ns	MOS
75	MKB4116J83	Z80-MOS	RAM	Chip	MNX	Military 16k x 1 Dynamic RAM Temp -55 to 85 Access Time 200ns No Refresh	MOS
76	MKB4116J84	Z80-MOS	RAM	Chip	MNX	Military 16k x 1 Dynamic RAM Temp -55 to 85 Access Time 250ns	MOS
77	MKB4116J93	Z80-MOS	RAM	Chip	MNX	Military 16k x 1 Dynamic RAM Temp -55 to 85 Access Time 200ns 1ms Refresh	MOS
78	MK77750	Z80-MOS	RAM	MOD		MDX-DRAM8;8kx8 Dynamic RAM,System Clock 2.5MHz,Access Time 350ns Max	MOS
79	MK77751	Z80-MOS	RAM	MOD		MDX-DRAM16;16kx8 Dynamic RAM,System Clock 2.5MHz,Access Time 350ns Max	MOS
80	MK77752	Z80-MOS	RAM	MOD		MDX-DRAM32;32kx8 Dynamic RAM,System Clock 2.5MHz,Access Time 350ns Max	MOS
81	MK77752-4	Z80-MOS	RAM	MOD		MDX-DRAM32-4;32kx8 Dynamic RAM,System Clock 4.0MHz,Access Time 200ns Max	MOS
82	MK77754	Z80-MOS	RAM	MOD		MDX-DRAM 16,16k x 8 Dyn RAM;System Clock 2.5MHz	MOS
83	MK77754-4	Z80-MOS	RAM	MOD		MDX-DRAM16-4;16kx8 Dynamic RAM,System Clock 4.0MHz,Access Time 200ns Max	MOS
84	MK77755	Z80-MOS	RAM	MOD		MDX-SRAM 4k x 8 Memory Size Memory Access 250ns	MOS
85	MK77756	Z80-MOS	RAM	MOD		MDX-SRAM 8k x 8 Memory Size Memory Access 250ns	MOS
86	MK77757	Z80-MOS	RAM	MOD		MDX-SRAM16 16k x 8 Memory Size Memory Access 250ns	MOS
87	MK78107	Z80-MOS	RAM	MOD		16384 Byte RAM Board W/32 MK4027s (RAM-80A)	MOS
88	MK78108	Z80-MOS	RAM	MOD		16384 Byte RAM Board W/8 MK4116s (RAM-80B)	MOS
89	MK30000	Z80-MOS	ROM	Chip	MNX	1024x8 ROM;Access Time 350ns	MOS
90	MK31000P	Z80-MOS	ROM	Chip	MNG	2048x8 Bit Static ROM;Access Time 550ns	MOS
91	MK32000	Z80-MOS	ROM	Chip	MNX	4096x8 ROM;Access Time 350ns	MOS
92	MK34000P	Z80-MOS	ROM	Chip	MNG	2048x8 Bit Static ROM;Access Time 350ns	MOS
93	MK36000	Z80-MOS	ROM	Chip	MNX	8192x8 ROM;Access Time 350ns	MOS
94	MKB34000P80	Z80-MOS	ROM	Chip	MNX	Military 2kx8 ROM Temp -40 to 85 Access Time 450ns	MOS
95	MKB34000P84	Z80-MOS	ROM	Chip	MNX	Military 2k x 8 ROM Temp -55 to 125 Access Time 450ns	MOS
96	MKB34000P	Z80-MOS	ROM	Chip	MNX	Military 2kx8 ROM Temp 0 to 70 Access Time 350ns	MOS
97	MKB36000P80	Z80-MOS	ROM	Chip	MNX	Military 8kx8 ROM Temp -40 to 85 Access Time 300ns	MOS
98	MKB36000P84	Z80-MOS	ROM	Chip	MNX	Military 8kx8 ROM Temp -55 to 125 Access Time 300ns	MOS
99	MKB36000P	Z80-MOS	ROM	Chip	MNX	Military 8kx8 ROM Temp 0 to 70 Access Time 250ns	MOS
100	MK3884N-4	Z80A-MOS	IO-20	Chip	MNG	Same as MK3884N Except Max Clock Freq 4MHzx	MOS
101	MK3884P-4	Z80A-MOS	IO-20	Chip	MNG	Same as MK3884N-4 Except Ceramic	MOS
102	MK3885P-4	Z80A-MOS	IO-20	Chip	MNG	Same as MK3885N-4 Except Ceramic	MOS
103	MK3887N-4	Z80A-MOS	IO-20	Chip	MNG	Same as MK3887N Except Max Clock Freq 4MHz	MOS
104	MK3887P-4	Z80A-MOS	IO-20	Chip	MNG	Same as MK3887N-4 Except Ceramic	MOS
105	MK3871N/90070	3870	DEV	MOD		EMU-70 Direct Drive PIO	MOS
106	MK3871N/90072	3870	DEV	MOD		Open Drain PIO	MOS
107	MK3871P/90070	3870	DEV	MOD		Same As MK3871N/90070 Except Ceramic	MOS
108	MK3871P/90072	3870	DEV	MOD		Same As MK3871N/90072 Except Ceramic	MOS
109	MK79052	3870-MOS	DEV	MOD			MOS
110	MK79056	3870-MOS	DEV	MOD			MOS

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MKB4027F84	Z80-MOS	RAM	Chip	MNX	Military 4kx1 Dynamic RAM Access Time 250ns Temp -55 to 85 16 Pin Flat	MOSS
2▼	M68K128DP		RAM	MOD		128k Byte Dyn RAM Mod;Includes Byte Parity;Fully VERSAbus Compatible	MOTA
3	MMS1102-31	LSI11	IO-55	MOD	MOS	8kx16 Add-ON Memory for use w/LSI 11 Systems	MOTA
4	MMS1102-31PC	LSI11	IO-55	MOD	MOS	8k x 16 Add-On Memory for Use w/LSI 11 Systems,w/Parity,Controller	MOTA
5	MMS1102-32	LSI11	IO-55	MOD	MOS	16kx16 Add-ON Memory for use w/LSI 11 Systems	MOTA
6	MMS1102-32PC	LSI11	IO-55	MOD	MOS	16k x 16 Add-On Memory for Use w/LSI 11 Systems,w/Parity,Controller	MOTA
7	MMS1102-34	LSI11	IO-55	MOD	MOS	32kx16 Add-ON Memory for use w/LSI 11 Systems	MOTA
8	MMS1102-34PC	LSI11	IO-55	MOD	MOS	32k x 16 Add-On Memory for Use w/LSI 11 Systems,w/Parity,Controller	MOTA
9	MMS1110	LSI11	IO-55	MOD		16k x 16 Plug In Main Memory System For Use With DECs LSI-11	MOTA
10	MMS1116	LSI11	IO-55	MOD		16k x 16 or 32k x 8 PDP11 Add-In Semiconductor Memory	MOTA
11	MMS1117-32	LSI11	IO-55	MOD		32k PDP-11 UNIBUS Compatible Plug-In Memory,Access Time-290nS	MOTA
12	MMS1117-32-P	LSI11	IO-55	MOD		32k PDP-11 UNIBUS Compatible Plug-In Memory, w/Parity,Access Time-290ns	MOTA
13	MMS1117-32PC	LSI11	IO-55	MOD		32k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Controller,290ns	MOTA
14	MMS1117-34	LSI11	IO-55	MOD		64k PDP-11 UNIBUS Compatible Plug-In Memory,Access Time-290nS	MOTA
15	MMS1117-34-P	LSI11	IO-55	MOD	:	64k PDP-11 UNIBUS Compatible Plug-In Memory, w/Parity,Access Time-290ns	MOTA
16	MMS1117-34PC	LSI11	IO-55	MOD		64k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Controller,290ns	MOTA
17	MMS1117-36-P	LSI11	IO-55	MOD		96k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-290ns	MOTA
18	MMS1117-36PC	LSI11	IO-55	MOD		96k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Controller,290ns	MOTA
19	MMS1117-38	LSI11	IO-55	MOD		128k PDP-11 UNIBUS Compatible Plug-In Memory,Access Time-290nS	MOTA
20	MMS1117-38-P	LSI11	IO-55	MOD		128k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-290hS	MOTA
21	MMS1117-38PC	LSI11	IO-55	MOD		128k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Controller,290ns	MOTA
22	MMS1117-42	LSI11	IO-55	MOD		32k PDP-11 UNIBUS Compatible Plug-In Memory ,Access Time-360nS	MOTA
23	MMS1117-42-P	LSI11	IO-55	MOD		32k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-360ns	MOTA
24	MMS1117-42-PC	LSI11	IO-55	MOD		32k PDP-11 UNIBUS Conpatible Plug-In Memory, w/Parity,Controller,360ns	MOTA
25	MMS1117-44	LSI11	IO-55	MOD		64k PDP-11 UNIBUS Compatible Plug-In Memory,Access Time-360nS	MOTA
26	MMS1117-44-P	LSI11	IO-55	MOD		64k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-360hS	MOTA
27	MMS1117-44-PC	LSI11	IO-55	MOD		64k PDP-11 UNIBUS Compatible Plug-In Memory, w/Parity,Controller,360ns	MOTA
28	MMS1117-46	LSI11	IO-55	MOD		96k PDP-11 UNIBUS Compatible Plug-In Memory, Access Time-360nS	MOTA
29	MMS1117-46-P	LSI11	IO-55	MOD		96k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-360ns	MOTA
30	MMS1117-46-PC	LSI11	IO-55	MOD		96k PDP-11 UNIBUS Compatible Plug-In Memory, w/Parity,Controller,360ns	MOTA
31	MMS1117-48	LSI11	IO-55	MOD		128k PDP-11 UNIBUS Compatible Plug-In Memory,Access Time-360nS	MOTA
32	MMS1117-48-P	LSI11	IO-55	MOD		128k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-360ns	MOTA
33	MMS1117-48-PC	LSI11	IO-55	MOD		128k PDP-11 UNIBUS Comptaible Plug-In Memory, w/Parity,Controller,360ns	MOTA
34	MMS1117-52	LSI11	IO-55	MOD		32k PDP-11 UNIBUS Compatible Plug-In Memory,Access Time-390nS	MOTA
35	MMS1117-52-P	LSI11	IO-55	MOD		32k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-390ns	MOTA
36	MMS1117-52-PC	LSI11	IO-55	MOD		32k PDP-11 UNIBUS Compatible Plug-In Memory, w/Parity,Controller,390ns	MOTA
37	MMS1117-54	LSI11	IO-55	MOD		64k PDP-11 UNIBUS Compatible Plug-In Memory,Access Time-390 nS	MOTA
38	MMS1117-54-P	LSI11	IO-55	MOD		64k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-390ns	MOTA
39	MMS1117-54-PC	LSI11	IO-55	MOD		64k PDP-11 UNIBUS Compatible Plug-In Memory, w/Parity,Controller,390ns	MOTA
40	MMS1117-56	LSI11	IO-55	MOD		96k PDP-11 UNIBUS Compatible Plug-In Memory, Access Time-390hs	MOTA
41	MMS1117-56-P	LSI11	IO-55	MOD		96k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-390ns	MOTA
42	MMS1117-56-PC	LSI11	IO-55	MOD		96k PDP-11 UNIBUS Compatible Plug-In Memory, w/Parity,Controller,390ns	MOTA
43	MMS1117-58	LSI11	IO-55	MOD		128k PDP-11 UNIBUS Compatible Plug-In Memory, Access Time-390hs	MOTA
44	MMS1117-58-P	LSI11	IO-55	MOD		128k PDP-11 UNIBUS Compatible Plug-In Memory,w/Parity,Access Time-390ns	MOTA
45	MMS1117-58-PC	LSI11	IO-55	MOD		128k PDP-11 UNIBUS Comptaible Plug-In Memory, w/Parity,Controller,390ns	MOTA
46	MMS1118	LSI11	IO-55	MOD		16kx18 Plug-In Main Memory for PDP-11/04,34 Computers	MOTA
47	MMS1118-1	LSI11	IO-55	MOD		12kx18 Plug-In Main Memory for PDP-11/04, 34 Computers	MOTA
48	MMS1118-2	LSI11	IO-55	MOD		8kx18 Plug-In Main Memory for PDP-11/04,34 Computers	MOTA
49	MMS3418	LSI11	IO-55	MOD		128kx18 Semiconductor Memory Card	MOTA
50	MMS80810	MCS80	IO-55	MOD		32k x 8 Plug In Semiconductor Memory For 8080A Systems	MOTA
51	MMS80810-1	MCS80	IO-55	MOD		16kx8 Bit Plug In Mem. Syst for 8080A Based Systems	MOTA
52	MGD8080DSM	MCS80	IO-92	MOD	MNX	Data Security Module;NMOS LSI Implementation of DES,160us Algorithm	MOTA
53	MC10900	MC10900	IO-12	Chip	BEX	MECL-LSI 8 Bit Parity ALU Slice;2 Input Data Ports;Int Latchl/O Ports	MOTA
54	MC14443AL	MC14100	IO-41	Chip	MCX	6 Channel Single Slope 10 Bit AD Converter;-55 to 125°C,Open Diam	MOTA
55	MC14443CL	MC14100	IO-41	Chip	MCX	6 Channel Single Slope 10 Bit AD Converter;-40 to 85°C,Open Diam	MOTA
56	MC14443CP	MC14100	IO-41	Chip	MCX	6 Channel Single Slope 10 Bit AD Converter;-40 to 85°C,Open Diam	MOTA
57	MC14447AL	MC14100	IO-41	Chip	MCX	6 Channel Single Slope 10 Bit AD Converter;-55 to 125°C	MOTA
58	MC14447CL	MC14100	IO-41	Chip	MCX	6 Channel Single Slope 10 Bit AD Converter;-40 to 85°C	MOTA
59	MC14447CP	MC14100	IO-41	Chip	MCX	6 Channel Single Slope 10 Bit AD Converter;-40 to 85°C	MOTA
60	MC141000L	MC141000	uCT	Chip		4 Bit Single Chip Microcomputer;1024x8B ROM;64x4B RAM;28p Pkg	MOTA
61	MC141000P	MC141000	uCT	Chip		4 Bit Single Chip Microcomputer;1024x8B ROM;64x4B RAM;28p Pkg	MOTA
62	MEX141000M	MC141000	DEV	MOD		MC141000/1200 Development System;M6800 EXORciser Based	MOTA
63	MC141099L	MC141099	uCT	Chip	MCX	4 Bit Single Chip Microcomputer;64x4B RAM,48 Pin Pkg	MOTA
64	MC141099P	MC141099	uCT	Chip	MCX	4 Bit Single Chip Microcomputer;64x4B RAM,48 Pin Pkg	MOTA
65	MC141200L	MC141200	uCT	Chip		4 Bit Single Chip Microcomputer;1024x8B ROM;64x4B RAM;40p Pkg	MOTA
66	MC141200P	MC141200	uCT	Chip		4 Bit Single Chip Microcomputer;1024x8B ROM;64x4B RAM;40p Pkg	MOTA
67	MC14500BAL	MC14500B	CPU	Chip	MCX	1 Bit Industrial Control Unit,-55 To 125°C;16 Pin Ceramic Pkg	MOTA
68	MC14500BCL	MC14500B	CPU	Chip	MCX	1 Bit Industrial Control Unit,-40 to 85°C;16 Pin Ceramic Pkg	MOTA
69	MC14500BCP	MC14500B	CPU	Chip	MCX	1 Bit Industrial Control Unit,-40 to 85°C;16 Pin Plastic Pkg	MOTA
70	DS14500A	MC14500B	DEV	MOD		Industrial Control Unit (ICU) Demonstration System;Includes DS14500B,C	MOTA
71	DS14500B	MC14500B	DEV	MOD		ICU Demonstration Unit;Processor Board Using MC14500B	MOTA
72	DS14500C	MC14500B	DEV	MOD		Input/Output Simulator Board;Used to Replace Controlled Equip	MOTA
73	MC14099BAL	MC14500B	IO-56	Chip	MCX	8 Bit Addressable Latch;Unidirection Port,-55 to 125°C,16 Pin Ceramic Pkg	MOTA
74	MC14099BCL	MC14500B	IO-56	Chip	MCX	8 Bit Addressable Latch;Unidirection Port,-40 to 85°C,16 Pin Ceramic Pkg	MOTA
75	MC14099BCP	MC14500B	IO-56	Chip	MCX	8 Bit Addressable Latch;Unidirection Port,-40 to 85°C,16 Pin Plastic Pkg	MOTA
76	MC14599BAL	MC14500B	IO-56	Chip	MCX	8 Bit Addressable Latch;Bidirectional Port;-55 to 125°C,18Pin Ceramic Pkg	MOTA
77	MC14599BCL	MC14500B	IO-56	Chip	MCX	8 Bit Addressable Latch;Bidirectional Port;-40 to 85°C,18Pin Ceramic Pkg	MOTA
78	MC14599BCP	MC14500B	IO-56	Chip	MCX	8 Bit Addressable Latch;Bidirectional Port;-40 to 85°C,18Pin Plastic Pkg	MOTA
79	MC3870	MC3870	uCT	Chip	MNX	8 Bit Single Chip Microcomputer	MOTA
80	MC3870L	MC3870	uCT	Chip	MNG	8 Bit Single Chip Microcontroller;Software Compatible with F8 Family	MOTA
81	MC3870P	MC3870	uCT	Chip	MNG	8 Bit Single Chip Microcontroller;Software Compatible with F8 Family	MOTA
82	MEX3870M	MC3870	DEV	MOD		MC3870 Devel System:Hardware Part of Emulator for Progm Devel of MC3870	MOTA
83	MC68120	MC6800	IO-13	Chip	MNG	HMOS Intelligent Peripheral Cont;2048 Bytes of ROM;8 Operating Modes	MOTA
84	MC68000	MC68000	CPU	Chip	MXX	16 Bit Microprocessor;14 Address Modes,61 Instruction Sets	MOTA
85	M6809TERMD2	MC6809	COMP	UNIT		EXORterm 220 Bundled Sys;32k Dyn RAM,CRT Ed,Macro Asmb,Linking Loader	MOTA
86	M6809TERMS2	MC6809	COMP	UNIT		Same as M6809TERMD2 Except 32k Static RAM	MOTA
87	M6809DB	MC6809	DEV	MOD		DEbug Module;EXbug 09 System Monitor Firmware (3k Bytes)	MOTA
88	M6809TERMD1	MC6809	DEV	UNIT		EXORterm 220 Dev Sys; 32k Dyn RAM,CRT Editor,Macro Asmb,Linking Loader	MOTA
89	M6809TERMS1	MC6809	DEV	UNIT		Same as M6809TERMD1 Except 32k Static RAM	MOTA
90	MC10800	M10800	CPU	Chip	BEX	4 Bit Processor Slice Used W/Microprogram Sequencer MC10801,-30 to 85°C	MOTA
91	MC10800M	M10800	CPU	Chip	BEX	4 Bit Processor Slice Used W/Microprogram Sequencer MC10801,-55 -150°C	MOTA
92	MC10801	M10800	IO-01	Chip	BEX	Microprogram Sequencer Providing Control Function For Processor MC10800	MOTA
93	MC10802	M10800	IO-01	Chip	BEX	Timing Function:Single cycle/Phase Stepping,Progm. No. of Phases	MOTA
94	MC10806	M10800	IO-01	Chip	BEX	Dual Access Stack;32x9 Bit Mem W/2 Address and Data Ports,2 Latches	MOTA
95	MC10803	M10800	IO-03	Chip	BEX	Memory Interface Function,Six 4-Bit Registers,ALU,Operand Select Logic	MOTA
96	MC10804	M10800	IO-21	Chip	BEX	4 Bit MECL/TTL Inverting Bidir. Transceiver With Latch	MOTA
97	MC10805	M10800	IO-21	Chip	BEX	5 Bit MECL/TTL Inverting Bidir. Transceiver With Latch	MOTA
98	MC10807	M10800	IO-21	Chip	BEX	5 Bit Bidirectional Bus Transceiver With Latch,-30° to 85°C	MOTA
99	MCM10143	M10800	IO-55	Chip	BEX	8 x 2 Multiport Register File	MOTA
100	MC10808	M10800	IO-90	Chip	BEX	Programmable Multi-Bit Shifter:Contains 16 Bit Shift Network	MOTA
101	MCM10149	M10800	PROM	Chip	BEX	256 x 4 PROM	MOTA
102	MCM10144F	M10800	RAM	Chip	BEX	256x1 RAM,High Speed Scratch Pad,Control,Buffer App,16Pin Flat Pkg	MOTA
103	MCM10145F	M10800	RAM	Chip	BEX	16x4 Array;Register File,Small Scratch Pad Applications,16Pin Flat Pkg	MOTA
104	MCM10146F	M10800	RAM	Chip	BEX	1024x1 RAM;High Speed Scratch Pad,Control,Cache,Buffer App,16Pin Flat Pk	MOTA
105	MCM10146L	M10800	RAM	Chip	BEX	1024x1 RAM;High Speed Scratch Pad,Control,Cache,Buffer App,16Pin Dual-In	MOTA
106	MCM10148	M10800	RAM	Chip	BEX	64 x 1 RAM	MOTA
107	MC2901AFM	M2900	CPU	Chip	BTD	4 Bit Microprocessor Slice;-55 to 125°C;Hermetic Flat Pack Pkg	MOTA
108	MC2901ALC	M2900	CPU	Chip	BTD	4 Bit Microprocessor Slice;0 to 70°C;Hermetic DIP Pkg	MOTA
109	MC2901ALM	M2900	CPU	Chip	BTD	4 Bit Microprocessor Slice;-55 to 125°C;Hermetic DIP Pkg	MOTA
110	MC2901LC	M2900	CPU	Chip	BTD	4 Bit Processor Slice Used With Microprogram Sequencer Unit MC2909	MOTA

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MC2901LM	M2900	CPU	Chip	BTD	4 Bit Processor Slice Used With Microprogram Sequencer Unit MC2909	MOTA
2	MC2903LC	M2900	CPU	Chip	BTX	4 Bit Microprocessor Slice,16 Registers,0 to 70°C,48 Pin DIP	MOTA
3	MC2903LM	M2900	CPU	Chip	BTX	4 Bit Microprocessor Slice,16 Registers,-55 to 125°C,48 Pin DIP	MOTA
4	MACE29/800	M2900	DEV	UNIT		Microcode Analyzer and Control Storage Emulator:uProgm Proc Devel Syst	MOTA
5	MC2909LC	M2900	IO-01	Chip	BTD	Microprogram Sequencer Used With Processor Unit MC 2901	MOTA
6	MC2909LM	M2900	IO-01	Chip	BTD	Microprogram Sequencer Used With Processor Unit MC 2901	MOTA
7	MC2909PC	M2900	IO-01	Chip	BTD	Microprogram Sequencer Used with Processor Unit MC2901	MOTA
8	MC2910LC	M2900	IO-01	Chip	BTX	Microprogram Controller;Address Sequencer;0 to 70°C	MOTA
9	MC2910LM	M2900	IO-01	Chip	BTX	Microprogram Controller;Address Sequencer;-55 to 125°C	MOTA
10	MC2911FM	M2900	IO-01	Chip	BTD	Microprogram Sequencer,Similar to MC2909 in 20 Pin Cer Flat Pack	MOTA
11	MC2911LC	M2900	IO-01	Chip	BTD	Microprogram Sequencer,Similar to MC2909 in 20 Pin Cer DIP	MOTA
12	MC2911LM	M2900	IO-01	Chip	BTD	Microprogram Sequencer,Similar to MC2909 in 20 Pin Cer DIP,Mil Temp	MOTA
13	MC2911PC	M2900	IO-01	Chip	BTD	Microprogram Sequencer,Similar to MC2909 in 20 Pin Plastic DIP	MOTA
14	MC2905FM	M2900	IO-21	Chip	BTD	Quad 2 Input OC Bus Transceiver W/3-State Receiver,-55° to 125°C	MOTA
15	MC2905LC	M2900	IO-21	Chip	BTD	Quad 2 Input OC Bus Transceiver W/3-State Receiver,0° to 70°C	MOTA
16	MC2905LM	M2900	IO-21	Chip	BTD	Quad 2 Input OC Bus Transceiver W/3-State Receiver,-55° to 125°C	MOTA
17	MC2905PC	M2900	IO-21	Chip	BTD	Quad 2 Input OC Bus Transceiver W/3-State Receiver, 0° to 70°C	MOTA
18	MC2906FM	M2900	IO-21	Chip	BTD	Quad 2 Input OC Bus Transceiver With Parity,-55° to 125°C	MOTA
19	MC2906LC	M2900	IO-21	Chip	BTD	Quad 2 Input OC Bus Transceiver With Parity,0° to 70°C	MOTA
20	MC2906LM	M2900	IO-21	Chip	BTD	Quad 2 Input OC Bus Transceiver With Parity,-55° to 125°C	MOTA
21	MC2906PC	M2900	IO-21	Chip	BTD	Quad 2 Input OC Bus Transceiver With Parity,0° to 70°C	MOTA
22	MC2907FM	M2900	IO-21	Chip	BTD	Quad Bus Transceiver W/3 State Receiver And Parity,-55° to 125°C	MOTA
23	MC2907LC	M2900	IO-21	Chip	BTD	Quad Bus Transceiver W/3 State Receiver And Parity,0° to 70°C	MOTA
24	MC2907LM	M2900	IO-21	Chip	BTD	Quad Bus Transceiver W/3 State Receiver and Parity,-55° to 125°C	MOTA
25	MC2907PC	M2900	IO-21	Chip	BTD	Quad Bus Transceiver W/3 State Receiver And Parity, 0° to 70°C	MOTA
26	MC2915	M2900	IO-21	Chip	BTD	4 Bit Transceiver for 3 State Bus	MOTA
27	MC2915AFM	M2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver With Interface Logic,-55° to 125°C	MOTA
28	MC2915ALC	M2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver With Interface Logic,0° to 70°C	MOTA
29	MC2915ALM	M2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver With Interface Logic,-55° to 125°C	MOTA
30	MC2915APC	M2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver With Interface Logic,0° to 70°C	MOTA
31	MC2916	M2900	IO-21	Chip	BTD	4 Bit Transceiver for 3 State Bus W/Parity Generator-Checker	MOTA
32	MC2916AFM	M2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver W/Parity Gen,Checker;-55° to 125°C	MOTA
33	MC2916ALC	M2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver W/Parity Gen,Checker;0° to 70°C	MOTA
34	MC2916ALM	M2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver W/Parity Gen,Checker;-55° to 125°C	MOTA
35	MC2916APC	M2900	IO-21	Chip	BTD	Quad 3 State Bus Transceiver W/Parity Gen,Checker;0° to 70°C	MOTA
36	MC2917	M2900	IO-21	Chip	BTD	4 Bit Transceiver;Similar to MC2916 in Space Saving 20 Pin Pkg	MOTA
37	MC2917AFM	M2900	IO-21	Chip	BTD	Quad 3 State Bus Trans.,Similar to MC 2916 in 20 Pin Pkg,-55° to 125°C	MOTA
38	MC2917ALC	M2900	IO-21	Chip	BTD	Quad 3 State Bus Trans.,Similar to MC 2916 in 20 Pin Pkg,0° to 70°C	MOTA
39	MC2917ALM	M2900	IO-21	Chip	BTD	Quad 3 State Bus Trans.,Similar to MC 2916 in 20 Pin Pkg,-55° to 125°C	MOTA
40	MC2917APC	M2900	IO-21	Chip	BTD	Quad 3 State Bus Trans.,Similar to MC 2916 in 20 Pin Pkg,0° to 70°C	MOTA
41	MC2918FM	M2900	IO-55	Chip	BTD	Quad D Register;-55° to 125°C,16 Pin Flatpack Pkg	MOTA
42	MC2918LC	M2900	IO-55	Chip	BTD	Quad D Register;0 to 70°C;16 Pin Hermetic DIP Pkg	MOTA
43	MC2918LM	M2900	IO-55	Chip	BTD	Quad D Register;-55 to 125°C;16 Pin Hermetic DIP Pkg	MOTA
44	MC2918PC	M2900	IO-55	Chip	BTD	Quad D Register;0 to 70°C;16 Pin Molded DIP Pkg	MOTA
45	MC29100LC	M2900	IO-55	Chip	BTD	16x8x48 Field Programmable Logic Assay,3 State output,0° to 70°C	MOTA
46	MC29100LM	M2900	IO-55	Chip	BTD	16x8x48 Field Programmable Logic Assay,3 State Output,-55° to 125°C	MOTA
47	MC29101LC	M2900	IO-55	Chip	BTD	16x8x48 Field Programmable Logic Assay,Open Coll Output,0° to 70°C	MOTA
48	MC29101LM	M2900	IO-55	Chip	BTD	16x8x48 Field Programmable Logic Assay,Open Coll Output,-55 to 125°C	MOTA
49	MC2902FM	M2900	IO-90	Chip	BTD	Look Ahead Carry Generator For Up To 4 MC2901 ALUs;Military-Flatpack	MOTA
50	MC2902LC	M2900	IO-90	Chip	BTD	Look Ahead Carry Generator For Up To 4 MC2901 ALUs;Commercial-Hermetic	MOTA
51	MC2902LM	M2900	IO-90	Chip	BTD	Look Ahead Carry Generator For Up To 4 MC2901 ALUs;Military-Hermetic	MOTA
52	MC2902PC	M2900	IO-90	Chip	BTD	Look Ahead Carry Generator For Up To 4 MC2901 ALUs;Commercial-Molded	MOTA
53	MCM5003AL	M2900	PROM	Chip	BTX	64x8 Static PROM;Commercial Ceramic Pkg;Open Coll Outputs	MOTA
54	MCM5004AL	M2900	PROM	Chip	BTX	64x8 Static PROM;Commercial Ceramic Pkg;Open Coll Outputs	MOTA
55	MCM5303AL	M2900	PROM	Chip	BTX	64x8 Static PROM;Military Ceramic Pkg;Open Coll Output	MOTA
56	MCM5303L	M2900	PROM	Chip	BTX	64x8 Field Programmable ROM;Military Ceramic Pkg;Open Coll Outputs	MOTA
57	MCM5304L	M2900	PROM	Chip	BTX	64x8 Field Programmable ROM;Military Ceramic Pkg;Open Coll Outputs	MOTA
58	MCM7640P	M2900	PROM	Chip	BTD	512x8 Field Programmable ROM;Open Collector Output;Plastic Pkg	MOTA
59	MCM7642L	M2900	PROM	Chip	BTD	1024x4 Field Programmable ROM;Open Collector Output;Ceramic Pkg	MOTA
60	MCM7643L	M2900	PROM	Chip	BTD	1024x4 Field Programmable ROM;Three State Output;Ceramic Pkg	MOTA
61	MCM7643P	M2900	PROM	Chip	BTD	1024x4 Field Programmable ROM;Three State Output;Ceramic Pkg	MOTA
62	MCM7660P	M2900	PROM	Chip	BTD	1024x8 Field Programmable ROM;Open Collector Output;Plastic Pkg	MOTA
63	MCM7661L	M2900	PROM	Chip	BTD	1024x8 Field Programmable ROM;Three State Output;Ceramic Pkg	MOTA
64	MCM7680L	M2900	PROM	Chip	BTD	1024x8 Field Programmable ROM;Open Collector,24 Pin Ceramic	MOTA
65	MCM7680P	M2900	PROM	Chip	BTD	1024x8 Field Programmable ROM;Open Collector,24 Pin Plastic	MOTA
66	MCM7681P	M2900	PROM	Chip	BTD	1024x8 Field Programmable ROM;3 State Output,24 Pin Plastic	MOTA
67	MCM82707L	M2900	PROM	Chip	BTD	1024x8 Field Programmable ROM;Open Collector,24 Pin Ceramic	MOTA
68	MCM82708L	M2900	PROM	Chip	BTD	1024x8 Field Programmable ROM;3 State Output,24 Pin Ceramic	MOTA
69	MCM82708P	M2900	PROM	Chip	BTD	1024x8 Field Programmable ROM;3 State Output,24 Pin Plastic	MOTA
70	MCM4064L	M2900	RAM	Chip	BTD	16x4 Static RAM;Access Time:60ns Max;Commercial Ceramic Pkg	MOTA
71	MCM4364L	M2900	RAM	Chip	BTD	16x4 Static RAM;Access Time:60ns Max;Military Ceramic Pkg	MOTA
72	MCM93415DM	M2900	RAM	Chip	BTX	1024x1 Read/Write RAM;Access Time 60ns Max;16 Pin DIP	MOTA
73	MCM93415PC	M2900	RAM	Chip	BTD	1024x1 Read/Write RAM,Access Time 35ns Typical;16 Pin Plastic	MOTA
74	MCM93425DC	M2900	RAM	Chip	BTD	1024x1 Read/Write RAM,Access Time 35ns Typical;16 Pin Ceramic	MOTA
75	MCM93425FM	M2900	RAM	Chip	BTX	1024x1 Read/Write RAM;Access Time 60ns Max;16 Pin Flat Pack	MOTA
76	MCM93425PC	M2900	RAM	Chip	BTD	1024x1 Read/Write RAM,Access Time 35ns Typical;16 Pin Plastic	MOTA
77▼	MC6801	M6800	uCT	Chip	MNG	uCT;Expanded M6800 Instr Set;Full Duplex Serial Communications Interface	MOTA
78	MC6801EL	M6800	uCT	Chip		8 Bit Single Chip Microcomputer,Ext Clock Divide by 1,SCI	MOTA
79	MC6801L	M6800	uCT	Chip		8 Bit Single Chip Microcomputer,Int Clock Divide by 4,Ser Comm Interface	MOTA
80	MC6803EL	M6800	uCT	Chip	MNG	8 Bit Microcomputer With External Clock;Expanded Instruction Set	MOTA
81	MC6803EP	M6800	uCT	Chip	MNG	8 Bit Microcomputer With External Clock;Expanded Instruction Set	MOTA
82	MC6803L	M6800	uCT	Chip	MNG	8 Bit Microcomputer With Internal Clock;Expanded Instruction Set	MOTA
83	MC6803NRL	M6800	uCT	Chip	MNG	8 Bit Microcomputer w/No RAM;40 Pin Ceramic Pkg	MOTA
84	MC6803NRP	M6800	uCT	Chip	MNG	8 Bit Microcomputer w/No RAM;40 Pin Plastic Pkg	MOTA
85	MC6803P	M6800	uCT	Chip	MNG	8 Bit Microcomputer With Internal Clock;Expanded Instruction Set	MOTA
86	MC6805L	M6800	uCT	Chip	MNG	8 Bit Microcomputer; On Chip RAM,ROM,I/O,Timer,Ceramic Pkg	MOTA
87	MC6805P2C	M6800	uCT	Chip	MNG	8 Bit Micro Computer, on Chip RAM, ROM, I/O, Timer, Cerdip Package	MOTA
88	MC6805P2L	M6800	uCT	Chip	MNG	8 Bit Micro Computer, on Chip RAM, ROM, I/O, Timer, Ceramic Package	MOTA
89	MC6805P2P	M6800	uCT	Chip	MNG	8 Bit Micro Computer, on Chip RAM, ROM, I/O, Timer, Plastic Package	MOTA
90	MC6805P	M6800	uCT	Chip	MNG	8 Bit Microcomputer; On Chip RAM,ROM,I/O,Timer,Plastic Pkg	MOTA
91▼	MC6805R2L	M6800	uCT	Chip	MNG	uCT:CPU,on Chip Clock,RAM,ROM,I/O,4 Ch 8 Bit A/D and Timer;Ceramic Pkg	MOTA
92▼	MC6805R2P	M6800	uCT	Chip	MNG	uCT:CPU,on Chip Clock,RAM,ROM,I/O,4 Ch 8 Bit A/D and Timer;Plastic Pkg	MOTA
93▼	MC6805R2S	M6800	uCT	Chip	MNG	uCT:CPU,on Chip Clock,RAM,ROM,I/O,4 Ch 8 Bit A/D and Timer;Cerdip Pkg	MOTA
94▼	MC6805U2L	M6800	uCT	Chip	MNG	uCT; CPU, on Chip Clk, RAM, ROM, I/O and Timer;Ceramic Pkg	MOTA
95▼	MC6805U2P	M6800	uCT	Chip	MNG	uCT; CPU, on Chip Clk, RAM, ROM, I/O and Timer;Plastic Pkg	MOTA
96▼	MC6805U2S	M6800	uCT	Chip	MNG	uCT; CPU, on Chip Clk, RAM, ROM, I/O and Timer;Cerdip Pkg	MOTA
97▼	MC68701	M6800	uCT	Chip	MNG	uCT;Same as MC6801MUC w/On Chip EPROM and EPROM Prog Mode;1.0MHz	MOTA
98▼	M68MM19A	M6800	uCT	MOD		uCT Module;2MHz Operation with RAM, ROM, Serial and Parallel I/O	MOTA
99	M68MM01	M6800	COMP	MOD		8 Bit Monoboard Microcomputer,Uses MC6800 MPU,MC6850 ACIA	MOTA
100	M68MM01A	M6800	COMP	MOD		8 Bit Monoboard Microcomputer,Uses MC6800 MPU,MC6850 ACIA	MOTA
101	M68MM01A2	M6800	COMP	MOD		8 Bit Monoboard Microcomputer,Same as M68MM01A,Except ROM Strap Option	MOTA
102	M68MM01B	M6800	COMP	MOD		8 Bit Monoboard Microcomputer;Uses MC6802 MPU,128 Byte RAM,1MHz Clock	MOTA
103	M68MM01B1	M6800	COMP	MOD		8 Bit Monoboard Microcomputer:Same as M68MM01B,Extra 256 Bytes RAM	MOTA
104	M68MM01B1A	M6800	COMP	MOD		Monoboard Micro Computer Module w/MC5802 MPU	MOTA
105	M68MM01D	M6800	COMP	MOD	MNG	8 Bit Monoboard Microcomputer;Uses MC 6800 MPU,6821 PIA,6850 ACIA,6840	MOTA
106	MC68A00CL	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Ceramic Pkg;Operating Freq 1.5MHz	MOTA
107	MC68A00CP	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Plastic Pkg;Operating Freq 1.5MHz	MOTA
108	MC68A00L	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Same as MC6800 With Extended Operating Freq 1.5MHz	MOTA
109	MC68A00P	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Same as MC6800 With Extended Operating Freq 1.5MHz	MOTA
110	MC68A09EL	M6800	CPU	Chip	MNG	8 Bit Microprocessor;External Clock Input 1.5MHz,Cer DIP	MOTA

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MC68A09EP	M6800	CPU	Chip	MNG	8 Bit Microprocessor;External Clock Input 1.5MHz,Plastic DIP	MOTA
2	MC68A09L	M6800	CPU	Chip	MNG	8 Bit Microprocessor;On Chip Oscillator 1.5MHz,Cer DIP	MOTA
3	MC68A09P	M6800	CPU	Chip	MNG	8 Bit Microprocessor;On Chip Oscillator 1.5MHz,Plastic DIP	MOTA
4	MC68B00L	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Same as MC6800 With Extended Operating Freq 2.0MHz	MOTA
5	MC68B00P	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Same as MC6800 With Extended Operating Freq 2.0MHz	MOTA
6	MC68B09EL	M6800	CPU	Chip	MNG	8 Bit Microprocessor;External Clock Input 2.0MHz,Cer DIP	MOTA
7	MC68B09EP	M6800	CPU	Chip	MNG	8 Bit Microprocessor;External Clock Input 2.0MHz,Plastic DIP	MOTA
8	MC68B09L	M6800	CPU	Chip	MNG	8 Bit Microprocessor;On Chip Oscillator 2.0MHz,Cer DIP	MOTA
9	MC68B09P	M6800	CPU	Chip	MNG	8 Bit Microprocessor;On Chip Oscillator 2.0MHz,Plastic DIP	MOTA
10	MC6800BQCS	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Military Temp Range;Op Freq 1.0MHz	MOTA
11	MC6800CL	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Extended Temperature Range:-40 To 85°C	MOTA
12	MC6800CP	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Plastic Pkg;Operating Freq 1.0MHz	MOTA
13	MC6800CQCS	M6800	CPU	Chip	MNG	8 Bit Microprocessor;Military Temp Range;Op Freq 1.0MHz	MOTA
14	MC6800L	M6800	CPU	Chip	MNG	8 Bit Microprocessing Unit;Ceramic Pkg;Op Freq 1.0MHz	MOTA
15	MC6800P	M6800	CPU	Chip	MNG	8 Bit Microprocessing Unit;Plastic Pkg;Op Freq 1.0MHz	MOTA
16	MC6802L	M6800	CPU	Chip	MNG	8-Bit CPU,Same as MC6800 Plus Internal Clk,Driver,128 Bytes RAM	MOTA
17	MC6802P	M6800	CPU	Chip	MNG	8-Bit CPU,Same as MC6800 Plus Internal Clk,Driver,128 Bytes RAM	MOTA
18▼	MC6803	M6800	CPU	Chip	MNG	CPU;Same as MC6801MCU without ROM;Contains: SIA, I/O Ports, Timer etc	MOTA
19	MC6808L	M6800	CPU	Chip	MNG	8 Bit Microprocessor W/clock on chip, Same Inst.Set as MC 6800,Cer Pkg	MOTA
20	MC6808P	M6800	CPU	Chip	MNG	8-Bit Microprocessor W/clock on chip,Same Inst.Set as MC6800,Plastic Pkg	MOTA
21	MC6809EL	M6800	CPU	Chip	MNG	8 Bit Microprocessor;External Clock Input 1.0MHz,Cer DIP	MOTA
22	MC6809EP	M6800	CPU	Chip	MNG	8 Bit Microprocessor;External Clock Input 1.0MHz,Plastic DIP	MOTA
23	MC6809L	M6800	CPU	Chip	MNG	8 Bit Microprocessor;On Chip Oscillator 1.0MHz,Cer DIP	MOTA
24	MC6809P	M6800	CPU	Chip	MNG	8 Bit Microprocessor;On Chip Oscillator 1.0MHz,Plastic DIP	MOTA
25▼	MC68000L4	M6800	CPU	Chip	MNG	CPU:32 Bit Data and Address Registers;16M Byte Direct Addr Range	MOTA
26▼	MC68000L6	M6800	CPU	Chip	MNG	CPU:32 Bit Data and Address Registers;16M Byte Direct Addr Range	MOTA
27▼	MC146805E2L	M6800	CPU	Chip	MCG	CPU:8 Bit Static w/RAM,I/O,and Timer;Ceramic Pkg	MOTA
28▼	MC146805E2S	M6800	CPU	Chip	MCG	CPU:8 Bit Static w/RAM,I/O,and Timer;Cerdip Pkg	MOTA
29	M68MM02	M6800	CPU	MOD	MNG	8 Bit CPU Module,Uses MC6800,1MHz Crystal Clock,Reset Circuitry,Timing	MOTA
30	M68MM19	M6800	CPU	MOD		Monoboard Microcomputer Module;128 Bytes Static RAM,PIA,PTM,ACIA	MOTA
31	M6809EXORD1	M6800	DEV			ExorciserII Development Sys. For MC6809,115V w/Dynamic Memory	MOTA
32	M6809EXORD2	M6800	DEV			Exorciser II Development Sys. for MC6809,230V W/Dynamic Memory	MOTA
33	M6809EXORS1	M6800	DEV			Exorciser II Development Sys. for MC6809,115V W/Static Memory	MOTA
34	M6809EXORS2	M6800	DEV			Exorcisor II Development Sys. for MC6809,230V W/Static Memory	MOTA
35	M6809EXORUD1	M6800	DEV			Use EXORciser II Development Sys for MC6809,115V w/Dynamic Memory	MOTA
36	M6809EXORUD2	M6800	DEV			Use EXORciser II Development Sys for MC6809,230V w/Dynamic Memory	MOTA
37	M6809EXORUS1	M6800	DEV			Use EXORciser II Development Sys for MC6809,115V w/Static Memory	MOTA
38	M6809EXORUS2	M6800	DEV			Use EXORciser II Development Sys for MC6809,230V w/Static Memory	MOTA
39	M68CIM1A	M6800	DEV	MOD		Cassette Interface Module,300bps Transmission,Part of M68ADSA1A/2A	MOTA
40	M68DIM1A	M6800	DEV	MOD		Display Interface Module;128 Character Set,Part of M68ADSA1A	MOTA
41	M68DIM2A	M6800	DEV	MOD		Display Interface Module:16 Lines of 32 Char,Part of M68ADS2A	MOTA
42	M68IFC	M6800	DEV	MOD		EXORcisor Interface Module	MOTA
43	M68KBD1	M6800	DEV	MOD		ASCII Keyboard,7 Bit ASCII Char Code,Part of M68ADSA1A/2A	MOTA
44	M68MM08	M6800	DEV	MOD		Microbug Monitor/Debug Mod:Consists of ROM and MEX6850 ACIA	MOTA
45	M68MM08A	M6800	DEV	MOD		Microbug Monitor/Debug Mod w/ROM	MOTA
46	M68SAC1	M6800	DEV	MOD		Stand Alone Computer,Part of M68ADSA1A/2A Devel System	MOTA
47	M6809PP	M6800	DEV	MOD		ERBM/PROM Programmer Module w/Software on Diskette (MDOS), 6809 Based	MOTA
48	MEK68MB5	M6800	DEV	MOD		Mother Module for use w/other expansion products	MOTA
49	MEK68R2	M6800	DEV	MOD		Programmable CRT Video Interface for MEK 6800 D2 KIT	MOTA
50	MEK68R2M	M6800	DEV	MOD		Programmable CRT Video Interface for MEK6802D3 Microcomputer	MOTA
51	MEK68RR	M6800	DEV	MOD		ROM/RAM Module Expansion Kit, Can Contain 8k RAM,64k ROM	MOTA
52	MEK68WW1	M6800	DEV	MOD		Wire Wrap Module Use w/MEK68MB,0°TO55°C,PC Board (Kit Form)	MOTA
53	MEK68WW	M6800	DEV	MOD		Wire Wrap Module Use W/MEK6800AB,0°TO55°,PC Beard (Kit Ferm)	MOTA
54	MEK6800D2C	M6800	DEV	MOD		M6800 Family Evaluation Kit 11,MPU Module Only, Kit Form	MOTA
55	MEK6800D2CAT	M6800	DEV	MOD		M6800 Family Evaluation Kit 11,MPU Module Only,Assembled	MOTA
56	MEK6800D2D	M6800	DEV	MOD		M6800 Family Evaluation Kit 11, Keyboard Module Only, Kit	MOTA
57	MEK6800D2DAT	M6800	DEV	MOD		M6800 Family Evaluation Kit 11,Keyboard Module Only,Assembled	MOTA
58▼	MEK6809D4	M6800	DEV	MOD		uCT Evaluation Board;D4Bug Monitor Firmware (4k) Expandable to 16k;DMA	MOTA
59	MEX68DB2	M6800	DEV	MOD		Debug Module;Optional Mod in M68SDT II System	MOTA
60	MEX68IC	M6800	DEV	MOD		EXORciser Input/Output Interconnecting Cable	MOTA
61	MEX68PI2	M6800	DEV	MOD		Printer Interface Module:Interfaces Devel Syst to Centronics Printer	MOTA
62	MEX68PP1A	M6800	DEV	MOD		EXORciser PROM Programmer Module With Its Software On Cassette	MOTA
63	MEX68PP1B	M6800	DEV	MOD		PROM Programmer Module With Its Software On Paper Tape	MOTA
64	MEX68PP1D	M6800	DEV	MOD		EXORciser PROM Programmer Module With Its Software On Diskette	MOTA
65	MEX68PP3M	M6800	DEV	MOD		ERBM/PROM Programmer Module w/Software on Diskette (MDOS), 6800 Based	MOTA
66	MEX68RR	M6800	DEV	MOD		EXORciser EROM/RAM Mod;16k ROM/PROM And 512 Bytes Of RAM	MOTA
67	MEX68SA2	M6800	DEV	MOD		Analyzer II for M6800 Syst Development and Troubleshooting;2MHz Version	MOTA
68	MEX68SA	M6800	DEV	MOD		Analyzer For M6800 Syst Development And Troubleshooting	MOTA
69	MEX68SPM	M6800	DEV	MOD		System Performance Monitor;Single Board Measurement Tool	MOTA
70	MEX68USE	M6800	DEV	MOD		User System Evaluator(USE)To Work With EXORciser And MEX68SA	MOTA
71	MEX68USEB	M6800	DEV	MOD		User System Evaluator B;To Work W/EXORciser and MEX68SA	MOTA
72	MEX68USM	M6800	DEV	MOD		Universal Support Module;Buffered Bi-dir Address/Data Bus	MOTA
73	MEX68WW	M6800	DEV	MOD		EXORciser Universal Wire Wrap Module	MOTA
74	MEX68XT	M6800	DEV	MOD		EXORciser Extender Module	MOTA
75	MEX6800	M6800	DEV	MOD		EXORciser MPU Module	MOTA
76	MEX6800-2	M6800	DEV	MOD		MPU II Module;Optional Mod in M68SDT II System	MOTA
77	MEX6802-46	M6800	DEV	MOD		Stand Alone Micro Computer used as Support Module for EXOR Development	MOTA
78	MEX6805SIM	M6800	DEV	MOD		Simulator Module and Macro Assembler (Diskette) for MC6805 System	MOTA
79	MEX6808-22S	M6800	DEV	MOD	MNX	8k,2.0MHZ Static RAM Mod, Uses one 8192x8 Bits Assay	MOTA
80	MEX6812-1	M6800	DEV	MOD		EXORciser 2k Static RAM Module	MOTA
81	MEX6815-1	M6800	DEV	MOD		EXORciser 8k Dynamic RAM Module	MOTA
82	MEX6815-3	M6800	DEV	MOD		EXORciser 8192x8 Dynamic RAM Module Consisting Of 16 MCM 6605 RAMs	MOTA
83	MEX6816-22S	M6800	DEV	MOD	MNX	16k,2.0MHZ Static RAM Mod, Uses two 8192x8 Bits Assay	MOTA
84	MEX6820	M6800	DEV	MOD		EXORciser Input/Output Module	MOTA
85	MEX6821-2	M6800	DEV	MOD		Input/Output Module:Four 8 Bit I/O Ports for Peripheral Interfacing	MOTA
86	MEX6845	M6800	DEV	MOD		CRT Control Support Module:Decoded/Selectable Addressing	MOTA
87	MEX6850	M6800	DEV	MOD		EXORciser Asynch Communications Interface Adapter (ACIA)	MOTA
88	MEX6850-2	M6800	DEV	MOD		ACIA/SSDA Support Module;8 or 9 Bit Transmission,Selectable Parity	MOTA
89	MEX68488	M6800	DEV	MOD		Gen Purpose Interface Adapter(GPIA) Support Module:120 Lines	MOTA
90	MEK6800D2	M6800	DEV	MODS		M6800 Family Evaluation Kit II,Two Modules Includes Keyboard And Display	MOTA
91	MEK6800D2AT	M6800	DEV	MODS		M6800 Family Evaluation Kit 11,(Assembled) Two Modules;Key Bd/Display	MOTA
92	EducatorII	M6800	DEV	UNIT		Educator Kit,On-Board Clock,128x8 RAM,Provision For Second 128x8RAM	MOTA
93	M68ADS2A	M6800	DEV	UNIT		Development System:For KB to CRT Data Input and Display	MOTA
94	M68FD3602	M6800	DEV	UNIT		EXORdisk With Two Drives	MOTA
95	M68FD3602-12	M6800	DEV	UNIT		EXORdisk For 220V,50/60 H2 Operation	MOTA
96	M68FD3602-19	M6800	DEV	UNIT		EXORdisk 19 Inch Rack Mounting Kit	MOTA
97	M68FD3602-24	M6800	DEV	UNIT		EXORdisk Cable For Expanding From 2 Drive To 4 Drive System	MOTA
98	M68MDM1	M6800	DEV	UNIT		5in CRT Display Monitor,650 Lines Hor Resl,Part of M68ADSA1A/2A	MOTA
99	M68SDTTU1	M6800	DEV	UNIT		Basic EXORciser 110V Table TOP Model With USE	MOTA
100	M68SDTTU2	M6800	DEV	UNIT		Basic EXORciser 220V Table Top Model With USE	MOTA
101	M68UCANA1	M6800	DEV	UNIT		Microcomputer Analyzer(uCA):In ckt Emulation,Signature Analysis,110 V	MOTA
102	M68UCANA2	M6800	DEV	UNIT		Microcomputer Analyzer(uCA):In ckt Emulation,Signature Analysis,220 V	MOTA
103	M68XAE6812D	M6800	DEV	UNIT		EXORciser Diskette W/EDOS,M6800 Resident Editor,M6800 Resident Assembler	MOTA
104	MEX68CTA	M6800	DEV	UNIT		EXORciser Component Tester For M6800 Components;Cassette Type Unit	MOTA
105	MEX68CTB	M6800	DEV	UNIT		EXORciser Component Tester For M6800 Components;Paper Tape Type Unit	MOTA
106	MEX68CTD	M6800	DEV	UNIT		EXORciser Component Tester For M6800 Components;Diskette Type Unit	MOTA
107	MEX68RK	M6800	DEV	UNIT		Basic EXORciser Rack Mounting Kit	MOTA
108	MEX6809-1	M6800	DEV	UNIT		MC 6809 Exorciser Support Pkg:for Exorterm 200;Uses MEX 6809 MPU/USE Mod	MOTA
109	MEX6809-2	M6800	DEV	UNIT		MC 6809 Exorciser Support Pkg:for Exorterm 220;Uses MEX 6809 MPU/USE Mod	MOTA
110	MPA-1	M6800	DEV	UNIT		Microprocessor Analyzer With Display For Hard/Software Diagnostics	MOTA

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	EducatorIIPowerSupply	M6800	DEVIO	UNIT		EducatorII Power Supply Kit,5.0±5% Volts DC Output at 1.0Amps,60Hz Clock	MOTA
2	MC68A40L	M6800	IO-01	Chip	MNG	Programmable Timer Mod,5V PS,Selectable Prescaler On Timer to 6MHz;Cer Pk	MOTA
3	MC68A40P	M6800	IO-01	Chip	MNG	Programmable Timer Mod,5V PS,Selectable Prescaler On Timer to 6MHz;Plas P	MOTA
4	MC68B40L	M6800	IO-01	Chip	MNG	Programmable Timer Mod,5V PS,Selectable Prescaler On Timer to 8MHz;Cer Pk	MOTA
5	MC68B40P	M6800	IO-01	Chip	MNG	Programmable Timer Mod,5V PS,Selectable Prescaler On Timer to 8MHz;Plas P	MOTA
6	MC6840L	M6800	IO-01	Chip	MNG	Programmable Timer Mod,5V PS,Selectable Prescaler On Timer to 4MHz;Cer Pk	MOTA
7	MC6840P	M6800	IO-01	Chip	MNG	Programmable Timer Mod,5V PS,Selectable Prescaler On Timer to 4MHz;Plas P	MOTA
8	M68MM10	M6800	IO-01	MOD		Programmable Timer Module	MOTA
9	MC6828L	M6800	IO-02	Chip	BXX	Priority Interrupt Controller Megalogic, 24 Pin Cer. Pkg	MOTA
10	MC6828P	M6800	IO-02	Chip	BXX	Priority Interrupt Controller MEGALOGIC, 24 Pin Plastic Pkg	MOTA
11	MC8507L	M6800	IO-02	Chip	BXX	Alternate Type Number to MC6828L	MOTA
12	MC8507P	M6800	IO-02	Chip	BXX	Alternate Type Number to MC6828P	MOTA
13	MC68A44L	M6800	IO-03	Chip	MNG	DMA Controller; 1.5MHz; tcyc 666ns; 40 Pin Ceramic Pkg	MOTA
14	MC68A44P	M6800	IO-03	Chip	MNG	DMA Controller;1.5 MHZ;tcyc 666ns;40 Pin Plastic Pkg	MOTA
15	MC68B44L	M6800	IO-03	Chip	MNG	DMA Controller;2.0 MHZ;tcyc 500ns;40 Pin Ceramic Pkg	MOTA
16	MC68B44P	M6800	IO-03	Chip	MNG	DMA Controller;2.0 MHZ;tcyc 500ns;40 Pin Plastic Pkg	MOTA
17	MC3480L	M6800	IO-03	Chip	BTD	Dynamic Memory Controller,Interfaces 4k/16k Dyn RAM to MPU	MOTA
18	MC3480P	M6800	IO-03	Chip	BTD	Dynamic Memory Controller,Interfaces 4k/16k Dyn RAM to MPU,Plastic Pkg	MOTA
19	MC6844L	M6800	IO-03	Chip	MNG	DMA Controller; 1.0MHz; tcyc 1.0us; 40 Pin Ceramic Pkg	MOTA
20	MC6844P	M6800	IO-03	Chip	MNG	DMA Controller; 1.0MHz; tcyc 1.0us; 40 Pin Plastic Pkg	MOTA
21	MMS68102-1	M6800	IO-03	MOD		8k 8 Non-Volatile Semiconductor Memory	MOTA
22	MMS68103-1	M6800	IO-03	MOD		Semiconductor Memory Board for M6800 Sys 8kx8	MOTA
23	M68MM11	M6800	IO-04	MOD		Micromodule 11:RS232 to TTY Adapter	MOTA
24	MC6843L	M6800	IO-07	Chip	MNG	Floppy Disk Controller,Integration Of All Key Functions,40Pin CeramicPkg	MOTA
25	MC6843P	M6800	IO-07	Chip	MNG	Floppy Disk Controller,Integration Of All Key Functions,40Pin PlasticPkg	MOTA
26	M68SFDC2	M6800	IO-07	MOD		Floppy Disk Controller Module for 6800 Based Dev Systems	MOTA
27	M68SFDC3	M6800	IO-07	MOD		Floppy Disk Controller Module for 6800 Based Development Systems	MOTA
28	M68SFDC	M6800	IO-07	MOD		Floppy Disk Controller Module(EXORciser Plug-In)	MOTA
29	M6809FDCONT3	M6800	IO-07	MOD		Floppy Disk Controller Module for 6809 Based Development Systems	MOTA
30	MEX68PI	M6800	IO-08	MOD		Printer Interface/IO Module	MOTA
31	MC6845L	M6800	IO-09	Chip	MNG	CRT Controller;Applicat Include TTY-And Lineprinter-Format Displays,Etc	MOTA
32	MC6845P	M6800	IO-09	Chip	MNG	CRT Controller;Applicat Include TTY-And Lineprinter-Format Displays,Etc	MOTA
33	MC6847L	M6800	IO-09	Chip	MNG	Video Display Generator;Generates 4 Alphanum,8 Graphic Modes,Noninterlace	MOTA
34	MC6847P	M6800	IO-09	Chip	MNG	Video Display Generator;Generates 4 Alphanum,8 Graphic Modes,Noninterlace	MOTA
35	MC6847YL	M6800	IO-09	Chip	MNG	Video Display Generator;Generates 4 Alphanum,8 Graphic Modes,Interlace	MOTA
36	MC6847YP	M6800	IO-09	Chip	MNG	Video Display Generator;Generates 4 Alphanum,8 Graphic Modes,Interlace	MOTA
37▼	M68KVAM	M6800	IO-11	MOD		VERSAbus Adapter Module:Interfaces 8 Bit EXORbus Mods and 16 Bit VERSAbus	MOTA
38▼	MC68120-1	M6800	IO-13	Chip	MNG	Intelligent Peripheral Controller;16 Bit Timer;128 Bytes Dual Ported RAM	MOTA
39▼	MC68121	M6800	IO-13	Chip	MNG	Intelligent Peripheral Controller;16 Bit Timer;128 Bytes Dual Ported RAM	MOTA
40▼	MC68121-1	M6800	IO-13	Chip	MNG	Intelligent Peripheral Controller;16 Bit Timer;128 Bytes Dual Ported RAM	MOTA
41	MC68A50L	M6800	IO-20	Chip	MNG	8-Bit Async Comm Interface Adapter;1.5MHz,24 Pin Ceramic Pkg	MOTA
42	MC68A50P	M6800	IO-20	Chip	MNG	8-Bit Async Comm Interface Adapter;1.5 MHZ, 24 Pin Plastic Pkg	MOTA
43	MC68A52CL	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Speed 1.5MHz,-40 to 85°C,Cer DIP	MOTA
44	MC68A52CP	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Speed 1.5MHz,-40 to 85°C,Plastic DIP	MOTA
45	MC68A52L	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Speed 1.5MHz,0 to 70°C,Cer DIP	MOTA
46	MC68A52P	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Speed 1.5MHz,0 to 70°C,Plastic DIP	MOTA
47	MC68A54CL	M6800	IO-20	Chip	MNG	Advanced Data Link Controller for ADCCP,HDLC,SDLC;Speed 1.5MHz	MOTA
48	MC68A54CP	M6800	IO-20	Chip	MNG	Advanced Data Link Controller for ADCCP,HDLC,SDLC;Speed 1.5MHz	MOTA
49	MC68A54L	M6800	IO-20	Chip	MNG	Advanced Data Link Controller for ADCCP,HDLC,SDLC;Speed 1.5MHz	MOTA
50	MC68A54P	M6800	IO-20	Chip	MNG	Advanced Data Link Controller for ADCCP,HDLC,SDLC;Speed 1.5MHz	MOTA
51	MC68B50L	M6800	IO-20	Chip	MNG	8-Bit Async Comm Interface Adapter;2.0MHz,24 Pin Ceramic Pkg	MOTA
52	MC68B50P	M6800	IO-20	Chip	MNG	8-Bit Async Comm Interface Adapter;2.0 MHZ,24 Pin Plastic Pkg	MOTA
53	MC68B52L	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Speed 2.0MHz,0 to 70°C,Cer DIP	MOTA
54	MC68B52P	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Speed 2.0MHz,0 to 70°C,Plastic DIP	MOTA
55	MC68B54L	M6800	IO-20	Chip	MNG	Advanced Data Link Controller for ADCCP,HDLC,SDLC;Speed 2.0MHz	MOTA
56	MC68B54P	M6800	IO-20	Chip	MNG	Advanced Data Link Controller for ADCCP,HDLC,SDLC;Speed 2.0MHz	MOTA
57	MC6850CL	M6800	IO-20	Chip	MNG	8-Bit Async Comm Interface Adapter;1.0 MHZ,Extend Temp-40 to 85°c	MOTA
58	MC6850L	M6800	IO-20	Chip	MNG	8-Bit Async Comm Interface Adapter;1.0 MHZ,24 Pin Ceramic Pkg	MOTA
59	MC6850P	M6800	IO-20	Chip	MNG	8-Bit Async Comm Interface Adapter;1.0 MHZ,24 Pin Plastic Pkg	MOTA
60	MC6852BJCS	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Speed 1.0MHz,-55 to 125°C,Mil 883B	MOTA
61	MC6852CJCS	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Speed 1.0MHz,-55 to 125°C,Mil 883C	MOTA
62	MC6852CL	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Simultaneous Xmit/Receive;Extend Temp	MOTA
63	MC6852CP	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Speed 1.0MHz,-40 to 85°C,Plastic DIP	MOTA
64	MC6852L	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Simultaneous Xmit/Receive;Ceramic Pkg	MOTA
65	MC6852P	M6800	IO-20	Chip	MNG	Synchronous Serial Data Adapter;Simultaneous Xmit/Receive;Plastic Pkg	MOTA
66	MC6854BQCS	M6800	IO-20	Chip	MNG	ADLC for ADCCP,HDLC,SDLC;Speed 1.0MHz;Mil Std 883B	MOTA
67	MC6854CL	M6800	IO-20	Chip	MNG	Advanced Data Link Controller for ADCCP,HDLC,SDLC;Speed 1.0MHz	MOTA
68	MC6854CP	M6800	IO-20	Chip	MNG	Advanced Data Link Controller for ADCCP,HDLC,SDLC;Speed 1.0MHz	MOTA
69	MC6854CQCS	M6800	IO-20	Chip	MNG	ADLC for ADCCP,HDLC,SDLC;Speed 1.0MHz;Mil Std 883C	MOTA
70	MC6854L	M6800	IO-20	Chip	MNG	Advanced Data Link Controller For ADCCP,HDLC,SDLC,40Pin Ceramic Pkg	MOTA
71	MC6854P	M6800	IO-20	Chip	MNG	Advanced Data Link Controller For ADCCP,HDLC,SDLC,40Pin Plastic Pkg	MOTA
72	MC6860CL	M6800	IO-20	Chip	MNG	0-600 Bps Digital Modem;Extended Temperature Range: -40 To 85°C	MOTA
73	MC6860L	M6800	IO-20	Chip	MNG	0-600 Bps Digital Modem,Ceramic Pkg	MOTA
74	MC6860P	M6800	IO-20	Chip	MNG	0-600 Bps Digital Modem,Plastic Pkg	MOTA
75	MC6862CL	M6800	IO-20	Chip	MNG	2400 Bps Digital Modulator;Extended Temperature Range:-40 To 85°C	MOTA
76	MC6862L	M6800	IO-20	Chip	MNG	8 Bit 2400 bps Digital Modulator,Ceramic Pkg	MOTA
77	MC6862P	M6800	IO-20	Chip	MNG	8 Bit 2400 bps Digital Modulator,Plastic Pkg	MOTA
78	M68MM07	M6800	IO-20	MOD	MNG	Quad Communications Micromodule:4 Ser Ports,21 Selectable Baud Rates	MOTA
79	MEX6854	M6800	IO-20	MOD		MC6854 Advanced Data Link Controller Support Module	MOTA
80	MC6880AL	M6800	IO-21	Chip	BTD	Quad 3-State Bus Transceiver;High Impedance Inputs,16Pin Ceramic DIP Pkg	MOTA
81	MC6880AP	M6800	IO-21	Chip	BTD	Quad 3-State Bus Transceiver;High Impedance Inputs,16Pin Plastic DIP Pkg	MOTA
82	MC6880L	M6800	IO-21	Chip	MNG	Quad 3 State Bus Transceiver With High Impedance PNP Inputs,Ceramic Pkg	MOTA
83	MC6880P	M6800	IO-21	Chip	MNG	Quad 3 State Bus Transceiver With High Impedance PNP Inputs,Plastic Pkg	MOTA
84	MC6889L	M6800	IO-21	Chip	BTD	Non-Inverting Quad 3-State Bus Transceiver,16Pin Ceramic DIP Pkg	MOTA
85	MC6889P	M6800	IO-21	Chip	BTD	Non-Inverting Quad 3-State Bus Transceiver,16Pin Plastic DIP Pkg	MOTA
86▼	MC6859L	M6800	IO-22	Chip	MNG	Data Security Device:Up to 400 KBPS Throughput Rate of 64Bit Block Cipher	MOTA
87	MC68A21L	M6800	IO-30	Chip	MNG	8 Bit Peripheral Interface Adapter;40 Pin Ceramic Package	MOTA
88	MC68A21P	M6800	IO-30	Chip	MNG	8 Bit Peripheral Interface Adapter;40 Pin Plastic Package	MOTA
89	MC68B21L	M6800	IO-30	Chip	MNG	8 Bit Peripheral Interface Adapter;40 Pin Ceramic Package	MOTA
90	MC68B21P	M6800	IO-30	Chip	MNG	8 Bit Peripheral Interface Adapter;40 Pin Plastic Package	MOTA
91	MC6820CL	M6800	IO-30	Chip	MNG	Peripheral Interface Adapter;Extended Temperature Range:-40 To 85°C	MOTA
92	MC6820L	M6800	IO-30	Chip	MNG	Peripheral Interface Adapter,Ceramic Pkg	MOTA
93	MC6820P	M6800	IO-30	Chip	MNG	Peripheral Interface Adapter,Plastic Pkg	MOTA
94	MC6821CL	M6800	IO-30	Chip	MNG	Peripheral Interface Adapter,Speed 1.0 MHz,8 Bit Data Bus,-40 to 85°C	MOTA
95	MC6821CP	M6800	IO-30	Chip	MNG	Peripheral Interface Adapter,Speed 1.0MHZ,8 Bit Data Bus,-40° to 85°C	MOTA
96	MC6821L	M6800	IO-30	Chip	MNG	Peripheral Interface Adapter,Speed 1.0MHZ,8 Bit Data Bus,0° to 70°C	MOTA
97	MC6821P	M6800	IO-30	Chip	MNG	Peripheral Interface Adapter,Speed 1.0MHZ,8 Bit Data Bus,0° to 70°C	MOTA
98	MC6881L	M6800	IO-30	Chip	BTD	Triple Bi-Directional Bus Extender/Switch,16 Pin Ceramic DIP Pkg	MOTA
99	MC6881P	M6800	IO-30	Chip	BTD	Triple Bi-Directional Bus Extender/Switch,16 Pin Plastic DIP Pkg	MOTA
100▼	MC68230	M6800	IO-30	Chip	MNG	Parallel Interface/Timer: Port Modes Inc Bit I/O;Unidir/Dir 8 and 16 Bit	MOTA
101	MC8T95L	M6800	IO-31	Chip	BTD	Alternate Type Number To MC6885L	MOTA
102	MC8T95P	M6800	IO-31	Chip	BTD	Alternate Type Number To MC6885P	MOTA
103	MC8T96L	M6800	IO-31	Chip	BTD	Alternate Type Number To MC6886L	MOTA
104	MC8T96P	M6800	IO-31	Chip	BTD	Alternate Type Number To MC6886P	MOTA
105	MC8T97L	M6800	IO-31	Chip	BTD	Alternate Type Number To MC6887L	MOTA
106	MC8T97P	M6800	IO-31	Chip	BTD	Alternate Type Number To MC6887P	MOTA
107	MC8T98L	M6800	IO-31	Chip	BTD	Alternate Type Number To MC6888L	MOTA
108	MC8T98P	M6800	IO-31	Chip	BTD	Alternate Type Number To MC6888P	MOTA
109	MC3482AL	M6800	IO-31	Chip	BTD	Alternate Type number for MC6882AL	MOTA

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MC3482AP	M6800	IO-31	Chip	BTD	Alternate Type number for MC6882AP	MOTA
2	MC3482BL	M6800	IO-31	Chip	BTD	Alternate Type number for MC6882BL	MOTA
3	MC3482BP	M6800	IO-31	Chip	BTD	Alternate Type number for MC6882BP	MOTA
4	MC6882AL	M6800	IO-31	Chip	BTD	Octal 3 Stake Buffer/Latch, tpd 8.0ns Typ, 0° to 75°C,Cer Pkg	MOTA
5	MC6882AP	M6800	IO-31	Chip	BTD	Octal 3 Stake Buffer/Latch, tpd 8.0ns Typ, 0° to 75°C,Plastic Pkg	MOTA
6	MC6882BL	M6800	IO-31	Chip	BTD	Octal 3 Stake Buffer/Latch, tpd 10ns Typ, 0° to 75°C,Cer Pkg	MOTA
7	MC6882BP	M6800	IO-31	Chip	BTD	Octal 3 Stake Buffer/Latch, tpd 10ns Typ, 0° to 75°C,Plastic Pkg	MOTA
8	MC6885L	M6800	IO-31	Chip	BTD	Hex 3 State Buffer;Non-Invert;2 Input Enable;Ceramic Pkg	MOTA
9	MC6885P	M6800	IO-31	Chip	BTD	Hex 3 State Buffer;Non-Invert;2 Input Enable;Plastic Pkg	MOTA
10	MC6886L	M6800	IO-31	Chip	BTD	Hex 3 State Buffer;Inverting;2 Input Enable;Ceramic Pkg	MOTA
11	MC6886P	M6800	IO-31	Chip	BTD	Hex 3 State Buffer;Inverting;2 Input Enable;Plastic Pkg	MOTA
12	MC6887L	M6800	IO-31	Chip	BTD	Hex 3 State Buffer;Non-Inverting;2 Single Input Enables;Ceramic Pkg	MOTA
13	MC6887P	M6800	IO-31	Chip	BTD	Hex 3 State Buffer;Non-Inverting;2 Single Input Enables;Plastic Pkg	MOTA
14	MC6888L	M6800	IO-31	Chip	BTD	Hex 3 State Buffer;Inverting;2 Single Input Enables;Ceramic Pkg	MOTA
15	MC6888P	M6800	IO-31	Chip	BTD	Hex 3 State Buffer;Inverting;2 Single Input Enables;Plastic Pkg	MOTA
16	MC6870A	M6800	IO-32	Chip	MNG	Limited Function Microprocessor Clock	MOTA
17	MC6871A	M6800	IO-32	Chip	MNG	Full Function Microprocessor Clock	MOTA
18	MC6871B	M6800	IO-32	Chip	MNG	Alternate Function Microprocessor Clock	MOTA
19▼	MC6875AL	M6800	IO-32	Chip	BTD	Two-Phase Clock Generator Driver;Ceramic Dip	MOTA
20	MC6875L	M6800	IO-32	Chip	MND	2 Phase Clock Generator/Driver;16 Pin Ceramic DIP	MOTA
21	MC6875P	M6800	IO-32	Chip	MND	2 Phase Clock Generator/Driver;16 Pin Plastic DIP	MOTA
22	MPQ6842	M6800	IO-32	Chip	MNG	MPU Clock Buffer	MOTA
23♦	MC68488L	M6800	IO-33	Chip	MNG	General Purpose Interface Adapter;Interfaces IEEE488 Bus and MC6800;Cer	MOTA
24♦	MC68488P	M6800	IO-33	Chip	MNG	General Purpose Interface Adapter;Interfaces IEEE488 Bus and MC6800;Plas	MOTA
25	M68MM03	M6800	IO-33	MOD		32/32 Input/Output Module for 8-Bit Bytes,User Selectable I/O Terminat	MOTA
26	M68MM12	M6800	IO-33	MOD		GPIB Module	MOTA
27	M68MM23	M6800	IO-33	MOD		Solid State Relay Module;Input/Output Optically Isolated	MOTA
28	M68MM05C	M6800	IO-40	MOD		Quad 12 Bit D/A Module	MOTA
29	M68MM13C	M6800	IO-40	MOD		Micromodule 13C:Digital Input(Optically Isolated);24 Input Channels	MOTA
30	M68MM13D	M6800	IO-40	MOD		Micromodule 13D:Digital Input(Optically Isolated);24cc Input Channels	MOTA
31	M68MM15C	M6800	IO-40	MOD		D/A Converter Module:4 Output Channels,Resolution 12 Bits	MOTA
32	M68MM15CI	M6800	IO-40	MOD		Micromodule 15CI:Analog Output Module,12 Bit Input,Current Output	MOTA
33	M68MM15CV	M6800	IO-40	MOD		Micromodule 15CV:Analog Output Module,12 Bit Input,Voltage Output	MOTA
34	M68MM05A	M6800	IO-41	MOD		8 Channel Differential 12 Bit A/D Module	MOTA
35	M68MM05B	M6800	IO-41	MOD		16 Channel Single Ended 12 Bit A/D Module	MOTA
36	M68MM13A	M6800	IO-41	MOD		Micromodule 13A:Digital Output(Contact Closer);16 Output Channels	MOTA
37	M68MM13B	M6800	IO-41	MOD		Micromodule 13B:Digital Output(Contact Closer);32 Output Channels	MOTA
38	M68MM15A	M6800	IO-41	MOD		A/D Converter Module:16 Diff or 32 Single Ended Channels,12 Bits	MOTA
39	M68MM15A1	M6800	IO-41	MOD		Micromodule 15A1:A/D Module,32S/16D Input Ch,12 Bit Output	MOTA
40	M68MM15B	M6800	IO-41	MOD		A/D Converter Module:1 Diff Channel,16 Bits	MOTA
41	M68MM15BEX	M6800	IO-41	MOD		Low-Level Expander Module;1 to 4 Channel	MOTA
42	MEK68MM16	M6800	IO-55	MOD		16k RAM Memory Module s/refresh for use w/MEK680203	MOTA
43	MEK68MM32	M6800	IO-55	MOD		32k RAM Memory Module w/refresh for use w/MEK6802D3	MOTA
44	MMS68100	M6800	IO-55	MOD		16k x 8 Semiconductor Memory;Access Time 475ns max	MOTA
45	MMS68102	M6800	IO-55	MOD		16k x 8Non-Volatile Semiconductor Memory for Use With EXORciser System	MOTA
46	MMS68102A	M6800	IO-55	MOD		16kx9 Non Volatile Semiconductor Memory for Use with EXORciser Syst	MOTA
47	MMS68102A-1	M6800	IO-55	MOD		8kx9 Non Volatile Semiconductor Memory for Use With EXORciser Syst	MOTA
48	MMS68103	M6800	IO-55	MOD		16k x 8Plug In Memory System For Use With MC6800 Based Systems	MOTA
49	MMS68103A	M6800	IO-55	MOD		16kx9 Plug In Memory System for Use with MC6800 Based Systems	MOTA
50	MMS68103A-1	M6800	IO-55	MOD		8kx9 Plug In Memory System for Use with MC6800 Based Systems	MOTA
51	MMS68104	M6800	IO-55	MOD		16k x 8Plug In Memory For Use With MEK6800D2 Kit	MOTA
52	MC6846L	M6800	IO-57	Chip	MNG	Combination 2048x8 ROM;8 Bit Bidirection Data I/O;16 Bit Timer-Counter	MOTA
53	MC6846P	M6800	IO-57	Chip	MNG	Combination 2048x8 ROM;8 Bit Bidirection Data I/O;16 Bit Timer-Counter	MOTA
54	IAC5	M6800	IO-92	MOD		Opto-Isolator for Industrial Signal Volt;95-130VAC In,Logic Output	MOTA
55	IAC5-A	M6800	IO-92	MOD		Opto-Isolator for Industrial Signal Volt;180-280 VAC In;3-6VDC Logic Out	MOTA
56	IDC5	M6800	IO-92	MOD		Opto-Isolator for Industrial Signal Volt;10-32VDC In,Logic Output	MOTA
57	MGD6800DSM	M6800	IO-92	MOD		Data Security Module,NMOS LSI Implementation of DES,400k bps Operation	MOTA
58	OAC5	M6800	IO-92	MOD		Opto-Isolator for Industrial Signal Volt;uP input;12-140 VAC Line Output	MOTA
59	OAC5-A	M6800	IO-92	MOD		Opto-Isolator for Industrial Signal Volt;24-280VAC Out;-3 to 6V Input	MOTA
60	ODC5	M6800	IO-92	MOD		Opto-Isolator for Industrial Signal Volt;uP input;60 VDC Max Output	MOTA
61	M68FDS3-1	M6800	PE-01	UNIT		EXORdisk III Floppy Disk Sys.,115V,60HZ For 6809 Based Systems	MOTA
62	M68FDS3-2	M6800	PE-01	UNIT		EXORdisk III Floppy Disk Sys.,230V,50HZ For 6809 Based Systems	MOTA
63	M68MODOS010	M6800	PE-01	UNIT		MODOS Floppy Disk Operating Syst;Uses 6800 MPU,16k RAM,EXORtum	MOTA
64	M68SFD1000	M6800	PE-01	UNIT		EXORdisk II-Consists of M68SFDU1000 Floppy Disk Drive,Controller,Cable	MOTA
65	M68SFD1012	M6800	PE-01	UNIT		EXORdisk II Floppy Disk System;115V,50HZ for 6800 Based System	MOTA
66	M68SFD1102	M6800	PE-01	UNIT		EXORdisk III Floppy Disk Sys.,115V,60HZ For 6800 Based Systems	MOTA
67	M68SFD1112	M6800	PE-01	UNIT		EXORdisk III Floppy Disk Sys.,115V,50HZ For 6800 Based Systems	MOTA
68	M68SFD2002	M6800	PE-01	UNIT		EXORdisk II Floppy Disk System;230V,50HZ for 6800 Based System	MOTA
69	M68SFD2102	M6800	PE-01	UNIT		EXORdisk III Floppy Disk Sys.,230V,50HZ For 6800 Based Systems	MOTA
70	M68SFD	M6800	PE-01	UNIT		EXORdisk II:Dual Drive F D Syst; 256,256 Bytes/Diskette/Soft Sector)	MOTA
71	M68SFDU1000	M6800	PE-01	UNIT		Floppy Disk Unit,110V,60Hz Option,Dual Side-By-Side Disk Drive	MOTA
72	M68SFDU1112E	M6800	PE-01	UNIT		EXORdisk III Floppy Disk Drive Expansion Sys,115V,50HZ for 6800 Systems	MOTA
73	M68SFDU2000	M6800	PE-01	UNIT		Floppy Disk Unit,220V,50Hz Option,Dual Side-By-Side Disk Drive	MOTA
74	M68SFD2000	M6800	PE-02	UNIT		EXORdiskII,220V,50Hz Option-Includes M68 SFDU,M68SFDC,M68SFDIC	MOTA
75	M68CP110-1	M6800	PE-10	UNIT		EXORprint Line Printer,110V,60Hz Option	MOTA
76	M68CP110-2	M6800	PE-10	UNIT		EXORprint Line Printer,220V,50Hz Option	MOTA
77	M68SXS220	M6800	PE-20	UNIT		EXORterm 220 Display Terminal:CRT,1920 Char Screen,7x9DM,32k RAM	MOTA
78	M68SXS	M6800	PE-20	UNIT		EXORterm 200 Display Terminal:12in CRT,1920 Char Screen,7x9 DM Options	MOTA
79	M68SXD	M6800	PE-23	UNIT		EXORterm 100 Display Terminal:12in CRT,1920 Char Screen,7x9 D Matrix	MOTA
80	M68SLP1000	M6800	PE-24	Unit		EXORprint-Consists Of M68CP110-1 EXORprint Line Printer,I/O Module,Cable	MOTA
81	M68SP702	M6800	PE-24	UNIT		Model 702:132 Col Char Impact Serial DM Printer;Speed 120cps,Option	MOTA
82	M68SP703	M6800	PE-24	UNIT		Model 703:132 Col Bidir Logic Seeking Dot Matrix Printer;Speed 180cps,Opt	MOTA
83	M68SP779	M6800	PE-24	UNIT		Model 779:Low Cost 5x7 Serial Dot Matrix Printer;Speed 60cps,Option	MOTA
84	M68SP781	M6800	PE-24	UNIT		Model 781:80 Col Char 5x7 Serial DM Printer;Speed 60cps,Option	MOTA
85	M68R680	M6800	PE-42	UNIT		EXOR Tape,High Speed Paper Tape Reader Table Top	MOTA
86	M68R680-12	M6800	PE-42	UNIT		EXOR Tape With 220V,50/60Hz Power Option	MOTA
87	M68R680-19	M6800	PE-42	UNIT		EXOR Tape 19 Inch Rack Mounting Kit	MOTA
88	PLT841	M6800	PE-60	Unit		DC Power Supply,Series Reg 3 Outputs,† 5 V/15A,± 12 V, Hold Time 8ms	MOTA
89	M68MMLC	M6800	PE-60	UNIT		Micromodule Chassis:5/10 Card Cage,Power Supply,Cooling Fan	MOTA
90	M68MMPS1	M6800	PE-60	UNIT		Power Supply Mounted on Long/Short Chassis,5 V,± 12 V	MOTA
91	PLT800	M6800	PE-60	UNIT		DC Power Supply,Series Regulated 3 Outputs,† 5 V/2A,± 9 to ± 12 V/0.3A	MOTA
92	PLT810	M6800	PE-60	UNIT		DC Power Supply,Series Regulated 3 Outputs,† 5 V/4A,± 9 to ± 12 V/0.7A	MOTA
93	PLT820	M6800	PE-60	UNIT		DC Power Supply,Series Regulated 3 Outputs,† 5 V/6A,± 9 to ± 12 V/1.0A	MOTA
94	PLT840	M6800	PE-60	UNIT		DC Power Supply,Series Regulated 3 Outputs,† 5 V/15A,± 12 V at 2.5/1.5A	MOTA
95	MCM2716L	M6800	PROM	Chip		2048x8 Ultraviolet Erasable PROM,Requires 12,5 and -5V	MOTA
96	MCM68708MTL	M6800	PROM	Chip	MNG	1024x8 Static PROM;3 State Output;24 Pin Ceramic Pkg	MOTA
97	MCM68A10CP	M6800	RAM	Chip	MNG	128x8 Static RAM;Access Time 360ns Max;Speed 1.5MHz;Plastic Pkg	MOTA
98	MCM68A10L	M6800	RAM	Chip	MNG	128x8 Static RAM;Access Time 360ns Max;Speed 1.5MHz;Cer Pkg	MOTA
99	MCM68B10L	M6800	RAM	Chip	MNG	128x8 Static RAM;Access Time 250ns Max;Speed 2.0MHz;Cer Pkg	MOTA
100	MCM68B10P	M6800	RAM	Chip	MNG	128x8 Static RAM;Access Time 250ns Max;Speed 2.0MHz;Plastic Pkg	MOTA
101	MCM2114P	M6800	RAM	Chip	MNG	1024x4 RAM;3 State Output,18 Pin Plastic Package	MOTA
102	MCM6604L2	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 375ns Min,Ceramic Pkg	MOTA
103	MCM6604L4	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 425ns Min,Ceramic Pkg	MOTA
104	MCM6604L	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 500ns Min,Ceramic Pkg	MOTA
105	MCM6604P2	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 375ns Min,Plastic Pkg	MOTA
106	MCM6604P4	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 425ns Min,Plastic Pkg	MOTA
107	MCM6604P	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 500ns Min,Plastic Pkg	MOTA
108	MCM6605AL1	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 290ns Min,Ceramic Pkg	MOTA
109	MCM6605AL	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 470ns Min,Ceramic Pkg	MOTA
110	MCM6605AP1	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 290ns Min,Plastic Pkg	MOTA

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MCM6605AP	M6800	RAM	Chip	MNG	4096 Bit Dynamic RAM;Read/Write Cycle Time 470ns Min,Plastic Pkg	MOTA
2	MCM6616L4	M6800	RAM	Chip	MNX	16,384x1 Dynamic RAM;3State TT Comp Output Access Time,250ns 16Pin Cer	MOTA
3	MCM6616L5	M6800	RAM	Chip	MNX	16,384x1 Dynamic RAM;3State TT Comp Output Access Time,300ns 16Pin Cer	MOTA
4	MCM6616P4	M6800	RAM	Chip	MNX	16,384x1 Dynamic RAM;3State TT Comp Output Access Time,250ns 16Pin Pla	MOTA
5	MCM6616P5	M6800	RAM	Chip	MNX	16,384x1 Dynamic RAM;3State TT Comp Output Access Time,300ns 16Pin Pla	MOTA
6	MCM6810ACL	M6800	RAM	Chip	MNG	128x8 Static RAM;Access Time 450nsMax;Extend Temp Range:-40 To 85°C	MOTA
7	MCM6810AL	M6800	RAM	Chip	MNG	128 x 8 Static RAM;Access Time 450ns Max,Ceramic Pkg	MOTA
8	MCM6810AP1	M6800	RAM	Chip	MNG	128 x 8 Static RAM;Access Time 350ns Max,Plastic Pkg	MOTA
9	MCM6810BJCS	M6800	RAM	Chip	MNG	128x8 Static RAM;Access Time 450ns Max;Speed 1.0MHz;Mil Std 883B	MOTA
10	MCM6810CJCS	M6800	RAM	Chip	MNG	128x8 Static RAM;Access Time 450ns Max;Speed 1.0MHz;Mil Std 883C	MOTA
11	MCM6810CP	M6800	RAM	Chip	MNG	128x8 Static RAM;Access Time 450ns Max;Speed 1.0MHz;Plastic Pkg	MOTA
12	MCM6810L	M6800	RAM	Chip	MNG	128x8 Static RAM;Access Time 450ns Max;Speed 1.0MHz;Cer Pkg	MOTA
13	M68MM06	M6800	RAM	MOD		2k Static RAM Module,2048 Bytes,User Selectable Base Address	MOTA
14	MEX6808-22	M6800	RAM	MOD	MNX	8192x8 Bit Static RAM Mod:Contains Eighteen 4096x1 Bit RAMs	MOTA
15	MEX6816-1	M6800	RAM	MOD		16,384x8-8Bits Dynamics NMOS Memory in One Array	MOTA
16	MEX6816-1HR	M6800	RAM	MOD	MNX	16384x8 Bit Dynamic Hidden Refresh RAM Module,Even Parity	MOTA
17	MEX6816-22	M6800	RAM	MOD	MNX	16384x8 Bit Static RAM Mod:Contains Thirtysix 4096x1 Bit RAMs	MOTA
18	MEX6816-22D	M6800	RAM	MOD	MXX	16384x8 Bit Dyn RAM Mod,Selectable Speed 1/1.5/2MHz,Cycle Steal Refresh	MOTA
19	MEX6832-1HR	M6800	RAM	MOD	MNX	32768x8 Bit Dynamic Hidden Refresh RAM Module,Even Parity	MOTA
20	MEX6832-22	M6800	RAM	MOD	MXX	32768x8 Bit Dyn RAM Mod,Selectable Speed 1/1.5/2MHz,Cycle Steal Refresh	MOTA
21	MEX6848-1HR	M6800	RAM	MOD	MNX	49152x8 Bit Dynamic Hidden Refresh RAM Module,Even Parity	MOTA
22	MEX6848-22	M6800	RAM	MOD	MXX	49152x8 Bit Dyn RAM Mod,Selectable Speed 1/1.5/2MHz,Cycle Steal Refresh	MOTA
23	MEX6864-1HR	M6800	RAM	MOD	MNX	65536x8 Bit Dynamic Hidden Refresh RAM Module,Even Parity	MOTA
24	MEX6864-22	M6800	RAM	MOD	MXX	65536x8 Bit Dyn RAM Mod,Selectable Speed 1/1.5/2MHz,Cycle Steal Refresh	MOTA
25	MCM68A30AC	M6800	ROM	Chip	MNG	1024x8 Static ROM,3 State Output,24 Pin Ceramic Pkg	MOTA
26	MCM68A308L	M6800	ROM	Chip	MNG	1024x8 Static ROM;3 State Output;24 Pin Ceramic Pkg	MOTA
27	MCM68A308P	M6800	ROM	Chip	MNG	1024x8 Static ROM;3 State Output;24 Pin Plastic Pkg	MOTA
28	MCM68A316AP	M6800	ROM	Chip	MNG	2048x8 Static ROM;3 State Output;24 Pin Plastic Pkg	MOTA
29	MCM68A316EC	M6800	ROM	Chip	MNG	2048x8 Bit ROM; Compatible With 2708 PROM; 0° to 70°C;Ceramic Pkg	MOTA
30	MCM68A332C	M6800	ROM	Chip	MNG	4096x8 Static ROM; 3 State Output; 24 Pin Ceramic Pkg	MOTA
31	MCM68A332P	M6800	ROM	Chip	MNG	4096x8 Static ROM;3 State Output;24 Pin Plastic Pkg	MOTA
32	MCM68A364P	M6800	ROM	Chip	MNG	8192x8 Static ROM; 3 State Output; tac 350ns Max;Plastic Pkg	MOTA
33	MCM68B308L	M6800	ROM	Chip	MNG	1024x8 Static ROM;3 State Output;24 Pin Ceramic Pkg	MOTA
34	MCM68B364C	M6800	ROM	Chip	MNG	8192x8 Static ROM; 3 State Output; tac 250ns Max;Cer Pkg	MOTA
35	MCM68B364P	M6800	ROM	Chip	MNG	8192x8 Static ROM; 3 State Output; tac 250ns Max;Plastic Pkg	MOTA
36	MCM6830AL	M6800	ROM	Chip	MNG	1024 x 8 Static ROM;Ceramic Pkg	MOTA
37	MCM6832C	M6800	ROM	Chip	MNG	2048x8 Mask Programmable ROM; Ceramic Pkg	MOTA
38	MCM6832P	M6800	ROM	Chip	MNG	2048 x 8 Mask-Programmable ROM;Plastic Pkg	MOTA
39	MCM65308P	M6800	ROM	Chip	MNG	1024x8 Binary Addressable ROM;Compatible With 2708 PROM;Plastic Pkg	MOTA
40	MCM65317L	M6800	ROM	Chip	MNG	2048x8 Bit ROM;Compatible With 2708 PROM;Ceramic Pkg	MOTA
41	MCM65317P	M6800	ROM	Chip	MNG	2048x8 Bit ROM;Compatible With 2708 PROM;Plastic Pkg	MOTA
42	MCM68308P	M6800	ROM	Chip	MNG	1024 x 8 Mask-Programmable ROM;Plastic Pkg	MOTA
43	MCM68316E1L	M6800	ROM	Chip	MNG	2048x8 Bit ROM;Compatible With 2708 PROM;-40 To 85°C;Ceramic Pkg	MOTA
44	MCM68316EL	M6800	ROM	Chip	MNG	2048x8 Bit ROM;Compatible With 2708 PROM;0 To 70°C;Ceramic Pkg	MOTA
45	MCM68317L	M6800	ROM	Chip	MNG	2048 x 8 Static ROM;3 State Outputs,Ceramic Pkg	MOTA
46	MCM68332L	M6800	ROM	Chip	MNG	4096x8 Static ROM;3 State Output;24 Pin Ceramic Pkg	MOTA
47	MCM68332P	M6800	ROM	Chip	MNG	4096x8 Static ROM;3 State Output;24 Pin Plastic Pkg	MOTA
48	TMS27A16L	M6800	ROM	Chip	MNG	2048x8 UV Erasable PROM;Access Time 300ns Max	MOTA
49	TMS2716L	M6800	ROM	Chip	MNG	2048x8 UV Erasable PROM;Access Time 450ns Max	MOTA
50	M68MM04	M6800	ROM	MOD		8k EROM/ROM Module,8 Sockets for Mounting MCM68708 or 68308	MOTA
51	M68MM04-1	M6800	ROM	MOD		16k EROM/ROM Module,16 Sockets for Mounting MCM68708 or 68308	MOTA
52▼	MC68A29L	M6800/09	IO-23	Chip	MNG	Memory Management Unit:Expands Addr Space of MC6809 from 64k Bytes to 2M	MOTA
53▼	MC68A29P	M6800/09	IO-23	Chip	MNG	Memory Management Unit:Expands Addr Space of MC6809 from 64k Bytes to 2M	MOTA
54▼	MC68B29L	M6800/09	IO-23	Chip	MNG	Memory Management Unit:Expands Addr Space of MC6809 from 64k Bytes to 2M	MOTA
55▼	MC68B29P	M6800/09	IO-23	Chip	MNG	Memory Management Unit:Expands Addr Space of MC6809 from 64k Bytes to 2M	MOTA
56▼	MC6829L	M6800/09	IO-23	Chip	MNG	Memory Management Unit:Expands Addr Space of MC6809 from 64k Bytes to 2M	MOTA
57▼	MC6829P	M6800/09	IO-23	Chip	MNG	Memory Management Unit:Expands Addr Space of MC6809 from 64k Bytes to 2M	MOTA
58	M6800B	M6800B	DEV	UNIT		Evaluation Module For Hardware And Program Development	MOTA
59▼	M68451	M68000	IO-03	Chip	MNG	Memory Management Unit:Supports Multi-user,Multi-tasking Oper;DMA Compat	MOTA
60	M6809FDCONT2	M6809	IO-07	MOD		Floppy Disk Controller Module for 6809 Based Dev Systems	MOTA
61	M6809FDS2-1	M6809	PE-01	UNIT		EXORdisk II Floppy Disk,115V,60HZ for 6809 Based Dev Systems	MOTA
62	M6809FDS2-2	M6809	PE-01	UNIT		EXORdisk II Floppy Disk,230V,60HZ for 6809 Based Dev Systems	MOTA
63	M6809FDS2-3	M6809	PE-01	UNIT		EXORdisk II Floppy Disk,115V,50HZ for 6809 based Dev Systems	MOTA
64▼	MMS1119N3064	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:64k Word Capacity;No Parity	MOTA
65▼	MMS1119N3096	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:96k Word Capacity;No Parity	MOTA
66▼	MMS1119N3128	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:128k Word Capacity;No Parity	MOTA
67▼	MMS1119N3256	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:256k Word Capacity;No Parity	MOTA
68▼	MMS1119N3512	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:512k Word Capacity;No Parity	MOTA
69▼	MMS1119N4064	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:64k Word Capacity;No Parity	MOTA
70▼	MMS1119N4096	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:96k Word Capacity;No Parity	MOTA
71▼	MMS1119N4128	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:128k Word Capacity;No Parity	MOTA
72▼	MMS1119N4256	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:256k Word Capacity;No Parity	MOTA
73▼	MMS1119N4512	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:512k Word Capacity;No Parity	MOTA
74▼	MMS1119P3064	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:64k Word Cap;Parity and Controller	MOTA
75▼	MMS1119P3096	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:96k Word Cap;Parity and Controller	MOTA
76▼	MMS1119P3128	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:128k Word Cap;Parity and Controller	MOTA
77▼	MMS1119P3256	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:256k Word Cap;Parity and Controller	MOTA
78▼	MMS1119P3512	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:512k Word Cap;Parity and Controller	MOTA
79▼	MMS1119P4064	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:64k Word Cap;Parity and Controller	MOTA
80▼	MMS1119P4096	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:96k Word Cap;Parity and Controller	MOTA
81▼	MMS1119P4128	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:128K Word Cap;Parity and Controller	MOTA
82▼	MMS1119P4256	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:256k Word Cap;Parity and Controller	MOTA
83▼	MMS1119P4512	PDP11	IO-57	MOD		Extended Unibus Compatible Mem Sys:512k Word Cap;Parity and Controller	MOTA
84	MMS1600-16	S1600	IO-57	MOD		16kx16 Semiconductor Memory For SPL/110,SPL/220 Computers	MOTA
85	MMS1600-16P	S1600	IO-57	MOD		16kx18 Semiconductor Memory For SPL/110,SPL/220 Computers	MOTA
86	MMS1600-32	S1600	IO-57	MOD		32kx16 Semiconductor Memory For SPL/110,SPL/220 Computers	MOTA
87	MMS1600-32P	S1600	IO-57	MOD		32kx18 Semiconductor Memory For SPL/110,SPL/220 Computers	MOTA
88▼	MMS780AE1032	VAX-11/780	IO-57	MOD		Memory Array Card;32k Words (256k Bytes) Using 16k RAM Chips	MOTA
89	MSC4501-LSI11	LSI11	RAM	MOD	MNG	16k W Add-On Mem;Quad Slot Compatible W/DEC LSI11 Or PDP 11/03 Syst	MSCC
90	MSC4503-LSI11DH	LSI11	RAM	MOD	MNG	4/8k W Add-On Mem;Dual Ht Board Compatible W/DEC LSI11 Or PDP 11/03 Syst	MSCC
91	MSC4601-LSI11DH	LSI11	RAM	MOD	MNG	16/32kW Add-On Mem;Dual Ht Board Compatible W/DEC LSI11 Or PDP 11/03 Syst	MSCC
92	MSC8001-Z80	MSC8001-Z80	COMP	MOD		8 Bit Computer on a Card;Uses Z80 CPU;78 Instructions	MSCC
93	MSC-MTS	MSC8001-Z80	DEV	UNIT		Multibus Test Station:For Production,Design,QC and Service	MSCC
94	MSC8101	MSC8001-Z80	IO-07	MOD		Floppy Disk Interface/Controller:Compatible W/Shugart SA800,SA400	MSCC
95	MSC8103	MSC8001-Z80	IO-57	MOD		Multibus I/O and Mem Mod:Up to 8k RAM,16k ROM/EPROM,48 I/O Lines	MSCC
96	MSC8202	MSC8001-Z80	PE-60	UNIT		Multibus Power Supply:±12V and ±5V DC Output	MSCC
97	MSC8206	MSC8001-Z80	PE-60	UNIT		Disk Support Power Source:Supports Two Disk Drives	MSCC
98	MSC4502-SBC80	MSC8001-Z80	RAM	MOD	MNG	16k W Add-On Mem;Compatible With All SBC80 Bus Systems	MSCC
99	MSC4602-SBC80	MSC8001-Z80	RAM	MOD	MNG	64k W Add-On Mem;Compatible With All SBC80 Bus Systems	MSCC
100	MSC2101#1	MS8001-Z80	RAM	MOD	MNG	1024 x 1 to 4k x 8 Static RAM on a Card;Cycle Time 1.0us	MSCC
101	MSC2101#2	MS8001-Z80	RAM	MOD	MNG	1024 x 1 to 4k x 8 Static RAM on a Card;Cycle Time 750ns	MSCC
102	MSC2101#3	MS8001-Z80	RAM	MOD	MNG	1024 x 1 to 4k x 8 Static RAM on a Card;Cycle Time 475ns	MSCC
103	MSC2101#4	MS8001-Z80	RAM	MOD	MNG	1024 x 1 to 4k x 8 Static RAM on a Card;Cycle Time 350ns	MSCC
104	MSC2101#5	MS8001-Z80	RAM	MOD	MNG	1024 x 1 to 4k x 8 Static RAM on a Card;Cycle Time 250ns	MSCC
105	MSC4201	MS8001-Z80	RAM	MOD	MCX	1024 x 8 to 4k x 8 Static RAM on a Card;Non Volatile	MSCC
106	MSC4301	MS8001-Z80	RAM	MOD	MNG	4096x1 to 32kx8 Dynamic RAM on a Card;Access Time 450ns,Cycle Time 600ns	MSCC
107	MSC2401-U3000	3000	RAM	MOD	MNG	64kx8,9 Or 32kx16,18W RAM;Compatible With Micro 3000 Bus	MSCC
108	uSA	MCS80,M6800	DEV	UNIT		Microsystem Analyzer:For Diagnosis,Emulation,Maint;Dual Processor Arch	MSS
109	MCS6502	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor;Addressable Mem 65k;On Chip Clock;40 Pin Pkg	MTY
110	MCS6503	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor;Addressable Mem 4.0k;On Chip Clock;28 Pin Pkg	MTY

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	MCS6504	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor;Addressable Mem 8.0k;On Chip Clock;28 Pin Pkg	MTY
2	MCS6505	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor;Addressable Mem 4.0k;On Chip Clock;28 Pin Pkg	MTY
3	MCS6506	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor;Addressable Mem 4.0k;On Chip Clock;28 Pin Pkg	MTY
4	MCS6507	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor,Addressable Mem 8.0k;On Chip Clock;28 Pin Pkg	MTY
5	MCS6512	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor;Addressable Mem 65k;Ext Clock;40 Pin Pkg	MTY
6	MCS6513	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor;Addressable Mem 4.0k;Ext Clock;28 Pin Pkg	MTY
7	MCS6514	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor;Addressable Mem 8.0k;Ext Clock;28 Pin Pkg	MTY
8	MCS6515	MCS6500	CPU	Chip	MNG	8 Bit Microprocessor;Addressable Mem 4.0k;Ext Clock;28 Pin Pkg	MTY
9	MCS6560	MCS6500	IO-09	Chip	MNG	Video Interface Controller,Microprocessor Interface Chip	MTY
10	MCS6520	MCS6500	IO-30	Chip		Peripheral Interface Adapter	MTY
11	MCS6522	MCS6500	IO-30	Chip		Peripheral Interface Adapter;Reg For Serial Operation	MTY
12	MCS6530	MCS6500	IO-57	Chip	MNG	Memory,I/O,Timer Array;Single Chip;RAM,ROM,I/O,Timer,40 Pin Pkg	MTY
13	MCS6532	MCS6500	IO-57	Chip	MNG	Mem,I/O,Timer Array;Single Chip;128x8 RAM	MTY
14	MCS2316	MCS6500	ROM	MOD		2048 x 8 Static ROM;Cer Pkg;Asynchronous Oper;TTL Compatible;3 Prog Chips	MTY
15	MCS2332	MCS6500	ROM	MOD		4096 x 8 Static ROM;Cer Pkg;Asynchronous Oper;TTL Compatible;2 Prog Chips	MTY
16	MPS2316	MCS6500	ROM	MOD		2048 x 8 Static ROM;Mld Pkg;Asynchromous Oper;TTL Compatible;3 Prog Chips	MTY
17	MPS2332	MCS6500	ROM	MOD		4096 x 8 Static ROM;Mld Pkg;Asynchromous Oper;TTL Compatible;2 Prog Chips	MTY
18	MPS7600-001	MPS7600	GAME	Chip	MPI	Video Game Array;3 Ball Games,Target,Digital Scoring,3 Sounds	MTY
19	MPS7600-002	MPS7600	GAME	Chip	MPI	Video Game Array:3 Games;Target,Race car,Tennis,Differently Progm from001	MTY
20	MPS7600-004	MPS7600	GAME	Chip	MPI	Video Game Array:2 Games,Pinball,Target,Differently Progm from 001/002	MTY
21	MPS7600-005	MPS7600	GAME	Chip	MPI	Video Game Array:3 Games,Sea Battle,Catch/Reshoot,Space Target,Diff Progm	MTY
22	MPS7601-001	MPS7600	GAME	Chip	MPI	Video Game Array:For 625 Line BW/PAL Std;4 Games,3 Speed/Sound,Dig Scor	MTY
23	MPS7601-002	MPS7600	GAME	Chip	MPI	Video Game Array:For 625 Line BW/PAL Std;3 Games,3 Speed/Sound,Dig Scor	MTY
24	MPS7601-004	MPS7600	GAME	Chip	MPI	Video Game Array:For 625 Line BW/PAL Std;2 Games,3 Speed/Sound,Dig Scor	MTY
25	MPS7601-005	MPS7600	GAME	Chip	MPI	Video Game Array:For 625 L;3 Games,Submarine,C/R,Target,3 Speed/Sound	MTY
26	MS801	800 Series	COMP	UNIT	MCX	8 Bit System Uses Intel 8008	MUL
27	MS808A	800 Series	COMP	UNIT		8 Bit System Uses Intel 8080A MPU	MUL
28	CPU808A	800 SERIES	CPU	MOD	MCX	8080A CPU;Up To 4RS232cPorts 48B Parallel IORTC,8 Interrupts	MUL
29	DB808A	800 SERIES	DEV	MOD	MCX	Hardware Debug Card	MUL
30	DMA808A	800 SERIES	IO-03	MOD	MCX	Multiple Processor DMA Card;Up To 32 SCPUS From One Master	MUL
31	PI808A	800 SERIES	IO-30	MOD	MCX	Peripheral Interface Card;Floppy Disk,Hi Speed Reader,Printer,Punch	MUL
32	I/O808A	800 SERIES	IO-33	MOD	MCX	General Purpose I/O Card;96 Bits(12 Ports) Software Programmable	MUL
33	PRM808A	800 SERIES	IO-55	MOD	MCX	12K And 4.0k PROM/RAM Card; Uses 2708 PROMs;16k Max Per Card	MUL
34	MEM808A	800 SERIES	RAM	MOD	MCX	16K Static RAM Card;Uses 2102 RAMs;128 Chips Per Card Max	MUL
35	MP808A	800 SERIES	RAM	MOD	MCX	Ninth Bit Memory Parity Card;To 64k Uses 2102 RAMS,64 Per Card Max	MUL
36	PM808A	800 SERIES	ROM	MOD	MCX	16k PROM Memory Card;Uses 2708 PROM,16k Max Per Card	MUL
37	muPRO80	muPRO80	COMP	UNIT	MNG	Complete Comp Incl 16k RAM,2 Parall,2 Serial I/O;8 Slot Expansion Increm	MUP
38	muPRO80-010	muPRO80	CPU	MOD	MNG	CPU Card W/8080A;Optional 8080A-1,8080A-2 W/400ns,350ns,.01% Acc Clock	MUP
39	muPRO80DS	muPRO80	DEV	UNIT		Microprocessor Devel Syst;Disk Based Multi User System for 8080/85	MUP
40	muPRO80E	muPRO80	DEV	UNIT		In-Circuit Emulator for 8080A;Incl Control/Display Console;Power Supply	MUP
41	muPRO80ED	muPRO80	DEV	UNIT		Emulator with Added Mem and I/O Cards;Incl BSAL-80 Software Pkgs	MUP
42	muPRO80P-2708	muPRO80	DEV	UNIT		PROM Programmer Used with muPRO80 for On-Card Progr of Up to 8 2708 PROMs	MUP
43	muPRO80-023	muPRO80	IO-03	MOD		RAM Refresh Card;Provides 1.0 or 2.0ms Refresh for Up to 64k Dynamic RAM	MUP
44	muPRO80-060	muPRO80	IO-07	MOD		Disk Controller Card for Up to 4 Drives;Compatible with IBM 3740	MUP
45	muPRO80-040	muPRO80	IO-20	MOD		Perpheral Interface;2 8-Bit Parallel,2 Serial Ports;RS232C or 20ma Loop	MUP
46	muPRO80-041	muPRO80	IO-30	MOD		Quad Parallel Interface;Uses 2 Type 8255 Prog I/O;2 8-Bit Bi-Dir Ports	MUP
47	muPRO80-050	muPRO80	IO-41	MOD		Data Acq Card;16 Single-Ended or 8 Diff Chan;12 Bit;40us Conversion	MUP
48	muPRO80-024-00	muPRO80	IO-55	MOD		Mem Card for Up to 4k PROM,1k Static RAM in 1k PROM,256 Byte RAM Increm	MUP
49	muPRO80-024-10	muPRO80	IO-55	MOD		Mem Card for Up to 4k PROM,4k Static RAM in 1k PROM,1k Bytes RAM Increm	MUP
50	muPRO80D-1	muPRO80	PE-02	UNIT		Disk Sys with Multi-User Task Executive Software;Incl 80-060 Controller	MUP
51	muPRO80D-2	muPRO80	PE-02	UNIT		Dual Disk Drive in Cabinet;Incl Power Supply;No Controller or Software	MUP
52	muPRO80R	muPRO80	PE-42	UNIT		Paper Tape Reader;Incl 8-Bit Parallel Interface;300 Characters/Sec	MUP
53	muPRO80-021	muPRO80	PROM	MOD		PROM Card for Up to 8 Type 2708 1k Chips;On-Card Progr W/80P-2708 Unit	MUP
54	muPRO80-023-01	muPRO80	RAM	MOD		8kx8 Dyn RAM;220ns Access,450ns Cycle;Auto Refresh by 80-023 Card	MUP
55	muPRO80-023-02	muPRO80	RAM	MOD		4kx8 Dyn RAM;220ns Access,450ns Cycle;Auto Refresh by 80-023 Card	MUP
56	MBC004	muPRO80	RAM	MOD		4kx8 Error Corr Dyn RAM Using 4k Bit RAMS;330ns Access,450ns Cycle Time	MUP
57	MBC008	muPRO80	RAM	MOD		8kx8 Error Corr Dyn RAM Using 4k Bit RAMS;330ns Access,450ns Cycle Time	MUP
58	MBC012	muPRO80	RAM	MOD		12kx8 Error Corr Dyn RAM Using 4k Bit RAMS;330ns Access,450ns Cycle Time	MUP
59	MBC016	muPRO80	RAM	MOD		16kx8 Error Corr Dyn RAM Using 4k Bit RAMS;330ns Access,450ns Cycle Time	MUP
60	MBC032	muPRO80	RAM	MOD		32kx8 Error Corr Dyn RAM Using 16k Bit RAMS;330ns Access,450ns Cycle Time	MUP
61	MBC048	muPRO80	RAM	MOD		48kx8 Error Corr Dyn RAM Using 16k Bit RAMS;330ns Access,450ns Cycle Time	MUP
62	MBC064	muPRO80	RAM	MOD		64kx8 Error Corr Dyn RAM Using 16k Bit RAMS;330ns Access,450ns Cycle Time	MUP
63	MBC116	muPRO80	RAM	MOD		16kx8 Error Corr Dyn RAM Using 16k Bit RAMS;330ns Access,450ns Cycle Time	MUP
64	MK3887P-10	Z80-MOS	IO-20	Chip	MNG	Same as MK3887N-10 Except CeraMOS as MK3887N-10 Except Cera	N
65	MK3881N-4	Z80-MOS	IO-30	Chip	MNG	Same as MK3881N Except Max CloMOS as MK3881N Except Max Clo	N
66#	NASCOMI	NASCOMI	COMP	MOD	MNG	8 Bit Microcomputer:Z80 Based Home Comp W/KB,Video,Cassette Interfaces	NASB
67#	NASCOMI-DISC	NASCOMI	IO-07	MODS		Floppy Disk Drive and Control Card	NASB
68#	NASCOMI-IO	NASCOMI	IO-30	MOD		6x8 Bit Parallel I/O,Serial I/O,4 Channel Counter Timer	NASB
69#	NASCOMI-BUF	NASCOMI	IO-31	MOD	BTD	Buffer Module:Buffers NASCOMI to 77 Way NASBUS	NASB
70#	NASCOMI-MEM	NASCOMI	IO-57	MOD		Mem Module:Up to 32k Dynamic RAM,4k EPROM	NASB
71#	uPD545C	uCOM-4	uCT	Chip	MPX	Single Component 4 Bit Microcomputer;RAM/ROM 96/2k;72 Instructions	NECD
72#	TK80	uCOM-8	COMP	MOD	MNG	Single Board Microcomputer For Learning uPD8080A Microcomputer System	NECD
73#	uPD371D	uCOM-8	IO-05	Chip	MXX	Cassette MT Controller:To Read/Write,Control Mag Tape Motion	NECD
74#	uPD379C	uCOM-8	IO-20	Chip	MNX	Synchronous Receiver/Transmitter:Full or Half Duplex Operation	NECD
75#	uPD463D	uCOM-8	PROM	Chip	MNG	2048 Bit Mask Programmable ROM,512 Word x4 Bit Or 256 Word x8 Bit	NECD
76#	uPD755D	uCOM-16	CPU	Chip	MNX	Register And ALU Chip,16 Bit,Pd 500mW,42 Pin DIPkg	NECJ
77#	uPD756D00	uCOM-16	IO-01	Chip	MNX	Control Chip, 16 Bit, Pd 500mW, 42 Pin DI Pkg	NECJ
78#	uCOM-4	uCOM-4	COMP	CHS	MNX	4 Bit Microcomputer System Using NEC uPD751D CPU	NECJ
79#	uPD547LC	uCOM-4	CPU	Chip	MPX	Complete Comp Chip of uCOM-44 Single Chip System;42 Pin Plastic Pkg	NECJ
80#	EVAKIT-41	uCOM-4	DEV	MOD		uCOM-41 Designer Evaluation Kit,COMP On A Board	NECJ
81#	EVAKIT-42	uCOM-4	DEV	MOD		uCOM-42 Designer Evaluation Kit,COMP On A Board	NECJ
82#	EVAKIT-43	uCOM-4	DEV	MOD		uCOM-43,44,45 Designer Evaluation Kit,COMP On A Board	NECJ
83#	uPD549C	uCOM-4	IO-09	Chip	MPX	Decoder/Display Driver	NECJ
84#	uPD757C	uCOM-4	IO-10	Chip	MNX	Keyboard And Display Controller	NECJ
85#	uPD5101LC	uCOM-4	RAM	Chip	MCX	256x4 RAM,Access Time 650ns Max	NECJ
86#	uPD5101LC-1	uCOM-4	RAM	Chip	MCX	256x4 RAM,Access Time 450ns Max	NECJ
87#	uPD764C	uCOM-4,41	IO-08	Chip	MNX	Printer Controller	NECJ
88#	uPD554C	uCOM-4,45	uCT	Chip	MPX	4 Bit Single Chip Comp of uCOM-45;Gen Purpose Controller;1kx8 ROM	NECJ
89#	uPD554LC	uCOM-4,45	uCT	Chip	MPX	4 Bit Single Chip Comp of uCOM-45;Gen Purpose Controller;1k x 8 ROM	NECJ
90#	uCOM-41	uCOM-41	COMP	CHS	MPX	4 Bit Microcomputer System Using NEC uPD541D CPU	NECJ
91#	uPD541C	uCOM-41	CPU	Chip	MPX	4 Bit CPU	NECJ
92#	uPD762C	uCOM-41	IO-33	Chip	MNX	Interface Chip	NECJ
93#	uPD542C	uCOM-41	IO-55	Chip	MPX	2kx8 ROM,128x4 RAM	NECJ
94#	uPD543C	uCOM-41	IO-57	Chip	MPX	ROM And Programmable I/O Port	NECJ
95#	uPD548C	uCOM-42	uCT	Chip	MPX	Complete Comp Chip Of uCOM-42 Single Chip System;42 Pin Plastic Pkg	NECJ
96#	uPD555D	uCOM-42	DEV	Chip	MPX	Evaluation Chip Of EVAKIT-42;64 Pin Ceramic Pkg	NECJ
97#	uPD546C	uCOM-43	uCT	Chip	MPX	Complete Comp Chip Of uCOM-43 Single Chip System;42 Pin Plastic Pkg	NECJ
98#	uPD556D	uCOM-43	DEV	Chip	MPX	Evaluation Chip Of EVAKIT-43;64 Pin Ceramic Pkg	NECJ
99#	uPD547C	uCOM-44	uCT	Chip	MPX	Complete Comp Chip Of uCOM-44 Single Chip System;42 Pin Plastic Pkg	NECJ
100#	uPD550LC	uCOM-45	uCT	Chip	MPX	4 Bit Single Chip Comp of uCOM-45;Gen Purpose Controller;640 x 8 ROM	NECJ
101#	uPD766G	uCOM-47	uCT	Chip	MNX	4 Bit uCT Chip;32x4 RAM,4000x10 ROM,I/O,ALU	NECJ
102#	uPD8035LC	uCOM-8	uCT	Chip	MNX	uPD8048C/D Except fpr 1024 X 8-Bit Internal ROM;Req Ext Program	NECJ
103	uPD8048C	uCOM-8	uCT	Chip	MNX	8-Bit Single Chip Comp;64x8 RAM;1kx8 ROM;27 I/O Lines;Plastic Package	NECJ
104#	uPD780C	uCOM-8	CPU	Chip	MNI	8-Bit Microprocessor,Z80 Compatible,Cl Period 400ns min;40-Pin Plas DIL	NECJ
105#	uPD780C-1	uCOM-8	CPU	Chip	MNI	8-Bit Microprocessor,Z80A Compatible,Cl period 250ns Min;40-Pin Plas DIL	NECJ
106#	uPD780D	uCOM-8	CPU	Chip	MNI	8-Bit Microprocessor,Z80 Compatible,Cl Period 400ns min;40-Pin Cer DIL	NECJ
107#	uPD780D-1	uCOM-8	CPU	Chip	MNI	8-Bit Microprocessor,Z80A Compatible,Cl period 250ns Min;40-Pin Cer DIL	NECJ
108#	uPB8214C	uCOM-8	IO-02	Chip		Priority Interrupt Controller	NECJ
109#	uPB8228C	uCOM-8	IO-02	Chip	BTX	8080A System Controller and Bus Driver for Small Mem Syst	NECJ
110#	uPB8238C	uCOM-8	IO-02	Chip	BTX	8080A System Controller and Bus Driver for Large Mem Syst	NECJ

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE
1#	uPD8259C-5	uCOM-8	IO-02	Chip	MNX	Programmable Interrupt Controller;8 Level Expandable to 64 Levels	NECJ
2#	uPD8257C-5	uCOM-8	IO-03	Chip	MNX	Programmable DMA Controller;4 Chan Expandable;Used with uPD8212 I/O	NECJ
3#	uPD369C	uCOM-8	IO-20	Chip	MNX	Universal Asynchronous Receiver Transmitter	NECJ
4#	uPD8251C	uCOM-8	IO-20	Chip	MNX	Programmable Communication Interface:USART	NECJ
5#	uPD8255C	uCOM-8	IO-30	Chip	MXX	Programmable Peripheral Interface,40 Pin Pkg	NECJ
6#	uPD752C	uCOM-8	IO-33	Chip	MNX	8 Bit I/O Port;Plastic Package	NECJ
7#	uPD752D	uCOM-8	IO-33	Chip	MNX	8 Bit I/O Port;Ceramic Package	NECJ
8#	uPD8355D	uCOM-8	IO-57	Chip	MNX	Combination 2kx8 ROM,Two 8-Bit I/O Ports;Access Time 400ns	NECJ
9#	uPB405D	uCOM-8	PROM	Chip	BTX	512x8 EPROM;Access Time 40ns Typ;Open Collector Output	NECJ
10	uPB406D	uCOM-8	PROM	Chip		1024x4 PROM;Access Time 50ns Typ;Open Collector	NECJ
11#	uPB425D	uCOM-8	PROM	Chip	BTX	512x8 EPROM;Access Time 40ns Typ;Tri State Output	NECJ
12#	uPB426D	uCOM-8	PROM	Chip		1024x4 PROM;Access Time 50ns Typ;Tri State	NECJ
13#	uPD466C	uCOM-8	PROM	Chip	MNG	2048x8 Static PROM;Access Time 475ns Max;Plastic Pkg	NECJ
14#	uPD410D1	uCOM-8	RAM	Chip	MNG	4096x1 Static RAM;Access Time 150ns Max	NECJ
15#	uPD410D2	uCOM-8	RAM	Chip	MNG	4096x1 Static RAM;Access Time 100ns Max	NECJ
16#	uPD410D	uCOM-8	RAM	Chip	MNG	4096x1 Static RAM;Access Time 200ns Max	NECJ
17#	uPD411AC	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 300ns Max;Plastic Pkg	NECJ
18#	uPD411AC-1	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 250ns Max;Plastic Pkg	NECJ
19#	uPD411AC-2	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 200ns Max;Plastic Pkg	NECJ
20#	uPD411AC-E	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 350ns Max;Plastic Pkg	NECJ
21#	uPD411AD	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 300ns Max;Ceramic Pkg	NECJ
22#	uPD411AD-1	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 250ns Max;Ceramic Pkg	NECJ
23#	uPD411AD-2	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 200ns Max;Ceramic Pkg	NECJ
24#	uPD411AD-E	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 350ns Max;Ceramic Pkg	NECJ
25#	uPD2111ALC	uCOM-8	RAM	Chip	MXX	256x4 Common I/O Static RAM;Access Time 350ns Max	NECJ
26#	uPD2111ALC-2	uCOM-8	RAM	Chip	MXX	256x4 Common I/O Static RAM;Access Time 250ns Max	NECJ
27#	uPD2111ALC-4	uCOM-8	RAM	Chip	MXX	256x4 Common I/O Static RAM;Access Time 450ns Max	NECJ
28#	uPD465C	uCOM-8	ROM	Chip	MNX	1024x8 Mask Programmable ROM;Plastic Pkg	NECJ
29#	uPD465D	uCOM-8	ROM	Chip	MNX	1024x8 Mask Programmable ROM;Ceramic Pkg	NECJ
30#	uPD8080AFC	uCOM-80F	CPU	Chip	MNX	8 Bit Microprocessor;Clock Freq 2.0 MHz;Plastic Pkg	NECJ
31#	uPD8080AFC-1	uCOM-80F	CPU	Chip	MNX	8 Bit Microprocessor;Clock Freq 3.0 MHz;Plastic Pkg	NECJ
32#	uPD8080AFC-2	uCOM-80F	CPU	Chip	MNX	8 Bit Microprocessor;Clock Freq 2.5 MHz;Plastic Pkg	NECJ
33#	uPD8080AFD	uCOM-80F	CPU	Chip	MNX	8 Bit Microprocessor;Clock Freq 2.0 MHz;Ceramic Pkg	NECJ
34#	uPD8080AFD-1	uCOM-80F	CPU	Chip	MNX	8 Bit Microprocessor;Clock Freq 3.0 MHz;Ceramic Pkg	NECJ
35#	uPD8080AFD-2	uCOM-80F	CPU	Chip	MNX	8 Bit Microprocessor;Clock Freq 2.5 MHz;Ceramic Pkg	NECJ
36▼#	uPD1519B	uCOM43	IO-92	Chip	MNX	ROM 4096x8;256x4 RAM	NECJ
37▼#	uPD1510C	uCOM44	IO-92	Chip	MNX	ALU;RAM/ROM/I/O;128x4 RAM 1008x8 ROM	NECJ
38▼#	uPD410D-1	uCOM8	RAM	Chip	MNG	4096x1 Static RAM;Access Time 150ns max	NECJ
39▼#	uPD410D-2	uCOM8	RAM	Chip	MNG	4096x1 Static RAM;Access Time 100ns max	NECJ
40▼#	uPD410D-3	uCOM8	RAM	Chip	MNG	4096x1 Static RAM;Access Time 90ns max	NECJ
41▼#	uPD2332C	uCOM8	ROM	Chip	MXX	4096x8 Bit ROM;Access time 450nS max	NECJ
42▼#	uPD2332D	uCOM8	ROM	Chipp	MXX	4096x8 Bit ROM;Access time 450nS max	NECJ
43#	uPB2901AD	uPB2900	CPU	Chip	BTD	4-Bit Bipolar Microprocessor Slice	NECJ
44#	uPB2905AD	uPB2900	IO-21	Chip	BTD	Quad Two-Input OC Bus Transceiver with Three State Receiver	NECJ
45#	uPB2906AD	uPB2900	IO-21	Chip	BTD	Quad Two-Input OC Bus Transceiver with Parity	NECJ
46#	uPB2907AD	uPB2900	IO-21	Chip	BTD	Quad OC Bus Transceiver with Three State Receiver and Parity	NECJ
47#	uPB2915AD	uPB2900	IO-21	Chip	BTD	Quad 3-State Bus Transceiver with Interface Logic	NECJ
48#	uPB2916AD	uPB2900	IO-21	Chip	BTD	Quad 3-State Bus Transceiver with Interface Logic	NECJ
49#	uPB2917AD	uPB2900	IO-21	Chip	BTD	Quad 3-State Bus Transceiver with Interface Logic	NECJ
50#	uPB2918D	uPB2900	IO-55	Chip	BTD	Quad Register with Standard and Three State Outputs	NECJ
51#	uPB2902AD	uPB2900	IO-90	Chip	BTD	High-Speed Look-Ahead Carry Generator	NECJ
52▼	uPB8214		IO-02	Chip		Priority Interrup Controller;8Level	NECM
53	uPD7520	uCOM 7500	CPU	Chip	MPX	48 x 4 RAM;24 I/O Lines;768 x 8 Bit PROM;28 Pin Plastic Pkg	NECM
54	uPD768B	uCOM-1600	CPU	Chip	MNX	16 Bit Single Chip Microprocessor,2 Bus,6.6MHz,5V Supply	NECM
55	uPD556B	uCOM-4	DEV	Chip	MPX	Evachip-43 for HW and SW Debugging;64 Pin Cer Quad-In-Line Package	NECM
56	uPD551C	uCOM-43	uCT	Chip	MPX	uCOM-46 Microcomp W/On-Chip A/D Conv;2% Resolution,4% Accuracy;40-Pin DIL	NECM
57	uPD553C	uCOM-43	uCT	Chip	MPX	High Neg Out Version of uCOM-43;Outs Can Be Pulled to-35 Volts	NECM
58	uPD557LC	uCOM-43	CPU	Chip		2k x 8 ROM,96 x 4 RAM,21 I/O Lines;28 Pin Dip	NECM
59	uPD650C	uCOM-43C	uCT	Chip	MCX	NECJ	NECM
60	uPD552C	uCOM-44	uCT	Chip	MPX	High Neg Out Version of uCOM-44;Outs Can Be Pulled to-35 Volts	NECM
61	uPD651G	uCOM-44	CPU	Chip	MCX	CMOS Version of uCOM-44	NECM
62	uPD651C	uCOM-44C	uCT	Chip	MCX	4 Bit Single Chip Microcomputer:RAM 64x4,ROM 1kx8,5V	NECM
63	uPD550C	uCOM-45	uCT	Chip	MPX	4 Bit Single Chip Comp of uCOM-45;Gen Purpose Controller;640x8 ROM	NECM
64	uPD652C	uCOM-45C	uCT	Chip	MCX	4 Bit Single Chip Microcomputer:RAM 32x4,ROM 1kx8,5V	NECM
65	uPD8049C	uCOM-8	uCT	Chip	MNG	8-Bit Single Chip uCOMP;5V Supply;128 RAM;2k Mask ROM;40-Pin DIL Plas Pkg	NECM
66	uPD8049D	uCOM-8	uCT	Chip	MNG	8-Bit Single Chip uCOMP;5V Supply;128 RAM;2k Mask ROM;40-Pin DIL Cer Pkg	NECM
67	uPD8748D	uCOM-8	uCT	Chip	MNX	8-Bit Single Chip Comp;64x8 RAM;1kx8 EPROM;27 I/O Liner;Req Ext Xtal	NECM
68	uPD8039LC	uCOM-8	CPU	Chip	MNG	8-Bit Single Chip uCt;5V Supply;128 RAM;40 Pin DIL Plastic Pkg	NECM
69	uPD8039LD	uCOM-8	CPU	Chip	MNG	8-Bit Single Chip uCt;5V Supply;128 RAM;40 Pin DIL Ceramic Pkg	NECM
70	uPD8080AD2	uCOM-8	CPU	Chip	MNG	8 Bit Microprocessor;Clock Freq 2.63MHz max	NECM
71	uPD8080AD	uCOM-8	CPU	Chip	MNG	8 Bit Microprocessor;Clock Freq 2.02MHz max	NECM
72	uPD8085AC	uCOM-8	CPU	Chip	MNX	Single Chip 8-Bit Microprocessor;1.3us Instruction Cycle;40-Pin Plas DIL	NECM
73#	uPD8085AD	uCOM-8	CPU	Chip	MNX	Single Chip 8-Bit Microprocessor;1.3us Instruction Cycle;40-Pin Cer DIL	NECM
74	NPM809A	uCOM-8	DEV	MOD		DMA Module;Includes Address Counter/Word Counter	NECM
75	NPM853	uCOM-8	DEV	MOD		EEPROM Programming Module;For uPD454D/uPD458D	NECM
76	TK-80A	uCOM-8	DEV	MOD		Single-board uCOMP for Developing 8080A Sys;Based on uPD8080AF Standard	NECM
77	PDA80	uCOM-8	DEV	UNIT		uCOM-8 Program Devel Aid;Complete System	NECM
78	uPD8253C	uCOM-8	IO-01	Chip	MNX	Programmable Interval Timer;Three 16-Bit Counters;24 Pin Plastic Pkg	NECM
79	uPB8228D	uCOM-8	IO-02	Chip		808A System Controller And Bus Driver For Small Mem Syst	NECM
80	uPB8238D	uCOM-8	IO-02	Chip		808A System Controller And Bus Driver For Large Mems Syst	NECM
81	uPD8259-5	uCOM-8	IO-02	Chip	MNX	Programmable Interrupt Controller;8 Level Expandable to 64;8085A Compat	NECM
82	uPD8259C	uCOM-8	IO-02	Chip	MNX	Programmable Interrupt Controller;8 Level Expandable to 64 Levels	NECM
83	uPD8259D	uCOM-8	IO-02	Chip	MNX	Programmable Interrupt Controller;8 Level Expandable to 64;28-Pin Cer Pkg	NECM
84	uPD8257C	uCOM-8	IO-03	Chip	MNX	Programmable DMA Controller;4 Chan Expandable;Used with uPD8212 I/O	NECM
85	uPD372D	uCOM-8	IO-07	Chip		Floppy Disk Controller;Controls Up To 4 F.D.Drives	NECM
86	uPD765C	uCOM-8	IO-07	Chip	MNX	Floppy Disk Controller,3 State,P Supply 5V;40 Pin Plastic Pkg	NECM
87	uPD758C	uCOM-8	IO-08	Chip	MNG	Digital Printer Controller;18 Instructions	NECM
88	uPD8279C-5	uCOM-8	IO-10	Chip	MNX	Keyboard/Display,64 Key,16 Char,3 State,40 Pin Plastic Pkg	NECM
89	uPD369D	uCOM-8	IO-20	Chip	MNX	Universal Asynchronous Receiver/Transmitter;0 To 70°C	NECM
90	uPB8216C	uCOM-8	IO-21	Chip	MNX	4 Bit Parallel Bi-direct Bus Driver;Non-Inverting;16 Pin Plastic Pkg	NECM
91	uPB8216D	uCOM-8	IO-21	Chip	MNX	4 Bit Parallel Bi-direct Bus Driver;Non-Inverting;16 Pin Ceramic Pkg	NECM
92	uPD8041C	uCOM-8	IO-30	Chip	MNX	8-Bit Gen Pur Prog IF W/1kx8 Mask ROM,64x8 RAM;40-Pin DIL Plas Pkg	NECM
93	uPD8041D	uCOM-8	IO-30	Chip	MNX	8-Bit Gen Pur Programmable IF;W/1kx8 Mask ROM,64x8 RAM;40-Pin DIL Cer Pkg	NECM
94	uPD8255AC-5	uCOM-8	IO-30	Chip	MNX	Perpheral Interface,3 State,P Supply 5V,40 Pin Plastic Pkg	NECM
95	uPD8255C-E	uCOM-8	IO-30	Chip		Programmable Peripheral Interface;40 Pin Plastic Pkg	NECM
96	uPD8741AC	uCOM-8	IO-30	Chip	MNX	8-Bit Gen Pur Prog if w/1kx8 UV EPROM;64x8 RAM;40 Pin DIL Plastic Pkg	NECM
97	uPD8741AD	uCOM-8	IO-30	Chip	MNX	8-Bit Gen Pur Prog if w/1kx8 UV EPROM;64x8 RAM;40 Pin DIL Ceramic Pkg	NECM
98	uPB8226C	uCOM-8	IO-31	Chip	MNX	4 Bit Parallel Bi-direct Bus Driver;Inverting;16 Pin Plastic Pkg	NECM
99	uPB8226D	uCOM-8	IO-31	Chip	MNX	4 Bit Parallel Bi-direct Bus Driver;Inverting;16 Pin Ceramic Pkg	NECM
100	uPB8224C	uCOM-8	IO-32	Chip	BTX	Clock Generator and Driver for 8080A Processors;Plastic Pkg	NECM
101	uPB8224D	uCOM-8	IO-32	Chip		Clock Generator And Driver For 8080A Processors	NECM
102	uPB8212C	uCOM-8	IO-33	Chip		8 Bit Input/Output Port;Plastic Pkg	NECM
103	uPB8212D	uCOM-8	IO-33	Chip		8 Bit Input/Output Port;Ceramic Pkg	NECM
104	uPD8243C	uCOM-8	IO-33	Chip	MNX	I/O Expander;5V Supply;Four 4-Bit I/O Ports;24-Pin Plastic DIL Package	NECM
105	uPD8243D	uCOM-8	IO-33	Chip	MNX	I/O Expander;5V Supply;Four 4-Bit I/O Ports;24-Pin Ceramic DIL Package	NECM
106	uPD754C	uCOM-8	IO-56	Chip	MNX	8 Bit High Speed Latch;tpd 100ns max	NECM
107	uPD754D	uCOM-8	IO-56	Chip	MNX	8-Bit High Speed Latch;tpd 100ns max	NECM
108	uPD8155C	uCOM-8	IO-57	Chip	MNX	256x8 RAM;Used W/uPD8085 CPU;Access Time 400ns;On-Chip 14 Bit Counter	NECM
109	uPD8156C	uCOM-8	IO-57	Chip	MNX	256x8 RAM;Used W/uPD8085 CPU;Access Time 400ns	NECM
110	uPD8355C	uCOM-8	IO-57	Chip	MNX	Combination 2kx8 ROM,Two 8-Bit I/O Ports;Access Time 400ns	NECM

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	uPD8755AD	uCOM-8	IO-57	Chip		2048x8 Bit Mask EPROM,2 General Purpose IO Ports	NECM
2	uPB403D	uCOM-8	PROM	Chip		256x4 PROM,Access Time 60ns,Open Collector	NECM
3	uPB417C	uCOM-8	PROM	Chip	BTX	1024x8 PROM;Access Time 200ns Max;24 Pin Plastic Pkg	NECM
4	uPD454D	uCOM-8	PROM	Chip	MNX	256x8 Static PROM;Access Time 800ns max	NECM
5	uPD458D	uCOM-8	PROM	Chip	MNX	1024x8 Static PROM;Access Time 450ns max	NECM
6	uPD464D	uCOM-8	PROM	Chip	MNG	256x8 Static PROM;Access Time 450ns max	NECM
7	uPD466D	uCOM-8	PROM	Chip	MNG	2048x8 Static PROM;Access Time 475ns Max;Ceramic Pkg	NECM
8	uPD2308AC	uCOM-8	PROM	Chip	MNX	1024x8 Static PROM;Access Time 450nS Max;Plastic Pkg	NECM
9	uPD2308D	uCOM-8	PROM	Chip	MNX	1024x8 Static PROM;Access Time 450ns Max;Ceramic Pkg	NECM
10	uPD2716D	uCOM-8	PROM	Chip	MNX	2kx8 EPROM;Access Time 450ns max;UV Erasable;24 Pin Ceramic Pkg	NECM
11	uPB2200D	uCOM-8	RAM	Chip	BTX	256x1 Bit RAM,Access Time 50ns,Tri State	NECM
12	uPB2202D	uCOM-8	RAM	Chip	BTX	256x1 Bit RAM,Access Time 65ns,Tri State	NECM
13	uPB2205D	uCOM-8	RAM	Chip	BTX	1024x1 Bit RAM,Access Time 50ns,Open Collector	NECM
14	uPB2206D	uCOM-8	RAM	Chip	BTX	256x1 Bit RAM,Access Time 50ns,Open Collector	NECM
15	uPB2289D	uCOM-8	RAM	Chip	BTX	16x4 Bit RAM,Access Time 35ns,Open Collector	NECM
16	uPB10142D	uCOM-8	RAM	Chip	BEX	64x1 Bit RAM,Access Time 12ns	NECM
17	uPB10144D	uCOM-8	RAM	Chip	BEX	64x1 Bit RAM,Access Time 25ns	NECM
18	uPB10148D	uCOM-8	RAM	Chip	BEX	64x1 Bit RAM,Access Time 15ns	NECM
19	uPD410D3	uCOM-8	RAM	Chip	MNG	4096x1 Static RAM;Access Time 90ns Max	NECM
20	uPD411D	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 300ns	NECM
21	uPD411D-1	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 250ns	NECM
22	uPD411D-2	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 200ns	NECM
23	uPD411D-3	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 150ns	NECM
24	uPD411D-4	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 135ns	NECM
25	uPD411D-E	uCOM-8	RAM	Chip	MNX	4096x1 Dynamic RAM;Access Time 350ns	NECM
26	uPD416C	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 300ns;Refresh 2.0ms;16 Pin Plastic Pkg	NECM
27	uPD416C-1	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 250ns;Refresh 2.0ms;16 Pin Plastic Pkg	NECM
28	uPD416C-2	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 200ns;Refresh 2.0ms;16 Pin Plastic Pkg	NECM
29	uPD416C-3	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 150ns;Refresh 2.0ms;16 Pin Plastic Pkg	NECM
30	uPD416C-5	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 120ns;Refresh 2.0ms;16 Pin Plastic Pkg	NECM
31	uPD416D	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 300ns;Refresh 2.0ms;16 Pin Ceramic Pkg	NECM
32	uPD416D-1	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 250ns;Refresh 2.0ms;16 Pin Ceramic Pkg	NECM
33	uPD416D-2	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 200ns;Refresh 2.0ms;16 Pin Ceramic Pkg	NECM
34	uPD416D-3	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 150ns;Refresh 2.0ms;16 Pin Ceramic Pkg	NECM
35	uPD416D-5	uCOM-8	RAM	Chip	MNG	16kx1 Dyn RAM;Access Time 120ns;Refresh 2.0ms;16 Pin Ceramic Pkg	NECM
36	uPD421	uCOM-8	RAM	Chip	MNG	1kx8 Static RAM;85/100/150/200ns tacc;Tri-State I/O;5V Sup;22-Pin DIL	NECM
37	uPD444C	uCOM-8	RAM	Chip	MCX	1kx4 Static RAM;Access Time 250ns Max,18 Pin Plastic Pkg	NECM
38	uPD445LC	uCOM-8	RAM	Chip	MCX	1kx4 Static RAM;Access Time 650ns Max,20 Pin Plastic Pkg	NECM
39	uPD445LC-1	uCOM-8	RAM	Chip	MCX	1kx4 Static RAM;Access Time 450ns Max,20 Pin Plastic Pkg	NECM
40	uPD2101ALC	uCOM-8	RAM	Chip		256x4 Decoded Static RAM,Access Time 350ns	NECM
41	uPD2101ALC-2	uCOM-8	RAM	Chip		256x4 Decoded Static RAM,Access Time 250ns	NECM
42	uPD2101ALC-4	uCOM-8	RAM	Chip		256x4 Decoded Static RAM,Access Time 450ns	NECM
43	uPD2102ALC	uCOM-8	RAM	Chip		1024x1 Decoded Static RAM,Access Time 350ns	NECM
44	uPD2102ALC-2	uCOM-8	RAM	Chip		1024x1 Decoded Static RAM,Access Time 250ns	NECM
45	uPD2102ALC-4	uCOM-8	RAM	Chip		1024x1 Decoded Static RAM,Access Time 450ns	NECM
46	uPD2114LC	uCOM-8	RAM	Chip	MNG	1kx4 Static RAM;450ns Access;18-Pin Plastic DIL Pkg	NECM
47	uPD2114LC-1	uCOM-8	RAM	Chip	MNG	1kx4 Static RAM;300ns Access;18-Pin Plastic DIL Pkg	NECM
48	uPD2114LC-2	uCOM-8	RAM	Chip	MNG	1kx4 Static RAM;250ns Access;18-Pin Cerdip DIL Pkg	NECM
49	uPD2114LC-3	uCOM-8	RAM	Chip	MNG	1kx4 Static RAM;200ns Access;18-Pin Plastic DIL Pkg	NECM
50	uPD2114LC-5	uCOM-8	RAM	Chip	MNG	1kx4 Static RAM;150ns Access;18-Pin Plastic DIL Pkg	NECM
51	uPD2114LD	uCOM-8	RAM	Chip	MNG	1kx4 Static RAM;450ns Access;18-Pin Cerdip DIL Pkg	NECM
52	uPD2114LD-1	uCOM-8	RAM	Chip	MNG	1kx4 Static RAM;300ns Access;18-Pin Cerdip DIL Pkg	NECM
53	uPD2114LD-3	uCOM-8	RAM	Chip	MNG	1kx4 Static RAM;200ns Access;18-Pin Cerdip DIL Pkg	NECM
54	uPD2114LD-5	uCOM-8	RAM	Chip	MNG	1kx4 Static RAM;150ns Access;18-Pin Cerdip DIL Pkg	NECM
55	uPD2147C	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;Access Time 55ns Max;18 Pin Plastic Pkg	NECM
56	uPD2147D	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;85ns Access;3-State Output;18-Pin Cer DIL Pkg	NECM
57	uPD2147D-2	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;70ns Access;3-State Output;18-Pin Cer DIL Pkg	NECM
58	uPD2147D-3	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;55ns Access;3-State Output;18-Pin Cer DIL Pkg	NECM
59	uPD4104C	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;300nS Access;18 Pin DIL Plastic Pkg	NECM
60	uPD4104C-1	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;200nS Access;18 Pin DIL Plastic Pkg	NECM
61	uPD4104C-2	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;150nS Access;18 Pin DIL Plastic Pkg	NECM
62	uPD4104C-3	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;120nS Access;18 Pin DIL Plastic Pkg	NECM
63	uPD4104D	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;300nS Access;18 Pin DIL Ceramic Pkg	NECM
64	uPD4104D-1	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;200nS Access;18 Pin DIL Ceramic Pkg	NECM
65	uPD4104D-2	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;150nS Access;18 Pin DIL Ceramic Pkg	NECM
66	uPD4104D-3	uCOM-8	RAM	Chip	MNX	4kx1 Static RAM;120nS Access;18 Pin DIL Ceramic Pkg	NECM
67	uPD5101C-E	uCOM-8	RAM	Chip		256x4 Low Power RAM,Access Time 1.0us	NECM
68	uPD6508C-1	uCOM-8	RAM	Chip	MNG	1kx1 Static RAM;Access Time 250ns max;IM5608 Replacement;Plastic Pkg	NECM
69	uPD2316EC	uCOM-8	ROM	Chip	MNX	2kx8 ROM;Access Time 450ns max;Tri-State,Intel 2316E Repl;Plastic Pkg	NECM
70	uPD2316ED	uCOM-8	ROM	Chip	MNX	2kx8 ROM;Access Time 450ns max;Tri-State;Intel 2316E Repl;Ceramic Pkg	NECM
71	uPD2364C	uCOM-8	ROM	Chip	MNX	8kx8 ROM;Access Time 450ns Max;24 Pin Plastic Pkg	NECM
72	uPD2364D	uCOM-8	ROM	Chip	MNX	8kx8 ROM;Access Time 450ns max;24-Pin Ceramic Pkg	NECM
73	uPD8021C	uPD8021	CPU	Chip	MNG	8 Bit Processor,ROM,RAM,I/O and Counter/Timer;28 Pin Plastic Pkg	NECM
74	uPD8022C	uPD8022	CPU	Chip	MNG	8 Bit Processor,ROM,RAM,I/O and Clk Gen;2 Ch 8 Bit A/D Conv;40 Pin PLs	NECM
75	uPD3301-1C	8080	IO-09	Chip		Sync Signal Gen,Row Buffer,Attribute Memory;For B/W or Color CRT;Plastic	NECM
76	uPD3301-2C	8080	IO-09	Chip		Sync Signal Gen,Row Buffer,Attribute Memory;For B/W or Color CRT;Plastic	NECM
77	uPD3301-2D	8080	IO-09	Chip		Sync Signal Gen,Row Buffer,Attribute Memory;For B/W or Color CRT;Ceramic	NECM
78	uPD7801B	8080A	CPU	Chip	MNG	8 Bit Single Chip uCT;4096x8 ROM;128 x 8 RAM;8 Bit ALU;48 I/O Lines	NECM
79	uPD782C	8080A/8085A	IO-09	Chip	MNX	Interface to Epson Model 210,220, and 240 Printers;7 x 7 Dot Matrix	NECM
80	NMS85/AR	NMS85/P	COMP	UNIT		8 Bit Microcomp Syst:Accounts Receivable Syst Based On NM85/P Using 8085	NMS
81	NMS85/GL	NMS85/P	COMP	UNIT		8 Bit Microcomp Syst:General Ledger Syst Based On NM85/P Using 8085	NMS
82	NMS85/P	NMS85/P	COMP	UNIT		8 Bit Microcomp Syst:Includes,54k RAM,PASCAL Compiler,Display,KB,Disk Dr	NMS
83	NMS85/WP	NMS85/P	COMP	UNIT		8 Bit Microcomp Syst:Word Processing Center Based On NM85/P Using 8085	NMS
84	HORIZON-1	HORIZON-1	COMP	UNIT		8 Bit Microcomputer;Uses Z80A Processor;32k RAM Board;Miniflop Disk;S-100	NOR
85	HORIZON-2	HORIZON-1	COMP	UNIT		8 Bit Microcomputer;Uses Z80A Processor;Two Minifloppy Disk Drives	NOR
86	ZPB-A	HORIZON-1	CPU	MOD		Z80A Processor Board;Runs at 4.0MHz	NOR
87	FPB-A	HORIZON-1	IO-90	MOD		Hardware Floating Point Board;Kit/Assm;Power Req 8V Unreg	NOR
88	MDS-A	HORIZON-1	PE-02	UNIT		Micro Disk Syst;Uses S-100 Bus Convention Of Z80;8080 Syst;Kit/Asm	NOR
89	ZPB-PROM	HORIZON-1	PROM	MOD		1k Byte Erasable PROM Option;Mounts on ZPB-A Board	NOR
90	RAM-16-A	HORIZON-1	RAM	UNIT		16k Dynamic RAM Board W/S-100 Bus Compatibility;Access Time 200ns	NOR
91	MM5799N	COPS57100	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer;1536 Microinstruction ROM	NSC
92	MM57140N	COPS57100	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer;Direct LED Display Drive	NSC
93	MM57152N	COPS57100	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer;Direct VF Display Drive	NSC
94	MM5782N	COPS57100	CPU	Chip	MPX	Memory and Processor Element	NSC
95	MM5781N	COPS57100	CROM	Chip	MPX	16k Control and ROM Element	NSC
96	MM57129N	COPS57100	CROM	Chip	MPX	32k Control and ROM Element	NSC
97	MM5785	COPS57100	IO-03	Chip	MPX	Memory Interface to 1024 x 1 RAM Devices	NSC
98	MM5788	COPS57100	IO-08	Chip	MPX	Printer Interface to Seiko Printers	NSC
99	MM57126	COPS57100	IO-55	Chip	MPX	Programmer Shift Register	NSC
100	MM57109	COPS57100	IO-90	Chip	MPX	Number Processing Unit;Use in Scientific Calculator Function	NSC
101	COP402	COP400	uCT	Chip	MPX	4 Bit Microcontroller;COP420 without ROM	NSC
102	COP410L	COP400	uCT	Chip	MPX	4 Bit Microcontroller;5mA;4.5-9.5V Supply	NSC
103	COP411L	COP400	uCT	Chip	MPX	4 Bit Microcontroller;COP410L in 20 PIN Pkg	NSC
104	COP420	COP400	uCT	Chip	MPX	4 Bit Microcontroller	NSC
105	COP420L	COP400	uCT	Chip	MPX	4 Bit Microcontroller;7mA;4-9V Supply	NSC
106	DP4201J	FIPS	IO-32	Chip		Clock Gen;Req Ext Xtal-Controlled OSC;16-Pin Glass/Glass DIL Pkg	NSC
107	DP4201N	FIPS	IO-32	Chip		Clock Gen;Req Ext Xtal-Controlled OSC;16-Pin Plas Pkg	NSC
108	INS4201	FIPS	IO-32	Chip	MPG	FIPS System Clock Chip	NSC
109	INS4702A	FIPS	PROM	Chip	MPG	Reprogrammable PROM	NSC
110	IDM2903ADC	IDM2900	uCT	Chip	BED	4 Bit Slice;0 to 70°C;Hermetic DIP;Expand Register File;Arith/Logic IS	NSC

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	IDM2903ADM	IDM2900	uCT	Chip	BED	4 Bit Slice;-55 to 125°C;Hermetic DIP;Expand Register File;Arith/Logic IS	NSC
2	IDM2903ADM/883	IDM2900	uCT	Chip	BED	4 Bit Slice;-55 to 125°C;Hermetic DIP;Expand Register File;Arith/Logic IS	NSC
3	IDM2901A-1DM/883	IDM2900	uCT	CHIP	BED	4 Bit Slice;Multifunction ALU;4 Status Flags;Expandable	NSC
4	IDM2901A-2DC	IDM2900	uCT	CHIP	BED	4 Bit Slice;0 to 70°C;Hermetic DIP;16-Word x 4-Bit 2 Port RAm;Hi-Speed	NSC
5	IDM2901A-2DM	IDM2900	uCT	CHIP	BED	4 Bit Slice;-55 to 125°C;Herm DIP;16-Word x 4-Bit 2 Port RAM;Hi-Speed	NSC
6	IDM2901A-2DM/883	IDM2900	uCT	CHIP	BED	4 Bit Slice;-55 to 125°C;Herm DIP;16-Word x 4-Bit 2 Port RAM;Hi-Speed	NSC
7	IDM2901A-2NC	IDM2900	uCT	CHIP	BED	4 Bit Slice;0 to 70°C;Molded Dip;16-Word x 4-Bit 2 Port RAM;Hi-Speed	NSC
8	IDM2901ADM/883	IDM2900	COMP	Chip	BED	4 Bit Slice;55to125°C;Hermetic DIP;Includes 16W x 4B 2 Port RAM	NSC
9	IDM2901ANC	IDM2900	COMP	Chip	BED	4 Bit Slice;0to70°C;Molded DIP;Includes 16W x 4B 2 Port RAM	NSC
10	IDM2901A-1DC	IDM2900	CPU	Chip	BED	4 Bit Slice;Max Clock Lo/Hi Time 25ns;0 to 70°C;Inc 16Wx4B 2 Port RAM	NSC
11	IDM2901A-1DM	IDM2900	CPU	Chip	BED	4 Bit Slice;Max Clock Lo/Hi Time 25ns;-55 to 125°C;Inc 16Wx4B 2 Port RAM	NSC
12	IDM2901A-1NC	IDM2900	CPU	Chip	BED	4 Bit Slice;Max Clock Lo/Hi Time 25ns;0 to 70°C;Inc 16Wx4B 2 Port RAM	NSC
13	IDM2901ADC	IDM2900	CPU	Chip	BED	4 Bit Slice;0 to 70°C;Hermetic DIP;Includes 16W x 4B 2 Port RAM	NSC
14	IDM2901ADM	IDM2900	CPU	Chip	BED	4 Bit Slice;-55 to 125°C;Hermetic DIP;Includes 16W x 4B 2 Port RAM	NSC
15	IDM2901AFM	IDM2900	CPU	Chip	BED	4 Bit Slice;-55 to 125°C;Hermetic Flat Pack;Inc 16W x 4B 2 Pt RAM	NSC
16	IDM2901APC	IDM2900	CPU	Chip	BED	4 Bit Slice;0 to 70°C;Molded DIP;Includes 16W x 4B 2 Port RAM	NSC
17	IDM2909AC	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;4-Bit Address Cont Seq thru Inst in ROM;0 to 70°C	NSC
18	IDM2909ADC	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;4 Bit Address Cont,Seq thru Inst in ROM,0 to 70°C	NSC
19	IDM2909ADM	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;4 Bit Addr Cont,Seq thru Inst in ROM,-55 to 125°C	NSC
20	IDM2909AJC	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;4-Bit Address Cont;Seq thru Inst in ROM;0 to 70°C	NSC
21	IDM2909AJM	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;4-Bit Address Cont;Seq thru Inst in ROM;-55 to 125	NSC
22	IDM2909AJM/883	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;4-Bit Address Cont;Seq thru Inst in ROM;-55 to 125	NSC
23	IDM2909ANC	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;4 Bit Address Cont,Seq thru Inst in ROM,0 to 70°C	NSC
24	IDM2910ADC	IDM2900	IO-01	Chip	BED	12 Bit Wide Address Controller;4 Address Sources;0 to 70°C;Hermetic DIP	NSC
25	IDM2910ADM	IDM2900	IO-01	Chip	BED	IDM2910ADC w/-55 to 125°C Temp Range	NSC
26	IDM2910ADM/883	IDM2900	IO-01	Chip	BED	IDM2910ADM w/100% Reliability Testing in Compliance With MIL-STD-883	NSC
27	IDM2910ANC	IDM2900	IO-01	Chip	BED	12 Bit Wide Address Controller; 4 Address Sources; 0 to 70°C; Molded DIP	NSC
28	IDM2911AC	IDM2900	IO-01	Chip	BED	Same as IDM2909 Except OR Inputs Disconnected and D R Inputs Connected	NSC
29	IDM2911ADC	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;Same as IDM2909 Except W/O OR In;W/D,R Inputs	NSC
30	IDM2911ADM	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;Same as IDM2909 Except W/O OR In;W/D,R Inputs	NSC
31	IDM2911AJC	IDM2900	IO-01	Chip	BED	Same as IDM2909 Except OR Inputs Disconnected and D R Inputs Connected	NSC
32	IDM2911AJM	IDM2900	IO-01	Chip	BED	Same as IDM2909 Except OR Inputs Disconnected and D R Inputs Connected	NSC
33	IDM2911AJM/883	IDM2900	IO-01	Chip	BED	Same as IDM2909 Except OR Inputs Disconnected and D R Inputs Connected	NSC
34	IDM2911ANC	IDM2900	IO-01	Chip	BED	Microprogram Sequencer;Same as IDM2909 Except W/O OR In;W/D,R Inputs	NSC
35	IDM29803JC	IDM2900	IO-01	Chip	BED	16 Way Branch Controller;Branch Cont W/16 Seperate Inst;0 to 70°C	NSC
36	IDM29803JM	IDM2900	IO-01	Chip	BED	16 Way Branch Controller;Branch Cont W/16 Seperate Inst;-55 to 125°C	NSC
37	IDM29803JM/883	IDM2900	IO-01	Chip	BED	16 Way Branch Controller;Cont w/16 Separate Inst MIL Temp/MIL-STD-883	NSC
38	IDM29803NC	IDM2900	IO-01	Chip	BED	16 Way Branch Controller;Branch Cont W/16 Seperate Inst;0 to 70°C	NSC
39	IDM29811JC	IDM2900	IO-01	Chip	BED	Next Address Controller;Used for Controlling IDM2911A Sequencer;0 to 70°C	NSC
40	IDM29811JM	IDM2900	IO-01	Chip	BED	Next Address Controller;Used for Controlling IDM2911A Seq;-55 to 125°C	NSC
41	IDM29811JM/883	IDM2900	IO-01	Chip	Bed	Next-Address Controller;16 Instructions;MIL Temp/MIL-STD-883NS	NSC
42	IDM29811NC	IDM2900	IO-01	Chip	BED	Next Address Controller;Used for Controlling IDM2911A Sequencer;0 to 70°C	NSC
43	IDM29705AJM/883	IDM2900	IO-55	Chip	BED	IDM2905JM w/Compliance to MIL-STD-883; Hi-Speed	NSC
44	IDM29705JC	IDM2900	IO-55	Chip	BED	16-Word x 4-Bit Two Port Register File; 0 to 70°C	NSC
45	IDM29705JM	IDM2900	IO-55	Chip	BED	16-Word x 4-Bit Two Port Register File; -55 to 125°C	NSC
46	IDM29705JM/883	IDM2900	IO-55	Chip	BED	IDM2905JM w/Compliance to MIL-STD-883	NSC
47	IDM29901JC	IDM2900	IO-55	Chip	BED	Octal Register;Edge Triggered Flip Flop Used for Tempo Storage;0 to 70°C	NSC
48	IDM29901JM	IDM2900	IO-55	Chip	BED	Octal Register;Edge Triggered Flip Flop Used for Tempo Stor;-55 to 125°C	NSC
49	IDM29901NC	IDM2900	IO-55	Chip	BED	Octal Register;Edge Triggered Flip Flop Used for Tempo Storage;0 to 70°C	NSC
50	IDM29901JM/883	IDM2900	IO-92	Chip	BED	TRI-State Octal Register;Direct Interface to Bus Organized Sys;MIL STDS	NSC
51	DM54S472	IDM2900	PROM	Chip	BED	512x8 PROM w/Tri-State Outputs; -55 to 125°C	NSC
52	DM54S473	IDM2900	PROM	Chip	BED	512x8 Open Collector PROM; -55 to 125°C; Max Access Time 60ns (Address)	NSC
53	DM54S474	IDM2900	PROM	Chip	BED	512x8 Tri-State PROM; -55 to 125°C; Access Time 65ns (Address)	NSC
54	DM54S475	IDM2900	PROM	Chip	BED	512x8 Open Collector PROM;-55 to 125°C;Access Time 65ns	NSC
55	DM54S572	IDM2900	PROM	Chip	BED	1024x4 Open Collector PROM;-55 to 125°C;Access Time 60ns(Max)	NSC
56	DM54S573	IDM2900	PROM	Chip	BED	1024x4 Tri-State PROM; -55 to 125°C; Access Time 60ns (Max) (Address)	NSC
57	DM54S574	IDM2900	PROM	Chip	BED	1024x4 TRI-State PROM;-55 to 125°C;Access Time 60nS(Max)	NSC
58	DM74S472	IDM2900	PROM	Chip	BED	512x8 PROM w/Tri-State Outputs; 0 to 70°C	NSC
59	DM74S473	IDM2900	PROM	Chip	BED	512x8 Open Collector PROM; 0 to 70°C; Max Access Time 60ns (Address)	NSC
60	DM74S474	IDM2900	PROM	Chip	BED	512x8 Tri-State PROM; 0 to 70°C; Access Time 65ns (Address)	NSC
61	DM74S475	IDM2900	PROM	Chip	BED	512x8 Open Collector PROM; 0 to 70°C; Access Time 65ns (Address)	NSC
62	DM74S572	IDM2900	PROM	Chip	BED	1024x4 Open Collector PROM; 0 to 70°C; Access Time 60ns (Max) (Address)	NSC
63	DM74S573	IDM2900	PROM	Chip	BED	1024x4 Tri-State PROM; 0 to 70°C; Access Time 60ns (Max) (Address)	NSC
64	DM74S574	IDM2900	PROM	Chip	BED	1024x4 TRI-State PROM;0 to 70°C;Access Time 60nS(Max)	NSC
65	DM77S184	IDM2900	PROM	Chip	BED	2048x4 Open Collector PROM;-55 to 125°C;Max Access Time 40nS	NSC
66	DM77S185	IDM2900	PROM	Chip	BED	2048x4 TRI-State PROM;-55 to 125°C;Max Access Time 40nS	NSC
67	DM87S184	IDM2900	PROM	Chip	BED	2048x4 Open Collector PROM;0 to 70°C;Max Access Time 40nS	NSC
68	DM87S185	IDM2900	PROM	Chip	BED	2048x4 TRI-State PROM;0 to 70°C;Max Access Time 40ns	NSC
69	IDM29750JC	IDM2900	PROM	Chip	BED	32x8 Field Programmable ROM W/Open Collector Output;0 to 70°C	NSC
70	IDM29750JM	IDM2900	PROM	Chip	BED	32x8 Field Programmable ROM W/Open Collector Output;-55 to 125°C	NSC
71	IDM29750JM/883	IDM2900	PROM	Chip	BED	32x8 Field Programmable ROM w/Open Coll Output MIL temp/MIL-STD-883	NSC
72	IDM29750NC	IDM2900	PROM	Chip	BED	32x8 Field Programmable ROM W/Open Collector Output;0 to 70°C	NSC
73	IDM29751JC	IDM2900	PROM	Chip	BED	32x8 Field Programmable ROM W/Tri State Output;0 to 70°C	NSC
74	IDM29751JM	IDM2900	PROM	Chip	BED	32x8 Field Programmable ROM W/Tri State Output;-55 to 125°C	NSC
75	IDM29751JM/883	IDM2900	PROM	Chip	BED	IDM29750JM/883 w/TRI-STATE Output NS	NSC
76	IDM29751NC	IDM2900	PROM	Chip	BED	32x8 Field Programmable ROM W/Tri State Output;0 to 70°C	NSC
77	IDM29760JC	IDM2900	PROM	Chip	BED	256x4 Field Programmable ROM W/Open Collector Output;0 to 70°C	NSC
78	IDM29760JM	IDM2900	PROM	Chip	BED	256x4 Field Programmable ROM W/Open Collector Output;-55 to 125°C	NSC
79	IDM29760JM/883	IDM2900	PROM	Chip	BED	256x4 Field Programmable ROM w/Open-Coll Output MIL Temp/MIL-STD-883	NSC
80	IDM29760NC	IDM2900	PROM	Chip	BED	256x4 Field Programmable ROM W/Open Collector Output;0 to 70°C	NSC
81	IDM29761JC	IDM2900	PROM	Chip	BED	256x4 Field Programmable ROM W/Tri State Output;0 to 70°C	NSC
82	IDM29761JM	IDM2900	PROM	Chip	BED	256x4 Field Programmable ROM W/Tri State Output;-55 to 125°C	NSC
83	IDM29761JM/883	IDM2900	PROM	Chip	BED	IDM29760JM/883 w/TRI-STATE Output N	NSC
84	IDM29761NC	IDM2900	PROM	Chip	BED	256x4 Field Programmable ROM W/Tri State Output;0 to 70°C	NSC
85	IDM29702DC	IDM2900	RAM	Chip	BED	16x4 Bit RAM W/Tri-State Output;0 to 70°C	NSC
86	IDM29702DM	IDM2900	RAM	Chip	BED	16x4 Bit RAM W/Tri-State Output;-55 to 125°C	NSC
87	IDM29702JC	IDM2900	RAM	Chip	BED	16x4 Bit RAM w/Open Collector Output; 0 to 70°C; Access From Address 25ns	NSC
88	IDM29702JM/883	IDM2900	RAM	Chip	BED	IDM29702JM w/Compliance to MIL-STD-883;	NSC
89	IDM29702NC	IDM2900	RAM	Chip	BED	16x4 Bit RAM W/Tri-State Output;0 to 70°C	NSC
90	IDM29703JC	IDM2900	RAM	Chip	BED	16x4 Bit RAM With Open Collector Output;0 to 70°C	NSC
91	IDM29703JM	IDM2900	RAM	Chip	BED	16x4 Bit RAM With Open Collector Output;-55 to 125°C	NSC
92	IDM29703JM/883	IDM2900	RAM	Chip	BED	IDM29702JM w/TRI-State Outputs	NSC
93	IDM29703NC	IDM2900	RAM	Chip	BED	16x4 Bit RAM With Open Collector Output;0 to 70°C	NSC
94	IDM29704AJC	IDM2900	RAM	Chip	BED	16x4 Bit,2 Port Reg File;Open Coll;0 to 70°C;Hermetic DIP	NSC
95	IDM29704AJM	IDM2900	RAM	Chip	BED	16x4 Bit,2 Port Reg File;Open Coll;55 to 125°C;Hermetic DIP	NSC
96	IDM29705AJC	IDM2900	RAM	Chip	BED	16x4 Bit,2 Port Reg File;Three State;0 to 70°C;Hermetic DIP	NSC
97	IDM29705AJM	IDM2900	RAM	Chip	BED	16x4 Bit,2 Port Reg File;Three State;55 to 125°C;Hermetic DIP	NSC
98	IDM29705ANC	IDM2900	RAM	Chip	BED	16x4 Bit,2 Port Reg File;Three State;0 to 70°C;Molded DIP	NSC
99	IDM29903JC	IDM2900	RAM	Chip	BED	64 Bit Edge Triggered Register;16x4 Clocked RAM as Addressable D Reg	NSC
100	IDM29903NC	IDM2900	RAM	Chip	BED	64 Bit Edge Triggered Register;16x4 Clocked RAM as Addressable D Reg	NSC
101	IMP16C400	IMP16	COMP	MOD	MPG	16 Bit uProc Card Incl IMP16A500 Chip Set, 1k RAM/1k ROM	NSC
102	IMP16C500	IMP16	COMP	MOD	MPG	16 Bit uProc Card Incl IMP16A502 Chip Set, 1k RAM/1k ROM	NSC
103	IMP16C200	IMP16	CPU	MOD	MPG	16 Bit CPU Card Incl IMP16A500 Chip Set,256 Bit RAM	NSC
104	IMP16C200A	IMP16	CPU	MOD	MPG	16 Bit CPU Card Incl IMP16A500 Chip Set,256 Bit RAM/512 Bit ROM	NSC
105	IMP16C300	IMP16	CPU	MOD	MPG	16 Bit CPU Card Incl IMP16A502 Chip Set,256 Bit RAM/512 Bit ROM	NSC
106	IMP16P200	IMP16	DEV	UNIT	MPG	16 Bit Development Unit Using The IMP16C200 CPU Card	NSC
107	IMP16P208	IMP16	DEV	UNIT	MPG	16 Bit Dev Unit Using IMP16C200 CPU Card,8kx16 Bit RAM	NSC
108	IMP16P300	IMP16	DEV	UNIT	MPG	16 Bit Development Unit Using The IMP16C300 CPU Card	NSC

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	IMP16P308	IMP16	DEV	UNIT	MPG	16 Bit Dev Unit Using IMP16C300 CPU Card,8kx16 Bit RAM	NSC
2	IMP16P004T	IMP16	IO-03	MOD	MPG	Memory Timing And Interface Control Card	NSC
3	IMP16P810W	IMP16	IO-04	MOD	MPG	TTY/Card Reader/Paper Tape Reader Card,2 Ports-TTY,Documation 300	NSC
4	IMP16P840W	IMP16	IO-07	MOD	MPG	Floppy Disk Controller/CRT Interface Card	NSC
5	IMP16L812W	IMP16	IO-08	MOD	MPG	Printer Interface Card For Centronics 306 Printer	NSC
6	IMP16P008P	IMP16	IO-55	MOD		ROM/PROM Memory Card,8 or 16 Bit Capability,Expands Memory To 65,536	NSC
7	IMP16P840	IMP16	PE-01	UNIT		Dual Drive Floppy Disk Subsystem (Shugart)	NSC
8	IMP16P812	IMP16	PE-10	UNIT		Centronics Printer	NSC
9	IMP00/810	IMP16	PE-24	UNIT		Teletype;ASR Model 33	NSC
10	IMP16/810	IMP16	PE-24	UNIT		Teletype,ASR Model 33	NSC
11	IMP16L825W	IMP16	PE-40	UNIT		Card Reader Interface Package	NSC
12	IMP16P825	IMP16	PE-40	UNIT		Card Reader For Documentation M300	NSC
13	IMP00852	IMP16	PE-42	UNIT		Paper Tape Reader(Plessey 1000 Hz)	NSC
14	IMP16L006B	IMP16	RAM	MOD	MPG	2k By 16 Bit Static Read/Write Memory Card W/16 Sockets For MM5204Q/5214	NSC
15	IMP16L006P	IMP16	RAM	MOD	MPG	2k By 16 Bit Static Read/Write Memory Card W/16 Blank Sockets For MM5204Q	NSC
16	IMP16P004	IMP16	RAM	MOD		RAM 4k Memory Card	NSC
17	IMP16P004A	IMP16	RAM	MOD	MPG	4kx16 Static RAM Card	NSC
18	IMP16L004	IMP16	ROM	MOD		4k Memory Card With Sockets For ROMs	NSC
19	INS8900D	IPC16	CPU	Chip	MNG	16 Bit Single Chip Microprocessor;Single Phase 2MHz Clock	NSC
20	IPC16C100	IPC16	CPU	MOD	MPG	PACE Application Card With CPU,Clock And I/O Units	NSC
21	IPC16P004A	IPC16	DEV	MOD	MPG	PACE Development System Static 4x16 RAM Card	NSC
22	IPC16P008B	IPC16	DEV	MOD		Blank Card With Capacity For 8kx16 Of ROM/PROM Used In Development Sys	NSC
23	IPC16P008P	IPC16	DEV	MOD	MPG	PACE Development System 8kx16 ROM/PROM Card	NSC
24	IPC16P100	IPC16	DEV	MOD	MPG	IMP 16/PACE Conversion Card Or PACE Development System CPU Card	NSC
25	IPC16P805	IPC16	DEV	MOD		PROM Programmer Card	NSC
26	IPC16P108	IPC16	DEV	UNIT	MPG	Basic PACE Development System With 8k Memory;Other Memory Size Opt Avail	NSC
27	IPC16P301	IPC16	DEV	UNIT		PACE Low Cost Development System For Application Systems,20 Key Keypad	NSC
28	IPC16P	IPC16	DEV	UNIT	MPG	Microprocessor Development System	NSC
29	IPC16P004T	IPC16	IO-03	MOD		Memory Timing And Control Card	NSC
30	DP8300N	IPC16	IO-21	Chip		Bus Transceiver Element	NSC
31	DP8302J	IPC16	IO-32	Chip		OSC,CPU Clock Driver,TTL Sys Clocks in 16-Pin Cavity DIP;2.6667MHz Xtal	NSC
32	DP8302N	IPC16	IO-32	Chip		Osc,CPU Clock Driver,TTL Sys Clocks in 16 Pin Plastic DIP;2.6667MHz Xtal	NSC
33	DP8305J	IPC16	IO-32	Chip		OSC,CPU Clock Driver,TTL Sys Clocks in 16-Pin Cavity DIP;4.0MHz Xtal	NSC
34	IPC16C800	IPC16	IO-33	MOD		General Purpose I/O Card,4 8 Bit Increments	NSC
35	IPC16P840	IPC16	PE-02	UNIT		PACE Disk Operating System,Peripheral To IMP And PACE MPU Dev Systems	NSC
36	IMP00/812	IPC16	PE-10	UNIT		High-Speed Printer;Centronics Model 306	NSC
37	IPC16P812	IPC16	PE-10	UNIT		Centronics Printer	NSC
38	IPC16P810	IPC16	PE-24	UNIT		ASR33 Teletype	NSC
39	IPC16P825	IPC16	PE-40	UNIT		Card Reader (Documentation M300)	NSC
40	IMP00/850	IPC16	PE-42	UNIT		High-Speed Paper Tape Reader	NSC
41	IPC16C001	IPC16	RAM	MOD	MPG	PACE Application Card With 1024x16 Static RAM Used W/IPC16C100 CPU	NSC
42	IPC16P004	IPC16	RAM	MOD	MPG	4096 16 Bit Dynamic RAM Storage	NSC
43	IPC16C001B	IPC16	ROM	MOD		Blank Card With Capacity For 1kx16 ROM/PROM	NSC
44	IPC16C001P	IPC16	ROM	MOD	MPG	PACE Application Card With 1024x16 ROM/PROM	NSC
45	IPC16C002B	IPC16	ROM	MOD		Blank Card With Capacity For 2kx16 Of ROM/PROM	NSC
46	IPC16C002P	IPC16	ROM	MOD	MPG	PACE Application Card With 2kx16 Of ROM/PROM	NSC
47	NS11/03	LSI11	RAM	MOD		16k x 16 Bit Memory Card;Hardware/Software Compatible W/PDP11/03,LSI11	NSC
48	INS1771D-1	MCP1600	IO-07	Chip	MNG	Floppy Disk Formatt/Controll;40 Pin Cer DIP Pkg,Replacem For FD1771 WDC	NSC
49	INS1771N-1	MCP1600	IO-07	Chip	MNG	Floppy Disk Format/Controll;40Pin PlasticDIP Pkg,Replace For FD1771 WDC	NSC
50	NSC800	NSC800	uCT	Chip	MNX	uProcessor on a Chip;Compatible With Z80 Instruction Set;10 Address Modes	NSC
51	INS8080AD	N8080A	CPU	Chip	MNG	8 Bit Microprocessor;2 usec Clock Cycle;Replacement For Intel 8080A	NSC
52	INS8080AD-1	N8080A	CPU	Chip	MNG	8 Bit Microprocessor;1.3 usec Clock Cycle	NSC
53	INS8080AD-2	N8080A	CPU	Chip	MNG	8 Bit Microprocessor;1.5 usec Clock Cycle	NSC
54	INS8228D	N8080A	IO-02	Chip	BTD	System Controller and Bus Driver	NSC
55	INS8238D	N8080A	IO-02	Chip	BTD	System Controller and Bus Driver	NSC
56	DP8350N	N8080A	IO-09	Chip	BIX	Progr CRT Contr Using Internal Mask Progr ROMs;TTL Compatible I/O	NSC
57	DP8228J	N8080A	IO-11	Chip	BXD	Sys Controller/Bus Driver;28-Pin DIL Glass/Glass Pkg	NSC
58	DP8228N	N8080A	IO-11	Chip	BXD	Sys Controller/Bus Driver;28-Pin DIL Plastic Pkg	NSC
59	DP8238J	N8080A	IO-11	Chip	BXD	Sys Controller/Bus Driver;28-Pin DIL Glass/Glass Pkg	NSC
60	DP8238N	N8080A	IO-11	Chip	BXD	Sys Controller/Bus Driver;28-Pin DIL Plastic Pkg	NSC
61	DP7304BJ	N8080A	IO-21	Chip	BXD	8-Bit Bidirectional Xceiver;3-State I/O Interfacing;20-Pin DIL Package	NSC
62	DP8216J	N8080A	IO-21	Chip	BXD	4-Bit Bidirectional Bus Transceiver;Non-Inverting 3-State Outputs;16-Pin	NSC
63	DP8226J	N8080A	IO-21	Chip	BXD	4-Bit Bidirectional Bus Transceiver;Inverting 3-State Outputs;16-Pin DIL	NSC
64	DP8304BJ	N8080A	IO-21	Chip	BXD	8-Bit Bidirectional Xceiver;3-State I/O Interfacing;20-Pin DIL Package	NSC
65	DP8304BN	N8080A	IO-21	Chip	BXD	8-Bit Bidirectional Xceiver;3-State I/O Interfacing;20-Pin DIL Package	NSC
66	INS8304N	N8080A	IO-21	Chip		8 Bit Bidirectional Transceiver;20 Pin Plastic DIP Pkg	NSC
67	INS8255D	N8080A	IO-30	Chip	MNG	Programmable Peripheral Interface;40 Pin Cer DIP Pkg	NSC
68	DP8224J	N8080A	IO-32	Chip	BXD	Clock Gen/Driver;Req External Xtal;16-Pin Glass/Glass DIL Pkg	NSC
69	DP8224N	N8080A	IO-32	Chip	BXD	Clock Gen/Driver;Req External Xtal;16-Pin Plastic DIL Pkg	NSC
70	INS8224J	N8080A	IO-32	Chip	BTD	Clock Generator and Driver;Ceramic DIP Pkg	NSC
71	INS8224N	N8080A	IO-32	Chip	BTD	Clock Generator and Driver;Molded DIP Pkg	NSC
72	DP8212J	N8080A	IO-33	Chip	BXD	8-Bit I/O Port W/8-Bit Latch,3-State Outs;24-Pin Glass/Glass DIL Pkg	NSC
73	DP8212N	N8080A	IO-33	Chip	BXD	8-Bit I/O Port W/8-Bit Latch,3-State Outs;24-Pin Plas DIL Pkg	NSC
74	INS8253	N8080A,SC/MP	IO-02	Chip		Programmable Interval Timer;3 Independent 16-Bit Counters	NSC
75	DP8350D	N8080A,SC/MP	IO-09	Chip	BIX	Progr CRT Contr Using Internal Mask Progr ROMs;TTL Compatible	NSC
76	INS8247	N8080A,SC/MP	IO-09	Chip		Display Controller;4 Digit,7 Segment Display;Controlled by 8 Data Bits	NSC
77	INS8248	N8080A,SC/MP	IO-09	Chip		Display Controller;6 Digit,7 Segment Display;7x16 ROM Contr by 4 Bits	NSC
78	INS8244	N8080A,SC/MP	IO-10	Chip		90 Key Keyboard Encoder	NSC
79	INS8245	N8080A,SC/MP	IO-10	Chip	BTD	16 Key Keyboard Encoder	NSC
80	INS8246	N8080A,SC/MP	IO-10	Chip	BTD	20 Key Keyboard Encoder	NSC
81	INS8250D	N8080A,SC/MP	IO-20	Chip	MNG	Asynchronous Communications Element;40 Pin Cer DIP Pkg	NSC
82	INS8250N	N8080A,SC/MP	IO-20	Chip	MNG	Asynchronous Communications Element;40 Pin Plastic DIP Pkg	NSC
83	INS8251D	N8080A,SC/MP	IO-20	Chip	MNG	Programmable Communications Interface;28 Pin Cer DIP Pkg	NSC
84	INS8208	N8080A,SC/MP	IO-21	Chip	BTD	8 Bit Bi-directional Bus Driver	NSC
85	INS8216J	N8080A,SC/MP	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver;Ceramic DIP Pkg	NSC
86	INS8216N	N8080A,SC/MP	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver;Molded DIP Pkg	NSC
87	INS8226J	N8080A,SC/MP	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver;Ceramic DIP Pkg	NSC
88	INS8226N	N8080A,SC/MP	IO-21	Chip	BTD	4 Bit Bi-Directional Bus Driver;Molded DIP Pkg	NSC
89	INS8254	N8080A,SC/MP	IO-30	Chip	BTD	Programmable Bit Addressable Interface	NSC
90	INS8202	N8080A,SC/MP	IO-31	Chip	BTD	8 Bit Bus Driver;Tri State	NSC
91	INS8203	N8080A,SC/MP	IO-31	Chip	BTD	8 Bit Bus Driver;Tri State;Inverting	NSC
92	INS8212J	N8080A,SC/MP	IO-33	Chip	BTD	8 Bit I/O Port;Ceramic DIP Pkg	NSC
93	INS8212N	N8080A,SC/MP	IO-33	Chip	BTD	8 Bit I/O Port;Molded DIP Pkg	NSC
94	INS82LS05	N8080A,SC/MP	IO-44	Chip	BTD	1 of 8 Binary Decoder for Data Routing or Memory Decoding	NSC
95	INS82C06	N8080A,SC/MP	IO-56	Chip		8-Bit Latch with 3-State Outputs	NSC
96	INS8154	N8080A,SC/MP	IO-57	Chip	BTD	128 x 8 Static RAM with 16 Bit I/O	NSC
97	BLC80/05	Series 80	COMP	MOD		Series 80 Board Level Computer;512 Bytes of Static RAM;8K Bytes of ROM	NSC
98	BLC80/07	Series 80	COMP	MOD		Series 80 Board Level Computer;512 Bytes of RAM;4k Bytes of PROM	NSC
99	BLC80/11T	Series 80	COMP	MOD		Series 80 Board Level Computer;BLC80/11 w/Ext Temp Rng(-40to85°C)	NSC
100	BLC80/12T	Series 80	COMP	MOD		Series 80 Board Level Computer;BLC80/12 w/Ext Temp Rng(-40to85°C)	NSC
101	BLC80/14T	Series 80	COMP	MOD		Series 80 Board Level Computer;BLC80/14 w/Ext Temp Rng(-40to85°C)	NSC
102	RMC80/10	Series 80	COMP	UNIT		Complete OEM Rack Mount Microcomputer with BLC80/10 CPU	NSC
103	RMC80/14	Series 80	COMP	UNIT		Complete OEM Rack Mount Microcomputer with BLC80/14 CPU	NSC
104	RMC80/204	Series 80	COMP	UNIT		Complete OEM Rack Mount Microcomputer with BLC80/204 CPU	NSC
105	BLC80/10	Series 80	CPU	MOD		Self Contained Single Bd Computer CPU,Sys Clk,1k RAM,4k PROM Sockets,I/O	NSC
106	BLC80/11	Series 80	CPU	MOD		Same as BLC80/10 with Sockets for Up to 8k PROM	NSC
107	BLC80/12	Series 80	CPU	MOD		Same as BLC80/11 with 2k Bytes RAM	NSC
108	BLC80/14	Series 80	CPU	MOD		Same as BLC80/11 with 4k Bytes RAM	NSC
109	BLC80/204	Series 80	CPU	MOD		Same as BLC80/14 with Bus Contr;8 Vectored Interrupt Capability	NSC
110	BLC80P	Series 80	DEV	MOD	MXX	Prototyping Package-Complete System for OEM Development	NSC

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	BLC910	Series 80	DEV	MOD	MXX	System Monitor with 2 Preprogrammed MM2708 EPROMs	NSC
2	BLC8610	Series 80	DEV	MOD		Extender Card with Switched Power	NSC
3	BLC80P/14	Series 80	DEV	MODS		Prototyping Kit Using 80/14 CPU	NSC
4	SPX80/40	Series 80	DEV	UNIT		STARPLEX DEV SYS;Keybd,Printer,CRT Monitor,Floppy Disk Drive Module Units	NSC
5	BLC501	Series 80	IO-03	MOD		Interrupt Priority Switch Selectable to 8 Levels	NSC
6	BLC8221	Series 80	IO-07	MOD		Floppy Disk Controller;Up to 4 Single or 2 Dual Sided Drives	NSC
7	BLC8229	Series 80	IO-09	MOD		CRT Controller/Keybd Interface;CRT Buffer Mem for 24 Lines of 8 Charact	NSC
8	BLC8534	Series 80	IO-23	MOD		Channel Control is Exercised Using Standard Series 80 Instructions/USART	NSC
9	BLC8538	Series 80	IO-23	MOD		8 Channel BLC8534	NSC
10	BLC508	Series 80	IO-33	MOD	MXX	I/O Expansion Board;4 8Bit Input,4 8Bit Output Ports	NSC
11	BLC517	Series 80	IO-33	MOD	MXX	Combination I/O Expansion Board	NSC
12	BLC610	Series 80	IO-33	MOD	MXX	Extender Board	NSC
13	BLC104	Series 80	IO-57	MOD	MNG	Mem-I/O Expansion Bd;4kx8 RAM;Up to 8k ROM;48 Programmable I/O	NSC
14	BLC116	Series 80	IO-57	MOD	MNG	Mem-I/O Expansion Bd;16kx8 RAM;Up to 8k ROM;48 Programmable I/O	NSC
15	BLC556	Series 80	IO-92	MOD		Optically Isolated Input/Output Board;Protects Sys from Ext Volt to 500V	NSC
16	BLC905	Series 80	IO-92	MOD	MXX	Universal Prototyping Board for BLC80P Prototyping Package	NSC
17	BLC530	Series 80	IO-92	UNIT		Current Loop Adapter;Current Loop Conv For RS232C Serial I/O Channels	NSC
18	BLC635	Series 80	PE-60	MOD		Power Supply for BLC 80 Bds;100 to 230VAC,50-60Hz	NSC
19	BLC655	Series 80	PE-60	MOD		Heavy Duty Pwr Supply;Twice Rated Curr of BLC635;For BLC80/10,7 Exp Bds	NSC
20	BLC016	Series 80	RAM	MOD		16k x 8 RAM;Uses MM5271	NSC
21	BLC032	Series 80	RAM	MOD		32kx8 RAM Board;Uses 16k Dynamic RAM Components	NSC
22	BLC048	Series 80	RAM	MOD		48kx8 RAM Board;Uses 16k Dynamic RAM Components	NSC
23	BLC064	Series 80	RAM	MOD		64kx8 RAM Board;Uses 16k Dynamic RAM Components	NSC
24	BLC8016	Series 80	RAM	MOD		On-Board Refresh and Control Logic;8 or 16 Bit Data Access;Aux Power Bus	NSC
25	BLC406	Series 80	ROM	MOD	MPX	6kx8 ROM/PROM;Uses 1302 ROM And 1702 PROM	NSC
26	BLC416	Series 80	ROM	MOD	MNG	16kx8 ROM/EPROM Expansion Bd;Up to 16 2308 ROMs or 2708 PROMs	NSC
27	BLC8432	Series 80	ROM	MOD	MNG	32kx8 ROM/EPROM Expansion Bd;Up to 16 2316 ROMs or 2716 PROMs	NSC
28	INS8060D	SC/MP	CPU	Chip	MNG	8 Bit Single Chip Microprocessor;40 Pin Cer DIP Pkg	NSC
29	INS8060N	SC/MP	CPU	Chip	MNG	8 Bit Single Chip Microprocessor;40 Pin Plastic DIP Pkg	NSC
30	ISP8C100	SC/MP	CPU	MOD		CPU Application Card With 256x8 RAM,512x8 ROM/PROM	NSC
31	ISP8P301	SC/MP	DEV	UNIT		Low Cost Development System With Application Cards And Keyboard	NSC
32	DS3654	SC/MP	IO-08	Chip		Printer Solenoid Driver;Serial Input;10 Open-Coll 300mA Output Drivers	NSC
33	ISP8A551	SC/MP	IO-31	Chip	MPG	Buffer Element	NSC
34	DM74LS175	SC/MP	IO-56	Chip		Quad Latch	NSC
35	ISP8A543	SC/MP	IO-56	Chip	MPG	Interface Latch Element	NSC
36	ISP8C002	SC/MP	RAM	MOD		2kx8 Bit Static RAM Application Card	NSC
37	ISP8C004B	SC/MP	ROM	MOD		4k By 8 ROM/PROM Socket Application Card	NSC
38	ISP8C004P	SC/MP	ROM	MOD		4kx8 Bit ROM/PROM Application Card	NSC
39	INS2651D	2650	IO-20	Chip	MNG	Programmable Communication Interface;Ceramic DIP Pkg	NSC
40	INS2651N	2650	IO-20	Chip	MNG	Programmable Communication Interface;Plastic DIP Pkg	NSC
41	INS8035	8048	uCT	CHIP	MNG	uProcessor on a Chip;64Bytes of RAM,N/A ROM;27I/O Lines	NSC
42	INS8039	8048	uCT	CHIP	MNG	uProcessor on a Chip;128Bytes of RAM,N/A/ ROM;27I/O Lines	NSC
43	INS8040	8048	uCT	CHIP	MNG	uProcessor on a Chip;256Bytes of RAM,N/A/ROM;27I/O Lines	NSC
44	INS8048	8048	uCT	CHIP	MNG	uProcessor on a Chip;64Bytes Of RAM,1.0k ROM; 27I/O Lines	NSC
45	INS8049	8048	uCT	CHIP	MNG	uProcessor on a Chip;128Bytes of RAM,2.0k ROM;27 I/O Lines	NSC
46	INS8050	8048	uCT	CHIP	MNG	uProcessor on a Chip;256Bytes of RAM,4.0k ROM;27I/O Lines	NSC
47	INS8243	8048	IO-33	CHIP	MNG	Input/Output Expander;XMOS Technology;Direct Expansion Of INS8048/49/50	NSC
48	INS8070	8070	uCT	CHIP	MNG	uProcessor on a Chip;64Bytes of RAM,No ROM;On-Chip Clock Generation	NSC
49	INS8072	8070	uCT	CHIP	MNG	uProcessor on a Chip;64Bytes Of RAM,2.5k ROM;On-Chip Clock Generation	NSC
50	OP-80A	OAE Series	PE-42	UNIT		0-5000CPS Tape Reader W/8-Bit Parallel Port for UPROC Interface	OAE
51	PP-2532	OAE Series	PE-50	UNIT		Programs the TMS2532 5V Only EPROM	OAE
52	PP-2708	OAE Series	PE-50	UNIT		Programs the 2708 Family of EPROMS	OAE
53	PP-2708/16	OAE Series	PE-50	UNIT		Programs TMS2716,TMS27L16 and 2708 Family EPROMS;Requires Ready/Wait Line	OAE
54	PP-2716	OAE Series	PE-50	UNIT		Programs Intels 2716 5V Only EPROM and The TMS2516	OAE
55	PP-2732	OAE Series	PE-50	UNIT		Programs Intels Edge-Triggered 5V Only Low Power 4k Byte EPROM	OAE
56	PP-T2716	OAE Series	PE-50	UNIT		Programs TMS2716 and TMS27L16 EPROMS	OAE
57	UPP-2700	OAE Series	PE-50	UNIT		Tests and Duplicates 1 to 16 EPROMS Simultaneously	OAE
58	UVS-11E	OAE Series	PE-51	UNIT		EPROM Erasing Lamp/Will Erase Up to 4 Chips at One Time in 20 Minutes	OAE
59	PCG	OBJ-S100	IO-92	MOD		Programmable Char Gen;Adds Software Created Characters to Video Display	OBJ
60	VDI	OBJ-S100	IO-92	MOD		Video Display Interface;Formats Selected By Software	OBJ
61	DB00A	OBJ-S100	PE-50	MOD		PROM Programming/Storage Card;For TMS2716,2708, and 27L08 PROMS	OBJ
62	DB08A	OBJ-S100	PE-50	MOD		PROM Programming/Storage Card;With 1k RAM;For TMS2716,2708,and 27L08 PROM	OBJ
63	DB16A	OBJ-S100	PE-50	MOD		PROM Programming/Storage Card;With 2k RAM;For TMS2716,2708,and 27L08 PROM	OBJ
64	CD23	C2#2,C3		UNIT		29 Megabyte Shugart Disk,Interface w/Mem Bd 0565U	OHS
65▼	CA9D	C2#2,C3	IO-08	MOD		Parrallel Centronics Line Printer IF w/Cable	OHS
66	CA10X	C2#2,C3	IO-20	MOD		16 Port Serial Board:RS232 and/or Hi Speed Synchronous	OHS
67▼	CA10N5	C2#2,C3	IO-57	MOD		CA10X Port Bd;4 Cluster Commun Ports/1 Network Commun Port at 500 Bound	OHS
68▼	CA17	C2#2,C3	IO-57	MOD		8k 2MHz RAM/1 Cluster Port/1 Aux RS232 Port	OHS
69▼	CA18	C2#2,C3	IO-57	MOD		1 Centronics Parrallel Printer Port w/Cable;	OHS
70▼	CA18A	C2#2,C3	IO-57	MOD		1 Centronics Parrallel Printer Port w/Cable w/8k 2MHz RAM/2 RS232 Ports	OHS
71▼	CA20	C2#2,C3	IO-57	MOD		8-Port I/O Bus and Calen Clk;IF for 8 Head end Cards/Battery Backup	OHS
72▼	CA20A	C2#2,C3	IO-57	MOD		8-Port I/O Bus;IF for 8 Head end Cards/Battery Backup	OHS
73▼	CA21	C2#2,C3	IO-57	MOD		48 Parrallel Lines I/O	OHS
74▼	CA14A	C2#2,C3	IO-92	MOD		Voice I/O Bd w/VORTAX Voice Mod;Enables Computer to Talk	OHS
75	CD74	C2#2,C3	PE-02	UNIT		74 Megabyte Hard Disk Drive,and Interface W/Mem Bd,OS65U	OHS
76	AC-9TP	C2#2,C3	PE-10	UNIT		Centronics 779,110cps Printer,Tractor Feed,Interface	OHS
77	AC-14	C2#2,C3	PE-10	UNIT		Word Processing Printer W/Interface	OHS
78▼	AC7B	C2#2,C3	PE-23	UNIT		Hazeltine 1500 CRT Terminal;U/Lower Case;80 Colx24 Lines;XY Adder	OHS
79	4KP	C2#2,C3	RAM	Chip		Adds 4k RAM to C1P And C2-4P(Static)	OHS
80	CM2	C2#2,C3	RAM	MOD		4k Static RAM,2.0MHz,Low Power,2102 Based	OHS
81▼	CM3A	C2#2,C3	RAM	MOD		16k Static RAM 1.5MHz;Access Time 215ns;Pwr Down Module	OHS
82	CM4	C2#2,C3	RAM	MOD		16k Dynamic RAM;1.0MHz,4027 Based,Ultra Low Cost	OHS
83	CM6	C2#2,C3	RAM	MOD		48k Dynamic RAM,1.0MHz,20 Address Bits	OHS
84	CM9	C2#2,C3	RAM	MOD		24k Static ram,High Density,20 Address Bits	OHS
85▼	CA22	C2#2C3	IO-57	MOD		High Speed Analog I/O Module;2 12 Bit D/A Converters;1 12/8 Bit A/D Conv	OHS
86▼	CA24	C2#2C3	IO-57	MOD		Prototyping Bd Solderless IF;PIA/TTL I/O	OHS
87▼	CA25	C2#2C3	IO-57	MOD		Security/AC Remote IF;Home Security	OHS
88▼	CA15	C2#2C3	IO-92	MOD		Univer Telephone IF	OHS
89▼	CA15B	C2#2C3	IO-92	MOD		Univer Telephone IF;w/VOTRAX Voice	OHS
90▼	AC3P	C2#2C3	PE-15	UNIT		Video Monitor;9in Diagonal Screen	OHS
91▼	AC5A	C2#2C3	PE-24	UNIT		OKI Data Model 0-22 Printer/IF;125lpm;8 Char Sizes 132 Cal	OHS
92▼	CA23	C2#2C3	PROM	MOD		PROM Blasters;Program 2758/2716/2732/2764;8-65k EPROMs	OHS
93	C3-A	C3	COMP	UNIT		8 Bit Microcomp CHALLENGER III:Uses 6502A,68B00,Z80,48k Static RAM	OHS
94	C3-B	C3	COMP	UNIT		8 Bit Microcomp CHALLENGER III:Uses 6502A,68B00,Z80;52k Static RAM	OHS
95	C3-C	C3	COMP	UNIT		8 Bit Microcomp CHALLENGER III:Uses 6502A,68B00,Z80;52k Static RAM	OHS
96	C3-OEM	C3	DEV	UNIT		8 Bit Microcomp W/32k Static RAM:3 CPUs 6502,6800,Z80	OHS
97♦	CM-10	C3	RAM	MOD		8k Static RAM For Expanding C3s	OHS
98#	LKIT16	LKIT16	DEV	MOD	MNG	16 Bit Microcomputer Kit;Uses MN1610A,500W RAM,1kW ROM,Keyboard	PAFJ
99#	CMTTYIF	LKIT16	IO-04	MOD		Philips Cassette and TTY Interface	PAFJ
100#	PRIF	LKIT16	IO-08	MOD		EUY-10E Printer Interface	PAFJ
101#	TVIF	LKIT16	IO-09	MOD		TV Interface	PAFJ
102#	TVIFOP	LKIT16	IO-10	MOD		Color TV and Full Keyboard Interface	PAFJ
103#	EXMEM	LKIT16	IO-55	MOD		Expandable Memory Board	PAFJ
104#	OBC1A	PFL16A	COMP	MOD	MNG	16 Bit One Board Computer Card;Uses MN1610CPU;Std Type	PAFJ
105#	OBC2A	PFL16A	COMP	MOD	MNG	16 Bit One Board Computer Card;Uses MN1610CPU;Word Subchannel I/F	PAFJ
106#	OBC3A	PFL16A	COMP	MOD	MNG	16 Bit One Board Computer Card;Uses MN1610CPU;Battery Supportable	PAFJ
107#	MN1610	PFL16A	CPU	Chip	MNG	16 Bit Microprocessor	PAFJ
108#	CPUA	PFL16A	CPU	MOD	MNG	16 Bit CPU Card;Uses MN1610 CPU	PAFJ
109#	CPUOPA	PFL16A	CPU	MOD	MNG	16 Bit CPU Option Card	PAFJ
110#	MN1630	PFL16A	IO-02	Chip	MNG	Subchannel Adapter;8 Bit Programmed Interface	PAFJ

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1#	MN1640	PFL16A	IO-02	Chip	MNG	Real Time System Controller	PAFJ
2#	MN1650	PFL16A	IO-02	Chip	MNG	DMA Channel Controller for 4 Subchannels	PAFJ
3#	BDMAA	PFL16A	IO-03	MOD	MNG	Byte DMA Subchannel Card	PAFJ
4#	DMACA	PFL16A	IO-03	MOD	MNG	DMA Channel Card	PAFJ
5#	WDMAA	PFL16A	IO-03	MOD	MNG	Word DMA Subchannel Card	PAFJ
6#	BIOC3A	PFL16A	IO-04	MOD	MNG	Basic I/O Controller Card for PF2061A and TTY	PAFJ
7#	BIOC2A	PFL16A	IO-06	MOD	MNG	Basic I/O Controller Card for PF2061A and F807A TW	PAFJ
8#	FDC1A	PFL16A	IO-07	MOD	MNG	Floppy Disk Controller Card	PAFJ
9#	ASAA	PFL16A	IO-20	MOD	MNG	Asynchronous Adapter Card	PAFJ
10#	BSAA	PFL16A	IO-20	MOD		Binary Synchronous Adapter Card	PAFJ
11#	SIAA	PFL16A	IO-20	MOD		Serial Interface Adapter Card;Provides RS232 Interface and 20mA Loop	PAFJ
12#	BUSAMPAA	PFL16A	IO-21	MOD		Microbus Amp Card	PAFJ
13#	DIA	PFL16A	IO-33	MOD		Digital Input Card with 64 Interface Lines	PAFJ
14#	DOA	PFL16A	IO-33	MOD		Digital Output Card with 64 Interface Lines	PAFJ
15#	IBAA	PFL16A	IO-33	MOD		IEC Bus Adapter Card	PAFJ
16#	PLCA1B	PFL16A	IO-33	MOD		Parallel Line Communication Adapter Card with Terminations	PAFJ
17#	PLCA2B	PFL16A	IO-33	MOD		Parallel Line Communication Adapter Card	PAFJ
18#	PLCA3A	PFL16A	IO-33	MOD		Parallel Line Communication Adapter Card;50mA Option Card	PAFJ
19#	CRM2KW	PFL16A	IO-55	MOD		2k Word Core Mem Card	PAFJ
20#	CRM8KW	PFL16A	IO-55	MOD		8k Word Core Mem Card	PAFJ
21#	MDOPA	PFL16A	IO-90	MOD		Multiply/Divide Operation Card	PAFJ
22#	BPMA	PFL16A	IO-92	MOD	MNG	Byte PM Subchannel Card	PAFJ
23#	PNLCA	PFL16A	IO-92	MOD		Panel Control Card	PAFJ
24#	PROMWA	PFL16A	IO-92	MOD	MNG	PROM Writer Card for 2708	PAFJ
25#	WPMA	PFL16A	IO-92	MOD	MNG	Word PM Subchannel Card	PAFJ
26#	PF2050A	PFL16A	PE-01	UNIT		Floppy Disk Drive Unit	PAFJ
27#	PF2061A	PFL16A	PE-42	UNIT		400/480 Character Paper Tape Reader	PAFJ
28#	PF2091A	PFL16A	PE-60	UNIT		Power Supply Unit for PFL16A Std Card System	PAFJ
29#	PF2090C2	PFL16A	PE-61	UNIT		Programmer Panel	PAFJ
30#	PF2090C	PFL16A	PE-61	UNIT		Console Panel	PAFJ
31#	ICRAM2KW	PFL16A	RAM	MOD		2k Word IC RAM Card	PAFJ
32#	ICRAM8KW	PFL16A	RAM	MOD		8k Word IC RAM Card	PAFJ
33#	ICROM1A	PFL16A	ROM	MOD		IC ROM Card up to 8k Word	PAFJ
34	EQUINOX-100	EQUINOX-100	COMP	UNIT		8 Bit Microcomputer System:Uses 8080A CPU	PAR
35	ECONORAMIII	EQUINOX-100	IO-57	MOD		8192x8 Mem Board W/Synchro Fresh Refreshing System,tac 250ns	PAR
36	KRATION	EQUINOX-100	IO-57	MOD		4096x8 Mem Board,Static,Cycle Time 450ns,Acc Time 450ns	PAR
37	T8	T8	DEV	UNIT		Microcomputer System Analyzer;Hexadecimal Keyboard;8 1/2 Digit Display	PAT
38	PM0	T8	10-92			Blank Programing Matrix	PAT
39	PM1	T8	10-92			Programing Matrix to Interface with the 8080 FΔmfly	PAT
40	PM2	T8	10-92			Programing Matrix to Interface with the Z80 Microprocessor	PAT
41	PM3	T8	10-92			Programing Matrix to Interface with the 2650 Microprocessor	PAT
42	PM4	T8	10-92			Programing Matrix to Interface with the 7.0 or 2.0MHz 6501 Microprocessor	PAT
43	PM5	T8	10-92			Programing Matrix to Interface with the 1.0 or 2.0MHz 6502 Microprocessor	PAT
44	PM6	T8	10-92			Programing Matrix to Interface with the 1.0 or 2.0MHz 6505 Microprocessor	PAT
45	PM8	T8	10-92			Programing Matrix to Interface with the SCAMP II (8060)	PAT
46	PM9	T8	10-92			Programing Matrix to Interface with the 8085 Microprocessor	PAT
47	12010	PCM-12A	CPU	MOD		Processor Card;Includes IM6100I CPU,4MHz Clock,Baud-Rate Generator	PCM
48	PCM-12kit	PCM-12A	DEV	UNIT		System Kit;Includes 12010 CPU,12030 Front Panel,And Power Supply	PCM
49	12060	PCM-12A	IO-04	MOD		TTY/CRT Interface Module;Provides RS-232 Interface And 20MA Loop	PCM
50	12080	PCM-12A	IO-05	MOD		Audio Cassette Recorder Interface	PCM
51	12070	PCM-12A	IO-06	MOD		High Speed Paper-Tape Reader/Punch Interface Module	PCM
52	12440	PCM-12A	IO-07	MOD		Floppy-Disk Interface Module;Compatible W/Data Sys Model 210 Floppy Disk	PCM
53	12030	PCM-12A	IO-10	MOD		Front Panel Module;Implements PDP-8/E Style Control Panel	PCM
54	12310	PCM-12A	IO-33	MOD		Parallel I/O Interface;Identical With DEC DR8-EAI/O For PDP-8/E	PCM
55	12020	PCM-12A	IO-55	MOD		4k-Word Static Memory Made Up Of 48 1k-Bit Memory Units	PCM
56	12040	PCM-12A	IO-55	MOD		Memory Extender Module;Extends Memory To 32k Words	PCM
57	12160	PCM-12A	IO-55	MOD		EPROM/RAM Combination;1.5k Words Erasable PROM,512 Words Static RAM	PCM
58	12230	PCM-12A	PE-60	MOD		Power Fail Module;Automatically Restores All Program Parameters	PCM
59	12900	PCM-12A	PE-60	MOD		Power Supply Mod;5V at 12 Amp,±12V at 1.7Amp	PCM
60	12210	PCM-12A	RAM	MOD	MCX	4k Words Non-Volatile RAM W/Re-Chargeable Battery Backup	PCM
61	12410	PCM-12A	RAM	MOD		8k Word Dynamic RAM	PCM
62	MICROPAC80A	MICROPAC80A	COMP	UNIT		8 Bit System Uses Intel 8080	PCS
63	CM4400	MICROPAC80A	CPU	MOD		Uses Intel 8080 MPU;8 Bit Parallel Processor	PCS
64	PM5010	MICROPAC80A	IO-01	MOD		16 Bit Digital Up/Down Counter Module	PCS
65	PM5012	MICROPAC80A	IO-01	MOD		16 Bit Interval Timer Module	PCS
66	PM5008	MICROPAC80A	IO-02	MOD		8 Channel Interrupt Expander Module	PCS
67	PM5080	MICROPAC80A	IO-04	MOD		TTY Controller Module;20mA Control Loop Data Transfer	PCS
68	PM5081	MICROPAC80A	IO-20	MOD		Serial-To-Parallel/Parallel-To-Serial Converter Compatible Controller	PCS
69	PM5082	MICROPAC80A	IO-20	MOD		8 Bit Serial/Parallel Converter Module	PCS
70	PM5009	MICROPAC80A	IO-31	MOD		8 Channel Relay Output Module	PCS
71	PM5011	MICROPAC80A	IO-32	MOD		Real Time Clock Module	PCS
72	PM5013	MICROPAC80A	IO-32	MOD		Real Time Clock And Power Fail Detect Module	PCS
73	PM5001	MICROPAC80A	IO-33	MOD		16 Bit Digital Input/Output Module	PCS
74	PM5004	MICROPAC80A	IO-33	MOD		16 Bit High Level Digital Input/Output;5-50V Inputs	PCS
75	PM5005	MICROPAC80A	IO-33	MOD		16 Bit High Level Digital Input/Output;Signals Up To 50V At 500mA	PCS
76	PM5006	MICROPAC80A	IO-33	MOD		16 Bit Optically Digital Input/Output	PCS
77	PM5007	MICROPAC80A	IO-33	MOD		16 Bit Optically Digital Input/Output	PCS
78	PM5021	MICROPAC80A	IO-40	MOD		2 Channel 12 Bit Digital-Analog Converter	PCS
79	PM5051	MICROPAC80A	IO-40	MOD		12 Bit Digital To Analog Converter Module	PCS
80	PM5054	MICROPAC80A	IO-41	MOD		16 Channel 12 Bit Analog-To-Digital Converter Module	PCS
81	CM4500	MICROPAC80A	IO-55	MOD		1k RAM,1k ROM Memory Module	PCS
82	CM4501	MICROPAC80A	IO-55	MOD		4k RAM In 1k Byte Increments Memory Module	PCS
83	CM4503	MICROPAC80A	IO-55	MOD		4k ROM In 256 Byte Increments Memory Module	PCS
84	PM5020	MICROPAC80A	IO-92	MOD		2 Channel 12 Bit Stepping Motor Controller Module	PCS
85	DS1000	MICROPAC80A	PE-01	UNIT		Floppy Diskette	PCS
86	VT1001	MICROPAC80A	PE-23	UNIT		Video Display Terminal;14in CRT;80 Char x 24 Lines	PCS
87	LP1001	MICROPAC80A	PE-24	UNIT		Line Printer;80 Column Line Printer W Software Driver Mod	PCS
88	PH1000	MICROPAC80A	PE-42	UNIT		Paper Tape Punch;Includes PM5001 Mod And Software Pkg	PCS
89	PR1000	MICROPAC80A	PE-42	UNIT		High Speed Paper Tape Reader;300 CPS;Includes PM5001 Mod	PCS
90	PB1000	MICROPAC80A	PE-50	UNIT		PROM Programmer	PCS
91	PB1001	MICROPAC80A	PE-50	UNIT		EROM Programmer:Programs 2708 EROMs in 2 Minutes	PCS
92	PM5100	MICROPAC80A	PE-61	MOD		Microcomputer Control Panel Set	PCS
93	PCS1880	PCS1880	COMP	MOD		8 Bit Single Board Microcomputer Using Z80A CPU;8MHz Clock	PCS
94	PCS1880A	PCS1880	COMP	MOD		8 Bit Single Board Microcomputer Using Z80A CPU W/Math Chip AMD9511	PCS
95	PCS1893	PCS1880	IO-92	MOD		Power Fail Module:2 TTL Comp Signals for AC Power Failure and Reset	PCS
96	PCS1806	SUPERPAC180	COMP	MOD		8 Bit Single Board Microcomputer;Uses 8080A CPU	PCS
97	PCS1810	SUPERPAC180	COMP	MOD		8 Bit Single Board Microcomputer;Uses 8080A CPU	PCS
98	PCS1810A	SUPERPAC180	COMP	MOD		8 Bit Single Board Microcomputer;Uses 8080A CPU;Contains 1k RAM	PCS
99	SPDS	SUPERPAC180	COMP	UNIT		SUPERPAC Microcomp Devel Syst;Designed to Support 8080A,Based Systems	PCS
100	SUPERPAC180	SUPERPAC180	COMP	UNIT		8 Bit Microcomp Syst;W/Front Panel CRT Display;3 Options As MICROPAC180	PCS
101	MPDS1	SUPERPAC180	DEV	UNIT		Microcomputer Development System;Teleprinter Based	PCS
102	MPDS2	SUPERPAC180	DEV	UNIT		Microcomputer Development System;Dual Cassette Silent Printer Based	PCS
103	MPDS3	SUPERPAC180	DEV	UNIT		Microcomputer Development System;Floppy Disc Based	PCS
104	PCS1812	SUPERPAC180	IO-09	MOD		CRT/Keyboard Interface Module;Software Control Of Screen Format	PCS
105	PCS1860	SUPERPAC180	IO-20	MOD		Quad Serial Port Module,4 Asynch Full Duplex Serial Ports,Programmable	PCS
106	PCS1804	SUPERPAC180	IO-33	MOD		AC/DC I/O Module;Controls 16 I/O Circuits	PCS
107	PCS1805	SUPERPAC180	IO-33	MOD		General Purpose I/O Module;Includes 1k Byte RAM;4 Interrupts	PCS
108	PCS1820	SUPERPAC180	IO-33	MOD		High Level Digital I/O Mod;32 I/Os	PCS
109	PCS1823	SUPERPAC180	IO-33	MOD		TTL I/O Module;64 TTL Inputs/Outputs	PCS
110	PCS1821	SUPERPAC180	IO-40	MOD		Optically Isolated Digital Input Module;32 Inputs,1500V Isolation	PCS

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE
1	PCS1825	SUPERPAC180	IO-40	MOD		Optically Isolated AC Output Module;16A.C. Outputs,Two 8 Bit Ports	PCS
2	PCS1830	SUPERPAC180	IO-40	MOD		Relay Output Module:16 Relay Outputs in Two 8 Bit Ports,5V Coils	PCS
3	PCS1850	SUPERPAC180	IO-41	MOD	MCX	CMOS A/D Module;16 Single Ended Inputs	PCS
4	PCS1850A	SUPERPAC180	IO-41	MOD	MCX	CMOS A/D Module;16 Single Ended Inputs With Analog Outputs	PCS
5	PCS1850B	SUPERPAC180	IO-41	MOD	MCX	CMOS A/D Module;16 Single Ended Inputs With Programmable Gain	PCS
6	PCS1850C	SUPERPAC180	IO-41	MOD	MCX	CMOS A/D Module;16 Single Ended Inputs With Analog Out,Program Gain	PCS
7	PCS1850D	SUPERPAC180	IO-41	MOD	MCX	CMOS A/D Module;8 Multiplexed Differential Analog Inputs	PCS
8	PCS1850E	SUPERPAC180	IO-41	MOD	MCX	CMOS A/D Module;8 Mux Diff Inputs With Analog Outputs	PCS
9	PCS1850F	SUPERPAC180	IO-41	MOD	MCX	CMOS A/D Module;8 Mux Diff Inputs With Programmable Gain	PCS
10	PCS1850G	SUPERPAC180	IO-41	MOD	MCX	CMOS A/D Module;8 Mux Diff Inputs W/Analog Out,Program Gain	PCS
11	PCS1851	SUPERPAC180	IO-41	MOD	MCX	CMOS A/D Module;16 se/8 Mux Diff Analog Input Ch;12 Bit Resolution	PCS
12	PCS1813	SUPERPAC180	IO-55	MOD		Memory W/4k Bytes RAM Expandable To 16k;Provision For 16k Bytes EROM/ROM	PCS
13	PCS1814	SUPERPAC180	RAM	MOD		Memory W/4k Bytes RAM Expandable To 8k;Battery Back Up	PCS
14▼#	N82S104		IO-01	Chip	BTX	Prog Logic Sequencer;Contain Logic and/or Gate Array;Open Coll Output	PHIN
15▼#	N82S105		IO-01	Chip	BTX	Prog Logic Sequencer;Contain Logic and/or Gate Array;Tri-State Output	PHIN
16▼#	S82S104		IO-01	Chip	BTX	Prog Logic Sequencer;Contain Logic and/or Gate Array;Open Coll Output	PHIN
17▼#	S82S105		IO-01	Chip	BTX	Prog Logic Sequencer;Contain Logic and/or Gate Array;Tri-State Output	PHIN
18	2650A-1I	2650	CPU	Chip	MNG	8 Bit Microprocessor;Cycle Time 1.5us;Ceramic DIP	PHIN
19#	2650A-1N	2650	CPU	Chip	MNG	8 Bit Microprocessor;Cycle Time 1.5us;Plastic DIP	PHIN
20	2650AI	2650	CPU	Chip	MNG	8 Bit Microprocessor;Cycle Time 2.4us;Ceramic DIP	PHIN
21#	2650AN	2650	CPU	Chip	MNG	8 Bit Microprocessor;Cycle Time 2.4us;Plastic DIP	PHIN
22#	2650B-1I	2650	CPU	Chip	MNG	High Speed Version of 2650B;Ceramic DIP	PHIN
23#	2650B-1N	2650	CPU	Chip	MNG	High Speed Version of 2650B;Plastic DIP	PHIN
24#	2650BI	2650	CPU	Chip	MNG	Variation of 2650A;More Powerful;Easier to Use;Ceramic DIP	PHIN
25#	2650BN	2650	CPU	Chip	MNG	Variation of 2650A;More Powerful;Easier to Use;Plastic DIP	PHIN
26#	2650PC4000	2650	DEV	MOD	MNG	PC-bd Emulator;Emulates 2656 Mem Interface Chip	PHIN
27#	2636I	2650	GAME	Chip	MNG	Prog Video IF For uProc Controlled Game Sys;40-Pin Cer DIP	PHIN
28#	2636N	2650	GAME	Chip	MNG	Prog Video for IF uProc Controlled Game Sys;40 Pin Plastic DIP	PHIN
29#	2621	2650	IO-02	Chip	MNG	Universal Sync Gen Timing/Control;TV Video PAL Format;(for Video Games)	PHIN
30#	2622	2650	IO-02	Chip	MNG	Universal Sync Gen Timing/Control;TV Video NTSC Format;(for Video Games)	PHIN
31#	2653I	2650	IO-02	Chip	MNG	Poly Gen Checker;6,7,8 Bit,128 Charac;Ceramic DIP;Compatible W/2651,52,61	PHIN
32#	2653N	2650	IO-02	Chip	MNG	Poly Genz Checker;Plastic DIP;Complements R/T,USART,USRT,UART	PHIN
33#	2651N	2650	10-01	Chip	MNG	Program Commun IF;Int or Ext Baud Rate Clock;Full or Half Duplex Oper	PHIN
34#	2621I	2650	10-02	Chip	MNG	Univ Sync Gen Time/Cont;TV Video PAL Format (Video Games)Cer DIP	PHIN
35#	2621N	2650	10-02	Chip	MNG	Univ Sync Gen Time/Cont;TV Video PAL Format(Video Games)Plas DIP	PHIN
36#	2622I	2650	10-02	Chip	MNG	Univ Sync Gen Time/Cont;TV Video NTSC Format(Video Games)Cer DIP	PHIN
37#	2622N	2650	10-02	Chip	MNG	Univ Sync Gen Time/Cont;TV Video NTSC Format (Video Games) Plastic DIP	PHIN
38#	2651I	2650	10-20	Chip		Programmable Communication Interface	PHIN
39#	2652I	2650	10-20	Chip		Multi Protocol Communications Cont Data Rate DC to 500Kbs	PHIN
40#	2655N	2650	10-33	Chip	MNG	Prog Peripheral IF;3 Ports W/24 Prog I/O Pins;300ns Read/Write Acc Time	PHIN
41#	N8T26AN	3000	10-21	Chip	BTX	Quad Bus Transceiver;Tri-State for Inverting Output	PHIN
42#	N8T28N	3000	10-21	Chip	BTX	Quad Bus Transceiver;Non-Inverting Output Tri-State	PHIN
43#	N74S182N	3000	10-90	Chip	BTX	High Speed Look Ahead Carry Generator	PHIN
44#	8021I	8048	uCT	Chip	MNG	Single-Chip 8-Bit uCOMP;1kB ROM,64 Byte RAM;5V Supply;28-Pin Cer DIP	PHIN
45#	8021N	8048	uCT	Chip	MNG	Single-Chip 8-Bit uCOMP;1kB ROM,64 Byte RAM;5V Supply;28-Pin Plas DIP	PHIN
46#	8048-8I	8048	uCT	Chip	MNG	8-Bit uComputer W/Mask ROM;5.0us Cycle;40-Pin Ceramic DIP	PHIN
47#	8048-8N	8048	uCT	Chip	MNG	8-Bit uComputer W/Mask ROM;5.0us Cycle;40-Pin Plastic DIP	PHIN
48#	8748-8I	8048	uCT	Chip	MNG	8-Bit uComputer W/EPROM;5.0us Cycle;40-Pin Ceramic DIP	PHIN
49#	8748I	8048	uCT	Chip	MNG	8-Bit uComputer W/EPROM;2.5us Cycle;40-Pin Ceramic DIP	PHIN
50#	MP8243I	8048	IO-33	Chip	MNX	I/O Xpander Adds Four 4-Bit Bidir Latched Ports to 8048,8021;24-Pin Cer	PHIN
51#	MP8243N	8048	IO-33	Chip	MNX	I/O Xpander Adds Four 4-Bit Bidir Latched Ports to 8048,8021;24-Pin Plas	PHIN
52	MPC577	MIPROC16		MOD		Analog Multiplexer Expander	PLM
53	MPC862	MIPROC16		MOD		Floating Paint Processor	PLM
54	MIPROC16	MIPROC16	CPU	MOD		16 Bit Microprocessor,Consits Of ALU,Accumulator,Program Counter,ROMs	PLM
55	MIPROCF-16	MIPROC16	CPU	MOD		16 Bit Processor;Instruction Cycle Time 250ns,2 GP Registers	PLM
56	MIPROCM-16	MIPROC16	CPU	MOD	BTD	16 Bit Processor;Instruction Cycle Time 350ns,83 Basic Inst	PLM
57	MPC175	MIPROC16	CPU	MOD		350ns Instruction Time CPU	PLM
58	MPC515	MIPROC16	CPU	MOD		250ns Instruction Time 16-Bit Processor	PLM
59	MIPROC-PK	MIPROC16	DEV	UNIT		Development System	PLM
60	681/1/00426	MIPROC16	IO-01	MOD		Monitor;Control Card for Program Mem Access and Breakpoint-Implementation	PLM
61	681/1/00169/000	MIPROC16	IO-02	MOD		Index/Interrupt Card;8 Level, Maskable Vectored Interrupt	PLM
62	681/1/00428	MIPROC16	IO-02	MOD		Interrput Expander Card;Provides 8 Additional Interrupt Lines,5V	PLM
63	MPC169	MIPROC16	IO-02	MOD		Index/Interrupt Card;8 Level Maskable Vectored Interrupt	PLM
64	MPC428	MIPROC16	IO-02	MOD		Interrupt Expander Card	PLM
65	681/1/00405/000	MIPROC16	IO-03	MOD		MIPROC16 Burst Mode DMA Controller	PLM
66	MPC550	MIPROC16	IO-03	MOD		DMA Controller 8M 16-Bit Words/Sec	PLM
67	MPC641	MIPROC16	IO-03	MOD		FiFo for Controller Dual 64 word FiFo Buffer MIPROC to MIPROC	PLM
68	MPC725	MIPROC16	IO-03	MOD		FiFo for Controller Dual 64 word FiFo Buffer PDP11 to MIPROC	PLM
69	SPM02-11	MIPROC16	IO-03	UNIT		Add on Mod;It is SPM-02 Configured as a DMA to PDP-11 or LSI-11	PLM
70	681/1/00261/002	MIPROC16	IO-20	MOD		Serial and Parallel I/F:Includes RS232-C,Current Loop I/F	PLM
71	681/1/00401	MIPROC16	IO-20	MOD		Asynchronous Serial I/O;Full Duplex,50-9600 Baud Transmission Rate	PLM
72	MPC401	MIPROC16	IO-20	MOD		Asynchronus Serial I/O;Full Duplex;50-9600 Baud Transmission Rate	PLM
73	681/1/00403	MIPROC16	IO-30	MOD		Parallel I/O Card;2 Ch 16 Bit Bidir Parallel Interface	PLM
74	MPC403	MIPROC16	IO-30	MOD		Parallel I/O;2 Channel 16-Bit Bidir;Parallel Interface	PLM
75	681/1/00422	MIPROC16	IO-33	MOD		6 Channel 16 Bit Parallel Input;Up to 850kW Transfer Rate	PLM
76	681/1/00424	MIPROC16	IO-33	MOD		6 Channel 16 Bit Parallel Output;Six 16 Bit Output Channels	PLM
77	MPC422	MIPROC16	IO-33	MOD		6 Channel Parallel I/P VP to 850kwd/s Transfer Rate	PLM
78	MPC424	MIPROC16	IO-33	MOD		6-Channel,16-Bit Parallel O/P	PLM
79	MPC575	MIPROC16	IO-41	MOD		16-Input A/D Converter 12-Bit Resoultion up to 100k Conversions/Sec	PLM
80	MPC579	MIPROC16	IO-44	MOD		2-Channel 12-Bit D/A Converter Voltage and Current Output	PLM
81	681/1/00182	MIPROC16	IO-45	MOD		Data Acquisition Module;8 Channel,12 Bit Resolution	PLM
82	681/1/00024	MIPROC16	IO-55	MOD		Development Memory Card;Up to 4k/1k 16B PROM,256W RAM	PLM
83	681/1/00407	MIPROC16	IO-55	MOD		Application Memory Card;Up to 4k/1k Progm/Data PROM,256W RAM	PLM
84	MPC407	MIPROC16	IO-55	MOD		Application Memory;4k Prog/1k Data PROM;256 Word RAM	PLM
85	MPC558	MIPROC16	IO-55	MOD		8k By 16-Bit RAM	PLM
86	681/1/00047	MIPROC16	IO-90	MOD		Hardware Multiply Card;Single Cycle Mult;16 Bit Signed Product	PLM
87	681/1/00581/000	MIPROC16	IO-90	MOD		Hardware Multiplier Card;32 Bit Software Controllable Product	PLM
88	MPC581	MIPROC16	IO-90	MOD		Double Precision Multiplier Fractional or Interger	PLM
89	681/1/00143	MIPROC16	IO-90	MODS		FFT Card Stacks;SPM-01 and -02 W/O Chassis,Fan	PLM
90	681/1/00122	MIPROC16	IO-90	UNIT		Fast Fourier Transform Proc Subsys;OEM Unit SPM-01;1024 FFT in 610ms	PLM
91	681/1/00142	MIPROC16	IO-90	UNIT		Fast Fourier Transform Proc Subsys;OEM Unit SPM-02;1024 FFT in 237ms	PLM
92	681/1/00443	MIPROC16	IO-92	MOD		Power Monitor and Clock;Unified Bus Interface	PLM
93	681/1/00499	MIPROC16	PE-60	UNIT		Card Bay;Contains 40A Power Supply,Fans,Slots for 13 Cards	PLM
94	MPC449	MIPROC16	PE-60	UNIT		Card Bay	PLM
95	681/1/00500	MIPROC16	PE-61	UNIT		AS;Application System Includes Power Supply;Holds up to 39 Cards	PLM
96	SPM-01/02	MIPROC16	PE-62	UNIT		FFT Development Syst:Incl:MIPROC-PK,PDP-11 Host Cross Assembler	PLM
97	681/1/00180	MIPROC16	PROM	MOD		8k x 16 PROM Card for PK System Only;Available in 3 Options	PLM
98	681/1/00505	MIPROC16	PROM	MOD		8k Word PROM Card;2 Variants Program Mem and Data Mem	PLM
99	MPC505	MIPROC16	PROM	MOD		8k Word PROM Card	PLM
100	681/1/00178	MIPROC16	RAM	MOD		2k x 16 RAM Card;Available in 7 Options	PLM
101	681/1/00430	MIPROC16	RAM	MOD		Perpheral Memory Card;Provides 2k x 16 Words of CMOS RAM	PLM
102	681/1/00433	MIPROC16	RAM	MOD		2k RAM Card;Unified Bus Interface;Avail in 3 Options	PLM
103	681/1/00436	MIPROC16	RAM	MOD		8k x 16 MOS RAM;Access Time 200ns;Available in 2 Options	PLM
104	681/1/00558	MIPROC16	RAM	MOD		8k Word 16 Bit RAM Card;Access Time 70ns max	PLM
105	MPC430	MIPROC16	RAM	MOD		Peripheral Memory Card	PLM
106	MPC433	MIPROC16	RAM	MOD		2k RAM Card	PLM
107	MPC818	MIPROC16	ROM	MOD		Downline Loader and Bootstrap	PLM
108	MPC446	MIPROC16	ROM	MODS		Monitor Card Set Hardware and Firmware Debug Monitor;3 Cards	PLM
109	PMB80M	PBM80	RAM	MOD		Mulitbus-Compatible Bubble Memory System;256k to 2M Bytes	PLM
110	M823					System Analyzer for 6800 Systems	PRO

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No.
(3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	PLS-858	PLS-858	COMP	MOD	MNG	One Card Sys;8085 CPU,Uses 2716 ROM;16 8-Bit I/O Ports	PRO
2	PLS-868	PLS-868	COMP	MOD	MNG	One Card Sys;6800 CPU,Uses 2716 ROM;16 8-Bit I/O Ports	PRO
3	PLS-881	PLS-881	COMP	MOD	MNG	Edge Card System;1 Card,Uses 8080A CPU, 1k RAM Storage,I/O,4kPROM SOCKETS	PRO
4	PLS-888	PLS-888	COMP	MOD	MNG	One Card Sys;8080 CPU,Uses 2716 ROM;16 8-Bit I/O Ports	PRO
5	PLS-898	PLS-898	COMP	MOD	MNG	One Card Sys;Z80 CPU,Uses 2716 ROM;16 8-Bit I/O Ports	PRO
6	7303	SER7000	IO-92	MOD		Keyboard Display Card;Alphanumeric Display w/ASCII Input	PRO
7	7801	7000	CPU	MOD		8085A Processor Card;Includes Clock,1k of RAM,Sockets for 4k RAM,8k ROM	PRO
8	7802	7000	CPU	MOD		6800 Processor Card;4k RAM;1k RAM Incl;8kROM;Cyrstal 1ms Clock	PRO
9	7803	7000	CPU	MOD		Z80 Processor Card;Includes Clock,1k of RAM,Sockets for 4k RAM,8k ROM	PRO
10▼	7320	7000	IO-02	MOD		Univer 8-Input Priority Interrupt Card	PRO
11	7301	7000	IO-20	MOD		RS232 TTy Drv/Rec Interface Card;Full Duplex;ASR/KSR TTy IF	PRO
12	7504-1	7000	IO-33	MOD		Triac Output Card;Switches from 40 to 280VAC at 2A on Each of 8 Loads	PRO
13▼	7507	7000	IO-33	MOD		Interface Between STD Bus/Industry STD I/O Module	PRO
14	7601	7000	IO-33	MOD		TTL I/O Port Card;32 Input Gates,32 Output Latches,(8 Ports);Exp Sockets	PRO
15	7602	7000	IO-33	MOD		TTL Output Port Card;64 Latched Output Lines,(8 Ports)	PRO
16	7603	7000	IO-33	MOD		TTL Input Port Card;64 Gated Input Lines;Sockets for Exp and Mem Mapping	PRO
17▼	7605	7000	IO-57	MOD		Programmable TTL I/O Card;8-Bit I/O Port;32 I/O Lines	PRO
18▼	7904	7000	IO-57	MOD		Decoded I/O Utiliy Card;Prototyping I/O Circuitry	PRO
19▼	7304	7000	IO-92	MOD		2 Fully Independent RS-232C Serial Data Commun	PRO
20	7502	7000	IO-92	MOD		Relay Output Card;8 SPST Relays with LED Displays;Use/Select Port Addr	PRO
21	7503	7000	IO-92	MOD		Optoisulated AC Input Card;Eight 115VAC Independent Inputs	PRO
22	7604	7000	IO-92	MOD	BTX	TTL I/O Card;8 Ports with Readback;Drives 16 Schottky TTL Loads	PRO
23	7702	7000	PROM	MOD		16k Byte EPROM Card;Includes Sockets for 8 2716 EPROMS;16,384 Bytes	PRO
24	7701	7000	RAM	MOD		16k Byte RAM Card;Includes Sockets for Up to 16k of RAM or PROM	PRO
25▼	PLS888A	8080A	uCT	MOD		Single Card uProcessor Sys;2k Byte RAM Capacity w/1k Include	PRO
26	SOLPC	SOL20	COMP	MOD		8 Bit Single Board Computer W/8080A CPU,2MHz Clock	PRT
27	SOL20/16	SOL20	COMP	UNIT		8 Bit Syst W/8080A,16k RAM,BASIC5,SOLOS Software	PRT
28	SOL20/32	SOL20	COMP	UNIT		8 Bit Syst W/8080A,32k RAM,BASIC5,SOLOS Software	PRT
29	SOLSIA	SOL20	COMP	UNIT		8 Bit Syst W/8080A,16k RAM,Extended BASIC,VM,CR	PRT
30	SOLSIIA	SOL20	COMP	UNIT		8 Bit Syst W/8080A,32k RAM,Extended BASIC,VM,CR	PRT
31	SOLSIIIA	SOL20	COMP	UNIT		8-Bit Syst W/8080A,65k Mem;Model 2 Dual Disk Sys,PT872 Video Monitor	PRT
32	SOLSIVA	SOL20	COMP	UNIT		8-Bit Syst W/8080A,65k Mem;Model 4 Quad Disk Sys,PT872 Video Montior	PRT
33	GPM	SOL20	IO-57	MOD		Gen Purpose Mem Mod:2k ROM Masked by CUTER Monitor Progm	PRT
34	HELIOSIIM2DS	SOL20	PE-01	UNIT		Floppy Disc Syst:One Dual FD Drive,Controller,Power Supply,Software	PRT
35	HELIOSIIM4DS	SOL20	PE-01	UNIT		Floppy Disc Syst:Two Dual FD Drives,Controller,Power Supply,Software	PRT
36	SOLPRINTER2	SOL20	PE-10	MOD		Word Processing Printer with Metal Print Wheel and Interface	PRT
37	SOLPRINTER2E	SOL20	PE-10	MOD		Economy Printer with Plastic Wheel and Interface	PRT
38	SOLPRINTER3	SOL20	PE-10	MOD		High Speed 200-cps Dot Matrix Printer with RS232 Interface	PRT
39	BOOTLOADPM	SOL20	PROM	MOD		BOOTLOAD Personality Mod W/2048 Byte PROM Stored Program	PRT
40	16KRA	SOL20	RAM	MOD		RAM Memory Mod:16384 Bytes of Dynamic RAM	PRT
41	32KRA	SOL20	RAM	MOD		RAM Memory Mod:32768 Bytes of Dynamic RAM	PRT
42	48KRA-1	SOL20	RAM	MOD	MNG	RAM Memory Mod;49152 Bytes of Dynamic RAM	PRT
43	64KRA-1	SOL20	RAM	MOD	MNG	RAM Memory Mod;65536 Bytes of Dynamic RAM	PRT
44	QUAY8000	QUAY8000	COMP	UNIT		8 Bit Microcomputer System;Uses QUAY80AI Microcomp Cards	QUY
45	QUAY80SMB	QUAY8000	IO-55	MOD		8k Static Memory Card For S100 Bus System	QUY
46	QUAY80MBP	QUAY8000	IO-92	MODS		Mother Board With Power Supply	QUY
47	QUAY90F/MPS	QUAY90	COMP	MOD		OEM Sys w/Floppy Disk Controller/Interface; 2.5MHz Clock Sys w/Z80 CPU	QUY
48	QUAY90MPS	QUAY90	COMP	MOD		8 Bit Microcomputer On A Card;Uses Z80 CPU	QUY
49	QUAY94F/MPS	QUAY90	COMP	MOD		OEM Sys w/Floppy Disk Controller/Interface;4.0MHz Clock Sys w/Z80A CPU	QUY
50	QUAY94MPS	QUAY90	COMP	MOD		8 Bit Microcomputer On A Card;Expanded QUAY90MPS System	QUY
51	QUAY80MCB	Q8000/8500	COMP	MOD		Provides S100 Bus IF and Facilities For Stand alone Operation	QUY
52	26-1051	TRS-80	COMP	UNIT		8-Bit uCOMP W/4k RAM,Lvl-I BASIC,Video Monitor,Recorder,Keyboard	RAD
53	26-1053	TRS-80	COMP	UNIT		8-Bit uCOMP W/16k RAM,Lvl-I BASIC,Video Monitor,Recorder,W/Num Keypad	RAD
54	26-1054	TRS-80	COMP	UNIT		8-Bit uCOMP W/4k RAM,Lvl-II BASIC,Video Monitor,Recorder,Keyboard	RAD
55	26-1056	TRS-80	COMP	UNIT		8-Bit uCOMP W/16k RAM,Lvl-II BASIC,Video Monitor,Recorder,W/Num Keypad	RAD
56	26-1145	TRS-80	IO-20	MOD		RS-232-C Board	RAD
57	26-1140	TRS-80	IO-57	UNIT		TRS-80 Expansion Interface	RAD
58	26-1141	TRS-80	IO-57	UNIT		Expansion Interface With 16k RAM	RAD
59	26-1142	TRS-80	IO-57	UNIT		Expansion Interface With 32k RAM	RAD
60	26-1171	TRS-80	IO-92	UNIT		Telephone Interface II(Originate/Answer);300 Baud	RAD
61	26-1180	TRS-80	IO-92	UNIT		Voice Synthesizer;Operates on 62 Phonemes to Create Any English Word	RAD
62	26-1205	TRS-80	IO-92	UNIT		Cassette Recorder	RAD
63	26-1161	TRS-80	PE-01	UNIT		Mini-Disk Sys 2,3,4;80k Bytes Storage;Requires 16k RAM	RAD
64	26-1160	TRS-80	PE-02	UNIT		TRS-80 Mini-Disk System;80k Bytes/Disk Storage,Req 16k RAM	RAD
65	26-1150	TRS-80	PE-10	UNIT		TRS-80 Line Printer;Prints From 60 to 110 Char/Sec	RAD
66	26-1152	TRS-80	PE-10	UNIT		Line Printer,Tractor Feed;Medium Speed,5x7 Dot Matrix,64-Char Upper ASCII	RAD
67	26-1153	TRS-80	PE-10	UNIT		150 Lines/Min 5x8 Dot Matrix Printer;Upper/Lower Case,4.75in Al. Paper	RAD
68	26-1155	TRS-80	PE-10	UNIT		Quick Printer II Similar to 26-1153	RAD
69	CDP1853CE	*See Descrp	IO-44	Chip	MCG	N-Bit 1 of 8 Decoder;*CDP1800 and CD4000	RCA
70▼	CDP18S602	CDP1800	COMP	MOD	MCG	uBoard Computer:w/CDP1802 CPU,X±a1-Controlledclk,Read-Write Mem;Par I/O	RCA
71▼	CDP18S603	CDP1800	COMP	MOD	MCG	uBoard Computer:w/CDP1802 CPU,X±a1-Controlledclk,Read-Write Mem;Par I/O	RCA
72	CDP1802CD	CDP1800	CPU	Chip	MCG	Register-Oriented,16x16-Bit Selectable Register Array;Op Volt 4-6.5V	RCA
73	CDP1802CE	CDP1800	CPU	Chip	MCG	8-Bit CPU;91 Instructions;16 Registers;Bidirect Data Bus;65kByte Addr/Up	RCA
74	CDP1802D	CDP1800	CPU	Chip	MCG	Register-Oriented,16x16-Bit Selectable Register Array;Op Volt 4-10.5V	RCA
75	CDP1802E	CDP1800	CPU	Chip	MCG	8-Bit CPU;91 Instructions;16 Registers;Bidirect Data Bus;65k Byte Addr/Up	RCA
76	CDP1804CD	CDP1800	CPU	Chip	MCG	Register-Oriented CPU with Mem Expansion;Op Volt 4-6.5V;-55 to 125°C	RCA
77	CDP1804CE	CDP1800	CPU	Chip	MCG	Register-Oriented CPU with Mem Expansion;Op Volt 4-6.5V;-40 to 80°C	RCA
78	CDP1804D	CDP1800	CPU	Chip	MCG	Register-Oriented CPU with Mem Expansion;Op Volt 4-10.5V;-55 to 125°C	RCA
79	CDP1804E	CDP1800	CPU	Chip	MCG	Register-Oriented CPU with Mem Expansion;Op Volt 4-10.5V;-40 to 80°C	RCA
80	CDP18S020	CDP1800	DEV	MOD	MCG	CDP1800 Evaluation Kit;Includes 256x8 RAM,Utility Program on ROM	RCA
81	CDP18S103	CDP1800	DEV	MOD	MCG	Plug In Mod Supplied w/CDS II/CDS III; Control	RCA
82	CDP18S205V1	CDP1800	DEV	MOD	MCG	Plug In Mod Supplied w/CDS II/; 4-Kilobyte RAM	RCA
83	CDP18S401	CDP1800	DEV	MOD	MCG	Plug In Mod Supplied w/CDS II/; ROM/RAM	RCA
84	CDP18S502	CDP1800	DEV	MOD	MCG	Plug In Mod Supplied w/CDS II/; Extender Card	RCA
85	CDP18S507	CDP1800	DEV	MOD	MCG	Plug In Mod Supplied w/CDS II/; Terminal Interface	RCA
86	CDP18S509	CDP1800	DEV	MOD	MCG	Plug In Mod Supplied w/CDS II/; I/O Decode	RCA
87	CDP18S601	CDP1800	DEV	MOD	MCG	COSMAC Microboard Computer;CPU,Memory,I/O	RCA
88	CDP18S620	CDP1800	DEV	MOD	MCG	Plug In Mod Supplied w/CDS II/CDS III;4-Kilobyte RAM	RCA
89	CDP18S621	CDP1800	DEV	MOD	MCG	Plug In Mod Supplied w/CDS II/CDS III, 16-Kilobyte RAM Microboard	RCA
90	CDP18S623	CDP1800	DEV	MOD	MCG	Plug In Mod Supplied w/CDS II/CDS III, 8-Kilobyte RAM	RCA
91	CDP18S801V1	CDP1800	DEV	MOD	MCG	CDS II/CDS III Dual Disk Drive Mechanism;100-120V AC 60Hz 250 W	RCA
92	CDP18S801V3	CDP1800	DEV	MOD	MCG	CDS II/CDS III Dual Disk Drive Mechanism;220V-240V ac 50Hz 250 W	RCA
93	CDP18S813	CDP1800	DEV	MOD	MCG	Opt. Modules (Avail Sep) w/CDS II/CDS III;Disk Interface	RCA
94	CDP18S024	CDP1800	DEV	MODS	MCG	EK/Assembler-Editor;Evaluation Kit with Software on Mag or Paper Tape	RCA
95	CDP18S025	CDP1800	DEV	MODS	MCG	Combination Eval Kit CDP18S020,Microterminal CDP18S021,5V PS CDP18S023	RCA
96	CDP18S102V1	CDP1800	DEV	MODS	MCG	Plut In Mod Supplied w/CDS II/CDS III;CPU	RCA
97	CDP18S206	CDP1800	DEV	MODS	MCG	Plut In Mod Supplied w/CDS II/CDS III;Address Latch and Bank Select	RCA
98	CDP18S480	CDP1800	DEV	MODS	MCG	PROM Progr Used w/Dev Sys II; Software on Diskette	RCA
99	CDP18S480V1	CDP1800	DEV	MODS	MCG	PROM Progr Used w/Dev Sys II; Software on Paper Tape	RCA
100	CDP18S480V2	CDP1800	DEV	MODS	MCG	PROM Progr Used w/Dev Sys II; Software on Cassette	RCA
101	CDP18S831	CDP1800	DEV	MODS	MCG	Micromonitor Op Sys;Includes CDP18S508 UART Ckt Bd,Software on Diskette	RCA
102	CDP18S837	CDP1800	DEV	MODS	MCG	Upgrade Pkg for CDS II to CDS III;Inc Floppy Disk Sys;Min 12-Bytes RAM	RCA
103	CDP18S005	CDP1800	DEV	UNIT	MCG	COSMAC Dev Sys II for PrototypRCA C Dev Sys II for Prototyp,ROM,I/O etc	RCA
104	CDP18S007V1	CDP1800	DEV	UNIT	MCG	COSMAC Dev Sys III Inc CDS Cen Proc 28k-Bytes RAM,CDOS Disk Sys;115V,60Hz	RCA
105	CDP18S007V3	CDP1800	DEV	UNIT	MCG	COSMAC Dev Sys III Inc CDS Cen Proc 28k-Bytes RAM,CDOS Disk Sys;220V,50Hz	RCA
106	CDP18S021	CDP1800	DEV	UNIT	MCG	Microterminal;Hand-held Keybd-LED Display for Evaluation Kit CDP18S020	RCA
107	CDP18S030	CDP1800	DEV	UNIT	MCG	Micromonitor;Used with Dev Sys II for Hardware/Software Debugging	RCA
108	CDP1861CD	CDP1800	IO-09	Chip	MCG	Video Display Controller;Programmable Vertical Resolution	RCA
109	CDP1862CD	CDP1800	IO-09	Chip	MCG	Color Gen. Controller for Use w/CDP1861 Video Display;NTSC Compatible	RCA
110	CDP1862CE	CDP1800	IO-09	Chip	MCG	Color Gen. Controller for Use w/CDP1861 Video Display;NTSC Compatible	RCA

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	CDP1862D	CDP1800	IO-09	Chip	MCG	Color Gen. Controller for Use w/CDP1861 Video Display;NTSC Compatible	RCA
2	CDP1862E	CDP1800	IO-09	Chip	MCG	Color Gen. Controller for Use w/CDP1861 Video Display;NTSC Compatible	RCA
3	CDP1864CD	CDP1800	IO-09	Chip	MCG	PAL-Compatible TV Interface;Bit Mapped Color B/W;192 V Linesx 64 H Dots	RCA
4	CDP1864CE	CDP1800	IO-09	Chip	MCG	PAL-Compatible TV Interface;Bit Mapped Color B/W;192 V Linesx 64 H Dots	RCA
5▼	CDP1871CD	CDP1800	IO-10	CHIP	MCG	Keyboard Encoder;Counter/Scan-Selection Logic,Control Logic	RCA
6▼	CDP1871CE	CDP1800	IO-10	CHIP	MCG	Keyboard Encoder;Counter/Scan-Selection Logic,Control Logic	RCA
7▼	CDP1871D	CDP1800	IO-10	CHIP	MCG	Keyboard Encoder;Counter/Scan-Selection Logic,Control Logic	RCA
8▼	CDP1871E	CDP1800	IO-10	CHIP	MCG	Keyboard Encoder;Counter/Scan-Selection Logic,Control Logic	RCA
9	CDP18S508	CDP1800	IO-20	MOD	MCG	CDP1854 UART Ckt Bd Used with CDSII Dev Sys for TTY or CRT Interface	RCA
10▼	CDP18S641	CDP1800	IO-20	MOD	MCX	Microboard UART Interface:Parallel to Serial I/O Data Controller	RCA
11	CDP1856CD	CDP1800	IO-21	Chip	MCG	4-Bit Bus Buffer Used Bet Mem and Data Bus;Op Volt 4-6.5V	RCA
12	CDP1856D	CDP1800	IO-21	Chip	MCG	4-Bit Bus Buffer Used Bet Mem and Data Bus;Op Volt 4-10.5V	RCA
13	CDP1856E	CDP1800	IO-21	Chip	MCG	4-Bit Bus Buffer/Separators Use Betw/CDP1802/04 Data Bus and Memory	RCA
14	CDP1857CD	CDP1800	IO-21	Chip	MCG	4-Bit Bus Buffer Used Bet I/O and Data Bus;Op Volt 4-6.5V	RCA
15	CDP1857CE	CDP1800	IO-21	Chip	MCG	4-Bit Bus Buffer/Separators Use Betw/CDP1802/04 Data Bus and I/O Device	RCA
16	CDP1857D	CDP1800	IO-21	Chip	MCG	4-Bit Bus Buffer Used Bet I/O and Data Bus;Op Volt 4-10.5V	RCA
17	CDP1857E	CDP1800	IO-21	Chip	MCG	4-Bit Bus Buffer/Separators Use Betw/CDP1802/04 Data Bus andI/O Device	RCA
18▼	CDP18S660	CDP1800	IO-23	MOD	MCX	Combination Memory and I/O Module;2k Bytes Ram;8k Bytes ROM/EPROM	RCA
19	CDP1851CD	CDP1800	IO-30	Chip	MCG	Programmable I/O Interface;20 Prog I/O Lines;Byte or Bit Programmable	RCA
20	CDP1851CE	CDP1800	IO-30	Chip	MCG	Programmable I/O Interface;20 Prog I/O Lines;Byte or Bit Programmable	RCA
21	CDP1851D	CDP1800	IO-30	Chip	MCG	Programmable I/O Interface;20 Prog I/O Lines;Byte or Bit Programmable	RCA
22	CDP1851E	CDP1800	IO-30	Chip	MCG	Programmable I/O Interface;20 Prog I/O Lines;Byte or Bit Programmable	RCA
23	CDP1852CD	CDP1800	IO-33	Chip	MCG	8 Bit Mode Programmable Input/Output Port	RCA
24	CDP1852CE	CDP1800	IO-33	Chip	MCG	8-Bit Input/Output Port;Interfaces w/CDP1802/4 MPU Directly;8-Bit Par.Reg	RCA
25	CDP1852D	CDP1800	IO-33	Chip	MCG	8 Bit Mode Programmable Input/Output Port	RCA
26	CDP1852E	CDP1800	IO-33	Chip	MCG	8-Bit Input/Output Port;Interfaces w/CDP1802/4 MPU Directly;8-Bit Par.Reg	RCA
27	CDP1869CD	CDP1800	IO-33	Chip	MCG	Address/Sound Gen;5.67MHz Dot Freq;Use w/CDP1870	RCA
28	CDP1869CE	CDP1800	IO-33	Chip	MCG	Address/Sound Gen;5.67MHz Dot Freq;Use w/CDP1870	RCA
29	CDP1869D	CDP1800	IO-33	Chip	MCG	Address/Sound Gen;5.67MHz Dot Freq;Use w/CDP1870	RCA
30	CDP1869E	CDP1800	IO-33	Chip	MCG	Address/Sound Gen;5.67MHz Dot Freq;Use w/CDP 1870	RCA
31	CDP1870CD	CDP1800	IO-33	Chip	MCG	Color Video Gen;Use w/CDP 1869	RCA
32	CDP1870CE	CDP1800	IO-33	Chip	MCG	Color Video Gen;Use w/CDP 1869	RCA
33	CDP1870D	CDP1800	IO-33	Chip	MCG	Color Video Gen;Use w/CDP 1869	RCA
34	CDP1870E	CDP1800	IO-33	Chip	MCG	Color Video Gen;Use w/CDP 1869	RCA
35	CDP18S510	CDP1800	IO-33	MOD	MCG	Byte I/O Ckt with 4 CDP1852 Chips;Used with CDS II Dev Sys	RCA
36▼	CDP18S642	CDP1800	IO-40	MOD	MCX	D/A Converter:2 Independent D/A Chs;12 or 8Bit Resolution;Assign. I/O Adr	RCA
37▼	CDP18S643	CDP1800	IO-41	MOD	MCX	A/D Converter:Multiplexed Inputs,16SE or 8 Diff;Scanned or Fixed In Modes	RCA
38	CDP1853CD	CDP1800	IO-44	Chip	MCG	1 of 8 Decoder Used with 3-Bit Select Lines of CPU;Op Volt 4-6.5V	RCA
39	CDP1853D	CDP1800	IO-44	Chip	MCG	1 of 8 Decoder Used with 3-Bit Select Lines of CPU;Op Volt 4-10.5V	RCA
40	CDP1858CD	CDP1800	IO-56	Chip	MCG	4-Bit Latch W/Dual 1 of 4 Decoders used W/256x4 RAM;4-6.5V;Ta -55to125°C	RCA
41	CDP1858CE	CDP1800	IO-56	Chip	MCG	4-Bit Latch W/Dual 1 of 4 Decoders used W/256x4 RAM;4-6.5V;Ta -40to85°C	RCA
42	CDP1858D	CDP1800	IO-56	Chip	MCG	4-Bit Latch W/Dual 1 of 4 Decoders used W/256x4 RAM;4-10.5V;Ta -55to125°C	RCA
43	CDP1858E	CDP1800	IO-56	Chip	MCG	4-Bit Latch W/Dual 1 of 4 Decoders used W/256x4 RAM;4-10.5V;Ta -40to85°C	RCA
44	CDP1859CD	CDP1800	IO-56	Chip	MCG	4-Bit Latch with 1 of 4 Decoder used W/1024x1 RAM;4-6.5V;Ta -55to125°C	RCA
45	CDP1859CE	CDP1800	IO-56	Chip	MCG	4-Bit Latch with 1 of 4 Decoder used W/1024x1 RAM;4-6.5V;Ta -40to85°C	RCA
46	CDP1859D	CDP1800	IO-56	Chip	MCG	4-Bit Latch with 1 of 4 Decoder used W/1024x1 RAM;4-10.5V;Ta -55to125°C	RCA
47	CDP1859E	CDP1800	IO-56	Chip	MCG	4-Bit Latch with 1 of 4 Decoder used W/1024x1 RAM;4-10.5V;Ta -40to85°C	RCA
48	CDP1866CD	CDP1800	IO-56	Chip	MCG	4-Bit Latch/Decoder Memory Interface for Use w/1024 Word RAM	RCA
49	CDP1866CE	CDP1800	IO-56	Chip	MCG	4-Bit Latch/Decoder Memory Interface for Use w/1024 Word RAM	RCA
50	CDP1866D	CDP1800	IO-56	Chip	MCG	4-Bit Latch/Decoder Memory Interface for use W/1024 Word RAM	RCA
51	CDP1866E	CDP1800	IO-56	Chip	MCG	4-Bit Latch/Decoder Memory Interface for Use w/1024 Word RAM	RCA
52	CDP1867CD	CDP1800	IO-56	Chip	MCG	Same As CDP1866 Except for Use W/4096 Word RAM	RCA
53	CDP1867CE	CDP1800	IO-56	Chip	MCG	Same As CDP 1866 Except for Use w/4096 Word RAM	RCA
54	CDP1867D	CDP1800	IO-56	Chip	MCG	Same As CDP 1866 Except for Use w/4096 Word RAM	RCA
55	CDP1867E	CDP1800	IO-56	Chip	MCG	Same As CDP 1866 Except for Use w/4096 Word RAM	RCA
56	CDP1868CD	CDP1800	IO-56	Chip	MCG	Same As CDP1866 Except for Pin Design	RCA
57	CDP1868CE	CDP1800	IO-56	Chip	MCG	Same as CDP1866 Except for Pin Design	RCA
58	CDP1868D	CDP1800	IO-56	Chip	MCG	Same As CDP1866 Except for Pin Design	RCA
59	CDP1868E	CDP1800	IO-56	Chip	MCG	Same as CDP1866 Except for Pin Design	RCA
60	CDP1855CD	CDP1800	IO-90	Chip	MCG	8-Bit Prog Mult/Divide Unit Direct Interface CDP1802/1804CPU	RCA
61	CDP1855CE	CDP1800	IO-90	Chip	MCG	8-Bit Prog Mult/Divide Unit Direct Interface CDP1802/1804CPU	RCA
62	CDP1855D	CDP1800	IO-90	Chip	MCG	8-Bit Prog Mult/Divide Unit Direct Interface CDP1802/1804CPU	RCA
63	CDP1855E	CDP1800	IO-90	Chip	MCG	8-Bit Prog Mult/Divide Unit Direct Interface CDP 1802/1804CPU	RCA
64	CDP1863CD	CDP1800	IO-92	Chip	MCG	8-Bit Programmable Frequency Generator;256 Audio Freq.Selections	RCA
65	CDP1863CE	CDP1800	IO-92	Chip	MCG	8-Bit Programmable Frequency Generator;256 Audio Freq.Selections	RCA
66	CDP1863D	CDP1800	IO-92	Chip	MCG	8-Bit Programmable Frequency Generator;256 Audio Freq.Selections	RCA
67	CDP1863E	CDP1800	IO-92	Chip	MCG	8-Bit Programmable Frequency Generator;256 Audio Freq.Selections	RCA
68▼	CDP1861CE	CDP1800	IO/09	CHIP	MCG	Video Display Controller;Programmable Vertical Resolution	RCA
69	CDP18S805V1	CDP1800	PE-01	UNIT		COSMAC Floppy Disk Sys II Used with CDP18S005(DEV SYS II);115VAC,60Hz	RCA
70	CDP18S805V3	CDP1800	PE-01	UNIT		COSMAC Floppy Disk Sys II Used with CDP18S005(DEV SYS II);220VAC,50Hz	RCA
71	CDP1821CD	CDP1800	RAM	Chip	MCG	1024x1 Static RAM;Operating Voltage 4.0 to 6.5V	RCA
72	CDP1821D	CDP1800	RAM	Chip	MCG	1024x1 Static RAM;Operating Voltage 4.0 to 10.5V	RCA
73	CDP1822CD	CDP1800	RAM	Chip	MCG	256x4 Static RAM;Operating Volt Range 4-6.5V;Ta -55 to 125°C	RCA
74	CDP1822CE	CDP1800	RAM	Chip	MCG	256x4 Static RAM;Operating Volt Range 4-6.5V;Ta -40 to 85°C	RCA
75	CDP1822D	CDP1800	RAM	Chip	MCG	256x4 Static RAM;Operating Volt Range 4-10.5V;Ta -55 to 125°C	RCA
76	CDP1822E	CDP1800	RAM	Chip	MCG	256x4 Static RAM;Operating Volt Range 4-10.5V;Ta -40 to 85°C	RCA
77	CDP1823CD	CDP1800	RAM	Chip	MCG	128x8 Static RAM;Operating Voltage 4.0 to 6.5V	RCA
78	CDP1823D	CDP1800	RAM	Chip	MCG	128x8 Static RAM;Operating Voltage 4.0 to 10.5V	RCA
79	CDP1824CD	CDP1800	RAM	Chip	MCG	32x8 Static RAM;Operating Volt 4-6.5V;Ceramic Pkg(-55 to 125°C)	RCA
80	CDP1824CE	CDP1800	RAM	Chip	MCG	32x8 Static RAM;Operating Volt 4-6.5V;Plastic Pkg(-40 to 85°C)	RCA
81	CDP1824D	CDP1800	RAM	Chip	MCG	32x8 Static RAM;Operating Volt 4-10.5V;Ceramic Pkg(-55 to 125°C)	RCA
82	CDP1824E	CDP1800	RAM	Chip	MCG	32x8 Static RAM;Operating Volt 4-10.5V;Plastic Pkg(-40 to 85°C)	RCA
83	CDP1825D	CDP1800	RAM	Chip	MCG	1024x4 Static RAM;Operating Volt 4-10.5V;TTL Compatible Inputs and Output	RCA
84▼	CDP18S621V1	CDP1800	RAM	MOD	MCX	16k Byte RAM:w/on Bd Addr Latches and Decoders;Buffered Addr/Data Lines	RCA
85▼	CDP18S622	CDP1800	RAM	MOD	MCX	8k Byte RAM:w/on Board Addr Latches and Decanders;w/Battery Backup	RCA
86▼	CDP18S624	CDP1800	RAM	MOD	MCX	4k Byte RAM:w/on Board Addr Latches and Decaders;w/Battery Backup	RCA
87	CDP1831CD	CDP1800	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-6.5V;Access Time 1us max	RCA
88	CDP1831CE	CDP1800	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-6.5V;Access Time 1us max	RCA
89	CDP1831D	CDP1800	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-10.5V;Access Time 400ns max	RCA
90	CDP1831E	CDP1800	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-10.5V;Access Time 400ns max	RCA
91	CDP1832CD	CDP1800	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-6.5V;Access Time 1us max	RCA
92	CDP1832CE	CDP1800	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-6.5V;Access Time 1us max	RCA
93	CDP1832D	CDP1800	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-10.5V;Access Time 500ns max	RCA
94	CDP1832E	CDP1800	ROM	Chip	MCG	512x8 Static ROM;Operating Volt Range 4-10.5V;Access Time 500ns max	RCA
95	CDP1833CD	CDP1800	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-6.5V;Access Time 775ns max	RCA
96	CDP1833CE	CDP1800	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-6.5V;Access Time 775ns max	RCA
97	CDP1833D	CDP1800	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-10.5V;Access Time 425ns max	RCA
98	CDP1833E	CDP1800	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-10.5V;Access Time 425ns max	RCA
99	CDP1834CD	CDP1800	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-6.5V;Access Time 750ns max	RCA
100	CDP1834CE	CDP1800	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-6.5V;Access Time 750ns max	RCA
101	CDP1834D	CDP1800	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-10.5V;Access Time 425ns max	RCA
102	CDP1834E	CDP1800	ROM	Chip	MCG	1024x8 Static ROM;Operating Volt Range 4-10.5V;Access Time 425ns max	RCA
103	CDP18S012	CDP1802	DEV	UNIT		COSMAC Microtutor II;Basic Microcomp for Operation/Programming Training	RCA
104	CDP18S023	CDP1802	PE-60	UNIT		COSMAC 5V Power Supply	RCA
105	CDP1854ACD	CD4000	IO-20	Chip	MCG	Prog UART;Full/Half Duplex;Baud Rate 500k typ at VDD 10 V	RCA
106	CDP1854ACE	CD4000	IO-20	Chip	MCG	Prog UART;Full/Half Duplex;Baud Rate,500k typ at VDD 10V	RCA
107	CDP1854AD	CD4000	IO-20	Chip	MCG	Prog UART;Full/Half Duplex;Baud Rate,250k typ at VDD 5.0V	RCA
108	CDP1854AE	CD4000	IO-20	Chip	MCG	Prog UART;Full/Half Duplex;Baud Rate,250k;typ at VDD 5.0V	RCA
109	VP44	COSMACVIP	DEV	ChS	MCG	RAM On-Board Expansion Kit for Avail Space on VIP Unit;Type 2114 RAMs	RCA
110	VP45	COSMACVIP	DEV	ChS	MCG	RAM On-Board Expansion Kit for Avail Space on VIP Unit;Type 9131 RAMs	RCA

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	CDP18S022	COSMACVIP	DEV	MOD	MCG	COSMAC VIP;Hobbyist Computer on a Card in Kit Form	RCA
2	VP550	COSMACVIP	DEV	MOD	MCG	Super Sound Bd;Music and Sound Synthesizer on Plug-In Bd for VIP Unit	RCA
3	VP560	COSMACVIP	DEV	MOD	MCG	EPROM Plug-In Bd for VIP Unit	RCA
4	VP565	COSMACVIP	DEV	MOD	MCG	EPROM Programmer Board	RCA
5	VP570	COSMACVIP	DEV	MOD	MCG	Mem Expansion Bd;4k of Type 2113 Static RAM;Req 5V,1A Ext Pwr Supply	RCA
6	VP580	COSMACVIP	DEV	MOD		Expansion Keyboard for Use with VIP Unit	RCA
7	VP585	COSMACVIP	DEV	MOD	MCG	Keyboard Interface Board	RCA
8	VP590	COSMACVIP	DEV	MOD	MCG	Color Display Bd;Provides 64 Color Zones for Color Video Display	RCA
9	VP595	COSMACVIP	DEV	MOD	MCG	Simple Sound Bd;Audio Osc,Ampl,and Speaker on Plug-in Bd for VIP Unit	RCA
10	CDP18S731	COSMACVIP	DEV	MODS	MCG	RAM/IO Expansion Kit;Type 9131 1024x4 RAMs	RCA
11	CDP18S745	COSMACVIP	DEV	MODS	MCG	RAM/IO Expansion Kit;Type 2114 1024x4 RAMs	RCA
12	CDP18S711	COSMACVIP	DEV	UNIT	MCG	COSMAC VIP(Video Interface Processor);Assembled Version of Hobbyist Comp	RCA
13	TC1210	COSMACVIP	DEV	UNIT		9 Inch Video Monitor for Use with VIP Unit	RCA
14	TC1212	COSMACVIP	DEV	UNIT		12 Inch Video Monitor for Use with VIP Unit	RCA
15	TC1217	COSMACVIP	DEV	UNIT		17 Inch Video Monitor for Use with VIP Unit	RCA
16	CMC68/04	CMC68/15	uCT	MOD		4Ch Com Board, Sync or Async; Includes CPU,Clock,RAM,ROM,I/O Ports,Timer	RCI
17	CMC68/15B	CMC68/15	COMP	MOD		8 Bit Microcomputer on a Card; 6800 CPU,2MHz Clock, 32 Parallel I/O Parts	RCI
18	CMC68/15G	CMC68/15	COMP	MOD		8 Bit Microcomputer on a Card; IEEE Version of CMC68/15 System	RCI
19	CDB01	CMC68/15	IO-07	MOD		CRT and Floppy Disc Controller Board (Supports CRT, KBD, Dual Floppies)	RCI
20	RRB68A	CMC68/15	IO-57	MOD		RAM/ROM Board:16k Bytes RAM/ROM; ROM/EPROM Sockets; RAM Cycle Time 450ns	RCI
21	DPA68/1M	CMC68/15	IO-92	MOD		Dual Port Adapter for RAM68/32 and 68/64 Boards to 1 Megabyte Capacity	RCI
22	RAM68/64	CMC68/15	RAM	MOD		8 Bit, 65k RAM, 16 Address, 750ns Cycle Time; 300ns Access Time	RCI
23	CMC68/15	CMP68/15	COMP	MOD		8 Bit Microcomputer on a Card;6800 CPU,1MHz Clock,32 Par IO Ports	RCI
24	CMC68/15C	CMP68/15	COMP	MOD		8 Bit Microcomputer on a Card,Same as CMC68/15 Except IO Options	RCI
25	RRB68	CMP68/15	IO-57	MOD		RAM/ROM Board:8k Bytes RAM,8 ROM/EPROM Sockets,RAM Cycle Time 450ns	RCI
26	A65-009	AIM65		MOD		Expansion Mother Board used to Extend AIM65	RKW
27	A1799	PPS4	DEV	Chip	MPX	Dev Version Of A17 ROM/RAM-I/O For Emulation,Progr Dev Of PPS4/2 System	RKW
28	10736,15380	PPS4	IO-08	Chip	MPX	2 Chip Set Victor Dot Matrix Printer Controller	RKW
29	A07	PPS4	IO-55	Chip	MPX	Comb 1024 x 8 ROM,116 x 4 RAM	RKW
30	A20	PPS4	IO-55	Chip	MPX	Comb 1536 x 8 ROM,116 x 4 RAM	RKW
31	A08	PPS4	IO-57	Chip	MPX	Comb 704 x 8 ROM;76 x 4 RAM	RKW
32	A17	PPS4	IO-57	Chip	MPX	ROM/RAM/IO;2k Bytes ROM,128 x 4 Bit Words RAM	RKW
33	10432	PPS4	RAM	Chip	MPX	256 x 4 RAM	RKW
34	10932	PPS4	RAM	Chip	MPX	512 x 4 RAM	RKW
35	MM75	PPS4/1	uCT	Chip	MPX	4 Bit One Chip Comp for Prod;640/48Byte ROM/RAM;22I/O Lines;28Pin Pkg	RKW
36	MM76EL	PPS4/1	uCT	Chip	MPX	4 Bit One Chip Computer;1024/48 Byte ROM/RAM;31 I/O Ports,Low Volt/Pwr	RKW
37	MM78	PPS4/1	uCT	Chip	MPX	4 Bit One Chip Comp for Prod;2k/128Byte ROM/RAM;31I/O Lines;42Pin Pkg	RKW
38	MM78L	PPS4/1	uCT	Chip	MPX	4 Bit One Chip Computer;2048/128 Byte ROM/RAM;31 I/O Ports,Low Volt/Pwr	RKW
39	A7699	PPS4/1	DEV	Chip	MPX	4 Bit Prototype MM76 Chip;No On-Chip ROM;Prog Dev with PPS4MP on Ext Mem	RKW
40	A7899	PPS4/1	DEV	Chip	MPX	4 Bit Prototype MM78 Chip;No On-Chip ROM;Prog Dev with PPS4MP on Ext Mem	RKW
41	XPO-1/76	PPS4/1	DEV	MOD	MPX	MM76 Dev Board;Incl A7699,Keybd/Display and Utility/Debug/Monitor Progr	RKW
42	XPO-1/78	PPS4/1	DEV	MOD	MPX	MM78 Dev Board;Incl A7899,Keybd/Display and Utility/Debug/Monitor Progr	RKW
43	11049	PPS4,8	IO-01	Chip	MPX	Interval Timer;Provides 4 12-Bit Counters	RKW
44	10929	PPS4,8	IO-03	Chip	MPX	4k RAM Interface	RKW
45	10789	PPS4,8	IO-08	Chip	MPX	Printer Control	RKW
46	RC7000	PPS4,8	IO-08	Chip	MPX	LRC Printer Controller;Provides ASCII Char Generation And Paper Feed	RKW
47	10814	PPS4,8	IO-09	Chip	MPX	Display Controller	RKW
48	10788	PPS4,8	IO-10	Chip	MPX	General Purpose Keyboard And Display Control	RKW
49	10815	PPS4,8	IO-10	Chip	MPX	Keyboard/Printer Controller	RKW
50	10930	PPS4,8	IO-20	Chip	MPX	Serial Data Controller	RKW
51	11696	PPS4,8	IO-30	Chip	MPX	Parallel I/O;24 Bi-Direct Lines;Static,Clocked Or Discrete Mode Program	RKW
52	10696	PPS4,8	IO-33	Chip	MPX	General Purpose Input/Output Device	RKW
53	A05	PPS4,8	ROM	Chip	MPX	1024 x 8 ROM	RKW
54	A52	PPS4,8	ROM	Chip	MPX	2048 x 8 ROM	RKW
55	A66	PPS4,8	ROM	Chip	MPX	4k x 8 ROM	RKW
56	A88	PPS4,8	ROM	Chip	MPX	8192x8 Bit ROM;Dynamic Address Decode Logic,42 Pin Pkg	RKW
57	A2199	PPS8	DEV	Chip	MPX	RAM-I/O Evaluation Ckt For Emulation And Dev Of PPS8/2 System	RKW
58	10817	PPS8	IO-03	Chip	MPX	Direct Memory Access Controller	RKW
59	10936	PPS8	IO-07	Chip	MPX	Floppy Disk Controller	RKW
60	10453	PPS8	IO-33	Chip	MPX	Parallel Data Controller	RKW
61	A21	PPS8	IO-57	Chip	MPX	2k/64 Byte ROM/RAM,16 Parallel,1 Serial I/O,16-Bit Timer,On-Chip Clock	RKW
62	10809	PPS8	RAM	Chip	MPX	256 x 8 RAM	RKW
63	R6500/1	R6500	uCT	Chip	MNG	One-Chip 8 Bit Microcomputer;6502CPu,64 Byte RAM,2k Byte ROM	RKW
64	AIM65	R6500	COMP	MOD	MNG	8 Bit uC Mod w/Print,Display,6502,RAM,ROM,I/O,IKB/4KB R/W RAM,Expandable	RKW
65	R6502	R6500	CPU	Chip	MNG	CPU W/On-Chip Clk;Non-Maskable Int;Sync Out;40 Pin Pkg;65kMem Addr Space	RKW
66	R6503	R6500	CPU	Chip	MNG	CPU W/On-Chip Clk;Non-Maskable Int;28 Pin Pkg;4k Mem Addr Space	RKW
67	R6504	R6500	CPU	Chip	MNG	CPU W/On-Chip Clk;Maskable Interrupt;28 Pin Pkg;8k Mem Addr Space	RKW
68	R6505	R6500	CPU	Chip	MNG	CPU W/On-Chip Clk;Maskable Interrupt;28 Pin Pkg;4k Mem Addr Space	RKW
69	R6506	R6500	CPU	Chip	MNG	CPU W/On-Chip Clk;Maskable Interrupt;Clk Out;28 Pin Pkg;4k Mem Addr Space	RKW
70	R6507	R6500	CPU	Chip	MNG	CPU W/On-Chip Clk;No Interrupt;28 Pin Pkg;8k Mem Addr Space	RKW
71	R6512	R6500	CPU	Chip	MNG	CPU W/On-Chip Clk;Non-Maskable Int;Sync Out;40 Pin Pkg;Ext Data Bus Hold	RKW
72	R6513	R6500	CPU	Chip	MNG	CPU;Ext Clk;Non-Maskable Interrupt;28 Pin Pkg;4k Mem Addr Space	RKW
73	R6514	R6500	CPU	Chip	MNG	CPU;Ext Clk;Maskable Interrupt;28 Pin Pkg;8k Mem Addr Space	RKW
74	R6515	R6500	CPU	Chip	MNG	CPU;Ext Clk;Maskable Interrupt;28 Pin Pkg;4k Mem Addr Space	RKW
75	R6500/1E	R6500	DEV	Chip	MNG	Emulator Device;Freq Option 1.0 or 2.0MHz;0° to 70°C;64 Pin Pkg	RKW
76	M65-001	R6500	DEV	MODS	MNG	USER 65 Host,Buffer Mods,1.0MHz Version,For Emul Replaces CPU	RKW
77	M65-002	R6500	DEV	MODS	MNG	USER 65 Host,Buffer Mods,2.0MHz Version,For Emul Extends Bus Lines	RKW
78	SYSTEM65	R6500	DEV	UNIT	MNG	Complete Dev Sys With Software;Incl 6502 CPU,16k RAM,14k ROM,Disk Drives	RKW
79	R6592	R6500	IO-08	Chip	MNG	Single Chip; On Chip 5x7 Dot Matrix Character Generation	RKW
80	R6545	R6500	IO-09	Chip	MNG	CRT Controller(CRTC):Address Refresh RAM to 16k Characters	RKW
81	R6545AC	R6500	IO-09	Chip	MNG	CRT Controller (CRTC); Addr Refresh RAM 16k Character; Freq 2MHz; Plastic	RKW
82	R6545AP	R6500	IO-09	Chip	MNG	CRT Controller (CRTC); Addr Refresh RAM 16k Character; Freq 2MHz; Plastic	RKW
83	R6545C	R6500	IO-09	Chip	MNG	CRT Controller (CRTC); Addr Refresh RAM 16k Character; Freq 1MHz; Plastic	RKW
84	R6545P	R6500	IO-09	Chip	MNG	CRT Controller (CRTC); Addr Refresh RAM 16k Character; Freq 1MHz; Plastic	RKW
85	R6541	R6500	IO-10	Chip	MNG	Programmable Keyboard/Display Controller(PKDC),2.0/1.0MHz	RKW
86	R6551AC	R6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,2.0MHz,0° to 70°C,28 Pin Ceramic Pkg	RKW
87	R6551ACE	R6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,2.0MHz,-40° to 85°C,28 Pin Ceramic Pkg	RKW
88	R6551AP	R6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,2.0MHz,0° to 70°C,28 Pin Plastic Pkg	RKW
89	R6551C	R6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,1.0MHz,0° to 70°C,28 Pin Ceramic Pkg	RKW
90	R6551CE	R6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,1.0MHz,-40° to 85°C,28 Pin Ceramic Pkg	RKW
91	R6551P	R6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,1.0MHz,0° to 70°C,28 Pin Plastic Pkg	RKW
92	R6520	R6500	IO-30	Chip	MNG	Peripheral Interface Adapter;8 Bit Parallel I/O;Pkg,Temp,Speed Variations	RKW
93	R6522	R6500	IO-30	Chip	MNG	Versatile Interface Adapter,Reg for Ser Operation;Pkg Temp,Speed Variatns	RKW
94	RLM658	R6500	IO-55	MOD	MNG	1 Megabit Linear Bubble Memory Mod:Uses 4 Parallel RBM256s	RKW
95	R6530	R6500	IO-57	Chip	MNG	Combination ROM,RAM,I/O and Timer;Pkg,Temp,Speed Variations	RKW
96	R6531AQ	R6500	IO-57	Chip	MNG	ROM/RAM/IO Counter(RRIOC):2k/128 ROM/RAM,0° to 70°C,2.0MHz,52 Pin Pl Pkg	RKW
97	R6531C	R6500	IO-57	Chip	MNG	ROM/RAM/IO Counter(RRIOC):2k/128 ROM/RAM,0° to 70°C,40 Pin Cer Pkg	RKW
98	R6531CE	R6500	IO-57	Chip	MNG	ROM/RAM/IO Counter(RRIOC):2k/128 ROM/RAM,-40° to 85°C,40 Pin Cer Pkg	RKW
99	R6531P	R6500	IO-57	Chip	MNG	ROM/RAM/IO Counter(RRIOC):2k/128 ROM/RAM,0° to 70°C,40 Pin Plastic Pkg	RKW
100	R6531Q	R6500	IO-57	Chip	MNG	ROM/RAM/IO Counter(RRIOC):2k/128 ROM/RAM,0° to 70°C,52 Pin Plastic Pkg	RKW
101	R6532	R6500	IO-57	Chip	MNG	Combination RAM,I/O, and Timer;Pkg,Temp,Speed Variations Available	RKW
102♦	R6534P	R6500	IO-57	Chip	MNG	ROM-I/O-Counter:4096 X 8 Mask Prog ROM;8 Bit Serial Ch;26 I/O Lines	RKW
103♦	R6534Q	R6500	IO-57	Chip	MNG	ROM-I/O-Counter:4096 X 8 Mask Prog ROM;8 Bit Serial Ch;26 I/O Lines	RKW
104	M65-031	R6500	RAM	MOD	MNG	16k Byte RAM Implem W/32 R2114 1024x4 Static RAMs,tac 450ns(1MHz)	RKW
105	M65-032	R6500	RAM	MOD	MNG	16k Byte RAM Implem W/32 R2114 1024x4 Static RAMs,tac 250ns(2MHz)	RKW
106	R2316BC	R6500	ROM	Chip	MNG	2048x8 Static ROM,450ns Access;250ns Chip Select;Ceramic,DIP,Tri State	RKW
107	R2316BP	R6500	ROM	Chip	MNG	2048x8 Static ROM,450ns Access;250ns Chip Select;Plastic,DIP,TTL Compat	RKW
108	R2316EC	R6500	ROM	Chip	MNG	2048x8 Static ROM,450ns Access;120ns Chip Select;Ceramic,DIP,Tri State	RKW
109	R2316EP	R6500	ROM	Chip	MNG	2048x8 Static ROM,450ns Access;120ns Chip Select;Plastic,DIP,TTL Compat	RKW
110	R2332-3C	R6500	ROM	Chip	MNG	4096x8 Static ROM;Access Time 300ns max;Ceramic DIP Pkg	RKW

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	R2332C	R6500	ROM	Chip	MNG	4096x8 Static ROM;Access Time 450ns max;Ceramic DIP Pkg	RKW
2	R2332P	R6500	ROM	Chip	MNG	4096x8 Static ROM;Access Time 450ns max;Plastic DIP Pkg	RKW
3	M65-045	R6500	ROM	MOD	MNG	PROM/ROM Mod;16k Byte x8,Accepts 2708,2716 PROMs/2316,2332 ROMs	RKW
4	M65-040	SYS65	PROM	MOD		PROM Programmer Module	RKW
5#	HEF4738VE	2650,3000	IO-33	Chip	MCX	IEC/IEEE Bus Interface:Connects Progm/Non Progm Equipt to IEC/IEEE Bus	RTCF
6#	HEF4738VP	2650,3000	IO-33	Chip	MCX	IEC/IEEE Bus Interface:Connects Progm/Non Progm Equipt to IEC/IEEE Bus	RTCF
7	2901ADC	Am2900	CPU	Chip	BTD	4 Bit Slice;Improved Replacement for Am2901;0° to 70°C;Hermetic DIP	RTN
8	2901ADM	Am2900	CPU	Chip	BTD	4 Bit Slice;Improved Replacement for Am2901;-55° to 125°C;Hermetic DIP	RTN
9	2901AFM	Am2900	CPU	Chip	BTD	4 Bit Slice;Improved Replacement for Am2901;-55° to 125°C;Flat Pack	RTN
10	2901APC	Am2900	CPU	Chip	BTD	4 Bit Slice;Improved Replacement for Am2901;0° to 70°C;Molded DIP	RTN
11	R29693DC	Am2900	IO-43	Chip		10 Input Quad 8 to 1 Programmable Multiplexer PMUX,0 to 75°C,DIP	RTN
12	R29693DM	Am2900	IO-43	Chip		10 Input Quad 8 to 1 Programmable Multiplexer PMUX,-55 to 125°C,DIP	RTN
13	R29693FM	Am2900	IO-43	Chip		10 Input Quad 8 to 1 Programmable Multiplexer PMUX,-55 to 125°C,FP	RTN
14	R29613DC	Am2900	PROM	Chip	BTX	512x4 Bit;Power Switched Thru Chip Select;Tri-State;Hermetic DIP	RTN
15	R29613DM	Am2900	PROM	Chip	BTX	512x4 Bit;Power Switched Thru Chip Select;Tri-State;Hermetic DIP	RTN
16	R29613FM	Am2900	PROM	Chip	BTX	512x4 Bit;Power Switched Thru Chip Select;Tri-State;Flatpack	RTN
17	R29623DC	Am2900	PROM	Chip	BTD	512 x 8 Bit;Power Switched Thru Chip Select;Tri State;Hermetic DIP	RTN
18	R29623DM	Am2900	PROM	Chip	BTD	512 x 8 Bit;Power Switched Thru Chip Select;Tri State;Hermetic DIP	RTN
19	R29623FM	Am2900	PROM	Chip	BTD	512 x 8 Bit;Power Switched Thru Chip Select;Tri State;Flatpack	RTN
20	R29631DC	Am2900	PROM	Chip	BTD	1024x8 Bit PROM;Access Time 70ns;Tri State;0 to 75°C;DIP	RTN
21	R29631DM	Am2900	PROM	Chip	BTD	1024x8 Bit PROM;Access Time 90ns;Tri State;-55 to 125°C;DIP	RTN
22	R29633DC	Am2900	PROM	Chip	BTD	1024x8 Bit;Pwr Switched Thru Ch Sel;Tri State;0 to 75°C;DIP	RTN
23	R29633DM	Am2900	PROM	Chip	BTD	1024x8 Bit;Pwr Switched Thru Ch Sel;Tri State;-55 to 125°C;DIP	RTN
24	R29635DC	Am2900	PROM	Chip	BTD	1024x8 Bit PROM;Access Time 70ns;Tri State;0 to 75°C;DIP	RTN
25	R29635DM	Am2900	PROM	Chip	BTD	1024x8 Bit PROM;Access Time 90ns;Tri State;-55 to 125°C;DIP	RTN
26	R29637DC	Am2900	PROM	Chip	BTD	1024x8 Bit;Pwr Switched Thru Ch Sel;Tri State;0 to 75°C;DIP	RTN
27	R29637DM	Am2900	PROM	Chip	BTD	1024x8 Bit;Pwr Switched Thru Ch Sel;Tri State;-55 to 125°C;DIP	RTN
28	R29651DC	Am2900	PROM	Chip	BTD	2048x4 Bit PROM;Access Time 75ns;Tri State;0 to 75°C;DIP	RTN
29	R29651DM	Am2900	PROM	Chip	BTD	2048x4 Bit PROM;Access Time 95ns;Tri State;-55 to 125°C;DIP	RTN
30	R29653DC	Am2900	PROM	Chip	BTD	2048x4 Bit;Pwr Switched Thru Ch Sel;Tri State;0 to 75°C;DIP	RTN
31	R29653DM	Am2900	PROM	Chip	BTD	2048x4 Bit;Pwr Switched Thru Ch Sel;Tri State;-55 to 125°C;DIP	RTN
32	R29681DC	Am2900	PROM	Chip	BTD	2048x8 Bit PROM;Access Time 80ns;Tri State;0 to 75°C;DIP	RTN
33	R29681DM	Am2900	PROM	Chip	BTD	2048x8 Bit PROM;Access Time 100ns;Tri State;-55 to 125°C;DIP	RTN
34	R29683DC	Am2900	PROM	Chip	BTD	2048x8 Bit;Pwr Switched Thru Ch Sel;Tri State;0 to 75°C;DIP	RTN
35	R29683DM	Am2900	PROM	Chip	BTD	2048x8 Bit;Pwr Switched Thru Ch Sel;Tri State;-55 to 125°C;DIP	RTN
36#	MICRAL-C	MICRAL	COMP	UNIT		8 Bit Syst;8080 CPU;24k RAM Basic,Mem to 64k,Key Bd,CRT,Diskette	R2E
37#	MICRAL-M	MICRAL	COMP	UNIT		8 Bit System;512k Memory,2816 I/O Devices,64 Buffered Chan	R2E
38#	MICRAL-S	MICRAL	COMP	UNIT		8 Bit System;64k Memory,352 I/O Devices,8 Buffered Chan	R2E
39	MIK11/2A	MIK11	COMP	UNIT		CAMAC Sys uC using LSI11/2;Async Port,Dataway Interface	SEC
40	MIK11/2C	MIK11	COMP	UNIT		Same as MK11/2A But With 32k RAM	SEC
41	MIK11/2S	MIK11	COMP	UNIT		Auxiliary Version of MK11/2A for Use With Other Computers	SEC
42	RAM11/16	MIK11	RAM	UNIT		16k Dynamic RAM W/Refresh,256 words PROM	SEC
43	RAM11/32	MIK11	RAM	UNIT		32k Dynamic RAM W/Refresh,256 words PROM	SEC
44#	M3856B1		IO-55		MNX	Prog/Data Storage;Prog/Data Counters, Plastic Pkg	SGAI
45#	M3857B1		IO-55	Chip	MNX	Prog/Data Storage;Prog/Data Counters, Stat Mem Interface,Plastic Pkg	SGAI
46#	M3856D1		10-55		MNX	Prog/Data Storage;Prog/Data Counters, Ceramic Slam Pkg	SGAI
47#	M3870B1	F8	uCT	Chip	MNG	8 Bit Single-Chip Microcomputer,Dual In-Line Plastic Package	SGAI
48#	M3870D1	F8	uCT	Chip	MNG	8 Bit Single-Chip Microcomputer,Dual In-Line Ceramic Slam Package	SGAI
49#	NBF8	F8	COMP	MOD		F8 Based Nanocomputer,1kB Mem for User,2kB Monitor Prog on ROM,Disp/Keyb	SGAI
50#	NBF8-S	F8	COMP	MOD		Same as NBF8,Including Box,Power Supply,Cables and Bread-Board	SGAI
51#	M3857D1	F8	IO-55	Chip	MNX	Prog/Data Storage;Prog/Data Counters,Stat Mem Interf,Ceramic Slam Pkg	SGAI
52#	CLZ80-4	Z80	COMP	MOD		Microcomputer Board;4k Byte RAM	SGAI
53#	CLZ80-4/2	Z80	COMP	MOD		Microcomputer Board;4k Byte RAM	SGAI
54#	CLZ80-4/8	Z80	COMP	MOD		Microcomputer Board,4k Byte RAM,Monitor/Debugger/Editor/Assembler Softw	SGAI
55#	CLZ80-16	Z80	COMP	MOD		Microcomputer Board;16k Byte RAM	SGAI
56#	CLZ80-16/2	Z80	COMP	MOD		Same as CLZ80-4/2,But with 16k Byte RAM	SGAI
57#	CLZ80-16/8	Z80	COMP	MOD		Same as CLZ80-4/8,But with 16k Byte RAM	SGAI
58#	NBZ80	Z80	COMP	MOD		Z80 Based Nanocomputer,4kB RAM,2kB Monitor Prog on EPROM,Display/Keyb	SGAI
59#	NBZ80-S	Z80	COMP	MOD		Same As NBZ80,Including Box,Power Supply,Cables and Bread-Board	SGAI
60#	Z80-CPUB1	Z80	CPU	Chip	MNG	8 Bit Microprocess;Clock Freq 2.5MHz Max,Temp 0 to 70°C;Plastic Pkg	SGAI
61#	Z80-CPUD1	Z80	CPU	Chip	MNG	8 Bit Microprocess;Clock Freq 2.5MHz Max,Temp 0 to 70°C;Ceramic Pkg	SGAI
62#	Z80A-CPUB1	Z80	CPU	Chip	MNG	8 Bit Microprocess;Clock Freq 4.0MHz Max,Temp 0 to 70°C;Plastic Pkg	SGAI
63#	Z80A-CPUD1	Z80	CPU	Chip	MNG	8 Bit Microprocess;Clock Freq 4.0MHz Max,Temp 0 to 70°C;Ceramic Pkg	SGAI
64#	PPZ80-B	Z80	DEV	MOD	MNG	Same as PPZ80-S;w/Separated Socket and Connecting Cable	SGAI
65#	PPZ80-ES	Z80	DEV	MOD	MNG	Same as PPZ80-S;w/4 ROM/PROM/EPROM Sockets;Memory Expansion up to 8k	SGAI
66#	PPZ80-S	Z80	DEV	MOD	MNG	EPROM Programming Board,Comp with M2704,08,58,16,32,UV Erasable EPROMs	SGAI
67#	Z80-CTCB1	Z80	IO-01	Chip	MNG	Counter Timer Ckt,Programmable 4 Chan for Data Comm,Clock 400ns Min,Plast	SGAI
68#	Z80-CTCD1	Z80	IO-01	Chip	MNG	Counter Timer Ckt,Programmable 4 Chan for Data Comm,Clock 400ns Min,Ceram	SGAI
69#	Z80A-CTCB1	Z80	IO-01	Chip	MNG	Counter Timer Ckt,Programmable 4 Chan for Data Comm,Clock 250ns Min,Plast	SGAI
70#	Z80A-CTCD1	Z80	IO-01	Chip	MNG	Counter Timer Ckt,Programmable 4 Chan for Data Comm,Clock 250ns Min,Ceram	SGAI
71#	Z80-DMAB1	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Chan;Plastic Pkg	SGAI
72#	Z80-DMAD1	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Chan;Ceramic Pkg	SGAI
73#	Z80A-DMAB1	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Chan;Plastic Pkg	SGAI
74#	Z80A-DMAD1	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Chan;Ceramic Pkg	SGAI
75#	VDZ80	Z80	IO-09	MOD	MNG	Video Display Board,With Outputs for Video Monitor or Commercial TV Rec	SGAI
76#	Z80-SIOB1	Z80	IO-20	Chip	MNG	Serial Input/Output Ckt;Programmable Dual Chan for Data Comm;Plastic Pkg	SGAI
77#	Z80-SIOD1	Z80	IO-20	Chip	MNG	Serial Input/Output Ckt;Programmable Dual Chan for Data Comm;Ceramic Pkg	SGAI
78▼#	Z80ASIO0B1	Z80	IO-20	Chip	MNG	Dual-Ch;Multifunction Peripheral Component:Clk Per 250ns min	SGAI
79▼#	Z80ASIO0D1	Z80	IO-20	Chip	MNG	Dual-Ch;Multifunction Peripheral Component:Clk Per 250ns min	SGAI
80▼#	Z80ASIO1B1	Z80	IO-20	Chip	MNG	Dual-Ch;Multifunction Peripheral Component:Clk Per 250ns min	SGAI
81▼#	Z80ASIO1D1	Z80	IO-20	Chip	MNG	Dual Ch,Multifunction Peripheral Component:Clk Period 250ns min	SGAI
82▼#	Z80ASIO2B1	Z80	IO-20	Chip	MNG	Dual-Ch;Multifunction Peripheral Component:Clk Per 250ns min	SGAI
83▼#	Z80ASIO2D1	Z80	IO-20	Chip	MNG	Dual Ch,Multifunction Peripheral Component:Clk Period 250ns min	SGAI
84▼#	Z80SIO0B1	Z80	IO-20	Chip	MNG	Dual-Ch,Multifunction Peripheral Component:Clk Per 400ns min	SGAI
85▼#	Z80SIO0D1	Z80	IO-20	Chip	MNG	Dual-Ch,Multifunction Peripheral Component:Clk Per 400ns min	SGAI
86▼#	Z80SIO1B1	Z80	IO-20	Chip	MNG	Dual-Ch,Multifunction Peripheral Component:Clk Per 400ns min	SGAI
87▼#	Z80SIO1D1	Z80	IO-20	Chip	MNG	Dual-Ch;Multifunction Peripheral Component:Clk Per 400ns min	SGAI
88▼#	Z80SIO2B1	Z80	IO-20	Chip	MNG	Dual-Ch,Multifunction Peripheral Component:Clk Per 400ns min	SGAI
89▼#	Z80SIO2D1	Z80	IO-20	Chip	MNG	Dual-Ch;Multifunction Peripheral Component:Clk Per 400ns min	SGAI
90▼#	Z80SIO9B1	Z80	IO-20	Chip	MNG	Serial to Parallel,Parallel to Serial Converter Controller;VCC 5.0V	SGAI
91▼#	Z80SIO9D1	Z80	IO-20	Chip	MNG	Serial to Parallel,Parallel to Serial Converter Controller;VCC 5.0V	SGAI
92#	Z80-PIOB1	Z80	IO-30	Chip	MNG	Parallel I/O(PIO)Interface Controller;Programmable 2 Port,Plastic Pkg	SGAI
93#	Z80-PIOD1	Z80	IO-30	Chip	MNG	Parallel I/O(PIO)Interface Controller;Programmable 2 Port,Ceramic Pkg	SGAI
94#	Z80A-PIOB1	Z80	IO-30	Chip	MNG	Parallel I/O(PIO)Interface Controller;Programmable 2 Port,Plastic Pkg	SGAI
95#	Z80A-PIOD1	Z80	IO-30	Chip	MNG	Parallel I/O(PIO)Interface Controller;Programmable 2 Port,Ceramic Pkg	SGAI
96#	PIZ80	Z80	IO-33	MOD	MNG	I/O Module,Including 8 Parallel Bidirectional I/O Ports	SGAI
97#	FLZ80	Z80	PE-01	UNIT	MNG	Floppy Disk Interface,Up to 4 Drives	SGAI
98#	RCZ80	Z80	PE-04	UNIT		Cassette Rec for CLZ80, NBZ80,NBZ80-S, NBF8, NBF8-S;RequiresW4Z80 Cable	SGAI
99#	SSZ80	Z80	PE-10	UNIT	MNG	Serial Printer and Interface,Impact Printing on 81/2 inch Paper,36-96 Col	SGAI
100#	TVZ80	Z80	PE-15	UNIT	MNG	Video Monitor Display for Use with VDZ80 or VTZ80	SGAI
101#	VTZ80	Z80	PE-23	UNIT	MNG	Stand Alone Video Terminal Using the VDZ80 Board	SGAI
102#	ALZ80	Z80	PE-60	UNIT		Power Supply, 15A/5V;To Be Used with CTZ80 Card Cage	SGAI
103#	NPF8	Z80	PE-60	UNIT		Mini Power Supply for NBF8 Nancomputer	SGAI
104#	NPZ80	Z80	PE-60	UNIT		Mini Power Supply for NBZ80 Nancomputer	SGAI
105#	NKF8	Z80	PE-61	UNIT		Calculator Style Keyboard/Display for NBZ8 Nancomputerr	SGAI
106#	NKZ80	Z80	PE-61	UNIT		Calculator Style Keyboard/Display for NBZ80 Nancomputer	SGAI
107#	RAZ80-16	Z80	RAM	MOD	MNG	16k Byte RAM Extension Plus 4 E/P/ROM Sockets	SGAI
108#	RAZ80-32	Z80	RAM	MOD	MNG	Same as RAZ80-16,But with 32k Byte RAM	SGAI
109#	RAZ80-48	Z80	RAM	MOD	MNG	Same as RAZ80-16,But with 48k Byte RAM	SGAI
110#	RAZ80-64	Z80	RAM	MOD	MNG	Same as RAZ80-16,But with 64k Byte RAM	SGAI

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1#	KNZ80	Z80	10-33	MOD		Conversion Kit;Converts NPZ80 into a CLZ80 4/2 Microcomputer Board	SGAI
2▼#	Z8001CPUD1	Z8000	CPU	Chip	MNG	Segmented 48 Pin;16-16 Bit Gen-Purpose Registers;414 Instruction Set	SGAI
3▼#	Z8002CPUD1	Z8000	CPU	Chip	MNG	Non-Segmented 40 Pin;16-16 Bit Gen Purpose Registers;414 Instr. Set	SGAI
4	2652-1I		IO-20	Chip	MNX	Multi-Protocol Communication Controller; Single 5V Supply; Ceramic Dip	SIC
5	2652-1N		IO-20	Chip	MNX	Multi-Protocol Communication Controller; Single 5V Supply; Plastic Dip	SIC
6	2652N		IO-20	Chip	MNX	Multi-Protocol Communication Controller; Single 5V Supply; Plastic Dip	SIC
7	2661-1I		IO-30	Chip	MNG	EPIC; Universal Syn/Asyn Data Commun. Cont. Baud Rate 50.19.2kbps Cer	SIC
8	2661-1N		IO-30	Chip	MNG	EPIC; Universal Syn/Asyn Data Commun. Cont. Baud Rate 50-19.2kbps Plas	SIC
9	2661-2I		IO-30	Chip	MNG	EPIC; Universal Syn/Asyn Data Commun. Cont. Baud Rate 45.4-38.4kbps Cer	SIC
10	2661-2N		IO-30	Chip	MNG	EPIC; Universal Syn/Asyn Data Commun. Cont. Baud Rate 45.5-38.4kbps Plas	SIC
11	2661-3I		IO-30	Chip	MNG	EPIC; Universal Syn/Asyn Data Commun. Cont. Baud Rate 50-19.2kbps Cer	SIC
12	2661-3N		IO-30	Chip	MNG	EPIC; Universal Syn/Asyn Data Commun. Cont. Baud Rate 50-19.2kbps Plas	SIC
13▼	N82S106F		IO-30	Chip	BTX	Field Programmable ROM Patch;Open Collector;Access Time 70ns;Ceramic Dip	SIC
14	N82S106N		IO-30	Chip	BTX	Field Programable ROM Patch;Open Collector;Access Time 70ns;Plastic Dip	SIC
15▼	N82S107F		IO-30	Chip	BTX	Field Programmable ROM Patch;Tri-State;Access Time 70ns;Ceramic Dip	SIC
16	N82S107N		IO-30	Chip	BTX	Field Programable ROM Patch;Tri State;Access Time 70ns;Plastic Dip	SIC
17▼	S82S106F		IO-30	Chip	BTX	Field Programmable Rom Patch;Open Collector;Access Time 100ns;Ceramic Dip	SIC
18	S82S106N		IO-30	Chip	BTX	Field Programable ROM Patch;Open Collector;Access Time 100nS;Plastic Dip	SIC
19▼	S82S107F		IO-30	Chip	BTX	Field Programmable Rom Patch;Tri-State;Access Time 100ns;Ceramic Dip	SIC
20	S82S107N		IO-30	Chip	BTX	Field Programable ROM Patch; Tri State; Access Time 100ns Plastic Dip	SIC
21	8T95F		IO-31	Chip	BTX	Hex Buffer; Tri State; Prog Delay 9.0/7.0ns On/Off	SIC
22	8T95N		IO-31	Chip	BTX	Hex Buffers; Tri State Prog Delay 9.0/7.0ns On/Off	SIC
23	8T96F		IO-31	Chip	BTX	Hex Buffer; Tri State; Prog Delay 6.0/7.0ns On/Off	SIC
24	8T96N		IO-31	Chip	BTX	Hex Buffers; Tri State Prog Delay 6.0/7.0ns On/Off	SIC
25	8T97F		IO-31	Chip	BTX	Hex Inverter; Tri State; Prog Delay 9.0/7.0ns On/Off	SIC
26	8T97N		IO-31	Chip	BTX	Hex Inverter; Tri State; Prog Delay 9.0/7.0ns On/Off	SIC
27	8T98F		IO-31	Chip	BTX	Hex Inverter; Tri State; Prog Delay 6.0/7.0ns On/Off	SIC
28	8T98N		IO-31	Chip	BTX	Hex Inverter; Tri State; Prog Delay 6.0/7.0ns On/Off	SIC
29▼	8X02I,XL		IO-34	Chip	BTD	Control Store Sequencer:1024 uInstruction Addressability;N-way Branch	SIC
30	MP8255I	MP8080A	IO-30	Chip		Programmable Peripheral Interface	SIC
31	N8X01N	N8x300	IO-20	Chip	BIX	CRC Generator/Checker;Data Rate 10MHz max,Plas Pkg	SIC
32	N8T32F	N8x300	IO-33	Chip		8 Bit Latched Addressable Bidir I/O Port;3 State Sync User Port,Cer Pkg	SIC
33	N8T32N	N8x300	IO-33	Chip		8 Bit Latched Addressable Bidir I/O Port;3 State Sync User Port,Plas Pkg	SIC
34	N8T33F	N8x300	IO-33	Chip		8 Bit Latched Addressable Bidir I/O Port;Open Col Syn User Port,Cer Pkg	SIC
35	N8T33N	N8x300	IO-33	Chip		8 Bit Latched Addressable Bidir I/O Port;Open Col Syn User Port,Plas Pkg	SIC
36	N8T35F	N8x300	IO-33	Chip		8 Bit Latched Addressable Bidir I/O Port;Open Col Asyn User Port,Cer Pkg	SIC
37	N8T35N	N8x300	IO-33	Chip		8 Bit Latched Addressable Bidir I/O Port;Open Col Asyn User Port,Plas Pkg	SIC
38	N8T36F	N8x300	IO-33	Chip		8 Bit Latched Addressable Bidir I/O Port;3 State Asyn User Port,Cer Pkg	SIC
39	N8T36N	N8x300	IO-33	Chip		8 Bit Latched Addressable Bidir I/O Port;3 State Asyn User Port,Plas Pkg	SIC
40	N8T39I	N8x300	IO-33	Chip		Bus Expander:Can Buffer Block of 16 I/O Ports;Ceramic Pkg	SIC
41	N8T39N	N8x300	IO-33	Chip		Bus Expander:Can Buffer Block of 16 I/O Ports;Plastic Pkg	SIC
42	N8T58I	N8x300	IO-33	Chip	BTD	Transparent Bus Expander;Prop Delay 15ns max;Cer Pkg	SIC
43	N8T58N	N8x300	IO-33	Chip	BTD	Transparent Bus Expander;Prop Delay 15ns max;Plas Pkg	SIC
44	N8X300	N8X300	COMP	MOD		Fixed Instruction Microcomputer System	SIC
45	N8X300I	N8X300	CPU	Chip	BTD	8 Bit Microprocessor;Interpreter	SIC
46	8X300KT100SK	N8X300	DEV	MOD		N8X300 Designers Evaluation Kit	SIC
47	N8X01F	N8X300	IO-20	Chip	BIX	CRC Generator/Checker;Data Rate 10 MHz max,Cer Pkg	SIC
48	ISP-8A/600I	SC/MP-II	CPU	Chip	MNG	8 Bit Single Chip Microprocessor SC/MP-II	SIC
49	2650	2650	CPU	Chip	MNG	8 Bit Microprocessor	SIC
50	2650KT9000	2650	DEV	MOD		Microprocessor Prototyping Kit;2650 CPU,256x4 RAM,4k PROM,8 Bit I/O Port	SIC
51	2650KT9500	2650	DEV	MOD		Prototyping Card;Includes 2650,512 Bytes RAM,1k Byte ROM,I/O	SIC
52	2650PC1001	2650	DEV	MOD	MNG	Microprocessor Prototyping Card;1k Byte ROM/ROM,8 Bit I/O Ports;DMA	SIC
53	2650PC1500	2650	DEV	MOD		Preassembled and Tested 2650KT9500 Prototyping Card	SIC
54	PC-4000	2650	DEV	MOD		PC-Board Emulator for 2656 Mem Interface Chip	SIC
55	TWIN	2650	DEV	MOD		Microcomputer Prototype Development System(TWIN);Soft/Hardware	SIC
56	2650DS2000	2650	DEV	UNIT		Microprocessor Demostration System;RS232 And TTY Interface	SIC
57	INSTRUCTOR50	2650	DEV	UNIT		uProc Learning Pkg;S100 IF For Sys Exp;512 Bytes On-Board RAM	SIC
58	2650PC3000	2650	IO-04	MOD		Intelligent Typewriter Controller;Var Band Rate,Storage 250 Char	SIC
59	N2651I	2650	IO-20	Chip		Programmable Communication Interface	SIC
60	N2652-1I	2650	IO-20	Chip		Multi Protocol Communications Controller (MPCC);Clock Freq 2.0MHz max	SIC
61	N2652I	2650	IO-20	Chip		Multi-Protocol Communication Cont Data Rate DC to 500kb/s	SIC
62	N2655I	2650	IO-30	Chip		Programmable Peripheral Interface PPI;3.0MHz Progm Timer	SIC
63	N2656I	2650	IO-57	Chip		System Memory Interface;2kx8 ROM,128x8 RAM,I/O	SIC
64	N82S123F	2650	PROM	Chip	BTX	32x8 ROM;Tri-State	SIC
65▼	N82S123N	2650	PROM	Chip	BTX	32 x 8 ROM;Tri-State	SIC
66	S82S123F	2650	PROM	Chip	BTX	32x8 ROM;Tri-State	SIC
67	2606-1B	2650	RAM	Chip	MNG	256x4 RAM for Peripheral,Terminals,Data Buffers	SIC
68	2650PC2000	2650	RAM	MOD	MNX	LK Memory Card;Uses 21L02,1kx1 Bit Static RAM,Single Plus 5V Supply	SIC
69	N2901-1I	2900	CPU	Chip	BTX	4 Bit Microprocessor	SIC
70	N3001,2	3000	CPU	ChS	BTD	4 Bit N3001-Microprogram Control Unit;N3002 Central Processing Element	SIC
71	S3001,2	3000	CPU	ChS	BTD	4 Bit N3001 Microprogram Control Unit;N3002 Central Processing Element	SIC
72	3000KT1000SK	3000	DEV	MOD		Designers Evaluation Kit	SIC
73	3000KT8080SK	3000	DEV	MOD		Bipolar Emulation Kit for 3000 Series:An 8080 System Emulator	SIC
74▼	N82S100F	3000	FPLA	Chip	BTX	16 x 48 x 8 FPLA; 48 Product Terms;8 Sum Terms;Tri-State Output	SIC
75▼	N82S101F	3000	FPLA	Chip	BTX	16 x 48 x 8 FPLA; 48 Product Terms;8 Sum Terms;Open Collector Output	SIC
76▼	N82S102F	3000	FPLA	Chip	BTX	16 x 9 Field Programmable Gate Array;Open Collector;6 In/9 Out Function	SIC
77	N82S102N	3000	FPLA	Chip	BTX	16x9 Field Programmable Gate Array;Open Coll;6 In/9 Out Funct	SIC
78▼	N82S103F	3000	FPLA	Chip	BTX	16 x 9 Field Programmable Gate Array;Tri-State;6 In/9 Out Function	SIC
79	N82S103N	3000	FPLA	Chip	BTX	16x9 Field Programmable Gate Array;Tri State;6 In/9 Out Funct	SIC
80	N82S200I	3000	FPLA	Chip	BTX	16x48x8 Mask Programmable Logic Array;Tri State,0 to 75°C	SIC
81	N82S200N	3000	FPLA	Chip	BTX	16x48x8 Mask Programmable Logic Array;Tri State;0 to 75°C	SIC
82	N82S201I	3000	FPLA	Chip	BTX	16x48x8 Mask Programmable Logic Array;Open Coll,0 to 75°C	SIC
83	N82S201N	3000	FPLA	Chip	BTX	16x48x8 Mask Programmable Logic Array;Open Coll;0 to 75°C	SIC
84▼	S82S100F	3000	FPLA	Chip	BTX	16 x 48 x 8 FPLA;48 Product Terms;8 Sum Terms;Tri-State Output	SIC
85▼	S82S101F	3000	FPLA	Chip	BTX	16 x 48 x 8 FPLA;48 Product Terms;8 Sum Terms;Open Collector Output	SIC
86▼	S82S102F	3000	FPLA	Chip	BTX	16 x 9 Field Programmable Gate Array;Open Collector;6 In/9 Out Functions	SIC
87▼	S82S103F	3000	FPLA	Chip	BTX	16 x 9 Field Programmable Gate Array;Tri-State;6 In/9 Out Functions	SIC
88	S82S200I	3000	FPLA	Chip	BTX	16x48x8 Mask Programmable Logic Array;Tri State;-55 to 125°C	SIC
89	S82S201I	3000	FPLA	Chip	BTX	16x48x8 Mask Programmable Logic Array;Open Coll;-55 to 125°C	SIC
90	N8X02I	3000	IO-01	Chip	BTX	Control Store Sequencer,Controls Fetch Seq of Microinstructions,Cer Pkg	SIC
91	N8X02N	3000	IO-01	Chip	BTX	Control Store Sequencer,Controls Fetch Seq of Microinstructions,Plas Pkg	SIC
92	N8T26AB	3000	IO-21	Chip	BTX	Quad Bus Transceiver;Tri-State for Inverting Output	SIC
93	N8T26AF	3000	IO-21	Chip	BTX	Quad Bus Transceiver;Tri-State for Inverting Output	SIC
94	N8T28B	3000	IO-21	Chip	BTX	Quad Bus Transceiver;Non Inverting Output Tri-State	SIC
95	N8T28F	3000	IO-21	Chip	BTX	Quad Bus Transceiver;Non Inverting Output Tri-State	SIC
96	S8T26AB	3000	IO-21	Chip	BTX	Quad Bus Transceiver;Inverting Output Tri-State	SIC
97	S8T26AF	3000	IO-21	Chip	BTX	Quad Bus Transceiver;Inverting Output Tri-State	SIC
98	S8T28B	3000	IO-21	Chip	BTX	Quad Bus Transceiver;Non Inverting Output Tri-State	SIC
99	S8T28F	3000	IO-21	Chip	BTX	Quad Bus Transceiver;Non Inverting Output Tri-State	SIC
100	N8T31F	3000	IO-33	Chip	BTX	8 Bit Bidirectional I/O Port	SIC
101	N8T31N	3000	IO-33	Chip	BTX	8 Bit Bidirectional I/O Port	SIC
102	N74S182B	3000	IO-90	Chip	BTX	High Speed Look Ahead Carry Generator	SIC
103	N74S182F	3000	IO-90	Chip	BTX	High Speed Look Ahead Carry Generator	SIC
104	N74S182W	3000	IO-90	Chip	BTX	High Speed Look Ahead Carry Generator	SIC
105	S54S182B	3000	IO-90	Chip	BTX	High Speed Look Ahead Carry Generator	SIC
106	S54S182F	3000	IO-90	Chip	BTX	High Speed Look Ahead Carry Generator	SIC
107	S54S182W	3000	IO-90	Chip	BTX	High Speed Look Ahead Carry Generator	SIC
108	N82S114I	3000	PROM	Chip	BTD	256x8 PROM	SIC
109▼	N82S115F	3000	PROM	Chip	BTX	512 x 8 PROM	SIC
110	N82S126F	3000	PROM	Chip	BTX	256x4 PROM;Open Collector	SIC

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1▼	N82S126N	3000	PROM	Chip	BTX	256 x 4 PROM;Open Collector	SIC
2	N82S129F	3000	PROM	Chip	BTX	256x4 PROM;Tri-State	SIC
3▼	N82S129N	3000	PROM	Chip	BTX	256 x 4 PROM;Tri-State	SIC
4	S82S126F	3000	PROM	Chip	BTX	256x4 PROM;Open Collector	SIC
5	S82S129F	3000	PROM	Chip	BTX	256x4 PROM;Tri-State	SIC
6▼	N82S09F	3000	RAM	Chip	BTD	64 x 9 Bipolar RAM	SIC
7	N82S10I	3000	RAM	Chip	BTX	1024x1 Bipolar RAM;Open Collector	SIC
8	N82S11I	3000	RAM	Chip	BTX	1024x1 Bipolar RAM;Tri-State	SIC
9	N82S25F	3000	RAM	Chip	BTD	16x4 Bipolar Scratch Pad Memory	SIC
10▼	N82S25N	3000	RAM	Chip	BTD	16 x 4 Bipolar Scratch Pad Memory	SIC
11	N82S116B	3000	RAM	Chip	BTD	256x1 Bipolar RAM;Tri-State	SIC
12	N82S116F	3000	RAM	Chip	BTD	256x1 Bipolar RAM;Tri-State	SIC
13	N82S117B	3000	RAM	Chip	BTD	256x1 Bipolar RAM;Open Collector	SIC
14	N82S117F	3000	RAM	Chip	BTD	256x1 Bipolar RAM;Open Collector	SIC
15▼	S82S09F	3000	RAM	Chip	BTD	64 x 9 Bipolar RAM	SIC
16	S82S10I	3000	RAM	Chip	BTX	1024x1 Bipolar RAM;Open Collector	SIC
17	S82S11I	3000	RAM	Chip	BTX	1024x1 Bipolar RAM;Tri-State	SIC
18	S82S25F	3000	RAM	Chip	BTD	16x4 Bipolar Scratch Pad Memory	SIC
19	MP8035LI	8048	uCT	Chip	MNG	8-Bit uComputer W/External ROM or PROM; 2.5us Cycle; 40-Pin Ceramic Dip	SIC
20	MP8035LN	8048	uCT	Chip	MNG	8-Bit uComputer W/External ROM or PROM; 2.5us Cycle; 40-Pin Plastic Dip	SIC
21	MP8048I	8048	uCT	Chip	MNG	8-Bit uComputer W/Mask ROM; 2.5us Cycle; 40-Pin Ceramic Dip	SIC
22	MP8048N	8048	uCT	Chip	MNG	8-Bit uComputer W/Mask ROM; 2.5us Cycle; 40-Pin Plastic Dip	SIC
23	MP8039I	8049	uCT	Chip	MNG	8-Bit uComputer W/External ROM or EPROM; 1.36us Cycle; 40Pin Ceramic Dip	SIC
24	MP8039N	8049	uCT	Chip	MNG	8-Bit uComputer W/External ROM or EPROM; 1.36us Cycle;40 Pin Plastic Dip	SIC
25	MP8049I	8049	uCT	Chip	MNG	8-Bit uComputer W/Mask ROM;1.36 us Cycle; 40 Pin Ceramic Dip	SIC
26	MP8049N	8049	uCT	Chip	MNG	8-Bit uComputer W/Mask ROM;1.36us Cycle; 40 Pin Plastic Dip	SIC
27	MP8080AI	8080A	CPU	Chip	MNG	8 Bit Microprocessor	SIC
28#	AMS-209	AMS		MOD		Parr I/O,24 Inputs w/Photocouplers and 24 Outputs w/Relays	SIEG
29#	AMS-D208	AMS		MOD		Parr I/O,24 Inputs W/Photocouplers and 24 Outputs W/Photocouplers	SIEG
30#	AMS-D2	AMS	COMP	MOD		CPU,SAB8085A,Interrupt Controller,Timer,Serial I/O,Parallel I/O	SIEG
31#	AMS-D3	AMS	COMP	MOD		CPU,SAB8085A,Interrupt Controller,Timer,Ser I/O,Part I/O,Arith Processor	SIEG
32#	AMS-D126	AMS	PROM	MOD		Memory Card,4kByte Stat CMOS/RAM;3 Sockets for ROM/EPROM(2716,2732)	SIEG
33#	SKC85	SKC85	COMP	MOD		Computer On a Card: 3 MHz 8085A CPU,22 I/O Parts,4k Byte EPROM	SIEG
34#	ECB85	SKC85	DEV	MOD		Exptal Comp On A Card:Uses CPU AM 8085A,44 Par IO Lines,2 Counter	SIEG
35#	SMP-E4	SMP	COMP	MOD		Comp on a Card;3MHz 8085A;2k Bit RAM;16k Bit EPROM;16 Parr I/O;Interr-Con	SIEG
36#	SMP-E8	SMP	COMP	MOD		CPU SAB8088 5MHz,4k RAM,16k EPROM,256 I/O Lines,DMA	SIEG
37#	SMP-E1	SMP	CPU	MOD		CPU and I/O Card;CPU SAB8080A	SIEG
38#	SMP-E2	SMP	CPU	MOD		CPU Serial I/O Card,3MHz 8085A,DMA	SIEG
39#	SMP-E3	SMP	CPU	MOD		CPU Serial I/O Card,3MHz 8085A,DMA,Arithmetic Processor Type AM9511	SIEG
40#	SMP-E3-A1	SMP	CPU	MOD		CPU Serial I/O Card,2MHz 8085A,DMA,Arithmetic Processor Type AM9511	SIEG
41#	SMP-E302	SMP	IO-02	MOD		Prog Interrupt Cont,Timer Card, Interrupt-Inputs,6 Programmable Counters	SIEG
42#	SMP-E303	SMP	IO-02	MOD		Prog Interrupt Cont,Timer Card,16 Interrupt-Inputs,10 Prog Counters	SIEG
43#	SMP-E341	SMP	IO-07	MOD		Floppy Disk-Controller,Single Density,2 Mini-Drivers or 2 Stand Drivers	SIEG
44#	SMP-E347	SMP	IO-07	MOD		Cassette Tape Controller,Mini or Standard Cassettes	SIEG
45#	SMP-STR341	SMP	IO-07	MOD		Software Driver for Floppy Disk Controller SMP-E341	SIEG
46#	SMP-RTOS1	SMP	IO-07	UNIT		Real Time Operating System	SIEG
47#	SMP-E355	SMP	IO-08	MOD		Printer Controller;5x7 Matrix Printing;ASCII	SIEG
48#	SMP-E308	SMP	IO-11	MOD		IEC-Bus-Talker/Listener	SIEG
49#	SMP-E309	SMP	IO-11	MOD		IEC-Bus-Controller	SIEG
50#	SMP-E220	SMP	IO-20	MOD		2 Ch Serial Input/Output Cards,RS232 Port	SIEG
51#	SMP-E200	SMP	IO-30	MOD		Parallel Input/Output Card TTL Level;72 Lines	SIEG
52#	SMP-E211	SMP	IO-30	MOD		Parallel Output w/Photocouplers,2 Channels Each with 8 Outputs	SIEG
53#	SMP-E212	SMP	IO-30	MOD		Parallel Input w/Photocouplers,2 Channels Each with 8 Inputs	SIEG
54#	SMP-E310	SMP	IO-32	MOD		Single Field Switches,64 Key/2 Shift Key,128 Light Driven Diode	SIEG
55#	SMP-E203	SMP	IO-33	MOD		Parallel Output Card w/16 Relays	SIEG
56#	SMP-E206	SMP	IO-33	MOD		Parallel Output w/16 Relays(2A)	SIEG
57#	SMP-E240	SMP	IO-40	MOD		Analog Output Card;4 Analog Outputs,Contains DAC	SIEG
58#	SMP-E230	SMP	IO-41	MOD		Analog Input Card;16 Inputs or 8 Differential Inputs	SIEG
59#	SMP-E420	SMP	PE-60	UNIT		Power Supply for ±5V and ±12V	SIEG
60#	SMP-E421	SMP	PE-60	UNIT		Power Supply for ±15V	SIEG
61#	SMP-MON2-A1	SMP	PROM	Chip		Monitor Program 2kb(2xSAB2708)	SIEG
62#	SMP-MON4	SMP	PROM	Chip		Monitor Program 2kb(1xSAB2716)	SIEG
63#	SMP-BAS1	SMP	PROM	CHIP		BASIC Interpreter (8xSAB2708)	SIEG
64#	SMP-BAS1-A1	SMP	PROM	CHIP		BASIC Interpreter Extension(1xSAB2708) for TTY-I/O	SIEG
65#	SMP-BAS1-A2	SMP	PROM	CHIP		BASIC Interpreter(4xSAB2716)	SIEG
66#	SMP-BAS1-A3	SMP	PROM	CHIP		BASIC Interpreter Extension(1xSAB2716) for TTY-I/O	SIEG
67#	SMP-MON8	SMP	PROM	CHIP		Monitor Program	SIEG
68#	SMP-E120	SMP	PROM	MOD		Memory Card 1k Static RAM,4k EPROM(8708)	SIEG
69#	SMP-E121	SMP	PROM	MOD		Memory Card 8k EPROM(SAB8708)	SIEG
70#	SMP-E123	SMP	PROM	MOD		Memory Card 16k EPROM(SAB2716)	SIEG
71#	SMP-E125	SMP	PROM	MOD		Memory Card 4k Static RAM,16k EPROM(SAB2716)	SIEG
72#	SMP-E126	SMP	PROM	MOD		Memory Card 32k EPROM (2732)	SIEG
73#	SMP-E127	SMP	PROM	MOD		Memory Card 4k Static RAM,32k EPROM(SAB2732)	SIEG
74▼#	SMP-E102	SMP	RAM	MOD		4k Byte Static RAM Memory Card	SIEG
75#	SMP-E103-A1	SMP	RAM	MOD		Memory Card 8k Static RAM	SIEG
76#	SMP-E104	SMP	RAM	MOD		Memory Card 16k Static RAM	SIEG
77#	SMP-E114	SMP	RAM	MOD		Memory Card 16k Dynamic RAM	SIEG
78#	SMP-E115	SMP	RAM	MOD		Memory Card 32k Dynamic RAM	SIEG
79#	SMP-E131	SMP	RAM	MOD		Memory Card 2k Battery Backup CMOS-RAM	SIEG
80#	SMP80-E122	SMP80	PROM	MOD		8 Kilo Byte EPROM Card for SAB2758	SIEG
81#	SMP80-E124	SMP80	PROM	MOD		8 Kilo Byte EPROM Card for SAB2758; 4 Kilo Byte Static RAM Card	SIEG
82#	SMP80-E102	SMP80	RAM	MOD		4 kilo Byte Static RAM Card	SIEG
83#	SMP80-E103	SMP80	RAM	MOD		8 kilo Byte Static RAM Card	SIEG
84	KR2376		IO-10	Chip	MTX	Keyboard Encoder ROM;Contains 2376 Bit ROM;Compatible with DTL/TTL/MOS	SMC
85	COM8017		IO-21	Chip		Universal Async Receiver/Transmitter;TTL Compatible;Full/Half Duplex	SMC
86	COM8502		IO-21	Chip		Universal Async Receiver/Transmitter;TTL Compatible;Full/Half Duplex	SMC
87	COM5016		IO-32	Chip	MTX	Dual Baud Rate Generator;Programmable Divider;2x16 Output Freqs;16 Rates	SMC
88	COM5016T		IO-32	Chip	MTX	Dual Baud Rate Generator;Programmable Divider;Driven by TTL Inputs Only	SMC
89	COM5026		IO-32	Chip	MTX	Baud Rate Generator;Programmable Divider;Crystal Oscillator;16 Output Frq	SMC
90	COM5026T		IO-32	Chip	MTX	Baud Rate Generator;Programmable Divider;Driven by TTL Inputs Only	SMC
91	COM8046		IO-32	Chip	MTX	Baud Rate Generator;Programmable Divider;32 Output Freqs;32 (A)Sync Rates	SMC
92	COM8046T		IO-32	Chip	MTX	Baud Rate Generator;Programmable Divider;External TTL Reference Use	SMC
93	COM8116		IO-32	Chip	MTX	Dual Baud Rate Generator;Programmable Divider;2x16 Output Freqs;16 Rates	SMC
94	COM8116T		IO-32	Chip	MTX	Dual Baud Rate Generator;Programmable Divider;External TTL Reference Use	SMC
95	COM8126		IO-32	Chip	MTX	Baud Rate Generator;Programmable Divider;16 Output Freqs;16 Baud Rates	SMC
96	COM8126T		IO-32	Chip	MTX	Baud Rate Generator;Programmable Divider;External TTL Reference Use	SMC
97	COM8136		IO-32	Chip	MTX	Dual Baud Rate Generator;Programmable Divider;2x16 Output Freqs;16 Rates	SMC
98	COM8136T		IO-32	Chip	MTX	Dual Baud Rate Generator;Programmable Divider;External TTL Reference Use	SMC
99	COM8146		IO-32	Chip	MTX	Baud Rate Generator;Programmable Divider;16 Output Freqs;16 (A)Sync Rates	SMC
100	COM8146T		IO-32	Chip	MTX	Baud Rate Generator;Programmable Divider;External TTL Reference Use	SMC
101	CCC3500	uPC Family	IO-05	Chip	MXX	Cassette/Cartridge Data Handler;Data Transfer Rate 250kbps	SMC
102	FDC3400	uPC Family	IO-07	Chip	MXX	Floppy Disk Hard Sector Data Handler;Single or Double Density Operation	SMC
103	FDC7003	uPC Family	IO-07	Chip	MNX	Floppy Disk Controller;5 Volt Only Supply	SMC
104	CRT5027	uPC Family	IO-09	Chip	MNG	CRT Video Time Controller;Programmable Display/Sync Format	SMC
105	CRT5037	uPC Family	IO-09	Chip	MNG	CRT Video Timer-Controller;Compatible with CRT8002,CRT7004	SMC
106▼	CRT5047	uPC Family	IO-09	Chip		Preprog CRT Video Timer/Controller;80 Char/Data Row;24 Data Rows/Frame	SMC
107	CRT5057	uPC Family	IO-09	Chip	MNG	CRT Video Timer-Controller;Compatible with CRT8002,CRT7004	SMC
108	CRT8002A	uPC Family	IO-09	Chip	MNG	CRT Video Display-Controller,Generator;Shift Reg Freq 20MHz;128 Char 7x11	SMC
109	CRT8002B	uPC Family	IO-09	Chip	MNG	CRT Video Display-Controller,Generator;Shift Reg Freq 15MHz;128 Char 7x11	SMC
110	CRT8002C	uPC Family	IO-09	Chip	MNG	CRT Video Display-Controller,Generator;Shift Reg Freq 10MHz;128 Char 7x11	SMC

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1▼	CRT9007	uPC Family	IO-09	Chip		CRT Video Processor/Controller;Prog 8-240 Char/Data Row;2-256 Data Row/Fr	SMC
2	CRT96364A	uPC Family	IO-09	Chip		CRT Controller;16 Line x 64 Char Display;OSC-50Hz Vertical Sync;Cursor	SMC
3	CRT96364B	uPC Family	IO-09	Chip		CRT Controller;16 Line x 64 Char Display;OSC-60Hz Vertical Sync;Cursor	SMC
4	KR3600	uPC Family	IO-10	Chip		Keyboard Encoder ROM;Contains 3600 Bit ROM;Encodes into 10 Bit Code	SMC
5	COM1671	uPC Family	IO-20	Chip		Asynchronous/Synchronous Transmitter-Receiver,5-8 Bit Characters	SMC
6	COM2017	uPC Family	IO-20	Chip	MPN	UART;Clock Freq 400kHz Max;Strobe 200ns;Full or Half Duplex	SMC
7	COM2017/H	uPC Family	IO-20	Chip	MPN	UART;Clock Freq 640kHz Max;Strobe 200ns;Full or Half Duplex	SMC
8	COM2502	uPC Family	IO-20	Chip	MPN	UART;Clock Freq 400kHz Max;Strobe 200ns;Full or Half Duplex	SMC
9	COM2502/H	uPC Family	IO-20	Chip	MPN	UART;Clock Freq 640kHz Max;Strobe 200ns;Full or Half Duplex	SMC
10	COM2601	uPC Family	IO-20	Chip	MPN	Universal Synchronous Receiver/Transmitter USRT;Full or Half Duplex	SMC
11	COM2651	uPC Family	IO-20	Chip		Programmable Communication Interface;Async/Sync-Full/Half Duplex Oper	SMC
12	COM5025	uPC Family	IO-20	Chip		Universal Synchronous Receiver/Transmitter,8 Or 16 Bit,Tri-State	SMC
13	COM5036	uPC Family	IO-20	Chip	MNX	Dual Baud Rate Gen;Can be Driven by Ext Crystal or TTL	SMC
14	COM5036T	uPC Family	IO-20	Chip	MNX	Dual Baud Rate Gen;Can be Driven by TTL Logic Only	SMC
15	COM5046	uPC Family	IO-20	Chip	MNX	Single Baud Rate Gen;Can be Driven by Ext Crystal or TTL	SMC
16	COM5046T	uPC Family	IO-20	Chip	MNX	Single Baud Rate Gen;Can be Driven by TTL Logic Only	SMC
17	COM8251A	uPC Family	IO-20	Chip	MNX	Universal Sync/Async Receiver/Transmitter;Baud Rate DC to 64k/9.6k	SMC
18	COM1863	uPC Family	IO-21	Chip		Universal Async Receiver/Transmitter;Direct TTL;Full/Half Duplex	SMC
19	COM8018	uPC Family	IO-21	Chip		Universal Async Receiver/Transmitter;Direct TTL Compatible;40k Baud	SMC
20	COM8004	uPC Family	IO-32	Chip	MNX	Dual 32 Bit CRC SDLC Generator/Checker;COM5025,USYNRT Companion	SMC
21	CRT7004A	uPC Family	IO-92	Chip	MNG	Dot Matrix Character Generator;128 Chars 7x11;Shift Freq 20MHz	SMC
22	CRT7004B	uPC Family	IO-92	Chip	MNG	Dot Matrix Character Generator;128 Chars 7x11;Shift Reg Freq 15MHz	SMC
23	CRT7004C	uPC Family	IO-92	Chip	MNG	Dot Matrix Character Generator;128 Chars 7x11;Shift Reg Freq 10MHz	SMC
24▼	CRT9006-83	uPC Family	IO-92	Chip		Single Row Buffer;83 Char;4.0MHz Read/Write Data Rate	SMC
25▼	CRT9006-135	uPC Family	IO-92	Chip		Single Row Buffer;135 Char;4.0MHz Read/Write Data Rate	SMC
26	ROM4732	uPC Family	ROM	Chip	MNX	4096x8 Bit ROM;TTL Compatible;TMS4732,TMS4700,TMS2708,2316E	SMC
27▼	FDC1791	FDC	IO-07	Chip	MXX	Floppy Disk Controller/Formatter;Single/Double Density;Read/Write Mode	SMC
28▼	FDC1792	FDC	IO-07	Chip	MXX	Floppy Disk Controller/Formatter;Single/Double Density;Read/Write Mode	SMC
29▼	FDC1793	FDC	IO-07	Chip	MXX	Floppy Disk Controller/Formatter;Single/Double Density;Read/Write Mode	SMC
30▼	FDC1794	FDC	IO-07	Chip	MXX	Floppy Disk Controller/Formatter;Single/Double Density;Read/Write Mode	SMC
31	CG4103	4100	IO-92	Chip		Character Generator;2240 Bit PROM;64 Chars of 5x7;TTL Compatible	SMC
32	MS3300	SMS	DEV	UNIT		Microcontroller Monitor;Debug And Maintenance Tool	SMS
33	FD0300	SMS	IO-07	MOD		Floppy Disk Controller;Controls Up To 4 Drives	SMS
34	FD0800	SMS	IO-07	MOD		Floppy Disk Controller Compatible With PDP-8E/PDP-8A	SMS
35	FD1100	SMS	IO-07	MOD		Floppy Disk Controller Compatible With PDP-11	SMS
36	SSM-85/1	SSM-85	COMP	MOD		8 Bit Computer On a Card;Uses 8085 CPU,1280 Byte RAM,LED/Monitor	SSC
37	SSM-85/2	SSM-85	COMP	MOD		8 Bit Computer on a Card;Uses 8085 CPU,256 Byte RAM,RS232 IO Port	SSC
38	SSM-7345	STD-BUS	IO-09	MOD		TV CRT Controller; Programmable Format; Inv. Video;Light Pen Input	SSC
39	SSM-7322	STD-BUS	IO-30	MOD		22 Parallel I/O Pins; Serial Interface (8 Bit); 14 Bit Counter/Timer	SSC
40	CB1	SSM-S100	CPU	MOD		CPU Board:Uses 8080A 2MHz,EPROM 2708,RAM 2112,8 Bit Port	SSM
41	CB2	SSM-S100	CPU	MOD		Z80 Based CPU Board:4k/8k ROM,Extended Address,Vector Jump,S100 Bus	SSM
42	AP1	SSM-S100	IO-02	MOD		Interrupt,Real Time Clock,Mem Management Kit or Assembled,Uses 8080	SSM
43	OB1	SSM-S100	IO-02	MOD		Vector Jump and Prototyping Board,Range 65536 Bytes	SSM
44	VB1B	SSM-S100	IO-09	MOD		S-100 Bus Video Board:64/32 Char Per Line By 16 Lines,1024 Byte Mem	SSM
45	VB2	SSM-S100	IO-09	MOD		S-100 Bus Video Board:64 Char Per Line By 16 Lines,Par Keyboard Input	SSM
46	IO4	SSM-S100	IO-20	MOD		S 100 Bus Computer Syst;Compatible I/O Board;2 Ser,2 Par Ports	SSM
47	IO2	SSM-S100	IO-30	MOD		8 Bit Parallel I/O Board:256 Possible Port Addresses;S100 Bus	SSM
48	MB9	SSM-S100	IO-55	MOD		S 100 Bus Compatible 4k Static PROM/RAM Board;Uses 2112,74S287	SSM
49	PB1	SSM-S100	IO-92	MOD		2708/2716 Programmer and 4k/8k EPROM Board	SSM
50	SB1	SSM-S100	IO-92	MOD		Music Synthesizer Board:15Hz to 25kHz;Mem Map 256 Bytes	SSM
51	T1	SSM-S100	IO-92	MOD		Terminator for S100 Bus,275 ohm Impedance at 2.75 Volts	SSM
52	MB4	SSM-S100	RAM	MOD		4k Static RAM Board:Uses 2102AL RAM,S100 Bus Compatible	SSM
53	MB6B	SSM-S100	RAM	MOD		8k/Dual 4k Static RAM Board:Uses 2102AL RAM;2/4MHz	SSM
54	MB7	SSM-S100	RAM	MOD		S100 Compatible Low Power 16k Static RAM Board,Uses uPD410	SSM
55	MB10	SSM-S100	RAM	MOD		24k Static RAM Kit or Assembled,Uses 2114L RAMs 250ns/450ns;S100 Bus	SSM
56	MB3	SSM-S100	ROM	MOD		2k/4k EPROM Board:Uses 1702A EPROM,S100 Bus Compatible	SSM
57	MB8A	SSM-S100	ROM	MOD		1k/16k EPROM Board:Uses 2708 EPROM,S100 Bus Compatible	SSM
58	SCM5101-1	SCM5101	RAM	Chip	MXX	256x4 Static CMOS RAM;450nS Access Time,0.2uA Standby Curr,Data Ret 2.0V	SSS
59	SCM5101-3	SCM5101	RAM	Chip	MXX	256x4 Static CMOS RAM;650nS Access Time,1.0uA Standby Curr,Data Ret 2.0V	SSS
60	SCM5101-8	SCM5101	RAM	Chip	MXX	256x4 Static CMOS RAM;800nS Access Time,10.0uA Standby Curr,Data Ret 4.5V	SSS
61▼	SCM5101-1A	SCM5101	RAM	CHIP	MXX	256x4 Static CMOS RAM;650ns Acess Time;.20uA Standby Curr,Data Ret 2.0V	SSS
62	SCM5102-1	SCM5102	RAM	Chip	MXX	1024x1 Stat CMOS RAM;450nS Access Time,0.2uA Standby Curr,Data Ret 2.0V	SSS
63	SCM5102-3	SCM5102	RAM	Chip	MXX	1024x1 Stat CMOS RAM;650nS Access Time,1.0uA Standby Curr,Data Ret 2.0V	SSS
64	SCM5102-8	SCM5102	RAM	Chip	MXX	1024x1 Stat CMOS RAM;800nS Access Time,10.0uA Standby Curr,Data Ret 4.5V	SSS
65▼	SCM5102-1A	SCM5102	RAM	CHIP	MXX	1024x1 Stat CMOS RAM;650ns Acess Time;.20uA Standby Curr,Data Ret 2.0V	SSS
66	MP68	SWTPC6800	COMP	MOD		Complete Computer System Kit;Includes MPA,B,C,D,F,M And P	STP
67	SWTPC6800	SWTPC6800	COMP	UNIT		8 Bit System Uses MOTA 6800 CPU,5.5x9in PCB	STP
68	MPA	SWTPC6800	CPU	MOD		Microprocessor/System Board Kit,Uses MOTA MC6800 MPU,MCM6830 ROM,MCM6810	STP
69	MPC	SWTPC6800	IO-20	MOD		Control Interface For Serial Terminal,5.25 x 3.50 In Board	STP
70	MPS	SWTPC6800	IO-20	MOD		Serial Interface Using MC6820 ACIA,5.25 x 3.50 In Board	STP
71	MPL	SWTPC6800	IO-30	MOD		Parallel Interface,Using MC6820 PIA,5.25 x 3.50 In Board	STP
72	MPB	SWTPC6800	IO-33	MOD		Mother Board With Interface Address Decoder,9 x 14 In Board	STP
73	MPM	SWTPC6800	IO-55	MOD		Memory Board;2048 Word On Board Capicity 4096 With Expansion Kit	STP
74	CT1024	SWTPC6800	PE-20	MOD		Terminal System Kit	STP
75	MPMX	SWTPC6800	RAM	MOD		Memory Expansion Kit;16 2102 Static RAM,5V Voltage Regulator	STP
76	SYP6504	SY6500	CPU	Chip	MNG	8 Bit uP Addressable Mem 8k;onSYK uP Addressable Mem 8k;onase	SY
77	SYC6502	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;on Chip Clock,IRQ,NMI,RDY,1MHz;Ceramic Case	SYK
78	SYC6502A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64K;on Chip Clock;IRQ,NMI,RDY,2MHz;Ceramic Case	SYK
79	SYC6502B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;on Chip Clock;IRQ,NMI,RDY,3MHz;Ceramic Case	SYK
80	SYC6503	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock,IRQ,NMI,1MHz;Ceramic Case	SYK
81	SYC6503A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,NMI,2MHz;Ceramic Case	SYK
82	SYC6503B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,NMI,3MHz;Ceramic Case	SYK
83	SYC6504	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock,IRQ,1MHz;Ceramic Case	SYK
84	SYC6504A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock;IRQ,2MHz;Ceramic Case	SYK
85	SYC6504B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock;IRQ,3MHz;Ceramic Case	SYK
86	SYC6505	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock,IRQ,RDY,1MHz;Ceramic Case	SYK
87	SYC6505A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,RDY,2MHz;Ceramic Case	SYK
88	SYC6505B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,RDY,3MHz;Ceramic Case	SYK
89	SYC6506	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock,IRQ,1MHz;Ceramic Case	SYK
90	SYC6506A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,2MHz;Ceramic Case	SYK
91	SYC6506B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,3MHz;Ceramic Case	SYK
92	SYC6507	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock,RDY,1MHz;Ceramic Case	SYK
93	SYC6507A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock;RDY,2MHz;Ceramic Case	SYK
94	SYC6507B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock;RDY,3MHz;Ceramic Case	SYK
95	SYC6512	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;Xternal Clock,IRQ,NMI,RDY,1MHz;Ceramic Case	SYK
96	SYC6512A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;Xternal Clock;IRQ,NMI,RDY,2MHz;Ceramic Case	SYK
97	SYC6512B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;Xternal Clock;IRQ,NMI,RDY,3MHz;Ceramic Case	SYK
98	SYC6513	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock,IRQ,NMI,1MHz;Ceramic Case	SYK
99	SYC6513A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock;IRQ,2MHz;Ceramic Case	SYK
100	SYC6513B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock;IRQ,NMI,3MHz;Ceramic Case	SYK
101	SYC6514	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;Xternal Clock,IRQ,1MHz;Ceramic Case	SYK
102	SYC6514A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;Xternal Clock;IRQ,2MHz;Ceramic Case	SYK
103	SYC6514B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;Xternal Clock;IRQ,3MHz;Ceramic Case	SYK
104	SYC6515	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock,IRQ,RDY,1MHz;Ceramic Case	SYK
105	SYC6515A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock;IRQ,2MHz;Ceramic Case	SYK
106	SYC6515B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock;IRQ,NMI,RDY,3MHz;Ceramic Case	SYK
107	SYP6502	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;on Chip Clock;IRQ,NMI,RDY,1MHz;Plastic Case	SYK
108	SYP6502A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;on Chip Clock;IRQ,NMI,RDY,2MHz;Plastic Case	SYK
109	SYP6502B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;on Chip Clock;IRQ,NMI,RDY,3MHz;Plastic Case	SYK
110	SYP6503	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,NMI,1MHz;Plastic Case	SYK

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	SYP6503A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,NMI,2MHz;Plastic Case	SYK
2	SYP6503B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,NMI,3MHz;Plastic Case	SYK
3	SYP6504A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock;IRQ,2MHz;Plastic Case	SYK
4	SYP6504B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock;IRQ,3MHz;Plastic Case	SYK
5	SYP6505	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,RDY,1MHz;Plastic Case	SYK
6	SYP6505A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,RDY,2MHz;Plastic Case	SYK
7	SYP6505B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,RDY,3MHz;Plastic Case	SYK
8	SYP6506	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,1MHz;Plastic Case	SYK
9	SYP6506A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,2MHz;Plastic Case	SYK
10	SYP6506B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;on Chip Clock;IRQ,3MHz;Plastic Case	SYK
11	SYP6507	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock ;RDY,1MHz;Plastic Casew	SYK
12	SYP6507A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock;RDY,2MHz;Plastic Case	SYK
13	SYP6507B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;on Chip Clock;RDY,3MHz;Plastic Case	SYK
14	SYP6512	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;Xternal Clock;IRQ,NMI,RDY,1MHz;Plastic Case	SYK
15	SYP6512A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;Xternal Clock;IRQ,NMI,RDY,2MHz;Plastic Case	SYK
16	SYP6512B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 64k;Xternal Clock;IRQ,RDY,3MHz;Plastic Case	SYK
17	SYP6513	SY6500	CPU	Chip	MNG	8 Bit uP;Addrressable Mem 4k;Xternal Clock;IRQ,NMI,1MHz;Plastic Case	SYK
18	SYP6513A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock;IRQ,NMI,2MHz;Plastic Case	SYK
19	SYP6513B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock;IRQ,RDY,3MHz;Plastic Case	SYK
20	SYP6514	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;Xternal Clock;IRQ,1MHz;Plastic Case	SYK
21	SYP6514A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 8k;Xternal Clock;IRQ,2MHz;Plastic Case	SYK
22	SYP6515	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock;IRQ,RDY,1MHz;Plastic Case	SYK
23	SYP6515A	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock;IRQ,RDY,2MHz;Plastic Case	SYK
24	SYP6515B	SY6500	CPU	Chip	MNG	8 Bit uP;Addressable Mem 4k;Xternal Clock;IRQ,RDY,3MHz;Plastic Case	SYK
25	MBC010-65	SY6500	CPU	MOD		8 Bit CPU on a Card,Exorcisor Bus;1k RAM,4ROM Sockets;ACIA	SYK
26	MBC020-65	SY6500	CPU	MOD		Computer Board,Exorcisor Bus;1k RAM,4 ROM Sockets;ACIA;Video Interface	SYK
27	SM100	SY6500	DEV	MOD		uCOMP;1kB Static RAM Up to 4kB On-Board;51 I/O Lines Expandable to 71	SYK
28	SY6500/1E	SY6500	DEV	MOD		Emulator:54 Pin Emulator for Development	SYK
29	SYM1	SY6500	DEV	MOD		uCOMP;1kB Static RAM Up to 4kB On-Board;50 I/O Lines;W/Keybd,LED Display	SYK
30	SY6545	SY6500	IO-09	Chip	MNG	CRT Controller,Comp W/SY6500,MCS6500,MC6800 Families,Tcy 500ns Min	SYK
31	SY6545A	SY6500	IO-09	Chip	MNG	CRT Controller,Comp W/SY6500,MCS6500,MC6800 Families,Tcy 1.0us Min	SYK
32	SYC6551	SY6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,15 Progm Baud Rates,Tcy 1.0us Min,Cer	SYK
33	SYC6551A	SY6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,15 Progm Baud Rates,Tcy 500ns Min,Cer	SYK
34	SYP6551	SY6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,15 Progm Baud Rates,Tcy 1.0us Min,Plas	SYK
35	SYP6551A	SY6500	IO-20	Chip	MNG	Asynch Comm Interface Adapter,15 Progm Baud Rates,Tcy 500ns Min,Plas	SYK
36	SYC68B21	SY6500	IO-30	Chip		PIA;2 8Bit Programmable I/O Ports;2 MHz;Ceramic Pkg	SYK
37	SYC6520	SY6500	IO-30	Chip	MNX	Peripheral Interface Adapter;Direct Replacement For MC6820;40 Pin Ceramic	SYK
38	SYC6520A	SY6500	IO-30	Chip	MNX	Peripheral Interface Adapter;Direct Replacement For MC6820;40 Pin Ceramic	SYK
39	SYC6521	SY6500	IO-30	Chip		PIA;2 8Bit Programmable I/O Ports;1 MHz;Ceramic Pkg	SYK
40	SYC6521A	SY6500	IO-30	Chip		PIA;2 8Bit Programmable I/O Ports;2 MHz;Ceramic Pkg	SYK
41	SYC6821	SY6500	IO-30	Chip		PIA;2 8Bit Programmable I/O Ports;1 MHz;Ceramic Pkg	SYK
42	SYP68B21	SY6500	IO-30	Chip		PIA;2 8Bit Programmable I/O Ports;2 MHz;Plastic Pkg	SYK
43	SYP6520	SY6500	IO-30	Chip	MNX	Peripheral Interface Adapter;Direct Replacement For MC6820;40 Pin Plastic	SYK
44	SYP6520A	SY6500	IO-30	Chip	MNX	Peripheral Interface Adapter;Direct Replacement For MC6820;40 Pin Plastic	SYK
45	SYP6521	SY6500	IO-30	Chip		PIA;2 8Bit Programmable I/O Ports;1 MHz;Plastic Pkg	SYK
46	SYP6521A	SY6500	IO-30	Chip		PIA;2 8Bit Programmable I/O Ports;2 MHz;Plastic Pkg	SYK
47	SYP6821	SY6500	IO-30	Chip		PIA;2 8Bit Programmable I/O Ports;1 MHz;Plastic Pkg	SYK
48	SYC6522	SY6500	IO-33	Chip		2 16Bit Programmable Timer/Counters;Serial Data Port;Speed 1MHz;Ceramic	SYK
49	SYC6522A	SY6500	IO-33	Chip		2 16Bit Programmable Timer/Counters;Serial Data Port;Speed 2MHz;Ceramic	SYK
50	SYP6522	SY6500	IO-33	Chip		2 16Bit Programmable Timer/Counters;Serial Data Part;Speed 1MHz;Plastic	SYK
51	SYP6522A	SY6500	IO-33	Chip		2 16Bit Programmable Timer/Counters;Serial Data Port;Speed 2MHz;Plastics	SYK
52	SY6530	SY6500	IO-57	Chip	MNG	Memory,I/O,Timer Array;Single Chip;RAM,ROM,I/O,Timer;40 Pin Pkg	SYK
53	SY6531	SY6500	IO-57	Chip		RAM,ROM,I/O,Counter/Timer:128x8 RAM,2048x8 ROM,16B Progm C/T,Tcy 1.0us	SYK
54	SY6531A	SY6500	IO-57	Chip		RAM,ROM,I/O,Counter/Timer:128x8 RAM,2048x8 ROM,16B Progm C/T,Tcy 500ns	SYK
55	SY6532	SY6500	IO-57	Chip	MNG	Memory,I/O,Timer Array;Single Chip;128 x 8 RAM,Two 8 Bit Ports	SYK
56	KTM2	SY6500	PE-61	MOD		54 Key Keyboard;Work W/Any RS232 Bus,Up to 9600 Baud	SYK
57	KTM2/80	SY6500	PE-61	MOD		80 Column Version of KTM2	SYK
58	SRM1	SY6500	RAM	ChS		Static RAM Memory Kit;1kB of RAM;Two Syk 2114L Static RAMS	SYK
59	SRM3	SY6500	RAM	ChS		Static RAM Memory Kit;3kB of RAM	SYK
60	MBC016-3	SY6500	RAM	MOD		16kx8 Static RAM Board;Pwr Consumption 2.5A typ;Speed 300nS;Exorcisor Bus	SYK
61	MBC016L	SY6500	RAM	MOD		16kx8 Static RAM Board;Pwr Consumption 1.75Atyp;Speed 500nS;Exorcisor Bus	SYK
62	MBC016L-3	SY6500	RAM	MOD		16kx8 Static RAM Board;Pwr Consumption 1.75Atyp;Speed 300nS;Exorcisor Bus	SYK
63	SYC6500/1	SY6500/1	CPU	Chip	MNG	8 Bit uProcessor;RAM/ROM 64/2k Byte;32 I/O Lines;40 Pin Ceramic Pkg	SYK
64	SYP6500/1	SY6500/1	CPU	Chip	MNG	8 Bit uProcessor;RAM/ROM 64/2k Byte;32 I/O Lines;40 Pin Plastic Pkg	SYK
65♦	SyZ8-01MCCCS	Z8	uCT	Chip		8 Bit uComp:128 Bytes ROM;32 I/O Lines;2 Prog 8 Bit Cntr/Timer	SYK
66♦	SyZ8-01MCCPS	Z8	uCT	Chip		8 Bit uComp:128 Bytes ROM;32 I/O Lines;2 Prog 8 Bit Cntr/Timer	SYK
67♦	SyZ8-02MPDQS	Z8	uCT	Chip		8 Bit uComp:128 Bytes RAM;Development Device	SYK
68▼	SVC6545	6500/6800	IO-09	Chip		CRT Controller:1MHz Clk Rate;A/N and Limited Graphics;Prog Cursor;Cer Pkg	SYK
69▼	SVC6545A	6500/6800	IO-09	Chip		CRT Controller:2MHz Clk Rate;A/N and Limited Graphics;Prog Cursor;Cer Pkg	SYK
70▼	SVP6545	6500/6800	IO-09	Chip		CRT Controller:1MHz Clk Rate;A/N and Limited Graphics;Prog Cursor;Pls Pkg	SYK
71▼	SVP6545A	6500/6800	IO-09	Chip		CRT Controller:2MHz Clk Rate;A/N and Limited Graphics;Prog Cursor;Pls Pkg	SYK
72	MBC010-68	6800	CPU	MOD		8 Bit CPU on a Card,Exorcisor Bus;1k RAM,4 ROM Sockets;ACIA	SYK
73	MBC020-68	6800	CPU	MOD		Computer Board,Exorcisor Bus;1k RAM,4 ROM Sockets;ACIA;Video Interface	SYK
74	TOKOM80-01	TOKOM80	COMP	UNIT		8 Bit System Uses Intel 8080 CPU;4.0k Bytes RAM/ROM	TAI
75	TOKOM80-02	TOKOM80	COMP	UNIT		8 Bit System Uses Intel 8080 CPU; 4.0k Bytes RAM/ROM	TAI
76	TOKOM80-03	TOKOM80	COMP	UNIT		8 Bit System Uses Intel 8080 CPU; 8.0k Bytes RAM/ROM	TAI
77	TOKOM80-04	TOKOM80	COMP	UNIT		8 Bit System Uses Intel 8080 CPU; 8.0k Bytes RAM/ROM	TAI
78	TOKOM80-05	TOKOM80	COMP	UNIT		8 Bit System Uses Intel 8080 CPU; 8.0k Bytes RAM/ROM	TAI
79	CPU-TAI	TOKOM80	CPU	MOD	MNX	CPU W/I/O Control Mod;Uses Intel 8080	TAI
80	DMA-TAI	TOKOM80	IO-03	MOD		Optional;Direct Memory Access DMA Module	TAI
81	TPC-TAI	TOKOM80	IO-04	MOD		Optional;TYPUTER Interface Module	TAI
82	TYC-HRC-TAI	TOKOM80	IO-04	MOD		TTY And High Speed Paper Tape Reader Interface Mod	TAI
83	TYC-TAI	TOKOM80	IO-04	MOD		TTY Interface Module	TAI
84	CTC-TAI	TOKOM80	IO-05	MOD		Optional;Cassette Tape Control Module	TAI
85	FDC-TAI	TOKOM80	IO-07	MOD		Optional;Floppy Disk Control Module	TAI
86	HPC-TAI	TOKOM80	IO-08	MOD		High Speed Printer Interface Mod	TAI
87	WMX-TAI	TOKOM80	IO-55	MOD		4k Byte ROM/RAM Mod	TAI
88	DCU-TAI	TOKOM80	PE-61	UNIT		Display And Control Panel	TAI
89	IMX-TAI	TOKOM80	RAM	MOD		IC Static RAM Memory Mod	TAI
90	8002	8002	DEV	UNIT		Interactive Software Development Microprocessor Lab For 8080,6800,Z-80	TEKT
91	DISCUSI	MCS80	PE-01	UNIT		Disc Mem, System:250000 Bytes per 8 inch Floppy Diskette,S-100 Compatible	THT
92	SBP0400ACJ	SBP0400	CPU	Chip	BIX	4 Bit-Slice Processor Element; 0-70°C	TII
93	SBP0400ACN	SBP0400	CPU	Chip	BIX	4 Bit-Slice Processor Element; 0-70°C	TII
94	SBP0400AMJ	SBP0400	CPU	Chip	BIX	4 Bit-Slice Processor Element; -55-125°C	TII
95	SBP0400C	SBP0400	CPU	Chip	BIX	4 Bit Controller/Processor Building Block;Freq 1.0MHz;0-70°C	TII
96	SBP0400M	SBP0400	CPU	Chip	BIX	4 Bit Controller/Processor Building Block;Freq 1.0MHz;-55-125°C	TII
97	SBP0401ACJ	SBP0400	CPU	Chip	BIX	4 Bit Slice Processor Element With Asynch u Instruction Decode 0-70°C	TII
98	SBP0401ACN	SBP0400	CPU	Chip	BIX	4 Bit Slice Processor Element With Asynch uInstruction Decode 0-70°C	TII
99	SBP0401AMJ	SBP0400	CPU	Chip	BIX	4 Bit Slice Processor Element With Asynch uInstruction Decode -55-125°C	TII
100	SN54LS481J	S481	CPU	Chip	BTD	4 Bit Slice Processor,Microprogrammable;48 Pin Cer DIP	TII
101	SN54S481	S481	CPU	Chip	BTD	4 Bit Slice Processor, Microprogrammable; Clock Cycle Time 90ns/345ma	TII
102	SN74LS481J	S481	CPU	Chip	BTD	4 Bit Slice Processor,Microprogrammable;48 Pin Cer DIP	TII
103	SN74LS481N	S481	CPU	Chip	BTD	4 Bit Slice Processor,Microporgrammable;48 Pin Plastic DIP	TII
104	SN74S481J	S481	CPU	Chip	BTD	4 Bit Slice Processor,Microprogrammable;48 Pin Cer DIP	TII
105	SN74S481N	S481	CPU	Chip	BTD	4 Bit Slice Processor,Microprogrammable;48 Pin Plastic DIP	TII
106	SN54S482J	S481	IO-01	Chip	BTD	4-Bit Slice Expandable Control Element	TII
107	SN74S482J	S481	IO-01	Chip	BTD	4-Bit Slice Expandable Control Element	TII
108	SN74S482N	S481	IO-01	Chip	BTD	4-Bit Slice Expandable Control Element	TII
109	SN54S226J	S481	IO-21	Chip	BTD	4-Bit Parallel Latched Bus Transceiver;Tri State Output	TII
110	SN54S240J	S481	IO-21	Chip	BTD	Octal Buffers/Line Drivers/Receivers	TII

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	SN54S241J	S481	IO-21	Chip	BTD	Octal Buffers/Line Drivers/Receivers	TII
2	SN74S226J	S481	IO-21	Chip	BTD	4-Bit Parallel Latched Bus Transceiver;Tri State Output	TII
3	SN74S226N	S481	IO-21	Chip	BTD	4-Bit Parallel Latched Bus Transceiver;Tri State Output	TII
4	SN74S240J	S481	IO-21	Chip	BTD	Octal Buffers/Line Drivers/Receivers	TII
5	SN74S240N	S481	IO-21	Chip	BTD	Octal Buffers/Line Drivers/Receivers	TII
6	SN74S241J	S481	IO-21	Chip	BTD	Octal Buffers/Line Drivers/Receivers	TII
7	SN54S373J	S481	IO-56	Chip	BTD	Octal D-Type Transparent Latches And Edge-Trig. Flip Flops	TII
8	SN54S412J	S481	IO-56	Chip	BTD	Multimode Buffered Latches	TII
9	SN74S373J	S481	IO-56	Chip	BTD	Octal D-Type Transparent Latches And Edge-Trig. Flip Flops	TII
10	SN74S373N	S481	IO-56	Chip	BTD	Octal D-Type Transparent Latches And Edge-Trig. Flip Flops	TII
11	SN74S412J	S481	IO-56	Chip	BTD	Multimode Buffered Latches	TII
12	SN74S412N	S481	IO-56	Chip	BTD	Multimode Buffered Latches	TII
13	TMS1000	TMS1000	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer W/ROM,RAM And ALU	TII
14	TMS1070	TMS1000	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer W/ROM,RAM And ALU	TII
15	TMS1100	TMS1000	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer W/ROM,RAM And ALU	TII
16	TMS1200	TMS1000	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer W/ROM,RAM And ALU	TII
17	TMS1270	TMS1000	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer W/ROM,RAM And ALU	TII
18	TMS1300	TMS1000	uCT	Chip	MPX	Single Chip 4 Bit Microcomputer W/ROM,RAM And ALU	TII
19▼	TMS1000C	TMS1000	uCT	CHIP	MNX	4-Bit uComputer w/ROM/RAM and ALU	TII
20▼	TMS1097JLL	TMS1000	uCT	CHIP	MPX	Same As TMS1400/1600 w/External Instruction Memory	TII
21▼	TMS1200C	TMS1000	uCT	CHIP	MNX	4-Bit uComputer w/ROM/RAM and ALU	TII
22▼	TMS1400NLL	TMS1000	uCT	CHIP	MPX	4-Bit uComputer;4096-word Instruction ROM;128-word RAM and 4-Bit ALU	TII
23▼	TMS1470NLL	TMS1000	uCT	CHIP	MPX	4-Bit uComputer;4096-word Instruction ROM;128-word RAM and 4-Bit ALU	TII
24▼	TMS1600NLL	TMS1000	uCT	CHIP	MPX	4-Bit uComputer;4096-word Instruction ROM;128-word RAM and 4-Bit ALU	TII
25▼	TMS1670NLL	TMS1000	uCT	CHIP	MPX	4-Bit uComputer;4096-word Instruction ROM;128-word RAM and 4-Bit ALU	TII
26	TMS1099JL/SE1	TMS1000	DEV	UNIT	MPX	Microcomputer System Evaluator	TII
27▼	TMS9918C	TMS1000	IO-92	CHIP	MNG	Video Display Processor;Interface to Color TV	TII
28▼	TMS9918P	TMS1000	IO-92	CHIP	MNG	Video Display Processor;Interface to Color TV	TII
29	TMS5501	TMS8080	IO-33	Chip	MNG	Multifunction Input/Output Controller	TII
30	TMS2564JL	TMS8080	PROM	Chip	MNX	8192x8 UV Erasable,Electrically Programmable ROM;TTL Comp	TII
31	TMS8080AJL	TMS8080A	CPU	Chip	MNG	Single Chip 8 Bit Parallel CPU,Microprocessor,Ceramic Pkg	TII
32	TMS8080ANL	TMS8080A	CPU	Chip	MNG	Single Chip 8 Bit Parallel CPU,Microprocessor,Plastic Pkg	TII
33	SN74S428N	TMS8080A	IO-02	Chip	BTD	Controller And Bus Driver For 8080A Systems	TII
34	SN74S438N	TMS8080A	IO-02	Chip	BTD	Controller And Bus Driver For 8080A Systems W/Advanced IO Response	TII
35	SN74LS424J	TMS8080A	IO-32	Chip		2 Phase Clock Gen/Driver For TMS8080A Microprocessor	TII
36	SN74LS424N	TMS8080A	IO-32	Chip		2 Phase Clock Gen/Drivers For TMS 8080A Microprocessor	TII
37	TMS9940M	TMS9900	uCT	Chip	MNG	Mask ROM Device Single Chip 128 Bytes Oscillator Freq 5MHz	TII
38	TMS9911-40NL	TMS9900	IO-03	Chip	MNG	Direct Memory Access Controller for 2 Indep Devices Plastic Pkg	TII
39#	TM990/303	TM990	IO-07	MOD		12V/200mA,-12V/200mA, 5V/3A;IBM 3740,TI FS 990 Compatible	TII
40▼	TM990/308	TM990	IO-20	MOD		Industrial Communication Module;Bus Compatible	TII
41	TM990/306	TM990	IO-22	MOD		Self-Contained Vocab;I/O TTL Compat;On Bd Amp Drives 80hm Spkr to 2.5W	TII
42	TM990/307	TM990	IO-23	MOD		Communicate W/4 Async or Sync Modem or Terminal Devices w/RS232 Interface	TII
43▼	TM990/306-2	TM990	IO-92	MOD		Speech Module;Bus Compatible Fixed Vocabulary	TII
44▼	TM990/1481	TM990/100	CPU	MOD		General Purpose CPU;Processor/Controller Bd	TII
45	TMS21L47-7NL	74TTL	RAM	Chip		Static RAM 18 Pin R/W Cycle Time 70ns Plastic Pkg	TII
46	TMS2147-5JDL	74TTL	RAM	Chip		Static RAM 18 Pins R/W Cycle Time 55ns Sidebraze	TII
47	TMS2147-5NL	74TTL	RAM	Chip		Static RAM 18 Pins R/W Cycle Time 55ns Plastic Pkg	TII
48	TMS2147-7JDL	74TTL	RAM	Chip		Static RAM 18 Pins R/W Cycle Time 70ns Sidebraze	TII
49	TMS2147-7JL	74TTL	RAM	Chip		Static RAM 18 Pins R/W Cycle Time 70ns Ceramic Pkg	TII
50	TMS2147-7NL	74TTL	RAM	Chip		Static RAM 18 Pins R/W Cycle Time 70ns Plastic Pkg	TII
51	TMS2147-9JDL	74TTL	RAM	Chip		Static RAM 18 Pin R/W Cycle Time 90ns Sidebraze	TII
52	TMS4044-15JDL	74TTL	RAM	Chip	MNG	4096 Bit Static RAM; Access Time 150ns; Sidebraised	TII
53	TMS4164-15JDL	74TTL	RAM	Chip	MNX	65,536 Bit Dynamic RAM	TII
54	TMS4244JL	74TTL	RAM	Chip	MNG	4096X1 Static RAM Cerdip	TII
55	TMS4244NL	74TTL	RAM	Chip	MNG	4096X1 Static RAM Plastic	TII
56	TMS4245JL	74TTL	RAM	Chip	MNG	1024X4-Bit Static RAM Cerdip	TII
57	TMS4245NL	74TTL	RAM	Chip	MNG	1024X4-Bit Static RAM Plastic	TII
58	TMS21L47-7JL	74TTL	RAM C	Chip		Static RAM 18 Pin R/W Cycle Time 70ns Ceramic Pkg	TII
59	TMS2508-25JL	74TTL	ROM	Chip		Static ROM Access Time 250ns Ceramic Pkg	TII
60	TMS2508-30JL	74TTL	ROM	Chip		Static ROM 5V Only Access Time 300ns Ceramic Pkg	TII
61	TMS2564JDL	74TTL	ROM	Chip		Static ROM 5V Only Access Time 450ns Sidebraze	TII
62▼	TBP18SA030J	990	PROM	CHIP	BTD	32x8 Electrically-Programmable ROM	TII
63▼	TBP24S86J	990	PROM	CHIP	BTD	1024x8 Electrically-Programmable ROM;TRI State Output	TII
64▼	TBP24S86M-J	990	PROM	CHIP	BTD	1024x8 Electrically-Programmable ROM;Tri State Output	TII
65▼	TBP24S86N	990	PROM	CHIP	BTD	1024x8 Electrically-Programmable ROM;TRI State Output	TII
66▼	TBP24SA41J	990	PROM	CHIP	BTD	1024x4 Electrically-Programmable ROM;Open Collector Output	TII
67▼	TBP24SA41M-J	990	PROM	CHIP	BTD	1024x4 Electrically-Programmable ROM;Open Collection Output	TII
68▼	TBP24SA41N	990	PROM	CHIP	BTD	1024x4 Electrically-Programmable ROM;Open Collector Output	TII
69▼	TBP28S41M-J	990	PROM	CHIP	BTD	1024x4 Electrically-Programmable ROM; Tri State Output	TII
70▼	TBP28SA86J	990	PROM	CHIP	BTD	1024x8 Electrically-Programmable ROM;Open Collector Output	TII
71▼	TBP28SA86M-J	990	PROM	CHIP	BTD	1024x8 Electrically-Programmable ROM;Open Collector Output	TII
72▼	TBP28SA86N	990	PROM	CHIP	BTD	1024x8 Electrically-Programmable ROM;Open Collector Output	TII
73	SN54S2708J	990,TMS8080	PROM	Chip	BTD	1024 x 8 Electrically Programmable ROM;Tri State Output;-55 to 125°C	TII
74	SN54S3708J	990,TMS8080	PROM	Chip	BTD	1024 x 8 Electrically Programmable ROM;Open Coll Output;-55 to 125°C	TII
75	SBP8316CJ	990,TMS8080	ROM	Chip	BIX	2048 x 8 IIL Mask Programmable ROM;5V Supply,0 to 70°C	TII
76	SBP8316CN	990,TMS8080	ROM	Chip	BIX	2048 x 8 IIL Mask Programmable ROM;5V Supply,0 to 70°C	TII
77	SBP8316MJ	990,TMS8080	ROM	Chip	BIX	2048 x 8 IIL Mask Programmable ROM;5V Supply,-55 to 125°C	TII
78	SBP9818CJ	990,TMS8080	ROM	Chip	BIX	2048 x 8 IIL Mask Programmable ROM;Selectable Icc;0 to 70°C	TII
79	SBP9818CN	990,TMS8080	ROM	Chip	BIX	2048 x 8 IIL Mask Programmable ROM;Selectable Icc;0 to 70°C	TII
80	SBP9818MJ	990,TMS8080	ROM	Chip	BIX	2048 x 8 IIL Mask Programmable ROM;Selectable Icc;-55 to 125°C	TII
81	TMS9940	9900	uCT	Chip	MNG	16 Bit Single Chip Microcomputer;16 User-Defined Program Control Flags	TII
82	TMS9940E	9900	uCT	Chip	MNG	128 Bytes of RAM Single Chip EPROM Device Oscillator Freq 5MHz	TII
83	TM990/100M-1	9900	COMP	MOD	MNG	16 Bit Microcomputer Mod;TMS9900 CPU;256 x 16 RAM;1kx16 EPROM W/TIBUG Mon	TII
84	TM990/100M-2	9900	COMP	MOD	MNG	16 Bit Microcomputer Mod;TMS9900 CPU;256 x 16 RAM;1kx16 EPROM Unprogrm	TII
85	TM990/100M-3	9900	COMP	MOD	MNG	16 Bit Microcomputer Mod;TMS9900 CPU;512 x 16 RAM;4kx16 EPROM Unprogrm	TII
86	TM990/101M-1	9900	COMP	MOD	MNG	16 Bit Microcomputer Mod;TMS9900 CPU;1kx16 RAM;1kx16 EPROM W/TIBUG Mon	TII
87	TM990/101M-2	9900	COMP	MOD	MNG	16 Bit Microcomputer Mod;TMS9900 CPU;1kx16 RAM;1kx16 Blank EPROM	TII
88	TM990/101M-3	9900	COMP	MOD	MNG	16 Bit Microcomputer Mod;TMS9900 CPU;2kx16 RAM;4kx16 Blank EPROM	TII
89	TM990/180M-1	9900	COMP	MOD	MNG	16 Bit Microcomp Mod;TMS9980 CPU;512x8 RAM;2kx8 EPROM W/TIBUG Mon	TII
90	TM990/189	9900	COMP	MOD	MNG	16 Bit Educational Module for teaching Microcomputer Fundamentals	TII
91	990/4	9900	COMP	UNIT		16 Bit System With External Stack And 7 Interrupts	TII
92	SBP9900ACJ	9900	CPU	Chip	BIX	16 Bit Microprocessor;Software Compat W/990 Family;0 to 70°C	TII
93	SBP9900AEJ	9900	CPU	Chip	BIX	16 Bit Microprocessor;Software Compat W/990 Family;-40 to 85°C	TII
94	SBP9900AMJ	9900	CPU	Chip	BIX	16 Bit Microprocessor;Software Compat W/990 Family;-55 to 125°C	TII
95	SBP9900ANJ	9900	CPU	Chip	BIX	16 Bit Microprocessor;Software Compat W/990 Fam;-55 to 125°C,Hi Rel	TII
96	TMS9900	9900	CPU	Chip	MNG	Single Chip 16 Bit CPU,Microprocessor	TII
97	TMS9900-40	9900	CPU	Chip	MNG	Single Chip 16-Bit CPU Microprocessor	TII
98	TMS9916	9900	CPU	Chip	MNG	Magnetic Bubble Memory Controller	TII
99	TMS9980A	9900	CPU	Chip		16-Bit CPU W/8-Bit Data Bus/9900 IS/40 Pin DIL	TII
100	TMS9981	9900	CPU	Chip		16-Bit CPU W/8-Bit Data Bus/9900 IS/Optional on-Chip Xtal OSC/40 Pin DIL	TII
101	TM990/302	9900	DEV	MOD		DEV Board for Developing Assembly Language Software for 990/9900 SYS	TII
102	SBP9964	9900	IO-01	Chip	BIX	Timing Controller for the SBP9900A;20-Pin Dil Pkg	TII
103	SBP9961CJ	9900	IO-02	Chip	BIX	Interrupt-Controller/Timer;40-Pin Dil Pkg;0° to 70°C	TII
104	SBP9961EJ	9900	IO-02	Chip	BIX	Interrupt-Controller/Timer;40-Pin Dil Pkg;-40° to 85°C	TII
105	SBP9961MJ	9900	IO-02	Chip	BIX	Interrupt-Controller/Timer;40-Pin Dil Pkg;-55° to 125°C	TII
106	TIM9907J	9900	IO-02	Chip	BTD	Priority Encoder;10-Line to 4-Line BCD;Alternate to type 74LS147	TII
107	TIM9907N	9900	IO-02	Chip	BTD	Priority Encoder;10-Line to 4-Line BCD;Alternate to type 74LS147	TII
108	TIM9908J	9900	IO-02	Chip	BTD	Priority Encoder;8-Line to 3-Line Binery;Alt to type 74LS348;3-State Out	TII
109	TIM9908N	9900	IO-02	Chip	BTD	Priority Encoder;8-Line to 3-Line Binery;Alt to type 74LS348;3-State Out	TII
110	TMS9901-40JL	9900	IO-03	Chip	MNG	Programmable Syst Interface Provides Interrupt Control Ceramic Pkg	TII

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	TMS9901-40NL	9900	IO-03	Chip	MNG	Same as TMS9901-40JL Except Plastic Pkg	TII
2	TMS9911-40JL	9900	IO-03	Chip	MNG	Direct Memory Access Controller for 2 Indep Devices Ceramic Pkg	TII
3	TMS9911JL	9900	IO-03	Chip		DMA Controller/Supports 2 Independent DMA Devices	TII
4	TMS9911NL	9900	IO-03	Chip		DMA Controller/Supports 2 Independent DMA Devices	TII
5	TIM9915	9900	IO-03	ChS		Mem Timing/Refresh Controller;Controls Oper of 4k/16k/64k Dynamic RAMS	TII
6	TMS9909JL	9900	IO-07	Chip		Floppy Disc Contr/Programmable Stepper-Motor and Data Transfer Rates	TII
7	TMS9909NL	9900	IO-07	Chip		Floppy Disc Contr/Programmable Stepper-Motor and Data Transfer Rates	TII
8	TMS9927JL	9900	IO-09	Chip	MNG	Video Timer/Controller;40-Pin DIL Cer Pkg	TII
9	TMS9927NL	9900	IO-09	Chip	MNG	Video Timer/Controller;40-Pin DIL Cer Pkg	TII
10	TMS9902-40JL	9900	IO-20	Chip	MNG	Async Comm Controller 18 Pin Dil Ceramic Pkg	TII
11	TMS9902-40NL	9900	IO-20	Chip	MNG	Same as TMS9902-40JL Except Plastic Pkg	TII
12	TMS9902JL	9900	IO-20	Chip	MNG	ASYNC Comm Controller/18-Pin DIL Cer Pkg	TII
13	TMS9902NL	9900	IO-20	Chip	MNG	Async Comm Controller/18-Pin DIL Plas Pkg	TII
14	TMS9903JL	9900	IO-20	Chip	MNG	SYNC Comm Controller/20-Pin DIL Cer Pkg	TII
15	TMS9903NL	9900	IO-20	Chip	MNG	SYNC Comm Controller/20-Pin DIL Plas Pkg	TII
16	SBP9965	9900	IO-30	Chip	BIX	uProc Mem-Mapped I/O Peripheral Interface/8-Bit I/O/40-Pin Pkg	TII
17	TMS9901JL	9900	IO-30	Chip	MNG	Programmable Syst Interface:Provides Interrupt Control,I/O Ports,Clock	TII
18	TMS9901NL	9900	IO-30	Chip	MNG	Programmable Syst Interface:Provides Interrup Control,I/O Ports,Clock	TII
19	TIM9904	9900	IO-32	Chip	BTD	4Ø Clock Gen/Driver/20-Pin DIL Cer or Plas Pkg;Alt to Type 74LS362	TII
20	TMS9914JL	9900	IO-33	Chip	MNG	Gen Pur Interface Bus Adapter/IEEE488-1975-78 Compatible	TII
21	TMS9914NL	9900	IO-33	Chip	MNG	Gen Pur Interface Bus Adapter/IEEE488-1975-78 Compatible;Plastic Pkg	TII
22	TM990/310	9900	IO-33	MOD		I/O Expansion Module;Compatible W/TM990 Microcomp Mod	TII
23	TM990/1240R	9900	IO-40	MOD		Hi Level Analog Output Sys 12 Bit 16SE 8Diff Expandable To 32SE 16Diff	TII
24	TM990/1241R	9900	IO-40	MOD		High Level Analog Output Syst 12 Bits 32SE 16 Diff Combination Analog/Int	TII
25	TM990/1241S	9900	IO-40	MOD		High Level Analog Output Sys 12 BITS 32SE 16Diff Combination Analog/Inter	TII
26	TM990/1243	9900	IO-40	MOD		High Level Analog Output System 8 12-Bit Dacs	TII
27	TIM9905J	9900	IO-43	Chip	BTD	Data Selec/Mux W/3-State Out/16-Pin Cer Pkg;Alt to typ 74LS251	TII
28	TIM9905N	9900	IO-43	Chip	BTD	Data Selec/Mux W/3-State Out/16-Pin Plas Pkg;Alt to type 74LS251	TII
29	SN74S225J	9900	IO-55	Chip	BTD	16x5 Bit Asynch First-In/First-Out Memory	TII
30	SN74S225N	9900	IO-55	Chip	BTD	16x5 Bit Asynch First-In/First-Out Memory	TII
31	TM990/201-41	9900	IO-55	MOD		Memory Expansion Board Bus 8k Bytes EPROM 4k Bytes SRAM Half Socketed	TII
32	TM990/201-42	9900	IO-55	MOD		Same as TM990/201-41 Except 16k Bytes EPROM 8k Bytes SRAM Fully Socketed	TII
33	TM990/201-43	9900	IO-55	MOD		Same as TM990/201-41 Except 32k Bytes EPROM 16k Bytes SRAM Fully Socketed	TII
34	TM990/203-21	9900	IO-55	MOD		Mem Expansion Board Bus 16k Bytes of DRAM	TII
35	TM990/203-22	9900	IO-55	MOD		Same as TM990/203-21 Except 32k Bytes Expandable 64 Bytes of DRAM	TII
36	TM990/203-23	9900	IO-55	MOD		Same as TM990/203-21 Except 64k Bytes of DRAM	TII
37	TM990/206-41	9900	IO-55	MOD		RAM Expansion Mem Board 8k Bytes SRAM Sockets for 16k Bytes	TII
38	TM990/206-42	9900	IO-55	MOD		Same as TM990/206-41 Except 16k Bytes SRAM Fully Socketed	TII
39	TM990/305	9900	IO-55	MOD		Mem and I/O Mem Capacity 32k Using TMS2516 on TMS2532 EPROMS	TII
40	TIM9906J	9900	IO-56	Chip	BTD	8-Bit Addr Latch/16-Pin Cer Pkg;Alt to type 74LS259	TII
41	TIM9906N	9900	IO-56	Chip	BTD	8-Bit Addr Latch/16-Pin Plas Pkg;Alt to type 74LS259	TII
42	SBP9960CJ	9900	IO-57	Chip	BIX	I/O Expander;CRU Based Interface;28-Pin DIL Pkg;o to 70°C	TII
43	SBP9960EJ	9900	IO-57	Chip	BIX	I/O Expander;CRU Based Interface;28-Pin DIL Pkg; -40 to 85°C	TII
44	SBP9960MJ	9900	IO-57	Chip	BIX	I/O Expander;CRU Based Interface;28-Pin DIL Pkg; -55 to 125°C	TII
45	306	9900	PE-10	UNIT		Line Printer	TII
46	588	9900	PE-10	UNIT		Line Printer	TII
47	913AVDT	9900	PE-23	UNIT		Video Display Terminal	TII
48	TM990/301	9900	PE-23	UNIT		Microterminal;Interfaces to TM990 Series Mods,Includes KB,Display	TII
49	733ASR	9900	PE-24	UNIT		Elec Data Term;Keyboard,Entry 30-Character-Per-Second Thermal Printer	TII
50	733KSR	9900	PE-24	UNIT		Elec Data Term;Keyboard Entry,30-Character-Per-Second Thermal Printer	TII
51	733	9900	PE-40	UNIT		SILENT 700 Card Reader;Sys Keyboard Printer/Principle Input/Outp Device	TII
52	804	9900	PE-40	UNIT		Card Reader	TII
53	733ASRROM	9900	PE-50	UNIT		Loader	TII
54▼	TBP28L22J	9900	PROM	Chip	BTDT	256x8 Mask-Programmable ROM	TII
55▼	TBP28L22N	9900	PROM	Chip	BTDT	256x8 Mask-Programmable ROM	TII
56▼	TBP28LA22J	9900	PROM	Chip	BTDT	256x8 Electrically-Programmable ROM	TII
57▼	TBP28LA22N	9900	PROM	Chip	BTDT	256x8 Electrically-Programmable ROM	TII
58▼	TBP28S41J	9900	PROM	Chip	BTD	1024x4 Electrically-Programmable ROM;Tri-State Output	TII
59▼	TBP28S41N	9900	PROM	Chip	BTD	1024x4 Electrically-Programmable ROM;Tri-State Output	TII
60	TMS27L08JL	9900	PROM	Chip	MNG	1024x8 Static Erasable EPROM;Cycle Time 450ns Min	TII
61▼	TBP18S030J	9900	PROM	CHIP	BTD	32x8 Electrically-Programmable ROM;Tri State Output	TII
62▼	TBP18S030M-J	9900	PROM	CHIP	BTD	32x8 Electrically-Programmable ROM;Tri State Output	TII
63▼	TBP18S030M-W	9900	PROM	CHIP	BTD	32x8 Electrically-Programmable ROM;Tri State Output	TII
64▼	TBP18S030N	9900	PROM	CHIP	BTD	32x8 Electrically-Programmable ROM;Tri State Output	TII
65▼	TBP18SA030M-J	9900	PROM	CHIP	BTD	32x8 Electrically-Programmable ROM;O T	TII
66▼	TBP18SA030M-W	9900	PROM	CHIP	BTD	32x8 Electrically-Programmable ROM	TII
67▼	TBP18SA030N	9900	PROM	CHIP	BTD	32x8 Electrically-Programmable ROM	TII
68▼	TBP24S10J	9900	PROM	CHIP	BTD	256x4 Electrically-Programmable ROM;Tri State Output	TII
69▼	TBP24S10M-J	9900	PROM	CHIP	BTD	256x4 Electrically-Programmable ROM;Tri State Output	TII
70▼	TBP24S10M-W	9900	PROM	CHIP	BTD	256x4 Electrically-Programmable ROM;Tri State Output	TII
71▼	TBP24S10N	9900	PROM	CHIP	BTD	256x4 Electrically-Programmable ROM;Tri State Output	TII
72▼	TBP24SA10J	9900	PROM	CHIP	BTD	256x4 Electrically-Programmable ROM;Tri State Output	TII
73▼	TBP24SA10M-J	9900	PROM	CHIP	BTD	256x4 Electrically-Programmable ROM;Tri State Output	TII
74▼	TBP24SA10M-W	9900	PROM	CHIP	BTD	256x4 Electrically-Programmable ROM;Tri State Output	TII
75▼	TBP24SA10N	9900	PROM	CHIP	BTD	256x4 Electrically-Programmable ROM;Tri State Output	TII
76▼	TBP28L22M-J	9900	PROM	CHIP	BTD	256x8 Electrically-Programmable ROM;Tri State Output	TII
77▼	TBP28LA22M-J	9900	PROM	CHIP	BTD	256x8 Electrically-Programmable ROM;Tri State Output	TII
78▼	TBP28S42M-J	9900	PROM	CHIP	BTD	512x8 Electrically-Programmable ROM;Tri State Output	TII
79▼	TBP28SA42M-J	9900	PROM	CHIP	BTD	512x8 Electrically-Programmable ROM;Tri State Output	TII
80	SN54S189J	9900	RAM	Chip	BTD	16x4 Static RAM;Fully Decoded;Tri-State Output	TII
81	SN54S189W	9900	RAM	Chip	BTD	16x4 Static RAM;Fully Decoded;Tri-State Output	TII
82	SN54S289J	9900	RAM	Chip	BTD	16x4 Static RAM;Fully Decoded;Open Collector Output	TII
83	SN54S289W	9900	RAM	Chip	BTD	16x4 Static RAM;Fully Decoded;Open Collector Output	TII
84	SN54S301J	9900	RAM	Chip	BTD	256x1 Static RAM;Fully Decoded;Open Collector Output	TII
85	SN54S301W	9900	RAM	Chip	BTD	256x1 Static RAM;Fully Decoded;Open Collector Output	TII
86	SN74S189J	9900	RAM	Chip	BTD	16x4 Static RAM;Fully Decoded;Tri-State Output	TII
87	SN74S189N	9900	RAM	Chip	BTD	16x4 Static RAM;Fully Decoded;Tri-State Output	TII
88	SN74S201J	9900	RAM	Chip	BTD	256x1 Static RAM;Fully Decoded;Tri-State Output	TII
89	SN74S201N	9900	RAM	Chip	BTD	256x1 Static RAM;Fully Decoded;Tri-State Output	TII
90	SN74S289J	9900	RAM	Chip	BTD	16x4 Static RAM;Fully Decoded;Open Collector Output	TII
91	SN74S289N	9900	RAM	Chip	BTD	16x4 Static RAM;Fully Decoded;Open Collector Output	TII
92	SN74S301J	9900	RAM	Chip	BTD	256x1 Static RAM;Fully Decoded:Open Collector Output	TII
93	SN74S301N	9900	RAM	Chip	BTD	256x1 Static RAM;Fully Decoded;Open Collector Output	TII
94	TMS4036NL	9900	RAM	Chip	MNG	64X8 Static RAM/MAX Access 1us/20-Pin Plas Pkg/3-State Outputs	TII
95	SN54S270J	9900	ROM	Chip	BTD	512x4 Mask-Programmed ROM	TII
96	SN54S271J	9900	ROM	Chip	BTD	256x8 Mask-Programmed ROM	TII
97	SN54S370J	9900	ROM	Chip	BTD	512x4 Mask-Programmed ROM	TII
98	SN54S371J	9900	ROM	Chip	BTD	256x8 Mask-Programmed ROM	TII
99	SN74S270J	9900	ROM	Chip	BTD	512x4 Mask-Programmed ROM	TII
100	SN74S270N	9900	ROM	Chip	BTD	512x4 Mask-Programmed ROM	TII
101	SN74S271J	9900	ROM	Chip	BTD	256x8 Mask-Programmed ROM	TII
102	SN74S271N	9900	ROM	Chip	BTD	256x8 Mask-Programmed ROM	TII
103	SN74S370J	9900	ROM	Chip	BTD	512x4 Mask-Programmed ROM	TII
104	SN74S370N	9900	ROM	Chip	BTD	512x4 Mask-Programmed ROM	TII
105	SN74S371J	9900	ROM	Chip	BTD	256 x 8 Mask-Programmed ROM	TII
106	SN74S371N	9900	ROM	Chip	BTD	256 x 8 Mask-Programmed ROM	TII
107	SN5488AJ	9900	ROM	Chip	BTD	32x8 Mask-Programmed ROM	TII
108	SN7488AJ	9900	ROM	Chip	BTD	32x8 Mask-Programmed ROM	TII
109	SN7488AN	9900	ROM	Chip	BTD	32x8 Mask-Programmed ROM	TII
110	SN54187J	9900	ROM	Chip	BTD	256x4 Mask-Programmed ROM	TII

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE
1	SN54187W	9900	ROM	Chip	BTD	256x4 Mask-Programmed ROM	TII
2	SN74187J	9900	ROM	Chip	BTD	256x4 Mask-Programmed ROM	TII
3	SN74187N	9900	ROM	Chip	BTD	256x4 Mask-programmed ROM	TII
4▼	TBP28S42J	9900	ROM	Chip	BTDT	512x8 Mask-Programmable ROM	TII
5▼	TBP28S42N	9900	ROM	Chip	BTD	512x8 Mask-Programmable ROM	TII
6▼	TBP28SA42J	9900	ROM	Chip	BTD	512x8 Electrically-Programmable ROM	TII
7▼	TBP28SA42N	9900	ROM	Chip	BTD	512x8 Electrically-Programmable ROM	TII
8	SN5488AW	9900	ROM	CHip	BTD	32x8 Mask-Programmed ROM	TII
9	MIKUL600	MIKUL600	COMP	UNIT	MNX	Industrial Control Microcomputer;Uses 6800 CPU	TLI
10	680	MIKUL600	CPU	MOD		Uses 6800 CPU;Auto Restart;Crystal Clock	TLI
11	MIKUL681	MIKUL600	CPU	MOD		Uses 6800 CPU With Watchdog	TLI
12	642	MIKUL600	IO-01	MOD		Hex Interval Timer	TLI
13	630	MIKUL600	IO-02	MOD		System Monitor/Console Terminal Interface	TLI
14	614	MIKUL600	IO-03	MOD		Video RAM Interface	TLI
15	631	MIKUL600	IO-20	MOD		3k 2708 PROM, 3/4k RAM,Serial Terminal Interface	TLI
16	652	MIKUL600	IO-20	MOD		Full RS 232 Serial I/O With Software Selected Baud Rate	TLI
17	654	MIKUL600	IO-20	MOD		Dual 20mA Loop Serial I/O	TLI
18	656	MIKUL600	IO-20	MOD		Quad EIA Serial I/O	TLI
19	700	MIKUL600	IO-20	MOD		LVDT Interface	TLI
20	623	MIKUL600	IO-31	MOD		16 Bit High Power Output	TLI
21	620	MIKUL600	IO-33	MOD		16 Bit TTL I/O With Interrupt Input	TLI
22	621	MIKUL600	IO-33	MOD		16 Bit Optically Isolated Input	TLI
23	624	MIKUL600	IO-33	MOD		32 Bit TTL I/O With Interrupt Input	TLI
24	627	MIKUL600	IO-33	MOD		32 Bit High Power Latch Output	TLI
25	675	MIKUL600	IO-41	MOD		16 Channel/8 Bit Analog Input	TLI
26	622	MIKUL600	IO-43	MOD		16 Digit Thumbwheel SW Multiplexer And 8 Bit High Power Output	TLI
27	610	MIKUL600	IO-55	MOD		1k 1702A PROM/0.5k RAM Memory	TLI
28	611	MIKUL600	IO-55	MOD		4k 2708 PROM/1k RAM Memory	TLI
29	612	MIKUL600	IO-55	MOD		4k x 8 RAM/6k PROM Memory	TLI
30	615	MIKUL600	IO-55	MOD		8k(2716)EPROM/1k RAM Memory	TLI
31	625	MIKUL600	IO-56	MOD		32 Bit Latch Input	TLI
32	600	MIKUL600	IO-92	MOD		Watchdog/Fault Detector	TLI
33	644	MIKUL600	IO-92	MOD		Resolver Interface	TLI
34	MIKUL629	MIKUL600	IO-92	MOD		12 Bit Interface Card	TLI
35	MIKUL717	MIKUL600	PE-16	MOD		6 Digit Multiplexed LED Display	TLI
36	698	MIKUL600	PE-50	UNIT		2708 PROM Programmer	TLI
37	MIKUL716	MIKUL600	PE-61	MOD		General Purpose 16 Key Keyboard	TLI
38	613	MIKUL600	RAM	MOD	MCX	2k CMOS Nonvolatile RAM Memory	TLI
39	618B	MIKUL600	RAM	MOD		12kx8 Static RAM Memory	TLI
40	MIKUL614B	MIKUL600	10-03	MOD		Video RAM Interface	TLI
41	MIKUL632	MIKUL600	10-33	MOD		Dual Via(6522)	TLI
42	MIKUL670G	MIKUL600	10-40	MOD		Dual D/A 12 Bit	TLI
43	MIKUL672	MIKUL600	10-40	MOD		Dual D/A 8 Bit	TLI
44	MIKUL616	MIKUL600	10-55	MOD		8k(2708) or 16k(2716) PROM	TLI
45	MIKUL996	MIKUL6000	COMP	MOD		16k Nonvolitale RAM for 9900	TLI
46	MIKUL6809-1	MIKUL6000	COMP	MOD		1 Card Comp;Uses 6808CPU,1k RAM,418k EPROM,3PIAs	TLI
47	MIKUL6809-2	MIKUL6000	COMP	MOD		1 Card Comp;Uses 6809CPU,2k RAM,4/8k EPROM,2 PIAs,2ACIAs	TLI
48	MIKUL6809-3	MIKUL6000	COMP	MOD		1 Card Comp;Uses 6809CPU,2k RAM,4/8k EPROM,2 PIAs,1ACIA,IPTM	TLI
49	MIKUL6008-2	MIKUL6000	IO-92	MOD		1 Card Comp;Uses 6808CPU,2k RAM,418k EPROM,2PIAs,2ACIAs	TLI
50	MIKUL6032	MIKUL6000	10-33	MOD		32/32 Input/Output Card for 8-Bit Bytes,User Select 1/0 Termination	TLI
51	MIKUL6064	MIKUL6000	10-33	MOD		64 Input Card,User Selectable Address,64 TTL/CMOS Compatible	TLI
52	MIKUL902	MIKUL900	IO-20	MOD		10 Channel Serial I/O Card(9900)	TLI
53	MIKUL995	MIKUL900	IO-55	MOD		9900 Nonvolitable RAM for 9900	TLI
54	MIKUL6001	MIKUL900	IO-55	MOD		For use with T9 Bug Monitor/Debug System Software	TLI
55	MIKUL991	MIKUL900	IO-92	MOD		I/O Expander(9900)	TLI
56	MIKUL993	MIKUL900	IO-92	MOD		Color/Graphic VRAM for 9900	TLI
57	T9BUG/6001	6809	DEV	MOD		Interactive Debug Monitor;3k Byte;Chip or Bus Compatible Board	TLI
58#	TMP8039P	TLCS-84		Chip	MNG	TMP 8049 Without Internal Program Memory	TOSJ
59#	TMP8035P	TLCS-84	uCT	Chip	MNG	TMP 8048 Without Internal Program Memory	TOSJ
60#	TMP8049P	TLCS-84	uCT	Chip	MNG	8 Bit uComp;1.36us Cycle;128/2k RAM/ROM;27I/O Lines;Exp Memory and I/O	TOSJ
61#	TMP8048P	TLCS-84 uCT	uCT	Chip	MNG	8Bit uComp;2.5us Cycle;64/1k RAM/ROM;27I/O Lines;Exp Memory and I/O	TOSJ
62#	TMP8085AP	TLCS-85A	CPU	Chip	MNG	8 Bit Parr CPU;IS 100% Software Comp W/TMP 9080 uProc;4 Vect Interrupt	TOSJ
63#	TMP8755AC	TLCS-85A	EPROM	Chip	MNG	16K Bit EPROM With I/O Ports for Use With TLCS-85A uComp; Eraseable	TOSJ
64▼#	TMP8355P	TLCS-85A	IO-57	Chip	MNG	2048x8 Bit ROM w/2 General Purpose I/O Ports	TOSJ
65#	TMP8155P	TLCS-85A	RAM	Chip	MNG	2048 Bit Static RAM with I/O Parts and Timer;Used W/TLCS-85A uComp;CE Lo	TOSJ
66#	TMP8156P	TLCS-85A	RAM	Chip	MNG	2048 Bit Static RAM with I/O Parts and Timer;Used W/TLCS-85A uComp;CE Hi	TOSJ
67#	TMM314AP	TLCS12		MOD	MNG	1024 x 4 Bit R/W Static RAM;I/O TTL Compatible; 450ns Access Time, 550mW	TOSJ
68#	T3219	TLCS12	IO-02	Chip		8-Bit Interrupt Latch Unit	TOSJ
69#	T3217	TLCS12	IO-21	Chip		12 Bit Bidirectional Bus Driver	TOSJ
70#	T3218	TLCS12	IO-33	Chip		I/O Device Control Unit	TOSJ
71#	T3220	TLCS12	IO-55	Chip		General Purpose 4/8 Bit Register	TOSJ
72#	T3146	TLCS12	PROM	Chip		512x4 Bit Rewritable ROM	TOSJ
73#	TMM322C	TLCS12	PROM	MOD	MNG	1024 x 8 Bit Static EPROM;I/O TTL Compatible,Tri State;DIP Ceramic	TOSJ
74#	TMM334P	TLCS12	PROM	MOD	MNI	2048 x 8 Bit Mask ROM;I/O TTL Compatible;Tri State; 450ns Access Time	TOSJ
75#	T3151	TLCS12	RAM	Chip		128x4 Bit Static RAM	TOSJ
76#	TC5501P	TLCS12	RAM	MOD	MXG	256x4 Bit R/W RAM;Nonvolatile;Tri State;I/O,TTL;DIP;Access Time:450ns	TOSJ
77#	T3216	TLCS12	ROM	Chip		Memory Control Unit	TOSJ
78#	T3233	TLCS12	ROM	Chip		512x4 Bit Mask ROM	TOSJ
79#	TMM323C	TLCS12	ROM	MOD	MNG	2048 x 8 Bit ROM;Tri State;Access Time: 450ns;525mW;DIP Ceramic	TOSJ
80#	T3190-1	TLCS12A	CPU	Chip	MPG	12 Bit Parallel CPU,3 Phase Clock,Higher Speed Than T3190	TOSJ
81#	EX-12/5	TLCS12A	IO-57	MOD		12 Bit 1k Word RAM/ROM Byte	TOSJ
82#	EX-1A	TLCS12A	RAM	ChS		12 Bit 4k Word RAM	TOSJ
83#	T3541A	TLCS122	RAM	Chip	MXG	R/W Controller,Nonvolatile;RAM/ROM Op	TOSJ
84▼#	TMP4300C	TLCS43	uCT	Chip	MNG	4-Bit Single Chip uComputer;External 2048x8 Bit ROM/128x4 Bit RAM Cap	TOSJ
85▼#	TMP4310AP	TLCS43	uCT	Chip	MNG	4-Bit Single Chip uComputer;Internal 1024x8 Bit ROM/48x4 Bit RAM Cap	TOSJ
86▼#	TMP4310APL	TLCS43	uCT	Chip	MNG	4-Bit Single Chip uComputer;Internal 1024x8 Bit ROM/48x4 Bit RAM Cap	TOSJ
87▼#	TMP4315BP	TLCS43	uCT	Chip	MNG	4-Bit Single Chip uComputer;Internal 1536x8 Bit ROM/64x4 Bit RAM Cap	TOSJ
88▼#	TMP4320AP	TLCS43	uCT	Chip	MNG	4-Bit Single Chip uComputer;Internal 2048x8 Bit ROM/128x4 Bit RAM Cap	TOSJ
89▼#	TCP4600AC	TLCS46A	uCT	Chip	MNG	4-Bit Single Chip uComputer;External 4096x8 Bit ROM/160x4 Bit RAM Cap	TOSJ
90▼#	TCP4620AP	TLCS46A	uCT	Chip	MNG	4-Bit Single Chip uComputer;Internal 2048x8 Bit ROM/96x4 Bit RAM Cap	TOSJ
91▼#	TCP4630AP	TLCS46A	uCT	Chip	MNG	4-Bit Single Chip uComputer;Internal 3072x8 Bit ROM/160x4 Bit RAM Cap	TOSJ
92#	EX-80	TLCS80	IO-57	MOD		8 Bit 2k RAM/4k ROM	TOSJ
93#	EX-80BS	TLCS80	IO-57	MOD		8 Bit 16k RAM/ROM	TOSJ
94▼#	TMP8243P	TLCS84	IO-23	Chip	MNG	I/O Expander;Four 4-Bit I/O Ports;And/Or Directly to Ports	TOSJ
95#	TDS400	TLCS85A	IO-57	ChS		8 Bit 48k RAM/16k ROM	TOSJ
96#	TDS800	TLCS85A	IO-57	ChS		8 Bit 48k RAM/16k ROM	TOSJ
97▼#	TMP8255AP	TMP9080A	IO-30	Chip	MNG	Prog Peripheral Interface;Programmable Modes of Oper;24 Prog I/O Pins	TOSJ
98▼#	TMP8255AP-5	TMP9080A	IO-30	Chip	MNG	Prog Peripheral Interface;Programmable Modes of Oper;24 Prog I/O Pins	TOSJ
99	MECA43	MECA43	COMP	UNIT		Digital Computer W/8 Bit Slice Arith Unit,Microprogrammed	TSC
100	BCD/R	MECA43	IO-20	HYB		Dual Bus Coupler Driver/Receiver:MIL STD 1553 Compatible,Bus Interface	TSC
101	DCU	MECA43	IO-30	HYB		Data Channel Unit:Avionics Mux Data Bus MIL STD1553 Compatible	TSC
102	MTU	MECA43	IO-43	HYB		Multiplex Terminal Unit:MIL STD 1553 Compatible,Par to Ser	TSC
103	MAIO2	MICROLINE	IO-20	MOD		2 Ch Asynchronous IO Board:2 Full Duplex Ser I/O Ports,S/Ware Progm Timer	UTE
104	MAIO4	MICROLINE	IO-20	MOD		4 Ch Asynchronous IO Board:4 Full Duplex Ser I/O Ports,S/Ware Progm Timer	UTE
105	MSIO2	MICROLINE	IO-20	MOD		2 Ch Synchronous IO Board:2 Full Duplex Ser I/O Ports,Dual RS232C	UTE
106	MICROSTOR	VECTOR MZ	PE-01	UNIT		Add-On Dual Micropulis Drives	VGI
107	VECTORMZ	VECTORMZ	COMP	UNIT		8 Bit Microcomputer Based on Z80A CPU and S100 Bus	VGI
108	VECTORMZ80CPU	VECTORMZ	CPU	MOD		Z-80 CPU Board;Uses Mosteks Z80A CPU;158 Instructions	VGI
109	VECTOR1PLUS	VECTOR1	COMP	UNIT	MNG	8 Bit Microcomputer Based On 8080A CPU and S100 Bus;Incl Minifloppy Disc	VGI
110	VGM	VECTOR1	COMP	UNIT		8 Bit Microcomputer;Includes VECTOR1,VECTOR1PLUS and 2 Minifloppy Discs	VGI

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	AVDB2	VECTOR1	IO-09	MOD		Alphanumeric Video Display Board;Generates 80 Char 24 Lines Display	VGI
2	AVDB	VECTOR1	IO-09	MOD		Flash writer Video Display Board;Generates 64 Char 16 Lines Display	VGI
3	HRGDB	VECTOR1	IO-09	MOD		High Resolution Graphics Display Board;256H x 240V Screen Element Display	VGI
4	BSIOB	VECTOR1	IO-20	MOD		Bit Streamer I/O Board;Uses 8251 USART;Also Operates as RS232 Port	VGI
5	PAIB	VECTOR1	IO-40	MOD		Precision Analog Interface Board;Uses 12 Bit Accu DACs	VGI
6	AIB	VECTOR1	IO-41	MOD		Analog Interface Board;Includes 8 Bit Port,4A to D Inputs	VGI
7	12KPRB	VECTOR1	IO-55	MOD		12K PROM/RAM Board;12k Bytes EPROM 2708 and 1k Byte Static RAM	VGI
8	16KSMB	VECTOR1	IO-55	MOD		16k Static Memory Board	VGI
9	PRB3	VECTOR1	IO-55	MOD		12k PROM ROM;12k 2708 EPROM;1k Static RAH;EPROM Programming Socket	VGI
10	PRB	VECTOR1	IO-55	MOD		PROM/RAM Board;1k RAM 2102;PROM up to 2k Byte 1702A;Usable W/ALTAIR	VGI
11	8KSRB	VECTOR1	IO-57	MOD		8k Static RAM Board;Buffered Address Lines W/Schmitt Triggers	VGI
12	DSS	VECTOR1	PE-01	UNIT		Dual-Stor System;Floppy Disk System,Dual,243k Bytes Per Disk	VGI
13	48KDRB	Z80	IO-55	MOD		48K Dynamic RAM Board/For Any S-100 Bus COMP. Using Z-80 CPU	VGI
14	SYSTEM100	PDP-11	DEV	UNIT		PDP-11/03,56kB Mos Mem,2-500kB Disk Dr,4-Port Mux,VT-100CRT,Printer	VIR
15	SYSTEM200	PDP-11	DEV	UNIT		PDP-11/34,128kB Par Mem,2-28MB Disk Dr,8-Port Mux,6 VT-100CRT,Printer	VIR
16	SYSTEM300	PDP-11	DEV	UNIT		PDP-11/34,128kB Par MEM,2-28MB Disk Dr,8-Port Mux,6 VT-100 CRT,Prin,LA36	VIR
17	SYSTEM400	PDP-11	DEV	UNIT		PDP-11/34,256kB Par Mem,2 8-Port Mux,12 VT-100CRT,2-28MB Disk Dr,Pr,LA36	VIR
18	CR1872	CR1872	uCT	Chip	MPG	4 Bit One Chip Microcontroller;Includes Processor,Storage,I/O Function	WDC
19	MCP1600	MCP1600	CPU	ChS	MNG	8 Bit 3 Chip CPU;CP1611B Data Chip,CP1621 Control Chip,CP1331 Microm Chip	WDC
20	MC160	MCP1600	DEV	MOD	MNG	Microcontroller Program Development System	WDC
21	MC160-01	MCP1600	DEV	MOD	MNG	Microcontroller Program Development Syst;Microinstruction Bus Interface	WDC
22	MC160-02	MCP1600	DEV	MOD	MNG	Microcontroller Program Development Syst;Microm Simulator-RAM	WDC
23	MC160-03	MCP1600	DEV	MOD	MNG	Microcontroller Program Development Syst;Microm Simulator-PROMs	WDC
24	CP1621	MCP1600	IO-01	Chip	MNG	Control Chip Interprets Macro-Instructions,11 Bit Return Reg	WDC
25	DM1881B	MCP1600	IO-03	Chip	MNG	Direct Memory Access (DMA) Controller	WDC
26	FD1771B	MCP1600	IO-07	Chip	MNG	Floppy Disk Controller/Formatter	WDC
27	BR2941L	MCP1600	IO-20	Chip	MNG	Dual Baud Rate Clock;16 Selectable Baud Rate Clock Freqs	WDC
28	UC1671B	MCP1600	IO-20	Chip	MNG	Asynchronous/Synchronous Receiver/Transmitter	WDC
29	UC1971A	MCP1600	IO-20	Chip	MNG	Chip Select Astro:Sync/Asyn Rec/Trans,Full Duplex;Cer Pkg	WDC
30	UC1971B	MCP1600	IO-20	Chip	MNG	Chip Select Astro:Sync/Asyn Rec/Trans,Full Duplex;Plastic Pkg	WDC
31	WD1931A	MCP1600	IO-20	Chip		Asynch/Synch Receiver/transmitter;Full Duplex;DC to 1M Baud/s	WDC
32	WD1931B	MCP1600	IO-20	Chip		Asynch/Synch Receiver/Transmitter;Full Duplex;DC to 1M Baud/s	WDC
33▼	WD1933A	MCP1600	IO-20	Chip	MNX	Sync Data Link Controller:DC to 2.05M Bits/sec Baud Rate;Error Detection	WDC
34▼	WD1933B	MCP1600	IO-20	Chip	MNX	Sync Data Link Controller:DC to 2.05M Bits/sec Baud Rate;Error Detection	WDC
35	CP1611B	MCP1600	IO-33	Chip	MNG	16 Bit DAL Bus Data Chip	WDC
36	CP1851B	MCP1600	IO-33	Chip	MNG	General Purpose Parallel Input/Output	WDC
37	FR1502E	MCP1600	IO-55	Chip		FIFO Buffer Register:9-Bitx40 Char Stack;Ceramic Pkg	WDC
38	FR1502F	MCP1600	IO-55	Chip		FIFO Buffer Register:9-Bitx40 Char Stack;Plastic Pkg	WDC
39	SR1641D	MCP1600	RAM	Chip	MNG	256 x 4 RAM;Access Time 300ns Max	WDC
40	CP1631	MCP1600	ROM	Chip	MNG	512 Word By 22 Bit Pattern Mask Programmable ROM;Access Time 200ns	WDC
41	MP1600	MP1600	CPU	ChS	MNG	16 Bit 4 Chip CPU;CP1651B Data Chip,CP1661B Control Chip,2CP1631B Microm	WDC
42	MP160	MP1600	DEV	MOD	MNG	Microcontroller Program Devel.Syst;Microprocessor Board	WDC
43	MP160-01	MP1600	DEV	MOD	MNG	Microcontroller Program Devel.Syst;TTY-HSPTR/P Interface	WDC
44	MP160-02	MP1600	DEV	MOD	MNG	Microcontroller Program Devel.Syst;8kx16 Bit Dyn.RAM	WDC
45	MP160-03	MP1600	DEV	MOD	MNG	Microcontroller Program Devel.Syst;Floppy Disk Controller	WDC
46	BR1941L	MP1600	IO-20	Chip		Dual BAUD Rate Generator	WDC
47	CG1921J	MP1600	IO-32	Chip		Four Phase Clock Generator	WDC
48	WD4020A	WD4200	uCT	Chip	MNG	ROMless Microcontroller;64x4 RAM,Addresses up to 1kx8 ROM;Cer Pkg	WDC
49	WD4020B	WD4200	uCT	Chip	MNG	ROMless Microcontroller;64x4 RAM,Addresses up to 1kx8 ROM;Plastic Pkg	WDC
50	WD4200E	WD4200	uCT	Chip	MNG	Single Chip Microcontroller:1kx8 ROM,64x4 RAM,23 I/O Lines,Cer Pkg	WDC
51	WD4200F	WD4200	uCT	Chip	MNG	Single Chip Microcontroller:1kx8 ROM,64x4 RAM;23 I/O Lines,Plastic Pkg	WDC
52	WD4210E	WD4200	uCT	Chip	MNG	Single Chip Microcontroller:1kx8 ROM,64x4 RAM;19 I/O Lines;Cer Pkg	WDC
53	WD4210F	WD4200	uCT	Chip	MNG	Single Chip Microcontroller:1kx8 ROM,64x4 RAM;19 I/O Lines;Plastic Pkg	WDC
54	WD900	WD9000	COMP	MOD		Computer on a Card:16 Bit,Uses WD9000 Chip Set;64k RAM	WDC
55	WD90	WD9000	COMP	UNIT		Computer System:16 Bit,Uses WD9000 Chip Set	WDC
56	WD9000	WD9000	CPU	ChS		Pascal MICROENGINE Microprocessor Chip Set:16 Bits,5 Chips	WDC
57	DM1883A	WD9000	IO-03	Chip		Direct Mem Access Controller;8 Bit Bidir Data Bus;Ceramic Pkg	WDC
58	DM1883B	WD9000	IO-03	Chip		Direct Mem Access Controller;8 Bit Bidir Data Bus;Plastic Pkg	WDC
59▼	FD1691V	WD9000	IO-07	Chip	MNG	Floppy Support Logic:Direct Interface to FD179x Services;Plastic Package	WDC
60	FD1781A	WD9000	IO-07	Chip		Floppy Disk Formatter/Controller;Soft Sector Format Compatibility	WDC
61	FD1781B	WD9000	IO-07	Chip		Floppy Disk Formatter/Controller;Soft Sector Format Compatibility	WDC
62	FD1791A	WD9000	IO-07	Chip		Floppy Disk Formatter/Controller;Double Density;Read/Write Mode	WDC
63▼	FD1791A-02	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:Inverted Data Bus;Ceramic Package	WDC
64	FD1791B	WD9000	IO-07	Chip		Floppy Disk Formatter/Controller;Double Density;Read/Write Mode	WDC
65▼	FD1791B-01	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:Inverted;Single/Double Density	WDC
66▼	FD1791B-02	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:Inverted Data Bus;Plastic Package	WDC
67	FD1792A	WD9000	IO-07	Chip		Floppy Disk Formatter/Controller;Single Density;Read/Write Mode	WDC
68▼	FD1792A-01	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:Single Density Only;Inverted Data Bus	WDC
69	FD1792B	WD9000	IO-07	Chip		Floppy Disk Formatter/Controller;Single Density;Read/Write Mode	WDC
70▼	FD1792B-01	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:Inverted;Single Density Only	WDC
71▼	FD1793A-01	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:Single/Double Density;True Data Bus	WDC
72▼	FD1793A-02	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:True Data Bus;Ceramic Package	WDC
73▼	FD1793B-01	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:True Single/Double Density	WDC
74▼	FD1793B-02	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:True Data Bus;Plastic Package	WDC
75▼	FD1794A-01	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:Single Density Only;True Data Bus	WDC
76▼	FD1794B-01	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:True Single Density Only	WDC
77▼	FD1795A-02	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:Inverted Data Bus;Side Selection	WDC
78▼	FD1795B-02	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:Inverted Data Bus;Side Selection	WDC
79▼	FD1797A-02	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:True Data Bus;Side Selection	WDC
80▼	FD1797B-02	WD9000	IO-07	Chip	MNG	Floppy Disk Formatter/Controller:True Data Bus;Side Selection	WDC
81▼	FD1691U	WD9000	IO-92	Chip	MNG	Floppy Support Logic:Direct Interface to FD197x Series;Ceramic Package	WDC
82	WD8250A	Z80,MCS80	IO-20	Chip	MNG	Asynch Communications Element:DC to 65k Baud;Cer Pkg	WDC
83	WD8250B	Z80,MCS80	IO-20	Chip	MNG	Asynch Communications Element:DC to 65k Baud;Plastic Pkg	WDC
84	uPSeries	uP Series	COMP	UNIT		8 Bit System Uses Intel 8080A	WLD
85	CPU1	uP Series	CPU	MOD		8 Bit CPU;Uses Intel 8080A,3.25 x 4.5 in Card	WLD
86	PI-1	uP Series	IO-02	MOD		8 Level Priority Interrupt Module	WLD
87	MC1	uP Series	IO-03	MOD		Static Memory Control Module;3.25 x 4.5 in Card	WLD
88	MC3	uP Series	IO-03	MOD		Static Memory Controller Module;For 32k Mem	WLD
89	232-1	uP Series	IO-20	MOD		Interface Conforming to EIA Standard RS232	WLD
90	BRG1A	uP Series	IO-20	MOD		Baud Rate Generator	WLD
91	MES4A	uP Series	IO-20	MOD		4 Transformer Coupled Electronic Switches,Usable as Line Driver/Rec	WLD
92	MLD8	uP Series	IO-20	MOD		8 Differential Line Drivers for Data Transmission to 6000 ft	WLD
93	MLR8	uP Series	IO-20	MOD		8 Differential Line Receivers for Data Transmission to 6000 ft	WLD
94	SCL1	uP Series	IO-20	MOD		Full Duplex Ser Current Loop Interface;For Communication	WLD
95	SCL1A	uP Series	IO-20	MOD		20mA Serial Curr Loop Interface;Data Rates from 110 to 38.4k Baud	WLD
96	SCL2	uP Series	IO-20	MOD		20mA Serial Curr Loop Interface;Data Rate From 110-9.6k Baud	WLD
97	BRG1B	uP Series	IO-32	MOD		Multiple Frequency Crystal Oscillator	WLD
98	RTC-1	uP Series	IO-32	MOD		Relative Time Clock and Watchdog Timer	WLD
99	BE-1	uP Series	IO-33	MOD		IO and Control Bus Extender for Use with CPU1,Can Drive to 64 Mods	WLD
100	BIO2	uP Series	IO-33	MOD		Programmable 24 Bit Input/Output Interface	WLD
101	BIO3	uP Series	IO-33	MOD		Optically Isolated Input Module;8 Bit Input Port	WLD
102	BIO4	uP Series	IO-33	MOD		Optically Isolated Input Module;8 Bit Latched Output Interface	WLD
103	IOC1	uP Series	IO-33	MOD		Input/Output Controller Interfaces 16 I/O Modules;3.25x4.5 in Card	WLD
104	DAC-1A	uP Series	IO-40	MOD		One,8 Bit DAC,Output ±1,±5,±10,0-5 or 0-10V,Includes Cont Logic	WLD
105	DAC-1B	uP Series	IO-40	MOD		Two,8 Bit DAC,Output ±1,±5,±10,0-5 or 0-10V,Includes Cont Logic	WLD
106	ADC3	uP Series	IO-41	MOD		Analog I/O Mod;12 Bit,8 Ch Differential ADC	WLD
107	DAC2A	uP Series	IO-41	MOD		Analog I/O Mod;One 12 Bit DAC	WLD
108	MEM2	uP Series	IO-55	MOD		256 Static RAM and 1024 ERPROM Module	WLD
109	HSA1	uP Series	IO-90	MOD		High-Speed Arithmetic Module FLT PT Multiply 84us;Sine x 2.2ms	WLD
110	LLA1	uP Series	IO-92	MOD		One Low-Level Differential Amp;Amplifies Low-Level Signals For ADC-3	WLD

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	[5] COMPONENT TYPE No. (NOTE 1)	[2] SYSTEM (FAMILY) TYPE No.	[3] COMP. CLASS	[4] COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	[1] MFR. CODE
1	LLA2	uP Series	IO-92	MOD		Two Low-Level Differential Amplifiers;Gains of 1,10,100,1000 Selectable	WLD
2	MAS2	uP Series	IO-92	MOD		Two 115V,4A SCRs W/Ckt Breakers,Reed Relay Isolated,Logic Control Inputs	WLD
3	MAS2A	uP Series	IO-92	MOD		Two 115V,15A Triacs W/Optically Isolated Logic Compatible Cont Inputs	WLD
4	PCI-1A	uP Series	IO-92	MOD		Process Control Inp Mod W/Resistor for Terminating 8,4-20mA Curr Loop	WLD
5	PCI-1B	uP Series	IO-92	MOD		Process Control Inp Mod W/Resistor for Terminating 8,10-50mA Curr Loop	WLD
6	PCO-1A	uP Series	IO-92	MOD		Two 4,0-20mA Current Loop Process Control Outputs	WLD
7	PCO-1B	uP Series	IO-92	MOD		Two,10-50mA Current Loop Process Control Outputs	WLD
8	PWC-2	uP Series	IO-92	UNIT		Prewired Cabinet for Analog/Dig Appln;Includes PWR-2 and Pow Sup	WLD
9	PWD-1	uP Series	IO-92	UNIT		Prewired Drawer for Dig I/O Applications;Includes Power Supply	WLD
10	PWD-2	uP Series	IO-92	UNIT		Prewired Drawer for Analog/Dig Appln;Includes Power Supply	WLD
11	PWR-1	uP Series	IO-92	UNIT		Prewired Rack W/28 Slot Card File for Dig I/O Applications	WLD
12	PWR-2	uP Series	IO-92	UNIT		Prewired Rack for Analog/Digital Applications	WLD
13	PTR-1	uP Series	PE-42	UNIT		300 Character/Sec Paper Tape Reader W/uP Interface	WLD
14	FP1	uP Series	PE-61	MOD		Standard Front Panel;Provides Control,Data Entry and Display	WLD
15	FP2	uP Series	PE-61	MOD		Front Panel with uP/PDP-11 Interface	WLD
16	PSC-1	uP Series	PE-61	MOD		Program Start Card,Used in Absence of FP-1 Front Panel	WLD
17	445-M	uP Series	PE-61	UNIT		Gen Purpose Operator Control Station W/Push Button Switches,6x6x8inch Enc	WLD
18	MEM4	uP Series	PROM	MOD		Module W/Sockets for Four 1k x 8 Bit ERPROMS,2708	WLD
19	MEM5	uP Series	PROM	MOD		1024 x 8 Bit ERPROM	WLD
20	MEM9	uP Series	PROM	MOD		2k EPROM (TMS2516)	WLD
21	MEM1B	uP Series	RAM	MOD		1024 x 8 Static RAM;Max Read/Write Time 500ns;3.25 x 4.5 in Card	WLD
22	MEM3	uP Series	RAM	MOD		4096 x 8 Bit Static RAM Module	WLD
23	MEM6	uP Series	RAM	MOD		1k x 8 Bit RAM W/Battery Backup and Power Fail Interrupt	WLD
24	MEM8	uP Series	RAM	MOD		2048 x 8 Bit Static RAM	WLD
25▼	MFC04		IO-07	MOD		Floppy Controller Module up to 4 Drives	WTK
26▼	MSI02		IO-20	MOD		Serial I/O Module Allows Sys to Support Multiple RS-232C;2 Ports	WTK
27▼	MSI04		IO-20	MOD		Serial I/O Module Allows Sys to Support Multiple RS-232C;4 Ports	WTK
28▼	MSI06		IO-20	MOD		Serial I/O Module Allows Sys to Support Multiple RS-232C;6 Ports	WTK
29▼	MSI08		IO-20	MOD		Serial I/O Module Allows Sys to Support Multiple RS-232C;8 Ports	WTK
30▼	MAI01		IO-33	MOD		Analog Interface Module Allows Input of Analog Signals;1 8-Bit ADC	WTK
31▼	MAI02		IO-33	MOD		Analog Interface Module Allows Input of Analog Signals;1 12 Bit ADC	WTK
32▼	MAI03		IO-33	MOD		Analog Interface Module Allows Input of Analog Signals;1 8 Bit ADC/1 MUX	WTK
33▼	MAI04		IO-33	MOD		Analog Interface Module Allows Input of Analog Signals;1 12 Bit ADC/1 MUX	WTK
34▼	MAI10		IO-33	MOD		Analog Interface Module Allows Input of Analog Signals;1 8-Bit DAC	WTK
35▼	MAI11		IO-33	MOD		Analog Interface Module Allows Input of Analog Signals;1 8-Bit DAC/ADC	WTK
36▼	MAI20		IO-33	MOD		Analog Interface Module Allows Input of Analog Signals;2 8-Bit DAC	WTK
37▼	MPI04		IO-33	MOD		Parallel I/O Module Provides Economic Basis to Add Multi Lines 4 Ports	WTK
38▼	MPI06		IO-33	MOD		Parallel I/O Module Provides Economic Basis to Add Multi Lines 6 Ports	WTK
39▼	MPI08		IO-33	MOD		Parallel I/O Module Provides Economic Basis to Add Multi Lines 8 Ports	WTK
40▼	MCS00		IO-92	MOD		Cassette/RS-232C Interface;Audio Cassette IF to Control Mod for Load/Dump	WTK
41▼	MCS01		IO-92	MOD		Cassette/RS-232C Interface;Audio Cassette IF to Control Mod for Load/Dump	WTK
42▼	MCT00		IO-92	MOD		Counter/Timer Module;Multipurpose;Accurate Measurements of Time/Freq	WTK
43▼	MCT02		IO-92	MOD		Counter/Timer Module;w/2 Prescaler	WTK
44▼	MCT10		IO-92	MOD		Counter/Timer Module;w/Battery Backup	WTK
45▼	MDSxy		IO-92	MOD		Driver/Sensor Module;Various Driver Pairs/Sensors	WTK
46▼	MEP03		ROM	MOD		EROM Programmer Module for 2704/2708;PREROM-E on Cassette	WTK
47▼	MRO16		ROM	MOD		ROM Module Allows Sys Read-Only-Mem Expansion -64k Bytes	WTK
48▼	MRO04	MCM68308	ROM	MOD		ROM Module Allows Sys Read-Only-Mem Expansion-64k Bytes	WTK
49▼	MRO08	MCM68308	ROM	MOD		ROM Module Allows Sys Read-Only-Mem Expansion-64k Bytes	WTK
50▼	MRO12	MCM68308	ROM	MOD		ROM Module Allows Sys Read-Only-Mem Expansion -64k Bytes	WTK
51	MGP00	Wince6800	IO-92	MOD		IEEE 488 GRIP Interface	WTK
52	MSS00	Wince6800	IO-92	MOD		Solid State Relay	WTK
53	MEP04	Wince6800	PROM	MOD		PROM Programmer for 2716	WTK
54	CM6800	WINCE 6800	COMP	MOD		8 Bit Computer On A Card Uses MOTA 6800 CPU, 6.5X4.5in PCB	WTK
55	WINCECTM	WINCE 6800	IO-01	MOD		Counter/Timer Module:Freq/Event Counter,Free Running Timer	WTK
56	CS6800	WINCE 6800	IO-05	MOD		Cassette Interface Module	WTK
57	WINCEFCM	WINCE 6800	IO-07	MOD		Floppy Controller Module:Interfaces to Full/Min Floppy Drive	WTK
58	WINCECIOM	WINCE 6800	IO-10	MOD		Console I/O Mod:16 Keys for Data Entry,15 LED Displays 7 Seq	WTK
59	WINCESIOM	WINCE 6800	IO-20	MOD		Serial I/O Mod:Options 2,4,6 or 8 RS232c Ser IO Ports	WTK
60	WINCEPIOM	WINCE 6800	IO-30	MOD		Parallel I/O Mod:64 I/O Lines Organized as Eight 8 Bit Ports	WTK
61	DS6800	WINCE 6800	IO-31	MOD		Relay Driver,Input Sensor Module	WTK
62	AD6800	WINCE 6800	IO-41	MOD		Analog-To-Digital Conv;Digital-To-Analog Conv;Multiplexer Module	WTK
63	FD6800	WINCE 6800	PE-01	UNIT		Flexible Disk System	WTK
64	PP6800	WINCE 6800	PROM	MOD		PROM Program Module For 2704,512x8 And 2708,1028x8,Erasable PROM	WTK
65	RA6800#1	WINCE 6800	RAM	MOD		Dynamic RAM Refresher Module,4.50 x 6.50 In PCB	WTK
66	RA6800#2	WINCE 6800	RAM	MOD		Dynamic RAM Module Used W/Refresher Module For 65k Memory Expansion	WTK
67	RA6800#3	WINCE 6800	RAM	MOD	MCX	CMOS RAM with Battery Back Up Module	WTK
68	RO6800	WINCE 6800	ROM	MOD		ROM Module With 16 Sockets For 2708s (1024x8 EROMS)	WTK
69▼	MCLxy	6800	CPU	MOD		Control Module;Pwr Three Volt Version 5/±12V;Various Config RAM -4k	WTK
70▼	MCVxy	6800	CPU	MOD		Control Module;Single Volt VerWTK ol Module;Single Volt Ver	WTK
71▼	MR100	6800	IO-57	MOD		RAM/I/O Controller;Generates Various Contr Signals;Contr -4 RAM Modules	WTK
72▼	MCMxy	6800	RAM	MOD	MXX	RAM/BATTERY MODULE;Ava 1-8k RAM;w/without Battery	WTK
73▼	MRA04	6800	RAM	MOD		RAM Module;4k Bytes;Allows Mem Expansion to 64k Bytes	WTK
74▼	MRA08	6800	RAM	MOD		RAM Module;8k Bytes;Allows Mem Expansion to 64k Bytes	WTK
75▼	MRA12	6800	RAM	MOD		RAM Module;12k Bytes;Allows Mem Expansion to 64k Bytes	WTK
76▼	MRA16	6800	RAM	MOD		RAM Module;16k Bytes;Allows Mem Expansion to 64k Bytes	WTK
77	VDB	ALPHA	IO-09	MODS		Video Display Board;S100 Bus Compatible;80 Char/line;25 Lines/Screen	XIT
78	X1TANALPHAMF	ALPHA	IO-92	UNIT		S100 Bus Maniframe;Includes Logic Ckt and Power Supply	XIT
79	DDDC	ZPU-2	IO-07	MOD		Dual-Density Disk Controller/S-100 Bus to Disk Drive Interface	XIT
80#	PPZ80-EB	Z80	DEV	MOD	MNG	Same as PPZ80-B;w/4 ROM/PROM/ESGAI as PPZ80-B;w/4 ROM/PROM/Eup to 8k	Y
81	ZT488	SBC80/05,10	DEV	UNIT		General Purpose Interface Bus IEEE 488 Analyzer,Used in Design,Debug	ZIA
82	ZT80	SBC80/05,10	IO-02	MOD		General Purpose Interface Bus IEEE 488(GPIB)Controller	ZIA
83	ZT7399	STD7000	IO-33	MOD		Dual 4 Digit BCD Counter/Timer for STD Bus (w/Optional Display)	ZIA
84	ZT7502	STD7000	IO-33	MOD		Octal Reed Card for STD Bus Dry or Mercury-Wetted;SPST/SPST	ZIA
85	ZT7488	STD7000	MOD	IO-92		General Purpose Interface Bus IEEE 488(GP1B)Controller	ZIA
86▼	Z-CIO-UCS		IO-33	CHIP		Counter/Timer and Parallel I/O Unit;3-16 Bit Counter;8 Bit I/O Port	ZIL
87▼	Z-CIO-UPS		IO-33	CHIP		Counter/Timer and Parallel I/O Unit;3-16 Bit Counter;8 Bit I/O Port	ZIL
88	PDS	PDS	COMP	UNIT		Program Development System:Including Hard/Software	ZIL
89	ZDS-PPB	ZDS	DEV	MOD		Combination PROM/EPROM Programmer Board	ZIL
90	ZDS-PPB/16	ZDS	DEV	MOD		Programmer Board:Accepts 2716 EPROM,82S27,82S181,82S131 PROMs	ZIL
91	ZDS-1/25	ZDS	DEV	UNIT		Emulator:For Devel of Prototype Syst Using Z80A,Clock Rates to 2.5MHz	ZIL
92	ZDS-1/40	ZDS	DEV	UNIT		Emulator:For Devel of Prototype Syst Using Z80/Z80A,Clock Rates to 4MHz	ZIL
93	ZDS-CIB	ZDS	IO-08	MOD		Prewired I/O Board for ZDS-306C Printer	ZIL
94	ZDS-ASPIO	ZDS	IO-20	MOD		I/O Bd:Incl One RS232 or Curr Loop Port,Interface for Printer,SW Driver	ZIL
95	ZDS-PIB	ZDS	IO-30	MOD		Parallel Interface Board:Provides 32Bidir IO Bits	ZIL
96	ZDS-306C	ZDS	PE-10	UNIT		Line Printer 120cps Impact,Includes Cable	ZIL
97	ZDS-CRT	ZDS	PE-23	UNIT		CRT Data Terminal;Software Carsor Control,Incl Cable	ZIL
98	ZDS-PRINT	ZDS	PE-24	UNIT		ZDS Printer Terminal:250 Lpm,10 Char/Line,120 Char/Sec,Bidir	ZIL
99▼	Z8MCUCS	Z8	uCT	CHIP		uComputer Unit;2k Byte ROM 32 I/O Lines;62k Addr Extern for Prog/Data Mem	ZIL
100▼	Z8MCUPS	Z8	uCT	CHIP		uComputer Unit;2k Byte ROM 32 I/O Lines;62k Addr Extern for Prog/Data Mem	ZIL
101	Z8-01MCCCS	Z8	CPU	Chip		32 I/O Lines;144 Byte Register File;Hi Speed Inst.4.25uS Max;Ceramic	ZIL
102	Z8-01MCCPS	Z8	CPU	Chip		32 I/O Lines;144 Byte Register File; Hi Speed Inst.4.25us Max; Plastic	ZIL
103	PDS8000MODEL10	Z8	DEV	MOD		Single User,General Purpose Microcomputer System	ZIL
104	PDS8000MODEL15	Z8	DEV	MOD		Single User,General Purpose Microcomputer System;Inc Z8000 Dev Module	ZIL
105▼	Z-UPC-UCS	Z8	IO-13	CHIP		Univer Peripheral Controller;3-8-Line I/O Ports;2k Bytes Inter ROM	ZIL
106	Z8034UPC	Z8	IO-30	Chip		Control by ROM-resident Internal SW;Data Manipulation;Data Buffering	ZIL
107	Z8060FIFO	Z8	IO-33	Chip		128 x 8;Extends Depth of Z-FIO w/o Limit;3-Stute Data Outputs	ZIL
108▼	Z6132-3CS	Z8,Z8000	RAM	CHIP	MNG	Conforms w/Z-Bus Spec;4096x8 Bits;Access Time 200ns;Cycle Time 350ns	ZIL
109▼	Z6132-3PS	Z8,Z8000	RAM	CHIP	MNG	Conforms w/Z-Bus;Spec;4096x8 Bits;Access Time 200ns;Cycle Time 350ns	ZIL
110▼	Z6132-4CS	Z8,Z8000	RAM	CHIP	MNG	Conforms w/Z-Bus;Spec;4096x8 Bits;Access Time 250ns;Cycle Time 375ns	ZIL

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE
1▼	Z6132-4PS	Z8,Z8000	RAM	CHIP	MNG	Conforms w/Z-Bus;Spec;4096x8 Bits;Access Time 250ns;Cycle Time 375ns	ZIL
2▼	Z6132-5CS	Z8,Z8000	RAM	CHIP	MNG	Conforms w/Z-Bus;Spec;4096x8 Bits;Access Time 300ns;Cycle Time 425ns	ZIL
3▼	Z6132-5PS	Z8,Z8000	RAM	CHIP	MNG	Conforms w/Z-Bus;Spec;4096x8 Bits;Access Time 300ns;Cycle Time 425ns	ZIL
4	Z80-MCB4	Z80	COMP	MOD		Z80 Microcomputer Board Containing 4k Bytes Memory	ZIL
5	Z80-MCB16	Z80	COMP	MOD		Z80 Microcomputer Board Containing 16k Bytes Memory	ZIL
6	Z80-CPUCE	Z80	CPU	Chip	MNG	8 Bit Microprocessor;Clock Freq 2.5MHz Max;Temp -40 To 85°C;Ceramic Pkg	ZIL
7	Z80-CPUCM	Z80	CPU	Chip	MNG	8 Bit Microprocessor;Clock Freq 2.5MHz Max;Temp -55 To 125°C;Cer Pkg	ZIL
8	Z80-CPUCS	Z80	CPU	Chip	MNG	8 Bit Microprocessor;Clock Freq 2.5MHz Max;Temp 0 To 70°C;Ceramic Pkg	ZIL
9	Z80-CPUPS	Z80	CPU	Chip	MNG	8 Bit Microprocessor;Clock Freq 2.5MHz Max;Temp 0 To 70°C;Plastic Pkg	ZIL
10	Z80A-CPUCS	Z80	CPU	Chip	MNG	8 Bit Microprocessor;Clock Freq 4.0MHz Max;Temp 0 To 70°C;Ceramic Pkg	ZIL
11	Z80A-CPUPS	Z80	CPU	Chip	MNG	8 Bit Microprocessor;Clock Freq 4.0MHz Max;Temp 0 To 70°C;Plastic Pkg	ZIL
12	Z80-CTCCS	Z80	IO-01	Chip	MNG	Counter Timer Ckt;Programmable 4 Ch;Clock Period 400ns Min	ZIL
13	Z80A-CTCCS	Z80	IO-01	Chip	MNG	Counter Timer Ckt;Programmable 4 Ch;Clock Period 250ns Min	ZIL
14	Z80ACTCCE	Z80	IO-01	Chip	MNG	Counter Timer Ckt;Programmable 4Ch;Clock Per 250nS Min	ZIL
15	Z80ACTCCM	Z80	IO-01	Chip	MNG	Counter Timer Ckt;Programmable 4Ch;Clock Per 250nS Min	ZIL
16	Z80ACTCPS	Z80	IO-01	Chip	MNG	Counter Timer Ckt;Programmable 4 Ch;Clock Per 250nS Min	ZIL
17	Z80CTCCE	Z80	IO-01	Chip	MNG	Counter Timer Ckt;Programmable 4 Ch;Clock Per 400nS Min	ZIL
18	Z80CTCCM	Z80	IO-01	Chip	MNG	Counter Timer Ckt;Programmable 4 Ch;Clock Per 400nS Min	ZIL
19	Z80CTCPS	Z80	IO-01	Chip	MNG	Counter Timer Ckt;Programmable 4Ch;Clock Per 400nS Min	ZIL
20	Z80-DMACE	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Ch;Ceramic Pkg	ZIL
21	Z80-DMACM	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Ch;Ceramic Pkg	ZIL
22	Z80-DMACS	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Ch;Ceramic Pkg	ZIL
23	Z80-DMAPS	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Ch;Plastic Pkg	ZIL
24	Z80A-DMACS	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Ch;Ceramic Pkg	ZIL
25	Z80A-DMAPS	Z80	IO-03	Chip	MNG	Direct Memory Access Ckt;Programmable 1 Ch;Plastic Pkg	ZIL
26♦	Z80-SIO/0CE	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
27♦	Z80-SIO/0CM	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
28♦	Z80-SIO/0CS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
29♦	Z80-SIO/0PS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
30♦	Z80-SIO/1CE	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
31♦	Z80-SIO/1CM	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
32♦	Z80-SIO/1CS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
33♦	Z80-SIO/1PS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
34♦	Z80-SIO/2CE	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
35♦	Z80-SIO/2CM	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
36♦	Z80-SIO/2CS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
37♦	Z80-SIO/2PS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
38	Z80A-SIO/0CE	Z80	IO-20	Chip	MNG	Dual Ch Programmable I/O;-40 to 85°C/Cer Pkg;Clock 250kHz-4.0MHz	ZIL
39♦	Z80A-SIO/0CM	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
40♦	Z80A-SIO/0CS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
41♦	Z80A-SIO/0PS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
42♦	Z80A-SIO/1CE	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
43♦	Z80A-SIO/1CM	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
44♦	Z80A-SIO/1CS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Programmable I/O	ZIL
45♦	Z80A-SIO/1PS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
46♦	Z80A-SIO/2CE	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
47♦	Z80A-SIO/2CM	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
48♦	Z80A-SIO/2CS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Programmable I/O	ZIL
49♦	Z80A-SIO/2PS	Z80	IO-20	Chip	MNG	Serial In/Output Controller;Dual Channel Programmable I/O	ZIL
50	Z80A-SIO/9CE	Z80	IO-20	Chip	MNG	Dual Ch Programmable I/O;-40 to 85°C/Cer Pkg;Clock 250KHz-4.0MHz	ZIL
51	Z80A-SIO/9CM	Z80	IO-20	Chip	MNG	Dual Ch Programmable I/O;-55 to 125°C/Cer Pkg;Clock 250KHz-4.0MHz	ZIL
52♦	Z80A-SIO/9CS	Z80	IO-20	Chip	MNG	Serial In/Output Contoller;Single Channel Multi-Function Peripheral	ZIL
53♦	Z80A-SIO/9PS	Z80	IO-20	Chip	MNG	Serial In/Output Contoller;Single Channel Multi-Function Peripheral	ZIL
54♦	Z80SIO/9CS	Z80	IO-20	Chip	MNG	Serial In/Output Contoller;Single Channel Multi-Function Peripheral	ZIL
55♦	Z80SIO/9PS	Z80	IO-20	Chip	MNG	Serial In/Output Contoller;Single Channel Multi-Function Peripheral	ZIL
56	Z80-PIOCE	Z80	IO-30	Chip	MNG	Parallel I/O Interface Controller;Programmable 2 Port;Ceramic Pkg	ZIL
57	Z80-PIOCM	Z80	IO-30	Chip	MNG	Parallel I/O Interface Controller;Programmable 2 Port;Ceramic Pkg	ZIL
58	Z80-PIOCS	Z80	IO-30	Chip	MNG	Parallel I/O Interface Controller;Programmable 2 Port;Ceramic Pkg	ZIL
59	Z80-PIOPS	Z80	IO-30	Chip	MNG	Parallel I/O Interface Controller;Programmable 2 Port;Plastic Pkg	ZIL
60	Z80A-PIOCE	Z80	IO-30	Chip	MNG	Parallel I/O Interface Controller;Programmable 2 Port;Ceramic Pkg	ZIL
61	Z80A-PIOCM	Z80	IO-30	Chip	MNG	Parallel I/O Interface Controller;Programmable 2 Port;Ceramic Pkg	ZIL
62	Z80A-PIOCS	Z80	IO-30	Chip	MNG	Parallel I/O Interface Controller;Programmable 2 Port;Ceramic Pkg	ZIL
63	Z80A-PIOPS	Z80	IO-30	Chip	MNG	Parallel I/O Interface Controller;Programmable 2 Port;Plastic Pkg	ZIL
64	Z80ADARTCE	Z80	IO-33	Chip	MNG	2 Independent Full-Duplex chs w/Sep Modem Controls;40 Pin Ceramic Dip	ZIL
65	Z80ADARTCM	Z80	IO-33	Chip	MNG	2 Independent Full-Duplex chs w/Sep Modem Controls;40 Pin Ceramic Dip	ZIL
66	Z80ADARTCS	Z80	IO-33	Chip	MNG	2 Independent Full-Duplex chs w/Sep Modem Controls;40 Pin Ceramic Dip	ZIL
67	Z80ADARTPS	Z80	IO-33	Chip	MNG	2 Independent Full-Duplex chs w/Sep Modem Controls;40 Pin Plastic Dip	ZIL
68	Z80DARTCE	Z80	IO-33	Chip	MNG	2 Independent Full-Duplex chs w/Sep Modem Controls;40 Pin Ceramic Dip	ZIL
69	Z80DARTCM	Z80	IO-33	Chip	MNG	2 Independent Full-Duplex chs w/Sep Modem Controls;40 Pin Ceramic Dip	ZIL
70	Z80DARTCS	Z80	IO-33	Chip	MNG	2 Independent Full-Duplex chs w/Sep Modem Controls;40 Pin Ceramic Dip	ZIL
71	Z80DARTPS	Z80	IO-33	Chip	MNG	2 Independent Full-Duplex chs w/Sep Modem Controls;40 Pin Plastic Dip	ZIL
72▼	Z80RMB	Z80	IO-57	MOD		RAM/ROM Memory Bd;16k/32k/64k Dyn RAM;8k Bytes ROM,RAM/EPROM	ZIL
73	Z6104-3CS	Z80	RAM	Chip	MNG	4096x1 Static RAM;Access Time 200ns Max;Ceramic Pkg	ZIL
74	Z6104-5CS	Z80	RAM	Chip	MNG	4096x1 Static RAM;Access Time 300ns Max;Ceramic Pkg	ZIL
75	Z6104-5PS	Z80	RAM	Chip	MNG	4096x1 Static RAM;Access Time 300ns Max;Plastic Pkg	ZIL
76	Z6104-6CS	Z80	RAM	Chip	MNG	4096x1 Static RAM;Access Time 350ns max;Ceramic Pkg	ZIL
77	Z80-MCB	Z80-MCS	COMP	MOD		8-Bit Single Bd Comp;Z80-CPU,Z80-CTC,Z80-PIO,4k Bytes RAM,4k Bytes ROM	ZIL
78	Z80A-MPB	Z80-MCS	CPU	MOD	MNG	8-Bit,4MHz System;Z80A-CPU,Z80A-SIO,Z80A-PIO,Z80A-CTC,Z80A-DMA	ZIL
79	Z80A-FDC	Z80-MCS	IO-07	MOD		8-Bit,4MHz System Disk Contr;Interface to Shugart 400,450,800,850 Drives	ZIL
80	Z80-SIB	Z80-MCS	IO-20	MOD		Serial I/O Board;Provides 4 Serial Full Duplex Channels	ZIL
81	Z80-IOB	Z80-MCS	IO-30	MOD		Input/Output Board;Interface W/64 Progm Data Lines and 16 Controls	ZIL
82	Z80-AIB	Z80-MCS	IO-41	MOD		Analog Input Board;32 Single Ended Analog Inputs,Single 5V PS	ZIL
83	Z80-AIBN	Z80-MCS	IO-41	MOD		Analog Input Board;32 Single Ended Analog Inputs,2 PS 5V,±15V	ZIL
84	Z80-AIO	Z80-MCS	IO-42	MOD		Analog Input-Output Board;32 Analog Input,2 Analog Outputs	ZIL
85	Z80-AION	Z80-MCS	IO-42	MOD		Analog Input-Output Board;2 Power Supplies Required 5.0V, ±15V	ZIL
86	Z80-MDC	Z80-MCS	IO-57	MOD		Mem/Disk Controller Board	ZIL
87	Z80-PMB	Z80-MCS	PROM	MOD		PROM Memory Board;5V Power Supply;16 Sockets for 32k Bytes ROM/PROM	ZIL
88	Z80-PPB	Z80-MCS	PROM	MOD		PROM Programmer Board;For Use W/EPROMs and PROMs	ZIL
89	Z80-PPB/16	Z80-MCS	PROM	MOD		PROM Programmer Board;For Use W/2716 EPROMs and 82S181 PROMs	ZIL
90	Z80A-RRM	Z80-MCS	RAM	MOD		8-Bit,4MHz System;16k x 1 Dyn RAM;Sockets for 64k Bytes RAM,8k Bytes ROM	ZIL
91	Z80-KBD	Z80-PDS	DEV	MOD		Keyboard Module for Use With Z80-VDB	ZIL
92	Z80-VDB	Z80-PDS	DEV	MOD		Video Display Board;Interfaces to Video Monitor and Keyboard	ZIL
93	Z8001CPU	Z8000	CPU	Chip	MNX	Segmented 48 Pin;16/16 Bit Gen-Purpose Registers;414 Instruction Set	ZIL
94	Z8002CPU	Z8000	CPU	Chip	MNX	Non-Segmented 40 Pin;16/16 Bit Gen-Purpose Registers;414 Instruction Set	ZIL
95	Z8030SCC	Z8000	IO-02	Chip		Dual Ch,Multi-Protocol Data Comunication Peripheral for Z-bus Use;40 Pin	ZIL
96	Z8036CIO	Z8000	IO-33	Chip	MNX	Contains 3 I/O Ports and 3 Counter/Timers;Z-bus Compatible;40 Pin Pkg	ZIL
97	Z8038FIO	Z8000	IO-33	Chip		128 x 8,Expandable to 16 Bits; Cascadable to Any Depth;40 Pin Pkg	ZIL
98▼	Z-FIOCS	Z8000	IO-92	CHIP		FIFO In/Out Interface Unit;Interlock/IEEE-48 Handshake Port Mode	ZIL
99▼	Z-FIOPS	Z8000	IO-92	CHIP		FIFO In/Out Interface Unit;Interlock/IEEE-48 Handshake Port Mode	ZIL
100▼	Z-UPC-UPS	Z8	IO-13	CHIP		Univer Peripheral Controller;3ZIL r Peripheral Controller;3er ROM	ZIOL

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D.
(3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	[4] SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	[2] GENERIC I.D. $-MULTI-SYSTEM APPLICATION	[3] SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	[1] MFR. CODE
1	SW-QJ713-AQ	LSI11	LSI11	OPS	RT-11 FMS-11 DECpack(RL01)SuppDEC FMS-11 DECpack(RL01)Supp	
2	SW-MACRO8/8000	Z8000	Z8000	ASB	Macroassembler for Z8000 ProgrAuC assembler for Z8000 Progr	ams
3	SW-AmSYS-BASIC	Z80	AmSYS8/8	LAN	BASIC for AmSYS8/8 User	AuC
4	SW-AmSYS-COBOL	Z80	AmSYS8/8	LAN	PROM Programmer	AuC
5	SW-AmSYS-PASCAL	Z80	AmSYS8/8	LAN	PASCAL to AmSYS8/8	AuC
6	SW-AMDOS8/8	Z80	AmSYS8/8	DOS	Disk Operating System;Access to File Mgmt System	AuC
7	SW-DEBUG8/8	Z80	AmSYS8/8	DEB	Program Debugger for AmSYS8/8;Contains Debug Nucleus, Assy/DisAssy Mod	AuC
8	SW-LINK8/8	Z80	AmSYS8/8	SUB	Relocatable Linkage Editor;Processes Object Files	AuC
9	SW-EDIT8/8	Z80$	AmSYS8/8	EDT	Line Oriented Editor for 8080/8085/Z80/Z8000 Microprocessors	AuC
10	SW-LIBR8/8	Z80$	AmSYS8/8	SUB	Object File Library for 8080/8085/Z80	AuC
11	SW-MACRO8/8	Z80$	AmSYS8/8	ASB	Macroassembler;Assembles Relocatable 8080/8085/Z80 Programs	AuC
12	SW-TRANS-8000	Z80$	AmSYS8/8	ASB	Translator for Z8000 Processor;Accepts 8080/8085/Z80 In for Z8000 Out	AuC
13	SW-AMDASM/29	2901	SYSTEM29	ASB	2 Pass Microprogram Assembler Used to Convert Formats into Machine Lan	AuC
14	SW-AMPARITY/29	2901	SYSTEM29	SSS	Post Processing Program to Generate One or More Parity Bits on Microco	AuC
15	SW-AMPROM/29	2901	SYSTEM29	SSS	Post Processing Program to Output Binary Object Codes to Corres;W/PROM	AuC
16	SW-AMSCRM/29	2901	SYSTEM29	SSS	Post Processing Program to Reorganize Columns of Microcode to PROM	AuC
17	SW-AMC95/MON	95/4000$	95/4000$	MON	TTY-Monitor Memory Inspection,Modification Loading Execution and Debug	AuC
18▼	SW-Am95/4620	AmZ8000	Am95/4005	MON	Real Time Multi-tasking Exec;PROM Based;for use w/Non-disk Based Sys	AMD
19▼	SW-Am95/4622	AmZ8000	Am95/4005	MON	Real Time Multi-tasking Exec;PROM Based;Inc Disk File Mgr	AMD
20▼	SW-Am95/4624	AmZ8000	Am95/4005	MON	Real Time Multi-tasking Exec;RAM Based;Inc Disk File Mgr	AMD
21▼	SW-AmSYSMACROZ8000	AmZ8000	Z8000	ASB	16 Bit Macroassembler;w/Relocatable Output and Linker	AMD
22▼	SW-8/8440	AmZ9000$	AmSYS8/8	CMP	AMC PASCAL Compiler,w/Interpreter,Run-Time Lib,Am9080/Z8000 Code Gen	AMD
23▼	SW-298450	AmZ9000$	AmSYS8/8	ASB	16 Bit Macroassembler;8080,8085 and 8 Bit Assemblers	AMD
24▼	SW-AMI-CROSS	S2200,8080$	S6800,S9900	CMP	Cross Support for Common Software Base	AMI
25▼	SW-AMI-PASCAL	S2200,8080$	S6800,S9900	CMP	Complete System;Stand Alone Micro/Minicomputer;Compat w/UCSD PASCAL	AMI
26▼	SW-STB-L	Z80	Z2,CS3	LAN	32K Structured Basic;Keyed Sequential Access Method;Structured Prog.	AMI
27	SW-S2000AP	2000	S2000	ASB	Disk Resident Assembler;Source Progr and MACRO Library File Inputs	AMI
28	SW-S2000DB	2000	S2000	DEB	Debug Progr;Allows Single Control W/DISPLAY,SET,REMOVE,Execute Comm	AMI
29	SW-S2000LD	2000	S2000	LOA	Resident Loader Used with MDC-100 Dev Unit,S2000 Emulator and Debug Pr	AMI
30	SW-S6800#1	6800	S6800	ASB	Cross Assembler;ANSI FORTRAN IV,IBM 360/370 BAL;NCSS Timesharing	AMI
31	SW-S6800#2	6800	S6800	LOA	Relocating Loader;ANSI FORTRAN IV,IBM 360/370 BAL;NCSS Timesharing	AMI
32	SW-S6800#3	6800	S6800	SIM	Simulator;ANSI FORTRAN IV,IBM 360/370 BAL;NCSS Timesharing	AMI
33	SW-AMDASM/80-D	2901	Am2900	ASB	Micro Program Assembler-Runs on Intellec System;Dual Density Floppy	AMV
34	SW-AMDASM/80-S	2901	Am2900	ASB	Micro Program Assembler-Runs on Intellec System-Single Density Floppy	AMV
35	SW-AMDASM	2901	AM2900	ASB	AMDAS Fortran Microcomputer Assembler	AMV
36	SW-Am9080A	9080A	Am9080A	SSS	Intel 8080,Software Support	AMV
37	SW-MicroDOS/BASIC	8080	EVENTSERIES	OPS	Operating Syst;MicroDOS/BASIC,An Extended Version of Basic Language	APP
38	SW-MicroEXEC	8080	EVENTSERIES	MON	Machine Language Software;Editor/Assembler,Debug,Program Execution	APP
39	SW-70S10	8080	70-100	MFS	Software Development Program,Includes Editor,Assemb,Debug/Subroutines	APP
40	SW-70S11	8080	70-100	LAN	Basic on Floppy Disk;Extended BASIC	APP
41	SW-70S12	8080	70-100	CMP	Disk Resident Program Compiler;FORTRAN	APP
42	SW-70S21	8080	70-100	SSS	System and Communication Protocol Operation;IBM 2780	APP
43	SW-70S232-1▼	8080	70-100	LOA	Firmware RS232 Program	APP
44	SW-70S232-2▼	8080	70-100	LOA	Firmware RS232 Program	APP
45	SW-ASC80#1	8080	ASC80	ASB	Resident Assembler	APS
46	SW-ASC80#2	8080	ASC80	EDT	Text Editor/Monitor	APS
47	SW-ASC80#3	8080	ASC80	SSS	Data Communications Utilities	APS
48	SW-ASC80#4	8080	ASC80	SIM	Programmable Controller Emulator	APS
49	SW-ASC80#5	8080	ASC80	ASB	Cross Assembler	APS
50	SW-ASC80#6	8080	ASC80	SIM	Simulator	APS
51	SW-ASC80#7	8080	ASC80	CMP	PL/M Cross Compiler	APS
52	SW-CAF8/10,20,PDP	F8	F8	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
53	SW-CAF8/DGC	F8	F8	ASB	Abs Cross Assembler For Data General Host Computer	BSO
54	SW-CFF8/10,20,PDP	F8	F8	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
55	SW-CFF8/DGC	F8	F8	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
56	SW-CPF8/10,20,PDP	F8	F8	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
57	SW-CPF8/DGC	F8	F8	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
58	SW-CRF8/10,20,PDP	F8	F8	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
59	SW-CRF8/DGC	F8	F8	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
60	SW-CXF8/10,20,PDP	F8	F8	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
61	SW-CXF8/DGC	F8	F8	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
62	SW-CYF8/10,20,PDP	F8	F8	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
63	SW-CYF8/DGC	F8	F8	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
64	SW-SIF8/10,20,PDP	F8	F8	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
65	SW-SIF8/DGC	F8	F8	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
66	SW-CAIMP8/DGC	IMP8	IMP8	ASB	Abs Cross Assembler For Data General Host Computer	BSO
67	SW-CAIMP8/10,20,PDP	IMP8	IMP8	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
68	SW-CFIMP8/DGC	IMP8	IMP8	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
69	SW-CFIMP8/10,20,PDP	IMP8	IMP8	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
70	SW-CPIMP8/DGC	IMP8	IMP8	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
71	SW-CPIMP8/10,20,PDP	IMP8	IMP8	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
72	SW-CRIMP8/DGC	IMP8	IMP8	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
73	SW-CRIMP8/10,20,PDP	IMP8	IMP8	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
74	SW-CXIMP8/DGC	IMP8	IMP8	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
75	SW-CXIMP8/10,20,PDP	IMP8	IMP8	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
76	SW-CYIMP8/DGC	IMP8	IMP8	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
77	SW-CYIMP8/10,20,PDP	IMP8	IMP8	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
78	SW-SIIMP8/DGC	IMP8	IMP8	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
79	SW-SIIMP8/10,20,PDP	IMP8	IMP8	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
80	SW-CAIM16/DGC	IM16	IMP16	ASB	Abs Cross Assembler For Data General Host Computer	BSO
81	SW-CAIM16/10,20,PDP	IM16	IMP16	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
82	SW-CFIM16/DGC	IM16	IMP16	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
83	SW-CFIM16/10,20,PDP	IM16	IMP16	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
84	SW-CPIM16/DGC	IM16	IMP16	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
85	SW-CPIM16/10,20,PDP	IM16	IMP16	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
86	SW-CRIM16/DGC	IM16	IMP16	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
87	SW-CRIM16/10,20,PDP	IM16	IMP16	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
88	SW-CXIM16/DGC	IM16	IMP16	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
89	SW-CXIM16/10,20,PDP	IM16	IMP16	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
90	SW-CYIM16/DGC	IM16	IMP16	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
91	SW-CYIM16/10,20,PDP	IM16	IMP16	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
92	SW-SIIM16/DGC	IM16	IMP16	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
93	SW-SIIM16/10,20,PDP	IM16	IMP16	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
94	SW-CAPACE/10,20,PDP	PACE	IPC16	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
95	SW-CAPACE/DGC	PACE	IPC16	ASB	Abs Cross Assembler For Data General Host Computer	BSO
96	SW-CFPACE/10,20,PDP	PACE	IPC16	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
97	SW-CFPACE/DGC	PACE	IPC16	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
98	SW-CPPACE/10,20,PDP	PACE	IPC16	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
99	SW-CPPACE/DGC	PACE	IPC16	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
100	SW-CRPACE/10,20,PDP	PACE	IPC16	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
101	SW-CRPACE/DGC	PACE	IPC16	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
102	SW-CXPACE/10,20,PDP	PACE	IPC16	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
103	SW-CXPACE/DGC	PACE	IPC16	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
104	SW-CYPACE/10,20,PDP	PACE	IPC16	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
105	SW-CYPACE/DGC	PACE	IPC16	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
106	SW-SIPACE/10,20,PDP	PACE	IPC16	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
107	SW-SIPACE/DGC	PACE	IPC16	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
108	SW-CAPPS4/DGC	PPS4	PPS4	ASB	Abs Cross Assembler For Data General Host Computer	BSO
109	SW-CAPPS4/10,20,PDP	PPS4	PPS4	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
110	SW-CFPPS4/DGC	PPS4	PPS4	CMP	Fortran Cross Compiler For Data General Host Computer	BSO

SYMBOLS AND CODES
EXPLAINED IN INTERPRETER

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	1 MFR. CODE
1	SW-CFPPS4/10,20,PDP	PPS4	PPS4	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
2	SW-CPPPS4/DGC	PPS4	PPS4	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
3	SW-CPPPS4/10,20,PDP	PPS4	PPS4	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
4	SW-CRPPS4/DGC	PPS4	PPS4	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
5	SW-CRPPS4/10,20,PDP	PPS4	PPS4	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
6	SW-CXPPS4/DGC	PPS4	PPS4	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
7	SW-CXPPS4/10,20,PDP	PPS4	PPS4	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
8	SW-CYPPS4/DGC	PPS4	PPS4	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
9	SW-CYPPS4/10,20,PDP	PPS4	PPS4	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
10	SW-SIPPS4/DGC	PPS4	PPS4	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
11	SW-SIPPS4/10,20,PDP	PPS4	PPS4	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
12	SW-CAPPS8/DGC	PPS8	PPS8	ASB	Abs Cross Assembler For Data General Host Computer	BSO
13	SW-CAPPS8/10,20,PDP	PPS8	PPS8	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
14	SW-CFPPS8/DGC	PPS8	PPS8	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
15	SW-CFPPS8/10,20,PDP	PPS8	PPS8	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
16	SW-CPPPS8/DGC	PPS8	PPS8	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
17	SW-CPPPS8/10,20,PDP	PPS8	PPS8	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
18	SW-CRPPS8/DGC	PPS8	PPS8	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
19	SW-CRPPS8/10,20,PDP	PPS8	PPS8	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
20	SW-CXPPS8/DGC	PPS8	PPS8	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
21	SW-CXPPS8/10,20,PDP	PPS8	PPS8	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
22	SW-CYPPS8/DGC	PPS8	PPS8	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
23	SW-CYPPS8/10,20,PDP	PPS8	PPS8	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
24	SW-SIPPS8/DGC	PPS8	PPS8	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
25	SW-SIPPS8/10,20,PDP	PPS8	PPS8	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
26	SW-CASCMP/10,20,PDP	SC/MP	SC/MP	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
27	SW-CASCMP/DGC	SC/MP	SC/MP	ASB	Abs Cross Assembler For Data General Host Computer	BSO
28	SW-CFSCMP/10,20,PDP	SC/MP	SC/MP	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
29	SW-CFSCMP/DGC	SC/MP	SC/MP	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
30	SW-CPSCMP/10,20,PDP	SC/MP	SC/MP	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
31	SW-CPSCMP/DGC	SC/MP	SC/MP	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
32	SW-CRSCMP/10,20,PDP	SC/MP	SC/MP	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
33	SW-CRSCMP/DGC	SC/MP	SC/MP	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
34	SW-CXSCMP/10,20,PDP	SC/MP	SC/MP	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
35	SW-CXSCMP/DGC	SC/MP	SC/MP	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
36	SW-CYSCMP/10,20,PDP	SC/MP	SC/MP	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
37	SW-CYSCMP/DGC	SC/MP	SC/MP	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
38	SW-SISCMP/10,20,PDP	SC/MP	SC/MP	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
39	SW-SISCMP/DGC	SC/MP	SC/MP	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
40	SW-CAZ80/10,20,PDP	Z80	Z80	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
41	SW-CFZ80/10,20,PDP	Z80	Z80	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
42	SW-CFZ80/DGC	Z80	Z80	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
43	SW-CPZ80/10,20,PDP	Z80	Z80	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
44	SW-CPZ80/DGC	Z80	Z80	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
45	SW-CRZ80/10,20,PDP	Z80	Z80	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
46	SW-CRZ80/DGC	Z80	Z80	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
47	SW-CXZ80/10,20,PDP	Z80	Z80	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
48	SW-CXZ80/DGC	Z80	Z80	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
49	SW-CYZ80/10,20,PDP	Z80	Z80	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
50	SW-CYZ80/DGC	Z80	Z80	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
51	SW-SIZ80/10,20,PDP	Z80	Z80	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
52	SW-SIZ80/DGC	Z80	Z80	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
53	SW-CF1000/10,20,PDP	1000	TMS1000	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
54	SW-CF1000/DGC	1000	TMS1000	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
55	SW-CP1000/10,20,PDP	1000	TMS1000	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
56	SW-CP1000/DGC	1000	TMS1000	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
57	SW-CR1000/10,20,PDP	1000	TMS1000	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
58	SW-CR1000/DGC	1000	TMS1000	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
59	SW-CX1000/10,20,PDP	1000	TMS1000	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
60	SW-CX1000/DGC	1000	TMS1000	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
61	SW-CY1000/10,20,PDP	1000	TMS1000	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
62	SW-CY1000/DGC	1000	TMS1000	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
63	SW-SI1000/10,20,PDP	1000	TMS1000	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
64	SW-SI1000/DGC	1000	TMS1000	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
65	SW-CF1800/10,20,PDP	1800	UC1800	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
66	SW-CF1800/DGC	1800	UC1800	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
67	SW-CP1800/10,20,PDP	1800	UC1800	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
68	SW-CP1800/DGC	1800	UC1800	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
69	SW-CR1800/10,20,PDP	1800	UC1800	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
70	SW-CR1800/DGC	1800	UC1800	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
71	SW-CX1800/10,20,PDP	1800	UC1800	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
72	SW-CX1800/DGC	1800	UC1800	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
73	SW-CY1800/10,20,PDP	1800	UC1800	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
74	SW-CY1800/DGC	1800	UC1800	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
75	SW-SI1800/10,20,PDP	1800	UC1800	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
76	SW-SI1800/DGC	1800	UC1800	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
77	SW-CF1802/10,20,PDP	1802	CDP1800	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
78	SW-CF1802/DGC	1802	CDP1800	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
79	SW-CP1802/10,20,PDP	1802	CDP1800	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
80	SW-CP1802/DGC	1802	CDP1800	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
81	SW-CR1802/10,20,PDP	1802	CDP1800	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
82	SW-CR1802/DGC	1802	CDP1800	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
83	SW-CX1802/10,20,PDP	1802	CDP1800	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
84	SW-CX1802/DGC	1802	CDP1800	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
85	SW-CY1802/10,20,PDP	1802	CDP1800	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
86	SW-CY1802/DGC	1802	CDP1800	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
87	SW-SI1802/10,20,PDP	1802	CDP1800	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
88	SW-SI1802/DGC	1802	CDP1800	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
89	SW-CF1804/10,20,PDP	1804	CDP1800	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
90	SW-CF1804/DGC	1804	CDP1800	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
91	SW-CP1804/10,20,PDP	1804	CDP1800	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
92	SW-CP1804/DGC	1804	CDP1800	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
93	SW-CR1804/10,20,PDP	1804	CDP1800	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
94	SW-CR1804/DGC	1804	CDP1800	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
95	SW-CX1804/10,20,PDP	1804	CDP1800	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
96	SW-CX1804/DGC	1804	CDP1800	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
97	SW-CY1804/10,20,PDP	1804	CDP1800	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
98	SW-CY1804/DGC	1804	CDP1800	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
99	SW-SI1804/10,20,PDP	1804	CDP1800	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
100	SW-SI1804/DGC	1804	CDP1800	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
101	SW-CF2000/10,20,PDP	2000	S2000	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
102	SW-CF2000/DGC	2000	S2000	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
103	SW-CP2000/10,20,PDP	2000	S2000	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
104	SW-CP2000/DGC	2000	S2000	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
105	SW-CR2000/10,20,PDP	2000	S2000	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
106	SW-CR2000/DGC	2000	S2000	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
107	SW-CX2000/10,20,PDP	2000	S2000	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
108	SW-CX2000/DGC	2000	S2000	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
109	SW-CY2000/10,20,PDP	2000	S2000	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
110	SW-CY2000/DGC	2000	S2000	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	[4] SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	[2] GENERIC I.D. $-MULTI-SYSTEM APPLICATION	[3] SYSTEM TYPE No.	CATEGORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	[1] MFR. CODE
1	SW-SI2000/10,20,PDP	2000	S2000	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
2	SW-SI2000/DGC	2000	S2000	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
3	SW-CF3870/10,20,PDP	3870	MC3870	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
4	SW-CF3870/DGC	3870	MC3870	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
5	SW-CP3870/10,20,PDP	3870	MC3870	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
6	SW-CP3870/DGC	3870	MC3870	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
7	SW-CR3870/10,20,PDP	3870	MC3870	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
8	SW-CR3870/DGC	3870	MC3870	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
9	SW-CX3870/10,20,PDP	3870	MC3870	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
10	SW-CX3870/DGC	3870	MC3870	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
11	SW-CY3870/10,20,PDP	3870	MC3870	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
12	SW-CY3870/DGC	3870	MC3870	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
13	SW-SI3870/10,20,PDP	3870	MC3870	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
14	SW-SI3870/DGC	3870	MC3870	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
15	SW-CF4004/10,20,PDP	4004	MCS4	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
16	SW-CF4004/DGC	4004	MCS4	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
17	SW-CP4004/10,20,PDP	4004	MCS4	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
18	SW-CP4004/DGC	4004	MCS4	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
19	SW-CR4004/10,20,PDP	4004	MCS4	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
20	SW-CR4004/DGC	4004	MCS4	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
21	SW-CX4004/10,20,PDP	4004	MCS4	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
22	SW-CX4004/DGC	4004	MCS4	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
23	SW-CY4004/10,20,PDP	4004	MCS4	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
24	SW-CY4004/DGC	4004	MCS4	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
25	SW-SI4004/10,20,PDP	4004	MCS4	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
26	SW-SI4004/DGC	4004	MCS4	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
27	SW-CF4040/10,20,PDP	4040	MCS40	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
28	SW-CF4040/DGC	4040	MCS40	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
29	SW-CP4040/10,20,PDP	4040	MCS40	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
30	SW-CP4040/DGC	4040	MCS40	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
31	SW-CR4040/10,20,PDP	4040	MCS40	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
32	SW-CR4040/DGC	4040	MCS40	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
33	SW-CX4040/10,20,PDP	4040	MCS40	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
34	SW-CX4040/DGC	4040	MCS40	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
35	SW-CY4040/10,20,PDP	4040	MCS40	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
36	SW-CY4040/DGC	4040	MCS40	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
37	SW-SI4040/10,20,PDP	4040	MCS40	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
38	SW-SI4040/DGC	4040	MCS40	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
39	SW-CF6500/10,20,PDP	6500	SY6500	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
40	SW-CF6500/DGC	6500	SY6500	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
41	SW-CP6500/10,20,PDP	6500	SY6500	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
42	SW-CP6500/DGC	6500	SY6500	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
43	SW-CR6500/10,20,PDP	6500	SY6500	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
44	SW-CR6500/DGC	6500	SY6500	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
45	SW-CX6500/10,20,PDP	6500	SY6500	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
46	SW-CX6500/DGC	6500	SY6500	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
47	SW-CY6500/10,20,PDP	6500	SY6500	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
48	SW-CY6500/DGC	6500	SY6500	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
49	SW-SI6500/10,20,PDP	6500	SY6500	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
50	SW-SI6500/DGC	6500	SY6500	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
51	SW-CF6800/10,20,PDP	6800	M6800	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
52	SW-CF6800/DGC	6800	M6800	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
53	SW-CP6800/10,20,PDP	6800	M6800	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
54	SW-CP6800/DGC	6800	M6800	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
55	SW-CR6800/10,20,PDP	6800	M6800	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
56	SW-CR6800/DGC	6800	M6800	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
57	SW-CX6800/10,20,PDP	6800	M6800	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
58	SW-CX6800/DGC	6800	M6800	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
59	SW-CY6800/10,20,PDP	6800	M6800	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
60	SW-CY6800/DGC	6800	M6800	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
61	SW-SI6800/10,20,PDP	6800	M6800	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
62	SW-SI6800/DGC	6800	M6800	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
63	SW-CA6801/10,20,PDP	6801	MC6801	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
64	SW-CA6801/DGC	6801	MC6801	ASB	Abs Cross Assembler For Data General Host Computer	BSO
65	SW-CF6801/10,20,PDP	6801	MC6801	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
66	SW-CF6801/DGC	6801	MC6801	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
67	SW-CP6801/10,20,PDP	6801	MC6801	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
68	SW-CP6801/DGC	6801	MC6801	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
69	SW-CR6801/10,20,PDP	6801	MC6801	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
70	SW-CR6801/DGC	6801	MC6801	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
71	SW-CX6801/10,20,PDP	6801	MC6801	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
72	SW-CX6801/DGC	6801	MC6801	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
73	SW-CY6801/10,20,PDP	6801	MC6801	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
74	SW-CY6801/DGC	6801	MC6801	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
75	SW-SI6801/10,20,PDP	6801	MC6801	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
76	SW-SI6801/DGC	6801	MC6801	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
77	SW-CA6802/10,20,PDP	6802	MC6802	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
78	SW-CA6802/DGC	6802	MS6802	ASB	Abs Cross Assembler For Data General Host Computer	BSO
79	SW-CF6802/10,20,PDP	6802	MS6802	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
80	SW-CF6802/DGC	6802	MS6802	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
81	SW-CP6802/10,20,PDP	6802	MS6802	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
82	SW-CP6802/DGC	6802	MS6802	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
83	SW-CR6802/10,20,PDP	6802	MS6802	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
84	SW-CR6802/DGC	6802	MS6802	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
85	SW-CX6802/10,20,PDP	6802	MS6802	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
86	SW-CX6802/DGC	6802	MS6802	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
87	SW-CY6802/10,20,PDP	6802	MS6802	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
88	SW-CY6802/DGC	6802	MS6802	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
89	SW-SI6802/10,20,PDP	6802	MS6802	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
90	SW-SI6802/DGC	6802	MS6802	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
91	SW-CA6809/10,20,PDP	6809	MC6809	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
92	SW-CA6809/DGC	6809	MC6809	ASB	Abs Cross Assembler For Data General Host Computer	BSO
93	SW-CF6809/10,20,PDP	6809	MC6809	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
94	SW-CF6809/DGC	6809	MC6809	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
95	SW-CP6809/10,20,PDP	6809	MC6809	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
96	SW-CP6809/DGC	6809	MC6809	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
97	SW-CR6809/10,20,PDP	6809	MC6809	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
98	SW-CR6809/DGC	6809	MC6809	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
99	SW-CX6809/10,20,PDP	6809	MC6809	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
100	SW-CX6809/DGC	6809	MC6809	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
101	SW-CY6809/10,20,PDP	6809	MC6809	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
102	SW-CY6809/DGC	6809	MC6809	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
103	SW-SI6809/10,20,PDP	6809	MC6809	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
104	SW-SI6809/DGC	6809	MC6809	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
105	SW-CA8000/10,20,PDP	8000	LP8000	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
106	SW-CA8000/DGC	8000	LP8000	ASB	Abs Cross Assembler For Data General Host Computer	BSO
107	SW-CF8000/10,20,PDP	8000	LP8000	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
108	SW-CF8000/DGC	8000	LP8000	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
109	SW-CP8000/10,20,PDP	8000	LP8000	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
110	SW-CP8000/DGC	8000	LP8000	CMP	Pascal Cross Compiler For Data General Host Computer	BSO

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	[4] SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	[2] GENERIC I.D. $-MULTI-SYSTEM APPLICATION	[3] SYSTEM TYPE No.	CATE-GORY	S O F T W A R E L I B R A R Y NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	[1] MFR. CODE
1	SW-CR8000/10,20,PDP	8000	LP8000	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
2	SW-CR8000/DGC	8000	LP8000	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
3	SW-CX8000/10,20,PDP	8000	LP8000	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
4	SW-CX8000/DGC	8000	LP8000	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
5	SW-CY8000/10,20,PDP	8000	LP8000	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
6	SW-CY8000/DGC	8000	LP8000	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
7	SW-SI8000/10,20,PDP	8000	LP8000	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
8	SW-SI8000/DGC	8000	LP8000	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
9	SW-CA8008/10,20,PDP	8008	MCS8	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
10	SW-CA8008/DGC	8008	MCS8	ASB	Abs Cross Assembler For Data General Host Computer	BSO
11	SW-CF8008/10,20,PDP	8008	MCS8	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
12	SW-CF8008/DGC	8008	MCS8	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
13	SW-CP8008/10,20,PDP	8008	MCS8	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
14	SW-CP8008/DGC	8008	MCS8	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
15	SW-CR8008/10,20,PDP	8008	MCS8	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
16	SW-CR8008/DGC	8008	MCS8	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
17	SW-CX8008/10,20,PDP	8008	MCS8	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
18	SW-CX8008/DGC	8008	MCS8	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
19	SW-CY8008/10,20,PDP	8008	MCS8	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
20	SW-CY8008/DGC	8008	MCS8	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
21	SW-SI8008/10,20,PDP	8008	MCS8	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
22	SW-SI8008/DGC	8008	MCS8	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
23	SW-CA8021/10,20,PDP	8021	MCS48	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
24	SW-CA8021/DGC	8021	MCS48	ASB	Abs Cross Assembler For Data General Host Computer	BSO
25	SW-CF8021/10,20,PDP	8021	MCS48	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
26	SW-CF8021/DGC	8021	MCS48	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
27	SW-CP8021/10,20,PDP	8021	MCS48	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
28	SW-CP8021/DGC	8021	MCS48	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
29	SW-CR8021/10,20,PDP	8021	MCS48	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
30	SW-CR8021/DGC	8021	MCS48	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
31	SW-CX8021/10,20,PDP	8021	MCS48	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
32	SW-CX8021/DGC	8021	MCS48	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
33	SW-CY8021/10,20,PDP	8021	MCS48	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
34	SW-CY8021/DGC	8021	MCS48	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
35	SW-SI8021/10,20,PDP	8021	MCS48	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
36	SW-SI8021/DGC	8021	MCS48	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
37	SW-CA8022/10,20,PDP	8022	CA8022	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
38	SW-CA8022/DGC	8022	CA8022	ASB	Abs Cross Assembler For Data General Host Computer	BSO
39	SW-CF8022/10,20,PDP	8022	CA8022	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
40	SW-CF8022/DGC	8022	CA8022	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
41	SW-CP8022/10,20,PDP	8022	CA8022	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
42	SW-CP8022/DGC	8022	CA8022	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
43	SW-CR8022/10,20,PDP	8022	CA8022	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
44	SW-CR8022/DGC	8022	CA8022	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
45	SW-CX8022/10,20,PDP	8022	CA8022	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
46	SW-CX8022/DGC	8022	CA8022	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
47	SW-CY8022/10,20,PDP	8022	CA8022	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
48	SW-CY8022/DGC	8022	CA8022	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
49	SW-SI8022/10,20,PDP	8022	CA8022	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
50	SW-SI8022/DGC	8022	CA8022	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
51	SW-CA8035/10,20,PDP	8035	MCS48	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
52	SW-CA8035/DGC	8035	MCS48	ASB	Abs Cross Assembler For Data General Host Computer	BSO
53	SW-CF8035/10,20,PDP	8035	MCS48	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
54	SW-CF8035/DGC	8035	MCS48	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
55	SW-CP8035/10,20,PDP	8035	MCS48	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
56	SW-CP8035/DGC	8035	MCS48	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
57	SW-CR8035/10,20,PDP	8035	MCS48	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
58	SW-CR8035/DGC	8035	MCS48	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
59	SW-CX8035/10,20,PDP	8035	MCS48	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
60	SW-CX8035/DGC	8035	MCS48	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
61	SW-CY8035/10,20,PDP	8035	MCS48	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
62	SW-CY8035/DGC	8035	MCS48	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
63	SW-SI8035/10,20,PDP	8035	MCS48	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
64	SW-SI8035/DGC	8035	MCS48	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
65	SW-CA8039/10,20,PDP	8039	uCOMP-8	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
66	SW-CA8039/DGC	8039	uCOMP-8	ASB	Abs Cross Assembler For Data General Host Computer	BSO
67	SW-CF8039/10,20,PDP	8039	uCOMP-8	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
68	SW-CF8039/DGC	8039	uCOMP-8	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
69	SW-CP8039/10,20,PDP	8039	uCOMP-8	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
70	SW-CP8039/DGC	8039	uCOMP-8	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
71	SW-CR8039/10,20,PDP	8039	uCOMP-8	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
72	SW-CR8039/DGC	8039	uCOMP-8	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
73	SW-CX8039/10,20,PDP	8039	uCOMP-8	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
74	SW-CX8039/DGC	8039	uCOMP-8	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
75	SW-CY8039/10,20,PDP	8039	uCOMP-8	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
76	SW-CY8039/DGC	8039	uCOMP-8	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
77	SW-SI8039/10,20,PDP	8039	uCOMP-8	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
78	SW-SI8039/DGC	8039	uCOMP-8	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
79	SW-CA8041/10,20,PDP	8041	UPI41	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
80	SW-CA8041/DGC	8041	UPI41	ASB	Abs Cross Assembler For Data General Host Computer	BSO
81	SW-CF8041/10,20,PDP	8041	UPI41	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
82	SW-CF8041/DGC	8041	UPI41	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
83	SW-CP8041/10,20,PDP	8041	UPI41	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
84	SW-CP8041/DGC	8041	UPI41	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
85	SW-CR8041/10,20,PDP	8041	UPI41	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
86	SW-CR8041/DGC	8041	UPI41	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
87	SW-CX8041/10,20,PDP	8041	UPI41	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
88	SW-CX8041/DGC	8041	UPI41	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
89	SW-CY8041/10,20,PDP	8041	UPI41	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
90	SW-CY8041/DGC	8041	UPI41	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
91	SW-SI8041/10,20,PDP	8041	UPI41	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
92	SW-SI8041/DGC	8041	UPI41	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
93	SW-CA8048/10,20,PDP	8048	MCS48	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
94	SW-CA8048/DGC	8048	MCS48	ASB	Abs Cross Assembler For Data General Host Computer	BSO
95	SW-CF8048/10,20,PDP	8048	MCS48	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
96	SW-CF8048/DGC	8048	MCS48	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
97	SW-CP8048/10,20,PDP	8048	MCS48	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
98	SW-CP8048/DGC	8048	MCS48	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
99	SW-CR8048/10,20,PDP	8048	MCS48	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
100	SW-CR8048/DGC	8048	MCS48	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
101	SW-CX8048/10,20,PDP	8048	MCS48	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
102	SW-CX8048/DGC	8048	MCS48	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
103	SW-CY8048/10,20,PDP	8048	MCS48	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
104	SW-CY8048/DGC	8048	MCS48	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
105	SW-SI8048/10,20,PDP	8048	MCS48	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
106	SW-SI8048/DGC	8048	MCS48	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
107	SW-CA8049/10,20,PDP	8049	MCS48	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
108	SW-CA8049/DGC	8049	MCS48	ASB	Abs Cross Assembler For Data General Host Computer	BSO
109	SW-CF8049/10,20,PDP	8049	MCS48	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
110	SW-CF8049/DGC	8049	MCS48	CMP	Fortran Cross Compiler For Data General Host Computer	BSO

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	1 MFR. CODE
1	SW-CP8049/10,20,PDP	8049	MCS48	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
2	SW-CP8049/DGC	8049	MCS48	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
3	SW-CR8049/10,20,PDP	8049	MCS48	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
4	SW-CR8049/DGC	8049	MCS48	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
5	SW-CX8049/10,20,PDP	8049	MCS48	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
6	SW-CX8049/DGC	8049	MCS48	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
7	SW-CY8049/10,20,PDP	8049	MCS48	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
8	SW-CY8049/DGC	8049	MCS48	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
9	SW-SI8049/10,20,PDP	8049	MCS48	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
10	SW-SI8049/DGC	8049	MCS48	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
11	SW-CA8080/10,20,PDP	8080	MCS80	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
12	SW-CA8080/DGC	8080	MCS80	ASB	Abs Cross Assembler For Data General Host Computer	BSO
13	SW-CF8080/10,20,PDP	8080	MCS80	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
14	SW-CF8080/DGC	8080	MCS80	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
15	SW-CP8080/10,20,PDP	8080	MCS80	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
16	SW-CP8080/DGC	8080	MCS80	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
17	SW-CR8080/10,20,PDP	8080	MCS80	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
18	SW-CR8080/DGC	8080	MCS80	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
19	SW-CX8080/10,20,PDP	8080	MCS80	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
20	SW-CX8080/DGC	8080	MCS80	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
21	SW-CY8080/10,20,PDP	8080	MCS80	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
22	SW-CY8080/DGC	8080	MCS80	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
23	SW-SI8080/10,20,PDP	8080	MCS80	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
24	SW-SI8080/DGC	8080	MCS80	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
25	SW-CA8085/10,20,PDP	8085	MCS85	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
26	SW-CA8085/DGC	8085	MCS85	ASB	Abs Cross Assembler For Data General Host Computer	BSO
27	SW-CF8085/10,20,PDP	8085	MCS85	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
28	SW-CF8085/DGC	8085	MCS85	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
29	SW-CP8085/10,20,PDP	8085	MCS85	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
30	SW-CP8085/DGC	8085	MCS85	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
31	SW-CR8085/10,20,PDP	8085	MCS85	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
32	SW-CR8085/DGC	8085	MCS85	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
33	SW-CX8085/10,20,PDP	8085	MCS85	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
34	SW-CX8085/DGC	8085	MCS85	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
35	SW-CY8085/10,20,PDP	8085	MCS85	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
36	SW-CY8085/DGC	8085	MCS85	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
37	SW-SI8085/10,20,PDP	8085	MCS85	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
38	SW-SI8085/DGC	8085	MCS85	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
39	SW-CA8086/10,20,PDP	8086	MCS86	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
40	SW-CA8086/DGC	8086	MCS86	ASB	Abs Cross Assembler For Data General Host Computer	BSO
41	SW-CF8086/10,20,PDP	8086	MCS86	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
42	SW-CF8086/DGC	8086	MCS86	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
43	SW-CP8086/10,20,PDP	8086	MCS86	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
44	SW-CP8086/DGC	8086	MCS86	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
45	SW-CR8086/10,20,PDP	8086	MCS86	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
46	SW-CR8086/DGC	8086	MCS86	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
47	SW-CX8086/10,20,PDP	8086	MCS86	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
48	SW-CX8086/DGC	8086	MCS86	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
49	SW-CY8086/10,20,PDP	8086	MCS86	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
50	SW-CY8086/DGC	8086	MCS86	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
51	SW-SI8086/10,20,PDP	8086	MCS86	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
52	SW-SI8086/DGC	8086	MCS86	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
53	SW-CA8748/10,20,PDP	8748	MCS48	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
54	SW-CA8748/DGC	8748	MCS48	ASB	Abs Cross Assembler For Data General Host Computer	BSO
55	SW-CF8748/10,20,PDP	8748	MCS48	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
56	SW-CF8748/DGC	8748	MCS48	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
57	SW-CP8748/10,20,PDP	8748	MCS48	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
58	SW-CP8748/DGC	8748	MCS48	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
59	SW-CR8748/10,20,PDP	8748	MCS48	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
60	SW-CR8748/DGC	8748	MCS48	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
61	SW-CX8748/10,20,PDP	8748	MCS48	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
62	SW-CX8748/DGC	8748	MCS48	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
63	SW-CY8748/10,20,PDP	8748	MCS48	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
64	SW-CY8748/DGC	8748	MCS48	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
65	SW-SI8748/10,20,PDP	8748	MCS48	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
66	SW-SI8748/DGC	8748	MCS48	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
67	SW-CA8900/10,20,PDP	8900	CA8900	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
68	SW-CA8900/DGC	8900	CA8900	ASB	Abs Cross Assembler For Data General Host Computer	BSO
69	SW-CF8900/10,20,PDP	8900	CA8900	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
70	SW-CF8900/DGC	8900	CA8900	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
71	SW-CP8900/10,20,PDP	8900	CA8900	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
72	SW-CP8900/DGC	8900	CA8900	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
73	SW-CR8900/10,20,PDP	8900	CA8900	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
74	SW-CR8900/DGC	8900	CA8900	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
75	SW-CX8900/10,20,PDP	8900	CA8900	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
76	SW-CX8900/DGC	8900	CA8900	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
77	SW-CY8900/10,20,PDP	8900	CA8900	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
78	SW-CY8900/DGC	8900	CA8900	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
79	SW-SI8900/10,20,PDP	8900	CA8900	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
80	SW-SI8900/DGC	8900	CA8900	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
81	SW-CA9440/10,20,PDP	9440	9440	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
82	SW-CA9440/DGC	9440	9440	ASB	Abs Cross Assembler For Data General Host Computer	BSO
83	SW-CF9440/10,20,PDP	9440	9440	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
84	SW-CF9440/DGC	9440	9440	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
85	SW-CP9440/10,20,PDP	9440	9440	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
86	SW-CP9440/DGC	9440	9440	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
87	SW-CR9440/10,20,PDP	9440	9440	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
88	SW-CR9440/DGC	9440	9440	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
89	SW-CX9440/10,20,PDP	9440	9440	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
90	SW-CX9440/DGC	9440	9440	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
91	SW-CY9440/10,20,PDP	9440	9440	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
92	SW-CY9440/DGC	9440	9440	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
93	SW-SI9440/10,20,PDP	9440	9440	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
94	SW-SI9440/DGC	9440	9440	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
95	SW-CA9900/10,20,PDP	9900	990	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
96	SW-CA9900/DGC	9900	990	ASB	Abs Cross Assembler For Data General Host Computer	BSO
97	SW-CF9900/10,20,PDP	9900	990	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
98	SW-CF9900/DGC	9900	990	CMP	Fortran Cross Compiler For Data General Host Computer	BSO
99	SW-CP9900/10,20,PDP	9900	990	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer	BSO
100	SW-CP9900/DGC	9900	990	CMP	Pascal Cross Compiler For Data General Host Computer	BSO
101	SW-CR9900/10,20,PDP	9900	990	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
102	SW-CR9900/DGC	9900	990	ASB	Reloc Cross Assembler For Data General Host Computer	BSO
103	SW-CX9900/10,20,PDP	9900	990	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
104	SW-CX9900/DGC	9900	990	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer	BSO
105	SW-CY9900/10,20,PDP	9900	990	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer	BSO
106	SW-CY9900/DGC	9900	990	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer	BSO
107	SW-SI9900/10,20,PDP	9900	990	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer	BSO
108	SW-SI9900/DGC	9900	990	DEB	Sym Simulator Debugger For Data General Host Computer	BSO
109	SW-CA9985/10,20,PDP	9985	CA9985	ASB	Abs Cross Assembler For DEC10,20 and PDP11 Host Computer	BSO
110	SW-CA9985/DGC	9985	CA9985	ASB	Abs Cross Assembler For Data General Host Computer	BSO

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	[4] SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	[2] GENERIC I.D. $-MULTI-SYSTEM APPLICATION	[3] SYSTEM TYPE No.	CATEGORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME	LANGUAGE	AVAILABILITY/COMPATIBILITY	[1] MFR. CODE
1	SW-CF9985/10,20,PDP	9985	CA9985	CMP	Fortran Cross Compiler For DEC10,20 and PDP11 Host Computer			BSO
2	SW-CF9985/DGC	9985	CA9985	CMP	Fortran Cross Compiler For Data General Host Computer			BSO
3	SW-CP9985/10,20,PDP	9985	CA9985	CMP	Pascal Cross Compiler For DEC10,20 and PDP11 Host Computer			BSO
4	SW-CP9985/DGC	9985	CA9985	CMP	Pascal Cross Compiler For Data General Host Computer			BSO
5	SW-CR9985/10,20,PDP	9985	CA9985	ASB	Reloc Cross Assembler For DEC10,20 and PDP11 Host Computer			BSO
6	SW-CR9985/DGC	9985	CA9985	ASB	Reloc Cross Assembler For Data General Host Computer			BSO
7	SW-CX9985/10,20,PDP	9985	CA9985	ASB	Abs Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer			BSO
8	SW-CX9985/DGC	9985	CA9985	ASB	Abs Cross Assembler W/X Ref-For Data General Host Computer			BSO
9	SW-CY9985/10,20,PDP	9985	CA9985	ASB	Reloc Cross Assembler W/X Ref-For DEC10,20 and PDP11 Host Computer			BSO
10	SW-CY9985/DGC	9985	CA9985	ASB	Reloc Cross Assembler W/X Ref-For Data General Host Computer			BSO
11	SW-SI9985/10,20,PDP	9985	CA9985	DEB	Sym Simulator Debugger For DEC10,20 and PDP11 Host Computer			BSO
12	SW-SI9985/DGC	9985	CA9985	DEB	Sym Simulator Debugger For Data General Host Computer			BSO
13	SW-DB/65	6500	DB/65	DEB	Debug Board Software and Hardware;Breakpoints;symbolic Debug			CAC
14	SW-6500F	6500	IBM,etc	ASB	Fortran Cross Assembler For IBM/370,CDC 6000,Honeywell 6000			CAC
15	SW-CSL/65-11	6500	PDP-11	CMP	Compiler For CSL/65(PL/65);Runs on PDP-11			CAC
16	SW-MINMIC	6500	PDP-11	ASB	Cross ASM For PDP-11;RT-11 or RSTS. Written in Macro-11			CAC
17	SW-CSL/65	6500	SYS65	CMP	Compiler For CSL/65(PL/65);Runs on System 65			CAC
18	SW-M1-CCOS	Z80	MM1		Real-Time Operating System			CLI
19	SW-MSERIES#1	8008	L,M SERIES	DEB	Octal Debug Technique			CLI
20	SW-MSERIES#2	8008	L,M SERIES	EDT	Editor			CLI
21	SW-MSERIES#3	8008	L,M SERIES	ASB	Assembler			CLI
22	SW-MSERIES#4	8008	L,M SERIES	ASB	Cross;Assembler;Operates on DEC PDP-8 Computer			CLI
23	SW-MSERIES#5	8008	L,M SERIES	SSS	PROM Programmer Control Program			CLI
24	SW-MSERIES#6	8008	L,M SERIES	SSS	Tape Conversion Program			CLI
25	SW-M1ABS	8080	MM1	ASB	Absolute Assembler Program			CLI
26	SW-M1BOS▼	8080	MM1	OPS	Basic Operating Sys for the MM1;Located in PROM Section of the CPU Bd			CLI
27	SW-M1DOS	8080	MM1	SSS	Resident Disk File Handling Program for F715andF725 Floppy Disk Sys			CLI
28	SW-M1EDIT	8080	MM1	EDT	Source Program Text Editor			CLI
29	SW-M1FORT	8080	MM1	CMP	Resident Compiler for FORTRAN IV			CLI
30	SW-M1ICON	8080	MM1	OPS	Input/Output Control Program Part of Basic Operating System for MM1			CLI
31	SW-M1LINK	8080	MM1	LOA	Linking Loader Program			CLI
32	SW-M1ODT	8080	MM1	MON	Sys Monitor/Debugging Program Part of Basic Operating System for MM1			CLI
33	SW-M1REL	8080	MM1	ASB	Relocating Assembler Program Used with Linking Loader Program			CLI
34	SW-M1SYSG	8080	MM1	SSS	System Generator Prog;Programs Control Sys for Combination of Peripher			CLI
35	SW-MCB216	Z80	Z2	MON	Monitor and Control BASIC Resident in 2 ROMs			CRO
36	SW-16KB-1608▼	Z80	Z2,CS3	LAN	16k BASIC in Prom;			CRO
37	SW-CB-308▼	Z80	Z2,CS3	LAN	3k Control BASIC in Prom;Control Applications;Integer Only Arith			CRO
38	SW-CDOS	Z80	Z2,CS3	OPS	Cromemco Disk Operating System:For IO Control,File Management			CRO
39	SW-DGR-L	Z80	Z2,CS3		15 Game Programs for DAZZLER:Model CGI, on 8 inch Disk			CRO
40	SW-DGR-S	Z80	Z2,CS3		15 Game Programs for DAZZLER:Model CGI,on 5 inch Disk			CRO
41	SW-FDA-L	Z80	Z2,CS3	ASB	Relocatable Macro Assembler on 8 in Floppy Disk			CRO
42	SW-FDA-S	Z80	Z2,CS3	ASB	Relocatable Macro Assembler on 5 in Floppy Disk			CRO
43	SW-FDB-L	Z80	Z2,CS3	LAN	16k BASIC:16k Disk-Extended Z80 BASIC;On 8 in Floppy Disk			CRO
44	SW-FDB-S	Z80	Z2,CS3	LAN	16k BASIC:16k Disk-Extended Z80 BASIC;On 5 in Floppy Disk			CRO
45	SW-FDC-L	Z80	Z2,CS3	CMP	COBOL Compiler on 8 in Floppy Disk			CRO
46	SW-FDC-S	Z80	Z2,CS3	CMP	COBOL Compiler on 5 in Floppy Disk			CRO
47	SW-FDF-L	Z80	Z2,CS3	LAN	FORTRAN IV:Operates as Part of CDOS;On 8 in Floppy Disk			CRO
48	SW-FDF-S	Z80	Z2,CS3	LAN	FORTRAN IV:Operates as Part of CDOS;On 5 in Floppy Disk			CRO
49	SW-FDG-L	Z80	Z2,CS3	SSS	Program to Use DAZZLER:Model CGI Displays Graphics,Alphanum,5inch Disk			CRO
50	SW-FDG-S	Z80	Z2,CS3	SSS	Program to Use DAZZLER:Model CGI Displays Graphics,Alphanum,5inch Disk			CRO
51	SW-FDR-L	Z80	Z2,CS3	LAN	RATFOR Rational FORTRAN;Added Statements Such as For,While,Else,8 inch			CRO
52	SW-FDR-S	Z80	Z2,CS3	LAN	RAT for Rational Fortran;Added Statements Such as FOR,WHILE,ELSE,5inch			CRO
53	SW-MUB-L	Z80	Z2,CS3	LAN	Multi-User BASIC:Software Pkg on 8 in Disk;Up to 7 Users			CRO
54	SW-MUB-S	Z80	Z2,CS3	LAN	Multi-User BASIC:Software Pkg on 5 in Disk;Up to 7 Users			CRO
55▼	SW-STB-S	Z80	Z2,CS3	LAN	32K Structured Basic;Keyed Sequential Access Method;Structured Prog.			CRO
56	SW-TSS-L	Z80	Z2,CS3	SIM	TRACE System Simulator on 8 in Floppy Disk			CRO
57	SW-TSS-S	Z80	Z2,CS3	SIM	TRACE System Simulator on 5 in Floppy Disk			CRO
58	SW-WPS-L	Z80	Z2,CS3	LAN	Word Processing System;Req 48k RAM Min;Avail 8 inch Disk			CRO
59	SW-WPS-S	Z80	Z2,CS3	LAN	Word Processing System;Req 48k RAM Min;Avail 5 inch Disk			CRO
60	SW-ZA-808▼	Z80	Z2,CS3	OPS	ASSEMBLER/RESIDENT OPERATING SYSTEM in 2708 Proms			CRO
61	SW-ZM-108▼	Z80	Z2,CS3	MON	MONITOR in 2708 Proms			CRO
62	SW-DBM-L	Z80A	Z2,CS3	BAS	Data Base Management;8inch Disk;Min 48K Reg;Sys 2 or 3 Compatible			CRO
63	SW-DBM-S	Z80A	Z2,CS3	BAS	Data Base Management Sys;5inch Disk;Min 48K Reg;Sys 2 or 3 Compatible			CRO
64	SW-FDM-L	Z80A	Z2,CS3	LAN	Multiuser BASIC;Max 7 Users;8 inch Disk			CRO
65	SW-FDM-S	Z80A	Z2,CS3	LAN	Multiuser BASIC;Max 7 Users;5 inch Disk			CRO
66	SW-MDBM-S	Z80A	Z2,CS3	BAS	Multiuser Data Base Manag;5inch Disk;Min 48K Reg;Sys 2 or 3 Compatible			CRO
67	SW-MDBN-L	Z80A	Z2,CS3	BAS	Multiuser Data Base Manag;8inch Disk;Min 48K Reg;Sys 2 or 3 Compatible			CRO
68	SW-QJ713-DZ	LSI11	LSI11	OPS	RT-11 FMS-11(Licence Only)Cat C			DE
69	SW-QJ013-CQ	LSI11	LSI11	OPS	RT-11 Real-Time Oper Sys for the Single User;DECpack(RL01);Supp Cat C			DEC
70	SW-QJ013-CX	LSI11	LSI11	OPS	RT-11 Real-Time Oper Sys for Single User;Floppy Disk(RX02);Supp CAT C			DEC
71	SW-QJ013-CY	LSI11	LSI11	OPS	RT-11 Real-Time Oper Sys for the Single User;Floppy Disk(RX01);Cat C			DEC
72	SW-QJ013-DZ	LSI11	LSI11	OPS	RT-11 Real-Time Oper Sys for the Single User;License Only;Supp Cat C			DEC
73	SW-QJ628-DZ	LSI11	LSI11	OPS	RSX-11M Oper Sys Provides Run-Time Environment;License Only Supp Cat C			DEC
74	SW-QJ642-AE	LSI11	LSI11	OPS	RSX-11S Oper Sys;Provides Run-time Environment;DECpack(RK05);Sup Cat A			DEC
75	SW-QJ642-AY	LSI11	LSI11	OPS	RSX-11S Oper Sys;Provides Run-time Environment;Floppy Disk(RX01);Cat A			DEC
76	SW-QJ642-CE	LSI11	LSI11	OPS	RSX-11S Oper Sys;Provides Run-time Environment;DECpack(RK05);Sup Cat C			DEC
77	SW-QJ642-CY	LSI11	LSI11	OPS	RSX-11S Oper Sys;Provides Run-time Environment;Floppy Disk(RX01);Cat C			DEC
78	SW-QJ642-DZ	LSI11	LSI11	OPS	RSX-11S Oper Sys;Provides Run-time Environment;License Only;Supp Cat C			DEC
79	SW-QJ713-AG	LSI11	LSI11	OPS	RT-11 FMS-11 Forms Manag Sys;DECtape 11(TU58)Supp Cat A			DEC
80	SW-QJ713-AY	LSI11	LSI11	OPS	RT-11 FMS-11 Floppy Disk(RX01)Supp Cat A			DEC
81	SW-QJ713-CG	LSI11	LSI11	OPS	RT-11 FMS-11 DECtape 11(TU58)Cat C			DEC
82	SW-QJ713-CQ	LSI11	LSI11	OPS	RT-11 FMS-11 DECpack(RL01)Cat C			DEC
83	SW-QJ713-CY	LSI11	LSI11	OPS	RT-11 FMS-11 Floppy Disk(RX01)Cat C			DEC
84	SW-QJ813-AQ	LSI11	LSI11	LAN	FORTRAN/RT-11 Extended Superset of FORTRAN IV;DECpack(RL01) Cat B			DEC
85	SW-QJ813-AY	LSI11	LSI11	LAN	FORTRAN/RT-11;Extended Superset of FORTRAN IV;Floppy Disk(RX01);Cat B			DEC
86	SW-QJ813-CQ	LSI11	LSI11	LAN	FORTRAN/RT-11 Extended Superset of FORTRAN;DECpack(RL01)Cat C			DEC
87	SW-QJ813-CY	LSI11	LSI11	LAN	FORTRAN/RT-11;Extended Superset of FORTRAN IV;Floppy Disk(RX01);Cat C			DEC
88	SW-QJ813-DZ	LSI11	LSI11	LAN	FORTRAN/RT-11;Extended Superset of FORTRAN IV;License Only;Supp Cat C			DEC
89	SW-QJ907-CQ	LSI11	LSI11	LAN	SPL-11 Interactive Program Lang for Sci;Eng;Bus;DECpack(RL01)Cat C			DEC
90	SW-QJ907-CY	LSI11	LSI11	LAN	APL-11;Interactive Program Lang for Sci;Eng,Bus;Flop Disk(RX01);Cat C			DEC
91	SW-QJ907-DZ	LSI11	LSI11	LAN	APL-11;Interactive Program Lang for Sci;Eng,Bus;License Only;Cat C			DEC
92	SW-QJ913-AE	LSI11	LSI11	LAN	BASIC-11/RT-11;DECpack(RK05);Support Category B			DEC
93	SW-QJ913-AQ	LSI11	LSI11	LAN	Basic-11/RT-11;DECpack(RL01)Cat B			DEC
94	SW-QJ913-AY	LSI11	LSI11	LAN	BASIC-11/RT-11;Floppy Disk(RX01);Support Category B			DEC
95	SW-QJ913-CQ	LSI11	LSI11	LAN	Basic-11/RT-11;DECpack(RL01)Cat C			DEC
96	SW-QJ913-DZ	LSI11	LSI11	LAN	BASIC-11/RT-11;License Only;Support Category C			DEC
97	SW-QJ918-AQ	LSI11	LSI11		Basic-Plus-2/RSX-11M Superset of Standard Basic;DECpack(RL01)Cat A			DEC
98	SW-QJ918-CQ	LSI11	LSI11		Basic-Plus-2/RSX-11M Superset of Standard Basic;DECpack(RL01)Cat C			DEC
99	SW-QJ921-AQ	LSI11	LSI11	OPS	Multi-User BASIC/RT-11;1-8 Users;DECpack(RL01);Supp Cat B			DEC
100	SW-QJ921-AY	LSI11	LSI11	OPS	Multi-user BASIC/RT-11;1-8 users;Floppy Disk(RX01);Support Category B			DEC
101	SW-QJ921-CQ	LSI11	LSI11	OPS	Multi-User BASIC/RT-11;1-8 Users;DECapck(RL01);Supp Cat C			DEC
102	SW-QJ921-CY	LSI11	LSI11	OPS	Multi-user BASIC/RT-11;1-8 users;DECpack(RK05);Support Category C			DEC
103	SW-QJ921-DZ	LSI11	LSI11	OPS	Multi-user BASIC/RT-11;1-8 users;License Only;Support Category C			DEC
104	SW-QJ922-AE	LSI11	LSI11	LAN	FOCAL/RT-11;Interact Program Lang for Sci;Eng,Stud;DECpack(RK05);CAT B			DEC
105	SW-QJ922-AY	LSI11	LSI11	LAN	FOCAL/RT-11;Interact Program Lang for Sci;Eng,Stud;FL DSK(RX01);Cat B			DEC
106	SW-QJ922-CY	LSI11	LSI11	LAN	FOCAL/RT-11;Interact Program Lang for Sci;Eng,Stud;FL DSK(RX01);Cat C			DEC
107	SW-QJ922-DZ	LSI11	LSI11	LAN	FOCAL/RT-11;Interact Program Lang for Sci;Eng,Stud;License Only;Cat C			DEC
108	SW-QJ960-AY	LSI11	LSI11	SUB	SSP-11/RT-11;Scientic Subroutine for FORTRAN/RT-11;FL DSK(RX01);Cat B			DEC
109	SW-QJ960-DZ	LSI11	LSI11	SUB	SSP-11/RT-11;Scientic Subroutine for FORTRAN/RT-11;License Only;Cat C			DEC
110	SW-QJ980-AQ	LSI11	LSI11	LAN	FORTRAN/RT-11;Extension of Standard;DECpack(RL01);Cat B			DEC

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	1 MFR. CODE
1	SW-QJ980-AY	LSI11	LSI11	LAN	FORTRAN/RT-11;Extension of Standard;Floppy Disk(RX01);Cat B	DEC
2	SW-QJ980-CQ	LSI11	LSI11	LAN	FORTRAN/RT-11;Extension of Standard;DECpack(RL01);Cat C	DEC
3	SW-QJ980-CY	LSI11	LSI11	LAN	FORTRAN/RT-11;Extension of Standard;Floppy Disk(RX01);Cat C	DEC
4	SW-QJ980-DZ	LSI11	LSI11	LAN	FORTRAN/RT-11;Extension of Standard;License Only;Support Cat C	DEC
5	SW-QJD58-AY	LSI11	LSI11	SIM	RT-11/LSI11 2780;Emulates IBM 2780 Terminal;On Floppy Disk RX01,Cat A	DEC
6	SW-QJD58-CQ	LSI11	LSI11	SIM	RT-11/LSI11 2780;Emulates IBM 2780 Terminal;On DECpack RL01,Cat C	DEC
7	SW-QJD58-CY	LSI11	LSI11	SIM	RT-11/LSI11 2780;Emulates IBM 2780 Terminal;On Floppy Disk RX01,Cat C	DEC
8	SW-QJD58-DZ	LSI11	LSI11	SIM	RT-11/LSI11 2780;Emulates IBM 2780 Terminal;License Only, Cat C	DEC
9	SW-QJV10-CB	LSI11	LSI11	MFS	PTS-11 Paper Tape Sys,ED-11 Editor,PALS Assmbl,LINK-11S Absolute Load,	DEC
10	SW-QJV11-CB	LSI11	LSI11	SSS	PROM Formatter Software,Minimum Hardware 4k LSI-11 or 11/03	DEC
11	SW-QJV13-DZ	LSI11	LSI11	OPS	RT-11 Run Time Systi;for Selected Modules in RT-11 Catagory C	DEC
12	SW-QJV40-YY	LSI11	LSI11	MFS	Writable Cont Store Software Development Tools/RT-11 On Floppy Disc	DEC
13	SW-QP100-AQ	LSI11	LSI11	LAN	FORTRAN IV-PLUS/RSX-11M;Superset of FORTRAN IV;DECpack(RL01);Cat A	DEC
14	SW-QP100-CQ	LSI11	LSI11	LAN	FORTRAN IV-PLUS/RSX-11M;Superset of FORTRAN IV;DECpack(RL01);Cat C	DEC
15	SW-QP100-DZ	LSI11	LSI11	LAN	FORTRAN IV-PLUS/RSX-11M;Superset of FORTRAN IV;Licence Only;Cat C	DEC
16	SW-QP230-AQ	LSI11	LSI11	LAN	FORTRAN IV/RSX-11M;Extended of FORTRAN IV;DECpack(RL01);Cat B	DEC
17	SW-QP230-CQ	LSI11	LSI11	LAN	FORTRAN IV/RSX-11M;Extended Superset of FORTRAN IV;DECpack(RL01);Cat C	DEC
18	SW-QP230-DZ	LSI11	LSI11	LAN	FORTRAN IV/RSX-11M;Extended Superset of FORTRAN IV;Licence Only;Cat C	DEC
19	SW-QP240-AQ	LSI11	LSI11	LAN	BASIC-11/RSX-11M;Superset of BASIC;Compiler;DECpack(RL01);Cat B	DEC
20	SW-QP240-CQ	LSI11	LSI11	LAN	BASIC-11/RSX-11M;Superset of BASIC;Comiler;DECpack(RL01);CatC	DEC
21	SW-QP240-DZ	LSI11	LSI11	LAN	BASIC-11/RSX-11M;Superset of BASIC;Compiler;Licence Only;Cat C	DEC
22	SW-QP901-AQ	LSI11	LSI11	SSS	RMS-11/RSX-11M;Keyed for RSX-11M;DECpack(RL01);Cat A	DEC
23	SW-QP901-CQ	LSI11	LSI11	SSS	RMS-11/RSX-11M;Keyed Access for RSX-11M;DECpack(RL01);Cat C	DEC
24	SW-QP901-DZ	LSI11	LSI11	SSS	RMS-11/RSX-11M;Keyed Access for RSX-11M;Licence Only;Cat C	DEC
25	SW-ZJ271-RB	LSI11	LSI11	DIA	LSI11 System Diagnostics;On Paper Tape,Support Catagory C	DEC
26	SW-ZJ271-RQ	LSI11	LSI11	DIA	LSI11 System Diagnostics;DECpack(RL01);Cat C	DEC
27	SW-ZJ271-RX	LSI11	LSI11	DIA	LSI11 System Diagnostics;Floppy Disk(RX02);Cat C	DEC
28	SW-ZJ271-RY	LSI11	LSI11	DIA	LSI11 System Diagnostics;Floppy Disk(RX01);Cat C	DEC
29	SW-ZJV01-RB	LSI11	LSI11	DIA	LSI11 Basic Diagnostics;On Paper Tape, Support Category C	DEC
30	SW-DOS,AOS	MICRONOVA	MICRONOVA	OPS	DOS-AndAOS-Compatible Versions of MBC/M,Tests Programs on Larger Comp	DGC
31	SW-MBC/M	MICRONOVA	MICRONOVA	OPS	Small Operating System,Provides I/O Buffering,Multitasking,ETC	DGC
32	SW-MICRONOVA#1	MICRONOVA	MICRONOVA	OPS	Disc Operating System	DGC
33	SW-MICRONOVA#2	MICRONOVA	MICRONOVA	SSS	Command Line Intetpreter	DGC
34	SW-MICRONOVA#3	MICRONOVA	MICRONOVA	EDT	Text Editor	DGC
35	SW-MICRONOVA#4	MICRONOVA	MICRONOVA	CMP	FORTRAN IV Compiler	DGC
36	SW-MICRONOVA#5	MICRONOVA	MICRONOVA	ASB	MACRO Assembler	DGC
37	SW-MICRONOVA#6	MICRONOVA	MICRONOVA	EDT	Library File Editor	DGC
38	SW-MICRONOVA#7	MICRONOVA	MICRONOVA	LOA	Relocatable Loader	DGC
39	SW-MICRONOVA#8	MICRONOVA	MICRONOVA	OPS	Real Time Operating System	DGC
40	SW-MICRONOVA#9	MICRONOVA	MICRONOVA	DEB	Symbolic Debugger	DGC
41	SW-ODT	MICRONOVA	MICRONOVA	DEB	Octal Debugger,Helps Test Programs After Installation in MBC/1	DGC
42	SW-PROMTAPE	MICRONOVA	MICRONOVA	SSS	Helps Transfer Programs to Programmable ROM	DGC
43	SW-TDGOPSYSTEM	MULTI$	TDGSYSTEMS	OPS	Op System for 8080,Z80,6800,6500	DIG
44	SW-TBXTVCOS	Z80	TDGZ80SYS	SUB	Cassette;TINYBASIC2;Limited Sub BASIC;Self Adapt to 6kPlus Mem;TV Out	DIG
45	SW-TDGASSEMBLER	Z80	TDGZ80SYS	ASB	Assembler with ASCII,Baudot,Selectric Compatibility	DIG
46	SW-TDGASSEMBLER2	Z80	TDGZ80SYS	ASB	Updated Z80 Assembler1	DIG
47	SW-TDGASSMEDIT	Z80	TDGZ80SYS	ASB	Assembler1 Source File Editor	DIG
48	SW-TDGBUS1	Z80	TDGZ80SYS	BAS	Business-Basic;Extended Maxi-BASIC	DIG
49	SW-TDGCBASIC	Z80	TDGZ80SYS	BAS	Compiler/Interpreter;Runs with MCOS	DIG
50	SW-TDGCONVERS	Z80	TDGZ80SYS	LAN	Interpretive Threaded Lang for PHIMON Based Sys	DIG
51	SW-TDGDISASSEMBLER	Z80	TDGZ80SYS	ASB	Disassembler with ASCII,Baudot,Selectric Compatibility	DIG
52	SW-TDGDISKMON	Z80	TDGZ80SYS	OPS	Disk Oper Sys;Controls Up to 4 Floppy and 4 Phideck Drives;Req 2k Mem	DIG
53	SW-TDGEBASIC	Z80	TDGZ80SYS	CMP	Hobbyist Oriented BASIC Compiler/Interpreter;Non Interactive	DIG
54	SW-TDGEDFORM	Z80	TDGZ80SYS	EDT	Editor/Formatter;Rewrite of Classy Text Editor;Avail on Cassette	DIG
55	SW-TDGEDUCATORZ80	Z80	TDGZ80SYS	OPS	Various Instructions Versus Z80 Status and Operation	DIG
56	SW-TDGHAM	Z80	TDGZ80SYS	LOA	Amateur Radio CW Send/Receive RTTY Baudot Cassette	DIG
57	SW-TDGMAXIBASIC	Z80	TDGZ80SYS	SUB	Basic Compatible with 110 Baud ASC11,60wpm Baudot,Selectric;7 Game Set	DIG
58	SW-TDGMCOS	Z80	TDGZ80SYS	OPS	Disk Oper Sys;Superset of CP/M	DIG
59	SW-TDGMCOSASSM	Z80	TDGZ80SYS	ASB	Relocating Macro Assembler;Switch for 8080 Opcodes Only;Runs with MCOS	DIG
60	SW-TDGMCOSGAMES	Z80	TDGZ80SYS	SUB	CBASIC/EBASIC Game Set;Requires 26k Mem,TVC64 and 2 Mini or Stnd Disks	DIG
61	SW-TDGMCOSTOP	Z80	TDGZ80SYS	SSS	Text Output Processor;Functions Under MCOS	DIG
62	SW-TDGMCOSUTIL	Z80	TDGZ80SYS	SSS	Minimum 20 External Commands Directly Executable by MCOS	DIG
63	SW-TDGMINIBASIC	Z80	TDGZ80SYS	SUB	Cassette;String Manip/Handl;Self Adapt to 6k Plus Mem;TV Out;4Game Set	DIG
64	SW-TDGOASIS	Z80	TDGZ80SYS	OPS	Disk Oper Sys;Util,File Mngmnt Incl ISAM,Sys Ed,Exec Lan;Req 34k,TVC64	DIG
65	SW-TDGOASISASSM	Z80	TDGZ80SYS	MFS	Z80 Macro Assembler,Debugger and Linking Loader	DIG
66	SW-TDGOBASIC	Z80	TDGZ80SYS	EDT	Extended BASIC;Supports all File Structures Incl ISAM	DIG
67	SW-TDGOPUS1	Z80	TDGZ80SYS	LAN	Personal/Business Appl;Syntax Similiar to BASIC;55 Dig,127 Alpha Char	DIG
68	SW-TDGOPUS2	Z80	TDGZ80SYS	LAN	OPUS1 Extended to Support ASCII,Machine Code,Diminsioned Files	DIG
69	SW-TDGPHIMON	Z80	TDGZ80SYS	OPS	Cassette Storage Op Sys;15 Commands;Directory Handling and Control Rou	DIG
70	SW-TDGSCRIPT	Z80	TDGZ80SYS	SSS	Word Processor;Produces Manuals,Letters,Etc.Generates Tables,Etc	DIG
71	SW-TDGTEXTEDITOR	Z80	TDGZ80SYS	BAS	Manipulation of Textual Material with ASCII,Baudot,SEL	DIG
72	SW-TDGTINYGAMES	Z80	TDGZ80SYS	SUB	Use with TBXTVCOS;Six Game Options on Cassette	DIG
73	SW-TDGVOT	Z80	TDGZ80SYS	ASB	VOTRAX1 Program Software Speech Synthesizer	DIG
74	SW-TDGWOPROC1	Z80	TDGZ80SYS	SSS	Word Processing System;Includes PHIMON and Suding Audio Cass Based Sys	DIG
75	SW-TDGZ80RELO	Z80	TDGZ80SYS	SSS	Object Code Relocation Program	DIG
76	SW-TDGEDUCATOR8080	8080	TDG8080SYS	OPS	Various Instructions Versus 8080 Status and Operation	DIG
77	SW-145-7001▼	COSMOS	COSMOS	SSS	Util;Programming and Debug Aid	DIV
78	SW-CS-1	COSMOS	RS-232C	OPS	Typical Industrial Control System Application of Eicomp Series Cards	DIV
79	SW-EM-1	COSMOS	RS-232C	OPS	Energy Management Control System Up to 127 Intelligent Remote Units	DIV
80	SW-DS-2	Z80$	8080	OPS	Universal Development W/Optional Emulators	DIV
81	SW-SYSTEM8#1	8080	SYSTEM8	ASB	Assembler	DSI
82	SW-SYSTEM8#2	8080	SYSTEM8	CMP	Symbolic Compiler	DSI
83	SW-SYSTEM8#3	8080	SYSTEM8	CMP	FORTRAN Compiler	DSI
84	SW-DTLIB	LSI11	LSI11	SUB	Real Time FORTRAN Support Using DEC RT-11 Routines	DTI
85	SW-DynaBASIC	M6800	DMS	ASB	Preprocessor/Translator;Equates Name to Integer Value	DYN
86	SW-DynaBASIC-I	M6800	DMS	BAS	Compiler Compatible W/BASIC Language for DYNAMO Mgmt System	DYN
87	SW-DynaSCRIPT	M6800	DMS	BAS	Word Processing System w/Floppy Disk Storage	DYN
88	SW-DynaSORT	M6800	DMS	CMP	BASIC Compiler w/Floppy Disk Storage	DYN
89	SW-DYNAMO	M6800	DMS	OPS	DYNAMO Disk Op System;Supports DynaBASIC	DYN
90	SW-LMS	M6800	DMS	OPS	Lab uComputer System for Industrial Applications and Instrumentation	DYN
91	SW-APPV2	6800	DMS	ASB	6800 MACRO Assembler and Linking Loader;Requires min 32k RAM	DYN
92	SW-DYNABASICV2	6800	DMS	CMP	BASIC Compiler;Requires min 32k RAM	DYN
93	SW-DYNAMOV2	6800	DMS	OPS	Dynamo V2 Diskette Operating System;Requires min 16k RAM	DYN
94	SW-ONLINEV2	6800	DMS	LOA	Asynchronous Communications Package	DYN
95	SW-ETC1000-D	6502	ETC1000	OPS	32k Disk Operating System;for any Programming Application	ETL
96	SW-ETC6502-0701	6502	ETC1000	ASB	Resident Assembler Program Cassette	ETL
97	SW-ETC6502-0712	6502	ETC1000	LAN	BASIC A Version Cassette	ETL
98	SW-ETC6502-1761	6502	ETC1000	MFS	General Program Library, Disk	ETL
99	SW-ETCDOS	6502	ETC1000	OPS	Disk Operating System;Includes Assembler,Debug,Trace,BASIC,FOCAL,Edito	ETL
100#	SW-ESEKVE	6800	EURO-6	MFS	Program Pkg for Driving Sequence Controller Based on EURO-6 Modules	EURF
101#	SW-EBUG▼	6800	EURO-6,E-6	DEB	EBUG Firmware Stored in 1024x8 Bit ROM;Interfaces W/TTY,RS 232C	EURF
102#	SW-EBUG-II	6800	EURO-6,E-6	DEB	EBUG Firmware Stored In 1024x8 Bit ROM;Interface w/TTY,RS232C	EURF
103#	SW-EUROTERM-6	6800	EUROTERM-6	MFS	Multifunction Program;Compiler,Interpreter,Editing	EURF
104	SW-ASSMBLRZ80	Z80	MSZ80	ASB	Assembler on Tape for Z80 Systems	FCC
105	SW-BASCOMZ80	Z80	MSZ80	LAN	BASIC Compiler:Basic Lang Compiler-Disk Based Syst,Requires 32k Mem	FCC
106	SW-BASICZ80	Z80	MSZ80	LAN	Extended Basic for Tape/DiskBasedSyst:For Z80 BasedSyst,Needs 32kB Mem	FCC
107	SW-EDITZ80	Z80	MSZ80	EDT	Editor on Tape for Z80 System	FCC
108	SW-EMULZ80	Z80	MSZ80	SIM	In-Circuit Emulator/Monitor Program on Tape for Z80 System	FCC
109	SW-MDOSBASICZ80	Z80	MSZ80	OPS	Disk Op Sys with Basic Interpreter for Z80 Sys;Standard Floppy or Mini	FCC
110	SW-MDOSEMULZ80	Z80	MSZ80	OPS	Disk Op Sys with In-Circuit Emulator forZ80Sys;Standard FloppyOrMini	FCC

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

4.SYSTEM SOFTWARE INDEX

IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D.
(3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	[4] SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	[2] GENERIC I.D. $-MULTI-SYSTEM APPLICATION	[3] SYSTEM TYPE No.	CATE-GORY	S O F T W A R E L I B R A R Y NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	[1] MFR. CODE
1	SW-MDOSZ80	Z80	MSZ80	OPS	Disk Op Sys for Z80 Incl Monitor/Debugger;Editor,Assembler,Utility	FCC
2	SW-MONZ80	Z80	MSZ80	MON	Monitor/Debugger on Tape for Z80 System	FCC
3	SW-QUICKRUNZ80	Z80	MSZ80	MFS	Co-Resident Pkg with Monitor/Debugger,Editor/Assembler for Z80 System	FCC
4	SW-RDOSZ80	Z80	MSZ80	OPS	RDOS:Disk Operating System with Relocatable Macro Assembler,Linkage Ed	FCC
5	SW-UTLTYOBJZ80	Z80	MSZ80	SSS	Utility Object Program for Tape Duplication on Z80 System	FCC
6	SW-WORDPROCESSZ80	Z80	MSZ80	BAS	Preparation of Documents,Reports/Manuals for Z80 System	FCC
7	SW-QUICKRUN1802	1802	MS1802	ASB	QUICKRUN Cross Assem Pkg:Runs on 8080/Z80 Process,Cross Assem For 1802	FCC
8	SW-QUICKRUN3870	3870	MS3870	ASB	QUICKRUN Cross Assem Pkg:Runs on 8080/Z80 Process,Cross Assem For 3870	FCC
9	SW-ASSMBLR6800	6800	MS6800	ASB	Assembler on Tape for 6800 System	FCC
10	SW-BASCOM6800/6802	6800	MS6800	LAN	BASIC Compiler:Basic Lang Compiler-Disk Based Syst,Requires 32k Mem	FCC
11	SW-EDIT6800	6800	MS6800	EDT	Editor on Tape for 6800 System	FCC
12	SW-EMUL6800	6800	MS6800	SIM	In-Circuit Emulator/Monitor Program on Tape for 6800 System	FCC
13	SW-MDOS6800	6800	MS6800	OPS	Disk Op Sys for 6800 Incl Monitor/Debugger,Editor,Assembler,Utility	FCC
14	SW-MDOSEMUL6800	6800	MS6800	OPS	Disk Op Sys with In-Circuit Emulator for 6800 Sys;Standard Floppy or M	FCC
15	SW-MON6800	6800	MS6800	MON	Monitor/Debugger on Tape for 6800 System	FCC
16	SW-QUICKRUN6800	6800	MS6800	MFS	Co-Resident Pkg with Monitor/Debugger,Editor/Assembler for 6800 System	FCC
17	SW-RDOS6800/6802	6800	MS6800	OPS	RDOS:Disk Operating System with Relocatable Macro Assembler;Linkage Ed	FCC
18	SW-UTLTYOBJ6800	6800	MS6800	SSS	Utility Object Program for Tape Duplication on 6800 System	FCC
19	SW-QUICKRUN8048	8048	MS8048	ASB	QUICKRUN Cross Assem Pkg:Runs on 8080/Z80 Process,Cross Assem for 8048	FCC
20	SW-ASSMBLR8080	8080	MS8080	ASB	Assembler on Tape for 8080 System	FCC
21	SW-BASCOM8080/8085	8080	MS8080	LAN	BASIC Compiler:Basic Lang Compiler-Disk Based Syst,Requires 32k Mem	FCC
22	SW-BASIC8080	8080	MS8080	LAN	Extend Basic for Tape/Disk Based Syst;For 8080 Based System Needs 32kB	FCC
23	SW-EDIT8080	8080	MS8080	EDT	Editor on Tape for 8080 System	FCC
24	SW-EMUL8080	8080	MS8080	MON	In-Circuit Emulator/Monitor Program on Tape for 8080 System	FCC
25	SW-MDOS8080	8080	MS8080	OPS	Disk Op Sys for 8080 Incl Monitor/Debugger,Editor,Assembler,Utility	FCC
26	SW-MDOSBASIC8080	8080	MS8080	OPS	Disk Op Sys with Basic Interpreter for 8080Sys;Standard Floppy or Mini	FCC
27	SW-MDOSEMUL8080	8080	MS8080	OPS	Disk Op Sys with In-Circuit Emulator for 8080Sys;Standard FloppyOrMini	FCC
28	SW-MON8080	8080	MS8080	MON	Monitor/Debugger on Tape for 8080 System	FCC
29	SW-QUICKRUN8080	8080	MS8080	MFS	Co-Resident Pkg with Monitor/Debugger,Editor and Assemb for 8080 Sys	FCC
30	SW-RDOS8080/8085	8080	MS8080	OPS	RDOS:Disk Operating System with Relocatable Macro Assembler,Linkage Ed	FCC
31	SW-UTLTYOBJ8080	8080	MS8080	SSS	Utility Object Program for Tape Duplication on 8080 System	FCC
32	SW-WORDPROCESS8080	8080	MS8080	BAS	Preparation of Documents,Reports and Manuals for 8080 System	FCC
33	SW-MICROFORTH#2	MULTI$	CDP1800	MFS	Multi-Level uProc Lang Pkg;Disk,Assembl,Compiler,Interpret,Editor,Debu	FOR
34	SW-MINIFORTH	MULTI$	LSI11	MFS	FOR	FOR
35	SW-MICROFORTH#1	MULTI$	MCS80	MFS	Multi-Level uProc Lang Pkg;Disk,Assemb,Compiler,Interpret,Editor,Debug	FOR
36	SW-F8-DOS	F8	F8	OPS	Formulator Operating System Provides Floppy Disk Bulk Storage Capabil	FSC
37	SW-F8-DOS-III	F8	F8	OPS	Floppy Disk Op System Provides Storage to Formulator MK II And III	FSC
38	SW-F8#1	F8	F8	ASB	Resident Assembler	FSC
39	SW-F8#2	F8	F8	SIM	Simulator	FSC
40	SW-F8CROSSASSEMBLER	F8	F8	ASB	Cross Assemb for Use on 16 Bit Minicomput/ANSI FORTRAN IV Compiler	FSC
41	SW-F387FTST	F8	F8	DIA	F3870 Functional Tester	FSC
42	SW-F387XPEP	F8	F8	SIM	F387 Prototyping Emulation and Programming System	FSC
43	SW-F3870SIMULATOR	F8	F8	SIM	Simulator Module to Develop,Test and Debug Programs,F3870	FSC
44	SW-F9508010XX	F8	F8	OPS	F8 Formulator Mark III;Same asMark II with Quad I/O and Com Mod etc	FSC
45	SW-F9508011XX	F8	F8	OPS	F8 Formulator Mark I	FSC
46	SW-F9508012XX	F8	F8	OPS	F8 Formulator Mark II;Same as Mark I with 16k Byte RAM	FSC
47	SW-F9508013X	F8	F8	OPS	16k-Byte RAM Growth Pkg Converts Formulator Mark I to Mark II	FSC
48	SW-F9508014X	F8	F8	OPS	Growth Pkg for Formulator Mark II Conv to Mark III Quad I/O /Com Mod	FSC
49	SW-F95080150	F8	F8	OPS	Growth Pkg III Upgrade Form Mark I/II to Floppy Disk Operation	FSC
50	SW-F895085003	F8	F8	SIM	ROM Simulation Module	FSC
51	SW-F895089022	F8	F8	SIM	F3870 Emulator,Stand Alone Printed Circuit Module	FSC
52	SW-FIRLINK	9440/9445	9440/9445	MFS	SW/HW Pkg,Linking Target Hdw to Microflame Dev Sys Debug/Mon Programs	FSC
53	SW-CAP16	GA16	GA16	ASB	Assembler;SPC 16 Host Computers	GEN
54	SW-DBOS16	GA16	GA16	OPS	Disk Based Operating System	GEN
55	SW-FSO16	GA16	GA16	OPS	Free-Standing Operating System	GEN
56	SW-RJE16	GA16	GA16	LOA	Remote Job Entry System;IBM 360/370	GEN
57	SW-RTOS16	GA16	GA16	OPS	Real Time Operating System	GEN
58	SW-RTX16	GA16	GA16	MON	Real Time Executive System;SPC 16 Host Computers	GEN
59	SW-SDLC	GA16	GA16	LOA	Synchronous Data Link Control Software	GEN
60	SW-SPC16IOS	GA16	GA16	LOA	Input/Output System;FORTRAN SPC16 Host Computers	GEN
61	SW-U1004E	GA16	GA16	SIM	Remote Station Emulator;Univac Host Computer	GEN
62	SW-SBACOMP	SBA	SBA	CMP	Converts List Of Boolean Equations To SBA Code, Host System Or CP1600	GIC
63	SW-SBASIM	SBA	SBA	SIM	Simulates SBA Actions For Prog Debug,Vertification,Host Sys Or CP1600	GIC
64	SW-S16AL	1600	GIMINI	ASB	Symbolic Assembler	GIC
65	SW-S16BMR	1600	GIMINI	SUB	Subroutines;Binary Math Routines	GIC
66	SW-S16BPT	1600	GIMINI	SSS	Binary Paper Tape Generator;FORTRAN IV;Gen Elec Time-Share Comp Networ	GIC
67	SW-S16CCR	1600	GIMINI	SUB	Subroutines:Code Conversion Routines	GIC
68	SW-S16DGS	1600	GIMINI	DIA	Diagnostic Program Package	GIC
69	SW-S16DMR	1600	GIMINI	SUB	Subroutines;Decimal Math Routines	GIC
70	SW-S16FPR	1600	GIMINI	SUB	Subroutines,Floating Point Routines	GIC
71	SW-S16IOD	1600	GIMINI	SUB	Subroutines;Input/Output Drivers	GIC
72	SW-S16LDR▼	1600	GIMINI	LOA	Reloading Program Loader	GIC
73	SW-S16LNK	1600	GIMINI	LOA	Object Module Linker;FORTRAN IV;Gen Elec Time-Share Computer Network	GIC
74	SW-S16MDP▼	1600	GIMINI	SSS	Memory Dump Program	GIC
75	SW-S16MTR▼	1600	GIMINI	MON	Monitor	GIC
76	SW-S16ODP▼	1600	GIMINI	DEB	On-Line Debug Program	GIC
77	SW-S16OML	1600	GIMINI	LOA	Object Module Linker	GIC
78	SW-S16RLL	1600	GIMINI	LOA	Relocating Linking Loader	GIC
79	SW-S16RTG	1600	GIMINI	SSS	ROM Tape Generator;FORTRAN IV;Gen Elec Time-Share Computer Network	GIC
80	SW-S16SAL	1600	GIMINI	ASB	Super Assembler	GIC
81	SW-S16SIM	1600	GIMINI	SIM	Simulator;FORTRAN IV;Gen Elec Time-Share Computer Network	GIC
82	SW-S16SXAL	1600	GIMINI	ASB	Symbolic Cross Assemb;FORTRAN IV;Gen Elec Time-Share Computer Network	GIC
83	SW-S16TXE	1600	GIMINI	EDT	Text Editor	GIC
84	SW-S16XAL	1600	GIMINI	ASB	Symbolic Cross Assemb;FORTRAN IV;Gen Elec Time-Share Computer Network	GIC
85	SW-S16XRF	1600	GIMINI	SSS	Concordance Generator	GIC
86	SW-SAL1600	1600	GIMINI	LAN	Super Assembly Language;High Level Operations	GIC
87	SW-PICAL	1600	PIC1600	ASB	Assembler Program;FORTRAN Version Available	GIC
88	SW-PICBUG▼	1600	PIC1600	DEB	Debugger Program with In-circuit Emulation	GIC
89	SW-PICSIM	1600	PIC1600	SIM	Simulator:Software Interactive Simulator Prog,FORTRAN Version Avail	GIC
90#	SW-LP8000#1	8000	LP8000	ASB	Assembler;FORTRAN IV	GICB
91#	SW-LP8000#2	8000	LP8000	SIM	Simulator;FORTRAN IV	GICB
92	SW-HBASIC	1800	1802	LAN	Basic Language Interpreter;Runs on HMDS(HUGES uP Dev System)	HAC
93	SW-AN/UYK-30MDS	AN/UYK-30	AN/UYK-30	ASB	Cross Assembler in PLM, A PL/1 Like Language	HACC
94	SW-H18HLL	2901	H18	LAN	Higher Level Language META PLAN	HACC
95	SW-H18LL	2901	H18	LOA	Linking Loader	HACC
96	SW-H18MA	2901	H18	ASB	Macro Assembler	HACC
97	SW-H18SIM	2901	H18	SIM	Simulator	HACC
98	SW-HM6100	6100	HM6100	SSS	Compatible with PDP-8/E(TM Digital Equip Corp)	HAS
99	SW-BUG8	8080	H8	DEB	Term Console Debug Prog for Machine Lang Prog;Req 3k Mem and User Prog	HEA
100	SW-H8-13	8080	H8	BAS	Extended Benton Harbor BASIC;1200 Baud Audio Cass;Req Min 12k Mem	HEA
101	SW-H8-14	8080	H8	BAS	Extended Benton Harbor BASIC;Fan Fold Paper;Req Min 12k Mem	HEA
102	SW-H8-15	8080	H8	OPS	Fan Fold Paper Tape Sys;Incl BH BASIC,HASL8,TED8,BUG8;Use with H10,Etc	HEA
103	SW-HASL8	8080	H8	ASB	Two Pass Absolute Assembler;1200 Baud Audio Cass;Req Min 8k Mem	HEA
104	SW-TED8	8080	H8	EDT	Line Oriented Text Editor;1200 Baud Audio Cass;Req Min 8k Mem	HEA
105	SW-MLZ-BASIC	Z80	MLZ80	EDT	Basic Interpreter	HEU
106	SW-MLZ-EXEC	Z80	MLZ80	SSS	Floppy Disk File Management	HEU
107	SW-ZRAID	Z80	MLZ80	MON	ZRAID Monitor Debug;Compatible with Z80 and 8080	HEU
108	SW-MLP8700	8080	MLP8080	MON	Monitor	HEU
109	SW-MLP8702	8080	MLP8080	OPS	Disk Operating System	HEU
110	SW-MLP8704	8080	MLP8080	OPS	Real Time Operating System	HEU

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D.
(3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	[4] SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	[2] GENERIC I.D. $-MULTI- SYSTEM APPLICATION	[3] SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	[1] MFR. CODE
1	SW-MLP8710	8080	MLP8080	EDT	Text Editor	HEU
2	SW-MLP8720	8080	MLP8080	ASB	Macro Assembler	HEU
3	SW-MLP8730	8080	MLP8080	DEB	Debug Package with Trace	HEU
4	SW-MLP8740	8080	MLP8080	EDT	Basic Interpreter	HEU
5	SW-MLP8760	8080	MLP8080	EDT	Disc File Management System and Basic Interpreter	HEU
6	SW-MLP-BASIC	8080	MLP8080	EDT	Basic Interpreter	HEU
7	SW-MLP-EXEC	8080	MLP8080	SSS	Floppy Disk File Management	HEU
8#	SW-MNAS	40 Series	HMCS45	ASB	MNEMANIC Assembler;Program Language	HITJ
9#	SW-HITAC8500	40 Series	HMCS45,42	ASB	Cross Assembler/Simulator;for HMCS 45,44,43,43C and 42	HITJ
10#	SW-HITAC10/10II	40 Series	HMCS45,44	ASB	Cross Assembler/Simulator for HMCS45,44	HITJ
11#	SW-H68/SD20#1	6800	HMCS6800	OPS	Floppy Disk Operating System FDOS	HITJ
12#	SW-H68/SD20#2▼	6800	HMCS6800	MON	Monitor on 4kB ROM	HITJ
13#	SW-H68/SD20#3	6800	HMCS6800	ASB	Macro Assembler	HITJ
14#	SW-H68/SD20#4	6800	HMCS6800	EDT	Linkage Editor	HITJ
15#	SW-H68/SD20#5	6800	HMCS6800	EDT	Text Editor	HITJ
16#	SW-H68/SD20#6	6800	HMCS6800	CMP	PL/H Compiler	HITJ
17#	SW-H68/SD20#7	6800	HMCS6800	SSS	EPROM Writer	HITJ
18#	SW-H68/SD20#8	6800	HMCS6800	DIA	Adaptive System Evaluator	HITJ
19	SW-MX800#1	8080	MX800	LOA	Program Loader	ICC
20	SW-MX800#2	8080	MX800	DEB	Interactive Debugger	ICC
21	SW-MX800#3	8080	MX800	SUB	I/O Subroutine	ICC
22	SW-MX800#4	8080	MX800	EDT	Editor	ICC
23	SW-MX800#5	8080	MX800	ASB	Assembler	ICC
24	SW-MX800#6	8080	MX800	SSS	PROM Programming Software Package	ICC
25	SW-BASIC9A	8080	PCS-80	LAN	9k Audio Cassette BASIC;Available in Paper Tape,Cassette	IMS
26	SW-BASIC9B	8080	PCS-80	LAN	CP/M Version of BASIC;Available in Diskette	IMS
27	SW-BASIC-C	8080	PCS-80	LAN	Commercial Disk BASIC;Available in Diskette	IMS
28	SW-FORTRANIV3.05	8080	PCS-80	CMP	FORTRAN IV Version 3.05 Compiler Meeting ANSI Standard	IMS
29	SW-IMDOS	8080	PCS-80	OPS	Multi-Disk Operating System Ind Editor,Utility,Diagnostics,Assembler	IMS
30	SW-PGM2A	8080	PCS-80	OPS	Tape Cassette Operating System;TARBELL Standard;Avail in Cass,EPROM	IMS
31	SW-6980-ILIST	6100	INTERCEPT	SSS	Listing for Software Component 6980-ISOFT	INL
32	SW-6980-ISOFT	6100	INTERCEPT	OPS	Software Component for Floppy Disk Operating System 6970-IFDOS	INL
33	SW-6981-FOPAL-III	6100	INTERCEPT	ASB	FORTRAN Cross Assembler for PALIII	INL
34	SW-6982-IS-LFOCA	6100	INTERCEPT	LAN	Focal-8(TM Digital Equip Corp)Interactive Algebraic Lang for 4k Mem	INL
35	SW-6982-QFO81-AC	6100	INTERCEPT	MFS	Extended Software Kit on Paper Tape;Compatible with PDP-8/E	INL
36	SW-6985-IDIAG-1	6100	INTERCEPT	DIA	Diagnostics for Intercept System	INL
37	SW-6985-IDIAG-2	6100	INTERCEPT	DIA	Diagnostics for Extended Memory Controller Module 6907-EMC	INL
38	SW-6985-IDIAG-3	6100	INTERCEPT	DIA	Diagnostic Software for Floppy Disk System 6970-IFDOS	INL
39	SW-IM6100	6100	6100	SSS	Compatible with PDP-8/E (TM Digital Equip Corp)	INL
40	SW-MDS-ICE49	MULTI$	INTELLEC800	SIM	MCS-48 In-Circuit Emulator	ITL
41	SW-INTERP40	MULTI$	MCS4,40	SIM	4004/4040Simulator:ANSI,FORTRAN IV:Large Scale Comp,Timeshare Serv	ITL
42	SW-PL/M	MULTI$	MCS8,80,85	CMP	Cross Compilers;ANSI,FORTRAN IV;Large Scale Comp,Time Serv8008/8080/85	ITL
43	SW-INTERP80	MULTI$	MCS80,85	SIM	8080 Simulator:FORTRAN IV;Timesharing Services 8080/8085	ITL
44	SW-MAC80	MULTI$	MSC80,85	ASB	Cross MACRO Assembler;FORTRAN IV:Lg Scale Comp,Timeshare Serv8080/8085	ITL
45	SW-CROMIS	3000	3000	ASB	Cross Microprogramming System;ANSI,FORTRAN IV	ITL
46	SW-MAC40	4040	MCS40	ASB	Cross MACRO Assembler:ANSI,FORTRAN IV:Large Scale,Tymshare,United Comp	ITL
47	SW-INTERP8	8008	MCS8	SIM	8008 Simulator:FORTRAN IV;Timesharing Services	ITL
48	SW-MAC8	8008	MCS8	ASB	Cross Assembler;ANSI,FORTRAN IV;Large Scale Computer,Timeshare Serv	ITL
49	SW-PL/M8	8008	MCS8	CMP	High Level Language Compiler;Translates to MCS8 Machine Code	ITL
50	SW-MDS320	8080	INTELLEC800	EDT	Basic-80 Extended ANS 1978 Basic Intellec Resident Interpreter	ITL
51	SW-MDS-D48	8080	INTELLEC800	MFS	MCS48 Disk Support Pkg:Includes Assembler ICE48,PROM Mapper Software	ITL
52	SW-MDS-ICE30	8080	INTELLEC800	Sim	3001 In-Circuit Emulator	ITL
53	SW-MDS-ICE48	8080	INTELLEC800	SIM	Development Software:8748 In-Circuit Emulator	ITL
54	SW-MDS-ICE80	8080	INTELLEC800	SIM	In-Circuit Emulator	ITL
55	SW-MDS-ICE85	8080	INTELLEC800	SIM	Development Software:8085 In-Circuit Emulator	ITL
56	SW-MDS-P48	8080	INTELLEC800	ASB	MCS48 Paper Tape Assembler	ITL
57	SW-MDS-PLM	8080	INTELLEC800	CMP	High Level Language Compiler Resident on INTELLEC System	ITL
58	SW-MDS-SIM100	8080	INTELLEC800	SIM	Bipolar ROM Simulator	ITL
59	SW-MDS-SIM101	8080	INTELLEC800	SIM	8k Bit Bipolar ROM Simulator;For Simulating 3601/3301 ROMs	ITL
60	SW-MDS-SIM102	8080	INTELLEC800	SIM	8k Bit Bipolar ROM Simulator;For Simulating 3602/3622/3302/3322	ITL
61	SW-MDS-SIM104	8080	INTELLEC800	SIM	8k Bit Bipolar ROM Simulator;For Simulating 3604/3624/3304A	ITL
62	SW-PL/M80	8080	MCS80	CMP	High Level Language Compiler;Translates to MCS80 Machine Code	ITL
63	SW-RMX/80	8080	MCS80	MON	Real Time Multi-task Executive Software:Operates on SBC80 and Sys 80	ITL
64	SW-SBC915▼	8080	MCS80	MON	GO/NO-GO Diskette Diag/Monitor Program on 4 ROMs	ITL
65	SW-SBC925▼	8080	MCS80	MON	GO/NO-GO Diskette Diag/Monitor Program on 4 ROMs	ITL
66	SW-MDS301	8080	MCS80,85	CMP	8080/8085 ANS 1977 FORTRAN Compiler,Requires MDS800 or MDS230	ITL
67	SW-MDS-ICE86	8086	INTELLEC800	SIM	8086 In-Circuit Emulator	ITL
68	SW-MDS311	8086	MCS86	CMP	Hi Level Lang Cross Compiler in Intellec Syst;PLM86 to 8086 Mach Code	ITL
69▼#	SW-COBOL80	Z80$	Z80	CMP	Consists 2 Comp Pkg;Compiler/Trans;Run Time Sys for Running Prog.	MATC
70▼#	SW-CP/M2.0	Z80$	Z80,8080	DOS	Support Text Editor,Assem,Debugger Sybsys;High-Level Language	MATC
71▼#	SW-FORTRAN80#1	Z80$	Z80,8080	CMP	Runs Under CP/M2.0;Comp s 100 s Statements/min;MACRO80/LINK80 Included	MATC
72#	SW-MTX-ALPHA	8080	2480	ASB	Program Occupies 3K Memory Will Work w/MT-2480,ALT-2480,MSBC-2480	MATC
73#	SW-C1400	1400	MN1400	ASB	J I S 5000 Level FORTRAN Cross Assembler	MATJ
74#	SW-L1400	1400	MN1400	ASB	Cross Assembler with PANAFACOM L-16A	MATJ
75	SW-MASMF8	F8	F8	ASB	Macro Assembler for Fairchild F8 (FORTRAN Cross Assembler)	MCT
76	SW-SIMF8	F8	F8	SIM	Simulator for Fairchild F8 (FORTRAN Cross Simulator)	MCT
77	SW-ASM40	MULTI$	MCS4,40	ASB	Assembler for Intel 4004/4040(FORTRAN Cross Assembler)	MCT
78	SW-MASM40	MULTI$	MCS4,40	ASB	Macro Assembler for Intel 4004/4040 (FORTRAN Cross Assembler)	MCT
79	SW-SIM40	MULTI$	MCS4,40	SIM	Simulator for Intel 4004/4040 (FORTRAN Cross Simulator)	MCT
80	SW-MASM80	MULTI$	MCS80,85	ASB	Macro Assembler for Intel 8080/8085 (FORTRAN Cross Assembler)	MCT
81	SW-SIM80	MULTI$	MCS80,85	SIM	Simulator for Intel 8080/8085 (FORTRAN Cross Simulator)	MCT
82	SW-META29	MULTI$	2900,3000	ASB	Meta Assembler for AMD 2900,Intel 3000 etc (Cross Assembler)	MCT
83	INTZ8	Z80	Z80		Interactive Simulator For Z80;Family	MCT
84	SW-MASMZ8R	Z80	Z80	ASB	Relocatable Macro Assembler for Z80 and Linking Loader(Cross Assembl)	MCT
85	SW-SIMZ8	Z80	Z80	SIM	Simulator for Z80 Microprocessor (Cross Simulator)	MCT
86	SW-CONV	Z80	Z80-MCS	ASB	Conversion Program from 8080 to Z80	MCT
87	SW-MASMZ8	Z80	Z80-MCS	ASB	Macro Assembler for Zilog/MOSTEK Z80(FORTRAN Cross Assembler)	MCT
88	SW-AZ8000R	Z8000	Z8000	ASB	Relocatable Marco Assembler For Zilog Z8000 (Fortran Cross Assemb)	MCT
89	SW-IZ8000	Z8000	Z8000	SIM	Simulator For Zilog Z8000 (Fortran Cross Simulator)	MCT
90	SW-MASM18	1802	CDP1802	ASB	Macro Assembler for RCA 1802 (FORTRAN Cross Assembler)	MCT
91	SW-A1802R	1802	1802	ASB	Relocatable Marco Assembler For RCA 1802 (Fortran Cross Assemb)	MCT
92	SW-SIM18	1802	1802	SIM	Simulator for Signetics 1802 (FORTRAN Cross Simulator)	MCT
93	SW-MASM26	2650	2650	ASB	Macro Assembler for Signetics 2650 (FORTRAN Cross Assembler)	MCT
94	SW-SIM26	2650	2650	SIM	Simulator for Signetics 2650 (FORTRAN Cross Simulator)	MCT
95	MASM65R	6500	MCS6500		Relocatable Assembler For 6500;Written In Fortran	MCT
96	SW-MASM65	6502	MCS6500	ASB	Macro Assembler for MOS Technology 650X(FORTRAN Cross Assembler)	MCT
97	MASM68R	6800	M6800		Relocatable Assembler For 6800;Written In Fortran	MCT
98	SW-MASM68	6800	M6800	ASB	Macro Assembler for Motorola 6800 (FORTRAN Cross Assembler)	MCT
99	SW-SIM68	6800	M6800	SIM	Simulator for Motorola 6800 (FORTRAN Cross Simulator)	MCT
100	SW-I6800	6800	6800	SIM	Simulator For Motorola 6800 (Fortran Cross Simulator)	MCT
101	SW-A6805R	6805	6805	ASB	Relocatable Marco Assembler For Motorola 6805 (Fortran Cross Assemb)	MCT
102	SW-A6809R	6809	6809	ASB	Relocatable Marco Assembler For Motorola 6809 (Fortran Cross Assemb)	MCT
103	SW-MASM41	8041	MCS41	ASB	Macro Assembler for 8041 Microprocessor (Cross Assembler)	MCT
104	SW-MASM48	8048	MCS48	ASB	Macro Assembler for Intel 8048 (FORTRAN Cross Assembler)	MCT
105	SW-SIM48	8048/49	MCS48	SIM	Simulator for 8048/8049 Microprocessor (Cross Simulator)	MCT
106	INT48	8048,8041	MCS48,41		Interactive Simulator For 8048;Family	MCT
107	SW-LOAD80	8080	INTELLEC800	LOA	MDS Resident Loader for MASM80R on Diskette	MCT
108	SW-ASM80	8080	MCS80	ASB	Assembler for Intel 8080 (FORTRAN Cross Assembler)	MCT
109	SW-MASM80R	8080	MCS80	ASB	Relocatable Macro Assembler for 8080 and Linking Loader (CrossAssembl)	MCT
110	SW-P816A▼	8080	MCS80	MFS	Assembler/Editor/Monitor for Intel SBC 80/10 and MDS on PROM Board	MCT

SYMBOLS AND CODES
EXPLAINED IN INTERPRETER

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	1 MFR. CODE
1	INT80	8080,8085	MCS80,85		Interactive Simulator For 8080;Family	MCT
2	SW-MASM99	9900	990	ASB	Macro Assembler for T.I.990(FORTRAN Cross Simulator)	MCT
3	SW-MICRO1#1	MICRO1	MICRO1	ASB	Machine Language Symbolic Assembler	MID
4	SW-MICRO1#10	MICRO1	MICRO1	ASB	Cross Micro Assembler;In FORTRAN	MID
5	SW-MICRO1#11	MICRO1	MICRO1	SIM	Cross Micro Simulator;In FORTRAN	MID
6	SW-MICRO1#12	MICRO1	MICRO1	SSS	I/C Memory MAP Generators for Control Memory Bit Patterns	MID
7	SW-MICRO1#13▼	MICRO1	MICRO1	SSS	Standard 21 Firmware Set	MID
8	SW-MICRO1#2	MICRO1	MICRO1	SSS	Utility Programs	MID
9	SW-MICRO1#3	MICRO1	MICRO1	LOA	Teletype Operating System	MID
10	SW-MICRO1#4	MICRO1	MICRO1	EDT	Tape Editor Program	MID
11	SW-MICRO1#5	MICRO1	MICRO1	DIA	Diagnostics for CPU;Memory and System Peripherals	MID
12	SW-MICRO1#6	MICRO1	MICRO1	SUB	I/O Drivers (Callable Subroutines) for System Peripherals	MID
13	SW-MICRO1#7	MICRO1	MICRO1	OPS	Alterable Control Operating System (ACOS)	MID
14	SW-MICRO1#8	MICRO1	MICRO1	ASB	Micro Language Assembler	MID
15	SW-MICRO1#9	MICRO1	MICRO1	SIM	Micro Simulator	MID
16	SW-CORRESPONDER	MULTI$	MCS80,Z80	SSS	Corresponder:To Maintain Demographically Coded Mailing Lists	MIP
17	SW-SUPERSORT	MULTI$	MCS80,Z80	SSS	Sort/Merge Software:Bench Marked at 560 Records/Min,Various Data Types	MIP
18	SW-TEX	MULTI$	MCS80,Z80	SSS	Output Formatter:TEX is TM of Digital Research	MIP
19	SW-WORDMASTER	MULTI$	MCS80,Z80	EDT	Text Editor;Comp with Cp/M,Dumb CRT W/Addr Cursor,Bi-Direct Word/Line	MIP
20#	SW-GBIAS0001	8080	MELPS4	ASB	CrossAssembler (MELCOM 70)	MITJ
21#	SW-GBIAS0002	8080	MELPS4	ASB	CrossAssembler (MELCOM 7000,COSMO 700)	MITJ
22#	SW-GBISM0001	8080	MELPS4	SIM	Simulator (MELCOM 70)	MITJ
23#	SW-GBISP0001	8080	MELPS4	SSS	Papertape Program for PROM Writer (MELCOM 70)	MITJ
24#	SW-GBISP0002	8080	MELPS4	SSS	Papertape Program for PROM Writer (MELCOM 7000,COSMO 700)	MITJ
25#	SW-GBIAS0003	8080	MELPS41	ASB	CrossAssembler (MELCOM 70)	MITJ
26#	SW-GBISM0002	8080	MELPS41	SIM	Simulator (MELCOM 70)	MITJ
27#	SW-GBISP0003	8080	MELPS41	SSS	Papertape Program for PROM Writer (MELCOM 70)	MITJ
28#	SW-GA1AS0100	8080	MELPS8	ASB	MELPS8 Cross Assembler:Host Program FORTRAN IV on MT,MELCOM70	MITJ
29#	SW-GA1SM0100	8080	MELPS8	SIM	MELPS8 Simulator:Host Program FORTRAN IV on MT,Runs on MELCOM70	MITJ
30#	SW-GA1SP0100	8080	MELPS8	SSS	MELPS8 Paper Tape for PROM Writers Generation Program on MELCOM70	MITJ
31#	SW-GA1TL0400	8080	MELPS8	CMP	MELPS8 PL/1U Cross Compiler:Host Program FORTRAN IV on MT,MELCOM7000	MITJ
32#	SW-GA2AS0100	8080	MELPS8	ASB	MELPS8 Self Assembler:Target Program on Paper Tape	MITJ
33#	SW-GA2SB0100	8080	MELPS8	SUB	MELPS8 Subroutine 1:Integer Arithmetic Operations;Target Progm on PT	MITJ
34#	SW-GA2SP0103	8080	MELPS8	EDT	MELPS8 Editor:Target Program on Paper Tape	MITJ
35#	SW-GA20S0100	8080	MELPS8	MON	MELPS8 Basic Operating Monitor BOM-PTS:Target Program On Paper Tape	MITJ
36#	SW-GA20S0101	8080	MELPS8	MON	MELPS8 Basic Operating Monitor BOM-B:Target Program On Paper Tape	MITJ
37#	SW-M58730-001S▼	8080	MELPS8	SUB	Integer Arithmetic Routine Resident on 8k ROM	MITJ
38#	SW-M58731-001S	8080	MELPS8	MON	MELPS8 Monitor BOM-B Resident on 16k ROM	MITJ
39#	SW-GAISM0110	8080	MELPS8/85	SIM	Simulator Programming for FORTRAN	MITJ
40#	SW-GAITL0100	8080	MELPS8/85	CMP	Crosscompiler (MELCOM 7000-B) for FORTRAN IV	MITJ
41	SW-MMI300	MICRO1	300	SSS	Software Compatible with NOVA(TM-Data Gen Corp)Series Computers	MMI
42	SW-MMI350#1	MICRO1	300	DIA	Exercisor;For Testing CPU,Clock,Teletype/Hi Speed Reader/Punch	MMI
43	SW-MMI350#2	MICRO1	300	LOA	Binary Loader;Available in Paper Tape	MMI
44	SW-MMI350#3	MICRO1	300	DEB	Debug;Available in Paper Tape	MMI
45	SW-MMI350FW▼	MICRO1	300	MFS	Exerciser;Binary Loader;Debug in 4k x 16 of PROM on PCB	MMI
46	SW-MMI600	MICRO1	600	SSS	Software Compatible with NOVA (TM-Data Gen Corp) Series Computers	MMI
47	SW-MMI600#1	MICRO1	600	EDT	Editor	MMI
48	SW-MMI600#2	MICRO1	600	ASB	Assembler	MMI
49	SW-MMI600#3	MICRO1	600	LOA	Loader	MMI
50	SW-MMI600#4	MICRO1	600	DEB	Debug	MMI
51	SW-MMI600#5	MICRO1	600	LAN	High Level Languages;ALGOL,BASIC,COBAL,FORTRAN	MMI
52	SW-MMI67110	6701	6701	ASB	FORTRAN IV Cross-Assmbl for ANSI Compiler:Large/Med Mach/Time Sharing	MMI
53	SW-MK79012	F8	F8-MOS	ASB	F8 FORTRAN IV Cross Assembler;Executes on 16 Bit Word Length Medium	MOS
54	SW-MK79056▼	F8	F8-MOS	SSS	MK3870/14001 Firmware Pkg;Preprogrammed 3870 Used W/VAB-2	MOS
55	SW-MK79079	F8	F8-MOS	ASB	AID-80F Cross Assembler for 3870/F8 Microcomputers	MOS
56	SW-MK79083	F8	F8-MOS	SSS	Cassette Tape Based AIM-72 SW For Use W/Silent 700 Terminal,SDB-50/70	MOS
57▼	SW-MK77962	Z80	FLP-80DOS	ASB	Includes Monitor/Debugger/Text Editor/Z80 Assembler/Relocating Link	MOS
58▼	SW-MK78142	Z80	FLP-80DOS	ASB	Includes Monitor/Debugger/Text Editor/Z80 Assembler/Relocating Link	MOS
59▼	SW-MK78197	Z80	MATRIX-80	DEB	Paper Tape Readers Punches Card Readers Line Printer	MOS
60▼	SW-MK77968	Z80	MEDEX-80	MON	Software/Diagnostic;System Consists of Initial Monitor/Card Handler	MOS
61▼	SW-MK77972	Z80	MITE-80	DEB	Multi Task Executive;Debugger;Marco Files ETC	MOS
62	SW-MK78117C	Z80	Z80	ASB	XFOR-80 FORTRAN IV Cross Assy Requires 20k 16 Bit Words Card Deck	MOS
63	SW-MK78117P	Z80	Z80	ASB	Same as SWMK78117C Except Paper Tapes	MOS
64	SW-MK78157	Z80	Z80	EDT	Basic Software Interpreter	MOS
65	SW-MK78158	Z80	Z80	LOA	FORTRAN IV Compiler	MOS
66	SW-MK78164	Z80	Z80	LOA	FLP-80DOS Software Library Vol 1 Including Source Object and Binary	MOS
67	SW-MK78165	Z80	Z80		Z80 MACRO Assembler Requires 32k Bytes	MOS
68	SW-MK79075	Z80	Z80		NON-MACRO 3870 Assembler	MOS
69	SW-MK79082	Z80	Z80		Driver Software for SDB80 SDB-50/70 AID-80F and Sys-80F	MOS
70	SW-MK79084	Z80	Z80		SWD-2 PPG-8/16 Object Programs on Silent 700 Cassette Tapes	MOS
71	SW-MK79085	Z80	Z80		Syntax Compatible to the MACRO-80	MOS
72	SW-ASMB-80▼	Z80	Z80-MOS	ASB	ASMB-80 Resident Assembler and Text Editor in 4 MK 34000 2kx8 ROMS	MOS
73	SW-DDT-80▼	Z80	Z80-MOS	OPS	DDT 80 Operating System in One MK34000 2kx8 ROM	MOS
74	SW-EDIT-80▼	Z80	Z80-MOS	EDT	Resident Z80 Text Editor	MOS
75	SW-FLP-80DOS	Z80	Z80-MOS	OPS	Disk Based Development System for Z80	MOS
76	SW-MK78117	Z80	Z80-MOS	ASB	Z80-FORTRAN Cross-Assembler;Supplied as a Source Deck	MOS
77	SW-MK78134	Z80	Z80-MOS	MON	Dual Floppy Disks	MOS
78	SW-MK78135	Z80	Z80-MOS	MFS	Z80 Development System Software (DSS-80):Includes Assemb,Editor Etc	MOS
79	SW-MK78136	Z80	Z80-MOS	OPS	Z80 Disk Operating Software (DOPS-80):Disk Controller,FD Handler	MOS
80	SW-MK78534	Z80	Z80-MOS	LAN	Complete Assembly Language Source Listing With Comments	MOS
81	SW-MK78536	Z80	Z80-MOS	LAN	Complete Assembly Language Source Listing of ASMB-80 Firmware Package	MOS
82	SW-MEX3870M▼	3870	MC3870	SIM	ROM Resident Emulator for Program Development of MC3870 Microcomputer	MOTA
83▼	SW-M68MM19SB	6800	MC6809	MFS	6k EPROM,Contains SUPERmon,SUPERlink,SUPERio,and SUPERutil	MOTA
84▼	SW-MEK6802EAC	6800	MEK6802	EDT	Editor/Assembler:300 Baud Audio Cassette;Runs Under CRTBUG or D3BUG2	MOTA
85▼	SW-MEK6802EAE	6800	MEK6802	EDT	Editor/Assembler:8-Programmed EPROMs;Runs Under CRTBUG or D3BUG2	MOTA
86	SW-HELP	6800	M6800	OPS	Time Sharing System Software:HELP:File System for Hardware/Software	MOTA
87	SW-JBUG▼	6800	M6800	MAN	Monitor Firmware of Evaluation Kit II MEK6800D2	MOTA
88	SW-M68ASMR010	6800	M6800	ASB	Resident Macro Assembler and Linking Loader;On Cassette,PT,Diskette	MOTA
89	SW-M68ASMR012	6800	M6800	ASB	Co-Resident Assembler for EXORciser;On Cassette,Paper Tape,Diskette	MOTA
90	SW-M68ASMR013	6800	M6800	ASB	EXORciser Resident Assmblr onCassette(A),Paper Tape(B),MDOS Diskett(M)	MOTA
91	SW-M68ASMR020	6800	M6800	ASB	Resident Macro Assembl/Linkage Editor;On Cassette,PaperTape,FloppyDisk	MOTA
92	SW-M68ASMR021D	6800	M6800	ASB	Resident Macro Assembler and Linking Loader;On Diskette	MOTA
93	SW-M68ASMR212	6800	M6800	ASB	Co-Resident Assembler for Evaluation Mod II;On Cassette,Paper Tape	MOTA
94	SW-M68BASR010	6800	M6800	EDT	EXORciser Resident BASIC Interpreter on Cassette(A),Paper Tape(B),MDOS	MOTA
95	SW-M68BASRC1▼	6800	M6800	EDT	BASIC Interpreter ROM Set	MOTA
96	SW-M68BASRM1▼	6800	M6800	EDT	EXORciser Resident BASIC Interpreter in ROM	MOTA
97	SW-M68CLIB1	6800	M6800	SUB	M6800 User Group Library Program 1-13;Casette	MOTA
98	SW-M68CLIB2	6800	M6800	SUB	M6800 User Group Library Program 14-25;Casette	MOTA
99	SW-M68CLIB3	6800	M6800	SUB	M6800 User Group Library Program 26-31;Casette	MOTA
100	SW-M68CLIB4	6800	M6800	SUB	M6800 User Group Library Program 32-47;Casette	MOTA
101	SW-M68CLIB5	6800	M6800	SUB	M6800 User Group Library Program 48-53;Casette	MOTA
102	SW-M68CLIB6	6800	M6800	SUB	M6800 User Group Library Program 54-64;Casette	MOTA
103	SW-M68CLIB7	6800	M6800	SUB	M6800 User Group Library Program 65-75;Casette	MOTA
104	SW-M68CLIB8	6800	M6800	SUB	M6800 User Group Library Program 76-82;Casette	MOTA
105	SW-M68CLIB9	6800	M6800	SUB	M6800 User Group Library Program 83-90;Casette	MOTA
106	SW-M68CLIB10	6800	M6800	SUB	M6800 User Group Library Program 91-100;Casette	MOTA
107	SW-M68CLIB11	6800	M6800	SUB	M6800 User Group Library Program 101-110;Casette	MOTA
108	SW-M68CLIB12	6800	M6800	Sub	M6800 User Group Library Program 111-115; Casette	MOTA
109	SW-M68CLIB13	6800	M6800	SUB	M6800 User Group Library Program 116-122;Casette	MOTA
110	SW-M68CLIB14	6800	M6800	SUB	M6800 User Group Library Program 123-125;Casette	MOTA

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

4.SYSTEM SOFTWARE INDEX

IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D.
(3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATE-GORY	S O F T W A R E L I B R A R Y NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	1 MFR. CODE
1	SW-M68COBOL010M	6800	M6800	CMP	Resident ANS COBOL Compiler:Media MDOS Diskette	MOTA
2	SW-M68EAB1▼	6800	M6800	ASB	Editor/Assembler Basic Module:14k ROM Resident M68ADS2A Plug-in Compat	MOTA
3	SW-M68EAB2	6800	M6800	MFS	Resident ROM BASIC Interpreter;Editor/Assembler and BASIC EPROMs;Mod	MOTA
4	SW-M68EAE6812	6800	M6800	ASB	Co-Resident Assembler/Editor for Evalu MOD I;On Cassette,PaperTape	MOTA
5	SW-M68EAM1▼	6800	M6800	ASB	Editor/Assembler Module:7k ROM Resident,M68ADS2A Plug-in Compatible	MOTA
6	SW-M68EDTR012	6800	M6800	EDT	Co-Resident Editor for EXORciser;On Cassette,Paper Tape,Diskette	MOTA
7	SW-M68EDTR013	6800	M6800	EDT	EXORciser Resident Editor on Cassette(A),Paper Tape(B),MDOS Diskett(M)	MOTA
8	SW-M68EDTR212	6800	M6800	EDT	Co-Resident Editor for Evaluation MOD II;On Cassette,Paper Tape	MOTA
9	SW-M68EML	6800	M6800	SIM	Simulator;On Cards,Mag Tapes;Multiple(7) Computer Compatability	MOTA
10	SW-M68FTNR010D	6800	M6800	CMP	Resident FORTRAN Compiler	MOTA
11	SW-M68FTNR012D	6800	M6800	CMP	Resident FORTRAN Compiler-Floppy Disk EDOS,FloppyDisk-MDOS also Avail	MOTA
12	SW-M68FTNR012M	6800	M6800	CMP	EXORciser Resident FORTRAN Compiler and Linking Loader on MDOS Diskett	MOTA
13	SW-M68IOS1▼	6800	M6800	MON	I/O Supervisor Firmware:For Program Development,Part of M68ADS1A/2A	MOTA
14▼	SW-M68KOXPASCL1	6800	M6800	CMP	CROSS PASCAL on Diskette for M6809 MDOS;Supports Structural Prog	MOTA
15▼	SW-M68KOXPASCL2	6800	M6800	CMP	CROSS PASCAL on Magnetic Tape for IBM 370;Supports Structural Prog	MOTA
16	SW-M68LIB1E	6800	M6800	SUB	M6800 User Group Library Program 1-25;EDOS Diskette	MOTA
17	SW-M68LIB1M	6800	M6800	SUB	M6800 User Group Library Program 1-25; MDOS Diskette	MOTA
18	SW-M68LIB2E	6800	M6800	SUB	M6800 User Group Library Program 26-50;EDOS Diskette	MOTA
19	SW-M68LIB2M	6800	M6800	SUB	M6800 User Group Library Program;26-50;MDOS Diskette	MOTA
20	SW-M68LIB3E	6800	M6800	SUB	M6800 User Group Library Program 51-75;EDOS Diskette	MOTA
21	SW-M68LIB3M	6800	M6800	SUB	M6800 User Group Library Program 51-75;MDOS Diskette	MOTA
22	SW-M68LIB4E	6800	M6800	SUB	M6800 User Group Library Program 76-90;EDOS Diskette	MOTA
23	SW-M68LIB5E	6800	M6800	SUB	M6800 User Group Library Program 91-125;EDOS Diskette	MOTA
24	SW-M68LIB5M	6800	M6800	SUB	M6800 User Group Program 91-125;MDOS Diskette	MOTA
25	SW-M68LIBA1E	6800	M6800	SUB	M6800 User Group Library Program 1-125;EDOS Diskette	MOTA
26	SW-M68LIBA1M	6800	M6800	SUB	M6800 User Group Library Program1-125;MDOS Diskette	MOTA
27	SW-M68MAE6813A	6800	M6800	MFS	Editor/Assembler on Casette for Use w/MICRObug	MOTA
28	SW-M68MAE6813B	6800	M6800	MFS	Editor/Assembler on Paper Tape for Use w/MICRObug	MOTA
29	SW-M68MASR010	6800	M6800	ASB	EXORciser Relocatable Macro-Assembler on Cassette,PaperTape,Diskette	MOTA
30	SW-M68MM08A▼	6800	M6800	DEB	ROM W/MICRObug Monitor/Debug Functions;Used W/M68MM01A/M68MM01A2	MOTA
31	SW-M68MM12ASWM	6800	M6800	SUB	Source Code on MDOS Diskette to Implement GPIB Listen/Talker Protocol	MOTA
32	SW-M68MM12SWM	6800	M6800	SUB	Source Code on MDOS Diskette of On-B-d EPROM,Impl of GPIB Protocol	MOTA
33	SW-M68MODOS010	6800	M6800	OPS	Floppy Disk Op Sys;Incl Obj Codes;I/O Addr Ch;Source/Obj Code for Cont	MOTA
34	SW-M68MPLC#1	6800	M6800	CMP	Cross Compiler;On Cards,Mag Tapes;Multiple(4) Computer Compatibility	MOTA
35	SW-M68MPLC#2	6800	M6800	OPS	Time Sharing System Software;Cross Compiler	MOTA
36	SW-M68MPLR010M	6800	M6800	CMP	Resident MPL Compiler:Based on PL/I,EXORciser/EXORterm Resident	MOTA
37	SW-M68SAM	6800	M6800	ASB	Cross Assembler;On Cards,Mag Tapes;Multiple (7)Computer Compatibility	MOTA
38	SW-M68UG2	6800	M6800	SUB	Paper Tape Lib,Prog 2;Exbug Routine INCHNP	MOTA
39	SW-M68UG3	6800	M6800	SUB	Paper Tape Lib,Prog 3;Exbug Rooutine INCH	MOTA
40	SW-M68UG4	6800	M6800	SUB	Paper Tape Lib,Prog 4;EXbug Routine OUTCH	MOTA
41	SW-M68UG5	6800	M6800	SUB	Paper Tape Lib,Prog 5;EXbug Routine PDATA	MOTA
42	SW-M68UG6	6800	M6800	Sub	Paper Tape Lib,Prog 6;Binary to Decimal ASCII Conversion	MOTA
43	SW-M68UG7	6800	M6800	SUB	Paper Tape Lib,Prog 7;High Speed Double Precision Multiply	MOTA
44	SW-M68UG8	6800	M6800	SUB	Paper Tape Lib,Prog 8;Reentrant 16-Bit Divide	MOTA
45	SW-M68UG9	6800	M6800	SUB	Paper Tape Lib,Prog 9;Reentrant Double Precision Mulitply	MOTA
46	SW-M68UG10	6800	M6800	SUB	Paper Tape Lib,Prog 10;M6800 Resident I/O Pkg-EXbug Version	MOTA
47	SW-M68UG11	6800	M6800	SUB	Paper Tape Lib,Prog 11;M6800 Resident I/O Pkg-MIKbug Version	MOTA
48	SW-M68UG12	6800	M6800	SUB	Paper Tape Lib,Prog 12;MPU Instruction Test	MOTA
49	SW-M68UG13	6800	M6800	SUB	Paper Tape Lib,Prog 13;Memory Test	MOTA
50	SW-M68UG14	6800	M6800	SUB	Paper Tape Lib,Prog 14;PIA TEST	MOTA
51	SW-M68UG15	6800	M6800	SUB	Paper Tape Lib,Prog 15;32-Bit Reentrant Floating Point Multiply	MOTA
52	SW-M68UG16	6800	M6800	SUB	Paper Tape Lib,Prog 16;High Density Tape Load	MOTA
53	SW-M68UG17	6800	M6800	SUB	Paper Tape Lib,Prog 17;High Density Tape Punch	MOTA
54	SW-M68UG18	6800	M6800	SUB	Paper Tape Lib,Prog 18;LPOUT	MOTA
55	SW-M68UG19	6800	M6800	SUB	Paper Tape Lib,Prog 19;Interdata Cross Assembler	MOTA
56	SW-M68UG20	6800	M6800	SUB	Paper Tape Lib,Prog 20;Tic-Tac-Toe	MOTA
57	SW-M68UG21	6800	M6800	SUB	Paper Tape Lib,Prog 21;Punch for Data I/O PROM Programmer	MOTA
58	SW-M68UG22	6800	M6800	SUB	Paper Tape Lib,Prog 22;BCD to Binary Conversion	MOTA
59	SW-M68UG23	6800	M6800	SUB	Paper Tape Lib,Prog 23;Square Root of a 16-Bit Number	MOTA
60	SW-M68UG24	6800	M6800	SUB	Paper Tape Lib,Prog 24;UPC Label Conversion	MOTA
61	SW-M68UG25	6800	M6800	SUB	Paper Tape Lib,Prog 25;ASCII Data to Morse Code Conversion	MOTA
62	SW-M68UG26	6800	M6800	SUB	Paper Tape Lib,Prog 26;32-Bit Floating Point Pkg	MOTA
63	SW-M68UG27	6800	M6800	SUB	Paper Tape Lib,Prog 27;Random Number Generator	MOTA
64	SW-M68UG28	6800	M6800	Sub	Paper Tape Lib,Prog 28; Punch for PROLOG Ser 90 PROM Programmer	MOTA
65	SW-M68UG29	6800	M6800	SUB	Paper Tape Lib,Prog 29;M6800 Real-Time Operating Sys	MOTA
66	SW-M68UG30	6800	M6800	SUB	Paper Tape Lib,Prog 30;Blackjack	MOTA
67	SW-M68UG31	6800	M6800	SUB	Paper Tape Lib,Prog 31;Binary to BCD Conversion	MOTA
68	SW-M68UG32	6800	M6800	SUB	Paper Tape Lib,Prog 32;Decimal Arith Pkg	MOTA
69	SW-M68UG33	6800	M6800	SUB	Paper Tape Lib,Prog 33;Delay Subroutine	MOTA
70	SW-M68UG36	6800	M6800	SUB	Paper Tape Lib,Prog 36; Christmas Card List	MOTA
71	SW-M68UG37	6800	M6800		Paper Tape Lib,Prog 37;Reentrant ASCII to Baudot Conv.Subroutine	MOTA
72	SW-M68UG38	6800	M6800	SUB	Paper Tape Lib,Prog 38; Text String (TXTSTG)	MOTA
73	SW-M68UG39	6800	M6800	SUB	Paper Tape Lib,Prog 39; Dump/Hex/Display	MOTA
74	SW-M68UG41	6800	M6800	SUB	Paper Tape Lib,Prog 41; Mem Dump to Disk (FDISK)	MOTA
75	SW-M68UG43	6800	M6800	SUB	Paper Tape Lib,Prog 43; DEBUG	MOTA
76	SW-M68UG44	6800	M6800	SUB	Paper Tape Lib,Prog 44;Towers of Hanoi Solution	MOTA
77	SW-M68UG45	6800	M6800	SUB	Paper Tape Lib,Prog 45;WL*03(Wire Lister)	MOTA
78	SW-M68UG46	6800	M6800	SUB	Paper Tape Lib,Prog 46;Non-Linear Conversion Tables(CVTBLS)	MOTA
79	SW-M68UG47	6800	M6800	SUB	Paper Tape Lib,Prog 47;Assemb/Edt Internal Transfer Routine Exbug	MOTA
80	SW-M68UG48	6800	M6800	SUB	Paper Tape Lib,Prog 48;Biorythm	MOTA
81	SW-M68UG49	6800	M6800	SUB	Paper Tape Lib,Prog 49;Trace	MOTA
82	SW-M68UG50	6800	M6800	SUB	Paper Tape Lib,Prog 50;24-Bit Reentrant Floating Point Pkg	MOTA
83	SW-M68UG51	6800	M6800	SUB	Paper Tape Lib,Prog 51;RDR1.B	MOTA
84	SW-M68UG52	6800	M6800	SUB	Paper Tape Lib,Prog 52;Missionaries and Cannibals (MISCAN)	MOTA
85	SW-M68UG53	6800	M6800	SUB	Paper Tape Lib,Prog 53;DUMP	MOTA
86	SW-M68UG54	6800	M6800	SUB	Paper Tape Lib,Prog 54;Char Generation on X-Y Recorder	MOTA
87	SW-M68UG55	6800	M6800	SUB	Paper Tape Lib,Prog 55;Cyclic Redundancy CK Char Gen	MOTA
88	SW-M68UG56	6800	M6800	SUB	Paper Tape Lib,Prog 56;Decode	MOTA
89	SW-M68UG57	6800	M6800	SUB	Paper Tape Lib,Prog 57;PRTMSG	MOTA
90	SW-M68UG58	6800	M6800	SUB	Paper Tape Lib,Prog 58;Disk File Transfer	MOTA
91	SW-M68UG59	6800	M6800	SUB	Paper Tape Lib,Prog 59; Quick Load (QLOAD)	MOTA
92	SW-M68UG60	6800	M6800	SUB	Paper Tape Lib,Prog 60;M6800 Res I/O Pkg MINIbug II Version	MOTA
93	SW-M68UG61	6800	M6800	SUB	Paper Tape Lib,Prog 61;MPL Core Sort Prog	MOTA
94	SW-M68UG62	6800	M6800	SUB	Paper Tape Lib,Prog 62;24-Hour Clock	MOTA
95	SW-M68UG63	6800	M6800	SUB	Paper Tape Lib,Prog 63;TTYIO	MOTA
96	SW-M68UG64	6800	M6800	SUB	Paper Tape Lib,Prog 64;Teletype Graph Generator	MOTA
97	SW-M68UG65	6800	M6800	SUB	Paper Tape Lib,Prog 65;MICRO-BASIC	MOTA
98	SW-M68UG66	6800	M6800	SUB	Paper Tape Lib,Prog 66;Instrument Interfacer	MOTA
99	SW-M68UG67	6800	M6800	SUB	Paper Tape Lib,Prog 67;M6800 Cross Asmb for Wang 2200B	MOTA
100	SW-M68UG68	6800	M6800	SUB	Paper Tape Lib,Prog 68;Gray Code to Binary Conversion	MOTA
101	SW-M68UG69	6800	M6800	SUB	Paper Tape Lib,Prog 69; PROM Programmer	MOTA
102	SW-M68UG70	6800	M6800	SUB	Paper Tape Lib,Prog 70;EIA to ASCII	MOTA
103	SW-M68UG71	6800	M6800	SUB	Paper Tape Lib,Prog 71;Telephone Dialer	MOTA
104	SW-M68UG72	6800	M6800	SUB	Paper Tape Lib,Prog 72;ISQRT	MOTA
105	SW-M68UG73	6800	M6800	SUB	Paper Tape Lib,Prog 73;Music	MOTA
106	SW-M68UG74	6800	M6800	SUB	Paper Tape Lib,Prog 74; False Loader	MOTA
107	SW-M68UG75	6800	M6800	SUB	Paper Tape Lib,Prog 75; Function exp(x),ln(x)	MOTA
108	SW-M68UG76	6800	M6800	SUB	Paper Tape Lib,Prog 76;FloatinPaint Math Routines	MOTA
109	SW-M68UG77	6800	M6800	SUB	Paper Tape Lib,Prog 77;BINA	MOTA
110	SW-M68UG78	6800	M6800	SUB	Paper Tape Lib,Prog 78;LPNT-Mem Dump to Line Printer	MOTA

SYMBOLS AND CODES
EXPLAINED IN INTERPRETER

4.SYSTEM SOFTWARE INDEX

IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	1 MFR. CODE
1	SW-M68UG79	6800	M6800	SUB	Paper Tape Lib,Prog 79;MECOPY	MOTA
2	SW-M68UG80	6800	M6800	SUB	Paper Tape Lib,Prog 80;HPZ644A Interface I/O	MOTA
3	SW-M68UG81	6800	M6800	SUB	Paper Tape Lib,Prog 81; CRT/EDOS	MOTA
4	SW-M68UG82	6800	M6800	SUB	Paper Tape Lib,Prog 82;PROM	MOTA
5	SW-M68UG83	6800	M6800	SUB	Paper Tape Lib,Prog 83;MEMOVE	MOTA
6	SW-M68UG84	6800	M6800	SUB	Paper Tape Lib,Prog 84;PNGEN	MOTA
7	SW-M68UG85	6800	M6800	SUB	Paper Tape Lib,Prog 85;NIM Game	MOTA
8	SW-M68UG86	6800	M6800	SUB	Paper Tape Lib,Prog 86;Morse Code Send and Receive	MOTA
9	SW-M68UG87	6800	M6800	SUB	Paper Tape Lib,Prog 87;EXORCYB	MOTA
10	SW-M68UG88	6800	M6800	SUB	Paper Tape Lib,Prog 88;CODEC-ASCII/BAUDOT	MOTA
11	SW-M68UG89	6800	M6800	SUB	Paper Tape Lib,Prog 89;Math	MOTA
12	SW-M68UG90	6800	M6800	SUB	Paper Tape Lib,Prog 90;MONTR4	MOTA
13	SW-M68UG91	6800	M6800	SUB	Paper Tape Lib,Prog 91;KEYBRD	MOTA
14	SW-M68UG92	6800	M6800	SUB	Paper Tape Lib,Prog 92;TRIG	MOTA
15	SW-M68UG93	6800	M6800	SUB	Paper Tape Lib,Prog 93;QUMEPR	MOTA
16	SW-M68UG94	6800	M6800	SUB	Paper Tape Lib,Prog 94;PPX	MOTA
17	SW-M68UG95	6800	M6800	SUB	Paper Tape Lib,Prog 95;INTEG	MOTA
18	SW-M68UG96	6800	M6800	SUB	Paper Tape Lib,Prog 96;SBBCD	MOTA
19	SW-M68UG97	6800	M6800	SUB	Paper Tape Lib,Prog 97;CONV	MOTA
20	SW-M68UG98	6800	M6800	SUB	Paper Tape Lib,Prog 98;BCDRTN	MOTA
21	SW-M68UG99	6800	M6800	SUB	Paper Tape Lib,Prog 99;FILETX	MOTA
22	SW-M68UG100	6800	M6800	SUB	Paper Tape Lib,Prog 100;PDP8EM	MOTA
23	SW-M68UG101	6800	M6800	SUB	Paper Tape Lib,Prog 101;FPCMP	MOTA
24	SW-M68UG102	6800	M6800	SUB	Paper Tape Lib,Prog 102;DA8CH	MOTA
25	SW-M68UG103	6800	M6800	SUB	Paper Tape Lib,Prog 103;DIABPD	MOTA
26	SW-M68UG104	6800	M6800	SUB	Paper Tape Lib,Prog 104;HSPTD	MOTA
27	SW-M68UG105	6800	M6800	SUB	Paper Tape Lib,Prog 105;PREMEX	MOTA
28	SW-M68UG106	6800	M6800	SUB	Paper Tape Lib,Prog 106;CRDDRV	MOTA
29	SW-M68UG107	6800	M6800	SUB	Paper Tape Lib,Prog 107;RSORT	MOTA
30	SW-M68UG108	6800	M6800	SUB	Paper Tape Lib,Prog 108;SIMUL	MOTA
31	SW-M68UG109	6800	M6800	SUB	Paper Tape Lib,Prog 109;FLAGX	MOTA
32	SW-M68UG110	6800	M6800	SUB	Paper Tape Lib,Prog 110;LPDRV1	MOTA
33	SW-M68UG111	6800	M6800	SUB	Paper Tape Lib,Prog 111;ALPHBT	MOTA
34	SW-M68UG112	6800	M6800	SUB	Paper Tape Lib,Prog 112;AUTOBD	MOTA
35	SW-M68UG113	6800	M6800	SUB	Paper Tape Lib,Prog 113;ARRAYP	MOTA
36	SW-M68UG114	6800	M6800	SUB	Paper Tape Lib,Prog 114;MAARS	MOTA
37	SW-M68UG115	6800	M6800	SUB	Paper Tape Lib,Prog 115;ACIACK	MOTA
38	SW-M68UG116	6800	M6800	SUB	Paper Tape Lib,Prog 116;DISKEY	MOTA
39	SW-M68UG117	6800	M6800	SUB	Paper Tape Lib,Prog 117;KTIME	MOTA
40	SW-M68UG118	6800	M6800	SUB	Paper Tape Lib,Prog 118;RTCLK	MOTA
41	SW-M68UG119	6800	M6800	SUB	Paper Tape Lib,Prog 119;PTCG	MOTA
42	SW-M68UG120	6800	M6800	SUB	Paper Tape Lib,Prog 120;BIGBAN	MOTA
43	SW-M68UG121	6800	M6800	SUB	Paper Tape Lib,Prog 121;PRMBUG	MOTA
44	SW-M68UG122	6800	M6800	SUB	Paper Tape Lib,Prog 122;MSTRMD	MOTA
45	SW-M68UG123	6800	M6800	SUB	Paper Tape Lib,Prog 123;DZMON	MOTA
46	SW-M68UG124	6800	M6800	SUB	Paper Tape Lib,Prog 124; PARITY	MOTA
47	SW-M68UG125	6800	M6800	SUB	Paper Tape Lib,Prog 125; HEXCAL	MOTA
48	SW-M68UG	6800	M6800	SSS	General Interest Programs for M6800 System	MOTA
49	SW-M68XAE6812A	6800	M6800	ASB	Resident Assembler/Editor on Cassette	MOTA
50	SW-M68XAE6812B	6800	M6800	ASB	Resident Assembler/Editor on Paper Tape(PT)	MOTA
51	SW-M68XAE6812D	6800	M6800	ASB	Resident Assenbler/Editor on Diskette	MOTA
52	SW-M68XAE6813	6800	M6800	ASB	Resident Editor/Assembler on Cassette(A),Paper Tape(B),MDOS Diskett(M)	MOTA
53	SW-M68XEARC1	6800	M6800	MFS	Editor/Assembler in EPROMs (7) for Use w/MICRObug	MOTA
54	SW-M6800#1▼	6800	M6800	DEB	EXORciser Exbug Firmware	MOTA
55	SW-M6800#2	6800	M6800	CMP	MPL Compiler;ANSI-Standard FORTRAN,Timesharing,In House Computer	MOTA
56	SW-M6800EDITORM	6800	M6800	EDT	Resident CRT Editor on MDOS Diskette:CRT/SCROLL Mode of Operation	MOTA
57	SW-M6805MASC01M	6800	M6800	MFS	Cross Macro Assembler and Linking Loader on MDOS Diskette,6805 Support	MOTA
58▼	SW-M6809BASICM	6800	M6800	CMP	Resident BASIC-M Interative Compiler on MDOS Diskette	MOTA
59	SW-M6809EDITOR	6800	M6800	EDT	Resident CRT Editor on MDOS Diskette;CRT/SCROLL Mode of Operation	MOTA
60	SW-M6809MASC01M	6800	M6800	MFS	Cross Macro Assembler and Linking Loader on MDOS Diskette,6809 Support	MOTA
61	SW-M6809MPL	6800	M6800	CMP	Resident Compiler on MDOS Diskette	MOTA
62	SW-M6809PASCLI	6800	M6800	EDT	Resident PASCAL Interpreter on MDOS Disk,M6809 Based,Edit/Link Loader	MOTA
63▼	SW-M6809XASMBL2	6800	M6800	ASB	Cross Macro Assmb:Mag Tape;IBM 370 Based;Cond Assembly,Expression Eval	MOTA
64▼	SW-M6809XASMBL3	6800	M6800	ASB	Cross Macro Assmb:Mag Tape;PDP-11 Based;Cond Assembly,Expression Eval	MOTA
65	SW-MEC68MIN2▼	6800	M6800	DEB	MINIBUG II Firmware:For Program Development,Part of M68ADS1A/2A Devel	MOTA
66▼	SW-MEK6809EAC	6800	M6800	EDT	Editor Assembler:300 Baud Audio Cassette;ROMable;Self-Sizing of Memory	MOTA
67	SW-MEX68CT2▼	6800	M6800	DIA	Personality Cd MC6800 Test Prog Used W/MEX68CT Test,On Cassette/Disk/T	MOTA
68	SW-MEX68CT3▼	6800	M6800	DIA	Personality Cd MC6820 Test Prog Used W/MEX68CT Test,On Cassette/Disk/T	MOTA
69	SW-MEX68CT4▼	6800	M6800	DIA	Personality Cd MC6820 Test Prog Used W/MEX68CT Test,On Cassette/Disk/T	MOTA
70	SW-MEX68CT5▼	6800	M6800	DIA	Personality Cd MC6830 Test Prog Used W/MEX68CT Test,OnCassette,Disk/Ta	MOTA
71	SW-MEX68CT6▼	6800	M6800	DIA	Universal ROM Personality Card Test Progam Used W/MEX68CT Tester	MOTA
72	SW-MEX68CT7▼	6800	M6800	DIA	Personal Cd MCM6810 Test Prg Used W/MEX68CT Test,OnCassette/Disk/Tape	MOTA
73	SW-MEX141000M	6800	M6800	SIM	Software Simulator Package of the MC141000/1200 Development System	MOTA
74	SW-MPBVM	6800	M6800	OPS	Time Sharing System Software;Build-Virtual Machine	MOTA
75	SW-MPCASM	6800	M6800	ASB	Cross Assembler,FORTRAN IV,Timesharing Networks	MOTA
76	SW-MPSSIM	6800	M6800	SIM	Simulator,Stand-Alone Pkg,On Own or In-House Computer	MOTA
77	SW-M68KEMLC	68000	M68000	SIM	Software Simulator Package of the M68000 on Magnetic Tape	MOTA
78	SW-MSC8301▼	Z80	MSC8001-Z80	MON	Uniform Monitor:Prog Dev Sys And Debug Monitor,ROM Resident,Machine In	MSCC
79	SW-MSC8303▼	Z80	MSC8001-Z80	OPS	Monolithic Systems Operating Sys (MSOS):File Management/Progm. Devel S	MSCC
80	SW-MCS6500#1	6500	MCS6500	ASB	Cross Assembler;For Microprocessor Program at Symbolic Assembly Level	MTY
81	SW-MCS6500#2	6500	MCS6500	SIM	Emulator;Calculates the Time of Sections of Code	MTY
82	SW-MCS6500ASM650	6500	MCS6500	ASB	Cross Assembler	MTY
83	SW-MCS6500ASM	6500	MCS6500	SSS	Interactive Program for Source Code;UCS Time Sharing	MTY
84	SW-MCS6500DMP	6500	MCS6500	SSS	ROM Dump Program;UCS Time Sharing	MTY
85	SW-MCS6500KIM	6500	MCS6500	SUB	KIMath;ROM-Resident Floating-Point Mathematical Subroutine Pkg	MTY
86	SW-MCS6500KIMRA	6500	MCS6500	ASB	KIM Resident Assemb/Editor;For Programs for MCS6500 Based Systems	MTY
87	SW-MCS6500SIM650	6500	MCS6500	SIM	Simulator;UCS Time Sharing	MTY
88	SW-MCS6500SIM	6500	MCS6500	SIM	Interactive Program for Simulator Command File;UCS Time Sharing	MTY
89	SW-MS801#1	8080	MS801	DEB	Standard Debug Package	MUL
90	SW-MS808A#1▼	8080	MS801	ASB	Relocatable Symbolic Assembler with Entry Linking	MUL
91	SW-MS808A#2▼	8080	MS808A	EDT	Text Editor	MUL
92	SW-MS808A#3▼	8080	MS808A	LOA	Relocatable Linking Loader	MUL
93	SW-MS808A#4▼	8080	MS808A	SSS	Utility Package and Debug (Hardware and Software)	MUL
94	SW-MS808A#5▼	8080	MS808A	DIA	Diagnostics	MUL
95	SW-MS808A#6▼	8080	MS808A	LAN	Focal (A Registered Trademark of Digital Equip Corp) Interpreter	MUL
96	SW-MS808A#7▼	8080	MS808A	EDT	Basic Interpreter (5k)	MUL
97	SW-MS808A#8▼	8080	MS808A	EDT	Basic Interpreter (8k)	MUL
98	SW-MS808A#9▼	8080	MS808A	EDT	Basic Interpreter (12k Extended)	MUL
99	SW-MS808A#10▼	8080	MS808A	CMP	FORTRAN IV Compiler	MUL
100	SW-MS808A#11▼	8080	MS808A	OPS	Floppy Disk Operating System (FDOS)	MUL
101	SW-BSAL80ASSBLR	8080	muPRO80	ASB	Block Structured Assembly Language Assembler;Uses High Level Syntax	MUP
102	SW-BSAL80EDIT	8080	muPRO80	EDT	Text Editor;11 HighLevel Comm Incl ADD,DELETE,FIND,REPLACE,KEEP etc	MUP
103	SW-BSAL80LNKLD	8080	muPRO80	LOA	Relocating/Linking Loader;Auto Program and Data Memory Allocations	MUP
104	SW-BSAL80/85	8080,85	muPRO80	MFS	Software for 8080,8085;Includes Assembly Language and Text Editor	MUP
105	SW-muPRO80DS	8080,85	muPRO80	OPS	Software of Devel Syst;On Disc Editor,Lang,Loader,Utilities,Emulator	MUP
106#	SW-NASBUGI▼	Z80	NASCOMI	MON	Monitor Firmware for NASCOMI Microcomputer	NASB
107	SW-PASCAL	8085	NMS85/P	CMP	PASCAL(UCSD)Compiler/Interpreter	NMS
108	SW-EXT-BASIC	MULTI$	HORIZON-1	LAN	Extended BASIC;Operates on Both Z80 and 8080 Systems	NOR
109	SW-MDS-PERS-DQ	Z80	HORIZON	DOS	Std DOS I/O for S-100 System;For Dbl Density or Quad Capacity	NOR
110	SW-SOFT-SPEC-DQ	Z80	HORIZON	SSS	Special non-Std 8,10,12,14 Digits for BASIC;Dbl Density or Quad Capa	NOR

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

4.SYSTEM SOFTWARE INDEX

IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATE-GORY	S O F T W A R E L I B R A R Y NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	1 MFR. CODE
1	SW-MONITOR	Z80	HORIZON-1	MON	MONITOR Program;For Maintenance and Debugging Functions	NOR
2	SW-PAS-AUX-DQ	Z80$	HORIZON	ASB	Aux Pkg to PAS-PRI w/8080,Z80 Assemble;For Dbl Density or Quad Capa.	NOR
3	SW-IMP16F000	IMP16	IMP16	SSS	ROM Utility Prog;TTY,ControlPanel/Binary PaperTape Punch;ANSI FORTRAN	NSC
4	SW-IMP16F002	IMP16	IMP16	DEB	Program Debug Aid	NSC
5	SW-IMP16F500	IMP16	IMP16	SSS	ROM Utility Prog;Memory Diagnostic ControlPanel/Demonstration Program	NSC
6	SW-IMP16F501	IMP16	IMP16	DIA	Diagnostic Program	NSC
7	SW-IMP16P	IMP16	IMP16	LOA	Loader	NSC
8	SW-IMP16S900	IMP16	IMP16	ASB	IMP Resident System to FORTRAN Cross Assembler Package	NSC
9	SW-IMP16S900A	IMP16	IMP16	ASB	Assembler;ANSI FORTRAN	NSC
10	SW-IMP16S901C	IMP16	IMP16	OPS	Complete Resident System Package on Paper Tape with Listings	NSC
11	SW-IMP16S901Q	IMP16	IMP16	OPS	Complete Resident System Package on Cards with Listings	NSC
12	SW-IMP16S902M	IMP16	IMP16	OPS	Complete Resident System Package on Diskette with Listings	NSC
13	SW-IPC-16S/103M	IPC16	IPC16	SSS	Enhanced DOS Software Package	NSC
14	SW-INS8295▼	MULTI$	SC/MP	LAN	National Industrial BASIC Language(NIBL) on 4k x 8 ROM	NSC
15	SW-IPC16S100C	PACE	IPC16	ASB	4k Paper Tape Cross Assembler	NSC
16	SW-IPC16S100Q	PACE	IPC16	ASB	4k Card Cross Assembler	NSC
17	SW-IPC16S101C	PACE	IPC16	ASB	PACE-IMP 16 8k Cross Assembler on Paper Tape	NSC
18	SW-IPC16S101Q	PACE	IPC16	ASB	PACE-IMP 16 8k Cross Assembler on Cards	NSC
19	SW-IPC16S102P	PACE	IPC16	ASB	PACE-FORTRAN Cross Assembler (Executer on IBM 360/370)	NSC
20	SW-IPC16S102Q	PACE	IPC16	ASB	Card Cross Assembler;PACE FORTRAN	NSC
21	SW-IPC16S901C	PACE	IPC16	OPS	Pace Resident Sys Pkg;SourceCode Editor,Assmbs,Loaders,DiagnosticsTape	NSC
22	SW-IPC16S901Q	PACE	IPC16	OPS	Pace Resident Sys Pkg;SourceCode Editor,Assmbl,Load,Diagnostics Cards	NSC
23	SW-ISP8S100C	SC/MP	SC/MP	ASB	SC/MP-IMP 16 4k Cross Assembler on Object Tapes	NSC
24	SW-ISP8S100Q	SC/MP	SC/MP	ASB	SC/MP-IMP 16 4k Cross Assembler on Object Cards	NSC
25	SW-ISP8S101C	SC/MP	SC/MP	ASB	SC/MP-IMP 16 8k Cross Assembler on Object Tapes	NSC
26	SW-ISP8S101Q	SC/MP	SC/MP	ASB	SC/MP-IMP 16 8k Cross Assembler on Object Cards	NSC
27	SW-ISP8S102P	SC/MP	SC/MP	LAN	FORTRAN Based Source Card Package Written in ANS FORTRAN	NSC
28	SW-ISP8S103C	SC/MP	SC/MP	SSS	8k PACE-P Based Pkg on Object Tapes	NSC
29	SW-ISP8S103Q	SC/MP	SC/MP	ASB	8k PACE-P Based Cross Assembler on Object Cards	NSC
30	SW-SC/MP#1	SC/MP	SC/MP	DEB	Debug Program;FORTRAN IV;Timeshare Services	NSC
31	SW-SC/MP#2	SC/MP	SC/MP	ASB	Resident Conversational Assembler/Editor	NSC
32	SW-SC/MP#3	SC/MP	SC/MP	DIA	System Diagnostics	NSC
33	SW-SC/MP#4	SC/MP	SC/MP	ASB	Cross Assembler	NSC
34	SW-SC/MP#5	SC/MP	SC/MP	LOA	Loader	NSC
35	SW-BLC910▼	8080	Series 80	MON	Prototyping System Monitor	NSC
36	SW-OS65D	MULTI$	C2#2,C3	OPS	Disk Operating System:Devel Oriented,For all Disk Based Computers	OHS
37	SW-OS65U	MULTI$	C2#2,C3	OPS	Operating Sys Integrated into 9 Digit Ext BASIC Standard W/CD74	OHS
38▼	SW-WP1B	6800	G3	EDT	Extended Editor(w/word Processing Features)w/InterActive Assem	OHS
39#	SW-LKIT16#1▼	1610	LKIT16	MON	LKIT 16 Monitor;Simple Assembler,Console Program	PAFJ
40#	SW-LKIT16#2▼	1610	LKIT16	LAN	Minimum BASIC	PAFJ
41#	SW-LKIT16#3▼	1610	LKIT16	LAN	Tiny BASIC	PAFJ
42#	SW-LKIT16#4▼	1610	LKIT16	ASB	Inverse Assembler	PAFJ
43#	SW-LKIT16#5	1610	LKIT16	LOA	Input/Output Routine	PAFJ
44#	SW-LKIT16#6	1610	LKIT16	SUB	Arithmetic and Primary Function Routine	PAFJ
45#	SW-LKIT16#7	1610	LKIT16	SUB	GAME;Black Jack,Air Flight,Mahjong Games	PAFJ
46#	SW-PFL16A#1	1610	PFL16A	SSS	UMOS/D Support System;PANAFACOMU Series Minicomputer OS	PAFJ
47#	SW-PFL16A#2	1610	PFL16A	SSS	UMOS/C Support System;PANAFACOMU Series Minicomputer OS	PAFJ
48#	SW-PFL16A#3	1610	PFL16A	SSS	MACC Support System;MACC-7/L Minicomputer	PAFJ
49#	SW-PFL16A#4	1610	PFL16A	SSS	Basic Support Program	PAFJ
50#	SW-PFL16A#5	1610	PFL16A	LOA	Linkage Loader	PAFJ
51#	SW-PFL16A#6	1610	PFL16A	SSS	Utility Programs	PAFJ
52#	SW-PFL16A#7	1610	PFL16A	OPS	PFL Self Standing System	PAFJ
53#	SW-PFL16A#8	1610	PFL16A	ASB	CAP;Cross Assembler	PAFJ
54#	SW-PFL16A#9	1610	PFL16A	LOA	LINK;Linkage Loader	PAFJ
55#	SW-PFL16A#10	1610	PFL16A	SIM	MICS;Simulator	PAFJ
56#	SW-PFL16A#11	1610	PFL16A	DEB	CDEBG;Connection Debugger	PAFJ
57#	SW-PFL16A#12	1610	PFL16A	SSS	FACOM M Series Support System;Macro Cross Assembler;Simulator etc	PAFJ
58#	SW-PFL16A#13	1610	PFL16A	SSS	FACOM 8 Series Support System	PAFJ
59#	SW-PFL16A#14	1610	PFL16A	SSS	IBM 370 Series Support System;Macro Cross Assembler;Simulator Etc	PAFJ
60#	SW-PFL16A#15	1610	PFL16A	CMP	PL/16;PL/1 Like High Level Language Compiler	PAFJ
61#	SW-PFL16A#16	1610	PFL16A	LAN	6k BASIC	PAFJ
62#	SW-PFL16A#17	1610	PFL16A	MFS	FPS 16;Floppy Programming System;BASIC,Assembler,File Utilities	PAFJ
63#	SW-PFL16A#18	1610	PFL16A	MON	Real Time Monitor;Monitor Macro Routine;I/O,Arithmetical Routine	PAFJ
64#	SW-PFL16A#19	1610	PFL16A	DEB	Debugging Program;Tracer,Inverse Assembler;Simple Assembler	PAFJ
65#	SW-PFL16A#20	1610	PFL16A	ASB	Macro Cross Assembler for UMOS/D Support System	PAFJ
66#	SW-PFL16A#21▼	1610	PFL16A	SSS	BUROM;IPL Program and BASIC Utilities ROM	PAFJ
67	SW-BASIC-EQ	8080	EQUINOX-100	LAN	Software Pkg,Language for Number-Oriented Programming	PAR
68	SW-EQU-ATE	8080	EQUINOX-100	MFS	Software Pkg for Text Oriented Programming,Editing and Assembly	PAR
69	SW-BDOS	Z80	CP/M	DOS	Basic DOS,64 Files Per Disk(Max 4 Disk Drives);0 TO 240k Bytes	PCC
70	SW-iCOM-DEBBIE	Z80$	Z80	DOS	Disk Extended BASIC; Compatible w/Z80,8080 PCC	PCC
71	SW-ALTAIRPKGII	8080	ALTAIR8800	MFS	Assembly Lang Dev Sys for 8080;Incl Monitor,Edit,Assem,Debug 8k Mem	PCC
72	SW-PCM12890	6100	PCM-12A	EDT	4k Basic Interpreter	PCM
73	SW-BOS80A	8080	MICROPAC80A	OPS	Basic Operating System	PCS
74	SW-DBG80	8080	MICROPAC80A	DEB	Debug Program;Allows Full Oper Control over Test Program Execution	PCS
75	SW-EDIT80A	8080	MICROPAC80A	EDT	Editor	PCS
76	SW-MAS80A	8080	MICROPAC80A	ASB	Macro Assembler	PCS
77	SW-MAS80R	8080	MICROPAC80A	ASB	Relocatable Macro Assembler	PCS
78	SW-REL80	8080	MICROPAC80A	LOA	Relocating and Linking Loader	PCS
79	SW-SPDS-ASMB	8080	SUPERPAC180	ASB	SUPERPAC Devl Absolute Macro Assembler	PCS
80	SW-SPDS-EDTL	8080	SUPERPAC180	EDT	SUPERPAC Devl Editor Program	PCS
81	SW-SPDS-FOS	8080	SUPERPAC180	OPS	SUPERPAC Devl Floppy Disk Operating System	PCS
82	SW-SPDS-FTC	8080	SUPERPAC180	CMP	SUPERPAC Devl FORTRAN Compiler	PCS
83	SW-SPDS-RLOD	8080	SUPERPAC180	LOA	SUPERPAC Devl Relocating Linking Loader	PCS
84	SW-SPDS-RSMB	8080	SUPERPAC180	ASB	SUPERPAC Devl Relocatable Macro Assembler	PCS
85	SW-SPDS-SPDOS	8080	SUPERPAC180	OPS	SUPERPAC Development Operating System	PCS
86	SW-SPDS-UDL	8080	SUPERPAC180	LOA	SUPERPAC Devl Up/Down Loader	PCS
87	SW-SPDS-XREF	8080	SUPERPAC180	SSS	SUPERPAC Devl Cross Reference Generator	PCS
88	SW-SPUR0	8080	SUPERPAC180	SSS	Super Pac Utility Routine 0;1k Byte Program In a 2708 EROM	PCS
89	SW-SPUR1	8080	SUPERPAC180	SSS	Super Pac Utility Routine 1;1k Byte Program In a 2708 EROM W/Subrout	PCS
90	SW-SPUR2	8080	SUPERPAC180	SSS	Super Pac Utility Routine 2;3k Byte Program in 3 2708 EROMS	PCS
91	SW-681/1/00271/000	MIPROC	MIPROC16	ASB	XASM FORTRAN MIPROC Cross Assembler and Simulator	PLM
92	SW-681/1/00281/000	MIPROC	MIPROC16	ASB	MIP11;PDP11 MACRO MIPROC Cross Assembler	PLM
93	SW-681/1/00446/000▼	MIPROC	MIPROC16	MON	Monitor;Interactive Debug Monitor	PLM
94	SW-NOVAXASM	MIPROC	MIPROC16	ASB	XASM;NOVA ASM MIPROC Cross Assembler	PLM
95	SW-PL-MIPROC	MIPROC	MIPROC16	CMP	PL MIPROC;High Level Language Cross Compiler for MIPROC	PLM
96	SW-MIPROCCORAL	MIPROC16	MIPROC16	CMP	Coral-66 Cross Compiler for MIPROC Runs on PDP11	PLM
97	SW-MPC281	MIPROC16	MIPROC16	ASB	MIP 11 PDP11 MARCO Cross Assembler	PLM
98	SW-MPC446	MIPROC16	MIPROC16	MON	Monitor Interactive Debug Monitor	PLM
99	SW-MPC729	MIPROC16	MIPROC16	SSS	Floating Point Software Pkg	PLM
100	SW-MIPROC16#1	1600	MIPROC16	ASB	Assembler;FORTRAN IV;TYMSHARE and GE Mark III	PLM
101	SW-MIPROC16#2	1600	MIPROC16	SIM	Simulator;FORTRAN IV;TYMSHARE and GE Mark III	PLM
102	SW-8080CHESS	8080	SOL20	SUB	Video Game on Cassette,Min Memory Required-16k	PRT
103	SW-ALS8	8080	SOL20	MFS	Resident Assembler,Simulator and Text Editor on Cassette,Min Mem Rq12k	PRT
104	SW-ALS8R▼	8080	SOL20	MFS	ROM Resident Assembly Language Op Syst with Simulator	PRT
105	SW-ASSM	8080	SOL20	ASB	Advanced 8080 Assembler on Cassette,Min Memory Required-10k	PRT
106	SW-BASIC5	8080	SOL20	LAN	BASIC5 on Cassette,Min Memory Required 10k	PRT
107	SW-DEBUG-PRT	8080	SOL20	ASB	8080 Debugger on Cassette,Min Memory Required-8k	PRT
108	SW-ECBASIC	8080	SOL20	LAN	Extended BASIC on Cassette,Min Memory Required 16k	PRT
109	SW-EDBASIC	8080	SOL20	LAN	Extended Disk BASIC Language,Min Memory Required 32k	PRT
110	SW-EDFORTRAN	8080	SOL20	LAN	Extended Disk FORTRAN;Min Memory Required 32k	PRT

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	[4] SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	[2] GENERIC I.D. $-MULTI-SYSTEM APPLICATION	[3] SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	[1] MFR. CODE
1	SW-EDIT	8080	SOL20	EDT	8080 Editor on Cassette,Min Memory Required 8k	PRT
2	SW-FOCAL	8080	SOL20	LAN	New 8080 FOCAL on Cassette,Min Memory Required 10k	PRT
3	SW-GAMEPAC1	8080	SOL20	SUB	GAMEPAC1 Video Game on Cassette,Min Memory Required 4k	PRT
4	SW-GAMPAC2	8080	SOL20	SUB	Video Game on Cassette,Min Memory Required-4k	PRT
5	SW-PILOT	8080	SOL20	LAN	PILOT on Cassette;Min Memory Required 16k	PRT
6	SW-PTDOS1-4	8080	SOL20	OPS	PT Disc Operating System(Replacement);Min Memory Required 32k	PRT
7	SW-PTDOS	8080	SOL20	OPS	Disc Operating System for Developing Programs	PRT
8	SW-SOFTWARE1	8080	SOL20	ASB	Resident Assembler Package on Cassette,Min Memory Required 6k	PRT
9	SW-SOLOS▼	8080	SOL20	MON	SOLOS:Monitor Program in 2048 Bytes ROM,Replaces Front Panel Controls	PRT
10	SW-TREK80	8080	SOL20	SUB	TREK80 Video Game on Cassette,Min Memory Required 8k	PRT
11	SW-Q2KBAI▼	Z80	QUAY8000	LAN	Tiny Basic In UVPROM to Run on QUAY 80AI System	QUY
12	SW-Q4KBAI	Z80	QUAY8000	LAN	Complete 4k Basic on Cassette Tape to Run on QUAY 80AI	QUY
13	SW-26-1146	Z80	TRS-80	LOA	Communications Program on Cassette (Level II)	RAD
14	SW-26-1501	Z80	TRS-80	BAS	Payroll Program (Up to 12 Employees)	RAD
15	SW-26-1502	Z80	TRS-80	BAS	In Memory Information Program;3 Assembly Lang Programs	RAD
16	SW-26-1503	Z80	TRS-80	BAS	Mailing List(Level-II,16k RAM Only);Program On Cassette	RAD
17	SW-26-1504	Z80	TRS-80	BAS	Payroll,Level II; Cassette	RAD
18	SW-26-1505	Z80	TRS-80	BAS	Word Processor (Scriptsit) Cassette	RAD
19	SW-26-1551	Z80	TRS-80	BAS	Mailing List;Program on Diskette(for 32K,2 Disk Business Systems)	RAD
20	SW-26-1552	Z80	TRS-80	BAS	General Ledger-I;Program on Diskette(for 32K,2Disk Business Systems)	RAD
21	SW-26-1553	Z80	TRS-80	BAS	Inventory Control Program on Diskette, 32k	RAD
22	SW-26-1556	Z80	TRS-80	BAS	Payroll Program on Diskette, 32k	RAD
23	SW-26-1563	Z80	TRS-80	BAS	Word Processor (Scriptsit) Disk	RAD
24	SW-26-1571	Z80	TRS-80	BAS	Real Estate Program, Vol I; Level II, 16k	RAD
25	SW-26-1572	Z80	TRS-80	BAS	Real Estate Program, Vol II; Level II, 16k	RAD
26	SW-26-1602	Z80	TRS-80	BAS	Personal Finance Program	RAD
27	SW-26-1603	Z80	TRS-80	BAS	Budget MANAGEMENT(Level-II 16K RAM Only);Program On Cassette	RAD
28	SW-26-1701	Z80	TRS-80	SUB	Math I Program	RAD
29	SW-26-1702	Z80	TRS-80	SUB	Algebra I Program	RAD
30	SW-26-1703	Z80	TRS-80	SUB	Statistical Analysis Program	RAD
31	SW-26-1704	Z80	TRS-80	SUB	Double Precision Subroutines(Level-II Only);Program On Cassette	RAD
32	SW-26-1705	Z80	TRS-80	SUB	Advanced Statistical Analysis(Level-II 16K Only);Program On Cassette	RAD
33	SW-26-1706	Z80	TRS-80	SUB	I.Q. Builder Program; Level I and II, 4k	RAD
34	SW-26-1707	Z80	TRS-80	BAS	BCL Standard and Poors Portfolio Mgmt and Security Selection System	RAD
35	SW-26-1708	Z80	TRS-80	SUB	TRS-80 Hands on BCL Program, Level II, 4k	RAD
36	SW-26-1709	Z80	TRS-80	AS	BCL Program World	RAD
37	SW-26-1710	Z80	TRS-80	AS	BCL Student Guide	RAD
38	SW-26-1711	Z80	TRS-80	AS	BCL Teachers Guide	RAD
39	SW-26-1713	Z80	TRS-80	AS	Teacher Aide	RAD
40	SW-26-1801	Z80	TRS-80	SUB	Backgammon/Blackjack Game Program, Level I, 4k	RAD
41	SW-26-1802	Z80	TRS-80	SUB	Quick,Watson Game Program	RAD
42	SW-26-1803	Z80	TRS-80	SUB	Backgammon/Blackjack Game Program, Level II, 4k	RAD
43	SW-26-1805	Z80	TRS-80	SUB	Game Pack-I(Level-I Only);Program On Cassette	RAD
44	SW-26-1806	Z80	TRS-80	AS	Casino Games Pkg	RAD
45	SW-26-1901	Z80	TRS-80	SUB	Microchess(Level-I or II);Program On Cassette	RAD
46	SW-26-1902	Z80	TRS-80	SUB	Micromusic(Level-I or II);Program On Cassette	RAD
47	SW-26-1903	Z80	TRS-80	SUB	Micro Movie Program, Level I and II, 16k	RAD
48	SW-26-1904	Z80	TRS-80	SUB	Micro Marquee Program, Level I and II, 4k	RAD
49	SW-26-1905	Z80	TRS-80	SUB	Flying Saucer Program, Level I and II, 4k	RAD
50	SW-26-1906	Z80	TRS-80	SUB	Invasion Force Program, Level I and II, 16k	RAD
51	SW-26-1907	Z80	TRS-80	SUB	Checkers 80 Program, Level I and II, 16k	RAD
52	SW-26-1908	Z80	TRS-80	AS	ELIZA	RAD
53	SW-26-1909	Z80	TRS-80	ASB	PYRAMID	RAD
54	SW-26-2001	Z80	TRS-80	DEB	T Bug Program;Monitor Program Gives Access to Z80 CPU	RAD
55	SW-26-2002	Z80	TRS-80	ASB	Editor/Assembler Program	RAD
56	SW-26-2003	Z80	TRS-80	LAN	Level I BASIC Course;Contains 8 Lessons W/26 Programs	RAD
57	SW-26-2004	Z80	TRS-80	SUB	Level-II Renumber(Level-II Only);Program On Cassette	RAD
58	SW-26-2005	Z80	TRS-80	LAN	Level-II Basic Course Part I(Level-II Only);Program On Cassette	RAD
59	SW-26-2006	Z80	TRS-80	LAN	Level-II Basic Course Part II(Level-II,16K Only);Program On Cassette	RAD
60	SW-26-2201	Z80	TRS-80	LAN	TRS-80 FORTRAN	RAD
61	SW-26-2202	Z80	TRS-80	ASB	Disk Editor/Assembler	RAD
62	SW-26-4501	Z80	TRS-80	BAS	General Ledger/MOD II	RAD
63	SW-26-4506	Z80	TRS-80	BAS	Disk Mailing List/MOD II	RAD
64	SW-26-4552	Z80	TRS-80	BAS	ICS Series 1/MOD II	RAD
65	SW-26-4554	Z80	TRS-80	BAS	Accts/Rec Series 1/MOD II	RAD
66	SW-26-1573	Z80	TRS-800	BAS	Real Estate Program, Vol III; Level II, 16k	RAD
67	SW-CDP18S91X	1800	CDP1800	MFS	Software Dev Pkg Avail on Timeshare Sys or Mag Tape and Card Deck	RCA
68	SW-CDP18S820	1800	CDP1800	MFS	MicroFORTH Software for COSMAC Dev Syst II	RCA
69	SW-CDP18S826	1800	CDP1800	SUB	Binary Fixed-Point Arithmetic Subroutines;Disk	RCA
70	SW-CDP18S826V1	1800	CDP1800	SUB	Binary Fixed-Point Arithmetic Subroutines;Paper-Tape	RCA
71	SW-CDP18S826V2	1800	CDP1800	SUB	Binary Fixed-Point Arithmetic Subroutine;Cassette	RCA
72	SW-CDP18S827	1800	CDP1800	SUB	Binary Floating-Point Arithmetic Subroutines;Disk	RCA
73	SW-CDP18S831	1800	CDP1800	OPS	COSMAC Micromonitor Operating System (MOPS)	RCA
74	SW-CDP18S834	1800	CDP1800	CMP	Compiler/Interpreter;for COSMAC CDOS (CDS 111) CDP18S007V1/V3;Diskette	RCA
75	SW-CDPR512▼	1800	CDP1800	SSS	Utility Progr ROM Used with Eval Kit CDP18S020;ASCII Conv,Mem R/W	RCA
76	SW-CDPR522▼	1800	CDP1800	SSS	Microterminal(CDP18S021) Contr Progr ROM;Keybd Scan,Display Controls	RCA
77	SW-CDPR582▼	1800	CDP1800	SUB	Fixed Point Bin Arith ROM;31 Routines;16-Bit 2s Compl Add,Subtr,Mult	RCA
78	SW-VP700▼	1800	COSMACVIP	LAN	Tiny BASIC on ROM Bd;14 Standard,12 Special Commands;Req ASCII Keybd	RCA
79	SW-A7800▼	PPS4/1	PPS4/1	SSS	Supervisery Utility/Debug/Monitor;Provided in ROM of Spec Progm PPS4/1	RKW
80	SW-A7806▼	PPS4/1	PPS4/1	ASB	Assembler/Line Editor for MM76;Provided in ROM of Spec Progm PPS4/1	RKW
81	SW-A7807▼	PPS4/1	PPS4/1	ASB	Assembler/Line Editor for MM77,78;Provided in ROM of Spec Progm PPS4/1	RKW
82	SW-PPS4/1	PPS4/1	PPS4/1	ASB	Cross Assembler;FORTRAN IV;Provides Symbol Cross Ref and Diagnostics	RKW
83	SW-PPS#3	PPS4,8	PPS4,8	SSS	OutputFormatter;FORTRAN IV;TimeshareSys-GE MarkIII,TYMCOM-S,IBM 370TSO	RKW
84	SW-A65-010▼	6500	AIM65	ASB	AIM65 Two-Pass Symbolic Assembler	RKW
85	SW-A65-020▼	6500	AIM65	EDT	BASIC Interpreter For AIM65	RKW
86	SW-A65-100▼	6500	AIM65	MON	AIM65 Resident Monitor/Debug/Text Editor	RKW
87	SW-AIMMON▼	6500	AIM65	MON	ROM Resident Advanced Interactive Monitor Program	RKW
88▼	SW-M65-650	6500	R6500	ASB	Macro Assembler and Linking Loader;Minifloppy Diskette-Based SW	RKW
89	SW-PL/65	6500	SYSTEM65	LAN	Hi-Level Lang,Resembles PL/1,ALGOL;Outputs Assembler;Structured Progr	RKW
90	SW-SYS65DEBUG	6500	SYSTEM65	DEB	Debug/Monitor;SingleStep or RealTimeMode;Set/Clear BreakPointCommands	RKW
91	SW-SYS65EDIT	6500	SYSTEM65	EDT	Text Editor with Line,String and Character Oriented Commands	RKW
92	SW-FDOS/FMS	Z80	REXZ-110	OPS	Floppy Disk Operating System/File Management	RLC
93#	SW-BAS-Z	Z80	CLZ80	LAN	BASIC 8k Control Interpreter for CLZ80	SGAI
94#	SW-BAS-Z/1	Z80	CLZ80	LAN	BASIC 8k Control Interpreter for BASIC,MO-Z,ASS-Z,EDI-Z	SGAI
95	SW-SIA-ASSEMBLER	8080	Z80	ASB	Incremental Assembler w/MACRO Expander;Commands ASM or ASML	SIA
96	SW-SIA-BASIC	8080	Z80	LAN	Interface w/Disk System;Screen and Keyboard;Uses ZIL Z80 u-Processor	SIA
97	SW-SIA-EDITOR	8080	Z80	EDT	Interacts w/SIA Intelligent Disk System;Screen;Commands	SIA
98	SW-SIA-TERMINALOS	8080	Z80	MON	Screen and Keyboard Controls System	SIA
99	SW-2650#1	2650	2650	LAN	Assembler Language;FORTRAN IV;Timesharing or Batch from SIC	SIC
100	SW-2650#2	2650	2650	SIM	Simulator;FORTRAN	SIC
101	SW-2650AR1000	2650	2650	ASB	Relocatable Assembler Version 5.0	SIC
102	SW-2650AS1000/1100	2650	2650	ASB	2650 Assembler Version 3.2;PIPHASM Symbolic Language	SIC
103	SW-2650PL1000	2650	2650	CMP	Devl Software;High Level Language Compiler Plus 32 Bit Computer	SIC
104	SW-2650PL1100	2650	2650	CMP	Devl Software;High Level Language Compiler Plus 14 Bit Computer	SIC
105	SW-2650SM1000/1100	2650	2650	SIM	2650 Simulator Version 1.2;PIPSIM FORTRAN IV Program	SIC
106	SW-PLUS	2650	2650	LAN	Higher Level Language;Written in ANSI FORTRAN IV	SIC
107	SW-8X00MA1000SS	3001,2	3000	ASB	Micro Assembler;Written in ANSI FORTRAN IV	SIC
108	SW-8X300AS100SS	8X300	N8X300	ASB	Micro Controller Cross Assembly Program or MCCAP:8x300 Cross Assembler	SIC
109	SW-8X300TC100SD	8X300	N8X300	SSS	N8X300 Programming Course;Audio/Visual Self Paced Cource	SIC
110#	SW-SMP80-MON1▼	8080	SMP80	MON	Monitor Program:For Monitoring/Testing of User Program on SMP80 System	SIEG

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATE-GORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	1 MFR. CODE
1	SW-MICROBASIC	8085	SSM-85	LAN	8085 MICRO BASIC:Modified Version of Palo Alto BASIC	SSC
2	SW-SSM2KMON▼	8080	SSM-S100	MON	Monitor Progm For 8080 Syst:Resident in Eight 1702 or Two 2708 EPROMs	SSM
3	SW-MPE	6800	SWTPC6800	ASB	Editor/Assembler Package	STP
4	SW-BAS-1	6500	SY6500	LAN	SYM BASIC	SYK
5	SW-EPS-1	6500	SY6500	DIA	SYM Diagnostic	SYK
6	SW-RAE-1	6500	SY6500	ASB	Resident Assembler/Editor;ROM	SYK
7	SW-SYSTEM65▼	6500	SY6500	OPS	Development System;ROM Resident Software;Debug, Text Editor,Assembler	SYK
8	SW-ASED-TAI	8080	TOKOM80	ASB	Assembler and Editor on System File Base	TAI
9	SW-CAS-TAI	8080	TOKOM80	ASB	Cross Assembler;Generates Object Codes from Symbolic Assembly Language	TAI
10	SW-DAP-TAI▼	8080	TOKOM80	DEB	Debugging Aids Program:Loader Hex Mem Dump,Editor,Execution Control	TAI
11	SW-IOT-TAI	8080	TOKOM80	DIA	I/O Test Programs;For TTY,PTR and Printer	TAI
12	SW-RA4K-TAI	8080	TOKOM80	ASB	Resident Assembler;For 4k Bytes System	TAI
13	SW-RA8K-TAI	8080	TOKOM80	ASB	Resident Assembler;For 8k Bytes System	TAI
14	SW-TEKDOS	8002	8002	OPS	Disk Operate System;Calls up Editor/Assembler Software,Debug,PROM,Prg	TEKT
15	SW-TMS8080#1	8080	TMS8080	ASB	Assembler;FORTRAN H With XL Option;IBM 360ALC;Batch Mode IBM 360/370	TII
16	SW-TMS8080#2	8080	TMS8080	SIM	Simulator;Batch or Interactive Mode,IBM 370	TII
17	SW-TMSW753P-3	990	FS990/4	EDT	Floppy Diskette for FS990 911 or 913 Video Display Terminal	TII
18	SW-TMSW754P-10	990	FS990/4	EDT	Diablo Disk for DS990	TII
19	SW-TMSW754P-4	990	FS990/4	EDT	Hawke Disk for DS990	TII
20	SW-TMSW754P-7	990	FS990/4	EDT	800 BPI Magnetic Tape for DS990	TII
21	SW-TMSW754P-8	990	FS990/4	EDT	1600 BPI Magnetic Tape for DS990	TII
22	SW-TMSW990/510F	990	FS990/4	LAN	Power Basic Set of Floppy Diskettes	TII
23	SW-TM990/402-1▼	990/9900	TM990/100M	ASB	Line-By-Line ASB;Supports the TM990/100M;Consists of Two EPROMS	TII
24	SW-TM990/450▼	990/9900	TM990/100M	LAN	EDITS/Translates Basic Lan to 9900 Instruc;Offers Eval Tools;EPROM	TII
25	SW-TM990/451▼	990/9900	TM990/100M	LAN	EDITS/Translates Basic Lan to 9900 Instruc;Des,Dev,Debug,Prog Cap;ROM	TII
26	SW-TM990/452▼	990/9900	TM990/100M	LAN	EDITS/Translates Basic Lan to 9900 Instruc;Provides Utilities;EPROM	TII
27	SW-TM990/402-2▼	990/9900	TM990/180M	ASB	Line-By-Line ASB;Supports the TM990/180M;Consists of One EPROM	TII
28	SW-TMSW303D	9900	FS990	ASB	TiPMX Executive Library	TII
29	SW-TMSW301F	9900	FS990/4	ASB	TiPMX Executive Library	TII
30	SW-TM990/430	9900	TMS9900	LAN	TI Pascal Microprocessor Executive Library	TII
31	SW-TMSW101T-17	9900	TMS9900	SSS	System Software Package	TII
32	SW-TMSW101T-18	9900	TMS9900	SSS	System Software Package	TII
33	SW-TM990/401-3	9900	TM990	MON	TIEBUG;Monitor Listing;Detects/Supports Baud Rates;Used w/TMS9902	TII
34	SW-TMSW510F	9900	TM990	MFS	POWER BASIC for FS990 Minicomputer;Uses Floppy Disk System	TII
35	SW-AMPL	9900	TM990/100M	SSS	AMPL Phototyping System	TII
36	SW-DX10	9900	TM990/100M	MFS	Multi Software Devel Syst;Includes Assembler,Editor,Librarian,FORTRAN	TII
37	SW-TIBUG▼	9900	TM990/100M	MON	Debug Monitor Program	TII
38	SW-990-733ASR	9900	990	SSS	System Software Package	TII
39	SW-SDSMAC	9900	990	ASB	Multi-Pass Assembler;National CSS,Tymshare and GE Timeshare Networks	TII
40	SW-TX990	9900	990	OPS	Terminal Executive Operating System	TII
41	SW-PROMPRO	6800	MIKUL600	SSS	Control Program for MIKUL 698 PROM Programmer	TLI
42	SW-T9BUG	6800	MIKUL6000	MFS	Monitor,Debug Utilities for MIKUL 6000 Systems	TLI
43	SW-TBUG	6800	MILUL600	MFS	Monitor/Debug/Utilities for MIKUL 600 Systems	TLI
44#	SW-TLCS12A-V1/ACOS			ASB	TLCS-12A Cross Assembler Version 1/ACOS	TOSJ
45#	SW-TLCS12A-V3/ACOS			ASB	TLCS-12A Cross Assembler Version 3/ACOS	TOSJ
46#	SW-TLCS12A/T40			ASB	TLCS-12A Cross Assembler Version/T40	TOSJ
47#	SW-TLCS12	TLCS12	TLCS12	SIM	Simulate Progm,FORTRAN:Cross Assembler;Simulator,Cross Compiler,Editor	TOSJ
48#	SW-TLCS12EX-1#1	TLCS12	TLCS12	SUB	Basic Subroutine;Arith Routine;Control Routine;Data Conv Routine	TOSJ
49#	SW-TLCS12EX-1#2	TLCS12	TLCS12	MFS	Self Programming System;Assembler,Loader,Service Program A and B	TOSJ
50	SW-ASSEM	MECA43	MECA43	ASB	Assembler:Cat:Software Generation;Language:FORTRAN IV,JOVIAL J73/I	TSC
51	SW-CG	MECA43	MECA43	SSS	Code Generator:Category:Software Generation;Language:JOVIAL J73/I	TSC
52	SW-COM	MECA43	MECA43	CMP	Compiler J73/I:Category:Software Generation;Language:JOVIAL J73/I	TSC
53	SW-DP	MECA43	MECA43	DIA	Diagnostic Programs;Cat:Hardware Verification;Lan:MECA43 Assembler	TSC
54	SW-IS	MECA43	MECA43	SIM	Interpretive Sim:Cat:Softw Verification;Lan:FORTRAN IV,JOVIAL J73/I	TSC
55	SW-LE	MECA43	MECA43	EDT	Linkage Edit:Cat:Software Generation;Language:Fortran IV,JOVIAL J73/I	TSC
56	SW-LOA	MECA43	MECA43	LOA	Loader:Cat. Software Generation;Language:PDP11 Assembler	TSC
57	SW-MCCA	MECA43	MECA43	ASB	Micro Code Cross Assembler:Hardware Support;Language:JOVIAL J73/I	TSC
58	SW-ML	MECA43	MECA43	LOA	Microprogram Loader:Hardware Support;Language:PDP11 Assembler	TSC
59	SW-TSP	MECA43	MECA43	DIA	Test Set Programs:Cat:Soft/Hardware Verification;Lan:PDP11 Assembler	TSC
60	SW-UP	MECA43	MECA43	SSS	Utility Programs:Category:Software Verification;Lan:MECA43 Assembler	TSC
61	SW-APL	Z80	VECTOR MZ	LAN	Full APL Language,Interactive	VGI
62	SW-CCA-DMS	Z80	VECTOR MZ	BAS	Data Management System In MBASIC	VGI
63	SW-CIS-COBOL	Z80	VECTOR MZ	LAN	Interactive Std Version/Runs Under CP/M	VGI
64	SW-CP/MEDITOR	Z80	VECTOR MZ	EDT	Advanced Screen Oriented Line Editor for CP/M	VGI
65	SW-EVIOS	Z80	VECTOR MZ	MON	Extended Video I/O For AVDB. Graphics,Screen Reading,etc.	VGI
66	SW-MBASIC	Z80	VECTOR MZ	LAN	Powerful Disk Basic,Precision to 60 Digits	VGI
67	SW-MZOS	Z80	VECTOR MZ	OPS	North Star DOS Compatible,But on Micropolis Disk	VGI
68	SW-UNASSEMBLER	Z80	VECTOR MZ	SSS	Dis-assembles Z80 Code	VGI
69	SW-UNIVID	Z80	VECTOR MZ	SIM	Extended Video I/O For AVDB2.Emulates Popular Terminals	VGI
70	SW-WMS	Z80	VECTOR MZ	EDT	Full Word Processing Software For Mem-Mapped Display	VGI
71	SW-ZSM	Z80	VECTOR MZ	ASB	Assembles Z80 Code,Linking Files,Conditional Assembly	VGI
72	SW-BASIC	8080	VECTOR1	LAN	BASIC Interpreter;Unlimited String Length;8 Commands, 18 Functions	VGI
73	SW-ESM	8080	VECTOR1	MON	Extended System Monitor;Provides 25 Commands, Requires 1k Byte PROM	VGI
74	SW-CP/M	8080/Z80	VECTOR1,MZ	OPS	Industry Standard Operating System	VGI
75	SW-MTX11	LSI11	LSI11	MON	Multitasking Executive;Ensures Real Time Control Of Multiple Tasks	VIR
76	SW-COGENTII	MULTI$	LSI11/PDP11	ASB	Accepts Metalanguage Description W/Syntax,Semantics,and Produces CMP	VIR
77	SW-Z80AL	Z80	Z80	ASB	Cross Assembler, Linking Loader For Zilog Z80, Runs on PDP-11	VIR
78	SW-6800AL	6800	M6800	ASB	Cross Assembler, Linking Loader For Motorola 6800, Runs on PDP-11	VIR
79	SW-8048/8748AL	8048/8748	LSI11/PDP11	ASB	Cross Dev SW;Generates Object Code,Linking Loader;For ITL 8048/8748	VIR
80	SW-8080/8085AL	8080,8085	MCS80,85	ASB	Cross Assembler, Linking Loader For Intel 8080/8085, Runs on PDP-11	VIR
81	SW-8086AL	8086	LSI11/PDP11	ASB	Cross Dev SW;Generates Object Code,Linking Loader;For ITL 8086	VIR
82	SW-MCP1600#1	1600	MCP1600	ASB	Assembler;Prepares Source and Output Listing and Binary File	WDC
83	SW-MCP1600#2	1600	MCP1600	SIM	Simulator;Provides Interactive Simulation of Program	WDC
84	SW-MCP1600#3	1600	MCP1600	SSS	ROMGEM;Generates Output Tapes for MICROM Patterns,PTA Patterns	WDC
85	SW-DEBUG	8080	uP Series	DEB	Debug Program on Paper Tape or ERPROM	WLD
86	SW-MATH	8080	uP Series	SUB	Math and Trigonometric Handlers on Paper Tape or ERPROM	WLD
87	SW-MODS	8080	uP Series	OPS	Microcomputer On-Line Development System	WLD
88	SW-PCB	8080	uP Series	LAN	Process Control BASIC Compiler;PDP-11 Resident	WLD
89	SW-PCB-EXTENDED	8080	uP Series	LAN	Process Control BASIC W/Extended Utilities,Paper Tape,EPROM	WLD
90	SW-REA-1	8080	uP Series	ASB	Resident Editor/Assembler;Available on Paper Tape or ERPROM	WLD
91	SW-uPSeries	8080	uP Series	ASB	Cross Assembler	WLD
92	SW-XAS-11	8080	uP Series	ASB	PDP-11/8080A Cross Assembler;Output on Paper Tape	WLD
93▼	SW-CAS00	6800		ASB	6800/6801 Cross-Assembler;2 Pass Assembler in Standard Fortran	WTK
94▼	SW-CCC00	6800		MFS	Cross-Assembler-Compiler-Linker-Floating Point and Simulator	WTK
95▼	SW-CFP00	6800		MFS	Cross-Floating Point Scientific Functions;Relocatable 6800 Assm Lang	WTK
96▼	SW-CLL00	6800		LOA	Cross-Linker;Standard Fortran;used for Linking w/MOTA CPU 6800/1/2 ETC	WTK
97▼	SW-CPL00	6800		CMP	P L/W Cross-Compiler;Block Structured Language	WTK
98▼	SW-CSM00	6800		SIM	6800 Simulator;Simulates Execution all 6800 uP Instru/Conditions	WTK
99▼	SW-RCB04	6800		LAN	Resident SW;300 Baud in MIKBUG;4k Indust Basic on Cassette	WTK
100▼	SW-RCB12	6800		LAN	Resident SW;300 Baud in MIKBUG;12k Indust Basic on Cassette	WTK
101▼	SW-RCE00	6800		MFS	Editor/Assembler on Cassette;General Purpose Editor/Assembles Programs	WTK
102▼	SW-RCH00	6800		LOA	High Speed Load/Punch;Load from or Punch to Cassette	WTK
103▼	SW-RDL00	6800		MFS	PL/W Compiler/Linker;Linking Loader on 8in Diskette	WTK
104▼	SW-RRB04	6800		EDT	Inudustrial Basic;ROM Module w/4-2708 EROMs w/4k Basic	WTK
105▼	SW-RRF00	6800		MFS	68308 ROM w/FANTOM-II;1k Loader/Monitor/Debugger for 6800 in ROM	WTK
106▼	SW-RRF01	6800		MFS	2708 EROM w/FANTOM-IIS;1k Loader/Monitor/Debugger for 6800 in ROM	WTK
107▼	SW-RRT00	6800		DOS	Boot-1 in 2708 EROM;for Control Module ROM;Based Sys w/WizRD	WTK
108	SW-CA6800	6800	CM6800	ASB	Cross Assem;FORTRAN IV;PDP11,IBM360,CDC6500,PD10-TYMSHARE Computer Nwk	WTK
109	SW-CAR90	6800	CM6800	ASB	6809 Cross Assembler	WTK
110	SW-FANTOM-II▼	6800	CM6800	MON	Monitor-Debugger Program with Single Step for 6800	WTK

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IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	[4] SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	[2] GENERIC I.D. $-MULTI-SYSTEM APPLICATION	[3] SYSTEM TYPE No.	CATE-GORY	S O F T W A R E L I B R A R Y NOTE: For Specific Software Compatibility Consult Manufacturer NAME LANGUAGE AVAILABILITY/COMPATIBILITY	[1] MFR. CODE
1	SW-LL6800	6800	CM6800	LOA	Link Loader;FORTRAN IV;PDP11,IBM360,CDC6500,PD10-TYMSHARE Computer Nwk	WTK
2	SW-PLW6800	6800	CM6800	CMP	Compiler;FORTRAN IV;PDP11,IBM360,CDC6500,PD10-TYMSHARE Computer Nwk	WTK
3	SW-RB6800#1	6800	CM6800	LAN	8k Basic for 6800	WTK
4	SW-RB6800#2	6800	CM6800	LAN	12k Basic for 6800	WTK
5	SW-RDC00	6800	CM6800	CMP	C Compiler	WTK
6	SW-RDP00	6800	CM6800	CMP	PL/W Compiler	WTK
7	SW-RDW00	6800	CM6800	OPS	Disk Operating System	WTK
8	SW-RE6800	6800	CM6800	EDT	Resident Editor for 6800	WTK
9	SW-RRM00	6800	CM6800	Sub	Floating Point-Long Integer Math Routines	WTK
10	SW-SM6800	6800	CM6800	SIM	Simulator;FORTRAN IV;PDP11,IBM360,CDC6500,PD10-TYMSHARE Computer Ntwk	WTK
11▼	SW-CAS90	6809		ASB	6809 Cross-Assembler;	WTK
12	SW-ZAPPLE-FORTRAN	Z80	ALPA	LAN	ZAPPLE FORTRAN;ANSI Standard FORTRAN IV	XIT
13	SW-FORTRAN	Z80	ZPU-2	LAN	ANSI Std Fortran IV;For CPM Operating System	XIT
14	SW-ZBUG	Z80	ZPU-2	DEB	Disk-Programmed Debugging Utility;For ELDOS or CPM Operating Systems	XIT
15	SW-PDS-Z8-SDP	Z8	PDS	DEV	Z8SDP;Development Pkg on Diskette and Cartridge Disk	ZIL
16	SW-ZDS-Z8-SDP	Z8	ZDS	DEV	Z8SDP; Development Pkg on Diskette for ZDS1/25 or ZDS1/40	ZIL
17	SW-PDS-ASYNC	Z80	PDS	LOA	Z80-ASYNC;Communications on Diskette,Cartridge Disk for PDS8000 Series	ZIL
18	SW-PDS-BASIC	Z80	PDS	EDT	Z80-Basic;Interpreter on Diskette and Cartridge for PDS8000 Series	ZIL
19	SW-PDS-COBOL	Z80	PDS	CMP	Z80-COBOL;Compiler and RTI on Diskette, Cart Disk	ZIL
20	SW-PDS-FORTRAN	Z80	PDS	CMP	Z80-FORTRAN;Compiler and RTI;Diskette and Docu Pkg/PDS8000,ZDS Series	ZIL
21	SW-PDS-MACP	Z80	PDS	ASB	MACP;Macro Processing on Diskette, Cartridge Disk/PDS8000,ZDS Series	ZIL
22	SW-PDS-PASCAL	Z80	PDS	CMP	Z80-PASCAL;Compiler/Interpreter on Diskette,Cent Disk/PDS8000 and ZDS	ZIL
23	SW-PDS-PLZ	Z80	PDS	CMP	Z80-PLZ;Language Compiler on Diskette,Cart Disk/PDS8000,ZDS Series	ZIL
24	SW-PDS-ZFORM	Z80	PDS	SSS	ZFORM;Text Formatting Pkg on Diskette and Cartridge Disk/PDS8000,ZDS	ZIL
25	SW-Z8000SDP	Z80	PDS	OPS	Includes Z8000;PLZ/ASM,Linker,Translator,Load Send,ZPROG 8000	ZIL
26	SW-ZDS1/25-DCP	Z80	ZDS	DEB	ZDS-1/25 Debug Command Package:Resedent In 3k PROM, 1k RAM, For Debug	ZIL
27	SW-ZDS1/40-DCP	Z80	ZDS	DEB	ZDS-1/40 Debug Command Package:Provides Disc Based Software Support	ZIL
28	SW-ZDS-ASYNC	Z80	ZDS	LOA	Z80-ASYNC; Communications Pkg on Diskette for ZDS1/25 or ZDS1/40	ZIL
29	SW-ZDS-BASIC	Z80	ZDS	LAN	BASIC Language Interpreter Subsystem	ZIL
30	SW-ZDS-FORTRAN	Z80	ZDS	LAN	FORTRAN IV For ZDS Development System	ZIL
31	SW-ZDS-MACP	Z80	ZDS	ASB	MACP;Macro Processing Pkg on Diskette for ZDS1/25 or ZDS1/40	ZIL
32	SW-ZDS-PASCAL	Z80	ZDS	CMP	Z80-PASCAL;Compiler/Interpreter on Diskette for ZDS1/25 or ZDS1/40	ZIL
33	SW-ZDS-PLZ	Z80	ZDS	LAN	PLZ Programming Language Implemented as Disk Based Programs	ZIL
34	SW-ZDS-RIO	Z80	ZDS	MFS	Z80-RIO;Includes OS Executive;Assembler,Linker,Editor,Mon,File Syst	ZIL
35	SW-PDS-Z8000-SDP	Z8000	PDS	DEV	Z8000SDP;Development Pkg on Diskette and Cartridge Disk	ZIL
36	SW-ZDS-Z8000-SDP	Z8000	ZDS	DEV	Z8000SDP Development Pkg on Diskette for ZDS1/25 or ZDS1/40	ZIL

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

5. INSTRUCTION SET INDEX

IN ORDER OF: (1)MANUFACTURER CODE &(2)SYSTEM TYPE No.

LINE No.	2 SYSTEM TYPE No. (IS-D.A.T.A. PREFIX)	No. BASIC INSTR	TOTAL No. INSTRUCTIONS W/VARIATIONS	SYMBOLS: DESCRIPTION	INSTRUCTION SET REFERENCE No.	INSTRUCT FORMAT DWG.	1 MFR. CODE
1	IS-AMC95/4000	74		Uses Am9080A Instruction Set	IS57		AuC
2	IS-S2000	51		8-Bit Instr Organiz in Two 4-Bit Bytes;Incl Appliance Control I/O Instr	IS79		AMI
3	IS-S6800	72	107	Include Binary,Decimal Arithmetic,Shift,Rotate,Load,Store,Branch,Etc	IS11	F2	AMI
4	IS-S9900	69	72	Single Address,Address Modes Include Work Space,Register,Indirect,Etc.	IS10	F5	AMI
5	IS-S9940	58		Subset of TMS9900 Family Instruction Set,Includes Arith,Program Cont	IS69		AMI
6	IS-S9980	69	72	Single Address,Address Modes Include Word Space,Register,Indirect,Etc.	IS10	F5	AMI
7	IS-Am2900	256		Microprogram Of Am2901 ALU And Am29811 Next Address Control Unit	IS63		AMV
8	IS-Am9080A	74		Decimal Arithmetic Capability;Multiple Byte Interrupt Instructions	IS57		AMV
9	IS-70-100	78	111	5 Types-Data Transfer,Arithmetic,Logical,Branch And Stack,I/O,Etc	IS57	F7	APP
10	IS-ASC40	45		4 Groups - Machine,14 Group Instructions,I/O And Accumulator	IS22	F14	APS
11	IS-ASC80	78	115	5 Types - Data,Transfer,Arithmetic,Logical,Branch And Stack I/O Etc	IS57	F7	APS
12	IS-ASCZ80	78	158	Basic Instr Set of 8080CPU With Additional 4,8 And 16 Bit Operations	IS64		APS
13	IS-CSS-1143	158		Uses Z80 Instruction Set;Includes All 78 of 8080A	IS65		CLI
14	IS-LSERIES	78		Include Double Precision,Decimal Arith;Prog Counter,Stack Control,Etc	IS29		CLI
15	IS-MSERIES	78		Include Double Precision,Decimal Arith;Prog Counter,Stack Control,Etc	IS29		CLI
16	IS-IMC40	60		Include Binary And Decimal Arithmetic Modes	IS56		COM
17	IS-Z2	158		Z80 Instructions:Basic Inst Set of 8080 CPU Plus 4,8,16B Operations	IS65		CRO
18	IS-LSI11	74	400	Single And Double Oper And Instructions;PDP11/40 Inst Set	IS17	F13	DEC
19	IS-PDP11/03	74	400	Single And Double Oper And Instructions;PDP11/40 Inst Set	IS17	F13	DEC
20	IS-MBC/1	41		Uses MICRONOVA,mN601 CPU Instruction Set	IS66		DGC
21	IS-MICRONOVA	41		16 Bit Instr Grouped into 6 Basic Formats;5 Addr Modes for Memory Instr	IS66		DGC
22	IS-TDG6500SYS	55		13 Address Modes,Decimal,Binary And Arithmetic	IS83		DIG
23	IS-TDG6800SYS	72		Include ACCX,Immediate,Direct,Extended,Indexed,Implied,Relative Address	IS6		DIG
24	IS-TDG8080SYS	78		5 Types-Data Transf,Arithm,Log,Branch and Stack,I/O,Etc	IS57		DIG
25	IS-TDGZ80SYS	78	158	Basic Instruction Set of Z80 CPU with Extensive 16 Bit Arithmetic	IS65		DIG
26	IS-M80	72	111	5 Types-Data Transf,Arithm,Log,Branch and Stack,I/O Etc	IS57	F7	DSI
27	IS-SYSTEM4	45		Executes Up to 80k Instructions Per Second	IS14		DSI
28	IS-SYSTEM4A	60		Executes Up to 80k Instructions Per Second	IS14		DSI
29	IS-SYSTEM4B	60		Executes Up to 80k Instructions Per Second	IS14		DSI
30	IS-SYSTEM8	72	111	5 Types-Data Trans,Arith,Log,Branch and Stack,I/O ETC	IS57		DSI
31	IS-SYSTEM8A	134		6 Inst Formats;Reg,Imm,Mem Ref,Move,Jump,Skip,Accum,I/O ETC	IS5		DSI
32	IS-DB8/1	158		Uses Z80 Instruction Set,Including 78 Instructions of 8080	IS65		DYB
33	IS-DMS	72	107	Include Binary,Decimal Arithmetic,Logical,Shift,Rotate,Etc	IS6	F11	DYN
34▼#	IS-68A00C	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
35▼#	IS-68A00CV	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
36▼#	IS-68A00P	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
37▼#	IS-68A00PV	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
38▼#	IS-68B00C	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
39▼#	IS-68B00P	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
40▼#	IS-EF6800C	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
41▼#	IS-EF6800CV	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
42▼#	IS-EF6800P	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
43▼#	IS-EF6800PV	72	72	Include Binary,Decimal,Arithmetic,ETC;Conditional/Unconditional Branch	IS6		EFCF
44▼#	IS-EF6805P2C	59	64	5 Diff Types Regis/Mem,Read/Modify/Write,Branch,Bit Manip and Contr	IS114a		EFCF
45▼#	IS-EF6805P2J	59	64	5 Diff Types Regis/Mem,Read/Modify/Write,Branch,Bit Manip and Contr	IS114a		EFCF
46▼#	IS-EF6805P2P	59	64	5 Diff Types Regis/Mem,Read/Modify/Write,Branch,Bit Manip and Contr	IS114a		EFCF
47▼#	IS-SFF9-68A09E	59	72	Include Load,Store,Compare,Add,Subtract,Transfer,Exchange,Push and Pull			EFCF
48▼#	IS-SFF9-68B09E	59	72	Include Load,Store,Compare,Add,Subtract,Transfer,Exchange,Push and Pull			EFCF
49▼#	IS-SFF9-68B09K	59	79	Include load,Store,Compare,Add,Subtract,Transfer,Exchange,Push and Pull			EFCF
50▼#	IS-SFF9-6809E	59	72	Include Load,Store,Compare,Add,Subtract,Transfer,Exchange,Push and Pull			EFCF
51▼#	IS-SFF9-6809K	59	72	Include Load,Store,Compare,Add,Subtract,Transfer,Exchange,Push and Pull			EFCF
52	IS-9440	35	2192	4 Classes of Multifunction Instructions for Efficient Memory Usage	IS107		FSC
53	IS-F8	76		2.0us Inst Cycle;Binary And Decimal Arithmetic	IS20		FSC
54	IS-F2900	512		Microprogram of 2901 Slice,With 9 Bit Microcode	IS63		FSC
55	IS-F3850	71		F8 Compatible, Powerful Arith Logic,Variety of Data Manipulations	IS123		FSC
56	IS-F3870	76		F 8 Compatible;Includes Accumulator Group,Branch,Memory Reference,Etc	IS20		FSC
57	IS-F6800	72		Addressing Modes-Accumulator,Immediate,Direct,Extended,Indexed,Etc	IS6	F25	FSC
58	IS-F6802	72		Binary/Decimal Arith,Logical,Shift,Rotate,Load,Store,Cond/UnCond Branch	IS6		FSC
59	IS-F6808	72		Same as F6800 w/Internal Clock Oscillator and Driver on the Same Chip	IS6	F25	FSC
60	IS-OCM-1	76		Based on F8 System;Binary and Decimal Arithmetic	IS20		FSC
61	IS-GA16/110	91		Several Hundred Variations For Data Acquis,Comm,Processing And Control	IS44		GEN
62	IS-GA16/220	91		Several Hundred Variations For Data Acquis,Comm,Processing And Control	IS44		GEN
63	IS-GIC8000	48		Includes Shift,I/O,Jump and Subroutine Instruction	IS43		GIC
64	IS-GIMINI	87		Include Arithmetic And Logic,I/O,Reg,Control,Jump And Cond Branch	IS36	F20	GIC
65	IS-PIC1650	31		12 Bit Word Format,Single Bit Manipulation	IS74		GIC
66	IS-PIC1655	31		12 Bit Word Format,Single Bit Manipulation	IS74		GIC
67	IS-PIC1670	31		12 Bit Word Format,Single Bit Manipulation	IS74		GIC
68#	IS-LP8000	48		Include Shift,I/O,Jump And Subroutine Instruction	IS43		GICB
69	IS-HCMP1802	91	255	Direct I/O Control, Multi Register Addressing	IS38		HAC
70	IS-H18	130		16,32,48 Bit Instructions;Includes Direct Short,Extend,Etc Address Mode	IS110		HACC
71	IS-HB61000	67		12 Bit Word Instructions;3 Classes;Memory Ref,Operate,I/O,Transfer	IS3	F1	HAS
72	IS-HM6100	67		12 Bit Word Instructions;3 Classes;Memory Ref,Operate,I/O Transfer	IS3	F1	HAS
73	IS-ADAM-12	158		Uses Z80 Instruction Set Format	IS-122		HEU
74	IS-MLP8080	78	117	Include Subroutine Call,Push And Pop,And Subroutine Return	IS57		HEU
75	IS-MLZ80	78	158	Basic Instruction Set of Z80 With Additional Operations	IS65		HEU
76▼#	IS-HD68A09DC	59	72	Compat at Source Data Code Level;Similar to HD46800	IS6a		HITJ
77▼#	IS-HD68A09DP	59	72	Compat at Source Data Code Level;Similar to HD46800	IS6a		HITJ
78▼#	IS-HD68B09DC	59	72	Compat at Source Data Code Level;Similar to HD46800	IS6a		HITJ
79▼#	IS-HD68B09DP	59	72	Compat at Source Data Code Level;Similar to HD46800	IS6a		HITJ
80▼#	IS-HD6801DC	72	82	Compat w/6800 Instru Set;16 Bit Oper/Hardware Multiply	IS6a		HITJ
81▼#	IS-HD6801DP	72	82	Compat w/6800 Instru Set;16 Bit Oper/Hardware Multiply	IS6a		HITJ
82▼#	IS-HD6809DC	59	72	Compat at Source Data Code Level;Similar to HD46800	IS6a		HITJ
83▼#	IS-HD6809DP	59	72	Compat at Source Data Code Level;Similar to HD46800	IS6a		HITJ
84▼#	IS-HD68000DC	56	56	1-5 Words in Length;Data Move,Integer Arithmetic,Shifts/Rotates Etc	IS104		HITJ
85	IS-MX800	78	111	5 Types-Data Transer,Arithmetic,Logical,Branch And Stack,I/O,Etc	IS57	F7	ICC
86	IS-MM1	78		Basic Instr Set of 8080 CPU With Custom Programming thru Program Plugs	IS29		ICL
87	IS-I-8080	72		Uses 8080A Instruction Set	IS57		IMS
88	IS-PCS-40	74		Uses 8085 Instruction Set	IS57a		IMS
89	IS-PCS-42	74		Uses 8085 Instruction Set	IS57a		IMS
90	IS-PCS-44	74		Uses 8085 Instruction Set	IS57a		IMS
91	IS-VDP-40	74		Uses 8085 Instruction Set	IS57a		IMS
92	IS-VDP-42	74		Uses 8085 Instruction Set	IS57a		IMS
93	IS-VDP-44	74		Uses 8085 Instruction Set	IS57a		IMS
94	IS-VDP-80	113		Uses 8085 Instruction Set	IS57a		IMS
95	IS-3000ITL	512		512 Microinstruction Addressability,Over 40 Useful Functions	IS13	F8	ITL
96	IS-MCS4	46		Include Machine,Input/Output And RAM,And Accumulator Group Instructions	IS22a	F14	ITL
97	IS-MCS8	48		Include Data Manipulation,Binary Arithmetic,And Jump To Subroutines	IS64	F7	ITL
98	IS-MCS40	60		4 Groups-Machine,14 Group Instructions,I/O And Accumulator	IS22	F14	ITL
99	IS-MCS48	96		Includes 24 Reg, 26 Accum, 23 Transfer, 13 I/O Control Instructions	IS62		ITL
100	IS-MCS80	78	111	5 Types-Data Transf,Arithm,Log,Branch And Stack,I/O,Etc	IS57	F7	ITL
101	IS-MCS85	80	113	8080 Instruction Set Plus Two Interrupt Mask Instructions	IS57a		ITL
102	IS-MCS86	111		Contains Data/Cont Transfer,Arith,Logic,String Manipulation,Proc Cont	IS108		ITL
103	IS-UPI41	90		Groups;Data Moves,Flags,Cont,Subrout,Accum,Reg,Timer Oper,Br,IO Insts	IS75		ITL
104#	IS-MN1400	75		Includes Register,Mem,Arith,Logic,I/O Addressing Functions	IS72		MATJ
105#	IS-MN1402	57		Includes Register,Mem,Arith,Logic,I/O Addressing Functions	IS72		MATJ
106#	IS-MN1404	48		Includes Register,Mem,Arith,Logic,I/O Addressing Functions	IS72		MATJ
107#	IS-MN1405	75		Includes Register,Mem,Arith,Logic,I/O Addressing Functions	IS72		MATJ
108#	IS-MN1430	75		Includes Register,Mem,Arith,Logic,I/O Addressing Functions	IS72		MATJ
109#	IS-MN1498	68		Includes Register,Mem,Arith,Logic,I/O Addressing Functions	IS72		MATJ
110#	IS-MN1499	75		Includes Register,Mem,Arith,Logic,I/O Addressing Functions	IS72		MATJ

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

5. INSTRUCTION SET INDEX

IN ORDER OF: (1)MANUFACTURER CODE &(2)SYSTEM TYPE No.

LINE No.	[2] SYSTEM TYPE No. (IS-D.A.T.A. PREFIX)	No. BASIC INSTR	TOTAL No. INSTRUCTIONS W/VARIATIONS	SYMBOLS: DESCRIPTION	INSTRUCTION SET REFERENCE No.	INSTRUCT FORMAT DWG.	[1] MFR. CODE
1	IS-MICRO1	107		Multiprecision Arithmetic;Standard 21 Firmware,Addable To Instructions	IS32	F19	MID
2#	IS-MELCS8/2	78		8080A Instructions:5 Types-Data Transf,Arith,Log,Branch/Stack,I/O Etc	IS57		MITJ
3#	IS-MELPS8	78		8080A Instructions:5 Types-Data Transf,Arith,Log,Branch/Stack,I/O Etc	IS57		MITJ
4#	IS-PCA0801	78		8080A Instructions:5 Types-Data Transf,Arith,Log,Branch/Stack,I/O Etc	IS57		MITJ
5	IS-5701	36		Microprogrammable;Inst In 32x9 ROM Can Be Modified In 8 Diff Ways	IS18		MMI
6	IS-6701	36		Microprogrammable;Inst In 32x9 ROM Can Be Modified In 8 Diff Ways	IS18		MMI
7	IS-AID-80F	78	158	Basic Instruction Set Of Z80 CPU With Extensive 16 Bit Arithmetic	IS65		MOS
8	IS-EMU-70	76		2.0us Inst Cycle;Binary and Decimal Arithmetic	IS20		MOS
9	IS-F8-MOS	76	243	2.0uS Inst Cycle;Binary and Decimal Arithmatic	IS20		MOS
10	IS-MD-SBC1	78		Uses Z80 Instruction Set	IS65		MOS
11	IS-MK3870	76		F8 Compatable;Includes Accumulator Group;Branch,Memory Reference	IS20		MOS
12	IS-MK3872	76		2.0us Inst Cycle;Binary and Decimal Arithmetic	IS20		MOS
13	IS-MK3876	76		Uses F-8 Instruction Set	IS20	DL167	MOS
14	IS-MK97400	70		Same Instruction Set as MK3874	IS20	S73a	MOS
15	IS-MK97401	70		Same Instruction Set as MK3874	IS20	S73a	MOS
16	IS-MK97402	70		Same Instruction Set as MK3874	IS20	S73a	MOS
17	IS-MK97403	70		Same Instruction Set as MK3874	IS20	S73a	MOS
18	IS-MK97404	70		Same Instruction Set as MK3874	IS20	S73a	MOS
19	IS-MK97405	70		Same Instruction Set as MK3874	IS20	S73a	MOS
20	IS-MKB3870P10	76		Uses F-8 Instruction Set	IS20	S73a	MOS
21	IS-MKB3870P	76		Uses F-8 Instruction Set	IS20	S73a	MOS
22	IS-OEM-80	78	158	Basic Instruction Set of Z80 CPU With Extensive 16 Bit Arithmetic	IS65		MOS
23	IS-SDB-80	78	158	Basic Instruction Set of Z80 CPU With Extensive 16 Bit Arithmetic	IS65		MOS
24	IS-M68MM01	72	107	Include Binary,Decimal Arithmetic,Logical,Shift,Rotate	IS6		MOTA
25	IS-M68MM01A	72	107	Include Binary,Decimal Arithmetic,Logical,Shift,Rotate	IS6		MOTA
26	IS-M2900	512		Microprogram of M2901ALU and M29811 Next Address Control Unit	IS63		MOTA
27	IS-M6800	72	107	Include Binary,Decimal Arithmetic,Logical,Shift,Rotate,Etc	IS6	F11	MOTA
28	IS-M10800	16		Basic Microprogram Sequencing Instr Incl Jump,Branch To Subroutine	IS61		MOTA
29	IS-MC3870	76		2.0us Instruction Cycle;Binary and Decimal Arithmetic	IS20		MOTA
30	IS-MC6801	82		Implements 72 MC6800 Instructions Plus 10 New Instructions	IS6a		MOTA
31	IS-MC6803			Implements Full MC6800 Instructions Plus Several New Instructions	IS6a		MOTA
32	IS-MC6805	61		Instruction Groups:Reg/Mem,Read/Modify/Write,Bit Manipul,Branch,Control	IS114	F11a	MOTA
33	IS-MC14500B	16		Include Accumulating Result Reg,Complement,ANDC,OR,ORC,XNOR,STOC,IEN	IS73		MOTA
34	IS-MC68000	61		Includes Signed/Unsigned Multiply,Divide,BCD Arith,Quick Arith	IS104		MOTA
35	IS-MC141000	43		IO,Data From ROM,Bit Control,Data Transfer,Arith/Logic,Branching,Subrt	IS90		MOTA
36	IS-MC141099	43		IO,Data from ROM,Bit Control,Data Transfer,Arith/Logic,Branching,Subrt	IS90		MOTA
37	IS-MC141200	43		IO,Data From ROM,Bit Control,Data Transfer,Arith/Logic,Branching,Subrt	IS90		MOTA
38	IS-MSC8001-Z80	78	158	Basic Instr Set of Z80 CPU With Additional 4,8 and 16 Bit Operations	IS65		MSCC
39	IS-MCS6500	55	146	13 Address Modes;Decimal And Binary Arithmetic	IS83	F9	MTY
40	IS-808AMULT	72		5 Types-Data Transf,Arithm,Log,Branch and Stack,I/O,Etc	IS57		MUL
41	IS-MS801	48		Include Data Manipulating,Binary Arithmetic And Jump To Subroutines	IS64	F7	MUL
42	IS-MS808A	78	111	5 Types-Data Transfer,Arithmetic,Logical,Branch And Stack,I/O,Etc	IS57	F7	MUL
43	IS-muPRO80	78	111	5 Types-Data Transfer,Arithmetic,Logical,Branch And Stack I/O,Etc.	IS57		MUP
44#	IS-NASCOMI	158	694	Z80 Instruction Set	IS65		NASB
45#	IS-TK80	78		Includes Arith And Logical Operators W/Direct,Register,Indirect,Immed	IS55	F26	NECD
46#	IS-uCOM-4	55		W/Control;Address/Data Load/Stor;Skip;Indirect Load Inst;Arith/Logic Op	IS60		NECJ
47#	IS-uCOM-41	79		Includes Acc, Skip Operations	IS59		NECJ
48#	IS-uCOM-43C	96		Expanded Version of IS 81 Incl Interrupt Enable/Disable,3 Level Stack	IS8/a		NECJ
49#	IS-uCOM-47	103		Includes Acc,Skip Operations	IS86		NECJ
50	IS-uCOM-8	78		Includes Arithmetic And Logical Operators W/Direct,Register,Indir,Immed	IS55	F26	NECM
51	IS-uPD780	158		Incl 78 of the 8080A Instructions;16 Categories of Instructions	IS65		NECM
52	IS-NMS85/P	80		8085 Instructions:8080 Inst Set Plus 2 Interrupt Mask Instructions	IS57a		NMS
53	IS-BLC80/10	78	111	Address Modes Include Direct,Register,Register Indirect,Immediate	IS57		NSC
54	IS-IDM2900	512		Microprogram of 2901 Slice,with 9 Bit Microcode	IS63		NSC
55	IS-IMP16C	43	60	Total Instr Include Extended Instr Set Implemented By 2nd Control-ROM	IS42		NSC
56	IS-IMP16L	43	60	Total Instr Include Extended Instr Set Implemented By 2nd Control-ROM	IS42		NSC
57	IS-IMP16P	43	60	Total Instr Include Extended Instr Set Implemented By 2nd Control-ROM	IS42		NSC
58	IS-INS8900	45	337	Address Modes;PC-Relative,Base Page,Indexed,Direct And Indirect	IS99		NSC
59	IS-IPC16C	45	337	8 Format Groups;Branch,Skip,Memory Transfer,Memory Operate Reg,Etc.	IS40		NSC
60	IS-IPC16P	45	337	8 Format Groups;Branch,Skip,Memory Transfer,Memory Operate Reg,Etc	IS40		NSC
61	IS-MM5781/82	52		16 Kilobits of ROM Organized as 32 Pages of 64x8 Bit Inst Word Each	IS92a		NSC
62	IS-MM5799N	51		1536 Words x8 Bit Instruction ROM	IS92		NSC
63	IS-MM5714ON	36		630 Words x8 Bit Instruction ROM	IS91		NSC
64	IS-N8080A	78	111	Address Modes Include Direct,Register,Register Indirect,Immediate	IS57		NSC
65	IS-SC/MP	46		9 Functional Groups;Addr Modes:PC-Relative,Auto-Inded;Indexed,Immediate	IS70		NSC
66#	IS-PFL16A	33	345	Include Byte Processing,Bit Operation,Decimal Arith,Stack Operation,Etc	IS30	F17	PAFJ
67	IS-EQUINOX-100	78		Uses 8080A Instruction Set,5 Types of Data Transfer	IS57		PAR
68	IS-PCM-12A	67		12 Bit Work Instructions;3 Classes;Memory Ref,Operate,I/O Transfer	IS3	F1	PCM
69	IS-MICROPAC80A	78	111	5 Types-Data Transfer,Arithmetic,Logical,Branch And Stack,I/O,Etc	IS57	F7	PCS
70	IS-PCS1806	78		5 Types-Data Transf,Arithm,Log,Branch and Stack,I/O,Etc	IS57		PCS
71	IS-PCS1810	78		5 Types-Data Transf,Arithm,Log,Branch and Stack,I/O,Etc	IS57		PCS
72	IS-PCS1810A	78		5 Types-Data Transf,Arith,Log,Branch and Stack,I/O,Etc	IS57		PCS
73	IS-SUPERPAC180	78		5 Types-Data Transf,Arith,Log,Branch and Stack,I/O,Etc	IS57		PCS
74	IS-MIPROC16	83	170	Include Move,Jump,Logic,Arith,Shift,Control,I/O,Interrupt,Assembler	IS111	F18	PLM
75	IS-PLS-858	80	113	Basic 8080 Instr Set with Read and Set Interrupt Mask Instr Added	IS76		PRO
76	IS-PLS-868	78	107	Include Binary;Decimal Arithmetic;Shift,Rotate,Load,Store,Branch,Etc.	IS11	F2	PRO
77	IS-PLS-881	78		Include Register And Memory,Program Address Control,Restart Address,Etc	IS67		PRO
78	IS-PLS-888	78		Include Register And Memory,Program Address Control,Restart Address,Etc	IS67		PRO
79	IS-PLS-898	158		Basic Instruction Set of Z80CPU With Extensive 16 Bit Arithmetic	IS65		PRO
80	IS-SOL20/16	78		5 Types Data Transf,Arith,Log,Branch and Stack,I/O Etc	IS57		PRT
81	IS-SOL20/32	78		5 Types Data Transf,Arith,Log,Branch and Stack,I/O Etc	IS57		PRT
82	IS-SOLPC	78		5 Types Data Transf,Arith,Log,Branch and Stack,I/O Etc	IS57		PRT
83	IS-SOLSIA	78		5 Types Data Transf,Arith,Log,Branch and Stack,I/O Etc	IS57		PRT
84	IS-SOLSIIA	78		5 Types Data Transf,Arith,Log,Branch and Stack,I/O Etc	IS57		PRT
85	IS-SOLSIII	78		5 Types Data Transf,Arith,Log,Branch and Stack,I/O Etc	IS57		PRT
86	IS-SOLSIV	78		5 Types Data Transf,Arith,Log,Branch and Stack,I/O Etc	IS57		PRT
87	IS-QUAY90MPS		158	Instruction Set of Z80 CPU W/8,16 Bit Operations	IS65		QUY
88	IS-QUAY8000		158	Instruction Set of Z80 CPU W/8,16 Bit Operations	IS65		QUY
89	IS-CDP1800	91	255	Basic Instr Set of 1802CPU;Expanded to 106 Instr for 1804CPU	IS38		RCA
90	IS-CMC68/15	72		6800 Instruction Set:Includes Bin,Dec Arithmetic,Logic,Shift Etc	IS6		RCI
91	IS-CMC68/15B	72		6800 Instruction Set:Includes Bin,Dec Arithmetic,Logic,Shift Etc	IS6		RCI
92	IS-CMC68/15C	72		6800 Instruction Set:Includes Bin,Dec Arithmetic,Logic,Shift Etc	IS6		RCI
93	IS-CMC68/15G	72		6800 Instruction Set:Includes Bin,Dec Arithmetic,Logic,Shift Etc	IS6		RCI
94	IS-MM75		69	RAM/ROM Address;Bit Manipulation;Arith,I/O;Transfer;Reg to Reg/Mem Inst	IS100		RKW
95	IS-MM78		68	RAM/ROM Address;Bit Manipulation;Arith,I/O;Transfer;Reg to Reg/Mem Inst	IS101		RKW
96	IS-PPS4/1	50		Multi-Function For Automatic Processing Manipulating Of Data	IS26		RKW
97	IS-R6500	56		Decimal/Binary Arithmetic Mode Selection;Include Accum,Immediate,etc.	IS83		RKW
98	IS-R6500/1	56		Decimal/Bin Arith Mode Selection; 13 Addressing Modes	IS83a		RKW
99	IS-SIA-2350	158		158 Instructions;Access Methods,Direct and Indexed			SIA
100	IS-SIA-3500	158		Data Types;Arithmetic,String,Dimensioned and Conversion			SIA
101	IS-2650	75	75	Include Load/Store Arithmetic,Logical,Compare,Rotate,Branch Functions	IS12	F4	SIC
102	IS-3000SIC	512		512 Micro Instruction Addressablility	IS13	F8	SIC
103	IS-ISP-8A/600I	46		SC/MP-II;Addressing;PC-Relative,Immediate,Indexed,Auto-Indexed	IS70		SIC
104	IS-MP8080AI	78	111	Data Transfer,Arith,Logical,Branch,Control Group Instructions	IS57		SIC
105	IS-N8X300	21		Fixed Instruction Set;8 Instruction Classes	IS78	F27	SIC
106	IS-SWTPC6800	72	107	Include ACCX,Immediate,Direct,Extended,Indexed,Implied,Relative Adress	IS6	F11	STP
107	IS-SY6500/1	53		Transf/Load,Arith/Logic,Rotate/Shift,Bit/Stack Manipulation,Jump/Call	IS83		SYK
108	IS-TOKOM80-01	78		5 Types-Data Transf, Arithm, Log, Branch And Stack, I/O, Etc	IS57	F7	TAI
109	IS-TOKOM80-02	78		5 Types-Data Transf, Arithm, Log, Branch And Stack, I/O, Etc	IS57	F7	TAI
110	IS-TOKOM80-03	78		5 Types-Data Transf, Arithm, Log, Branch And Stack, I/O, Etc	IS57	F7	TAI

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

5. INSTRUCTION SET INDEX

IN ORDER OF: (1)MANUFACTURER CODE &(2)SYSTEM TYPE No.

LINE No.	2 SYSTEM TYPE No. (IS-D.A.T.A. PREFIX)	No. BASIC INSTR	TOTAL No. INSTRUCTIONS W/VARIATIONS	SYMBOLS: DESCRIPTION	INSTRUCTION SET REFERENCE No.	INSTRUCT FORMAT DWG.	1 MFR. CODE
1	IS-TOKOM80-04	78		5 Types-Data Transf, Arithm, Log, Branch And Stack, I/O, Etc	IS57	F7	TAI
2	IS-TOKOM80-05	78		5 Types-Data Transf, Arithm, Log, Branch And Stack, I/O, Etc	IS57	F7	TAI
3	IS-990/4	69	72	Single Address,Address Modes Include Work Space;Register,Indirect,Etc	IS10	F5	TII
4	IS-S481	210		Expandable Micro/Macro,Add/Subtract,Logical Operations	IS85		TII
5	IS-SBP0400	76	512	Include Data-InBus,Extended WorkReg,RegFile And WorkReg Source Operands	IS47	F22	TII
6	IS-SBP0400A	76	512	Include Data-InBus,Extended WorkReg,RegFile And WorkReg Source Operands	IS47	F22	TII
7	IS-TM990/100M	69		7 Addressing Modes,9 Instruction Formats,16 Bit Word Instructions	IS95	F28	TII
8	IS-TMS1000	43	43	Include Register,Memory,Arithmetic,Logic,Inp,Outp,Addressing Functions	IS7		TII
9	IS-TMS1070	43	43	Include Register,Memory,Arithmetic,Logic,Inp,Outp,Addressing Functions	IS7		TII
10	IS-TMS1100	54	54	Include Register,Memory,Arithmetic,Logic,Inp,Outp,Addressing Functions	IS8		TII
11	IS-TMS1200	43	43	Include Register,Memory,Arithmetic,Logic,Inp,Outp,Addressing Functions	IS7		TII
12	IS-TMS1270	43	43	Include Register,Memory,Arithmetic,Logic,Inp,Outp,Addressing Functions	IS7		TII
13	IS-TMS1300	54	54	Include Register,Memory,Arithmetic,Logic,Inp,Outp,Addressing Functions	IS8		TII
14	IS-TMS8080	78	112	1,2 Or 3 Byte;Include Accum,I/O,Counter And Stack Control,Reg Functions	IS9	F7	TII
15	IS-TMS8080A	78	112	1,2 or 3 Byte,Include Accum,I/O,Counter and Stack Control,Reg Functions	IS9		TII
16	IS-TMS9940	58		Subset of TMS9900 Family Instruction Set,Includes Arith,Program Cont	IS69		TII
17	IS-TMS9980	69	72	Single Address,Address Modes Include Work Space,Register,Indirect,Etc	IS10	F5	TII
18	IS-MC6809	59	139	Address Modes Include:Inherent,Extended,Immed,Indexed,Relative	IS124		TLI
19	IS-MIKUL600	112		Include ACCX,Immediate,Direct,Extended,Indexed,Implied,Relative Address	IS6		TLI
20#	IS-TLCS12	18		Type I-Double Operand And Type II-Single/No Operand Inst	IS49		TOSJ
21#	IS-TLCS12A	19	108	Type I-Double Operand And Type II-Single/No Operand Inst	IS50		TOSJ
22	IS-MWPS	158	158	Instruction Set of Z80 CPU W/8,16 Bit Operations	IS65		VGI
23	IS-CR1872	20		Program Control;Parallel Data,Shift Area Operation Instructions	IS89		WDC
24	IS-MCP1600	84	98	Microinstruction Set Including Decimal Operation,1 Or 2 Microcycle Inst	IS15		WDC
25	IS-MP1600	112		Microinstruction Set;Data General NOVA Compatible I/O Inst	IS15		WDC
26	IS-WD4200	49		Arith,Control Transfer,Mem/Register Reference,Test and I/O Instructions	IS118		WDC
27	IS-WD9000	100		Inst Set for uP Chip Set,Computer on Card WD900 and Syst WD90	IS119		WDC
28	IS-uPSeries	72	111	5 Types-Data Transfer,Arithmetic,Logical,Branch And Stack,I/O,Etc	IS57	F7	WLD

6. SYSTEM INTERFACE

IN ORDER OF: (1)DATA BITS (2)MFR. CODE (3)SYSTEM TYPE No.

LINE No.	[3] SYSTEM TYPE No.	[1] DATA BITS	ADDRESSING: TYPE	ISOLATED DEVICES @ PORT WIDTH	MEMORY-SPACE DEV @ PT WIDTH	OPERATING MODE: TYPE of OP.	SERIAL No. BITS	INTERRUPT: V-vectored Pr-priority P-poll TYPE	No LNS	No LEV	S-softw,DMA I-interrupt INITI-ATION	DMA LOC.	I/O LINES: ADDR	SENS	CNTL	FLAG	MISC	TRANSFER: INSTR TIME (s)	OPER. CAPABILITY CODE	MAXIMUM BAUD RATE: ASYNC (BPS)	SYNC. (BPS)	SYSTEM DWG.	[2] MFR. CODE
1	MC14500B	1	B	32/1	256/1	S	1				S		4			2		1.0u		1.0M	1.0M	S89	MOTA
2	S2000	4	B	1/8	8k/8	PS					S	NA	13	9	6	0		4.0u	A			S93	AMI
3	Am2900	4	M		16/4	P		MPrV	8	8M	I		4					150n	A			S66	AMV
4	IMC40	4	B	64/4	4k/4	PS		P	1	1	S	NA	12	4	9	1		12u	AB	9.6k	19k	S58	COM
5#	MN1400	4	I	14/4		P		P	2	2	IS	NA	11	2	24	3		10u	A			S88	MATJ
6	M2900	4	M		16/4	P		MPV		8			4			4		150n	A			S66	MOTA
7	M10800	4	M		256/4	P							4			4		75n	A			S44	MOTA
8#	uCOM-4	4	M		120/8	P					S	NA	12	1	6	1		5.0u	A				NECJ
9#	uCOM-41	4	M		4/8	PS		V	5	4	S	NA	12	5		2	16	6.4u					NECJ
10#	uCOM-42	4	I	35/1				PrV	2	2		NA		1	2	1	34	10u				S109	NECJ
11#	uCOM-43C	4	1	35/1				V	1	1	S	NA			2	1	35	10u	A			S110	NECJ
12#	uCOM-44C	4	1	35/1							S	NA						10u	A			S111	NECJ
13	COP402	4	I	23/1		PS	4	PrV	2	2		NA	10		3	1	2	8.0u		250k	250k		NSC
14	COP410L	4	I	19/1		PS	4	PrV	1	1		NA			1	1	2	32uF		62k	62k		NSC
15	COP411L	4	I	15/1		PS	4	PrV	1	1		NA			1	1	2	32uF		62k	62k		NSC
16	COP420	4	I	23/1		PS	4	PrV	2	2		NA			1	1	2	8.0uF		250k	250k		NSC
17	COP420L	4	I	23/1		PS	4	PrV	2	2		NA			1	1	2	32uF		62k	62k		NSC
18	MM5781/82	4	I	24/1		PS	4	PrV	2	2		NA		5	2	1	13	10uF					NSC
19	MM5782/129	4	I	24/1		PS	4	PrV	2	2		NA		5	2	1	13	10uF					NSC
20	MM5799N	4	I	22/1		PS	4	PrV	1	1		NA		5	2	1	12	9.0uF				S124	NSC
21	MM57140N	4	I	24/1		PS		PrV	1	1		NA		5		2	12	15uF				S123	NSC
22	MM57152N	4	I	24/1		PS		PrV	1	1		NA		5		2	12	15uF					NSC
23	S6800	8	M		65k/16	PS	8	PPr	2		I	EXT	16		7	6			A			S1	AMI
24	70-100	8	I	256/8		PS	8	PrV	1	1	SI	CPU	8		3			5.0u	ABC	19	56k		APP
25	EVENT2000	8	I	256/8		PS	8	PrV	1	1	S	CPU						5.0u	B	76k	112k		APP
26	ASC80	8	B	256/8	256/8	PS	10	MV	8	8M	IS	EXT	14	4	5			2.0u	AB	9.6k	56k		APS
27	CSS-1143	8	B		64k/8	PS	8	MPr			IS	EXT			2	2		500n§	BC			S144	CLI
28	TDG6500SYS	8	M		512/8	PS	2	PrV	1	8	DIS	CPU	16					1.0u§	A	9.6k	9.6k		DIG
29	TDG6800SYS	8	M		512/8	P	2	PrV	1	8	DIS	CPU	16					1.0u§	A	9.6k	9.6k		DIG
30	TDG8080SYS	8	I	512/8		PS	2	PrV	8	8	DIS	CPU	16					500n§	AB	9.6k	9.6k		DIG
31	DB8/1	8	I	3/8		PS		V			IS		16		13				BC	9.6k			DYB
32	DMS	8	M		64k/8	PS	2	PPrV	6	8	IS	CPU		6	6			20u	AB	19k	50k		DYN
33	INNOVATOR	8	I	18/8		S	1	2PM	2	2	DIS	EXT	16				23	1.0u	B	9.6k			EDSI
34	ETC1000	8	B	256/8	64k/8	PS	1	PPrV	1	8			24	4	8	4		1.5u	AB	19k	500k	S121	ETL
35	PIC1650	8	M		4/8	P					S	NA			32			4.0u	A			S114	GIC
36	PIC1655	8	M		3/8	P					S	NA			20			4.0u	A			S114a	GIC
37	PIC1670	8	M		4/8	P					S	NA			32			4.0u	A			S114b	GIC
38#	LP8000	8	M		64/8	P					S	NA	14		4	4		15u	A			S37	GICB
39	HCMP1802	8	B	256/8	64k/8	PS	5	PV	1	1	DIS	CPU	8	6	10	4	12	2.5u	ABC	800k	800k	S42	HAC
40	H8	8	I	256/8	64k/8	PS		MPrV		7	IS	EXT	16		5			4.9u	ABC	9.6k			HEA
41	MLP8080	8	B	256/8	64k/8	PS	32	PrV	8	8	DIS	EXT	16		3		12	4.0u	AB	9.6k		S20	HEU
42	MLZ80	8	B	256/8	65k/8	PS	1	PrV	8	8	DIS	CPU	16				32	3.5u	AB	19k	19k	S153	HEU
43	MCS8	8	B	256/8	16k/8	P		V	1	8	S		8	0	0	0		20u				S41	ITL
44	MCS48	8	B	8/8	256/8	PS	1	PrV	27	1	S		12	2	8	5		2.5u	A			S65	ITL
45	MCS80	8	B	256/8	64k/8	P		V	1	8	S	EXT	8	0	0	5		2.0u				S12	ITL
46	MCS85	8	B	256/8	64k/8	PS	1	PrV	5	16	IS	EXT	8	2	3	5		1.3u	A			S64	ITL
47	UPI41	8	I	2/8		P		V	2	1	S	NA						5.0u	A			S97	ITL
48	MICRO1	8	I	32/8				PrV		4	DIS	EXT	24	12	9	4		8.0u	AB	9.6k	50k		MID
49	F8-MOS	8	B	512/8	65k/8	PS		VPPr	1	U	DIS	EXT	16		8			2.0u	AB	9.6k	50k	S15	MOS
50	M6800	8	M		65k/8	PS	8	PPr	2	2	DIS	EXT	16	2	2	4	3	2.0u*	AB	500k	600k	S7	MOTA
51	MSC8001-Z80	8	B	256/8	64k/8	PS		PPrV		U	DIS	EXT	16			6		2.0u	ABC	600k	600k	S96	MSCC
52	MS808A	8	I	256/8		PS	8	PPrV	1	16	IS	EXT	8		2			5.0u	AB	9.6k	9.6k		MUL
53	muPRO80	8	I	256/8		PS		8Pr		8		EXT	16						ABC	9.6k	9.6k		MUP
54#	NASCOMI	8	B	256/8	64k/8	PS	1	PrV	1	U	DIS	EXT	16		6	2		5.5u	ABC	9.6k		S140	NASB
55	uCOM-8	8	B	512/8	64k/8	P		V	1		IS	EXT	16		9	6		2.0u	A				NECJ
56#	uCOM-80F	8	B	512/8	64k	P		V	1		S	EXT	16		9	5		2.0u	A				NECJ
57	NMS85/P	8	B	256/8	256/8	PS		PPrV	12	12	DIS	EXT	18	1	1			1.3u	AB	9.6k			NMS
58	SC/MP	8	M		64k/8	S	3		1	1	DIS	CPU	16	2	6	3		10u	A			S132	NSC
59	EQUINOX-100	8	I	256/8		PS	8	V	1	8	S	EXT	16					5.0u	AB	4.8k			PAR
60	MICROPAC80A	8	M		256/16	PS		P	1		IS	NA	16	8	12	8		2.5u	ABC	640k			PCS
61	PCS1806	8	M		256/8	PS		PPrV	2	8	IS	NA	16		10			2.0u	AC	9.6k		S67	PCS
62	PCS1810	8	M		256/8	PS		PPrV	2	8	IS	NA	16		10			2.0u	ABC	9.6k		S68	PCS
63	SUPERPAC180	8	M		256/8	PS		PPrV	2	8	IS	NA	16		10			2.0u	ABC	9.6k			PCS
64	PLS-858	8	I	16/8	S168	PS	1	Pr	1	5	IS	NA		5	4			320nF	A		55k		PRO
65	PLS-868	8	I	16/8		P		V	1	3	IS	NA		3	4			1.0uF	A		55k	S169	PRO
66	PLS-881	8	I	5/8		P		Pr	1	1	IS	NA		2	4			488nF	A		55k	S76	PRO
67	PLS-888	8	I	16/8		P		Pr	1	1	IS	NA		2	5			488nF	A		55k	S170	PRO
68	PLS-898	8	I	16/8		PS		Pr	1	2	IS	NA		3	2			400nF	A		70k	S156a	PRO
69	QUAY90MPS	8	I	512/8		PS		PV	1	128	IS	CPU	16					4.0u	AB	9.6M			QUY
70	CDP1800	8	I	8/8		PS	8	PrV	1		DIS	CPU	8	6	4	4	13	2.5u*	ABC	800k§	400k	S42	RCA
71	CMC68/15	8	M		4/8	PS	5	PPrV	8	8	IS	EXT	16	8	4	4	17	4.0u	ABC	19k	19k	S141	RCI
72	CMC68/15C	8	M		2/8	PS	5	PPrV	8	8	IS	EXT	16	4	2	2	23	4.0u	AB	19k	19k		RCI
73	CMC68/15G	8	M		4/8	PS	5	PPrV	8	8	IS	EXT	16	4	2	2	23	1.0u§		19k	19k	S174	RCI
74	AIM65	8	M	28/1	65k/16	PS	8	PrV	3	3	DIS	EXT	16	2	4	7		6.0u	AC			S135	RKW
75#	MICRAL-M	8	B	2816/8	512k/8	PS	8	Pr	8	64	IS	NA	8		8			2.0u	ABC	9.6k	9.6k		R2E
76#	MICRAL-S	8	B	352/8	64k/8	PS	8	Pr	8	8	IS	NA	8		8			2.0u	ABC	9.6k	9.6k		R2E
77	2650	8	I	256/8		PS	1	V	1	1	IS	EXT	15	1	11	1		4.8u	A			S3	SIC
78	MIKUL600	8	M		64k/8	P		PPrV	2		DIS	EXT	16		15	6		3.0u	ABD	9.6k			TLI
79	MIKUL6000	8	M		64k/8	PS	8	PPr	2	2	DIS	EXT	16	2	2	4	3	2.0u*	AB	500k	600k	S7	TLI
80	VECTOR1PLUS	8	B	512/8	65k/8	PS	5	PrV	8	8	IS	NA	16		2				ABC	9.6k	56k		VGI
81	uPSeries	8	I	128/8		PS		PrV	8	8	DIS	EXT	16		14			5.0u	ABC	38k	38k	S30	WLD
82	CM6800	8	M		65k/8	PS	10	PPrV	1		IS	NA	16		3	6		5.0u	AB	500k	9.6k		WTK
83	MCZ	8	I	128/8	64k/8	PS	8	PPrV	1		IS	NA	16		13	8		4.4u	AB	38k			ZIL
84	PDS	8	I	128/8	64k/8	PS	8	PPrV	1	M	IS	NA	16		13	8		4.4u	AB	38k			ZIL
85	HB61000	12	I	64/12		PS	8	PrV			DIS							2.5u*	ABC	9.6k		S146	HAS
86	HM6100	12	I	64/12		PS	8	PrV			DIS	EXT	12	4		4		2.5u*	ABC			S62	HAS
87	IM6100	12	I	64/12		PS	8	PrV			DIS	EXT	12	4		4		2.5u*				S62	INL
88	PCM-12A	12	I	63/12		PS	8	PPrV	1		DIS	CPU		12	12			8.5u	ABC	9.6k			PCM
89	S9900	16	I	256/12		PS	16	V	1		DIS	EXT	12					12u	A			S5	AMI
90	MICRONOVA	16	I	64/16		PS	16	Pr	1	16	DIS	CPU	15		2			4.8u	AB	19k	56k	S59	DGC
91	GA16/110	16	I	64/16				PrV	64	3	IS	NA	6	2	2	2		2.5u	AB	9.6k	2.5M	S49	GEN
92	GA16/220	16	I	64/16				PrV	64	3	DIS	CPU	6	2	2	2		2.5u	AB	9.6k	2.5M	S50	GEN
93	GIMINI	16	M		65k/16			PrV	2		DIS	EXT	16	16	16	16		4.0u		9.6k	9.6k	S55	GIC
94	H11	16	M		8000/16	PS		PrV		1	DIS	EXT	16		17			11uF	ABC	9.6k			HEA
95	IMP16	16	B	64k/16	64k/16	PS	4	PPrV	2	2	IS	EXT	16	4	4	16		10u	A			S35	NSC
96	IPC16C	16	M		64k/16	S	3	PPrV	6	6	IS	EXT	16	3	3	16		9.5u	A			S32	NSC
97#	LKIT16	16	I	8/16		P		Pr	3	3	DIS	EXT	8	3	3	32		4.0u	A				PAFJ
98#	PFL16A	16	I	256/16		P		Pr	3	3	DIS	EXT	8	3	3	32		3.5u	ABC	1.2k	9.6k	S23	PAFJ
99	MIPROC16	16	I	256/16		PS	8	PPrV	8	256	DIS	EXT	8		2			350n	AB	19k		S24	PLM
100	990/4	16	B	4k/1	32k/16	PS		PrV	4	16	DIS	EXT	15		7			4.0u				S5	TII
101	TMS9940	16	I	256/1		PS		PrV	2	4	IS	NA	8		7	32		4.0u				S81	TII

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

10. MICROPROCESSORS

IN ORDER OF: (1)DATA BITS (2)ARCHITECTURE (3)No. BASIC INSTRUCTIONS & (4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZ. 1 DATA BITS	ORGANIZ. 2 ARCHI-TECT-URE	TECH NOL.	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RAM/ROM %BIT CONFIG MIXED ▼-bits (BYTES)	MAX. CLOCK FREQ. (Hz)	No Øs	OPER. VOLTAGES V1 (V)	V2 (V)	V3 (V)	MAX. OPER. PWR. DISS. (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	3 No. BASIC INSTR	A D R	M O D E	DRAWINGS CPU INTERNAL ARCHIT ECTURE	DRAWINGS OUTLINE Δ=MO	MFR. CODE
1	uPD557LC		Chip		0.0	-35	96/2k	180k		-8.0			288m	10	70					DL67	NECM
2	MC14500BAL	1	Chip	MCX	11	4.0	512	1.0M	1	15				55	125	16			C73	DL76	MOTA
3	MC14500BCL	1	Chip	MCX	11	4.0	512	1.0M	1	15				40	85	16			C73	DL76	MOTA
4	MC14500BCP	1	Chip	MCX	11	4.0	512	1.0M	1	15				40	85	16			C73	DL53	MOTA
5▼#	HD44770	4	uCT	MNX			88/2k			5.0											HITJ
6▼#	HD44780	4	uCT	MNX			128/2k			5.0											HITJ
7▼#	HD44790	4	uCT	MNX						5.0											HITJ
8	WD4020A	4	uCT	MNG	2.0	.80	256▼%			5.0				0	70				C137	DL160	WDC
9	WD4020B	4	uCT	MNG	2.0	.80	256▼%			5.0				0	70				C137	DL161	WDC
10	WD4200E	4	uCT	MNG	2.0	.80§	256/8k▼%	4.0M		5.0			750m☑	0	70				C136	DL162	WDC
11	WD4200F	4	uCT	MNG	2.0	.80§	256/8k▼%	4.0M		5.0			750m☑	0	70				C136	DL163	WDC
12	WD4210E	4	uCT	MNG	2.0	.80§	256/8k▼%	4.0M		5.0			750m☑	0	70				C136a	DL☑	WDC
13	WD4210F	4	uCT	MNG	2.0	.80§	256/8k▼%	4.0M		5.0			750m☑	0	70				C136a	DL☑	WDC
14	CR1872	4	uCT	MPG	3.5	.80	128/512%	150k	1	5.0	-8.0		200m	0	70	20			C91	DL☑	WDC
15	MM57140N	4	uCT	MPX	-4.0	-6.2	220Ø/5kØ▼	280k	1	-9.0			135m	0	70	36			C95	DL67c	NSC
16	MM5799N	4	uCT	MPX	-1.0	-4.0	384Ø/12kØ▼	450k	1	-9.0			162m	0	70	41			C96	DL67c	NSC
17	MC141000L	4	uCT	MCX	3.5	1.5	256Ø/8kØ▼	600k	1	5.0			11m	40	85	43			C125	DL☑	MOTA
18	MC141000P	4	uCT	MCX	3.5	1.5	256Ø/8kØ▼	600k	1	5.0			11m	40	85	43			C125	DL☑	MOTA
19	MC141099L	4	uCT	MCX	2.0	.80	256Ø/8kØ▼	600k	1	5.0			11m	40	85	43			C125b	DL☑	MOTA
20	MC141099P	4	uCT	MCX	2.0	.80	256Ø/8kØ▼	600k	1	5.0			11m	40	85	43			C125b	DL☑	MOTA
21	MC141200L	4	uCT	MCX	3.5	1.5	256Ø/8kØ▼	600k	1	5.0			11m	40	85	43			C125a	DL1d	MOTA
22	MC141200P	4	uCT	MCX	3.5	1.5	256Ø/8kØ▼	600k	1	5.0			11m	40	85	43			C125a	DL27	MOTA
23	TMS1000	4	uCT	MPX	-1.3	-4.0	256Ø/8kØ	400k	2	-15			400m☑	0	70	43			C7	DL24	TII
24	TMS1070	4	uCT	MPX	-6.0	-8.0	256Ø/8kØ	400k	1	-15			400m☑	0	70	43			C9	DL24	TII
25	TMS1200	4	uCT	MPX	-1.3	-4.0	256Ø/8kØ	400k	1	-15			600m☑	0	70	43			C7a	DL11	TII
26	TMS1270	4	uCT	MPX	-6.0	-8.0	256Ø/8kØ	400k	1	-15			600m☑	0	70	43			C10	DL11	TII
27#	MN1404	4	uCT	MNG	2.4	.80	64Ø/4kØ▼	300k	2	5.0			140m	30	70	48	2		C145d		MATJ
28#	MN1454	4	uCT	MCX			256/4k▼									48					MATJ
29	MM75	4	uCT	MPX	3.5	.80	48/640%	80k	4	5.0	-15		125m	0	70	50			C106	DL☑	RKW
30	MM76EL	4	uCT	MPX	3.5	.80	48/1024%	80k	4	5.0	-8.5		25m	0	70	50			C129	DL☑	RKW
31	MM78	4	uCT	MPX	3.5	.80	128/2.0k%	80k	4	5.0	-15		125m	0	70	50			C108	DL☑	RKW
32	MM78L	4	uCT	MPX	3.5	.80	128/2.0k%	100k	4	5.0	-8.5		15m†	0	70	50			C131	DL☑	RKW
33#	MN1403	4	uCT	MNX	2.4	.80	64/4k▼			5.0			140m	30	70	50	2		C145a	DL20c	MATJ
34#	HMCS42	4	uCT	MPX	3.7	2.7	32Ø/544Ø%				-10		100m†	20	75	51				DL☑	HITJ
35#	HMCS42C	4	uCT	MCX	2.4	.80%	32Ø/544Ø%			5.0			1.5m†	20	75	51					HITJ
36	S2000	4	uCT	MNG	3.5	.80	64/1.0kØ%	850k	1	9.0			700m☑	0	70	51			C84	DL42g	AMI
37	S2000A	4	uCT	MNG	3.5	.80	64/1.0kØ%	850k	1	9.0			700m☑	0	70	51			C84	DL42g	AMI
38	S2150	4	uCT	MNG	3.5	.80	80/1.5kØ%	850k	1	9.0			700m☑	0	70	51			C84	DL42g	AMI
39	S2150A	4	uCT	MNG	3.5	.80	80/1.5kØ%	850k	1	9.0			700m☑	0	70	51			C84	DL42g	AMI
40	TMS1100	4	uCT	MPX	-1.3	-4.0	512Ø/16kØ	400k	1	-15			400m☑	0	70	54			C8	DL24	TII
41	TMS1300	4	uCT	MPX	-1.3	-4.0	512Ø/16kØ	400k	1	-15			600m☑	0	70	54			C8a	DL11	TII
42#	MN1402	4	uCT	MNG	2.4	.80	128Ø/6kØ▼	300k	2	5.0			180m	30	70	57	2		C145c	DL67a	MATJ
43#	MN1432	4	uCT	MPX	-4.0	-10	128/8k▼			-15			420m	30	70	58	2		C145c	DL67a	MATJ
44#	uPD547C	4	uCT	MPX	0.0	-10	64Ø/1kØ	440k	1	-10			500m	10	70	58			C88	DL59	NECJ
45#	uPD547LC	4	uCT	MPX	0.0	-10	64Ø/1kØ	180k	1	-8.0			500m	10	70	58			C88	DL59	NECJ
46#	uPD550C	4	uCT	MPX	0.0	-10	32Ø/640Ø	400k	1	-10				10	70	58			C86	DL67	NECJ
47#	uPD554C	4	uCT	MPX	0.0	-10	32Ø/1kØ	400k	1	-10				10	70	58			C86a	DL67	NECJ
48	S2400	4	uCT	MNG	3.5	.80	128/4kØ%	850k	1	9.0			700m☑	0	70	59			C140	DL42g	AMI
49	S2400A	4	uCT	MNG	3.5	.80	128/4kØ%	850k	1	9.0			700m☑	0	70	59			C140	DL42g	AMI
50#	MN1498	4	uCT	MNG	2.4	.80	256Ø/0▼	300k	2	5.0			250m	30	70	68	2		C145b	DL11j	MATJ
51#	HMCS43	4	uCT	MPX	3.7	2.7	80Ø/1kØ%				-10		200m†	20	75	71				DL☑	HITJ
52#	HMCS43C	4	uCT	MCX	2.4	.80%	80Ø/1kØ%			5.0			2.0m†	20	75	71				DL☑	HITJ
53#	HMCS44A	4	uCT	MPX	3.7	2.7	160Ø/2kØ%				-10		300m†	20	75	71				DL☑	HITJ
54#	HMCS44C	4	uCT	MCX	2.4	.80%	160Ø/2kØ%			5.0			2.0m†	20	75	71				DL☑	HITJ
55#	HMCS45A	4	uCT	MPX	3.7	2.7	160Ø/2kØ%				-10		300m†	20	75	71			C128	FP☑	HITJ
56#	HMCS45C	4	uCT	MCX	2.4	.80%	160Ø/2kØ%			5.0			2.0m†	20	75	71				FP☑	HITJ
57#	uPD545C	4	uCT	MPX			96Ø/1.9kØ%	100k	1		-10					72			C80	DL☑	NECD
58#	MN1400	4	uCT	MNG	2.4	.80	256Ø/8kØ▼	300k	2	5.0			200m	30	70	75	2		C145	DL11j	MATJ
59#	MN1405	4	uCT	MNG	2.4	.80	512Ø/16kØ▼	300k	2	5.0			250m	30	70	75	2				MATJ
60#	MN1430	4	uCT	MPG	-6.0	-12	256Ø/8kØ▼	210k	2	-15			450m	30	70	75	2		C145		MATJ
61#	MN1435	4	uCT	MPX	-4.0	-10	512/16k▼			-15			600m	30	70	75	2		C145	DL11j	MATJ
62#	MN1450	4	uCT	MCX	2.4	.80	256/8k▼			5.0				30	70	75	2			DL11j	MATJ
63#	MN1453	4	uCT	MCX	2.4	.80	256/4k▼			5.0				30	70	75			C145a	DL20c	MATJ
64#	MN1455	4	uCT	MCX			512/16k▼									75					MATJ
65#	MN1499	4	uCT	MNG	2.4	.80	256Ø/0▼	300k	2	5.0			250m	30	70	75	2		C145e	DL15a	MATJ
66#	MN1499A	4	uCT	MNG	2.4	.80	512Ø/0▼	300k	2	5.0			250m	30	70	75			C145e	DL15a	MATJ
67#	uPD546C	4	uCT	MPX	-4.3	-2.0	96Ø/2kØ%	440k			-10		500m	10	70	80			C79	DL59	NECJ
68#	uPD550LC	4	uCT	MPX	0.0	-10	8k▼	400k	1	-10				10	70	96			C86	DL67	NECJ
69#	uPD554LC	4	uCT	MPX	0.0	-10	8k▼	400k	1	-10				10	70	96			C86a	DL67	NECJ
70#	uPD650C	4	uCT	MCX	3.5	1.5	16k▼	440k		5.0			10m	30	85	96				DL59	NECJ
71#	uPD652C	4	uCT	MCX	3.5	1.5	8k▼	440k		5.0			10m	30	85	96				DL67	NECJ
72#	uPD766G	4	uCT	MNX			32Ø/4kØ		1	5.0						103			C85	FP11	NECJ
73▼	Am29203DC	4	Chip	BTO	2.0	.80	16/32%			5.0				0	70				C101		AMD
74▼	Am29203DM	4	Chip	BTO	2.0	.30	16/32%			5.0				55	125				C101		AMD
75	IDM2903ADC	4	Chip	BED	2.0	0.8	64/0▼			5.0			172m	0	70				C101		NSC
76	IDM2903ADM	4	Chip	BED	2.0	0.8	64/0▼			5.0			195m	55	125				C101		NSC
77	MC2903LC	4	Chip	BTX	2.0	.80				5.0				0	70				C114	DL☑	MOTA
78	MC2903LM	4	Chip	BTX	2.0	.80				5.0				55	125				C114	DL☑	MOTA
79#	uPD541C	4	Chip	MPX	2.3	.75				5.0	-5.0		525m	10	70				C56	DL59	NECJ
80	uPD651G	4	Chip	MCX	.70	.30	64/1k	440k		5.0			10m	30	85					FP23	NECM
81	uPD7520	4	Chip	MPX			48/768	300k		-6.0	-10		30m	10	70				C164		NECM
82	IDM2901A-1DM/883	4	Chip	BED	2.0	0.8	64/0▼	16M	1	5.0			138m	55	125	8	1		C36		NSC
83	IDM2901A-2DC	4	Chip	BED	2.0	0.8	64/0▼	20M	1	5.0			130m	0	70	8	1		C36		NSC
84	IDM2901A-2DM	4	Chip	BED	2.0	0.8	64/0▼	16M	1	5.0			138m	55	125	8	1		C36		NSC
85	IDM2901A-2DM/883	4	Chip	BED	2.0	0.8	64/0▼	16M	1	5.0			138m	55	125	8	1		C36		NSC
86	IDM2901A-2NC	4	Chip	BED	2.0	0.8	64/0▼	20M	1	5.0			130m	0	70	8	1		C36		NSC
87	IDM2901ADM/883	4	Chip	BED	2.0	0.8	6410▼	16M	1	5.0			138m	55	125	8	1		C36		NSC
88	IDM2901ANC	4	Chip	BED	2.0	0.8	64/0▼	16M	1	5.0			130m	0	70	8	1		C36		NSC
89	MC10800	4	Chip	BEX	-.96	-1.6%	256/256	100M	2	-5.2	-2.0		1.6	30	85	16			C46	DL55	MOTA
90	MC10800M	4	Chip	BEX	-.93	-1.6%	256/256	100M	2	-5.2	-2.0		1.6	55	150	16			C46	DL55	MOTA
91	MC2901LC	4	Chip	BTD	2.0	.80§	512/8k	9.5M	1	5.0			1.4	0	70	23	4		C36	DL1h	MOTA
92	2901AFM#1	4	Chip	BTD	2.0	.80§	256/256	12M	1	5.0			1.4	55	125	24Δ	4		C36a	FP12	MMI
93	2901AJC	4	Chip	BTD	2.0	.80§	256/256	15M	1	5.0			1.2	0	70	24Δ	4		C36	DL11h	MMI
94	2901AJM	4	Chip	BTD	2.0	.80§	256/256	12M	1	5.0			1.4	55	125	24Δ	4		C36	DL11h	MMI
95	2901ANC	4	Chip	BTD	2.0	.80§	256/256	15M	1	5.0			1.2	0	70	24Δ	4		C36	DL11g	MMI
96	MMI5701	4	Chip	BTD	2.0	.80	4.0k	4.3M	1	5.0			1.4	55	125	36			C20	DL1c	MMI
97	MMI6701	4	Chip	BTD			4.0k	5.7M	1	5.0			1.4	0	75	36			C20	DL1c	MMI
98	MM5782N	4	Chip	MPX	-1.0	-6.5	640Ø/16k▼	400k	1	-9.0			225m	0	70	42			C97	DL67c	NSC
99	PPS4/1	4	Chip	MPX	3.5	-12	96/1.3k	199k	4	5.0	-12		375m	0	70	50			C27	DL44	RKW
100#	TFK10660	4	Chip	MPX	3.5	-12	256/1k	199k	4	5.0	-12		375m	0	70	50			C26		ALGG
101#	TFK11660	4	Chip	MPX	3.5	-12	128/2k	199k	4	5.0	-12			0	70	50			C27		ALGG
102	uPD551C	4	Chip	MPX	0.0	-10	256/8000▼Ø	440k	1	-10			400m	10	70	58			C142	DL101	NECM
103	C4040	4	Chip	MPG	3.5	.80	256/256%	740k	2	5.0	-10		900m	0	70	60			C19	DL3a	ITL
104	P4040	4	Chip	MPG	3.5	.80	256/256%	740k	2	5.0	-10		900m	0	70	60			C19	DL14a	ITL
105	9405ADC	4	Chip	BIX	2.0	.70	16/16	13M	1	5.0			800m	0	75	64Δ			C100	DL7g	FSC
106	9405ADM	4	Chip	BIX	2.0	.70	16/16	13M	1	5.0			800m	55	125	64Δ			C100	DL7g	FSC
107	9405APC	4	Chip	BIX	2.0	.70	16/16	13M	1	5.0			800m	0	75	64Δ			C100	DL18d	FSC
108#	M58840-XXXP	4	Chip	MPX	1.4	4.2	128/2k	600k	1	15			700m	0	70	68	1		C160	DL218	MITJ

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

10. MICROPROCESSORS

IN ORDER OF: (1)DATA BITS (2)ARCHITECTURE (3)No. BASIC INSTRUCTIONS & (4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZ. 1 DATA BITS	ORGANIZ. 2 ARCHI-TECT-URE	TECH NOL.	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RAM/ROM %BIT CONFIG MIXED ▼-bits (BYTES)	MAX. CLOCK FREQ. (Hz)	No Øs	OPER. VOLTAGES V1 (V)	V2 (V)	V3 (V)	MAX. OPER. PWR. DISS. (W)	OPERATING 3 TEMP. (-)	TEMP. (+)	No. BASIC INSTR	A M D O D R E	DRAWINGS CPU INTERNAL ARCHIT-ECTURE	DRAWINGS OUTLINE Δ=MO	MFR. CODE
1	SBP0400ACJ	4	Chip	BIX	2.0	.80	256/512%	5.0M	1	5.0			1.0	0	70	76		C47	DL1a	TII
2	SBP0400ACN	4	Chip	BIX	2.0	.80	256/512%	5.0M	1	5.0			1.0	0	70	76		C47	DL11	TII
3	SBP0400AMJ	4	Chip	BIX	2.0	.80	256/512%	5.0M	1	5.0			1.0	55	125	76		C47	DL1a	TII
4	SBP0400C	4	Chip	BIX	2.0	.80	256/512%	1.0M	1	5.0			1.0	0	70	76		C47	DL11	TII
5	SBP0400M	4	Chip	BIX	2.0	.80	256/512%	1.0M	1	5.0			1.0	55	125	76		C47	DL11	TII
6	SBP0401ACJ	4	Chip	BIX	2.0	.80	256/512%	5.0M	1	5.0			1.5	0	70	76		C47	DL1a	TII
7	SBP0401ACN	4	Chip	BIX	2.0	.80	256/512%	5.0M	1	5.0			1.5	0	70	76		C47	DL11	TII
8	SBP0401AMJ	4	Chip	BIX	2.0	.80	256/512%	5.0M	1	5.0			1.5	55	125	76		C47	DL1a	TII
9	uPD552C	4	Chip	MPX	0.0	-10	256/8000▼Ø	440k	1	-10			500m	10	70	80			DL59	NECM
10	uPD553C	4	Chip	MPX	0.0	-10	384/8000▼Ø	440k	1	-10			500m	10	70	80			DL59	NECM
11#	uPD8085AD	4	Chip	MNX	2.0	.80		3.0M	1	5.0						80	4	C87	DL☑	NECJ
12#	M58494-XXXP	4	Chip	MCX			32/4k	455k	1	5.0			5.0m			92	1	C161	FL22	MITJ
13#	uPB2901AD	4	Chip	BTD	2.0	.80		16M		5.0			1.5	0	70	96			DL100	NECJ
14#	uPD651C	4	Chip	MCX	.70	.30	64/1k	440k		5.0			10m	30	85	96			DL59	NECM
15	SN54LS481J	4	Chip	BTD	2.0	.80	256/256	10M	1	5.0			1.0	55	125	210Δ		C61	DL71	TII
16	SN54S481	4	Chip	BTD	2.0	.80	256/256	9.0M	1	5.0			2.1	55	125	210Δ		C61	DL92	TII
17	SN74LS481J	4	Chip	BTD	2.0	.80	256/256	10M	1	5.0			1.0	0	70	210Δ		C61	DL71	TII
18	SN74LS481N	4	Chip	BTD	2.0	.80	256/256	10M	1	5.0			1.0	0	70	210Δ		C61	DL92	TII
19	SN74S481J	4	Chip	BTD	2.0	.80	256/256	10M	1	5.0			1.6	0	70	210Δ		C61	DL92	TII
20	SN74S481N	4	Chip	BTD	2.0	.80	256/256	10M	1	5.0			1.6	0	70	210Δ		C61	DL92	TII
21	2901ADC	4	Chip	BTD	2.0	.80§	256/256	25M	1	5.0			2.4	0	70	512Δ	4	C36	DL11g	RTN
22	2901ADM	4	Chip	BTD	2.0	.70§	256/256	15M	1	5.0			2.4	55	125	512Δ	4	C36	DL11g	RTN
23	2901AFM	4	Chip	BTD	2.0	.70§	256/256	15M	1	5.0			2.4	55	125	512Δ	4	C36	FP4	RTN
24	2901APC	4	Chip	BTD	2.0	.80§	256/256	25M	1	5.0			2.4	0	70	512Δ	4	C36	DL11h	RTN
25	9409DC	4	Chip	BTD	2.0	.80§		15M	1	5.0			1.2	0	70	512Δ		C36	DL37c	FSC
26	9409DM	4	Chip	BTD	2.0	.80§		12M	1	5.0			1.4	55	125	512Δ		C36	DL37c	FSC
27	9409PC	4	Chip	BTD	2.0	.80§		15M	1	5.0			1.2	0	70	512Δ		C36	DL11m	FSC
28	Am2901ADC	4	Chip	BTD	2.0	.80§	256/256	15M	1	5.0			1.3	0	70	512Δ	4	C36	DL1h	AMV
29	Am2901ADM	4	Chip	BTD	2.0	.80§	256/256	12M	1	5.0			1.4	55	125	512Δ	4	C36	DL1h	AMV
30	Am2901AFM	4	Chip	BTD	2.0	.80§	256/256	12M	1	5.0			1.4	55	125	512Δ	4	C36	FP4	AMV
31	Am2901APC	4	Chip	BTD	2.0	.80§	256/256	15M	1	5.0			1.3	0	70	512Δ	4	C36		AMV
32	Am2901AXC	4	Chip	BTD	2.0	.80§	256/256	15M	1	5.0			1.2	0	70	512Δ	4	C36	CH1	AMV
33▼	Am2901BDC	4	Chip	BTO	2.0	.80	256/256	16M	1	5.0				0	70	512Δ	4	C36	DL1h	AMD
34▼	Am2901BDM	4	Chip	BTO	2.0	.80	256/256	15M	1	5.0				55	125	512Δ	4	C36	DL1h	AMD
35▼	Am2901BFM	4	Chip	BTO	2.0	.80	256/256	15M	1	5.0				55	125	512Δ	4	C36a	FP4	AMD
36▼	Am2901BPC	4	Chip	BTO	2.0	.80	256/256	16M	1	5.0				0	70	512Δ	4	C36	DL112a	AMD
37▼	Am2901CDC	4	Chip	BTO	2.0	.80	256/256			5.0				0	70	512Δ	4	C36	DL1h	AMD
38▼	Am2901CDM	4	Chip	BTO	2.0	.80	256/256			5.0				55	125	512Δ	4	C36	DL1h	AMD
39▼	Am2901CFM	4	Chip	BTO	2.0	.80	256/256			5.0				55	125	512Δ	4	C36a	FP4	AMD
40▼	Am2901CPC	4	Chip	BTO	2.0	.80	256/256			5.0				0	70	512Δ	4	C36	DL112a	AMD
41	Am2901DC	4	Chip	BTD	2.0	.80§	256/256	9.5M	1	5.0			1.4	0	70	512Δ	4	C36	DL1h	AMV
42	Am2901DM	4	Chip	BTD	2.0	.70§	256/256	8.3M	1	5.0			1.4	55	125	512Δ	4	C36	DL1h	AMV
43	Am2901FM	4	Chip	BTD	2.0	.70§	256/256	8.3M	1	5.0			1.4	55	125	512Δ	4	C36	FP4	AMV
44	Am2901PC	4	Chip	BTD	2.0	.80§	256/256	9.5M	1	5.0			1.4	0	70	512Δ	4	C36		AMV
45	Am2903DC	4	Chip	BTD	2.0	.80	16/32%	12M	1	5.0			1.8	0	70	512Δ		C101	DL☑	AMV
46	Am2903DM	4	Chip	BTD	2.0	.80	16/32%	12M	1	5.0			2.0	55	125	512Δ		C101	DL☑	AMV
47	Am2903FM	4	Chip	BTD	2.0	.80	16/32%	12M	1	5.0			1.8	55	125	512		C101	FP☑	AMV
48▼	Am29203FM	4	Chip	BTD	2.0	.30	16/32%			5.0				55	125	512Δ		C101		AMD
49	F2901ADC	4	Chip	BTD	2.0	.80§		15M	1	5.0			1.2	0	70	512Δ		C36	DL37c	FSC
50	F2901ADM	4	Chip	BTD	2.0	.80§		12M	1	5.0			1.4	55	125	512Δ		C36	DL37c	FSC
51	F2901APC	4	Chip	BTD	2.0	.80§		15M	1	5.0			1.2	0	70	512Δ		C36	DL11m	FSC
52	IDM2901A-1DC	4	Chip	BED	2.0	.80§	16/32%	16M	1	5.0			1.3	0	70	512Δ		C36	DL37d	NSC
53	IDM2901A-1DM	4	Chip	BED	2.0	.80§	16/32%	16M	1	5.0			1.4	55	125	512Δ		C36	DL37d	NSC
54	IDM2901A-1NC	4	Chip	BED	2.0	.80§	16/32%	16M	1	5.0			1.3	0	70	512Δ		C36	DL11f	NSC
55	IDM2901ADC	4	Chip	BED	2.0	.80§	16/32%	16M	1	5.0			1.3	0	70	512Δ		C36	DL37d	NSC
56	IDM2901ADM	4	Chip	BED	2.0	.80§	16/32%	15M	1	5.0			1.4	55	125	512Δ		C36	DL37d	NSC
57	IDM2901AFM	4	Chip	BED	2.0	.80§	16/32%	15M	1	5.0			1.4	55	125	512Δ		C36a	FP12	NSC
58	IDM2901APC	4	Chip	BED	2.0	.80§	16/32%	16M	1	5.0			1.3	0	70	512Δ		C36	DL☑	NSC
59	MC2901AFM	4	Chip	BTX	2.0	.80	256/256	12M	1	5.0			1.4	55	125	512Δ	4	C36a	FP13	MOTA
60	MC2901ALC	4	Chip	BTX	2.0	.80	256/256	15M	1	5.0			1.3	0	70	512Δ	4	C36	DL112	MOTA
61	MC2901ALM	4	Chip	BTX	2.0	.80	256/256	12M	1	5.0			1.4	55	125	512Δ	4	C36	DL112	MOTA
62	MC2901LM	4	Chip	BTD	2.0	.70§	512/8k	8.3M	1	5.0			1.4	55	125	512Δ	4	C36	DL1h	MOTA
63	N2901-1I	4	Chip	BTD	2.0	.80	16/32%	25M	1	5.0			1.3	0	70	512Δ		C36	DL1b	SIC
64	C3001,2	4	ChS	BTD	2.0	.80§	256/256%	14M	1	5.0			2.1	0	70	512Δ	5	C4	DL12a	ITL
65	D3001,2	4	ChS	BTD	2.0	.80§	256/256%	14M	1	5.0			2.1	0	70	512Δ	5	C4	DL29	ITL
66	MC3001,2	4	ChS	BTD	2.0	.80§	256/256%	14M	1	5.0			2.3	55	125	512Δ	5	C4	DL29	ITL
67	N3001,2	4	ChS	BTD	2.0	.80§	16/32%	14M	1	5.0			2.1	0	70	512Δ	5	C4	DL12	SIC
68	S3001,2	4	ChS	BTD	2.0	.80§	16/32%	14M	1	5.0			2.1	0	70	512Δ	5	C4	DL12	SIC
69▼	TMS1000C	4	CHIP	MNX	4.0	1.0	64/1k	1.0M		5.0			200m	0	70	16			DL24	TII
70▼	TMS1200C	4	CHIP	MNX	4.0	1.0	64/1k	1.0M		5.0			200m	0	70	16			DL11	TII
71▼	TMS1097JLL	4	CHIP	MPX	-2.4	-.50	128/4k	3.3uΔ		-15			600m	0	70	54				TII
72▼	TMS1400NLL	4	CHIP	MPX	-2.4	-.50	128/4k	3.3uΔ		-15			600m	0	70	54			DL24	TII
73▼	TMS1470NLL	4	CHIP	MPX	-2.4	-.50	128/4k	3.3uΔ		-15			600m	0	70	54			DL24	TII
74▼	TMS1600NLL	4	CHIP	MPX	-2.4	-.50	128/4k	3.3uΔ		-15			600m	0	70	54			DL11	TII
75▼	TMS1670NLL	4	CHIP	MPX	-2.4	-.50	128/4k	3.3uΔ		-15			600m	0	70	54			DL11	TII
76	MC6803EL	8	uCT	MNG			128	3.58M	2	5.0							7	C113	DL1d	MOTA
77	MC6803EP	8	uCT	MNG			128	3.58M	2	5.0							7	C113	DL27	MOTA
78	MC6803L	8	uCT	MNG			128	3.58M	2	5.0							7	C113	DL1d	MOTA
79	MC6803P	8	uCT	MNG			128	3.58M	2	5.0							7	C113	DL27	MOTA
80#	TMP8035P	8	uCT	MNG	2.0	0.8	64k/1k▼	400k	1	5.0			1.5 ☑	0	70			C155	DL208	TOSJ
81#	TMP8039P	8	uCT	MNG	2.0	0.8	128K/2K▼	1.36uΔ		5.0			1.5 ☑	0	70			C155	DL208	TOSJ
82#	TMP8039P-6	8	uCT	MNG	2.0	0.8	128K/2K▼	2.7uΔ		5.0			1.5 ☑	0	70			C155	DL208	TOSJ
83#	TMP8048P	8	uCT	MNG	2.0	0.8	64K/1K	400k	1	5.0			1.5 ☑	0	70			C155	DL208	TOSJ
84#	TMP8049P	8	uCT	MNG	2.0	0.8	128K/2K▼	1.36uΔ		5.0			1.5 ☑	0	70			C155	DL208	TOSJ
85#	TMP8049P-6	8	uCT	MNG	2.0	0.8	128K/2K▼	2.7uΔ		5.0			1.5 ☑	0	70			C155	DL208	TOSJ
86	PIC1650	8	uCT	MNI	2.4	.65	32Ø/512Ø%	1.0M	1	5.0			350m	0	70	31	2	C77	DL42e	GIC
87	PIC1655	8	uCT	MNI	2.4	.65	32Ø/512Ø%	1.0M	1	5.0			350m	0	70	31	2		DL36e	GIC
88	PIC1670	8	uCT	MNI	2.4	.65	32Ø/1kØ%	1.0M	1	5.0			350m	0	70	31	2		DL42e	GIC
89	S2152	8	uCT	MNG	3.5	.80	80/1.5kØ%	850k	1	9.0			700m	0	70	51		C84	DL42g	AMI
90	S2210	8	uCT	MCG	3.5	.80	64/1.0kØ%	850k	1	9.0			700m	0	70	51		C84	DL42g	AMI
91	SYC6500/1	8	uCT	MNG	2.0	.80	64/2k	1.0M	1	5.0			500m†	0	70	53	13	C126	DL149	SYK
92	SYP6500/1	8	uCT	MNG	2.0	.80	64/2k	1.0M	1	5.0			500m†	0	70	53	13	C126	DL149	SYK
93	R6500/1	8	uCT	MNG	2.4	.40	64Ø/2kØ	4.0M	1	5.0			500m†	0	70	56	13	C132	DL26	RKW
94	MC6805L	8	uCT	MNG	2.0	.80	64Ø/1.1kØ	4.0M	2	5.0				0	70	61	6	C127	DL74	MOTA
95	MC6805P	8	uCT	MNG	2.0	.80	64Ø/1.1kØ	4.0M	2	5.0				0	70	61	6	C127	DL75	MOTA
96#	8021I	8	uCT	MNG	2.0	.80	64/1k	3.0M	1	5.0			330m	0	70	64		C102	DL☑	PHIN
97#	8021N	8	uCT	MNG	2.0	.80	64/1k	3.0M	1	5.0			330m	0	70	64		C102	DL☑	PHIN
98	MK3873	8	uCT		2.0	.80	64/2k	4.0M	1	5.0			400m	0	70	70	4	C139	DL167	MOS
99	MK3874	8	uCT	BTX	2.0	.80	64/2k	4.0M	1	5.0			400m	0	70	70	4	C139	DL167	MOS
100	MK97400	8	uCT	BTX	2.0	.80	64/2k	4.0M	1	5.0			400m	0	70	70	4	C139	DL167	MOS
101	MK97401	8	uCT	BTX	2.0	.80	64/2k	4.0M	1	5.0			400m	0	70	70	4	C139	DL167	MOS
102	MK97402	8	uCT	BTX	2.0	.80	64/2k	4.0M	1	5.0			400m	0	70	70	4	C139	DL167	MOS
103	MK97403	8	uCT	BTX	2.0	.80	64/2k	4.0M	1	5.0			400m	0	70	70	4	C139	DL167	MOS
104	MK97404	8	uCT	BTX	2.0	.80	64/2k	4.0M	1	5.0			400m	0	70	70	4	C139	DL167	MOS
105	MK97405	8	uCT	BTX	2.0	.80	64/2k	4.0M	1	5.0			400m	0	70	70	4	C139	DL167	MOS
106	P8021	8	uCT	MNG	2.0	.80	64Ø/1kØ	4.0M	1	5.0			300m	0	70	70	4	C102	DL35	ITL
107▼	Z8MCUCS	8	uCT		2.0	.80	2k			5.0				0	70	72		C112	DL190	ZIL
108▼	Z8MCUPS	8	uCT		2.0	.80	2k			5.0				0	70	72		C112	DL189	ZIL
109	P8022	8	uCT	MNG	2.0	.80	64Ø/2kØ	4.0M	1	5.0			400m	0	70	74	4	C117	DL42f	ITL
110	F3870DC	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	0	70	76	8	C83	DL37c	FSC

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

10. MICROPROCESSORS

IN ORDER OF: (1)DATA BITS (2)ARCHITECTURE (3)No. BASIC INSTRUCTIONS & (4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZ. 1 DATA BITS	2 ARCHI -TECT -URE	INPUT LOGIC LEVELS TECH NOL.	HIGH (min) (V)	LOW (max) (V)	RAM/ROM %BIT CONFIG MIXED ▼-bits (BYTES)	MAX. CLOCK FREQ. (Hz)	No Øs	OPER. VOLTAGES V1 (V)	V2 (V)	V3 (V)	MAX. OPER. PWR. DISS. (W)	OPERATING TEMP. (-)	(+)	3 No. BASIC INSTR	A D D R	M O D E	DRAWINGS CPU INTERNAL ARCHIT ECTURE	OUTLINE Δ=MO	MFR. CODE
1	F3870DL	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	40	85	76	8		C83	DL37c	FSC
2	F3870DM	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	55	125	76	8		C83	DL37c	FSC
3	F3870PC	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	0	70	76	8		C83	DL11i	FSC
4	F3870PL	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	40	85	76	8		C83	DL11i	FSC
5	F3870PM	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	55	125	76	8		C83	DL11i	FSC
6	F3872DC	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	0	70	76	8		C83	DL37c	FSC
7	F3872DL	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	40	85	76	8		C83	DL37c	FSC
8	F3872DM	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	55	125	76	8		C83	DL37c	FSC
9	F3872PC	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	0	70	76	8		C83	DL11i	FSC
10	F3876DC	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	0	70	76	8		C83	DL37	FSC
11	F3876DL	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	40	85	76	8		C83	DL37	FSC
12	F3876DM	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	55	125	76	8		C83	DL37	FSC
13	F3876PC	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	0	70	76	8		C83	DL11i	FSC
14	F3876PL	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	40	85	76	8		C83	DL11i	FSC
15	F3876PM	8	uCT	MNG	2.0	.80	64/2.0k	4.0M	1	5.0			1.0 ☑	55	125	76	8		C83	DL11i	FSC
16	F3878DC	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	0	70	76	8		C83	DL37c	FSC
17	F3878DL	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	40	85	76	8		C83	DL37c	FSC
18	F3878DM	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	55	125	76	8		C83	DL37c	FSC
19	F3878PC	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	0	70	76	8		C83	DL11i	FSC
20	F3878PL	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	40	85	76	8		C83	DL11i	FSC
21	F3878PM	8	uCT	MNG	2.0	.80	64/4.0k	4.0M	1	5.0			1.0 ☑	55	125	76	8		C83	DL11i	FSC
22	MC3870L	8	uCT	MNG	2.0	.80	64Ø/2kØ	4.0M	1	5.0			275m†	0	70	76	8		C94	DL1d	MOTA
23	MC3870P	8	uCT	MNG	2.0	.80	64Ø/2kØ	4.0M	1	5.0			275m†	0	70	76	8		C94	DL27	MOTA
24	MK3876N/16X	8	uCT	MNG	2.0	.80	128/2k	4.0M	1	5.0			1.5	0	70	76	8		C139b	DL167	MOS
25	MK3876P/16X	8	uCT	MNG	2.0	.80	128/2k	4.0M	1	5.0			1.5	0	70	76	8		C139b	DL167	MOS
26	MK3876P/17X	8	uCT	MNG	2.0	.80	128/2k	4.0M	1	5.5	2.2		1.5	0	70	76	8		C139b	DL167	MOS
27	MKB3870P10	8	uCT	MNG	2.0	.80	64/2k	4.0M	1	5.0			425m	40	85	76	8		C139	DL167	MOS
28	INS8035	8	uCT	MNG	2.0	0.8	64	15.0m		5.0			1.5 ☑	0	70	90			C158	DL216	NSC
29	INS8039	8	uCT	MNG	2.0	0.8	128	15.0m		5.0			1.5 ☑	0	70	90			C158	DL216	NSC
30	INS8040	8	uCT	MNG	2.0	0.8	256	15.0m		5.0			1.5 ☑	0	70	90			C158	DL216	NSC
31	INS8048	8	uCT	MNG	2.0	0.8	64/1.0k	15.0m		5.0			1.5 ☑	0	70	90			C158	DL216	NSC
32	INS8049	8	uCT	MNG	2.0	0.8	128/2k	15.0m		5.0			1.5 ☑	0	70	90			C158	DL216	NSC
33	INS8050	8	uCT	MNG	2.0	0.8	256/4k	15.0m		5.0			1.5 ☑	0	70	90			C158	DL216	NSC
34	C8748-4	8	uCT	MNG	2.0	.80	64Ø/1kØ	6.0M	1	5.0			1.3	0	70	95	5		C146	DL☑	ITL
35	D8035-4	8	uCT	MNG	2.0	.80	64Ø/256	6.0M	1	5.0			1.3	0	70	95	5		C146a	DL☑	ITL
36	P8035-4	8	uCT	MNG	2.0	.80	64/256	6.0M	1	5.0			1.3	0	70	95	5		C146a	DL☑	ITL
37	B8748	8	uCT	MNG	2.0	.80	64Ø/1.0kØ	6.0M	1	5.0			675m	0	70	96	4		C146	DL☑	ITL
38	B8748-8	8	uCT	MNG	2.0	.80	64Ø/1.0kØ	3.0M	1	5.0			675m	0	70	96	4		C146	DL☑	ITL
39	D8035	8	uCT	MNG	2.0	.80	64Ø/0.0Ø	6.0M	1	5.0			675m	0	70	96	4		C146a	DL11e	ITL
40	D8035-8	8	uCT	MNG	2.0	.80	64Ø/0.0Ø	3.0M	1	5.0			675m	0	70	96	4		C146a	DL11e	ITL
41	D8039	8	uCT	MNG	2.0	.80	128/0	11M	1	5.0			700m	0	70	96	5		C103a	DL38	ITL
42	D8039-6	8	uCT	MNG	2.0	.80	128/0	6.0M	1	5.0			700m	0	70	96	5		C103a	DL38	ITL
43	D8048	8	uCT	MNG	2.0	.80	64Ø/1.0kØ	6.0M	1	5.0			675m	0	70	96	4		C146d	DL11e	ITL
44	D8049	8	uCT	MNG	2.0	.80	128/2k	11M	1	5.0			700m	0	70	96	5		C103	DL38	ITL
45	P8035	8	uCT	MNG	2.0	.80	64Ø/0.0Ø	6.0M	1	5.0			675m	0	70	96	4		C146a	DL11d	ITL
46	P8035-8	8	uCT	MNG	2.0	.80	64Ø/0.0Ø	3.0M	1	5.0			675m	0	70	96	4		C146a	DL11d	ITL
47	P8039	8	uCT	MNG	2.0	.80	128/0	11M	1	5.0			700m	0	70	96	5		C103a	DL42f	ITL
48	P8039-6	8	uCT	MNG	2.0	.80	128/0	6.0M	1	5.0			700m	0	70	96	5		C103a	DL42f	ITL
49	P8048	8	uCT	MNG	2.0	.80	64Ø/1.0kØ	6.0M	1	5.0			675m	0	70	96	4		C146d	DL11d	ITL
50	P8048-8	8	uCT	MNG	2.0	.80	64Ø/1.0kØ	3.0M	1	5.0			675m	0	70	96	4		C146d	DL11d	ITL
51	P8049	8	uCT	MNG	2.0	.80	128/2k	11M	1	5.0			700m	0	70	96	5		C103	DL42f	ITL
52	NSC800	8	uCT	MNX	3.5	1.5		1.6u		5.0			1.0	0	70	158	10		C159	DL216	NSC
53	INS8070	8	uCT	MNG	2.0	0.8	64			5.0			500m†	0	70	192			C157	DL216	NSC
54	INS8072	8	uCT	MNG	2.0	0.8	64/2.5k	15.0m		5.0			500m†	0	70	192			C157	DL216	NSC
55	LCP593	8	CdS	MPX			256/256	800k	2	5.0	-9.0		1.6	0	70	48			C43	MD2	CLI
56	LCP593-1	8	CdS	MPX			256/256	500k	2	5.0	-9.0		1.6	0	70	48			C43	MD2	CLI
57	MCP893	8	CdS	MNX			256/256	208M	2	12	5.0	-5.0	2.0	0	70	78			C15	MD2	CLI
58	F100220B	8	Chip		1.1	1.8				4.5	2.0		4.1	0	85				C156	FP21	FSC
59#	TMP8085AP	8	Chip	MNG	2.0	0.8				5.0			1.5 ☑	0	70				C154	DL208	TOSJ
60	uPD8022C	8	Chip	MNG	2.0	.80	64/2k	50uΔ		5.0			1.0 ☑	0	70				C165	DL101	NECM
61	N8X300I	8	Chip	BTD	2.0	.80	16/32%	4.0M	1	5.0			2.2	0	70	21			C82	DL32a	SIC
62	Z8-01MCCCS	8	Chip		2.0	.80	128/2k	8.0M	1	5.0				0	70	43	11		C112	DL190	ZIL
63	Z8-01MCCPS	8	Chip		2.0	.80	128/2k	8.0M	1	5.0				0	70	43	11		C112	DL189	ZIL
64	INS8060D	8	Chip	MNG	2.0	.80§	256/512%	2.0M	1	5.0				0	70	46			C104	DL37d	NSC
65	INS8060N	8	Chip	MNG	2.0	.80§	256/512%	2.0M	1	5.0				0	70	46			C104	DL11f	NSC
66	ISP-8A/600I	8	Chip	MNI	2.0	.80	256/1.0k%	4.0M	1	5.0			250m	0	70	46	4		C65	DL1b	SIC
67	C8008	8	Chip	MNG	3.5	.80	16k▼	500k	2	5.0	-9.0		540m	0	70	48			C43	DL19b	ITL
68	C8008-1	8	Chip	MNG	3.5	.80	16k▼	800k	2	5.0	-9.0		540m	0	70	48			C43	DL19b	ITL
69#	LP8000	8	Chip	MPN	3.5	.80	0/1k	800k	1	5.0	-12		1.0	0	75	48			C42	DL50	GICB
70	R6502	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			575m	0	70	56	13		C12a	DL☑	RKW
71	R6503	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			575m	0	70	56	13		C12b	DL☑	RKW
72	R6504	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			575m	0	70	56	13		C12c	DL☑	RKW
73	R6505	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			575m	0	70	56	13		C12d	DL☑	RKW
74	R6506	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			575m	0	70	56	13		C12e	DL☑	RKW
75	R6507	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			575m	0	70	56	13		C12	DL☑	RKW
76	R6512	8	Chip	MNG	2.4	.40	64/1k	2.0M	2				575m	0	70	56	13		C12f	DL☑	RKW
77	R6513	8	Chip	MNG	2.4	.40	64/1k	2.0M	2				575m	0	70	56	13		C12g	DL☑	RKW
78	R6514	8	Chip	MNG	2.4	.40	64/1k	2.0M	2				575m	0	70	56	13		C12h	DL☑	RKW
79	R6515	8	Chip	MNG	2.4	.40	64/1k	2.0M	2				575m	0	70	56	13		C12j	DL☑	RKW
80	SYC6502	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12a	DL☑	SYK
81	SYC6502A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12a	DL☑	SYK
82	SYC6502B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12a	DL☑	SYK
83▼	SYC6502C	8	Chip		3.3	.40		4.0M	1	5.0				0	70	56			C12a		SYK
84	SYC6503	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12b	DL☑	SYK
85	SYC6503A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12b	DL☑	SYK
86	SYC6503B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12b	DL☑	SYK
87	SYC6504	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12c	DL☑	SYK
88	SYC6504A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12c	DL☑	SYK
89	SYC6504B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12c	DL☑	SYK
90	SYC6505	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12d	DL☑	SYK
91	SYC6505A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12d	DL☑	SYK
92	SYC6505B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12d	DL☑	SYK
93	SYC6506	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12e	DL☑	SYK
94	SYC6506A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12e	DL☑	SYK
95	SYC6506B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12e	DL☑	SYK
96	SYC6507	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12	DL☑	SYK
97	SYC6507A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12	DL☑	SYK
98	SYC6507B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12	DL☑	SYK
99	SYC6512	8	Chip	MNG	4.7	.20		1.0M	2	5.0			700m	0	70	56	13		C12f	DL☑	SYK
100	SYC6512A	8	Chip	MNG	4.7	.20		2.0M	2	5.0			700m	0	70	56	13		C12f	DL☑	SYK
101	SYC6512B	8	Chip	MNG	4.7	.20		3.0M	2	5.0			800m	0	70	56	13		C12f	DL☑	SYK
102	SYC6513	8	Chip	MNG	4.7	.20		1.0M	2	5.0			700m	0	70	56	13		C12g	DL☑	SYK
103	SYC6513A	8	Chip	MNG	4.7	.20		2.0M	2	5.0			700m	0	70	56	13		C12g	DL☑	SYK
104	SYC6513B	8	Chip	MNG	4.7	.20		3.0M	2	5.0			800m	0	70	56	13		C12g	DL☑	SYK
105	SYC6514	8	Chip	MNG	4.7	.20		1.0M	2	5.0			700m	0	70	56	13		C12h	DL☑	SYK
106	SYC6514A	8	Chip	MNG	4.7	.20		2.0M	2	5.0			700m	0	70	56	13		C12h	DL☑	SYK
107	SYC6514B	8	Chip	MNG	4.7	.20		3.0M	2	5.0			800m	0	70	56	13		C12h	DL☑	SYK
108	SYC6515	8	Chip	MNG	4.7	.20		1.0M	2	5.0			700m	0	70	56	13		C12j	DL☑	SYK
109	SYC6515A	8	Chip	MNG	4.7	.20		2.0M	2	5.0			700m	0	70	56	13		C12j	DL☑	SYK
110	SYC6515B	8	Chip	MNG	4.7	.20		3.0M	2	5.0			800m	0	70	56	13		C12j	DL☑	SYK

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

10. MICROPROCESSORS

IN ORDER OF: (1)DATA BITS (2)ARCHITECTURE (3)No. BASIC INSTRUCTIONS & (4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZ. 1 DATA BITS	2 ARCHI-TECT-URE	TECH NOL.	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	RAM/ROM %BIT CONFIG MIXED ▼-bits (BYTES)	MAX. CLOCK FREQ. (Hz)	No Øs	OPER. VOLTAGES V1 (V)	V2 (V)	V3 (V)	MAX. OPER. PWR. DISS. (W)	OPERATING TEMP. (-)	(+)	3 No. BASIC INSTR	A D D R	M O D E	DRAWINGS CPU INTERNAL ARCHITECTURE	OUTLINE Δ=MO	MFR. CODE
1	SYP6502	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12a	DL☑	SYK
2	SYP6502A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12a	DL☑	SYK
3	SYP6502B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12a	DL☑	SYK
4▼	SYP6502C	8	Chip		3.3	.40		4.0M	1	5.0				0	70	56			C12a		SYK
5	SYP6503	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12b	DL☑	SYK
6	SYP6503A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12b	DL☑	SYK
7	SYP6503B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12b	DL☑	SYK
8	SYP6504	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12c	DL☑	SYK
9	SYP6504A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12c	DL☑	SYK
10	SYP6504B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12c	DL☑	SYK
11	SYP6505	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12d	DL☑	SYK
12	SYP6505A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12d	DL☑	SYK
13	SYP6505B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12d	DL☑	SYK
14	SYP6506	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12e	DL☑	SYK
15	SYP6506A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12e	DL☑	SYK
16	SYP6506B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12e	DL☑	SYK
17	SYP6507	8	Chip	MNG	2.4	.40		1.0M	2	5.0			700m	0	70	56	13		C12	DL☑	SYK
18	SYP6507A	8	Chip	MNG	2.4	.40		2.0M	2	5.0			700m	0	70	56	13		C12	DL☑	SYK
19	SYP6507B	8	Chip	MNG	2.4	.40		3.0M	2	5.0			800m	0	70	56	13		C12	DL☑	SYK
20	SYP6512	8	Chip	MNG	4.7	.20		1.0M	2	5.0			700m	0	70	56	13		C12f	DL☑	SYK
21	SYP6512A	8	Chip	MNG	4.7	.20		2.0M	2	5.0			700m	0	70	56	13		C12f	DL☑	SYK
22	SYP6512B	8	Chip	MNG	4.7	.20		3.0M	2	5.0			800m	0	70	56	13		C12f	DL☑	SYK
23	SYP6513	8	Chip	MNG	4.7	.20		1.0M	2	5.0			700m	0	70	56	13		C12g	DL☑	SYK
24	SYP6513A	8	Chip	MNG	4.7	.20		2.0M	2	5.0			700m	0	70	56	13		C12g	DL☑	SYK
25	SYP6513B	8	Chip	MNG	4.7	.20		3.0M	2	5.0			800m	0	70	56	13		C12g	DL☑	SYK
26	SYP6514	8	Chip	MNG	4.7	.20		1.0M	2	5.0			700m	0	70	56	13		C12h	DL☑	SYK
27	SYP6514A	8	Chip	MNG	4.7	.20		2.0M	2	5.0			700m	0	70	56	13		C12h	DL☑	SYK
28	SYP6514B	8	Chip	MNG	4.7	.20		3.0M	2	5.0			800m	0	70	56	13		C12h	DL☑	SYK
29	SYP6515	8	Chip	MNG	4.7	.20		1.0M	2	5.0			700m	0	70	56	13		C12j	DL☑	SYK
30	SYP6515A	8	Chip	MNG	4.7	.20		2.0M	2	5.0			700m	0	70	56	13		C12j	DL☑	SYK
31	SYP6515B	8	Chip	MNG	4.7	.20		3.0M	2	5.0			800m	0	70	56	13		C12j	DL☑	SYK
32	MCS6502	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			700m	0	70	57	13		C12a		MTY
33	MCS6503	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			700m	0	70	57	13		C12b		MTY
34	MCS6504	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			700m	0	70	57	13		C12c		MTY
35	MCS6505	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			700m	0	70	57	13		C12d		MTY
36	MCS6506	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			700m	0	70	57	13		C12e		MTY
37	MCS6507	8	Chip	MNG	2.4	.40	64/1k	2.0M	1	5.0			700m	0	70	57	13		C12		MTY
38	MCS6512	8	Chip	MNG	2.4	.40	64/1k	2.0M	2	5.0			700m	0	70	57	13		C12f		MTY
39	MCS6513	8	Chip	MNG	2.4	.40	64/1k	2.0M	2	5.0			700m	0	70	57	13		C12g		MTY
40	MCS6514	8	Chip	MNG	2.4	.40	64/1k	2.0M	2	5.0			700m	0	70	57	13		C12h		MTY
41	MCS6515	8	Chip	MNG	2.4	.40	64/1k	2.0M	2	5.0			700m	0	70	57	13		C12j		MTY
42#	HD6805P	8	Chip	MNG	2.0	.80	64/1.1K	4.0M	1	5.0			350m	0	70	59	10				HITJ
43♦	MC68A09EL	8	Chip	MNG	2.0	.80		1.5M	2	5.0				0	70	59	10			DL1d	MOTA
44♦	MC68A09EP	8	Chip	MNG	2.0	.80		1.5M	2	5.0				0	70	59	10			DL27	MOTA
45♦	MC68A09L	8	Chip	MNG	2.0	.80		1.5M	2	5.0				0	70	59	10			DL1d	MOTA
46♦	MC68A09P	8	Chip	MNG	2.0	.80		1.5M	2	5.0				0	70	59	10			DL27	MOTA
47♦	MC68B09EL	8	Chip	MNG	2.0	.80		2.0M	2	5.0				0	70	59	10			DL1d	MOTA
48♦	MC68B09EP	8	Chip	MNG	2.0	.80		2.0M	2	5.0				0	70	59	10			DL27	MOTA
49♦	MC68B09L	8	Chip	MNG	2.0	.80		2.0M	2	5.0				0	70	59	10			DL1d	MOTA
50♦	MC68B09P	8	Chip	MNG	2.0	.80		2.0M	2	5.0				0	70	59	10			DL27	MOTA
51♦	MC6809EL	8	Chip	MNG	2.0	.80		1.0M	2	5.0				0	70	59	10			DL1d	MOTA
52♦	MC6809EP	8	Chip	MNG	2.0	.80		1.0M	2	5.0				0	70	59	10			DL27	MOTA
53♦	MC6809L	8	Chip	MNG	2.0	.80		1.0M	2	5.0				0	70	59	10			DL1d	MOTA
54♦	MC6809P	8	Chip	MNG	2.0	.80		1.0M	2	5.0				0	70	59	10			DL27	MOTA
55▼	S6805	8	Chip	MNX	2.0	.80	64/1.0k	4.0M		5.0			350mt	0	70	59	10				AMI
56▼#	SFF9-68A09E	8	Chip	MNG	2.0	.80§		6.0M		5.0			1.0	0	70	59	10			DL167	EFCF
57▼#	SFF9-68A09K	8	Chip	MNG	2.0	.80§		6.0M		5.0			1.0	0	70	59	10			DL167	EFCF
58▼#	SFF9-68B09E	8	Chip	MNG	2.0	.80§		8.0M		5.0			1.0	0	70	59	10			DL167	EFCF
59▼#	SFF9-68B09K	8	Chip	MNG	2.0	.80§		8.0M		5.0			1.0	0	70	59	10			DL167	EFCF
60▼#	SFF9-6809K	8	Chip	MNG	2.0	.80§		4.0M		5.0			1.0	0	70	59	10			DL167	EFCF
61▼	MC146805E2L	8	Chip	MCG	3.0	.80	112/	5.0M	1	5.0			20mt	0	70	61	10		C171	DL228	MOTA
62▼	MC146805E2P	8	Chip	MCG	3.0	.80	112/	5.0M	1	5.0			20mt	0	70	61	10		C171	DL229	MOTA
63▼	MC146805E2S	8	Chip	MCG	3.0	.80	112/	5.0M	1	5.0			20mt	0	70	61	10		C171	DL112b	MOTA
64	uPD8021C	8	Chip	MNG	2.0	.80	64/1k	3.0M	1	5.5			330m	0	70	64				DL67	NECM
65	F3850	8	Chip	MNX	2.9	.80	64/			0.0	12.0		330mt	0	70	71			C154		FSC
66▼#	EF68A00C	8	Chip	MNG	2.0	.80§	65k	1.5M	2	5.0			1.0	0	70	72	7		C13	DL167	EFCF
67▼#	EF68A00CV	8	Chip	MNG	2.0	.80§	65k	1.5M	2	5.0			1.0	40	85	72	7		C13	DL167	EFCF
68▼#	EF68A00P	8	Chip	MNG	2.0	.80§	65k	1.5M	2	5.0			1.0	0	70	72	7		C13	DL167	EFCF
69▼#	EF68A00PV	8	Chip	MNG	2.0	.80§	65k	1.5M	2	5.0			1.0	40	85	72	7		C13	DL167	EFCF
70▼#	EF68B00C	8	Chip	MNG	2.0	.80§	65k	2.0M	2	5.0			1.0	0	70	72	7		C13	DL167	EFCF
71▼#	EF68B00P	8	Chip	MNG	2.0	.80§	65k	2.0M	2	5.0			1.0	0	70	72	7		C13	DL167	EFCF
72▼#	EF6800C	8	Chip	MNG	2.0	.80§	65k	1.0M	2	5.0			1.0	0	70	72	7		C13	DL167	EFCF
73▼#	EF6800CV	8	Chip	MNG	2.0	.80§	65k	1.0M	2	5.0			1.0	40	85	72	7		C13	DL167	EFCF
74▼#	EF6800P	8	Chip	MNG	2.0	.80§	65k	1.0M	2	5.0			1.0	0	70	72	7		C13	DL167	EFCF
75▼#	EF6800PV	8	Chip	MNG	2.0	.80§	65k	1.0M	2	5.0			1.0	40	85	72	7		C13	DL167	EFCF
76▼#	EF6802C	8	Chip	MNG	2.0	.80§	32	1.0M	2	5.0			1.2	0	70	72	7		C67	DL167	EFCF
77▼#	EF6802P	8	Chip	MNG	2.0	.80§	32	1.0M	2	5.0			1.2	0	70	72	7		C67	DL167	EFCF
78	F68A00P	8	Chip		2.0	.80§	65K/	1.5M	2	5.0			1.0	0	70	72	7		C66	DL11i	FSC
79	F68B00P	8	Chip		2.0	.80§	65K/	2.0M	2	5.0			1.0	0	70	72	7		C66	DL11i	FSC
80	F6800	8	Chip		2.0	.30		1.0M	2	5.0			1.2	0	70	72	7		C66	DL☑	FSC
81	F6800C	8	Chip		2.0	.30		1.0M	2	5.0			1.2	40	85	72	7		C66	DL☑	FSC
82#	HD468A00P	8	Chip	MNG	2.0	.80	128/1K	1.5M	2	5.0			1.0	20	75	72	7		C13		HITJ
83#	HD468B00P	8	Chip	MNG	2.0	.80	128/1K	2.0M	2	5.0			1.0	20	75	72	7		C13		HITJ
84#	HD46800DP	8	Chip	MNG	2.0	.80§	128/1k	1.0M	2	5.0			1.0	20	75	72	7		C13	DL☑	HITJ
85#	HD46802P	8	Chip	MNG	2.0	.80	128	4.0M		5.0			1.2	20	75	72	7		C121	DL☑	HITJ
86	JANM38510/40001BQC	8	Chip	MNG	2.0	.80§		1.0M	2	5.0			1.0 ☑	55	125	72	7		C144	DL176	MIL
87	JANM38510/40001CQC	8	Chip	MNG	2.0	.80§		1.0M	2	5.0			1.0 ☑	55	125	72	7		C144	DL176	MIL
88	MC68A00CL	8	Chip	MNG	2.0	.80§	128/1k	1.5M	2	5.0			1.0	40	85	72	7		C13	DL1d	MOTA
89	MC68A00CP	8	Chip	MNG	2.0	.80§	128/1k	1.5M	2	5.0			1.0	40	85	72	7		C13	DL27	MOTA
90	MC68A00L	8	Chip	MNG	2.0	.80§	128/1k	1.5M	2	5.0			1.0	0	70	72	7		C13	DL1d	MOTA
91	MC68A00P	8	Chip	MNG	2.0	.80§	128/1k	1.5M	2	5.0			1.0	0	70	72	7		C13	DL27	MOTA
92	MC68B00L	8	Chip	MNG	2.0	.80§	128/1k	2.0M	2	5.0			1.0	0	70	72	7		C13	DL1d	MOTA
93	MC68B00P	8	Chip	MNG	2.0	.80§	128/1k	2.0M	2	5.0			1.0	0	70	72	7		C13	DL27	MOTA
94	MC6800BQCS	8	Chip	MNG	2.0	.80§	128/1k	1.0M	2	5.0			1.0	55	125	72	7		C13	DL1d	MOTA
95	MC6800CL	8	Chip	MNG	2.0	.80§	128/1k	1.0M	2	5.0			1.2	40	85	72	7		C13	DL1d	MOTA
96	MC6800CP	8	Chip	MNG	2.0	.80§	128/1k	1.0M	2	5.0			1.0	40	85	72	7		C13	DL27	MOTA
97	MC6800CQCS	8	Chip	MNG	2.0	.80§	128/1k	1.0M	2	5.0			1.0	55	125	72	7		C13	DL1d	MOTA
98	MC6800L	8	Chip	MNG	2.0	.80§	128/1k	1.0M	2	5.0			1.2	0	70	72	7		C13	DL1d	MOTA
99	MC6800P	8	Chip	MNG	2.0	.80§	128/1k	1.0M	2	5.0			1.2	0	70	72	7		C13	DL27	MOTA
100	MC6802L	8	Chip	MNG	2.0	.80	128Ø/1k	4.0M	2	5.0			1.2	0	70	72	7		C67	DL1d	MOTA
101	MC6802P	8	Chip	MNG	2.0	.80	128Ø/1k	4.0M	2	5.0			1.2	0	70	72	7		C67	DL27	MOTA
102	MC6808L	8	Chip	MNG	2.0	.80		1.0M	2	5.0			1.2 ☑	0	70	72	7		C67a	DL1d	MOTA
103	MC6808P	8	Chip	MNG	2.0	.80		1.0M	2	5.0			1.2 ☑	0	70	72	7		C67a	DL27	MOTA
104	MD68SC02AC	8	Chip	MCX	2.0	.80	128/	5.0M	2	5.0			15mt	40	85	72	7		C67		MITC
105	MD68SC02AE	8	Chip	MCX	2.0	.80	128/	5.0m	2	5.0			15mt	40	85	72	7		C67		MITC
106▼	S68A02	8	Chip	MNX	2.0	.80	128Ø/512	6.0M	2	5.0			1.2	0	70	72	7		C67	DL1n	AMI
107	S6800	8	Chip	MNX	2.4	.40	128/1.0k	1.0M	2	5.0			1.2	0	70	72	7		C2	DL2	AMI
108	S6802	8	Chip	MNX	2.0	.80	128Ø/512	4.0M	2	5.0			1.2	0	70	72	7		C67	DL1n	AMI

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

10. MICROPROCESSORS

IN ORDER OF: (1)DATA BITS (2)ARCHITECTURE (3)No. BASIC INSTRUCTIONS & (4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZ. 1 DATA BITS	ORGANIZ. 2 ARCHI-TECT-URE	TECH NOL.	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RAM/ROM %BIT CONFIG MIXED ▼-bits (BYTES)	MAX. CLOCK FREQ. (Hz)	No Øs	OPER. VOLTAGES V1 (V)	V2 (V)	V3 (V)	MAX. OPER. PWR. DISS. (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	3 No. BASIC INSTR	A D R	M O D E	DRAWINGS CPU INTERNAL ARCHITECTURE	DRAWINGS OUTLINE Δ=MO	MFR. CODE
1	S6802P	8	Chip	MNX	2.0	.80	128Ø/512	4.0M	2	5.0			1.2	0	70	72	7		C67	DL11k	AMI
2	Am9080A1DC	8	Chip	MNG	3.0	.80	256/256%	3.1M	2	12	5.0	-5.0	820m	0	70	74			C35	DL37b	AMV
3	Am9080A1PC	8	Chip	MNG	3.0	.80	256/256%	3.0M	2	12	5.0	-5.0	820m	0	70	74			C35	DL☑	AMV
4	Am9080A2DC	8	Chip	MNG	3.0	.80	256/256%	2.6M	2	12	5.0	-5.0	820m	0	70	74			C35	DL37b	AMV
5	Am9080A2DM	8	Chip	MNG	3.0	.80	256/256%	2.6M	2	12	5.0	-5.0	820m	55	125	74			C35	DL37b	AMV
6	Am9080A2PC	8	Chip	MNG	3.0	.80	256/256%	2.6M	2	12	5.0	-5.0	820m	0	70	74			C35	DL☑	AMV
7	Am9080A4DC	8	Chip	MNG	3.0	.80	256/256%	4.0M	2	12	5.0	-5.0	820m	0	70	74			C35	DL37b	AMV
8	Am9080ADC	8	Chip	MNG	3.0	.80	256/256%	2.0M	2	12	5.0	-5.0	820m	0	70	74			C35	DL37b	AMV
9	Am9080ADM	8	Chip	MNG	3.0	.80	256/256%	2.0M	2	12	5.0	-5.0	820m	55	125	74			C35	DL37b	AMV
10	Am9080APC	8	Chip	MNG	3.0	.80	256/256%	2.0M	2	12	5.0	-5.0	820m	0	70	74			C35	DL☑	AMV
11	2650	8	Chip	MNG	2.2	.80§	256/1.0k%	1.25M	1	5.0			525m	0	70	75	8		C3	DL1b	SIC
12	2650A-1I	8	Chip	MNG	2.2	.80§	256/1.0k%	6.6M	1	5.0			750m	0	70	75	8		C3	DL1b	SIC
13#	2650A-1N	8	Chip	MNG	2.2	0.8§		2.0M	1	5.0			750m	0	70	75	8		C3	DL1b	PHIN
14	2650AI	8	Chip	MNG	2.2	.80§	256/1.0k%	4.1M	1	5.0			750m	0	70	75	8		C3	DL1b	SIC
15#	2650AN	8	Chip	MNG	2.2	0.8§		1.25M	1	5.0			750m	0	70	75	8		C3	DL1b	PHIN
16#	2650B-1I	8	Chip	MNG	2.2	0.8§		2.0M	1	5.0			750m	0	70	75	8		C3	DL1b	PHIN
17#	2650B-1N	8	Chip	MNG	2.2	0.8§		2.0M	1	5.0			750m	0	70	75	8		C3	DL1b	PHIN
18#	2650BI	8	Chip	MNG	2.2	0.8§		1.25M	1	5.0			750m	0	70	75	8		C3	DL1b	PHIN
19#	2650BN	8	Chip	MNG	2.2	0.8§		1.25M	1	5.0			750m	0	70	75	8		C3	DL1b	PHIN
20	3850	8	Chip	MNX	3.5	.80	64/1.0k	2.0M	1	12	5.0		700m	0	70	76	8		C23		FSC
21	MK3850	8	Chip	MNX	3.5	.80	64/1k	2.0M	1	12	5.0		700m	0	70	76	8		C24		MOS
22	C8080A1	8	Chip	MNG	3.3	.80	256/256%	3.12M	2	12	5.0	-5.0	1.2	0	70	78	4		C15	DL37	ITL
23	C8080A2	8	Chip	MNG	3.3	.80	256/256%	2.63M	2	12	5.0	-5.0	1.2	0	70	78	4		C15	DL37	ITL
24	C8080A	8	Chip	MNG	3.3	.80	256/256%	2.08M	2	12	5.0	-5.0	1.2	0	70	78	4		C15	DL37	ITL
25	D8080A1	8	Chip	MNG	3.3	.80	256/256%	3.12M	2	12	5.0	-5.0	1.5 ☑	0	70	78	4		C15	DL85	ITL
26	D8080A2	8	Chip	MNG	3.3	.80	256/256%	2.63M	2	12	5.0	-5.0	1.5 ☑	0	70	78	4		C15	DL85	ITL
27	D8080A	8	Chip	MNG	3.3	.80	256/256%	2.08M	2	12	5.0	-5.0	1.5 ☑	0	70	78	4		C15	DL85	ITL
28	INS8080AD	8	Chip	MNG	3.3	.80§		2.0M	2	12	5.0	-5.0	1.5 ☑	0	70	78	4		C54	DL1	NSC
29	INS8080AD-1	8	Chip	MNG	3.3	.80§		2.0M	2	12	5.0	-5.0	1.5 ☑	0	70	78	4		C54	DL1	NSC
30#	M5L8080AP	8	Chip	MNG	3.3	.80		2.0M	2	12	5.0	-5.0	1.5 ☑	0	70	78	1		C15	DL123	MITJ
31#	M5L8080AS	8	Chip	MNG	3.3	.80		2.0M	2	12	5.0	-5.0	1.5 ☑	0	70	78	1		C15	DL122	MITJ
32	JANM38510/42001BQB	8	Chip	MNG	3.7	.45%		2.0M	2	12	5.0	-5.0	1.7 ☑	55	125	78	4		C15	DL176	MIL
33	JANM38510/42001CQB	8	Chip	MNG	3.7	.45%		2.0M	2	12	5.0	-5.0	1.7 ☑	55	125	78	4		C15	DL176	MIL
34#	M58710S	8	Chip	MNG	3.3	.80	256/256%	2.0M	2	12	5.0	-5.0	1.5 ☑	0	70	78	4		C120	DL122	MITJ
35	MC8080A	8	Chip	MNG	3.0	.80	256/256%	2.08M	2	12	5.0	-5.0	1.4	55	125	78	4		C15	DL37	ITL
36	MD8080A	8	Chip	MNG	3.0	.80	256/256%	2.08M	2	12	5.0	-5.0	1.4	55	125	78	4		C15	DL85	ITL
37	MK3880	8	Chip	MNG	2.0	.80	256/2k	2.5M	1	5.0			750m	0	70	78	4		C63	DL42d	MOS
38	MKB3880P34	8	Chip	MNG	2.0	.80	256/2k	2.5M	1	5.0			750m	55	100	78	4		C63	DL42d	MOS
39	MP8080AI	8	Chip	MNG	3.3	.80	256/256%		2	12	5.0	-5.0	1.2	0	70	78	4		C15	DL1b	SIC
40	P8080A1	8	Chip	MNG	3.3	.80	256/256%	3.12M	2	12	5.0	-5.0	1.5 ☑	0	70	78	4		C15	DL42f	ITL
41	P8080A2	8	Chip	MNG	3.3	.80	256/256%	2.63M	2	12	5.0	-5.0	1.5 ☑	0	70	78	4		C15	DL42f	ITL
42	P8080A	8	Chip	MNG	3.3	.80	256/256%	2.08M	2	12	5.0	-5.0	1.5 ☑	0	70	78	4		C15	DL42f	ITL
43	TMS8080AJL	8	Chip	MNG	3.3	.80	64/2.0k		2	12	5.0	-5.0	1.5	0	70	78	4		C6	DL1a	TII
44	TMS8080ANL	8	Chip	MNG	3.3	.80	64/2.0k		2	12	5.0	-5.0	1.5	0	70	78	4		C6	DL11	TII
45	uPD8080AD2	8	Chip	MNG	3.0	.80	256/2k%	2.63M		12	5.0	-5.0	1.3	10	70	78	4		C55	DL50b	NECM
46	uPD8080AD	8	Chip	MNG	3.0	.80	256/2k%	2.02M		12	5.0	-5.0	1.3	10	70	78	4		C55	DL50b	NECM
47	uPD8080AFC	8	Chip	MNG	3.3	.80	256/2k	2.0M	2	12	5.0	-5.0	1.3	0	70	78	4		C99	DL101	NECM
48	uPD8080AFC-1	8	Chip	MNG	3.3	.80	256/2k	3.0M	2	12	5.0	-5.0	1.3	0	70	78	4		C99	DL101	NECM
49	uPD8080AFC-2	8	Chip	MNG	3.3	.80	256/2k	2.5M	2	12	5.0	-5.0	1.3	0	70	78	4		C99	DL101	NECM
50	uPD8080AFD	8	Chip	MNG	3.3	.80	256/2k	2.0M	2	12	5.0	-5.0	1.3	0	70	78	4		C99	DL50b	NECM
51	uPD8080AFD-1	8	Chip	MNG	3.3	.80	256/2k	3.0M	2	12	5.0	-5.0	1.3	0	70	78	4		C99	DL50b	NECM
52	uPD8080AFD-2	8	Chip	MNG	3.3	.80	256/2k	2.5M	2	12	5.0	-5.0	1.3	0	70	78	4		C99	DL50b	NECM
53	Am8085ACC	8	Chip		2.0	.45		3.0M	2	5.0			850m	0	70	80	4		C87	DL180	AMV
54	Am8085ADC	8	Chip		2.0	.45		3.0M	2	5.0			850m	0	70	80	4		C87	DL178	AMV
55	Am8085APC	8	Chip		2.0	.45		3.0M	2	5.0			850m	0	70	80	4		C87	DL179	AMV
56	C8085A2	8	Chip	MNX	2.0	.80	256/256%	5.0M	1	5.0			850m	0	70	80	4		C58	DL37	ITL
57	C8085A	8	Chip	MNX	2.0	.80	256/256%	3.0M	1	5.0			850m	0	70	80	4		C58	DL37	ITL
58#	M5L8085AP-20	8	Chip	MNG	2.2	.80		3.0M		5.0			1.5 ☑	0	70	80	1		C58	DL123	MITJ
59#	M5L8085AS-20	8	Chip	MNG	2.2	.80		3.0M		5.0			1.5 ☑	0	70	80	1		C58	DL122	MITJ
60	P8085A2	8	Chip	MNX	2.0	.80	256/256%	5.0M	1	5.0			850m	0	70	80	4		C58	DL42f	ITL
61	P8085A	8	Chip	MNX	2.0	.80	256/256%	3.0M	1	5.0			850m	0	70	80	4		C58	DL42f	ITL
62	uPD8085AC	8	Chip	MNX	2.0	.80		3.0M	1	5.0			850m	0	70	80			C87	DL101	NECM
63	MC6801EL	8	Chip	MNG	2.0	.80	128/2k			5.0				0	70	82	7		C124		MOTA
64	MC6801L	8	Chip	MNG	2.0	.80	128/2k			5.0				0	70	82	7		C123		MOTA
65	B8035L	8	Chip	MNG	2.0	.80	64/1k	2.5uΔ		7.0			1.5	0	70	90			C59b	DL☑	ITL
66	B8039-6	8	Chip	MNG	2.0	.80	128/2k	6.0M		7.0			1.5	0	70	90			C103	DL☑	ITL
67	B8748-6	8	Chip	MNG	2.0	.80	64/1k	2.5uΔ		7.0			1.5	0	70	90			C59b	DL☑	ITL
68	C8035L	8	Chip	MNG	2.0	.80	64/1k	2.5uΔ		7.0			1.5	0	70	90			C59b	DL70	ITL
69	C8748-6	8	Chip	MNG	2.0	.80	64/1k	2.5uΔ		7.0			1.5	0	70	90			C59b	DL70	ITL
70	C8748-8	8	Chip	MNG	2.0	.80	64/1k	4.1uΔ		7.0			1.5	0	70	90			C59b	DL70	ITL
71	D8035L	8	Chip	MNG	2.0	.80	64/1k	2.5uΔ		7.0			1.5	0	70	90			C59b	DL148	ITL
72	P8035L	8	Chip	MNG	2.0	.80	64/1k	2.5uΔ		7.0			1.5	0	70	90			C59b	DL149	ITL
73	CDP1802CD	8	Chip	MCG	3.5	1.5	32/512	3.2M	1	5.0			10m†	55	125	91			C44	DL1f	RCA
74	CDP1802CE	8	Chip	MCG	3.5	1.5	32/512	3.2M	1	5.0			10m†	40	85	91			C44	DL1f	RCA
75	CDP1802D	8	Chip	MCG	7.0	3.0	32/512	6.4M	1	10			100m†	55	125	91			C44	DL1f	RCA
76	CDP1802E	8	Chip	MCG	3.5	1.5	32/512	3.2M	1	5.0			10m†	40	85	91			C44	DL1f	RCA
77	HCMP1802CD	8	Chip	MCG	3.5	1.5	32/512	3.2M	1	5.0			2.5m	55	125	91	7		C44	DL☑	HAC
78	HCMP1802D	8	Chip	MCG	7.0	3.0	32/512	6.4M	1	10			5.0m	55	125	91	7		C44	DL☑	HAC
79#	8048-8I	8	Chip	MNG	2.0	.80	64/1k	6.0M	1	5.0			675m	0	70	96			C146d	DL☑	PHIN
80#	8048-8N	8	Chip	MNG	2.0	.80	64/1k	6.0M	1	5.0			675m	0	70	96			C146d	DL☑	PHIN
81#	8748-8I	8	Chip	MNG	2.0	.80	64/1k*	6.0M	1	5.0			675m	0	70	96			C146	DL☑	PHIN
82#	8748I	8	Chip	MNG	2.0	.80	64/1k*	6.0M	1	5.0			675m	0	70	96			C146	DL☑	PHIN
83	MP8035-8I	8	Chip	MNG	2.0	.80	64/0	6.0m	1	5.0			675m	0	70	96			C146a	DL☑	SIC
84	MP8035LI	8	Chip	MNG	2.0	.80	64/0	6.0M	1	5.0			675m	0	70	96			C146a	DL☑	SIC
85	MP8035LN	8	Chip	MNG	2.0	.80	64/0	6.0m	1	5.0			675m	0	70	96			C146a	DL☑	SIC
86	MP8039I	8	Chip	MNG	2.0	.80	128/2K			5.0			850m	0	70	96			C146b	DL☑	SIC
87	MP8039N	8	Chip	MNG	2.0	.80	128/2k			5.0			850m	0	70	96			C146b	DL☑	SIC
88	MP8048I	8	Chip	MNG	2.0	.80	64/1K	6.0M	1	5.0			675m	0	70	96			C146d	DL☑	SIC
89	MP8048N	8	Chip	MNG	2.0	.80	64/1k	6.0M	1	5.0			675m	0	70	96			C146d	DL☑	SIC
90	MP8049I	8	Chip	MNG	2.0	.80	128/2K			5.0			850m	0	70	96			C146b	DL☑	SIC
91	MP8049N	8	Chip	MNG	2.0	.80	128/2k			5.0			850m	0	70	96			C146b	DL☑	SIC
92#	uPD8035LC	8	Chip	MNG	2.0	.80	64/1k	6.0M	1	5.0			675m	0	70	96			C141	DL176	NECJ
93	uPD8039LC	8	Chip	MNX	2.0	.80	128/0Ø	400k	1	5.0			700m	0	70	96			C141	DL174	NECM
94	uPD8039LD	8	Chip	MNX	2.0	.80	128/0Ø	400k	1	5.0			700m	0	70	96			C141	DL174	NECM
95	uPD8048C	8	Chip	MNG	2.0	.80	64/1k	6.0M	1	5.0			675m	0	70	96			C141	DL101	NECM
96	uPD8049C	8	Chip	MNX	2.0	.80	128/2kØ	400k	1	5.0			700m	0	70	96			C141	DL101	NECM
97	uPD8049D	8	Chip	MNX	2.0	.80	128/2kØ	400k	1	5.0			700m	0	70	96			C141	DL174	NECM
98	uPD8748D	8	Chip	MNG	2.0	.80	64/1k*	6.0M	1	5.0			675m	0	70	96			C141	DL174	NECM
99	CDP1804CD	8	Chip	MCG	3.5	1.5	64Ø/2kØ	3.2M	1	5.0			10m†	55	125	106			C118	DL1F	RCA
100	CDP1804CE	8	Chip	MCG	3.5	1.5	64Ø/2kØ	3.2M	1	5.0			10m†	40	85	106			C118		RCA
101	CDP1804D	8	Chip	MCG	7.0	3.0	64Ø/2kØ	6.4M	1	10			100m†	55	125	106			C118	DL1f	RCA
102	CDP1804E	8	Chip	MCG	7.0	3.0	64Ø/2kØ	6.4M	1	10			100m†	40	85	106			C118		RCA
103	C8088	8	Chip	MNG	2.0	.80	1.0M▼	5.0M	1	5.0			2.5	0	70	111	24		C143	DL70	ITL
104	D8088	8	Chip	MNG	2.0	.80		5.0M	1	5.0			1.3	0	70	111	24		C143	DL175	ITL
105	P8088	8	Chip	MNG	2.0	.80	1.0M▼	5.0M	1	5.0			2.5	0	70	111	24		C143	DL149	ITL
106	B8085A	8	Chip	MNX	2.0	.80	256/256%	1.3uΔ		5.0			1.5	0	70	113			C87	DL☑	ITL
107	B8085A-2	8	Chip	MNX	2.0	.80	256/256%	.80uΔ		5.0			1.5	0	70	113			C87	DL☑	ITL
108	D8085A	8	Chip	MNX	2.0	.80	256/256%	1.3uΔ		5.0			1.5	0	70	113			C78	DL148	ITL

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

10. MICROPROCESSORS

IN ORDER OF: (1)DATA BITS (2)ARCHITECTURE (3)No. BASIC INSTRUCTIONS & (4)TYPE No.

LINE No.	[4] TYPE No.	ORGANIZ. [1] DATA BITS	[2] ARCHI-TECT-URE	TECH NOL.	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	RAM/ROM %BIT CONFIG MIXED ▼-bits (BYTES)	MAX. CLOCK FREQ. (Hz)	No Øs	OPER. VOLTAGES V1 (V)	V2 (V)	V3 (V)	MAX. OPER. PWR. DISS. (W)	OPERATING TEMP. (-)	(+)	[3] No. BASIC INSTR	AM DO DD RE	DRAWINGS CPU INTERNAL ARCHITECTURE	OUTLINE Δ=MO	MFR. CODE
1	D8085A-2	8	Chip	MNX	2.0	.80	256/256%	.80uΔ		5.0			1.5	0	70	113		C78	DL148	ITL
2	B8080A	8	Chip	MNG	3.3	.80	128/2k	2.0uΔ		20	20		1.5	0	70	121		C15	DL☐	ITL
3	B8080A-1	8	Chip	MNG	3.3	.80	128/2k	1.3uΔ		20	20		1.5	0	70	121		C15	DL☐	ITL
4	B8080A-2	8	Chip	MNG	3.3	.80	128/2k	1.5uΔ		20	20		1.5	0	70	121		C15	DL☐	ITL
5	uPD7801B	8	Chip	MNG			128/4k	2.0uΔ	1	5.0						125		C163	FP11	NECM
6#	uPD780C	8	Chip	MNI	2.0	.80§	26/0	2.5M	1	5.0			750m	0	70	158		C122	DL101	NECJ
7#	uPD780C-1	8	Chip	MNI	2.0	.80§	26/0	4.0M	1	5.0			1.0	0	70	158		C122	DL101	NECJ
8#	uPD780D	8	Chip	MNI	2.0	.80§	26/0	2.5M	1	5.0			750m	0	70	158		C122	DL174	NECJ
9#	uPD780D-1	8	Chip	MNI	2.0	.80§	26/0	4.0M	1	5.0			1.0	0	70	158		C122	DL174	NECJ
10	Z80-CPUCE	8	Chip	MNG	2.0	.80	4k/0▼	2.5M	1	5.0			750m	40	85	158	10	C81	DL1k	ZIL
11	Z80-CPUCM	8	Chip	MNG	2.0	.80	4k/0▼	2.5M	1	5.0			750m	55	125	158	10	C81	DL1k	ZIL
12	Z80-CPUCS	8	Chip	MNG	2.0	.80	4k/0▼	2.5M	1	5.0			750m	0	70	158	10	C81	DL1k	ZIL
13	Z80-CPUPS	8	Chip	MNG	2.0	.80	4k/0▼	2.5M	1	5.0			750m	0	70	158	10	C81	DL1k	ZIL
14	Z80A-CPUCS	8	Chip	MNG	2.0	.80	4k/0▼	4.0M	1	5.0			1.0	0	70	158	10	C81	DL1k	ZIL
15	Z80A-CPUPS	8	Chip	MNG	2.0	.80	4k/0▼	4.0M	1	5.0			1.0	0	70	158	10	C81	DL1k	ZIL
16	MCP1600	8	ChS	MNG	4.0	.80	0.0/512%	3.3M	4	12	5.0	-5.0		0	70	84		C14		WDC
17▼#	HD68A09DC	8	CPU	MNG	2.0	.80§		4.0M		5.0			1.0	0	70	59				HITJ
18▼#	HD68A09DP	8	CPU	MNG	2.0	.80§		4.0M		5.0			1.0	0	70	59				HITJ
19▼#	HD68B09DC	8	CPU	MNG	2.0	.80§		4.0M		5.0			1.0	0	70	59				HITJ
20▼#	HD68B09DP	8	CPU	MNG	2.0	.80§		4.0M		5.0			1.0	0	70	59				HITJ
21▼#	HD6809DC	8	CPU	MNG	2.0	.80§		4.0M		5.0			1.0	0	70	59				HITJ
22▼#	HD6809DP	8	CPU	MNG	2.0	.80§		4.0M		5.0			1.0	0	70	59				HITJ
23	9000-0080	8	MOD		3.3	.80	1k/2k	2.0M	2	12	5.0	-5.0				72	4	C76		DSI
24	M68MM02	8	MOD	MNG	2.0	.80§	128/1k	1.0M	2	5.0			1.2	0	70	72	7	C68	MD2q	MOTA
25	MX800	8	MOD	MNX			256/512		2							72			MD2a	ICC
26	CPU-TAI	8	MOD	MNX			4k			5.0				0	45	74			MD2e	TAI
27	MM1-CPU	8	MOD	MNG	2.0	.80	1kØ/4kØ	2.0M	2	5.0	12	-12	10	0	70	78	4	C74	MD3	CLI
28	MICRO1	8	MOD				0.0/1.0k	4.5M	2	12	5.0	-16		0	50	107		C33		MID
29	M8A	8	MOD	BTX			5k/2k▼	4.0M	1	5.0			9.8	0	60	134	4		MD2c	DSI
30	MK77850	8	MOD		2.4	.50	4k/256	2.5M	1	5.0			5.5	0	50	158		C147		MOS
31	MK77850-4	8	MOD		2.4	.50	4k/256	4.0M	1	5.0			5.5	0	50	158		C147		MOS
32#	T3190-1	12	Chip	MPG	3.6	.80	4.0k		3	5.0	-5.0		1.0	20	80	19		C49	DL56	TOSJ
33	HM6100-2	12	Chip	MCG	3.5	1.0	4.0k	4.0M	1	5.0			12m	55	125	67	3	C1	DL1	HAS
34	HM6100-9	12	Chip	MCG	3.5	1.0	4.0k	4.0M	1	5.0			12m	40	85	67	3	C1	DL1	HAS
35	HM6100A-2	12	Chip	MCG	7.0	2.0	4.0k	8.0M	1	10			100m	55	125	67	3	C1	DL1	HAS
36	HM6100A-9	12	Chip	MCG	7.0	2.0	4.0k	8.0M	1	10			100m	40	85	67	3	C1	DL1	HAS
37	HM6100C-5	12	Chip	MCG	3.5	1.0	4.0k	3.3M	1	5.0			25m	0	70	67	3	C1	DL1	HAS
38	IM6100-1IDL	12	Chip	MCG	3.5	1.0	4k	3.33M	1	5.0			12m	40	85	67	2	C1	DL37a	INL
39	IM6100-1IPL	12	Chip	MCG	3.5	1.0	4k	3.33M	1	5.0			12m	40	85	67	2	C1	DL86	INL
40	IM6100-1MDL	12	Chip	MCG	3.5	1.0	4k	2.5M	1	5.0			12m	55	125	67	2	C1	DL37a	INL
41	IM6100AIDL	12	Chip	MCG	3.5	1.0	4.0k	5.71M	1	10			100m	40	85	67	2	C1	DL37a	INL
42	IM6100AIPL	12	Chip	MCG	3.5	1.0	4.0k	5.71M	1	10			100m	40	85	67	2	C1	DL86	INL
43	IM6100AMDL	12	Chip	MCG	3.5	1.0	4.0k	5.0M	1	10			100m	55	125	67	2	C1	DL37a	INL
44	IM6100IPL	12	Chip	MCG	3.5	1.0	4.0k	2.5M	1	5.0			12m	40	85	67	2	C1	DL86	INL
45	MC68000	16	uCT	MNG									1.2 †	0	70	56	14	C162	DL☐	MOTA
46♦	MC68000L	16	uCT	MNG									1.2 †	0	70	56	14	C162	DL231	MOTA
47	SBP9900ACJ	16	Chip▼	BIX	2.0	.80	2k/8k	3.0M	1	.56			500m†	0	70			C62	DL15	TII
48	SBP9900AEJ	16	Chip▼	BIX	2.0	.80	2k/8k	3.0M	1	.50			500m†	40	85			C62	DL15	TII
49	SBP9900AMJ	16	Chip▼	BIX	2.0	.80	2k/8k	3.0M	1	.50			500m†	55	125			C62	DL15	TII
50	SBP9900ANJ	16	Chip▼	BIX	2.0	.80	2k/8k	3.0M	1	.50			500m†	55	125			C62	DL15	TII
51	TMS9916	16	Chip	MNG	3.3	.80	1023/2k	2.0M	2	12	5.0	-5.0	800m	0	70		15	C150		TII
52#	MN1610	16	Chip	MNG	2.4	.80	8k/8k	2.0M	2	12	5.0	-3.0	1.2	30	100	33	6	C32	DL48	PAFJ
53	mN601	16	Chip	MNG	2.75	.50%	4k/0▼	8.33M	2	14	10	5.0	1.1	0	70	41	5	C75	DL6n	DGC
54	mN602	16	Chip	MNX	2.5	.50		4.16M	2	12	5.0	-5.0	1.1 †	0	70	41	5	C135	DL1a	DGC
55	IMP16C200A	16	Chip	MPG	4.0	-2.0	256/512	5.7M	4	5.0	-12			0	70	43	4	C41	DL☐	NSC
56	INS8900D	16	Chip	MNG	2.4	.80	256/512%	2.0M	1	12	5.0	-8.0	1.3	0	70	45	4	C105	DL37d	NSC
57▼#	EF68000	16	Chip	MNG	2.0	.80§		8.0M		5.0			1.2 †	0	70	56	14	C162		EFCF
58▼	MC68000L4	16	Chip	MNG	2.0	.80		4.0M		5.0			1.0 †	0	70	56	14	C162	DL231	MOTA
59▼	MC68000L6	16	Chip	MNG	2.0	.80		6.0M		5.0			1.0 †	0	70	56	14	C162	DL231	MOTA
60	S9900	16	Chip	MNG	2.4	.40	2k/8k	3.0M	4	12	5.0	-5.0	1.2	0	70	67	5	C5		AMI
61	TMS9900	16	Chip	MNG	2.4	.40	2.0k/8k	3.0M	4	12	5.0	-5.0	1.2	0	70	67	5	C5	DL15	TII
62	TMS9900-40	16	Chip	MNG	2.2	.80	2.0k/8k	4.0M	4	12	5.0	-5.0	1.2m	0	70	67	5	C5	DL15	TII
63	TMS9980A	16	Chip	MNG	2.2	.80		10M	4	12	5.0	-5.0	1.2	0	70	67		C133a		TII
64	TMS9981	16	Chip	MNG	2.2	.80		10M	4	12	5.0	-5.0	1.2	0	70	67		C133b		TII
65	S9980	16	Chip	MNG	2.4	.40	2k/8k	2.5M	4	12	5.0	-5.0	855m	0	70	69	8	C64		AMI
66▼	S9981	16	Chip	MNG	2.4	.40	2k/8k	2.5M	4	12	5.0	-5.0	855m	0	70	69	8	C64	DL1n	AMI
67	CP1600	16	Chip	MNI	2.4	.65	256/512%	3.3M	2	12	5.0	-3.0	900m	0	70	87	4	C37	DL42b	GIC
68	CP1600A	16	Chip	MNI	2.4	.65	256/512%	5.0M	2	12	5.0	-3.0	900m	0	70	87	4	C37	DL42b	GIC
69	CP1610	16	Chip	MNI	2.4	.65	256/512%	2.0M	2	11	5.0	-3.0	1.3	0	70	87	4	C119	DL42b	GIC
70	Z8001CPU	16	Chip	MNX	2.0	.80		4.0M	1	5.0			1.5	0	70	110	8	C151	DL190	ZIL
71▼#	Z8001CPUD1	16	Chip	MNG	2.0	.80		4.0M	1	5.0				0	70	110	8	C151		SGAI
72	Z8002CPU	16	Chip	MNX	2.0	.80		4.0M	1	5.0			1.5	0	70	110	8	C152	DL191	ZIL
73▼#	Z8002CPUD1	16	Chip	MNG	2.0	.80		4.0M	1	5.0				0	70	110	8	C152		SGAI
74	D8086	16	Chip	MNG	2.0	.80§	512/512	5.0M	1	5.0			1.4	0	70	111	24	C116	DL38	ITL
75	D8086-4	16	Chip	MNG	2.0	.80§	512/512	4.0M	1	5.0			1.4	0	70	111	24	C116	DL38	ITL
76	C8086	16	Chip	MNG	2.0	.80	1.0M▼	5.0M		5.0			2.5	0	70	134	24	C116	DL70	ITL
77	C8086-2	16	Chip	MNG	2.0	.80	1.0M▼	8.0M		5.0			2.5	0	70	134	24	C116	DL70	ITL
78	C8086-4	16	Chip	MNG	2.0	.80	1.0M▼	4.0M		5.0			2.5	0	70	134	24	C116	DL70	ITL
79	D8086-2	16	Chip	MNG	2.0	.80	1.0M▼	8.0M		5.0			2.5	0	70	134	24	C116	DL148	ITL
80	P8086	16	Chip	MNG	2.0	.80	1.0M▼	5.0M		5.0			2.5	0	70	134	24	C116	DL149	ITL
81	P8086-2	16	Chip	MNG	2.0	.80	1.0M▼	8.0M		5.0			2.5	0	70	134	24	C116	DL149	ITL
82	P8086-4	16	Chip	MNG	2.0	.80	1.0M▼	4.0M		5.0			2.5	0	70	134	24	C116	DL149	ITL
83#	uPD755D	16	ChS	MNX	3.0	.80				12	5.0	-5.0	1.0	10	70			C57	DL58	NECJ
84	WD9000	16	ChS		4.0	.80	0/11k▼%	3.0M	4	12	5.0	-3.9		0	70					WDC
85	MP1600	16	ChS	MNG	4.0	.80	0.0/512%	3.3M	4	12	5.0	-5.0		0	70	112	23	C14a		WDC
86▼#	HD68000DC	16	CPU	MNG	2.0	.80§		8.0M		5.0			1.2 †	0	70	56	14	C162		HITJ
87	AMC95/4016	16	MOD				8k/12k	4.0m												AUC
88	IMP16C200	16	MOD	MPG	4.0	-2.0	256/0.0	5.7M	4	5.0	-12			0	70	43	4	C41	DL☐	NSC
89	IMP16C400	16	MOD	MPG	4.0	-2.0	1k/1k	5.7M	4	5.0	-12			0	70	43	4	C41	DL☐	NSC
90	IMP16C300	16	MOD	MPG	4.0	-2.0	256/512	5.7M	4	5.0	-12			0	70	60	4	C41	DL☐	NSC
91	IMP16C500	16	MOD	MPG	4.0	-2.0	1k/1k	5.7M	4	5.0	-12			0	70	60	4	C41	DL☐	NSC
92	MIPROCF-16	16	MOD	BTD	2.0	.80	8k/8k	4.0M	1	5.0			17	0	70	83		C34		PLM
93	MIPROCM-16	16	MOD	BTD	2.0	.80	8k/8k	2.85M	1	5.0			17	0	70	83		C34	MD2b	PLM

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

11. READ-WRITE MEMORIES (RAMS)

IN ORDER OF: (1)No. WORDS (2)BITS PER WORD (3)WORST CASE R/W CYCLE TIME &(4)TYPE No.

LINE No.	TYPE No. [4]	ORGANIZATION [1] No. WORDS	ORGANIZATION [2] BITS PER WORD	MODE	TECHNOLOGY	[3] W/C Min. Rd/Wr CYC.TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED POWER SUPPLY SPAN NEG. (V)	RATED POWER SUPPLY SPAN POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	MFR. CODE
1	MCM10145F	16	4	S	BEX	4.0n$	650m	5.2	0.0	-.81	-1.47	0	75	A79	FP10	MOTA
2	Am29700DC	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80	0	75	A65	DL6e	AMV
3	Am29700DM	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80	55	125	A65	DL6e	AMV
4	Am29700FM	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80	55	125	A65	FP1a	AMV
5	Am29700PC	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80	0	75	A65	DL33c	AMV
6	Am29701DC	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80§	0	75	A65	DL6e	AMV
7	Am29701DM	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80§	55	125	A65	DL6e	AMV
8	Am29701FM	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80§	55	125	A65	FP1a	AMV
9	Am29701PC	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80§	0	75	A65	DL33c	AMV
10	Am29702DC	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80	0	75	A66	DL6e	AMV
11	Am29702DM	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80	55	125	A66	DL6e	AMV
12	Am29702FM	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80	55	125	A66	FP1a	AMV
13	Am29702PC	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80	0	75	A66	DL33c	AMV
14	Am29703DC	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80§	0	75	A66	DL6e	AMV
15	Am29703DM	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80§	55	125	A66	DL6e	AMV
16	Am29703FM	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80§	55	125	A66	FP1a	AMV
17	Am29703PC	16	4	S	BTD	18n†	500m†	0.0	5.0	2.0	.80§	0	75	A66	DL33c	AMV
18	N82S25F	16	4	S	BTD	20n	525m	0.0	5.0	2.0	.85	0	75	A6	DL6	SIC
19▼	N82S25N	16	4	S	BTD	20n	525m	0.0	5.0	2.0	.85	0	75	A6	DL4	SIC
20	Am29704DC	16	4	S	BTD	25n†	885m	0.0	5.0	2.0	.80	0	70	A67	DL49	AMV
21	Am29704DM	16	4	S	BTD	25n†	885m	0.0	5.0	2.0	.80	55	125	A67	DL49	AMV
22	Am29704FM	16	4	S	BTD	25n†	885m	0.0	5.0	2.0	.80	55	125	A67	FP5	AMV
23	Am29704PC	16	4	S	BTD	25n†	885m	0.0	5.0	2.0	.80	0	70	A67		AMV
24	Am29705DC	16	4	S	BTD	25n†	885m	0.0	5.0	2.0	.80§	0	70	A67	DL49	AMV
25	Am29705DM	16	4	S	BTD	25n†	885m	0.0	5.0	2.0	.80§	55	125	A67	DL49	AMV
26	Am29705FM	16	4	S	BTD	25n†	885m	0.0	5.0	2.0	.80§	55	125	A67	FP5	AMV
27	Am29705PC	16	4	S	BTD	25n†	885m	0.0	5.0	2.0	.80§	0	70	A67		AMV
28	IDM29702JC	16	4	S	BTD	25n$	525m	0	5.0	2.0	0.8	0	70	A113	DL	NSC
29	IDM29702JM	16	4	S	BTD	25n$	525m	0	5.0	2.0	0.8	55	125	A113	DL	NSC
30	IDM29702JM/883	16	4	S	BTD	25n$	525m	0	5.0	2.0	0.8	55	125	A113	DL	NSC
31	S82S25F	16	4	S	BTD	25n	600m	0.0	5.0	2.0	.80	55	125	A6	DL6	SIC
32	SN54S189J	16	4	S	BTD	25n†	550m	0.0	5.0	2.0	.80§	55	125	A38	DL6d	TII
33	SN54S189W	16	4	S	BTD	25n†	550m	0.0	5.0	2.0	.80§	55	125	A38	Δ004AG	TII
34	SN54S289J	16	4	S	BTD	25n†	525m	0.0	5.0	2.0	.80	55	125	A38	DL6d	TII
35	SN54S289W	16	4	S	BTD	25n†	525m	0.0	5.0	2.0	.80	55	125	A38	Δ004AG	TII
36	SN74S189J	16	4	S	BTD	25n†	550m	0.0	5.0	2.0	.80§	0	70	A38	DL6d	TII
37	SN74S189N	16	4	S	BTD	25n†	550m	0.0	5.0	2.0	.80§	0	70	A38	DL23	TII
38	SN74S289J	16	4	S	BTD	25n†	525m	0.0	5.0	2.0	.80	0	70	A38	DL6d	TII
39	SN74S289N	16	4	S	BTD	25n†	525m	0.0	5.0	2.0	.80	0	70	A38	DL23	TII
40	9410DC	16	4	S	BTD	35n$†	550m	0.0	5.0	2.0	.80§	0	75	A133	DL152	FSC
41	9410DM	16	4	S	BTD	35n$†	550m	0.0	5.0	2.0	.70§	55	125	A133	DL152	FSC
42	9410PC	16	4	S	BTD	35n$†	550m	0.0	5.0	2.0	.80§	0	75	A133	DL153	FSC
43	IDM29702DC	16	4	S	BED	35n$	550m	0.0	5.0	2.0	.80§	0	70	A113	DL6q	NSC
44	IDM29702NC	16	4	S	BED	35n$	550m	0.0	5.0	2.0	.80§	0	70	A113	DL33a	NSC
45	IDM29703JC	16	4	S	BED	35n$	525m	0.0	5.0	2.0	.80	0	70	A113	DL6q	NSC
46	IDM29703NC	16	4	S	BED	35n$	525m	0.0	5.0	2.0	.80	0	70	A113	DL33a	NSC
47	IDM29704AJC	16	4	S	BED	35n$	775m	0.0	5.0	2.0	.80	0	70	A67	DL36g	NSC
48	IDM29705AJC	16	4	S	BED	35n$	775m	0.0	5.0	2.0	.80	0	70	A67	DL36g	NSC
49	IDM29705ANC	16	4	S	BED	35n$	775m	0.0	5.0	2.0	.80	0	70	A67	DL67c	NSC
50	IDM29704AJM	16	4	S	BED	40n$	725m	0.0	5.0	2.0	.80	55	125	A67	DL36g	NSC
51	IDM29705AJM	16	4	S	BED	40n$	725m	0.0	5.0	2.0	.80	55	125	A67	DL36g	NSC
52	IDM29903JC	16	4	S	BED	40n$	500m	0.0	5.0	2.0	.80	0	70	A114	DL40c	NSC
53	IDM29903NC	16	4	S	BED	40n$	500m	0.0	5.0	2.0	.80	0	70	A114	DL111	NSC
54	IDM29702DM	16	4	S	BED	50n$	550m	0.0	5.0	2.0	.80§	55	125	A113	DL6q	NSC
55	IDM29703JM	16	4	S	BED	50n$	525m	0.0	5.0	2.0	.80	55	125	A113	DL6q	NSC
56	MCM4064L	16	4	S	BTD	60n$	551m	0.0	5.0	2.0	.80	0	85	A38	DL53a	MOTA
57	MCM4364L	16	4	S	BTD	60n$	551m	0.0	5.0	2.0	.80	55	125	A38	DL53a	MOTA
58	CDP1824D	32	8	S	MCG	200n$†	5.0m†	0.0	10	7.0	3.0	55	125	A34	DL25	RCA
59	HCMP1824D	32	8	S	MCG	200n$†	5.0m†	0.0	10	7.0	3.0	55	125	A34	DL☑	HAC
60	CDP1824E	32	8	S	MCG	320n$	5.0m	0.0	10	7.0	3.0	40	85	A34	DL119	RCA
61	CDP1824CD	32	8	S	MCG	400n$†	2.5m†	0.0	5.0	3.5	1.5	55	125	A34	DL25	RCA
62	HCMP1824CD	32	8	S	MCG	400n$†	2.5m†	0.0	5.0	3.5	1.5	55	125	A34	DL☑	HAC
63	CDP1824CE	32	8	S	MCG	710n$	2.5m	0.0	5.0	3.5	1.5	40	85	A34	DL119	RCA
64	TMS4036NL	64	8	S	MNG	1.0u	250m†	0.0	5.0	2.0	.80§	0	70	A130	DL17	TII
65▼	N82S09F	64	9	S	BTD	35n	950m	0.0	5.0	2.0	.85	0	75	A4	DL10	SIC
66▼	S82S09F	64	9	S	BTD	50n	1.0	0.0	5.0	2.0	.80	55	125	A4	DL10	SIC
67	IM6512AIDN	64	12	S	MCG	150n$	2.5m	0.0	10	7.0	2.0	40	85	A55	DL25a	INL
68	IM6512AIJN	64	12	S	MCG	150n$	2.5m	0.0	10	7.0	2.0	40	85	A55	DL40a	INL
69	IM6512AMDN	64	12	S	MCG	150n$	2.5m	0.0	10	7.0	2.0	55	125	A55	DL25a	INL
70	IM6512AMFN	64	12	S	MCG	150n$	2.5m	0.0	10	7.0	2.0	55	125	A55	FP6	INL
71	IM6512AMJN	64	12	S	MCG	150n$	2.5m	0.0	10	7.0	2.0	55	125	A55	DL40a	INL
72	HM6511-2	64	12	S	MCG	240n	12.5m	0.0	5.0	2.5	1.5§	55	125	A119	DL☑	HAS
73	HM6511-9	64	12	S	MCG	240n	12.5m	0.0	5.0	2.5	1.5§	40	85	A119	DL☑	HAS
74	HM6511C-9	64	12	S	MCG	240n	12.5m	0.0	5.0	2.5	1.5§	40	85	A119	DL☑	HAS
75	HM1-6512-2	64	12	S	MCG	450n	22m☑	0.0	5.0	3.0	.80§	55	125	A55a	DL40d	HAS
76	HM1-6512-9	64	12	S	MCG	450n	22m☑	0.0	5.0	3.0	.80§	40	85	A55a	DL40d	HAS
77	HM3-6512-9	64	12	S	MCG	450n	22m☑	0.0	5.0	3.0	.80§	40	85	A55a	DL20d	HAS
78	HM1-6512C-9	64	12	S	MCG	650n	22m☑	0.0	5.0	3.5	.80§	40	85	A55a	DL40d	HAS
79	HM3-6512C-9	64	12	S	MCG	650n	22m☑	0.0	5.0	3.5	.80§	40	85	A55a	DL20d	HAS
80	CDP1823D	128	8	S	MCG	200n†$	10m	0.0	10	7.0	3.0	55	125	A111	Δ015AG	RCA
81	MCM68B10L	128	8	S	MNG	250n	525m	0.0	5.0	2.0	.80§	0	70	A1	DL9b	MOTA
82	MCM68B10P	128	8	S	MNG	250n	525m	0.0	5.0	2.0	.80§	0	70	A1	DL7b	MOTA
83	CDP1823CD	128	8	S	MCG	350n†$	7.5m†	0.0	5.0	3.5	1.5	55	125	A111	Δ015AG	RCA
84	CDP1823CE	128	8	S	MCG	350n†$	7.5m†	0.0	5.0	3.5	1.5	40	85	A111	Δ015AG	RCA
85	CDP1823E	128	8	S	MCG	350n†$	7.5m†	0.0	5.0	3.5	1.5	40	85	A111	Δ015AG	RCA
86	F6810-1P	128	8	S	MNG	350n		0.0	5.0	2.0	.80	0	70	A1	DL151	FSC
87	MCM6810AP1	128	8	S	MNG	350n	400m	0.0	5.0	2.0	.80	0	70	A1	DL7b	MOTA
88#	HM468A10P	128	8	S	MNG	360n	350m	0.0	5.0	2.0	.80§	20	75	A1	DL14c	HITJ
89	MCM68A10CP	128	8	S	MNG	360n	525m	0.0	5.0	2.0	.80§	40	85	A1	DL7b	MOTA
90	MCM68A10L	128	8	S	MNG	360n	525m	0.0	5.0	2.0	.80§	0	70	A1	DL9b	MOTA
91	F6810P	128	8	S	MNG	450n		0.0	5.0	2.0	.80	0	70	A1	DL151	FSC
92#	HM46810	128	8	S	MNG	450n	350m	0.0	5.0	2.0	.80§	20	75	A1	DL81	HITJ
93#	HM46810P	128	8	S	MNG	450n	350m	0.0	5.0	2.0	.80§	20	75	A1	DL14c	HITJ
94	MCM6810ACL	128	8	S	MNG	450n	350m	0.0	5.0	2.0	.80	40	85	A1	DL9b	MOTA
95	MCM6810AL	128	8	S	MNG	450n	350m	0.0	5.0	2.0	.80	0	70	A1	DL9b	MOTA
96	MCM6810BJCS	128	8	S	MNG	450n	420m	0.0	5.0	2.0	.80§	55	125	A1	DL☑	MOTA
97	MCM6810CJCS	128	8	S	MNG	450n	420m	0.0	5.0	2.0	.80§	55	125	A1	DL☑	MOTA
98	MCM6810CP	128	8	S	MNG	450n	420m	0.0	5.0	2.0	.80§	40	85	A1	DL7b	MOTA
99	S6810-1	128	8	S	MNG	575n	650m	0.0	5.0	2.4	.40§	0	70	A1	DL3	AMI
100	MCM6810L	128	8	S	MNG	1.0u	650m	0.0	5.0	2.0	.80§	0	70	A1	DL13a	MOTA
101	S6810	128	8	S	MNG	1.0u	650m	0.0	5.0	2.4	.40§	0	70	A1	DL3	AMI
102#	MN1101	128	9	S	MCG	500n$	50m	0.0	5.0	2.4	.60	0	70			MATJ
103	MCM10144F	256	1	S	BEX	7.0n$	650m	5.2	0.0	-.81	-1.47	0	75	A78	FP10	MOTA
104	N82S116B	256	1	S	BTD	40n	575m	0.0	5.0	2.0	.85§	0	75	A7	DL4	SIC
105	N82S116F	256	1	S	BTD	40n	575m	0.0	5.0	2.0	.85§	0	75	A7	DL6	SIC
106	N82S117B	256	1	S	BTD	40n	575m	0.0	5.0	2.0	.85§	0	75	A7	DL4	SIC
107	N82S117F	256	1	S	BTD	40n	575m	0.0	5.0	2.0	.85§	0	75	A7	DL6	SIC
108	Am29720DC	256	1	S	BTD	45n$	350m	0.0	5.0	2.0	.80	0	75	A68	DL8c	AMV
109	Am29720PC	256	1	S	BTD	45n$	350m	0.0	5.0	2.0	.80	0	75	A68	DL33c	AMV
110	Am29721DC	256	1	S	BTD	45n$	350m	0.0	5.0	2.0	.80§	0	75	A68	DL8c	AMV

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

11. READ-WRITE MEMORIES (RAMS)

IN ORDER OF: (1)No. WORDS (2)BITS PER WORD (3)WORST CASE R/W CYCLE TIME &(4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZATION 1 No. WORDS	ORGANIZATION 2 BITS PER WORD	MODE	TECHN-OLOGY	3 W/C Min. Rd/Wr CYC.TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED POWER SUPPLY SPAN NEG. (V)	RATED POWER SUPPLY SPAN POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	MFR. CODE
1	Am29721PC	256	1	S	BTD	45n$	350m	0.0	5.0	2.0	.80§	0	75	A68	DL33c	AMV
2	Am29720DM	256	1	S	BTD	55n$	350m	0.0	5.0	2.0	.80	55	125	A68	DL8c	AMV
3	Am29720FM	256	1	S	BTD	55n$	350m	0.0	5.0	2.0	.80	55	125	A68	FP1a	AMV
4	Am29721DM	256	1	S	BTD	55n$	350m	0.0	5.0	2.0	.80§	55	125	A68	DL8c	AMV
5	Am29721FM	256	1	S	BTD	55n$	350m	0.0	5.0	2.0	.80§	55	125	A68	FP1a	AMV
6	SN74S201J	256	1	S	BTD	65n†	700m	0.0	5.0	2.0	.80§	0	70	A39	DL6d	TII
7	SN74S201N	256	1	S	BTD	65n†	700m	0.0	5.0	2.0	.80§	0	70	A39	DL23	TII
8	SN74S301J	256	1	S	BTD	65n†	700m	0.0	5.0	2.0	.80	0	70	A39a	DL6d	TII
9	SN74S301N	256	1	S	BTD	65n†	700m	0.0	5.0	2.0	.80	0	70	A39a	DL23	TII
10	SN54S301J	256	1	S	BTD	100n†	775m	0.0	5.0	2.0	.80	55	125	A39a	DL6d	TII
11	SN54S301W	256	1	S	BTD	100n†	775m	0.0	5.0	2.0	.80	55	125	A39a	Δ004AG	TII
12	IM6523MFE	256	1	S	MCG	250n	10m	0.0	5.0	3.0	.80	55	125	A49	FP☑	INL
13	Am9101EDC	256	4	S	MNG	200n	275m	0.0	5.0	2.0	.80	0	70	A43	DL41a	AMV
14	Am9101EPC	256	4	S	MNG	200n	275m	0.0	5.0	2.0	.80	0	70	A43	DL5a	AMV
15	Am9111EDC	256	4	S	MNG	200n	275m	0.0	5.0	2.0	.80	0	70	A45	DL19b	AMV
16	Am9111EPC	256	4	S	MNG	200n	275m	0.0	5.0	2.0	.80	0	70	A45	DL20a	AMV
17	Am9112EDC	256	4	S	MNG	200n	290m	0.0	5.0	2.0	.80	0	70	A46	DL8c	AMV
18	Am9112EPC	256	4	S	MNG	200n	290m	0.0	5.0	2.0	.80	0	70	A46	DL4a	AMV
19	HM1-6561B-2	256	4	S	MCG	230n	12.5m	0.0	5.0	2.5	1.5§	55	125	A126	DL40d	HAS
20	HM1-6561B-9	256	4	S	MCG	230n	12.5m	0.0	5.0	2.5	1.5§	40	85	A126	DL40d	HAS
21	HM3-6561B-9	256	4	S	MCG	230n	12.5m	0.0	5.0	2.5	1.5§	40	85	A126	DL20d	HAS
22	IM6551AIDF	256	4	S	MCG	245n	5.5m	0.0	11	7.7	2.2	40	85	A37	DL5b	INL
23	IM6551AMDF	256	4	S	MCG	245n	5.5m	0.0	11	7.7	2.2	55	125	A37	DL5b	INL
24	IM6561AIDN	256	4	S	MCG	245n	5.5m	0.0	11	7.7	2.2	40	85	A36	DL19a	INL
25	IM6561AIJN	256	4	S	MCG	245n	5.5m	0.0	11	7.7	2.2	40	85	A36	DL19c	INL
26	IM6561AMDN	256	4	S	MCG	245n	5.5m	0.0	11	7.7	2.2	55	125	A36	DL19a	INL
27	Am9101DDC	256	4	S	MNG	250n	275m	0.0	5.0	2.0	.80	0	70	A43	DL41a	AMV
28	Am9101DPC	256	4	S	MNG	250n	275m	0.0	5.0	2.0	.80	0	70	A43	DL5a	AMV
29	Am9111DDC	256	4	S	MNG	250n	275m	0.0	5.0	2.0	.80	0	70	A45	DL19b	AMV
30	Am9111DPC	256	4	S	MNG	250n	275m	0.0	5.0	2.0	.80	0	70	A45	DL20a	AMV
31	Am9112DDC	256	4	S	MNG	250n	290m	0.0	5.0	2.0	.80	0	70	A46	DL8c	AMV
32	Am9112DPC	256	4	S	MNG	250n	290m	0.0	5.0	2.0	.80	0	70	A46	DL4a	AMV
33	CDP1822CE	256	4	S	MCG	250n$	2.5m♦	0.0	5.0	3.5	1.5	40	85	A129	DL136	RCA
34	CDP1822D	256	4	S	MCG	250n$	10m♦	0.0	10	7.0	3.0	40	85	A129	DL21e	RCA
35	CDP1822E	256	4	S	MCG	250n$	10m♦	0.0	10	3.5	1.5	40	85	A129	DL136	RCA
36	HCMP1822D	256	4	S	MCG	250n$	5.0m†	0.0	10	7.0	3.0	55	125	A33	DL☑	HAC
37#	uPD2101ALC-2	256	4	S	MXX	250n	350m	0.0	5.0	2.0	.80	10	70	A61	DL5d	NECJ
38#	uPD2111ALC-2	256	4	S	MXX	250n	325m	0.0	5.0	2.0	.80	10	70	A60	DL20c	NECJ
39	Am91L01CDC	256	4	S	MNG	300n	170m	0.0	5.0	2.0	.80	0	70	A43	DL41a	AMV
40	Am91L01CDM	256	4	S	MNG	300n	170m	0.0	5.0	2.0	.80	55	125	A43	DL41a	AMV
41	Am91L01CPC	256	4	S	MNG	300n	170m	0.0	5.0	2.0	.80	0	70	A43	DL5a	AMV
42	Am91L11CDC	256	4	S	MNG	300n	170m	0.0	5.0	2.0	.80	0	70	A45	DL19b	AMV
43	Am91L11CDM	256	4	S	MNG	300n	170m	0.0	5.0	2.0	.80	55	125	A45	DL19b	AMV
44	Am91L11CPC	256	4	S	MNG	300n	170m	0.0	5.0	2.0	.80	0	70	A45	DL20a	AMV
45	Am91L12CDC	256	4	S	MNG	300n	175m	0.0	5.0	2.0	.80	0	70	A46	DL8c	AMV
46	Am91L12CDM	256	4	S	MNG	300n	175m	0.0	5.0	2.0	.80	55	125	A46	DL8c	AMV
47	Am91L12CPC	256	4	S	MNG	300n	175m	0.0	5.0	2.0	.80	0	70	A46	DL4a	AMV
48	Am9101CDC	256	4	S	MNG	300n	275m	0.0	5.0	2.0	.80	0	70	A43	DL41a	AMV
49	Am9101CDM	256	4	S	MNG	300n	275m	0.0	5.0	2.0	.80	55	125	A43	DL41a	AMV
50	Am9101CPC	256	4	S	MNG	300n	275m	0.0	5.0	2.0	.80	0	70	A43	DL5a	AMV
51	Am9111CDC	256	4	S	MNG	300n	275m	0.0	5.0	2.0	.80	0	70	A45	DL19b	AMV
52	Am9111CDM	256	4	S	MNG	300n	275m	0.0	5.0	2.0	.80	55	125	A45	DL19b	AMV
53	Am9111CPC	256	4	S	MNG	300n	275m	0.0	5.0	2.0	.80	0	70	A45	DL20a	AMV
54	Am9112CDC	256	4	S	MNG	300n	290m	0.0	5.0	2.0	.80	0	70	A46	DL8c	AMV
55	Am9112CDM	256	4	S	MNG	300n	290m	0.0	5.0	2.0	.80	55	125	A46	DL8c	AMV
56	Am9112CPC	256	4	S	MNG	300n	290m	0.0	5.0	2.0	.80	0	70	A46	DL4a	AMV
57	HM1-6561-2	256	4	S	MCG	310n	12.5m	0.0	5.0	2.5	1.5§	55	125	A126	DL40d	HAS
58	HM1-6561-9	256	4	S	MCG	310n	12.5m	0.0	5.0	2.5	1.5§	40	85	A126	DL40d	HAS
59	HM3-6561-9	256	4	S	MCG	310n	12.5m	0.0	5.0	2.5	1.5§	40	85	A126	DL20d	HAS
60	3538FDC	256	4	S	MNX	350n	300m	0.0	5.0	2.2	.65	0	70	A24	DL21c	FSC
61	3538FDL	256	4	S	MNX	350n	350m	0.0	5.0	2.0	.80	55	85	A24	DL21c	FSC
62	3538FDM	256	4	S	MNX	350n	350m	0.0	5.0	2.0	.80	55	125	A24	DL21c	FSC
63#	uPD2101ALC	256	4	S	MXX	350n	350m	0.0	5.0	2.0	.80	10	70	A61	DL5d	NECJ
64#	uPD2111ALC	256	4	S	MXX	350n	325m	0.0	5.0	2.0	.80	10	70	A60	DL20c	NECJ
65	Am91L01BDC	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	0	70	A43	DL41a	AMV
66	Am91L01BDM	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	55	125	A43	DL41a	AMV
67	Am91L01BFM	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	55	125	A43	FP2	AMV
68	Am91L01BPC	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	0	70	A43	DL5a	AMV
69	Am91L11BDC	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	0	70	A45	DL19b	AMV
70	Am91L11BDM	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	55	125	A45	DL19b	AMV
71	Am91L11BFM	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	55	125	A45	FP2	AMV
72	Am91L11BPC	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	0	70	A45	DL20a	AMV
73	Am91L12BDC	256	4	S	MNG	400n	175m	0.0	5.0	2.0	.80	0	70	A46	DL8c	AMV
74	Am91L12BDM	256	4	S	MNG	400n	175m	0.0	5.0	2.0	.80	55	125	A46	DL8c	AMV
75	Am91L12BFM	256	4	S	MNG	400n	175m	0.0	5.0	2.0	.80	55	125	A46	FP9	AMV
76	Am91L12BPC	256	4	S	MNG	400n	175m	0.0	5.0	2.0	.80	0	70	A46	DL4a	AMV
77	Am9101BDC	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	0	70	A43	DL41a	AMV
78	Am9101BDM	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	55	125	A43	DL41a	AMV
79	Am9101BFM	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	55	125	A43	FP2	AMV
80	Am9101BPC	256	4	S	MNG	400n	155m	0.0	5.0	2.0	.80	0	70	A43	DL5a	AMV
81	Am9111BDC	256	4	S	MNG	400n	250m	0.0	5.0	2.0	.80	0	70	A45	DL19b	AMV
82	Am9111BDM	256	4	S	MNG	400n	250m	0.0	5.0	2.0	.80	55	125	A45	DL19b	AMV
83	Am9111BFM	256	4	S	MNG	400n	250m	0.0	5.0	2.0	.80	55	125	A45	FP2	AMV
84	Am9111BPC	256	4	S	MNG	400n	250m	0.0	5.0	2.0	.80	0	70	A45	DL20a	AMV
85	Am9112BDC	256	4	S	MNG	400n	290m	0.0	5.0	2.0	.80	0	70	A46	DL8c	AMV
86	Am9112BDM	256	4	S	MNG	400n	290m	0.0	5.0	2.0	.80	55	125	A46	DL8c	AMV
87	Am9112BFM	256	4	S	MNG	400n	290m	0.0	5.0	2.0	.80	55	125	A46	FP9	AMV
88	Am9112BPC	256	4	S	MNG	400n	290m	0.0	5.0	2.0	.80	0	70	A46	DL4a	AMV
89	HM1-6561D-5	256	4	S	MCG	430n	12.5m	0.0	5.0	2.5	1.5§	0	75	A126	DL40d	HAS
90	HM3-6561D-5	256	4	S	MCG	430n	12.5m	0.0	5.0	2.5	1.5§	0	75	A126	DL20d	HAS
91	35381DC	256	4	S	MNX	450n	300m	0.0	5.0	2.2	.65	0	70	A24	DL21c	FSC
92	35381DL	256	4	S	MNX	450n	350m	0.0	5.0	2.0	.80	55	85	A24	DL21c	FSC
93	35381DM	256	4	S	MNX	450n	350m	0.0	5.0	2.0	.80	55	125	A24	DL21c	FSC
94	CDP1822CD	256	4	S	MCG	450n$	2.5m♦	0.0	5.0	3.5	1.5	40	85	A129	DL21e	RCA
95	HCMP1822CD	256	4	S	MCG	450n$	2.5m†	0.0	5.0	3.5	1.5	55	125	A33	DL☑	HAC
96#	HM435101-1	256	4	S	MCG	450n	1.0 ☑	0.0	5.0	2.2	.65§	0	70	A21	DL5e	HITJ
97#	HM435101P-1	256	4	S	MCG	450n	1.0 ☑	0.0	5.0	2.2	.65§	0	70	A21	DL5a	HITJ
98	SCM5101-1	256	4	S	MXX	450n	110m	0.0	5.0	2.0	.80§	0	70	A150		SSS
99	SR1641D	256	4	S	MNG	450n	600m	5.0	12			0	70	A14		WDC
100#	TC5501P	256	4	S	MXG	450n	75m	0.0	5.0	2.2	0.65	30	85	A142	DL194	TOSJ
101#	uPD2101ALC-4	256	4	S	MXX	450n	350m	0.0	5.0	2.0	.80	10	70	A61	DL5d	NECJ
102#	uPD2111ALC-4	256	4	S	MXX	450n	325m	0.0	5.0	2.0	.80	10	70	A60	DL20c	NECJ
103	uPD5101LC-1	256	4	S	MCG	450n	135m	0.0	5.0	2.2	.65§	0	70	A110	DL98	NECM
104	2606-1B	256	4	S	MNG	500n	400m	0.0	5.0	2.2	.65§	0	70	A2	DL4	SIC
105	Am91L01ADC	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	0	70	A43	DL41a	AMV
106	Am91L01ADM	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	55	125	A43	DL41a	AMV
107	Am91L01AFM	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	55	125	A43	FP2	AMV
108	Am91L01APC	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	0	70	A43	DL5a	AMV
109	Am91L11ADC	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	0	70	A45	DL19b	AMV
110	Am91L11ADM	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	55	125	A45	DL19b	AMV

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

11. READ-WRITE MEMORIES (RAMS)

IN ORDER OF: (1)No. WORDS (2)BITS PER WORD
(3)WORST CASE R/W CYCLE TIME &(4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZATION 1 No. WORDS	2 BITS PER WORD	MODE	TECHNOLOGY	3 W/C Min. Rd/Wr CYC.TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED POWER SUPPLY SPAN NEG. (V)	POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	OPERATING TEMP. (-)	(+)	DRAWINGS LOGIC/ BLOCK	OUTLINE Δ=MO	MFR. CODE
1	Am91L11AFM	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	55	125	A45	FP2	AMV
2	Am91L11APC	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	0	70	A45	DL20a	AMV
3	Am91L12ADC	256	4	S	MNG	500n	175m	0.0	5.0	2.0	.80	0	70	A46	DL8c	AMV
4	Am91L12ADM	256	4	S	MNG	500n	175m	0.0	5.0	2.0	.80	55	125	A46	DL8c	AMV
5	Am91L12AFM	256	4	S	MNG	500n	175m	0.0	5.0	2.0	.80	55	125	A46	FP9	AMV
6	Am91L12APC	256	4	S	MNG	500n	175m	0.0	5.0	2.0	.80	0	70	A46	DL4a	AMV
7	Am9101ADC	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	0	70	A43	DL41a	AMV
8	Am9101ADM	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	55	125	A43	DL41a	AMV
9	Am9101AFM	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	55	125	A43	FP2	AMV
10	Am9101APC	256	4	S	MNG	500n	155m	0.0	5.0	2.0	.80	0	70	A43	DL5a	AMV
11	Am9111ADC	256	4	S	MNG	500n	250m	0.0	5.0	2.0	.80	0	70	A45	DL19b	AMV
12	Am9111ADM	256	4	S	MNG	500n	250m	0.0	5.0	2.0	.80	55	125	A45	DL19b	AMV
13	Am9111AFM	256	4	S	MNG	500n	250m	0.0	5.0	2.0	.80	55	125	A45	FP2	AMV
14	Am9111APC	256	4	S	MNG	500n	250m	0.0	5.0	2.0	.80	0	70	A45	DL20a	AMV
15	Am9112ADC	256	4	S	MNG	500n	290m	0.0	5.0	2.0	.80	0	70	A46	DL8c	AMV
16	Am9112ADM	256	4	S	MNG	500n	290m	0.0	5.0	2.0	.80	55	125	A46	DL8c	AMV
17	Am9112AFM	256	4	S	MNG	500n	290m	0.0	5.0	2.0	.80	55	125	A46	FP9	AMV
18	Am9112APC	256	4	S	MNG	500n	290m	0.0	5.0	2.0	.80	0	70	A46	DL4a	AMV
19	C2101-1	256	4	S	MNG	500n	300m	0.0	5.0	2.2	.65	0	70	A43	DL41a	AMV
20	P2101-1	256	4	S	MNG	500n	300m	0.0	5.0	2.2	.65	0	70	A43	DL5a	AMV
21	35382DC	256	4	S	MNX	650n	300m	0.0	5.0	2.2	.65	0	70	A24	DL21c	FSC
22	35382DL	256	4	S	MNX	650n	350m	0.0	5.0	2.0	.80	55	85	A24	DL21c	FSC
23	35382DM	256	4	S	MNX	650n	350m	0.0	5.0	2.0	.80	55	125	A24	DL21c	FSC
24	C2101-2	256	4	S	MNG	650n	300m	0.0	5.0	2.2	.65	0	70	A43	DL41a	AMV
25	C5101	256	4	S	MCI	650n	135m	0.0	5.0	2.2	.65§	0	70	A21	DL41	ITL
26	C5101-3	256	4	S	MCI	650n	135m	0.0	5.0	2.2	.65§	0	70	A21	DL41	ITL
27	C5101L3	256	4	S	MCI	650n	135m	0.0	5.0	2.2	.65§	0	70	A21	DL41	ITL
28#	HM435101	256	4	S	MCG	650n	1.0 ☑	0.0	5.0	2.2	.65§	0	70	A21	DL5e	HITJ
29#	HM435101P	256	4	S	MCG	650n	1.0 ☑	0.0	5.0	2.2	.65§	0	70	A21	DL5a	HITJ
30#	HM435101V	256	4	S	MCG	650n	1.0 ☑	0.0	5.0	2.2	.80§	0	70	A21	DL120	HITJ
31#	HM435101VP	256	4	S	MCG	650n	1.0 ☑	0.0	5.0	2.2	.80§	0	70	A21	DL5a	HITJ
32	P2101-2	256	4	S	MNG	650n	300m	0.0	5.0	2.2	.65	0	70	A43	DL5a	AMV
33	P5101	256	4	S	MCI	650n	135m	0.0	5.0	2.2	.65§	0	70	A21	DL5a	ITL
34	P5101-3	256	4	S	MCI	650n	135m	0.0	5.0	2.2	.65§	0	70	A21	DL5a	ITL
35	P5101L3	256	4	S	MCI	650n	135m	0.0	5.0	2.2	.65§	0	70	A21	DL5a	ITL
36▼	SCM5101-1A	256	4	S	MXX	650n	110m	0.0	5.0	2.0	.80§	0	70	A150		SSS
37	SCM5101-3	256	4	S	MXX	650n	110m	0.0	5.0	2.0	.80§	0	70	A150		SSS
38#	TC5501P-1	256	4	S	MXG	650n	75m	0.0	5.0	2.2	0.65	30	85	A142	DL194	TOSJ
39	uPD5101LC	256	4	S	MCG	650n	135m	0.0	5.0	2.2	.65§	0	70	A110	DL98	NECM
40	IM6561CJN	256	4	S	MCG	730n	500u	0.0	5.0	3.0	.80	0	75	A36	DL19c	INL
41	IM6561IDN	256	4	S	MCG	730n	500u	0.0	5.0	3.0	.80	40	85	A36	DL19a	INL
42	IM6561IJN	256	4	S	MCG	730n	500u	0.0	5.0	3.0	.80	40	85	A36	DL19c	INL
43	IM6561MDN	256	4	S	MCG	730n	500u	0.0	5.0	3.0	.80	55	125	A36	DL19a	INL
44	SCM5101-8	256	4	S	MXX	800n	125m	0.0	5.0	2.0	.80§	0	70	A150		SSS
45#	uPD5101C-E	256	4	S	MCX	800n$	5m	0.0	5.0	2.2	.65	0	70	A58	DL5d	NECJ
46	C8101-2	256	4	S	MNG	850n	350m	0.0	5.0	2.2	.45§	0	70	A10	DL41	ITL
47	C8111-2	256	4	S	MNG	850n	350m	0.0	5.0	2.2	.65§	0	70	A22	DL19b	ITL
48	P8101-2	256	4	S	MNG	850n	350m	0.0	5.0	2.2	.45§	0	70	A10	DL5a	ITL
49	P8111-2	256	4	S	MNG	850n	350m	0.0	5.0	2.2	.65§	0	70	A22	DL20a	ITL
50	C2101	256	4	S	MNG	1.0u	300m	0.0	5.0	2.2	.65	0	70	A43	DL41a	AMV
51	C4101	256	4	S	MNG	1.0u	150m†	0.0	5.0		§			A10	DL41	ITL
52	P2101	256	4	S	MNG	1.0u	300m	0.0	5.0	2.2	.65	0	70	A43	DL5a	AMV
53	P4101	256	4	S	MNG	1.0u	150m†	0.0	5.0		§			A10	DL5a	ITL
54	10432	256	4	D	MPX	1.8u$	330m	12	5.0	3.5	-12.8	0	70	A29	DL44	RKW
55#	TFK10432	256	4	D	MPX	1.8u$	330m	12	5.0	3.5	-12.8	0	70	A29		ALGG
56	MC8155	256	8	S	MNG		1.5 ☑	0.5	7.0	2.0	.80	55	125	A132	DL148	ITL
57	MD8155	256	8	S	MNG		1.5 ☑	0.5	7.0	2.0	.80	55	125	A132	DL70	ITL
58	MP8155	256	8	S	MNG		1.5 ☑	0.5	7.0	2.0	.80	55	125	A132	DL140	ITL
59	C8155-2	256	8	S	MNX	330n$	1.5 ☑☑	0.5	7.0	2.0	.80	0	70	A152	DL70	ITL
60	C8156-2	256	8	S	MNX	330n$	1.5 ☑	0.5	7.0	2.0	.80	0	70	A152	DL70	ITL
61	D8155-2	256	8	S	MNX	330n$	1.5 ☑☑	0.5	7.0	2.0	.80	0	70	A152	DL148	ITL
62	D8156-2	256	8	S	MNX	330n$	1.5 ☑	0.5	7.0	2.0	.80	0	70	A152	DL148	ITL
63	P8155-2	256	8	S	MNX	330n$	1.5 ☑☑	0.5	7.0	2.0	.80	0	70	A152	DL140	ITL
64	P8156-2	256	8	S	MNX	330n$	1.5 ☑	0.5	7.0	2.0	.80	0	70	A152	DL140	ITL
65	C8155	256	8	S	MNX	400n$	1.5 ☑	0.5	7.0	2.0	.80	0	70	A152	DL70	ITL
66	C8156	256	8	S	MNX	400n$	1.5 ☑	0.5	7.0	2.0	.80	0	70	A152	DL70	ITL
67	D8155	256	8	S	MNX	400n$	1.5 ☑	0.5	7.0	2.0	.80	0	70	A152	DL148	ITL
68	D8156	256	8	S	MNX	400n$	1.5 ☑	0.5	7.0	2.0	.80	0	70	A152	DL148	ITL
69	P8155	256	8	S	MNX	400n$	1.5 ☑	0.5	7.0	2.0	.80	0	70	A152	DL140	ITL
70	P8156	256	8	S	MNX	400n$	1.5 ☑	0.5	7.0	2.0	.80	0	70	A152	DL140	ITL
71#	TMP8155P	256	8	S	MNG	400nΔ$	1.5 ☑	0.0	5.0	2.0	0.8	0	70	A153	DL208	TOSJ
72#	TMP8156P	256	8	S	MNG	400nΔ$	1.5 ☑	0.0	5.0	2.0	0.8	0	70	A153	DL208	TOSJ
73	10809	256	8	D	MPX	1.8u$	350m	12	5.0	3.5	-12.8	0	70	A27	DL44	RKW
74	10932	512	4	D	MPX	1.8u$	330m	12	5.0	3.5	-12.8	0	70	A28	DL44	RKW
75#	TFK10932	512	4	D	MPX	1.8u$	330m	12	5.0	3.5	-12.8	0	70	A20		ALGG
76	MCM10146F	1024	1	S	BEX	8.0n$	754m	5.2	0.0	-.81	-1.47	0	75	A80	FP10	MOTA
77	MCM10146L	1024	1	S	BEX	8.0n$	754m	5.2	0.0	-.81	-1.47	0	75	A80	DL76	MOTA
78	MCM93415PC	1024	1	S	BTX	35n$†	500m†							A81	DL53	MOTA
79	MCM93425DC	1024	1	S	BTX	35n$†	500m†							A82	DL76	MOTA
80	MCM93425PC	1024	1	S	BTX	35n$†	500m†							A82	DL53	MOTA
81	MCM93415DM	1024	1	S	BTX	40n	512m	0.0	5.0	2.1	.80	55	125	A81	DL76	MOTA
82	MCM93425FM	1024	1	S	BTX	40n	512m	0.0	5.0	2.1	.80§	55	125	A82	FP☑	MOTA
83	N82S10I	1024	1	S	BTX	40n	850m	0.0	5.0	2.1	.85	0	75	A5	DL8	SIC
84	N82S11I	1024	1	S	BTX	40n	850m	0.0	5.0	2.1	.85§	0	75	A5	DL8	SIC
85	S82S10I	1024	1	S	BTX	55n	850m	0.0	5.0	2.1	.80	55	125	A5	DL8	SIC
86	S82S11I	1024	1	S	BTX	55n	850m	0.0	5.0	2.1	.80§	55	125	A5	DL8	SIC
87	IM6508A-1IJE	1024	1	S	MCG	160n	1.1m	0.0	11	7.7	2.2	40	85	A17	DL33b	INL
88	IM6518A-1IJN	1024	1	S	MCG	160n	1.1m	0.0	11	7.7	2.2	40	85	A17a	DL19c	INL
89	Am9102EDC	1024	1	S	MNG	200n	250m	0.0	5.0	2.0	.80	0	70	A44	DL4a	AMV
90	Am9102EPC	1024	1	S	MNG	200n	250m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
91	CDP1821D	1024	1	S	MCG	200n†$	5.0m†	0.0	10	7.0	3.0	55	125	A32	DL52	RCA
92	HM1-6508B-2	1024	1	S	MCG	220n	12.5m	0.0	5.0	2.5	1.5§	55	125	A125	DL128	HAS
93	HM1-6508B-9	1024	1	S	MCG	220n	12.5m	0.0	5.0	2.5	1.5§	40	85	A125	DL128	HAS
94	HM1-6518B-2	1024	1	S	MCG	220n	12.5m	0.0	5.0	2.5	1.5§	55	125	A127	DL40d	HAS
95	HM1-6518B-9	1024	1	S	MCG	220n	12.5m	0.0	5.0	2.5	1.5§	40	85	A127	DL40d	HAS
96	HM3-6508B-9	1024	1	S	MCG	220n	12.5m	0.0	5.0	2.5	1.5§	40	85	A125	DL129	HAS
97	HM3-6518B-9	1024	1	S	MCG	220n	12.5m	0.0	5.0	2.5	1.5§	40	85	A127	DL20d	HAS
98	IM6508AIJE	1024	1	S	MCG	245n	5.5m	0.0	11	7.7	2.2	40	85	A17	DL33b	INL
99	IM6518AIJN	1024	1	S	MCG	245n	5.5m	0.0	11	7.7	2.2	40	85	A17a	DL19c	INL
100	Am9102DDC	1024	1	S	MNG	250n	250m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
101	Am9102DPC	1024	1	S	MNG	250n	250m	0.0	5.0	2.0	.80	0	70	A44	DL4a	AMV
102#	uPD2102ALC-2	1024	1	S	MNX	250n	350m	0.0	5.0	2.0	.80	10	70	A62	DL6g	NECJ
103	HM1-6508-2	1024	1	S	MCG	280n	12.5m	0.0	5.0	2.5	1.5§	55	125	A125	DL128	HAS
104	HM1-6508-9	1024	1	S	MCG	280n	12.5m	0.0	5.0	2.5	1.5§	40	85	A125	DL128	HAS
105	HM1-6518-2	1024	1	S	MCG	280n	12.5m	0.0	5.0	2.5	1.5§	55	125	A127	DL40d	HAS
106	HM1-6518-9	1024	1	S	MCG	280n	12.5m	0.0	5.0	2.5	1.5§	40	85	A127	DL40d	HAS
107	HM3-6508-9	1024	1	S	MCG	280n	12.5m	0.0	5.0	2.5	1.5§	40	85	A125	DL129	HAS
108	HM3-6518-9	1024	1	S	MCG	280n	12.5m	0.0	5.0	2.5	1.5§	40	85	A127	DL20d	HAS
109	Am91L02CDC	1024	1	S	MNG	300n	155m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
110	Am91L02CDM	1024	1	S	MNG	300n	155m	0.0	5.0	2.0	.80	55	125	A44	DL8c	AMV

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

11. READ-WRITE MEMORIES (RAMS)

IN ORDER OF: (1)No. WORDS (2)BITS PER WORD (3)WORST CASE R/W CYCLE TIME &(4)TYPE No.

LINE No.	[4] TYPE No.	ORGANIZATION [1] No. WORDS	[2] BITS PER WORD	MODE	TECHN-OLOGY	[3] W/C Min. Rd/Wr CYC.TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED POWER SUPPLY SPAN NEG. (V)	POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	OPERATING TEMP. (-)	(+)	DRAWINGS LOGIC/ BLOCK	OUTLINE Δ=MO	MFR. CODE
1	Am91L02CPC	1024	1	S	MNG	300n	155m	0.0	5.0	2.0	.80	0	70	A44	DL4a	AMV
2	Am9102CDC	1024	1	S	MNG	300n	250m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
3	Am9102CDM	1024	1	S	MNG	300n	250m	0.0	5.0	2.0	.80	55	125	A44	DL8c	AMV
4	Am9102CPC	1024	1	S	MNG	300n	250m	0.0	5.0	2.0	.80	0	70	A44	DL4a	AMV
5	CDP1821CD	1024	1	S	MCG	350n†$	2.5m†	0.0	5.0	3.5	1.5	55	125	A32	DL52	RCA
6	CDP1821CE	1024	1	S	MCG	350n†$	2.5m†	0.0	5.0	3.5	1.5	40	85	A32	DL52	RCA
7	CDP1821E	1024	1	S	MCG	350n†$	2.5m†	0.0	5.0	3.5	1.5	40	85	A32	DL52	RCA
8#	uPD2102ALC	1024	1	S	MNX	350n	350m	0.0	5.0	2.0	.80	10	70	A62	DL6g	NECJ
9	HM1-6508D-5	1024	1	S	MCG	380n	12.5m	0.0	5.0	2.5	1.5§	0	75	A125	DL128	HAS
10	HM1-6518D-5	1024	1	S	MCG	380n	12.5m	0.0	5.0	2.5	1.5§	0	75	A127	DL40d	HAS
11	HM3-6508D-5	1024	1	S	MCG	380n	12.5m	0.0	5.0	2.5	1.5§	0	75	A125	DL129	HAS
12	HM3-6518D-5	1024	1	S	MCG	380n	12.5m	0.0	5.0	2.5	1.5§	0	75	A127	DL20d	HAS
13	Am91L02BDC	1024	1	S	MNG	400n	140m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
14	Am91L02BDM	1024	1	S	MNG	400n	140m	0.0	5.0	2.0	.80	55	125	A44	DL8c	AMV
15	Am91L02BFM	1024	1	S	MNG	400n	140m	0.0	5.0	2.0	.80	55	125	A44	FP9	AMV
16	Am91L02BPC	1024	1	S	MNG	400n	140m	0.0	5.0	2.0	.80	0	70	A44	DL33c	AMV
17	Am9102BDC	1024	1	S	MNG	400n	250m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
18	Am9102BDM	1024	1	S	MNG	400n	275m	0.0	5.0	2.0	.80	55	125	A44	DL8c	AMV
19	Am9102BFM	1024	1	S	MNG	400n	275m	0.0	5.0	2.0	.80	55	125	A44	FP1a	AMV
20	Am9102BPC	1024	1	S	MNG	400n	250m	0.0	5.0	2.0	.80	0	70	A44	DL33c	AMV
21	21021DC	1024	1	S	MNX	450n	250m	0.0	5.0	2.2	.65	0	70	A23	DL6b	FSC
22	21021DL	1024	1	S	MNX	450n	350m	0.0	5.0	2.0	.80	55	85	A23	DL6b	FSC
23	21021DM	1024	1	S	MNX	450n	350m	0.0	5.0	2.0	.80	55	125	A23	DL6b	FSC
24	C8102A4	1024	1	S	MNG	450n	350m	0.0	5.0	2.0	.80§	0	70	A8	DL39	ITL
25	P8102A4	1024	1	S	MNG	450n	350m	0.0	5.0	2.0	.80§	0	70	A8	DL33	ITL
26#	uPD2102ALC-4	1024	1	S	MNX	450n	350m	0.0	5.0	2.0	.80	10	70	A62	DL6g	NECJ
27	Am91L02ADC	1024	1	S	MNG	500n	140m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
28	Am91L02ADM	1024	1	S	MNG	500n	140m	0.0	5.0	2.0	.80	55	125	A44	DL8c	AMV
29	Am91L02AFM	1024	1	S	MNG	500n	140m	0.0	5.0	2.0	.80	55	125	A44	FP9	AMV
30	Am91L02APC	1024	1	S	MNG	500n	140m	0.0	5.0	2.0	.80	0	70	A44	DL4a	AMV
31	Am9102ADC	1024	1	S	MNG	500n	225m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
32	Am9102ADM	1024	1	S	MNG	500n	225m	0.0	5.0	2.0	.80	55	125	A44	DL8c	AMV
33	Am9102AFM	1024	1	S	MNG	500n	225m	0.0	5.0	2.0	.80	55	125	A44	FP9	AMV
34	Am9102APC	1024	1	S	MNG	500n	225m	0.0	5.0	2.0	.80	0	70	A44	DL4a	AMV
35	IM6508-1IJE	1024	1	S	MCG	500n	50u	0.0	5.0	3.0	.80	40	85	A17	DL33b	INL
36	IM6518-1IJN	1024	1	S	MCG	500n	50u	0.0	5.0	3.0	.80	40	85	A17a	DL19c	INL
37	21022DC	1024	1	S	MNX	650n	250m	0.0	5.0	2.2	.65	0	70	A23	DL6b	FSC
38	21022DL	1024	1	S	MNX	650n	350m	0.0	5.0	2.0	.80	55	85	A23	DL6b	FSC
39	21022DM	1024	1	S	MNX	650n	350m	0.0	5.0	2.0	.80	55	125	A23	DL6b	FSC
40	Am91L02DC	1024	1	S	MNG	650n	155m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
41	Am91L02DM	1024	1	S	MNG	650n	155m	0.0	5.0	2.0	.80	55	125	A44	DL8c	AMV
42	Am91L02FM	1024	1	S	MNG	650n	155m	0.0	5.0	2.0	.80	55	125	A44	FP9	AMV
43	Am91L02PC	1024	1	S	MNG	650n	155m	0.0	5.0	2.0	.80	0	70	A44	DL4a	AMV
44	Am9102DC	1024	1	S	MNG	650n	250m	0.0	5.0	2.0	.80	0	70	A44	DL8c	AMV
45	Am9102DM	1024	1	S	MNG	650n	250m	0.0	5.0	2.0	.80	55	125	A44	DL8c	AMV
46	Am9102FM	1024	1	S	MNG	650n	250m	0.0	5.0	2.0	.80	55	125	A44	FP9	AMV
47	Am9102PC	1024	1	S	MNG	650n	250m	0.0	5.0	2.0	.80	0	70	A44	DL4a	AMV
48	IM6508CJE	1024	1	S	MCG	760n	500u	0.0	5.0	3.0	.80	0	75	A17	DL33b	INL
49	IM6508IJE	1024	1	S	MCG	760n	500u	0.0	5.0	3.0	.80	40	85	A17	DL33b	INL
50	IM6518CJN	1024	1	S	MCG	760n	500u	0.0	5.0	3.0	.80	0	75	A17a	DL19c	INL
51	IM6518IJN	1024	1	S	MCG	760n	500u	0.0	5.0	3.0	.80	40	85	A17a	DL19c	INL
52	C8102-2	1024	1	S	MNG	850n	350m	0.0	5.0	2.2	.65§	0	70	A8	DL39	ITL
53	P8102-2	1024	1	S	MNG	850n	350m	0.0	5.0	2.2	.65§	0	70	A8	DL33	ITL
54	MM1-RAM	1024	4	S	MNG		1.5	0.0	5.0	2.0	.80			A83	MD3	CLI
55	TMS4245JL	1024	4	S	MNG	120n	350m	0.0	5.0	2.4	.40	0	70			TII
56	TMS4245NL	1024	4	S	MNG	120n	350m	0.0	5.0	2.4	.40	0	70			TII
57	uPD2114LD-5	1024	4	S		150n	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
58	Am9131EDC	1024	4	S	MNG	200n	578m	0.0	5.0	2.0	.80	0	70	A95	DL41a	AMV
59#	HM472114AP-2	1024	4	S	MNG	200n	1.0 ☑	0.0	5.0	2.0	.80§	0	70	A123	DL121	HITJ
60	MCM2114P	1024	4	S	MNG	200n	400m†	0.0	5.0		§	0	70	A76	DL☑	MOTA
61#	TMM314AP-1	1024	4	S	MNG	200n	850m	0.0	5.0	2.0	0.8	0	70	A147	DL195	TOSJ
62#	TMM314APL-1	1024	4	S	MNG	200n	850m	0.0	5.0	2.0	0.8	0	70	A147	DL195	TOSJ
63	uPD2114LC-3	1024	4	S	MNG	200n	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
64	uPD2114LD-3	1024	4	S	MNG	200n	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
65	Am91L31ADC	1024	4	S	MNG	250n	368m	0.0	5.0	2.0	.80	0	70	A95	DL41a	AMV
66	Am91L31DDC	1024	4	S	MNG	250n	368m	0.0	5.0	2.0	.80	0	70	A95	DL41a	AMV
67	Am9131DDC	1024	4	S	MNG	250n	578m	0.0	5.0	2.0	.80	0	70	A95	DL41a	AMV
68	uPD2114LC-2	1024	4	S	MNG	250n	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
69	uPD2114LD-2	1024	4	S	MNG	250n	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
70	Am91L31CDC	1024	4	S	MNG	300n	368m	0.0	5.0	2.0	.80	0	70	A95	DL41a	AMV
71	Am91L31CDM	1024	4	S	MNG	300n	368m	0.0	5.0	2.0	.80	55	125	A95	DL41a	AMV
72	Am9131CDC	1024	4	S	MNG	300n	578m	0.0	5.0	2.0	.80	0	70	A95	DL41a	AMV
73	Am9131CDM	1024	4	S	MNG	300n	578m	0.0	5.0	2.0	.80	55	125	A95	DL41a	AMV
74#	HM472114-3	1024	4	S	MNG	300n	1.0 ☑	0.0	5.0	2.0	.80§	0	70	A86	DL40b	HITJ
75#	HM472114P-3	1024	4	S	MNG	300n	1.0 ☑	0.0	5.0	2.0	.80§	0	70	A86	DL121	HITJ
76	uPD2114LC-1	1024	4	S	MNG	300n	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
77	uPD2114LD-1	1024	4	S	MNG	300n	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
78	Am9130EDC	1024	4	S	MNG	320n	578m	0.0	5.0	2.0	.80	0	70	A47	DL41a	AMV
79	CDP1825D	1024	4	S	MCG	350n$	20m	0.0	10	7.0	3.0§	55	125	A118	DL25	RCA
80	Am91L30DDC	1024	4	S	MNG	395n	368m	0.0	5.0	2.0	.80	0	70	A47	DL41a	AMV
81	Am9130DDC	1024	4	S	MNG	395n	578m	0.0	5.0	2.0	.80	0	70	A47	DL41a	AMV
82	Am91L31BDC	1024	4	S	MNG	400n	368m	0.0	5.0	2.0	.80	0	70	A95	DL41a	AMV
83	Am91L31BDM	1024	4	S	MNG	400n	368m	0.0	5.0	2.0	.80	55	125	A95	DL41a	AMV
84	Am9131BDC	1024	4	S	MNG	400n	578m	0.0	5.0	2.0	.80	0	70	A95	DL41a	AMV
85	Am9131BDM	1024	4	S	MNG	400n	578m	0.0	5.0	2.0	.80	55	125	A95	DL41a	AMV
86#	HM472114-4	1024	4	S	MNG	450n	1.0 ☑	0.0	5.0	2.0	.80§	0	70	A86	DL40b	HITJ
87#	HM472114P-4	1024	4	S	MNG	450n	1.0 ☑	0.0	5.0	2.0	.80§	0	70	A86	DL121	HITJ
88	MCS2114-45	1024	4	S		450n	500m	0	5.0	10	4.0	0	70	A138	DL187	MTY
89	MCS2114L-45	1024	4	S		450n	350m	0	5.0	10	4.0	0	70	A138	DL187	MTY
90	MCT2114-45	1024	4	S		450n	500m	0	5.0	10	4.0	0	70	A138	DL187	MTY
91	MCT2114L-45	1024	4	S		450n	350m	0	5.0	10	4.0	0	70	A138	DL187	MTY
92	MPS2114-45	1024	4	S		450n	500m	0	5.0	10	4.0	0	70	A138	DL187	MTY
93	MPS2114L-45	1024	4	S		450n	350m	0	5.0	10	4.0	0	70	A138	DL187	MTY
94	MPT2114-45	1024	4	S		450n	500m	0	5.0	10	4.0	0	70	A138	DL187	MTY
95	MPT2114L-45	1024	4	S		450n	350m	0	5.0	10	4.0	0	70	A138	DL187	MTY
96	SCM5102-1	1024	4	S	MXX	450n	110m	0.0	5.0	2.0	.80§	0	70	A151		SSS
97#	TMM314AP	1024	4	S	MNG	450n	850m	0.0	5.0	2.0	0.8	0	70	A147	DL195	TOSJ
98#	TMM314APL	1024	4	S	MNG	450n	850m	0.0	5.0	2.0	0.8	0	70	A147	DL195	TOSJ
99	uPD445LC-1	1024	4	S	MCX	450n	150m	0.0	5.0	2.2	.65	10	70	A128	DL☑	NECM
100	uPD2114LC	1024	4	S	MNG	450n	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
101	uPD2114LD	1024	4	S	MNG	450n	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
102	MK4114	1024	4	S	MNX	460n	120m		5	2.0	.80	0	70			MOS
103	Am91L30CDC	1024	4	S	MNG	470n	368m	0.0	5.0	2.0	.80	0	70	A47	DL41a	AMV
104	Am91L30CDM	1024	4	S	MNG	470n	368m	0.0	5.0	2.0	.80	55	125	A47	DL41a	AMV
105	Am9130CDC	1024	4	S	MNG	470n	578m	0.0	5.0	2.0	.80	0	70	A47	DL41a	AMV
106	Am9130CDM	1024	4	S	MNG	470n	578m	0.0	5.0	2.0	.80	55	125	A47	DL41a	AMV
107	HM6533-2	1024	4	S	MCG	475n†	35m	0.0	5.0	2.5	1.5§	55	125	A120	DL☑	HAS
108	HM6533-9	1024	4	S	MCG	475n†	35m	0.0	5.0	2.5	1.5§	40	85	A120	DL☑	HAS
109	Am91L31ADM	1024	4	S	MNG	500n	368m	0.0	5.0	2.0	.80	55	125	A95	DL41a	AMV
110	Am9131ADC	1024	4	S	MNG	500n	578m	0.0	5.0	2.0	.80	0	70	A95	DL41a	AMV

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

11. READ-WRITE MEMORIES (RAMS)

IN ORDER OF: (1)No. WORDS (2)BITS PER WORD (3)WORST CASE R/W CYCLE TIME &(4)TYPE No.

LINE No.	[4] TYPE No.	ORGANIZATION [1] No. WORDS	[2] BITS PER WORD	MODE	TECHNOLOGY	[3] W/C Min. Rd/Wr CYC.TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED POWER SUPPLY SPAN NEG. (V)	POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	OPERATING TEMP. (-)	(+)	DRAWINGS LOGIC/ BLOCK	OUTLINE Δ=MO	MFR. CODE
1	Am9131ADM	1024	4	S	MNG	500n	578m	0.0	5.0	2.0	.80	55	125	A95	DL41a	AMV
2#	TC5047AP-1	1024	4	S	MXG	500n	100m	0.0	5.0	3.0	0.6	30	85	A141	DL193	TOSJ
3	Am91L30BDC	1024	4	S	MNG	620n	368m	0.0	5.0	2.0	.80	0	70	A47	DL41a	AMV
4	Am91L30BDM	1024	4	S	MNG	620n	368m	0.0	5.0	2.0	.80	55	125	A47	DL41a	AMV
5	Am9130BDC	1024	4	S	MNG	620n	578m	0.0	5.0	2.0	.80	0	70	A47	DL41a	AMV
6	Am9130BDM	1024	4	S	MNG	620n	578m	0.0	5.0	2.0	.80	55	125	A47	DL41a	AMV
7	HM6533C-9	1024	4	S	MCG	650n	35m	0.0	5.0	2.5	1.5§	40	85	A120	DL☑	HAS
8▼	SCM5102-1A	1024	4	S	MXX	650n	110m	0.0	5.0	2.0	.80§	0	70	A151		SSS
9	SCM5102-3	1024	4	S	MXX	650n	110m	0.0	5.0	2.0	.80§	0	70	A151		SSS
10	uPD445LC	1024	4	S	MCX	650n	150m	0.0	5.0	2.2	.65	10	70	A128	DL☑	NECM
11	Am91L30ADC	1024	4	S	MNG	770n	368m	0.0	5.0	2.0	.80	0	70	A47	DL41a	AMV
12	Am91L30ADM	1024	4	S	MNG	770n	368m	0.0	5.0	2.0	.80	55	125	A47	DL41a	AMV
13	Am9130ADC	1024	4	S	MNG	770n	578m	0.0	5.0	2.0	.80	0	70	A47	DL41a	AMV
14	Am9130ADM	1024	4	S	MNG	770n	578m	0.0	5.0	2.0	.80	55	125	A47	DL41a	AMV
15	SCM5102-8	1024	4	S	MXX	800n	125m	0.0	5.0	2.0	.80§	0	70	A151		SSS
16#	TC5047AP-2	1024	4	S	MXG	800n	100m	0.0	5.0	3.0	0.6	30	85	A141	DL193	TOSJ
17	uPD2114LC-5	1024	4	S		150m	357m	0.0	5.0	2.0	.80§	10	80	A104	DL96	NECM
18	IC8185	1024	8	S	MNG		1.5 ☑	0.5	7.0	2.0	.80	40	85	A132	DL144	ITL
19	ID8185	1024	8	S	MNG		1.5 ☑	0.5	7.0	2.0	.80	40	85	A132	DL145	ITL
20	IP8185	1024	8	S	MNG		1.5 ☑	0.5	7.0	2.0	.80	40	85	A132	DL182	ITL
21	P8185	1024	8	S	MNG		1.5 ☑	0.5	7.0	2.0	.80	0	70	A132	DL207	ITL
22	uPD421	1024	8	S	MNG	85n$		0.0	5.0	2.0	.80§			A136	DL☑	NECM
23	C8185-2	1024	8	S	MNG	200n$	500m	0.0	5.0	2.0	.80	0	70	A132	DL144	ITL
24	D8185-2	1024	8	S	MNG	200n$	500m	0.0	5.0	2.0	.80	0	70	A132	DL145	ITL
25	P8185-2	1024	8	S	MNG	200n$	500m	0.0	5.0	2.0	.80	0	70	A132	DL182	ITL
26	9010-1231	1024	8		MNX	250n$	3.6	0.0	5.0			0	60		MD2c	WSC
27	C8185	1024	8	S	MNG	300n$	500m	0.0	5.0	2.0	.80	0	70	A132	DL144	ITL
28	D8185	1024	8	S	MNG	300n$	500m	0.0	5.0	2.0	.80	0	70	A132	DL145	ITL
29	9010-1210	1024	8		MNX	500n$	3.7	0.0	5.0			0	60		MD2c	WSC
30	9010-1250	1024	8		MNX	500n$	1.8	0.0	24			0	60		MD2c	WSC
31	IC8155	2056	8	S		400n$	1.5 ☑	0.5	7.0	2.0	.80	40	85	A152	DL70	ITL
32	IC8156	2056	8	S		400n$	1.5 ☑	0.5	7.0	2.0	.80	40	85	A152	DL70	ITL
33	ID8155	2056	8	S		400n$	1.5 ☑	0.5	7.0	2.0	.80	40	85	A152	DL148	ITL
34	ID8156	2056	8	S		400n$	1.5 ☑	0.5	7.0	2.0	.80	40	85	A152	DL148	ITL
35	IP8155	2056	8	S		400n$	1.5 ☑	0.5	7.0	2.0	.80	40	85	A152	DL140	ITL
36	IP8156	2056	8	S		400n$	1.5 ☑	0.5	7.0	2.0	.80	40	85	A152	DL140	ITL
37	TDM-SCA0216H	2096	16	S	MCX	350n$	1.8	0.0	5.0	2.0	.80	55	85			TSC
38#	HM4847-2	4096	1	S	MNX	45n	850m	0.0	5.0	2.0	.80§	0	70	A122	DL40b	HITJ
39#	HM4847-3	4096	1	S	MNX	55n	800m	0.0	5.0	2.0	.80§	0	70	A122	DL40b	HITJ
40	TMS2147-5JDL	4096	1		MNG	55n	990m	0.0	5.0	2.0	.80	0	70			TII
41	TMS2147-5NL	4096	1		MNG	55n	990m	0.0	5.0	2.0	.80	0	70			TII
42	uPD2147D-3	4096	1	S	MXX	55n$	900m	0.0	5.0	2.0	.80§			A92	DL96	NECM
43#	HM6147	4096	1	S	MCX	70n	1.0 ☑	0.0	5.0	2.4	.80§	0	70		DL☑	HITJ
44	TMS21L47-7JDL	4096	1		MNG	70n	770m	0.0	5.0	2.0	.80	0	70			TII
45	TMS21L47-7JL	4096	1		MNG	70n	770m	0.0	5.0	2.0	.80	0	70			TII
46	TMS21L47-7NL	4096	1		MNG	70n	770m	0.0	5.0	2.0	.80	0	70			TII
47	TMS2147-7JDL	4096	1		MNG	70n	880m	0.0	5.0	2.0	.80	0	70			TII
48	TMS2147-7JL	4096	1		MNG	70n	880m	0.0	5.0	2.0	.80	0	70			TII
49	TMS2147-7NL	4096	1		MNG	70n	880m	0.0	5.0	2.0	.80	0	70			TII
50	uPD2147D-2	4096	1	S	MXX	70n$	800m	0.0	5.0	2.0	.80§			A92	DL96	NECM
51	uPD2147D	4096	1	S	MXX	85n$	800m	0.0	5.0	2.0	.80§			A92	DL96	NECM
52	TMS2147-9JDL	4096	1		MNG	90n	990m	0.0	5.0	2.0	.80	0	70			TII
53	TMS2147-9JL	4096	1		MNG	90n	990m	0.0	5.0	2.0	.80	0	70			TII
54	TMS2147-9NL	4096	1		MNG	90n	990m	0.0	5.0	2.0	.80	0	70	TII		TII
55	TMS4244JL	4096	1	S	MNG	120n	300m	0.0	5.0	2.0	.80	0	70			TII
56	TMS4244NL	4096	1	S	MNG	120n	300m	0.0	5.0	2.0	.80	0	70			TII
57#	MN1002	4096	1	D	MNG	200n$	400m	5.0	12	2.4	.60	0	70			MATJ
58	TMS4164-10JDL	4096	1		MNG	200n	250m	0.0	5.0	2.4	.80	0	70			TII
59#	uPD410D2	4096	1	S	MNG	220n	470m†	5.0	12	2.4	.60§	0	70	A57	DL5c	NECJ
60	uPD410D3	4096	1	S	MNG	220n	470m†	5.0	12	2.4	.60§	0	70	A57	DL97	NECM
61▼#	uPD410D-2	4096	1	S	MNG	220n	470m†	5.0	12	2.4	.60§	0	70	A57	DL5c	NECJ
62▼#	uPD410D-3	4096	1	S	MNG	220n	470m†	5.0	12	2.4	.60§	0	70	A57	DL97	NECJ
63#	HM4710	4096	1	D	MNX	230n	600m	5.2	12						DL☑	HITJ
64	uPD4104C-3	4096	1	S	MNX	230n	220m	0.0	5.0	2.2	.80	0	70	A135	DL96	NECM
65	uPD4104D-3	4096	1	S	MNX	230n	220m	0.0	5.0	2.2	.80	0	70	A135	DL96	NECM
66	TMS4164-12JDL	4096	1		MNG	250n	200m	0.0	5.0	2.4	.80	0	70			TII
67	uPD4104C-2	4096	1	S	MNX	260n	220m	0.0	5.0	2.2	.80	0	70	A135	DL96	NECM
68	uPD4104D-2	4096	1	S	MNX	260n	220m	0.0	5.0	2.2	.80	0	70	A135	DL96	NECM
69#	HM4711-1	4096	1	D	MNG	290n	720m	5.0	12	2.4	.80§	0	70	A85	DL5e	HITJ
70	MCM6605AL1	4096	1	D	MNG	290n	335m†	5.0	12	3.0	.80§	0	70	A30	DL21d	MOTA
71	MCM6605AP1	4096	1	D	MNG	290n	335m†	5.0	12	3.0	.80§	0	70	A30	DL54	MOTA
72	MK4104-3	4096	1	S	MNX	310n	120m		5	2.0	.80	0	70			MOS
73	MKB4104J4	4096	1	S	MNX	310n	120n	0.0	5.0	2.0	.80	0	70			MOS
74	MKB4104J5	4096	1	S	MNX	310n	120n	0.0	5.0	2.0	.80	0	70			MOS
75	MKB4104J6	4096	1	S	MNX	310n	120n	0.0	5.0	2.0	.80	0	70			MOS
76	MKB4104J85	4096	1	S	MNX	310n	120n	0.0	5.0	2.0	.80	55	125			MOS
77	MKB4104J86	4096	1	S	MNX	310n	120n	0.0	5.0	2.0	.80	55	125			MOS
78	uPD4104C-1	4096	1	S	MNX	310n	115m	0.0	5.0	2.2	.80	0	70	A135	DL96	NECM
79	uPD4104D-1	4096	1	S	MNX	310n	115m	0.0	5.0	2.2	.80	0	70	A135	DL96	NECM
80	Am9140EDC	4096	1	S	MNG	320n	578m	0.0	5.0	2.0	.80	0	70	A48	DL41a	AMV
81	Am9141BDM	4096	1	S	MNG	320n	578m	0.0	5.0	2.0	.80	55	125	A96	DL41a	AMV
82#	HM4704L-2	4096	1	D	MNX	320n	462m	5.0	12						DL☑	HITJ
83#	HM4711-2	4096	1	D	MNG	320n	720m	5.0	12	2.4	.80§	0	70	A85	DL5e	HITJ
84	MK4027-2	4096	1	D	MNX	320n	462m	5.0	12	2.2	.80	0	70			MOS
85#	uPD410D1	4096	1	S	MNG	330n	470m†	5.0	12	2.4	.60§	0	70	A57	DL5c	NECJ
86▼#	uPD410D-1	4096	1	S	MNG	330n	470m†	5.0	12	2.4	.60§	0	70	A57	DL5c	NECJ
87	Z6104-3CS	4096	1	S	MNG	340n	385m†	0.0	5.0	2.0	.80	0	70	A89	DL25b	ZIL
88#	HM4704L-3	4096	1	D	MNX	375n	392m	5.0	12						DL☑	HITJ
89#	HM4704L-4	4096	1	D	MNX	375n	392m	5.0	12						DL☑	HITJ
90	MCM6604L2	4096	1	D	MNG	375n	630m	5.0	12	2.4	.80§	0	70	A31	DL53	MOTA
91	MCM6604P2	4096	1	D	MNG	375n	630m	5.0	12	2.4	.80§	0	70	A31	DL6c	MOTA
92	MK4027-3	4096	1	D	MNX	375n	462m	5.0	12	2.2	.80	0	70			MOS
93	MK4027-4	4096	1	D	MNX	375n	462m	5.0	12	2.2	.80	0	70			MOS
94	MK4096-6	4096	1	D	MNX	375n	450m	5.0	12	2.4	.80	0	70			MOS
95	MK4096-77	4096	1	D	MNX	375n	570m	5.0	12	2.4	.80	55	85			MOS
96	MKB4027F84	4096	1	D	MNX	375n	462m	5.0	12	2.2	.80	55	85			MOS
97	MKB4027J2	4096	1	D	MNX	375n	462m	5.0	12	2.2	.80	0	70			MOS
98	MKB4027J3	4096	1	D	MNX	375n	462m	5.0	12	2.2	.80	0	70			MOS
99	MKB4027J4	4096	1	D	MNX	375n	462m	5.0	12	2.2	.80	0	70			MOS
100	MKB4027J83	4096	1	D	MNX	375n	462m	5.0	12	2.2	.80	55	85			MOS
101	MKB4027J84	4096	1	D	MNX	375n	462m	5.0	12	2.2	.80	55	85			MOS
102#	HM4711-3	4096	1	D	MNG	380n	720m	5.0	12	2.4	.80§	0	70	A85	DL5e	HITJ
103#	uPD411D-3	4096	1	D	MNX	380n	500m†	5.0	12	2.4	.60§	0	70	A59	DL5c	NECJ
104	MK4104-4	4096	1	S	MNX	385n	120m		5	2.0	.80	0	70			MOS
105	Am91L40DDC	4096	1	S	MNG	395n	368m	0.0	5.0	2.0	.80	0	70	A48	DL41a	AMV
106	Am91L41DDC	4096	1	S	MNG	395n	368m	0.0	5.0	2.0	.80	0	70	A96	DL41a	AMV
107	Am9140DDC	4096	1	S	MNG	395n	578m	0.0	5.0	2.0	.80	0	70	A48	DL41a	AMV
108	Am9141CDM	4096	1	S	MNG	395n	578m	0.0	5.0	2.0	.80	55	125	A96	DL41a	AMV
109	Am9050EDC	4096	1	D	MNG	400n	750m	5.0	12	2.4	.80	0	70	A50	DL19b	AMV
110	Am9050EPC	4096	1	D	MNG	400n	750m	5.0	12	2.4	.80	0	70	A50	DL20a	AMV

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

11. READ-WRITE MEMORIES (RAMS)

IN ORDER OF: (1)No. WORDS (2)BITS PER WORD (3)WORST CASE R/W CYCLE TIME &(4)TYPE No.

LINE No.	[4] TYPE No.	ORGANIZATION [1] No. WORDS	[2] BITS PER WORD	MODE	TECHN-OLOGY	[3] W/C Min. Rd/Wr CYC.TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED POWER SUPPLY SPAN NEG. (V)	POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	OPERATING TEMP. (-)	(+)	DRAWINGS LOGIC/ BLOCK	OUTLINE Δ=MO	MFR. CODE
1	Am9060EDC	4096	1	D	MNG	400n	750m	5.0	12	2.4	.80	0	70	A42	DL41a	AMV
2	Am9060EPC	4096	1	D	MNG	400n	750m	5.0	12	2.4	.80	0	70	A42	DL5a	AMV
3	uPD411AC-2	4096	1	D	MNX	400n	460m†	5.0	12	2.4	.60§	0	70	A106	DL98	NECM
4#	uPD411D-2	4096	1	D	MNX	400n	450m†	5.0	12	2.4	.60§	0	70	A59	DL5c	NECJ
5	MCM6604L4	4096	1	D	MNG	425n	630m	5.0	12	2.4	.80§	0	70	A31	DL6c	MOTA
6	MCM6604P4	4096	1	D	MNG	425n	630m	5.0	12	2.4	.80§	0	70	A31	DL53	MOTA
7	MK4096-16	4096	1	D	MNX	425n	385m	5.0	12	2.4	.80	0	70			MOS
8	MK4096-86	4096	1	D	MNX	425n	500m	5.0	12	2.4	.80	55	85			MOS
9	Am9050DDC	4096	1	D	MNG	430n	750m	5.0	12	2.4	.80	0	70	A50	DL19b	AMV
10	Am9050DPC	4096	1	D	MNG	430n	750m	5.0	12	2.4	.80	0	70	A50	DL20a	AMV
11	Am9060DDC	4096	1	D	MNG	430n	750m	5.0	12	2.4	.80	0	70	A42	DL41a	AMV
12	Am9060DPC	4096	1	D	MNG	430n	750m	5.0	12	2.4	.80	0	70	A42	DL5a	AMV
13	uPD411AC-1	4096	1	D	MNX	430n	460m†	5.0	12	2.4	.60§	0	70	A106	DL98	NECM
14#	uPD411D-1	4096	1	D	MNX	430n	450m†	5.0	12	2.4	.60§	0	70	A59	DL5c	NECJ
15#	uPD410D	4096	1	S	MNG	440n	470m†	5.0	12	2.4	.60§	0	70	A57	DL5c	NECJ
16	Z6104-5CS	4096	1	S	MNG	440n	220m†	0.0	5.0	2.0	.80	0	70	A89	DL25b	ZIL
17	Z6104-5PS	4096	1	S	MNG	440n	220m†	0.0	5.0	2.0	.80	0	70	A89	DL25b	ZIL
18	MK4104-5	4096	1	S	MNX	460n	120m		5	2.0	.80	0	70			MOS
19	uPD4104C	4096	1	S	MNX	460n	115m	0.0	5.0	2.2	.80	0	70	A135	DL96	NECM
20	uPD4104D	4096	1	S	MNX	460n	115m	0.0	5.0	2.2	.80	0	70	A135	DL96	NECM
21	Am91L40CDC	4096	1	S	MNG	470n	368m	0.0	5.0	2.0	.80	0	70	A48	DL41a	AMV
22	Am91L40CDM	4096	1	S	MNG	470n	368m	0.0	5.0	2.0	.80	55	125	A48	DL41a	AMV
23	Am91L41CDC	4096	1	S	MNG	470n	368m	0.0	5.0	2.0	.80	0	70	A96	DL41a	AMV
24	Am91L41CDM	4096	1	S	MNG	470n	368m	0.0	5.0	2.0	.80	55	125	A96	DL41a	AMV
25	Am9050CDC	4096	1	D	MNG	470n	750m	5.0	12	2.4	.80	0	70	A50	DL19b	AMV
26	Am9050CPC	4096	1	D	MNG	470n	750m	5.0	12	2.4	.80	0	70	A50	DL20a	AMV
27	Am9060CDC	4096	1	D	MNG	470n	750m	5.0	12	2.4	.80	0	70	A42	DL41a	AMV
28	Am9060CPC	4096	1	D	MNG	470n	750m	5.0	12	2.4	.80	0	70	A42	DL5a	AMV
29	Am9140CDC	4096	1	S	MNG	470n	578m	0.0	5.0	2.0	.80	0	70	A48	DL41a	AMV
30	Am9140CDM	4096	1	S	MNG	470n	578m	0.0	5.0	2.0	.80	55	125	A48	DL41a	AMV
31	Am9141ADM	4096	1	S	MNG	470n	578m	0.0	5.0	2.0	.80	55	125	A96	DL41a	AMV
32	Am9141EDC	4096	1	S	MNG	470n	578m	0.0	5.0	2.0	.80	0	70	A96	DL41a	AMV
33	C8107B4	4096	1	D	MNG	470n	1.2	5.0	12	2.4	.60§	0	70	A3	DL41	ITL
34	MCM6605AL	4096	1	D	MNG	470n	335m†	5.0	12	3.0	.80§	0	70	A30	DL21d	MOTA
35	MCM6605AP	4096	1	D	MNG	470n	335m†	5.0	12	3.0	.80§	0	70	A30	DL54	MOTA
36	P8107B4	4096	1	D	MNG	470n	1.2	5.0	12	2.4	.60§	0	70	A3	DL5a	ITL
37	uPD411AC	4096	1	D	MNX	470n	460m†	5.0	12	2.4	.60§	0	70	A106	DL98	NECM
38#	uPD411D	4096	1	D	MNX	470n	450m†	5.0	12	2.4	.60§	0	70	A59	DL5c	NECJ
39	HM6543-2	4096	1	S	MCG	475n†	35m	0.0	5.0	2.5	1.5§	55	125	A121	DL☑	HAS
40	HM6543-9	4096	1	S	MCG	475n†	35m	0.0	5.0	2.5	1.5§	40	85	A121	DL☑	HAS
41	mN606	4096	1	D	MNG	490n	280m	4.25	14	4.0	.80	0	70	A87	DL17b	DGC
42	MCM6604L	4096	1	D	MNG	500n	630m	5.0	12	2.4	.80§	0	70	A31	DL6c	MOTA
43	MCM6604P	4096	1	D	MNG	500n	630m	5.0	12	2.4	.80§	0	70	A31	DL53	MOTA
44	MK4096-11	4096	1	D	MNX	500n	320m	5.0	12	2.4	.80	0	70			MOS
45	MK4096-85	4096	1	D	MNX	500n	450m	5.0	12	2.4	.80	55	85			MOS
46	Z6104-6CS	4096	1	S	MNG	510n	200m	0.0	5.0	2.0	.80	0	70	A89	DL25b	ZIL
47	HM6543C-9	4096	1	S	MCG	560n	35m	0.0	5.0	2.5	1.5§	40	85	A121	DL☑	HAS
48	Am91L40BDC	4096	1	S	MNG	620n	368m	0.0	5.0	2.0	.80	0	70	A48	DL41a	AMV
49	Am91L40BDM	4096	1	S	MNG	620n	368m	0.0	5.0	2.0	.80	55	125	A48	DL41a	AMV
50	Am91L41BDC	4096	1	S	MNG	620n	368m	0.0	5.0	2.0	.80	0	70	A96	DL41a	AMV
51	Am91L41BDM	4096	1	S	MNG	620n	368m	0.0	5.0	2.0	.80	55	125	A96	DL41a	AMV
52	Am9140BDC	4096	1	S	MNG	620n	578m	0.0	5.0	2.0	.80	0	70	A48	DL41a	AMV
53	Am9140BDM	4096	1	S	MNG	620n	578m	0.0	5.0	2.0	.80	55	125	A48	DL41a	AMV
54	Am9141CDC	4096	1	S	MNG	620n	578m	0.0	5.0	2.0	.80	0	70	A96	DL41a	AMV
55	Am9141DDC	4096	1	S	MNG	620n	578m	0.0	5.0	2.0	.80	0	70	A96	DL41a	AMV
56#	HM4315P	4096	1	S	MCX	620n	1.0 ☑	0.0	5.0	2.4	.80	0	70	A124	DL40b	HITJ
57	Am91L40ADC	4096	1	S	MNG	770n	368m	0.0	5.0	2.0	.80	0	70	A48	DL41a	AMV
58	Am91L40ADM	4096	1	S	MNG	770n	368m	0.0	5.0	2.0	.80	55	125	A48	DL41a	AMV
59	Am91L41ADC	4096	1	S	MNG	770n	368m	0.0	5.0	2.0	.80	0	70	A96	DL41a	AMV
60	Am91L41ADM	4096	1	S	MNG	770n	368m	0.0	5.0	2.0	.80	55	125	A96	DL41a	AMV
61	Am9140ADC	4096	1	S	MNG	770n	578m	0.0	5.0	2.0	.80	0	70	A48	DL41a	AMV
62	Am9140ADM	4096	1	S	MNG	770n	578m	0.0	5.0	2.0	.80	55	125	A48	DL41a	AMV
63	Am9141ADC	4096	1	S	MNG	770n	578m	0.0	5.0	2.0	.80	0	70	A96	DL41a	AMV
64	Am9141BDC	4096	1	S	MNG	770n	578m	0.0	5.0	2.0	.80	0	70	A96	DL41a	AMV
65	uPD411AC-E	4096	1	D	MNX	800n	300m†	5.0	12	2.4	.60§	0	70	A106	DL98	NECM
66#	uPD411D-E	4096	1	D	MNX	800n	350m†	5.0	12	2.4	.60§	0	70	A59	DL5c	NECJ
67	9010-1200	4096	8		MNX	250n$	11	24	24			0	60		MD2c	WSC
68	9010-1230	4096	8		MNX	250n$	8.8	24	24			0	60		MD2c	WSC
69	MSC2101#5	4096	8	S	MNG	250n	6.0	0.0	5.0	2.5	.50	0	50		MD2f	MSCC
70	MSC2101#4	4096	8	S	MNG	350n	6.0	0.0	5.0	2.5	.50	0	50		MD2f	MSCC
71	IMX-TAI	4096	8	S	MNX	420n		0.0	5.0			0	45		MD2e	TAI
72	MSC4201	4096	8	S	MCX	450n	9.0	0.0	5.0	2.5	.50	0	50		MD2h	MSCC
73	MSC2101#3	4096	8	S	MNG	475n	6.0	0.0	5.0	2.5	.50	0	50		MD2f	MSCC
74▼	Z6132-3CS	4096	8	D	MNG	600n	200m	0.0	5.0	2.0	.80	0	70			ZIL
75▼	Z6132-3PS	4096	8	D	MNG	600n	200m	0.0	5.0	2.0	.80	0	70			ZIL
76▼	Z6132-4CS	4096	8	D	MNG	650n	200m	0.0	5.0	2.0	.80	0	70			ZIL
77▼	Z6132-4PS	4096	8	D	MNG	650n	200m	0.0	5.0	2.0	.80	0	70			ZIL
78▼	Z6132-5CS	4096	8	D	MNG	700n	200m	0.0	5.0	2.0	.80	0	70			ZIL
79▼	Z6132-5PS	4096	8	D	MNG	700n	200m	0.0	5.0	2.0	.80	0	70			ZIL
80	MSC2101#2	4096	8	S	MNG	750n	6.0	0.0	5.0	2.5	.50	0	50		MD2f	MSCC
81	MSC2101#1	4096	8	S	MNG	1.0u	6.0	0.0	5.0	2.5	.50	0	50		MD2f	MSCC
82	Am90R16EDC	16384	1	D	MNG	200n$	426m	5.0	12	2.7	.80	0	70	A137	DL6s	AMV
83	Am9016EDC	16384	1	D	MNG	200n$	426m	5.0	12	2.7	.80	0	70	A137	DL6s	AMV
84#	HM4816	16384	1	D	MNX	200n	1.0 ☑	0.0	5.0	2.4	.80	0	70		DL☑	HITJ
85	Am90R16DDC	16384	1	D	MNG	250n$	426m	5.0	12	2.7	.80	0	70	A137	DL6s	AMV
86	Am9016DDC	16384	1	D	MNG	250n$	426m	5.0	12	2.7	.80	0	70	A137	DL6s	AMV
87	Am90R16CDC	16384	1	D	MNG	300n$	426m	5.0	12	2.7	.80	0	70	A137	DL6s	AMV
88	Am9016CDC	16384	1	D	MNG	300n$	426m	5.0	12	2.7	.80	0	70	A137	DL6s	AMV
89#	TMM416D-2	16384	1	D	MNG	320n	1.0	0.0	5.0	2.7	0.8	0	70	A149	DL199	TOSJ
90	uPD416C-5	16384	1	D	MNG	320n	462m	5.0	12	2.4	.80	0	70	A109	DL93	NECM
91	uPD416D-5	16384	1	D	MNG	320n	462m	5.0	12	2.4	.80	0	70	A109	DL6f	NECM
92#	HM4716A-2	16384	1	D	MNX	375n	462m	5.0	12						DL☑	HITJ
93#	HM4716A-3	16384	1	D	MNX	375n	462m	5.0	12						DL☑	HITJ
94	MK4116-2	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	0	70			MOS
95	MK4116-3	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	0	70			MOS
96	MKB4116E84	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	55	85			MOS
97	MKB4116F84	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	55	85			MOS
98	MKB4116J2	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	0	70		MO	MOS
99	MKB4116J3	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	0	70			MOS
100	MKB4116J4	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	0	70			MOS
101	MKB4116J83	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	55	85			MOS
102	MKB4116J84	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	55	85			MOS
103	MKB4116J93	16384	1	D	MNX	375n	462m	5.0	12	2.4	.80	55	85			MOS
104#	TMM416D-3	16384	1	D	MNG	375n	1.0	0.0	5.0	2.7	0.8	0	70	A149	DL199	TOSJ
105	uPD416C-2	16384	1	D	MNG	375n	462m	5.0	12	2.4	.80	0	70	A109	DL93	NECM
106	uPD416C-3	16384	1	D	MNG	375n	462m	5.0	12	2.4	.80	0	70	A109	DL93	NECM
107	uPD416D-2	16384	1	D	MNG	375n	462m	5.0	12	2.4	.80	0	70	A109	DL6f	NECM
108	uPD416D-3	16384	1	D	MNG	375n	462m	5.0	12	2.4	.80	0	70	A109	DL6f	NECM
109	MCM6616L4	16384	1	D	MNG	400n	1.0 ☑	5.0	12	2.4	.80§	0	70	A77	DL73	MOTA
110	MCM6616P4	16384	1	D	MNG	400n	1.0 ☑	5.0	12	2.4	.80§	0	70	A77	DL53	MOTA

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

11. READ-WRITE MEMORIES (RAMS)

IN ORDER OF: (1)No. WORDS (2)BITS PER WORD (3)WORST CASE R/W CYCLE TIME &(4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZATION 1 No. WORDS	ORGANIZATION 2 BITS PER WORD	MODE	TECHN-OLOGY	3 W/C Min. Rd/Wr CYC.TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED POWER SUPPLY SPAN NEG. (V)	RATED POWER SUPPLY SPAN POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	MFR. CODE
1#	HM4716A-4	16384	1	D	MNX	410n	462m	5.0	12						DL⍁	HITJ
2	MK4116-4	16384	1	D	MNX	410n	462m	5.0	12	2.4	.80	0	70			MOS
3#	TMM416D-4	16384	1	D	MNG	410n	1.0	0.0	5.0	2.7	0.8	0	70	A149	DL199	TOSJ
4	uPD416C-1	16384	1	D	MNG	410n	462m	5.0	12	2.4	.80	0	70	A109	DL93	NECM
5	uPD416D-1	16384	1	D	MNG	410n	462m	5.0	12	2.4	.80	0	70	A109	DL6f	NECM
6	MCM6616L5	16384	1	D	MNG	450n	1.0 ⍁	5.0	12	2.4	.80§	0	70	A77	DL73	MOTA
7	MCM6616P5	16384	1	D	MNG	450n	1.0 ⍁	5.0	12	2.4	.80§	0	70	A77	DL53	MOTA
8	uPD416C	16384	1	D	MNG	510n	462m	5.0	12	2.4	.80	0	70	A109	DL93	NECM
9	uPD416D	16384	1	D	MNG	510n	462m	5.0	12	2.4	.80	0	70	A109	DL6f	NECM
10	TDM-SCA1624M	16384	24	S	MCX	350n$	15	0.0	5.0	2.0	.80	55	85			TSC
11	TDM-SCA2416M	24576	16	S	MCX	350n$	15	0.0	5.0	2.0	.80	55	85			TSC
12	TMS4132-15JDL	32768	1	D	MNG	375n	380m†	5.0	12	2.4	.80§	0	70	A100		TII
13	TMS4132-20JDL	32768	1	D	MNG	375n	380m†	5.0	12	2.4	.80§	0	70	A100		TII
14	TMS4132-25JDL	32768	1	D	MNG	410n	380m†	5.0	12	2.4	.80§	0	70	A100		TII
15	MSC4301	32768	8	D	MNG	600n	18	0.0	5.0	2.5	.50	0	50		MD2g	MSCC
16	TMS4164-15JDL	65536	1	D	MNX	250	125m†	0.0	5.0	2.4	.80	0	70	A100a		TII

12. READ-ONLY MEMORIES (ROMS)

IN ORDER OF: (1)TYPE CODE (2)No. WORDS (3)BITS/WORD (4)ACCESS TIME & (5)TYPE No.

LINE No.	5 TYPE No.	1 TYPE CODE	ORGANIZATION 2 No. WORDS	3 BITS PER WORD	OP. MODE P C G O M D E	TECHNOLOGY	4 MAX. ACCESS TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED PWR. SUPPLY SPAN NEG. (V)	POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	OPERATING TEMP. (-)	(+)	SYM:*-MIN Δ-MAX S-STATIC D-DYNAMIC DESCRIPT.	DRAWINGS LOGIC/ BLOCK	OUTLINE Δ=MO	MFR. CODE
1▼	N82S100F	FPLA	48	8	SC	BTX	50n	850m	0.0	5.0	2.0	.80§	0	75		B2	DL10	SIC
2▼	N82S101F	FPLA	48	8	SC	BTX	50n	850m	0.0	5.0	2.0	.80§	0	75		B2	DL10	SIC
3	HM1-6611A-2	FPLA	256	4	SE	MCX	325n	300m	0.0	10	7.0	2.0§	55	125	Tri-State	B115	DL130	HAS
4	HM1-6611A-9	FPLA	256	4	SE	MCX	325n	300m	0.0	10	7.0	2.0§	40	85	Tri-State	B115	DL130	HAS
5	HM1-6611-2	FPLA	256	4	SE	MCX	500n	50m	0.0	5.0	3.0	.80§	55	125	Tri-State	B115	DL130	HAS
6	HM1-6611-9	FPLA	256	4	SE	MCX	500n	50m	0.0	5.0	3.0	.80§	40	85	Tri-State	B115	DL130	HAS
7	HM9-6611-2	FPLA	256	4	SE	MCX	500n	50m	0.0	5.0	3.0	.80§	55	125	Tri-State	B115	FP9a	HAS
8	IDM29750JC	PROM	32	8	SE	BED	30n	550m	0.0	5.0	2.0	.80	0	70		B98	DL6q	NSC
9	IDM29750NC	PROM	32	8	SE	BED	30n	550m	0.0	5.0	2.0	.80	0	70		B98	DL33a	NSC
10	IDM29751JC	PROM	32	8	SE	BED	30n	550m	0.0	5.0	2.0	.80§	0	70		B98	DL6q	NSC
11	IDM29751NC	PROM	32	8	SE	BED	30n	550m	0.0	5.0	2.0	.80§	0	70		B98	DL33a	NSC
12	IDM29750JM/883	PROM	32	8	SE	BED	35n	550m	0.0	5.0	2.0	0.8	55	125	Ti-Wfuse	B98	DL	NSC
13	IDM29751JM/883	PROM	32	8	SE	BED	35n	550m	0.0	5.0	2.0	0.8§	55	125	Ti-Wfuse	B98	DL	NSC
14	Am29750DC	PROM	32	8	SE	BTD	40n	500m	0.0	5.0	2.0	.80	0	70	Open Coll	B70	DL8c	AMV
15	Am29751DC	PROM	32	8	SE	BTD	40n	550m	0.0	5.0	2.0	.80§	0	70	Tri-State	B70	DL8c	AMV
16	IDM29750JM	PROM	32	8	SE	BED	40n	550m	0.0	5.0	2.0	.80	55	125		B98	DL6q	NSC
17	IDM29751JM	PROM	32	8	SE	BED	40n	550m	0.0	5.0	2.0	.80§	55	125		B98	DL6q	NSC
18▼	TBP18S030J	PROM	32	8	SE	BTD	40n	550m	0.0	5.0	2.0	.80§	0	70		B33	DL6d	TII
19▼	TBP18S030N	PROM	32	8	SE	BTD	40n	550m	0.0	5.0	2.0	.80§	0	70		B33	DL23	TII
20▼	TBP18SA030J	PROM	32	8	SE	BTD	40n	550m	0.0	5.0	2.0	.80	0	70		B33	DL6d	TII
21▼	TBP18SA030N	PROM	32	8	SE	BTD	40n	550m	0.0	5.0	2.0	.80	0	70		B33	DL23	TII
22	IM5600CFE	PROM	32	8	SE	BTX	50n	1.0	0.0	5.0	2.0	.80§	0	75		B81	FP8	INL
23	IM5610CFE	PROM	32	8	SE	BTX	50n	1.0	0.0	5.0	2.0	.80§	0	75		B81	FP8	INL
24	N82S123F	PROM	32	8	SC	BTX	50n	385m	0.0	5.0	2.0	.85§	0	75		B5	DL6	SIC
25▼	N82S123N	PROM	32	8	SC	BTX	50n	385m	0.0	5.0	2.0	.85§	0	75		B5	DL4	SIC
26	Am29750DM	PROM	32	8	SE	BTD	60n	500m	0.0	5.0	2.0	.80	55	125	Open Coll	B70	DL8c	AMV
27	Am29751DM	PROM	32	8	SE	BTD	60n	550m	0.0	5.0	2.0	.80§	55	125	Tri-State	B70	DL8c	AMV
28	S82S123F	PROM	32	8	SC	BTX	65n	425m	0.0	5.0	2.0	.80§	55	125		B5	DL6	SIC
29	MCM5003AL	PROM	64	8	SE	BTX	75n	600m	0.0	5.0	2.5	.45%	0	70		B64	DL68	MOTA
30	MCM5004AL	PROM	64	8	SE	BTX	75n	600m	0.0	5.0	2.5	.45%	0	70		B64	DL68	MOTA
31	MCM5303AL	PROM	64	8	SE	BTX	75n	600m	0.0	5.0	2.5	.45%	55	125		B64	DL68	MOTA
32	MCM5303L	PROM	64	8	SE	BTX	75n	475m	0.0	5.0	2.5	.45%	55	125	Open Coll	B64	DL68	MOTA
33	MCM5304L	PROM	64	8	SE	BTX	75n	600m	0.0	5.0	2.5	.45%	55	125		B64	DL68	MOTA
34	IDM29760JC	PROM	256	4	SE	BED	50n	650m	0.0	5.0	2.0	.80	0	70		B99	DL6q	NSC
35	IDM29760JM/883	PROM	256	4	SE	BED	50n	650m	0.0	5.0	2.0	0.8	55	125	Ti-Wfuse	B99	DL	NSC
36	IDM29760NC	PROM	256	4	SE	BED	50n	650m	0.0	5.0	2.0	.80	0	70		B99	DL33a	NSC
37	IDM29761JC	PROM	256	4	SE	BED	50n	650m	0.0	5.0	2.0	.80§	0	70		B99	DL6q	NSC
38	IDM29761JM/883	PROM	256	4	SE	BED	50n	650m	0.0	5.0	2.0	0.8§	55	125	Ti-Wfuse	B99	DL	NSC
39	IDM29761NC	PROM	256	4	SE	BED	50n	650m	0.0	5.0	2.0	.80§	0	70		B99	DL33a	NSC
40	N82S126F	PROM	256	4	SC	BTX	50n	600m	0.0	5.0	2.0	.85	0	75		B4	DL6	SIC
41▼	N82S126N	PROM	256	4	SC	BTX	50n	600m	0.0	5.0	2.0	.85	0	75		B4	DL4	SIC
42	N82S129F	PROM	256	4	SC	BTX	50n	600m	0.0	5.0	2.0	.85§	0	75		B4	DL6	SIC
43▼	N82S129N	PROM	256	4	SC	BTX	50n	600m	0.0	5.0	2.0	.85§	0	75		B4	DL4	SIC
44	IDM29760JM	PROM	256	4	SE	BED	60n	650m	0.0	5.0	2.0	.80	55	125		B99	DL6q	NSC
45	IDM29761JM	PROM	256	4	SE	BED	60n	650m	0.0	5.0	2.0	.80§	55	125		B99	DL6q	NSC
46	IM5603ACFE	PROM	256	4	SE	BTX	60n	650m	0.0	5.0	2.0	.80	0	75		B82	FP8	INL
47	IM5603ACPE	PROM	256	4	SE	BTX	60n	650m	0.0	5.0	2.0	.80	0	75		B82	DL33e	INL
48	IM5623CFE	PROM	256	4	SE	BTX	65n	650m	0.0	5.0	2.0	.80	0	75		B82	FP8	INL
49	IM5623CPE	PROM	256	4	SE	BTX	65n	650m	0.0	5.0	2.0	.80	0	75		B82	DL33e	INL
50▼	TBP24S10J	PROM	256	4	SE	BTD	65n	675m	0.0	5.0	2.0	.80§	0	70		B33a	DL6d	TII
51▼	TBP24S10N	PROM	256	4	SE	BTD	65n	675m	0.0	5.0	2.0	.80§	0	70		B33a	DL23	TII
52▼	TBP24SA10J	PROM	256	4	SE	BTD	65n	675m	0.0	5.0	2.0	.80	0	70		B33a	DL6d	TII
53▼	TBP24SA10N	PROM	256	4	SE	BTD	65n	675m	0.0	5.0	2.0	.80	0	70		B33a	DL23	TII
54	Am29760DC	PROM	256	4	SE	BTD	70n	400m	0.0	5.0	2.0	.80	0	75	Open Coll	B71	DL6e	AMV
55	Am29761DC	PROM	256	4	SE	BTD	70n	400m	0.0	5.0	2.0	.80§	0	75	Tri-State	B71	DL6e	AMV
56	Am29761DM	PROM	256	4	SE	BTD	70n	400m	0.0	5.0	2.0	.80§	55	125	Tri-State	B71	DL6e	AMV
57	S82S126F	PROM	256	4	SC	BTX	70n	625m	0.0	5.0	2.0	.80	55	125		B4	DL6	SIC
58	S82S129F	PROM	256	4	SC	BTX	70n	625m	0.0	5.0	2.0	.80§	55	125		B4	DL6	SIC
59▼	TBP24S10M-J	PROM	256	4	SE	BTD	75n	675m	0.0	5.0	2.0	.80§	55	125		B33a	DL6d	TII
60▼	TBP24S10M-W	PROM	256	4	SE	BTD	75n	675m	0.0	5.0	2.0	.80§	55	125		B33a	Δ004AG	TII
61	Am29760DM	PROM	256	4	SE	BTD	80n	400m	0.0	5.0	2.0	.80	55	125	Open Coll	B71	DL6e	AMV
62	Am29760FM	PROM	256	4	SE	BTD	80n	400m	0.0	5.0	2.0	.80	55	125	Open Coll	B71	FP1a	AMV
63	Am29761FM	PROM	256	4	SE	BTD	80n	400m	0.0	5.0	2.0	.80§	55	125	Tri-State	B71	FP1a	AMV
64	HM9-6611A-2	PROM	256	4	SE	MCX	325n	300m	0.0	10	7.0	2.0§	55	125	Tri-State	B115	FP9a	HAS
65	HM1-6611D-5	PROM	256	4	SE	MCX	800n	125m	0.0	5.0	3.0	.65§	0	75	Tri-State	B115	DL130	HAS
66	N82S114I	PROM	256	8	SC	BTD	60n	925m	0.0	5.0	2.0	.85§	0	75		B3	DL9	SIC
67▼	TBP28LA22J	PROM	256	8	SE	BTD	70n	775m	0.0	5.0	2.0	.80	0	70		B7	DL16	TII
68▼	TBP28LA22N	PROM	256	8	SE	BTD	70n	775m	0.0	5.0	2.0	.80	0	70		B7	DL17	TII
69▼	TBP28L22J	PROM	256	8	SE	BTD	80n	775m	0.0	5.0	2.0	.80§	0	70		B7	DL16	TII
70▼	TBP28L22M-J	PROM	256	8	SE	BTD	80n	775m	0.0	5.0	2.0	.80§	55	125		B7	DL16	TII
71▼	TBP28L22N	PROM	256	8	SE	BTD	80n	775m	0.0	5.0	2.0	.80§	0	70		B7	DL17	TII
72#	uPD464D	PROM	256	8	SC	MNG	450n	520m†	0.0	12	2.4	.70§	10	70		B55	DL45b	NECJ
73	MK3602P-1	PROM	256	8	SE	MNG	550n	300m	9.0	5.0	3.0	.65	0	70		B39a	DL9f	MOS
74	MK3702T-1	PROM	256	8	SE	MNG	550n	300m	9.0	5.0	3.0	.65	0	70	Erasable	B39a	DL72	MOS
75	Am9702-1DC	PROM	256	8		MNG	750n	1.0	9.0	5.0	3.0	.80	0	70		B39	DL9c	AMV
76	Am9702-1HDC	PROM	256	8		MNG	750n	1.0	9.0	5.0	3.0	.80	0	70		B39	DL9c	AMV
77	MK3602P-2	PROM	256	8	SE	MNG	750n	300m	9.0	5.0	3.0	.65	0	70		B39a	DL9f	MOS
78	MK3702T-2	PROM	256	8	SE	MNG	750n	300m	9.0	5.0	3.0	.65	0	70	Erasable	B39a	DL72	MOS
79#	uPD454D	PROM	256	8	SE	MNX	800n	245m†	0.0	12	3.0	.70§	10	70	EEPROM	B53	DL45b	NECJ
80	Am1702ADC	PROM	256	8	SC	MPG	1.0u	540m	9.0	5.0	3.0	.80	0	70	Erasable	B39	DL89a	AMV
81	Am9702AHDL	PROM	256	8	SC	MNG	1.0u	540m	9.0	5.0	3.0	.80	55	125	Erasable	B39	DL89a	AMV
82	Am9702DC	PROM	256	8		MNG	1.0u	1.0	9.0	5.0	3.0	.80	0	70		B39	DL9c	AMV
83	Am9702HDC	PROM	256	8		MNG	1.0u	1.0	9.0	5.0	3.0	.80	0	70		B39	DL9c	AMV
84	C1702	PROM	256	8		MNG	1.0u	1.0	9.0	5.0	3.0	.80	0	70		B39	DL9c	AMV
85	C1702A	PROM	256	8		MNG	1.0u	1.0	9.0	5.0	3.0	.80	0	70		B39	DL9c	AMV
86	C8302	PROM	256	8	SC	MPG	1.0u	540m	9.0	5.0	3.0	.65§	0	70	Mask	B13a	DL3a	ITL
87	CDP1842CD	PROM	256	8	SE	MCG	1.0u		0.5	7.0	3.5	1.5	40	85	EPROM	C44	DL137	RCA
88	MK3602P-3	PROM	256	8	SE	MNG	1.0u	300m	9.0	5.0	3.0	.65	0	70		B39a	DL9f	MOS
89	MK3702T-3	PROM	256	8	SE	MNG	1.0u	300m	9.0	5.0	3.0	.65	0	70	Erasable	B39a	DL72	MOS
90	P8302	PROM	256	8	SC	MPG	1.0u	540m	9.0	5.0	3.0	.65§	0	70	Mask	B13a	DL14a	ITL
91	C8702A	PROM	256	8	SE	MPG	1.3u	540m	0.0	12	3.0	.65§	0	70	Reprogram	B13	DL3a	ITL
92	C4302	PROM	256	8	SC	MNG	1.7u		0.0	5.0		§	0	70	Mask	B13a	DL3a	ITL
93	C4702A	PROM	256	8	SE	MPG	1.7u		0.0	5.0		§	0	70	Erasable	B13	DL3a	ITL
94	P4302	PROM	256	8	SC	MNG	1.7u		0.0	5.0		§	0	70	Mask	B13a	DL14a	ITL
95	P4702A	PROM	256	8	SE	MPG	1.7u		0.0	5.0		§	0	70	Erasable	B13	DL14a	ITL
96	C1702-1	PROM	256	8		MNG	750u	1.0	9.0	5.0	3.0	.80	0	70		B39	DL9c	AMV
97	R29613DC	PROM	512	4	SE	BTX	60n	650m	0.0	5.0	2.0	.80§	0	75	Tri-State	B74b	DL6h	RTN
98	R29613DM	PROM	512	4	SE	BTX	75n	650m	0.0	5.0	2.0	.80§	55	125	Tri-State	B74b	DL6h	RTN
99	R29613FM	PROM	512	4	SE	BTX	75n	650m	0.0	5.0	2.0	.80§	55	125	Tri-State	B74b	FP1b	RTN
100▼	TBP28S42M-J	PROM	512	8	SE	BTD			0.0	5.0	2.0	.80§	55	125		B7a	DL16	TII
101	MCM7640P	PROM	512	8	SE	BTD	40n†		0.0	5.0					Open Coll	B65	DL69	MOTA
102	IM5605ACDG	PROM	512	8	SE	MCS	55n	925m	0.0	5.0	2.0	.80	0	75		B84	DL7i	INL
103	IM5605ACJG	PROM	512	8	SE	MCS	55n	925m	0.0	5.0	2.0	.80	0	75		B84	DL7i	INL
104	IM5625ACDG	PROM	512	8	SE	MCS	55n	925m	0.0	5.0	2.0	.80	0	75		B84	DL7i	INL
105	IM5625ACJG	PROM	512	8	SE	MCS	55n	925m	0.0	5.0	2.0	.80	0	75		B84	DL7i	INL
106▼	TBP28S42J	PROM	512	8	SE	BTD	55n†	600m†	0.0	5.0	2.0	.80§	0	70		B7a	DL16	TII

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

12. READ-ONLY MEMORIES (ROMS)

IN ORDER OF: (1)TYPE CODE (2)No. WORDS (3)BITS/WORD (4)ACCESS TIME & (5)TYPE No.

LINE No.	5 TYPE No.	1 TYPE CODE	ORGANIZATION 2 No. WORDS	3 BITS PER WORD	OP. MODE PCGOM DE	4 TECHNOLOGY	MAX. ACCESS TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED PWR. SUPPLY SPAN NEG. (V)	POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	OPERATING TEMP. (-)	(+)	SYM:*-MIN Δ-MAX S-STATIC D-DYNAMIC DESCRIPT.	DRAWINGS LOGIC/ BLOCK	OUTLINE Δ=MO	MFR. CODE
1▼	TBP28S42N	PROM	512	8	SE	BTD	55n†	600mt	0.0	5.0	2.0	.80§	0	70		B7a	DL17	TII
2	DM54S472	PROM	512	8	SE	BED	60n	775m	0.0	5.0	2.0	0.8§	55	125	Ti-WFuse	B137	DL	NSC
3	DM54S473	PROM	512	8	SE	BED	60n	775m	0.0	5.0	2.0	0.8	55	125	Ti-WFuse	B137	DL	NSC
4	DM74S472	PROM	512	8	SE	BED	60n	775m	0.0	5.0	2.0	0.8§	0	70	Ti-WFuse	B137	DL	NSC
5	DM74S473	PROM	512	8	SE	BED	60n	775m	0.0	5.0	2.0	0.8	0	70	Ti-WFuse	B137	DL	NSC
6▼	N82S115F	PROM	512	8	SC	BTD	60n	925m	0.0	5.0	2.0	.85§	0	75		B3a	DL9	SIC
7	DM54S474	PROM	512	8	SE	BED	65n	850m	0.0	5.0	2.0	0.8	55	125	Ti-WFuse	B138	DL	NSC
8	DM54S475	PROM	512	8	SE	BED	65n	850m	0.0	5.0	2.0	0.8	55	125	Ti-WFuse	B138	DL	NSC
9	DM74S474	PROM	512	8	SE	BED	65n	850m	0.0	5.0	2.0	0.8	0	70	Ti-WFuse	B138	DL	NSC
10	DM74S475	PROM	512	8	SE	BED	65n	850m	0.0	5.0	2.0	0.8	0	70	Ti-WFuse	B138	DL	NSC
11	IM5605AMDG	PROM	512	8	SE	MCS	70n	925m	0.0	5.0	2.0	.80	55	125		B84	DL7i	INL
12	IM5605AMJG	PROM	512	8	SE	MCS	70n	925m	0.0	5.0	2.0	.80	55	125		B84	DL7i	INL
13	IM5605CDG	PROM	512	8	SE	BTX	70n	925m	0.0	5.0	2.0	.80	0	75		B84	DL7i	INL
14	IM5625AMDG	PROM	512	8	SE	MCS	70n	925m	0.0	5.0	2.0	.80	55	125		B84	DL7i	INL
15	IM5625AMJG	PROM	512	8	SE	MCS	70n	925m	0.0	5.0	2.0	.80	55	125		B84	DL7i	INL
16	IM5625CDG	PROM	512	8	SE	BTX	70n	925m	0.0	5.0	2.0	.80	0	75		B84	DL7i	INL
17	R29623DC	PROM	512	8	SE	BTD	70n	755m	0.0	5.0	2.0	.80§	0	75	Power Sw	B88a	DL∅	RTN
18#	uPB405D	PROM	512	8	SE	BTX	70n	800m	0.0	5.0	2.0	.80	25	75		B59	DL18c	NECJ
19#	uPB425D	PROM	512	8	SE	BTX	70n	800m	0.0	5.0	2.0	.80§	25	75		B59	DL18c	NECJ
20▼	TBP28SA42J	PROM	512	8	SE	BTD	75n	775m	0.0	5.0	2.0	.80	0	70		B7a	DL16	TII
21▼	TBP28SA42N	PROM	512	8	SE	BTD	75n	775m	0.0	5.0	2.0	.80	0	70		B7a	DL17	TII
22	IM5605MDG	PROM	512	8	SE	BTX	80n	925m	0.0	5.0	2.0	.80	55	125		B84	DL7i	INL
23	IM5625MDG	PROM	512	8	SE	BTX	80n	925m	0.0	5.0	2.0	.80	55	125		B84	DL7i	INL
24	R29623DM	PROM	512	8	SE	BTD	85n	755m	0.0	5.0	2.0	.80§	55	125	Power Sw	B88a	DL∅	RTN
25	R29623FM	PROM	512	8	SE	BTD	85n	755m	0.0	5.0	2.0	.80§	55	125	Power Sw	B88a	FP∅	RTN
26▼	TBP24SA41J	PROM	1024	4	SE	BTD	35n†	700m	0.0	5.0	2.0	.80	0	70		B92	DL19	TII
27▼	TBP24SA41N	PROM	1024	4	SE	BTD	35n†	700m	0.0	5.0	2.0	.80	0	70		B92	DL20	TII
28▼	TBP28S41J	PROM	1024	4	SE	BTD	35n†	700m	0.0	5.0	2.0	.80§	0	70		B92	DL19	TII
29▼	TBP28S41M-J	PROM	1024	4	SE	BTD	35n†	700m	0.0	5.0	2.0	.80§	55	125		B92	DL19	TII
30▼	TBP28S41N	PROM	1024	4	SE	BTD	35n†	700m	0.0	5.0	2.0	.80§	0	70		B92	DL20	TII
31	MCM7642L	PROM	1024	4	SE	BTD	40n†		0.0	5.0					Open Coll	B66		MOTA
32	MCM7643L	PROM	1024	4	SE	BTD	40n†		0.0	5.0					Tri-State	B66		MOTA
33	MCM7643P	PROM	1024	4	SE	BTD	40n†		0.0	5.0					Tri-State	B66		MOTA
34	IM56S26CD	PROM	1024	4	SE	BXX	50n		0.0	5.0	2.0	.80§	0	75	Tri-State	B58	DL25a	INL
35	IM56S26CJ	PROM	1024	4	SE	BXX	50n		0.0	5.0	2.0	.80§	0	75	Tri-State	B58	DL40a	INL
36	DM54S572	PROM	1024	4	SE	BED	60n	700m	0.0	5.0	2.0	0.8	55	125	Ti-WFuse	B139	DL	NSC
37	DM54S573	PROM	1024	4	SE	BED	60n	700m	0.0	5.0	2.0	0.8§	55	125	Ti-WFuse	B139	DL	NSC
38	DM54S574	PROM	1024	4	SE	BED	60n	700m	0.0	5.0	2.0	0.8§	55	125	Ti-WFuse	B139	DL	NSC
39	DM74S572	PROM	1024	4	SE	BED	60n	700m	0.0	5.0	2.0	0.8	0	70	Ti-WFuse	B139	DL	NSC
40	DM74S573	PROM	1024	4	SE	BED	60n	700m	0.0	5.0	2.0	0.8§	0	70	Ti-WFuse	B139	DL	NSC
41	DM74S574	PROM	1024	4	SE	BED	60n	700m	0.0	5.0	2.0	0.8§	0	70	Ti-WFuse	B139	DL	NSC
42	IM56S26MD	PROM	1024	4	SE	BXX	60n		0.0	5.0	2.0	.80§	55	125	Tri-State	B58	DL25a	INL
43	IM56S26MJ	PROM	1024	4	SE	BXX	60n		0.0	5.0	2.0	.80§	55	125	Tri-State	B58	DL40a	INL
44	MCM7660P	PROM	1024	8	SE	BTD	40n†		0.0	5.0					Open Coll	B67		MOTA
45	MCM7661L	PROM	1024	8	SE	BTD	40n†		0.0	5.0					Tri-State	B67		MOTA
46	SN54S2708J	PROM	1024	8	SE	BTD	45n†	600m	0.0	5.0	2.0	.80§	55	125		B94	DL9a	TII
47	SN54S3708J	PROM	1024	8	SE	BTD	45n†	600m	0.0	5.0	2.0	.80	55	125		B94	DL9a	TII
48▼	TBP24S86J	PROM	1024	8	SE	BTD	45n†	600mt	0.0	5.0	2.0	.80§	0	70		B93	DL9a	TII
49▼	TBP24S86M-J	PROM	1024	8	SE	BTD	45n†	600mt	0.0	5.0	2.0	.80§	55	125		B93	DL9a	TII
50▼	TBP24S86N	PROM	1024	8	SE	BTD	45n†	600mt	0.0	5.0	2.0	.80§	0	70		B93	DL18	TII
51▼	TBP28SA86J	PROM	1024	8	SE	BTD	45n†	600mt	0.0	5.0	2.0	.80	0	70		B93	DL9a	TII
52▼	TBP28SA86N	PROM	1024	8	SE	BTD	45n†	600mt	0.0	5.0	2.0	.80	0	70		B93	DL18	TII
53	R29631DC	PROM	1024	8	SE	BTD	70n	850m	0.0	5.0	2.0	.80§	0	75		B120	DL∅	RTN
54	R29635DC	PROM	1024	8	SE	BTD	70n	850m	0.0	5.0	2.0	.80§	0	75		B121	DL∅	RTN
55	R29633DC	PROM	1024	8	SE	BTD	75n	225m	0.0	5.0	2.0	.80§	0	75	Pwr Sw	B120a	DL∅	RTN
56	R29637DC	PROM	1024	8	SE	BTD	75n	225m	0.0	5.0	2.0	.80§	0	75	Pwr Sw	B121a	DL∅	RTN
57	R29631DM	PROM	1024	8	SE	BTD	90n	850m	0.0	5.0	2.0	.80§	55	125		B120	DL∅	RTN
58	R29635DM	PROM	1024	8	SE	BTD	90n	850m	0.0	5.0	2.0	.80	55	125		B121	DL∅	RTN
59	R29633DM	PROM	1024	8	SE	BTD	115n	225m	0.0	5.0	2.0	.80	55	125	Pwr Sw	B120a	DL∅	RTN
60	R29637DM	PROM	1024	8	SE	BTD	115n	225m	0.0	5.0	2.0	.80	55	125	Pwr Sw	B121a	DL∅	RTN
61	C8308	PROM	1024	8	SC	MNG	450n	775m	5.0	12	3.3	.80§	0	70	Mask	B15	DL3a	ITL
62	C8704	PROM	1024	8	SE	MNG	450n	800m	5.0	12	3.0	.65§	0	70	Reprogram	B6	DL3a	ITL
63	C8708	PROM	1024	8	SE	MNG	450n	800m	5.0	12	3.0	.65§	0	70	Reprogram	B6	DL3a	ITL
64#	HN462708	PROM	1024	8	SE	MNG	450n	850mt	5.0	12	3.0	.65§	0	70		B79	DL9g	HITJ
65	MCM68708MTL	PROM	1024	8	SE	MNG	450n	750m	5.0	12	2.0	.80§	55	125		B35	DL9b	MOTA
66	MK2708	PROM	1024	8	SE	MNG	450n	450m	5.0	12	3.0	.65	0	70	Erasable	B68		MOS
67	P8308	PROM	1024	8	SC	MNG	450n	775m	5.0	12	3.3	.80§	0	70	Mask	B15	DL14a	ITL
68	TMS27L08JL	PROM	1024	8	SE	MNG	450n	475m	5.0	12	2.2	.65§	0	70	Erasable	B68	Δ015AA	TII
69#	uPD458D	PROM	1024	8	SE	MNX	450n	605mt	0.0	12	3.0	.70§	10	70	EEPROM	B54	DL57	NECJ
70	uPD2308AC	PROM	1024	8	SC	MNX	450n	545m	5.0	12	2.4	.80§	10	70		B56	DL18e	NECM
71	uPD2308AD	PROM	1024	8	SC	MNX	450n	545m	5.0	12	2.4	.80§	10	70	Mask	B56	DL45b	NECM
72#	uPD2308D	PROM	1024	8	SC	MNX	450n	545m	5.0	12	2.4	.80§	10	70		B56	DL45b	NECJ
73	9010-1321	PROM	1024	8	SE	MNX	750n	11	24	32			0	60			MD2c	WSC
74	DM77S184	PROM	2048	4	SE	BED	40n	700m	0.0	5.0	2.0	0.8	55	125	Ti-W Fuse	B140	DL	NSC
75	DM77S185	PROM	2048	4	SE	BED	40n	700m	0.0	5.0	2.0	0.8§	55	125	Ti-WFuse	B140	DL	NSC
76	DM87S184	PROM	2048	4	SE	BED	40n	700m	0.0	5.0	2.0	0.8	0	70	Ti-W Fuse	B140	DL	NSC
77	DM87S185	PROM	2048	4	SE	BED	40n	700m	0.0	5.0	2.0	0.8§	0	70	Ti-WFuse	B140	DL	NSC
78	R29651DC	PROM	2048	4	SE	BTD	75n	850m	0.0	5.0	2.0	.80§	0	75		B123	DL∅	RTN
79	R29653DC	PROM	2048	4	SE	BTD	80n	225m	0.0	5.0	2.0	.80§	0	75	Pwr Sw	B123a	DL∅	RTN
80	R29651DM	PROM	2048	4	SE	BTD	95n	850m	0.0	5.0	2.0	.80	55	125		B123	DL∅	RTN
81	R29653DM	PROM	2048	4	SE	BTD	100n	225m	0.0	5.0	2.0	.80	55	125	Pwr Sw	B123a	DL∅	RTN
82	MM1-PROM	PROM	2048	8	SE	MNG		4.5	12	5.0	2.0	.80			Erasable	B77	MD3	CLI
83	R29681DC	PROM	2048	8	SE	BTD	80n	900m	0.0	5.0	2.0	.80§	0	75		B124	DL∅	RTN
84	R29683DC	PROM	2048	8	SE	BTD	85n	225m	0.0	5.0	2.0	.80§	0	75	Pwr Sw	B124a	DL∅	RTN
85	R29681DM	PROM	2048	8	SE	BTD	100n	900m	0.0	5.0	2.0	.80	55	125		B124	DL∅	RTN
86	R29683DM	PROM	2048	8	SE	BTD	105n	225m	0.0	5.0	2.0	.80	55	125	Pwr Sw	B124a	DL∅	RTN
87	C8355-2	PROM	2048	8			300n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Ceramic	Z57-10	DL70	ITL
88	D8355-2	PROM	2048	8			300n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Hermetic	Z57-10	DL148	ITL
89	P8355-2	PROM	2048	8			300n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Plastic	Z57-10	DL140	ITL
90	TMS27A16L	PROM	2048	8	SE	MNG	300n	1.0	5.0	12	2.2	.65	0	70	Erasable	B85	DL9b	MOTA
91	C8355	PROM	2048	8			400n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Ceramic	Z57-10	DL70	ITL
92	D8355	PROM	2048	8			400n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Hermetic	Z57-10	DL148	ITL
93	IC8355	PROM	2048	8			400n	1.5 ∅	0.5	7.0	2.0	.80	40	85	Ceramic	Z57-10	DL70	ITL
94	ID8355	PROM	2048	8			400n	1.5 ∅	0.5	7.0	2.0	.80	40	85	Hermetic	Z57-10	DL148	ITL
95	IP8355	PROM	2048	8			400n	1.5 ∅	0.5	7.0	2.0	.80	40	85	Plastic	Z57-10	DL140	ITL
96	P8355	PROM	2048	8			400n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Plastic	Z57-10	DL140	ITL
97	C8755A	PROM	2048	8			450n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Ceramic	Z57-11	DL70	ITL
98	C8755A-2	PROM	2048	8			450n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Ceramic	Z57-11	DL70	ITL
99	D8755A	PROM	2048	8			450n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Hermetic	Z57-11	DL148	ITL
100	D8755A-2	PROM	2048	8			450n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Hermetic	Z57-11	DL148	ITL
101#	HN462716	PROM	2048	8	SE		450n	385m	0.0	5.0	2.0	.80§	20	75		B111	DL9g	HITJ
102	P8755A	PROM	2048	8			450n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Plastic	Z57-11	DL140	ITL
103	P8755A-2	PROM	2048	8			450n	1.5 ∅	0.5	7.0	2.0	.80	0	70	Plastic	Z57-11	DL140	ITL
104#	TMP8755AC	PROM	2048	8	SE	MNG	450n	1.5 ∅	0.0	5.0	2.0	0.8	0	70	Eraseable	B135	DL209	TOSJ
105	TMS2716L	PROM	2048	8	SE	MNG	450n	1.0	5.0	12	2.2	.65	0	70	Erasable	B85	DL9b	MOTA
106#	uPD466C	PROM	2048	8	SC	MNG	475n	416mt	5.0	12	3.0	.80§	10	70		B57	DL67	NECJ
107#	uPD466D	PROM	2048	8	SC	MNG	475n	416mt	5.0	12	3.0	.80§	10	70		B57	DL57	NECJ
108	9010-1322	PROM	2048	8	SE	MNX	750n	11	24	32			0	60			MD2c	WSC
109	IC8755	PROM	2048	8			750n	1.5 ∅	0.5	7.0	2.0	.80	40	85	Ceramic	Z57-11	DL70	ITL
110	ID8755	PROM	2048	8			750n	1.5 ∅	0.5	7.0	2.0	.80	40	85	Hermetic	Z57-11	DL148	ITL

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

12. READ-ONLY MEMORIES (ROMS)

IN ORDER OF: (1)TYPE CODE (2)No. WORDS (3)BITS/WORD (4)ACCESS TIME & (5)TYPE No.

LINE No.	[5] TYPE No.	[1] TYPE CODE	ORGANIZATION [2] No. WORDS	[3] BITS PER WORD	OP. MODE PCGOMDE	TECHNOLOGY	[4] MAX. ACCESS TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED PWR. SUPPLY SPAN NEG. (V)	POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	OPERATING TEMP. (-)	(+)	SYM:*-MIN Δ-MAX S-STATIC D-DYNAMIC DESCRIPT.	DRAWINGS LOGIC/ BLOCK	OUTLINE Δ=MO	MFR. CODE
1	IP8755	PROM	2048	8			750n	1.5 ☑	0.5	7.0	2.0	.80	40	85	Plastic	Z57-11	DL140	ITL
2	9010-1323	PROM	3072	8	SE	MNX	750n	11	24	32			0	60			MD2c	WSC
3	9010-1324	PROM	4096	8	SE	MNX	750n	11	24	32			0	60			MD2c	WSC
4	TMS25L32JDL	PROM	4192	8	SE	MNG	450n	455m	0.0	5.0	2.0	.80§	0	70	ROM	B90		TII
5	TMS2564JL	PROM	8192	8	SE	MNX	450n	840m	0.0	5.0	2.2	.65	0	70	EPROM		DL☑	TII
6	TDMSCP1624M	PROM	16384	24	SE	BTX	100n$	6.0	0.0	5.0	2.0	.80	55	85	Pwr Sw			TSC
7	3851	PSU	1024	8	SC	MNX	2.0u	566m	0.0	12	3.5	.80	0	70	W/Timer	B17		FSC
8	MK3851N/12X	PSU	1024	8	SC	MNX	2.0u	566m	0.0	12	3.5	.80	0	70	Prog Stor	B128	DL167	MOS
9	MK3851P/12X	PSU	1024	8	SC	MNX	2.0u	566m	0.0	12	3.5	.80	0	70	Prog Stor	B128	DL167	MOS
10	SN5488AJ	ROM	32	8	SC	BTD	45n	400m	0.0	5.0	2.0	.80	55	125		B30	DL6d	TII
11	SN5488AW	ROM	32	8	SC	BTD	45n	400m	0.0	5.0	2.0	.80	55	125		B30	Δ004AG	TII
12	SN7488AJ	ROM	32	8	SC	BTD	45n	400m	0.0	5.0	2.0	.80	0	70		B30	DL6d	TII
13	SN7488AN	ROM	32	8	SC	BTD	45n	400m	0.0	5.0	2.0	.80	0	70		B30	DL23	TII
14	SN54187J	ROM	256	4	SC	BTD	60n	650m	0.0	5.0	2.0	.80	55	125		B31	DL6d	TII
15	SN54187W	ROM	256	4	SC	BTD	60n	650m	0.0	5.0	2.0	.80	55	125		B31	Δ004AG	TII
16	SN74187J	ROM	256	4	SC	BTD	60n	650m	0.0	5.0	2.0	.80	0	70		B31	DL6d	TII
17	SN74187N	ROM	256	4	SC	BTD	60n	650m	0.0	5.0	2.0	.80	0	70		B31	DL23	TII
18	SN54S371J	ROM	256	8	SC	BTD	45n†	775m	0.0	5.0	2.0	.80§	55	125		B8	DL16	TII
19	SN74S271J	ROM	256	8	SC	BTD	70n	775m	0.0	5.0	2.0	.80	0	70		B8a	DL16	TII
20	SN74S271N	ROM	256	8	SC	BTD	70n	775m	0.0	5.0	2.0	.80	0	70		B8a	DL17	TII
21	SN74S371J	ROM	256	8	SC	BTD	70n	775m	0.0	5.0	2.0	.80§	0	70		B8	DL16	TII
22	SN74S371N	ROM	256	8	SC	BTD	70n	775m	0.0	5.0	2.0	.80§	0	70		B8	DL17	TII
23	SN54S271J	ROM	256	8	SC	BTD	95n	775m	0.0	5.0	2.0	.80	55	125		B8a	DL16	TII
24#	HN35600P	ROM	256	8	SC	MPX	930n	1.0	15	0.0	-1.5	-5.5	0	70	4 Bit I/O	B109	DL4a	HITJ
25	SN74S270J	ROM	512	4	SC	BTD	70n	775m	0.0	5.0	2.0	.80	0	70		B32	DL6d	TII
26	SN74S270N	ROM	512	4	SC	BTD	70n	775m	0.0	5.0	2.0	.80	0	70		B32	DL23	TII
27	SN74S370J	ROM	512	4	SC	BTD	70n	775m	0.0	5.0	2.0	.80§	0	70		B32a	DL6d	TII
28	SN74S370N	ROM	512	4	SC	BTD	70n	775m	0.0	5.0	2.0	.80§	0	70		B32a	DL23	TII
29	SN54S270J	ROM	512	4	SC	BTD	95n	775m	0.0	5.0	2.0	.80	55	125		B32	DL6d	TII
30	SN54S370J	ROM	512	4	SC	BTD	95n	775m	0.0	5.0	2.0	.80§	55	125		B32a	DL6d	TII
31	CDP1831D	ROM	512	8	SC	MCG	400n	5.0m♦	0.0	10	7.0	3.0	40	85		B25	DL137	RCA
32	CDP1831E	ROM	512	8	SC	MCG	400n	5.0m♦	0.0	10	7.0	3.0	40	85		B25	Δ015AA	RCA
33	HCMP1831D	ROM	512	8	SC	MCG	400n†	30m†	0.0	10			55	125		B25		HAC
34	HCMP1832D	ROM	512	8	SC	MCG	400n†	15m†	0.0	10			55	125		B26		HAC
35	Am9214DC	ROM	512	8	SC	MNG	500n	263m	0.0	5.0	2.0	.80§	0	70		B37	DL9d	AMV
36	Am9214DM	ROM	512	8	SC	MNG	500n	350m	0.0	5.0	2.0	.80§	55	125		B37	DL9d	AMV
37	CDP1832D	ROM	512	8	SC	MCG	500n	5.0m♦	0.0	10	7.0	3.0	40	85		B26	DL137	RCA
38	CDP1832E	ROM	512	8	SC	MCG	500n	5.0m♦	0.0	10	7.0	3.0	40	85		B26	Δ015AA	RCA
39	S6834	ROM	512	8	S	MPX	575n	750m	12	5.0	2.75	.80§	0	70				AMI
40	S6834-1	ROM	512	8	S	MPX	750n	750m	12	5.0	2.75	.80§	0	70				AMI
41	HCMP1831CD	ROM	512	8	SC	MCG	850n†	30m†	0.0	5.0			55	125		B25		HAC
42	HCMP1832CD	ROM	512	8	SC	MCG	850n†	15m†	0.0	5.0			55	125		B26		HAC
43	Am35142DC	ROM	512	8	SC	MNG	1.0u	250m	0.0	5.0	2.0	.80§	0	70		B37	DL9d	AMV
44	CDP1831CD	ROM	512	8	SC	MCG	1.0u	2.5m♦	0.0	5.0	3.5	1.5	40	85		B25	DL137	RCA
45	CDP1831CE	ROM	512	8	SC	MCG	1.0u	2.5m♦	0.0	5.0	3.5	1.5	40	85		B25	Δ015AA	RCA
46	CDP1832CD	ROM	512	8	SC	MCG	1.0u	2.5m♦	0.0	5.0	3.5	1.5	40	85		B26	DL137	RCA
47	CDP1832CE	ROM	512	8	SC	MCG	1.0u	2.5m♦	0.0	5.0	3.5	1.5	40	85		B26	Δ015AA	RCA
48	Am35141DC	ROM	512	8	SC	MNG	700m	250m	0.0	5.0	2.0	.80§	0	70		B37	DL9d	AMV
49	Am9208DDC	ROM	1024	8	SC	MNG	250n	603m	0.0	12	2.4	.80§	0	70	Mask	B38	DL89	AMV
50	MCM68B308L	ROM	1024	8	SC	MNG	250n	650m	0.0	5.0	2.0	.80§	0	70		B107	DL9b	MOTA
51	Am9208CDC	ROM	1024	8	SC	MNG	300n	485m	0.0	12	2.4	.80§	0	70	Mask	B38	DL89	AMV
52	Am9208CDM	ROM	1024	8	SC	MNG	300n	685m	0.0	12	2.6	.80§	55	125	Mask	B38	DL89	AMV
53	HCMP1833D	ROM	1024	8	SC	MCG	350n†	120m†	0.0	10			55	125		B75		HAC
54	HCMP1834D	ROM	1024	8	SC	MCG	350n†	15m†	0.0	10			55	125		B76		HAC
55	MCM68A30AC	ROM	1024	8	SC	MNG	350n	650m	0.0	5.0	2.0	.80§	0	70		B106	DL68	MOTA
56	MCM68A308L	ROM	1024	8	SC	MNG	350n	650m	0.0	5.0	2.0	.80§	0	70		B107	DL9b	MOTA
57	MCM68A308P	ROM	1024	8	SC	MNG	350n	650m	0.0	5.0	2.0	.80§	0	70		B107	DL7b	MOTA
58	MCM65308P	ROM	1024	8	SC	MNG	350n	1.0	5.0	12	4.0	.80§	0	70		B6	DL7b	MOTA
59	MK30000	ROM	1024	8	SC	MNX	350n	330m	0.0	5.0	2.0	.80	0	70	Mask			MOS
60	Am9208BDC	ROM	1024	8	SC	MNG	400n	485m	0.0	12	2.4	.80§	0	70	Mask	B38	DL89	AMV
61	Am9208BDM	ROM	1024	8	SC	MNG	400n	591m	0.0	12	2.6	.80§	55	125	Mask	B38	DL89	AMV
62	CDP1833D	ROM	1024	8	SC	MCG	425n	5.0m♦	0.0	10	7.0	3.0	40	85		B75	DL137	RCA
63	CDP1833E	ROM	1024	8	SC	MCG	425n	5.0m♦	0.0	10	7.0	3.0	40	85		B75	Δ015AA	RCA
64	CDP1834D	ROM	1024	8	SC	MCG	425n	5.0m†	0.0	10	7.0	3.0	40	85		B116	DL137	RCA
65	CDP1834E	ROM	1024	8	SC	MCG	425n		0.0	10	7.0	3.0	40	85		B116	Δ015AA	RCA
66	F68308P	ROM	1024	8	SC	MNG	500n	650m	0.0	5.0	2.0	.80§	0	70			DL151	FSC
67#	HN46830	ROM	1024	8	SC	MNX	500n	350m†	0.0	5.0					Mark		DL☑	HITJ
68	MCM6830AL	ROM	1024	8	SC	MNG	500n	650m	0.0	5.0	2.0	.80	0	70		B1	DL9b	MOTA
69	MCM68308P	ROM	1024	8	SC	MNG	500n	650m	0.0	5.0	2.0	.80	0	70		B24	DL7b	MOTA
70#	uPD465C	ROM	1024	8	C	MNX	500n	310m	5.0	12	3.0	.70	10	70		B60	DL18e	NECJ
71#	uPD465D	ROM	1024	8	C	MNX	500n	310m	5.0	12	3.0	.70	10	70		B60	DL45b	NECJ
72	S6830	ROM	1024	8	SS	MNG	575n	650m	0.0	5.0	2.4	.40§	0	70		B1	DL3	AMI
73	CDP1834CD	ROM	1024	8	SC	MCG	750n	5.0m†	0.0	5.0	3.5	1.5	40	85		B116	DL137	RCA
74	CDP1834CE	ROM	1024	8	SC	MCG	750n		0.0	5.0	3.5	1.5	40	85		B116	Δ015AA	RCA
75	CDP1833CD	ROM	1024	8	SC	MCG	775n	2.5m♦	0.0	5.0	3.5	1.5	40	85		B75	DL137	RCA
76	CDP1833CE	ROM	1024	8	SC	MCG	775n	2.5m♦	0.0	5.0	3.5	1.5	40	85		B75	Δ015AA	RCA
77	HCMP1833CD	ROM	1024	8	SC	MCG	850n†	120m†	0.0	5.0			55	125		B75		HAC
78	HCMP1834CD	ROM	1024	8	SC	MCG	850n†	15m†	0.0	5.0			55	125		B76		HAC
79#	M58730-XXXS	ROM	1024	8	SC	MNG	850n	720m	5.0	12	3.3	.80	0	70	Mask	B112	DL125	MITJ
80#	HN35800P	ROM	1024	8	SC	MPX	930n	1.0	15	0.0	-1.5	-5.5	0	70		B110	DL67	HITJ
81	A05	ROM	1024	8	SC	MPX	1.8u†	250m	12	5.0	3.5	-12	0	70		B20	DL44	RKW
82	HM6312A-9	ROM	1024	12	SE	MCG	200n	100m	0.0	10	7.0	2.0	40	85	Prog RAM	B29a	DL☑	HAS
83	HM6312A-2	ROM	1024	12	SE	MCG	220n	100m	0.0	10	7.0	2.0	55	125	Prog RAM	B29a	DL☑	HAS
84	IM6312AIJN	ROM	1024	12	SC	MCG	250n†	11u†	0.0	11	7.7	2.2	40	85		B29	DL19c	INL
85	IM6312CJN	ROM	1024	12	SC	MCG	500n†	7.0u†	0.0	7.0	4.9	1.4	0	75		B29	DL19c	INL
86	IM6312IJN	ROM	1024	12	SC	MCG	500n†	7.0u†	0.0	7.0	4.9	1.4	40	85		B29	DL19c	INL
87	HM6312-9	ROM	1024	12	SE	MCG	510n	25m	0.0	5.0	3.5	1.0	40	85	Prog RAM	B29a	DL☑	HAS
88	HM6312-2	ROM	1024	12	SE	MCG	560n	25m	0.0	5.0	3.5	1.0	55	125	Prog RAM	B29a	DL☑	HAS
89	HM6312C-9	ROM	1024	12	SE	MCG	640n	25m	0.0	5.0	3.5	1.0	40	85	Prog RAM	B29a	DL☑	HAS
90	C4316A	ROM	2048	8	SC	MNG			0.0	5.0		§	0	70		B14	DL3a	ITL
91#	HD46846P	ROM	2048	8	SC			800m	0.0	5.0	2.0	.80	20	75	I/O Timer	B114	DL☑	HITJ
92	P4316A	ROM	2048	8	SC	MNG			0.0	5.0		§	0	70		B14	DL14a	ITL
93	SBP9818CJ	ROM	2048	8	SC	BIX	200n			.30▼	2.0	.80	0	70	Mask	B89	DL9a	TII
94	SBP9818CN	ROM	2048	8	SC	BIX	200n			.30▼	2.0	.80	0	70	Mask	B89	DL18	TII
95	SBP9818MJ	ROM	2048	8	SC	BIX	200n			.30▼	2.0	.80	55	125	Mask	B89	DL9a	TII
96	9010-1332	ROM	2048	8	SC	MNX	250n	4.8	0.0	5.0			0	60	Perm ROM		MD2c	DSI
97	Am9216CDC	ROM	2048	8	SC	MNG	300n	1.0	0.0	12	2.4	.80§	0	70		B36	DL9c	AMV
98	Am9218CDC	ROM	2048	8	SC	MNG	350n	350m	0.0	5.0	2.0	.80	0	70	Mask	B86	DL89	AMV
99	MCM68A316AP	ROM	2048	8	SC	MNG	350n	650m	0.0	5.0	2.0	.80§	0	70		B108	DL7b	MOTA
100	MCM68A316EC	ROM	2048	8	SC	MNG	350n	650m	0.0	5.0	2.0	.80§	0	70		B108a	DL68	MOTA
101	MK34000P	ROM	2048	8	SC	MNG	350n	330m	0.0	5.0	2.0	.80	0	70	Mask	B14	DL9f	MOS
102	SBP8316CJ	ROM	2048	8	SC	BIX	350n	500m†	0.0	5.0	2.0	.80	0	70	Mask	B89	DL9a	TII
103	SBP8316CN	ROM	2048	8	SC	BIX	350n	500m†	0.0	5.0	2.0	.80	0	70	Mask	B89	DL18	TII
104	SBP8316MJ	ROM	2048	8	SC	BIX	350n	500m†	0.0	5.0	2.0	.80	55	125	Mask	B89	DL9a	TII
105	Am9216BDC	ROM	2048	8	SC	MNG	400n	1.0	0.0	12	2.4	.80§	0	70		B36	DL9c	AMV
106	Am9216BDM	ROM	2048	8	SC	MNG	400n	1.0	0.0	12	2.6	.80§	55	125		B36	DL9c	AMV
107	Am9217BDC	ROM	2048	8	SC	MNG	450n	350m	0.0	5.0	2.0	.80§	0	70	Mask	B14	DL89	AMV
108	Am9217BDM	ROM	2048	8	SC	MNG	450n	400m	0.0	5.0	2.0	.80§	55	125	Mask	B14	DL89	AMV
109	Am9218BDC	ROM	2048	8	SC	MNG	450n	350m	0.0	5.0	2.0	.80	0	70	Mask	B86	DL89	AMV
110	Am9218BDM	ROM	2048	8	SC	MNG	450n	400m	0.0	5.0	2.0	.80	55	125	Mask	B86	DL89	AMV

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

12. READ-ONLY MEMORIES (ROMS)

IN ORDER OF: (1)TYPE CODE (2)No. WORDS (3)BITS/WORD (4)ACCESS TIME & (5)TYPE No.

LINE No.	5 TYPE No.	1 TYPE CODE	ORGANIZATION 2 No. WORDS	3 BITS PER WORD	OP. MODE PCGMOD E	TECHNOLOGY	4 MAX. ACCESS TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED PWR. SUPPLY SPAN NEG. (V)	POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	LOW (max) (V)	OPERATING TEMP. (-)	(+)	SYM:*-MIN Δ-MAX S-STATIC D-DYNAMIC DESCRIPT.	DRAWINGS LOGIC/ BLOCK	OUTLINE Δ=MO	MFR. CODE
1	C8316E	ROM	2048	8	SC	MNG	450n	475m	0.0	5.0	2.0	.80	0	70	Mask	B86	DL89	AMV
2	R2316BC	ROM	2048	8	SC	MNG	450n	490m	0.0	5.0	2.0	.80§	0	70		B101a	DL☑	RKW
3	R2316BP	ROM	2048	8	SC	MNG	450n	490m	0.0	5.0	2.0	.80§	0	70		B101a		RKW
4	R2316EC	ROM	2048	8	SC		450n	325m	0.0	5.0	2.0	.80	0	70	Cer/Plas	B136	DL217	RKW
5	S6831	ROM	2048	8	SC	MNX	450n	400m	0.0	5.0	2.0	.80§	0	70		B103	DL9h	AMI
6	S6831A	ROM	2048	8	SC	MNX	450n	400m	0.0	5.0	2.0	.80§	0	70		B103a	DL9h	AMI
7	S6831B	ROM	2048	8	SC	MNX	450n	400m	0.0	5.0	2.0	.80§	0	70		B103b	DL9h	AMI
8	S6831C	ROM	2048	8	SC	MNX	450n	400m	0.0	5.0	2.0	.80§	0	70		B103c	DL9h	AMI
9#	uPD2316EC	ROM	2048	8	SC	MNX	450n	600m	0.0	5.0	2.0	.80§	10	70		B61a	DL18e	NECJ
10#	uPD2316ED	ROM	2048	8	SC	MNX	450n	600m	0.0	5.0	2.0	.80§	10	70		B61a	DL45b	NECJ
11	F68316P	ROM	2048	8	SC	MNG	500n	650m	0.0	5.0	2.0	.80§	0	70		B63	DL151	FSC
12	MCM65317L	ROM	2048	8	SC	MNG	500n	527m	5.0	12	3.0	.80§	0	70		B62	DL9b	MOTA
13	MCM65317P	ROM	2048	8	SC	MNG	500n	527m	5.0	12	3.0	.80§	0	70		B62	DL7b	MOTA
14	MCM68316E1L	ROM	2048	8	SC	MNG	500n	650m	0.0	5.0	2.0	.80§	-40	85		B63	DL9b	MOTA
15	MCM68316EL	ROM	2048	8	SC	MNG	500n	650m	0.0	5.0	2.0	.80§	0	70		B63	DL9b	MOTA
16	MCM68317L	ROM	2048	8	SC	MNX	500n		0.0	5.0		§				B34	DL9b	MOTA
17	Am9217ADC	ROM	2048	8	SC	MNG	550n	350m	0.0	5.0	2.0	.80§	0	70	Mask	B14	DL89	AMV
18	Am9217ADM	ROM	2048	8	SC	MNG	550n	400m	0.0	5.0	2.0	.80§	55	125	Mask	B14	DL89	AMV
19	MCM6832C	ROM	2048	8	SC	MNG	550n	527m	5.0	12	3.0	.80§	0	70		B23	DL68	MOTA
20	MCM6832P	ROM	2048	8	SC	MNG	550n	527m	5.0	12	3.0	.80	0	70		B23	DL7b	MOTA
21	MK31000P	ROM	2048	8	SC	MNG	550n	330m	0.0	5.0	2.0	.80	0	70	Mask	B14	DL9f	MOS
22	3516	ROM	2048	8	SC	MNG	600n		0.0	5.0						B16		FSC
23▼	SCM5317	ROM	2048	8	SC	MCG	625n	125m	0.0	5.0	4.6	.40	55	125	MASK		DL☑	SSS
24▼	SCM5316	ROM	2048	8	SC	MCG	700n	175m	0.0	5.0	2.0	.80	55	125	MASK		DL☑	SSS
25	C8316A	ROM	2048	8	SC	MNG	850n	490m	0.0	5.0	2.0	.80§	0	70		B14	DL3a	ITL
26	HCMP1835D	ROM	2048	8	SC	MCX	850n	30m	0.0	5.0	3.4	1.6	55	125		B117		HAC
27#	M58731-XXXP	ROM	2048	8	SC	MNG	850n	490m	0.0	5.0	2.0	.80	0	70	Mask	B113	DL124	MITJ
28#	M58731-XXXS	ROM	2048	8	SC	MNG	850n	490m	0.0	5.0	2.0	.80	0	70	Mask	B113	DL125	MITJ
29	P8316A	ROM	2048	8	SC	MNG	850n	490m	0.0	5.0	2.0	.80§	0	70		B14	DL14a	ITL
30	A52	ROM	2048	8	SC	MPX	1.8u†	200m	12	5.0	3.5	-12	0	70		B19	DL44	RKW
31	A66	ROM	4096	8	C	MPX		330m	12	5.0	3.5	-1.5	0	70		B100	DL☑	RKW
32	9010-1334	ROM	4096	8	SC	MNX	250n	8.7	0.0	5.0			0	60	Perm ROM		MD2c	DSI
33	MK32000	ROM	4096	8	SC	MNX	300n	200m	0.0	5.0	2.0	.80	0	70	Mask			MOS
34	R2332-3C	ROM	4096	8	SC	MNG	300n	600m	0.0	5.0	2.0	.80§	0	70		B102	DL☑	RKW
35	MCM68A332C	ROM	4096	8	SC	MNG	350n	400m	0.0	5.0	2.0	.80§	0	70		B105	DL68	MOTA
36	MCM68A332P	ROM	4096	8	SC	MNG	350n	400m	0.0	5.0	2.0	.80§	0	70		B105	DL7b	MOTA
37	R2332C	ROM	4096	8	SC	MNG	450n	600m	0.0	5.0	2.0	.80§	0	70		B102	DL☑	RKW
38	R2332P	ROM	4096	8	SC	MNG	450n	600m	0.0	5.0	2.0	.80§	0	70		B102		RKW
39	ROM4732	ROM	4096	8	S	MNX	450n	580m	0.0	5.0	2.0	.65	1	70	32k ROM	B69	DL☑	SMC
40	S68332	ROM	4096	8	SC	MNX	450n	600m	0.0	5.0	2.0	.80§	0	70		B104	DL3c	AMI
41▼#	uPD2332C	ROM	4096	8	SC	MNX	450n	550m	0.0	5.0	2.0	.80§	10	70	MASK	B96	DL102	NECJ
42▼#	uPD2332D	ROM	4096	8	SC	MNX	450n	550m	0.0	5.0	2.0	.80§	10	70	MASK	B96	DL45a	NECJ
43	MCM68332L	ROM	4096	8	SC	MNG	500n	650m	0.0	5.0	2.0	.80§	0	70		B105	DL9b	MOTA
44	MCM68332P	ROM	4096	8	SC	MNG	500n	650m	0.0	5.0	2.0	.80§	0	70		B105	DL7b	MOTA
45#	HN46532-3	ROM	4096	8	SC	MNG	650n	200m†	0.0	5.0	2.0	.80	20	75		B80	DL80	HITJ
46	A88	ROM	8192	8	SC			410m	12	5.0	3.5	-1.5	0	70		B100a	DL☑	RKW
47	MCM68B364C	ROM	8192	8	SC	MNG	250n	400m	0.0	5.0	2.0	.80§	0	70		B118	DL68	MOTA
48	MCM68B364P	ROM	8192	8	SC	MNG	250n	400m	0.0	5.0	2.0	.80§	0	70		B118	DL142	MOTA
49	MK36000	ROM	8192	8	SC	MNX	300n	200m	0.0	5.0	2.0	.80	0	70	Mask			MOS
50	MCM68A364P	ROM	8192	8	SC	MNG	350n	400m	0.0	5.0	2.0	.80§	0	70		B118	DL142	MOTA
51	uPD2364C	ROM	8192	8	SC	MNX	450n	700m	0.0	5.0	2.0	.80§	10	70	Mask	B126	DL102	NECM
52	uPD2364D	ROM	8192	8	SC	MNX	450n	700m	0.0	5.0	2.0	.80§	10	70	Mask	B126	DL170	NECM

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	[3] TYPE No.	[1] TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ☑-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	[2] MFR. CODE
1	MK3854P-10	0.	8	3.5	.80	0.0	12	541m	40	85	Direct Memory Access	Z03-30	DL167	MOS
2▼	Am2909ADC	01	4	2.0	.80§	0.0	5.0		0	70	Internal Addr Register;Icc 130mA Max	Z01-2	DL49	AMD
3▼	Am2909ADM	01	4	2.0	.70§	0.0	5.0		55	125	Internal Addr Register;Icc 130mA Max	Z01-2	DL49	AMD
4▼	Am2909AFM	01	4	2.0	.70§	0.0	5.0		55	125	Internal Addr Register;Icc 130mA Max	Z01-2	FP5	AMD
5▼	Am2909APC	01	4	2.0	.80§	0.0	5.0		0	70	Internal Addr Register;Icc 130mA Max	Z01-2	DL143a	AMD
6▼	Am2911ADC	01	4	2.0	.80§	0.0	5.0		0	70	Internal Addr Register;Icc 130mA Max	Z01-2a	DL51	AMD
7▼	Am2911ADM	01	4	2.0	.70§	0.0	5.0		55	125	Internal Addr Register;Icc 130mA Max	Z01-2a	DL51	AMD
8	S6840	01	16	2.0	.80	0.0	5.0	550m	0	70	Programmable Timer,3 Bin Counters	Z01-12	DL67e	AMI
9	Am2909DC	01	4	2.0	.80	0.0	5.0	650m	0	70	Microprogram Sequencer	Z01-2	DL49	AMV
10	Am2909DM	01	4	2.0	.70	0.0	5.0	650m	55	125	Microprogram Sequencer	Z01-2	DL49	AMV
11	Am2909FM	01	4	2.0	.70	0.0	5.0	650m	55	125	Microprogram Sequencer	Z01-2	FP5	AMV
12♦	Am2909PC	01	4	2.0	.80	0.0	5.0	650m	0	70	Microprogram Sequencer	Z01-2	DL143a	AMV
13	Am2910DC	01	12	2.0	.80	0.0	5.0	975mt	0	70	Microprogram Controller/Sequencer	Z01-10	DL1g	AMV
14	Am2910DM	01	12	2.0	.80	0.0	5.0	975mt	55	125	Microprogram Controller/Sequencer	Z01-10	DL1g	AMV
15	Am2910FM	01	12	2.0	.80	0.0	5.0	975mt	55	125	Microprogram Controller/Sequencer	Z01-10a		AMV
16	Am2910PC	01	12	2.0	.80	0.0	5.0		0	70	Microprogram Controller/Sequencer	Z01-10	DL☑	AMV
17	Am2911DC	01	4	2.0	.80	0.0	5.0	650m	0	70	Microprogram Sequencer	Z01-2a	DL51	AMV
18	Am2911DM	01	4	2.0	.70	0.0	5.0	650m	55	125	Microprogram Sequencer	Z01-2a	DL51	AMV
19	Am2911PC	01	4	2.0	.80	0.0	5.0	650m	0	70	Microprogram Sequencer	Z01-2a	DL60	AMV
20	Am9513CC	01	16			0.0	5.0		0	70	8 or 16 Bit Bus Interf;Sys Timing	Z01-20	DL178	AMV
21	Am9513DC	01	16			0.0	5.0		0	70	8 or 16 Bit Bus Interf;Sys Timing	Z01-20	DL180	AMV
22	Am9513DM	01	16			0.0	5.0		55	125	8 or 16 Bit Bus Interf;Sys Timing	Z01-20	DL180	AMV
23	Am9513PC	01	16			0.0	5.0		0	70	8 or 16 Bit Bus Interf;Sys Timing	Z01-20	DL179	AMV
24	Am29803DC	01	4	2.0	.80	0.0	5.0	400m	0	70	16 Way Branch Control Unit	Z01-6	DL6e	AMV
25	Am29803DM	01	4	2.0	.70	0.0	5.0	400m	55	125	16 Way Branch Control Unit	Z01-6	DL6e	AMV
26	Am29803FM	01	4	2.0	.70	0.0	5.0	400m	55	125	16 Way Branch Control Unit	Z01-6	FP1a	AMV
27	Am29803PC	01	4	2.0	.80	0.0	5.0	400m	0	70	16 Way Branch Control Unit	Z01-6	DL33c	AMV
28	Am29811DC	01	4	2.0	.80	0.0	5.0	400m	0	70	Next Address Control Unit	Z01-7	DL6e	AMV
29	Am29811DM	01	4	2.0	.70	0.0	5.0	400m	55	125	Next Address Control Unit	Z01-7	DL33c	AMV
30	Am29811FM	01	4	2.0	.70	0.0	5.0	400m	55	125	Next Address Control Unit	Z01-7	FP1a	AMV
31	9406DC	01	4	2.0	.80	0.0	5.0	800m	0	75	Program Stack,16W x 4 Bit	Z01-17	DL154	FSC
32	9406DM	01	4	2.0	.70	0.0	5.0	800m	55	125	Program Stack,16wx4Bit	Z01-17	DL154	FSC
33	9406PC	01	4	2.0	.80	0.0	5.0	800m	0	75	Program Stack,16wx4Bit	Z01-17	DL155	FSC
34	9408DC	01	10	2.0	.80	0.0	5.0	650mt	0	75	Microprogram Sequencer,8 Branches	Z01-18	DL37C	FSC
35	9408DM	01	10	2.0	.80	0.0	5.0	650mt	55	125	Microprogram Sequencer,8 Branches	Z01-18	DL37C	FSC
36	9408PC	01	10	2.0	.80	0.0	5.0	650mt	0	75	Microprogram Sequencer,8 Branches	Z01-18	DL11i	FSC
37	F6840D	01	16	2.0	.80§	0.0	5.0	550m	0	70	Programmable Timer;28 Pin Ceramic	Z01-22	DL203	FSC
38	F6840P	01	16	2.0	.80§	0.0	5.0	550m	0	70	Programmable Timer;28 Pin Plastic	Z01-22	DL204	FSC
39	C8253	01	16	2.2	.80	0.0	5.0	1.0 ☑	0	70	Program Interval Timer;t clk 380ns	Z01-9	DL3a	ITL
40	C8253-5	01	16	2.2	.80	0.0	5.0	700m	0	70	Programmable Interval Timer,Ceramic	Z01-9	DL3a	ITL
41	D8253	01	8	2.2	.80	0.0	5.0	1.0 ☑	0	70	Program Interval Timer;t clk 380ns	Z01-9	DL7a	ITL
42	D8253-5	01	16	2.2	.80	0.0	5.0	1.0 ☑	0	70	Prog Interval Timer;Clk 380ns	Z01-9	DL7h	ITL
43	P8253	01	16	2.2	.80	0.0	5.0	1.0 ☑	0	70	Program Interval Timer;t clk 380ns	Z01-9	DL14a	ITL
44	P8253-5	01	16	2.2	.80	0.0	5.0	700m	0	70	Programmable Interval Timer,Plastic	Z01-9	DL14a	ITL
45	2909FM	01	4	2.0	.70§	0.0	5.0	650m	55	125	Microprogram Sequencer;4 Bit Counter	Z01-2	DL43	MMI
46	2909JC	01	4	2.0	.80§	0.0	5.0	650m	0	70	Microprogram Sequencer;4 Bit Counter	Z01-2	DL29	MMI
47	2909JM	01	4	2.0	.70§	0.0	5.0	650m	55	125	Microprogram Sequencer;4 Bit Counter	Z01-2	DL29	MMI
48	2909NC	01	4	2.0	.80§	0.0	5.0	650m	0	70	Microprogram Sequencer;4 Bit Counter	Z01-2	DL17	MMI
49	2911JC	01	4	2.0	.80§	0.0	5.0	650m	0	70	Microprogram Sequencer;4 Bit Counter	Z01-2a	DL16	MMI
50	2911JM	01	4	2.0	.70§	0.0	5.0	650m	55	125	Microprogram Sequencer;4 Bit Counter	Z01-2a	DL16	MMI
51	2911NC	01	4	2.0	.80§	0.0	5.0	650m	0	70	Microprogram Sequencer;4 Bit Counter	Z01-2a	DL17	MMI
52	MMI57110D	01	8	2.0	.80	0.0	5.0		55	125	Microprogram Controller	Z01-4	DL1h	MMI
53	MMI67110D	01	8	2.0	.80	0.0	5.0		0	70	Microprogram Controller	Z01-4	DL1h	MMI
54	MK3882N	01	8	2.0	.80	0.0	5.0	500m	0	70	Counter Timer 4 8Bit Channels	Z01-8	DL74	MOS
55	MK3882P	01	8	2.0	.80	0.0	5.0	500m	0	70	Same as MK3882N Except Ceramic	Z01-8	DL36d	MOS
56	MC68A40L	01	16	2.0	.80	0.0	5.0	550m	0	70	Progm Timer Mod,Min Write PW 280us	Z01-12	DL74	MOTA
57	MC68A40P	01	16	2.0	.80	0.0	5.0	550m	0	70	Progm Timer Mod,Min Write PW 280us	Z01-12	DL75	MOTA
58	MC68B40L	01	16	2.0	.80	0.0	5.0	550m	0	70	Progm Timer Mod,Min Write PW 220us	Z01-12	DL74	MOTA
59	MC68B40P	01	16	2.0	.80	0.0	5.0	550m	0	70	Progm Timer Mod,Min Write PW 220us	Z01-12	DL75	MOTA
60	MC2909LC	01	4	2.0	.80	0.0	5.0	650m	0	70	Microprogram Sequencer	Z01-2	DL49	MOTA
61	MC2909LM	01	4	2.0	.70	0.0	5.0	650m	55	125	Microprogram Sequencer	Z01-2	DL49	MOTA
62	MC2909PC	01	4	2.0	.80	0.0	5.0	650m	0	70	Microprogram Sequencer	Z01-2	DL75	MOTA
63	MC2910LC	01	12	2.0	.80	0.0	5.0		0	70	Microprogram Controller	Z01-15	DL112	MOTA
64	MC2910LM	01	12	2.0	.80	0.0	5.0		55	125	Microprogram Controller	Z01-15	DL112	MOTA
65	MC2911FM	01	4	2.0	.80	0.0	5.0	650m	55	125	Microprogram Sequencer	Z01-2a	FP14	MOTA
66	MC2911LC	01	4	2.0	.80	0.0	5.0	650m	0	70	Microprogram Sequencer	Z01-2a	DL133	MOTA
67	MC2911LM	01	4	2.0	.80	0.0	5.0	650m	55	125	Microprogram Sequencer	Z01-2a	DL133	MOTA
68	MC2911PC	01	4	2.0	.80	0.0	5.0	650m	0	70	Microprogram Sequencer	Z01-2a	DL132	MOTA
69	MC6840L	01	16	2.0	.80	0.0	5.0	550m	0	70	Progm Timer Mod,Min Write PW 450us	Z01-12	DL74	MOTA
70	MC6840P	01	16	2.0	.80	0.0	5.0	550m	0	70	Progm Timer Mod,Min Write PW 450us	Z01-12	DL75	MOTA
71	MC10801	01	4	-1.9	-.81%	5.2	0.0	1.6	30	85	Microprogram Sequencer	Z01-5	DL55	MOTA
72	MC10806	01	9	-1.1	-1.4	5.2	0.0	2.1	30	85	Dual Access Stack;32x9 Bit	Z01-14	DL55	MOTA
73▼#	uPB2909AD	01	12	2.0	.80	0.0	5.0		10	70	MicroProgram Sequencer		DL105	NECJ
74▼#	uPB2911AD	01	12	2.0	.80	0.0	5.0		10	70	MicroProgram Sequencer		DL110	NECJ
75#	uPD756D00	01	16	3.0	.80	5.0	12	662m	10	70	Control Chip Part of 16 Bit CPU	Z01-13	DL58	NECJ
76#	uPD8253C	01	8	2.2	.80	0.0	5.0	700m	0	70	Progm Interval Timer,tclk 300ns	Z01-9	DL18e	NECJ
77♦	IDM2909AC	01	4	2.0	0.8§	0	5.0	650m	0	70	4-Bit Cascadable Slice;Inter Add Reg	Z01-2	DL67	NSC
78	IDM2909ADC	01	4	2.0	.80§	0.0	5.0	650m	0	70	Microprogram Sequencer;4B Addr Cont	Z01-2	DL36g	NSC
79	IDM2909ADM	01	4	2.0	.80§	0.0	5.0	650m	55	125	Microprogram Sequencer;4B Addr Cont	Z01-2	DL36g	NSC
80♦	IDM2909AJC	01	4	2.0	0.8§	0	5.0	650m	0	70	4-Bit Cascadable Slice;Inter Add Reg	DL67	DL	NSC
81♦	IDM2909AJM	01	4	2.0	0.8§	0	5.0	650m	55	125	4-Bit Cascadable Slice;Inter Add Reg	Z01-2	DL67	NSC
82♦	IDM2909AJM/883	01	4	2.0	0.8§	0	5.0	650m	55	125	4-Bit Cascadable Slice;Inter Add Reg	Z01-2	DL67	NSC
83	IDM2909ANC	01	4	2.0	.80§	0.0	5.0	650m	0	70	Microprogram Sequencer;4B Addr Cont	Z01-2	DL67c	NSC
84	IDM2910ADC	01	12	2.0	0.8	0	5.0	1.3	0	70	12 Bit Wide Address Controller	Z01-10	DL	NSC
85♦	IDM2910ADM	01	12	2.0	0.8	0	5.0	1.4	55	125	12 Bit Wide Address Controller	Z01-10	DL73	NSC
86♦	IDM2910ADM/883	01	12	2.0	0.8	0	5.0	1.4	55	125	12 Bit Wide Address Controller		DL73	NSC
87♦	IDM2910ANC	01	12	2.0	0.8	0	5.0	1.3	0	70	12 Bit Wide Address Controller	Z01-10	DL129	NSC
88♦	IDM2911AC	01	4	2.0	0.8§§	0	5.0	650m	0	70	IDM2909 w/OR In Disconn;R J In Conn	Z01-2	DL110	NSC
89	IDM2911ADC	01	4	2.0	.80§	0.0	5.0	650m	0	70	Microprogram Sequencer;W/O OR Input	Z01-2a	DL51b	NSC
90	IDM2911ADM	01	4	2.0	.80§	0.0	5.0	650m	55	125	Microprogram Sequencer;W/O OR Input	Z01-2a	DL51b	NSC
91♦	IDM2911AJC	01	4	2.0	0.8§	0	5.0	650m	0	70	IDM2909 W/OR In Disconn;R J In Conn	Z01-2	DL110	NSC
92♦	IDM2911AJM	01	4	2.0	0.8§	0	5.0	650m	55	125	IDM2909 W/OR In Disconn;R J In Conn	Z01-2	DL110	NSC
93	IDM2911ANC	01	4	2.0	.80§	0.0	5.0	650m	0	70	Microprogram Sequencer;W/O OR Input	Z01-2a	DL109	NSC
94	IDM29803JC	01	4L	2.0	.80	0.0	5.0	650m	0	70	16 Way Branch Controller	Z01-6	DL6q	NSC
95	IDM29803JM	01	4L	2.0	.80	0.0	5.0	650m	55	125	16 Way Branch Controller	Z01-6	DL6q	NSC
96♦	IDM29803JM/883	01		2.0	0.8	0	5.0	650m	55	125	16 Way Branch Controller	Z01-6	DL87	NSC
97	IDM29803NC	01	4L	2.0	.80	0.0	5.0	650m	0	70	16 Way Branch Controller	Z01-6	DL33a	NSC
98	IDM29811JC	01	4	2.0	.80	0.0	5.0	550m	0	70	Next Address Controller	Z01-7	DL6q	NSC
99	IDM29811JM	01	4	2.0	.80	0.0	5.0	550m	55	125	Next Address Controller	Z01-7	DL6q	NSC
100♦	IDM29811JM/883	01		2.0	0.8	0	5.0	550m	55	125	Next Address Controller	Z01-7	DL87	NSC
101	IDM29811NC	01	4	2.0	.80	0.0	5.0	550m	0	70	Next Address Controller	Z01-7	DL33a	NSC
102▼#	N82S104	01	8	2.0	.85	0.0	5.2	560mt	0	75	Prog Logic Sequencer;Bipolar Field			PHIN
103▼#	N82S105	01	8	2.0	.85	0.0	5.2	560mt	0	75	Prog Logic Sequencer;Bipolar Field			PHIN
104▼#	S82S104	01	8	2.0	.85	0.0	5.5	560mt	55	125	Prog Logic Sequencer;Bipolar Field			PHIN
105▼#	S82S105	01	8	2.0	.85	0.0	5.5	560mt	55	125	Prog Logic Sequencer;Bipolar Field			PHIN
106	N8X02I	01	10	2.0	.80§	0.0	5.0	650m	0	70	Control Store Sequencer;Cer Pkg	Z01-1	DL105	SIC
107	N8X02N	01	10	2.0	.80§	0.0	5.0	650m	0	70	Control Store Sequencer;Plas Pkg	Z01-1	DL105	SIC
108	SBP9964	01		2.0	.80						Timing Controller for SBP9900A	Z01-19		TII
109	SN54S482J	01	4	2.0	.80	0.0	5.0	650m	55	125	4-Bit Slice Control Element	Z01-3	DL16	TII
110	SN74S482J	01	4	2.0	.80	0.0	5.0	700m	0	70	4 Bit Slice Control Element	Z01-3	DL16	TII

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN Ø-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1	SN74S482N	01	4	2.0	.80	0.0	5.0	700m	0	70	4-Bit Slice Control Element	Z01-3	DL17	TII
2	Z80-CTCCS	01	8	2.0	.80	0.0	5.0	600m	0	70	Counter Timer Ckt;Program 4 Ch	Z01-11	DL36f	ZIL
3	Z80A-CTCCS	01	8	2.0	.80	0.0	5.0	600m	0	70	Counter Timer Ckt;Program 4 Ch	Z01-11	DL36f	ZIL
4	Z80ACTCCE	01	8	2.0	.80	0.0	5.0	600m	40	85	Counter Timer Ckt;Program 4 Ch	Z01-11	DL36f	ZIL
5	Z80ACTCCM	01	8	2.0	.80	0.0	5.0	600m	55	125	Counter Timer Ckt;Program 4 Ch	Z01-11	DL36f	ZIL
6	Z80ACTCPS	01	8	2.0	.80	0.0	5.0	600m	0	70	Counter Timer Ckt;Program 4 Ch	Z01-11	DL36f	ZIL
7	Z80CTCCE	01	8	2.0	.80	0.0	5.0	600m	40	85	Counter Timer Ckt;Program 4 Ch	Z01-11	DL36f	ZIL
8	Z80CTCCM	01	8	2.0	.80	0.0	5.0	600m	55	125	Counter Timer Ckt;Program 4 Ch	Z01-11	DL36f	ZIL
9	Z80CTCPS	01	8	2.0	.80	0.0	5.0	600m	0	70	Counter Timer Ckt;Program 4 Ch	Z01-11	DL36f	ZIL
10	Am2913DC	02	8	2.0	.80§	0.0	5.0	120m	0	70	Tri-State Priority Interupt Expander	Z02-5	DL51	AMV
11	Am2913DM	02	8	2.0	.70§	0.0	5.0	120m	55	125	Tri-State Priority Interupt Expander	Z02-5	DL51	AMV
12	Am2913FM	02	8	2.0	.70§	0.0	5.0	120m	55	125	Tri-State Priority Interupt Expander	Z02-5		AMV
13	Am2913PC	02	8	2.0	.80§	0.0	5.0	120m	0	70	Tri-State Priority Interupt Expander	Z02-5	DL60	AMV
14	Am2914DC	02	8	2.0	.80	0.0	5.0		0	70	Vectored Priority Interrupt Encoder	Z02-2	DL1g	AMV
15	Am2914DM	02	8	2.0	.80	0.0	5.0		55	125	Vectored Priority Interrupt Encoder	Z02-2	DL1g	AMV
16	Am2914FM	02	8	2.0	.80	0.0	5.0		55	125	Vectored Priority Interrupt Encoder	Z02-2	DL1g	AMV
17	Am2914PC	02	8	2.0	.80	0.0	5.0		0	70	Vectored Priority Interrupt Encoder	Z02-2	DL1g	AMV
18	Am2914XC	02	8	2.0	.80	0.0	5.0		0	70	Vectored Priority Interrupt Encoder	Z02-2	DL1g	AMV
19	Am2914XM	02	8	2.0	.80	0.0	5.0		55	125	Vectored Priority Interrupt Encoder	Z02-2	DL1g	AMV
20	Am8228DM	02	8	2.4	.45%	0.0	5.0	950m	55	125	Sys Controller/Driver For Am9080A	Z02-7	DL49	AMV
21	Am8228PC	02	8	2.4	.45%	0.0	5.0	950m	0	70	Sys Controller/Driver For Am9080A	Z02-7	DL67b	AMV
22	Am8228XC	02	8	2.4	.45%	0.0	5.0	950m	0	70	Sys Controller/Driver For Am9080A	Z02-7	CH3	AMV
23	Am8238DM	02	8	2.4	.45%	0.0	5.0	950m	55	125	Sys Controller/Driver For Am9080A	Z02-7	DL49	AMV
24	Am8238PC	02	8	2.4	.45%	0.0	5.0	950m	0	70	Sys Controller/Driver For Am9080A	Z02-7	DL67b	AMV
25	Am8238XC	02	8	2.4	.45%	0.0	5.0	950m	0	70	Sys Controller/Driver For Am9080A	Z02-7	CH3	AMV
26	Am9519-1CC	02	8	2.0	.80	0.0	5.0	625m	0	70	Universal Interrupt Controller	Z02-21	DL143	AMV
27	Am9519-1DC	02	8	2.0	.80	0.0	5.0	625m	0	70	Universal Interrupt Controller	Z02-21	DL182	AMV
28	Am9519-1PC	02	8	2.0	.80	0.0	5.0	625m	0	70	Universal Interrupt Controller	Z02-21	DL181	AMV
29	Am9519CC	02	8	2.0	.80	0.0	5.0	625m	0	70	Universal Interrupt Controller	Z02-21	DL143	AMV
30	Am9519DC	02	8	2.0	.80	0.0	5.0	625m	0	70	Universal Interrupt Controller	Z02-21	DL182	AMV
31	Am9519DM	02	8	2.0	.80	0.0	5.0	625m	55	125	Universal Interrupt Controller	Z02-21	DL182	AMV
32	Am9519PC	02	8	2.0	.80	0.0	5.0	625m	0	70	Universal Interrupt Controller	Z02-21	DL181	AMV
33	D8238	02	8	2.4	.45%	0.0	5.0	950m	0	70	Sys Controller/Driver For Am9080A	Z02-7	DL49	AMV
34	mN613	02	16	2.5	.50	5.0	12	615m†	0	70	Interprets and Executes I/O Instr	Z02-18	DL1r	DGC
35	HD6101-2	02	12	4.9	1.4	0.0	7.0	7.0m	50	125	CMOS Parallel Interface Element	Z02-4	DL1	HAS
36	HD6101-9	02	12	4.9	1.4	0.0	7.0	7.0m	40	85	CMOS Parallel Interface Element	Z02-4	DL1	HAS
37	HD6101A-2	02	12	7.7	2.2	0.0	11	11m	50	125	CMOS Parallel Interface Element	Z02-4	DL1	HAS
38	HD6101A-9	02	12	7.7	2.2	0.0	11	11m	40	85	CMOS Parallel Interface Element	Z02-4	DL1	HAS
39	IM6101-1IDL	02	12	3.0	.80	0.0	5.0	2.5m	40	85	CMOS Progr Interface;TTL Compatible	Z02-3	DL37a	INL
40	IM6101-1IPL	02	12	3.0	.80	0.0	5.0	2.5m	40	85	CMOS Progr Interface;TTL Compatible	Z02-3	DL86	INL
41	IM6101-1MDL	02	12	3.0	.80	0.0	5.0	2.5m	55	125	CMOS Progr Interface;TTL Compatible	Z02-3	DL37a	INL
42	IM6101AIDL	02	12	7.0	2.0	0.0	10	20m	40	85	CMOS Progr Interface;TTL Compatible	Z02-3	DL37a	INL
43	IM6101AIPL	02	12	7.0	2.0	0.0	10	20m	40	85	CMOS Progr Interface;TTL Compatible	Z02-3	DL86	INL
44	IM6101AMDL	02	12	7.0	2.0	0.0	10	20m	55	125	CMOS Progr Interface;TTL Compatible	Z02-3	DL37a	INL
45	IM6101IPL	02	12	3.0	.80	0.0	5.0	2.5m	40	85	CMOS Progr Interface;TTL Compatible	Z02-3	DL86	INL
46	C3214	02	4	2.0	.80	0.0	5.0	650m	0	75	Interrupt Control Unit	Z02-6	DL34	ITL
47	C8214	02	8R	2.0	.80	0.0	5.0	650m	0	70	Priority Interrupt Control Unit	Z02-6	DL39	ITL
48	C8228	02	8	2.4	.45%	0.0	5.0	950m	0	70	Controller And Bus Driver	Z02-10	DL36	ITL
49	C8238	02	8	2.4	.45%	0.5	7.0	950mØ	0	70	System Controller/Driver for MCS80	Z02-7	DL36	ITL
50	C8259A	02		2.0		0.5	7.0	1.0 Ø	40	85	Prog Interrupt Controller	Z02-9	DL146	ITL
51	C8259A-2	02		2.0		0.5	7.0	1.0 Ø	40	85	Prog Interrupt Controller	Z02-9	DL146	ITL
52	C8259A-8	02		2.0		0.5	7.0	1.0 Ø	40	85	Prog Interrupt Controller	Z02-9	DL146	ITL
53	C8288	02		2.0	.80§	0.0	5.0	1.5 Ø	0	70	Bus Controller for 8086;Cl Pd 125ns	Z02-14	DL212	ITL
54	D3214	02	4	2.0	.80	0.0	5.0	650m	0	75	Interrupt Control Unit	Z02-6	DL7a	ITL
55	D8214	02	8R	2.0	.80	0.0	5.0	650m	0	70	Priority Interrupt Control Unit	Z02-6	DL6a	ITL
56	D8228	02	8	2.4	.45%	0.0	5.0	950m	0	70	Controller And Bus Driver	Z02-10	DL35	ITL
57	D8259	02	8	2.0	.80	0.0	5.0	500m	0	70	Progm Interrupt Controller,Cer Pkg	Z02-9	DL35	ITL
58	D8259-5	02	8	2.0	.80	0.0	5.0	500m	0	70	Progm Interrupt Controller,Cer Pkg	Z02-9	DL35	ITL
59	D8259A	02	8	2.0	.80	0.0	5.0	425m	0	70	Progm Interrupt Controller,RD 235ns	Z02-15	DL35	ITL
60	D8259A-2	02		2.0		0.5	7.0	1.0 Ø	40	85	Prog Interrupt Controller	Z02-9	DL147	ITL
61	D8259A-8	02	8	2.0	.80	0.0	5.0	425m	0	70	Progm Interrupt Controller,RD 420ns	Z02-15	DL35	ITL
62	D8288	02		2.0	.80§	0.0	5.0	1.5 Ø	0	70	Bus Controller for 8086;Cl Pd 125ns	Z02-14	DL211	ITL
63	MD3214	02	4	2.0	.80	0.0	5.0	650m	55	125	Interrupt Control Unit	Z02-6	DL7a	ITL
64	MD8214	02	8	2.0	.80	0.0	5.0	650m	55	125	Priority Interrupt Control Unit	Z02-6	DL7a	ITL
65	P3214	02	4	2.0	.80	0.0	5.0	650m	0	75	Interrupt Control Unit	Z02-6	DL14a	ITL
66	P8214	02	8R	2.0	.80	0.0	5.0	650m	0	70	Priority Interrupt Control Unit	Z02-6	DL33	ITL
67	P8228	02	8	2.4	.45%	0.0	5.0	950m	0	70	Controller And Bus Driver	Z02-10	DL43	ITL
68	P8259	02	8	2.0	.80	0.0	5.0	500m	0	70	Progm Interrupt Controller,Plas Pkg	Z02-9	DL43	ITL
69	P8259-5	02	8	2.0	.80	0.0	5.0	500m	0	70	Progm Interrupt Controller,Plas Pkg	Z02-9	DL43	ITL
70	P8259A	02	8	2.0	.80	0.0	5.0	425m	0	70	Progm Interrupt Controller,RD 235ns	Z02-15	DL43	ITL
71	P8259A-2	02		2.0		0.5	7.0	1.0 Ø	40	85	Prog Interrupt Controller	Z02-9	DL181	ITL
72	P8259A-8	02	8	2.0	.80	0.0	5.0	425m	0	70	Progm Interrupt Controller,RD 420ns	Z02-15	DL43	ITL
73	P8288	02		2.0	.80§	0.0	5.0	850m	0	70	Bus Controller for 8086,Cl Pd 125ns	Z02-14	DL118	ITL
74#	M54551K	02	8	2.0	.80	0.0	5.0	1.0 Ø	0	75	Syst Controller and Bus Driver	Z02-10	DL126	MITJ
75	MC6828L	02	8	2.0	.80	0.0	5.0	625m	0	75	Priority Interrupt Controller	Z02-17	DL68	MOTA
76	MC6828P	02	8	2.0	.80	0.0	5.0	625m	0	75	Priority Interrupt Controller	Z02-17	DL69	MOTA
77#	uPB8214C	02	8	2.0	.80	0.0	5.0	650m	0	70	Priority Interrupt Controller	Z02-6	DL18e	NECJ
78#	uPB8228C	02	8	2.4	.45%	0.0	5.0		0	70	8080A Controller For Small Mem Sys	Z02-8	DL67	NECJ
79#	uPB8228D	02	8	2.4	.45%	0.0	5.0		0	70	8080A Controller For Small Mem Sys	Z02-8	DL57	NECJ
80#	uPB8238C	02	8	2.4	.45%	0.0	5.0		0	70	8080A Controller For Large Mem Sys	Z02-8	DL67	NECJ
81▼	uPB8214	02	8R	2.0	.80	0.0	5.0		0	70	Priority Interrupt Controller	Z02-6	DL102	NECM
82	uPB8238D	02		2.4	.45%	0.0	5.0	950m	0	70	8080A Controller For Large Mem Sys	Z02-8	DL57	NECM
83#	uPD8259C	02	8	2.0	.80	0.0	5.0	500m	0	70	Progm Interrupt Controller	Z02-9	DL67	NECM
84	uPD8259D	02	8	2.0	.80	0.0	5.0	500m	0	70	Progm Interrupt Controller	Z02-9	DL172	NECM
85#	MN1630	02	8	2.4	.80	3.0	12	1.0	30	125	Subchannel Adapter	Z02-11	DL48	PAFJ
86#	MN1640	02		2.4	.80	0.0	5.0	500m	30	125	Real Time System Controller		DL48	PAFJ
87	SBP9961CJ	02	15R	2.0	.80	0.0	5.0	797m	0	70	Interrupt Controller/Timer	Z02-16		TII
88	SBP9961EJ	02	15R	2.0	.80	0.0	5.0	797m	40	85	Interrupt Controller/Timer	Z02-16		TII
89	SBP9961MJ	02	15R	2.0	.80	0.0	5.0	797m	55	125	Interrupt Controller/Timer	Z02-16		TII
90	SN74S428N	02	8	2.0	.80	0.0	5.0	950m	0	70	Controller/Bus Driver For 8080A Syst	Z02-12	DL24	TII
91	SN74S438N	02	8	2.0	.80	0.0	5.0	950m	0	70	Controller/Bus Driver For 8080A Sys	Z02-12	DL24	TII
92	TIM9907J	02	4L	2.0	.80	0.0	5.0	315m	0	70	10-Line Decimal to 4-Line BCD Encode	Z02-19		TII
93	TIM9907N	02	4L	2.0	.80	0.0	5.0	315m	0	70	10-Line Decimal to 4-Line BCD Encode	Z02-19		TII
94	TIM9908J	02	3L	2.0	.80§	0.0	5.0	131m	0	70	Encodes 8 Lines to 3-Line Bin(Octal)	Z02-20		TII
95	TIM9908N	02	3L	2.0	.80§	0.0	5.0	131m	0	70	Encodes 8 Lines to 3-Line Bin(Octal)	Z02-20		TII
96	Am2940DC	03	8	2.0	.80	0.0	5.0	1.4	0	70	4 Contr Modes;8 DMA Instructions	Z03-23	DL143	AMV
97	Am2940DM	03	8	2.0	.80	0.0	5.0	1.6	55	125	4 Contr Modes;8 DMA Instructions	Z03-23	DL143	AMV
98	Am2940FM	03	8	2.0	.80	0.0	5.0	1.6	55	125	4 Contr Modes;8 DMA Instructions	Z03-23	FP5a	AMV
99	Am2940PC	03	8	2.0	.80	0.0	5.0	1.4	0	70	4 Contr Modes;8 DMA Instructions	Z03-23	DL143a	AMV
100	Am2942DC	03	8	2.0	.80	0.0	5.0	1.3	0	70	4 Contr Modes;16 Instr;8 Tim/Count	Z03-24	DL150	AMV
101	Am2942DM	03	8	2.0	.80	0.0	5.0	1.4	55	125	4 Contr Modes;16 Instr;8 Tim/Count	Z03-24	DL150	AMV
102	Am2942FM	03	8	2.0	.80	0.0	5.0	1.4	55	125	4 Contr Modes;16 Instr;8 Tim/Count	Z03-24	FP18	AMV
103	Am2942PC	03	8	2.0	.80	0.0	5.0	1.3	0	70	4 Contr Modes;16 Instr;8 Tim/Count	Z03-24	DL5f	AMV
104	Am9517-1PC	03	8	2.0	.80	0.0	5.0	650m	0	70	Multimode DMA Contoller;3MHz Clock	Z03-27	DL179	AMV
105	Am9517-4DC	03	8	2.0	.80	0.0	5.0	650m	0	70	Multimode DMA Controller;4MHz Clockk	Z03-27	DL180	AMV
106	Am9517-4PC	03	8	2.0	.80	0.0	5.0	650m	0	70	Multimode DMA Controller;4MHz Clock	Z03-27	DL179	AMV
107	Am9517DC	03	8	2.0	.80	0.0	5.0	650m	0	70	Multimode DMA Controller;3MHz Clock	Z03-27	DL180	AMV
108	Am9517DM	03	8	2.0	.80	0.0	5.0	650m	55	125	Multimode DMA Contoller;3MHz Clock	Z03-27	DL180	AMV
109	Am9517PC	03	8	2.0	.80	0.0	5.0	650m	0	70	Multimode DMA Contoller;3MHz Clock	Z03-27	DL179	AMV
110	mN506	03	4D	2.0	.50	5.0	5.0	600m	0	70	Quad Sense Ampl;RAM to Memory Bus	Z03-17	DL82	DGC

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ☑-ABS.MAX. %-OUTPUT

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1	DT2771	03	12			0.0	5.0	1.0 †			2 Ch/12 Bit D/A;18 Bit Memory Adder	Z03-34		DTI
2	DT2782	03	12			0.0	5.0	7.5	0	70	16 Ch/12 Bit A/D Sys;±10V Analog In	Z03-35		DTI
3	DT2784	03	12			0.0	5.0	7.5	0	70	16 Ch/12 Bit A/D Sys;±10V Analog In	Z03-35		DTI
4	3852	03	8	3.5	.80	0.0	12	710m	0	70	Dynamic Memory Interface:To RAM	Z03-2		FSC
5	3853	03	8	3.5	.80	0.0	12	710m	0	70	Static Memory Interface	Z03-3		FSC
6	3854	03	8	3.5	.80	0.0	12	536m	0	70	Direct Memory Access	Z03-4		FSC
7#	HD46504RP-1	03	2P	2.0	.80	0.0	5.0	1.0	20	75	DMA Controller;Speed 1.5MHz			HITJ
8	IM6102-1IDL	03	12	3.0	1.0	0.0	5.0	10m	40	85	Mem Extension/DMA/Int Timer/Control	Z03-15	DL37a	INL
9	IM6102-1IPL	03	12	3.0	1.0	0.0	5.0	10m	40	85	Mem Extension/DMA/Int Timer/Control	Z03-15	DL86	INL
10	IM6102-1MDL	03	12	3.0	.80	0.0	5.0	10m	55	125	Mem Extension/DMA/Int Timer/Control	Z03-15	DL37a	INL
11	IM6102AIDL	03	12	7.0	2.0	0.0	10	40m	40	85	Mem Extension/DMA/Int Timer/Control	Z03-15	DL37a	INL
12	IM6102AIPL	03	12	7.0	2.0	0.0	10	40m	40	85	Mem Extension/DMA/Int Timer/Control	Z03-15	DL86	INL
13	IM6102AMDL	03	12	7.0	2.0	0.0	10	40m	55	125	Mem Extension/DMA/Int Timer/Control	Z03-15	DL37a	INL
14	IM6102IPL	03	12	3.0	.80	0.0	5.0	9.0m	40	85	Mem Extension/DMA/Int Timer/Control	Z03-15	DL86	INL
15	C7220	03	9			0.0	5.0		0	70	Bubble Memory Controller	Z03-38	DL70	ITL
16	C8089	03	16	2.0	.80	0.0	5.0	2.5 ☑	0	70	8/16-Bit I/O Processor;1MByte Addr	Z03-26	DL148	ITL
17	C8202	03	18	2.2	.80	0.0	5.0	1.4 ☑	0	70	Dynamic RAM Controller Z03-37	Z03-37	DL70	ITL
18	C8237	03		2.0	.80	0.5	7.0	1.5 ☑	0	70	Prog DMA Controller	Z03-27	DL70	ITL
19	C8237-2	03		2.0	.80	0.5	7.0	1.5 ☑	0	70	Prog DMA Controller	Z03-27	DL70	ITL
20	C8257	03		2.0	.80	0.5	7.0	1.0 ☑	0	70	Prog DMA Controller	Z03-13	DL70	ITL
21	C8257-5	03		2.0	.80	0.5	7.0	1.0 ☑	0	70	Prog DMA Controller	Z03-13	DL70	ITL
22	D7220	03	9			0.0	5.0		0	70	Bubble Memory Controller	Z03-38	DL148	ITL
23	D8089	03	16	2.0	.80	0.0	5.0	1.7	0	70	8/16-Bit I/O Processor;1M Byte Addr	Z03-26	DL175	ITL
24	D8202	03	18	2.0	.80	0.0	5.0	1.2	0	70	Dynamic RAM Controller		DL38	ITL
25	D8237	03		2.0	.80	0.5	7.0	1.5 ☑	0	70	Prog DMA Controller	Z03-27	DL148	ITL
26	D8237-2	03		2.0	.80	0.5	7.0	1.5 ☑	0	70	Prog DMA Controller	Z03-27	DL148	ITL
27	D8257	03	8	2.0	.80	0.0	5.0	600m	0	70	Progm DMA Controller,tRD 300ns Max	Z03-13	DL38	ITL
28	D8257-5	03	8	2.0	.80	0.0	5.0	600m	0	70	Progm DMA Controller,tRD 200ns Max	Z03-13	DL38	ITL
29	P4289	03	4	3.5	.80	10	5.0	400m	0	70	Standard Memory Interface	Z03-1	DL42	ITL
30	P7220	03	9			0.0	5.0		0	70	Bubble Memory Controller	Z03-38	DL149	ITL
31	P8089	03	16	2.0	.80	0.0	5.0	2.5 ☑	0	70	8/16-Bit I/O Processor;1MByte Addr	Z03-26	DL149	ITL
32	P8202	03	18	2.2	.80	0.0	5.0	1.4 ☑	0	70	Dynamic RAM Controller	Z03-37	DL149	ITL
33	P8237	03		2.0	.80	0.5	7.0	1.5 ☑	0	70	Prog DMA Controller	Z03-27	DL149	ITL
34	P8237-2	03		2.0	.80	0.5	7.0	1.5 ☑	0	70	Prog DMA Controller	Z03-27	DL149	ITL
35	P8257	03	8	2.0	.80	0.0	5.0	600m	0	70	Progm DMA Controller,tRD 300ns Max	Z03-13	DL42f	ITL
36	P8257-5	03	8	2.0	.80	0.0	5.0	600m	0	70	Progm DMA Controller,tRD 200ns Max	Z03-13	DL42f	ITL
37▼#	M5L8257P	03	4C	2.0	.80	0.0	5.0	1.0	0	70	Programmable DMA Controller	Z03-13	DL123	MITJ
38▼#	M5L8257P-5	03	4C	2.0	.80	0.0	5.0	1.0	0	70	Programmable DMA Controller	Z03-13	DL123	MITJ
39	MC3480L	03	8	2.0	.80	0.0	5.0	350m	0	70	Dyn Memory Controller	Z03-21	DL68	MOTA
40	MC3480P	03	8	2.0	.80	0.0	5.0	350m	0	70	Dyn Memory Controller	Z03-21	DL69	MOTA
41	MC6844L	03		2.0	.80	0.0	5.0	500m	0	70	DMA Controller;Transfer Rate 1MB/s	Z03-20	DL1d	MOTA
42	MC6844P	03		2.0	.80	0.0	5.0	500m	0	70	DMA Controller;Transfer Rate 1MB/s	Z03-20	DL27	MOTA
43	MC10803	03	4	-1.1	-1.4	5.2	0.0	1.5 †	30	85	MECL-LSI Memory Interface Function	Z03-10	DL55	MOTA
44#	uPD8257C	03	8	2.0	.80	0.0	5.0	600m	0	70	Progm DMA Controller	Z03-13	DL11c	NECJ
45	uPD8257C-5	03		2.0	.80	0.0	5.0	1.0 ☑	0	70	TRDE 200nS Max;TAFDB 170nS Max		DL101	NECM
46	MM5785	03	10	8.3	5.5	9.5	0.0	135m	0	70	RAM Interface Chip	Z03-19	DL67c	NSC
47#	MN1650	03	4D	2.4	.80	3.0	12	1.0	30	125	DMA Channel Controller	Z03-9	DL48	PAFJ
48	10817	03	8P	3.5	-12	12	5.0	400m	0	70	Direct Memory Access Controller	Z03-11	DL44	RKW
49	10929	03	4	-12	3.5	12	5.0	330m	0	70	4k RAM Interface	Z03-8	DL44	RKW
50	TMS9901-40JL	03		2.0	.80	0.0	5.0	750m	0	70	Programmable System Inter Ceramic	Z30-13	DL1a	TII
51	TMS9901-40NL	03		2.0	.80	0.0	5.0	750m	0	70	Programmable System Inter Plastic	Z30-13	DL11	TII
52	TMS9911-40JL	03	16	2.2	.80	0.0	5.0	700m	0	70	DMA Controller for 2 Indep Devices	Z03-22	DL1a	TII
53	TMS9911JL	03									DMA Controller for 2 Indep Devices	Z03-22		TII
54	TMS9911NL	03									DMA Controller for 2 Indep Devices	Z03-22		TII
55	DM1883A	03	8	2.0	.80	0.0	5.0	450m	0	70	DMA Controller;Max Clock f 2.0MHz	Z03-25	DL160	WDC
56	DM1883B	03	8	2.0	.80	0.0	5.0	450m	0	70	DMA Controller;Max Clock f 2.0MHz	Z03-25	DL161	WDC
57	Z80-DMACE	03	8	2.0	.80	0.0	5.0	750m	40	85	Direct Mem Access;4 Modes;Cer Pkg	Z03-14	DL1k	ZIL
58	Z80-DMACM	03	8	2.0	.80	0.0	5.0	750m	55	125	Direct Mem Access;4 Modes;Cer Pkg	Z03-14	DL1k	ZIL
59	Z80-DMACS	03	8	2.0	.80	0.0	5.0	750m	0	70	Direct Mem Access;4 Modes;Cer Pkg	Z03-14	DL1k	ZIL
60	Z80-DMAPS	03	8	2.0	.80	0.0	5.0	750m	0	70	Direct Mem Access;4 Modes;Pl Pkg	Z03-14	DL1k	ZIL
61	Z80A-DMACS	03	8	2.0	.80	0.0	5.0	1.0	0	70	Direct Mem Access;4 Modes;Cer Pkg	Z03-14	DL1k	ZIL
62	Z80A-DMAPS	03	8	2.0	.80	0.0	5.0	1.0	0	70	Direct Mem Access;4 Modes;Pl Pkg	Z03-14	DL1k	ZIL
63	Z8010MMU	03		2.0	.80	0.0	5.0				Memory Management Unit	Z03-39		ZIL
64	uPD371D	05	8	3.0	.80	5.0	12	400m	0	70	Mag Tape Cassette Controller	Z05-1	DL58a	NECM
65#	HD46503SP-1	07	8	2.0	.80	0.0	5.0	800m	20	75	Floppy Disk Controller,Speed 1.5MHz			HITJ
66	C8271	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Floppy Disk Controller	Z07-5	DL70	ITL
67	C8271-6	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Floppy Disk Controller	Z07-5	DL70	ITL
68	C8271-8	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Floppy Disk Controller	Z07-5	DL70	ITL
69	C8272	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	FDC Single/Double Density	Z07-14	DL70	ITL
70	D8271	07	8	2.0	.80	0.0	5.0	800m	0	70	Progm Floppy Disk Controller	Z07-5	DL38	ITL
71	D8271-6	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Floppy Disk Controller	Z07-5	DL148	ITL
72	D8271-8	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Floppy Disk Controller	Z07-5	DL148	ITL
73	D8272	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	FDC Single/Double Density	Z07-14	DL148	ITL
74	P8271	07	8	2.0	.80	0.0	5.0	800m			Program Floppy Disk Controller	Z07-5	DL42f	ITL
75	P8271-6	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Floppy Disk Controller	Z07-5	DL149	ITL
76	P8271-8	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Floppy Disk Controller	Z07-5	DL149	ITL
77	P8272	07	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	FDC Single/Double Density	Z07-14	DL149	ITL
78	MC6843L	07		2.0	.80	0.0	5.0	400m	0	70	Floppy Disk Controller;3740 Comp	Z07-7	DL1d	MOTA
79	MC6843P	07		2.0	.80	0.0	5.0	400m	0	70	Floppy Disk Controller;3740 Comp	Z07-7	DL27	MOTA
80#	uPD765C	07		2.0	.80	0.0	5.0	750m	10	70	Floppy Disk Controller,3 State		DL101	NECJ
81	uPD372D	07		3.0	.80	5.0	12	365m	0	70	Floppy Disk Controller	Z07-3	DL58a	NECM
82	INS1771D-1	07	8	2.6	.80	5.0	12		0	70	Floppy Disk Formatter/Controller	Z07-6	DL37d	NSC
83	INS1771N-1	07	8	2.6	.80	5.0	12		0	70	Floppy Disk Formatter/Controller	Z07-6	DL11f	NSC
84	10936	07	8	-12	3.5	12	5.0	450m	0	70	Floppy Disk Controller	Z07-1	DL44	RKW
85▼	FDC1791	07	8			0.0	12				Floppy Disk Controller/Formatter	Z07-9	DL37e	SMC
86▼	FDC1792	07	8			0.0	12				Floppy Disk Controller/Formatter	DL37e	Z07-9a	SMC
87▼	FDC1793	07	8			0.0	12				Floppy Disk Controller/Formatter	Z07-9	DL37e	SMC
88▼	FDC1794	07	8			0.0	12				Floppy Disk Controller/Formatter	Z07-9a	DL37e	SMC
89	FDC3400	07		305	080	12	5.0	476m	0	70	HSDH;Prog Sync Byte;TTL I/O;§	Z07-11	DL☑	SMC
90	SY1791	07	8			0.0	5.0				Pin for Pin Replacement For FD1791	Z07-9		SYK
91	SY6591	07	8			0.0	5.0				6500/6800 Compat Funct Equiv FD1791	Z07-11		SYK
92	TM990/303	07				0.0	12	2.4	0	70	Use w/SA400/800,CDC9404B Disc Drives	Z07-13		TII
93	TMS9909JL	07	8			0.0	5.0				Floppy Disk Controller	Z07-8		TII
94	TMS9909NL	07	8			0.0	5.0				Floppy Disk Controller	Z07-8		TII
95▼	FD1771A-01	07	8	2.6	.80	0	12	500m	0	70	Soft Sector Format Capability	Z07-9	DL160	WDC
96	FD1771B	07	8			5.0	12		0	70	Floppy Disk Controller/Formatter	Z07-2		WDC
97▼	FD1771B-01	07	8	2.6	.80	0	12	500m	0	70	Soft Sector Format Capability	Z07-9	DL161	WDC
98	FD1781A	07	8	2.6	.80	0.0	12	270mt	0	70	FD Formatter/Controller,Double Den	Z07-10	DL160	WDC
99	FD1781B	07	8	2.6	.80	0.0	12	270mt	0	70	FD Formatter/Controller,Double Den	Z07-10	DL161	WDC
100	FD1791A	07	8	2.6	.80	0.0	12	295mt	0	70	FD Formatter/Control;Double Density	Z07-9	DL160	WDC
101▼	FD1791A-01	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL160	WDC
102▼	FD1791A-02	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL160	WDC
103	FD1791B	07	8	2.6	.80	0.0	12	295mt	0	70	FD Formatter/Control;Double Density	Z07-9	DL161	WDC
104▼	FD1791B-02	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL161	WDC
105	FD1792A	07	8	2.6	.80	0.0	12	295mt	0	70	FD Formatter/Control;Single Density	Z07-9a	DL160	WDC
106▼	FD1792A-01	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL160	WDC
107	FD1792B	07	8	2.6	.80	0.0	12	295mt	0	70	FD Formatter/Control;Single Density	Z07-9a	DL161	WDC
108▼	FD1793A-01	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL160	WDC
109▼	FD1793A-02	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL161	WDC
110▼	FD1793B-02	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL161	WDC

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ∅-ABS.MAX. %-OUTPUT

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1▼	FD1794A-01	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL160	WDC
2▼	FD1795A-02	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL160	WDC
3▼	FD1795B-02	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL161	WDC
4▼	FD1797A-02	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL160	WDC
5▼	FD1797B-02	07	8	2.6	.80	0	12	500m	0	70	Two VFO Control Signals	Z07-9	DL161	WDC
6▼	WD1000	07	8			0.0	5.0				256 BYTE Buffer;Control to 4 Drives			WDC
7	C8295	08	8	2.0	.80	0.0	5.0		0	70	Dot Matrix Printer Controller	Z08-6	DL70	ITL
8	D8295	08	8	2.0	.80	0.0	5.0		0	70	Dot Matrix Printer Controller	Z08-6	DL148	ITL
9	P8295	08	8	2.0	.80	0.0	5.0		0	70	DOT Matrix Printer Controller	Z08-6	DL42f	ITL
10	uPD758C	08		3.0	.80	5.0	12	340m	0	70	Printer Controller;18 Instructions	Z08-3	DL59	NECM
11	MM5788	08	20L	8.5	5.5	9.5	0.0	90m	0	70	Printer Interface Chip	Z08-4	DL11f	NSC
12	10736,15380	08		-12	3.5	12	5.0	330m	0	70	Victor Dot Matrix Printer Controller	Z08-2	DL44	RKW
13	10789	08	8	3.5	-12	12	5.0	200m	0	70	Printer Control	Z08-1	DL44	RKW
14	R6592	08	7	2.0	.80	0.0	5.0	500m	0	70	for Epson Dot Matrix Impact Print	Z08-7	DL∅	RKW
15	RC7000	08	4	3.5	.80	10	5.0	75m†	0	70	LRC Dot Matrix Printer Controller	Z08-5	DL∅	RKW
16#	MMD256	09	16	2.0	.80§	0.0	5.0	2.5	0	70	256 x 256 Dots CRT Controller Module		MD2r	
17#	MMD256D	09	16			0.0	12	3.2	0	70	256 x 256 Dots CRT Controller Module		MD2r	
18	S68045	09	8			0.0	5.0				For Use With Raster Scan Display	Z09-30		AMI
19	S68047	09	8	2.0	.60	0.0	5.0	225m†	0	70	Video Display Generator,fvc 6.4MHz	Z09-19	DL1n	AMI
20	HCMP1861CD	09	8			0.0	5.0	500m∅	55	125	Programmable Crt Controller	Z09-12	Δ015AG	HAC
21#	HD46505RP	09	8	2.0	.80	0.0	5.0	1.0	20	75	Same as HD46505R But in Plastic Pkg	Z09-6	DL∅	HITJ
22#	HD46505SP-1	09	8	2.0	.80	0.0	5.0	1.0	20	75	CRT Controller, Speed 1.5MHz			HITJ
23#	HD46505SP-2	09	8	2.0	.80	0.0	5.0	1.0	20	75	CRT Controller,Speed 2.0MHz			HITJ
24	C8275	09	8	2.0	.80	0.0	5.0	800m	0	70	Progm CRT Controller	Z09-7	DL37	ITL
25	D8275	09	8	2.0	.80	0.0	5.0	1.0 ∅	0	70	Prog CRT Controller	Z09-7	DL148	ITL
26	P8275	09	8			0.0	5.0				Program CRT Controller	Z09-7	DL42f	ITL
27#	MTX256-2	09	8	2.0	.70	0.0	5.0		0	70	TV CRT Control;256x256 Dot Raster	Z09-5	MD2m	MAT
28#	MTX816	09	8	3.5	.80	0.0	5.0	1.2	0	70	TV CRT Controller;8x16 Fld,128x8 RAM	Z09-2	MD2n	MAT
29#	MTX1632	09	8	2.0	.70	0.0	5.0	3.0	0	70	TV CRT Control;16x32 Fld,512x8 RAM	Z09-3	MD2p	MAT
30#	MTX1632SL	09	8	2.0	.70	0.0	5.0	3.0	0	70	TV CRT Control;16x32 Fld,512x8 RAM	Z09-3	MD2p	MAT
31#	MTX1648/64SL	09	8	2.0	.70	0.0	5.0	3.0	0	70	TV CRT Controller;16x64 Fld;1kx8 RAM	Z09-10	MD2r	MAT
32#	MTX2064	09	8	2.0	.70	0.0	5.0	3.0	0	70	TV CRT Controller;20x64 Field	Z09-9	MD∅	MAT
33#	MTX2480	09	8	2.0	.70	0.0	5.0	7.5	0	70	TV CRT Control;24x80 Fld,4096x9 RAM	Z09-4	MD2k	MAT
34#	MTX-A1	09	8	2.0	.80	0.0	5.0	675m	0	70	Alphanum Displ/KB Controller;Dot Mat	Z09-11	DL∅	MAT
35#	MTX-B1	09	8	2.0	.80	0.0	5.0	675m	0	70	Alphanum Disp/KB Cont;7 or 14x16Seg		DL∅	MAT
36#	MN1205A	09	4	2.4	.80	0.0	5.0	15m	30	70	Numeric Display Decoder/Driver	Z09-25a	DL166	MATJ
37#	MN1205D	09	4	2.4	.80	0.0	5.0	15m	30	70	Numeric Display Decoder/Driver	Z09-25	DL67a	MATJ
38#	MN1205E	09	4	2.4	.80	0.0	5.0	15m	30	70	Numeric Display Decoder/Driver	Z09-25	DL67a	MATJ
39#	MN1205F	09	4	2.4	.80	0.0	5.0	15m	30	70	Numeric Display Decoder/Driver		DL165	MATJ
40#	MN1205G	09	4	2.4	.80	0.0	5.0	15m	30	70	Numeric Display Decoder/Driver	Z09-25	DL67a	MATJ
41#	MN1205H	09	4	2.4	.80	0.0	5.0	15m	30	70	Numeric Display Decoder/Driver	Z09-25	DL67a	MATJ
42#	MN1205P	09	4	2.4	.80	0.0	5.0	15m	30	70	Numeric Display Decoder/Driver	Z09-25	DL67a	MATJ
43#	MN1205Q	09	4	2.4	.80	0.0	5.0	15m	30	70	Numeric Display Decoder/Driver	Z09-25	DL67a	MATJ
44	MMI6051/6052J	09	5L			0.0	5.0	525m	0	75	5x7 Character Gen,Row Scan,2 Chips	Z09-15	DL∅	MMI
45	MC6845L	09		2.0	.80	0.0	5.0	600m	0	70	CRT Controller;Progm Scan	Z09-21	DL1d	MOTA
46	MC6845P	09		2.0	.80	0.0	5.0	600m	0	70	CRT Controller;Progm Scan	Z09-21	DL27	MOTA
47	MC6847L	09		2.0	.80	0.0	5.0		0	70	Video Display Generator;fc 3.58MHz	Z09-20	DL1d	MOTA
48	MC6847P	09		2.0	.80	0.0	5.0		0	70	Video Display Generator;fc 3.58MHz	Z09-20	DL27	MOTA
49	MC6847YL	09		2.0	.80	0.0	5.0		0	70	Video Display Generator;fc 3.58MHz	Z09-20	DL1d	MOTA
50	MC6847YP	09		2.0	.80	0.0	5.0		0	70	Video Display Generator;fc 3.58MHz	Z09-20	DL27	MOTA
51	MCS6560	09	8	2.4	.40	0.0	5.0	500m	0	70	Video Interface Controller			MTY
52	uPD781C	09	8	2.0	.80	0.0	5.0	675m	9	70	Dot Matrix Printer Controller Z	Z09-32	DL101	NECM
53	uPD782C	09	8	2.0	.80	0.0	5.0	675m	9	70	Dot Matrix Printer Controller			NECM
54	uPD3301-1C	09		2.2	.80	0.0	5.0	450m†	0	70	Programmable CRT Cont;tCY .5uS min	Z09-36	DL101	NECM
55	uPD3301-1D	09		2.2	.80	0.0	5.0	450m†	0	70	Programmable CRT Cont;tCY .5uS min	Z09-366	DL1	NECM
56	uPD3301-2C	09		2.2	.80	0.0	5.0	450m†	0	70	Programmable CRT Cont;tCY .38uS min	Z09-36	DL101	NECM
57	uPD3301-2D	09		2.2	.80	0.0	5.0	450m†	0	70	Programmable CRT Cont;tCY .38uS min	Z09-36	DL1	NECM
58	DP8350D	09	12	2.0	.80	0.0	5.0	850m†	0	70	Programmable CRT Controller	Z09-23	DL37d	NSC
59	DP8350N	09	12	2.0	.80	0.0	5.0	850m†	0	70	Programmable CRT Controller;40PinDIL	Z09-23	DL63	NSC
60	CDP1861CD	09	8			0.0	5.0	500m∅	55	125	Vid Display Cont R/T Interrupt Gen	Z09-12	Δ015AG	RCA
61▼	CDP1861CE	09				0.0	5.0	500m∅	40	85	Vid Display Cont R/T Interrupt Gen	Z09-12	Δ015AA	RCA
62	CDP1862CD	09		3.5	1.5	0.5	7.0	500m	55	125	Color Generator Controller	Z09-33	DL137	RCA
63	CDP1862CE	09		3.5	1.5	0.5	7.0	500m	40	85	Color Generator Controller	Z09-33	Δ015AA	RCA
64	CDP1862D	09		3.5	1.5	0.5	7.0	500m	55	125	Color Generator Controller	Z09-33	DL137	RCA
65	CDP1862E	09		3.5	1.5	0.5	7.0	500m	40	85	Color Generator Controller	Z09-33	Δ015AA	RCA
66	CDP1864CD	09	8	3.5	1.5	0.5	7.0	500m	55	1255	Color TV Interface Pal Compatible	Z09-34	DL221	RCA
67	CDP1864CE	09	8	3.5	1.5	0.5	7.0	500m	40	85	Color TV Interface Pal Compatible	Z09-34	DL220	RCA
68	10814	09		3.5	-12	12	5.0	200m	0	70	Display Controller	Z09-1	DL44	RKW
69	R6545	09	8	2.0	.80	0.0	5.0				CRT Controller,2.0M/1.0MHz Operation	Z09-24	DL26	RKW
70	R6545AC	09	8	2.0	.80	0.0	5.0	700m	0	70	CRT Controller 2.0 MHz Operation	Z09-24	DL26	RKW
71	R6545AP	09	8	2.0	.80	0.0	5.0	700m	0	70	CRT Controller 2.0MHz Operation	Z09-24	DL26	RKW
72	R6545C	09	8	2.0	.80	0.0	5.0	700m		70	CRT Controller 1.0MHz Operation	Z09-24	DL26	RKW
73	R6545P	09	8	2.0	.80	0.0	5.0	700m	0	70	CRT Controller 1.0MHz Operation	Z09-24	DL26	RKW
74	CRT5027	09	8	3.5	.80	0.0	12	1.2	0	70	CRT Video Time Controller VTAC	Z09-8	DL∅	SMC
75	CRT5037	09	8	3.5	.80	0.0	12	1.2	0	70	CRT Video Timer-Controller	Z09Ω29	DL∅	SMC
76▼	CRT5047	09	2D			0.0	12				Preprog Video Timer/ControllerZ09-29	Z09-29	DL37e	SMC
77	CRT5057	09	8	3.5	.80	0.0	12	1.2	0	70	CRT Video Timer-Controller	Z09-29	DL∅	SMC
78	CRT8002A	09		2.0	.80	0.0	5.0	500m	0	70	Video Display Controller-Generator	Z09-27	DL∅	SMC
79	CRT8002B	09		2.0	.80	0.0	5.0	500m	0	70	Video Display Controller-Generator	Z09-27	DL∅	SMC
80	CRT8002C	09		2.0	.80	0.0	5.0	500m	0	70	Video Display Controller-Generator	Z09-27	DL∅	SMC
81▼	CRT9007	09	8			0.0	5.0				CRT Video Processor/Controller		DL37e	SMC
82	CRT96364A	09	16L	2.2	.65	0.0	5.0	500m	0	70	CRT Control;Comp CRT 8002,CRT7004	Z09-28	DL∅	SMC
83	SY6545	09		2.0	.80	0.0	5.0	500m	0	70	CRT Controller,tACR 395ns Max	Z09-22	DL∅	SYK
84	SY6545A	09		2.0	.80	0.0	5.0	500m	0	70	CRT Controller,tACR 200ns Max	Z09-22	DL∅	SYK
85	TMS9927JL	09	8	2.0	.80						Video Timer/Controller;Cer Pkg	Z09-26	DL1a	TII
86	TMS9927NL	09	8	2.0	.80						Video Timer/Controller;Plas Pkg	Z09-26	DL11	TII
87	Am8279-5CC	10	8	2.0	.80	0.0	5.0	600m	0	70	trr 250ns;Clock Period 320ns		DL178	AMV
88	Am8279-5PC	10	8	2.0	.80	0.0	5.0	600m	0	70	trr 250ns;Clock Period 320ns		DL179	AMV
89	Am8279CC	10	8	2.0	.80	0.0	5.0	600m	0	70	TRR 420ns;Clock Period 500ns	Z10	DL178	AMV
90	Am8279PC	10	8	2.0	.80	0.0	5.0	600m	0	70	trr 420ns;Clock Period 500ns		DL179	AMV
91	C8279	10	8	2.0	.80	0.0	5.0	1.0 ∅	0	70	Prog Keyboard/Display Interface	Z10-2	DL70	ITL
92	C8279-5	10	8	2.0	.80	0.0	5.0	1.0 ∅	0	70	Prog Keyboard/Display Interface	Z10-2	DL70	ITL
93	D8278	10	8	2.0	.80	0.0	5.0	1.5 ∅	0	70	Progm Keyboard Interface,Cer Pkg	Z10-7	DL38	ITL
94	D8279	10	8	2.0	.80	0.0	5.0	600m	0	70	Program Keyboard/Display Interface	Z10-2	DL38	ITL
95	D8279-5	10	8	2.0	.80	0.0	5.0	600m	0	70	Program Keyboard/Display Interface	Z10-2	DL38	ITL
96	P8278	10	8	2.0	.80	0.0	5.0	1.5 ∅	0	70	Progm Keyboard Interface,Plas Pkg	Z10-7	DL42f	ITL
97	P8279	10	8	2.0	.80	0.0	5.0	600m	0	70	Program Keyboard/Display Interface	Z10-2	DL42f	ITL
98	P8279-5	10	8	2.0	.80	0.0	5.0	600m	0	70	Program Keyboard/Display Interface	Z10-2	DL42f	ITL
99#	M58609-XXS	10		4.0	.80	12	5.0	200m	20	75	Keyboard Encoder,Clock 100kHz Max	Z10-8	DL122	MITJ
100#	M58620-XXXS	10		3.5	1.5	12	5.0	500m	20	75	Keyboard Encoder,Has CE Terminal	Z10-9	DL122	MITJ
101▼	CDP1871CD	10	8	3.5	1.5§	0.0	6.5	500m∅	55	125	Keyboard Encoder		DL221	RCA
102▼	CDP1871CE	10	8	3.5	1.5§	0.0	6.5	500m∅	40	85	Keyboard Encoder		DL220	RCA
103▼	CDP1871D	10	8	3.5	1.5§	0.0	10.5	500m∅	55	125	Keyboard Encoder		DL221	RCA
104▼	CDP1871E	10	8	3.5	1.5§	0.0	10.5	500m∅	40	85	Keyboard Encoder		DL220	RCA
105	10788	10	8	3.5	-12	12	5.0	200m	0	70	Keyboard And Display Control	Z10-3	DL44	RKW
106	10815	10		3.5	-12	12	5.0	200m	0	70	Keyboard/Printer Controller	Z10-4	DL44	RKW
107	R6541	10	8	2.0	.80	0.0	5.0				Prog KB/Display Controller	Z10-10	DL26	RKW
108	KR2376	10	9	3.5	.80	12	5.0	200m	0	70	Keyboard Encoder ROM;2 Key Rollover	Z10-11	DL∅	SMC
109	KR3600	10	10L	3.5	.80	12	5.0	374m	0	70	Keyboard Encoder ROM:Prog KB Intf	Z10-5	DL∅	SMC
110	C8218	11		2.4	.45%	0.0	5.0	1.2	0	70	uComp Bus Contr for MCS80 Family	Z11-1	DL146	ITL

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ☑-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1	C8219	11		2.4	.45%	0.0	5.0	1.2	0	70	uComp Bus Contr for MCS85 Family	Z11-1	DL146	ITL
2	C8289	11		2.0	.80	0.0	5.0	1.5 ☑	0	70	Bus ARBITER;Provides MultiMaster Sys	Z11-3	DL212	ITL
3	D8218	11		2.4	.45%	0.0	5.0	1.2	0	70	uComp Bus Contr for MCS80 Family	Z11-1	DL147	ITL
4	D8219	11		2.4	.45%	0.0	5.0	1.2	0	70	uComp Bus Contr for MCS85 Family	Z11-1	DL147	ITL
5	D8289	11		2.0	.80	0.0	5.0	1.5 ☑	0	70	Bus ARBITER;Provides MultiMaster Sys	Z11-3	DL211	ITL
6	P8218	11		2.4	.45%	0.5	7.0	1.2 ☑	0	70	uComp Bus Contr for MCS80 Family	Z11-1	DL181	ITL
7	P8219	11		2.4	.45%	0.5	7.0	1.2 ☑	0	70	uComp Bus Contr for MCS80 Family	Z11-1	DL181	ITL
8	P8289	11		2.0	.80	0.0	5.0	1.5 ☑	0	70	Bus ARBITER;Provides MultiMaster Sys	Z11-3	DL118	ITL
9#	M5L8228P	11	8	2.0	.80	0.0	5.0	1.0 ☑	0	75	Sys Cont/Bus Driver for M5L 8080AP,S			MITJ
10	DP8228J	11	8	3.3	.45%	0.0	5.0	997m	0	70	Sys Contr/Bus Dr;GENs Rd/Wr Control	Z11-2	DL159	NSC
11	DP8228N	11	8	3.3	.45%	0.0	5.0	997m	0	70	Sys Contr/Bus Dr;GENs Rd/Wr Control	Z11-2	DL67c	NSC
12	DP8238J	11	8	3.3	.45%	0.0	5.0	997m	0	70	Sys Contr/Bus Dr;GENs Rd/Wr Control	Z11-2	DL159	NSC
13	DP8238N	11	8	3.3	.45%	0.0	5.0	997m	0	70	Sys Contr/Bus Dr;GENs Rd/Wr Control	Z11-2	DL67c	NSC
14	Am2904DC	12	4	2.0	.70	0.0	5.0	140m	0	70	ALU Status,Shift Control Functions	Z12-1	DL37b	AMV
15	Am2904DM	12	4	2.0	.70	0.0	5.0	140m	55	125	ALU Status,Shift Control Functions	Z12-1	DL37b	AMV
16	Am2904FM	12	4	2.0	.70	0.0	5.0	140m	55	125	ALU Status,Shift Control Functions	Z12-1	FP4a	AMV
17	Am2904PC	12	4	2.0	.70	0.0	5.0	140m	0	70	ALU Status,Shift Control Functions	Z12-1	DL112a	AMV
18	9404DC	12	4	2.0	.80§	0.0	5.0	450m	0	75	Data Path Switch,typ 27ns max	Z12-2	DL154	FSC
19	9404DM	12	4	2.0	.70§	0.0	5.0	450m	55	125	Data Path Switch,typ 27ns max	Z12-2	DL154	FSC
20	9404PC	12	4	2.0	.80§	0.0	5.0	450m	0	75	Data Path Switch,typ 27ns max	Z12-2	DL155	FSC
21	MC10900	12	8					910m	0	70	MECL-LSI 8-Bit Parity ALU Slice	Z12-3	DL219	MOTA
22♦	MC68120	13	8			0.0	5.0				Enhanced M6800 CPU;8x8 Bit Multiply	Z13-1	DL230	MOTA
23▼	MC68120-1	13	8			0.0	5.0	1.2	0	70	Cycle Time 2.0us max at fo 1.25MHz	Z13-1	DL230	MOTA
24▼	MC68121	13	8			0.0	5.0	1.2	0	70	Cycle Time 2.0us,max at fo 1.0MHz	Z13-1	DL230	MOTA
25▼	MC68121-1	13	8			0.0	5.0	1.2	0	70	Cycle Time 2.0us max at fo 1.25MHz	Z13-1	DL230	MOTA
26▼	Z-UPC-UCS	13	6R			0.0	5.0				3 Prog I/O Ports;2k Bytes Prog ROM		DL190	ZIL
27▼	Z-UPC-UPS	13	6R			0.0	5.0				3 Prog I/O Ports;2k Bytes Prog ROM		DL189	ZIL
28	COM8017	20	8S	2.0	.80	0.0	5.0	150m	0	70	UART;40k Baud;200ns Strobes;§ Z20-21	DL☑	SMC	
29▼	S68A52	20	8SΔ	2.0	.80	0.0	5.0	525m	0	70	Synchronous Serial Data Adapter	Z20-13	DL9h	AMI
30	S68A54L	20	85	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-32	DL67d	AMI
31	S68A54P	20	85	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-32	DL74	AMI
32▼	S68B52	20	8SΔ	2.0	.80	0.0	5.0	525m	0	70	Synchronous Serial Data Adapter	Z20-13	DL9h	AMI
33▼	S68B54	20	85	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-32	DL74	AMI
34	S2350	20	8	2.0	.80	0.0	5.0	750m	0	70	Universal Syn Receiver/Transmitter	Z20-1	DL2	AMI
35	S6850	20	8S	2.4	.40	0.0	5.0	525m	0	70	Asynchronous Com Interface Adapter	Z20-11	DL3	AMI
36	S6851	20	8	2.0	.80	0.0	5.0	450m	0	70	ICC 90 MA;CIN 10PF ° VIN OV;(PCI)	Z20-26	DL105	AMI
37	S6852	20	8SΔ	2.0	.80	0.0	5.0	525m	0	70	Synchronous Serial Data Adapter	Z20-13	DL9h	AMI
38	S6854L	20	8S	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-32	DL67d	AMI
39	S6854P	20	8S	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-32	DL74	AMI
40	S9902	20	8	2.2	.80	0.0	5.0	500m	0	70	Asynchronous Communications Control	Z20-36	DL168	AMI
41	Am9551-4DC	20	8	2.0	.80	0.0	5.0	400m	0	70	Prog Serial Data Comm Interface	Z20-16	DL49	AMV
42	Am9551DC	20	8	2.0	.80	0.0	5.0	400m	0	70	Prog Serial Data Comm Interface	Z20-16	DL49	AMV
43	Am9551DM	20	8	2.0	.80	0.0	5.0	400m	55	125	Prog Serial Data Comm Interface	Z20-16	DL49	AMV
44	MM1-OPT	20	8	2.0	.80	12	12	7.8			Clock,1 Serial,4 Parallel I/O Pts	Z20-19	MD3	CLI
45#	ADLC540/E-6	20	8			12	12		0	55	RS 422 and RS 232C Std. Interface			EURF
46	9401PC	20	16	2.0	.80	0.0	5.0	500m	0	70	CRC Gen/Checker; 14 Pin Plastic Pkg	Z20-1	DL157	FSC
47	9411DC	20	16	2.0	.80	0.0	5.0	550m	0	75	CRC Gen/Checker,Clock 10MHz	Z20-41	DL156	FSC
48	9411DM	20	16	2.0	.70	0.0	5.0	550m	55	125	CRC Gen/Checker,Clock 10MHz	Z20-41	DL156	FSC
49	9411FM	20	16	2.0	.70	0.0	5.0	550m	55	125	CRC Gen/Checker,Clock 10MHz	Z20-41	FP19	FSC
50	9411PC	20	16	2.0	.80	0.0	5.0	550m	0	75	CRC Gen/Checker,Clock 10MHz	Z20-41	DL157	FSC
51	F68A54P	20	8	2.0	.65§	0.0	5.0	250m	0	70	Adv Data Link Controller;28 Pin Pls	Z20-50	DL204	FSC
52	F3846DC	20	16	2.0	.80§	0.0	5.0	600m	0	70	SPCC;Line/Byte Control Protocols	Z20-34	DL37c	FSC
53	F3846PC	20	16	2.0	.80§	0.0	5.0	600m	0	70	SPCC;Line/Byte Control Protocols	Z20-34	DL11m	FSC
54	F6854P	20	8	2.0	.65§	0.0	5.0	250m	0	70	Adv Data Link Controller;28 Pin Cer	Z20-50	DL204	FSC
55	F6856DC	20	16	2.0	.80§	0.0	5.0	600m	0	70	Synch Protocol Comm Controller(SPCC)		DL37c	FSC
56	F6856PC	20	16	2.0	.80§	0.0	5.0	600m	0	70	Synch Protocol Comm Controller(SPCC)		DL11m	FSC
57	F38431DC	20	8	2.7	.80§	0.0	12	500m	0	70	USART;28 Pin,Ceramic;Sync:320K Baud	Z20-49	DL36	FSC
58	F38431DL	20	8	2.7	.80§	0.0	12	500m	55	85	USART;28 Pin,Ceramic;Sync:160K Baud	Z20-49	DL36	FSC
59	F38431DM	20	8	2.7	.80§	0.0	12	500m	55	125	USART;28 Pin,Ceramic;Sync:160K Baud	Z20-49	DL36	FSC
60	F38431PC	20	8	2.7	.80§	0.0	12	500m	0	70	USART;28 Pin,Plastic;Sync:3200K Baud	Z20-49	DL74	FSC
61	F38432DC	20	8	2.7	.80§§	0.0	12	500m	0	70	USART;28 Pin,Ceramic;Sync:160K Baud	Z20-49	DL36	FSC
62	F38432DL	20	8	2.7	.80§	0.0	12	500m	55	85	USART;28 Pin,Ceramic;Sync:80K Baud	Z20-49	DL36	FSC
63	F38432DM	20	8	2.7	.80§	0.0	12	500m	55	1254	USART;28 Pin,Ceramic;Sync:80K Baud	Z20-49	DL36	FSC
64	F38432PC	20	8	2.7	.80§	0.0	12	0	0	70	USART;28 Pin;Plastic;Sync:160K Baud	Z20-49	DL74	FSC
65	F38433DC	20	8	2.7	.80§	0.0	12	500m	0	70	USART;28 Pin,Ceramic;Sync:80K Baud	Z20-49	DL36	FSC
66	F38433PC	20	8	2.7	.80§	0.0	12	500m	0	70	USART;28 Pin,Plastic;Sync:80K Baud	Z20-49	DL74	FSC
67	HCMP1854CD	20	8			0.0	5.0	500m	55	125	Universal Asynch Receiver/Trans	Z20-7		HAC
68	HCMP1854D	20	8			0.0	10	500m	55	125	Universal Asynch Receiver/Trans	Z20-7		HAC
69	HD1-6402-2	20	8	3.5	1.0	0.0	5.0	500u	55	125	Universal Asynch Receiver/Trans	Z20-4	DL37e	HAS
70	HD1-6402-9	20	8	3.5	1.0	0.0	5.0	500u	40	85	Universal Asynch Receiver/Trans	Z20-4	DL37e	HAS
71	HD1-6402A-2	20	8	7.0	2.0	0.0	10	5.0m	55	125	Universal Asynch Receiver/Trans	Z20-4	DL37e	HAS
72	HD1-6402A-9	20	8	7.0	2.0	0.0	10	5.0m	40	85	Universal Asynch Receiver/Trans	Z20-4	DL37e	HAS
73	HD1-6402C-9	20	8	3.0	.80	0.0	5.0	4.0m	40	85	Universal Asynch Receiver/Trans	Z20-4	DL37e	HAS
74	HD3-6402-2	20	8	3.5	1.0	0.0	5.0	500u	55	125	Universal Asynch Receiver/Trans	Z20-4	DL131	HAS
75	HD3-6402-9	20	8	3.5	1.0	0.0	5.0	500u	40	85	Universal Asynch Receiver/Trans	Z20-4	DL131	HAS
76	HD3-6402A-2	20	8	7.0	2.0	0.0	10	5.0m	55	125	Universal Asynch Receiver/Trans	Z20-4	DL131	HAS
77	HD3-6402A-9	20	8	7.0	2.0	0.0	10	5.0m	40	85	Universal Asynch Receiver/Trans	Z20-4	DL131	HAS
78	HD3-6402C-9	20	8	3.0	.80	0.0	5.0	4.0m	40	85	Universal Asynch Receiver/Trans	Z20-4	DL131	HAS
79#	HD468A52P	20	8	2.0	.80	0.0	5.0	525m	20	75	Syn Sec Data Adapters,Speed 1.5MHz			HITJ
80#	HD46850P	20	1SΔ	2.0	.80	0.0	5.0	525m	20	75	Asynchronous Comm Interface Adapter	Z20-14	DL☑	HITJ
81#	HD46852P	20	8	2.0	.80	0.0	5.0	525m	20	75	Syn Sec Data Adapters,Speed 1.0MHz			HITJ
82	IM6402-1IDL	20	8	3.0	.80	0.0	5.0	9.5m	40	85	UART;3-State Output Contr Buffers	Z20-4	DL37a	INL
83	IM6402-1IPL	20	8	3.0	.80	0.0	5.0	9.5m	40	85	UART;3-State Output Contr Buffers	Z20-4	DL86	INL
84	IM6402-1MDL	20	8	3.0	.80	0.0	5.0	9.5m	55	125	UART;3-State Output Contr Buffers	Z20-4	DL37a	INL
85	IM6402AIDL	20	8	7.0	2.0	0.0	10	90m	40	85	UART;3-State Output Contr Buffers	Z20-4	DL37a	INL
86	IM6402AIPL	20	8	7.0	2.0	0.0	10	90m	40	85	UART;3-State Output Contr Buffers	Z20-4	DL86	INL
87	IM6402AMDL	20	8	7.0	2.0	0.0	10	90m	55	125	UART;3-State Output Contr Buffers	Z20-4	DL37a	INL
88	IM6402IPL	20	8	3.0	.80	0.0	5.0	6.0m	40	85	UART;3-State Output Contr Buffers	Z20-4	DL86	INL
89	IM6403-1IDL	20	8	3.0	.80	0.0	5.0	28m	40	85	UART;Ext Xtal;On-Chip Osc-Divider	Z20-4a	DL37a	INL
90	IM6403-1IPL	20	8	3.0	.80	0.0	5.0	28m	40	85	UART;Ext Xtal;On-Chip Osc-Divider	Z20-4a	DL86	INL
91	IM6403-1MDL	20	8	3.0	.80	0.0	5.0	28m	55	125	UART;Ext Xtal;On-Chip Osc-Divider	Z20-4a	DL37a	INL
92	IM6403AIDL	20	8	7.0	2.0	0.0	10	130m	40	85	UART;Ext Xtal;On-Chip Osc-Divider	Z20-4a	DL37a	INL
93	IM6403AIPL	20	8	7.0	2.0	0.0	10	130m	40	85	UART;Ext Xtal;On-Chip Osc-Divider	Z20-4a	DL86	INL
94	IM6403AMDL	20	8	7.0	2.0	0.0	10	130m	55	125	UART;Ext Xtal;On-Chip Osc-Divider	Z20-4a	DL37a	INL
95	IM6403IPL	20	8	3.0	.80	0.0	5.0	19m	40	85	UART;Ext Xtal;On-Chip Osc-Divider	Z20-4a	DL86	INL
96	C8251	20	8	2.0	.80	0.0	5.0	400m	0	70	Program Communication Interface	Z20-12	DL36	ITL
97	C8251A	20	8	2.0	.80	0.0	5.0		0	70	Program Comm Interface;Auto Detect	Z20-12	DL36	ITL
98	C8273	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Program HDLC/SDLC Protocol Control	Z20-18	DL70	ITL
99	C8273-4	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Program HDLC/SDLC Protocol Control	Z20-18	DL70	ITL
100	C8273-8	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Program HDLC/SDLC Protocol Control	Z20-18	DL70	ITL
101	CS2657	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Prog Communication Interface	Z20-12	DL146	ITL
102	D8251A	20	8	2.0	.80	0.0	5.0	500m	0	70	Progm Communication Interface	Z20-12	DL35	ITL
103	D8273	20	8Δ	2.0	.80	0.0	5.0	800m	0	70	Progm HDLC/SDLC Protocol Controller	Z20-18	DL38	ITL
104	D8273-4	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Program HDLC/SDLC Protocol Control	Z20-18	DL148	ITL
105	D8273-8	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Program HDLC/SDLC Protocol Control	Z20-18	DL148	ITL
106	DS2657	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Prog Communication Interface	Z20-12	DL35	ITL
107	MD8251	20	8	2.0	.80	0.0	5.0		55	125	Progm Communication Interface	Z20-12	DL35	ITL
108	P8251A	20	8	2.0	.80	0.0	5.0	500m	0	70	Progm Communication Interface	Z20-12	DL43	ITL
109	P8273	20	8Δ	2.0	.80	0.0	5.0	800m	0	70	Progm HDLC/SDLC Protocol Controller	Z20-18	DL42f	ITL
110	P8273-4	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Program HDLC/SDLC Protocol Control	Z20-18	DL149	ITL

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY NEG. (V)	RATED PWR. SUPPLY POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
											SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ☑-ABS.MAX. %-OUTPUT			
1	P8273-8	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Program HDLC/SDLC Protocol Control	Z20-18	DL149	ITL
2	PS2657	20	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Prog Communication Interface	Z20-12	DL181	ITL
3▼#	M5L8251AP	20	8	2.2	.80	0.0	5.0	1.0	0	70	Programmable Communication Interface	Z20-6	DL181	MITJ
4	MK3884P-10	20	8	2.0	.80	0.0	5.0	800m	40	85	Same as MK3884N-4 Except Ceramic	201-21	DL42d	MOS
5	MC68A50L	20	1SΔ	2.0	.80§	0.0	5.0	525m	0	70	AC Interface Adapter;tcycE 666ns min	Z20-14	DL1d	MOTA
6	MC68A50P	20	1SΔ	2.0	.80§	0.0	5.0	525m	0	70	AC Interface Adapter;tcycE 666ns min	Z20-14	DL27	MOTA
7	MC68A52CL	20	8	2.0	.80	0.0	5.0	525m	40	85	Syn Ser Data Adapter,Speed 1.5MHz	Z20-13	DL9b	MOTA
8	MC68A52CP	20	8	2.0	.80	0.0	5.0	525m	40	85	Syn Ser Data Adapter,Speed 1.5MHz	Z20-13	DL7b	MOTA
9	MC68A52L	20	8	2.0	.80	0.0	5.0	525m	0	70	Syn Ser Data Adapter,Speed 1.5MHz	Z20-13	DL9b	MOTA
10	MC68A52P	20	8	2.0	.80	0.0	5.0	525m	0	70	Syn Ser Data Adapter,Speed 1.5MHz	Z20-13	DL7b	MOTA
11	MC68A54CL	20	8	2.0	.80	0.0	5.0	850m	40	85	Advanced Data Link Controller	Z20-33	DL113	MOTA
12	MC68A54CP	20	8	2.0	.80	0.0	5.0	850m	40	85	Advanced Data Link Controller	Z20-33	DL74	MOTA
13	MC68A54L	20	8	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-33	DL113	MOTA
14	MC68A54P	20	8	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-33	DL74	MOTA
15	MC68B50L	20	1SΔ	2.0	.80§	0.0	5.0	525m	0	70	AC Interface Adapter;tcycE 500ns min	Z20-14	DL1d	MOTA
16	MC68B50P	20	1SΔ	2.0	.80§	0.0	5.0	525m	0	70	AC Interface Adapter;tcycE 500ns min	Z20-14	DL27	MOTA
17	MC68B52L	20	8	2.0	.80	0.0	5.0	525m	0	70	Syn Ser Data Adapter,Speed 2.0MHz	Z20-13	DL9b	MOTA
18	MC68B52P	20	8	2.0	.80	0.0	5.0	525m	0	70	Syn Ser Data Adapter,Speed 2.0MHz	Z20-13	DL7b	MOTA
19	MC68B54L	20	8	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-33	DL113	MOTA
20	MC68B54P	20	8	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-33	DL74	MOTA
21	MC6850CL	20	1SΔ	2.0	.80§	0.0	5.0	525m	40	85	Asynchronous Comm Interface Adapter	Z20-14	DL9b	MOTA
22	MC6850L	20	1SΔ	2.0	.80	0.0	5.0	525m	0	70	Asynchronous Com Interface Adaptor	Z20-14	DL9b	MOTA
23	MC6850P	20	1SΔ	2.0	.80	0.0	5.0	525m	0	70	Asynchronous Com Interface Adaptor	Z20-14	DL7b	MOTA
24	MC6852BJCS	20	8	2.0	.80	0.0	5.0	525m	55	125	Syn Ser Data Adapter,Speed 1.0MHz	Z20-13	DL9b	MOTA
25	MC6852CJCS	20	8	2.0	.80	0.0	5.0	525m	55	125	Syn Ser Data Adapter,Speed 1.0MHz	Z20-13	DL9b	MOTA
26	MC6852CL	20	8	2.0	.80§	0.0	5.0	525m	40	85	Synchronous Serial Data Adapter	Z20-13	DL9b	MOTA
27	MC6852CP	20	8	2.0	.80	0.0	5.0	525m	40	85	Syn Ser Data Adapter,Speed 1.0MHz	Z20-13	DL7b	MOTA
28	MC6852L	20	8	2.0	.80§	0.0	5.0	525m	0	70	Synchronous Serial Data Adapter	Z20-13	DL9b	MOTA
29	MC6852P	20	8	2.0	.80§	0.0	5.0	525m	0	70	Synchronous Serial Data Adapter	Z20-13	DL7b	MOTA
30	MC6854BQCS	20	8	2.0	.80	0.0	5.0	850m	55	125	Advanced Data Link Controller	Z20-33	DL☑	MOTA
31	MC6854CL	20	8	2.0	.80	0.0	5.0	850m	40	85	Advanced Data Link Controller	Z20-33	DL113	MOTA
32	MC6854CP	20	8	2.0	.80	0.0	5.0	850m	40	85	Advanced Data Link Controller	Z20-33	DL74	MOTA
33	MC6854CQCS	20	8	2.0	.80	0.0	5.0	850m	55	125	Advanced Data Link Controller	Z20-33	DL☑	MOTA
34	MC6854L	20	8	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-33	DL113	MOTA
35	MC6854P	20	8	2.0	.80	0.0	5.0	850m	0	70	Advanced Data Link Controller	Z20-33	DL74	MOTA
36	MC6860CL	20	1SΔ	2.0	.80§	0.0	5.0	325m	40	85	0-600Bps Digital Modem	Z20-8	DL9b	MOTA
37	MC6860L	20	1SΔ	2.0	.80	0.0	5.0	325m	0	70	0-600 Bps Digital Modem	Z20-8	DL9b	MOTA
38	MC6860P	20	1SΔ	2.0	.80	0.0	5.0	325m	0	70	0-600 Bps Digital Modem	Z20-8	DL7b	MOTA
39	MC6862CL	20	6	2.0	.80	0.0	5.0	300m	40	85	2400Bps Digital Modulator	Z20-8	DL9b	MOTA
40	MC6862L	20	6	2.0	.80	0.0	5.0	300m	0	70	2400 bps Digital Modulator	Z20-10	DL9b	MOTA
41	MC6862P	20	6	2.0	.80	0.0	5.0	300m	0	70	2400 bps Digital Modulator	Z20-10	DL7b	MOTA
42#	uPD8251C	20	8	2.0	.80	0.0	5.0	400m	10	70	Prog Comm Interface: USART	Z20-6	DL67	NECJ
43	uPD369D	20	1SΔ	3.0	.80	5.0	12	495m	0	70	Universal Asynch Rec/Transmitter	Z20-5	DL58a	NECM
44	INS2651D	20	8	2.0	.80	0.0	5.0	750m	0	70	Progm Communication Interface	Z20-26	DL36g	NSC
45	INS2651N	20	8	2.0	.80	0.0	5.0	750m	0	70	Progm Communication Interface	Z20-26	DL67c	NSC
46	INS8250D	20	8	2.0	.80	0.0	5.0	400m	0	70	Asynch Comm Element	Z20-29	DL37d	NSC
47	INS8250N	20	8	2.0	.80	0.0	5.0	400m	0	70	Asynch Comm Element	Z20-29	DL11f	NSC
48	INS8251D	20	8	2.0	.80	0.0	5.0	400m	0	70	Progm Comm Interface	Z20-30	DL36g	NSC
49#	2651I	20	8	2.0	.80	0.0	5.0	450m†	0	70	Prog Comm Interface	Z20-26	DL105	PHIN
50#	2652I	20	16	2.0	.80	0.0	5.0	750m†	0	70	Multi Protocol Comm Comtroller,1MHz	Z20-27	DL16	PHIN
51	7301	20		3.0	-3.0	0.0	5.0	1.9			RS232 TTY Drv/Rec Card;	Z20-47		PRO
52▼	CDP18S641	20	8			15	15		0	70	Selectable Baud Rate			RCA
53	CDP1854ACE	20	8	3.5	1.5	0.0	5.0	2.5m♦	40	85	CMOS URAT	Z20-7	DLIF	RCA
54	CDP1854AD	20	8	3.5	1.5	0.0	5.0	2.5m♦	40	85	CMOS UART	Z20-7	DL1f	RCA
55	CDP1854AE	20	8	3.5	1.5	0.0	5.0	2.5m♦	40	85	CMOS URAT			RCA
56	10930	20	1SΔ	3.5	-12	12	5.0	330m	0	70	Serial Data Controller	Z20-17	DL44	RKW
57	R6551AC	20	8	2.0	.80	0.0	5.0	500m	0	70	Asynch Comm Interface Adapter	Z20-38	DL140	RKW
58	R6551ACE	20	8	2.0	.80	0.0	5.0	500m	40	85	Asynch Comm Interface Adapter	Z20-38	DL140	RKW
59	R6551AP	20	8	2.0	.80	0.0	5.0	500m	0	70	Asynch Comm Interface Adapter	Z20-38	DL141	RKW
60	R6551C	20	8	2.0	.80	0.0	5.0	500m	0	70	Asynch Comm Interface Adapter	Z20-38	DL140	RKW
61	R6551CE	20	8	2.0	.80	0.0	5.0	500m	40	85	Asynch Comm Interface Adapter	Z20-38	DL140	RKW
62	R6551P	20	8	2.0	.80	0.0	5.0	500m	0	70	Asynch Comm Interface Adapter	Z20-38	DL141	RKW
63▼#	Z80ASIO0B1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL184	SGAI
64▼#	Z80ASIO0D1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL183	SGAI
65▼#	Z80ASIO1B1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL184	SGAI
66▼#	Z80ASIO1D1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL183	SGAI
67▼#	Z80ASIO2B1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL184	SGAI
68▼#	Z80ASIO2D1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL183	SGAI
69▼#	Z80SIO0B1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocals	Z20-37a	DL184	SGAI
70▼#	Z80SIO1B1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Proto	Z20-37b	DL184	SGAI
71▼#	Z80SIO1D1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocals	A20-37b	DL183	SGAI
72▼#	Z80SIO2B1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Proto	Z20-37c	DL184	SGAI
73▼#	Z80SIO2D1	20	8	2.0	.80	0.0	5.0		0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocals	Z20-37c	DL183	SGAI
74	2652-1N	20	16	2.0	.80§	0.3	7.0	800m	0	70	Multi-Protocol;NMOS;2.0MHz Max Clk	Z20-27	DL☑	SIC
75	2652N	20	16	2.0	.80§	0.3	7.0	800m	0	70	Multi-Protocol;NMOS;1.0MHz Max Clk	Z20-27		SIC
76	N8X01F	20	1LS	2.0	.80	0.0	5.0	590m	0	70	Cyclic Redund Check Gen/Checker,Cer	Z20-25	DL106	SIC
77	N8X01N	20	1LS	2.0	.80	0.0	5.0	490m	0	70	Cyclic Redund Check Gen/Checker,Plas	Z20-25	DL106	SIC
78	N2651I	20	8	2.0	.80	0.0	5.0	450m†	0	70	Prog Comm Interface	Z20-26	DL105	SIC
79	N2652-1I	20	16	2.0	.80	0.0	5.0	750m	0	70	Multi Protocol Comm Controller,2MHz	Z20-27	DL1b	SIC
80	N2652I	20	16	2.0	.80	0.0	5.0	750m	0	70	Multi Protocol Comm Controller,1MHz	Z20-27	DL1b	SIC
81	COM1671	20	8S	2.4	.80	5.0	12	525m	0	70	Async/Sync Transmitter Receiver ASTR	Z20-3	DL☑	SMC
82	COM1863	20	8Δ			0.0	5.0				UART;Double Buffered;40k Baud	Z20-21	DL☑	SMC
83	COM2017	20	8S	3.0	.80§	12	5.0	280m	0	70	UART:Clock Freq 400kHZ Max,40k Baud	Z20-21	DL☑	SMC
84	COM2017/H	20	8S	3.0	.80§	12	5.0	280m	0	70	UART:Clock Freq 640kHZ Max,40k Baud	Z20-21	DL☑	SMC
85	COM2502	20	8S	3.0	.80§	12	5.0	280m	0	70	UART:Clock Freq 400kHZ Max,40k Baud	Z20-21	DL☑	SMC
86	COM2502/H	20	8S	3.0	.80§	12	5.0	280m	0	70	UART:Clock Freq 640kHZ Max,40k Baud	Z20-21	DL☑	SMC
87	COM2601	20	8S	3.5	.80§	12	5.0	476m	0	70	USRT:250k Baud,200ns Strobes	Z20-20	DL☑	SMC
88	COM2651	20	8S			0.0	5.0				PCI;Compatible with 2651,1N2651	Z20-26	DL☑	SMC
89	COM5025	20	16S	3.5	.80	0.0	12		0	70	Multi-protocol Univ Syn Rec/Trans	Z20-24	DL☑	SMC
90	COM5036	20	32F	3.5	.80	0.0	12	489m	0	70	Dual Baud Rate Gen:Prog Divider	Z20-22	DL☑	SMC
91	COM5036T	20	32F	3.5	.80	0.0	12	489m	0	70	Dual Baud Rate Gen:Prog Divider	Z20-22a	DL☑	SMC
92	COM5046	20	16F	3.5	.80	0.0	12	489m	0	70	Baud Rate Gen:Prog Divider	Z20-23	DL☑	SMC
93	COM5046T	20	16F	3.5	.80	0.0	12	489m	0	70	Baud Rate Gen:Prog Divider	Z20-23a	DL☑	SMC
94	COM8018	20	8Δ			0.0	5.0				UART,200ns Strobes	Z20-21	DL☑	SMC
95	COM8251A	20	8SΔ			0.0	5.0				USART Double Buffered	Z20-30	DL☑	SMC
96	COM8502	20	8S	2.0	.80	0.0	5.0	150m	0	70	UART;5 Volt Only Supply;§	Z20-21	DL☑	SMC
97	SYC6551	20	8	2.0	.80	0.0	5.0	500m	0	70	Asynch Comm Interface,tACR 395ns Max	Z20-35	DL134	SYK
98	SYC6551A	20	8	2.0	.80	0.0	5.0	500m	0	70	Asynch Comm Interface,tACR 200ns Max	Z20-35	DL134	SYK
99	SYP6551	20	8	2.0	.80	0.0	5.0	500m	0	70	Asynch Comm Interface,tACR 395ns Max	Z20-35	DL135	SYK
100	SYP6551A	20	8	2.0	.80	0.0	5.0	500m	0	70	Asynch Comm Interface,tACR 200ns Max	Z20-35	DL135	SYK
101	TMS9902-40JL	20	85	2.0	.80	0.0	5.0	500m	0	70	Async Comm Controller Ceramic Pkg	Z20-39		TII
102	TMS9902-40NL	20	85	2.0	.80	0.0	5.0	500m	0	70	Async Comm Controller Plastic Pkg	Z20-39		TII
103	TMS9902JL	20	8S	2.0	.80	0.0	5.0	500m	0	70	Async Comm Controller;Cer Pkg	Z20-39		TII
104	TMS9902NL	20	8S	2.0	.80	0.0	5.0	500m	0	70	Async Comm Controller;Plas Pkg	Z20-39		TII
105	TMS9903JL	20	SΔ	2.2	.80	0.0	5.0	500m	0	70	Sync Comm Controller;Cer Pkg	Z20-40		TII
106	TMS9903NL	20	SΔ	2.2	.80	0.0	5.0	500m	0	70	Sync Comm Controller;Plas Pkg	Z20-40	DL17	TII
107	BR1941L	20		3.5	.80	0.0	12	474m	0	70	Dual Baud Rate Cl;No Neg Supply Req	Z20-44a	DL☑	WDC
108	BR2941L	20		3.5	.80	5.0	12	725m	0	70	Lo Cost Version of BR1941L;Req-VDC	Z20-44	DL☑	WDC
109	UC1671B	20	8								Asyn/Syn Rec/Trans;To 1M Band/S	Z20-3		WDC
110	UC1971A	20	8	2.4	.80	0.0	12	600m	0	70	Chip Select Astro:DC to 1M Band/S	Z20-45	DL160	WDC

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ☑-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1	UC1971B	20	8	2.4	.80	0.0	12	600m	0	70	Chip Select Astro:DC to 1M Band/S	Z20-45	DL161	WDC
2	WD1931A	20	8	2.4	.80	0.0	12	520m	0	70	Asynch/Synch Receiver/Transmitter	Z20-43	DL160	WDC
3	WD1931B	20	8	2.4	.80	0.0	12	520m	0	70	Asynch/Synch Receiver/Transmitter	Z20-43	DL161	WDC
4▼	WD1933A	20	8	2.4	.80	0.0	5.0		0	70	Sync Data Link Controller Z	Z20-42	DL160	WDC
5▼	WD1933B	20	8	2.4	.80	0.0	5.0		0	70	Sync Data Link Controller	Z20-42	DL161	WDC
6	WD8250A	20	8	2.0	.80§	0.0	5.0	400m	0	70	Asynch Communication Element	Z20-46	DL160	WDC
7	WD8250B	20	8	2.0	.80§	0.0	5.0	400m	0	70	Asynch Communication Element	Z20-46	DL161	WDC
8	Z80-SIO/0CE	20	8	2.0	.80	0.0	5.0	500m	40	85	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL138	ZIL
9	Z80-SIO/0CM	20	8	2.0	.80	0.0	5.0	500m	55	125	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL138	ZIL
10	Z80-SIO/0CS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL138	ZIL
11	Z80-SIO/0PS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL11f	ZIL
12	Z80-SIO/1CE	20	8	2.0	.80	0.0	5.0	500m	40	85	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL138	ZIL
13	Z80-SIO/1CM	20	8	2.0	.80	0.0	5.0	500m	55	125	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL138	ZIL
14	Z80-SIO/1CS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL138	ZIL
15	Z80-SIO/1PS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL11f	ZIL
16	Z80-SIO/2CE	20	8	2.0	.80	0.0	5.0	500m	40	85	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL138	ZIL
17	Z80-SIO/2CM	20	8	2.0	.80	0.0	5.0	500m	55	125	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL138	ZIL
18	Z80-SIO/2CS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL138	ZIL
19	Z80-SIO/2PS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL11f	ZIL
20	Z80A-SIO/0CE	20	8	2.0	.80	0.0	5.0	500m	40	85	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL138	ZIL
21	Z80A-SIO/0CM	20	8	2.0	.80	0.0	5.0	500m	55	125	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL138	ZIL
22	Z80A-SIO/0CS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL138	ZIL
23	Z80A-SIO/0PS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37a	DL11f	ZIL
24	Z80A-SIO/1CE	20	8	2.0	.80	0.0	5.0	500m	40	85	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL138	ZIL
25	Z80A-SIO/1CM	20	8	2.0	.80	0.0	5.0	500m	55	125	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL138	ZIL
26	Z80A-SIO/1CS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL138	ZIL
27	Z80A-SIO/1PS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37b	DL11f	ZIL
28	Z80A-SIO/2CE	20	8	2.0	.80	0.0	5.0	500m	40	85	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL138	ZIL
29	Z80A-SIO/2CM	20	8	2.0	.80	0.0	5.0	500m	55	125	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL138	ZIL
30	Z80A-SIO/2CS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL138	ZIL
31	Z80A-SIO/2PS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-37c	DL11f	ZIL
32	Z80A-SIO/9CE	20	8	2.0	.80	0.0	5.0	500m	40	85	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-51	DL138	ZIL
33	Z80A-SIO/9CM	20	8	2.0	.80	0.0	5.0	500m	55	125	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-51	DL138	ZIL
34	Z80A-SIO/9CS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-51	DL138	ZIL
35	Z80A-SIO/9PS	20	8	2.0	.80	0.0	5.0	500m	0	70	Syn/Asyn;HDLC,SDLC,BiSyn Protocols	Z20-51	DL11n	ZIL
36	Z80SIO/9CS	20	8	2.0	.80	0.0	5.0	500m	0	70	SYN/Asyn;HDLC,SDLC;BiSyn Protocols	Z20-51	DL138	ZIL
37	Z80SIO/9PS	20	8	2.0	.80	0.0	5.0	500m	0	70	SYN/Asyn;HDLC,SDLC;BiSyn Protocols	Z20-51	DL11n	ZIL
38	Z8030SCC	20	8	2.0	.80	0.0	5.0				2-OtoIN Bit per Sec,Full Duplex Chs	Z20-52		ZIL
39	Am2905DC	21	4	2.0	.80	0.0	5.0	525m	0	70	Quad 2 Input OC Bus Transceiver	Z21-3	DL7d	AMV
40	Am2905DM	21	4	2.0	.70	0.0	5.0	525m	55	125	Quad 2 Input OC Bus Transceiver	Z21-3	DL7d	AMV
41	Am2905FM	21	4	2.0	.70	0.0	5.0	525m	55	125	Quad 2 Input OC Bus Transceiver	Z21-3	FP3	AMV
42	Am2905PC	21	4	2.0	.80	0.0	5.0	525m	0	70	Quad 2 Input OC Bus Transceiver	Z21-3	DL7c	AMV
43	Am2906DC	21	4	2.0	.80	0.0	5.0	525m	0	70	Quad 2 Input OC Bus Transceiver	Z21-4	DL7d	AMV
44	Am2906DM	21	4	2.0	.70	0.0	5.0	525m	55	125	Quad 2 Input OC Bus Transceiver	Z21-4	DL7d	AMV
45	Am2906FM	21	4	2.0	.70	0.0	5.0	525m	55	125	Quad 2 Input OC Bus Transceiver	Z21-4	FP3	AMV
46	Am2906PC	21	4	2.0	.80	0.0	5.0	525m	0	70	Quad 2 Input OC Bus Transceiver	Z21-4	DL7c	AMV
47	Am2907DC	21	4	2.0	.80	0.0	5.0	550m	0	70	Quad Bus Transceiver	Z21-5	DL51	AMV
48	Am2907DM	21	4	2.0	.70	0.0	5.0	550m	55	125	Quad Bus Transceiver	Z21-5	DL51	AMV
49	Am2907FM	21	4	2.0	.70	0.0	5.0	550m	55	125	Quad Bus Transceiver	Z21-5		AMV
50	Am2907PC	21	4	2.0	.80	0.0	5.0	550m	0	70	Quad Bus Transceiver	Z21-5	DL60	AMV
51	Am2915ADC	21	4	2.0	.80	0.0	5.0	475m	0	70	Quad High Speed LSI Bus-Transceiver	Z21-3	DL7n	AMV
52	Am2915ADM	21	4	2.0	.80	0.0	5.0	475m	0	70	Quad High Speed LSI Bus-Transceiver	Z21-3	DL7n	AMV
53	Am2915AFM	21	4	2.0	.70	0.0	5.0	475m	55	125	Quad High Speed LSI Bus-Transceiver	Z21-3	FP3a	AMV
54	Am2915APC	21	4	2.0	.80	0.0	5.0	475m	0	70	Quad High Speed LSI Bus-Transceiver	Z21-3	DL7m	AMV
55	Am2915DC	21	4	2.0	.80§	0.0	5.0	450m	0	70	Quad 3 State Bus Transceiver	Z21-3	DL7d	AMV
56	Am2915DM	21	4	2.0	.80§	0.0	5.0	450m	55	125	Quad 3 State Bus Transceiver	Z21-3	DL7d	AMV
57	Am2915FM	21	4	2.0	.80§	0.0	5.0	450m	55	125	Quad 3 State Bus Transceiver	Z21-3	FP3	AMV
58	Am2915PC	21	4	2.0	.80§	0.0	5.0	450m	0	70	Quad 3 State Bus Transceiver	Z21-3	DL7c	AMV
59	Am2916ADC	21	4	2.0	.80	0.0	5.0	550m	0	70	Low-Power Schottky Bus Transceiver	Z21-4	DL7n	AMV
60	Am2916ADM	21	4	2.0	.80	0.0	5.0	550m	0	70	Low-Power Schottky Bus Transceiver	Z21-4	DL7n	AMV
61	Am2916AFM	21	4	2.0	.70	0.0	5.0	550m	55	125	Low-Power Schottky Bus Transceiver	Z21-4	FP3a	AMV
62	Am2916APC	21	4	2.0	.80	0.0	5.0	550m	0	70	Low-Power Schottky Bus Transceiver	Z21-4	DL7m	AMV
63	Am2916DC	21	4	2.0	.80§	0.0	5.0	550m	0	70	Quad 3 State Bus Transceiver	Z21-4		AMV
64	Am2916DM	21	4	2.0	.80§	0.0	5.0	550m	55	125	Quad 3 State Bus Transceiver	Z21-4		AMV
65	Am2916FM	21	4	2.0	.80§	0.0	5.0	550m	55	125	Quad 3 State Bus Transceiver	Z21-4		AMV
66	Am2916PC	21	4	2.0	.80§	0.0	5.0	550m	0	70	Quad 3 State Bus Transceiver	Z21-4		AMV
67	Am2917ADC	21		2.0	.80	0.0	5.0	475m	0	70	Low-Power Schottky Bus Tranceiver	Z21-5	DL60b	AMV
68	Am2917ADM	21		2.0	.80	0.0	5.0	475m	55	125	Low-Power Schottky Bus Tranceiver	Z21-5	DL60b	AMV
69	Am2917AFM	21		2.0	.70	0.0	5.0	475m	55	125	Low-Power Schottky Bus Tranceiver	Z21-5	FP20	AMV
70	Am2917APC	21		2.0	.80	0.0	5.0	475m	0	70	Low-Power Schottky Bus Tranceiver	Z21-5	DL60a	AMV
71	Am2917DC	21	4	2.0	.80§	0.0	5.0	475m	0	70	Quad 3 State Bus Transceiver	Z21-5		AMV
72	Am2917DM	21	4	2.0	.80§	0.0	5.0	475m	55	125	Quad 3 State Bus Transceiver	Z21-5		AMV
73	Am2917FM	21	4	2.0	.80§	0.0	5.0	475m	55	125	Quad 3 State Bus Transceiver	Z21-5		AMV
74	Am2917PC	21	4	2.0	.80§	0.0	5.0	475m	0	70	Quad 3 State Bus Transceiver	Z21-5		AMV
75	Am8216XC	21	4	2.0	.95§	0.0	5.0	650m	0	70	Parallel Bidirectional Bus Driver	Z21-12	CH5	AMV
76	Am8226XC	21	4	2.0	.95§	0.0	5.0	600m	0	70	Parallel Bidirectional Bus Driver	Z21-13	CH6	AMV
77	MD8216	21	4	2.0	.95§	0.0	5.0	650m	55	125	Parallel Bidirectional Bus Driver	Z21-12	DL87	AMV
78	MD8226	21	4	2.0	.95§	0.0	5.0	600m	55	125	Parallel Bidirectional Bus Driver	Z21-13	DL87	AMV
79	mN629	21	2	2.0	.80	5.0	5.0	1.2	0	70	CPU to I/O Bus Interface;Diff Drive	Z21-9	DL51a	DGC
80	mN634	21	8D	2.0	.80		5.0	1.4	0	70	Octal Transceiver;CPU to Memory Bus	Z21-15	DL51a	DGC
81	mN636	21	2	2.0	.80	5.0	5.0	1.2	0	70	mN603 Controller to I/O Bus	Z21-9	DL51a	DGC
82	F6852	21	8S	2.0	.80§	0.0	5.0	525m	0	70	8-Bit Bi-directional Data Bus	Z21-25		FSC
83	HCMP1856CD	21	4			0.0	5.0	500m	55	125	4 Bit Bus Buffer/Separator	Z21-11		HAC
84	HCMP1856D	21	4			0.0	10	500m	55	125	4 Bit Bus Buffer/Separator	Z21-11		HAC
85	HCMP1857CD	21	4			0.0	5.0	500m	55	125	4 Bit Bus Buffer/Separator	Z21-11a		HAC
86	HCMP1857D	21	4			0.0	10	500m	55	125	4 Bit Bus Buffer/Separator	Z21-11a		HAC
87#	HD268T26P	21	4	2.0	.85§	0.0	5.0	435m	20	75	Quad Bus Transceiver,Plastic Pkg	Z21-1	DL6m	HITJ
88	B8226	21	4	2.0	.95§	0.5	7.0	600m☑	0	70	Parallel Bidirectional Bus Driver	Z21-13	DL☑	ITL
89	C8286	21	8	2.0	.80§	0.0	5.0	1.0 ☑	0	70	8B Par Bidir Bus Driver;IO Del 35ns	Z21-19	DL212	ITL
90	C8287	21	8	2.0	.80§	0.0	5.0	1.0 ☑	0	70	8B Par Bidir Bus Driver;IO Del 25ns	Z21-20	DL212	ITL
91	D3216	21	4	2.0	.95§	0.0	5.0	650m	0	75	Parallel Bidirectional Bus Driver	Z21-12	DL6a	ITL
92	D3226	21	4	2.0	.95§	0.0	5.0	600m	0	75	Parallel Inv Bidirect Bus Driver	Z21-13	DL6a	ITL
93	D8216	21	4	2.0	.95	0.0	5.0	650m	0	70	Parallel Bidirectional Bus Driver	Z21-12	DL6a	ITL
94	D8226	21	4	2.0	.95	0.0	5.0	600m	0	70	Parallel Bidirectional Bus Driver	Z21-13	DL6a	ITL
95	D8286	21	8	2.0	.80§	0.0	5.0	1.0 ☑	0	70	8B Par Bidir Bus Driver;IO Del 35ns	Z21-19	DL211	ITL
96	D8287	21	8	2.0	.80§	0.0	5.0	1.0 ☑	0	70	8B Par Bidir Bus Driver;IO Del 25ns	Z21-20	DL211	ITL
97	MD3216	21	4	2.0	.95§	0.0	5.0	650m	55	125	Parallel Bidirectional Bus Driver	Z21-12	DL6a	ITL
98	MD3226	21	4	2.0	.95§	0.0	5.0	600m	55	125	Parallel Inv Bidirect Bus Driver	Z21-13	DL6a	ITL
99	P3216	21	4	2.0	.95§	0.0	5.0	650m	0	75	Parallel Bidirectional Bus Driver	Z21-12	DL33	ITL
100	P3226	21	4	2.0	.95§	0.0	5.0	600m	0	75	Parallel Inv Bidirect Bus Driver	Z21-13	DL33	ITL
101	P8216	21	4	2.0	.95	0.0	5.0	650m	0	70	Parallel Bidirectional Bus Driver	Z21-12	DL33	ITL
102	P8226	21	4	2.0	.95	0.0	5.0	600m	0	70	Parallel Bidirectional Bus Driver	Z21-13	DL33	ITL
103	P8286	21	8	2.0	.80§	0.0	5.0	675m	0	70	8B Par Bidir Bus Driver,IO Del 35ns	Z21-19	DL118	ITL
104	P8287	21	8	2.0	.80§	0.0	5.0	475m	0	70	8B Par Bidir Bus Driver;IO Del 25ns	Z21-20	DL118	ITL
105	MC2905FM	21	4	2.0	.70	0.0	5.0	525m	55	125	Quad 2-Input OC Bus Transceiver	Z21-3	FP16	MOTA
106	MC2905LC	21	4	2.0	.80	0.0	5.0	525m	0	70	Quad 2-Input OC Bus Transceiver	Z21-3	DL68	MOTA
107	MC2905LM	21	4	2.0	.70	0.0	5.0	525m	55	125	Quad 2-Input OC Bus Transceiver	Z21-3	DL68	MOTA
108	MC2905PC	21	4	2.0	.80	0.0	5.0	525m	0	70	Quad 2-Input OC Bus Transceiver	Z21-3	DL69	MOTA
109	MC2906FM	21	4	2.0	.70	0.0	5.0	525m	55	125	Quad 2-In OC Bus Transc W/Parity	Z21-4	FP16	MOTA
110	MC2906LC	21	4	2.0	.80	0.0	5.0	525m	0	70	Quad 2-In OC Bus Transc W/Parity	Z21-4	DL68	MOTA

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ☑-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1	MC2906LM	21	4	2.0	.70	0.0	5.0	525m	55	125	Quad 2-In OC Bus Transc W/Parity	Z21-4	DL68	MOTA
2	MC2906PC	21	4	2.0	.80	0.0	5.0	525m	0	70	Quad 2-In OC Bus Transc W/Parity	Z21-4	DL69	MOTA
3	MC2907FM	21	4	2.0	.70	0.0	5.0	550m	55	125	Quad Bus Transceiver W/Parity	Z21-5	FP14	MOTA
4	MC2907LC	21	4	2.0	.80	0.0	5.0	550m	0	70	Quad Bus Transceiver W/Parity	Z21-5	DL133	MOTA
5	MC2907LM	21	4	2.0	.70	0.0	5.0	550m	55	125	Quad Bus Transceiver W/Parity	Z21-5	DL133	MOTA
6	MC2907PC	21	4	2.0	.80	0.0	5.0	550m	0	70	Quad Bus Transceiver W/Parity	Z21-5	DL132	MOTA
7	MC2915AFM	21	4	2.0	.70§	0.0	5.0	475m	55	125	Quad 3 State Bus Transceiver	Z21-3	FP16	MOTA
8	MC2915ALC	21	4	2.0	.80§	0.0	5.0	475m	0	70	Quad 3 State Bus Transceiver	Z21-3	DL68	MOTA
9	MC2915ALM	21	4	2.0	.70§	0.0	5.0	475m	55	125	Quad 3 State Bus Transceiver	Z21-3	DL68	MOTA
10	MC2915APC	21	4	2.0	.80§	0.0	5.0	475m	0	70	Quad 3 State Bus Transceiver	Z21-3	DL69	MOTA
11	MC2916AFM	21	4	2.0	.70§	0.0	5.0	550m	55	125	Quad 3 State Bus Transceiver	Z21-4	FP16	MOTA
12	MC2916ALC	21	4	2.0	.80§	0.0	5.0	550m	0	70	Quad 3 State Bus Transceiver	Z21-4	DL68	MOTA
13	MC2916ALM	21	4	2.0	.70§	0.0	5.0	550m	55	125	Quad 3 State Bus Transceiver	Z21-4	DL68	MOTA
14	MC2916APC	21	4	2.0	.80§	0.0	5.0	550m	0	70	Quad 3 State Bus Transceiver	Z21-4	DL69	MOTA
15	MC2917AFM	21	4	2.0	.70§	0.0	5.0	475m	55	125	Quad 3 State Bus Transceiver	Z21-5	FP14	MOTA
16	MC2917ALC	21	4	2.0	.80§	0.0	5.0	475m	0	70	Quad 3 State Bus Transceiver	Z21-5	DL133	MOTA
17	MC2917ALM	21	4	2.0	.70§	0.0	5.0	475m	55	125	Quad 3 State Bus Transceiver	Z21-5	DL133	MOTA
18	MC2917APC	21	4	2.0	.80§	0.0	5.0	475m	0	70	Quad 3 State Bus Transceiver	Z21-5	DL132	MOTA
19	MC6880AL	21	4	2.0	.85§	0.0	5.0	456m	0	75	Quad Bus Transceiver,Three State	Z21-1	DL76	MOTA
20	MC6880AP	21	4	2.0	.85§	0.0	5.0	456m	0	75	Quad Bus Transceiver,Three State	Z21-1	DL53	MOTA
21	MC6880L	21	4	2.0	.85§	0.0	5.0	435m	0	75	Quad Three State Bus Transceiver	Z21-1	DL6c	MOTA
22	MC6880P	21	4	2.0	.85§	0.0	5.0	435m	0	75	Quad Three State Bus Transceiver	Z21-1	DL53	MOTA
23	MC6889L	21	4D	2.0	.85§	0.0	5.0	456m	0	75	Non-Inverting Quad Bus Transceiver	Z21-2	DL76	MOTA
24	MC6889P	21	4D	2.0	.85§	0.0	5.0	456m	0	75	Non-Inverting Quad Bus Transceiver	Z21-2	DL53	MOTA
25	uPB8216C	21	4	2.0	.95§	0.0	5.0	650m	0	70	4 Bit Par Bidirectional Bus Driver	Z21-14	DL93	NECM
26	uPB8216D	21	4	2.0	.95§	0.0	5.0	650m	10	70	4 Bit Parallel Bidir Bus Driver	Z21-14	DL6f	NECM
27	uPB8226C	21	4	2.0	.95§	0.0	5.0	600m	0	70	4 Bit Par Bidirectional Bus Driver	Z21-17	DL93	NECM
28	uPB8226D	21	4	2.0	.95§	0.0	5.0	600m	0	70	4 Bit Par Bidirectional Bus Driver	Z21-17	DL6f	NECM
29	DP7304BJ	21	8	2.0	.70§	0.0	5.0	715m	55	125	8-Bit,3-St,Bidirec Xceiver/48mA Dr	Z21-21		NSC
30	DP8216J	21	4	2.0	.95§	0.0	5.0	650m	0	70	4-Bit Bidirec Bus Xceiver;noninvert	Z21-22a	DL6q	NSC
31	DP8226J	21	4	2.0	.95§	0.0	5.0	650m	0	70	4-Bit Bidierc Bus Xceiver;inverting	Z21-22b	DL6q	NSC
32	DP8304BJ	21	8	2.0	.80§	0.0	5.0	682m	0	70	8-Bit,3-St,Bidirec Xceiver/48mA Dr	Z21-21		NSC
33	DP8304BN	21	8	2.0	.80§	0.0	5.0	682m	0	70	8-Bit,3-St,Bidirec xceiver/48ma Dr	Z21-21	DL109	NSC
34	INS8304N	21	8	2.0	.80§	0.0	5.0	500m	0	70	8 Bit Bidir Transceiver	Z21-18	DL109	NSC
35#	N8T26AN	21	4	2.0	.85§	0.0	5.0	457m	0	70	Quad Bus Transceiver	Z21-1	DL4	PHIN
36#	N8T28N	21	4	2.0	.85§	0.0	5.0	578m	0	70	Quad Bus Transceiver	Z21-2	DL4	PHIN
37	CDP1856CD	21	4	3.5	1.5	0.0	5.0	500u†	55	125	4 Bit Bus Buffer/Separator	Z21-11	Δ001AE	RCA
38	CDP1856CE	21	4	3.5	1.5	0.0	5.0	500u†	40	85	4-Bit Bus Buffer/Separator	Z21-11	Δ001AE	RCA
39	CDP1856D	21	4	7.0	3.0	0.0	10	1.0m†	55	125	4 Bit Bus Buffer/Separator	Z21-11	Δ001AE	RCA
40	CDP1856E	21	4	7.0	3.0	0.0	10	1.0m†	40	85	4-Bit Bus Buffer/Separator			RCA
41	CDP1857CD	21	4	3.5	1.5	0.0	5.0	500u†	55	125	4 Bit Bus Buffer/Separator	Z21-11a	Δ001AE	RCA
42	CDP1857CE	21	4	3.5	1.5	0.0	5.0	500u†	40	85	4-Bit Bus Buffer/Separator			RCA
43	CDP1857D	21	4	7.0	3.0	0.0	10	1.0m†	55	125	4 Bit Bus Buffer/Separator	Z21-11a	Δ001AE	RCA
44	CDP1857E	21	4	7.0	3.0	0.0	10	1.0m†	40	85	4-Bit Bus Buffer/Separator			RCA
45	N8T26AB	21	4	2.0	.85§	0.0	5.0	457m	0	70	Quad Bus Transceiver	Z21-1	DL4	SIC
46	N8T26AF	21	4	2.0	.85§	0.0	5.0	457m	0	70	Quad Bus Transceiver	Z21-1	DL6	SIC
47	N8T28B	21	4	2.0	.85§	0.0	5.0	578m	0	70	Quad Bus Transceiver	Z21-2	DL4	SIC
48	N8T28F	21	4	2.0	.85§	0.0	5.0	578m	0	70	Quad Bus Transceiver	Z21-2	DL6	SIC
49	S8T26AB	21	4	2.0	.85§	0.0	5.0	457m	55	125	Quad Bus Transceiver	Z21-1	DL4	SIC
50	S8T26AF	21	4	2.0	.85§	0.0	5.0	457m	55	125	Quad Bus Transceiver	Z21-1	DL6	SIC
51	S8T28B	21	4	2.0	.85§	0.0	5.0	578m	55	125	Quad Bus Transceiver	Z21-2	DL4	SIC
52	S8T28F	21	4	2.0	.85§	0.0	5.0	578m	55	125	Quad Bus Transceiver	Z21-2	DL6	SIC
53	SN54S226J	21	4	2.0	.80§	0.0	5.0	625m†	55	125	4 Bit Par Latched Bus Transceiver	Z21-8	DL6d	TII
54	SN54S240J	21	4	2.0	.80	0.0	5.0	750m	55	125	Octal Buffers/Line Drivers/Receiver	Z21-6	DL16	TII
55	SN54S241J	21	4	2.0	.80	0.0	5.0	850m	55	125	Octal Buffers/Line Drivers/Receiver	Z21-7	DL16	TII
56	SN74S226J	21	4	2.0	.80§	0.0	5.0	625m†	0	70	4 Bit Par Latched Bus Transceiver	Z21-8	DL6d	TII
57	SN74S226N	21	4	2.0	.80§	0.0	5.0	625m†	0	70	4 Bit Par Latched Bus Transceiver	Z21-8	DL23	TII
58	SN74S240J	21	4	2.0	.80	0.0	5.0	750m	0	70	Octal Buffers/Line Drivers/Receiver	Z21-6	DL16	TII
59	SN74S240N	21	4	2.0	.80	0.0	5.0	750m	0	70	Octal Buffers/Line Drivers/Receiver	Z21-6	DL17	TII
60	SN74S241J	21	4	2.0	.80	0.0	5.0	900m	0	70	Octal Buffers/Line Drivers/Receiver	Z21-7	DL16	TII
61	9414D	22	64	2.0	.80	0.0	5.0	750m†	0	75	56-Bit Key Word;2 64 Word x 4Bit ROM	Z22-01	DL37c	FSC
62	C8294	22	8	2.0	.80	0.0	5.0	1.5 ☑	0	70	Data Encryption Unit	Z22-2	DL70	ITL
63	D8294	22	8	2.0	.80	0.0	5.0	1.5 ☑	0	70	Data Encryption Unit	Z22-2	DL148	ITL
64	P8294	22	8	2.0	.80	0.0	5.0		0	70	DATA Encryption Unit	Z22-2	DL42f	ITL
65▼	MC6859L	22	64	2.0	.80	0.0	5.0	1.0 †	0	70	Data Encryption Standard Algorithm	Z22-3	DL9b	MOTA
66	TM990/306	22				0.0	12	2.3	0	70	179 Wd Base Speech Set	Z22-2		TII
67	DT3762	23	16L			0.0	12	2.4	0	55	4 D/A Output Channels,Volt /Current			DTI
68▼#	M5L8243P	23	4	2.0	.80	0.0	5.0	600m	20	70	Input/Output Expander		DL124	MITJ
69▼	MC68A29L	23		2.0	.80	0.0	5.0	800m	0	70	Enable Cycle Time 667ns	Z23-4	DL228	MOTA
70▼	MC68A29P	23		2.0	.80	0.0	5.0	800m	0	70	Enable Cycle Time 667ns	Z23-4	DL229	MOTA
71▼	MC68B29L	23		2.0	.80	0.0	5.0	800m	0	70	Enable Cycle Time 500ns	Z23-4	DL228	MOTA
72▼	MC68B29P	23		2.0	.80	0.0	5.0	800m	0	70	Enable Cycle Time 500ns	Z23-4	DL229	MOTA
73▼	MC6829L	23		2.0	.80	0.0	5.0	800m	0	70	Enable Cycle Time 1.0us	Z23-4	DL228	MOTA
74▼	MC6829P	23		2.0	.80	0.0	5.0	800m	0	70	Enable Cycle Time 1.0us	Z23-4	DL229	MOTA
75▼	CDP18S660	23	4			0.0	5.0		0	70	40 Parallel I/O Lines			RCA
76	TM990/307	23				0.0	12	2.4	0	70	Interfaces 801 Auto-dialer	Z23-1		TII
77▼#	TMP8243P	23	4	2.0	.80	0.0	5.0	800m	0	70	I/O Expander;Four 4-Bit I/O Ports		DL7	TOSJ
78▼	Am8255A-5DC	30	8		.80	0.0	5.0	1.0 ☑	0	70	Prog Peripheral Interface	Z30-7	DL1h	AMD
79▼	Am8255A-5PC	30	8		.80	0.0	5.0	1.0 ☑	0	70	Prog Peripheral Interface	Z30-7	DL112	AMD
80▼	Am8255ADC	30	8		.80	0.0	5.0	1.0 ☑	0	70	Prog Peripheral Interface	Z30-7	DL1h	AMD
81▼	Am8255APC	30	8		.80	0.0	5.0	1.0 ☑	0	70	Prog Peripheral Interface Z30-7	DL112	CL112	AMD
82	S68A21	30	8	2.0	.80	0.0	5.0	550m	0	70	(PIA);Freq 1.5 MHz;Resp Time 1Z30-1	.0 uS	DL42J	AMI
83	S68B21	30	8	2.0	.80	0.0	5.0	550m	0	70	(PAI);Freq 2.0 MHz;Resp Time 1.0 uS	Z30-1	DL42J	AMI
84▼	S68H21	30	8	2.0	.80	0.0	5.0	550m	0	70	Peripheral Inter Adapter;Program	Z30-1	DL1n	AMI
85	S6820	30	8	2.4	.40§	0.0	5.0	600m	0	70	Peripheral Interface Adapter	Z30-1	DL2	AMI
86	S6821	30	8	2.0	.80	0.0	5.0	550m	0	70	(PIA);Freq 1.0 MHz;Resp Time 1.0 uS	Z30-1	DL42J	AMI
87	S9901	30	16	2.0	.80	0.0	5.0	750m☑	0	70	Programmable System Interface	Z30-13	DL1n	AMI
88	Am9555-4DC	30	8	2.0	.80	0.0	5.0	200m	0	70	Programmable Peripheral Interface	Z30-8	DL37b	AMV
89	Am9555DC	30	8	2.0	.80	0.0	5.0	200m	0	70	Programmable Peripheral Interface	Z30-8	DL37b	AMV
90	Am9555DM	30	8	2.0	.80	0.0	5.0	200m	55	125	Programmable Peripheral Interface	Z30-8	DL37b	AMV
91	MP1216	30	12			0.0	5.0	5.0	0	70	Resistor Programmable Instr. Amp	Z30-26		BUB
92	MP1216-PGA	30	12			0.0	5.0	5.0	0	70	Software Programmable Amplifer	Z30-26		BUB
93	MM1-DIO	30	8	2.0	.80	0.0	5.0	12			Parallel I/O with up to 8 TTL Ports	Z30-6	MD3	CLI
94	DT2768	30	16			0.0	5.0	7.5	0	70	DEC LST 11,11/2 Bus Compatible	Z30-25		DTI
95	DT2768I	30	16			0.0	5.0	7.5	0	55	200V Bit to Bit Isol;All Data Lines	Z30-25		DTI
96▼#	EF68A21C	30	8	2.0	.80	0.0	5.0	550m	0	70	Peripheral Inter Adapter;Sp 1.5MHz	Z30-1	DL167	EFCF
97▼#	EF68A21CV	30	8	2.0	.80	0.0	5.0	550m	40	85	Peripheral Inter Adapter;Sp 1.5MHz	Z30-1	DL167	EFCF
98▼#	EF68A21PV	30	8	2.0	.80	0.0	5.0	550m	40	85	Peripheral Inter Adapter;Sp 1.5MHz	Z30-1	DL167	EFCF
99▼#	EF68B21C	30	8	2.0	.80	0.0	5.0	550m	0	70	Peripheral Inter Adapter;Sp 2.0MHz	Z30-1	DL167	EFCF
100▼#	EF68B21P	30	8	2.0	.80	0.0	5.0	550m	0	70	Peripheral Inter Adapter;Sp 2.A30-1	DL167	0MHz	EFCF
101▼#	EF6821C	30	8	2.0	.80	0.0	5.0	550m	0	70	Peripheral Inter Adapter;Sp 1.0MHz	Z30-1	DL167	EFCF
102▼#	EF6821CV	30	8	2.0	.80	0.0	5.0	550m	40	85	Peripheral Inter Adapter;Sp 1.0MHz	Z30-1	DL167	EFCF
103▼#	EF6821P	30	8	2.0	.80	0.0	5.0	550m	0	70	Peripheral Inter Adapter;Sp 1.0MHz	Z30-1	DL167	EFCF
104▼#	EF6821PV	30	8	2.0	.80	0.0	5.0	550m	40	85	Peripheral Inter Adapter;Sp 1.0MHz	Z30-1	DL167	EFCF
105	F3861	30	8	3.5	.80	0.0	12	250m†	0	70	Peripherial Input/Output for F8 Sys	Z30-24		FSC
106	F3871DC	30	8	2.0	.80	0.0	12	200m†	0	70	Peripherial Input/Output for F8 Sys	Z30-24	DL37c	FSC
107	F3871DL	30	8	2.0	.80	0.0	12	200m†	40	85	Peripheral Input/Output for F8 Sys	Z30-23	DL37c	FSC
108	F3871DM	30	8	2.0	.80	0.0	12	200m†	55	125	Peripheral Input/Output for F8 Sys	Z30-23	DL37c	FSC
109	F3871PC	30	8	2.0	.80	0.0	12	200m†	0	70	Peripheral Input/Output for F8 Sys	Z30-23	DL37c	FSC
110	F3871PL	30	8	2.0	.80	0.0	12	200m†	40	85	Peripheral Input/Output for F8 Sys	Z30-23	DL11i	FSC

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	[3] TYPE No.	[1] TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	[2] MFR. CODE
											SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ☑-ABS.MAX. %-OUTPUT			
1	F3871PM	30	8	2.0	.80	0.0	12	200m†	55	125	Peripheral Input/Output for F8 Sys	Z30-23	DL11i	FSC
2	PIC1640	30	8	2.0	.80	0.0	5.0				Programmable Interface Controller	Z30-10	DL42c	GIC
3	HCMP1851CD,P	30	2P	3.5	1.5	0.0	5.0		55	125	Prog Dual Port I/O or 20Bit Prog Lns			HAC
4	HCMP1851D,P	30	2P	7.0	3.0	0.0	12		55	125	Prog Dual Port I/O or 20Bit Prog Lns			HAC
5#	HD468A21P	30	2P	2.0	.80	0.0	5.0	650m	20	75	PI Adapter;Periph Set Up 135nS min	Z30-1		HITJ
6#	HD468B21P	30	2P	2.0	.80	0.0	5.0	650m	20	75	PI Adapter;Periph Set Up 135nS min	Z30-1		HITJ
7#	HD46821P	30	2P	2.0	.80§	0.0	5.0	650m	20	75	Peripheral Interface Adapter	Z30-1	DL☑	HITJ
8	IM6103AIDL	30	12	7.0	2.0	0.0	10	100m	40	85	Par IO Port;20 Programmable I/O Pins	Z30-16	DL37a	INL
9	IM6103AIPL	30	12	7.0	2.0	0.0	10	100m	40	85	Par IO Port;20 Programmable I/O Pins	Z30-16	DL86	INL
10	IM6103AMDL	30	12	7.0	2.0	0.0	10	100m	55	125	Par IO Port;20 Programmable I/O Pins	Z30-16	DL37a	INL
11	IM6103AMDL/883B	30	12	7.0	2.0	0.0	10	100m	55	125	Par IO Port;20 Programmable I/O Pins	Z30-16	DL37a	INL
12	IM6103CPL	30	12	3.0	.80	0.0	5.0	13m	0	70	Par IO Port;20 Programmable I/O Pins	Z30-16	DL86	INL
13	IM6103IDL	30	12	3.0	.80	0.0	5.0	13m	40	85	Par IO Port;20 Programmable I/O Pins	Z30-16	DL37a	INL
14	IM6103IPL	30	12	3.0	.80	0.0	5.0	13m	40	85	Par IO Port;20 Programmable I/O Pins	Z30-16	DL86	INL
15	IM6103MDL	30	12	3.0	.80	0.0	5.0	13m	55	125	Par IO Port;20 Programmable I/O Pins	Z30-16	DL37a	INL
16	IM6103MDL/883B	30	12	3.0	.80	0.0	5.0	13m	55	125	Par IO Port;20 Programmable I/O Pins	Z30-16	DL37a	INL
17	C8255	30	3P	2.0	.80	0.0	5.0	200m	0	70	Programmable Peripheral Interface	Z30-3	DL37	ITL
18	C8255A	30	24	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Peripheral Interface	Z30-7	DL70	ITL
19	C8255A-5	30	24	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Peripheral Interface	Z30-7	DL70	ITL
20	D8255A	30	24	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Peripheral Interface	Z30-7	DL38	ITL
21	D8255A-5	30	24	2.0	.80	0.0	5.0	1.0 ☑	0	70	Program Peripheral Interface,Cer Pkg	Z30-7	DL38	ITL
22	MD8255A	30	3P	2.0	.80	0.0	5.0	600m	55	125	Progmmable Peripheral Interface	Z30-7	DL85	ITL
23	P4265	30	8	3.5	.80	10	5.0	525m†	0	85	Programmable I/O Device	Z30-4	DL43	ITL
24	P8255A	30	24	2.0	.80	0.0	5.0	1.0 ☑	0	70	Program Peripheral Interface	Z30-7	DL42f	ITL
25	P8255A-5	30	24	2.0	.80	0.0	5.0	1.0 ☑	0	70	Progrm Peripheral Interface,Plas Pkg	Z30-7	DL42f	ITL
26▼#	M5L8255AP	30	12	2.0	.80	0.0	5.0	1.0	0	70	Programmable Peripheral Interface	Z30-3	DL123	MITJ
27▼#	M5L8255AP-5	30	12	2.0	.80	0.0	5.0	1.0	0	70	Programmable Peripheral Interface	Z30-3	DL123	MITJ
28#	M58740P	30	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Peripheral Interface	Z30-20	DL123	MITJ
29#	M58740S	30	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	Programmable Peripheral Interface	Z30-20	DL122	MITJ
30	MK3861	30	8	3.5	.80	0.0	12	480m	0	70	Peripheral Input/Output	Z30-14		MOS
31	MK3881N	30	8	2.0	.80	0.0	5.0	525m	0	70	Parallel I/O Controller Programmable	Z30-5	DL86a	MOS
32	MK3881P	30	8	2.0	.80	0.0	5.0	525m	0	70	Same as MK3881N Except Ceramic	Z30-5	DL42d	MOS
33	MC68A21L	30	2P	2.0	.80§	0.0	5.0	550m	0	70	PI Adapter;Periph Set up 135ns min	Z30-1	DL1d	MOTA
34	MC68A21P	30	2P	2.0	.80§	0.0	5.0	550m	0	70	PI Adapter;Periph Set up 135ns min	Z30-1	DL27	MOTA
35	MC68B21L	30	2P	2.0	.80§	0.0	5.0	550m	0	70	PI Adapter;Periph Set up 100ns min	Z30-1	DL1d	MOTA
36	MC68B21P	30	2P	2.0	.80§	0.0	5.0	550m	0	70	PI Adapter;Periph Set up 100ns min	Z30-1	DL27	MOTA
37	MC6820CL	30	2P	2.0	.80§	0.0	5.0	650m	40	85	Peripheral Interface Adapter	Z30-1	DL1d	MOTA
38	MC6820L	30	2P	2.0	.80§	0.0	5.0	650m	0	70	Peripheral Interface Adapter	Z30-1	DL1d	MOTA
39	MC6820P	30	2P	2.0	.80§	0.0	5.0	650m	0	70	Peripheral Interface Adapter	Z30-1	DL27	MOTA
40	MC6821CL	30	2P	2.0	.80§	0.0	5.0	550m	40	85	Peripheral Interface Adapter	Z30-1	DL1d	MOTA
41	MC6821CP	30	2P	2.0	.80§	0.0	5.0	550m	40	85	Peripheral Interface Adapter	Z30-1	DL27	MOTA
42	MC6821L	30	2P	2.0	.80§	0.0	5.0	550m	0	70	Peripheral Interface Adapter	Z30-1	DL1d	MOTA
43	MC6821P	30	2P	2.0	.80§	0.0	5.0	550m	0	70	Peripheral Interface Adapter	Z30-1	DL27	MOTA
44	MC6881L	30	3P	2.0	.80	0.0	5.0	367m	0	70	Triple Bi-Directional Bus Switch	Z30-12	DL76	MOTA
45	MC6881P	30	3P	2.0	.80	0.0	5.0	367m	0	70	Triple Bi-Directional Bus Switch	Z30-12	DL53	MOTA
46▼	MC68230	30	16			0.0	5.0				24 Prog I/O,plus 4 Handshake Lines			MOTA
47	MCS6520	30	8	2.4	.40	0.0	5.0	500m	0	70	Peripheral Interface Adapter			MTY
48	MCS6522	30	8	2.4	.40	0.0	5.0	1.0	0	70	Versatile Interface Adapter	Z30-9		MTY
49#	uPD8255C-E	30	3P	2.0	.80	0.0	5.0	200m	10	70	Programmable Peripheral Interface	Z30-3	DL11c	NECJ
50	uPD8041C	30	8	2.0	.80	0.0	5.0	675m	0	70	8-Bit Univ Prog Peripheral IF	Z30-22	DL101	NECM
51	uPD8041D	30	8	2.0	.80§	0.0	5.0	675m	0	70	8-Bit Univ Prog Peripheral IF	Z30-22	DL174	NECM
52	uPD8741AC	30	8	2.0	.80§	0.0	5.0	675m	0	70	8-Bit Univ Prog Peripheral IF	Z30-22	DL101	NECM
53	uPD8741AD	30	8	2.0	.80§	0.0	5.0	675m	0	70	8-Bit Univ Prog Peripheral IF	Z30-22	DL174	NECM
54	INS8255D	30	8	2.0	.80	0.0	5.0	160m†	0	70	Progm Peripheral Interface	Z30-18	DL37d	NSC
55	CDP1851CD	30		3.5	1.5	0.5	7.0		55	125	20 Programmable I/O Lines	Z30-30	DL221	RCA
56	CDP1851CE	30		3.5	1.5	0.5	7.0		40	85	20 Programmable I/O Lines	Z30-30	DL220	RCA
57	CDP1851D	30		3.5	1.5	0.5	11		55	125	20 Programmable I/O Lines	Z30-30	DL221	RCA
58	CDP1851E	30		3.5	1.5	0.5	11		40	85	20 Programmable I/O Lines	Z30-30	DL220	RCA
59	11696	30	8	3.5	-12	12	5.0	330m†	0	70	Par I/O;24 Bidir I/O Lines	Z30-19	DL☑	RKW
60	R6520	30	8	2.0	.80	0.0	5.0	500m	0	70	Peripheral Interface Adapter(PIA)	Z30-15	DL☑	RKW
61	R6522	30	8	2.4	.80	0.0	5.0	750m	0	70	Versatile Interface Adapter(VIA)	Z30-9	DL☑	RKW
62	2661-1I	30	8	2.0	.80	0.5	6.0	750m	0	70	EPIC;Baud Rate 50-19.2k bps Ceramic	Z30-28	DL☑	SIC
63	2661-1N	30	8	2.0	.80	0.5	6.0	750m	0	70	EPIC;Baud Rate 50-19.2k bps Plastic	Z30-28	DL☑	SIC
64	2661-2I	30	8	2.0	.80	0.5	6.0	750m	0	70	EPIC;Baud Rate 45.5-38.4k bps Cer	Z30-28	DL☑	SIC
65	2661-2N	30	8	2.0	.80	0.5	6.0	750m	0	70	EPIC;Baud Rate 45.5-38.4k bps Plas	Z30-28	DL☑	SIC
66	2661-3I	30	8	2.0	.80	0.5	6.0	750m	0	70	EPIC;Baud Rate 50-19.2k bps Ceramic	Z30-28	DL☑	SIC
67	2661-3N	30	8	2.0	.80	0.5	6.0	750m	0	70	EPIC;Baud Rate 50-19.2k bps Plastic	Z30-28	DL☑	SIC
68	MP8255I	30	3P	2.0	.80	0.0	5.0	200m†	0	70	Programmable Peripheral Interface	Z30-7	DL1b	SIC
69▼	N82S106F	30	8	2.0	.80§	0.0	7.0	895m	0	75	Bipolar Field Prog ROM Patch Ceramic	Z30-27		SIC
70	N82S106N	30	8	2.0	.80§	0.0	7.0	895m	0	75	Bipolar Field Prog ROM Patch Plastic	Z30-27		SIC
71▼	N82S107F	30	8	2.0	.80§	0.0	7.0	895m	0	75	Bipolar Field Prog ROM Patch Ceramic	Z30-27		SIC
72	N82S107N	30	8	2.0	.80§	0.0	7.0	895m	0	75	Bipolar Field Prog ROM Patch Plastic	Z30-27		SIC
73	N2655I	30	8	2.0	.80	0.0	5.0		0	70	Prog Peripheral Interface	Z30-17	DL1b	SIC
74▼	S82S106F	30	8	2.0	.80§	0.0	7.0	950m	55	125	Bipolar Field Prog ROM Patch Ceramic	Z30-27		SIC
75	S82S106N	30	8	2.0	.80§	0.0	7.0	950m	55	125	Bipolar Field Prog ROM Patch Plastic	Z30-27		SIC
76▼	S82S107F	30	8	2.0	.80§	0.0	7.0	950m	55	125	Bipolar Field Prog ROM Patch Ceramic	Z30-27		SIC
77	S82S107N	30	8	2.0	.80§	0.0	7.0	950m	55	125	Bipolar Field Prog ROM Patch Plastic	Z30-27		SIC
78	SYC68B21	30	2P	2.0	.80§	0.0	5.0	500m	0	70	Cycle Time 500ns;Int Pulse w 500n	Z30-1	DL177a	SYK
79	SYC6520	30	8	2.0	.80	0.0	5.0	500m	0	70	Speed 1MHz	Z30-15	DL26	SYK
80	SYC6520A	30	8	2.0	.80	0.0	5.0	500m	0	70	Speed 2MHz	Z30-15	DL26	SYK
81	SYC6521	30	2P	2.0	.80§	0.0	5.0	500m	0	70	Cycle Time 1.0us;Int Pulse w 500n	Z30-1	DL177a	SYK
82	SYC6521A	30	2P	2.0	.80§	0.0	5.0	500m	0	70	Cycle Time 500ns;Int Pulse w 5Z30-1	00ns	DL177a	SYK
83	SYC6522	30	8	2.4	.40	0.0	5.0	700m	0	70	Versatile Interface Adapter	Z30-9	DL26	SYK
84	SYC6522A	30	8	2.4	.40	0.0	5.0	700m	0	70	Versatile Interface Adapter	Z30-9	DL26	SYK
85	SYC6821	30	2P	2.0	.80§	0.0	5.0	500m	0	70	Cycle Time 1.0us;Int Pulse w 500n	Z30-1	DL177a	SYK
86	SYP68B21	30	2P	2.0	.80§	0.0	5.0	500m	0	70	Cycle Time 500ns;Int Pulse w 500n	Z30-1	DL177	SYK
87	SYP6520	30	8	2.0	.80	0.0	5.0	500m	0	70	Speed 1MHz	Z30-15	DL26	SYK
88	SYP6520A	30	8	2.0	.80	0.0	5.0	500m	0	70	Speed 2MHz	Z30-15	DL26	SYK
89	SYP6521	30	2P	2.0	.80§	0.0	5.0	500m	0	70	Cycle Time 1.0us;Int Pulse w 500n	Z30-1	DL177	SYK
90	SYP6521A	30	2P	2.0	.80§	0.0	5.0	500m	0	70	Cycle Time 500ns;Int Pulse w 500n	Z30-1	DL177	SYK
91	SYP6522	30	8	2.4	.40	0.0	5.0	700m	0	70	Versatile Interface Adapter	Z30-9	DL26	SYK
92	SYP6522A	30	8	2.4	.40	0.0	5.0	700m	0	70	Versatile Interface Adapter	Z30-9	DL26	SYK
93	SYP6821	30	2P	2.0	.80§	0.0	5.0	500m	0	70	Cycle Time 1.0us;Int Pulse w 500n	Z30-1	DL177	SYK
94	SBP9965	30	8	2.0	.80						uProc Mem-Mapped I/O Peripheral IF	Z30-21		TII
95	TMS9901JL	30		2.0	.80	0.0	5.0	300m	0	70	Programmable Systems Interface	Z30-13	DL1a	TII
96	TMS9901NL	30		2.0	.80	0.0	5.0	300m	0	70	Programmable Systems Interface	Z30-13	DL11	TII
97▼#	TMP8255AP	30	8	2.0	.80	0.0	5.0	1.0	0	70	Prog Peripheral Interface	Z30-8	DL179	TOSJ
98▼#	TMP8255AP-5	30	8	2.0	.80	0.0	5.0	1.0	0	70	Prog Peripheral Interface Z30-8		DL179	TOSJ
99	Z80-PIOCE	30	8	2.0	.80	0.0	5.0	350m	40	85	Par Interface Controller;Program	Z30-11	DL1m	ZIL
100	Z80-PIOCM	30	8	2.0	.80	0.0	5.0	350m	55	125	Par Interface Controller;Program	Z30-11	DL1m	ZIL
101	Z80-PIOCS	30	8	2.0	.80	0.0	5.0	350m	0	70	Par Interface Controller;Program	Z30-11	DL1m	ZIL
102	Z80-PIOPS	30	8	2.0	.80	0.0	5.0	350m	0	70	Par Interface Controller;Program	Z30-11	DL1m	ZIL
103	Z80A-PIOCE	30	8	2.0	.80	0.0	5.0	350m	40	85	Par Interface Controller;Program	Z30-11	DL1m	ZIL
104	Z80A-PIOCM	30	8	2.0	.80	0.0	5.0	350m	55	125	Par Interface Controller;Program	Z30-11	DL1m	ZIL
105	Z80A-PIOCS	30	8	2.0	.80	0.0	5.0	350m	0	70	Par Interface Controller;Program	Z30-11	DL1m	ZIL
106	Z80A-PIOPS	30	8	2.0	.80	0.0	5.0	350m	0	70	Par Interface Controller;Program	Z30-11	DL1m	ZIL
107	Z8034UPC	30	8	2.0	.80	0.0	5.0				For Distributed Processing Z-Bus use	Z30-29		ZIL
108▼#	EF68A21P	30	8	2.0	.80	0.0	5.0	550m	0	70	Peripheral Inter Adapter;Sp 1.Z30-1	DL167	EFCF	5MHz
109	MC6882AL	31	8	2.0	.80§	0.0	5.0	625m	0	75	Octal Buffer/Latch,Hold Time 10ns	Z31-5	DL133	MOTA
110	MC6882AP	31	8	2.0	.80§	0.0	5.0	625m	0	75	Octal Buffer/Latch,Hold Time 10ns	Z31-5	DL132	MOTA

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ☑-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1	MC6882BL	31	8	2.0	.80§	0.0	5.0	625m	0	75	Octal Buffer/Latch,Hold Time 10ns	Z31-6	DL133	MOTA
2	MC6882BP	31	8	2.0	.80§	0.0	5.0	625m	0	75	Octal Buffer/Latch,Hold Time 10ns	Z31-6	DL132	MOTA
3	MC6885L	31	6D	2.0	.80§	0.0	5.0	490m	0	75	Hex 3 State Buffer/Non-Inverting	Z31-1	DL76	MOTA
4	MC6885P	31	6D	2.0	.80§	0.0	5.0	490m	0	75	Hex 3 State Buffer/Non-Inverting	Z31-1	DL53	MOTA
5	MC6886L	31	6D	2.0	.80§	0.0	5.0	445m	0	75	Hex 3 State Buffer/Inverting	Z31-2	DL76	MOTA
6	MC6886P	31	6D	2.0	.80§	0.0	5.0	445m	0	75	Hex 3 State Buffer/Inverting	Z31-2	DL53	MOTA
7	MC6887L	31	6D	2.0	.80§	0.0	5.0	490m	0	75	Hex 3 State Buffer/Non-Inverting	Z31-3	DL76	MOTA
8	MC6887P	31	6D	0.0	.80§	0.0	5.0	490m	0	75	Hex 3 State Buffer/Non-Inverting	Z31-3	DL53	MOTA
9	MC6888L	31	6D	2.0	.80§	0.0	5.0	445m	0	75	Hex 3 State Buffer/Inverting	Z31-4	DL76	MOTA
10	MC6888P	31	6D	0.0	.80§	0.0	5.0	445m	0	75	Hex 3 State Buffer/Inverting	Z31-4	DL53	MOTA
11	8T95F	31		2.0	.80§	0.0	5.0				Hex Buffer;Prog. Delay 9/7ns On/Off	Z31-8		SIC
12	8T95N	31		2.0	.80§	0.0	5.0				Hex Buffer;Prog. Delay 9/7ns On/Off	Z31-8		SIC
13	8T96F	31		2.0	.80§	0.0	5.0				Hex Buffer;Prog. Delay 6/7ns On/Off	Z31-10		SIC
14	8T96N	31		2.0	.80§	0.0	5.0				Hex Buffer;Prog. Delay 6/7ns On/Off	Z31-10		SIC
15	8T97F	31		2.0	.80§	0.0	5.0				Hex Inverter;Prog.Delay 9/7nS On/Off	Z31-9		SIC
16	8T97N	31		2.0	.80§	0.0	5.0				Hex Inverter;Prog.Delay 9/7nS On/OFF	Z31-9		SIC
17	8T98F	31		2.0	.80§	0.0	5.0				Hex Inverter;Prog.Delay 6/7nS On/Off	Z31-11		SIC
18	8T98N	31		2.0	.80§	0.0	5.0				Hex Inverter;Prog.Delay 6/7nS On/OFF	Z31-11		SIC
19	COM8046T	32				0.0	5.0				Baud Rate Gene;UART/USRT/ASTRO Comp	DL☑	SMC	
20	Am8224DC	32	2Ø	2.6	.80	0.0	12	70m	0	70	Clock Gen/Driver for Am8080A/9080A	Z32-8	DL87	AMV
21	Am8224DM	32	2Ø	2.8	.80	0.0	12	720m	55	125	Clock Gen/Driver For Am8080A/9080A	Z32-8	DL87	AMV
22	Am8224PC	32	2Ø	2.6	.80	0.0	12	720m	0	70	Clock Gen/Driver For Am8080A/9080A	Z32-8	DL4a	AMV
23	Am8224XC	32	2Ø	2.6	.80	0.0	12	70m	0	70	Clock Gen/Driver For Am8080A/9080A	Z32-8	CH2	AMV
24	mN638	32	2Ø	2.0	.80		18.5	414m	0	70	Clock Driver for mN606 RAM	Z32-13	DL83	DGC
25	mN640	32	2Ø	2.0	.80		15	680m	0	70	CPU Clock Driver;Dual 3 Input	Z32-13a	DL83	DGC
26▼#	EFF6875C	32	2Ø	2.0	.80§	0.0	5.0		0	70	Generator/Driver Clock;Fo 2.0MHz max		DL77	EFCF
27▼#	EFF6875P	32	2Ø	2.0	.80§	0.0	5.0		0	70	Generator/Driver Clock;Fo 2.0MHz max		DL33d	EFCF
28#	HD26501	32	2Ø	2.0	.80	0.0	5.0				Clock Pulse Generator/Controller	Z32-12	DL77a	HITJ
29	C4201	32	2Ø	3.5	2.0	5.0	15	300m	0	70	Clock Generator,Crystal Controlled	Z32-7	DL39	ITL
30	C7230	32		2.0	.80	0.0	12		0	70	Current Pulse Generator/Bubble Mem	Z03-38	DL☑	ITL
31	C8224	32	2Ø	2.0	.80	0.0	12	719m	0	70	Clock Generator And Driver	Z32-4	DL39	ITL
32	C8284	32		2.0	.80	0.0	5.0	1.0 ☑	0	70	Clock Gen and Driver;Xtal f 23MHz	Z32-14	DL144	ITL
33	D4201	32	2Ø	3.5	2.0	5.0	15	300m	0	70	Clock Generator,Crystal Controlled	Z32-7	DL6a	ITL
34	D7230	32		2.0	.80	0.0	12		0	70	Current Pulse Generator/Bubble Mem	Z03-38	DL215	ITL
35	D8210	32	8	2.0	.80	0.0	12	550m	0	70	TTL-TO-MOS Level Shift,Clock Driver	Z32-5	DL40	ITL
36	D8224	32	2Ø	2.0	.80	0.0	12	719m	0	70	Clock Generator And Driver	Z32-4	DL6a	ITL
37	D8284	32		2.0	.80	0.0	5.0	1.0 ☑	0	70	Clock Gen and Driver;Xtal f 23MHz	Z32-14	DL145	ITL
38	MD8224	32	2Ø	2.0	.80	0.0	12	719m	55	125	Clock Generator And Driver	Z32-4	DL6a	ITL
39	P4201	32	2Ø	3.5	2.0	5.0	15	300m	0	70	Clock Generator,Crystal Controlled	Z32-7	DL33	ITL
40	P7230	32		2.0	.80	0.0	12		0	70	Current Pulse Generator/Bubble Mem	Z03-38	DL214	ITL
41	P8210	32	8	2.0	.80	0.0	12	550m	0	70	TTL-TO-MOS Level Shift,Clock Driver	Z32-5	DL20a	ITL
42	P8224	32	2Ø	2.0	.80	0.0	12	719m	0	70	Clock Generator And Driver	Z32-4	DL33	ITL
43	P8284	32		2.0	.80	0.0	5.0	700m	0	70	Clock Gen and Driver,Xtal f 25MHz	Z32-14	DL182	ITL
44#	M5L8224P	32		2.0	.80	0.0	12	800m☑	0	70	Clock Gen/Driver;Xtal Controlled	Z32-8		MITJ
45#	M54550P	32	2Ø	2.0	.80	0.0	12	800m☑	0	75	Clock Generator and Driver	Z32-8	DL127	MITJ
46	MC6870A	32	2Ø	2.4	.40%	0.0	5.0	285m	0	70	2 Phase Limited Function MPU Clock	Z32-2	MD1	MOTA
47	MC6871A	32	2Ø	2.4	.40%	0.0	5.0	285m	0	70	2 Phase Full Function MPU Clock	Z32-3	MD1	MOTA
48	MC6871B	32	2Ø	2.4	.40%	0.0	5.0	285m	0	70	2 Phase Alternate Function MPU Clock	Z32-3a	MD1	MOTA
49▼	MC6875AL	32		2.0	.80	0.0	5.0		55	125	Requires Heat Sink above TA 95°C	Z32-11	DL76	MOTA
50	MC6875L	32	2Ø	2.0	.80	0.0	5.0	350m†	0	70	2 Phase Clock Generator/Driver	Z32-11	DL76	MOTA
51	MC6875P	32	2Ø	2.0	.80	0.0	5.0	350m†	0	70	2 Phase Clock Generator/Driver	Z32-11	DL53	MOTA
52	MPQ6842	32	2Ø	4.7	.30	0.0	5.0	900m☑	55	150	MPU Clock Buffer	Z32-1	DL28	MOTA
53	uPB8224C	32	4	2.0	.80	0.0	12		0	70	Clock Generator And Driver For8080A	Z32-4	DL93	NECM
54	uPB8224D	32	4	2.0	.80	0.0	12	719m	0	70	Clock Generator And Driver For 8080A	Z32-4	DL6f	NECM
55	DP4201J	32				10	5.0	375m	0	70	Clock Gen/MOS,TTL Out/DC-6MHz	Z32-17	DL6q	NSC
56	DP4201N	32				10	5.0	375m	0	70	Clock Gen/MOS,TTL Out/DC-6MHz	Z32-17	DL33a	NSC
57	DP8224J	32		2.0	.80	0.0	12	719m	0	70	Clock Gen/Dr;Xtal Controlled Osc	Z32-18	DL6q	NSC
58	DP8224N	32	8	2.0	.80	0.0	12	719m	0	70	Clock Gen/Dr;Xtal Controlled Osc	Z32-18	DL33a	NSC
59	DP8302J	32		2.0	.80	12	5.0	850m	0	70	PACE Sys Timing Element;2.6667M Xtal	Z32-16	DL6q	NSC
60	DP8302N	32		2.0	.80	12	5.0	850m	0	70	PACE Sys Timing Element;2.6667M Xtal	Z32-16	DL33a	NSC
61	DP8305J	32		2.0	.80	12	5.0	850m	0	70	PACE Sys Timing Elemen;4.0MHz Xtal	Z32-16	DL6q	NSC
62	COM5016	32	Δ			0.0	12				Dual Baud Rate Gene;Full Duplex	Z32-19	DL☑	SMC
63	COM5016T	32	Δ			0.0	12				Dual Baud Rate Gene;Full Duplex	Z32-19	DL☑	SMC
64	COM5026	32				0.0	12				Baud Rate Gene;UART/USRT/ASTRO	Z32-20a	DL☑	SMC
65	COM5026T	32				0.0	12				Baud Rate Gene;UART/USRT/ASTRO	Z32-20a	DL☑	SMC
66	COM8004	32	9S			0.0	5.0				SDLC 32 Bit CRC	Z32-22	DL☑	SMC
67	COM8046	32				0.0	5.0				Baud Rate Gene;UART/USRT/ASTRO Comp	Z32-21	DL☑	SMC
68	COM8116	32	Δ			0.0	5.0				Baud Rate Gene;Full Duplex;COM5016	Z32-19	DL☑	SMC
69	COM8116T	32	Δ			0.0	5.0				Baud Rate Gene;Compatible w COM5026	Z32-20	DL☑	SMC
70	COM8116Y	32	Δ			0.0	5.0				Baud Rate Gene;Full Duplex;COM5016	Z32-19	DL☑	SMC
71	COM8126	32				0.0	5.0				Baud Rate Gene;Compatible w/COM5026	Z32-20	DL☑	SMC
72	COM8126T	32				0.0	5.0				Baud Rate Gene;Compatible w/COM5026	Z32-20	DL☑	SMC
73	COM8136	32	Δ			0.0	5.0				Baud Rate Gene;Full Duplex;COM5036	Z32-19a	DL☑	SMC
74	COM8136T	32	Δ			0.0	5.0				Baud Rate Gene;Full Duplex;COM5036	Z32-19a	DL☑	SMC
75	COM8146	32				0.0	5.0				Baud Rate Gene;Compatible w/COM5046	Z32-21-	DL☑	SMC
76	COM8146T	32				0.0	5.0				Baud Rate Gene;Compatible w/COM5046	Z32-21	DL☑	SMC
77	SN74LS424J	32	2Ø	2.0	.80	0.0	12	720m	0	70	2 Phase Clock Gen/Drv For TMS8080A	Z32-10		TII
78	SN74LS424N	32	2Ø	2.0	.80	0.0	12	720m	0	70	2 Phase Clock Gen/Drv For TMS8080A	Z32-10		TII
79	TIM9904	32	4Ø	2.0	.80	0.0	12.0	1.1	0	70	4Ø Clock Gen/Driver;Plas or Cer Pkg	Z32-15		TII
80#	TFK10696	33	3P	3.5	-12	12	5.0	330m	0	70	Gen Purpose I/O;12 Inputs;12 Outputs	Z33-3		ALGG
81▼	Am2950DC	33	8	2.0	.80	0.0	5.0		0	70	Non-Inverting		DL49	AMD
82▼	Am2950DM	33	8	2.0	.80	0.0	5.0		55	125	Non-Inverting		DL49	AMD
83▼	Am2950FM	33	8	2.0	.80	0.0	5.0		55	125	Non-Inverting		FP5	AMD
84▼	Am2951DC	33	8	2.0	.80	0.0	5.0		0	70	Inverting		DL49	AMD
85▼	Am2951DM	33	8	2.0	.80	0.0	5.0		55	125	Inverting	DL49		AMD
86▼	Am2951FM	33	8	2.0	.80	0.0	5.0		55	125	Inverting		FP5	AMD
87▼	Am2951PC	33	8	2.0	.80	0.0	5.0		0	70	Inverting		DL143a	AMD
88	S68488P	33	8	2.0	.80	0.0	5.0	600m	0	70	General Purpose Interface Adapter	Z33-20	DL2	AMI
89	Am8212DM	33	8	2.0	.80§	0.0	5.0	650m	55	125	8 Bit I/O Port; Hermetic Dip Pkg	Z33-6	DL88	AMV
90	Am8212XC	33	8	2.0	.85§	0.0	5.0	650m	55	125	8 Bit I/O Port,Hermetic Dip Pkg	Z33-6	CH4	AMV
91	D/7A-W	33	8			18	18				Multi-Channel uComputer/Anolog Inter	Z33-34	DL☑	CRO
92	mN603	33	16	2.7	.80	4.25	14	657m	0	70	Interprets and Executes I/O Instr	Z33-15	DL6n	DGC
93	F68488	33	8	2.0	.80§	0.0	5.0	600m†	0	70	Interface Adapter	Z33-28	DL86	FSC
94	IOB1680	33	8	2.4	.65	0.0	12		0	70	I/O Buffer;Presetable 16 Bit Timer	Z33-10	DL42e	GIC
95	HCMP1852CD	33	8	3.5	1.5	0.0	5.0	500u†	55	125	8 Bit CMOS Input/Output Port	Z33-5	DL☑	HAC
96	HCMP1852D	33	8	7.0	3.0	0.0	10	1.0m†	55	125	8 Bit CMOS Input/Output Port	Z33-5	DL☑	HAC
97	B8212	33	8	2.0	.85§	0.5	7.0	1.5 ☑	0	75	8-Bit Input/Output Port	Z33-16	DL186	ITL
98	B8243	33	4	2.0	.80	0.0	5.0	200m☑	0	70	I/O Expander; Four 4-Bit I/O Ports	Z33-9	DL186	ITL
99	B8741A	33	8	2.2	.80	0.0	5.0	625m	0	70	Gen Purpose Prog Interface Device	Z33-25	DL148	ITL
100	C8041A	33	8	2.2	.80	0.0	5.0	1.5 ☑	0	70	General Purpose Prog Inter Device	Z33-25	DL70	ITL
101	C8243	33	4	2.0	.80	0.0	5.0	200m☑	0	70	I/O Expander; Four 4-Bit I/O Ports	Z33-9	DL210	ITL
102	C8282	33	8	2.0	.80§	0.0	5.0	1.0 ☑	0	70	8-Bit I/O Port;I/O Delay 35ns	Z33-22	DL212	ITL
103	C8283	33	8	2.0	.80§	0.0	5.0	1.0 ☑	0	70	8-Bit I/O Port;I/O Delay 35ns	Z33-23	DL212	ITL
104	C8291	33	8	2.0	.80	0.0	5.0	900m	0	70	GIBP Talker/Listener	Z33-24	DL70	ITL
105	C8292	33	8	2.0	.80	0.0	5.0	1.5 ☑	0	70	GIBP Controller	Z33-29	DL70	ITL
106	C8293	33	8	2.0	.80	0.0	5.0	1.0 ☑	0	70	GIBP Controller	Z33-29	DL70	ITL
107	C8641A	33	8	2.2	.80	0.0	5.0	1.5 ☑	0	70	Gen Purpose Prog Inter Device	Z33-25	DL70	ITL
108	C8741A	33	8	2.2	.80	0.0	5.0	1.5 ☑	0	70	Gen Purpose Prog Inter Device	Z33-25	DL70	ITL
109	D3212	33	8	2.0	.85§	0.0	5.0	650m	0	75	Multi-Mode Latch Buffer	Z33-16	DL7a	ITL
110	D8041A	33	8	2.2	.80	0.0	5.0	1.5 ☑	0	70	General Purpose Prog Inter Device	Z33-25	DL148	ITL

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN Ø-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1	D8156	33	8	2.0	.80	0.5	7.0	1.5 Ø	0	70	Prog. 14-Bit Binary Counter/Timer	A152	DL148	ITL
2	D8212	33	8	2.0	.85	0.0	5.0	650m	0	75	8 Bit Input/Output Port	Z33-16	DL7a	ITL
3	D8243	33	4	2.0	.80	0.0	5.0	200m	0	70	I/O Expander; Four 4 Bit I/O Ports	Z33-9	DL7h	ITL
4	D8282	33	8	2.0	.80§	0.0	5.0	1.0 Ø	0	70	8-Bit I/O Port;I/O Delay 35ns	Z33-22	DL211	ITL
5	D8283	33	8	2.0	.80§	0.0	5.0	1.0 Ø	0	70	8-Bit I/O Port;I/O Delay 35ns	Z33-23	DL211	ITL
6	D8291	33	8	2.0	.80	0.0	5.0		0	70	GPIB Talker Listener,Cer Pkg	Z33-24	DL38	ITL
7	D8292	33	8	2.0	.80	0.0	5.0		0	70	GPIB Controller,Cer Pkg		DL38	ITL
8	D8293	33	8	2.0	.80	0.0	5.0	1.0 Ø	0	70	GIBP Controller	Z33-29	DL148	ITL
9	D8641A	33	8	2.2	.80	0.0	5.0	1.5 Ø	0	70	Gen Purpose Prog Inter Device	Z33-25	DL148	ITL
10	D8741A	33	8	2.2	.80	0.0	5.0	1.5 Ø	0	70	Gen Purpose Prog Inter Device	Z33-25	DL148	ITL
11	MD3212	33	8	2.0	.85§	0.0	5.0	650m	55	125	Multi-Mode Latch Buffer	Z33-16	DL7a	ITL
12	MD8212	33	8	2.0	.80	0.0	5.0	725m	55	125	8 Bit Input/Output Port	Z33-16	DL7a	ITL
13	P3212	33	8	2.0	.85§	0.0	5.0	650m	0	75	Multi-Mode Latch Buffer	Z33-16	DL14a	ITL
14	P4207	33	8	3.5	.80	10	5.0	400m	0	70	4 Input/12 Output Lines	Z33-2	DL43	ITL
15	P4209	33	8	3.5	.80	10	5.0	400m	0	70	12 Input/4 Output Lines	Z33-2a	DL43	ITL
16	P4211	33	8	3.5	.80	10	5.0	400m	0	70	8 Input/8 Output Lines	Z33-2b	DL43	ITL
17	P8041A	33	8	2.2	.80	0.0	5.0	625m	0	70	Gen Purpose Prog Interface Device	Z33-25	DL149	ITL
18	P8212	33	8	2.0	.85	0.0	5.0	650m	0	75	8 Bit Input/Output Port	Z33-16	DL14a	ITL
19	P8243	33	4	2.0	.80	0.0	5.0	200m	0	70	I/O Expander; Four 4 Bit I/O Ports	Z33-9	DL14c	ITL
20	P8282	33	8	2.0	.80§	0.0	5.0	800m	0	70	8 Bit IO Port,IO Delay 35ns Max	Z33-22	DL118	ITL
21	P8283	33	8	2.0	.80§	0.0	5.0	800m	0	70	8 Bit IO Port,IO Delay 25ns Max	Z33-23	DL118	ITL
22	P8291	33	8	2.0	.80	0.0	5.0		0	70	GPIB Talker Listener,Plas Pkg	Z33-24	DL42f	ITL
23	P8292	33	8	2.0	.80	0.0	5.0		0	70	GPIB Controller,Plas Pkg		DL42f	ITL
24	P8293	33	8	2.0	.80	0.0	5.0	1.0 Ø	0	70	GIBP Controller	Z33-29	DL149	ITL
25	P8641A	33	8	2.2	.80	0.0	5.0	1.5 Ø	0	70	Gen Purpose Prog Inter Device	Z33-25	DL149	ITL
26	P8741A	33	8	2.2	.80	0.0	5.0	1.5 Ø	0	70	Gen Purpose Prog Inter Device	Z33-25	DL149	ITL
27#	M54552P	33	8	2.0	.85	0.0	5.0	800mØ	0	75	8 Bit Input/Output Port	Z33-16	DL124	MITJ
28▼	MC68488L	33		2.0	.80	0.0	5.0		0	70	Read/Write Cycle Time 1.0us min	Z33-20		MOTA
29▼	MC68488P	33		2.0	.80	0.0	5.0		0	70	Read/Write Cycle Time 1.0us min	Z33-20		MOTA
30#	uPD752C	33	8	3.0	.65	5.0	12	185m	10	70	Input/Output Port	Z33-7	DL18e	NECJ
31#	uPD752D	33	8	3.0	.65	5.0	12	185m	10	70	Input/Output Port	Z33-7	DL45b	NECJ
32#	uPD762C	33		2.2	.60	0.0	5.0	175m†	10	70	Interface Chip	Z33-8	DL59	NECJ
33	uPD8243C	33	4	2.0	.80	0.0	5.0	100m	0	70	I/O Expander W/Four 4-Bit Bidir I/Os	Z33-9	DL102	NECM
34	uPD8243D	33	4	2.0	.80	0.0	5.0	100m	0	70	I/O Expander W/Four 4-Bit Bidir I/Os	Z33-9	DL171	NECM
35	DP8212J	33	8	2.0	.85§	0.0	5.0	682m	0	75	8-Bit I/O Port/Replaces Buf,LchgMux	Z33-27	DL18	NSC
36	DP8212N	33	8	2.0	.85§	0.0	5.0	682m	0	75	8-Bit I/O Port/Replaces Buf,LchgMux	Z33-27	DL18g	NSC
37	INS8212J	33	8	2.0	.85§	0.0	5.0	650m	0	75	8 Bit Input/Output Port	Z33-19	DL7k	NSC
38	INS8212N	33	8	2.0	.85§	0.0	5.0	650m	0	75	8 Bit Input/Output Port	Z33-19	DL18g	NSC
39	INS8243	33	4	2.0	0.8	0.0	5.0	100m	0	70	I/O Expander;IF W/INS8048/49/50 uCT	Z33-30	DL213	NSC
40#	MP8243I	33	4	2.0	.80	0.0	5.0	200m	0	70	I/O Expander;Four 4-Bit I/O Ports	Z33-9	DLØ	PHIN
41#	MP8243N	33	4	2.0	.80	0.0	5.0	200m	0	70	I/O Expander;Four 4-Bit I/O Ports	Z33-9	DLØ	PHIN
42	CDP1852CD	33	8	5.0†	0.0†	0.0	5.0	500u†	55	125	8 Bit CMOS Input/Output Port	Z33-5	Δ015AG	RCA
43	CDP1852CE	33	8	5.0†	0.0†	0.0	5.0	500u†	40	85	8-Bit CMOS Input/Output Ports Z	Z33-5	Δ015Ag	RCA
44	CDP1852D	33	8	10†	0.0†	0.0	10	1.0m†	55	125	8 Bit CMOS Input/Output Port	Z33-5	Δ015AG	RCA
45	CDP1852E	33	8	5.0†	0.0†	0.0	5.0	500u†	40	85	8-Bit CMOS Input/Output Ports	Z33-5	Δ015Ag	RCA
46	CDP1869CD	33	4	3.5	1.5	0.0	7.0	500m	55	125	Latch/Decoder Mem Interface	Z33-35	DL221	RCA
47	CDP1869CE	33	4	3.5	1.5	0.0	7.0	500m	40	85	Latch/Decoder Mem Interface	Z33-35	DL220	RCA
48	CDP1869D	33	4	3.5	1.5	0.0	7.0	500m	55	125	Latch/Decoder Mem Interface	Z33-35	DL221	RCA
49	CDP1869E	33	4	3.5	1.5	0.0	7.0	500m	40	85	Latch/Decoder Mem Interface	Z33-35	DL220	RCA
50	CDP1870CD	33	4	3.5	1.5	0.0	7.0	500m	55	125	Latch/Decoder Mem Interface	Z33-36	DL221	RCA
51	CDP1870CE	33	4	3.5	1.5	0.0	7.0	500m	40	85	Latch/Decoder Mem Interface	Z33-36	DL220	RCA
52	CDP1870D	33	4	3.5	1.5	0.0	7.0	500m	55	125	Latch/Decoder Mem Interface	Z33-36	DL221	RCA
53	CDP1870E	33	4	3.5	1.5	0.0	7.0	500m	40	85	Latch/Decoder Mem Interface	Z33-36	DL220	RCA
54	10453	33		3.5	-12	12	5.0	330m	0	70	Parallel Data Controller	Z33-14	DL44	RKW
55	10696	33	3P	3.5	-12	12	5.0	330m	0	70	General Purpose Input/Output	Z33-3	DL44	RKW
56#	HEF4738VE	33	8	7.0	3.0	0.0	10	400mØ	40	85	IEC/IEEE Bus Interface,Cer Pkg	Z33-21	DL116	RTCF
57#	HEF4738VP	33	8	7.0	3.0	0.0	10	400mØ	40	85	IEC/IEEE Bus Interface,Plastic Pkg	Z33-21	DL117	RTCF
58	N8T31F	33	8	2.0	.80	0.0	5.0	750m	0	70	Bidirectional I/O Port	Z33-1	DL7	SIC
59	N8T31N	33	8	2.0	.80	0.0	5.0	750m	0	70	Bidirectional I/O Port	Z33-1	DL14	SIC
60	N8T32F	33	8	2.0	.80§	0.0	5.0	750m	0	70	Bidir Port/Interf Vector Byte;Synch	Z33-11	DL7j	SIC
61	N8T32N	33	8	2.0	.80§	0.0	5.0	750m	0	70	Bidir Port/IVB;Synch;Plas Pkg	Z33-11	DL7j	SIC
62	N8T33F	33	8	2.0	.80	0.0	5.0	750m	0	70	Bidir Port/IVB;Synch;Cer Pkg	Z33-11	DL7j	SIC
63	N8T33N	33	8	2.0	.80	0.0	5.0	750m	0	70	Bidir Port/IVB;Synch;Plas Pkg	Z33-11	DL7j	SIC
64	N8T35F	33	8	2.0	.80	0.0	5.0	750m	0	70	Bidir Port/IVB;Asynch;Cer Pkg	Z33-11	DL7j	SIC
65	N8T35N	33	8	2.0	.80	0.0	5.0	750m	0	70	Bidir Port/IVB;Asynch;Plas Pkg	Z33-11	DL7j	SIC
66	N8T36F	33	8	2.0	.80§	0.0	5.0	750m	0	70	Bidir Port/IVB;Asynch;Cer Pkg	Z33-11	DL7j	SIC
67	N8T36N	33	8	2.0	.80§	0.0	5.0	750m	0	70	Bidir Port/IVB;Asynch;Plas Pkg	Z33-11	DL7j	SIC
68	N8T39I	33	8	2.0	.80§	0.0	5.0	1.0	0	70	Bus Expander;tpd 15ns,Cer Pkg	Z33-12	DL105	SIC
69	N8T39N	33	8	2.0	.80§	0.0	5.0	1.0	0	70	Bus Expander;tpd 15ns,Plas Pkg	Z33-12	DL105	SIC
70	N8T58I	33	8	2.0	.80§	0.0	5.0	1.0	0	70	Transparent Bus Expander;Cer Pkg	Z33-18	DL105	SIC
71	N8T58N	33	8	2.0	.80§	0.0	5.0	1.0	0	70	Transparent Bus Expander;Plas Pkg	Z33-18	DL105	SIC
72	TMS5501	33	4	3.3	.80	5.0	12	565m	0	70	Multifunction I/O Controller	Z33-13	DL1a	TII
73	Z80ADARTCE	33		2.0	.80	0.0	5.0	500m	40	85	Max Clock Rate 4.0MHz	Z21-26	DL190	ZIL
74	Z80ADARTCM	33		2.0	.80	0.0	5.0	500m	55	125	Max Clock Rate 4.0MHz	Z21-26	DL190	ZIL
75	Z80ADARTCS	33		2.0	.80	0.0	5.0	500m	0	70	Max Clock Rate 4.0MHz	Z21-26	DL190	ZIL
76	Z80ADARTPS	33		2.0	.80	0.0	5.0	500m	0	70	Max Clock Rate 4.0MHz	Z21-26	DL189	ZIL
77	Z80DARTCE	33		2.0	.80	0.0	5.0	500m	40	85	Max Clock Rate 2.5MHz	Z21-26	DL190	ZIL
78	Z80DARTCM	33		2.0	.80	0.0	5.0	500m	55	125	Max Clock Rate 2.5MHz	Z21-26	DL190	ZIL
79	Z80DARTCS	33		2.0	.80	0.0	5.0	500m	0	70	Max Clock Rate 2.5MHz	Z21-26	DL190	ZIL
80	Z80DARTPS	33		2.0	.80	0.0	5.0	500m	0	70	Max Clock Rate 2.5MHz	Z21-26	DL189	ZIL
81	Z8036CIO	33	8	2.0	.80	0.0	5.0				Counter/Timer and Parallel I/O Unit	Z33-31		ZIL
82	Z8038FIO	33	8	2.0	.80	0.0	5.0				Async Bidirectional FIFO Buffer	Z33-32		ZIL
83	Z8060FIFO	33	8	2.0	.80	0.0	5.0				Async Bidirectional FIFO Buffer	Z33-33		ZIL
84▼	Z-CIO-UCS	33	8			0.0	5.0				Counter/Timer and Parallel I/O Unit		DL190	ZIL
85▼	Z-CIO-UPS	33	8			0.0	5.0				Counter/Timer and Parallel I/O Unit		DL189	ZIL
86▼	8X02I,XL	34		2.0	.80§	0.0	5.0		0	70	4-Level Stack Reg;3-Bit Command Code			SIC
87	MP10	40	8	2.0	.80	15	15	1.3	0	70	2 Channel Analog Output For 8080	Z40-1	DL61	BUB
88	MP11	40	8	2.0	.80	15	15	1.3	0	70	2 Channel Analog Output For 6800	Z40-1	DL61	BUB
89	MM1-AI/AO	40	12			15	15	7.2	0	70	Analog I/O Data Acq Sys;12 Bit D/A	Z45-2		CLI
90	DT2726	40	12			0.0	5.0	2.0	0	70	4Ch 12-Bit D/A Converter	Z40-5		DTI
91	DT2727	40	8			0.0	5.0	2.0	0	70	4Ch 8-Bit D/A Converter	Z40-5		DTI
92	DAC1600	40	10	2.2	.65	0.0	12	325m	0	75	Dual DAC;Two 10 Bit PWM Output	Z40-2	DL42e	GIC
93#	MN1204	40	12	2.4	.80	0.0	5.0		30	70	Quad D/A Converter,Osc Freq 1.3MHz	Z40-4	DL166	MATJ
94▼	CDP18S642	40	12			15	15		0	70	Bipolar or Unipolar Voltage Output			RCA
95	MP20	41	8	2.0	.80	15	15	1.3	0	70	16 Channel Analog Input For 8080	Z41-1	DL62	BUB
96	MP21	41	8	2.0	.80	15	15	1.3	0	70	16 Channel Analog Input For 6800	Z41-1	DL62	BUB
97	MP22	41	12L	2.0	.80	15	15	1.0	0	70	16 Channel Microperiph Analog Input		MDØ	BUB
98	DT2722	41	12			0.0	5.0	3.8	0	70	16 SE or 8 Differential Chs	Z41-7		DTI
99	DT2724	41	12			0.0	5.0	3.8	0	70	16 SE or 8 Differential Chs	Z41-7		DTI
100	DT2725	41	12			0.0	5.0	3.8	0	70	10V E max In;4 Ch Sys;CMR ±250 max	Z41-7		DTI
101	DT2781	41	12			0.0	5.0	7.5	0	70	16 Chan/12 Bit AD;2 Ind. 12 Bit DA	Z41-6		DTI
102	DT2785	41	12			0.0	5.0	7.5	0	70	16 Chan/12 Bit AD;2 Ind. 12 Bit DA	Z41-6		DTI
103▼	ST-724	41	12			0.0	5.0		0	55	Multibus Compat;±15Vdc On Bd Conv			DTL
104▼	ST-LSI-RLY	41	12			0.0	12		0	70	User Selectable Output Coding			DTL
105#	ADC228/E6	41	8			0.0	5.0	1.5	0	55	8 Channel Data Acquistion Module			EURF
106	ICL8052ACDD/7103ACDI	41	9L	2.4	.40%	15	15	500mØ	0	70	4 1/2 Digit Precision Pr;Ceramic DIP	Z41-3	DL66	INL
107	ICL8052ACPD/7103ACPI	41	9L	2.4	.40%	15	15	500mØ	0	70	4 1/2 Digit Precision Pr;Plastic DIP	Z41-3	DL65	INL

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ∅-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1	ICL8052CDD/7101CDL	41	15L	2.4	.40%	15	15	500m∅	0	70	3 1/2 Digit A/D Pair;Ceramic DIP	Z41-2	DL64	INL
2	ICL8052CDD/7103CDI	41	9L	2.4	.40%	15	15	500m∅	0	70	3 1/2 Digit Precision Pr;Ceramic DIP	Z41-3	DL66	INL
3	ICL8052CPD/7101CPL	41	15L	2.4	.40%	15	15	500m∅	0	70	3 1/2 Digit A/D Pair;Plastic DIP	Z41-2	DL63	INL
4	ICL8052CPD/7103CPI	41	9L	2.4	.40%	15	15	500m∅	0	70	3 1/2 Digit Precision Pr;Plastic DIP	Z41-3	DL65	INL
5	MN2020	41	3	2.2	.80	0.0	15	300m	0	70	Precision Hybrid Amplifier			MNC
6	MN5500	41	12	2.0	.80	15	15	1.7	0	70	12 Bit ADC,Conversion Time 25us Max	Z41-5	DL115	MNC
7	MC14443AL	41	10	7.0	3.0	0.0	10	15m	55	125	6 Ch Analog to Digital Converters	Z41-4	DL6c	MOTA
8	MC14443CL	41	10	7.0	3.0	0.0	10	15m	40	85	6 Ch Analog to Digital Converters	Z41-4	DL6c	MOTA
9	MC14443CP	41	10	7.0	3.0	0.0	10	15m	40	85	6 Ch Analog to Digital Converters	Z41-4	DL53	MOTA
10	MC14447AL	41	10	7.0	3.0	0.0	10	15m	55	125	6 Ch Analog to Digital Converters	Z41-4	DL6c	MOTA
11	MC14447CL	41	10	7.0	3.0	0.0	10	15m	40	85	6 Ch Analog to Digital Converters	Z41-4	DL6c	MOTA
12	MC14447CP	41	10	7.0	3.0	0.0	10	15m	40	85	6 Ch Analog to Digital Converters	Z41-4	DL53	MOTA
13▼	CDP18S643	41	12			15	15		0	70	SH;Bipolar or Unipolar Voltage Input			RCA
14	MAS-839	43	12			15	15	2.4			Two 8 Channel Multiplexers;§	Z45-1		CLI
15	MUX1600	43	18	2.2	.80	0.0	12	96m	0	75	16 Ch Analog Multiplexer	Z43-2	DL36e	GIC
16#	MN1202	43	4	2.4	.80§	0.0	5.0		30	70	Quad 2 Line to 1 Line Multiplexer	Z43-5	DL165	MATJ
17	R29693DC	43	8	2.0	.80§	0.0	5.0	700m	0	75	Programmable Mux;Fusible Link Progm	Z43-3	DL∅	RTN
18	R29693DM	43	8	2.0	.80§	0.0	5.0	700m	55	125	Programmable Mux;Fusible Link Progm	Z43-3	DL∅	RTN
19	R29693FM	43	8	2.0	.80§	0.0	5.0	700m	55	125	Programmable Mux;Fusible Link Progm	Z43-3	FP∅	RTN
20	TIM9905J	43	8	2.0	.80§	0.0	5.0	63m	0	70	Data Sel/Mux W/3-State Out;Cer Pkg	Z43-4		TII
21	TIM9905N	43	8	2.0	.80§	0.0	5.0	63m	0	70	Data Sel/Mux W/3-State Out;Plas Pkg	Z43-4		TII
22	Am25LS138DM	44	8L	2.0	.70	0.0	5.0	50m	55	125	3 To 8 Line Decoder/Demultiplexer	Z44-3	DL87	AMV
23	Am25LS138FM	44	8L	2.0	.70	0.0	5.0	50m	55	125	3 To 8 Line Decoder/Demultiplexer	Z44-3	FP∅	AMV
24	Am25LS138PC	44		2.0	.80	0.0	5.0	50m	0	70	3 To 8 Line Decoder/Demultiplexer	Z44-3	DL4a	AMV
25	Am25LS138XC	44	8L	2.0	.80	0.0	5.0	50m	0	70	3 To 8 Line Decoder/Demultiplexer	Z44-3	CH∅	AMV
26	Am25LS138XM	44		2.0	.70	0.0	5.0	50m	55	125	3 To 8 Line Decoder/Demultiplexer	Z44-3	CH∅	AMV
27	HCMP1853CD	44	8L			0.0	5.0	500m	55	125	N Bit 1 of 8 Decoder	Z44-5		HAC
28	HCMP1853D	44	8L			0.0	10	500m	55	125	N Bit 1 of 8 Decoder	Z44-5		HAC
29	D8205	44	8	2.0	.85	0.0	5.0	350m	0	75	High Speed 1 Out of 8 Bin Decoder	Z44-1	DL6a	ITL
30	P8205	44	8	2.0	.85	0.0	5.0	350m	0	75	High Speed 1 Out of 8 Bin Decoder	Z44-1	DL33	ITL
31	CDP1853CD	44	8L	3.5	1.5	0.0	5.0	500u†	55	125	1 of 8 Decoder for I/O Expansion	Z44-5	Δ001AE	RCA
32	CDP1853CE	44	8L	3.5	1.5	0.0	5.0	500u†	40	85	1 of 8 Decoder for I/O Expansion	Z44-5	Δ001AE	RCA
33	CDP1853D	44	8L	7.0	3.0	0.0	10	1.0m†	55	125	1 of 8 Decoder for I/O Expansion	Z44-5	Δ001AE	RCA
34	CDP1853E	44	8L	3.5	1.5	0.0	5.0	500u†	40	85	1 of 8 Decoder for I/O Expansion	Z44-5	Δ001AE	RCA
35▼	MP32BG-CG	45	12			15	15	1.3	40	100	Data Acquisition;16 Single end Chan			BUB
36	DT3752	45	8			0.0	12	2.4	0	55	16 SE or 8 Diff Channels	Z45-3		DTI
37	DT3754	45	8			0.0	12	2.4	0	55	16 SE or 8 Diff Channels	Z45-3		DTI
38	DT3755	45	8			0.0	12	2.4	0	55	4 Differential Channels;Isolated	Z45-3		DTI
39▼#	HD46508P1A1	45	10	2.0	.80§	0.0	5.0	500m	20	75	Acquisition Data Analog Unit			HITJ
40▼#	HD46508P1A2	45	10	2.0	.80§	0.0	5.0	500m	20	75	Acquisition Data Analog Unit			HITJ
41▼#	HD46508P2A1	45	10	2.0	.80§	0.0	5.0	500m	20	75	Acquisition Data Analog Unit			HITJ
42▼#	HD46508P-A1	45	10	2.0	.80§	0.0	5.0	500m	20	75	Acquisition Data Analog Unit			HITJ
43	Am29LS18DC	55	4	2.0	.80	0.0	5.0	140m	0	70	Low Power Schottky Version of 2918DC	Z55-5	DL6s	AMV
44	Am29LS18DM	55	4	2.0	.70	0.0	5.0	140m	55	125	Low Power Schottky Version of 2918DM	Z55-5	DL6s	AMV
45	Am29LS18FM	55	4	2.0	.70	0.0	5.0	140m	55	125	Low-Power Version of 2918FM	Z55-5	FP9	AMV
46	Am29LS18PC	55	4	2.0	.80	0.0	5.0	140m	0	70	Low Power Schottky Version of 2918PC	Z55-5	DL6r	AMV
47	Am2918DC	55	4	2.0	.80§	0.0	5.0	600m	0	70	D Regist W/Standard and 3 State Out	Z55-5	DL6e	AMV
48	Am2918DM	55	4	2.0	.80§	0.0	5.0	600m	55	125	D Regist W/Standard and 3 State Out	Z55-5	DL6e	AMV
49	Am2918FM	55	4	2.0	.80§	0.0	5.0	600m	55	125	D Regist W/Standard and 3 State Out	Z55-5	FP1a	AMV
50	Am2918PC	55	4	2.0	.80§	0.0	5.0	600m	0	70	D Regist W/Standard and 3 State Out	Z55-5	DL33c	AMV
51	Am2919DC	55	4	2.0	.80	0.0	5.0	195	0	70	Quad Register;MAX Clock Freq 30 MHZ	Z55-19	DL60b	AMV
52	Am2919DM	55	4	2.0	.80	0.0	5.0	180m	0	70	Quad Register;MAX Clock Freq 25 MHZ	Z55-19	DL60b	AMV
53	Am2919FM	55	4	2.0	.70	0.0	5.0	180m	55	125	Quad Register;Max Clock Freq 25MHz	Z55-19	FP20	AMV
54	Am2919PC	55	4	2.0	.80	0.0	5.0	195	0	70	Quad Register;MAX Clock Freq 30 MHZ	Z55-19	DL60a	AMV
55	9403ADC	55	64	2.0	.80§	0.0	5.0	850m	0	75		Z55-2	DL7g	FSC
56	9403ADM	55	64	2.0	.70§	0.0	5.0	850m	55	125		Z55-2	DL7g	FSC
57	9403APC	55	64	2.0	.80§	0.0	5.0	850m	0	75		Z55-2	DL7g	FSC
58	9407DC	55		2.0	.80§	0.0	5.0	725m	0	75	Data Access Register, 3 Register	Z55-17	DL154	FSC
59	9407DM	55		2.0	.70§	0.0	5.0	725m	55	125	Data Access Register, 3 Register	Z55-17	DL154	FSC
60	9407PC	55		2.0	.80§	0.0	5.0	725m	0	75	Data Access Register, 3 Register	Z55-17	DL155	FSC
61	9423DC	55	4	2.0	.80§	0.0	5.0	750m	0	75	16x4 Bit Async FIFO Mem	Z55-2	DL7g	FSC
62	9423DM	55	4	2.0	.70§	0.0	5.0	750m	55	125	16x4 Bit Async FIFO Mem	Z55-2	DL7g	FSC
63	9423PC	55	4	2.0	.80§	0.0	5.0	750m	0	75	16x4 Bit Async FIFO Mem	Z55-2	DL18d	FSC
64	C4003	55	10	3.5	.80	10	5.0	127m	0	70	Outp Expander,S/P Shift Register	Z55-4	DL39	ITL
65	D4003	55	10	3.5	.80	10	5.0	127m	0	70	Outp Expander,S/P Shift Register	Z55-4	DL6a	ITL
66	P4003	55	10	3.5	.80	10	5.0	127m	0	70	Outp Expander,S/P Shift Register	Z55-4	DL33	ITL
67	29LS18FM	55	4	2.0	.70§	0.0	5.0	140m	55	125	Low Power Schottky Version of 2918FM	Z55-5	FP1c	MMI
68	29LS18JC	55	4	2.0	.80§	0.0	5.0	140m	0	70	Low Power Schottky Version of 2918JC	Z55-5	DL6p	MMI
69	29LS18JM	55	4	2.0	.70§	0.0	5.0	140m	55	125	Low Power Schottky Version of 2918JM	Z55-5	DL6p	MMI
70	29LS18NC	55	4	2.0	.80§	0.0	5.0	140m	0	70	Low Power Schottky Version of 2918NC	Z55-5	DL93	MMI
71	MMI57LS315J	55	8	2.0	.80	0.0	5.0		55	125	Octal Register with I/O	Z55-15	DL107	MMI
72	MMI57S374J	55	8	2.0	.80§	0.0	5.0	700m	55	125	Octal Register;Iol 32mA	Z55-7	DL107	MMI
73	MMI57S376J	55	8	2.0	.80§	0.0	5.0	700m	55	125	Octal Register With Inverting Output	Z55-8	DL107	MMI
74	MMI57S378J	55	8	2.0	.80§	0.0	5.0	700m	55	125	Octal Register W/Inv OP,Iol 32mA	Z55-8	DL107	MMI
75	MMI67LS315J	55	8	2.0	.80	0.0	5.0		0	70	Octal Register with I/O	Z55-15	DL107	MMI
76	MMI67LS315N	55	8	2.0	.80	0.0	5.0		0	70	Octal Register with I/O	Z55-15	DL108	MMI
77	MMI67S374J	55	8	2.0	.80§	0.0	5.0	700m	0	70	Octal Register:Iol 32mA	Z55-7	DL107	MMI
78	MMI67S374N	55	8	2.0	.80§	0.0	5.0	700m	0	70	Octal Register:Iol 32mA	Z55-7	DL108	MMI
79	MMI67S376J	55	8	2.0	.80§	0.0	5.0	700m	0	70	Octal Register With Inverting Output	Z55-8	DL107	MMI
80	MMI67S376N	55	8	2.0	.80§	0.0	5.0	700m	0	70	Octal Register With Inverting Output	Z55-8	DL108	MMI
81	MMI67S378J	55	8	2.0	.80§	0.0	5.0	700m	0	70	Octal Register W/Inv OP,Iol 32mA	Z55-8	DL107	MMI
82	MMI67S378N	55	8	2.0	.80§	0.0	5.0	700m	0	70	Octal Register W/Inv OP,Iol 32mA	Z55-8	DL108	MMI
83	MMI57401J	55	4	2.0	.80	0.0	5.0	750m	55	125	64x4 FIFO Mem,15MHz Shift	Z55-9	DL6p	MMI
84	MMI67401J	55	4	2.0	.80	0.0	5.0	750m	0	70	64x4 FIFO Mem,15MHz Shift	Z55-9	DL6p	MMI
85	MC2918FM	55	4	2.0	.80§	0.0	5.0	650m	55	125	Quad D Register,Clock Freq 75MHz	Z55-5	FP10	MOTA
86	MC2918LC	55	4	2.0	.80§	0.0	5.0	650m	0	70	Quad D Register,Clock Freq 75MHz	Z55-5	DL76	MOTA
87	MC2918LM	55	4	2.0	.80§	0.0	5.0	650m	55	125	Quad D Register,Clock Freq 75MHz	Z55-5	DL76	MOTA
88	MC2918PC	55	4	2.0	.80§	0.0	5.0	650m	0	70	Quad D Register,Clock Freq 75MHz	Z55-5	DL53	MOTA
89	MC29100LC	55		2.0	.80§	0.0	5.0	600m†	0	70	FPLA,In 16,Out 8,Product 48	Z55-14	DL∅	MOTA
90	MC29100LM	55		2.0	.80§	0.0	5.0	600m†	55	125	FPLA,In 16,Out 8,Product 48	Z55-14	DL∅	MOTA
91	MC29101LC	55		2.0	.80	0.0	5.0	600m†	0	70	FPLA,In 16,Out 8,Product 48	Z55-14	DL∅	MOTA
92	MC29101LM	55		2.0	.80	0.0	5.0	600m†	55	125	FPLA,In 16,Out 8,Product 48	Z55-14	DL∅	MOTA
93	IDM29705AJM	55	4	2.0	0.8	0	5.0	725m	55	125	Hi-Speed IDM29705JM/883	Z55-21	DL	NSC
94♦	IDM29705JC	55	4	2.0	0.8	0	5.0	725m	0	70	16x4 Two Port Register File	Z55-21	DL67	NSC
95♦	IDM29705JM	55	4	2.0	0.8	0	5.0	725m	55	125	16x4 Two Port Register File Z5	Z55-21	DL67	NSC
96♦	IDM29705JM/883	55	4	2.0	0.8	0	5.0	725m	55	125	IDM29705JM w/Compliance to MIL-STD	Z55-21	DL67	NSC
97	IDM29901JC	55	8	2.0	.80§	0.0	5.0	225m	0	70	Octal Register;For Temporary Storage	Z55-10	DL110	NSC
98	IDM29901JM	55	8	2.0	.70§	0.0	5.0	225m	55	125	Octal Register;For Temporary Storage	Z55-10	DL110	NSC
99	IDM29901NC	55	8	2.0	.80§	0.0	5.0	225m	0	70	Octal Register;For Temporary Storage	Z55-10	DL109	NSC
100	MM57126	55	1LS	8.3	5.5	9.5	0.0	180m	0	70	16x64 Bit Shift Register	Z55-6	DL94	NSC
101	A07	55	8	3.5	-12	12	5.0	200m	0	70	116x4 Bit RAM,1024x8 Bit ROM	Z55-12	DL∅	RKW
102	A08	55	8	3.5	-12	12	5.0	200m	0	70	76x4 Bit RAM,704x8 Bit ROM	Z55-12a	DL∅	RKW
103	A20	55	8	3.5	-12	12	5.0	500m	0	70	128x4 Bit RAM,1536x8 Bit ROM	Z55-13	DL∅	RKW
104#	M3856B1	55	16	2.9	.80	0.0	12.0	1.1	0	70	Prog/Data Storage;Prog/Data Counters	Z93	DL184	SGAI
105#	M3856D1	55	16	2.9	.80	0.0	12.0	1.1	0	70	Prog/Data Storage;Prog/Data Counters	Z93	DL185	SGAI
106	SN74S225J	55	80	2.0	.80§	0.0	5.0	600m	0	70	16Wx5 Bit Async FIFO Mem	Z55-1	DL16	TII

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ∅-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	2 MFR. CODE
1	SN74S225N	55	80	2.0	.80§	0.0	5.0	600m	0	70	16Wx5 Bit Async FIFO Mem	Z55-1	DL17	TII
2	FR1502E	55	9	3.5	.80	12	5.0		0	70	FIFO Buffer Register,DC to 1MHz	Z55-18	DL162	WDC
3	FR1502F	55	9	3.5	.80	12	5.0		0	70	FIFO Buffer Register,DC to 1MHz	Z55-18	DL163	WDC
4	HCMP1858CD	56	4			0.0	5.0	500m	55	125	4 Bit Latch With Decode	Z56-7		HAC
5	HCMP1858D	56	4			0.0	10	500m	55	125	4 Bit Latch With Decode	Z56-7		HAC
6	HCMP1859CD	56	4			0.0	5.0	500m	55	125	4 Bit Latch With Decode	Z56-8		HAC
7	HCMP1859D	56	4			0.0	10	500m	55	125	4 Bit Latch With Decode	Z56-8		HAC
8#	MN1201	56	4	2.4	.80	0.0	5.0		30	70	Dual 4 Bit Data Latch	Z56-13	DL165	MATJ
9#	MN1201A	56	4	2.4	.80	0.0	5.0		30	70	Dual 4 Bit Data Latch	Z56-14	DL164	MATJ
10	MMI57S373J	56	8	2.0	.80§	0.0	5.0	800m	55	125	Octal Latch;Iol 32mA	Z56-9	DL107	MMI
11	MMI57S380J	56	8	2.0	.80§	0.0	5.0	800m	55	125	Octal Latch W/Inverting Output	Z56-10	DL107	MMI
12	MMI57S382J	56	8	2.0	.80§	0.0	5.0	800m	55	125	Octal Latch W/Inv Op,Iol 32mA	Z56-10	DL107	MMI
13	MMI67S373J	56	8	2.0	.80§	0.0	5.0	800m	0	70	Octal Latch;Iol 32mA	Z56-9	DL107	MMI
14	MMI67S373N	56	8	2.0	.80§	0.0	5.0	800m	0	70	Octal Latch;Iol 32mA	Z56-9	DL108	MMI
15	MMI67S380J	56	8	2.0	.80§	0.0	5.0	800m	0	70	Octal Latch W/Inverting Output	Z56-10	DL107	MMI
16	MMI67S380N	56	8	2.0	.80§	0.0	5.0	800m	0	70	Octal Latch W/Inverting Output	Z56-10	DL108	MMI
17	MMI67S382J	56	8	2.0	.80§	0.0	5.0	800m	0	70	Octal Latch W/Inv OP,Iol 32mA	Z56-10	DL107	MMI
18	MMI67S382N	56	8	2.0	.80§	0.0	5.0	800m	0	70	Octal Latch W/Inv OP,Iol 32mA	Z56-10	DL108	MMI
19	MC14099BAL	56	8	11	4.0	0.0	15		55	125	Addressable Latch;Unidirectional	Z56-5	DL76	MOTA
20	MC14099BCL	56	8	11	4.0	0.0	15		40	85	Addressable Latch;Unidirectional	Z56-5	DL76	MOTA
21	MC14099BCP	56	8	11	4.0	0.0	15		40	85	Addressable Latch;Unidirectional	Z56-5	DL53	MOTA
22	MC14599BAL	56	8	11	4.0	0.0	15		55	125	Addressable Latch;Bidirectional Port	Z56-6	DL91	MOTA
23	MC14599BCL	56	8	11	4.0	0.0	15		40	85	Addressable Latch;Bidirectional Port	Z56-6	DL91	MOTA
24	MC14599BCP	56	8	11	4.0	0.0	15		40	85	Addressable Latch;Bidirectional Port	Z56-6	DL90	MOTA
25	uPD754C	56	8	3.0	.90§	5.0	12	470m	10	70	8 Bit Latch;Tpd 100ns max	Z56-4	DL18b	NECM
26	uPD754D	56	8	3.0	.90§	5.0	12	470m	10	70	8 Bit Latch;Tpd 100ns max	Z56-4	DL45a	NECM
27	CDP1858CD	56	4	3.5	1.5	0.0	5.0	500ut	55	125	4-Bit Latch W/Dual 1 of 4 Decoders	Z56-8	Δ001AE	RCA
28	CDP1858CE	56	4	3.5	1.5	0.0	5.0	2.5m♦	40	85	4-Bit Latch With Decoder	Z56-8	Δ001AC	RCA
29	CDP1858D	56	4	7.0	3.0	0.0	10	1.0mt	55	125	4-Bit Latch W/Dual 1 of 4 Decoders	Z56-8	Δ001AE	RCA
30	CDP1858E	56	4	7.0	3.0	0.0	10	5.0m♦	40	85	4-Bit Latch With Decoder	Z56-8	Δ001AC	RCA
31	CDP1859CD	56	4	3.5	1.5	0.0	5.0	500m	55	125	4-Bit Latch W/Single 1 of 4 Decoder	Z56-7	Δ001AE	RCA
32	CDP1859CE	56	4	3.5	1.5	0.0	5.0	2.5m♦	40	85	4-Bit Latch With Decoder	Z56-7	Δ001AC	RCA
33	CDP1859D	56	4	7.0	3.0	0.0	10	500m	55	125	4-Bit Latch W/Single 1 of 4 Decoder	Z56-7	Δ001AE	RCA
34	CDP1859E	56	4	7.0	3.0	0.0	10	5.0m♦	40	85	4-Bit Latch With Decoder	Z56-7	Δ001AC	RCA
35	CDP1866CD	56	4	3.5	1.5	0.0	6.5	500m	55	125	Latch/Decoder Mem Interface		DL25	RCA
36	CDP1866CE	56	4	3.5	1.5	0.0	6.5	500m	40	85	Latch/Decoder Mem Interface		DL119	RCA
37	CDP1866D	56	4	3.5	1.5	0.0	10.5	500m	55	125	Latch/Decoder Mem Interface		DL25	RCA
38	CDP1866E	56	4	3.5	1.5	0.0	10.5	500m	40	85	Latch/Decoder Mem Interface		DL119	RCA
39	CDP1867CD	56	4	3.5	1.5	0.0	6.5	500m	55	125	Latch/Decoder Mem Interface		DL25	RCA
40	CDP1867CE	56	4	3.5	1.5	0.0	6.5	500m	40	85	Latch/Decoder Mem Interface		DL119	RCA
41	CDP1867D	56	4	3.5	1.5	0.0	10.5	500m	55	125	Latch/Decoder Mem Interface		DL25	RCA
42	CDP1867E	56	4	3.5	1.5	0.0	10.5	500m	40	85	Latch/Decoder Mem Interface		DL119	RCA
43	CDP1868CD	56	4	3.5	1.5	0.0	6.5	500m	55	125	Latch/Decoder Mem Interface		DL25	RCA
44	CDP1868CE	56	4	3.5	1.5	0.0	10.5	500m	40	85	Latch/Decoder Mem Interface		DL119	RCA
45	CDP1868D	56	4	3.5	1.5	0.0	6.5	500m	55	125	Latch/Decoder Mem Interface		DL25	RCA
46	CDP1868E	56	4	3.5	1.5	0.0	10.5	500m	40	85	Latch/Decoder Mem Interface		DL119	RCA
47	SN54S373J	56	8	2.0	.80§	0.0	5.0	800m	55	125	Octal D-Type Latches	Z56-1	DL16	TII
48	SN54S412J	56	8	2.0	.85§	0.0	5.0	410m	55	125	Multi-Mode Buffered Latches	Z56-3	Δ015AA	TII
49	SN74S373J	56	8	2.0	.80§	0.0	5.0	800m	0	70	Octal D-Type Latches	Z56-1	DL16	TII
50	SN74S373N	56	8	2.0	.80§	0.0	5.0	800m	0	70	Octal D-Type Latches	Z56-1	DL17	TII
51	SN74S412J	56	8	2.0	.85§	0.0	5.0	650m	0	70	Multi-Mode Buffered Latches	Z56-3	Δ015AA	TII
52	SN74S412N	56	8	2.0	.85§	0.0	5.0	650m	0	70	Multi-Mode Buffered Latches	Z56-3	DL14b	TII
53	TIM9906J	56	8	2.0	.80	0.0	5.0	189m	0	70	8-Bit Addressable Latch;Cer Pkg	Z56-12		TII
54	TIM9906N	56	8	2.0	.80	0.0	5.0	189m	0	70	8-Bit Addressable Latch;Plas Pkg	Z56-12		TII
55	S6846	57	8	2.0	.80	0.0	5.0	1.0	0	70	Combination ROM-I/O-Timer	Z57-8	DL1n	AMI
56	MMD-1MI	57	8			12	12	9.2			Memory Interface Board	Z57-6		E/L
57	F3851	57	16	2.9	.80§	0.0	12	275mt	0	70	Program Storage Unit for F8 System	Z57-21		FSC
58	F3857DL	57	16	2.9	.80§	0.0	12	1.1	40	85	2k PSU/Static Mem Interface/F8 Sys	Z57-23	DL160	FSC
59	F3857DM	57	16	2.9	.80§	0.0	12	1.1	55	125	2k PSU/Static Mem Interface/F8 Sys	Z57-23	DL160	FSC
60	F3857PC	57	16	2.9	.80§	0.0	12	1.1	0	70	2k PSU/Static Mem Interface/F8 Sys	Z57-23	DL86	FSC
61	F3857PL	57	16	2.9	.80§	0.0	12	1.1	40	85	2k PSU/Static Mem Interface/F8 Sys	Z57-23	DL86	FSC
62	F3857PM	57	16	2.9	.80§	0.0	12	1.1	55	125	2k PSU/Static Mem Interface/F8 Sys	Z57-23	DL86	FSC
63	F6846D	57	8	2.0	.80§	0.0	5.0	800m	0	70	Interface F6800/F6802;40 Pin Plastic	Z30-24	DL11i	FSC
64	C4001	57	8	3.5	.80	10	5.0	300m	0	70	256 x 8 ROM And 4 Bit I/O Port	Z57-2	DL39	ITL
65	C4002-1	57	4	3.5	.80	10	5.0	330m	0	70	320 Bit RAM And 4 Bit Output Port	Z57-4	DL39	ITL
66	C8155	57	8	2.0	.80	0.0	5.0	900m	0	70	400ns Access Time;2 Progm 8B IO Port	Z57-9a	DL37	ITL
67	C8155-2	57	8	2.0	.80	0.0	5.0	900m	0	70	330ns Access Time;2 Progm 8B IO Port	Z57-9a	DL37	ITL
68	C8156	57	8	2.0	.80	0.0	5.0	900m	0	70	400ns Access Time;2 Progm 8B IO Port	Z57-9	DL37	ITL
69	C8156-2	57	8	2.0	.80	0.0	5.0	900m	0	70	330ns Access Time;2 Progm 8B IO Port	Z57-9	DL37	ITL
70	C8355	57	8	2.0	.80	0.5	7.0	1.5 ∅	0	70	2Kx8-Bit ROM and Two 8-Bit I/O Ports	Z57-10	DL148	ITL
71	C8355-2	57	8	2.0	.80	0.5	7.0	1.5 ∅	0	70	2kx8-Bit ROM and Two 8-Bit I/O Ports	Z57-10	DL148	ITL
72	C8755	57	8	2.0	.80	0.0	5.0	900m	10	70	2kx8 EPROM And Two 8 Bit I/O Ports	Z57-11	DL70	ITL
73	C8755A-2	57	8	2.0	.80	0.5	7.0	1.5 ∅	0	70	2Kx8-Bit ROM and Two 8-Bit I/O Ports	Z57-11	DL70	ITL
74	D4001	57	8	3.5	.80	10	5.0	300m	0	70	256 x 8 ROM And 4 Bit I/O Port	Z57-2	DL6a	ITL
75	D4002-1	57	4	3.5	.80	10	5.0	330m	0	70	320 Bit RAM And 4 Bit Output Port	Z57-4	DL6a	ITL
76	D8155	57	8	2.0	.80	0.0	5.0	900m	0	70	400ns Access Time;2 Progm 8B IO Port	Z57-9a	DL38	ITL
77	D8155-2	57	8	2.0	.80	0.0	5.0	900m	0	70	330ns Access Time;2 Progm 8B IO Port	Z57-9a	DL38	ITL
78	D8156-2	57	8	2.0	.80	0.0	5.0	900m	0	70	330ns Access Time;2 Progm 8B IO Port	Z57-9	DL38	ITL
79	D8355	57	8	2.0	.80	0.0	5.0	900m	10	70	2kx8 ROM And Two 8 Bit I/O Ports	Z57-10	DL11e	ITL
80	D8755A	57	8	2.0	.80	0.5	7.0	1.5 ∅	0	70	2kx8-Bit ROM and Two 8-Bit I/O Ports	Z57-11	DL148	ITL
81	D8755A-2	57	8	2.0	.80	0.5	7.0	1.5 ∅	0	70	2kx8-Bit ROM and Two 8-Bit I/O Ports	Z57-11	DL148	ITL
82	P4001	57	8	3.5	.80	10	5.0	300m	0	70	256 x 8 ROM And 4 Bit I/O Port	Z57-2	DL33	ITL
83	P4002-1	57		3.5	.80	10	5.0	330m	0	70	320 Bit RAM And 4 Bit Output Port	Z57-4	DL33	ITL
84	P4308	57	8	3.5	.80	10	5.0	400m	0	70	1024 x 8 ROM With 4 I/O Ports	Z57-3	DL43	ITL
85	P8155	57	8	2.0	.80	0.0	5.0	900m	0	70	400ns Access Time;2 Progm 8B IO Port	Z57-9a	DL42f	ITL
86	P8155-2	57	8	2.0	.80	0.0	5.0	900m	0	70	330ns Access Time;2 Progm 8B IO Port	Z57-9a	DL42f	ITL
87	P8156	57	8	2.0	.80	0.0	5.0	900m	0	70	400ns Access Time;2 Progm 8B IO Port	Z57-9	DL42f	ITL
88	P8156-2	57	8	2.0	.80	0.0	5.0	900m	0	70	330ns Access Time;2 Progm 8B IO Port	Z57-9	DL42f	ITL
89	P8355	57	8	2.0	.80	0.0	5.0	900m	10	70	2kx8 ROM And Two 8 Bit I/O Ports	Z57-10	DL11d	ITL
90	P8755A	57	8	2.0	.80	0.5	7.0	1.5 ∅	0	70	2kx8-Bit ROM and Two 8-Bit I/O Ports	Z57-11	DL149	ITL
91	P8755A-2	57	8	2.0	.80	0.5	7.0	1.5 ∅	0	70	2kx8-Bit ROM and Two 8-Bit I/O Ports	Z57-11	DL149	ITL
92	MC6846L	57	8	2.0	.80	0.0	5.0	1.0	0	70	Combination ROM-Parallel I/O-Timer	Z57-8	DL1d	MOTA
93	MC6846P	57	8	2.0	.80	0.0	5.0	1.0	0	70	Combination ROM-Parallel I/O-Timer	Z57-8	DL27	MOTA
94	MCS6530	57	8	2.4	.40	0.0	5.0	1.0	0	70	1024x8 ROM,64x8 RAM,I/O Bus,Timer	Z57-1	DL26	MTY
95	MCS6532	57	8	2.4	.40	0.0	5.0	1.0	0	70	128x8 RAM Mem,I/O,Timer Array	Z57-12	DL26	MTY
96#	uPD8155C	57	8	2.0	.80	0.0	5.0		0	70	256x8 RAM And 2 Progm 8 Bit I/O Port	Z57-9	DL∅	NECJ
97#	uPD8156C	57	8	2.0	.80	0.0	5.0		0	70	256x8 RAM And 2 Progm 8 Bit I/O Port	Z57-9	DL∅	NECJ
98#	uPD8355C	57	8	2.0	.80	0.0	5.0				2kx8 ROM And Two 8 Bit I/O Ports	Z57-10	DL11c	NECJ
99#	uPD8355D	57	8	2.0	.80	0.0	5.0				2kx8 ROM And Two 8 Bit I/O Ports	Z57-10	DL∅	NECJ
100	A17	57	16	-12	3.5	12	5.0	400m	0	70	2048x8 ROM/128x4 RAM/IO	Z57-5	DL44	RKW
101	A21	57	8	3.5	-12	12	5.0	600mt	0	70	64x8 RAM,2048x8 ROM,2 IO Ports	Z57-15	DL∅	RKW
102	R6530	57	8	2.4	.40	0.0	5.0	1.0	0	70	1024x8 ROM,64x8 RAM,I/O Bus,Timer	Z57-1	DL26	RKW
103	R6531AQ	57	8	2.0	.80	0.0	5.0	1.0	0	70	2048x8 ROM,128x8 RAM,IO,2.0MHz	Z57-17a	DL139	RKW
104	R6531C	57	8	2.0	.80	0.0	5.0	1.0	0	70	2048x8 ROM,128x8 RAM,IO,1.0MHz	Z57-17	DL26	RKW
105	R6531CE	57	8	2.0	.80	0.0	5.0	1.0	40	85	2048x8 ROM,128x8 RAM,IO,1.0MHz	Z57-17	DL26	RKW
106	R6531P	57	8	2.0	.80	0.0	5.0	1.0	0	70	2048x8 ROM,128x8 RAM,IO,1.0MHz	Z57-17	DL26	RKW
107	R6531Q	57	8	2.0	.80	0.0	5.0	1.0	0	70	2048x8 ROM,128x8 RAM,IO,1.0MHz	Z57-17a	DL139	RKW
108	R6532	57	8	2.4	.40	0.0	5.0	1.0	0	70	128x8 RAM Mem,I/O Timer(RIOT)	Z57-12	DL26	RKW
109	R6534P	57	8	2.0	.80	0.0	5.0	1.0	0	70	4096x8 ROM,Counter,IO,1.0 MHz	Z57-18	DL26	RKW
110	R6534Q	57	8	2.0	.80	0.0	5.0	1.0	0	70	4096x8 ROM,Counter,IO,1.0 MHz	Z57-18a	DL139	RKW

SYMBOLS AND CODES EXPLAINED IN INTERPRETER

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	[3] TYPE No.	[1] TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE †-TYPICAL *-MIN ☑-ABS.MAX. %-OUTPUT DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE Δ=MO	[2] MFR. CODE
1	N2656I	57	8	2.2	.80	0.0	5.0	750m	0	70	System Memory Interface	Z57-13	DL1b	SIC
2	SY6530	57	8	2.4	.40	0.0	5.0	1.0	0	70	1024x8 ROM,64x8 RAM,I/O Bus,Timer	Z57-1	DL26	SYK
3	SY6531	57	8	2.0	.80	0.0	5.0	500m	0	70	RAM,ROM,2IO Ports,tACR 395ns Max	Z57-16	DL☑	SYK
4	SY6531A	57	8	2.0	.80	0.0	5.0	500m	0	70	RAM,ROM,2IO Ports,tACR 200ns Max	Z57-16	DL☑	SYK
5	SY6532	57	8	2.4	.40	0.0	5.0	1.0	0	70	128x8 RAM Mem,I/O,Timer Array	Z57-12	DL26	SYK
6	SBP9960CJ	57	16P	2.0	.80	0.0	5.0	423m	0	70	I/O Expander	Z57-20		TII
7	SBP9960EJ	57	16P	2.0	.80	0.0	5.0	423m	40	85	I/O Expander	Z57-20		TII
8	SBP9960MJ	57	16P	2.0	.80	0.0	5.0	423m	55	125	I/O Expander	Z57-20		TII
9▼#	TMP8355P	57	8	2.0	.80	0.0	5.0	1.5	0	70	8-Bit ROM w/I/O Ports	Z57-10	DL208	TOSJ
10▼	Am9511A-1DM	90	8	2.0	.80	0.0	12	2.0 ☑	55	125	Arithmetic Processor	Z90-6	DL9c	AMD
11▼	Am9511ADC	90	8	2.0	.80	0.0	12	2.0 ☑	0	70	Arithmetic Processor	Z90-6	DL9c	AMD
12▼	Am9511ADM	90	8	2.0	.80	0.0	12	2.0 ☑	55	125	Arithmetic Processor	Z90-6	DL9c	AMD
13▼	Am9512-1DC	90	8	2.0	.80	0.0	12	2.0 ☑	0	70	3.0MHz Max Clock Frequency		DL9c	AMD
14▼	Am9512-1DM	90	8	2.0	.80	0.0	12	2.0 ☑	55	125	3.0MHz Max Clock Frequency		DL9c	AMD
15▼	Am9512DC	90	8	2.0	.80	0.0	12	2.0 ☑	0	70	2.0MHz Max Clock Frequency		DL9c	AMD
16▼	Am9512DM	90	8	2.0	.80	0.0	12	2.0 ☑	55	125	2.0MHz Max Clock Frequency		DL9c	AMD
17▼	S2811	90	12	2.0	.80	0.0	5.0	1.0	0	70	Sig Process Peri;(Prog);Avial Cer	Z90-8	DL159	AMI
18	Am2902DC	90	4	2.0	.80	0.0	5.0	470m	0	70	Look Ahead Carry Generator	Z90-3	DL6e	AMV
19	Am2902DM	90	4	2.0	.80	0.0	5.0	495m	55	125	Look Ahead Carry Generator	Z90-3	DL6e	AMV
20	Am2902FM	90	4	2.0	.80	0.0	5.0	495m	55	125	Look Ahead Carry Generator	Z90-3	FP1a	AMV
21	Am2902PC	90	4	2.0	.80	0.0	5.0	470m	0	70	Look Ahead Carry Generator	Z90-3	DL33c	AMV
22	HCMP1855CD,P	90	8	3.5	1.5	0.0	5.0		55	125	8x8 Mulitply/Divide Chip			HAC
23	HCMP1855D,P	90	8	7.0	3.0	0.0	12		55	125	8x8 Multiply/DivideChip			HAC
24	C3003	90	8	2.0	.80	0.0	5.0	650m	0	70	Look Ahead Carry Generator	Z90-2	DL36	ITL
25	C8231	90	8	2.0	.80	0.0	5.0	1.5 ☑	0	70	Fixed/Float Single/Double Precision	Z90-6	DL210	ITL
26	C8232	90	8	2.0	.80	0.0	5.0	1.5 ☑	0	70	Floating Point;Single/Double Prec	Z90-7	DL210	ITL
27	D3003	90	8	2.0	.80	0.0	5.0	650m	0	70	Look Ahead Carry Generator	Z90-2	DL35	ITL
28	D8231	90	8	2.0	.80	0.0	5.0	1.5 ☑	0	70	Fixed/Float Single/Double Precision	Z90-6	DL7h	ITL
29	D8232	90	8	2.0	.80	0.0	5.0	1.5 ☑	0	70	Floating Point;Single/Double Prec	Z90-7	DL7h	ITL
30	MC3003	90	8	2.0	.80	0.0	5.0	650m	55	125	Look Ahead Carry Generator	Z90-2	DL36	ITL
31	P8231	90	8	2.0	.80	0.0	5.0	1.5 ☑	0	70	Fixed/Float Single/Double Precision	Z90-6	DL14c	ITL
32	P8232	90	8	2.0	.80	0.0	5.0	1.5 ☑	0	70	Floating Point;Single/Double Prec	Z90-7	D14c	ITL
33	MMI57558-1D	90	8	2.0	.80§	0.0	5.0	1.4	55	125	8x8 Multiplier; Speed 135ns max	Z90-4	DL42h	MMI
34	MMI57558-1F	90	8	2.0	.80§	0.0	5.0	1.4	55	125	8x8 Multiplier; Speed 135ns max	Z90-4a	FP4	MMI
35	MMI57558D	90	8	2.0	.80§	0.0	5.0	1.4	55	125	8x8 Multiplier,Speed 100ns typ	Z90-4	DL42h	MMI
36	MMI57558F	90	8	2.0	.80§	0.0	5.0	1.4	55	125	8x8 Multiplier; Speed 155ns max	Z90-4a	FP4	MMI
37	MMI67558-1D	90	8	2.0	.80§	0.0	5.0	1.4	0	70	8x8 Multiplier; Speed 125ns max	Z90-4	DL42h	MMI
38	MMI67558D	90	8	2.0	.80§	0.0	5.0	1.4	0	70	8x8 Multiplier,Speed 100ns typ	Z90-4	DL42h	MMI
39	MC2902FM	90	4	2.0	.80§	0.0	5.0	495m	55	125	Look Ahead Carry Generator	Z90-3	FP10	MOTA
40	MC2902LC	90	4	2.0	.80§	0.0	5.0	470m	0	70	Look Ahead Carry Generator	Z90-3	DL6l	MOTA
41	MC2902LM	90	4	2.0	.80§	0.0	5.0	495m	55	125	Look Ahead Carry Generator	Z90-3	DL6l	MOTA
42	MC2902PC	90	4	2.0	.80§	0.0	5.0	470m	0	70	Look Ahead Carry Generator	Z90-3	DL53	MOTA
43	MC10808	90	16	-1.1	-1.4	5.2	0.0	1.8	30	85	Programmable Multi-Bit Shifter	Z90-5	DL55	MOTA
44#	N74S182N	90	4	2.0	.80	0.0	5.0	545m	0	70	Look Ahead Carry Generator	Z90-1	DL4	PHIN
45	CDP1855CD	90	8	3.5	1.5	0.0	5.0	500m	55	125	Progr;Multiply/Divide Unit	Z20-54	DL1f	RCA
46	CDP1855CE	90	8	3.5	1.5	0.0	5.0	500m	40	85	Progr;Multiply/Divide Unit	Z20-54	DL1f	RCA
47	CDP1855D	90	8	3.5	1.5	0.0	5.0	500m	55	125	Progr;Multiply/Divide Unit	Z20-54	DL1f	RCA
48	CDP1855E	90	8	3.5	1.5	0.0	5.0	500m	40	85	Progr;Multiply/Divide Unit	Z20-54	DL1f	RCA
49	N74S182B	90	4	2.0	.80	0.0	5.0	545m	0	70	Look Ahead Carry Generator	Z90-1	DL4	SIC
50	N74S182F	90	4	2.0	.80	0.0	5.0	545m	0	70	Look Ahead Carry Generator	Z90-1	DL6	SIC
51	N74S182W	90	4	2.0	.80	0.0	5.0	545m	0	70	Look Ahead Carry Generator	Z90-1	FP1	SIC
52	S54S182B	90	4	2.0	.80	0.0	5.0	495m	55	125	Look Ahead Carry Generator	Z90-1	DL4	SIC
53	S54S182F	90	4	2.0	.80	0.0	5.0	495m	55	125	Look Ahead Carry Generator	Z90-1	DL6	SIC
54	S54S182W	90	4	2.0	.80	0.0	5.0	495m	55	125	Look Ahead Carry Generator	Z90-1	FP1	SIC
55	MPS7600-001	91	4G	-1.0	-2.5	8.0	0.0		0	70	Vid Game;Tennis,Hockey,H Ball,Target	Z91-1	DL36c	MTY
56	MPS7600-002	91	3G	-1.0	-2.5	8.0	0.0		0	70	VGA:525L,Target,Tennis,Race Car	Z91-1	DL36c	MTY
57	MPS7600-004	91	2G	-1.0	-2.5	8.0	0.0		0	70	VGA:525L,Target,Pinball	Z91-1	DL36c	MTY
58	MPS7600-005	91	3G	-1.0	-2.5	8.0	0.0		0	70	VGA:525L,Sea Battl,Tar,Catch/Reshoot	Z91-1	DL36c	MTY
59	MPS7601-001	91	4G	-1.0	-2.5	8.0	0.0		0	70	VGA:625L,Tenn,Target,Hock,Handball	Z91-1	DL36c	MTY
60	MPS7601-002	91	3G	-1.0	-2.5	8.0	0.0		0	70	VGA:625L,Tenn,Target,Race Car	Z91-1	DL36c	MTY
61	MPS7601-004	91	2G	-1.0	-2.5	8.0	0.0		0	70	VGA:625L,Target,Pinball	Z91-1	DL36c	MTY
62	MPS7601-005	91	3G	-1.0	-2.5	8.0	0.0		0	70	VGA:625L,Target,Submarine,C/Reshoot	Z91-1	DL36c	MTY
63#	2636I	91		2.2	.80	0.0	5.0	800m	0	55	Provides All Common Game Circuits	Z91-2	DL☑	PHIN
64▼	S2814	92				0.0	5.0	500m	0	70	Fast Fourier XFMR;32 Point BloZ92-18	DL159	AMI	AMI
65▼#	EF68A40C	92	16	2.0	.80	0.0	5.0	550m	0	70	Program Timer Module;Timer 6.0MHz		DL67c	EFCF
66▼#	EF68A40CV	92	16	2.0	.80	0.0	5.0	550m	40	85	Program Timer Module;Timer 6.0MHz		DL67c	EFCF
67▼#	EF68A40P	92	16	2.0	.80	0.0	5.0	550m	0	70	Program Timer Module;Timer 6.0MHz		DL134	EFCF
68▼#	EF68A40PV	92	16	2.0	.80	0.0	5.0	550m	40	85	Program Timer Module;Timer 6.0MHz		DL134	EFCF
69▼#	EF68B40C	92	16	2.0	.80	0.0	5.0	550m	0	70	Program Timer Module;Timer 8.0MHz		DL67c	EFCF
70▼#	EF68B40P	92	16	2.0	.80	0.0	5.0	550m	0	70	Program Timer Module;Timer 8.0MHz		DL134	EFCF
71▼#	EF6840C	92	16	2.0	.80	0.0	5.0	550m	0	70	Program Timer Module;Timer 4.0MHz		DL67c	EFCF
72▼#	EF6840CV	92	16	2.0	.80	0.0	5.0	550m	40	85	Program Timer Module;Timer 4.0MHz		DL67c	EFCF
73▼#	EF6840P	92	16	2.0	.80	0.0	5.0	550m	0	70	Program Timer Module;Timer 4.0MHz		DL134	EFCF
74▼#	EF6840PV	92	16	2.0	.80	0.0	5.0	550m	40	85	Program Timer Module;Timer 4.0MHz		DL134	EFCF
75▼#	uPD1510C	92	12	2.0	.80	0.0	5.0		10	70	ALU;RAM/ROM/I/O/		DL59	NECJ
76▼#	uPD1511C	92	12	2.0	.80	0.0	5.0		10	70	ALU;RAM/ROM/I/O		DL59	NECJ
77▼#	uPD1514C	92	12	2.0	.80	0.0	5.0		10	70	ALU;RAM/ROM/I/O		DL69	NECJ
78▼#	uPD1519B	92	12	2.0	.80	0.0	5.0		10	70	ALU;RAM/ROM/I/O		DL173	NECJ
79	uPD556B	92	4	0.0	-10	10	0.0	500m	10	70	Evaluation Chip for uCOM-43/44/45	Z92-9	DL173	NECM
80	7502	92				0.0	5.0	2.0			Relay Output Card	Z92-10		PRO
81	7503	92				0.0	5.0				Optoisolated AC Input Card;VBR 1500V	Z92-11		PRO
82	7604	92				0.0	5.0	3.5			TTL I/O Card;User Select Port Addr	Z92-12		PRO
83	CDP1863CD	92	8	3.5	1.5	0.5	6.0	500m	55	125	Progr Freq Generator	Z92-17	Δ001AC	RCA
84	CDP1863CE	92	8	3.5	1.5	0.5	6.0	500m	40	85	Progr Freq Generator	Z92-17	Δ001AC	RCA
85	CDP1863D	92	8	3.5	1.5	0.5	10	500m	55	125	Progr Freq Generator	Z92-17	Δ001AC	RCA
86	CDP1863E	92	8	3.5	1.5	0.5	10	500m	40	85	Progr Freq Generator	Z92-17	Δ001AC	RCA
87	2637I	92	8	2.2	.80§	0.5	7.0	800m	0	55	Universal Video Interface Ceramic	Z92-16		SIC
88	2637N	92	8	2.2	.80§	0.5	7.0	800m	0	55	Universal Video Interface Plastic	Z92-16		SIC
89	CCC3500	92		3.5	.80	12	5.0	476m	0	70	Cassette/Cartridge Data Handler	Z92-14	DL☑	SMC
90	CG4103	92	7	12.5	3.0	-14	14	400m	25	85	Char Gene;Static;Single Mask	Z92-15	DL☑	SMC
91	CRT7004A	92		2.0	080	0.0	5.0	500m	0	70	Char Gene;Access Time 400ns;Cursor	Z92-13	DL☑	SMC
92	CRT7004B	92		2.0	080	0.0	5.0	500m	0	70	Char Gene;Access Time 400ns;Cursor	Z92-13	DL☑	SMC
93	CRT7004C	92		2.0	080	0.0	5.0	500m	0	70	Char Gene;Access Time 400ns;Cursor	Z92-13	DL☑	SMC
94▼	CRT9006-83	92	8			0.0	5.0				Single Row Buffer;83 Char		DL9b	SMC
95▼	CRT9006-135	92	8			0.0	5.0				Single Row Buffer;135 Char		DL9b	SMC
96▼	Z-FIOCS	92	7			0.0	5.0				FIFO In/Output Interface Unit		DL190	ZIL
97▼	Z-FIOPS	92	7			0.0	5.0				FIFO In/Output Interface Unit		DL189	ZIL

IN TYPE NUMBER SEQUENCE

TYPE No.	MFRS	MIL-M-38510/
M38510/40001BQC	MOTA	400 ☑ AMEND 1 USAF
M38510/40001CQC	MOTA	400 ☑ AMEND 1 USAF
M38510/42001BQB	ITL	420 AMEND 1 USAF
M38510/42001CQB	ITL	420 AMEND

MILITARY DOCUMENTS

Department of Defense Index of Specifications and Standards

Device Manufacturers Qualifications on Test Reference Letter.

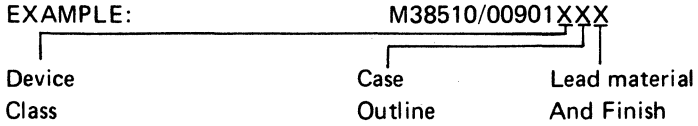
MIL–M–38510D Military Specification, General Specification for Microcircuits, dated 31 August August 1977, Amendment 1 dated 21 July 1978; Supplement 1B, dated 31 October 1978.

QPL–38510–44 Qualified Products List (Part 1) of Products Qualified Under Military Specification MIL–M–38510, dated 27 June 1980. Qualified Products List (Part II) of Products Qualified Under Military Specification MIL–M–38510, dated 27 June 1980. These products are considered qualified products. Therefore, manufacturers listed on QPL-38510 shall "JAN" mark and ship the specific part-numbered devices for which they are listed, providing all required quality conformance inspections have been successfully completed. They have not been subjected to all the tests required for qualification under the latest effective issue of MIL–M–38510; however, the manufacturers have performed sufficient similar tests to indicate that the products have the potential of complying with the MIL–M–38510 requirements.

MIL–STD–833B Military Standard; Test Methods and Procedures for Microelectronics, dated 31 August 1977, Notice I, dated 21 July 1978.

MIL–STD–1562A Military Standard; List of Standard Microcircuits, dated 15 October 1979.

NOTE: The 3-letter suffix at the end of the type number represents device class (degree of quality assurance testing), case outline and lead material finish as shown below:



† - Qualification included TX Devices
Δ - TX and TXV Devices
§ - NATO
☑ - USAF Preferred (TX Type Only)
Ø - Mil-Std-701 Device

14A. COMMERCIAL-TO-MILITARY TYPE NUMBER CROSS REFERENCE

COMMERCIAL TYPE No.	MILITARY TYPE No. M38510/
6800	40001
8080A	42001

15. SYSTEM BLOCK DRAWINGS

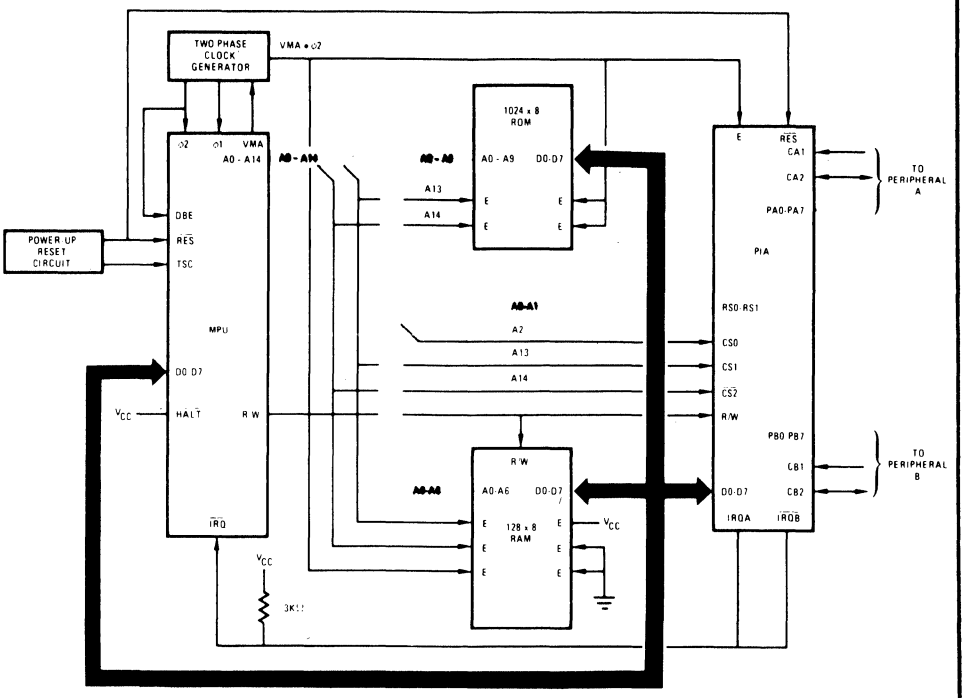
IN DRAWING NUMBER SEQUENCE

NOTES These drawings are referenced in the Microcomputer Systems section of this D.A.T.A.BOOK in accordance with information supplied by the manufacturers.

Since representations may vary, the sources of information should be consulted before critical connections are made to the systems, or to obtain additional detail.

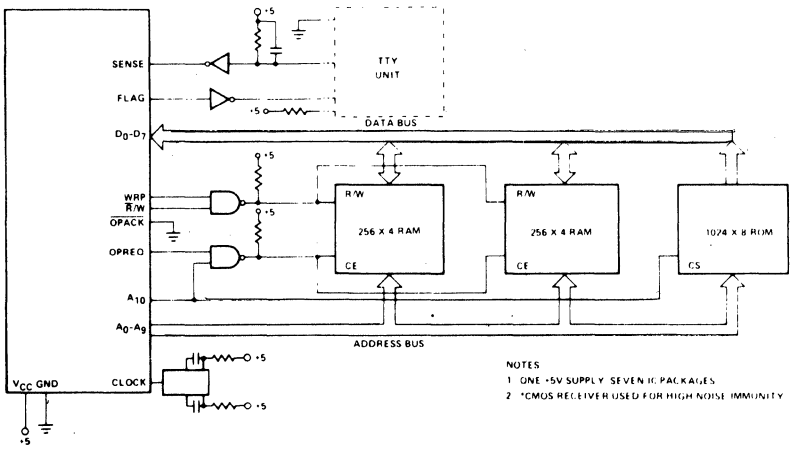
S1

S6800 AMI



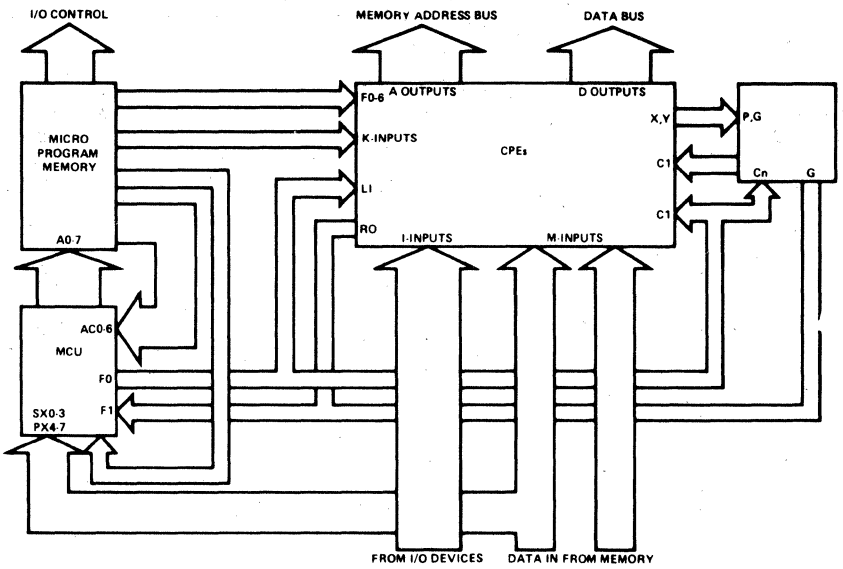
S3

2650 SIC



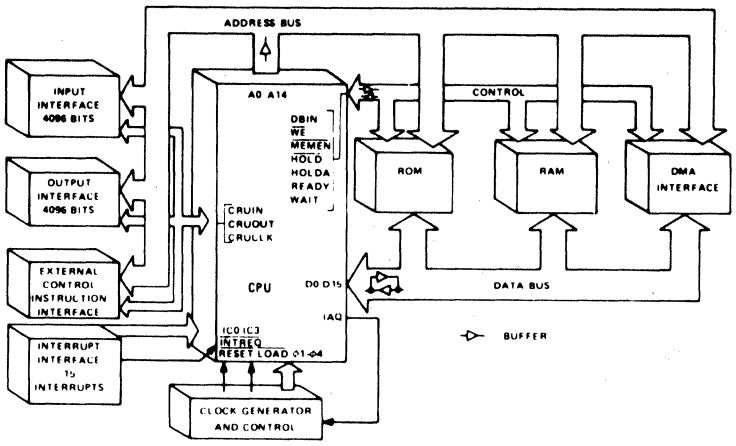
S4

3000 ITL ITL
3000 SIC SIC



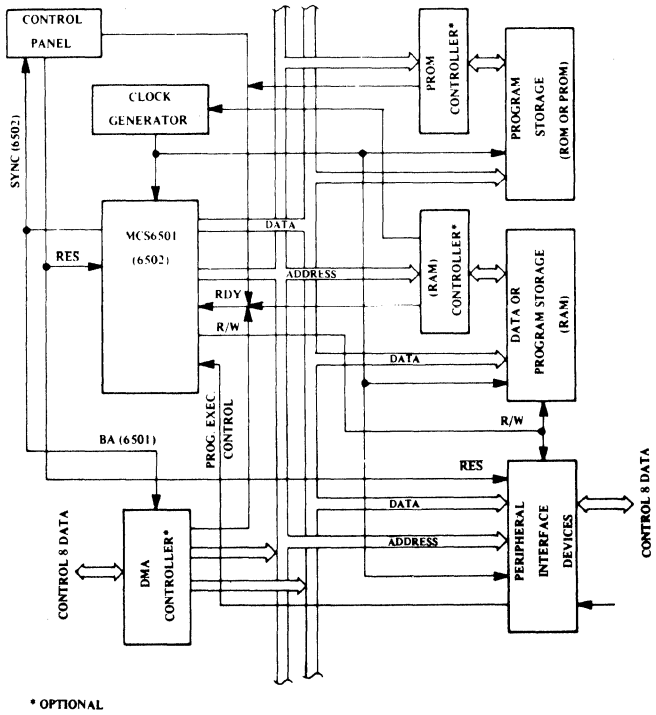
S5

990/4 TII
S9900 AMI



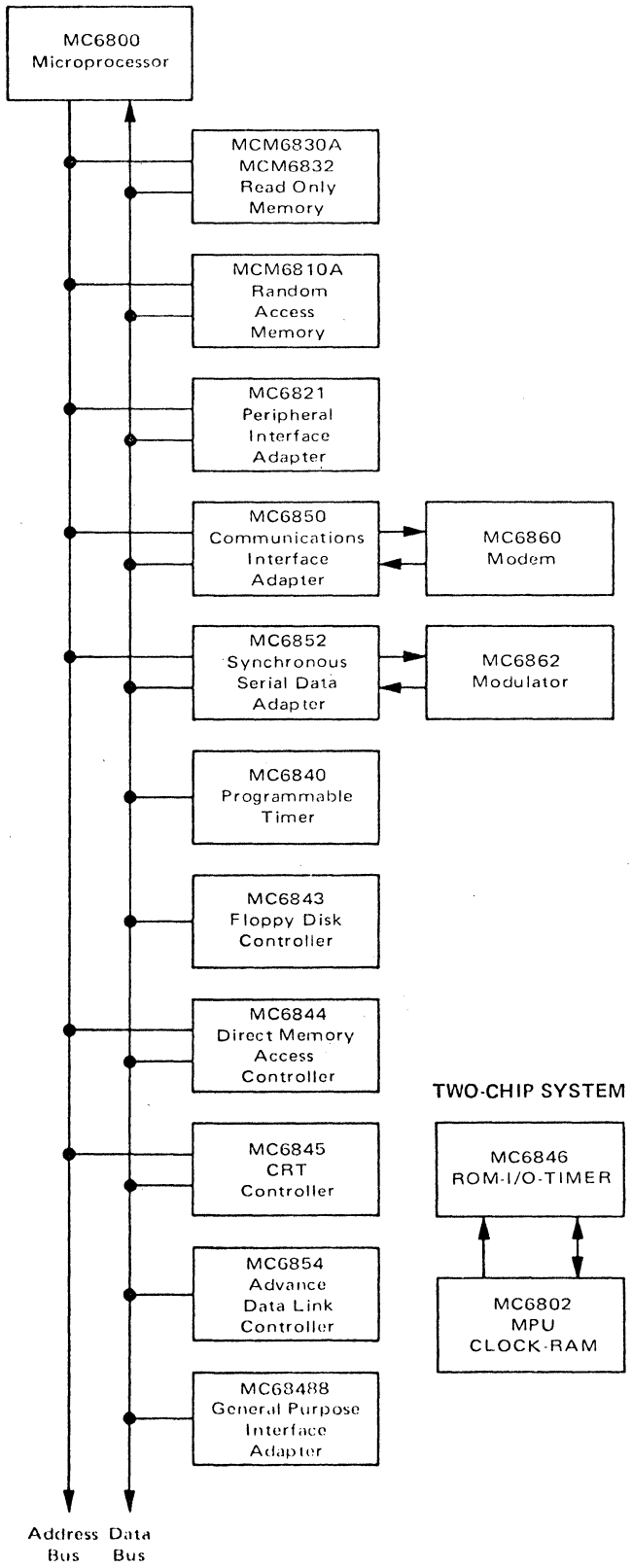
S6

MCS6500 MTY
SY6500 SYK



S7

M6800 MOTA
MICRO68 EPA
MICRO68B EPA
MICRO68K EPA



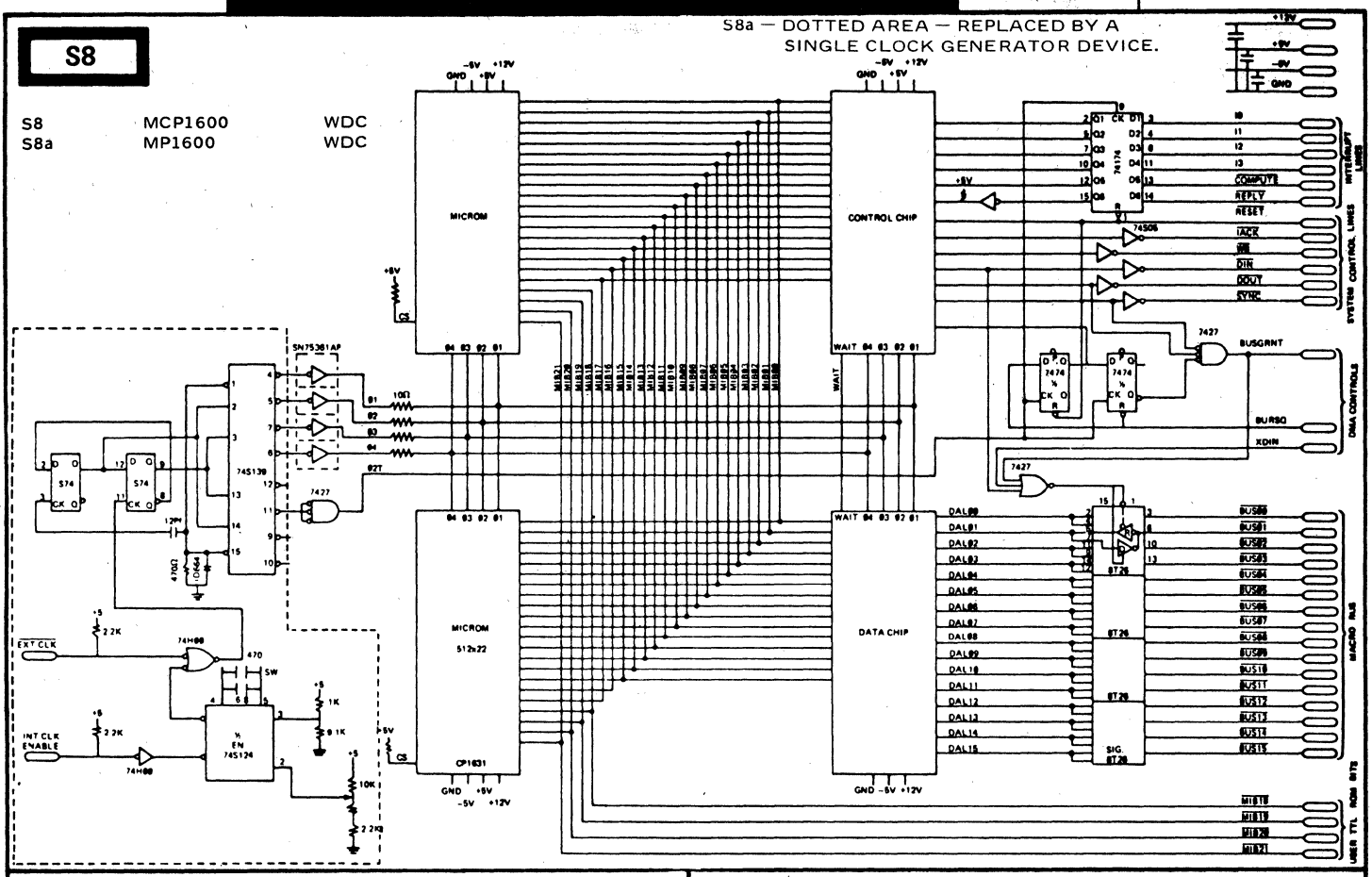
15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

S8

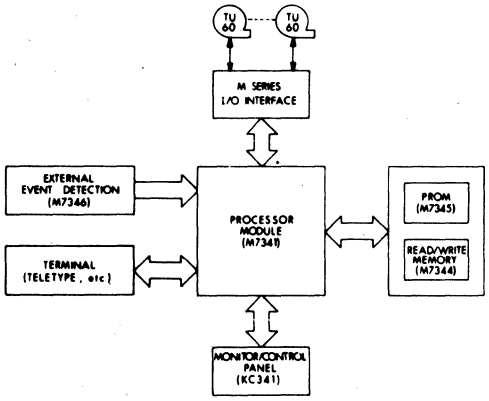
S8a — DOTTED AREA — REPLACED BY A SINGLE CLOCK GENERATOR DEVICE.

S8	MCP1600	WDC
S8a	MP1600	WDC



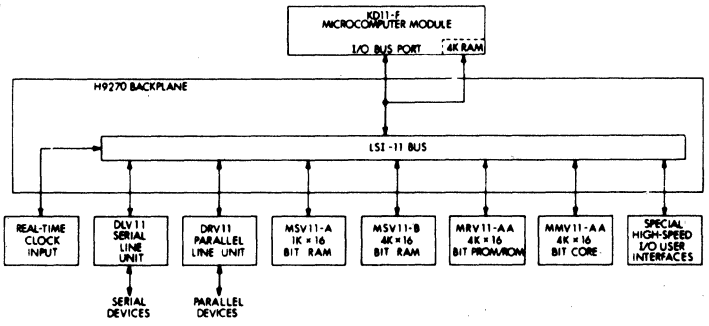
S10

MPS DEC



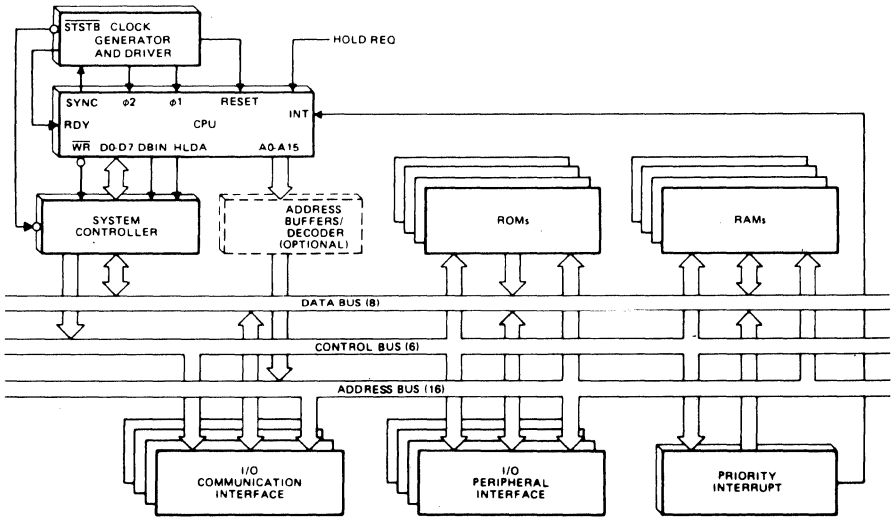
S11

LSI11 DEC
PDP11/03 DEC



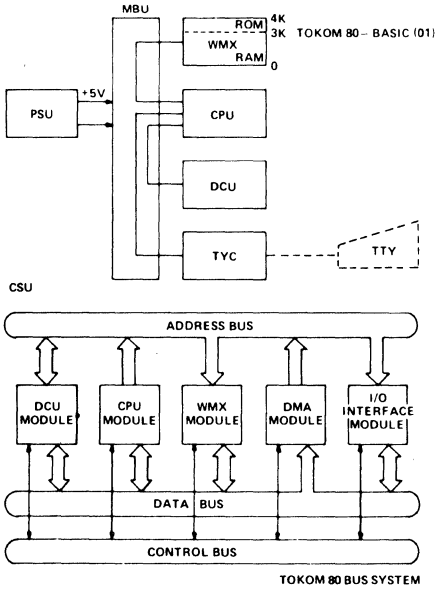
S12

MCS80 ITL



S13

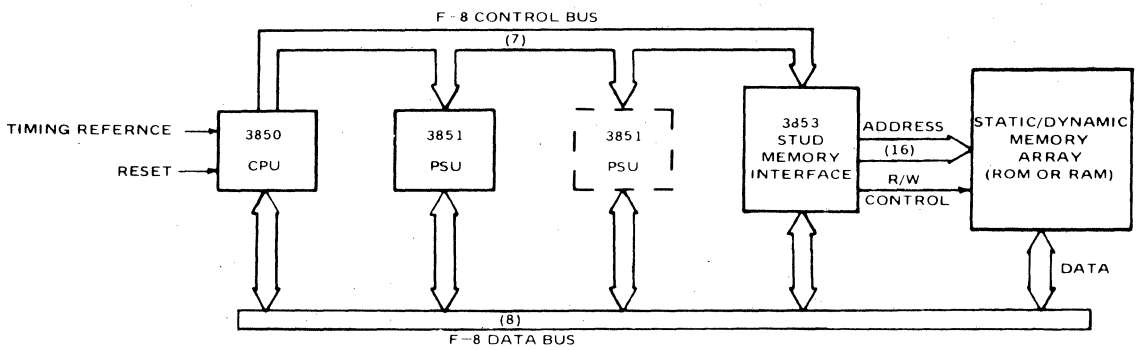
TOKOM80-01 TAI



TOKOM 80 BUS SYSTEM

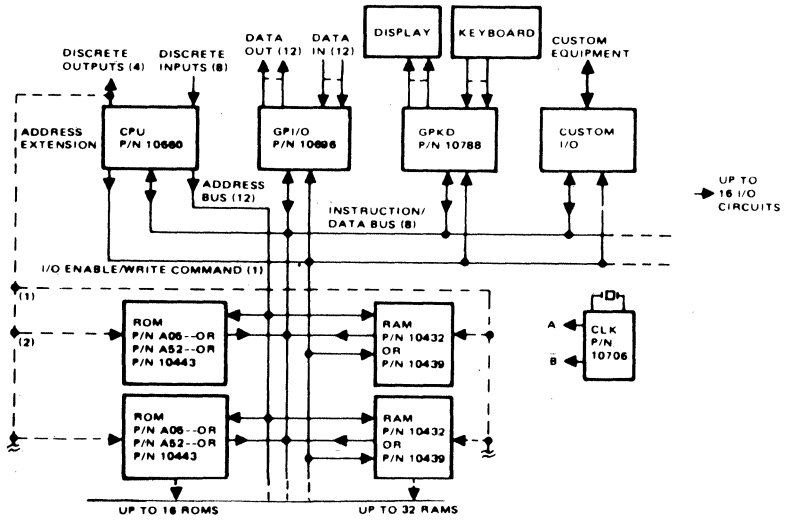
S15

F8 FSC
F8-MOS MOS



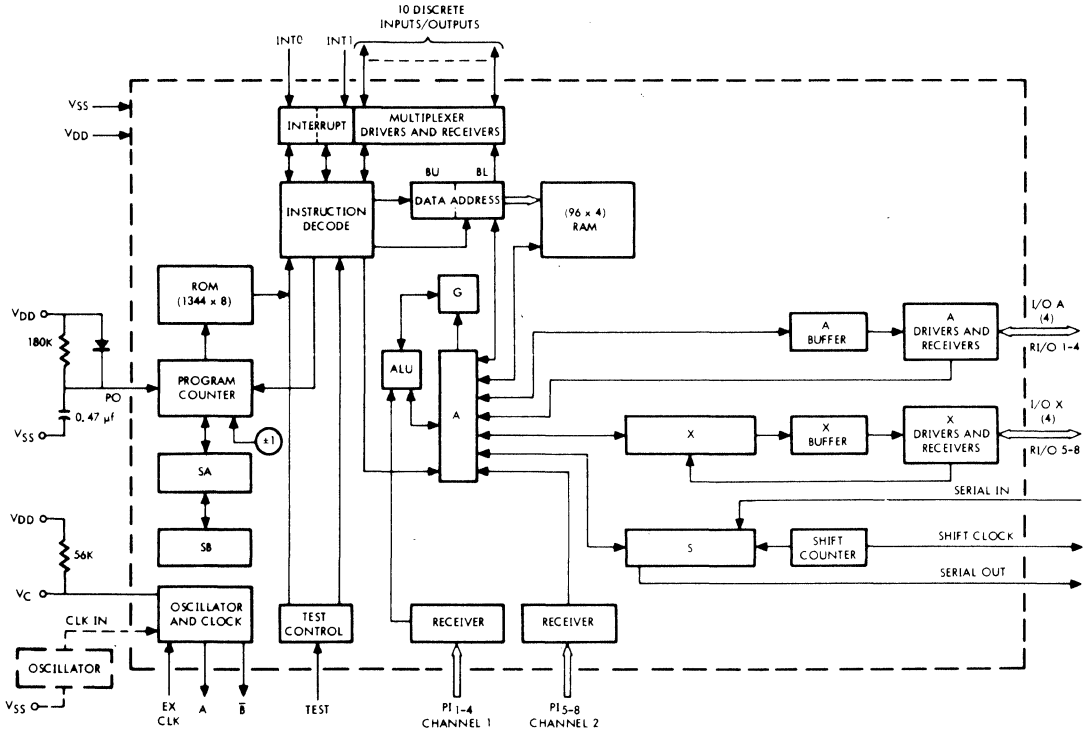
S16

PPS4 RKW
PPS4/2 RKW



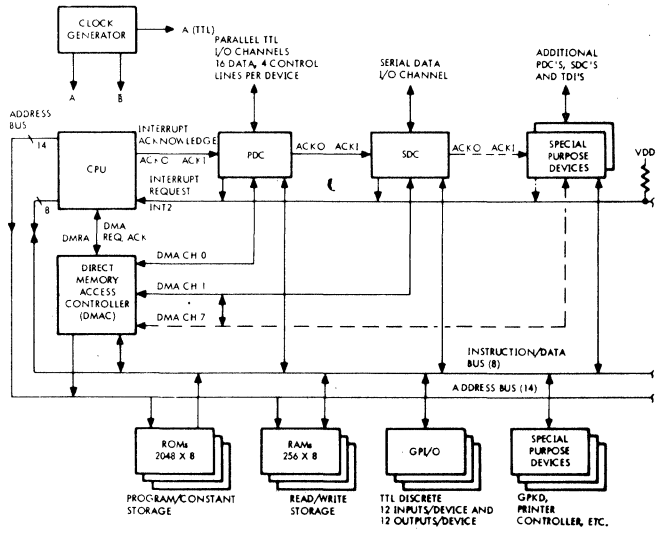
S17

PPS4/1 RKW



S18

PPS8 RKW

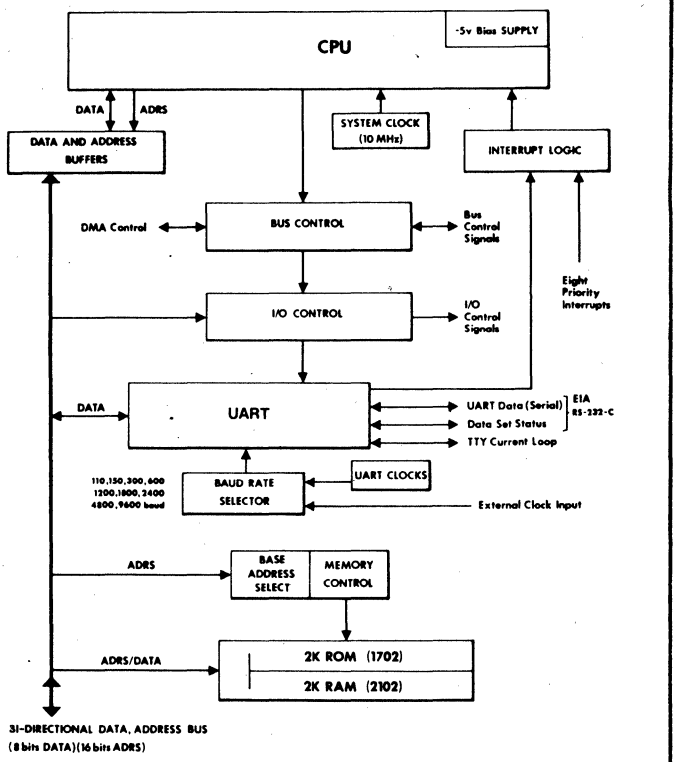


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

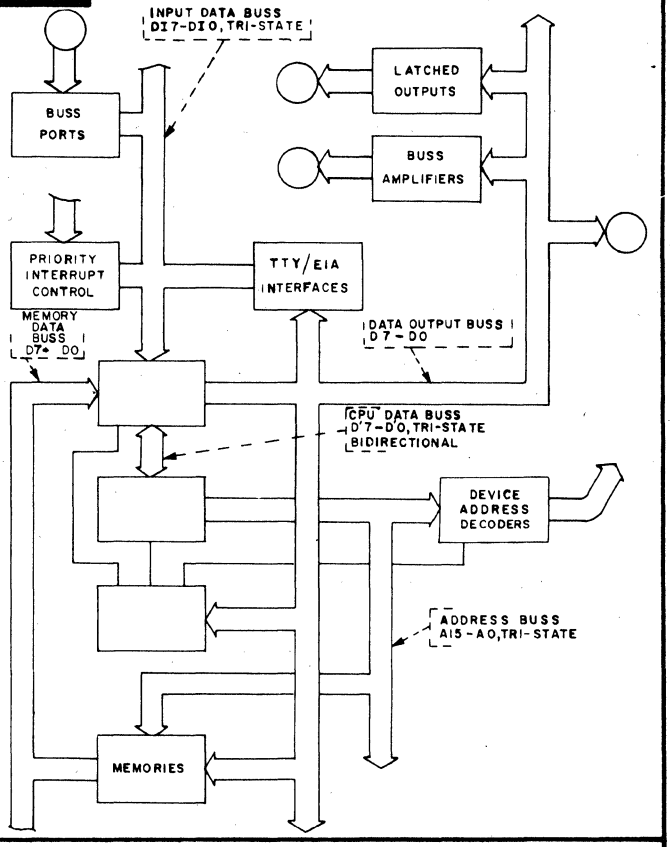
S20

MLP8080 HEU



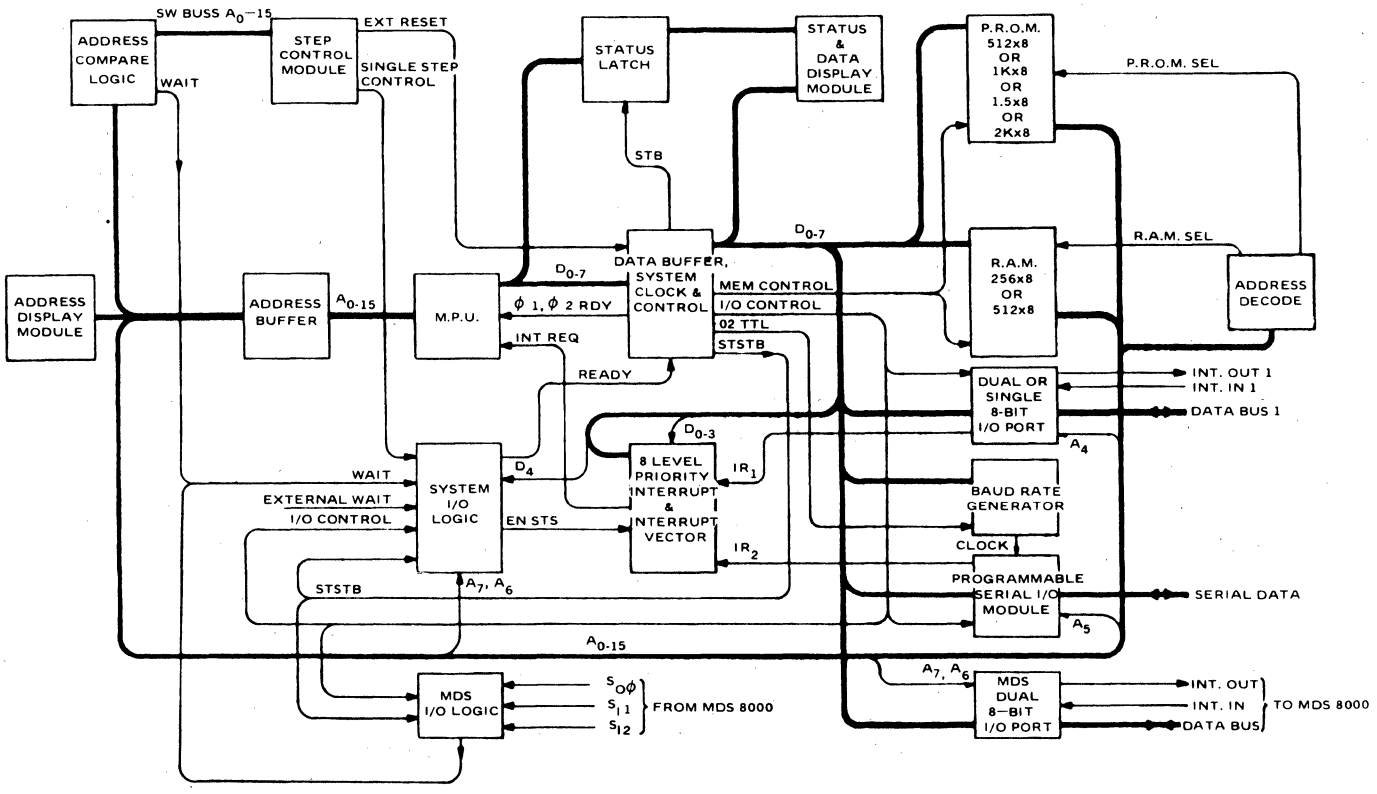
S21

L SERIES CLI
M SERIES CLI



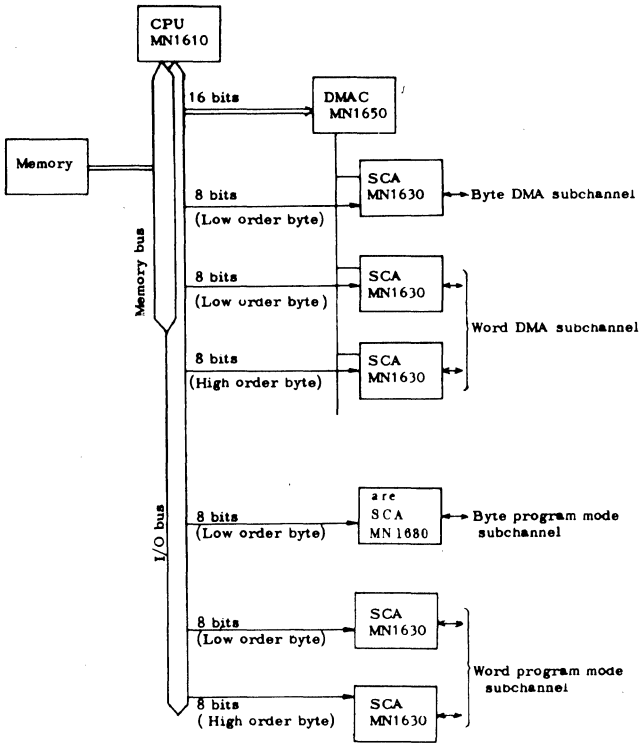
S22

MX800 ICC



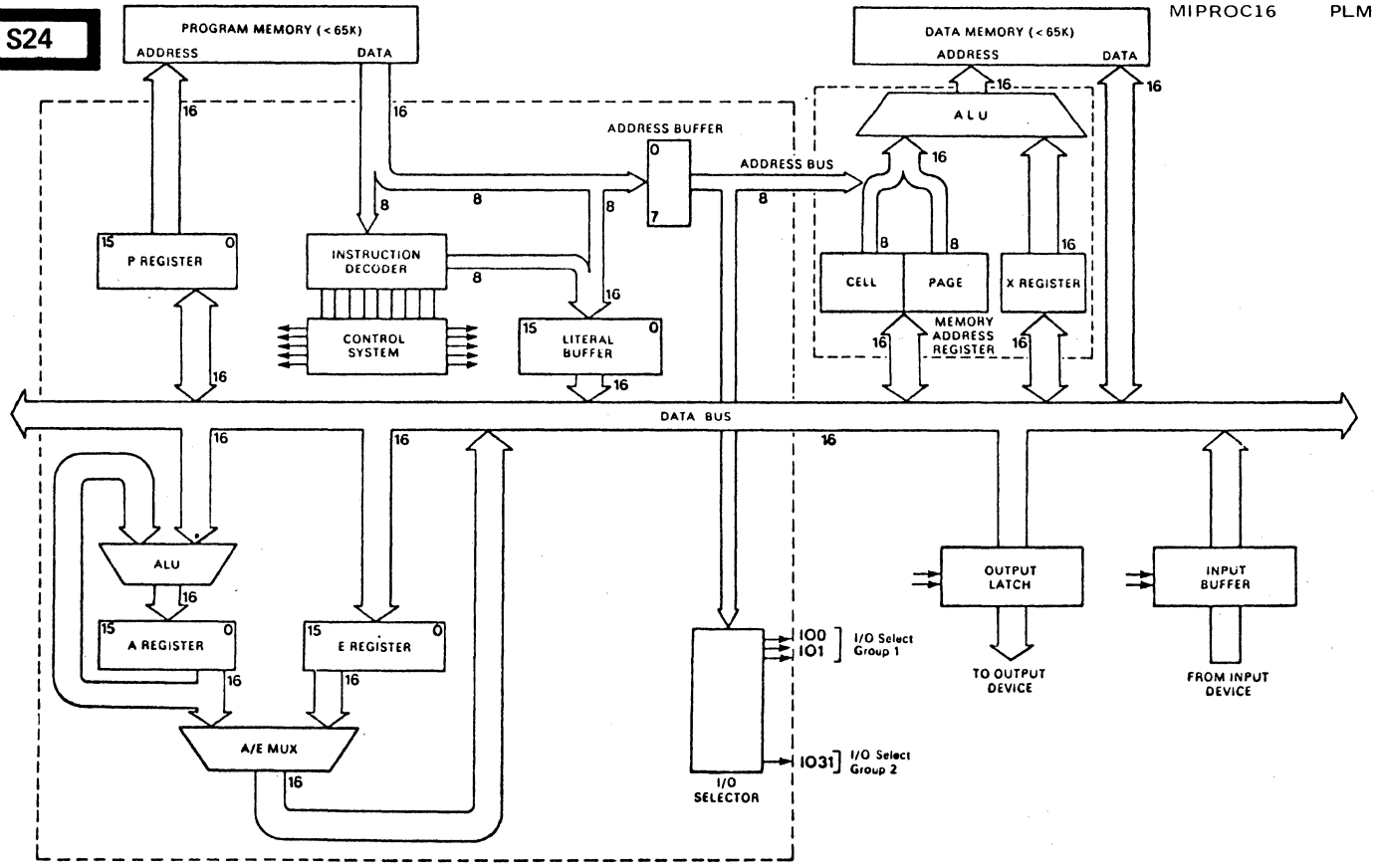
S23

PFL16A PAFJ



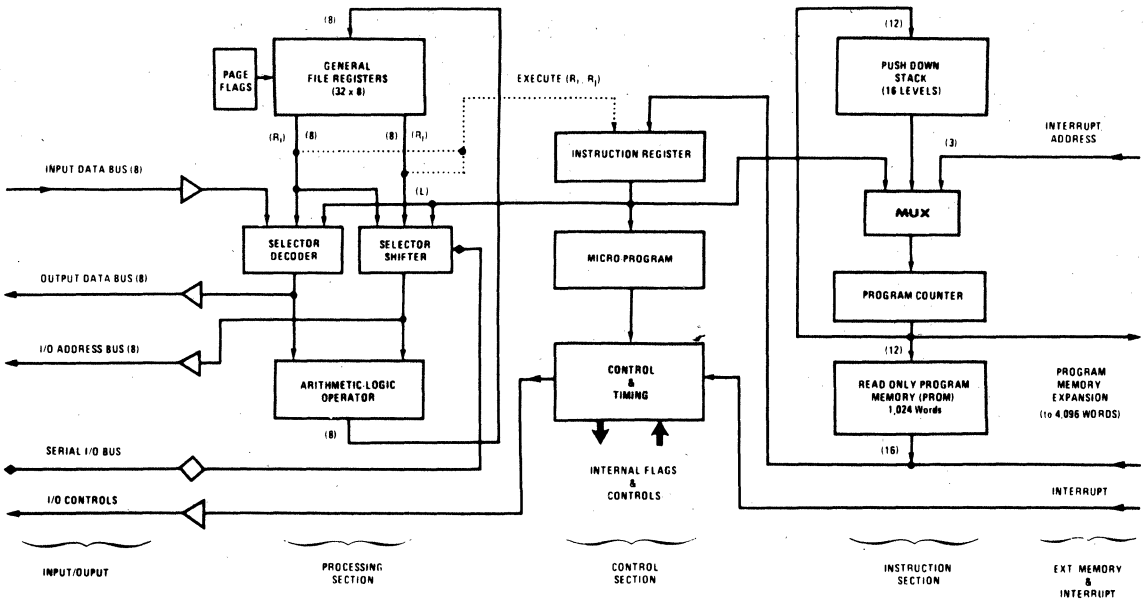
S24

MIPROC16 PLM



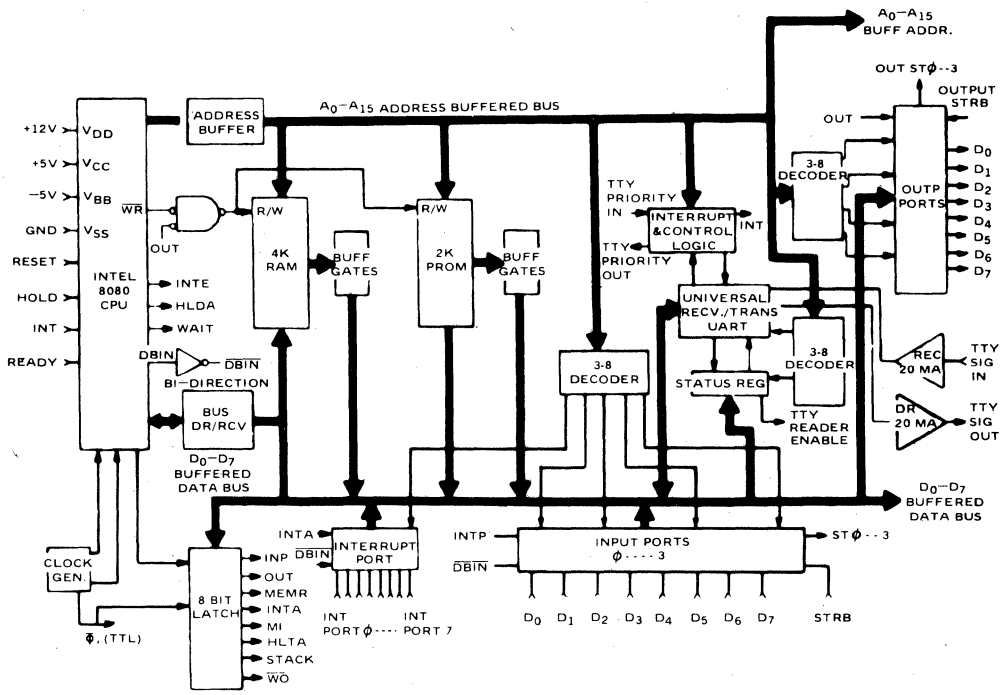
S26

XMC360 XEC



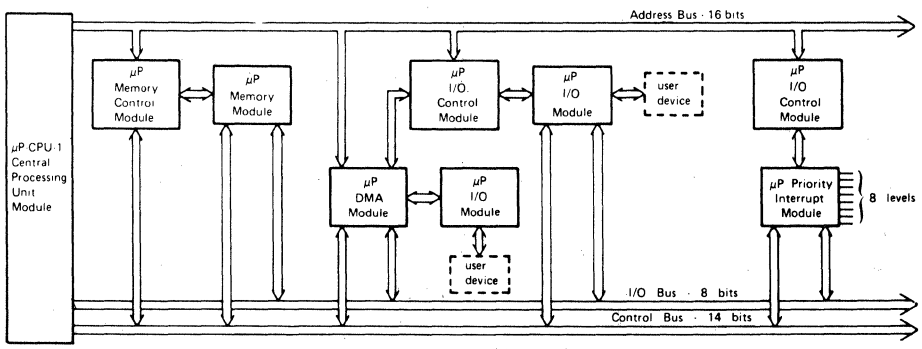
S28

DL8A DNI



S30

uP SERIES WLD



15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

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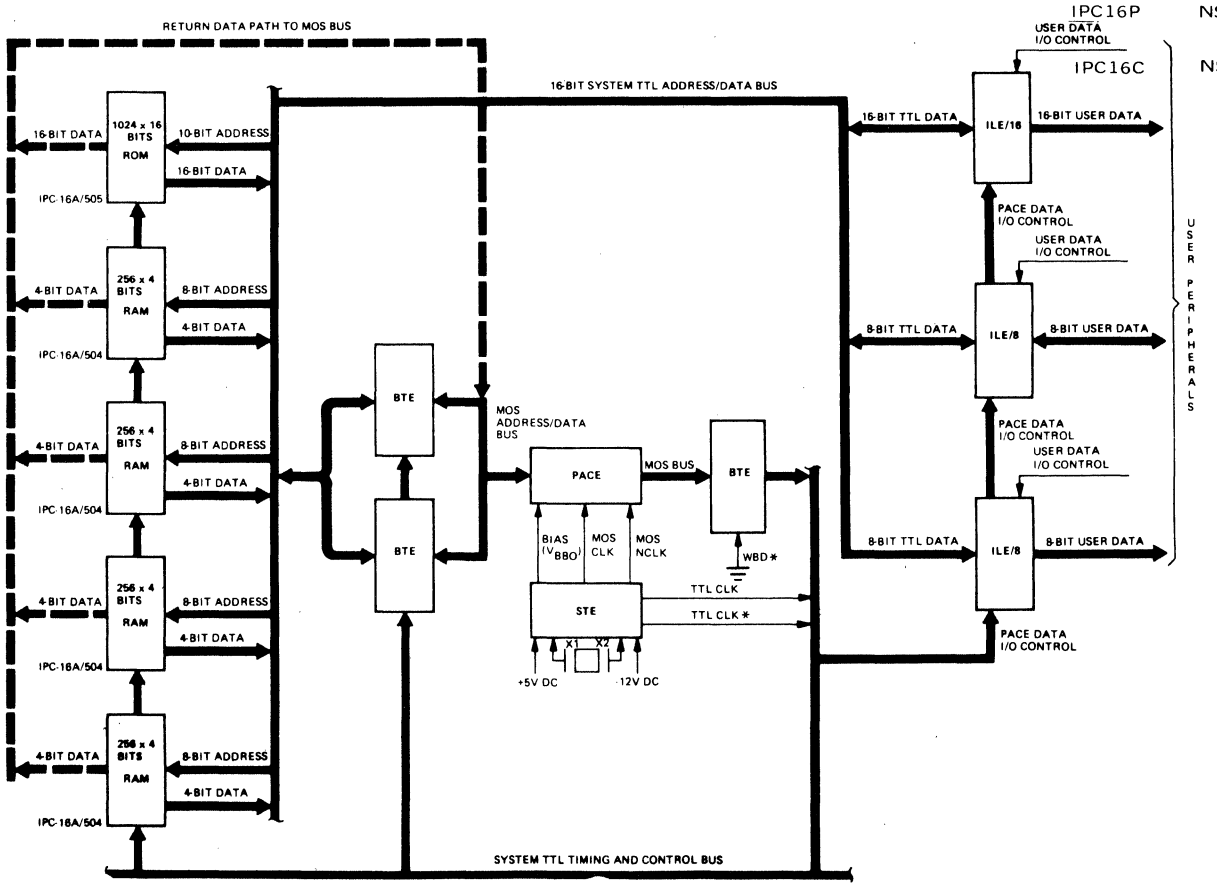
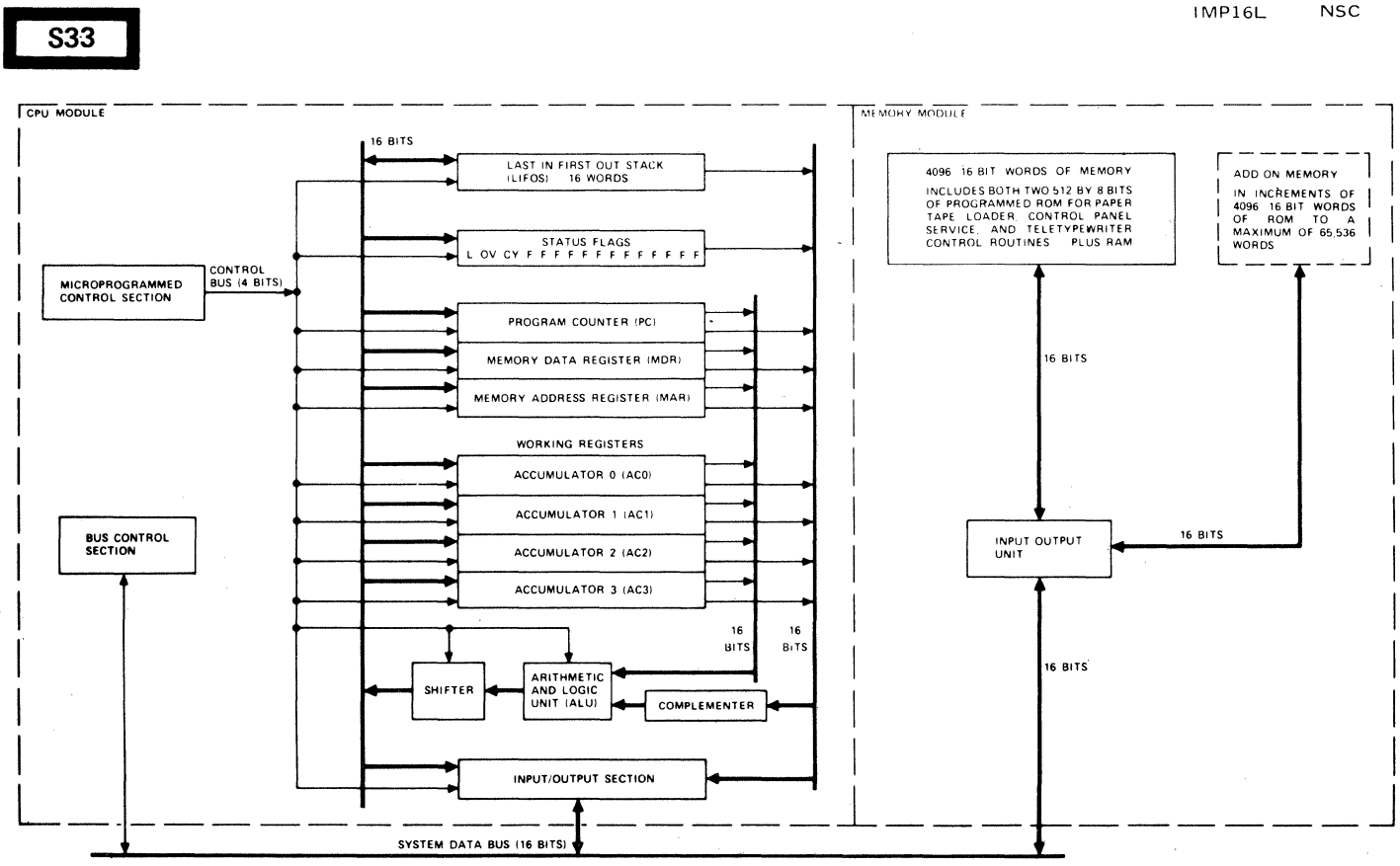


S33



15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

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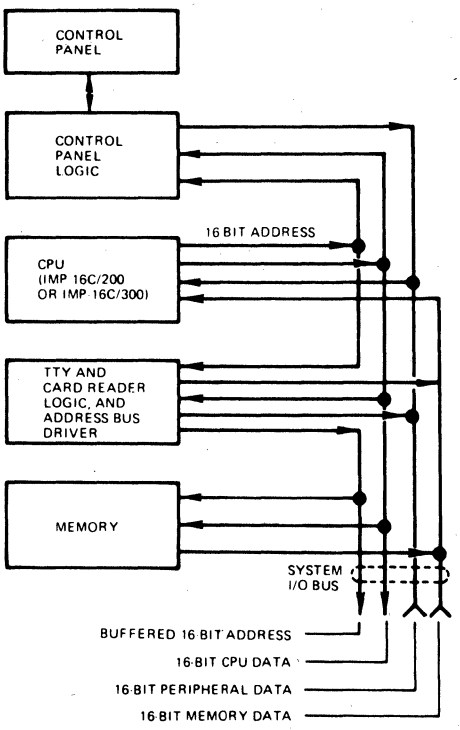
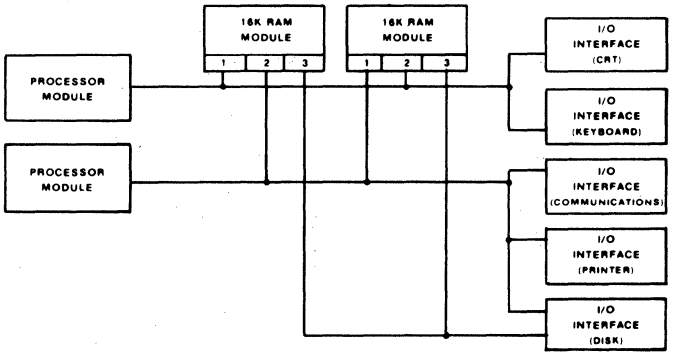
IMP16P NSC



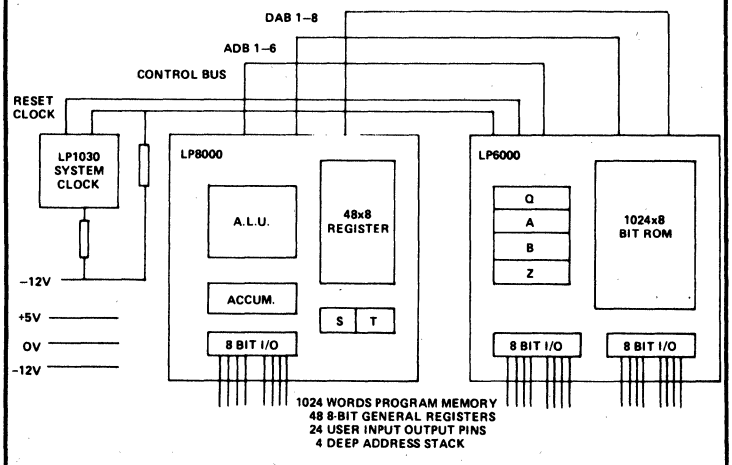
S36

SIA3000 SIA



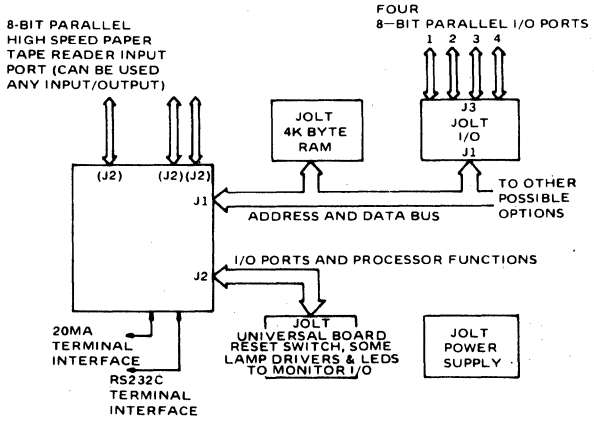
S37

LP8000 GICB

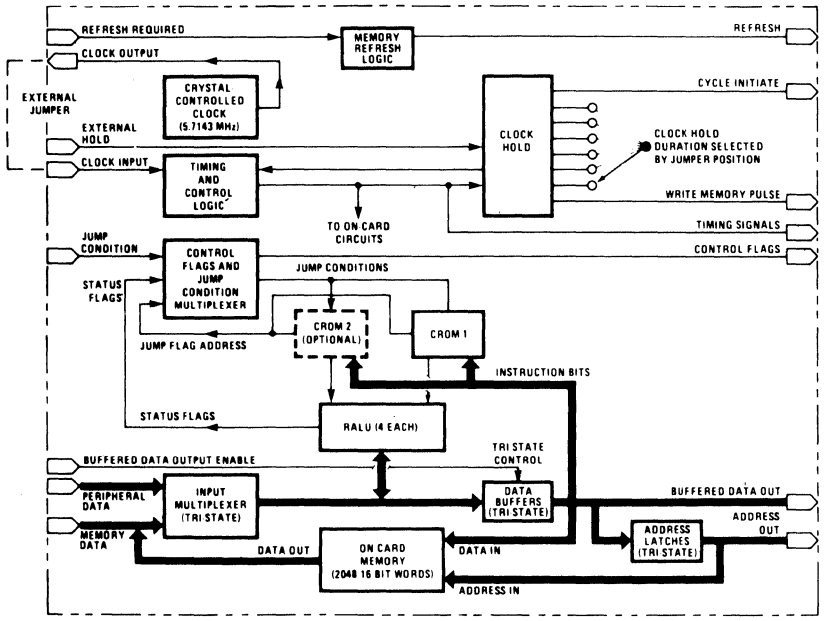


S38

JOLT MCA

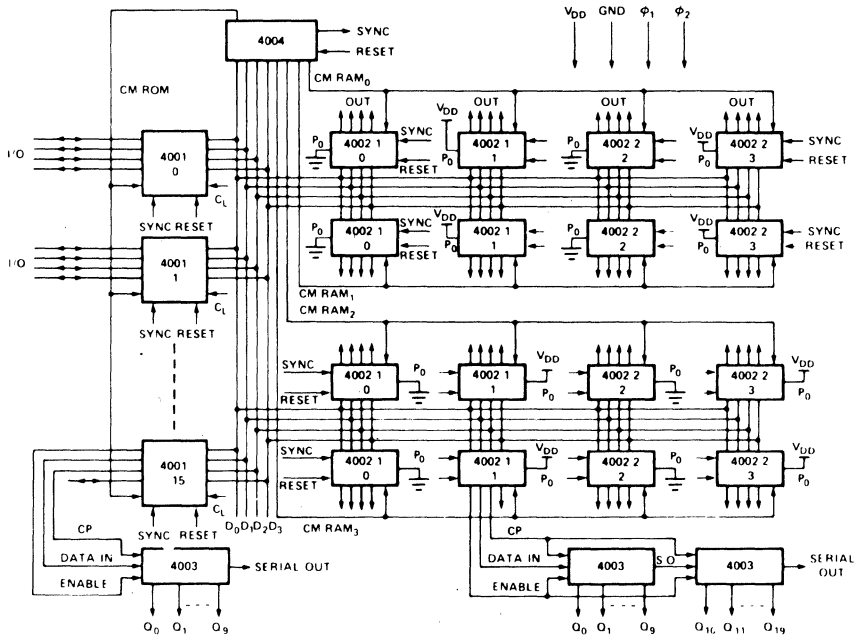


S39



S40

MCS4 ITL
FIPS NSC

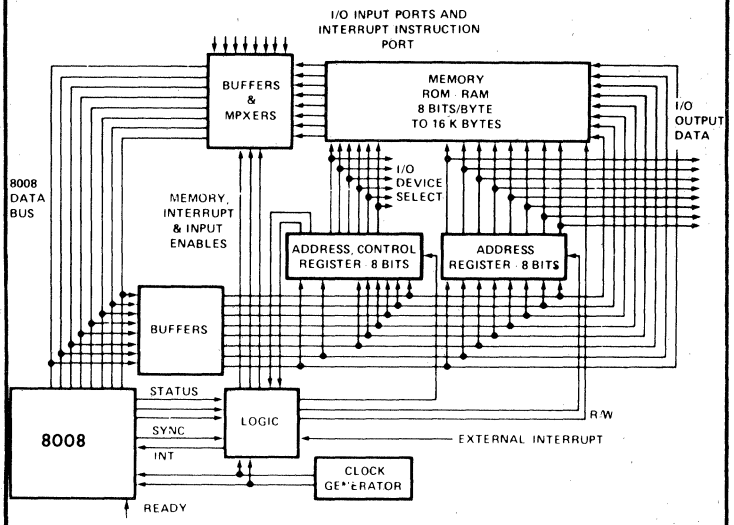


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

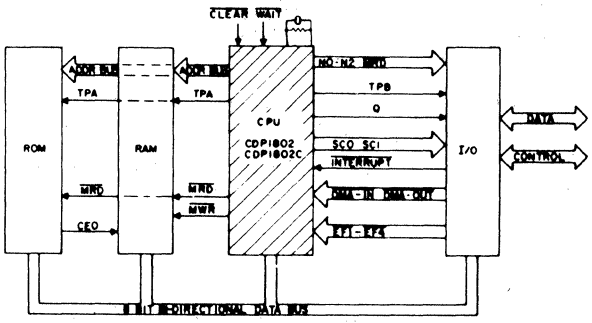
S41

MCS8 ITL



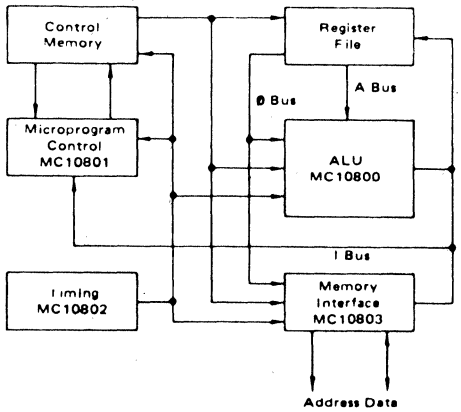
S42

CDP1800 RCA
HCMP1802 HAC
SCP1802 SSS



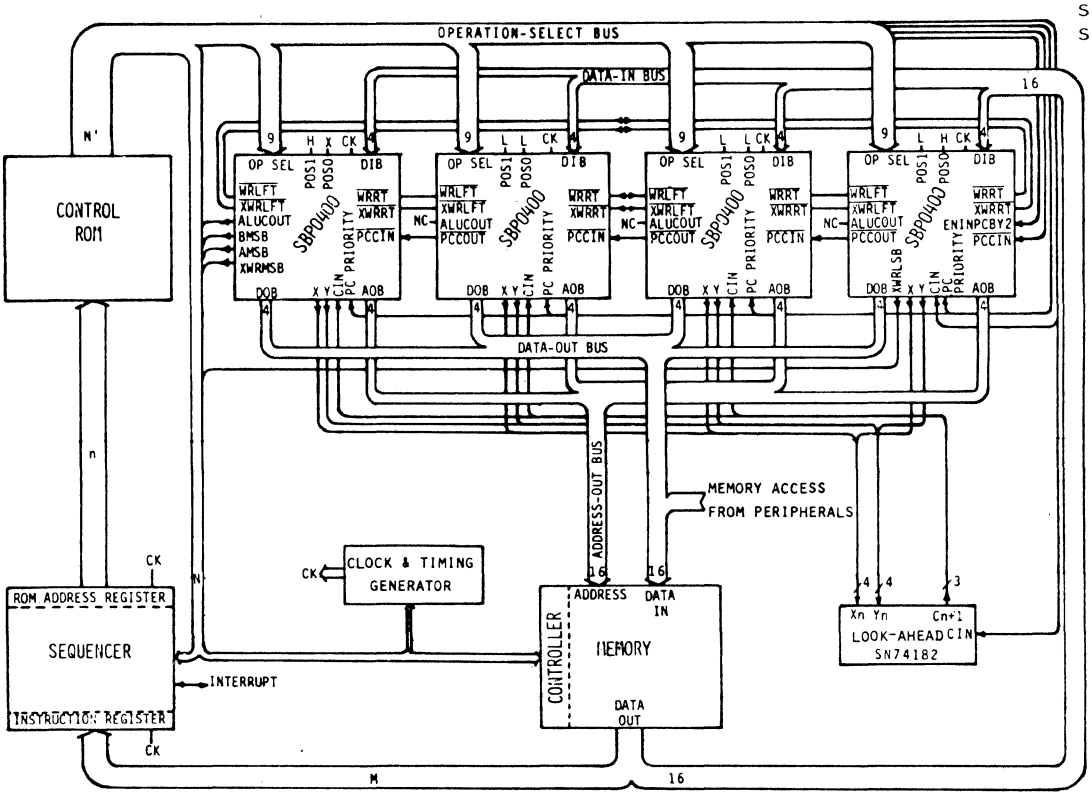
S44

M10800 MOTA



S45

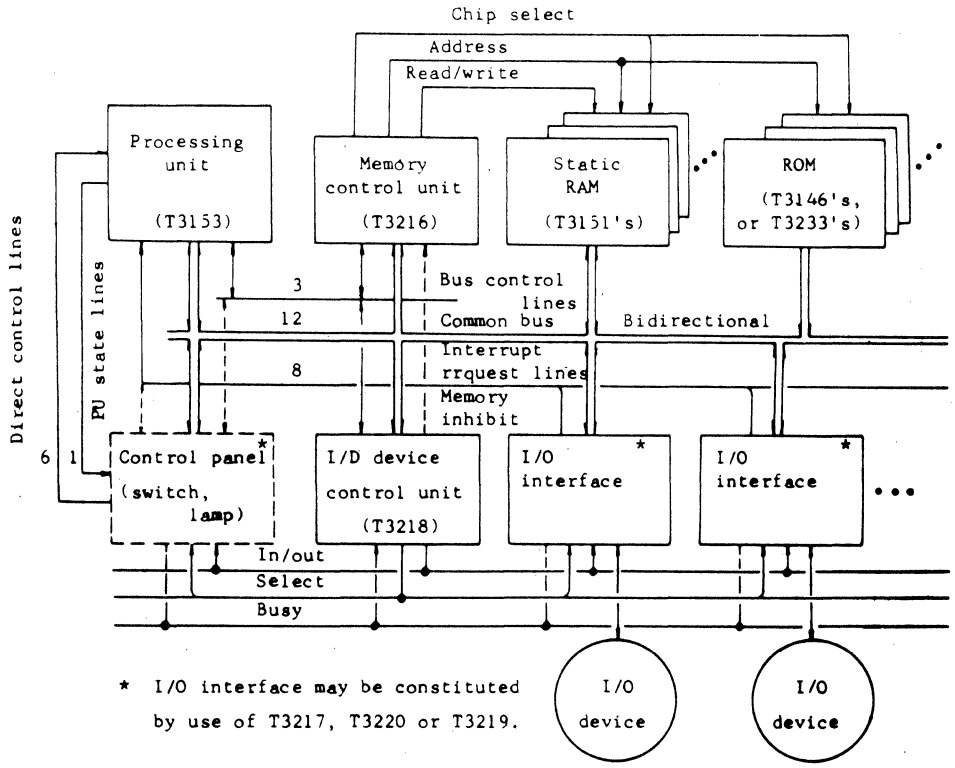
SBP0400 TII
SBP0400A TII



TYPICAL 16-BIT MACHINE USING SBP0400'S

S47

TLCS12 TOSJ



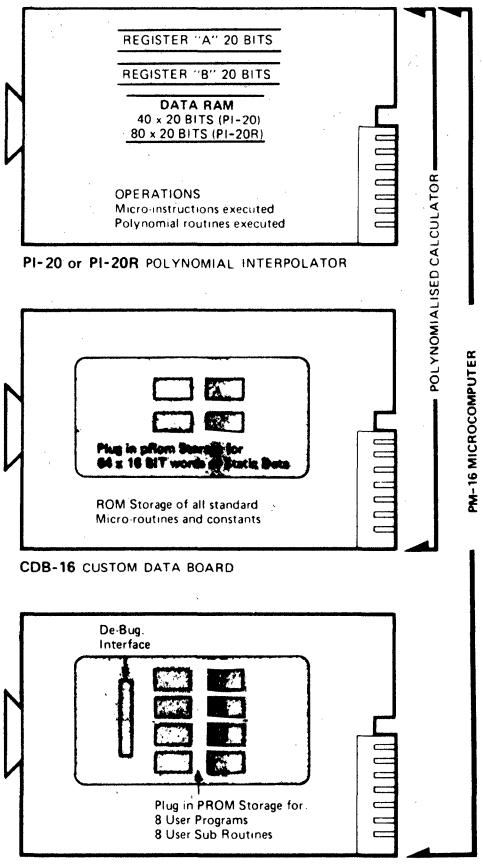
* I/O interface may be constituted by use of T3217, T3220 or T3219.

15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

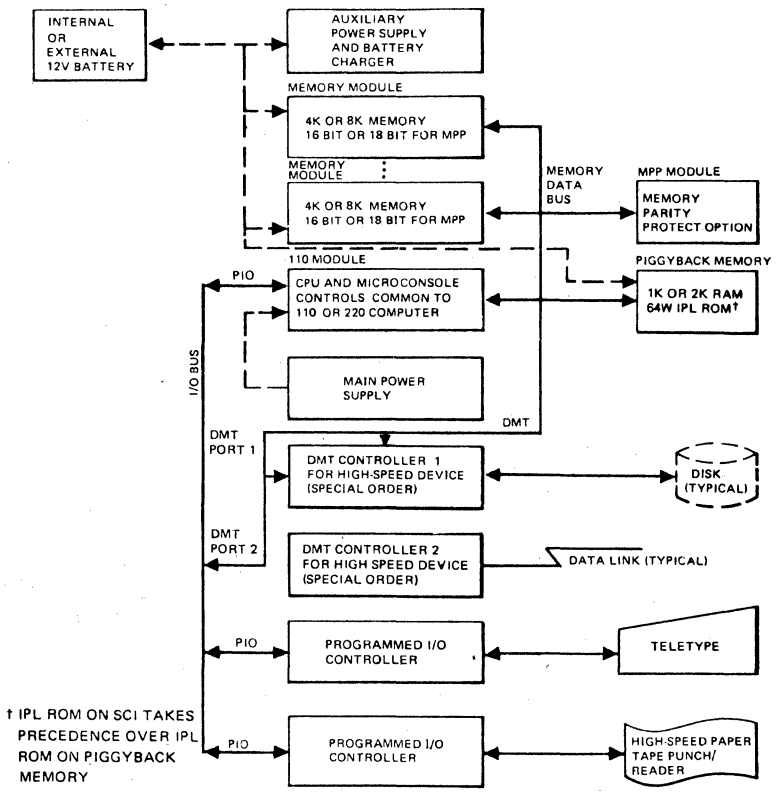
S48

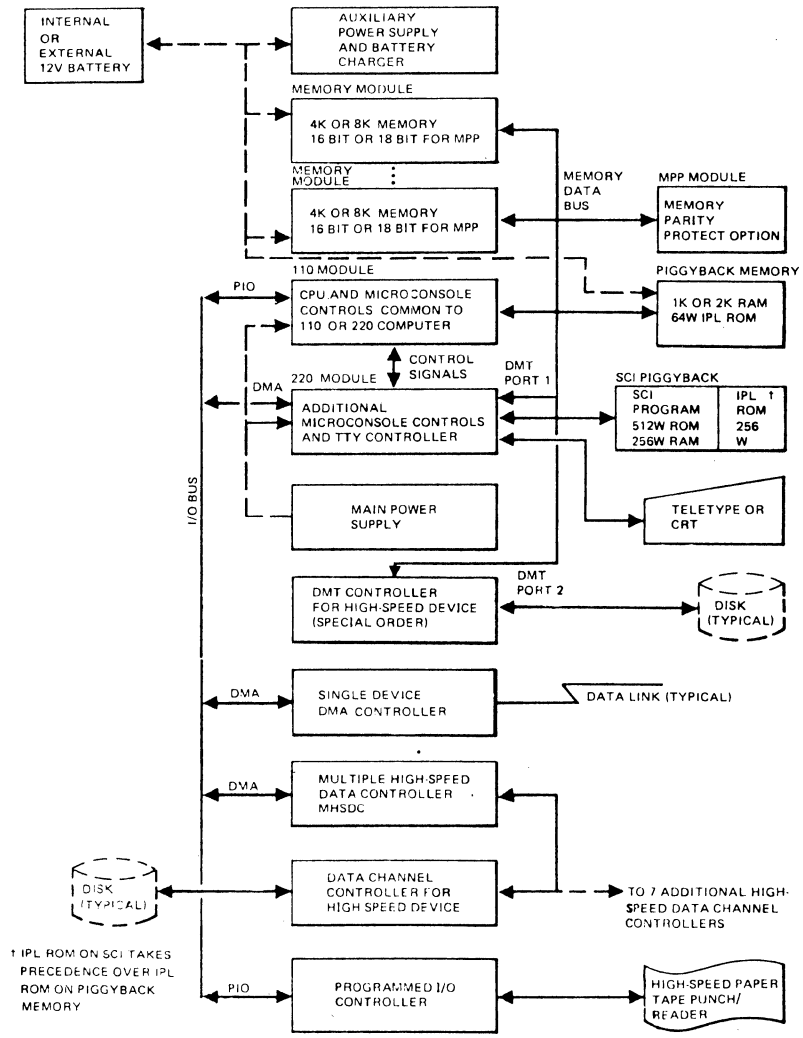
PM16-1 BAHB
PM16-2 BAHB



GA16/110 GEN

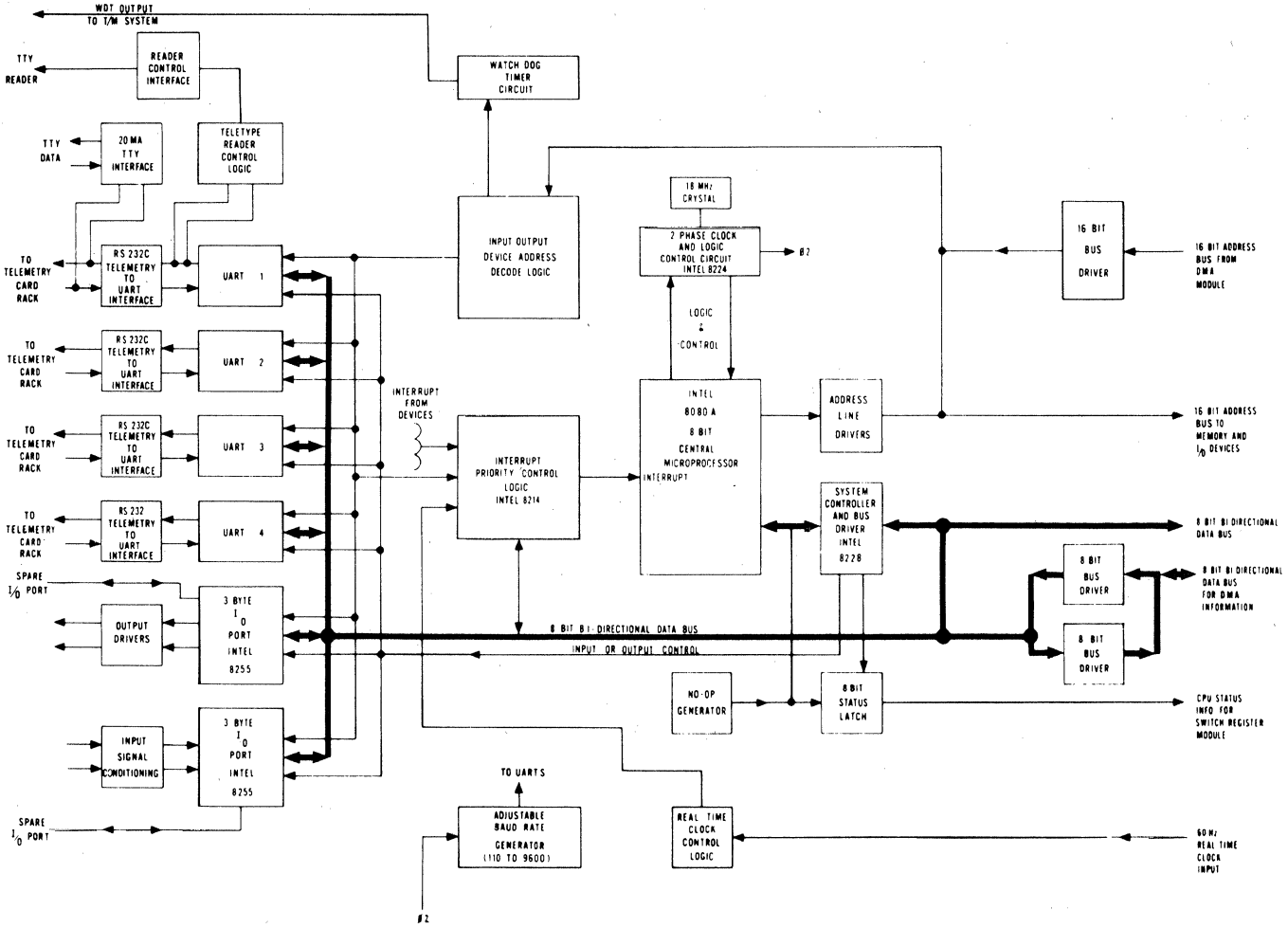
S49




INTERNAL OR EXTERNAL 12V BATTERY
AUXILIARY POWER SUPPLY AND BATTERY CHARGER
MEMORY MODULE
4K OR 8K MEMORY 16 BIT OR 18 BIT FOR MPP
MEMORY MODULE
4K OR 8K MEMORY 16 BIT OR 18 BIT FOR MPP
MEMORY DATA BUS
MPP MODULE
MEMORY PARITY PROTECT OPTION
110 MODULE
PIO
CPU AND MICROCONSOLE CONTROLS COMMON TO 110 OR 220 COMPUTER
PIGGYBACK MEMORY
1K OR 2K RAM 64W IPL ROM
CONTROL SIGNALS
DMT PORT 1
220 MODULE
DMA
ADDITIONAL MICROCONSOLE CONTROLS AND TTY CONTROLLER
SCI PIGGYBACK
SCI PROGRAM 512W ROM 256W RAM
IPL † ROM 256 W
I/O BUS
MAIN POWER SUPPLY
TELETYPE OR CRT
DMT PORT 2
DMT CONTROLLER FOR HIGH-SPEED DEVICE (SPECIAL ORDER)
DISK (TYPICAL)
DMA
SINGLE DEVICE DMA CONTROLLER
DATA LINK (TYPICAL)
DMA
MULTIPLE HIGH-SPEED DATA CONTROLLER MHSDC
DISK (TYPICAL)
DATA CHANNEL CONTROLLER FOR HIGH SPEED DEVICE
TO 7 ADDITIONAL HIGH-SPEED DATA CHANNEL CONTROLLERS
† IPL ROM ON SCI TAKES PRECEDENCE OVER IPL ROM ON PIGGYBACK MEMORY
PIO
PROGRAMMED I/O CONTROLLER
HIGH-SPEED PAPER TAPE PUNCH/ READER

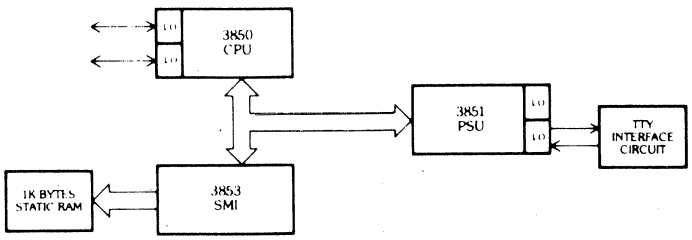
S51

808A MULT MUL



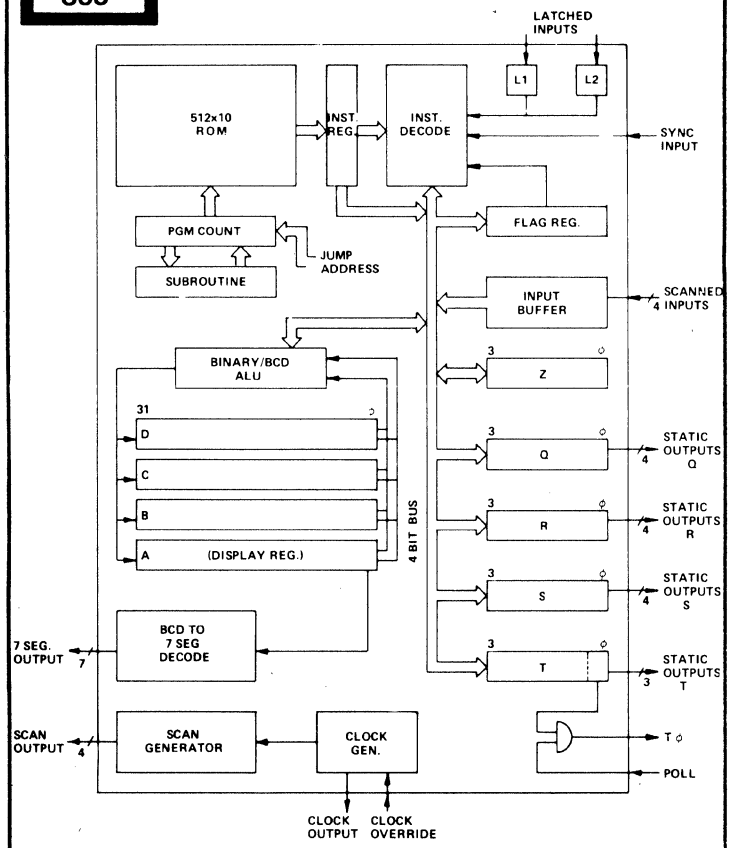
S52

MICROPRO FSC



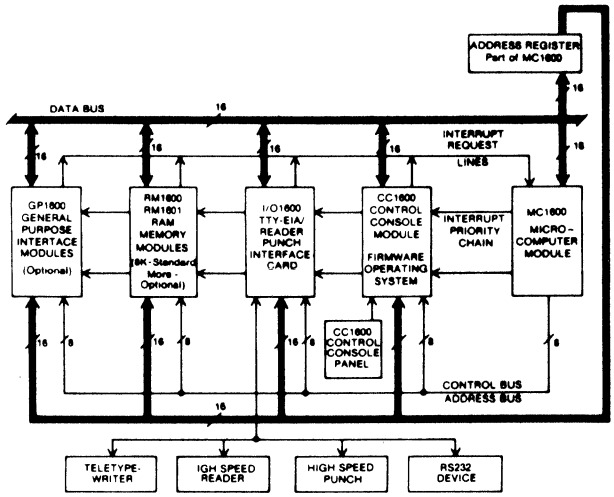
S53

CR1872 WDC



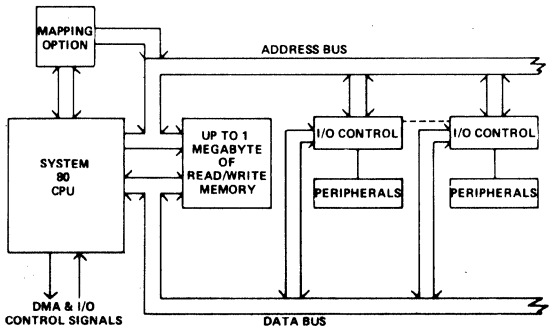
S55

GIMINI GIC



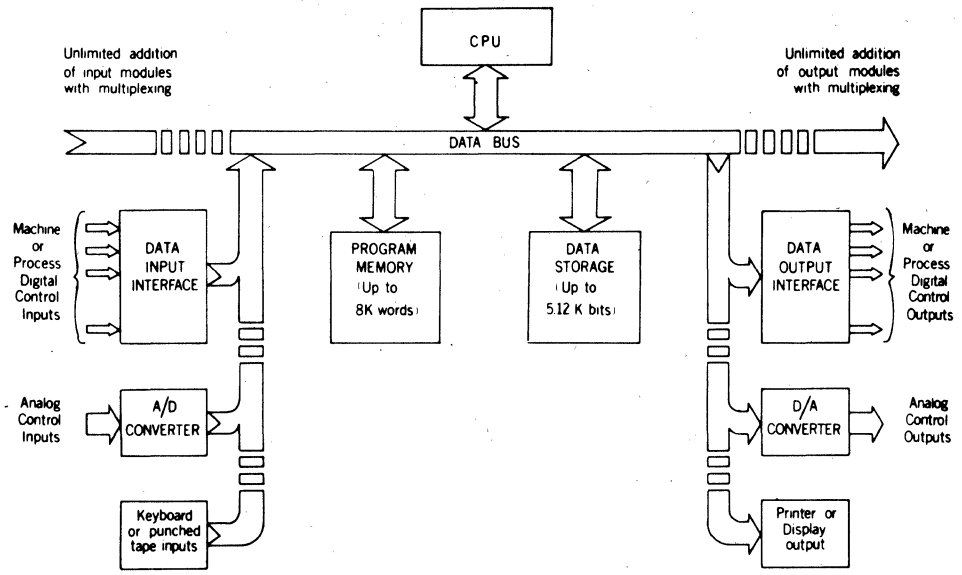
S57

SYSTEM80C EMM
SYSTEM80HS EMM
SYSTEM80S EMM



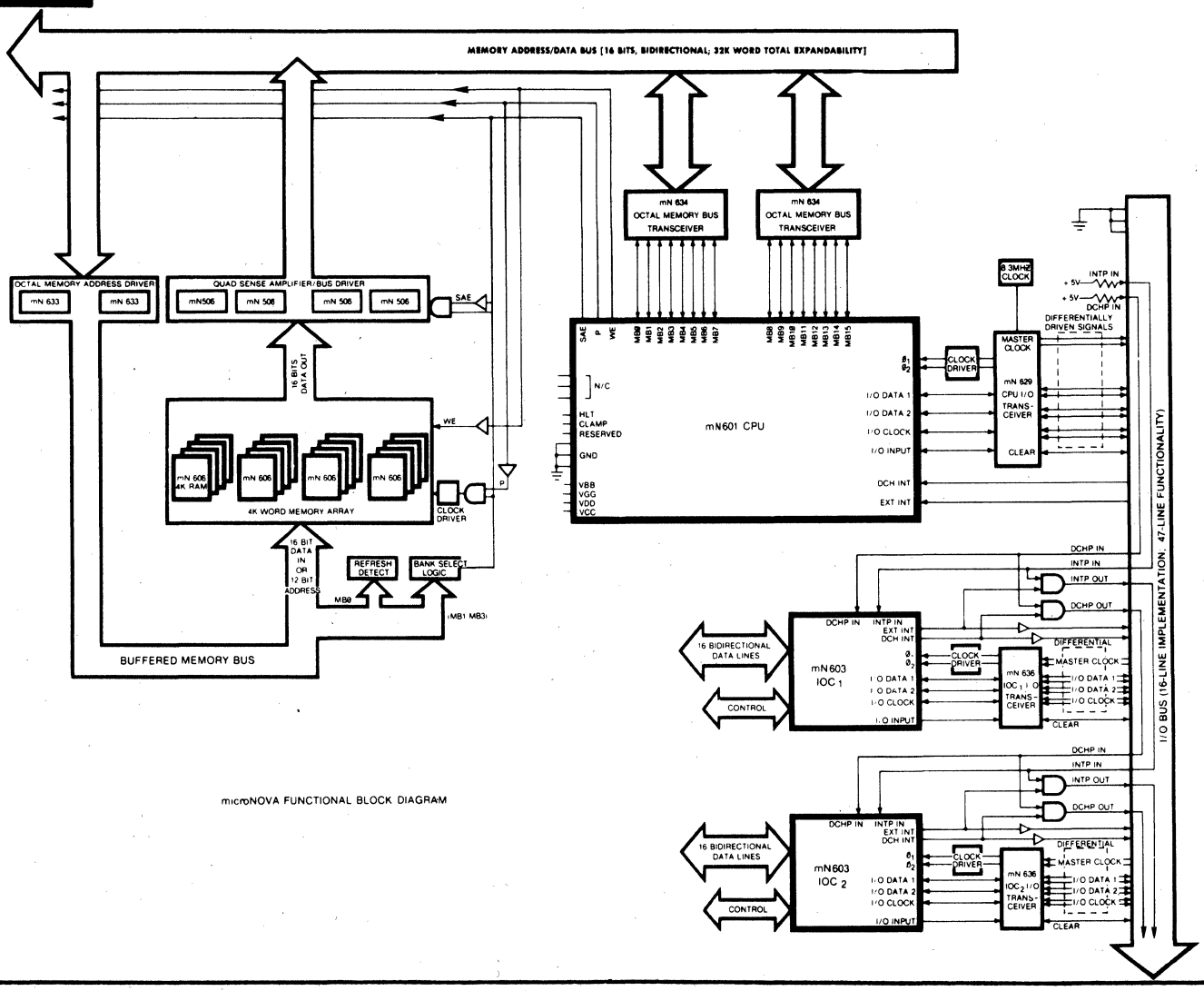
S58

IMC40 COM



S59

MICRONOVA DGC



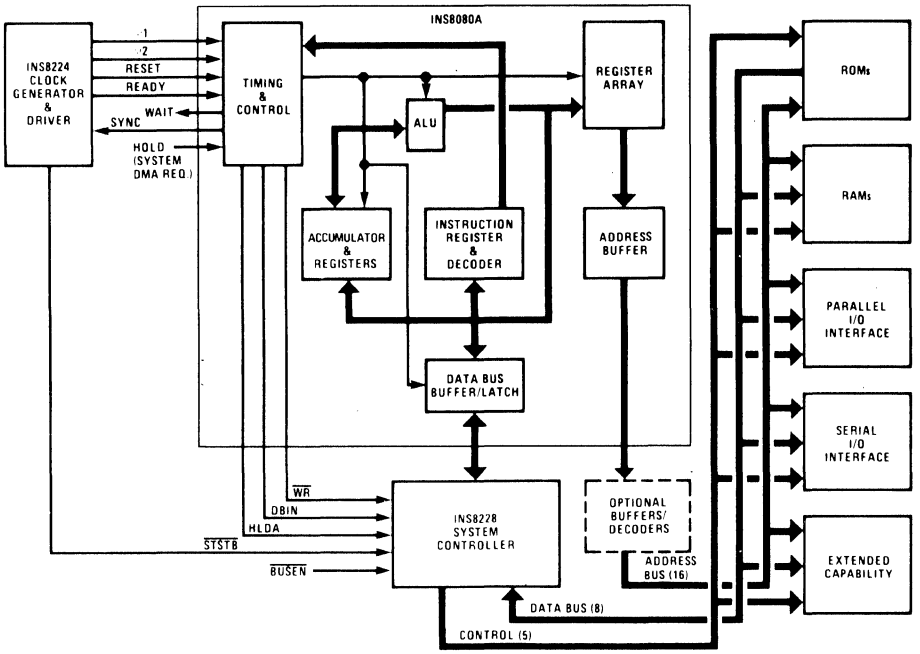
microNOVA FUNCTIONAL BLOCK DIAGRAM

15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

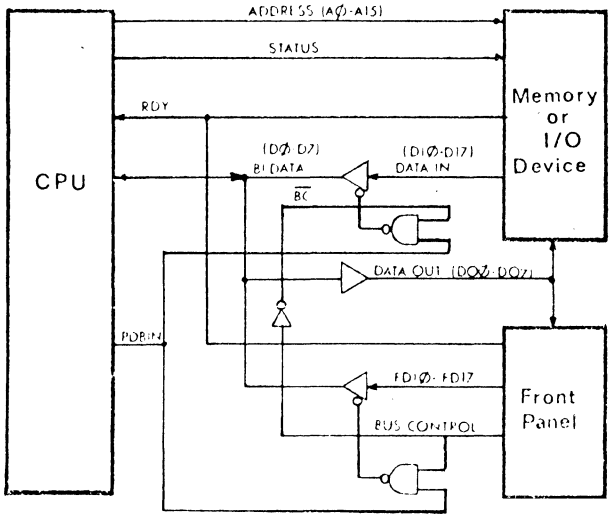
S60

N8080A NSC



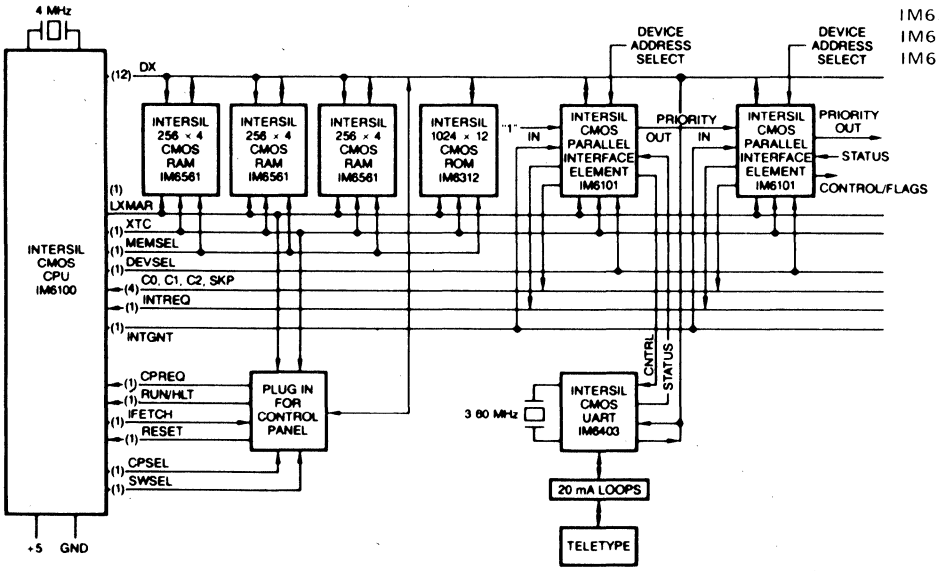
S61

ALTAIR8800B PCC
ALTAIR8800B-T PCC



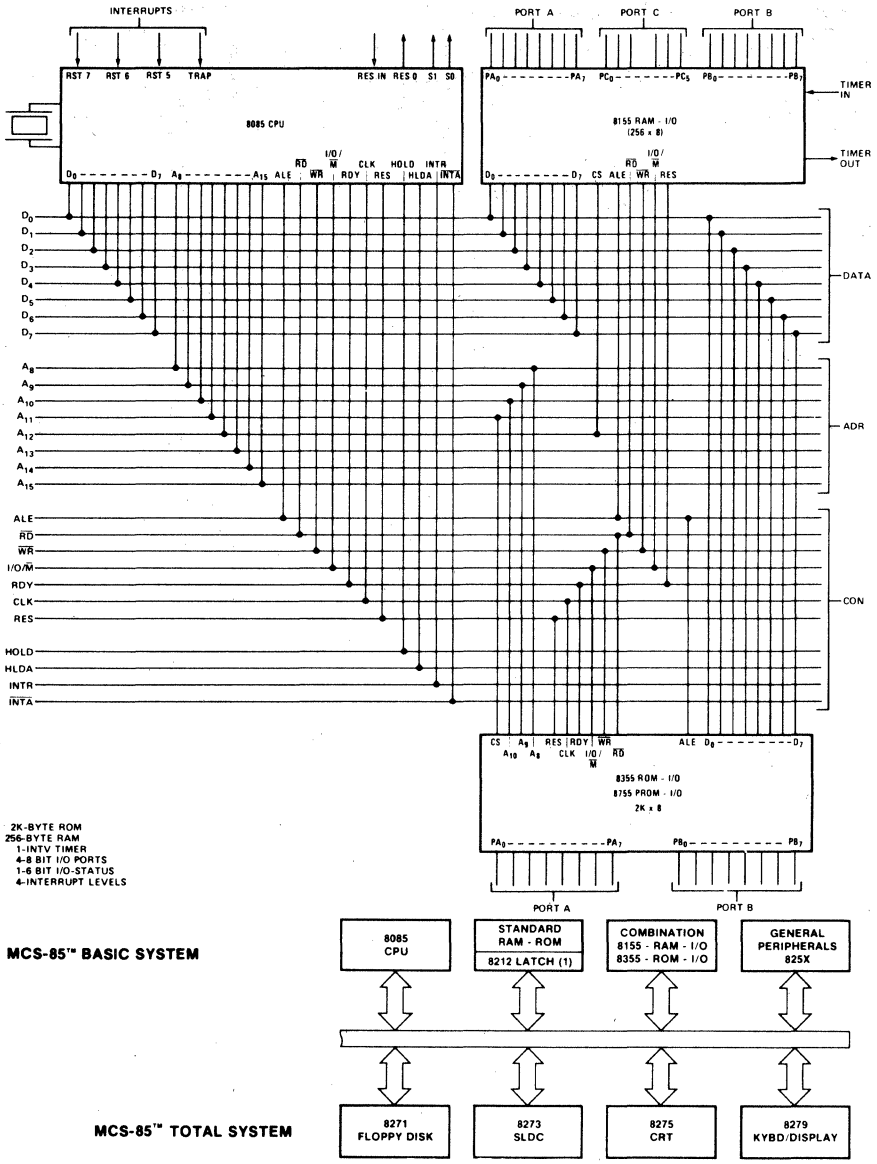
S62

IM6100 INL
IM6100A INL
IM6100C INL



S64

MSC85 ITL

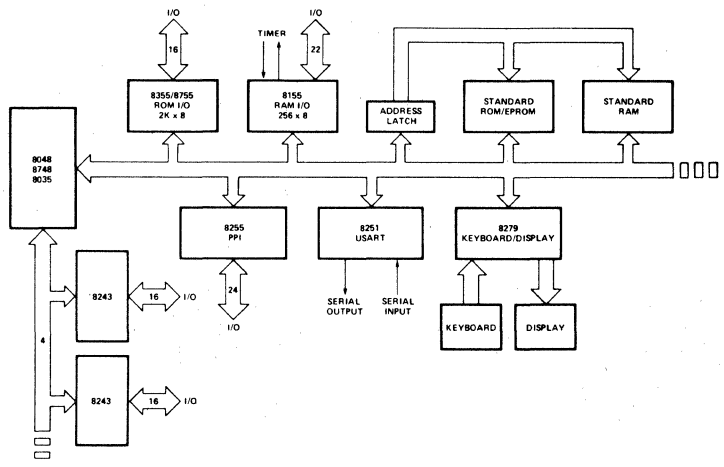


MCS-85™ BASIC SYSTEM

MCS-85™ TOTAL SYSTEM

S65

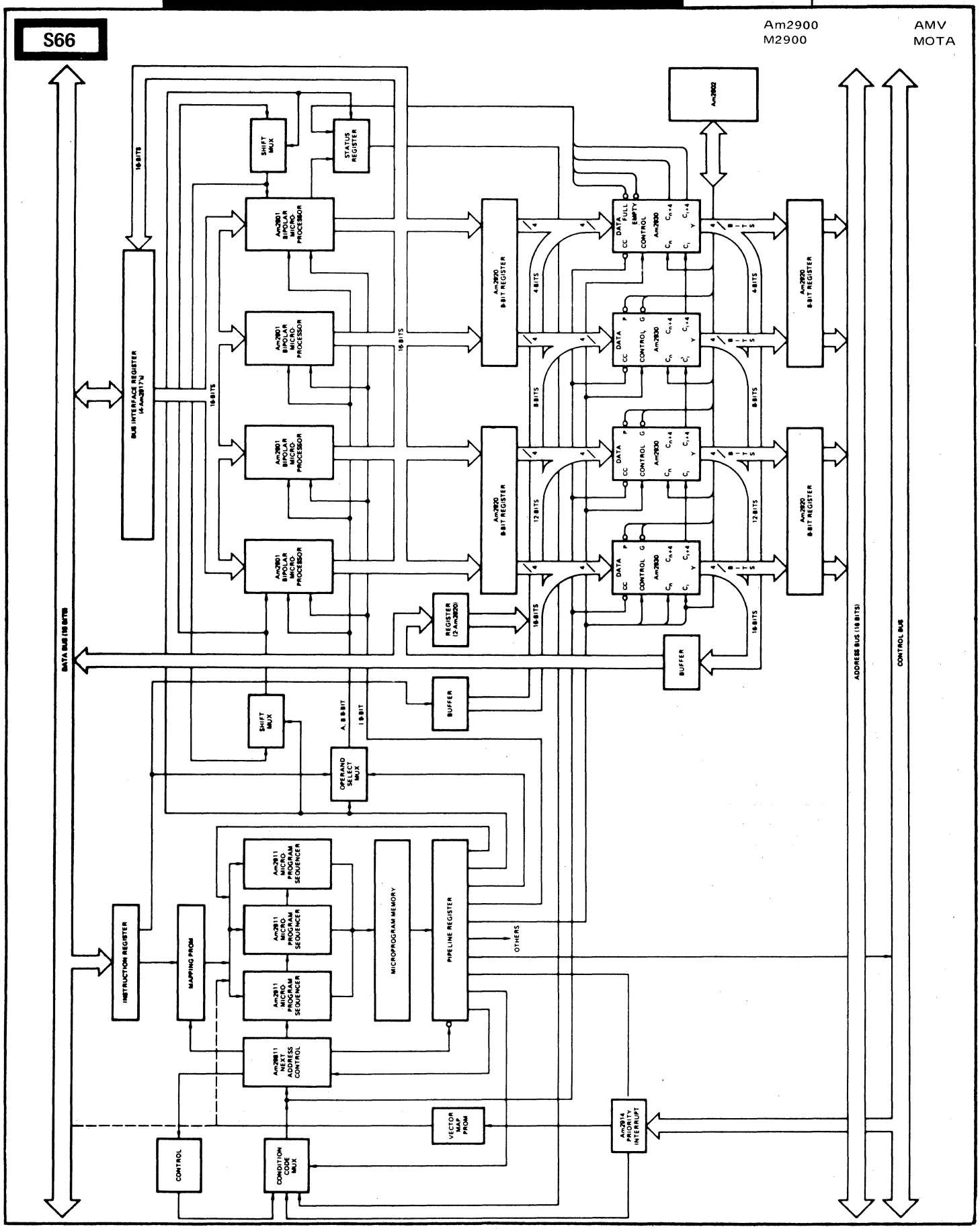
MCS48 ITL



S66

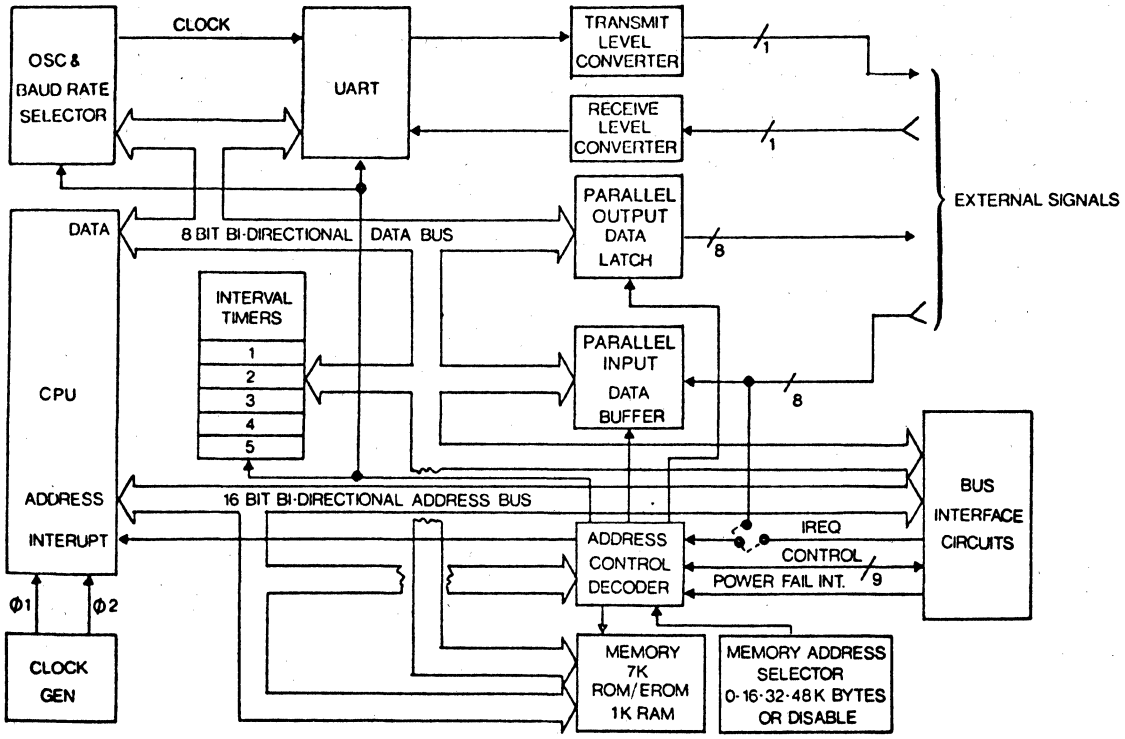
Am2900
M2900

AMV
MOTA



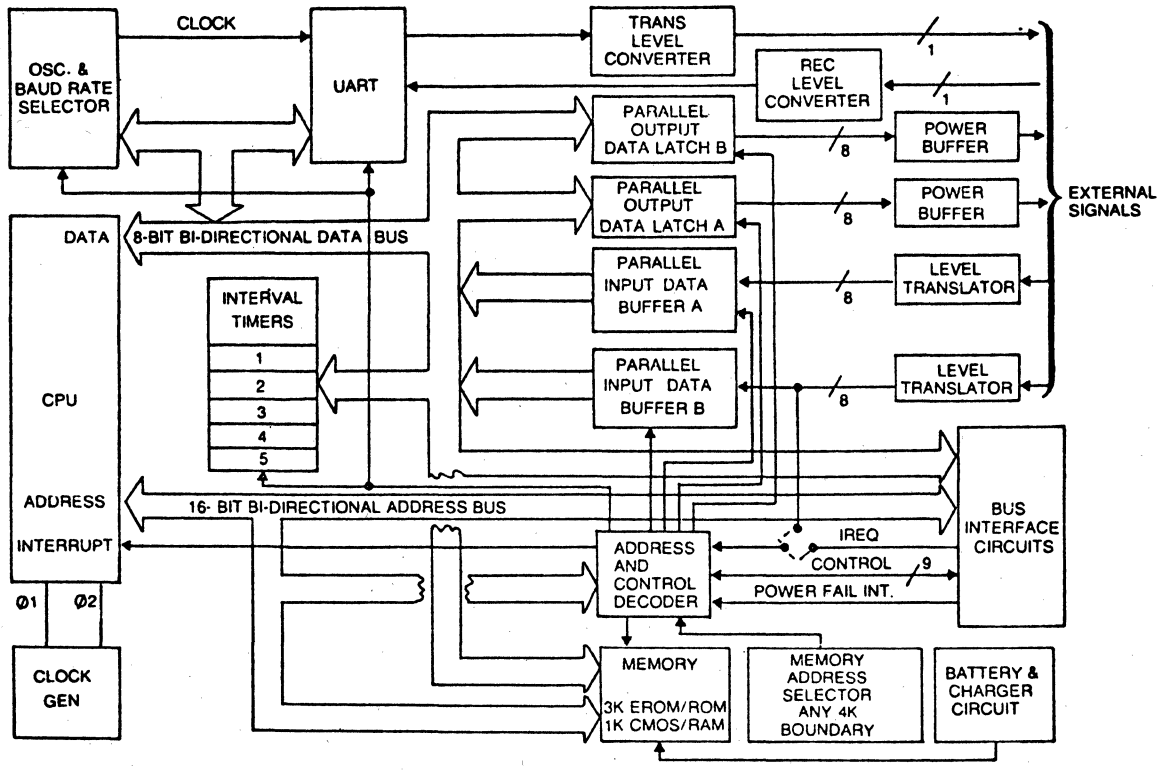
S67

PCS1806 PCS



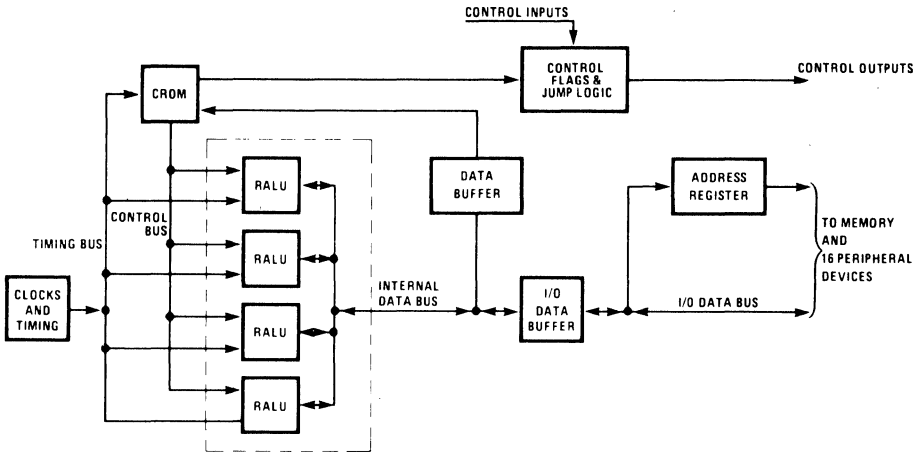
S68

PCS1810 PCS



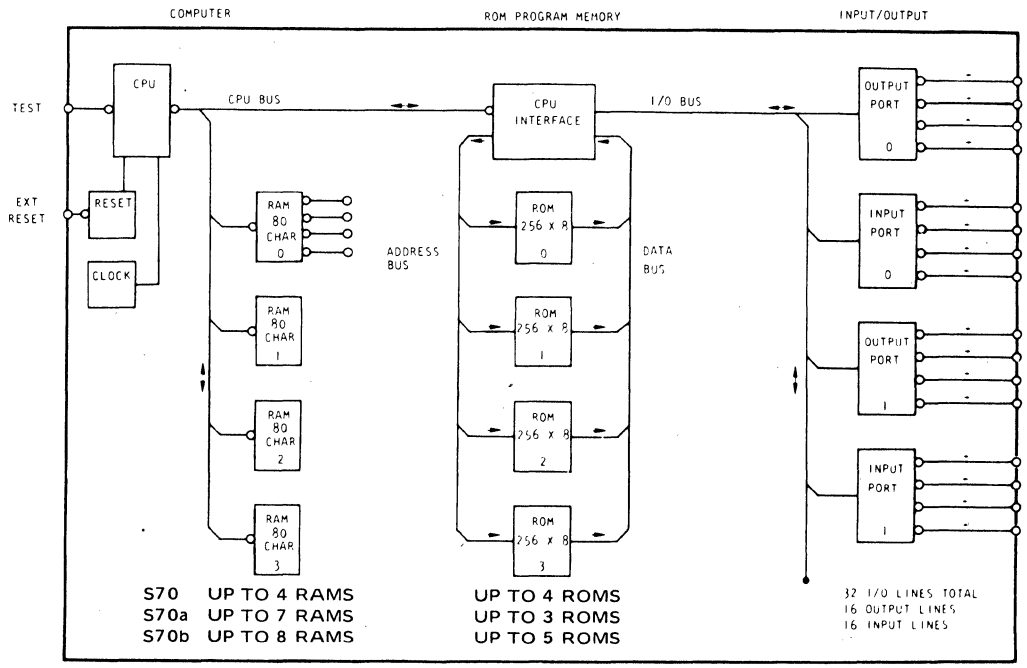
S69

IMP16C NSC



S70

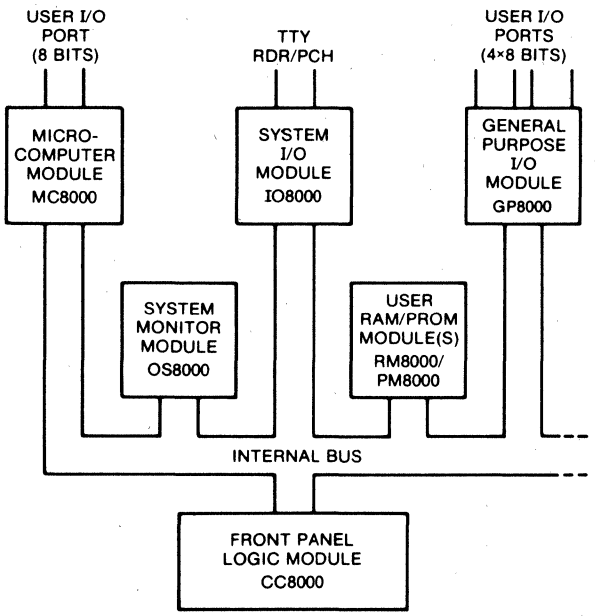
S70 PLS-401 PRO
S70a PLS-411 PRO
S70b PLS-441 PRO



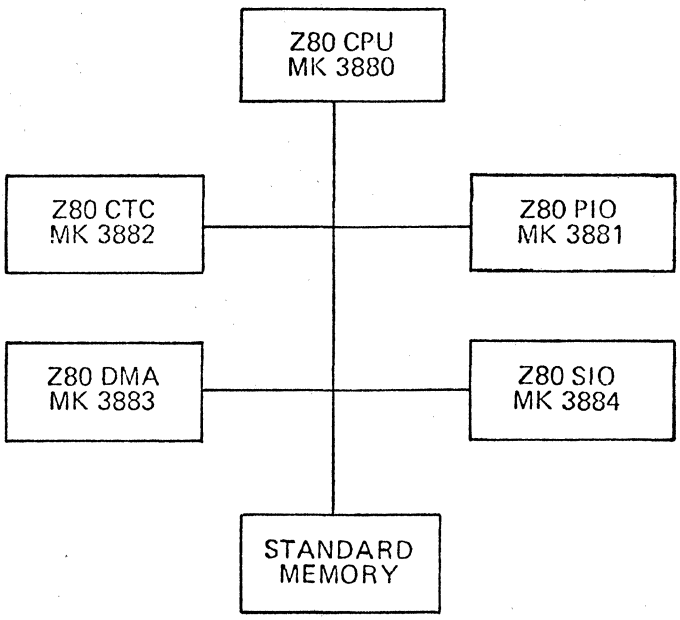
15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

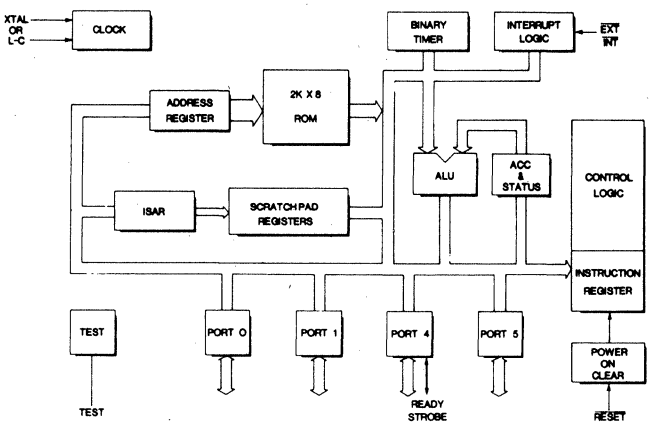
S71 GIC8000 GIC



S72 Z80-MOS MOS

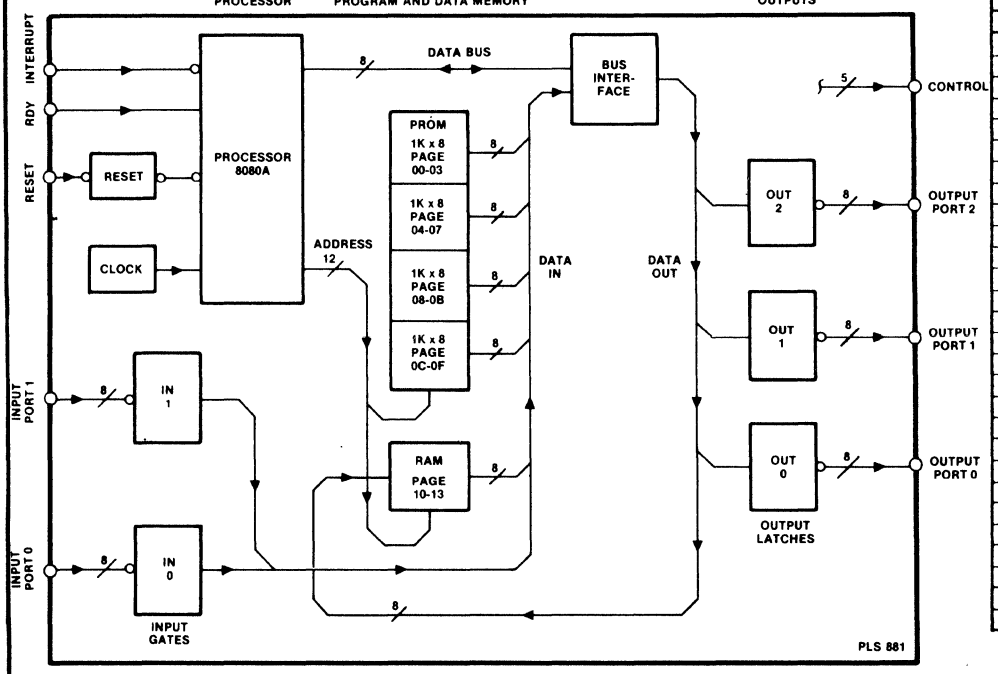


S73 MK3870 MOS
MC3870 MOTA
MK3872 MOS



PLS-881 PRO

S76

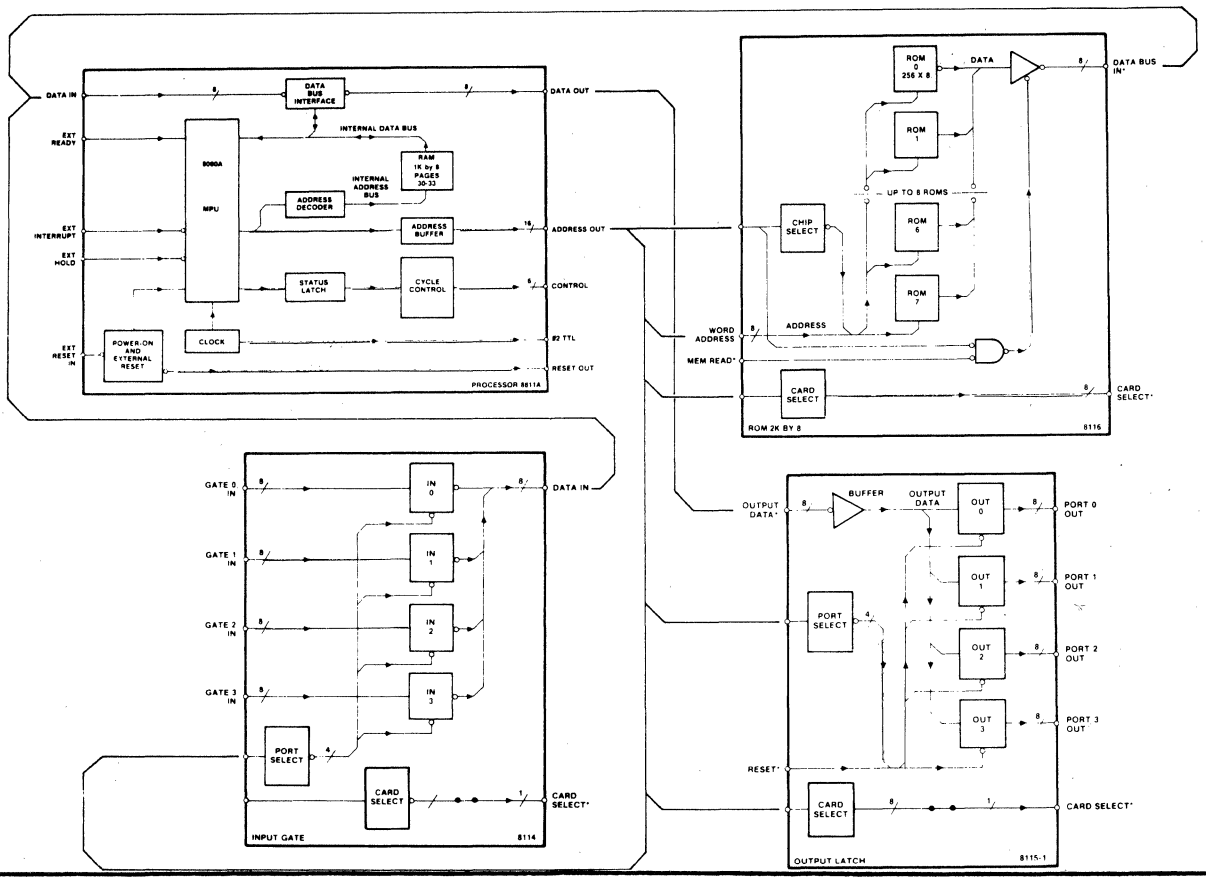


EDGE CONNECTOR PIN LIST					
PIN NUMBER / SIGNAL FLOW / SIGNAL			PIN NUMBER / SIGNAL FLOW / SIGNAL		
+ 5 VOLTS	IN	2	1	IN	+ 5 VOLTS
GROUND	IN	4	3	IN	GROUND
-5 VOLTS	IN	6	5	IN	-5 VOLTS
IN0-5*	IN	8	7	IN	IN1-5*
IN0-6*	IN	10	9	IN	IN1-6*
IN0-7*	IN	12	11	IN	IN1-7*
IN0-8*	IN	14	13	IN	IN1-8*
IN0-4*	IN	16	15	IN	IN1-4*
IN0-3*	IN	18	17	IN	IN1-3*
IN0-2*	IN	20	19	IN	IN1-2*
IN0-1*	IN	22	21	IN	IN1-1*
OUT0-1*	OUT	24	23	OUT	OUT0-5*
OUT0-2*	OUT	26	25	OUT	OUT0-6*
OUT0-3*	OUT	28	27	OUT	OUT0-7*
OUT0-4*	OUT	30	29	OUT	OUT0-8*
OUT1-1*	OUT	32	31	OUT	OUT1-5*
OUT1-2*	OUT	34	33	OUT	OUT1-6*
OUT1-3*	OUT	36	35	OUT	OUT1-7*
OUT1-4*	OUT	38	37	OUT	OUT1-8*
OUT2-1*	OUT	40	39	OUT	OUT2-5*
OUT2-2*	OUT	42	41	OUT	OUT2-6*
OUT2-3*	OUT	44	43	OUT	OUT2-7*
OUT2-4*	OUT	46	45	OUT	OUT2-8*
INTA*	OUT	48	47	IN	IREQ*
WAIT*	OUT	50	49	IN	RDY
(SPARE) RST	OUT	52	51	OUT	OSC
RESET*	IN	54	53	OUT	RST*
+ 12 VOLTS	IN	56	55	IN	+ 12 VOLTS

*Designates Active Low Level Logic

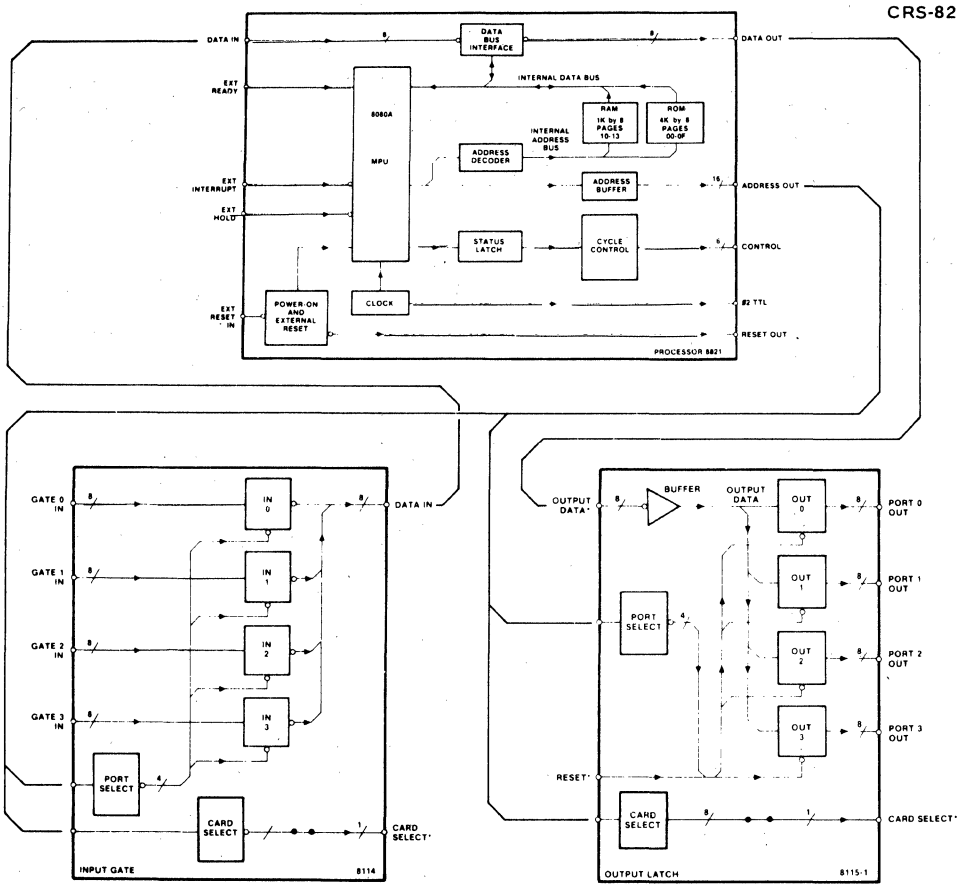
CRS-81 PRO

S77



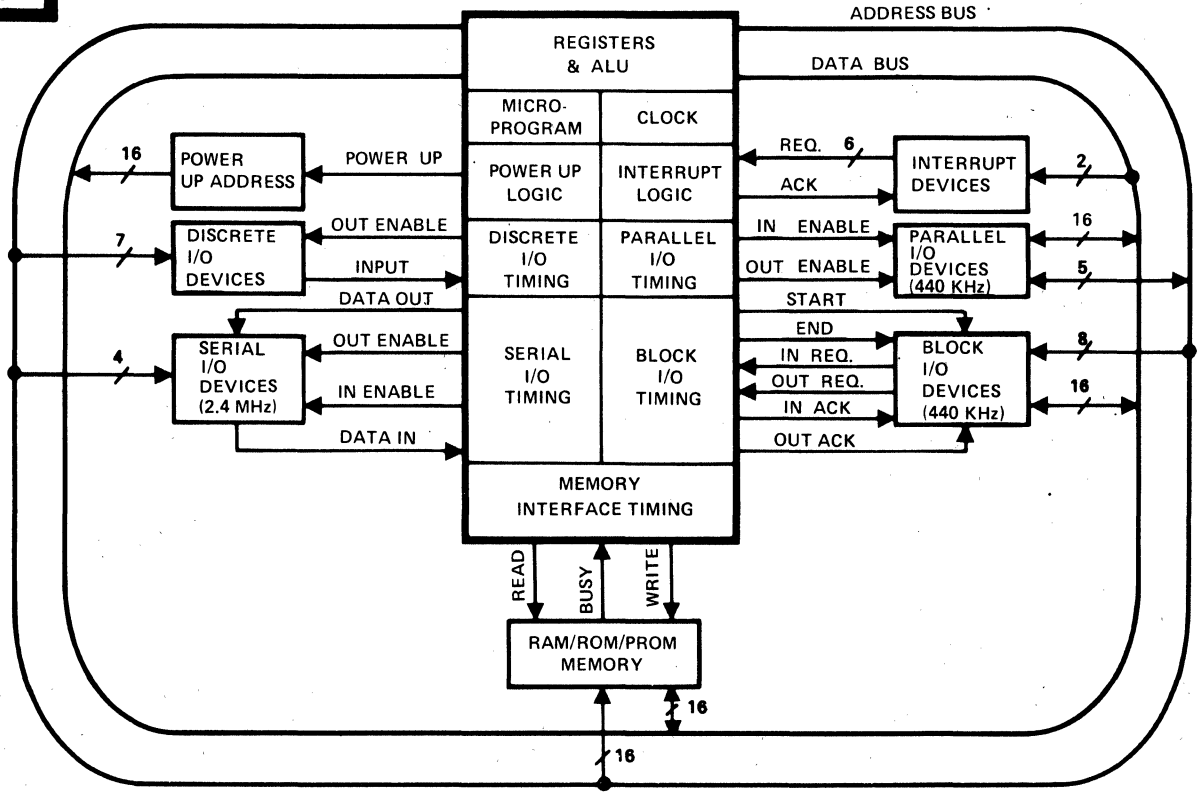
S78

CRS-82 PRO



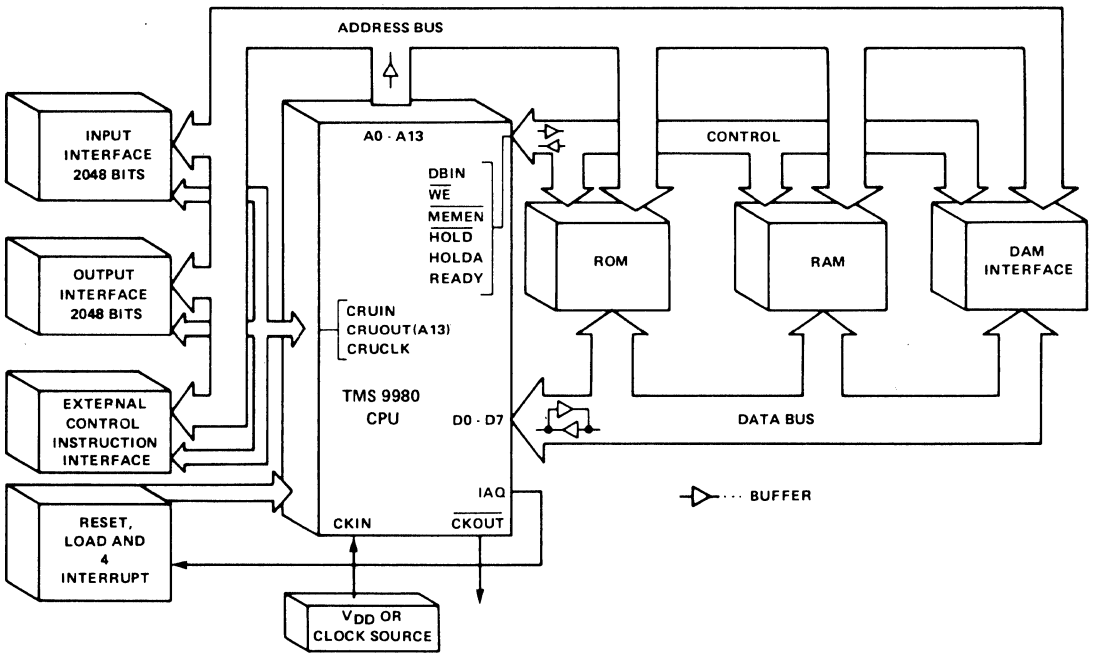
S79

AN/UYK-30 HACC



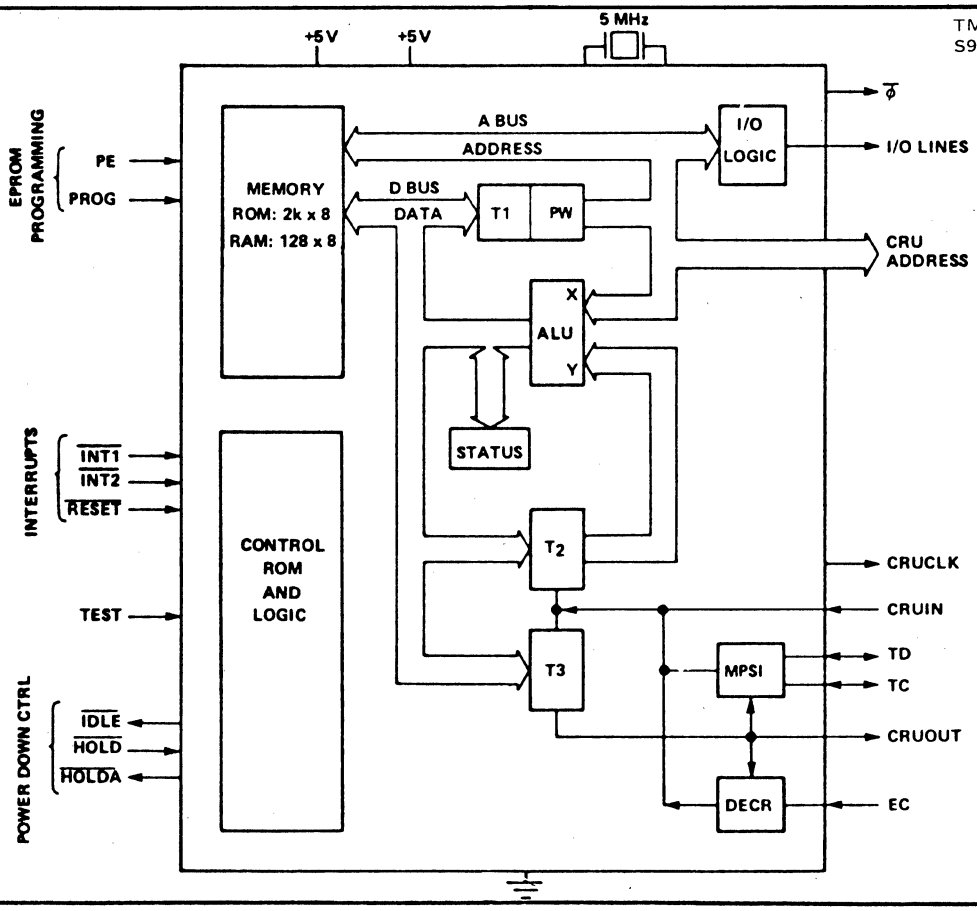
S80

TMS9980 TII
S9980 AMI



S81

TMS9940 TII
S9940 AMI

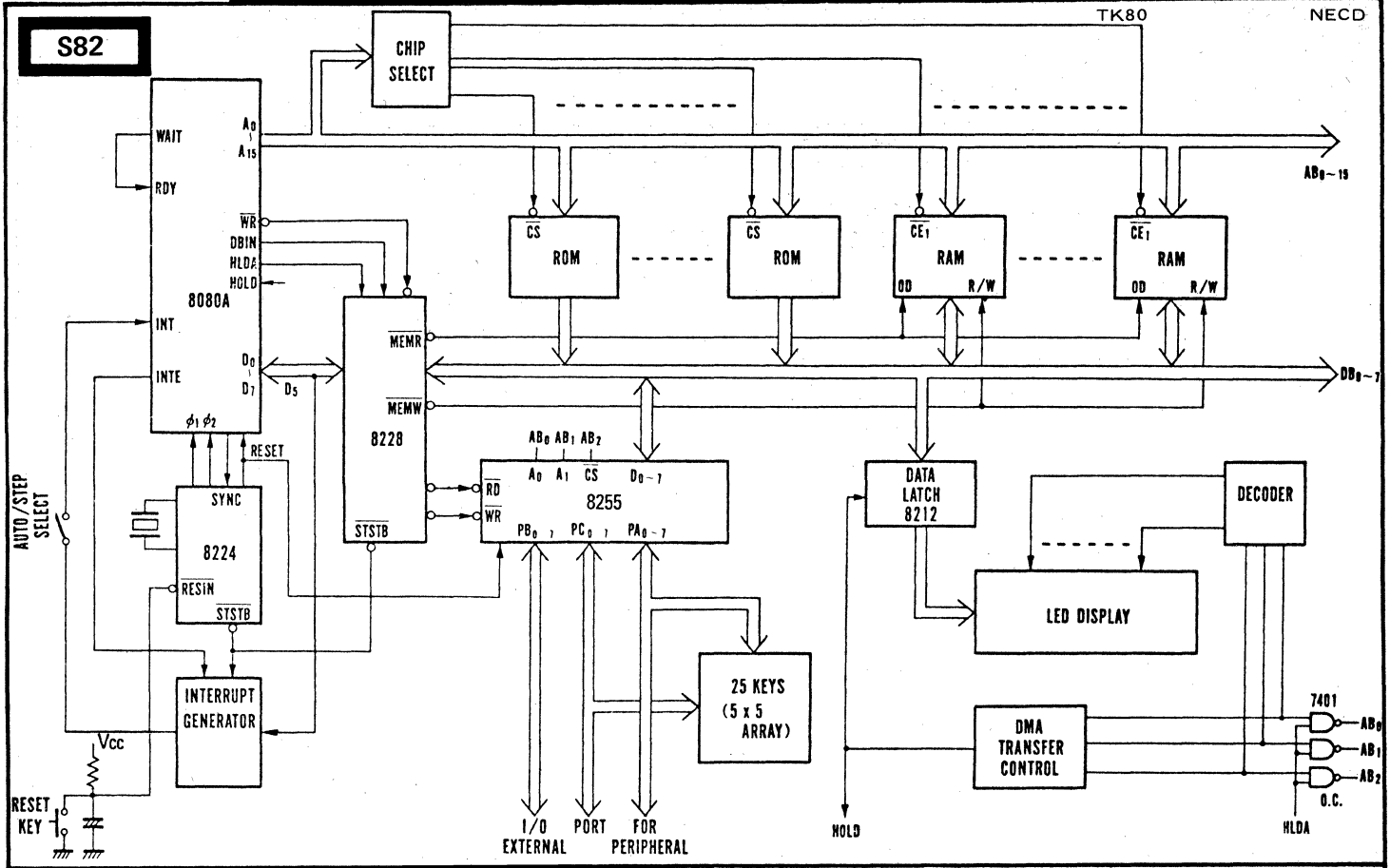


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

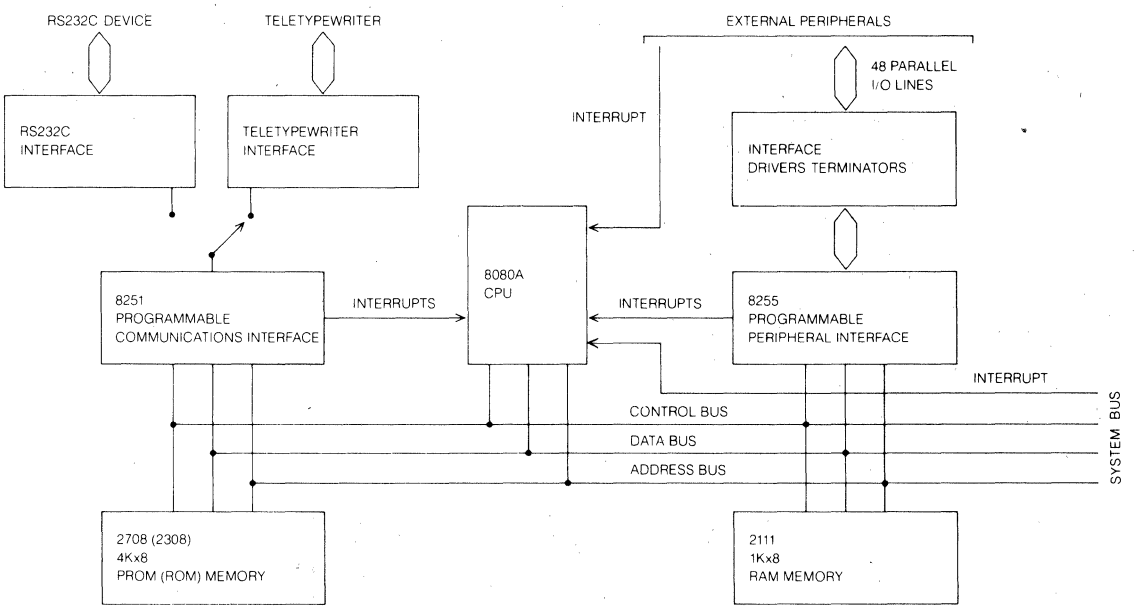
S82

TK80 NECD



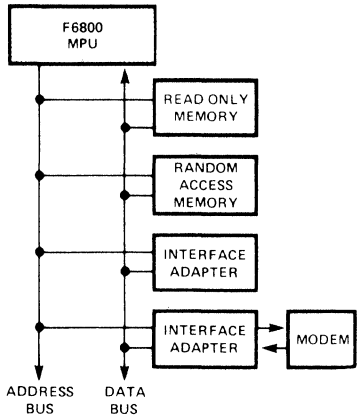
S83

BLC80/10 NSC



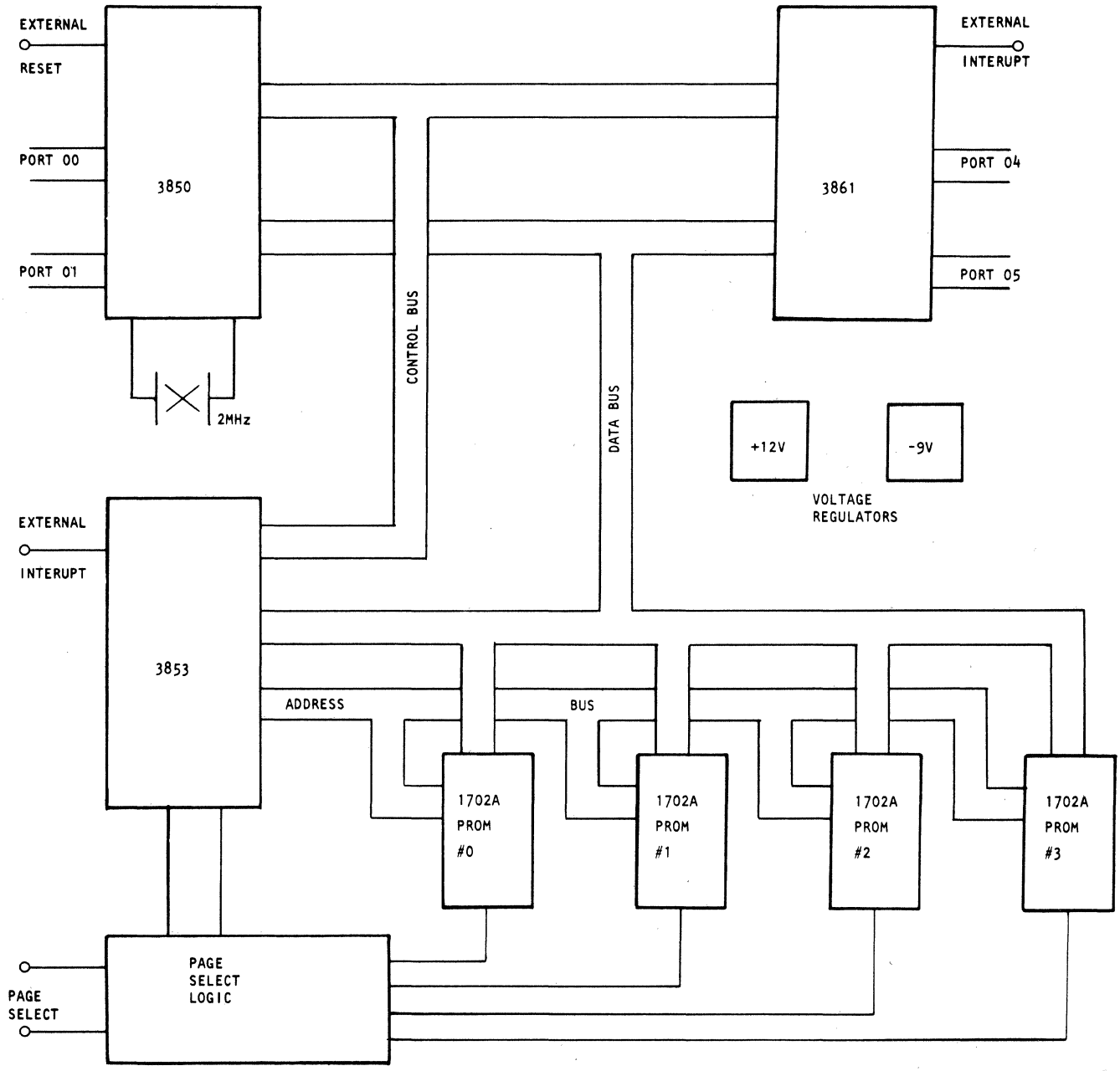
S84

F6800 FSC



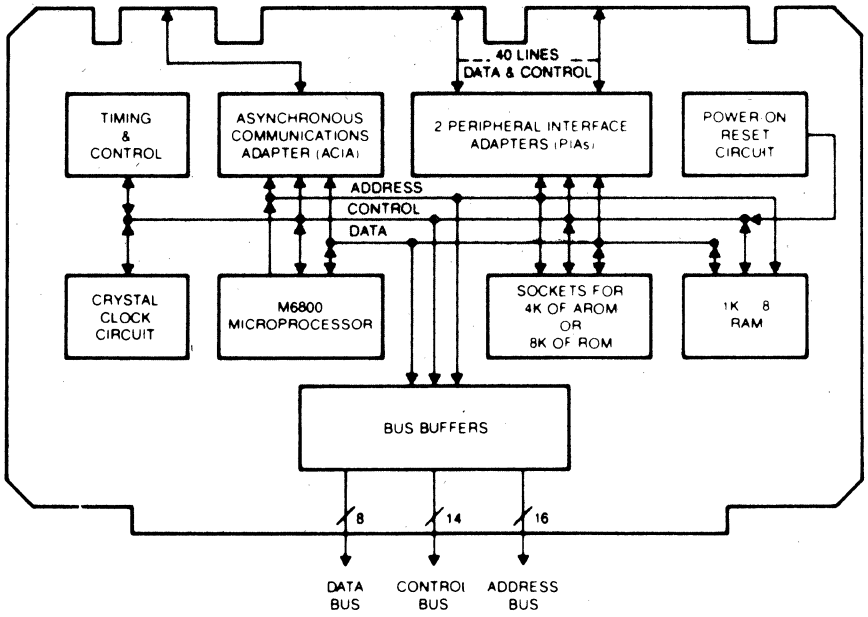
S86

7808 OEI



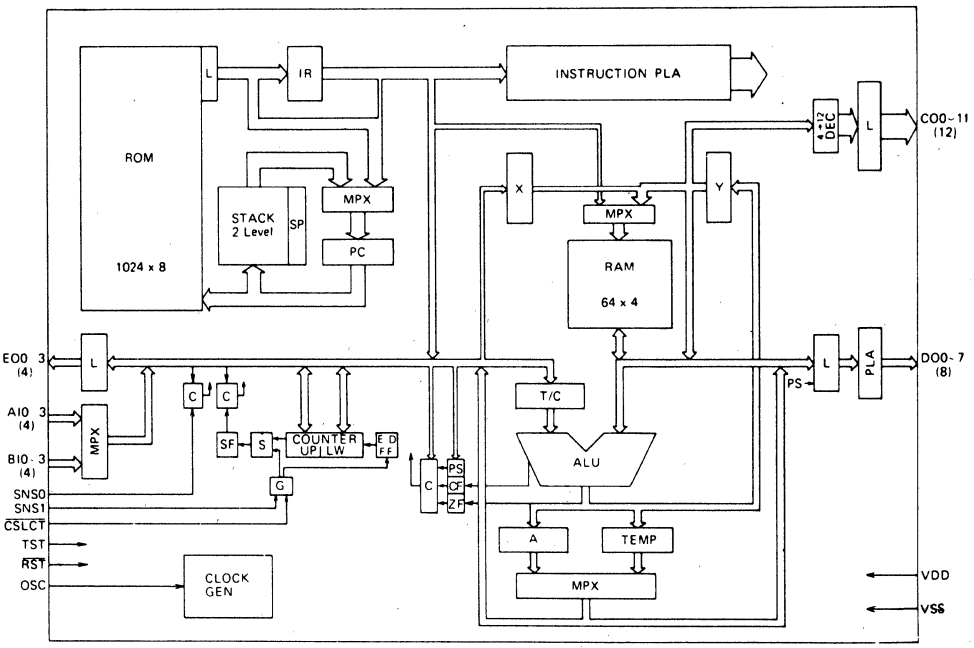
S87

M68MM01 MOTA



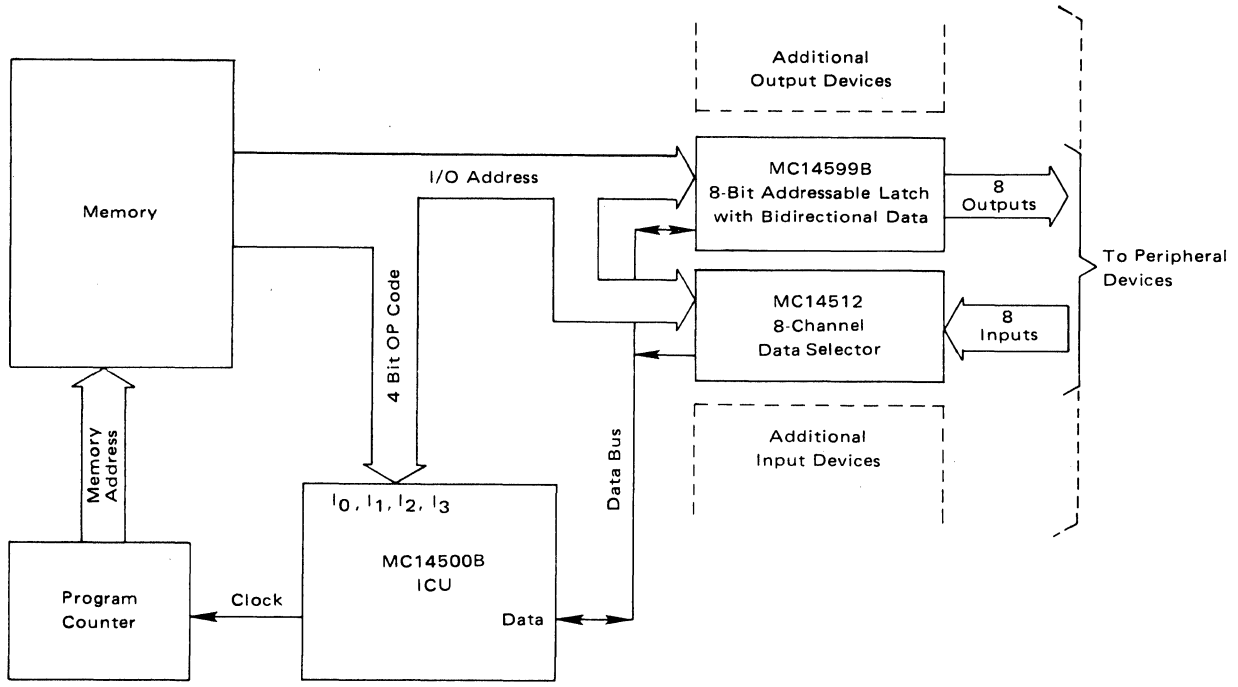
S88

MN1400 MATJ
MN1430 MATJ
MN1450 MATJ



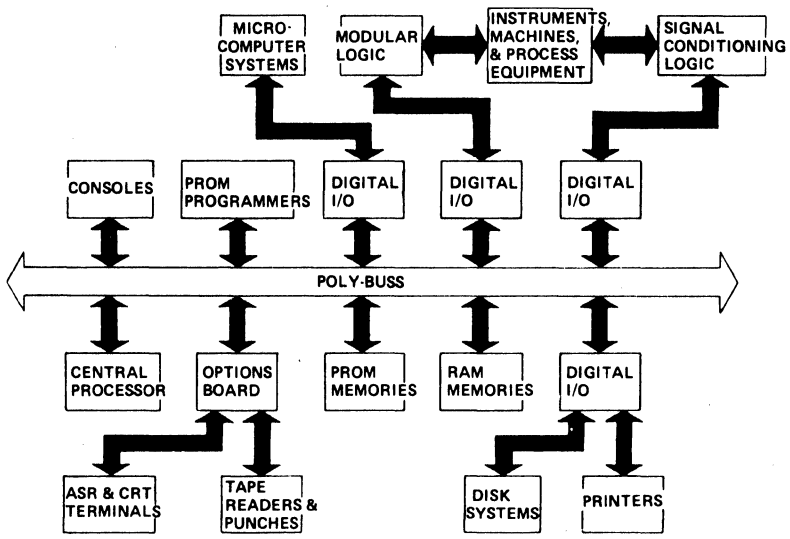
S89

MC14500B MOTA



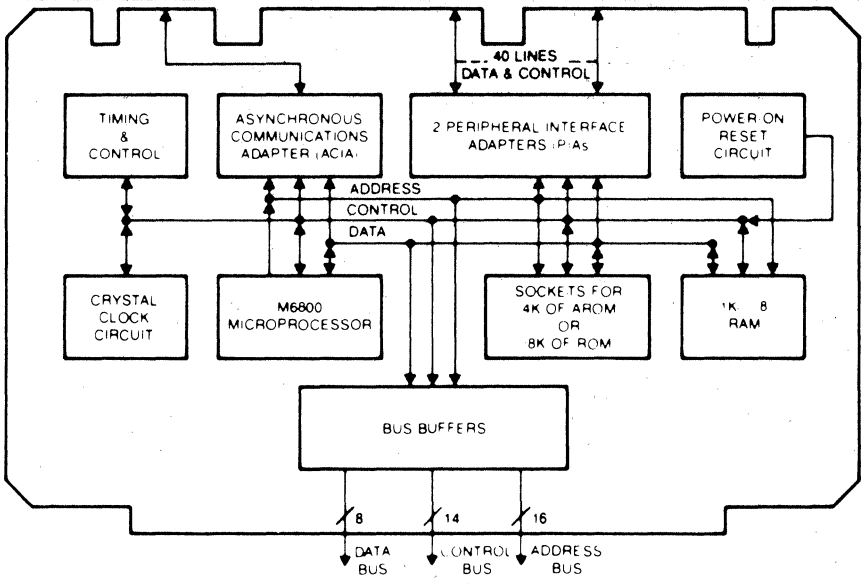
S90

MM1 SYSTEM CLI



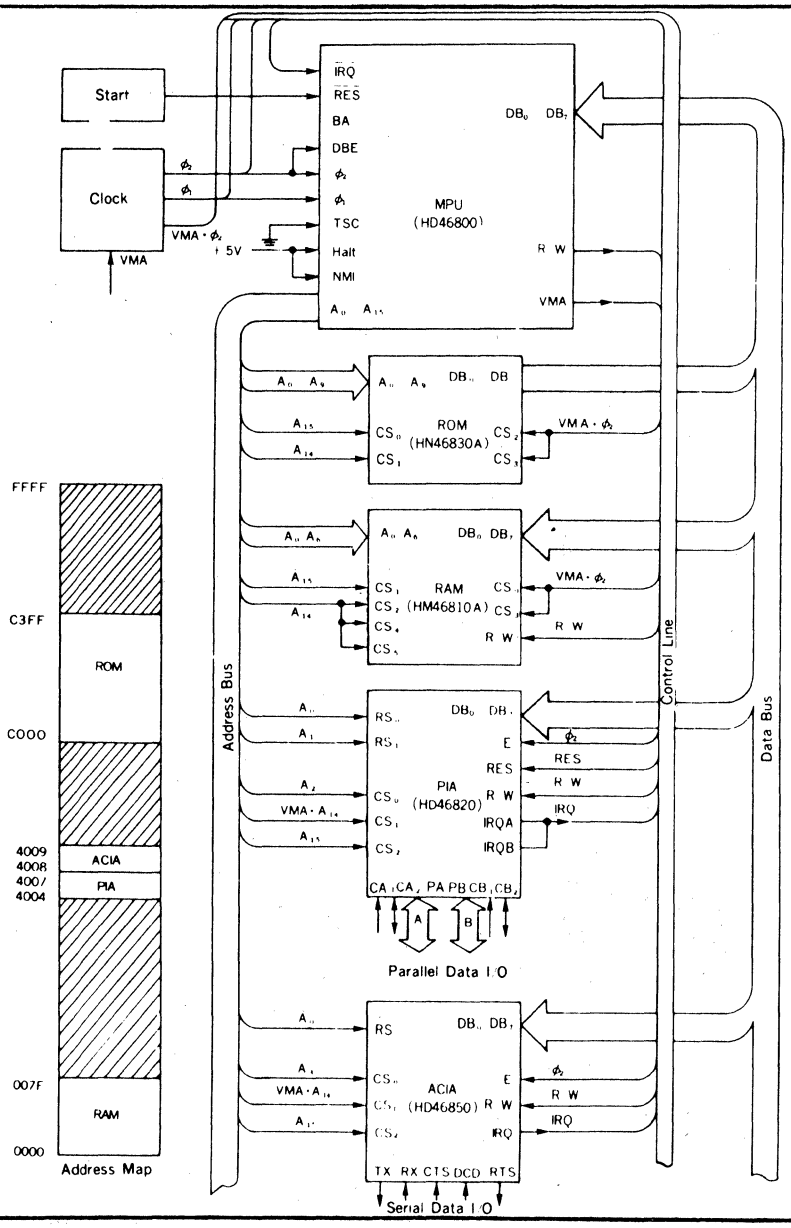
S91

M68MM01A MOTA



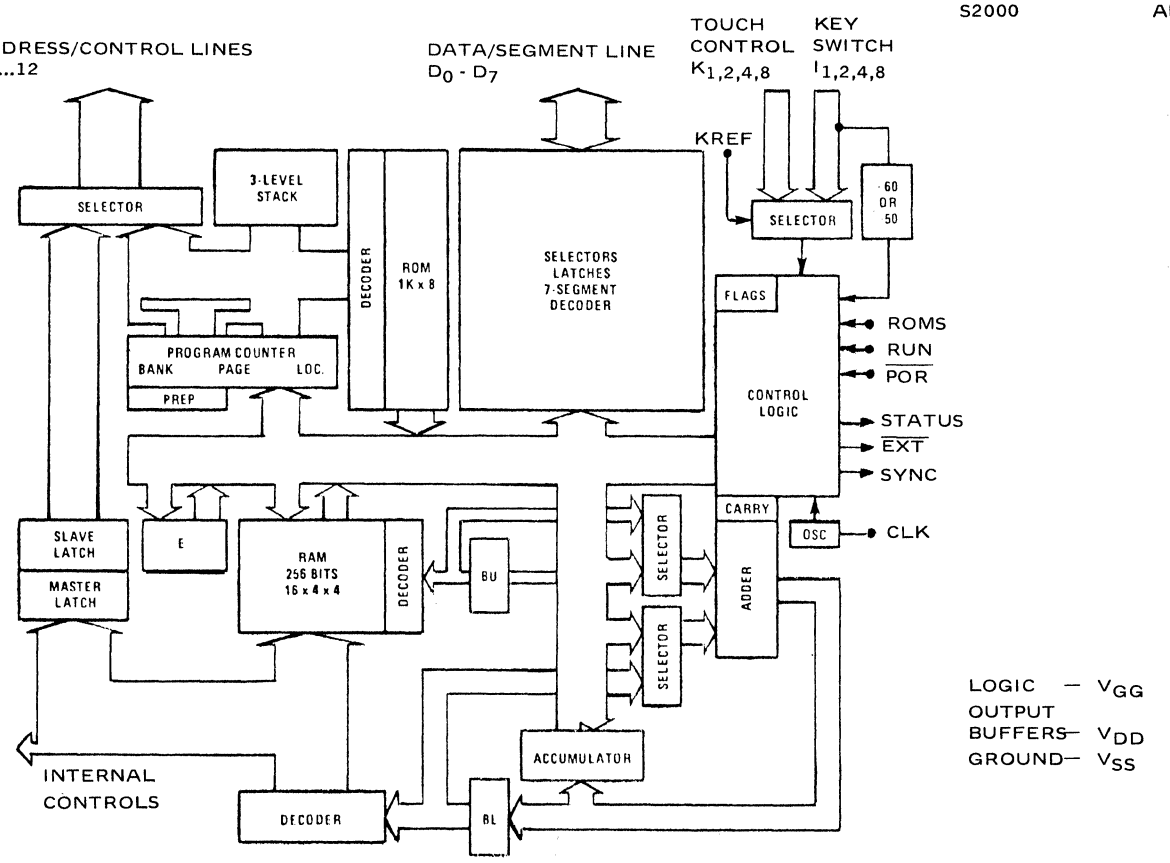
S92

HMCS 6800 HITJ



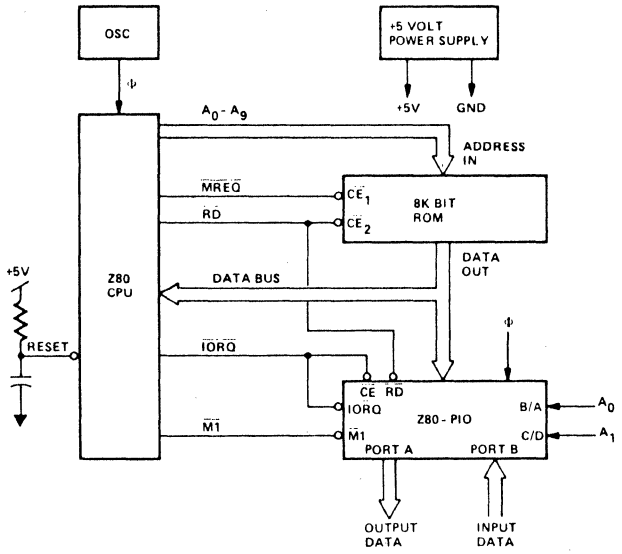
S93

S2000 AMI



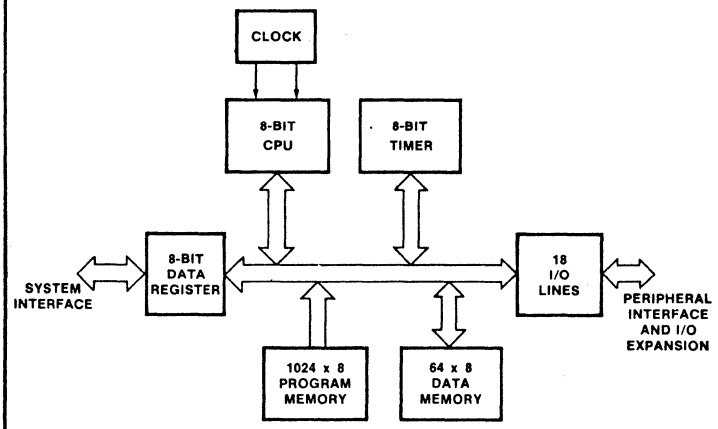
S96

MSC8001-Z80 MSCC



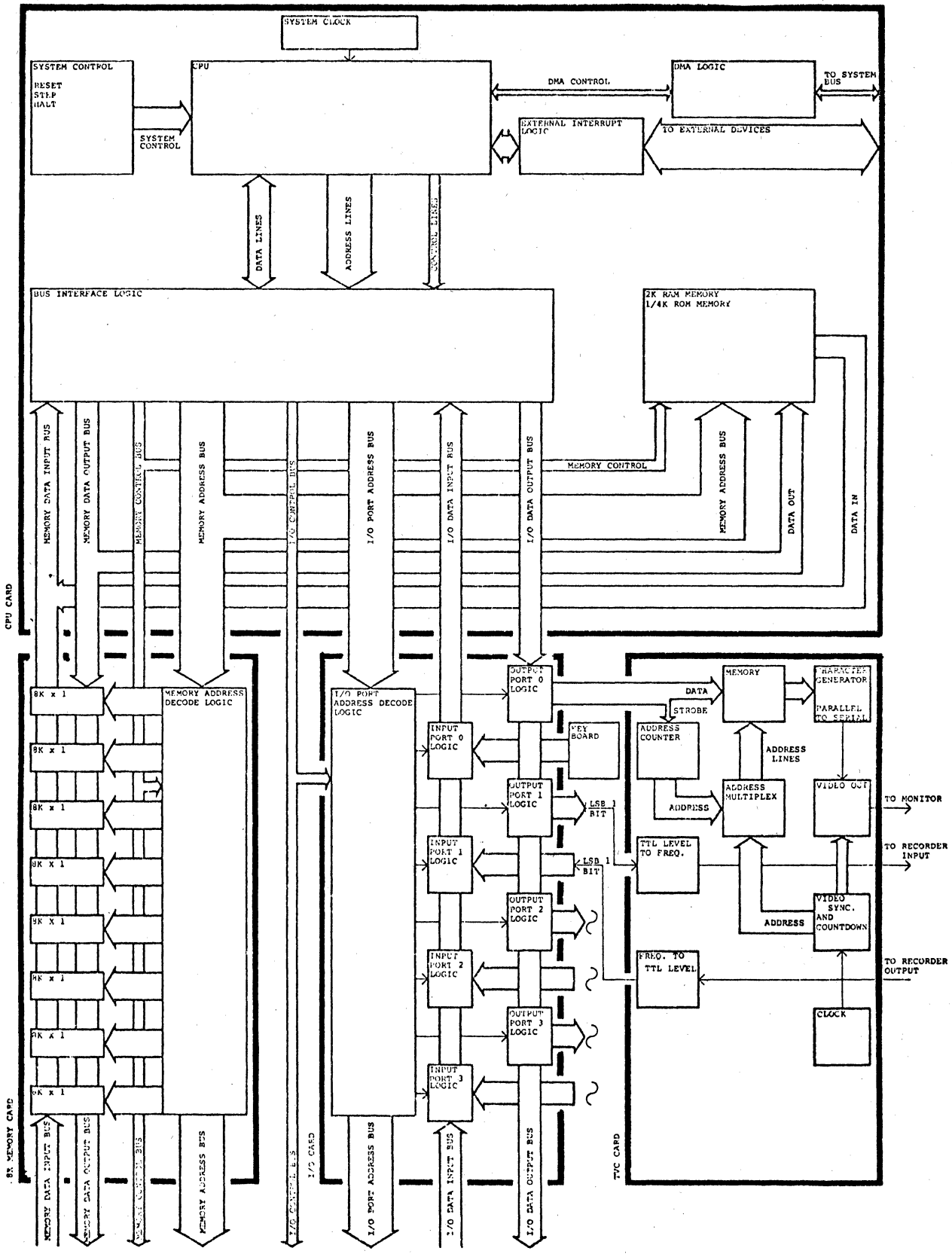
S97

UPI41 ITL



S98

TDGZ80SYS1 DIG
TDGZ80SYS2 DIG

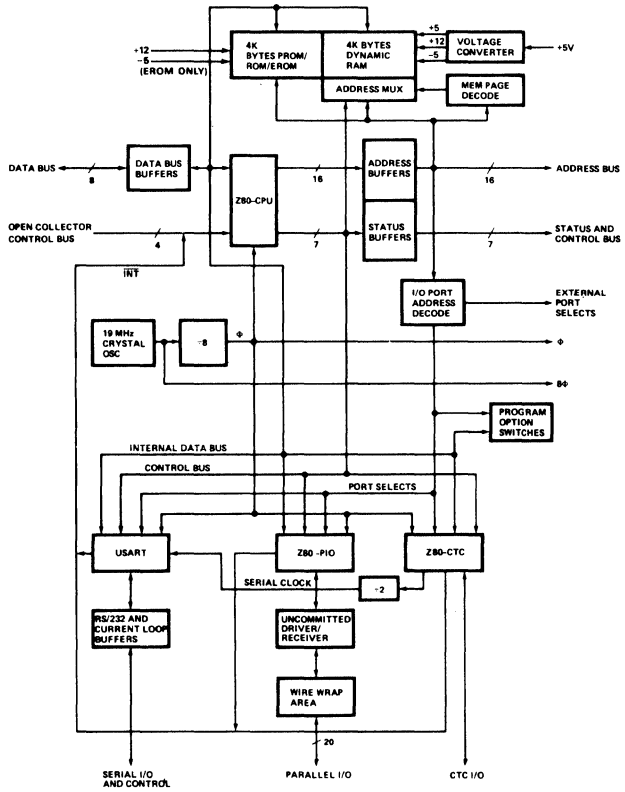


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

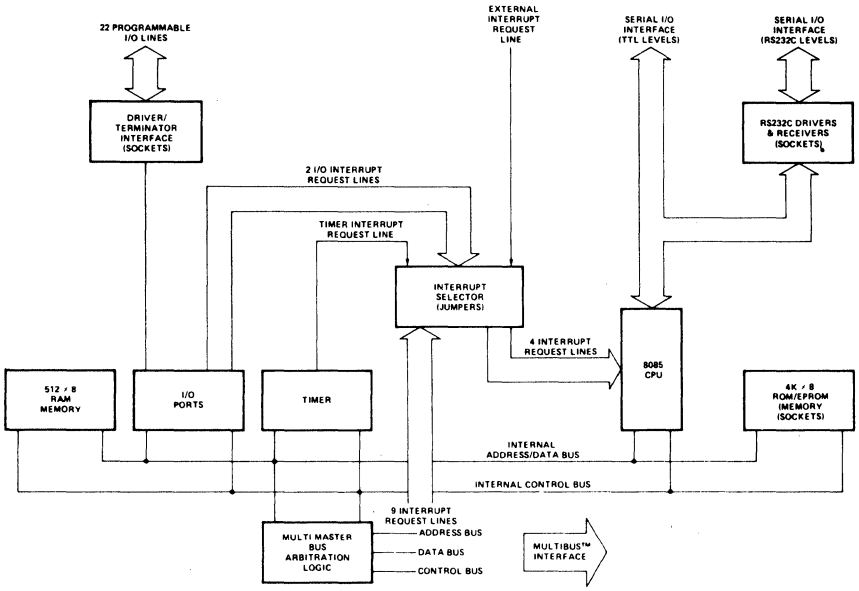
S99

Z80-MCB ZIL



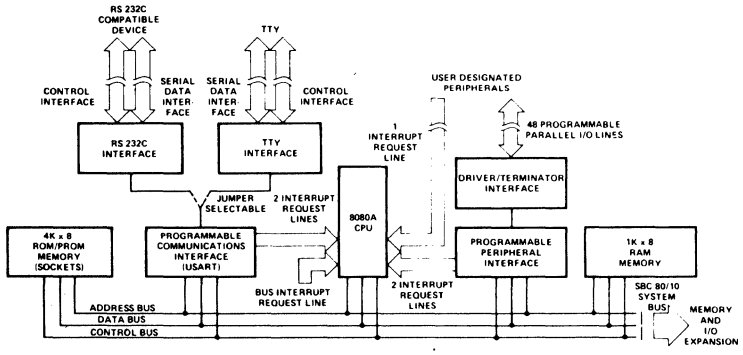
S100

SBC80/05 ITL



S101

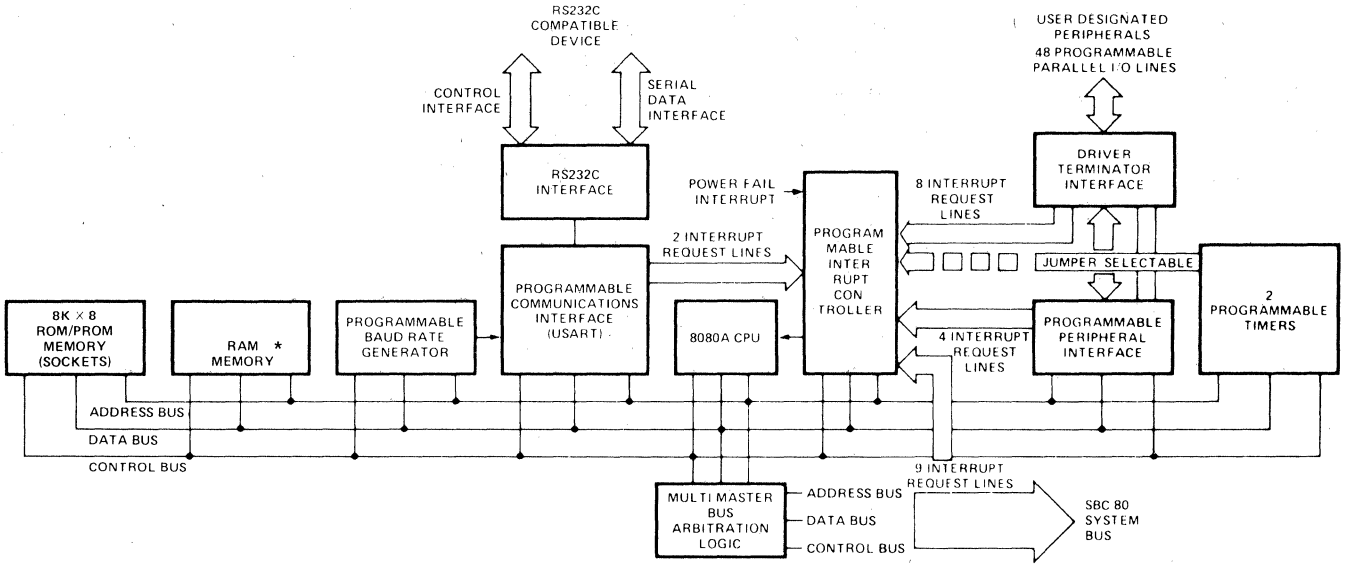
SBC80/10 ITL



1. Interrupts originating from the Programmable Communications Interface and Programmable Peripheral Interface are jumper selectable.

S102

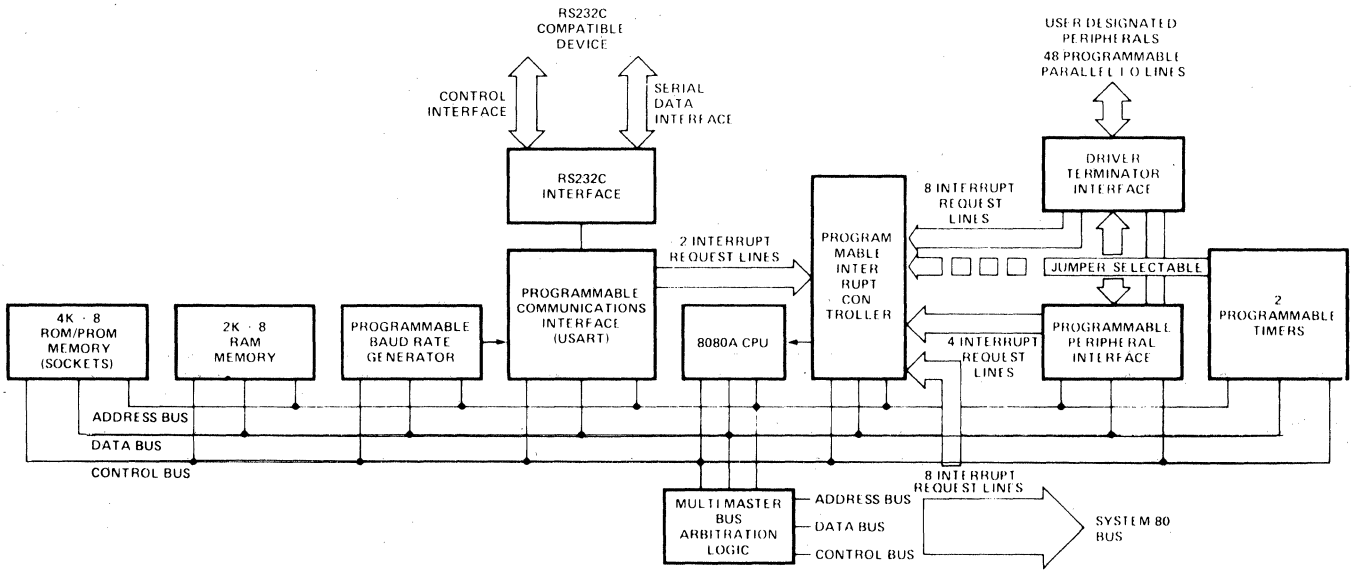
S102 SBC80/20 ITL
SBC80/20-4 ITL



* S102 - 2KX8 RAM
S102a - 4KX8 RAM

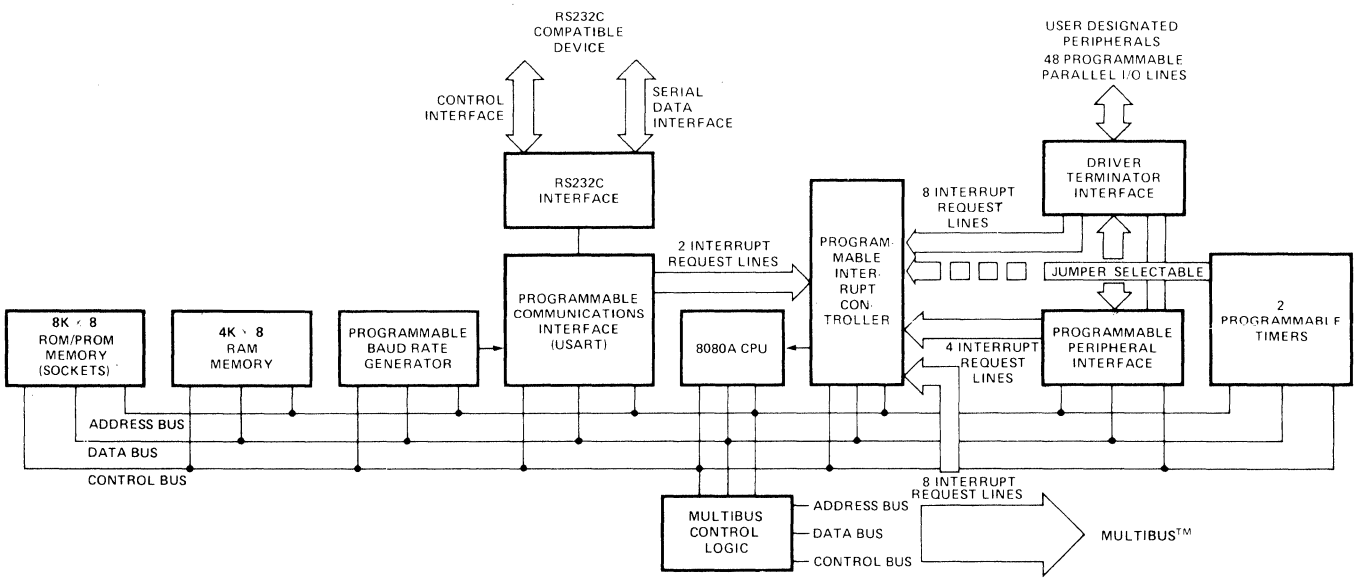
S103

SYSTEM 80/20 ITL



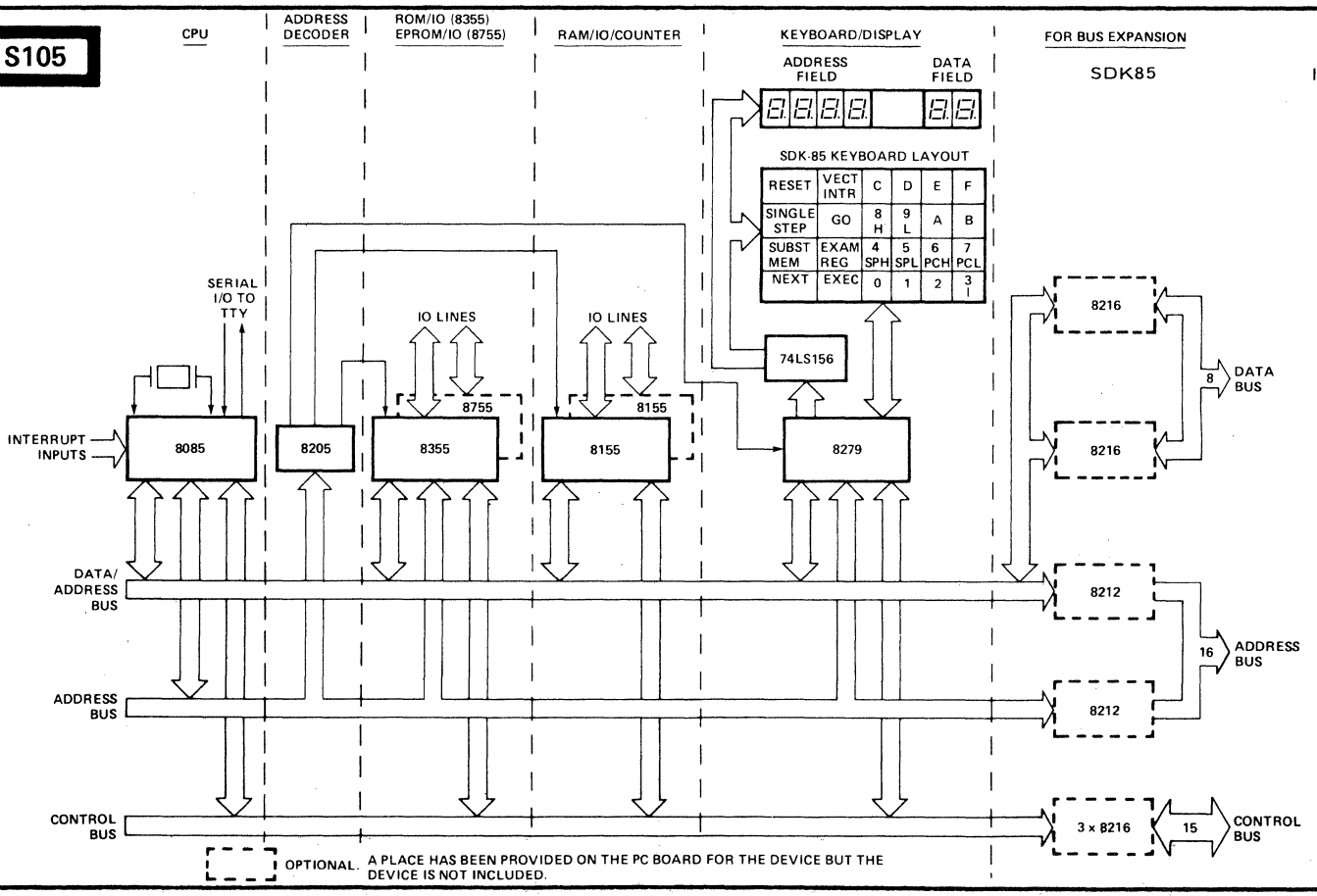
S104

SYSTEM 80/20-4 ITL



S105

ITL

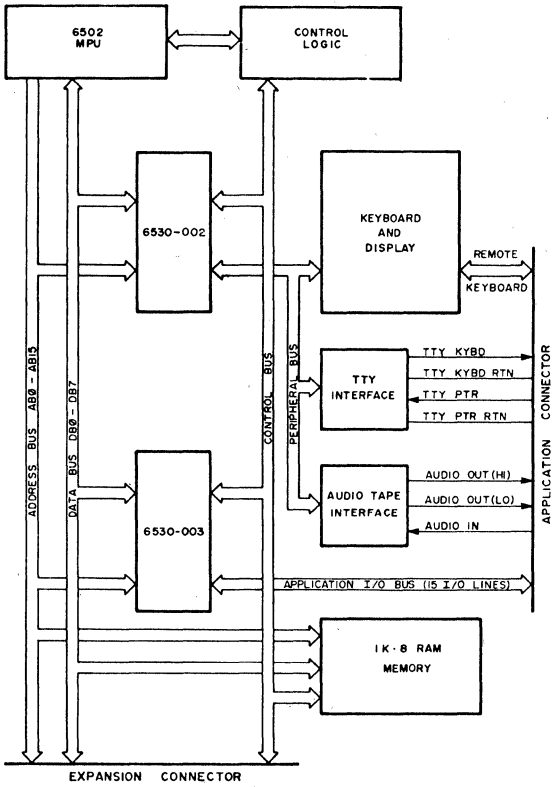


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

S106

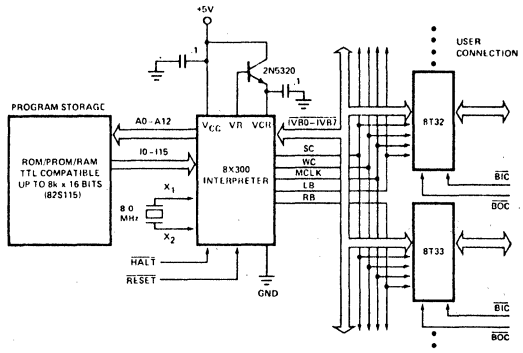
KIM-1 MTY



S107

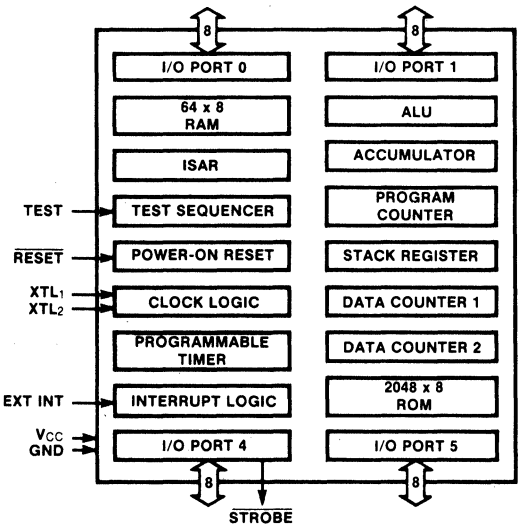
N8X300 SIC

TYPICAL SYSTEM CONFIGURATION



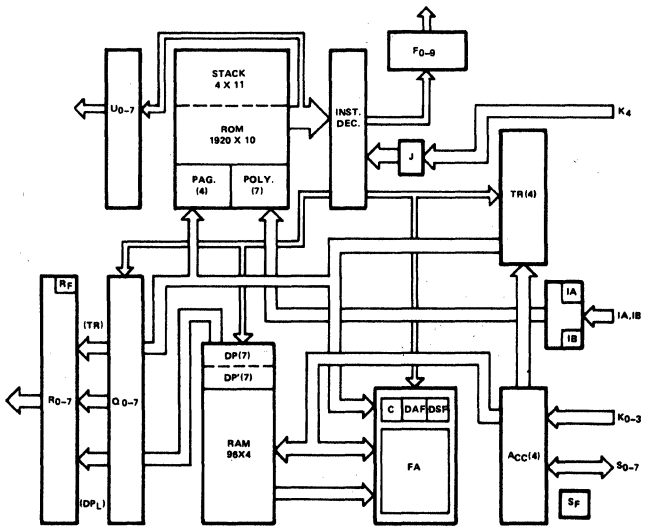
S108

F3870 FSC



S109

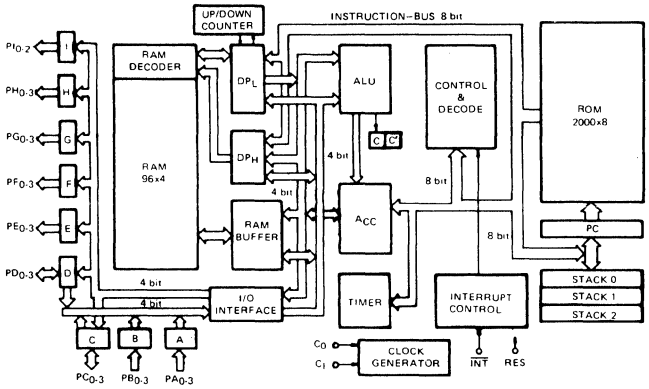
uCOM-42 NECJ



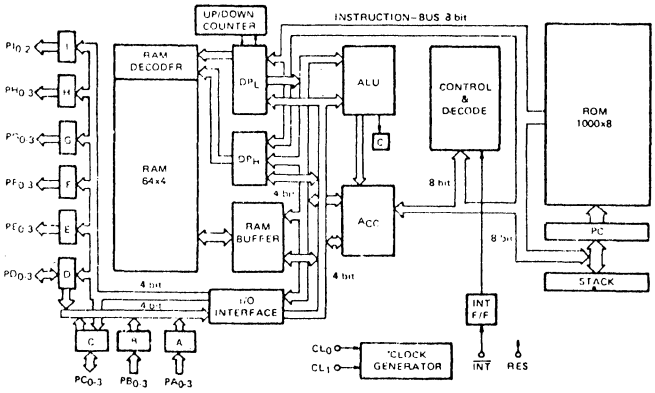
15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

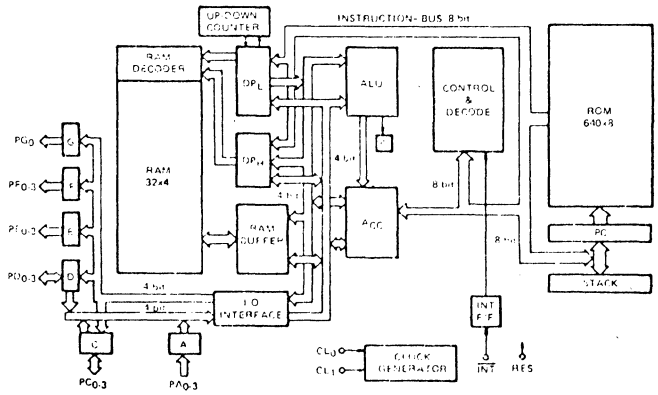
S110 μCOM-43c NECJ



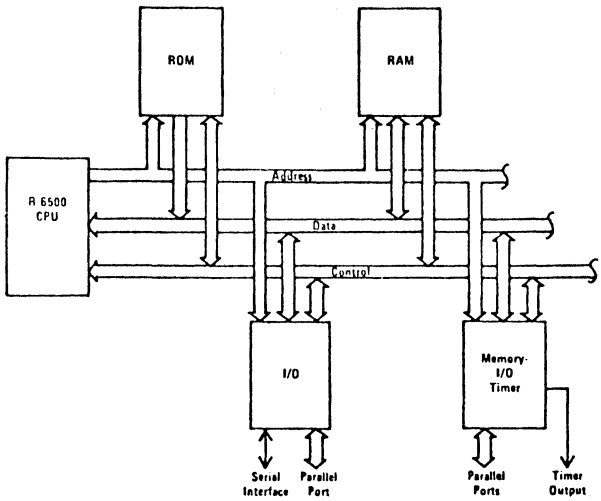
S111 μ COM-44c NECJ



S112 μCOM-45c NECM



S113 R6500 RKW

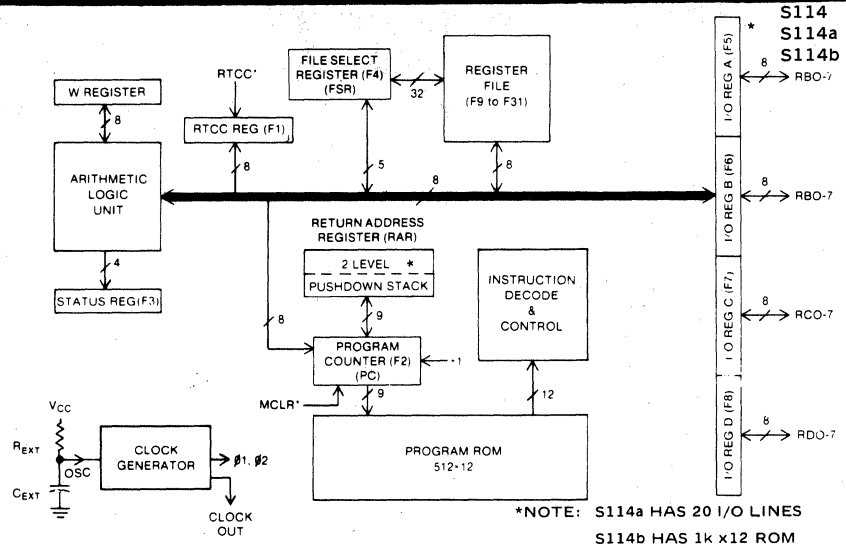


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

S114

S114 PIC1650 GIC
S114a PIC1655 GIC
S114b PIC1670 GIC

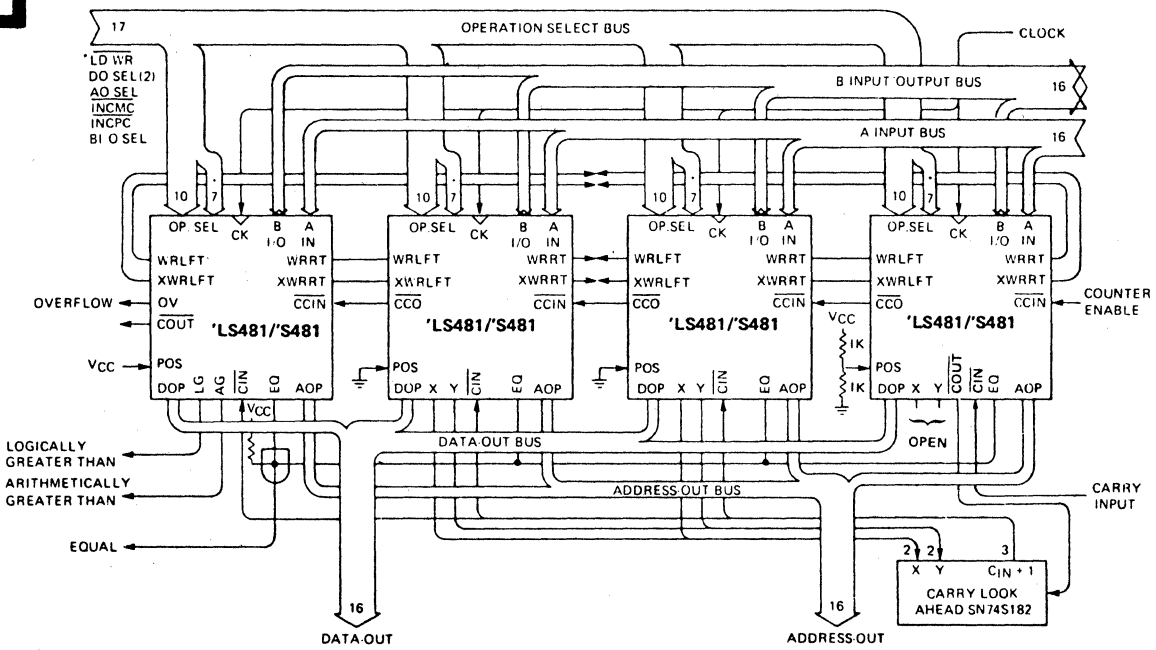


*NOTE: S114a HAS 20 I/O LINES
S114b HAS 1k x12 ROM AND 4-LEVEL STACK

S115

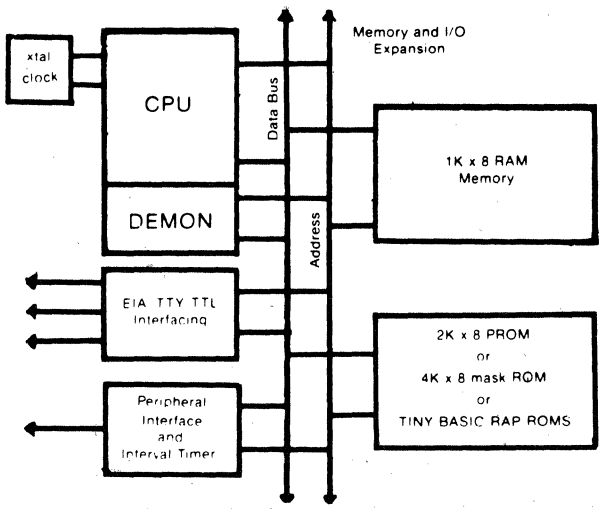
S481 TII
LS481 TII

TYPICAL 16-BIT PROCESSOR



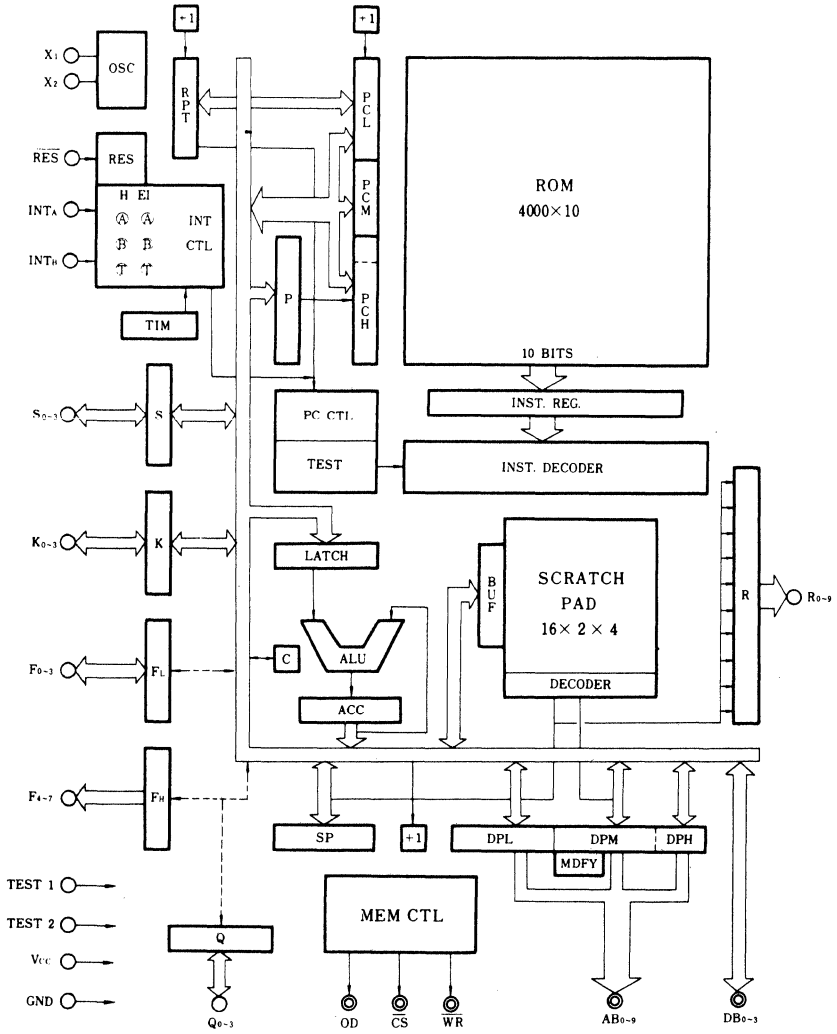
S116

SUPERJOLT MCA



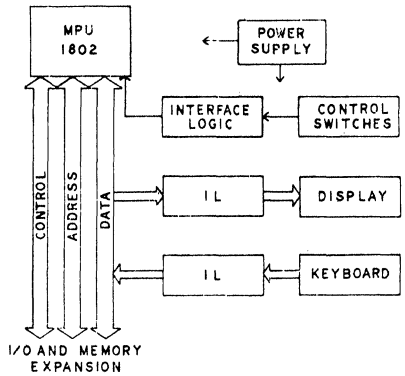
S117

uCOM-47 NECJ



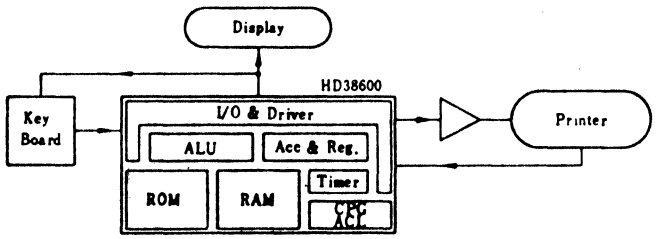
S119

UC1800 INF



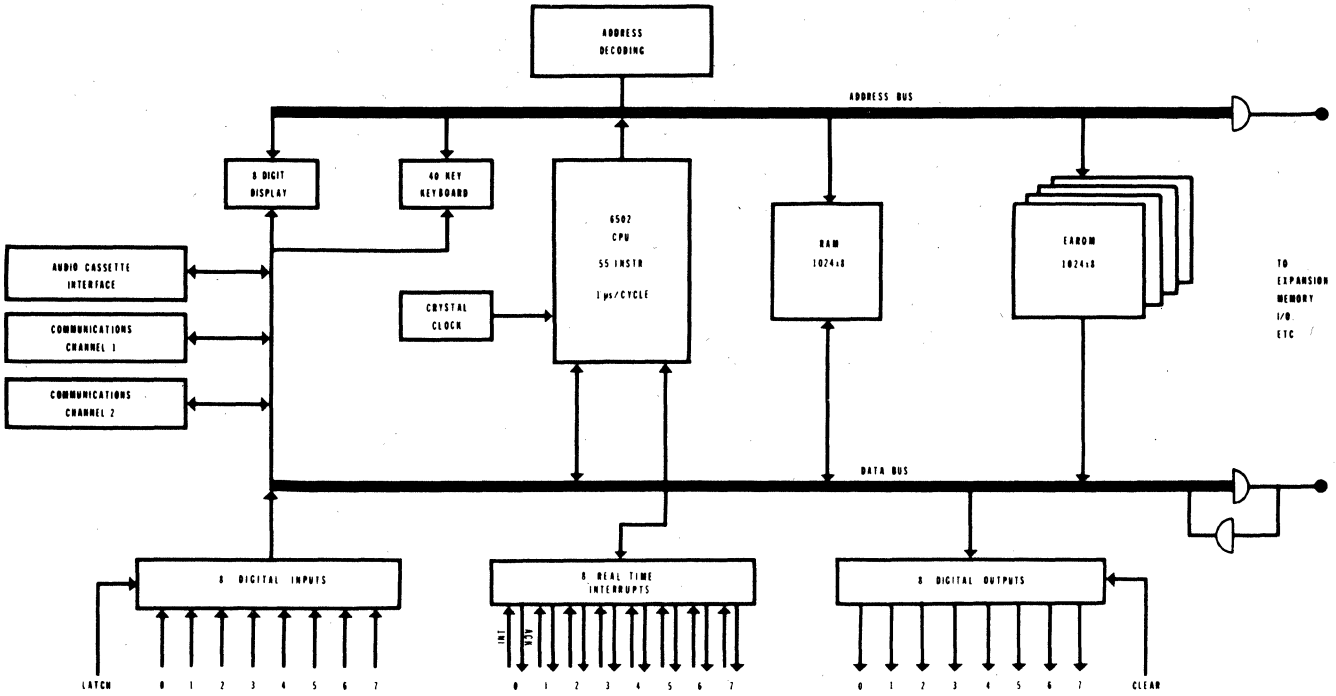
S120

HMCS45 HITJ

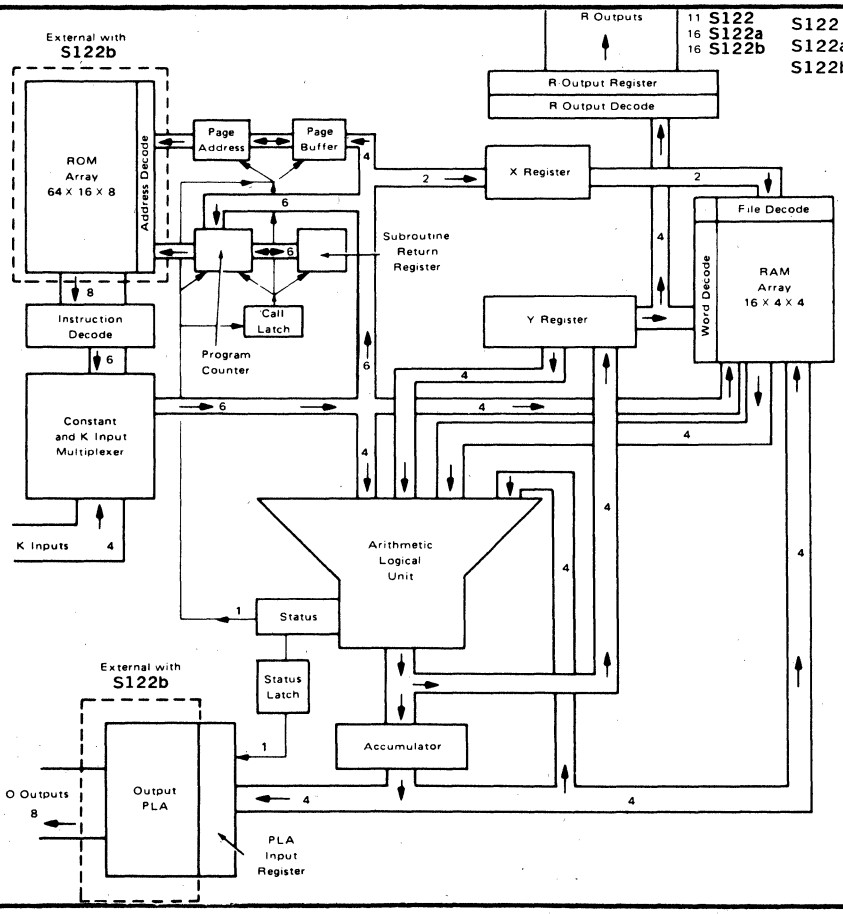


ETC1000 ETL

S121



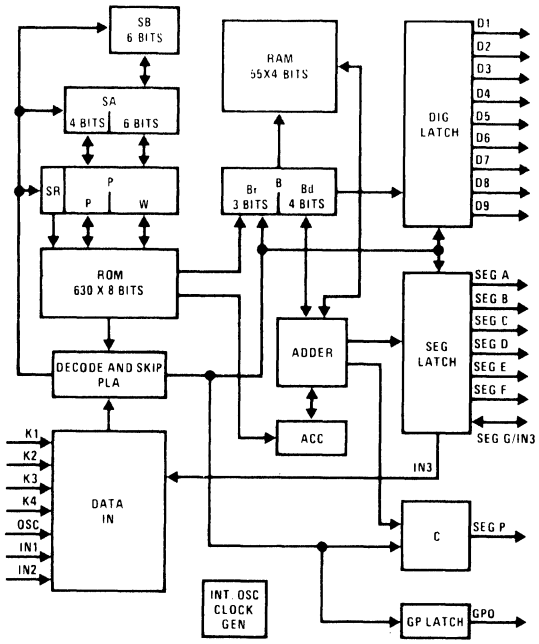
S122



11 S122	S122	MC141000	MOTA
16 S122a	S122a	MC141200	MOTA
16 S122b	S122b	MC141099	MOTA

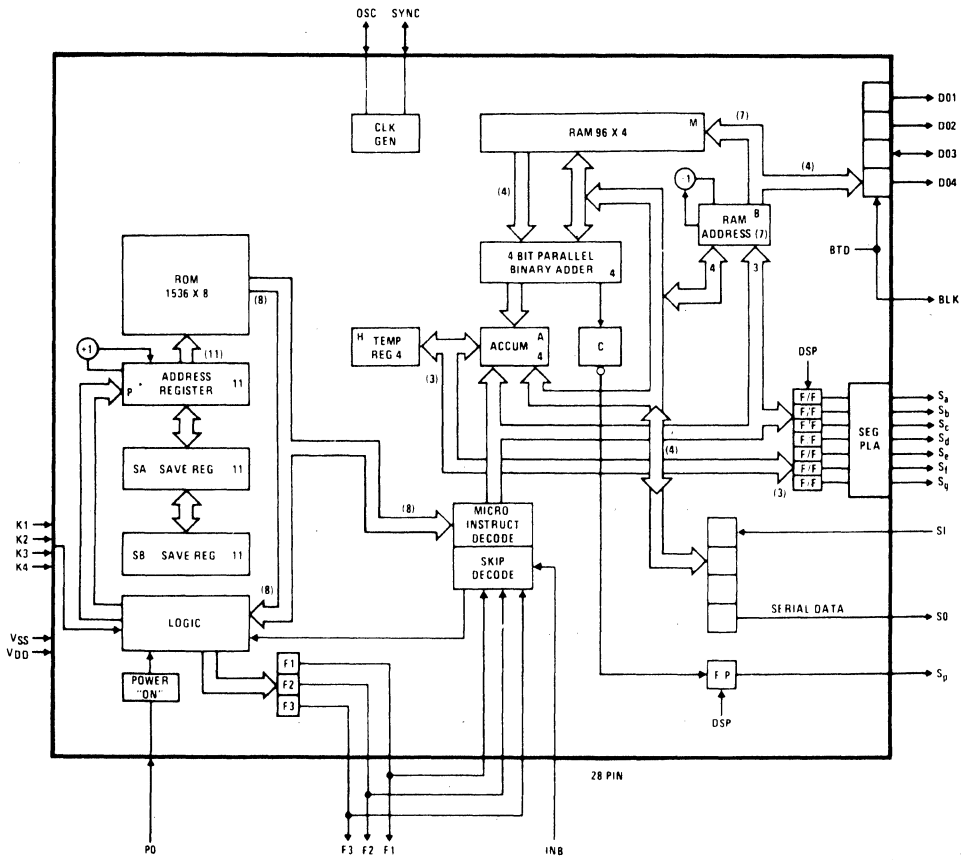
S123

MM57140N NSC
MM57152N NSC



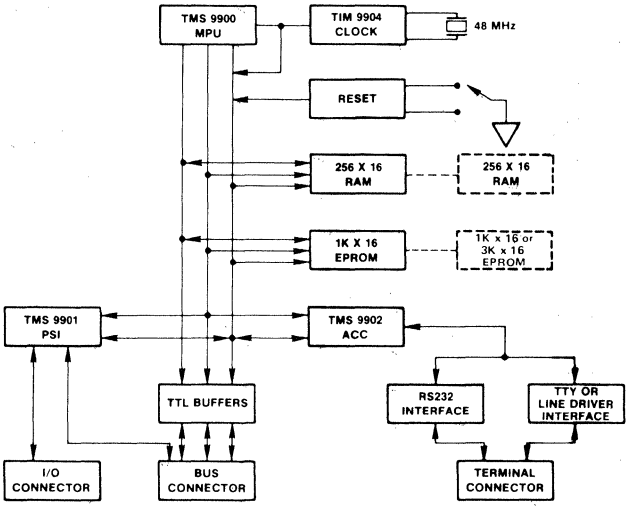
S124

MM5799N NSC



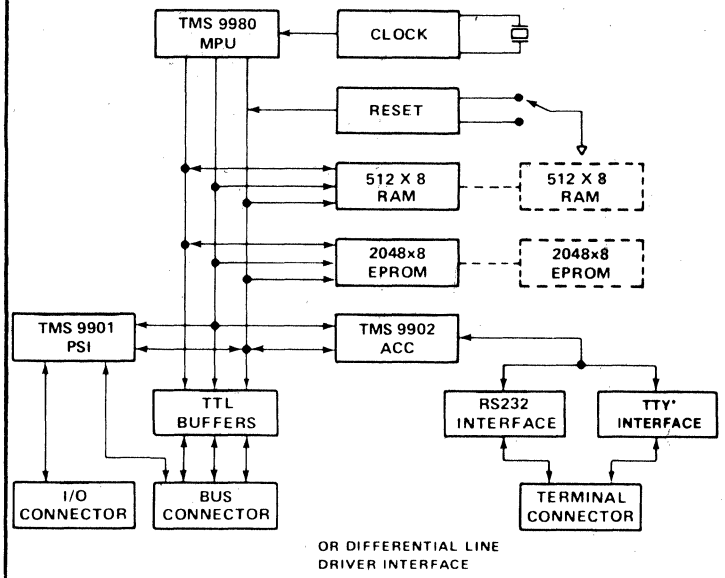
S125

TM990/100M TII



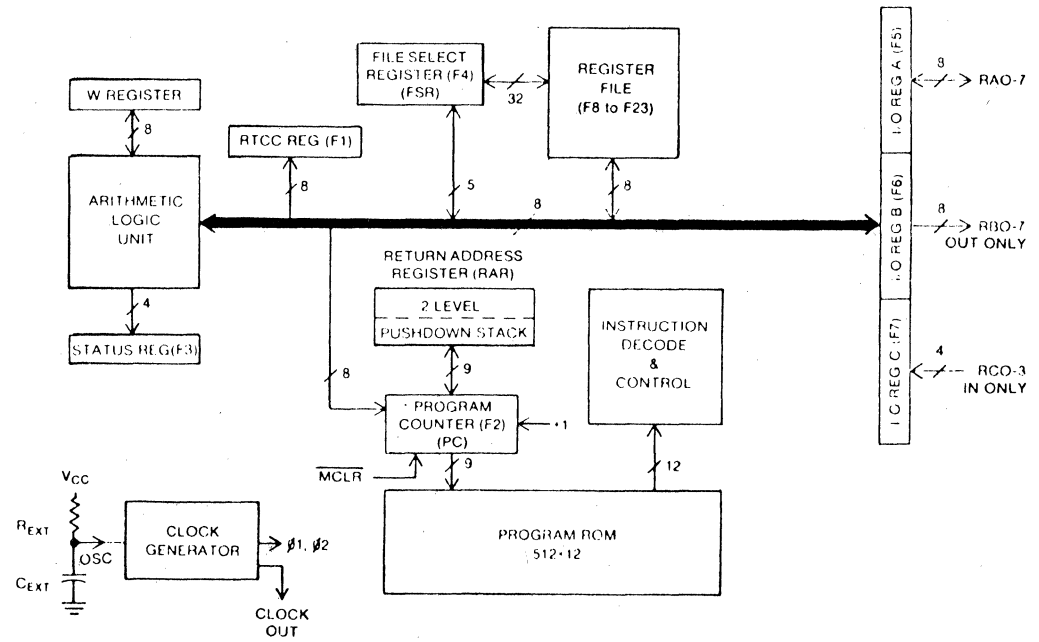
S126

TM990/180M TII



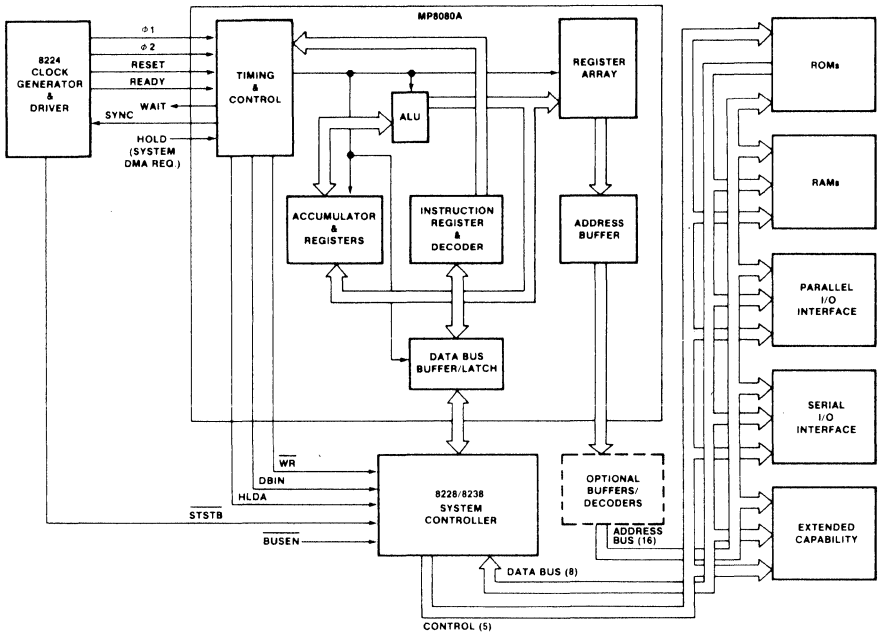
S127

PIC1654 GIC



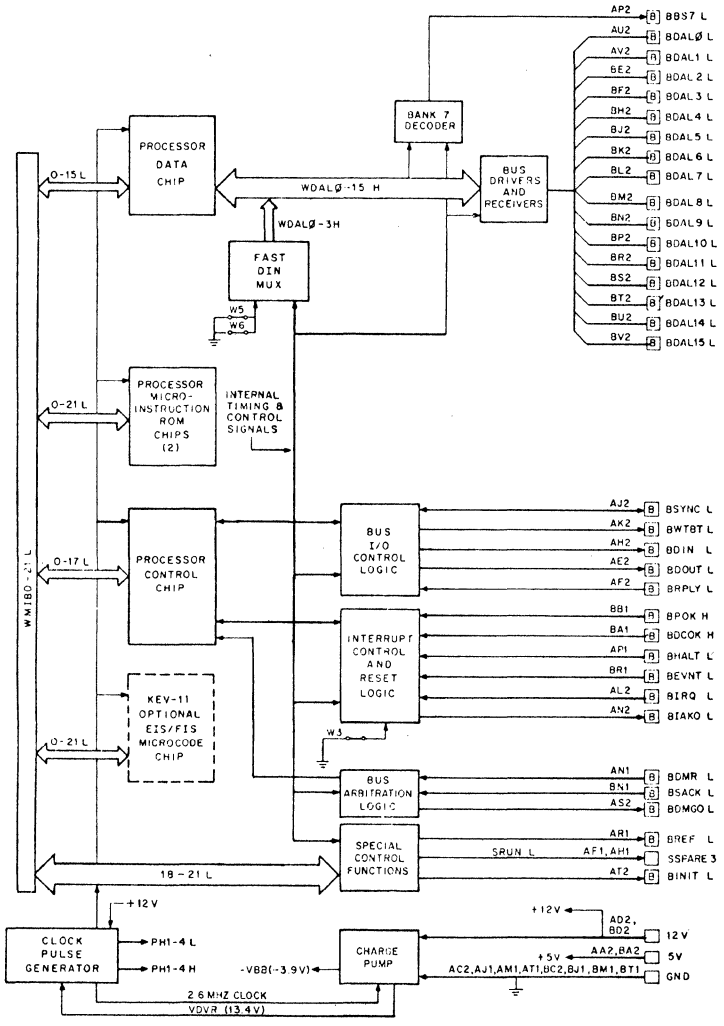
S128

MP8080AI SIC



S129

LSI11/2 DEC

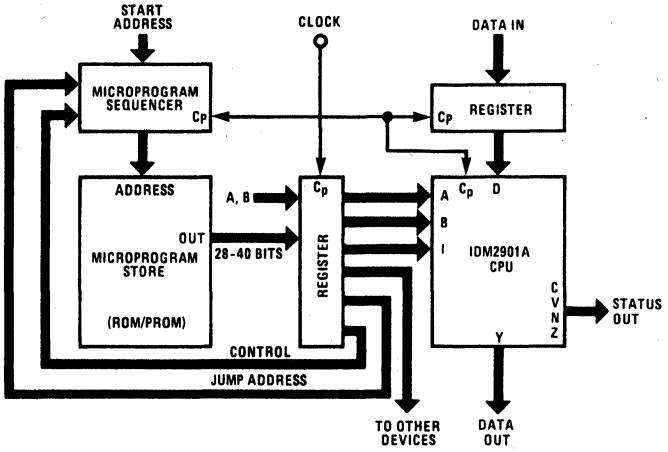


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

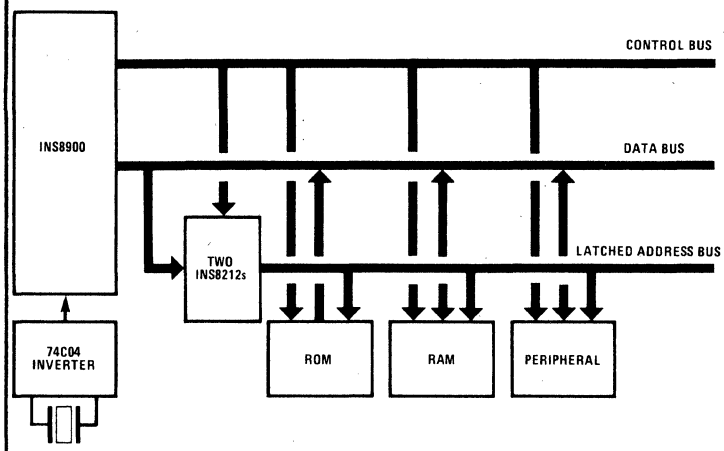
S130

IDM2900 NSC



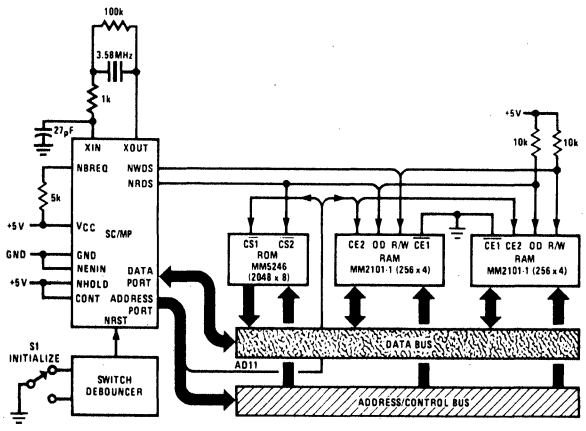
S131

INS8900 NSC



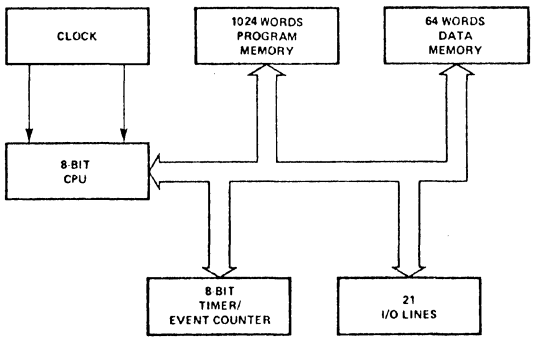
S132

SC/MP NSC



INS8060 Four-Chip System

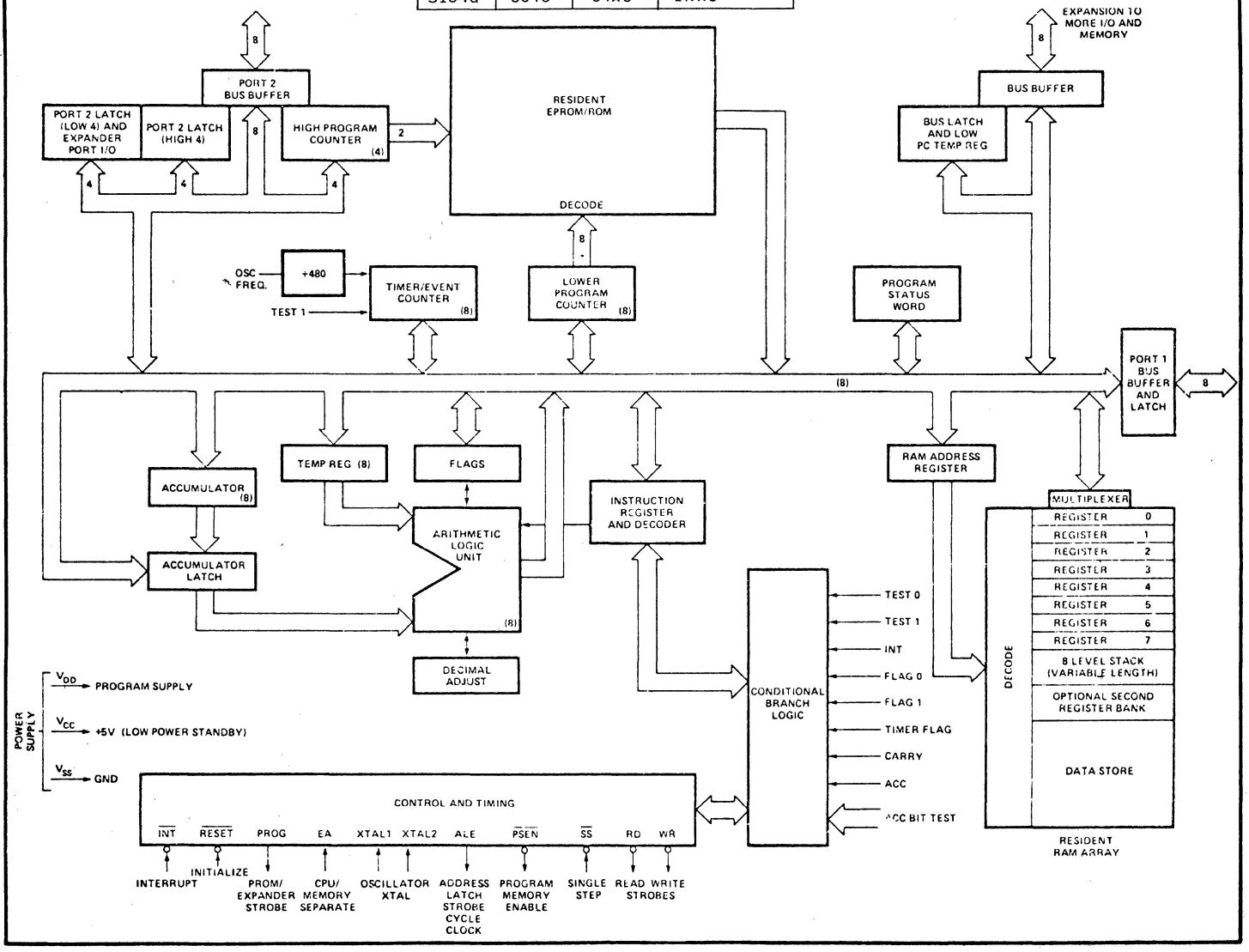
S133



	TYPE	ROM	MFR
S133	8021 8048	1kx8	ITL, PHIN
S133a	8748	1kx8	ITL, PHIN
S133b	8035	External	ITL, PHIN

S134

		RAM/ROM		
S134	8748	64x8	1kx8 EPROM	ITL
S134a	8035	64x8	EXTERNAL	ITL
S134b	8049	128x8	2kx8	ITL
S134c	8039	128x8	EXTERNAL	ITL
S134d	8048	64x8	1kx8	ITL

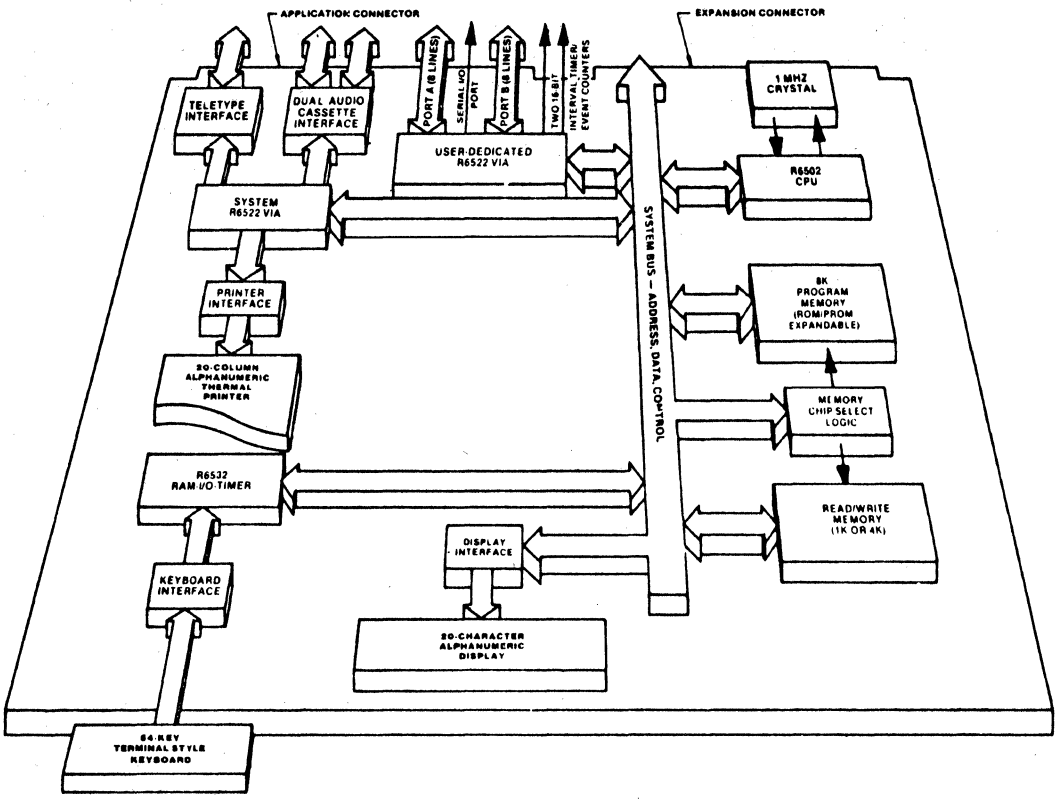


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

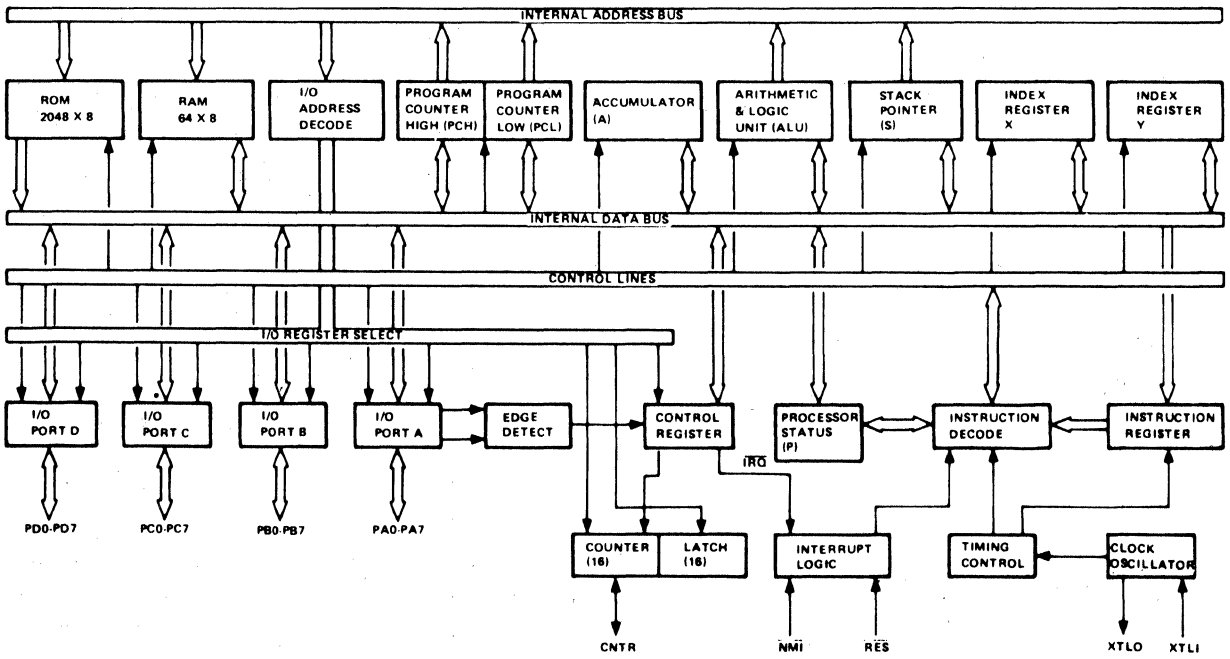
AIM65 RKW

S135



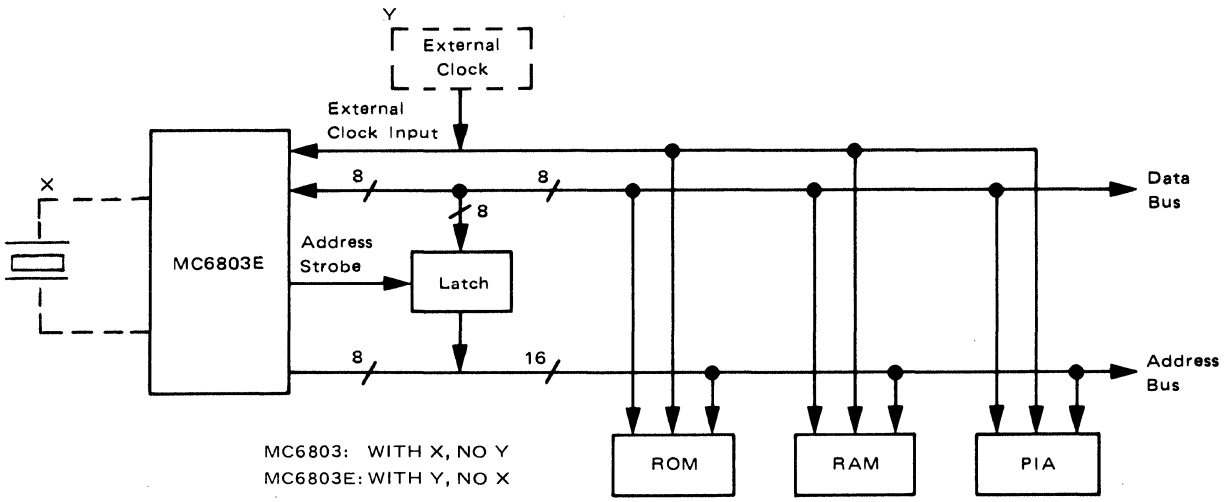
R6500/1 RKW

S136



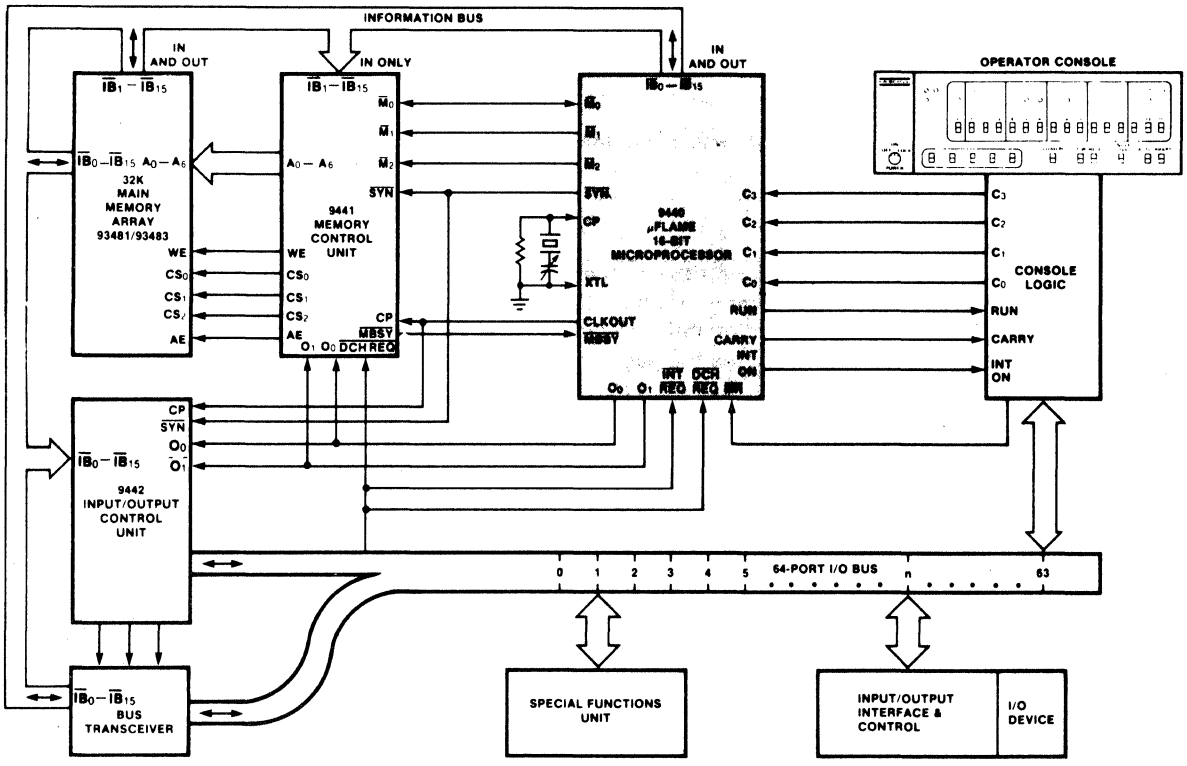
S137

MC6803 MOTA



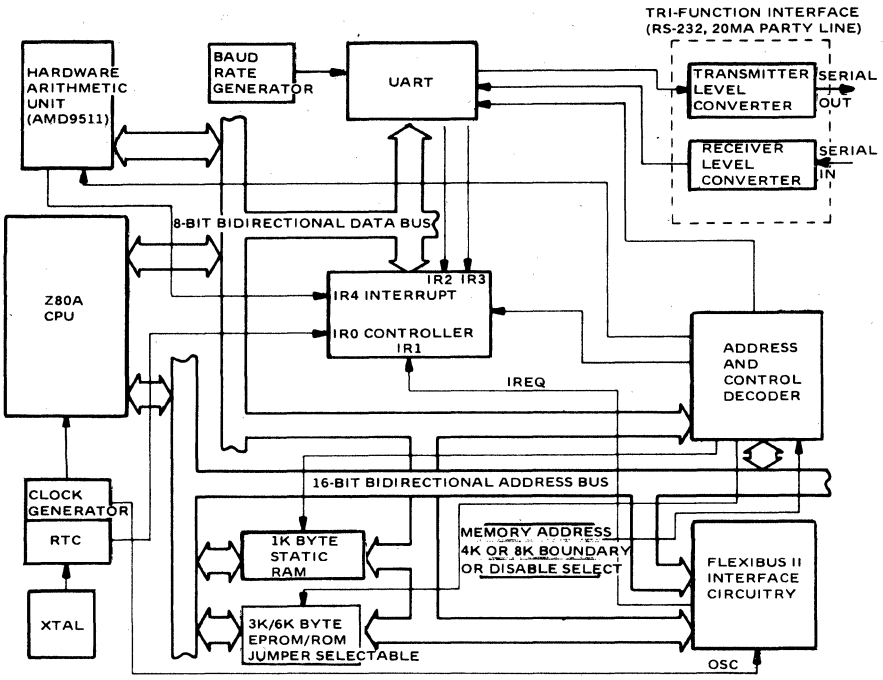
S138

9440 FSC



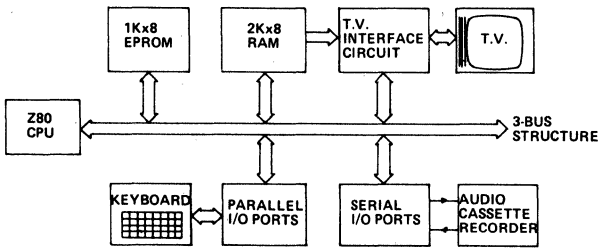
S139

PCS1880 PCS



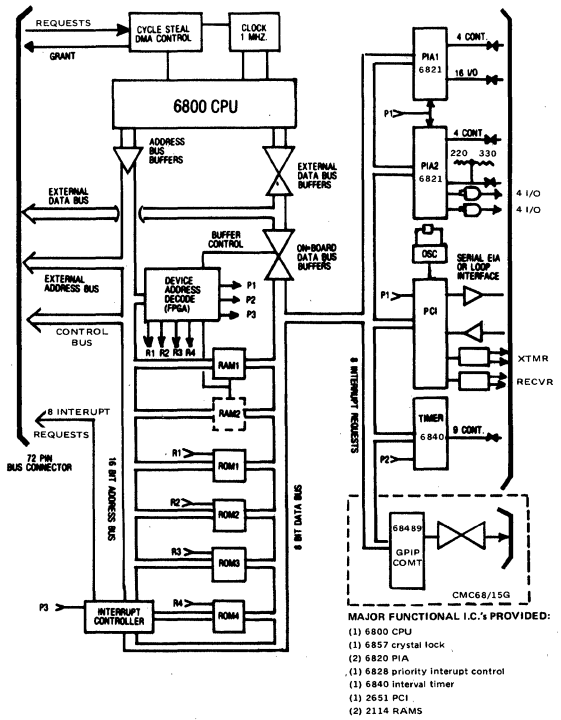
S140

NASCOMI NASB



S141

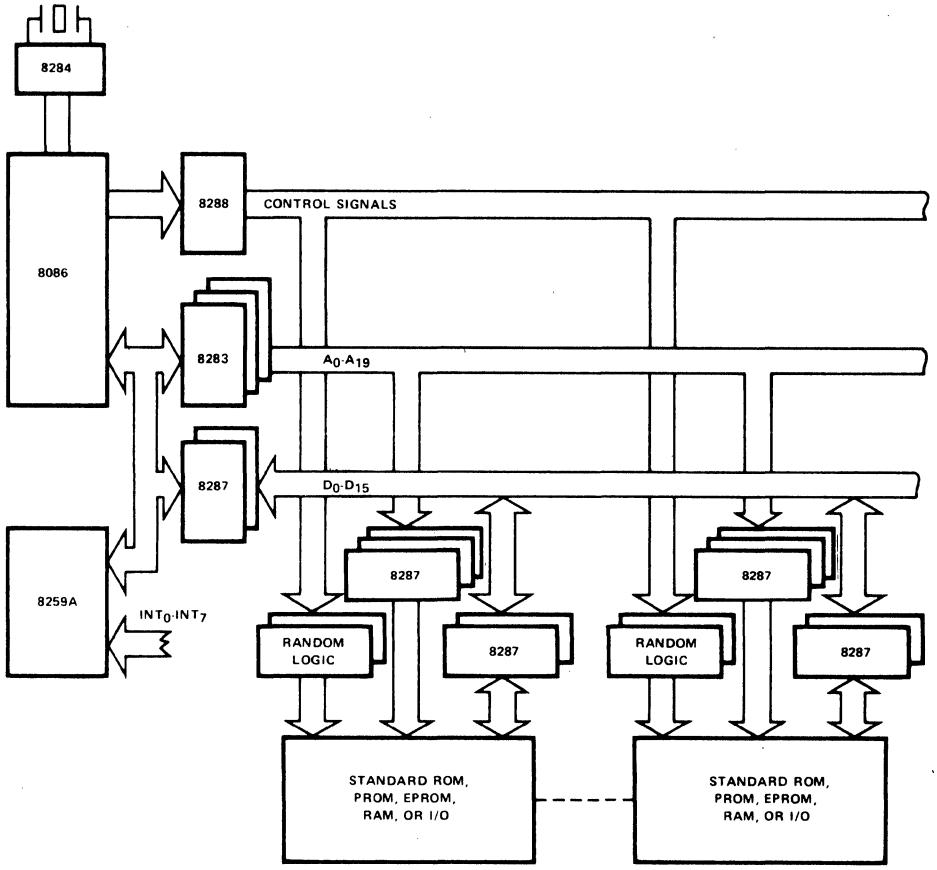
CMC68/15 RCI



MAJOR FUNCTIONAL I.C.'s PROVIDED:
(1) 6800 CPU
(1) 6857 crystal lock
(2) 6820 PIA
(1) 6828 priority interupt control
(1) 6840 interval timer
(1) 2651 PCI
(2) 2114 RAMS

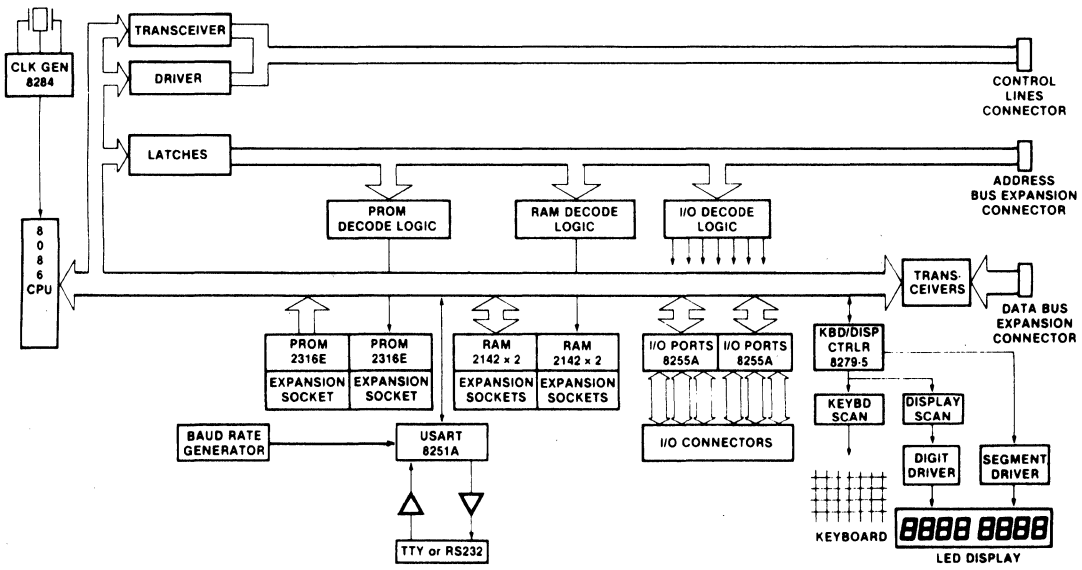
S142

MCS86



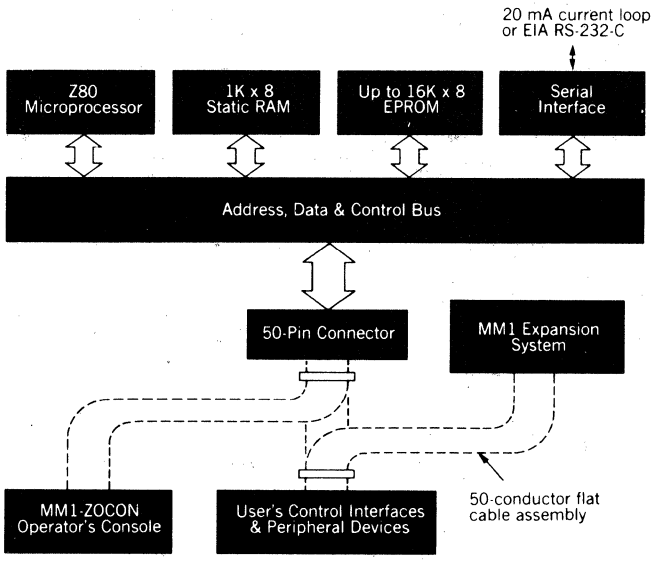
S143

SDK86 ITL



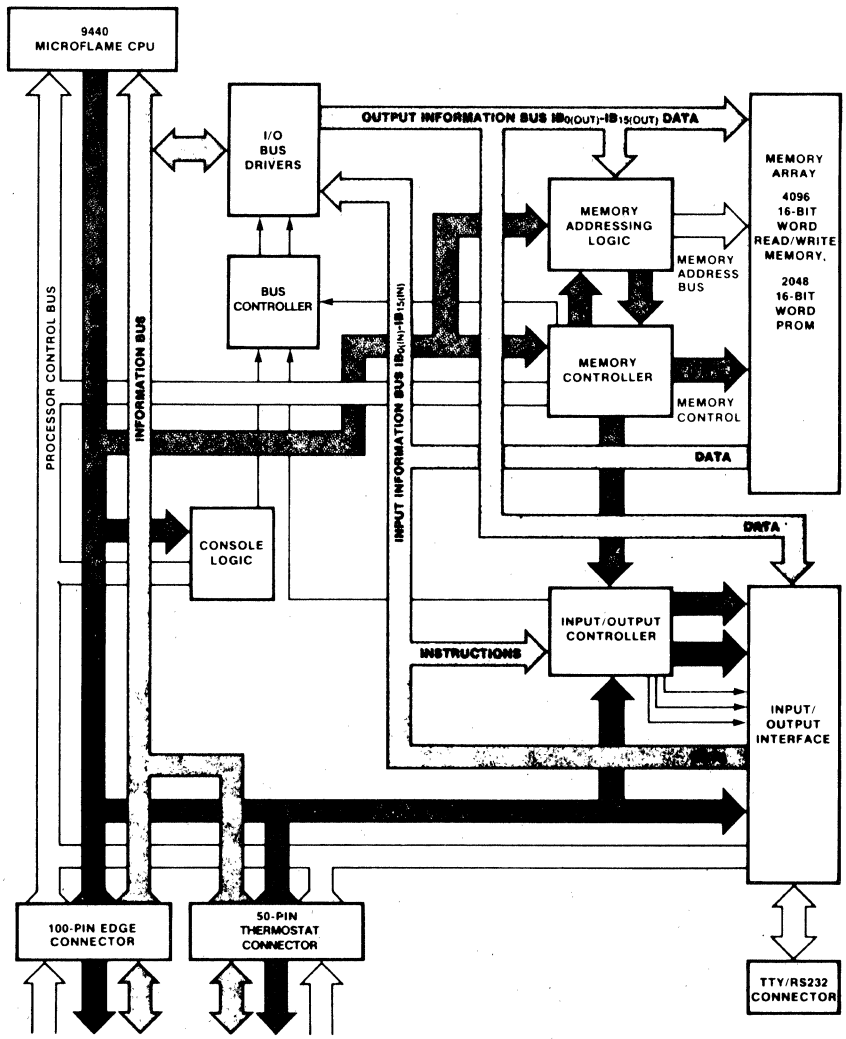
S144

CSS-1143 CLI



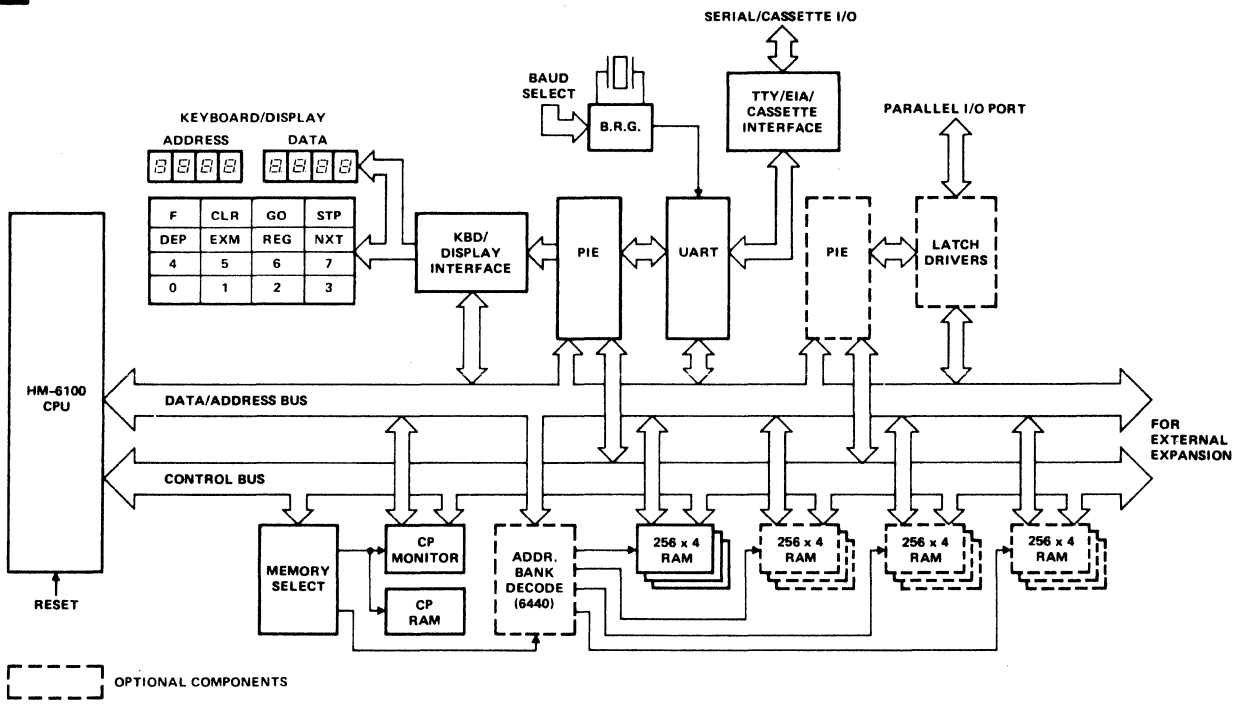
S145

SPARK—16 FSC



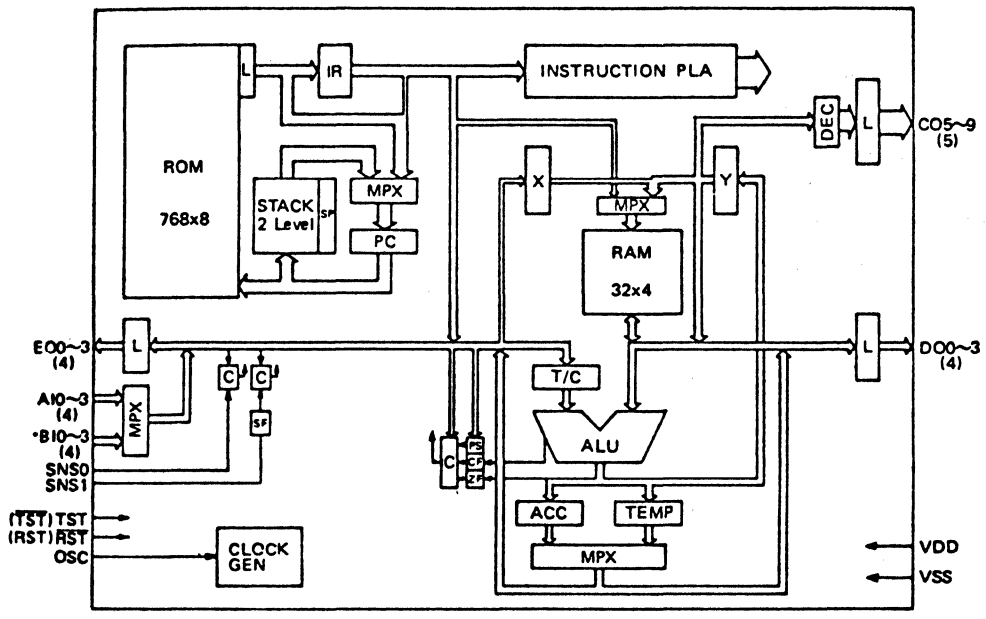
HB61000 HAS

S146



MN1402 MATJ
MN1432 MATJ

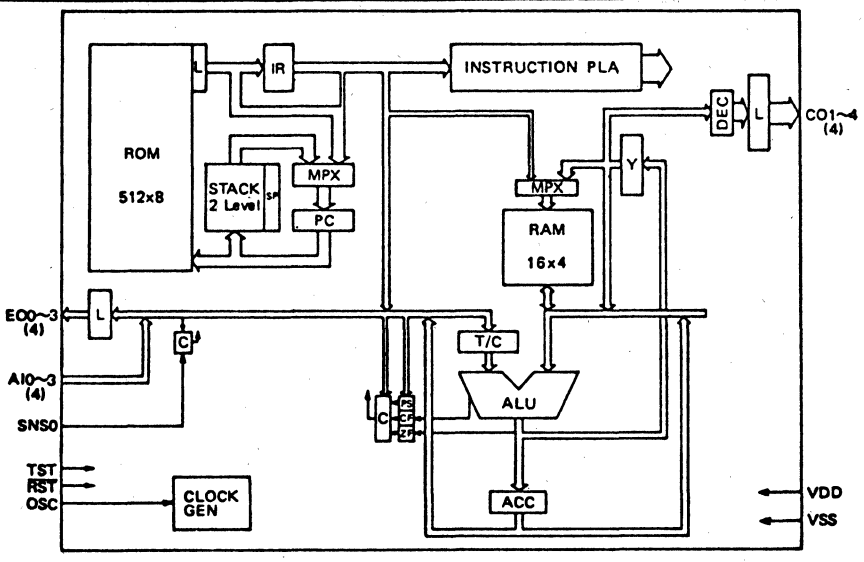
S147



( ): MN1432

S148

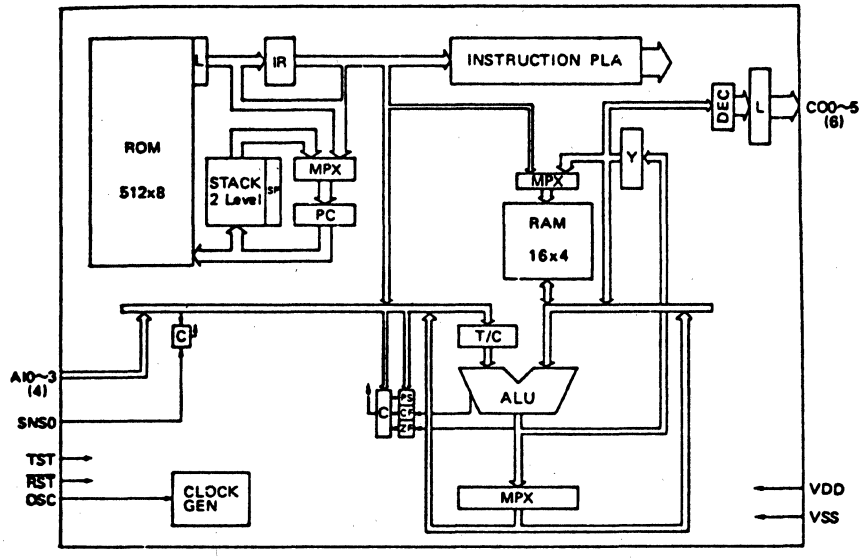
MN1403 MATJ
MN1453 MATJ



S148a: RAM 64 x 4

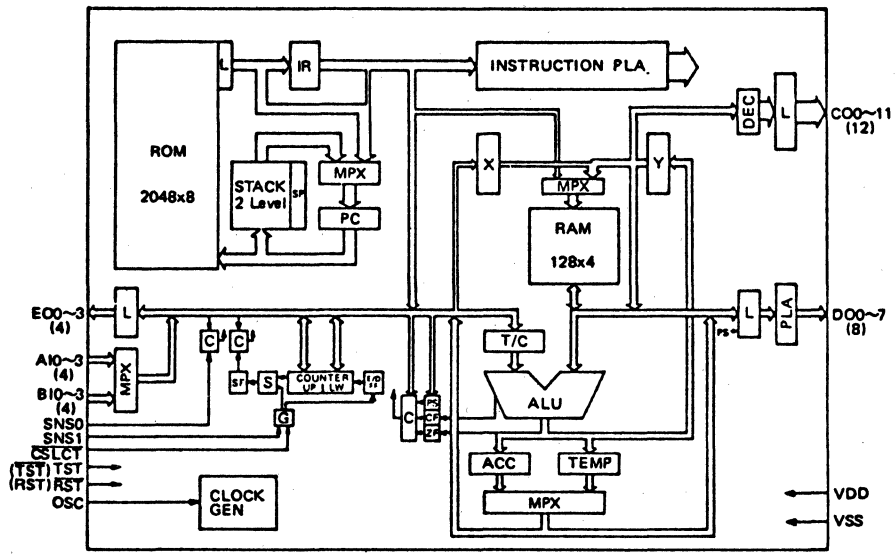
S149

MN1404 MATJ



S150

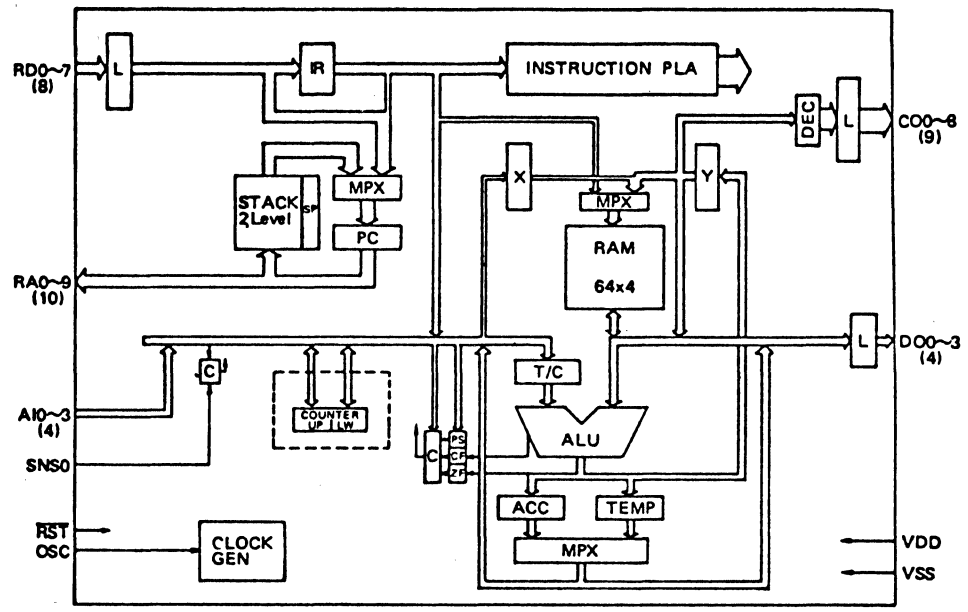
MN1405 MATJ
MN1435 MATJ



( ): MN1435

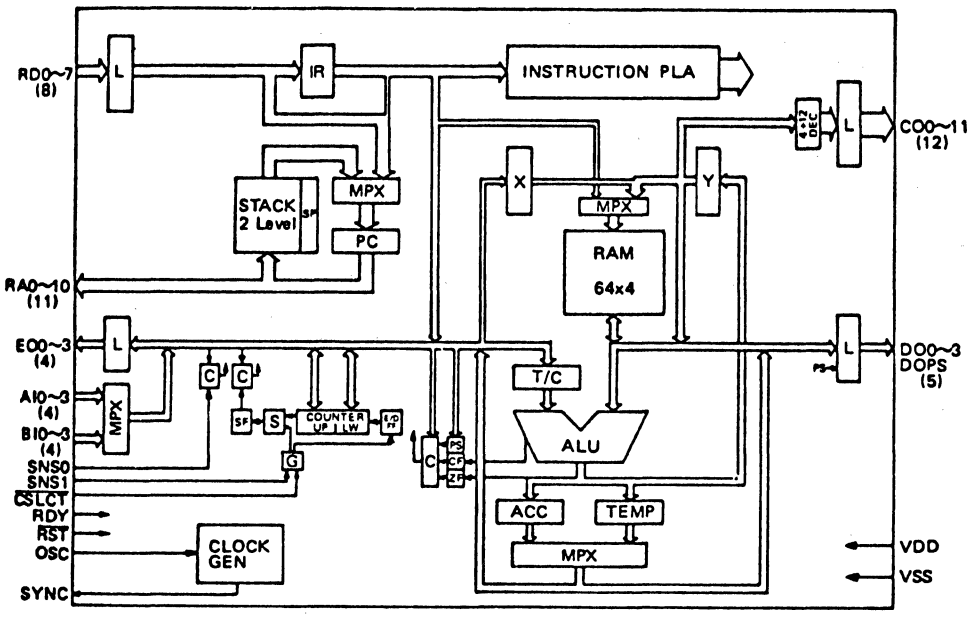
S151

MN1498 MATJ



S152

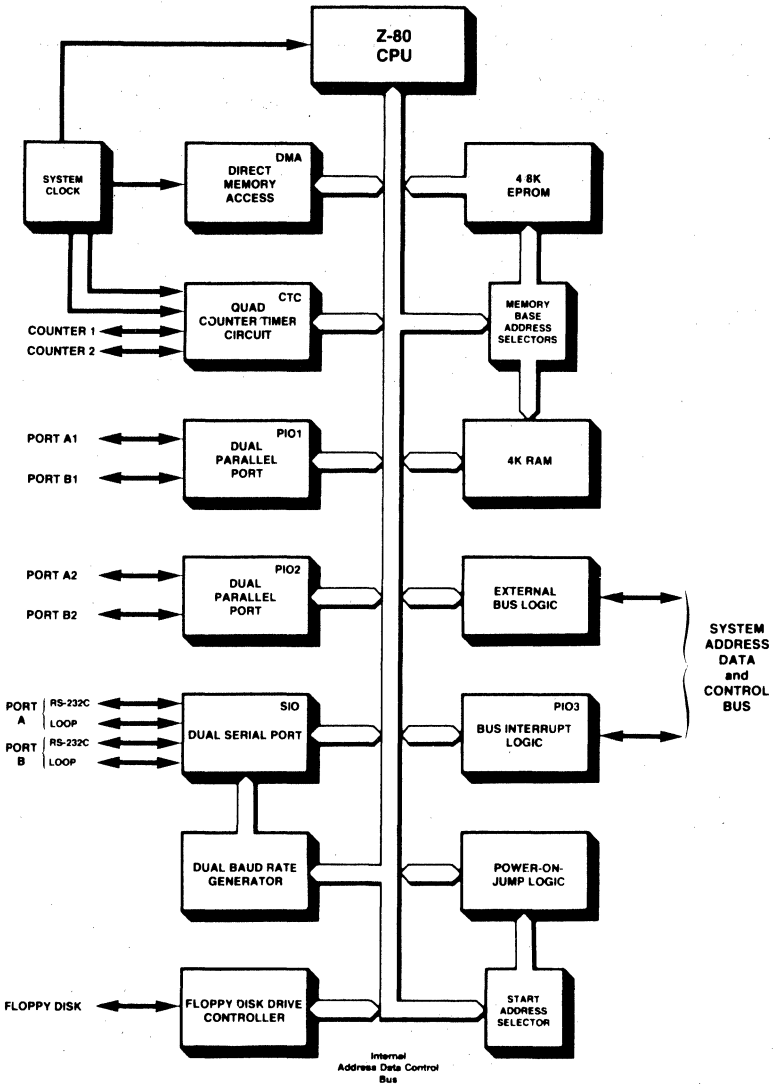
MN1499 MATJ
MN1499A MATJ



S152a: RAM 128 x 4

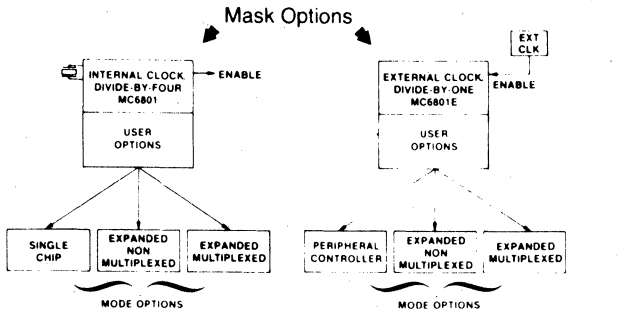
S153

MLZ80 HEU



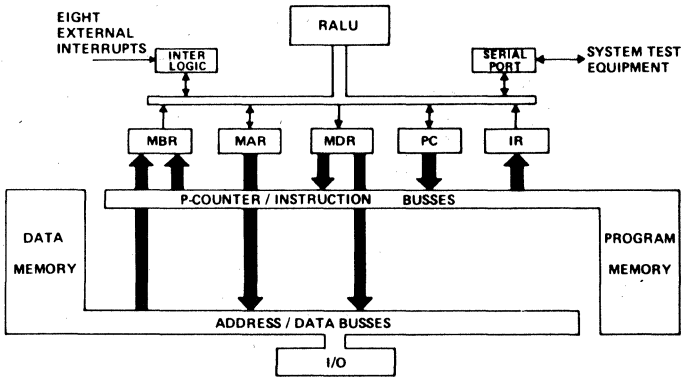
S154

MC6801 MOTA



S155

H18 HACC

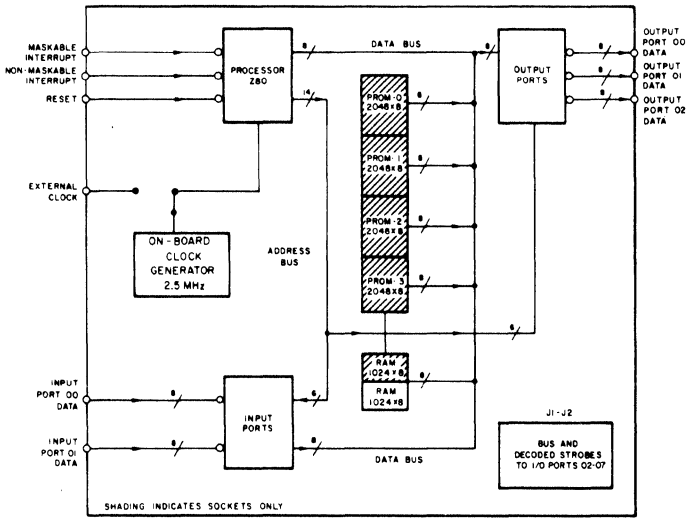


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

S156

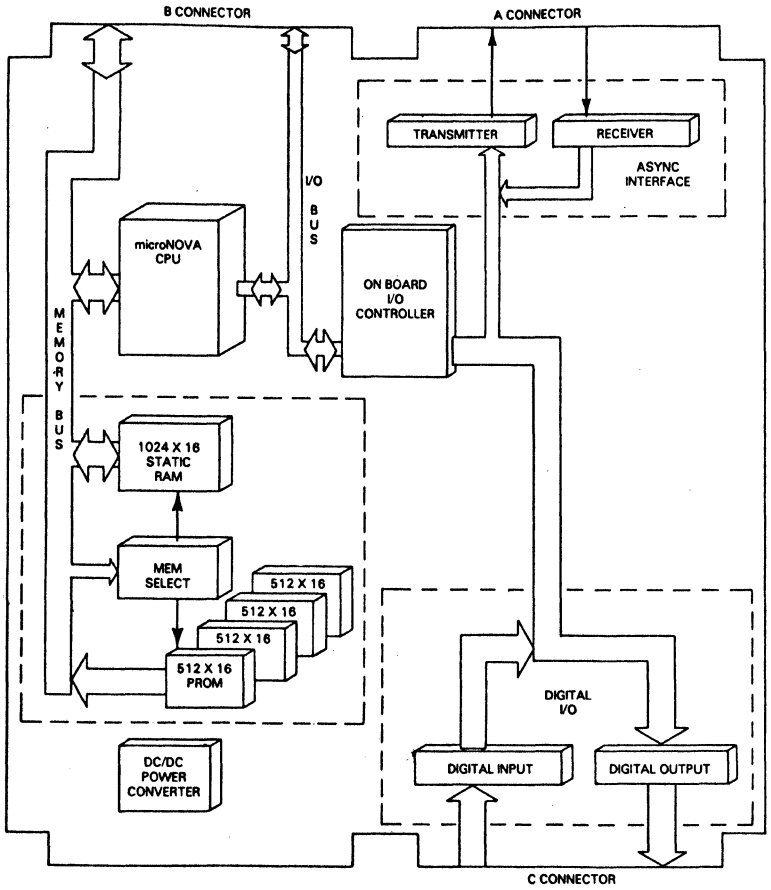
MD-SBC1 MOS



a) NO ON-BOARD CLOCK GENERATOR

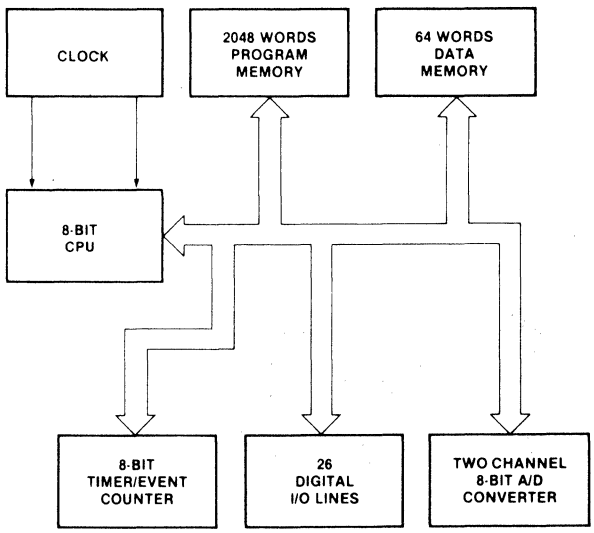
S157

MBC/1 DGC



S158

8022 ITL

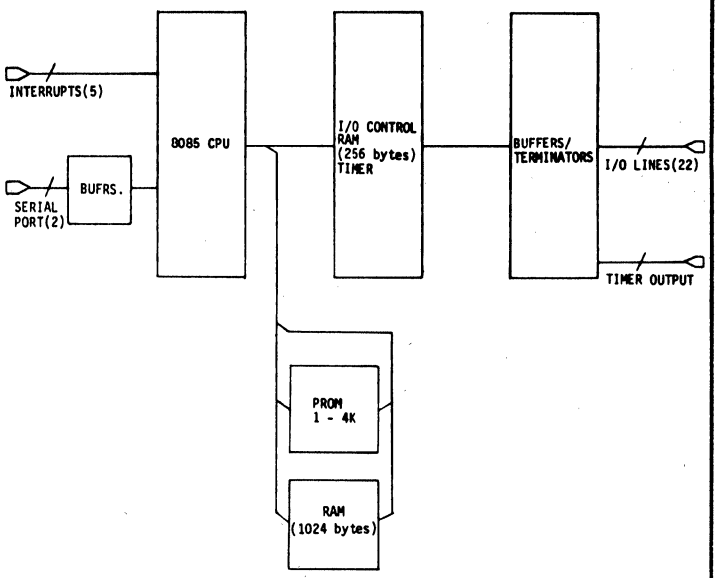


15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

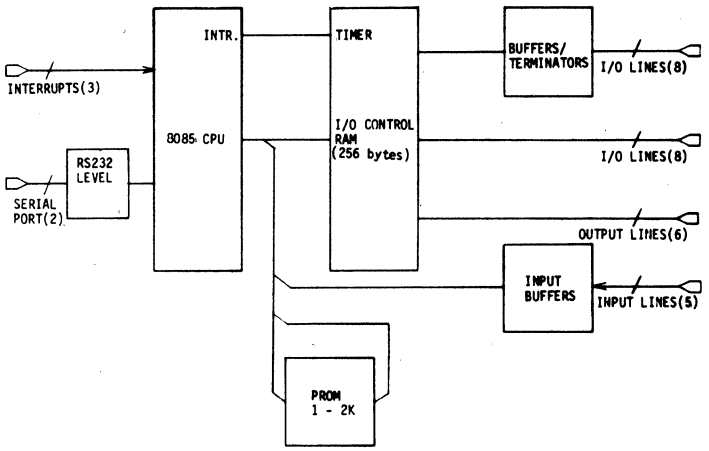
S161

SSM-85/1 SSC



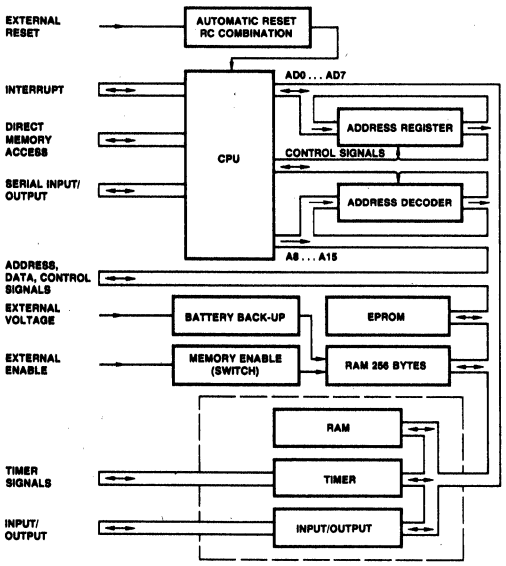
S162

SSM-85/2 SSC



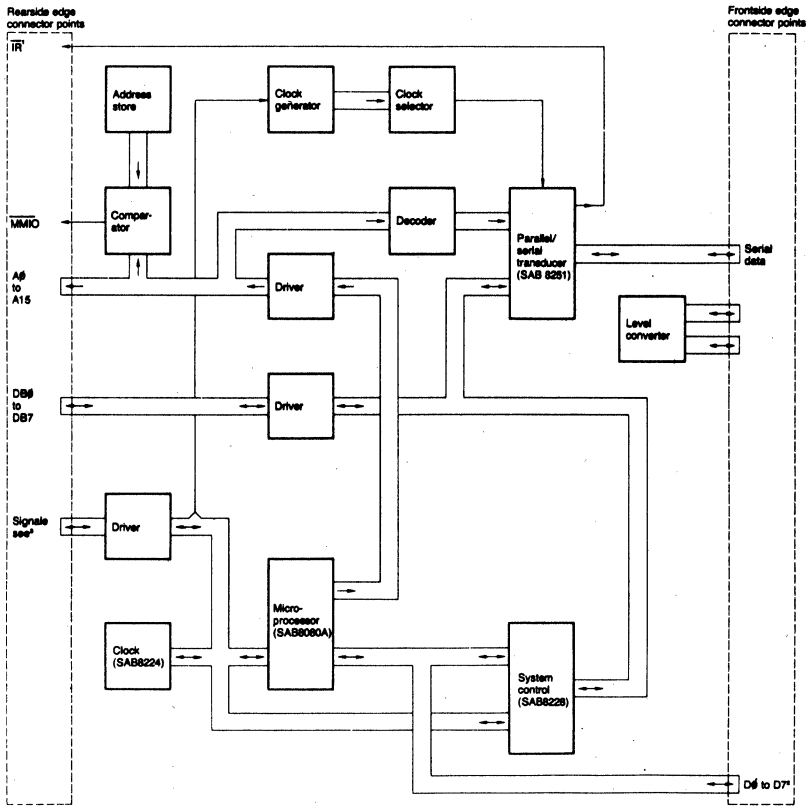
S163

SKC85 SIEG



S164

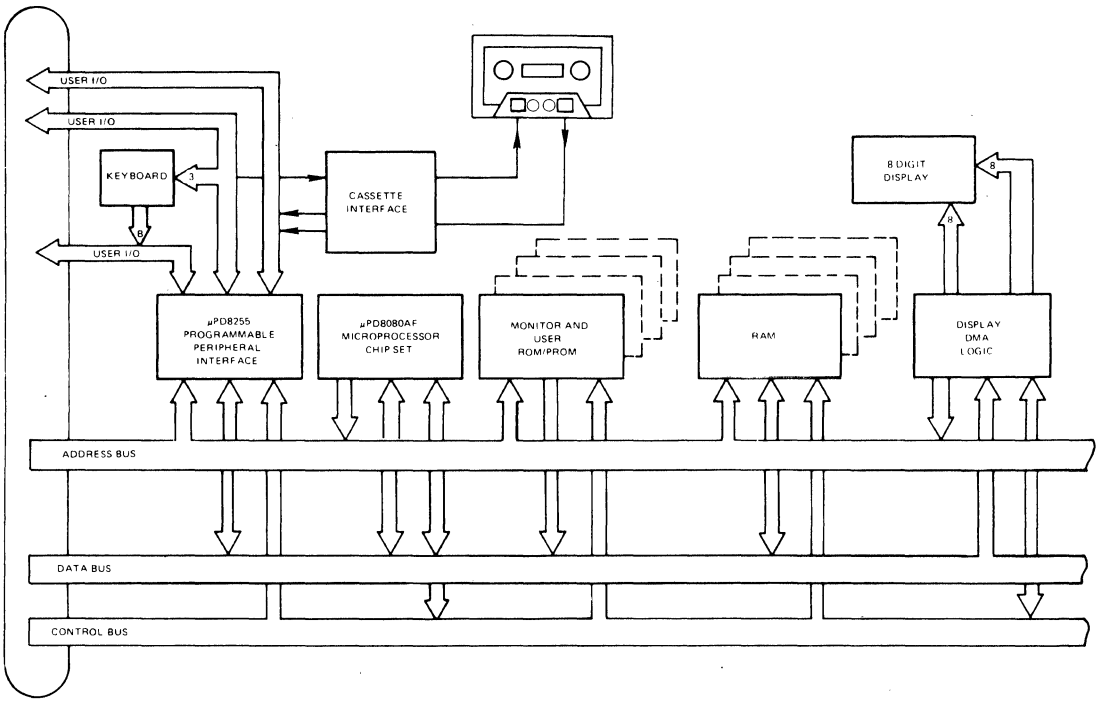
SMP80 SIEG



*IR = Interrupt – Demand (special signal)
*Internal central unit signals for testing
*RESIN, RESET, OSC, Ø1TTL, Ø2TTL, SYNC, STSTB, MEMR, MEMW, IOR, IOW, RDYIN, WAIT, INTE, INT, INTA, HOLD, HLDA, BUSEN, INTBUS (special signal), RST7 (special signal)

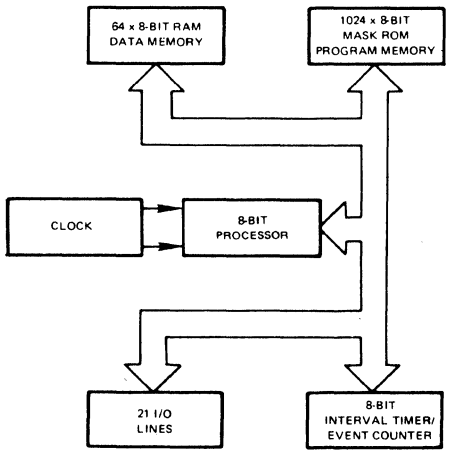
S165

TK-80A NECM



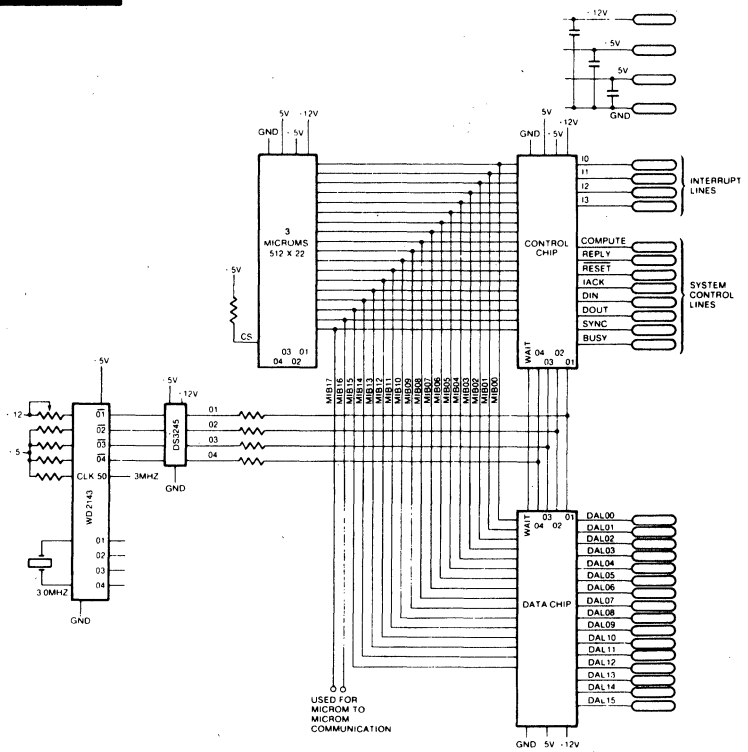
S166

µPD8021 NECM



S167

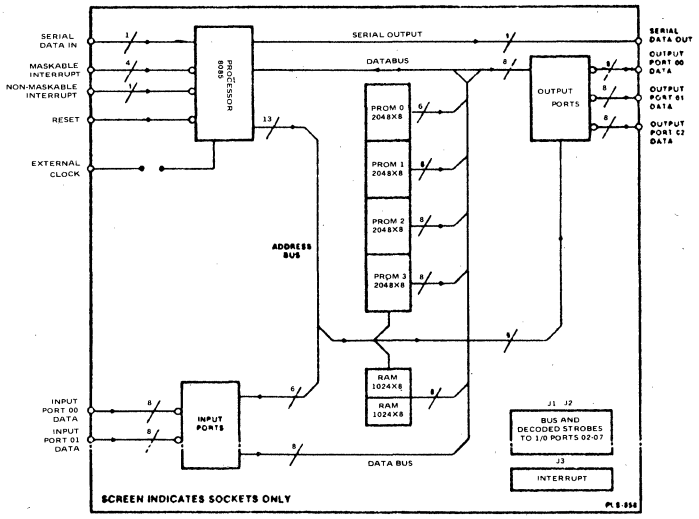
WD9000 WDC



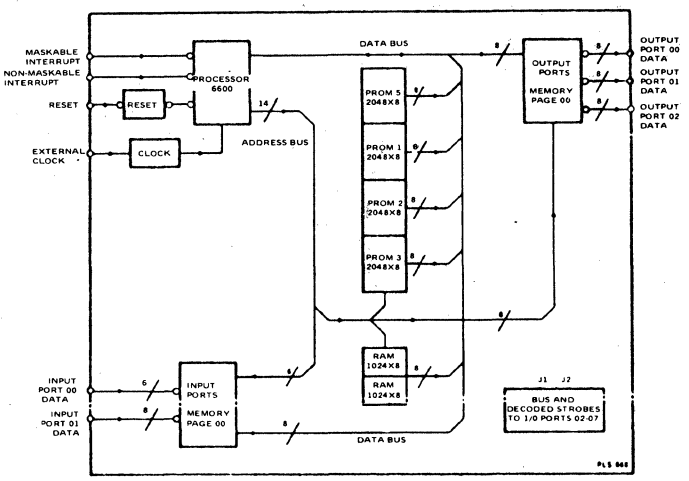
15. SYSTEM BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

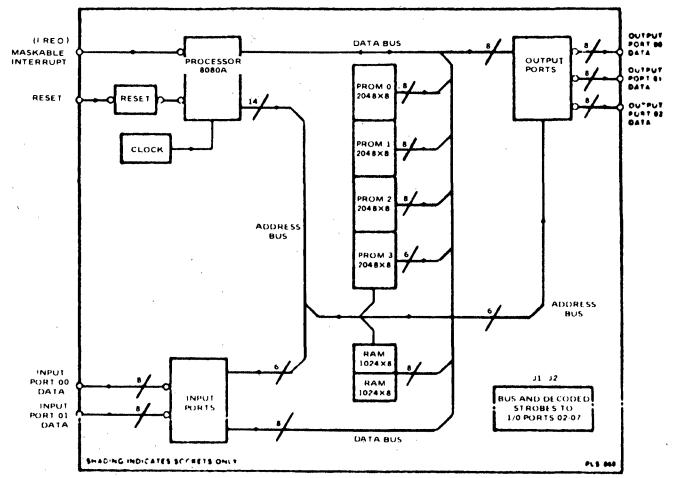
S168



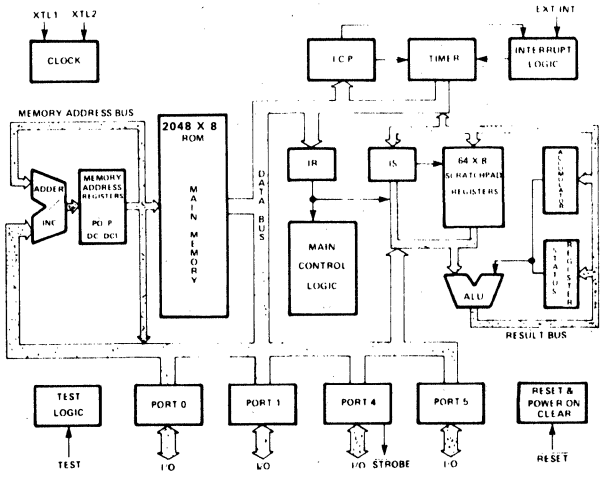
S169



S170



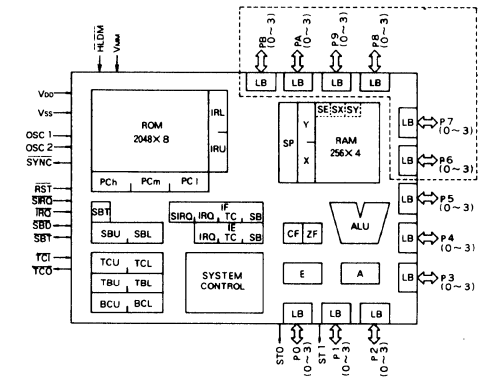
S171



15. SYSTEM BLOCK DRAWINGS

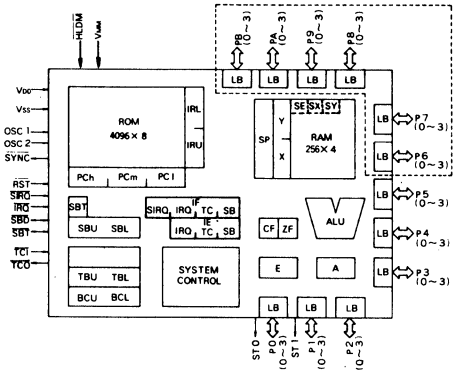
IN DRAWING NUMBER SEQUENCE

S172



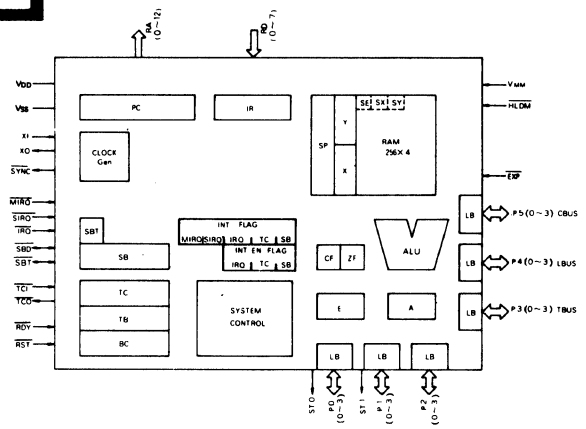
Note) MN1542 does not include a part circled in dotted line.

S173

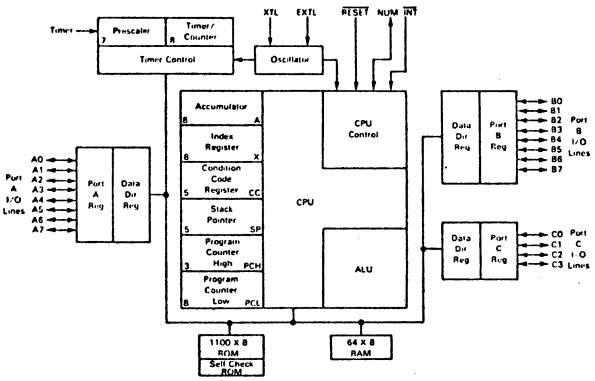


Note) MN1544 does not inclued a part circled in dotted line.

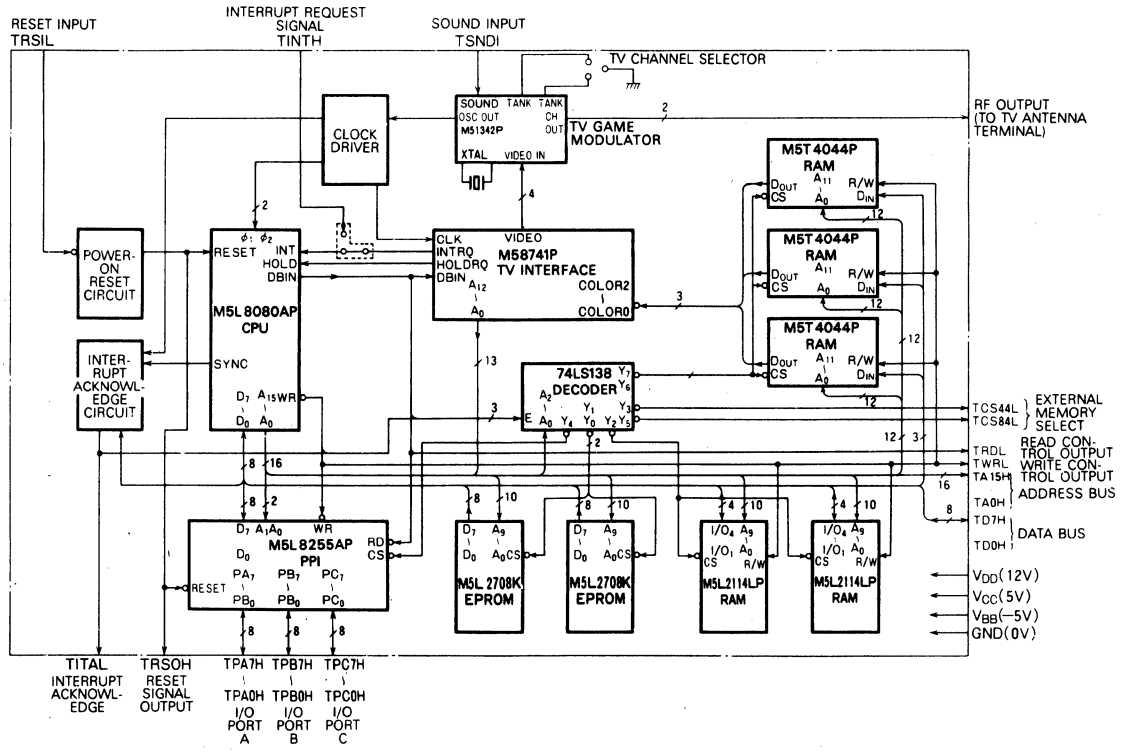
S174



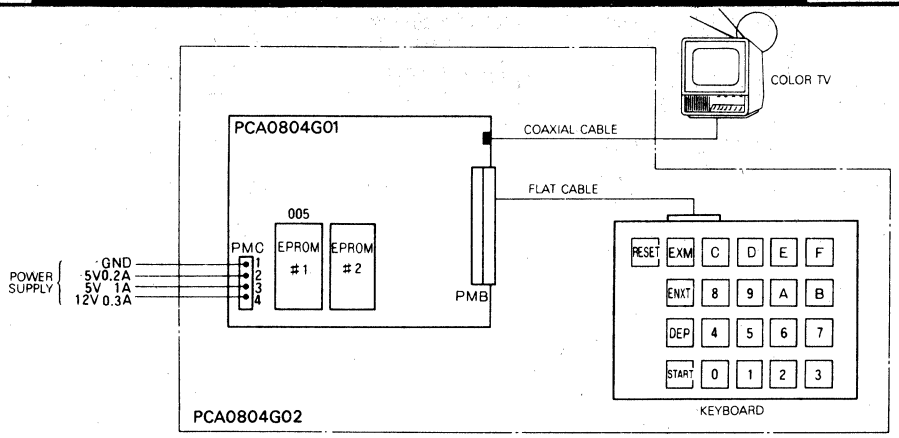
S174a



S175

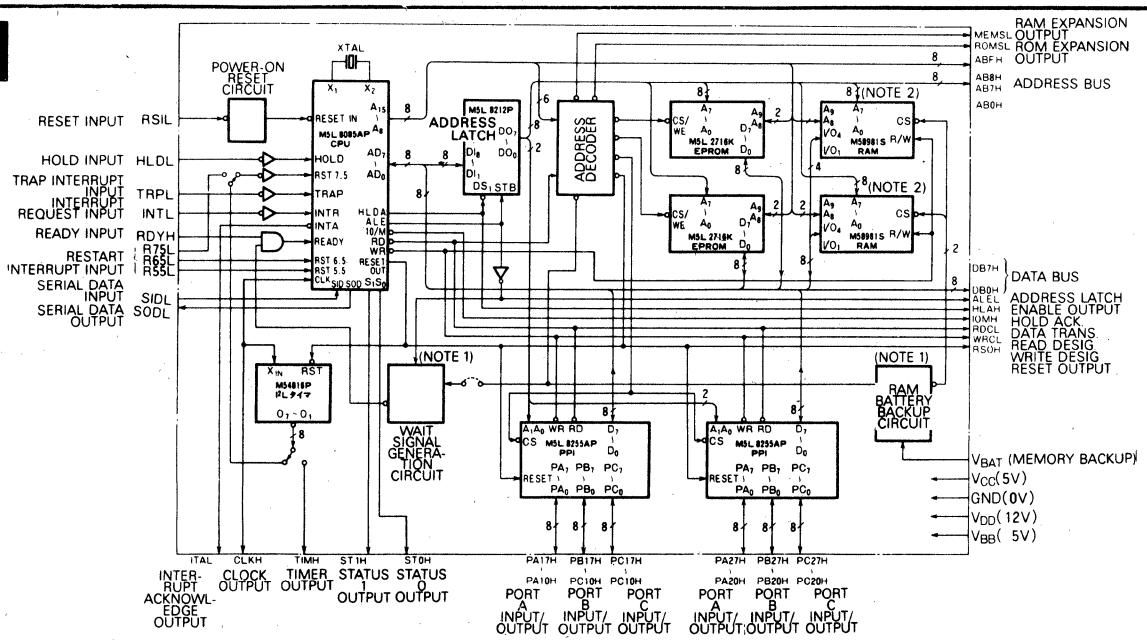


S176



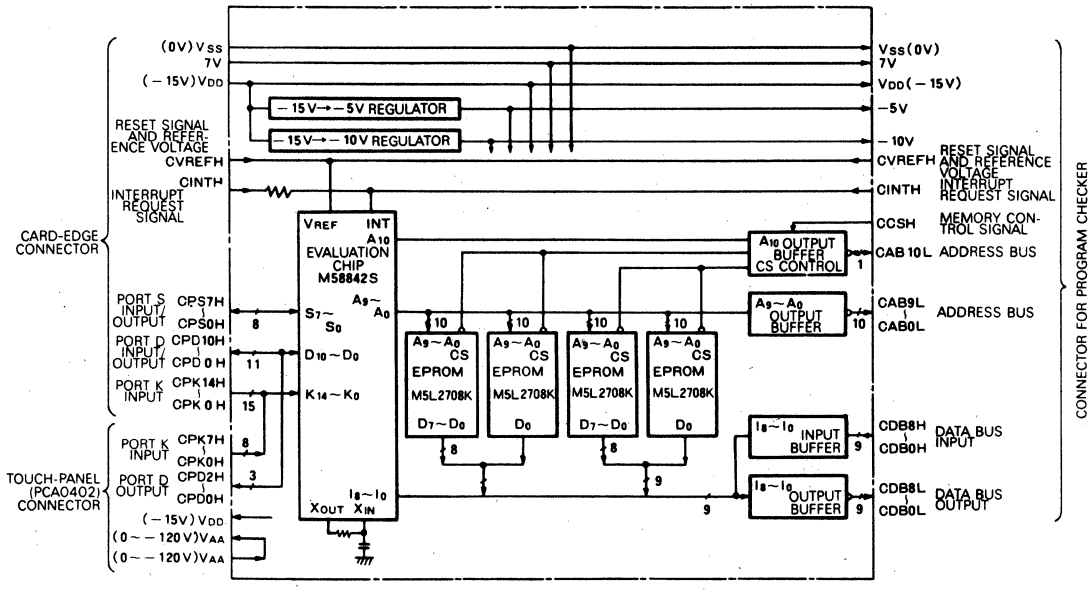
Note 3 : #1 M5L 2708K (005). Contains the monitor program, and line, block, and character display program.
#2 M5L 2708K. Blank EPROM for user's program storage.

S177

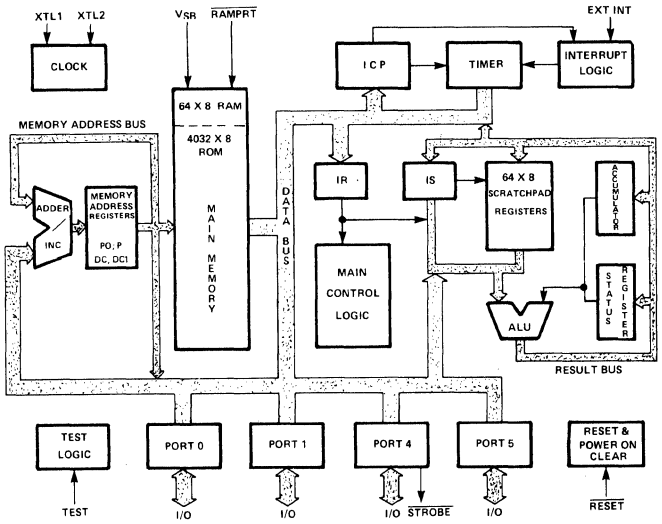


Note 1 : The wait signal generation circuit and the RAM battery backup circuit are not mounted on the PCA8501G01.
2 : The M5L 21114LPs are mounted on the PCA8501G01, instead of M58981Ss.

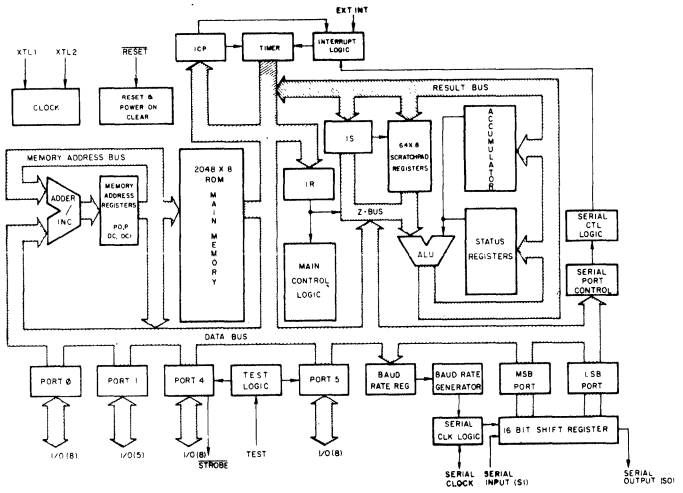
S178



S179

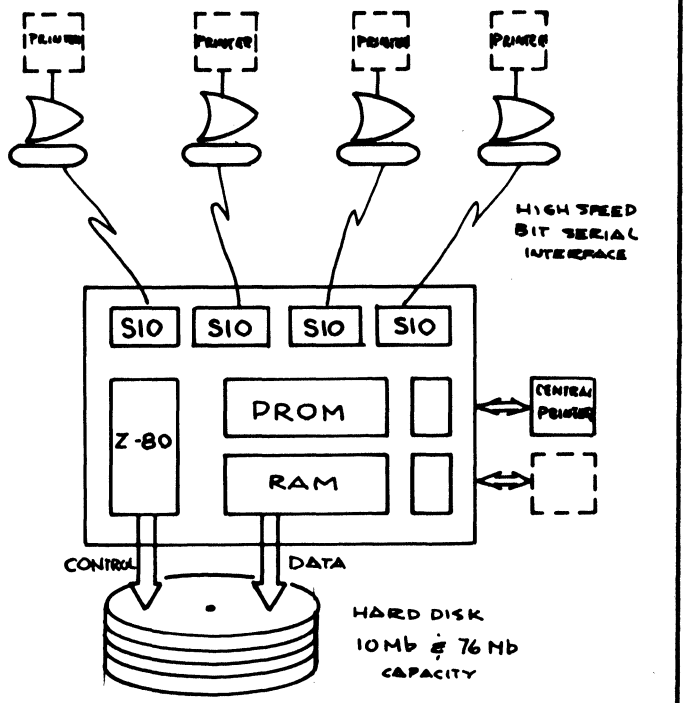


S180

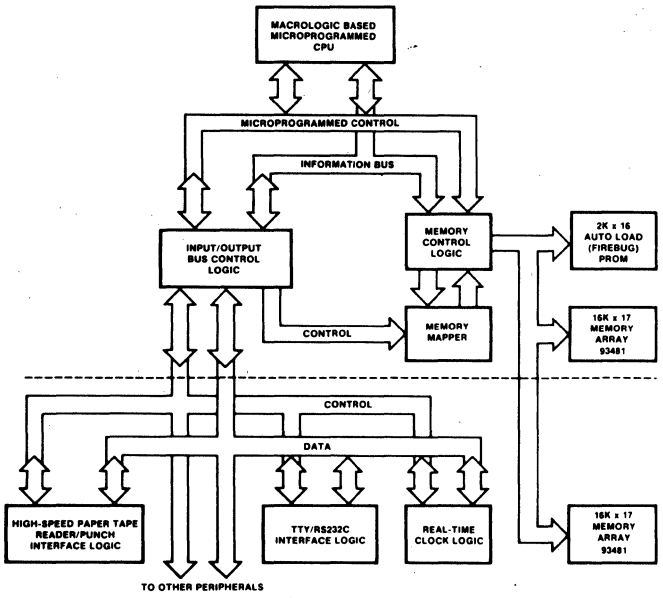


S181

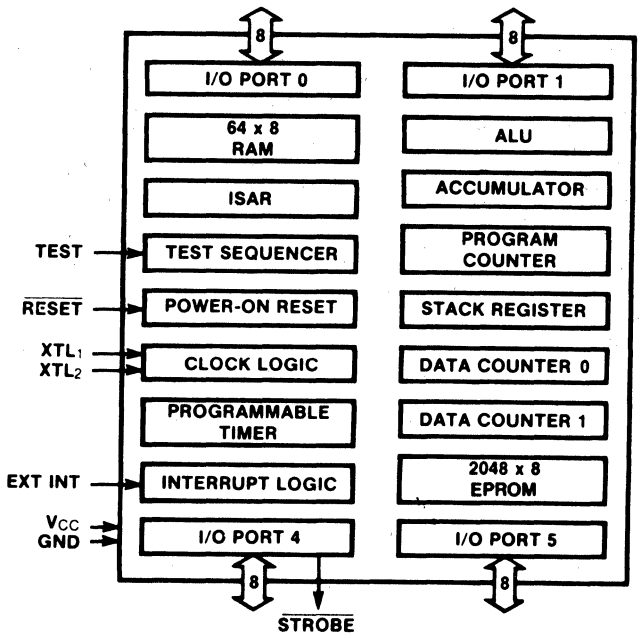
S182



S183


MACROLOGIC BASED MICROPROGRAMMED CPU
MICROPROGRAMMED CONTROL
INFORMATION BUS
INPUT/OUTPUT BUS CONTROL LOGIC
MEMORY CONTROL LOGIC
2K x 16 AUTO LOAD (FIREBUG) PROM
CONTROL
MEMORY MAPPER
16K x 17 MEMORY ARRAY 93481
CONTROL
DATA
HIGH-SPEED PAPER TAPE READER/PUNCH INTERFACE LOGIC
TTY/RS232C INTERFACE LOGIC
REAL-TIME CLOCK LOGIC
16K x 17 MEMORY ARRAY 93481
TO OTHER PERIPHERALS

S184


8
8
I/O PORT 0
I/O PORT 1
64 x 8 RAM
ALU
ISAR
ACCUMULATOR
TEST
TEST SEQUENCER
PROGRAM COUNTER
RESET
POWER-ON RESET
STACK REGISTER
XTL1
XTL2
CLOCK LOGIC
DATA COUNTER 0
PROGRAMMABLE TIMER
DATA COUNTER 1
EXT INT
INTERRUPT LOGIC
2048 x 8 EPROM
VCC
GND
I/O PORT 4
I/O PORT 5
8
8
STROBE

16. INSTRUCTION FORMAT DRAWINGS

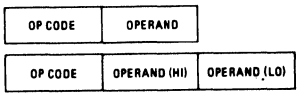
IN DRAWING NUMBER SEQUENCE

NOTES: These drawings are referenced in the Instruction Set Index section of this D.A.T.A.BOOK in accordance with information supplied by the manufacturers.

Since representations may vary, the sources of information should be consulted for additional detail and explanation.

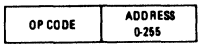
F2

Immediate Addressing

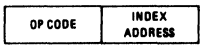


Extended Addressing

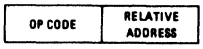
Direct Addressing



Indexed Addressing

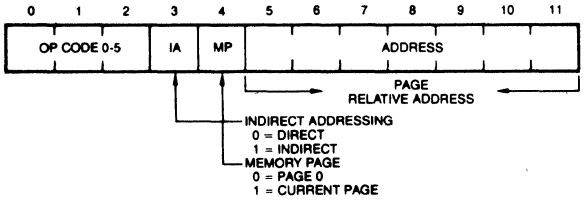


Relative Addressing

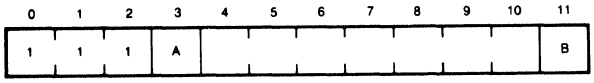


F1

MEMORY REFERENCE INSTRUCTION FORMAT

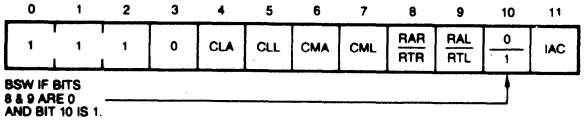


BASIC OPR INSTRUCTION FORMAT



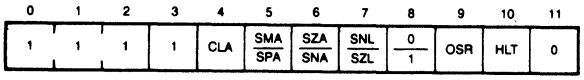
MICROINSTRUCTION	A	B
GROUP 1	0	0 or 1
GROUP 2	1	0
GROUP 3	1	1

GROUP 1 MICROINSTRUCTION FORMAT



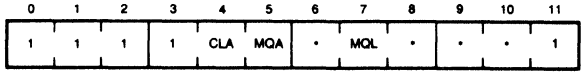
LOGICAL SEQUENCES:
1—CLA, CLL
2—CMA, CML
3—IAC
4—RAR, RAL, RTR, RTL, BSW

GROUP 2 MICROINSTRUCTION FORMAT



LOGICAL SEQUENCES:
1 (Bit 8 is Zero) — SMA or SZA or SNL
(Bit 8 is One) — SPA and SNA and SZL
2 — CLA
3 — OSR, HTL

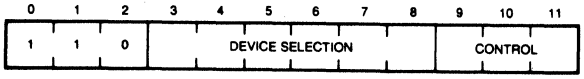
GROUP 3 MICROINSTRUCTION FORMAT



LOGICAL SEQUENCE:
1—CLA
2—MQA, MQL
3—ALL OTHERS

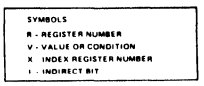
*Don't Care

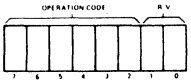
IOT INSTRUCTION FORMAT



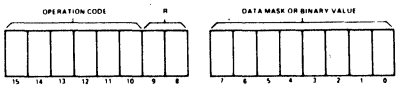
F4

(Z) REGISTER ADDRESSING

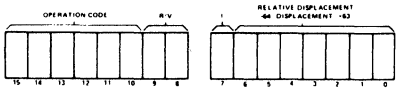




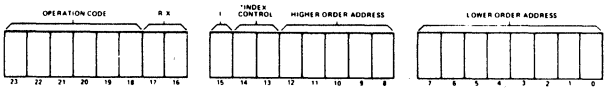
(I) IMMEDIATE ADDRESSING



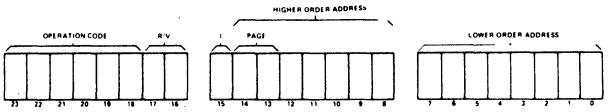
(R) RELATIVE ADDRESSING



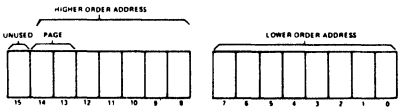
(A) ABSOLUTE ADDRESSING (NON-BRANCH INSTRUCTIONS)



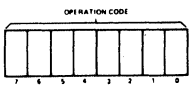
(B) ABSOLUTE ADDRESSING (BRANCH INSTRUCTIONS)



INDIRECT ADDRESSING



(E) MISCELLANEOUS INSTRUCTIONS

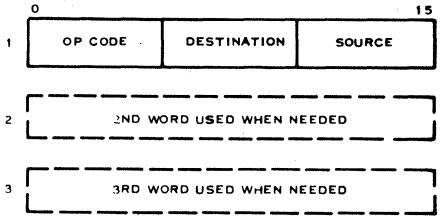


*INDEX CONTROL
00 - NON-INDEXED
01 - INDEXED WITH AUTO-INCREMENT
10 - INDEXED WITH AUTO-DECREMENT
11 - INDEXED ONLY

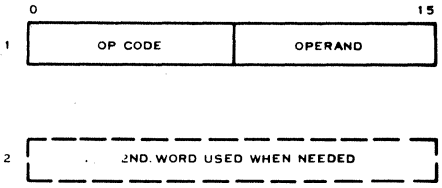
16. INSTRUCTION FORMAT DRAWINGS

IN DRAWING NUMBER SEQUENCE

F5

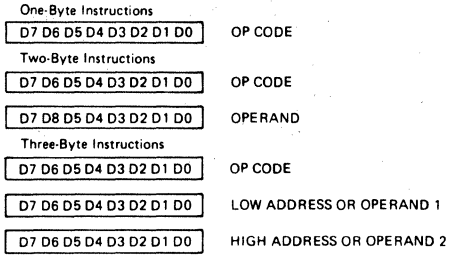


Two Address Instruction Format

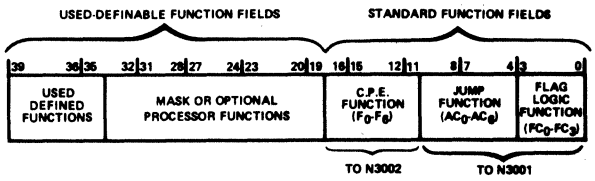


Single Address Instruction Format

F7



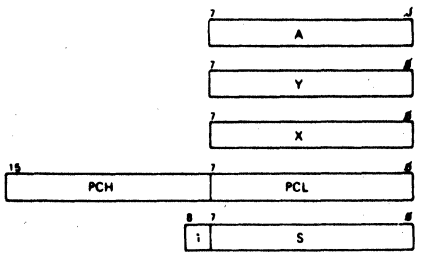
F8



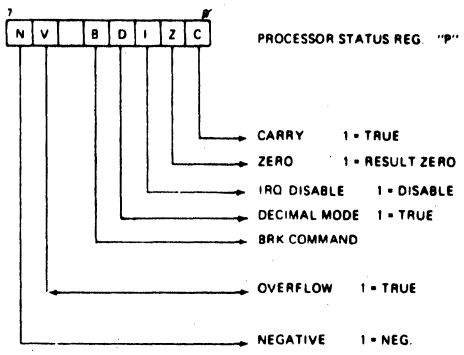
Note: The mask field need only be used during masking operations. At other times, it is entirely user definable.

F9

PROGRAMMING MODEL

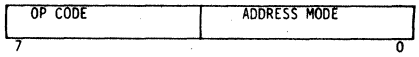


ACCUMULATOR	A
INDEX REGISTER	Y
INDEX REGISTER	X
PROGRAM COUNTER	"PC"
STACK POINTER	"S"

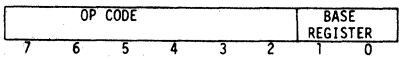


F10

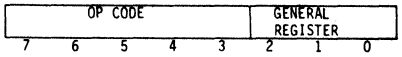
1. Arithmetic and logical instructions.



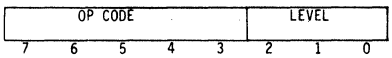
2. Base register instructions.



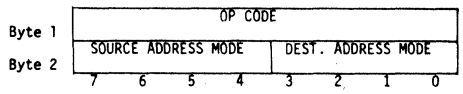
3. General register instructions.



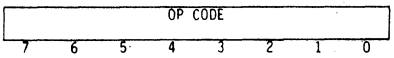
4. Interrupt level instructions.



5. Move instructions.



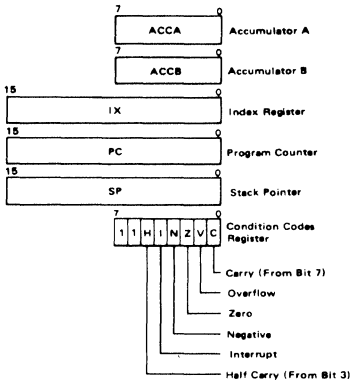
6. General machine instructions.



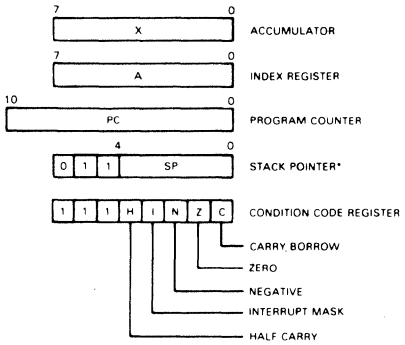
16. INSTRUCTION FORMAT DRAWINGS

IN DRAWING NUMBER SEQUENCE

F11



F11

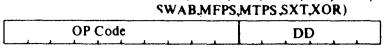


*STACK POINTER IS INITIALIZED TO $7F ON RESET

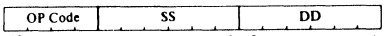
F11a

F13

Single Operand Group (CLR,CLRB,COM,COMB,INC,INCB, DEC,DECB,NEG,NEGB,ADC,ADCB, SBC,SBCB,TST,TSTB,ROR,RORB, ROL,ROLB,ASR,ASRB,ASL,ASLB,JMP, SWAB,MFPS,MTPS,SXT,XOR)

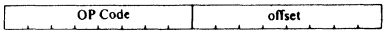


Double Operand Group (BIT,BITB,BIC,BICB,BIS,BISB,ADD, SUB MOV,MOVB,CMP,CMPB)

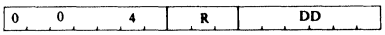


Program Control Group

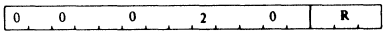
a. Branch (all branch instructions)



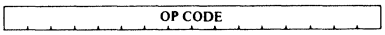
b. Jump To Subroutine (JSR)



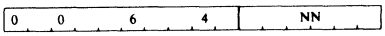
c. Subroutine Return (RTS)



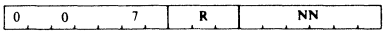
d. Traps (break point, IOT,EMT,TRAP,BPT)



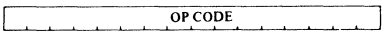
e. Mark (MARK)



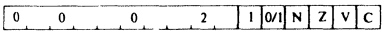
f. Subtract 1 and branch (if ≠ 0) (SOB)



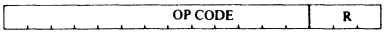
Operate Group (HALT,WAIT,RTI,RESET,RTT,NOP)



Condition Code Operators (all condition code instructions)

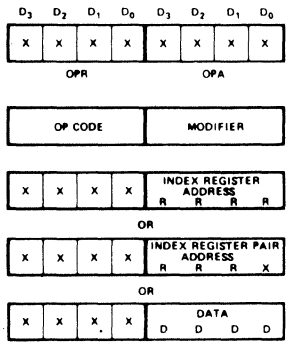


Fixed and Floating Point Arithmetic (optional EIS/FIS)(FADD, FSUB,FMUL,FDIV,MUL, DIV,ASH,ASHC)

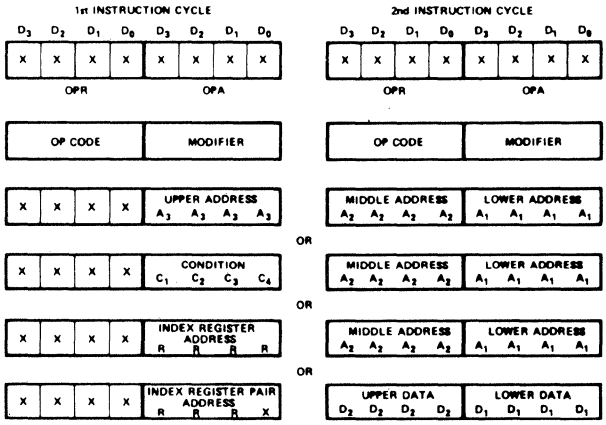


F14

ONE WORD INSTRUCTIONS

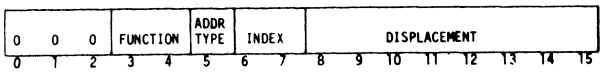


TWO WORD INSTRUCTIONS

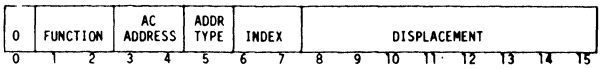


F15

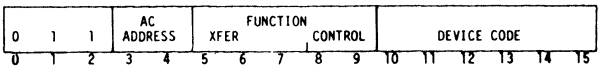
JUMP AND MODIFY MEMORY INSTRUCTION



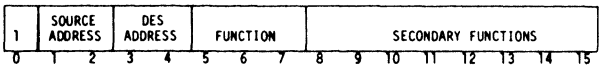
MOVE DATA INSTRUCTION



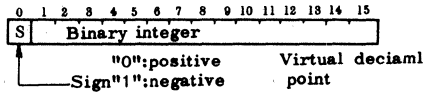
INPUT/OUTPUT INSTRUCTION



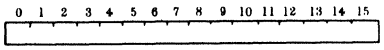
ARITHMETIC AND LOGIC INSTRUCTION



F17

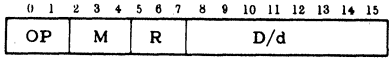


Binary fixed point number format



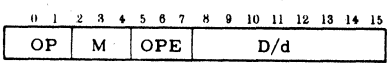
Logical arithmetic data format

Register - Memory transfer



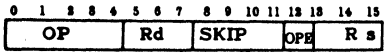
(R ≠ 110,111)

Memory operation or Branch operation

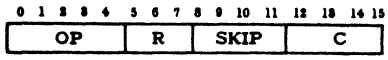


(OPE=110,111)

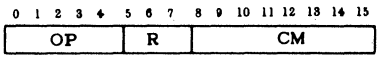
RR-type instruction (Register-Register operation)



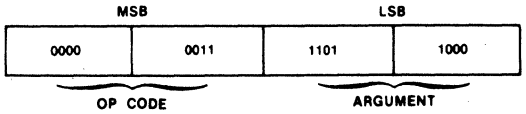
RC-type instruction (Register Change operation)



RCM-typel instruction (Register-Command operation)



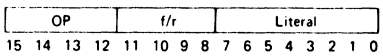
F18



F19

Literal Commands

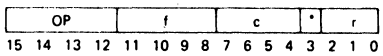
The literal class commands with OP codes of 1 to 6 have the following format:



In this format the operation code occupies the four high order bits. Bits 11-8 contain either a file register designator (f) or a register or control group designator (r). Bits 7-0 contain an eight-bit literal which is transferred as an operand to the B-bus.

Operate Commands

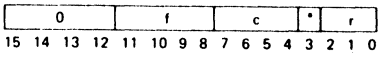
The operate class commands with OP codes of 7 to F have the following format:



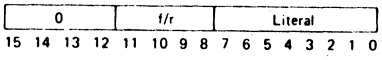
Executive Command (OP code 0)

The execute command causes the contents of the U register to be ORed with the eight high order bits of the command to form an effective command. This operation is also performed when r = 7 for the operate class commands. The execute command has zero-bits in the four high order bits. The remainder of the command has the format required for the effective command to be executed.

Formats for Executive Commands

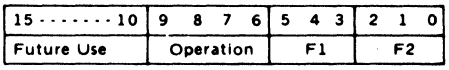


If U contains Operate command OP code.



If U contains Literal command OP code.

F20



16. INSTRUCTION FORMAT DRAWINGS

IN DRAWING NUMBER SEQUENCE

F22

OPERATION FORM I

FUNCTION	OP3 → OP0	D1 D0	S2 S1 S0
a. RF ALU WR → RF	ALU: LLLL → HHHH	L L	RF: LLL → HHH
b. RF ALU WR → WR	ALU: LLLL → HHHH	L H	RF: LLL → HHH
c. *DIB ALU WR → DOB	ALU: LLLL → HHHH	H H	L L L
d. *DIB ALU WR → WR	ALU: LLLL → HHHH	H H	L L H
e. DIB ALU XWR → WR	ALU: LLLL → HHHH	H H	L H H
f. DIB ALU WR → XWR	ALU: LLLL → HHHH	H H	H L L
g. DIB ALU XWR → XWR	ALU: LLLL → HHHH	H H	H H L
h. DIB ALU XWR → DOB	ALU: LLLL → HHHH	H H	H H H

NOTE: When PC PRIORITY is low WR → AOB.
*XWR → AOB.

OPERATION FORM II

FUNCTION	OP3 → OP0	D1 D0	S2 S1 S0
a. RF plus WR plus ALUCIN → XWR	L L H H	H L	RF: LLL → HHH
b. RF plus DIB plus ALUCIN → WR	L H L L	H L	RF: LLL → HHH
c. RF plus DIB plus ALUCIN → XWR	L H L H	H L	RF: LLL → HHH
d. RF plus DIB plus ALUCIN → RF	L H H H	H L	RF: LLL → HHH
e. RF plus XWR plus ALUCIN → WR	H H L L	H L	RF: LLL → HHH
f. RF plus XWR plus ALUCIN → XWR	H H L H	H L	RF: LLL → HHH
g. XWR plus ALUCIN → RF	H H H L	H L	RF: LLL → HHH
h. DIB plus WR plus ALUCIN → XWR	L L H H	H H	L H L
i. DIB plus WR plus ALUCIN → DOB	L H H H	H H	L H L
j. DIB plus XWR plus ALUCIN → WR	H H L L	H H	L H L
k. DIB plus XWR plus ALUCIN → XWR	H H L H	H H	L H L
l. XWR plus ALUCIN → DOB	H H H L	H H	L H L

OPERATION FORM III

FUNCTION	OP3 → OP0	D1 D0	S2 S1 S0
a. DIB → RF	H H H H	H L	RF: LLL → HHH
b. RF → DOB	L L L L	H L	RF: LLL → HHH
c. RF → XWR	L L L H	H L	RF: LLL → HHH
d. DIB → WR	L H H L	H L	X X X
	L H H L	H H	L H L
e. DIB → XWR	L L L H	H H	L H L
f. DIB → DOB	H H H H	H H	L H L
	L L L L	H H	L H L

OPERATION FORM IV

FUNCTION	OP3→OP0	D1 D0	S2 S1 S0
a. (WR minus DIB minus 1 plus ALUCIN) LCIR → WR, XWR	H L L L	H H	L H L
b. (WR plus DIB plus ALUCIN) LCIR → WR, XWR	H L L H	H H	L H L
c. (WR minus RF minus 1 plus ALUCIN) LCIR → WR, XWR	H L L L	H L	RF: LLL → HHH
d. (WR plus RF plus ALUCIN) LCIR → WR, XWR	H L L H	H L	RF: LLL → HHH
	H L H L	H L	X X X
e. (WR plus ALUCIN) RSA → WR, XWR	H L H L	H H	L H L
f. (WR minus DIB minus 1 plus ALUCIN) RSA → WR, XWR	L L H L	H H	L H L
g. (WR plus DIB plus ALUCIN) RSA → WR, XWR	H L H H	H H	L H L
h. (WR minus RF minus 1 plus ALUCIN) RSA → WR, XWR	L L H L	H L	RF: LLL → HHH
i. (WR plus RF plus ALUCIN) RSA → WR, XWR	H L H H	H L	RF: LLL → HHH

OPERATION FORM V

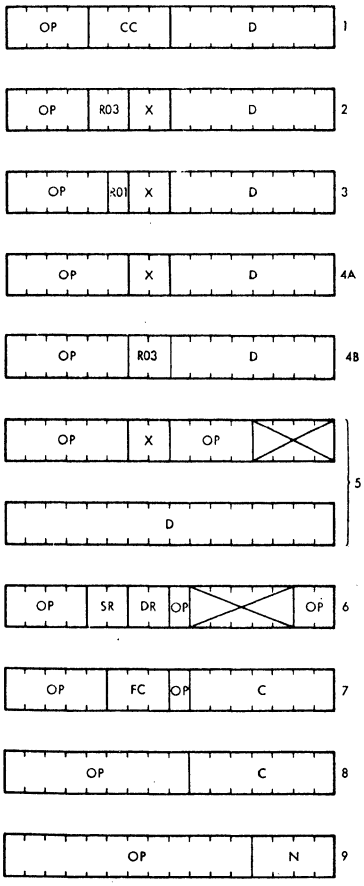
FUNCTION	OP3 → OP0	D1 D0	S2 S1 S0
a. (WR plus ALUCIN) RSA → WR	L L L L	H H	H L H
b. (WR plus ALUCIN) RCIR → WR	L L L H	H H	H L H
c. (WR plus ALUCIN) LSA → WR	H L L H	H H	H L H
d. (WR plus ALUCIN) LCIR → WR	L L H L	H H	H L H
e. (WR plus ALUCIN) RSL → WR	L L H H	H H	H L H
f. (WR plus ALUCIN) LSL → WR	H L L L	H H	H L H
	H L H L	H H	H L H

OPERATION FORM VI

FUNCTION	OP3 → OP0	D1 D0	R2 R1 R0
a. (WR plus ALUCIN, XWR) RSA → (WR, XWR)	L H L L	H H	H L H
b. (WR plus ALUCIN, XWR) RICR → (WR, XWR)	L H L H	H H	H L H
c. (WR plus ALUCIN, XWR) LSA → (WR, XWR)	H H L H	H H	H L H
d. (WR plus ALUCIN, XWR) LCIR → (WR, XWR)	L H H L	H H	H L H
e. (WR plus ALUCIN, XWR) RSL → (WR, XWR)	L H H H	H H	H L H
f. (WR plus ALUCIN, XWR) LSL → (WR, XWR)	H H L L	H H	H L H
	H H H L	H H	H L H

Alphabetical listing of all source operands are provided in Tables X, Y, Z, and AA.

F23



DEFINITIONS

OP - OPERATION CODE
D - DISPLACEMENT
R03 - AC0, AC1, AC2 OR AC3
R01 - AC0 OR AC1
X - INDEX REGISTER
- 0 - BASE
- 1 - PROGRAM COUNTER
- 2 - AC2
- 3 - AC3

PC - PROGRAM COUNTER
EA - EFFECTIVE ADDRESS
- IF X = 0, EA = D
- IF X = 1, EA = (PC) + D
- IF X = 2, EA = (AC2) + D
- IF X = 3, EA = (AC3) + D

SR - SOURCE REGISTER (AC0, AC1, AC2 OR AC3)
DR - DESTINATION REGISTER (AC0, AC1, AC2 OR AC3)
IEF - INTERRUPT ENABLE FLIP FLOP
SEL - "SELECT" CONTROL FLAG
FC - CONTROL FLAG CODE
- 0 - FB
- 1 - IEF
- 2 - SEL
- 3 - F11
- 4 - F12
- 5 - F13
- 6 - F14
- 7 - F15

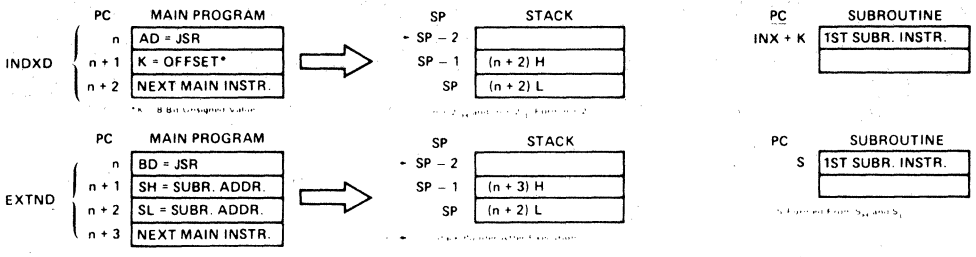
C - CONTROL CODE
N - BIT NUMBER
CC - CONDITION CODE
- 0 - INTERRUPT
- 1 - (AC0) = 0
- 2 - (AC0) ≥ 0
- 3 - BIT 0 OF (AC0) = 1
- 4 - BIT 1 OF (AC0) = 1
- 5 - (AC0) ≠ 0
- 6 - CONTROL PANEL INTERRUPT
- 7 - CONTROL PANEL START
- 8 - STACK FULL
- 9 - (IEF) = 1
- 10 - CARRY = 1 [(SEL) = 0] OVERFLOW = 1 [(SEL) = 1]
- 11 - (AC0) ≤ 0
- 12 - U1
- 13 - U2
- 14 - U3
- 15 - U4

L - LINK FLIP FLOP
STK - PUSHDOWN STACK
SF - STATUS FLAG REGISTER

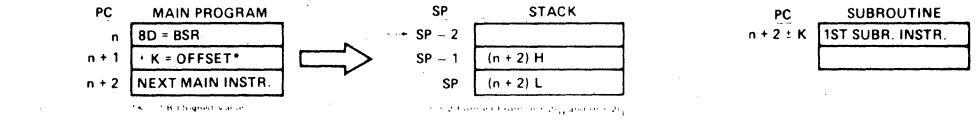
F25

SPECIAL OPERATIONS

JSR, JUMP TO SUBROUTINE:

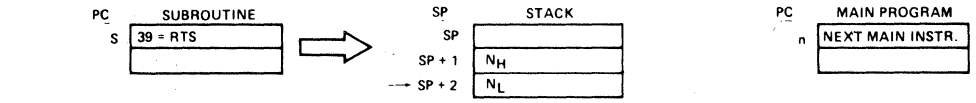


BSR, BRANCH TO SUBROUTINE:



JMP, JUMP:

RTS, RETURN FROM SUBROUTINE:



RTI, RETURN FROM INTERRUPT:

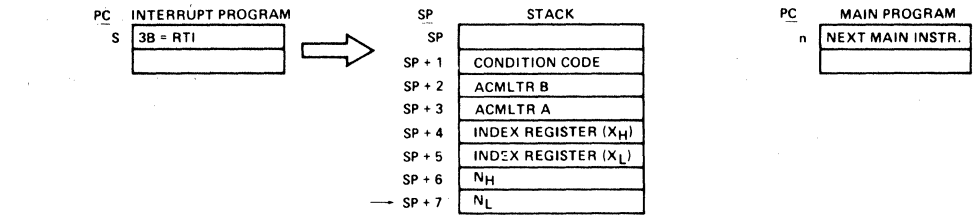


TABLE 6 – CONDITION CODE REGISTER MANIPULATION INSTRUCTIONS

OPERATIONS	MNEMONIC	IMPLIED			BOOLEAN OPERATION	COND. CODE REG.					
		OP	~	#		5	4	3	2	1	0
						H	I	N	Z	V	C
Clear Carry	CLC	0C	2	1	0 → C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0 → I	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0 → V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1 → C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1 → I	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1 → V	•	•	•	•	S	•
Acmltr A → CCR	TAP	06	2	1	A → CCR	(12)					
CCR → Acmltr A	TPA	07	2	1	CCR → A	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES: (Bit set if test is true and cleared otherwise)

1 (Bit V) Test: Result = 10000000?

2 (Bit C) Test: Result = 00000000?

3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)

4 (Bit V) Test: Operand = 10000000 prior to execution?

5 (Bit V) Test: Operand = 01111111 prior to execution?

6 (Bit V) Test: Set equal to result of N + C after shift has occurred.

7 Bit N) Test: Sign bit of most significant (MS) byte = 1?

8 (Bit V) Test: 2s complement overflow from subtraction of MS bytes?

9 (Bit N) Test: Result less than "0"? (Bit 15 = 1)

10 (All) Load Condition Code Register from Stack. (See Special Operations)

11 (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt is required to exit the wait state.

12 (All) Set according to the contents of Accumulator A.

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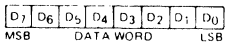
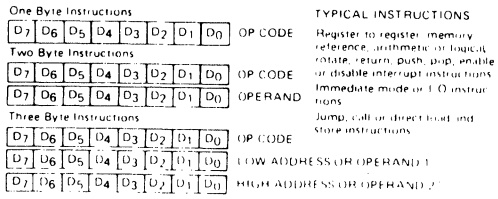
DATA AND INSTRUCTION FORMATS

Data in the μPD8080A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

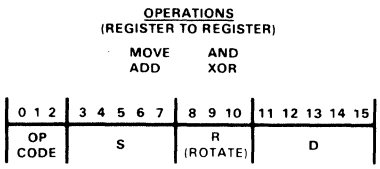


Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

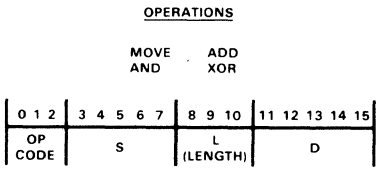


F27

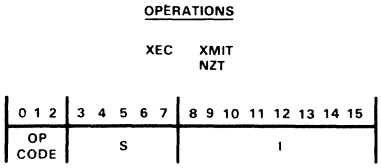
INSTRUCTION FORMATS



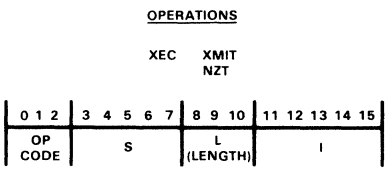
Type I



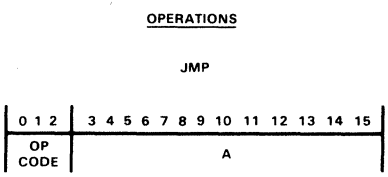
Type II



Type III



Type IV



Type V

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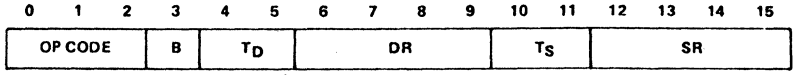
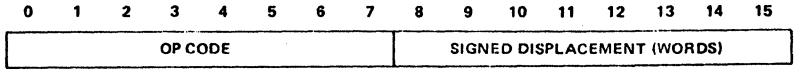
FORMAT 1 INSTRUCTION.

GENERAL FORMAT:

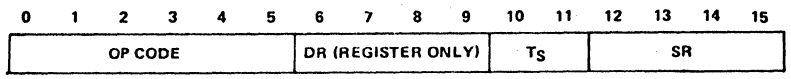


GENERAL FORMAT:



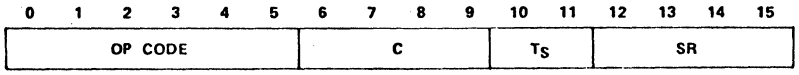
FORMAT 3/9 INSTRUCTIONS

General Format:



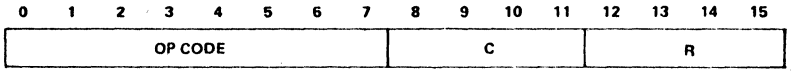
FORMAT 4 (CRU MULTIBIT) INSTRUCTIONS

GENERAL FORMAT:



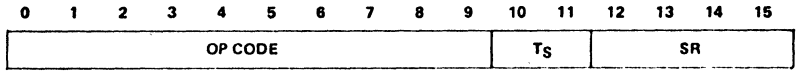
FORMAT 5 (SHIFT) INSTRUCTIONS

General Format:



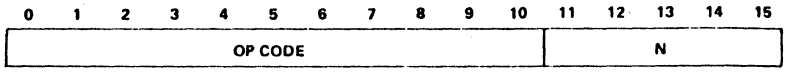
FORMAT 6 INSTRUCTIONS

General Format:



FORMAT 7 (RTWP, CONTROL) INSTRUCTIONS

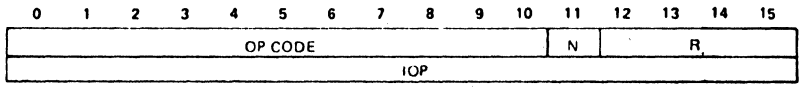
General Format:



FORMAT 8 (IMMEDIATE, INTERNAL REGISTER LOAD/STORE) INSTRUCTIONS

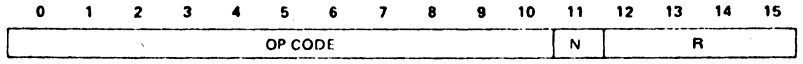
Immediate Register Instructions

General format:



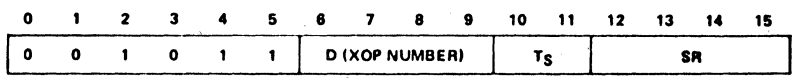
Internal Register Store Instructions

General format:



FORMAT 9 (XOP) INSTRUCTION

General Format:



F29

Flags

Control Register R252 contains the following six flags:

C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

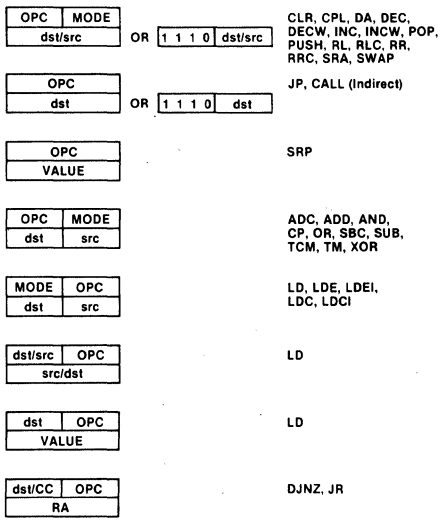
0	Cleared to zero
1	Set to one
*	Set or cleared according to operation
–	Unaffected
X	Undefined

Condition Codes

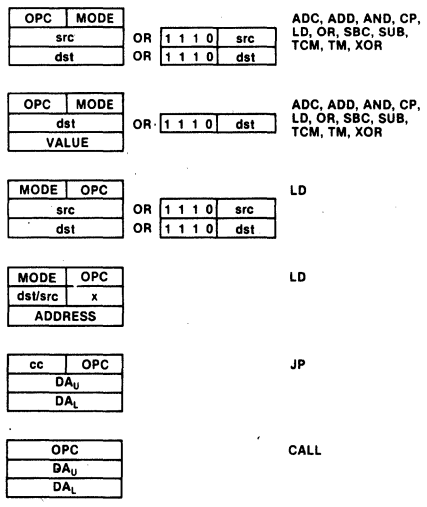
Condition Codes Value	Mnemonic	Meaning	Flags Set
1000		Always true	---
0111	C	Carry	C = 1
1111	NC	No carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000		Never true	---

Instruction Formats

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

MEMORY REFERENCE INSTRUCTIONS

MNE-MONIC	OP CODE	OPERATION	NUMBER OF STATES
AND	0_8	**LOGICAL AND DIRECT (I = 0)** **Operation: (AC) ← —(AC) ∧ (EA)** **Description: Contents of the EA are logically AND'ed with the contents of the AC and the result is stored in AC.**	10
		LOGICAL AND INDIRECT (I = 1, PA ≠ 0010-0017$_8$) **Operation: (AC) ← —(AC) ∧ ((PA))**	15
		LOGICAL AND AUTOINDEX (I = 1, PA = 0010-0017$_8$) **Operation: (PA) ← —(PA) + 1; (AC) ← —(AC) ∧ ((PA))**	16
TAD	1_8	BINARY ADD DIRECT (I = 0) Operation: (AC) ← —(AC) + (EA) Description: Contents of the EA are ADD'ed with the contents of the AC and the result is stored in the AC; carry out complements the LINK. If AC is initially cleared, this instruction acts as LOAD from Memory	10
		BINARY ADD INDIRECT (I = 1, PA ≠ 0010-0017$_8$) Operation: (AC) ← —(AC) + ((PA))	15
		BINARY ADD AUTOINDEX (I = 1, PA = 0010-0017$_8$) Operation: (PA) ← —(PA) + 1; (AC) ← —(AC) + ((PA))	16
ISZ	2_8	**INCREMENT AND SKIP IF ZERO DIRECT (I = 0)** **Operation: (EA) ← —(EA) +1; if (EA) = 0000$_8$, PC ← —PC + 1** **Description: Contents of the EA are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.**	16
		INCREMENT AND SKIP IF ZERO INDIRECT (I = 1, PA ≠ 0010-0017$_8$) **Operation: ((PA)) ← —((PA)) + 1; if ((PA)) = 0000$_8$, PC ← —PC + 1**	21
		INCREMENT AND SKIP IF ZERO AUTOINDEX (I = 1, PA = 0010-0017$_8$) **Operation: (PA) ← —(PA) +1; ((PA)) ← —((PA)) + 1; if ((PA)) = 0000$_8$, PC ← —PC + 1**	22
DCA	3_8	DEPOSIT AND CLEAR THE ACCUMULATOR DIRECT (I = 0) Operation: (EA) ← —(AC); (AC) ← —0000$_8$ Description: The contents of the AC are stored in EA and the AC is cleared.	11
		DEPOSIT AND CLEAR THE ACCUMULATOR INDIRECT (I = 1, PA ≠ 0010-0017$_8$) Operation: ((PA)) ← —(AC); (AC) ← —0000$_8$	16
		DEPOSIT AND CLEAR THE ACCUMULATOR AUTOINDEX (I = 1, PA = 0010-0017$_8$) Operation: (PA) ← —(PA) + 1; ((PA)) ← —(AC); (AC) ← —0000$_8$	17
JMS	4_8	**JUMP TO SUBROUTINE DIRECT (I = 0)** **Operation: (EA) ← —(PC), (PC) ← —EA + 1** **Description: The contents of the PC are stored in the EA. The PC is incremented by 1 immediately after every instruction fetch. The contents of the EA now point to the next sequential instruction following the JMS (return address). The next instruction is taken from EA + 1.**	11
		JUMP TO SUBROUTINE INDIRECT (I = 1, PA ≠ 0010-0017$_8$) **Operation: ((PA)) ← —PC, (PC) ← —(PA) + 1**	16
		JUMP TO SUBROUTINE AUTOINDEX (I = 1, PA = 0010-0017$_8$) **Operation: (PA) ← —(PA) + 1; ((PA)) ← —PC, (PC) ← —(PA) + 1**	17
JMP	5_8	JUMP DIRECT (I = 0) Operation: (PC) ← —EA Description: The next instruction is taken from the EA.	10
		JUMP INDIRECT (I = 1, PA ≠ 0010-0017$_8$) Operation: (PC) ← —(PA)	15
		JUMP AUTOINDEX (I = 1, PA = 0010-0017$_8$) Operation: (PA) ← —(PA) + 1; (PC) ← —(PA)	16

GROUP 1 OPERATION MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES
NOP	**7000**	**1**	**NO OPERATION—This instruction causes a 10 state delay in program execution, without affecting the state of the IM6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.**	10
IAC	7001	3	INCREMENT ACCUMULATOR—The content of the AC is incremented by one (1) and carry out complements the Link (L).	10
RAL	**7004**	**4**	**ROTATE ACCUMULATOR LEFT—The contents of the AC and L are rotated one binary position to the left. AC (0) is shifted to L and L is shifted to AC (11).**	15
RTL	7006	4	ROTATE TWO LEFT—The contents of the AC and L are rotated two binary positions to the left. AC (1) is shifted to L and L is shifted to AC (10).	15
RAR	**7010**	**4**	**ROTATE ACCUMULATOR RIGHT—The content of the AC and L are rotated one binary position to the right. AC (11) is shifted to L and L is shifted to AC (0).**	15
RTR	7012	4	ROTATE TWO RIGHT—The contents of the AC and L are rotated two binary positions to the right. AC (10) is shifted to L and L is shifted to AC (1).	15
BSW	**7002**	**4**	**BYTE SWAP—The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC (0) is swapped with AC (6), AC (1) with AC (7), etc. L is not affected.**	15
CML	7020	2	COMPLEMENT LINK—The content of the link is complemented.	10
CMA	**7040**	**2**	**COMPLEMENT ACCUMULATOR—The content of each bit of the AC is complemented having the effect of replacing the content of the AC with its one's complement.**	10
CIA	7041	2,3	COMPLEMENT AND INCREMENT ACCUMULATOR—The content of the AC is replaced with its two's complement. Carry out complements the LINK.	10
CLL	**7100**	**1**	**CLEAR LINK—The link is loaded with a binary 0.**	**10**
CLL RAL	7104	1,4	CLEAR LINK—ROTATE ACCUMULATOR LEFT.	15
CLL RTL	**7106**	**1,4**	**CLEAR LINK—ROTATE TWO LEFT.**	**15**
CLL RAR	7110	1,4	CLEAR LINK—ROTATE ACCUMULATOR RIGHT.	15
CLL RTR	**7112**	**1,4**	**CLEAR LINK—ROTATE TWO RIGHT.**	**15**
STL	7120	1,2	SET THE LINK—The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.	10
CLA	**7200**	**1**	**CLEAR ACCUMULATOR—The accumulator is loaded with binary 0's.**	**10**
CLA IAC	7201	1,3	CLEAR ACCUMULATOR—INCREMENT ACCUMULATOR.	10
GLT	**7204**	**1,4**	**GET THE LINK—The AC is cleared; the content of L is shifted into AC (11), a 0 is shifted into L. This is a microprogrammed combination of CLA and RAL.**	**15**
CLA CLL	7300	1	CLEAR ACCUMULATOR—CLEAR LINK.	10
STA	**7240**	**1,2**	**SET THE ACCUMULATOR—Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.**	**10**

Cont'd on next page

IS3 Cont'd

IS3 Cont'd

GROUP 2 OPERATE MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES
NOP	**7400**	**1**	**NO OPERATION**—See GROUP 1 MICROINSTRUCTIONS	**10**
HLT	7402	3	HALT—Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.	10
OSR	**7404**	**3**	**OR WITH SWITCH REGISTER**—The content of the Switch Register if OR'ed with the content of the AC and the result is stored in the AC. The OSR INSTRUCTION TIMING is shown in Figure 8. The IM6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B.	15
SKP	7410	1	SKIP—The content of the I C is incremented by 1, to skip the next sequential instruction.	10
SNL	**7420**	**1**	**SKIP ON NON-ZERO LINK**—The content of L is sampled, the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.	**10**
SZL	7430	1	SKIP ON ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 0. If the L contains a 1, the next instruction is executed.	10
SZA	**7440**	**1**	**SKIP ON ZERO ACCUMULATOR**—The content of the AC is sampled; the next sequential instruction is skipped if the AC has all bits which are 0. If any bit in the AC is a 1, the next instruction is executed.	**10**
SNA	7450	1	SKIP ON NON-ZERO ACCUMULATOR—The content of the AC is sampled, the next sequential instruction is skipped if the AC has any bits which are not 0. If every bit in the AC is 0, the next instruction is executed.	10
SZA SNL	**7460**	**1**	**SKIP ON ZERO ACCUMULATOR, *OR* SKIP ON NON-ZERO LINK, *OR* BOTH**	**10**
SNA SZL	7470	1	SKIP ON NON-ZERO ACCUMULATOR ***AND*** SKIP ON ZERO LINK	10
SMA	**7500**	**1**	**SKIP ON MINUS ACCUMULATOR**—If the content of AC (0) contains a 1, indicating that the AC contains a negative two's complement number, the next sequential instruction is skipped. If AC (0) contains a 0, the next instruction is executed.	**10**
SPA	7510	1	SKIP ON POSITIVE ACCUMULATOR—The contents of AC (0) are sampled. If AC (0) contains a 0, indicating that the AC contains a positive two's complement number, the next sequential instruction is skipped. If AC (0) contains a 1, the next instruction is executed.	10
SMA SNL	**7520**	**1**	**SKIP ON MINUS ACCUMULATOR *OR* SKIP ON NON-ZERO LINK *OR* BOTH**	**10**
SPA SZL	7530	1	SKIP ON POSITIVE ACCUMULATOR ***AND*** SKIP ON ZERO LINK	10
SMA SZA	**7540**	**1**	**SKIP ON MINUS ACCUMULATOR *OR* SKIP ON ZERO ACCUMULATOR *OR* BOTH**	**10**
SPA SNA	7550	1	SKIP ON POSITIVE ACCUMULATOR ***AND*** SKIP ON NON-ZERO ACCUMULATOR	10
SMA SZA SNL	**7560**	**1**	**SKIP ON MINUS ACCUMULATOR *OR* SKIP ON ZERO ACCUMULATOR *OR* SKIP ON NON-ZERO LINK *OR* ALL**	**10**
SPA SNA SZL	7570	1	SKIP ON POSITIVE ACCUMULATOR ***AND*** SKIP ON NON-ZERO ACCUMULATOR ***AND*** SKIP ON ZERO LINK	10
CLA	**7600**	**2**	**CLEAR ACCUMULATOR**—The AC is loaded with binary 0's.	**10**
LAS	7604	1,3	LOAD ACCUMULATOR WITH SWITCH REGISTER—The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.	15
SZA CLA	**7640**	**1,2**	**SKIP ON ZERO ACCUMULATOR *THEN* CLEAR ACCUMULATOR**	**10**
SNA CLA	7650	1,2	SKIP ON NON-ZERO ACCUMULATOR ***THEN*** CLEAR ACCUMULATOR	10
SMA CLA	**7700**	**1,2**	**SKIP ON MINUS ACCUMULATOR *THEN* CLEAR ACCUMULATOR**	**10**
SPA CLA	7710	1,2	SKIP ON POSITIVE ACCUMULATOR ***THEN*** CLEAR ACCUMULATOR	10

GROUP 3 OPERATE MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES
NOP	**7401**	**3**	**NO OPERATION**—See Group 1 Microinstructions	**10**
MQL	7421	2	MQ REGISTER LOAD—The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost	10
MQA	**7501**	**2**	**MQ REGISTER INTO ACCUMULATOR**—The content of the MQ is OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.	**10**
SWP	7521	3	SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are interchanged accomplishing a microprogrammed combination of MQA and MQL	10
CLA	**7601**	**1**	**CLEAR ACCUMULATOR**	**10**
CAM	7621	3	CLEAR ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogrammed combination of CLA and MQL	10
ACL	**7701**	**3**	**CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR**—This is equivalent to a microprogrammed combination of CLA and MQA.	**10**
CLA SWP	7721	3	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared	10

PROCESSOR IOT INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON—If Interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.
ION	6001	INTERRUPT TURN ON—The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction. The INTERRUPT ENABLE TIMING is shown in Figure 13
IOF	6002	INTERRUPT TURN OFF—The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request
SRQ	6003	SKIP IF INT REQUEST—The next sequential instruction is skipped if the INT request bus is low
GTF	6004	GET FLAGS—The following machine states are read into the indicated bits of AC. bit 0—Link bit 2—INT request bus bit 4—Interrupt Enable FF Other bits may be modified by external inputs (ex. Extended memory control).
RTF	6005	RETURN FLAGS—Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states (ex. Extended memory control)
SGT	6006	Operation is determined by external devices, if any.
CAF	6007	CLEAR ALL FLAGS—AC and Link are cleared. Interrupt system is disabled

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS5

OP CODE	MNEMONIC	DESCRIPTION	TIME IS5	TIME IS5a
Register Instructions				
11111RRR	LDR	Load ACC from R	2.75 us	.875 us
11101RRR	SBR	Subtract R from ACC	3.25	.875
11011RRR	ACR	Add R and CY to ACC	3.50	.875
11001RRR	ADR	Add R to ACC	3.25	.875
10111RRR	ANR	And R with ACC	2.75	.875
10101RRR	IOR	Inclusive Or R with ACC	2.75	.875
10011RRR	XOR	Exclusive Or R with ACC	2.75	.875
01101RRR	STR	Store ACC into R	3.75	1.00
00011RRR	INR	Increment R	3.25	.875
01000RRR AAAAAAAA AAAAAAAA	DJP	Decrement R. If result is ≠ -1, jump to A	4.00 - 6.00	.875 - 1.50
01001RRR BBBBBBBB	DSP	Decrement R. If result is ≠ -1, add B to PC. (-128 ≦ B ≦ +127)	3.75 - 5.75	.875 - 1.50
10001RRR	MLR	Multiply ACC by R	14.50 - 18.50	3.25 - 4.25
01111RRR	DVR	Divide ACC by R	17.50 - 21.50	3.50 - 4.50
Immediate Instructions				
11110000 DDDDDDDD	LDI	Load D into ACC	4.00 us	1.125 us
11100000 DDDDDDDD	SBI	Subtract D from ACC	4.50	1.125
11010000 DDDDDDDD	ACI	Add D and CY to ACC	4.75	1.125
11000000 DDDDDDDD	ADI	Add D to ACC	4.50	1.125
10110000 DDDDDDDD	ANI	And D with ACC	4.00	1.125
10100000 DDDDDDDD	IOI	Inclusive Or D with ACC	4.00	1.125
10010000 DDDDDDDD	XOI	Exclusive Or D with ACC	4.00	1.125
10000000 DDDDDDDD	MLI	Multiply ACC by D	15.75-19.75	3.75 - 4.75
01110000 DDDDDDDD	DVI	Divide ACC by D	18.75-22.75	4.00 - 5.00
Memory Reference Instructions				
11110100 AAAAAAAA AAAAAAAA	LDA	Load ACC from M(A)	6.00 us	1.50 us
111101QQ	LDN	Load ACC from M((Q)) Increment Q	5.25	1.25
11110000 CCCCCCCC	LDB	Load ACC from M((Q)+C)	5.75	1.50
11110000 11111111	LDX	Load ACC from M((Q)+(RO))	6.25	1.50
11100100 AAAAAAAA AAAAAAAA	SBA	Subtract M(A) from ACC	6.50 us	1.5 us
111001QQ	SBN	Subtract M((Q)) from ACC Increment Q	5.75	1.25
11100000 CCCCCCCC	SBB	Subtract M((Q)+C) from ACC	6.25	1.5
11100000 11111111	SBX	Subtract M((Q)+(RO)) from ACC	6.75	1.5
11010100 AAAAAAAA AAAAAAAA	ACA	Add M(A) and CY to ACC	6.75	1.5
110101QQ	ACN	Add M((Q)) and CY to ACC, Increment Q	6.00	1.25
11010000 CCCCCCCC	ACB	Add M((Q)+C) and CY to ACC	6.50	1.5
11010000 11111111	ACX	Add M((Q)+(RO)) and CY to ACC	6.50	1.5
11000100 AAAAAAAA AAAAAAAA	ADA	Add M(A) to ACC	6.50	1.5
110001QQ	ADN	Add M((Q)) to ACC, Increment Q	5.75	1.25
11000000 CCCCCCCC	ADB	Add M((Q)+C) to ACC	6.26	1.5
11000000 11111111	ADX	Add M((Q)+(RO)) to ACC	6.75	1.5
10110100 AAAAAAAA AAAAAAAA	ANA	And M(A) with ACC	6.00	1.5
101101QQ	ANN	And M((Q)) with ACC, Increment Q	5.25	1.25
10110000 CCCCCCCC	ANB	And M((Q)+C) with ACC	5.75	1.5
10110000 11111111	ANX	And M((Q+(RO)) with ACC	6.25	1.5
10100100 AAAAAAAA AAAAAAAA	IOA	Inclusive Or M(A) with ACC	6.00	1.5
101001QQ	ION	Inclusive Or M((Q)) with ACC Increment Q	5.25	1.25
10100000 CCCCCCCC	IOB	Inclusive Or M((Q)+C)with ACC	5.75	1.5
10100000 11111111	IOX	Inclusive Or M((Q)+(RO)) with ACC	6.25	1.5

IS5

OP CODE	MNEMONIC	DESCRIPTION	Time(us) IS5	Time(us) IS5a
Memory Reference Instructions (cont)				
10010100 AAAAAAAA AAAAAAAA	XOA	Exclusive Or M(A) with ACC	6.00 us	1.50 us
100101QQ	XON	Exclusive Or M((Q)) with ACC Increment Q	5.25	1.25
10010000 CCCCCCCC	XOB	Exclusive Or M((Q)+C) with ACC	5.75	1.5
10010000 11111111	XOX	Exclusive Or M((Q)+(RO)) with ACC	6.25	1.5
10000100 AAAAAAAA AAAAAAAA	MLA	Multiply ACC by M(A)	17.75-21.75	4.0 - 5.0
100001QQ	MLN	Multiply ACC by M((Q)), Increment Q	17.00-21.00	3.75 - 4.75
10000000 CCCCCCCC	MLB	Multiply ACC by M((Q)+C)	17.50-21.50	4.0 - 5.0
10000000 11111111	MLX	Multiply ACC by M((Q)+(RO))	18.00-22.00	4.0 - 5.0
01110100 AAAAAAAA AAAAAAAA	DVA	Divide ACC by M(A)	20.75 - 24.75	4.25 - 5.25
011101QQ	DVN	Divide ACC by M((Q)), Increment Q	20.00 - 24.00	4.0 - 5.0
01110000 CCCCCCCC	DVB	Divide ACC by M((Q)+C)	20.50 - 24.50	4.25 - 5.25
01110000 11111111	DVX	Divide ACC by M((Q)+(RO))	21.00 - 25.00	4.25 - 5.25
01100100 AAAAAAAA AAAAAAAA	STA	Store ACC at M(A)	7.50	1.75
011001QQ	STN	Store ACC at M((Q)), Increment Q	6.57	1.5
01100000 CCCCCCCC	STB	Store ACC at M((Q)+C)	7.25	1.75
01100000 11111111	STX	Store ACC at M((Q) + (RO))	7.75	1.75
Move Instructions				
01100000 1SSS1RRR	MRR	R ←(S)	7.50 us	1.75 us
01100000 1SSS0100 AAAAAAAA AAAAAAAA	MRA	A ←(S)	11.25	2.5
01100000 1SSS00QQ CCCCCCCC	MRB	M((Q)+C) ← (S)	11.00	2.5
01100000 1SSS00QQ 11111111	MRX	M((Q)+(RO)) ←(S)	11.50	2.5
01100000 1SSS01QQ	MRN	M((Q))←(S), Increment Q	10.50 us	2.25 us
01100000 00001RRR DDDDDDDD	MIR	R← D	8.75	2.00
01100000 00000100 DDDDDDDD AAAAAAAA AAAAAAAA	MIA	M(A)←D	12.50	2.75
01100000 00000000 DDDDDDDD CCCCCCCC	MIB	M((Q)+C)← D	12.25	2.75
01100000 00000000 DDDDDDDD 11111111	MIX	M((Q)+(RO))←D	12.75	2.75
01100000 00000100	MIN	M((Q)) ←D, Increment Q	11.75	2.50
01100000 01001RRR AAAAAAAA AAAAAAAA	MAR	R ← M(A)	10.75	2.625
01100000 01000100 AAAAAAAA AAAAAAAA EEEEEEEE EEEEEEEE	MAA	M(E)←M(A)	14.50	3.375
01100000 01000000 AAAAAAAA AAAAAAAA CCCCCCCC	MAB	M((Q)+C)←M(A)	14.25	3.375
01100000 01000000 AAAAAAAA AAAAAAAA 11111111	MAX	M((Q)+(RO))←M(A)	14.75	3.375
01100000 010001QQ AAAAAAAA AAAAAAAA	MAN	M((Q))←M(A), Increment Q	13.75	3.125
01100000 00TT1RRR CCCCCCCC	MBR	R←M((T)+C)	10.50	2.625

Cont'd on next page

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS5 Cont'd

IS5 Cont'd

OP CODE	MNEMONIC	DESCRIPTION	TIME(us) IS5	TIME(us) IS5a
		Move Instructions (cont)		
01100000 00TT0100 CCCCCCCC AAAAAAAA AAAAAAAA	MBA	M(A)← M((T)+C)	14.25 us	3.375 us
01100000 00TT00QQ CCCCCCCC FFFFFFFF	MBB	M((Q)+F) ← M((T)+C)	14.00	3.375
01100000 00TT00QQ CCCCCCCC 11111111	MBX	M((Q)+(R0))← M((T)+C)	14.50	3.375
01100000 00TT0100 CCCCCCCC	MBN	M((Q))←M((T) + C)	13.50	3.125
01100000 00TT1RRR CCCCCCCC	MXR	R← M((T)+(R0))	11.00	2.625
01100000 00TT0100 CCCCCCCC AAAAAAAA AAAAAAAA	MXA	M(A)← M((T)+(R0))	14.75	3.375
01100000 00TT00QQ CCCCCCCC FFFFFFFF	MXB	M((Q)+F)← M((T)+(R0))	14.50	3.375
01100000 00TT00QQ 11111111 FFFFFFFF	MXX	M((Q)+(R0))← M((T)+(R0))	15.00	3.375
01100000 00TT01QQ CCCCCCCC	MXN	M((Q))← M((T)+(R0)), Increment Q	14.00	3.125
01100000 01TT1RRR	MNR	R←M((T)), Increment T	10.00	2.375
01100000 01TT0100 AAAAAAAA AAAAAAAA	MNA	M(A)←M((T)), Increment T	13.75	3.125
01100000 CCCCCCCC	MNB	M((Q)+C)←M((T)),Increment T	13.50	3.125
01100000 01TT00QQ 11111111	MNX	M((Q)+(R0))←M((T)), Increment T	14.00	3.125
01100000 01TT01QQ	MNN	M((Q))←M((T)), Increment QT	13.00	2.875

OP CODE	MNEMONIC	DESCRIPTION	TIME(us) IS5	TIME(us) IS5a
		Jump Instructions		
01010001 AAAAAAAA AAAAAAAA	JC1	If CY is set, jump to A	4.25-5.75 us	1.0 - 1.25 us
01010000 AAAAAAAA AAAAAAAA	JC0	If CY is cleared, jump to A	4.25-6.25	1.0 - 1.25
01010010 AAAAAAAA AAAAAAAA	JAZ	If ACC = 0, jump to A	4.25-6.25	1.0 - 1.25
01010011 AAAAAAAA AAAAAAAA	JAN	If ACC ≠ 0, jump to A	4.25-5.75	1.0 - 1.25
01010100 AAAAAAAA AAAAAAAA	JAP	If ACC ≥ 0, jump to A	4.25-6.25	1.0 - 1.25
01010101 AAAAAAAA AAAAAAAA	JAM	If ACC < 0, jump to A	4.25-5.75	1.0 - 1.25
01010110 AAAAAAAA AAAAAAAA	JMP	Jump to A	5.50	1.125
01010111 AAAAAAAA AAAAAAAA	JSR	M((Q3)) PC (8:15), M((Q3)+1) ←PC (0:7), Q3←(Q3)+2, jump to A	10.75	1.875
00001110	RFS	Q3←(Q3)-2, PC(8:15)←M((Q3)), PC(0:7)←M((Q3)+1) (Return from subroutine)	6.75	1.50

OP CODE	MNEMONIC	DESCRIPTION	TIME (us) IS5	TIME (us) IS5a
		Skip Instructions		
01011001 BBBBBBBB	SC1	If CY is set, add B to PC	4.00-5.50 us	.875-1.125 us
01011000 BBBBBBBB	SC0	If CY is cleared, add B to PC	4.00-6.00	.875-1.125
01011010 BBBBBBBB	SAZ	If ACC = 0, add B to PC	4.00-6.00	.875-1.125
01011011 BBBBBBBB	SAN	If ACC ≠ 0, add B to PC	4.00-5.50	.875-1.125
01011100 BBBBBBBB	SAP	If ACC ≥ 0, add B to PC	4.00-6.00	.875-1.125
01011101 BBBBBBBB	SAM	If ACC < 0, add B to PC	4.00-5.50	.875-1.125
01011110 BBBBBBBB	SKP	Add B to PC	5.25	.875
01011111 BBBBBBBB	SSR	M((Q3))←PC(8:15), M((Q3)+1) ←PC(0:7), Q3←(Q3)+2, Add B to PC	10.50	1.75
00001011	APC	Add ACC to PC	3.25	1.00

OP CODE	MNEMONIC	DESCRIPTION	TIME(us) IS5	TIME(us) IS5a
		Accumulator and Carry Instructions		
00000001	INA	Increment ACC	3.75 us	.75 us
00000010	CLA	Clear ACC	3.50	.75
00000011	CMA	Complement ACC	3.25	.75
00000100	RAL	Rotate ACC left one bit	4.00	.75
00000101	RAR	Rotate ACC right one bit	13.25	.75
00000110	SHL	Shift ACC left one bit	3.75	.75
00000111	SHR	Shift ACC right one bit	14.00	.75
00001000	CLC	Clear CY	3.50	.75
00001010	STC	Set CY	3.50	.75
00001001	CMC	Complement CY	4.00	.75
		I/O Instructions		
00100000 CCCCCCCC	INP	Input Byte from Device C to ACC	5.25 us	1.0 us
00101000 CCCCCCCC	OUT	Output Byte from ACC to Device C	5.25	1.0
00100100	IPI	Input Byte from Device (R7) to ACC	3.75	.875
00101100	OTI	Output Byte from ACC to Device (R7)	3.75	.875
		Control Instructions		
00000000	NOP	No Operation	2.75 us	.75 us
00001111	RFI	Return from Interrupt	80.25-82.00	5.0
00001101	WTI	Wait for Interrupt	2.25+	1.0+
00110LLL	INT	Interrupt Level L	80.75-87.75	5.0
00001100	XIM	Exchange IM with ACC	5.50	1.25
00000000	CVX	Convert to Hexadecimal	2.75	.75
00010LLL	XLP	Exchange level PC*	10.75	2.0
		Base Register Instructions		
00101QQ AAAAAAAA AAAAAAAA	LDQ	Load A into Q	6.50 us	1.375 us
00101QQ	ADQ	Add ACC +256 X R7 to Q	5.75	1.25
00100QQ	INQ	Increment Q	4.50	1.0
00100QQ	DEQ	Decrement Q	4.50	1.0

* ACTS AS JSR 3 ON IS5

ACCUMULATOR AND MEMORY INSTRUCTIONS

OPERATIONS	MNEMONIC	IMMED OP	IMMED ~	IMMED =	DIRECT OP	DIRECT ~	DIRECT =	INDEX OP	INDEX ~	INDEX =	EXTND OP	EXTND ~	EXTND =	IMPLIED OP	IMPLIED ~	IMPLIED =	BOOLEAN/ARITHMETIC OPERATION (All register labels refer to contents)	5 H	4 I	3 N	2 Z	1 V	0 C
Add	ADDA	8B	2	2	9B	3	2	AB	5	2	BB	4	3				A + M → A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	5	2	FB	4	3				B + M → B	↕	•	↕	↕	↕	↕
Add Acmltrs	ABA													1B	2	1	A + B → A	↕	•	↕	↕	↕	↕
Add with Carry	ADCA	89	2	2	99	3	2	A9	5	2	B9	4	3				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	5	2	F9	4	3				B + M + C → B	↕	•	↕	↕	↕	↕
And	ANDA	84	2	2	94	3	2	A4	5	2	B4	4	3				A · M → A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	5	2	F4	4	3				B · M → B	•	•	↕	↕	R	•
Bit Test	BITA	85	2	2	95	3	2	A5	5	2	B5	4	3				A · M	•	•	↕	↕	R	•
	BITB	C5	2	2	D5	3	2	E5	5	2	F5	4	3				B · M	•	•	↕	↕	R	•
Clear	CLR							6F	7	2	7F	6	3				00 → M	•	•	R	S	R	R
	CLRA													4F	2	1	00 → A	•	•	R	S	R	R
	CLRB													5F	2	1	00 → B	•	•	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	5	2	B1	4	3				A − M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	5	2	F1	4	3				B − M	•	•	↕	↕	↕	↕
Compare Acmltrs	CBA													11	2	1	A − B	•	•	↕	↕	↕	↕
Complement, 1's	COM							63	7	2	73	6	3				M̄ → M	•	•	↕	↕	R	S
	COMA													43	2	1	Ā → A	•	•	↕	↕	R	S
	COMB													53	2	1	B̄ → B	•	•	↕	↕	R	S
Complement, 2's (Negate)	NEG							60	7	2	70	6	3				00 − M → M	•	•	↕	↕	①	②
	NEGA													40	2	1	00 − A → A	•	•	↕	↕	①	②
	NEGB													50	2	1	00 − B → B	•	•	↕	↕	①	②
Decimal Adjust, A	DAA													19	2	1	Converts Binary Add. of BCD Characters into BCD Format	•	•	↕	↕	↕	③
Decrement	DEC							6A	7	2	7A	6	3				M − 1 → M	•	•	↕	↕	4	•
	DECA													4A	2	1	A − 1 → A	•	•	↕	↕	4	•
	DECB													5A	2	1	B − 1 → B	•	•	↕	↕	4	•
Exclusive OR	EORA	88	2	2	98	3	2	A8	5	2	B8	4	3				A⊕M → A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	5	2	F8	4	3				B⊕M → B	•	•	↕	↕	R	•
Increment	INC							6C	7	2	7C	6	3				M + 1 → M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1 → A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1 → B	•	•	↕	↕	⑤	•
Load Acmltr	LDAA	86	2	2	96	3	2	A6	5	2	B6	4	3				M → A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	5	2	F6	4	3				M → B	•	•	↕	↕	R	•
Or, Inclusive	ORAA	8A	2	2	9A	3	2	AA	5	2	BA	4	3				A + M → A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	5	2	FA	4	3				B + M → B	•	•	↕	↕	R	•
Push Data	PSHA													36	4	1	A → M_{SP}, SP − 1 → SP	•	•	•	•	•	•
	PSHB													37	4	1	B → M_{SP}, SP − 1 → SP	•	•	•	•	•	•
Pull Data	PULA													32	4	1	SP + 1 → SP, M_{SP} → A	•	•	•	•	•	•
	PULB													33	4	1	SP + 1 → SP, M_{SP} → B	•	•	•	•	•	•
Rotate Left	ROL							69	7	2	79	6	3				M	•	•	↕	↕	⑥	↕
	ROLA													49	2	1	A	•	•	↕	↕	⑥	↕
	ROLB													59	2	1	B	•	•	↕	↕	⑥	↕
Rotate Right	ROR							66	7	2	76	6	3				M	•	•	↕	↕	⑥	↕
	RORA													46	2	1	A	•	•	↕	↕	⑥	↕
	RORB													56	2	1	B	•	•	↕	↕	⑥	↕
Shift Left, Arithmetic	ASL							68	7	2	78	6	3				M	•	•	↕	↕	⑥	↕
	ASLA													48	2	1	A	•	•	↕	↕	⑥	↕
	ASLB													58	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Arithmetic	ASR							67	7	2	77	6	3				M	•	•	↕	↕	⑥	↕
	ASRA													47	2	1	A	•	•	↕	↕	⑥	↕
	ASRB													57	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Logic	LSR							64	7	2	74	6	3				M	•	•	R	↕	⑥	↕
	LSRA													44	2	1	A	•	•	R	↕	⑥	↕
	LSRB													54	2	1	B	•	•	R	↕	⑥	↕
Store Acmltr.	STAA				97	4	2	A7	6	2	B7	5	3				A → M	•	•	↕	↕	R	•
	STAB				D7	4	2	E7	6	2	F7	5	3				B → M	•	•	↕	↕	R	•
Subtract	SUBA	80	2	2	90	3	2	A0	5	2	B0	4	3				A − M → A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	5	2	F0	4	3				B − M → B	•	•	↕	↕	↕	↕
Subtract Acmltrs.	SBA													10	2	1	A − B → A	•	•	↕	↕	↕	↕
Subtr. with Carry	SBCA	82	2	2	92	3	2	A2	5	2	B2	4	3				A − M − C → A	•	•	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	E2	5	2	F2	4	3				B − M − C → B	•	•	↕	↕	↕	↕
Transfer Acmltrs	TAB													16	2	1	A → B	•	•	↕	↕	R	•
	TBA													17	2	1	B → A	•	•	↕	↕	R	•
Test, Zero or Minus	TST							6D	7	2	7D	6	3				M − 00	•	•	↕	↕	R	R
	TSTA													4D	2	1	A − 00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B − 00	•	•	↕	↕	R	R
																		H	I	N	Z	V	C

LEGEND:

OP Operation Code (Hexadecimal);
~ Number of MPU Cycles;
= Number of Program Bytes;
+ Arithmetic Plus;
− Arithmetic Minus;
· Boolean AND;
M_{SP} Contents of memory location pointed to be Stack Pointer;
+ Boolean Inclusive OR;
⊕ Boolean Exclusive OR;
M̄ Complement of M;
→ Transfer Into;
0 Bit = Zero;
00 Byte = Zero;

Note – Accumulator addressing mode instructions are included in the column for IMPLIED addressing

CONDITION CODE SYMBOLS:

H Half-carry from bit 3;
I Interrupt mask
N Negative (sign bit)
Z Zero (byte)
V Overflow, 2's complement
C Carry from bit 7
R Reset Always
S Set Always
↕ Test and set if true, cleared otherwise
• Not Affected

Cont'd on next page

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS6 Cont'd

IS6 Cont'd

INDEX REGISTER AND STACK MANIPULATION INSTRUCTIONS

POINTER OPERATIONS	MNEMONIC	IMMED OP	IMMED ~	IMMED #	DIRECT OP	DIRECT ~	DIRECT #	INDEX OP	INDEX ~	INDEX #	EXTND OP	EXTND ~	EXTND #	IMPLIED OP	IMPLIED ~	IMPLIED #	BOOLEAN/ARITHMETIC OPERATION	5 H	4 I	3 N	2 Z	1 V	0 C
Compare Index Reg	CPX	8C	3	3	9C	4	2	AC	6	2	BC	5	3				$X_H - M, X_L - (M+1)$	•	•	⑦	↕	⑦	•
Decrement Index Reg	DEX													09	4	1	$X - 1 \rightarrow X$	•	•	•	↕	•	•
Decrement Stack Pntr	DES													34	4	1	$SP - 1 \rightarrow SP$	•	•	•	•	•	•
Increment Index Reg	INX													08	4	1	$X + 1 \rightarrow X$	•	•	•	↕	•	•
Increment Stack Pntr	INS													31	4	1	$SP + 1 \rightarrow SP$	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	6	2	FE	5	3				$M \rightarrow X_H, (M+1) \rightarrow X_L$	•	•	⑨	↕	R	•
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	6	2	BE	5	3				$M \rightarrow SP_H, (M+1) \rightarrow SP_L$	•	•	⑨	↕	R	•
Store Index Reg	STX				DF	5	2	EF	7	2	FF	6	3				$X_H \rightarrow M, X_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Store Stack Pntr	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H \rightarrow M, SP_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Indx Reg → Stack Pntr	TXS													35	4	1	$X - 1 \rightarrow SP$	•	•	•	•	•	•
Stack Pntr → Indx Reg	TSX													30	4	1	$SP + 1 \rightarrow X$	•	•	•	•	•	•

JUMP AND BRANCH INSTRUCTIONS

OPERATIONS	MNEMONIC	RELATIVE OP	RELATIVE ~	RELATIVE #	INDEX OP	INDEX ~	INDEX #	EXTND OP	EXTND ~	EXTND #	IMPLIED OP	IMPLIED ~	IMPLIED #	BRANCH TEST	5 H	4 I	3 N	2 Z	1 V	0 C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = Zero	BEQ	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										$N \oplus V = 0$	•	•	•	•	•	•
Branch If > Zero	BGT	2E	4	2										$Z + (N \oplus V) = 0$	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										C + Z = 0	•	•	•	•	•	•
Branch If ≤ Zero	BLE	2F	4	2										$Z + (N \oplus V) = 1$	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										C + Z = 1	•	•	•	•	•	•
Branch If < Zero	BLT	2D	4	2										$N \oplus V = 1$	•	•	•	•	•	•
Branch If Minus	BMI	2B	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	26	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	BD	9	3					•	•	•	•	•	•
No Operation	NOP										02	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		⑩					
Return From Subroutine	RTS										39	5	1		•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1	See Special Operations	•	•	•	•	•	•
Wait for Interrupt	WAI										3E	9	1		•	⑪	•	•	•	•

CONDITION CODE REGISTER MANIPULATION INSTRUCTIONS

OPERATIONS	MNEMONIC	IMPLIED OP	IMPLIED ~	IMPLIED #	BOOLEAN OPERATION	5 H	4 I	3 N	2 Z	1 V	0 C
Clear Carry	CLC	0C	2	1	0 → C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0 → I	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0 → V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1 → C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1 → I	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1 → V	•	•	•	•	S	•
Acmltr A → CCR	TAP	06	2	1	A → CCR	⑫					
CCR → Acmltr A	TPA	07	2	1	CCR → A	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES:

(Bit set if test is true and cleared otherwise)

1 (Bit V) Test: Result = 10000000?
2 (Bit C) Test: Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N⊕C after shift has occurred
7 (Bit N) Test: Sign bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt is required to exit the wait state
12 (All) Set according to the contents of Accumulator A

INSTRUCTION ADDRESSING MODES AND ASSOCIATED EXECUTION TIMES

(Times in Machine Cycles)

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied	Relative
ABA		•	•	•	•	•	2	•
ADC	x	•	2	3	4	5	•	•
ADD	x	•	2	3	4	5	•	•
AND	x	•	2	3	4	5	•	•
ASL		2	•	•	6	7	•	•
ASR		2	•	•	6	7	•	•
BCC		•	•	•	•	•	•	4
BCS		•	•	•	•	•	•	4
BEA		•	•	•	•	•	•	4
BGE		•	•	•	•	•	•	4
BGT		•	•	•	•	•	•	4
BHI		•	•	•	•	•	•	4
BIT	x	•	2	3	4	5	•	•
BLE		•	•	•	•	•	•	4
BLS		•	•	•	•	•	•	4
BLT		•	•	•	•	•	•	4
BMI		•	•	•	•	•	•	4
BNE		•	•	•	•	•	•	4
BPL		•	•	•	•	•	•	4
BRA		•	•	•	•	•	•	4
BSR		•	•	•	•	•	•	8
BVC		•	•	•	•	•	•	4
BVS		•	•	•	•	•	•	4
CBA		•	•	•	•	•	2	•
CLC		•	•	•	•	•	2	•
CLI		•	•	•	•	•	2	•
CLR		2	•	•	6	7	•	•
CLV		•	•	•	•	•	2	•
CMP	x	•	2	3	4	5	•	•
COM		2	•	•	6	7	•	•
CPX		•	3	4	5	6	•	•
DAA		•	•	•	•	•	2	•
DEC		2	•	•	6	7	•	•
DES		•	•	•	•	•	4	•
DEX		•	•	•	•	•	4	•
EOR	x	•	2	3	4	5	•	•

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied
INC		2	•	•	6	7	•
INS		•	•	•	•	•	4
INX		•	•	•	•	•	4
JMP		•	•	•	3	4	•
JSR		•	•	•	9	8	•
LDA	x	•	2	3	4	5	•
LDS		•	3	4	5	6	•
LDX		•	3	4	5	6	•
LSR		2	•	•	6	7	•
NEG		2	•	•	6	7	•
NOP		•	•	•	•	•	2
ORA	x	•	2	3	4	5	•
PSH		•	•	•	•	•	4
PUL		•	•	•	•	•	4
ROL		2	•	•	6	7	•
ROR		2	•	•	6	7	•
RTI		•	•	•	•	•	10
RTS		•	•	•	•	•	5
SBA		•	•	•	•	•	2
SBC	x	•	2	3	4	5	•
SEC		•	•	•	•	•	2
SEI		•	•	•	•	•	2
SEV		•	•	•	•	•	2
STA	x	•	•	4	5	6	•
STS		•	•	5	6	7	•
STX		•	•	5	6	7	•
SUB	x	•	2	3	4	5	•
SWI		•	•	•	•	•	12
TAB		•	•	•	•	•	2
TAP		•	•	•	•	•	2
TBA		•	•	•	•	•	2
TPA		•	•	•	•	•	2
TST		2	•	•	6	7	•
TSX		•	•	•	•	•	4
TSX		•	•	•	•	•	4
WAI		•	•	•	•	•	9

NOTE: Interrupt time is 12 cycles from the end of the instruction being executed, except following a WAI instruction. Then it is 4 cycles.

Cont'd on next page

IS6a

MC6801 — MC6803 NEW INSTRUCTIONS

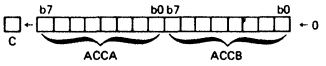
ABX Adds the 8-bit unsigned accumulator B to the 16-bit X-Register taking into account the possible carry out of the low order byte of the X-Register.

IX ← IX + ACCB

ADDD Adds the double precision ACCAB to the double precision value M:M+1 and places the results in ACCAB.

ACCAB ← (ACCAB) + (M:M+1)

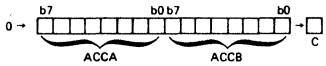
ASLD Shifts all bits of ACCAB one place to the left. Bit 0 is loaded with a zero. The C bit is loaded from the most significant bit of ACCAB.



LDD Loads the contents of double precision memory location into the double accumulator A:B. The condition codes are set according to the data.

ACCAB ← (M:M+1)

LSRD Shifts all bits of ACCAB one place to the right. Bit 15 is loaded with zero. The C bit is loaded from the least significant bit of ACCAB.



MUL Multiplies the 8 bits in accumulator A with the 8 bits in accumulator B to obtain a 16-bit unsigned number in A:B.ACCA contains MSB of result.

ACCAB ← ACCA * ACCB

PSHX The contents of the index register is pushed onto the stack at the address contained in the stack pointer. The stack pointer is decremented by 2.

↓ (IXL), SP ← (SP) – 0001
↓ (IXH), SP ← (SP) – 0001

PULX The index register is pulled from the stack beginning at the current address contained in the current address contained in the stack pointer +1. The stack pointer is incremented by 2 in total.

SP ← (SP) + 1; ↑ IXH
SP ← (SP) + 1; ↑ IXL

STD Stores the contents of double accumulator A:B in memory. The contents of ACCAB remain unchanged.

M:M+1 ← (ACCAB)

SUBD Subtracts the contents of M:M+1 from the contents of double accumulator AB and places the result in ACCAB.

ACCAB ← (ACCAB) – (M:M+1)

MC6803 PROGRAMMING MODE

The execution time of key instructions has been reduced.
Table 2 shows instruction execution times in machine cycles.

	ACCX	Immediate	Direct	Extended	Indexed	Inherent	Relative
ABA	•	•	•	•	•	2	•
ABX	•	•	•	•	•	3	•
ADC	•	2	3	4	4	•	•
ADD	•	2	3	4	4	•	•
ADDD	•	4	5	6	6	•	•
AND	•	2	3	4	4	•	•
ASL	2	•	•	6	6	•	•
ASLD	•	•	•	•	•	3	•
ASR	2	•	•	6	6	•	•
BCC	•	•	•	•	•	3	•
BCS	•	•	•	•	•	3	•
BEQ	•	•	•	•	•	3	•
BGE	•	•	•	•	•	3	•
BGT	•	•	•	•	•	3	•
BHI	•	•	•	•	•	3	•
BIT	•	2	3	4	4	•	•
BLE	•	•	•	•	•	3	•
BLS	•	•	•	•	•	3	•
BLT	•	•	•	•	•	3	•
BMI	•	•	•	•	•	3	•
BNE	•	•	•	•	•	3	•
BPL	•	•	•	•	•	3	•
BRA	•	•	•	•	•	3	•
BSR	•	•	•	•	•	6	•
BVC	•	•	•	•	•	3	•
BVS	•	•	•	•	•	3	•
CBA	•	•	•	•	•	2	•
CLC	•	•	•	•	•	2	•
CLI	•	•	•	•	•	2	•
CLR	2	•	•	6	6	•	•
CLV	•	•	•	•	•	2	•
CMP	•	2	3	4	4	•	•
COM	2	•	•	6	6	•	•
CPX	•	4	5	6	6	•	•
DAA	•	•	•	•	•	2	•
DEC	2	•	•	6	6	•	•
DES	•	•	•	•	•	3	•
DEX	•	•	•	•	•	3	•
EOR	•	2	3	4	4	•	•
INC	2	•	•	6	6	•	•
INS	•	•	•	•	•	3	•

	ACCX	Immediate	Direct	Extended	Indexed	Inherent	Relative
INX	•	•	•	•	•	3	•
JMP	•	•	•	3	3	•	•
JSR	•	•	5	6	6	•	•
LDA	•	2	3	4	4	•	•
LDD	•	3	4	5	5	•	•
LDS	•	3	4	5	5	•	•
LDX	•	3	4	5	5	•	•
LSR	2	•	•	6	6	•	•
LSRD	•	•	•	•	•	3	•
MUL	•	•	•	•	•	10	•
NEG	2	•	•	6	6	•	•
NOP	•	•	•	•	•	2	•
ORA	•	2	3	4	4	•	•
PSH	3	•	•	•	•	•	•
PSHX	•	•	•	•	4	•	•
PUL	4	•	•	•	•	•	•
PULX	•	•	•	•	•	5	•
ROL	2	•	6	6	•	•	•
ROR	2	•	6	6	•	•	•
RTI	•	•	•	•	•	10	•
RTS	•	•	•	•	•	5	•
SBA	•	•	•	•	•	2	•
SBC	•	2	3	4	4	•	•
SEC	•	•	•	•	•	2	•
SEI	•	•	•	•	•	2	•
SEV	•	•	•	•	•	2	•
STA	•	•	3	4	4	•	•
STD	•	•	4	5	5	•	•
STS	•	•	4	5	5	•	•
STX	•	•	4	5	5	•	•
SUB	•	2	3	4	4	•	•
SUBD	•	4	5	6	6	•	•
SWI	•	•	•	•	•	12	•
TAB	•	•	•	•	•	2	•
TAP	•	•	•	•	•	2	•
TBA	•	•	•	•	•	2	•
TPA	•	•	•	•	•	2	•
TST	2	•	•	6	6	•	•
TSX	•	•	•	•	•	3	•
TXS	•	•	•	•	•	3	•
WAI	•	•	•	•	•	9	•

standard instruction set with a description, mnemonic, and status effect. The mnemonics were defined for easy reference to the functional description. Eighteen mnemonics use an identifier to indicate the condition that satisfies the status requirement for a successful branch or call if the instruction is followed immediately by a branch or call command. "C" means that if the instruction generates a carry (status = one), then a following branch or call is executed. If a branch instruction does not follow or if there is no carry (status = zero), then the program counter proceeds to the next address without changing the normal counting sequence. "N" means that if no borrow (equal to a carry in two's complement arithmetic) is generated, an ensuing branch or call is taken. "Z" indicates that if the two's complement of zero in the accumulator (instruction CPAIZ) is attempted with a branch or call following, then the branch or call is taken. "1", "LE", "NE", and "NEZ" are used to indicate conditions for branch and call for seven test instructions. The test instructions do not modify data at all; tests are used solely in conjunction with subsequent branches or calls.

If an instruction that does not affect status is placed between an instruction that does affect status and a branch or call instruction, then the branch or call is always successful. This is true because status always returns to its normal state (status = one) after one instruction cycle, and branches and calls are taken if status equals one.

FUNCTION	MNEMONIC	STATUS EFFECTS		DESCRIPTION
		C	N	
Register to Register	TAY			Transfer accumulator to Y register.
	TYA			Transfer Y register to accumulator.
	CLA			Clear accumulator.
Transfer Register to Memory	TAM			Transfer accumulator to memory.
	TAMIY			Transfer accumulator to memory and increment Y register.
	TAMZA			Transfer accumulator to memory and zero accumulator.
Memory to Register	TMY			Transfer memory to Y register.
	TMA			Transfer memory to accumulator.
	XMA			Exchange memory and accumulator.
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Increment memory and load into accumulator. If carry, one to status.
	DMAN	Y		Decrement memory and load into accumulator. If no borrow, one to status.
	IA			Increment accumulator, no status effect.
	IYC	Y		Increment Y register. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	A8AAC	Y		Add 8 to accumulator, results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator, results to accumulator. If carry, one to status.
	A6AAC	Y		Add 6 to accumulator, results to accumulator. If carry, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.
Arithmetic Compare	ALEM	Y		If accumulator less than or equal to memory, one to status.
	ALEC	Y		If accumulator less than or equal to a constant, one to status.
Logical Compare	MNEZ		Y	If memory not equal to zero, one to status.
	YNEA		Y	If Y register not equal to accumulator, one to status and status latch.
	YNEC		Y	If Y register not equal to a constant, one to status.

FUNCTION	MNEMONIC	STATUS EFFECTS		DESCRIPTION
		C	N	
Bits in Memory	SBIT			Set memory bit.
	RBIT			Reset memory bit.
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register.
	TCMIY			Transfer constant to memory and increment Y.
Input	KNEZ		Y	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator.
Output	SETR			Set R output addressed by Y.
	RSTR			Reset R output addressed by Y.
	TDO			Transfer data from accumulator and status latch to O outputs.
	CLO			Clear O-output register.
RAM 'X' Addressing	LDX			Load 'X' with a constant.
	COMX			Complement 'X'.
ROM Addressing	BR			Branch on status = one.
	CALL			Call subroutine on status = one.
	RETN			Return from subroutine.
	LDP			Load page buffer with constant.

NOTES: C-Y (Yes) means that if there is a carry out of the MSB, status output goes to the one state. If no carry is generated, status output goes to the zero state.

N-Y (Yes) means that if the bits compared are not equal, status output goes to the one state. If the bits are equal, status output goes to the zero state.

A zero in status remains through the next instruction cycle only. If the next instruction is a branch or call and status is a zero, then the branch or call is not executed successfully.

standard instruction set with a description, mnemonic, and status effect. The mnemonics were defined for easy reference to the functional description. Eighteen mnemonics use an identifier to indicate the condition that satisfies the status requirement for a successful branch or call if the instruction is followed immediately by a branch or call command. "C" means that if the instruction generates a carry (status = one), then a following branch or call is executed. If a branch instruction does not follow or if there is no carry (status = zero), then the program counter proceeds to the next address without changing the normal counting sequence. "N" means that if no borrow (equal to a carry in two's complement arithmetic) is generated, an ensuing branch or call is taken. "Z" indicates that if the two's complement of zero in the accumulator (instruction CPAIZ) is attempted with a branch or call following, then the branch or call is taken. "1", "LE", "NE", and "NEZ" are used to indicate conditions for branch and call for seven test instructions. The test instructions do not modify data at all; tests are used solely in conjunction with subsequent branches or calls.

If an instruction that does not affect status is placed between an instruction that does affect status and a branch or call instruction, then the branch or call is always successful. This is true because status always returns to its normal state (status = one) after one instruction cycle, and branches and calls are taken if status equals one.

FUNCTION	MNEMONIC	STATUS EFFECT		DESCRIPTION
		C	N	
Register-to-Register Transfer	TAY			Transfer accumulator to Y register
	TYA			Transfer Y register to accumulator
	CLA			Clear accumulator
Register to Memory	TAM			Transfer accumulator to memory
	TAMIYC	Y		Transfer accumulator to memory and increment Y register. If carry, one to status.
	TAMDYN	Y		Transfer accumulator to memory and decrement Y register. If no borrow, one to status.
	TAMZA			Transfer accumulator to memory and zero accumulator
Memory to Register	TMY			Transfer memory to Y register
	TMA			Transfer memory to accumulator
	XMA			Exchange memory and accumulator
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Increment memory and load into accumulator. If carry, one to status.
	DMAN	Y		Decrement memory and load into accumulator. If no borrow, one to status.
	IAC	Y		Increment accumulator. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	A2AAC	Y		Add 2 to accumulator. Results to accumulator. If carry, one to status.
	A3AAC	Y		Add 3 to accumulator. Results to accumulator. If carry, one to status.
	A4AAC	Y		Add 4 to accumulator. Results to accumulator. If carry, one to status.
	A5AAC	Y		Add 5 to accumulator. Results to accumulator. If carry, one to status.
	A6AAC	Y		Add 6 to accumulator. Results to accumulator. If carry, one to status.
	A7AAC	Y		Add 7 to accumulator. Results to accumulator. If carry, one to status.
	A8AAC	Y		Add 8 to accumulator. Results to accumulator. If carry, one to status.
	A9AAC	Y		Add 9 to accumulator. Results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator. Results to accumulator. If carry, one to status.
	A11AAC	Y		Add 11 to accumulator. Results to accumulator. If carry, one to status.
	A12AAC	Y		Add 12 to accumulator. Results to accumulator. If carry, one to status.
	A13AAC	Y		Add 13 to accumulator. Results to accumulator. If carry, one to status.
	A14AAC	Y		Add 14 to accumulator. Results to accumulator. If carry, one to status.
	IYC	Y		Increment Y register. If carry, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.

FUNCTION	MNEMONIC	STATUS EFFECT		DESCRIPTION
		C	N	
Arithmetic Compare	ALEM	Y		If accumulator less than or equal to memory, one to status.
Logical Compare	MNEA		Y	If memory is not equal to accumulator, one to status.
	MNEZ		Y	If memory not equal to zero, one to status.
	YNEA		Y	If Y register not equal to accumulator, one to status and status latch.
	YNEC		Y	If Y register not equal to a constant, one to status.
Bits in Memory	SBIT			Set memory bit
	RBIT			Reset memory bit
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register
	TCMIY			Transfer constant to memory and increment Y
Input	KNEZ		Y	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator
Output	SETR			Set R output addressed by Y
	RSTR			Reset R output addressed by Y
	TDO			Transfer data from accumulator and status latch to O-outputs
RAM X Addressing	LDX			Load X with file address
	COMX			Complement the MSB of X
ROM Addressing	BR			Branch on status = one
	CALL			Call subroutine on status = one
	RETN			Return from subroutine
	LDP			Load page buffer with constant
	COMC			Complement chapter

NOTES: C,Y (Yes) means that if there is a carry out of the MSB, status output goes to the one state. If no carry is generated, status output goes to the zero state.

N,Y (Yes) means that if the bits compared are not equal, status output goes to the one state. If the bits are equal status output goes to the zero state.

A zero in status remains through the next instruction cycle only. If the next instruction is a branch or call and status is a zero, then the branch or call is not executed successfully.

SYMBOL	DESCRIPTION
$<b_2>$	Second byte of instruction
$<b_3>$	Third byte of instruction

r_a

Register #	Register Name
000	B
001	C
010	D
011	E
100	H
101	L
111	A

r_b

Register #	Register Name
00	BC
01	DE
10	HL
11	SP

r_c

Register #	Register Name
0	BC
1	DE

r_d

Register #	Register Name
00	BC
01	DE
10	HL

r_{dL}	Least significant 8 bits of r_d
r_{dH}	Most significant 8 bits of r_d
f	Flags — True condition
	Zero (Z) — Result is zero
	Carry (C) — Carry/borrow out of MSB is one
	Parity (P) — Parity of result is even
	Sign (S) — MSB of result is one
	Carry 1 (C1) — Carry out of fourth bit is one
M	Memory address defined by registers H and L
( )	Contents of specified address or register
[ ]	Contents at address contained in specified register
←	Is transferred to
↔	Exchange
Am	Bit m of A register (accumulator)
{ }	Flags affected
b_2	Single byte immediate operand
b_3b_2	Double byte immediate operand
$(nnn)_8$	(nnn) is an octal (base 8) number

ACCUMULATOR GROUP INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
ACI	b_2	2	2/7	(A) ← (A) + $<b_2>$+(carry), add the second byte of the instruction and the contents of the carry flag to register A and place in A. {C,Z,S,P,C1}
ADC	M	1	2/7	(A) ← (A) + (M) + (carry). {C,Z,S,P,C1}
ADC	r_a	1	1/4	(A) ← (A) + (r_a) + (carry). {C,Z,S,P,C1}
ADD	M	1	2/7	(A) ← (A) + (M), add the contents of M to register A and place in A. {C,Z,S,P,C1}
ADD	r_a	1	1/4	(A) ← (A) + (r_a). {C,Z,S,P,C1}
ADI	b_2	2	2/7	(A) ← (A) + $<b_2>$. {C,Z,S,P,C1}
ANA	M	1	2/7	(A) ← (A) AND (M), take the logical AND of M and register A and place in A. The carry flag will be reset low. {C,Z,S,P,C1}
ANA	r_a	1	1/4	(A) ← (A) AND (r_a). {C,Z,S,P,C1}
ANI	b_2	2	2/7	(A) ← (A) AND $<b_2>$. {C,Z,S,P,C1}
CMA		1	1/4	(A) ← ($\bar{A}$), complement A.
CMC		1	1/4	(carry) ← ($\overline{carry}$), complement the carry flag. {C}
CMP	M	1	2/7	(A) − (M), compare the contents of M to register A and set the flags accordingly. {C,Z,S,P,C1} (A) = (M) Z = 1 (A) ≠ (M) Z = 0 (A) < (M) C = 1 (A) > (M) C = 0
CMP	r_a	1	1/4	(A) − (r_a). {C,Z,S,P,C1}
CPI	b_2	2	2/7	(A)−$<b_2>$. {C,Z,S,P,C1}
DAA		1	1/4	(A)←BCD correction of (A). The 8 bit A contents is corrected to form two 4 bit BCD digits after a binary arithmetic operation. A fifth flag C1 indicates the overflow from A_3. The carry flag C indicates the overflow from A_7 (See Table 3). {C,Z,S,P,C1}
DAD	r_b	1	1/10	(HL) ← (HL) + (r_b), add the contents of double register r_b to double register HL and place in HL. {C}
LDA	b_3b_2	3	4/13	(A)←[$<b_3>$ $<b_2>$]
LDAX	r_c	1	2/7	(A)←[(r_c)]
ORA	M	1	2/7	(A) ← (A) OR (M), take the logical OR of the contents of M and register A and place in A. The carry flag will be reset. {C,Z,S,P,C1}
ORA	r_a	1	1/4	(A) ← (A) OR (r_a). {C,Z,S,P,C1}
ORI	b_2	2	2/7	(A) ← (A) OR $<b_2>$. {C,Z,S,P,C1}
RAL		1	1/4	A_{m+1}←A_m, A_0←(carry), (carry)←(A_7). Shift the contents of register A to the left one bit through the carry flag. {C}
RAR		1	1/4	A_m←A_{m+1}, A_7←(carry), (carry)←A_0. {C}
RLC		1	1/4	A_{m+1}←A_m, A_0←A_7 (carry)←(A_7). Shift the contents of register A to the left one bit. Shift A_7 into A and into the carry flag. {C}
RRC		1	1/4	A_m←A_{m+1}, A_7←A_0, (carry)←(A_0). {C}

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ACCUMULATOR GROUP INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
SBB	M	1	2/7	(A)←(A)−(M)−(carry), subtract the contents of M and the contents of the carry flag from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). {C,Z,S,P,C1}
SBB	r_a	1	1/4	(A)←(A)−(r_a)−(carry). {C,Z,S,P,C1}
SBI	b_2	2	2/7	(A)←(A)−<b_2>−(carry). {C,Z,S,P,C1}
STA	b_3b_2	3	4/13	[<b_3> <b_2>]←(A), store contents of A in memory address given in bytes 2 and 3.
STAX	r_c	1	2/7	[(r_c)]←(A), store contents of A in memory address given in BC or DE.
STC		1	1/4	(carry)←1, set carry flag to a 1 (true condition).
SUB	M	1	2/7	(A)←(A)−(M), subtract the contents of M from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). {C,Z,S,P,C1}
SUB	r_a	1	1/4	(A)←(A)−(r_a). {C,Z,S,P,C1}
SUI	b_2	2	2/7	(A)←(A)−<b_2>. {C,Z,S,P,C1}
XRA	M	1	2/7	(A)←(A) XOR (M), take the exclusive OR of the contents of M and register A and place in A. The carry flag will be reset. {C,Z,S,P,C1}
XRA	r_a	1	1/4	(A)←(A) XOR (r_a). {C,Z,S,P,C1}
XRI	b_2	2	2/7	(A)←(A) XOR <b_2>. {C,Z,S,P,C1}

INPUT/OUTPUT INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
IN	b_2	2	3/10	(A)← (input data from data bus), byte 2 is sent on bits A7-A0 and A15-A8 as the input device address. INP status is given on the data bus.
OUT	b_2	2	3/10	(Output data)← (A), byte 2 is sent on bits A7-A0 and A15-A8 as the output device address. OUT status is given on the data bus.

MACHINE INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
HLT		1	2/7	Halt, all machine operations stop. All registers are maintained. Only an interrupt can return the TMS 8080 to the run mode. Note that a HLT should not be placed in location zero, otherwise after the reset pin is active, the TMS 8080 will enter a nonrecoverable state (until power is removed), i.e., in halt with interrupts disabled. This condition also occurs if a HLT is executed while interrupts are disabled. HLTA status is given on the data bus.
NOP		1	1/4	(PC)← (PC)+1, no operation.

PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
CALL	b_3b_2	3	5/17	[(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PC)← <b_3> <b_2>, transfer PC to the stack address given by SP, decrement SP twice, and jump unconditionally to address given in bytes 2 and 3.
Conditional call instructions for true flags:				
(f)			5/17 (Pass)	If (f) = 1, [(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PS)←<b_3> <b_2>, otherwise (PC)← (PC)+3. If the flag specified, f, is 1, then execute a call. Otherwise, execute the next instruction.
CC (carry)	b_3b_2	3	3/11 (Fail)	
CPE (parity)	b_3b_2	3		
CM (sign)	b_3b_2	3		
CZ (zero)	b_3b_2	3		
Conditional call instructions for false flags:				
(f)			5/17 (Pass)	If (f) = 0, [(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PC)←<b_3> <b_2>, otherwise (PC)←(PC)+3.
CNC (carry)	b_3b_2	3	3/11 (Fail)	
CPO (parity)	b_3b_2	3		
CP (sign)	b_3b_2	3		
CNZ (zero)	b_3b_2	3		
DI		1	1/4	Disable interrupts. INTE is driven false to indicate that no interrupts will be accepted.
EI		1	1/4	Enable interrupts. INTE is driven true to indicate that an interrupt will be accepted. Execution of this instruction is delayed to allow the next instruction to be executed before the INT input is polled.
JMP	b_3b_2	3	3/10	(PC)← <b_3> <b_2>, jump unconditionally to address given in bytes 2 and 3.
Conditional jump instructions for true flags:				
(f)			3/10	If (f) = 1, (PC)← <b_3><b_2>, otherwise (PC)←(PC)+3. If the flag specified, f, is 1, execute a JMP. Otherwise, execute the next instruction.
JC (carry)	b_3b_2	3		
JPE (parity)	b_3b_2	3		
JM (sign)	b_3b_2	3		
JZ (zero)	b_3b_2	3		

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PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
Conditional jump instructions for false flags:				
(f)			3/10	If (f) = 0, (PC)←<b_3> <b_2>, othewise (PC)←(PC)+3.
JNC (carry)	b_3b_2	3		
JPO (parity)	b_3b_2	3		
JM (sign)	b_3b_2	3		
JNZ (zero)	b_3b_2	3		
PCHL		1	1/5	(PC)←(HL)
POP	PSW	1	3/10	(F)←[(SP)], (A)←[(SP)+1], (SP)←(SP)+2, restore the last stack values addressed by SP into A and F. Increment SP twice.
POP	r_d	1	3/10	(r_{dL})←[(SP)], (r_{dH})←[(SP)+1], (SP)←(SP)+2.
PUSH	PSW	1	3/11	[(SP)−1]←(A), [(SP)−2]←(F), (SP)←(SP)−2, save the contents of A and F into the stack addressed by SP. Decrement SP twice.
PUSH	r_d	1	3/11	[(SP)−1]←(r_{dL}), [(SP)−2]←(r_{dH}), (SP)←(SP)−2.
RET		1	3/10	(PC)←[(SP)] [(SP)+1], (SP)←(SP)+2, return to program at memory address given by last values in the stack. The SP is incremented by two.
Conditional return instructions for true flags:				
(f)			3/11 (Pass)	If (f) = 1, (PC)←[(SP)] [(SP+1], (SP)←(SP)+2. If the flag specified, f, is 1, execute a RET. Otherwise, execute the next instruction.
RC (carry)	C	1	1/5 (Fail)	
RPE (parity)	P	1		
RM (sign)	S	1		
RZ (zero)	Z	1		
Conditional return instructions for false flags:				
(f)			3/11 (Pass)	If (f) = 0, (PC)←[(SP)] [(SP)+1], (SP)←(SP)+2.
RNC (carry)	C	1	1/5 (Fail)	
RPO (parity)	P	1		
RP (sign)	S	1		
RNZ (zero)	Z	1		
RST		1	3/11	[(SP)−1] [(SP)−2] ←(PC) (SP)←(SP)−2, (PC)←0000R0$_8$ where R is a 3 bit field in RST (RST=3R7$_8$). Transfer PC to the stack address given by SP, decrement SP twice, and jump to the address specified by R.
SPHL		1	1/5	(SP)←(HL).

REGISTER GROUP INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
DCR	M	1	3/10	(M)←(M)−1, decrement the contents of memory location specified by H and L. {Z,S,P,C1}
DCR	r_a	1	1/5	(r_a)←(r_a)−1, decrement the contents of register r_a. {Z,S,P,C1}
DCX	r_b	1	1/5	(r_b)←(r_b)−1, decrement double registers BC, DE, HL, or SP.
INR	M	1	3/10	(M)←(M)+1, increment the contents of memory location specified by H and L. {Z,S,P,C1}
INR	r_a	1	1/5	(r_a)←(r_a)+1, increment the contents of register r_a. {Z,S,P,C1}
INX	r_b	1	1/5	(r_b)←(r_b)+1, increment double registers BC, DE, HL, or SP.
LHLD	b_3b_2	3	5/16	(L)←[<b_3> <b_2>]; (H)← [<b_3> <b_2>+1], load registers H and L with contents of the two memory locations specified by bytes 3 and 2.
LXI	$r_bb_3b_2$	3	3/10	(r_{bH})←<b_3>; (r_{bL})←<b_2>, load double registers BC, DE, HL, or SP immediate with bytes 3, 2, respectively.
MVI	M,b_2	2	3/10	(M)←<b_2>, store immediate byte 2 in the address specified by HL
MVI	r_ab_2	2	2/7	(r_a)←<b_2>, load register r_a immediate with byte 2 of the instruction.
MOV	Mr_a	1	2/7	(M)←(r_a), store register r_a in the memory location addressed by H and L.
MOV	r_aM	1	2/7	(r_a)←(M), load register r_a with contents of memory addressed by HL.
MOV	$r_{a1}r_{a2}$	1	1/5	(r_{a1})←(r_{a2}), load register r_{a1} with contents of r_{a2}, r_{a2} contents remain unchanged.
SHLD	b_3b_2	3	5/16	[<b_3> <b_2>]←(L); [<b_3> <b_2>+1)]←(H), store the contents of H and L into two successive memory locations specified by bytes 3 and 2.
XCHG		1	1/4	(H)↔(D); (L)↔(E), exchange double registers HL and DE
XTHL		1	5/18	(L)↔[(SP)], (H)↔[(SP)+1], (SP)=(SP), exchange the top of the stack with register HL.

TERMS AND DEFINITIONS

TERM	DEFINITION
B	Byte indicator (1=byte, 0 = word)
C	Bit count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
W	Workspace register
WRn	Workspace register n
(n)	Contents of n
a→b	a is transferred to b
|n|	Absolute value of n
+	Arithmetic addition
–	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
⊕	Logical exclusive OR
$\bar{n}$	Logical complement of n

STATUS REGISTER

The status register contains the interrupt mask level and information pertaining to the instruction operation.

0	1	2	3	4	5	6	7 8 9 10 11	12 13 14 15
ST0	ST1	ST2	ST3	ST4	ST5	ST6	not used (=0)	ST12 ST13 ST14 ST15
L>	A>	=	C	O	P	X		Interrupt Mask

BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
ST0	LOGICAL GREATER THAN	C,CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB(SA) = MSB(DA) and MSB of (DA) – (SA) = 1
		CI	If MSB(W) = 1 and MSB of IOP = 0, or if MSB(W) = MSB of IOP and MSB of IOP – (W) = 1
		ABS	If (SA) ≠ 0
		All Others	If result ≠ 0
ST1	ARITHMETIC GREATER THAN	C,CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB(DA) – (SA) = 1
		CI	If MSB(W) = 0 and MSB of IOP = 1, or if MSB(W) = MSB of IOP and MSB of IOP – (W) = 1
		ABS	If MSB(SA) = 0 and (SA) ≠ 0
		All Others	If MSB of result = 0 and result ≠ 0

BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
ST2	EQUAL	C,CB	If (SA) = (DA)
		CI	If (W) = IOP
		COC	If (SA) and ($\overline{DA}$) = 0
		CZC	If (SA) and (DA) = 0
		TB	If CRUIN = 1
		ABS	If (SA) = 0
		All Others	If result = 0
ST3	CARRY	A,AB,ABS,AI,DEC, DECT,INC,INCT, NEG,S,SB	If CARRY OUT = 1
		SLA,SRA,SRC,SRL	If last bit shifted out = 1
ST4	OVERFLOW	A,AB	If MSB(SA) = MSB(DA) and MSB of result ≠ MSB(DA)
		AI	If MSB(W) = MSB of IOP and MSB of result ≠ MSB(W)
		S,SB	If MSB(SA) ≠ MSB(DA) and MSB of result ≠ MSB(DA)
		DEC,DECT,INC,INCT	If MSB(SA) ≠ MSB of result
		SLA	If MSB changes during shift
		DIV	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of (DA) – (SA) = 0
		ABS,NEG	If (SA) = 8000_{16}
ST5	PARITY	CB,MOVB	If (SA) has odd number of 1's
		LDCR,STCR	If 1 ≤ C ≤ 8 and (SA) has odd number of 1's
		AB,SB,SOCB,SZCB	If result has odd number of 1's
ST6	XOP	XOP	If XOP instruction is executed
ST12–ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1
		RTWP	If corresponding bit of WR15 is 1

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Dual Operand Instructions with Multiple Addressing Modes for Source and Destination Operand

MNEMONIC	OP CODE 0 1 2	B 3	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
A	1 0 1	0	Add	Yes	0-4	(SA)+(DA) → (DA)
AB	1 0 1	1	Add bytes	Yes	0-5	(SA)+(DA) → (DA)
C	1 0 0	0	Compare	Yes	0-2	Compare (SA) to (DA) and set appropriate status bits
CB	1 0 0	1	Compare bytes	Yes	0-2,5	Compare (SA) to (DA) and set appropriate status bits
S	0 1 1	0	Subtract	Yes	0-4	(DA) – (SA) → (DA)
SB	0 1 1	1	Subtract bytes	Yes	0-5	(DA) – (SA) → (DA)
SOC	1 1 1	0	Set ones corresponding	Yes	0-2	(DA) OR (SA) → (DA)
SOCB	1 1 1	1	Set ones corresponding bytes	Yes	0-2,5	(DA) OR (SA) → (DA)
SZC	0 1 0	0	Set zeroes corresponding	Yes	0-2	(DA) AND ($\overline{SA}$) → (DA)
SZCB	0 1 0	1	Set zeroes corresponding bytes	Yes	0-2,5	(DA) AND ($\overline{SA}$) → (DA)
MOV	1 1 0	0	Move	Yes	0-2	(SA) → (DA)
MOVB	1 1 0	1	Move bytes	Yes	0-2,5	(SA) → (DA)

Dual Operand Instructions with Multiple Addressing Modes

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
COC	0 0 1 0 0 0	Compare ones corresponding	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	0 0 1 0 0 1	Compare zeros corresponding	No	2	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	0 0 1 0 1 0	Exclusive OR	Yes	0-2	(D) ⊕ (SA) → (D)
MPY	0 0 1 1 1 0	Multiply	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D+1 (least significant). If WR15 is D, the next word in memory after WR15 will be used for the least significant half of the product.
DIV	0 0 1 1 1 1	Divide	No	4	If unsigned (SA) is less than unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D+1) by unsigned (SA). Quotient → (D), remainder → (D+1). If D = 15, the next word in memory after WR15 will be used for the remainder.

Extended Operation (XOP) Instruction

The T_S and S fields provide multiple mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4D) \rightarrow (WP)$
$(41_{16} + 4D) \rightarrow (PC)$
SA → (new WR11)
(old WP) → (new WR13)
(old PC) → (new WR14)
(old ST) → (new WR15)

does not test interrupt requests ($\overline{INTREQ}$) upon completion of the XOP instruction.

Single Operand Instructions

The T_S and S fields provide multiple mode addressing capability for the source operand.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
B	0 0 0 0 0 1 0 0 0 1	Branch	No	–	(SA) → (PC)
BL	0 0 0 0 0 1 1 0 1 0	Branch and link	No	–	(PC) → (WR11); SA → (PC)
BLWP	0 0 0 0 0 1 0 0 0 0	Branch and load workspace pointer	No	–	(SA) → (WP);(SA+1) → (PC); (old WP) → (new WR13); (old PC) → (new WR14); (old ST) → (new WR15); the interrupt input ($\overline{INTREQ}$) is not tested upon completion of the BLWP instruction.
CLR	0 0 0 0 0 1 0 0 1 1	Clear operand	No	–	0 → (SA)
SETO	0 0 0 0 0 1 1 1 0 0	Set to ones	No	–	$FFFF_{16}$ → (SA)
INV	0 0 0 0 0 1 0 1 0 1	Invert	Yes	0-2	($\overline{SA}$) → (SA)
NEG	0 0 0 0 0 1 0 1 0 0	Negate	Yes	0-4	–(SA) → (SA)
ABS	0 0 0 0 0 1 1 1 0 1	Absolute value	No	0-4	|(SA)| → (SA)
SWPB	0 0 0 0 0 1 1 0 1 1	Swap bytes	No	–	(SA), bits 0 thru 7 → (SA), bits 8 thru 15; (SA), bits 8 thru 15 → (SA), bits 0 thru 7.
INC	0 0 0 0 0 1 0 1 1 0	Increment	Yes	0-4	(SA) + 1 → (SA)
INCT	0 0 0 0 0 1 0 1 1 1	Increment by two	Yes	0-4	(SA) + 2 → (SA)
DEC	0 0 0 0 0 1 1 0 0 0	Decrement	Yes	0-4	(SA) – 1 → (SA)
DECT	0 0 0 0 0 1 1 0 0 1	Decrement by two	Yes	0-4	(SA) – 2 → (SA)
X	0 0 0 0 0 1 0 0 1 0	Execute	No	–	Execute the instruction at SA. (see note)

NOTE: If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the TMS 9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

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CRU Multiple-Bit Instructions

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
LDCR	0 0 1 1 0 0	Load communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	0 0 1 1 0 1	Store communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

†ST5 is affected only if 1 ≤ C ≤ 8.

CRU Single-Bit Instructions

CRU relative addressing is used to address the selected CRU bit.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	STATUS BITS AFFECTED	DESCRIPTION
SBO	0 0 0 1 1 1 0 1	Set bit to one	–	Set the selected CRU output bit to 1.
SBZ	0 0 0 1 1 1 1 0	Set bit to zero	–	Set the selected CRU output bit to 0.
TB	0 0 0 1 1 1 1 1	Test bit	2	If the selected CRU input bit = 1, set ST2.

Jump Instructions

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	ST CONDITION TO LOAD PC
JEQ	0 0 0 1 0 0 1 1	Jump equal	ST2 = 1
JGT	0 0 0 1 0 1 0 1	Jump greater than	ST1 = 1
JH	0 0 0 1 1 0 1 1	Jump high	ST0 = 1 and ST2 = 0
JHE	0 0 0 1 0 1 0 0	Jump high or equal	ST0 = 1 or ST2 = 1
JL	0 0 0 1 1 0 1 0	Jump low	ST0 = 0 and ST2 = 0
JLE	0 0 0 1 0 0 1 0	Jump low or equal	ST0 = 0 or ST2 = 1
JLT	0 0 0 1 0 0 0 1	Jump less than	ST1 = 0 and ST2 = 0
JMP	0 0 0 1 0 0 0 0	Jump unconditional	unconditional
JNC	0 0 0 1 0 1 1 1	Jump no carry	ST3 = 0
JNE	0 0 0 1 0 1 1 0	Jump not equal	ST2 = 0
JNO	0 0 0 1 1 0 0 1	Jump no overflow	ST4 = 0
JOC	0 0 0 1 1 0 0 0	Jump on carry	ST3 = 1
JOP	0 0 0 1 1 1 0 0	Jump odd parity	ST5 = 1

Shift Instructions

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
SLA	0 0 0 0 1 0 1 0	Shift left arithmetic	Yes	0-4	Shift (W) left. Fill vacated bit positions with 0.
SRA	0 0 0 0 1 0 0 0	Shift right arithmetic	Yes	0-3	Shift (W) right. Fill vacated bit positions with original MSB of (W).
SRC	0 0 0 0 1 0 1 1	Shift right circular	Yes	0-3	Shift (W) right. Shift previous LSB into MSB.
SRL	0 0 0 0 1 0 0 1	Shift right logical	Yes	0-3	Shift (W) right. Fill vacated bit positions with 0's.

Immediate Register Instructions

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
AI	0 0 0 0 0 0 1 0 0 0 1	Add immediate	Yes	0-4	(W) + IOP → (W)
ANDI	0 0 0 0 0 0 1 0 0 1 0	AND immediate	Yes	0-2	(W) AND IOP → (W)
CI	0 0 0 0 0 0 1 0 1 0 0	Compare immediate	Yes	0-2	Compare (W) to IOP and set appropriate status bits
LI	0 0 0 0 0 0 1 0 0 0 0	Load immediate	Yes	0-2	IOP → (W)
ORI	0 0 0 0 0 0 1 0 0 1 1	OR immediate	Yes	0-2	(W) OR IOP → (W)

Internal Register Load Immediate Instructions

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
LWPI	0 0 0 0 0 0 1 0 1 1 1	Load workspace pointer immediate	IOP → (WP), no ST bits affected
LIMI	0 0 0 0 0 0 1 1 0 0 0	Load interrupt mask	IOP, bits 12 thru 15 → ST12 thru ST15

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Internal Register Store Instructions

No ST bits are affected.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
STST	0 0 0 0 0 0 1 0 1 1 0	Store status register	(ST) → (W)
STWP	0 0 0 0 0 0 1 0 1 0 1	Store workspace pointer	(WP) → (W)

Return Workspace Pointer (RTWP) Instruction

The RTWP instruction causes the following transfers to occur:

(WR15) → (ST)
(WR14) → (PC)
(WR13) → (WP)

External Instructions

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	STATUS BITS AFFECTED	DESCRIPTION	ADDRESS BUS A0 A1 A2
IDLE	0 0 0 0 0 0 1 1 0 1 0	Idle	–	Suspend TMS 9900 instruction execution until an interrupt, $\overline{LOAD}$, or $\overline{RESET}$ occurs	L H L
RSET	0 0 0 0 0 0 1 1 0 1 1	Reset	12–15	0 → ST12 thru ST15	L H H
CKOF	0 0 0 0 0 0 1 1 1 1 0	User defined		---	H L H
CKON	0 0 0 0 0 0 1 1 1 0 1	User defined		---	H H L
LREX	0 0 0 0 0 0 1 1 1 1 1	User defined		---	H H H

INSTRUCTION EXECUTION TIMES

Instruction execution times for the TMS 9900 are a function of:

1) Clock cycle time, $t_{c(\phi)}$
2) Addressing mode used where operands have multiple addressing mode capability
3) Number of wait states required per memory access.

Table 3 lists the number of clock cycles and memory accesses required to execute each TMS 9900 instruction. For instructions with multiple addressing modes for either or both operands, the table lists the number of clock cycles and memory accesses with all operands addressed in the workspace-register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the appropriate values from the referenced tables. The total instruction-execution time for an instruction is:

$$T = t_{c(\phi)} (C + W \cdot M)$$

where:

T = total instruction execution time;
$t_{c(\phi)}$ = clock cycle time;
C = number of clock cycles for instruction execution plus address modification;
W = number of required wait states per memory access for instruction execution plus address modification;
M = number of memory accesses.

ADDRESS MODIFICATION – TABLE A

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	8	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2

ADDRESS MODIFICATION – TABLE B

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	6	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2

INSTRUCTION EXECUTION TIMES

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST
A	14	4	A	A
AB	14	4	B	B
ABS (MSB = 0)	12	2	A	–
(MSB = 1)	14	3	A	–
AI	14	4	–	–
ANDI	14	4	–	–
B	8	2	A	–
BL	12	3	A	–
BLWP	26	6	A	–
C	14	3	A	A
CB	14	3	B	B
CI	14	3	–	–
CKOF	12	1	–	–
CKON	12	1	–	–
CLR	10	3	A	–
COC	14	3	A	–
CZC	14	3	A	–
DEC	10	3	A	–
DECT	10	3	A	–
DIV (ST4 is set)	16	3	A	–
DIV (ST4 is reset)*	92-124	6	A	–
IDLE	12	1	–	–
INC	10	3	A	–
INCT	10	3	A	–
INV	10	3	A	–
Jump (PC is changed)	10	1	–	–
(PC is not changed)	8	1	–	–
LDCR (C = 0)	52	3	A	–
(1≤C≤8)	20+2C	3	B	–
(9≤C≤15)	20+2C	3	A	–
LI	12	3	–	–
LIMI	16	3	–	–
LREX	12	1	–	–
$\overline{RESET}$ function	28	6	–	–
$\overline{LOAD}$ function	24	6	–	–
Interrupt context switch	24	6	–	–

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST
LWPI	10	2	–	–
MOV	14	4	A	A
MOVB	14	4	B	B
MPY	52	5	A	–
NEG	12	3	A	–
ORI	14	4	–	–
RSET	12	1	–	–
RTWP	14	4	–	–
S	14	4	A	A
SB	14	4	B	B
SBO	12	2	–	–
SBZ	12	2	–	–
SETO	10	3	A	–
Shift (C≠0)	12+2C	3	–	–
(C=0, Bits 12–15 of WR0=0)	52	4	–	–
(C=0, Bits 12–15 of WRP+N≠0)	20+2N	4	–	–
SOC	14	4	A	A
SOCB	14	4	B	B
STCR (C=0)	60	4	A	–
(1≤C≤7)	42	4	B	–
(C=8)	44	4	B	–
(9≤C≤15)	58	4	A	–
STST	8	2	–	–
STWP	8	2	–	–
SWPB	10	3	A	–
SZC	14	4	A	A
SZCB	14	4	B	B
TB	12	2	–	–
X **	8	2	A	–
XOP	44	8	A	–
XOR	14	4	A	–
Undefined op codes 0000-01FF,0320-033F,0C00-0FFF	6	1	–	–
0780-07FF	8	2	A	–

*Execution time is dependent upon the partial quotient after each clock cycle during execution.
**Execution time is added to the execution time of the instruction located at the source address.
†The letters A and B refer to the respective tables that follow.

IS11

		Addressing Mode							Condition Reg
		Implied	Immediate	Direct	Extended	Indexed	Relative	Boolean/Arith	5 4 3 2 1 0
Instruction	Mnemonic	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	Operation	H I N Z V C
Logical and	ANDA		84 2 2	94 3 2	B4 4 3	A4 5 2		A • M → A	• • ↕ ↕ R •
	ANDB		C4 2 2	D4 3 2	F4 4 3	E4 5 2		B • M → B	• • ↕ ↕ R •
Inclusive or	ORAA		8A 2 2	9A 3 2	BA 4 3	AA 5 2		A + M → A	• • ↕ ↕ R •
	ORAB		CA 2 2	DA 3 2	FA 4 3	EA 5 2		B + M → B	• • ↕ ↕ R •
Exclusive or	EORA		88 2 2	98 3 2	B8 4 3	A8 5 2		A ⊕ M → A	• • ↕ ↕ R •
	EORB		C8 2 2	D8 3 2	F8 4 3	E8 5 2		B ⊕ M → B	• • ↕ ↕ R •
Shift left arithmetic	ASLA	48 2 1						A/B/M: C ← b7 … b0 ← 0	• • ↕ ↕ 6 ↕
	ASLB	58 2 1							• • ↕ ↕ 6 ↕
	ASL				78 6 3	68 7 2			• • ↕ ↕ 6 ↕
Shift right arithmetic	ASRA	47 2 1						A/B/M: b7 … b0 → C	• • ↕ ↕ 6 ↕
	ASRB	57 2 1							• • ↕ ↕ 6 ↕
	ASR				77 6 3	67 7 2			• • ↕ ↕ 6 ↕
Shift right logical	LSRA	44 2 1						A/B/M: 0 → b7 … b0 → C	• • R ↕ 6 ↕
	LSRB	54 2 1							• • R ↕ 6 ↕
	LSR				74 6 3	64 7 2			• • R ↕ 6 ↕
Rotate left	ROLA	49 2 1						A/B/M: C ← b7 … b0	• • ↕ ↕ 6 ↕
	ROLB	59 2 1							• • ↕ ↕ 6 ↕
	ROL				79 6 3	69 7 2			• • ↕ ↕ 6 ↕
Rotate right	RORA	46 2 1						A/B/M: C → b7 … b0	• • ↕ ↕ 6 ↕
	RORB	56 2 1							• • ↕ ↕ 6 ↕
	ROR				76 6 3	66 7 2			• • ↕ ↕ 6 ↕
Compare accumulators	CBA	11 2 1						A − B	• • ↕ ↕ ↕ ↕
Compare	CMPA		81 2 2	91 3 2	B1 4 3	A1 5 2		A − M	• • ↕ ↕ ↕ ↕
	CMPB		C1 2 2	D1 3 2	F1 4 3	E1 5 2		B − M	• • ↕ ↕ ↕ ↕
Compare index register	CPX		8C 3 3	9C 4 2	BC 5 3	AC 6 2		X_H − M, X_L − (M+1)	• • 7 ↕ 8 •
Test (zero or minus)	TSTA	4D 2 1						A − 00	• • ↕ ↕ R R
	TSTB	5D 2 1						B − 00	• • ↕ ↕ R R
	TST				7D 6 3	6D 7 2		M − 00	• • ↕ ↕ R R
Bit test	BITA		85 2 2	95 3 2	B5 4 3	A5 5 2		A • M	• • ↕ ↕ R •
	BITB		C5 2 2	D5 3 2	F5 4 3	E5 5 2		B • M	• • ↕ ↕ R •
								TEST	
Branch	BRA						20 4 2		• • • • • •
Branch if carry clear	BCC						24 4 2	C = 0	• • • • • •
Branch if carry set	BCS						25 4 2	C = 1	• • • • • •
Branch if overflow clear	BVC						28 4 2	V = 0	• • • • • •
Branch if overflow set	BVS						29 4 2	V = 1	• • • • • •
Branch if equal to zero	BEQ						27 4 2	Z = 1	• • • • • •
Branch if greater or equal to zero	BGE						2C 4 2	N ⊕ V = 0	• • • • • •
Branch if greater than zero	BGT						2E 4 2	Z + (N ⊕ V) = 0	• • • • • •
Branch if less than zero	BLT						2D 4 2	N ⊕ V = 1	• • • • • •
Branch if less than or equal to zero	BLE						2F 4 2	Z + (N ⊕ V) = 1	• • • • • •
Branch if not equal to zero	BNE						26 4 2	Z = 0	• • • • • •
Branch if minus	BMI						2B 4 2	N = 1	• • • • • •
Branch if plus	BPL						2A 4 2	N = 0	• • • • • •
Branch if higher	BHI						22 4 2	C + Z = 0	• • • • • •
Branch if lower or same	BLS						23 4 2	C + Z = 1	• • • • • •

OP = Operation Code MC = Number of MPU Cycles PB = Number of Program Bytes

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		Addressing Mode																Condition Reg					
		Implied			Immediate			Direct			Extended			Indexed			Relative			Boolean/Arith	5	4	3	2	1	0
Instruction	Mnemonic	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP MC PB			Operation	H	I	N	Z	V	C
Load accumulator	LDAA				86	2	2	96	3	2	B6	4	3	A6	5	2				M → A	•	•	↕	↕	R	•
	LDAB				C6	2	2	D6	3	2	F6	4	3	E6	5	2				M → B	•	•	↕	↕	R	•
Load stack pointer	LDS				8E	3	3	9E	4	2	BE	5	3	AE	6	2				M → SP_H, (M + 1) → SP_L	•	•	↕	↕	R	•
Load index register	LDX				CE	3	3	DE	4	2	FE	5	3	EE	6	2				M → X_H, (M + 1) → X_L	•	•	↕	↕	R	•
Store accumulator	STAA							97	4	2	B7	5	3	A7	6	2				A → M	•	•	↕	↕	R	•
	STAB							D7	4	2	F7	5	3	E7	6	2				B → M	•	•	↕	↕	R	•
Store stack pointer	STS							9F	5	2	BF	6	3	AF	7	2				SP_H → M, SP_L → (M + 1)	•	•	↕	↕	R	•
Store index register	STX							DF	5	2	FF	6	3	EF	7	2				X_H → M, X_L → (M + 1)	•	•	↕	↕	R	•
Transfer accumulators	TAB	16	2	1																A → B	•	•	↕	↕	R	•
	TBA	17	2	1																B → A	•	•	↕	↕	R	•
Transfer Acc. to cond. reg.	TAP	06	2	1																A → CCR	Note 12					
Transfer cond. reg. to Acc.	TPA	07	2	1																CCR → A	•	•	•	•	•	•
Transfer stck ptr to index	TSX	30	4	1																SP + 1 → X	•	•	•	•	•	•
Transfer index to stck ptr	TXS	35	4	1																X − 1 → SP	•	•	•	•	•	•
Pull data	PULA	32	4	1																SP + 1 → SP, M_{SP} → A	•	•	•	•	•	•
	PULB	33	4	1																SP + 1 → SP, M_{SP} → B	•	•	•	•	•	•
Push data	PSHA	36	4	1																A → M_{SP}, SP − 1 → SP	•	•	•	•	•	•
	PSHB	37	4	1																B → M_{SP}, SP − 1 → SP	•	•	•	•	•	•
Add accumulators	ABA	1B	2	1																A + B → A	↕	•	↕	↕	↕	↕
Add	ADDA				8B	2	2	9B	3	2	BB	4	3	AB	5	2				A + M → A	↕	•	↕	↕	↕	↕
	ADDB				CB	2	2	DB	3	2	FB	4	3	EB	5	2				B + M → B	↕	•	↕	↕	↕	↕
Add with carry	ADCA				89	2	2	99	3	2	B9	4	3	A9	5	2				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB				C9	2	2	D9	3	2	F9	4	3	E9	5	2				B + M + C → B	↕	•	↕	↕	↕	↕
Subtract accumulators	SBA	10	2	1																A − B → A	•	•	↕	↕	↕	↕
Subtract	SUBA				80	2	2	90	3	2	B0	4	3	A0	5	2				A − M → A	•	•	↕	↕	↕	↕
	SUBB				C0	2	2	D0	3	2	F0	4	3	E0	5	2				B − M → B	•	•	↕	↕	↕	↕
Subtract with carry	SBCA				82	2	2	92	3	2	B2	4	3	A2	5	2				A − M − C → A	•	•	↕	↕	↕	↕
	SBCB				C2	2	2	D2	3	2	F2	4	3	E2	5	2				B − M − C → B	•	•	↕	↕	↕	↕
Increment	INCA	4C	2	1																A + 1 → A	•	•	↕	↕	5	•
	INCB	5C	2	1																B + 1 → B	•	•	↕	↕	5	•
	INC										7C	6	3	6C	7	2				M + 1 → M	•	•	↕	↕	5	•
Increment stack pointer	INS	31	4	1																SP + 1 → SP	•	•	•	•	•	•
Increment index reg.	INX	08	4	1																X + 1 → X	•	•	•	↕	•	•
Decrement	DECA	4A	2	1																A − 1 → A	•	•	↕	↕	4	•
	DECB	5A	2	1																B − 1 → B	•	•	↕	↕	4	•
	DEC										7A	6	3	6A	7	2				M − 1 → M	•	•	↕	↕	4	•
Decrement stack pointer	DES	34	4	1																SP − 1 → SP	•	•	•	•	•	•
Decrement index register	DEX	09	4	1																X − 1 → X	•	•	•	↕	•	•
Complement (1's)	COMA	43	2	1																$\overline{A}$ → A	•	•	↕	↕	R	S
	COMB	53	2	1																$\overline{B}$ → B	•	•	↕	↕	R	S
	COM										73	6	3	63	7	2				$\overline{M}$ → M	•	•	↕	↕	R	S
Complement (2's)	NEGA	40	2	1																00 − A → A	•	•	↕	↕	1	2
	NEGB	50	2	1																00 − B → B	•	•	↕	↕	1	2
	NEG										70	6	3	60	7	2				00 − M → M	•	•	↕	↕	1	2
Decimal adjust accumulator	DAA	19	2	1																	•	•	↕	↕	↕	3

OP = Operation Code MC = Number of MPU Cycles PB = Number of Program Bytes

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		Addressing Modes							Condition Reg.
		Implied	Direct	Immediate	Extended	Indexed	Relative	Boolean/Arith	5 4 3 2 1 0
Instruction	Mnemonic	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	Operation	H I N Z V C
Branch to subroutine	BSR						8D 8 2		• • • • • •
Jump to subroutine	JSR				BD 9 3	AD 8 2		See Special Operations	• • • • • •
Jump	JMP				7E 3 3	6E 4 2			• • • • • •
Return from subroutine	RTS	39 5 1							• • • • • •
Return from interrupt	RTI	3B 10 1							Note 10
Software interrupt	SWI	3F 12 1							• S • • • •
Wait for interrupt	WAI	3E 9 1							• ‡ • • • •
No operation	NOP	02 2 1						PC + 1 → PC	• • • • • •
Clear	CLRA	4F 2 1						00 → A	• • R S R R
	CLRB	5F 2 1						00 → B	• • R S R R
	CLR				7F 6 3	6F 7 2		00 → M	• • R S R R
Clear carry	CLC	0C 2 1						0 → C	• • • • • R
Clear interrupt mask	CLI	0E 2 1						0 → I	• R • • • •
Clear overflow	CLV	0A 2 1						0 → V	• • • • R •
Set carry	SEC	0D 2 1						1 → C	• • • • • S
Set interrupt mask	SEI	0F 2 1						1 → I	• S • • • •
Set overflow	SEV	0B 2 1						1 → V	• • • • S •

CONDITION CODE SYMBOLS:

- H Half-carry from bit 3;
- I Interrupt mask
- N Negative (sign bit)
- Z Zero (byte)
- V Overflow, 2's complement
- C Carry from bit 7
- R Reset Always
- S Set Always
- ‡ Test and set if true, cleared otherwise
- • Not Affected

LEGEND:

- OP Operation Code (Hexadecimal):
- MC Number of MPU Cycles;
- PB Number of Program Bytes;
- + Arithmetic Plus;
- − Arithmetic Minus;
- • Boolean AND;
- M_{SP} Contents of memory location pointed to by Stack Pointer;
- + Boolean Inclusive OR;
- ⊕ Boolean Exclusive OR;
- $\overline{M}$ Complement of M;
- → Transfer Into;
- 0 Bit = Zero;
- 00 Byte = Zero;

Note – Accumulator addressing mode instructions are included in the IMPLIED addressing.

CONDITION CODE REGISTER NOTES:

(Bit set if test is true and cleared otherwise)

1 (Bit V) Test: Result = 10000000?
2 (Bit C) Test: Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N • C after shift has occurred.
7 (Bit N) Test: Sign bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs, if previously set, a Non-Maskable Interrupt is required to exit the wait state.
12 (ALL) Set according to the contents of Accumulator A

MICROPROCESSOR INSTRUCTION SET

	MNEMONIC	OP CODE	FORMAT*	DESCRIPTION OF OPERATION	AFFECTS	CYCLES
LOAD/STORE	LOD Z	000 000	1Z	Load Register Zero	CC (Note 1)	2
	LOD I	000 001	2I	Load Immediate	CC (Note 1)	2
	LOD R	000 010	2R	Load Relative	CC (Note 1)	3
	LOD A	000 011	3A	Load Absolute	CC (Note 1)	4
	STR Z	110 000	1Z	Store Register Zero (r ≠ 0)	CC (Note 1)	2
	STR R	110 010	2R	Store Relative		3
	STR A	110 011	3A	Store Absolute		4
ARITHMETIC	ADD Z	100 000	1Z	Add to Register Zero w wo Carry	C, CC (Note 1), IDC, OVF	2
	ADD I	100 001	2I	Add Immediate w wo Carry	C, CC (Note 1), IDC, OVF	2
	ADD R	100 010	2R	Add Relative w wo Carry	C, CC (Note 1), IDC, OVF	3
	ADD A	100 011	3A	Add Absolute w/wo Carry	C, CC (Note 1), IDC, OVF	4
	SUB Z	101 000	1Z	Subtract from Register Zero w wo Borrow	C, CC (Note 1), IDC, OVF	2
	SUB I	101 001	2I	Subtract Immediate w wo Borrow	C, CC (Note 1), IDC, OVF	2
	SUB R	101 010	2R	Subtract Relative w/wo Borrow	C, CC (Note 1), IDC, OVF	3
	SUB A	101 011	3A	Subtract Absolute w wo Borrow	C, CC (Note 1), IDC, OVF	4
	DAR	100 101	1Z	Decimal Adjust Register	CC (Note 2)	3
LOGICAL	AND Z	010 000	1Z	AND to Register Zero (r ≠ 0)	CC (Note 1)	2
	AND I	010 001	2I	AND Immediate	CC (Note 1)	2
	AND R	010 010	2R	AND Relative	CC (Note 1)	3
	AND A	010 011	3A	AND Absolute	CC (Note 1)	4
	IOR Z	011 000	1Z	Inclusive OR to Register Zero	CC (Note 1)	2
	IOR I	011 001	2I	Inclusive OR Immediate	CC (Note 1)	2
	IOR R	011 010	2R	Inclusive OR Relative	CC (Note 1)	3
	IOR A	011 011	3A	Inclusive OR Absolute	CC (Note 1)	4
	EOR Z	001 000	1Z	Exclusive OR to Register Zero	CC (Note 1)	2
	EOR I	001 001	2I	Exclusive OR Immediate	CC (Note 1)	2
	EOR R	001 010	2R	Exclusive OR Relative	CC (Note 1)	3
	EOR A	001 011	3A	Exclusive OR Absolute	CC (Note 1)	4
COMPARE	COM Z	111 000	1Z	Compare to Register Zero Arithmetic/Logical	CC (Note 3)	2
	COM I	111 001	2I	Compare Immediate Arithmetic/Logical	CC (Note 4)	2
	COM R	111 010	2R	Compare Relative Arithmetic/Logical	CC (Note 4)	3
	COM A	111 011	3A	Compare Absolute Arithmetic/Logical	CC (Note 4)	4
ROTATE	RRR	010 100	1Z	Rotate Register Right w/wo Carry	C, CC, IDC, OVF	2
	RRL	110 100	1Z	Rotate Register Left w/wo Carry	C, CC, IDC, OVF	2
BRANCH	BCT R	000 110	2R	Branch On Condition True Relative	–	3
	BCT A	000 111	3B	Branch On Condition True Absolute	–	3
	BCF R	100 110	2R	Branch On Condition False Relative	–	3
	BCF A	100 111	3B	Branch On Condition False Absolute	–	3
	BRN R	010 110	2R	Branch On Register Non-Zero Relative	–	3
	BRN A	010 111	3B	Branch On Register Non-Zero Absolute	–	3
	BIR R	110 110	2R	Branch On Incrementing Register Relative	–	3
	BIR A	110 111	3B	Branch On Incrementing Register Absolute	–	3
	BDR R	111 110	2R	Branch On Decrementing Register Relative	–	3
	BDR A	111 111	3B	Branch On Decrementing Register Absolute	–	3
	ZBRR	100 110 11	2ER	Zero Branch Relative, Unconditional	–	3
	BXA	100 111 11	3EB	Branch Indexed Absolute, Unconditional (Note 5)	–	3
SUBROUTINE BRANCH/RETURN	BST R	001 110	2R	Branch To Subroutine On Condition True, Relative	SP	3
	BST A	001 111	3B	Branch To Subroutine On Condition True, Absolute	SP	3
	BSF R	101 110	2R	Branch To Subroutine On Condition False, Relative	SP	3
	BSF A	101 111	3B	Branch To Subroutine On Condition False, Absolute	SP	3
	BSN R	011 110	2R	Branch To Subroutine On Non-Zero Register, Relative	SP	3
	BSN A	011 111	3B	Branch To Subroutine On Non-Zero Register, Absolute	SP	3
	ZBSR	101 110 11	2ER	Zero Branch To Subroutine Relative, Unconditional	SP	3
	BSXA	101 111 11	3EB	Branch To Subroutine, Indexed, Absolute Unconditional (note 5)	SP	3
	RET C	000 101	1Z	Return From Subroutine, Conditional	SP	3
	RET E	001 101	1Z	Return From Subroutine and Enable Interrupt, Conditional	SP, II	3
INPUT/OUTPUT	WRTD	111 100	1Z	Write Data	–	2
	REDD	011 100	1Z	Read Data	CC (Note 1)	2
	WRTC	101 100	1Z	Write Control	–	2
	REDC	001 100	1Z	Read Control	CC (Note 1)	2
	WRTE	110,101	2I	Write Extended	–	3
	REDE	010 101	2I	Read Extended	CC (Note 1)	3
MISC.	HALT	010 000 00	1E	Halt, Enter Wait State	–	2
	NOP	110 000 00	1E	No Operation	–	2
	TMI	111 101	2I	Test Under Mask Immediate	CC (Note 6)	3
PROGRAM STATUS	LPS U	100 100 10	1E	Load Program Status, Upper	F, II, SP	2
	LPS L	100 100 11	1E	Load Program Status, Lower	CC, IDC, RS, WC, OVF, COM, C	2
	SPS U	000 100 10	1E	Store Program Status, Upper	CC (Note 1)	2
	SPS L	000 100 11	1E	Store Program Status, Lower	CC (Note 1)	2
	CPS U	011 101 00	2EI	Clear Program Status, Upper, Masked	F, II, SP	3
	CPS L	011 101 01	2EI	Clear Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	PPS U	011 101 10	2EI	Preset Program Status, Upper, Masked	F, II, SP	3
	PPS L	011 101 11	2EI	Preset Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	TPS U	101 101 00	2EI	Test Program Status, Upper, Masked	CC (Note 6)	3
	TPS L	101 101 01	2EI	Test Program Status, Lower, Masked	CC (Note 6)	3

***FORMAT CODE: The number indicates the number of bytes. The letter(s) indicate the format type(s). See other side**

NOTES:
1. Condition code (CC1, CC0): 01 if positive, 00 if zero, 10 if negative.
2. Condition code is set to a meaningless value.
3. Condition code (CC1, CC0): 01 if R0 > r, 00 if R0 = r, 10 if R0 < r
4. Condition code (CC1, CC0): 01 if r > V, 00 if r = V, 10 if r < V.
5. Index register must be register 3, or 3'
6. Condition code (CC1, CC0): 00 if all selected bits are 1s, 10 if not all the selected bits are 1s.

PROGRAM STATUS WORD

PSU

7	6	5	4	3	2	1	0
S	F	II	Not Used	Not Used	SP2	SP1	SP0

S Sense
F Flag
II Interrupt Inhibit
SP2 Stack Pointer Two
SP1 Stack Pointer One
SP0 Stack Pointer Zero

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

CC1 Condition Code One
CC0 Condition Code Zero
IDC Interdigit Carry
RS Register Bank Select
WC With/Without Carry
OVF Overflow
COM Logical/Arith Compare
C Carry/Borrow

FUNCTION DESCRIPTION

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
0	I	XX	–	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	**Logically AND AC with the K-bus.** Add the result to R_n and carry input (CI). Deposit the sum in AC and R_n.
		OO	ILR	$R_n + CI \rightarrow R_n, AC$	Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the result in AC.
		II	ALR	$AC + R_n + CI \rightarrow R_n, AC$	Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.
0	II	XX	–	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		II	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
0	III	XX	–	$AT_L \wedge \overline{(I_L \wedge K_L)} \rightarrow RO$ $LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)] \vee [AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	None
		OO	SRA	$AT_L \rightarrow RO \quad AT_H \rightarrow AT_L \quad LI \rightarrow AT_H$	Shift AC or T, as specified, right one bit position. Place the previous low order bit value on RO and fill the high order bit from the data on LI. Used to shift or rotate AC or T right one bit.
1	I	XX	–	$K \vee R_n \rightarrow MAR$ $R_n + K + CI \rightarrow R_n$	**Logically OR R_n with the K-bus.** Deposit the result in MAR. Add the K-bus to R_n and CI. Deposit the result in R_n.
		OO	LMI	$R_n \rightarrow MAR \quad R_n + CI \rightarrow R_n$	Load MAR from R_n. Conditionally increment R_n. Used to maintain a macro-instruction program counter.
		II	DSM	$11 \rightarrow MAR \quad R_n - 1 + CI \rightarrow R_n$	Set MAR to all one's. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement R_n.

F GROUP	R GROUP	K BUS	NAME	EQUATION	
1	II	XX	–	$K \vee M \rightarrow MAR$ $M + K + CI \rightarrow AT$	**Logically OR the M-bus with the K-bus.** Deposit the result in MAR. Add the K-bus to the M-bus and CI. Deposit the sum in AC or T.
		OO	LMM	$M \rightarrow MAR \quad M + CI \rightarrow AT$	Load MAR from the M-bus. Add CI to the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.
		II	LDM	$11 \rightarrow MAR$ $M - 1 + CI \rightarrow AT$	Set MAR to all ones. Subtract one from the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.
1	III	XX	–	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	**Logically OR the K-bus with the complement of AC or T, as specified.** Add the result to the logical AND of specified register with the K-bus. Add the sum to CI. Deposit the result in the specified register.
		OO	CIA	$\overline{AT} + CI \rightarrow AT$	Add CI to the complement of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.
		II	DCA	$AT - 1 + CI \rightarrow AT$	Subtract one from AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.
2	I	XX	–	$(AC \wedge K) - 1 + CI \rightarrow R_n$ **(See Note 1)**	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in R_n.
		OO	CSR	$CI - 1 \rightarrow R_n$ **(See Note 1)**	Subtract one from CI and deposit the difference in R_n. Used to conditionally clear or set R_n to all 0's or 1's, respectively.
		II	SDR	$AC - 1 + CI \rightarrow R_n$ **(See Note 1)**	Subtract one from AC and add the difference to CI. Deposit the sum in R_n. Used to store AC in R_n or to store the decremented value of AC in R_n.
2	II	XX	–	$(AC \wedge K) - 1 + CI \rightarrow AT$ **(See Note 1)**	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$ **(See Note 1)**	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		II	SDA	$AC - 1 + CI \rightarrow AT$ **(See Note 1)**	Subtract one from AC and add the difference to CI. Deposit the sum in AC or T. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.

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FUNCTION DESCRIPTION (CONT'D)

IS13 Cont'd

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
2	III	XX	–	(I ∧ K) – 1 + CI → AT (See Note 1)	Logically AND the data of the K-bus with the data on the I-bus. Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CAS	CI –1 → AT	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		II	LDI	I – 1 + CI → AT	Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified. Used to load input bus data or decremented input bus data in the specified register.
3	I	XX	–	R_n + (AC ∧ K) + CI → R_n	Logically AND AC with the K-bus. Add R_n and CI to the result. Deposit the sum in R_n.
		OO	INR	R_n + CI → R_n	Add CI to R_n and deposit the sum in R_n. Used to increment R_n.
		II	ADR	AC + R_n + CI → R_n	Add AC to R_n. Add the result to CI and deposit the sum in R_n. Used to add the accumulator to a register or to add the incremented value of the accumulator to a register.
3	II	XX	–	M + (AC ∧ K) + CI → AT	Logically AND AC with the K-bus. Add the result to CI and the M-bus Deposit the sum in AC or T.
		OO	ACM	M + CI → AT	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		II	AMA	M + AC + CI → AT	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
3	III	XX	–	AT + (I ∧ K) + CI → AT	Logically AND the K-bus with the I-bus. Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.
		OO	INA	AT + CI → AT	Conditionally increment AC or T. Used to increment AC or T.
		II	AIA	I + AT + CI → AT	Add the I-bus to AC or T. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.
4	I	XX	–	CI ∨ (R_n ∧ AC ∧ K) → CO R_n ∧ (AC ∧ K) → R_n	Logically AND the K-bus with AC. Logically AND the result with the contents of R_n. Deposit the final result in R_n. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.
		OO	CLR	CI → CO 0 → R_n	Clear R_n to all 0's. Force CO to CI. Used to clear a register and force CO to CI.
		II	ANR	CI ∨ (R_n ∧ AC) → CO R_n ∧ AC → R_n	Logically AND AC with R_n. Deposit the result in R_n. Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.
4	II	XX	–	CI ∨ (M ∧ AC ∧ K) → CO M ∧ (AC ∧ K) → AT	Logically AND the K-bus with AC. Logically AND the result with the M-bus. Deposit the final result in AC or T. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO 0 → AT	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
		II	ANM	CI ∨ (M ∧ AC) → CO M ∧ AC → AT	Logically AND the M-bus with AC. Deposit the result in AC or T. Force CO to one if the result is non-zero. Used to AND M-bus data to the accumulator and test for a zero result.
4	III	XX	–	CI ∨ (AT ∧ I ∧ K) → CO AT ∧ (I ∧ K) → AT	Logically AND the I-bus with the K-bus. Logically AND the result with AC or T. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO 0 → AT	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
		II	ANI	CI ∨ (AT ∧ I) → CO AT ∧ I → AT	Logically AND the I-bus with AC or T, as specified Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.
5	I	XX	–	CI ∨ (R_n ∧ K) → CO K ∧ R_n → R_n	Logically AND the K-bus with R_n. Deposit the result in R_n. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLR	CI → CO 0 → R_n	Clear R_n to all 0's Force CO to CI. Used to clear a register and force CO to CI.
		II	TZR	CI ∨ R_n → CO R_n → R_n	Force CO to one if R_n is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register for masking and, optionally, testing for a zero result.
5	II	XX	–	CI ∨ (M ∧ K) → CO K ∧ M → AT	Logically AND the K-bus with the M-bus. Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO 0 → AT	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
		II	LTM	CI ∨ M → CO M → AT	Load AC or T, as specified, from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for a zero result. Also used to AND the K-bus with the M-bus for masking and, optionally, testing for a zero result.
5	III	XX	–	CI ∨ (AT ∧ K) → CO K ∧ AT → AT	Logically AND the K-bus with AC or T, as specified. Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO 0 → AT	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
		II	TZA	CI ∨ AT → CO AT → AT	Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND the K-bus to the specified register for masking and, optionally, testing for a zero result.

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F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
6	I	XX	–	CI ∨ (AC ∧ K) → CO R_n ∨ (AC ∧ K) → R_n	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the result of the carry OR on CO. Logically OR R_n with the logical AND of AC and the K-bus. Deposit the result in R_n.
		OO	NOP	CI → CO R_n → R_n	Force CO to CI. Used as a null operation or to force CO to CI.
		II	ORR	CI ∨ AC → CO R_n ∨ AC → R_n	Force CO to one if AC is non-zero. Logically OR AC with R_n. Deposit the result in R_n. Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.
6	II	XX	–	CI ∨ (AC ∧ K) → CO M ∨ (AC ∧ K) → AT	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the carry OR on CO. Logically OR the M-bus, with the logical AND of AC and the K-bus. Deposit the final result in AC or T.
		OO	LMF	CI → CO M → AT	Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to CI.
		II	ORM	CI ∨ AC → CO M ∨ AC → AT	Force CO to one if AC is non-zero. Logically OR the M-bus with AC. Deposit the result in AC or T, as specified. Used to OR M-bus with the AC and, optionally, test the previous value of AC for zero.
6	III	XX	–	CI ∨ (I ∧ K) → CO AT ∨ (I ∧ K) → AT	Logically OR CI with the word-wise OR of the logical AND of the I-bus and the K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Logically OR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	NOP	CI → CO R_n → R_n	Force CO to CI. Used as a null operation or to force CO to CI.
		II	ORI	CI ∨ I → CO I ∨ AT → AT	Force CO to one if the data on the I-bus is non-zero. Logically OR the I-bus to AC or T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.

FUNCTION DESCRIPTION (CONT'D)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
7	I	XX	–	CI ∨ (R_n ∧ AC ∧ K) → CO R_n ⊕ (AC ∧ K) → R_n	Logically OR CI with the word-wise OR of the logical AND of R_n and AC and the K-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive-NOR the result with R_n. Deposit the final result in R_n.
		OO	CMR	CI → CO $\overline{R_n}$ → R_n	Complement the contents of R_n. Force CO to CI.
		II	XNR	CI ∨ (R_n ∧ AC) → CO R_n ⊕ AC → R_n	Force CO to one if the logical AND of AC and R_n is non-zero. Exclusive-NOR AC with R_n. Deposit the result in R_n. Used to exclusive-NOR the accumulator with a register.
7	II	XX	–	CI ∨ (M ∧ AC ∧ K) → CO M ⊕ (AC ∧ K) → AT	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus and M-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive NOR the result with the M-bus. Deposit the final result in AC or T.
		OO	LCM	CI → CO $\overline{M}$ → AT	Load the complement of the M-bus into AC or T, as specified. Force CO to CI.
		II	XNM	CI ∨ (M ∧ AC) → CO M ⊕ AC → AT	Force CO to one if the logical AND of AC and the M-bus is non-zero. Exclusive-NOR AC with the M-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR memory data with the accumulator.
7	III	XX	–	CI ∨ (AT ∧ I ∧ K) → CO AT ⊕ (I ∧ K) → AT	Logically OR CI with the word-wise OR of the logical AND of the specified register and the I-bus and K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Exclusive-NOR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	CMA	CI → CO $\overline{AT}$ → AT	Complement AC or T, as specified. Force CO to CI.
		II	XNI	CI ∨ (AT ∧ I) → CO I ⊕ AT → AT	Force CO to one if the logical AND of the specified register and the I-bus is non-zero. Exclusive-NOR AC with the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

ADDRESS CONTROL FUNCTION SUMMARY

MNEMONIC	DESCRIPTION	FUNCTION AC_8	5	4	3	2	1	0	NEXT ROW MA_8	7	6	5	4	NEXT COL MA_3	2	1	0
JCC	Jump in current column	0	0	d_4	d_3	d_2	d_1	d_0	d_4	d_3	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JZR	Jump to zero row	0	1	0	d_3	d_2	d_1	d_0	0	0	0	0	0	d_3	d_2	d_1	d_0
JCR	Jump in current row	0	1	1	d_3	d_2	d_1	d_0	m_8	m_7	m_6	m_5	m_4	d_3	d_2	d_1	d_0
JCE	Jump in column/enable	1	1	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JFL	Jump/test F latch	1	0	0	d_3	d_2	d_1	d_0	m_8	d_3	d_2	d_1	d_0	m_3	0	1	f
JCF	Jump/test C flag	1	0	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	c
JZF	Jump/test Z flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	z
JPR	Jump/test PR latch	1	1	0	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	p_3	p_2	p_1	p_0
JLL	Jump/test left PR bits	1	1	0	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	0	1	p_3	p_2
JRL	Jump/test right PR bits	1	1	1	1	1	d_1	d_0	m_8	m_7	1	d_1	d_0	1	1	p_1	p_0
JPX	Jump/test PX bus	1	1	1	1	0	d_1	d_0	m_8	m_7	m_6	d_1	d_0	x_7	x_6	x_5	x_4

NOTE
d_n = Data on address control line n
m_n = Data in microprogram address register bit n
p_n = Data in PR latch bit n
x_n = Data on PX bus line n (active LOW)
f, c, z = Contents of F latch, C flag, or Z flag respectively

FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC_1	0
Flag Input	SCZ	Set C flag and Z flag to f	0	0
	STZ	Set Z flag to f	0	1
	STC	Set C flag to f	1	0
	HCZ	Hold C flag and Z flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC_3	2
Flag Output	FF0	Force FO to 0	0	0
	FFC	Force FO to C flag	0	1
	FFZ	Force FO to Z flag	1	0
	FF1	Force FO to 1	1	1

LOAD FUNCTION	NEXT ROW					NEXT COL			
LD	MA_8	7	6	5	4	MA_3	2	1	0
0	See Appendix A					See Appendix A			
1	0	x_3	x_2	x_1	x_0	x_7	x_6	x_5	x_4

NOTE
f = Contents of the F latch
x_n = Data on PX or SX bus line n (active LOW)

INSTRUCTION SET

HEX CODING		MNEMONIC OPR	MNEMONIC OPA	DESCRIPTION OF OPERATION
0	0	NOP		No operation
1 A_2	C_X A_1	JCN	C_X LABEL	Jump on condition C_X to the program memory address A_1, A_2, otherwise continue in sequence. (see back cover.)
2 D_2	P_X0 D_1	FIM D_2	P_X D_1	Fetch immediate from program memory data D_1, D_2 to index register pair P_X.
2	P_X1	SRC	P_X	Send register control. Send the contents of index register pair P_X to I/O ports and RAM register as chip select and RAM character address.
3	P_X0	FIN	P_X	Fetch indirect. Send contents of register pair 0 out as a program memory address. Data fetched is placed into register pair P_X.
3	P_X1	JIN	P_X	Jump indirect. Jump to the program memory address designated by contents of register pair P_X.
4 A_2	A_3 A_1	JUN	 LABEL	Jump unconditional to program memory address A_1, A_2, A_3.
5 A_2	A_3 A_1	JMS	 LABEL	Jump to subroutine located at program memory address A_1, A_2, A_3. Save previous address (push down in stack.)
6	R_X	INC	R_X	Increment contents of register R_X.
7 A_2	R_X A_1	ISZ	R_X LABEL	Increment and step on zero. Increment contents of register R_X, if result is not 0 go to program memory address A_1, A_2, otherwise step to the next instruction in sequence.
8	R_X	ADD	R_X	Add contents of register R_X to accumulator.
9	R_X	SUB	R_X	Subtract contents of register R_X to accumulator with borrow.
A	R_X	LD	R_X	Load contents of register $R_X$to accumulator.
B	R_X	XCH	R_X	Exchange contents of index register R_X and accumulator.
C	D_X	BBL	D_X	Branch back one level in stack to the program memory address stored by a prior JMS instruction. Load data D_X to accumulator.
D	D_X	LDM	D_X	Load data D_X to accumulator.
E	X	I - O and RAM register instructions.		
F	X	Accumulator instructions.		

A_1 Low order address bits
A_2 High order address bits
A_3 Chip select

P_X1 Register pairs P_0 through P_7 designated by odd characters 1, 3, 5, 7, 9, B, D, F
P_X0 Register pairs P_0 through P_7 designated by even characters 0, 2, 4, 6, 8, A, C, E

R_X Register 0 —— F

D_X Data
D_1 Data for odd register
D_2 Data for even register

C_X Jump conditions

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I/O AND RAM REGISTER INSTRUCTIONS

HEX CODING	MNEMONIC OPR	MNEMONIC OPA	DESCRIPTION OF OPERATION
E 0	WRM		Write the contents of the accumulator into the previously selected RAM register character.
E 1	WMP		Write the contents of the accumulator into the previously selected RAM output port (Output lines.)
E 2	WRR		Write the contents of the accumulator into the previously selected output port. (I/O lines.)
E 3	WPM		Write the contents of the accumulator into the previously selected RAM program memory.
E 4	WRO		Write the contents of the accumulator into the previously selected RAM status character).
E 5	WR1		Write the contents of the accumulator into the previously selected RAM status character 1.
E 6	WR2		Write the contents of the accumulator into the previously selected RAM status character 2.
E 7	WR3		Write the contents of the accumulator into the previously selected RAM status character 3.
E 8	SBM		Subtract the previously selected RAM register character from accumulator with borrow.
E 9	RDM		Read the previously selected RAM register character into the accumulator.
E A	RDR		Read the contents of the previously selected input port into the accumulator. (I/O lines.)
E B	ADM		Add the previously selected RAM register character to accumulator with carry.
E C	RDO		Read the previously selected RAM status character 0 into accumulator.
E D	RD1		Read the previously selected RAM status character 1 into accumulator.
E E	RD2		Read the previously selected RAM status character 2 into accumulator.
E E	RD3		Read the previously selected RAM status character 3 into accumulator.

REGISTER PAIR PX LOOKUP TABLE

	PX 0 RRR 0		PX 1 RRR 1	
PX	FIM	FIN	SRC	JIN
P0	20	30	21	31
P1	22	32	23	33
P2	24	34	25	35
P3	26	36	27	37
P4	28	38	29	39
P5	2A	3A	2B	3B
P6	2C	3C	2D	3D
P7	2E	3E	2F	3F

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ACCUMULATOR INSTRUCTIONS

HEX CODING	MNEMONIC OPR	MNEMONIC OPA	DESCRIPTION OF OPERATION
F 0	CLB		Clear both. (Accumulator and carry.)
F 1	CLC		Clear carry.
F 2	IAC		Increment accumulator.
F 3	CMC		Complement carry.
F 4	CMA		Complement accumulator.
F 5	RAL		Rotate left. (Accumulator and carry.)
F 6	RAR		Rotate Right. (Accumulator and carry.)
F 7	TCC		Transmit carry to accumulator and clear carry.
F 8	DAC		Decrement accumulator.
F 9	TCS		Transfer carry subtract and clear carry.
F A	STC		Set carry.
F B	DAA		Decimal adjust accumulator.
F C	KBP		Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
F D	DCL		Designate command line.
F E			
F F			

JCN HEX	C_x MNEMONIC	C_8	C_4	C_2	C_1	
						Invert Jump Condition
						Jump if Accumulator = 0
						Jump if Carry Bit = 1
						Jump if Test Input = 0 (High)
10		0	0	0	0	NO OPERATION
11	TO	0	0	0	1	Jump if test = 0 (High)
12	C1	0	0	1	0	Jump if CY = 1
13	TO+C1	0	0	1	1	Jump if test = 0 or CY = 1
14	AO	0	1	0	0	Jump if AC = 0
15	TO+AO	0	1	0	1	Jump if test = 0 or AC = 0
16	C1+AO	0	1	1	0	Jump if CY = 1 or AC = 0
17	TO+C1+AO	0	1	1	1	Jump if test = 0 or CY = 1 or AC = 0
18		1	0	0	0	Jump Unconditionally
19	T1	1	0	0	1	Jump if test = 1 (Low)
1A	CO	1	0	1	0	Jump if CY = 0
1B	T1CO	1	0	1	1	Jump if test = 1 and CY = 0
1C	A1	1	1	0	0	Jump if AC $\neq$ 0
1D	T1A1	1	1	0	1	Jump if test = 1 and AC $\neq$ 0
1E	COA1	1	1	1	0	Jump if CY = 0 and AC $\neq$ 0
1F	T1COA1	1	1	1	1	Jump if test = 1 and CY = 0 and AC $\neq$ 0

OPC	MNEMO	DESCRIPTION	OPERATION	NB	ZB	C4	C8	N	Z	V	C	MICRO-CYCLES
0 (Ø)	JMP	JUMP	LC←MIØ-11	–	–	–	–	–	–	–	–	2
0 (1)	RFS	RETURN FROM SUBROUTINE	LC←RR	–	–	–	–	–	–	–	–	2
1	JXX	CONDITIONAL JUMP	LC←MIØ-7	–	–	–	–	–	–	–	–	2
2	AL	ADD LITERAL	Ra←Ra+LIT	•	•	•	•	–	–	–	–	1
3	CL	COMPARE LITERAL	Ra-LIT	•	•	•	•	–	–	–	–	1
4	NL	AND LITERAL	Ra←Ra∧LIT	•	•	–	–	–	–	–	–	1
5	TL	TEST LITERAL	Ra∧LIT	•	•	–	–	–	–	–	–	1
6	LL	LOAD LITERAL	Ra←LIT	•	•	–	–	–	–	–	–	1
70	RI	RESET INTERRUPTS		–	–	–	–	–	–	–	–	1
71	SI	SET INTERRUPTS		–	–	–	–	–	–	–	–	1
72	CCF	COPY COND. FLAGS	Ra←FLAGS	–	–	–	–	–	–	–	–	1
73	LCF	LOAD COND. FLAGS	FLAGS$\overset{C}{\leftarrow}$Ra	–	–	–	–	–	–	–	–	1
74												
75	LGL	LOAD G LOW	G←(Ra)$_{0-2}$	–	–	–	–	–	–	–	–	1
76	CIB	CONDITIONALLY INCREMENT BYTE	Ra$\overset{08}{\leftarrow}$Ra+1	•	•	•	•	–	–	–	–	1
77	CDB	CONDITIONALLY DECREMENT BYTE	Ra$\overset{08}{\leftarrow}$Ra−1	•	•	•	•	–	–	–	–	1
80	MB	MOVE BYTE	Ra←Rb	•	•	–	–	•	•	0	–	1
82	MW	MOVE WORD	Ra←Rb	•	•	–	–	•	•	0	–	2
84	CMB	CONDITIONALLY MOVE BYTE	Ra$\overset{C}{\leftarrow}$Rb	(•	•	–	–	•	•	0	–)·0	1
86	CMW	CONDITIONALLY MOVE WORD	Ra$\overset{C}{\leftarrow}$Rb	(•	•	–	–	•	•	0	–)·0	2
88	SLBC	SHIFT LEFT BYTE WITH CARRY	Ra←2Rb+C	•	•	•	•	•	•	•	•	1
8A	SLWC	SHIFT LEFT WORD WITH CARRY	Ra←2Rb+C	•	•	•	•	•	•	•	•	2
8C	SLB	SHIFT LEFT BYTE	Ra←2Rb	•	•	•	•	•	•	•	•	1
8E	SLW	SHIFT LEFT WORD	Ra←2Rb	•	•	•	•	•	•	•	•	2
90	ICB1	INCREMENT BYTE BY 1	Ra←Rb+1	•	•	•	•	•	•	•	•	1
92	ICW1	INCREMENT WORD BY 1	Ra←Rb+1	•	•	•	•	•	•	•	•	2
94	ICB2	INCREMENT BYTE BY 2	Ra←Rb+2	•	•	•	•	•	•	•	•	1
96	ICW2	INCREMENT WORD BY 2	Ra←Rb+2	•	•	•	•	•	•	•	•	2
98	TCB	TWOS COMPLEMENT BYTE	Ra← −Rb	•	•	•	•	•	•	•	•	1
9A	TCW	TWOS COMPLEMENT WORD	Ra← −Rb	•	•	•	•	•	•	•	•	2
9C	OCB	ONES COMPLEMENT BYTE	Ra←~Rb	•	•	0	0	•	•	0	1	1
9E	OCW	ONES COMPLEMENT WORD	Ra←~Rb	•	•	0	0	•	•	0	1	2
AØ	AB	ADD BYTE	Ra←Ra+Rb	•	•	•	•	•	•	•	•	1
A2	AW	ADD WORD	Ra←Ra+Rb	•	•	•	•	•	•	•	•	2
A4	CAB	CONDITIONALLY ADD BYTE	Ra$\overset{C}{\leftarrow}$Ra+Rb	(•	•	•	•	•	•	•	•)·0	1
A6	CAW	CONDITIONALLY ADD WORD	Ra$\overset{C}{\leftarrow}$Ra+Rb	(•	•	•	•	•	•	•	•)·0	2
A8	ABC	ADD BYTE WITH CARRY	Ra←Ra+Rb+C	•	•	•	•	•	•	•	•	1
AA	AWC	ADD WORD WITH CARRY	Ra←Ra+Rb+C	•	•	•	•	•	•	•	•	2
AC	CAD	CONDITIONALLY ADD DIGITS	(Ra$\overset{C4}{\leftarrow}$Ra+Rb)$_{0-3}$	•	•	•	•	•	•	•	•	1
AE	CAWI	CONDITIONALLY ADD WORD ON ICS	Ra$\overset{ICS}{\leftarrow}$Ra+Rb	(•	•	•	•	•	•	•	•)·0	2
BØ	SB	SUBTRACT BYTE	Ra←Ra−Rb	•	•	•	•	•	•	•	•	1
B2	SW	SUBTRACT WORD	Ra←Ra−Rb	•	•	•	•	•	•	•	•	2
B4	CB	COMPARE BYTE	Ra−Rb	•	•	•	•	•	•	•	•	1
B6	CW	COMPARE WORD	Ra−Rb	•	•	•	•	•	•	•	•	2
B8	SBC	SUBTRACT BYTE WITH CARRY	Ra←Ra−Rb−C	•	•	•	•	•	•	•	•	1
BA	SWC	SUBTRACT WORD WITH CARRY	Ra←Ra−Rb−C	•	•	•	•	•	•	•	•	2
BC	DB1	DECREMENT BYTE BY 1	Ra←Rb−1	•	•	•	•	•	•	•	•	1
BE	DW1	DECREMENT WORD BY 1	Ra←Rb−1	•	•	•	•	•	•	•	•	2
CØ	NB	AND BYTE	Ra←Ra∧Rb	•	•	–	–	•	•	0	–	1
C2	NW	AND WORD	Ra←Ra∧Rb	•	•	–	–	•	•	0	–	2
C4	TB	TEST BYTE	Ra∧Rb	•	•	–	–	•	•	0	–	1
C6	TW	TEST WORD	Ra∧Rb	•	•	–	–	•	•	0	–	2
C8	ORB	OR BYTE	Ra←Ra∨Rb	•	•	–	–	•	•	0	–	1
CA	ORW	OR WORD	Ra←Ra∨Rb	•	•	–	–	•	•	0	–	2
CC	XB	EXCLUSIVE-OR BYTE	Ra←Ra∨Rb	•	•	–	–	•	•	0	–	1
CE	XW	EXCLUSIVE-OR WORD	Ra←Ra∨Rb	•	•	–	–	•	•	0	–	2
DØ	NCB	AND COMPLEMENT BYTE	Ra←Ra∧~Rb	•	•	–	–	•	•	0	–	1
D2	NCW	AND COMPLEMENT WORD	Ra←Ra∧~Rb	•	•	–	–	•	•	0	–	2
D8	SRBC	SHIFT RIGHT BYTE WITH CARRY	Ra←C Rb/2	•	•	0	•	•	•	0	•	1
DA	SRWC	SHIFT RIGHT WORD WITH CARRY	Ra←C Rb/2	•	•	0	•	•	•	0	•	2
DC	SRB	SHIFT RIGHT BYTE	Ra←Rb/2	•	•	0	•	•	•	0	•	1
DE	SRW	SHIFT RIGHT WORD	Ra←Rb/2	•	•	0	•	•	•	0	•	2
EØ	IB	INPUT BYTE		•	•	–	–	•	•	0	–	1
E2	IW	INPUT WORD		•	•	–	–	•	•	0	–	2
E4	ISB	INPUT STATUS BYTE		•	•	–	–	•	•	0	–	1
E6	ISW	INPUT STATUS WORD		•	•	–	–	•	•	0	–	2
EC	MI	MODIFY INSTRUCTION	MIB V Rb Ra	–	–	–	–	–	–	–	–	1
EE	LTR	LOAD TRANSLATION REGISTER	TR←Rb Ra	–	–	–	–	–	–	–	–	2
FØ	RIB1	READ AND INCREMENT BYTE BY 1	M←Rb Ra Ra←Ra+1	•	•	•	•	–	–	–	–	1
F1	WIB1	WRITE AND INCREMENT BYTE BY 1	M←Rb Ra Ra←Ra+1	•	•	•	•	–	–	–	–	1
F2	RIW1	READ AND INCREMENT WORD BY 1	M←Rb Ra Ra←Ra+1	•	•	•	•	–	–	–	–	2
F3	WIW1	WRITE AND INCREMENT WORD BY 1	M←Rb Ra Ra←Ra+1	•	•	•	•	–	–	–	–	2
F4	RIB2	READ AND INCREMENT BYTE BY 2	M←Rb Ra Ra←Ra+2	•	•	•	•	–	–	–	–	1
F5	WIB2	WRITE AND INCREMENT BYTE BY 2	M←Rb Ra Ra←Ra+2	•	•	•	•	–	–	–	–	1
F6	RIW2	READ AND INCREMENT WORD BY 2	M←Rb Ra Ra←Ra+2	•	•	•	•	–	–	–	–	2
F7	WIW2	WRITE AND INCREMENT WORD BY 2	M←Rb Ra Ra←Ra+2	•	•	•	•	–	–	–	–	2
F8	R	READ	M←Rb Ra	–	–	–	–	–	–	–	–	1
F9	W	WRITE	M←Rb Ra	–	–	–	–	–	–	–	–	1
FA	RA	READ ACKNOWLEDGE	M←Rb Ra	–	–	–	–	–	–	–	–	1
FB	WA	WRITE ACKNOWLEDGE	M←Rb Ra	–	–	–	–	–	–	–	–	1
FC	OB	OUTPUT BYTE	M←Rb Ra	–	–	–	–	–	–	–	–	1
FD	OW	OUTPUT WORD	M←Rb Ra	–	–	–	–	–	–	–	–	1
FE	OS	OUTPUT STATUS	M←Rb Ra	–	–	–	–	–	–	–	–	1
FF	NOP	NO-OPERATION	– –	–	–	–	–	–	–	–	–	1

NOTES
- • = Conditionally set/cleared.
- – = Not affected.
- 0 = Cleared.
- 1 = Set.
- ( ) C = The contents of the parentheses is conditioned on C flag.

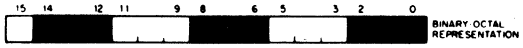
INSTRUCTION SET

Mnemonic	Time States	# Bytes	Instruction Codes			Condition Bits CZSP	Description
Lr1r2	5	1	11	DDD	SSS	****	r1←r2
LrM	8	1	11	DDD	111	****	r←M
LMr	7	1	11	111	SSS	****	M←r
Lri	8	2	00	DDD	110	****	r←<B2>
LMI	9	2	00	111	110	****	M←<B2>
INr	5	1	00	DDD	000	*YYY	r←r+1 r≠A,M
DCr	5	1	00	DDD	001	*YYY	r←r−1 r≠A,M
ADr	5	1	10	000	SSS	YYYY	A←A+r
ADM	8	1	10	000	111	YYYY	A←A+M
ADI	8	2	00	000	100	YYYY	A←A+<B2>
ACr	5	1	10	001	SSS	YYYY	A←A+r+C
ACM	8	1	10	001	111	YYYY	A←A+M+C
ACI	8	2	00	001	100	YYYY	A←A+<B2>+C
SUr	5	1	10	010	SSS	YYYY	A←A−r
SUM	8	1	10	010	111	YYYY	A←A−M
SUI	8	2	00	010	100	YYYY	A←A−<B2>
SBr	5	1	10	011	SSS	YYYY	A←A−r−C
SBM	8	1	10	011	111	YYYY	A←A−M−C
SBI	8	2	00	011	100	YYYY	A←A−<B2>−C
NDr	5	1	10	100	SSS	0YYY	A←A AND r
NDM	8	1	10	100	111	0YYY	A←A AND M
NDI	8	2	00	100	100	0YYY	A←A AND <B2>
XRr	5	1	10	101	SSS	0YYY	A←A EXCLUSIVE OR r
XRM	8	1	10	101	111	0YYY	A←A EXCLUSIVE OR M
XRI	8	2	00	101	100	0YYY	A←A EXCLUSIVE OR <B2>
ORr	5	1	10	110	SSS	0YYY	A←A OR r
ORM	8	1	10	110	111	0YYY	A←A OR M
ORI	8	2	00	110	100	0YYY	A←A OR <B2>
CPr	5	1	10	111	SSS	YYYY	A-r } Set condition bits
CPM	8	1	10	111	111	YYYY	A-M } Z=1 if A=r, M, <B2>
CPI	8	2	00	111	100	YYYY	A-<B2> } C=1 if A<r, M, <B2>
RLC	5	1	00	000	010	Y***	A(m+1)←A(m), A(0)← A(7), C←A(7)
RRC	5	1	00	001	010	Y***	A(m)←A(m+1), A(7)← (0), C←A(0),
RAL	5	1	00	010	010	Y***	A(m+1)←A(m), C←A(7), A(0)←C
RAR	5	1	00	011	010	Y***	A(m)←A(m+1), C←A(0), A(7)←C
JMP	11	3	01	XXX	100	****	P←<B3> <B2>
JFc	9/11	3	01	0C$_4$C$_3$	000	****	P←<B3> <B2>, If Flag c clear else P←P+3
JTc	9/11	3	01	1C$_4$C$_3$	000	****	P←<B3> <B2>, If Flag c set, else P←P+3
CAL	11	3	01	XXX	110	****	STACK←P+3, P←<B3> <B2>
CFc	9/11	3	01	0C$_4$C$_3$	000	****	STACK←P,P←<B3><B2>, If Flag c clear, else P←P+3
CTc	9/11	3	01	1C$_4$C$_3$	010	****	STACK←P,P←<B3><B2>, If Flag c set, else P←P+3
RET	5	1	00	XXX	111	****	P←STACK
RFc	3/5	1	00	0C$_4$C$_3$	011	****	P←STACK, If Flag c clear, else P←P+1
RTc	3/5	1	00	1C$_4$C$_3$	011	****	P←STACK, If Flag c set, else P←P+1
RST	5	1	00	AAA	101	****	STACK←P, P←AAA000
INP	8	1	01	00M	MM1	****	A←Contents of Port MMM
OUT	6	1	01	RRM	MM1	****	Port RRMMM←ARR≠00
HLT	4	1	00	000	00X	****	Enter Stopped State
HLT	4	1	11	111	111	****	Enter Stopped State

DEFINITIONS

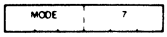
r	Index Register A,B,C,D,E,H,L
M	Memory location pointed to by H, L
c	Condition flags C,Z,S,P
C$_4$C$_3$ = 00	— C(carry) 10 — S(sign)
	01 — Z(zero) 11 — P(parity)
<B2>	Byte 2 of a multibyte instruction
<B3>	Byte 3 of a multibyte instruction
A(m)	Bit m of the A Register
P	Program Counter
XXX	Don't care
STACK	Pushdown register for P storage
SSS	Source Register
DDD	Destination Register
←	Is replaced by
*	Remains the same
Y	Can change

WORD FORMAT



Mode	Name	Symbolic	Description
0	register	R	(R) is operand [ex. R2=%2]
1	register deferred	(R)	(R) is address
2	auto-increment	(R)+	(R) is adrs; (R) +(1 or 2)
3	auto-incr deferred	@(R)+	(R) is adrs of adrs; (R) + 2
4	auto-decrement	−(R)	(R) − (1 or 2); is adrs
5	auto-decr deferred	@−(R)	(R) − 2; (R) is adrs of adrs
6	index	X(R)	(R) + X is adrs
7	index deferred	@X(R)	(R) + X is adrs of adrs

PROGRAM COUNTER ADDRESSING Reg = 7



2	immediate	#n	operand n follows instr
3	absolute	@#A	address A follows instr
6	relative	A	instr adrs + 4 + X is adrs
7	relative deferred	@A	instr adrs + 4 + X is adrs of adrs

LEGEND

Op Codes

■	= 0 for word/1 for byte
SS	= source field (6 bits)
DD	= destination field (6 bits)
R	= gen register (3 bits), 0 to 7
XXX	= offset (8 bits), +127 to −128
N	= number (3 bits)
NN	= number (6 bits)

Operations

( )	= contents of
s	= contents of source
d	= contents of destination
r	= contents of register
←	= becomes
X	= relative address
%	= register definition

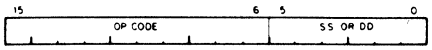
Boolean

∧	= AND
∨	= inclusive OR
∀	= exclusive OR
~	= NOT

Condition Codes

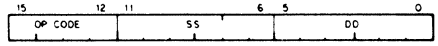
*	= conditionally set/cleared
—	= not affected
0	= cleared
1	= set

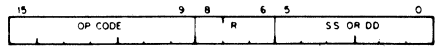
SINGLE OPERAND: OPR dst



Mnemonic	Op Code	Instruction	dst Result	N	Z	V	C
General							
CLR(B)	■ 050DD	clear	0	0	1	0	0
COM(B)	■ 051DD	complement (1's)	~d	*	*	0	1
INC(B)	■ 052DD	increment	d + 1	*	*	*	–
DEC(B)	■ 053DD	decrement	d − 1	*	*	*	–
NEG(B)	■ 054DD	negate (2's compl)	−d	*	*	*	*
TST(B)	■ 057DD	test	d	*	*	0	0
Rotate & Shift							
ROR(B)	■ 060DD	rotate right	→ C, d	*	*	*	*
ROL(B)	■ 061DD	rotate left	C, d ←	*	*	*	*
ASR(B)	■ 062DD	arith shift right	d/2	*	*	*	*
ASL(B)	■ 063DD	arith shift left	2d	*	*	*	*
SWAB	0003DD	swap bytes		*	*	0	0
Multiple Precision							
ADC(B)	■ 055DD	add carry	d + C	*	*	*	*
SBC(B)	■ 056DD	subtract carry	d − C	*	*	*	*
SXT	0067DD	sign extend	0 or −1	–	*	0	–
Processor Status (PS) Operators							
MFPS	1067DD	move byte from PS	d ← PS	*	*	0	–
MTPS	1064SS	move byte to PS	PS ← s	*	*	*	*

DOUBLE OPERAND: OPR src, dst OPR src, R or OPR R, dst





Mnemonic	Op Code	Instruction	Operation	N	Z	V	C
General							
MOV(B)	■ 1SSDD	move	d ← s	*	*	0	–
CMP(B)	■ 2SSDD	compare	s − d	*	*	*	*
ADD	06SSDD	add	d ← s + d	*	*	*	*
SUB	16SSDD	subtract	d ← d − s	*	*	*	*
Logical							
BIT(B)	■ 3SSDD	bit test (AND)	s ∧ d	*	*	0	–
BIC(B)	■ 4SSDD	bit clear	d ← (~s) ∧ d	*	*	0	–
BIS(B)	■ 5SSDD	bit set (OR)	d ← s ∨ d	*	*	0	–
XOR	074RDD	exclusive OR	d ← r ∨ d	*	*	0	–

Cont'd on next page

IS17 Cont'd

Optional EIS

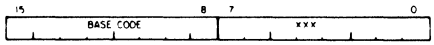
MUL	070RSS	multiply	r ← r x s	•	•	0	•
DIV	071RSS	divide	r ← r/s	•	•	•	•
ASH	072RSS	shift arithmetically		•	•	•	•
ASHC	073RSS	arith shift combined		•	•	•	•

Optional FIS

FADD	07500R	floating add	•	•	0	0
FSUB	07501R	floating subtract	•	•	0	0
FMUL	07502R	floating multiply	•	•	0	0
FDIV	07503R	floating divide	•	•	0	0

BRANCH: B - - location

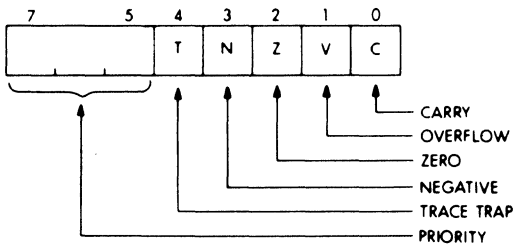
If condition is satisfied:
Branch to location,
New PC ← Updated PC + (2 x offset)
adrs of br instr + 2



Op Code = Base Code + XXX

Mnemonic	Base Code	Instruction	Branch Condition	
Branches				
BR	000400	branch (unconditional)	(always)	
BNE	001000	br if not equal (to 0)	≠ 0	Z = 0
BEQ	001400	br if equal (to 0)	= 0	Z = 1
BPL	100000	branch if plus	+	N = 0
BMI	100400	branch if minus	−	N = 1
BVC	102000	br if overflow is clear		V = 0
BVS	102400	br if overflow is set		V = 1
BCC	103000	br if carry is clear		C = 0
BCS	103400	br if carry is set		C = 1
Signed Conditional Branches				
BGE	002000	br if greater or equal (to 0)	≥0	N ⊻ V = 0
BLT	002400	br if less than (0)	<0	N ⊻ V = 1
BGT	003000	br if greater than (0)	>0	Z v (N ⊻ V) = 0
BLE	003400	br if less or equal (to 0)	≤0	Z v (N ⊻ V) = 1
Unsigned Conditional Branches				
BHI	101000	branch if higher	>	C v Z = 0
BLOS	101400	branch if lower or same	≤	C v Z = 1
BHIS	103000	branch if higher or same	≥	C = 0
BLO	103400	branch if lower	<	C = 1

PROCESSOR STATUS WORD



IS17 Cont'd

JUMP & SUBROUTINE

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	jump	PC ← dst
JSR	004RDD	jump to subroutine	use same R
RTS	00020R	return from subroutine	use same R
MARK	0064NN	mark	aid in subr return
SOB	077RNN	subtract 1 & br (if ≠ 0)	(R) − 1, then if (R) ≠ 0: PC ← Updated PC − (2 x NN)

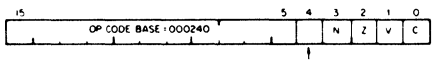
TRAP & INTERRUPT:

Mnemonic	Op Code	Instruction	Notes
EMT	104000 to 104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400 to 104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
RTT	000006	return from interrupt	inhibit T bit trap

MISCELLANEOUS:

Mnemonic	Op Code	Instruction
HALT	000000	halt
WAIT	000001	wait for interrupt
RESET	000005	reset external bus
NOP	000240	(no operation)

CONDITION CODE OPERATORS:



0 = CLEAR SELECTED COND. CODE BITS
1 = SET SELECTED COND. CODE BITS

Mnemonic	Op Code	Instruction	N	Z	V	C
CLC	000241	clear C	-	-	-	0
CLV	000242	clear V	-	-	0	-
CLZ	000244	clear Z	-	0	-	-
CLN	000250	clear N	0	-	-	-
CCC	000257	clear all cc bits	0	0	0	0
SEC	000261	set C	-	-	-	1
SEV	000262	set V	-	-	1	-
SEZ	000264	set Z	-	1	-	-
SEN	000270	set N	1	-	-	-
SCC	000277	set all cc bits	1	1	1	1

NUMERICAL OP CODE LIST

OP Code	Mnemonic
00 00 00	HALT
00 00 01	WAIT
00 00 02	RTI
00 00 03	BPT
00 00 04	IOT
00 00 05	RESET
00 00 06	RTT
00 00 07 – 00 00 77	(unused)
00 01 DD	JMP
00 02 0R	RTS
00 02 10 – 00 02 27	(reserved)
00 02 40	NOP
00 02 41 – 00 02 77	cond codes
00 03 DD	SWAB
00 04 XXX	BR
00 10 XXX	BNE
00 14 XXX	BEQ
00 20 XXX	BGE
00 24 XXX	BLT
00 30 XXX	BGT
00 34 XXX	BLE
00 4R DD	JSR
00 50 DD	CLR
00 51 DD	COM
00 52 DD	INC
00 53 DD	DEC
00 54 DD	NEG
00 55 DD	ADC
00 56 DD	SBC
00 57 DD	TST

OP Code	Mnemonic
00 60 DD	ROR
00 61 DD	ROL
00 62 DD	ASR
00 63 DD	ASL
00 64 NN	MARK
00 67 DD	SXT
00 70 00 – 00 77 77	(unused)
01 SS DD	MOV
02 SS DD	CMP
03 SS DD	BIT
04 SS DD	BIC
05 SS DD	BIS
06 SS DD	ADD
07 0R SS	MUL
07 1R SS	DIV
07 2R SS	ASH
07 3R SS	ASHC
07 4R DD	XOR
07 50 0R	FADD
07 50 1R	FSUB
07 50 2R	FMUL
07 50 3R	FDIV
07 50 40 – 07 67 77	(unused)
07 7R NN	SOB
10 00 XXX	BPL
10 04 XXX	BMI
10 10 XXX	BHI
10 14 XXX	BLOS
10 20 XXX	BVC
10 24 XXX	BVS
10 30 XXX	BCC, BHIS
10 34 XXX	BCS, BLO

OP Code	Mnemonic
10 40 00 – 10 43 77	EMT
10 44 00 – 10 47 77	TRAP
10 50 DD	CLRB
10 51 DD	COMB
10 52 DD	INCB
10 53 DD	DECB
10 54 DD	NEGB
10 55 DD	ADCB
10 56 DD	SBCB
10 57 DD	TSTB
10 60 DD	RORB
10 61 DD	ROLB
10 62 DD	ASRB
10 63 DD	ASLB
10 64 SS	MTPS
10 67 DD	MFPS
11 SS DD	MOVB
12 SS DD	CMPB
13 SS DD	BITB
14 SS DD	BICB
15 SS DD	BISB
16 SS DD	SUB

INSTRUCTIONS IN THE 32 x 9 ROM – POSITIVE LOGIC (1 = H ≈ 3 V) INTERPRETATION

ROM WORD							ALU Instruction (See Pg. 10 for Symbology)	ALU OUTPUT		TYPICAL USES	
I_7	I_6	I_5	I_4	I_3	Decimal	Octal		No Carry In (C_N = L)	With Carry In (C_N = H)		
L	L	L	L	L	0	00	LLLL + HHHH + C_N	Force 1111	Force 0000	Initialization (Force 1's or 0's)	
L	L	L	L	H	1	01	AND A_I & B_j	$A_I \wedge B_j$	$A_I \wedge B_j$	AND	A_I & B_j
L	L	L	H	L	2	02	AND D_I & B_j	$D_I \wedge B_j$	$D_I \wedge B_j$	"	D_I & B_j
L	L	L	H	H	3	03	OR A_I & B_j	$A_I \vee B_j$	$A_I \vee B_j$	OR	A_I & B_j
L	L	H	L	L	4	04	OR D_I & B_j	$D_I \vee B_j$	$D_I \vee B_j$	"	D_I & B_j
L	L	H	L	H	5	05	Exclusive OR A_I & B_j	$A_I \veebar B_j$	$A_I \veebar B_j$	Exclusive Or	A_I & B_j
L	L	H	H	L	6	06	Exclusive OR D_I & B_j	$D_I \veebar B_j$	$D_I \veebar B_j$	"	D_I & B_j
L	L	H	H	H	7	07	$\overline{A_I}$ + HHHH + C_N	$\overline{A_I}$ + 1111	$\overline{A_I}$	Invert	A_I
L	H	L	L	L	8	10	$\overline{D_I}$ + HHHH + C_N	$\overline{D_I}$ + 1111	$\overline{D_I}$	"	D_I
L	H	L	L	H	9	11	$\overline{B_j}$ + HHHH + C_N	$\overline{B_j}$ + 1111	$\overline{B_j}$	"	B_j
L	H	L	H	L	10	12	$\overline{Q}$ + HHHH + C_N	$\overline{Q}$ + 1111	$\overline{Q}$	"	Q
L	H	L	H	H	11	13	$\overline{A_I}$ + LLLL + C_N	$\overline{A_I}$	$\overline{A_I}$ + 0001	2's Complement Of	A_I
L	H	H	L	L	12	14	$\overline{D_I}$ + LLLL + C_N	$\overline{D_I}$	$\overline{D_I}$ + 0001	"	D_I
L	H	H	L	H	13	15	$\overline{B_j}$ + LLLL + C_N	$\overline{B_j}$	$\overline{B_j}$ + 0001	"	B_j
L	H	H	H	L	14	16	$\overline{Q}$ + LLLL + C_N	$\overline{Q}$	$\overline{Q}$ + 0001	"	Q
L	H	H	H	H	15	17	A_I + LLLL + C_N	A_I	A_I + 0001	Transfer Or Increment	A_I
H	L	L	L	L	16	20	D_I + LLLL + C_N	D_I	D_I + 0001	"	D_I
H	L	L	L	H	17	21	B_j + LLLL + C_N	B_j	B_j + 0001	"	B_j
H	L	L	H	L	18	22	Q + LLLL + C_N	Q	Q + 0001	"	Q
H	L	L	H	H	19	23	A_I + HHHH + C_N	A_I + 1111	A_I	Decrement Or Transfer	A_I
H	L	H	L	L	20	24	D_I + HHHH + C_N	D_I + 1111	D_I	"	D_I
H	L	H	L	H	21	25	B_j + HHHH + C_N	B_j + 1111	B_j	"	B_j
H	L	H	H	L	22	26	Q + HHHH + C_N	Q + 1111	Q	"	Q
H	L	H	H	H	23	27	A_I + B_j + C_N	A_I + B_j	A_I + B_j + 0001	Add	A_I & B_j
H	H	L	L	L	24	30	D_I + B_j + C_N	D_I + B_j	D_I + B_j + 0001	"	D_I & B_j
H	H	L	L	H	25	31	A_I + Q + C_N	A_I + Q	A_I + Q + 0001	"	A_I & Q
H	H	L	H	L	26	32	D_I + Q + C_N	D_I + Q	D_I + Q + 0001	"	D_I & Q
H	H	L	H	H	27	33	A_I + $\overline{B_j}$ + C_N	A_I - B_j - 0001	A_I - B_j	Subtract	A_I & B_j
H	H	H	L	L	28	34	B_j + $\overline{A_I}$ + C_N	B_j - A_I - 0001	B_j - A_I	"	B_j & A_I
H	H	H	L	H	29	35	D_I + $\overline{B_j}$ + C_N	D_I - B_j - 0001	D_I - B_j	"	D_I & B_j
H	H	H	H	L	30	36	B_j + $\overline{D_I}$ + C_N	B_j - D_I - 0001	B_j - D_I	"	B_j & D_I
H	H	H	H	H	31	37	D_I + $\overline{Q}$ + C_N	D_I - Q - 0001	D_I - Q	"	D_I & Q

INSTRUCTION MODIFIERS IN THE 8 x 8 ROM – POSITIVE LOGIC (1 = H ≈ 3 V) INTERPRETATION

Rom Word			Rom Word	Load Control		Shift Control			Data Out Control		
I_2	I_1	I_0	Decimal	Load Ram B_j	Load Q	Shift Left	Shift Right	Don't Shift	A Latch	B Latch	ALU Output F
L	L	L	0	X				X			X
L	L	H	1	X				X	X		
L	H	L	2	X				X		X	
L	H	H	3	X		X					X
H	L	L	4	X			X				X
H	L	H	5	X	X	X					X
H	H	L	6	X	X		X				X
H	H	H	7		X			X			X

INSTRUCTIONS LOCATED IN THE ON CHIP ROMS

SYMBOL DEFINITIONS

A_I = Any of the 16 four bit registers in the multiport RAM (I = 0 to 15)

B_J = " " (J = 0 to 15)

$A_I + B_J$ = A_I plus B_J (arithmetic addition)

$A_I \veebar B_J$ = A_I exclusive OR'ed with B_J

$A_I \vee B_J$ = A_I or B_J (logic inclusive or)

$A_I \wedge B_J$ = A_I and B_J (logic and)

$\overline{A_I}$ = The complement of A_I

$A_I \longrightarrow Q$ = Transfer A_I to Q, A_I saved, Old Q is lost

$A_I \longrightarrow$ OUT = Transfer A_I to the output pins, A_I is saved

$\overrightarrow{A_I}$ = A_I shifted right one bit

$\overleftarrow{A_I}$ = A_I shifted left one bit

$B_J - A_I$ = B_J minus A_I = $B_J + \overline{A_I} + C_N = B_J$ + 2's compl of A_I

ACCUMULATOR GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD CARRY	LNK		ACC←(ACC) + CRY	19	1	1	1/0	1/0	1/0	1/0
ADD IMMEDIATE	AI	ii	ACC←(ACC) + H'ii'	24ii	2	2 5	1/0	1/0	1/0	1/0
AND IMMEDIATE	NI	ii	ACC←(ACC) ∧ H'ii'	21ii	2	2 5	0	1/0	0	1/0
CLEAR	CLR		ACC←H'00'	70	1	1				
COMPARE IMMEDIATE	CI	ii	H'ii' + $\overline{(ACC)}$ + 1	25ii	2	2 5	1/0	1/0	1/0	1/0
COMPLEMENT	COM		ACC←(ACC) ⊕ H'FF'	18	1	1	0	1/0	0	1/0
EXCLUSIVE-OR IMMEDIATE	XI	ii	ACC←(ACC) ⊕ H'ii'	23ii	2	2 5	0	1/0	0	1/0
INCREMENT	INC		ACC←(ACC) + 1	1F	1	1	1/0	1/0	1/0	1/0
LOAD IMMEDIATE	LI	ii	ACC←H'ii'	20ii	2	2 5				
LOAD IMMEDIATE SHORT	LIS	i	ACC←H'0i'	7i	1	1				
OR IMMEDIATE	OI	ii	ACC←(ACC) ∨ H'ii'	22ii	2	2 5	0	1/0	0	1/0
SHIFT LEFT ONE	SL	1	SHIFT LEFT 1	13	1	1	0	1/0	0	1/0
SHIFT LEFT FOUR	SL	4	SHIFT LEFT 4	15	1	1	0	1/0	0	1/0
SHIFT RIGHT ONE	SR	1	SHIFT RIGHT 1	12	1	1	0	1/0	0	1
SHIFT RIGHT FOUR	SR	4	SHIFT RIGHT 4	14	1	1	0	1 0	0	1

BRANCH INSTRUCTIONS

In all conditional branches $PC_0 \leftarrow (PC_0) + 2$ if the test condition is not met. Execution is complete in 3 0 cycles

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
BRANCH ON CARRY	BC	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if CRY 1	82aa	2	3 5				
BRANCH ON POSITIVE	BP	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if SIGN 1	81aa	2	3 5				
BRANCH ON ZERO	BZ	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ZERO 1	84aa	2	3 5				
BRANCH ON TRUE	BT	taa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if any test is true	81aa	2	3 5				
			t TEST CONDITION: 2^2 ZERO, 2^1 CRY, 2^0 SIGN							
BRANCH IF NEGATIVE	BM	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if SIGN 0	91aa	2	3 5				
BRANCH IF NO CARRY	BNC	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if CARRY 0	92aa	2	3 5				
BRANCH IF NO OVERFLOW	BNO	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if OVF 0	98aa	2	3 5				
BRANCH IF NOT ZERO	BNZ	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ZERO 0	94aa	2	3 5				
BRANCH IF FALSE TEST	BF	taa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if all false test bits	9taa	2	3 5				
			t TEST CONDITION: 2^3 OVF, 2^2 ZERO, 2^1 CRY, 2^0 SIGN							
BRANCH IF ISAR (LOWER) ≠ 7	BR7	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ISARL ≠ 7 $PC_0 \leftarrow (PC_0) + 2$ if ISARL 7	8Faa	2	2 5 2 0				
BRANCH RELATIVE	BR	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$	90aa	2	3 5				
JUMP*	JMP	aaaa	$PC_0 \leftarrow H'aaaa'$	29aaaa	3	5 5	*Privileged instruction			

MEMORY REFERENCE INSTRUCTIONS

In all Memory Reference Instructions, the Data Counter is incremented DC←DC + 1

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD BINARY	AM		ACC←(ACC) + [(DC)]	88	1	2 5	1/0	1/0	1/0	1/0
ADD DECIMAL	AMD		ACC←(ACC) + [(DC)]	89	1	2 5	1/0	1/0	1/0	1/0
AND	NM		ACC←(ACC) ∧ [(DC)]	8A	1	2 5	0	1/0	0	1/0
COMPARE	CM		[(DC)] + $\overline{(ACC)}$ + 1	8D	1	2 5	1/0	1/0	1/0	1/0
EXCLUSIVE OR	XM		ACC←(ACC) ⊕ [(DC)]	8C	1	2 5	0	1/0	0	1/0
LOAD	LM		ACC←[(DC)]	16	1	2 5				
LOGICAL OR	OM		ACC←(ACC) ∨ [(DC)]	8B	1	2 5	0	1/0	0	1/0
STORE	ST		(DC)←(ACC)	17	1	2 5				

ADDRESS REGISTER GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD to DATA COUNTER	ADC		DC←(DC) + (ACC)	8E	1	2 5				
CALL to SUBROUTINE*	PK		$PC_0U \leftarrow (r12)$, $PC_0L \leftarrow (r13)$, $PC_1 \leftarrow (PC_0)$	0C	1	4				
CALL to SUBROUTINE IMMEDIATE*	PI	aaaa	$PC_1 \leftarrow (PC_0)$, $PC_0 \leftarrow H'aaaa'$	28aaaa	3	6 5				
EXCHANGE DC	XDC		$DC_0 \rightleftarrows DC_1$	2C	1	2				
LOAD DATA COUNTER	LR	DC,Q	DCU←(r14), DCL←(r15)	0F	1	4				
LOAD DATA COUNTER	LR	DC,H	DCU←(r10), DCL←(r11)	10	1	4				
LOAD DC IMMEDIATE	DCI	aaaa	DC←H'aaaa'	2Aaaaa	3	6				
LOAD PROGRAM COUNTER	LR	PO,Q	$PC_0U \leftarrow (r14)$, $PC_0L \leftarrow (r15)$	0D	1	4				
LOAD STACK REGISTER	LR	P,K	$PC_1U \leftarrow (r12)$, $PC_1L \leftarrow (r13)$	09	1	4				
RETURN FROM SUBROUTINE*	POP		$PC_0 \leftarrow (PC_1)$	1C	1	2				
STORE DATA COUNTER	LR	Q,DC	r14←(DCU), r15←(DCL)	0E	1	4				
STORE DATA COUNTER	LR	H,DC	r10←(DCU), r11←(DCL)	11	1	4				
STORE STACK REGISTER	LR	K,P	$r12 \leftarrow (PC_1U)$, $r13 \leftarrow (PC_1L)$	08	1	4				

Cont'd on next page

IS20 Cont'd

SCRATCHPAD REGISTER INSTRUCTIONS (Refer to Scratchpad Addressing Modes)

IS20 Cont'd

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD BINARY	AS	r	ACC←(ACC) + (r)	Cr	1	1	1/0	1/0	1/0	1/0
ADD DECIMAL	ASD	r	ACC←(ACC) + (r)	Dr	1	2	1/0	1/0	1/0	1/0
DECREMENT	DS	r	r←(r) + H'FF'	3r	1	1.5	1/0	1/0	1/0	1/0
LOAD	LR	A,r	ACC←(r)	4r	1	1				
LOAD	LR	A,KU	ACC←(r12)	00	1	1				
LOAD	LR	A,KL	ACC←(r13)	01	1	1				
LOAD	LR	A,QU	ACC←(r14)	02	1	1				
LOAD	LR	A,QL	ACC←(r15)	03	1	1				
LOAD	LR	r,A	r←(ACC)	5r	1	1				
LOAD	LR	KU,A	r12←(ACC)	04	1	1				
LOAD	LR	KL,A	r13←(ACC)	05	1	1				
LOAD	LR	QU,A	r14←(ACC)	06	1	1				
LOAD	LR	QL,A	r15←(ACC)	07	1	1				
AND	NS	r	ACC←(ACC) ∧ (r)	Fr	1	1	0	1/0	0	1/0
EXCLUSIVE OR	XS	r	ACC←(ACC) ⊕ (r)	Er	1	1	0	1/0	0	1/0

*Privileged instruction

MISCELLANEOUS INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
DISABLE INTERRUPT	DI		RESET ICB	1A	1	2				
ENABLE INTERRUPT*	EI		SET ICB	1B	1	2				
INPUT	IN	aa	ACC←(INPUT PORT aa)	26aa	2	4	0	1/0	0	1/0
INPUT SHORT	INS	a	ACC←(INPUT PORT a)	Aa	1	4***	0	1/0	0	1/0
LOAD ISAR	LR	IS,A	ISAR←(ACC)	0B	1	1				
LOAD ISAR LOWER	LISL	a	ISARL←a	1101a**	1	1				
LOAD ISAR UPPER	LISU	a	ISARU←a	01100a**	1	1				
LOAD STATUS REGISTER*	LR	W,J	W←(r9)	1D	1	2	1/0	1/0	1/0	1/0
NO OPERATION	NOP		PC_0←(PC_0) + 1	2B	1	1				
OUTPUT	OUT	aa	OUTPUT PORT aa←(ACC)	27aa	2	4				
OUTPUT SHORT	OUTS	a	OUTPUT PORT a←(ACC)	Ba	1	4***				
STORE ISAR	LR	A,IS	ACC←(ISAR)	0A	1	1				
STORE STATUS REG	LR	J,W	r9←(W)	1E	1	1				

*Privileged instruction
**3 bit octal digit
***2 machine cycles for CPU ports

NOTES

Each lower case character represents a Hexadecimal digit
Each cycle equals 4 machine clock periods
Lower case denotes variables specified by programmer

Function Definitions

←	is replaced by
( )	the contents of
(–)	Binary "1"s complement of
+	Arithmetic Add (Binary or Decimal)
⊕	Logical "OR" exclusive
∧	Logical "AND"
∨	Logical "OR" inclusive
H	Hexadecimal digit

Register Names

a	Address Variable
A	Accumulator
DC	Data Counter (Indirect Address Register)
DC_0	Data Counter #0 (Indirect Address Register #0)
DC_1	Data Counter #1 (Indirect Address Register #1)
DCL	Least significant 8 bits of Data Counter Addressed
DCU	Most significant 8 bits of Data Counter Addressed
H	Scratchpad Register #10 and #11
i and ii	immediate operand
ICB	Interrupt Control Bit
IS	Indirect Scratchpad Address Register
ISAR	Indirect Scratchpad Address Register
ISARL	Least Significant 3 bits of ISAR
ISARU	Most Significant 3 bits of ISAR
J	Scratchpad Register #9
K	Registers #12 and #13
KL	Register #13
KU	Register #12
PC_0	Program Counter
PC_0L	Least Significant 8 bits of Program Counter
PC_0U	Most Significant 8 bits of Program Counter
PC_1	Stack Register
PC_1L	Least Significant 8 bits of Program Counter
PC_1U	Most Significant 8 bits of Active Stack Register
Q	Registers #14 and #15
QL	Register #15
QU	Register #14
r	Scratchpad Register (any address thru 11)
W	Status Register

Scratchpad Addressing Modes (Machine Code Format)

r C	(Hexadecimal). Register Addressed by ISAR (Unmodified)
r D	(Hexadecimal). Register Addressed by ISAR, ISARL Incremented
r E	(Hexadecimal). Register Addressed by ISAR, ISARL Decremented
r F	(No operation performed)
r 0 thru B	(Hexadecimal). Register 0 thru 11 addressed directly from the Instruction

Status Register

–	No change in condition
1/0	is set to "1" or "0" depending on conditions
CRY	Carry Flag
OVF	Overflow Flag
SIGN	Sign of Result Flag
ZERO	Zero Flag

BASIC INSTRUCTION SET

The basic instruction set of the 4040 and 4004 (CPU) are shown below. The following section will describe each instruction in detail.

[Those instructions preceded by an asterisk (*) are 2 word instructions that occupy 2 successive locations in ROM]

MACHINE INSTRUCTIONS (Logic 1 = Low Voltage = Negative Voltage; Logic 0 = High Voltage = Ground)

MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
NOP	0 0 0 0	0 0 0 0	No operation.
*JCN	0 0 0 1 $A_2 A_2 A_2 A_2$	$C_1 C_2 C_3 C_4$ $A_1 A_1 A_1 A_1$	Jump to ROM address $A_2 A_2 A_2 A_2$, $A_1 A_1 A_1 A_1$ (within the same ROM that contains this JCN instruction) if condition $C_1 C_2 C_3 C_4$[1] is true, otherwise skip (go to the next instruction in sequence).
*FIM	0 0 1 0 $D_2 D_2 D_2 D_2$	R R R 0 $D_1 D_1 D_1 D_1$	Fetch immediate (direct) from ROM Data D_2, D_1 to index register pair location RRR.[2]
SRC	0 0 1 0	R R R 1	Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the Instruction Cycle.
FIN	0 0 1 1	R R R 0	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.
JIN	0 0 1 1	R R R 1	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the Instruction Cycle.
*JUN	0 1 0 0 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump unconditional to ROM address A_3, A_2, A_1.
*JMS	0 1 0 1 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump to subroutine ROM address A_3, A_2, A_1, save old address. (Up 1 level in stack.)
INC	0 1 1 0	R R R R	Increment contents of register RRRR.[3]
*ISZ	0 1 1 1 $A_2 A_2 A_2 A_2$	R R R R $A_1 A_1 A_1 A_1$	Increment contents of register RRRR. Go to ROM address A_2, A_1 (within the same ROM that contains this ISZ instruction) if result ≠0, otherwise skip (go to the next instruction in sequence).
ADD	1 0 0 0	R R R R	Add contents of register RRRR to accumulator with carry.
SUB	1 0 0 1	R R R R	Subtract contents of register RRRR to accumulator with borrow.
LD	1 0 1 0	R R R R	Load contents of register RRRR to accumulator.
XCH	1 0 1 1	R R R R	Exchange contents of index register RRRR and accumulator.
BBL	1 1 0 0	D D D D	Branch back (down 1 level in stack) and load data DDDD to accumulator.
LDM	1 1 0 1	D D D D	Load data DDDD to accumulator.

INPUT/OUTPUT AND RAM INSTRUCTIONS

(The RAM's and ROM's operated on in the I/O and RAM instructions have been previously selected by the last SRC instruction executed.)

MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
WRM	1 1 1 0	0 0 0 0	Write the contents of the accumulator into the previously selected RAM main memory character.
WMP	1 1 1 0	0 0 0 1	Write the contents of the accumulator into the previously selected RAM output port.
WRR	1 1 1 0	0 0 1 0	Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)
WPM	1 1 1 0	0 0 1 1	Write the contents of the accumulator into the previously selected half byte of read/write program memory (for use with 4008/4009 only)
WRϕ[4]	1 1 1 0	0 1 0 0	Write the contents of the accumulator into the previously selected RAM status character 0.
WR1[4]	1 1 1 0	0 1 0 1	Write the contents of the accumulator into the previously selected RAM status character 1.
WR2[4]	1 1 1 0	0 1 1 0	Write the contents of the accumulator into the previously selected RAM status character 2.
WR3[4]	1 1 1 0	0 1 1 1	Write the contents of the accumulator into the previously selected RAM status character 3.
SBM	1 1 1 0	1 0 0 0	Subtract the previously selected RAM main memory character from accumulator with borrow.
RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator.
RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)
ADM	1 1 1 0	1 0 1 1	Add the previously selected RAM main memory character to accumulator with carry.
RDϕ[4]	1 1 1 0	1 1 0 0	Read the previously selected RAM status character 0 into accumulator.
RD1[4]	1 1 1 0	1 1 0 1	Read the previously selected RAM status character 1 into accumulator.
RD2[4]	1 1 1 0	1 1 1 0	Read the previously selected RAM status character 2 into accumulator.
RD3[4]	1 1 1 0	1 1 1 1	Read the previously selected RAM status character 3 into accumulator.

Cont'd on next page

IS22 Cont'd

IS22 Cont'd

ACCUMULATOR GROUP INSTRUCTIONS

CLB	1 1 1 1	0 0 0 0	Clear both. (Accumulator and carry)
CLC	1 1 1 1	0 0 0 1	Clear carry.
IAC	1 1 1 1	0 0 1 0	Increment accumulator.
CMC	1 1 1 1	0 0 1 1	Complement carry.
CMA	1 1 1 1	0 1 0 0	Complement accumulator.
RAL	1 1 1 1	0 1 0 1	Rotate left. (Accumulator and carry)
RAR	1 1 1 1	0 1 1 0	Rotate right. (Accumulator and carry)
TCC	1 1 1 1	0 1 1 1	Transmit carry to accumulator and clear carry.
DAC	1 1 1 1	1 0 0 0	Decrement accumulator.
TCS	1 1 1 1	1 0 0 1	Transfer carry subtract and clear carry.
STC	1 1 1 1	1 0 1 0	Set carry.
DAA	1 1 1 1	1 0 1 1	Decimal adjust accumulator.
KBP	1 1 1 1	1 1 0 0	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
DCL	1 1 1 1	1 1 0 1	Designate command line.

OMIT FOR IS22a

MNEMONIC	OPR $D_3D_2D_1D_0$	OPA $D_3D_2D_1D_0$	DESCRIPTION OF OPERATION
HLT	0 0 0 0	0 0 0 1	Halt – inhibit program counter and data buffers.
BBS	0 0 0 0	0 0 1 0	Branch Back from Interrupt and restore the previous SRC. The Program Counter and send register control are restored to their pre-interrupt value.
LCR	0 0 0 0	0 0 1 1	The contents of the COMMAND REGISTER are transferred to the ACCUMULATOR.
OR4	0 0 0 0	0 1 0 0	The 4 bit contents of register #4 are logically "OR-ed" with the ACCUM.
OR5	0 0 0 0	0 1 0 1	The 4 bit contents of index register #5 are logically "OR-ed" with the ACCUMULATOR.
AN6	0 0 0 0	0 1 1 0	The 4 bit contents of index register #6 are logically "AND-ed" with the ACCUMULATOR
AN7	0 0 0 0	0 1 1 1	The 4 bit contents of index register #7 are logically "AND-ed" with the ACCUMULATOR.
DB0	0 0 0 0	1 0 0 0	DESIGNATE ROM BANK 0. CM-ROM$_0$ becomes enabled.
DB1	0 0 0 0	1 0 0 1	DESIGNATE ROM BANK 1. CM-ROM$_1$ becomes enabled.
SB0	0 0 0 0	1 0 1 0	SELECT INDEX REGISTER BANK 0. The index register: 0 - 7.
SB1	0 0 0 0	1 0 1 1	SELECT INDEX REGISTER BANK 1. The index registers 0* - 7*.
EIN	0 0 0 0	1 1 0 0	ENABLE INTERRUPT.
DIN	0 0 0 0	1 1 0 1	DISABLE INTERRUPT.
RPM	0 0 0 0	1 1 1 0	READ PROGRAM MEMORY.

NOTES (1)The condition code is assigned as follows

$C_1 = 1$ Invert jump condition $C_2 = 1$ Jump if accumulator is zero $C_4 = 1$ Jump if test signal is a 0
$C_1 = 0$ Not invert jump condition $C_3 = 1$ Jump if carry/link is a 1

(2)RRR is the address of 1 of 8 index register pairs in the CPU.

(3)RRRR is the address of 1 of 16 index registers in the CPU.

(4)Each RAM chip has 4 registers, each with twenty 4-bit characters subdivided into 16 main memory characters and 4 status characters. Chip number, RAM register and main memory character are addressed by an SRC instruction. For the selected chip and register, however, status character locations are selected by the instruction code (OPA).

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS25

IS25

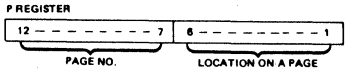
Note: The only instruction that can be used in ROM location 0000 is T* +1 (i.e., OP Code 81).

DEFINITIONS OF SYMBOLIC NOTATION

Symbols

A	Accumulator Register, A(4:1)
A/Bn	Line n of Address Bus
B	RAM Address Register, B(12:1)
C	Carry Link Flip-Flop
FF1, FF2	General Flip-Flop 1, General Flip-Flop 2
I	Instruction (Typically 8-bit Field)
I/Dn	Line n of Instruction/Data Bus
In	Byte n of Long Instruction (i.e. I1 = 1st byte, I2 = 2nd byte)
M	RAM Memory Contents Designated by Register B
m	General Numeric Designator, m = 1, 2, 3, . . .
n	General Numeric Designator, n = 1, 2, 3, . . .
P	ROM Program Counter Register, P (12:1)
BL	Lower Field of Register B (4:1)
BM	Middle Field of B Register, B (8:5)
BU	Upper Field of B Register, B (12:9)
R(n)	Bit n of General Register R
R(m:n)	Bits m thru n of General Register R inclusive [e.g.,R(12:7)]
SA	Upper Stack of Save Registers, SA(12:1)
SB	Lower Stack of Save Registers, SB(12:1)
W/IO	Write Command and I/O Enable Line
X	Secondary Accumulator Register, X(4:1)
Digit	Four Bit Field (sometimes referred to as Data or Character)
Byte	Eight Bit Field
Page	ROM Block of 64 Bytes (*)
←	Replaces
↔	Exchange
—	1's Complement (e.g., $\bar{A}$ is 1's complement of A)
V	Logical Inclusive OR
⊻	Logical Exclusive OR
∧	Logical and
+	Algebraic Add
-	Algebraic Subtract

*A page is defined in the PPS as 64 ROM address locations. The page number is specified by the six (6) most significant bits of the 12-bit P register. The locations within a page are defined by the six (6) least significant bits.



ARITHMETIC INSTRUCTIONS

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
AD	0B 0000 1011	Add (1 cycle)	The result of binary addition of contents of accumulator and 4-bit contents of the RAM currently addressed by B register, replaces the contents of accumulator. The resulting carry-out is loaded into C flip-flop.	C, A ← A+M
ADC	0A 0000 1010	Add with carry-in (1 cycle)	Same as AD except the C flip-flop serves as a carry-in to the adder.	C,A ← A+M+C
ADSK	09 0000 1001	Add and skip on carry-out (1 cycle)	Same as AD except the next ROM word will be skipped (ignored) if a carry-out is generated.	C,A ← A+M Skip if C = 1
ADCSK	08 0000 1000	Add with carry-in and skip on carry-out (1 cycle)	Same as ADSK except the C flip-flop serves as a carry-in to the adder.	C,A ← A+M+C Skip if C = 1
ADI	60-6E *0110 xxxx Except 65	Add immediate and skip on carry-out (1 cycle)	The result of binary addition of contents of accumulator and 4-bit immediate field of instruction word replaces the contents of accumulator. The next ROM word will be skipped (ignored) if a carry-out is generated. This instruction does not use or change the C flip-flop. The immediate field I(4:1) of this instruction may not be equal to binary 0000 or 1010 (See CYS and DC)	A ← A+[I(4:1)] Skip if carry-out = one I(4:1) ≠ 0000 I(4:1) ≠ 1010 See Note 3
DC	66 0110 0101	Decimal Correction (1 cycle)	Binary 1010 is added to contents of accumulator. Result is stored in accumulator. Instruction does not use or change carry flip-flop or skip.	A ← A+1010

LOGICAL INSTRUCTIONS

AND	0D 0000 1101	Logical AND (1 cycle)	The result of logical AND of accumulator and 4-bit contents of RAM currently addressed by B register replaces contents of accumulator.	A ← A∧M
OR	0F 0000 1111	Logical OR (1 cycle)	The result of logic OR of accumulator and 4-bit contents of RAM currently addressed by B register replaces contents of accumulator.	A ← A∨M
EOR	0C 0000 1100	Logical Exclusive-OR (1 cycle)	The result of logic exclusive-OR of accumulator and 4-bit contents of RAM currently addressed by B register replaces contents of accumulator.	A ← A⊻M
COMP	0E 0000 1110	Complement (1 cycle)	Each bit of the accumulator is logically complemented and placed in accumulator.	A ← $\bar{A}$

*xxxx Indicates restrictions on bit patterns allowable in immediate field as specified in the symbolic equation description.

DATA TRANSFER INSTRUCTION

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
SC	20 0010 0000	Set Carry flip-flop (1 cycle)	The C flip-flop is set to 1.	C ← 1
RC	24 0010 0100	Reset Carry flip-flop (1 cycle)	The C flip-flop is set to 0.	C ← 0
SF1	22 0010 0010	Set FF1 (1 cycle)	Flip-flop 1 is set to 1.	FF1 ← 1
RF1	26 0010 0110	Reset FF1 (1 cycle)	Flip-flop 1 is set to 0.	FF1 ← 0
SF2	21 0010 0001	Set FF2 (1 cycle)	Flip-flop 2 is set to 1.	FF2 ← 1
RF2	25 0010 0101	Reset FF2 (1 cycle)	Flip-flop 2 is set to 0.	FF2 ← 0
LD	30-37 0011 0 . . .	Load Accumulator from Memory (1 cycle)	The 4-bit contents of RAM currently addressed by B register are placed in the accumulator. The RAM address in the B register is then modified by the result of an exclusive-OR of the 3-bit immediate field I(3:1) and B(7:5).	A ← M; B(7:5) ← B(7:5)⊻[I(3:1)] See Note 3
EX	38-3F 0011 1 . . .	Exchange Accumulator and Memory (1 cycle)	Same as LD except the contents of accumulator are also placed in currently addressed RAM location.	A ↔ M B(7:5) ← B(7:5)⊻[I(3:1)] See Note 3
EXD	28-2F 0010 1 . . .	Exchange Accumulator and Memory and decrement BL (1 cycle) See Note 3	Same as EX except RAM address in B register is further modified by decrementing BL by 1. If the new contents of BL is 1111, the next ROM word will be ignored.	A ↔ M B(7:5) ← B(7:5)⊻[I(3:1)]; BL ← BL-1 Skip on BL=1111
LDI	70-7F 0111	Load Accumulator Immediate (1 cycle)	The 4-bit contents, immediate field I(4:1), of the instruction are placed in accumulator. (See Note below)	A ← [I(4:1)] See Note 3
LAX	12 0001 0010	Load Accumulator from X register (1 cycle)	The 4-bit contents of the X register are placed in the accumulator	A ← X
LXA	1B 0001 1011	Load X register from Accumulator (1 cycle)	The contents of the accumulator are transferred to the X register.	X ← A
LABL	11 0001 0001	Load Accumulator with BL (1 cycle)	The contents of BL register are transferred to the accumulator.	A ← BL
LBMX	10 0001 0000	Load BM with X (1 cycle)	The contents of X register are transferred to BM register	BM ← X
LBUA	04 0000 0100	Load BU with A (1 cycle)	The contents of accumulator are transferred to BU register. Also, the contents of currently addressed RAM are transferred to accumulator.	BU ← A, A ← M

NOTE
Only the first occurrence of an LDI in a consecutive string of LDI's will be executed. The program will ignore the remaining LDI's and execute next valid instruction.

DATA TRANSFER INSTRUCTIONS (CONT)

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
XABL	19 0001 1001	Exchange Accumulator and BL (1 cycle)	The contents of accumulator and BL register are exchanged.	A ↔ BL
XBMX	18 0001 1000	Exchange BM and X (1 cycle)	The contents of BM register and X register are exchanged.	X ↔ BM
XAX	1A 0001 1010	Exchange Accumulator and X (1 cycle)	The contents of accumulator and X register are exchanged.	A ↔ X
XS	06 0000 0110	Exchange SA and SB (1 cycle)	The 12-bit contents of SA register and SB register are exchanged.	SA ↔ SB
CYS	6F 0110 1111	Cycle SA register and accumulator. (1 cycle)	A 4-bit right shift of the SA register takes place with the four bits which are shifted off the end of SA being transferred into the accumulator. The contents of the accumulator are placed in the left end of SA register.	A ← SA(4:1) SA(4:1) ← SA(8:5) SA(8:5) ← SA(12:9) SA(12:9) ← A
LB*	CO-CF 1st word 1100 . . . . 2nd word from page 3	Load B Indirect (2 cycles)	Sixteen consecutive locations on ROM page 3 (I_2) contain data which can be loaded into the eight least significant bits of the B register by use of any LB instruction. The four most significant bits of B register will be loaded with zeros. The contents of the SB register will be destroyed and loaded with O's. This instruction takes two cycles to execute but occupies only one ROM word. (Automatic return) (See Note below.)	SB ← SA, SA ← P P(12:5) ← 0000 1100 P(4:1) ← I1(4:1) BU ← 0000 B(8:1) ← [I2(8:1)] P ← SA, SA ← SB ← 0 See Notes 3 and 4
LBL*	00 1st word 0000 0000 2nd word	Load B Long (2 cycles)	This instruction occupies two ROM words, the second of which will be loaded into the eight least significant bits of the B register. The four most significant bits of B (BU) will be loaded with zeros. (See Note below.)	BU ← 0000 B(8:1) ← [I2(8:1)] See Note 3
INCB	17 0001 0111	Increment BL (1 cycle)	BL register (least significant four bits of B register) is incremented by 1. If the new contents of BL is 0000, then the next ROM word will be ignored.	BL ← BL +1 Skip on BL=0000
DECB	1F 0001 1111	Decrement BL (1 cycle)	BL register is decremented by 1. If the new contents of BL is 1111, then the next ROM word will be ignored.	BL ← BL-1 Skip on BL = 1111

NOTE
*Only the first occurrence of an LB or LBL instruction in a consecutive string of LB or LBL will be executed. The program will ignore the remaining LB or LBL and execute the next valid instruction. Within subroutines the LB instruction must be used with caution because the contents of SB have been modified.

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CONTROL TRANSFER INSTRUCTIONS

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
T	80-BF 10-- ----	Transfer (1 cycle)	An unconditional transfer to a ROM word on the current page takes place. The least significant 6-bits of P register P(6:1) are replaced by six bit immediate field I(6:1).	P(6:1) ← I(6:1)
TM	DO-FF 1st word 11xx --[*]- 2nd word from page 3 ---- ----	Transfer and Mark Indirect (2 cycles)	48 Consecutive locations on ROM page 3 contains pointer data which identify subroutine entry addresses. These subroutine entry addresses are limited to pages 4 through 7. This TM instruction will save the address of the next ROM word in the SA register after loading the original contents of SA into SB. A transfer then occurs to one of the subroutine entry addresses. This instruction occupies one ROM word but takes two cycles for execution.	SB ← SA, SA ← P P(12:7) ← 000011 P(6:1) ← I1(6:1) P(12:9) ← 0001 P(8:1) ← I2(8:1) See Note 4 Note: I1(6:5)≠ 00
TL	50-5F 1st word 0101 ---- 2nd word ---- ----	Transfer Long (2 cycles)	This instruction executes a transfer to any ROM word on any page. It occupies two ROM words and requires two cycles for execution. The first byte loads P(12:9) with field I1(4:1) and then the second byte I2(8:1) is placed in P(8:1).	P(12:9) ← I1(4:1); P(8:1) ← I2(8:1)
TML	01-03 1st word 0000 00xx* 2nd word ---- ----	Transfer and Mark Long (2 cycles)	This instruction executes a transfer and mark to any location on ROM pages 4 through 15. It occupies two ROM words and requires two cycle times for execution.	See Note 4 SB ← SA, SA ← P P(12:9) ← I1(4:1) P(8:1) ← I2(8:1) Note I1(2:1) ≠ 00
SKC	15 0001 0101	Skip on Carry flip-flop (1 cycle)	The next ROM word will be ignored if C flip-flop is 1.	Skip if C = 1
SKZ	1E 0001 1110	Skip on Accumulator Zero (1 cycle)	The next ROM word will be ignored if accumulator is zero.	Skip if A = 0
SKBI	40-4F 0100 ----	Skip if BL Equal to Immediate (cycle)	The next ROM word will be ignored if the least significant four bits of B register (BL) is equal to the 4-bit immediate field I(4:1) of instruction.	Skip if BL = I(4:1)
SKF1	16 0001 0110	Skip if FF1 Equals 1 (1 cycle)	The next ROM word will be ignored if FF1 is 1.	Skip if FF1 = 1
SKF2	14 0001 0100	Skip if FF2 Equals 1 (1 cycle)	The next ROM word will be ignored if FF2 is 1.	Skip if FF2 = 1
RTN	05 0000 0101	Return (1 cycle)	This instruction executes a return from subroutine by loading contents of SA register into P register and interchanges the SB and SA registers.	P ← SA, SA ↔ SB

*xx Indicates restrictions on bit patterns allowable in the designated bit positions in the instruction field as specified in the symbolic equation description.

CONTROL TRANSFER INSTRUCTIONS (CONT)

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
RTNSK	07 0000 0111	Return and Skip (1 cycle)	Same as RTN except the first ROM word encountered after the return from subroutine is skipped.	P ← SA, SA ↔ SB P ← P+1

INPUT/OUTPUT INSTRUCTIONS

IOL	1C 1st word 0001 1100 2nd word ---- ----	Input/Output Long (2 cycles)	This instruction occupies two ROM words and requires two cycles for execution. The first ROM word is received by the CPU and sets up the I/O Enable signal. The second ROM word is then received by the I/O devices and decoded for address and command. The contents of the accumulator inverted are placed on the data lines for acceptance by the I/O. At the same time, input data received by the I/O device is transferred to the accumulator inverted.	I2 ← I/O Device $\overline{A}$ ← Data Bus A ← $\overline{\text{Data Bus}}$
DIA	27 0010 0111	Discrete Input Group A (1 cycle)	Data at the inputs to discrete. Group A is transferred to the accumulator.	A ← DIA
DIB	23 0010 0011	Discrete Input Group B (1 cycle)	Data at the inputs to discrete. Group B is transferrad to the accumulator.	A ← DIB
DOA	1D 0001 1101	Discrete Output (1 cycle)	The contents of the accumulator are transferred to the discrete output register.	DOA ← A

SPECIAL INSTRUCTION

SAG	13 0001 0011	Special Address Generation (1 cycle)	This instruction causes the eight most significant bits of the RAM address output to be zeroed during the next cycle only. Note that this instruction does not alter the contents of the B register.	A/B Bus (12:5) ← 0000 0000 A/B Bus (4:1) ← BL (4:1) Contents of "B" remain unchanged

GENERAL NOTES

(1) The word "skip" or "ignore" as used in this instruction set means the word will read from memory but not executed. Each skipped or ignored word will require one clock cycle time.

(2) The reference to ROM pages and locations are defined as the ROM address appearing on the A/B bus. During initial Power On the starting address is Page 0 Location 0 and is automatically incremented each clock cycle.

(3) Instruction ADI, LD, EX, EXD, LDI, LB and LBL have a numeric value coded as part of the instruction in the immediate field. This numeric value must be in complementary form on the bus. All of these immediate fields which are inverted are shown in brackets.
For example: ADI 1, as written by the programmer who wishes to add one to the value in the accumulator, is converted to $6E_{(16)}$=0110[1110] ; the bracketed binary value is the value as seen on the data bus.
If the programmer is using the Rockwell Assembler he does not have to manually determine the proper inverted value as the assembler does this for him.

(4) On all instructions which transfer the contents of P into SA, the P register has already been advanced to the next instruction location.

CAUTION

The only instruction that can be used in ROM location 0000 is transfer instruction T* + 1 (i.e., OP Code 81).

I/O SECTION INSTRUCTIONS

IS25a ONLY

Mnemonic	Command Name	I/D Bus 8 7 6 5 4 3 2 1	Accumulator A4 A3 A2 A1	Description
SES	Select Enable Status	0 S S 0 X X X 0	1 X X X	Enable All Outputs (Enable F/F ← 1) Accumulator ← 1XXX if I/O(00BL) = 1 Accumulator ← 0XXX if I/O(00BL) = 0
SES	Select Enable Status	0 S S 0 X X X 0	0 X X X	Disable All Outputs (Enable F/F ← 0) Accumulator ← 1XXX if I/O(00BL) = 1 Accumulator ← 0XXX if I/O(00BL) = 0
SOS	Select Output Status	0 S S 0 X X X 1	1 X X X	I/O(00BL) F/F ← 1 Accumulator ← 1XXX Accumulator ← 0XXX if I/O(00BL) = 0
SOS	Select Output Status	0 S S 0 X X X 1	0 X X X	I/O(00BL) F/F ← 0 Accumulator ← 1XXX if I/O(00BL) = 1 Accumulator ← 0XXX if I/O(00BL) = 0

Op Code	Bytes	Cycles	Description
RAM Addressing Instructions			
LAB	1	1	Load Accumulator from B Lower (least significant 4 bits)
LBA	1	1	Load B Lower from Accumulator
*LB **	1	1	Load B Upper with zero and B Lower with immediate field
*EOB	1	1	Exclusive Or B-Upper with three bit immediate field
*LBL **	2	2	Load B Register Long with 7 bit (4 bits 1st byte, 3 bits 2nd byte) immediate field
*INCB	2	2	Increment B Lower and modify B Upper with 2 bit immediate field; Skip if BL counts to 0. This instruction should not be skipped.
*DECB	2	2	Decrement B Lower and modify B Upper with 2 bit immediate field; Skip if BL counts to 15. This instruction should not be skipped.
Bit Manipulation Instructions			
*SB	1	1	Set Bit in word in memory. Specific bit designated by 2 bit immediate field and specific word addressed by B register
*RB	1	1	Reset Bit in word in memory. Specific bit designated by 2 bit immediate field and specific word addressed by B register
*SKBF	1	1	Skip on designated Bit in addressed Memory when bit is false (zero). Bit is selected by 2 bit immediate field.
Register to Register Instructions			
LXA	1	1	Load X Register from Accumulator
XAX	1	1	Exchange Accumulator and X Register contents
XAS	1	1	Exchange Accumulator and S-Register contents
Register Memory Instructions			
*L	1	1	Load Accumulator from Memory and modify B Upper with 2-bit immediate field
*X	1	1	Exchange Accumulator with Memory and modify B Upper with 2-bit immediate field
*XDSK	1	1	Exchange Accumulator with Memory and modify B Upper with 2-bit immediate field; Decrement B Lower and Skip if BL ≠ 15
*XNSK	1	1	Exchange Accumulator with Memory and modify B Upper with 2-bit immediate field; Increment B Lower and Skip if BL ≠ 0
Arithmetic Instructions			
A	1	1	Add Memory to Accumulator (carry not used or set)
AC	1	1	Add Memory and Carry to Accumulator; form sum and carry
ACSK	1	1	Add Memory and Carry to Accumulator; Skip if resulting Carry equals "one"
DC	1	1	Decimal Correct (Add 6 with no carry in or out and no skip)
COM	1	1	Complement Accumulator
RC	1	1	Reset Carry
SC	1	1	Set Carry
SKNC	1	1	Skip on No Carry
*LAI ***	1	1	Load Accumulator with contents of Immediate field
*AISK	1	1	Add Accumulator and Immediate field, Skip on No Overflow. No Carry is set. (AISK 6 = DC so no skip occurs)
ROM Addressing Instructions			
RT	1	2	Return from Subroutine
RTSK	1	2+	Return from Subroutine-Skip first instruction of one or two bytes in length (3 cycles or 4 cycles)
T	1	2	Transfer on page to 6 bit immediate field location
NOP	1	1	No Operation
TL	2	3	Transfer Long off page to pages 1 through 15
TLB	3	4	Transfer Long Banked off page to pages 17 through 21
TM	1	2	Transfer and Mark to special subroutine page 22
TML	2	3	Transfer and Mark Long to subroutine on pages 1 through 15
TMLB	3	4	Transfer and Mark Long Banked to subroutine on pages 17 through 21

*The immediate field (IF) is two, three or four bits which are included as part of the 8-bit instruction. If not specified otherwise the immediate field is 4 bits.

**When LB or LBL instructions appear in sequence as a string of LB or LBL or mixtures of LB and LBL instructions only the first one of them will be executed. The remainder of the LB or LBL instructions in the sequence will be ignored.

***When more than one LAI instruction occurs in sequence, only the first LAI instruction encountered will be executed. The remainder of the LAI instructions in the string will be ignored.

Op Code	Bytes	Cycles	Description
Logical Comparison Instructions			
SKMEA	1	1	Skip on Memory Equals Accumulator
*SKBEI	2	2	Skip on B-Lower Equals Immediate field**
*SKAEI	2	2	Skip on Accumulator Equals Immediate field** (IF ≠ 15)
Input/Output Instructions			
SOS	1	1	Set Output, bit selected by B Lower
ROS	1	1	Reset Output, bit selected by B Lower
SKIH	1	1	Skip on Input High on bit selected by B Lower
IX	1	1	Input to X Register from RIO lines 5 thru 8
OX	1	1	Output from X Register to RIO lines 5 thru 8
IOA	1	1	Input A Receivers to Accumulator and Output A to A Buffer to RIO lines 1 thru 4 (mask option to also output X to X Buffers)
IOS	1	1	Serial Input and Output from S — shifting takes 8 cycles concurrent with other instruction operations
I1SK	1	1	Input Channel 1, Add to A and Skip if No Carry is generated
I2C	1	1	Input Channel 2 to A and complement
INT1L	1	1	Skip on INT1 equals -V
INT0H	1	1	Skip on INT0 equals V_{SS}
Conditional Transfer Instructions †			
TC	2	3-2	Transfer within page on Carry Set
TNC	3	4-3	Transfer within page on No Carry Set
TLC	3	4-3	Transfer Long on Carry Set
TLNC	4	5-3	Transfer Long on No Carry Set
TBF	3	4-3	Transfer within page on Bit in Memory False
TBT	2	3-2	Transfer within page on Bit in Memory True
TLBF	4	5-3	Transfer Long on Bit in Memory False
TLBT	3	4-3	Transfer Long on Bit in Memory True
TE	3	4-3	Transfer within page on A Equal Memory
TNE	2	3-2	Transfer within page on A Not Equal Memory
TLE	4	5-3	Transfer Long on A Equal Memory
TLNE	3	4-3	Transfer Long on A Not Equal Memory
TIH	3	4-3	Transfer within page if input Selected by B Lower is High
TIL	2	3-2	Transfer within page if Input Selected by B Lower is Low
TLIH	4	5-3	Transfer Long on Input Selected High
TLIL	3	4-3	Transfer Long on Input Selected Low

† These are all macro instructions which must not be preceded by an instruction which executes a skip. In the cycles column the first number indicates number of cycles when condition is met and second number indicates number of cycles when the condition for transfer is not met.

IS27

IS27

Symbol	Symbolic Notation Item or Function
A	Accumulator Register A (1:8)
X	RAM Address Register and Index, X(1:8)
Y	RAM Address Register Y(1:8)
Z	RAM Address Register Z(1:8)
L	Link Register L(1:16)
P	Program Counter Register P(1:14)
S	Stack Pointer Register
W	The W Register
C	Carry Flip-Flop
IC	Intermediate state of Carry Flip-Flop
Q	Intermediate Carry Flip-Flop
I	Instruction I(1:8)
I1	First byte of multiple byte instruction I1(1:8)
I2	Second byte of multiple byte instruction I2(1:8)
I3	Third byte of multiple byte instruction I3(1:8)
M	RAM memory contents
R(n)	Bit n of Register R
R(n:m)	Bit n through m of R, inclusively
W/IO	Write and I/O Enable Control Line
RIH	Read Inhibit Control Line
Byte	Eight-bit Data Field
Digit	Four-bit Data Field
Page	Block of 128 bytes
⟶	Replaces (or ⟵)
⟷	Exchange
$\overline{R}$	1's complement of state R
^	Logical Product (AND)
v	Logical Sum (Inclusive OR)
v	Logical (Exclusive OR)
-	Algebraic Subtract
+	Algebraic Add
>	Greater than
<	Less than
=	Equal to
I/D(8:1)	Instruction/Data Bus (lines 1 through 8)
(L)	ROM memory contents addressed by L
SP_u	Byte from upper address portion of Subroutine Entry Pool
SP_l	Byte from lower address portion of Subroutine Entry Pool

Mnemonic	Name	Bytes	Cycles	Description	
				Verbal	Symbolic
L	Load A	1	1	The current RAM operand is placed in the accumulator	A⟵M
LN	Load A, Increment Address	1	1	Same as L. Additionally, the X register is incremented	A⟵M X⟵X+1, skip if X=0
LD	Load A, Decrement Address	1	1	Same as L. Additionally, the X register is decremented	A⟵M X⟵X-1, skip if X=127
LNXL	Load A, Increment Address, Exchange L	1	1	Same as LN. Additionally, the contents of the L register and the Z & X registers are exchanged	A⟵M X⟵X+1, skip if X=0 Z, X⟷L
LDXL	Load A, Decrement Address, Exchange L	1	1	Same as LD. Additionally the contents of the L register and the Z & X registers are exchanged	A⟵M X⟵X-1, skip if X=127 Z, X⟷L
LNCX	Load A, Increment & Compare Address, Exchange L	1	1	Same as LNXL. Additionally, the next instruction is skipped if X = Y	A⟵M X⟵X+1 Skip if X(7:1)≠0 or X(7:1)≠Y(7:1) Z, X⟷L
LDCX	Load A, Decrement & Compare Address, Exchange L	1	1	Same as LDXL. Additionally, the next instruction is skipped if X = Y	A⟵M X⟵X-1 Skip if X(7:1)≠127 or X(7:1)≠Y(7:1) Z, X⟷L
LNXY	Load A, Increment Address, Exchange Y	1	1	Same as LN. Additionally, the contents of the X & Y registers are exchanged	A⟵M X⟵X+1, skip if X=0 X⟷Y
S	Store A	1	1	The contents of the accumulator are stored in the current RAM operand address	M⟵A
SN	Store A, Increment Address	1	1	Same as S. Additionally, the X register is incremented	M⟵A X⟵X+1, skip if X=0
SD	Store A, Decrement Address	1	1	Same as S. Additionally, the X register is decremented	M⟵A X⟵X-1, skip if X=127
SNXL	Store A, Increment Address, Exchange L	1	1	Same as SN. Additionally, the contents of the L register and the Z & X registers are exchanged	M⟵A X⟵X+1, skip if X=0 Z, X⟷L

Mnemonic	Name	Bytes	Cycles	Description	
				Verbal	Symbolic
SDXL	Store A, Decrement Address, Exchange L	1	1	Same as SD. Additionally, the contents of the L register and the Z & X registers are exchanged	M⟵A X⟵X-1, skip if X=127 Z, X⟷L
SNCX	Store A, Increment & Compare Address, Exchange L	1	1	Same as SNXL. Additionally, the next instruction is skipped if X = Y	M⟵A X⟵X+1 Skip if X(7:1)≠0 or X(7:1)≠Y(7:1) Z, X⟷L
SDCX	Store A, Decrement & Compare Address, Exchange L	1	1	Same as SDXL. Additionally, the next instruction is skipped if X = Y	M⟵A X⟵X-1 Skip if X(7:1)≠127 or X(7:1)≠Y(7:1) Z, X⟷L
SNXY	Store A, Increment Address, Exchange Y	1	1	Same as SN. Additionally, the contents of the X and Y registers are exchanged	M⟵A X⟵X+1, skip if X=0 X⟷Y
X	Exchange	2	2	These instructions are identical to the corresponding store instructions except that the accumulator and the current RAM operand are exchanged	A⟷M
XN	Exchange, Increment Address	2	2		A⟷M X⟵X+1, skip if X=0
XD	Exchange, Decrement Address	2	2		A⟷M X⟵X-1, skip if X=127
XNXL	Exchange, Increment Address, Exchange L	2	2		A⟷M X⟵X+1, skip if X=0 Z, X⟷L
XDXL	Exchange, Decrement Address, Exchange L	2	2		A⟷M X⟵X-1, skip if X=127 Z, X⟷L
XNCX	Exchange, Increment & Compare Address, Exchange L	2	2		A⟷M X⟵X+1 Skip if X(7:1)≠0 or X(7:1)≠Y(7:1) Z, X⟷L
XDCX	Exchange, Decrement & Compare Address, Exchange L	2	2	These instructions are identical to the corresponding store instructions except that the accumulator and the current RAM operand are exchanged	A⟷M X⟵X-1 Skip if X(7:1)≠127 or X(7:1)≠Y(7:1) Z, X⟷L

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Mnemonic	Name	Bytes	Cycles	Description	
				Verbal	Symbolic
XNXY	Exchange, Increment Address, Exchange Y	2	2	These instructions are identical to the corresponding store instructions except that the accumulator and the current RAM operand are exchanged	A ⟷ M X ← X+1, skip if X=0 X ⟷ Y
LX	Load X	1,2	2	The current RAM operand is placed in the X register	X ← M
LY	Load Y	1,2	2	The current RAM operand is placed in the Y register	Y ← M
LZ	Load Z	1,2	2	The current RAM operand is placed in the Z register	Z ← M
LAI	Load A Immediate	1-3	3	The specified literal operand is placed in the accumulator	A ← I3
LXI	Load X Immediate	1-3	3	The specified literal operand is placed in the X register	X ← I3
LYI	Load Y Immediate	1-3	3	The specified literal operand is placed in the Y register	Y ← I3
LZI	Load Z Immediate	1-3	3	The specified literal operand is placed in the Z register	Z ← I3
LAL	Load A through Link	1,2	3	The ROM operand addressed by the L register is placed in the accumulator	W ← A, A ← (L) L ← L+1 L(16) ← C
LXL	Load X through Link	1,2	3	The ROM operand addressed by the L register is placed in the X register	X ← (L) L ← L+1 L(16) ← C
LYL	Load Y through Link	1,2	3	The ROM operand addressed by the L register is placed in the Y register	Y ← (L) L ← L+1 L(16) ← C
LZL	Load Z through Link	1,2	3	The ROM operand addressed by the L register is placed in the Z register	Z ← (L) L ← L+1 L(16) ← C
LXA	Load X from A	1	1	The contents of the accumulator are placed in the X register	X ← A
LYA	Load Y from A	1	1	The contents of the accumulator are placed in the Y register	Y ← A
LZA	Load Z from A	1	1	The contents of the accumulator are placed in the Z register	Z ← A

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Mnemonic	Name	Bytes	Cycles	Description	
				Verbal	Symbolic
LLA	Load L from A	1	1	The contents of the accumulator are placed in the upper 8 bits of the L register	L(16:9) ← A
XY	Exchange Y	1	1	The contents of the X and Y register are exchanged	X ⟷ Y
XL	Exchange L	1	1	The contents of the L register and the Z & X registers are exchanged	L ⟷ Z,X
XAX	Exchange A and X	1	1	The contents of the X register and the accumulator are exchanged	A ⟷ X
XAY	Exchange A and Y	1	1	The contents of the Y register and the accumulator are exchanged	A ⟷ Y
XAZ	Exchange A and Z	1	1	The contents of the Z register and the accumulator are exchanged	A ⟷ Z
XAL	Exchange A and L	1	1	The contents of the upper half of the L register and the accumulator are exchanged	A ⟷ L(16:9)
INCX	Increment X	1	1	The X register is incremented by one	X ← X+1 Skip if X=0
DECX	Decrement X	1	1	The X register is decremented by one	X ← X-1 Skip if X=127
INXY	Increment X, Exchange Y	1	1	The X register is incremented and the contents of the X and Y registers are exchanged	X ← X+1, skip if X=0 X ⟷ Y
DEXY	Decrement X, Exchange Y	1	1	The X register is decremented and the contents of the X and Y registers are exchanged	X ← X-1, skip if X=127 X ⟷ Y
INCY	Increment Y	2	2	The Y register is incremented by one	Y ← Y+1 Skip if Y=0
DECY	Decrement Y	2	2	The Y register is decremented by one	Y ← Y-1 Skip if Y=127
PSHA	Push A	1,2	2	The contents of the accumulator are pushed into the stack	A → (S) S ← S+1
PSHX	Push X	1,2	2	The contents of the X register are pushed into the stack	X → (S) S ← S+1
PSHY	Push Y	1,2	2	The contents of the Y register are pushed into the stack	Y → (S) S ← S+1

Mnemonic	Name	Bytes	Cycles	Description	
				Verbal	Symbolic
PSHZ	Push Z	1,2	2	The contents of the Z register are pushed into the stack	Z → (S) S ← S+1
PSHL	Push L	1	3	The contents of the L register are pushed into the stack and replaced by the contents of the A and W registers	L → (S+1, S) A,W ← L S ← S+2
POPA	Pop A	1,2	2	The uppermost byte is popped from the stack and placed in the accumulator	S ← S-1 A ← (S) Skip if S=31
POPX	Pop X	1,2	2	The uppermost byte is popped from the stack and placed in the X register	S ← S-1 X ← (S) Skip if S=31
POPY	Pop Y	1,2	2	The uppermost byte is popped from the stack and placed in the Y register	S ← S-1 Y ← (S) Skip if S=31
POPZ	Pop Z	1,2	2	The uppermost byte is popped from the stack and placed in the Z register	S ← S-1 Z ← (S) Skip if S=31
POPL	Pop L	1	3	The uppermost 2 bytes are popped from the stack and placed in the L register	S ← S-2 L ← (S+1, S)
A	Add	1	1	The sum of the accumulator and the current RAM operand are placed in the accumulator	C,A ← A+M Q ← IC
AC	Add with Carry	1	1	Same as A except the carry flip-flop, C, is used as a carry-in	C,A ← A+M+C Q ← IC
ASK	Add, Skip on Carry	1	1	Same as A. Additionally, the next instruction is skipped if a carry-out is generated	C,A ← A+M Q ← IC Skip if C=1
ACSK	Add with Carry, Skip on Carry	1	1	Same as AC. Additionally, the next instruction is skipped if a carry-out is generated	C,A ← A+M+C Skip if C=1
AISK	Add Immediate, Skip on Carry	1-3	3	The sum of the accumulator and the specified literal operand is placed in the accumulator	A ← A+I3 Q ← IC Skip if carry-out
INCA	Increment A	1	1	The accumulator is incremented by one	A ← A+1 Q ← IC
DC	Decimal Correct (1)	1	1	The hexadecimal value 66 is added to the accumulator	A ← $A+66_{16}$ Q ← IC

Mnemonic	Name	Bytes	Cycles	Description	
				Verbal	Symbolic
DCC	Decimal Correct (2)	1	1	The accumulator is modified based on the states of the C & Q flip-flops	C,Q 0,0 A ← $A+(9A)_{16}$ 0,1 A ← $A+(A0)_{16}$ 1,0 A ← $A+(FA)_{16}$ 1,1 No change
AN	Logical AND	1	1	The logical product of the accumulator and the current RAM operand is placed in the accumulator	A ← A∧M
ANI	Logical AND Immediate	1-3	3	The logical product of the accumulator and the specified literal operand is placed in the accumulator	A ← A∧I3
OR	Logical OR	1	1	The logical sum of the accumulator and the current RAM operand is placed in the accumulator	A ← A∨M
EOR	Logical Exclusive OR	1	1	The logical exclusive OR (addition without carry) of the accumulator and the current RAM operand is placed in the accumulator	A ← A⊻M
COM	Complement	1	1	The one's complement of the accumulator is placed in the accumulator	A ← $\overline{A}$
SC	Set Carry	1	1	The carry flip-flop, C, is set (1)	C ← 1
RC	Reset Carry	1	1	The carry flip-flop, C, is reset (0)	C ← 0
RAR	Rotate A Right	1	1	The accumulator and C flip-flop are circular shifted one bit to the right	A(8:1) → C
RAL	Rotate A Left	1	1	The accumulator and C flip-flop are circular shifted one bit to the left	A(8:1) ← C
MDR	Move Digit Right	1	1	The accumulator is shifted right 4 bits and the least significant 4 bits of the current RAM operand are placed in the vacated accumulator positions	A(8:5) → A(4:1) M(4:1) → A(8:5)
MDL	Move Digit Left	1	1	The accumulator is shifted left 4 bits and the most significant 4 bits of the current RAM operand are placed in the vacated accumulator positions	A(8:5) ← A(4:1) A(4:1) ← M(8:5)

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Mnemonic	Name	Bytes	Cycles	Description	
				Verbal	Symbolic
SB	Set Bit (n)	1,2	2	The specified bit of the current RAM operand is set (1)	$M \leftarrow M \vee 2^{(n-1)}$
RB	Reset Bit (n)	1,2	2	The specified bit of the current RAM operand is reset (0)	$M \leftarrow M \wedge \overline{2^{(n-1)}}$
B	Branch	1,2	1,2	The specified address is placed in the P register	P(7:1) ← I1(7:1) If I1(8)=1, P(14:8) ← I2(7:1)
BDI	Branch, Disable Interrupts	2	2	Same as B. Additionally, the interrupts are disabled	P(7:1) ← I1(7:1) P(14:8) ← I2(7:1) Disable interrupts
BL	Branch and Link	1,2	3	The specified address is placed in the P register. The previous contents of the P register (incremented) are saved in the L register together with the state of the C flip-flop. The previous contents of the L register are pushed into the stack	L → (S+1, S) S ← S+2 P → L(15:9, 7:1) C → L(16) If I1(6)=1 P(14:8) ← SP_U(7:1) P(7:1) ← SPI(7:1) If I1(6)=0 P(12:8) ← I1(5:1) P(7:1) ← I2(7:1) P(13) ← I2(8) P(14) ← 0
RT	Return	1	3	The P register and C flip-flop are loaded from the L register. The uppermost 2 bytes are popped from the stack and placed in the L register	P ← L(15:9,7:1) C ← L(16) S ← S-2 L ← (S+1, S)
RSK	Return & Skip	1	3	Same as RT except that the next instruction (i.e., the instruction at the "return" location) is skipped	P ← L(15:9,7:1) C ← L(16) S ← S-2, L ← (S+1, S) Skip next instruction
RTI	Return, Enable Interrupts	1	3	Same as RT. Additionally, the interrupts are enabled	P ← L(15:9,7:1) C ← L(16) S ← S-2, L ← (S+1, S) Enable interrupts
NOP	No Operation	1	1	No function is performed. The branch condition tag is used	
SKC	Skip if Carry	1	1	The next instruction is skipped if the carry flip-flop, C, is set	Skip if C=1

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Mnemonic	Name	Bytes	Cycles	Description	
				Verbal	Symbolic
SKNC	Skip if No Carry	1	1	The next instruction is skipped if the carry flip-flop,C, is reset	Skip if C=0
SKZ	Skip if Zero	1	1	The next instruction is skipped if the accumulator equals zero	Skip if A=0
SKNZ	Skip if Non-Zero	1	1	The next instruction is skipped if the accumulator does not equal zero	Skip if A≠0
SKP	Skip if Positive	1	1	The next instruction is skipped if the most significant bit of the accumulator is zero	Skip if A(8)=0
SKN	Skip if Negative	1	1	The next instruction is skipped if the most significant bit of the accumulator is one	Skip if A(8)=1
SKE	Skip if Equal	1	1	The next instruction is skipped if the accumulator and the current RAM operand are equal	Skip if A=M
BBT	Branch if Bit (n) True	2,3	2,3	A program branch is executed if the specified bit of the current RAM operand is true (1)	If $M \wedge 2^{(n-1)}=1$, then P(7:1) ← I2(7:1) & if I2(8)=1, P(14:8) ← I3(7:1)
BBF	Branch if Bit (n) False	2,3	2,3	A program branch is executed if the specified bit of the current RAM operand is false (0)	If $M \wedge 2^{(n-1)}=0$ then P(7:1) ← I2(7:1) & if I2(8)=1, P(14:8) ← I3(7:1)
BC	Branch if Carry	2,3	2,3	A program branch is executed if the carry flip-flop, C, is set (1)	If C=1, then P(7:1) ← I2(7:1) & if I2(8)=1, P(14:8) ← I3(7:1)
BNC	Branch if No Carry	2,3	2,3	A program branch is executed if the carry flip-flop, C, is reset (0)	If C=0, then P(7:1) ← I2(7:1) & if I2(8)=1, P(14:8) ← I3(7:1)
BZ	Branch if Zero	2,3	2,3	A program branch is executed if the accumulator equals zero	If A=0, then P(7:1) ← I2(7:1) & if I2(8)=1, P(14:8) ← I3(7:1)
BNZ	Branch if Non-Zero	2,3	2,3	A program branch is executed if the accumulator does not equal zero	If A≠0, then P(7:1) ← I2(7:1) & if I2(8)=1, P(14:8) ← I3(7:1)

Mnemonic	Name	Bytes	Cycles	Description	
				Verbal	Symbolic
BP	Branch if Positive	2,3	2,3	A program branch is executed if the most significant bit of the accumulator is zero	If A(8)=0, then P(7:1) ← I2(7:1) & if I2(8)=1, P(14:8) ← I3(7:1)
BN	Branch if Negative	2,3	2,3	A program branch is executed if the most significant bit of the accumulator is one	If A(8)=1, then P(7:1) ← I2(7:1) & if I2(8)=1, P(14:8) ← I3(7:1)
BNE	Branch if Not Equal	2,3	2,3	A program branch is executed if the accumulator is not equal to the current RAM operand	If A≠M, then P(7:1) ← I2(7:1) & if I2(8)=1, P(14:8) ← I3(7:1)
IO4	Digit I/O (C, D)	2	2	Command C is transmitted to I/O device D. Bits 8-5 of the accumulator are transmitted to the device and bits 1-4 are received from the device	I2 → I/D(8:1) A(8:5) → I/D(8:5) A(4:1) ← I/D(4:1)
IN	Input (C, D)	2	2	Command C is transmitted to I/O device D. The accumulator is loaded with a data byte transmitted by the device. If D is omitted, a zero (all-call) device address is transmitted	I2 → I/D(8:1) A ← I/D(8:1)
OUT	Output (C, D)	2	2	Same as IN except the accumulator contents are transmitted to the device	I2 → I/D(8:1) A → I/D(8:1)
RIS	Read Interrupt Status	2	2	The accumulator is loaded with the interrupt status word from the highest priority I/O device currently requesting service.	I2 → I/D(8:1) A ← I/D(8:1)

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Instruction Set Summary

MNEMONIC	OCTAL OPCODE	BYTES	DESCRIPTION	REGISTER AFFECTED	FLAGS AFFECTED	CLOCK CYCLES	MEMORY REFERENCE
ACI	316	2	Add (with carry) immediate	A	All	7	2
ADC M	216	1	Add memory (with carry)	A	All	7	2
ADC s	21s	1	Add register s (with carry)	A	All	4	1
ADD M	206	1	Add memory	A	All	7	2
ADD s	20s	1	Add register s	A	All	4	1
ADI	306	2	Add immediate	A	All	7	2
AND M	246	1	And memory	A	All	7	2
AND s	24s	1	And register s	A	All	4	1
ANI	346	2	And immediate	A	All	7	2
CALL	315	3	Call (unconditional)	PC,SP	-	17	5
CC	334	3	Call on carry	PC,SP	-	11/17	3/5
CE	314	3	Call on equal (CZ)	PC,SP	-	11/17	3/5
CM	374	3	Call on minus	PC,SP	-	11/17	3/5
CMA	057	1	Complement A (ones compl.)	A	-	4	1
CMC	077	1	Complement carry	-	c	4	1
CMP M	276	1	Compare memory	-	All	7	2
CMP s	27s	1	Compare register s	-	All	4	1
CNC	324	3	Call on no carry	PC,SP	-	11/17	3/5
CNE	304	3	Call on not equal (CNZ)	PC,SP	-	11/17	3/5
CNZ	304	3	Call on not zero	PC,SP	-	11/17	3/5
CP	364	3	Call on positive	PC,SP	-	11/17	3/5
CPE	354	3	Call on parity even	PC,SP	-	11/17	3/5
CPI	376	2	Compare immediate	-	All	7	2
CPO	344	3	Call on parity odd	PC,SP	-	11/17	3/5
CZ	314	3	Call on zero	PC,SP	-	11/17	3/5
DAA	047	1	Decimal adjust	A	All	4	1
DAD B	011	1	Double add BC	HL	c	10	1
DAD D	031	1	Double add DE	HL	c	10	1
DAD H	051	1	Double add HL	HL	c	10	1
DAD SP	071	1	Double add SP	HL	c	10	1
DCR d	0d5	1	Decrement register d	d	zspx	5	1
DCR M	065	1	Decrement memory	M	zspx	10	2
DCX B	013	1	Decrement BC	BC	-	5	1
DCX D	033	1	Decrement DE	DE	-	5	1
DCX H	053	1	Decrement HL	HL	-	5	1
DCX SP	073	1	Decrement SP	SP	-	5	1
DI	363	1	Disable interrupts	-	-	4	1
EI	373	1	Enable interrupts	-	-	4	1
HLT	166	1	Halt	-	-	7	1
IN	333	2	Input	A	-	10	2
INR d	0d4	1	Increment register	d	zspx	5	1
INR M	064	1	Increment memory	M	zspx	10	3
INX B	003	1	Increment BC	BC	-	5	1
INX D	023	1	Increment DE	DE	-	5	1
INX H	043	1	Increment HL	HL	-	5	1
INX SP	063	1	Increment SP	SP	-	5	1
JC	332	3	Jump on carry	PC	-	10	3
JE	312	3	Jump on equal (JZ)	PC	-	10	3
JM	372	3	Jump on minus	PC	-	10	3
JMP	303	3	Jump (unconditional)	PC	-	10	3
JNC	322	3	Jump on no carry	PC	-	10	3
JNE	302	3	Jump on not equal (JNZ)	PC	-	10	3
JNZ	302	3	Jump on not zero	PC	-	10	3
JP	362	3	Jump on positive	PC	-	10	3
JPE	352	3	Jump on parity even	PC	-	10	3
JPO	342	3	Jump on parity odd	PC	-	10	3
JZ	312	3	Jump on zero	PC	-	10	3
LDA	072	3	Load A direct	A	-	13	4
LDAX B	012	1	Load A indirect (BC)	A	-	7	2
LDAX D	032	1	Load A indirect (DE)	A	-	7	2
LHLD	052	3	Load HL double direct	HL	-	16	5
LXI B	001	3	Load BC immediate	BC	-	10	3
LXI D	021	3	Load DE immediate	DE	-	10	3
LXI H	041	3	Load HL immediate	HL	-	10	3
LXI SP	061	3	Load SP immediate	SP	-	10	3
MOV d,M	1d6	1	Move from M to d	d	-	7	2
MOV d,s	1ds	1	Move from s to d	d	-	5	1
MOV M,s	16s	1	Move from s to M	M	-	7	2
MVI d	0d6	2	Move immediate to register	d	-	7	2
MVI M	066	2	Move immediate to memory	M	-	10	3
NOP	000	1	No operation	-	-	4	1
ORA M	266	1	Or memory	A	All	7	2
ORA s	26s	1	Or register	A	All	4	1
ORI	366	2	Or immediate	A	All	7	2
OUT	323	2	Output	A	-	10	2

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MNEMONIC	OCTAL OPCODE	BYTES	DESCRIPTION	REGISTER AFFECTED	FLAGS AFFECTED	CLOCK CYCLES	MEMORY REFERENCES
PCHL	351	1	Load PC from HL (Jump)	PC	-	5	1
POP B	3Ø1	1	Pop BC	BC,SP	-	1Ø	3
POP D	321	1	Pop DE	DE,SP	-	1Ø	3
POP H	341	1	Pop HL	HL,SP	-	1Ø	3
POP PSW	361	1	Pop PSW (A and flags)	A,SP	All	1Ø	3
PUSH B	3Ø5	1	Push BC	SP	-	11	3
PUSH D	325	1	Push DE	SP	-	11	3
PUSH H	345	1	Push HL	SP	-	11	3
PUSH PSW	365	1	Push PSW (A and flags)	SP	-	11	3
RAL	Ø27	1	Rotate A and carry left	A	c	4	1
RAR	Ø37	1	Ratate A and carry right	A	c	4	1
RC	33Ø	1	Return on carry	PC,SP	-	5/11	1/3
RE	31Ø	1	Return on equal (RZ)	PC,SP	-	5/11	1/3
RET	311	1	Return (unconditional)	PC,SP	-	1Ø	3
RLC	ØØ7	1	Rotate A left	A	c	4	1
RM	37Ø	1	Return on minus	PC,SP	-	5/11	1/3
RNC	32Ø	1	Return on no carry	PC,SP	-	5/11	1/3
RNE	3ØØ	1	Return on not equal (RNZ)	PC,SP	-	5/11	1/3
RNZ	3ØØ	1	Return on not zero	PC,SP	-	5/11	1/3
RP	36Ø	1	Return on positive	PC,SP	-	5/11	1/3
RPE	35Ø	1	Return on parity even	PC,SP	-	5/11	1/3
RPO	34Ø	1	Return on parity odd	PC,SP	-	5/11	1/3
RRC	Ø17	1	Rotate A right	A	c	4	1
RST n	3n7	1	Restart (Call)	PC,SP	-	11	3
RZ	31Ø	1	Return on zero	PC,SP	-	5/11	1/3
SBB M	236	1	Subtract M (with borrow)	A	All	7	2
SBB s	23s	1	Subtract register (w/ brw.)				
SBI	336	2	Subtract immediate (")	A	All	7	2
SHLD	Ø42	3	Store HL double direct	-	-	16	5
SHLL	Ø51	1	Shift HL left (DAD H)	HL	c	1Ø	1
SPHL	371	1	Load SP from HL	SP	-	5	1
STA	Ø62	3	Store A direct	-	-	13	4
STAX B	ØØ2	1	Store A indirect (BC)	-	-	7	2
STAX D	Ø22	1	Store A indirect (DE)	-	-	7	2
STC	Ø67	1	Set carry	-	c	4	1
SUB M	226	1	Subtract memory	A	All	7	2
SUB s	22s	1	Subtract register	A	All	4	1
SUI	326	2	Subtract immediate	A	All	7	2
XCHG	353	1	Exchange HL, DE	DEHL	-	4	1
XRA M	256	1	Exclusive or memory	A	All	7	2
XRA s	25s	1	Exclusive or register	A	All	4	1
XRI	356	2	Exclusive or immediate	A	All	7	2
XTHL	343	1	Exchange HL w/ top of stack	HL	-	18	5

INSTRUCTION SET

INDEX REGISTER INSTRUCTIONS:

Mnemonic	Instruction Code	Description
Ld s	01 DDD SSS	Load register d with the contents of register s.
Ld M	01 DDD 110	Load register d with the contents of memory.
LM s	01 110 SSS	Load memory with the contents of register s.
Ldi	00 DDD 110 BB BBB BBB	Load register d with data B----B.
LMI	00 110 110 BB BBB BBB	Load memory with data B----B.
INd	00 DDD 100	Increment the contents of register d.
DCd	00 DDD 101	Decrement the contents of register d.

INDEX REGISTER PAIR INSTRUCTIONS:

Mnemonic	Instruction Code	Description
LXI p	00 PP0 001 XX XXX XXX YY YYY YYY	Load the register pair pp with bytes 2 and 3 of the instruction. The high-order byte (3) is loaded into the first register in pair.
DE<>HL	11 101 011	Exchange the D & E registers with the H & L registers
SP<>HL	11 100 011	Exchange the H & L registers with last 2 entries in stack.
SP < HL	11 111 001	Set the H & L registers into the stack pointer.
PC < HL	11 101 001	Set the H & L registers into the program counter. Indirect Jump.
INX p	00 PP0 011	Increment register pair p.
DCX p	00 PP1 011	Decrement register pair p.
STHL	00 100 010 LL LLL LLL HH HHH HHH	Store the H & L registers in the memory location designated by bytes 2 and 3.
LDHL	00 101 010 LL LLL LLL HH HHH HHH	Load the H & L registers from the memory location designated by bytes 2 and 3.
STAX p	00 PP0 010	Store the A register in the memory location indicated by the contents of register pair p. (For p = BC & DE only.)
LDAX p	00 PP1 010	Load the A register from the memory location indicated by the contents of the register pair p. (For p = BC & DE only.)
DADX p	00 PP1 001	Add the register pair p to the H & L registers; store the result in H & L. Only carry affected (set on overflow).

PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS:

Mnemonic	Instruction Code	Description
JMP	11 000 011 LL LLL LLL HH HHH HHH	Unconditionally jump to memory address H----HL----L.
JFc	11 CC0 010 LL LLL LLL HH HHH HHH	Jump to memory address H----HL----L if flip-flop c is false. Otherwise, execute the next instruction in sequence.
JTc	11 CC1 010 LL LLL LLL HH HHH HHH	Jump to memory address H----HL----L if flip-flop c is true. Otherwise, execute the next instruction in sequence.
CAL	11 001 101 LL LLL LLL HH HHH HHH	Unconditionally call the subroutine at memory address H----HL----L. Save the current address in memory stack, decrement stack pointer by 2.
CFc	11 CC0 100 LL LLL LLL HH HHH HHH	Call the subroutine at memory address H----HL----L if the flip-flop c is false and save the current address in memory stack; decrement stack pointer by 2. Otherwise, execute next instruction in sequence.
CTc	11 CC1 100 LL LLL LLL HH HHH HHH	Call the subroutine at memory address H----HL----L if the flip-flop c is true, and save the current address in memory stack; decrement the stack pointer by 2. Otherwise, execute next instruction in sequence.
RET	11 001 001	Unconditionally return; increment stack pointer by 2.
RFc	11 CC0 000	Return if the flip-flop c is false; increment stack pointer by 2. Otherwise, execute the next instruction in sequence.
RTc	11 CC1 000	Return if the flip-flop c is true; increment stack pointer by 2. Otherwise, execute the next instruction in sequence.
RST	11 AAA 111	Call subroutine at memory address AAA000. Save current location in memory stack; decrement stack pointer by 2.
PSHX r	11 rr0 101	Store the register pair r in the memory stack; decrement stack pointer by 2.
POPX r	11 rr0 001	Load the register pair r from the memory stack; increment stack pointer by 2.

INPUT/OUTPUT INSTRUCTIONS:

Mnemonic	Instruction Code	Description
INP	11 011 011 MM MMM MMM	Read the contents of the selected input port M into the accumulator
OUT	11 010 011 MM MMM MMM	Write the contents of the accumulator into the selected output port M.

ACCUMULATOR INSTRUCTIONS:

Mnemonic	Instruction Code	Description
AD s	10 000 SSS	Add the contents of register s, memory or data B----B to the accumulator
AD M	10 000 110	An overflow sets the carry flip-flop.
ADI	11 000 110 BB BBB BBB	
AC s	10 001 SSS	Add the contents of register s, memory or data B----B to the accumu-
AC M	10 001 110	lator with carry. An overflow sets the carry flip-flop.
ACI	11 001 110 BB BBB BBB	
SU s	10 010 SSS	Subtract the contents of register s, memory or data B----B from the
SU M	10 010 110	accumulator. An underflow sets the carry flip-flop.
SUI	11 010 110 BB BBB BBB	
SB s	10 011 SSS	Subtract the contents of register s, memory or data B----B from the
SB M	10 011 110	accumulator with carry. An underflow sets the carry flip-flop.
SBI	11 011 110 BB BBB BBB	
ND s	10 100 SSS	Compute the logical AND of the contents of register s, memory or
ND M	10 100 110	data B----B with the accumulator.
NDI	11 100 110 BB BBB BBB	
XR s	10 101 SSS	Compute the EXCLUSIVE OR of the contents of register s, memory or
XR M	10 101 110	data B----B with the accumulator.
XRI	11 101 110 BB BBB BBB	
OR s	10 110 SSS	Compute the INCLUSIVE OR of the contents of register s, memory or
OR M	10 110 110	data B----B with the accumulator.
ORI	11 110 110 BB BBB BBB	
CP s	10 111 SSS	Compare the contents of register s, memory or data B----B with the
CP M	10 111 110	accumulator. Accumulator is unchanged. If equal, set zero flip-
CPI	11 111 110 BB BBB BBB	flop. If the accumulator is less than s, set carry flip-flop; if greater, clear the carry.
RLC	00 000 111	Rotate the contents of the accumulator left one bit.
RRC	00 001 111	Rotate the contents of the accumulator right one bit.
RAR	00 011 111	Rotate the contents of the accumulator right one bit through the carry.
RAL	00 010 111	Rotate the contents of the accumulator left one bit through the carry.
STA	00 110 010 LL LLL LLL HH HHH HHH	Store the A register in the memory location designated by bytes 2 and 3.
LDA	00 111 010 LL LLL LLL HH HHH HHH	Load the A register from the memory location designated by bytes 2 and 3.
DAA	00 100 111	Decimal Adjust Accumulator. Adjust the A register to contain two valid BCD digits after performing a decimal operation. All flags affected.
CMA	00 101 111	Complement the A register.

CONDITION FLAG INSTRUCTIONS:

Mnemonic	Instruction Code	Description
STC	00 110 111	Set the Carry bit.
CMC	00 111 111	Complement the Carry bit.

INTERRUPT CONTROL INSTRUCTIONS:

Mnemonic	Instruction Code	Description
EI	11 111 011	Enable Interrupts.
DI	11 110 011	Disable Interrupts.

MACHINE INSTRUCTIONS:

Mnemonic	Instruction Code	Description
HLT	01 110 110	Enter the STOPPED state and remain there until interrupted.
NOP	00 000 000	No operation.

NOTES:

1. SSS=source register
   DDD=destination register

   These registers, s and d, are designated:
   A(accumulator-111)
   B(000), C(001), D(010),
   E(011), H(100), L(101),
   M(110)

2. HH HHH HHH = high-order addr.
   LL LLL LLL = low-order addr.

3. Memory Stack Pairs:

   The memory stack pair r is designated:
   TT=00⇒BC
   TT=01⇒DE
   TT=10⇒HL
   TT=11⇒A register and condition flags (F).

   The format of F is:
   D_0=CY_2 (carry)
   D_1=1
   D_2=parity (set if even)
   D_3=0
   D_4=CY_1 (carry in DAA)
   D_5=0
   D_6=Z (zero)
   D_7=S (sign)

4. Memory is addressed by registers H (high-order address) and L (low-order address).

5. CC=flip-flop these flip-flops c are designated:
   C(carry-01), Z(zero result-00),
   S(sign-11), P(parity-10).

6. Register Pairs:
   The register pair p is designated:
   pp=00⇒BC, pp=01=DE,
   pp=10⇒HL, pp=11=stack pointer

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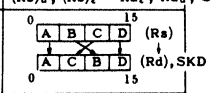
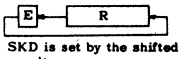
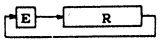
Format symbol		Instruction name	Operation	
RM	L	Load	(EA)→ Rd	
	ST	Store	(Rs)→ EA	
	B	Branch	EA → IC	
	BAL	Branch and Link	(IC) → R4 EA → IC	
	IMS	Increment Memory and Skip if Result is Zero	(EA) + 1 → EA	Only when arithmetic result of the left is "0"
	DMS	Decrement Memory and Skip if Result is Zero.	(EA)-1 → EA	(IC) + I → IC
RR	A	Add	(Rd)+(Rs)→Rd, SKD C0 → E C0 ∀ C1 → OVF	Only when the result of processing of the left matches the skip condition which is specified in SKD.
	S	Subtract	(Rd)+($\overline{Rs}$)+1→ Rd, SKD C0 → E C0 ∀ C1 → OVF	
	C	Compare	(Rd)+($\overline{Rs}$)+1 → SKD	(IC)+1→IC
	CB	Compare Byte	(Rd)ℓ+ ($\overline{Rs}$)ℓ+ 1 → SKD	
	MV	Move	(Rs) → Rd, SKD	
	MVB	Move Byte	(Rs)ℓ → Rd ℓ, SKD	
	BSWP	Byte Swap	(Rs)u, (Rs)ℓ → Rdℓ, Rdu, SKD	
	DSWP	Digit Swap		
	LAD	Load Adjust Part	When a carry is generated from each digit as a result of (Rd)+(Rs), 0110 is set at the pertinent digit of Rd and when there is no carry, 0000 is set and SKD is simultaneously set.	
	AND	And	(Rd)∧(Rs)→Rd, SKD	
	OR	Or	(Rd)∨(Rs)→Rd, SKD	
	EOR	Exclusive Or	(Rd)∀(Rs)→Rd, SKD	
RC	SL	Operate on E and Shift Left 1 Bit	The E register is operated and the below shift is performed.  SKD is set by the shifted result.	
	SR	Operate on E and Shift Right 1 Bit	E register is operated and the following shift is performed.  SKD is set by the shifted result.	Only when SKD is specified and the skip condition is satisfied by the processing of the left. (IC)+1→IC
	SBIT	Set Bit	(R)∨BP→R, SKD	
	RBIT	Reset Bit	(R)∧ $\overline{BP}$→R, SKD	
	TBIT	Test Bit	(R)∧ BP→SKD	
	AI	Add Immediate	(R)+Imm→R, SKD	
	SI	Subtract Immediate	(R)+$\overline{Imm}$+1→R, SKD	
	LPSW	Load Program Status Word	(n)→STR (n+1)→IC	
	H	Halt	CPU Stop	
	PUSH	Push the Stack	(Rs) → (SP) ↓	
	POP	Pop the Stack	(SP) ↑ → Rd	
	RET	Return	(R4) → IC	
RCM	RD	Read	(I/O) → Rd	
	WT	Write	(Rs) → I/O	
	MVI	Move Immediate	IMM → RL	

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Execute Instructions Table

Instruction name	Mnemonic code	Operand format	Remarks
Load Store	L ST	r, Exp	Exp is expressed as follows according to address modification: • Direct, relative ... Expression • Indirect, relative indirect .....(Expression) • Direct index... Expression (X0) or Expression (X1) • Indirect index...(Expression) (X0) or (Expression) (X1)
Decrement memory Branch & Link Increment Memory Branch	DMS BAL IMS B	Exp	
Byte Swap Digit Swap Move Move Byte And Load Adjust Or Exclusive Or Add Subtract Compare Compare Byte	BSWP DSWP MV MVB AND LAD OR EOR A S C CB	r,r [, Skip]	• Skip is not performed when Skip is omitted. • Register set operation is not performed when Set is omitted.
Shift Left Shift Right	SL SR	r [, Set] [, Skip]	
Push Pop	PUSH POP	r	
Halt Return	H RET	None	
Load PSW	LPSW	Exp	
Set Bit Reset Bit Test Bit Add Immediate Subtract Immediate	SBIT RBIT TBIT AI SI	r, Exp [, Skip]	
Move Immediate Read Write	MVI RD WT	r, Exp	
No Operation	NOP (*1)	None	Substituted by MV, Ro, Ro
Skip On Condition	SKIP (*1)	r [, Skip]	Substituted by MV r, r [,Skip]
Clear Register	CLEAR (*1)	r	Substituted by EOR r, r

Definition of symbols

( )..... Omission possible

r ..... Write register symbol. R0, R1, R2, R3 (or X0), R4 (X1), SP, or STR is specified.

Exp ... Write expression. Expression is decimal number, hexadecimal number, alphabet character, address assignment counter reference symbol (* entered), or symbol entered and connected by + or −.

Skip, Set.. Performs register set operation and skip conditions setting as shown in Table 3.4.

(*1) ... Extended mnemonic code.

Where

EA	Indicates the effective address
(EA)	Indicates the contents of the effective address
(SP) ↓	The data is stored at the address indicated by the contents of SP and the contents of SP are then decremented by 1
(SP) ↑	The contents of SP are incremented by 1 and the contents of the address indicated by that value are read.
CO	Carry is generated from bit 0
C1	Carry is generated from bit 1
SKD	Skip condition
Rs	Means the source register
Rd	Means the destination register
Rℓ	Indicates the low order byte (bits 8~15) of the register
Ru	Indicates the high order byte (bits 0~7) of the register
BP	Value (0~15) of bit position specification part of instruction
Imm	Value (bit 12~15) of immediate specification part of instruction
IMM	" (bit 8~15) "
I/O	Register of I/O controller
(a)	Contents of fixed address of memory corresponding to the level occupied interrupt
(n+1)	Same as (a) Level 0 n = 0 " 1 n = 2 " 2 n = 4

Operation of CPU when interrupt accepted	(STR)	→	n
	(IC)	→	n + 1
	(100 + n)	→	STR
	(101 + n)	→	IC

IS32

No.	Name	Class Instruction	Code	Mnemonic	Literal to Register Subfunctions	Operations
0	Execute	Execute	0XXX	E	NA	0X is ORed with U Register
1	Literal to Register	Literal Class Commands	10XX	LZ	Load Zero	No operation
			11XX	LT	Load T	XX replace contents of T
			12XX	LM	Load M	XX replace contents of M
			13XX	LN	Load N	XX replace N & M is cleared.
			14XX	JP	Jump	to page 0.
			15XX	JP	Jump	to page 1.
			1CXX	JP	Jump	to page 2.
			1DXX	JP	Jump	to page 3.
			16XX	LU	Load U	XX replaces contents of U.
			17XX	LS	Load Seven	Internal Controls
2	Load File		2fXX	LF	N/A	f = file number
3	Add to File		3fXX	AF	N/A	f = file number
4	Test If Zero		4fXX	TZ	N/A	Skip on no bits match, if file f of the ones in the XX.
5	Test Not Zero		5fXX	TN	N/A	Skip on any bits match in file f of the ones in X.
6	Compare		6fXX	CP	N/A	Skip on f + XX>2^8 -1
						c Field (Binary)
7	Control	Operate Class Commands (C field)	7fc*r	K (destination T,M,N,L,U)	N/A	0000 No operation 0001 Enter Sense Switches 0010 Shift Right Four Bits 0100 Enter Internal Status 0111 Enter Console Switches 1000 Clear I/O Mode 1001 Control Output 1010 Data Output 1011 Space Serial TTY

No.	Name	Class Instruction	Code	Mnemonic	Literal to Register Subfunctions	C field (binary)
7	Control	Operate Class Commands	7fc*r		N/A	1100 Concurrent Acknowledge 1101 Interrupt Acknowledge 1110 Data Input 1111 Spare
8	Add		8fc*r	A	N/A	0001 Modify Flags 0010 File + T 0100 Sum + 1 1000 Sum + Link Bit
9	Subtract		9fc*r	S	N/A	0001 Modify Flags 0010 File + T Complement 0100 Inhibit Increment 1000 Difference + Line
10	Read/Write Memory		Afc*r	R/S	N/A	00XX Transfer 01XX Decrement 10XX Add Link 11XX Increment XX1X Half Cycle XXX1 Write (Not Read)
11	Copy		Bfc*r	C	N/A	XXX1 Modify Flags XX1X Select T X1XX Select + 1 1XXX Select Link
12	OR		Cfc*r	O	N/A	XXX1 Modify Flags XX1X Select T X1XX Select T Complement 1XXX Linked Zero Test

No.	Name		Code	Mnemonic	Literal to Register Subfunctions	C field (binary)
13	Exclusive OR		Dfc*r	X		Same as OR
14	AND		Efc*r	N		Same as OR
15	Shift		Ffc*r	H		XXX1 Modify Flags XX1X Shift Right X1XX Insert ONE 1XXX Insert Link

NOTE: If* = 0, result of operation is placed in file (f).

① f = file address

② c = sub op code field

③ * = inhibit file write

④ r = destination field

NOTES TO THE INSTRUCTION SET

Register-to-Register Operations - These orders facilitate functional operations between any selected pair of file registers (R_i, R_j). The result is placed back into (R_i), except for Compare which does not alter any register. The entire file is immediately addressable.

Literal Operations - These orders use the immediate 8-bit literal (L) field of an instruction word for operation on a file register. The file is "paged" into eight word blocks for these operations.

BCD Operations - Each file register is configured to hold two 4-bit decimal numbers. BCD functions may be performed on either the left or right fields (L, R). The file is paged into eight word blocks for BCD op's.

Bit Operations - The entire general file is immediately addressable to the bit level (B_j).

Register Operations & Shifts - The entire file is immediately addressable. N = 1 to 8.

Execute - This powerful instructions allows the programmer to construct a machine instruction in the file and then "execute" it.

■Multi-precision Orders

*Indexable Address provide by file (R_j)

▲I/O operation rate may be controlled by the peripheral (for slow devices).

⊙Shift rate controllable by peripheral (maximum rate = 120 n/sec per bit).

●Flags - Page bits (2), Carry, Interrupt Block.

Register-to-Register Operations (R_i, R_j)

ADD, SUBTRACT, AND, OR, EXCLUSIVE-OR, ADD w/CS■, SUBTRACT w/CS■	480 n/sec
COMPARE & Skip 3-Ways (>, =, <)	600 n/sec
MOVE ($R_j \rightarrow R_i$)	480 n/sec

Literal-Register Operations (L, R_i)

ADD, SUBTRACT, AND, OR, EXCLUSIVE-OR	360 n/sec
COMPARE & Skip 3-Ways (>, =, <)	480 n/sec
MOVE (L → R_i)	360 n/sec

Register Operations (R_i)

LOAD ZERO, LOGIC INVERT, TWO'S COMPLEMENT	360 n/sec
INCREMENT & Skip =0 (≠ 0) DECREMENT & Skip=0 (≠ 0)	480 n/sec
SENSE PARITY & Skip Odd (E)	480 n/sec

BCD Arithmetic (Left or Right Field) (LR_i, LR_j) or (RR_i, RR_j)

LOAD ZERO, SWAP L↔R Field	360 n/sec
ADD, SUBTRACT	480 n/sec
ADD w/CS & Skip $\overline{CG}$ ■ SUBTRACT w/CS & Skip CG■	600 n/sec
ADD· SUBTRACT CORRECT	360 n/sec
MOVE ($LR_j \rightarrow LR_i$) or ($RR_i \rightarrow RR_j$)	480 n/sec

Bit Operations (B_j of 8-bit field R_i)

SET, RESET, INVERT	360 n/sec
SENSE & Skip TRUE (FALSE)	480 n/sec

Transfers & Sub-Routine Linkage

JUMP UNCONDITIONAL JUMP & LINK	360 n/sec
RETURN from LINK	480 n/sec

Register Shifts (R_i, N places)

CIRCULAR LEFT or RIGHT LOGIC LEFT or RIGHT ARITHMETIC LEFT or RIGHT	360+120N n/sec

Status & Special Instructions

LOAD STATUS, STORE STATUS SET/RESET STATUS FLAG ●	360 n/sec
EXECUTE FILE REGISTERS	360+I n/sec
SENSE CARRY & Skip True (F)	480 n/sec

Input/Output Orders▲

INPUT device (R_j) to File R_i OUTPUT File R_i to device (R_j)	600 n/sec 600 n/sec
INPUT device (L) to File R_i OUPTUT File R_i to device (L)	480 n/sec 480 n/sec
SET/RESET EXTERNAL dev (R_j)* SET/RESET EXTERNAL dev (L)	480 n/sec 480 n/sec
SENSE EXTERNAL (R_j)*Skip T(F) SENSE EXTERNAL (L) Skip T (F)	600 n/sec 600 n/sec
SERIAL INPUT/OUTPUT ⊙	360+120N

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS36

		MNEMONICS	OPERATION	MICROCYCLES Dir.	Indr.	Imm.	Stack	COMMENTS
External Reference Instructions	Arithmetic & Logic	ADD	ADD	10	8	8	11	
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	Result not saved
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	
	I/O	MVO	MoVe Out	10	8	8	11	
		MVI	MoVe In	10	8	8	11	
Internal Register Instructions	Register to Register	ADDR	ADD contents of Registers	6				Add one cycle
		SUBR	SUBtract contents of Register	6				if Register 6 or 7
		CMPR	CoMPare Registers by subtr.	6				Result not saved
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		MOVR	MOVe Register	6				
	Single Register	CLRR	CLeaR Register	6				XORR with itself, except*
		TSTR	TeST Register	6				
		JR	Jump to address in Register	7*				PC ← (RRR)
		INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				Two Words
		SIN	Software INterrupt	6				Pulse to PCIT pin
		RSWD	Return Status WorD	6				
		PULR	PULl from stack to Register	11*				PULR = MVI@R6
		PSHR	PuSH Register to stack	9*				PSHR = MVO@R6
	Register Shift	SLL	Shift Logical Left	6				one or two position shift capability. Add two cycles for 2-position shift
		RLC	Rotate Left thru Carry	6				
		SLLC	Shift Logical Left thru Carry	6				
		SLR	Shift Logical Right	6				
		SAR	Shift Arithmetic Right	6				
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				
		SWAP	SWAP 8-bit bytes	6				2-position=SWAP twice
Control Instructions		HLT	HaLT	4				
		SDBD	Set Double Byte Data	4				Must precede external reference to double byte data
		EIS	Enable Interrupt System	4				
		DIS	Disable Interrupt System	4				
		TCI	Terminate Current Interrupt	4				Not Interruptible
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
Jump Instructions		J	Jump	12				
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				Return Address saved in R4, 5 or 6
		JSRE	Jump, Save Return & Enable	12				
		JSRD	Jump, Save Return & Disable Interrupt	12				
Conditional Branch Instructions		B	unconditional Branch	7				Displacement in PC+1
		BC, BLGE	Branch on Carry, C=1	7				PC ← PC ± Displacement
		BNC, BLLT	Branch on No Carry, C=0	7				Add 2 cycles if test condition
		BOV	Branch on OVerflow, OV=0	7				is true.
		BNOV	Branch on No OVerflow, OV=0	7				
		BPL	Branch on PLus, S=0	7				
		BMI	Branch on MInus, S=1	7				
		BZE, BEQ	Branch on ZEro or EQual	7				Z=1
		BNZE, BNEQ	Branch if Not ZEro or Not EQual	7				Z=0
		BLT	Branch if Less Than	7				S∀OV=1
		BGE	Branch if Greater than or Equal	7				S∀OV=0
		BLE	Branch if Less than or Equal	7				Z ∨ (S∀OV)=1
		BGT	Branch if Greater Than	7				Z ∨ (S∀OV)=0
		BUSC	Branch if Sign ≠ Carry	7				C ∀ S=1
		BESC	Branch if Sign = Carry	7				C ∀ S=0
		BEXT	Branch if External condition is True	7				4 LSB of Instruction are decoded to select 1 of 16 external conditions.

1 MICROCYCLE = 2 CLOCK CYCLES

COSMAC Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer

N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high byte)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip Flop

INSTRUCTION SET

The COSMAC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)
N0 = Least significant Bit of N Register

Operation Notation
M(R(N)) →D; R(N) + 1

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

INSTRUCTION SUMMARY

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D; R(N) +1
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X) +1
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P) +1
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X) −1
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) +1
DECREMENT REG N	DEC	2N	R(N) −1
INCREMENT REG X	IRX	60	R(X) +1
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1
LOGIC OPERATIONS◆◆			
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P) +1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P) +1
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P) +1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76◆	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E◆	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL		

◆NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.
◆◆NOTE: THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.
AFTER AN ADD INSTRUCTION:
DF = 1 DENOTES A CARRY HAS OCCURRED
DF = 0 DENOTES A CARRY HAS NOT OCCURRED
AFTER A SUBTRACT INSTRUCTION:
DF = 1 DENOTES NO BORROW, D IS A TRUE POSITIVE NUMBER
DF = 0 DENOTES A BORROW, D IS TWO'S COMPLEMENT
THE SYNTAX "−(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS◆◆			
ADD	ADD	F4	M(R(X)) +D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) +D→DF, D; R(P) +1
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) +D +DF→DF, D R(P) +1
SUBTRACT D	SD	F5	M(R(X))−D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))−D→DF, D; R(P) +1
SUBTRACT D WITH BORROW	SDB	75	M(R(X))−D−(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))−D−(NOT DF)→DF, D; R(P) +1
SUBTRACT MEMORY	SM	F7	D−M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D−M(R(P))→DF, D; R(P) +1
SUBTRACT MEMORY WITH BORROW	SMB	77	D−M(R(X))−(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D−M(R(P))−(NOT DF)→DF, D R(P) +1
BRANCH INSTRUCTIONS–SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38◆	R(P) +1
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF DF=1	BDF	33◆	IF DF=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B◆	IF DF=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=1	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=0	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=1	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=0	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=1	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=0	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=1	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=0	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P) +1

◆NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.
◆◆NOTE: THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.
AFTER AN ADD INSTRUCTION:
DF = 1 DENOTES A CARRY HAS OCCURRED
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AFTER A SUBTRACT INSTRUCTION:
DF = 1 DENOTES NO BORROW, D IS A TRUE POSITIVE NUMBER
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THE SYNTAX "−(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

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Notations/Symbols Used in Instruction Descriptions

Notation/ Symbol	Meaning
ACr	Denotes specific working accumulator (AC0, AC1, AC2, or AC3), where *r* is number of accumulator referenced in instruction.
cc	Denotes 4-bit condition code value for conditional branch instructions.
CRY	Indicates Carry Flag is set if carry exists due to instruction (either addition or subtraction) or reset if no carry exists.
disp	Stands for displacement value and represents operand in non-memory-reference instruction or address field in memory-reference instruction. Disp is 8-bit, signed twos-complement number except when base page is referenced; in latter case, disp is unsigned if BPS=0.
dr	Denotes number of destination working accumulator specified in instruction-word field. Working accumulator is AC0, AC1, AC2, or AC3.
EA	Denotes effective address specified by instructions directly, indirectly, or by indexing. Effective address contents are used during execution of instruction.
fc	Denotes number of referenced flag.
FR	Denotes Status and Control Flags Register.
IEN	Denotes Interrupt Enable Flag.
ℓ	Denotes inclusion of 1-bit Link Flag (LINK) in shift operations.
n	Unsigned number indicates number of bit positions to be shifted in Shift and Rotate Instructions.
OVF	Indicates Overflow Flag is set if overflow exists due to instruction (either addition or subtraction) or is reset if no overflow exists. Overflow occurs if signs of operands are alike and sign of result is different from operands.
PC	Denotes Program Counter. During address formation, PC is incremented by 1 to contain address 1 greater than that of instruction being executed.
r	Denotes number of working accumulator specified in instruction-word field. Working accumulator is AC0, AC1, AC2, or AC3.
STK	Denotes top word of 10-word Last-In/First-Out Stack.
sr	Denotes number of source working accumulator specified in instruction-word field. Working accumulator is AC0, AC1, AC2, or AC3.
xr	When not zero, xr value designates number of accumulator to be used in indexed and relative-memory addressing modes. When zero, base-page addressing is indicated.
( )	Denotes contents of item within parentheses. (ACr) is read as *contents of ACr*. (EA) is read as *contents of EA*.
[ ]	Denotes *result of*.
~	Indicates logical complement (ones complement) of value on right-hand side of ~.
→	Means *replaces*.
←	Means *is replaced by*.

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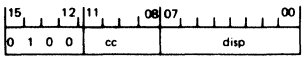
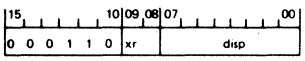
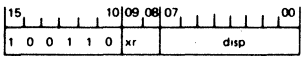
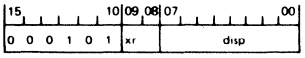
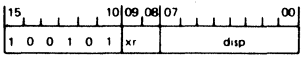
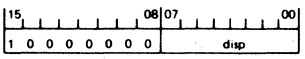
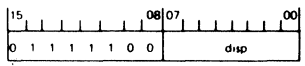
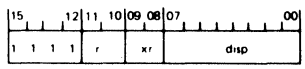
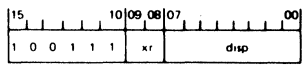
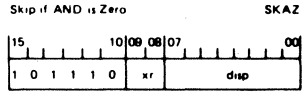
IS40 Cont'd

Notations/Symbols Used in Instruction Descriptions (Continued)

Notation/ Symbol	Meaning
@	Appearing in operand field of instruction, denotes indirect addressing.
+10	Modulo 10 addition.
∧	Denotes AND operation.
∨	Denotes OR operation.
∇	Denotes EXCLUSIVE OR operation.

PACE Instruction Summary

Instruction/Mnemonic	Operation/Description	Assembler Format	Execution Time/Cycles (M)
BRANCH INSTRUCTIONS			
Branch-On Condition BOC 	(PC)←(PC) + disp if cc true 16 possible condition codes (cc) exist. Condition codes are listed in table B-3. If condition for branching designated by cc is true, value of disp (sign extended from bit 7 through bit 15) is added to PC and sum is stored in PC.	BOC cc, disp	5M + E_R + 1M if branch
Jump JMP 	(PC)←EA Effective address EA replaces PC contents. Next instruction is fetched from location designated by new contents of PC.	JMP disp (xr)	4M + E_R
Jump Indirect JMP@ 	(PC)←(EA) Contents of effective address replace PC contents. Next instruction is fetched from location designated by new contents of PC.	JMP @disp (xr)	4M + 2E_R
Jump to Subroutine JSR 	(STK)←(PC), (PC)← EA Contents of PC are stored on top of Stack. Effective address replaces PC contents. Next instruction is fetched from location designated by new contents of PC.	JSR disp (xr)	5M + E_R
Jump to Subroutine Indirect JSR@ 	(STK)←(PC), (PC)← (EA) Contents of PC are stored on top of Stack. Contents of effective address replace PC contents. Next instruction is fetched from location designated by new contents of PC.	JSR @disp (xr)	5M + 2E_R
Return from Subroutine RTS 	(PC)← (STK) + disp Contents of PC are replaced by sum of disp added to contents pulled from top of Stack. Program control is transferred to location specified by new contents of PC.	RTS disp	5M + E_R
Return from Interrupt RTI 	(PC)←(STK) + disp, IEN = 1 Interrupt Enable Flag (IEN) is set. PC contents are replaced by sum of disp and word pulled from top of Stack. Program control is transferred to location specified by new contents of PC	RTI disp	6M + E_R
SKIP INSTRUCTIONS			
Skip if Not Equal SKNE 	If (ACr) ≠ (EA), (PC)←(PC) + 1 ACr contents and contents of effective memory location EA are compared. If contents of ACr and EA are not equal, next instruction in sequence is skipped. Contents of ACr and EA are unaltered. If 8-bit data length is selected, only lower 8 bits are compared	SKNE r, disp (xr)	5M + 2E_R + 1M if skip
Skip if Greater SKG 	If (AC0) > (EA), (PC)← (PC) + 1 AC0 contents and contents of effective memory location EA are compared as signed numbers. If contents of AC0 are greater (more positive) than contents of EA, next instruction in sequence is skipped. Contents of AC0 and EA are unaltered. If 8-bit data length is selected, only lower 8 bits are compared	SKG 0, disp (xr)	7M + 2E_R + 1M if skip
Skip if AND is Zero SKAZ 	If ((AC0) ∧ (EA)) = 0, (PC)← (PC) + 1 AC0 contents and contents of effective memory location EA are ANDed. If result equals zero, next instruction in sequence is skipped. Contents of AC0 and EA are unaltered. If 8-bit data length is selected, only lower 8 bits are tested.	SKAZ 0, disp (xr)	5M + 2E_R + 1M if skip

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IS38 Cont'd

INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS–LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P) +1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8♦	R(P) +2
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=0	LBNF	C8	IF DF=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38♦	R(P) +1
LONG SKIP (SEE NLBR)	LSKP	C8♦	R(P) +2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2 ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)–1
RETURN	RET	70	M(R(X))→(X,P); R(X) +1 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X) +1 0→IE

#An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

♦NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
INPUT–OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) +1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) +1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) +1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) +1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) +1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) +1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) +1; N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch.

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

   The short-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test the status (1 or 0) of the four EF flags
   f) Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch with the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch.

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

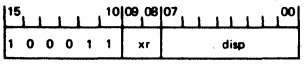
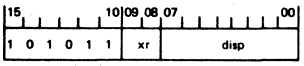
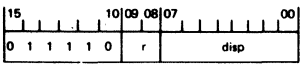
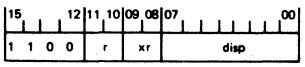
   They can:
   a) Skip unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test for IE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

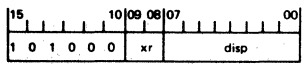
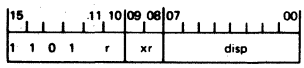
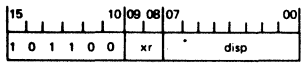
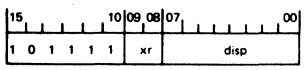
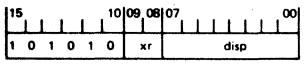
IS40 Cont'd

IS40 Cont'd

PACE Instruction Summary (Continued)

Instruction/Mnemonic	Operation/Description	Assembler Format	Execution Time/Cycles (M)
SKIP INSTRUCTIONS (Continued)			
Increment and Skip if Zero ISZ 	(EA)←(EA) + 1, if (EA) = 0, (PC)←(PC) + 1 EA contents are incremented by 1. If new contents of EA equal zero, next instruction in sequence is skipped. If 8-bit data length is selected, only lower 8 bits are tested.	ISZ disp (xr)	$7M + 2E_R + E_W + 1M$ if skip
Decrement and Skip if Zero DSZ 	(EA)←(EA) - 1, if (EA) = 0, (PC)←(PC) + 1 EA contents are decremented by 1. If new contents of EA equal zero, next instruction in sequence is skipped. If 8-bit data length is selected, only lower 8 bits are tested.	DSZ disp (xr)	$7M + 2E_R + E_W + 1M$ if skip
Add Immediate, Skip if Zero AISZ 	(ACr)←(ACr) + disp, if (ACr) = 0, (PC)←(PC) + 1 ACr contents are replaced by sum of contents of ACr and disp (sign bit 7 extended through bit 15). Initial contents of ACr are lost. If new contents of ACr equal zero, contents of PC are incremented by 1, thus skipping next instruction. AISZ Instruction always tests full 16-bit result independent of data length selected.	AISZ r, disp	$5M + E_R + 1M$ if skip
MEMORY DATA-TRANSFER INSTRUCTIONS			
Load LD 	(ACr) ← (EA) ACr contents are replaced by EA contents. Initial contents of ACr are lost; contents of EA are unaltered.	LD r, disp (xr)	$4M + 2E_R$

PACE Instruction Summary (Continued)

Instruction/Mnemonic	Operation/Description	Assembler Format	Execution Time/Cycles (M)
MEMORY DATA-TRANSFER INSTRUCTIONS (Continued)			
Load Indirect LD@ 	(AC0)←((EA)) AC0 contents are replaced indirectly by EA contents. Initial contents of AC0 are lost; contents of EA and location designating EA are unaltered.	LD 0, @disp (xr)	$5M + 3E_R$
Store ST 	(EA)←(ACr) EA contents are replaced by contents of ACr. Initial contents of EA are lost; contents of ACr are unaltered.	ST r, disp (xr)	$4M + E_R + E_W$
Store Indirect ST@ 	((EA))←(AC0) EA contents are replaced indirectly by AC0 contents. Initial contents of EA are lost; contents of AC0 and location designating EA are unaltered.	ST 0, @disp (xr)	$4M + 2E_R + E_W$
Load with Sign Extended LSEX 	(AC0)←(EA) bit 7 extended AC0 contents are replaced by EA contents with bit 7 extended through bits 8-15. Initial contents of AC0 are lost; contents of EA are unaltered. LSEX permits 8-bit data loading from memory or peripheral to be operated on as 16-bit data.	LSEX 0, disp (xr)	$4M + 2E_R$
MEMORY DATA-OPERATE INSTRUCTIONS			
AND AND 	(AC0)←(AC0) ∧ (EA) AC0 contents and EA contents are ANDed. Result is stored in AC0. Initial contents of AC0 are lost; contents of EA are unaltered.	AND 0, disp (xr)	$4M + 2E_R$

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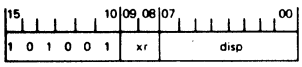
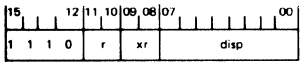
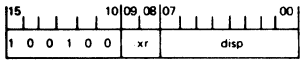
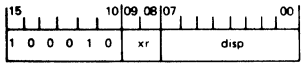
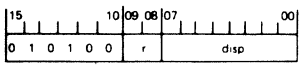
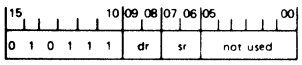
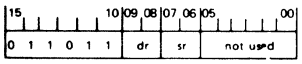
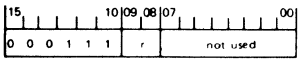
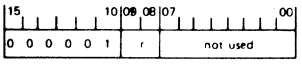
PACE Instruction Summary (Continued)

Instruction/Mnemonic	Operation/Description	Assembler Format	Execution Time/Cycles (M)
MEMORY DATA-OPERATE INSTRUCTIONS (Continued)			
OR OR 	(AC0) ← (AC0) ∨ (EA) AC0 contents and EA contents are ORed inclusively. Result in stored in AC0. Initial contents of AC0 are lost; contents of EA are unaltered.	OR 0, disp (xr)	$4M + 2E_R$
Add ADD 	(ACr) ← (ACr) + (EA), OV, CY ACr contents are added algebraically to EA contents. Sum is stored in ACr, and contents of EA are unaltered. Initial contents of ACr are lost. Overflow or Carry Flag is set if overflow or carry occurs, respectively; otherwise Overflow and Carry Flags are cleared.	ADD r, disp (xr)	$4M + 2E_R$
Subtract with Borrow SUBB 	(AC0) ← (AC0) + ~(EA) + (CY), OV, CY AC0 contents are added to complement of EA and carry. Result is stored in AC0 and contents of EA are unaltered. Initial contents of AC0 are lost. Carry and Overflow Flags are set according to result of operation.	SUBB 0, disp (xr)	$4M + 2E_R$
Decimal Add DECA 	(AC0) ← (AC0) $+_{10}$ (EA) $+_{10}$ (CY), OV, CY AC0 contents are treated as 4-digit number and added modulo 10 (for each digit) to contents of EA (treated as 4-digit number) and carry. Initial contents of AC0 are lost; contents of EA are unaltered. Carry Flag is set based on decimal carry output. Overflow Flag is set to arbitrary state.	DECA 0, disp (xr)	$7M + 2E_R$

PACE Instruction Summary (Continued)

Instruction/Mnemonic	Operation/Description	Assembler Format	Execution Time/Cycles (M)
REGISTER DATA-TRANSFER INSTRUCTIONS			
Load Immediate LI 	(ACr) ← disp ACr contents are replaced by disp with sign bit 7 extended through bit 15. Initial contents of ACr are lost.	LI r, disp	$4M + E_R$
Register Copy RCPY 	(ACdr) ← (ACsr) Destination Register ACdr contents are replaced by contents of Source Register ACsr. Initial contents of ACdr are lost and initial contents of ACsr are unaltered.	RCPY sr, dr	$4M + E_R$
Register Exchange RXCH 	(ACdr) ↔ (ACsr), (ACsr) ↔ (ACdr) ACsr contents and ACdr contents are exchanged	RXCH sr, dr	$6M + E_R$
Exchange Register and Stack XCHRS 	(STK) ↔ (ACr), (ACr) ↔ (STK) Contents of top of Stack and accumulator designated by ACr are exchanged	XCHRS	$6M + E_R$
Copy Flags into Register CFR 	(ACr) ← (FR) ACr contents are replaced by contents of FR. Initial contents of ACr are lost, contents of FR are unaltered.	CFR	$4M + E_R$

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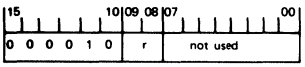
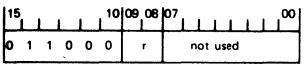
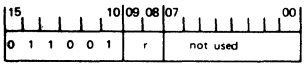
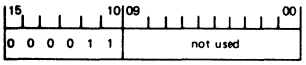
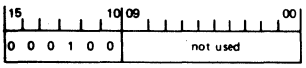
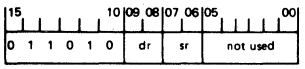
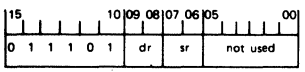
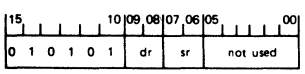
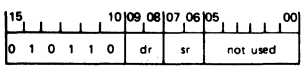
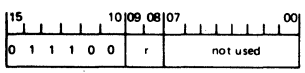
PACE Instruction Summary (Continued)

Instruction/Mnemonic	Operation/Description	Assembler Format	Execution Time/Cycles (M)
REGISTER DATA-TRANSFER INSTRUCTIONS (Continued)			
Copy Register into Flags CRF 	(FR)←(ACr) FR contents are replaced by ACr contents. Initial contents of FR are lost; contents of ACr are unaltered.	CRF r	$4M + E_R$
Push Register onto Stack PUSH 	(STK)←(ACr) Stack is pushed by contents of accumulator designated by ACr. Thus, top of Stack holds ACr contents and Stack Pointer is incremented by 1. Initial contents of ACr are unaltered.	PUSH r	$4M + E_R$
Pull Stack into Register PULL 	(ACr)←(STK) Stack is pulled. Contents from top of Stack replace ACr contents. Initial contents of ACr are lost. Contents of Stack Pointer are decremented by 1.	PULL r	$4M + E_R$
Push Flags onto Stack PUSHF 	(STK)←(FR) FR contents are pushed onto Stack. Contents of FR are unchanged.	PUSHF	$4M + E_R$
Pull Stack into Flags PULLF 	(FR)←(STK) FR contents are replaced by contents pulled from top of Stack. Initial contents of FR are lost.	PULLF	$4M + E_R$

PACE Instruction Summary (Continued)

Instruction/Mnemonic	Operation/Description	Assembler Format	Execution Time/Cycles (M)
REGISTER DATA-OPERATE INSTRUCTIONS			
Register Add RADD 	(ACdr)←(ACdr) + (ACsr), OV, CY ACdr contents are replaced by sum of contents of ACdr and ACsr. Initial contents of ACdr are lost and contents of ACsr are unaltered. Overflow and Carry Flags are modified according to result.	RADD sr, dr	$4M + E_R$
Register Add with Carry RADC 	(ACdr)←(ACdr) + (ACsr) + (CY), OV, CY ACdr contents are replaced by sum of ACdr and ACsr contents and carry. Initial ACdr contents are lost and ACsr contents are unaltered. Overflow and Carry Flags are modified according to result.	RADC sr, dr	$4M + E_R$
Register AND RAND 	(ACdr)←(ACdr) ∧ (ACsr) ACdr contents are replaced by result of ANDing ACdr and ACsr contents. Initial contents of ACdr are lost and initial contents of ACsr are unaltered.	RAND sr, dr	$4M + E_R$
Register EXCLUSIVE OR RXOR 	(ACdr)←(ACdr) ∨ (ACsr) ACdr contents are replaced by result of EXCLUSIVEly ORing ACdr contents and ACsr contents. Initial contents of ACdr are lost and initial contents of ACsr are unaltered.	RXOR sr, dr	$4M + E_R$
Complement and Add Immediate CAI 	(ACr)←~(ACr) + disp ACr contents are replaced by sum of complement of ACr and disp (sign bit 7 extended through bit 15). Initial contents of ACr are lost. Values of 0 and 1 in disp field produce ones and twos, complement, respectively, of (ACr).	CAI r, disp	$5M + E_R$

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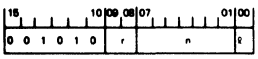
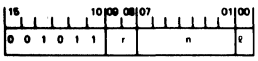
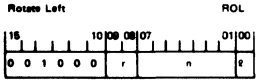
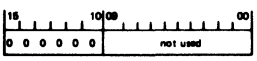
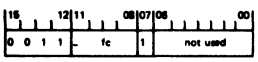
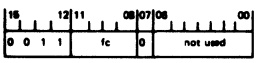
PACE Instruction Summary (Continued)

Instruction/Mnemonic	Operation/Description	Assembler Format	Execution Time/Cycles (M)
SHIFT AND ROTATE INSTRUCTIONS			
Shift Left SHL 	(ACr)←(ACr) shifted left n places, w/wo link ACr contents are shifted left n (n = 0-127) bit positions. If selected data length is 8 bits, then bits 8-15 are set to zero. Data shifted out of most significant bit for specified data length are lost if ℓ = 0 and are loaded into LINK if ℓ = 1.	SHL r, n, ℓ	(5 + 3n) M + E_R, n = 1-127; 6M + E_R, n = 0
Shift Right SHR 	(ACr)←(ACr) shifted right n places, w/wo link ACr contents are shifted right n (n = 0-127) bit positions. If selected data length is 8 bits, then bits 8-15 are set to zero. Zeros are shifted into most significant bit for specified data length if ℓ = 0. Contents of LINK are shifted in if ℓ = 1, and contents of LINK are unchanged. Data shifted out of least significant bit are lost.	SHR r, n, ℓ	(5 + 3n) M + E_R, n = 1-127; 6M + E_R, n = 0
Rotate Left ROL 	(ACr)←(ACr) rotated left n places, w/wo link ACr contents are rotated left n (n = 0-127) bit positions. If selected data length is 8 bits, then bits 8-15 are set to zero. Data shifted out of most significant bit position for specified data length are shifted into least significant bit if ℓ = 0, and into LINK if ℓ = 1, in which case least significant bit is loaded from LINK.	ROL r, n, ℓ	(5 + 3n) M + E_R, n = 1-127; 6M + E_R, n = 0
Rotate Right ROR 	(ACr)←(ACr) rotated right n places, w/wo link ACr contents are rotated right n (n = 0-127) bit positions. If selected data length is 8 bits, then bits 8-15 are set to zero. Data shifted out of least significant bit are shifted into most significant bit for specified data length if ℓ = 0, and into LINK if ℓ = 1, in which case most significant bit is loaded from LINK.	ROR r, n, ℓ	(5 + 3n) M + E_R, n = 1-127; 6M + E_R, n = 0

PACE Instruction Summary (Continued)

Instruction/Mnemonic	Operation/Description	Assembler Format	Execution Time/Cycles (M)
MISCELLANEOUS INSTRUCTIONS			
Halt HALT 	Halt Microprocessor halts and remains halted until CONTIN Input to Jump Condition Multiplexer makes transition from logic '1' to logic '0'.	HALT	- - - - - -
Set Flag SFLG 	$(FR)_{fc}$←1 Flag, or bit of FR, specified by flag code fc is set true. All other bits of FR are unaltered.	SFLG fc	5M + E_R
Pulse Flag PFLG 	$(FR)_{fc}$←1, $(FR)_{fc}$←0 Flag (bit fc of FR) is first set true and then set false (after four clock periods), causing pulsing or resetting of flag, depending on initial state of flag. All other bits of FR are unaffected.	PFLG fc	6M + E_R

Branch Conditions

Condition Code (cc)	Mnemonic	Condition
0000	STFL	Stack Full (contains nine or more words).
0001	REQ0	(AC0) equal to zero (see note 1).
0010	PSIGN	(AC0) has positive sign (see note 2).
0011	BIT0	Bit 0 of AC0 true.
0100	BIT1	Bit 1 of AC0 true.
0101	NREQ0	(AC0) is nonzero (see note 1).
0110	BIT2	Bit 2 of AC0 is true.
0111	CONTIN	CONTIN (continue) Input is true.
1000	LINK	LINK is true.
1001	IEN	IEN is true.
1010	CARRY	CARRY is true.
1011	NSIGN	(AC0) has negative sign (see note 2).
1100	OVF	OVF is true.
1101	JC13	JC13 Input is true (see note 3).
1110	JC14	JC14 Input is true.
1111	JC15	JC15 Input is true.

NOTES:
1. If selected data length is 8 bits, only bits 0 through 7 of AC0 are tested.
2. Bit 7 is sign bit (instead of bit 15) if selected data length is 8 bits.
3. JC13 is used by PACE Microprocessor Development System and is not accessible during prototyping.

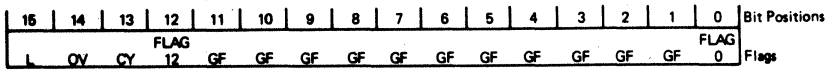
IS42

Basic Instruction Set

Instruction	Mnemonic	Execution Cycles
Memory Reference Instructions		
Load	LD	5
Load Indirect[a]	LD	5
Store	ST	6
Store Indirect[a]	ST	8
Add	ADD	5
Subtract	SUB	5
Jump	JMP	3
Jump Indirect[a]	JMP	5
Jump to Subroutine	JSR	4
Jump to Subroutine Indirect[a]	JSR	6
Increment and Skip if Zero	ISZ	7,8 if SKIP
Decrement and Skip if Zero	DSZ	8,9 if SKIP
Skip if AND is Zero	SKAZ	6,7 if SKIP
Skip if Greater	SKG	Like Signs: 8,9 if SKIP Unlike Signs: 9,10 if SKIP
Skip if Not Equal	SKNE	6
And	AND	5
Or	OR	5
Register Reference Instructions		
Push on to Stack Register	PUSH	3
Pull from Stack	PULL	3
Add Immediate, Skip if Zero	AISZ	4,5 if SKIP
Load Immediate	LI	3
Complement and Add Immediate	CAI	3
Register Copy	RCPY	6
Exchange Register and Top of Stack	XCHRS	5
Exchange Registers	RXCH	8
Register And	RAND	6
Register Exclusive Or	RXOR	6
Register Add	RADD	3
Shift Left	SHL	4 + 3k[b]
Shift Right	SHR	4 + 3k
Rotate Left	ROL	4 + 3k
Rotate Right	ROR	4 + 3k
Input/Output, Flag, and Halt Instructions		
Set Flag	SFLG	4
Pulse Flag	PFLG	4
Push Flags on Stack	PUSHF	4
Pull Flags from Stack	PULLF	5
Register In	RIN	7
Register Out	ROUT	7
Halt	HALT	–
Transfer of Control Instructions		
Branch-On Condition	BOC	4,5 if branch
Return from Subroutine	RTS	4
Return from Interrupt	RTI	5
Jump to Subroutine Implied	JSRI	4

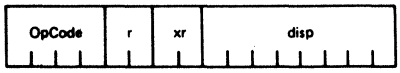
a - The symbol @ must precede the designation of the memory location whose contents become the effective address by indirection.

b - "k" equals the number of bits shifted.

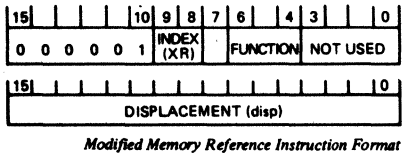


Bit Position	Flag Name	Mnemonic	Significance
15	Link	L	Used for double-word shifts
14	Overflow	OV	Set if an arithmetic overflow occurs
13	Carry	CY	Set if a carry occurs (from most significant bit) during an arithmetic operation
12 through 0	General-Purpose Flags	GF	Use specified by user (Status flags 0 and 12 are externally available)

CPU Status Flag Assignments



Format for Basic Memory Reference Instructions



Modified Memory Reference Instruction Format

EXTENDED INSTRUCTION SET

Instruction	Mnemonic	Execution Cycles
Multiply	MPY	106 to 122
Divide	DIV	125 to 159
Double Precision Add	DADD	12
Double Precision Subtract	DSUB	12
Load Byte	LDB	20 (left) 12 (right)
Store Byte	STB	24 (left) 17 (right)
Set Status Flag	SETST	17 to 36
Clear Status Flag	CLRST	17 to 36
Skip if Status Flag True	SKSTF	19 to 39
Set Bit	SETBIT	15 to 34
Clear Bit	CLRBIT	15 to 34
Complement Bit	CMPBIT	15 to 34
Skip if Bit True	SKBIT	19 to 39
Interrupt Scan	ISCAN	9 to 80
Jump Indirect to Level Zero Interrupt	JINT	7
Jump Through Pointer	JMPP	7
Jump to Subroutine Through Pointer	JSRP	8

MNEMONICS		OPERATION	CYCLES
	LAR	Load Accumulator from Register	1
	SAR	Store Accumulator in Register	1
	DEC	Decrement Register by one *	1
	ADR	BCD Add Accumulator with Register *	2
	BAD	Binary Add Accumulator with Register *	1
	AND	Logical AND Accumulator with Register	1
	EOR	Exclusive OR Accumulator with Register	1
		* The results of these operations are stored in the respective register. The result of all other operations is stored in the accumulator.	
	LSS	Load S with Short (3-bit) Literal	1
	LST	Load T with Short (3-bit) Literal	1
	SAT	Store Accumulator in Register T	1
	SST	Store Accumulator in Registers S & T	1
	LAL	Load Accumulator with 8-bit Literal	2
	LAS	Load Accumulator with 4-bit Literal	1
	ALL	Logical AND, Accumulator with 8-bit Literal	
	ORL	Logical OR, Accumulator with 8-bit Literal	
	EOL	Exclusive OR, Accumulator with 8-bit Literal	
	ALA	Add Accumulator with 8-bit Literal	
	CMP	Compare Accumulator with 8-bit Literal	
	LIX	Load Accumulator Indirect Module X	4
	LIY	Load Accumulator Indirect Module Y	4
	SIX	Store Accumulator Indirect Module X	3
Shift Operations	LSA	Shift Accumulator Left 1-bit	1
	RSA	Shift Accumulator Right 1-bit	1
	LSN	Shift Accumulator Left 4-bits	1
	RSN	Shift Accumulator Right 4-bits	1
Input/Output Instructions	LAM	Load Accumulator from Module Direct	2
	SAM	Store Accumulator in Module Direct	3
	LIM	Load Accumulator from Module Indirect	4
	SIM	Store Accumulator in Module Indirect	3
Jumps Within 2K Page	JMP	Jump Unconditional	3
	JIZ	Jump if all Zeros	3/2*
	JNZ	Jump if not all zeros	3/2
	JIP	Jump if sign bit positive	3/2
	JRS	Jump if Register S not equal to seven	3/2
	JCS	Jump if carry bit set	3/2
	JCN	Jump if carry bit not set	3/2
Subroutine Instructions	GOS	Go to Subroutine	3
	RET	Return from Subroutine	2
* 3 cycles if true, 2 cycles if false			

MNEMONICS	OPERATION	CYCLES
SAX	Store Accumulator in Register X	1
SAY	Store Accumulator in Register Y	1
LAX	Load Accumulator from Register X	1
LAY	Load Accumulator from Register Y	1
SZX	Store Accumulator in Z Register Module X	3
SZY	Store Accumulator in Z Register Module Y	3
SQZ	Store Accumulator in Q Counter Module X	3
SQY	Store Accumulator in Q Counter Module Y	3
SAV	Store Accumulator in Register V	1
SAW	Store Accumulator in Register W	1
LAV	Load Accumulator in Register V	1
LAW	Load Accumulator in Register W	1
CIA	Clear Accumulator to Zeros	1

Extended Processor Option

OP CODE	V P	DESCRIPTION	CYCLE
EXTENDED PROCESSOR OPTION (2)			
MPY	A*B(n)→B,C	Multiplies Registers	1.92 + 0.48 (n) μs
DIV	(B,C)/A→C(n),B	Divides Registers	2.40 + 0.96 (n) μs

Shift

OP CODE	V P	DESCRIPTION	CYCLE
SHIFTS (8)			
SRA	R, Count	Shift Right Arithmetic	(1 + n/2)
SRC	R, Count	Shift Right Circular	(1 + n/2)
SRLC	R, Count	Shift Right Logical and Count	(1 + n/2)
SRCL	R, Count	Shift Right Circular Thru Link	(1 + n/2)

Programmed Input/Output

OP CODE	V P	DESCRIPTION	CYCLE
INPUT/OUTPUT (6)			
DTOR	R, Device	Data Transfer Out of Register	2
DTIR	R, Device	Data Transfer Into Register	2
DTOM	R, Device	Data Transfer Out of Memory	2
DTIM	R, Device	Data Transfer Into Memory	2
CTRL	FUN, Device	Output Function Control Pulse	2
TEST	FUN, Device	Test Device	2

Skip

OP CODE	V P	DESCRIPTION	CYCLE
SKIP (EXTENDED MNEMONICS) (8)			
SKZ	DISP	Skip if Zero	1
SKN	DISP	Skip if Non Zero	1
SKP	DISP	Skip if Plus	1
SKM	DISP	Skip if Minus	1
SKOT	DISP	Skip on Overflow True	1
SKOF	DISP	Skip on Overflow False (No Overflow)	1
SKS	DISP	Skip on Link Set	1
SKR	DISP	Skip on Link Reset	1

Control

OP CODE	V P	DESCRIPTION	CYCLE
CONTROL (9)			
INE		Interrupt Enable	1
INH		Interrupt Inhibit	1
FMS		Foreground Mode Set	1
BMS		Background Mode Set	1
PMA		Pulse Monitor Alarm	1
LKS		Set Link	1
LKR		Reset Link	1
SYNC		General Sync Pulse	1
WAIT		Stops Instruction Execution	1

Register Change

OP CODE	V P	DESCRIPTION	CYCLE
REGISTER CHANGE (16)			
ZERO	R	Zero Register	1
XEC	R	Execute Register Contents	1
TRS	R	Transfer Register to Status	1
TSR	R	Transfer Status to Register	1
RCSW	R	Read Console Switches	1
DSPL	R	Transfer Register to Console Display	1
ZLBY	R	Zero Left Byte	1
ZRBY	R	Zero Right Byte	1
EXBY	R	Exchange Bytes	1
RTRN	R	Subroutine Return	1
RISE	R	Restore Interrupt System Enable	1
RLK	R	Add Link to Register	1
INCR	R	Increment Register	1
DECR	R	Decrement Register	1
CMPL	R	Complement Register	1
ADDS	R	Add Shift Counter to Register	1

Memory Reference

OP CODE	V P	DESCRIPTION	CYCLE
MEMORY REFERENCE (4)			
LDA	Addr	Load Register A	2
STA	Addr	Store Register A	2
JMP	Addr	Jump Unconditionally	1
JSR	Addr	Jump to Subroutine	1
MEMORY REFERENCE WITH INDEXING (12)			
LDR	R, Addr, X	Load Register	2
STR	R, Addr, X	Store Register	2
CMR	R, Addr, X	Compare Memory with Register	2
LDBY	R, Addr, X	Load Byte	2
STBY	R, Addr, X	Store Byte	2
LARS	Addr, X	Load All Register and Status	10
SARS	Addr, X	Store All Register and Status	10
INCM	Addr, X	Increment Memory	2
DECM	Addr, X	Decrement Memory	2
SBIT	n, Addr, X	Set Bit n (n 0–7)	2
RBIT	n, Addr, X	Reset Bit n (n 0–7)	2
TBIT	n, Addr, X	Test Bit n (n 0–7)	2

Register Operate

OP CODE	V P	DESCRIPTION	CYCLE
REGISTER OPERATE (6)			
RTR	Rd, Rs	Transfer Register to Register	1
ADD	Rd, Rs	Add Registers	1
SUB	Rd, Rs	Sub Registers	1
AND	Rd, Rs	And Registers	1
XOR	Rd, Rs	Exclusive Or Registers	1
OR	Rd, Rs	Or Registers	1
REGISTER OPERATE COMPARE (5)			
ADDC	Rd, Rs	Add Registers and Compare	1
SUBC	Rd, Rs	Subtract Registers and Compare	1
ANDC	Rd, Rs	And Registers and Compare	1
XORC	Rd, Rs	Exclusive Or Registers and Compare	1
ORC	Rd, Rs	Or Registers and Compare	1
REGISTER OPERATE LITERAL (6)			
LDV	R, (Value)	Load Value into Register	2
ADDV	R, (Value)	Add Value to Register	2
SUBV	R, (Value)	Subtract Value from Register	2
ANDV	R, (Value)	And Value with Register	2
XORV	R, (Value)	Exclusive Or Value with Register	2
ORV	R, (Value)	Or Value with Register	2
REGISTER OPERATE LITERAL COMPARE (4)			
ADDVC	R, (Value)	Add Value to Register and Compare	2
SUBVC	R, (Value)	Subtract Value from Register and Compare	2
ANDVC	R, (Value)	And Value with Register and Compare	2
XORVC	R, (Value)	Exclusive Or with Register and Compare	2

DATA-IN BUS SOURCE OPERANDS

OPERATION	OP. FORM	OP3 → OP0 OP FIELD	D1 D0 D-FIELD	S2 → S0 S-FIELD
DIB → DOB	IIIf	HHHH	HH	LHL
DIB → DOB	IIIf	LLLL	HH	LHL
DIB → RF	IIIa	HHHH	HL	LLL → HHH
DIB → WR	IIId	LHHL	HL	XXX
DIB → WR	IIId	LHHL	HH	LHL
DIB → XWR	IIIe	LLLH	HH	LHL
*DIB ALU WR → DOB	Ic	LLLL → HHHH	HH	LLL
*DIB ALU WR → WR	Id	LLLL → HHHH	HH	LLH
DIB ALU WR → XWR	If	LLLL → HHHH	HH	HLL
DIB ALU XWR → DOB	Ih	LLLL → HHHH	HH	HHH
DIB ALU XWR → WR	Ie	LLLL → HHHH	HH	LHH
DIB ALU XWR → XWR	Ig	LLLL → HHHH	HH	HHL
(DIB plus WR plus ALUCIN) LCIR → WR, XWR	IVb	HLLH	HH	LHL
(DIB plus WR plus ALUCIN) RSA → WR, XWR	IVq	HLHH	HH	LHL
DIB plus RF plus ALUCIN → RF	IId	LHHH	HL	LLL → HHH
DIB plus RF plus ALUCIN → WR	IIb	LHLL	HL	LLL → HHH
DIB plus RF plus ALUCIN → XWR	IIc	LHLH	HL	LLL → HHH
DIB plus WR plus ALUCIN → DOB	IIi	LHHH	HH	LHL
DIB plus WR plus ALUCIN → XWR	IIh	LLHH	HH	LHL
DIB plus XWR plus ALUCIN → WR	IIj	HHLL	HH	LHL
DIB plus XWR plus ALUCIN → XWR	IIk	HHLH	HH	LHL

EXTENDED WORKING REGISTER SOURCE OPERANDS

OPERATION	OP. FORM	OP3 → OP0 OP FIELD	D1 D0 D-FIELD	S2 → S0 S-FIELD
XWR ALU DIB → DOB	Ih	LLLL → HHHH	HH	HHH
XWR ALU DIB → WR	Ie	LLLL → HHHH	HH	LHH
XWR ALU DIB → XWR	Ig	LLLL → HHHH	HH	HHL
XWR plus ALUCIN → DOB	III	HHHL	HH	LHL
XWR plus ALUCIN → RF	IIj	HHHL	HL	LLL → HHH
XWR plus DIB plus ALUCIN → WR	IIk	HHLL	HH	LHL
XWR plus DIB plus ALUCIN → XWR	IIe	HHLH	HH	LHL
XWR plus RF plus ALUCIN → WR	IIf	HHLL	HL	LLL → HHH
XWR plus RF plus ALUCIN → XWR		HHLH	HL	LLL → HHH

REGISTER FILE SOURCE OPERANDS

OPERATION	OP. FORM	OP3 → OP0 OP FIELD	D1 D0 D-FIELD	S2 → S0 S-FIELD
RF → DOB	IIIb	LLLL	HL	LLL → HHH
RF → XWR	IIIc	LLLH	HL	LLL → HHH
RF ALU WR → RF	Ia	LLLL → HHHH	LL	LLL → HHH
RF ALU WR → WR	Ib	LLLL → HHHH	LH	LLL → HHH
RF plus DIB plus ALUCIN → RF	IId	LHHH	HL	LLL → HHH
RF plus DIB plus ALUCIN → WR	IIb	LHLL	HL	LLL → HHH
RF plus DIB plus ALUCIN → XWR	IIc	LHLH	HL	LLL → HHH
(RF plus WR plus ALUCIN) LCIR → WR, XWR	IVd	HLLH	HL	LLL → HHH
(RF plus WR plus ALUCIN) RSA → WR, XWR	IVi	HLHH	HL	LLL → HHH
RF plus WR plus ALUCIN → XWR	IIa	LLHH	HL	LLL → HHH
RF plus XWR plus ALUCIN → WR	IIe	HHLL	HL	LLL → HHH
RF plus XWR plus ALUCIN → XWR	IIf	HHLH	HL	LLL → HHH

WORKING REGISTER SOURCE OPERANDS

OPERATION	OP. FORM	OP3 → OP0 OP FIELD	D1 D0 D-FIELD	S2 → S0 S-FIELD
*WR ALU DIB → DOB	Ic	LLLL → HHHH	HH	LLL
*WR ALU DIB → WR	Id	LLLL → HHHH	HH	LLH
WR ALU DIB → XWR	If	LLLL → HHHH	HH	HLL
WR ALU RF → RF	Ia	LLLL → HHHH	LL	LLL → HHH
WR ALU RF → WR	Ib	LLLL → HHHH	LH	LLL → HHH
(WR minus DIB minus 1 plus ALUCIN) LCIR → WR, XWR	IVa	HLLL	HH	LHL
(WR minus DIB minus 1 plus ALUCIN) RSA → WR, XWR	IVf	LLHL	HH	LHL
(WR minus RF minus 1 plus ALUCIN) LCIR → WR, XWR	IVc	HLLL	HL	LLL → HHH
(WR minus RF minus 1 plus ALUCIN) RSA → WR, XWR	IVh	LLHL	HL	LLL → HHH
(WR plus ALUCIN) RSA → WR, XWR	IVe	HLHL	HL	XXX
(WR plus ALUCIN) RSA → WR, XWR	IVe	HLHL	HH	LHL
(WR plus ALUCIN) LCIR → WR	Vd	LLHH	HH	HLH
(WR plus ALUCIN) LCIR → WR	Vd	HLHH	HH	HLH
(WR plus ALUCIN) LSA → WR	Vc	LLHL	HH	HLH
(WR plus ALUCIN) LSL → WR	Vf	HLHL	HH	HLH
(WR plus ALUCIN) RCIR → WR	Vb	LLLH	HH	HLH
(WR plus ALUCIN) RCIR → WR	Vb	HLLH	HH	HLH
(WR plus ALUCIN) RSA → WR	Va	LLLL	HH	HLH
(WR plus ALUCIN) RSL → WR	Ve	HLLL	HH	HLH
(WR plus ALUCIN, XWR) LCIR → (WR, XWR)	VId	HHHH	HH	HLH
(WR plus ALUCIN, XWR) LCIR → (WR, XWR)	VId	LHHH	HH	HLH
(WR plus ALUCIN, XWR) LSA → (WR, XWR)	VIc	LHHL	HH	HLH
(WR plus ALUCIN, XWR) LSL → (WR, XWR)	VIf	HHHL	HH	HLH
(WR plus ALUCIN, XWR) RCIR → (WR, XWR)	VIb	HHLH	HH	HLH
(WR plus ALUCIN, XWR) RCIR → (WR, XWR)	VIb	LHLH	HH	HLH
(WR plus ALUCIN, XWR) RSA → (WR, XWR)	VIa	LHLL	HH	HLH
(WR plus ALUCIN, XWR) RSL → (WR, XWR)	VIe	HHLL	HH	HLH
WR plus DIB plus ALUCIN → DOB	IIi	LHHH	HH	LHL
WR plus DIB plus ALUCIN → XWR	IIh	LLHH	HH	LHL
(WR plus DIB plus ALUCIN) LCIR → WR, XWR	IVb	HLLH	HH	LHL
(WR plus DIB plus ALUCIN) RSA → WR, XWR	IVg	HLHH	HH	LHL
WR plus RF plus ALUCIN → XWR	IIa	LLHH	HL	LLL → HHH
(WR plus RF plus ALUCIN) LCIR → WR, XWR	IVd	HLLH	HL	LLL → HHH
(WR plus RF plus ALUCIN) RSA → WR, XWR	IVi	HLHH	HL	LLL → HHH

INSTRUCTION SET FOR THE 9404

INPUTS					OUTPUTS				FUNCTION	INPUTS					OUTPUTS					FUNCTION
I_4	I_3	I_2	I_1	I_0	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$		I_4	I_3	I_2	I_1	I_0	$\overline{LO}$	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$	$\overline{RO}$	
L	L	L	L	L	L	L	L	L	Byte Mask	H	L	L	L	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		K-Bus Sign Extend
L	L	L	L	H	H	H	H	H	Byte Mask	H	L	L	L	H	$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		K-Bus Sign Extend
L	L	L	H	L	L	L	L	H	Minus "2" in 2s Comp(1)	H	L	L	H	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		D-Bus Sign Extend
L	L	L	H	H	L	L	L	L	Minus "1" in 2s Comp(1)	H	L	L	H	H	$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$		D-Bus Sign Extend
L	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus	H	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	$\overline{RI}$		D-Bus Shift Left
L	L	H	L	H	H	H	H	H	Byte Mask D-Bus	H	L	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	$\overline{RI}$		K-Bus Shift Left
L	L	H	H	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus	H	L	H	H	L		$\overline{LI}$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	D-Bus Shift Right
L	L	H	H	H	L	L	L	L	Byte Mask D-Bus	H	L	H	H	H		$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	D-Bus Shift Right Arith(2)
L	H	L	L	L	L	H	H	H	Negative Byte Sign Mask	H	H	L	L	L		$\overline{LI}$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	K-Bus Shift Right
L	H	L	L	H	H	H	H	H	Positive Byte Sign Mask	H	H	L	L	H		$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	K-Bus Shift Right Arith(2)
L	H	L	H	L	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Byte Mask K-Bus	H	H	L	H	L		$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		Byte Mask K-Bus
L	H	L	H	H	L	L	L	L	Byte Mask K-Bus	H	H	L	H	H		H	H	H	H		Byte Mask K-Bus
L	H	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Load Byte	H	H	H	L	L		D_3	D_2	D_1	D_0		Complement D-Bus
L	H	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Load Byte	H	H	H	L	H		K_3	K_2	K_1	K_0		Complement K-Bus
L	H	H	H	L	H	H	H	L	Plus "1"	H	H	H	H	L							Undefined (Reserved)
L	H	H	H	H	H	H	H	H	Zero	H	H	H	H	H							Undefined (Reserved)

H = HIGH Level
L = LOW Level

(1) Comp = Complement
(2) Arith = Arithmetic

INSTRUCTION SET FOR THE 9407

INSTRUCTION				COMBINATORIAL FUNCTION AVAILABLE ON THE X-BUS	SEQUENTIAL FUNCTION OCCURRING ON THE NEXT RISING CP EDGE
I_3	I_2	I_1	I_0		
L	L	L	L	R_0	R_0 plus D plus CI → R_0 and 0-register
L	L	L	H	R_0 plus D plus CI	
L	L	H	L	R_0	R_0 plus D plus CI → R_1 and 0-register
L	L	H	H	R_0 plus D plus CI	
L	H	L	L	R_0	R_0 plus D plus CI → R_2 and 0-register
L	H	L	H	R_0 plus D plus CI	
L	H	H	L	R_1	R_1 plus D plus CI → R_1 and 0-register
L	H	H	H	R_1 plus D plus CI	
H	L	L	L	R_2	D plus CI → R_2 and 0-register
H	L	L	H	D plus CI	
H	L	H	L	R_0	D plus CI → R_0 and 0-register
H	L	H	H	D plus CI	
H	H	L	L	R_2	R_2 plus D plus CI → R_2 and 0-register
H	H	L	H	R_2 plus D plus CI	
H	H	H	L	R_1	D plus CI → R_1 and 0-register
H	H	H	H	D plus CI	

L = LOW Level
H = HIGH Lev-l

INSTRUCTION FIELD ASSIGNMENT FOR THE 9405

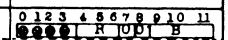
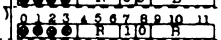
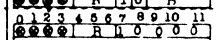
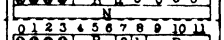
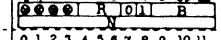
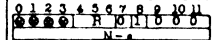
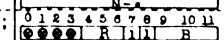
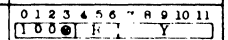
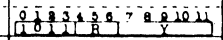
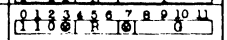
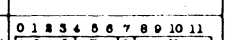
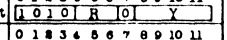
I_2	I_1	I_0	INTERNAL OPERATION	
L	L	L	Rx plus D-Bus plus 1 → Rx	Accumulate
L	L	H	Rx plus D-Bus → Rx	Accumulate
L	H	L	Rx · D-Bus → Rx	Logic AND
L	H	H	D-Bus → Rx	Load
H	L	L	Rx → Output Register	Output
H	L	H	Rx + D-Bus →	Logic OR
H	H	L	Rx ⊕ D-Bus → Rx	Exclusive OR
H	H	H	D-Bus → Rx	Load Complement

NOTES:
1. Rx is the RAM location addressed by A_0-A_2.
2. The result of any operation is always loaded into the Output Register.

Machine instruction set in TLCS-12

Name	Mnemonic	Function	Condition code C N Z	OP-code	Type	Mnemonic	2nd operand address	Instruction format
Load	LOAD R,y	M[R]←M[Y]	– – –	0	RR	y←R	Y←R	0 1 2 3 4 5 6 7 8 9 10 11 0 ● ● ● R 0 0 B
Swap	SWAP R,y	M[R]⇄M[Y]; IS←PSW<3>	– – –	1	R●R	y←(B) ●B	Y←M[B]; (B←0) M[B]←M[B]+1	0 1 2 3 4 5 6 7 8 9 10 11 0 ● ● ● R 1 0 B
And	AND R,y	M[R]←M[R]∧M[Y]	– ○ ○	2	RI	y←N	Y←M^{-1}(N); PC←PC+1	0 1 2 3 4 5 6 7 8 9 10 11 0 ● ● ● R 1 0 0 0 0 N
Or	OR R,y	M[R]←M[R]∨M[Y]	– ○ ○	3	RX	y←N (B)	Y←N+M[B]; PC←PC+1	0 1 2 3 4 5 6 7 8 9 10 11 0 ● ● ● R 0 1 1 B N
Add	ADD R,y	COM[R]←COM[R]+M[Y]	○ ○ ○	4	RS	y←N	Y←N; PC←PC+1	0 1 2 3 4 5 6 7 8 9 10 11 0 ● ● ● R 0 1 1 0 0 0 N–*
Subtract	SUB R,y	COM[R]←COM[R]+M[Y]+1	○ ○ ○	5	R●X	y←(N (B)) ●N (B)	Y←M[N+M[B]]; PC←PC+1	0 1 2 3 4 5 6 7 8 9 10 11 0 ● ● ● R 1 1 1 B N
Multiply	MPY R,y	M[R]○M[R+1]←M[R]×M[Y]	– ○ ○	6	R●S	y←(N) ●N	Y←M[N]; PC←PC+1	0 1 2 3 4 5 6 7 8 9 10 11 0 ● ● ● R 1 1 1 0 0 0 N–*
Execute	EXEC R,y	M[R] is interpreted as an instruction and executed. The Y is added to Y of M[R].	△ △ △ (affected by M[R])	7				
Branch on condition set	BCS R,Y	If (CNZ)∧(R)≠0, then PC←PC+Y; else NOP.	– – –	8	OFFSET Y←–16 to +15			0 1 2 3 4 5 6 7 8 9 10 11 1 0 0 ● R Y
Branch-on-condition cleared	BCC R,Y	If (CNZ)∧(R)=0, then PC←PC+Y; else NOP.	– – –	9				
Rotate left or right	ROT R,Y	COM[R]←COM[R]×2^{Y} (rotate)	○ ○ ○	10				0 1 2 3 4 5 6 7 8 9 10 11 1 0 1 ● R Y
Increment or decr.	INCR R,Y	COM[R]←COM[R]+Y	○ ○ ○	11				
Set a bit	SETB R,G	M[R]<G>←1	– ○ ○	12;0	BIT POSITION G←0 to 11 (G=12 to 15 ; set condition code only)			0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 ● R ● G
Clear a bit	CLRB R,G	M[R]<G>←0	– ○ ○	12;1				
Invert a bit	INVB R,G	M[R]<G>←~M[R]<G>	– ○ ○	13;0				
Test a bit	TSTB R,G	Null←M[R]<G>	– ○ ○	13;1				
Test or operate	TEST R,F	If F_7=1, M[R]←0; if F_8=1, C←0; if F_9=1, C←~C; if F_{10}=1, M[R]←~M[R]; if F_{11}=1, COM[R]←COM[R]+1	○ ○ ○	14				0 1 2 3 4 5 6 7 8 9 10 11 1 1 1 0 R F_8 F_9 F_{10} F_{11}
No-operation	NOP	No action (delay only)	– – –	15				0 1 2 3 4 5 6 7 8 9 10 11 1 1 1 1 ● ● ● ● ● ● ● ●

Note : M(α) : contents of address α, ∧ : bit-wise AND, ∨ : bit-wise OR, – : unchanged, M^{-1}(N) : address of N, ● : 0 or 1,
M[R]<G> : content of bit position G of address R, ○ : concatenation, ~ : complement, ○ : updated, * : address of itself.

TYPE	Name	Mnemonic	Function	Condition code C+ N Z	OP-code	Addressing for Type I instruction: Format	Mnemonic	2nd operand address	Instruction format
I	Load	LOAD R,y	M(R)←M(Y)	– – –	0	RR	y←B	Y←B	
	Swap	SWAP R,y	IS←PSW<8> M(R)←M(Y);	– – –	1	R●R	y←(B) ●B	Y←M[B];(B←B) M(B)←M(B)+1	
	And	AND R,y	M(R)←M(R)∧M(Y)	– ○ ○	2	RI	y←=N	Y←=N; PC←PC+1	
	Or	OR R,y	M(R)←M(R)∨M(Y)	– ○ ○	3	RX	y←N(B)	Y←N+M(B); PC←PC+1	
	Add	ADD R,y	CoM(R)←CoM(R)+M(Y)	○ ○ ○	4	RS	y←N	Y←N; PC←PC+1	
	Subtract	SUB R,y	CoM(R)←CoM(R)+¬M(Y)+1	○ ○ ○	5	R●X	y←(N(B)) ●N(B)	Y←M(N+M(B)); PC←PC+1	
	Multiply	MPY R,y	M(R)oM(R+1)←M(R)×M(Y)	– ○ ○	6	R●S	y←(N) ●N	Y←M(N); PC←PC+1	
	Divide	DIV R,y	If Quotient overflows C←1 Otherwise C←0 M(R)oM(R+1)←M(Y) M(R)←Quotient M(R+1)←Remainder	○ ○ ○	7				
	Store	STOR R,y	M(Y)←M(R)	– – –	14				
	Compare	COMP R,y	CoNULL←CoM(R)+¬M(Y)+1	○ ○ ○	15				
II	Branch-on-condition set	BCS R,Y	If(CNZ)∧(R)≠0, then PC←PC+Y; else NOP;	– – –	8	OFFSET Y←–16 to +15 2's Complement			
	Branch-on-condition cleared	BCC R,Y	If(CNZ)∧(R)=0, then PC←PC+Y; else NOP.	– – –	9				
	Increment or decrement	INCR R,Y	CoM(R)←CoM(R)+Y	○ ○ ○	11				
	Set a bit	SETB R,O	M(R)<O>←1; If O≥12, M(R)←4095	– ○ ○	12;0	BIT POSITION O←0 to 11			
	Clear a bit	CLRB R,O	M(R)<O>←0; If O≥12, M(R)←0	– ○ ○	12;1				
	Invert a bit	INVB R,O	M(R)<O>←¬M(R)<O> ; If O≥12, M(R)←¬M(R)	– ○ ○	13;0				
	Test a bit	TSTB R,O	Null←M(R)<O> ; If O≥12, Null←M(R)	– ○ ○	13;1				
	Rotate left or right	ROT R,Y	CoM(R)←CoM(R)×2^Y (rotate)	○ ○ ○	10;0	OFFSET Y←–8 to +7 2's Complement			
	Test or operate	TEST R,F	If F_3=1, M(R)←0; If F_2=1, C←0; If F_1=1, M(R)←¬M(R); If F_0=1, CoM(R)←CoM(R)+1	○ ○ ○	10;1				

Note: M(a): contents of address a, ∧: bit-wise AND, ∨: bit-wise OR, –: unchanged, ¬^{-1}(N): address of N,
M(R)<O>: content of bit position O, o: concatenation, ~: complement, ○: updated, ⊗: 0 or 1,
+ If R=R_1, Undefine ++ R must be even •: address of itself.

Instruction Set Summary

A total of 256 independent instructions are available, addressed by 8 bit words stored in the program pROMs. These are summarised below

A & B refer to REGISTER "A" and REGISTER "B" contents respectively.

38 Arithmetical Instructions & Maths Routines

Examples:

B + A	COMPLEMENT MSD OF A
½ (B – A)	ONE LEFT SHIFT OF A
B ÷ A	FOUR LEFT SHIFTS OF A
NEGATE A	WILL 2A OVERFLOW?
SIN (A)	IS A = 0? (16MSDs)
ARCTAN (A)	LOG TO BASE 2, 4, 8 or 16
2A	ANTILOG TO BASE 2, 4, 8 or 16
A ÷ 4	SQUARE, CUBE or FOURTH ROOT

8 Conditional Instructions

Examples:

NEGATE A if 1 in P Flag
COMPLEMENT MSD of A if 1 in P Flag

13 Standard Constant Load Instructions

Examples:

Reciprocals of 2, 3, 7, 10 and 32
0.7071
0.3600

22 Custom Constant Load Instructions

Examples:

LOAD STATIC DATA PACK 1, CONSTANT 5
LOAD STATIC DATA PACK 0, CONSTANT 15

9 Custom Polynomial Load Instructions

Example:

LOAD AND DERIVE COEFFICIENTS OF
STATIC DATA PACK 3, POLYNOMINAL 2

16 Specialised Single Instruction Maths Routines

Examples:

DERIVE BINARY POLYNOMIAL COEFFICIENTS
A-D CONVERSION ROUTINE
BINARY TO BCD CONVERSION
INVERSE INTERPOLATE POLYNOMIAL
CARTESIAN TO POLAR CONVERSION (XY→Rθ)
POLYNOMIALISED CALCULATOR TEST ROUTINE
INTERPOLATE PACK 3 SURFACE

8 Flag Instructions

Example:

EXTERNAL STATE TO "P" FLAG

35 Location Jumps and Skip Instructions

Examples:

JUMP TO SUB-ROUTINE PAGE 8
SKIP if 0 in "P" FLAG

64 Ram Read/Write Instructions

Examples:

READ RAM LOCATION 15 to A
COPY A TO RAM LOCATION 31

36 Input/Output Instructions

Examples:

INPUT TO A FROM DIGITAL SOURCE 7
OUTPUT A TO DIGITAL ACCEPTOR 5
STATICISE MULTIPLEX ADDRESS 0110

23 Miscellaneous Instructions

Examples:

INTERCHANGE B & A
LOAD TO 8 LEVEL DATA STACK
AVERAGE 8 LEVELS OF DATA STACK
COPY 5 RAM LOCATIONS TO ALGORITHM RAM

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7 D6 D5 D4 D3 D2 D1 D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE							
MOV d,s	Move register to register	0 1 d d d s s s	4				
MOV M,s	Move register to memory	0 1 1 1 0 s s s	7				
MOV d,M	Move memory to register	0 1 d d d 1 1 0	7				
MVI d,D8	Move immediate to register	0 0 d d d 1 1 0	7				
MVI M,D8	Move immediate to memory	0 0 1 1 0 1 1 0	10				
INCREMENT/DECREMENT							
INR d	Increment register	0 0 d d d 1 0 0	5	•	•	•	
DCR d	Decrement register	0 0 d d d 1 0 1	5	•	•	•	
INR M	Increment memory	0 0 1 1 0 1 0 0	10	•	•	•	
DCR M	Decrement memory	0 0 1 1 0 1 0 1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR							
ADD s	Add register to A	1 0 0 0 0 s s s	4	•	•	•	•
ADC s	Add register to A with carry	1 0 0 0 1 s s s	4	•	•	•	•
SUB s	Subtract register from A	1 0 0 1 0 s s s	4	•	•	•	•
SSB s	Subtract register from A with borrow	1 0 0 1 1 s s s	4	•	•	•	•
ANA s	AND register with A	1 0 1 0 0 s s s	4	•	•	•	0
XRA s	Exclusive OR register with A	1 0 1 0 1 s s s	4	•	•	•	0
ORA s	OR register with A	1 0 1 1 0 s s s	4	•	•	•	0
CMP s	Compare register with A	1 0 1 1 1 s s s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR							
ADD M	Add memory to A	1 0 0 0 0 1 1 0	7	•	•	•	•
ADC M	Add memory to A with carry	1 0 0 0 1 1 1 0	7	•	•	•	•
SUB M	Subtract memory from A	1 0 0 1 0 1 1 0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1 0 0 1 1 1 1 0	7	•	•	•	•
ANA M	AND memory with A	1 0 1 0 0 1 1 0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1 0 1 0 1 1 1 0	7	•	•	•	0
ORA M	OR memory with A	1 0 1 1 0 1 1 0	7	•	•	•	0
CMP M	Compare memory with A	1 0 1 1 1 1 1 0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR							
ADI D8	Add immediate to A	1 1 0 0 0 1 1 0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1 1 0 0 1 1 1 0	7	•	•	•	•
SUI D8	Subtract immediate from A	1 1 0 1 0 1 1 0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1 1 0 1 1 1 1 0	7	•	•	•	•
ANI D8	AND immediate with A	1 1 1 0 0 1 1 0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1 1 1 0 1 1 1 0	7	•	•	•	0
ORI D8	OR immediate with A	1 1 1 1 0 1 1 0	7	•	•	•	0
CPI D8	Compare immediate with A	1 1 1 1 1 1 1 0	7	•	•	•	•
ALU – ROTATE							
RLC	Rotate A left, MSB to carry (8-bit)	0 0 0 0 0 1 1 1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0 0 0 0 1 1 1 1	4				•
RAL	Rotate A left through carry (9-bit)	0 0 0 1 0 1 1 1	4				•
RAR	Rotate A right through carry (9-bit)	0 0 0 1 1 1 1 1	4				•
JUMP							
JMP ADDR	Jump unconditional	1 1 0 0 0 0 1 1	10				
JNZ ADDR	Jump on not zero	1 1 0 0 0 0 1 0	10				
JZ ADDR	Jump on zero	1 1 0 0 1 0 1 0	10				
JNC ADDR	Jump on no carry	1 1 0 1 0 0 1 0	10				
JC ADDR	Jump on carry	1 1 0 1 1 0 1 0	10				
JPO ADDR	Jump on parity odd	1 1 1 0 0 0 1 0	10				
JPE ADDR	Jump on parity even	1 1 1 0 1 0 1 0	10				
JP ADDR	Jump on positive	1 1 1 1 0 0 1 0	10				
JM ADDR	Jump on minus	1 1 1 1 1 0 1 0	10				
CALL							
CALL ADDR	Call unconditional	1 1 0 0 1 1 0 1	17				
CNZ ADDR	Call on not zero	1 1 0 0 0 1 0 0	11/17				
CZ ADDR	Call on zero	1 1 0 0 1 1 0 0	11/17				
CNC ADDR	Call on no carry	1 1 0 1 0 1 0 0	11/17				
CC ADDR	Call on carry	1 1 0 1 1 1 0 0	11/17				
CPO ADDR	Call on parity odd	1 1 1 0 0 1 0 0	11/17				
CPE ADDR	Call on parity even	1 1 1 0 1 1 0 0	11/17				
CP ADDR	Call on positive	1 1 1 1 0 1 0 0	11/17				
CM ADDR	Call on minus	1 1 1 1 1 1 0 0	11/17				
RETURN							
RET	Return	1 1 0 0 1 0 0 1	11				
RNZ	Return on not zero	1 1 0 0 0 0 0 0	5/11				
RZ	Return on zero	1 1 0 0 1 0 0 0	5/11				
RNC	Return on no carry	1 1 0 1 0 0 0 0	5/11				
RC	Return on carry	1 1 0 1 1 0 0 0	5/11				
RPO	Return on parity odd	1 1 1 0 0 0 0 0	5/11				
RPE	Return on parity even	1 1 1 0 1 0 0 0	5/11				
RP	Return on positive	1 1 1 1 0 0 0 0	5/11				
RM	Return on minus	1 1 1 1 1 0 0 0	5/11				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7 D6 D5 D4 D3 D2 D1 D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR							
LXI B,D16	Load immediate register pair BC	0 0 0 0 0 0 0 1	10				
LXI D,D16	Load immediate register pair DE	0 0 0 1 0 0 0 1	10				
LXI H,D16	Load immediate register pair HL	0 0 1 0 0 0 0 1	10				
LXI SP,D16	Load immediate Stack Pointer	0 0 1 1 0 0 0 1	10				
PUSH							
PUSH B	Push register pair BC on stack	1 1 0 0 0 1 0 1	11				
PUSH D	Push register pair DE on stack	1 1 0 1 0 1 0 1	11				
PUSH H	Push register pair HL on stack	1 1 1 0 0 1 0 1	11				
PUSH PSW	Push A and flags on stack	1 1 1 1 0 1 0 1	11				
POP							
POP B	Pop register pair BC off stack	1 1 0 0 0 0 0 1	10				
POP D	Pop register pair DE off stack	1 1 0 1 0 0 0 1	10				
POP H	Pop register pair HL off stack	1 1 1 0 0 0 0 1	10				
POP PSW	Pop A and flags off stack	1 1 1 1 0 0 0 1	10	•	•	•	•
DOUBLE ADD							
DAD B	Add BC to HL	0 0 0 0 1 0 0 1	11				•
DAD D	Add DE to HL	0 0 0 1 1 0 0 1	11				•
DAD H	Add HL to HL	0 0 1 0 1 0 0 1	11				•
DAD SP	Add Stack Pointer to HL	0 0 1 1 1 0 0 1	11				•
INCREMENT REGISTER PAIR							
INX B	Increment BC	0 0 0 0 0 0 1 1	5				
INX D	Increment DE	0 0 0 1 0 0 1 1	5				
INX H	Increment HL	0 0 1 0 0 0 1 1	5				
INX SP	Increment Stack Pointer	0 0 1 1 0 0 1 1	5				
DECREMENT REGISTER PAIR							
DCX B	Decrement BC	0 0 0 0 1 0 1 1	5				
DCX D	Decrement DE	0 0 0 1 1 0 1 1	5				
DCX H	Decrement HL	0 0 1 0 1 0 1 1	5				
DCX SP	Decrement Stack Pointer	0 0 1 1 1 0 1 1	5				
REGISTER INDIRECT							
STAX B	Store A at ADDR in B	0 0 0 0 0 0 1 0	7				
STAX D	Store A at ADDR in D	0 0 0 1 0 0 1 0	7				
LDAX B	Load A at ADDR in B	0 0 0 0 1 0 1 0	7				
LDAX D	Load A at ADDR in D	0 0 0 1 1 0 1 0	7				
DIRECT							
STA ADDR	Store A direct	0 0 1 1 0 0 1 0	13				
LDA ADDR	Load A direct	0 0 1 1 1 0 1 0	13				
SHLD ADDR	Store HL direct	0 0 1 0 0 0 1 0	16				
LHLD ADDR	Load HL direct	0 0 1 0 1 0 1 0	16				
MOVE REGISTER PAIR							
XCHG	Exchange DE and HL register pairs	1 1 1 0 1 0 1 1	4				
XTHL	Exchange top of stack and HL	1 1 1 0 0 0 1 1	17				
SPHL	HL to Stack Pointer	1 1 1 1 1 0 0 1	4				
PCHL	HL to Program Counter	1 1 1 0 1 0 0 1	5				
INPUT/OUTPUT							
IN A	Input	1 1 0 1 1 0 1 1	10				
OUT A	Output	1 1 0 1 0 0 1 1	10				
EI	Enable interrupts	1 1 1 1 1 0 1 1	4				
DI	Disable interrupts	1 1 1 1 0 0 1 1	4				
RST A	Restart	1 1 A A A 1 1 1	11				
MISCELLANEOUS							
CMA	Complement A	0 0 1 0 1 1 1 1	4				
STC	Set carry	0 0 1 1 0 1 1 1	4				1
CMC	Complement carry	0 0 1 1 1 1 1 1	4				CY
DAA	Decimal adjust A	0 0 1 0 0 1 1 1	4	•	•	•	•
NOP	No-operation	0 0 0 0 0 0 0 0	4				
HLT	Halt	0 1 1 1 0 1 1 0	7				

NOTES

[1] Operand Symbols used
A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.

[3] Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
– = flag not affected
0 = flag reset
1 = flag set

INSTRUCTION TABLE

MNEMONIC OPR	MNEMONIC OPA	HEX CODING		DESCRIPTION OF OPERATION
NOP		0	0	No operation.
SKP		1	0	Skip the next instruction word.
JCN	C_x	1	C_x	Jump on condition C_x to the program memory address A1, A2, otherwise continue in sequence (see back cover).
	LABEL	A_2	A_1	
FIM	P_x	2	P_x0	Fetch immediate from program memory data D1. D2 to index register pair P_x.
D2	D1	D2	D1	
SRC	P_x	2	P_x1	Send register control. Send the contents of index register pair P_x to I/O ports and RAM register as chip select and RAM character address.
FIN	P_x	3	P_x0	Fetch indirect. Send contents of register pair 0 out as a program memory address. Data fetched is placed into register pair P_x.
JIN	P_x	3	P_x1	Jump indirect. Jump to the program memory address designated by contents of register pair P_x.
JUN		4	A_3	Jump unconditional to program memory address A1, A2, A3.
	LABEL	A_2	A_1	
JMS		5	A_3	Jump to subroutine located at program memory address A1, A2, A3. Save previous address (push down in stack).
	LABEL	A_2	A_1	
INC	R_x	6	R_x	Increment contents of register R_x.
ISZ	R_x	7	R_x	Increment and step on zero. Increment contents of register R_x. If result is not 0 go to program memory address A1, A2, otherwise step to the next instruction in sequence.
	LABEL	A_2	A_1	
ADD	R_x	8	R_x	Add contents of register R_x to accumulator.
SUB	R_x	9	R_x	Subtract contents of register R_x to accumulator with borrow.
LD	R_x	A	R_x	Load contents of register Rx to accumulator.
XCH	R_x	B	R_x	Exchange contents of index register R_x and accumulator.
BBL	D_x	C	D_x	Branch back one level in stack to the program memory address stored by a prior JMS instruction. Load data D_x to accumulator.
LDM	D_x	D	D_x	Load data D_x to accumulator.
		E	X	I/O and RAM register instructions.
		F	X	Accumulator instructions.

REGISTER PAIR PX LOOKUP TABLE

BANK	PX	FIM	FIN	SRC	JIN
0	P0	20	30	21	31
0	P1	22	32	23	33
0	P2	24	34	25	35
0	P3	26	36	27	37
1	P0'	20	30	21	31
1	P1'	22	32	23	33
1	P2'	24	34	25	35
1	P3'	26	36	27	37
Common	P4	28	38	29	39
Common	P5	2A	3A	2B	3B
Common	P6	2C	3C	2D	3D
Common	P7	2E	3E	2F	3F

I/O AND RAM REGISTER INSTRUCTIONS

MNEMONIC OPR	MNEMONIC OPA	HEX CODING	DESCRIPTION OF OPERATION
WRM		E 0	Write contents of accumulator into previously selected RAM register character.
WMP		E 1	Write contents of accumulator into previously selected RAM output port. (Output lines.)
WRR		E 2	Write contents of accumulator into previously selected output port. (I/O lines.)
WPM		E 3	Write contents of accumulator into previously selected RAM program memory.
WR0		E 4	Write contents of accumulator into previously selected RAM status character 0.
WR1		E 5	Write contents of accumulator into previously selected RAM status character 1.
WR2		E 6	Write contents of accumulator into previously selected RAM status character 2.
WR3		E 7	Write contents of accumulator into previously selected RAM status character 3.
SBM		E 8	Subtract previously selected RAM register character from accumulator with borrow.
RDM		E 9	Read previously selected RAM register character into accumulator.
RDR		E A	Read contents of previously selected input port into accumulator. (I/O lines.)
ADM		E B	Add previously selected RAM register character to accumulator with carry.
RD0		E C	Read previously selected RAM status character 0 into accumulator.
RD1		E D	Read previously selected RAM status character 1 into accumulator.
RD2		E E	Read previously selected RAM status character 2 into accumulator.
RD3		E F	Read previously selected RAM status character 3 into accumulator.

EXTENDED INSTRUCTIONS

MNEMONIC OPR	MNEMONIC OPA	Hex Coding	DESCRIPTION OF OPERATION
HLT		0 1	Halt - Inhibit program counter and data buffers.
BBS		0 2	Branch Back from Interrupt and restore the previous SRC. The Program Counter and send register control are restored to their pre-interrupt value.
LCR		0 3	The contents of the COMMAND REGISTER are transferred to the ACCUMULATOR.
OR4		0 4	The 4 bit contents of register #4 are logically "OR ed" with the ACCUM.
OR5		0 5	The 4 bit contents of index register #5 are logically "OR ed" with the ACCUMULATOR.
AN6		0 6	The 4 bit contents of index register #6 are logically "AND ed" with the ACCUMULATOR.
AN7		0 7	The 4 bit contents of index register #7 are logically "AND ed" with the ACCUMULATOR.
DB0		0 8	DESIGNATE ROM BANK 0. CM ROM_0 becomes enabled.
DB1		0 9	DESIGNATE ROM BANK 1. CM ROM_1 becomes enabled.
SB0		0 A	SELECT INDEX REGISTER BANK 0. The index register Pairs 0-3.
SB1		0 B	SELECT INDEX REGISTER BANK 1. The index register pairs 0*-3*.
EIN		0 C	ENABLE INTERRUPT.
DIN		0 D	DISABLE INTERRUPT.
RPM		0 E	READ PROGRAM MEMORY.

Cont'd on next page

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ACCUMULATOR INSTRUCTIONS

MNEMONIC OPR	MNEMONIC OPA	Hex Coding	DESCRIPTION OF OPERATION
CLB		F 0	Clear both. (Accumulator and carry.)
CLC		F 1	Clear carry
IAC		F 2	Increment accumulator
CMC		F 3	Complement carry
CMA		F 4	Complement accumulator
RAL		F 5	Rotate left (Accumulator and carry)
RAR		F 6	Rotate right (Accumulator and carry)
TCC		F 7	Transmit carry to accumulator and clear carry
DAC		F 8	Decrement accumulator
TCS		F 9	Transfer carry subtract and clear carry
STC		F A	Set carry
DAA		F B	Decimal adjust accumulator
KBP		F C	Keyboard process Converts contents of accumulator from a one out of four code to a binary code
DCL		F D	Designate command line
		F E	
		F F	

Cx CONDITION TABLE FOR JCN INSTRUCTION

C_x MNEMONIC	JCN HEX	C_8	C_4	C_2	C_1	
						Invert Jump Condition
						Jump if Accumulator = 0
						Jump if Carry Bit = 1
						Jump if Test Input = 0 (High)
	10	0	0	0	0	NO OPERATION OR SKP
TO	11	0	0	0	1	Jump if test = 0 (High)
C1	12	0	0	1	0	Jump if CY = 1
TO+C1	13	0	0	1	1	Jump if test = 0 or CY = 1
AO	14	0	1	0	0	Jump if AC = 0
TO+AO	15	0	1	0	1	Jump if test = 0 or AC = 0
C1+AO	16	0	1	1	0	Jump if CY = 1 or AC = 0
TO+C1+AO	17	0	1	1	1	Jump if test = 0 or CY = 1 or AC = 0
	18	1	0	0	0	Jump Unconditionally
T1	19	1	0	0	1	Jump if test = 1 (Low)
CO	1A	1	0	1	0	Jump if CY = 0
T1CO	1B	1	0	1	1	Jump if test = 1 and CY = 0
A1	1C	1	1	0	0	Jump if AC ≠ 0
T1A1	1D	1	1	0	1	Jump if test = 1 and AC ≠ 0
COA1	1E	1	1	1	0	Jump if CY = 0 and AC ≠ 0
T1COA1	1F	1	1	1	1	Jump if test = 1 and CY = 0 and AC ≠ 0

A_1	Low order address bits
A_2	High order address bits
A_3	Chip select
P_x1	Odd register pairs see P_x Lookup Table
P_x0	Even register pairs see P_x Lookup Table
R_x	Register 0 F
D_x	Data
D_1	Data for odd register
D_2	Data for even register
C_x	Jump conditions

instruction set

Mnemonic		Description	Operation	Op Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	No. of Bytes	No. of Machine (M) Cycles	No. of µcycles (T)	(A)	(B)	Condition Flags S	Z	AC	P	CY
DATA TRANSFER GROUP																					
LDA		Load Accumulator Direct	(A) ← ((byte 3)(byte 2))	0	0	1	1	1	0	1	0	3	4	13	13	13					
LDAX	B	Load Accumulator Indirect	(A) ← ((B))	0	0	0	0	1	0	1	0	1	2	7	7	7					
LDAX	D	Load Accumulator Indirect	(A) ← ((D))	0	0	0	1	1	0	1	0	1	2	7	7	7					
LHLD		Load H and L Direct	(L) ← ((byte 3)(byte 2)) (H) ← ((byte 3)(byte 2) + 1)	0	0	1	0	1	0	1	0	3	5	16	16	16					
LXI	B	Load Immediate, Registers B and C	(B) ← (byte 3) (C) ← (byte 2)	0	0	0	0	0	0	0	1	3	3	10	10	10					
LXI	D	Load Immediate, Registers D and E	(D) ← (byte 3) (E) ← (byte 2)	0	0	0	1	0	0	0	1	3	3	10	10	10					
LXI	H	Load Immediate, Registers H and L	(H) ← (byte 3) (L) ← (byte 2)	0	0	1	0	0	0	0	1	3	3	10	10	10					
LXI	SP	Load Immediate, Stack Pointer	(SPH) ← (byte 3) (SPL) ← (byte 2)	0	0	1	1	0	0	0	1	3	3	10	10	10	(Flags Not Affected)				
MOV	M, r	Move to Memory	((H)(L)) ← (r)	0	1	1	1	0	*S*	*S*	*S*	1	2	7	7	7					
MOV	r, M	Move from Memory	(r) ← ((H)(L))	0	1	*D*	*D*	*D*	1	1	0	1	2	7	7	7					
MOV	r1, r2	Move Registers	(r1) ← (r2)	0	1	*D*	*D*	*D*	*S*	*S*	*S*	1	1	5	4	5					
MVI	M	Move to Memory Immediate	((H)(L)) ← (byte 2)	0	0	1	1	0	1	1	0	2	3	10	10	10					
MVI	r	Move Immediate	(r) ← (byte 2)	0	0	*D*	*D*	*D*	1	1	0	2	2	7	7	7					
SHLD		Store H and L Direct	((byte 3)(byte 2)) ← (L) ((byte 3)(byte 2) + 1) ← (H)	0	0	1	0	0	0	1	0	3	5	16	16	16					
STA		Store Accumulator Direct	((byte 3)(byte 2)) ← (A)	0	0	1	1	0	0	1	0	3	4	13	13	13					
STAX	B	Store Accumulator Indirect	((B)) ← (A)	0	0	0	0	0	0	1	0	1	2	7	7	7					
STAX	D	Store Accumulator Indirect	((D)) ← (A)	0	0	0	1	0	0	1	0	1	2	7	7	7					
XCHG		Exchange H and L with D and E	(H) ↔ (D) (L) ↔ (E)	1	1	1	0	1	0	1	1	1	1	4	4	4					
ARITHMETIC GROUP																					
ACI		Add Immediate with Carry	(A) ← (A) + (byte 2) + (CY)	1	1	0	0	1	1	1	0	2	2	7	7	7	‡	‡	‡	‡	‡
ADC	M	Add Memory with Carry	(A) ← (A) + ((H)(L)) + (CY)	1	0	0	0	1	1	1	0	1	2	7	7	7	‡	‡	‡	‡	‡
ADC	r	Add Register with Carry	(A) ← (A) + (r) + (CY)	1	0	0	0	1	*S*	*S*	*S*	1	1	4	4	4	‡	‡	‡	‡	‡
ADD	M	Add Memory	(A) ← (A) + ((H)(L))	1	0	0	0	0	1	1	0	1	2	7	7	7	‡	‡	‡	‡	‡
ADD	r	Add Register	(A) ← (A) + (r)	1	0	0	0	0	*S*	*S*	*S*	1	1	4	4	4	‡	‡	‡	‡	‡
ADI		Add Immediate	(A) ← (A) + (byte 2)	1	1	0	0	0	1	1	0	1	2	7	7	7	‡	‡	‡	‡	‡
DAA		Decimal Adjust Accumulator	8-bit number in Accumulator is converted to two 4 bit BCD digits	0	0	1	0	0	1	1	1	1	1	4	4	4	‡	‡	‡	‡	‡
DAD	B	Add B and C to H and L	(H)(L) ← (H)(L) + (B)(C)	0	0	0	0	1	0	0	1	1	3	10	10	10	·	·	·	·	‡
DAD	D	Add D and E to H and L	(H)(L) ← (H)(L) + (D)(E)	0	0	0	1	1	0	0	1	1	3	10	10	10	·	·	·	·	‡
DAD	H	Add H and L to H and L	(H)(L) ← (H)(L) + (H)(L)	0	0	1	0	1	0	0	1	1	3	10	10	10	·	·	·	·	‡
DAD	SP	Add Stack Pointer to H and L	(H)(L) ← (H)(L) + (SP)	0	0	1	1	1	0	0	1	1	3	10	10	10	·	·	·	·	‡
DCR	M	Decrement Memory	((H)(L)) ← ((H)(L)) - 1	0	0	1	1	0	1	0	1	1	3	10	10	10	‡	‡	‡	‡	·
DCR	r	Decrement Register	(r) ← (r) - 1	0	0	*D*	*D*	*D*	1	0	1	1	1	5	4	5	‡	‡	‡	‡	·
DCX	B	Decrement Registers B and C	(B)(C) ← (B)(C) - 1	0	0	0	0	1	0	1	1	1	1	5	5	5	·	·	·	·	·
DCX	D	Decrement Registers D and E	(D)(E) ← (D)(E) - 1	0	0	0	1	1	0	1	1	1	1	5	5	5	·	·	·	·	·
DCX	H	Decrement Registers H and L	(H)(L) ← (H)(L) - 1	0	0	1	0	1	0	1	1	1	1	5	5	5	·	·	·	·	·
DCX	SP	Decrement Stack Pointer	(SP) ← (SP) - 1	0	0	1	1	1	0	1	1	1	1	5	5	5	·	·	·	·	·
INR	M	Increment Memory	((H)(L)) ← ((H)(L)) + 1	0	0	1	1	0	1	0	0	1	3	10	10	10	‡	‡	‡	‡	·
INR	r	Increment Register	(r) ← (r) + 1	0	0	*D*	*D*	*D*	1	0	0	1	1	5	4	5	‡	‡	‡	‡	·
INX	B	Increment Registers B and C	(B)(C) ← (B)(C) + 1	0	0	0	0	0	0	1	1	1	1	5	5	5	·	·	·	·	·
INX	D	Increment Registers D and E	(D)(E) ← (D)(E) + 1	0	0	0	1	0	0	1	1	1	1	5	5	5	·	·	·	·	·
INX	H	Increment Registers H and L	(H)(L) ← (H)(L) + 1	0	0	1	0	0	0	1	1	1	1	5	5	5	·	·	·	·	·
INX	SP	Increment Stack Pointer	(SP) ← (SP) + 1	0	0	1	1	0	0	1	1	1	1	5	5	5	·	·	·	·	·
SBB	M	Subtract Memory with Borrow	(A) ← (A) - ((H)(L)) - (CY)	1	0	0	1	1	1	1	0	1	2	7	7	7	‡	‡	‡	‡	‡
SBB	r	Subtract Register with Borrow	(A) ← (A) - (r) - (CY)	1	0	0	1	1	*S*	*S*	*S*	1	1	4	4	4	‡	‡	‡	‡	‡
SBI		Subtract Immediate with Borrow	(A) ← (A) - (byte 2) - (CY)	1	1	0	1	1	1	1	0	2	2	7	7	7	‡	‡	‡	‡	‡
SUB	M	Subtract Memory	(A) ← (A) - ((H)(L))	1	0	0	1	0	1	1	0	1	2	7	7	7	‡	‡	‡	‡	‡
SUB	r	Subtract Register	(A) ← (A) - (r)	1	0	0	1	0	*S*	*S*	*S*	1	1	4	4	4	‡	‡	‡	‡	‡
SUI		Subtract Immediate	(A) ← (A) - (byte 2)	1	1	0	1	0	1	1	0	2	2	7	7	7	‡	‡	‡	‡	‡
LOGICAL GROUP																					
ANA	M	AND Memory	(A) ← (A) ∧ ((H)(L))	1	0	1	0	0	1	1	0	1	2	7	7	7	‡	‡	-	‡	0
ANA	r	AND Register	(A) ← (A) ∧ (r)	1	0	1	0	0	*S*	*S*	*S*	1	1	4	4	4	‡	‡	-	‡	0
ANI		AND Immediate	(A) ← (A) ∧ (byte 2)	1	1	1	0	0	1	1	0	2	2	7	7	7	‡	‡	-	‡	0
CMA		Complement Accumulator	(A) ← ($\bar{A}$)	0	0	1	0	1	1	1	1	1	1	4	4	4	·	·	·	·	·
CMC		Complement Carry	(CY) ← ($\overline{CY}$)	0	0	1	1	1	1	1	1	1	1	4	4	4	·	·	·	·	‡
CMP	M	Compare Memory	(A) - ((H)(L))	1	0	1	1	1	1	1	0	1	2	7	7	7	‡	‡[a]	‡	‡	‡[a]
CMP	r	Compare Register	(A) - (r)	1	0	1	1	1	*S*	*S*	*S*	1	1	4	4	4	‡	‡[b]	‡	‡	‡[b]
CPI		Compare Immediate	(A) - (byte 2)	1	1	1	1	1	1	1	0	2	2	7	7	7	‡	‡[c]	‡	‡	‡[c]
ORA	M	OR Memory	(A) ← (A) ∨ ((H)(L))	1	0	1	1	0	1	1	0	1	2	7	7	7	‡	‡	0	‡	0
ORA	r	OR Register	(A) ← (A) ∨ (r)	1	0	1	1	0	*S*	*S*	*S*	1	1	4	4	4	‡	‡	0	‡	0
ORI		OR Immediate	(A) ← (A) ∨ (byte 2)	1	1	1	1	0	1	1	0	2	2	7	7	7	‡	‡	0	‡	0
RAL		Rotate Left through Carry	(A_{n+1}) ← (A_n), (CY) ← (A_7), (A_0) ← (CY)	0	0	0	1	0	1	1	1	1	1	4	4	4	·	·	·	·	‡
RAR		Rotate Right through Carry	(A_n) ← (A_{n+1}), (CY) ← (A_0), (A_7) ← (CY)	0	0	0	1	1	1	1	1	1	1	4	4	4	·	·	·	·	‡
RLC		Rotate Left	(A_{n+1}) ← (A_n), (A_0) ← (A_7), (CY) ← (A_7)	0	0	0	0	0	1	1	1	1	1	4	4	4	·	·	·	·	‡
RRC		Rotate Right	(A_n) ← (A_{n-1}), (A_7) ← (A_0), (CY) ← (A_0)	0	0	0	0	1	1	1	1	1	1	4	4	4	·	·	·	·	‡
STC		Set Carry	(CY) ← 1	0	0	1	1	0	1	1	1	1	1	4	4	4	·	·	·	·	1
XRA	M	Exclusive OR Memory	(A) ← (A) ∀ ((H)(L))	1	0	1	0	1	1	1	0	1	2	7	7	7	‡	‡	0	‡	0
XRA	r	Exclusive OR Register	(A) ← (A) ∀ (r)	1	0	1	0	1	*S*	*S*	*S*	1	1	4	4	4	‡	‡	0	‡	0
XRI		Exclusive OR Immediate	(A) ← (A) ∀ (byte 2)	1	1	1	0	1	1	1	0	2	2	7	7	7	‡	‡	0	‡	0

Notes: a. Z = 1 if (A) = (H)(L); CY = 1 if (A) < (H)(L)

b. Z = 1 if (A) = (r); CY = 1 if (A) < (r)

c. Z = 1 if (A) = (byte 2); CY = 1 if (A) < (byte 2)

Cont'd on next page

instruction set (cont'd.)

Mnemonic	Description	Operation	Op Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	No. of Bytes	No. of Machine (M) Cycles	No. of μcycles (T)	(A)	(B)	Condition Flags S	Z	AC	P	CY
BRANCH GROUP																				
CALL	Call Unconditional	((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	0	1	1	0	1	3	5	17	18	17					
CC	Call on Carry	If CY = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	1	1	1	0	0	3	3/5	11/17	9/18	11/17					
CM	Call on Minus	If S = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	1	1	1	1	0	0	3	3/5	11/17	9/18	11/17					
CNC	Call on No Carry	If CY = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	1	0	1	0	0	3	3/5	11/17	9/18	11/17					
CNZ	Call on Not Zero	If Z = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	0	0	1	0	0	3	3/5	11/17	9/18	11/17	(Flags Not Affected)				
CP	Call on Positive	If S = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	1	1	0	1	0	0	3	3/5	11/17	9/18	11/17					
CPE	Call on Parity Even	If P = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	1	0	1	1	0	0	3	3/5	11/17	9/18	11/17					
CPO	Call on Parity Odd	If P = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	1	0	0	1	0	0	3	3/5	11/17	9/18	11/17					
CZ	Call on Zero	If Z = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	0	1	1	0	0	3	3/5	11/17	9/18	11/17					
JC	Jump on Carry	If CY = 1, (PC) ← (byte 3)(byte 2)	1	1	0	1	1	0	1	0	3	3	10	10	10					
JM	Jump on Minus	If S = 1, (PC) ← (byte 3)(byte 2)	1	1	1	1	1	0	1	0	3	3	10	10	10					
JMP	Jump Unconditional	(PC) ← (byte 3)(byte 2)	1	1	0	0	0	0	1	1	3	3	10	10	10					
JNC	Jump on No Carry	If CY = 0, (PC) ← (byte 3)(byte 2)	1	1	0	1	0	0	1	0	3	3	10	10	10					
JNZ	Jump on Not Zero	If Z = 0, (PC) ← (byte 3)(byte 2)	1	1	0	0	0	0	1	0	3	3	10	10	10					
JP	Jump on Positive	If S = 0, (PC) ← (byte 3)(byte 2)	1	1	1	1	0	0	1	0	3	3	10	10	10					
JPE	Jump on Parity Even	If P = 1, (PC) ← (byte 3)(byte 2)	1	1	1	0	1	0	1	0	3	3	10	10	10					
JPO	Jump on Parity Odd	If P = 0, (PC) ← (byte 3)(byte 2)	1	1	1	0	0	0	1	0	3	3	10	10	10					
JZ	Jump on Zero	If Z = 1, (PC) ← (byte 3)(byte 2)	1	1	0	0	1	0	1	0	3	3	10	10	10					
PCHL	H and L to Program Counter	(PCH) ← (H) (PCL) ← (L)	1	1	1	0	1	0	0	1	1	1	5	6	5					
RC	Return on Carry	If CY = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	1	0	0	0	1	1/3	5/11	6/12	5/11					
RET	Return	(PCL) ← ((SP)). (PCH) ← ((SP) + 1). (SP) ← (SP) + 2.	1	1	0	0	1	0	0	1	1	3	10	10	10					
RM	Return on Minus	If S = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	1	0	0	0	1	1/3	5/11	6/12	5/10					
RNC	Return on No Carry	If CY = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	0	0	0	0	1	1/3	5/11	6/12	5/10					
RNZ	Return on Not Zero	If Z = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	0	0	0	0	1	1/3	5/11	6/12	5/10					
RP	Return on Positive	If S = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	0	0	0	0	1	1/3	5/11	6/12	5/10					
RPE	Return on Parity Even	If P = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	1	0	0	0	1	1/3	5/11	6/12	5/10					
RPO	Return on Parity Odd	If P = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	0	0	0	0	1	1/3	5/11	6/12	5/10					

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instruction set (cont'd.)

Mnemonic	Description	Operation	Op Code								No. of Bytes	No. of Machine (M) Cycles	No. of μcycles (T)	(A)	(B)	Condition Flags				
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0						S	Z	AC	P	CY
BRANCH GROUP (continued)																				
RST	Restart	((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← 8 * (NNN)	1	1	N	N	N	1	1	1	1	3	11	12	11					
RZ	Return on Zero	If Z = 1: (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	1	0	0	0	1	1/3	5/11	6/12	5/11					
STACK, I/O, AND MACHINE CONTROL GROUP																				
DI	Disable Interrupts	The interrupt system is disabled following the execution of the DI instruction	1	1	1	1	0	0	1	1	1	1	4	4	4	·	·	·	·	·
EI	Enable Interrupts	The interrupt system is enabled following the execution of next instruction	1	1	1	1	1	0	1	1	1	1	4	4	4	·	·	·	·	·
HLT	Halt	Processor is stopped, registers and flags are unaffected	0	1	1	1	0	1	1	0	1	1	7	7	7	·	·	·	·	·
IN	Input	(A) ← (data)	1	1	0	1	1	0	1	1	2	3	10	10	10	·	·	·	·	·
NOP	No Operation	No operation is performed, registers and flags are unaffected	0	0	0	0	0	0	0	0	1	1	4	4	4	·	·	·	·	·
OUT	Output	(data) ← (A)	1	1	0	1	0	0	1	1	2	3	10	10	10	·	·	·	·	·
POP B	Pop Registers B and C off Stack	(C) ← ((SP)) (B) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	0	0	0	1	1	3	10	10	10	·	·	·	·	·
POP D	Pop Registers D and E off Stack	(D) ← ((SP)) (E) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	0	0	0	1	1	3	10	10	10	·	·	·	·	·
POP H	Pop Registers H and L off Stack	(H) ← ((SP)) (L) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	0	0	0	1	1	3	10	10	10	·	·	·	·	·
POP PSW	Pop Accumulator and Flags off Stack	(CY) ← $((SP))_0$ (P) ← $((SP))_2$ (AC) ← $((SP))_4$ (Z) ← $((SP))_6$ (S) ← $((SP))_7$ (A) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	0	0	0	1	1	3	10	10	10	‡	‡	‡	‡	‡
PUSH B	Push Registers B and C on Stack	((SP) - 1) ← (B) ((SP) - 2) ← (C) (SP) ← (SP) - 2	1	1	0	0	0	1	0	1	1	3	11	12	11	·	·	·	·	·
PUSH D	Push Registers D and E on Stack	((SP) - 1) ← (D) ((SP) - 2) ← (E) (SP) ← (SP) - 2	1	1	0	1	0	1	0	1	1	3	11	12	11	·	·	·	·	·
PUSH H	Push Registers H and L on Stack	((SP) - 1) ← (H) ((SP) - 2) ← (L) (SP) ← (SP) - 2	1	1	1	0	0	1	0	1	1	3	11	12	11	·	·	·	·	·
PUSH PSW	Push Accumulator and Flags on Stack	((SP) - 1) ← (A) $((SP) - 2)_0$ ← (CY) $((SP) - 2)_1$ ← 1 $((SP) - 2)_2$ ← (P) $((SP) - 2)_3$ ← 0 $((SP) - 2)_4$ ← (AC) $((SP) - 2)_5$ ← 0 $((SP) - 2)_6$ ← (Z) $((SP) - 2)_7$ ← (S) (SP) ← (SP) - 2	1	1	1	1	0	1	0	1	1	3	11	12	11	·	·	·	·	·
SPHL	Move H and L to Stack Pointer	(SP) ← (H)(L)	1	1	1	1	1	0	0	1	1	1	5	6	5	·	·	·	·	·
XTHL	Exchange Top of Stack with H and L	(L) ↔ ((SP)) (H) ↔ ((SP) + 1)	1	1	1	0	0	0	1	1	1	5	18	16	18	·	·	·	·	·
RIM	Read Interrupt Mask																			
SIM	Set Interrupt Mask																			

condition flags and standard rules

There are five condition flags associated with the execution of instructions on the INS8080A. They are Zero, Sign, Parity, Carry, and Auxiliary Carry, and each flag is represented by a 1-bit register in the CPU. A flag is "set" by forcing the bit to 1, "reset" by forcing the bit to 0. The bit positions of the flags are indicated in the PUSH and POP PSW instructions.

Unless indicated otherwise, when an instruction affects a flag, it affects it in the following manner:

ZERO (Z): If the result of an instruction has the value 0, this flag is set; otherwise, it is reset.

SIGN (S): If the most significant bit of the result of the operation has the value 1, this flag is set; otherwise, it is reset.

PARITY (P): If the modulo 2 sum of the bits of the result of the operation is 0 (that is, if the result has even parity), this flag is set; otherwise, it is reset (that is, if the result has odd parity).

CARRY (CY): If the instruction resulted in a carry (from addition) or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set; otherwise, it is reset.

AUXILIARY CARRY (AC): If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise, it is reset. This flag is affected by single-precision additions, subtractions, increments, decrements, comparisons, and logical operations; however, AC is used principally with additions and increments preceding a DAA (Decimal Adjust Accumulator) Instruction.

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symbols and abbreviations

The following symbols and abbreviations are used in the subsequent description of the INS8080A instructions:

Symbols	Meaning
A	Register A (Accumulator)
B	Register B
C	Register C
D	Register D
H	Register H
L	Register L
DDD, SSS	The bit pattern designating one of the registers A, B, C, D, E, H, L (DDD = destination, SSS = source):

DDD or SSS	Register Name
111	A
000	B
001	C
010	D
011	E
100	H
101	L

byte 2	The second byte of the instruction
byte 3	The third byte of the instruction
port	8-bit address of an I/O device
r, r1, r2	One of the registers A, B, C, D, E, H, L

Symbols	Meaning
PC	16-bit program counter register (PCH and PCL are used to refer to the high-order and low-order 8 bits respectively.)
SP	16-bit stack pointer register (SPH and SPL are used to refer to the high-order and low-order 8 bits respectively.)
( )	The contents of the memory location or registers enclosed in the parentheses
←	"Is replaced by"
∧	Logical AND
∀	Exclusive OR
V	Inclusive OR
+	Addition
-	Twos complement subtraction
•	Multiplication
↔	"Exchange"
$\overline{\ }$	The ones complement (for example, $(\overline{A})$)
n	The restart number 0 through 7
NNN	The binary representation 000 through 111 for restart number 0 through 7 respectively
•	"Not affected"
0	"Reset"
1	"Set"
x	Unknown
↕	Flags affected according to Standard Rules

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

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MNEMONIC	INSTRUCTION NAME	FUNCTION	FORMAT	EXECUTION TIME IN MICROSECONDS
LOAD AND STORE				
LD	LOAD	(EA) → (ACr), IF INDIRECT ((EA)) → (ACr)	2	7.0, 9.8 IF INDIRECT
ST	STORE	(ACN) → (EA), IF INDIRECT (ACr) → ((EA))	2	8.4, 11.2 IF INDIRECT
LDB	LOAD BYTE	(1/2 EA) → (AC0 LESS SIGNIFICANT BYTE)	5	16.8 TO 28.0
STB	STORE BYTE	(AC0 LESS SIGNIFICANT BYTE → (1/2 EA) 0 → (SEL)	5	23.8 TO 32.2
ARITHMETIC				
ADD	ADD	(ACr) + (EA) → (ACr) OV, CY	2	7.0
SUB	SUBTRACT	(ACr) - (EA) → (ACr) OV, CY	2	7.0
MPY	MULTIPLY	(EA) * (AC1) → {(AC0, (AC1)} L 0 → (SEL)	5	148.4 TO 170.8
DIV	DIVIDE	{(AC0), (AC1)} → (EA) → (AC0) QUOTIENT 0 → (SEL) OV, L → (AC1) REMAINDER	5	177.8 TO 222.6
DADD	DOUBLE PRECISION ADD	{(AC0), (AC1)} + {(EA), (EA+1)} → {(AC0), (AC1)} 0 → (SEL) OV, CY	5	16.8
DSUB	DOUBLE PRECISION SUBTRACT	{(AC0), (AC1)} - {(EA), (EA + 1)} → {(AC0), (AC1)} 0 → (SEL) OV, CY	5 4B	16.8 4.2
LOGICAL				
AND	AND	(R01) "AND" (EA) → (R01)	3	7.0
OR	OR	(R01) "OR" (EA) → (R01)	3	7.0
SKIP				
ISZ	INCREMENT AND SKIP IF ZERO	(EA) + 1 → (EA) IF (EA) = 0, (PC) + 1 → (PC)	4B	9.8, 11.2 IF SKIP
DSZ	DECREMENT AND SKIP IF ZERO	(EA) - 1 → (EA) IF (EA) = 0, (PC) + 1 - (PC)	4B	11.2, 12.6 IF SKIP
SKG	SKIP IF GREATER THAN	IF (ACr) > (EA), (PC) + 1 → (PC)	2	11.2 TO 14.0
SKNE	SKIP IF NOT EQUAL	IF (ACr) ≠ (EA), (PC) + 1 → (PC)	2	8.4
SKAZ	SKIP IF "AND" IS ZERO	IF (R01) "AND" (EA) = 0, (PC) + 1 → (PC)	3	8.4, 9.8 IF SKIP
SKSTF	SKIP IF STATUS FLAG TRUE	IF (STATUS FLAG N) = 1, (PC) + 1 → (PC) 0 (SEL)	9	18.2 TO 44.8
SKBIT	SKIP IF BIT TRUE	IF (AC0 BIT N) = 1, (PC) + 1 → (PC) 0 (SEL)	9	18.2 TO 44.8
SINGLE BIT				
SETST	SET STATUS BIT	1 → (STATUS FLAG N)	9	18.2 TO 44.8
CLRST	CLEAR STATUS BIT	0 → (STATUS FLAG N)	9	18.2 TO 44.8
SETBIT	SET BIT	1 → (AC0 BIT N)	9	18.2 TO 44.8
CLRBIT	CLEAR BIT	0 → (AC0 BIT N)	9	18.2 TO 44.8
CMPBIT	COMPLEMENT BIT	$\overline{\text{(AC0 BIT N)}}$ → (AC0 BIT N)	9	18.2 TO 44.8
TRANSFER				
JMP	JUMP	EA → (PC), IF INDIRECT (EA) → (ACr)	4A	4.2, 7.0 IF INDIRECT
JSR	JUMP TO SUBROUTINE	(PC) → (STK)	4A	5.6, 8.4 IF INDIRECT
BOC	BRANCH ON CONDITION	EA → (PC), IF INDIRECT (EA) → (PC) IF CONDITION CC IS TRUE, (PC) + D - (PC)	1	5.6, 7.0 IF BRANCH
RTI	RETURN FROM INTERRUPT	(STK) + C → (PC) 1 → (IEF)	8	7.0
RTS	RETURN FROM SUBROUTINE	(STK) + C → (PC)	8	5.6
JSRI	JUMP TO SUBROUTINE IMPLIED	(PC) → (STK) $FFB0_{16}$ + C → (PC)	8	5.6

MNEMONIC	INSTRUCTION NAME	FUNCTION	FORMAT	EXECUTION TIME IN MICROSECONDS
TRANSFER (cont)				
JMPP	JUMP THROUGH POINTER	(100_{16} +N) → (PC)	9	9.8
JSRP	JMP TO SUBROUTINE THRU POINTER	(PC) → (STK) (100_{16} + C) → (PC)	8	11.2
INTERRUPT				
JINT	JUMP INDIRECT TO LEVEL 0	(PC) → (STK), 0 → (IEF) (120_{16} +N) → PC	9	9.8
ISCAN	INTERRUPT SCAN	1/2 (AC1) → (AC1) UNTIL 1 SHIFTED OUT (AC2) + NUMBER OF SHIFTS → (AC2)	9	8.4 TO 100.8
SHIFT				
ROL	ROTATE LEFT	2 (ACr) → (ACr) IF SEL = 0, (BIT 15) → (BIT 0) IF SEL = 1, (BIT 15) → (L), (L) → (BIT 0) } D TIMES	4B	5.6 + 4.2D
ROR	ROTATE RIGHT	1/2 (ACr) → (ACr) IF SEL = 0, (BIT 0) → (BIT 15) IF SEL = 1, (BIT 0) → (L), (L) → (BIT 15) } D TIMES	4B	5.6 + 4.2D
SHL	SHIFT LEFT	2 (ACr) → (ACr) 0 → (BIT 0) IF SEL = 1, (BIT 15) → (L) } D TIMES	4B	5.6 + 4.2D
SHR	SHIFT RIGHT	1/2 (ACr) → (ACr) IF SEL = 0, 0 → (BIT 15) IF SEL = 1, (L) → (BIT 15), 0 → (L) } D TIMES	4B	5.6 + 4.2D
STACK				
PUSH	PUSH ONTO STACK	(ACr) → (STK)	4B	4.2
PULL	PULL FROM STACK	(STK) → (ACr)	4B	4.2
PUSHF	PUSH STATUS FLAGS ONTO STACK	(SF) → (STK)	8	5.6
PULLF	PULL STATUS FLAGS FROM STACK INTO FLAG REGISTER	(STK) → (ACr)	8	7.0
XCHRS	EXCHANGE REGISTER AND STACK	(ACr) → (STK) (STK) → (ACr)	4B	7.0
IMMEDIATE				
LI	LOAD IMMEDIATE	D → (ACr)	4B	4.2
AISZ	ADD IMMEDIATE AND SKIP IF ZERO	(ACr) + D → (ACr) OV, CY IF (ACr) = 0, (PC) + 1 → (PC)	4B	5.6, 7.0 IF SKIP
CAI	COMPLEMENT AND ADD IMMEDIATE	~ (ACr) + D → (ACr)		
REGISTER				
RADD	REGISTER ADD	(SR) + (DR) → (DR) OV, CY	6	4.2
RXCH	REGISTER EXCHANGE	(SR) → (DR), (DR) → (SR)	6	11.2
RCPY	REGISTER COPY	(SR) → (DR)	6	8.4
RXOR	REGISTER EXCLUSIVE OR	(SR) ⊕ (DR) → (DR)	6	8.4
RAND	REGISTER AND	(SR) "AND" (DR) → (DR)	6	8.4
INPUT/OUTPUT				
RIN	REGISTER INPUT	(AC3) + C → (IO ADDR) (IO DATA) → (AC0)	8	9.8
ROUT	REGISTER OUTPUT	(AC3) + C → (IOADDR) (AC0) → (IO DATA)	8	9.8
SFLG	SET FLAG	C → (IOADDR), 1 → (CONTROL FLAG FC)	7	5.6
PFLG	PULSE FLAG	C → (IOADDR), 1 → (CONTROL FLAG FC)	7	5.6
HALT	HALT	PROCESSOR HALTS	8	—

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MNEMONIC ↓ INSTRUCTION — CYCLES ↓ — CONDITIONS

MNEMONIC	CODE OPR	CODE OPA	CYCLES	DESCRIPTION	FB	FA	FZ	FC
CLA	1101	0000	1	Acc ← 0			1	
CLB	1111	1000	1	Acc, FC ← 0			1	0
CLC	1111	1001	1	FC ← 0				0
CMA	1111	1010	1	Acc ← $\overline{(Acc)}$			×	
CMC	1111	1011	1	FC ← $\overline{(FC)}$				×
INC	1111	1100	1	Acc ← (Acc)+1			×	×
DEC	1111	1101	1	Acc ← (Acc)−1			×	×
RAR	1111	1110	1	Acc_{n-1} ← (Acc_n), FC ← (Acc_0), Acc_3 ← (FC)			×	×
RAL	1111	1111	1	Acc_n ← (Acc_{n-1}), Acc_0 ← (FC), FC ← (Acc_3)			×	×
RFA	1111	0010	1	FA ← 0		0		
SFA	1111	0011	1	FA ← 1		1		
RFB	1111	0100	1	FB ← 0	0			
SFB	1111	0101	1	FB ← 1	1			
ADD	1110	0000	1	Acc ← (Acc)+(DP)+(FC)			×	×
SBD	1110	0001	1	Acc ← (Acc)−(DP)−(FC)			×	×
ADB	1110	0010	1	Acc ← (Acc)+(DP)+(FC)			×	×
SBB	1110	0011	1	Acc ← (Acc)−(DP)−(FC)			×	×
ANL	1110	0100	1	Acc ← (Acc)∧(DP)			×	
ORL	1110	0101	1	Acc ← (Acc)∨(DP)			×	
EXL	1110	0110	1	Acc ← (Acc)∀(DP)			×	
S	1010	0000	1	(DP) ← (Acc)				
SM	1010	0 $M_2M_1M_0$	1	(DP) ← (Acc); DP_M ← $(DP_M)\forall 0M_2M_1M_0$				
L	1011	0000	1	Acc ← (DP)			×	
LM	1011	0 $M_2M_1M_0$	1	Acc ← (DP); DP_M ← $(DP_M)\forall 0M_2M_1M_0$			×	
X	1000	0000	1	(Acc) ⇄ (DP)			×	
XM	1000	0 $M_2M_1M_0$	1	(Acc) ⇄ (DP); DP_M ← $(DP_M)\forall 0M_2M_1M_0$			×	
XD	1001	0000	1 or 2	(Acc) ⇄ (DP); skip if DP_L=0; DP_L ← (DP_L)−1			×	
XMD	1001	0 $M_2M_1M_0$	1 or 2	(Acc) ⇄ (DP); DP_M ← $(DP_M)\forall 0M_2M_1M_0$ skip if DP_L=0; DP_L ← (DP_L)−1			×	
LI	1101	$D_3D_2D_1D_0$	1	Acc ← $D_3D_2D_1D_0$			×	
LBO	0111	0100	2	Acc, TR ← $(DP)_{ROM}$			×	
LBA	1110	1001	1	Acc, TR ← $(DP)_{RAM}$			×	
LDI	0101 D_M	D_H D_L	2	DP ← $D_HD_MD_L$				
SDP	1010	10 P_1P_0	4	(P_1P_0) ← (DP)				
LDP	1011	10 P_1P_0	4	DP ← (P_1P_0)				
DED	0111	0000	1 or 2	skip if DP_L=$0_{(16)}$ DP ← (DP)−1				
IND	0111	0110	1 or 2	skip if DP_L=$F_{(16)}$; DP ← (DP)+1				
TAT	1110	0111	1	TR ← (Acc)				
TTA	1110	1000	1	Acc ← (TR)			×	
XTA	1110	1010	1	(Acc) ⇄ (TR)			×	
XHA	1110	1101	1	(Acc) ⇄ (DP_H)			×	
XMA	1110	1110	1	(Acc) ⇄ (DP_M)			×	
XLA	1110	1111	1	(Acc) ⇄ (DP_L)			×	
LW	1000	1000	1	Acc ← (WR)			×	
SW	1001	1000	1	WR ← (Acc)				
DEW	1000	1100	1 or 2	skip if WR=0; WR ← (WR)−1				
LKB	1110	1100	1	Acc, TR ← (KB)			×	
SK	0111	0001	1 or 2	skip if FK=1				
RFK	1111	0110	1	FK ← 0				
SFK	1111	0111	1	FK ← 1				

MNEMONIC	CODE OPR	CODE OPA	CYCLES	DESCRIPTION	FB	FA	FZ	FC
EI	1001	1100	1					
DI	1001	1101	1					
SSR	1010	11 S_1S_0	4	(S_1S_0) ← (TR), (SR), (Acc)				
LSR	1011	11 S_1S_0	4	TR, SR, Acc ← (S_1S_0)	×	×	×	×
SEI	0110	$I_3I_2I_1I_0$	1 or 2	skip if Acc=$I_3I_2I_1I_0$				
SZ	0111	1000	1 or 2	skip if FZ=1				
SZN	0111	1100	1 or 2	skip if FZ=0				
SC	0111	1001	1 or 2	skip if FC=1				
SCN	0111	1101	1 or 2	skip if FC=0				
SAT	0111	1010	1 or 2	skip if FA=1				
SAF	0111	1110	1 or 2	skip if FA=0				
SBT	0111	1011	1 or 2	skip if FB=1				
SBF	0111	1111	1 or 2	skip if FB=0				
JCP	001 P_4	$P_3P_2P_1P_0$	1	PC ← $P_4P_3P_2P_1P_0$				
JMP	0100 P_M	P_H P_L	2	PC ← $P_HP_MP_L$				
JDP	0111	0101	1	PC ← (DP)				
CAL	0001 P_M	P_H P_L	5	↓(SP) ← (PC)+2 PC ← $P_HP_MP_L$				
RT	0111	0011	5	PC ← (SP)↑				
RTS	0111	0010	6	PC ← (SP)↑, PC ← (PC)+1				
NOP	1111	0000	1	No Operation				

	Mnemonic	Instruction code OPR	Instruction code OPA	Description of Operation
Control instruction	NOP	0 0 0 0	0 × × ×	No operation
	STP	0 0 0 0	1 × × ×	Stop
	CFR	0 0 0 1	0 × × ×	reset CTF.
	CFS	0 0 0 1	1 × × ×	set CTF.
Address store instruction	SDR	0 0 1 0	0 r r r	store AC in $WR_{1-3}(n)$. n=rrr
	SDU	0 0 1 0	1 r r r	AC is incremented by one and stored in $WR_{1-3}(n)$. n=rrr
	SDS	0 0 1 0	1 1 1 1	SP is decremented and stores AC in $WR_{1-3}(n)$ with n specified by SP. n=(SP)
Address load instruction	LDR	0 0 1 1	0 r r r	load AC with $WR_{1-3}(n)$. n=rrr
	LDU	0 0 1 1	1 r r r	load AC with $WR_{1-3}(n)$. Then AC is incremented by one. n=rrr
	LDS	0 0 1 1	1 1 1 1	load AC with $WR_{1-3}(n)$ specified by SP. Then SP is incremented by one and the contents of AC and SC are exchanged. n=(SP)
	LDI	0 1 0 0 $a_2\ a_2\ a_2\ a_2$	$a_3\ a_3\ a_3\ a_3$ $a_1\ a_1\ a_1\ a_1$	loads AC_H, AC_M, and AC_L with 12 bits expressed by a_3, a_2, and a_1 respectively.
Branch instruction	JCN	0 1 0 1 $a_2\ a_2\ a_2\ a_2$	$C_3\ C_2\ C_1\ C_0$ $a_1\ a_1\ a_1\ a_1$	If J="1" exchange the contents of AC and SC then jump to SC_H, a_2, a_1. AC becomes SC+2. If J="0" execute SC+2. (Note 1)
Data load instruction	LAR	0 1 1 0	0 r r r	load A_{CC} with $WR_0(n)$. n=rrr
	LAD	0 1 1 0	1 0 0 0	load A_{CC} with the data of the memory location addressed by AC.
	LAM	0 1 1 0	1 m m m	load A_{CC} with the data of the memory location addressed by AC and mmm. (Note 2)
	LAI	0 1 1 1	d d d d	load A_{CC} with dddd.
Data store instruction	SAR	1 0 0 0	0 r r r	Store the A_{CC} content into $WR_0(n)$. n=rrr
	SAD	1 0 0 0	1 0 0 0	Store the A_{CC} content into the memory location addressed by AC.
	SAM	1 0 0 0	1 m m m	Store the A_{CC} content into the memory location addressed by AC and mmm. (Note 2)
Skip instruction	ISU	1 1 0 0	0 r r r	Skips to address SC+2, if $WR_0(n)=0$ n=rrr. Otherwise $WR_0(n)$ is incremented by one.
	ISD	1 1 0 0	1 r r r	Skips to address SC+2, if $WR_0(n)=0$ n=rrr. Otherwise $WR_0(n)$ is decremented by one.
Indirect load instruction	LIN	1 1 0 1	$a_3\ a_3\ a_3\ a_3$	load TM and A_{CC} with the content of the memory location addressed by $a_3\ AC_M\ AC_L$.
Arithmetic & Logic Operation	ORL	1 0 0 1	1 0 0 1	OR operation is carried out between the A_{CC} and the content of memory location addressed by AC.
	ANL	1 0 0 1	1 0 1 0	AND operation is carried out between the A_{CC} and the content of the memory location addressed by AC.
	EXL	1 0 0 1	1 1 0 0	Exclusive OR operation is carried out between the A_{CC} and the content of the memory location addressed by AC.
	ADR	1 0 1 0	0 r r r	Addition is carried out between the A_{CC} and the $WR_0(n)$. n=rrr
	ADD	1 0 1 0	1 0 0 0	Addition is carried out between the A_{CC} and the content of the memory location addressed by AC.
	ADM	1 0 1 0	1 m m m	Addition is carried out between the A_{CC} and the content of the memory location addressed by AC and mmm. (Note 2)
	SBR	1 0 1 1	0 r r r	Subtraction is carried out between the A_{CC} and the $WR_0(n)$. n=rrr
	SBD	1 0 1 1	1 0 0 0	Subtraction is carried out between the A_{CC} and the content of the memory location addressed by AC.
	SBM	1 0 1 1	1 m m m	Subtraction is carried out between the A_{CC} and the content of the memory location addressed by AC and mmm. (Note 2)

Note 1 : $J=\overline{C_3}\cdot(C_2\cdot A_{CC}=0+C_1\cdot OVF=1+C_0\cdot CDF=1)+C_3\cdot(\overline{C_2\cdot A_{CC}=0+C_1\cdot OVF=1+C_0\cdot CDF=1})$

Note 2 : The address for which three bits of AC_M are substituted with mmm.

AC_H AC_M AC_L

(× × × × × m m m × × × ×)

Operations for Registers

(OPR 1 1 1 0 is common to all)

Mnemonic	OPA	Description of Operation
TAS	0 0 0 1	transfers the content of the AC to SC.
TSA	0 0 1 0	transfers the content of the SC to AC.
XSA	0 0 1 1	exchanges the content of the SC with AC.
IAC	0 1 0 0	AC is incremented by one.
DAC	0 1 0 1	AC is decremented by one.
TAL	1 0 0 0	transfers the content of the A_{CC} to AC_L.
TAM	1 0 0 1	transfers the content of the A_{CC} to AC_M.
TAH	1 0 1 0	transfers the content of the A_{CC} to AC_H.
TAT	1 0 1 1	transfers the content of the A_{CC} to TM.
TLA	1 1 0 0	transfers the content of the AC_L to A_{CC}.
TMA	1 1 0 1	transfers the content of the AC_M to A_{CC}.
THA	1 1 1 0	transfers the content of the AC_H to A_{CC}.
TTA	1 1 1 1	transfers the content of the TM to A_{CC}.

Operations for Accumulator

(OPR 1 1 1 1 is common to all)

Mnemonic	OPA	Description of Operation
CLB	0 0 0 0	clear A_{CC} and OVF.
CLC	0 0 0 1	clear OVF.
CLA	0 0 1 0	clear A_{CC}
CMC	0 1 0 0	Complement OVF; $\overline{OVF}\rightarrow OVF$.
CMA	0 1 0 1	Complement A_{CC}; $\overline{A_{CC}}\rightarrow A_{CC}$.
RAL	0 1 1 0	Rotate left. $OVF\rightarrow A_{CC0}$, $A_{CC3}\rightarrow OVF$, $A_{CCi}\rightarrow A_{CCi+1}$.
RAR	0 1 1 1	Rotate right. $A_{CC0}\rightarrow OVF$, $OVF\rightarrow A_{CC3}$, $A_{CCi}\rightarrow A_{CCi-1}$.
INC	1 0 1 0	A_{CC} is incremented by one.
DEC	1 0 1 1	A_{CC} is decremented by one.
DAA	1 1 0 0	Decimal adjust A_{CC} in addition.
DAS	1 1 0 1	Decimal adjust A_{CC} in subtraction.

FUNCTIONAL DESCRIPTION

Four instruction control inputs, IC0 – IC3, and nine select lines, CS0 – CS8, control the flow of data within the MC10801 Microprogram Control Function. The following information describes programming these inputs to perform the various circuit functions. *All truth tables are expressed in negative logic with V_{OL} being a logic 1 and V_{OH} a logic 0.*

TABLE 2[5]

MNEM	CODE IC3	IC2	IC1	IC0	DESCRIPTION	RESET $\overline{RST}$	BRANCH OR REPEAT CONDITION[2]	REGISTER AND FLIP FLOP OUTPUTS [4] V_{OL} → V_{OH} CR0[7]	CR1	CR2	LIFO STACK CR4 – CR7[6]	RSQ[3]
X	X	X	X	X	RESET CONDITION	0	X	0	0	0	"PUSH" CR0 TO STACK	0
INC	1	1	0	0	INCREMENT	1	X	CR0 plus C_{in}	–	–	–	–
JMP	0	0	1	0	JUMP TO NEXT ADDRESS	1	X	NA	–	–	–	–
JIB	1	0	0	0	JUMP TO I BUS	1	X	IB·NA	–	–	–	–
JIN	1	0	0	1	JUMP TO I BUS & LOAD CR2	1	X	IB·NA	–	IB	–	–
JPI	1	0	1	0	JUMP TO PRIMARY INST.	1	X	CR2·NA	–	–	–	–
JEP	1	1	1	0	JUMP TO EXTERNAL PORT	1	X	ØB·NA	–	–	–	–
JL2	0	0	0	1	JUMP & LOAD CR2	1	X	NA	–	IB	–	–
JLA	0	0	1	1	JUMP & LOAD ADDRESS	1	X	NA	CR0 plus C_{in}	–	–	–
JSR	0	0	0	0	JUMP TO SUBROUTINE	1	$\overline{RSQ}$+RIN·$\overline{XB}$=0	NA	–	–	"PUSH" CR0 TO STACK	–
						1	$\overline{RSQ}$+RIN·$\overline{XB}$=1	NA	–	–	"PUSH" CR0 plus C_{in}	–
RTN	1	1	1	1	RETURN FROM SUBROUTINE	1	$\overline{RSQ}$+RIN·$\overline{XB}$=0	CR4	CR1 plus C_{in}	–	"POP" STACK TO CR0	–
						1	$\overline{RSQ}$+RIN·$\overline{XB}$=1	CR4	–	–	"POP" STACK TO CR0	0
RSR	1	1	0	1	REPEAT SUBROUTINE	1	X	CR0 plus C_{in}	NA	–	–	1
RPI	1	0	1	1	REPEAT INSTRUCTION	1	$\overline{RSQ}$+RIN·$\overline{XB}$=0	–	CR1 plus C_{in}	–	–	–
						1	$\overline{RSQ}$+RIN·$\overline{XB}$=1	CR1·NA	–	–	–	0
BRC	0	1	0	1	BRANCH ON CONDITION	1	$\overline{XB}$·(CS4+$\overline{B}$)=0	NA	–	–	–	–
						1	$\overline{XB}$·(CS4+$\overline{B}$)=1	CR0 plus C_{in}	–	–	–	–
BSR	0	1	0	0	BRANCH TO SUBROUTINE	1	$\overline{XB}$·(CS4+$\overline{B}$)=0	NA	–	–	"PUSH" CR0 plus C_{in}	–
						1	$\overline{XB}$·(CS4+$\overline{B}$)=1	CR0 plus C_{in}	–	–	–	–
ROC	0	1	1	1	RETURN ON CONDITION	1	$\overline{XB}$·(CS4+$\overline{B}$)=0	CR4	–	–	"POP" STACK TO CR0	–
						1	$\overline{XB}$·(CS4+$\overline{B}$)=1	NA	–	–	–	–
BRM	0	1	1	0	BRANCH & MODIFY	1	CS4=1	NA	–	–	–	–
						1	CS4=0	CR00=NA0·B CR01=NA1·XB CR02=NA2 CR03=NA3	–	–	–	–

NOTES.
1. X = DON'T CARE STATE
   – = NO CHANGE
2. EQUATIONS APPLY AS SHOWN, WHERE:
   RIN = (CR13·CR12·CR11·CR10)
   $\overline{XB}$ = EXTERNAL EXTENDER BUS NODE (see Table 3)
   $\overline{B}$ = COMPLEMENT OF BRANCH INPUT
3. RSQ = OUTPUT OF RSR FLIP FLOP
4. ALL REGISTERS AND RSR FLIP FLOP CHANGE STATE ON V_{OL} TO V_{OH} (POSITIVE GOING) CLOCK TRANSITION
5. NEGATIVE LOGIC USED THROUGHOUT
6. TABLE 8 SHOWS LIFO STACK TRUTH TABLE
7. CR0 CHIP OUTPUTS ENABLED WHEN CS5=1

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle
Accumulator	ADD A, R	Add register to A	1	1
	ADD A, @R	Add data memory to A	1	1
	ADD A, #data	Add immediate to A	2	2
	ADDC A, R	Add register with carry	1	1
	ADDC A, @R	Add data memory with carry	1	1
	ADDC A, #data	Add immediate with carry	2	2
	ANL A, R	And register to A	1	1
	ANL A, @R	And data memory to A	1	1
	ANL A, #data	And immediate to A	2	2
	ORL A, R	Or register to A	1	1
	ORL A, @R	Or data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2
	XRL A, R	Exclusive Or register to A	1	1
	XRL A, @R	Exclusive or data memory to A	1	1
	XRL A, #data	Exclusive or immediate to A	2	2
	INC A	Increment A	1	1
	DEC A	Decrement A	1	1
	CLR A	Clear A	1	1
	CPL A	Complement A	1	1
	DA A	Decimal Adjust A	1	1
	SWAP A	Swap nibbles of A	1	1
	RL A	Rotate A left	1	1
	RLC A	Rotate A left through carry	1	1
	RR A	Rotate A right	1	1
	RRC A	Rotate A right through carry	1	1
Input/Output	IN A, P	Input port to A	1	2
	OUTL P, A	Output A to port	1	2
	ANL P, #data	And immediate to port	2	2
	ORL P, #data	Or immediate to port	2	2
	INS A, BUS	Input BUS to A	1	2
	OUTL BUS, A	Output A to BUS	1	2
	ANL BUS, #data	And immediate to BUS	2	2
	ORL BUS, #data	Or immediate to BUS	2	2
	MOVD A, P	Input Expander port to A	1	2
	MOVD P, A	Output A to Expander port	1	2
	ANLD P, A	And A to Expander port	1	2
	ORLD P, A	Or A to Expander port	1	2
Registers	INC R	Increment register	1	1
	INC @R	Increment data memory	1	1
	DEC R	Decrement register	1	1
Branch	JMP addr	Jump unconditional	2	2
	JMPP @A	Jump indirect	1	2
	DJNZ R, addr	Decrement register and skip	2	2
	JC addr	Jump on Carry = 1	2	2
	JNC addr	Jump on Carry = 0	2	2
	J Z addr	Jump on A Zero	2	2
	JNZ addr	Jump on A not Zero	2	2
	JT0 addr	Jump on T0 = 1	2	2
	JNT0 addr	Jump on T0 = 0	2	2
	JT1 addr	Jump on T1 = 1	2	2
	JNT1 addr	Jump on T1 = 0	2	2
	JF0 addr	Jump on F0 = 1	2	2
	JF1 addr	Jump on F1 = 1	2	2
	JTF addr	Jump on timer flag	2	2
	JNI addr	Jump on $\overline{INT}$ = 0	2	2
	JBb addr	Jump on Accumulator Bit	2	2

	Mnemonic	Description	Bytes	Cycles
Subroutine	CALL	Jump to subroutine	2	2
	RET	Return	1	2
	RETR	Return and restore status	1	2
Flags	CLR C	Clear Carry	1	1
	CPL C	Complement Carry	1	1
	CLR F0	Clear Flag 0	1	1
	CPL F0	Complement Flag 0	1	1
	CLR F1	Clear Flag 1	1	1
	CPL F1	Complement Flag 1	1	1
Data Moves	MOV A, R	Move register to A	1	1
	MOV A, @R	Move data memory to A	1	1
	MOV A, #data	Move immediate to A	2	2
	MOV R, A	Move A to register	1	1
	MOV @R, A	Move A to data memory	1	1
	MOV R, #data	Move immediate to register	2	2
	MOV @R, #data	Move immediate to data memory	2	2
	MOV A, PSW	Move PSW to A	1	1
	MOV PSW, A	Move A to PSW	1	1
	XCH A, R	Exchange A and register	1	1
	XCH A, @R	Exchange A and data memory	1	1
	XCHD A, @R	Exchange nibble of A and register	1	1
	MOVX A, @R	Move external data memory to A	1	2
	MOVX @R, A	Move A to external data memory	1	2
	MOVP A, @A	Move to A from current page	1	2
	MOVP3 A, @A	Move to A from Page 3	1	2
Timer/Counter	MOV A, T	Read Timer/Counter	1	1
	MOV T, A	Load Timer/Counter	1	1
	STRT T	Start Timer	1	1
	STRT CNT	Start Counter	1	1
	STOP TCNT	Stop Timer/Counter	1	1
	EN TCNTI	Enable Timer/Counter Interrupt	1	1
	DIS TCNTI	Disable Timer/Counter Interrupt	1	1
Control	EN I	Enable external interrupt	1	1
	DIS I	Disable external interrupt	1	1
	SEL RB0	Select register bank 0	1	1
	SEL RB1	Select register bank 1	1	1
	SEL MB0	Select memory bank 0	1	1
	SEL MB1	Select memory bank 1	1	1
	ENT0 CLK	Enable Clock output on T0	1	1
	NOP	No Operation	1	1

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MICRO CODE				ALU SOURCE OPERANDS	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

Figure 2. ALU Source Operand Control.

MICRO CODE				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S − R
L	H	L	2	R Minus S	R − S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
H	H	L	6	R EX-OR S	R ∀ S
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X= Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB, Down is toward LSB.

Figure 4. ALU Destination Control.

TABLE II-B
FUNCTIONAL DESCRIPTION OF Am29811 INSTRUCTION SET

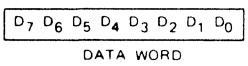
MNEMONIC	INPUTS			OUTPUTS				
	INSTRUCTION I_3 I_2 I_1 I_0	FUNCTION	TEST INPUT	NEXT ADDR SOURCE	FILE	COUNTER	MAP-E	PL-E
JZ	L L L L	JUMP ZERO	X	D	HOLD	L L*	H	L
CJS	L L L H	COND JSB PL	L	PC	HOLD	HOLD	H	L
			H	D	PUSH	HOLD	H	L
JMAP	L L H L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L L H H	COND JUMP PL	L	PC	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
PUSH	L H L L	PUSH/COND LD CNTR	L	PC	PUSH	HOLD	H	L
			H	PC	PUSH	LOAD	H	L
JSRP	L H L H	COND JSB R/PL	L	R	PUSH	HOLD	H	L
			H	D	PUSH	HOLD	H	L
CJV	L H H L	COND JUMP VECTOR	L	PC	HOLD	HOLD	H	H
			H	D	HOLD	HOLD	H	H
JRP	L H H H	COND JUMP R/PL	L	R	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
RFCT	H L L L	REPEAT LOOP, CNTR ≠ 0	L	F	HOLD	DEC	H	L
			H	PC	POP	HOLD	H	L
RPCT	H L L H	REPEAT PL, CNTR ≠ 0	L	D	HOLD	DEC	H	L
			H	PC	HOLD	HOLD	H	L
CRTN	H L H L	COND RTN	L	PC	HOLD	HOLD	H	L
			H	F	POP	HOLD	H	L
CJPP	H L H H	COND JUMP PL & POP	L	PC	HOLD	HOLD	H	L
			H	D	POP	HOLD	H	L
LDCT	H H L L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H H L H	TEST END LOOP	L	F	HOLD	HOLD	H	L
			H	PC	POP	HOLD	H	L
CONT	H H H L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H H H H	JUMP PL	X	D	HOLD	HOLD	H	L

L = LOW H = HIGH X = Don't Care DEC = Decrement *LL = Special Case

BASIC INSTRUCTION SET

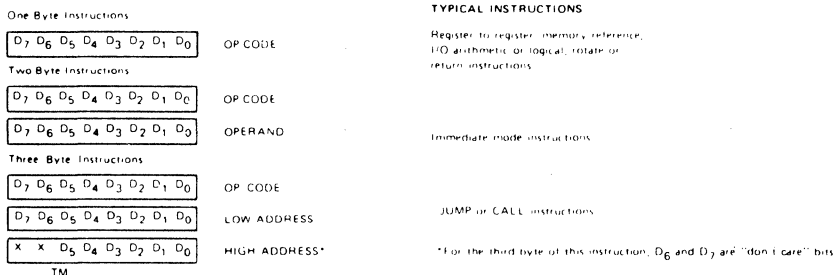
Data and Instruction Formats

Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.



DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.



For the MCS-8™ a logic "1" is defined as a high level and a logic "0" is defined as a low level.

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
(1) MOV r_1, r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) MOV r, M	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
MOV M, r	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) MVI r	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
MVI M	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INR r	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCR r	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADD r	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADD M	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ADC r	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B from the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ADC M	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	
SUB r	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUB M	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0 B B	0 1 0 B B B	1 0 0 B B B	
SBB r	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBB M	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0 B B	0 1 1 B B B	1 0 0 B B B	

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BASIC INSTRUCTION SET

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
ANA r	(5)	1 0	1 0 0	S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
ANA M	(8)	1 0	1 0 0	1 1 1	
ANI	(8)	0 0 B B	1 0 0 B B B	1 0 0 B B B	
XRA r	(5)	1 0	1 0 1	S S S	Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRA M	(8)	1 0	1 0 1	1 1 1	
XRI	(8)	0 0 B B	1 0 1 B B B	1 0 0 B B B	
ORA r	(5)	1 0	1 1 0	S S S	Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator.
ORA M	(8)	1 0	1 1 0	1 1 1	
ORI	(8)	0 0 B B	1 1 0 B B B	1 0 0 B B B	
CMP r	(5)	1 0	1 1 1	S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CMP M	(8)	1 0	1 1 1	1 1 1	
CPI	(8)	0 0 B B	1 1 1 B B B	1 0 0 B B B	
RLC	(5)	0 0	0 0 0	0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0	Rotate the content of the accumulator right through the carry.
Program Counter and Stack Control Instructions					
(4) JMP	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$.
(5) JNC, JNZ, JP, JPO	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
JC, JZ JM, JPE	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
CALL	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$. Save the current address (up one level in the stack).
CNC, CNZ, CP, CPO	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
CC, CZ, CM, CPE	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
RET	(5)	0 0	X X X	1 1 1	Unconditionally return (down one level in the stack).
RNC, RNZ, RP, RPO	(3 or 5)	0 0	0 C_4 C_3	1 1	Return (down one level in the stack) if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
RC, RZ RM, RPE	(3 or 5)	0 0	1 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).
Input/Output Instructions					
IN	(8)	0 1	0 0 M	M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00).
Machine Instruction					
HLT	(4)	0 0	0 0 0	0 0 X	Enter the STOPPED state and remain there until interrupted.
	(4)	1 1	1 1 1	1 1 1	

NOTES:
(1) SSS - Source Index Register, DDD - Destination Index Register } These registers, r_i, are designated A(accumulator–000), B(001), C(010), D(011), E(100), H(101), L(110).
(2) Memory registers are addressed by the contents of registers H & L.
(3) Additional bytes of instruction are designated by BBBBBBBB.
(4) X - "Don't Care".
(5) Flag flip-flops are defined by $C_4 C_3$: carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

INSTRUCTION SET

The following is a summary of the Z80 instruction set showing the assembly language mnemonic and the symbolic operation performed by the instruction. A more detailed listing appears in the Z80-CPU technical manual. The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges
- Memory Block Moves
- Memory Block Searches
- 8-bit arithmetic and logic
- 16-bit arithmetic
- General purpose Accumulator & Flag Operations
- Miscellaneous Group
- Rotates and Shifts
- Bit Set, Reset and Test
- Input and Output
- Jumps
- Calls
- Restarts
- Returns

In the table the following terminology is used.

- b ≡ a bit number in any 8-bit register or memory location
- cc ≡ flag condition code
  - NZ ≡ non zero
  - Z ≡ zero
  - NC ≡ non carry
  - C ≡ carry
  - PO ≡ Parity odd or no over flow
  - PE ≡ Parity even or over flow
  - P ≡ Positive
  - M ≡ Negative (minus)
- d ≡ any 8-bit destination register or memory location
- dd ≡ any 16-bit destination register or memory location
- e ≡ 8-bit signed 2's complement displacement used in relative jumps and indexed addressing
- L ≡ 8 special call locations in page zero. In decimal notation these are 0, 8, 16, 24, 32, 40, 48 and 56
- n ≡ any 8-bit binary number
- nn ≡ any 16-bit binary number
- r ≡ any 8-bit general purpose register (A,B,C, D,E,H, or L)
- s ≡ any 8-bit source register or memory location
- s_b ≡ a bit in a specific 8-bit register or memory location
- ss ≡ any 16-bit source register or memory location
- subscript "L" ≡ the low order 8 bits of a 16-bit register
- subscript "H" ≡ the high order 8 bits of a 16-bit register
- ( ) ≡ the contents within the ( ) are to be used as a pointer to a memory location or I/O port number

8-bit registers are A, B, C, D, E, H, L, I and R
16-bit register pairs are AF, BC, DE and HL
16-bit registers are SP, PC, IX and IY

Addressing Modes implemented include combinations of the following:

Immediate	Indexed
Immediate extended	Register
Modified Page Zero	Implied
Relative	Register Indirect
Extended	Bit

	Mnemonic	Symbolic Operation	Comments
8-BIT LOADS	LD r, s	r ← s	s ≡ r, n, (HL), (IX+e), (IY+e)
	LD d, r	d ← r	d ≡ (HL), r (IX+e), (IY+e)
	LD d, n	d ← n	d ≡ (HL), (IX+e), (IY+e)
	LD A, s	A ← s	s ≡ (BC), (DE), (nn), I, R
	LD d, A	d ← A	d ≡ (BC), (DE), (nn), I, R
16-BIT LOADS	LD dd, nn	dd ← nn	dd ≡ BC, DE, HL, SP, IX, IY
	LD dd, (nn)	dd ← (nn)	dd ≡ BC, DE, HL, SP, IX, IY
	LD (nn), ss	(nn) ← ss	ss ≡ BC, DE, HL, SP, IX, IY
	LD SP, ss	SP ← ss	ss = HL, IX, IY
	PUSH ss	$(SP-1) \leftarrow ss_H$; $(SP-2) \leftarrow ss_L$	ss = BC, DE, HL, AF, IX, IY
	POP dd	$dd_L \leftarrow (SP)$; $dd_H \leftarrow (SP+1)$	dd = BC, DE, HL, AF, IX, IY

	Mnemonic	Symbolic Operation	Comments
EXCHANGES	EX DE, HL	DE ↔ HL	
	EX AF, AF'	AF ↔ AF'	
	EXX	$\begin{pmatrix}BC\\DE\\HL\end{pmatrix} \leftrightarrow \begin{pmatrix}BC'\\DE'\\HL'\end{pmatrix}$	
	EX (SP), ss	$(SP) \leftrightarrow ss_L$, $(SP+1) \leftrightarrow ss_H$	ss ≡ HL, IX, IY
MEMORY BLOCK MOVES	LDI	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1	
	LDIR	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1 Repeat until BC = 0	
	LDD	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1	
	LDDR	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1 Repeat until BC = 0	

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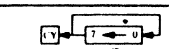
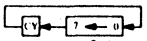
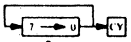
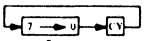
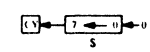
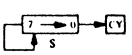
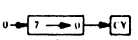
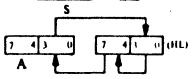
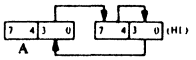
	Mnemonic	Symbolic Operation	Comments
MEMORY BLOCK SEARCHES	CPI	A-(HL), HL ← HL+1 BC ← BC-1	
	CPIR	A-(HL), HL ← HL+1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	A-(HL) sets the flags only. A is not affected
	CPD	A-(HL), HL ← HL-1 BC ← BC-1	
	CPDR	A-(HL), HL ← HL-1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	
8-BIT ALU	ADD s	A ← A + s	
	ADC s	A ← A + s + CY	CY is the carry flag
	SUB s	A ← A - s	
	SBC s	A ← A - s - CY	s ≡ r, n, (HL) (IX+e), (IY+e)
	AND s	A ← A ∧ s	
	OR s	A ← A ∨ s	
	XOR s	A ← A ⊕ s	
	CP s	A - s	s = r, n (HL) (IX+e), (IY+e)
	INC d	d ← d + 1	d = r, (HL) (IX+e), (IY+e)
	DEC d	d ← d - 1	
16-BIT ARITHMETIC	ADD HL, ss	HL ← HL + ss	ss ≡ BC, DE HL, SP
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL - ss - CY	
	ADD IX, ss	IX ← IX + ss	ss ≡ BC, DE, IX, SP
	ADD IY, ss	IY ← IY + ss	ss ≡ BC, DE, IY, SP
	INC dd	dd ← dd + 1	dd ≡ BC, DE, HL, SP, IX, IY
	DEC dd	dd ← dd - 1	dd ≡ BC, DE, HL, SP, IX, IY
GP ACC. & FLAG	DAA	Converts A contents into packed BCD following add or subtract.	Operands must be in packed BCD format
	CPL	$A \leftarrow \overline{A}$	
	NEG	$A \leftarrow \overline{A} + 1$	
	CCF	$CY \leftarrow \overline{CY}$	
	SCF	CY ← 1	
MISCELLANEOUS GROUP	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable Interrupts	
	EI	Enable Interrupts	
	IM0	Set interrupt mode 0	8080A mode
	IM1	Set interrupt mode 1	Call to 0038_H
	IM2	Set interrupt mode 2	Indirect Call
JUMPS	JP nn	PC ← nn	cc { NZ PO, Z PE, NC P, C M }
	JP cc, nn	If condition cc is true PC ← nn, else continue	
	JR e	PC ← PC + e	
	JR kk, e	If condition kk is true PC ← PC + e, else continue	kk { NZ NC, Z C }
	JP (ss)	PC ← ss	ss = HL, IX, IY
	DJNZ e	B ← B - 1, if B = 0 continue, else PC ← PC + e	
CALLS	CALL nn	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, PC ← nn	
	CALL cc, nn	If condition cc is false continue, else same as CALL nn	

	Mnemonic	Symbolic Operation	Comments
ROTATES AND SHIFTS	RLC s		
	RL s		
	RRC s		
	RR s		
	SLA s		s ≡ r, (HL) (IX+e), (IY+e)
	SRA s		
	SRL s		
	RLD		
	RRD		
BIT S, R, & T	BIT b, s	Z ← s_b	Z is zero flag
	SET b, s	s_b ← 1	s ≡ r, (HL) (IX+e), (IY+e)
	RES b, s	s_b ← 0	
INPUT AND OUTPUT	IN A (n)	A ← (n)	
	IN r, (C)	r ← (C)	Set flags
	INI	(HL) ← (C), HL ← HL + 1 B ← B - 1	
	INIR	(HL) ← (C), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	IND	(HL) ← (C), HL ← HL - 1 B ← B - 1	
	INDR	(HL) ← (C), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
	OUT(n), A	(n) ← A	
	OUT(C), r	(C) ← r	
	OUTI	(C) ← (HL), HL ← HL + 1 B ← B - 1	
	OUTIR	(C) ← (HL), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	OUTD	(C) ← (HL), HL ← HL - 1 B ← B - 1	
	OUTDR	(C) ← (HL), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
RESTARTS	RST L	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, $PC_H \leftarrow 0$ $PC_L \leftarrow L$	
RETURNS	RET	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$	
	RET cc	If condition cc is false continue, else same as RET	
	RET I	Return from interrupt, same as RET	
	RET N	Return from non-maskable interrupt	

INSTRUCTION SET

Memory Reference Class (MRI) – This class contains instructions that move data between accumulators and memory, instructions which modify memory, and jump instructions that alter the program flow.

Arithmetic and Logical Class (ALC) – This class contains instructions that manipulate the contents of accumulators and the Carry flag and instructions which perform all the arithmetic and logical functions between accumulators.

Input/Output Class (I/O) – This class contains instructions that move data between the accumulators and the I/O peripheral devices and instructions which serve only to control the I/O devices.

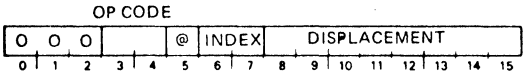
Multiply/Divide Class (M/D) – This class contains two instructions that perform unsigned integer multiplication and division on the accumulators.

Stack Manipulation Class (STK) – This class contains instructions that move data between accumulators and the stack or the stack and frame pointers.

Central Processor Control Class (CPU) – This class contains instructions that modify the state of the CPU as well as general I/O instructions.

MEMORY REFERENCE INSTRUCTIONS (MRI)

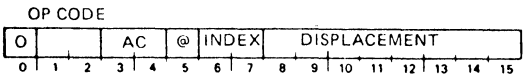
NO ACCUMULATOR



In the No Accumulator – MRI format instructions, bits 0-2 are 000, and bits 3-4 contain the operation code. The effective address is computed from bits 5-15 as described under "Effective Memory Address Calculation."

DSZ	014000	Decrement location *E* by 1 and skip if result is zero.
ISZ	010000	Increment location *E* by 1 and skip if result is zero.
JMP	000000	Jump to location *E* (put *E* in PC).
JSR	004000	Load PC + 1 in AC3 and jump to subroutine at location *E* (put *E* in PC).

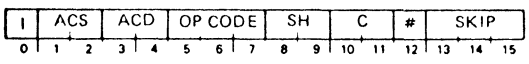
ONE ACCUMULATOR



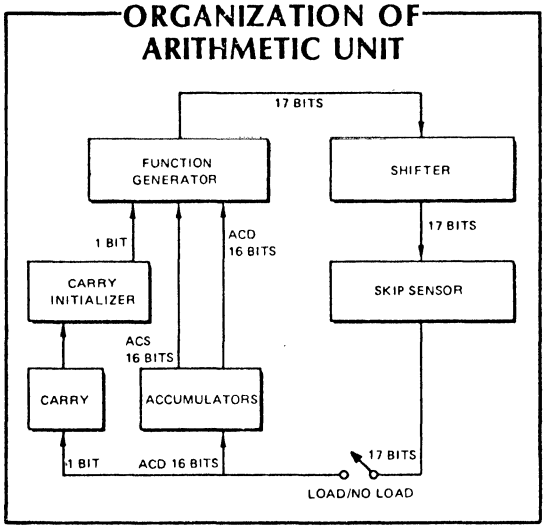
In the One Accumulator – MRI format instructions, bit 0 is 0, and bits 1-2 contain the operation code. Bits 3-4 specify the accumulator for the operation. The effective address is computed from bits 5-15 as described under "Effective Memory Address Calculation."

LDA	020000	Load contents of location *E* into AC.
STA	040000	Store AC in location *E*.

ARITHMETIC AND LOGICAL INSTRUCTIONS (ALC)



In the ALC format instructions, bit 0 is 1, bits 1 and 2 specify the source accumulator, bits 3 and 4 specify the destination accumulator, bits 5-7 contain the operation code, bits 8 and 9 specify the action of the shifter, bits 10 and 11 specify the value to which the carry bit will be initialized, bit 12 specifies whether or not the result will be loaded into the destination accumulator, and bits 13-15 specify the skip test. Each instruction in this format utilizes an arithmetic unit whose logical organization is illustrated below.

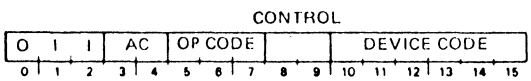


Each instruction specifies two accumulators to supply operands to the function generator, which performs the function specified by bits 5-7 of the instruction. The function generator also produces a carry bit whose value depends upon three quantities: an initial value specified by the instruction, the inputs, and the function performed. The initial value may be derived from the previous value of the carry bit, or the instruction may specify an independent value.

The 17-bit output of the function generator, made up of the carry bit and the 16-bit function result, then goes to the shifter. In the shifter, the 17-bit result can be rotated one place right or left, or the two 8-bit halves of the function result can be swapped without affecting the carry bit. The 17-bit output of the shifter can then be tested for a skip. The skip sensor can test whether the carry bit or the rest of the 17-bit result is or is not equal to zero. After the skip sensor has tested the shifter output it can be loaded into the carry bit and the destination accumulator. Note, however, that loading is not necessary. An instruction in this format can perform a complicated arithmetic and shifting operation and test the result for a skip without affecting the carry bit or either of the operands.

ADC	102000	Add the complement of ACS to ACD
ADD	103000	Add ACS to ACD
AND	103400	And ACS with ACD
COM	100000	Place the complement of ACS in ACD
INC	101400	Place ACS + 1 in ACD
MOV	101000	Move ACS to ACD
NEG	100400	Place negative of ACS in ACD
SUB	102400	Subtract ACS from ACD

INPUT/OUTPUT INSTRUCTIONS (I/O)



Cont'd on next page

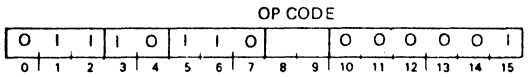
IS66 Cont'd

IS66 Cont'd

In the Input/Output format instructions, bits 0-2 are 011, bits 3-4 specify the accumulator for the operation, bits 5-7 contain the operation code, bits 8-9 specify the control signal to be used, and bits 10-15 contain the device code of the referenced device.

DIA	060400	Data in, A buffer to AC.
DIB	061400	Data in, B buffer to AC.
DIC	062400	Data in, C buffer to AC.
DOA	061000	Data out, AC to A buffer.
DOB	062000	Data out, AC to B buffer.
DOC	063000	Data out, AC to C buffer.
NIO	060000	No operation.
SKPBN	063400	Skip if Busy is 1.
SKPBZ	0635000	Skip if Busy is 0.
SKPDN	063600	Skip if Done is 1.
SKPDZ	063700	Skip if Done is 0.

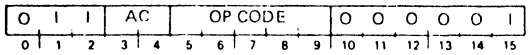
MULTIPLY/DIVIDE INSTRUCTIONS (M/D)



For compatibility with the rest of the NOVA line of computers, multiply and divide are I/O instructions that reference device code 01. Although the instructions are in the standard I/O format, the operation of these instructions is in no way similar to I/O instructions.

DIV	073101	If overflow, set Carry. Otherwise divide AC0-AC1 by AC2. Put quotient in AC1, remainder in AC0.
MUL	073301	Multiply AC1 by AC2, add product to AC0, put result in AC0-AC1.

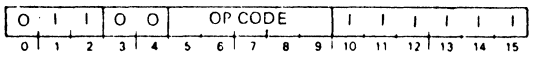
STACK MANIPULATION INSTRUCTIONS (STK)



The stack feature of the microNOVA processor is programmed with eight I/O instructions which use the device code 01. Although the instructions are in the standard I/O format, the operation of these instructions is in no way similar to I/O instructions.

MFFP	060201	Move contents of frame pointer to AC.
MFSP	061201	Move contents of stack pointer to AC.
MTFP	060001	Move contents of AC to frame pointer.
MTSP	061001	Move contents of AC to stack pointer.
POPA	061601	Move top word on stack to AC and decrement stack pointer.
PSHA	061401	Increment stack pointer and move contents of AC to top of stack.
RET	062601	Restore accumulators, program counter and carry from last return block on STACK.
SAV	062401	Push a 5-word return block on STACK.
MSKO	062077	Set up Interrupt Disable flags according to mask in AC (= DOB -, CPU).
RTCEN	071077	Enable interrupts from CPU real-time clock (= DOA 2, CPU).
RTCDS	065077	Disable interrupts from CPU real-time clock (= DOA 1, CPU).
TRAP	100010	Software interrupt (ALC format no-skip, no-load)

CENTRAL PROCESSOR CONTROL INSTRUCTIONS (CPU)



I/O instructions with a device code of 77 perform a number of special functions rather than controlling a specific device. In all but the I/O SKIP instruction, I/O instructions with a device code of 77 use bits 8-9 to control the condition of the Interrupt On flag. An I/O SKIP instruction with a device code of 77 uses bits 8-9 to test the state of the Interrupt On flag.

HALT	063077	Halt the processor (= DOC 0, CPU).
INTA	061477	Acknowledge interrupt by loading code of nearest device that is requesting an interrupt into AC bits 10-15 (= DIB -, CPU).
INTDS	060277	Disable interrupt by clearing Interrupt On (= NIOC CPU).
INTEN	060177	Enable interrupt by setting Interrupt On (= NIOS CPU).
IORST	061077	Clear all IO devices (= DOAC 0, CPU).

The following two pages contain all of the 8080 instructions in a concise, meaningful form. The mnemonic is an abbreviation or acronym that s easy to remember and has been standardized wherever possible. Also, the operation code OPR has been designated Instruction and the operand code OPA has been designated modifier since these terms are more meaningful. Some of the rules used to derive the mnemonics used are as follows: CL is clear and SE is set, LD for LOAD and ST for STORE. These will always appear at the beginning of the mnemonic; i.e. CLA (Clear Accumulator). Letters that appear at the end are: N, Indirect; D, Direct; and I, Immediately i.e. LDAI Load Accumulator Immediately.

The flag status nomenclature is as follows: low case letters are variable and upper case followed by 0 or a 1 indicate absolute condition.

The Register and Memory Instruction Summary is used as follows: Under the Instruction mnemonic one finds the instruction wanted, i.e. CPA (Compare with Accumulator). Then from the modifier one selects what is to be compared with A. The shaded area across the top indicates the possibilites. If A were selected it would be comparing A with A and this is the Hex Code BF. If B were selected it would be comparing A with B and this is the Hex Code B8. Thus, the Hex Code for each instruction and modifier combination appears at the intersection of the instruction row and register modifier column. The program address control instructions, Restart Address instructions, register pair operations and I/O instructions are derived similarly.

PROGRAM ADDRESS CONTROL INSTRUCTIONS

INSTRUCTION MNEMONIC		FLAG CONDITIONS, Cx									DESCRIPTION OF OPERATION		INSTRUCTION CATEGORY
INSTR	MODIFIER		≥	≠			<	=			ARITHMETIC		
		UN	CO	ZO	SO	PO	C1	Z1	S1	P1	LOGICAL		
JMP	Cx	C3	D2	C2	F2	E2	DA	CA	FA	EA	Jump on Condition	3 BYTE INSTR.	JMP
JSR	Cx	CD	D4	C4	F4	E4	DC	CC	FC	EC	Jump to Subroutine		JSR
RET	Cx	C9	D0	C0	F0	E0	D8	C8	F8	E8	Return on Condition		RET

RESTART ADDRESS INSTRUCTION

		00	08	10	18	20	28	30	38	Specified address on page 00	
RST	xx	C7	CF	D7	DF	E7	EF	F7	FF	Restart at specified address	RST

REGISTER PAIR OPERATIONS

		AF	BC	DE	HL	SP	PC	FLAG			
INCP	xx		03	13	23	33			Increment Pair		CTP
DECP	xx		0B	1B	2B	3B			Decrement Pair		CTP
STAN	xx		02	12	77				Store A Indirect		LMR
LDAN	xx		0A	1A	7E				Load A Indirect		LRM
APHL	xx		09	19	29	39		c	Add Pair to H/L		APH
PSP	xx	F5	C5	D5	E5				Push Pair		PSP
PLP	xx	F1	C1	D1	E1			(AF: c,d,z,s,p)	Pull Pair		PLP
SHLD					22				Store H/L Direct	3 BYTE INSTR.	SHD
LHLD					2A				Load H/L Direct		LHD
LPI	xx		01	11	21	31	C3		Load Pair Immediate		LPI
XTHL	xx				E3				Exchange Top & HL		XTH
XPDH	xx			EB					Exchange Pair D/E & H/L		XDH
SPHL	xx					F9			Load SP with H/L		SPH
PCHL	xx						E9		Load PC with H/L		PCH

INPUT/OUTPUT INSTRUCTIONS

INP	Pxx	DB	The Second Byte Pxx is a 2 digit hex port address	Input Port xx	INP
OUT	Pxx	D3		Output Port xx	OUT

2 BYTE INSTR.

Cont'd on next page

IS67 Cont'd

MACHINE INSTRUCTIONS

IS67 Cont'd

	4 TIME STATES	5 TIME STATES								
NOP		00	7F	40	49	52	5B	64	6D	No operation	**NOP**
HLT		76								Halt	**HLT**
EIN		FB								Enable Interupt	**INT**
DIN		F3								Disable Interupt	**INT**

Address, Register Pair, I/O and Machine Instructions

REGISTER AND MEMORY INSTRUCTIONS

INSTRUCTION MNEMONIC												
						IMMEDIATE 2 BYTES						
						MEMORY						
		REGISTER							H,L		FLAG STATUS	DESCRIPTION OF OPERATION	INSTRUCTION CATEGORY
INSTR	MODIFIER	A	B	C	D	E	H	L	M	I			
LDA	x	7F	78	79	7A	7B	7C	7D	7E	3E		Load with register x	**LRR LRM LRI**
LDB	x	47	40	41	42	43	44	45	46	0S			
LDC	x	4F	48	49	4A	4B	4C	4D	4E	0E			
LDD	x	57	50	51	52	53	54	55	56	16			
LDE	x	5F	58	59	5A	5B	5C	5D	5E	1E			
LDH	x	67	60	61	62	63	64	65	66	26			
LDL	x	6F	68	69	6A	6B	6C	6D	6E	2E			
LDM	x	77	70	71	72	73	74	75		36		Load memory with x	**LMR LMI**
INC	x	3C	04	0C	14	1C	24	2C	34		d,z,s,p	Increment register	**CTR CTM**
DEC	x	3D	05	0D	15	1D	25	2D	35		d,z,s,p	Decrement register	
ADA	x	87	80	81	82	83	84	85	86	C6	c,d,z,s,p	Add to A	**ALR ALM ALI**
ADC	x	8F	88	89	8A	8B	8C	8D	8E	CE	c,d,z,s,p	Add to A W/C	
SUA	x	97	90	91	92	93	94	95	96	D6	c,d,z,s,p	Sub from A	
SUC	x	9F	98	99	9A	9B	9C	9D	9E	DE	c,d,z,s,p	Sub from A W/C	
AND	x	A7	A0	A1	A2	A3	A4	A5	A6	E6	C0,D0,z,s,p	And with A	
XRA	x	AF	A8	A9	AA	AB	AC	AD	AE	EE	C0,D0,z,s,p	Exclusive or with A	
ORA	x	B7	B0	B1	B2	B3	B4	B5	B6	F6	C0,D0,z,x,p	Or with A	
CPA	x	BF	B8	B9	BA	BB	BC	BD	BE	FE	c,d,z,s,p	Compare with A	
CLB		AF	0 → C, 0 → A								C0,D0,Z1,S0,P1	Clear A and carry	**ACC**
CLC		B7	0 → C								C0,D0,z,s,p	Clear carry	
CMC		3F	$\overline{C}$ → C								c	Complement carry	
CMA		2F	$\overline{A}$ → A									Complement A	
SEC		37	1 → C								C1	Set carry	
DAA		27	C = ?, Cy = ?								c,d,z,s,p	Decimal adjust A	
RRC		0F	A1 → C; A1 → A8								c	Rotate A right	**ROT**
RAL		17	A8 → C → A1								c	Rotate A left W/C	
RAR		1F	A1 → C → A8								c	Rotate A right W/C	
RLC		07	A8 → C; A8 → A1								c	Rotate A left	
STAD		32	A → M						3 Bytes			Store A direct	**STAD LDAD**
LDAD		3A	M → A									Load A direct	

3 Byte Instructions: Byte 2 = Lower Order Address
Byte 3 = Higher Order Address

DEFINITIONS

A	Accumulator register
B,C,D,E	General registers
H	High order memory address register
L	Low order memory address register
M	Memory
I	Immediate
r	Registers A B C D E H L
x	Registers r, Memory M, Immediate I
c	Carry flag (CONDITION FLAGS)
d	Decimal carry (CONDITION FLAGS)
z	Zero flag (CONDITION FLAGS)
s	Sign flag (CONDITION FLAGS)
p	Parity flag (CONDITION FLAGS)
UN	unconditional
CO	carry flag = 0
DO	decimal carry = 0
ZO	zero flag = 0 (non. zero result)
SO	sign flag = 0 (MSB = 0)
PO	parity flag = 0 (odd parity)
C1	carry flag = 1
D1	decimal carry = 1
Z1	zero flag = 1 (zero result)
S1	sign flag = 1 (MSB = 1)
P1	parity flag = 1 (even parity)
F	flag register

INSTRUCTION TIMING CALCULATIONS

T = Nt

T = Execution Time

N = Number of time states

t = Time State Time

Register and Memory Instructions

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS68

IS68

INSTRUCTION	INSTRUCTION TIME (μsec)		ADDRESSING MODES
	FAST MEMORY*	SLOW MEMORY**	
MEMORY REFERENCE			
ADD	1.5	2.25	DIRECT, INDEXED
ADD DOUBLE	2.25	2.75	DIRECT, INDEXED
AND	1.75	2.25	DIRECT, INDEXED
COMPARE	2.0	2.5	DIRECT, INDEXED
DIVIDE	20.25	20.5	DIRECT, INDEXED
LIMIT	3.5	4.0	RELATIVE
LOAD	1.5	2.25	DIRECT, INDEXED, REL., REL. INDIR.
MULTIPLY	10.5	10.75	DIRECT, INDEXED
OR	1.75	2.25	DIRECT, INDEXED
STORE	2.0	3.5	DIRECT, INDEXED, REL. INDIRECT
SUBTRACT	1.5	2.25	DIRECT, INDEXED
REGISTER - REGISTER			
ABSOLUTE VALUE	2.5	3.0	REGISTER
ADD REGISTER	1.5	2.0	REGISTER
AND REGISTER	1.75	2.0	REGISTER
COMPARE REGISTER	2.0	2.5	REGISTER
COMPLEMENT	2.0	2.0	REGISTER
MOVE	1.5	2.0	REGISTER
NEGATE	2.0	2.5	REGISTER
OR REGISTER	2.0	2.0	REGISTER
POP STACK	2.75	3.25	STACK
PUSH STACK	2.5	3.5	STACK
SUBTRACT REGISTER	1.5	2.0	REGISTER
SHIFT			
ROTATE	2.75 + .75N***	3.25 + .75N***	IMMEDIATE
SHIFT LEFT	2.5 + .5N	2.5 + .5N	IMMEDIATE
SHIFT LEFT DOUBLE	3.25 + N	3.25 + N	IMMEDIATE
SHIFT RIGHT	2.5 + .5N	2.5 + .5N	IMMEDIATE
SHIFT RIGHT ARITH.	2.75 + .5N	3.25 + .5N	IMMEDIATE
SHIFT RIGHT DOUBLE	4.25 + .75N	4.25 + .75N	IMMEDIATE
BRANCH			
BRANCH NEGATIVE	2.0	2.5	RELATIVE, REL. INDIRECT
BRANCH NOT ZERO	2.0	2.5	RELATIVE, REL. INDIRECT
BRANCH POSITIVE	2.0	2.5	RELATIVE, REL. INDIRECT
BRANCH ZERO	2.0	2.5	RELATIVE, REL. INDIRECT
INCREMENT & BRANCH IF ≠ 0	2.25	2.75	RELATIVE
JUMP	1.75	2.25	RELATIVE, REL. INDIRECT
JUMP SUBROUTINE	2.0	3.0	RELATIVE, INDIRECT, REL. INDIR.
SKIP IF "AND" ZERO	2.75	3.75	DIRECT, INDEXED
IMMEDIATE			
ADD IMMEDIATE	1.25	1.75	IMMEDIATE
COMPARE IMMEDIATE	2.0	2.5	IMMEDIATE
LOAD IMMEDIATE	1.25	1.75	IMMEDIATE
INPUT/OUTPUT			
INITIATE BLOCK TRANSFER	2.5	3.25	DIRECT
PARALLEL IN	2.25	2.5	INPUT/OUTPUT
PARALLEL OUT	2.25	2.5	INPUT/OUTPUT
PULSE OUT	2.25	2.75	INPUT/OUTPUT
SERIAL IN	6.5	7.0	INPUT/OUTPUT
SERIAL OUT	6.5	7.0	INPUT/OUTPUT
SKIP IF I/O READY	2.75	3.25	INPUT/OUTPUT
CONTROL			
INTERRUPT MASK	1.75	2.0	IMMEDIATE
LOCK	2.75	3.75	DIRECT
RETURN INTERRUPT	3.5	5.25	IMPLIED
RETURN SUBROUTINE	2.75	3.75	IMPLIED

*MEMORY ACCESS LESS THAN 160 NSEC

**MEMORY ACCESS LESS THAN 660 NSEC

***N = NUMBER OF PLACES SHIFTED MINUS ONE

ARITHMETIC (16)
ADD (W, B, IMM), SUB (W, B), COMPARE (W, B, IMM), INCR (1, 2), DECR (1, 2) MPY, DIV, DADD, DSUB

PROGRAM CONTROL (19)
BRANCH (LINK, LOAD WP), JUMP, JUMP CONDITIONAL (11), RETURN, LOAD (INT MASK, CONFIG. WORD), EXTENDED OPERATION

DATA CONTROL (4)
MOVE (W, B), LOAD (IMM, WP), SWAP BYTES, SOC (W, B), SZC (W, B)

LOGICAL (4)
AND I, OR I, INV, XOR

SHIFTS (4)
SRA, SRL, SRC, SLA

I/O (5)
LDCR, STCR, TB, SBO, SBZ

POWER DOWN (1)
IDLE

NOTE: W = word, B = byte, I = immediate

TMS 9940 Typical Instruction Execution Times

• BRANCH	2.4 μs
• CONDITIONAL JUMP	1.6 μs
• ADD WORD	
REG TO REG	3.2 μs
INDIRECT TO INDEXED	7.2 μs
• ADD BYTE	
REG TO REG	2.0 μs
• MULTIPLY	32 μs
• DIVIDE	44.8 μs
• DECIMAL ADD 2 DIGITS	7.6 μs
• LOAD CRU (REG TO CRU)	
8 BITS	9.2 μs
16 BITS	16.0 μs
• STORE CRU (CRU TO REG)	
8 BITS	10.8 μs
16 BITS	17.6 μs
• SET CRU BIT TO ONE/ZERO	2.4 μs

DOUBLE-BYTE INSTRUCTIONS

MNEMONIC	DESCRIPTION	OBJECT FORMAT	OPERATION	MICRO-CYCLES
	Memory Reference Instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
LD	Load	1 1 0 0 0 m ptr | disp	(AC)←(EA)	18
ST	Store	1 1 0 0 1	(EA)←(AC)	18
AND	AND	1 1 0 1 0	(AC)←(AC) ∧ (EA)	18
OR	OR	1 1 0 1 1	(AC)←(AC) ∨ (EA)	18
XOR	Exclusive-OR	1 1 1 0 0	(AC)←(AC) ∀ (EA)	18
DAD	Decimal Add	1 1 1 0 1	$(AC)\leftarrow(AC)_{10} + (EA)_{10} + (CY/L);(CY/L)$	23
ADD	Add	1 1 1 1 0	(AC)←(AC) + (EA) + (CY/L);(CY/L),(OV)	19
CAD	Complement and Add	1 1 1 1 1	(AC)←(AC) + ~(EA) + (CY/L);(CY/L),(OV)	20
	Memory Increment/Decrement Instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
ILD	Increment and Load	1 0 1 0 1 0 ptr | disp	(AC), (EA)←(EA) + 1	22
DLD	Decrement and Load	1 0 1 1 1 0	(AC), (EA)←(EA) - 1	22
	Immediate Instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
LDI	Load Immediate	1 1 0 0 0 1 0 0 | data	(AC)← data	10
ANI	AND Immediate	1 1 0 1 0 1 0 0	(AC)←(AC) ∧ data	10
ORI	OR Immediate	1 1 0 1 1 1 0 0	(AC)←(AC) ∨ data	10
XRI	Exclusive-OR Immediate	1 1 1 0 0 1 0 0	(AC)←(AC) ∀ data	10
DAI	Decimal Add Immediate	1 1 1 0 1 1 0 0	$(AC)\leftarrow(AC)_{10} + data_{10} + (CY/L);(CY/L)$	15
ADI	Add Immediate	1 1 1 1 0 1 0 0	(AC)←(AC) + data + (CY/L);(CY/L),(OV)	11
CAI	Complement and Add Immediate	1 1 1 1 1 1 0 0	(AC)←(AC) + ~data + (CY/L);(CY/L),(OV)	12
	Transfer Instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
JMP	Jump	1 0 0 1 0 0 ptr | disp	(PC)←EA	11
JP	Jump if Positive	1 0 0 1 0 1	If (AC) ⩾ 0, (PC)←EA	9, 11
JZ	Jump if Zero	1 0 0 1 1 0	If (AC) = 0, (PC)←EA	9, 11
JNZ	Jump if Not Zero	1 0 0 1 1 1	If (AC) ≠ 0, (PC)←EA	9, 11
	Double-Byte Miscellaneous Instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
DLY	Delay	1 0 0 0 1 1 1 1 | disp	count AC to -1, delay = 13 + 2(AC) + 2 disp + 2^9 disp microcycles	13 to 131,593

SINGLE-BYTE INSTRUCTIONS

MNEMONIC	DESCRIPTION	OBJECT FORMAT	OPERATION	MICRO-CYCLES
	Extension Register Instructions	7 6 5 4 3 2 1 0		
LDE	Load AC from Extension	0 1 0 0 0 0 0 0	(AC)←(E)	6
XAE	Exchange AC and Extension	0 0 0 0 0 0 0 1	(AC)↔(E)	7
ANE	AND Extension	0 1 0 1 0 0 0 0	(AC)←(AC) ∧ (E)	6
ORE	OR Extension	0 1 0 1 1 0 0 0	(AC)←(AC) ∨ (E)	6
XRE	Exclusive-OR Extension	0 1 1 0 0 0 0 0	(AC)←(AC) ∀ (E)	6
DAE	Decimal Add Extension	0 1 1 0 1 0 0 0	$(AC)\leftarrow(AC)_{10} + (E)_{10} + (CY/L);(CY/L)$	11
ADE	Add Extension	0 1 1 1 0 0 0 0	(AC)←(AC) + (E) + (CY/L);(CY/L),(OV)	7
CAE	Complement and Add Extension	0 1 1 1 1 0 0 0	(AC)←(AC) + ~(E) + (CY/L);(CY/L),(OV)	8
	Pointer Register Move Instructions	7 6 5 4 3 2 1 0		
XPAL	Exchange Pointer Low	0 0 1 1 0 0 ptr	$(AC)\leftrightarrow(PTR_{7:0})$	8
XPAH	Exchange Pointer High	0 0 1 1 0 1	$(AC)\leftrightarrow(PTR_{15:8})$	8
XPPC	Exchange Pointer with PC	0 0 1 1 1 1	(PC)↔(PTR)	7
	Shift, Rotate, Serial I/O Instructions	7 6 5 4 3 2 1 0		
SIO	Serial Input/Output	0 0 0 1 1 0 0 1	$(E_i)\rightarrow(E_{i-1})$, SIN→$(E_7)$, (E_0)→SOUT	5
SR	Shift Right	0 0 0 1 1 1 0 0	$(AC_i)\rightarrow(AC_{i-1})$, 0→$(AC_7)$	5
SRL	Shift Right with Link	0 0 0 1 1 1 0 1	$(AC_i)\rightarrow(AC_{i-1})$, (CY/L)→$(AC_7)$	5
RR	Rotate Right	0 0 0 1 1 1 1 0	$(AC_i)\rightarrow(AC_{i-1})$, $(AC_0)\rightarrow(AC_7)$	5
RRL	Rotate Right with Link	0 0 0 1 1 1 1 1	$(AC_i)\rightarrow(AC_{i-1})$, $(AC_0)\rightarrow$(CY/L)→(AC_7)	5
	Single-Byte Miscellaneous Instructions	7 6 5 4 3 2 1 0		
HALT	Halt	0 0 0 0 0 0 0 0	Pulse H-flag	8
CCL	Clear Carry/Link	0 0 0 0 0 0 1 0	(CY/L)←0	5
SCL	Set Carry/Link	0 0 0 0 0 0 1 1	(CY/L)←1	5
DINT	Disable Interrupt	0 0 0 0 0 1 0 0	(IE)←0	6
IEN	Enable Interrupt	0 0 0 0 0 1 0 1	(IE)←1	6
CSA	Copy Status to AC	0 0 0 0 0 1 1 0	(AC)←(SR)	5
CAS	Copy AC to Status	0 0 0 0 0 1 1 1	(SR)←(AC)	6
NOP	No Operation	0 0 0 0 1 0 0 0	None	5

Cont'd on next page

IS70 Cont'd

IS70 Cont'd

Instruction Execution Time

INSTRUCTION	READ CYCLES	WRITE CYCLES	TOTAL MICROCYCLES	INSTRUCTION	READ CYCLES	WRITE CYCLES	MICROCYCLES
ADD	3	0	19	JP	2	0	9, 11 for Jump
ADE	1	0	7	JZ	2	0	9, 11 for Jump
ADI	2	0	11	LD	3	0	18
AND	3	0	18	LDE	1	0	6
ANE	1	0	6	LDI	2	0	10
ANI	2	0	10	NOP	1	0	5
CAD	3	0	20	OR	3	0	18
CAE	1	0	8	ORE	1	0	6
CAI	2	0	12	ORI	2	0	10
CAS	1	0	6	RR	1	0	5
CCL	1	0	5	RRL	1	0	5
CSA	1	0	5	SCL	1	0	5
DAD	3	0	23	SIO	1	0	5
DAE	1	0	11	SR	1	0	5
DAI	2	0	15	SRL	1	0	5
DINT	1	0	6	ST	2	1	18
DLD	3	1	22	XAE	1	0	7
DLY	2	0	13 - 131593	XOR	3	0	18
HALT	2	0	8	XPAH	1	0	8
IEN	1	0	6	XPAL	1	0	8
ILD	3	1	22	XPPC	1	0	7
JMP	2	0	11	XRE	1	0	6
JNZ	2	0	9, 11 for Jump	XRI	2	0	10

Note: If slow memory is being used, the appropriate delay should be added for each read or write cycle.

Symbols and Notations Used to Express Instruction Execution

SYMBOL AND NOTATION	MEANING
AC	8-bit Accumulator.
CY/L	Carry/Link Flag in the Status Register.
data	Signed, 8-bit immediate data field.
disp	Displacement; represents an operand in a nonmemory reference instruction or an address modifier field in a memory reference instruction. It is a signed twos-complement number.
EA	Effective Address as specified by the instruction.
E	Extension Register; provides for temporary storage, variable displacements and separate serial input/output port.
i	Unspecified bit of a register.
IE	Interrupt Enable Flag.
m	Mode bit, used in memory reference instructions. Blank parameter sets m = 0, @ sets m = 1.
OV	Overflow Flag in the Status Register.
PC	Program Counter (Pointer Register 0); during address formation, PC points to the last byte of the instruction being executed.
ptr	Pointer Register (ptr = 0 through 3). The register specified in byte 1 of the instruction.
$ptr_{n:m}$	Pointer register bits; n:m = 7 through 0 or 15 through 8.
SIN	Serial Input pin.
SOUT	Serial Output pin.
SR	8-bit Status Register.
( )	Means "contents of." For example, (EA) is contents of Effective Address.
[ ]	Means optional field in the assembler instruction format.
~	Ones complement of value to right of ~.
→	Means "replaces."
←	Means "is replaced by."
↔	Means "exchange."
@	When used in the operand field of the instruction, sets the mode bit (m) to 1 for auto-incrementing/auto-decrementing indexing.
10^+	Modulo 10 addition.
∧	AND operation.
∨	Inclusive-OR operation.
⊻	Exclusive-OR operation.
≥	Greater than or equal to.
=	Equals.
≠	Does not equal.

∧ logical AND (AND) ∨ inclusive OR (OR) ∀ exclusive OR (XOR)

	MNEMONIC		OP CODE BINARY		OP CODE HEX	STATUS EFFECTS	FUNCTION
DATA TRANSFER GROUP	L	load	0000	1101	0D	ZF	A ← M (X, Y)
	LD	load direct	0010	00 a	2a	ZF	A ← M (0, a)
	LI	load immediate	0101	d	5d	ZF	A ← d
	LIC	*load increment Y	0000	1110	0E	ZF	A ← M (X, Y), Y ← Y + 1
	LDC	*load decrement Y	0000	1111	0F	ZF	A ← M (X, Y), Y ← Y − 1
	ST	store	0000	1010	0A		M (X, Y) ← A
	STD	store direct	0010	01 a	2(4+a)		M (0, a) ← A
	STIC	*store increment Y	0000	1011	0B	ZF	M (X, Y) ← A, Y ← Y + 1
	STDC	store decrement Y	0000	1100	0C	ZF	M (X, Y) ← A, Y ← Y − 1
	LX	load X	0011	0 d	3d		X ← d
	LY	load Y	0110	d	6d		Y ← d
	TAX	transfer A to X	0000	0001	01		X ← A
	TAY	transfer A to Y	0000	0011	03		Y ← A
	TYA	transfer Y to A	0000	0010	02	ZF	A ← Y
	TACU	transfer A to counter upper	0001	1001	19		CU ← A
	TACL	transfer A to counter lower	0001	1000	18		CL ← A
	TCAU	transfer counter upper to A	0001	1011	1B	ZF	A ← CU
	TCAL	transfer counter lower to A	0001	1010	1A	ZF	A ← CL
ARITHMETIC AND LOGICAL GROUP	AND	and	0000	0100	04	ZF	A ← A ∧ M (X, Y)
	ANDI	and immediate	0111	d	7d	ZF	A ← A ∧ d
	OR	or	0000	0101	05	ZF	A ← A ∨ M (X, Y)
	XOR	Exclusive or	0000	0110	06	ZF	A ← A ∀ M (X, Y)
	A	add	0000	0111	07	CF ZF	A ← A + M (X, Y) + CF
	AI	add immediate	1000	d	8d	CF ZF	A ← A + d
	CPL	complement	0000	1000	08	ZF	A ← $\bar{A}$
	C	compare	0000	1001	09	CF ZF	$\bar{A}$ + M (X, Y) + 1
	CI	compare immediate	1001	d	9d	CF ZF	A + $\bar{d}$ + 1
	CY	compare Y	1010	d	Ad	ZF	Y ∀ d
	SL	shift	0001	1110	1E	CF ZF	A ← A + A
	ICY	increment Y	0010	1100	2C	CF ZF	Y ← Y + 1
	DCY	decrement Y	0010	1101	2D	ZF	Y ← Y − 1
	ICM	*increment memory	0010	1110	2E	CF ZF	M (X, Y) ← M (X, Y) + 1
	DCM	*decrement memory	0010	1111	2F	CF ZF	M (X, Y) ← M (X, Y) +F
	SM	*set memory bits	1011	d	Bd		M (X, Y) ← M (X, Y) ∨ d
	RM	*reset memory bits	1100	d	Cd		M (X, Y) ← M (X, Y) ∧ $\bar{d}$
	TB	test bits	1101	d	Dd	ZF	A ∧ d

* Single-byte 2-cycle instruction (Two machine cycles are required to execute the instruction, 20μs typ.)
** Two-byte 2-cycle instruction (Two machine cycles are required to execute the instruction, 20μs typ.)
Single-byte single-cycle instruction unless specified (single machine cycle is required to execute the instruction, 10μs typ.)

	MNEMONIC		OP CODE BINARY		OP CODE HEX	STATUS EFFECTS	FUNCTION
I/O GROUP	INA	input via A-port	0001	0100	14	ZF	A ← A-port
	INB	input via B-port	0001	0101	15	ZF	A ← B-port
	OTD	output to D-port	0001	0010	12		D-port ← A, PS
	OTMD	output memory to D-port	0001	0001	11		D-port ← M (X, Y), PS
	OTE	output to E-port	0001	0000	10		E-port ← A
	OTIE	output immediate to E-port	1111	d	Fd		E-port ← d
	RCO	reset C-port	0001	0110	16		C-port (Y) ← 0
	SCO	set C-port	0001	0111	17		C-port (Y) ← 1
	CCO	clear C-port	0001	0011	13		C-port (11~0) ← 0
CONTROL GROUP	RC	reset CF	0010	1000	28	CF	CF ← 0
	RP	reset PS	0010	1001	29	PS	PS ← 0
	SC	set CF	0010	1010	2A	CF	CF ← 1
	SP	set PS	0010	1011	2B	PS	PS ← 1
	BS0	**branch if SNS0=1	0011 m	1011 m	3B mm		PC (7 ~ 0) ← mm if SNS0=1
	BS1	**branch if SF=1	0011 m	1101 m	3D mm		PC (7 ~ 0) ← mm if SF=1
	BS01	**branch if SNS0=1 or SF=1	0011 m	1111 m	3F mm		PC (7 ~ 0) ← mm if SNS0∨SF=1
	BSN0	**branch if SNS0=0	0011 m	1010 m	3A mm		PC (7 ~ 0) ← mm if SNS0=0
	BSN1	**branch if SF=0	0011 m	1100 m	3C mm		PC (7 ~ 0) ← mm if SF=0
	BSN01	**branch if SNS0=0 and SF=0	0011 m	1110 m	3E mm		PC (7 ~ 0) ← mm if SNS0 ∨ SF=0
	BP	**branch is PS=1	1110 m	1001 m	E9 mm		PC (7 ~ 0) ← mm if PS=1
	BC	**branch if CF=1	1110 m	0101 m	E5 mm		PC (7 ~ 0) ← mm if CF=1
	BZ	**branch if ZF=1	1110 m	0011 m	E3 mm		PC (7 ~ 0) ← mm if ZF=1
	BPC	**branch if PS=1 or CF=1	1110 m	1101 m	ED mm		PC(7~0) ← mm if PS ∨ CF=1
	BPZ	**branch if PS=1 or ZF=1	1110 m	1011 m	EB mm		PC(7~0) ← mm if PS ∨ ZF=1
	BCZ	**branch if CF=1 or ZF=1	1110 m	0111 m	E7 mm		PC(7~0) ← mm if CF ∨ ZF=1
	BPCZ	**branch if PS=1, CF=1 or ZF=1	1110 m	1111 m	EF mm		PC(7~0) ← mm if PS ∨ CF ∨ ZF=1
	BNP	**branch if PS=0	1110 m	1000 m	E8 mm		PC(7~0) ← mm if PS=0
	BNC	**branch if CF=0	1110 m	0100 m	E4 mm		PC(7~0) ← mm if CF=0
	BNZ	**branch if ZF=0	1110 m	0010 m	E2 mm		PC (7 ~ 0) ← mm if ZF=0
	BNPC	**branch if PS=0 and CF=0	1110 m	1100 m	EC mm		PC(7~0) ← mm if PS ∨ CF=0
	BNPZ	**branch if PS=0 and ZF=0	1110 m	1010 m	EA mm		PC(7~0) ← mm if PS ∨ ZF=0
	BNCZ	**branch if CF=0 and ZF=0	1110 m	0110 m	E6 mm		PC(7~0) ← mm if CF ∨ ZF=0
	BNPCZ	**branch if PS=0, CF=0 and ZF=0	1110 m	1110 m	EE mm		PC(7~0) ← mm if PS ∨ CF ∨ ZF=0
	JMP	**jump	0100 m	0 p m	4 p mm		PC(10~8) ← p, PC(7~0) ← mm
	CAL	**call	0100 m	1 p m	4(8+p) mm		STACK ← PC + 2 PC(10~8) ← p, PC(7~0) ← mm
	RET	return	0001	1111	1F		PC(10~0) ← STACK
	EC	enable counter	0001	1101	1D		E/D ← 1
	DC	disable counter	0001	1100	1C		E/D ← 0
	NOP	no operation	0000	0000	00		

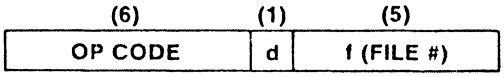
Instruction Code		Mnemonic	Action
0	0000	NOPO	No change in registers. RR → RR, Flag O → ⎍
1	0001	LD	Load result register. Data → RR
2	0010	LDC	Load complement. $\overline{\text{Data}}$ → RR
3	0011	AND	Logical AND. RR·Data → RR
4	0100	ANDC	Logical AND complement. RR·$\overline{\text{Data}}$ → RR
5	0101	OR	Logical OR. RR + Data → RR
6	0110	ORC	Logical OR complement. RR + $\overline{\text{Data}}$ → RR
7	0111	XNOR	Exclusive NOR. If RR = Data, RR → 1
8	1000	STO	Store. RR → Data Pin, Write → ⎍
9	1001	STOC	Store complement. $\overline{\text{RR}}$ → Data Pin, Write → ⎍
A	1010	IEN	Input enable. Data → IEN Register
B	1011	OEN	Output enable. Data → OEN Register
C	1100	JMP	Jump. JMP Flag → ⎍
D	1101	RTN	Return. RTN Flag → ⎍ and skip next instruction
E	1110	SKZ	Skip next instruction if RR = 0
F	1111	NOPF	No change in registers. RR → RR, Flag F → ⎍

Instruction Set Summary

For an oscillator frequency of 1MHz, the instruction execution time is 4 μsec, except if a conditional test is true or if the PC register is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

In the following PIC instruction descriptions "k" represents an eight bit constant or literal value, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register, if "d" is one, the result is returned to the file register specified in the instruction. If the "d" operand is omitted, the f register is assumed as the destination. "f" and "d" may be numbers, characters, or symbols as described in the PIC Assembler and PIC Simulator instructions. "C" represents the carry bit, "Z" represents the zero bit, and "DC" represents the digit carry bit.

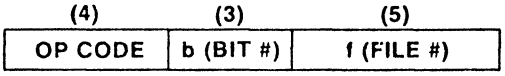
GENERAL FILE REGISTER OPERATIONS



for d = 0, f→W
d = 1, f→f

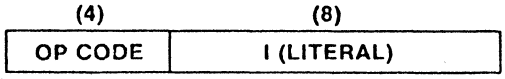
Instruction (Octal)				Name	Syntax		Operation	Status
000000	0	00000	(0000)	No Operation	NOP	—	—	—
000000	1	fffff	(0040)	Move W to f *	MOVWF	f	W→f	—
000001	0	fffff	(0100)	Clear W	CLRW	—	O→W	Z
000001	1	fffff	(0140)	Clear f	CLRF	f	O→f	Z
000010	d	fffff	(0200)	Subtract W from f	SUBWF	f, d	f - W→d	C,DC,Z
000011	d	fffff	(0300)	Decrement f	DECF	f, d	f - 1→d	Z
000100	d	fffff	(0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000101	d	fffff	(0500)	AND W and f	ANDWF	f, d	W∧f→d	Z
000110	d	fffff	(0600)	Exclusive OR W and f	XORWF	f, d	W∀f→d	Z
000111	d	fffff	(0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001000	d	fffff	(1000)	Move f	MOVF	f, d	f→d	Z
001001	d	fffff	(1100)	Complement f	COMF	f, d	$\bar{f}$→d	Z
001010	d	fffff	(1200)	Increment f	INCF	f, d	f+1→d	Z
001011	d	fffff	(1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	—
001100	d	fffff	(1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001101	d	fffff	(1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001110	d	fffff	(1600)	Swap halves f	SWAPF	f, d	f(0-3)⇄f(4-7)→d	—
001111	d	fffff	(1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	—

BIT LEVEL FILE REGISTER OPERATIONS



Instruction (Octal)				Name	Syntax		Operation	Status
0100	bbb	fffff	(2000)	Bit Clear f	BCF	f, b	0→f(b)	—
0101	bbb	fffff	(2400)	Bit Set f	BSF	f, b	1→f(b)	—
0110	bbb	fffff	(3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b); skip if clear	—
0111	bbb	fffff	(3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b); skip if set	—

LITERAL AND CONTROL OPERATIONS



Instruction (Octal)			Name	Syntax		Operation	Status
1000	k k k k k k k k	(4000)	Return	RET	—	0 → W, RAR → PC	—
1000	k k k k k k k k	(4000)	Return and place Literal in W	RETLW	k	k → W, RAR → PC	—
1001	k k k k k k k k	(4400)	Call subroutine *	CALL	k	PC → RAR, k→ PC	—
101x	k k k k k k k k	(5X00)**	Go To address	GOTO	k	k → PC	—
1100	k k k k k k k k	(6000)	Move Literal to W	MOVLW	k	k→W	—
1101	k k k k k k k k	(6400)	Inclusive OR Literal and W	IORLW	k	kVW→W	Z
1110	k k k k k k k k	(7000)	AND Literal and W	ANDLW	k	kAW→W	Z
1111	k k k k k k k k	(7400)	Exclusive OR Literal and W	XORLW	k	k∀W→W	Z

*The 9th bit of the program counter in the PIC1650 is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in page 0. However, subroutines can be called from page 0 or page 1 since the RAR is 9 bits wide. (Page 0: 0-255. Page 1: 256-511).
**If X = 0, the address is in page 0; if X = 1, the address is in page 1. The PIC assembler takes care of assigning the correct op codes.

Cont'd on next page

IS74 Cont'd

IS74 Cont'd

OTHER INSTRUCTION MNEMONICS REGONIZED BY THE PIC1650 ASSEMBLER

Instruction (Octal)	Name	Syntax	Equivalent Operation(s)	Status
0100 000 00011 (2003)	Clear Carry	CLRC	BCF3, 0	—
0101 000 00011 (2403)	Set Carry	SETC	BSF3,0	—
0100 001 00011 (2043)	Clear Digit Carry	CLRDC	BCF3,1	—
0101 001 00011 (2443)	Set Digit Carry	SETDC	BSF3,1	—
0100 010 00011 (2103)	Clear Zero	CLRZ	BCF3, 2	—
0101 010 00011 (2503)	Set Zero	SETZ	BSF3,2	—
0111 000 00011 (3403)	Skip on Carry	SKPC	BTFSS3,0	—
0110 000 00011 (3003)	Skip on No Carry	SKPNC	BTFSC3,0	—
0111 001 00011 (3443)	Skip on Digit Carry	SKPDC	BTFSS3,1	—
0110 001 00011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC3, 1	—
0111 010 00011 (3503)	Skip on Zero	SKPZ	BTFSS3, 2	—
0110 010 00011 (3103)	Skip on No Zero	SKPNZ	BTFSC3, 2	—
001000 1 f f f f f (1040)	Test File	TSTF f	MOVF f, 1	Z
001000 0 f f f f f (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001001 1 f f f f f (1140) 001010 d f f f f f (1200)	Negate File	NEGF, f,d	COMF f, 1 INCF f, d	Z
011000 0 00011 (3003) 001010 d f f f f f (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011000 0 00011 (3003) 000011 d f f f f f (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011000 1 00011 (3043) 001010 d f f f f f (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011000 1 00011 (3043) 000011 d f f f f f (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101× kkkkkkkk (5×00)	Branch	B K	GO TO K	—
0110 00000011 (3003) 101× kkkkkkkk (5×00)	Branch on Carry	BC K	BTFSC 3,0 GO TO K	—
0111 00000011 (3403) 101× kkkkkkkk (5×00)	Branch on No Carry	BNC K	BTFSS 3,0 GO TO K	—
0110 00100011 (3043) 101× kkkkkkkk (5×00)	Branch on Digit Carry	BDC K	BTFSG 3,1 GO TO K	—
0111 00100011 (3443) 101× kkkkkkkk (5×00)	Branch on No Digit Carry	BNDC K	BTFSS 3,1 GO TO K	—
0110 01000011 (3103) 101× kkkkkkkk (5×00)	Branch on Zero	BZ K	BTFSC 3,2 GO TO K	—
0111 01000011 (3503) 101× kkkkkkkk (5×00)	Branch on No Zero	BNZ K	BTFSS 3,2 GO TO K	—

if × = 0, address is in page 0.
if × = 1, address is in page 1.

8041/8741

UPI INSTRUCTION SET

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
ADD A,Rr	Add register to A	1	1
ADD A,@Rr	Add data memory to A	1	1
ADD A,#data	Add immediate to A	2	2
ADDC A,Rr	Add immed. to A with carry	1	1
ADDC A,@Rr	Add immed. to A with carry	1	1
ADDC A,#data	Add immed. to A with carry	2	2
ANL A,Rr	AND register to A	1	1
ANL A,@Rr	AND data memory to A	1	1
ANL A,#data	AND immediate to A	2	2
ORL A,Rr	OR register to A	1	1
ORL A,@Rr	OR data memory to A	1	1
ORL A,#data	OR immediate to A	2	2
XRL A,Rr	Exclusive OR register to A	1	1
XRL A,@Rr	Exclusive OR data memory to A	1	1
XRL A,#data	Exclusive OR immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal Adjust A	1	1
SWAP A	Swap digits of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
INPUT/OUTPUT			
IN A,Pp	Input port to A	1	2
OUTL Pp,A	Output A to port	1	2
ANL Pp,#data	AND immediate to port	2	2
ORL Pp,#data	OR immediate to port	2	2
IN A,DBB	Input DBB to A, clear IBF	1	1
OUT DBB,A	Output A to DBB, set OBF	1	1
MOVD A,Pp	Input Expander port to A	1	2
MOVD Pp,A	Output A to Expander port	1	2
ANLD Pp,A	AND A to Expander port	1	2
ORLD Pp,A	OR A to Expander port	1	2
DATA MOVES			
MOV A,Rr	Move register to A	1	1
MOV A,@Rr	Move data memory to A	1	1
MOV A,#data	Move immediate to A	2	2
MOV Rr,A	Move A to register	1	1
MOV @Rr,A	Move A to data memory	1	1
MOV Rr,#data	Move immediate to register	2	2
MOV @Rr,#data	Move immediate to data memory	2	2
MOV A,PSW	Move PSW to A	1	1
MOV PSW,A	Move A to PSW	1	1
XCH A,Rr	Exchange A and register	1	1
XCH A,@Rr	Exchange A and data memory	1	1
XCHD A,@Rr	Exchange digit of A and register	1	1
MOVP A,@A	Move to A from current page	1	2
MOVP3 A,@A	Move to A from page 3	1	2
TIMER/COUNTER			
MOV A,T	Read Timer/Counter	1	1
MOV T,A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/Counter Interrupt	1	1
DIS TCNTI	Disable Timer/Counter Interrupt	1	1

Mnemonic	Description	Bytes	Cycles
CONTROL			
EN I	Enable IBF Interrupt	1	1
DIS I	Disable IBF Interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
NOP	No Operation	1	1
REGISTERS			
INC Rr	Increment register	1	1
INC @Rr	Increment data memory	1	1
DEC Rr	Decrement register	1	1
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
FLAGS			
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear F1 Flag	1	1
CPL F1	Complement F1 Flag	1	1
BRANCH			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R,addr	Decrement register and skip	2	2
JC addr	Jump on Carry = 1	2	2
JNC addr	Jump on Carry = 0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 Flag = 1	2	2
JF1 addr	Jump on F1 Flag = 1	2	2
JTF addr	Jump on Timer Flag = 1, Clear Flag	2	2
JNIBF addr	Jump on IBF Flag = 0	2	2
JOBF addr	Jump on OBF Flag = 1	2	2
JBb addr	Jump on Accumulator Bit	2	2

REGISTER AND MEMORY INSTRUCTIONS

INSTRUCTION MNEMONIC						IMMEDIATE 2 BYTES					FLAG STATUS	DESCRIPTION OF OPERATION
						MEMORY						
INSTR	MODIFIER	REGISTER A	B	C	D	E	H	L	H,L M	I		
LDA	x	7F	78	79	7A	7B	7C	7D	7E	3E		Load with register x
LDB	x	47	40	41	42	43	44	45	46	06		
LDC	x	4F	48	49	4A	4B	4C	4D	4E	0E		
LDD	x	57	50	51	52	53	54	55	56	16		
LDE	x	5F	58	59	5A	5B	5C	5D	5E	1E		
LDH	x	67	60	61	62	63	64	65	66	26		
LDL	x	6F	68	69	6A	6B	6C	6D	6E	2E		
LDM	x	77	70	71	72	73	74	75		36		Load memory with x
INC	x	3C	04	0C	14	1C	24	2C	34		d,z,s,p	Increment register
DEC	x	3D	05	0D	15	1D	25	2D	35		d,z,s,p	Decrement register
ADA	x	87	80	81	82	83	84	85	86	C6	c,d,z,s,p	Add to A
ADC	x	8F	88	89	8A	8B	8C	8D	8E	CE	c,d,z,s,p	Add to A W/C
SUA	x	97	90	91	92	93	94	95	96	D6	c,d,z,s,p	Sub from A
SUC	x	9F	98	99	9A	9B	9C	9D	9E	DE	c,d,z,s,p	Sub from A W/C
AND	x	A7	A0	A1	A2	A3	A4	A5	A6	E6	C0,D0,z,s,p	And with A
XRA	x	AF	A8	A9	AA	AB	AC	AD	AE	EE	C0,D0,z,s,p	Exclusive or with A
ORA	x	B7	B0	B1	B2	B3	B4	B5	B6	F6	C0,D0,z,x,p	Or with A
CPA	x	BF	B8	B9	BA	BB	BC	BD	BE	FE	c,d,z,s,p	Compare with A
CLB		AF	0 → C, 0 → A								C0,D0,Z1,S0,P1	Clear A and carry
CLC		B7	0 → C								C0,D0,z,s,p	Clear carry
CMC		3F	$\overline{C}$ → C								c	Complement carry
CMA		2F	$\overline{A}$ → A									Complement A
SEC		37	1 → C								C1	Set carry
DAA		27	C = ?, Cy = ?								c,d,z,s,p	Decimal adjust A
RRC		0F	A1 → C; A1 → A8								c	Rotate A right
RAL		17	A8 → C → A1								c	Rotate A left W/C
RAR		1F	A1 → C → A8								c	Rotate A right W/C
RLC		07	A8 → C; A8 → A1								c	Rotate A left
STAD		32	A → M						3 Bytes			Store A direct
LDAD		3A	M → A									Load A direct

3 Byte Instructions: Byte 2 = Lower Order Address
Byte 3 = Higher Order Address

PROGRAM ADDRESS CONTROL INSTRUCTIONS

INSTRUCTION MNEMONIC		FLAG CONDITIONS, Cx									DESCRIPTION OF OPERATION	
			≥	≠			: <	=			ARITHMETIC	
INSTR	MODIFIER	UN	CO	ZO	SO	PO	C1	Z1	S1	P1	LOGICAL	
JMP	Cx	C3	D2	C2	F2	E2	DA	CA	FA	EA	Jump on Condition	3 BYTE INSTR.
JSR	Cx	CD	D4	C4	F4	E4	DC	CC	FC	EC	Jump to Subroutine	
RET	Cx	C9	D0	C0	F0	E0	D8	C8	F8	E8	Return on Condition	

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REGISTER AND MEMORY INSTRUCTIONS

INSTRUCTION MNEMONIC		REGISTER							IMMEDIATE 2 BYTES / MEMORY		FLAG STATUS	DESCRIPTION OF OPERATION
INSTR	MODIFIER	A	B	C	D	E	H	L	H,L M	I		
LDA	x	7F	78	79	7A	7B	7C	7D	7E	3E		
LDB	x	47	40	41	42	43	44	45	46	06		
LDC	x	4F	48	49	4A	4B	4C	4D	4E	0E		
LDD	x	57	50	51	52	53	54	55	56	16		Load with register x
LDE	x	5F	58	59	5A	5B	5C	5D	5E	1E		
LDH	x	67	60	61	62	63	64	65	66	26		
LDL	x	6F	68	69	6A	6B	6C	6D	6E	2E		
LDM	x	77	70	71	72	73	74	75		36		Load memory with x
INC	x	3C	04	0C	14	1C	24	2C	34		d,z,s,p	Increment register
DEC	x	3D	05	0D	15	1D	25	2D	35		d,z,s,p	Decrement register
ADA	x	87	80	81	82	83	84	85	86	C6	c,d,z,s,p	Add to A
ADC	x	8F	88	89	8A	8B	8C	8D	8E	CE	c,d,z,s,p	Add to A W/C
SUA	x	97	90	91	92	93	94	95	96	D6	c,d,z,s,p	Sub from A
SUC	x	9F	98	99	9A	9B	9C	9D	9E	DE	c,d,z,s,p	Sub from A W/C
AND	x	A7	A0	A1	A2	A3	A4	A5	A6	E6	C0,D0,z,s,p	And with A
XRA	x	AF	A8	A9	AA	AB	AC	AD	AE	EE	C0,D0,z,s,p	Exclusive or with A
ORA	x	B7	B0	B1	B2	B3	B4	B5	B6	F6	C0,D0,z,x,p	Or with A
CPA	x	BF	B8	B9	BA	BB	BC	BD	BE	FE	c,d,z,s,p	Compare with A
CLB		AF	0 → C, 0 → A								C0,D0,Z1,S0,P1	Clear A and carry
CLC		B7	0 → C								C0,D0,z,s,p	Clear carry
CMC		3F	$\overline{C}$ → C								c	Complement carry
CMA		2F	$\overline{A}$ → A									Complement A
SEC		37	1 → C								C1	Set carry
DAA		27	C = ?, Cy = ?								c,d,z,s,p	Decimal adjust A
RRC		0F	A1 → C; A1 → A8								c	Rotate A right
RAL		17	A8 → C → A1								c	Rotate A left W/C
RAR		1F	A1 → C → A8								c	Rotate A right W/C
RLC		07	A8 → C; A8 → A1								c	Rotate A left
STAD		32	A → M						3 Bytes			Store A direct
LDAD		3A	M → A									Load A direct

3 Byte Instructions: Byte 2 = Lower Order Address
Byte 3 = Higher Order Address

PROGRAM ADDRESS CONTROL INSTRUCTIONS

INSTRUCTION MNEMONIC		FLAG CONDITIONS, Cx									DESCRIPTION OF OPERATION	
INSTR	MODIFIER		≥	≠			: <	=			ARITHMETIC	
		UN	CO	ZO	SO	PO	C1	Z1	S1	P1	LOGICAL	
JMP	Cx	C3	D2	C2	F2	E2	DA	CA	FA	EA	Jump on Condition	3 BYTE INSTR.
JSR	Cx	CD	D4	C4	F4	E4	DC	CC	FC	EC	Jump to Subroutine	
RET	Cx	C9	D0	C0	F0	E0	D8	C8	F8	E8	Return on Condition	

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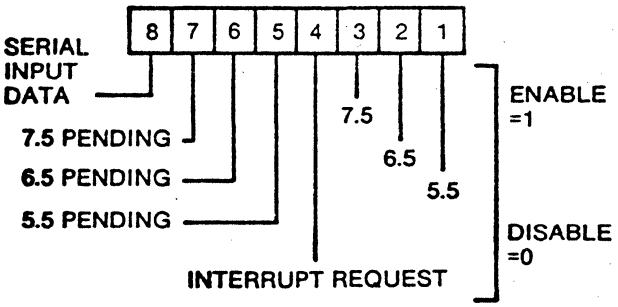
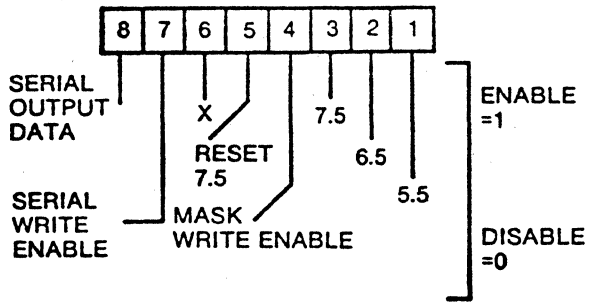
REGISTER A AFTER RIM

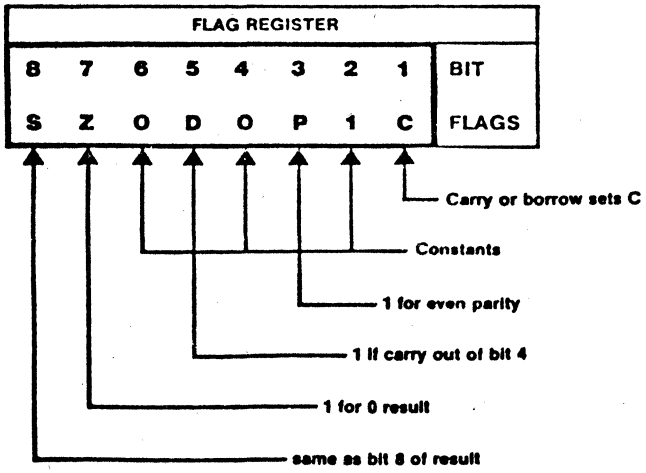


REGISTER A FOR SIM



MACHINE INSTRUCTIONS

	4 TIME STATES	5 TIME STATES							
NOP		00	7F	40	49	52	5B	64	6D	No operation
HLT		76								Halt



AUTOMATIC MEMORY OPERATIONS

PSP, JSR, RST :	Page at (SP-1) Line at (SP-2)
PLP, RET :	Line from (SP) Page from (SP + 1)
XTHL :	L ↔ (SP) H ↔ (SP + 1)
LHLD **SHLD** :	(L) ↔ (ADR) (H) ↔ (ADR + 1)

INSTRUCTION MNEMONIC	OP CODE	FORMATS	DESCRIPTION	I/O CONTROL SIGNALS	→ INSTRUCTION CYCLE → Instruction Input and Data Processing	→ INSTRUCTION CYCLE → Address/IV Bus Output
MOVE	0	Register to Register 0 2 3 7 8 10 11 15 0 | S | R | D S≠07,17,20-37$_8$ D≠10,20-37$_8$	(S) → D Move contents of register specified by S to register specified by D. Right rotate contents of register S by R places before operation.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RB =	0 0 X X	1 if D = 07,17 0 1 if D = 17 0 if D = 07
		IV Bus to Register: 0 2 3 7 8 10 11 15 0 | S | L | D S=20-37$_8$ D≠10,20-37$_8$	Move right rotated IV bus (source) data specified by S to register specified by D. L specifies the length of source data with most significant bits set to zero.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RB =	0 0 0 if S = 20-27 1 if S = 30-37	1 if D = 07,17 0 1 if D = 17 0 if D = 07
		Register to IV Bus: 0 2 3 7 8 10 11 15 0 | S | L | D S≠07,17,20-37$_8$ D=20-37$_8$	Move contents of register specified by S to the IV bus. Before placement on IV bus, data is shifted as specified by D, and L bits merged with destination IV bus data.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RB =	0 0 0 if D = 20-27 1 if D = 30-37	0 1 0 if D = 20-27 1 if D = 30-37
		IV Bus to IV Bus: 0 2 3 7 8 10 11 15 0 | S | L | D S=20-37$_8$ D=20-37$_8$	Move right rotated IV bus data (sources) specified by S to the IV bus. Before placement on IV bus, data is shifted or specified by D and merged with original source data. L specifies the length of source data to be operated on.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RB =	0 0 0 if S = 20-27 1 if S = 30-37	0 1 0 if D = 20-27 1 if D = 30-37
ADD	1	SAME AS MOVE	(S) plus (AUX) → D Same as MOVE but contents of AUX added to the source data. If carry from most significant bit then OVF = 1, otherwise OVF = 0		SAME AS MOVE	
AND	2	SAME AS MOVE	(S)∧(AUX) → D Same as MOVE but contents of AUX ANDed with source data.		SAME AS MOVE	
XOR	3	SAME AS MOVE	(S) ⊕ (AUX) → D Same as MOVE but contents of AUX exclusive ORed with source data.		SAME AS MOVE	
XEC	4	Register Immediate: 0 2 3 7 8 15 4 | S | I S≠07,17,20-37$_8$ I=000-377$_8$	Execute instruction at current page address offset by I + (S). Execute the instruction at the address determined by concatenating 5 high order bits of PC with the 8 bit sum of I and register specified by S. PC is not incremented.	SC = WC = $\overline{LB}$/RB	0 0 x	0 0 x
		IV Bus Immediate: 0 2 3 7 8 10 11 15 4 | S | L | I S=20-37$_8$ I=00-37$_8$	Execute the instruction at the address determined by concatenating 8 high order bits of PC with the 5 bit sum of I and rotated IV bus data (source) specified by S. R/L specifies length of source data with most significant bits set to zero. PC is not incremented.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RB =	0 0 0 if S = 20-27 1 if S = 30-37	0 0 x x

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IS78 Cont'd

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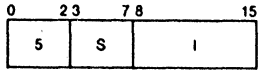
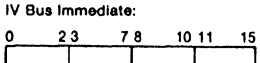
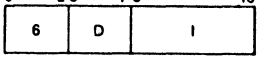
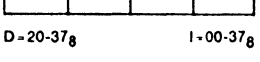
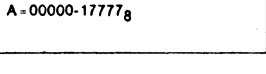
INSTRUCTION MNEMONIC	OP CODE	FORMATS	DESCRIPTION	I/O CONTROL SIGNALS	← INSTRUCTION CYCLE → Instruction Input and Data Processing	Address IV Bus Output
NZT	5	Register Immediate:  $S \neq 07,17,20\text{-}37_8$ $I = 000\text{-}377_8$	If (S) = 0, jump to current page address offset by I; if S = 0, PC + 1 → PC If contents of register specified by S is non zero then transfer to address determined by concatenating 5 high order bits of PC with I; if contents of register specified by S is zero, increment PC.	SC = WC = $\overline{LB}$/RB =	0 0 x	0 0 x
		IV Bus Immediate:  $S = 20\text{-}37_8$ $I = 00\text{-}37_8$	If right rotated IV bus data (source) is Non Zero then Transfer to address determined by concatenating 8 high order bits of PC with I; if contents of register specified by S is zero, increment PC.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RB =	0 0 0 if S = 20-27 1 if S = 30-37	0 0 x x
XMIT	6	Register Immediate:  $D \neq 10, 20\text{-}37_8$ $I = 000\text{-}377_8$	Transmit I → D Transmit and store 8 bit binary pattern I to register specified by D.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RD =	0 0 x x	1 if D = 07,17 0 1 if D = 17 0 if D = 07
		IV BUS IMMEDIATE  $D = 20\text{-}37_8$ $I = 00\text{-}37_8$	Transmit binary pattern I to IV bus. Before placement on IV bus, literal I is shifted as specified by D and L bits merged with existing IV bus data.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RB =	0 0 0 if D = 20-27 1 if D = 30-37	0 1 0 if D = 20-27 1 if D = 30-37
JMP	7	Address Immediate:  $A = 00000\text{-}17777_8$	Jump to Program Address A Jump to program storage address A. A is stored in the address register (AR).	SC = WC = $\overline{LB}$/RB =	0 0 x	0 0 x

ROM ADDRESSING INSTRUCTIONS

MNEMONIC	OPERATION	NO. OF CYCLES
NOP	No operation	1
JMP X	Jump to location x within present page if previous instruction was not a PP or to location x on page defined by previous PP. X → LR. PPR → PR if previous instruction was a PP. PBR → BR if previous instruction was a PP. NOTE: The last instruction on a ROM page cannot be a JMP or JMS.	1
JMS X	Jump to subroutine at location x. LR + 1 → L Stack, PR → P Stack, X → LR (The stack is 3 levels deep.) 15 → PR if previous instruction was not a PP, PPR → PR if previous instruction was a PP. NOTE: The last instruction in a ROM page cannot be a JMP or a JMS.	2
RT	Return from subroutine, L Stack → LR, P Stack → PR	1
RTS	*Return from subroutine and skip 1 instruction. L Stack → LR, P Stack → PR, then skip.	1+n (≥ 2)
PP X	*Prepare page or bank. X → PP if previous instruction was not a PP (0 ≤ X ≤ F). X → PB if previous instruction was a PP (0 ≤ X ≤ 7).	1

*SKIP INSTRUCTIONS (SEE ALSO RTS, ADIS, ADCS, XCI, AND XCD)

SZC	*Skip if carry bit = 0.	1+n
SZM Z	*Skip if RAM bit Z = 0. Z selects bit of RAM word addressed by BL and BU. Z = 0 to 3.	1+n
SOS	*Skip if "sec FF" = 1 (Timer output is tested). If skip is performed the "sec FF" is reset to 0.	1+n
SZK	*Skip if key input selected by last executed LAI is a 0.	1+n
SZI	*Skip if I input selected by last executed LAI is a 0.	1+n
SBE	*Skip if BL = E.	1+n
SAM	*Skip if ACC = RAM (RAM and ACC remain un changed).	1+n
TF1	*Test Flag #1 and skip if flag is set.	1+n
TF2	*Test Flag #2 and skip if flag is set.	1+n

ARITHMETIC AND LOGICAL INSTRUCTIONS

ADIS X	*Add X to ACC and skip if sum ≤ 15. CARRY unaltered X + ACC → ACC.	1+n
ADCS	*Add RAM to ACC and CARRY, and skip if sum ≤ 15. RAM + ACC + CARRY → ACC, CARRY. If sum ≤ 15, 0 → CARRY. If sum > 15, 1 → CARRY.	1+n
ADD	Add RAM to ACC, CARRY unaltered, ACC + RAM → ACC.	1
AND	Logical AND of ACC and RAM, ACC ∧ RAM → ACC	1
XOR	Logical EXCLUSIVE OR of ACC and RAM, ACC ⊕ RAM → ACC.	1
STC	Set CARRY to 1	1
RSC	Reset CARRY to 0	1
CMA	Complement ACC, $\overline{ACC}$ → ACC.	1
SF1	Set flag #1	1
RF1	Reset flag #1	1
SF2	Set flag #2	1
RF2	Reset flag #2	1

REGISTER INSTRUCTIONS

LAI X	Load ACC immediate. Only the first LAI in a sequence is executed. K or I inputs selected by ones in binary form of X. X → ACC and X → K or I select. (X = 0 to 15).	1
LAB	Load ACC from BL register. BL → ACC.	1
LAE	Load ACC from E register. E → ACC.	1
XAB	Exchange ACC and BL. BL ↔ ACC.	1
XABU	Exchange ACC and BU. ACC most significant 2 bits are not changed. BU (1, 0) ↔ ACC (1, 0). ACC (2, 3) remain unchanged.	1
XAE	Exchange ACC and E register. ACC ↔ E.	1
***	Denotes an LB instruction. Only the first LB of a sequence is executed.	
LBE Y	***Load BL with E and BU with Y. Y → BU (Y = 0 to 3), E → BL.	1
LBZ Y	***Load BL with 0 and BU with Y. 0 → BL, Y → BU (Y = 0 to 3).	1
LBF Y	***Load BL with 15 and BU with Y. 15 → BL, Y → BU (Y = 0 to 3).	1
LBEP Y	***Load BL with E + 1 and BU with Y. E + 1 → BL, Y → BU (Y = 0 to 3).	1

RAM INSTRUCTIONS

MNEMONIC	OPERATION	NO. OF CYCLES
LAM Y	Load ACC from RAM, then modify BU. RAM → ACC, BU ⊕ Y → BU (Sec 2-2).	1
XC Y	Exchange ACC and RAM, then modify BU. RAM ↔ ACC, BU ⊕ Y → BU (Sec 2-2).	1
XCI Y	*Exchange ACC and RAM, increment BL, then modify BU and skip if BL = 0 after incrementing. ACC ↔ RAM, BL + 1 → BL, BU ⊕ Y → BU (Section 2-2).	1+n
XCD Y	*Exchange ACC and RAM, decrement BL, then modify BU, and skip if BL was 0 prior to decrementing. ACC ↔ RAM, BL - 1 → BL, BU ⊕ Y → BU (Section 2-2).	1+n
STM Z	Set RAM bit to a 1. RAM word addressed by BL and BU registers. 1 → RAM bit Z (Z = 0 to 3).	1
RSM Z	Reset RAM bit to a 0. RAM word addressed by BL and BU registers. 0 -- RAM bit Z (Z = 0 to 3).	1

I/O INSTRUCTIONS

INP	INPut data to ACC and RAM. DO - D3 → ACC, D4 - D7 → RAM.	1
OUT	OUTPut ACC and RAM to D lines. Generate $\overline{EXT}$ signal at T7. Display Latch remains unchanged. ACC → DO - D3, RAM → D4 - D7.	1
DISN	Encode ACC and store in Display Latch (DISplay Number). ACC → SEGMENT DECODER → DISPLAY LATCH. Exit from floating mode on D lines. IF CARRY = 1, D7 (DECIMAL POINT) = 1.	1
DISB	Output ACC and RAM to Display Latch. ACC → DISPLAY LATCH (0 - 3) → DO - D3, RAM → DISPLAY LATCH (4 - 7) → D4 - D7.	1
MVS	Move A-line Master Strobe Latch contents to Slave Latch (output). Enter floating mode on D lines.	1
PSH	Preset HIGH, Master Strobe Latch bit pointed to by BL register. BL 0 to 12: Set Latch bit 0 to 12. BL = 13: Multiplex operation. BL = 14: Exit D lines from float. BL = 15: Set all Master Strobe Latch bits to a 1.	1
PSL	Preset LOW, Master Strobe Latch bit pointed to by BL register. BL 0 to 12: Reset Latch bit 0 to 12. BL = 13: Static operation. BL = 14: Float D lines. BL = 15: Reset all Master Strobe Latch bits to a 0.	1
EUR	(EURopean). Set 50/60HZ and Display Latch output polarities, according to the argument of the last executed LAI instruction, as follows: LS ACC BIT = 1: NORMAL POLARITY/DISPLAY LATCH LS ACC BIT = 0: INVERTED POLARITY/DISPLAY LATCH MS ACC BIT = 1: 50HZ OPERATION/TIMER MS ACC BIT = 0: 60HZ OPERATION/TIMER	

*Skips, when invoked, skip the very next instruction; whenever that skipped instruction is a PP (Prepare Page) however, the next instruction is skipped as well. n= the number of instructions that are skipped.

INSTRUCTION SET

①	②	③	④
CMA	1	$A_{CC} \leftarrow (\overline{A_{CC}})$	
CIA	1	$A_{CC} \leftarrow (\overline{A_{CC}})+1$	
INA	1/2	$A_{CC} \leftarrow (A_{CC})+1$	Carry=1
DEA	1/2	$A_{CC} \leftarrow (A_{CC})-1$	Borrow≠1
RFC	1	C←0	
SFC	1	C←1	
DSM	1	Decimal Subtract Mode	
DAM	1	Decimal Add Mode	
AD	1/2	$A_{CC} \leftarrow (A_{CC})+[DP]$	Carry=1
ADC	1	$A_{CC},C \leftarrow (A_{CC})+[DP]+(C)$	
ADI	1/2	$A_{CC} \leftarrow (A_{CC})+I_3I_2I_1I_0$	Carry=1
LM	1	$A_{CC} \leftarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2M_1M_0$	
XM	1	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2M_1M_0$	
XMI	1/2	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2M_1M_0$ $DP_L \leftarrow (DP_L)+1$	$(DP_L)=8$ or $(DP_L)=0$
XMD	1/2	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2M_1M_0$ $DP_L \leftarrow (DP_L)-1$	$(DP_L)=F$ or $(DP_L)=7$
LI	1	$A_{CC} \leftarrow I_3I_2I_1I_0$	
LDI	1	$DP \leftarrow I_6-I_0$	
IND	1/2	$DP_L \leftarrow (DP_L)+1$	$(DP_L)=8$ or $(DP_L)=0$
DED	1/2	$DP_L \leftarrow (DP_L)-1$	$(DP_L)=F$ or $(DP_L)=7$
XDP	1	(DP)↔(DP')	
ZAG	1	$000DP_L \leftarrow (DP)$	

①	②	③	④
XTA	1	$(A_{CC}) \leftrightarrow (TR)$	
LTI	1	$TR \leftarrow I_3I_2I_1I_0$	
QS1	1	$Q_{n+1} \leftarrow Q_n, Q_0 \leftarrow 1$	
QS0	1	$Q_{n+1} \leftarrow Q_n, Q_0 \leftarrow 0$	
SB	1	$[DP,B_1,B_0] \leftarrow 1$	
RB	1	$[DP,B_1,B_0] \leftarrow 0$	
SBT	1/2	Skip if $[DP,B_1,B_0]=1$	$B_1B_0=1$
SC	1/2	Skip if (C)=1	(C)=1
SEM	1/2	Skip if $(A_{CC})=[DP]$	$(A_{CC})=[DP]$
SEI	1/2	Skip if $(A_{CC})=I_3I_2I_1I_0$	$(A_{CC})=I_3I_2I_1I_0$
SK4	1/2	Skip if $K_4=1$	$K_4=1$
JPT	1	$PC \leftarrow (TR), P_{6-0}$	
JPA	1	$PC_{6-4} \leftarrow P_{6-4}$ $PC_{3-0} \leftarrow P_{3-0} \vee (A_{CC})$	
JCP	1	$PC_{6-0} \leftarrow P_{6-0}$	
CAL	1	$[STACK] \leftarrow (PC)$ $PC \leftarrow 1000P_6P_5P_4P_3P_2P_1P_0$	
RT	1	PC←[STACK]	
RTS	2	PC←[STACK] PC←(PC)+1	
EIA	1	Enable IA port	
DIA	1	Disable IA port	
EIB	1	Enable IB port	
DIB	1	Disable IB port	
OIU	1	$U_{7-0} \leftarrow I_{7-0}$ $R_{7-0} \leftarrow (Q_{7-0})$	
ERO	1	Enable R port	
DRO	1	Disable R port	

①	②	③
OQR	1	R←(Q)
OTR	1	$R_{7-4} \leftarrow (TR), R_{3-0} \leftarrow (DP_L)$
SFS	1	S←(A_{CC})
RFS	1	S port Input Mode
IS	1	$A_{CC} \leftarrow S$
IK	1	$A_{CC} \leftarrow K$
RF1	1	$F_1 \leftarrow 0$
SF1	1	$F_1 \leftarrow 1$
RF2	1	$F_2 \leftarrow 0$
SF2	1	$F_2 \leftarrow 1$
RF3	1	$F_3 \leftarrow 0$
SF3	1	$F_3 \leftarrow 1$
RF4	1	$F_4 \leftarrow 0$
SF4	1	$F_4 \leftarrow 1$
RF5	1	$F_5 \leftarrow 0$
SF5	1	$F_5 \leftarrow 1$
RF6	1	$F_6 \leftarrow 0$
SF6	1	$F_6 \leftarrow 1$
RF7	1	$F_7 \leftarrow 0$
SF7	1	$F_7 \leftarrow 1$
RF8	1	$F_8 \leftarrow 0$
SF8	1	$F_8 \leftarrow 1$
RF9	1	$F_9 \leftarrow 0$
SF9	1	$F_9 \leftarrow 1$
RF0	1	$F_0 \leftarrow 0$
SF0	1	$F_0 \leftarrow 1$
NOP	1	No Operation

Notes: ① **MNEMONIC**
② **CYCLES**
③ **DESCRIPTION**
④ **CONDITION FOR SKIP**

INSTRUCTION SETS

①	②	③	④	⑤
CLA	1	1	$A_{CC} \leftarrow 0$	
CMA	1	1	$A_{CC} \leftarrow \overline{(A_{CC})}$	
CIA	1	1	$A_{CC} \leftarrow \overline{(A_{CC})}+1$	
INC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+1$ skip if Carry	Carry
DEC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})-1$ skip if Borrow	Borrow
CLC	1	1	$C \leftarrow 0$	
STC	1	1	$C \leftarrow 1$	
* XC	1	1	$(C) \rightleftharpoons (C')$	
* RAR	1	1	$(A_{CCn-1}) \leftarrow (A_{CCn})$ $C \leftarrow (A_{CC0})$, $(A_{CC3}) \leftarrow (C)$	
* INM	1	1/2-3	$[(DP)] \leftarrow [(DP)]+1$ skip if $[(DP)]=0$	$[(DP)]=0$
* DEM	1	1/2-3	$[(DP)] \leftarrow [(DP)]-1$ skip if $[(DP)]=F$	$[(DP)]=F$
AD	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+[(DP)]$ skip if Carry	Carry
ADS	1	1/2-3	$A_{CC}, C \leftarrow (A_{CC})+[(DP)]+(C)$ skip if Carry	Carry
ADC	1	1	$A_{CC}, C \leftarrow (A_{CC})+[(DP)]+(C)$	
DAA	1	1	$A_{CC} \leftarrow (A_{CC})+6$	
DAS	1	1	$A_{CC} \leftarrow (A_{CC})+10$	
EXL	1	1	$A_{CC} \leftarrow (A_{CC}) \forall [(DP)]$	
LI	1	1	$A_{CC} \leftarrow I_3 I_2 I_1 I_0$	
S	1	1	$[(DP)] \leftarrow (A_{CC})$	
L	1	1	$A_{CC} \leftarrow [(DP)]$	
LM	1	1	$A_{CC} \leftarrow [(DP)]$ $DP_H \leftarrow (DP_H) \forall 0 M_1 M_0$	
X	1	1	$(A_{CC}) \rightleftharpoons [(DP)]$	
XM	1	1	$(A_{CC}) \rightleftharpoons [(DP)]$ $DP_H \leftarrow (DP_H) \forall 0 M_1 M_0$	
XD	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$ $DP_L \leftarrow (DP_L)-1$ skip if $(DP_L)=F$	$(DP_L)=F$
XMD	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$ $DP_H \leftarrow (DP_H) \forall 0 M_1 M_0$ $DP_L \leftarrow (DP_L)-1$ skip if $(DP_L)=F$	$(DP_L)=F$

①	②	③	④	⑤
XI	1	1/2-3	$(A_{CC}) \leftarrow [(DP)]$ $DP_L \leftarrow (DP_L)+1$ skip if $(DP_L)=0$	$(DP_L)=0$
XMI	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$ $DP_H \leftarrow (DP_H) \forall 0 M_1 M_0$ $DP_L \leftarrow (DP_L)+1$ skip if $(DP_L)=0$	$(DP_L)=0$
LDI	2	2	$DP \leftarrow I_6 - I_0$	
LDZ	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3 I_2 I_1 I_0$	
DED	1	1/2-3	$DP_L \leftarrow (DP_L)-1$ skip if $(DP_L)=F$	$(DP_L)=F$
IND	1	1/2-3	$DP_L \leftarrow (DP_L)+1$ skip if $(DP_L)=0$	$(DP_L)=0$
TAL	1	1	$DP_L \leftarrow (A_{CC})$	
TLA	1	1	$A_{CC} \leftarrow (DP_L)$	
* XHX	1	2	$(X) \rightleftharpoons (DP_H)$	
* XLY	1	2	$(Y) \rightleftharpoons (DP_L)$	
* THX	1	2	$X \leftarrow (DP_H)$	
* TLY	1	2	$Y \leftarrow (DP_L)$	
* XAZ	1	2	$(Z) \rightleftharpoons (A_{CC})$	
* XAW	1	2	$(W) \rightleftharpoons (A_{CC})$	
* TAZ	1	2	$Z \leftarrow (A_{CC})$	
* TAW	1	2	$W \leftarrow (A_{CC})$	
* XHR	1	2	$(R) \rightleftharpoons (DP_H)$	
* XLS	1	2	$(S) \rightleftharpoons (DP_L)$	
SMB	1	1	$[(DP, B_1B_0)] \leftarrow 1$	
RMB	1	1	$[(DP, B_1B_0)] \leftarrow 0$	
TMB	1	1/2-3	skip if $[(DP, B_1B_0)]=1$	$[(DP, B_1B_0)]=1$
TAB	1	1/2-3	skip if $(A_{CC}(B_1B_0))=1$	$(A_{CC}(B_1B_0))=1$
CMB	1	1/2-3	skip if $(A_{CC}(B_1B_0))$ $=[(DP, B_1B_0)]$	$(A_{CC}(B_1B_0))$ $=[(DP, B_1B_0)]$
* SFB	1	2	FLAG $(B_1B_0) \leftarrow 1$	
* RFB	1	2	FLAG $(B_1B_0) \leftarrow 0$	
* FBT	1	2/3-4	skip if (FLAG $(B_1B_0))=1$	(FLAG$(B_1B_0))=1$
* FBF	1	2/3-4	skip if (FLAG $(B_1B_0))=0$	(FLAG$(B_1B_0))=0$
CM	1	1/2-3	skip if $(A_{CC})=[(DP)]$	$(A_{CC}) = [(DP)]$
CI	2	2/3-4	skip if $(A_{CC})=I_3 I_2 I_1 I_0$	$(A_{CC})=I_3 I_2 I_1 I_0$
CLI	2	2/3-4	skip if $(DP_L)=I_3 I_2 I_1 I_0$	$(DP_L)=I_3 I_2 I_1 I_0$

①	②	③	④	⑤
TC	1	1/2-3	skip if (C)=1	(C)=1
TIT	1	1/2-3	skip if (INT F/F)=1 INT F/F←0	(INT F/F)=1
JCP	1	1	$PC_{5-0} \leftarrow P_5 - P_0$	
JMP	2	2	$PC \leftarrow P_{10} - P_0$	
JPA	1	2	$PC_{5-0} \leftarrow A_3 A_2 A_1 A_0 00$	
* EI	1	1	INTE F F←1	
* DI	1	1	INTE F F←0	
CZP	1	1	STACK←(PC) $PC \leftarrow 00000 P_3 P_2 P_1 P_0 00$	
CAL	2	2	STACK←(PC) $PC \leftarrow P_{10} - P_0$	
RT	1	2	PC←(STACK)	
RTS	1	3-4	PC←(STACK) PC←(PC)+1,2	Unconditional
* STM	2	2	TM F F←0 TIMER←$I_5 - I_0$	
* TTM	1	1/2-3	skip if (TM F/F)=1	(TM F/F)=1
SEB	1	2	PORT E $(B_1B_0) \leftarrow 1$	
REB	1	1	PORT E $(B_1B_0) \leftarrow 0$	
SPB	1	1	PORT $(DP_L, B_1B_0) \leftarrow 1$	
RPB	1	1	PORT $(DP_L, B_1B_0) \leftarrow 0$	
TPA	1	2/3-4	skip if (PORT A $(B_1B_0))=1$	(PORT A $(B_1B_0))$ $= 1$
TPB	1	1/2-3	skip if (PORT $(DL_L, B_1B_0))$ $=1$	(PORT $(DP_L$, $B_1B_0))=1$
OE	1	2	PORT E←(A_{CC})	
OP	1	1	PORT $(DP_L) \leftarrow (A_{CC})$	
OCD	2	2	PORT C,D←$I_7 - I_0$	
IA	2	2	$A_{CC} \leftarrow$(PORT A)	
IP	1	1	$A_{CC} \leftarrow$(PORT (DP_L))	
NOP	1	1	No Operation	

Notes: ① MNEMONIC
② BYTES
③ CYCLES
④ DESCRIPTION
⑤ CONDITION FOR SKIP
* These Instructions Apply Only to the μCOM-43. (IS81a)

IS83 **IS83**

GENERIC: IS83 - 6500

IS83 - 6500/I

IS83 - 6500 without "ROR"

INSTRUCTION SET

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS. X			ABS. Y			RELATIVE			INDIRECT			Z. PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← [7 … 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2								• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2								• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2								• • • • • • • •	BEQ
BIT	A∧M				2C	4	3	24	3	2																																M_7 M_6• • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2								• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2								• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2								• • • • • • • •	BPL
BRK	BREAK (See Fig. 1)													00	7	1																									• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2								• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2								• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • • •	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																																N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																																N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB (See Fig 2)				20	6	3																																		• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → [7 … 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	← [7 … 0] ← [C] ←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	→ [C] → [7 … 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT (See Fig 1)													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB (See Fig 2)													60	6	1																									• • • • • • • •	RTS
SBC	A − M − C → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																														96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																	• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													98	2	1																									N • • • • • Z •	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED

(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT = BORROW

(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD	M_7	MEMORY BIT 7
Y	INDEX Y		SUBTRACT	M_6	MEMORY BIT 6
A	ACCUMULATOR	∧	AND	n	NO. CYCLES
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR	#	NO. BYTES
Ms	MEMORY PER STACK POINTER	∀	EXCLUSIVE OR		

NOTE: Instruction "BRK" Applicable to IS83a only

"DEX" Not applicable to IS83b

"DEY" Not applicable to IS83b

"ROR" Not applicable to IS83b

OPERATION FORM, COMMAND FORMAT, AND TEST OUTPUTS

OPERATION FORM		COMMAND FORMAT												TEST OUTPUTS							
														MSP		ALL		$\overline{MSP}$		MSP	$\overline{MSP}$
NO.	OPERATION	OP0 (7)[1]	OP1 (8)	OP2 (9)	OP3 (10)	OP4 (17)	OP5 (14)	OP6 (13)	OP7 (11)	OP8 (15)	OP9 (16)	LSP $\overline{CIN}$ (18)		LG (21)	AG (20)	EQ (23)	$\overline{COUT}$ (22)	X (21)	Y (20)	OVFL (37)	$\overline{CCO}$ (37)
IA	(↑A + B + $\overline{CIN}$) · Σ' BUS ONLY[2]	H	L	L	A SOURCE		B SOURCE			A' FNCT	B' FNCT	L = CARRY		Σ' ≠ ZERO	Σ' > ZERO	Σ' ZERO	$\overline{COUT}$	X[4]	Y[4]	OVFL	$\overline{CCO}$
IB	(↑A + B + CIN) · REGISTER	L	REGISTER		LL = AI − A		LLL = BI · B			L A · A'	L B · B'	H = NO									
			LL = Σ' − WR		LH = H'S − A		LLH = H'S · B			H A · A'	H B · B'	CARRY									
			LH = Σ' − XWR		HL = BI − A		LHL = BI · WR · B														
			HL = Σ' − PC		HH = WR − A		LHH = WR · B														
			HH = Σ' − MC				HLL = BI · XWR · B														
							HLH = XWR − B														
							HHL = BI · PC − B														
							HHH = PC − B														
IIA	(A + B + $\overline{CIN}$) ↳ WR, XWR[2]	H	H	H	L	H	L	FUNCT	B' SRC	A' SRC	SHIFT	L = SUB		Σ' ≠ ZERO	Σ' > ZERO	Σ' ZERO	$\overline{COUT}$	X	Y	OVFL	$\overline{CCO}$
IIB	(B − A − 1) ↳ WR, XWR	H	H	H	L	H	L	L = A − A'	L = BI − B'	L = AI − A'	L = LFT	H = ADD									
								H = Ā − A'	H = WR · B'	H = BI − A'	H = RT										
III	(A + B + $\overline{CIN}$) ↳ REGISTER	H	H	L	H	A' SRC	REGISTER	B' SOURCE		SHIFT	TYPE	L CARRY		Σ' ≠ ZERO	Σ' > ZERO	Σ' ZERO	$\overline{COUT}$	X	Y	OVFL	$\overline{CCO}$
						L = AI − A'	L = Σ' − MC	LL = BI − B'		L = LOG	L = LFT	H NO		*DURING ARITHMETIC SHIFTS A' + C IS COMPARED TO −1							
						H = BI − A'	H = Σ' − XWR	LH = WR − B'		H = ARITH	H = RT	CARRY								SHIFT	
								HL = XWR − B'						Σ' ≠ 1	Σ' > 1	Σ' 1	$\overline{COUT}$	X	Y	OVFL	$\overline{CCO}$
								HH = L'S − B'													
IV	AI ↳ Σ' BUS	H	H	H	L	H	H	REG OR AI		SHIFT		TYPE		AI ≠ ZERO	AI > ZERO	AI ZERO	$\overline{CIN}$	X	Y	L	$\overline{CCO}$
								LL = AI ↳ Σ'		LL LOG		L LFT								(FOR	
VA	WR ↳ WR	H	H	H	L	H	H	LH WR ↳ WR		LH ARITH		H RT								LSA	
VB	XWR ↳ XWR	H	H	H	L	H	H	HL XWR ↳ XWR		HL ROTATE										OVFL)	
VI	WR, XWR ↳ WR, XWR	H	H	H	L	H	H	HH = WR XWR · WR XWR		HH (NOT DEFINED)											
VIIA	A B (N1 N2)	H	H	H	L	L	B' SOURCE			A' SRC	OPER	H		N1 > N2	N1 N2	N1 N2	LG	X	Y		$\overline{CCO}$
VIIB	B A (N1 N2)	H	H	H	L	L	(SAME AS FORM I ABOVE)			L AI · A'	L A B										
										H WR · A'	H B A										
VIIIA	NOR/AND LOGICAL OPERATIONS	H	FUNCTION			A' SRC	REG[1]	B SOURCE		A' FNCT	B' FNCT	REG[1]		Σ' ≠ ZERO	Σ' > ZERO	Σ' ZERO	$\overline{CIN}$	X	Y	L	$\overline{CCO}$
VIIIB	OR/NAND LOGICAL OPERATIONS	H	LHL = NOR			L = AI − A	LL = WR	LL = BI − B		L = A − A'	L = B − B'	(SEE									
VIIIC	EX OR/EX NOR LOGICAL OPERATIONS	H	LHH = OR			H = WR − A	LH = XWR	LH = WR − B		H = Ā − A'	H B − B'	UNDER									
			HLL = XOR				HL = PC	HL = XWR − B				OP5									
							HH = Σ'	HH = PC − B				COLUMN)									
IX	NO OPERATION (ZERO → Σ' BUS)	H	H	H	H	H	H or L	H or L	H or L	H or L	H or L	H or L		L	L	H	$\overline{CIN}$	X	Y	L	$\overline{CCO}$
X	CRC ACCUMULATION	H	H	H	H	L	L	L	L	L	O/I[5]	H						X	Y	L	$\overline{CCO}$
XI	SIGNED INTEGER DIVIDE — A. START	H	H	H	H	L	L	H	L	H	H	H				DIV ZERO					
	B. ITERATE (N 1 CLKS)	H	H	H	H	L	H	L	H	O/I[6]	O/I[6]	H									
	C. ITERATE FINISH	H	H	H	H	L	H	H	L	O/I[6]	O/I[6]	H									
	D. FIX REMAINDER	H	H	H	H	L	H	L	L	O/I[6]	O/I[6]	H									
	E. ADJUST QUOTIENT	H	H	H	H	L	L	H	H	O/I[6]	O/I[6]	H									
XII	UNSIGNED DIVIDE — A. START	H	H	H	H	L	L	L	L	H	H	L			DIV OVFL						
	B. ITERATE (N 1 CLKS)	H	H	H	H	L	L	L	H	H	O/I[6]	L									
	C. FINISH	H	H	H	H	L	L	L	H	L	O/I[6]	L									
XIII	UNSIGNED MULTIPLY	H	H	H	H	L	L	H	L	L	O/I[6]	H									
XIV	SIGNED INTEGER MULTIPLY	H	H	H	H	L	H	H	H	O/I[6]	O/I[6]	H									

AO SEL (42)
L MC
H PC

DO1 SEL (29)
DO2 SEL (30)
LL Σ' BUS
LH WR
HL XWR
HH HI Z

BI O SEL (29)
L OUTPUT
H INPUT

$\overline{LD\ WR}$ (24)
L AI · WR
H NO LOAD

INC $\overline{MC}$ (35)
L INC
H HOLD

$\overline{INC\ PC}$ (43)
L INC
H HOLD

$\overline{CCI}$ (44)
LSP L: x 1
LSP H: x 2
MID OR MSP
L CARRY
H NO CARRY

POS (19)
0 V MID
2.4 V LSP
5 V MSP

PIN NUMBER	DATA PORTS AI	BI/O	DOP	AOP	BIT (2^n)
	(6)	(46)	(34)	(38)	0 (LSB)
	(5)	(47)	(33)	(39)	1
	(4)	(1)	(32)	(40)	2
	(3)	(2)	(31)	(41)	3 (MSB)

PIN ASSIGNMENTS

WRRT (26)	CK (45)
WRLFT (25)	V_{CC} (12)
XWRRT (28)	GND (36)
XWRLFT (27)	

NOTES
1. NUMERALS IN PARENTHESIS ARE PIN NUMBERS
2. − DESTINED FOR ↳ SHIFTED AND DESTINED FOR
3. H = HIGH VOLTAGE LEVEL, L = LOW VOLTAGE LEVEL
4. X AND Y ARE CARRY LOOK AHEAD FUNCTIONS
5. O IS OUTPUT ON LSP, I IS INPUT ON $\overline{LSP}$
6. O IS OUTPUT ON MSP, I IS INPUT ON $\overline{MSP}$
7. VOLTAGE VALUES ARE NOMINAL

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS86

IS86

CMA	00	1011	0111	1	A←($\bar{A}$)		
INA	00	0110	0001	½	Acc←(Acc)+1	Carry=1	
DEA	00	0110	1111	½	Acc←(Acc)−1	Borrow≠1	
RAL	00	1111	1111	1	A_0←C, C←A_3 A_{n+1}←A_n		
SFC	00	0001	0011	1	C←1		
RFC	00	0001	0010	1	C←0		
MMM	00	0010	1010	1	MF←0		
SMM	00	0010	1000	1	MF←1		
SMR	00	1000	0011	1	MR←(Acc)		
QOM	00	1000	0010	1	QF←(Acc)		
DSM	00	1011	1001	1	Decimal Subtract Mode		
DAM	00	1011	1101	1	Decimal Add Mode		
AD	00	1011	1110	½	Acc←(Acc)+[(DP)]	Carry=1	
ADNC	00	1011	1010	½	Acc←(Acc)+[(DP)]	Carry=0	
ADC	00	1011	1111	1	Acc, C←(Acc)+[(DP)]+(C)		
ADI	00	0110	$I_3I_2I_1I_0$	½	Acc←(Acc)+I_{3-0}	Carry=1	
TSM	00	1010	0111	1	DB←[SM]		
TMS	00	1010	0110	1	SM←DB		
TSMI	00	1010	0101	½	DB←[SM], DP_L←(DP_L)+1	(DP_L)=0	
TMSI	00	1010	0100	½	SM←DB, DP_L←(DP_L)+1	(DP_L)=0	
S	00	1000	0111	1	[(DP)]←(Acc)		
SI	00	1000	0101	½	[(DP)]←(Acc), DP_L←(DP_L)+1	(DP_L)=0	
XMI	00	1101	01 M_1M_0	⅔	[(DP)]←(Acc), DP_M←(DP_M)∨M_1M_0, DP_L←(DP_L)+1	(DP_L)=0	
XMD	00	1101	00 M_1M_0	⅔	[(DP)]←(Acc), DP_M←(DP_M)∨M_1M_0, DP_L←(DP_L)−1	(DP_L)=F	
XM	00	1100	01 M_1M_0	2	[(DP)]←(Acc), DP_M←(DP_M)∨M_1M_0		
LM	00	1100	00 M_1M_0	1	Acc←[(DP)], DP_M←(DP_M)∨M_1M_0		
LLI*	01	0011	$I_3I_2I_1I_0$	1	DP_L←I_{3-0}		
LHMI*	01	01 I_5I_4	$I_3I_2I_1I_0$	1	$DP_{H,M}$←I_{5-0}		
LI*	01	0010	$I_3I_2I_1I_0$	1	Acc←I_{3-0}		
IND	00	1011	0100	½	DP_L←(DP_L)+1	(DP_L)=0	
DED	00	1011	0000	½	DP_L←(DP_L)−1	(DP_L)=F	
TLA	00	1111	0000	1	Acc←(DP_L)		
TMA	00	1111	0010	1	Acc←(DP_M)		
THA	00	1111	0011	1	00 A_1A_0←(DP_H)		
TAL	00	1001	0000	1	DP_L←(Acc)		
TAM	00	1001	0010	1	DP_M←(Acc)		
TAH	00	1001	0011	1	DP_H←($Acc_{1,0}$)		
ZAG	00	1011	0001	1	$DP_{H,M}$ Zero Mask		
SDP n	00	1110	00 I_1I_0	3	MM←(DP) n=I_1I_0		
LDP n	00	1010	00 I_1I_0	3	DP←[MM] n=I_1I_0		
LRI n	00	0100	$I_3I_2I_1I_0$	1	RPT←I_{3-0} n=$I_3I_2I_1I_0$		
LRA	00	1000	0000	1	RPT←(Acc)		
LPI* n	01	000 I_4	$I_3I_2I_1I_0$	1	P←I_{4-0}		
TSPA	00	1111	0001	1	Acc←(SP)		
TASP	00	1001	0001	1	SP←(Acc)		
TPAC	00	1111	0100	1	C←(P_4), Acc←(P_{3-0})		
TACP	00	1001	0100	1	P_4←(C), P_{3-0}←(Acc)		
SU	00	0000	0101	1	U←1		
RU	00	0000	0001	1	U←0		
SAB n	00	0010	01 B_1B_0	1	A_n←1 n=B_1B_0		
RAB n	00	0010	00 B_1B_0	1	A_n←0 n=B_1B_0		

SABT n	00	1000	11 B_1B_0	½	Skip if A_n=1 n=B_1B_0	A_n=1	
SABF n	00	1000	10 B_1B_0	½	Skip if A_n=0 n=B_1B_0	A_n=0	
SBT n	00	1010	11 B_1B_0	½	Skip if $[(DP)]_n$=1 n=B_1B_0	$[(DP)]_n$=1	
SFT n	00	1101	11 B_1B_0	½	Skip if F_n=1 n=B_1B_0	F_n=1	
SFF n	00	1101	10 B_1B_0	½	Skip if F_n=0 n=B_1B_0	F_n=0	
SQT n	00	1100	11 B_1B_0	½	Skip if Q_n=1 n=B_1B_0	Q_n=1	
SQF n	00	1100	10 B_1B_0	½	Skip if Q_n=0 n=B_1B_0	Q_n=0	
SEM	00	1011	1100	½	Skip if (Acc)=[(DP)]	(Acc) =[(DP)]	
SNEM	00	1011	1000	½	Skip if (Acc)≠[(DP)]	(Acc) ≠[(DP)]	
SC	00	1111	1100	½	Skip if (C)=1	(C)=1	
SNC	00	1111	1000	½	Skip if (C)=0	(C)=0	
SUT	00	1111	1110	½	Skip if (U)=1	(U)=1	
SUF	00	1111	1010	½	Skip if (U)=0	(U)=0	
SLEI	00	0101	$I_3I_2I_1I_0$	½	Skip if (DP_L)=I_{3-0}	(DP_L)=I_{3-0}	
SEI	00	0111	$I_3I_2I_1I_0$	½	Skip if (Acc)=I_{3-0}	(Acc)=I_{3-0}	
JPA	00	1000	0100	1	PC_{11-7}←(P), PC_{6-4}←0, PC_{3-0}←(Acc)		
JCP	11	0 $I_6I_5I_4$	$I_3I_2I_1I_0$	1	PC_{6-0}←I_{6-0}		
JPP	11	1 $I_6I_5I_4$	$I_3I_2I_1I_0$	1	PC_{11-7}←(P), PC_{6-0}←I_{6-0}		
CAL	10	0 $I_6I_5I_4$	$I_3I_2I_1I_0$	3	[(SP)]←(PC), SP←(SP)+1, PC_{11-7}←1, PC_{6-0}←I_{6-0}		
CALP	10	1 $I_6I_5I_4$	$I_3I_2I_1I_0$	3	[(SP)]←(PC), SP←(SP)+1, PC_{11-7}←(P), PC_{6-0}←I_{6-0}		
RT	01	1111	1110	3	SP=(SP)−1, PC←[(SP)]		
RTS	01	1111	1111	4	SP←(SP)−1, PC←[(SP)], PC←(PC)+1		
EIA	00	0000	1001	1	Enable INT_A		
EIB	00	0000	1010	1	" INT_B		
EIAB	00	0000	1011	1	" $INT_{A,B}$		
EIT	00	0000	1000	1	" INT_T		
DIA	00	0000	1101	1	Disable INT_A		
DIB	00	0000	1110	1	" INT_B		
DIAB	00	0000	1111	1	" $INT_{A,B}$		
DIT	00	0000	1100	1	" INT_T		
SCM n	00	1110	10 I_1I_0	1	MM_n←(U), (MF), (C) n=I_1I_0		
LCM n	00	1010	10 I_1I_0	1	U, MF, C←$[MM]_n$ n=I_1I_0		
STM	00	1000	0001	1	TM_H←(Acc)		
OUT	00	1001	0101	1	DB←(Acc)		
IN	00	1111	0101	1	Acc←DB		
IK	00	0001	0101	1	K←K_{3-0}		
IS	00	0001	0110	1	S←S_{3-0}		
IKS	00	0001	0100	1	K←K_{3-0}, S←S_{3-0}		
LK	00	1111	0111	1	Acc←(K)		
LS	00	1111	0110	1	Acc←(S)		
SK	00	1001	0111	1	K←(Acc)		
SS	00	1001	0110	1	S←(Acc)		
SF n	00	0011	I_3 1 I_1I_0	1	F_n←1 n=$I_3I_1I_0$		
RF n	00	0011	I_3 0 I_1I_0	1	F_n←0 n=$I_3I_1I_0$		
SQ n	00	0001	11 I_1I_0	1	Q_n←1 n=I_1I_0		
RQ n	00	0001	10 I_1I_0	1	Q_n←0 n=I_1I_0		
SR	00	0000	0011	1	R_n←1 n=(DP_L)		
RR	00	0000	0010	1	R_n←0 n=(DP_L)		
CPMI	00	1011	0101	1	Compare (Acc) and [(DP)], R_n←1/0, DP_L←(DP_L)+1		
SBF	00	0001	0001	1	Set Bus Floating		
RBF	00	0001	0000	1	Reset Bus Floating		
NOP	00	0000	0000	1	No Operation		

INSTRUCTIONS

The following symbols and abbreviations are used in the subsequent description of μCOM-83 instructions:

SYMBOLS	MEANING
SR	(Staus Register)
BSD (SR_7)	External RAM Bank Select Flag
EXT IE (SR_6)	External Interrupt Enable Flag
T/C IE (SR_5)	T/C Interrupt Enable Flag
Q0 IE (SR_4)	Q0 Interrupt Enable Flag
F (SR_3)	Software Flag
C (SR_2)	Carry Flag
AC (SR_1)	Auxiliary Carry Flag
ZF (SR_0)	Zero Flag
PMR	(Peripheral Mode Flag)
BSP (PMR_7)	External ROM Bnak Select Flag
MUL (PMR_3)	Multiplication Flag
DIV (PMR_2)	Division Flag
CM1 (PMR_1)	Counter Mode Flag
CM0 (PMR_0)	
R	8-bit R Register
SP	8-bit Stack Pointer Register
Q	8-bit Q Register
PC	12-bit Program Counter Register (PC_H and PC_L are used to refer to the high-order 4 bits and low-order 8 bits respectively).
I	8-bit Immediate data quantity

SYMBOLS	MEANING
addr	8-bit or 16-bit address quantity
B_2	The Second byte of the instruction
B_3	The Third byte of the instruction
@	Indirect addressing mode
d	R Register number 0 through 2
i	Q Register number 0 through 3
j	D Register number 0 through 3
n	Bit n of the Register or data,. or Zero Page Subroutine Call number 0 through 7
[X]	The content addressed by X enclosed in the parentheses
(X)	The content of X enclosed in the parentheses
^	Logical AND
v	Inclusive OR
v	Exclusive OR
+	Addition
—	The one's complement (e.g., $(\bar{A})$
←	"Is transferred to"

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IS87 Cont'd

IS87 Cont'd

① Mnemonic
② Object code
③ Bytes
④ Cycles
⑤ Description

①	②			③	④	⑤
MULT	0 1 0 0 1 0 0 1			1	2	MUL←1
DIV	0 1 0 0 0 0 0 1			1	2	DIV←1
INC @Rd	1 0 0 0 0 0 d_1 d_0			1	3	(Rd)←(Rd)+1
INCM addr	1 0 0 0 0 0 1 1	B_2		2	4	(B_2)←(B_2)+1
DEC @Rd	1 0 0 0 0 1 d_1 d_0			1	3	(Rd)←(Rd)−1
DECM addr	1 0 0 0 0 1 1 1	B_2		2	4	(B_2)←(B_2)−1
CMPL @Rd	1 0 0 0 1 0 d_1 d_0			1	3	(Rd)←$\overline{(Rd)}$
CMPLM addr	1 0 0 0 1 0 1 1	B_2		2	4	(B_2)←$\overline{(B_2)}$
DA @Rd	1 0 0 0 1 1 d_1 d_0			1	4	Decimal Adjust (Rd)
DAM addr	1 0 0 0 1 1 1 1	B_2		2	5	Decimal Adjust (B_2)
ANLD addr	1 0 1 1 0 0 0 0	B_2		2	5	(B_2)←(B_2)∧(R0)
ANL @R0, @R1	1 0 1 1 0 0 0 1			1	4	(R0)←(R0)∧(R1)
ANL @R0, @R2	1 0 1 1 0 0 1 0			1	4	(R0)←(R0)∧(R2)
ANLM @R0, addr	1 0 1 1 0 0 1 1	B_2		2	5	(R0)←(R0)∧(B_2)
ANL @R1, @R0	1 0 1 1 0 1 0 0			1	4	(R1)←(R1)∧(R0)
ANLI @R0, I	1 0 1 1 0 1 0 1	B_2		2	4	(R0)←(R0)∧B_2
ANL @R1, @R2	1 0 1 1 0 1 1 0			1	4	(R1)←(R1)∧(R2)
ANLDI addr, I	1 0 1 1 0 1 1 1	B_2	B_3	3	5	(B_2)←(B_2)∧B_3
ANL @R2, @R0	1 0 1 1 1 0 0 0			1	4	(R2)←(R2)∧(R0)
ANL @R2, @R1	1 0 1 1 1 0 0 1			1	4	(R2)←(R2)∧(R1)
ANLA0	1 0 1 1 1 0 1 0			1	4	(R0)←(R0)∧(R1), R0←(R0)+1
ANLA1	1 0 1 1 1 0 1 1			1	4	(R0)←(R0)∧(R1), R1←(R1)+1
ANLA	1 0 1 1 1 1 0 0			1	4	(R0)←(R0)∧(R1), R0←(R0)+1 R1←(R1)+1

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IS87 Cont'd

IS87 Cont'd

① Mnemonic
② Object code
③ Bytes
④ Cycles
⑤ Description

①	②			③	④	⑤
ORLD addr	1 1 0 0 0 0 0 0	B_2		2	5	$(B_2) \leftarrow (B_2) \vee (R0)$
ORL @R0, @R1	1 1 0 0 0 0 0 1			1	4	$(R0) \leftarrow (R0) \vee (R1)$
ORL @R0, @R2	1 1 0 0 0 0 1 0			1	4	$(R0) \leftarrow (R0) \vee (R2)$
ORLM @R0, addr	1 1 0 0 0 0 1 1	B_2		2	5	$(R0) \leftarrow (R0) \vee (B_2)$
ORL @R1, @R0	1 1 0 0 0 1 0 0			1	4	$(R1) \leftarrow (R1) \vee (R0)$
ORLI @R0, I	1 1 0 0 0 1 0 1	B_2		2	4	$(R0) \leftarrow (R0) \vee B_2$
ORL @R1, @R2	1 1 0 0 0 1 1 0			1	4	$(R1) \leftarrow (R1) \vee (R2)$
ORLDI addr, I	1 1 0 0 0 1 1 1	B_2	B_3	3	5	$(B_2) \leftarrow (B_2) \vee B_3$
ORL @R2, @R0	1 1 0 0 1 0 0 0			1	4	$(R2) \leftarrow (R2) \vee (R0)$
ORL @R2, @R1	1 1 0 0 1 0 0 1			1	4	$(R2) \leftarrow (R2) \vee (R1)$
ORLA0	1 1 0 0 1 0 1 0			1	4	$(R0) \leftarrow (R0) \vee (R1)$, $R0 \leftarrow (R0)+1$
ORLA1	1 1 0 0 1 0 1 1			1	4	$(R0) \leftarrow (R0) \vee (R1)$, $R1 \leftarrow (R1)+1$
ORLA	1 1 0 0 1 1 0 0			1	4	$(R0) \leftarrow (R0) \vee (R1)$, $R0 \leftarrow (R0)+1$ $R1 \leftarrow (R1)+1$
XRLD addr	1 1 0 1 0 0 0 0	B_2		2	5	$(B_2) \leftarrow (B_2) \veebar (R0)$
XRL @R0, @R1	1 1 0 1 0 0 0 1			1	4	$(R0) \leftarrow (R0) \veebar (R1)$
XRL @R0, @R2	1 1 0 1 0 0 1 0			1	4	$(R0) \leftarrow (R0) \veebar (R2)$
XRLM @R0, addr	1 1 0 1 0 0 1 1	B_2		2	5	$(R0) \leftarrow (R0) \veebar (B_2)$
XRL @R1, @R0	1 1 0 1 0 1 0 0			1	4	$(R1) \leftarrow (R1) \veebar (R0)$
XRLI @R0, I	1 1 0 1 0 1 0 1	B_2		2	4	$(R0) \leftarrow (R0) \veebar B_2$
XRL @R1, @R2	1 1 0 1 0 1 1 0			1	4	$(R1) \leftarrow (R1) \veebar (R2)$
XRLDI addr, I	1 1 0 1 0 1 1 1	B_2	B_3	3	5	$(B_2) \leftarrow (B_2) \veebar B_3$
XRL @R2, @R0	1 1 0 1 1 0 0 0			1	4	$(R2) \leftarrow (R2) \veebar (R0)$
XRL @R2, @R1	1 1 0 1 1 0 0 1			1	4	$(R2) \leftarrow (R2) \veebar (R1)$
XRLA0	1 1 0 1 1 0 1 0			1	4	$(R0) \leftarrow (R0) \veebar (R1)$, $R0 \leftarrow (R0)+1$
XRLA1	1 1 0 1 1 0 1 1			1	4	$(R0) \leftarrow (R0) \veebar (R1)$, $R1 \leftarrow (R1)+1$
XRLA	1 1 0 1 1 1 0 0			1	4	$(R0) \leftarrow (R0) \veebar (R1)$, $R0 \leftarrow (R0)+1$ $R1 \leftarrow (R1)+1$
ADDD addr	1 1 1 0 0 0 0 0	B_2		2	5	$(B_2) \leftarrow (B_2)+(R0)$
ADD @R0, @R1	1 1 1 0 0 0 0 1			1	4	$(R0) \leftarrow (R0)+(R1)$
ADD @R0, @R2	1 1 1 0 0 0 1 0			1	4	$(R0) \leftarrow (R0)+(R2)$

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① Mnemonic
② Object code
③ Bytes
④ Cycles
⑤ Description

①	②			③	④	⑤
ADDM @R0, addr	11100011	B_2		2	5	(R0)←(R0)+(B_2)
ADD @R1, @R0	11100100			1	4	(R1)←(R1)+(R0)
ADDI @R0, I	11100101	B_2		2	4	(R0)←(R0)+B_2
ADD @R1, @R2	11100110			1	4	(R1)←(R1)+(R2)
ADDDI addr, I	11100111	B_2	B_3	3	5	(B_2)←(B_2)+B_3
ADD @R2, @R0	11101000			1	4	(R2)←(R2)+(R0)
ADD @R2, @R1	11101001			1	4	(R2)←(R2)+(R1)
ADDA0	11101010			1	4	(R0)←(R0)+(R1), R0←(R0)+1
ADDA1	11101011			1	4	(R0)←(R0)+(R1), R1←(R1)+1
ADDA	11101100			1	4	(R0)←(R0)+(R1), R0←(R0)+1 R1←(R1)+1
ADCD addr	11110000	B_2		2	5	(B_2)←(B_2)+(R0)+(C)
ADC @R0, @R1	11110001			1	4	(R0)←(R0)+(R1)+(C)
ADC @R0, R2	11110010			1	4	(R0)←(R0)+(R2)+(C)
ADCM @R0, addr	11110011	B_2		2	5	(R0)←(R0)+(B_2)+(C)
ADC @R1, @R0	11110100			1	4	(R1)←(R1)+(R0)+(C)
ADCI @R0, I	11110101	B_2		2	4	(R0)←(R0)+B_2+(C)
ADC @R1, @R2	11110110			1	4	(R1)←(R1)+(R2)+(C)
ADCDI addr, I	11110111	B_2	B_3	3	5	(B_2)←(B_2)+B_3+(C)
ADC @R2, @R0	11111000			1	4	(R2)←(R2)+(R0)+(C)
ADC @R2, @R1	11111001			1	4	(R2)←(R2)+(R1)+(C)
ADCA0	11111010			1	4	(R0)←(R0)+(R1)+(C), R0←(R0)+1
ADCA1	11111011			1	4	(R0)←(R0)+(R1)+(C), R1←(R1)+1
ADCA	11111100			1	4	(R0)←(R0)+(R1)+(C), R0←(R0)+1 R1←(R1)+1
RC	01000010			1	3	C←0
SC	01001010			1	3	C←1
RF	01000011			1	3	F←0
SF	01001011			1	3	F←1
RBSD	01000111			1	3	BSD←0
SBSD	01001111			1	3	BSD←1

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① Mnemonic
② Object code
③ Bytes
④ Cycles
⑤ Description

①	②			③	④	⑤
XCHS Rd	0 0 0 1 0 0 d_1 d_0			1	4	(Rd)↔(SP)
XCHM Rd, addr	0 0 0 1 1 0 d_1 d_0	B_2		2	5	(Rd)↔(B_2)
XCH01	0 0 0 1 1 1 0 0			1	4	(R0)↔(R1)
XCH12	0 0 0 1 1 1 0 1			1	4	(R1)↔(R2)
XCH02	0 0 0 1 1 1 1 0			1	4	(R0)↔(R2)
INC Rd	0 0 1 0 0 0 d_1 d_0			1	3	Rd←(Rd)+1
DEC Rd	0 0 1 0 0 1 d_1 d_0			1	3	Rd←(Rd)−1
MOVI Rd, I	0 0 1 0 1 0 d_1 d_0	B_2		2	3	Rd←B_2
ADDI Rd, I	0 0 1 0 1 1 d_1 d_0	B_2		2	4	Rd←(Rd)+B_2
PUSHR	0 0 0 1 0 1 0 0			1	4	(SP-1)←(R2), (SP-2)←(R1) (SP-3)←(R0), SP←(SP)−3
PUSH Rd	0 0 1 1 0 0 d_1 d_0			1	2	(SP-1)←(Rd), SP←(SP)−1
POPR	0 0 0 1 0 1 0 1			1	4	R0←(SP), R1←(SP+1) R2←(SP+2), SP←(SP)+3
POP Rd	0 0 1 1 0 1 d_1 d_0			1	2	Rd←(SP), SP←(SP)+1
STR addr	0 0 0 1 0 1 1 0	B_2		2	5	(B_2)←(R0), (B_2+1)←(R1) (B_2+2)←(R2)
ST Rd, addr	0 0 1 1 1 0 d_1 d_0	B_2		2	3	(B_2)←(Rd)
LDR addr	0 0 0 1 0 1 1 1	B_2		2	5	R0←(B_2), R1←(B_2+1) R2←(B_2+2)
LD Rd, addr	0 0 1 1 1 1 d_1 d_0	B_2		2	3	Rd←(B_2)
TR	0 0 0 0 0 1 0 0			1	4	(R0)←(PC_H, (R0))
MOVD addr	1 0 1 0 0 0 0 0	B_2		2	4	(B2)←(R0)
MOV @R0, @R1	1 0 1 0 0 0 0 1			1	3	(R0)←(R1)
MOV @R0, @R2	1 0 1 0 0 0 1 0			1	3	(R0)←(R2)
MOVM @R0, addr	1 0 1 0 0 0 1 1	B_2		2	4	(R0)←(B_2)
MOV @R1, @R0	1 0 1 0 0 1 0 0			1	3	(R1)←(R0)
MOVI @R0, I	1 0 1 0 0 1 0 1	B_2		2	3	(R0)←B_2
MOV @R1, @R2	1 0 1 0 0 1 1 0			1	3	(R1)←(R2)
MOVDI addr, I	1 0 1 0 0 1 1 1	B_2	B_3	3	4	(B_2)←B_3
MOV @R2, @R0	1 0 1 0 1 0 0 0			1	3	(R2)←(R0)
MOV @R2, @R1	1 0 1 0 1 0 0 1			1	3	(R2)←(R1)
MOVA0	1 0 1 0 1 0 1 0			1	3	(R0)←(R1), R0←(R0)+1
MOVA1	1 0 1 0 1 0 1 1			1	3	(R0)←(R1), R1←(R1)+1
MOVA	1 0 1 0 1 1 0 0			1	3	(R0)←(R1), R0←(R0)+1 R1←(R1)+1

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① Mnemonic
② Object code
③ Bytes
④ Cycles
⑤ Description

①	②			③	④	⑤
RL @Rd	1 0 0 1 0 0 d_1 d_0			1	3	$(Rd)_{n+1} \leftarrow (Rd)_n$, $C \leftarrow (Rd)_7$ ($n=0\sim6$) $(Rd)_0 \leftarrow (C)$
RLM addr	1 0 0 1 0 0 1 1	B_2		2	4	$(B_2)_{n+1} \leftarrow (B_2)_n$, $C \leftarrow (B_2)_7$ ($n=0\sim6$) $(B_2)_0 \leftarrow (C)$
RR @Rd	1 0 0 1 0 1 d_1 d_0			1	3	$(Rd)_n \leftarrow (Rd)_{n+1}$, $(Rd)_7 \leftarrow (C)$ ($n=0\sim6$) $C \leftarrow (Rd)_0$
RRM addr	1 0 0 1 0 1 1 1	B_2		2	4	$(B_2)_n \leftarrow (B_2)_{n+1}$, $(B_2)_7 \leftarrow (C)$ ($n=0\sim6$) $C \leftarrow (B_2)_0$
RLD @Rd	1 0 0 1 1 0 d_1 d_0			1	4	$(Q_3)_{3\sim0} \leftarrow (Rd)_{7\sim4}$, $(Rd)_{7\sim4} \leftarrow (Rd)_{3\sim0}$ $(Rd)_{3\sim0} \leftarrow (Q_3)_{3\sim0}$
RLDM addr	1 0 0 1 1 0 1 1	B_2		2	5	$(Q_3)_{3\sim0} \leftarrow (B_2)_{7\sim4}$, $(B_2)_{7\sim4} \leftarrow (B_2)_{3\sim0}$ $(B_2)_{3\sim0} \leftarrow (Q_3)_{3\sim0}$
SB$_n$ @Rd	0 1 0 1 0 1 1 1	B_2		2	4	$(Rd)_n \leftarrow 1$
SB$_n$ Q_i	0 1 0 1 0 1 1 1	B_2		2	4	$Q_{i,n} \leftarrow 1$
SB$_n$ PMR	0 1 0 1 0 1 1 1	B_2		2	4	$PMR_n \leftarrow 1$
RB$_n$ @Rd	0 1 0 1 0 1 1 1	B_2		2	4	$(Rd)_n \leftarrow 0$
RB$_n$ Q_i	0 1 0 1 0 1 1 1	B_2		2	4	$Q_{i,n} \leftarrow 0$
RB$_n$ PMR	0 1 0 1 0 1 1 1	B_2		2	4	$PMR_n \leftarrow 0$
RTNI	0 0 0 0 0 0 1 1			1	4	$SR \leftarrow (SP)$, $Q3_H$, $PC_H \leftarrow (SP+1)$ $PC_L \leftarrow (SP+2)$, $SP \leftarrow (SP)+3$
DIQ0	0 1 0 0 0 1 0 0			1	3	Q0IE←0
EIQ0	0 1 0 0 1 1 0 0			1	3	Q0IE←1
DITC	0 1 0 0 0 1 0 1			1	3	T/C IE←0
EITC	0 1 0 0 1 1 0 1			1	3	T/C IE←1
DIEXT	0 1 0 0 0 1 1 0			1	3	EXT IE←0
EIEXT	0 1 0 0 1 1 1 0			1	3	EXT IE←1
JMP addr	0 1 1 0 I_3 I_2 I_1 I_0	B_2		2	3	$PC_H \leftarrow I_3\ I_2\ I_1\ I_0$, $PC_L \leftarrow B_2$
JNZ addr	0 1 0 1 0 0 0 0	B_2		2	3	$PC_L \leftarrow B_2$ if(ZF)≠1
JZ addr	0 1 0 1 1 0 0 0	B_2		2	3	$PC_L \leftarrow B_2$ if(ZF)=1
JNAC addr	0 1 0 1 0 0 0 1	B_2		2	3	$PC_L \leftarrow B_2$ if (AC)≠1
JAC addr	0 1 0 1 1 0 0 1	B_2		2	3	$PC_L \leftarrow B_2$ if (AC)=1
JNC addr	0 1 0 1 0 0 1 0	B_2		2	3	$PC_L \leftarrow B_2$ if (C)≠1
JC addr	0 1 0 1 1 0 1 0	B_2		2	3	$PC_L \leftarrow B_2$ if (C)=1
JNF addr	0 1 0 1 0 0 1 1	B_2		2	3	$PC_L \leftarrow B_2$ if (F)≠1
JF addr	0 1 0 1 1 0 1 1	B_2		2	3	$PC_L \leftarrow B_2$ if (F)=1
JNMD addr	0 1 0 1 0 1 0 1	B_2		2	2	$PC_L \leftarrow B_2$ if (MUL)∨(DIV)≠1
JMD addr	0 1 0 1 1 1 0 1	B_2		2	2	$PC_L \leftarrow B_2$ if (MUL)∨(DIV)=1

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① Mnemonic
② Object code
③ Bytes
④ Cycles
⑤ Description

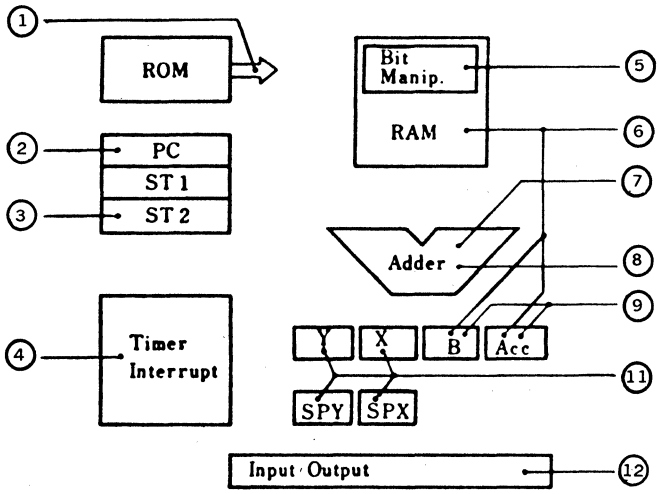
①	②			③	④	⑤
JTB$_a$ @Rd, addr	0 1 0 1 1 1 1 1	B_2	B_3	3	4	$PC_L \leftarrow B_3$ if $(Rd)_a=1$
JTB$_a$ Q_i, addr	0 1 0 1 1 1 1 1	B_2	B_3	3	4	$PC_L \leftarrow B_3$ if $(Q_i)_a=1$
JTB$_a$ PMR, addr	0 1 0 1 1 1 1 1	B_2	B_3	3	4	$PC_L \leftarrow B_3$ if $(PMR)_a=1$
JTB$_a$ D_j, addr	0 1 0 1 1 1 1 1	B_2	B_3	3	4	$PC_L \leftarrow B_3$ if $(D_j)_a=1$
JFB$_a$ @Rd, addr	0 1 0 1 1 1 1 1	B_2	B_3	3	4	$PC_L \leftarrow B_3$ if $(Rd)_a=0$
JFB$_a$ Q_i, addr	0 1 0 1 1 1 1 1	B_2	B_3	3	4	$PC_L \leftarrow B_3$ if $(Q_i)_a=0$
JFB$_a$ PMR, addr	0 1 0 1 1 1 1 1	B_2	B_3	3	4	$PC_L \leftarrow B_3$ if $(PMR)_a=0$
JFB$_a$ D_j, addr	0 1 0 1 1 1 1 1	B_2	B_3	3	4	$PC_L \leftarrow B_3$ if $(D_j)_a=0$
JNZR2 addr	0 1 0 1 0 1 0 0	B_2		2	3	$R2 \leftarrow (R2)-1$, if $(R2) \neq 0$ $PC_L \leftarrow B_2$
JZR2 addr	0 1 0 1 1 1 0 0	B_2		2	3	$R2 \leftarrow (R2)-1$, if $(R2)=0$ $PC_L \leftarrow B_2$
CALL addr	0 1 1 1 I_3 I_2 I_1 I_0	B_2		2	5	$PC_H \leftarrow I_3\ I_2\ I_1\ I_0$, $PC_L \leftarrow B_2$ $(SP-1) \leftarrow (PC_L)$, $(SP-2) \leftarrow (Q3_H)(PC_H)$, $SP \leftarrow (SP)-2$
FCAL n	0 0 0 0 1 I_2 I_1 I_0			1	4	$PC_H \leftarrow 0$, $PC_L \leftarrow 0\ 0\ 0\ 1\ I_2\ I_1\ I_0\ 0$ $(SP-1) \leftarrow (PC_L)$, $(SP-2) \leftarrow (Q3_H)(PC_H)$, $SP \leftarrow (SP)-2$
RTN	0 0 0 0 0 0 0 1 0			1	3	$PC_H \leftarrow (SP)_L$, $PC_L \leftarrow (SP+1)$, $SP \leftarrow (SP)+2$
NOP	0 0 0 0 0 0 0 0 0			1	2	No Operation

IS88

* INSTRUCTION SYSTEM

THIS DEVICE HAS A STANDARD INSTRUCTION SYSTEM COMPOSED OF 69 TYPES.

EACH INSTRUCTION IS ONE WORD INSTRUCTION.



Instruction types are:
1)Constant (LAI etc.3types)
2)ROM Addressing (BR etc.4types)
3)Stack (LMSIY etc. 3types)
4)Interrupt or Timer
(SEIE etc. 5types)
5)RAM Bit Manipulation
(SEM etc. 3types)
6)RAM to Register
(LAM etc. 6types)
7)Arithmetic (AMC etc. 15types)
8)Compare (MNEI etc. 7types)
9)Register to Register
(LAB etc.3types)
10)RAM Addressing (LXA etc. 12types)
11)Input/Output (SED etc. 8types)

* ROM ADDRESSING WAY
Page addressing way
(1 page = 64 words)

* RAM ADDRESSING WAY
X-register addresses RAM File.
(1 File = 16 digit)
Y-register addresses RAM Digit.

Group	Mnemonic Code	Operation
Register to Register	LAB	B → A
	LBA	A → B
	XAMR,m(m = 0 – 15)	A ↔ MR(m)
RAM Addressing	LXA	A → X
	LYA	A → Y
	LASPX	SPX → A
	LASPY	SPY → A
	LXI,i(i = 0 – 15)	i → X
	LYI,i(•)	i → Y
	IY	Y + 1 → Y, NZ ?
	DY	Y – 1 → Y, NB ?
	AYY	Y + A → Y, C ?
	SYY	Y – A → Y, NB ?
	XSP(XY)	SP(XY) ⟷ (XY)
	LAY	Y → A
Register to RAM	LAM (XY)	M → A (SP(XY) ⟷ (XY))
	LBM(XY)	M → B (•)
	XMA(XY)	M ↔ A (•)
	XMB(XY)	M ↔ B (•)
	LMAIY(X)	A → M, Y + 1 → Y, NZ ? (SPX ↔ X)
	LMADY(X)	A → M, Y – 1 → Y, NB ? (SPX ↔ X)
Immediate	LMIIY,i (i = 0 – 15)	i → M, Y + 1 → Y, NZ ?
	LAI,i (•)	i → A
	LBI,i (•)	i → B

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Group	Mnemonic Code	Operation
Arithmetic	AI,i(i = 0 – 15)	i + A → A, C ?
	IB	B + 1 → B, NZ ?
	DB	B – 1 → B, NB ?
	AMC	M + A + C → A, C ?
	SMC	M – A – C → A, NB ?
	AM	M + A → A, C ?
	DA(A,S)	Decimal adjust
	NEGA	$\bar{A}$ + 1 → A
	SEC	Set Carry
	REC	Reset Carry
	TC	Test Carry
	ROTL	Rotate Left A with Carry
	ROTR	Rotate Right A with Carry
	OR	AUB → A
	COMB	$\bar{B}$ → B
Compare	MNEI,i(i = 0 – 15)	if M ≠ i then Set Status
	YNEI,i(")	"Y ≠ i "
	ALEI,i(")	"A ≦ i "
	ALEM	"A ≦ M "
	BLEM	"B ≦ M "
	ANEM	"A ≠ M "
	BNEM	"B ≠ M "
RAM bit manipulation	SEM,n(n = 0 – 3)	Set RAM bit
	REM,n(")	Reset RAM bit
	TM,n (")	Test RAM bit (if M(n) = 1 then Set Status)

Group	Mnemonic Code	Operation
ROM Addresing	BR,l(l = 0 – 63)	Branch on Status One
	CAL,l(l = 0 – 63)	Call Subroutine on Status One
	LPU,u(u = 0 – 63)	Load Page on Status One
	RTN	Return from Subroutine
	(BRL)	LPU + BR(macro)
	(CALL)	LPU + CAL(")
Stack register	LMSIY,n(n = 0 – 3)	$\overline{ST2n}$ → M, Y + 1 → Y, NZ ?
	LSMDY,n(n = 0 – 2)	$\overline{M}$ → ST2n, Y – 1 → Y, NB ?
	LASC,n(n = 0 – 3)	$\overline{ST2n}$ + C → A
Interrupt	SE(f)(f = IF1,IF0,IE,T)	Set f
	RE(f)(f = IF1,IF0,IE,T)	Reset f
	T(f)(f = IF1,IF0,I1,I0)	Test f(if f=1 then Set Status)
	LTI,i(i = 0 – 15)	i → Timer
	RTNI	Return Interrupt (RTN and SEIE)
I/O	SED	Set D(Y)
	RED	Reset D(Y)
	TD	Test D(Y)(if D(Y)=1 then Set status)
	LAR,p(p = 0 – 5)	R(p) → A
	LRA,p(")	A → R(p)
	LRD,p(")	Decoder → R(p)
	LRB,p(")	B → R(p)
	LBR,p(")	R(p) → B

Instruction Set

TYPE 1: PROGRAM CONTROL INSTRUCTIONS

HSØ — Hold Until SYNC = Ø — 9 5 4 0 — 01110

Format: HSØ
Operation: Program execution stops until SYNC = Ø.
Timing: Waits as required. Responds in one cycle when SYNC = Ø.

HS1 — Hold until SYNC = 1 — 9 5 4 0 — 01111

Format: HS1
Operation: Program execution stops until SYNC = 1.
Timing: Waits as required. Responds in one cycle when SYNC = 1.
Example: To synchronize the program to the rising edge of SYNC, program HSØ followed by HS1.
Example: To synchronize the program to the falling edge of SYNC, program HS1 followed by HSØ.

VEC — Vectored Jump — 9 5 4 0 — 11111 00000

Format: VEC
Address Ø (if Z=Ø)
Address 1 (if Z=1)
• •
• •
• •
Address 15 (if Z=15)
Operation: The address of the location following the VECTOR OP Code is logically ORed with the contents of the Z accumulator. The contents of this vectored location are then placed into the program counter. Since the OR function is performed on Vector address plus one, then the VECTOR OP Code must be at an address that ends in a binary 1111.
Timing: Two clock cycles

JMP — Jump Conditionally — 9 4 3 0 — 111100 COND

JSR — Jump to Subroutine Conditionally — 9 4 3 0 — 111101 COND

Format: JMP COND, ADDRESS
JSR COND, ADDRESS
Operation: Both of the OP Codes provide a conditional jump to the desired address. In both cases the jump is executed if, and only if, the specified condition is met. In both cases the address immediately follows the OP Code in ROM memory. The JSR also loads PC+2 into the return register if the jump is executed.
There are 15 conditions that can be programmed. The conditions are listed as follows:

Programmable Conditions

Code	Mnemonic	Description
0000	UNC	Jump Unconditionally
0001	ZØ	Jump if Z Digit Bit Ø=1
0010	Z1	Jump if Z Digit Bit 1=1
0011	Z2	Jump if Z Digit Bit 2=1
0100	Z3	Jump if Z Digit Bit 3=1
0101	ZZ	Jump if Z Digit =Ø
0110	CB	Jump if Carry/Borrow (CB) Flag =1
0111	NE	Jump if Result not Zero (RNZ) Flag =1
1000	-	Jump Unconditionally
1001	FØ	Jump if Flag Digit Bit Ø=1
1010	F1	Jump if Flag Digit Bit 1=1
1011	F2	Jump if Flag Digit Bit 2=1
1100	F3	Jump if Flag Digit Bit 3=1
1101	FZ	Jump if Flag Digit =Ø
1110	L1	Jump if Latched Input #1 =1
1111	L2	Jump if Latched Input #1 =1

RTN — Return From Subroutine — 9 4 3 0 — 111111

Format: RTN
Operation: The contents of the return register are placed in PC.

Instruction Set

TYPE 2: PARALLEL DATA OPERATIONS

These OP Codes are further subdivided into two areas:
(A) Digit extraction per scan time, and (B) litteral operations. In some cases, the Z accumulator is implied in the OP Code. In others, the register is programmable from the following list:

Z = Z accumulator
Q = Static Outputs QØ-Q3
R = Static Outputs RØ-R3
S = Static Outputs SØ-S3
T = Static Outputs TØ-T3
F = Flag Register (4 Bit)
L = Latch Register (A, L2, L1)

(A) Digit Extractions

INØ — Input Select O (To Z) — 9 5 43 2 0 — 11100 DTM

Format: 7 INØ DTM
Operation: The input select output line (INS) is set to Ø. The 4 scanned input lines (INØ-IN3) are loaded into the Z accumulator during the specified digit time (Ø-7).
Timing: As required to SYNC. (28 MAX), plus one to execute.

IN1 — Input Select 1 (To Z) — 9 5 43 2 0 — 11101 DTM

Format: IN1 DTM
Operation: Same as INØ except that the INS OUTPUT line is set to 1.
Timing: Same as INØ.

FET — Fetch Digit — 9 6 5 4 3 2 0 — 1101 SRC DTM

Format: ... SRC DTM
Operation: Fetches any single digit from the 32 digit shift register bank as specified by the programmed digit time (Ø-7) and register (RA-RD). The specified digit is placed in the Z accumulator.
Timing: A required to SYNC. 36 max. clocks.

(B) Literal Operations

LDL — Load Literal — 9 7 6 3 2 0 — 010 DATA DST

Format: ORL DATA DST
Operation: The 4-bit literal data field is logically ORed with the destination register.
Timing: 1 Cycle.

MOVZ — Move Z Digit — 9 6 5 3 2 0 — 0110 DST

Format: MOVZ DST
Operation: The contents of the 4-bit Z accumulator are moved to the destination register. Z is not altered.
Timing: 1 Cycle.
Note: When the destination register is the latch register and the OP Code is LDL, ORL, or ANDL, then the literal data affects the latches as follows:

3	2	1	Ø
A	L2	L1	–

Ø Resets Latched Input #1, 1 does not alter.
Ø Resets Latched Input #2, 1 does not alter.
Ø Sets BCD Arithmetic, 1 sets *Binary*.

Instruction Set

TYPE 3: SHIFT AREA OPERATION

RNG — Range of Operation — 9 6 5 3 2 0 — 1100 END + 1 START - 1

Format: RNG START END
Operation: Defines the start and end digit counts for the rest of the OP codes in this section. Each of the four shift registers (RA-RD) contains 8 4-bit digits (Ø-7). This instruction specifies the range of digits the programmer wishes to restrict and operation to. The actual values stored in the OP Code are: start digit minus one and end digit plus one, thus bracketing the operation region. Wrap-around from digit 7 through digit Ø and on is permitted. The assembler takes the specified start and stop digit counts, adjusts them (MOD 8), and stores the results in the appropriate fields.
Timing: As required to SYNC to the start digit time. 32 max. clocks.
Example: To execute an operation over digits 2 to 5 inclusive program:
RNG 2, 5 (stored as 1100 000 111).
Example: To execute an operation over the full 8 digits program:
RNG 0, 7 (stored as 1100 000 111).
Example: To execute an operation over digits 5 to 4 with wrap-around through 7 to 0 program:
RNG 5, 4.
Example: To SYNC the program to a specific digit time program:
RNG X, X where "X" is the SYNC digit.

Each of the following instructions *must* be *immediately* preceeded by a RNG instruction. The source and destination fields must be one of the following registers.

Source or Destination

RA - Shift register A. (The display register)
RB - Shift register B.
RC - Shift register C.
RD - Shift register D.

Source Only

Z - Z accumulator (one digit).
I0 - Scan Inputs I0-I3 with INS = Ø.
I1 - Scan Inputs I0-I3 with INS = 1.
ZERO - All zeros (0000) lietral.

Note: Shift registers RA-RD are the same registers that are specified in the source field of the fetch OP Code (see type 2 OP Code). The binary code for a zero literal is not a zero.

ADD — Addition — 9 5 4 3 2 0 — 100001 DST SRC

Format: ADD SRC DST
Operation: A BCD or Binary addition over the range of digits specified in the RNG OP Codes is performed. The results are placed in the destination shift register. Digits not included via the RNG OP Code are not altered.
Timing: 4 + (4X # digits) cycles.

SUB — Subtract — 9 5 4 3 2 0 — 10010 DST SRC

Format: SUB SRC DST
Operation: A BCD or Binary subtraction over the range of digits specified in the RNG OP Code is performed. The results are placed in the destination shift register.
Timing: 4 + (4X # digits) cycles.

CMP — Compare Digits — 9 5 4 3 2 0 — 10011 DST SRC

Format: Same as SUB except that the result is not placed in the destination. The result (zero, borrow, etc.) can be tested via a conditional jump.
Timing: Same as SUB.

MOV — Move — 9 5 4 3 2 0 — 10111 DST SRC

Format: MOV SRC DST
Operation: The source digit(s) are moved to the corresponding destination digit(s) as specified by the RNG OP Code.
Timing: 4 + (4X # digits) cycles.

OR — Logical OR — 9 5 4 3 2 0 — 10000 DST SRC

Format: OR SRC DST
Operation: A logical OR is performed over the digits specified by the RNG OP Code, and the result is placed in the destination.
Timing: 4 + (4X # digits) cycles.

AND — Logical AND — 9 5 4 3 2 0 — 10100 DST SRC

Format: AND SRC DST
Operation: A logical AND is performed over the digits specified by the RNG OP Code, and the results are placed in the destination.
Timing: 4 + (4X # digits) cycles.

ROR — Rotate Right — 10110 DST SRC

Format: ROR DST
Operation: If BCD: A1 digit right shift is done over the digits specified by the RNG OP Code with the END digit getting a Ø.
If Binary: A1 bit right shift is done over the digits specified by the RNG OP Code with the MSB getting a Ø.
Timing: 4 + (4X # digits) cycles.

ROL — Rotate Left — 10101 DST SRC

Format: ROL DST
Operation: If BCD: A1 digit left shift is done over the digits specified by the RNG OP Code with the Start digit getting a Ø.
If Binary: A1 bit left shift is done over the digits specified by the RNG OP Code with the LSB getting a Ø.
Timing: 4 + (4X # digits) cycles.

Standard Instruction Set

Function	Mnemonic	Status Effects CARRY	Status Effects COMPARED	Description
Register to Register	TAY			Transfer accumulator to Y register.
	TYA			Transfer Y register to accumulator.
	CLA			Clear accumulator.
Transfer Register to Memory	TAM			Transfer accumulator to memory.
	TAMIY			Transfer accumulator to memory and increment Y register.
	TAMZA			Transfer accumulator to memory and zero accumulator.
Memory to Register	TMY			Transfer memory to Y register.
	TMA			Transfer memory to accumulator.
	XMA			Exchange memory and accumulator.
Arithmetic	AMAAC	√		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	√		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	√		Increment memory and load into accumulator. If carry, one to status.
	DMAN	√		Decrement memory and load into accumulator. If no borrow, one to status.
	IA			Increment accumulator, no status effect.
	IYC	√		Increment Y register. If carry, one to status.
	DAN	√		Decrement accumulator. If no borrow, one to status.
	DYN	√		Decrement Y register. If no borrow, one to status.
	A8AAC	√		Add 8 to accumulator, results to accumulator. If carry, one to status.
	A10AAC	√		Add 10 to accumulator, results to accumulator. If carry, one to status.
	A6AAC	√		Add 6 to accumulator, results to accumulator. If carry, one to status.
	CPAIZ	√		Complement accumulator and increment. If then zero, one to status.
Arithmetic Compare	ALEM	√		If accumulator less than or equal to memory, one to status.
	ALEC	√		If accumulator less than or equal to a constant, one to status.
Logical Compare	MNEZ		√	If memory not equal to zero, one to status.
	YNEA		√	If Y register not equal to accumulator, one to status and status latch.
	YNEC		√	If Y register not equal to a constant, one to status.
Bits in Memory	SBIT			Set memory bit.
	RBIT			Reset memory bit.
	TBIT1		√	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register.
	TCMIY			Transfer constant to memory and increment Y.
Input	KNEZ		√	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator.
Output	SETR			Set R output addressed by Y.
	RSTR			Reset R output addressed by Y.
	TDO			Transfer data from accumulator and status latch to O outputs.
	CLO			Clear O-output register.
RAM 'X' Addressing	LDX			Load 'X' with a constant.
	COMX			Complement 'X'.
ROM Addressing	BR			Branch on status = one.
	CALL			Call subroutine on status = one.
	RETN			Return from subroutine.
	LDP			Load page buffer with constant.

NOTE: If the bits COMPARED are not equal, or if there is a CARRY from the MSB of the adder, status will stay at one. Otherwise, status will go to a zero for one instruction cycle. Branch and Call can only execute successfully when status is a one. The check marks (√) indicate the instructions that affect the status.

IS91

standard instructions "0" = low = V_{DD}; "1" = high = V_{SS}

	MNEMONIC	DATA FLOW	STATUS – SKIP IF	DESCRIPTION
Arithmetic Operations	AD	M + A → A		Add M(B) to A, Store sum in A
	ADD	C + M + A → A		Add carry bit to M(B). Add sum to A, store sum in A.
		1 → C Overflow	Overflow	
	SUB	M + $\bar{A}$ + C → A		Subtract A from M
		Overflow → C	Overflow	Overflow to C
	COMP	$\bar{A}$ → A		One's complement of A to A
	LAX (Y)	Y → A		Y → A, Y = 0_t - 15
	ADX (Y)	A + Y → A	No overflow	Add constant (Y) to A. Store sum in A. Y = 1, 2. . .15.
	TAM		A = M(B)	Compare contents of A to M(B), skip if A = M(B)
	SC	1 → C		Set C register
	RSC	0 → C		Reset C register
	TC		C = 0	Skip if C = 0
Input/Output	DSPA*	A → S_a – S_g, C → S_p		A to output latches, 7-segment decoded to S_a – S_g. Segment decode is programmable. (7-segment or 4-bit binary). C to S_p latch.
	DSPB	B4 – B1 → D4 - D1		B4 – B1 to digit output latches D4 - D1
	DSPC*	B4 – B1 → D9 - D1	Always Skips	B4 – B1 decoded to digit output latches, (1 of 9), B_d = S → 13
	RGPO	Reset Output		GPO is latched to V_{SS}
	SGPO	Set Output		GPO is latched to V_{DD}
	READ	K4 - K1 → A		Read K inputs to A
Input Test	TIN1		IN1 = 1	Test IN1
	TIN2		IN2 = 0	Test IN2
	TKB		K = 0	Skip if any K input active
	TIN3		IN3 = 0	Test IN3 (SEG g)
Control Functions	GO	I_6 – I_1 → P		Load next ROM instruction address.
	CALL	If ($\overline{LG}$) SET – SR		Call subroutine. If previous
		I_6 – I_1 → P,		instruction was not LG, set SR.
		SA_W → SB_W, P+1 → SA		
	RET	SA_W → P_W		Pop up ROM address save registers
		If ($\overline{SR}$) SA_P → P_P		0 SR
		SA_W ↔ SB_W		
	LG/GO	I_4 – I_1 → P_P		Two micro-cycle operation. Long GO
		I_6 – I_1 (Second Word) → P_W		TO, Load P_P and P_W.
	LG/CALL	SA → SB, P + 1 → SA		Two micro-cycle operation. Long
		I_6 – I_1 (Second Word) → P_W		call. Load P_P and P_W. Push down address save registers.
	NOP			No operation.
Memory Digit Operations	EXC (r)	A ↔ M(B)		Exchange data word at M(B) with A
		B_r ⊕ r → B_r		EXCLUSIVE-OR B_r with r, r = 0, 1, 2, 3
	EXC -(r)	A ↔ M(B)		Exchange and decrement B
		B_r ⊕ r → B_r, B_d - 1 → B_d	B_d → 3, 2, 1, 0	EXCLUSIVE OR B_r with r, r = 0, 1, 2, 3
	EXC +(r)	A ↔ M(B)		Exchange and increment B_d
		B_r ⊕ r → B_r, B_d + 1 → B_d	B_d → 13	EXCLUSIVE-OR B_r with r, r = 0, 1, 2, 3
	MTA (r)	M(B) → A		Load accumulator with data word M(B)
		B_r ⊕ r → B_r		EXCLUSIVE-OR B_r with r, r = 0, 1, 2, 3
Memory Bit Operations	TM (Z)		M (B, Z) = 0	Test bit Z of M(B), skip if zero Z = 1, 2, 4, 8
Memory Address Operations	LB (r,d)	r → B_r, d → B_d		r = 0, 1, 2, 3 d = 5, 6, 7, or 12, 13, 14, 15
	ATB	A → B_d		Transfer contents of accumulator to B_d register
	BTA	B_d → A		Transfer contents of B_d register to accumulator
	SB7	Set B7		Sets B7. 5th register is addressed independent of B5 and B6
	RB7	Reset B7		B5 and B6 are unchanged

*DSPA can be programmed to turn on DSPC.

standard instructions

	MNEMONIC	DATA FLOW	SKIP IF	DESCRIPTION
Arithmetic Operations	AD	M + A → A		Add M (B) to A, store sum in A
	ADD	C + M + A → A		Add carry bit to M (B). Add sum to A, store sum in A
		1 → C if A ≥ 10 0 → C if A < 10	A < 10	Set C if A ≥ 10, reset C if A < 10
	SUB	M + $\overline{A}$ + C → A		Subtract A from M
		Overflow → C	Overflow	Overflow to C
	COMP	$\overline{A}$ → A		One's complement of A to A
	OTA	0 → A		Clear Accumulator
	ADX (Y)	A + Y → A	No overflow and Y ≠ 6	Add constant (Y) to A. Store sum in A. Y = 1, 2 . . . 15
	HXA	H ↔ A		Exchange contents of H register with A
	TAM		A = M (B)	Compare contents of A to M (B), skip if A = M (B)
	SC	1 → C		Set C register
	RSC	0 → C		Reset C register
	TC		C = 0	Skip if C = 0
Input Test	TIN		INB = 1	Test INB. Active state of input is programmable
	TF (N)		F (N) = 0	Test F (N) pin. N = 1, 2, 3
	TKB		K = 1	Skip if any K input active. Active state of input is programmable
	TIR		DO3 = 0	Test DO3 pin as input
Input/Output	BTD	$\overline{B_d}$ → DO4 – DO1		Transfer contents of B_d to digit output latches, turns BLK output low for one cycle time
	DSPA	A → S_a – S_d H → S_e – S_g $\overline{C}$ → S_p		A4 – A1 to output latches, directly to outputs S_a – S_d. H3 – H1 to output latches, direct to S_e – S_g. $\overline{C}$ to S_p latch
	DSPS	A → S_a – S_g $\overline{C}$ → S_p		A to putput latches, 7-segment decoded to S_a – S_g. Segment decode is programmable. $\overline{C}$ to S_p latch
	AXO	SI → A A → SO		Exchange accumulator with serial input/output
	LDF	If $\overline{I6^*}$: $\overline{I5^*}$ → F3 If $\overline{I4^*}$: $\overline{I3^*}$ → F2 If $\overline{I2^*}$: $\overline{I1^*}$ → F1		N = 1, 2, 3. Load F (N) from next instruction word. 2 microcycle instruction
	READ	K4 – K1 → A		Read K inputs to A. Active state of input is programmable

*Second microcycle word

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	MNEMONIC	DATA FLOW	SKIP IF	DESCRIPTION
Input/Output	BTD	B_d → DO4 – DO1		Transfer contents of B_d to digit output latches
	DSPA	A → S_a – S_d 0 → S_e – S_g C → S_p		A4–A1 to output latches, directly to outputs S_a–S_d 0 to outputs S_e–S_g C to S_p latch
	DSPS	A → S_a – S_g C → S_p		A to output latches, 7-segment decoded to S_a–S_g C to S_p latch
	AXO	SI → A A → SO		Exchange accumulator with serial input/output
	LDF	I → F (N)		N = 1, 2, 3, 4. Load F (N) from next instruction word 2 microcycle instruction
Input Test	TIN		INB = 1	Test INB. Active state of input is programmable
	TK (N)	if F4 = 0	K (N) = 1	N = 1, 2, 3, 4. Active state of input is programmable
		if F4 = 1	F (N) = 1	N = 1, 2, 3
	TKB		K (N) = 1	N = 1, 2, 3, 4. Skip if any K input active
	TIR		ΔIRB	Test IRB. Skip if IRB has changed since last test of IRB

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IS92 Cont'd

	MNEMONIC	DATA FLOW	SKIP IF	DESCRIPTION
Control Functions	GO TO (GO)	$I_6 - I_1 \rightarrow P_W$ If $P_P = 1111$ X : $11110 \rightarrow P_P$		Load next ROM instruction address If on page 36_8 or 37_8 reset page address to 36_8 (Note 1)
	CALL	$I_6 - I_1 \rightarrow P_W$, $IIII \rightarrow P_P$ If $P_P \neq$ IIIIX : SA → SB, P + 1 → SA		Call subroutine. If not on page 36_8 or 37_8, push down address save registers. Set page address to 37_8
	RET	SA → P SB → SA, SB → SB		Pop up ROM address save registers
	RETS	SA → P SB → SA, SB → SB	SKIP	RET, then skip next instruction upon return
	LG/GO	Load P $\overline{I_4} - \overline{I_1}, I_8^* \rightarrow P_P$ $I_6^* - I_1^* \rightarrow P_W$		2 microcycle operation. Long GO TO, Load P_P and P_W (Note 1)
	LG/CALL	SA → SB, P + 1 → SA Load P		2 microcycle operation. Long call. Load P_P and P_W. Push down address save register (Note 1)
	NOP			No operation
Memory Digit Operations	EXC (r)	A ↔ M (B) $B_r \oplus r \rightarrow B_r$		Exchange data word at M (B) with A. EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	EXC –(r)	A ↔ M (B) $B_r \oplus r \rightarrow B_r$, $B_d - 1 \rightarrow B_d$	$B_d \rightarrow 15$	Exchange and decrement B_d EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	EXC +(r)	A ↔ M (B) $B_r \oplus r \rightarrow B_r$, $B_d + 1 \rightarrow B_d$	$B_d \rightarrow 0$ or $B_d \rightarrow 13$	Exchange and increment B_d EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	MTA (r)	M (B) → A $B_r \oplus r \rightarrow B_r$		Load accumulator with data word M (B) EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	LM (Y)	Y → M (B) $B_d + 1 \rightarrow B_d$		Load memory with Y. Y = 0, 1, 2, . . .15 Increment B_d
Memory Bit Operations	SM (Z)	1 → M (B, Z)		Set Bit Z of M (B), Z = 1, 2, 4, 8
	RSM (Z)	0 → M (B, Z)		Reset Bit Z of M (B)
	TM (Z)		M (B, Z) = 0	Test Bit Z of M (B), skip if 0
Memory Address Operations	LB (r, d)	r → B_r, d → B_d		r = 0, 1, 2, 3. d = 0 , 11, 12, 13, 14, 15. Load B register. Successive LB's are ignored (Note 2)
	LBL	$I_7^* - I_5^* \rightarrow B_r$, $I_4^* - I_1^* \rightarrow B_d$		2 microcycle instruction. Load next ROM word into B register
	ATB	A → B_d		Transfer contents of accumulator to B_d register
	BTA	B_d → A		Transfer contents of B_d register to accumulator
	HXBR	H ↔ B_r		Exchange contents of H and B_r registers

Note 1: ROM pages 10_8 through 17_8 cannot be used.

*Second microcycle word

Note 2: d = 4, 11, 12, 13, 14, 15 when RAM is configured 8 x 12 x 4.

INSTRUCTION DESCRIPTION TERMS

TERM	DEFINITION
B	Byte indicator (1 = byte, 0 = word)
C	Bit count
DR	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
M.A.	Memory Address
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
SR	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
WR or R	Workspace register
WRn or Rn	Workspace register n
(n)	Contents of n
a → b	a is transferred to b
(a) → b	Contents of a is transferred to be
[n]	Absolute value of n
+	Arithmetic addition
–	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
⊕	Logical exclusive OR
n	Logical complement of n
>	Hexadecimal value

INSTRUCTION SET, ALPHABETICAL INDEX

ASSEMBLY LANGUAGE MNEMONIC	MACHINE LANGUAGE OP CODE	FORMAT	STATUS REG. BITS AFFECTED	RESULT COMPARED TO ZERO	INSTRUCTION	PARAGRAPH
A	A000	1	0-4	X	Add (word)	4.6.1
AB	B000	1	0-5	X	Add (byte)	4.6.1
ABS	0740	6	0-2	X	Absolute Value	4.6.6
AI	0220	8	0-4	X	Add Immediate	4.6.8
ANDI	0240	8	0-2	X	AND Immediate	4.6.8
B	0440	6	–		Branch	4.6.6
BL	0680	6	–		Branch and Link (R11)	4.6.6
BLWP	0400	6	–		Branch; New Workspace Pointer	4.6.6
C	8000	1	0-2		Compare (word)	4.6.1
CB	9000	1	0-2,5		Compare (byte)	4.6.1
CI	0280	8	0-2		Compare Immediate	4.6.8
CKOF	03C0	7	–		User Defined	4.6.7
CKON	03A0	7	–		User Defined	4.6.7
CLR	04C0	6	–		Clear Operand	4.6.6
COC	2000	3	2		Compare Ones Corresponding	4.6.3
CZC	2400	3	2		Compare Zeroes Corresponding	4.6.3
DEC	0600	6	0-4	X	Decrement (by one)	4.6.6
DECT	0640	6	0-4	X	Decrement (by two)	4.6.6
DIV	3C00	9	4		Divide	4.6.3
IDLE	0340	7	–		Computer Idle	4.6.7
INC	0580	6	0-4	X	Increment (by one)	4.6.6
INCT	05C0	6	0-4	X	Increment (by two)	4.6.6
INV	0540	6	0-2	X	Invert (One's Complement)	4.6.6
JEQ	1300	2	-		Jump Equal (ST2 1)	4.6.2
JGT	1500	2	–		Jump Greater Than (ST1 1), Arithmetic	4.6.2
JH	1B00	2	–		Jump High (ST0 1 and ST2=0), Logical	4.6.2
JHE	1400	2	–		Jump High or Equal (ST0 or ST2=1), Logical	4.6.2
JL	1A00	2	–		Jump Low (ST0 and ST2=0), Logical	4.6.2
JLE	1200	2	–		Jump Low or Equal (ST0=0 or ST2=1), Logical	4.6.2
JLT	1100	2	–		Jump Less Than (ST1 and ST2=0), Arithmetic	4.6.2
JMP	1000	2	–		Jump Unconditional	4.6.2
JNC	1700	2	–		Jump No Carry (ST3=0)	4.6.2
JNE	1600	2	–		Jump Not Equal (ST2=0)	4.6.2
JNO	1900	2	–		Jump No Overflow (ST4-0)	4.6.2
JOC	1800	2	–		Jump On Carry (ST3-1)	4.6.2

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INSTRUCTION SET, ALPHABETICAL INDEX (Concluded)

ASSEMBLY LANGUAGE MNEMONIC	MACHINE LANGUAGE OP CODE	FORMAT	STATUS REG. BITS AFFECTED	RESULT COMPARED TO ZERO	INSTRUCTION	PARAGRAPH
JOP	1C00	2	–		Jump Odd Parity (ST5=1)	4.6.2
LDCR	3000	4	0-2,5	X	Load CRU	4.6.4
LI	0200	8	–	X	Load Immediate	4.6.8
LIMI	0300	8	12-15		Load Interrupt Mask Immediate	4.6.8
LREX	03E0	7	12-15		Load and Execute	4.6.7
LWPI	02E0	8	–		Load Immediate to Workspace Pointer	4.6.8
MOV	C000	1	0-2	X	Move (word)	4.6.1
MOVB	D000	1	0-2,5	X	Move (byte)	4.6.1
MPY	3800	9	–		Multiply	4.6.3
NEG	0500	6	0-2	X	Negate (Two's Complement)	4.6.6
ORI	0260	8	0-2	X	OR Immediate	4.6.8
RSET	0360	7	12-15		Reset AU	4.6.7
RTWP	0380	7	0-15		Return from Context Switch	4.6.7
S	6000	1	0-4	X	Subtract (word)	4.6.1
SB	7000	1	0-5	X	Subtract (byte)	4.6.1
SBO	1D00	2	–		Set CRU Bit to One	4.6.2
SBZ	1E00	2	–		Set CRU Bit to Zero	4.6.2
SETO	0700	6	–		Set Ones	4.6.6
SLA	0A00	5	0-4	X	Shift Left Arithmetic	4.6.5
SOC	E000	1	0-2	X	Set Ones Corresponding (word)	4.6.1
SOCB	F000	1	0-2,5	X	Set Ones Corresponding (byte)	4.6.1
SRA	0800	5	0-3	X	Shift Right (sign extended)	4.6.5
SRC	0B00	5	0-3	X	Shift Right Circular	4.6.5
SRL	0900	5	0-3	X	Shift Right Logical	4.6.5
STCR	3400	4	0-2,5	X	Store From CRU	4.6.4
STST	02C0	8	–		Store Status Register	4.6.8
STWP	02A0	8	–		Store Workspace Pointer	4.6.8
SWPB	06C0	6	–		Swap Bytes	4.6.6
SZC	4000	1	0-2	X	Set Zeroes Corresponding (word)	4.6.1
SZCB	5000	1	0-2,5	X	Set Zeroes Corresponding (byte)	4.6.1
TB	1F00	2	2		Test CRU Bit	4.6.2
X	0480	6	–		Execute	4.6.6
XOP	2C00	9	6		Extended Operation	4.6.9
XOR	2800	3	0-2	X	Exclusive OR	4.6.3

Cont'd on next page

IS95 Cont'd

INSTRUCTION SET, NUMERICAL INDEX

MACHINE LANGUAGE OP CODE (HEXADECIMAL)	ASSEMBLY LANGUAGE MNEMONIC	INSTRUCTION	FORMAT	STATUS BITS AFFECTED
0200	LI	Load Immediate	8	0-2
0220	AI	Add Immediate	8	0-4
0240	ANDI	And Immediate	8	0-2
0260	ORI	Or Immediate	8	0-2
0280	CI	Compare Immediate	8	0-2
02A0	STWP	Store WP	8	–
02C0	STST	Store ST	8	–
02E0	LWPI	Load WP Immediate	8	–
0300	LIMI	Load Int. Mask	8	12-15
0340	IDLE	Idle	7	–
0360	RSET	Reset AU	7	12-15
0380	RTWP	Return from Context Sw.	7	0-15
03A0	CKON	User Defined	7	–
03C0	CKOF	User Defined	7	–
03E0	LREX	Load & Execute	7	–
0400	BLWP	Branch; New WP	6	–
0440	B	Branch	6	–
0480	X	Execute	6	–
04C0	CLR	Clear to Zeroes	6	–
0500	NEG	Negate to Ones	6	0-2
0540	INV	Invert	6	0-2
0580	INC	Increment by 1	6	0-4
05C0	INCT	Increment by 2	6	0-4
0600	DEC	Decrement by 1	6	0-4
0640	DECT	Decrement by 2	6	0-4
0680	BL	Branch and Link	6	–
06C0	SWPB	Swap Bytes	6	–
0700	SETO	Set to Ones	6	–
0740	ABS	Absolute Value	6	0-2
0800	SRA	Shift Right Arithmetic	5	0-3
0900	SRL	Shift Right Logical	5	0-3
0A00	SLA	Shift Left Arithmetic	5	0-4
0B00	SRC	Shift Right Circular	5	0-3
1000	JMP	Unconditional Jump	2	–
1100	JLT	Jump on Less Than	2	–
1200	JLE	Jump on Less Than or Equal	2	–
1300	JEQ	Jump on Equal	2	–
1400	JHE	Jump on High or Equal	2	–
1500	JGT	Jump on Greater Than	2	–
1600	JNE	Jump on Not Equal	2	–
1700	JNC	Jump on No Carry	2	–
1800	JOC	Jump on Carry	2	–
1900	JNO	Jump on No Overflow	2	–
1A00	JL	Jump on Low	2	–
1B00	JH	Jump on High	2	–
1C00	JOP	Jump on Odd Parity	2	–
1D00	SBO	Set CRU Bits to Ones	2	–
1E00	SBZ	Set CRU Bits to Zeroes	2	–
1F00	TB	Test CRU Bit	2	2
2000	COC	Compare Ones Corresponding	3	2
2400	CZC	Compare Zeroes Corresponding	3	2
2800	XOR	Exclusive Or	3	0-2
2C00	XOP	Extended Operation	9	6
3000	LDCR	Load CRU	4	0-2,5
3400	STCR	Store CRU	4	0-2,5
3800	MPY	Multiply	9	–
3C00	DIV	Divide	9	4
4000	SZC	Set Zeroes Corresponding (Word)	1	0-2
5000	SZCB	Set Zeroes Corresponding (Byte)	1	0-2,5
6000	S	Subtract Word	1	0-4
7000	SB	Subtract Byte	1	0-5
8000	C	Compare Word	1	0-2
9000	CB	Compare Byte	1	0-2,5
A000	A	Add Word	1	0-4
B000	AB	Add Byte	1	0-5
C000	MOV	Move Word	1	0-2
D000	MOVB	Move Byte	1	0-2,5
E000	SOC	Set Ones Corresponding (Word)	1	0-2
F000	SOCB	Set Ones Corresponding (Byte)	1	0-2,5

IS95 Cont'd

IS97

	Mnemonic		Description	Bytes	Cycle
Accumulator	ADD	A,R	Add register to A	1	1
	ADD	A,@R	Add data memory to A	1	1
	ADD	A,#data	Add immediate to A	2	2
	ADDC	A,R	Add with carry	1	1
	ADDC	A,@R	Add with carry	1	1
	ADDC	A,#data	Add with carry	2	2
	ANL	A,R	And register to A	1	1
	ANL	A,@R	And data memory to A	1	1
	ANL	A,#data	And immediate to A	2	2
	ORL	A,R	Or register to A	1	1
	ORL	A,@R	Or data memory to A	1	1
	ORL	A,#data	Or immediate to A	2	2
	XRL	A,R	Exclusive Or register to A	1	1
	XRL	A,@R	Exclusive or data memory to A	1	1
	XRL	A,#data	Exclusive or immediate to A	2	2
	INC	A	Increment A	1	1
	DEC	A	Decrement A	1	1
	CLR	A	Clear A	1	1
	CPL	A	Complement A	1	1
	DA	A	Decimal Adjust A	1	1
	SWAP	A	Swap nibbles of A	1	1
	RL	A	Rotate A left	1	1
	RLC	A	Rotate A left through carry	1	1
	RR	A	Rotate A right	1	1
	RRC	A	Rotate A right through carry	1	1
Input/Output	IN	A,P	Input port to A	1	2
	OUTL	P,A	Output A to port	1	2
	MOVD	A,P	Input Expander port to A	1	2
	MOVD	P,A	Output A to Expander port	1	2
	ANLD	P,A	And A to Expander port	1	2
	ORLD	P,A	Or A to Expander port	1	2
Registers	INC	R	Increment register	1	1
	INC	@R	Increment data memory	1	1
Branch	JMP	addr	Jump unconditional	2	2
	JMPP	@A	Jump indirect	1	2
	DJNZ	R,addr	Decrement register and Jump on R not zero	2	2
	JC	addr	Jump on Carry = 1	2	2
	JNC	addr	Jump on Carry = 0	2	2
	JZ	addr	Jump on A Zero	2	2
	JNZ	addr	Jump on A not Zero	2	2
	JT1	addr	Jump on T1 = 1	2	2
	JNT1	addr	Jump on T1 = 0	2	2
	JTF	addr	Jump on timer flag	2	2
Subroutine	CALL		Jump to subroutine	2	2
	RET		Return	1	2
Flags	CLR	C	Clear Carry	1	1
	CPL	C	Complement Carry	1	1
Data Moves	MOV	A,R	Move register to A	1	1
	MOV	A,@R	Move data memory to A	1	1
	MOV	A,#data	Move immediate to A	2	2
	MOV	R,A	Move A to register	1	1
	MOV	@R,A	Move A to data memory	1	1
	MOV	R,#data	Move immediate to register	2	2
	MOV	@R,#data	Move immediate to data memory	2	2
	XCH	A,R	Exchange A and register	1	1
	XCH	A,@R	Exchange A and data memory	1	2
	XCHD	A,@R	Exchange nibble of A and register	1	1
	MOVP	A,@A	Move to A from current page	1	2
Timer/Counter	MOV	A,T	Read Timer/Counter	1	1
	MOV	T,A	Load Timer/Counter	1	1
	STRT	T	Start Timer	1	1
	STRT	CNT	Start Counter	1	1
	STOP	TCNT	Stop Timer/Counter	1	1
	NOP		No Operation	1	1

Instruction Summary

Mnemonic	Meaning	Operation	Maximum Execution Time (Note)	Instruction Format
1. Branch Instructions				
BOC	Branch On Condition (Table 4)	(PC) ← (PC) + disp if cc true	5M + E_R + 1M if branch	0 1 0 0 cc | disp
JMP	Jump	(PC) ← EA	4M + E_R	0 0 0 1 1 0 xr
JMP@	Jump Indirect	(PC) ← (EA)	4M + 2E_R	1 0 0 1 1 0
JSR	Jump To Subroutine	(STK) ← (PC), (PC) ← EA	5M + E_R	0 0 0 1 0 1
JSR@	Jump To Subroutine Indirect	(STK) ← (PC), (PC) ← (EA)	5M + 2E_R	1 0 0 1 0 1
RTS	Return from Subroutine	(PC) ← (STK) + disp	5M + E_R	1 0 0 0 0 0 0 0
RTI	Return from Interrupt	(PC) ← (STK) + disp, IEN = 1	6M + E_R	0 1 1 1 1 1 0 0
2. Skip Instructions				
SKNE	Skip if Not Equal	If (ACr) ≠ (EA), (PC) ← (PC) + 1	5M + 2E_R + 1M if skip	1 1 1 1 r | xr | disp
SKG	Skip if Greater	If (AC0) > (EA), (PC) ← (PC) + 1	7M + 2E_R + 1M if skip	1 0 0 1 1 1
SKAZ	Skip if And is Zero	If [(AC0) ∧ (EA)] = 0, (PC) ← (PC) + 1	5M + 2E_R + 1M if skip	1 0 1 1 1 0
ISZ	Increment and Skip if Zero	(EA) ← (EA) + 1, if (EA) = 0, (PC) ← (PC) + 1	7M + 2E_R + E_W + 1M if skip	1 0 0 0 1 1
DSZ	Decrement and Skip if Zero	(EA) ← (EA) − 1, if (EA) = 0, (PC) ← (PC) + 1	7M + 2E_R + E_W + 1M if skip	1 0 1 0 1 1
AISZ	Add Immediate, Skip if Zero	(ACr) ← (ACr) + disp, if (ACr) = 0, (PC) ← (PC) + 1	5M + E_R + 1M if skip	0 1 1 1 1 0 r
3. Memory Data Transfer Instructions				
LD	Load	(ACr) ← (EA)	4M + 2E_R	1 1 0 0 r | xr | disp
LD@	Load Indirect	(AC0) ← ((EA))	5M + 3E_R	1 0 1 0 0 0
ST	Store	(EA) ← (ACr)	4M + E_R + E_W	1 1 0 1 r
ST@	Store Indirect	((EA)) ← (AC0)	4M + 2E_R + E_W	1 0 1 1 0 0
LSEX	Load With Sign Extended	(AC0) ← (EA) bit 7 extended	4M + 2E_R	1 0 1 1 1 1
4. Memory Data Operate Instructions				
AND	And	(AC0) ← (AC0) ∧ (EA)	4M + 2E_R	1 0 1 0 1 0 | xr | disp
OR	Or	(AC0) ← (AC0) ∨ (EA)	4M + 2E_R	1 0 1 0 0 1
ADD	Add	(ACr) ← (ACr) + (EA), OV, CY	4M + 2E_R	1 1 1 0 r
SUBB	Subtract with Borrow	(AC0) ← (AC0) + ~ (EA) + (CY), OV, CY	4M + 2E_R	1 0 0 1 0 0
DECA	Decimal Add	(AC0) ← (AC0) $+_{10}$ (EA) $+_{10}$ (CY), OV, CY	7M + 2E_R	1 0 0 0 1 0
5. Register Data Transfer Instructions				
LI	Load Immediate	(ACr) ← disp	4M + E_R	0 1 0 1 0 0 r | disp
RCPY	Register Copy	(ACdr) ← (ACsr)	4M + E_R	0 1 0 1 1 1 dr sr | 000 000
RXCH	Register Exchange	(ACdr) ← (ACsr), (ACsr) ← (ACdr)	6M + E_R	0 1 1 0 1 1 dr sr
XCHRS	Exchange Register and Stack	(STK) ← (ACr), (ACr) ← (STK)	6M + E_R	0 0 0 1 1 1 r | 0 0
CFR	Copy Flags Into Register	(ACr) ← (FR)	4M + E_R	0 0 0 0 0 1
CRF	Copy Register Into Flags	(FR) ← (ACr)	4M + E_R	0 0 0 0 1 0
PUSH	Push Register Onto Stack	(STK) ← (ACr)	4M + E_R	0 1 1 0 0 0
PULL	Pull Stack Into Register	(ACr) ← (STK)	4M + E_R	0 1 1 0 0 1
PUSHF	Push Flags Onto Stack	(STK) ← (FR)	4M + E_R	0 0 0 0 1 1 0 0
PULLF	Pull Stack Into Flags	(FR) ← (STK)	4M + E_R	0 0 0 1 0 0 0 0
6. Register Data Operate Instructions				
RADD	Register Add	(ACdr) ← (ACdr) + (ACsr), OV, CY	4M + E_R	0 1 1 0 1 0 dr sr | 000 000
RADC	Register Add With Carry	(ACdr) ← (ACdr) + (ACsr) + (CY), OV, CY	4M + E_R	0 1 1 1 0 1
RAND	Register And	(ACdr) ← (ACdr) ∧ (ACsr)	4M + E_R	0 1 0 1 0 1
RXOR	Register Exclusive OR	(ACdr) ← (ACdr) ▽ (ACsr)	4M + E_R	0 1 0 1 1 0
CAI	Complement and Add Immediate	(ACr) ← ~ (ACr) + disp	5M + E_R	0 1 1 1 0 0 r | disp
7. Shift And Rotate Instructions				
SHL	Shift Left	(ACr) ← (ACr) shifted left n places, w/wo link	(5 + 3n) M + E_R, n = 1 – 127; 6M + E_R, n = 0	0 0 1 0 1 0 r | n | ℓ
SHR	Shift Right	(ACr) ← (ACr) shifted right n places, w/wo link		0 0 1 0 1 1
ROL	Rotate Left	(ACr) ← (ACr) rotated left n places, w/wo link		0 0 1 0 0 0
ROR	Rotate Right	(ACr) ← (ACr) rotated right n places, w/wo link		0 0 1 0 0 1
8. Miscellaneous Instructions				
HALT	Halt	Halt		0 0 0 0 0 0 0 0 0 | 0000000
SFLG	Set Flag (Table 5)	(FR)$_{fc}$ ← 1	5M + E_R	0 0 1 1 fc 1
PFLG	Pulse Flag (Table 5)	(FR)$_{fc}$ ← 1, (FR)$_{fc}$ ← 0	6M + E_R	0 0 1 1 fc 0
NOP	No Operation	(PC) ← (PC) + 1	4M + E_R	0 1 0 1 1 1 0 0 0

Note: M = Machine cycle time = 4 clock periods
n = number of shifts
E_R = Extend time for read cycle
E_W = Extend time for write cycle
External interrupt response time is 7M + E_R plus time to finish current instruction.

Table 4. Branch Conditions

Number	Mnemonic	Condition
0	STFL	Stack full
1	REQ0	(AC0) equal to zero(1)
2	PSIGN	(AC0) has positive sign(2)
3	BIT 0	Bit 0 of AC0 true
4	BIT 1	Bit 1 of AC0 true
5	NREQ0	(AC0) is non-zero(1)
6	BIT 2	Bit 2 AC0 is true
7	CONTIN	CONTIN (continue) input is true
8	LINK	LINK is true
9	IEN	IEN is true
10	CARRY	CARRY is true
11	NSIGN	(AC0) has negative sign(2)
12	OVF	OVF is true
13	JC13	JC13 input is true
14	JC14	JC14 input is true
15	JC15	JC15 input is true

Note 1: If the selected data length is 8 bits, only bits 0-7 of AC0 are tested.
Note 2: Bit 7 is the sign bit (instead of bit 15) if the selected data length is 8 bits.

Table 5. Status and Control Flags

Register Bit	Flag Name	Function
0	"1"	Not used–always logic 1
1	IE1	Interrupt Enable Level 1
2	IE2	Interrupt Enable Level 2
3	IE3	Interrupt Enable Level 3
4	IE4	Interrupt Enable Level 4
5	IE5	Interrupt Enable Level 5
6	OVF	Overflow
7	CRY	Carry
8	LINK	Link
9	IEN	Master Interrupt Enable
10	BYTE	8 bit data length
11	F11	Flag 11
12	F12	Flag 12
13	F13	Flag 13
14	F14	Flag 14
15	"1"	Always logic 1, set for Interrupt 0 exit

INSTRUCTION SET

RAM Addressing Instructions

XAB	Exchange A with BL
LBA	Load BL from A
LB	Load BU=0, BL=Immediate
EOB	Exclusive OR BU
LBL	Load B Long
INCB	Increment B
DECB	Decrement B

Bit Manipulation Instructions

SB	Set Bit
RB	Reset Bit
SKBF	Skip on Bit False

Register to Register Instructions

XAS	Exchange A and S
LSA	Load S from A

Register Memory Instructions

L	Load A from Memory
X	Exchange A and Memory
XDSK	Exchange A with Memory. Decrement BL and Skip if BL Counts to 15
XNSK	Exchange A with Memory. Increment BL and Skip if BL Counts to 0

Arithmetic Instructions

A	Add Memory to A
AC	Add Memory with Carry to A
ACSK	Add Memory with Carry to A and Skip on No Carry-out
ASK	Add Memory to A and Skip on no Carry-out
DC	Decimal Correction
COM	Complement A
RC	Reset Carry
SC	Set Carry
SKNC	Skip on No Carry
LAI	Load A with Immediate Field
AISK	Add Immediate and Skip on No Carry-out

Logical Comparison Instructions

SKMEA	Skip if Memory Equals A
SKBEI	Skip if BL Equals Immediate Field
SKAEI	Skip if A Equals Immediate Field

Input/Output Instructions IS100

SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IBM	Input Channel B ANDed with A
OB	Output from A to Channel B
IAM	Input Channel A ANDed with A
OA	Output from A to Channel A
I1	Input Channel 1
INT1H	Skip if INT1 Input (RI08) is Low
DIN1	Skip if INT1 Flip-flop is Reset
INT0L	Skip if INT0 Input is High
DIN0	Skip if INT0 Flip-flop is Reset
SEG1	Decoder Matrix to Channel A
SEG2	Decoder Matrix to Channel B

Conditional Transfer Instructions

TC	Transfer on Carry Set
TNC	Transfer on No Carry Set
TLC	Transfer Long on Carry Set
TLNC	Transfer Long on No Carry Set
TBF	Transfer on Bit in Memory False
TBT	Transfer on Bit in Memory True
TLBF	Transfer Long on Bit in Memory False
TLBT	Transfer Long on Bit in Memory True
TE	Transfer on A = Memory
TNE	Transfer on A ≠ Memory
TLE	Transfer Long on A = Memory
TLNE	Transfer Long on A ≠ Memory
TIH	Transfer if Input High
TIL	Transfer if Input Low
TLIH	Transfer Long if Input High
TLIL	Transfer Long if Input Low

ROM Addressing Instructions

RT	Return from Subroutine
RTSK	Return and Skip
T	Transfer on Page
NOP	No Operation
TL	Transfer Long
TM	Transfer and Mark
TML	Transfer and Mark Long

Input/Output Instructions IS100a

SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IBM	Input Channel B ANDed with A
*IBM	Same Plus Presets Upper Counter
OB	Output from A to Buffer B
IAM	Input Channel A ANDed with A
*IAM	Same Plus Clears Appropriate Counters
OA	Output from A to Buffer A
IOS	Serial Input/Output
I1	Input Channel 1
*I1	Load A from LS 4 bits of Upper or Lower Data Reg.
I2C	Input Channel 2 and Complement
*I2C	Load A from MS 4 bits of Upper or Lower Data Reg.
INT1H	Skip if INT1 Input is High
DIN1	Skip if INT1 Flip-flop is Reset
INT0L	Skip if INT0 Input is Low
DIN0	Skip if INT0 Flip-flop is Reset
SEG1	Decode Matrix Output to Channels A and B
*SEG2	Puts MM76C in Counter Mode

*Instruction Functions when in Counter Mode.

INSTRUCTION SET

RAM Addressing Instructions

XAB	Exchange A with BL
LBA	Load BL from A
LB	Load BL, BU → O
EOB	Exclusive OR BU
LBL	Load B Long
INCB	Increment B
DECB	Decrement B
SAG	Special Address Generation

Bit Manipulation Instructions

SB	Set Bit
RB	Reset Bit
SKBF	Skip on Bit False

Register to Register Instructions

LXA	Load X from A
XAS	Exchange A and S
XAX	Exchange A and X

Arithmetic Instructions

A	Add Memory to A
AC	Add Memory with Carry to A
ACSK	Add Memory with Carry to A and Skip on Carry-out
DC	Decimal Correction
COM	Complement A
RC	Reset Carry
SC	Set Carry
SKNC	Skip on No Carry
LAI	Load A with Immediate Field
AISK	Add Immediate and Skip on No Carry-out

ROM Addressing Instructions

RT	Return from Subroutine
RTSK	Return and Skip
T	Transfer on Page
NOP	No Operation
TL	Transfer Long
TLB	Transfer Long Banked
TM	Transfer and Mark
TML	Transfer and Mark Long
TMLB	Transfer and Mark Long Banked

Logical Comparison Instructions

SKMEA	Skip If Memory Equals A
SKBEI	Skip if BL Equals Immediate Field
SKAEI	Skip If A Equals Immediate Field
TAB	Table Look Up

Input/Output Instructions

SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IX	Input X from RIO 5-8
OX	Output X to RIO 5-8
IOA	Input A Receivers to A and output A to RIO 1-4
IOS	Serial Input/Output
I1SK	Input Channel 1. Add to A, Skip if No Carry
I2C	Input Channel 2 and Complement
INT1L	Skip if INT1 Input is Low
INT0H	Skip if INT0 Input is High

Conditional Transfer Instructions

TC	Transfer on Carry Set
TNC	Transfer on No Carry Set
TLC	Transfer Long on Carry Set
TLNC	Transfer Long on No Carry Set
TBF	Transfer on Bit in Memory False
TBT	Transfer on Bit in Memory True
TLBF	Transfer Long on Bit in Memory False
TLBT	Transfer Long on Bit in Memory True
TE	Transfer on A = Memory
TNE	Transfer on A ≠ Memory
TLE	Transfer Long on A = Memory
TLNE	Transfer Long on A ≠ Memory
TIH	Transfer if Input High
TIL	Transfer If Input Low
TLIH	Transfer Long if Input High
TLIL	Transfer Long if Input Low

Register Memory Instructions

L	Load A from Memory
X	Exchange A and Memory
XDSK	Exchange A with Memory. Decrement BL and Skip if BL Counts to 15
XNSK	Exchange A with Memory. Increment BL and Skip if BL Counts to 0

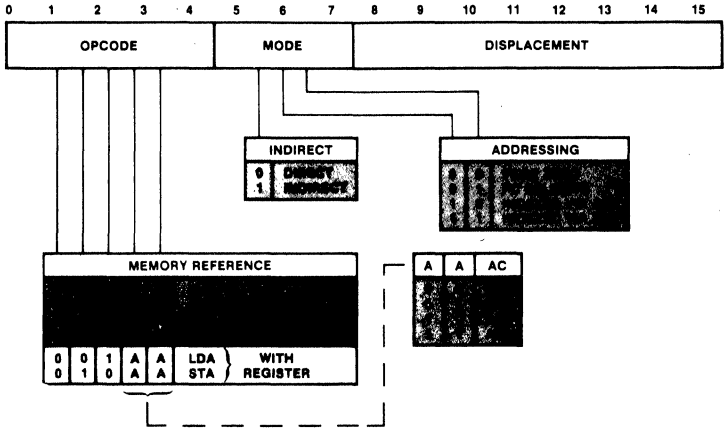
MC68000 INSTRUCTION SET SUMMARY

MNEMONIC	DESCRIPTION
ABCD	Add Decimal with Extend
ADD	Add
ADDX	Add with Extend
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Arithmetic Compare
DCNT	Decrement and Branch Non-Zero
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive Or
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LDM	Load Multiple Registers
LDQ	Load Register Quick
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Two's Complement
NEGX	Two's Complement with Extend
NOP	No Operation
NOT	One's Complement
OR	Logical Or
PACK	Pack ASCII to BCD
PEA	Push Effective Address
RESET	Reset External Devices
ROTL	Rotate Left without Extend
ROTR	Rotate Right without Extend
ROTXL	Rotate Left with Extend
ROTXR	Rotate Right with Extend
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
SCC	Set Conditional
STM	Store Multiple Registers
STOP	Stop
SUB	Subtract
SUBX	Subtract with Extend
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink Stack
UNPK	Unpack BCD to ASCII

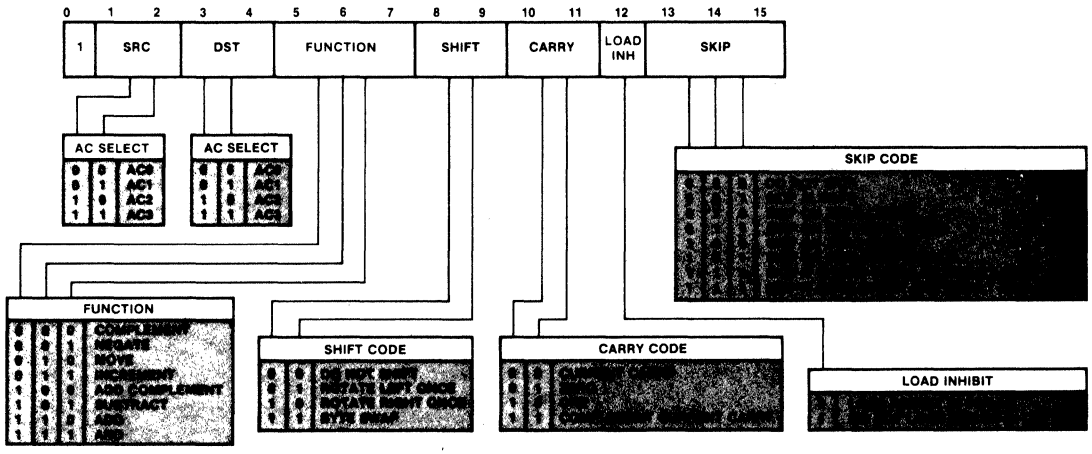
IS107

IS107

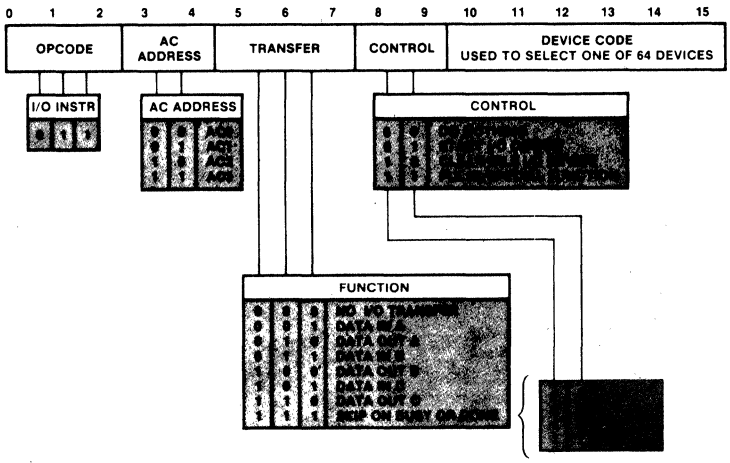
9440 INSTRUCTIONS



Memory Reference instructions without register are used for branching (JMP, JSR) without involving accumulators. These instructions are also used for modifying memory (ISZ, DSZ). Memory Reference instructions with register are used to move 16-bit words between the memory and the accumulators.



Arithmetic/Logic instructions perform arithmetic (ADD, ADC, INC, NEG, SUB) or Boolean (AND, COM, MOV) operations on the contents of two registers. The result of each operation together with the Carry bit can be rotated and tested for skip conditions as part of the same arithmetic/logic instruction; loading in the destination register is optional.



Input/Output instructions move data between the 9440 accumulators and three buffers in the peripheral device interface. These instructions also perform control functions in the I/O device and test the status flags in both the peripheral circuitry and the central processor.

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IS107 Cont'd

IS107 Cont'd

9440 INSTRUCTION EXECUTION

NO.	INSTRUCTION OR OPERATION	CYCLE TYPE AND SEQUENCE*								EXECUTION TIME (μs) @		
		FETCH	READ	WRITE	LD MAR	I/O OUT	I/O IN	WAIT	DCH	8 MHz	10 MHz	12 MHz
1	Jump	1								1.875	1.5	1.25
2	Jump Indirect	3	1	2						5.50	4.4	3.66
3	Jump to Subroutine	1								1.875	1.5	1.25
4	JSR Indirect	3	1	2						5.50	4.4	3.66
5	Increment and Skip if Zero	3	1	2						5.50	4.4	3.66
6	ISZ Indirect	5	1,3	2,4						9.125	7.3	6.07
7	Decrement and Skip if Zero	3	1	2						5.50	4.4	3.66
8	DSZ Indirect	5	1,3	2,4						9.125	7.3	6.07
9	Load Accumulator	2	1							3.75	3.0	2.50
10	LDA Indirect	4	1,3	2						7.375	5.9	4.91
11	Store Accumulator	3	1	2						5.50	4.4	3.66
12	STA Indirect	5	1,3	2,4						9.125	7.3	6.07
13	Complement	1								1.875	1.5	1.25
14	Negate	1								1.875	1.5	1.25
15	Move	1								1.875	1.5	1.25
16	Increment	1								1.875	1.5	1.25
17	Add Complement	1								1.875	1.5	1.25
18	Subtract	1								1.875	1.5	1.25
19	Add	1								1.875	1.5	1.25
20	AND	1								1.875	1.5	1.25
21	ALU with Skip	1,2								3.75	3.0	2.50
22	I/O Data In	2					1			3.125	2.5	2.08
23	I/O Data Out	2				1				3.125	2.5	2.08
24	Skip on Busy or Done	2					1			3.125	2.5	2.08
25	Interrupt	5	3	2,4	1					9.0	7.2	5.98
26	Data Channel								1	1.25	1.0	0.83
27	Wait							1		1.25	1.0	0.83
28	Examine Accumulator					2	1	3		2.50	2.0	1.66
29	Deposit Accumulator					2	1	3		3.125	2.5	1.66
30	Load PC		2				1	3		3.125	2.5	2.08
31	Examine Memory		2				1	3		3.125	2.5	2.08
32	Examine Next		2				1	3		3.125	2.5	2.08
33	Deposit Memory			3	2		1	4		4.75	3.8	3.15
34	Deposit Next			3	2		1	4		4.75	3.8	3.15
35	Continue	2					1			3.125	2.5	2.08

*e.g., No. 6, ISZ Indirect:
1st cycle — READ
2nd cycle — WRITE
3rd cycle — READ
4th cycle — WRITE
5th cycle — FETCH

DATA TRANSFER

MOV = Move:

	76543210	76543210	76543210	76543210
Register/memory to/from register	100010dw	mod reg r/m		
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1
Immediate to register	1011w reg	data	data if w=1	
Memory to accumulator	1010000w	addr-low	addr-high	
Accumulator to memory	1010001w	addr-low	addr-high	
Register/memory to segment register	10001110	mod 0 reg r/m		
Segment register to register/memory	10001100	mod 0 reg r/m		

PUSH = Push:

Register/memory	11111111	mod 110 r/m
Register	01010 reg	
Segment register	000 reg 110	

POP = Pop:

Register/memory	10001111	mod 000 r/m
Register	01011 reg	
Segment register	000 reg 111	

XCHG = Exchange:

Register/memory with register	1000011w	mod reg r/m
Register with accumulator	10010 reg	

IN/INW = Input to AL/AX from:

Fixed port	1110010w	port
Variable port	1110110w	

OUT/OUTW = Output from AL/AX to:

Fixed port	1110011w	port
Variable port	1110111w	
XLAT=Translate byte to AL	11010111	
LEA=Load EA to register	10001101	mod reg r/m
LDS=Load pointer to DS	11000101	mod reg r/m
LES=Load pointer to ES	11000100	mod reg r/m
LAHF=Load AH with flags	10011111	
SAHF=Store AH into flags	10011110	
PUSHF=Push flags	10011100	
POPF=Pop flags	10011101	

ARITHMETIC

ADD = Add:

Reg./memory with register to either	000000dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s:w=01
Immediate to accumulator	0000010w	data	data if w=1	

ADC = Add with carry:

Reg./memory with register to either	000100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s:w=01
Immediate to accumulator	0001010w	data	data if w=1	

INC = Increment:

Register/memory	1111111w	mod 000 r/m
Register	01000 reg	
AAA=ASCII adjust for add	00110111	
DAA=Decimal adjust for add	00100111	

SUB = Subtract:

Reg./memory and register to either	001010dw	mod reg r/m		
immediate from register/memory	100000sw	mod 101 r/m	data	data if s:w=01
Immediate from accumulator	0010110w	data	data if w=1	

SBB = Subtract with borrow

Reg./memory and register to either	000110dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s:w=01
Immediate from accumulator	0001110w	data	data if w=1	

DEC = Decrement:

	76543210	76543210	76543210	76543210
Register/memory	1111111w	mod 001 r/m		
Register	01001 reg			
NEG Change sign	1111011w	mod 011 r/m		

CMP = Compare:

Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s:w=01
Immediate with accumulator	0011110w	data	data if w=1	
AAS=ASCII adjust for subtract	00111111			
DAS=Decimal adjust for subtract	00101111			
MUL=Multiply (unsigned)	1111011w	mod 100 r/m		
IMUL=Integer multiply (signed)	1111011w	mod 101 r/m		
AAM=ASCII adjust for multiply	11010100	00001010		
DIV=Divide (unsigned)	1111011w	mod 110 r/m		
IDIV=Integer divide (signed)	1111011w	mod 111 r/m		
AAD=ASCII adjust for divide	11010101	00001010		
CBW=Convert byte to word	10011000			
CWD=Convert word to double word	10011001			

LOGIC

NOT=Invert	1111011w	mod 010 r/m
SHL/SAL=Shift logical/arithmetic left	110100vw	mod 100 r/m
SHR=Shift logical right	110100vw	mod 101 r/m
SAR=Shift arithmetic right	110100vw	mod 111 r/m
ROL=Rotate left	110100vw	mod 000 r/m
ROR=Rotate right	110100vw	mod 001 r/m
RCL=Rotate through carry flag left	110100vw	mod 010 r/m
RCR=Rotate through carry right	110100vw	mod 011 r/m

AND = And:

Reg./memory and register to either	001000dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1
Immediate to accumulator	0010010w	data	data if w=1	

TEST = And function to flags, no result:

Register/memory and register	1000010w	mod reg r/m		
Immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1
Immediate data and accumulator	1010100w	data	data if w=1	

OR = Or:

Reg./memory and register to either	000010dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1
Immediate to accumulator	0000110w	data	data if w=1	

XOR = Exclusive or:

Reg./memory and register to either	001100dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1
Immediate to accumulator	0011010w	data	data if w=1	

STRING MANIPULATION

REP=Repeat	1111001z
MOVB/MOVW=Move byte/word	1010010w
CMPB/CMPW=Compare byte/word	1010011w
SCAB/SCAW=Scan byte/word	1010111w
LODB/LODW=Load byte/wd to AL/AX	1010110w
STOB/STOW=Stor byte/wd frm AL/A	1010101w

Cont'd on next page

IS108 Cont'd

CONTROL TRANSFER

CALL = Call:	76543210	76543210	76543210
Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 010 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 011 r/m	

JMP = Unconditional Jump:			
Direct within segment	11101001	disp-low	disp-high
Direct within segment-short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	

RET = Return from CALL:			
Within segment	11000011		
Within seg. adding immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment, adding immediate to SP	11001010	data-low	data-high

JE/JZ=Jump on equal/zero	01110100	disp
JL/JNGE=Jump on less/not greater or equal	01111100	disp
JLE/JNG=Jump on less or equal/not greater	01111110	disp
JB/JNAE=Jump on below/not above or equal	01110010	disp
JBE/JNA=Jump on below or equal/ not above	01110110	disp
JP/JPE=Jump on parity/parity even	01111010	disp
JO=Jump on overflow	01110000	disp
JS=Jump on sign	01111000	disp
JNE/JNZ=Jump on not equal/not zero	01110101	disp
JNL/JGE=Jump on not less/greater or equal	01111101	disp
JNLE/JG=Jump on not less or equal/ greater	01111111	disp

	76543210	76543210
JNB/JAE Jump on not below/above or equal	01110011	disp
JNBE/JA=Jump on not below or equal/above	01110111	disp
JNP/JPO=Jump on not par/par odd	01111011	disp
JNO Jump on not overflow	01110001	disp
JNS Jump on not sign	01111001	disp
LOOP=Loop CX times	11100010	disp
LOOPZ/LOOPE Loop while zero/equal	11100001	disp
LOOPNZ/LOOPNE Loop while not zero/equal	11100000	disp
JCXZ Jump on CX zero	11100011	disp

INT = Interrupt		
Type specified	11001101	type
Type 3	11001100	
INTO=Interrupt on overflow	11001110	
IRET=Interrupt return	11001111	

PROCESSOR CONTROL

CLC=Clear carry	11111000	
CMC=Complement carry	11110101	
STC=Set carry	11111001	
CLD=Clear direction	11111100	
STD=Set direction	11111101	
CLI=Clear interrupt	11111010	
STI=Set interrupt	11111011	
HLT=Halt	11110100	
WAIT=Wait	10011011	
ESC=Escape (to external device)	11011 x	mod x r/m
LOCK=Bus lock prefix	11110000	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to"; if d = 0 then "from"
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

meca-43 instructions

Instruction Name	Mnemonic	Op. Code	Instruction Name	Mnemonic	Op. Code	Instruction Name	Mnemonic	Op. Code	Instruction Name	Mnemonic	Op. Code
Data Transfer (A)			Add (A)			Logical (A)			Transfer (BR)		
Load (A)	LDA	14	Add to (A)	ADD	02	Logical Product	AND	04	Transfer On (BR)	TBRI	21
Load (A) From (xi)	LAXi	31	Add (B) To (A)	ADBA	26	Logical Sum	LOR	34	Transfer On (BR)	TBRP	21
Load (A) From (B)	LAFB	06	Add (xi) To (A)	AXiA	26	Exclusive Or	XOR	23			
Load (A) From (BR)	LABR	31							Skip		
Immediate Byte To (A)	IBAR	35							Skip More Positive Than (A)	SMP	36
Exchange Bytes of (A)	EXBA	35				Shift (A)			Skip If Discrete 0	DS0	05
Store (A)	STA	33	Add (B)			Shift (A) Right	SAR	07	Skip If Discrete 1	DS1	05
			Add To (B)	ADB	03	Shift (A) Left	SAL	20			
			Add (A) To (B)	ADAB	26						
Data Transfer (B)						Shift (B)			Input Output		
Load (B)	LDB	11				Shift (B) Right	SBR	07	Input To (A)	INA	17
Load (B) From (A)	LBFA	06	Add (X)			Shift (B) Left	SBL	20	Input To (B)	INB	17
Immediate Byte To (B)	IBBR	06	Add to (X) Direct	AXD	15				Output From (A)	OTA	16
Exchange Bytes Of (B)	EXBB	35	Add To (X) Immediate	AXI	15				Output From (B)	OTB	16
Store (B)	STB	01				Shift (A) And (B)			Double ADD	DAD	03
						Shift Double Right	SDR	06	Double SUBTRACT	DSU	13
			Add (BR)			Shift Double Left	SDL	35	Double LOAD	DLD	11
Data Transfer (X)			Add To (BR) Direct	ABRD	15	Normalize	NRM	26	Double STORE	DST	01
Load (X) Direct	LXD	24	Add To (BR) Immediate	ABRI	15				Double MULTIPLY	DML	37
Load (X) Immediate	LXI	24							Double DIVIDE	DDV	27
Load (xi) From (A)	LXiA	31				Transfer Unconditional			Double FLOAT	FLD	26
Store (X) Common	SXC	25				Transfer	TRA	30	Double FIX	FXD	26
Store (X) Direct	SXD	25	Subtract (A)			Transfer	TRS	00	Double Float ADD	FAD	03
			Subtract From (A)	SUB	12	Transfer and Return	TTR	00	Double Float SUBTRACT	FSD	13
			Reverse Subtract (A)	RSA	10				Double Float MULTIPLY	FMD	37
			Subtract (B) From (A)	SBFA	35				Double Float DIVIDE	FDD	27
Data Transfer (BR)						Transfer (A)			Single FLOAT	FLS	26
Load (BR) Direct	LBRD	24	Subtract (B)			Transfer If (A)	TRZ	32	Single FIX	FXS	26
Load (BR) Immediate	LBRI	24	Subtract From (B)	SBB	13	Transfer If (A)	TRN	22	Single Float ADD	FAS	03
Load (BR) From (A)	LBRA	31							Single Float SUBTRACT	FSS	13
Immediate Byte To (BR)	IBBA	06	Multiply Divide			Transfer (X)			Single Float MULTIPLY	FMS	37
Store (BR) Common	SBRC	25	Multiply	MPY	37	Transfer On Indirect	TXI	21	Single Float DIVIDE	FDS	27
Store (BR) Direct	SBRD	25	Divide	DIV	27	Transfer On (Xi) Rel. to (P)	TXP	21			

INSTRUCTION TIMES

The instruction times of a representative group of the H18 instruction set are presented below.

ADD REGISTER	0.25 μsec
ADD DIRECT	0.5 μsec
ADD INDEXED	0.75 μsec
MULTIPLY	4 μsec
DIVIDE	5.75 μsec
SINE-COSINE	19.75 μsec
SQUARE ROOT	13.75 μsec
BIT SET/RESET	0.75 μsec
BRANCH	0.75/1.0 μsec

INSTRUCTION SET

The H18 provides single instructions which do the work usually performed by subroutines in other comparable processors. Included in the 130 member instruction set are:

- 16-bit, 32-bit, and 48-bit instructions
- High speed signed MULTIPLY and DIVIDE
- SINE, COSINE, and SQUARE ROOT
- Block and word manipulation
- Test and set capability of any bit in a 64K word memory
- Extensive logical operations
  Single and double shifts
- Built-in self-test for fault detection and isolation
- Multiprocessor coordination instructions with memory lock capability
- Scheduling instruction for executive control
- ABSOLUTE VALUE, single/double precision
- LIMIT, limits a value x between an upper and lower bound
- LOAD FIELD, loads a 1 to 16 bit field from memory to any register (unpacks data)
- STORE FIELD, stores a 1 to 16 bit field from any register to any place in memory (packs data)
- DECREMENT and BRANCH for efficient loop control

ADDRESSING MODES

The following 11 addressing modes were chosen based on statistical studies of avionic systems.

	RANGE
Direct Short	0 - 255
Direct Extended	0 - 64K
Indexed Short	0 - 64K
Indexed Long	0 - 64K
Bit Short	256 - 383
Bit Extended	0 - 64K
Relative	PC ± 128
Indirect (Optional Indexing)	0 - 64K
Register	8
Immediate	8 or 16 bits
Stack	

MIPROC Instruction Sets

KEY TO INSTRUCTION SET CONTENTS

Basic Hardware—Instructions relating to basic hardware are those shown without shading.

Extended Hardware—With the extended hardware the instruction set includes the basic hardware instruction and those shown shaded.

Hardware Instruction Set—These are instructions implemented by the hardware.

Assembler Instruction Set—These instructions are recognized by the assembler and are converted into one or more hardware instructions.

Mnemonic—The mnemonic is a representation of the instruction as recognized by the assembler.

Argument—The contents to be inserted in the argument are defined by the symbols used in this column.

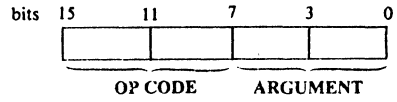
Object Code—The hexadecimal representation of the instruction word.

Function—A symbolic representation of the function as defined by the following instruction sets.

Addressing Method—The addressing method used as defined above.

Execution Cycles—The number of cycles taken to perform the instruction. Each cycle takes 350ns for Basic Miproc and 385ns for the Extended version.

INSTRUCTION FORMAT



The 16-bit instruction word is represented by four hexadecimal characters. The first two represent the op-codes; the others being the argument.

MEMORY ACCESS METHODS

Program Memory
Program Memory is accessed via the Program Counter. Any one of the 64K words locations can be accessed directly.

Data Memory
Data Memory is accessed in one of seven modes: Direct, Indirect, Indexed, Indexed Direct, Indexed Indirect, Auto-Indexed Direct, Auto-Indexed Indirect.

Direct Addressing
The data memory location is defined by the combination of the argument (least significant byte) of the instruction word and the most significant byte of the MAR.

Indirect Addressing
Indirect Addressing uses the contents of the MAR to address any location in the data memory. The content of MAR has to be set to the desired address before an instruction using Indirect addressing is executed.

Indexed
Indexed addressing uses the full 16-bit contents of the optional Index register to address a location in data memory.

Indexed Direct
The contents of the X register are added to the Direct address found from the argument of the instruction and the most significant byte of the MAR to give the data location required.

Indexed Indirect
The data memory address is found from the sum of the contents of the X register and MAR.

Auto-Indexed Direct
Auto-Indexed Direct addressing uses the same method as Indexed Direct but the X register is then modified. The X register contents are incremented by 1 and then tested for zero. If a zero is found, the next instruction is treated as a NOP.

Auto-Indexed Indirect
Auto-Indexed Indirect is an Indexed Indirect instruction modified in the same way as the Auto Indexed Direct.

TABLE OF SYMBOLS USED

A	contents of A register.
E	contents of E register.
A, E	contents of A and E register forming a 32-bit word.
P	contents of Program Counter.
M	contents of MAR.
X	contents of X register.
$A_{[n]}$	contents of bit n of A register.
C	output of C buffer. (Literal mode.)
D	contents of data memory location in current page, addressed by D buffer (i.e. DIRECTLY addressed).
DI	contents of data memory location addressed by M register (i.e. INDIRECTLY addressed).
DW	contents of data memory addressed by X register (X-addressed).
DX	contents of data memory addressed by current page plus D buffer plus X, (i.e. indexed direct).
DK	contents of data memory addressed by the MAR plus X.
D*	contents of data memory location in current interrupt trap vector page addressed by D buffer.
−A	2's complement of contents of A register.
Ā	1's complement of contents of A register.
plus	arithmetic ADD operator.
−	arithmetic SUBTRACT operator.
•	arithmetic MULTIPLY operator.
÷	arithmetic integer DIVIDE operator; R denotes the remainder.
+	logical OR operator.
•	logical AND operator.
⊕	logical EXCLUSIVE OR operator.
→	assignment of L.H. value to R.H. location.
S	undefined assembler code argument used for direct data word location—programmer inserts SYMBOLIC or NUMERIC (decimal or hex) data.
L	undefined assembler code argument, program lable—programmer inserts LABEL.
N1, N2	undefined assembler code arguments, used to define contents of MAR—programmer inserts NUMERIC (decimal or hex) data.
XX	undefined object code argument—assembler (or object code programmer) inserts 2 hex characters.
#	prefix used to identify numbers as hexadecimal.

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IS111 Cont'd

IS111 Cont'd

Hardware Instruction Set

MNEMONIC	ARGUMENT	OBJECT CODE	FUNCTION	ADDRESSING METHOD	EXECUTION CYCLES
MOVE					
Load A					
LDA	S	00XX	D → A	Direct	1
LDAI		3800	DI → A	Indirect	1
LDAW		D100	DW → A	Indexed	1
LDAX	S	CEXX	DX → A	Indexed Direct	1
LDAK		CF00	DK → A	Indexed Indirect	1
LDAT	S	D0XX	DX → A, X plus 1 → X	Auto-Indexed Direct	1
LDAS	S	D200	DK → A, X plus 1 → X	Auto-Indexed Indirect	1
LDAV	S	19XX	D* → A		
Load E					
LDE	S	01XX	D → E	Direct	1
LDEI		3C00	DI → E	Indirect	1
LDEW		D600	DW → E	Indexed	1
LDEX	S	D3XX	DX → E	Indexed Direct	1
LDEK		D400	DK → E	Indexed Indirect	1
LDET	S	D5XX	DX → E; X plus 1 → X	Auto-Indexed Direct	1
LDES		D700	DK → E; X plus 1 → X	Auto-Indexed Indirect	1
Load X					
LDX	S	E4XX	D → X	Direct	1
Store A					
STA	S	02XX	A → D	Direct	1
STAI		3300	A → DI	Indirect	1
STAW		DB00	A → DW	Indexed	1
STAX	S	D8XX	A → DX	Indexed Direct	1
STAK		D900	A → DK	Indexed Indirect	1
STAT	S	DAXX	A → DX, X plus 1 → X	Auto-Indexed Direct	1
STAS		DC00	A → DK, X plus 1 → X	Auto-Indexed Indirect	1
STAV	S	4EXX	A → D*		
Store E					
STE	S	27XX	E → D	Direct	1
STEI		3D00	E → DI	Indirect	1
STEW		E000	E → DW	Indexed	1
STEX	S	DDXX	E → DX	Indexed Direct	1
STEK		DE00	E → DK	Indexed Indirect	1
STET	S	DFXX	E → DX; X plus 1 → X	Auto-Indexed Direct	1
STES		E100	E → DK, X plus 1 → X	Auto-Indexed Indirect	1
Store X					
STX	S	E5XX	X → D	Direct	1
Store P					
STP	S	03XX	P → D	Direct	1
STPX	S	EBXX	P → DX	Indexed Direct	1
Register to Register					
RAE		0D00	A → E		1
REA		0E00	E → A		1
RPA		0F00	P → A		1
RAM		3A00	A → M		1
REM		3B00	E → M		1
RAX		4C00	A → X		1
RXA		4B00	X → A		1
REX		E300	E → X		1
RXE		E200	X → E		1
RMA		4D00	M → A		1
RME		FD00	M → E		1
Load Constant					
LCA	+S, −S	10XX, 16XX	C → A		1
LCE	+S, −S	35XX, 17XX	C → E		1
PAGE	N1, (N2)	9EXX-ADXX, 8EXX-9DXX	C → M		1
LCX	−S	50XX	C → X (-ve Const.)		1
JUMP					
JMP	S	1AXX	D → P	Direct	1
JMPI		8C00	DI → P	Indirect	1
JMPX	S	8DXX	DX → P	Indexed Direct	1
Jump to A					
JMA		1F00	A → P		1
Jump Literal					
JMPC	L	21XX, 63XX-71XX	C → P		1
LOGICAL					
AND					
AND	S	06XX	A·D → A	Direct	1
ANDI		4400	A·DI → A	Indirect	1
ANDW		B100	A·DW → A	Indexed	1
ANDX	S	AEXX	A·DX → A	Indexed Direct	1
ANDK		AF00	A·DK → A	Indexed Indirect	1
ANDT	S	B0XX	A·DX → A, X plus 1 → X	Auto-Indexed Direct	
ANDS		B200	A·DK → A; X plus 1 → X	Auto-Indexed Indirect	
AND E					
ANDE		4700	A·E → A		1
AND Constant					
ANDC	S	B3XX	A·C → A		1
OR					
ORA	S	08XX	A + D → A	Direct	1
ORAI		4500	A + DI → A	Indirect	1
ORAW		B700	A + DW → A	Indexed	1
ORAX	S	B4XX	A + DX → A	Indexed Direct	1
ORAK		B500	A + DK → A	Indexed Indirect	1
ORAT	S	B6XX	A + DX → A, X plus 1 → X	Auto-Indexed Direct	
ORAS		B800	A + DK → A, X plus 1 → X	Auto-Indexed Indirect	
OR E					
ORAE		4800	A + E → A		1
OR Constant					
ORAC	S	B9XX	A + C → A		1
EX OR					
ERA	S	07XX	A ⊕ D → A	Direct	1
ERAI		4600	A ⊕ DI → A	Indirect	1
ERAW		FA00	A ⊕ DW → A	Indexed	1
ERAX	S	F7XX	A ⊕ DX → A	Indexed Direct	1
ERAK		F600	A ⊕ DK → A	Indexed Indirect	1
ERAT	S	F9XX	A ⊕ DX → A; X plus 1 → X	Auto-Indexed Direct	
ERAS		FB00	A ⊕ DK → A; X plus 1 → X	Auto-Indexed Indirect	
EX OR E					
ERAE		4900	A ⊕ E → A		1
EX OR Constant					
ERAC	S	FCXX	A ⊕ C → A		1
Bit Set					
BSET	S	28XX, 7300-7A00	1 → A[n]		1
Bit Clear					
BCLR	S	29XX, 7CFF-83FF	0 → A[n]		1
Clear A					
CLRA		1400	0 → A		1
Set A					
SOA		1500	−1 → A		1
Invert A					
NEGA		1300	$\bar{A}$ → A		1
ARITHMETIC					
Add					
ADD	S	04XX	A plus D → A	Direct	1
ADDI		3400	A plus DI → A	Indirect	1
ADDW		E800	A plus DW → A	Indexed	1
ADDX	S	E6XX	A plus DX → A	Indexed Direct	1
ADDK		E700	A plus DK → A	Indexed Indirect	1
ADDT	S	4AXX	A plus DX → A	Auto-Indexed Direct	
ADDS		E900	A plus DK → A,	Auto-Indexed Indirect	
Add E					
ADDE		3700	A plus E → A		1
Add X					
ADRX		EA00	A plus X → A		1
Add Constant					
ADDC	S	42XX	A plus C plus 1 → A		1
Subtract					
SUB	S	05XX	A − D → A	Direct	1
SUBI		4100	A − DI → A	Indirect	1
SUBW		EF00	A − DW → A	Indexed	1
SUBX	S	ECXX	A − DX → A	Indexed Direct	1
SUBK		ED00	A − DK → A	Indexed Indirect	1
SUBT	S	EFXX	A − DX → A;	Auto-Indexed Direct	
SUBS		F000	A − DK → A;	Auto-Indexed Indirect	
Subtract E					
SUBE		3E00	A − E → A		1
Subtract Constant					
SUBC	S	43XX	A − C → A		1
Multiply/Add					
MLL	S	18XX	E•D plus A → A, I	Direct	16 to 32
§ MLLI		3F00	E•D plus A → A, E	Indirect	
§ MLLW		F300	E•DW plus A → A, E	Indexed	
§ MLLX		F1XX	E•DX plus A → A, E	Indexed Direct	
§ MLLK		F200	E•DK plus A → A, E	Indexed Indirect	
Divide					
DLL	S	19XX	A, I ÷ D → E; 2•R → A	Direct	16 to 32
Increment A					
INCA		1100	A plus 1 → A		1
Decrement A					
DECA		1200	A − 1 → A		1
SHIFT (+ symbol used to denote plus operator in shift function description)					
Shift Left–Zero In					
SLZ		1C00	A[n] → A[n + 1]; 0 → A[0] E[n] → E[n + 1]; 0 → E[0]		1
Shift Left–One In					
SLO		0A00	A[n] → A[n + 1]; 1 → A[0] E[n] → E[n + 1]; 0 → E[0]		1
Shift Left–Extended					
SLE		0C00	A[n] → A[n + 1]; E[15] → A[0] E[n] → E[n + 1]; 0 → E[0]		1
SLET		BB00	A[n] → A[n + 1]; E[15] → A[0] E[n] → E[n + 1]; 0 → E[0]	Auto Indexed	1
Rotate Left					
SLR		1B00	A[n] → A[n + 1]; A[15] → A[0] E[n] → E[n + 1]; 0 → E[0]		1
Shift Right–Zero In					
SRZ		1D00	A[n] → A[n − 1]; 0 → A[15] E[n] → E[n − 1]; A[0] → E[15]		1
Shift Right–One In					
SRO		0B00	A[n] → A[n − 1]; 1 → A[15] E[n] → E[n − 1]; A[0] → E[15]		1
Shift Right–Sign Extended					
SRS		4F00	A[n] → A[n − 1]; A[15] → A[15] E[n] → E[n − 1]; A[0] → E[15]		1
§ SRST		B700	A[n] → A[n − 1]; A[15] → A[15] L[n] → E[n − 1]; A[0] → E[15]	Auto Indexed	
Rotate Right					
SRR		0900	A[n] → A[n − 1]; A[0] → A[15] E[n] → E[n − 1]; A[0] → E[15]		1
CONTROL					
SKZ		2C00	Skip if A is Zero		1
SKNZ		2D00	Skip if A is Not Zero		1
SKN		2E00	Skip if A Negative		1
SKZP		2F00	Skip if A Zero/pos.		1
BSKO	S	5300-6200	Skip if Bit is One		1
BSKZ	S	BE00-CD00	Skip if Bit is Zero		1
NOP		§ FFFF	No Operation		1
NOPT		7200	X plus 1 → X. Skip if X becomes Zero		1
SKC		2A00	Skip if Carry flag set		1
SKNC		2000	Skip if Carry flag clear		1
SKV		2300	Skip if Overflow flag set		1
SKNV		2B00	Skip if Overflow flag clear		1

Cont'd on next page

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IS111 Cont'd

Hardware Instruction Set (cont.)

MNEMONIC	ARGUMENT	OBJECT CODE	FUNCTION	ADDRESSING METHOD	EXECUTION CYCLES
INPUT/OUTPUT					
Input to A					
INA	S	24XX	Input Channel S → A		1
Output from A					
OTA	S	25XX	A → Output Channel S		1

MNEMONIC	ARGUMENT	OBJECT CODE	FUNCTION	ADDRESSING METHOD	EXECUTION CYCLES
INTERRUPT					
Interrupt On					
ION		BA00	1 → Interrupt Enable		1
Interrupt Off					
IOF		BB00	0 → Interrupt Enable		1
Return from Interrupt					
IONR	S	BCXX	D° → P; 1 → Interrupt Enable		1
Load M Direct Vectored					
LDM	S	32XX	D° → M		1
Store M Direct Vectored					
STM	S	31XX	M → D°		1
LDMZ		3600	DW → M X plus 1 → X		1

Assembler Instruction Set

MNEMONIC	ARGUMENT	OBJECT CODE	FUNCTION	ADDRESSING METHOD	EXECUTION CYCLES
ARITHMETIC					
Multiply					
MUQ	S	1400 (CLRA)	0 → A	Direct	
		18XX (MLL)	E • D plus A → A, E		(16 to 32) + 1
MUQI		1400 (CLRA)	0 → A		
		3F00	E • DI plus A → A, E	Indirect	(16 to 32) + 1
MUQW		1400 (CLRA)	0 → A		
		F300	E • DW plus A → A, E	Indexed	(16 to 32) + 1
			DW is limited to being a positive number		
MUQX	S	1400 (CLRA)	0 → A	Indexed Direct	(16 to 32) + 1
		F1XX	E • DX plus A → A, E		
MUQK		1400 (CLRA)	0 → A	Indexed Indirect	(16 to 32) + 1
		F200	E • DK plus A → A, E		
Multiply A Direct					
MUL	S	0D00 (RAE)	A → E		
		1400 (CLRA)	0 → A	Direct	(16 to 32) + 2
		18XX (MLL)	E • D plus A → A, E		
Divide E					
DIQ	S	1400 (CLRA)	0 → A		
		19XX (DLL)	E ÷ D → E, 2°R → A	Direct	(16 to 32) + 1
Divide A					
DIV	S	0D00 (RAE)	A → E		
		1400 (CLRA)	0 → A		
		19XX (DLL)	E ÷ D → E; 2°R → A	Direct	(16 to 32) + 2
2's Complement A					
CMPA		1300 (NEGA)	Ā → A		
		1100 (INCA)	A plus 1 → A		2
Increment X					
INCX		7200 (NOPT)	X plus 1 → X		2
		1E00 (NOP)			
MEMORY MODIFICATION					
Increment and Load Pointer					
LDIM	S	00XX (LDA)	D → A	Direct	4
		1100 (INCA)	A plus 1 → A		
		02XX (STA)	A → D		
		3A00 (RAM)	A → M		
Decrement and Load Pointer					
LDDM	S	00XX (LDA)	D → A		
		1200 (DECA)	A − 1 → A	Direct	4
		02XX (STA)	A → D		
		3A00 (RAM)	A → M		
Index Pointer By E and Load					
LDEM	S	00XX (LDA)	D → A	Direct	4
		3700 (ADDE)	A plus E → A		
		02XX (STA)	A → D		
		3A00 (RAM)	A → M		
Increment and Skip if Zero					
ISZ	S	00XX (LDA)	D → A	Direct	4
		1100 (INCA)	A plus 1 → A		
		02XX (STA)	A → D		
		2C00 (SKZ)	Skip if Zero		
Decrement and Skip if Zero					
DSZ	S	00XX (LDA)	D → A	Direct	4
		1200 (DECA)	A − 1 → A		
		02XX (STA)	A → D		
		2C00 (SKZ)	Skip if Zero		

MNEMONIC	ARGUMENT	OBJECT CODE	FUNCTION	ADDRESSING METHOD	EXECUTION CYCLES
MEMORY MODIFICATION					
Load & Increment X					
LDIX	S	CEXX (LDAX)	DX → A	Indexed Direct	3
		1100 (INCA)	A plus 1 → A		
		D8XX (STAX)	A → DX		
Load & Decrement X					
LDDX	S	CEXX (LDAX)	DX → A	Indexed Direct	3
		1200 (DECA)	A minus 1 → A		
		D8XX (STAX)	A → DX		
Load & Add E					
LAEX	S	CEXX (LDAX)	DX → A	Indexed Direct	3
		3700 (ADDE)	A plus E → A		
		D8XX (STAX)	A → DX		
Increment and Skip if Zero					
ISZX	S	CEXX (LDAX)	DX → A	Indexed Direct	4
		1100 (INCA)	A plus 1 → A		
		D8XX (STAX)	A → DX		
		2C00 (SKZ)	Skip if A → 0		
Decrement & Skip if Zero					
DSZX	S	CEXX (LDAX)	DX → A	Indexed Direct	4
		1200 (DECA)	A minus 1 → A		
		D8XX (STAX)	A → DX		
		2C00 (SKZ)	Skip if A → 0		
SHIFT					
SLZT		1C00 (SLZ)	SLZ (see basic instruction set)		
		7200 (NOPT)	X plus 1 → X; Skip if X becomes Zero		2
SLOT		0A00 (SLO)	SLO (see basic instruction set)		
		7200 (NOPT)	X plus 1 → X; Skip if X becomes Zero		2
SLRT		1B00 (SLR)	SLR (see basic instruction set)		
		7200 (NOPT)	X plus 1 → X; Skip if X becomes Zero		2
SRZT		1D00 (SRZ)	SRZ (see basic instruction set)		
		7200 (NOPT)	X plus 1 → X; Skip if X becomes Zero		2
SROT		0B00 (SRO)	SRO (see basic instruction set)		
		7200 (NOPT)	X plus 1 → X; Skip if X becomes Zero		2
SRRT		0960 (SRR)	SRR (see basic instruction set)		
		7200 (NOPT)	X plus 1 → X; Skip if X becomes Zero		2
JUMP & SUBROUTINE					
Jump to Subroutine					
JPS	L	03XX (STP)	P → D		2
		See JMPC	C → P		
Return from Subroutine					
RTS	L	00XX (LDA)	D → A		
		4201 (ADDC)	A plus 2 → A		3
		1F00 (JMA)	A → P		
Jump above 4K					
JUMP	L	1AXX (JMP)	D → P		1
Jump to Subroutine above 4K					
JUPS	L	$03X_1X_2$ (STP)	P → D_2		
		$1AX_1X_2$ (JMP)	D_2 → P		2

§ *Recognized by the PDP 11 assembler only from Version 1 Edit 3.*

IS112

IS112

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle	Hexadecimal Opcode
Accumulator	ADD A,R_r	Add register to A	1	1	68-6F
	ADD A,@R	Add data memory to A	1	1	60-61
	ADD A,#data	Add immediate to A	2	2	03
	ADDC A,R_r	Add register with carry	1	1	78-7F
	ADDC A,@R	Add data memory with carry	1	1	70-71
	ADDC A,#data	Add immediate with carry	2	2	13
	ANL A,R_r	And register to A	1	1	58-5F
	ANL A,@R	And data memory to A	1	1	50-51
	ANL A,#data	And immediate to A	2	2	53
	ORL A,R_r	Or register to A	1	1	48-4F
	ORL A,@R	Or data memory to A	1	1	40-41
	ORL A,#data	Or immediate to A	2	2	43
	XRL A,R_r	Exclusive Or register to A	1	1	D8-DF
	XRL A,@R	Exclusive Or data memory to A	1	1	D0-D1
	XRL A,#data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67
Input/Output	IN A, P_p	Input port to A	1	2	08,09,0A
	OUT P_pA	Output A to port	1	2	90,39,3A
	MOVD A,P_p	Input expander port to A	1	2	0C-0F
	MOVD P_p,A	Output A to expander port	1	2	3C-3F
	ANLD P_p,A	And A to expander port	1	2	9C-9F
	ORLD P_p,A	Or A to expander port	1	2	8C-8F
Registers	INC R_r	Increment register	1	1	18-1F
	INC @R	Increment data memory	1	1	10-11
Branch	JMP addr	Jump unconditional	2	2	04,24,33,64, 84,A4,C4,E4
	JMPP @A	Jump indirect	1	2	B3
	DJNZ R,addr	Decrement register and jump on R not zero	2	2	E8-EF
	JC addr	Jump on carry = 1	2	2	F6
	JNC addr	Jump on carry = 0	2	2	E6
	JZ addr	Jump on A zero	2	2	C6
	JNZ addr	Jump on A not zero	2	2	96
	JT0	Jump on T0 = 1	2	2	36
	JNT0	Jump on T0 = 0	2	2	26
	JT1 addr	Jump on T1 = 1	2	2	56
	JNT1 addr	Jump on T1 = 0	2	2	46
	JTF addr	Jump on timer flag	2	2	16
Subroutine	CALL	Jump to subroutine	1	2	14,34,54,74, 94,B4,D4,F4
	RET	Return	1	2	83
Flags	CLR C	Clear carry	1	1k	97
	CPL C	Complement carry	1	1	A7
Data Moves	MOV A,R_r	Move register to A	1	1	F8-FF
	MOV A,@R	Move data memory to A	1	1	F0-F1
	MOV A,#data	Move immediate to A	2	2	23
	MOV R_r,A	Move A to register	1	1	A8-AF
	MOV @R,A	Move A to data memory	1	1	A0-A1
	MOV R_r,#data	Move immediate to register	2	2	B8-BF
	MOV @R,#data	Move immediate to data memory	2	2	B0-B1
	XCH A,R_r	Exchange A and register	1	1	28-2F
	XCH A,@R	Exchange A and data memory	1	1	20-21
	XCHD A,@R	Exchange nibble of A and register	1	1	30-'31
	MOVP A,@A	Move to A from current page	1	2	A3
Timer/Counter	MOV A,T	Read timer/counter	1	1	42
	MOV T,A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
A/D Converter	RAD	Move conversion result register to A	1	2	80
	SEL AN0	Select analog input zero	1	1	85
	SEL AN1	Select analog input one	1	1	95
Interrupts	EN I	Enable external interrupt	1	1	05
	DIS I	Disable external interrupt	1	1	15
	EN TCNTI	Enable timer/counter interrupt	1	1	2 5
	DIS TCNTI	Disable timer/counter interrupt	1	1	35
	RET I	Return from interrupt	1	2	93
	NOP	No operation	1	1	00

SYMBOLS AND ABBREVIATIONS USED

A	Accumulator
addr	11-Bit Program Memory Address
AN0, AN1	Analog Input 0, Analog Input 1
CNT	Event Counter
data	8-Bit Number or Expression
I	Interrupt
P	Mnemonic for "in-page" Operation
P_p	Port Designator (P = 1, 2 or 4-7)
R_r	Register Designator (r = 0-7)
T	Timer
T0, T1	Test 0, Test 1
#	Immediate Data Prefix
@	Indirect Address Prefix

IS113

S2000 Family Instruction Set Summary

The S2000 and S2150 contain 51 instructions, all single byte, with 49 that are single cycle. The S2200 and S2400 contain 59 instructions, of which 52 are single cycle and single byte.

Nearly all S2000/2150 instructions are common to the entire family, which allows the programmer to develop software expertise and easily move up the S2000 product line.

Register Instructions

S2000/2150	S2200/2400	
LAI X	LAI X	X→ACC, 0≤X≤15; (In S2000/2150 Select I and K Inputs also)
LAB	LAB	BL→ACC
LAE	LAE	E→ACC
XAB	XAB	BL→ACC
XABU	XABU	BU→ACC, (IN S2150, BITS 2, 1, AND 0; IN OTHERS, BITS 1 AND 0 ONLY)
XAE	XAE	ACC→E
LBE Y	LBE Y	Y→BU, E→BL, 0≤Y≤3
LBZ Y	LBZ Y	Y→BU, 0→BL, 0≤Y≤3
LBF Y		Y→BU, 15→BL, 0≤Y≤3
LBEP Y		Y→BU, E+1→BL, 0≤Y≤3
	SRB	1→BA
	RRB	0→BA
	LMDI X+	X(6)→BA, X(5-4)→BU, X(3-0)→BL
	RAR	ACC(I)→ACC(I-1), ACC(0)→CARRY, CARRY→ACC(3)
	XAK	KSR→ACC
	LANG	ACC→AR(3-0), RAM→AR(7-4)
	LNMA	ACC→NR(3-0), RAM→NR(7-4), THEN NR→BIN
	MOD	ACC→MOD(3-0), RAM→MOD(7-4)
	RBIN	BIN(3-0)→ACC; BIN(7-4)→RAM

RAM Instructions

S2000/2150	S2200/2400	
LAM Y*	LAM Y*	RAM→ACC, BU•Y→BU
XC Y*	XC Y*	RAM→ACC, BU•Y→BU
XCI Y*	XCI Y*	ACC→RAM, BL+1→BL, BU•Y→BU SKIP IF BL=0 (AFTER INCREMENT)
XCD Y*	XCD Y*	ACC→RAM, BL-1→BL, BU•Y→BU SKIP IF BL=0 (BEFORE DECREMENT)
STM Z	STM Z	1→RAM BIT Z, 0≤Z≤3
RSM Z	RSM Z	0→RAM BIT Z, 0≤Z≤3
	LMA	ACC→RAM
	STMI Z+	1→RAM BIT Z, 0≤Z≤255, (RAM BANK 1)
	RSMI Z+	0→RAM BIT Z, 0≤Z≤255, (RAM BANK 1)

Input/Output Instructions

S2000/2150	S2200/2400	
INP	IND	D3-D0→ACC, D7-D4→RAM
OUT	OUT	ACC→D3-D0, RAM→D7-D4 (NOT LATCHED)
DISN	DISN	ACC→SEGMENT DECODER→DISPLAY LATCH→D6-D0, CARRY→DISPLAY LATCH→D7
DISB	DISB	ACC→DISPLAY LATCH→D3-D0, RAM→DISPLAY LATCH→D7-D4
MVS	MVS	A-LINE MASTER STROBE LATCH→A LINES
PSH	PSH	PRESET HIGH [BL]→MASTER STROBE LATCH
PSL	PSL	PRESET LOW [BL]→MASTER STROBE LATCH
EUR		(EUROPEAN) SET 50/60Hz AND DISPLAY LATCH POLARITY
	INK	K3-K0→ACC, K7-K4→RAM

+8 bits in the second byte of an instruction.
*Assembled code contains complement of those arguments (the assembler does it automatically).

S2000/S2150 and S2200/S2400 Instruction Set Summary

Program Control Instructions

S2000/2150	S2200/2400	
PP X*	PP X*	IF PREVIOUS INSTRUCTION = PP, X→PPR (0≤X≤15) IF PREVIOUS INSTRUCTION = PP, X→PBR (0≤X≤7)
JMP X	JMP X	JUMP TO LOCATION X, X→LR (0≤X≤15) EXCEPT IF PREVIOUS INSTRUCTION = PP
JMS X	JMS X	JUMP TO SUBROUTINE AT X, LR+1→L STACK, PR→P STACK, X→LR, 15→PR EXCEPT IF PREVIOUS INSTRUCTION = PP
RT	RT	L STACK→LR, P STACK→PR
RTS	RTS	L STACK→LR, P STACK→PR, SKIP INSTR.
NOP	NOP	NO OPERATION
	RTI	RETURN FROM INTERRUPT, RESTORE REGISTERS
	TLU	IF PREVIOUS INSTRUCTION WAS A PP, DO A TABLE LOOK-UP SEQUENCE: PC+1→STACK RAM→PC(3-0), ACC→PC(7-4), PPR(3-2)→PC(9-8) ROM(7-4)→RAM, ROM(3-0)→ACC STACK→PC. IF PREVIOUS INSTRUCTION WAS NOT A PP, DO AN INDEXED SUBROUTINE CALL: PC+1→STACK RAM→PC(3-0), ACC→PC(7-4)

Skip Instructions (Skip 1 Non-PP Instruction) (RAM = Memory at BU,BL)

S2000/2150	S2200/2400	
SZC	SZC	SKIP IF CARRY=0
SZM Z	SZM Z	SKIP IF RAM BIT Z=0, 0≤Z≤3
SZK	SZK	SKIP IF K BIT(S)=0, (BIT(S) IN LAST LAI)
SBE	SBE	SKIP IF BL=E
SAM	SAM	SKIP IF ACC=RAM
SZI		SKIP IF I BIT(S)=0, (BIT(S) IN LAST LAI)
SOS		SKIP IF SF=1, 0→SF. (SF='SECONDS' FLAG OUTPUT OF +50/+60 COUNTER)
TF1		SKIP IF FLAG 1=1
TF2		SKIP IF FLAG 2=1
	SZMI Z+	SKIP IF RAM BIT=0, (IN RAM BANK 1) 0≤Z≤255
	SKFL X+	SKIP IF FLAG=1

Arithmetic and Logical Instructions

S2000/2150	S2200/2400	
ADCS	ADCS	RAM+ACC+CARRY→ACC+C, SKIP IF SUM≤15
ADIS X	ADIS X	X+ACC→ACC, SKIP IF SUM ≤15, CARRY UNALTERED
ADD	ADD	ACC+RAM→ACC, CARRY UNALTERED
AND	AND	ACC & RAM→ACC
XOR	XOR	ACC•RAM→ACC
STC	STC	1→CARRY
RSC	RSC	0→CARRY
CMA	CMA	15-ACC→ACC (LOGICAL 1's COMPLEMENT ACC)
SF1		1→FLAG 1
RF1		0→FLAG 1
SF2		1→FLAG 2
RF2		0→FLAG 2
	SFLG X+	1→FLAG X
	RFLG X+	0→FLAG X

+8 bits in the second byte of an instruction.
*Assembled code contains complement of those arguments (assembler does it for you).

IS114

MC6805 INSTRUCTION SET

Included here is a complete list of instructions available on the MC6805. They are grouped according to register/memory instructions, read/modify/write instructions, branch instructions, bit manipulation instructions, and control instructions.

REGISTER/MEMORY INSTRUCTIONS

Instruction Lists

ADC	Add Memory and Carry to Accumulator
ADD	Add Memory to Accumulator
AND	And Memory to Accumulator
BIT	Bit Test Memory with Accumulator
CMP	Compare Accumulator with Memory
CPX	Compare Index Register with Memory
EOR	Exclusive or Memory with Accumulator
JMP	Jump Absolute
JSR	Jump to Subroutine
LDA	Load Accumulator from Memory
LDX	Load Index Register from Memory
ORA	Or Memory with Accumulator
SBC	Subtract Memory and Borrow from Accumulator
STA	Store Accumulator in Memory
STX	Store Index Register in Memory
SUB	Subtract Memory from Accumulator

READ/MODIFY/WRITE INSTRUCTIONS

ASL	Arithmetic Shift Left (Same as LSL)
ASR	Arithmetic Shift Right
CLR	Clear
COM	Complement
DEC	Decrement
INC	Increment
LSL	Logical Shift Left (Same as ASL)
LSR	Logical Shift Right
NEG	Negate
ROL	Rotate Left thru Carry
ROR	Rotate Right thru Carry
TST	Test for Negative or Zero

BIT MANIPULATION INSTRUCTIONS

BCLR	Bit Clear Bit n in Memory
BRCLR	Branch if Bit n is Clear in Memory
BRSET	Branch if Bit n is Set in Memory
BSET	Bit Set Bit n in Memory

BRANCH INSTRUCTIONS

BRA	Branch Always
BCC	Branch if Carry Clear (Same as BHS)
BCS	Branch if Carry Set (Same as BLO)
BEQ	Branch if Equal
BHCC	Branch if Half Carry Clear
BHCS	Branch if Half Carry Set
BHI	Branch if Higher
BHS	Branch if Higher or Same (Same as BCC)
BIH	Branch if Interrupt Line is HIGH
BIL	Branch if Interrupt Line is Low
BLO	Branch if Lower (Same as BCS)
BLS	Branch if Lower or Same
BMC	Branch if Interrupt Mask is Clear
BMI	Branch if Minus
BMS	Branch if Interrupt Mask is Set
BNE	Branch if Not Equal
BPL	Branch if Plus
BSR	Branch to Subroutine

CONTROL INSTRUCTIONS

CLC	Clear Carry Bit
CLI	Clear Interrupt Mask Bit
NOP	No-Operation
RSP	Reset Stack Pointer
RTI	Return from Interrupt
RTS	Return from Subroutine
SEC	Set Carry Bit
SEI	Set Interrupt Mask Bit
SWI	Software Interrupt
TAX	Transfer Accumulator to Index Register
TXA	Transfer Index Register to Accumulator

TABLE 2 REGISTER MEMORY INSTRUCTIONS

		Addressing Modes																					
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8 Bit Offset)			Indexed (16-Bit Offset)					
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles			
Load A from Memory	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6			
Load X from Memory	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6			
Store A in Memory	STA				B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7			
Store X in Memory	STX				BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7			
Add Memory to A	ADD	AB	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6			
Add Memory and Carry to A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6			
Subtract Memory	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6			
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6			
AND Memory to A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6			
OR Memory with A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6			
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6			
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6			
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6			
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6			
Jump Unconditional	JMP				BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5			
Jump to Subroutine	JSR				BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9			

TABLE 3 READ MODIFY WRITE INSTRUCTIONS

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8 Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
Decrement	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
Clear	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
Complement	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
Negate (2's Complement)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
Rotate Left Thru Carry	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
Rotate Right Thru Carry	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
Logical Shift Left	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
Logical Shift Right	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
Arithmetic Shift Right	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
Test for Negative or Zero	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

TABLE 5 - BIT MANIPULATION INSTRUCTIONS

		Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is set	BRSET n (n = 0 - 7)				2 · n	3	10
Branch IFF Bit n is clear	BRCLR n (n = 0 - 7)				01 + 2 · n	3	10
Set Bit n	BSET n (n = 0 - 7)	10 + 2 · n	2	7			
Clear bit n	BCLR n (n = 0 - 7)	11 + 2 · n	2	7			

TABLE 4 — BRANCH INSTRUCTIONS

		Relative Addressing Mode		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	4
Branch Never	BRN	21	2	4
Branch IFF Higher	BHI	22	2	4
Branch IFF Lower or Same	BLS	23	2	4
Branch IFF Carry Clear	BCC	24	2	4
(Branch IFF Higher or Same)	(BHS)	24	2	4
Branch IFF Carry Set	BCS	25	2	4
(Branch IFF Lower)	(BLO)	25	2	4
Branch IFF Not Equal	BNE	26	2	4
Branch IFF Equal	BEQ	27	2	4
Branch IFF Half Carry Clear	BHCC	28	2	4
Branch IFF Half Carry Set	BHCS	29	2	4
Branch IFF Plus	BPL	2A	2	4
Branch IFF Minus	BMI	2B	2	4
Branch IFF Interupt Mask Bit is Clear	BMC	2C	2	4
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	4
Branch IFF Interrupt Line is Low	BIL	2E	2	4
Branch IFF Interrupt Line is High	BIH	2F	2	4
Branch to Subroutine	BSR	AD	2	8

TABLE 6 — CONTROL INSTRUCTIONS

		Inherent		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	11
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No Operation	NOP	9D	1	2

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS115

Group	Mnemonic code	Function	Status	IS115	IS115a	IS115b
Register to Register	LAB	B → A		×		
	LBA	A → B		×		
	LAY	Y → A				
	LASPX	SPX → A		×		
	LASPY	SPY → A		×		
	XAMR, m	A ↔ MR(m)				
R A M Address	LXA	A → X				
	LYA	A → Y				
	LXI, i	i → X				
	LYI, i	i → Y				
	IY	Y+1 → Y	NZ			
	DY	Y-1 → Y	NB			
	AYY	Y+A → Y	C			
	SYY	Y-A → Y	NB			
	XSPX	X ↔ SPX				
	XSPY	Y ↔ SPY		×		
	XSPXY	X ↔ SPX, Y↔ SPY		×		
Register R A M	LAM(XY)	M → A (XY ↔ SPXY)				
	LBM(XY)	M → B (XY ↔ SPXY)		×		
	XMA(XY)	M ↔ A (XY ↔ SPXY)				
	XMB(XY)	M ↔ B (XY ↔ SPXY)		×		
	LMAIY(X)	A → M, Y+1 → Y (X↔SPX)				
	LMADY(X)	A → M, Y-1 → Y (X↔SPX)				
Immediate	LMIIY, i	i → M, Y+1 → Y	NZ			
	LAI, i	i → A				
	LBI, i	i → B		×		
Arithmetic	AI, i	A+i → A	C			
	IB	B+1 → B	NZ	×		
	DB	B-1 → B	NB	×		
	AMC	M+A+C → A	C			
	SMC	M-A-$\bar{C}$ → A	NB			
	AM	M+A → A	C			
	DAA	Decimal Adjust(Addition)				
	DAS	Decimal Adjust(Subtraction)				
	NEGA	$\bar{A}$+1 → A				
	COMB	$\bar{B}$ → B		×		
	SEC	1 → C (F/F)				
	REC	0 → C (F/F)				
	TC	Test C (F/F)	C(F/F)			
	ROTL	Rotation Left				
	ROTR	Rotation Right				
	OR	A v B → A		×		
Compare	MNEI, i	M ≠ i	NZ			
	YNEI, i	Y ≠ i	NZ			
	ANEM	A ≠ M	NZ			
	BNEM	B ≠ M	NZ	×		
	ALEI, i	A ≦ i	NB			
	ALEM	A ≦ M	NB			
	BLEM	B ≦ M	NB	×		

Cont'd on next page

IS115 Cont'd

IS115 Cont'd

Group	Mnemonic	Function	Status	IS115	IS115a	IS115b
R A M bit Manipulation	SEM, n	1 → M(n)				
	REM, n	0 → M(n)				
	TM, n	Test M(n)	M(n)			
R O M Address	BR, a	Branch on Status 1	1			
	CAL, a	Subroutine Jump on Status 1	1			
	LPU, u	Load Page on Status 1				
	TBR, p	Table Branch				×
	RTN	Return				
Interrupt	SEIE	1 → I/E		×		
	SEIF0	1 → IF0		×		
	SEIF1	1 → IF1		×		
	SETF	1 → TF		×		
	SECF	1 → CF		×		×
	REIE	0 → I/E		×		
	REIF0	0 → IF0		×		
	REIF1	0 → IF1		×		
	RETF	0 → TF		×		
	RECF	0 → CF		×		×
	TI0	Test INT0	INT0	×		
	TI1	Test INT1	INT1	×		
	TIF0	Test IF0	IF0	×		
	TIF1	Test IF1	IF1	×		
	TTF	Test TF	TF	×		×
	LTI, i	i → Timer/Counter		×		
	LTA	A → Timer/Counter		×		×
	LAT	Timer/Counter → A		×		×
	RTNI	Return Interrupt		×		
Input / Output	SED	1 → D (Y)				
	RED	0 → D (Y)				
	TD	Test D(Y)	D(Y)			
	SEDD, n	1 → D (n)				×
	REDD, n	0 → D (n)				×
	LAR, p	R(P) → A				
	LBR, p	R(P) → B				
	LRA, p	A → R(P)				
	LRB, p	B → R(P)				
	P, p	Pattern Generation				×
Input/Output	LRD, p	Display Decoder R(p)		×	×	
Stack	LMSIY, n	$\overline{ST2(n)}$→M, Y+1→Y	NZ	×	×	
	LSMDY, n	$\overline{M}$→ST2(n), Y-1→Y	NB	×	×	
	LASC, n	$\overline{ST2(n)}$ + C→A		×	×	
	NOP	No Operation				

Note)1. (XY) after a mnemonic code has four means as follows.

Mnemonic only	Instruction execution only
Mnemonic X	Instruction execution, X↔SPX
Mnemonic Y	Instruction execution, Y↔SPY
Mnemonic XY	Instruction, X↔SPX, Y↔SPY

2. Status column shows the factor which affects to a status by the instruction of status change.

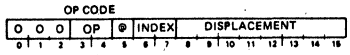
3. Carry flip-flop is not always affected by executing the instruction which affects to a state.
Instructions which affect to carry flip-flop are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

IS117

MEMORY REFERENCE INSTRUCTIONS (MRI)

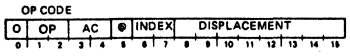
NO ACCUMULATOR



In the No Accumulator—MRI format instructions, bits 0-2 are 000, and bits 3-4 contain the operation code. The effective address "E" is computed from bits 5-15 as shown in Figure 5.

	OP	
JMP	00	Jump to location E (put E in PC).
JSR	01	Load PC + 1 in AC3 and jump to subroutine at location E (put E in PC).
ISZ	10	Increment location E by 1 and skip if result is zero.
DSZ	11	Decrement location E by 1 and skip if result is zero.

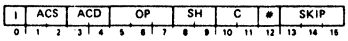
ONE ACCUMULATOR



In the One Accumulator—MRI format instructions, bit 0 is 0, and bits 1-2 contain the operation code. Bits 3-4 specify the accumulator for the operation. The effective address is computed from bits 5-15 as shown in Figure 5.

	OP	
LDA	01	Load contents of location E into AC.
STA	10	Store AC in location E.

ARITHMETIC AND LOGICAL INSTRUCTIONS (ALC)



In the ALC format instructions, bit 0 is 1, bits 1 and 2 specify the source accumulator, bits 3 and 4 specify the destination accumulator, bits 5-7 contain the operation code, bits 8 and 9 specify the action of the shifter, bits 10 and 11 specify the value to which the carry bit will be initialized, bit 12 specifies whether or not the result will be loaded into the destination accumulator, and bits 13-15 specify the skip test. Each instruction in this format utilizes an arithmetic unit whose logical organization is illustrated below.

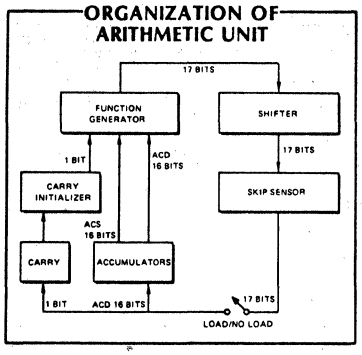


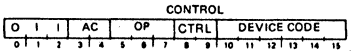
FIGURE 4

Each instruction specifies two accumulators to supply operands to the function generator, which performs the function specified by bits 5-7 of the instruction. The function generator also produces a carry bit whose value depends upon three quantities: an initial value specified by the instruction, the inputs, and the function performed. The initial value can be derived from the previous value of the carry bit, or the instruction can specify an independent value.

The 17-bit output of the function generator, made up of the carry bit and the 16-bit function result, then goes to the shifter, where it can be rotated one place right or left, or the two 8-bit halves of the function result can be swapped without affecting the carry bit. The 17-bit output of the shifter can then be tested for a skip. The skip sensor can test whether the carry bit or the rest of the 17-bit result is or is not equal to zero. After being tested by the skip sensor, the shifter output can be loaded into the carry bit and the destination accumulator. An instruction in this format can perform a complicated arithmetic and shifting operation, and test the result for a skip without affecting the carry bit or either of the operands.

	OP	
COM	000	Place the complement of ACS in ACD
NEG	001	Place negative of ACS in ACD
MOV	010	Move ACS to ACD
INC	011	Place ACS + 1 in ACD
ADC	100	Add the complement of ACS to ACD
SUB	101	Subtract ACS from ACD
ADD	110	Add ACS to ACD
AND	111	And ACS with ACD

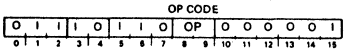
INPUT/OUTPUT INSTRUCTIONS (I/O)



In the Input/Output format instructions, bit 0-2 are 011, bits 3-4 specify the accumulator for the operation, bits 5-7 contain the operation code, bits 8-9 select a control pulse or a test condition and bits 10-15 contain the device code of the referenced device.

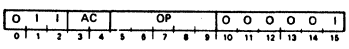
	OP	
NIO	000	No operation.
DOA	010	Data out, AC to A buffer.
DIB	011	Data in, B buffer to AC.
DOB	100	Data out, AC to C buffer.
DIC	101	Data in, C buffer to AC.
DOC	110	Data out, AC to C buffer.
SKP	111	Skip.

MULTIPLY/DIVIDE INSTRUCTIONS (M/D)



	OP	
DIV	01	If AC0-AC2, set carry and abort the operation. Otherwise, clear carry and divide the 32-bit integer located in AC0 (most significant) and AC1 (least significant) by AC2. The 16-bit quotient is placed in AC1 and the 16-bit remainder is placed in AC0.
MUL	11	Multiply the 16-bit integers located in AC1 and AC2 and ADD AC0 to then 32-bit product. The most significant 16 bits of this result are placed in AC0; the least significant in AC1.

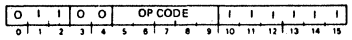
STACK MANIPULATION INSTRUCTION (STK)



Stack support in the microNOVA processor consists of eight instructions.

	OP	
MTFP	00000	Move contents of AC to frame pointer.
MFFP	00010	Move contents of frame pointer to AC.
MTSP	01000	Move contents of AC to stack pointer.
MFSP	01010	Move contents of stack pointer to AC.
PSHA	01100	Increment stack pointer and move contents of AC to top of stack.
POPA	01110	Move top word on stack to AC and decrement stack pointer.
SAV	10100	Push a 5-word return block on STACK.

CENTRAL PROCESSOR CONTROL INSTRUCTIONS (CPU)



I/O instructions with a device code of 77 perform a number of special functions rather than controlling a specific device. In all but the I/O SKIP instruction, I/O instructions with a device code of 77 use bits 8-9 to control the condition of the Interrupt On flag. An I/O SKIP instruction with a device code of 77 uses bits 8-9 to test the state of the Interrupt On flag.

HALT	063077	Halt the processor.
INTA	061477	Acknowledge interrupt by loading code of the highest priority device requesting an interrupt into AC bits 10-15.
INTDS	060277	Disable interrupt by clearing Interrupt On.
INTEN	060177	Enable interrupt by setting Interrupt On.
IORST	061077	Clear all I/O devices (= DOAC 0, CPU).
MSKO	062077	Set up Interupt Disable flags according to mask in AC.
RTCEN	071077	Enable interrupts from CPU real-time clock.
RTCDS	065077	Disable interrupts from CPU real-time clock.

NOTE: Instructions for exercising the upper 64KB memory address space may be found in Integrated Activity Manual (014-74-04)

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WD4200/4210 INSTRUCTION SET

Table 1 is a symbol table providing internal architecture, instruction operand, and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the WD4200/4210 instruction set.

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TABLE 1. WD4200/4210 INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition	Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS		**INSTRUCTION OPERAND SYMBOLS**	
A	4-bit Accumulator	d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
B	6-bit RAM Address Register	r	2-bit Operand Field, 0-3 binary (RAM Register Select)
Br	Upper 2 bits of B (register address)	a	10-bit Operand Field, 0-1023 binary (ROM Address)
Bd	Lower 4 bits of B (digit address)	y	4-bit Operand Field, 0-15 binary (Immediate Data)
C	1-bit Carry Register	RAM(s)	Content and RAM location addressed by s
D	4-bit Data Output Port	ROM(t)	Content and ROM location addressed by t
EN	4-bit Enable Register		
G	4-bit Register to latch data for G I/O Port		
IL	Two 1-bit Latches associated with the IN_3 or IN0 Inputs	**OPERATIONAL SYMBOLS**	
IN	4-bit Input Port	+	Plus
L	8-bit TRI-STATE® I/O Port	-	Minus
M	4-bit contents of RAM Memory Pointed to by B Register	→	Replaces
PC	10-bit ROM Address Register (program counter)	··	Is exchanged with
Q	8-bit Register to latch data for L I/O Port	=	Is equal to
SA	10-bit Subroutine Save Register A	$\overline{A}$	The ones complement of A
SB	10-bit Subroutine Save Register B	●	Exclusive-OR
SC	10-bit Subroutine Save Register C	:	Range of values
SIO	4-bit Shift Register and Counter		
SK	Logic-Controlled Clock Output		

TABLE 2. WD4200/4210 INSTRUCTION SET TABLE (Note 1)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011 0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0011 0001	A + RAM(B) → A	None	Add A to RAM
ADT		4A	0100 1010	A + 10_{10} → A	None	Add Ten to A
AISC	y	5-	0101 y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CASC		10	0001 0000	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0000 0000	0 → A	None	Clear A
COMP		40	0100 0000	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	0100 0100	None	None	No Operation
RC		32	0011 0010	"0" → C	None	Reset C
SC		22	0010 0010	"1" → C	None	Set C
XOR		02	0000 0010	A ● RAM(B) → A	None	Exclusive-OR A with RAM
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111 1111	ROM (PC9,8, A, M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6_	0110 00a9,8 a7:0	a → PC	None	Jump
JP	a	--	1 a6:0 (Pages 2, 3 only) or 11 a5:0 (all other pages)	a → $PC_{6:0}$ a → $PC_{5:0}$	None	Jump within Page (Note 4)
JSRP	a	--	10 a5:0	PC + 1 → SA → SB → SC 0010 → $PC_{9:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6_	0110 10a9,8 a7:0	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
RET		48	0100 1000	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0100 1001	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33 3C	0011 0011 0011 1100	A → $Q_{7:4}$ RAM(B) → $Q_{3:0}$	None	Copy A, RAM to Q
CQMA		33 2C	0110 0111 0010 1100	$Q_{7:4}$ → RAM(B) $Q_{3:0}$ → A	None	Copy Q to RAM, A
LD	r	_5	00r 0101	RAM(B) → A BR® r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r, d	23 --	0010 0011 00r d	RAM(r,d) → A	None	Load A with RAM pointed to directly by r, d
LQID		BF	1011 1111	ROM($PC_{9:8}$, A, M) → Q SB → SC	None	Load Q Indirect (Note 3)
RMB	0	4C	0100 1100	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	0100 0101	0 → $RAM(B)_1$		
	2	42	0100 0010	0 → $RAM(B)_2$		
	3	43	0100 0011	0 → $RAM(B)_3$		
SMB	0	4D	0100 1101	1 → $RAM(B)_0$	None	Set RAM Bit
	1	47	0100 0111	1 → $RAM(B)_1$		
	2	46	0100 0110	1 → $RAM(B)_2$		
	3	4B	0100 1011	1 → $RAM(B)_3$		
STII	y	7_	0111 y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	_6	00r 0110	RAM(B) ·· A	None	Exchange RAM with A, Exclusive OR Br with r
XAD	r, d	23 --	0010 0011 10r d	Br® r → Br	None	Exchange A with RAM pointed to directly by r, d
XDS	r	_7	00r 0111	RAM(B) ·· A Bc - 1 → Bd Br® r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR br with r
XIS	r	_4	00r 0100	RAM(B) ·· A Bd + 1 → Bd Br® r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101 0000	A → Bd	None	Copy A to Bd
CBA		4E	0100 1110	BD ·· A	None	Copy Bd to A
LBI	r, d	--	00r (d (d = 0, 9:15) or 33 0011 0011 -- 10r d (any d)	r,d → B	Skip until not a LBI	Load B Immediate with r, d (Note 6)
LEI	y	33 6_	0011 0011 0110 y	y → EN	None	Load EN Immediate (Note 7)
XABR		12	0001 0010	A ·· Br(0, 0 → A_3, A_2)	None	Exchange A with Br
TEST INSTRUCTIONS						
SKC		20	0010 0000		C = "1"	Skip if C is True
SKE		21	0010 0001		A = (RAM(B)	Skip if A Equals RAM
SKGZ		33	0011 0011		$G_{3:0}$ =0	Skip if G is Zero (all 4 bits)
		21	0010 0001			
SKGBZ		33	0011 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 0001		G_0 = 0	
	1	11	0001 0001	2nd byte	G_1 = 0	
	2	03	0000 0011		G_2 = 0	
	3	13	0001 0011		G_3 = 0	
SKMBZ	0	01	0000 0001		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0001 0001		$RAM(B)_1$ = 0	
	2	03	0000 0011		$RAM(B)_2$ = 0	
	3	13	0001 0011		$RAM(B)_3$ =0	
SKT		41	0100 0001		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0011 0011 0010 1010	G → A	None	Input G ports to A
ININ		33 28	0011 0011 0010 1000	IN → A	None	Input IN inputs to A (Note 2)
INIL		33 29	0011 0011 0010 1001	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Notes 2 and 3)
INL		33 2E	0011 0011 0010 1110	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM, A
OBD		33 3E	0011 0011 0011 1110	Bd → D	None	Output Bd to D Outputs
OGI	y	33 5-	0011 0011 0101 y	y → G	None	Output to G Ports Immediate
OMG		33 3A	0110 0111 0011 1010	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0100 1111	A → SIO, C → SK	None	Exchange A with SIO (Note 3)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g. Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The INI and INIL instructions are not available on the 24-pin WD4210 since this device does not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump while in subroutine pages 2 or 3 to any ROM location within the two-page boundary of page 2 or 3. The JP instruction otherwise permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14 or 15. The machine code for the lower 4 bits equals the binary view of the "d" data *minus 1*: e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal B (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 5 (1111_2).

Note 7: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection of deselection of a particular function associated with each bit (see Functional Description: EN Register).

Pascal MICROENGINE™ Instruction Set Format

Instructions are one byte long, followed by zero to four parameters. Most parameters specify one word of information, and are one of five basic types.

UB Unsigned byte: high order byte of parameter is implicitly zero.

SB Signed byte: high order byte is sign extension of bit 7.

DB Don't care byte: can be treated as SB or UB, as value is always in the range 0...127.

B Big: this parameter is one byte long when used to represent values in the range 0...127, and is two bytes long when representing values in the range 128...32767. If the first byte is in 0...127, the high byte of the parameter is implicitly zero. Otherwise, bit 7 of the first byte is cleared and it is used as the high order byte of the parameter. The second byte is used as the low order byte.

W Word: the next two bytes, low byte first, are the parameter value.

More detailed information on the Pascal MICROENGINE™ instructions (P-Code) is contained in the Pascal Operations Manual.

These mnemonics are intended only for further understanding of P-code. Neither the Microengine Company nor the University of California at San Diego provide P-code assembler software.

Mnemonic	Instruction Code	Parameters	Description
Constant One Word Loads			
SLDC	0...31		Short Load Word Constant (Value 0-31)
LDCN	152		Load Constant Nil
LDCB	128	UB	Load Constant Byte
LDCI	129	W	Load Constant Word
LCA	130	B	Load Constant Address
Local One Word Loads and Store			
SLDL1...16	32...47		Short Load Local Word
LDL	135	B	Load Local Word
LLA	132	B	Load Local Address
STL	164	B	Store Local
Global One Word Loads and Store			
SLDO1...16	48...63		Short Load Global Word
LDO	133	B	Load Global Word
LAO	134	B	Load Global Address
SRO	165	B	Store Global Word
Intermediate One-Word Loads and Store			
LOD	137	DB, B	Load Intermediate Word
LDA	136	DB, B	Load Intermediate Address
STR	166	DB, B	Store Intermediate Word
Indirect One-Word Loads and Store			
STO	196		Store Indirect
Extended One-Word Loads and Store			
LDE	154	UB, B	Load Word Extended
LAE	155	UB, B	Load Address Extended
STE	217	UB, B	Store Word Extended
Multiple Word Loads and Stores (Sets and Reals)			
LDC	131	B, UB	Load Multiple Word Constant
LDM	208	UB	Load Multiple Words
STM	142	UB	Store Multiple Words
Byte Arrays			
LDB	167		Load Byte
STB	200		Store Byte

Mnemonic	Instruction Code	Parameters	Description
Record and Array Indexing and Assignment			
MOV	197	B	Move Words
SIND0...7	120...127		Short Index and Load Word
IND	230	B	Static Index and Load Word
INC	231	B	Increment Field Pointer
IXA	215	B	Index Array
IXP	216	UB_1, UB_2	Index Packed Array
LDP	201		Load A Packed field
STP	202		Store Into A Packed Field
Logicals			
LAND	161		Logical And
LOR	160		Logical Or
LNOT	229		Logical Not
LEUSW	180		Compare Unsigned Word <
GEUSW	181		Compare Unsigned Word > =
Integers			
ABI	224		Absolute Value of Integer
NGI	225		Negate Integer
ADI	162		Add Integers
SBI	163		Subtract Integers
MPI	140		Multiply Integers
DUP1	226		Copy Integer
DVI	141		Divide Integers
MODI	143		Modulo Integers
CHK	203		Check Against Subrange Bounds
EQUI	176		Compare Integer =
NEQI	177		Compare Integer < >
LEQI	178		Compare Integer < =
GEQI	179		Compare Integer > =
Reals (All Over/Underflows Cause a Run-Time Error)			
FLT	204		Float Top-of-Stack
TNC	190		Truncate Real
RND	191		Round Real
ABR	227		Absolute Value of Real
ADR	192		Add Reals
NGR	228		Negate Real
SBR	193		Subtract Reals
MPR	194		Multiply Reals
DUP2	198		Copy Real
DVR	195		Divide Reals
EQUREAL	205		Compare Real =
LEQREAL	206		Compare Real < =
GEQREAL	207		Compare Real > =
Sets			
ADJ	199	UB	Adjust Set
SRS	188		Build Subrange Set
INN	218		Set Membership
UNI	219		Set Union
INT	220		Set Intersection
DIF	221		Set Difference
EQUPWR	182		Set Compare
LEQPWR	183		Set Compare < (Subset of)
GEQPWR	184		Set Compare > (Superset of)

Mnemonic	Instruction Code	Parameters	Description
Byte Arrays			
EQUBYT	185	B	Byte Array Compare
LEQBYT	186	B	Byte Array Compare <
GEQBYT	187	B	Byte Array Compare >
Jumps			
UJP	138	SB	Unconditional Jump
FJP	212	SB	False Jump
EFJ	210	SB	Equal False Jump
NFJ	211	SB	Not Equal False Jump
UJPL	139	W	Unconditional Long Jump
FJPL	213	W	False Long Jump
XJP	214	B	Case Jump
Procedure and Function Calls and Returns			
CPL	144	UB	Call Local Procedure
CPG	145	UB	Call Global Procedure
CPI	146	DB, UB	Call Intermediate Procedure
CXL	147	UB_1, UB_2	Call Local External Procedure
CXG	148	UB_1, UB_2	Call Global External Procedure
CXI	149	UB_1, DB, UB_2	Call Intermediate External Procedure
CPF	151		Call Formal Procedure
RPU	150	B	Return From User Procedure
LSL	153	DB	Load Static Link Onto Stack
NOP	156		No Operation
SIGNAL	222		Signal
WAIT	223		Wait on Semaphore
LPR	157		Load Processor Register
SPR	209		Store Processor Register
BPT	158		Break Point
RBP	159		Return From Breakpoint
SWAP	189		Swap Top-of-Stack with Next to Top-of-Stack

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	
ACCUMULATOR																	
ADD A, = data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•				
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•				
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•				
ADDC A, = data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•				
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•				
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•				
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2					
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1					IS120,a,b
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1					
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1					
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1					
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•				
DEC A	(A) ← (A) – 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1					
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1					
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2					
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1					
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1					
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1					
RLC A	(AN + 1) ← (AN); N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•				
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1					
RRC A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•				
SWAP A	(A_{4-7}) ← (A_{0-3})	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1					
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2					
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1					
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1					
BRANCH																	
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2					
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2					
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					IS120 ONLY
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2					
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1					
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JNI addr	(PC 0 – 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					

MNEMONIC	FUNCTION	DESCRIPTION									CYCLES	BYTES	
BRANCH													
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2	
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2	
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	IS120a ONLY
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1	
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JNIBF addr	(PC 0 – 7) ← addr if IBF = (PC) ← (PC) + 2 if IBF = 1	Jump to specified address if input buffer full flag is low.	1 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JOBF	(PC 0 – 7) ← addr if OBF = 1 (PC) ← (PC) + 2 if OBF = 0	Jump to specified address if output buffer full flag is set.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	
BRANCH (CONT.)																	
JNT0 addr	(PC 0 - 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					IS120,a
JNT1 addr	(PC 0 - 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JNZ addr	(PC 0 - 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JTF addr	(PC 0 - 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JT0 addr	(PC 0 - 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
BRANCH																	
DJNZ Rr, addr	(Rr) ← (Rr) - 1; r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2					
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JMP addr	(PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2					
JMPP @ A	(PC 0 - 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1					
JNC addr	(PC 0 - 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					IS120b ONLY
JNT1 addr	(PC 0 - 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JNZ addr	(PC 0 - 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JTF addr	(PC 0 - 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2					
CONTROL																	
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1					
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1					
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1					
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 - 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1					IS120 ONLY
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 - 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1					
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 - 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1					
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 - 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1					
CONTROL																	
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1					
DIS I		Disable the External Interrupt input	0	0	0	1	0	1	0	1	1	1					
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 - 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1					IS120a ONLY
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 - 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1					
DATA MOVES																	
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2					
MOV A, Rr	(A) ← (Rr); r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1					
MOV A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1					
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1					
MOV Rr, # data	(Rr) ← data; r = 0 - 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2					
MOV Rr, A	(Rr) ← (A); r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1					
MOV @ Rr, A	((Rr)) ← (A); r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1					
MOV @ Rr, # data	((Rr)) ← data; r = 0 - 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2					IS120 ONLY
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1					
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1					
MOVP3 A, @ A	(PC 0 - 7) ← (A) (PC 8 - 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1					
MOVX A, @ R	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1					
MOVX @ R, A	((Rr)) ← (A); r = 0 - 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1					
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1					
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1					
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1					

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1	
DATA MOVES																	
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0	0	1	0	0	0	1	1	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
MOV A, Rr	(A) ← (Rr); r = 0 7	Move the contents of the designated registers into the Accumulator	1	1	1	1	1	r	r	r	1	1					
MOV A, @ Rr	(A) ← ((Rr)); r = 0 1	Move Indirect the contents of data memory location into the Accumulator	1	1	1	1	0	0	0	r	1	1					
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1					
MOV Rr, # data	(Rr) ← data; r = 0 7	Move Immediate the specified data into the designated register.	1	0	1	1	1	r	r	r	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
MOV Rr, A	(Rr) ← (A); r = 0 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1					
MOV @ Rr, A	((Rr)) ← (A); r = 0 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1					IS120a ONLY
MOV @ Rr, # data	((Rr)) ← data, r = 0 1	Move Immediate the specified data into data memory.	1	0	1	1	0	0	0	r	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1					
MOVP A, @ A	(PC 0 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1					
MOVP3 A, @ A	(PC 0 7) ← (A) (PC 8 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1					
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1					
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1					
XCHD A, @ Rr	(A 0 - 3) ⇆ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1					
DATA MOVES																	
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator	0	0	1	0	0	0	1	1	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
MOV A, Rr	(A) ← (Rr), r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1					
MOV A, @ Rr	(A) ← ((Rr)), r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator	1	1	1	1	0	0	0	r	1	1					
MOV Rr, # data	(Rr) ← data, r = 0 - 7	Move Immediate the specified data into the designated register.	1	0	1	1	1	r	r	r	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
MOV Rr, A	(Rr) ← (A), r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1					IS120b ONLY
MOV @ Rr, A	((Rr)) ← (A); r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1					
MOV @ Rr, # data	((Rr)) ← data, r = 0 - 1	Move Immediate the specified data into data memory.	1	0	1	1	0	0	0	r	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1					
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents	0	0	1	0	1	r	r	r	1	1					
XCH A, @ Rr	(A) ⇄ ((Rr)), r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1					
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)), r = 0 - 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1					
INPUT/OUTPUT																	
ANL BUS, data	(BUS) ← (BUS) AND data	Logical and Immediate specified data with contents of BUS	1	0	0	1	1	0	0	0	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
ANL Pp, data	(Pp) ← (Pp) AND data p = 1 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 3) p = 4 7	Logical and contents of Accumulator with designated port (4 7)	1	0	0	1	1	1	p	p	2	1					
IN A, Pp	(A) ← (Pp) p = 1 2	Input data from designated port (1 2) into Accumulator	0	0	0	0	1	0	p	p	2	1					
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator	0	0	0	0	1	0	0	0	2	1					
MOVD A, Pp	(A 0 3) ← (Pp), p = 4 7 (A 4 7) ← 0	Move contents of designated port (4 7) into Accumulator	0	0	0	0	1	1	p	p	2	1					IS120 ONLY
MOVD Pp, A	(Pp) ← A 0 3, p = 4 7	Move contents of Accumulator to designated port (4 7)	0	0	1	1	1	1	p	p	1	1					
ORL BUS, data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS	1	0	0	0	1	0	0	0	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 3) p = 4 7	Logical or contents of Accumulator with designated port (4 7)	1	0	0	0	1	1	p	p	1	1					
ORL Pp, data	(Pp) ← (Pp) OR data p = 1 2	Logical or Immediate specified data with designated port (1 2)	1	0	0	0	1	0	p	p	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS	0	0	0	0	0	0	1	0	1	1					
OUTL Pp, A	(Pp) ← (A) p = 1 2	Output contents of Accumulator to designated port (1 2)	0	0	1	1	1	0	p	p	1	1					
INPUT/OUTPUT																	
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 3) p = 4 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1					
IN A, Pp	(A) ← (Pp), p = 1 2	Input data from designated port (1 2) into Accumulator	0	0	0	0	1	0	p	p	2	1					
IN A, DBB	(A) ← (DBB)	Input strobed DBB data into Accumulator and clear IBF.	0	0	1	0	0	0	1	0	1	1					
MOVD A, Pp	(A 0 - 3) ← (Pp), p = 4 7 (A 4 7) ← 0	Move contents of designated port (4 7) into Accumulator	0	0	0	0	1	1	p	p	2	1					IS120a ONLY
MOVD Pp, A	(Pp) ← A 0 3, p = 4 7	Move contents of Accumulator to designated port (4 7)	0	0	1	1	1	1	p	p	1	1					
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 3) p = 4 7	Logical or contents of Accumulator with designated port (4 7)	1	0	0	0	1	1	p	p	1	1					
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 2	Logical or Immediate specified data with designated port (1 2)	1	0	0	0	1	0	p	p	2	2					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0							
OUT DBB, A	(DBB) (A)	Output contents of Accumulator onto DBB and set OBF.	0	0	0	0	0	0	1	0	1	1					
OUTL Pp, A	(Pp) ← (A), p = 1 2	Output contents of Accumulator to designated port (1 2)	0	0	1	1	1	0	p	p	1	1					

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MNEMONIC	FUNCTION	DESCRIPTION	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAG C
INPUT/OUTPUT													
ANLD Pp, A	$(P_p) \leftarrow (P_p)$ AND (A 0 - 3) p = 4 - 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1	
IN A, P_p	(A) ← (P_p); p = 1 - 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1	
MOVD A, P_p	(A 0 - 3) ← (P_p); p = 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1	
MOVD P_p, A	(P_p) ← A 0 - 3; p = 4 - 7	Move contents of Accumulator to designated port (4 - 7).	0	0	1	1	1	1	p	p	1	1	
ORLD P_p, A	$(P_p) \leftarrow (P_p)$ OR (A 0 - 3) p = 4 - 7	Logical or contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1	
OUTL P_p, A	(P_p) ← (A); p = 1 - 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1	
FLAGS													
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1	•
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1.	1	0	1	1	0	1	0	1	1	1	•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1	•
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1	•
FLAGS													
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•
REGISTERS													
DEC Rr	(Rr) ← (Rr) - 1, r = 0 - 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1	
INC Rr	(Rr) ← (Rr) + 1, r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1	
INC @ Rr	((Rr)) ← ((Rr)) + 1, r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1	
SUBROUTINE													
CALL addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Call designated Subroutine.	a10	a9	a8	1	0	1	0	0 a0	2	2	
RET	(SP) ← (SP) - 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1	
RETR	(SP) ← (SP) - 1 (PC) ← ((SP)) (PSW 4 - 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1	
TIMER/COUNTER													
EN TCNTI		Enable Internal Interrupt Flag for Timer Counter output.	0	0	1	0	0	1	0	1	1	1	
DIS TCNTI		Disable Internal Interrupt Flag for Timer Counter output.	0	0	1	1	0	1	0	1	1	1	
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1	
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1	
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1	
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1	
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1	
MISCELLANEOUS													
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1	

IS120b ONLY

IS120,a

IS120b ONLY

IS120,a

IS120b
ONLY

REGISTERS													
INC Rr	(Rr) ← (Rr) + 1, r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1	
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1	
SUBROUTINE													
CALL addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Call designated Subroutine.	a10	a9	a8	1	0	1	0	0 a0	2	2	
RET	(SP) ← (SP) - 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1	
TIMER/COUNTER													
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1	
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1	
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1	
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1	
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1	
MISCELLANEOUS													
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1	

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
IBF	Input Buffer Full Flag

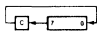
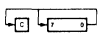
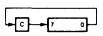
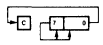
SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By
OBF	Output Buffer Full
DBB	Data Bus Buffer

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

IS121

Instruction Summary

Instruction and Operation	Addr Mode dst	Addr Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst,src dst ← dst + src + C	(Note 1)		1□	* * * * 0 *
ADD dst,src dst ← dst + src	(Note 1)		0□	* * * * 0 *
AND dst,src dst ← dst AND src	(Note 1)		5□	- * * 0 - -
CALL dst SP ← SP - 2 @SP ← PC; PC ← dst	DA IRR		D6 D4	- - - - - -
CCF C ← NOT C			EF	* - - - - -
CLR dst dst ← 0	R IR		B0 B1	- - - - - -
COM dst dst ← NOT dst	R IR		60 61	- * * 0 - -
CP dst,src dst - src	(Note 1)		A□	* * * * - -
DA dst dst ← DA dst	R IR		40 41	* * * X - -
DEC dst dst ← dst - 1	R IR		00 01	- * * * - -
DECW dst dst ← dst - 1	RR IR		80 81	- * * * - -
DI IMR (7) ← 0			8F	- - - - - -
DJNZ r,dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range: +127, -128	RA		rA r=0-F	- - - - - -
EI IMR (7) ← 1			9F	- - - - - -
INC dst dst ← dst + 1	r R IR		rE r=0-F 20 21	- * * * - -
INCW dst dst ← dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR (7) ← 1			BF	* * * * * *
JP cc,dst if cc is true PC ← dst	DA IRR		cD c=0-F 30	- - - - - -
JR cc,dst if cc is true, PC ← PC + dst Range: +127, -128	RA		cB c=0-F	- - - - - -
LD dst,src dst ← src	r r R r X r Ir R R IR IR	IM R r X r Ir r R IR IM IM R	rC r8 r9 r=0-F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst,src dst ← src	r Irr	Irr r	C2 D2	- - - - - -
LDCI dst,src dst ← src r ← r + 1; rr ← rr + 1	Ir Irr	Irr Ir	C3 D3	- - - - - -
LDE dst,src dst ← src	r Irr	Irr r	82 92	- - - - - -

Instruction and Operation	Addr Mode dst	Addr Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
LDEI dst,src dst ← src r ← r + 1; rr ← rr + 1	Ir Irr	Irr Ir	83 93	- - - - - -
NOP			FF	- - - - - -
OR dst,src dst ← dst OR src	(Note 1)		4□	- * * 0 - -
POP dst dst ← @SP SP ← SP + 1	R IR		50 51	- - - - - -
PUSH src SP ← SP - 1; @SP ← src		R IR	70 71	- - - - - -
RCF C ← 0			CF	0 - - - - -
RET PC ← @SP; SP ← SP + 2			AF	- - - - - -
RL dst 	R IR		90 91	* * * * - -
RLC dst 	R IR		10 11	* * * * - -
RR dst 	R IR		E0 E1	* * * * - -
RRC dst 	R IR		C0 C1	* * * * - -
SBC dst,src dst ← dst - src - C	(Note 1)		3□	* * * * 1 *
SCF C ← 1			DF	1 - - - - -
SRA dst 	R IR		D0 D1	* * * 0 - -
SRP src RP ← src		IM	31	- - - - - -
SUB dst,src dst ← dst - src	(Note 1)		2□	* * * * 1 *
SWAP dst 	R IR		F0 F1	X * * X - -
TCM dst,src (NOT dst) AND src	(Note 1)		6□	- * * 0 - -
TM dst,src	(Note 1)		7□	- * * 0 - -
XOR dst,src dst ← dst XOR src	(Note 1)		B□	- * * 0 - -

Z8 Instruction Set

Note 1

These instructions have an identical set of addressing modes, which are encoded for brevity in this table. The higher opcode nibble is found in the instruction set table above. The lower nibble is expressed symbolically by a □ in the table above, and its value is found in the following table to the right of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Addr Mode dst	Addr Mode src	Lower Opcode Nibble
r	r	2
r	Ir	3
R	R	4
R	IR	5
R	IM	6
IR	IM	7

IS122

	0	1	2	3	4	5	6	7
00	NOP NOP 000-00 4A	LD BC,nn LXI B,nn 001-01 10D	LD (BC),A LDAX B 002-02 7A	INC BC INX B 003-03 6A	INC B INR B 004-04 4A--SZV	DEC B DCR B 005-05 4A--SZV	LD B,n MVI B,n 006-06 7B	RLCA RLC 007-07 4A--C
01	EX AF,AF — 010-08 4A--SZVC	**ADD *,BC** **DAD B** **011-09** **11A/15E--C**	LD A,(BC) STAX B 012-0A 7A	DEC BC DCX B 013-0B 6A	INC C INR C 014-0C 4A--SZV	DEC C DCR C 015-0D 4A--SZV	LD C,n MVI C,n 016-0E 7B	RRCA RRC 017-0F 4A--C
02	DJNZ,e — 020-10 8C/13C	LD DE,nn LXI D,nn 021-11 10D	LD (DE),A LDAX D 022-12 7A	INC DE INX D 023-13 6A	INC D INR D 024-14 4A--SZV	DEC D DCR D 025-15 4A--SZV	LD D,n MVI D,n 026-16 7B	RLA RAL 027-17 4A--C
03	JR e — 030-18 12C	**ADD *,DE** **DAD D** **031-19** **11A/15E--C**	LD A,(DE) STAX D 032-1A 7A	DEC DE DCX D 033-1B 6A	INC E INR E 034-1C 4A--SZV	DEC E DCR E 035-1D 4A--SZV	LD E,n MVI E,n 036-1E 7B	RRA RAR 037-1F 4A--C
04	JP NZ,e — 040-20 7C/12C	**LD *,nn** **LXI H,nn** **041-21** **10D/14J**	**LD (nn),*** **SHLD** **042-22** **16A/20J**	**INC *** **INX H** **043-23** **6A/10E**	INC H INR H 044-24 4A--SZV	DEC H DCR H 045-25 4A--SZV	LD H,n MVI H,n 046-26 7B	DAA DAA 047-27 4A--SZPC
05	JR Z,e — 050-28 7C/12C	**ADD *,HL** **DAD H** **051-29** **11A/15E--C**	**LD *,(nn)** **LHLD** **052-2A** **16A/20J**	**DEC *** **DCX H** **053-2B** **6A/10E**	INC L INR L 054-2C 4A--SZV	DEC L DCR L 055-2D 4A--SZV	LD L,n MVI L,n 056-2E 7B	CPL CMA 057-2F 4A
06	JR NC,e — 060-30 7C/12C	LD SP,nn LXI SP,nn 061-31 10D	LD (nn),A STA 062-32 13D	INC SP INX SP 063-33 6A	**INC (*)** **INR M** **084-34** **11A/23G--SZV**	**DEC (*)** **DCR M** **065-35** **11A/23G--SZV**	**LD (*),n** **MVI M,n** **066-36** **10B/19H**	SCF STC 067-37 4A--C
07	JR C,e — 070-38 7C/12C	**ADD *,SP** **DAD SP** **071-39** **11A/15A--C**	LD A,(nn) LDA 072-3A 13D	DEC SP DCX SP 073-3B 6A	INC A INR A 074-3C 4A--SZV	DEC A DCR A 075-3D 4A--SZV	LD A,n MVI A,n 076-3E 7B	CCF CMC 077-3F 4A--C

10	LD B,B
	MOV B,B
	100-40
	4A
		LD B,C
		MOV B,C
		101-41
		4A
			LD B,D
			MOV B,D
			102-42
			4A
				LD B,E
				MOV B,E
				103-43
				4A
					LD B,H
					MOV B,H
					104-44
					4A
						LD B,L
						MOV B,L
						105-45
						4A
							LD B,(*)
							MOV B,M
							106-46
							7A/19G
								LD B,A
								MOV B,A
								107-47
								4A

11	LD C,B
	MOV C,B
	110-48
	4A
		LD C,C
		MOV C,C
		111-49
		4A
			LD C,D
			MOV C,D
			112-4A
			4A
				LD C,E
				MOV C,E
				113-4B
				4A
					LD C,H
					MOV C,H
					114-4C
					4A
						LD C,L
						MOV C,L
						115-4D
						4A
							LD C,(*)
							MOV C,M
							116-4E
							7A/19G
								LD C,A
								MOV C,A
								117-4F
								4A

12	LD D,B
	MOV D,B
	120-50
	4A
		LD D,C
		MOV D,C
		121-51
		4A
			LD D,D
			MOV D,D
			122-52
			4A
				LD D,E
				MOV D,E
				123-53
				4A
					LD D,H
					MOV D,H
					124-54
					4A
						LD D,L
						MOV D,L
						125-55
						4A
							LD D,(*)
							MOV D,M
							126-56
							7A/19G
								LD D,A
								MOV D,A
								127-57
								4A

13	LD E,B
	MOV E,B
	130-58
	4A
		LD E,C
		MOV E,C
		131-59
		4A
			LD E,D
			MOV E,D
			132-5A
			4A
				LD E,E
				MOV E,E
				133-5B
				4A
					LD E,H
					MOV E,H
					134-5C
					4A
						LD E,L
						MOV E,L
						135-5D
						4A
							LD E,(*)
							MOV E,M
							136-5E
							7A/19G
								LD E,A
								MOV E,A
								137-5F
								4A

14	LD H,B
	MOV H,B
	140-60
	4A
		LD H,C
		MOV H,C
		140-61
		4A
			LD H,D
			MOV H,D
			142-62
			4A
				LD H,E
				MOV H,E
				143-63
				4A
					LD H,H
					MOV H,H
					144-64
					4A
						LD H,L
						MOV H,L
						145-65
						4A
							LD H,(*)
							MOV H,M
							146-66
							7A/19G
								LD H,A
								MOV H,A
								147-67
								4A

15	LD L,B
	MOV L,B
	150-68
	4A
		LD L,C
		MOV L,C
		151-69
		4A
			LD L,D
			MOV L,D
			152-6A
			4A
				LD L,E
				MOV L,E
				153-6B
				4A
					LD L,H
					MOV L,H
					154-6C
					4A
						LD L,L
						MOV L,L
						155-6D
						4A
							LD L,(*)
							MOV L,M
							156-6E
							7A/19G
								LD L,A
								MOV L,A
								157-6F
								4A

16	**LD (*),B** **MOV M,B** **160-70** **7A/19G**	**LD (*),C** **MOV M,C** **161-71** **7A/19G**	**LD (*),D** **MOV M,D** **162-72** **7A/19G**	**LD (*),E** **MOV M,E** **163-73** **7A/19G**	**LD (*),H** **MOV M,H** **164-74** **7A/19G**	**LD (*),L** **MOV M,L** **165-75** **7A/19G**	HALT HALT 166-76	**LD (*),A** **MOV M,A** **167-77** **7A/19G**

17	LD A,B
	MOV A,B
	170-78
	4A
		LD A,C
		MOV A,C
		171-79
		4A
			LD A,D
			MOV A,D
			172-7A
			4A
				LD A,E
				MOV A,E
				173-7B
				4A
					LD A,H
					MOV A,H
					174-7C
					4A
						LD A,L
						MOV A,L
						175-7D
						4A
							LD A,(*)
							MOV A,M
							176-7E
							7A/19G
								LD A,A
								MOV A,A
								177-7F
								4A

	0	1	2	3	4	5	6	7
20	ADD B ADD B 200-80 4A--SZVC	ADD C ADD C 201-81 4A--SZVC	ADD D ADD D 202-82 4A--SZVC	ADD E ADD E 203-83 4A--SZVC	ADD H ADD H 204-84 4A--SZVC	ADD L ADD L 205-85 4A--SZVC	**ADD (*)** **ADD M** **206-86** **7A/19G--SZVC**	ADD A ADD A 207-87 4A--SZVC
21	ADC B ADC B 210-88 4A--SZVC	ADC C ADC C 211-89 4A--SZVC	ADC D ADC D 212-8A 4A--SZVC	ADC E ADC E 213-8B 4A--SZVC	ADC H ADC H 214-8C 4A--SZVC	ADC L ADC L 215-8D 4A--SZVC	**ADC (*)** **ADC M** **216-8E** **7A/19G--SZVC**	ADC A ADC A 217-8F 4A--SZVC
22	SUB B SUB B 220-90 4A--SZVC	SUB C SUB C 221-91 4A--SZVC	SUB D SUB D 222-92 4A--SZVC	SUB E SUB E 223-93 4A--SZVC	SUB H SUB H 224-94 4A--SZVC	SUB L SUB L 225-95 4A--SZVC	**SUB (*)** **SUB M** **226-96** **7A/19G--SZVC**	SUB A SUB A 227-97 4A--SZVC
23	SBC B SBB B 230-98 4A--SZVC	SBC C SBB C 231-99 4A--SZVC	SBC D SBB D 232-9A 4A--SZVC	SBC E SBB E 233-9B 4A--SZVC	SBC H SBB H 234-9C 4A--SZVC	SBC L SBB L 235-9D 4A--SZVC	**SBC (*)** **SBB M** **236-9E** **7A/19G--SZVC**	SBC A SBB A 237-9F 4A--SZVC
24	AND B ANA B 240-A0 4A--SZPC	AND C ANA C 241-A1 4A--SZPC	AND D ANA D 242-A2 4A--SZPC	AND E ANA E 243-A3 4A--SZPC	AND H ANA H 244-A4 4A--SZPC	AND L ANA L 245-A5 4A--SZPC	**AND (*)** **ANA M** **246-A6** **7A/19G--SZPC**	AND A ANA A 247-A7 4A--SZPC
25	XOR B XRA B 250-A8 4A--SZPC	XOR C XRA C 251-A9 4A--SZPC	XOR D XRA D 252-AA 4A--SZPC	XOR E XRA E 253-AB 4A--SZPC	XOR H XRA H 254-AC 4A--SZPC	XOR L XRA L 255-AD 4A--SZPC	**XOR (*)** **XRA M** **256-AE** **7A/19G--SZPC**	XOR A XRA A 257-AF 4A--SZPC
26	OR B ORA B 260-B0 4A--SZPC	OR C ORA C 261-B1 4A--SZPC	OR D ORA D 262-B2 4A--SZPC	OR E ORA E 263-B3 4A--SZPC	OR H ORA H 264-B4 4A--SZPC	OR L ORA L 265-B5 4A--SZPC	**OR (*)** **ORA M** **266-B6** **7A/19G--SZPC**	OR A ORA A 267-B7 4A--SZPC
27	CP B CMLP B 270-B8 4A--SZVC	CP C CMP C 271-B9 4A--SZVC	CP D CMP D 272-BA 4A--SZVC	CP E CMP E 273-BB 4A--SZVC	CP H CMP H 274-BC 4A--SZVC	CP L CMP L 275-BD 4A--SZVC	**CP (*)** **CMP M** **276-BE** **7A/19G--SZVC**	CP A CMP A 277-BF 4A--SZVC
30	RET NZ RNZ 300-C0 5A/11A	POP BC POP B 301-C1 10A	JP NZ,nn JNZ 302-C2 10D	JP nn JMP 303-C3 10D	CALL NZ,nn CNZ 304-C4 10D/17D	PUSH BC PUSH B 305-C5 11A	ADD n ADI 306-C6 7B--SZVC	**RST 0** **RST 0** 307-C7 11A
31	**RET Z** **RZ** 310-C8 5A/11A	RET RET 311-C9 10A	JP Z,nn JZ 312-CA 10D	(SPECIAL) (PREFIX) 313-CB	CALL Z,nn CZ 314-CC 10D/17D	CALL nn CALL 315-CD 17D	ADC n ACI 316-CE 7B--SZVC	RST 1 RST 1 317-CF 11A
32	RET NC RNC 320-D0 5A/11A	POP DE POP D 321-D1 10A	JP NC,nn JNC 322-D2 10D	OUT (n),A OUT 323-D3 11B	CALL NC,nn CNC 324-D4 10D/17D	PUSH DE PUSH D 325-D5 11A	SUB n SUI 326-D6 7B--SZVC	RST 2 RST 2 327-D7 11A
33	RET C RC 330-D8 5A/11A	EXX — 331-D9 4A	JP C,nn JC 332-DA 10D	IN A,(n) IN 333-DB 10B	CALL C,nn CC 334-DC 10D/17D	****IX**** (PREFIX) 335-DD	SBC n SBI 336-DE 7B--SZVC	RST 3 RST 3 337-DF 11A
34	RET PO RPO 340-E0 5A/11A	**POP *** **POP H** **341-E1** **10A/14E**	JP PO,nn JPO 342-E2 10D	**EX (SP),*** **XTHL** **343-E3** **19A/23E**	CALL PO,nn CPO 344-E4 10D/17D	**PUSH *** **PUSH H** **345-E5** **11A/15E**	AND n ANI 346-E6 7B--SZPC	RST 4 RST 4 347-E7 11A
35	RET PE RPE 350-E8 5A/11A	**JP (*)** **PCHL** **351-E9** **4A/8E**	JP PE,nn JPE 352-EA 10D	EX DE,HL XCHG 353-EB 4A	CALL PE,nn CPE 354-EC 10D/17D	******** (PREFIX) 355-ED	XOR n XRI 356-EE 7B--SZPC	RST 5 RST 5 357-EF 11A
36	RET P RP 360-F0 5A/11A	POP AF POP PSW 361-F1 10A--SZVC	JP P,nn JP 362-F2 10D	DI — 363-F3 4A	CALL P,nn CP 364-F4 10D/17D	PUSH AF PUSH PSW 365-F5 11A	OR n ORI 366-F6 7B--SZPC	RST 6 RST 6 367-F7 11A
37	RET M RM 370-F8 5A/11A	**LD SP,*** **SPHL** **371-F9** **6A/10E**	JP M,nn JM 372-FA 10D	EI — 373-FB 4A	CALL M,nn CM 374-FC 10D/17D	****IY**** (PREFIX) 375-FD	CP n CPI 376-FE 7B--SZVC	RST 7 RST 7 377-FF 11A

A OPCODE
B OPCODE Operand
C OPCODE Displacement
D OPCODE Operand L Operand H
E OPCODE1 OPCODE
F OPCODE1 OPCODE Operand
G OPCODE1 OPCODE Displacement
H OPCODE1 OPCODE Displacement Operand
J OPCODE1 OPCODE Operand L Operand H

OPCODE1 = 335-DD For IX Operand
= 375-ED For IY Operand

* MEANS HL, IX, or IY
(*) MEANS (HL), (IX + d), or (IY + d)

	0	1	2	3	4	5	6	7
10	IN B,(C) 100-40 11K--SZP	OUT (C),B 101-41 12K	SBC HL,BC 102-42 15K--SZVC	LD (NN),BC 103-43 20L	NEG 104-44 8K--CZVS	RETN 105-45 14K	IM 0 106-46 8K	LD I,A 107-47 9K
11	IN C,(C) 110-48 11K--SZP	OUT (C),C 111-49 12K	ADC HL,BC 112-4A 15K--SZVC	LD BC,(nn) 113-4B 20L		RETI 115-4D 14K		LD R,A 117-4F 9K
12	IN D,(C) 120-50 11K--SZP	OUT (C),D 121-51 12K	SBC HL,DE 122-52 15K--SZVC	LD (nn),DE 123-53 20L			IM 1 126-56 8K	LD A,I 127-57 9K--SZV
13	IN E,(C) 130-58 11K--SZP	OUT (C),E 131-59 12K	ADC HL,DE 132-5A 15K--SZVC	LD DE,(nn) 133-5B 20L			IM 2 136-5E 8K	LD A,R 137-5F 9K--SZV
14	IN H,(C) 140-60 11K--SZP	OUT (C),H 141-61 12K	SBC HL,HL 142-62 15K--SZVC	LD (nn),HL 143-63 20L				RRD 147-67 18K--SZP
15	IN L,(C) 150-68 11K--SZP	OUT (C),L 151-69 12K	ADC HL,HL 152-6A 15K--SZVC	LD HL,(nn) 153-6B 20L				RLD 157-6F 18K--SZP
16	IN F,(C) 160-70 11K--SZP	OUT (C),F 161-71 12K	SBC HL,SP 162-72 15K--SZVC	LD (nn),SP 163-73 20L				
17	IN A,(C) 170-78 11K--SZP	OUT (C),A 171-79 12K	ADC HL,SP 172-7A 15K--SZVC	LD SP,(nn) 173-7B 20L				
24	LDI 240-A0 16K--P(SZ)	CPI 241-A1 16K--SZP	INI 242-A2 15K--Z(SP)	OUTI 243-A3 15K--Z(SP)				
25	LDD 250-A8 16K--P(SZ)	CPD 251-A9 16K--SZP	IND 252-AA 15K--Z(SP)	OUTD 253-AB 15K--Z(SP)				
26	LDIR 260-B0 21M/16K--P(SZ)	CPIR 261-B1 21M/16K--SZP	INIR 262-B2 20M/15K--Z(SP)	OTIR 263-B3 20M/15K--Z(SP)				
27	LDDR 270-B8 21M/16K--P(SZ)	CPDR 271-B9 21M/16K--SZP	INDR 272-BA 20M/15K--Z(SP)	OTDR 273-BB 20M/15K--Z(SP)				

313 PREFIX GROUP			
RLC r 313/00r 8B/23H--SZPC	RRC r 313/01r 8B/23H--SZPC	RL r 313/02r 8B/23H--SZPC	RR r 313/03r 8B/23H--SZPC
SLA r 313/04r 8B/23H--SZPC	SRA r 313/05r 8B/23H--SZPC	— 313/0x6 15B	SRL r 313/07r 8B/23H--SZPC
BIT/RES/SET 313/xb6 12B	BIT b,r 313/1br 8B/20H--Z(SP)	RES b,r 313/2br 8B/20H	SET b,r 313/3br 8B/20H

SLASH INDICATES TWO WORD OPCODE
"b" = "bit" 7 = MSB, 0 = LSB
"r" = "register" SEE REGISTER LIST

Table 2-6. Symbology used in Table 2-7

SYMBOL	INTERPRETATION
A	The Accumulator.
(Ā)	The complement of accumulator contents.
a	A single hexadecimal digit being interpreted as data.
aa	Two hexadecimal digits being interpreted as a single byte of data, or as the high order byte of 16 bits of data.
bb	Two hexadecimal digits being interpreted as the low order byte of 16 bits of data.
Binary	Binary arithmetic specified.
C	The carry status flag.
DB	F8 System Data Bus.
DC0	The primary data counter register.
DC0L	The low order byte of the primary data counter register.
DC0U	The high order byte of the primary data counter register.
DC1	The secondary data counter register.
Decimal	Decimal arithmetic specified.
e	A single octal digit being interpreted as data.
H	Scratchpad bytes 10 and 11.
ii	Two hexadecimal digits being interpreted as the high order byte of a 16-bit address, or as a simple byte address displacement.
ISAR	The six-bit scratchpad address register.
ISARL	The low order three bits of ISAR.
ISARU	The high order three bits of ISAR.
J	Scratchpad byte 9.
jj	Two hexadecimal digits being interpreted as the low order byte of a 16-bit address.
K	Scratchpad bytes 12 and 13.
KL	Scratchpad byte 13.
KU	Scratchpad byte 12.
O	The overflow status flag.
P	A single hexadecimal digit being interpreted as an I/O port address (0-15).
PP	Two hexadecimal digits being interpreted as an I/O port address (0-255).
PC0	The program counter register.
PC0L	The low order byte of the program counter register.
PC0U	The high order byte of the program counter register.
PC1	The static register.
PC1L	The low order byte of the stack register.
PC1U	The high order byte of the stack register.
Q	Scratchpad bytes 14 and 15.
QL	Scratchpad byte 15.
QU	Scratchpad byte 14.
r	Single hexadecimal digit interpreted as scratchpad address: r = 0 through B for locations 0 through B in scratchpad r = C for ISAR as address source with no change after access r = D for ISAR as address source with ISARL = ISARL + 1 after access. r = E for ISAR as address source with ISARL = ISARL -1 after access r = F is not allowed
S	The sign status flag.
t	A single hexadecimal digit identifying a status condition which will be tested by a "Branch on Condition" instruction.
W	The status register.
Z	The zero status flag.
∧	The logical OR of 8-bit quantities on each side of this symbol is specified.
⊕	The logical Exclusive-OR of 8-bit quantities on each side of this symbol is specified.
←	The value to the right of this symbol is to be loaded into the location specified on the left of this symbol.
( )	The contents of the location within the brackets is specified.
(( ))	The contents of the memory word addressed by the contents of the location within the double brackets is specified.
+	The binary address of 8-bit quantities on each side of this symbol is specified.

Table 2-7. Instructions' Execution and Timing

OP CODE	OPERAND(S)	OBJECT CODE	CYCLE	ROMC STATE	TIMING	STATUS FLAGS O	Z	C	S	INTERRUPT	FUNCTION
LR	A, KU	00	S	0	3S	–	–	–	–		A ← (r12)
LR	A, KL	01	S	0	3S	–	–	–	–		A ← (r13)
LR	A, QU	02	S	0	3S	–	–	–	–		A ← (r14)
LR	A, QL	03	S	0	3S	–	–	–	–		A ← (r15)
LR	KU, A	04	S	0	3S	–	–	–	–		r12 ← (A)
LR	KL, A	05	S	0	3S	–	–	–	–		r13 ← (A)
LR	QU, A	06	S	0	3S	–	–	–	–		r14 ← (A)
LR	QL, A	07	S	0	3S	–	–	–	–		r15 ← (A)
LR	K, P	08	L	7	5	–	–	–	–		r12 ← (PC1U)
			L	B	5	–	–	–	–		r13 ← (PC1L)
			S	0	3S	–	–	–	–		
LR	P, K	09	L	15	2	–	–	–	–		PC1U ← (r12)
			L	18	2	–	–	–	–		PC1L ← (r13)
			S	0	3S	–	–	–	–		
LR	A, IS	0A	S	0	3S	–	–	–	–		A ← (ISAR)
LR	IS, A	0B	S	0	3S	–	–	–	–		ISAR ← (A)
PK		0C	L	12	2	–	–	–	–		PC1 ← (PC0); PC0L ← (r13)
			L	14	2	–	–	–	–		PC0U ← (r12)
			S	0	3S	–	–	–	–	x	
LR	P0, Q	0D	L	17	2	–	–	–	–		PC0L ← (r15)
			L	14	2	–	–	–	–		PC0U ← (r14)
			S	0	3S	–	–	–	–		

Table 2-7. Instructions' Execution and Timing (Continued)

OP CODE	OPERAND(S)	OBJECT CODE	CYCLE	ROMC STATE	TIMING	STATUS FLAGS O	Z	C	S	INTERRUPT	FUNCTION
LR	Q, DC	0E	L	6	5	–	–	–	–		r14 ← (DC0U)
			L	9	5	–	–	–	–		r15 ← (DC0L)
			S	0	3S	–	–	–	–		
LR	DC, Q	0F	L	16	2	–	–	–	–		DC0U ← (R14)
			L	19	2	–	–	–	–		DC0L ← (R15)
			S	0	3S	–	–	–	–		
LR	DC, H	10	L	16	2	–	–	–	–		DC0U ← (R10)
			L	19	2	–	–	–	–		DC0L ← (R11)
			S	0	3S	–	–	–	–		
LR	H, DC	11	L	6	5	–	–	–	–		r10 ← (DC0U)
			L	9	5	–	–	–	–		r11 ← (DC0L)
			S	0	3S	–	–	–	–		
SR	1	12	S	0	3S	0	1/0	0	1		Shift (A) right one bit position (zero fill)
SL	1	13	S	0	3S	0	1/0	0	1/0		Shift (A) left one bit position (zero fill)
SR	4	14	S	0	3S	0	1/0	0	1		Shift (A) right four bit positions (zero fill)
SL	4	15	S	0	3S	0	1/0	0	1/0		Shift (A) left four bit positions (zero fill)
LM		16	L	2	6	–	–	–	–		A ← ((DC0))
			S	0	3S	–	–	–	–		
ST		17	L	5	1	–	–	–	–		(DC) ← (A)
			S	0	3S	–	–	–	–		
COM		18	S	0	3S	0	1/0	0	1/0		A ← (A) ⊕ H'FF' Complement accumulator
LNK		19	S	0	3S	1/0	1/0	1/0	1/0		A ← (A) + (C)
DI		1A	S	1C	0	–	–	–	–	v	Clear ICB.
			S	0	3S	–	–	–	–		
EI		1B	S	1C	0	–	–	–	–		Set ICB.
			S	0	3S	–	–	–	–	x	
POP		1C	S	4	0	–	–	–	–		PC0 ← (PC1)
			S	0	3S	–	–	–	–	x	
LR	W, J	1D	S	1C	0	1/0	1/0	1/0	1/0		W ← (r9)
			S	0	3S	–	–	–	–	x	
LR	J, W	1E	S	0	3S	–	–	–	–		r9 ← (W)
INC		1F	S	0	3S	1/0	1/0	1/0	1/0		A ← (A) + 1
LI	aa	20	L	3	6	–	–	–	–		A ← H'aa'
	aa		S	0	3S	–	–	–	–		
NI	aa	21	L	3	4	0	1/0	0	1/0		A ← (A) ∧ H'aa'
	aa		S	0	3S	–	–	–	–		
OI	aa	22	L	3	4	0	1/0	0	1/0		A ← (A) ∨ H'aa'
	aa		S	0	3S	–	–	–	–		
XI	aa	23	L	3	4	0	1/0	0	1/0		A ← (A) ⊕ H'aa'
	aa		S	0	3S	–	–	–	–		
AI	aa	24	L	3	4	1/0	1/0	1/0	1/0		A ← (A) + H'aa'
	aa		S	0	3S	–	–	–	–		

Table 2-7. Instructions' Execution and Timing (Continued)

OP CODE	OPERAND(S)	OBJECT CODE	CYCLE	ROMC STATE	TIMING	STATUS FLAGS O	Z	C	S	INTERRUPT	FUNCTION
CI	aa	25	L	3	4	–	–	–	–		Perform H'aa' + (Ā) + 1. Do not save result, but modify status flags to reflect result.
	aa	aa	S	0	3S	1/0	1/0	1/0	1/0		
IN	PP	26	L	3	2	–	–	–	–		DB ← PP
	PP	PP	L	1B	6	0	1/0	0	1/0		A ← (I/O Port PP)
			S	0	3S	–	–	–	–		
OUT	PP	27	L	3	2	–	–	–	–		DB ← PP
	PP	pp	L	1A	1	–	–	–	–		I/O Port PP ← (A)
			S	0	3S	–	–	–	–	x	
PI	iijj	28	L	3	6	–	–	–	–		A ← H'ii'
	ii	ii	S	D	0	–	–	–	–		PC1 ← (PC0) + 1
	jj	jj	L	C	2	–	–	–	–		PC0L ← H'jj'
			L	14	1	–	–	–	–		PC0U ← (A)
			S	0	3S	–	–	–	–	x	
JMP	iijj	29	L	3	6	–	–	–	–		A ← H'ii'
	ii	ii	L	C	2	–	–	–	–		PC0L ← H'jj'
	jj	jj	L	14	1	–	–	–	–		PC0U ← (A)
			S	0	3S	–	–	–	–	x	
DCI	iijj	2A	L	11	2	–	–	–	–		DC0U ← ii
	ii	ii	S	3	0	–	–	–	–		(increment PC0)
	jj	jj	L	E	2	–	–	–	–		DC0L ← jj
			S	3	0	–	–	–	–		(increment PC0)
			S	0	3S	–	–	–	–		
NOP		2B	S	0	0	–	–	–	–		
XDC		2C	S	1D	0	–	–	–	–		DC0 ⇄ DC1
			S	0	0	–	–	–	–		
DS	r	3r	L	0	3L	1/0	1/0	1/0	1/0		r ← (r) + H'FF' Decrement scratchpad byte
LR	A, r	4r	S	0	3S						A ← (r)
LR	r, A	5r	S	0	3S						r ← (A)
LISU	e	6e	S	0	3S						ISARU ← 0'e'
LISL	e	68 + e	S	0	3S						ISARL ← 0'e'
LIS	a	7a	S	0	3S						A ← H'0a'
BT	e, ii	8e	S	1C	0						Test e / W register
	ii	ii	S	3	0						Res = 0 so PC0 ← (PC0) + 2
			S	0	3S						
			S	1C	0						Test e / W register
			L	1	2						Res ≠ 0 so PC0 ← (PC0) + H'ii' + 1
			S	0	3S						
AM		88	L	2	4	1/0	1/0	1/0	1/0		A ← (A) + ((DC0)) Binary, DC0 ← (DC) + 1
			S	0	3S						
AMD		89	L	2	4	1/0	1/0	1/0	1/0		A ← (A) + ((DC0)) Decimal, DC0 ← (DC0) + 1
			S	0	3S						

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INSTRUCTION/ FORMS		6809 ADDRESSING MODES: INHERENT OP	~	#	DIRECT OP	~	#	EXTENDED OP	~	#	IMMEDIATE OP	~	#	INDEXED[1] OP	~	#	RELATIVE OP	~[5]	#	DESCRIPTION	5 H	3 N	2 Z	1 V	0 C
ABX		3A	3	1																	B + X → X (UNSIGNED)	•	•	•	•	•
ADC	ADCA				99	4	2	B9	5	3	89	2	2	A9	4+	2+					A + M + C → A	↕	↕	↕	↕	↕
	ADCB				D9	4	2	F9	5	3	C9	2	2	E9	4+	2+					B + M + C → B	↕	↕	↕	↕	↕
ADD	ADDA				9B	4	2	BB	5	3	8B	2	2	AB	4+	2+					A + M → A	↕	↕	↕	↕	↕
	ADDB				DB	4	2	FB	5	3	CB	2	2	EB	4+	2+					B + M → B	↕	↕	↕	↕	↕
	ADDD				D3	6	2	F3	7	3	C3	4	3	E3	6+	2+					D + M:M + 1 → D	↕	↕	↕	↕	↕
AND	ANDA				94	4	2	B4	5	3	84	2	2	A4	4+	2+					A ∧ M → A	•	↕	↕	0	•
	ANDB				D4	4	2	F4	5	3	C4	2	2	E4	4+	2+					B ∧ M → B	•	↕	↕	0	•
	ANDCC										1C	3	2								CC ∧ IMM → CC					↕
ASL	ASLA	48	2	1																	A/B/M c b7 b0	↕	↕	↕	↕	↕
	ASLB	58	2	1																		↕	↕	↕	↕	↕
	ASL				08	6	2	78	7	3				68	6+	2+						↕	↕	↕	↕	↕
ASR	ASRA	47	2	1																	A/B/M b7 b0 c	↕	↕	↕	•	↕
	ASR	57	2	1																		↕	↕	↕	•	↕
	ASR				07	6	2	77	7	3				67	6+	2+						↕	↕	↕	•	↕
BCC	BCC																24	3	2		Branch C = 0	•	•	•	•	•
	LBCC																10 24	5(6)	4		Long Branch C = 0	•	•	•	•	•
BCS	BCS																25	3	2		Branch C = 1	•	•	•	•	•
	LBCS																10 25	5(6)	4		Long Branch C = 1	•	•	•	•	•
BEQ	BEQ																27	3	2		Branch Z = 0	•	•	•	•	•
	LBEQ																10 27	5(6)	4		Long Branch Z = 0	•	•	•	•	•
BGE	BGE																2C	3	2		Branch ≥ Zero	•	•	•	•	•
	LBGE																10 2C	5(6)	4		Long Branch ≥ Zero	•	•	•	•	•
BGT	BGT																2E	3	2		Branch > Zero	•	•	•	•	•
	LBGT																10 2E	5(6)	4		Long Branch > Zero	•	•	•	•	•
BHI	BHI																22	3	2		Branch Higher	•	•	•	•	•
	LBHI																10 22	5(6)	4		Long Branch Higher	•	•	•	•	•
BHS	BHS																24	3	2		Branch Higher or Same	•	•	•	•	•
	LBHS																10 24	5(6)	4		Long Branch Higher or Same	•	•	•	•	•
BIT	BITA				95	4	2	B5	5	3	85	2	2	A5	4+	2+					Bit Test A (M ∧ A)	•	↕	↕	0	•
	BITB				D5	4	2	F5	5	3	C5	2	2	E5	4+	2+					Bit Test B (M ∧ B)	•	↕	↕	0	•
BLE	BLE																2F	3	2		Branch ≤ Zero	•	•	•	•	•
	LBLE																10 2F	5(6)	4		Long Branch ≤ Zero	•	•	•	•	•
BLO	BLO																25	3	2		Branch Lower	•	•	•	•	•
	LBLO																10 25	5(6)	4		Long Branch Lower	•	•	•	•	•
BLS	BLS																23	3	2		Branch Lower or Same	•	•	•	•	•
	LBLS																10 23	5(6)	4		Long Branch Lower or Same	•	•	•	•	•
BLT	BLT																2D	3	2		Branch < Zero	•	•	•	•	•
	LBLT																10 2D	5(6)	4		Long Branch < Zero	•	•	•	•	•
BMI	BMI																2B	3	2		Branch Minus	•	•	•	•	•
	LBMI																10 2B	5(6)	4		Long Branch Minus	•	•	•	•	•
BNE	BNE																26	3	2		Branch Z ≠ 0	•	•	•	•	•
	LBNE																10 26	5(6)	4		Long Branch Z ≠ 0	•	•	•	•	•
BPL	BPL																2A	3	2		Branch Plus	•	•	•	•	•
	LBPL																10 2A	5(6)	4		Long Branch Plus	•	•	•	•	•
BRA	BRA																20	3	2		Branch Always	•	•	•	•	•
	LBRA																16	5	3		Long Branch Always	•	•	•	•	•
BRN	BRN																21	3	2		Branch Never	•	•	•	•	•
	LBRN																10 21	5	4		Long Branch Never	•	•	•	•	•

Cont'd on next page

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS124 Con'd

INSTRUCTION/ FORMS		INHERENT OP	~	#	DIRECT OP	~	#	EXTENDED OP	~	#	IMMEDIATE OP	~	#	INDEXED[1] OP	~	#	RELATIVE OP	~[5]	#	DESCRIPTION	5 H	3 N	2 Z	1 V	0 C
BSR	BSR																8D	7	2	Branch to Subroutine	•	•	•	•	•
	LBSR																17	9	3	Long Branch to Subroutine	•	•	•	•	•
BVC	BVC																28	3	2	Branch V = 0	•	•	•	•	•
	LBVC																10 28	5(6)	4	Long Branch V = 0	•	•	•	•	•
BVS	BVS																29	3	2	Branch V = 1	•	•	•	•	•
	LBVS																10 29	5(6)	4	Long Branch V = 1	•	•	•	•	•
CLR	CLRA	4F	2	1																0 → A	•	0	1	0	0
	CLRB	5F	2	1																0 → B	•	0	1	0	0
	CLR				0F	6	2	7F	7	3				6F	6+	2+				0 → M	•	0	1	0	0
CMP	CMPA				91	4	2	B1	5	3	81	2	2	A1	4+	2+				Compare M from A	8	‡	‡	‡	‡
	CMPB				D1	4	2	F1	5	3	C1	2	2	E1	4+	2+				Compare M from B	8	‡	‡	‡	‡
	CMPD				10 93	7	3	10 B3	8	4	10 83	5	4	10 A3	7+	3+				Compare M: M + 1 from D	•	‡	‡	‡	‡
	CMPS				11 9C	7	3	11 BC	8	4	11 8C	5	4	11 AC	7+	3+				Compare M: M + 1 from S	•	‡	‡	‡	‡
	CMPU				11 93	7	3	11 B3	8	4	11 83	5	4	11 A3	7+	3+				Compare M: M + 1 from U	•	‡	‡	‡	‡
	CMPX				9C	6	2	BC	7	3	8C	4	3	AC	6+	2+				Compare M: M + 1 from X	•	‡	‡	‡	‡
	CMPY				10 9C	7	3	10 BC	8	4	10 8C	5	4	10 AC	7+	3+				Compare M: M + 1 from Y	•	‡	‡	‡	‡
COM	COMA	43	2	1																Ā → A	•	‡	‡	0	1
	COMB	53	2	1																B̄ → B	•	‡	‡	0	1
	COM				03	6	2	73	7	3				63	6+	2+				M̄ → M	•	‡	‡	0	1
CWAI		3C	20	2																CC ∧ IMM → CC; Wait for Interrupt					1
DAA		19	2	1																Decimal Adjust A	•	‡	‡	0	‡
DEC	DECA	4A	2	1																A − 1 → A	•	‡	‡	‡	•
	DECB	5A	2	1																B − 1 → B	•	‡	‡	‡	•
	DEC				0A	6	2	7A	7	3				6A	6+	2+				M − 1 → M	•	‡	‡	‡	•
EOR	EORA				98	4	2	B8	5	3	88	2	2	A8	4+	2+				A ∨ M → A	•	‡	‡	0	•
	EORB				D8	4	2	F8	5	3	C8	2	2	E8	4+	2+				B ∨ M → B	•	‡	‡	0	•
EXG	R1, R2	1E	7	2																R1 ↔ R2[2]	•	•	•	•	•
INC	INCA	4C	2	1																A + 1 → A	•	‡	‡	‡	•
	INCB	5C	2	1																B + 1 → B	•	‡	‡	‡	•
	INC				0C	6	2	7C	7	3				6C	6+	2+				M + 1 → M	•	‡	‡	‡	•
JMP					0E	3	2	7E	4	3				6E	3+	2+				EA[3] → PC	•	•	•	•	•
JSR					9D	7	2	BD	8	3				AD	7+	2+				Jump to Subroutine	•	•	•	•	•
LD	LDA				96	4	2	B6	5	3	86	2	2	A6	4+	2+				M → A	•	‡	‡	0	•
	LDB				D6	4	2	F6	5	3	C6	2	2	E6	4+	2+				M → B	•	‡	‡	0	•
	LDD				DC	5	2	FC	6	3	CC	3	3	EC	5+	2+				M: M + 1 → D	•	‡	‡	0	•
	LDS				10 DE	6	3	10 FE	7	4	10 CE	4	4	10 EE	6+	3+				M: M + 1 → S	•	‡	‡	0	•
	LDU				DE	5	2	FE	6	3	CE	3	3	EE	5+	2+				M: M + 1 → U	•	‡	‡	0	•
	LDX				9E	5	2	BE	6	3	8E	3	3	AE	5+	2+				M: M + 1 → X	•	‡	‡	0	•
	LDY				10 9E	6	3	10 BE	7	4	10 8E	4	4	10 AE	6+	3+				M: M + 1 → Y	•	‡	‡	0	•
LEA	LEAS													32	4+	2+				EA[3] → S	•	•	•	•	•
	LEAU													33	4+	2+				EA[3] → U	•	•	•	•	•
	LEAX													30	4+	2+				EA[3] → X	•	•	‡	•	•
	LEAY													31	4+	2+				EA[3] → Y	•	•	‡	•	•
LSL	LSLA	48	2	1																A, B, M } C b7 b0 ← 0	•	‡	‡	‡	‡
	LSLB	58	2	1																	•	‡	‡	‡	‡
	LSL				08	6	2	78	7	3				68	6+	2+					•	‡	‡	‡	‡
LSR	LSRA	44	2	1																A, B, M } 0 → b7 b0 C	•	0	‡	•	‡
	LSRB	54	2	1																	•	0	‡	•	‡
	LSR				04	6	2	74	7	3				64	6+	2+					•	0	‡	•	‡
MUL		3D	11	1																A × B → D (Unsigned)	•	•	‡	•	9
NEG	NEGA	40	2	1																Ā + 1 → A	8	‡	‡	‡	‡
	NEGB	50	2	1																B̄ + 1 → B	8	‡	‡	‡	‡
	NEG				00	6	2	70	7	3				60	6+	2+				M̄ + 1 → M	8	‡	‡	‡	‡
NOP		12	2	1																No Operation	•	•	•	•	•
OR	ORA				9A	4	2	BA	5	3	8A	2	2	AA	4+	2+				A ∨ M → A	•	‡	‡	0	•
	ORB				DA	4	2	FA	5	3	CA	2	2	EA	4+	2+				B ∨ M → B	•	‡	‡	0	•
	ORCC										1A	3	2							CC ∨ IMM → CC					7
PSH	PSHS	34	5+[4]	2																Push Registers on S Stack	•	•	•	•	•
	PSHU	36	5+[4]	2																Push Registers on U Stack	•	•	•	•	•

INSTRUCTION/ FORMS	INHERENT OP	~	#	DIRECT OP	~	#	EXTENDED OP	~	#	IMMEDIATE OP	~	#	INDEXED[1] OP	~	#	RELATIVE OP	~[5]	#	DESCRIPTION	5 H	3 N	2 Z	1 V	0 C

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PUL	PULS	35	5+	2														Pull Registers from S Stack	•	•	•	•	•
	PULU	37	5+	2														Pull Registers from U Stack	•	•	•	•	•
ROL	ROLA	49	2	1														A	•	↕	↕	↕	↕
	ROLB	59	2	1														B	•	↕	↕	↕	↕
	ROL				09	6	2	79	7	3				69	6+	2+		M c b7 ← b0	•	↕	↕	↕	↕
ROR	RORA	46	2	1														A	•	↕	↕	•	↕
	RORB	56	2	1														B	•	↕	↕	•	↕
	ROR				06	6	2	76	7	3				66	6+	2+		M c b7 → b0	•	↕	↕	•	↕
RTI		3B	6/15	1														Return From Interrupt					7
RTS		39	5	1														Return From Subroutine	•	•	•	•	•
SBC	SBCA				92	4	2	B2	5	3	82	2	2	A2	4+	2+		A − M − C → A	8	↕	↕	↕	↕
	SBCB				D2	4	2	F2	5	3	C2	2	2	E2	4+	2+		B − M − C → B	8	↕	↕	↕	↕
SEX		1D	2	1														Sign Extend B into A	•	↕	↕	0	•
ST	STA				97	4	2	B7	5	3				A7	4+	2+		A → M	•	↕	↕	0	•
	STB				D7	4	2	F7	5	3				E7	4+	2+		B → M	•	↕	↕	0	•
	STD				DD	5	2	FD	6	3				ED	5+	2+		D → M: M + 1	•	↕	↕	0	•
	STS				10	6	3	10	7	4				10	6+	3+		S → M: M + 1	•	↕	↕	0	•
					DF			FF						EF									
	STU				DF	5	2	FF	6	3				EF	5+	2+		U → M: M + 1	•	↕	↕	0	•
	STX				9F	5	2	BF	6	3				AF	5+	2+		X → M: M + 1	•	↕	↕	0	•
	STY				10	6	3	10	7	4				10				Y → M: M + 1	•	↕	↕	0	•
					9F			BF						AF	6+	3+							
SUB	SUBA				90	4	2	B0	5	3	80	2	2	A0	4+	2+		A − M → A	8	↕	↕	↕	↕
	SUBB				D0	4	2	F0	5	3	C0	2	2	E0	4+	2+		B − M → B	8	↕	↕	↕	↕
	SUBD				93	6	2	B3	7	3	83	4	3	A3	6+	2+		D − M: M + 1 → D	•	↕	↕	↕	↕
SWI	SWI[1]	3F	19	1														Software Interrupt 1	•	•	•	•	•
	SWI2[2]	10 3F	20	2														Software Interrupt 2	•	•	•	•	•
	SWI3[3]	11 3F	20	2														Software Interrupt 3	•	•	•	•	•
SYNC		13	≥2	1														Synchronize to Interrupt	•	•	•	•	•
TFR	R1, R2	1F	7	2														R1 → R2[4]	•	•	•	•	•
TST	TSTA	4D	2	1														Test A	•	↕	↕	0	•
	TSTB	5D	2	1														Test B	•	↕	↕	0	•
	TST				0D	6	2	7D	7	3				6D	6+	2+		Test M	•	↕	↕	0	•

INDEXED ADDRESSING MODES

		NON INDIRECT				INDIRECT			
TYPE	FORMS	Assembler Form	Post-Byte OP Code	+ ~	+ #	Assembler Form	Post-Byte OP Code	+ ~	+ #
CONSTANT OFFSET FROM R	NO OFFSET	, R	1RR00100	0	0	[, R]	1RR10100	3	0
	5 BIT OFFSET	n, R	0RRnnnnn	1	0	defaults to 8-bit			
	8 BIT OFFSET	n, R	1RR01000	1	1	[n, R]	1RR11000	4	1
	16 BIT OFFSET	n, R	1RR01001	4	2	[n, R]	1RR11001	7	2
ACCUMULATOR OFFSET FROM R	A—REGISTER OFFSET	A, R	1RR00110	1	0	[A, R]	1RR10110	4	0
	B—REGISTER OFFSET	B, R	1RR00101	1	0	[B, R]	1RR10101	4	0
	D—REGISTER OFFSET	D, R	1RR01011	4	0	[D, R]	1RR11011	7	0
AUTO INCREMENT/DECREMENT R	INCREMENT BY 1	, R+	1RR00000	2	0	not allowed			
	INCREMENT BY 2	, R++	1RR00001	3	0	[, R++]	1RR10001	6	0
	DECREMENT BY 1	, −R	1RR00010	2	0	not allowed			
	DECREMENT BY 2	, −−R	1RR00011	3	0	[, −−R]	1RR10011	6	0
CONSTANT OFFSET FROM PC	8 BIT OFFSET	n, PCR	1XX01100	1	1	[n, PCR]	1XX11100	4	1
	16 BIT OFFSET	n, PCR	1XX01101	5	2	[n, PCR]	1XX11101	8	2
EXTENDED INDIRECT	16 BIT ADDRESS	—	—	-	-	[n]	10011111	5	2

R = X, Y, U, or S
X = DON'T CARE

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6809 STACKING ORDER

INCREASING MEMORY ↓

PULL ORDER ↓

CC
A
B
DP
X Hi
X Lo
Y Hi
Y Lo
U/S Hi
U/S Lo
PC Hi
PC Lo

↑ PUSH ORDER

6809 VECTORS

FFFE	Restart
FFFC	NMI
FFFA	SWI
FFF8	IRQ
FFF6	FIRQ
FFF4	SWI2
FFF2	SWI3
FFF0	Reserved

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Simple Conditional Branches

Condition	*Complement*
BEQ	BNE
BMI	BPL
BCS	BCC
BVS	BVC

Signed Conditional Branches

Condition	*Complement*
BGT	BLE
BGE	BLT
BEQ	BNE
BLE	BGT
BLT	BGE

Unsigned Conditional Branches

Condition	*Complement*
BHI	BLS
BHS	BLO
BEQ	BNE
BLS	BHI
BLO	BHS

HEXADECIMAL AND DECIMAL CONVERSION

HOW TO USE THE TABLES

CONVERSION TO DECIMAL. Find the decimal weights for corresponding hexadecimal characters beginning with the least significant character. The sum of the decimal weight is the decimal value of the hexadecimal number.

CONVERSION TO HEXADECIMAL. Find the highest decimal value in the table which is lower than or equal to the decimal number to be converted. The corresponding hexadecimal character is the most significant character. Subtract the decimal value found from the decimal number to be converted. With this difference repeat the process to find subsequent hexadecimal characters.

HEXADECIMAL AND DECIMAL CONVERSION

15 BYTE 8				7 BYTE 0			
15 CHAR 12		11 CHAR 8		7 CHAR 4		3 CHAR 0	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0
1	4 096	1	256	1	16	1	1
2	8 192	2	512	2	32	2	2
3	12 288	3	768	3	48	3	3
4	16 384	4	1 024	4	64	4	4
5	20 480	5	1 280	5	80	5	5
6	24 576	6	1 536	6	96	6	6
7	28 672	7	1 792	7	112	7	7
8	32 768	8	2 048	8	128	8	8
9	36 864	9	2 304	9	144	9	9
A	40 960	A	2 560	A	160	A	10
B	45 056	B	2 816	B	176	B	11
C	49 152	C	3 072	C	192	C	12
D	53 248	D	3 328	D	208	D	13
E	57 344	E	3 584	E	224	E	14
F	61 440	F	3 840	F	240	F	15

POWERS OF TWO

n	2^n
	1
	2
	4
	8
	16
	32
	64
	128
	256
	512
	1 024
	2 048
	4 096
	8 192
	16 384
	32 768
	65 536
	131 072
	262 144
	524 288
	1 048 576

ASCII CHARACTER SET (7-BIT CODE)

MS CHAR / LS CHAR	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0 0000	NUL	DLE	SP	0	@	P	`	p
1 0001	SOH	DC1	!	1	A	Q	a	q
2 0010	STX	DC2	"	2	B	R	b	r
3 0011	ETC	DC3	#	3	C	S	c	s
4 0100	EOT	DC4	$	4	D	T	d	t
5 0101	ENQ	NAK	%	5	E	U	e	u
6 0110	ACK	SYN	&	6	F	V	f	v
7 0111	BEL	ETB	'	7	G	W	g	w
8 1000	BS	CAN	(	8	H	X	h	x
9 1001	HT	EM	)	9	I	Y	i	y
A 1010	LF	SUB	*	:	J	Z	j	z
B 1011	VT	ESC	+	;	K	[	k	{
C 1100	FF	FS	,	<	L	\	l	|
D 1101	CR	GS	-	=	M	]	m	}
E 1110	SO	RS	.	>	N	↑	n	~
F 1111	SI	US	/	?	O	←	o	DEL

INDEXED ADDRESSING POST BYTE REGISTER BIT ASSIGNMENTS

POST-BYTE REGISTER BIT								INDEXED ADDRESSING MODE
7	6	5	4	3	2	1	0	
0	X	X	X	X	X	X	X	EA = ,R ± 4 BIT OFFSET
1	X	X	0	0	0	0	0	,R+
1	X	X	X	0	0	0	1	,R++
1	X	X	0	0	0	1	0	,-R
1	X	X	X	0	0	1	1	,--R
1	X	X	X	0	1	0	0	EA = ,R ± 0 OFFSET
1	X	X	X	0	1	0	1	EA = ,R ± ACCB OFFSET
1	X	X	X	0	1	1	0	EA = ,R ± ACCA OFFSET
1	X	X	X	1	0	0	0	EA = ,R ± 7 BIT OFFSET
1	X	X	X	1	0	0	1	EA = ,R ± 15 BIT OFFSET
1	X	X	X	1	0	1	1	EA = ,R ± D OFFSET)
1	X	X	X	1	1	0	0	EA = ,PC ± 7 BIT OFFSET
1	X	X	X	1	1	0	1	EA = ,PC ± 15 BIT OFFSET
1	X	X	1	1	1	1	1	EA = ,ADDRESS

ADDRESSING MODE FIELD

I FIELD
FOR B7 = 1: INDIRECT
FOR B7 = 0: SIGN BIT

REGISTER FIELD
00:R = X
01:R = Y
10:R = U
11:R = S

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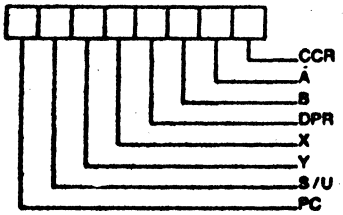
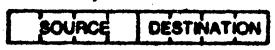
PUSH/PULL POST BYTE



TRANSFER/EXCHANGE POST BYTE



REGISTER FIELD

0000 = D (A:B)
0001 = X
0010 = Y
0011 = U
0100 = S
0101 = PC
1000 = A
1001 = B
1010 = CCR
1011 = DPR

OP	MNEM	MODE	~	#
00	NEG	DIRECT	6	2
03	COM	↑	6	2
04	LSR		6	2
06	ROR		6	2
07	ASR		6	2
08	ASL/LSL		6	2
09	ROL		6	2
0A	DEC		6	2
0C	INC		6	2
0D	TST		6	2
0E	JMP	↓	3	2
0F	CLR	DIRECT	6	2
12	NOP	INHERENT	2	1
13	SYNC	INHERENT	2	1
16	LBRA	RELATIVE	5	3
17	LBSR	RELATIVE	9	3
19	DAA	INHERENT	2	1
1A	ORCC	IMMED	3	2

OP	MNEM	MODE	~	#
1C	ANDCC	IMMED	3	2
1D	SEX	INHERENT	2	1
1E	EXG	↕	8	2
1F	TFR	INHERENT	7	2
20	BRA	RELATIVE	3	2
21	BRN	↑	3	2
22	BHI		3	2
23	BLS		3	2
24	BHS/BCC		3	2
25	BLO/BCS		3	2
26	BNE		3	2
27	BEQ		3	2
28	BVC		3	2
29	BVS		3	2
2A	BPL		3	2
2B	BMI		3	2
2C	BGE		3	2
2D	BLT	↓ RELATIVE	3	2

OP	MNEM	MODE	~	#
2E	BGT	RELATIVE	3	2
2F	BLE	RELATIVE	3	2
30	LEAX	INDEXED	4	2
31	LEAY	↕	4	2
32	LEAS		4	2
33	LEAU	INDEXED	4	2
34	PSHS	INHERENT	5	2
35	PULS	↑	5	2
36	PSHU		5	2
37	PULU		5	2
39	RTS		5	1
3A	ABX		3	1
3B	RTI		6/16	1
3C	CWAI		21	2
3D	MUL		11	1
3F	SWI		19	1
40	NEGA	↓	2	1
43	COMA	INHERENT	2	1

OP	MNEM	MODE	~	#
44	LSRA	INHERENT	2	1
46	RORA	↑	2	1
47	ASRA		2	1
48	ASLA/LSLA		2	1
49	ROLA		2	1
4A	DECA		2	1
4C	INCA		2	1
4D	TSTA		2	1
4F	CLRA		2	1
50	NEGB		2	1
53	COMB		2	1
54	LSRB		2	1
56	RORB		2	1
57	ASRA		2	1
58	ASLB/LSLB		2	1
59	ROLB		2	1
5A	DECB		2	1
5C	INCB	↓ INHERENT	2	1

OP	MNEM	MODE	~	#
5D	TSTB	INHERENT	2	1
5F	CLRB	INHERENT	2	1
60	NEG	INDEXED	6	2
63	COM	↑	6	2
64	LSR		6	2
66	ROR		6	2
67	ASR		6	2
68	ASL/LSL		6	2
69	ROL		6	2
6A	DEC		6	2
6C	INC		6	2
6D	TST		6	2
6E	JMP	↓	3	2
6F	CLR	INDEXED	6	2
70	NEG	EXTENDED	7	3
73	COM	↑	7	3
74	LSR		7	3
76	ROR	↓ EXTENDED	7	3

OP	MNEM	MODE	~	#
77	ASR	EXTENDED	7	3
78	ASL/LSL	↑	7	3
79	ROL		7	3
7A	DEC		7	3
7C	INC		7	3
7D	TST		7	3
7E	JMP	↓	4	3
7F	CLR	EXTENDED	7	3
80	SUBA	IMMED	2	2
81	CMPA	↑	2	2
82	SBCA		2	2
83	SUBD		4	3
84	ANDA		2	2
85	BITA		2	2
86	LDA		2	2
88	EORA		2	2
89	ADCA		2	2
8A	ORA	↓ IMMED	2	2

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OP	MNEM	MODE	~	#
8B	ADDA	IMMED	2	2
8C	CMPX	IMMED	4	3
8D	BSR	RELATIVE	7	2
8E	LDX	IMMED	3	3
90	SUBA	DIRECT	4	2
91	CMPA	↕	4	2
92	SBCA	↕	4	2
93	SUBD	↕	6	2
94	ANDA	↕	4	2
95	BITA	↕	4	2
96	LDA	↕	4	2
97	STA	↕	4	2
98	EORA	↕	4	2
99	ADCA	↕	4	2
9A	ORA	↕	4	2
9B	ADDA	↕	4	2
9C	CMPX	↕	6	2
9D	JSR	DIRECT	7	2
9E	LDX	DIRECT	5	2
9F	STX	DIRECT	5	2
A0	SUBA	INDEXED	4	2
A1	CMPA	↕	4	2
A2	SBCA	↕	4	2
A3	SUBD	↕	6	2
A4	ANDA	↕	4	2
A5	BITA	↕	4	2
A6	LDA	↕	4	2
A7	STA	↕	4	2
A8	EORA	↕	4	2
A9	ADCA	↕	4	2
AA	ORA	↕	4	2
AB	ADDA	↕	4	2
AC	CMPX	↕	6	2
AD	JSR	↕	7	2
AE	LDX	↕	5	2
AF	STX	INDEXED	5	2
B0	SUBA	EXTENDED	5	3
B1	CMPA	↕	5	3
B2	SBCA	↕	5	3
B3	SUBD	↕	7	3
B4	ANDA	↕	5	3
B5	BITA	↕	5	3
B6	LDA	↕	5	3
B7	STA	↕	5	3
B8	EORA	↕	5	3
B9	ADCA	↕	5	3
BA	ORA	↕	5	3
BB	ADDA	↕	5	3
BC	CMPX	↕	7	3
BD	JSR	↕	8	3
BE	LDX	↕	6	3
BF	STX	EXTENDED	6	3
C0	SUBB	IMMED	2	2
C1	CMPB	IMMED	2	2

OP	MNEM	MODE	~	#
C2	SBCB	IMMED	2	2
C3	ADDD	↕	4	3
C4	ANDB	↕	2	2
C5	BITB	↕	2	2
C6	LDB	↕	2	2
C8	EORB	↕	2	2
C9	ADCB	↕	2	2
CA	ORB	↕	2	2
CB	ADDB	↕	2	2
CC	LDD	↕	3	3
CE	LDU	IMMED	3	3
D0	SUBB	DIRECT	4	2
D1	CMPB	↕	4	2
D2	SBCB	↕	4	2
D3	ADDD	↕	6	2
D4	ANDB	↕	4	2
D5	BITB	↕	4	2
D6	LDB	DIRECT	4	2
D7	STB	DIRECT	4	2
D8	EORB	↕	4	2
D9	ADCB	↕	4	2
DA	ORB	↕	4	2
DB	ADDB	↕	4	2
DC	LDD	↕	5	2
DD	STD	↕	5	2
DE	LDU	↕	5	2
DF	STU	DIRECT	5	2
E0	SUBB	INDEXED	4	2
E1	CMPB	↕	4	2
E2	SBCB	↕	4	2
E3	ADDD	↕	6	2
E4	ANDB	↕	4	2
E5	BITB	↕	4	2
E6	LDB	↕	4	2
E7	STB	↕	4	2
E8	EORB	INDEXED	4	2
E9	ADCB	INDEXED	4	2
EA	ORB	↕	4	2
EB	ADDB	↕	4	2
EC	LDD	↕	5	2
ED	STD	↕	5	2
EE	LDU	↕	5	2
EF	STU	INDEXED	5	2
F0	SUBB	EXTENDED	5	3
F1	CMPB	↕	5	3
F2	SBCB	↕	5	3
F3	ADDD	↕	7	3
F4	ANDB	↕	5	3
F5	BITB	↕	5	3
F6	LDB	↕	5	3
F7	STB	↕	5	3
F8	EORB	↕	5	3
F9	ADCB	↕	5	3
FA	ORB	EXTENDED	5	3

OP	MNEM	MODE	~	#
FB	ADDB	EXTENDED	5	3
FC	LDD	↕	6	3
FD	STD	↕	6	3
FE	LDU	↕	6	3
FF	STU	EXTENDED	6	3
1021	LBRN	RELATIVE	5	4
1022	LBHI	↕	5(6)	4
1023	LBLS	↕	5(6)	4
1024	LBHS/LBCC	↕	5(6)	4
1025	LBCS/LBLO	↕	5(6)	4
1026	LBNE	↕	5(6)	4
1027	LBEQ	↕	5(6)	4
1028	LBVC	↕	5(6)	4
1029	LBVS	↕	5(6)	4
102A	LBPL	↕	5(6)	4
102B	LBMI	↕	5(6)	4
102C	LBGE	↕	5(6)	4
102D	LBLT	RELATIVE	5(6)	4
102E	LBGT	RELATIVE	5(6)	4
102F	LBLE	RELATIVE	5(6)	4
103F	SWI/2	INHERENT	20	2
1083	CMPD	IMMED	5	4
108C	CMPY	↕	5	4
108E	LDY	IMMED	4	4
1093	CMPD	DIRECT	7	3
109C	CMPY	↕	7	3
109E	LDY	↕	6	3
109F	STY	DIRECT	6	3
10A3	CMPD	INDEXED	7	3
10AC	CMPY	↕	7	3
10AE	LDY	↕	6	3
10AF	STY	INDEXED	6	3
10B3	CMPD	EXTENDED	8	4
10BC	CMPY	↕	8	4
10BE	LDY	↕	7	4
10BF	STY	EXTENDED	7	4
10CE	LDS	IMMED	4	4
10DE	LDS	DIRECT	6	3
10DF	STS	DIRECT	6	3
10EE	LDS	INDEXED	6	3
10EF	STS	INDEXED	6	3
10FE	LDS	EXTENDED	7	4
10FF	STS	EXTENDED	7	4
113F	SWI/3	INHERENT	20	2
1183	CMPU	IMMED	5	4
118C	CMPS	IMMED	5	4
1193	CMPU	DIRECT	7	3
119C	CMPS	DIRECT	7	3
11A3	CMPU	INDEXED	7	3
11AC	CMPS	INDEXED	7	3
11B3	CMPU	EXTENDED	8	4
11BC	CMPS	EXTENDED	8	4

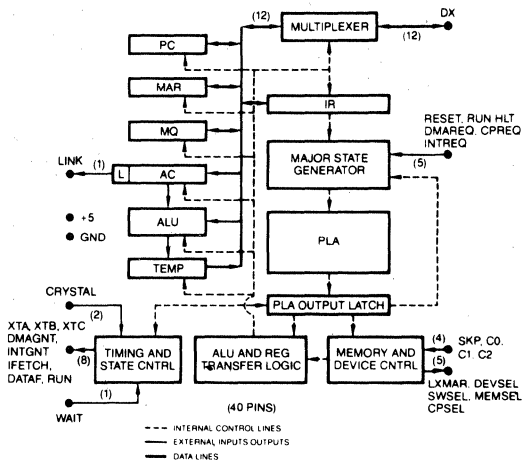
18. CPU INTERNAL ARCHITECTURE DRAWINGS

IN DRAWING NUMBER SEQUENCE

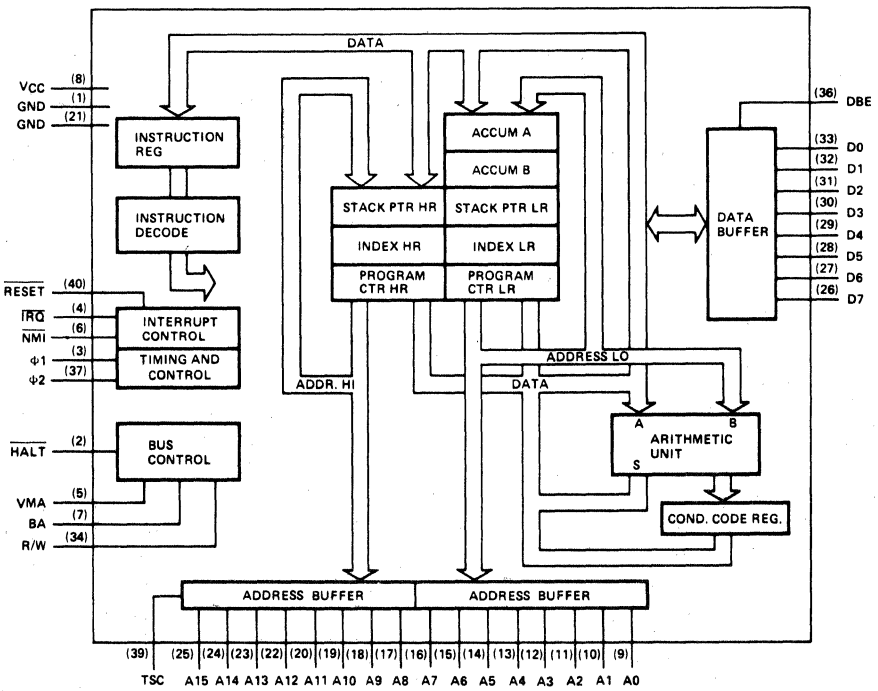
NOTES: These drawings are referenced in the Microprocessors section of this D.A.T.A.-BOOK in accordance with information supplied by the manufacturers.

Since representations may vary, the sources of information should be consulted before critical connections are made to the devices, or to obtain additional detail.

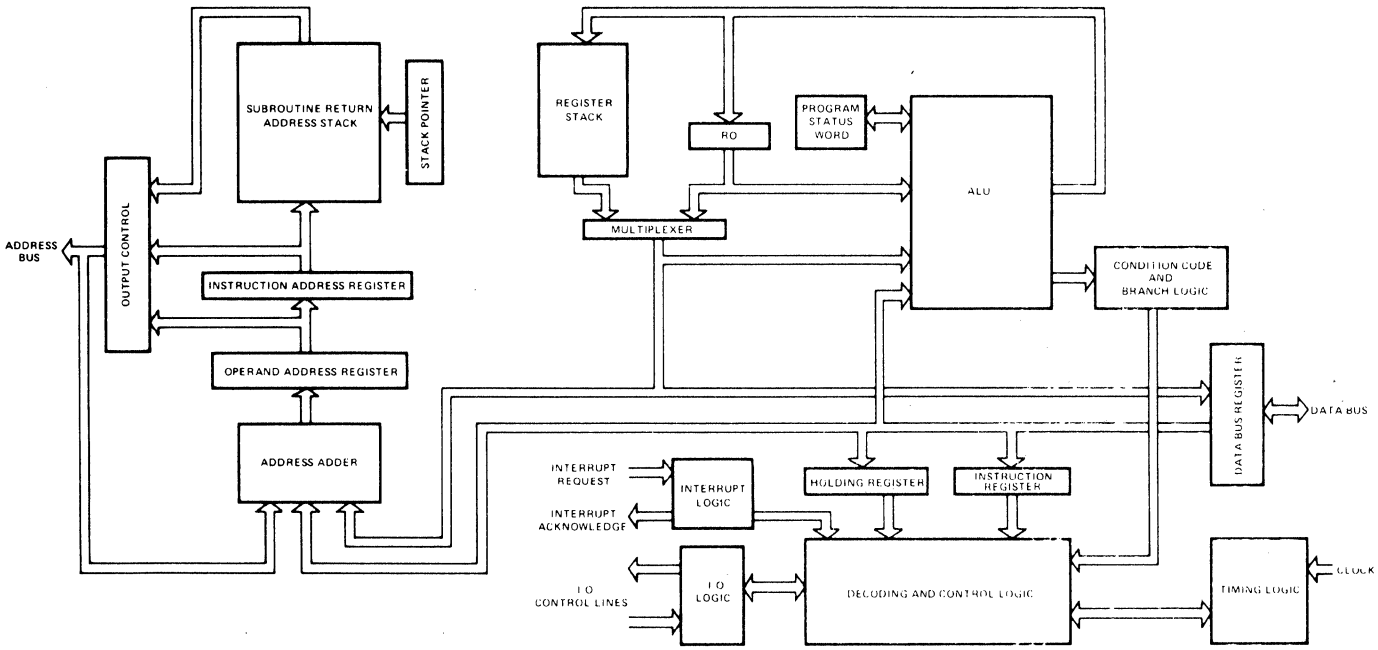
C1

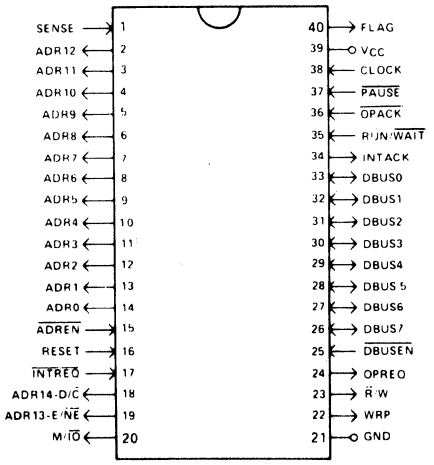


C2



C3



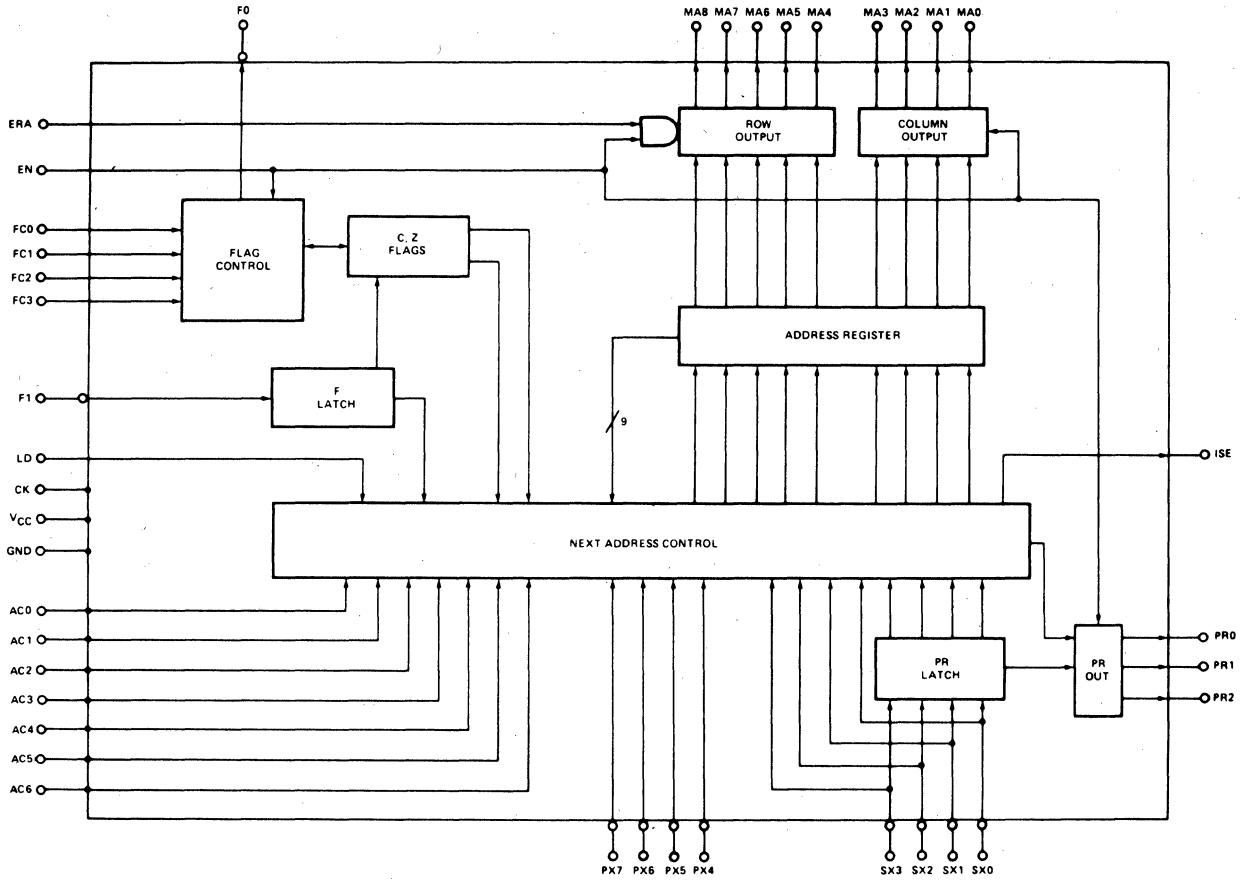


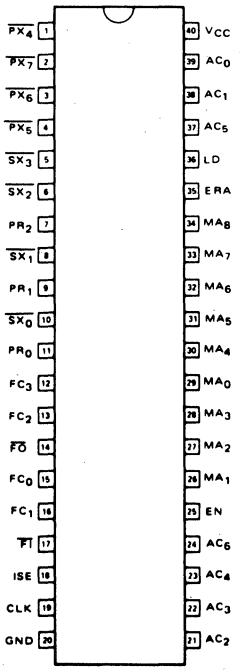
C3a

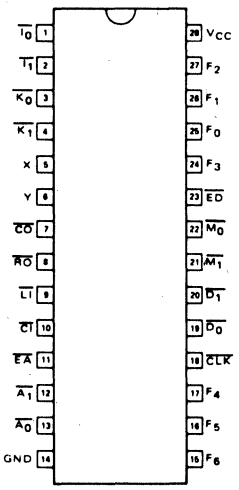
NOTE

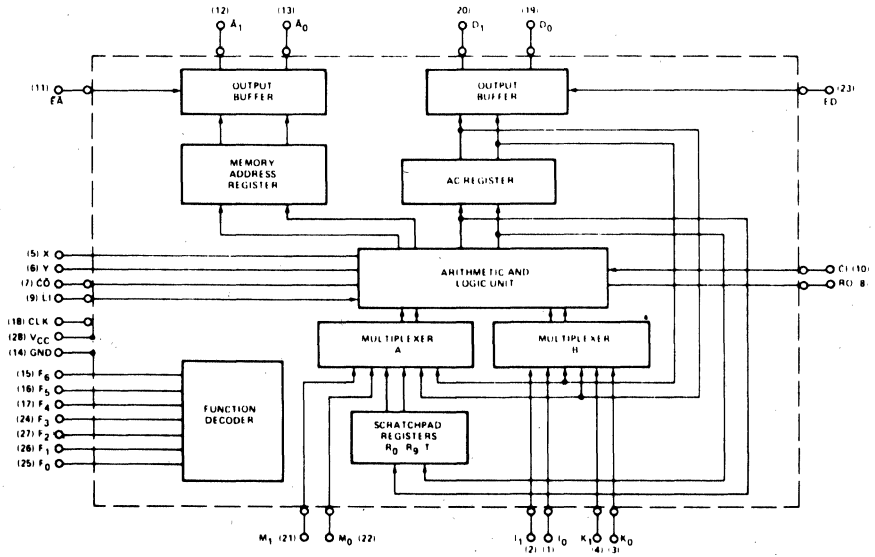
1. For 2650B and 2650B– 1 pin 15 is BEN and pin 25 is CYLAST.

C4


F0
MA8 MA7 MA6 MA5 MA4
MA3 MA2 MA1 MA0
ERA
EN
ROW OUTPUT
COLUMN OUTPUT
FC0
FC1
FC2
FC3
FLAG CONTROL
C, Z FLAGS
ADDRESS REGISTER
F1
F LATCH
/9
LD
CK
VCC
GND
ISE
NEXT ADDRESS CONTROL
AC0
AC1
AC2
AC3
AC4
AC5
AC6
PR LATCH
PR OUT
PR0
PR1
PR2
PX7 PX6 PX5 PX4
SX3 SX2 SX1 SX0


PX4 1
PX7 2
PX6 3
PX5 4
SX3 5
SX2 6
PR2 7
SX1 8
PR1 9
SX0 10
PR0 11
FC3 12
FC2 13
FO 14
FC0 15
FC1 16
F1 17
ISE 18
CLK 19
GND 20
40 VCC
39 AC0
38 AC1
37 AC5
36 LD
35 ERA
34 MA8
33 MA7
32 MA6
31 MA5
30 MA4
29 MA0
28 MA3
27 MA2
26 MA1
25 EN
24 AC6
23 AC4
22 AC3
21 AC2

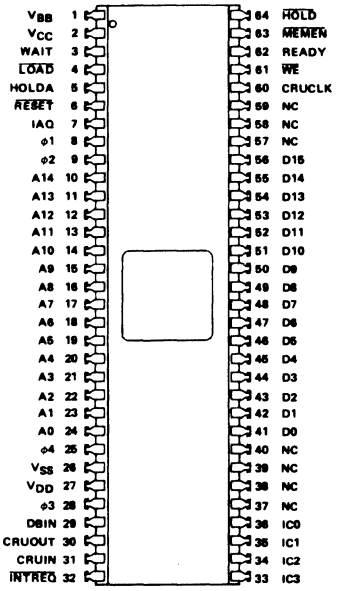

I0 1
I1 2
K0 3
K1 4
X 5
Y 6
CO 7
RO 8
LI 9
CI 10
EA 11
A1 12
A0 13
GND 14
28 VCC
27 F2
26 F1
25 F0
24 F3
23 ED
22 M0
21 M1
20 D1
19 D0
18 CLK
17 F4
16 F5
15 F6

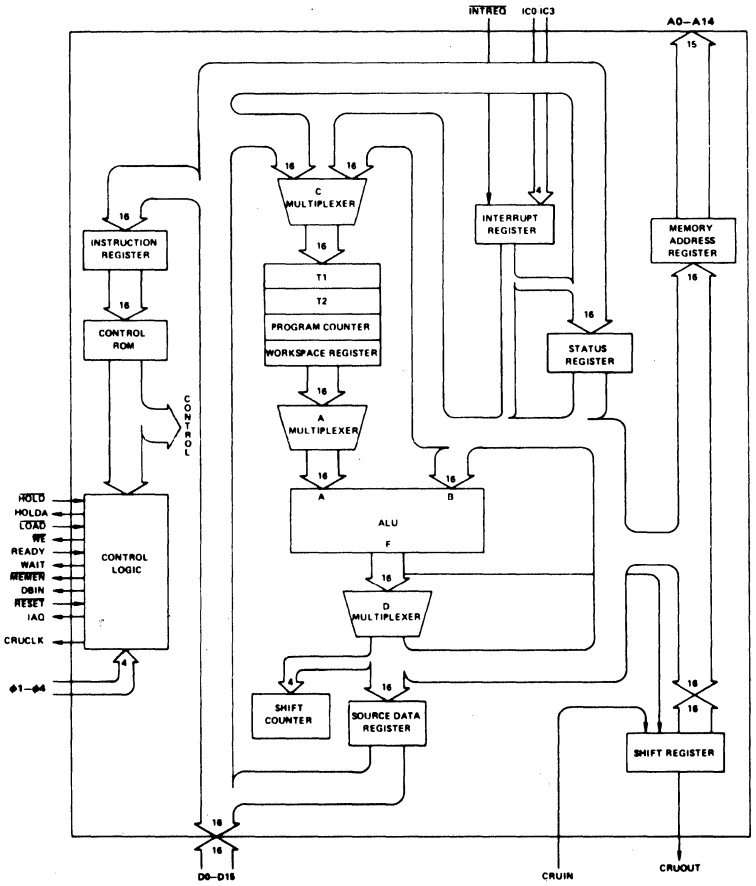

A1
A0
D1
D0
EA
OUTPUT BUFFER
OUTPUT BUFFER
ED
MEMORY ADDRESS REGISTER
AC REGISTER
X
Y
CO
LI
ARITHMETIC AND LOGIC UNIT
CI
RO
CLK
VCC
GND
MULTIPLEXER A
MULTIPLEXER B
F6
F5
F4
F3
F2
F1
F0
FUNCTION DECODER
SCRATCHPAD REGISTERS R0 R3
M1
M0
I1
I0
K1
K0

18. CPU INTERNAL ARCHITECTURE DRAWINGS

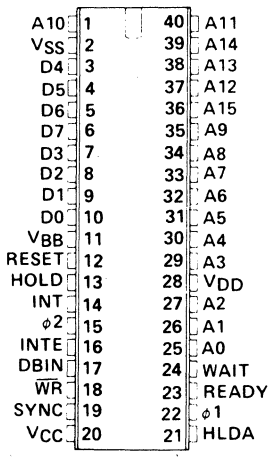
IN DRAWING NUMBER SEQUENCE

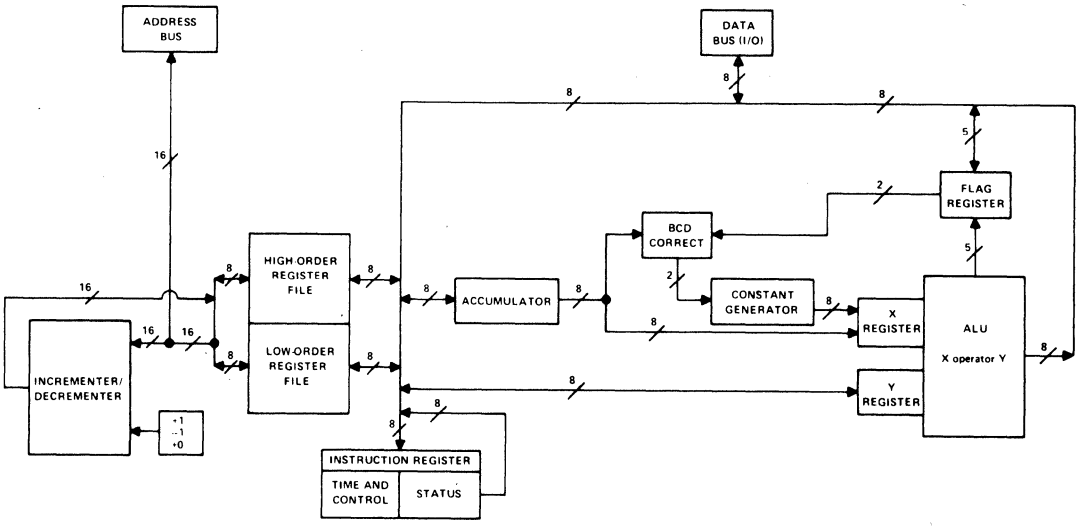
C5





C6

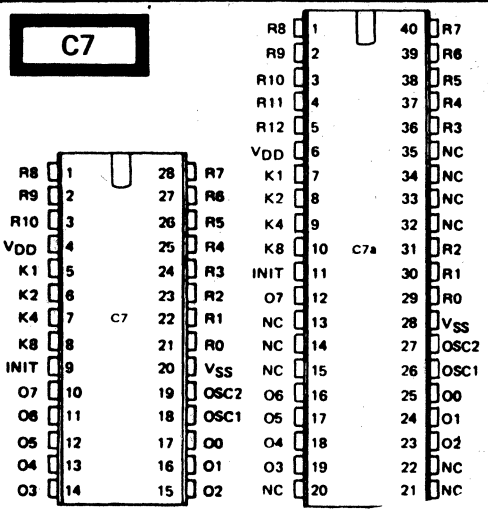


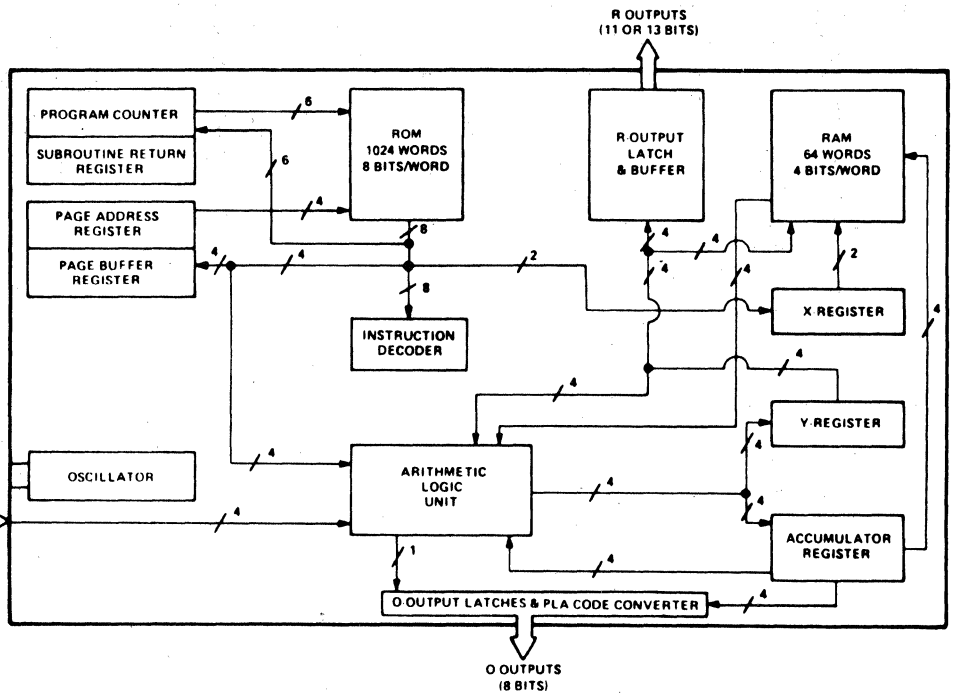


18. CPU INTERNAL ARCHITECTURE DRAWINGS

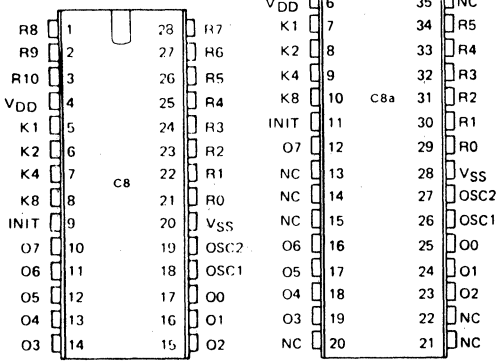
IN DRAWING NUMBER SEQUENCE

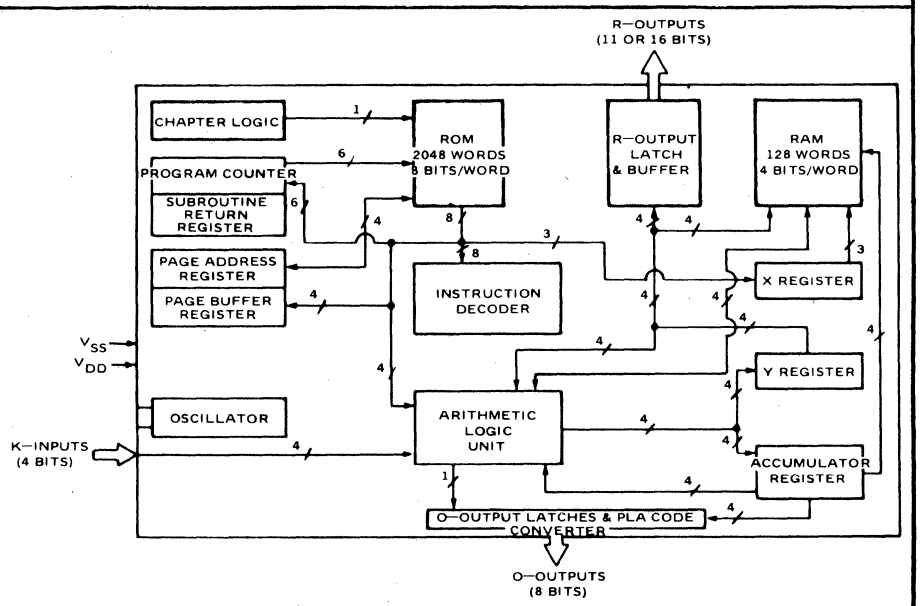
C7



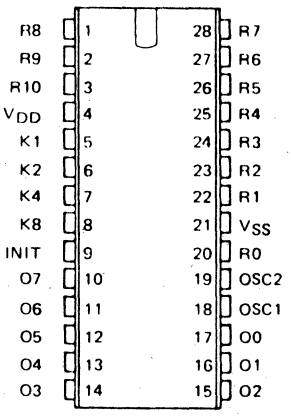


C8

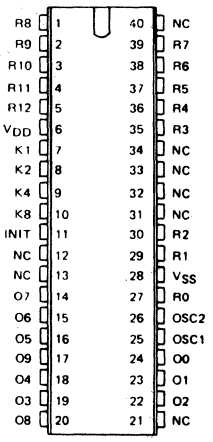




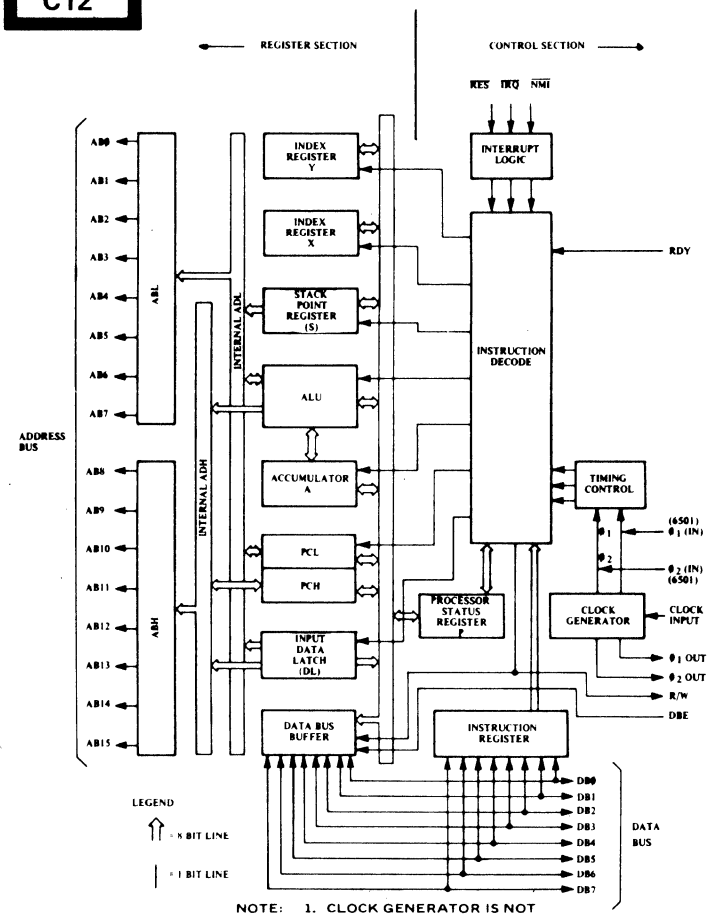
C9



C10

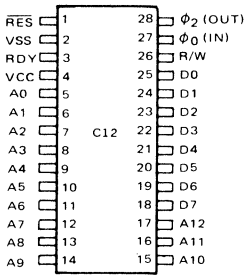


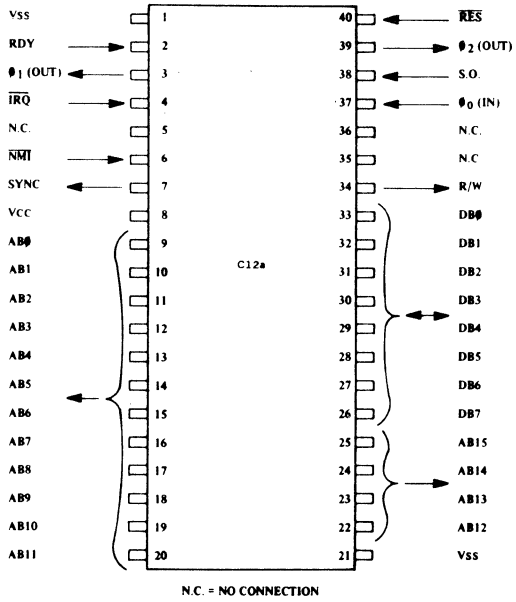
C12



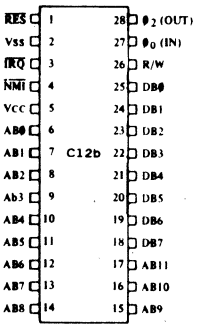
NOTE: 1. CLOCK GENERATOR IS NOT INCLUDED ON C12.

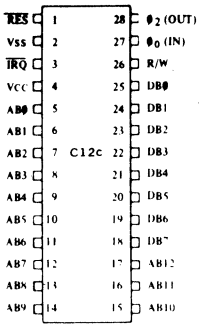
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE PRODUCTS.

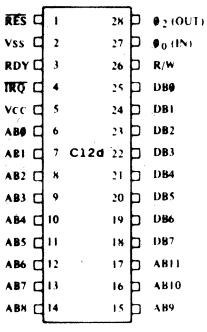


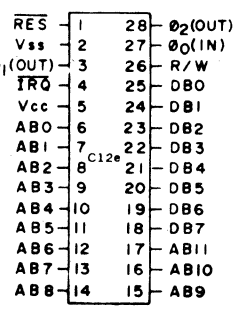


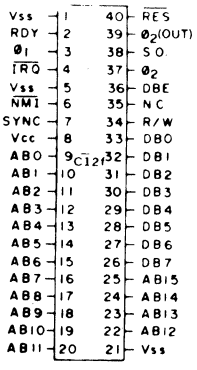
N.C. = NO CONNECTION

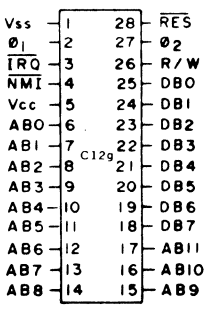


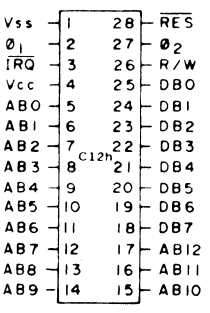


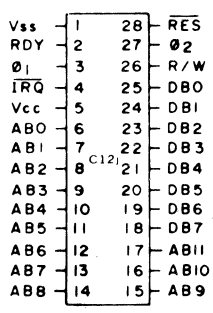




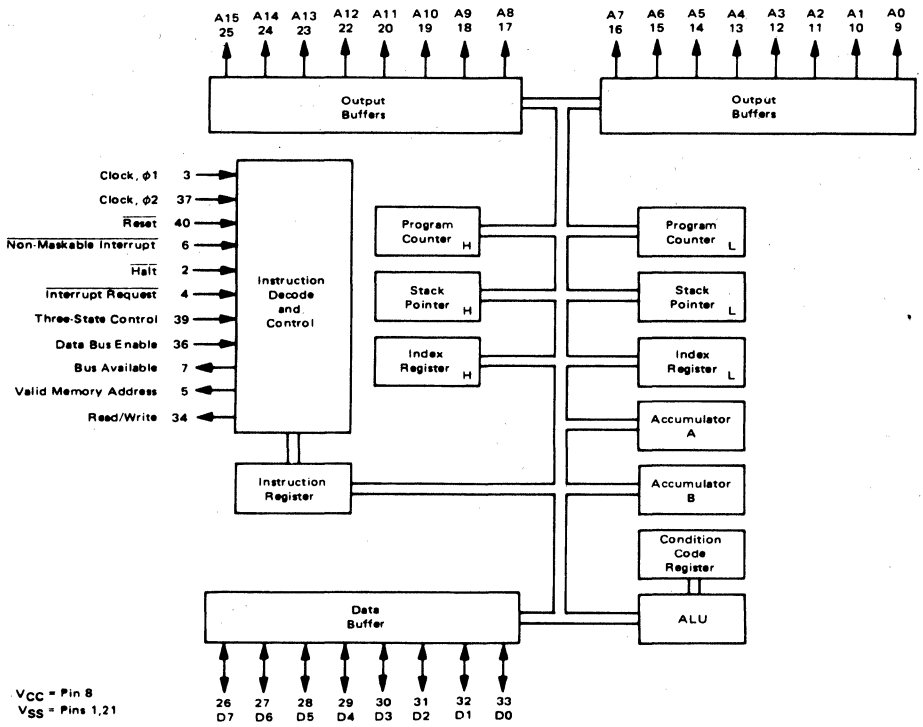




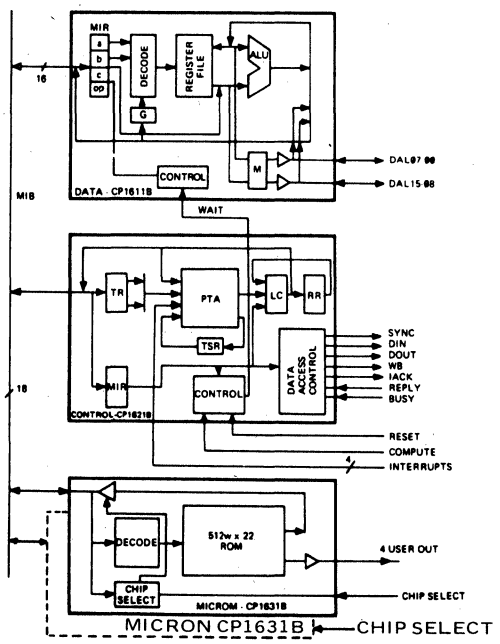




C13

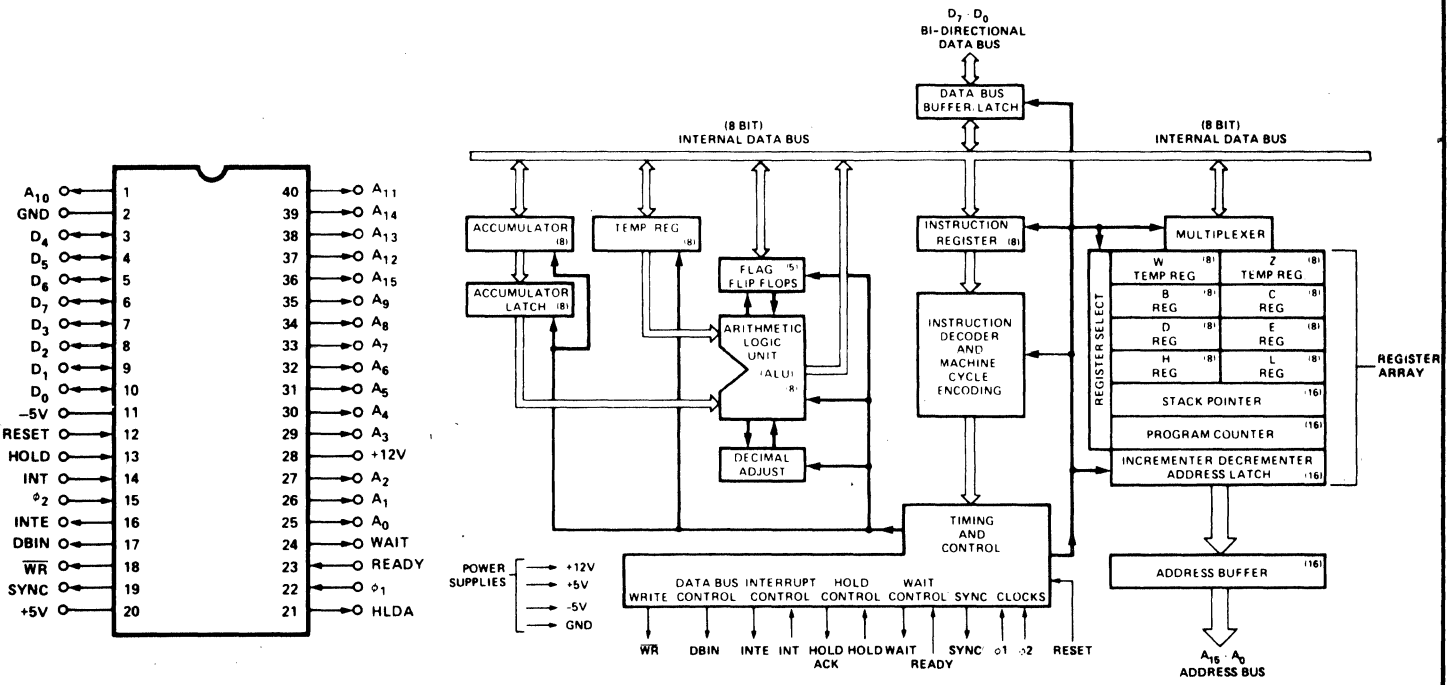


C14

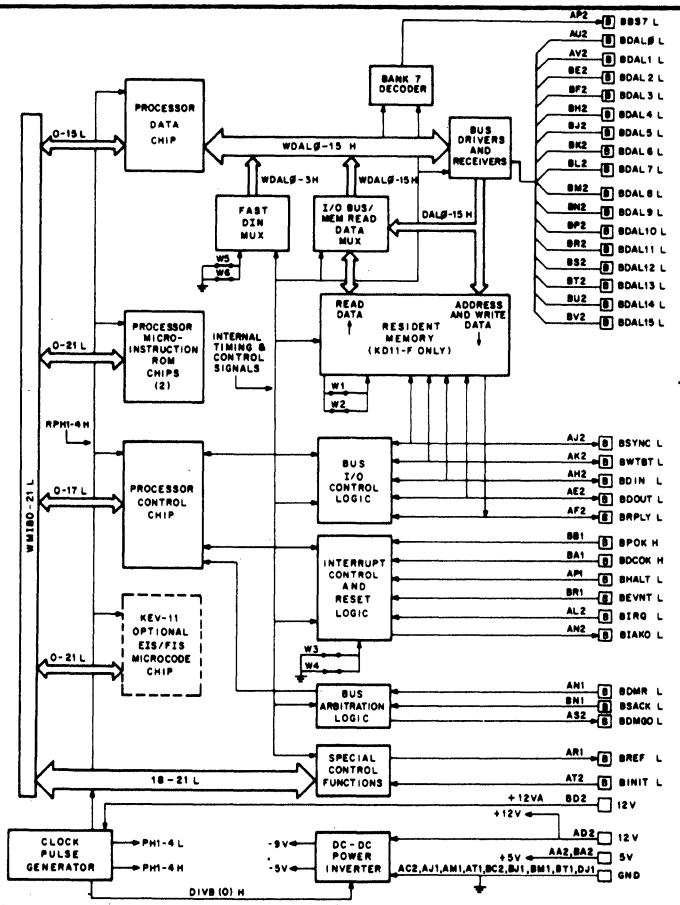


C14a — ADDITIONAL SHOWN IN DOTTED LINE.

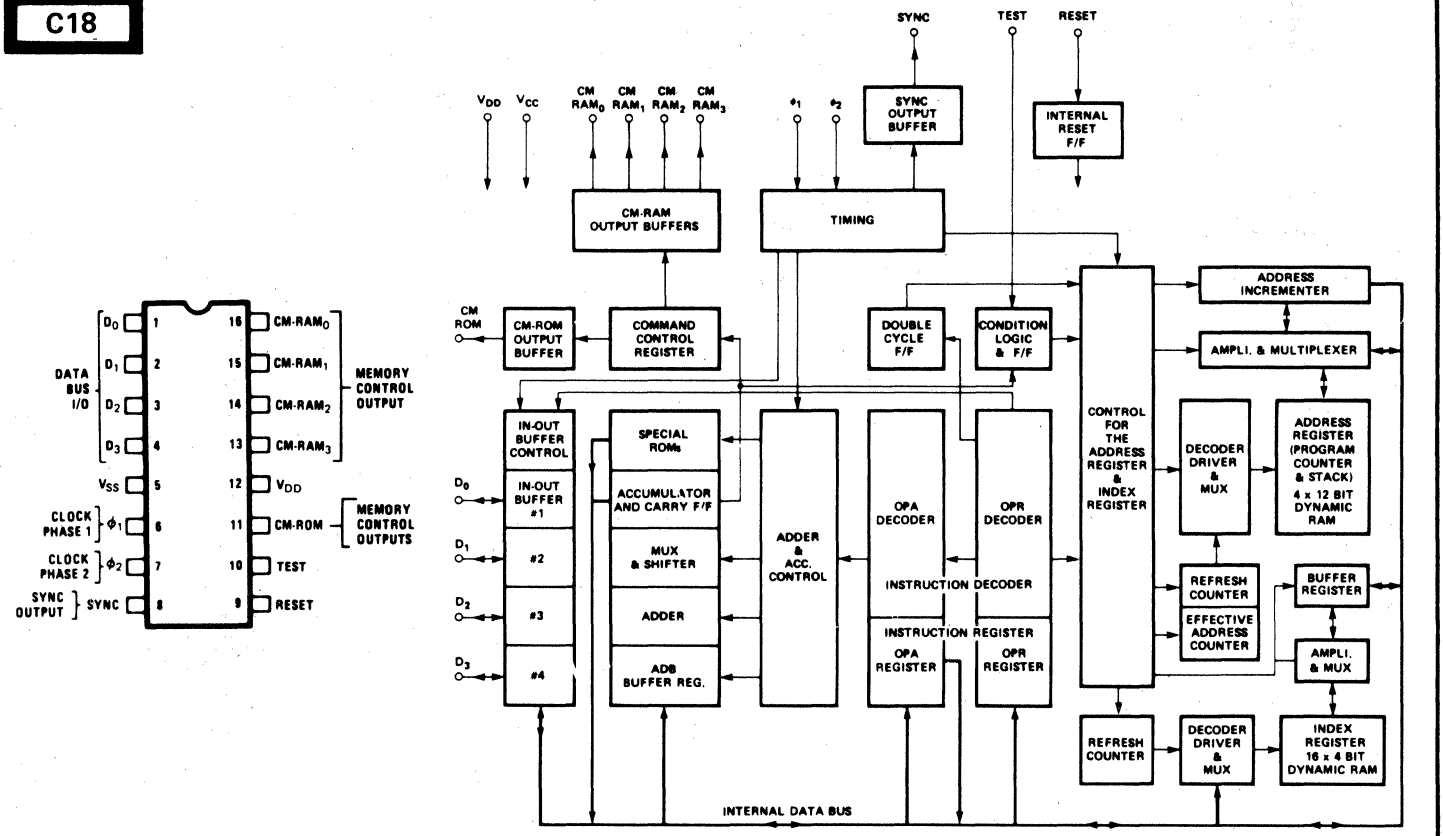
C15


A10 1
GND 2
D4 3
D5 4
D6 5
D7 6
D3 7
D2 8
D1 9
D0 10
-5V 11
RESET 12
HOLD 13
INT 14
Φ2 15
INTE 16
DBIN 17
WR 18
SYNC 19
+5V 20
40 A11
39 A14
38 A13
37 A12
36 A15
35 A9
34 A8
33 A7
32 A6
31 A5
30 A4
29 A3
28 +12V
27 A2
26 A1
25 A0
24 WAIT
23 READY
22 Φ1
21 HLDA
D7 - D0 BI-DIRECTIONAL DATA BUS
DATA BUS BUFFER LATCH
(8 BIT) INTERNAL DATA BUS
(8 BIT) INTERNAL DATA BUS
ACCUMULATOR (8)
TEMP REG (8)
ACCUMULATOR LATCH (8)
FLAG (5) FLIP FLOPS
ARITHMETIC LOGIC UNIT (ALU) (8)
DECIMAL ADJUST
INSTRUCTION REGISTER (8)
INSTRUCTION DECODER AND MACHINE CYCLE ENCODING
MULTIPLEXER
REGISTER SELECT
W TEMP REG (8)
Z TEMP REG (8)
B REG (8)
C REG (8)
D REG (8)
E REG (8)
H REG (8)
L REG (8)
STACK POINTER (16)
PROGRAM COUNTER (16)
INCREMENTER DECREMENTER ADDRESS LATCH (16)
REGISTER ARRAY
TIMING AND CONTROL
POWER SUPPLIES
+12V
+5V
-5V
GND
DATA BUS WRITE CONTROL
INTERRUPT CONTROL
HOLD CONTROL
WAIT CONTROL
SYNC
CLOCKS
ADDRESS BUFFER (16)
WR
DBIN
INTE
INT
HOLD ACK
HOLD
WAIT
READY
SYNC
Φ1
Φ2
RESET
A15 - A0 ADDRESS BUS

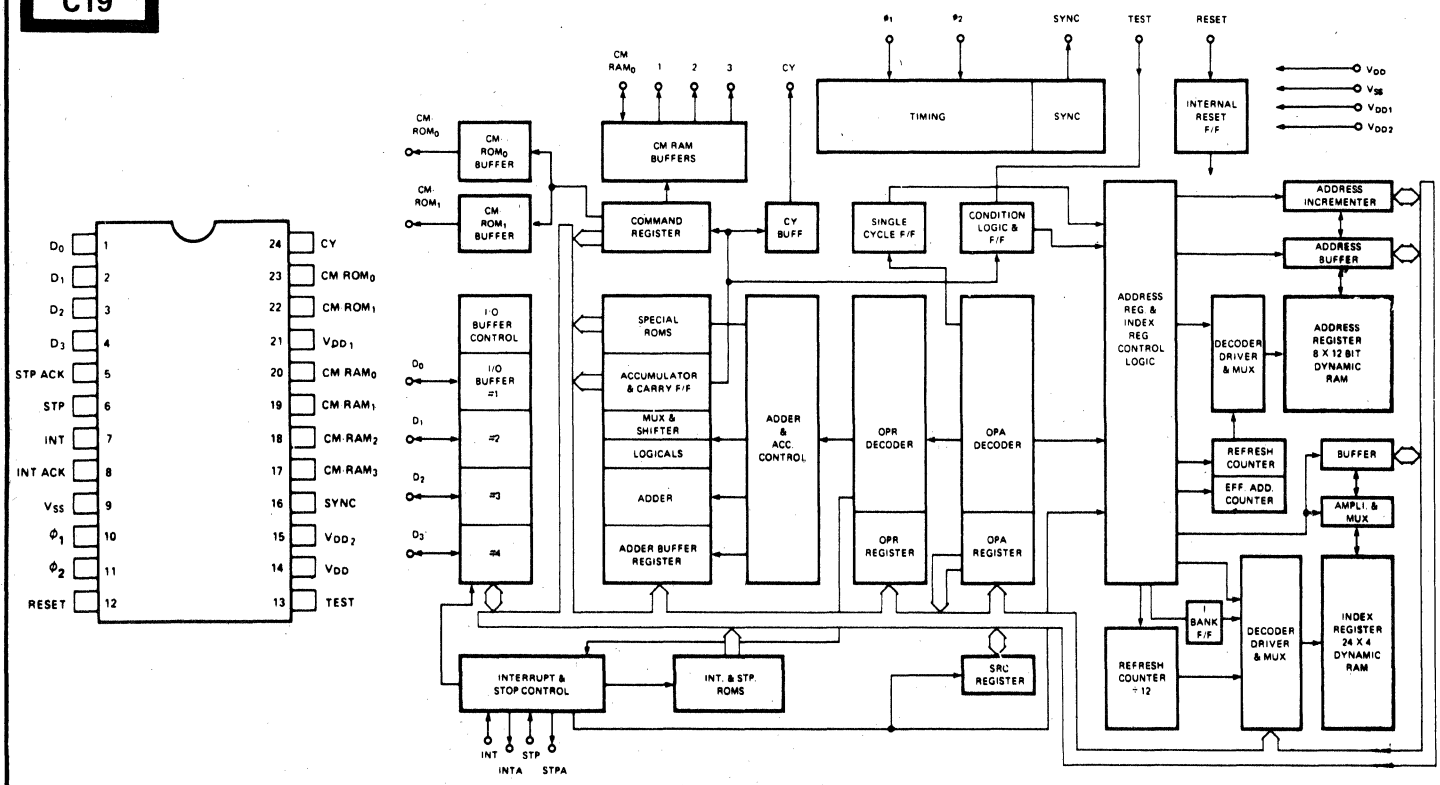
C17


BANK 7 DECODER
PROCESSOR DATA CHIP
0-15 L
WDAL0-15 H
BUS DRIVERS AND RECEIVERS
WDAL0-3H
WDAL0-15H
FAST DIN MUX
I/O BUS/ MEM READ DATA MUX
DAL0-15 H
W5
W6
READ DATA
ADDRESS AND WRITE DATA
RESIDENT MEMORY (KD11-F ONLY)
W1
W2
PROCESSOR MICRO-INSTRUCTION ROM CHIPS (2)
0-21 L
INTERNAL TIMING & CONTROL SIGNALS
RPH1-4H
PROCESSOR CONTROL CHIP
0-17 L
WM18Q-21 L
BUS I/O CONTROL LOGIC
INTERRUPT CONTROL AND RESET LOGIC
KEV-11 OPTIONAL EIS/FIS MICROCODE CHIP
0-21 L
W3
W4
BUS ARBITRATION LOGIC
SPECIAL CONTROL FUNCTIONS
18-21 L
+12VA
+12V
CLOCK PULSE GENERATOR
PH1-4 L
PH1-4 H
DIV8 (0) H
-9V
-5V
DC-DC POWER INVERTER
+5V
AC2,AJ1,AM1,AT1,BC2,BJ1,BM1,BT1,DJ1
AA2,BA2
AD2
AP2 BBS7 L
AU2 BDAL0 L
AV2 BDAL1 L
BE2 BDAL2 L
BF2 BDAL3 L
BH2 BDAL4 L
BJ2 BDAL5 L
BK2 BDAL6 L
BL2 BDAL7 L
BM2 BDAL8 L
BN2 BDAL9 L
BP2 BDAL10 L
BR2 BDAL11 L
BS2 BDAL12 L
BT2 BDAL13 L
BU2 BDAL14 L
BV2 BDAL15 L
AJ2 BSYNC L
AK2 BWTBT L
AH2 BDIN L
AE2 BDOUT L
AF2 BRPLY L
BB1 BPOK H
BA1 BDCOK H
AP1 BHALT L
BR1 BEVNT L
AL2 BIRQ L
AN2 BIAKO L
AN1 BDMR L
BN1 BSACK L
AS2 BDMGO L
AR1 BREF L
AT2 BINIT L
BD2 12V
AD2 12V
AA2,BA2 5V
AC2,AJ1,AM1,AT1,BC2,BJ1,BM1,BT1,DJ1 GND

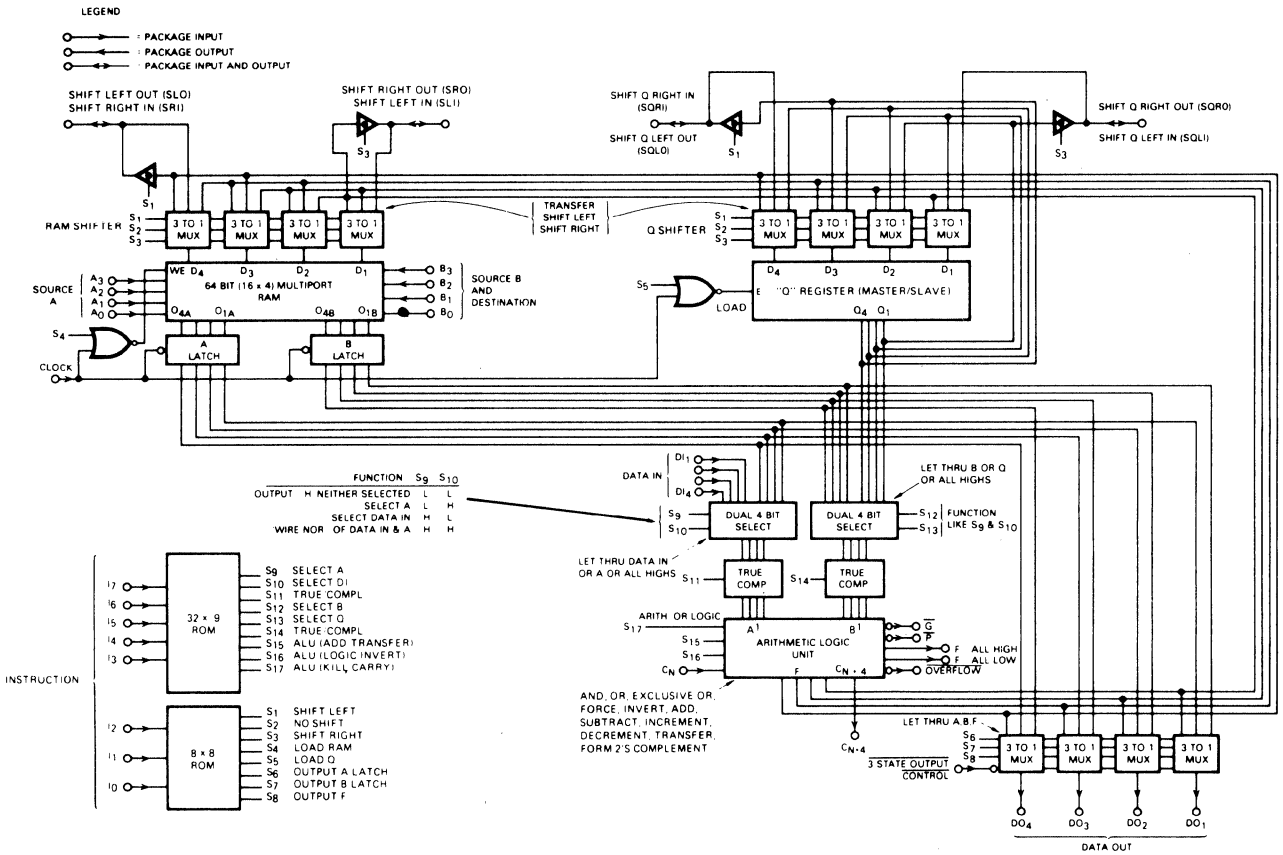
C18

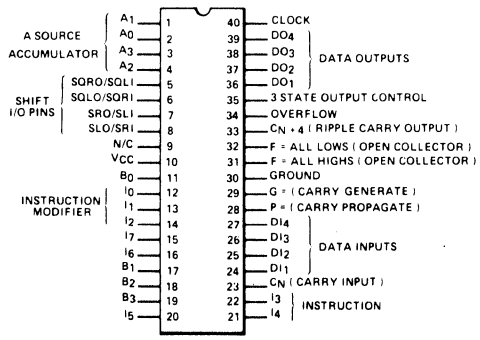

SYNC
TEST
RESET
VDD
VCC
CM RAM0
CM RAM1
CM RAM2
CM RAM3
φ1
φ2
SYNC OUTPUT BUFFER
INTERNAL RESET F/F
CM-RAM OUTPUT BUFFERS
TIMING
DATA BUS I/O
D0
D1
D2
D3
VSS
CLOCK PHASE 1
CLOCK PHASE 2
SYNC OUTPUT
CM-RAM0
CM-RAM1
CM-RAM2
CM-RAM3
MEMORY CONTROL OUTPUT
VDD
CM-ROM
MEMORY CONTROL OUTPUTS
TEST
RESET
CM ROM
CM-ROM OUTPUT BUFFER
COMMAND CONTROL REGISTER
DOUBLE CYCLE F/F
CONDITION LOGIC & F/F
ADDRESS INCREMENTER
AMPLI. & MULTIPLEXER
IN-OUT BUFFER CONTROL
IN-OUT BUFFER #1
#2
#3
#4
SPECIAL ROMs
ACCUMULATOR AND CARRY F/F
MUX & SHIFTER
ADDER
ADB BUFFER REG.
ADDER & ACC. CONTROL
OPA DECODER
INSTRUCTION DECODER
INSTRUCTION REGISTER
OPA REGISTER
OPR DECODER
OPR REGISTER
CONTROL FOR THE ADDRESS REGISTER & INDEX REGISTER
DECODER DRIVER & MUX
ADDRESS REGISTER (PROGRAM COUNTER & STACK) 4 x 12 BIT DYNAMIC RAM
REFRESH COUNTER
EFFECTIVE ADDRESS COUNTER
BUFFER REGISTER
AMPLI. & MUX
REFRESH COUNTER
DECODER DRIVER & MUX
INDEX REGISTER 16 x 4 BIT DYNAMIC RAM
INTERNAL DATA BUS

C19

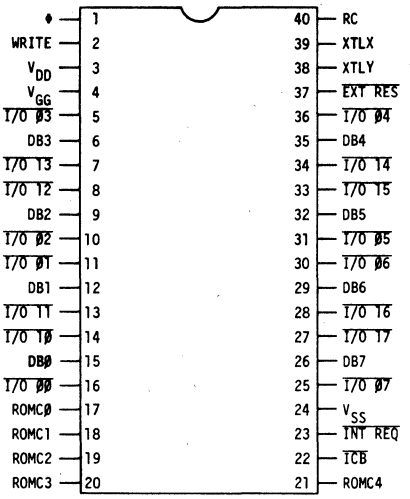

D0
D1
D2
D3
STP ACK
STP
INT
INT ACK
VSS
φ1
φ2
RESET
CY
CM ROM0
CM ROM1
VDD1
CM RAM0
CM RAM1
CM RAM2
CM RAM3
SYNC
VDD2
VDD
TEST
φ1
φ2
SYNC
TEST
RESET
CM RAM0
1
2
3
CY
TIMING
SYNC
INTERNAL RESET F/F
VDD
VSS
VDD1
VDD2
CM ROM0
CM ROM0 BUFFER
CM ROM1
CM ROM1 BUFFER
CM RAM BUFFERS
COMMAND REGISTER
CY BUFF
SINGLE CYCLE F/F
CONDITION LOGIC & F/F
ADDRESS INCREMENTER
ADDRESS BUFFER
I/O BUFFER CONTROL
I/O BUFFER #1
#2
#3
#4
SPECIAL ROMS
ACCUMULATOR & CARRY F/F
MUX & SHIFTER
LOGICALS
ADDER
ADDER BUFFER REGISTER
ADDER & ACC. CONTROL
OPR DECODER
OPR REGISTER
OPA DECODER
OPA REGISTER
ADDRESS REG. & INDEX REG CONTROL LOGIC
DECODER DRIVER & MUX
ADDRESS REGISTER 8 X 12 BIT DYNAMIC RAM
REFRESH COUNTER
EFF. ADD. COUNTER
BUFFER
AMPLI. & MUX
1 BANK F/F
DECODER DRIVER & MUX
INDEX REGISTER 24 X 4 DYNAMIC RAM
REFRESH COUNTER ÷12
INTERRUPT & STOP CONTROL
INT. & STP. ROMS
SRC REGISTER
INT
STP
INTA
STPA

C20


LEGEND
: PACKAGE INPUT
: PACKAGE OUTPUT
: PACKAGE INPUT AND OUTPUT
SHIFT LEFT OUT (SLO)
SHIFT RIGHT IN (SRI)
SHIFT RIGHT OUT (SRO)
SHIFT LEFT IN (SLI)
SHIFT Q RIGHT IN (SQRI)
SHIFT Q LEFT OUT (SQLO)
SHIFT Q RIGHT OUT (SQRO)
SHIFT Q LEFT IN (SQLI)
RAM SHIFTER
3 TO 1 MUX
TRANSFER
SHIFT LEFT
SHIFT RIGHT
Q SHIFTER
SOURCE A
64 BIT (16 x 4) MULTIPORT RAM
SOURCE B AND DESTINATION
A LATCH
B LATCH
CLOCK
LOAD
"Q" REGISTER (MASTER/SLAVE)
FUNCTION S9 S10
OUTPUT H NEITHER SELECTED L L
SELECT A L H
SELECT DATA IN H L
WIRE NOR OF DATA IN & A H H
DATA IN
DUAL 4 BIT SELECT
LET THRU B OR Q OR ALL HIGHS
FUNCTION LIKE S9 & S10
LET THRU DATA IN OR A OR ALL HIGHS
TRUE COMP
ARITH OR LOGIC
ARITHMETIC LOGIC UNIT
ALL HIGH
ALL LOW
OVERFLOW
AND, OR, EXCLUSIVE OR, FORCE, INVERT, ADD, SUBTRACT, INCREMENT, DECREMENT, TRANSFER, FORM 2'S COMPLEMENT
LET THRU A,B,F
3 STATE OUTPUT CONTROL
DATA OUT
INSTRUCTION
32 x 9 ROM
8 x 8 ROM
SELECT A
SELECT D
TRUE COMPL
SELECT B
SELECT Q
TRUE COMPL
ALU (ADD TRANSFER)
ALU (LOGIC INVERT)
ALU (KILL CARRY)
SHIFT LEFT
NO SHIFT
SHIFT RIGHT
LOAD RAM
LOAD Q
OUTPUT A LATCH
OUTPUT B LATCH
OUTPUT F

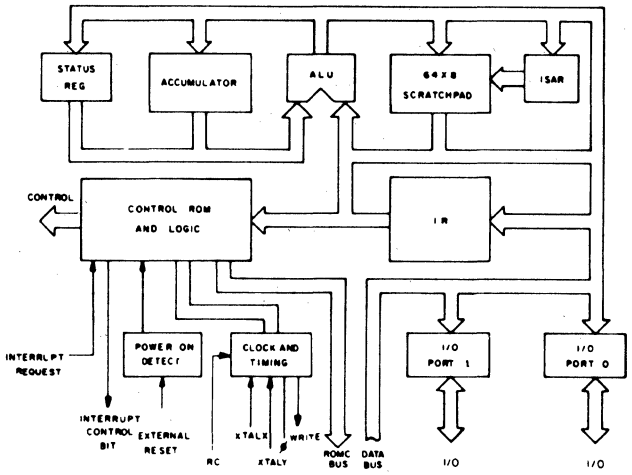

A SOURCE ACCUMULATOR
SHIFT I/O PINS
SQRO/SQLI
SQLO/SQRI
SRO/SLI
SLO/SRI
N/C
VCC
GROUND
INSTRUCTION MODIFIER
CLOCK
DO4
DO3
DO2
DO1
DATA OUTPUTS
3 STATE OUTPUT CONTROL
OVERFLOW
CN + 4 (RIPPLE CARRY OUTPUT)
F = ALL LOWS (OPEN COLLECTOR)
F = ALL HIGHS (OPEN COLLECTOR)
G = (CARRY GENERATE)
P = (CARRY PROPAGATE)
DI4
DI3
DI2
DI1
DATA INPUTS
CN (CARRY INPUT)
INSTRUCTION

C23

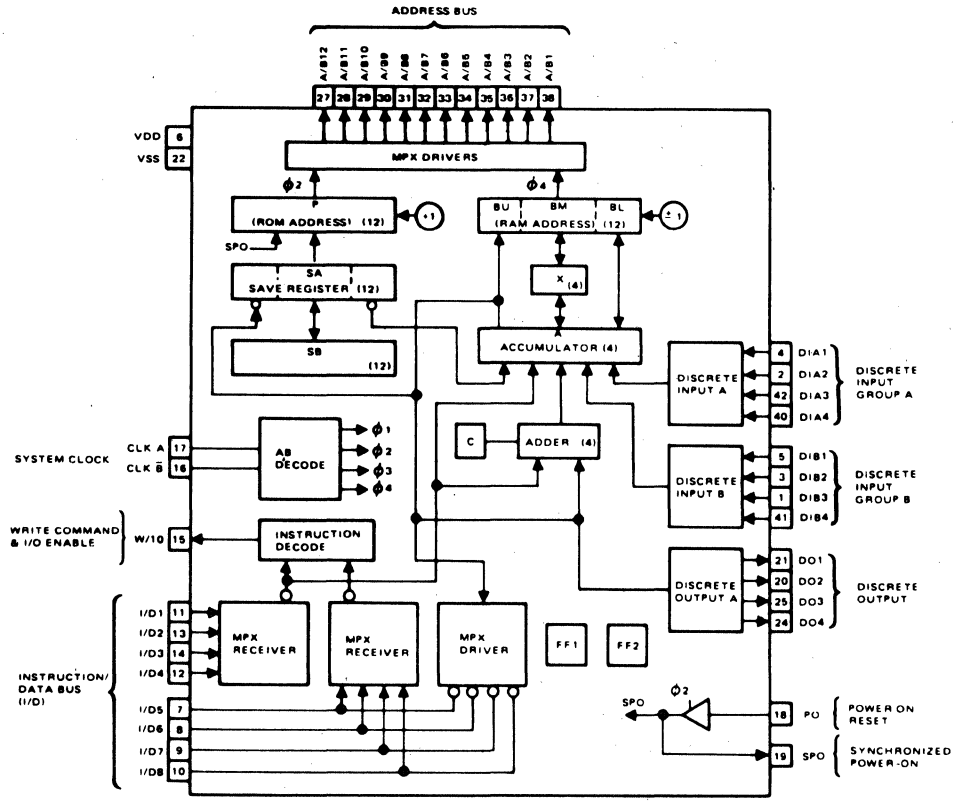


PIN NAME	DESCRIPTION	TYPE
DBØ - DB7	Data Bus Lines	Bidirectional
φ, WRITE	Clock Lines	Output
I/O ØØ - I/O Ø7	I/O Port Zero	Bidirectional
I/O 1Ø - I/O 17	I/O Port One	Bidirectional
RC	RC Network Pin	Input
ROMCØ - ROMC4	Control Lines	Output
EXT RES	External Reset	Input
INT REQ	Interrupt Request	Input
ICB	Interrupt Control Bit	Output
XTLX	Crystal Clock Line	Output
XTLY	External Clock Line	Input
V_{SS}, V_{DD}, V_{GG}	Power Lines	Input

C24



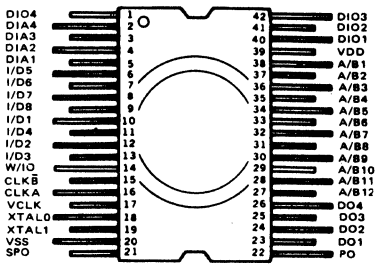
C26

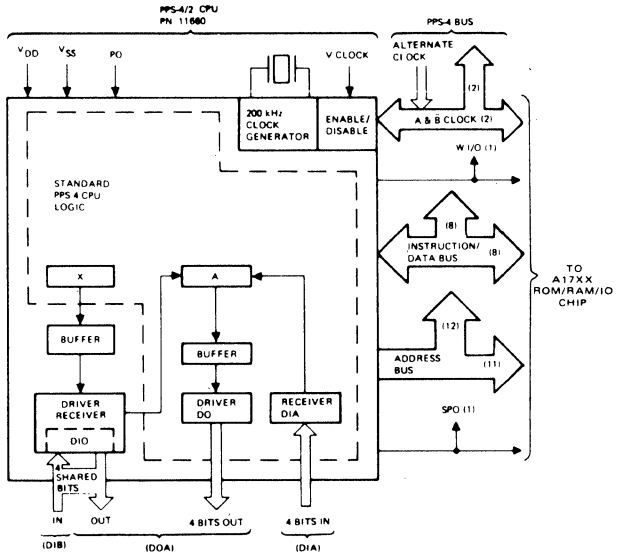


18. CPU INTERNAL ARCHITECTURE DRAWINGS

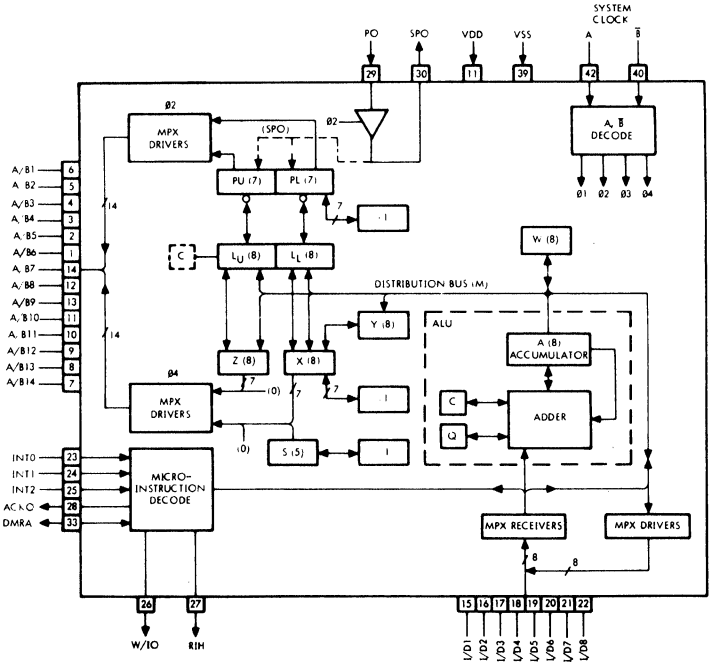
IN DRAWING NUMBER SEQUENCE

C27

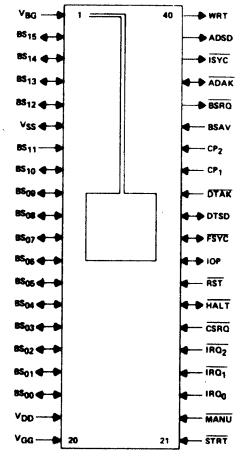


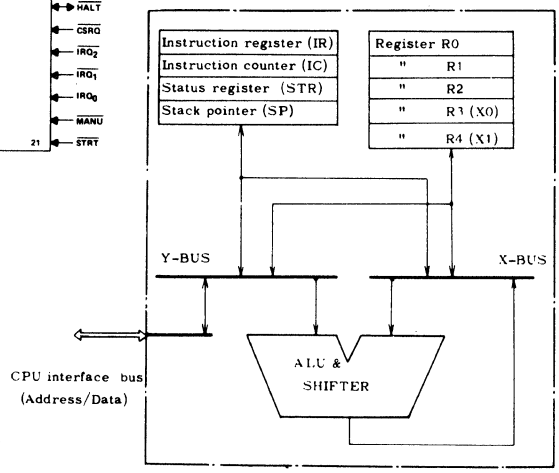


C28

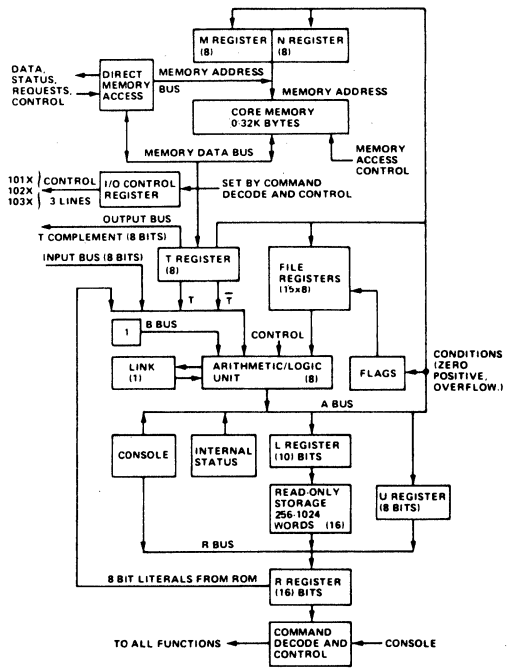


C32

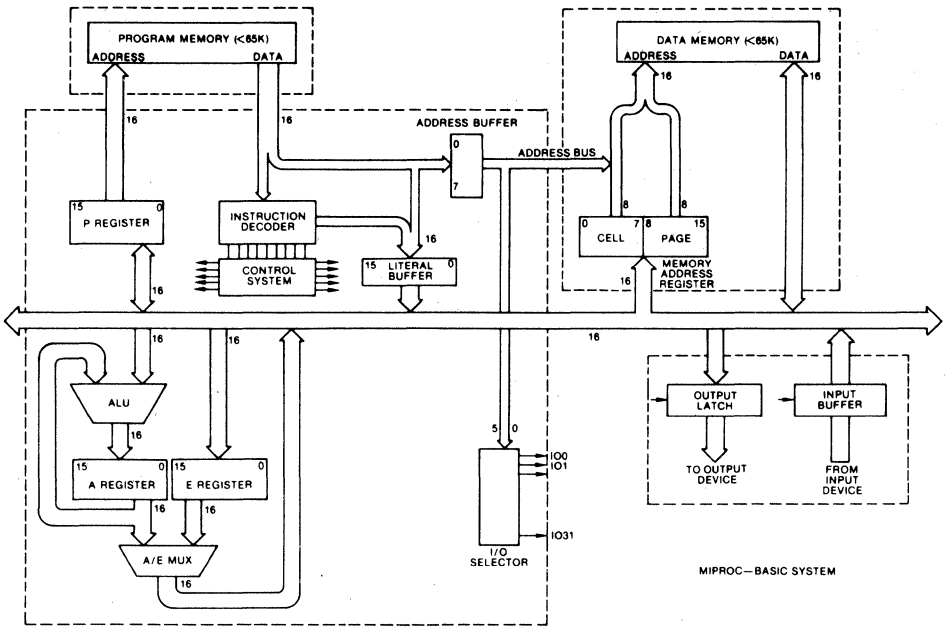


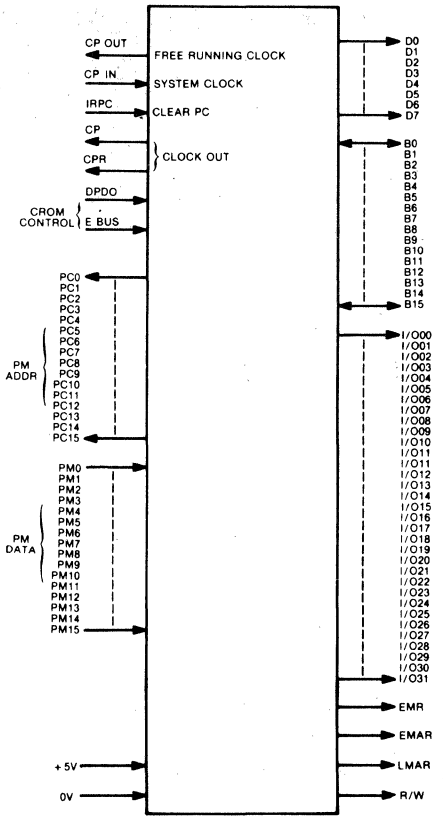


C33

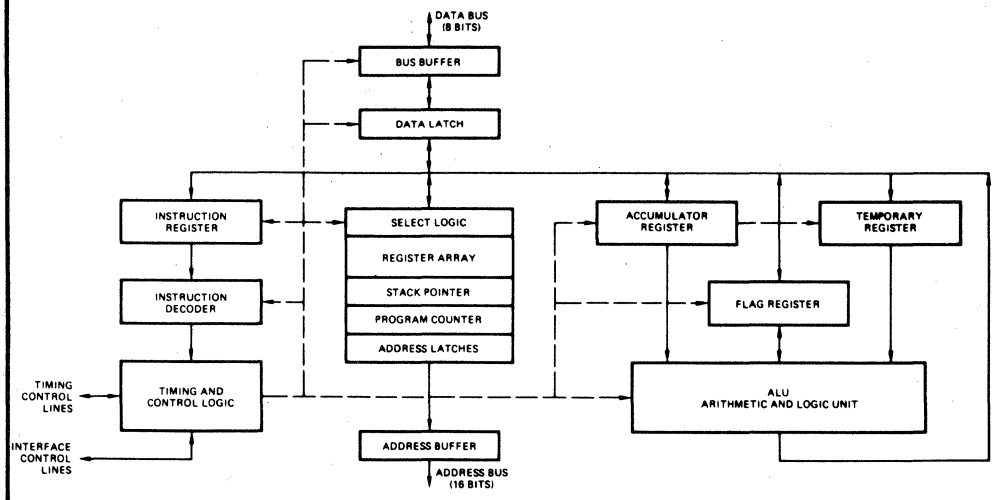


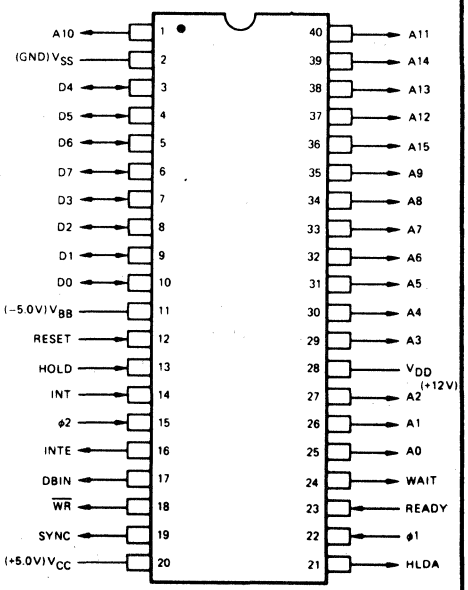
C34


PROGRAM MEMORY (<65K)
ADDRESS
DATA
DATA MEMORY (<65K)
ADDRESS
DATA
ADDRESS BUFFER
ADDRESS BUS
P REGISTER
INSTRUCTION DECODER
CONTROL SYSTEM
LITERAL BUFFER
CELL
PAGE
MEMORY ADDRESS REGISTER
ALU
A REGISTER
E REGISTER
A/E MUX
I/O SELECTOR
IO0
IO1
IO31
OUTPUT LATCH
INPUT BUFFER
TO OUTPUT DEVICE
FROM INPUT DEVICE
MIPROC—BASIC SYSTEM

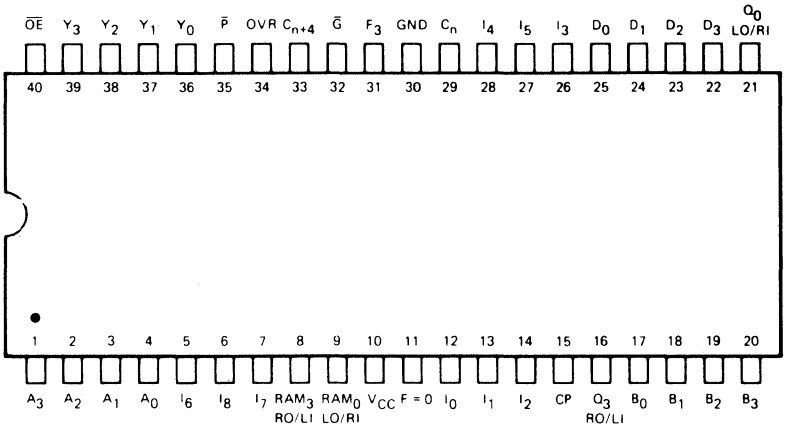

CP OUT
FREE RUNNING CLOCK
CP IN
SYSTEM CLOCK
IRPC
CLEAR PC
CP
CPR
CLOCK OUT
DPDO
CROM CONTROL
E BUS
PM ADDR
PM DATA
+5V
0V
EMR
EMAR
LMAR
R/W

C35

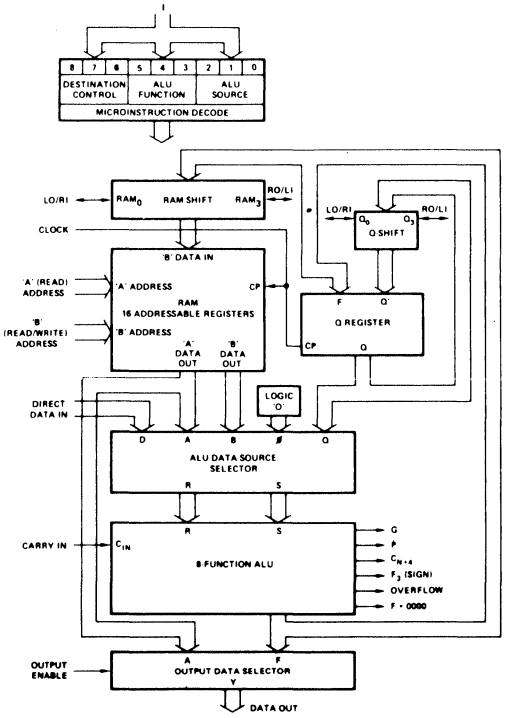

DATA BUS (8 BITS)
BUS BUFFER
DATA LATCH
INSTRUCTION REGISTER
INSTRUCTION DECODER
TIMING AND CONTROL LOGIC
TIMING CONTROL LINES
INTERFACE CONTROL LINES
SELECT LOGIC
REGISTER ARRAY
STACK POINTER
PROGRAM COUNTER
ADDRESS LATCHES
ADDRESS BUFFER
ADDRESS BUS (16 BITS)
ACCUMULATOR REGISTER
TEMPORARY REGISTER
FLAG REGISTER
ALU
ARITHMETIC AND LOGIC UNIT


A10
(GND) VSS
D4
D5
D6
D7
D3
D2
D1
D0
(-5.0V) VBB
RESET
HOLD
INT
φ2
INTE
DBIN
WR
SYNC
(+5.0V) VCC
A11
A14
A13
A12
A15
A9
A8
A7
A6
A5
A4
A3
VDD (+12V)
A2
A1
A0
WAIT
READY
φ1
HLDA

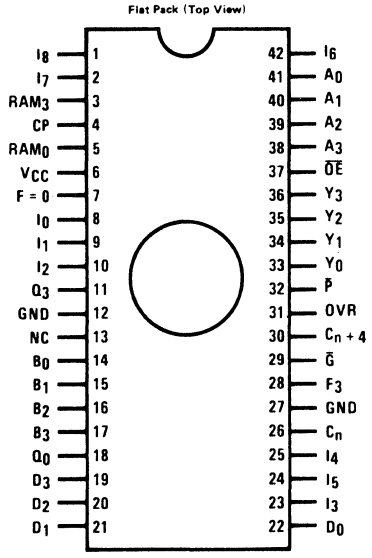
C36



C36



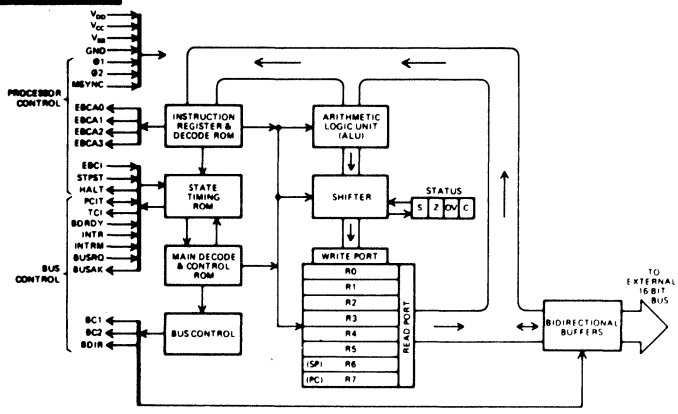
Flat Pack (Top View)

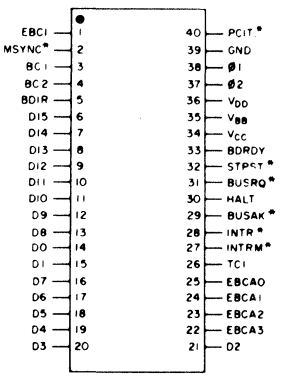


NOTE: BOTH GROUNDS (PINS 12 and 27) MUST BE CONNECTED.

C36a

C37

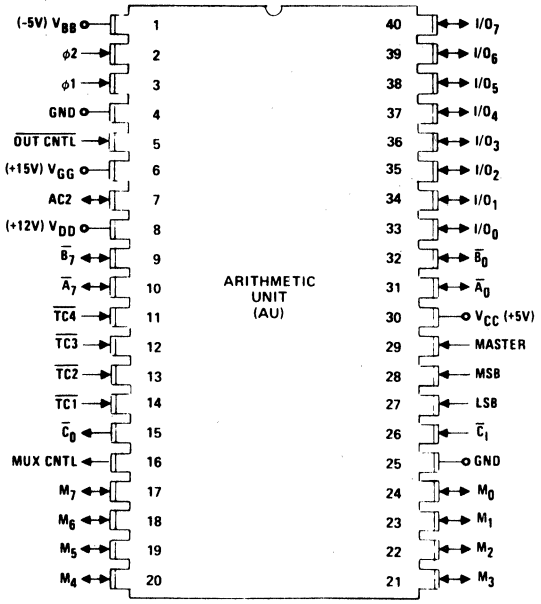




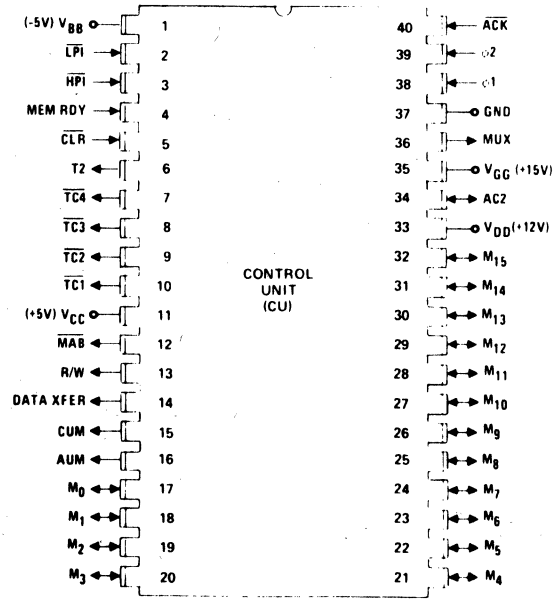
*ACTIVE LOW LEVEL

C38

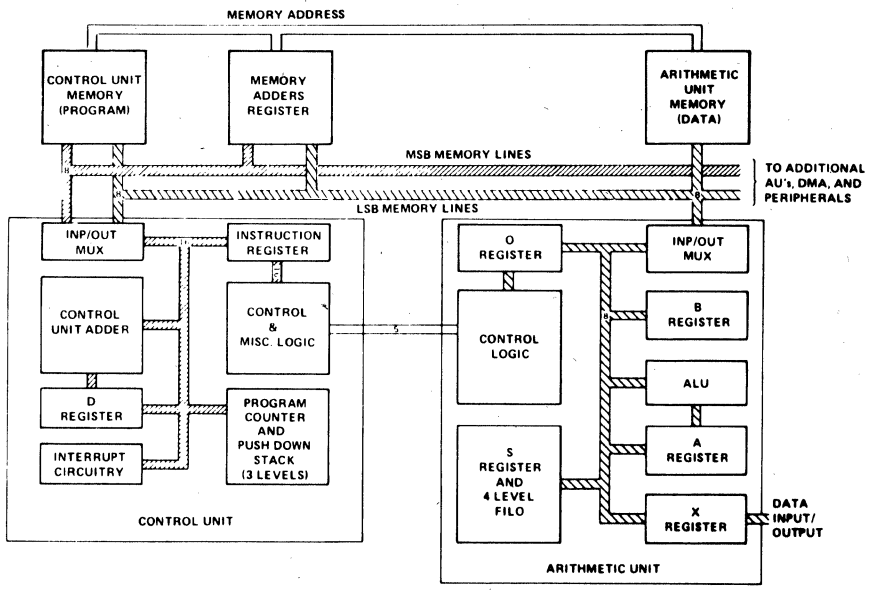
ARITHMETIC UNIT



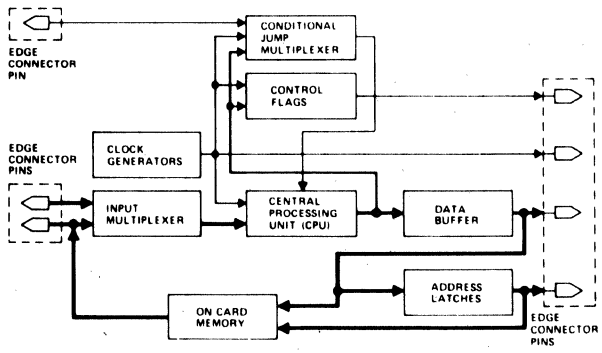
CONTROL UNIT



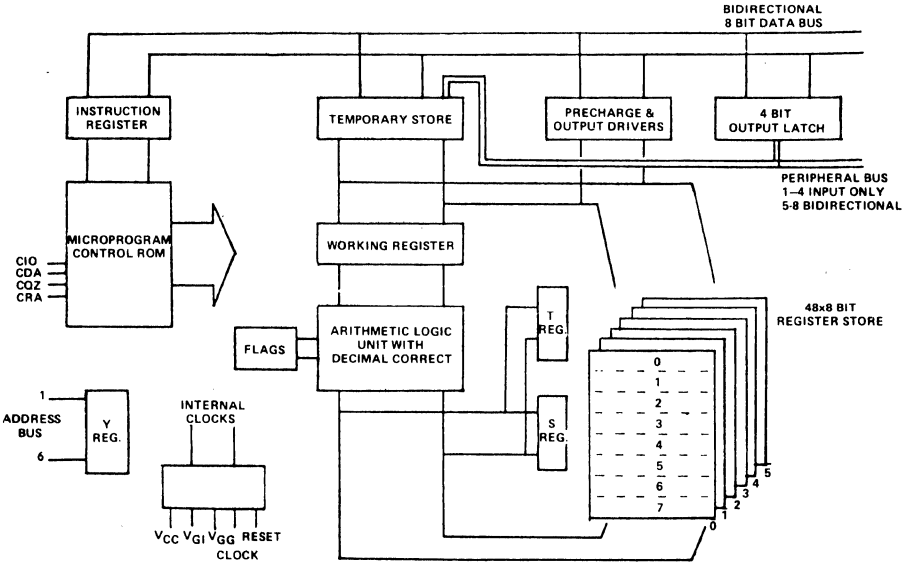
MICROCOMPUTER ARCHITECTURE



C41



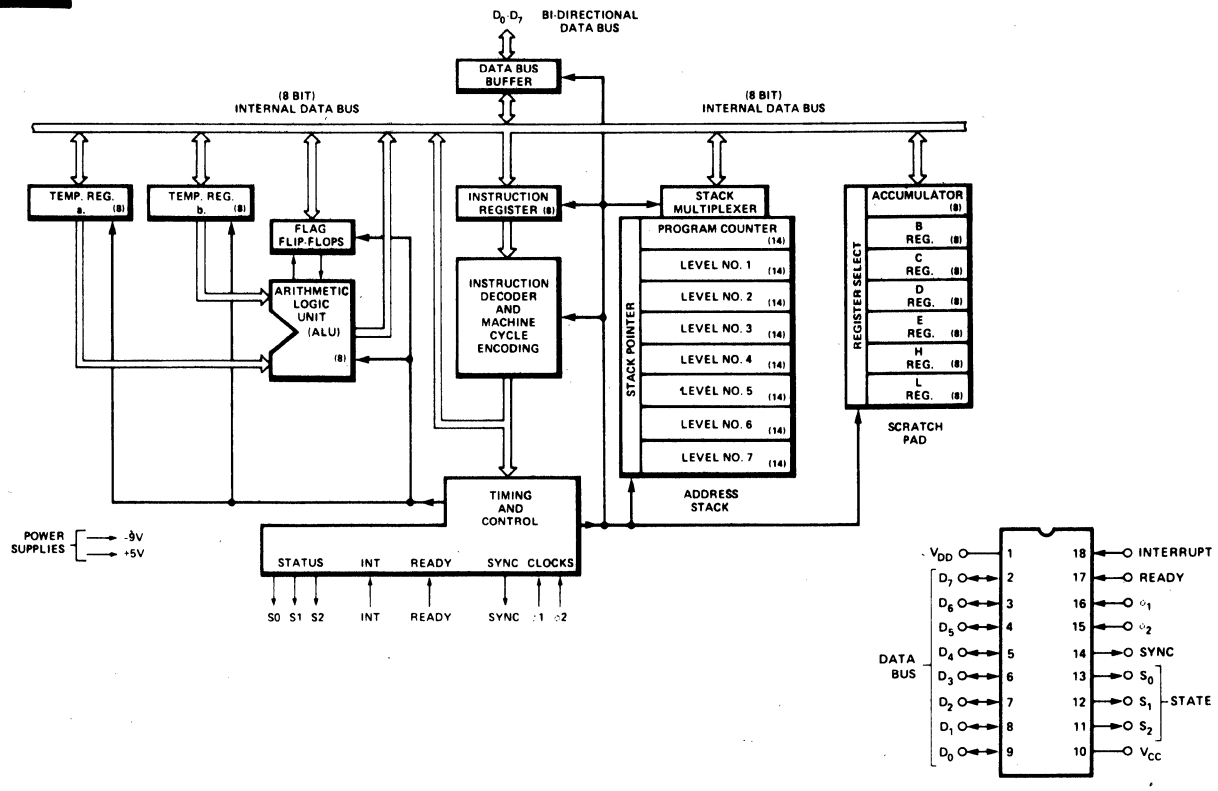
C42



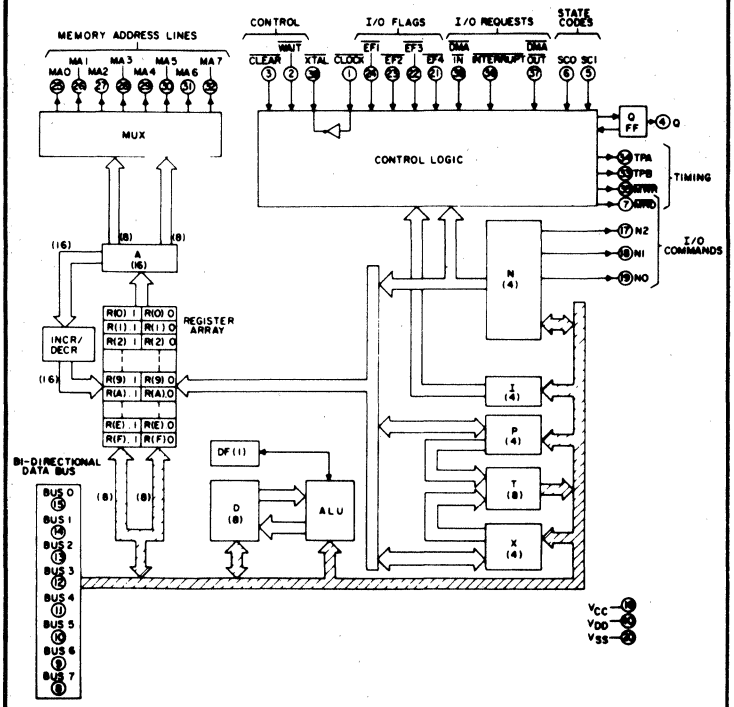
PIN CONNECTIONS

1	Vcc	22	Address Bus 1
2	Power on Reset	23	" " 2
3	Clock	24	" " 3
4	Not Used	25	" " 4
5	" "	26	" " 5
6	Data Bus 8	27	" " 6
7	" " 7	28	Not Used
8	" " 6	29	" "
9	" " 5	30	" "
10	" " 4	31	" "
11	" " 3	32	" "
12	" " 2	33	" "
13	" " 1	34	" "
14	Peripheral Bus 8	35	CIO
15	" " 7	36	CDA
16	" " 6	37	CQZ
17	" " 5	38	CRA
18	" " 4	39	Vgg
19	" " 3	40	Vgi
20	" " 2		
21	" " 1		

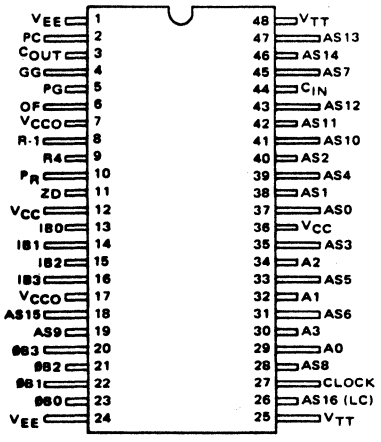
C43

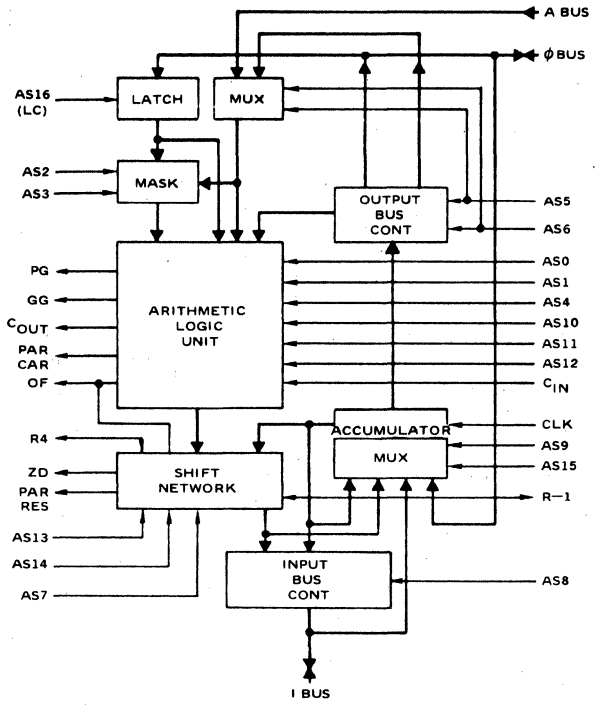


C44

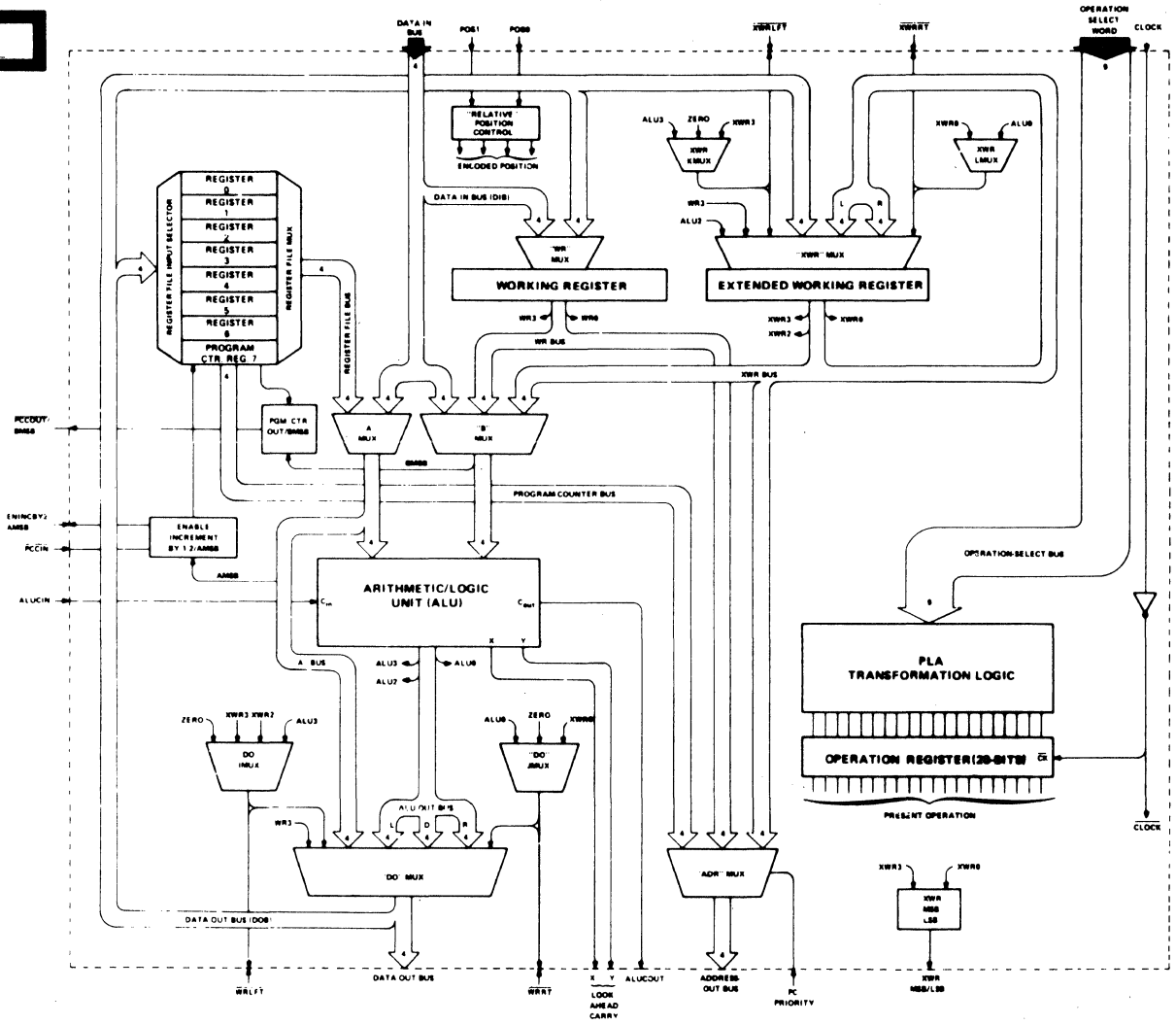

MEMORY ADDRESS LINES
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7
CONTROL
WAIT
CLEAR XTAL
I/O FLAGS
EF1 EF2 EF3 EF4
CLOCK
I/O REQUESTS
DMA IN DMA OUT
INTERRUPT
STATE CODES
SC0 SC1
MUX
CONTROL LOGIC
Q FF
TPA
TPB
SYNC
TIMING
N2
N1
N0
I/O COMMANDS
A (16)
INCR/ DECR
REGISTER ARRAY
N (4)
I (4)
P (4)
T (8)
X (4)
DF (1)
D (8)
ALU
BI-DIRECTIONAL DATA BUS
BUS 0
BUS 1
BUS 2
BUS 3
BUS 4
BUS 5
BUS 6
BUS 7
VCC
VDD
VSS

C46


VEE 1
PC 2
COUT 3
GG 4
PG 5
OF 6
VCCO 7
R-1 8
R4 9
PR 10
ZD 11
VCC 12
I80 13
I81 14
I82 15
I83 16
VCCO 17
AS15 18
AS9 19
$83 20
$82 21
$81 22
$80 23
VEE 24
48 VTT
47 AS13
46 AS14
45 AS7
44 CIN
43 AS12
42 AS11
41 AS10
40 AS2
39 AS4
38 AS1
37 AS0
36 VCC
35 AS3
34 A2
33 AS5
32 A1
31 AS6
30 A3
29 A0
28 AS8
27 CLOCK
26 AS16 (LC)
25 VTT


A BUS
φ BUS
AS16 (LC)
LATCH
MUX
AS2
AS3
MASK
OUTPUT BUS CONT
AS5
AS6
PG
GG
COUT
PAR CAR
OF
ARITHMETIC LOGIC UNIT
AS0
AS1
AS4
AS10
AS11
AS12
CIN
R4
ZD
PAR RES
SHIFT NETWORK
ACCUMULATOR
MUX
CLK
AS9
AS15
R-1
AS13
AS14
AS7
INPUT BUS CONT
AS8
I BUS

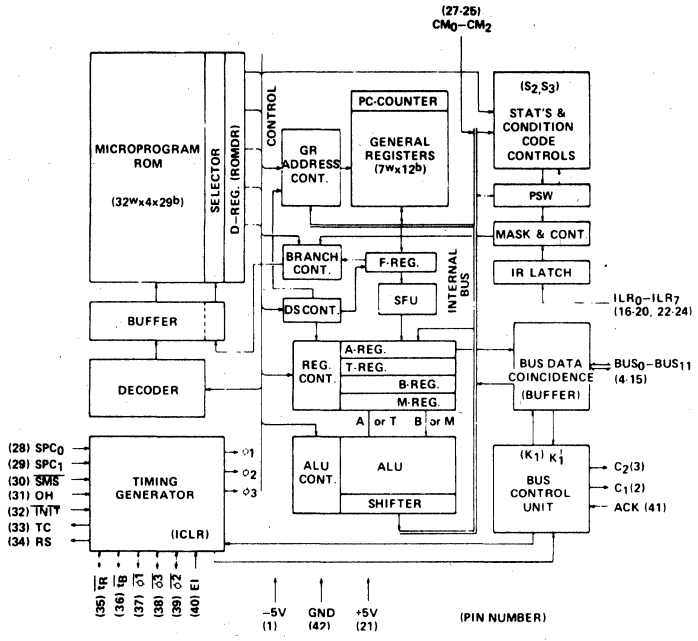
C47

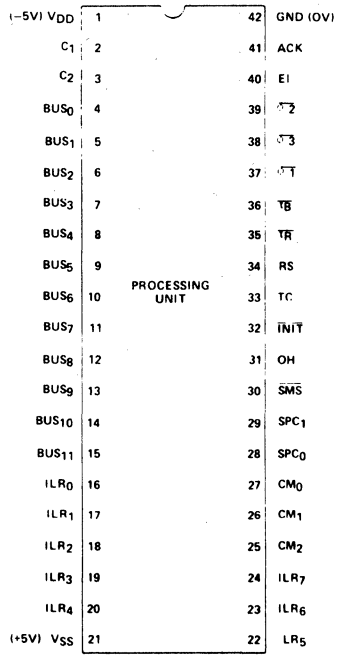


PIN NUMBER	PIN NAME
1	D1
2	D0
3	S2
4	S1
5	S0
6	$\overline{\text{XWRLFT}}$
7	$\overline{\text{XWRRT}}$
8	XWR MSB/LSB
9	$\overline{\text{WRRT}}$
10	$\overline{\text{WRLFT}}$
11	ALUCIN
12	DOB0
13	DOB1
14	DOB2
15	DOB3
16	DIB3
17	DIB2
24	DIB1
25	DIB0

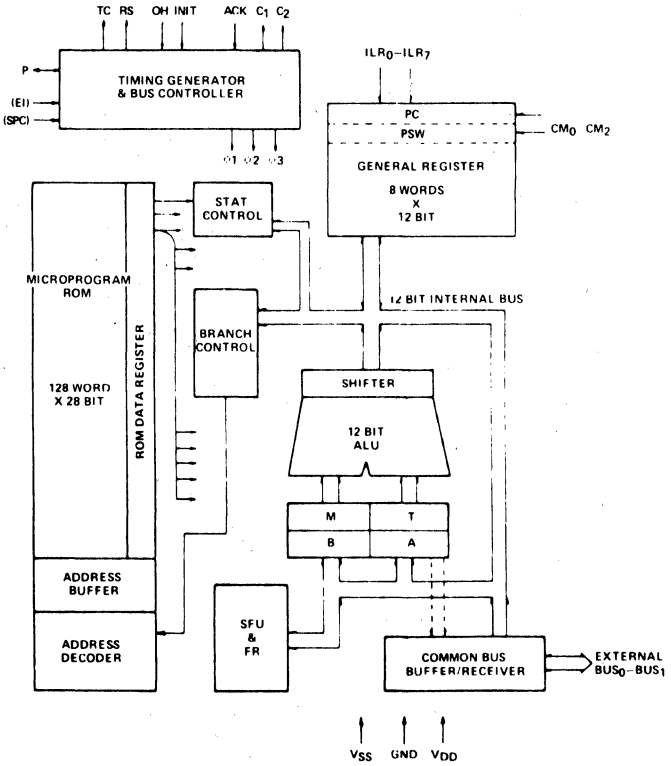
PIN NUMBER	PIN NAME
18	$\overline{\text{PCCIN}}$
19	$\overline{\text{PCCOUT}}$/ BMSB
20	GND
21	POS0
22	POS1
23	ENINCBY2/ AMSB
26	CLOCK
27	INJECTOR 1
28	AOB3
29	AOB2
31	AOB1
32	AOB0
30	PC PRIORITY
33	X
34	Y
35	ALUCOUT
36	OP3
37	OP2
38	OP1
39	OP0
40	INJECTOR 2

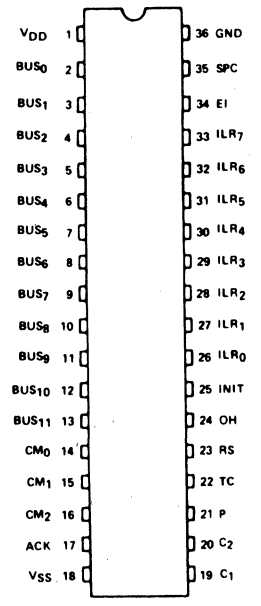
C48


(27-25) CM0–CM2
MICROPROGRAM ROM
(32w x 4x 29b)
SELECTOR
D-REG. (ROMDR)
CONTROL
PC-COUNTER
GENERAL REGISTERS (7w x 12b)
GR ADDRESS CONT.
(S2,S3)
STAT'S & CONDITION CODE CONTROLS
PSW
MASK & CONT.
IR LATCH
BRANCH CONT.
F-REG.
SFU
INTERNAL BUS
DS CONT.
ILR0–ILR7 (16-20, 22-24)
BUFFER
DECODER
REG. CONT.
A-REG.
T-REG.
B-REG.
M-REG.
A or T B or M
BUS DATA COINCIDENCE (BUFFER)
BUS0–BUS11 (4-15)
(28) SPC0
(29) SPC1
(30) SMS
(31) OH
(32) INIT
(33) TC
(34) RS
TIMING GENERATOR
(ICLR)
ALU CONT.
ALU
SHIFTER
(K1) K1'
BUS CONTROL UNIT
C2(3)
C1(2)
ACK (41)
(35) IR
(36) IB
(37) Φ1
(38) Φ3
(39) Φ2
(40) EI
–5V (1)
GND (42)
+5V (21)
(PIN NUMBER)

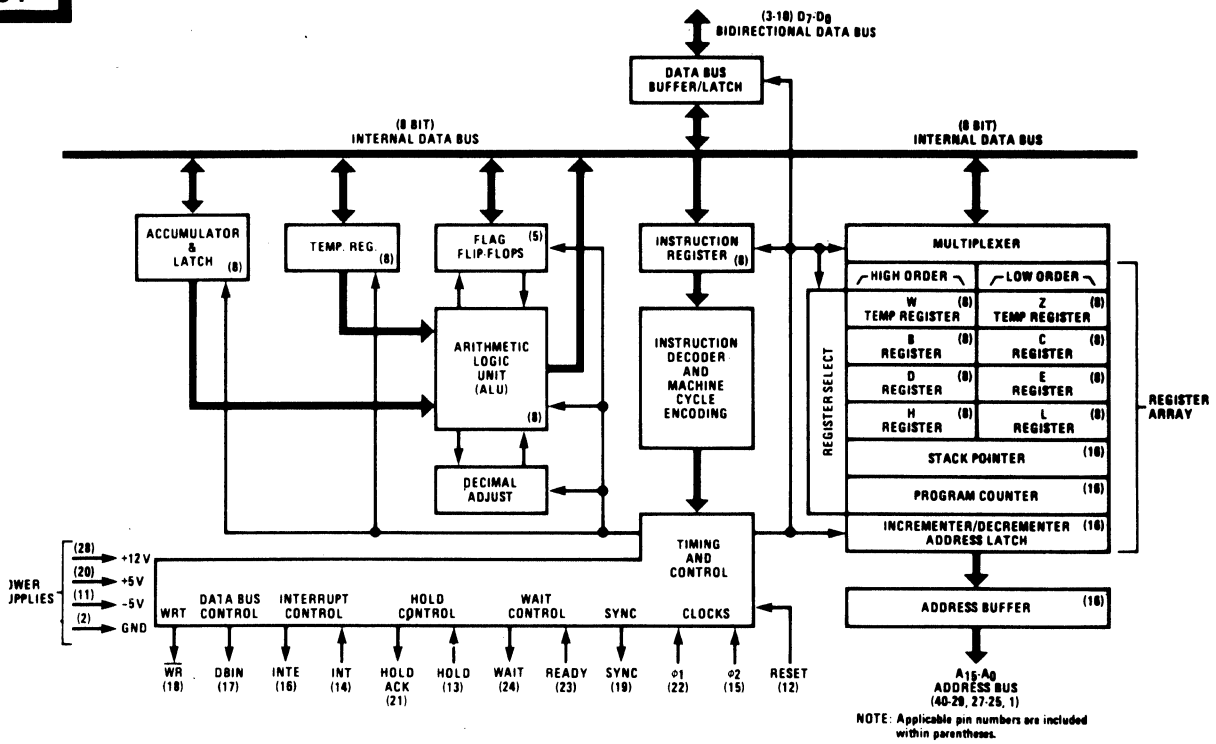

(–5V) VDD 1
C1 2
C2 3
BUS0 4
BUS1 5
BUS2 6
BUS3 7
BUS4 8
BUS5 9
BUS6 10
BUS7 11
BUS8 12
BUS9 13
BUS10 14
BUS11 15
ILR0 16
ILR1 17
ILR2 18
ILR3 19
ILR4 20
(+5V) VSS 21
PROCESSING UNIT
42 GND (0V)
41 ACK
40 EI
39 Φ2
38 Φ3
37 Φ1
36 IB
35 IR
34 RS
33 TC
32 INIT
31 OH
30 SMS
29 SPC1
28 SPC0
27 CM0
26 CM1
25 CM2
24 ILR7
23 ILR6
22 LR5

C49


TC RS OH INIT ACK C1 C2
P
(EI)
(SPC)
TIMING GENERATOR & BUS CONTROLLER
Φ1 Φ2 Φ3
ILR0–ILR7
PC
PSW
CM0 CM2
GENERAL REGISTER
8 WORDS X 12 BIT
STAT CONTROL
MICROPROGRAM ROM
128 WORD X 28 BIT
ROM DATA REGISTER
12 BIT INTERNAL BUS
BRANCH CONTROL
SHIFTER
12 BIT ALU
M
T
B
A
ADDRESS BUFFER
ADDRESS DECODER
SFU & FR
COMMON BUS BUFFER/RECEIVER
EXTERNAL BUS0–BUS1
VSS GND VDD

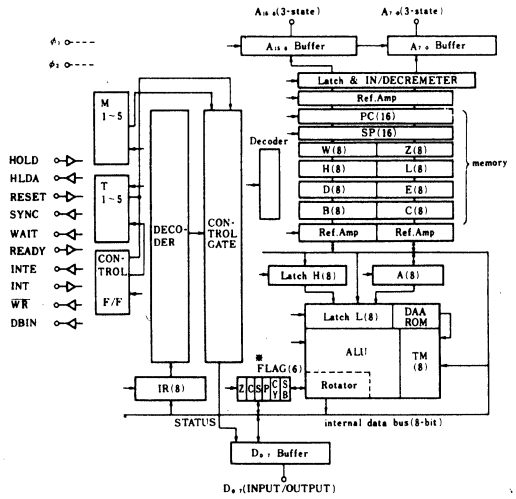

VDD 1
BUS0 2
BUS1 3
BUS2 4
BUS3 5
BUS4 6
BUS5 7
BUS6 8
BUS7 9
BUS8 10
BUS9 11
BUS10 12
BUS11 13
CM0 14
CM1 15
CM2 16
ACK 17
VSS 18
36 GND
35 SPC
34 EI
33 ILR7
32 ILR6
31 ILR5
30 ILR4
29 ILR3
28 ILR2
27 ILR1
26 ILR0
25 INIT
24 OH
23 RS
22 TC
21 P
20 C2
19 C1

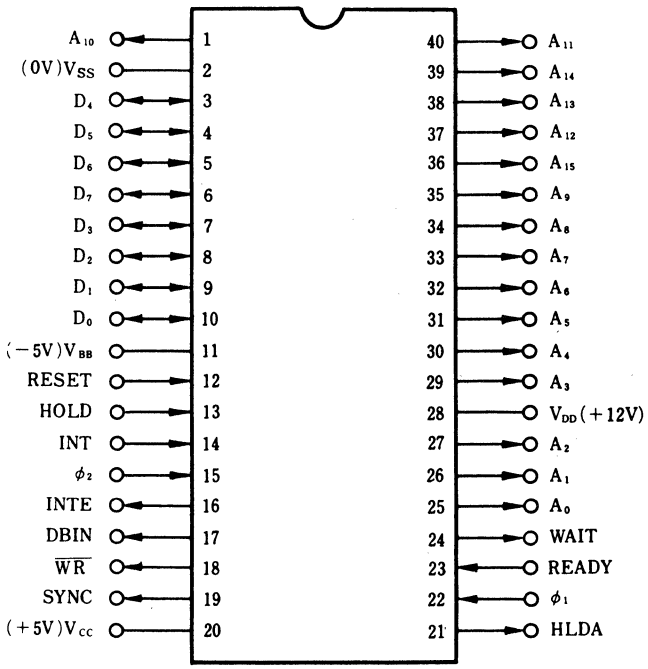
C54



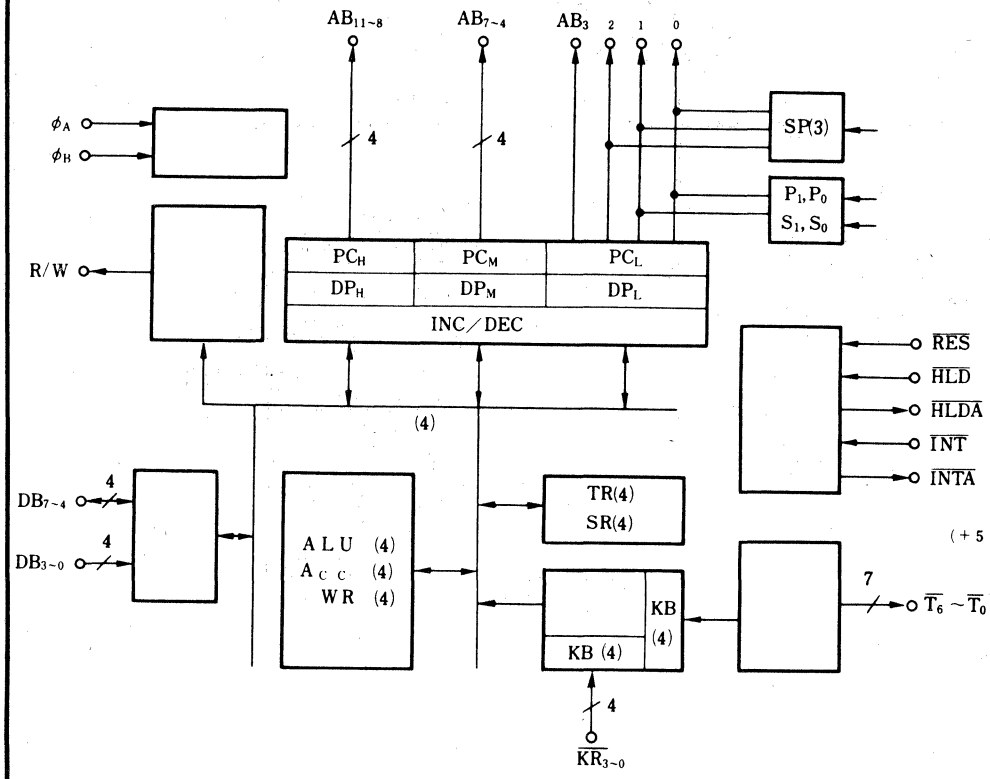
NOTE: Applicable pin numbers are included within parentheses.

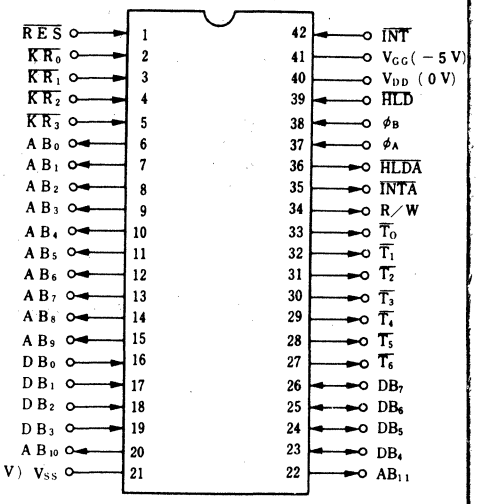
C55



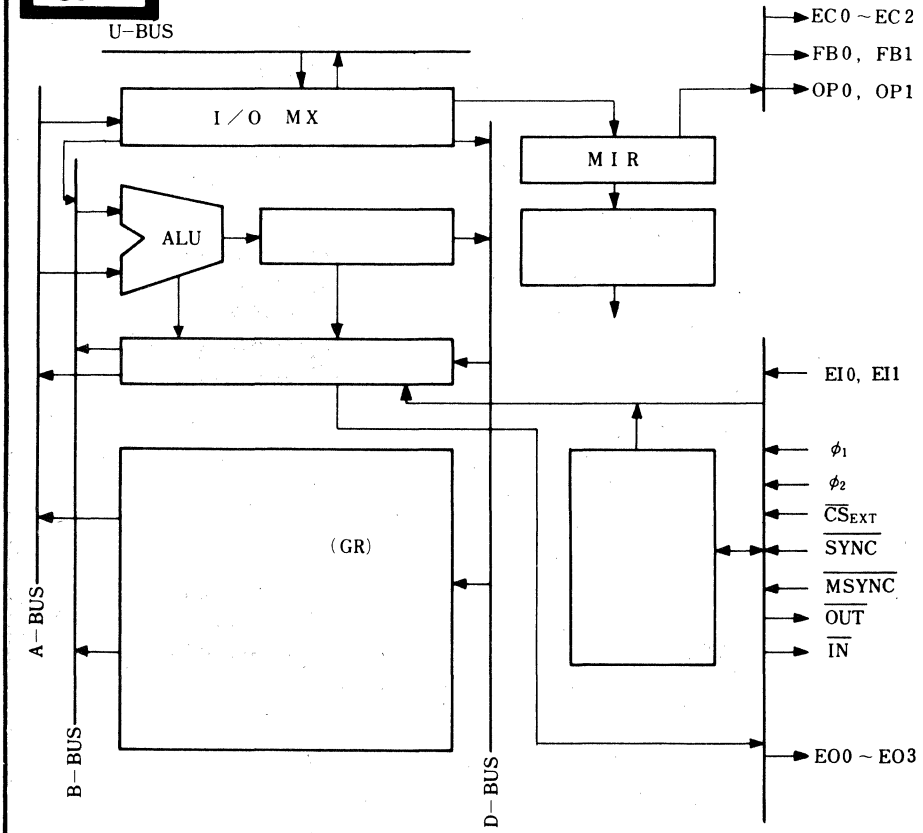


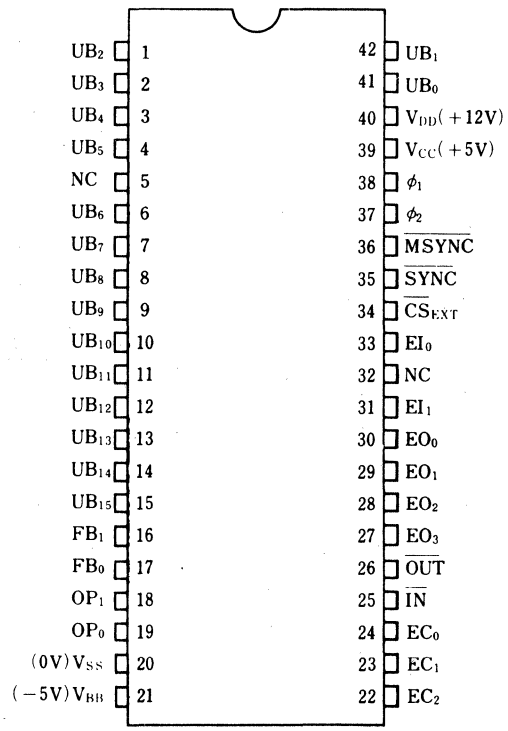
C56


AB11~8
AB7~4
AB3 2 1 0
φA
φH
4
4
SP(3)
P1, P0
S1, S0
R/W
PCH
PCM
PCL
DPH
DPM
DPL
INC/DEC
(4)
RES
HLD
HLDA
INT
INTA
DB7~4
DB3~0
4
4
ALU (4)
ACC (4)
WR (4)
TR(4)
SR(4)
KB
(4)
KB (4)
7
T6 ~ T0
4
KR3~0

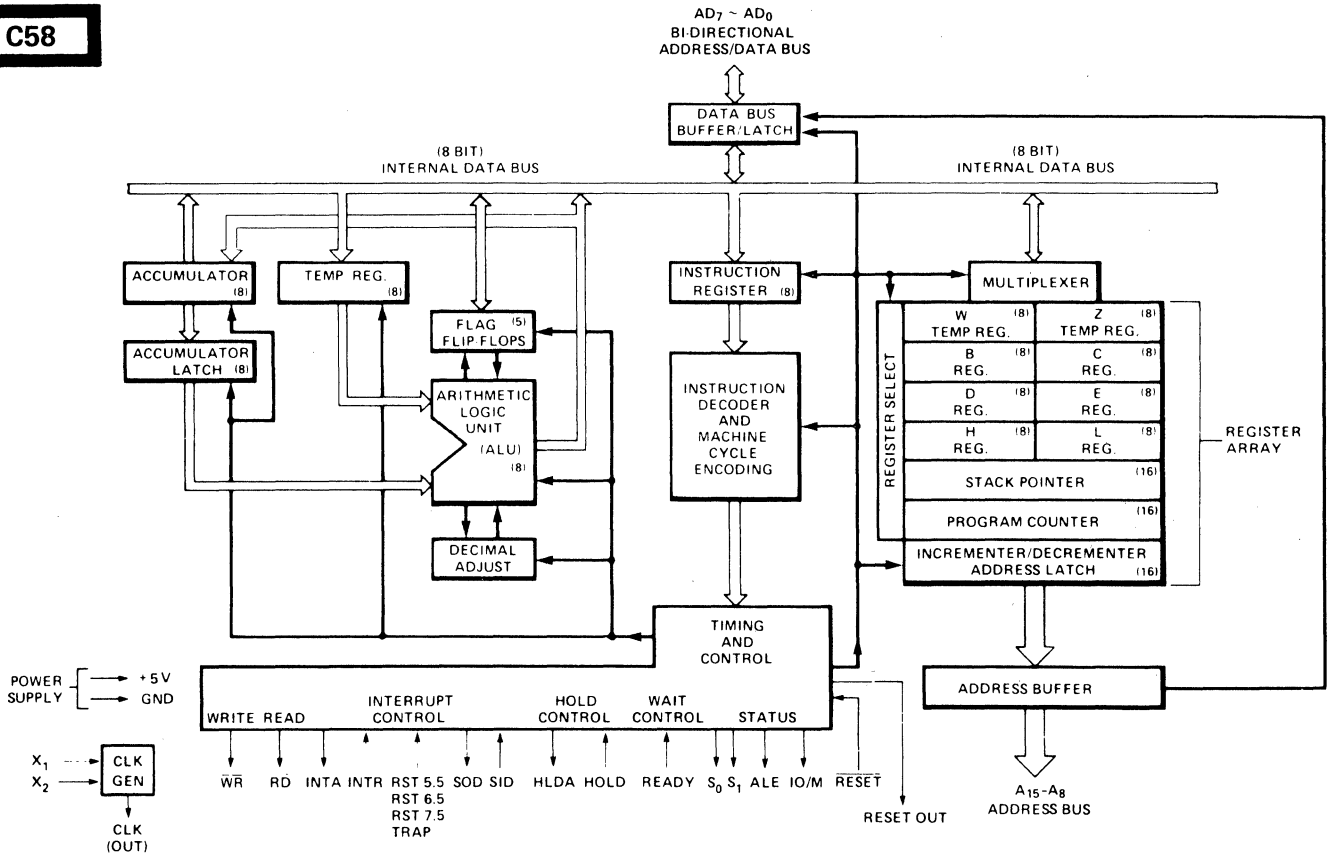

RES 1
KR0 2
KR1 3
KR2 4
KR3 5
AB0 6
AB1 7
AB2 8
AB3 9
AB4 10
AB5 11
AB6 12
AB7 13
AB8 14
AB9 15
DB0 16
DB1 17
DB2 18
DB3 19
AB10 20
(+5V) VSS 21
42 INT
41 VGG (−5V)
40 VDD (0V)
39 HLD
38 φB
37 φA
36 HLDA
35 INTA
34 R/W
33 T0
32 T1
31 T2
30 T3
29 T4
28 T5
27 T6
26 DB7
25 DB6
24 DB5
23 DB4
22 AB11

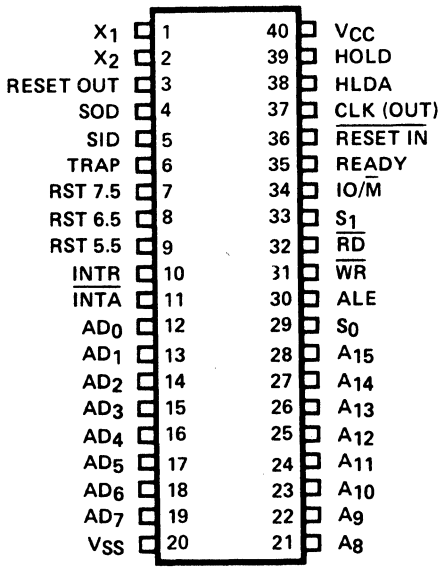
C57


U-BUS
EC0 ~ EC2
FB0, FB1
OP0, OP1
I/O MX
MIR
ALU
EI0, EI1
φ1
φ2
CSEXT
SYNC
MSYNC
OUT
IN
(GR)
EO0 ~ EO3
A-BUS
B-BUS
D-BUS

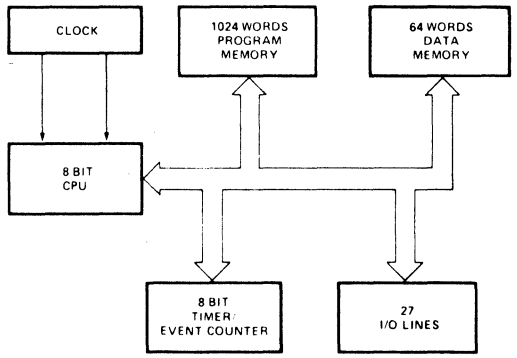

UB2 1
UB3 2
UB4 3
UB5 4
NC 5
UB6 6
UB7 7
UB8 8
UB9 9
UB10 10
UB11 11
UB12 12
UB13 13
UB14 14
UB15 15
FB1 16
FB0 17
OP1 18
OP0 19
(0V) VSS 20
(−5V) VBB 21
42 UB1
41 UB0
40 VDD (+12V)
39 VCC (+5V)
38 φ1
37 φ2
36 MSYNC
35 SYNC
34 CSEXT
33 EI0
32 NC
31 EI1
30 EO0
29 EO1
28 EO2
27 EO3
26 OUT
25 IN
24 EC0
23 EC1
22 EC2

C58

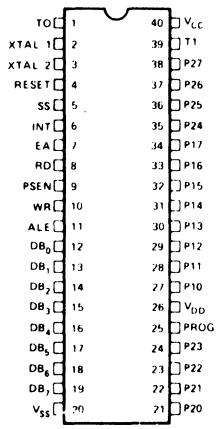




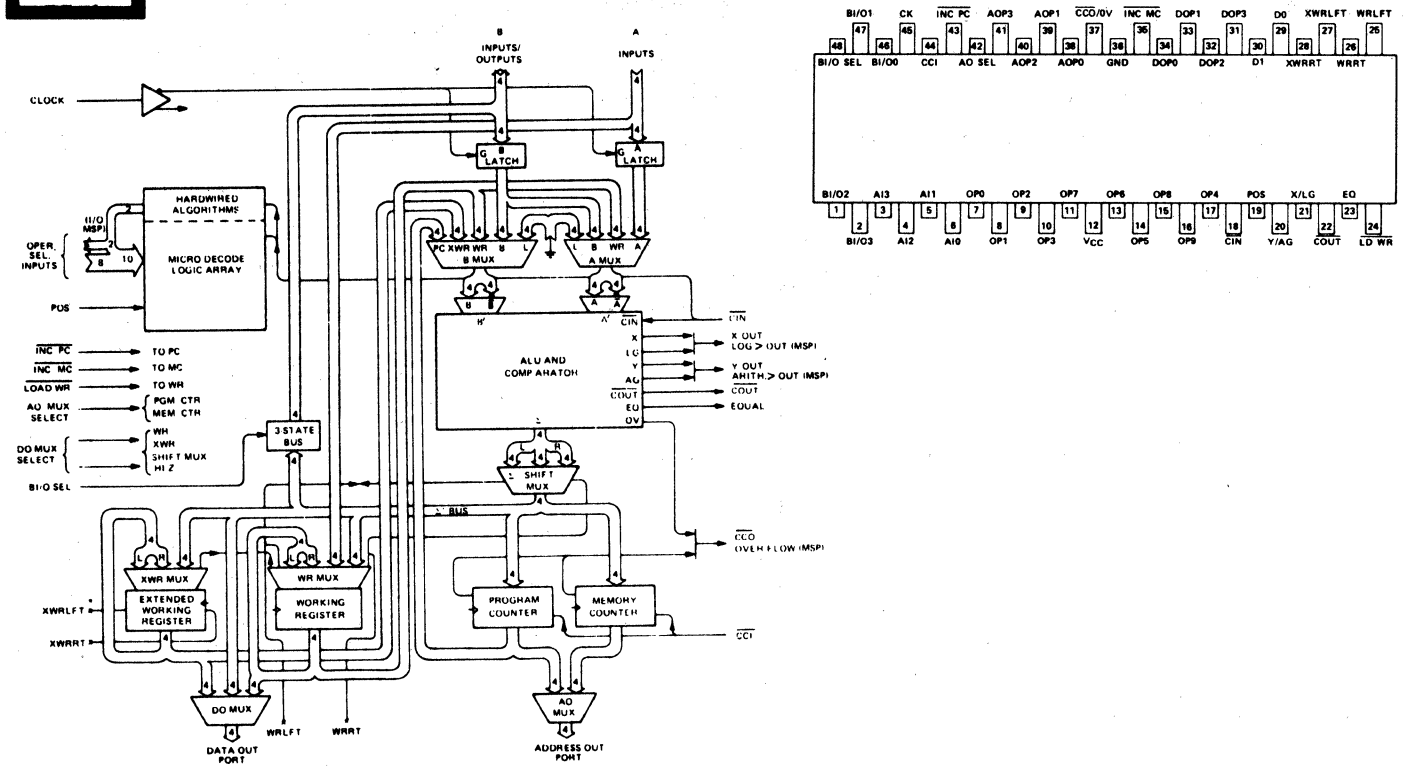
C59



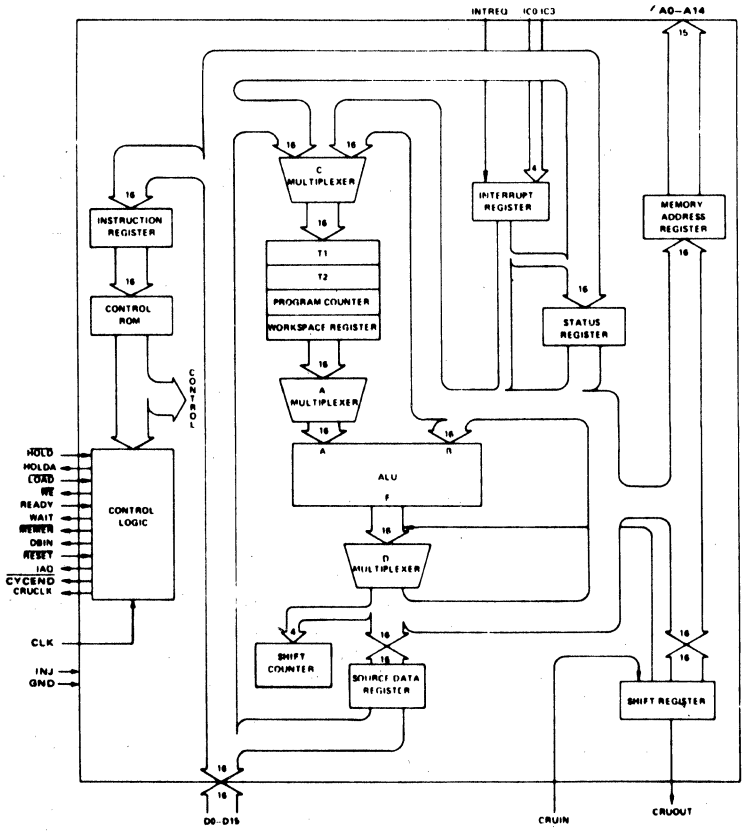
	PROGRAM MEMORY
C59	ROM
C59a	EPROM
C59b	NOT INCLUDED

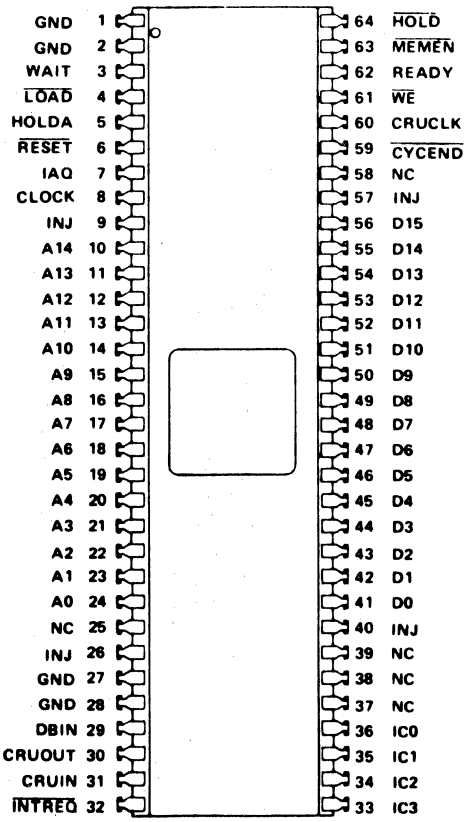


C61


B INPUTS/ OUTPUTS
A INPUTS
CLOCK
G B LATCH
G A LATCH
HARDWIRED ALGORITHMS
MICRO DECODE LOGIC ARRAY
I/O MSPI
OPER. SEL. INPUTS
POS
PC XWR WR B MUX
L B WR A MUX
ALU AND COMP AHATOH
CIN
X OUT LOG> OUT (MSPI)
Y OUT ARITH.> OUT (MSPI)
COUT
EQUAL
OV
INC PC
INC MC
LOAD WR
AQ MUX SELECT
DO MUX SELECT
BI/O SEL
TO PC
TO MC
TO WR
PGM CTR
MEM CTR
WR
XWR
SHIFT MUX
HI Z
3 STATE BUS
SHIFT MUX
BUS
CCO OVERFLOW (MSPI)
XWR MUX
WR MUX
EXTENDED WORKING REGISTER
WORKING REGISTER
PROGRAM COUNTER
MEMORY COUNTER
CCI
XWRLFT
XWRRT
DO MUX
AQ MUX
WRLFT
WRRT
DATA OUT PORT
ADDRESS OUT PORT
BI/O1 CK INC PC AOP3 AOP1 CCO/OV INC MC DOP1 DOP3 D0 XWRLFT WRLFT
BI/O SEL BI/O0 CCI AO SEL AOP2 AOP0 GND DOP0 DOP2 D1 XWRRT WRRT
BI/O2 AI3 AI1 OP0 OP2 OP7 OP6 OP8 OP4 POS X/LG EO
BI/O3 AI2 AI0 OP1 OP3 VCC OP5 OP9 CIN Y/AG COUT LD WR

C62

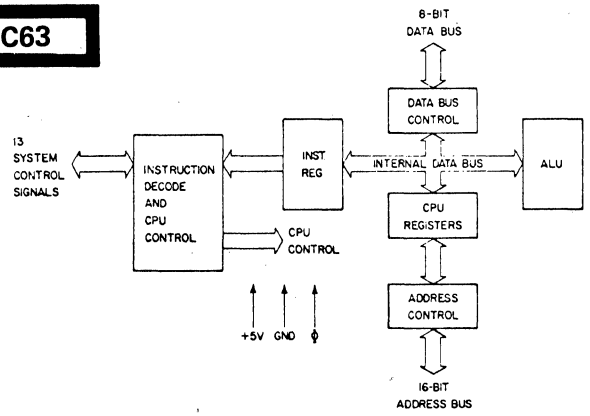

INTREQ IC0 IC3
A0–A14
C MULTIPLEXER
INTERRUPT REGISTER
MEMORY ADDRESS REGISTER
INSTRUCTION REGISTER
T1
T2
PROGRAM COUNTER
WORKSPACE REGISTER
STATUS REGISTER
CONTROL ROM
A MULTIPLEXER
CONTROL
ALU
D MULTIPLEXER
HOLD
HOLDA
LOAD
WE
READY
WAIT
MEMEN
DBIN
RESET
IAQ
CYCEND
CRUCLK
CONTROL LOGIC
CLK
INJ
GND
SHIFT COUNTER
SOURCE DATA REGISTER
SHIFT REGISTER
D0–D15
CRUIN
CRUOUT


GND 1
GND 2
WAIT 3
LOAD 4
HOLDA 5
RESET 6
IAQ 7
CLOCK 8
INJ 9
A14 10
A13 11
A12 12
A11 13
A10 14
A9 15
A8 16
A7 17
A6 18
A5 19
A4 20
A3 21
A2 22
A1 23
A0 24
NC 25
INJ 26
GND 27
GND 28
DBIN 29
CRUOUT 30
CRUIN 31
INTREQ 32
64 HOLD
63 MEMEN
62 READY
61 WE
60 CRUCLK
59 CYCEND
58 NC
57 INJ
56 D15
55 D14
54 D13
53 D12
52 D11
51 D10
50 D9
49 D8
48 D7
47 D6
46 D5
45 D4
44 D3
43 D2
42 D1
41 D0
40 INJ
39 NC
38 NC
37 NC
36 IC0
35 IC1
34 IC2
33 IC3

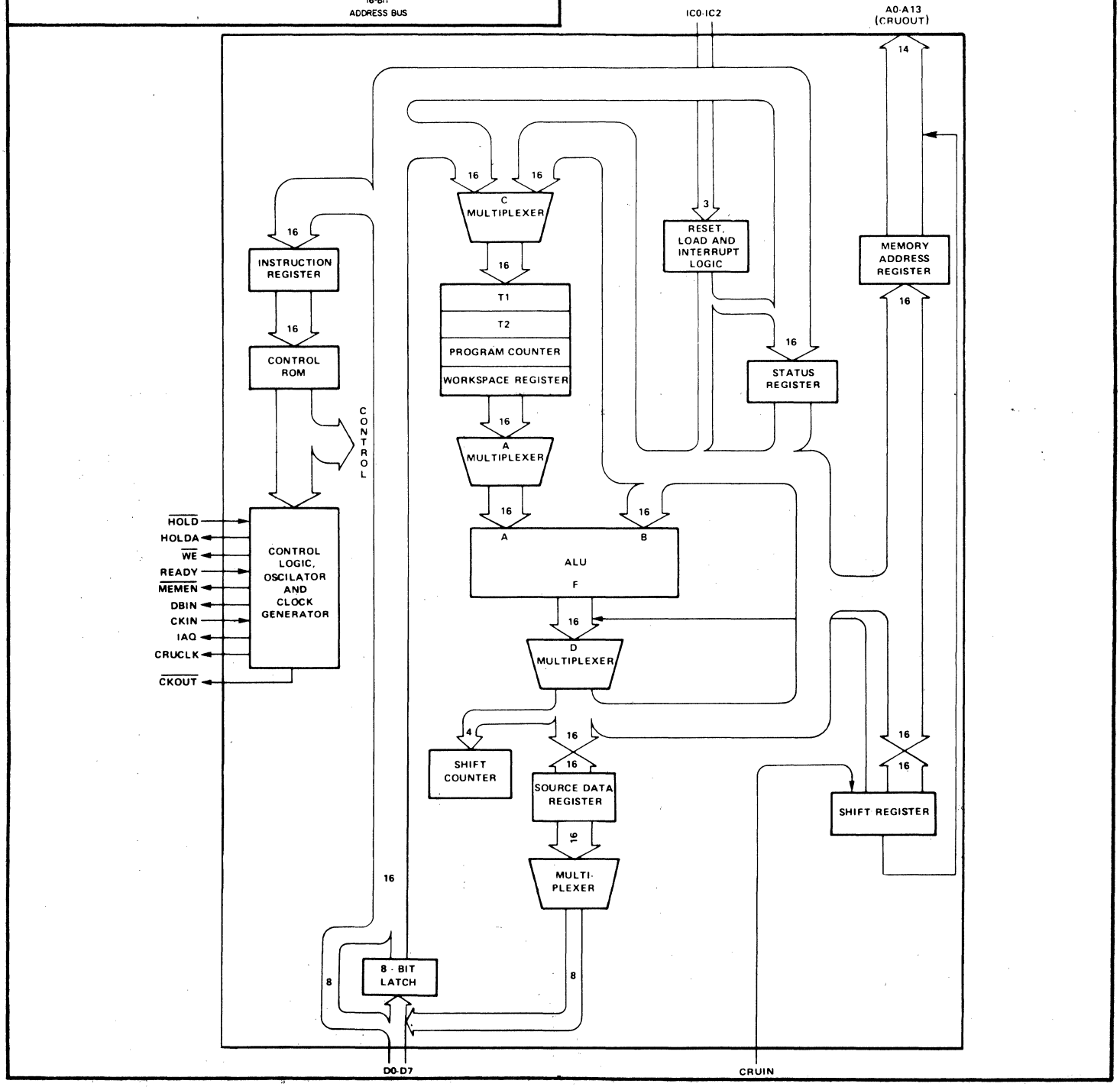
18. CPU INTERNAL ARCHITECTURE DRAWINGS

IN DRAWING NUMBER SEQUENCE

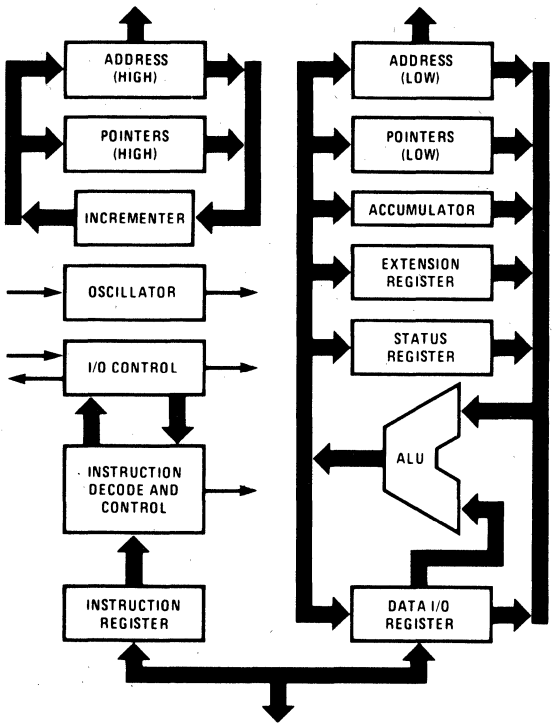
C63

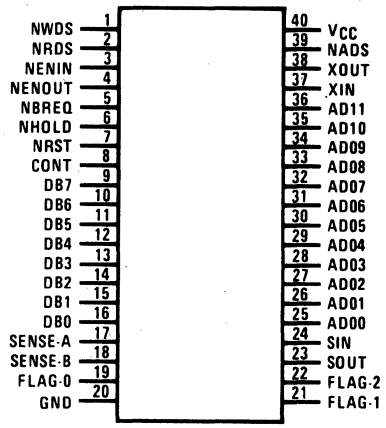


C64

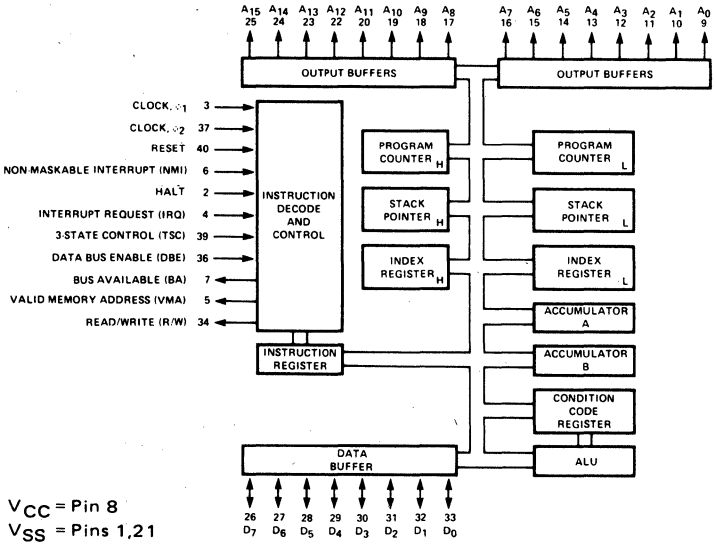


C65

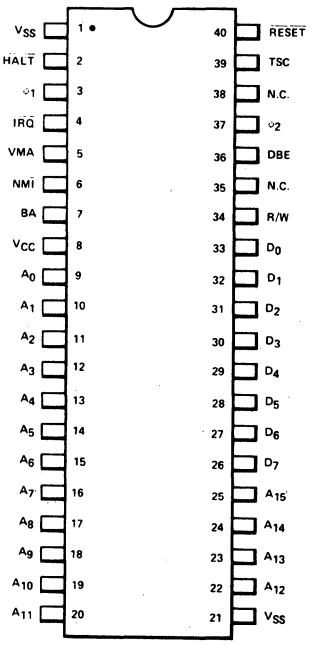




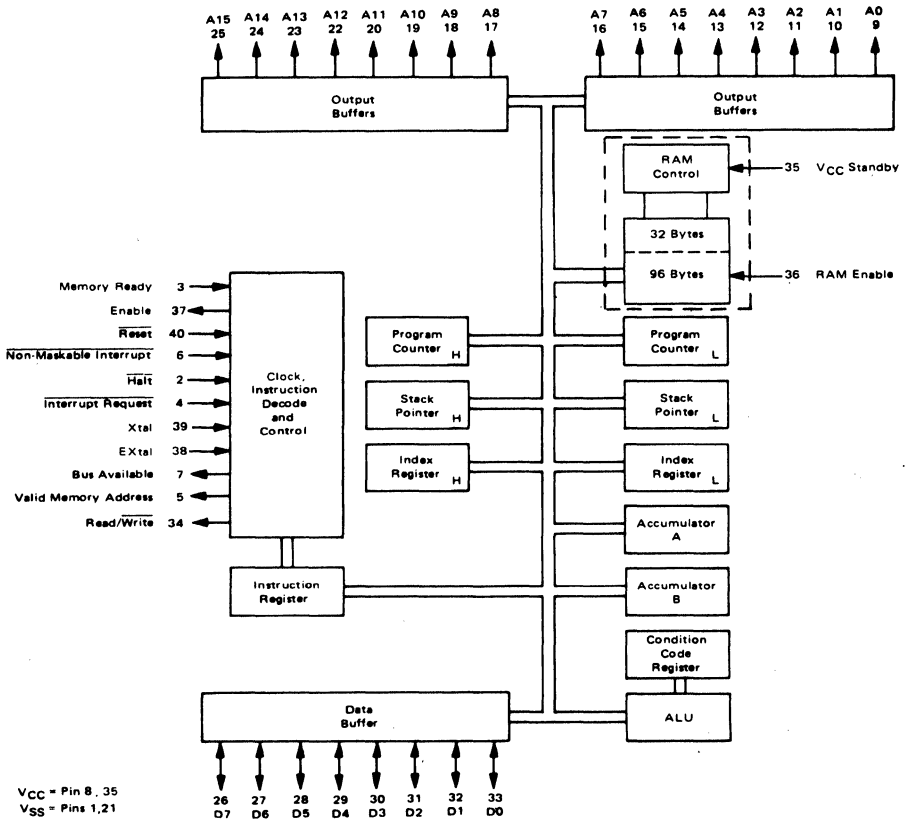
C66



VCC = Pin 8
VSS = Pins 1,21



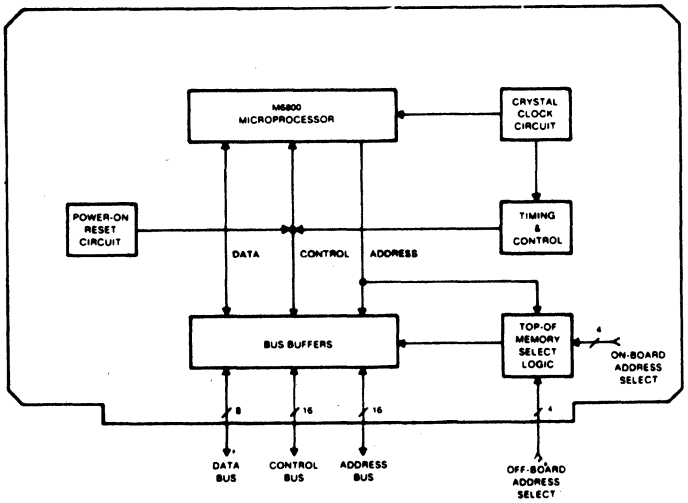
C67



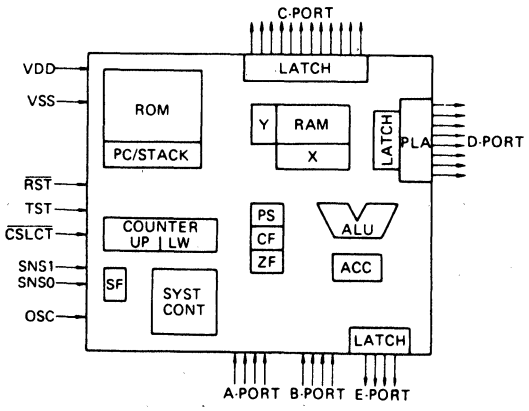
C67a: WITHOUT DOTTED BOX AND V_{SS} = PINS 1,21,36

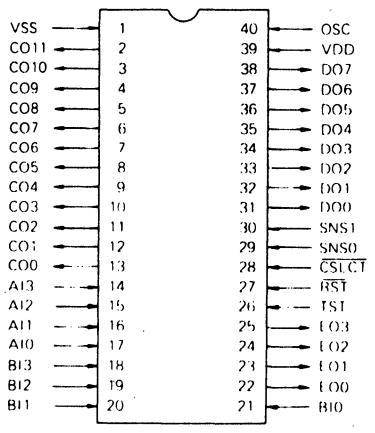
NOTE: C67b SAME AS C67a WITH PINS 38 AND 39 REVERSED.

C68

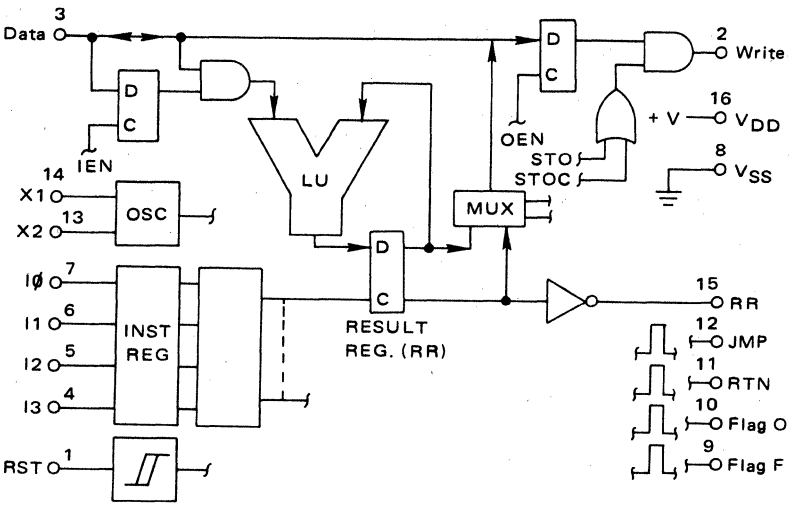


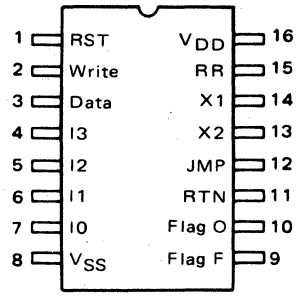
C69



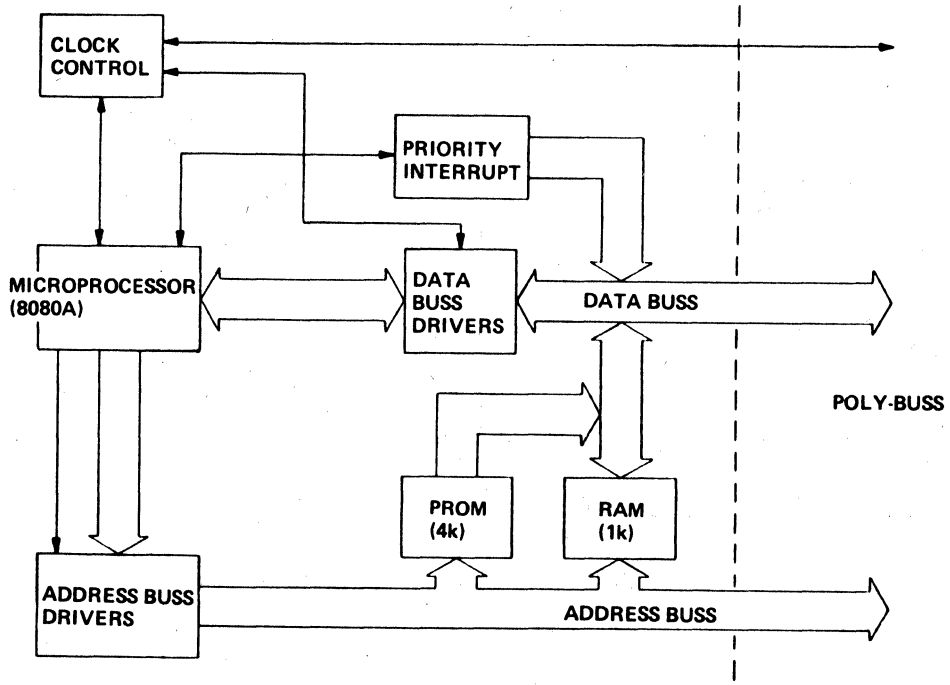


C73

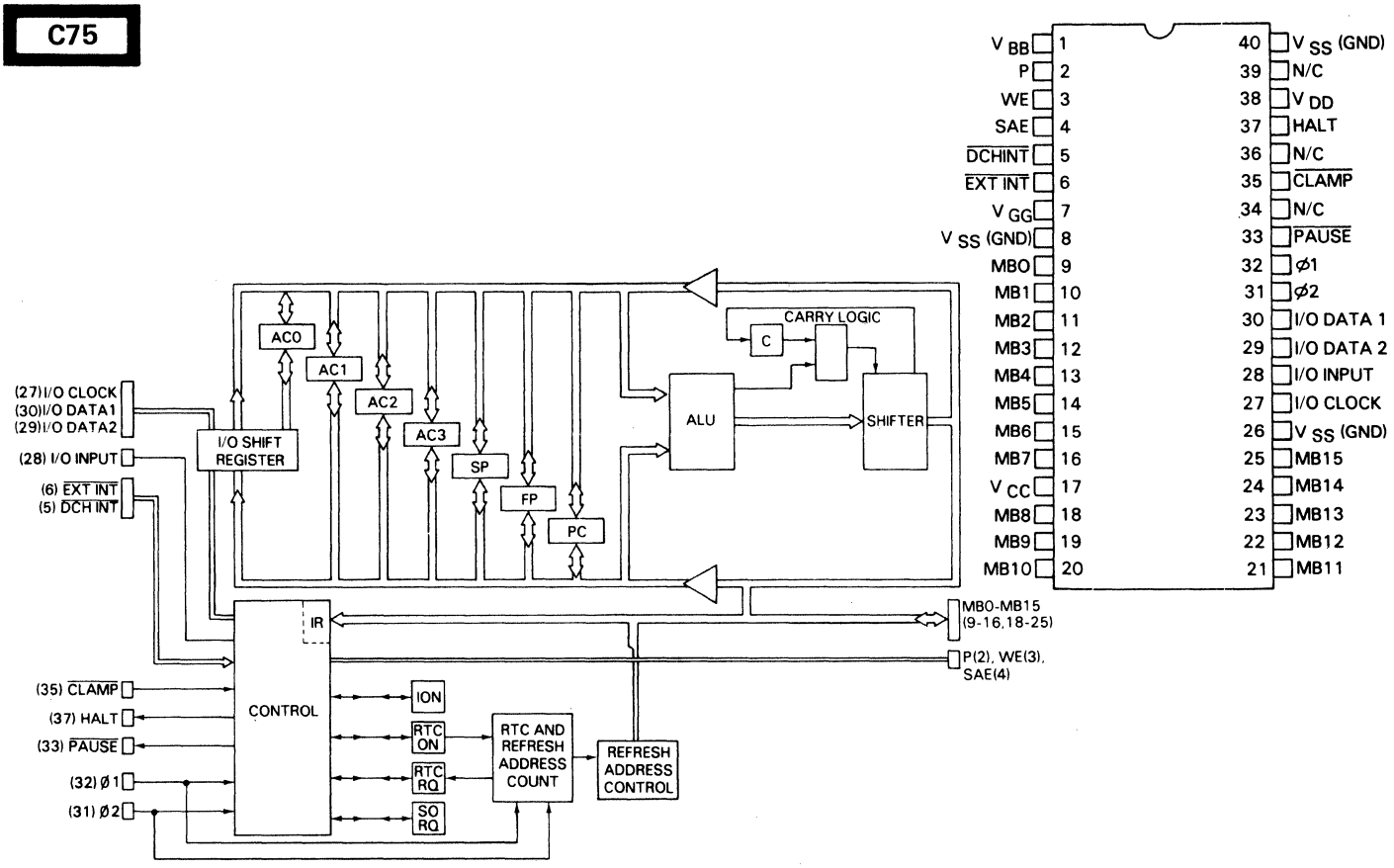

3
Data
D
C
IEN
14
X1
13
X2
OSC
LU
D
C
OEN
MUX
2
Write
+ V
16
VDD
STO
STOC
8
VSS
I0
7
I1
6
I2
5
I3
4
INST
REG
RESULT
REG. (RR)
15
RR
12
JMP
11
RTN
10
Flag O
9
Flag F
RST
1


1 RST
2 Write
3 Data
4 I3
5 I2
6 I1
7 I0
8 VSS
16 VDD
15 RR
14 X1
13 X2
12 JMP
11 RTN
10 Flag O
9 Flag F

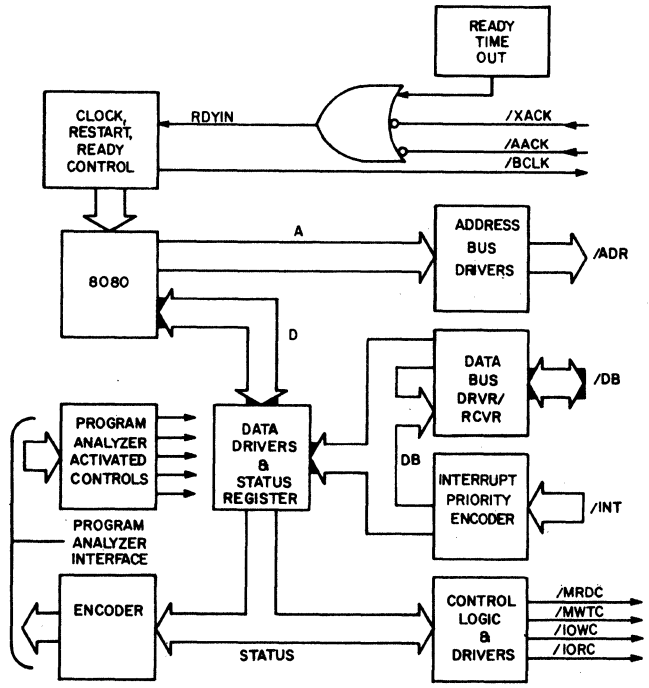
C74


CLOCK CONTROL
PRIORITY INTERRUPT
MICROPROCESSOR (8080A)
DATA BUSS DRIVERS
DATA BUSS
POLY-BUSS
PROM (4k)
RAM (1k)
ADDRESS BUSS DRIVERS
ADDRESS BUSS

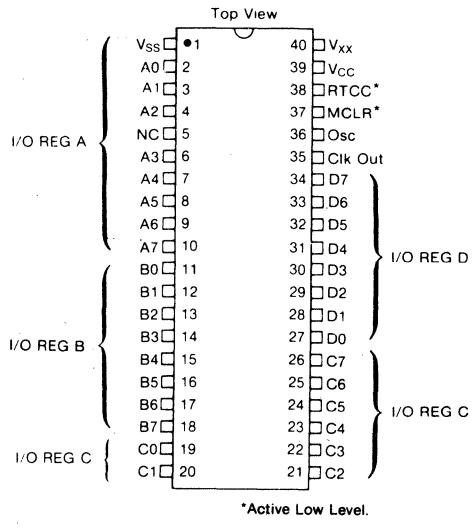
C75



C76

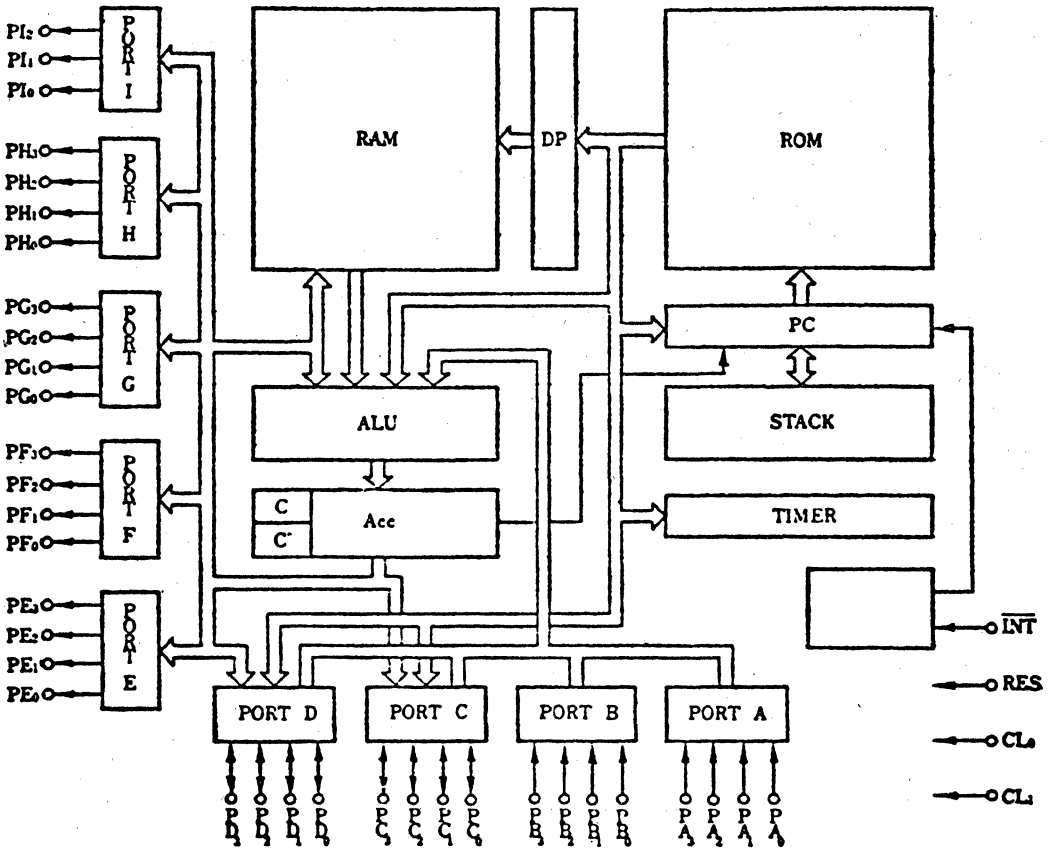


C77

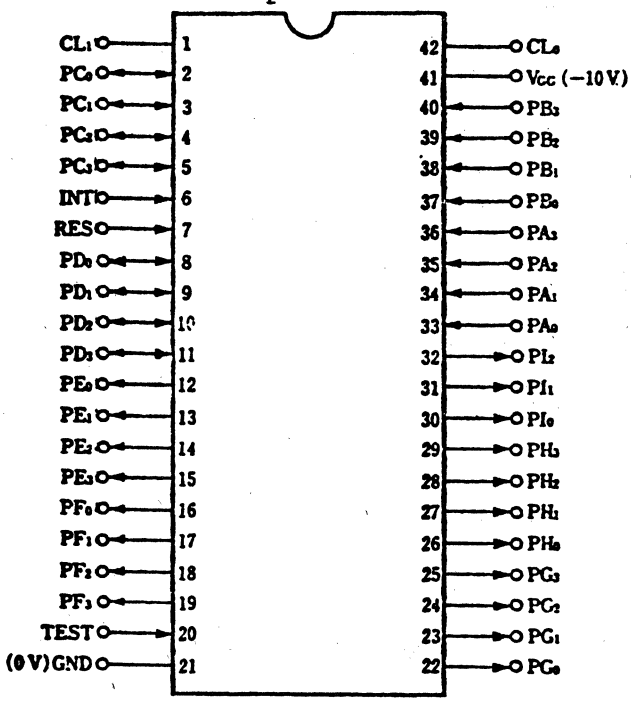


*Active Low Level.

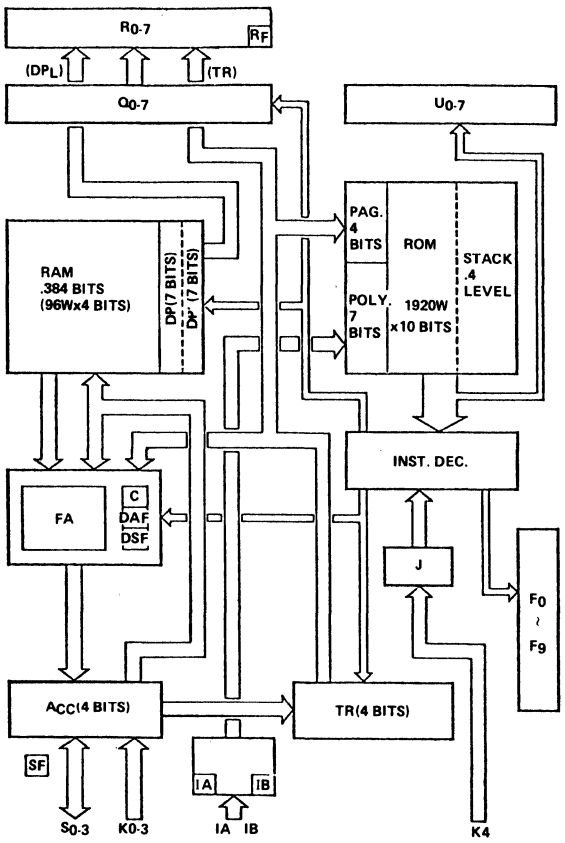
C79

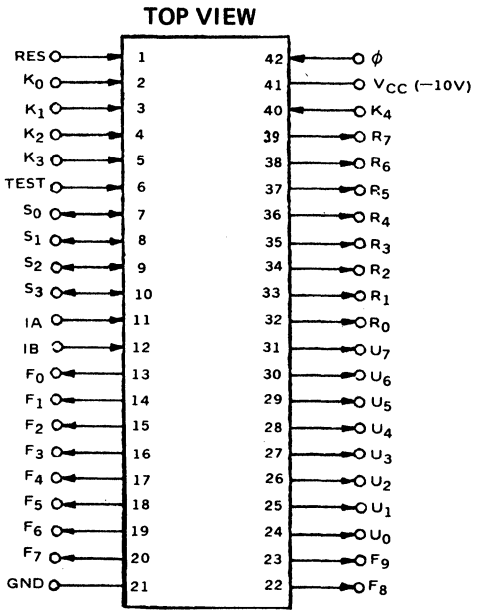

PI2
PI1
PI0
PORT I
PH3
PH2
PH1
PH0
PORT H
PG3
PG2
PG1
PG0
PORT G
PF3
PF2
PF1
PF0
PORT F
PE3
PE2
PE1
PE0
PORT E
RAM
DP
ROM
PC
ALU
STACK
C
C'
Acc
TIMER
INT
RES
CL0
CL1
PORT D
PORT C
PORT B
PORT A

Top View

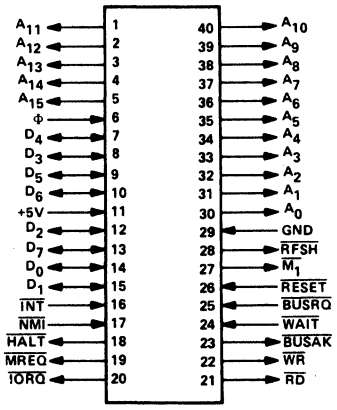

CL1 1
PC0 2
PC1 3
PC2 4
PC3 5
INT 6
RES 7
PD0 8
PD1 9
PD2 10
PD3 11
PE0 12
PE1 13
PE2 14
PE3 15
PF0 16
PF1 17
PF2 18
PF3 19
TEST 20
(0V) GND 21
42 CL0
41 Vcc (−10V)
40 PB3
39 PB2
38 PB1
37 PB0
36 PA3
35 PA2
34 PA1
33 PA0
32 PI2
31 PI1
30 PI0
29 PH3
28 PH2
27 PH1
26 PH0
25 PG3
24 PG2
23 PG1
22 PG0

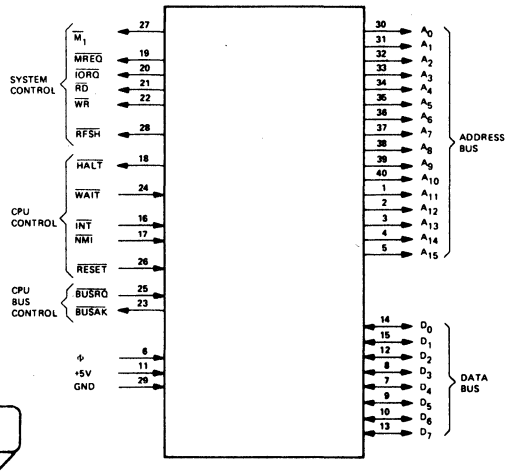
C80

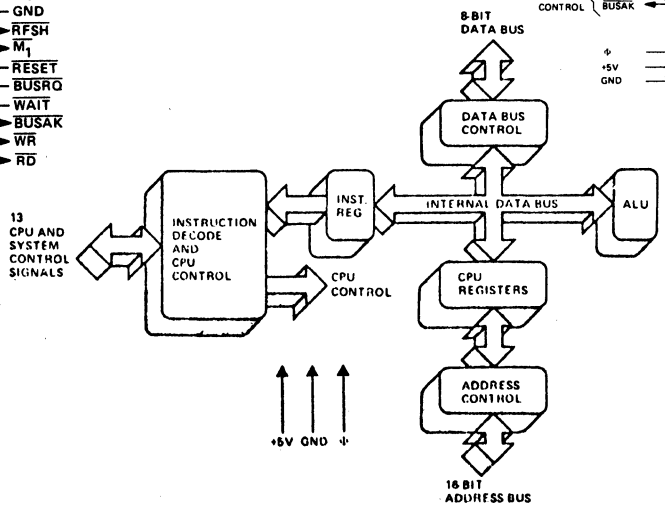

R0-7
RF
(DPL)
(TR)
Q0-7
U0-7
RAM
.384 BITS
(96Wx4 BITS)
DP(7 BITS)
DP' (7 BITS)
PAG.
4
BITS
ROM
STACK
.4
LEVEL
POLY.
7
BITS
1920W
x10 BITS
INST. DEC.
FA
C
DAF
DSF
J
F0
~
F9
ACC(4 BITS)
TR(4 BITS)
SF
IA
IB
S0-3
K0-3
IA IB
K4


TOP VIEW
RES 1
K0 2
K1 3
K2 4
K3 5
TEST 6
S0 7
S1 8
S2 9
S3 10
IA 11
IB 12
F0 13
F1 14
F2 15
F3 16
F4 17
F5 18
F6 19
F7 20
GND 21
42 φ
41 VCC (−10V)
40 K4
39 R7
38 R6
37 R5
36 R4
35 R3
34 R2
33 R1
32 R0
31 U7
30 U6
29 U5
28 U4
27 U3
26 U2
25 U1
24 U0
23 F9
22 F8

C81

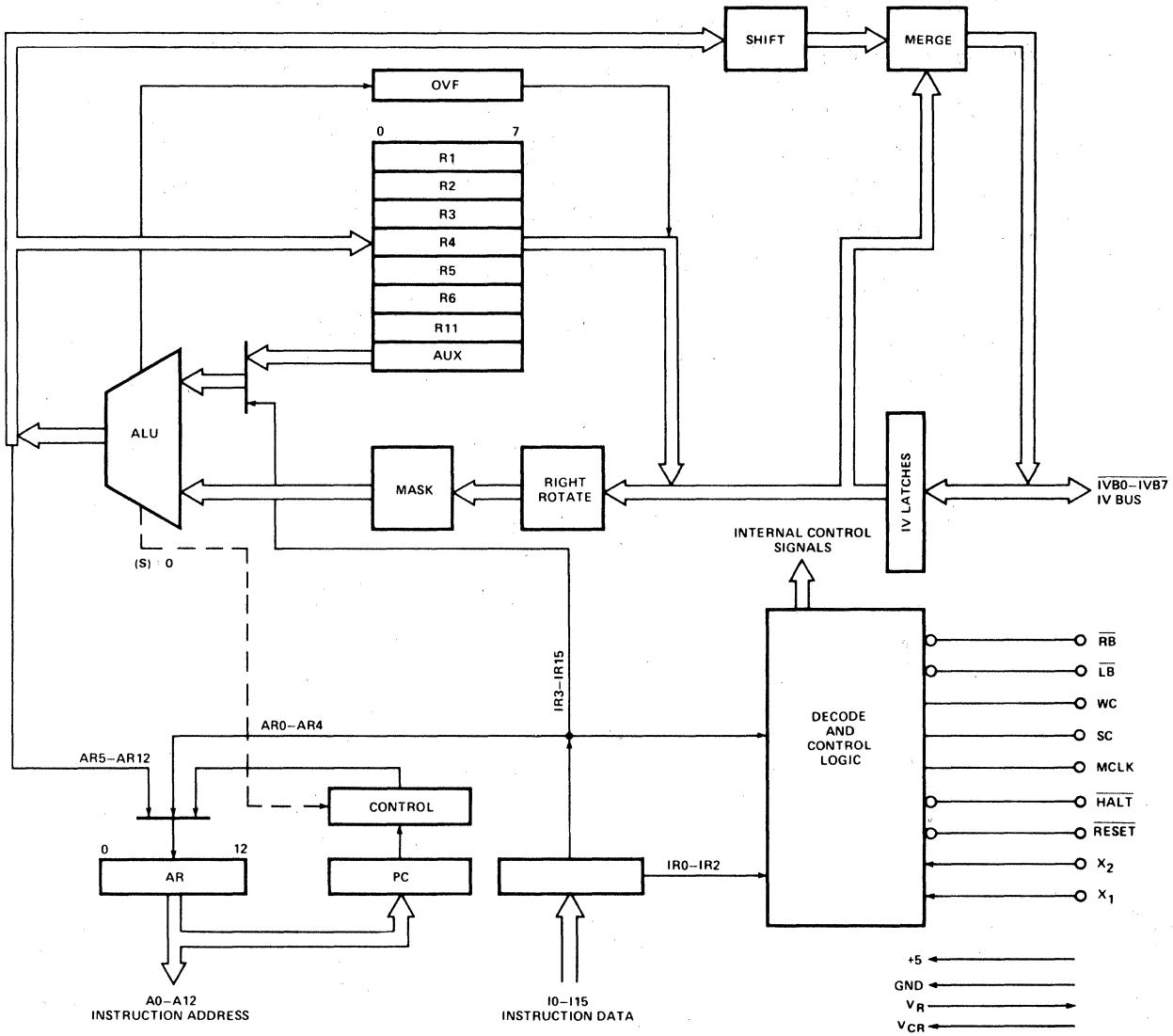

A11 1
A12 2
A13 3
A14 4
A15 5
Φ 6
D4 7
D3 8
D5 9
D6 10
+5V 11
D2 12
D7 13
D0 14
D1 15
INT 16
NMI 17
HALT 18
MREQ 19
IORQ 20
40 A10
39 A9
38 A8
37 A7
36 A6
35 A5
34 A4
33 A3
32 A2
31 A1
30 A0
29 GND
28 RFSH
27 M1
26 RESET
25 BUSRQ
24 WAIT
23 BUSAK
22 WR
21 RD

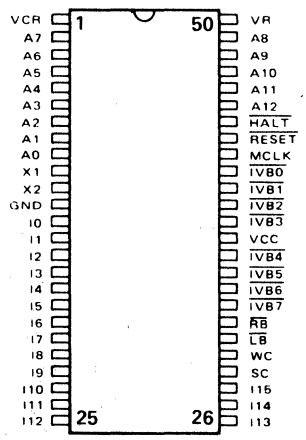

SYSTEM CONTROL
M1 27
MREQ 19
IORQ 20
RD 21
WR 22
RFSH 28
CPU CONTROL
HALT 18
WAIT 24
INT 16
NMI 17
RESET 26
CPU BUS CONTROL
BUSRQ 25
BUSAK 23
Φ 6
+5V 11
GND 29
30 A0
31 A1
32 A2
33 A3
34 A4
35 A5
36 A6
37 A7
38 A8
39 A9
40 A10
1 A11
2 A12
3 A13
4 A14
5 A15
ADDRESS BUS
14 D0
15 D1
12 D2
8 D3
7 D4
9 D5
10 D6
13 D7
DATA BUS


8-BIT DATA BUS
DATA BUS CONTROL
INTERNAL DATA BUS
INST. REG
ALU
13 CPU AND SYSTEM CONTROL SIGNALS
INSTRUCTION DECODE AND CPU CONTROL
CPU CONTROL
CPU REGISTERS
ADDRESS CONTROL
+5V GND Φ
16 BIT ADDRESS BUS

C82

INTERPRETER ARCHITECTURE

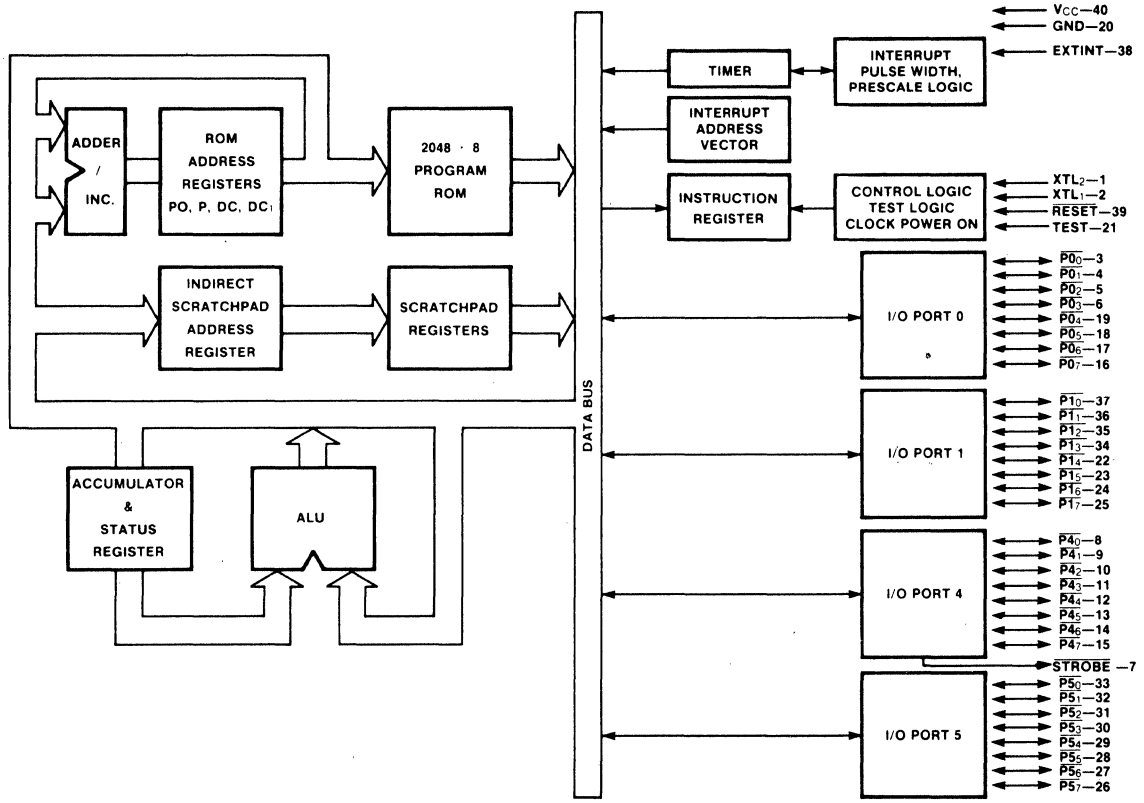


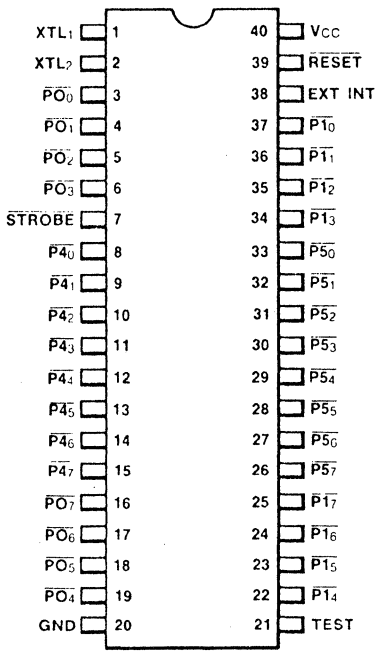


18. CPU INTERNAL ARCHITECTURE DRAWINGS

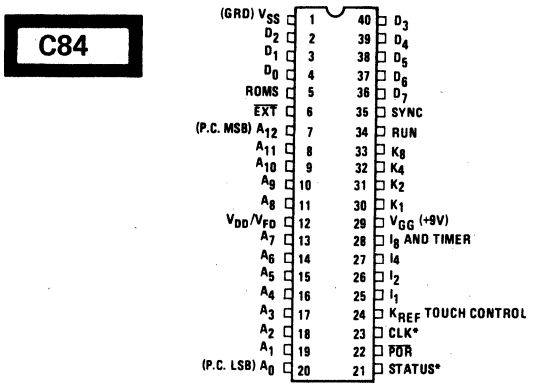
IN DRAWING NUMBER SEQUENCE

C83

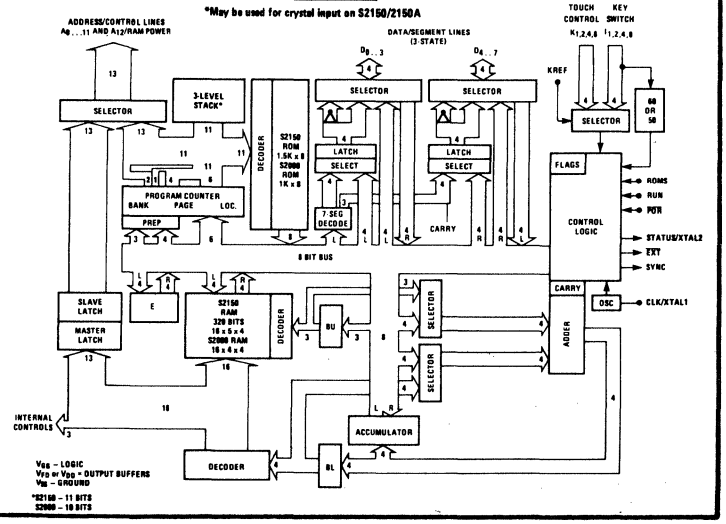




C84



*May be used for crystal input on S2150/2150A



18. CPU INTERNAL ARCHITECTURE DRAWINGS

IN DRAWING NUMBER SEQUENCE

C85

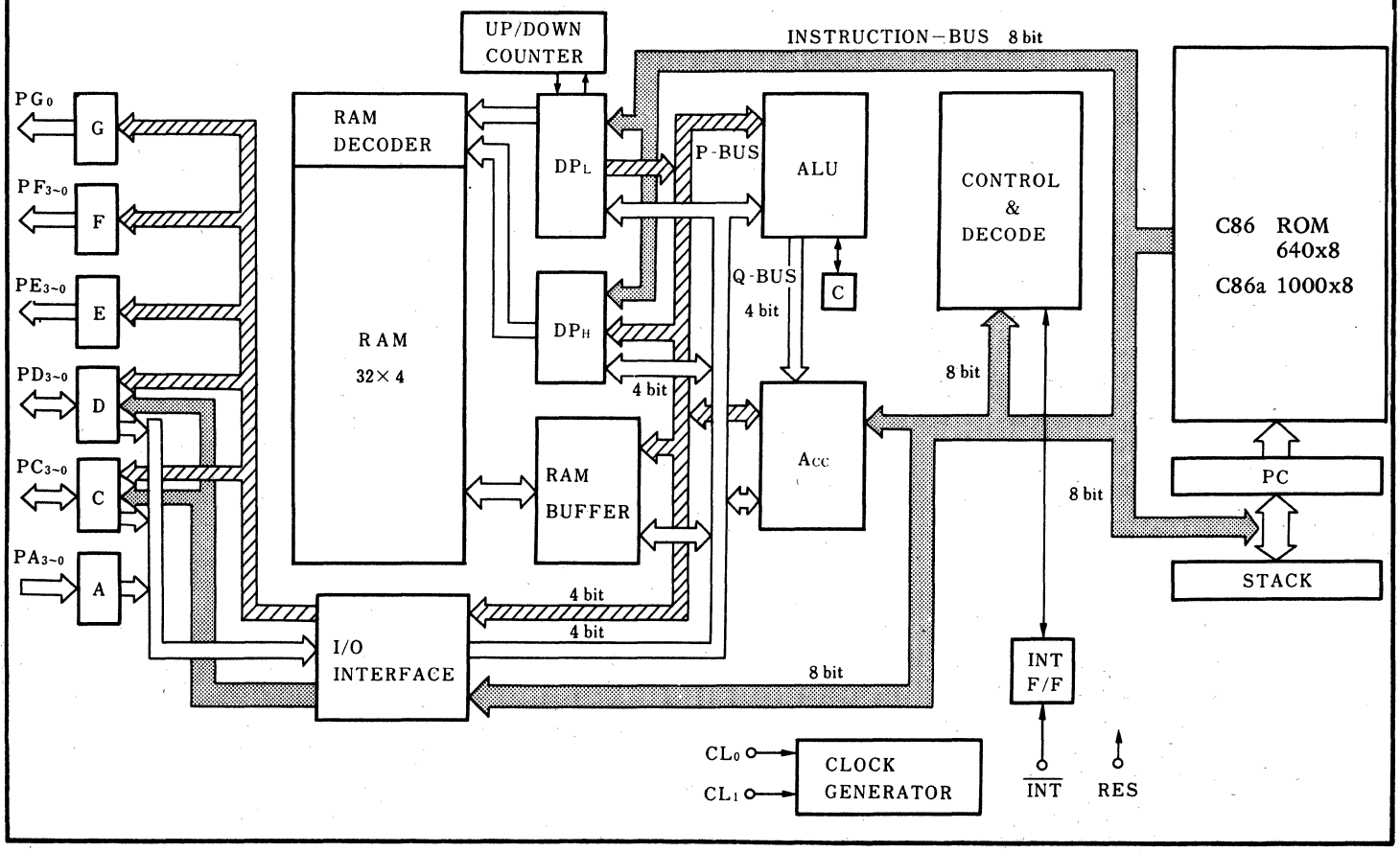
(Top View)

NC	1	64	IC(GND)
NC	2	63	NC
$\overline{RES}$	3	62	K_0
Q_3	4	61	K_1
Q_2	5	60	K_2
Q_1	6	59	K_3
Q_0	7	58	S_0
F_7	8	57	S_1
F_6	9	56	S_2
F_5	10	55	S_3
F_4	11	54	INT_B
F_3	12	53	INT_A
F_2	13	52	DB_0
F_1	14	51	DB_1
F_0	15	50	DB_2
TEST 2	16	49	DB_3
R_9	17	48	AB_9
R_8	18	47	AB_8
R_7	19	46	OD
R_6	20	45	$\overline{CS}$
R_5	21	44	$\overline{WR}$
R_4	22	43	AB_4
R_3	23	42	V_{CC} (+5V)
R_2	24	41	AB_7
R_1	25	40	AB_6
R_0	26	39	AB_5
TEST 1	27	38	AB_3
X_2	28	37	AB_2
X_1	29	36	AB_1
NC	30	35	AB_0
NC	31	34	NC
GND	32	33	GND

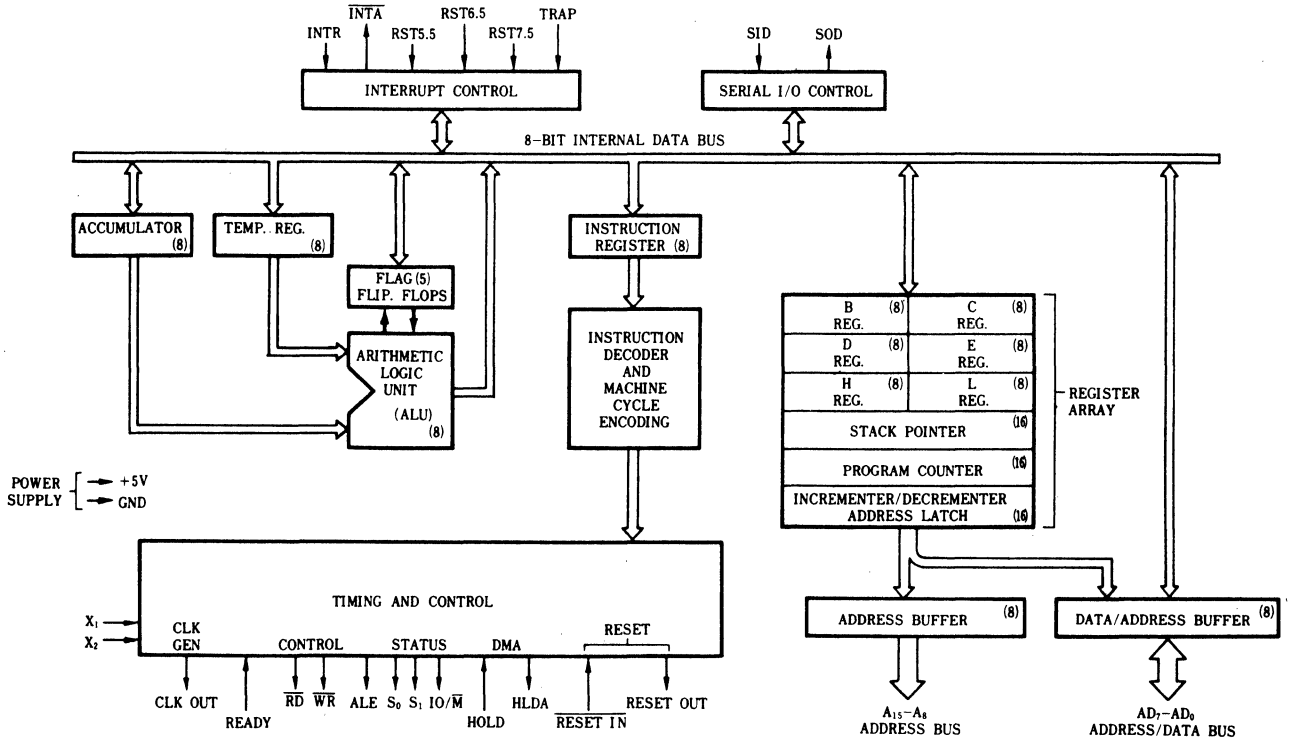
C86

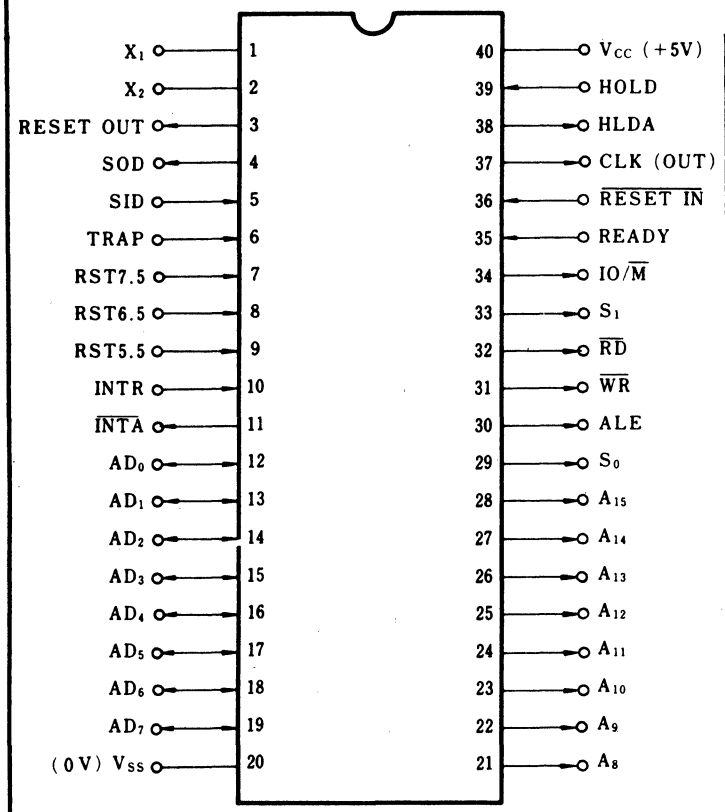
(Top View)

CL_1	1	28	CL_0
PC_0	2	27	V_{GG} (−10V)
PC_1	3	26	RES
PC_2	4	25	$\overline{INT}$
PC_3	5	24	PA_3
PD_0	6	23	PA_2
PD_1	7	22	PA_1
PD_2	8	21	PA_0
PD_3	9	20	PG_0
PE_0	10	19	PF_3
PE_1	11	18	PF_2
PE_2	12	17	PF_1
PE_3	13	16	PF_0
(0V) V_{SS}	14	15	TEST



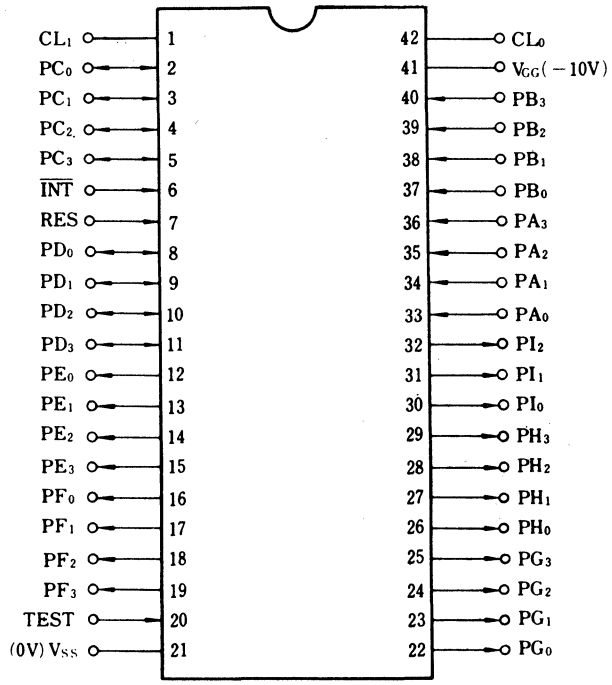
C87



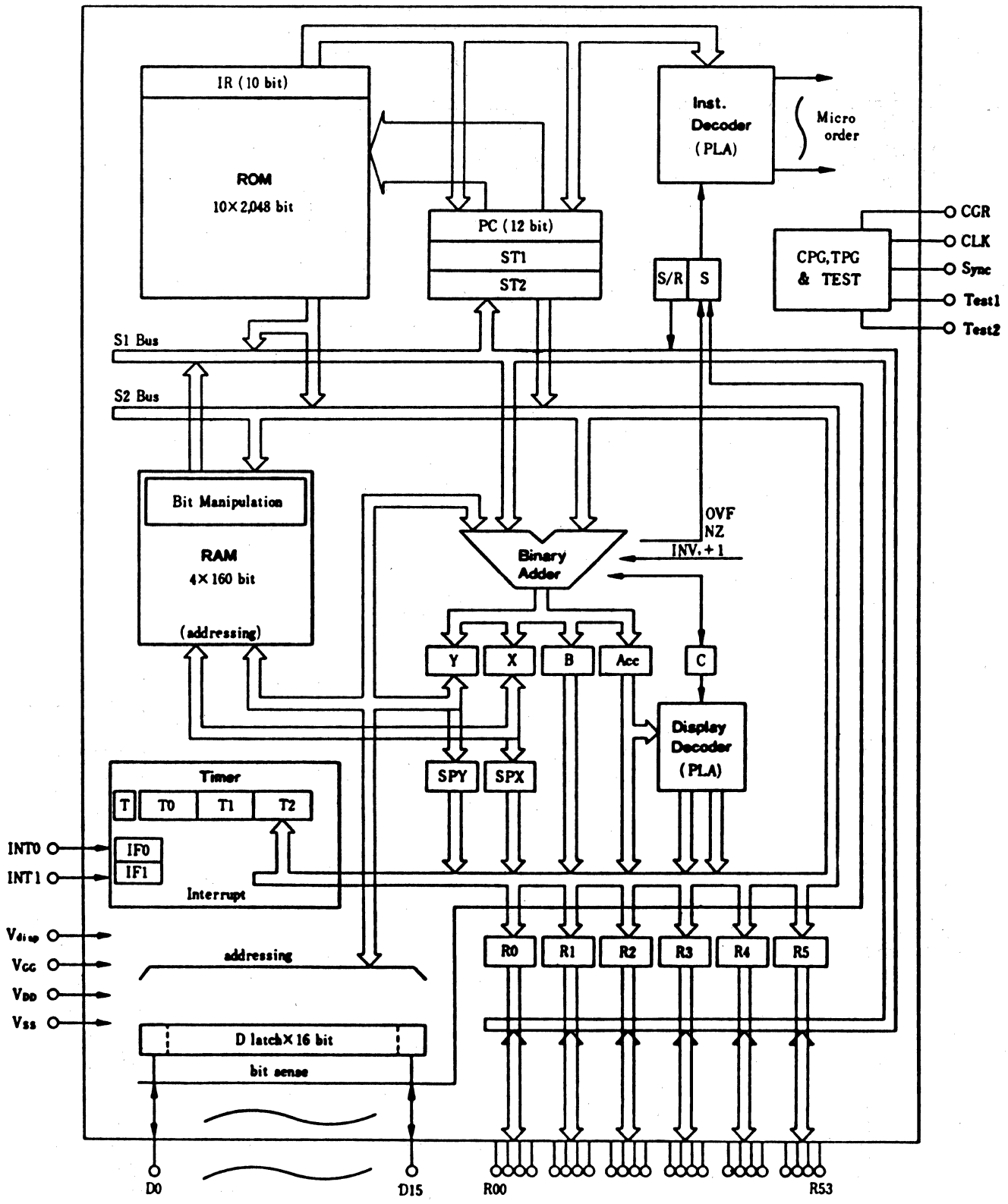


C88

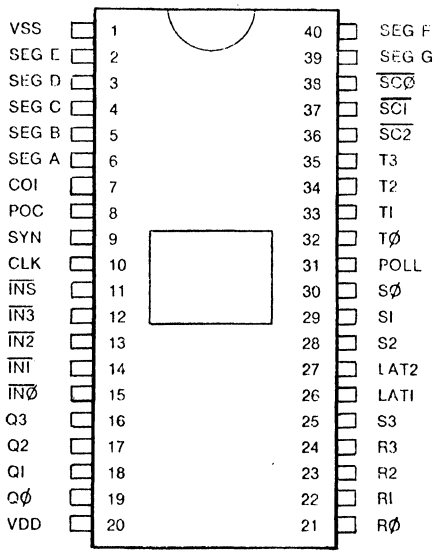
(Top View)



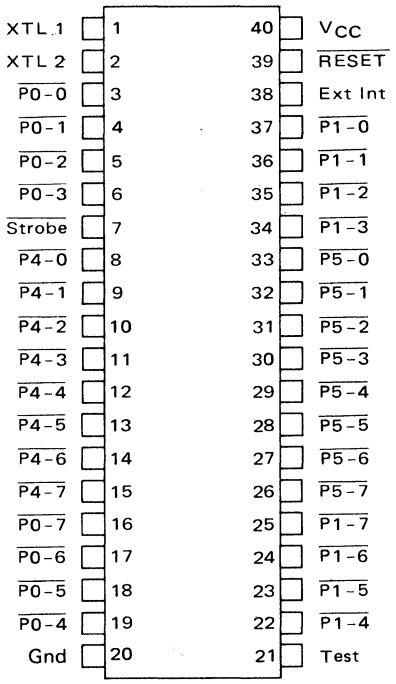
C90


IR (10 bit)
ROM
10×2,048 bit
Inst.
Decoder
(PLA)
Micro
order
PC (12 bit)
ST1
ST2
S/R
S
CPG,TPG
& TEST
CGR
CLK
Sync
Test1
Test2
S1 Bus
S2 Bus
Bit Manipulation
RAM
4×160 bit
(addressing)
OVF
NZ
INV, +1
Binary
Adder
Y
X
B
Acc
C
Display
Decoder
(PLA)
SPY
SPX
Timer
T
T0
T1
T2
IF0
IF1
Interrupt
INT0
INT1
Vdisp
Vcc
VDD
Vss
addressing
R0
R1
R2
R3
R4
R5
D latch×16 bit
bit sense
D0
D15
R00
R53

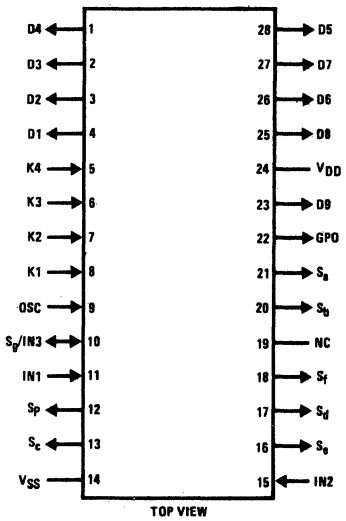
C91



C94



C95

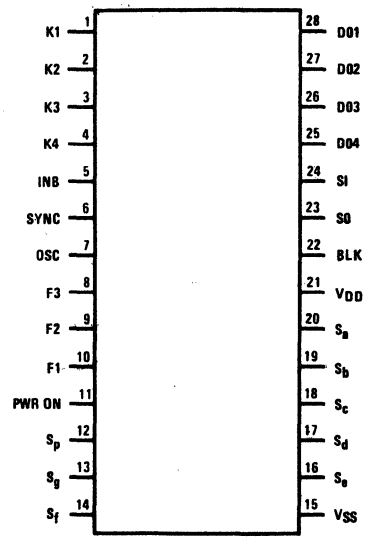


TOP VIEW

Pin Descriptions

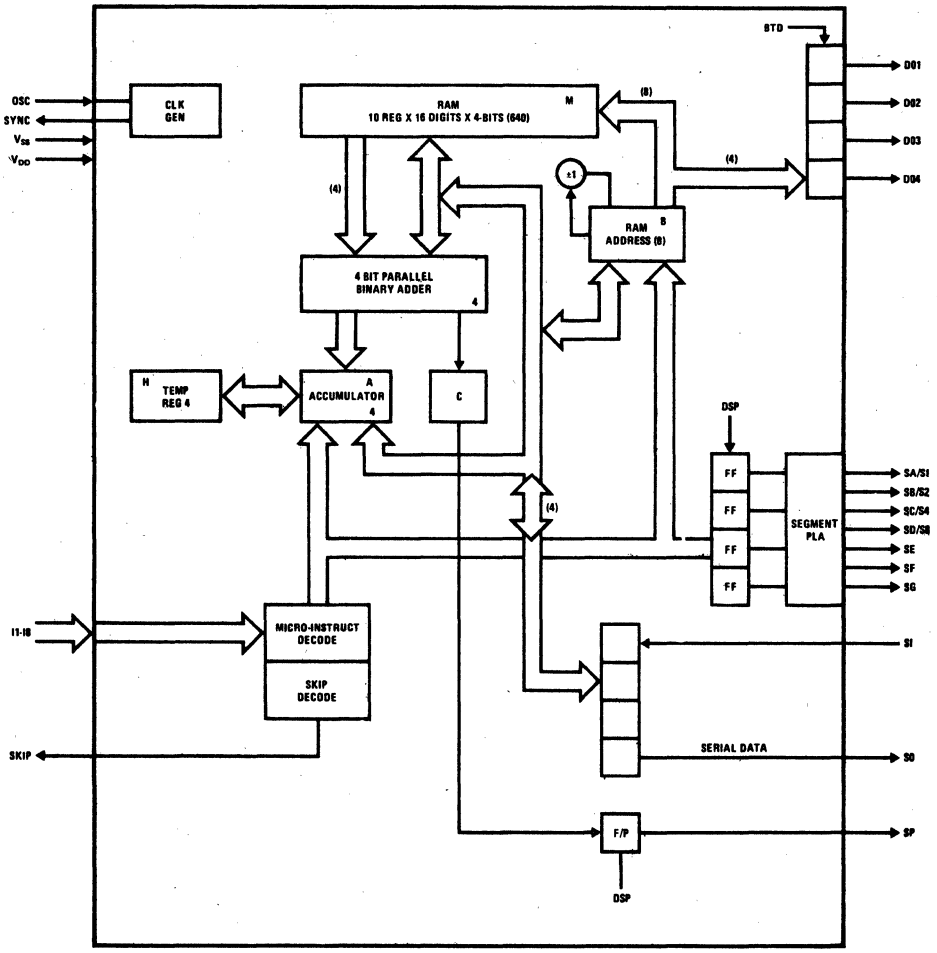
K1–K4	Keyboard Inputs
IN1, IN2, IN3	General Purpose Inputs
OSC	Programmable as External Oscillator
D1–D9	Digit Outputs
S_a–S_g	Segment Outputs
Sp	Decimal Point Segment Output
GPO	General Purpose Output
V_{DD}	–9 Volts
V_{SS}	0 Volts

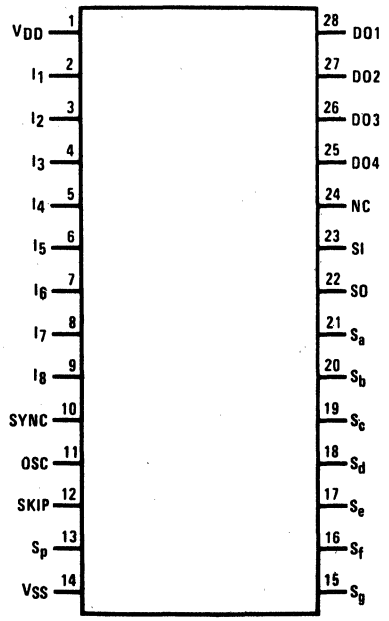
C96



TOP VIEW

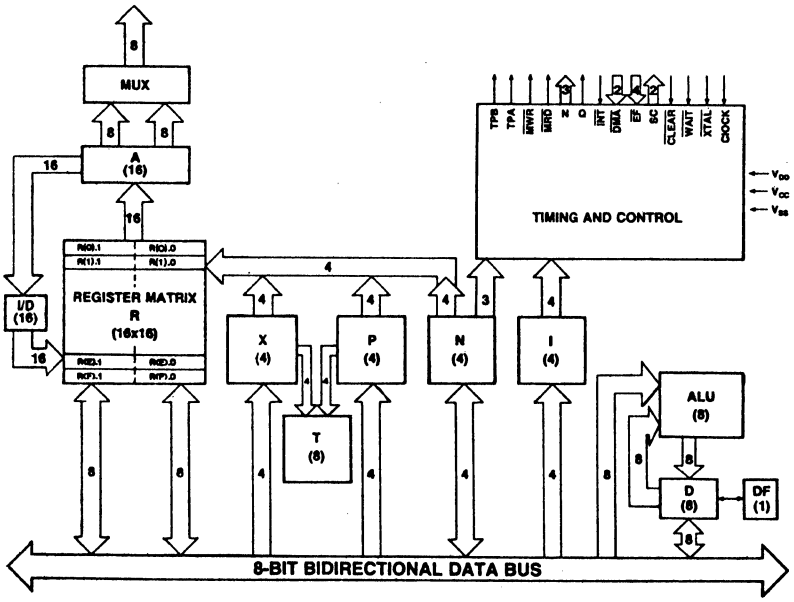
C97


OSC
SYNC
V_{SS}
V_{DD}
CLK GEN
RAM
10 REG X 16 DIGITS X 4-BITS (640)
M
(8)
(4)
±1
RAM ADDRESS (B)
B
4 BIT PARALLEL BINARY ADDER
4
H
TEMP REG 4
A
ACCUMULATOR
4
C
STD
DO1
DO2
DO3
DO4
DSP
FF
FF
FF
FF
SEGMENT PLA
SA/S1
SB/S2
SC/S4
SD/S8
SE
SF
SG
I1-I8
MICRO-INSTRUCT DECODE
SKIP DECODE
SKIP
SI
SERIAL DATA
SO
F/P
SP
DSP

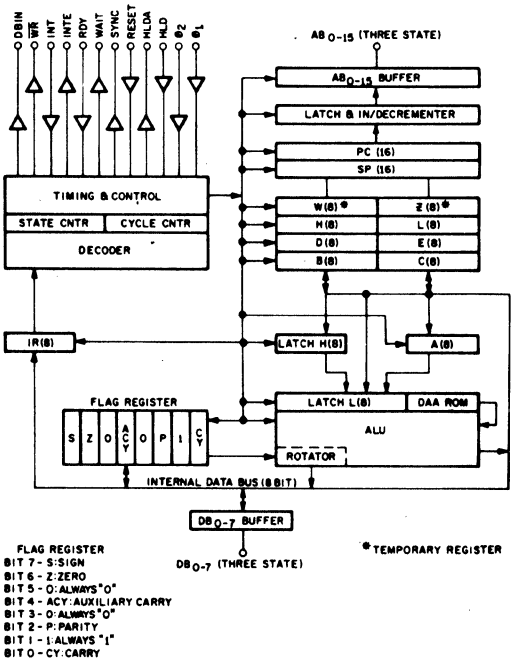

V_{DD} 1
I_1 2
I_2 3
I_3 4
I_4 5
I_5 6
I_6 7
I_7 8
I_8 9
SYNC 10
OSC 11
SKIP 12
S_p 13
V_{SS} 14
28 DO1
27 DO2
26 DO3
25 DO4
24 NC
23 SI
22 SO
21 S_a
20 S_b
19 S_c
18 S_d
17 S_e
16 S_f
15 S_g

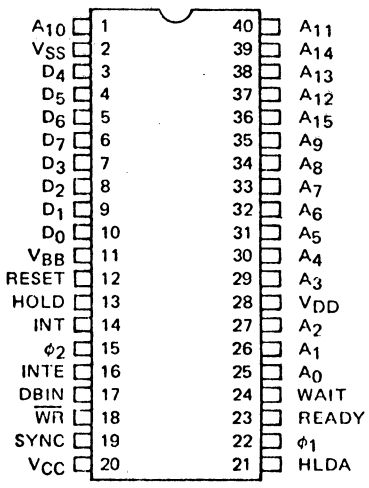
TOP VIEW

C98

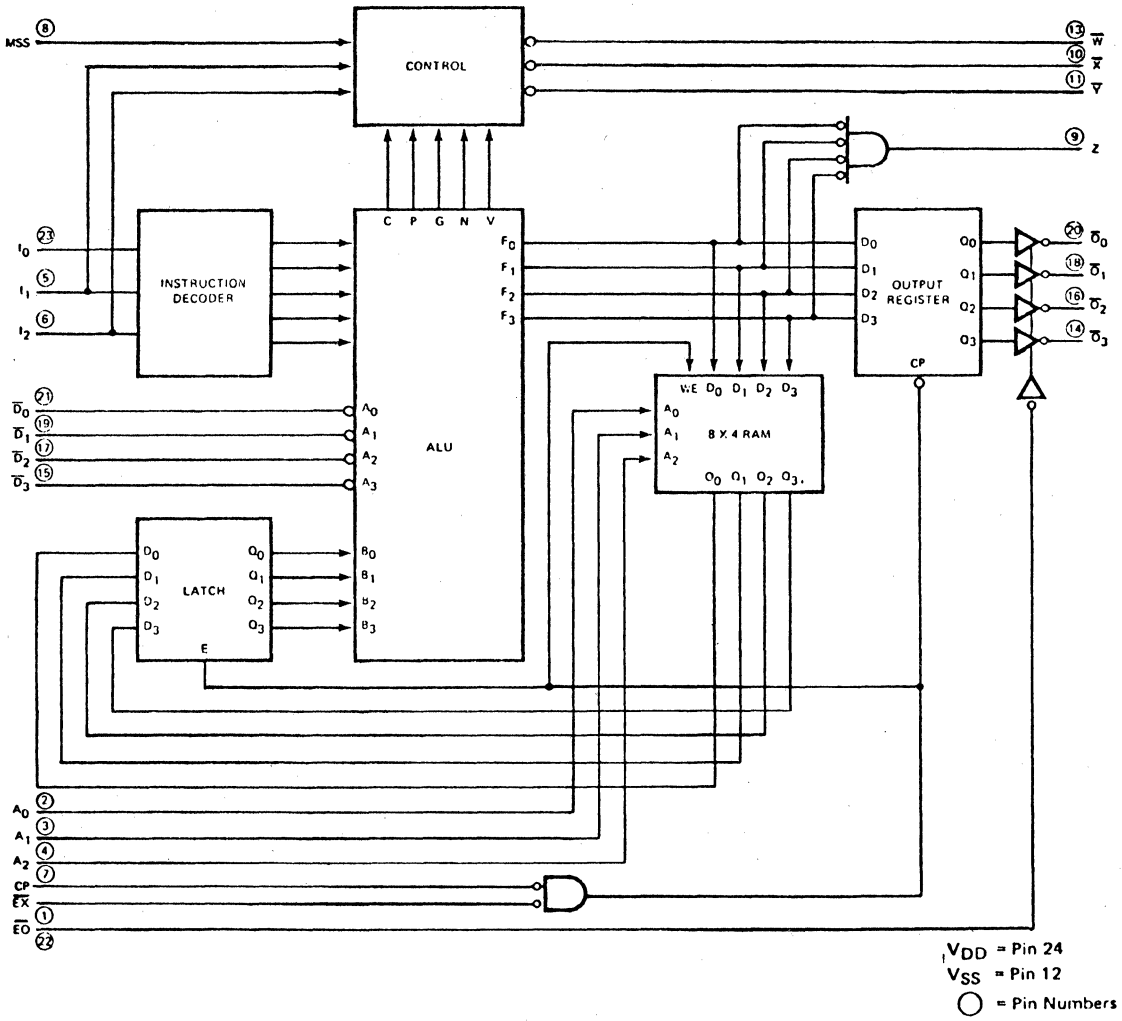

MUX
A (16)
REGISTER MATRIX R (16x16)
I/D (16)
X (4)
P (4)
N (4)
I (4)
T (8)
ALU (8)
D (8)
DF (1)
TIMING AND CONTROL
8-BIT BIDIRECTIONAL DATA BUS

C99

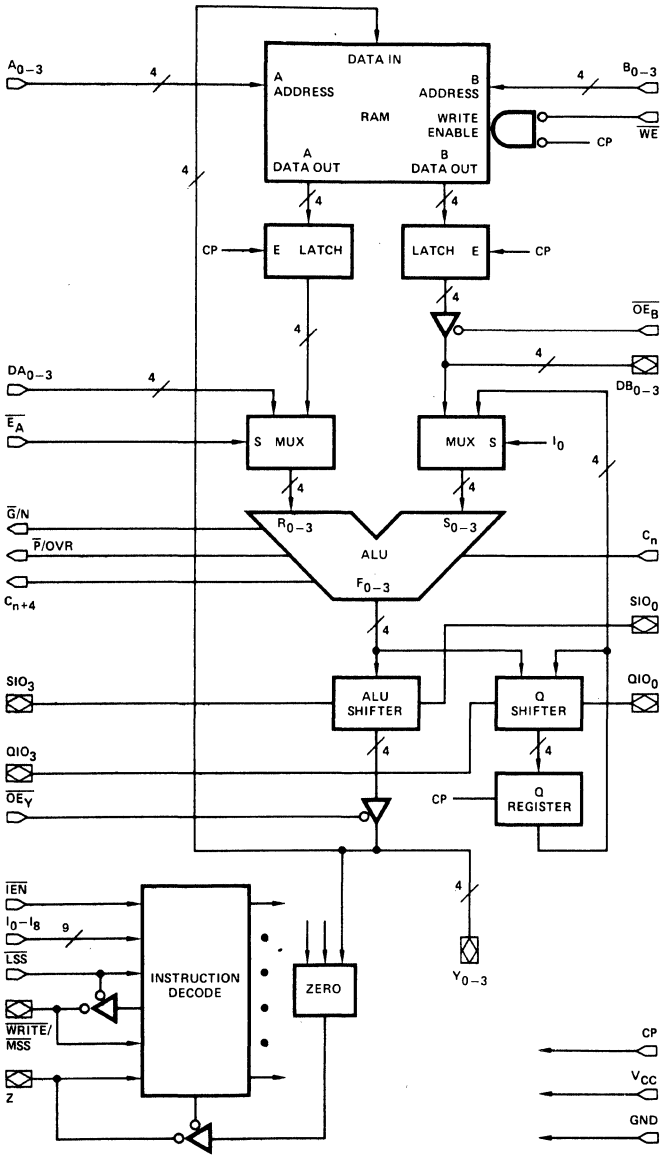

AB0-15 (THREE STATE)
AB0-15 BUFFER
LATCH & IN/DECREMENTER
PC (16)
SP (16)
TIMING & CONTROL
STATE CNTR
CYCLE CNTR
DECODER
W(8)*
Z(8)*
H(8)
L(8)
D(8)
E(8)
B(8)
C(8)
IR(8)
LATCH H(8)
A(8)
FLAG REGISTER
LATCH L(8)
DAA ROM
ALU
ROTATOR
INTERNAL DATA BUS (8 BIT)
DB0-7 BUFFER
DB0-7 (THREE STATE)
*TEMPORARY REGISTER
FLAG REGISTER
BIT 7 - S:SIGN
BIT 6 - Z:ZERO
BIT 5 - 0:ALWAYS "0"
BIT 4 - ACY:AUXILIARY CARRY
BIT 3 - 0:ALWAYS "0"
BIT 2 - P:PARITY
BIT 1 - 1:ALWAYS "1"
BIT 0 - CY:CARRY


A10 1
VSS 2
D4 3
D5 4
D6 5
D7 6
D3 7
D2 8
D1 9
D0 10
VBB 11
RESET 12
HOLD 13
INT 14
ϕ2 15
INTE 16
DBIN 17
WR 18
SYNC 19
VCC 20
40 A11
39 A14
38 A13
37 A12
36 A15
35 A9
34 A8
33 A7
32 A6
31 A5
30 A4
29 A3
28 VDD
27 A2
26 A1
25 A0
24 WAIT
23 READY
22 ϕ1
21 HLDA

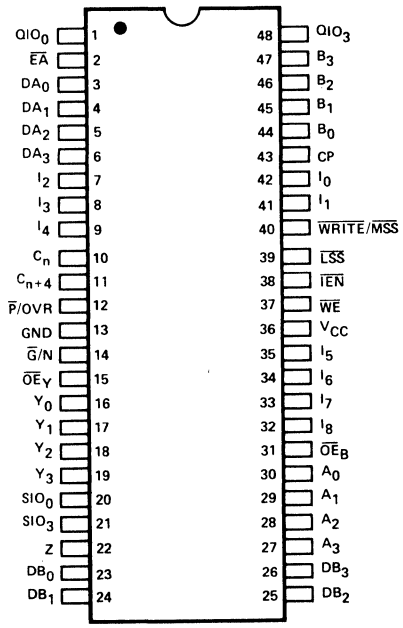
C100


CONTROL
INSTRUCTION DECODER
ALU
C P G N V
LATCH
E
8 X 4 RAM
WE
OUTPUT REGISTER
CP
MSS
I0
I1
I2
A0
A1
A2
CP
EX
EO
W
X
Y
Z
VDD = Pin 24
VSS = Pin 12
= Pin Numbers

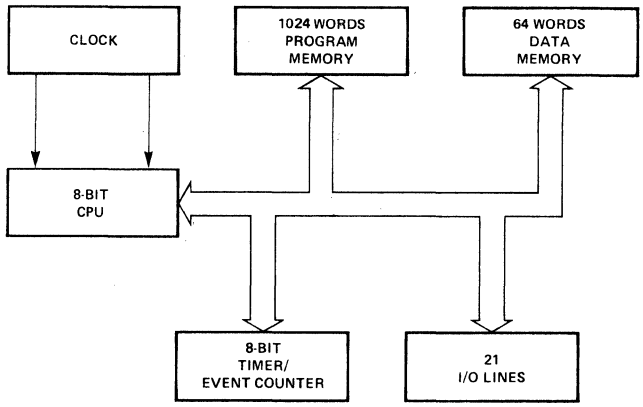
C101

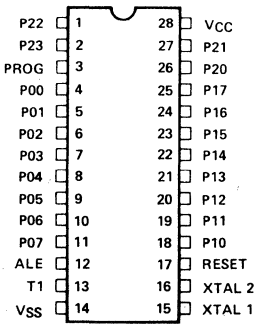


Top View

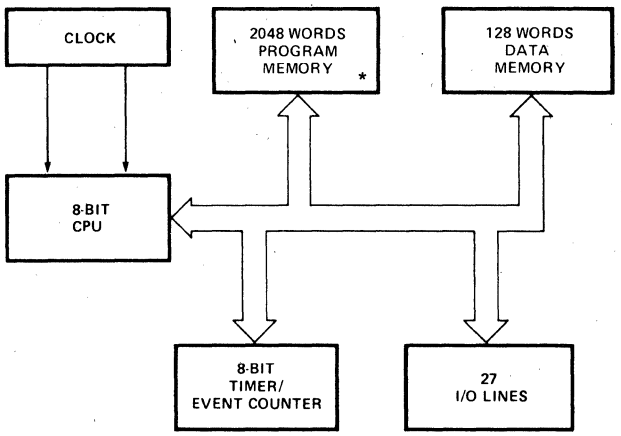


C102

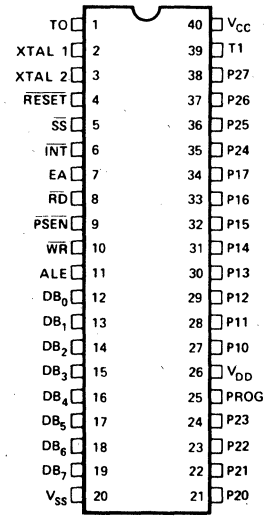




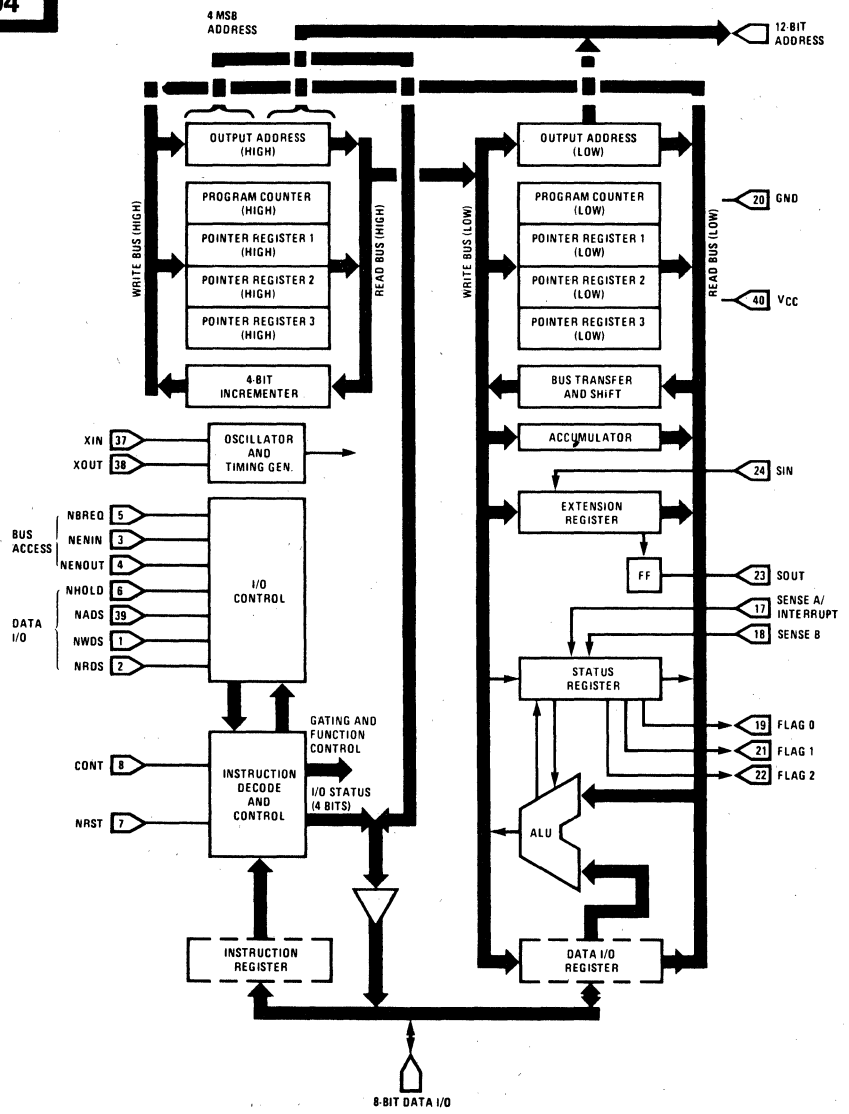
C103

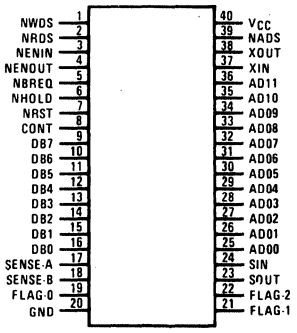


* C103a: WITHOUT PROGRAM MEMORY

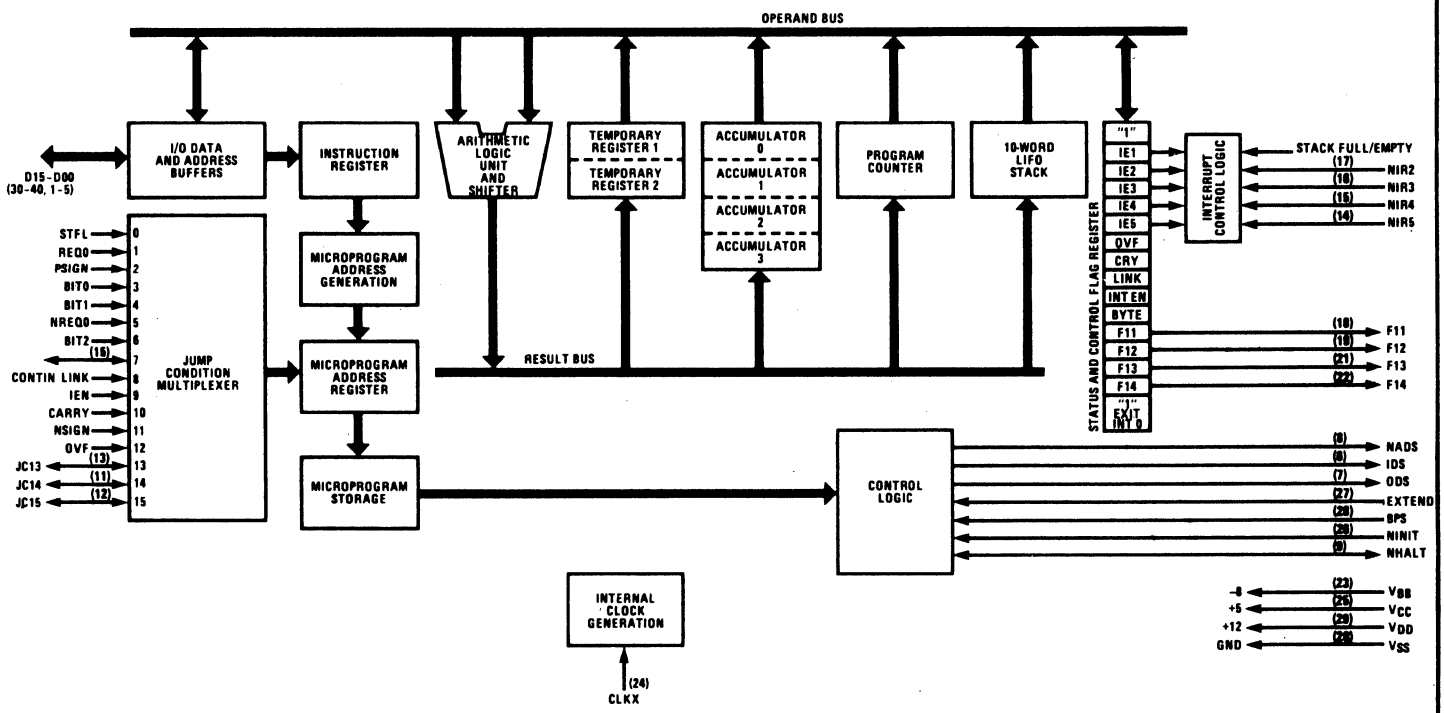


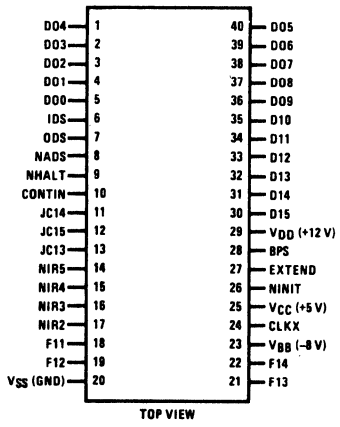
C104





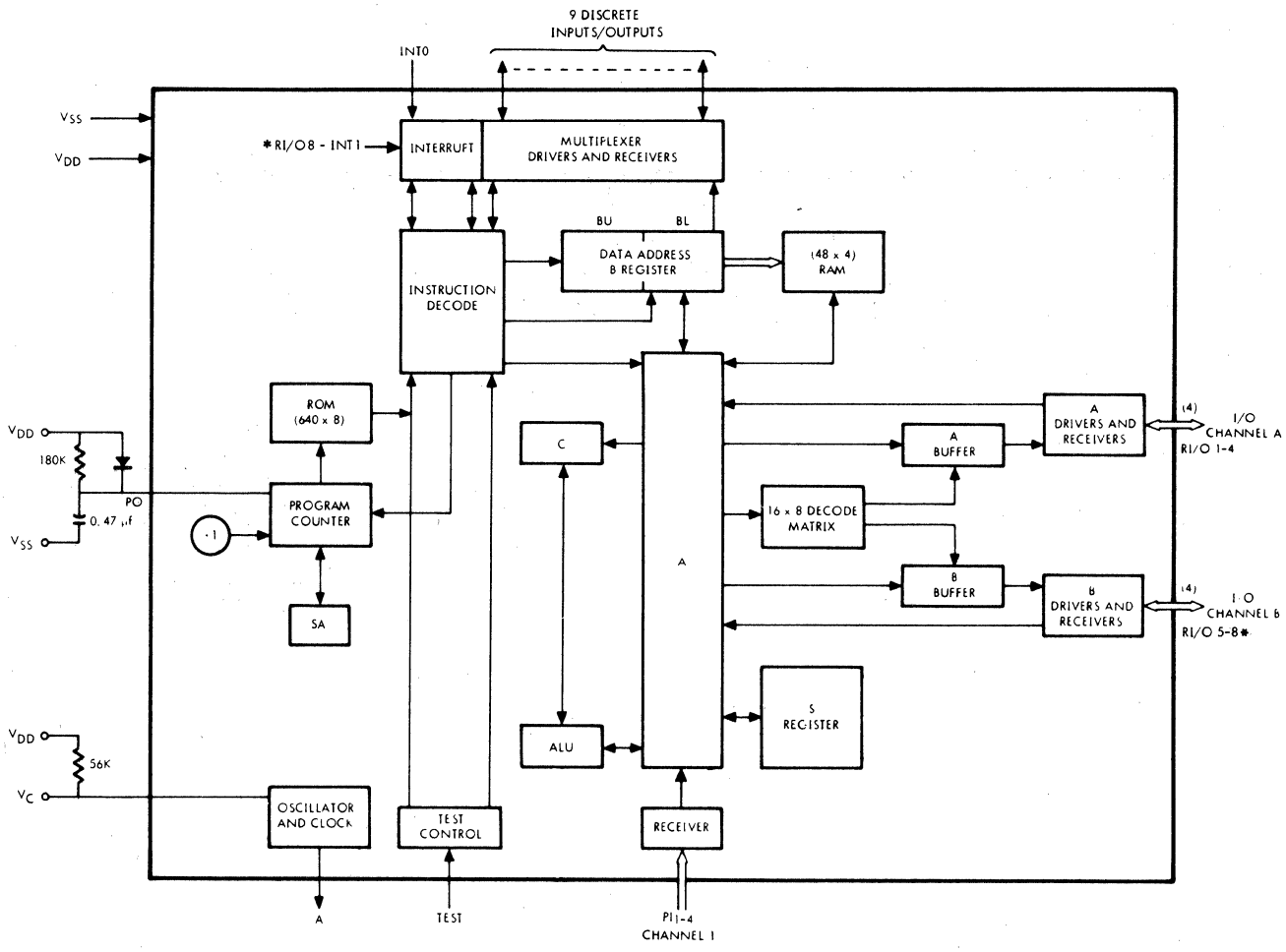
C105

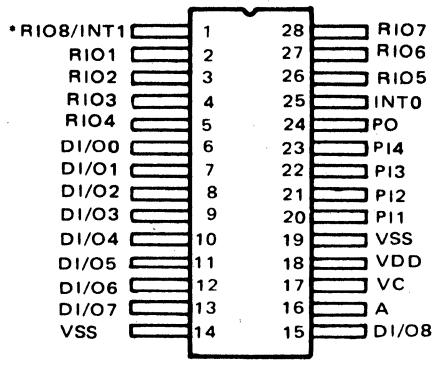




TOP VIEW

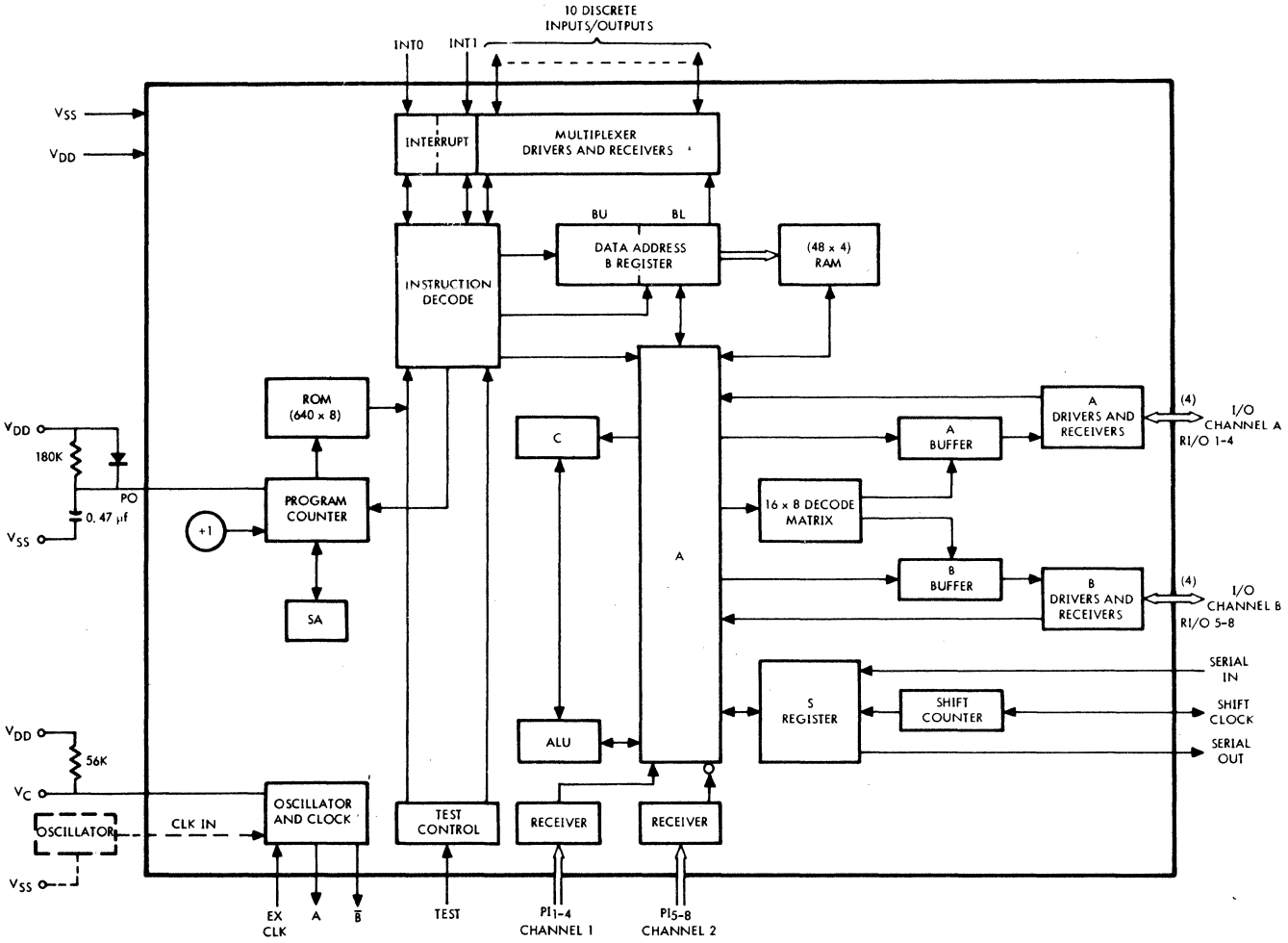
C106

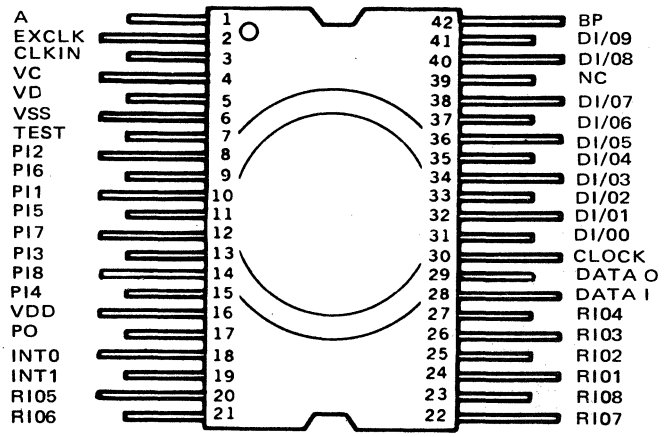




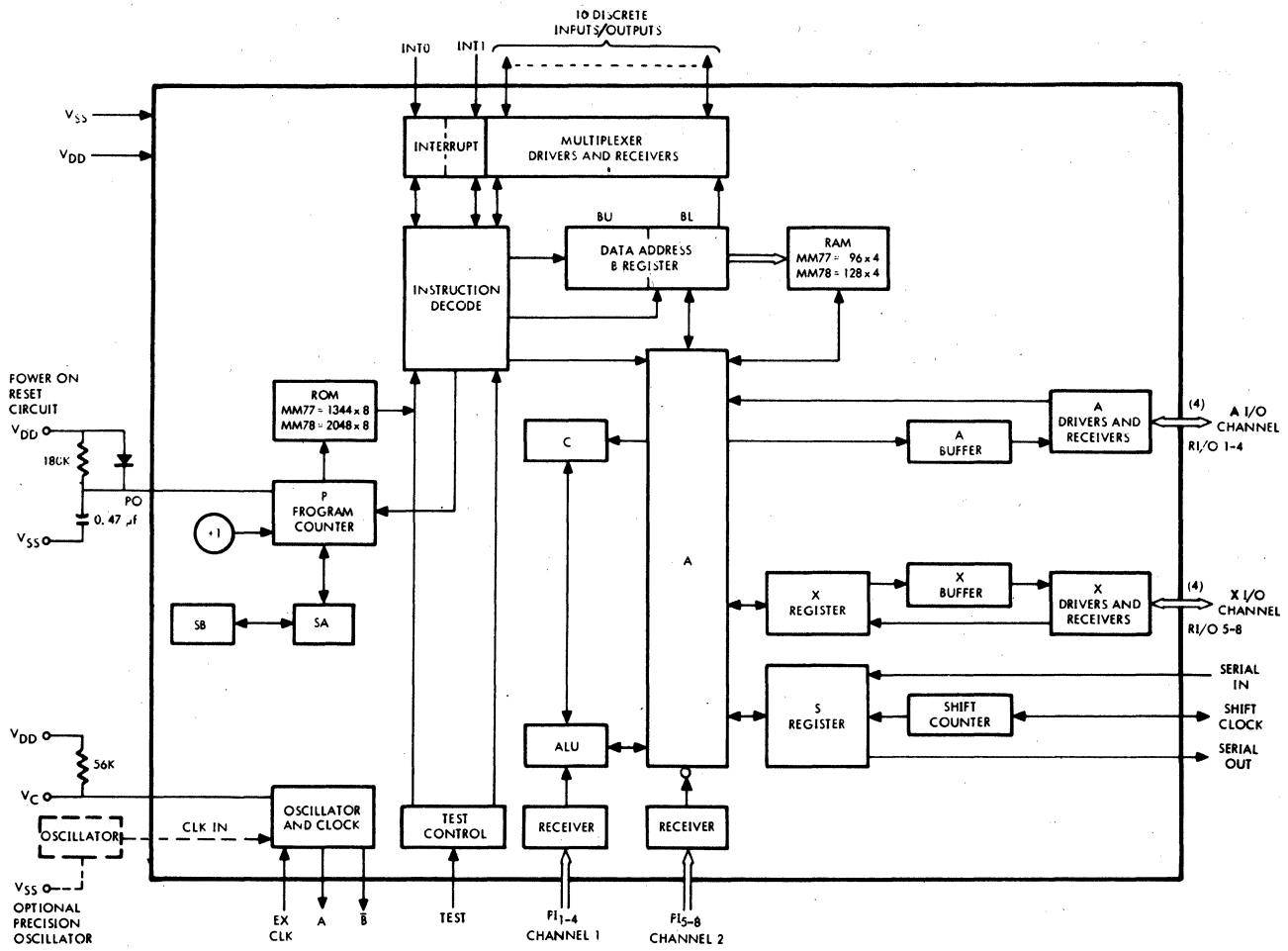
* RIO8=INT1

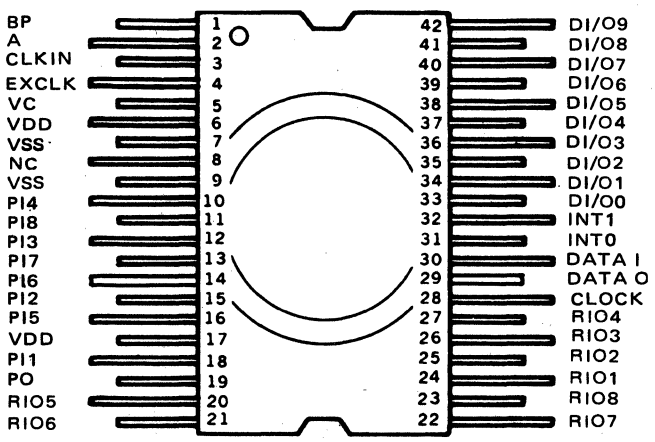
C107


10 DISCRETE INPUTS/OUTPUTS
INT0
INT1
VSS
VDD
INTERRUPT
MULTIPLEXER DRIVERS AND RECEIVERS
BU
BL
DATA ADDRESS B REGISTER
(48 x 4) RAM
INSTRUCTION DECODE
ROM (640 x 8)
PROGRAM COUNTER
+1
SA
C
A
A BUFFER
A DRIVERS AND RECEIVERS
(4)
I/O CHANNEL A
RI/O 1-4
16 x 8 DECODE MATRIX
B BUFFER
B DRIVERS AND RECEIVERS
(4)
I/O CHANNEL B
RI/O 5-8
S REGISTER
SHIFT COUNTER
SERIAL IN
SHIFT CLOCK
SERIAL OUT
ALU
RECEIVER
RECEIVER
TEST CONTROL
OSCILLATOR AND CLOCK
CLK IN
OSCILLATOR
VDD
180K
PO
0.47 µf
56K
VC
EX CLK
A
B
TEST
PI1-4 CHANNEL 1
PI5-8 CHANNEL 2

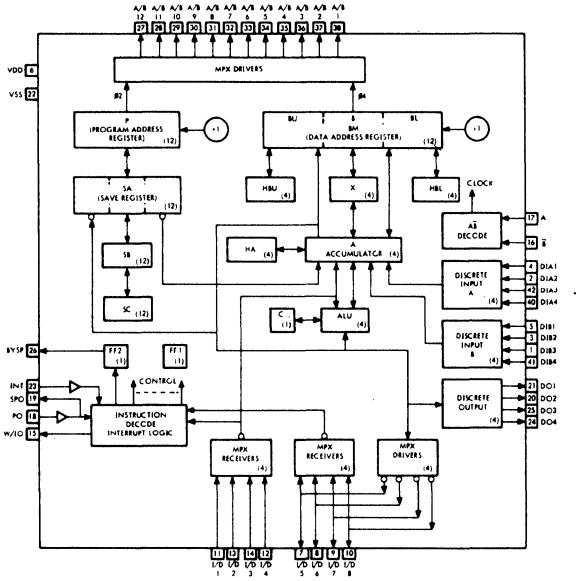

A 1
EXCLK 2
CLKIN 3
VC 4
VD 5
VSS 6
TEST 7
PI2 8
PI6 9
PI1 10
PI5 11
PI7 12
PI3 13
PI8 14
PI4 15
VDD 16
PO 17
INT0 18
INT1 19
RI05 20
RI06 21
42 BP
41 DI/09
40 DI/08
39 NC
38 DI/07
37 DI/06
36 DI/05
35 DI/04
34 DI/03
33 DI/02
32 DI/01
31 DI/00
30 CLOCK
29 DATA O
28 DATA I
27 RI04
26 RI03
25 RI02
24 RI01
23 RI08
22 RI07

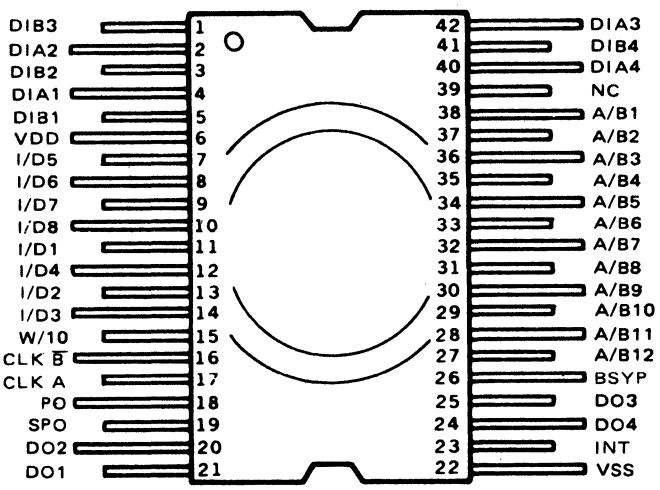
C108


10 DISCRETE INPUTS/OUTPUTS
INT0
INT1
VSS
VDD
INTERRUPT
MULTIPLEXER DRIVERS AND RECEIVERS
BU
BL
DATA ADDRESS B REGISTER
RAM MM77 = 96 x 4 MM78 = 128 x 4
INSTRUCTION DECODE
FOWER ON RESET CIRCUIT
ROM MM77 = 1344 x 8 MM78 = 2048 x 8
C
A
A DRIVERS AND RECEIVERS
(4)
A I/O CHANNEL RI/O 1-4
A BUFFER
P FROGRAM COUNTER
PO
180K
0.47 µf
+1
SB
SA
X REGISTER
X BUFFER
X DRIVERS AND RECEIVERS
(4)
X I/O CHANNEL RI/O 5-8
SERIAL IN
S REGISTER
SHIFT COUNTER
SHIFT CLOCK
SERIAL OUT
ALU
56K
VC
OSCILLATOR
CLK IN
OSCILLATOR AND CLOCK
TEST CONTROL
RECEIVER
RECEIVER
OPTIONAL PRECISION OSCILLATOR
EX CLK
A
B
TEST
FI1-4 CHANNEL 1
FI5-8 CHANNEL 2

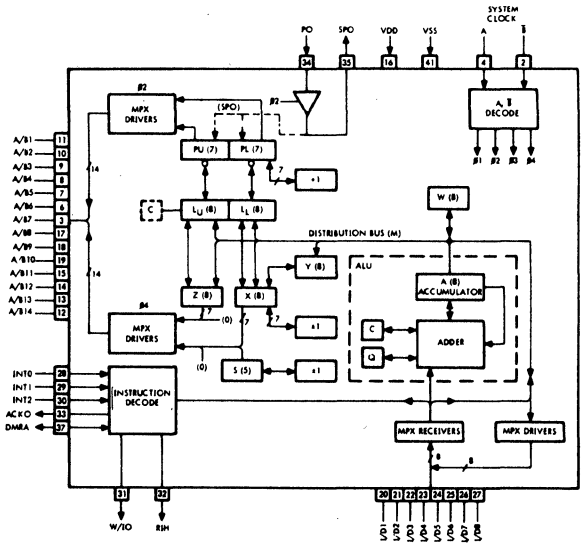

BP 1
A 2
CLKIN 3
EXCLK 4
VC 5
VDD 6
VSS 7
NC 8
VSS 9
PI4 10
PI8 11
PI3 12
PI7 13
PI6 14
PI2 15
PI5 16
VDD 17
PI1 18
PO 19
RIO5 20
RIO6 21
42 DI/O9
41 DI/O8
40 DI/O7
39 DI/O6
38 DI/O5
37 DI/O4
36 DI/O3
35 DI/O2
34 DI/O1
33 DI/O0
32 INT1
31 INT0
30 DATA I
29 DATA O
28 CLOCK
27 RIO4
26 RIO3
25 RIO2
24 RIO1
23 RIO8
22 RIO7

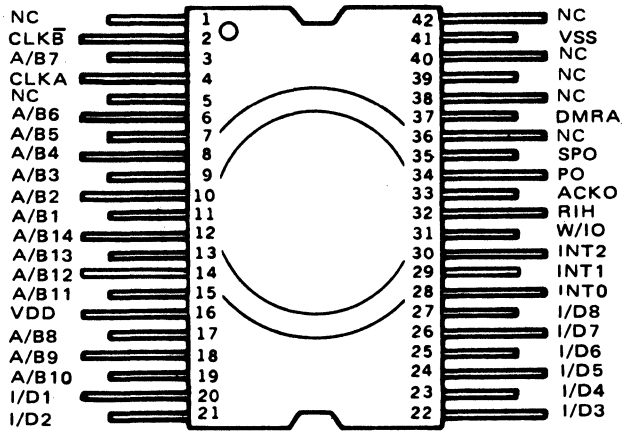
C109


MPX DRIVERS
PROGRAM ADDRESS REGISTER (12)
DATA ADDRESS REGISTER (12)
SA SAVE REGISTER (12)
SB (12)
SC (12)
HBU (4)
X (4)
HBL (4)
CLOCK
HA (4)
ACCUMULATOR (4)
C (1)
ALU (4)
FF2 (1)
FF1 (1)
CONTROL
INSTRUCTION DECODE INTERRUPT LOGIC
MPX RECEIVERS (4)
MPX RECEIVERS (4)
MPX DRIVERS (4)
DISCRETE INPUT A (4)
DISCRETE INPUT B (4)
DISCRETE OUTPUT (4)

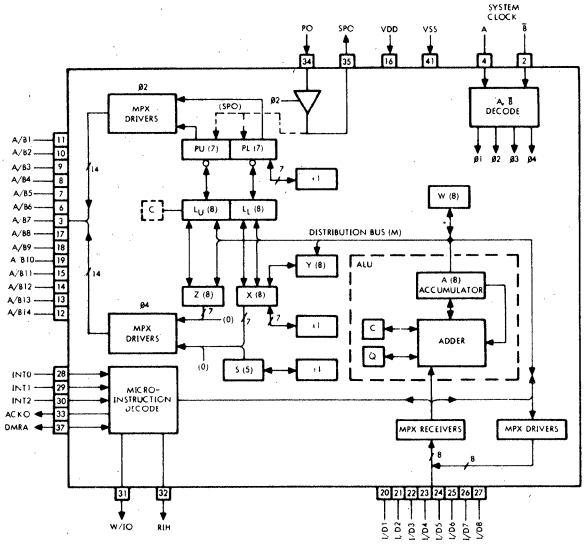

DIB3 1
DIA2 2
DIB2 3
DIA1 4
DIB1 5
VDD 6
I/D5 7
I/D6 8
I/D7 9
I/D8 10
I/D1 11
I/D4 12
I/D2 13
I/D3 14
W/10 15
CLK B 16
CLK A 17
PO 18
SPO 19
DO2 20
DO1 21
42 DIA3
41 DIB4
40 DIA4
39 NC
38 A/B1
37 A/B2
36 A/B3
35 A/B4
34 A/B5
33 A/B6
32 A/B7
31 A/B8
30 A/B9
29 A/B10
28 A/B11
27 A/B12
26 BSYP
25 DO3
24 DO4
23 INT
22 VSS

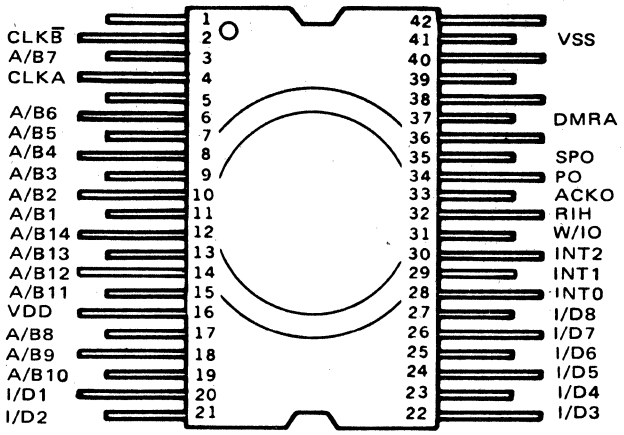
C110


SYSTEM CLOCK
PO
SPO
VDD
VSS
MPX DRIVERS
A, B DECODE
PU (7)
PL (7)
LU (8)
LL (8)
W (8)
DISTRIBUTION BUS (M)
Y (8)
Z (8)
X (8)
ALU
A (8) ACCUMULATOR
ADDER
S (5)
INSTRUCTION DECODE
MPX RECEIVERS
MPX DRIVERS
W/IO
RIH

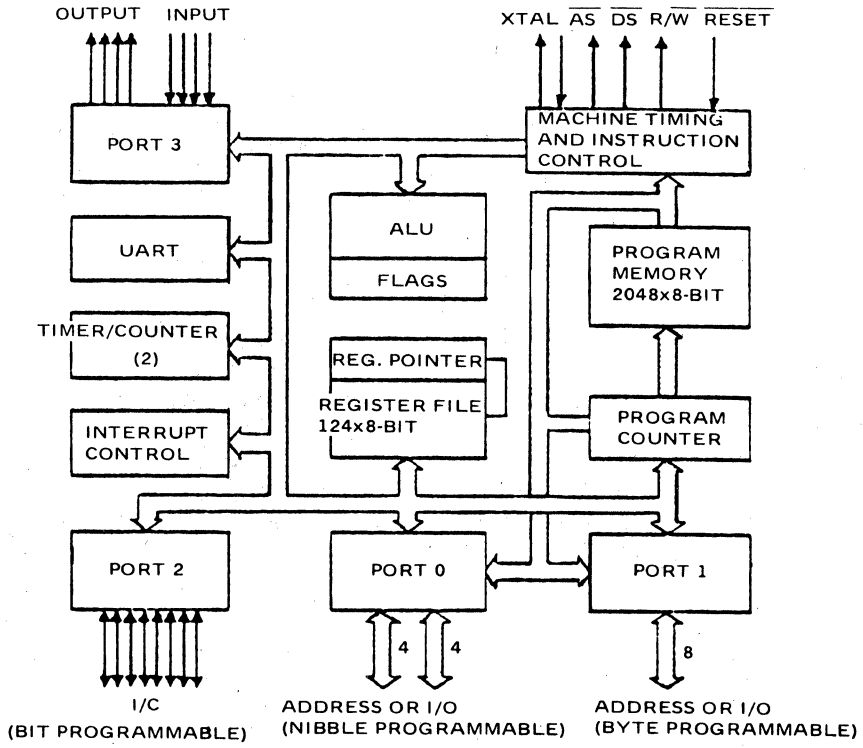

NC 1
CLKB 2
A/B7 3
CLKA 4
NC 5
A/B6 6
A/B5 7
A/B4 8
A/B3 9
A/B2 10
A/B1 11
A/B14 12
A/B13 13
A/B12 14
A/B11 15
VDD 16
A/B8 17
A/B9 18
A/B10 19
I/D1 20
I/D2 21
42 NC
41 VSS
40 NC
39 NC
38 NC
37 DMRA
36 NC
35 SPO
34 PO
33 ACKO
32 RIH
31 W/IO
30 INT2
29 INT1
28 INT0
27 I/D8
26 I/D7
25 I/D6
24 I/D5
23 I/D4
22 I/D3

C111

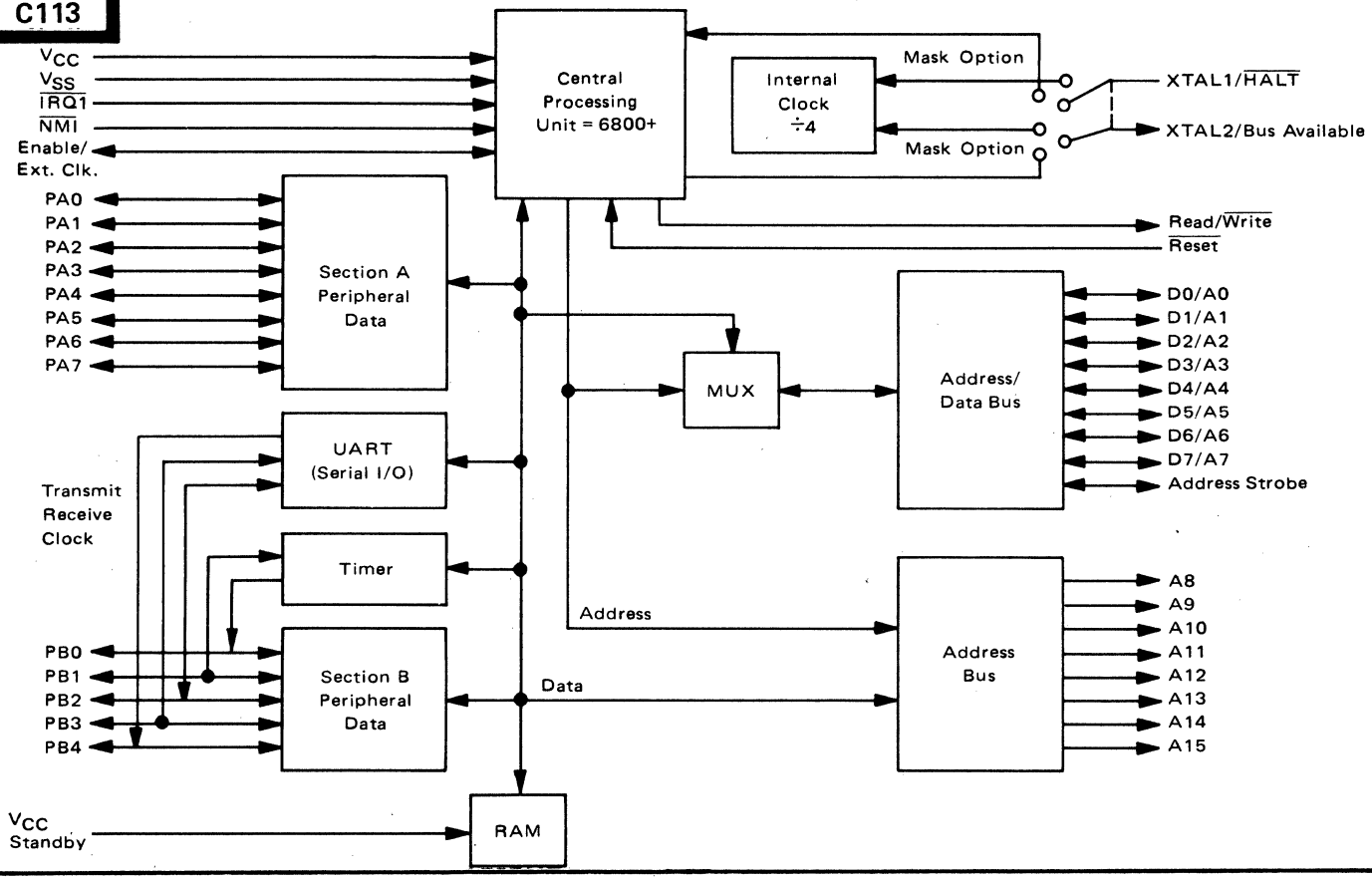

SYSTEM CLOCK
PO
SPO
VDD
VSS
MPX DRIVERS
A, B DECODE
PU (7)
PL (7)
W (8)
DISTRIBUTION BUS (M)
Y (8)
ALU
A (8) ACCUMULATOR
Z (8)
X (8)
C
Q
ADDER
S (5)
MICRO-INSTRUCTION DECODE
MPX RECEIVERS
MPX DRIVERS
INT0
INT1
INT2
ACKO
DMRA
W/IO
RIH


CLKB
A/B7
CLKA
A/B6
A/B5
A/B4
A/B3
A/B2
A/B1
A/B14
A/B13
A/B12
A/B11
VDD
A/B8
A/B9
A/B10
I/D1
I/D2
VSS
DMRA
SPO
PO
ACKO
RIH
W/IO
INT2
INT1
INT0
I/D8
I/D7
I/D6
I/D5
I/D4
I/D3

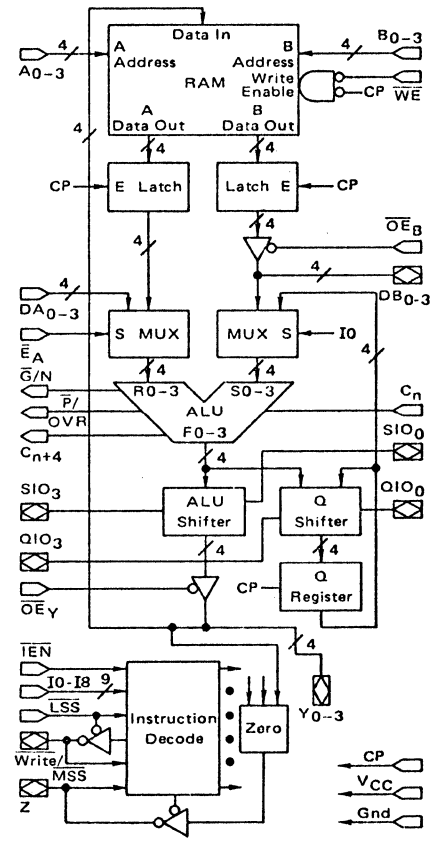
C112

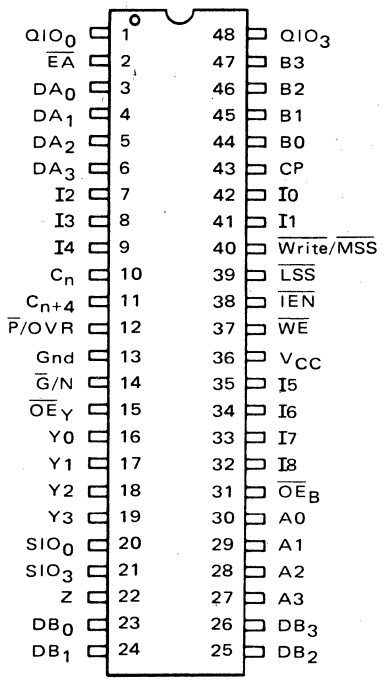

OUTPUT
INPUT
XTAL
AS
DS
R/W
RESET
PORT 3
MACHINE TIMING AND INSTRUCTION CONTROL
UART
ALU
FLAGS
PROGRAM MEMORY 2048x8-BIT
TIMER/COUNTER (2)
REG. POINTER
REGISTER FILE 124x8-BIT
PROGRAM COUNTER
INTERRUPT CONTROL
PORT 2
PORT 0
PORT 1
4
4
8
I/C
(BIT PROGRAMMABLE)
ADDRESS OR I/O
(NIBBLE PROGRAMMABLE)
ADDRESS OR I/O
(BYTE PROGRAMMABLE)

C113

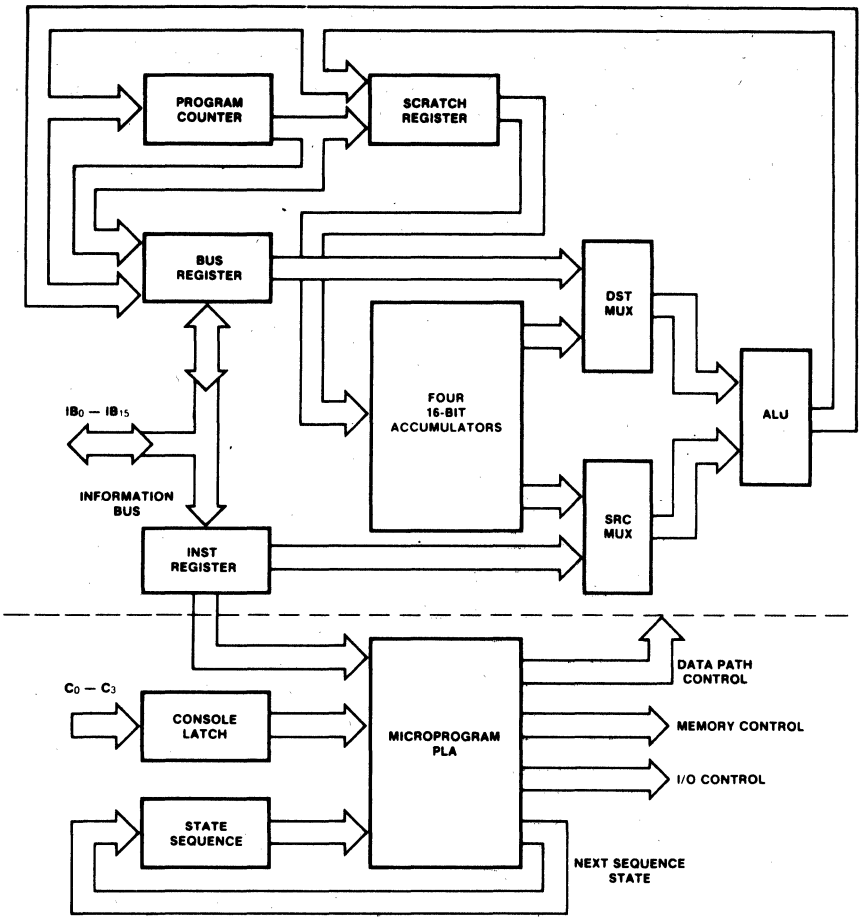

VCC
VSS
IRQ1
NMI
Enable/
Ext. Clk.
Central Processing Unit = 6800+
Internal Clock ÷4
Mask Option
Mask Option
XTAL1/HALT
XTAL2/Bus Available
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
Section A Peripheral Data
Read/Write
Reset
MUX
Address/ Data Bus
D0/A0
D1/A1
D2/A2
D3/A3
D4/A4
D5/A5
D6/A6
D7/A7
Address Strobe
UART (Serial I/O)
Transmit
Receive
Clock
Timer
Address
Address Bus
A8
A9
A10
A11
A12
A13
A14
A15
PB0
PB1
PB2
PB3
PB4
Section B Peripheral Data
Data
VCC Standby
RAM

C114

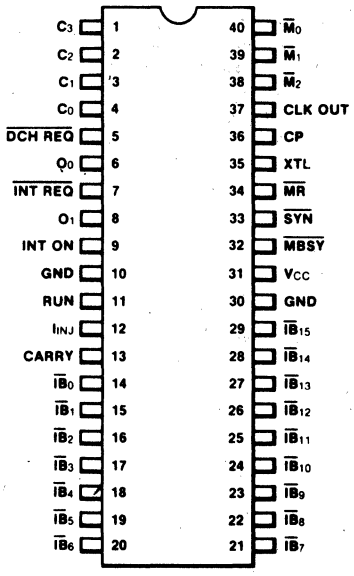

Data In
A Address
B Address
RAM
Write Enable
CP
WE
A Data Out
B Data Out
A0-3
B0-3
E Latch
Latch E
OEB
DA0-3
DB0-3
S MUX
MUX S
I0
EA
G/N
P/OVR
R0-3
S0-3
ALU
F0-3
Cn
Cn+4
SIO0
SIO3
QIO0
QIO3
ALU Shifter
Q Shifter
Q Register
OEY
IEN
I0-I8
LSS
Write/
MSS
Z
Instruction Decode
Zero
Y0-3
VCC
Gnd


QIO0 1
EA 2
DA0 3
DA1 4
DA2 5
DA3 6
I2 7
I3 8
I4 9
Cn 10
Cn+4 11
P/OVR 12
Gnd 13
G/N 14
OEY 15
Y0 16
Y1 17
Y2 18
Y3 19
SIO0 20
SIO3 21
Z 22
DB0 23
DB1 24
48 QIO3
47 B3
46 B2
45 B1
44 B0
43 CP
42 I0
41 I1
40 Write/MSS
39 LSS
38 IEN
37 WE
36 VCC
35 I5
34 I6
33 I7
32 I8
31 OEB
30 A0
29 A1
28 A2
27 A3
26 DB3
25 DB2

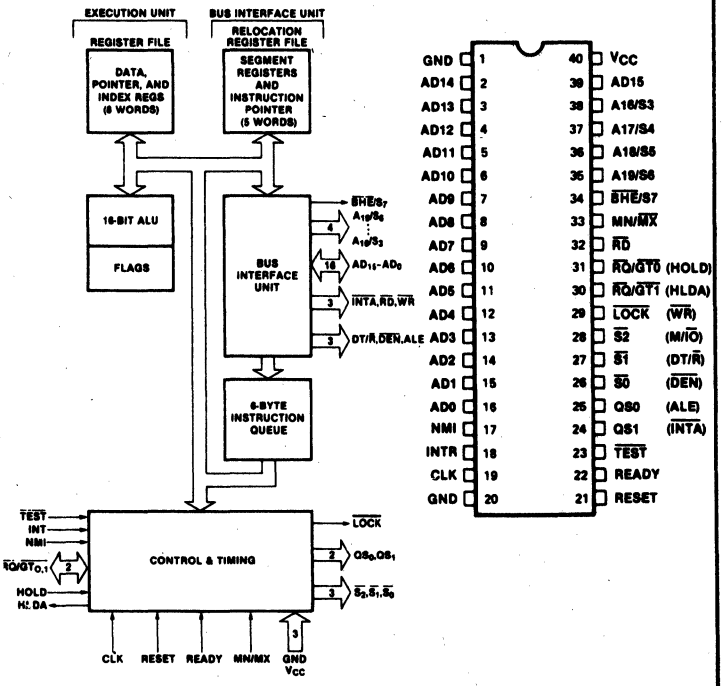
C115



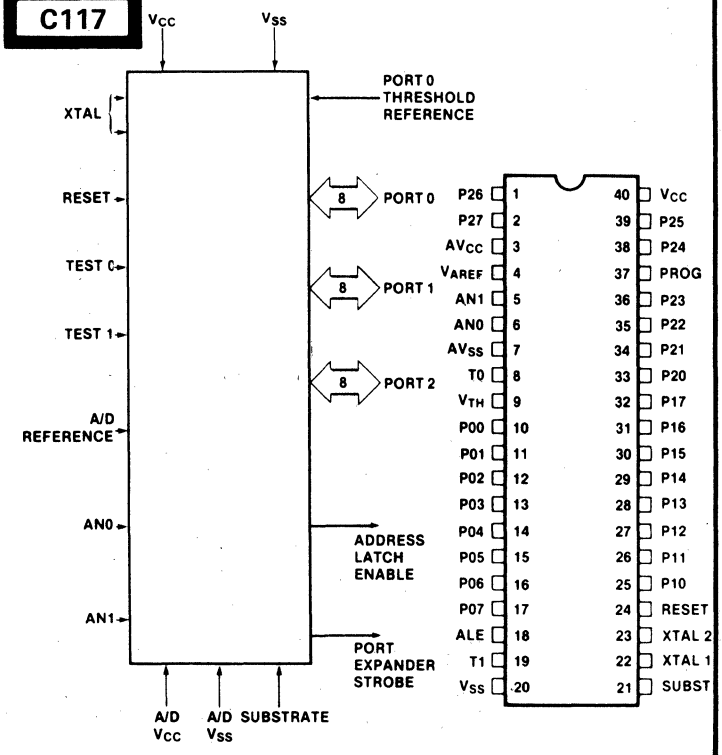
(TOP VIEW)



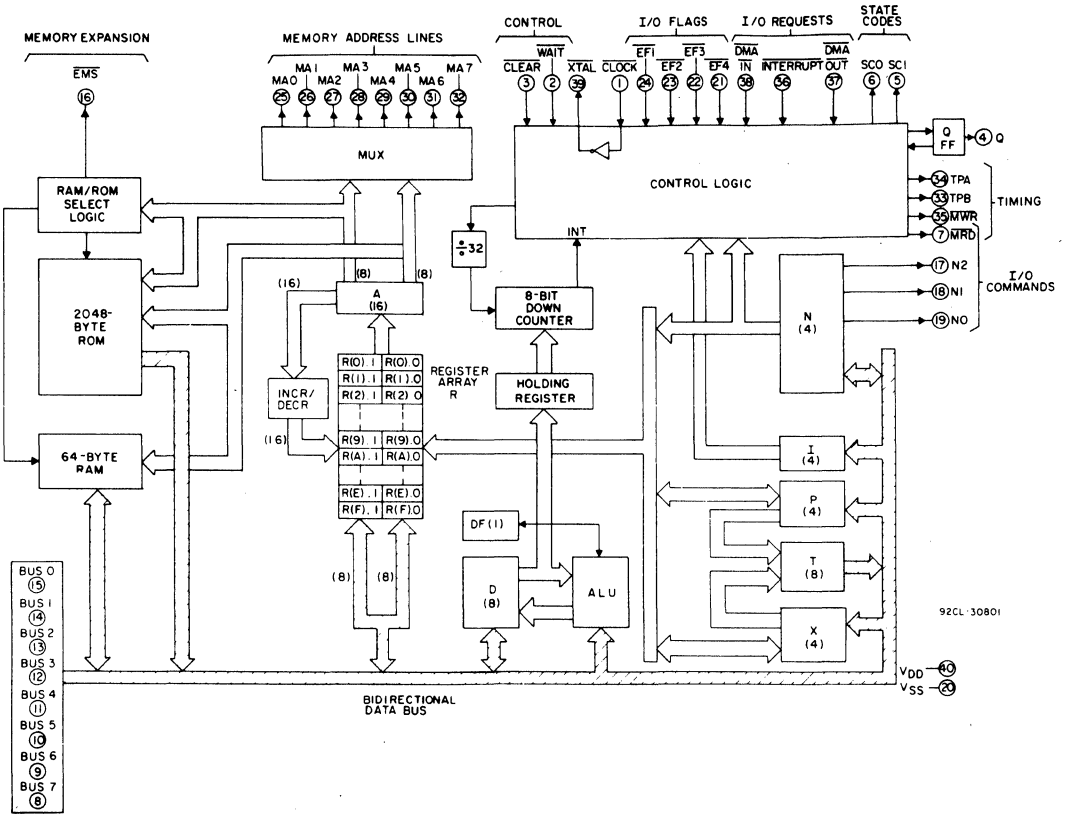
C116



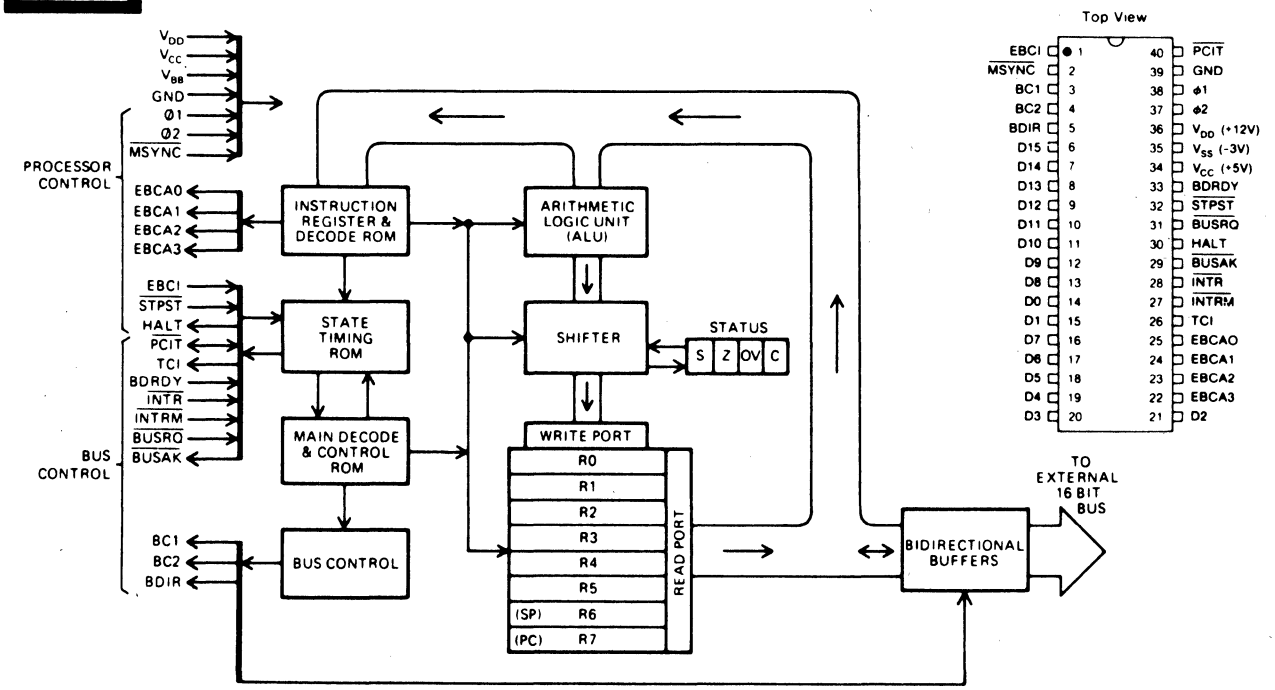
C117



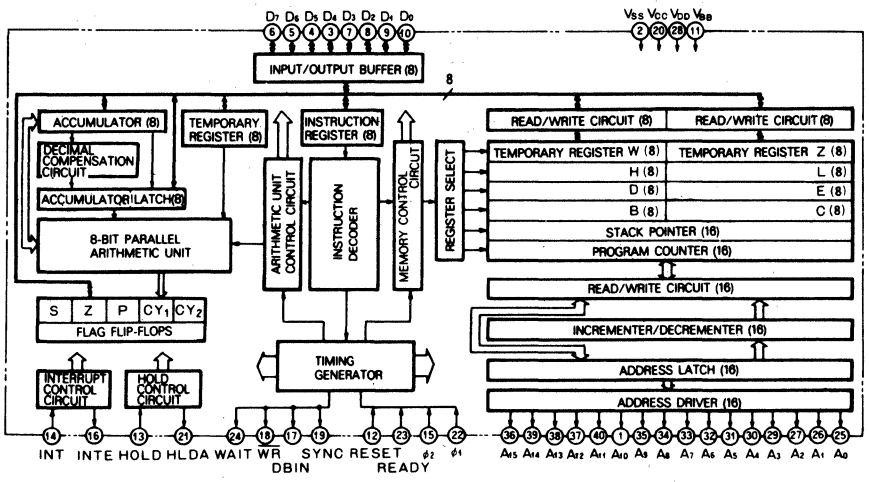
C118


MEMORY EXPANSION
EMS
MEMORY ADDRESS LINES
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7
CONTROL
WAIT
CLEAR XTAL
I/O FLAGS
EF1 EF2 EF3 EF4
CLOCK
I/O REQUESTS
DMA IN DMA OUT
INTERRUPT
STATE CODES
SCO SCI
MUX
CONTROL LOGIC
Q FF
Q
TPA
TPB
MWR
MRD
TIMING
INT
÷32
RAM/ROM SELECT LOGIC
2048-BYTE ROM
64-BYTE RAM
A (16)
8-BIT DOWN COUNTER
HOLDING REGISTER
INCR/DECR
REGISTER ARRAY R
R(0).I R(0).O
R(1).I R(1).O
R(2).I R(2).O
R(9).I R(9).O
R(A).I R(A).O
R(E).I R(E).O
R(F).I R(F).O
N (4)
N2
N1
N0
I/O COMMANDS
I (4)
P (4)
T (8)
X (4)
DF(1)
D (8)
ALU
BUS 0
BUS 1
BUS 2
BUS 3
BUS 4
BUS 5
BUS 6
BUS 7
BIDIRECTIONAL DATA BUS
VDD
VSS
92CL-30801

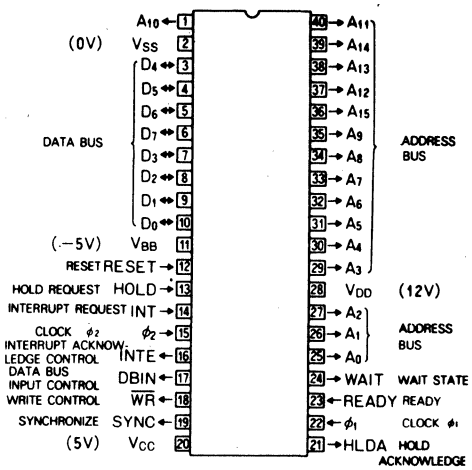
C119


VDD
VCC
VBB
GND
Ø1
Ø2
MSYNC
PROCESSOR CONTROL
EBCA0
EBCA1
EBCA2
EBCA3
EBCI
STPST
HALT
PCIT
TCI
BDRDY
INTR
INTRM
BUSRQ
BUSAK
BUS CONTROL
BC1
BC2
BDIR
INSTRUCTION REGISTER & DECODE ROM
STATE TIMING ROM
MAIN DECODE & CONTROL ROM
BUS CONTROL
ARITHMETIC LOGIC UNIT (ALU)
SHIFTER
STATUS
S Z OV C
WRITE PORT
READ PORT
R0
R1
R2
R3
R4
R5
(SP) R6
(PC) R7
BIDIRECTIONAL BUFFERS
TO EXTERNAL 16 BIT BUS
Top View
EBCI 1
MSYNC 2
BC1 3
BC2 4
BDIR 5
D15 6
D14 7
D13 8
D12 9
D11 10
D10 11
D9 12
D8 13
D0 14
D1 15
D7 16
D6 17
D5 18
D4 19
D3 20
40 PCIT
39 GND
38 Ø1
37 Ø2
36 VDD (+12V)
35 VSS (-3V)
34 VCC (+5V)
33 BDRDY
32 STPST
31 BUSRQ
30 HALT
29 BUSAK
28 INTR
27 INTRM
26 TCI
25 EBCA0
24 EBCA1
23 EBCA2
22 EBCA3
21 D2

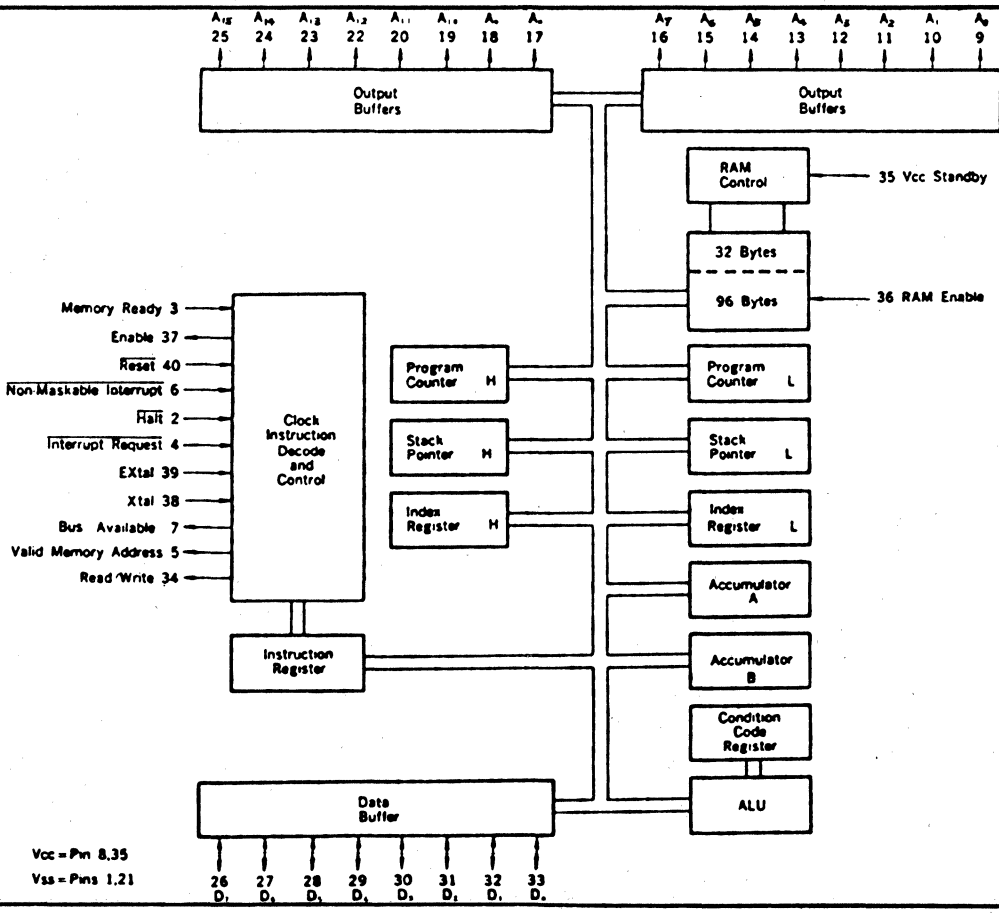
C120



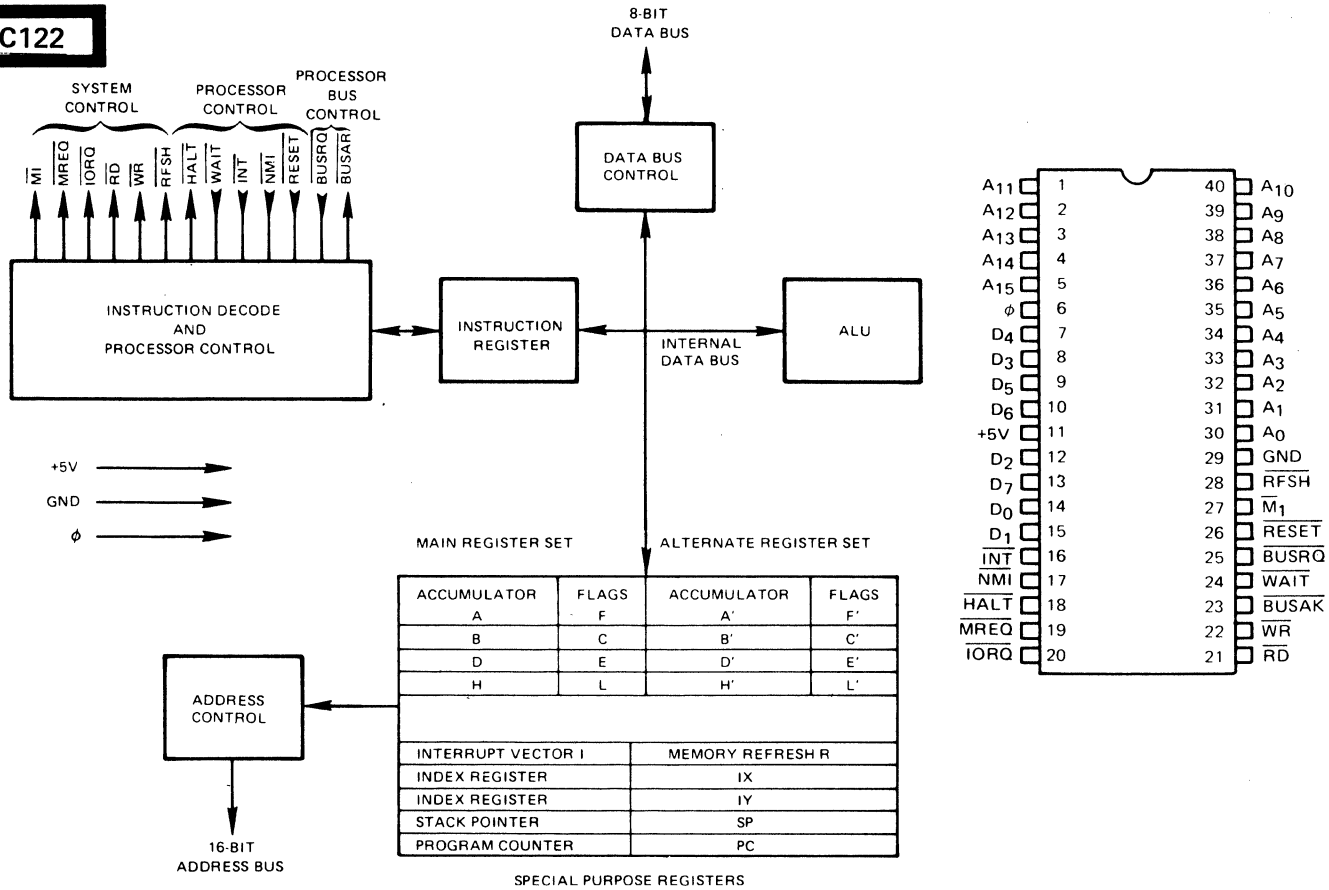
(TOP VIEW)



C121



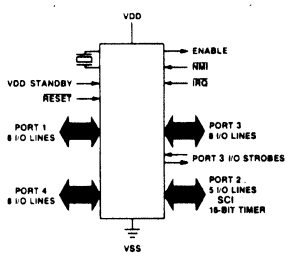
C122



ACCUMULATOR	FLAGS	ACCUMULATOR	FLAGS
A	F	A'	F'
B	C	B'	C'
D	E	D'	E'
H	L	H'	L'

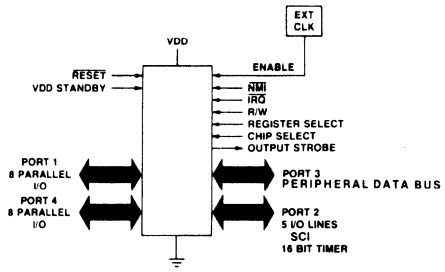
INTERRUPT VECTOR I	MEMORY REFRESH R
INDEX REGISTER	IX
INDEX REGISTER	IY
STACK POINTER	SP
PROGRAM COUNTER	PC

C123



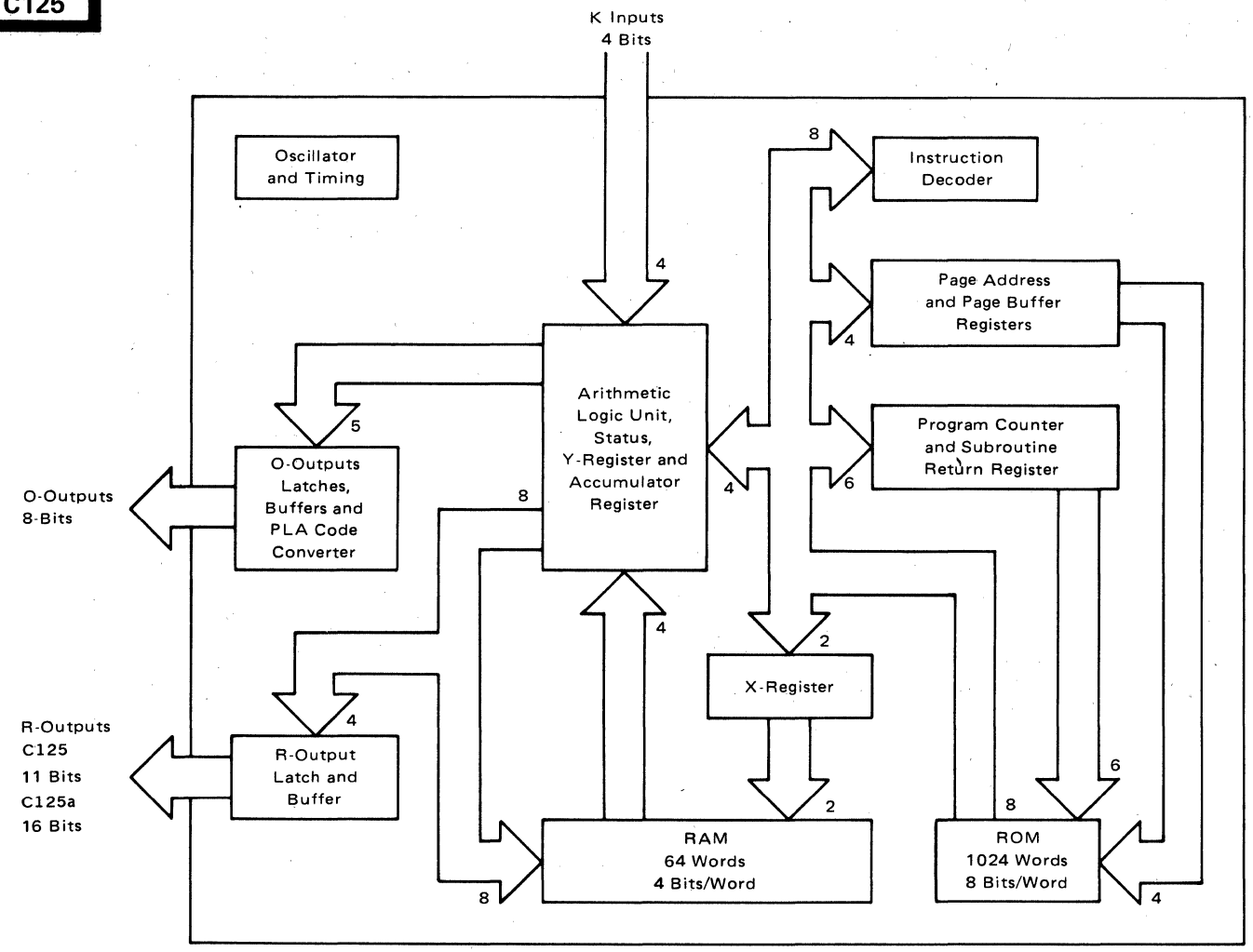
SINGLE CHIP MODE

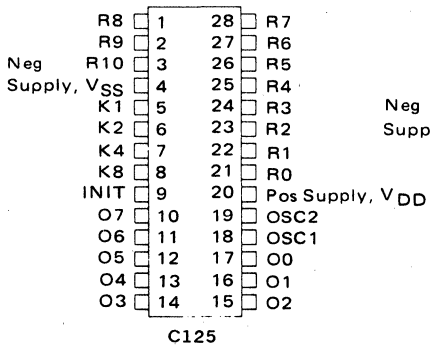
C124



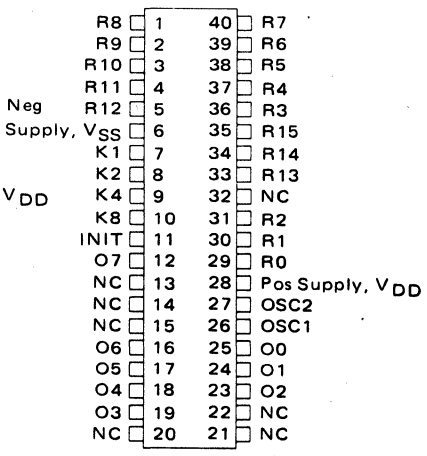
SINGLE CHIP MODE
EXTERNAL CLOCK/
DIVIDE-BY-ONE

C125

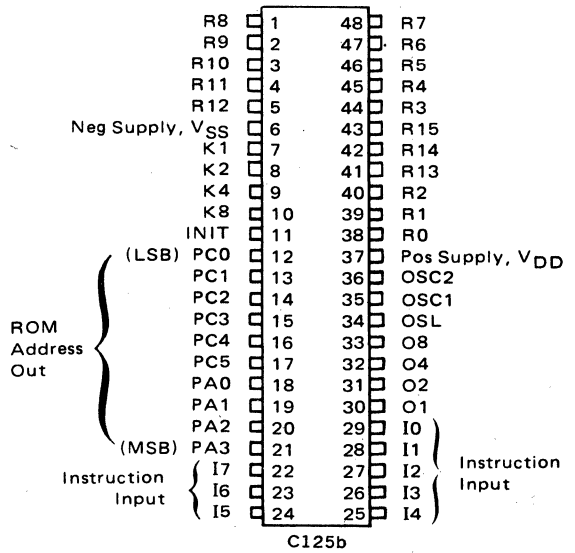




C125



C125a



ROM Address Out

Instruction Input

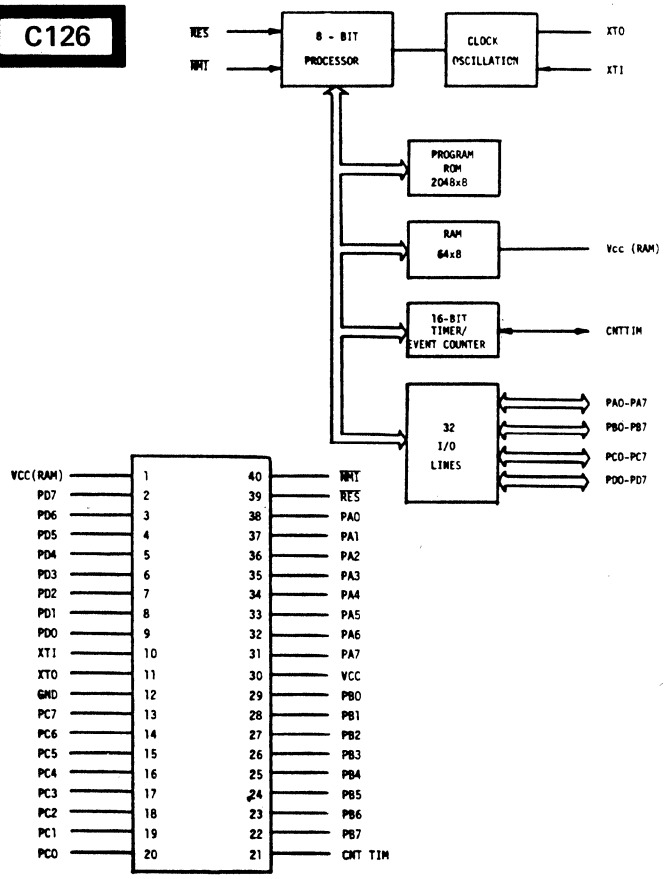
Instruction Input

C125b

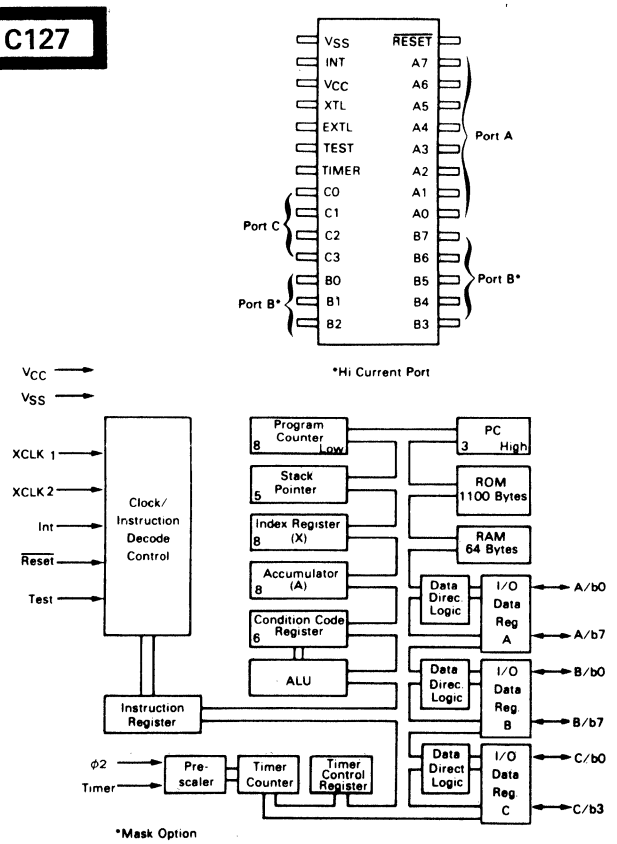
18. CPU INTERNAL ARCHITECTURE DRAWINGS

IN DRAWING NUMBER SEQUENCE

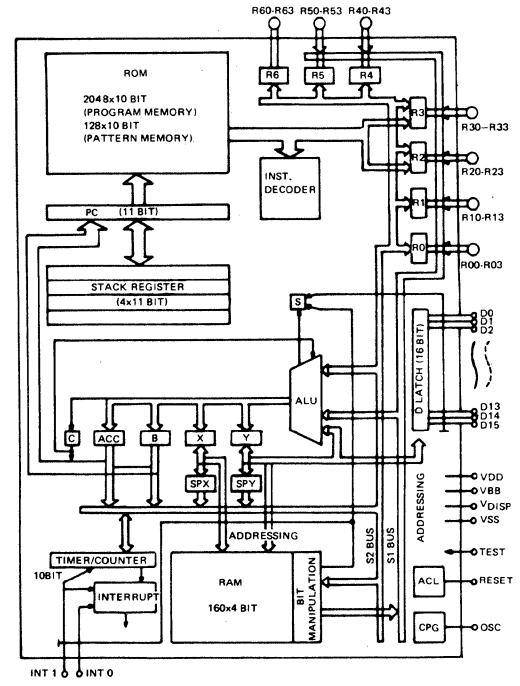
C126



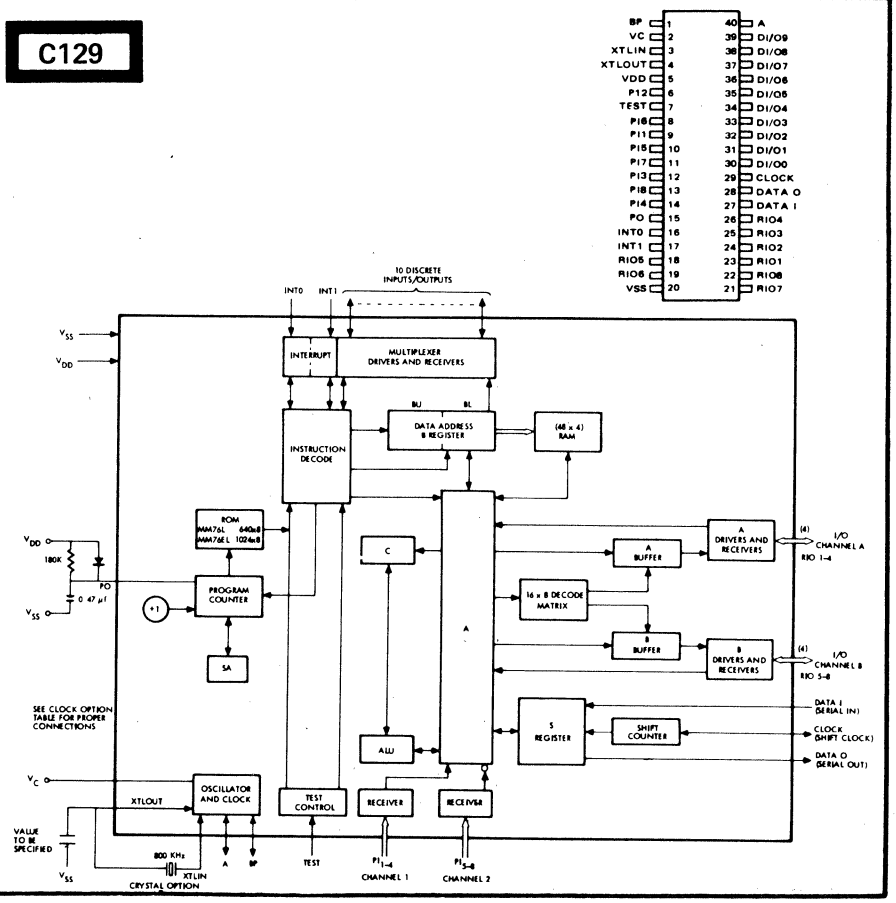
C127



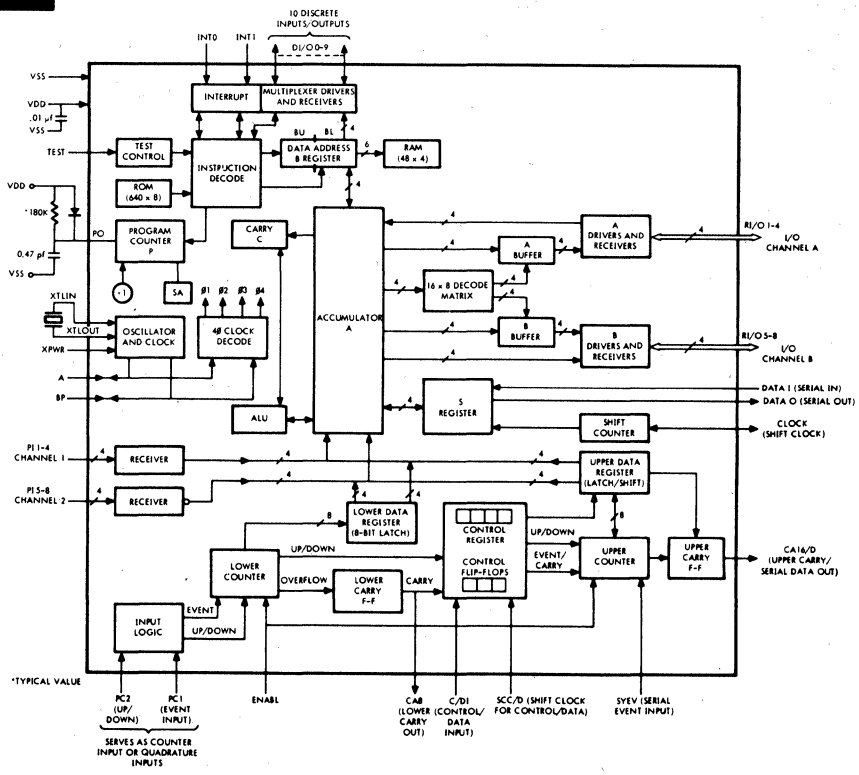
C128

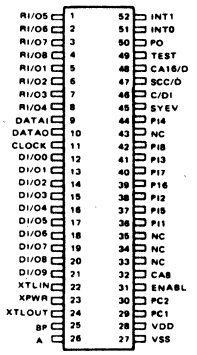


C129

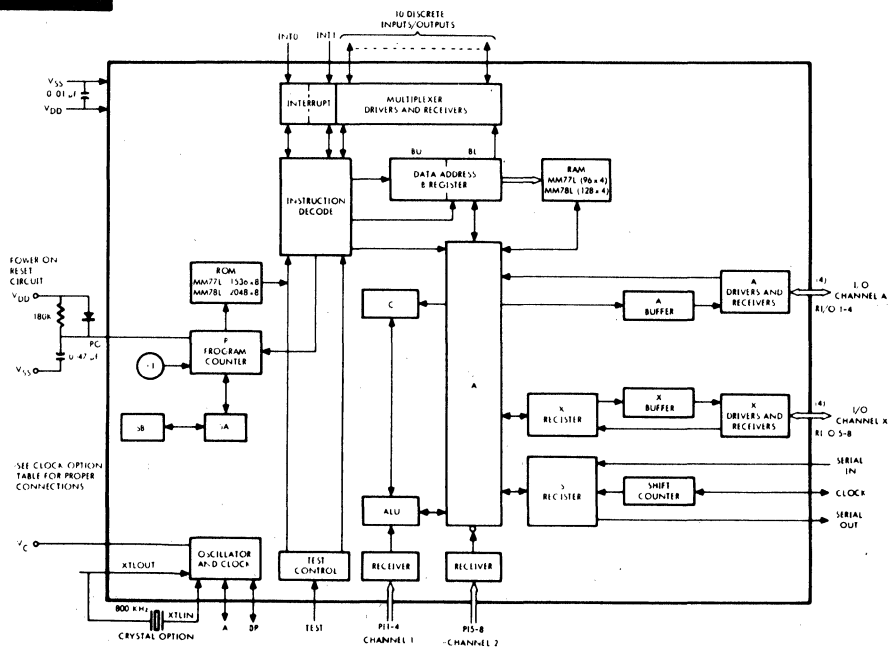


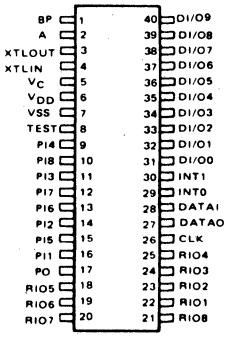
C130


10 DISCRETE INPUTS/OUTPUTS
DI/O0-9
INT0
INT1
INTERRUPT
MULTIPLEXER DRIVERS AND RECEIVERS
VSS
VDD
.01 µf
TEST
TEST CONTROL
INSTRUCTION DECODE
DATA ADDRESS B REGISTER
RAM (48 x 4)
ROM (640 x 8)
180K
PO
PROGRAM COUNTER P
CARRY C
0.47 pf
+1
SA
ø1 ø2 ø3 ø4
XTLIN
XTLOUT
OSCILLATOR AND CLOCK
48 CLOCK DECODE
XPWR
A
BP
ACCUMULATOR A
16 x 8 DECODE MATRIX
A BUFFER
B BUFFER
A DRIVERS AND RECEIVERS
B DRIVERS AND RECEIVERS
RI/O 1-4
I/O CHANNEL A
RI/O 5-8
I/O CHANNEL B
ALU
S REGISTER
DATA I (SERIAL IN)
DATA O (SERIAL OUT)
SHIFT COUNTER
CLOCK (SHIFT CLOCK)
PI 1-4 CHANNEL 1
PI 5-8 CHANNEL 2
RECEIVER
UPPER DATA REGISTER (LATCH/SHIFT)
LOWER DATA REGISTER (8-BIT LATCH)
CONTROL REGISTER
CONTROL FLIP-FLOPS
UP/DOWN
EVENT/ CARRY
LOWER COUNTER
OVERFLOW
LOWER CARRY F-F
UPPER COUNTER
UPPER CARRY F-F
CA16/D (UPPER CARRY/ SERIAL DATA OUT)
INPUT LOGIC
EVENT
*TYPICAL VALUE
PC2 (UP/ DOWN)
PC1 (EVENT INPUT)
SERVES AS COUNTER INPUT OR QUADRATURE INPUTS
ENABL
CAB (LOWER CARRY OUT)
C/DI (CONTROL/ DATA INPUT)
SCC/D (SHIFT CLOCK FOR CONTROL/DATA)
SYEV (SERIAL EVENT INPUT)


RI/O5 1
RI/O6 2
RI/O7 3
RI/O8 4
RI/O1 5
RI/O2 6
RI/O3 7
RI/O4 8
DATAI 9
DATAO 10
CLOCK 11
DI/O0 12
DI/O1 13
DI/O2 14
DI/O3 15
DI/O4 16
DI/O5 17
DI/O6 18
DI/O7 19
DI/O8 20
DI/O9 21
XTLIN 22
XPWR 23
XTLOUT 24
BP 25
A 26
52 INT1
51 INT0
50 PO
49 TEST
48 CA16/D
47 SCC/D
46 C/DI
45 SYEV
44 PI4
43 NC
42 PI8
41 PI3
40 PI7
39 PI6
38 PI2
37 PI5
36 PI1
35 NC
34 NC
33 NC
32 CAB
31 ENABL
30 PC2
29 PC1
28 VDD
27 VSS

C131

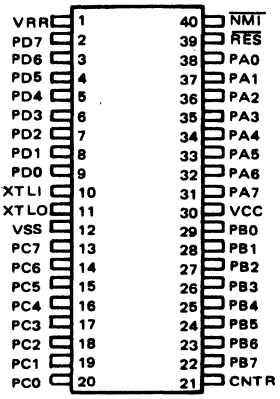

10 DISCRETE INPUTS/OUTPUTS
INT0
INT1
VSS
0.01 µf
VDD
INTERRUPT
MULTIPLEXER DRIVERS AND RECEIVERS
BU
BL
DATA ADDRESS B REGISTER
RAM MM77L (96 x 4) MM78L (128 x 4)
INSTRUCTION DECODE
POWER ON RESET CIRCUIT
ROM MM77L 1536 x 8 MM78L 2048 x 8
180K
PC
P PROGRAM COUNTER
0.47 µf
+1
:B
:A
C
A
A BUFFER
A DRIVERS AND RECEIVERS
I/O CHANNEL A
RI/O 1-4
X REGISTER
X BUFFER
X DRIVERS AND RECEIVERS
I/O CHANNEL X
RI/O 5-8
S REGISTER
SERIAL IN
SHIFT COUNTER
CLOCK
SERIAL OUT
SEE CLOCK OPTION TABLE FOR PROPER CONNECTIONS
ALU
VC
OSCILLATOR AND CLOCK
XTLOUT
TEST CONTROL
RECEIVER
RECEIVER
800 KHz
XTLIN
CRYSTAL OPTION
A
DP
TEST
PI1-4 CHANNEL 1
PI5-8 CHANNEL 2


BP 1
A 2
XTLOUT 3
XTLIN 4
VC 5
VDD 6
VSS 7
TEST 8
PI4 9
PI8 10
PI3 11
PI7 12
PI6 13
PI2 14
PI5 15
PI1 16
PO 17
RIO5 18
RIO6 19
RIO7 20
40 DI/O9
39 DI/O8
38 DI/O7
37 DI/O6
36 DI/O5
35 DI/O4
34 DI/O3
33 DI/O2
32 DI/O1
31 DI/O0
30 INT1
29 INT0
28 DATAI
27 DATAO
26 CLK
25 RIO4
24 RIO3
23 RIO2
22 RIO1
21 RIO8

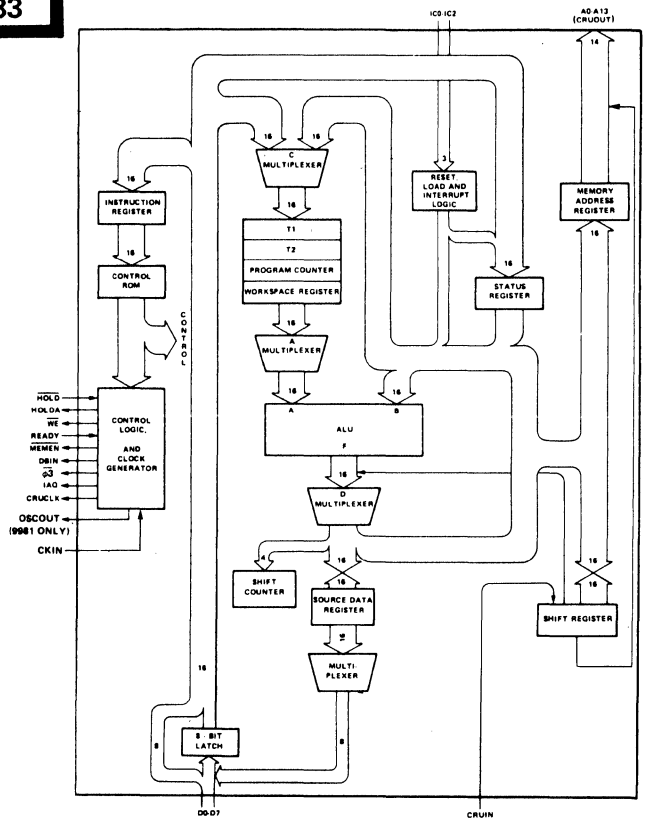
18. CPU INTERNAL ARCHITECTURE DRAWINGS

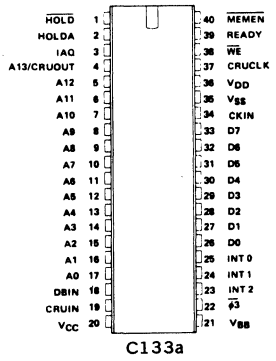
IN DRAWING NUMBER SEQUENCE

C132

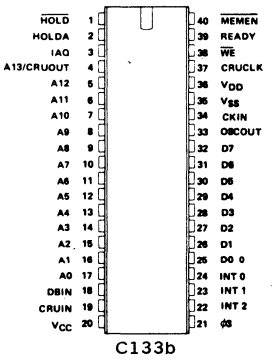


C133



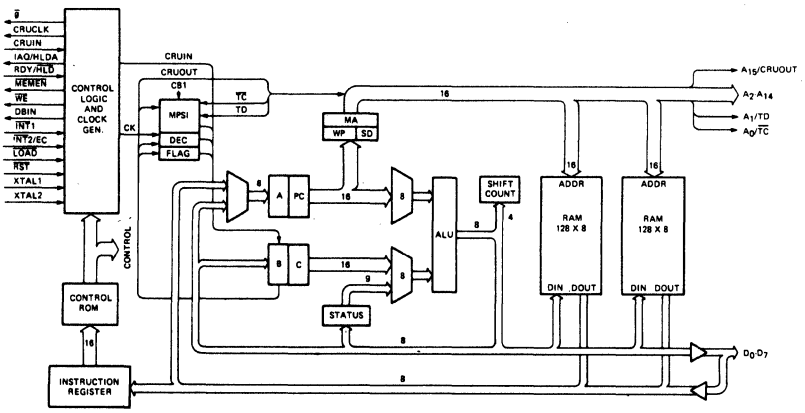


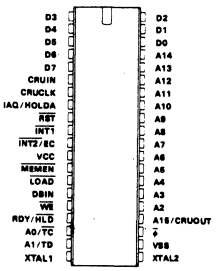
C133a



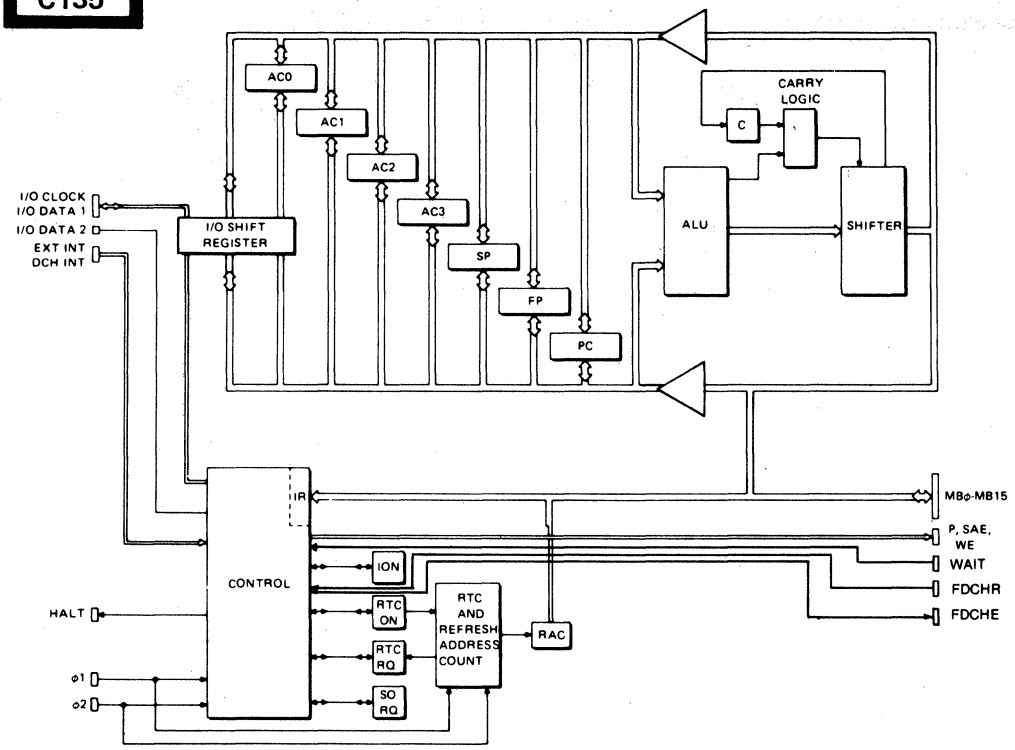
C133b

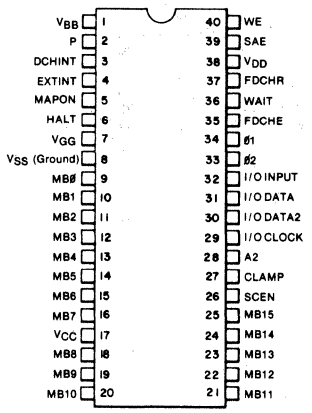
C134



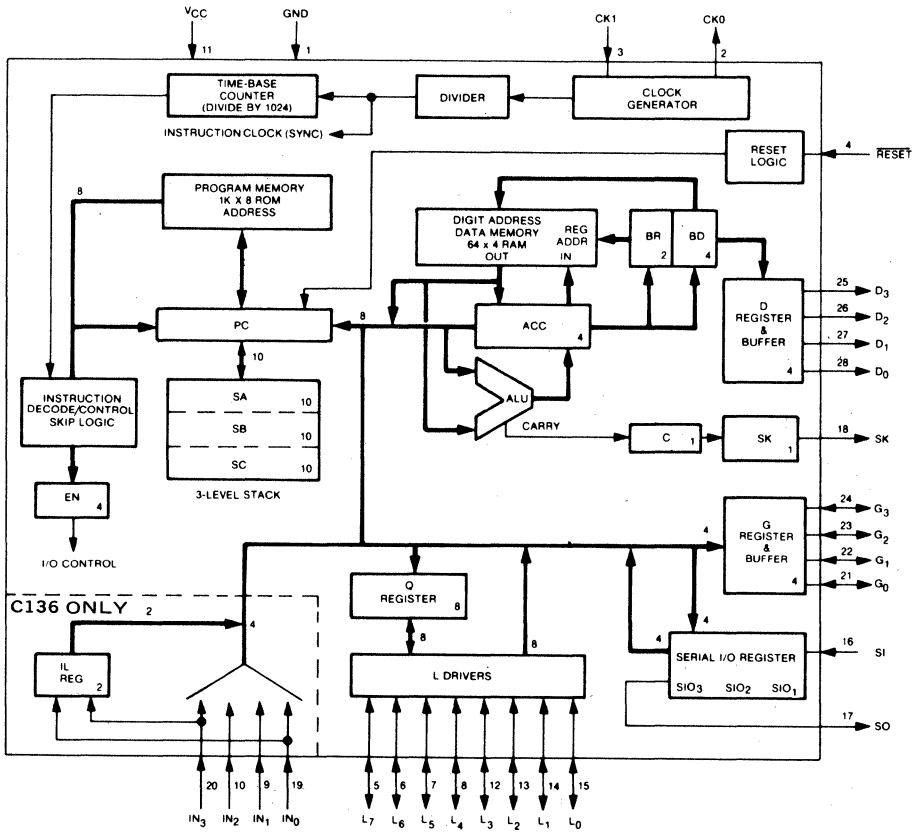


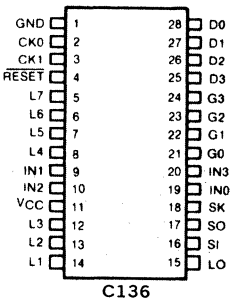
C135



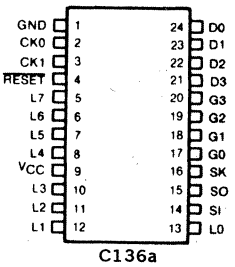


C136



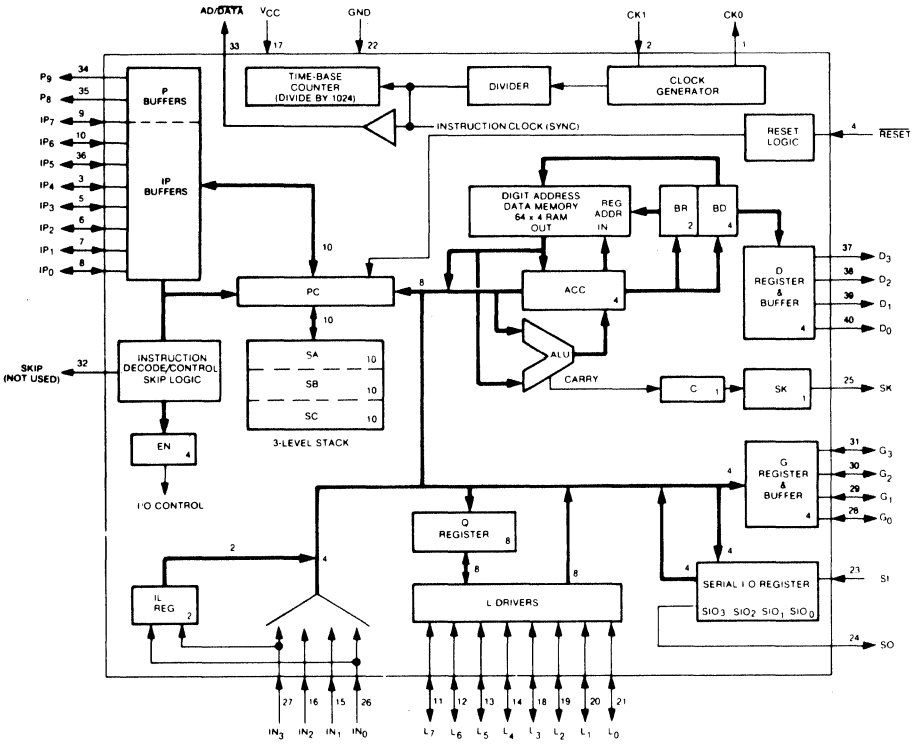


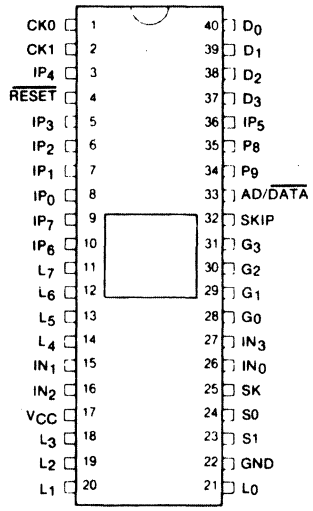
C136



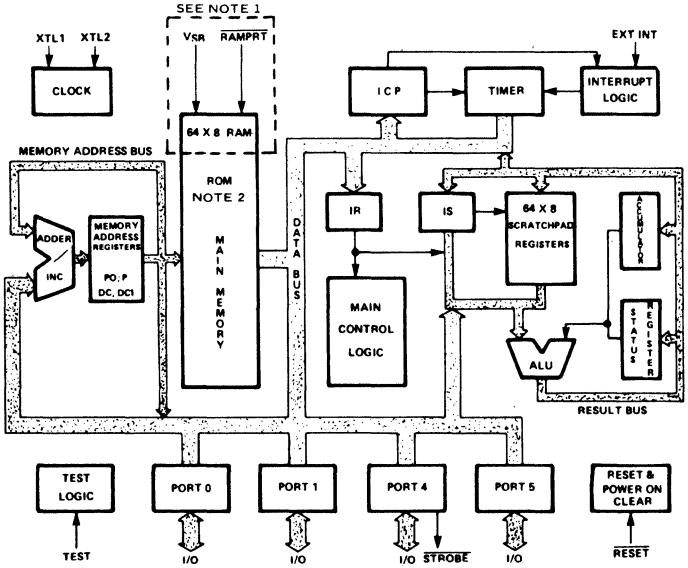
C136a

C137



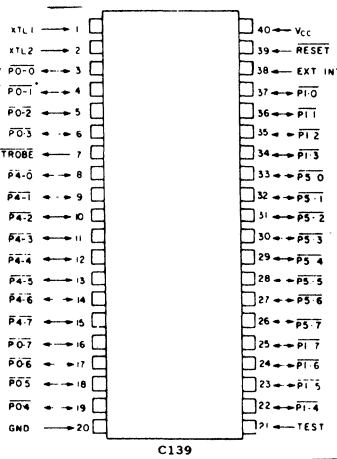


C139

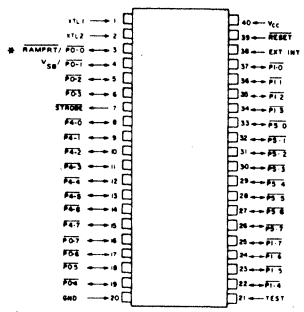


NOTE 1. RAM CIRCUITRY ENCLOSED WITHIN DOTTED LINES APPLIES ONLY FOR C139a AND C139b.

NOTE 2. C139 AND C139b: 2048 x 8 ROM
C139a: 4032 x 8 ROM

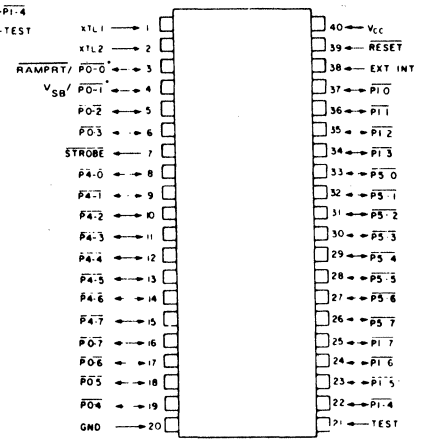


C139



*PROGRAMMABLE (PORT PINS BECOME V_{SB} AND $\overline{RAMPRT}$ WITH STANDBY POWER OPTION)

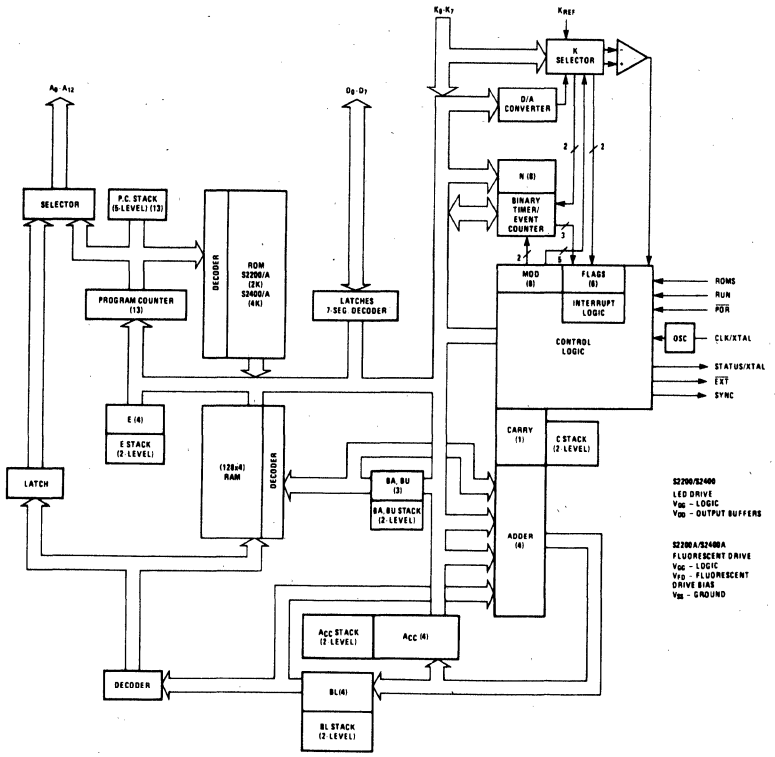
C139a



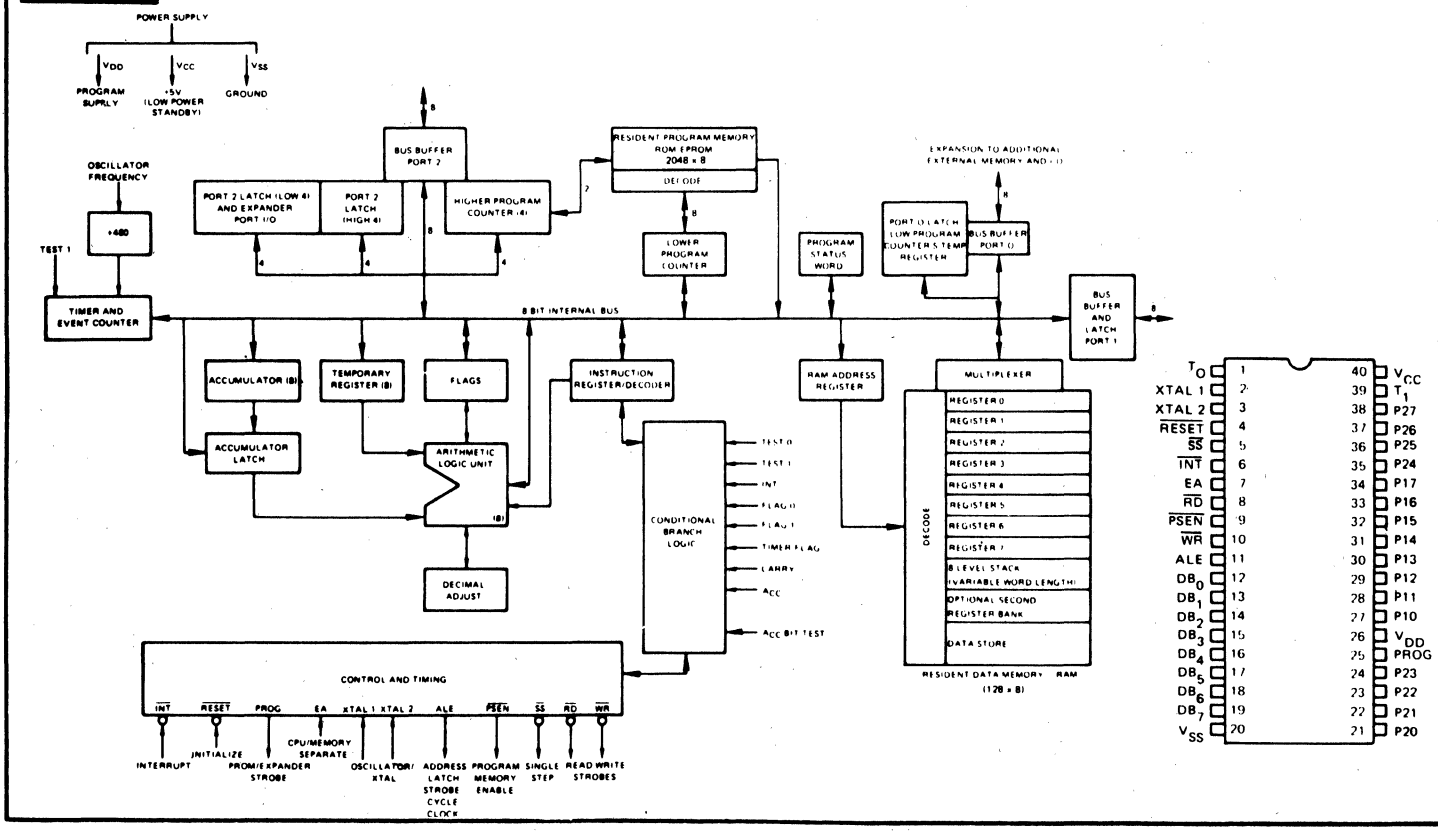
*PROGRAMMABLE (PORT PINS BECOME V_{SB} AND $\overline{RAMPRT}$ WITH STANDBY POWER OPTION)

C139b

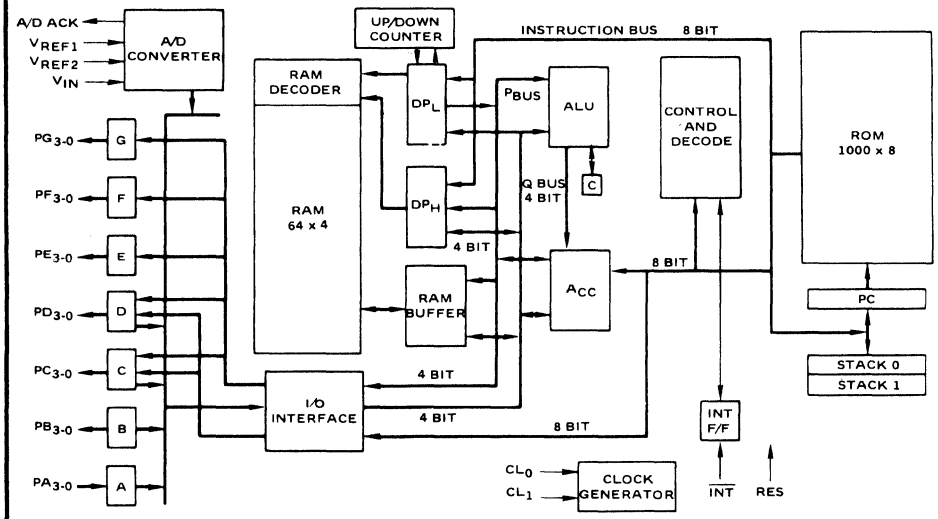
C140

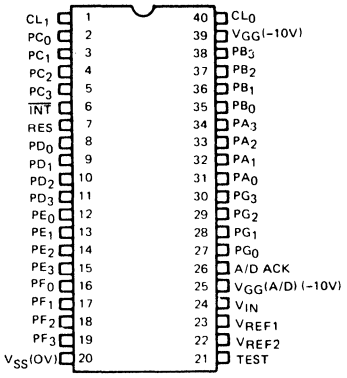

K SELECTOR
D/A CONVERTER
N (8)
BINARY TIMER/ EVENT COUNTER
MOD (8)
FLAGS (6)
INTERRUPT LOGIC
CONTROL LOGIC
OSC
ROMS
RUN
POR
CLK/XTAL
STATUS/XTAL
EXT
SYNC
SELECTOR
P.C. STACK (6-LEVEL) (13)
PROGRAM COUNTER (13)
DECODER
ROM S2200/A (2K) S2400/A (4K)
LATCHES 7-SEG DECODER
E (4)
E STACK (2-LEVEL)
LATCH
(128x4) RAM
DECODER
BA, BU (3)
BA, BU STACK (2-LEVEL)
CARRY (1)
C STACK (2-LEVEL)
ADDER (4)
ACC STACK (2-LEVEL)
ACC (4)
DECODER
BL (4)
BL STACK (2-LEVEL)
S2200/S2400 LED DRIVE
S2200A/S2400A FLUORESCENT DRIVE

C141


POWER SUPPLY
VDD
VCC
VSS
PROGRAM SUPPLY
+5V (LOW POWER STANDBY)
GROUND
BUS BUFFER PORT 2
RESIDENT PROGRAM MEMORY ROM EPROM 2048 x 8
DECODE
EXPANSION TO ADDITIONAL EXTERNAL MEMORY AND I/O
OSCILLATOR FREQUENCY
÷480
TEST 1
PORT 2 LATCH (LOW 4) AND EXPANDER PORT I/O
PORT 2 LATCH (HIGH 4)
HIGHER PROGRAM COUNTER (4)
LOWER PROGRAM COUNTER
PROGRAM STATUS WORD
PORT 0 LATCH LOW PROGRAM COUNTER/STACK REGISTER
BUS BUFFER PORT 0
TIMER AND EVENT COUNTER
8 BIT INTERNAL BUS
BUS BUFFER AND LATCH PORT 1
ACCUMULATOR (8)
TEMPORARY REGISTER (8)
FLAGS
INSTRUCTION REGISTER/DECODER
RAM ADDRESS REGISTER
MULTIPLEXER
ACCUMULATOR LATCH
ARITHMETIC LOGIC UNIT
DECIMAL ADJUST
CONDITIONAL BRANCH LOGIC
TEST 0
TEST 1
INT
FLAG 0
FLAG 1
TIMER FLAG
CARRY
ACC
ACC BIT TEST
DECODE
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8 LEVEL STACK (VARIABLE WORD LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
RESIDENT DATA MEMORY RAM (128 x 8)
CONTROL AND TIMING
INT
RESET
PROG
EA
XTAL 1
XTAL 2
ALE
PSEN
SS
RD
WR
INTERRUPT
INITIALIZE
PROM/EXPANDER STROBE
CPU/MEMORY SEPARATE
OSCILLATOR/ XTAL
ADDRESS LATCH STROBE CYCLE CLOCK
PROGRAM MEMORY ENABLE
SINGLE STEP
READ WRITE STROBES
T0 1
XTAL 1 2
XTAL 2 3
RESET 4
SS 5
INT 6
EA 7
RD 8
PSEN 9
WR 10
ALE 11
DB0 12
DB1 13
DB2 14
DB3 15
DB4 16
DB5 17
DB6 18
DB7 19
VSS 20
40 VCC
39 T1
38 P27
37 P26
36 P25
35 P24
34 P17
33 P16
32 P15
31 P14
30 P13
29 P12
28 P11
27 P10
26 VDD PROG
25 PROG
24 P23
23 P22
22 P21
21 P20

C142

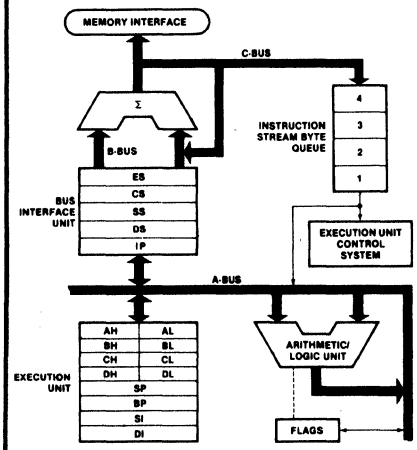


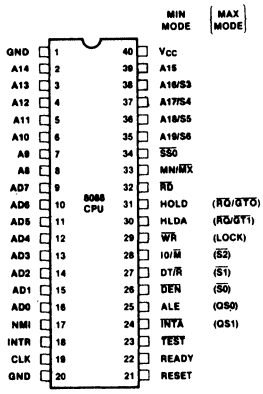


PIN NAMES

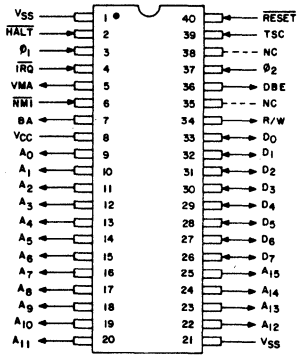
CL_0-CL_1	External Clock Source
PC_0-PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
TEST	Input for Testing (Normally GND)
$V_{REF1,2}$	Reference Voltages
V_{IN}	Analog Input Voltage
$V_{GG(A/D)}$	A/D Supply Voltage
A/D ACK	A/D Acknowledge Output
PG_0-PG_3	Output Port G
PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B

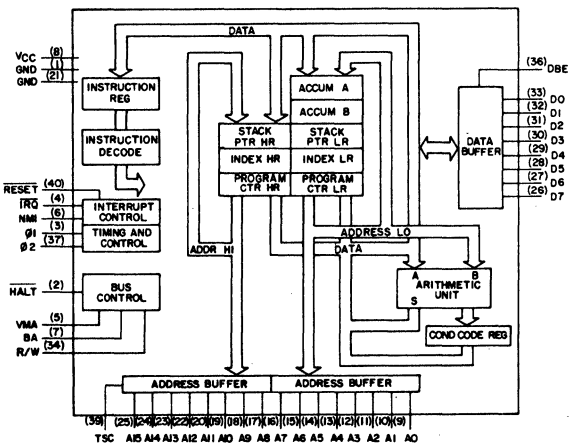
C143





C144

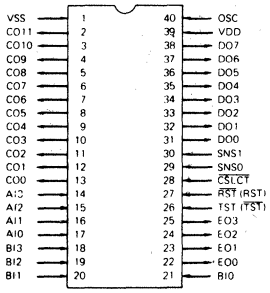




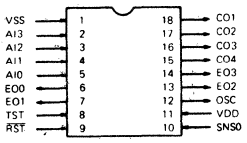
18. CPU INTERNAL ARCHITECTURE DRAWINGS

IN DRAWING NUMBER SEQUENCE

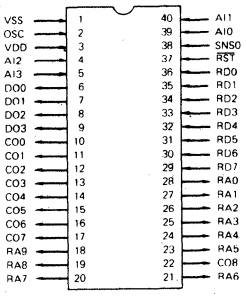
C145



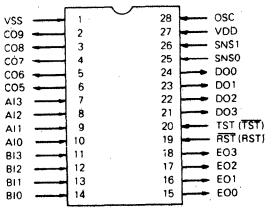
C145



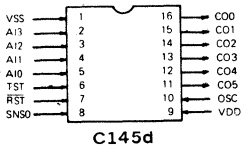
C145a



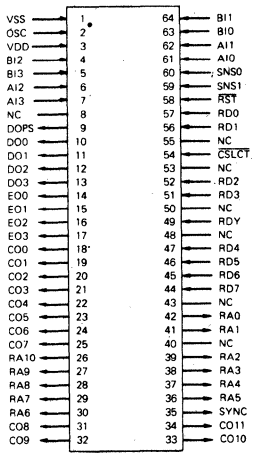
C145b



C145c



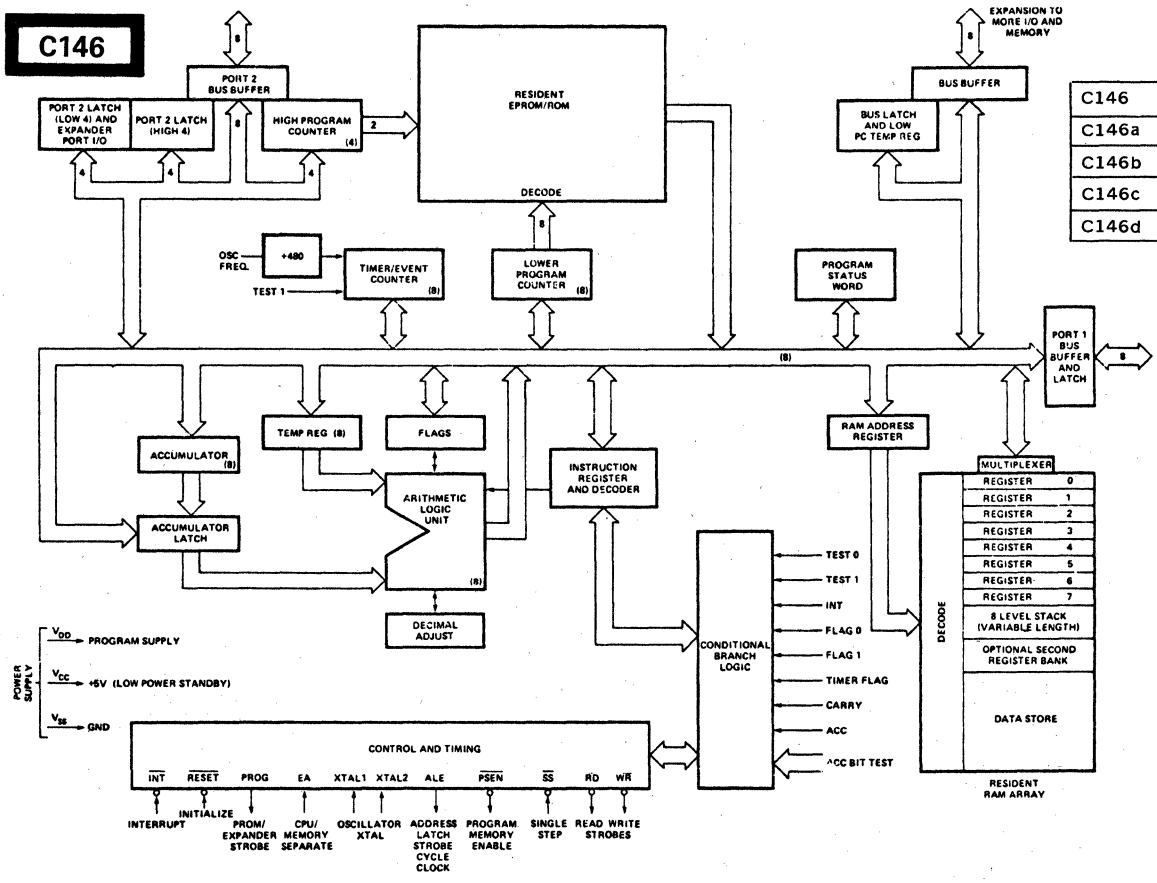
C145d



C145e

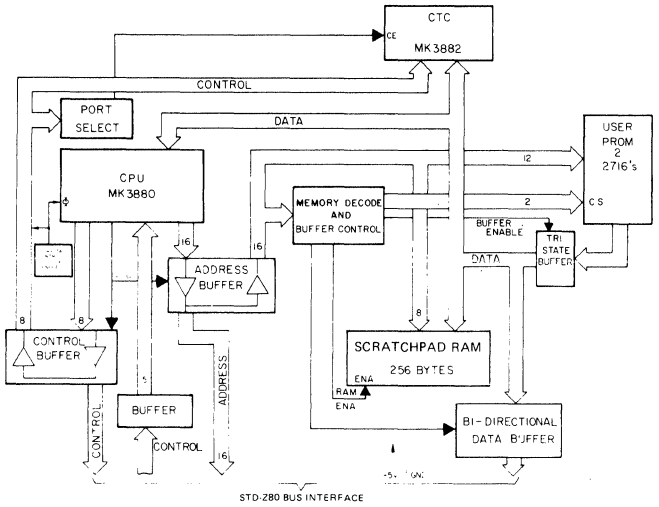
VDD	: Power Supply (+5V)	AI0 ~ AI3	: A Input Port
Vss	: Circuit GND Potential (0V)	BI0 ~ BI3	: B Input Port
RST	: Reset Input	CO0 ~ CO11	: C Output Port
CSLCT	: Counter Selection	DO0 ~ DO7	: D Output Port
SNS0, SNS1	: Sense Input	EO0 ~ EO3	: E Output Port
OSC	: Frequency Control	TST (TST)	: LSI Test Input

C146

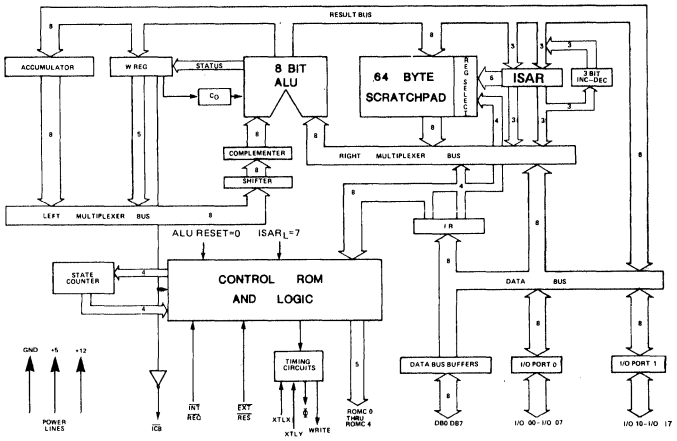


	RAM/ROM	
C146	64x8	1kx8 EPROM
C146a	64x8	EXTERNAL
C146b	128x8	2kx8
C146c	128x8	EXTERNAL
C146d	64x8	1kx8

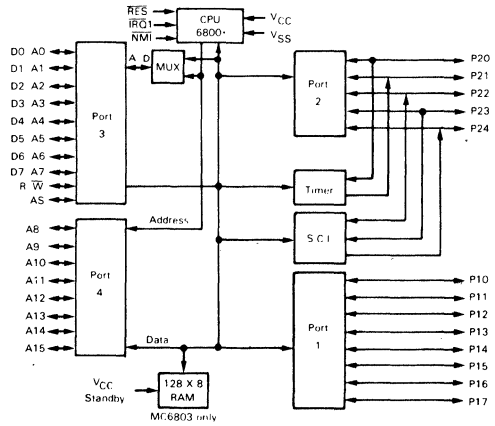
C147



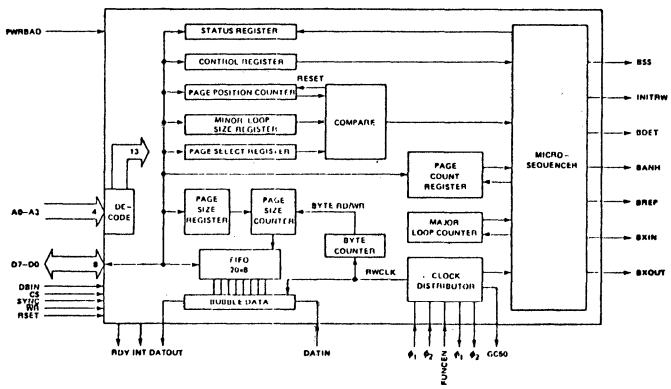
C148



C149



C150



C151

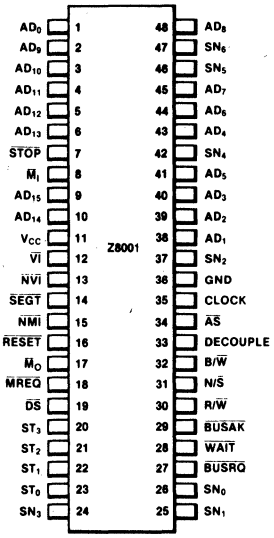


Figure 8. Z8001 Pin Assignments

C152

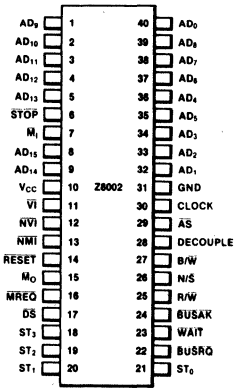
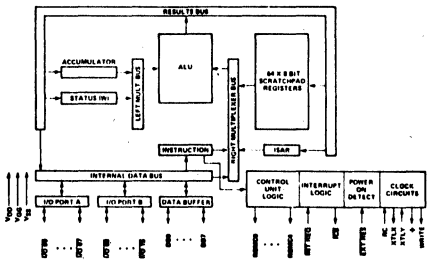


Figure 9. Z8002 Pin Assignments

C153



C154

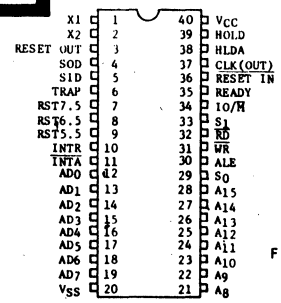
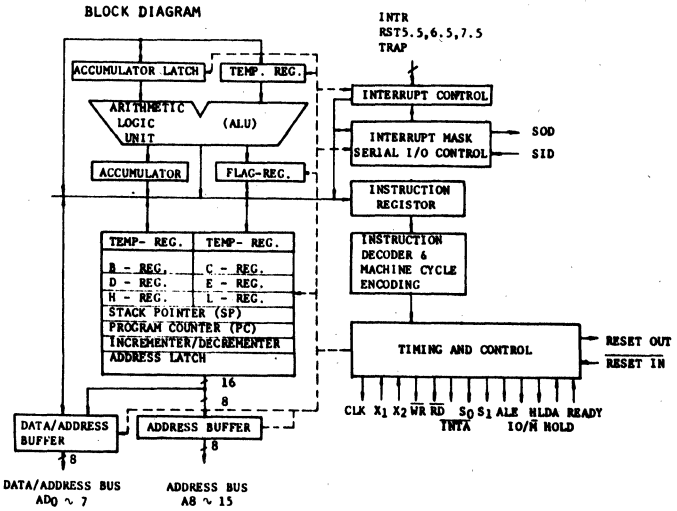


FIGURE 1. TMP8035AP PINOUT DIAGRAM

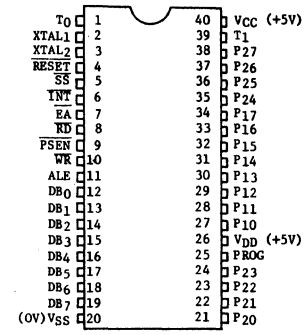
BLOCK DIAGRAM



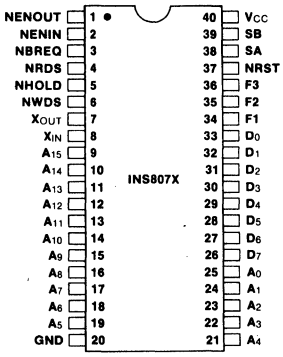
18. CPU INTERNAL ARCHITECTURE DRAWINGS

IN DRAWING NUMBER SEQUENCE

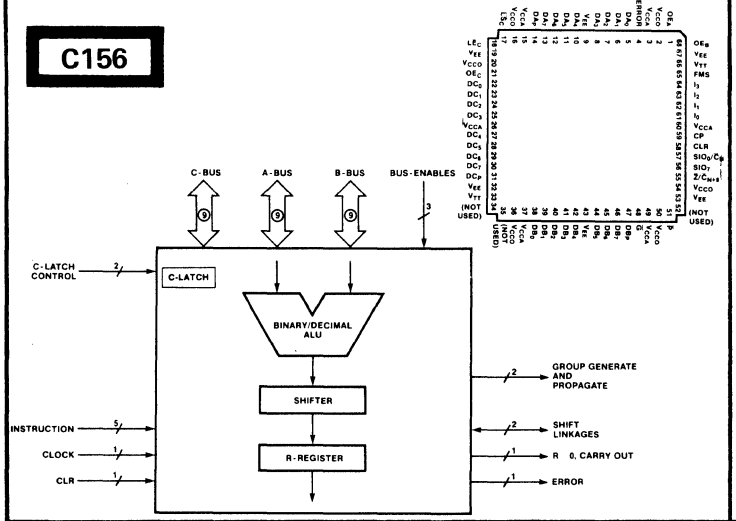
C155

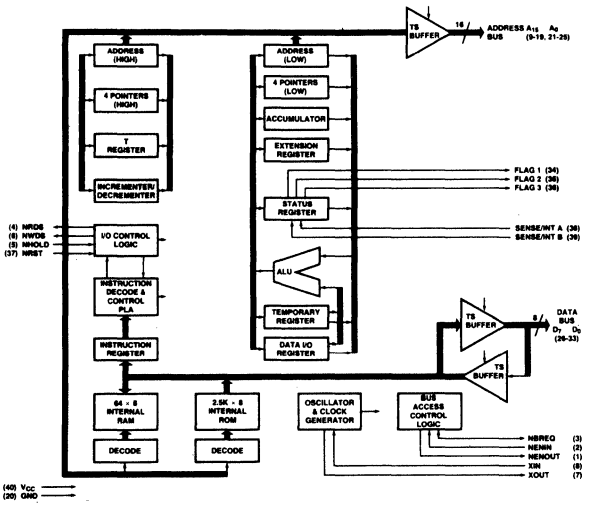


C157

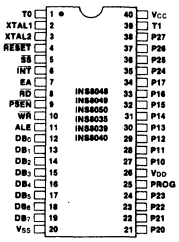


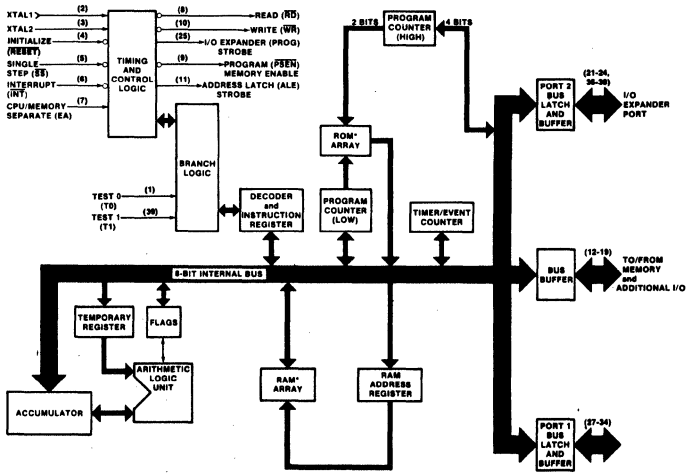
C156





C158



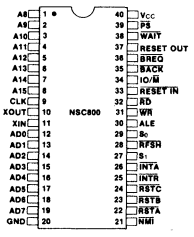


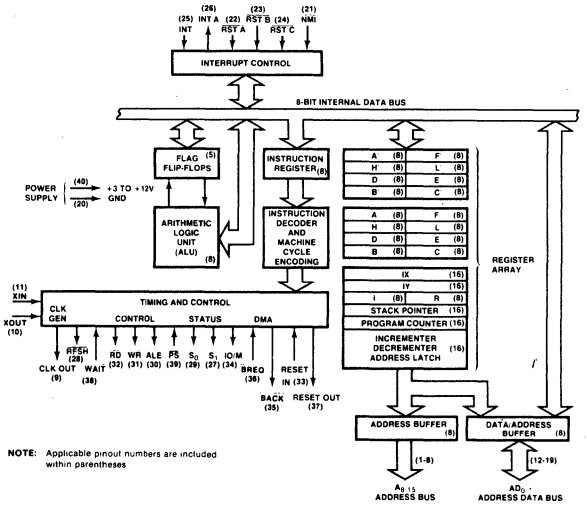
*ROM AND RAM CAPACITIES
INS8048 - 1K x 8 ROM - 64 x 8 RAM
INS8049 - 2K x 8 ROM - 128 x 8 RAM
INS8050 - 4K x 8 ROM - 256 x 8 RAM

POWER SUPPLY
V_{CC} -(40) +5 POWER SUPPLY
V_{DD} -(26) STANDBY SUPPLY
V_{SS} -(20) GND

NOTE: Applicable pinout numbers are included within parentheses

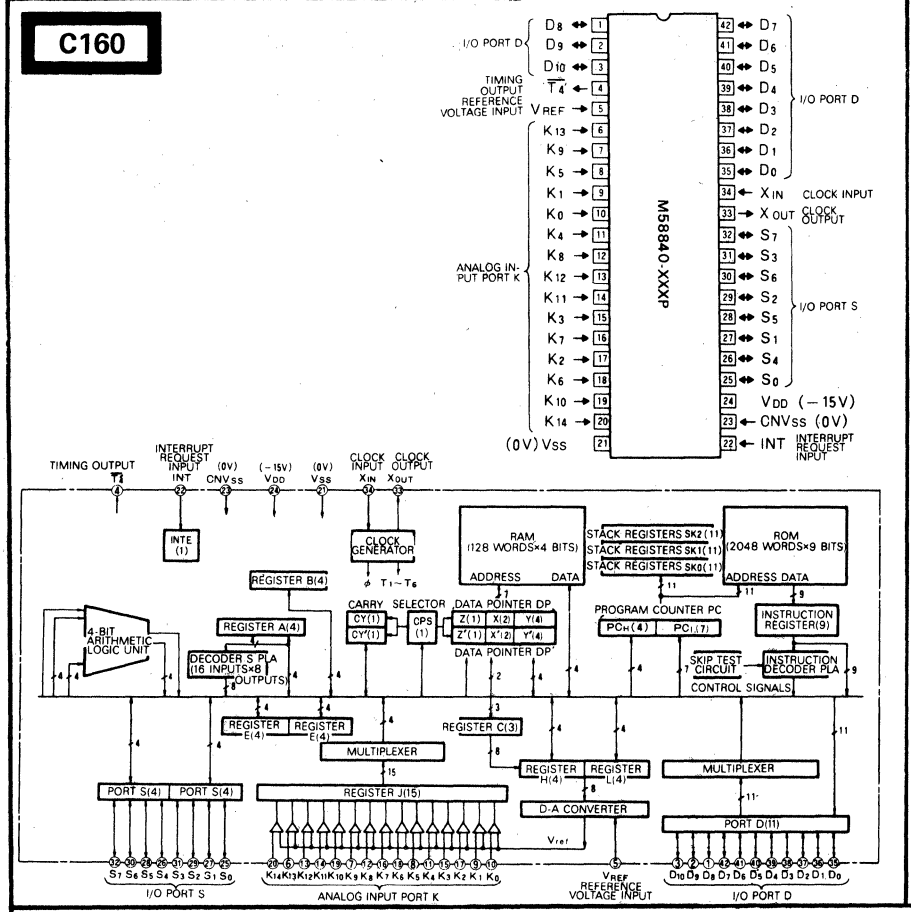
C159



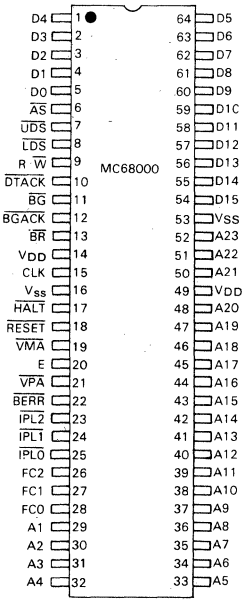


NOTE: Applicable pinout numbers are included within parentheses

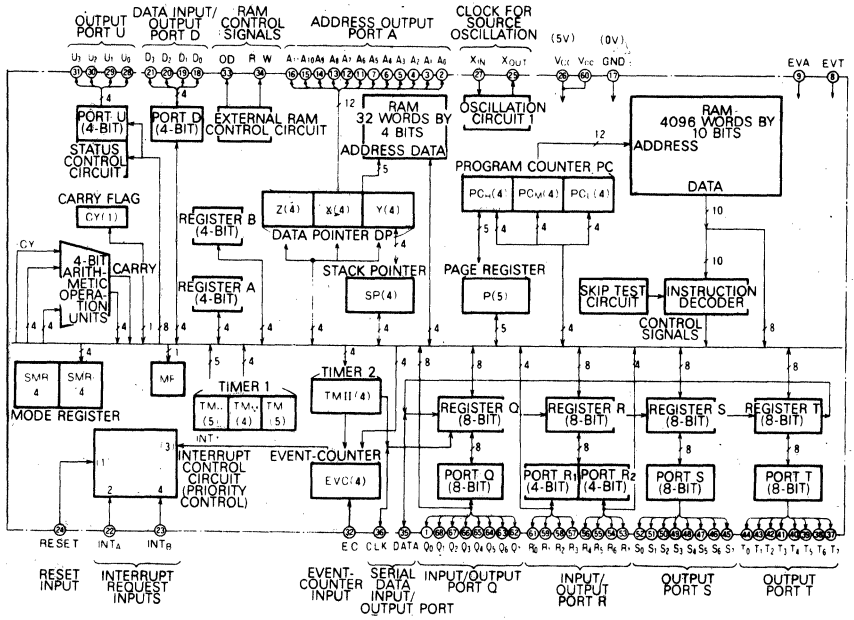
C160



C162



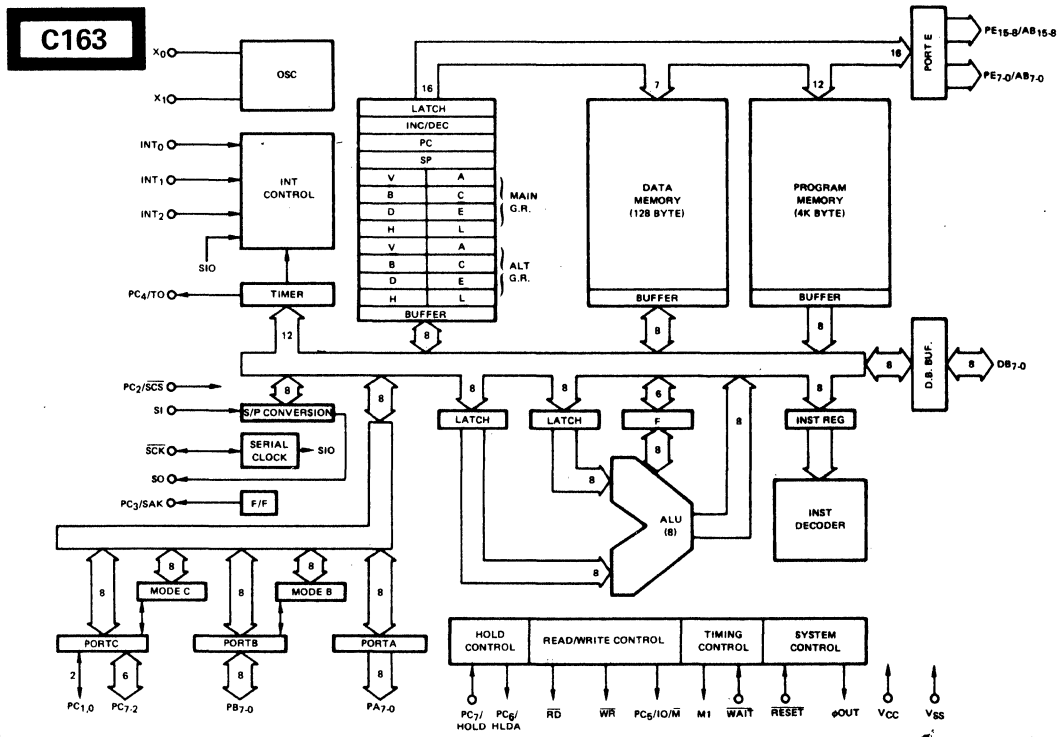
C161

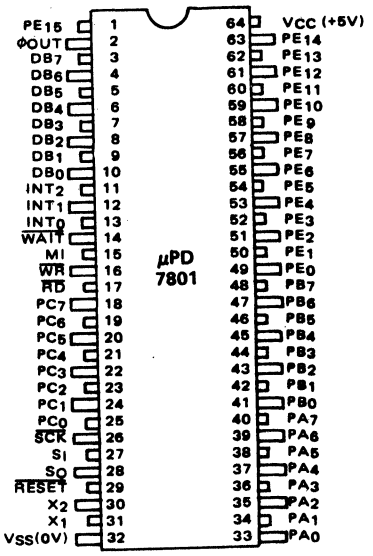


18. CPU INTERNAL ARCHITECTURE DRAWINGS

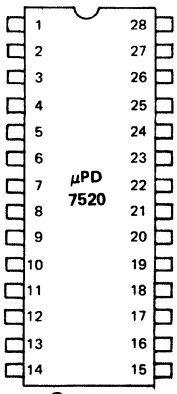
IN DRAWING NUMBER SEQUENCE

C163





C164

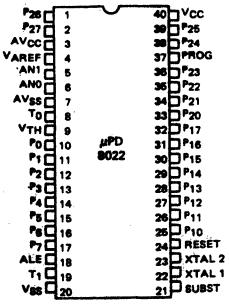


PIN NAMES

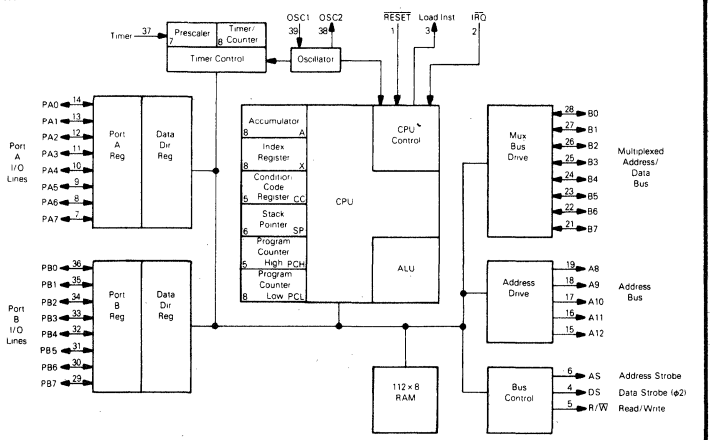
T_{0-5}	6-Bit Digit Output for LED
S_{0-7}	8-Bit Segment Output for LED
PORT 1_{0-3}	4-Bit Input Port
PORT 3_{0-1}	2-Bit Output Port
PORT 4_{0-3}	4-Bit Input/Output Port (Be Able to Use 2-Bit Extended Digit Port)
CLK	Input for Internal Clock Generator
V_{GG}	Single Voltage Input
V_{SS}	Ground
RESET	Reset Input

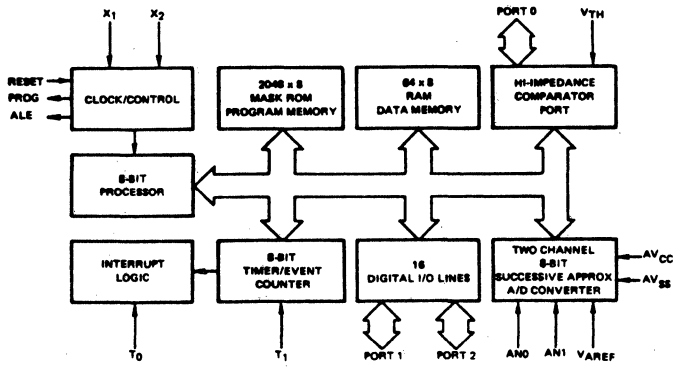
Note: ① Pin names have not yet been assigned.

C165



C171





19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

NOTES: These drawings are referenced in the Read-Write Memories (RAMS), Read-Only Memories (ROMS) and Interface and Support sections of this D.A.T.A.BOOK in accordance with information supplied by the manufacturers.

Since representations may vary, the sources of information should be consulted before critical connections are made to the devices, or to obtain additional detail.

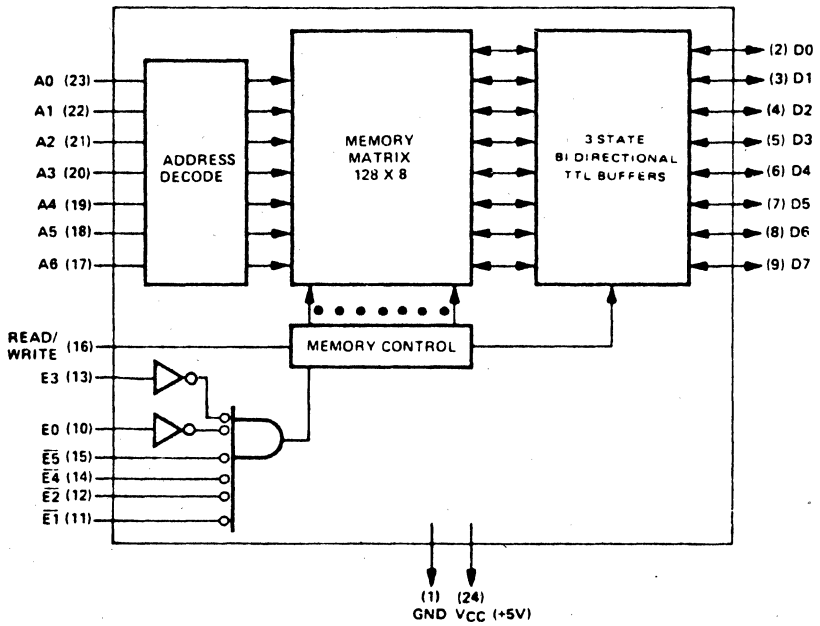
LOGIC DRAWINGS NO. SIGNIFICANCE

The first three characters (a letter and two numerals) of the logic drawings number have the following significance. The letter code (interpreted in the adjacent block) indicates the circuit family (according to technical section title in this D.A.T.A.BOOK); the next two numerals indicate the "use" or "type of" category, within that technical section. The last digit or digits indicate a serial number assigned by D.A.T.A.

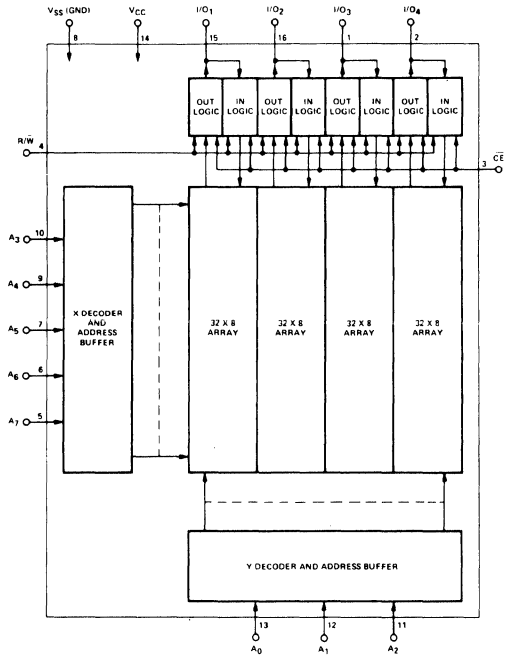
LOGIC DRAWING No. PREFIX
(Letter Code)

Letter Code	Applies to Tech. Sect No.
A	11
B	12
Z	13

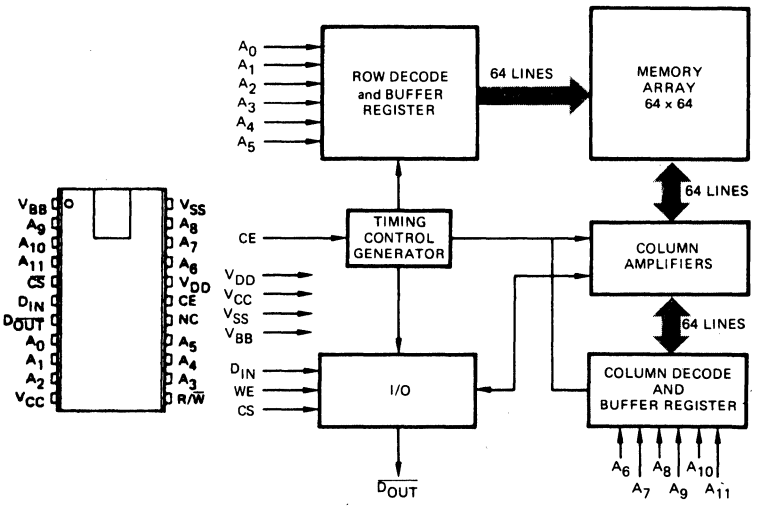
A1



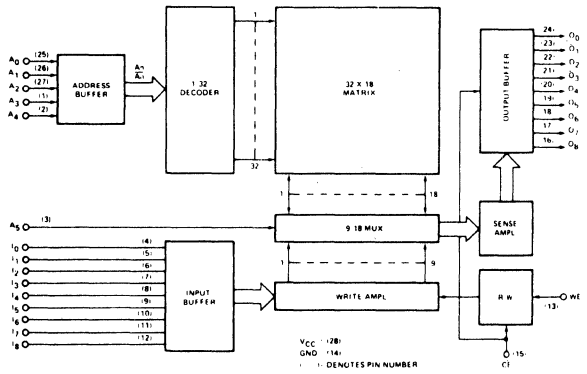
A2


OUT LOGIC
IN LOGIC
X DECODER AND ADDRESS BUFFER
32 X 8 ARRAY
Y DECODER AND ADDRESS BUFFER

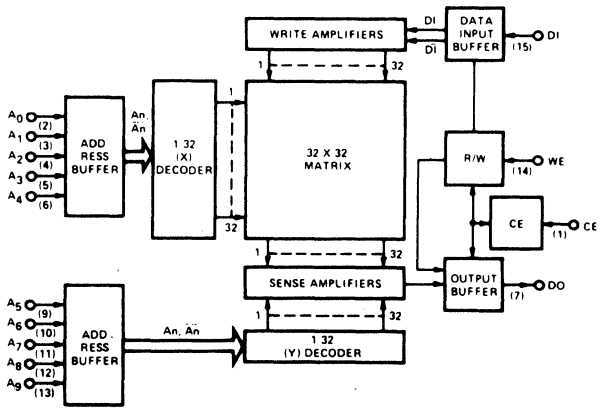
A3


ROW DECODE and BUFFER REGISTER
64 LINES
MEMORY ARRAY 64 x 64
TIMING CONTROL GENERATOR
COLUMN AMPLIFIERS
COLUMN DECODE AND BUFFER REGISTER
I/O

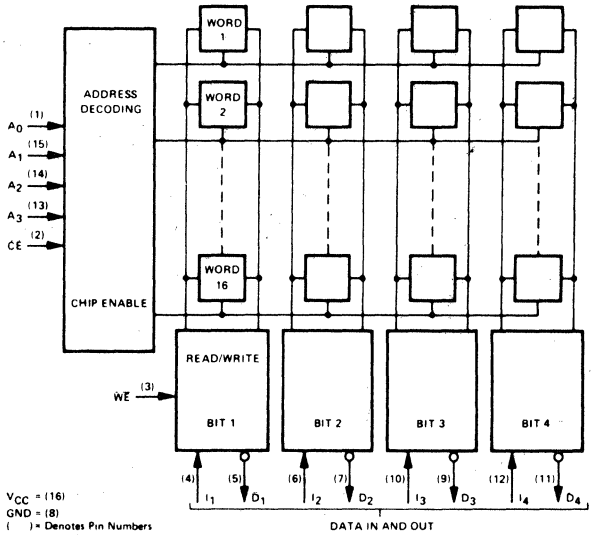
A4


ADDRESS BUFFER
1 32 DECODER
32 X 18 MATRIX
OUTPUT BUFFER
9 18 MUX
SENSE AMPL
INPUT BUFFER
WRITE AMPL

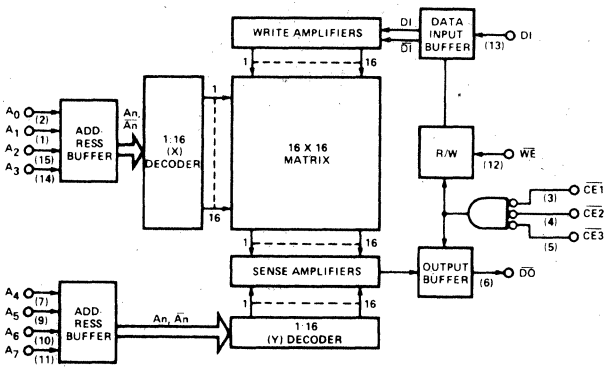
A5


WRITE AMPLIFIERS
DATA INPUT BUFFER
ADD RESS BUFFER
1 32 (X) DECODER
32 X 32 MATRIX
R/W
CE
SENSE AMPLIFIERS
OUTPUT BUFFER
1 32 (Y) DECODER

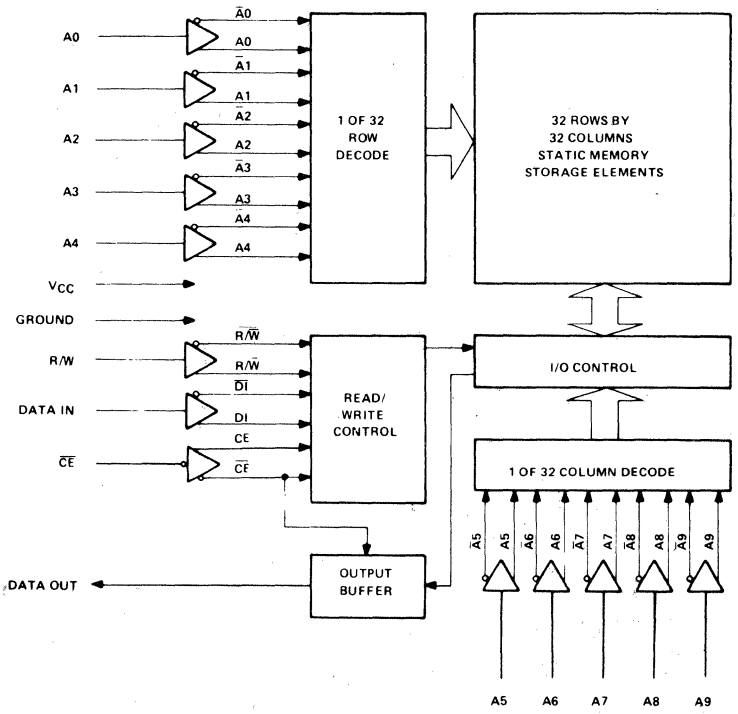
A6

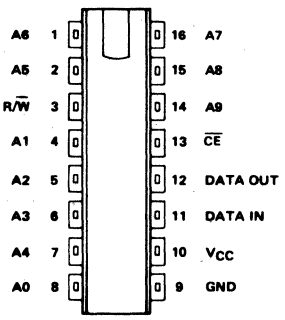

WORD 1
WORD 2
WORD 16
ADDRESS DECODING
CHIP ENABLE
READ/WRITE
BIT 1
BIT 2
BIT 3
BIT 4
A0 (1)
A1 (15)
A2 (14)
A3 (13)
CE (2)
WE (3)
(4) (5) I1 O1
(6) (7) I2 O2
(10) (9) I3 O3
(12) (11) I4 O4
DATA IN AND OUT
VCC = (16)
GND = (8)
( ) = Denotes Pin Numbers

A7

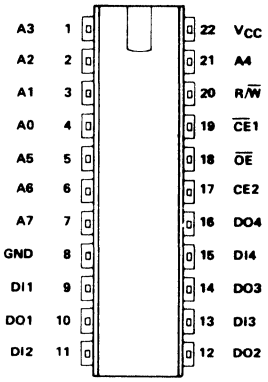

WRITE AMPLIFIERS
DI
DI
DATA INPUT BUFFER
(13)
ADD. RESS BUFFER
1:16 (X) DECODER
16 X 16 MATRIX
R/W
WE
(12)
CE1
CE2
CE3
(3)
(4)
(5)
SENSE AMPLIFIERS
OUTPUT BUFFER
DO
(6)
ADD. RESS BUFFER
1:16 (Y) DECODER
A0 (2)
A1 (1)
A2 (15)
A3 (14)
A4 (7)
A5 (9)
A6 (10)
A7 (11)
An, An

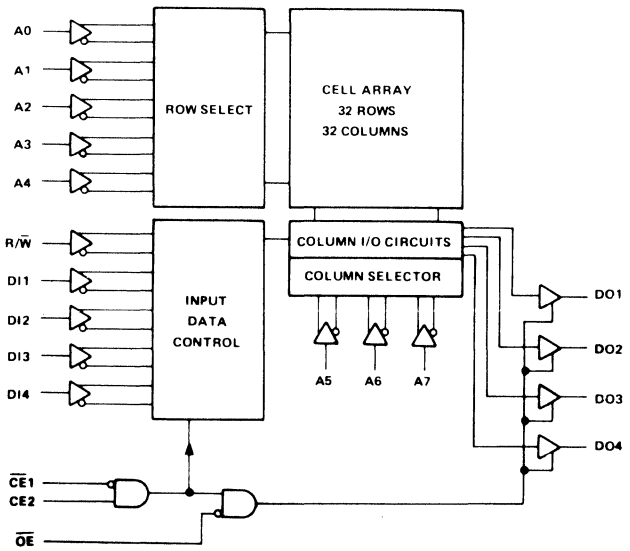
A8


A0
A1
A2
A3
A4
VCC
GROUND
R/W
DATA IN
CE
1 OF 32 ROW DECODE
32 ROWS BY 32 COLUMNS STATIC MEMORY STORAGE ELEMENTS
READ/ WRITE CONTROL
I/O CONTROL
1 OF 32 COLUMN DECODE
OUTPUT BUFFER
DATA OUT
A5
A6
A7
A8
A9

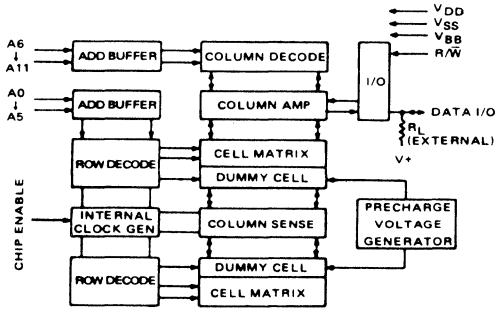

A6 1
A5 2
R/W 3
A1 4
A2 5
A3 6
A4 7
A0 8
16 A7
15 A8
14 A9
13 CE
12 DATA OUT
11 DATA IN
10 VCC
9 GND

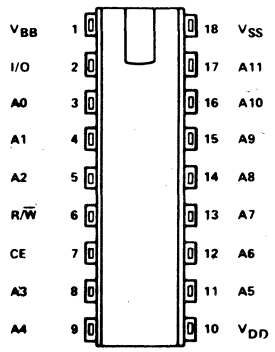
A10





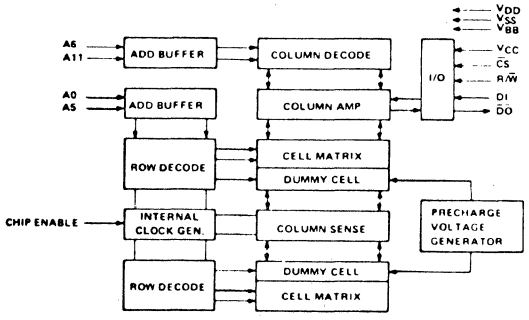
A12

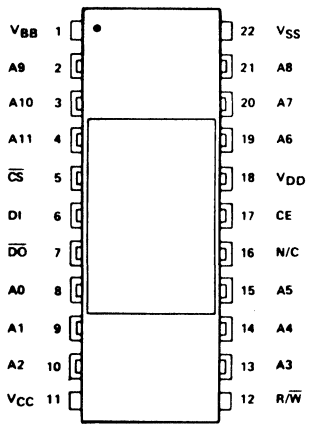




A12a: PIN 7 — $\overline{CE}$

A13



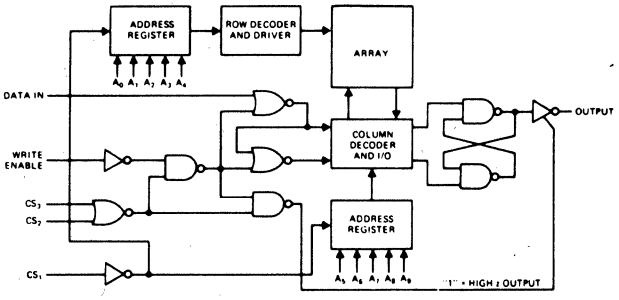


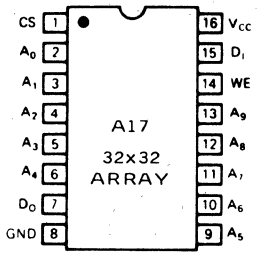
A14

PIN CONNECTION

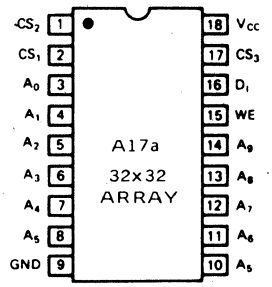
VBB	1	24	A3
A2	2	23	A4
A1	3	22	VSS
A0	4	21	CS
CE	5	20	RE
VDD	6	19	A5
VCC	7	18	A6
WE	8	17	A7
D11	9	16	D14
DØ1	10	15	DØ4
D12	11	14	D13
DØ2	12	13	D03

A17

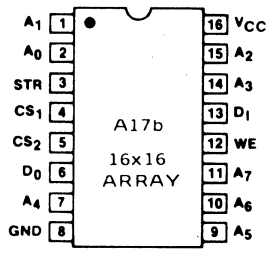




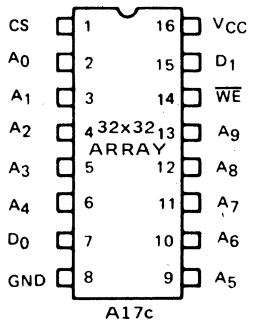
TOP VIEW



TOP VIEW

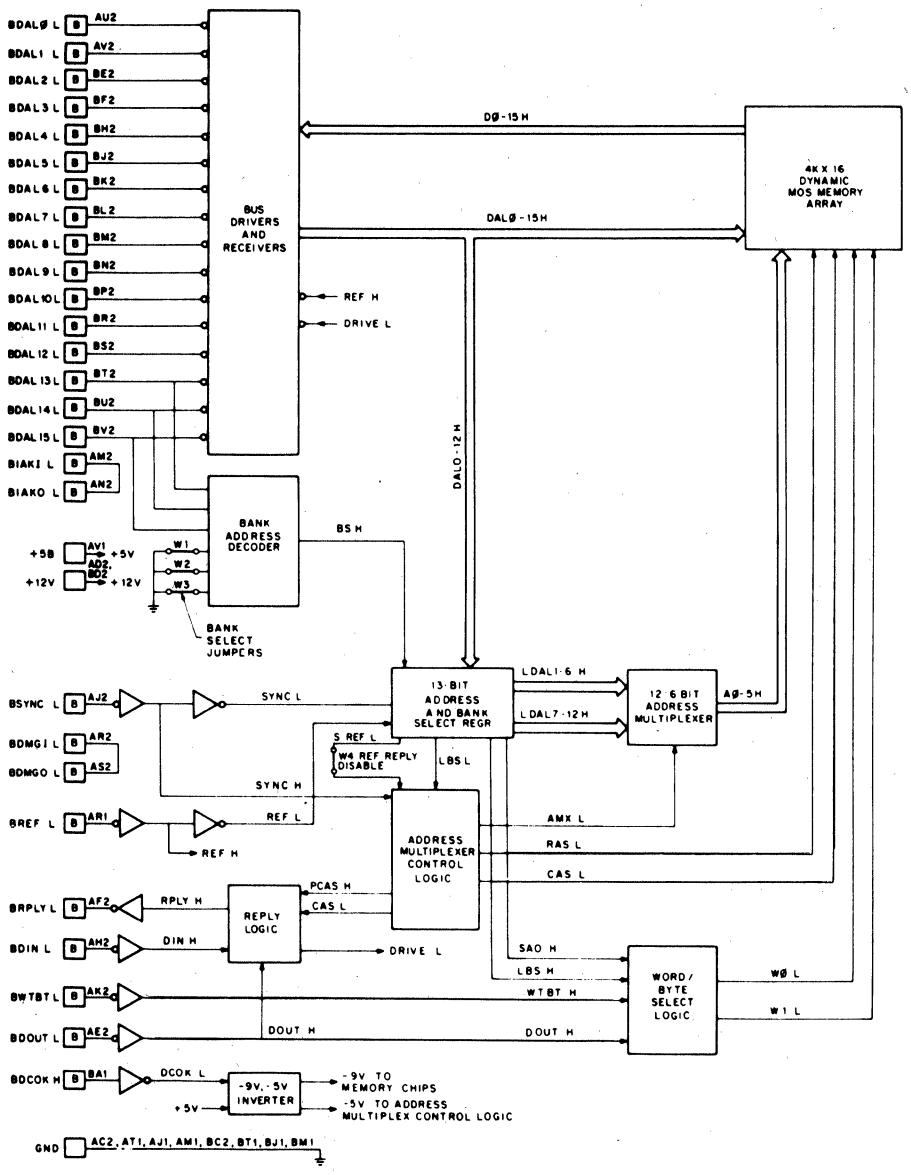


TOP VIEW

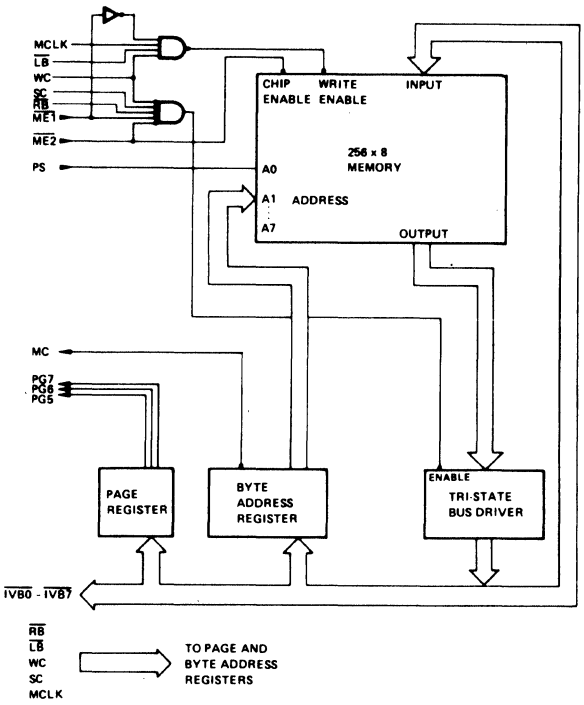


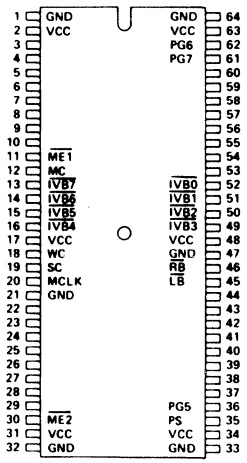
A17c

A19

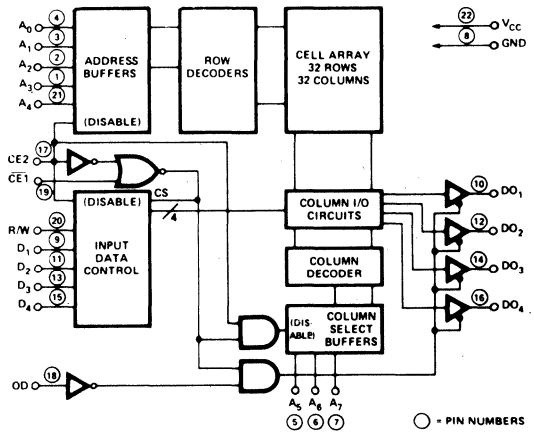


A20

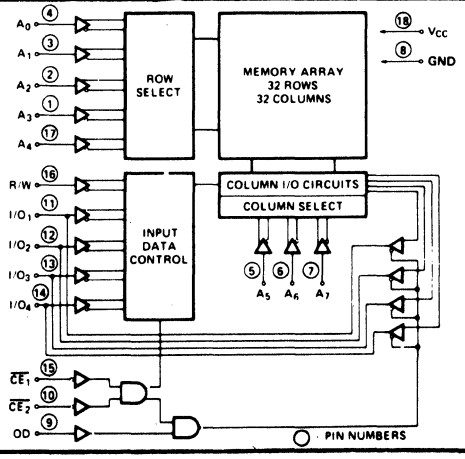

MCLK
LB
WC
SC
RB
ME1
ME2
PS
CHIP ENABLE
WRITE ENABLE
INPUT
256 x 8 MEMORY
A0
A1
ADDRESS
A7
OUTPUT
MC
PG7
PG6
PG5
PAGE REGISTER
BYTE ADDRESS REGISTER
ENABLE
TRI-STATE BUS DRIVER
IVB0 - IVB7
RB
LB
WC
SC
MCLK
TO PAGE AND BYTE ADDRESS REGISTERS


1 GND
2 VCC
3
4
5
6
7
8
9
10
11 ME1
12 MC
13 IVB7
14 IVB6
15 IVB5
16 IVB4
17 VCC
18 WC
19 SC
20 MCLK
21 GND
22
23
24
25
26
27
28
29
30 ME2
31 VCC
32 GND
64 GND
63 VCC
62 PG6
61 PG7
60
59
58
57
56
55
54
53
52 IVB0
51 IVB1
50 IVB2
49 IVB3
48 VCC
47 GND
46 RB
45 LB
44
43
42
41
40
39
38
37
36 PG5
35 PS
34 VCC
33 GND

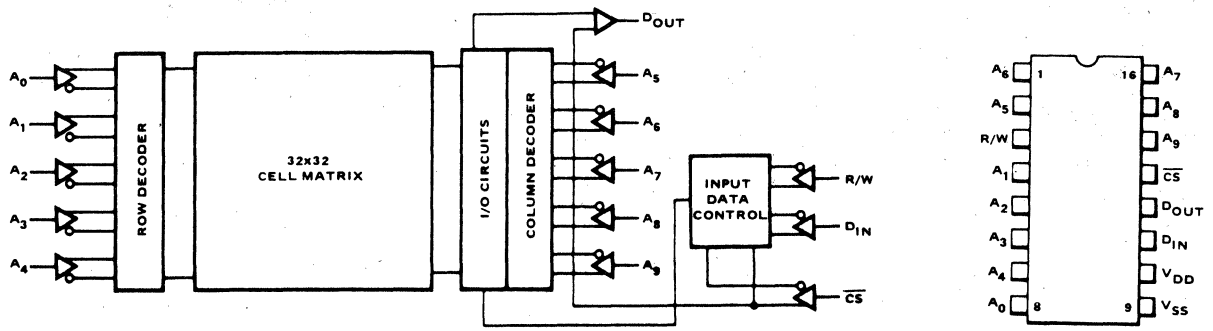
A21


A0 4
A1 3
A2 2
A3 1
A4 21
ADDRESS BUFFERS
(DISABLE)
ROW DECODERS
CELL ARRAY 32 ROWS 32 COLUMNS
22 VCC
8 GND
CE2 17
CE1 19
(DISABLE)
CS
4
R/W 20
D1 9
D2 11
D3 13
D4 15
INPUT DATA CONTROL
COLUMN I/O CIRCUITS
COLUMN DECODER
(DISABLE)
COLUMN SELECT BUFFERS
OD 18
10 DO1
12 DO2
14 DO3
16 DO4
A5 A6 A7
5 6 7
○ = PIN NUMBERS

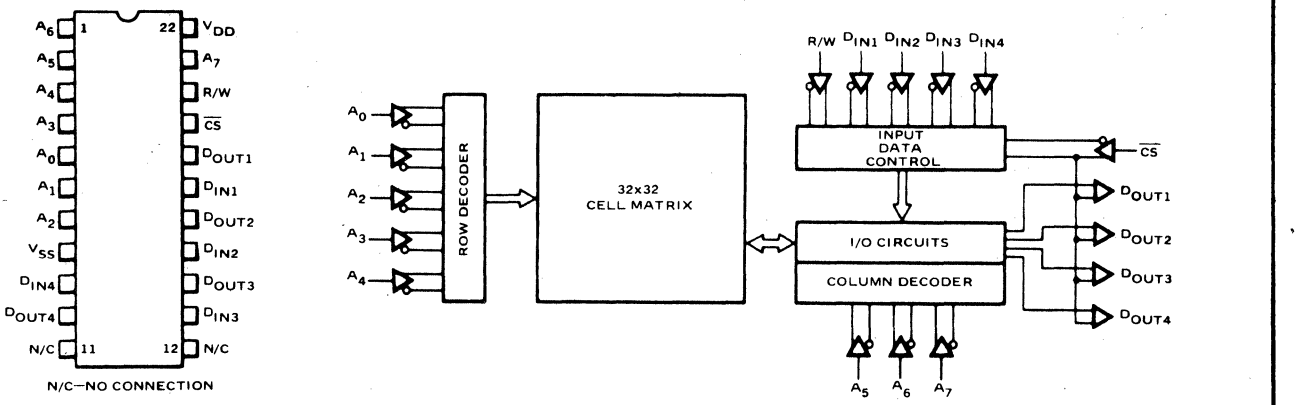
A22


A0 4
A1 3
A2 2
A3 1
A4 17
ROW SELECT
MEMORY ARRAY 32 ROWS 32 COLUMNS
18 VCC
8 GND
R/W 16
I/O1 11
I/O2 12
I/O3 13
I/O4 14
INPUT DATA CONTROL
COLUMN I/O CIRCUITS
COLUMN SELECT
5 6 7
A5 A6 A7
CE1 15
CE2 10
OD 9
○ - PIN NUMBERS

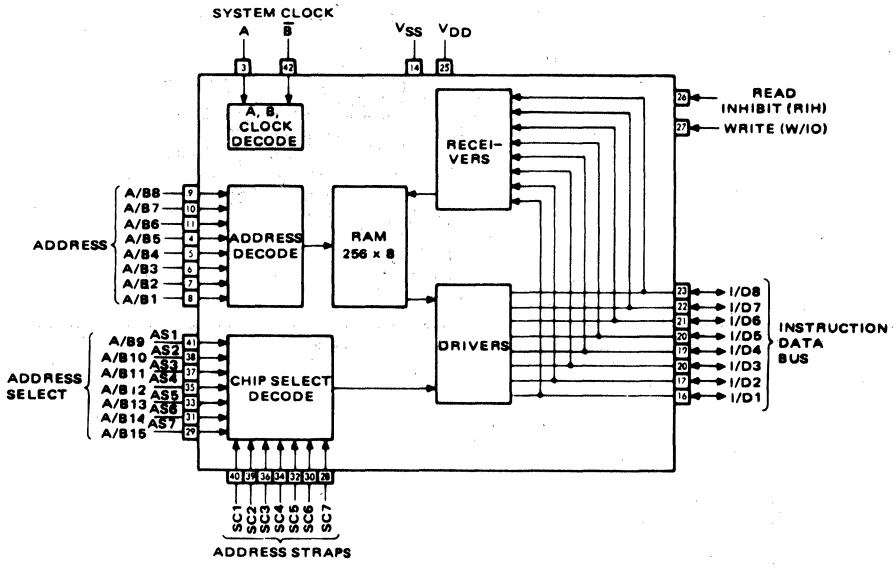
A23



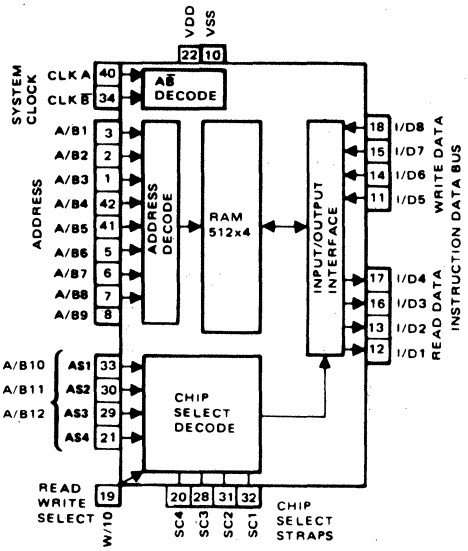
A24



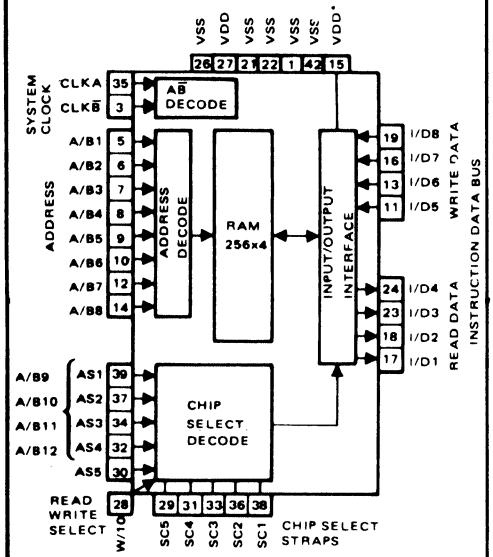
A27



A28

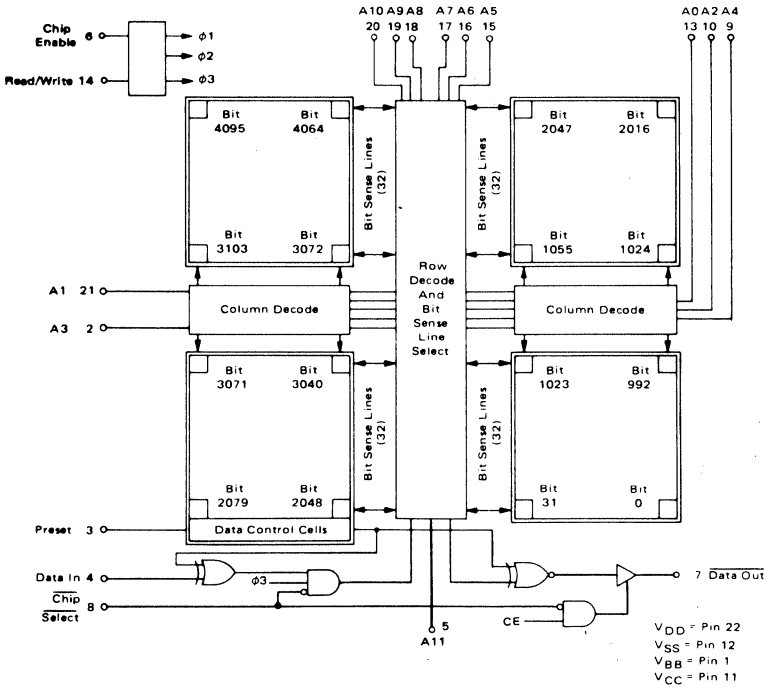


A29

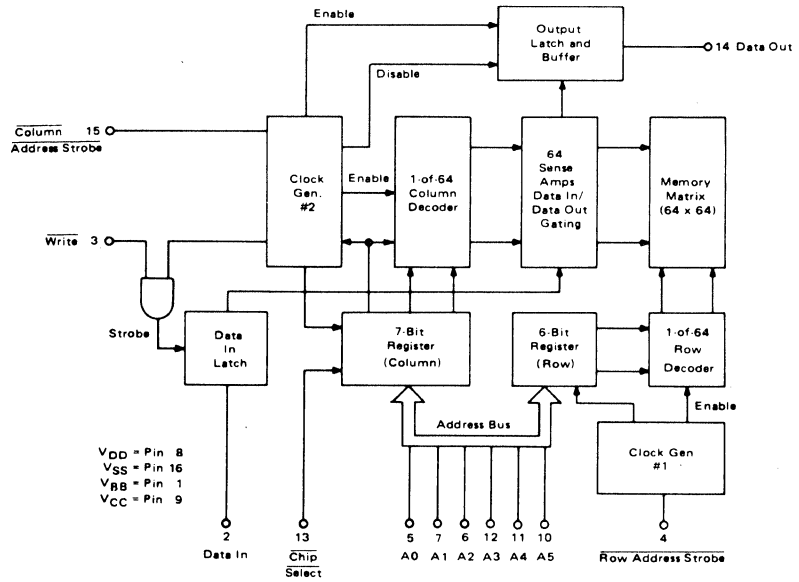


THIS INPUT IS A SEPARATE VDD SOURCE FOR THE OUTPUT DRIVERS. THIS IS USEFUL FOR ISOLATING INDIVIDUAL CIRCUITS DURING DEVICE TESTING AND FOR FAULT ISOLATION WHEN MULTIPLE CIRCUITS ARE CONNECTED TO THE DATA BUS.

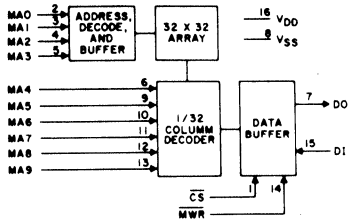
A30



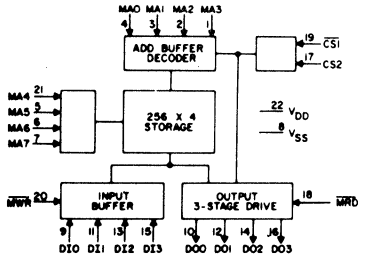
A31



A32



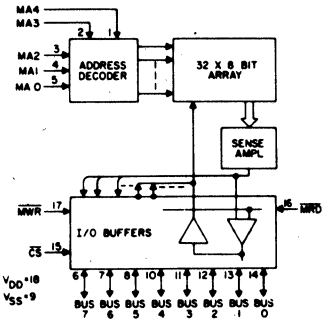
A33



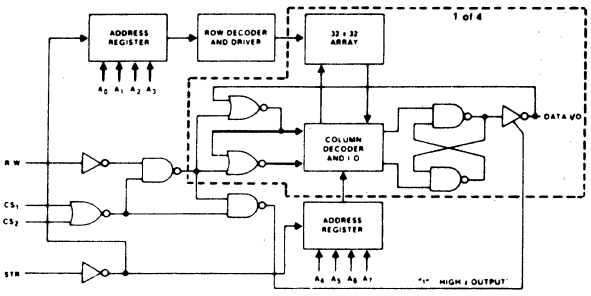
19. LOGIC/BLOCK DRAWINGS

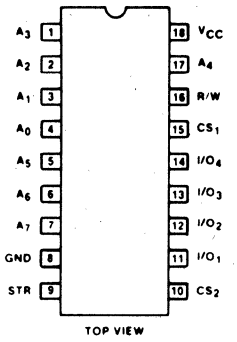
IN DRAWING NUMBER SEQUENCE

A34

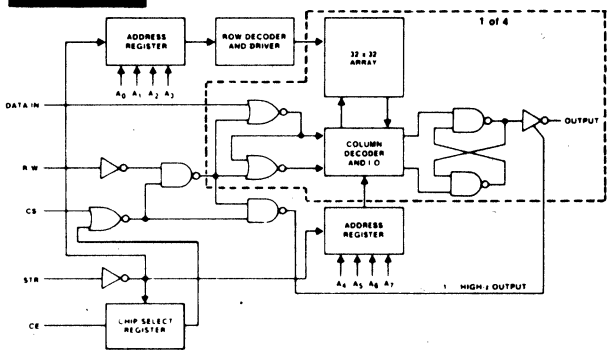


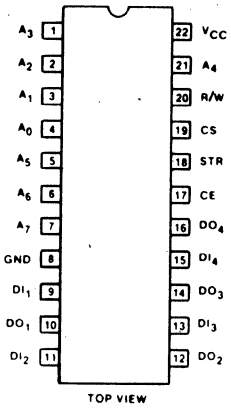
A36



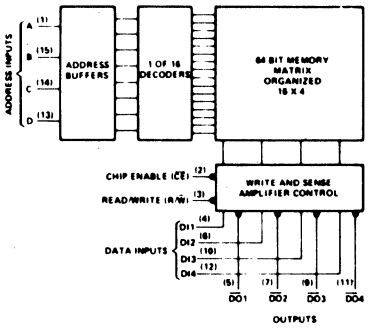


A37

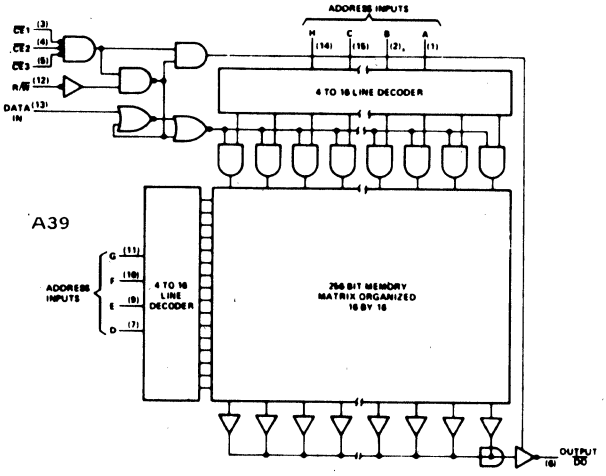




A38

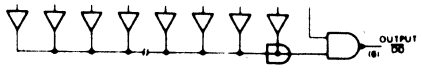


A39

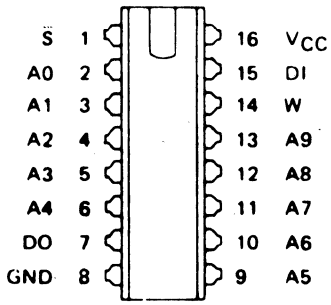


A39a

SAME AS A39 EXCEPT OUTPUT IS AS SHOWN BELOW.

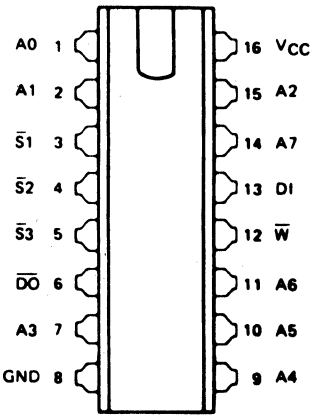


A40



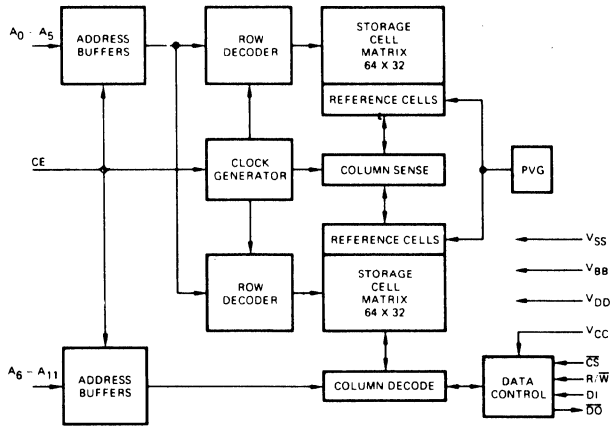
A40a: PIN1—E/S

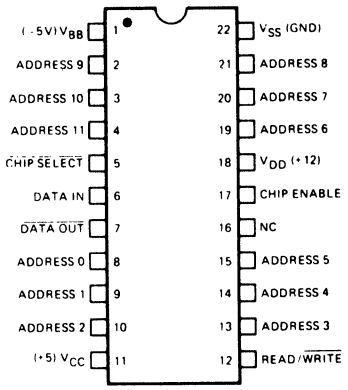
A41



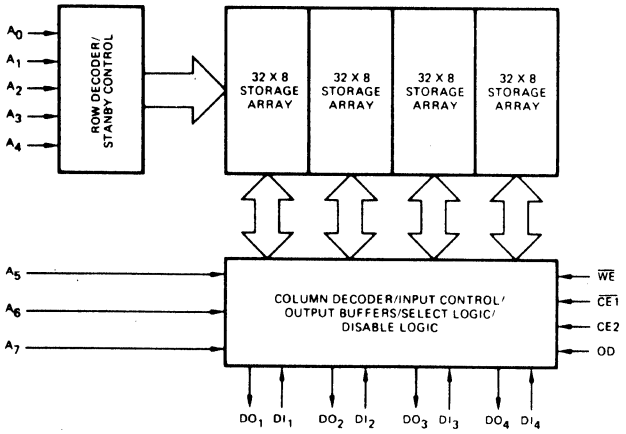
A41a:
PIN 3—$\overline{E}_1/\overline{S}_1$
PIN 4—$\overline{E}_2/\overline{S}_2$
PIN 5—E_3/S_3

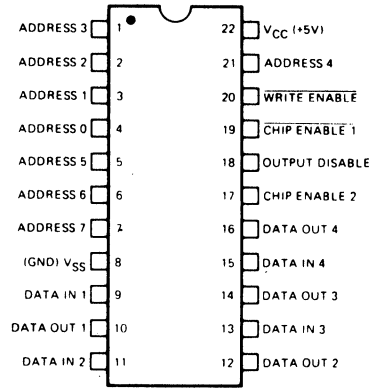
A42



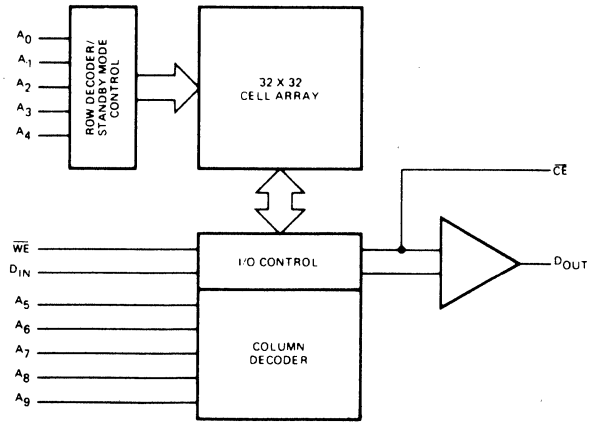


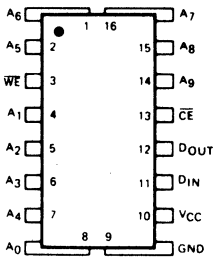
A43



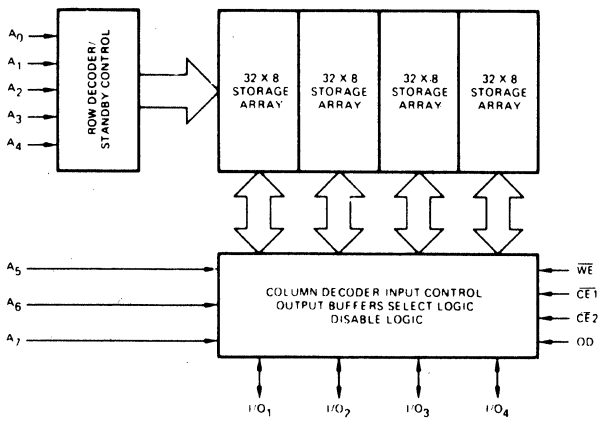


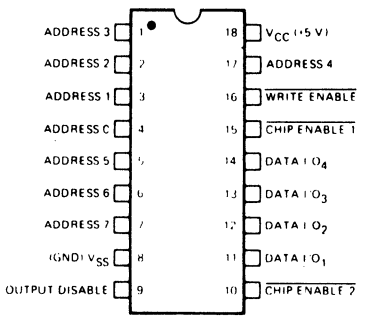
A44





A45

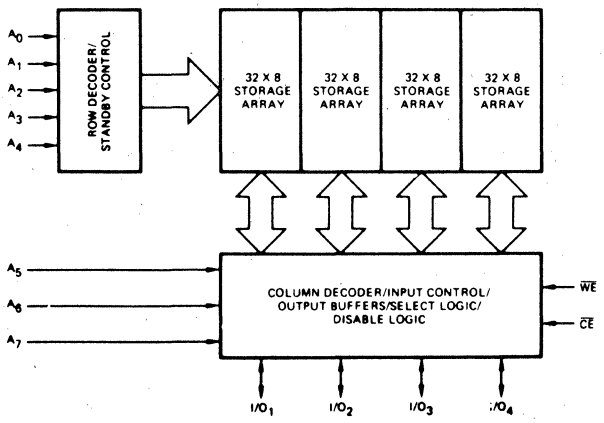


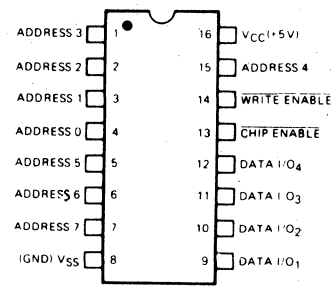


19. LOGIC/BLOCK DRAWINGS

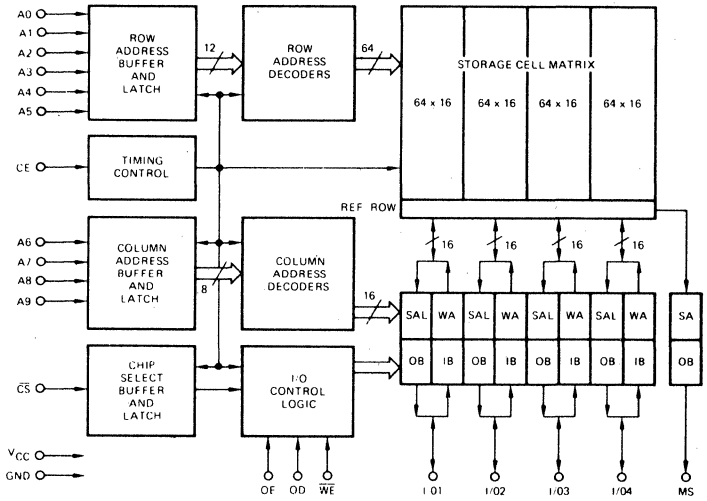
IN DRAWING NUMBER SEQUENCE

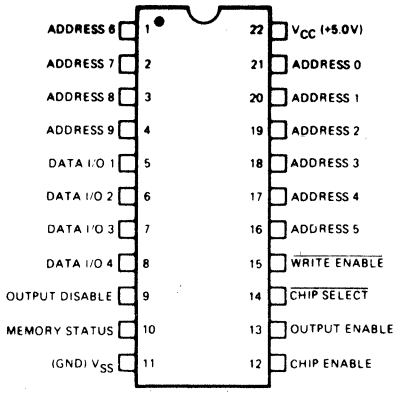
A46



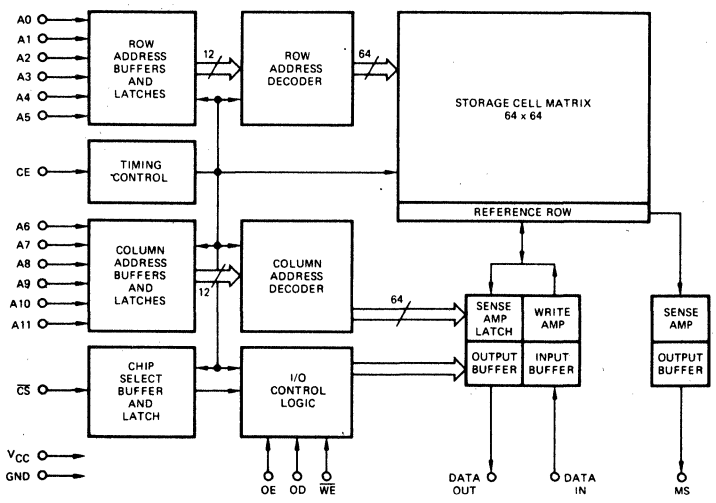


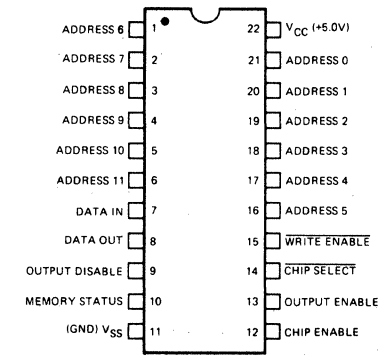
A47





A48

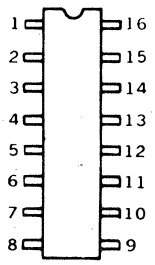




Top View

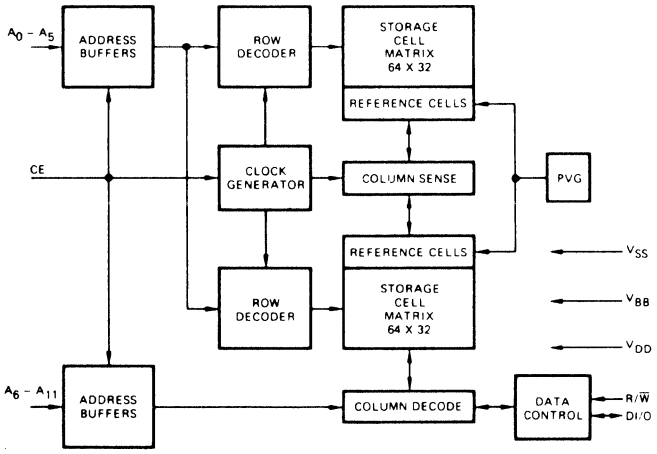
Pin 1 is marked for orientation.

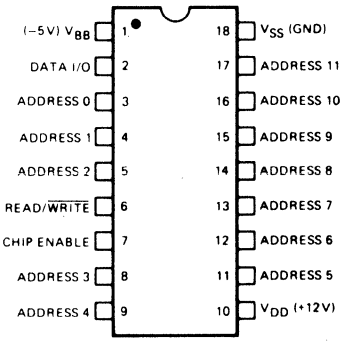
A49



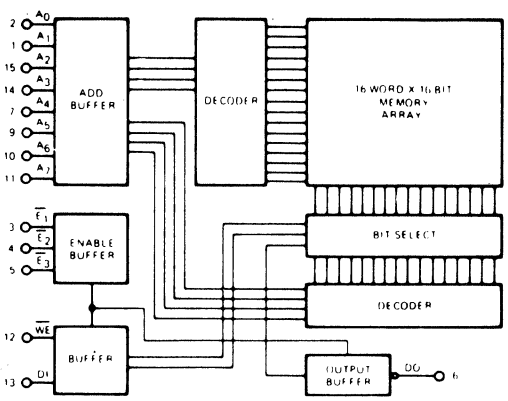
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A49	A1	A0	CS1	CS2	CS3	DO	A4	GND	A5	A6	A7	WE	DI	A3	A2	VCC

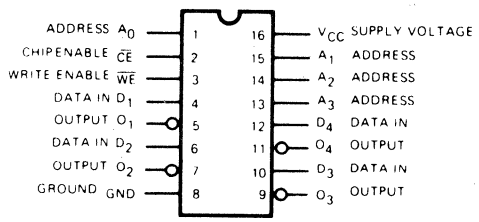
A50



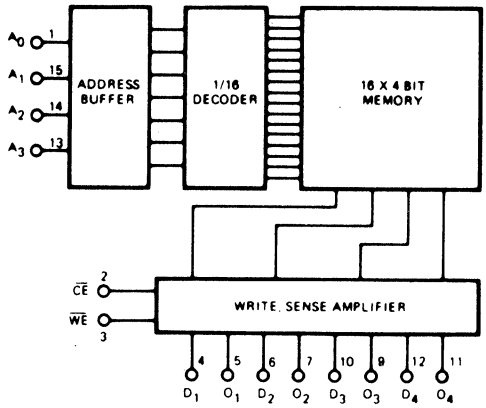


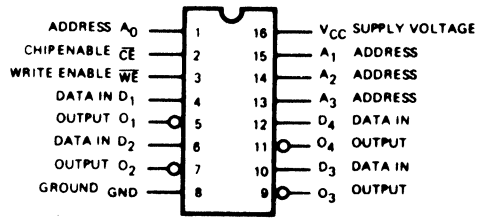
A51





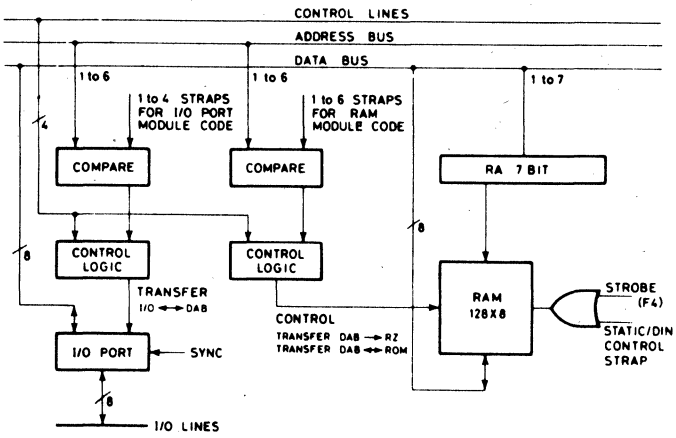
A52

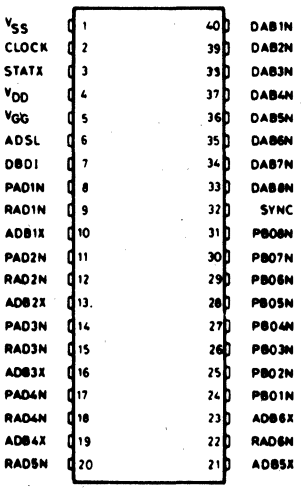




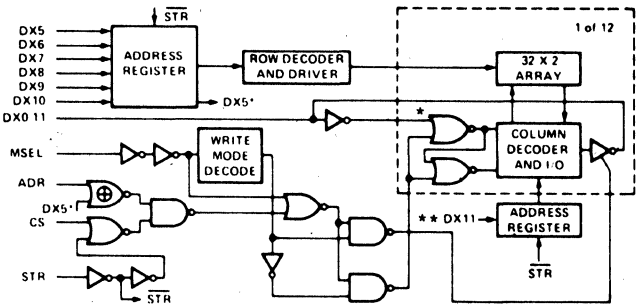
V_{CC} = 16
GND = 8

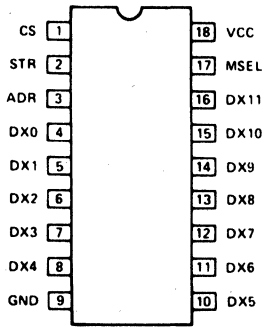
A54





A55



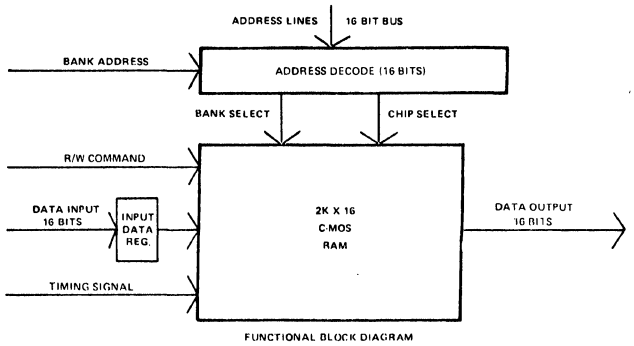


* A55a HAS INVERTING INPUT
** A55a IS Dx8

19. LOGIC/BLOCK DRAWINGS

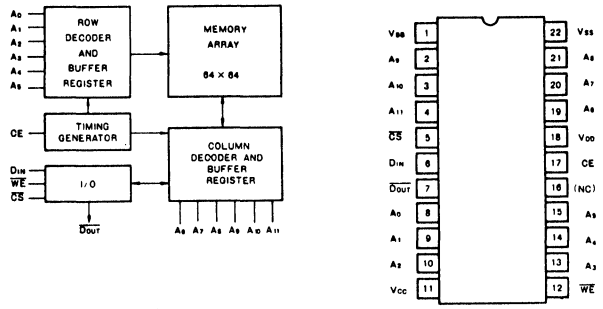
IN DRAWING NUMBER SEQUENCE

A56

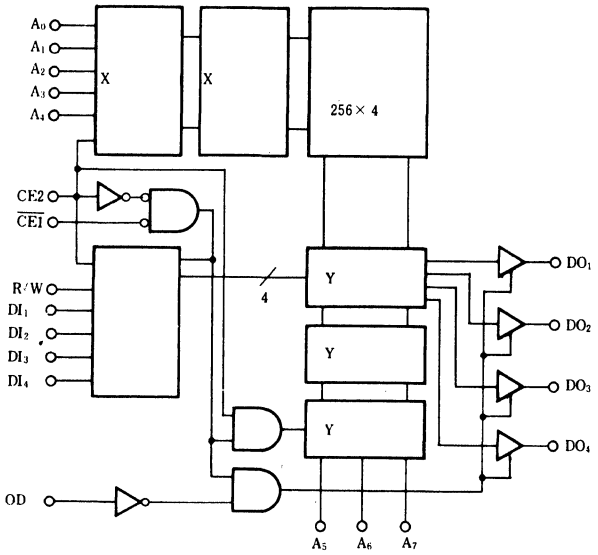


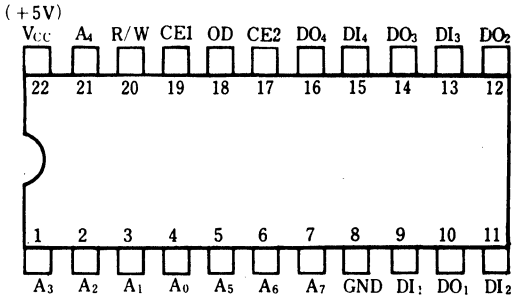
FUNCTIONAL BLOCK DIAGRAM

A57

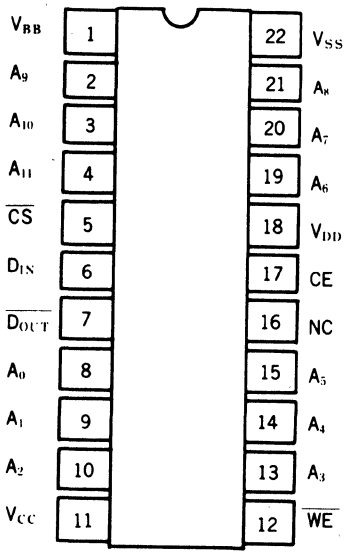


A58

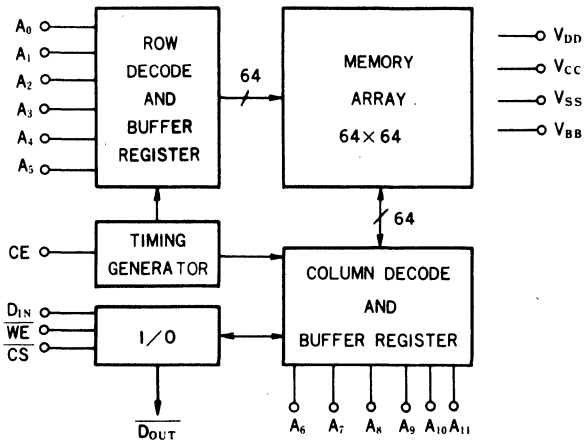




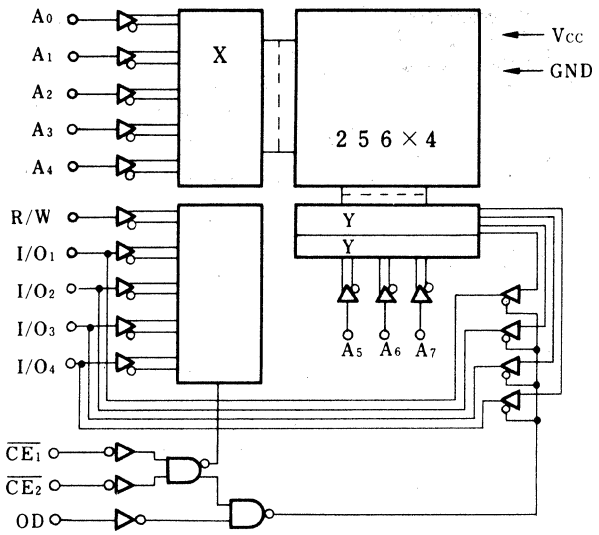
A59

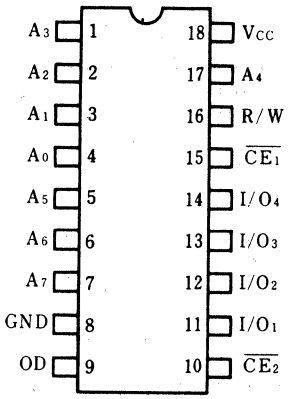


$A_0 \sim A_{11}$	Address Inputs
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power(+12V)
V_{CC}	Power(+5V)
V_{SS}	Ground
V_{BB}	Power(−5V)
NC	Not Connected
$A_0 \sim A_5$	Refresh Addresses

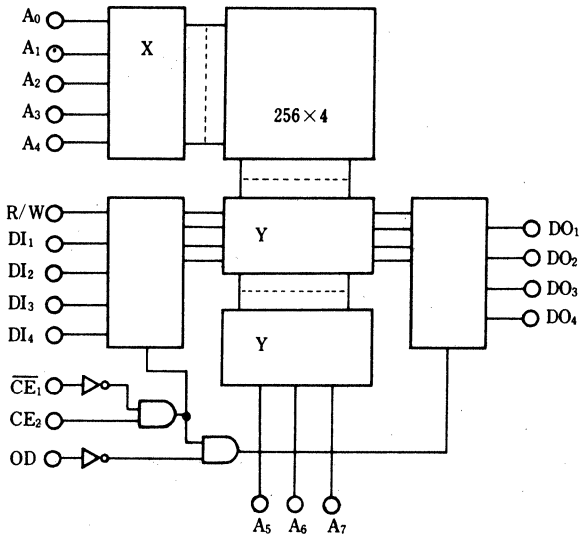


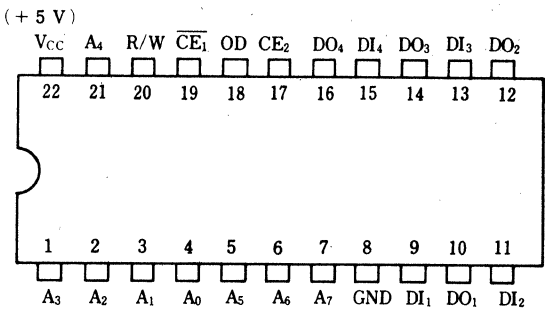
A60


A0
A1
A2
A3
A4
X
256×4
Vcc
GND
R/W
I/O1
I/O2
I/O3
I/O4
Y
Y
A5 A6 A7
CE1
CE2
OD

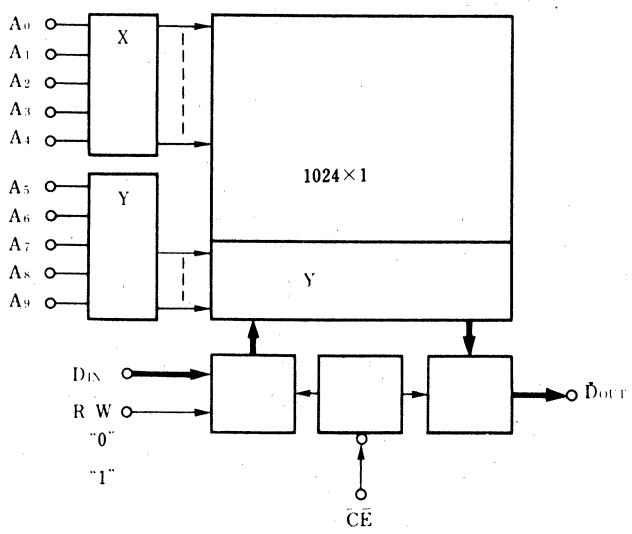

A3 1 18 Vcc
A2 2 17 A4
A1 3 16 R/W
A0 4 15 CE1
A5 5 14 I/O4
A6 6 13 I/O3
A7 7 12 I/O2
GND 8 11 I/O1
OD 9 10 CE2

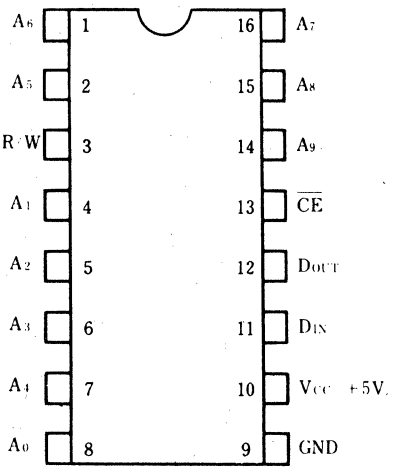
A61


A0
A1
A2
A3
A4
X
256×4
R/W
DI1
DI2
DI3
DI4
Y
Y
DO1
DO2
DO3
DO4
CE1
CE2
OD
A5 A6 A7

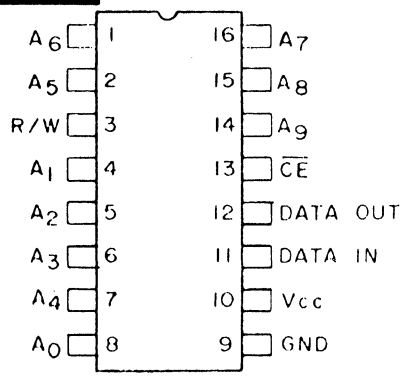

(+5V)
Vcc A4 R/W CE1 OD CE2 DO4 DI4 DO3 DI3 DO2
22 21 20 19 18 17 16 15 14 13 12
1 2 3 4 5 6 7 8 9 10 11
A3 A2 A1 A0 A5 A6 A7 GND DI1 DO1 DI2

A62

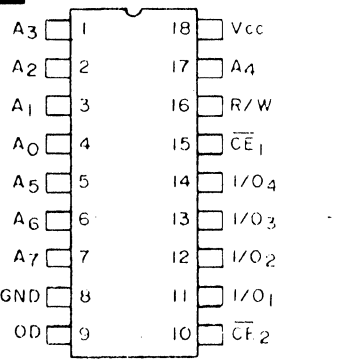

A0
A1
A2
A3
A4
X
1024×1
A5
A6
A7
A8
A9
Y
Y
DIN
R/W
"0"
"1"
DOUT
CE


A6 1 16 A7
A5 2 15 A8
R/W 3 14 A9
A1 4 13 CE
A2 5 12 DOUT
A3 6 11 DIN
A4 7 10 Vcc +5V
A0 8 9 GND

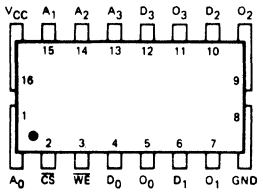
A63

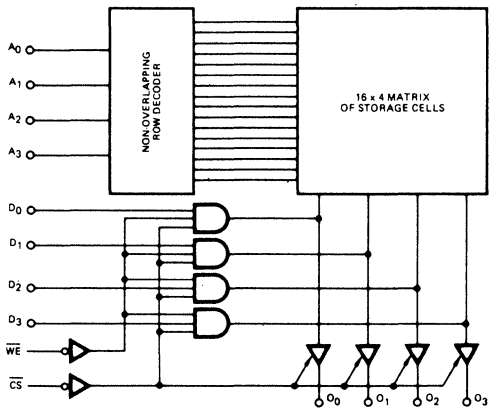


A64

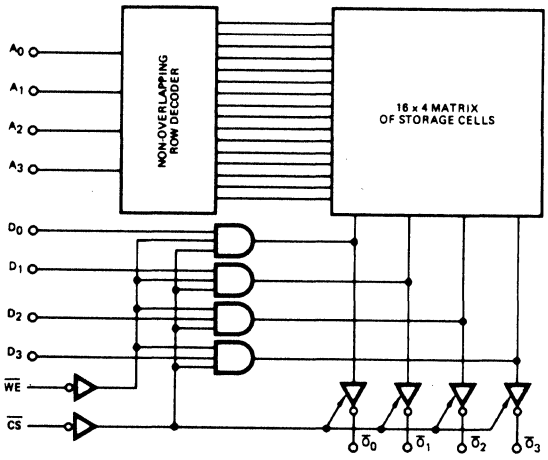


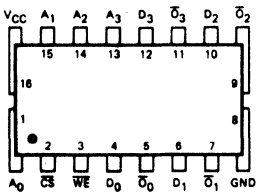
A65



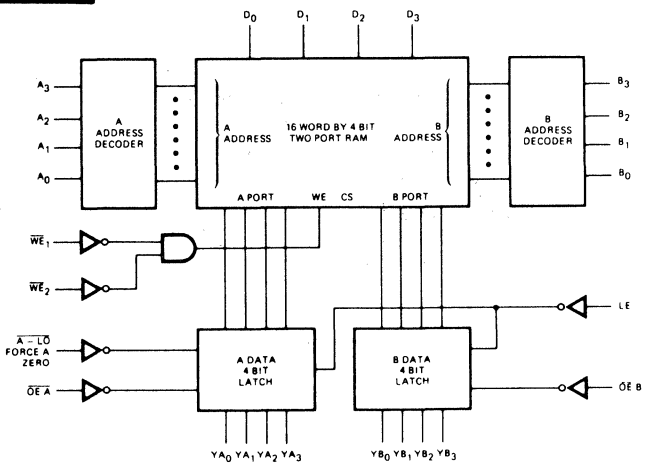


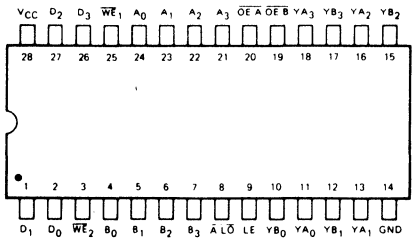
A66



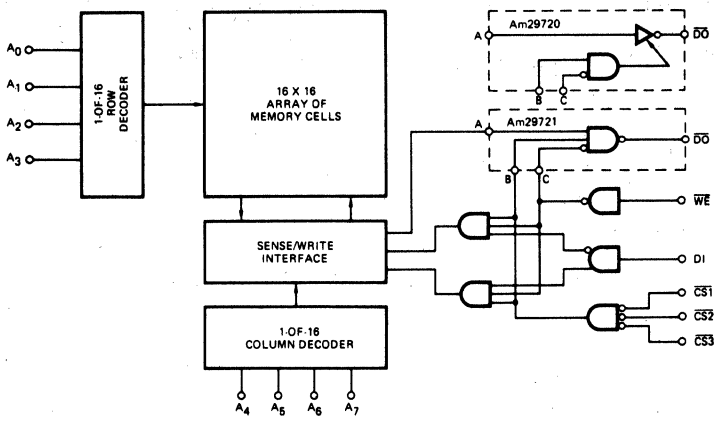


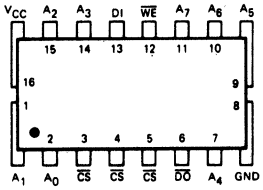
A67



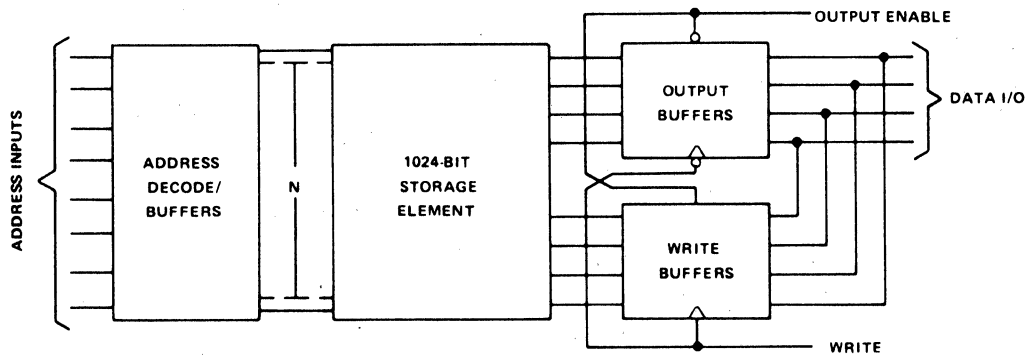


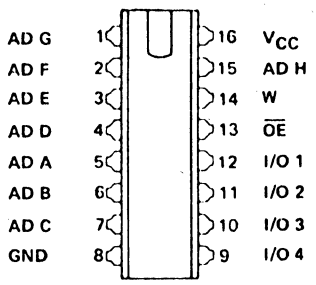
A68


A0
A1
A2
A3
1-OF-16 ROW DECODER
16 X 16 ARRAY OF MEMORY CELLS
SENSE/WRITE INTERFACE
1-OF-16 COLUMN DECODER
A4
A5
A6
A7
Am29720
Am29721
DO
WE
DI
CS1
CS2
CS3

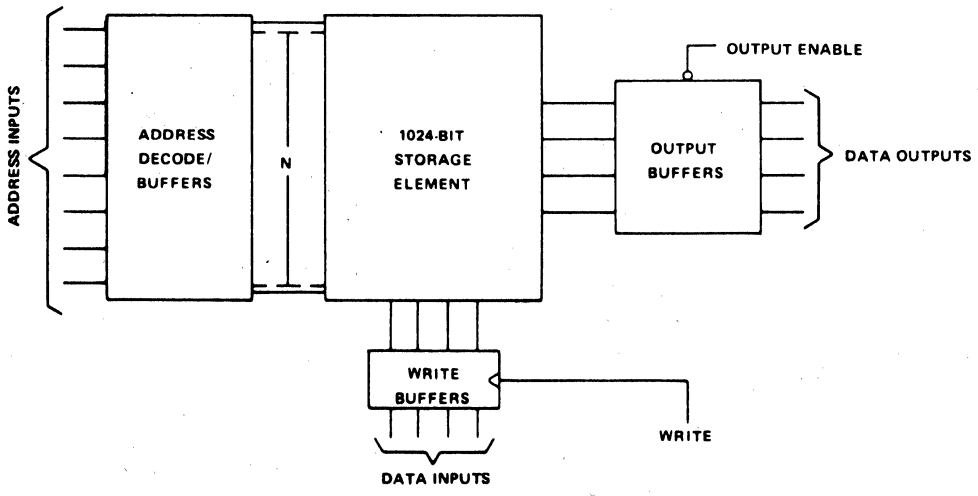

VCC A2 A3 DI WE A7 A6 A5
15 14 13 12 11 10
16 9
1 8
2 3 4 5 6 7
A1 A0 CS CS CS DO A4 GND

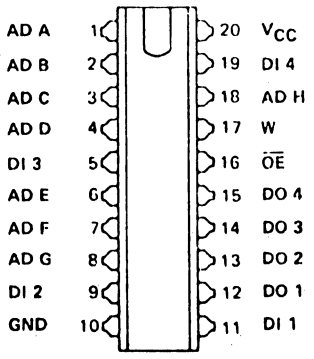
A73


ADDRESS INPUTS
ADDRESS DECODE/ BUFFERS
N
1024-BIT STORAGE ELEMENT
OUTPUT ENABLE
OUTPUT BUFFERS
DATA I/O
WRITE BUFFERS
WRITE

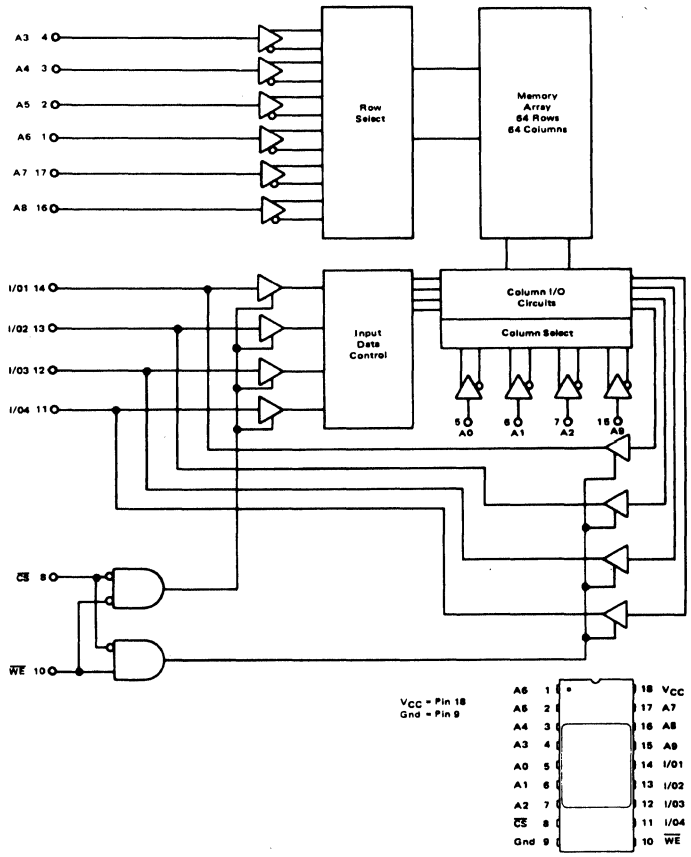

AD G 1
AD F 2
AD E 3
AD D 4
AD A 5
AD B 6
AD C 7
GND 8
16 VCC
15 AD H
14 W
13 OE
12 I/O 1
11 I/O 2
10 I/O 3
9 I/O 4

A74

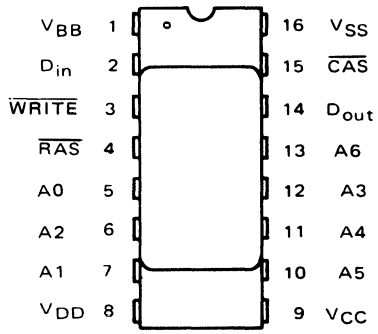

ADDRESS INPUTS
ADDRESS DECODE/ BUFFERS
N
1024-BIT STORAGE ELEMENT
OUTPUT ENABLE
OUTPUT BUFFERS
DATA OUTPUTS
WRITE BUFFERS
WRITE
DATA INPUTS


AD A 1
AD B 2
AD C 3
AD D 4
DI 3 5
AD E 6
AD F 7
AD G 8
DI 2 9
GND 10
20 VCC
19 DI 4
18 AD H
17 W
16 OE
15 DO 4
14 DO 3
13 DO 2
12 DO 1
11 DI 1

A76



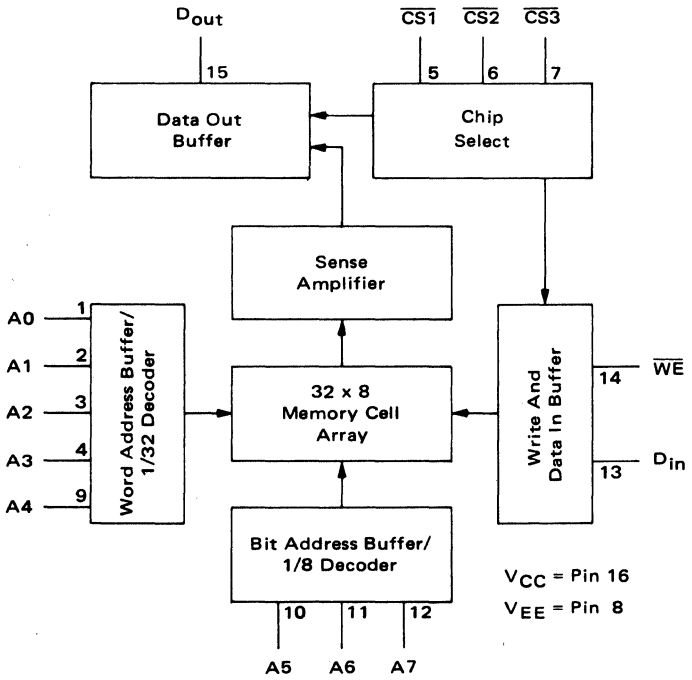
A77

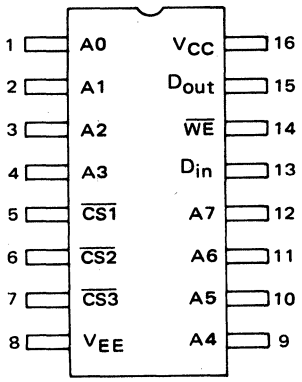


PIN NAMES

A0–A6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{in}	Data In
D_{out}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{BB}	Power (-5 V)
V_{CC}	Power (+5 V)
V_{DD}	Power (+12 V)
V_{SS}	Ground

A78





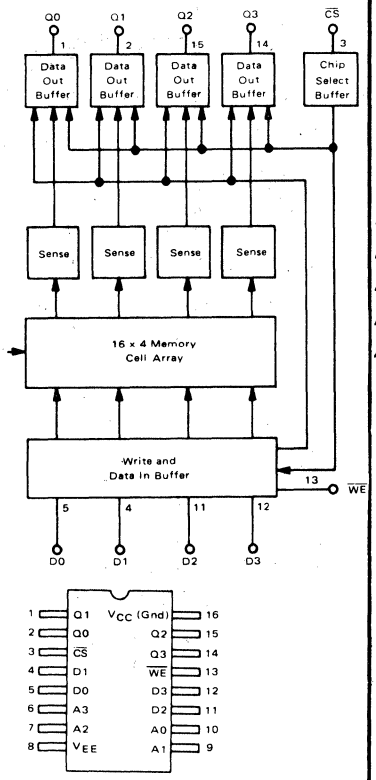
PIN NOTATION

CS	Chip Select Input
A0 thru A7	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

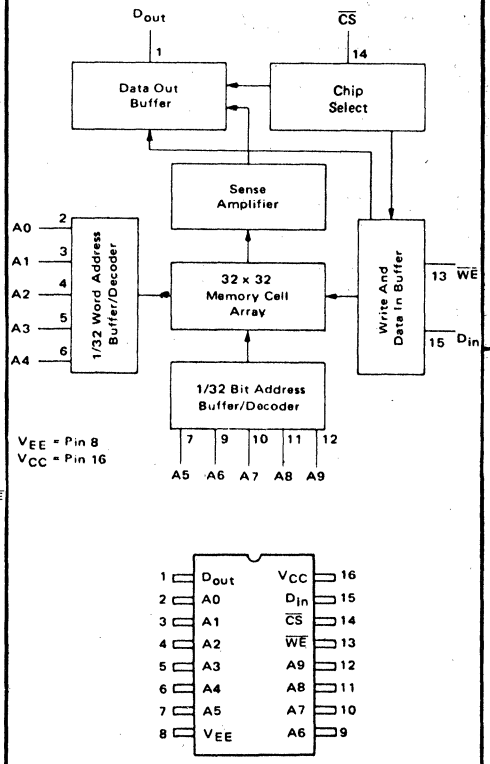
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

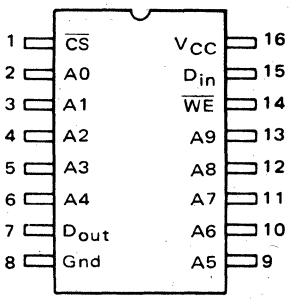
A79



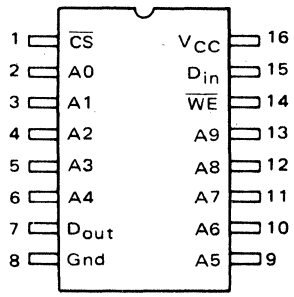
A80



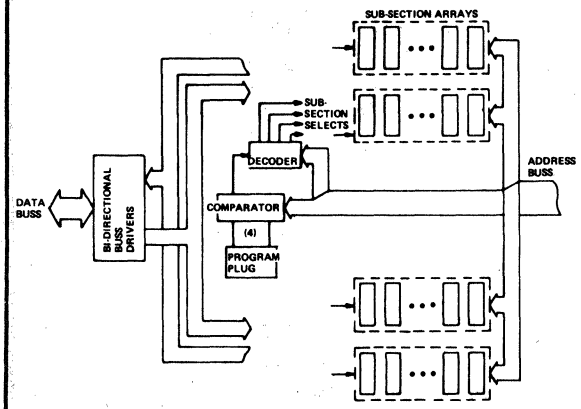
A81



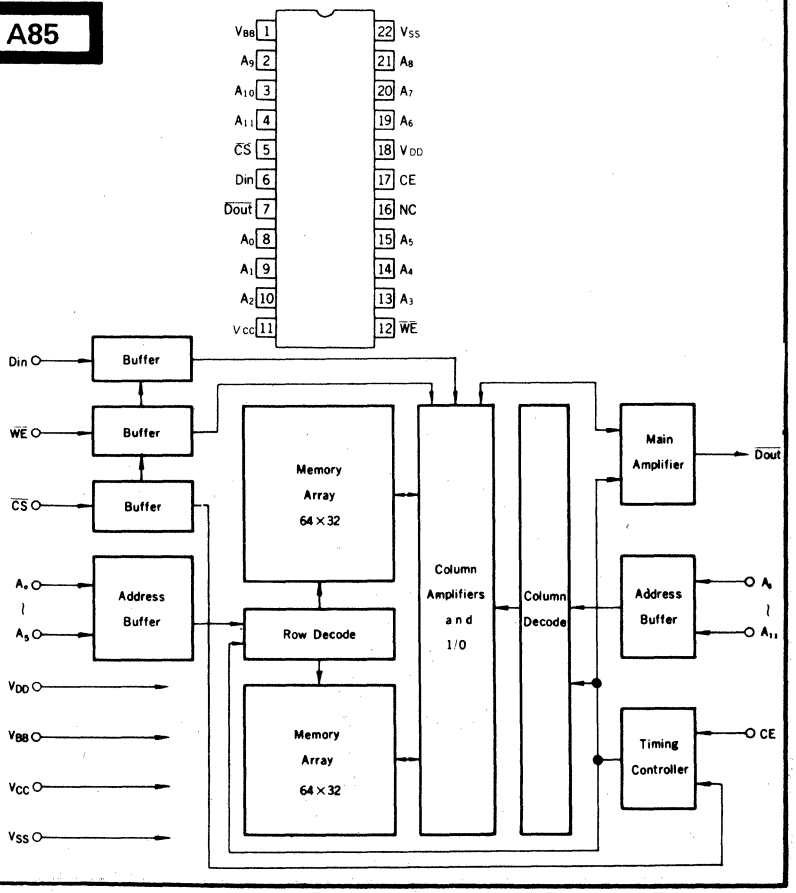
A82



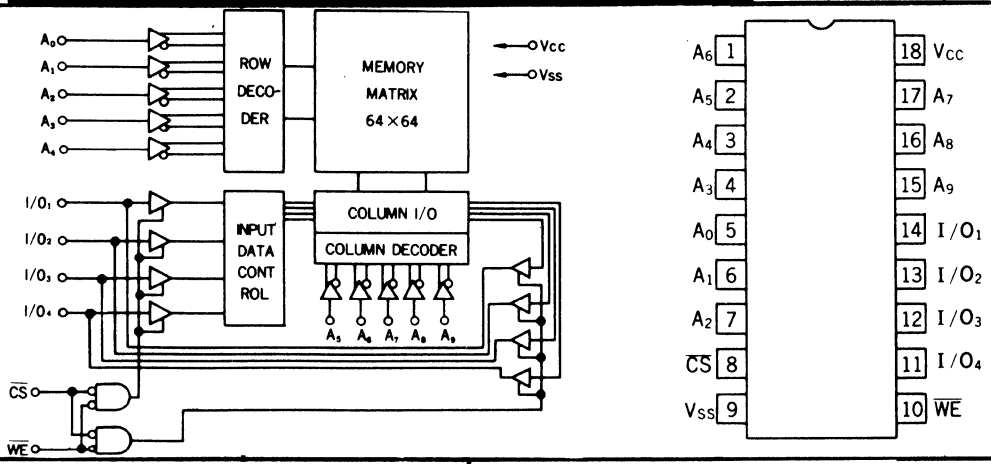
A83



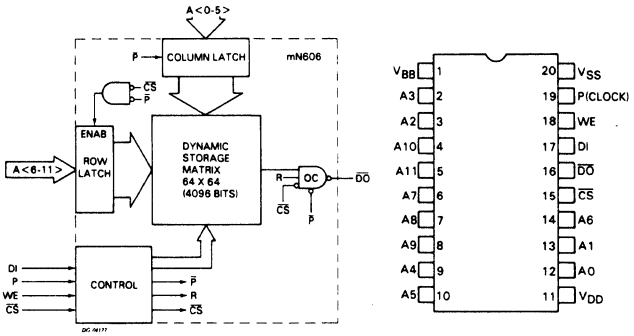
A85



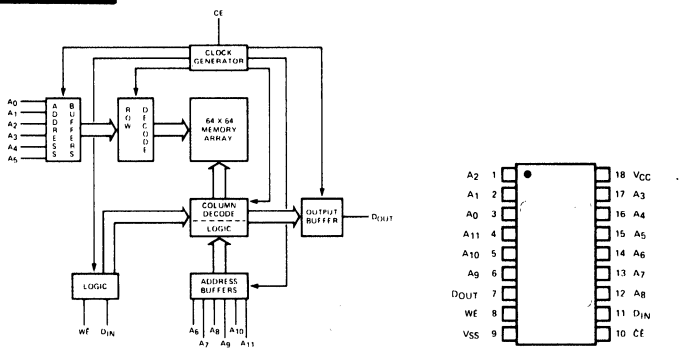
A86



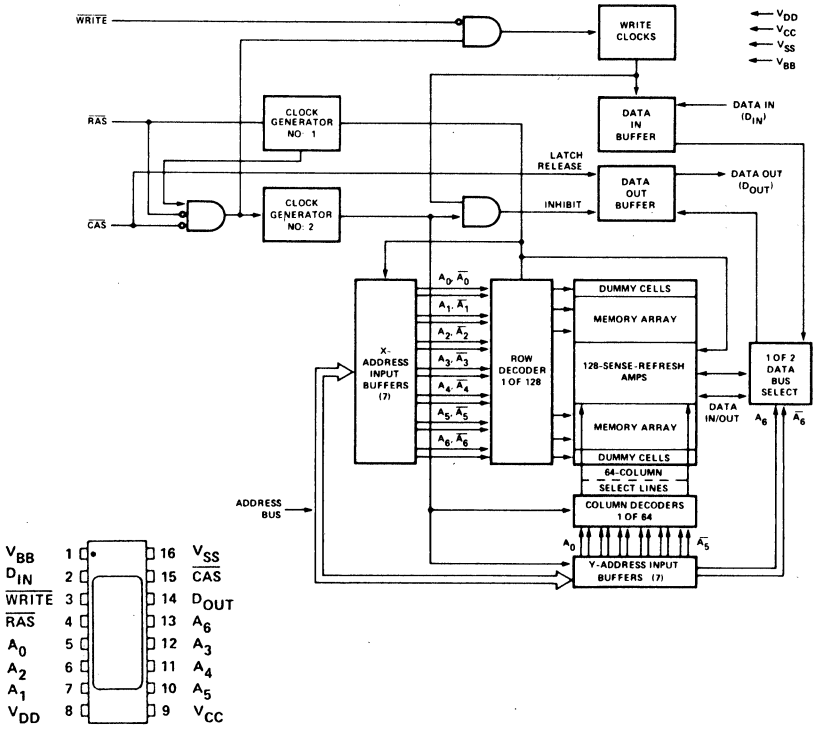
A87



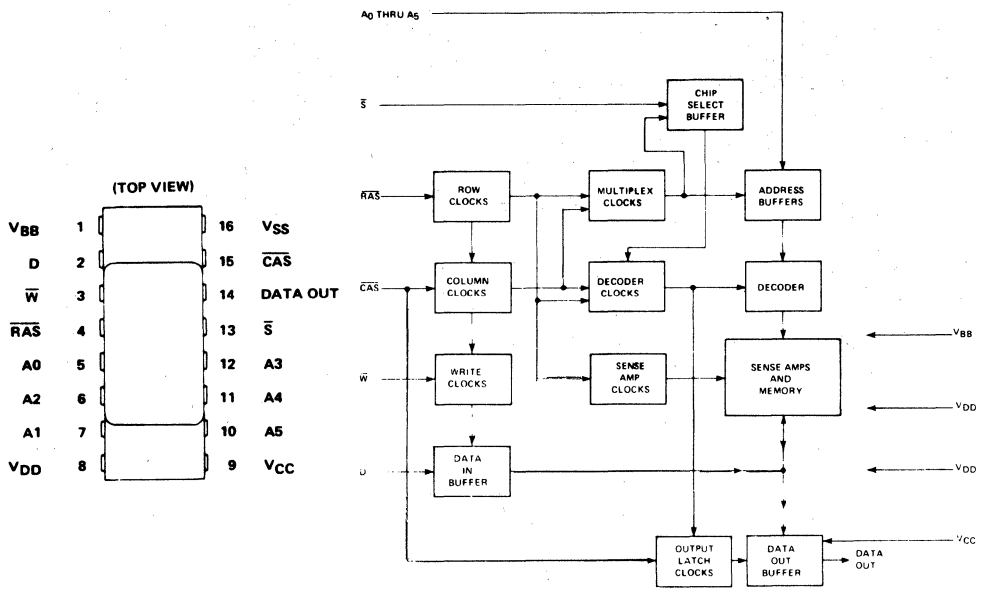
A89



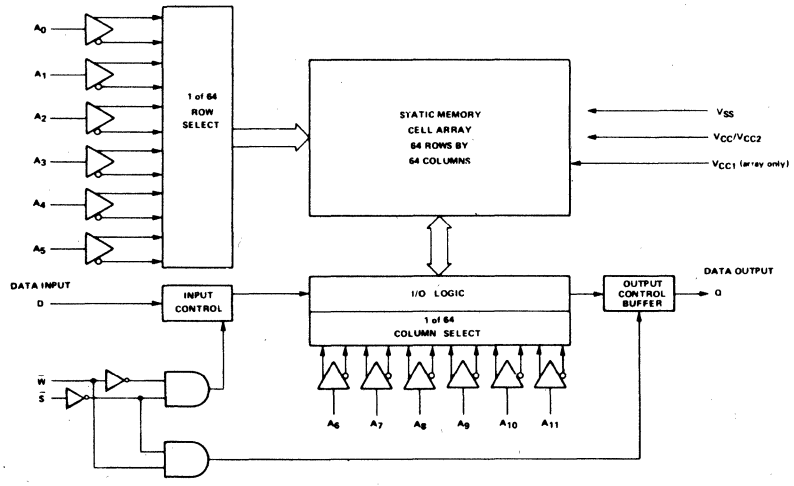
A90

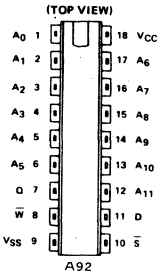


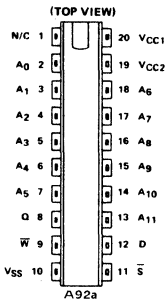
A91



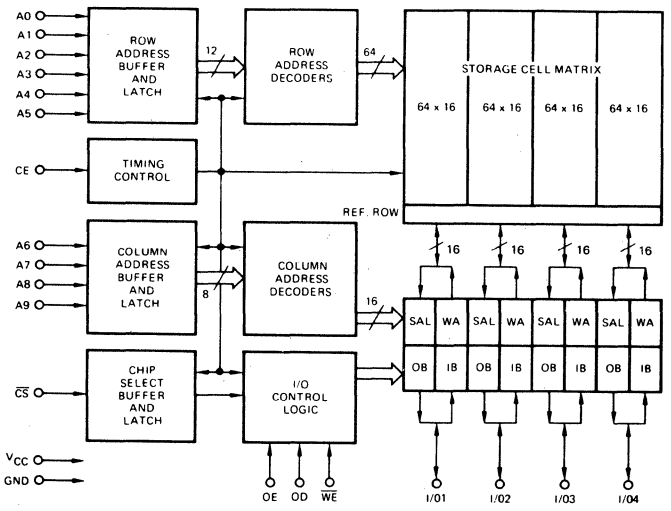
A92

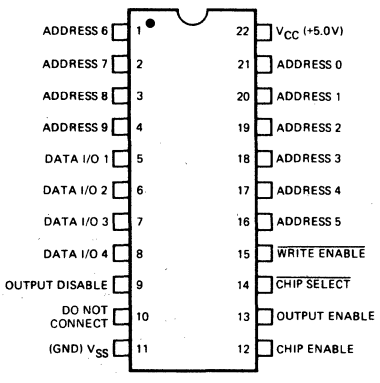






A95





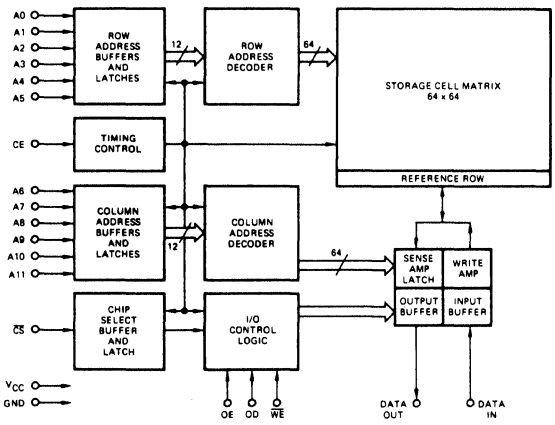
Top View

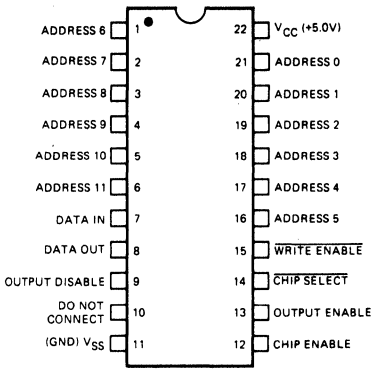
Pin 1 is marked for orientation.

19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

A96

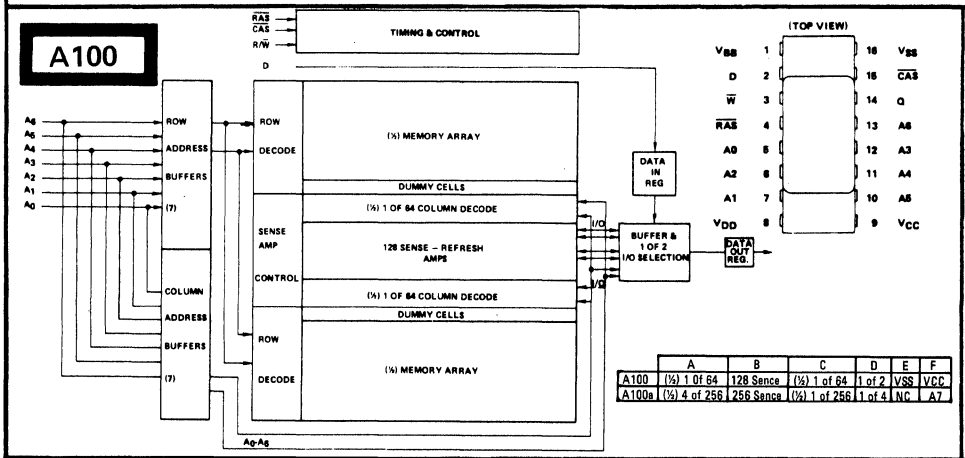




Top View

Pin 1 is marked for orientation.

A100

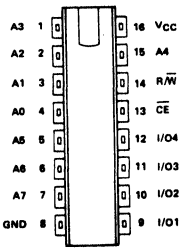


(TOP VIEW)

	A	B	C	D	E	F
A100	(½) 1 Of 64	128 Sence	(½) 1 of 64	1 of 2	VSS	VCC
A100a	(½) 4 of 256	256 Sence	(½) 1 of 256	1 of 4	NC	A7

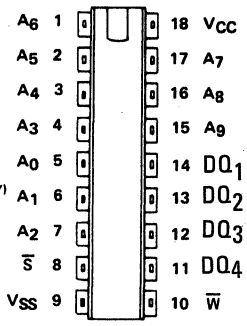
A103

(TOP VIEW)

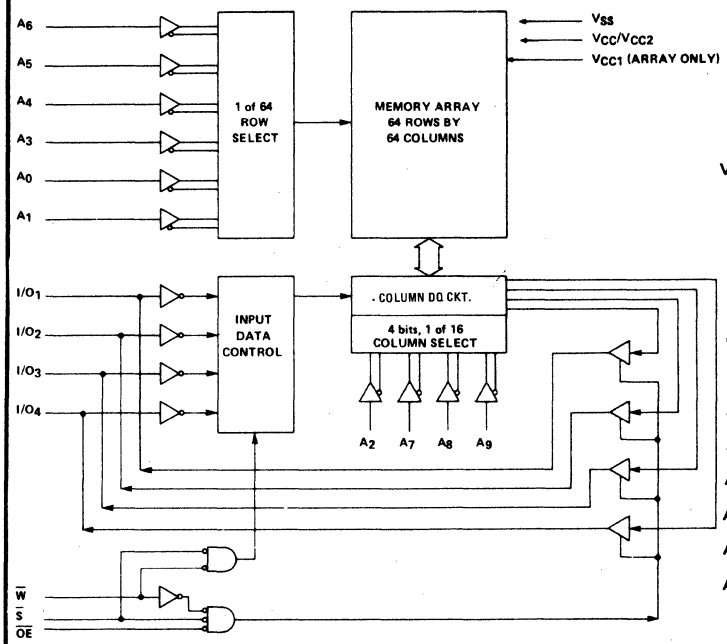


A104

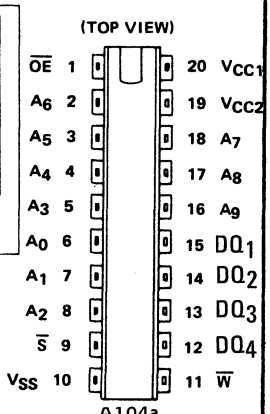
(TOP VIEW)



A104

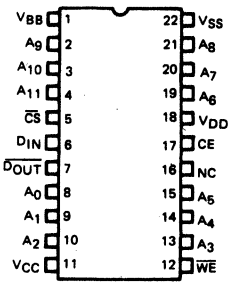


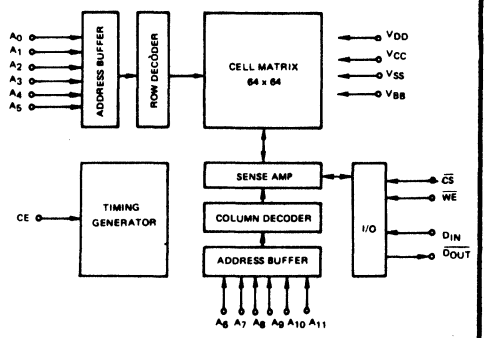
(TOP VIEW)



A104a

A106

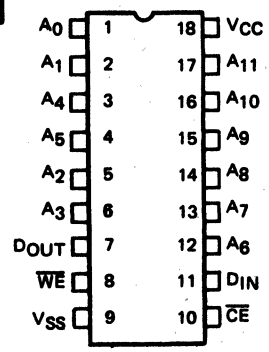


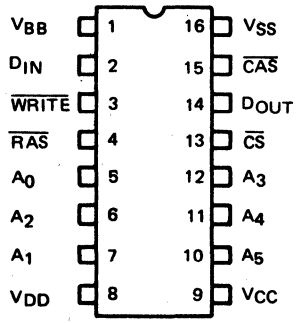


19. LOGIC/BLOCK DRAWINGS

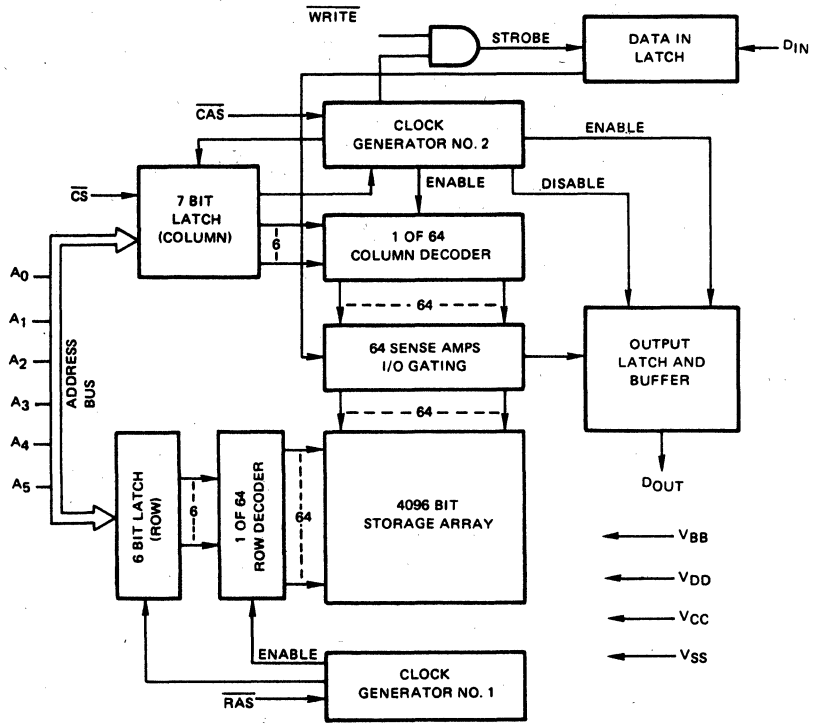
IN DRAWING NUMBER SEQUENCE

A107

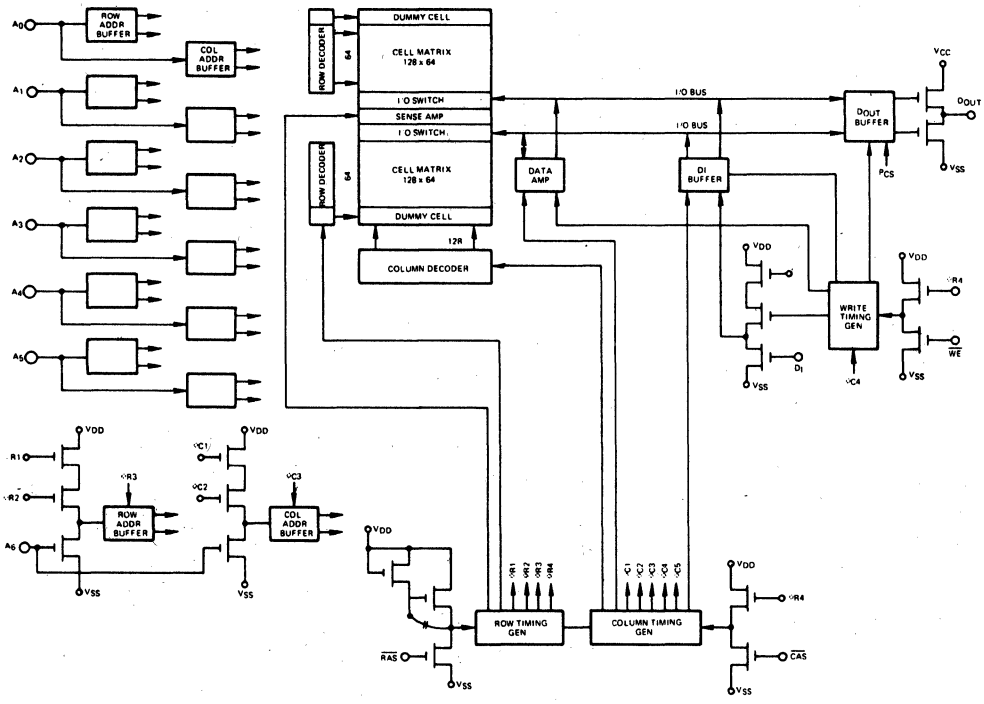


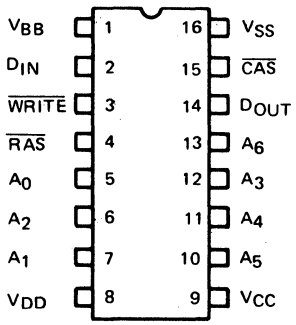


A108

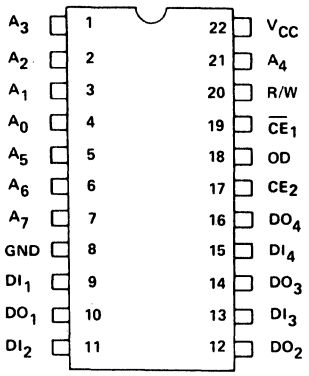


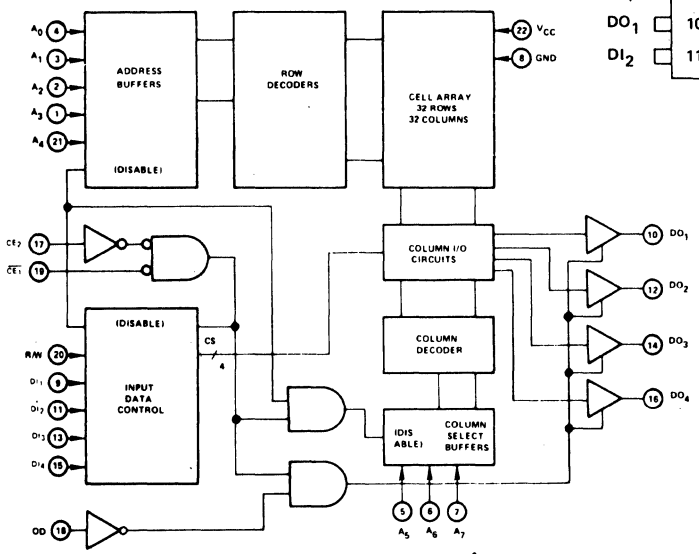
A109



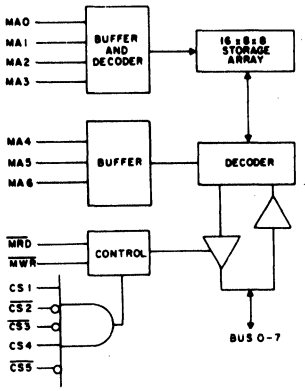


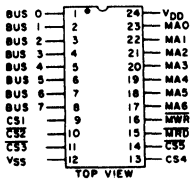
A110



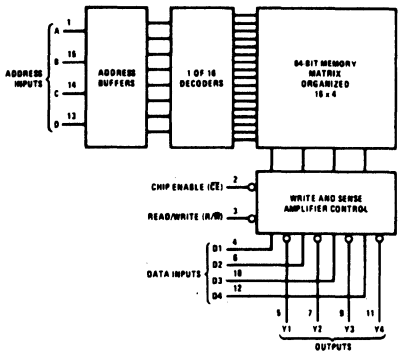


A111

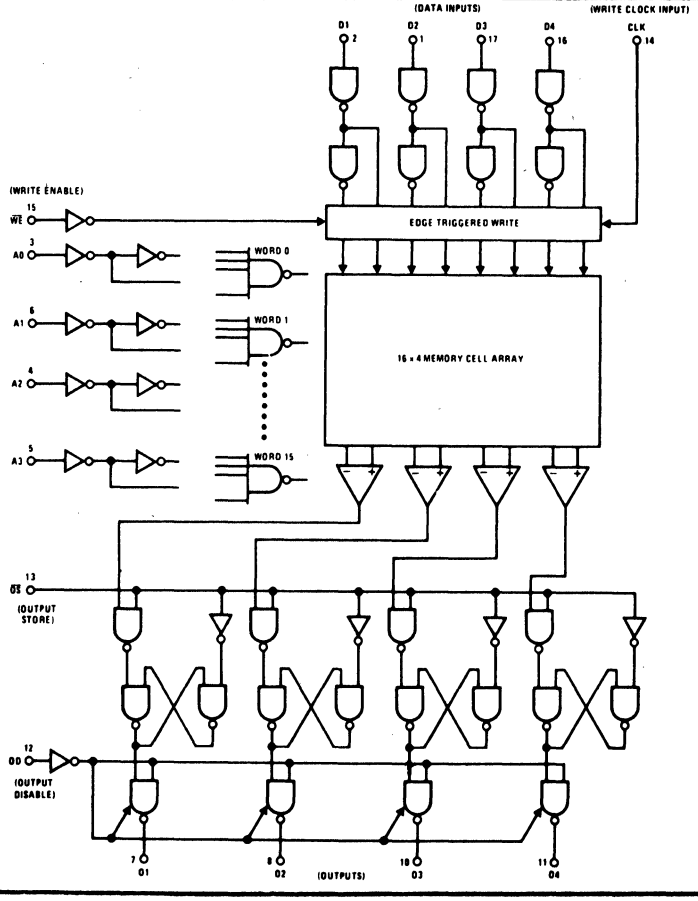




A113



A114

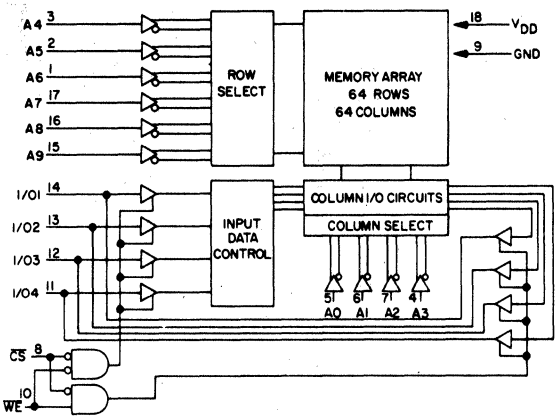


A116

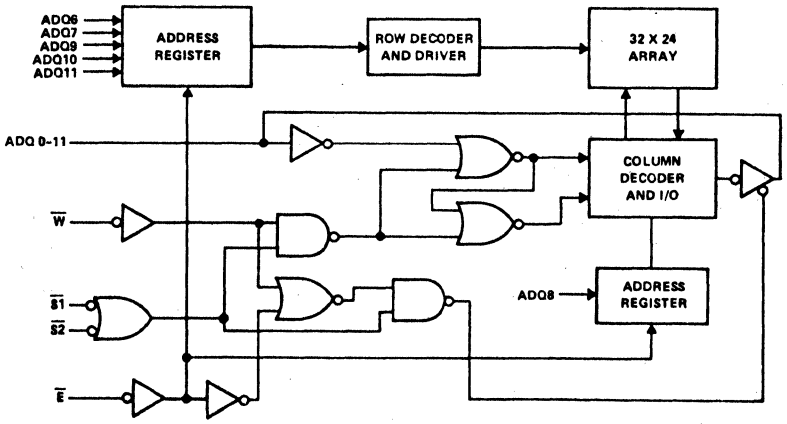
(TOP VIEW)

A7	1	24	VCC
A6	2	23	A8
A5	3	22	A9
A4	4	21	$\overline{W}$
A3	5	20	$\overline{OE}$
A2	6	19	A10
A1	7	18	$\overline{CS}$
A0	8	17	DQ8
DQ1	9	16	DQ7
DQ2	10	15	DQ6
DQ3	11	14	DQ5
VSS	12	13	DQ4

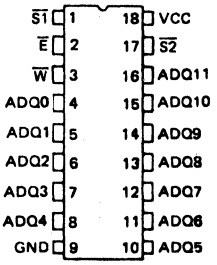
A118



A119

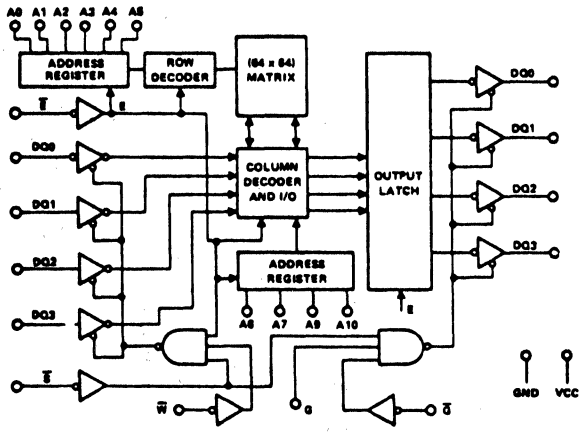


TOP VIEW

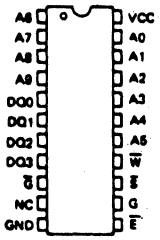


ADQ - Address/Data
$\overline{S}$ - Chip Select
$\overline{E}$ - Chip Enable
$\overline{W}$ - Write Enable

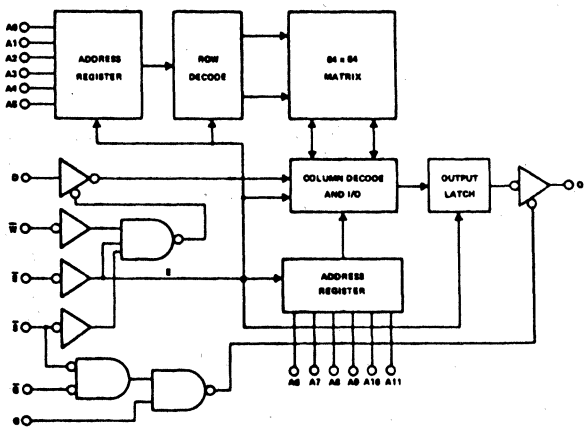
A120



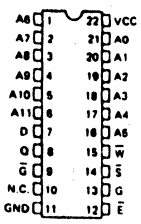
TOP VIEW



A121



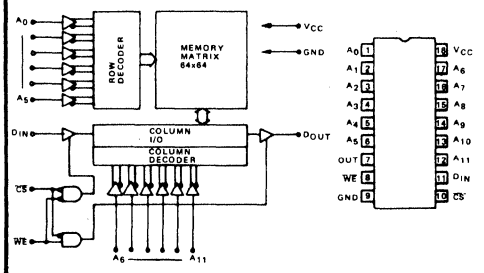
TOP VIEW



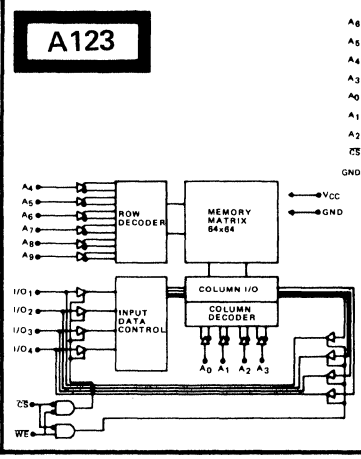
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

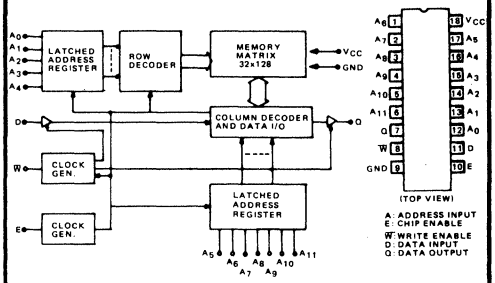
A122



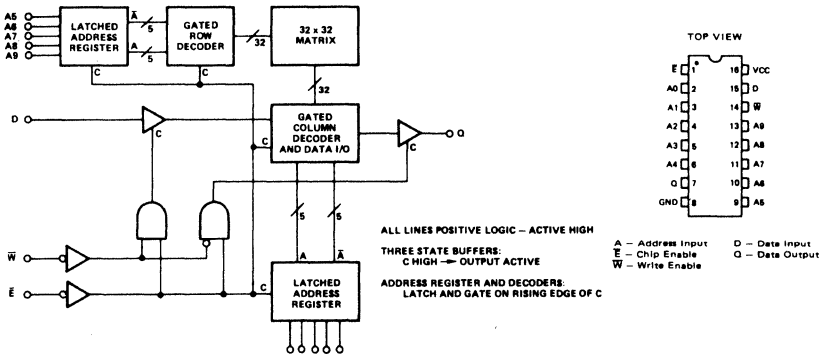
A123



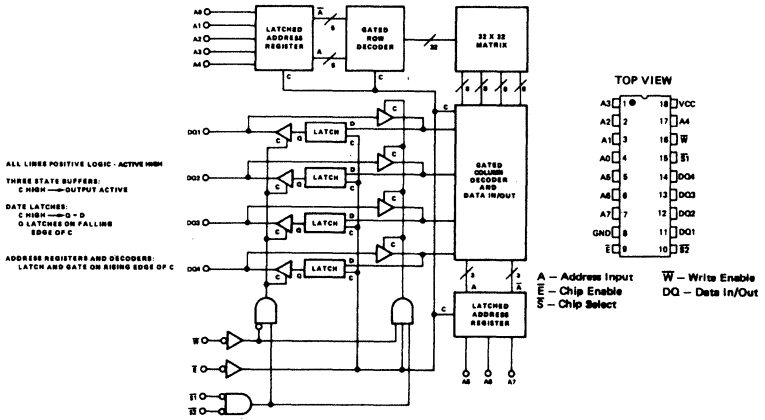
A124



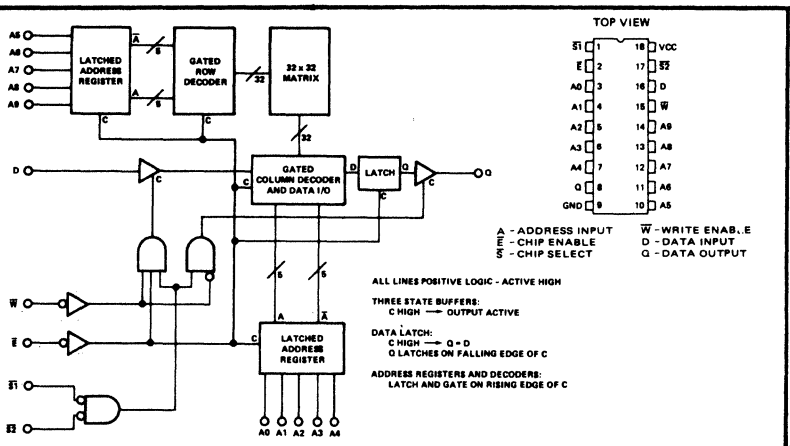
A125



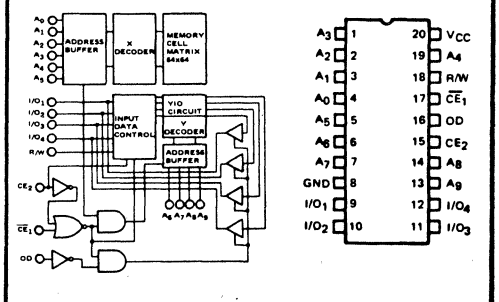
A126



A127



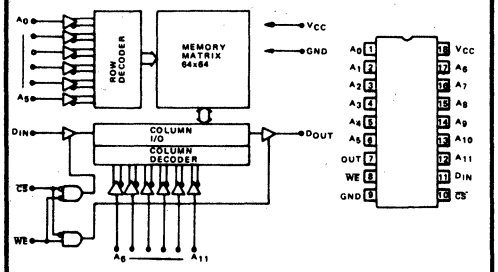
A128



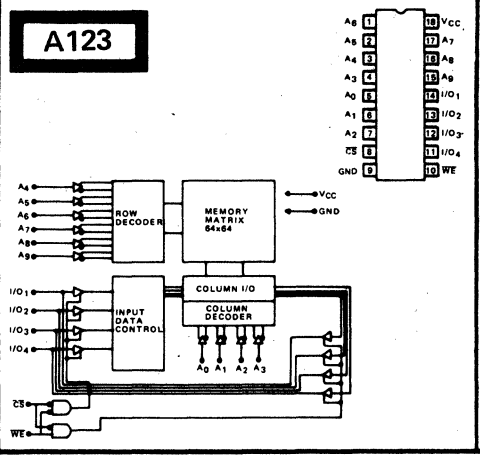
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

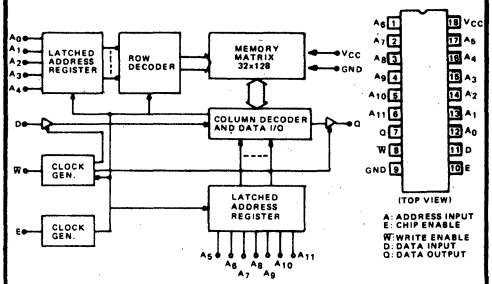
A122



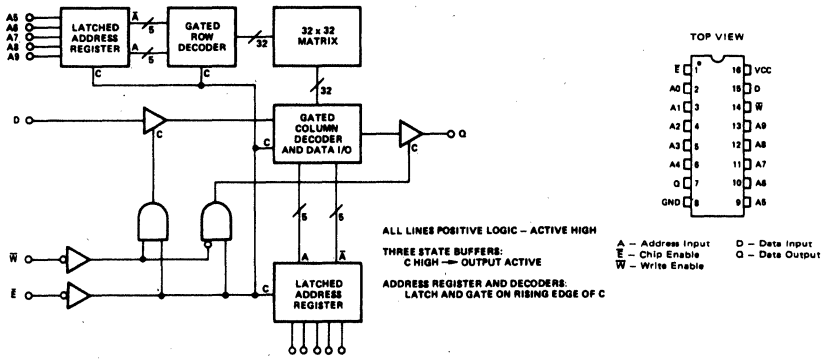
A123



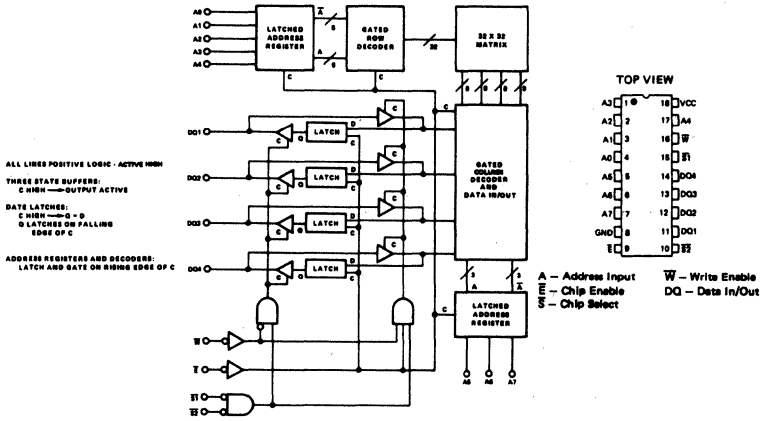
A124



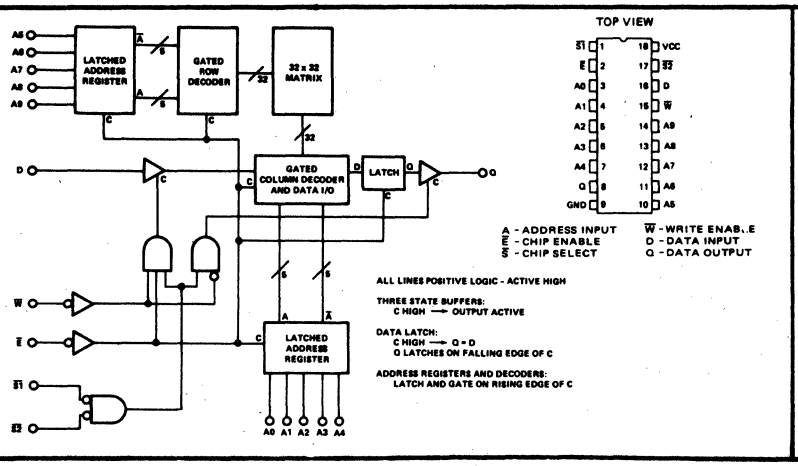
A125



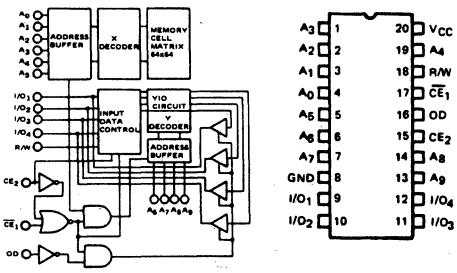
A126



A127



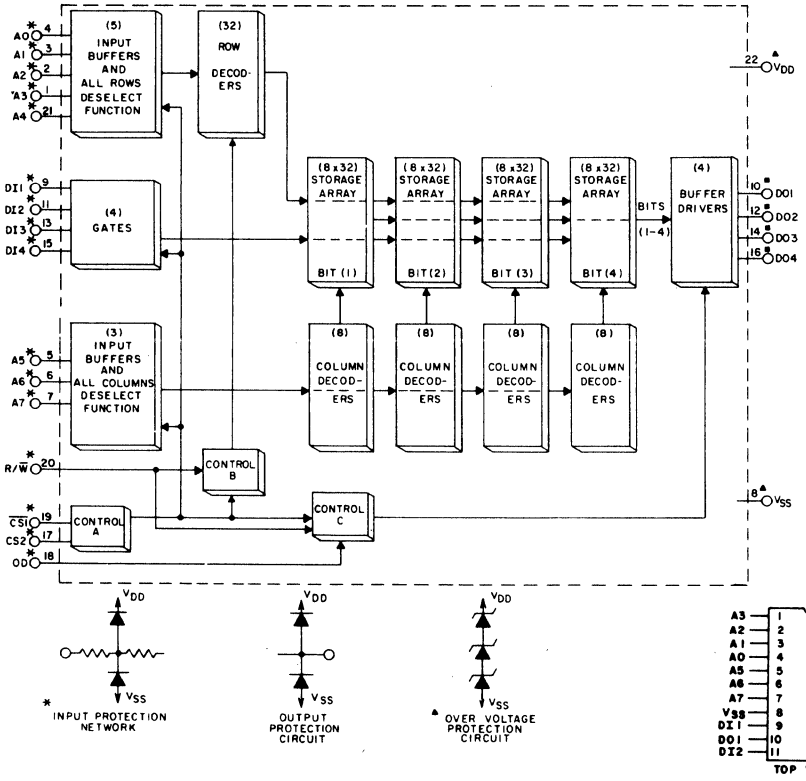
A128



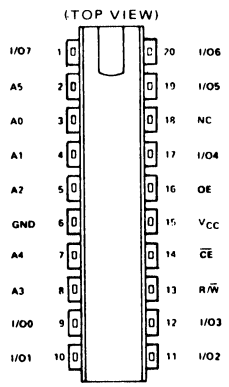
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

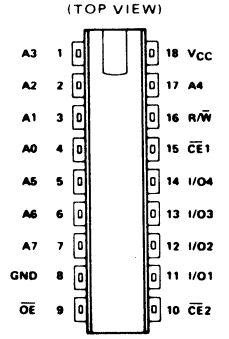
A129



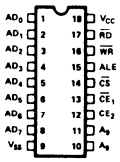
A130

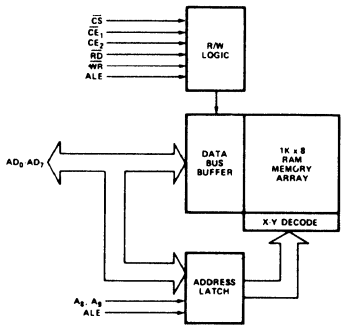


A131



A132

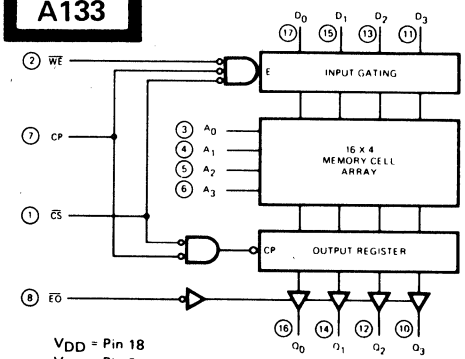




PIN NAMES

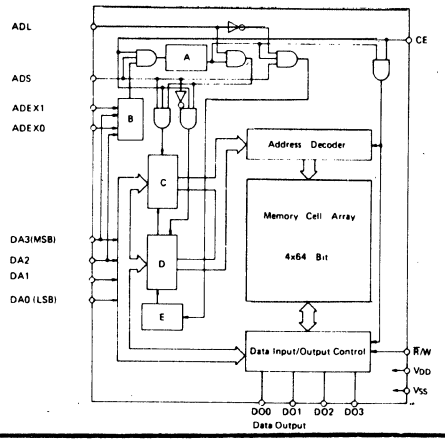
AD_0 AD_7	ADDRESS/DATA LINES
A_8, A_9	ADDRESS LINES
$\overline{CS}$	CHIP SELECT
$\overline{CE}_1$	CHIP ENABLE (IO/$\overline{M}$)
CE_2	CHIP ENABLE
ALE	ADDRESS LATCH ENABLE
$\overline{RD}$	READ ENABLE
$\overline{WR}$	WRITE ENABLE

A133

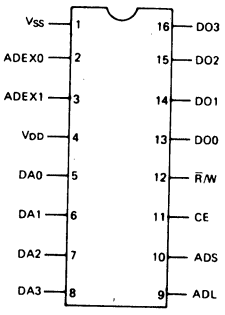


VDD = Pin 18
VSS = Pin 9
○ = Pin Numbers

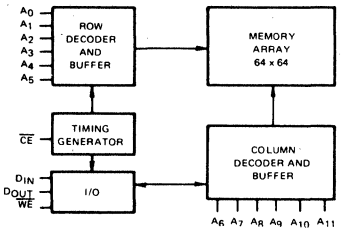
A134

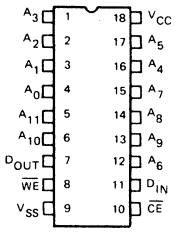


A: Internal chip select
B: Coincidence circuit
C: Address latch group 2 (most significant 2 bits)
D: Address latch group 1 (least significant 4 bits)
E: Address + 1

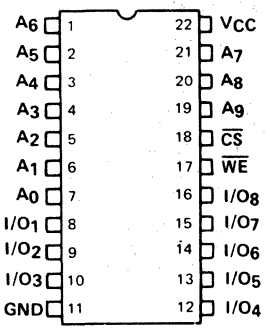


A135

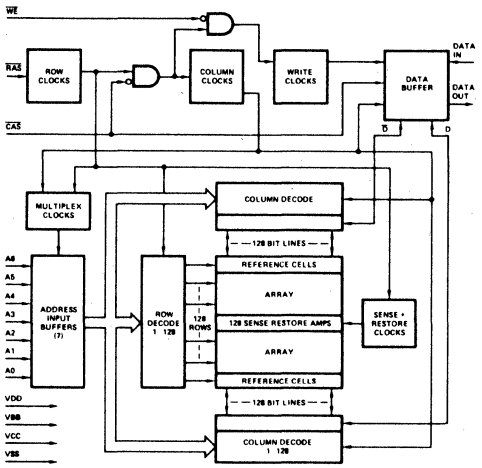


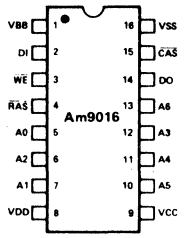


A136



A137



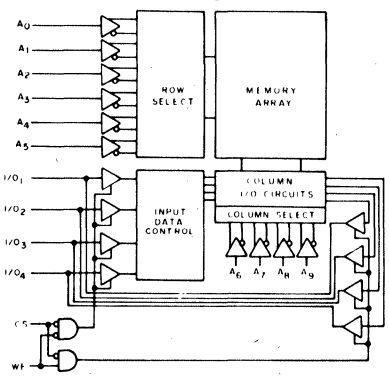


Top View
Pin 1 is marked for orientation.

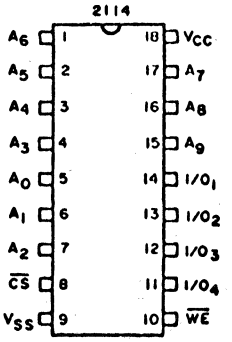
A0 – A6	ADDRESS INPUTS
CAS	COLUMN ADDRESS STROBE
DI	DATA IN
DO	DATA OUT
RAS	ROW ADDRESS STROBE
VDD	POWER (+12V)
VCC	POWER (+5V)
VSS	GROUND
VBB	POWER (–5V)
WE	WRITE ENABLE

A138

BLOCK DIAGRAM



PIN CONFIGURATION

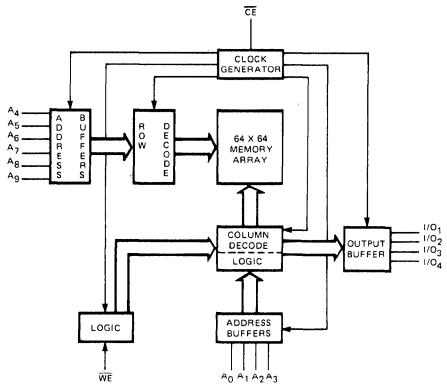


19. LOGIC/BLOCK DRAWINGS

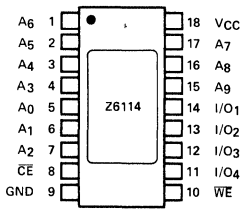
IN DRAWING NUMBER SEQUENCE

A139

Functional Block Diagram

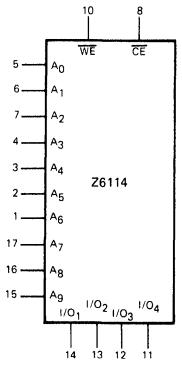


Pin Configuration



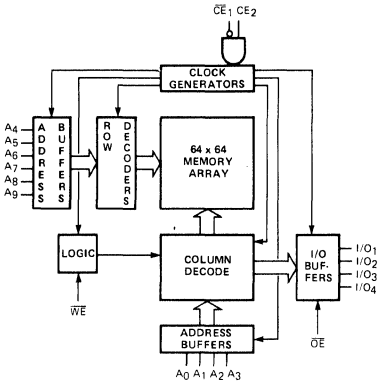
A_0–A_{11}	ADDRESS INPUTS
$\overline{CE}$	CHIP ENABLE
V_{SS}	GROUND
V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE
I/O_1–I/O_4	DATA INPUT/OUTPUTS

Logic Symbol

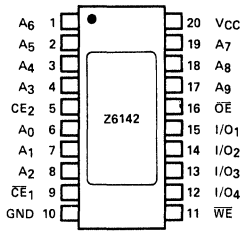


A140

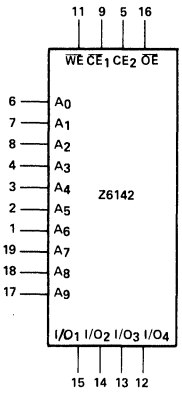
Functional Block Diagram



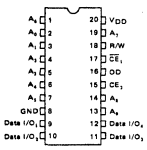
Pin Configuration



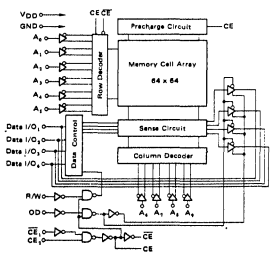
Logic Symbol



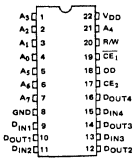
A141

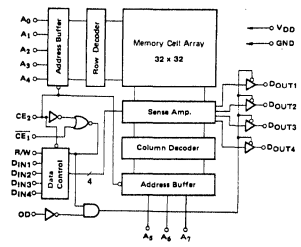


BLOCK DIAGRAM

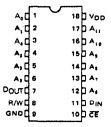


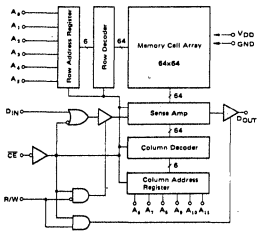
A142



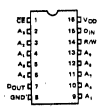


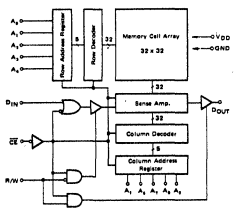
A143



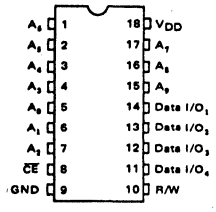


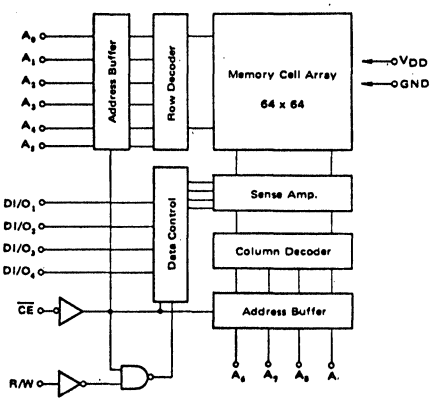
A144



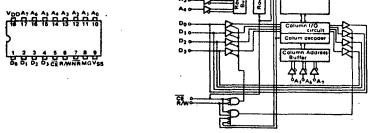


A145

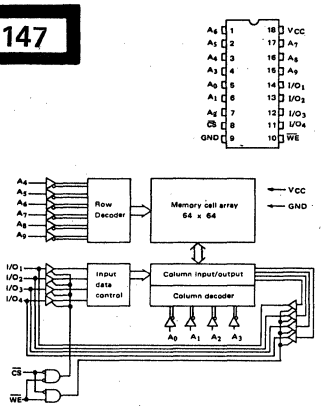




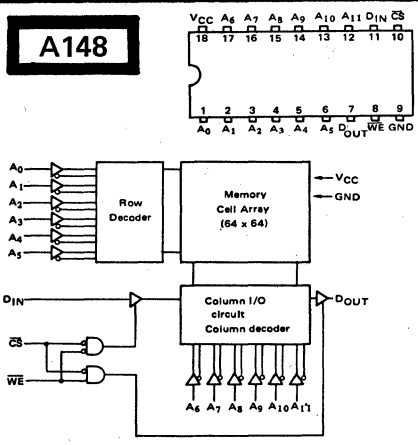
A146



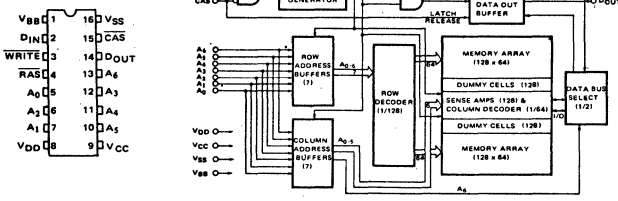
A147



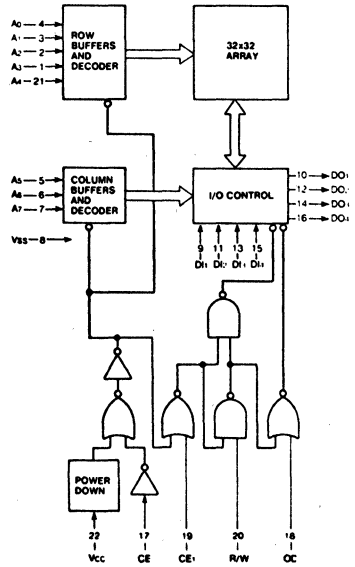
A148

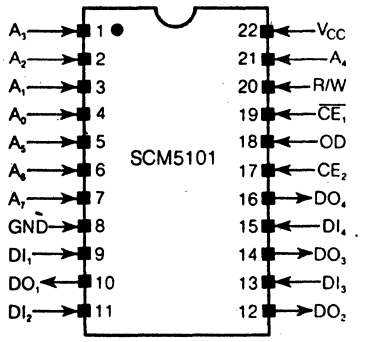


A149

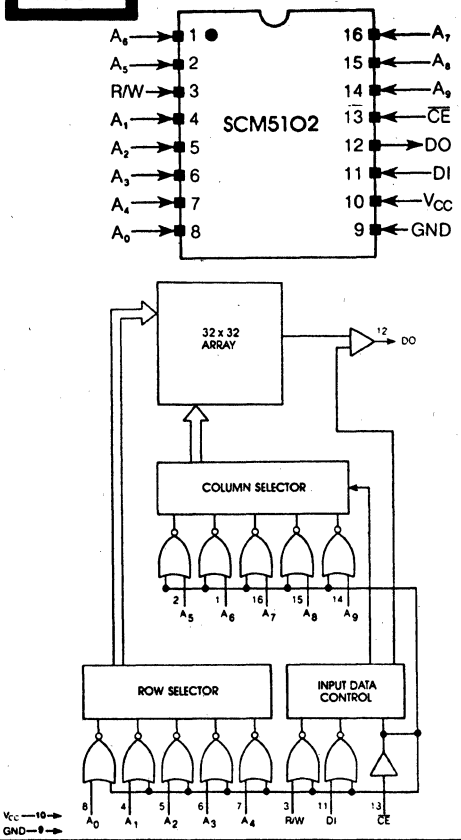


A150

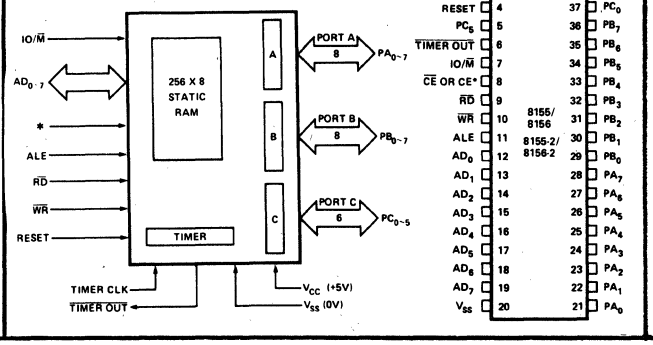




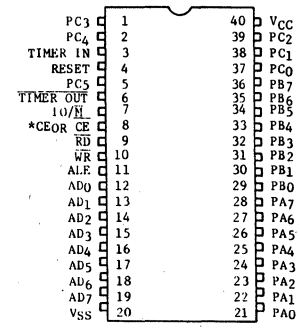
A151



A152



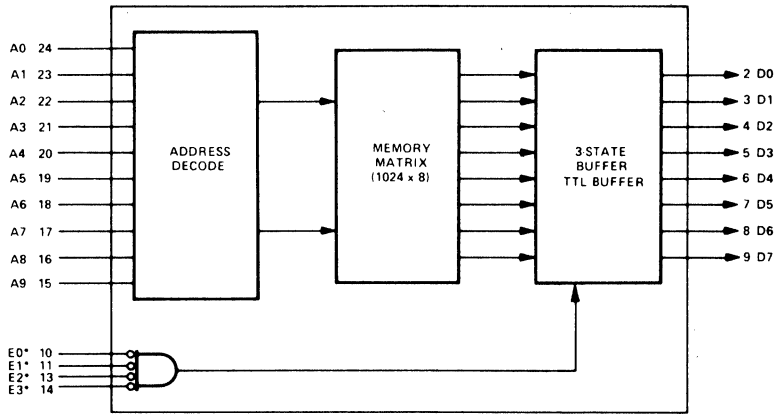
A153



19. LOGIC/BLOCK DRAWINGS

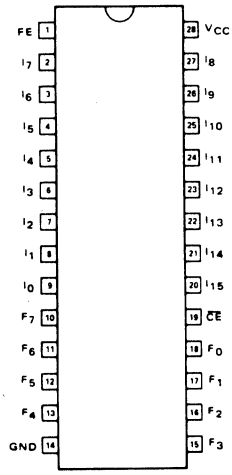
IN DRAWING NUMBER SEQUENCE

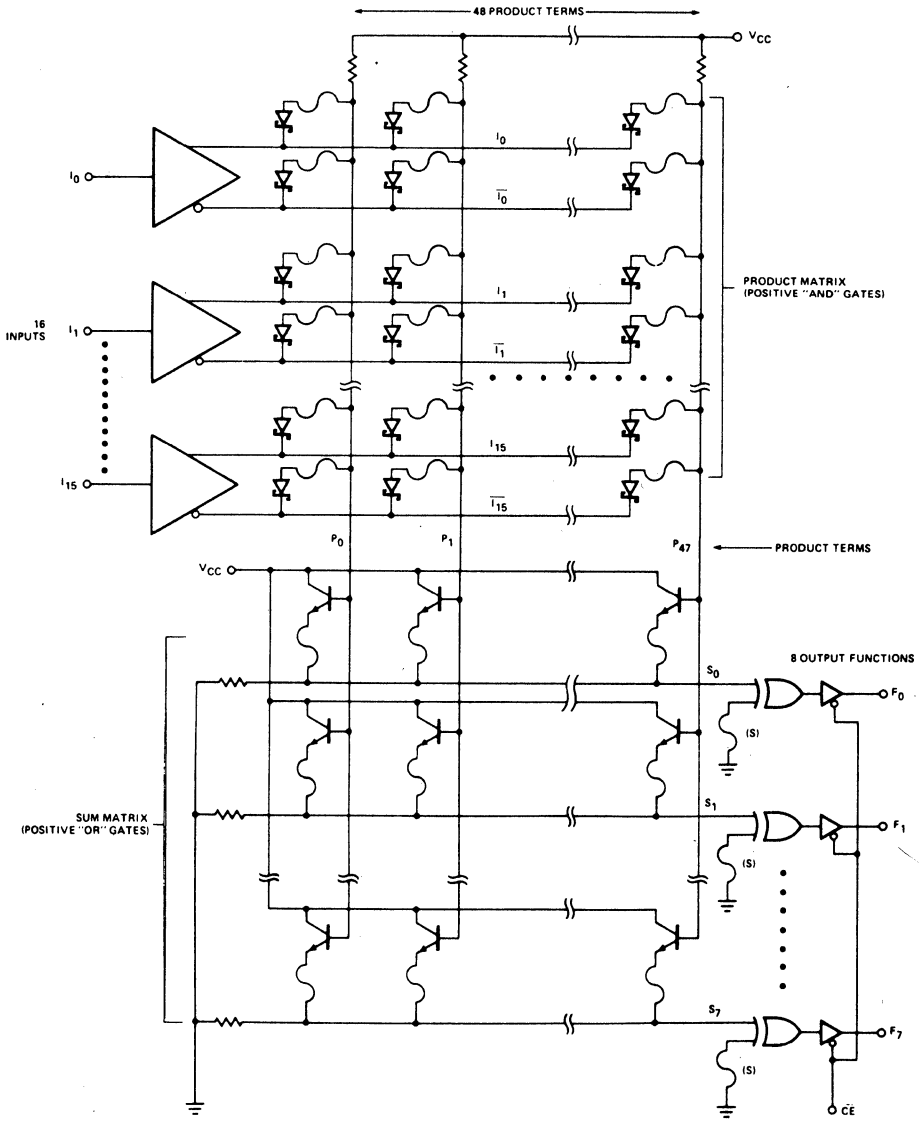
B1



*Active level defined by the customer.

B2

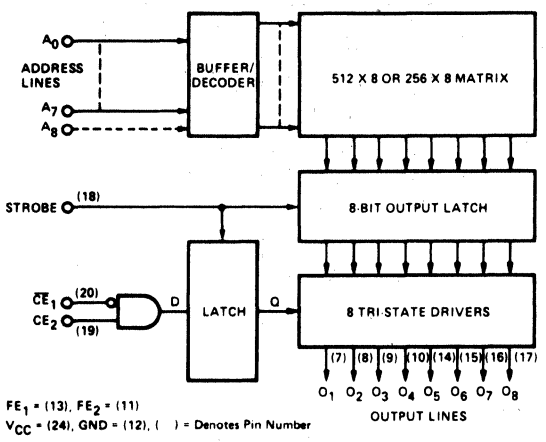


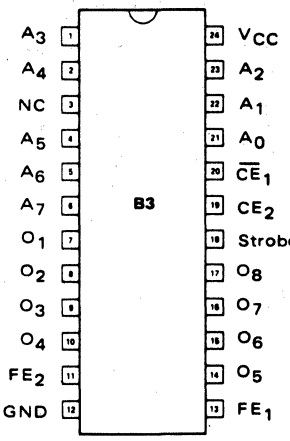


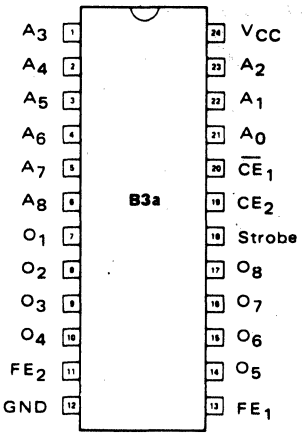
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

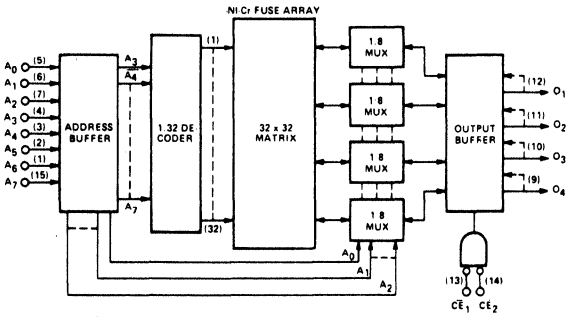
B3



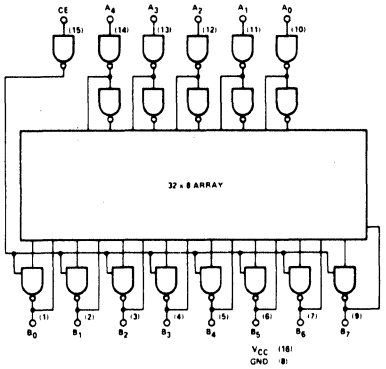




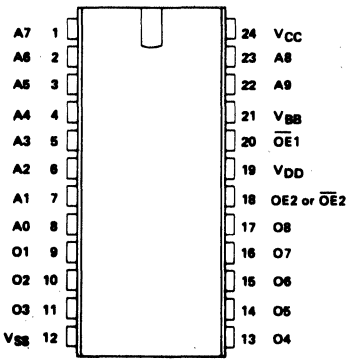
B4

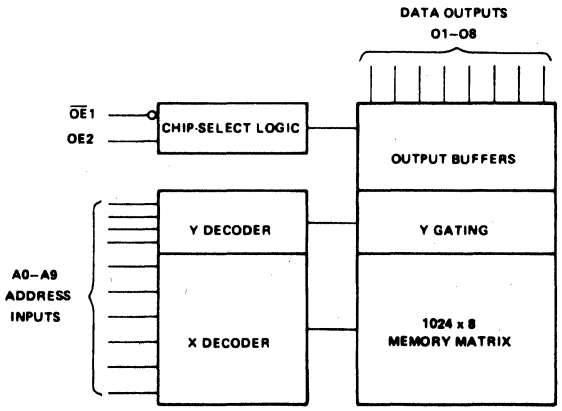


B5

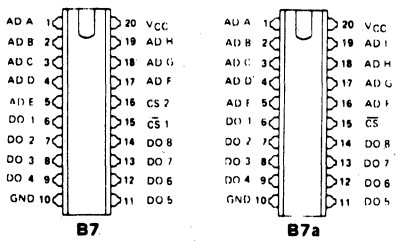


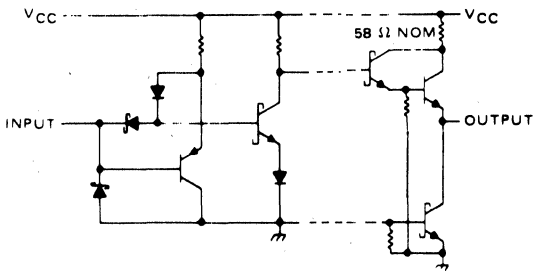
B6





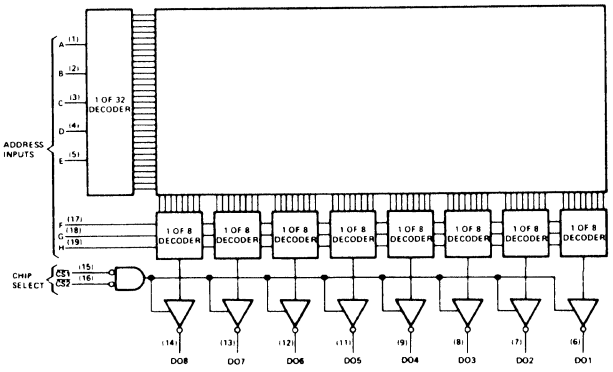
B7



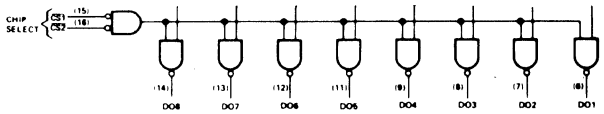


B8

B8

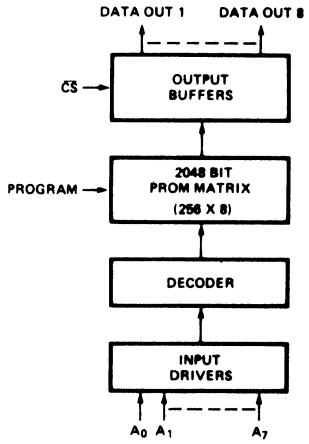


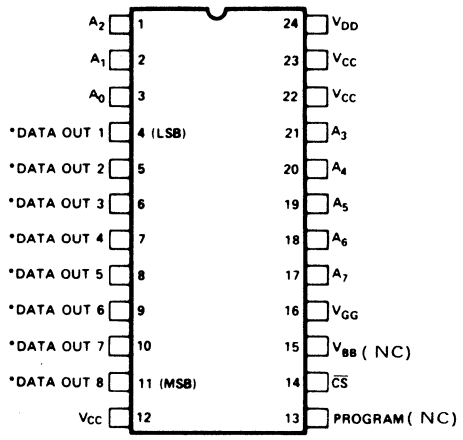
B8a—OUTPUTS ARE AS SHOWN BELOW



B13

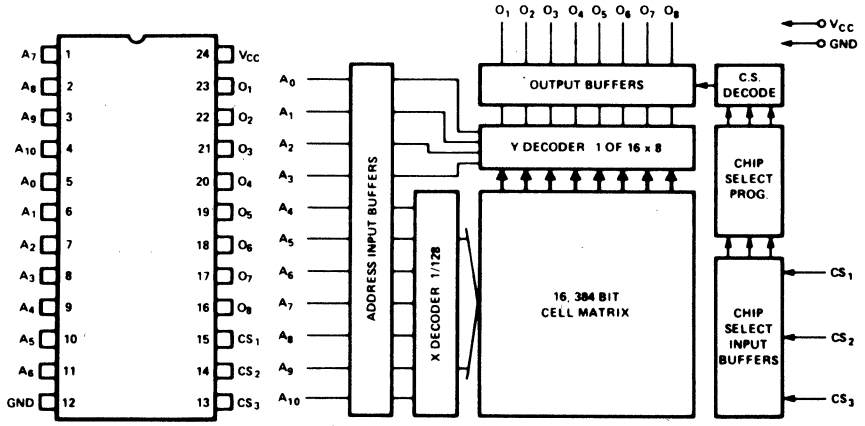
BLOCK DIAGRAM



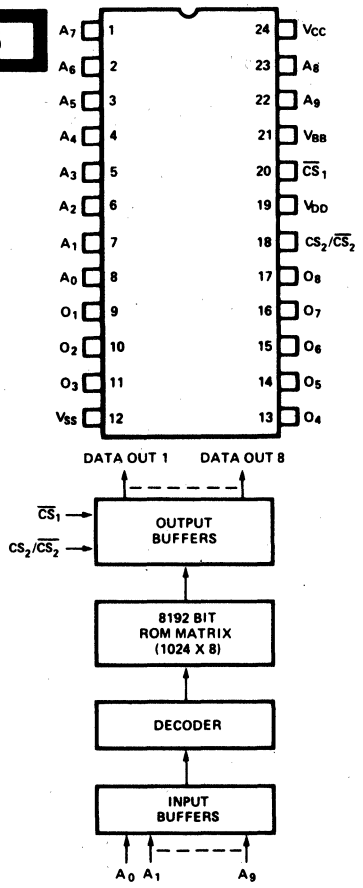


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING.
PINS 13,15
NC FOR B13a

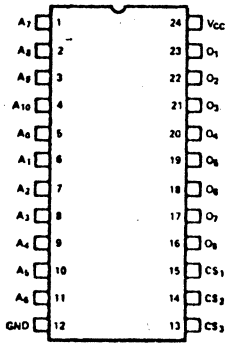
B14



B15

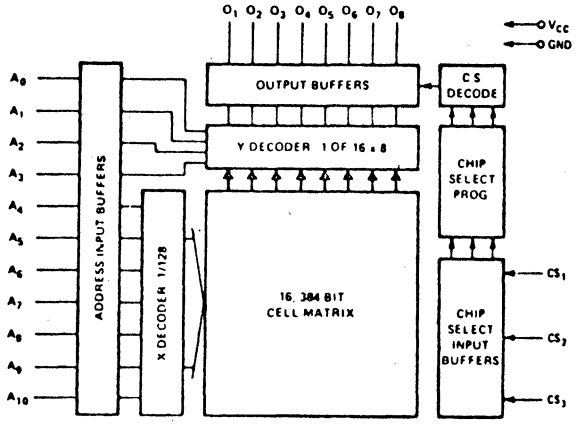


B16

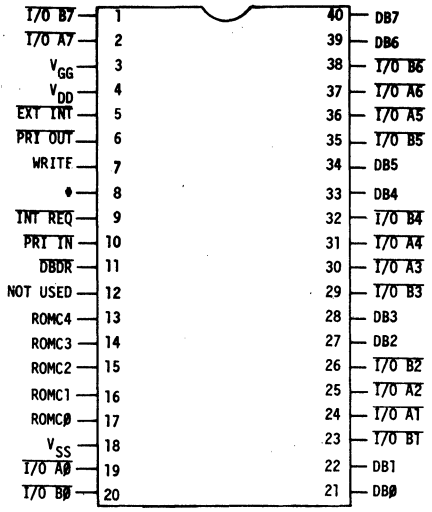


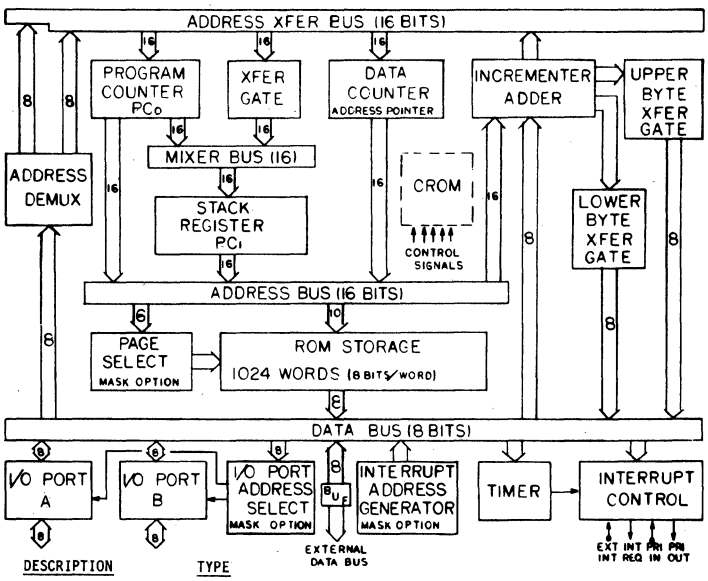
PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
CS_1-CS_3	PROGRAMMABLE CHIP SELECT INPUTS



B17



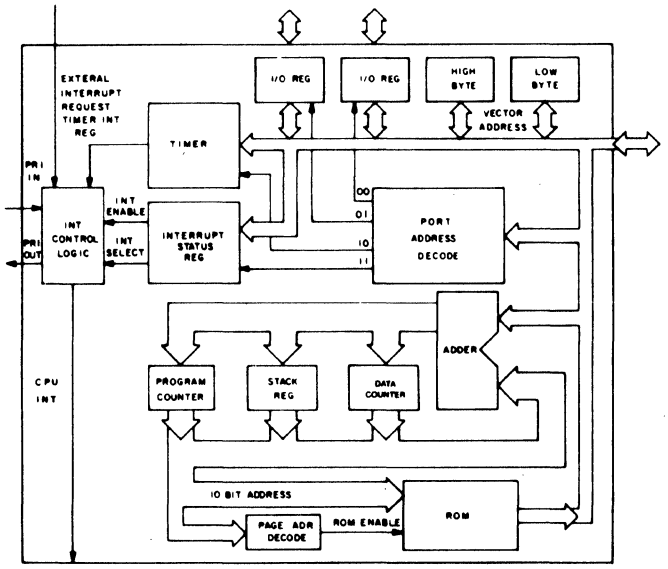


PIN NAME	DESCRIPTION	TYPE
I/O AØ - I/O A7	I/O Port A	Bidirectional
I/O BØ - I/O B7	I/O Port B	Bidirectional
DBØ - DB7	Data Bus	Input
ROMCØ - ROMC4	Control Lines	Input
Φ, WRITE	Clock Lines	Input
EXT INT	External Interrupt	Input
PRI IN	Priority In	Input
PRI OUT	Priority Out	Output
INT REQ	Interrupt Request	Output
DBDR	Data Bus Drive	Output
V_{SS}, V_{DD}, V_{GG}	Power Supply Lines	Input

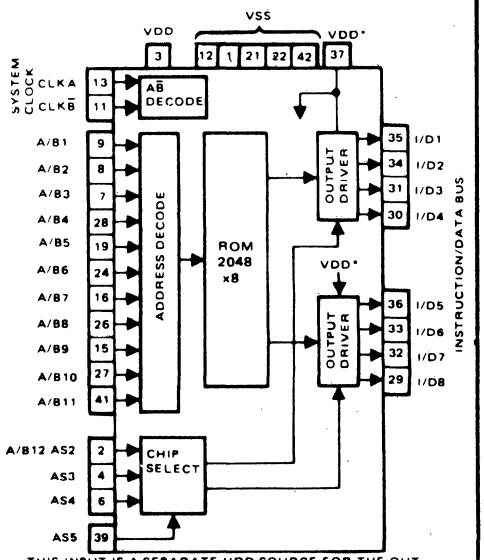
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

B18



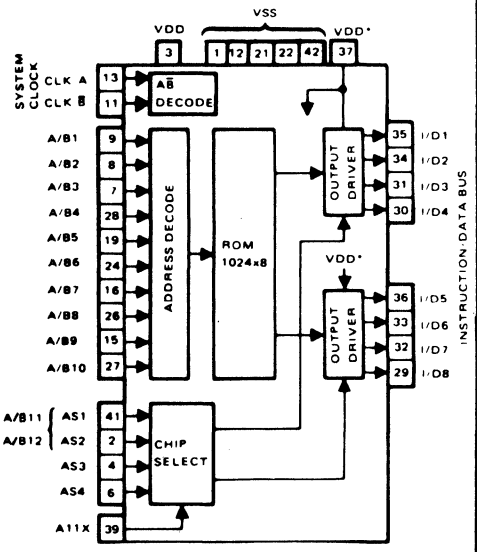
B19



THIS INPUT IS A SEPARATE VDD SOURCE FOR THE OUT-PUT DRIVERS. THIS IS USEFUL FOR ISOLATING INDIVIDUAL CIRCUITS DURING DEVICE TESTING AND FAULT ISOLATION WHEN MULTIPLE CIRCUITS ARE CONNECTED TO THE DATA BUS.

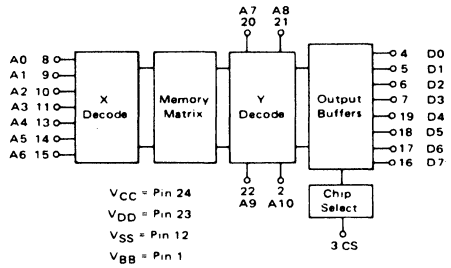
THE AS5 INPUT IS DISABLED BY MASK OPERATION FOR PPS-4 APPLICATIONS. ALSO, THE OPTION OF CREATING, BY MASK OPERATION, A 4096 x 4-BIT ORGANIZATION IS NOT AVAILABLE FOR THE A52--ROM.

B20



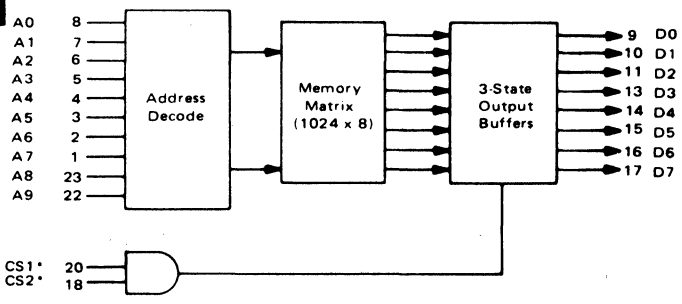
THIS INPUT IS A SEPARATE VDD SOURCE FOR THE OUT PUT DRIVERS. THIS IS USEFUL FOR ISOLATING INDIVIDUAL CIRCUITS DURING DEVICE TESTING AND FAULT ISOLATION WHEN MULTIPLE CIRCUITS ARE CONNECTED TO THE DATA BUS.

B23



V_{CC} = Pin 24
V_{DD} = Pin 23
V_{SS} = Pin 12
V_{BB} = Pin 1

B24



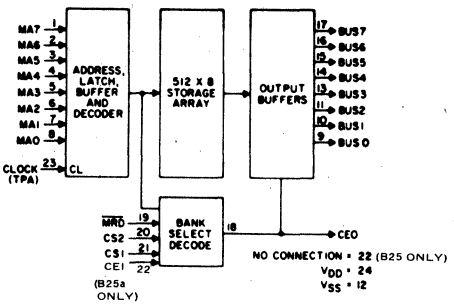
*Active level defined by the customer.

V_{CC} = Pin 24
Gnd = Pin 12

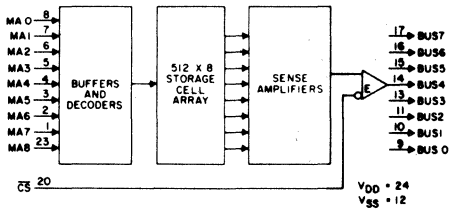
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

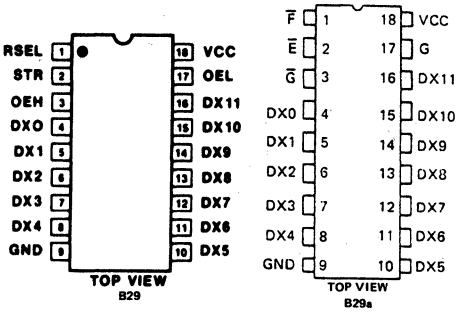
B25



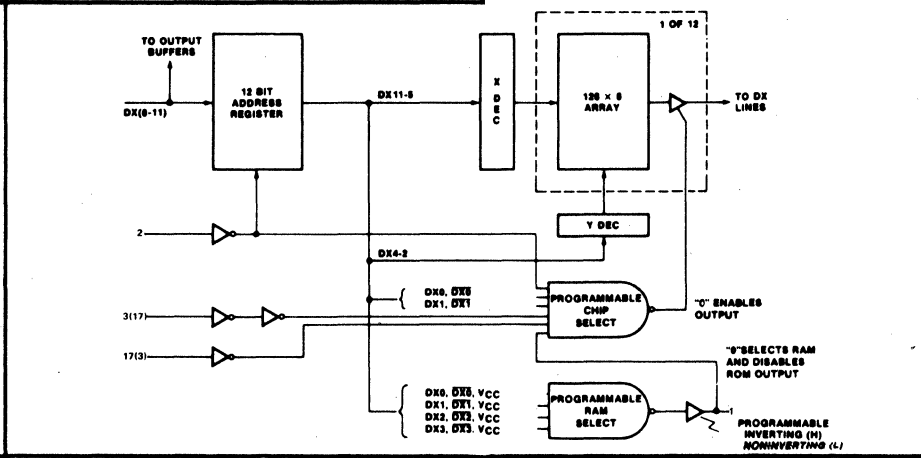
B26



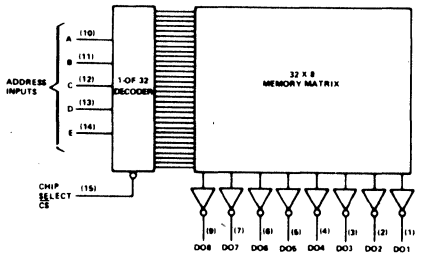
B29



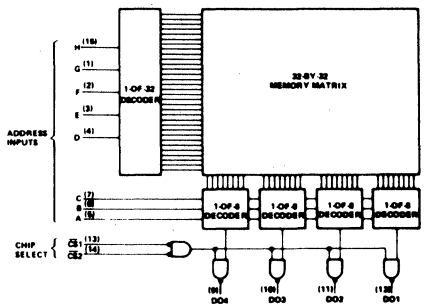
B27



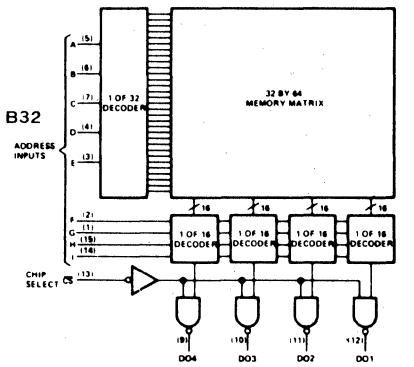
B30



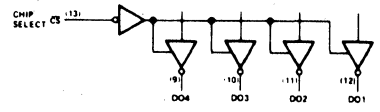
B31



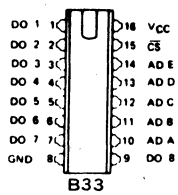
B32

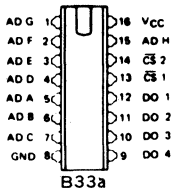


B32a—OUTPUTS ARE AS SHOWN BELOW



B33

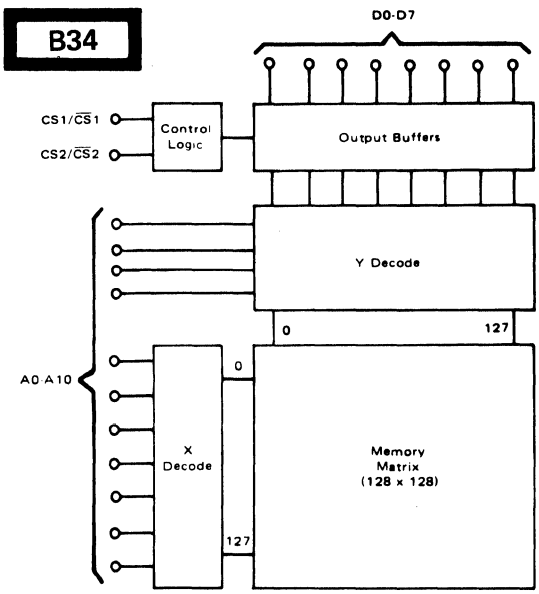


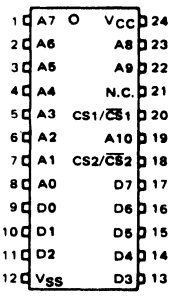


19. LOGIC/BLOCK DRAWINGS

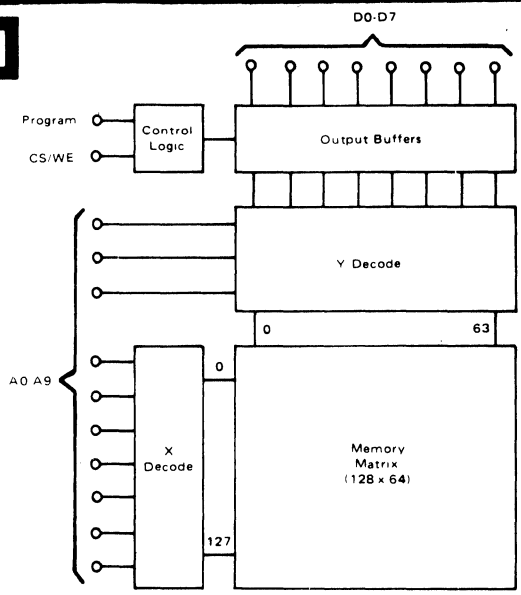
IN DRAWING NUMBER SEQUENCE

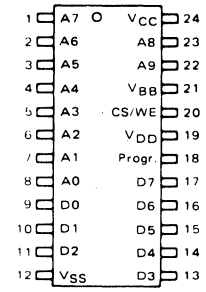
B34



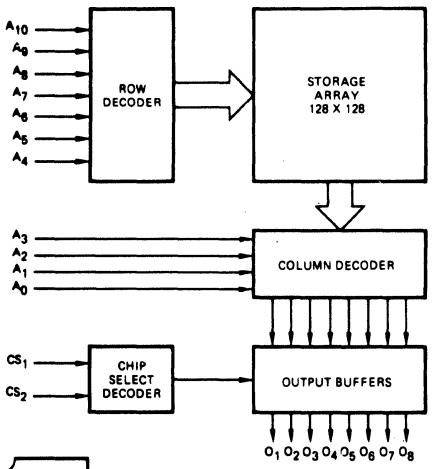


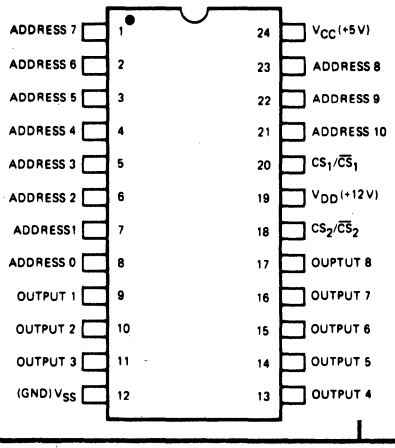
B35



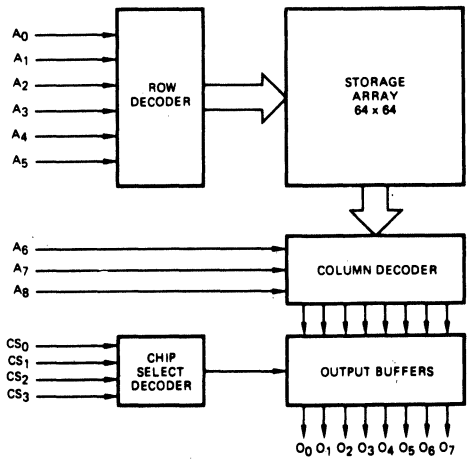


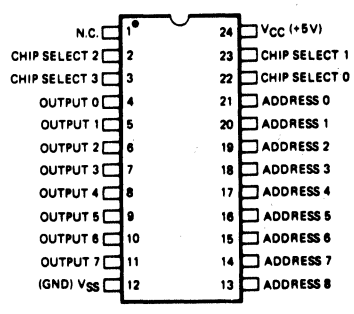
B36



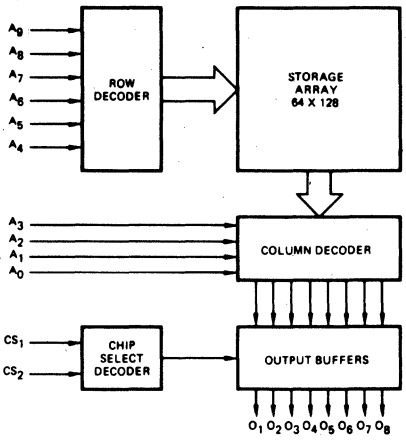


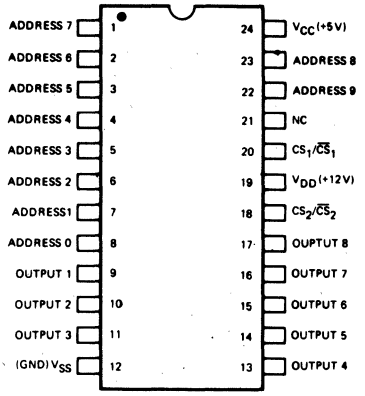
B37



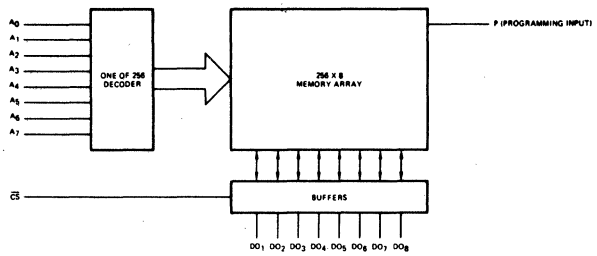


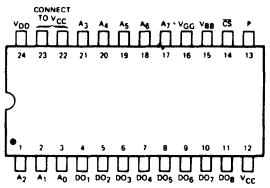
B38



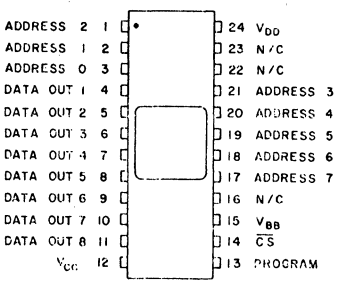


B39



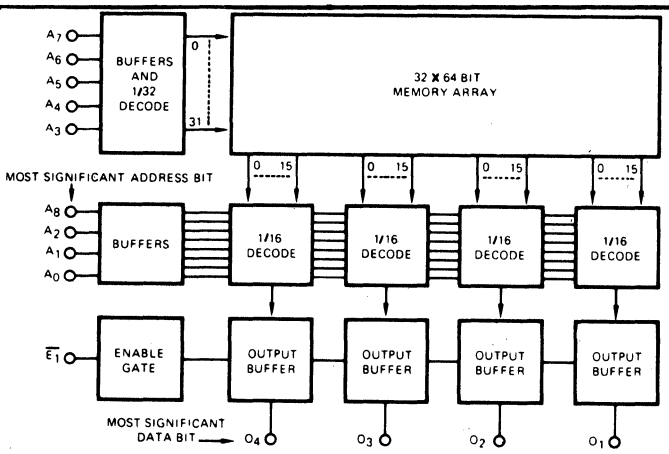


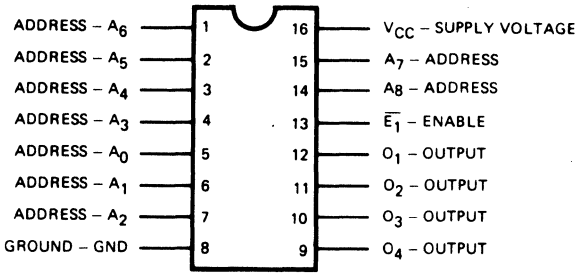
B39



B39a

B40

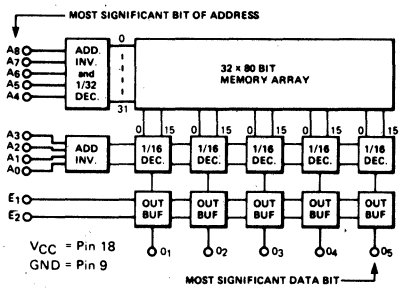


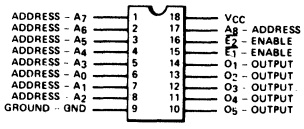


To enable the device, $\overline{E_1}$ must be low.

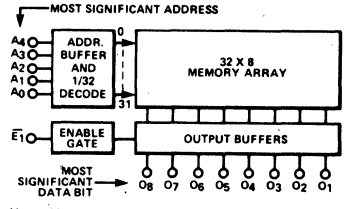
B40a—PIN13=$\overline{E_1}$—ENABLE AND PROGRAM PIN.

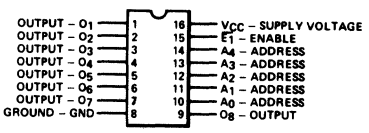
B41





B42

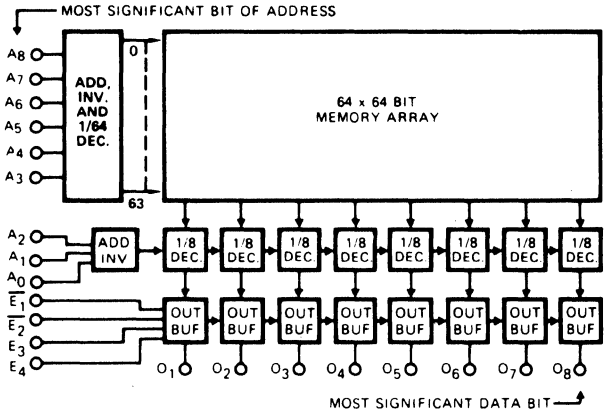




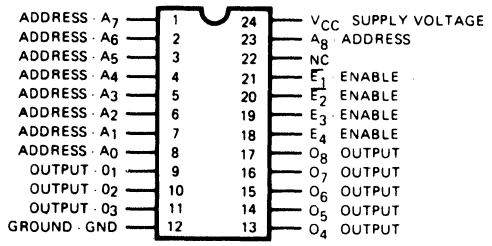
VCC = 16
GND = 8

To enable the device, $\overline{E_1}$ must be LOW.

B43

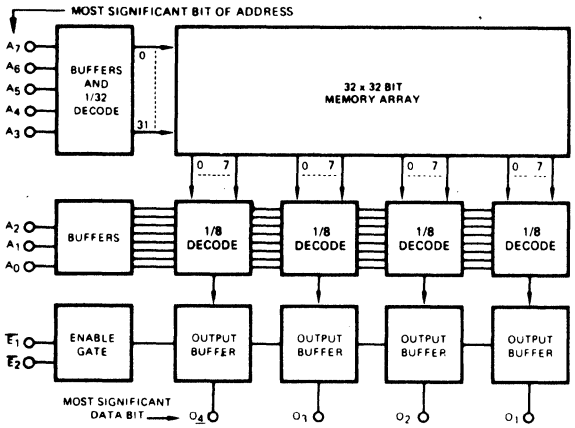


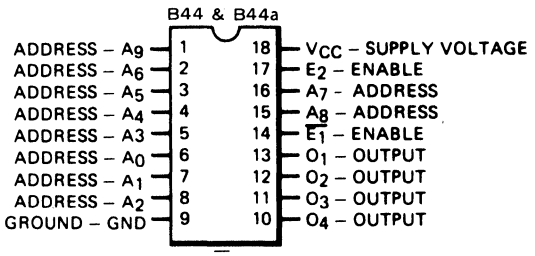
V_{CC} = 24
GND = 12



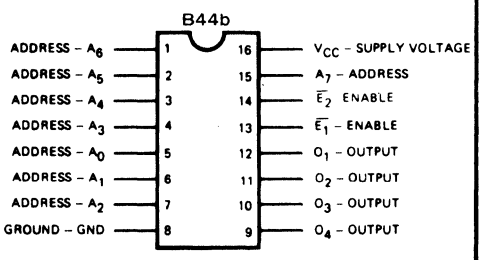
To enable the device, $\overline{E_1}$ and $\overline{E_2}$ must be LOW AND E_3 and E_4 must be HIGH.

B44

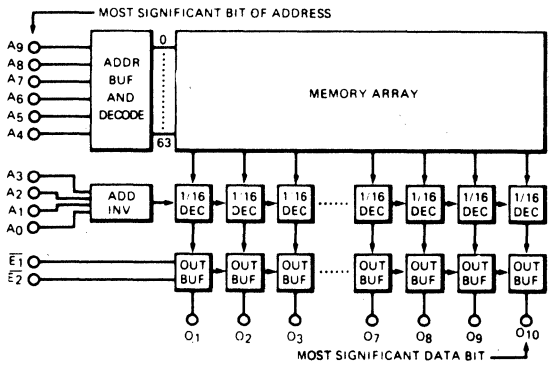


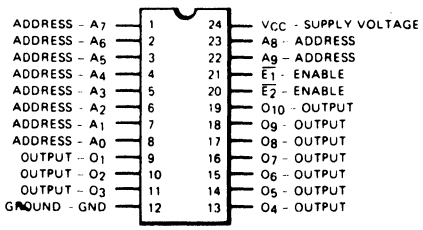


B44a—PIN 14=$\overline{E_1}$—ENABLE AND PROGRAM PIN.

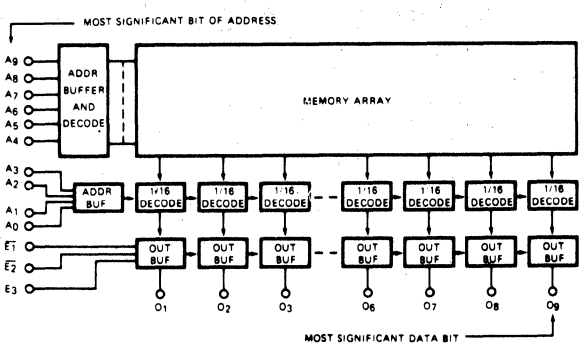


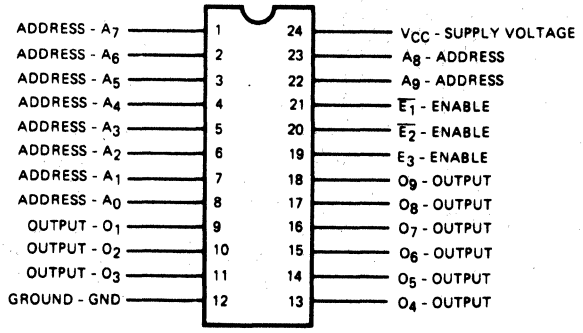
B45



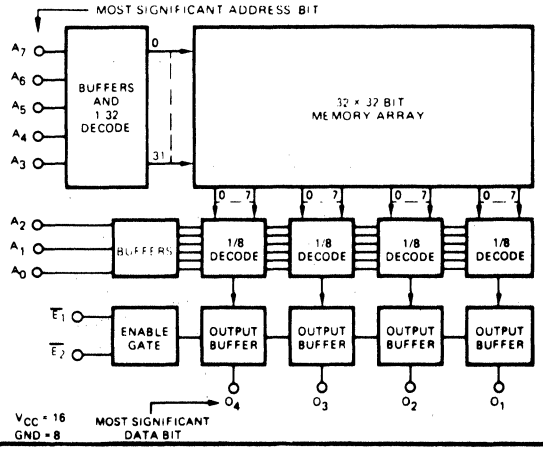


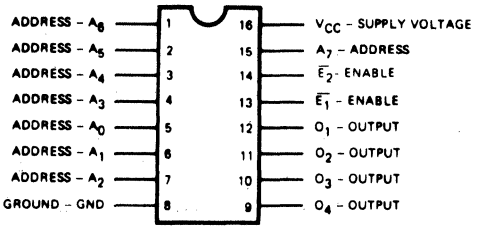
B46





B47

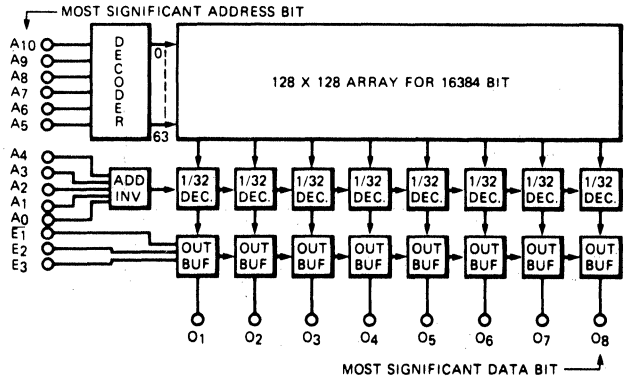


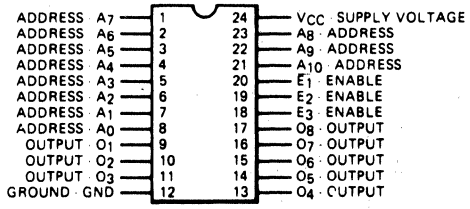


To enable the device, $\overline{E_1}$ and $\overline{E_2}$ must be low.

B47a — PIN 13 = $\overline{E}_1$ — ENABLE AND PROGRAM PIN

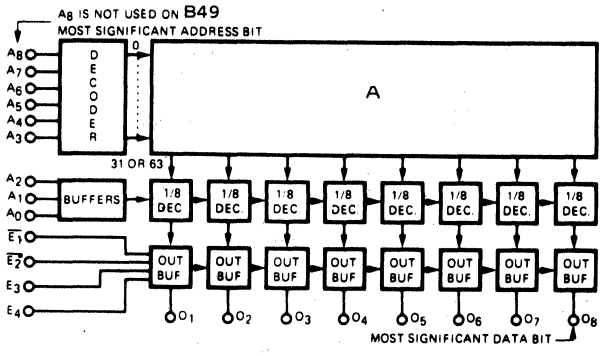
B48

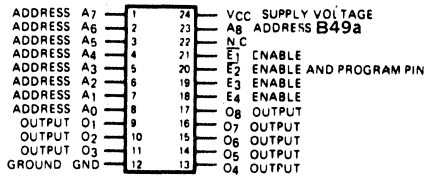




Note:
The Chip is Enabled when $\overline{E_1}$ is Low and E_2 and E_3 are High.

B49





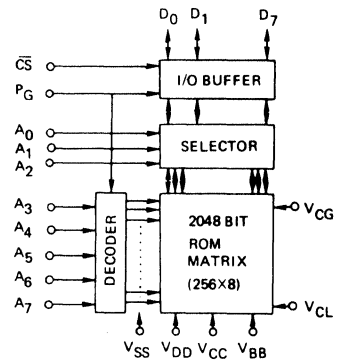
B49— 1. A—32x64 ARRAY
2. A_8 IS NOT CONNECTED

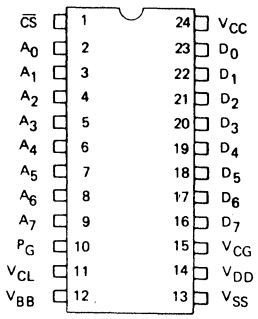
B49a— 1. A—64x64 ARRAY
2. A_8—ADDRESS

19. LOGIC/BLOCK DRAWINGS

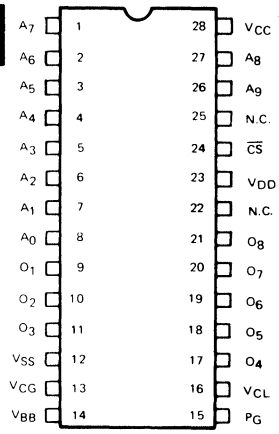
IN DRAWING NUMBER SEQUENCE

B53

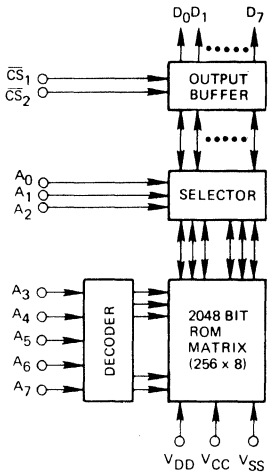


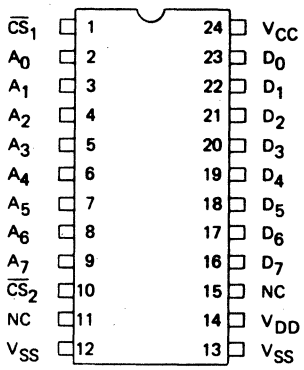


B54

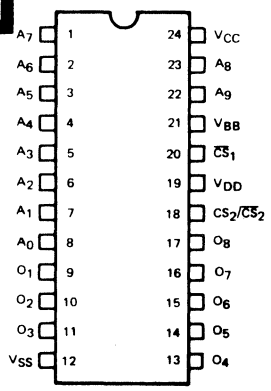


B55

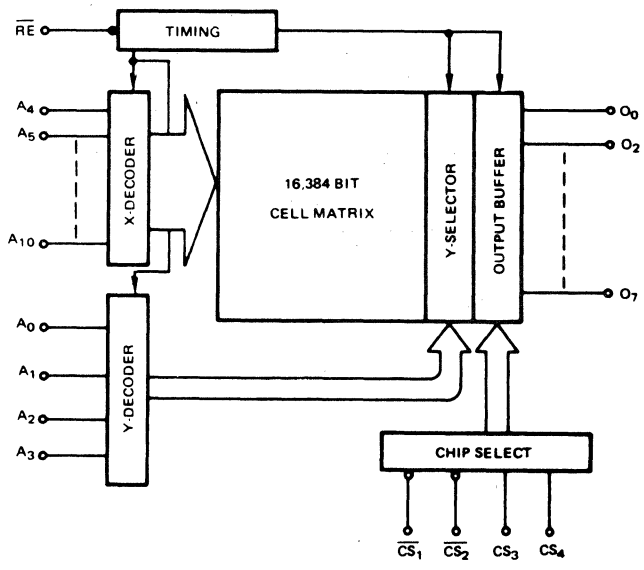


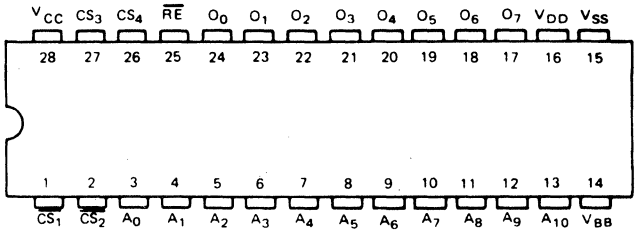


B56

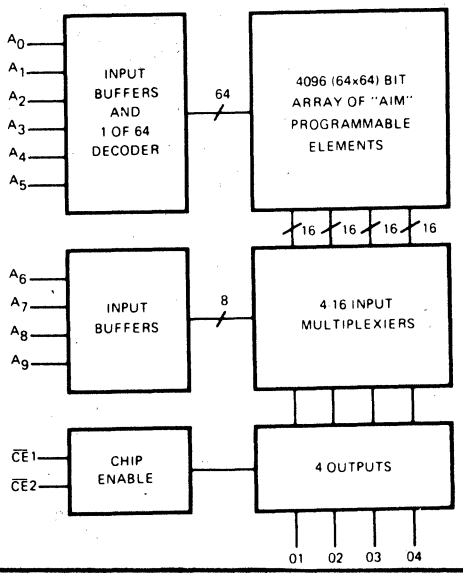


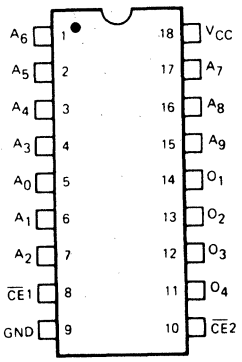
B57



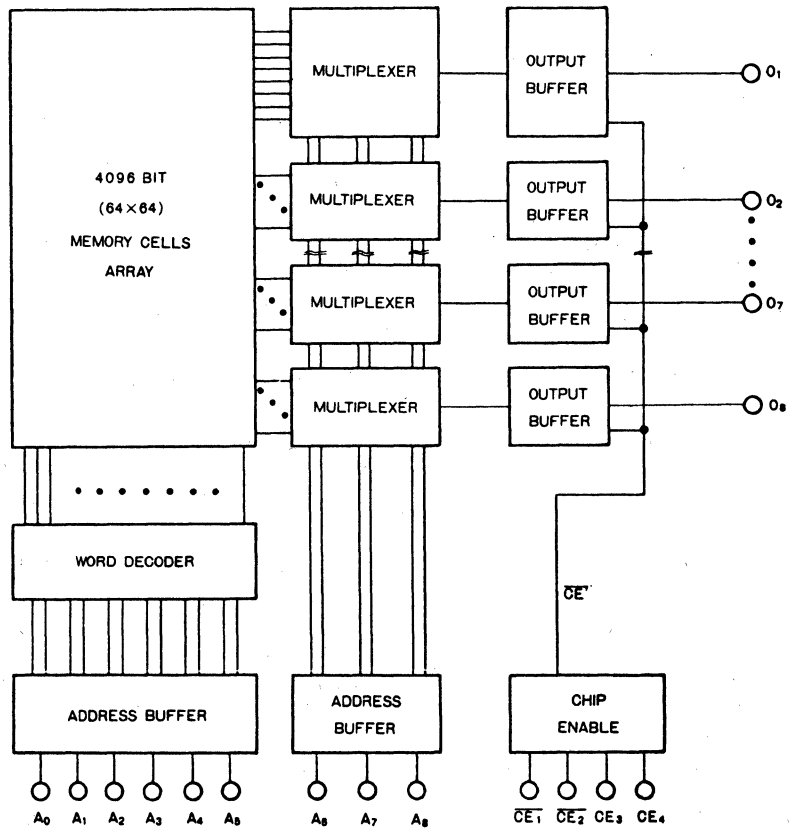


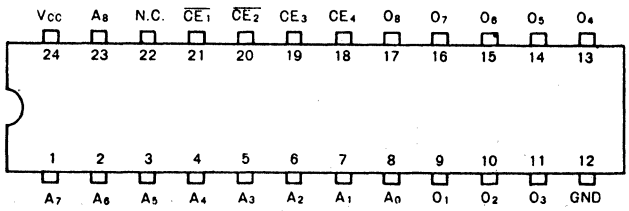
B58


A0
A1
A2
A3
A4
A5
INPUT BUFFERS AND 1 OF 64 DECODER
64
4096 (64x64) BIT ARRAY OF "AIM" PROGRAMMABLE ELEMENTS
16 16 16 16
A6
A7
A8
A9
INPUT BUFFERS
8
4 16 INPUT MULTIPLEXIERS
CE1
CE2
CHIP ENABLE
4 OUTPUTS
O1 O2 O3 O4

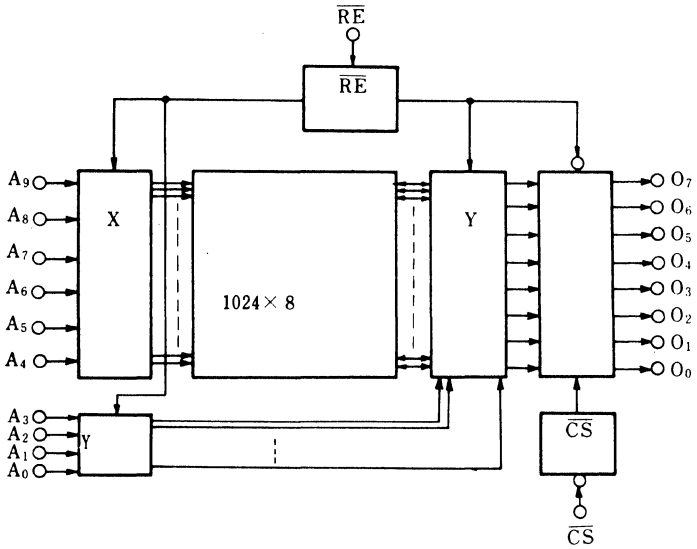

A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CE1 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 O1
13 O2
12 O3
11 O4
10 CE2

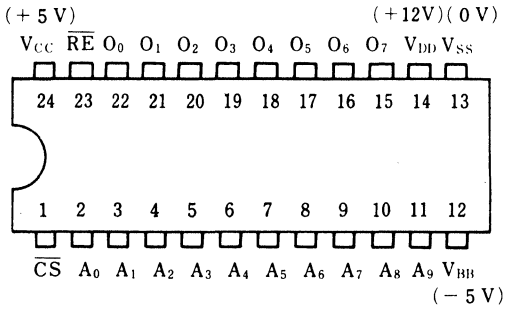
B59


4096 BIT (64×64) MEMORY CELLS ARRAY
MULTIPLEXER
MULTIPLEXER
MULTIPLEXER
MULTIPLEXER
OUTPUT BUFFER
OUTPUT BUFFER
OUTPUT BUFFER
OUTPUT BUFFER
O1
O2
O7
O8
WORD DECODER
ADDRESS BUFFER
ADDRESS BUFFER
CHIP ENABLE
CE
A0 A1 A2 A3 A4 A5
A6 A7 A8
CE1 CE2 CE3 CE4

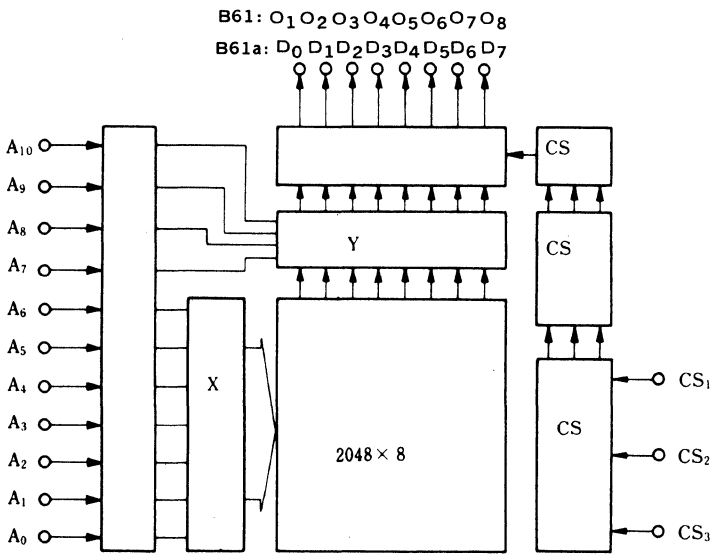

VCC A8 N.C. CE1 CE2 CE3 CE4 O8 O7 O6 O5 O4
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
A7 A6 A5 A4 A3 A2 A1 A0 O1 O2 O3 GND

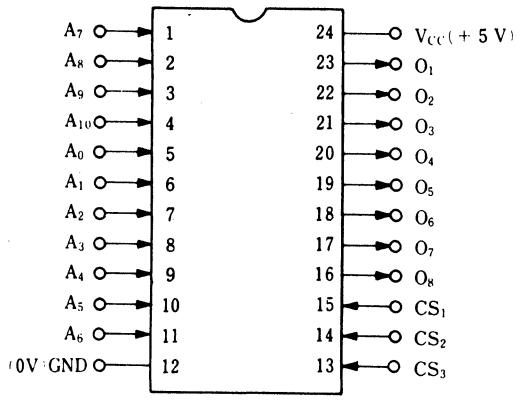
B60



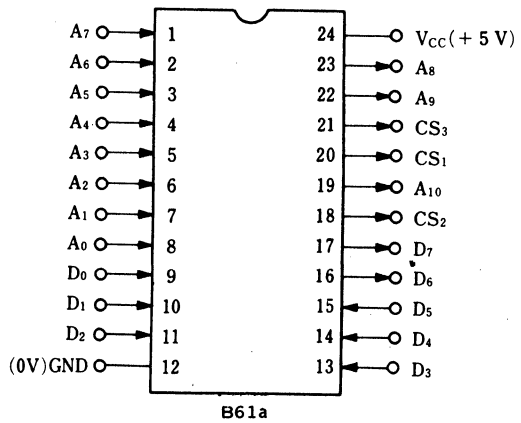


B61



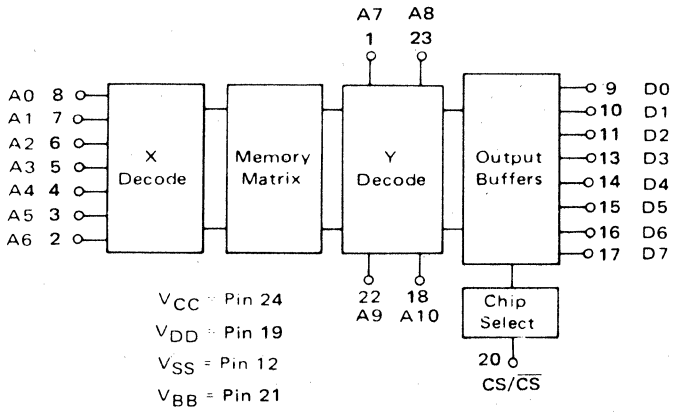


B61

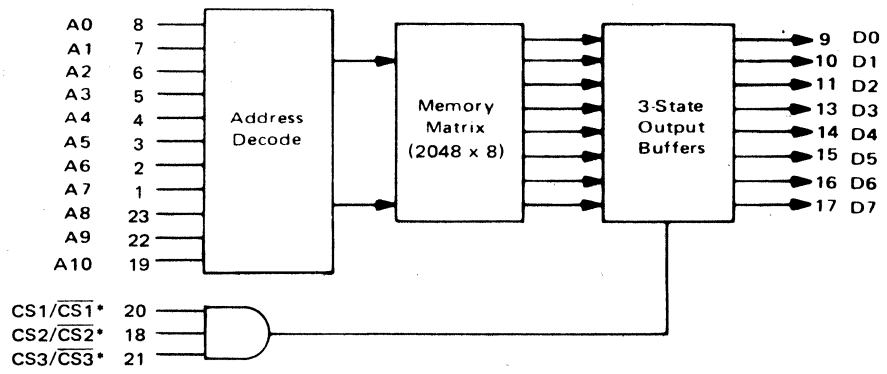


B61a

B62



B63

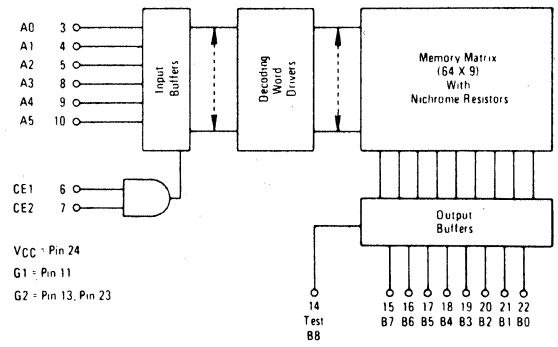


* Active level defined by the user.

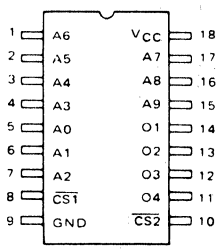
V_{CC} = Pin 24
Gnd = Pin 12

B64

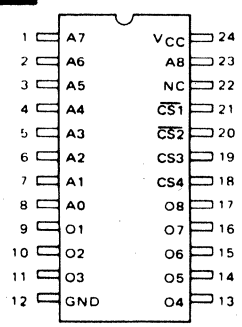
NOTE: Under normal operating conditions, G1 and G2 are connected to ground. Both CE1 and CE2 must be high to enable the memory.



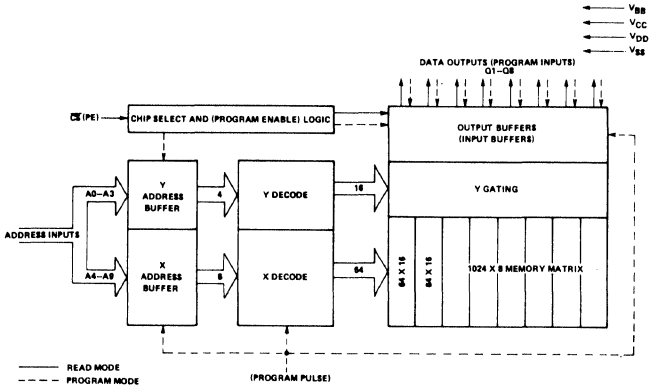
B66

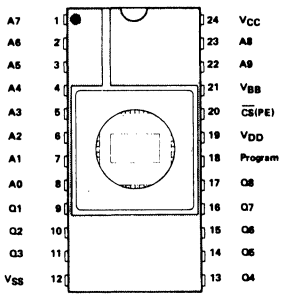


B67

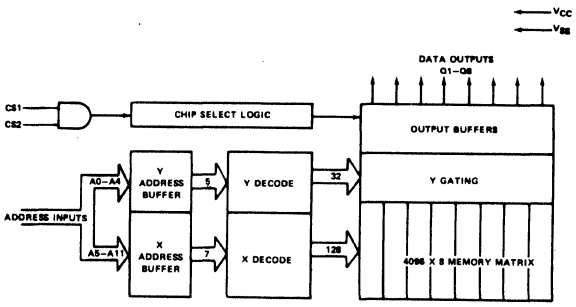


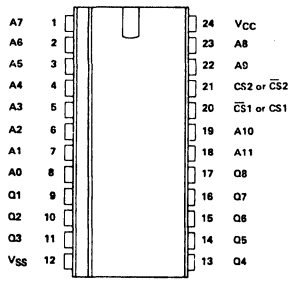
B68



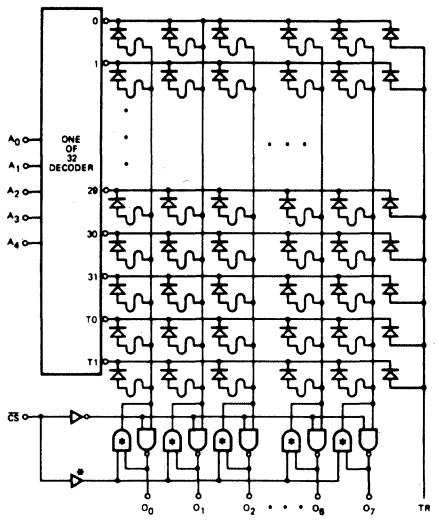


B69

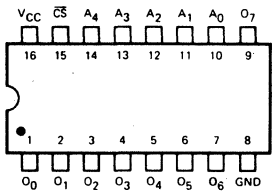




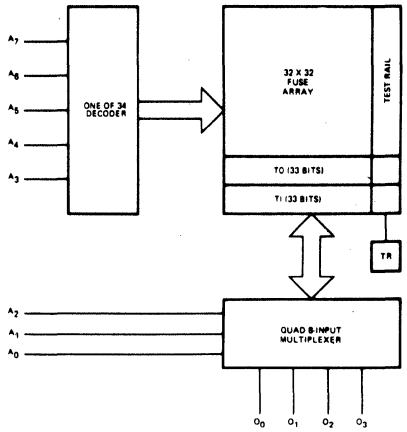
B70

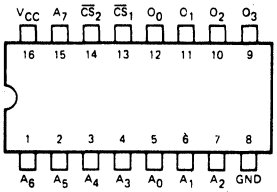


* = High Voltage Gate for Programming
T0 = Test Word
T1 = Test Word
TR = Test Rail



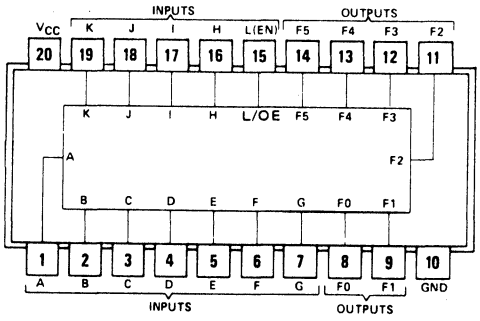
B71



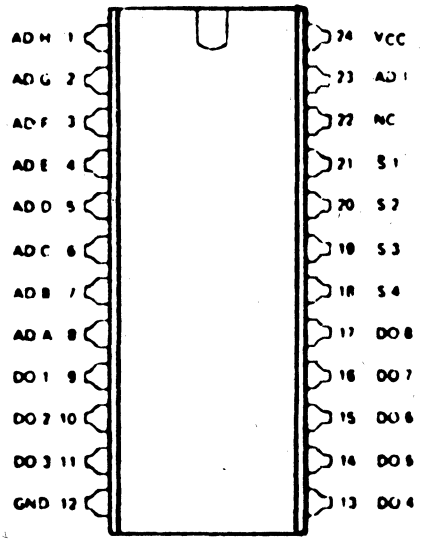


TO = Test Word
TI = Test Word
TR = Test Rail

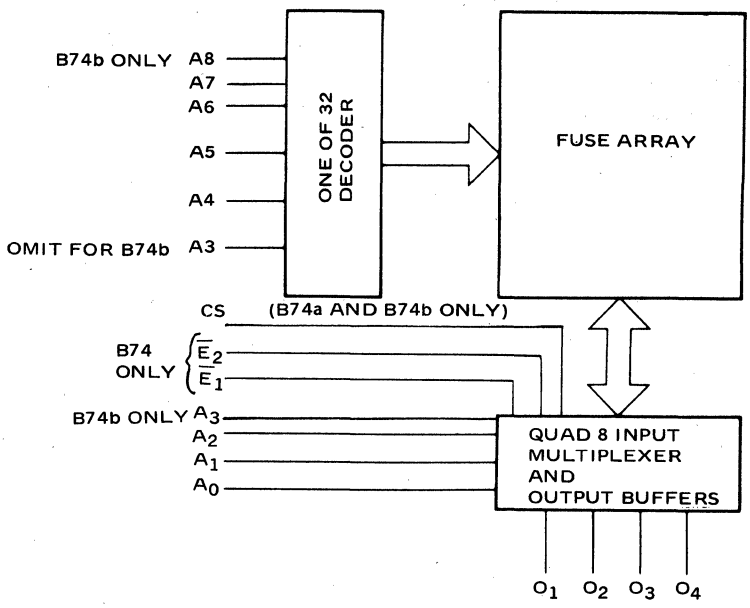
B72



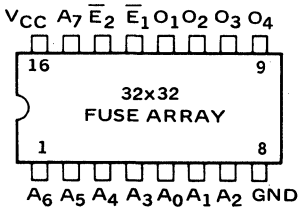
B73



B74

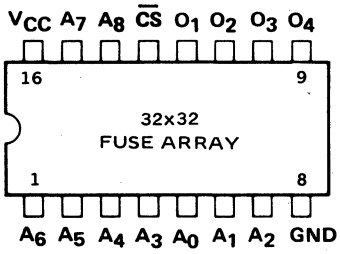


Top View



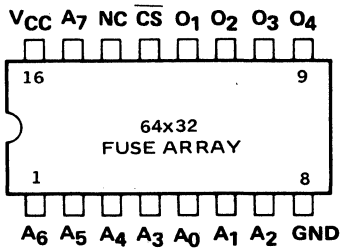
NOTE: PIN 1 IS MARKED FOR ORIENTATION

B74



PIN 13 IS ALSO THE PROGRAMMING PIN (PP)

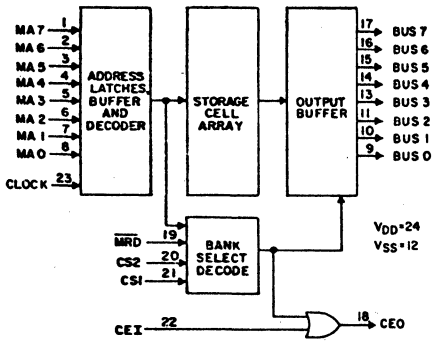
B74a



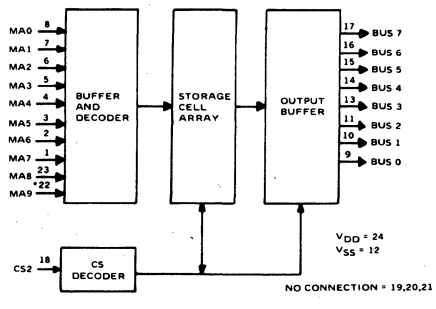
NOTE: PIN 1 IS MARKED FOR ORIENTATION

B74b

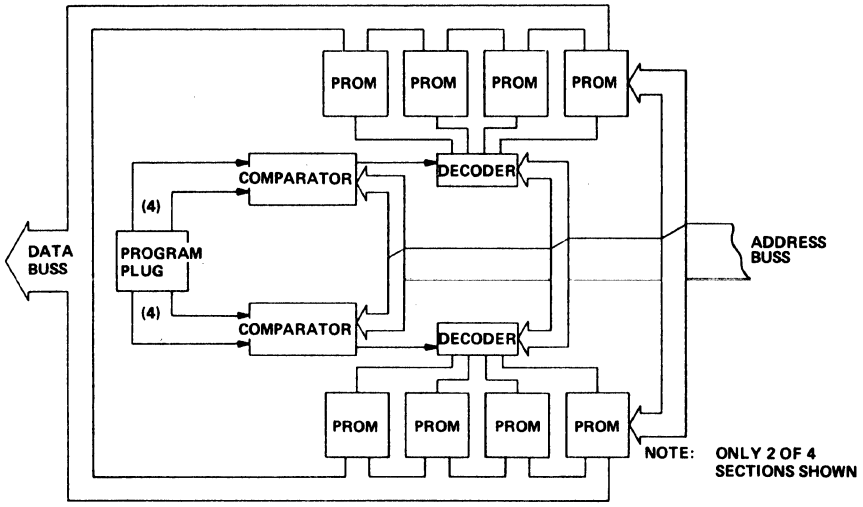
B75



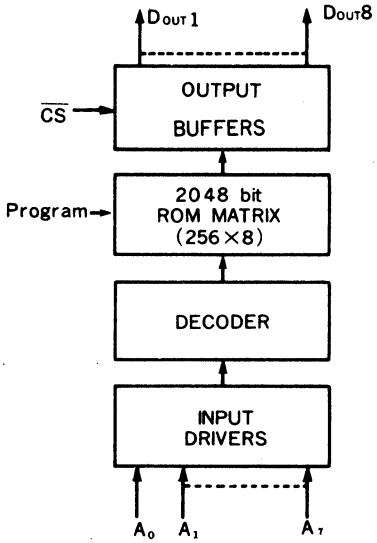
B76

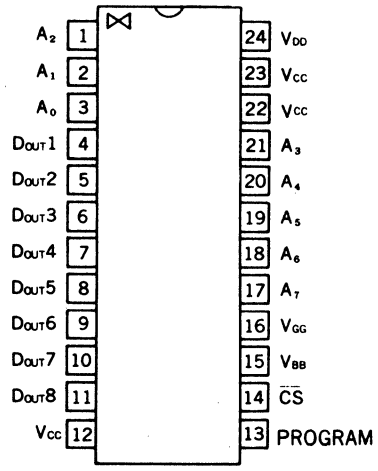


B77

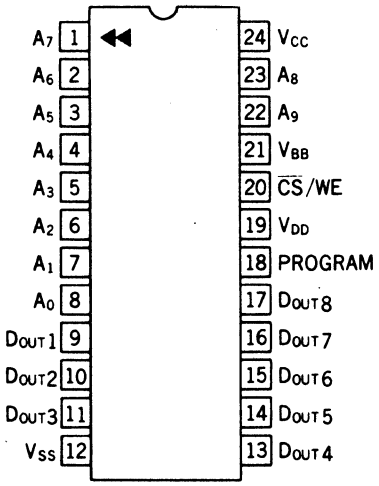

PROM
PROM
PROM
PROM
COMPARATOR
DECODER
(4)
PROGRAM PLUG
(4)
COMPARATOR
DECODER
DATA BUSS
ADDRESS BUSS
PROM
PROM
PROM
PROM
NOTE: ONLY 2 OF 4 SECTIONS SHOWN

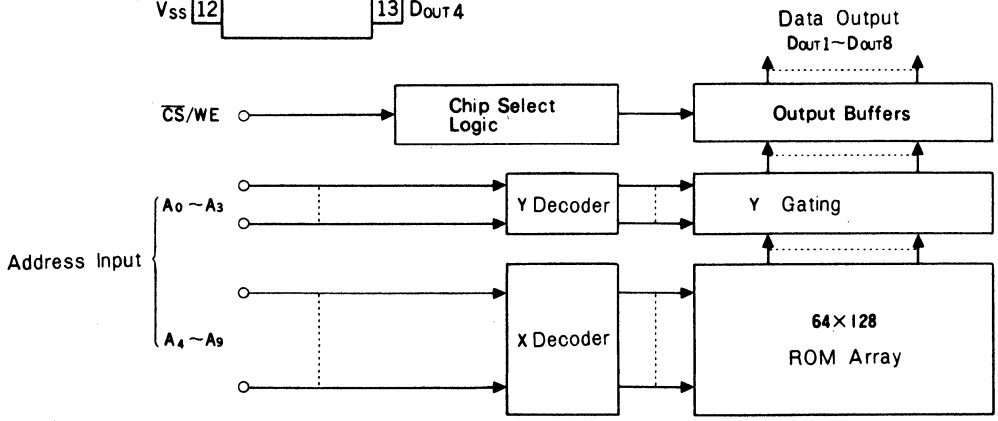
B78


DOUT1
DOUT8
CS
OUTPUT BUFFERS
Program
2048 bit ROM MATRIX (256×8)
DECODER
INPUT DRIVERS
A0
A1
A7

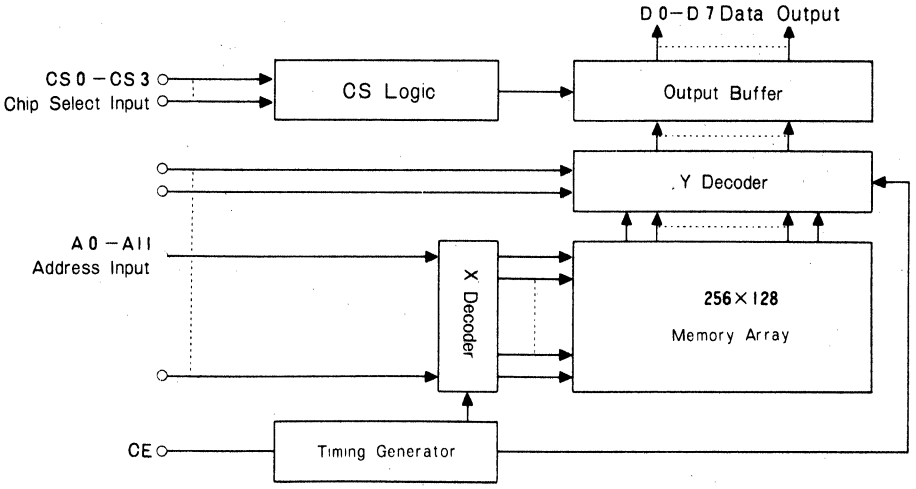

A2 1
A1 2
A0 3
DOUT1 4
DOUT2 5
DOUT3 6
DOUT4 7
DOUT5 8
DOUT6 9
DOUT7 10
DOUT8 11
VCC 12
24 VDD
23 VCC
22 VCC
21 A3
20 A4
19 A5
18 A6
17 A7
16 VGG
15 VBB
14 CS
13 PROGRAM

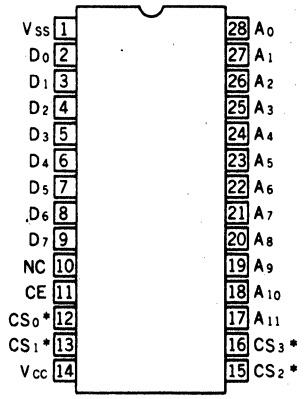
B79


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DOUT1 9
DOUT2 10
DOUT3 11
VSS 12
24 VCC
23 A8
22 A9
21 VBB
20 CS/WE
19 VDD
18 PROGRAM
17 DOUT8
16 DOUT7
15 DOUT6
14 DOUT5
13 DOUT4


Data Output
DOUT1~DOUT8
CS/WE
Chip Select Logic
Output Buffers
Address Input
A0 ~A3
Y Decoder
Y Gating
A4 ~A9
X Decoder
64×128
ROM Array

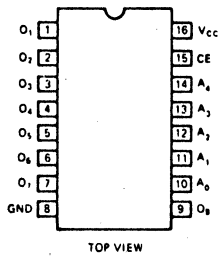
B80

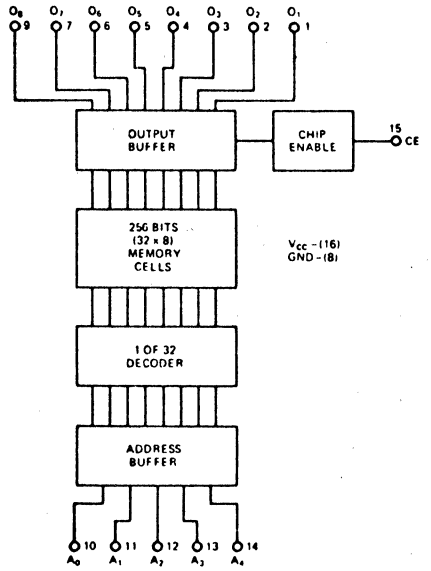




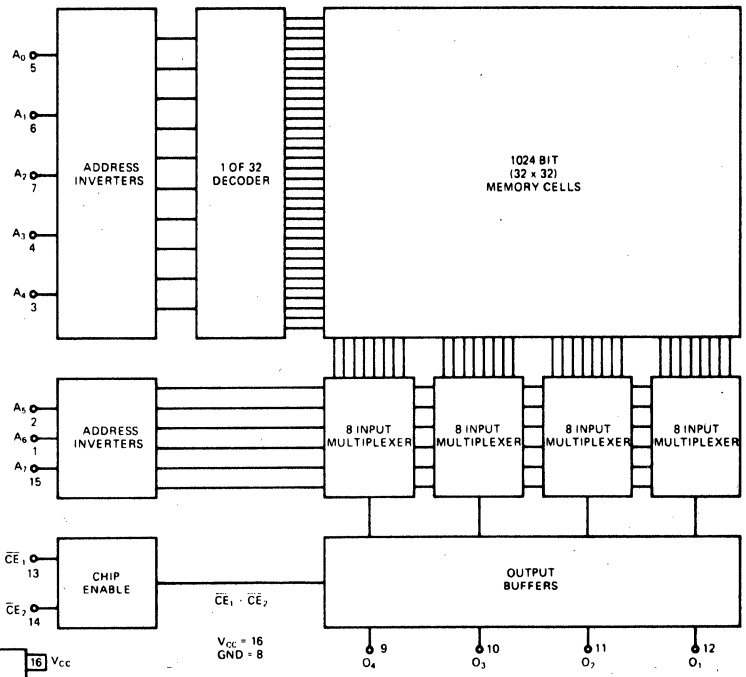
* Mask Programmable

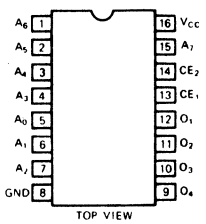
B81





B82

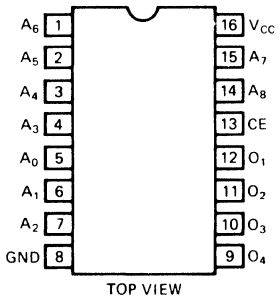




19. LOGIC/BLOCK DRAWINGS

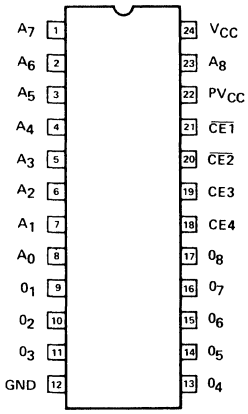
IN DRAWING NUMBER SEQUENCE

B83

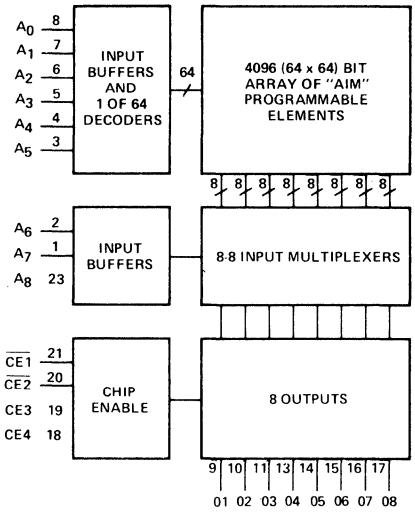


TOP VIEW

B84

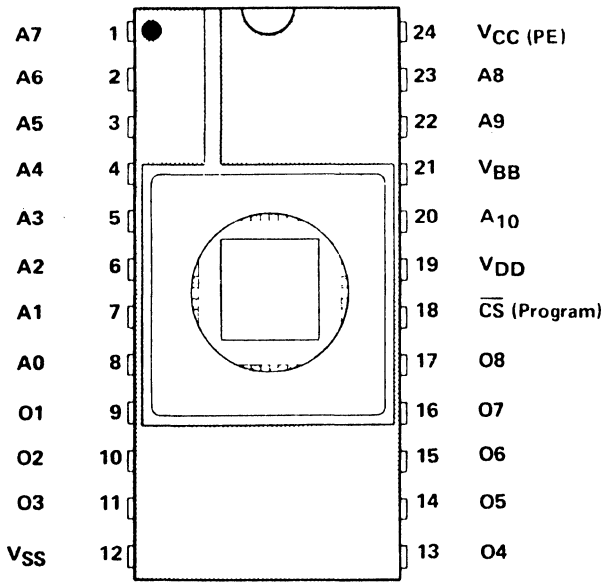


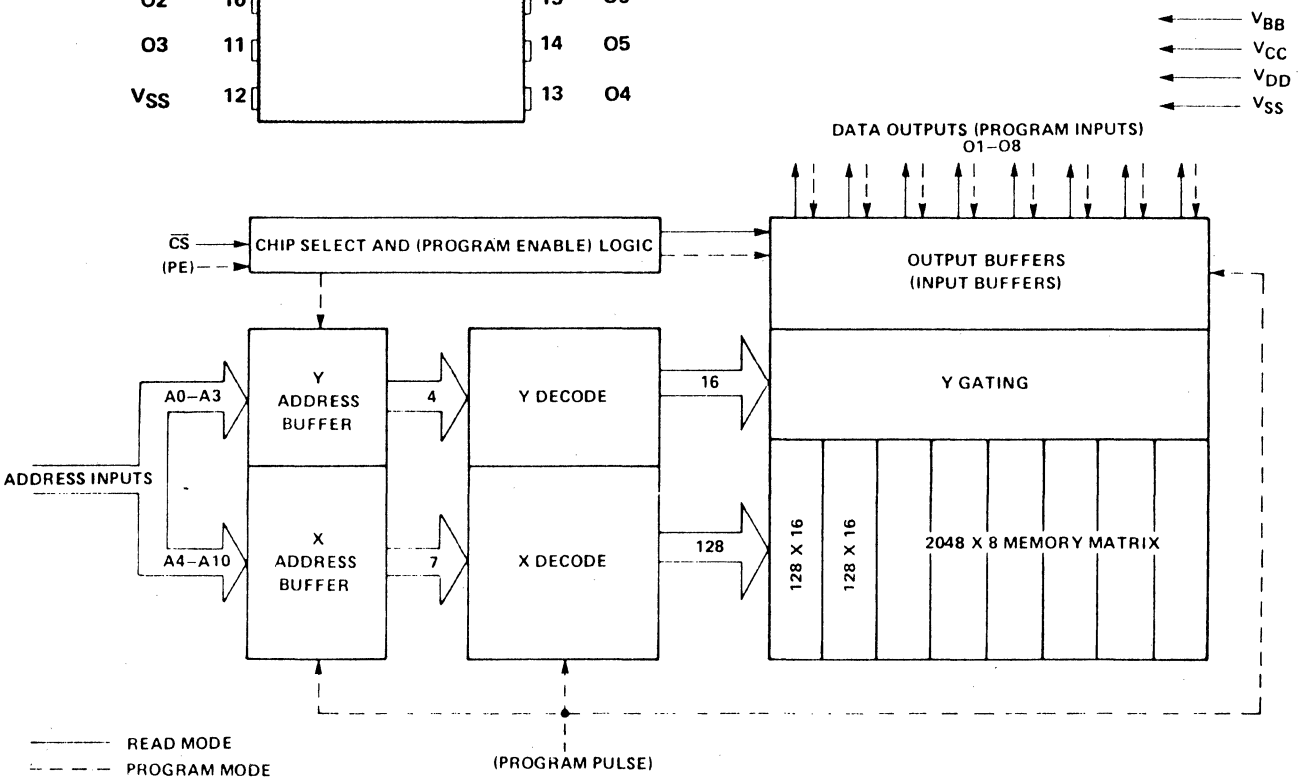
NOTE:
1. Pin 22 must be left open
2. The chip is enabled when E_1 and E_2 are low and E_3 and E_4 are high.



B85

(TOP VIEW)

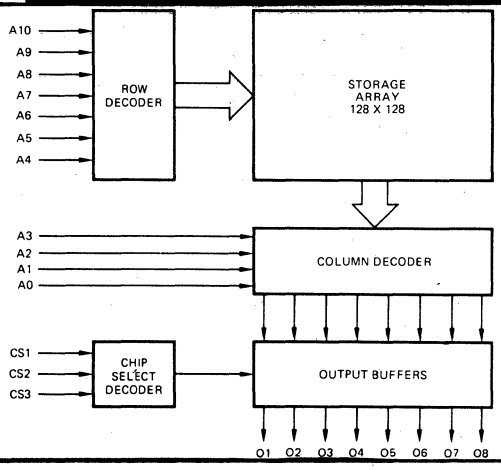


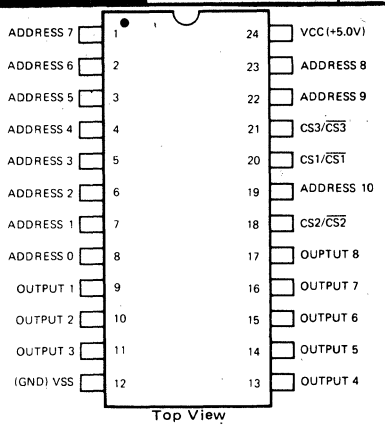


19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

B86

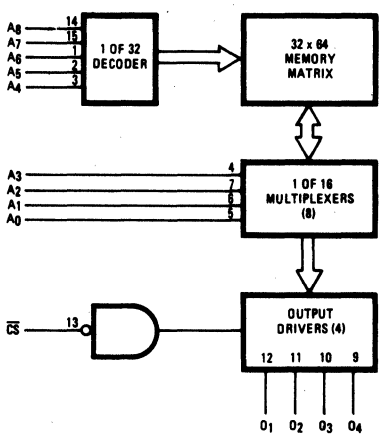


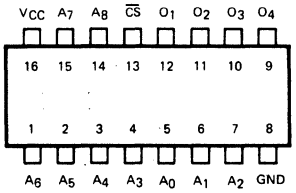


Top View

Pin 1 is marked for orientation.

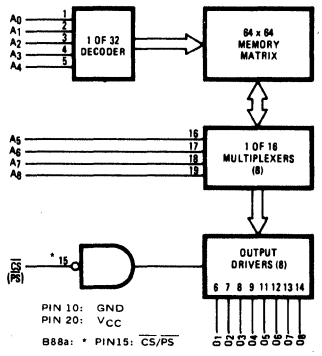
B87





Pin 13 is also the programming pin (pp).

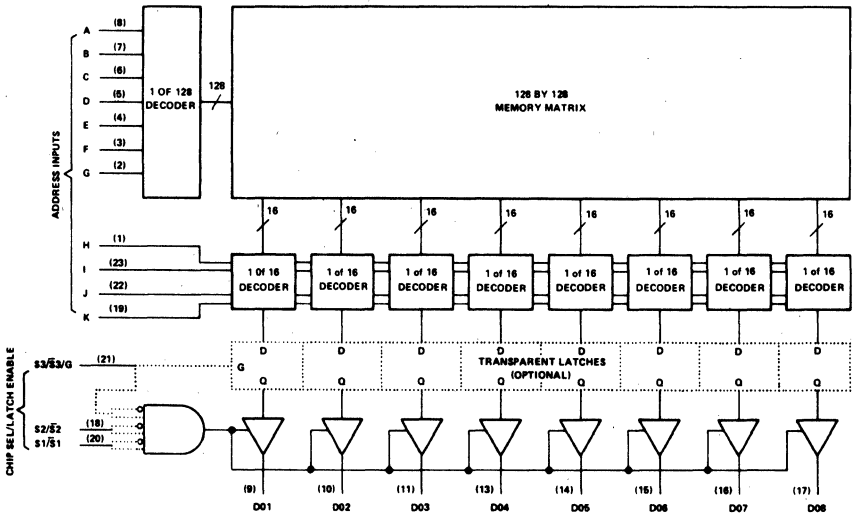
B88



PIN 10: GND
PIN 20: V_{CC}

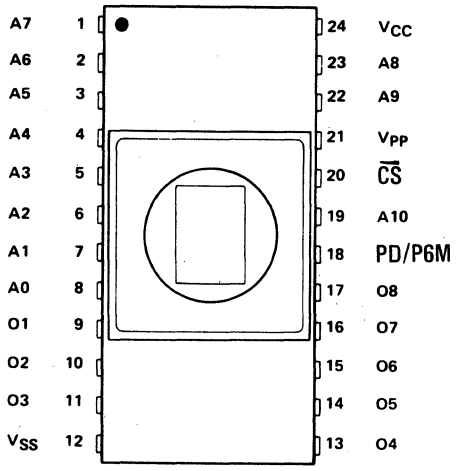
B88a: * PIN15: $\overline{CS}/\overline{PS}$

B89



NOTE: ····· INDICATES PROGRAMMABLE OPTIONS

B90



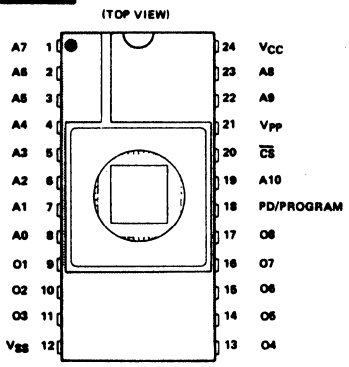
Pin #	24	23	22	21	20	19	18	17	16	14	13	12
B90	VCC	A8	A9	VPP	PD/P6M	A10	A11	O8	O7	O5	O4	VSS
B90a	VCC	A8	A9	VPP	CS	A10	PG/P6M	O8	O7	O5	O4	VSS

Pin #	11	10	9	8	7	6	5	4	3	2	1	15
B90	O3	O2	O1	A0	A1	A2	A3	A4	A5	A6	A7	O8
B90a	O3	O2	O1	A0	A1	A2	A3	A4	A5	A6	A7	O8

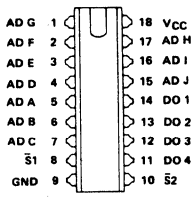
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

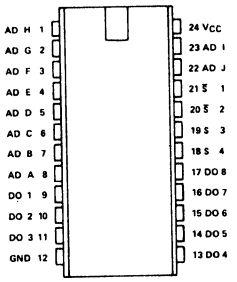
B91



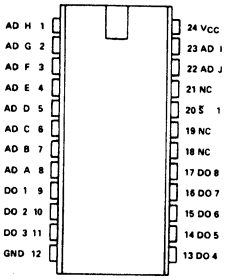
B92



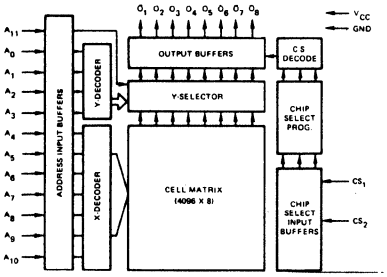
B93

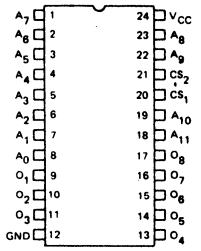


B94

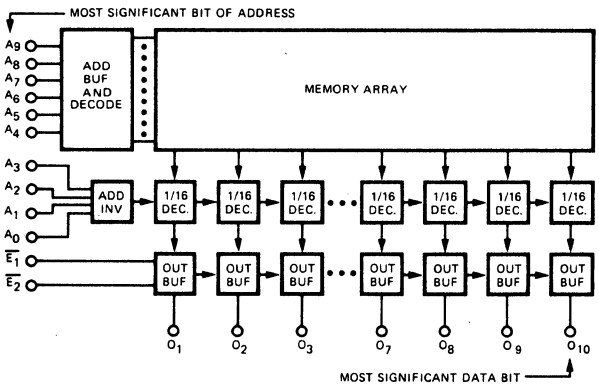


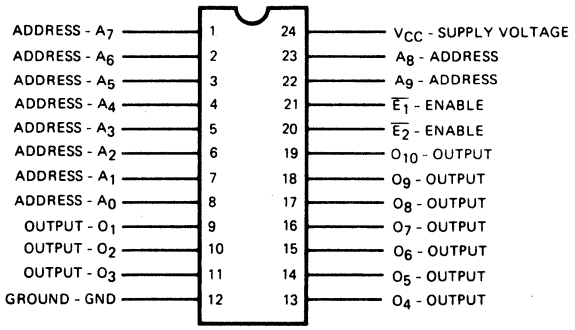
B96



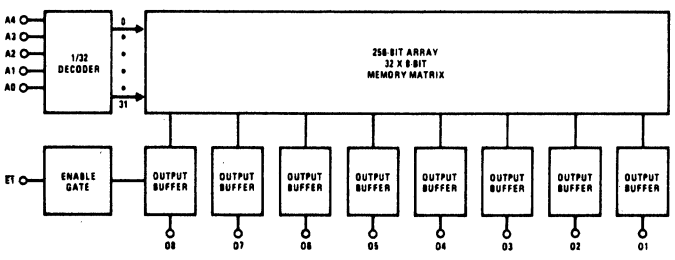


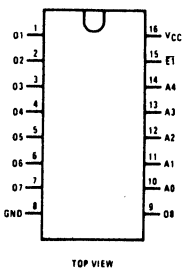
B97



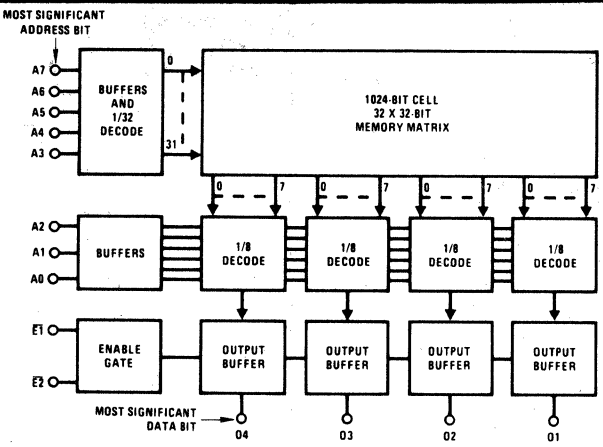


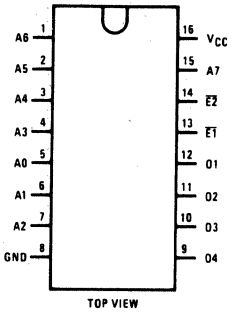
B98



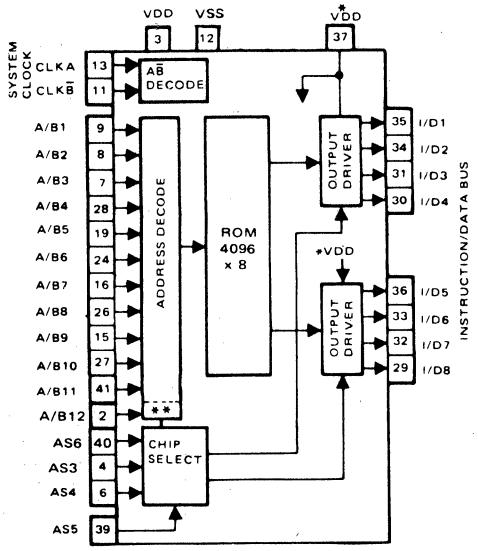


B99





B100

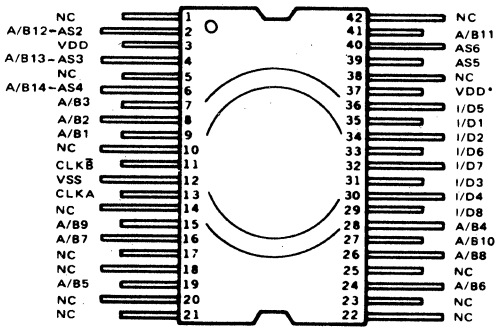


*THIS INPUT IS A SEPARATE VDD SOURCE FOR THE OUTPUT DRIVERS. THIS IS USEFUL FOR ISOLATING INDIVIDUAL CIRCUITS DURING DEVICE TESTING AND FAULT ISOLATION WHEN MULTIPLE CIRCUITS ARE CONNECTED TO THE DATA BUS.

**P CODES ARE AVAILABLE TO REVERSE PINS 2 AND 4 FOR ROMS USED IN VIRTUAL SYSTEMS INTERNALLY.

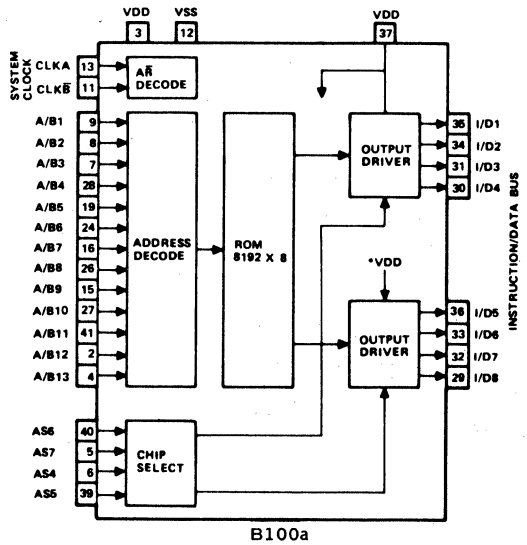
THE AS5 INPUT AND AS6 INPUT MAY BE DISABLED BY MARK OPERATION.

B100



*SEPARATE VDD FOR OUTPUT DRIVERS

B100



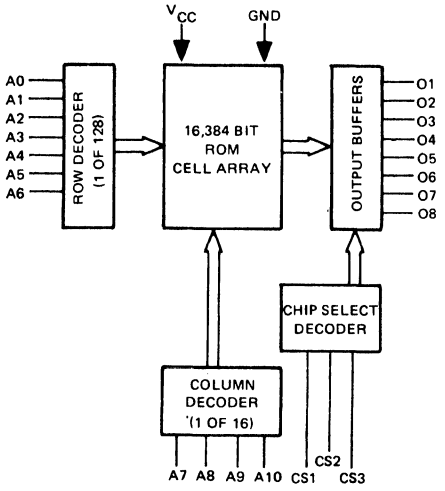
B100a

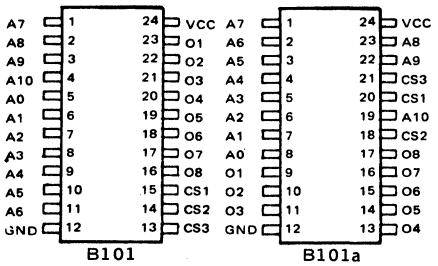
B100a: PIN 2 = A/B12
PIN 4 = A/B13
PIN 5 = AS7
PIN 6 = AS4

19. LOGIC/BLOCK DRAWINGS

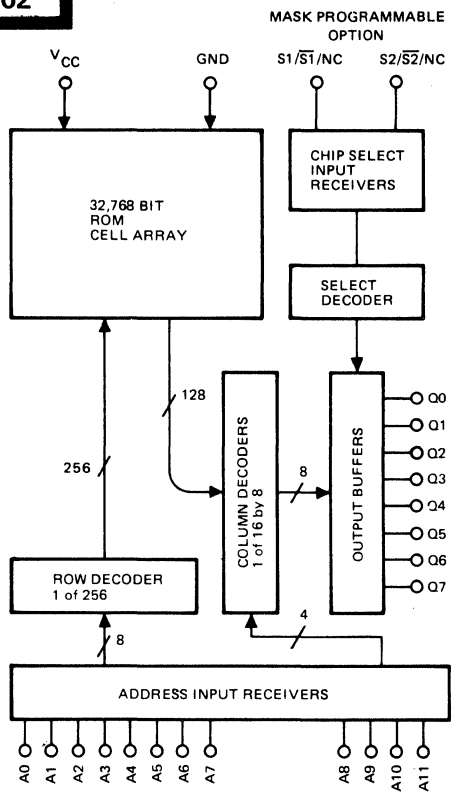
IN DRAWING NUMBER SEQUENCE

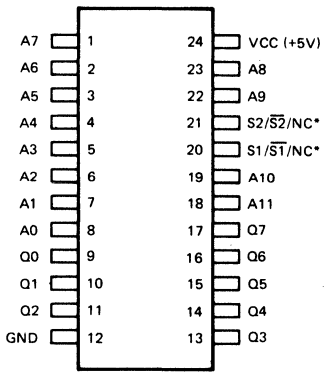
B101





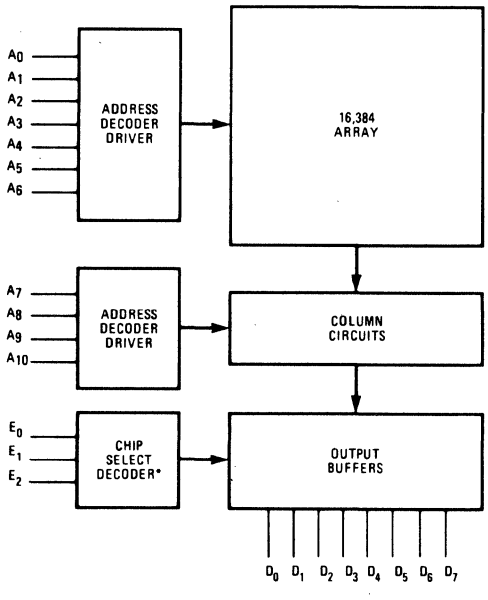
B102



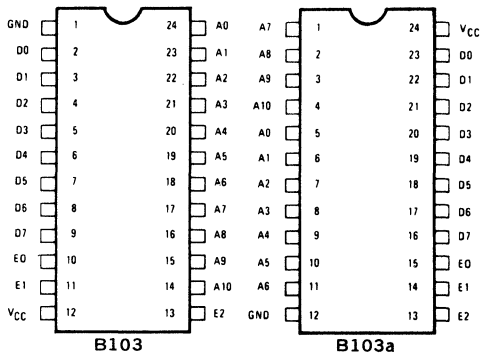


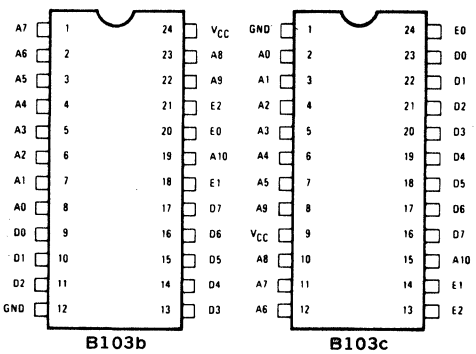
*Mask-programmable option

B103



*PROGRAMMABLE CHIP SELECTS

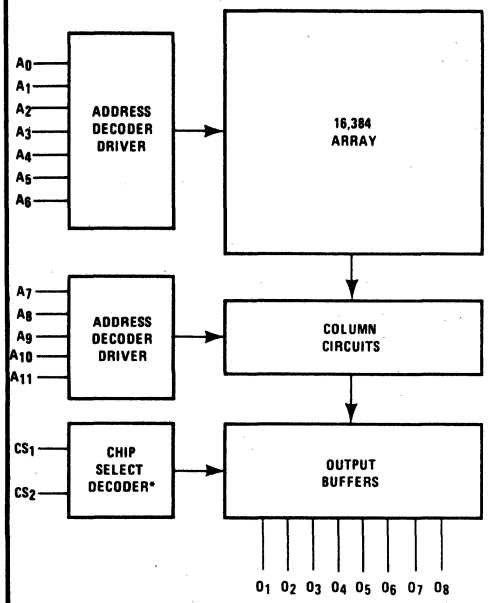




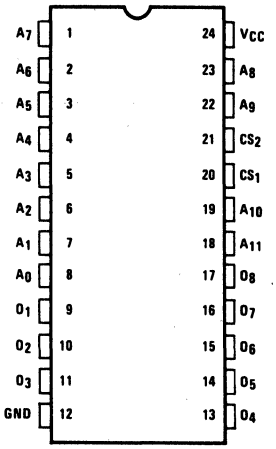
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

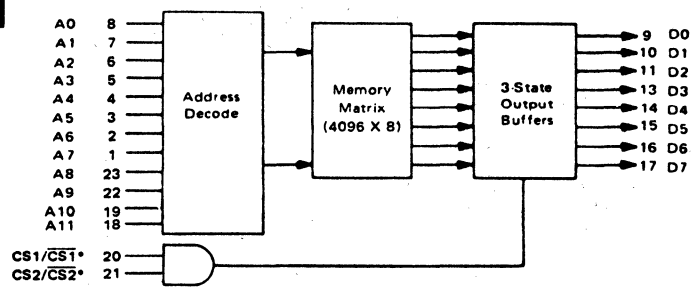
B104



*PROGRAMMABLE CHIP SELECTS



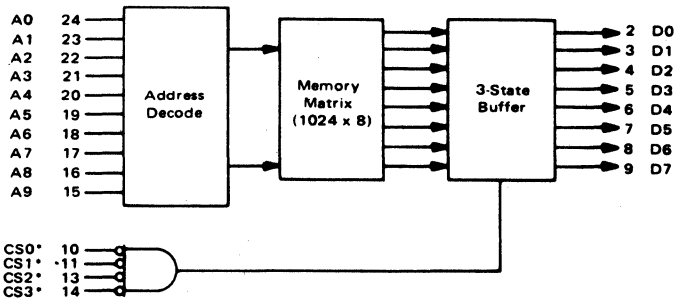
B105



* Active level defined by the user.

VCC = Pin 24
Gnd = Pin 12

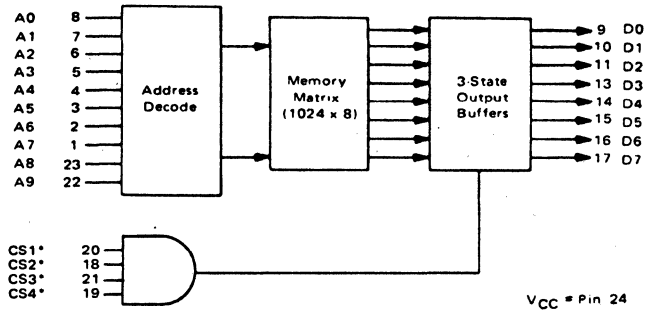
B106



*Active level defined by the customer.

VCC = Pin 12
Gnd = Pin 1

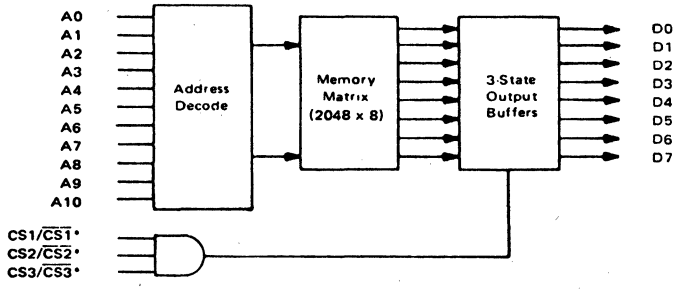
B107



*Active level defined by the customer.

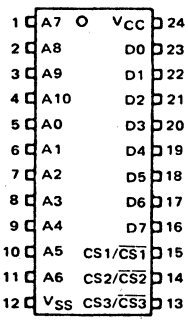
VCC = Pin 24
Gnd = Pin 12

B108

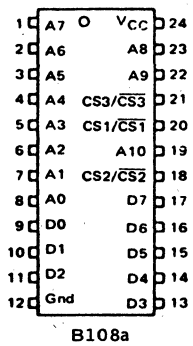


* Active level defined by the user.

VCC = Pin 24
VSS = Pin 12

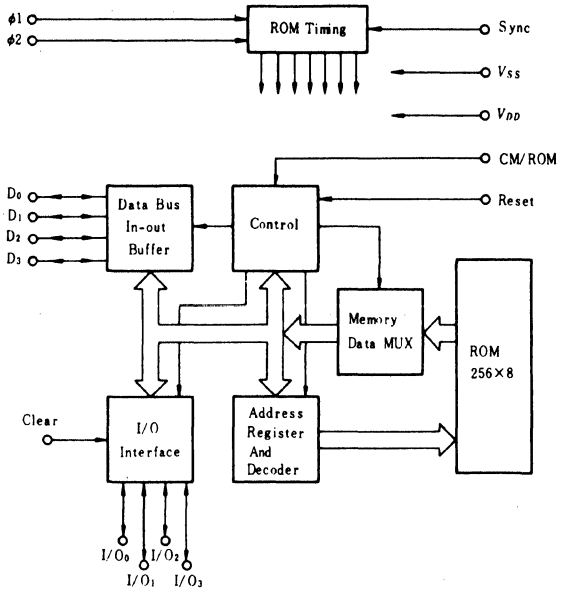


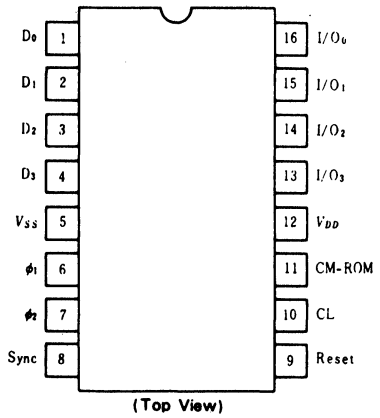
B108



B108a

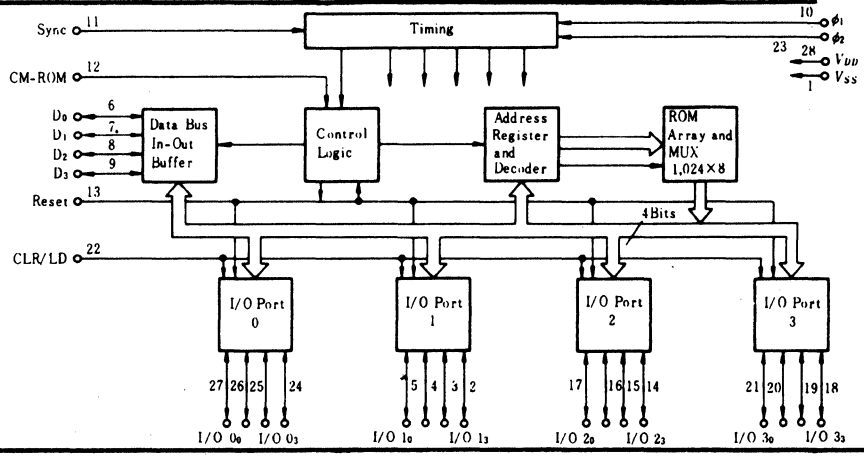
B109

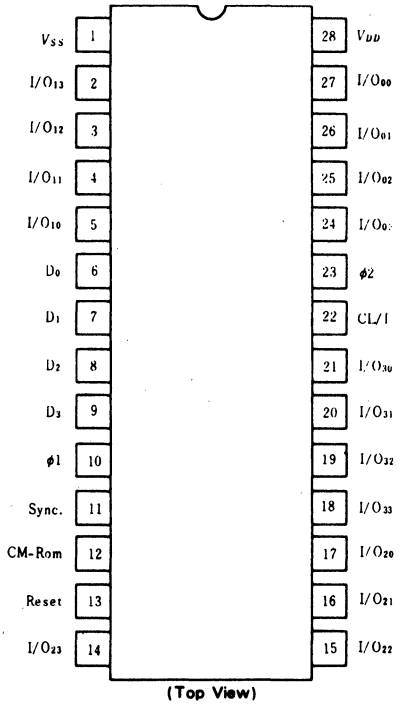




(Top View)

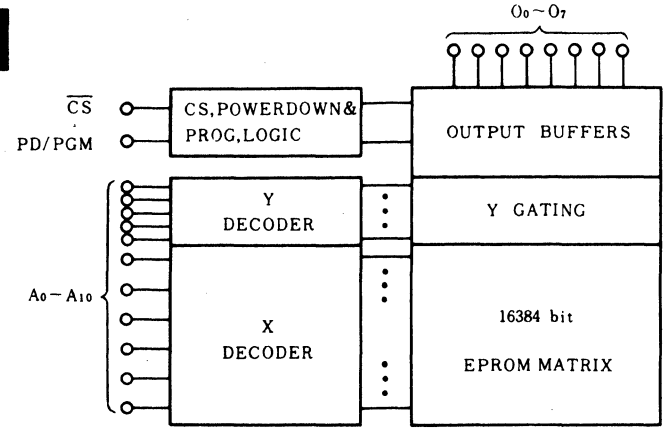
B110

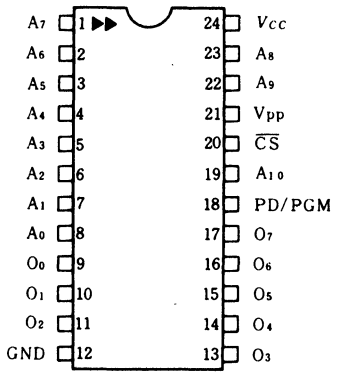




(Top View)

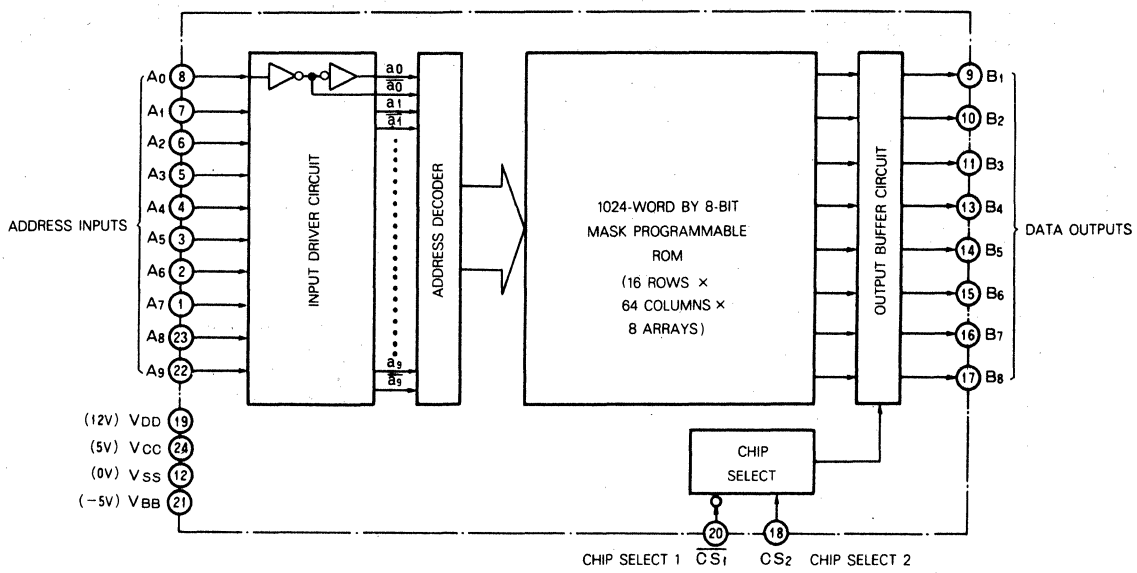
B111



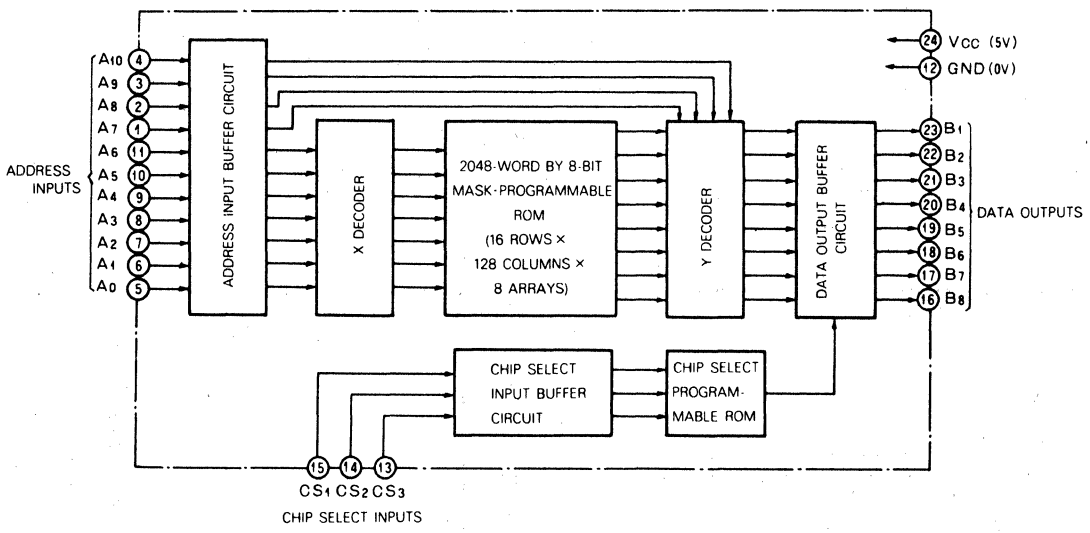


(Top View)

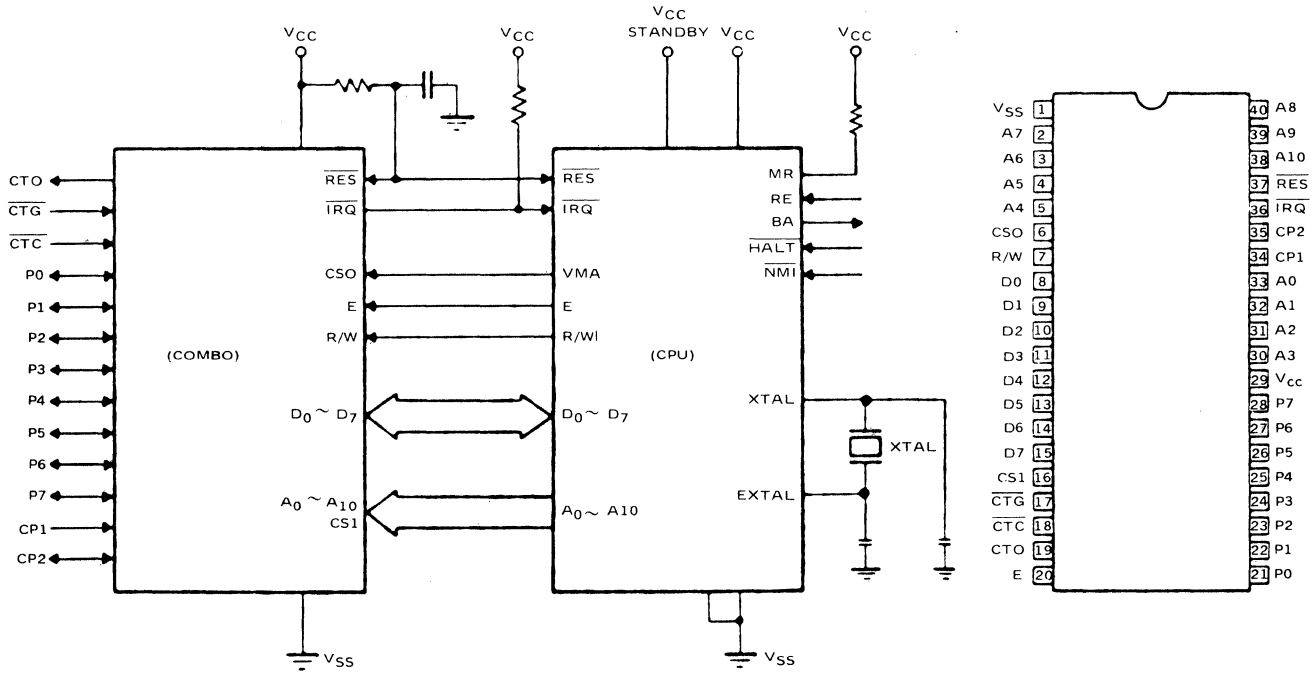
B112


ADDRESS INPUTS
A0 8
A1 7
A2 6
A3 5
A4 4
A5 3
A6 2
A7 1
A8 23
A9 22
INPUT DRIVER CIRCUIT
a0
ā0
a1
ā1
a9
ā9
ADDRESS DECODER
1024-WORD BY 8-BIT
MASK PROGRAMMABLE
ROM
(16 ROWS ×
64 COLUMNS ×
8 ARRAYS)
OUTPUT BUFFER CIRCUIT
9 B1
10 B2
11 B3
13 B4
14 B5
15 B6
16 B7
17 B8
DATA OUTPUTS
(12V) VDD 19
(5V) VCC 24
(0V) VSS 12
(−5V) VBB 21
CHIP SELECT
CHIP SELECT 1
20 CS1
18 CS2
CHIP SELECT 2

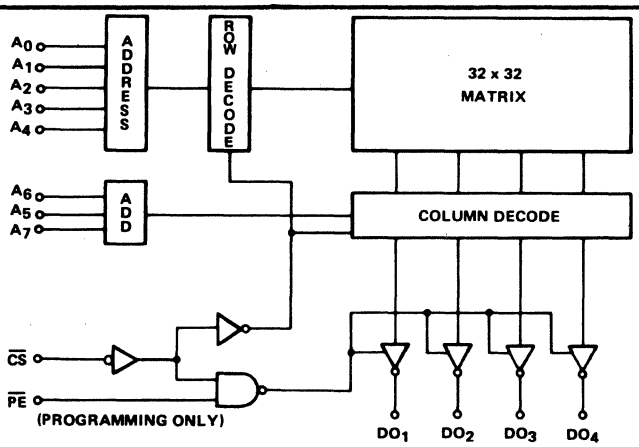
B113


ADDRESS INPUTS
A10 4
A9 3
A8 2
A7 1
A6 11
A5 10
A4 9
A3 8
A2 7
A1 6
A0 5
ADDRESS INPUT BUFFER CIRCUIT
X DECODER
2048-WORD BY 8-BIT
MASK-PROGRAMMABLE
ROM
(16 ROWS ×
128 COLUMNS ×
8 ARRAYS)
Y DECODER
DATA OUTPUT BUFFER
CIRCUIT
24 VCC (5V)
12 GND (0V)
23 B1
22 B2
21 B3
20 B4
19 B5
18 B6
17 B7
16 B8
DATA OUTPUTS
CHIP SELECT
INPUT BUFFER
CIRCUIT
CHIP SELECT
PROGRAM-
MABLE ROM
15 14 13
CS1 CS2 CS3
CHIP SELECT INPUTS

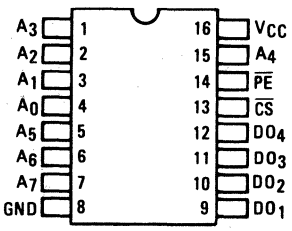
B114



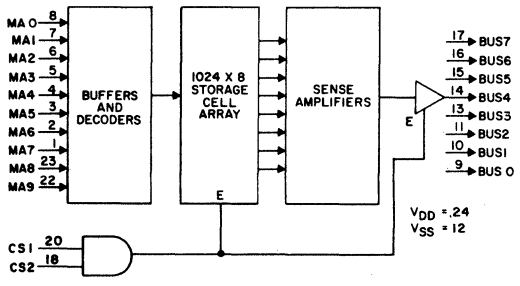
B115



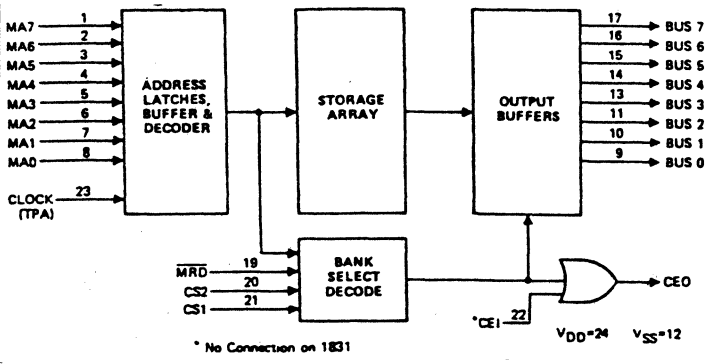
TOP VIEW - D.I.P.



B116



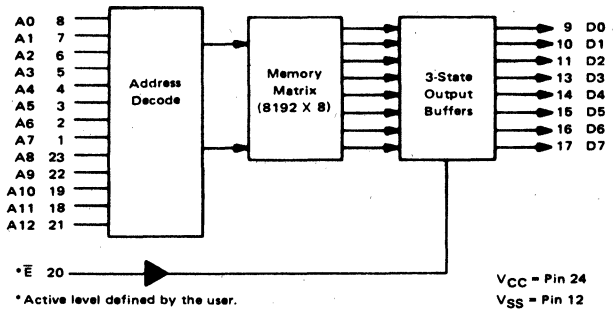
B117



19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

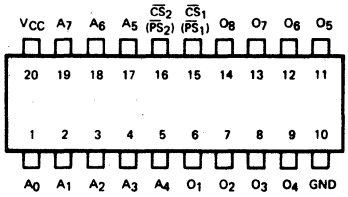
B118



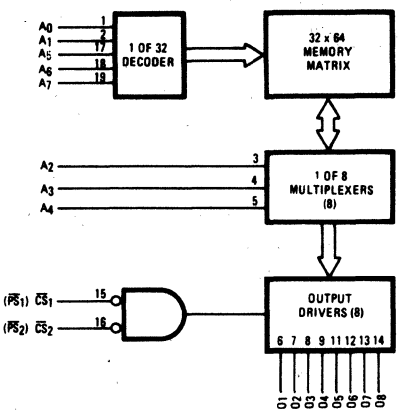
*Active level defined by the user.

V_{CC} = Pin 24
V_{SS} = Pin 12

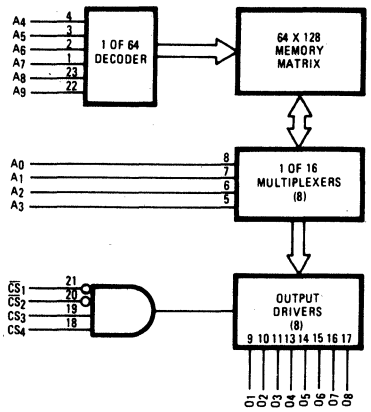
B119

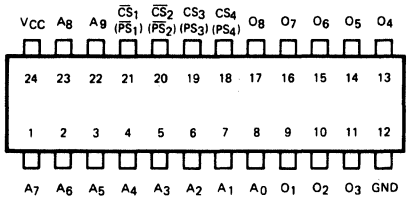


Pin 15 is also the programmiag pin (pp).



B120

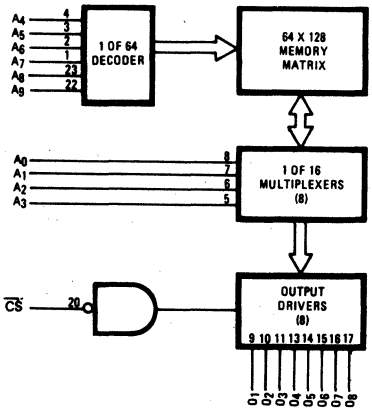


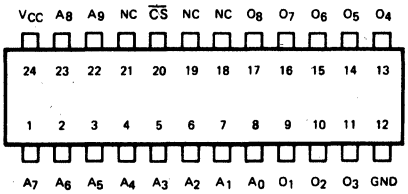


Pin 20 is also the programming pin.

B120a: PINS: 18 - CS_4 (PS_4)
19 - CS_3 (PS_3)
20 - $\overline{CS}_2$ ($\overline{PS}_2$)
21 - $\overline{CS}_1$ ($\overline{PS}_1$)

B121

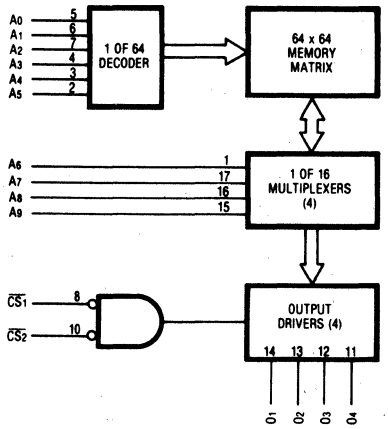


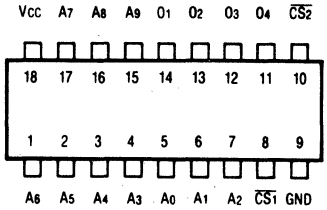


Pin 20 is also the programming pin.

B121a: PIN 20 - $\overline{CS}$ ($\overline{PS}$)

B122





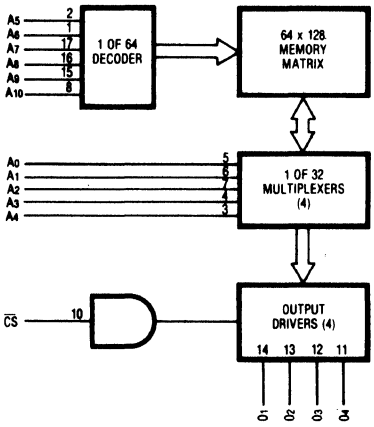
Pin 10 is also the programming pin.

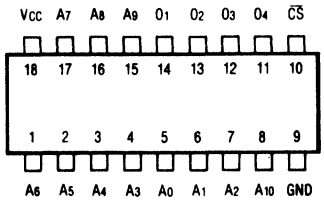
B122a: PINS- 8 - $\overline{CS}_1$ ($\overline{PS}_1$)
10 - $\overline{CS}_2$ ($\overline{PS}_2$)

19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

B123

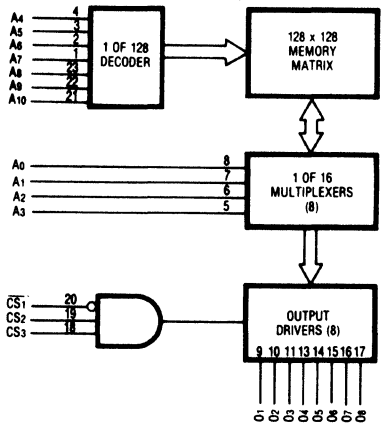


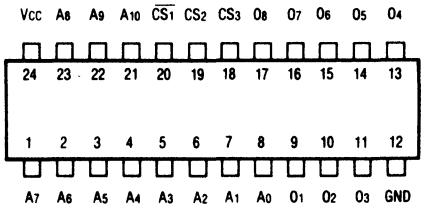


B123a: PIN 10 - $\overline{CS}$ ($\overline{PS}$)

Pin 10 is also the programming pin.

B124

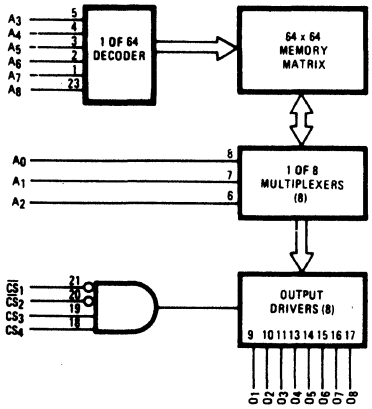


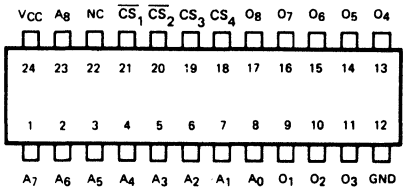


B124a: PINS: 18 - CS_3 (PS_3)
19 - CS_2 (PS_2)
20 - $\overline{CS_1}$ (PS_1)

Pin 20 is also the programming pin.

B125

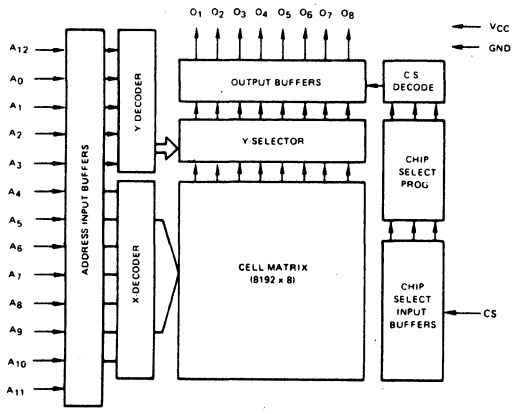


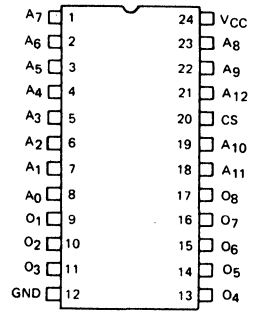


B125a: PINS 21 - $\overline{CS_1}$ ($\overline{PS_1}$)
20 - $\overline{CS_2}$ ($\overline{PS_2}$)
19 - CS_3 (PS_3)
18 - CS_4 (PS_4)

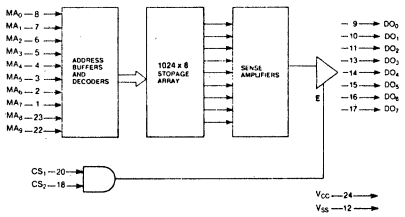
Pin 20 is also the programming pin.

B126



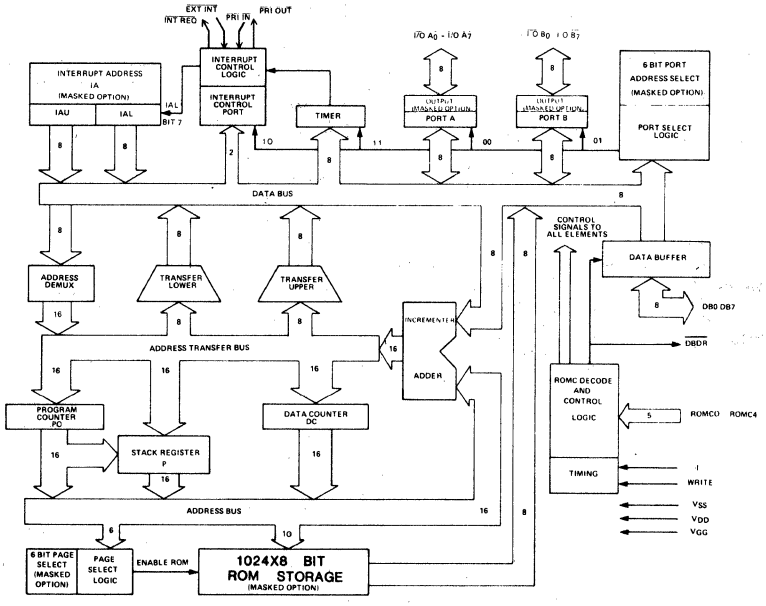


B127



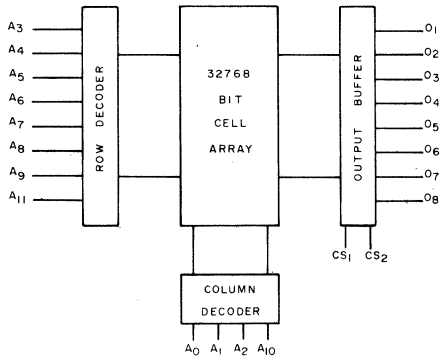
B128

FUNCTIONAL DIAGRAM

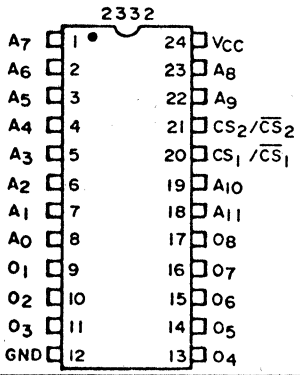


B129

BLOCK DIAGRAM

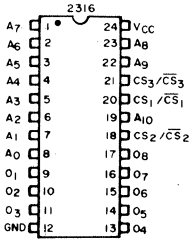


PIN CONFIGURATION

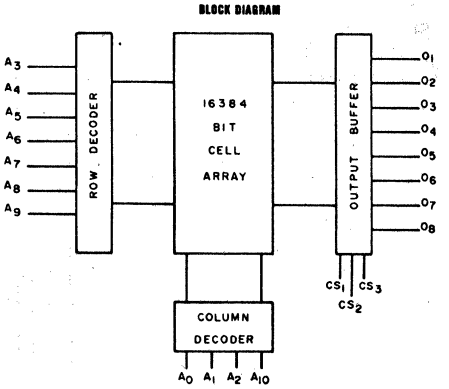


B131

PIN CONFIGURATION



BLOCK DIAGRAM

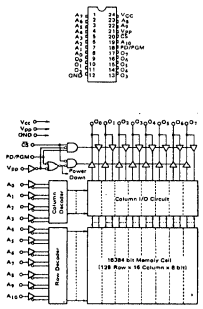


B130

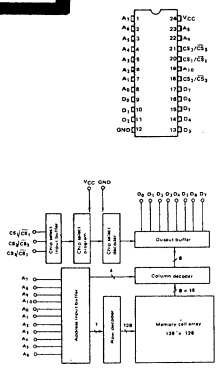
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

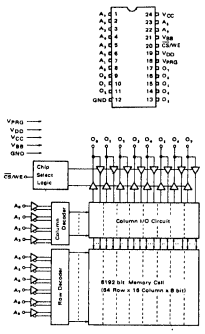
B132



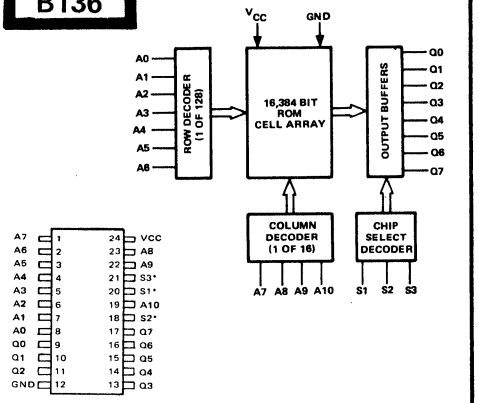
B133



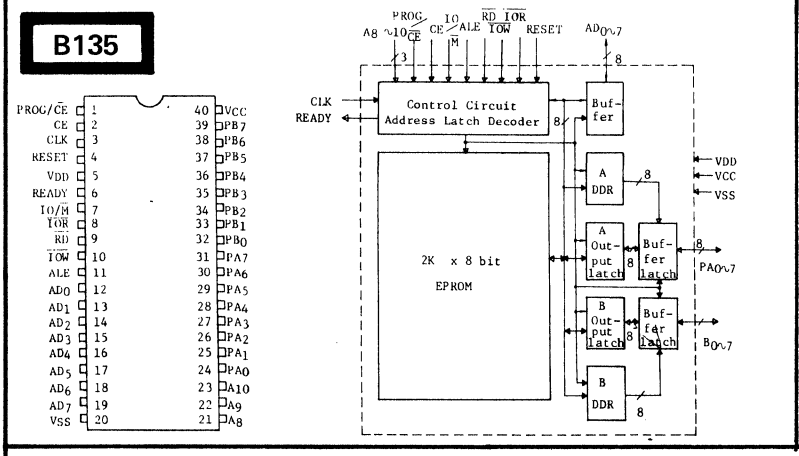
B134



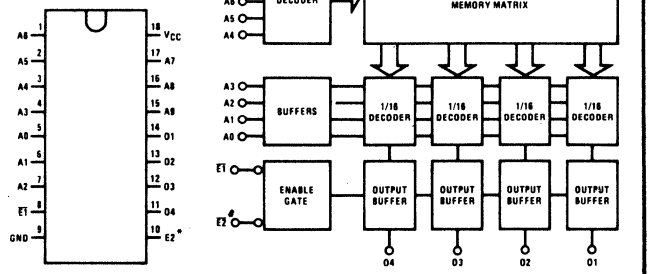
B136



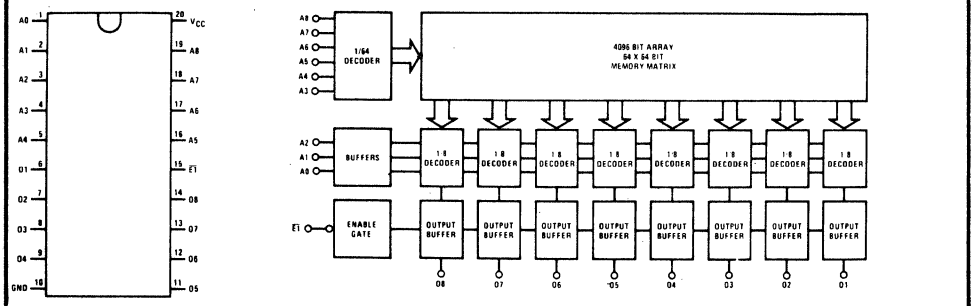
B135



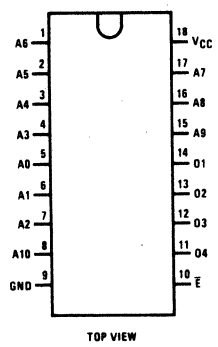
B139



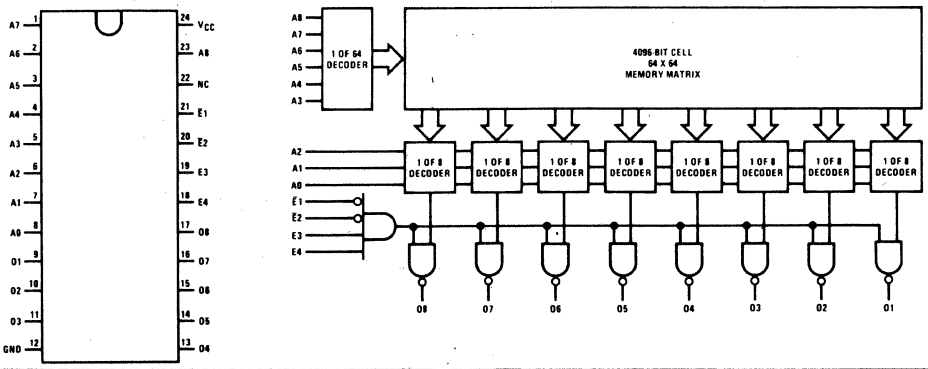
B137

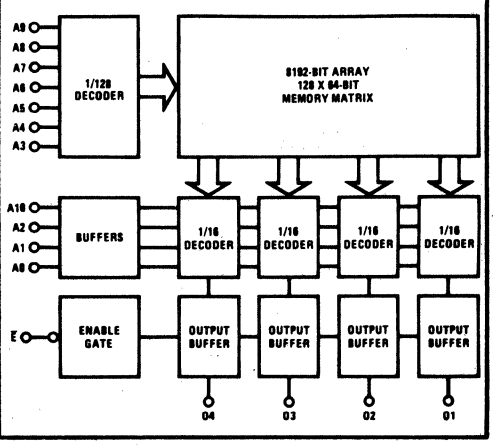


B140



B138





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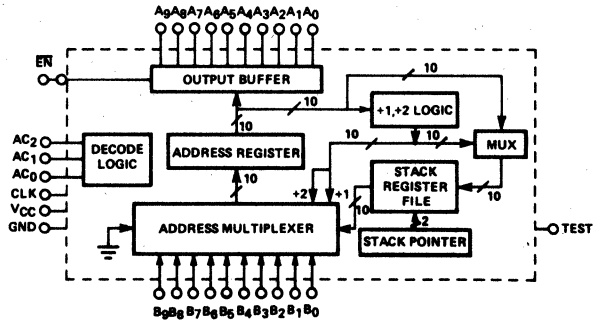

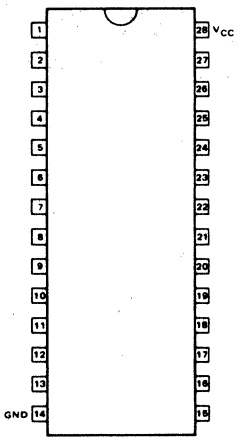

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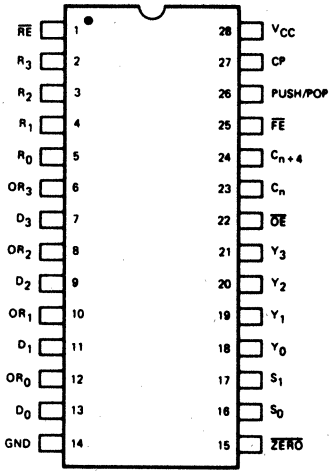

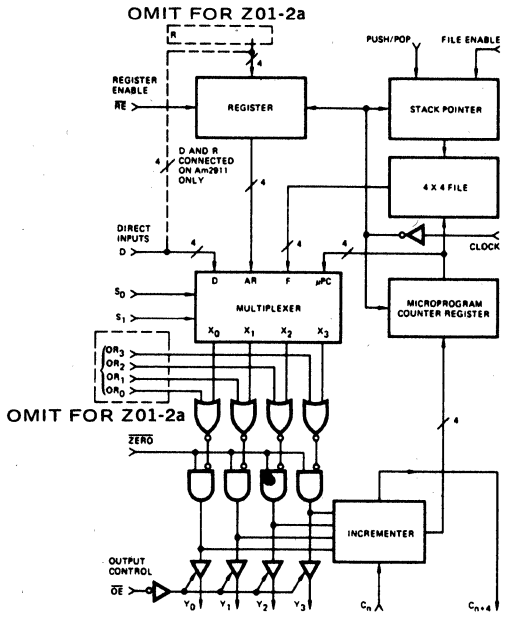

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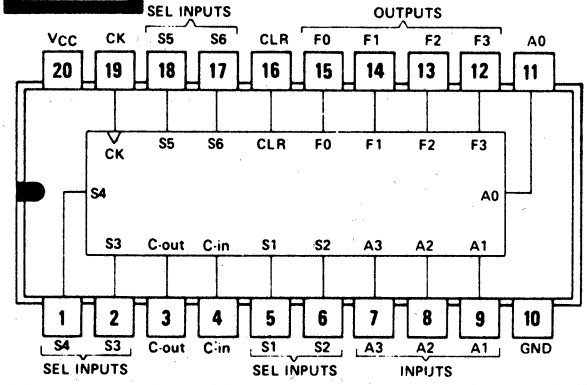

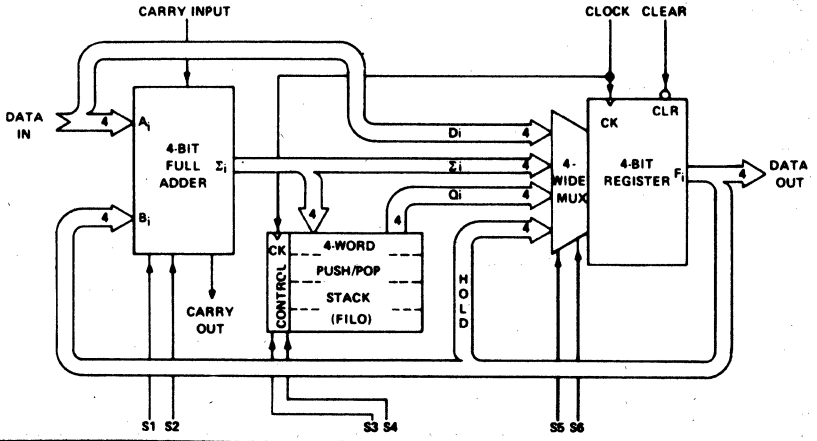

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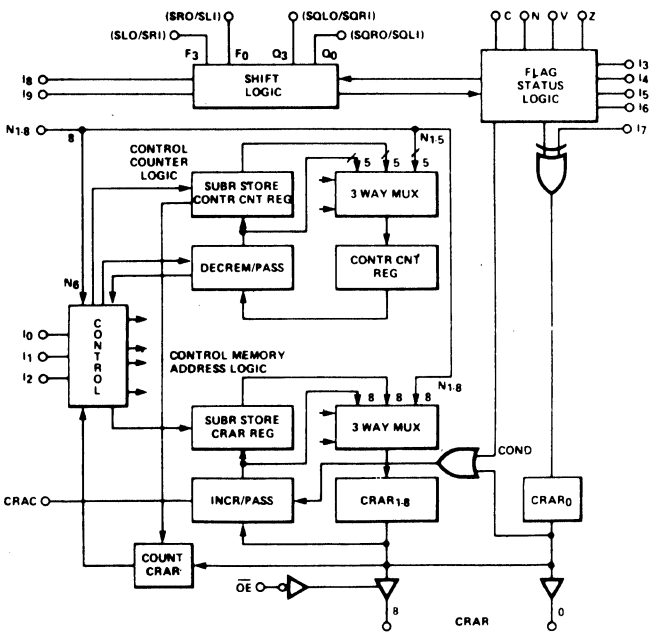
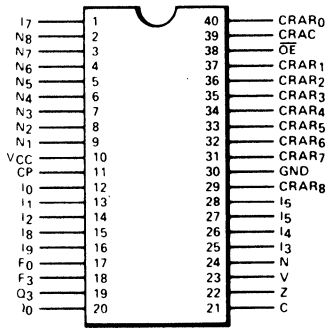
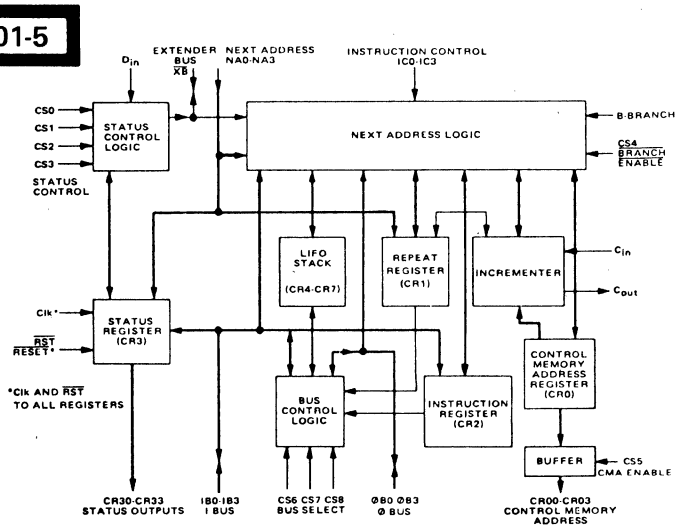
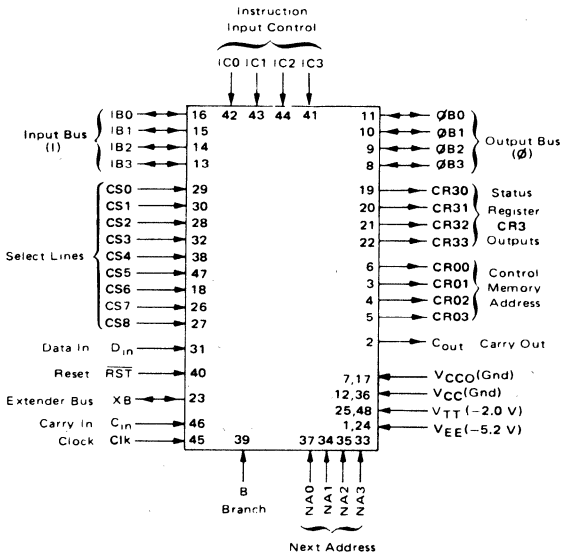




Z01-5





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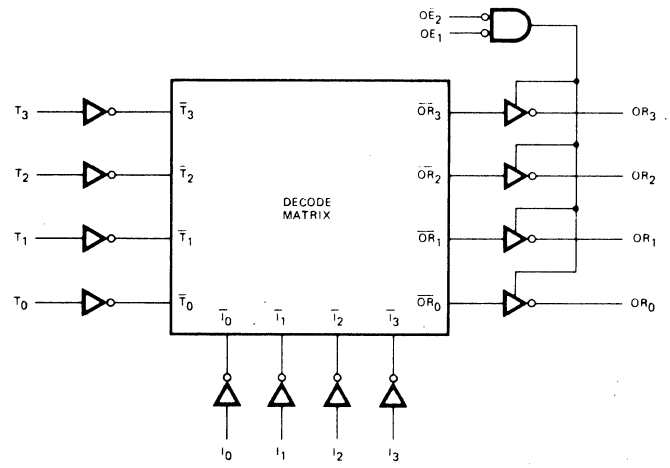

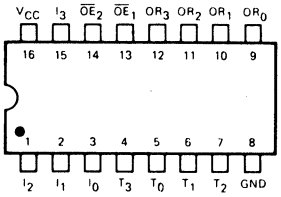

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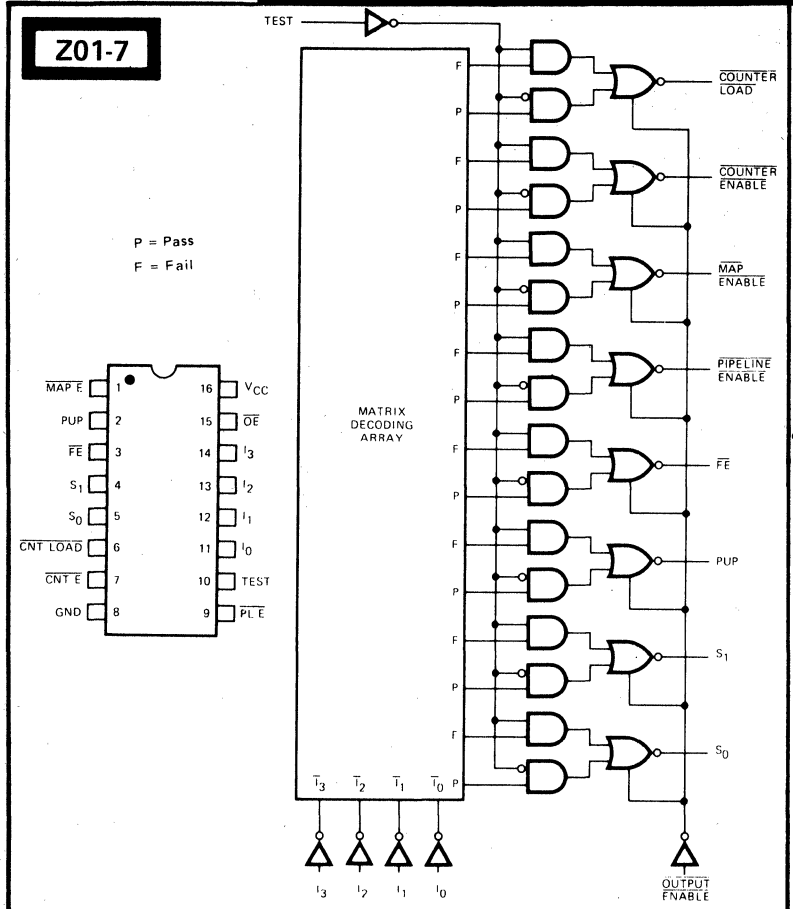

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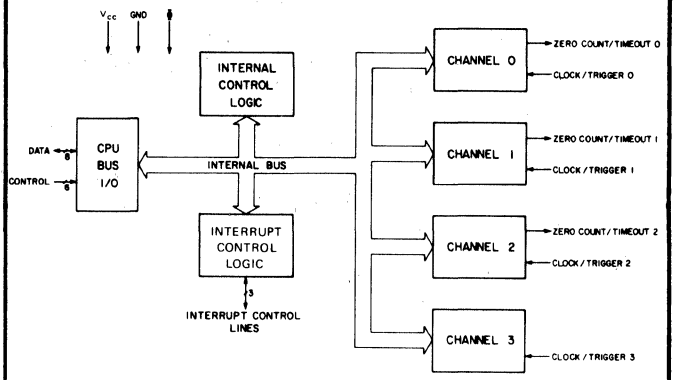

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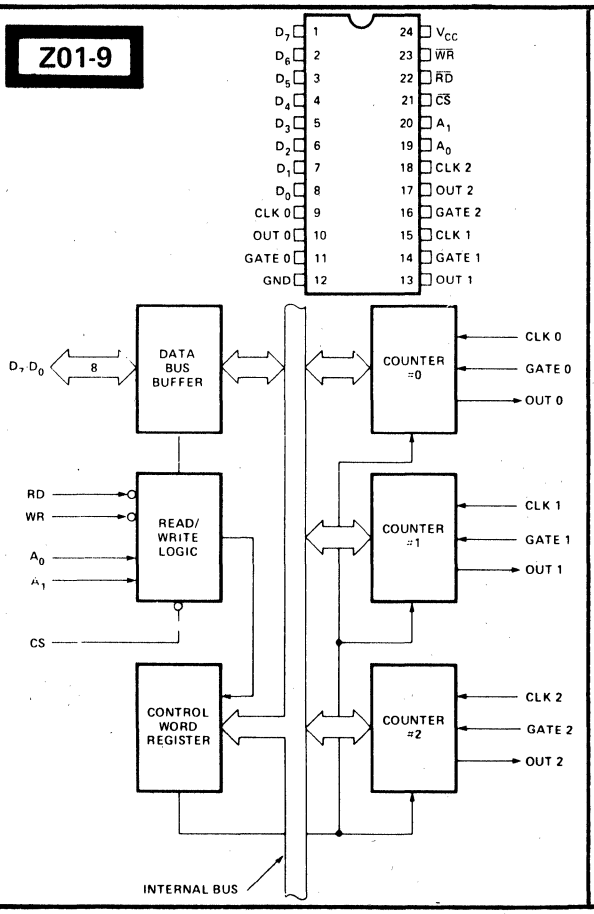

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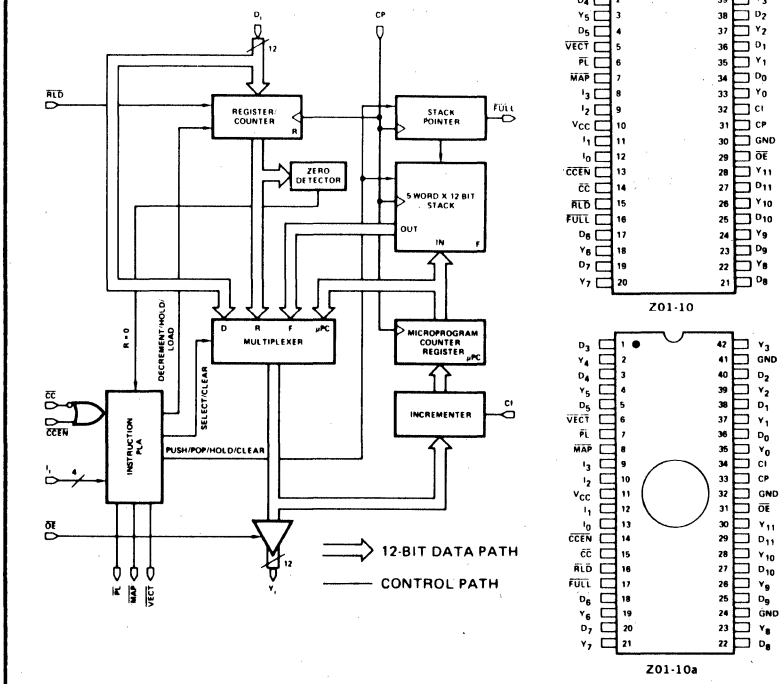
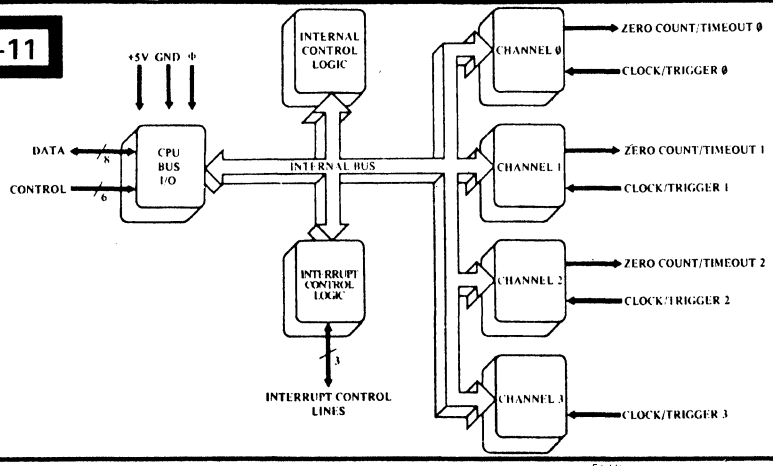
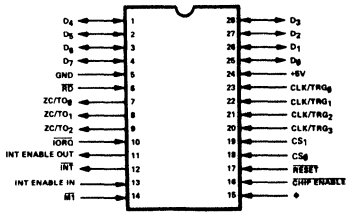


19. LOGIC/BLOCK DRAWINGS

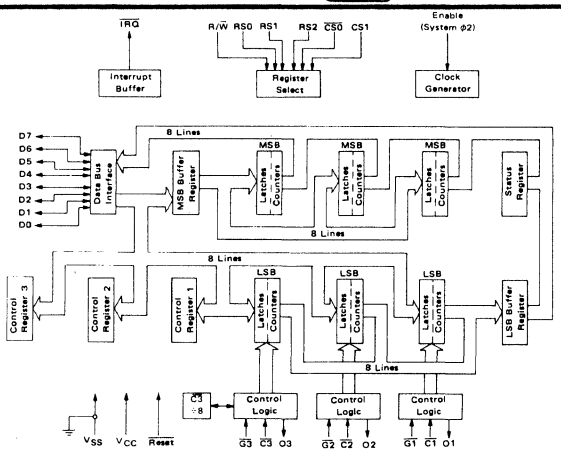
IN DRAWING NUMBER SEQUENCE

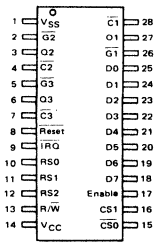
Z01-11





Z01-12





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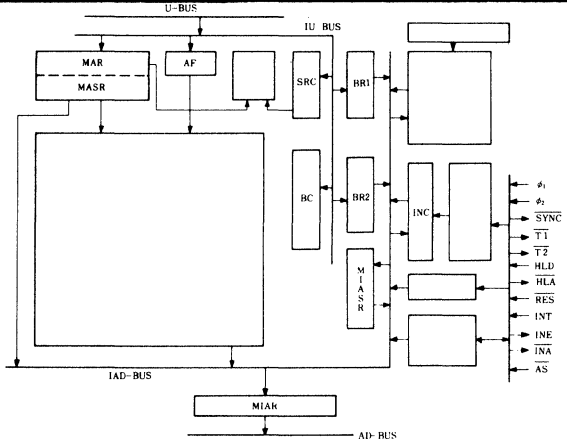
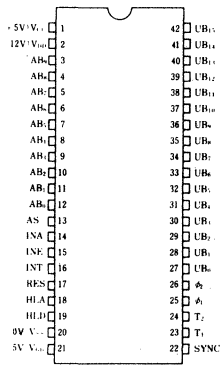
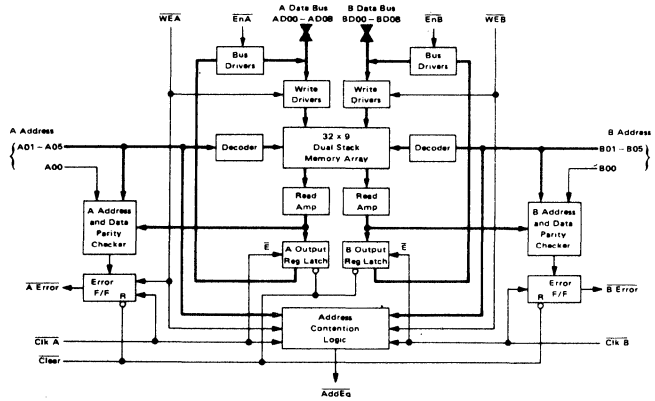
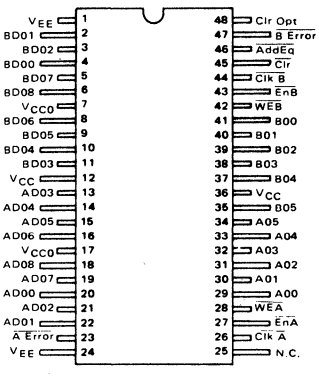




Z01-14





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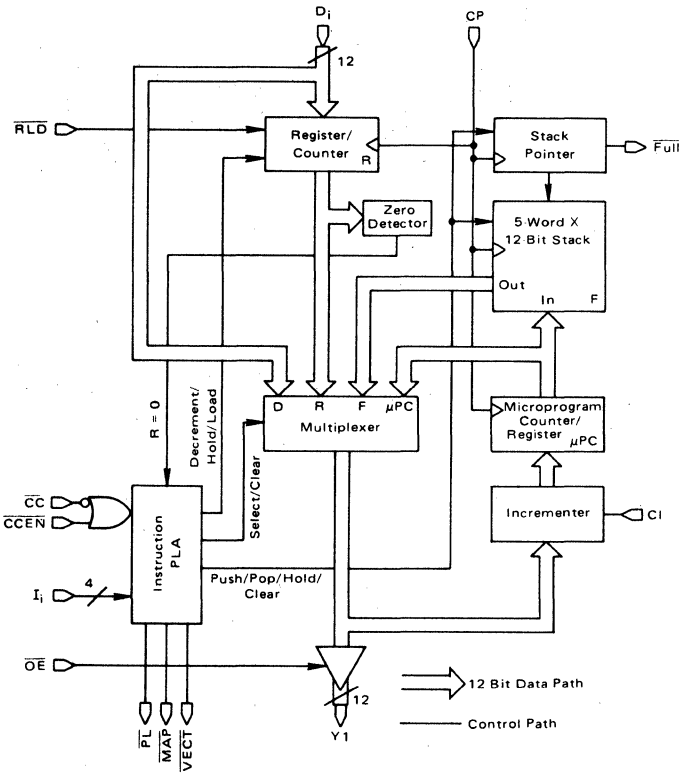
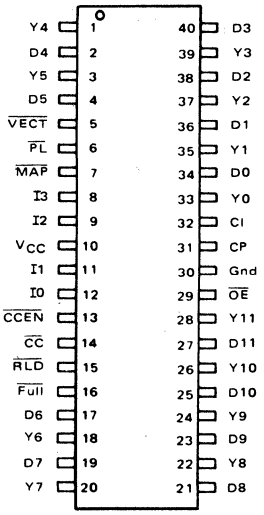
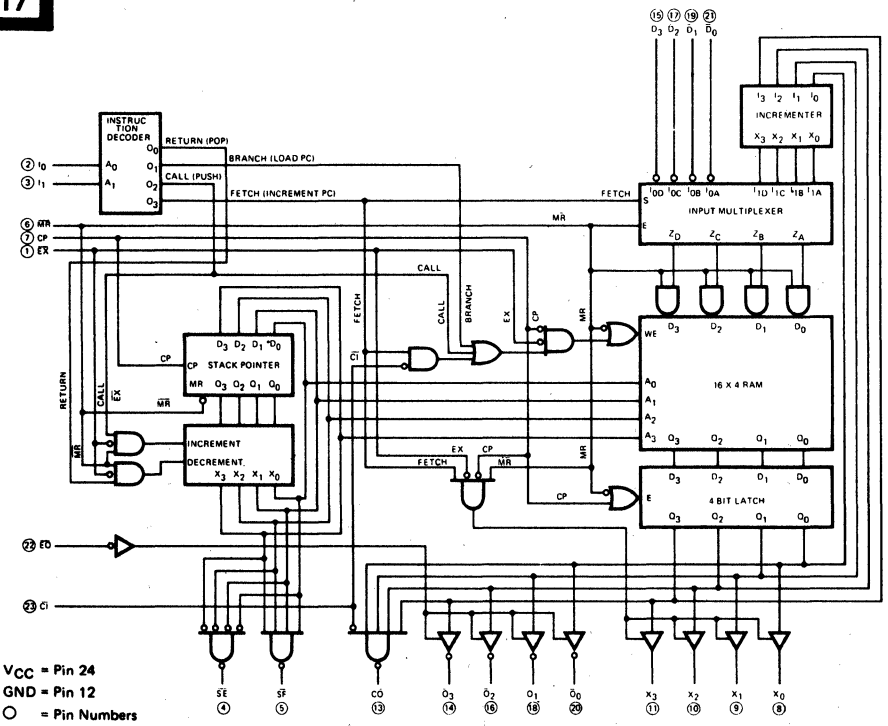
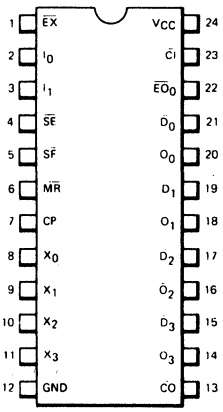

Di
12
CP
RLD
Register/ Counter
R
Stack Pointer
Full
Zero Detector
5 Word X 12 Bit Stack
Out
In
F
R = 0
Decrement/ Hold/Load
D
R
F
μPC
Multiplexer
Microprogram Counter/ Register
μPC
Select/Clear
CC
CCEN
Instruction PLA
Incrementer
CI
Ii
4
Push/Pop/Hold/ Clear
OE
12
Y1
PL
MAP
VECT
12 Bit Data Path
Control Path

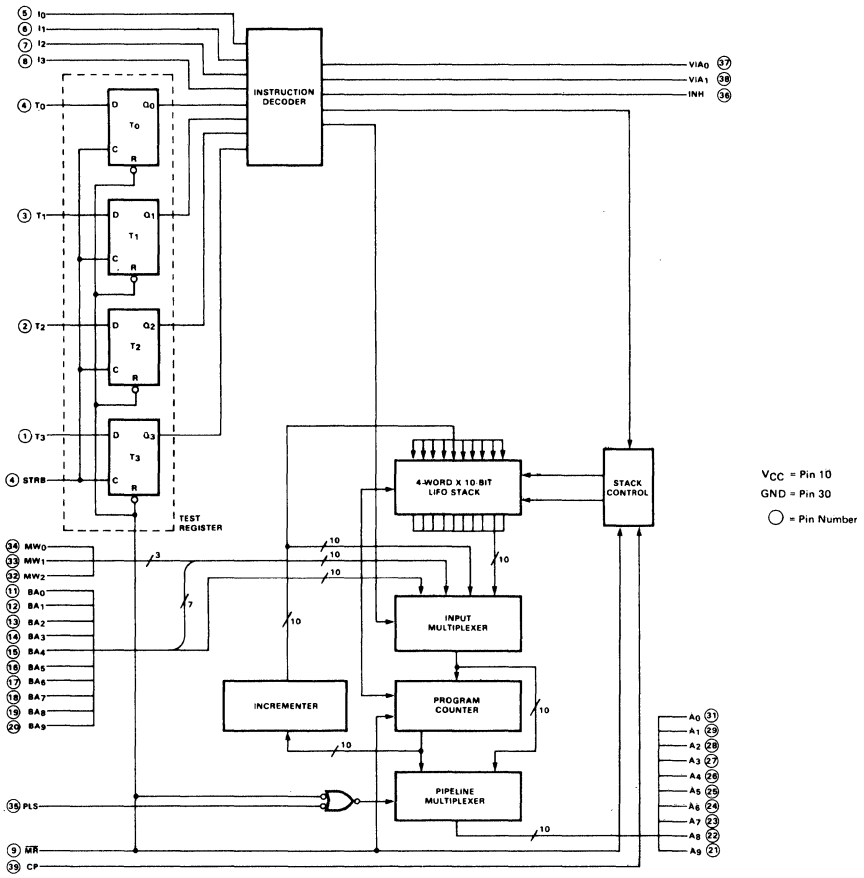

Y4 1
D4 2
Y5 3
D5 4
VECT 5
PL 6
MAP 7
I3 8
I2 9
VCC 10
I1 11
I0 12
CCEN 13
CC 14
RLD 15
Full 16
D6 17
Y6 18
D7 19
Y7 20
40 D3
39 Y3
38 D2
37 Y2
36 D1
35 Y1
34 D0
33 Y0
32 CI
31 CP
30 Gnd
29 OE
28 Y11
27 D11
26 Y10
25 D10
24 Y9
23 D9
22 Y8
21 D8

Z01-17

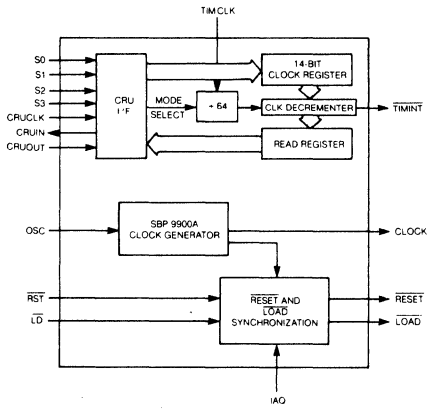

INSTRUCTION DECODER
RETURN (POP)
BRANCH (LOAD PC)
CALL (PUSH)
FETCH (INCREMENT PC)
INCREMENTER
INPUT MULTIPLEXER
STACK POINTER
INCREMENT
DECREMENT
16 X 4 RAM
4 BIT LATCH
VCC = Pin 24
GND = Pin 12
○ = Pin Numbers


1 EX
2 I0
3 I1
4 SE
5 SF
6 MR
7 CP
8 X0
9 X1
10 X2
11 X3
12 GND
VCC 24
CI 23
EO0 22
D0 21
O0 20
D1 19
O1 18
D2 17
O2 16
D3 15
O3 14
CO 13

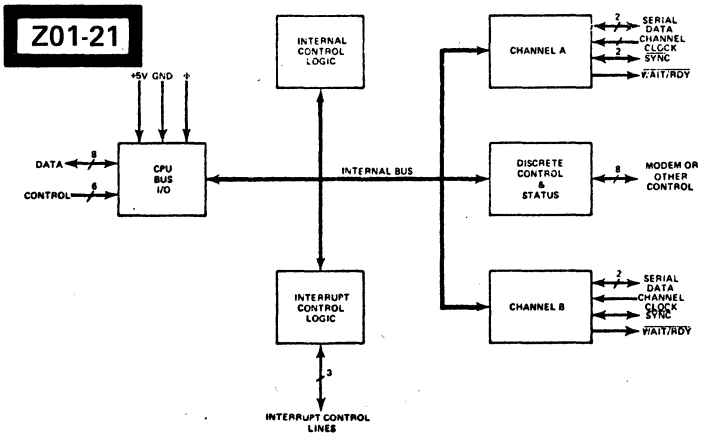
Z01-18



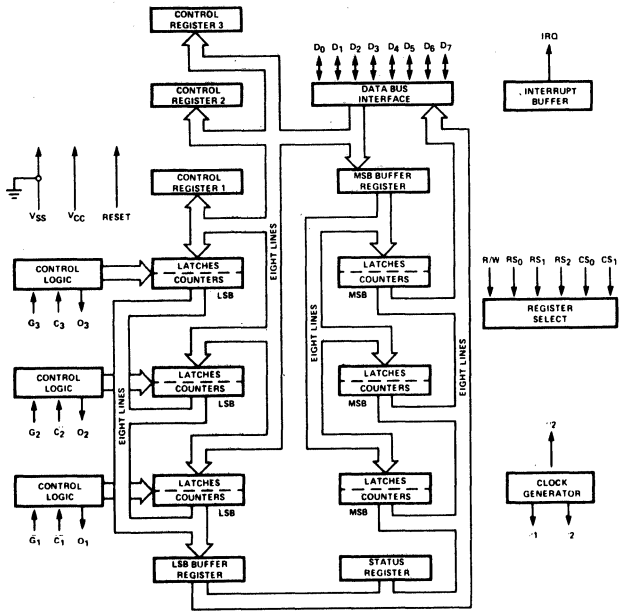
Z01-19



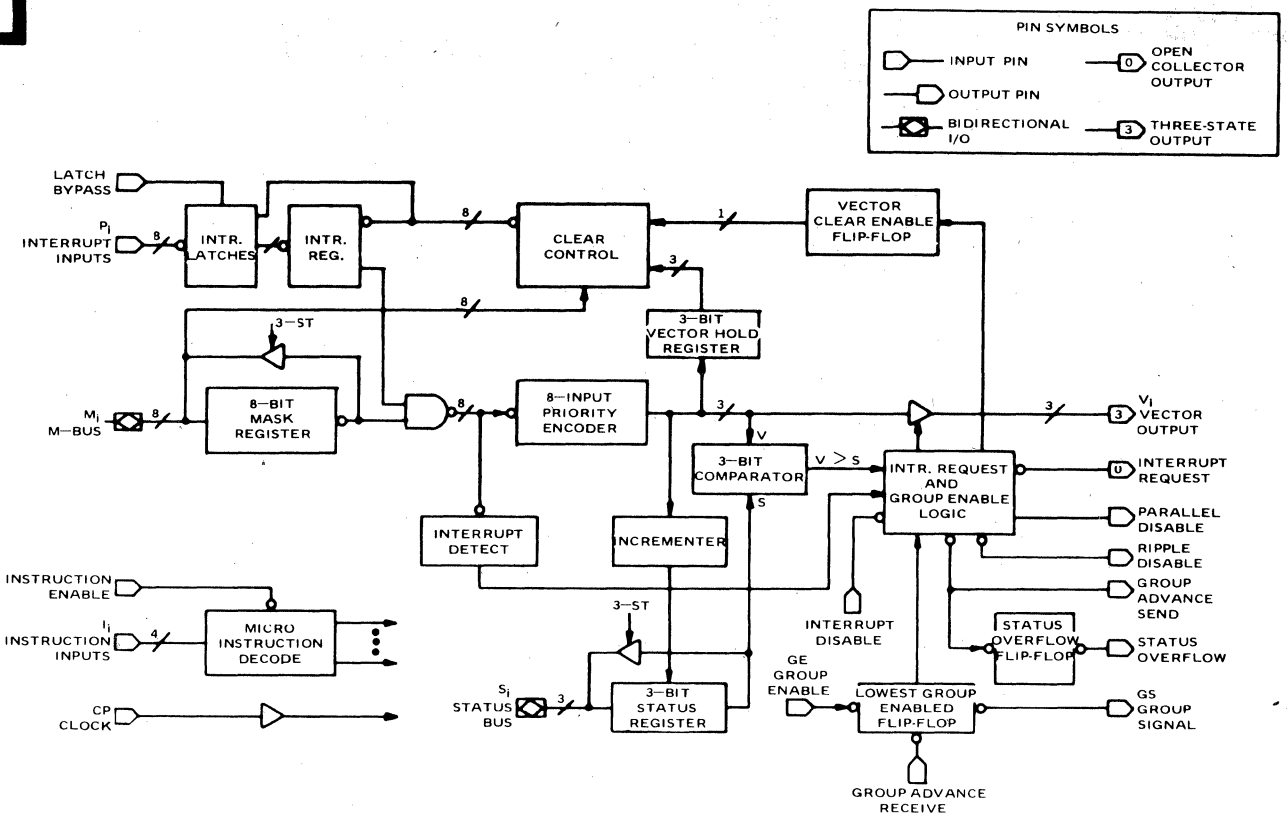
Z01-21



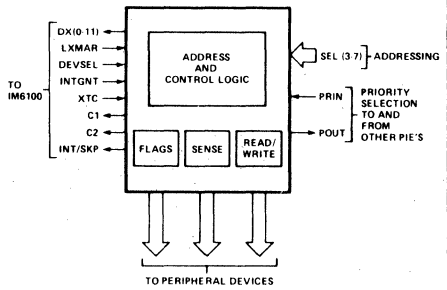
Z01-22



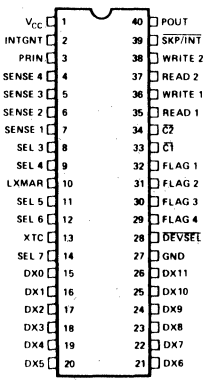
Z02-2



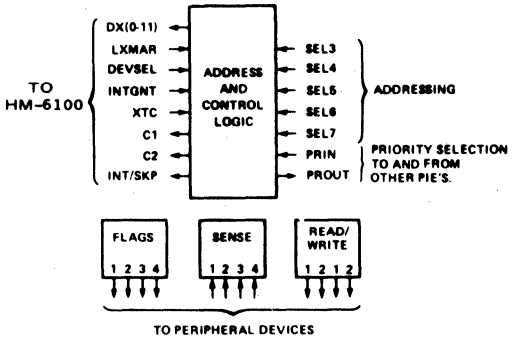
Z02-3



PIN CONFIGURATION



Z02-4



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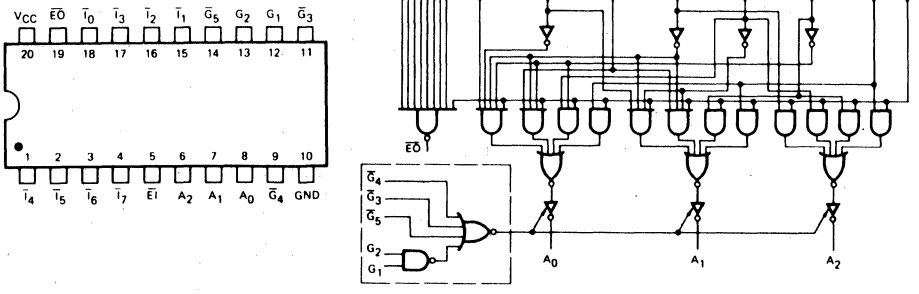
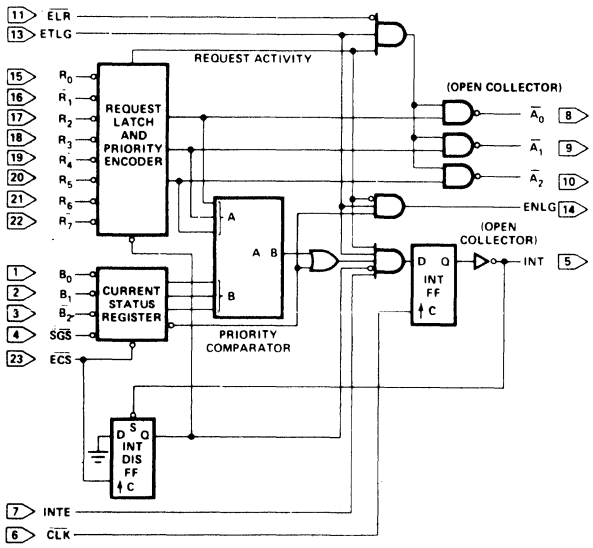
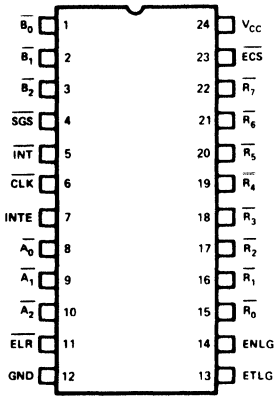
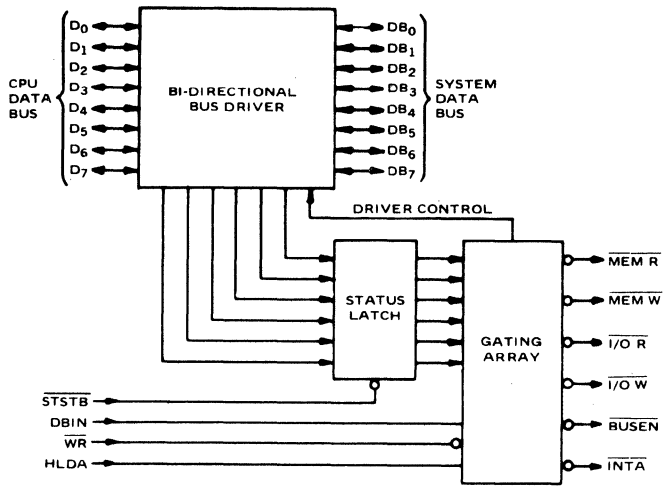


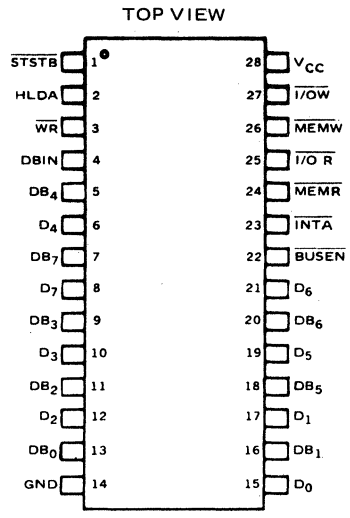
Z02-6





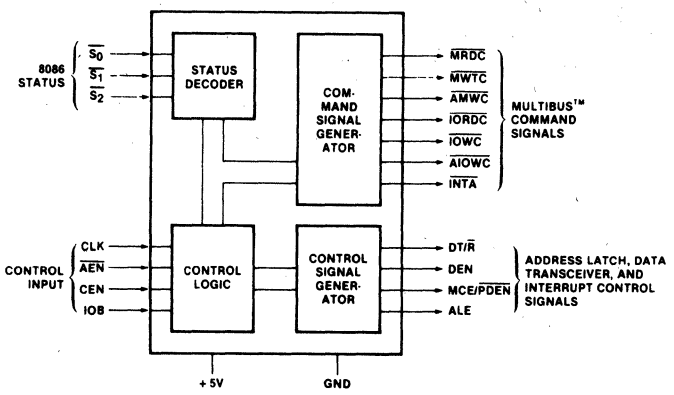
Z02-7

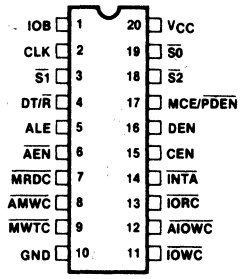




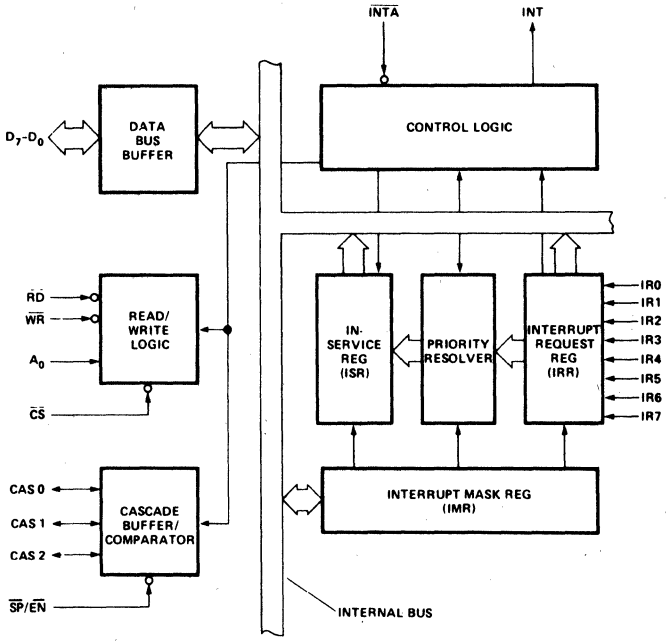
NOTE: PIN 1 IS MARKED FOR ORIENTATION

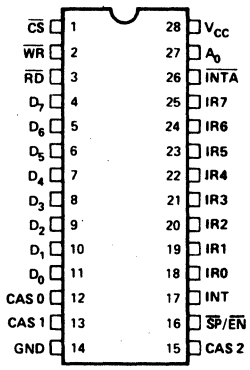
Z02-14



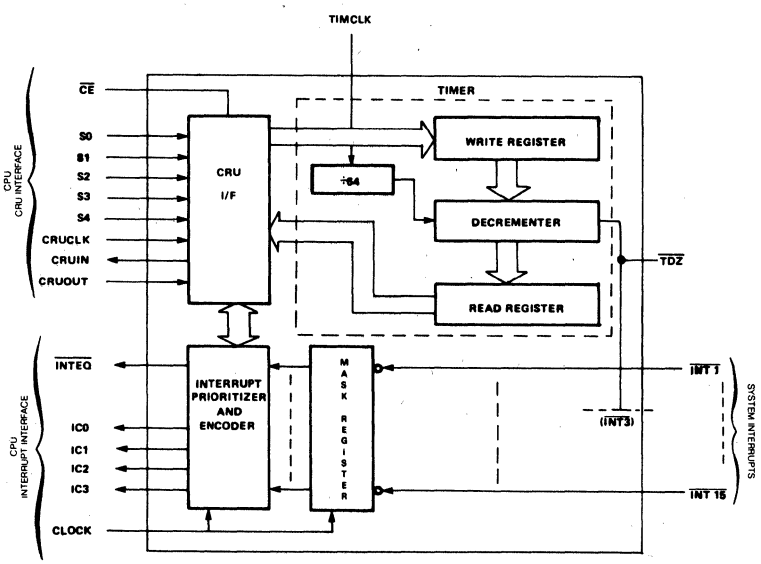


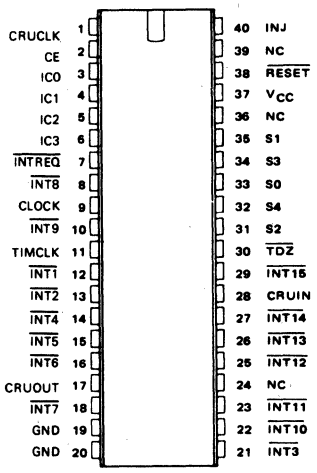
Z02-15



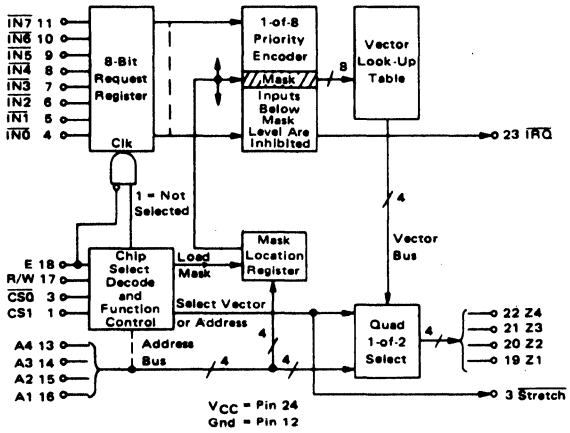


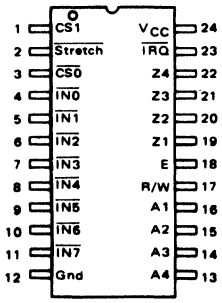
Z02-16



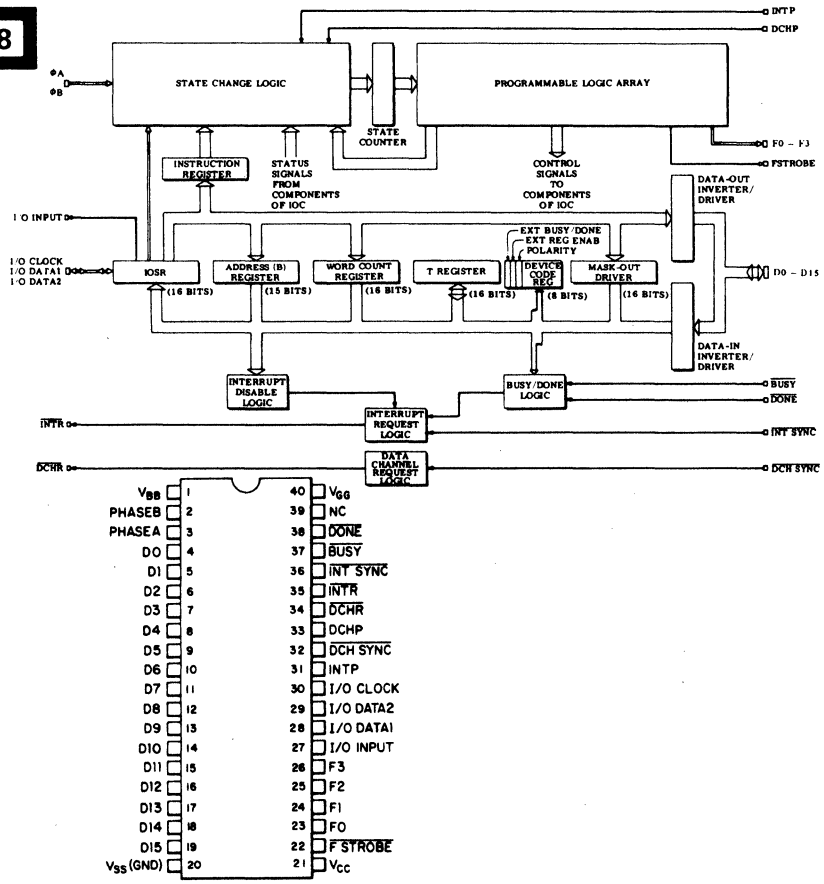


Z02-17

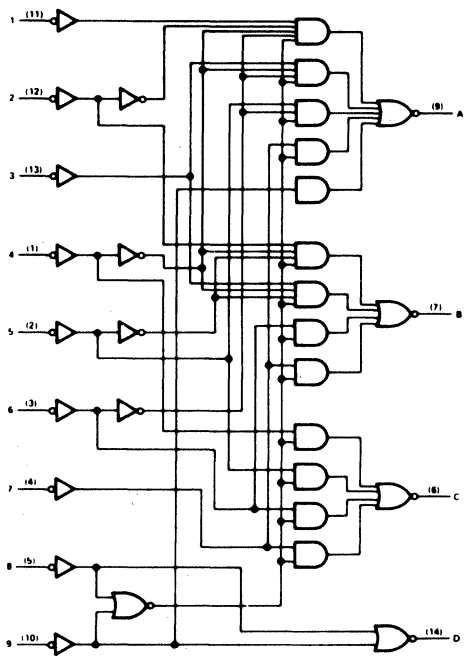


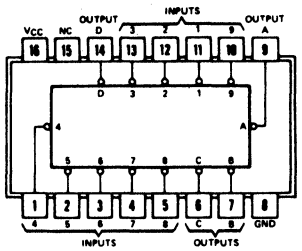


Z02-18

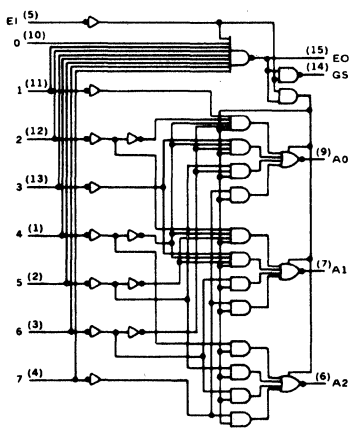


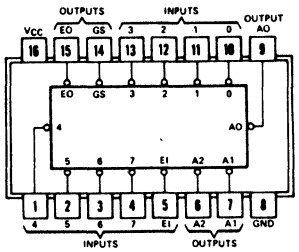
Z02-19





Z02-20

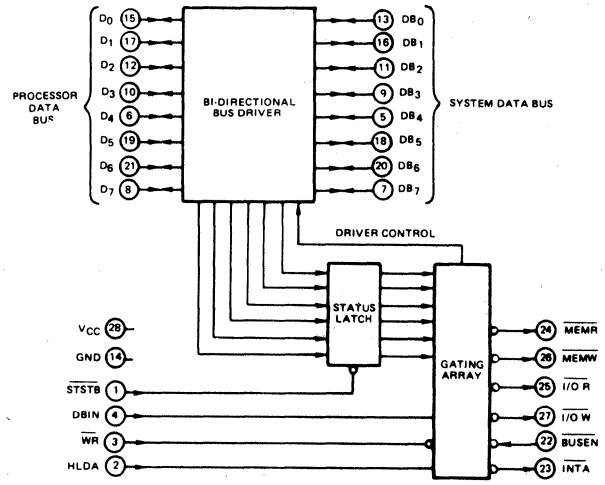




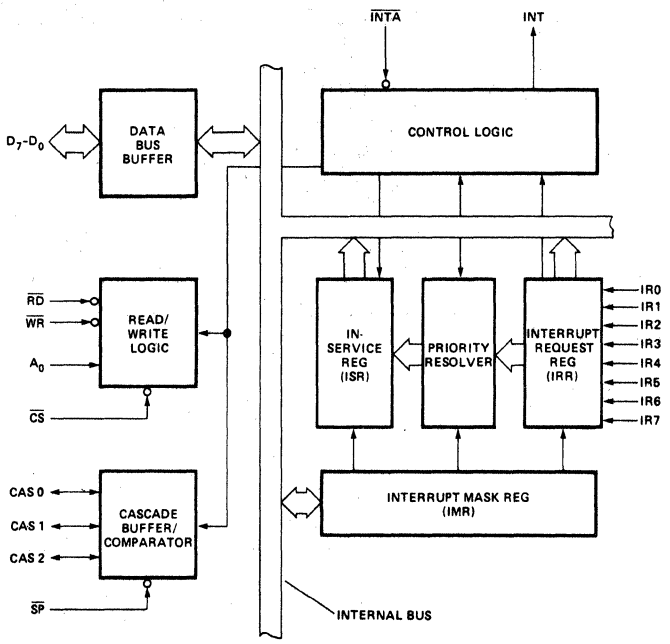
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

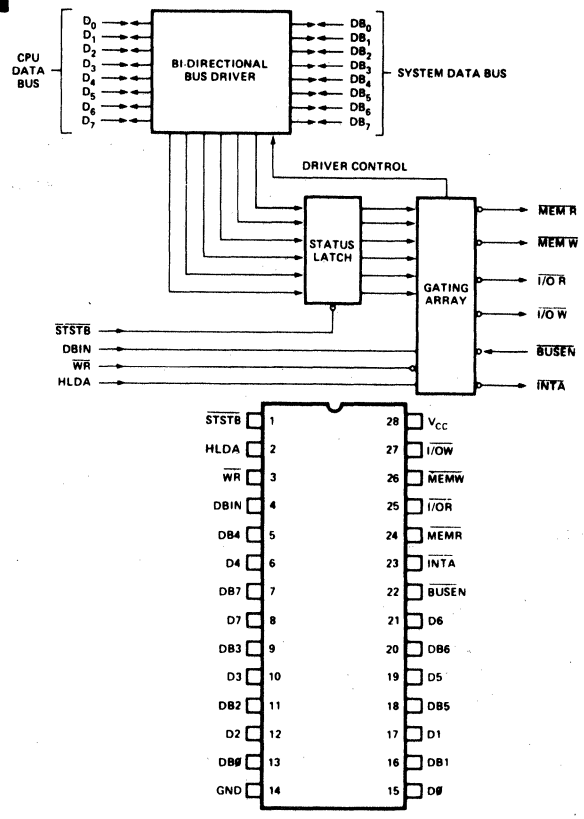
Z02-8

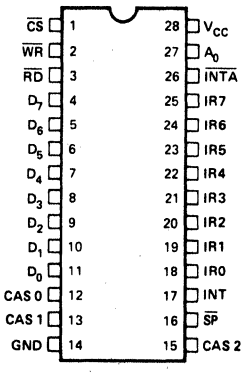


Z02-9

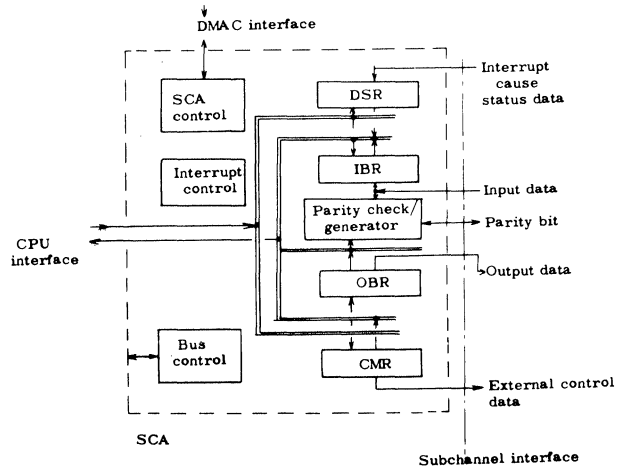


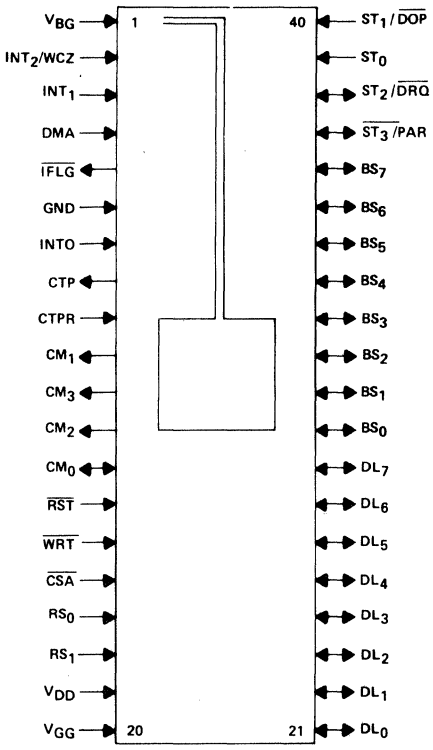
Z02-10



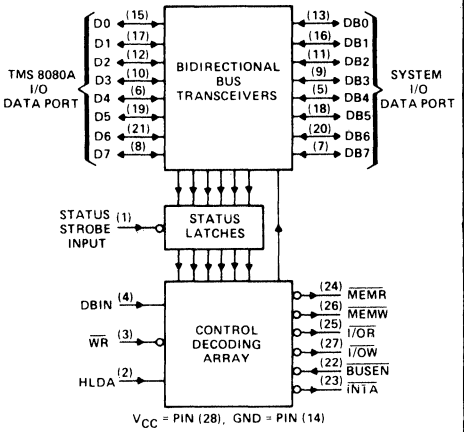


Z02-11

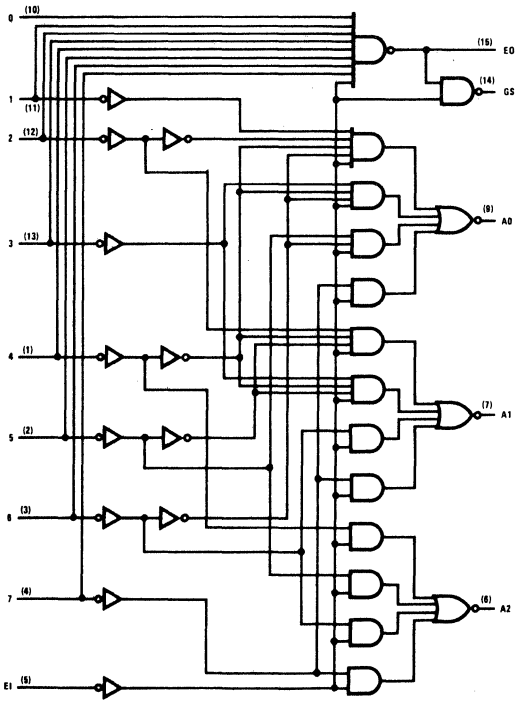




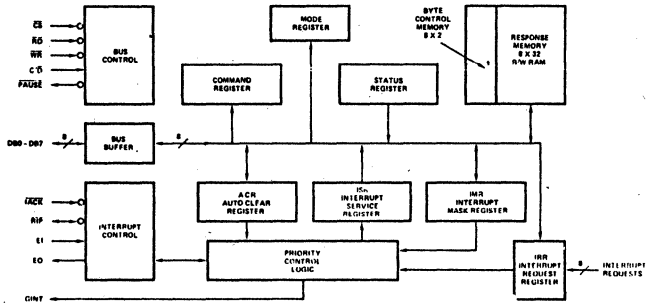
Z02-12

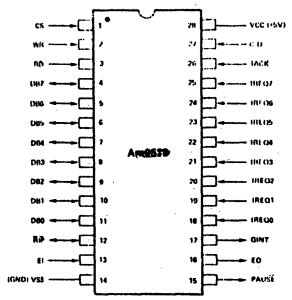


Z02-13

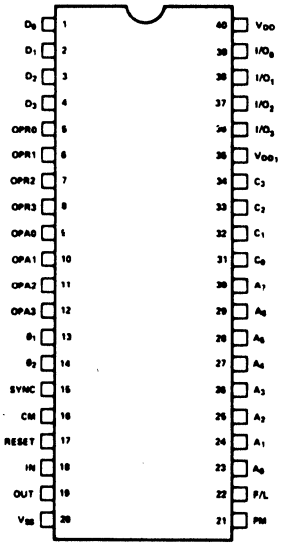


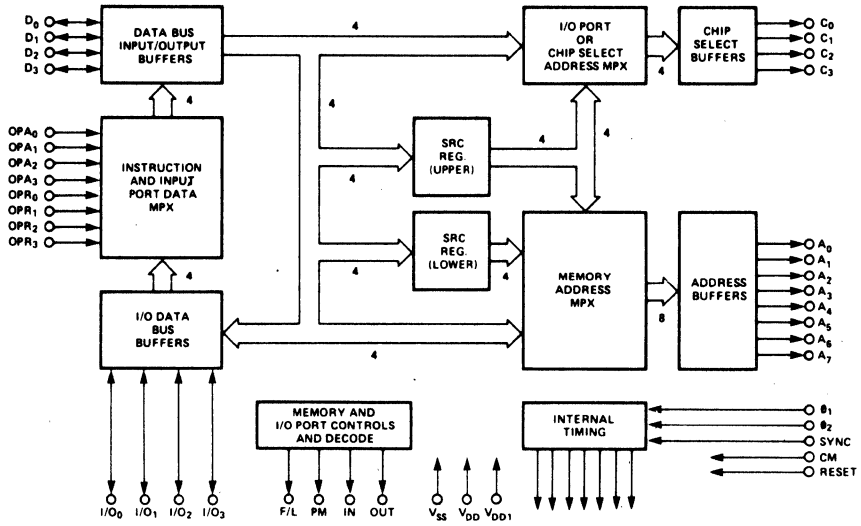
Z02-21


CS
RD
WR
C/D
PAUSE
BUS CONTROL
MODE REGISTER
BYTE CONTROL MEMORY 8 X 2
RESPONSE MEMORY 8 X 32 R/W RAM
COMMAND REGISTER
STATUS REGISTER
D80 - D87
BUS BUFFER
IACK
RIP
EI
EO
INTERRUPT CONTROL
ACR AUTO CLEAR REGISTER
ISR INTERRUPT SERVICE REGISTER
IMR INTERRUPT MASK REGISTER
PRIORITY CONTRVL LOGIC
IRR INTERRUPT REQUEST REGISTER
INTERRUPT REQUESTS
CINT

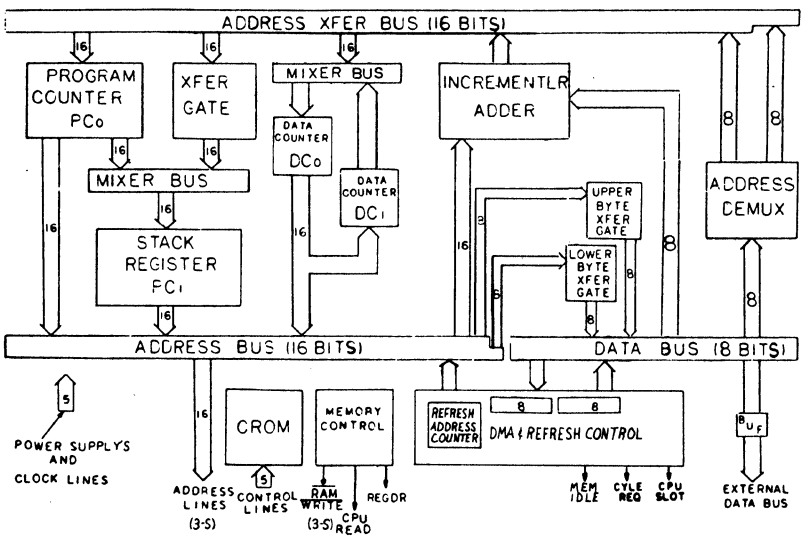

CS
WR
RD
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
RIP
EI
(GND) VSS
VCC (+5V)
IACK
IREQ7
IREQ6
IREQ5
IREQ4
IREQ3
IREQ2
IREQ1
IREQ0
CINT
EO
PAUSE

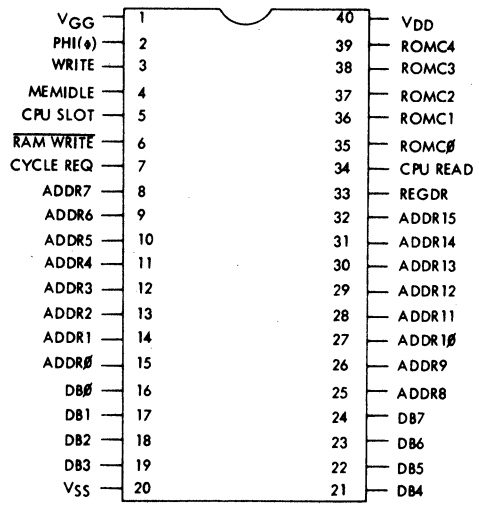
Z03-1





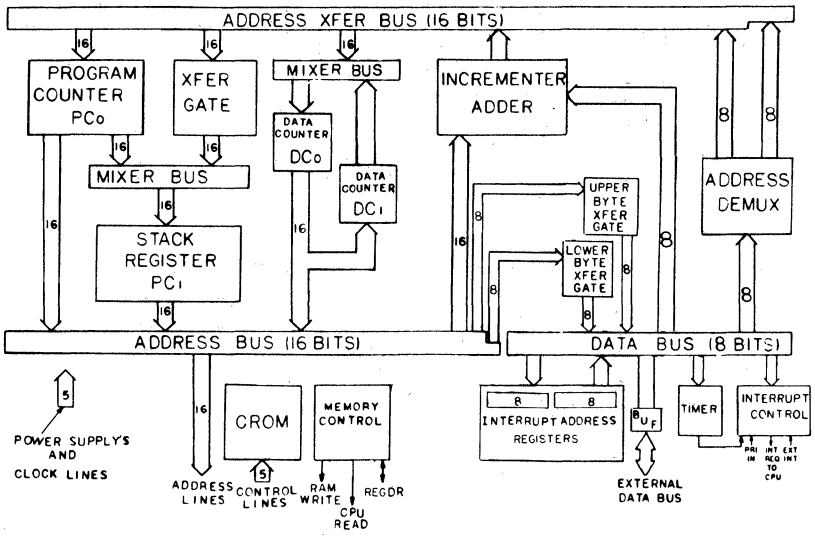
Z03-2

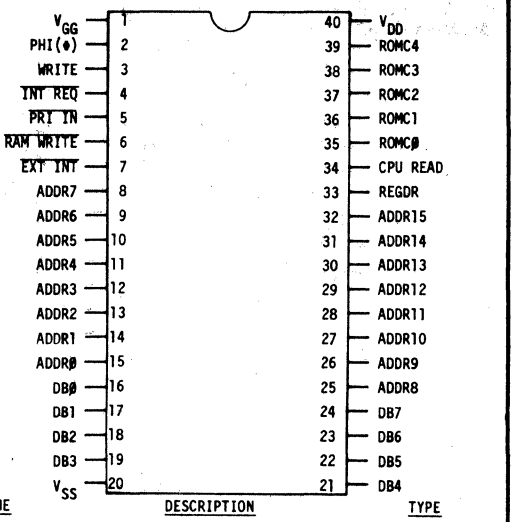




PIN NAME	DESCRIPTION	TYPE
DBØ - DB7	Data Bus Lines	Bidirectional
ADDRØ - ADDR15	Address Lines	Output
Φ, WRITE	Clock Lines	Input
MEMIDLE	DMA Timing Line	Output
CYCLE REQ	RAM Timing Line	Output
CPU SLOT	Timing Line	Output
CPU READ	RAM Timing Line	Output
REGDR	Register Drive Line	Input/Output
RAM WRITE	Write Line	Output
ROMCØ - ROMC4	Control Lines	Input
VSS, VDD, VGG	Power Lines	Input

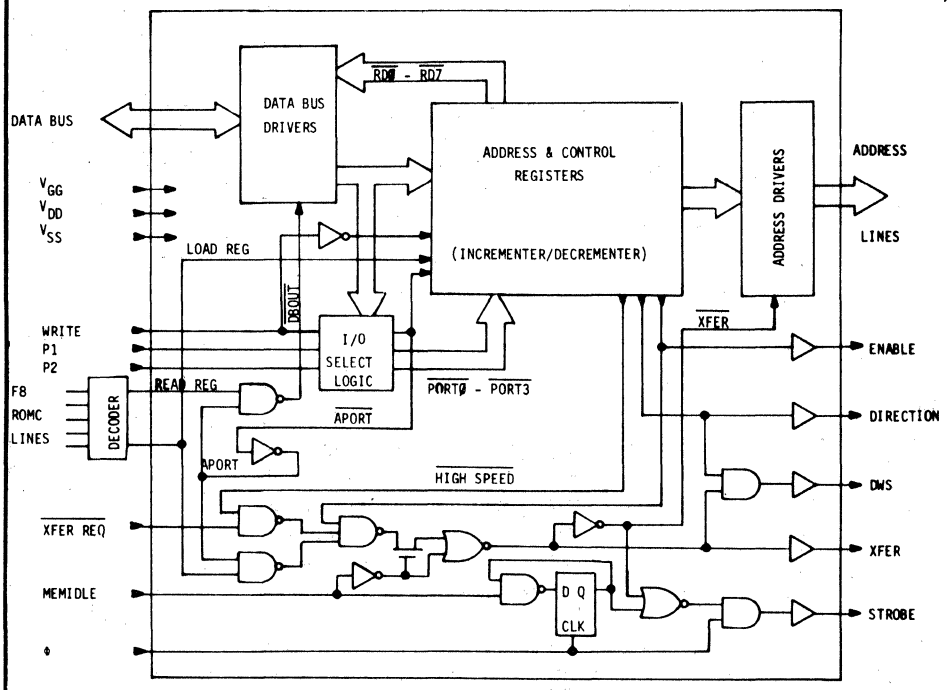
Z03-3

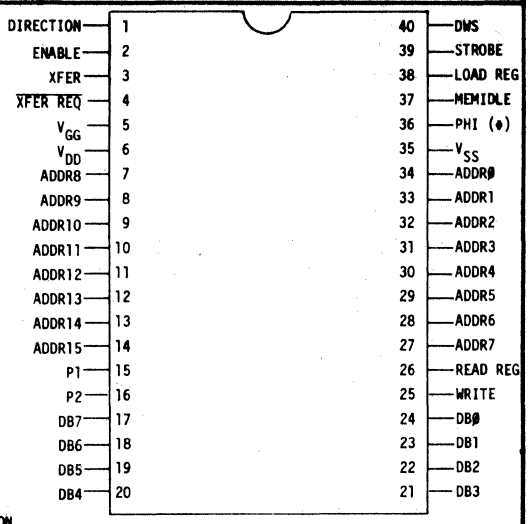




PIN NAME	DESCRIPTION	TYPE
DBØ - DB7	Data Bus Lines	Bidirectional
ADDRØ - ADDR15	Address Lines	Output
Φ, WRITE	Clock Lines	Input
INT REQ	Interrupt Request	Output
PRI IN	Priority In Line	Input
RAM WRITE	Write Line	Output
EXT INT	External Interrupt Line	Input
REGDR	Register Drive Line	Input/Output
CPU READ	CPU Read Line	Output
ROMCØ - ROMC4	Control Lines	Input
V_{SS}, V_{DD}, V_{GG}	Power Supply Lines	Input

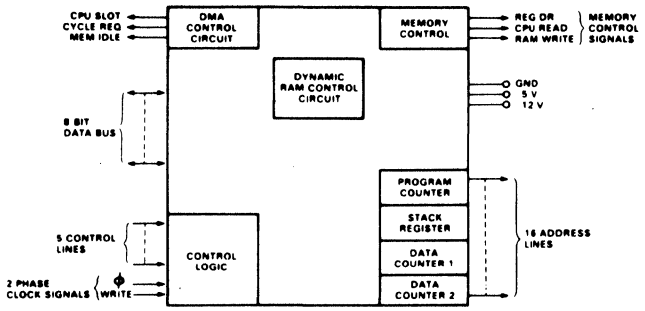
Z03-4



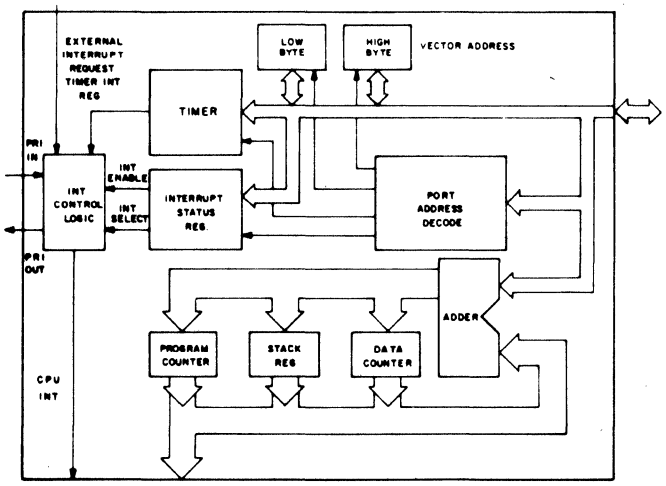


PIN NAME	DESCRIPTION	TYPE
DBØ - DB7	Data Bus Lines	Bidirectional
ADDRØ - ADDR15	Address Lines	Output
Φ, WRITE	Clock Lines	Input
LOAD REG/READ REG	Registers Load/Read Line	Input
P1, P2	Port Address Select	Input
MEMIDLE	Memory Idle Line	Input
XFER REQ	Transfer Request Line	Input
ENABLE, DIRECTION	Control Status Lines	Output
DWS, XFER	DMA Write Slot, Transfer	Output
STROBE	Output Strobe Line	Output
V_{SS}, V_{DD}, V_{GG}	Power Lines	Input

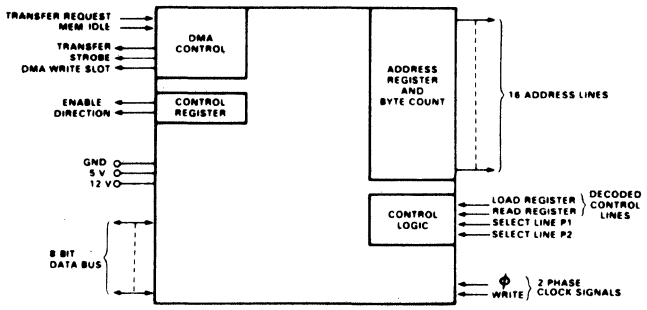
Z03-5



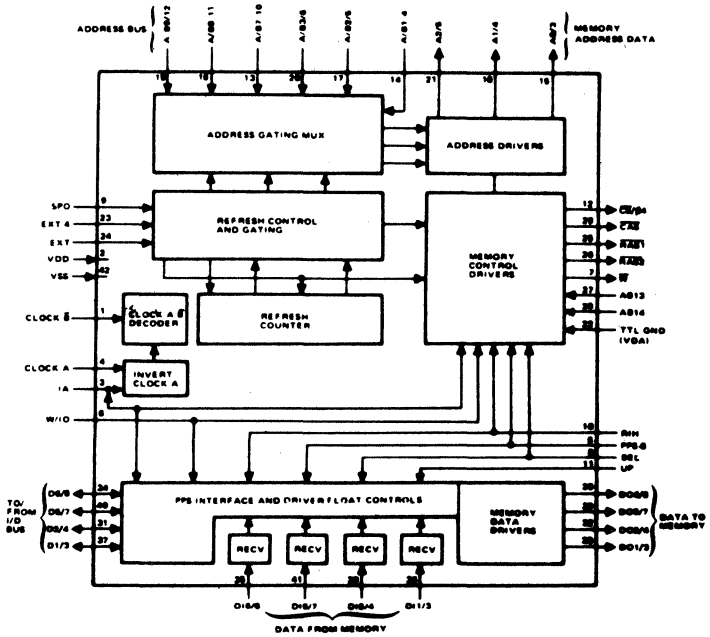
Z03-6



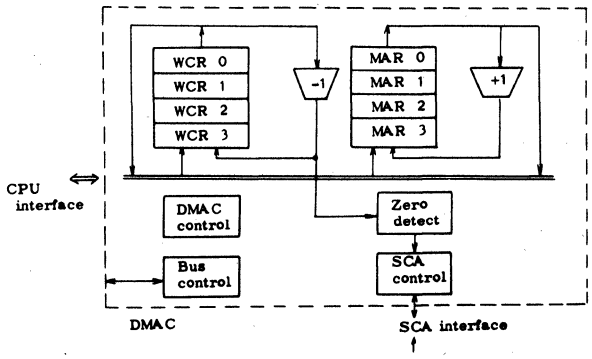
Z03-7

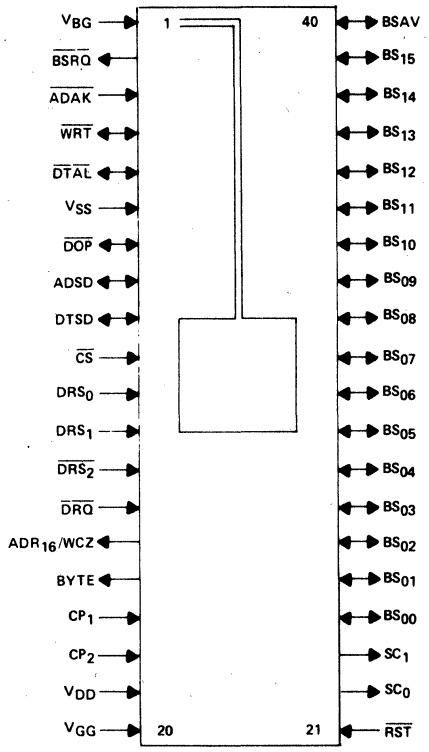


Z03-8

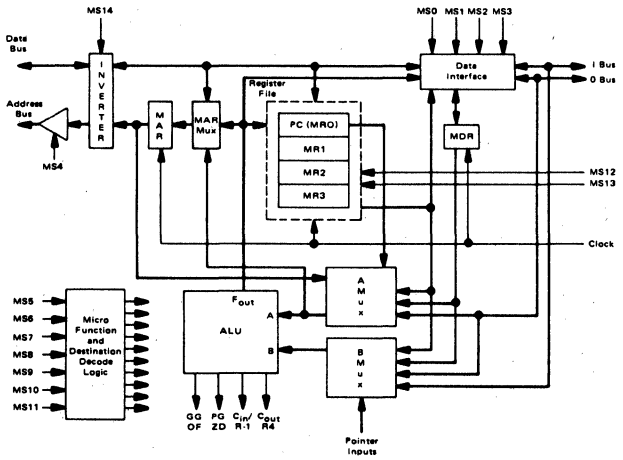


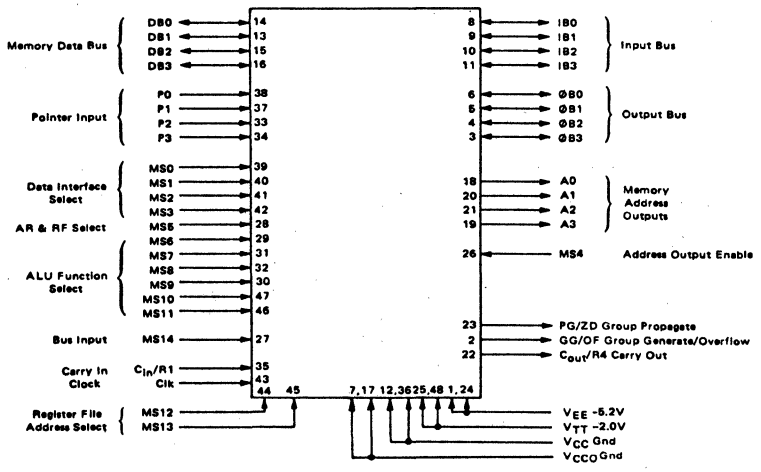
Z03-9


WCR 0
WCR 1
WCR 2
WCR 3
-1
MAR 0
MAR 1
MAR 2
MAR 3
+1
CPU interface
DMAC control
Zero detect
Bus control
SCA control
DMAC
SCA interface

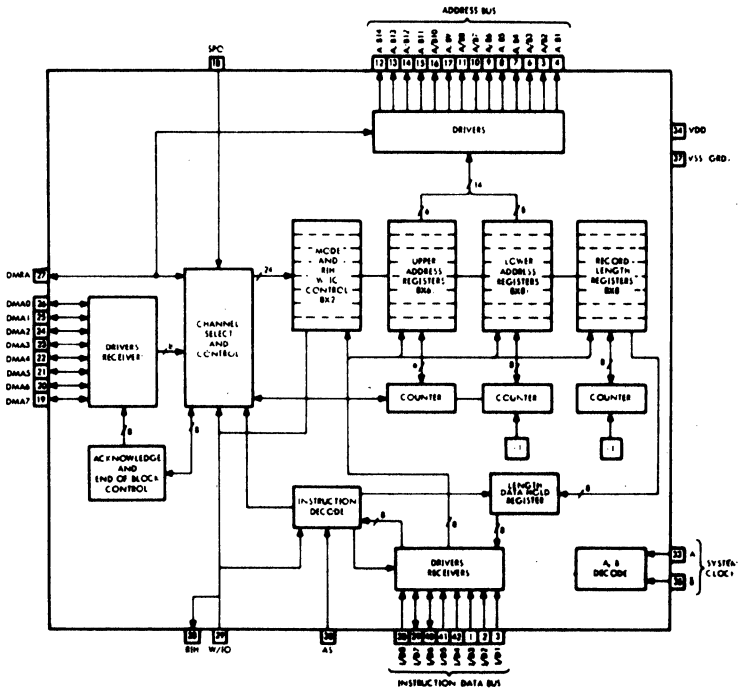

V_{BG}
$\overline{BSRQ}$
$\overline{ADAK}$
$\overline{WRT}$
$\overline{DTAL}$
V_{SS}
$\overline{DOP}$
ADSD
DTSD
$\overline{CS}$
DRS_0
DRS_1
$\overline{DRS_2}$
$\overline{DRQ}$
ADR_{16}/WCZ
BYTE
CP_1
CP_2
V_{DD}
V_{GG}
1
20
21
40
BSAV
BS_{15}
BS_{14}
BS_{13}
BS_{12}
BS_{11}
BS_{10}
BS_{09}
BS_{08}
BS_{07}
BS_{06}
BS_{05}
BS_{04}
BS_{03}
BS_{02}
BS_{01}
BS_{00}
SC_1
SC_0
$\overline{RST}$

Z03-10

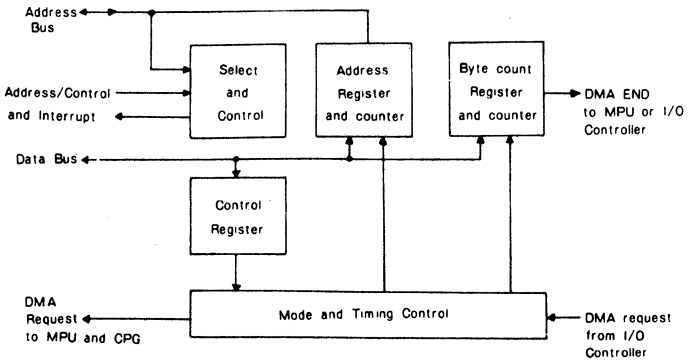

MS14
Data Bus
Address Bus
MS4
INVERTER
MAR
MAR Mux
Register File
PC (MRO)
MR1
MR2
MR3
MS0 MS1 MS2 MS3
Data Interface
I Bus
O Bus
MDR
MS12
MS13
Clock
MS5
MS6
MS7
MS8
MS9
MS10
MS11
Micro Function and Destination Decode Logic
ALU
F_{out}
A
B
AMux
BMux
GG OF
PG ZD
C_{in}/ R-1
C_{out} R4
Pointer Inputs

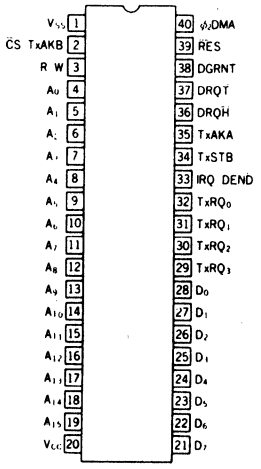

Memory Data Bus
DB0
DB1
DB2
DB3
Pointer Input
P0
P1
P2
P3
Data Interface Select
MS0
MS1
MS2
MS3
AR & RF Select
MS5
ALU Function Select
MS6
MS7
MS8
MS9
MS10
MS11
Bus Input
MS14
Carry In Clock
C_{in}/R1
Clk
Register File Address Select
MS12
MS13
14
13
15
16
38
37
33
34
39
40
41
42
28
29
31
32
30
47
46
27
35
43
44
45
7,17
12,36
25,48
1,24
8
9
10
11
6
5
4
3
18
20
21
19
26
23
2
22
IB0
IB1
IB2
IB3
Input Bus
ØB0
ØB1
ØB2
ØB3
Output Bus
A0
A1
A2
A3
Memory Address Outputs
MS4
Address Output Enable
PG/ZD Group Propagate
GG/OF Group Generate/Overflow
C_{out}/R4 Carry Out
V_{EE} -5.2V
V_{TT} -2.0V
V_{CC} Gnd
V_{CCO} Gnd

Z03-11

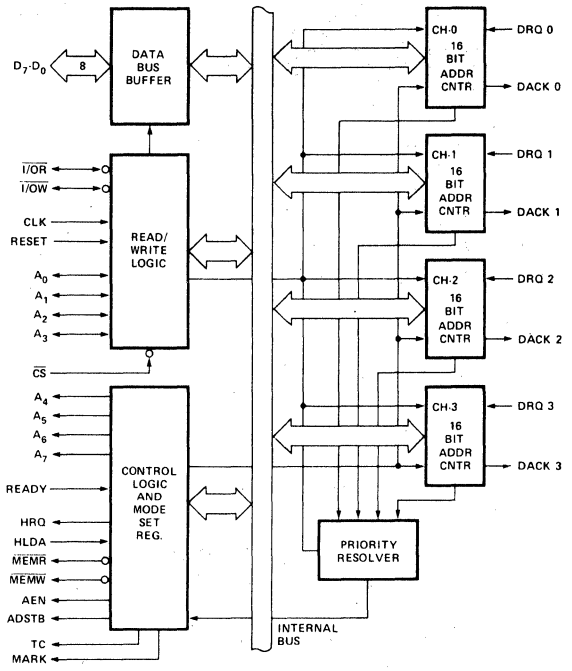

ADDRESS BUS
DRIVERS
VDD
VSS GND
DMAREQ
DRIVERS RECEIVER
CHANNEL SELECT AND CONTROL
MODE AND BIH W/IC CONTROL 8X2
UPPER ADDRESS REGISTERS 8X8
LOWER ADDRESS REGISTERS 8X8
RECORD LENGTH REGISTERS 8X8
COUNTER
COUNTER
COUNTER
ACKNOWLEDGE AND END OF BLOCK CONTROL
INSTRUCTION DECODE
DRIVERS RECEIVERS
A, B DECODE
SYSTEM CLOCK
BIH
W/IO
A5
INSTRUCTION DATA BUS

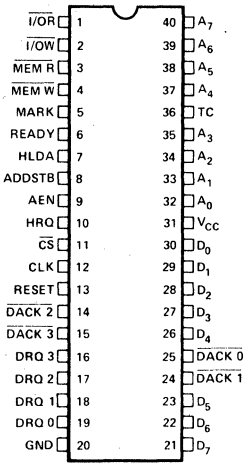
Z03-12


Address Bus
Address/Control and Interrupt
Data Bus
Select and Control
Address Register and counter
Byte count Register and counter
DMA END to MPU or I/O Controller
Control Register
DMA Request to MPU and CPG
Mode and Timing Control
DMA request from I/O Controller

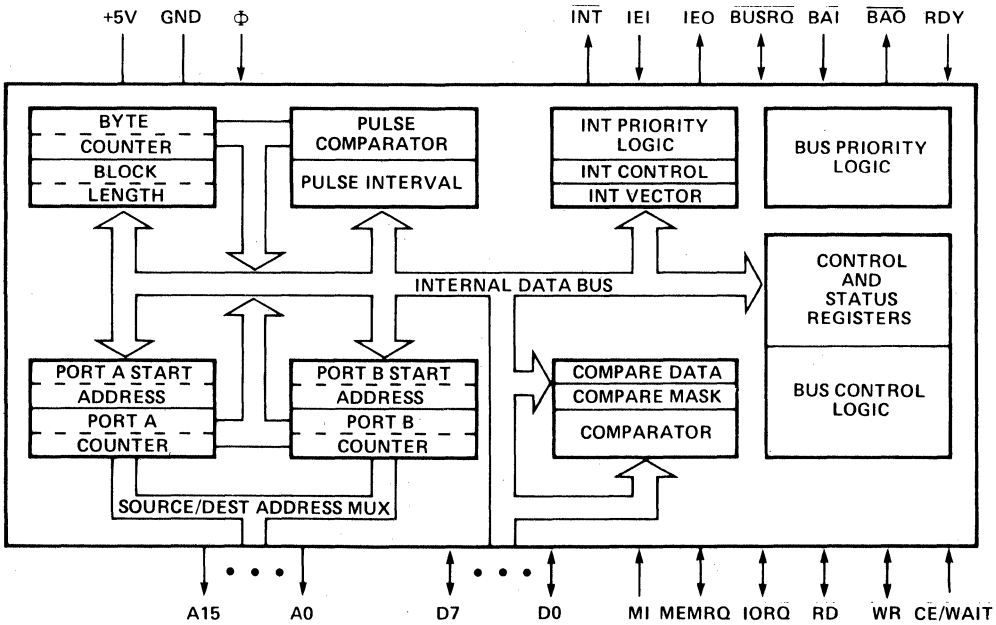

VSS 1
CS TxAKB 2
R W 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
A9 13
A10 14
A11 15
A12 16
A13 17
A14 18
A15 19
VCC 20
40 ΦDMA
39 RES
38 DGRNT
37 DRQT
36 DRQH
35 TxAKA
34 TxSTB
33 IRQ DEND
32 TxRQ0
31 TxRQ1
30 TxRQ2
29 TxRQ3
28 D0
27 D1
26 D2
25 D3
24 D4
23 D5
22 D6
21 D7

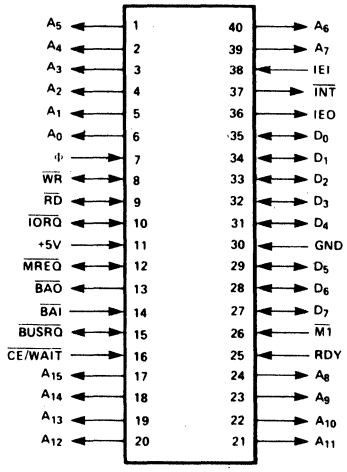
Z03-13


DATA BUS BUFFER
READ/ WRITE LOGIC
CONTROL LOGIC AND MODE SET REG.
CH-0 16 BIT ADDR CNTR
CH-1 16 BIT ADDR CNTR
CH-2 16 BIT ADDR CNTR
CH-3 16 BIT ADDR CNTR
PRIORITY RESOLVER
INTERNAL BUS
D7-D0
8
I/OR
I/OW
CLK
RESET
A0
A1
A2
A3
CS
A4
A5
A6
A7
READY
HRQ
HLDA
MEMR
MEMW
AEN
ADSTB
TC
MARK
DRQ 0
DACK 0
DRQ 1
DACK 1
DRQ 2
DACK 2
DRQ 3
DACK 3

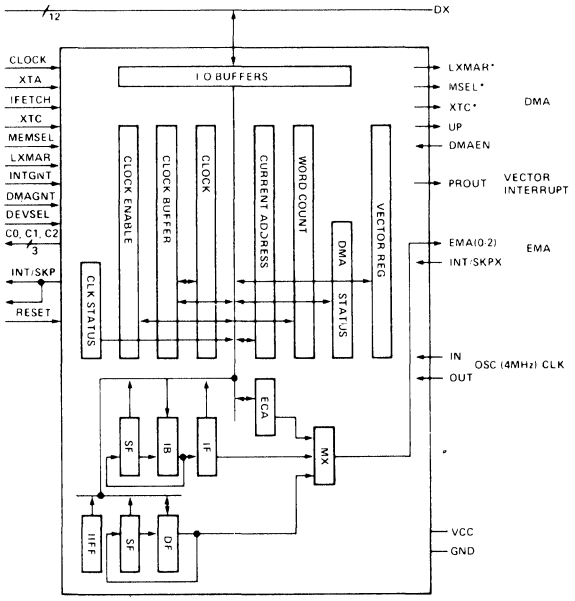

I/OR 1
I/OW 2
MEM R 3
MEM W 4
MARK 5
READY 6
HLDA 7
ADDSTB 8
AEN 9
HRQ 10
CS 11
CLK 12
RESET 13
DACK 2 14
DACK 3 15
DRQ 3 16
DRQ 2 17
DRQ 1 18
DRQ 0 19
GND 20
40 A7
39 A6
38 A5
37 A4
36 TC
35 A3
34 A2
33 A1
32 A0
31 VCC
30 D0
29 D1
28 D2
27 D3
26 D4
25 DACK 0
24 DACK 1
23 D5
22 D6
21 D7

Z03-14

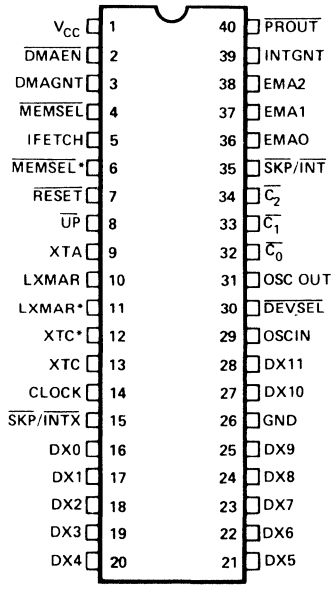

+5V
GND
Φ
INT
IEI
IEO
BUSRQ
BAI
BAO
RDY
BYTE COUNTER
BLOCK LENGTH
PULSE COMPARATOR
PULSE INTERVAL
INT PRIORITY LOGIC
INT CONTROL
INT VECTOR
BUS PRIORITY LOGIC
INTERNAL DATA BUS
CONTROL AND STATUS REGISTERS
PORT A START ADDRESS
PORT A COUNTER
PORT B START ADDRESS
PORT B COUNTER
COMPARE DATA
COMPARE MASK
COMPARATOR
BUS CONTROL LOGIC
SOURCE/DEST ADDRESS MUX
A15
A0
D7
D0
MI
MEMRQ
IORQ
RD
WR
CE/WAIT


A5 1
A4 2
A3 3
A2 4
A1 5
A0 6
Φ 7
WR 8
RD 9
IORQ 10
+5V 11
MREQ 12
BAO 13
BAI 14
BUSRQ 15
CE/WAIT 16
A15 17
A14 18
A13 19
A12 20
40 A6
39 A7
38 IEI
37 INT
36 IEO
35 D0
34 D1
33 D2
32 D3
31 D4
30 GND
29 D5
28 D6
27 D7
26 M1
25 RDY
24 A8
23 A9
22 A10
21 A11

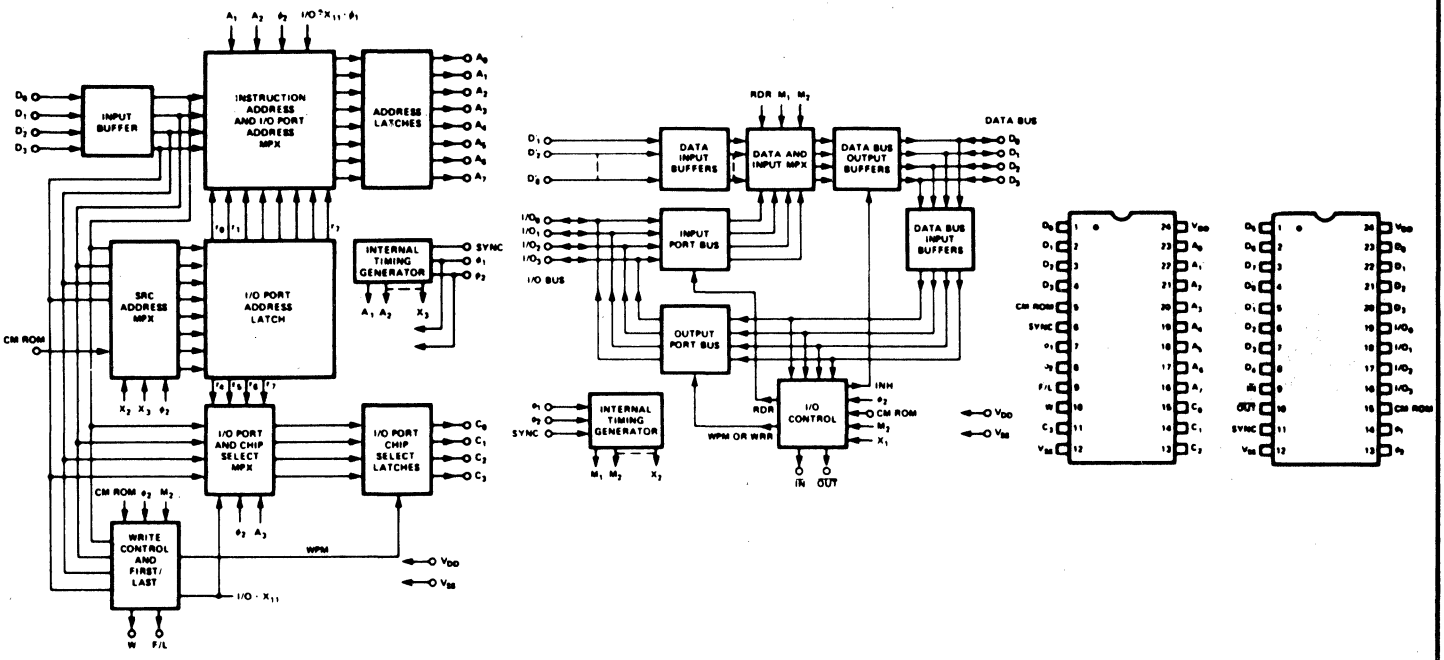
Z03-15



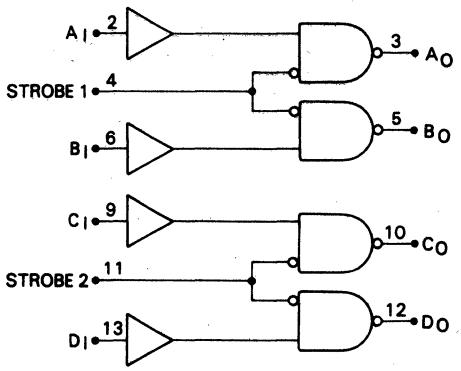
PIN CONFIGURATION



Z03-16

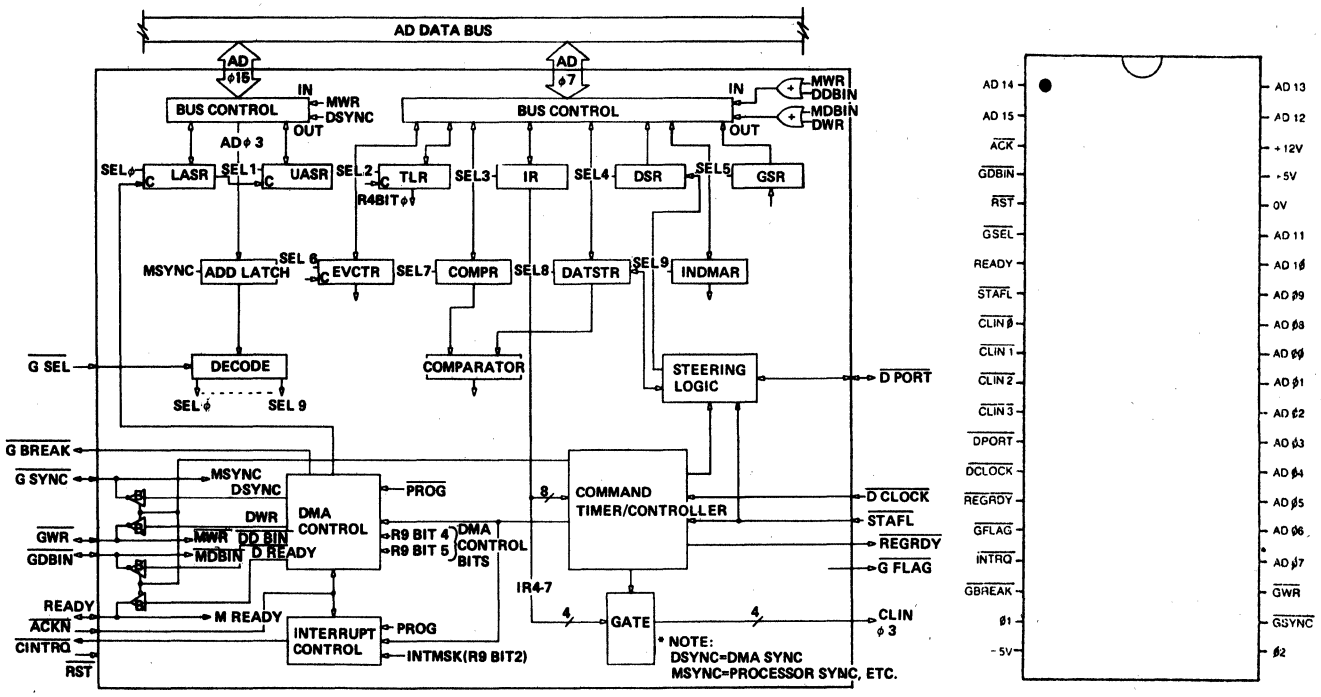


Z03-17

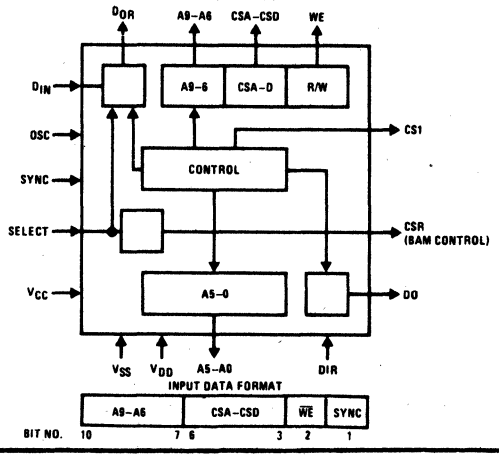


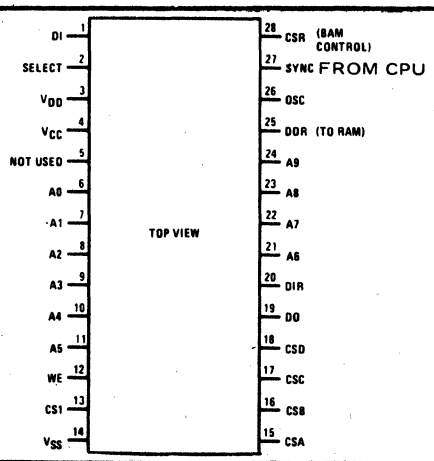
PIN 1 = V_{CC} A
PIN 7 = GND
PIN 8 = V_{EE}
PIN 14 = V_{CC} D

Z03-18

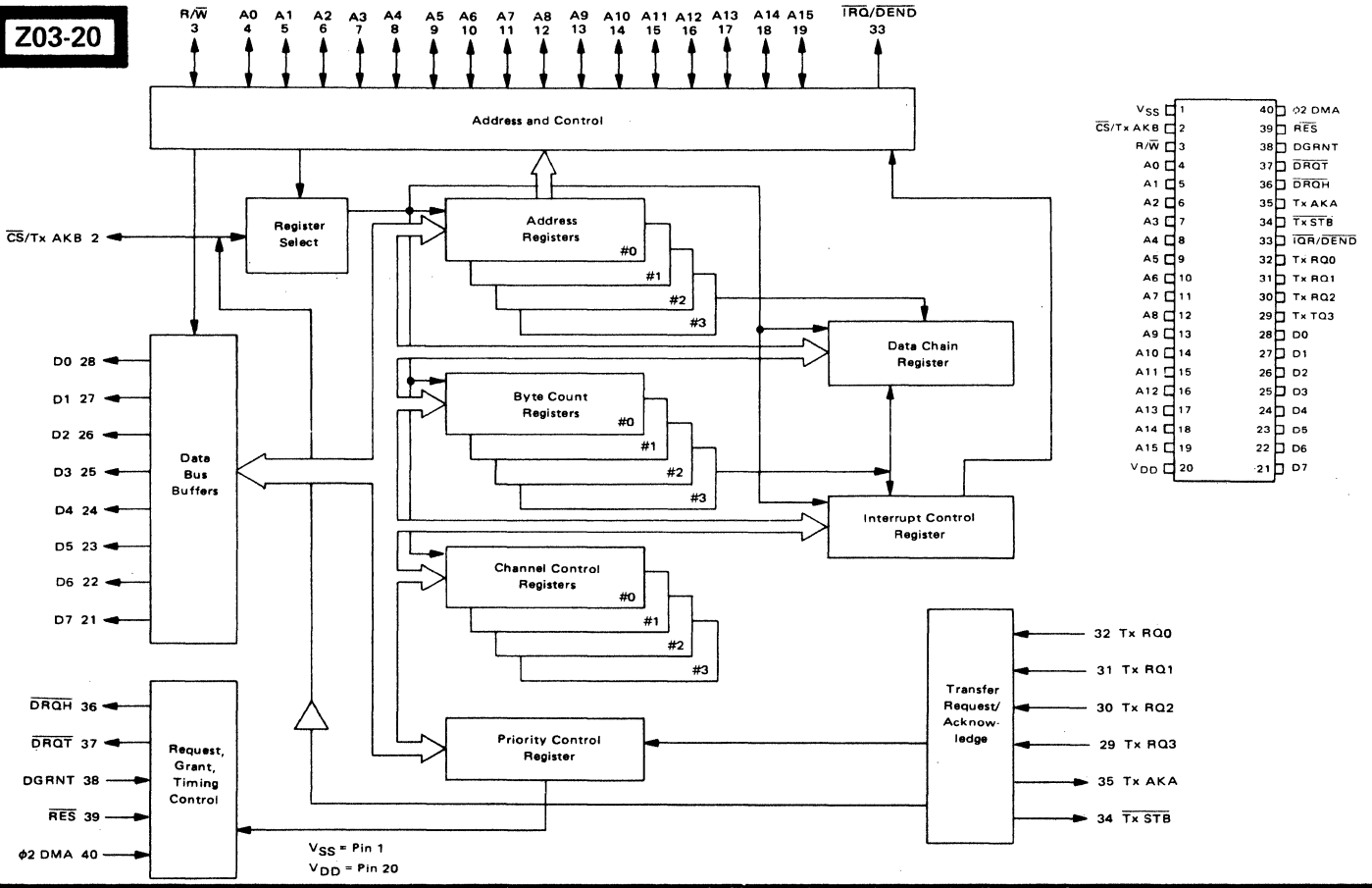


Z03-19

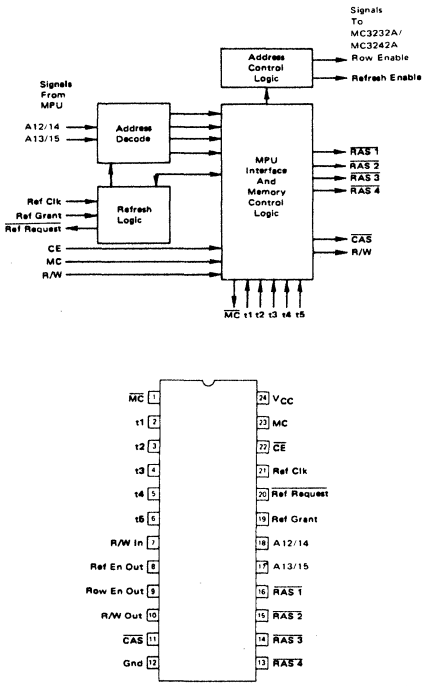




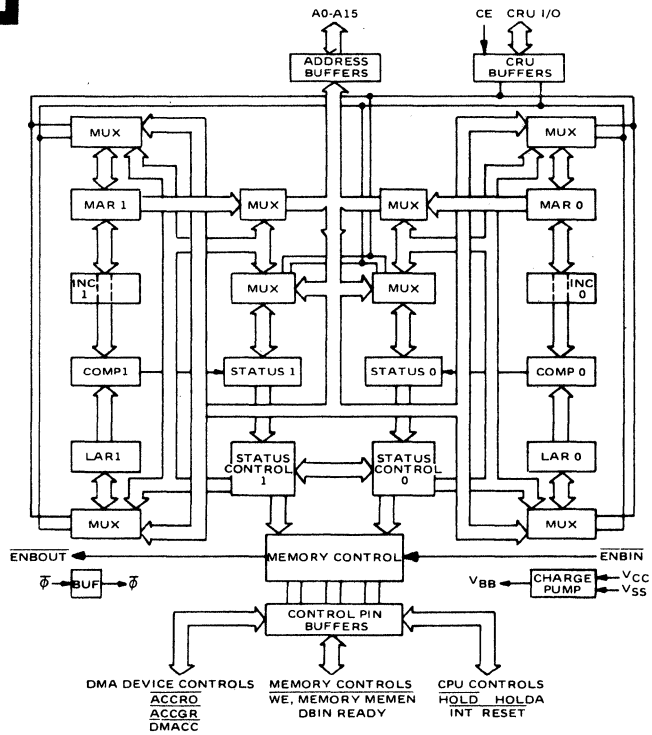
Z03-20



Z03-21



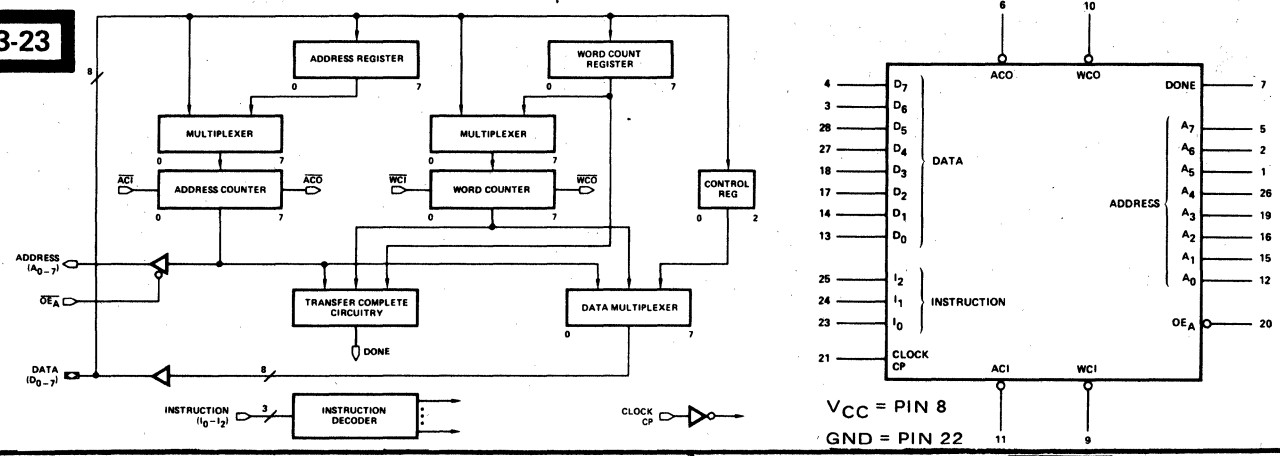
Z03-22



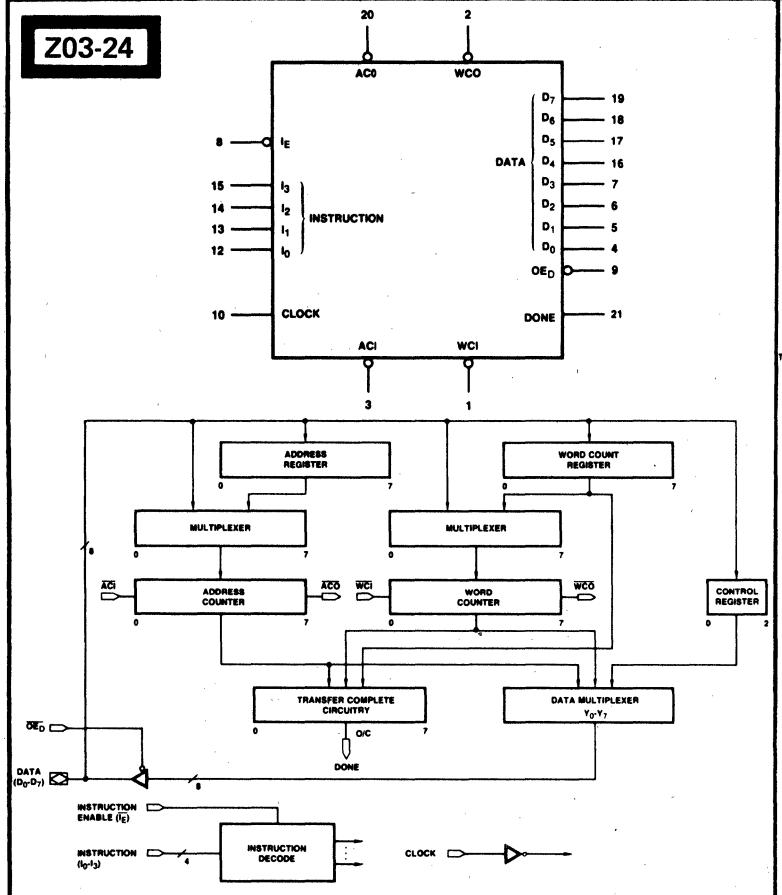
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

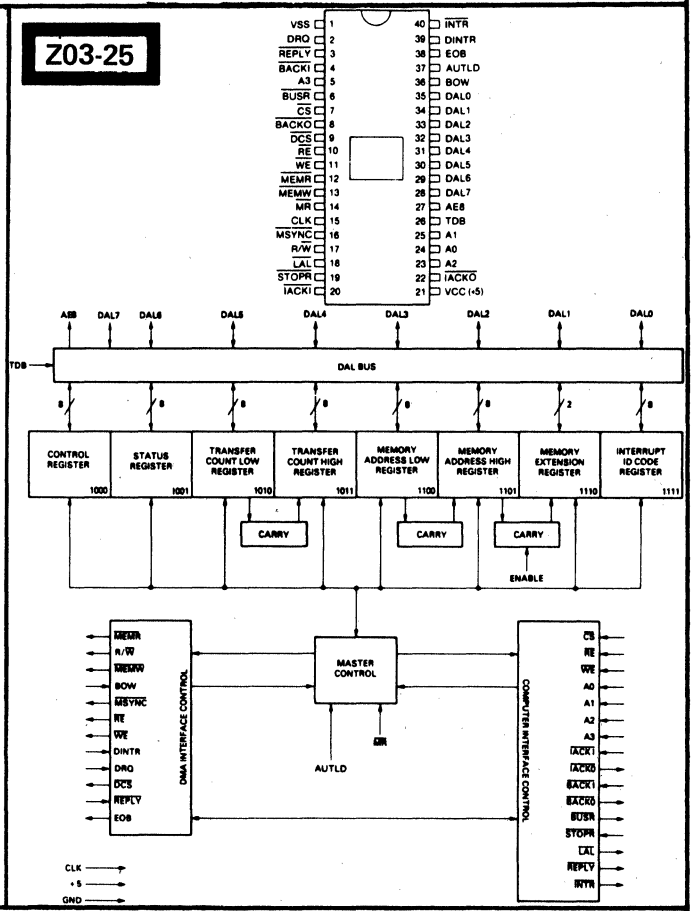
Z03-23



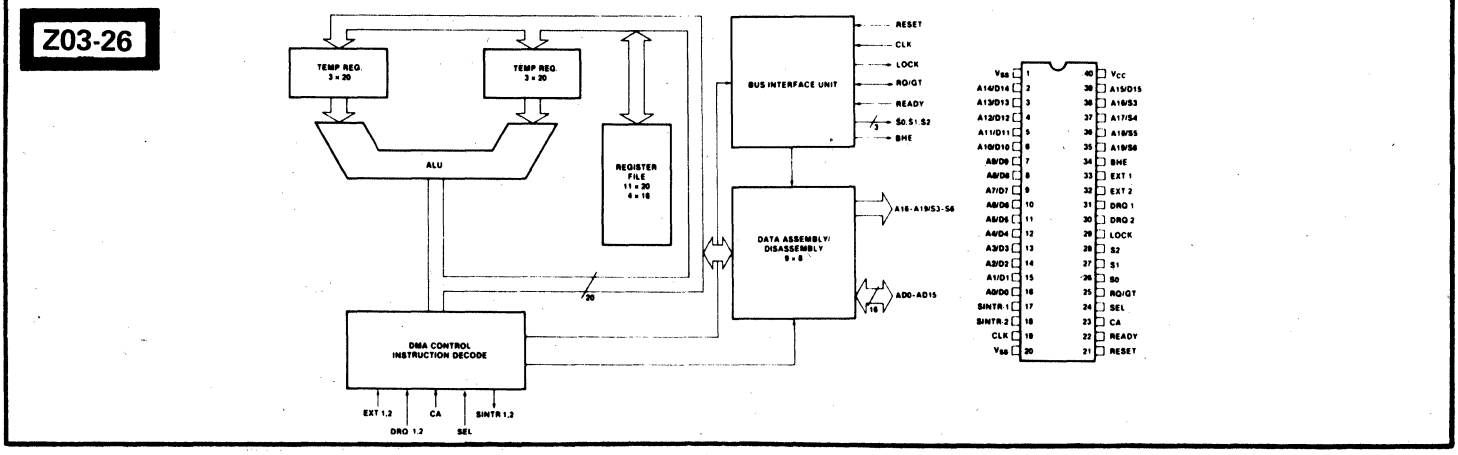
Z03-24



Z03-25



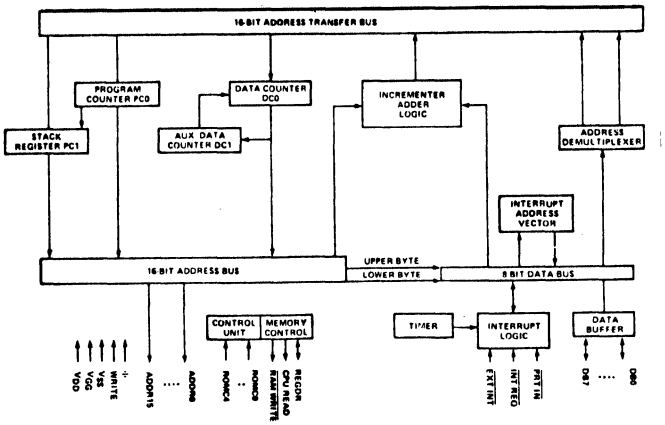
Z03-26



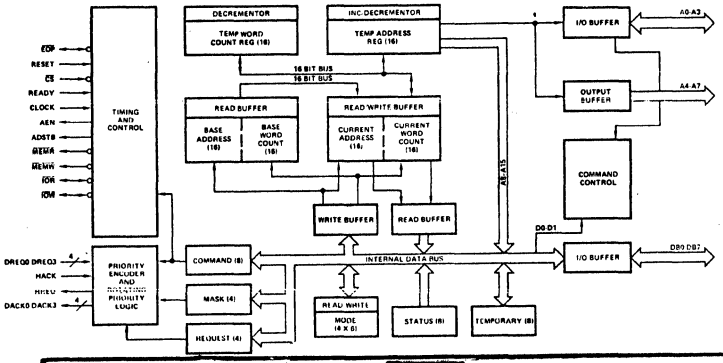
19. LOGIC/BLOCK DRAWINGS

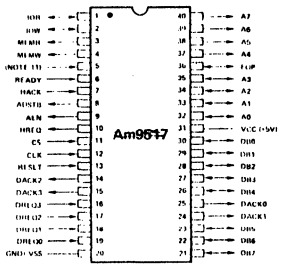
IN DRAWING NUMBER SEQUENCE

Z03-21

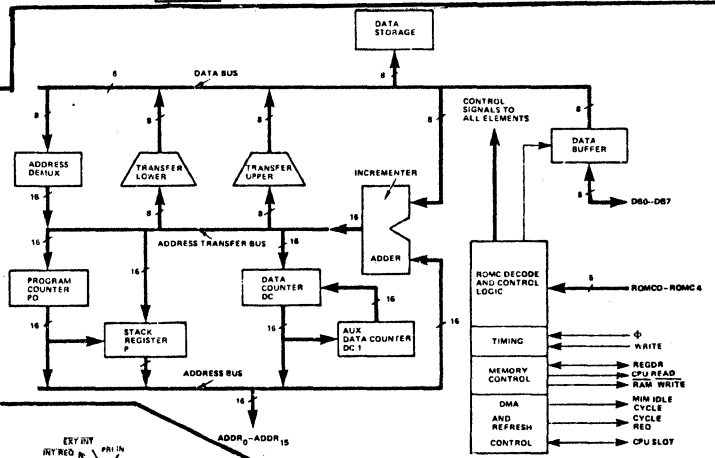


Z03-27

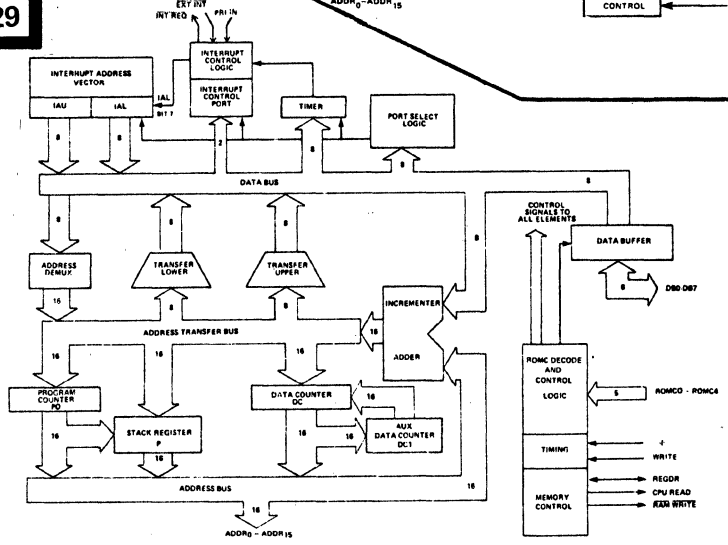




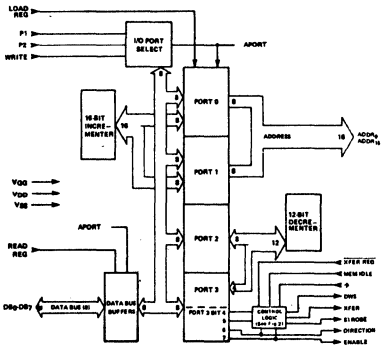
Z03-28



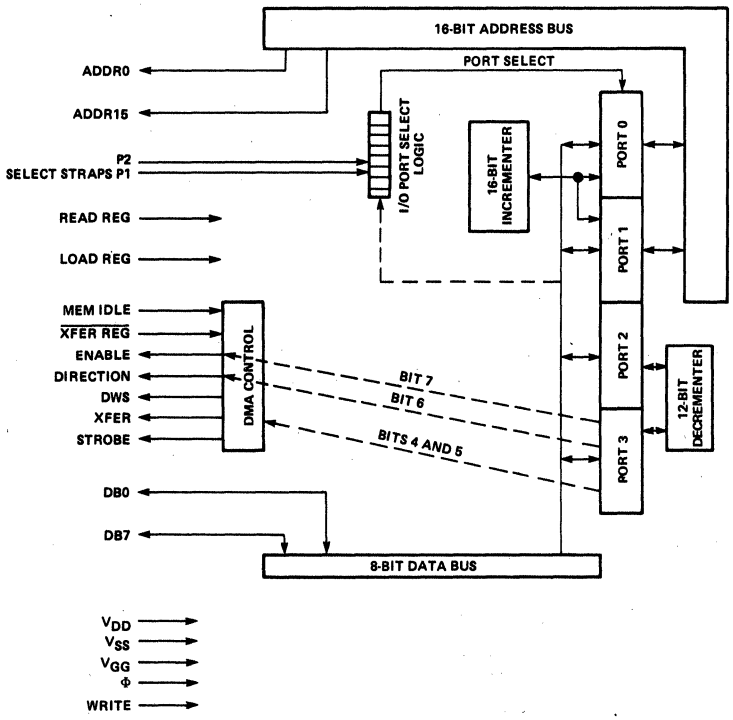
Z03-29



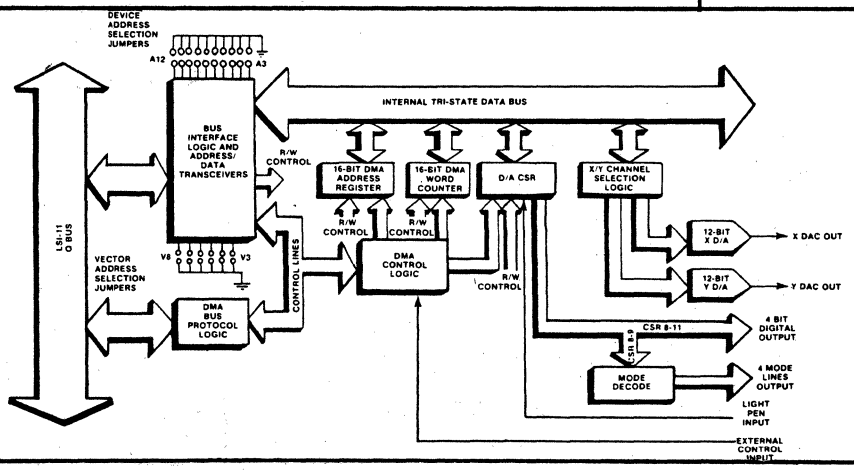
Z03-30



Z03-33


16-BIT ADDRESS BUS
PORT SELECT
ADDR0
ADDR15
P2
SELECT STRAPS P1
READ REG
LOAD REG
MEM IDLE
XFER REG
ENABLE
DIRECTION
DWS
XFER
STROBE
I/O PORT SELECT LOGIC
16-BIT INCREMENTER
DMA CONTROL
BIT 7
BIT 6
BITS 4 AND 5
PORT 0
PORT 1
PORT 2
PORT 3
12-BIT DECREMENTER
DB0
DB7
8-BIT DATA BUS
VDD
VSS
VGG
Φ
WRITE

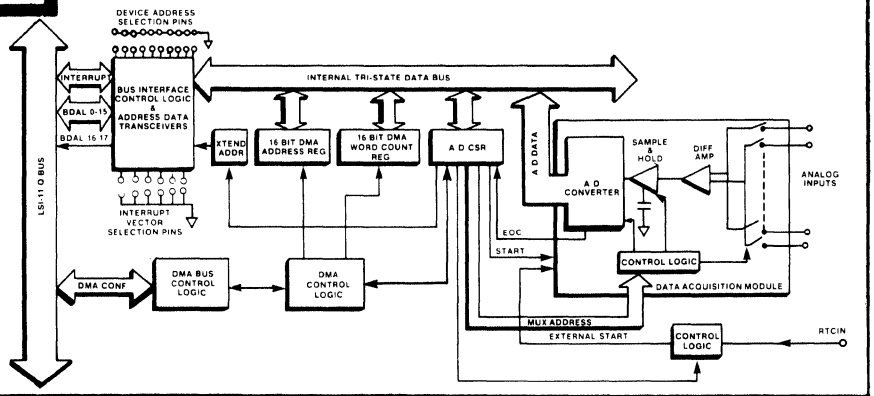
Z03-34


DEVICE ADDRESS SELECTION JUMPERS
A12
A3
INTERNAL TRI-STATE DATA BUS
BUS INTERFACE LOGIC AND ADDRESS/DATA TRANSCEIVERS
R/W CONTROL
16-BIT DMA ADDRESS REGISTER
16-BIT DMA WORD COUNTER
D/A CSR
X/Y CHANNEL SELECTION LOGIC
LSI-11 Q BUS
VECTOR ADDRESS SELECTION JUMPERS
V8
V3
DMA BUS PROTOCOL LOGIC
CONTROL LINES
DMA CONTROL LOGIC
12-BIT X D/A
X DAC OUT
12-BIT Y D/A
Y DAC OUT
CSR 8-11
4 BIT DIGITAL OUTPUT
CSR 4-7
MODE DECODE
4 MODE LINES OUTPUT
LIGHT PEN INPUT
EXTERNAL CONTROL INPUT

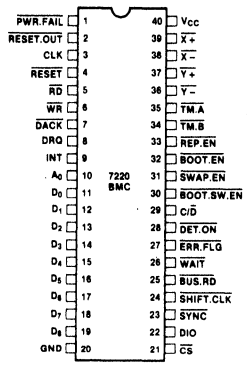
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

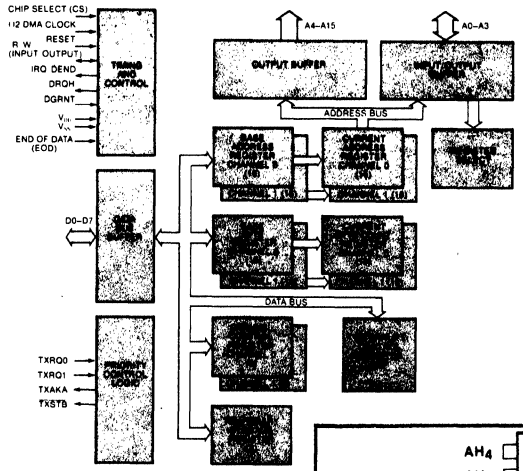
Z03-35

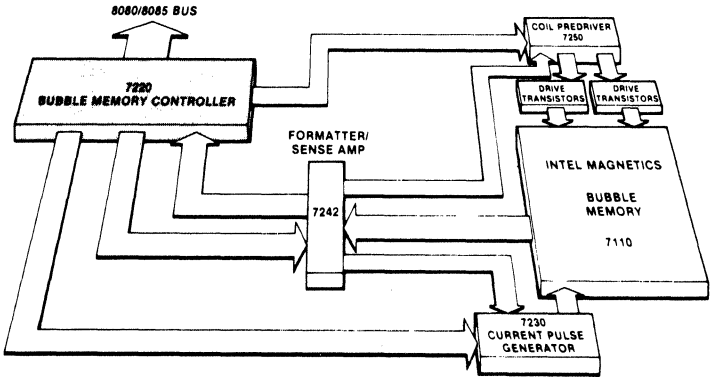


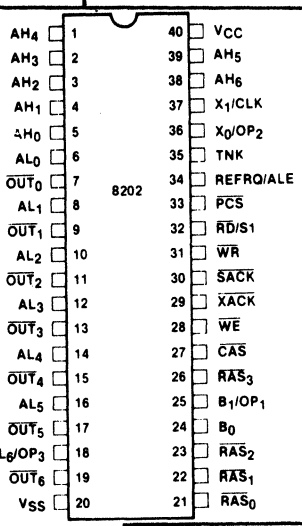
Z03-38



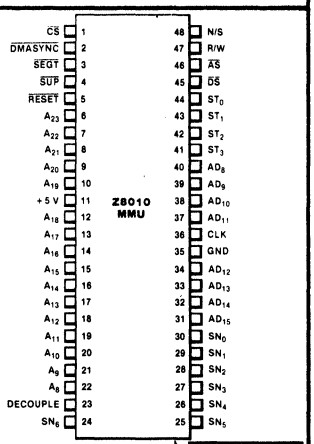
Z03-36



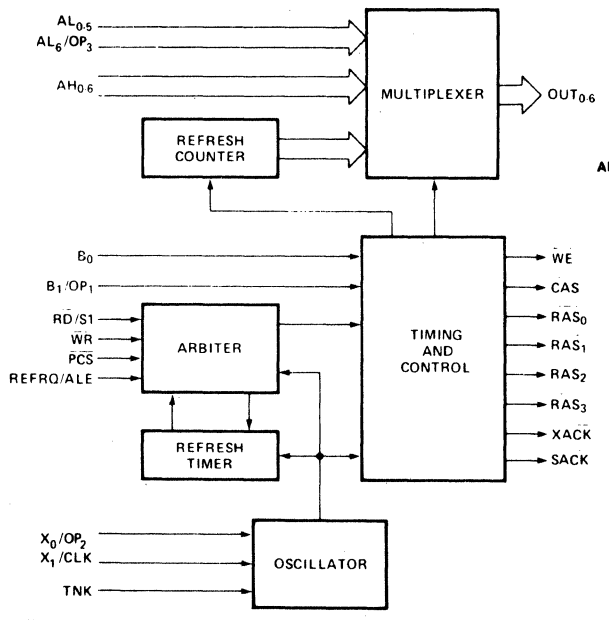


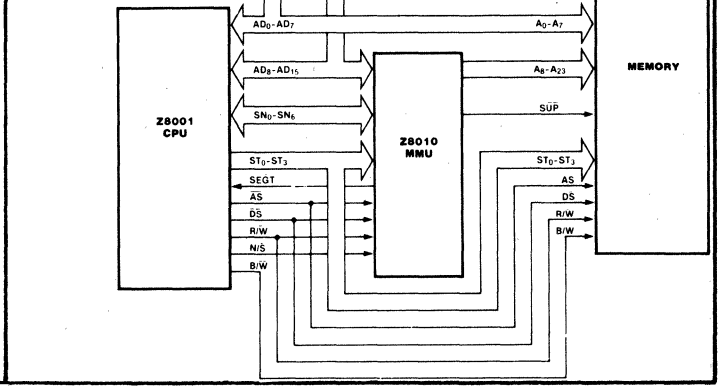


Z03-39

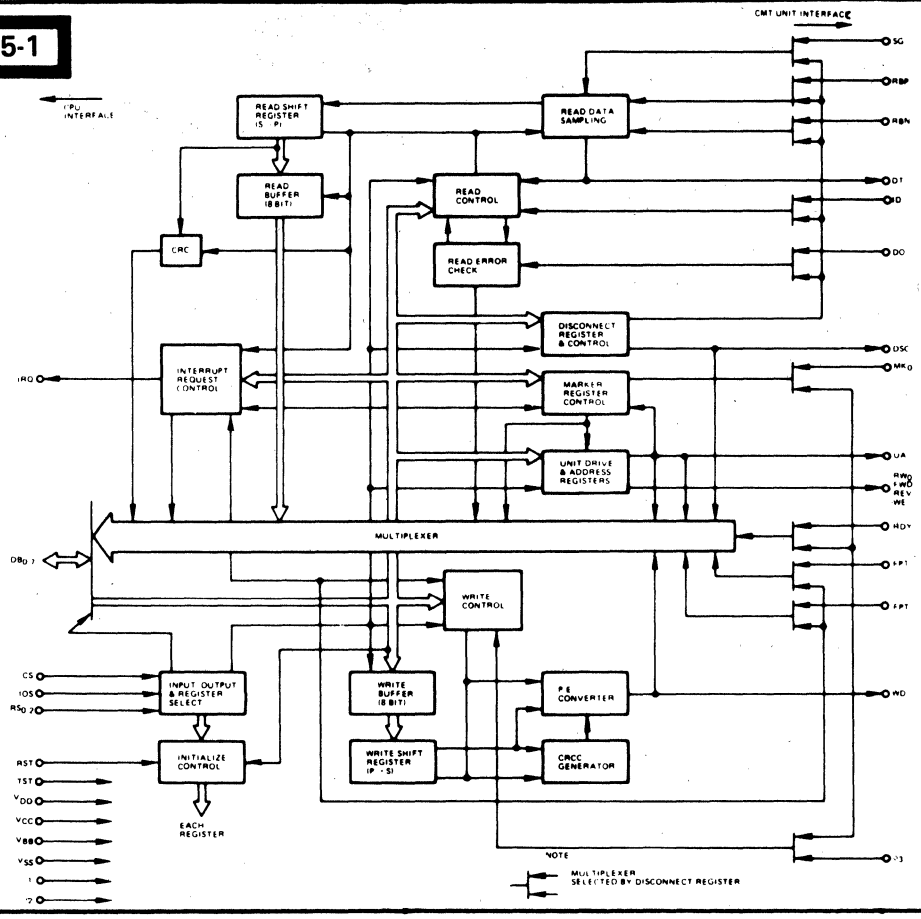


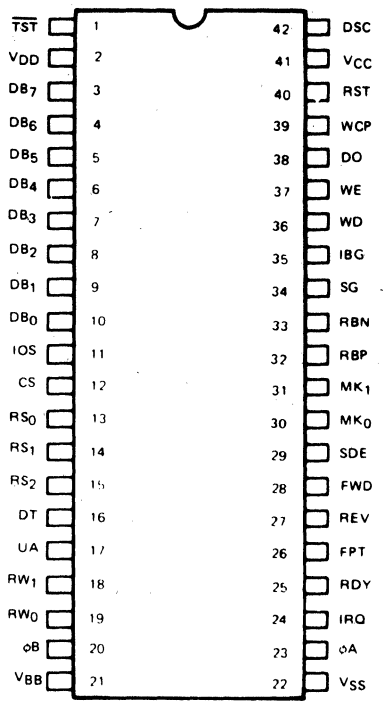
Z03-37



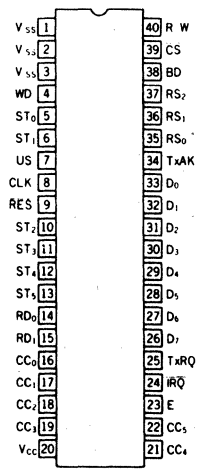


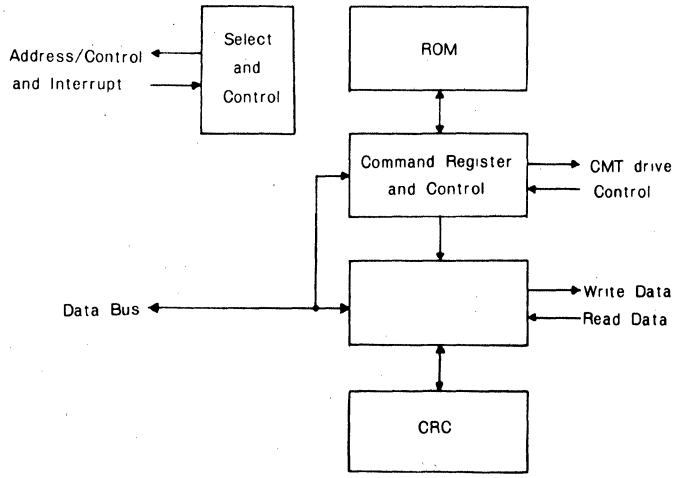
Z05-1


CMT UNIT INTERFACE
CPU INTERFACE
READ SHIFT REGISTER (S - P)
READ DATA SAMPLING
READ BUFFER (8 BIT)
READ CONTROL
CRC
READ ERROR CHECK
DISCONNECT REGISTER & CONTROL
INTERRUPT REQUEST CONTROL
MARKER REGISTER CONTROL
UNIT DRIVE & ADDRESS REGISTERS
MULTIPLEXER
WRITE CONTROL
INPUT OUTPUT & REGISTER SELECT
WRITE BUFFER (8 BIT)
P-S CONVERTER
INITIALIZE CONTROL
WRITE SHIFT REGISTER (P - S)
CRCC GENERATOR
EACH REGISTER
NOTE
MULTIPLEXER SELECTED BY DISCONNECT REGISTER

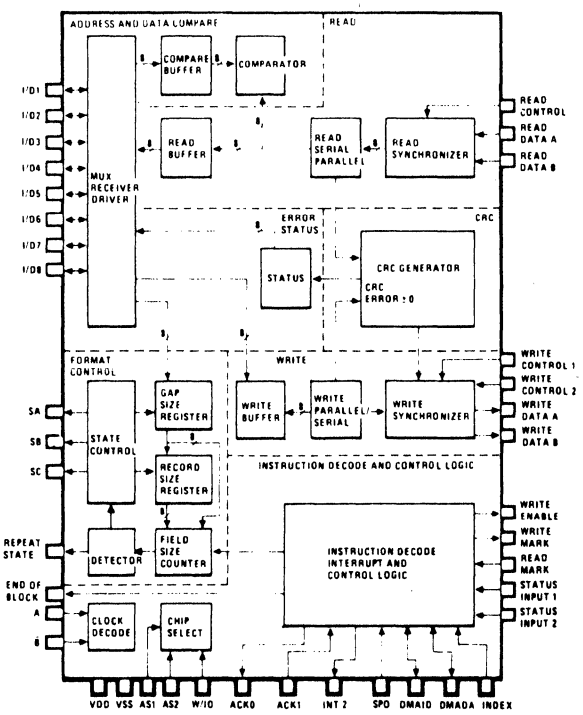

TST 1
VDD 2
DB7 3
DB6 4
DB5 5
DB4 6
DB3 7
DB2 8
DB1 9
DB0 10
IOS 11
CS 12
RS0 13
RS1 14
RS2 15
DT 16
UA 17
RW1 18
RW0 19
øB 20
VBB 21
42 DSC
41 VCC
40 RST
39 WCP
38 DO
37 WE
36 WD
35 IBG
34 SG
33 RBN
32 RBP
31 MK1
30 MK0
29 SDE
28 FWD
27 REV
26 FPT
25 RDY
24 IRQ
23 øA
22 VSS

Z05-2

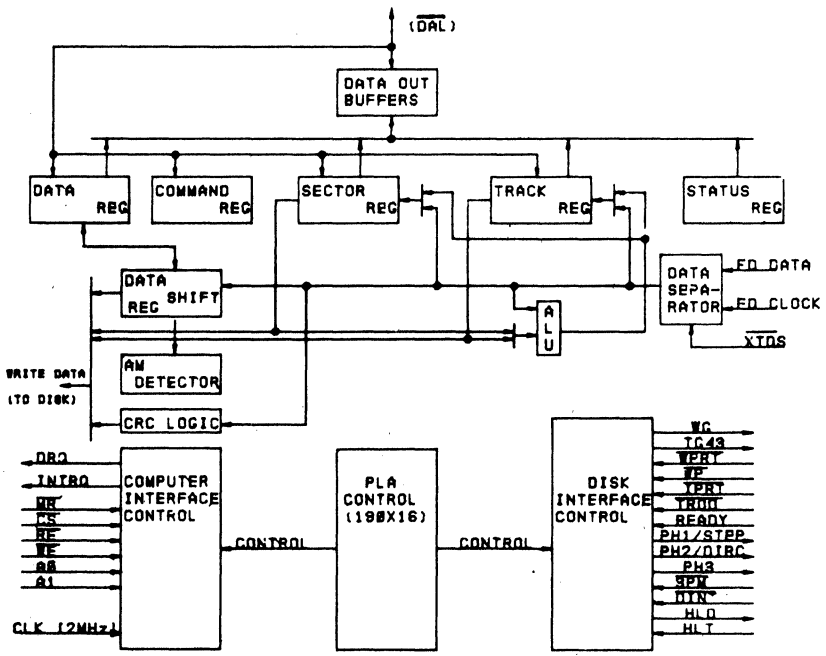

VSS 1
VSS 2
VSS 3
WD 4
ST0 5
ST1 6
US 7
CLK 8
RES 9
ST2 10
ST3 11
ST4 12
ST5 13
RD0 14
RD1 15
CC0 16
CC1 17
CC2 18
CC3 19
VCC 20
40 R W
39 CS
38 BD
37 RS2
36 RS1
35 RS0
34 TxAK
33 D0
32 D1
31 D2
30 D3
29 D4
28 D5
27 D6
26 D7
25 TxRQ
24 IRQ
23 E
22 CC5
21 CC4

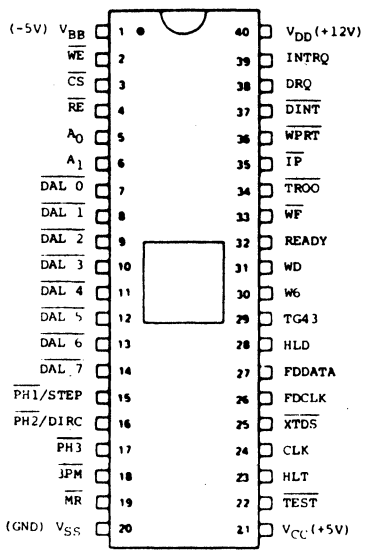

Address/Control and Interrupt
Select and Control
ROM
Command Register and Control
CMT drive Control
Data Bus
Write Data
Read Data
CRC

Z07-1


ADDRESS AND DATA COMPARE
READ
COMPARE BUFFER
COMPARATOR
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
MUX RECEIVER DRIVER
READ BUFFER
READ SERIAL PARALLEL
READ SYNCHRONIZER
READ CONTROL
READ DATA A
READ DATA B
ERROR STATUS
CRC
STATUS
CRC GENERATOR
CRC ERROR : 0
FORMAT CONTROL
WRITE
WRITE CONTROL 1
WRITE CONTROL 2
WRITE DATA A
WRITE DATA B
GAP SIZE REGISTER
WRITE BUFFER
WRITE PARALLEL/SERIAL
WRITE SYNCHRONIZER
SA
SB
SC
STATE CONTROL
RECORD SIZE REGISTER
INSTRUCTION DECODE AND CONTROL LOGIC
REPEAT STATE
DETECTOR
FIELD SIZE COUNTER
INSTRUCTION DECODE INTERRUPT AND CONTROL LOGIC
WRITE ENABLE
WRITE MARK
READ MARK
STATUS INPUT 1
STATUS INPUT 2
END OF BLOCK
A
B
CLOCK DECODE
CHIP SELECT
VDD VSS AS1 AS2 W/IO ACK0 ACK1 INT 2 SPO DMAID DMADA INDEX

Z07-2

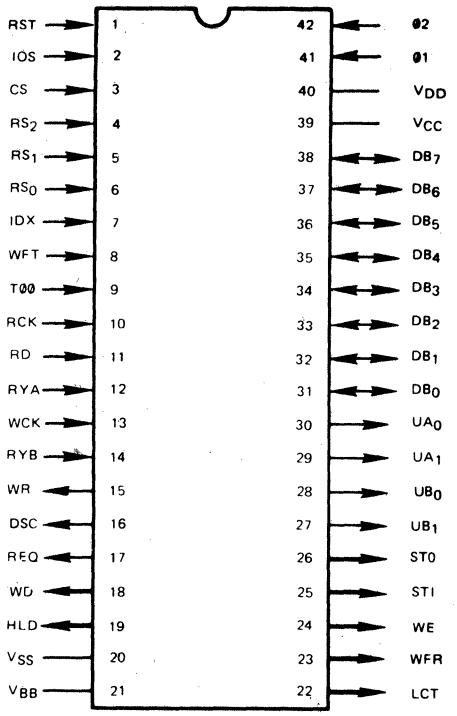

(DAL)
DATA OUT BUFFERS
DATA REG
COMMAND REG
SECTOR REG
TRACK REG
STATUS REG
DATA REG SHIFT
A L U
DATA SEPA-RATOR
FD DATA
FD CLOCK
XTDS
AM DETECTOR
WRITE DATA (TO DISK)
CRC LOGIC
DRQ
INTRQ
WR
CS
RE
WE
A0
A1
CLK (2MHz)
COMPUTER INTERFACE CONTROL
CONTROL
PLA CONTROL (198X16)
CONTROL
DISK INTERFACE CONTROL
WG
TG43
WPRT
WF
TPRT
TR00
READY
PH1/STEP
PH2/DIRC
PH3
3PM
DIN
HLD
HLT


(-5V) VBB
WE
CS
RE
A0
A1
DAL 0
DAL 1
DAL 2
DAL 3
DAL 4
DAL 5
DAL 6
DAL 7
PH1/STEP
PH2/DIRC
PH3
3PM
MR
(GND) VSS
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
VDD (+12V)
INTRQ
DRQ
DINT
WPRT
IP
TR00
WF
READY
WD
W6
TG43
HLD
FDDATA
FDCLK
XTDS
CLK
HLT
TEST
VCC (+5V)

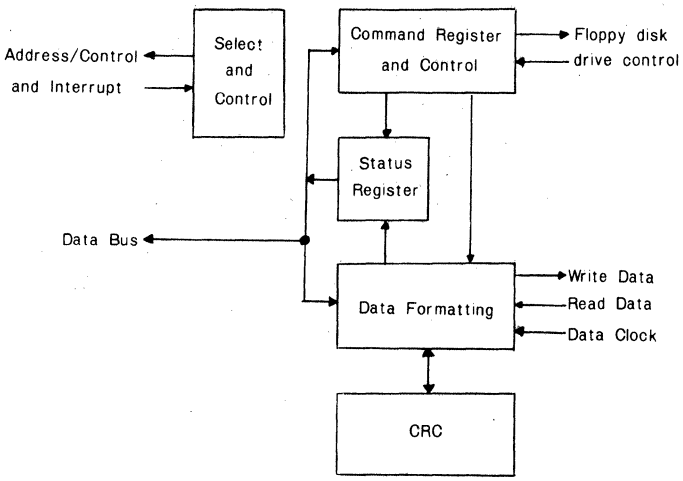
19. LOGIC/BLOCK DRAWINGS

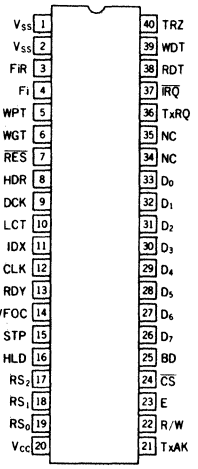
IN DRAWING NUMBER SEQUENCE

Z07-3

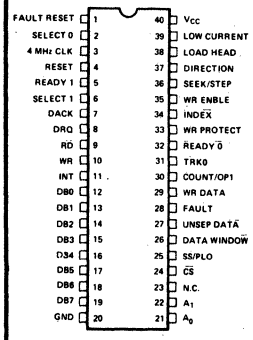


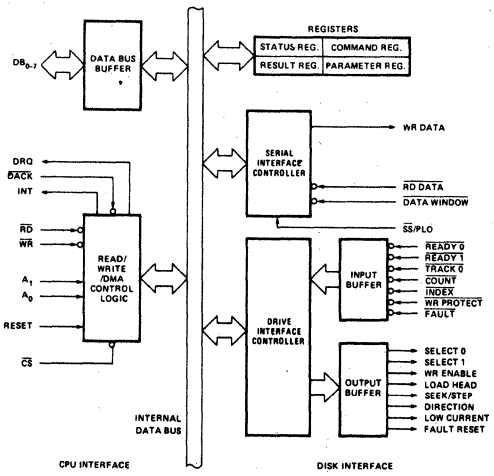
Z07-4



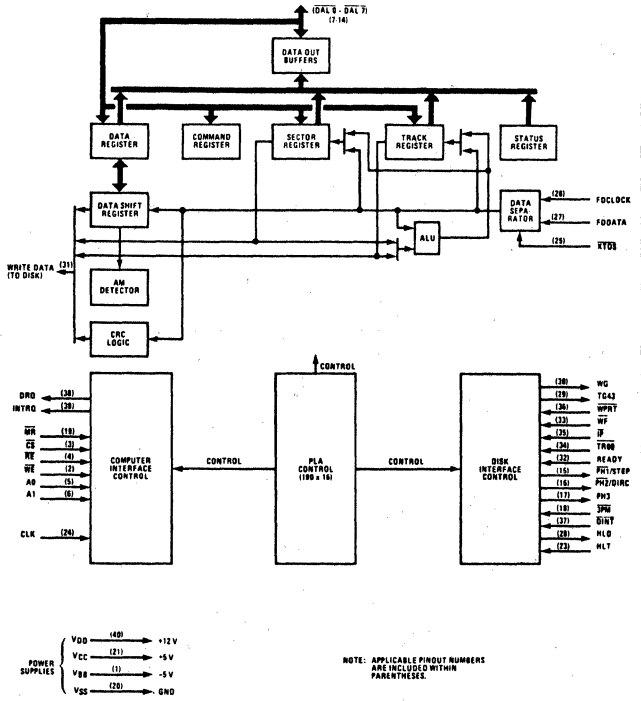


Z07-5





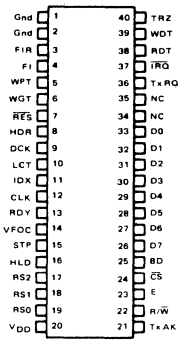
Z07-6

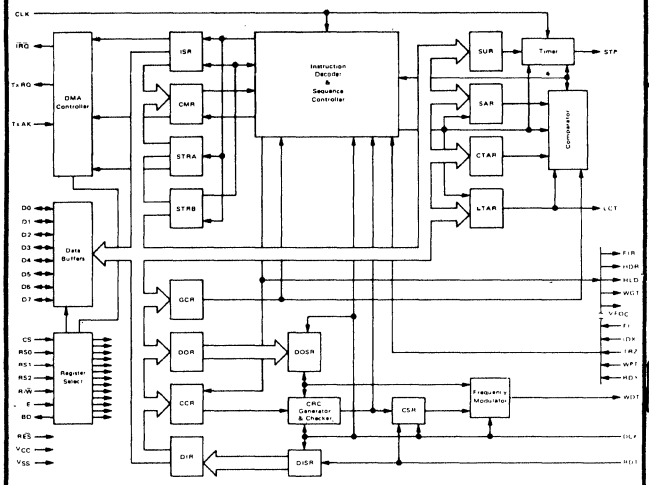


19. LOGIC/BLOCK DRAWINGS

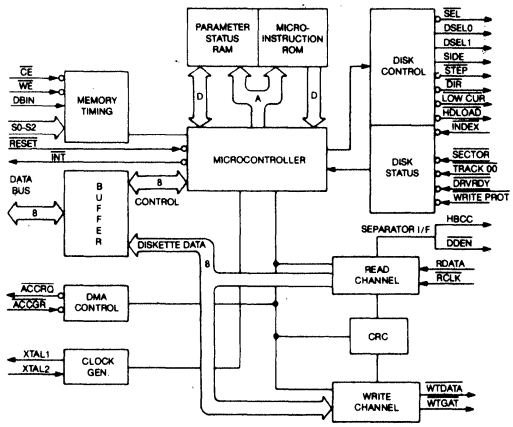
IN DRAWING NUMBER SEQUENCE

Z07-7

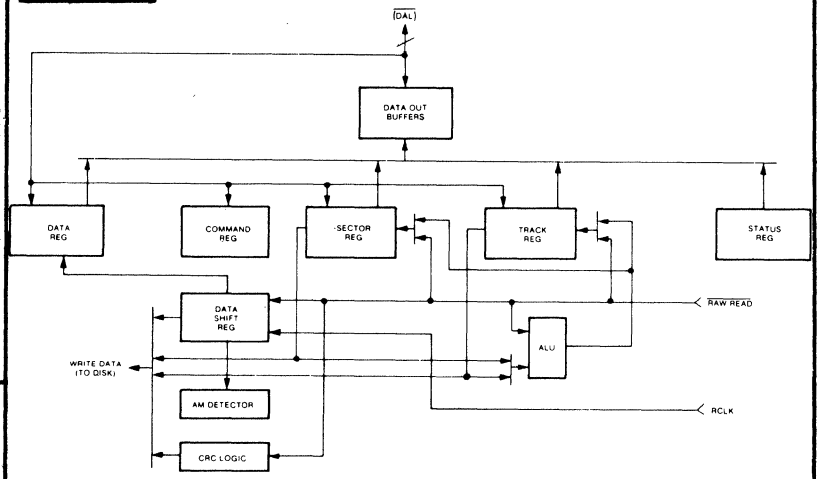




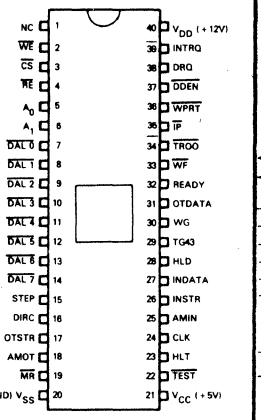
Z07-8

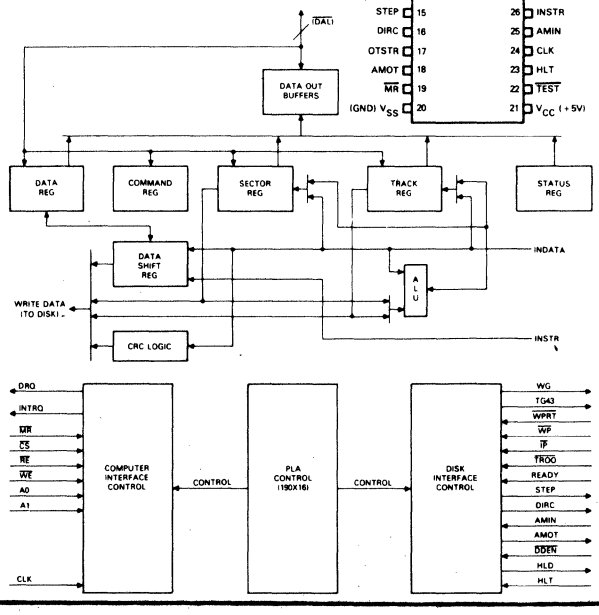


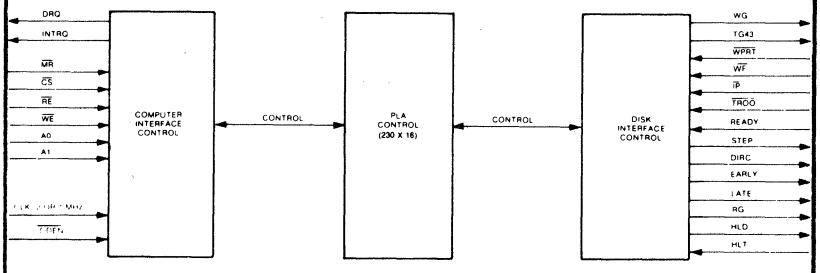
Z07-9

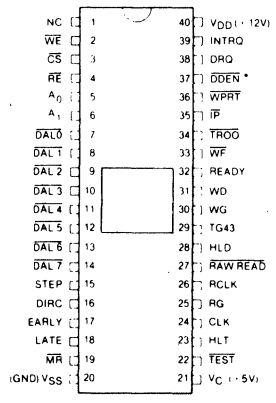


Z07-10







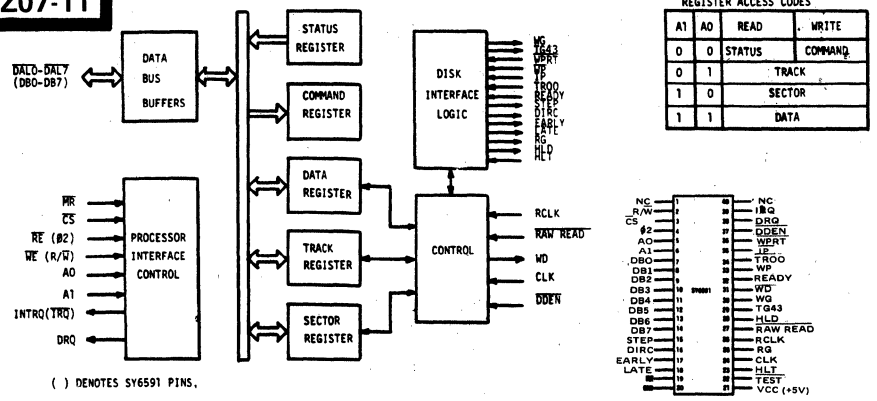


Z07-9a: PIN 37 MUST BE LEFT OPEN

19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

Z07-11

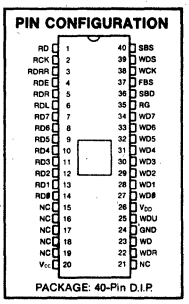


REGISTER ACCESS CODES

A1	A0	READ	WRITE
0	0	STATUS	COMMAND
0	1	TRACK	
1	0	SECTOR	
1	1	DATA	

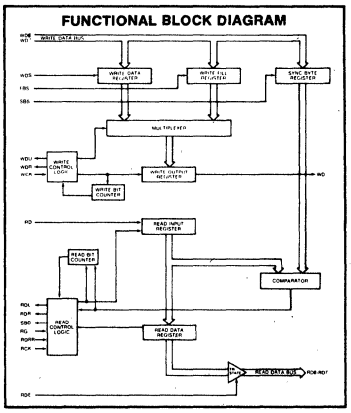
Z07-12

PIN CONFIGURATION

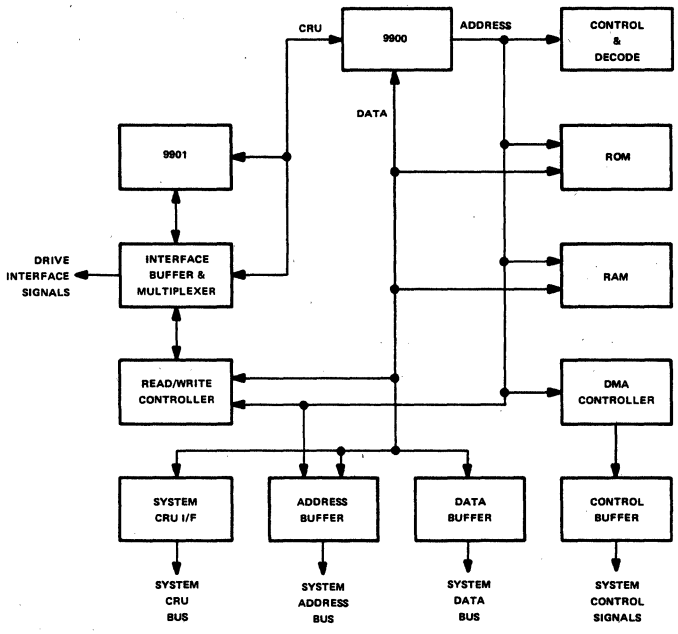


PACKAGE: 40-Pin D.I.P.

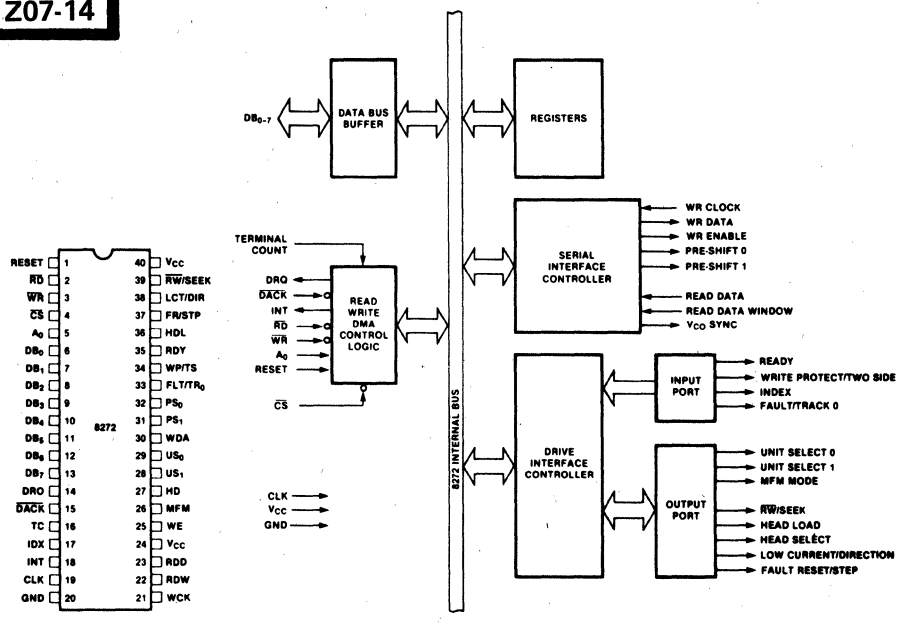
FUNCTIONAL BLOCK DIAGRAM



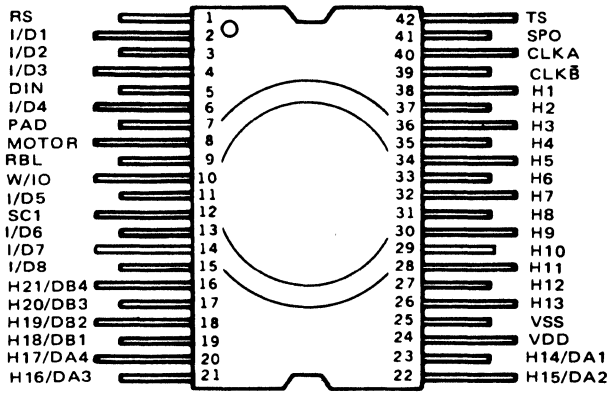
Z07-13



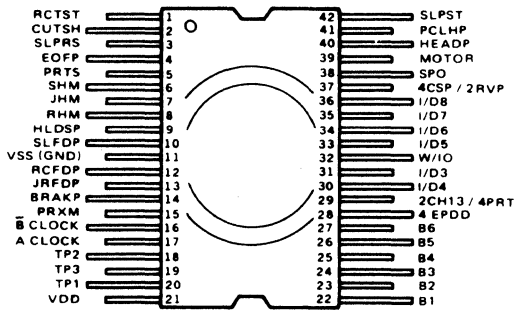
Z07-14

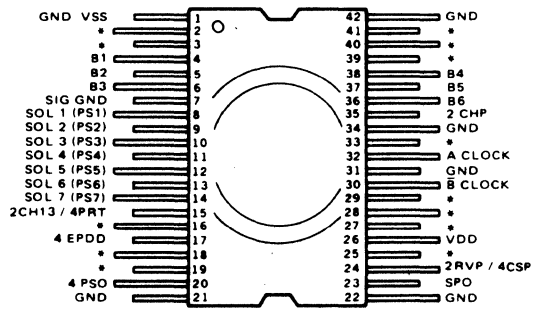


Z08-1

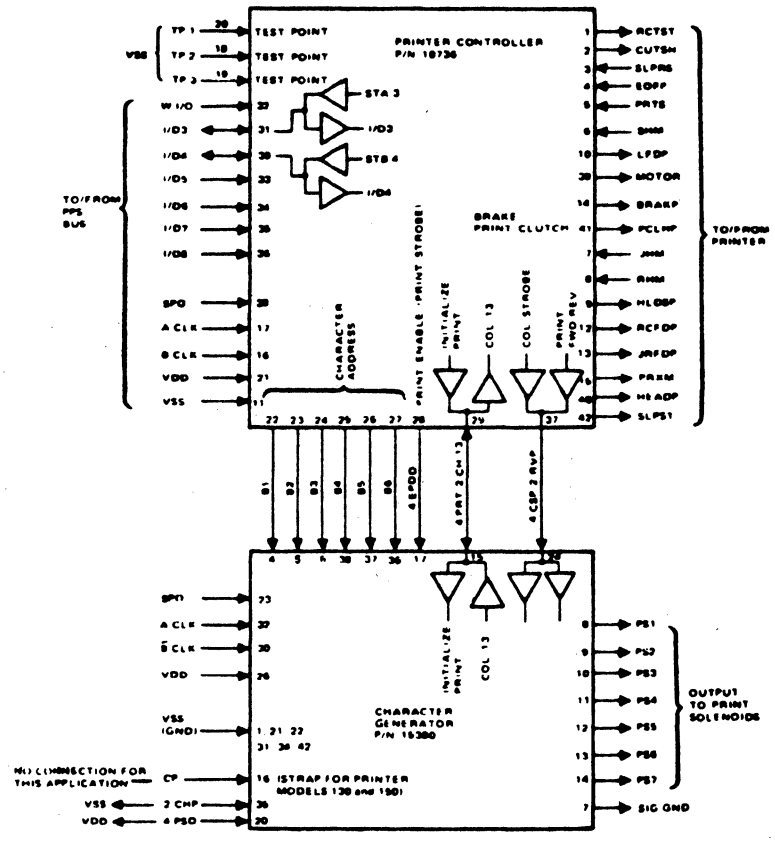


Z08-2





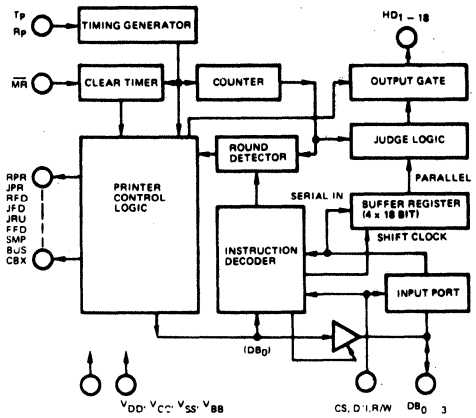
* NO CONNECTION

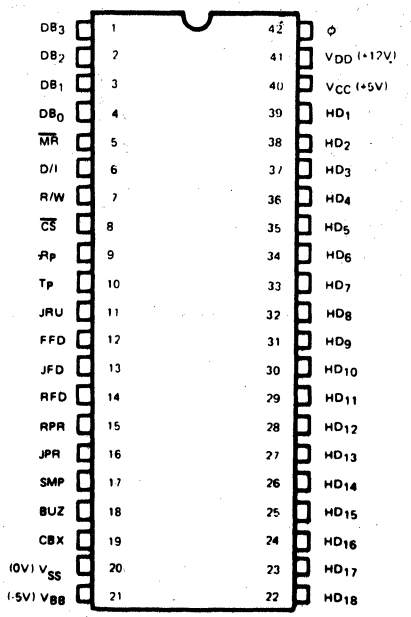


19. LOGIC/BLOCK DRAWINGS

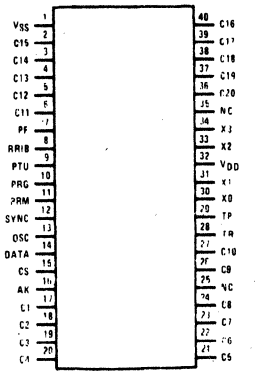
IN DRAWING NUMBER SEQUENCE

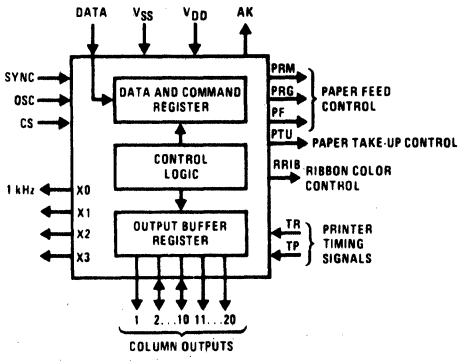
Z08-3



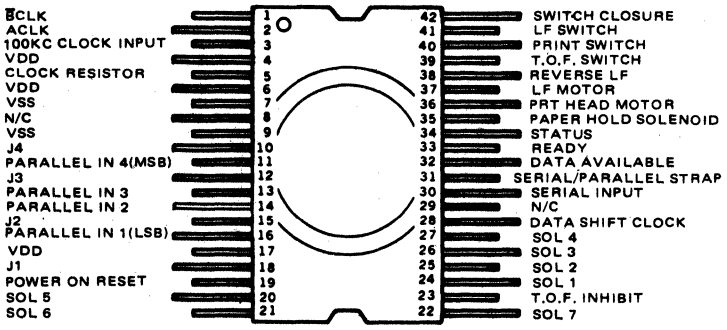


Z08-4

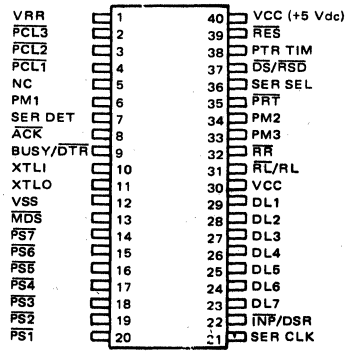




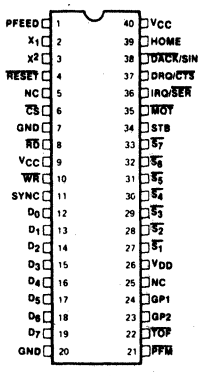
Z08-5

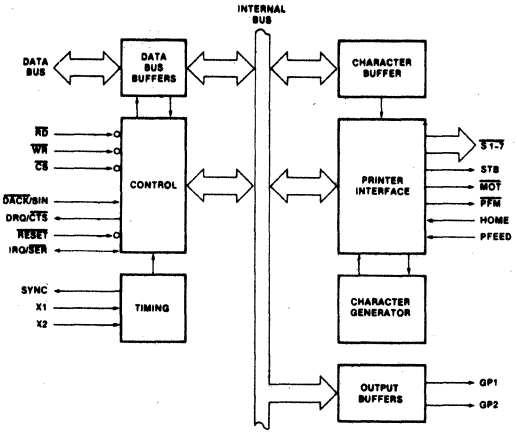


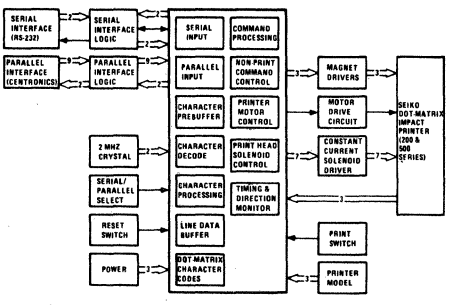
Z08-7



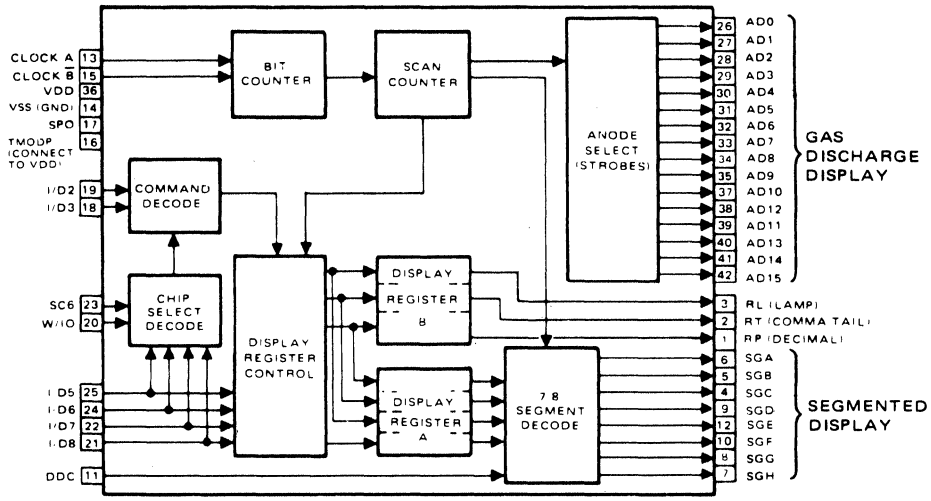
Z08-6



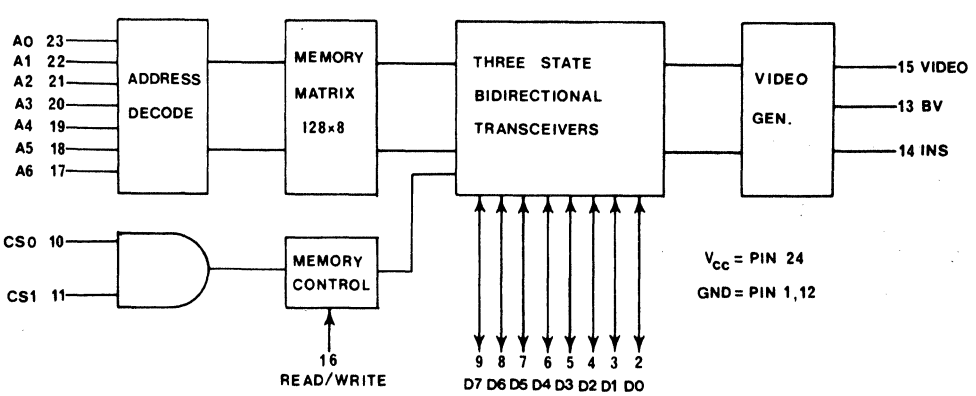




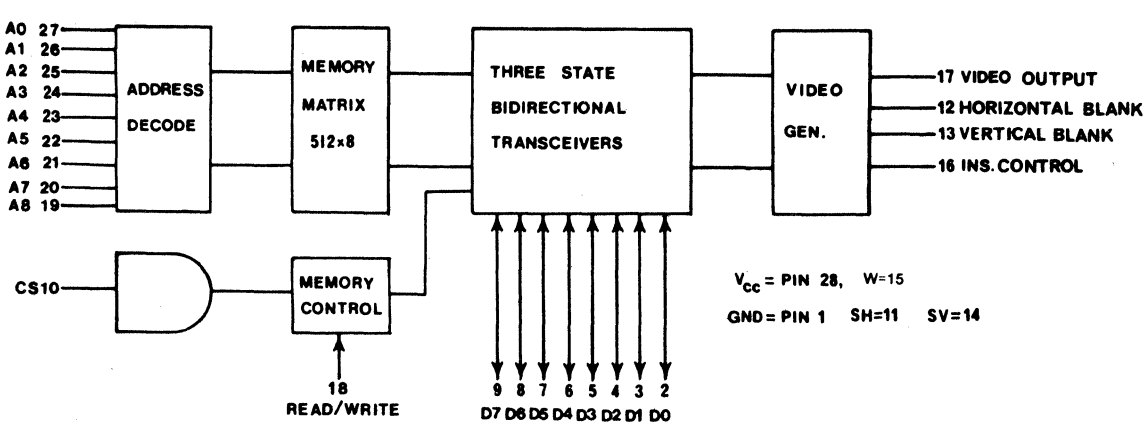
Z09-1



Z09-2



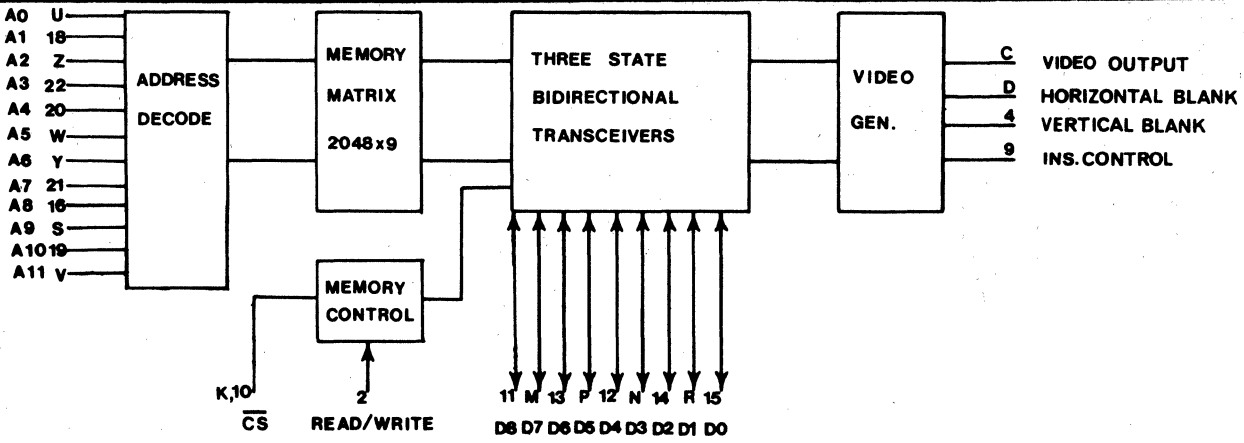
Z09-3



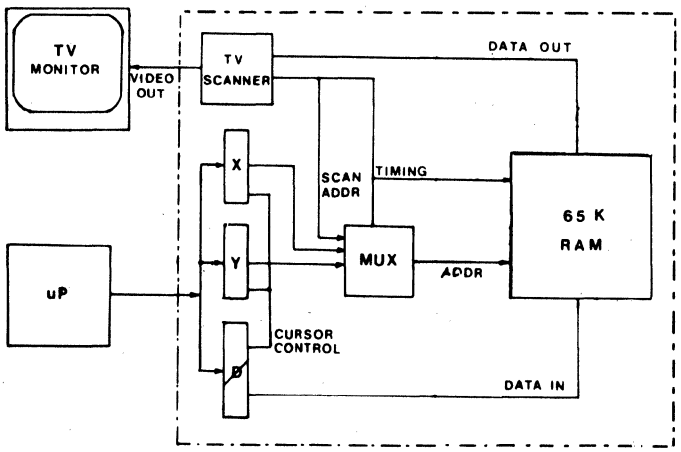
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

Z09-4



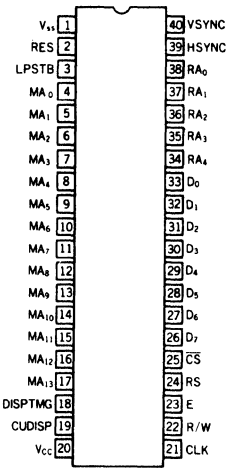
Z09-5

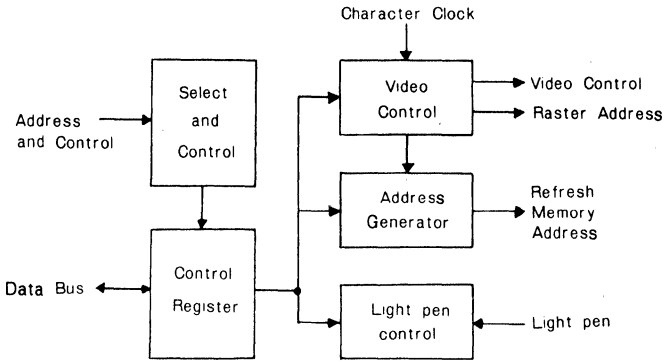


PIN		SIGNAL	FUNCTION
	1	VE	Vector enable
A		M/S	Master/Slave
	2	RH	Reset horizontal
B		DCLK	Dot Clock
	3	GND	
C		GND	
	4	RV	Reset vertical
D		—	—
	5	DOUTO	TTL video out
E		+12V	—
	6	DDϕ	Image data bit
F		—	—
	7	—	—
H		ALPHA	Alphanumeric video input
	8	VDO	Composite video output
J		—	—
	9	SV	Vertical Sync
K		SH	Horizontal Sync
	10	BV	Vertical Blank
L		—	—
	11	READY LOAD	
M		READY	
	12	D1	Data Input Bit 1
N		DO	Data Input Bit O
	13	D3	Data Input Bit 3
P		D2	Data Input Bit 2
	14	D5	Data Input Bit 5
R		D4	Data Input Bit 4
	15	D7	Data Input Bit 7
S		D6	Data Input Bit 6
	16	—	—
T		R/W	Read/Write
	17	CS	Chip Select
U		$\overline{CS}$	Chip select bar
	18	MA1	Address Bit 1
V		MAO	Address Bit O
	19	—	—
W		—	—
	20	+5V	—
X		+5V	—
	21	—	—
Y		—	—
	22	—	—
Z		—	—

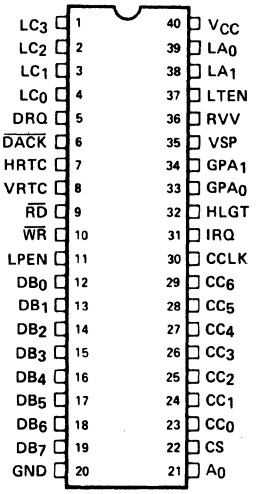
★NOTE: Alpha input (Pin H) has to be tied low when not used.

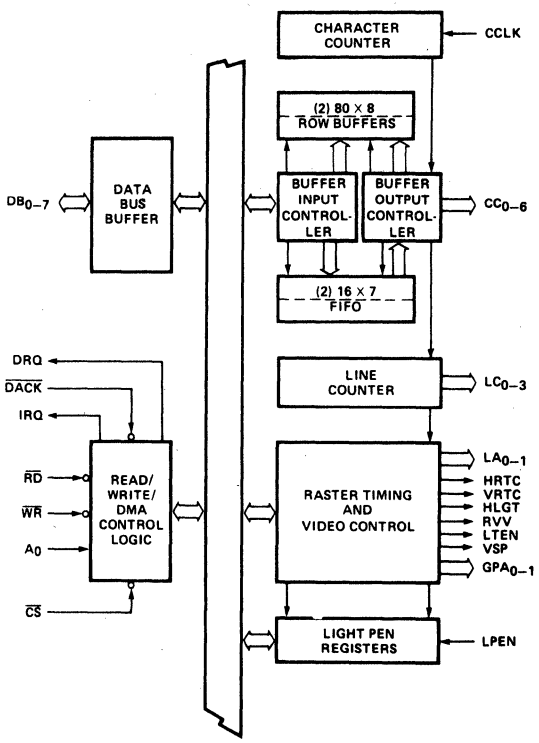
Z09-6


Vss 1
RES 2
LPSTB 3
MA0 4
MA1 5
MA2 6
MA3 7
MA4 8
MA5 9
MA6 10
MA7 11
MA8 12
MA9 13
MA10 14
MA11 15
MA12 16
MA13 17
DISPTMG 18
CUDISP 19
Vcc 20
40 VSYNC
39 HSYNC
38 RA0
37 RA1
36 RA2
35 RA3
34 RA4
33 D0
32 D1
31 D2
30 D3
29 D4
28 D5
27 D6
26 D7
25 CS
24 RS
23 E
22 R/W
21 CLK

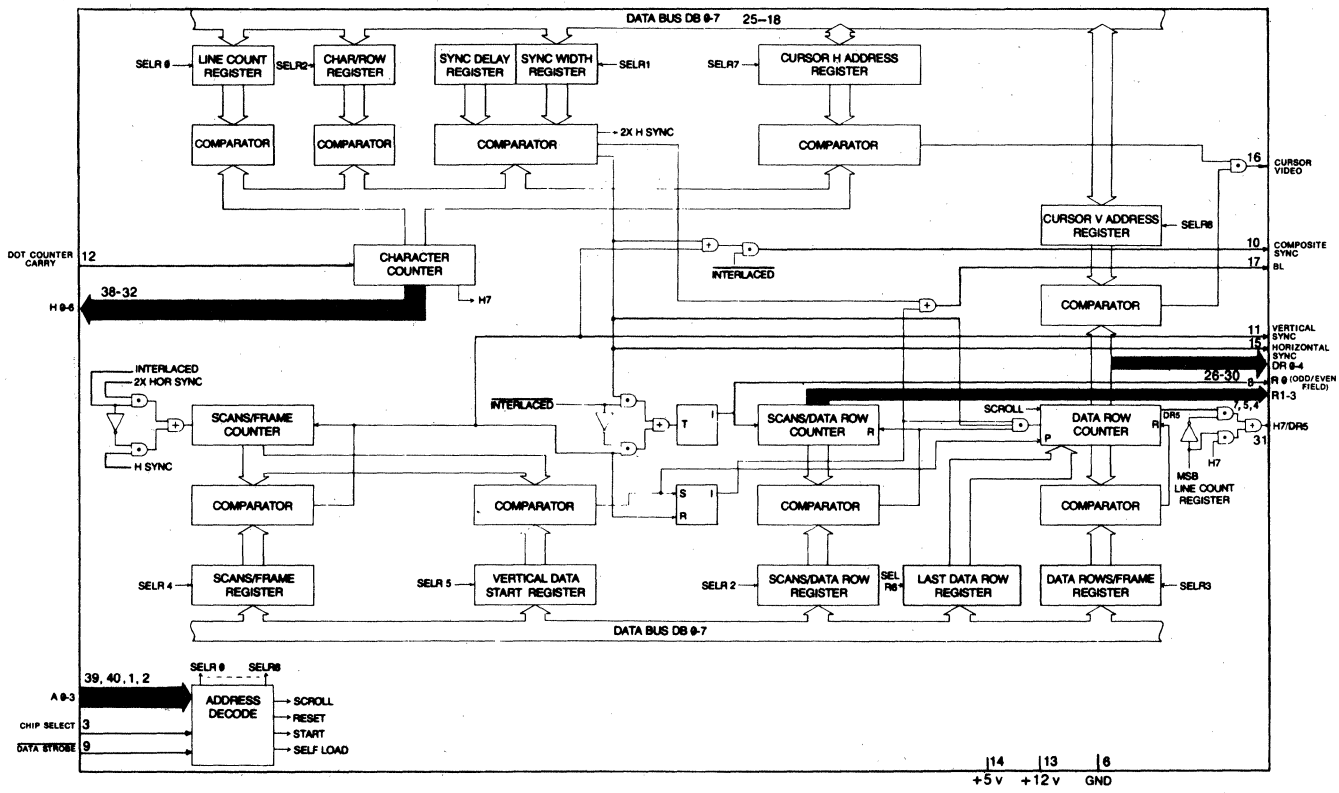

Character Clock
Address and Control
Select and Control
Video Control
Video Control
Raster Address
Address Generator
Refresh Memory Address
Data Bus
Control Register
Light pen control
Light pen

Z09-7

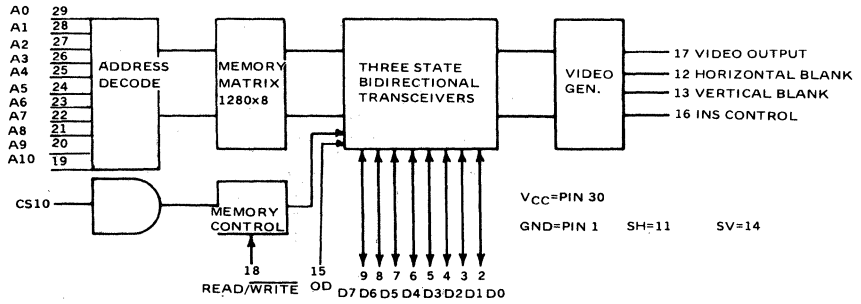

LC3 1
LC2 2
LC1 3
LC0 4
DRQ 5
DACK 6
HRTC 7
VRTC 8
RD 9
WR 10
LPEN 11
DB0 12
DB1 13
DB2 14
DB3 15
DB4 16
DB5 17
DB6 18
DB7 19
GND 20
40 Vcc
39 LA0
38 LA1
37 LTEN
36 RVV
35 VSP
34 GPA1
33 GPA0
32 HLGT
31 IRQ
30 CCLK
29 CC6
28 CC5
27 CC4
26 CC3
25 CC2
24 CC1
23 CC0
22 CS
21 A0


CHARACTER COUNTER
CCLK
(2) 80 x 8 ROW BUFFERS
DB0–7
DATA BUS BUFFER
BUFFER INPUT CONTROL-LER
BUFFER OUTPUT CONTROL-LER
CC0–6
(2) 16 x 7 FIFO
DRQ
DACK
IRQ
LINE COUNTER
LC0–3
RD
WR
A0
CS
READ/ WRITE/ DMA CONTROL LOGIC
RASTER TIMING AND VIDEO CONTROL
LA0–1
HRTC
VRTC
HLGT
RVV
LTEN
VSP
GPA0–1
LIGHT PEN REGISTERS
LPEN

Z09-8

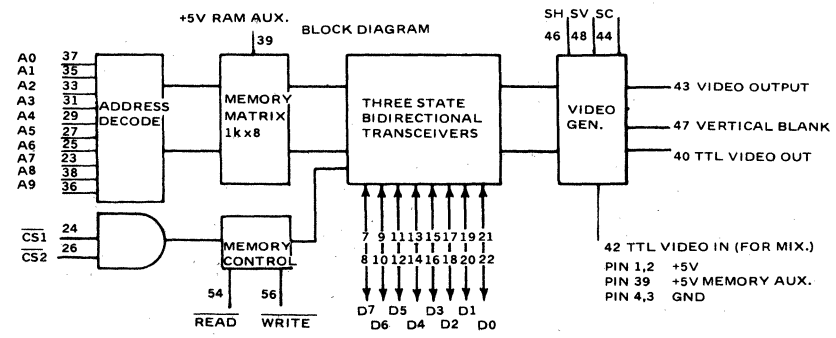


Z09-9

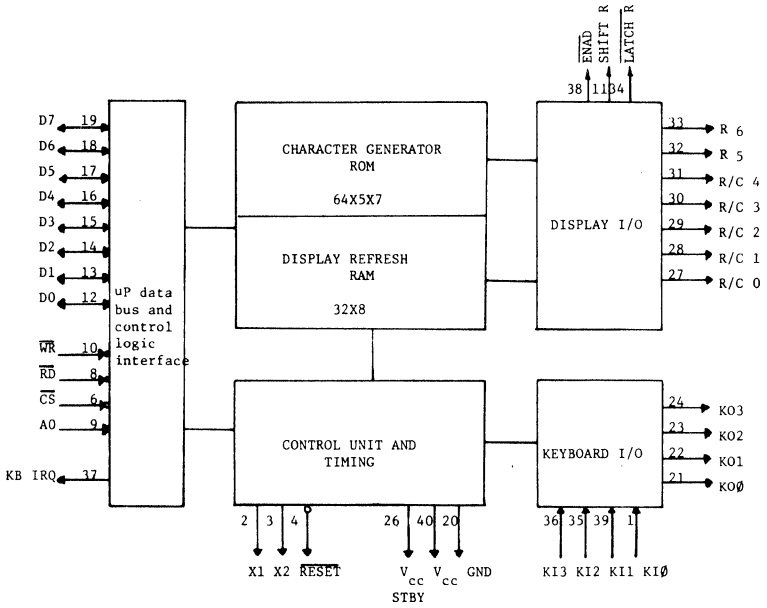


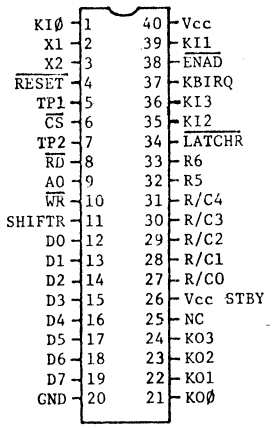
Z09-10

FUNCTION	PIN NO.		FUNCTION
+5V	2	1	+5V
GND	4	3	GND
—	6	5	—
D17	8	7	D07
D16	10	9	D06
D15	12	11	D05
D14	14	13	D04
D13	16	15	D03
D12	18	17	D02
D11	20	19	D01
D10	22	21	D00
$\overline{CS1}$	24	23	A7
$\overline{CS2}$	26	25	A6
—	28	27	A5
—	30	29	A4
—	32	31	A3
—	34	33	A2
A8	36	35	A1
A8	38	37	A0
TTL V. OUT	40	39	+5 V. RAM
TTL V. IN	42	41	—
C. SYNC. IN	44	43	VDO
H. SYNC. IN	46	45	—
V. SYNC. IN	48	47	BV
—	50	49	—
—	52	51	—
$\overline{READ}$	54	53	—
$\overline{WRITE}$	56	55	—

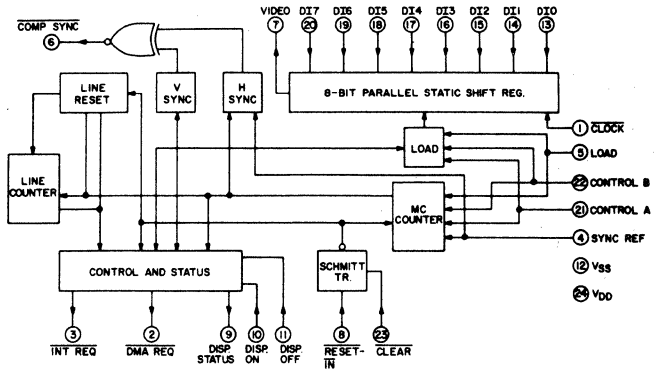


Z09-11

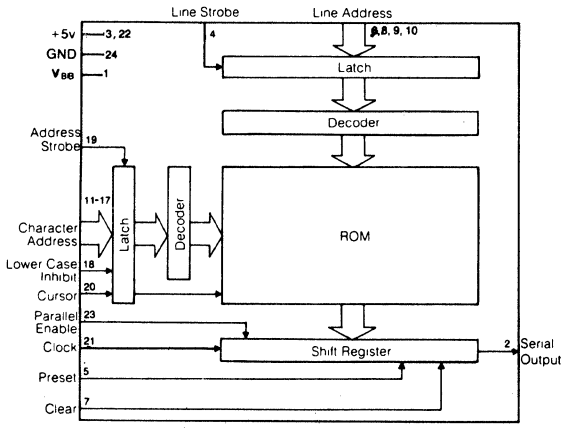




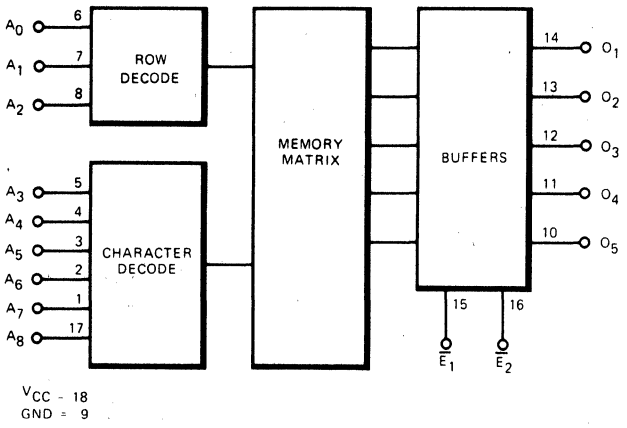
Z09-12

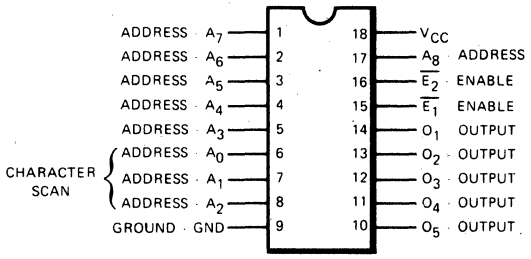


Z09-13



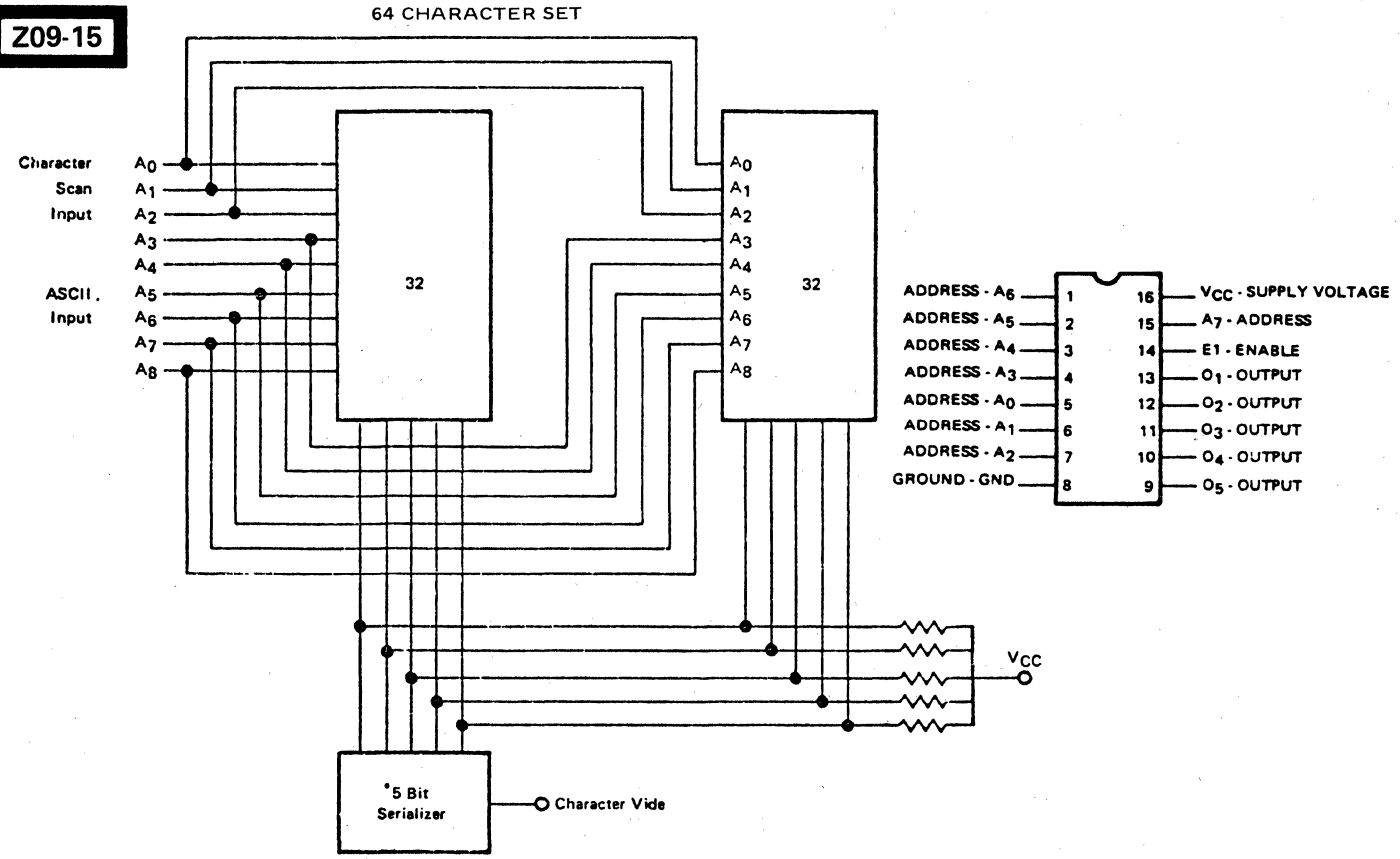
Z09-14



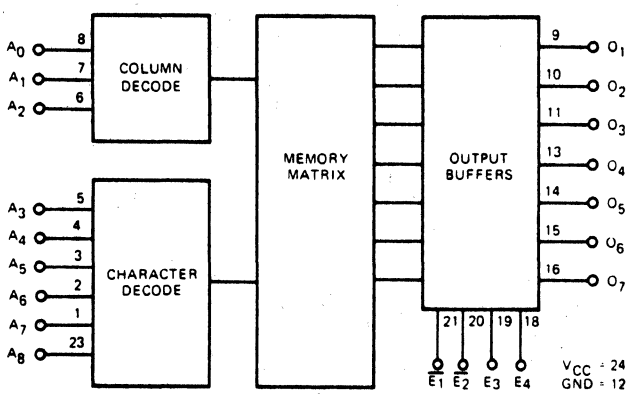


To enable the device, $\overline{E_1}$ and $\overline{E_2}$ must be LOW.

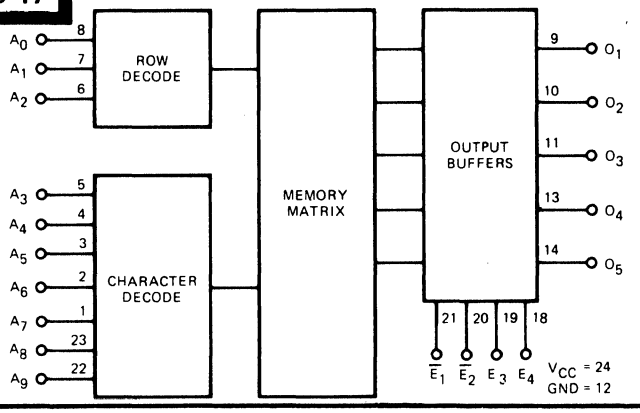
Z09-15



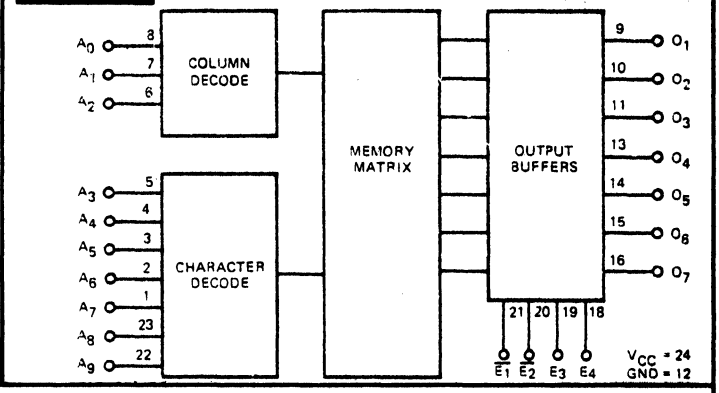
Z09-16



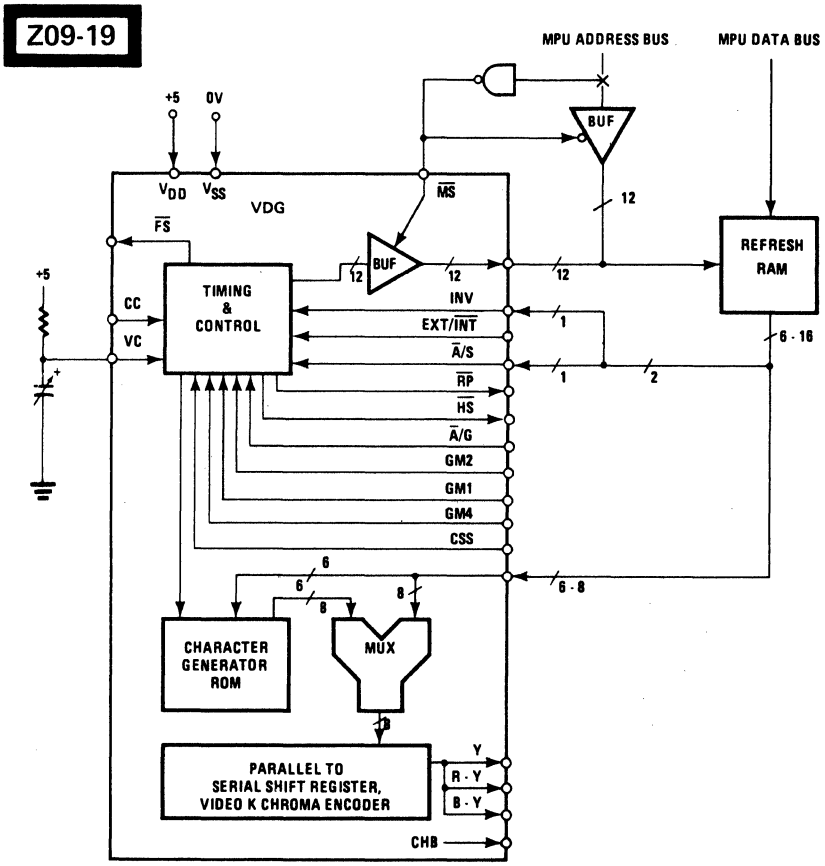
Z09-17

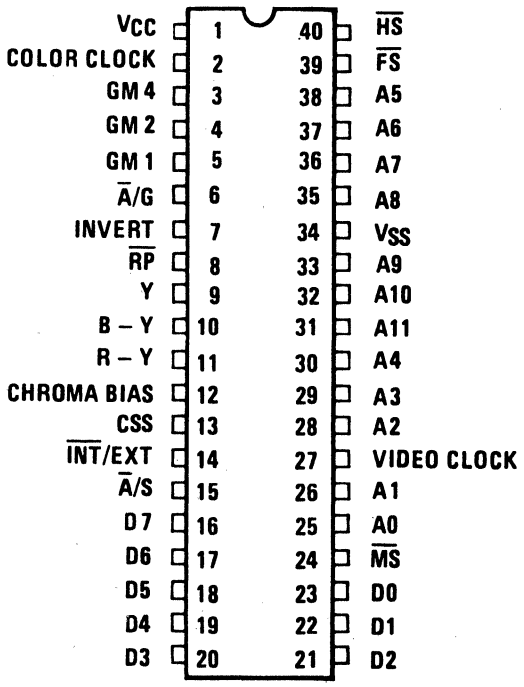


Z09-18

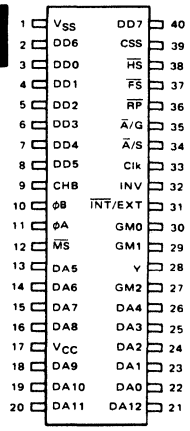


Z09-19

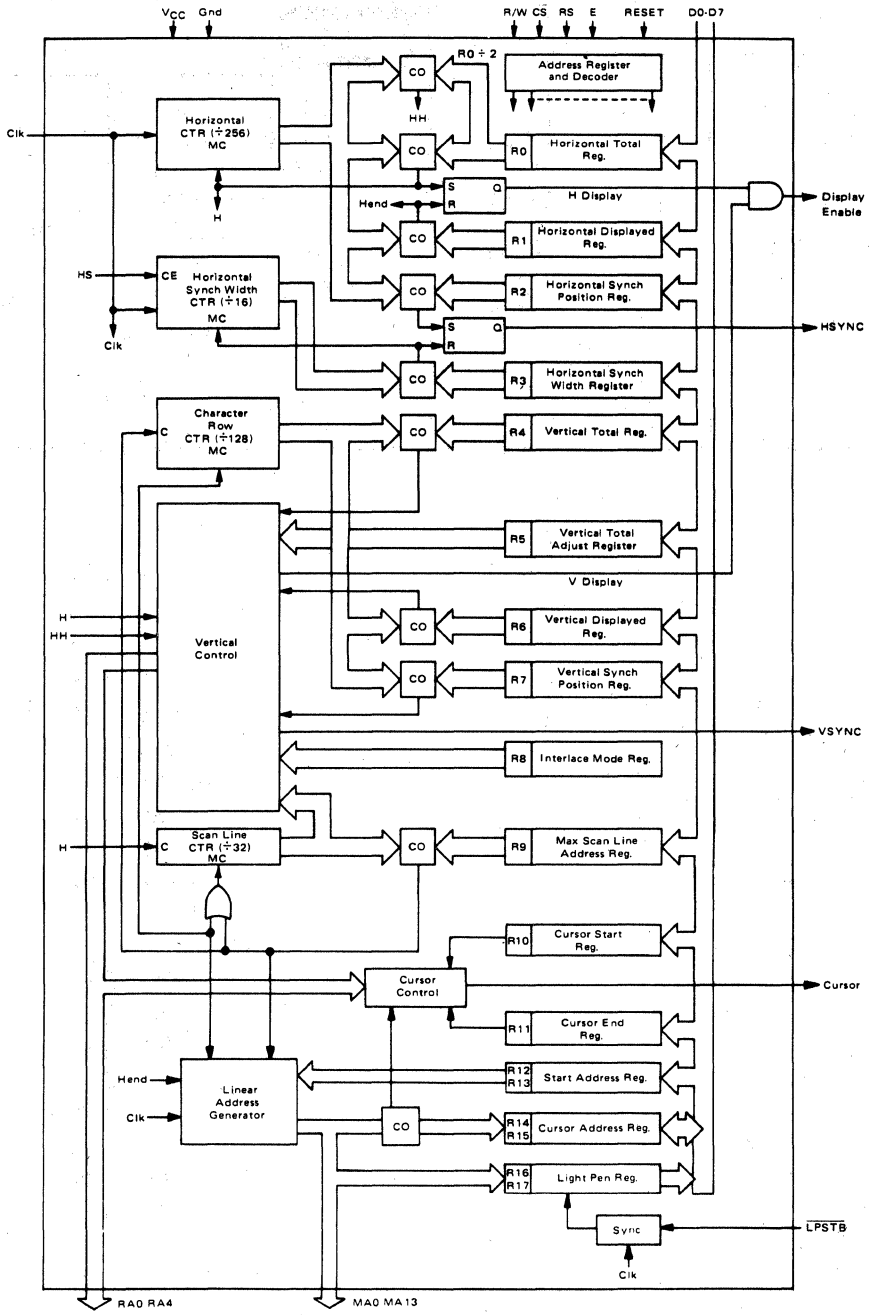


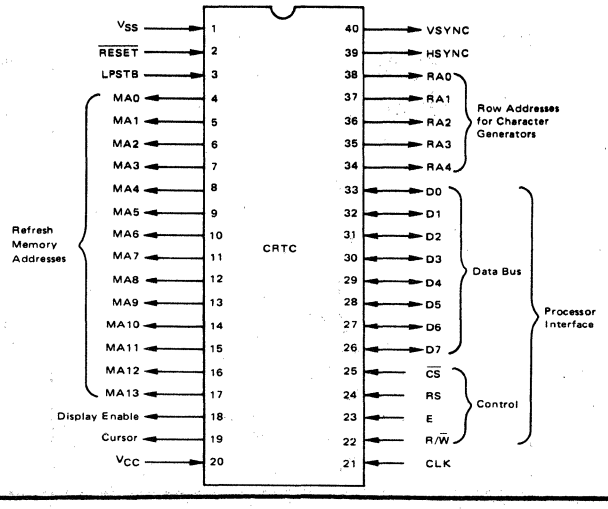


Z09-20

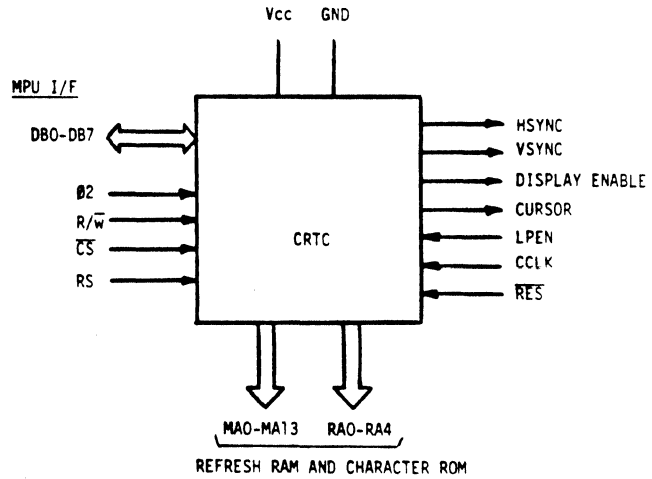


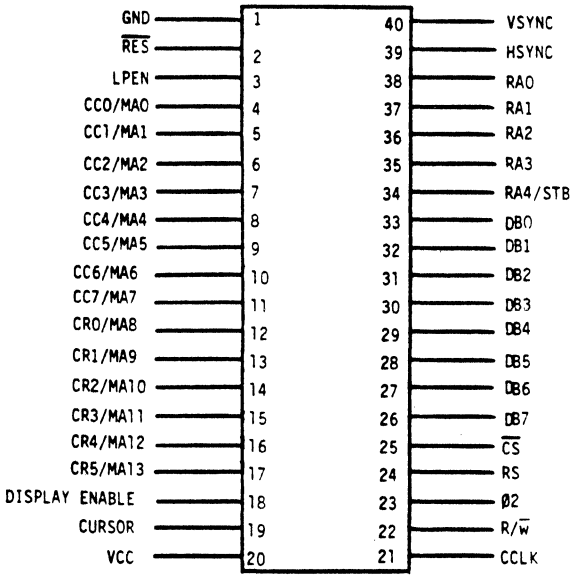
Z09-21


VCC Gnd
R/W CS RS E RESET D0-D7
R0 ÷ 2
Address Register and Decoder
CO
HH
Clk
Horizontal CTR (÷256) MC
H
R0 Horizontal Total Reg.
S Q R
Hend
H Display
Display Enable
R1 Horizontal Displayed Reg.
HS
CE Horizontal Synch Width CTR (÷16) MC
R2 Horizontal Synch Position Reg.
HSYNC
R3 Horizontal Synch Width Register
Character Row CTR (÷128) MC
R4 Vertical Total Reg.
R5 Vertical Total Adjust Register
V Display
Vertical Control
R6 Vertical Displayed Reg.
R7 Vertical Synch Position Reg.
VSYNC
R8 Interlace Mode Reg.
Scan Line CTR (÷32) MC
R9 Max Scan Line Address Reg.
R10 Cursor Start Reg.
Cursor Control
Cursor
R11 Cursor End Reg.
Linear Address Generator
R12 R13 Start Address Reg.
R14 R15 Cursor Address Reg.
R16 R17 Light Pen Reg.
Sync
LPSTB
RA0 RA4
MA0 MA13

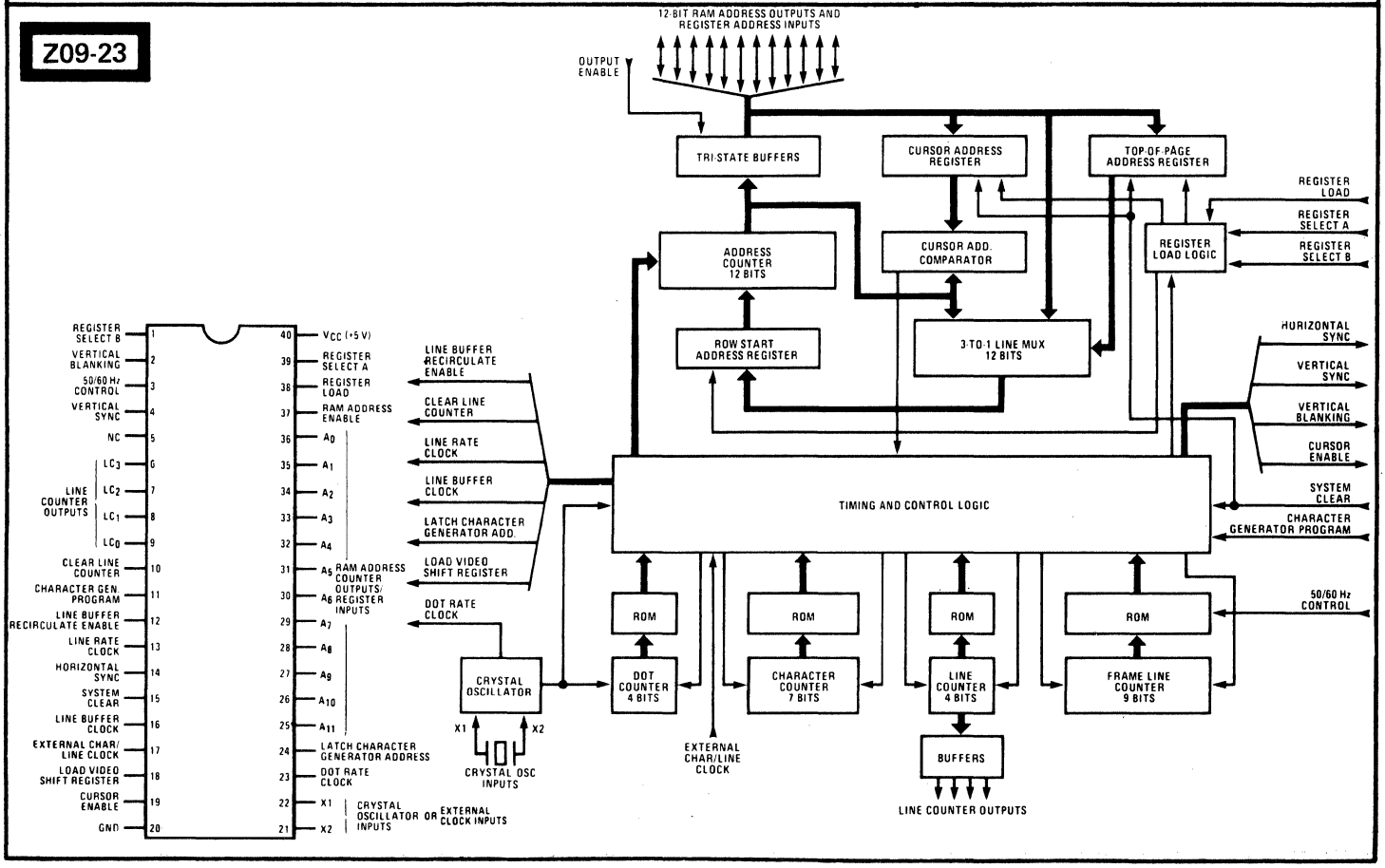

VSS 1
RESET 2
LPSTB 3
MA0 4
MA1 5
MA2 6
MA3 7
MA4 8
MA5 9
MA6 10
MA7 11
MA8 12
MA9 13
MA10 14
MA11 15
MA12 16
MA13 17
Display Enable 18
Cursor 19
VCC 20
CRTC
40 VSYNC
39 HSYNC
38 RA0
37 RA1
36 RA2
35 RA3
34 RA4
33 D0
32 D1
31 D2
30 D3
29 D4
28 D5
27 D6
26 D7
25 CS
24 RS
23 E
22 R/W
21 CLK
Refresh Memory Addresses
Row Addresses for Character Generators
Data Bus
Control
Processor Interface

Z09-22


Vcc
GND
MPU I/F
DB0-DB7
Ø2
R/W
CS
RS
CRTC
HSYNC
VSYNC
DISPLAY ENABLE
CURSOR
LPEN
CCLK
RES
MA0-MA13
RA0-RA4
REFRESH RAM AND CHARACTER ROM


GND 1
RES 2
LPEN 3
CC0/MA0 4
CC1/MA1 5
CC2/MA2 6
CC3/MA3 7
CC4/MA4 8
CC5/MA5 9
CC6/MA6 10
CC7/MA7 11
CR0/MA8 12
CR1/MA9 13
CR2/MA10 14
CR3/MA11 15
CR4/MA12 16
CR5/MA13 17
DISPLAY ENABLE 18
CURSOR 19
VCC 20
40 VSYNC
39 HSYNC
38 RA0
37 RA1
36 RA2
35 RA3
34 RA4/STB
33 DB0
32 DB1
31 DB2
30 DB3
29 DB4
28 DB5
27 DB6
26 DB7
25 CS
24 RS
23 Ø2
22 R/W
21 CCLK

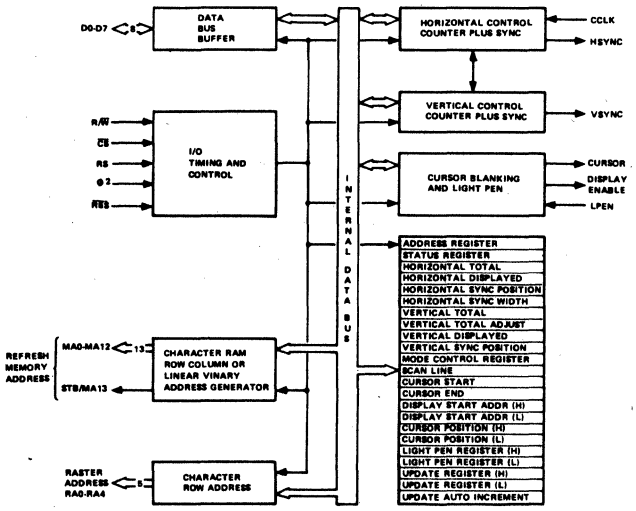
Z09-23

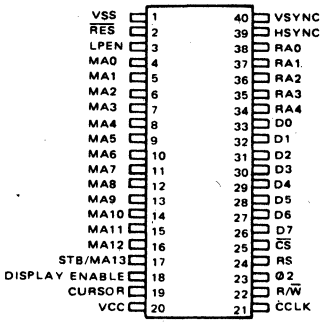

12-BIT RAM ADDRESS OUTPUTS AND REGISTER ADDRESS INPUTS
OUTPUT ENABLE
TRI-STATE BUFFERS
CURSOR ADDRESS REGISTER
TOP-OF-PAGE ADDRESS REGISTER
REGISTER LOAD
REGISTER SELECT A
REGISTER SELECT B
REGISTER LOAD LOGIC
ADDRESS COUNTER 12 BITS
CURSOR ADD. COMPARATOR
ROW START ADDRESS REGISTER
3-TO-1 LINE MUX 12 BITS
HORIZONTAL SYNC
VERTICAL SYNC
VERTICAL BLANKING
CURSOR ENABLE
SYSTEM CLEAR
CHARACTER GENERATOR PROGRAM
TIMING AND CONTROL LOGIC
50/60 Hz CONTROL
ROM
DOT COUNTER 4 BITS
CHARACTER COUNTER 7 BITS
LINE COUNTER 4 BITS
FRAME LINE COUNTER 9 BITS
BUFFERS
LINE COUNTER OUTPUTS
CRYSTAL OSCILLATOR
X1
X2
40Ø
CRYSTAL OSC INPUTS
EXTERNAL CHAR/LINE CLOCK
REGISTER SELECT B 1
VERTICAL BLANKING 2
50/60 Hz CONTROL 3
VERTICAL SYNC 4
NC 5
LC3 6
LC2 7
LC1 8
LC0 9
LINE COUNTER OUTPUTS
CLEAR LINE COUNTER 10
CHARACTER GEN. PROGRAM 11
LINE BUFFER RECIRCULATE ENABLE 12
LINE RATE CLOCK 13
HORIZONTAL SYNC 14
SYSTEM CLEAR 15
LINE BUFFER CLOCK 16
EXTERNAL CHAR/ LINE CLOCK 17
LOAD VIDEO SHIFT REGISTER 18
CURSOR ENABLE 19
GND 20
40 VCC (+5 V)
39 REGISTER SELECT A
38 REGISTER LOAD
37 RAM ADDRESS ENABLE
36 A0
35 A1
34 A2
33 A3
32 A4
31 A5
30 A6
RAM ADDRESS COUNTER OUTPUTS/ REGISTER INPUTS
29 A7
28 A8
27 A9
26 A10
25 A11
24 LATCH CHARACTER GENERATOR ADDRESS
23 DOT RATE CLOCK
22 X1
21 X2
CRYSTAL OSCILLATOR OR EXTERNAL CLOCK INPUTS
LINE BUFFER RECIRCULATE ENABLE
CLEAR LINE COUNTER
LINE RATE CLOCK
LINE BUFFER CLOCK
LATCH CHARACTER GENERATOR ADD.
LOAD VIDEO SHIFT REGISTER
DOT RATE CLOCK

19. LOGIC/BLOCK DRAWINGS

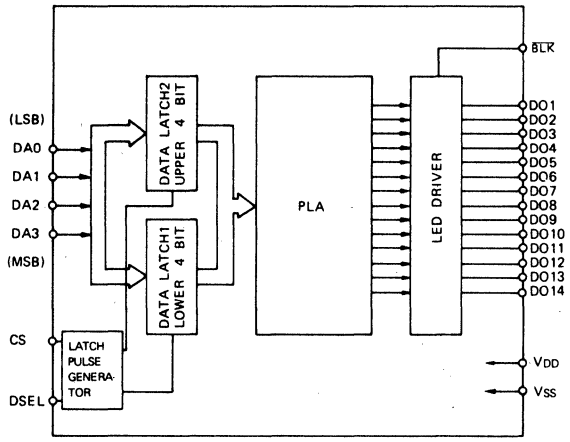
IN DRAWING NUMBER SEQUENCE

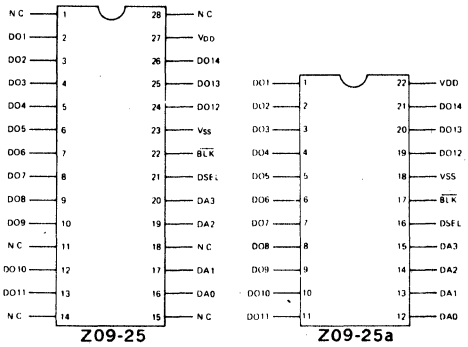
Z09-24





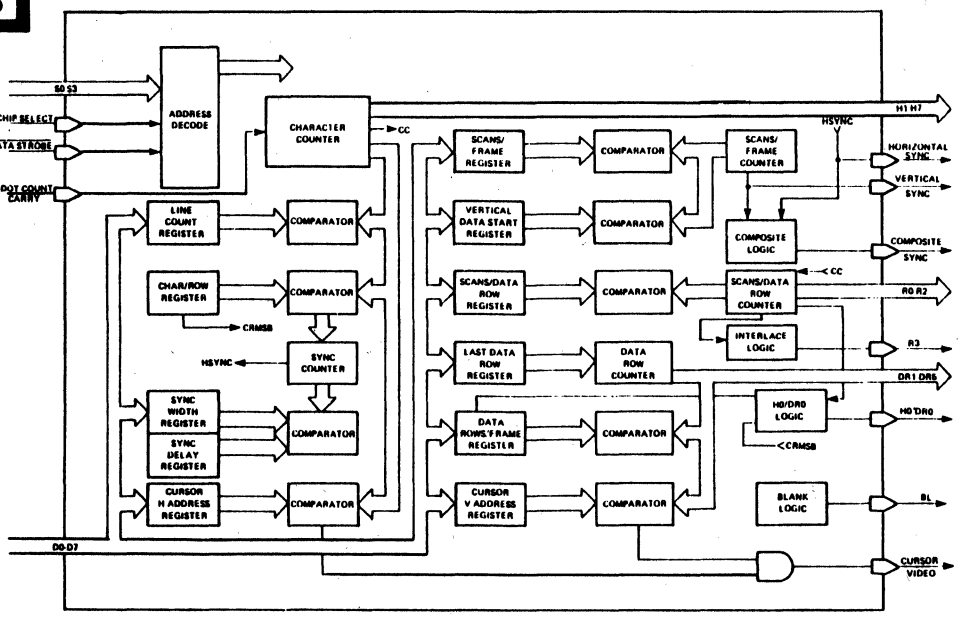
Z09-25

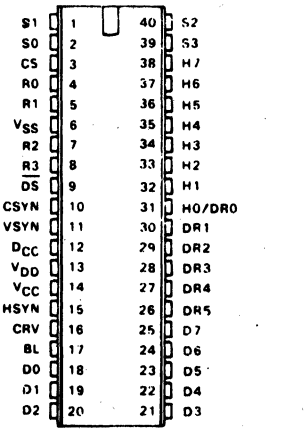




* Note: Chip-select input allows selection of an individual package in common input data system (Option).

Z09-26

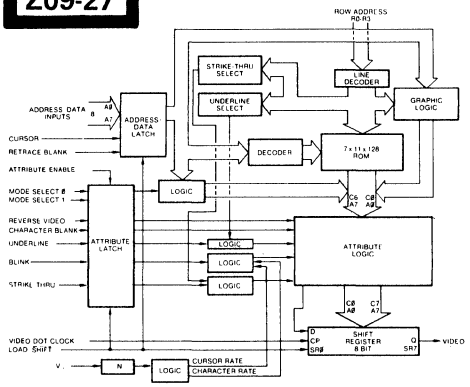




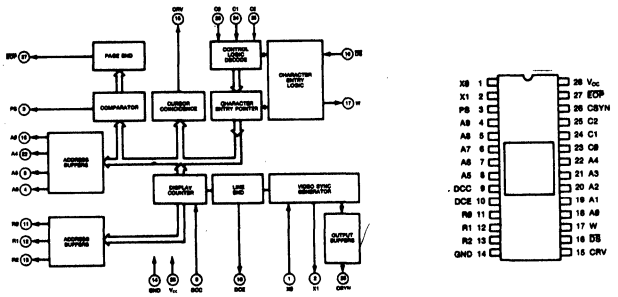
29. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

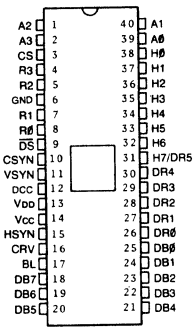
Z09-27

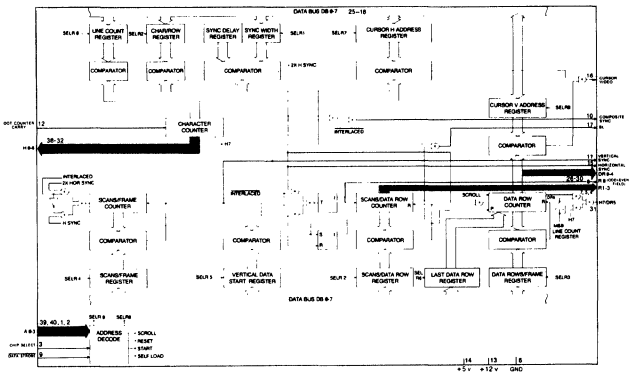


Z09-28

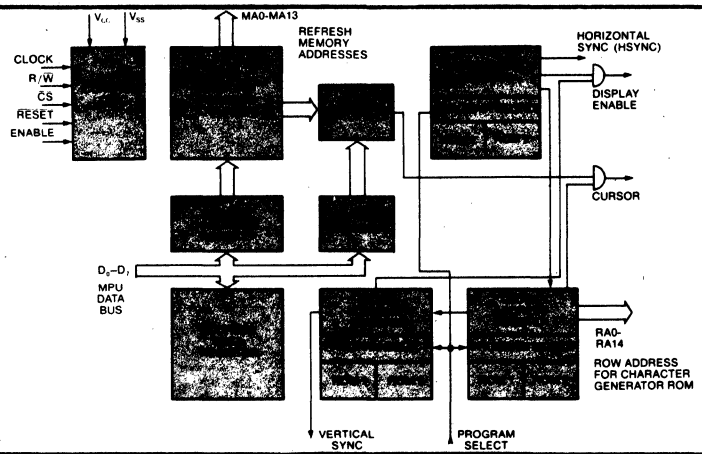


Z09-29

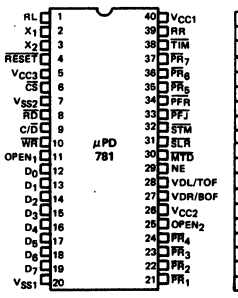




Z09-30



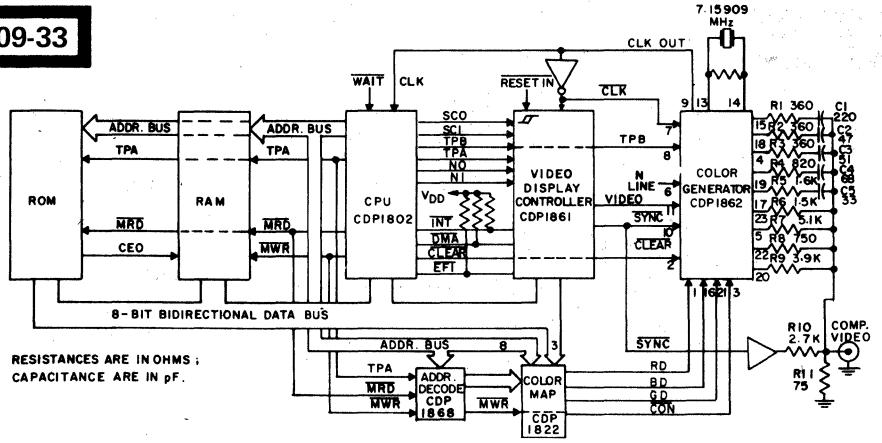
Z09-32



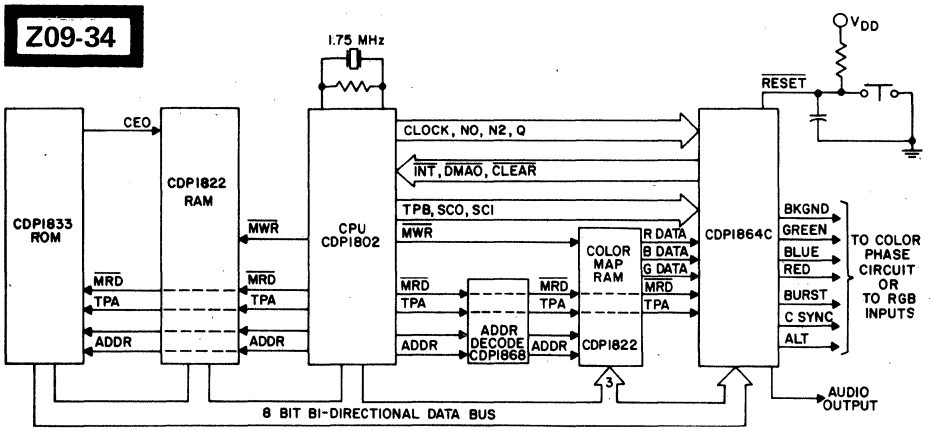
PIN NAMES

RL	Reset Signal (L)
RR	Reset Signal (R)
X_1, X_2	Crystal Inputs
RESET	Reset
CS	Chip Select
RD	Read
C/D	Command/Data
WR	Write
D_{0-7}	Data Bus
PR_1-PR_7	Print Solenoids
VDR/BOF	Validation (R)/BOF Sensor
VDL/TOF	Validation (L)/TOF Sensor
NE	Low Paper Detector
MTD	Motor Drive
SLR	Slip Release
STM	Stamp
PFJ	Paper Feed Journal
PFR	Paper Feed Receipt
TIM	Timing Signal

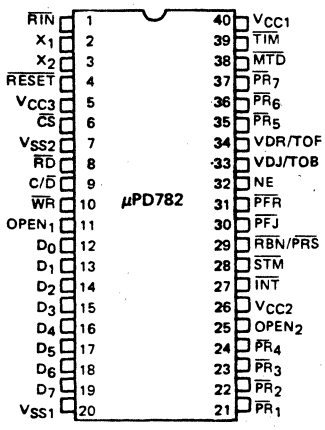
Z09-33



Z09-34

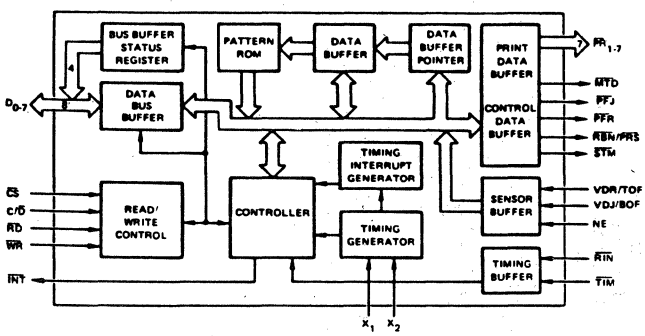


Z09-35

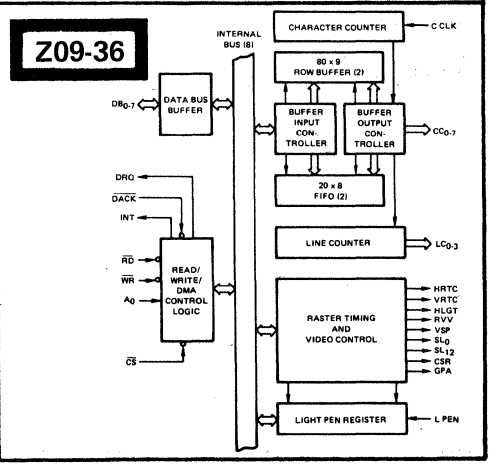


PIN NAMES

$\overline{RIN}$	Reset In
X_1 X_2	Crystal Inputs
$\overline{RESET}$	Reset
V_{CC1-3}	DC Power
V_{SS1-2}	Signal Ground
$\overline{CS}$	Chip Select
$\overline{RD}$	Read
C/$\overline{D}$	Command/Data
$\overline{WR}$	Write
$OPEN_{1-2}$	No Connection
D_0-D_7	Data Bus
$\overline{PR_1}$-$\overline{PR_7}$	Print Solenoids
$\overline{INT}$	Interrupt
$\overline{STM}$	Stamp
$\overline{RBN}$/$\overline{PRS}$	Ribbon/Paper Release
$\overline{PFJ}$	Paper Feed Journal
$\overline{PFR}$	Paper Feed Receipt
NE	Low Paper Detector
VDJ/BOF	Validation J/BOF Sensor
VDR/BOT	Validation R/BOT Sensor
$\overline{MTD}$	Motor Drive
$\overline{TIM}$	Timing Signal



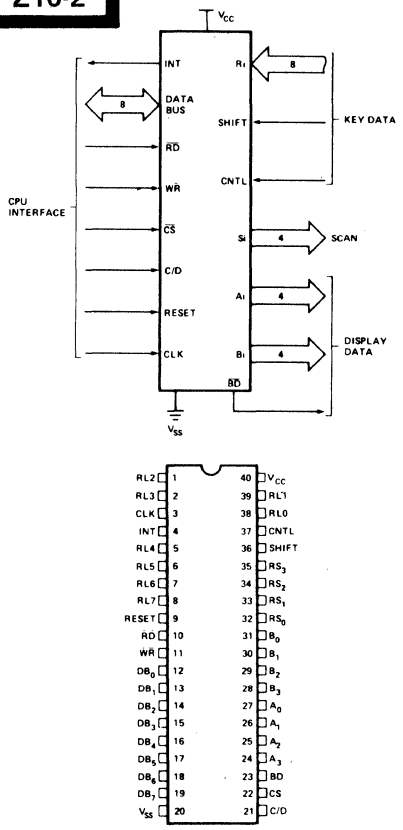
Z09-36



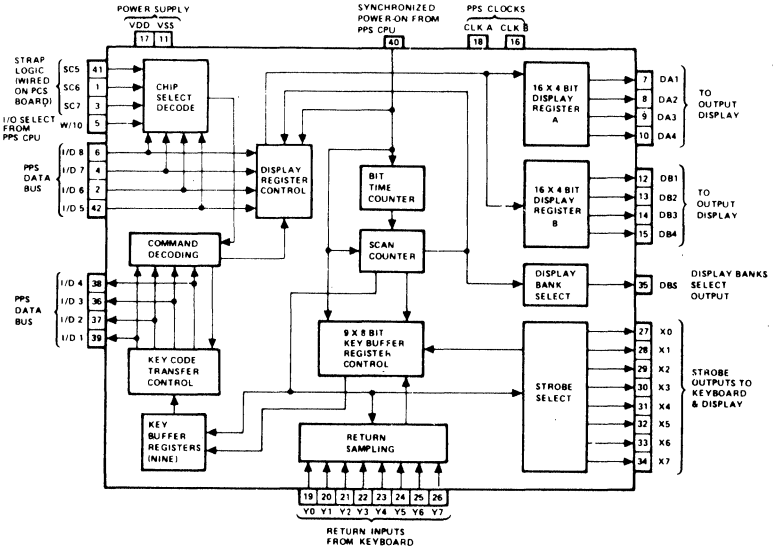
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

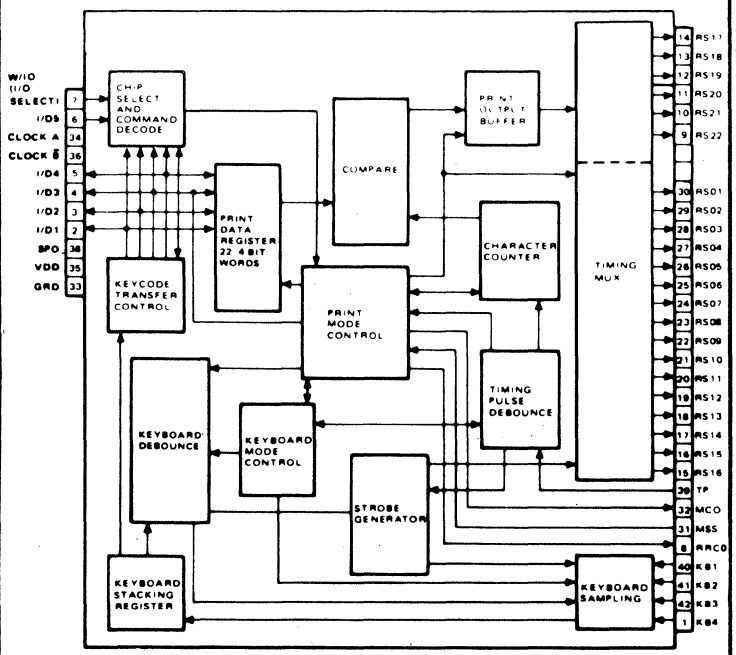
Z10-2



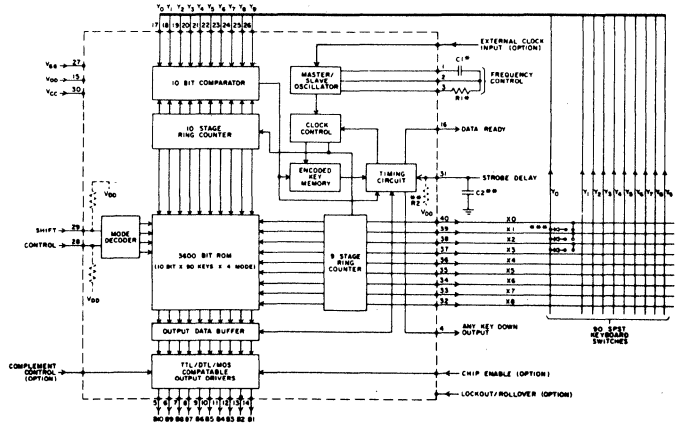
Z10-3



Z10-4

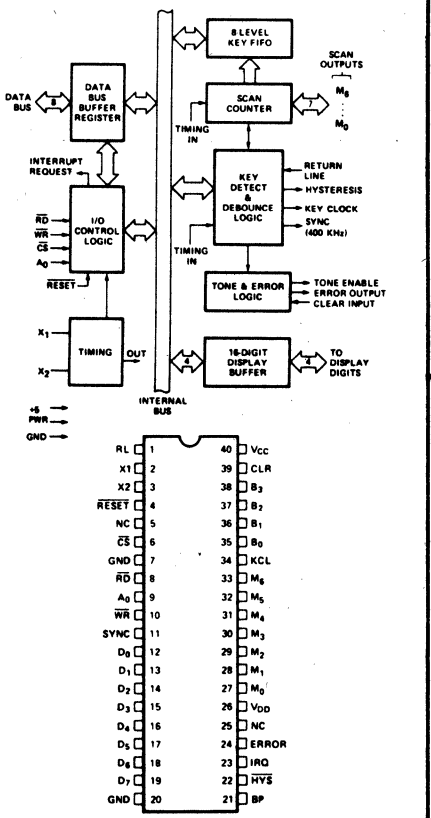


Z10-5

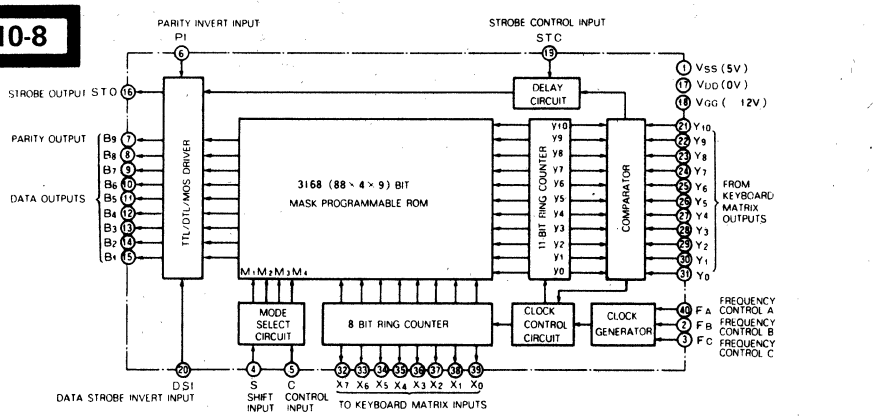


NOTE: REFER TO FIG. 1 FOR OPTION PIN SELECTION.
* R: (100K Ω), C: (45pF) PROVIDES APPROX 50KHz CLOCK FREQ.
** C2 (300nS DELAY/CPF) R2 SUPPLIED INTERNALLY.
*** DIODES NECESSARY FOR COMPLETE 4 KEY ROLLOVER OPERATION.

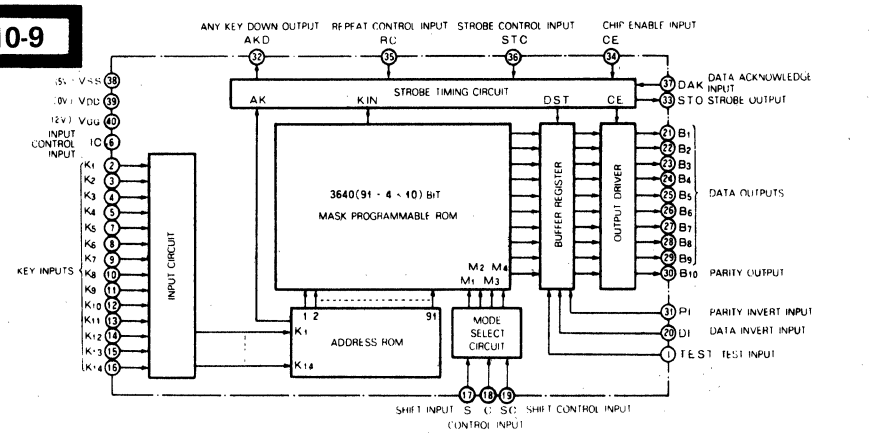
Z10-7



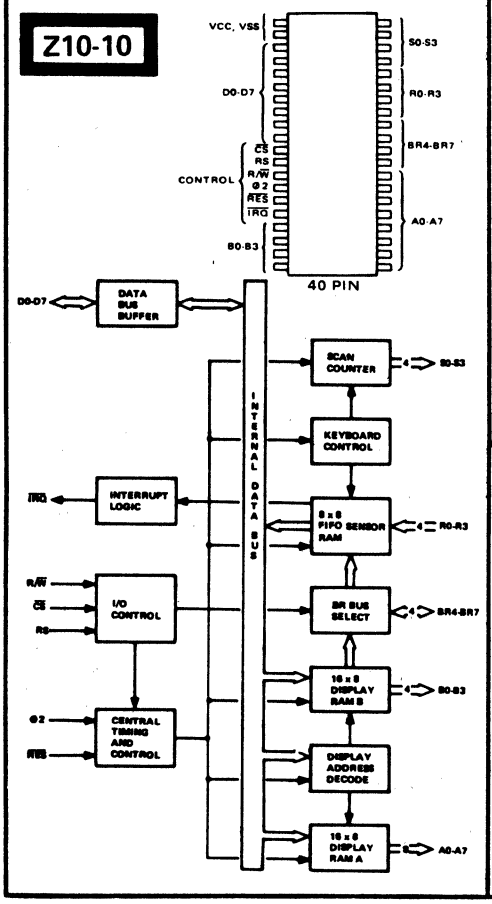
Z10-8



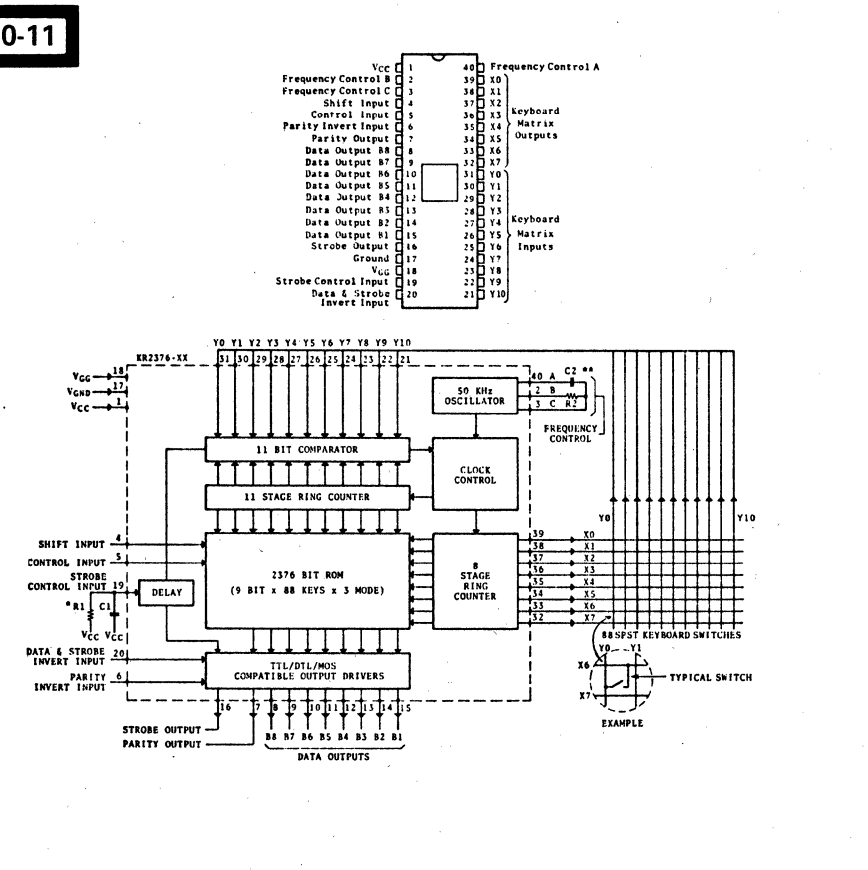
Z10-9



Z10-10



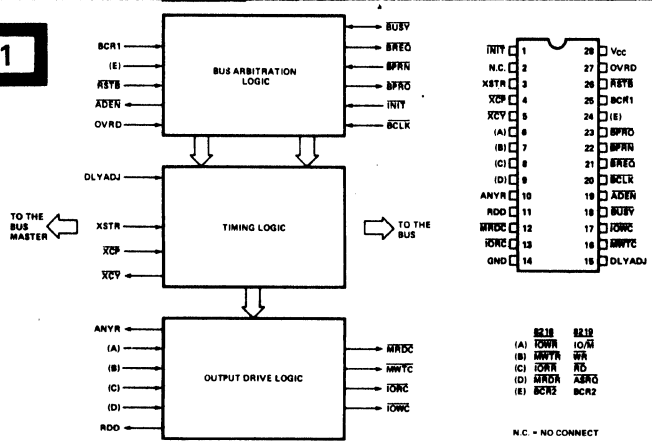
Z10-11



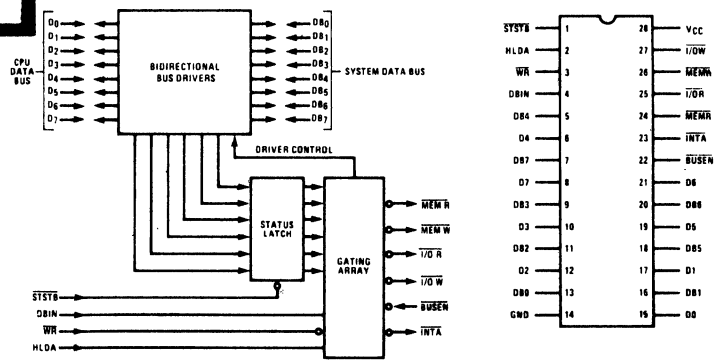
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

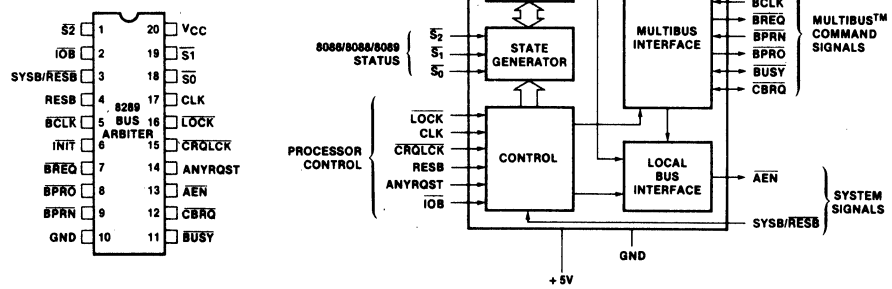
Z11-1



Z11-2



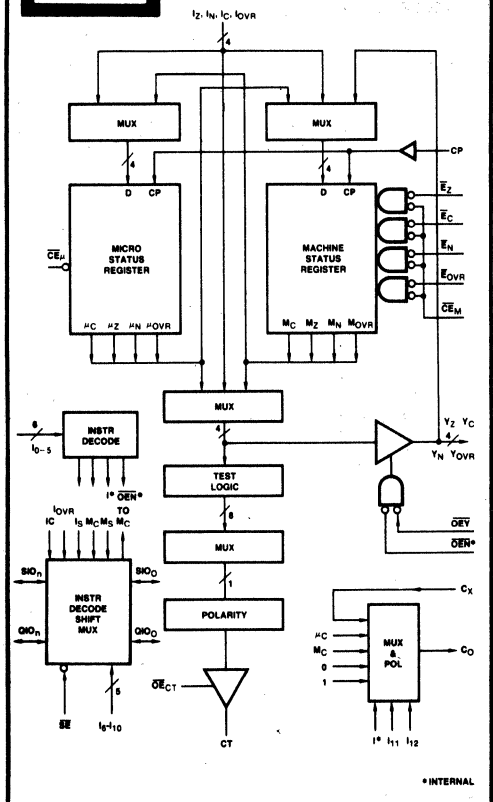
Z11-3



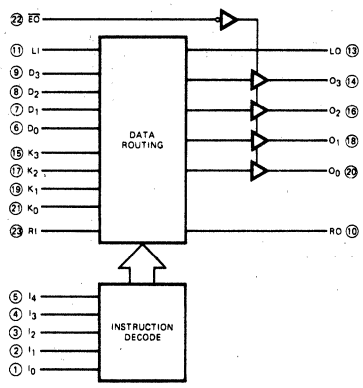
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

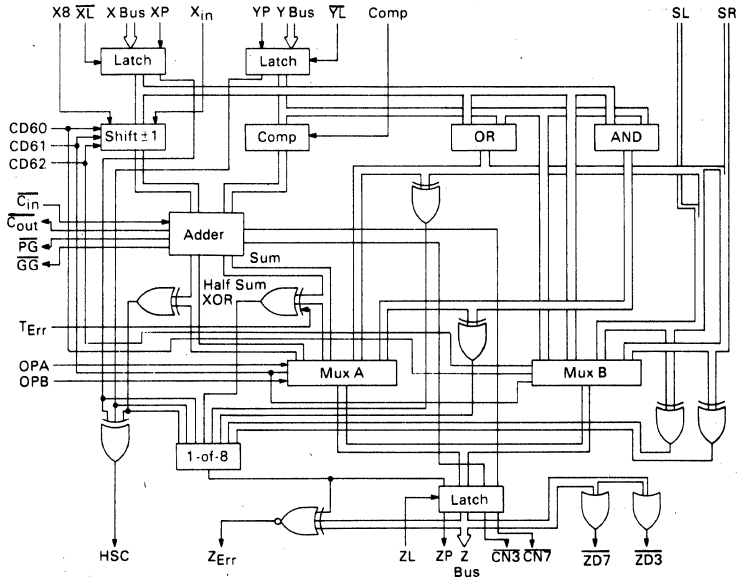
Z12-1



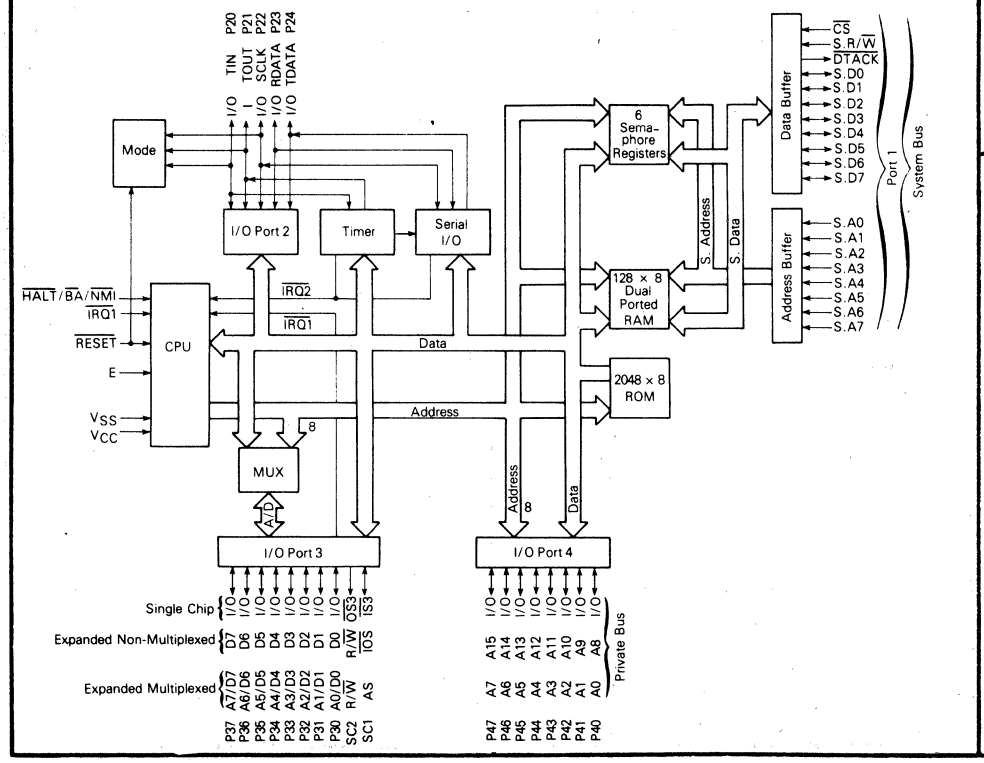
Z12-2



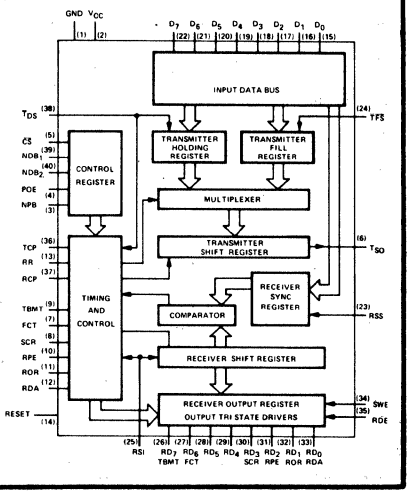
Z12-3



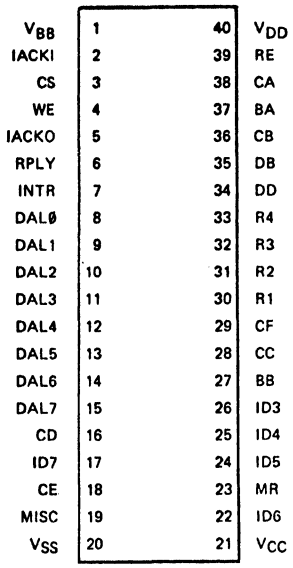
Z13-1

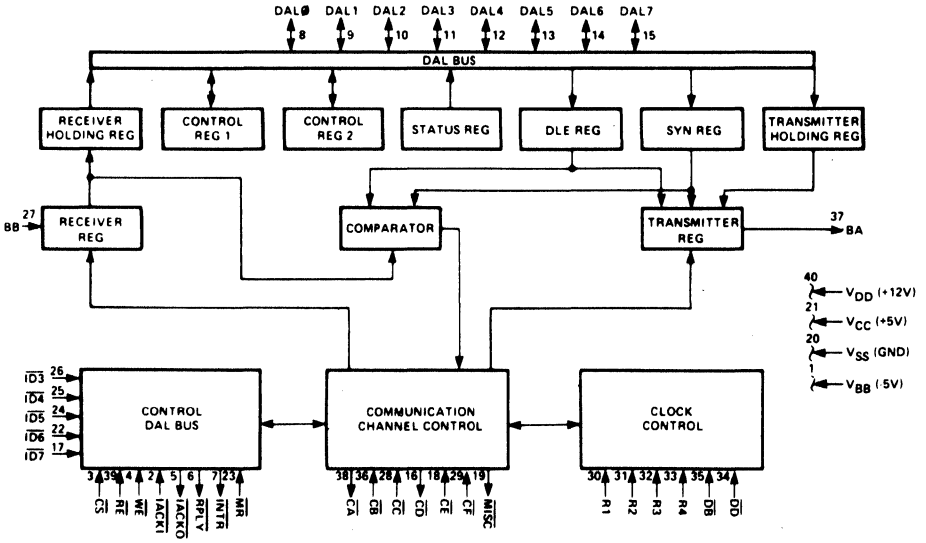


Z20-1

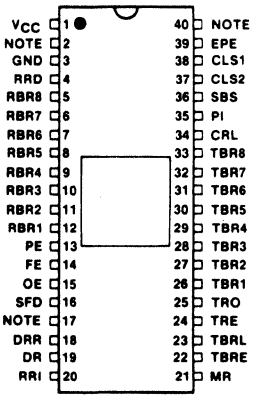


Z20-3



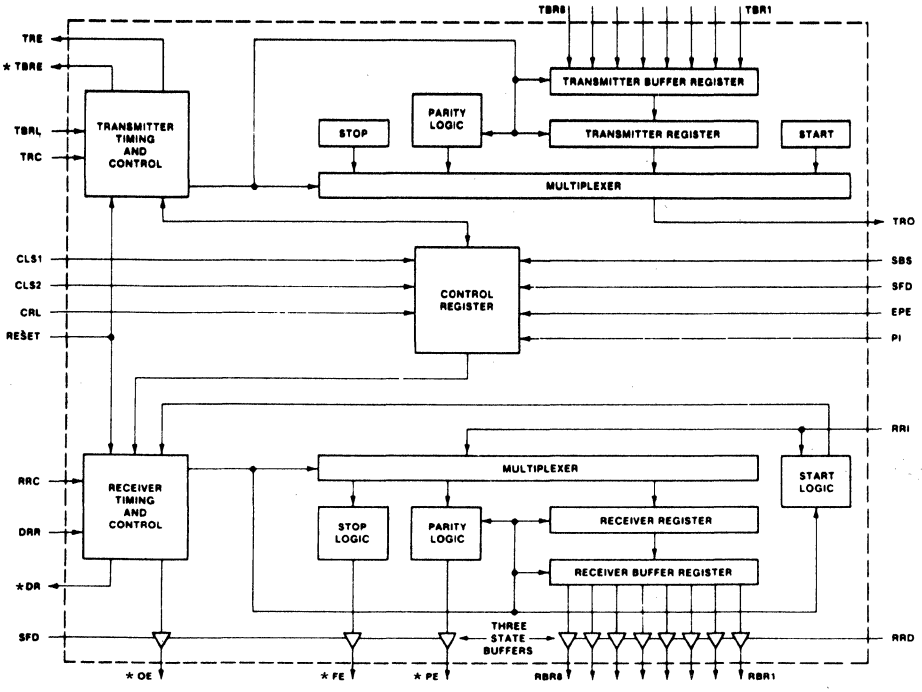


Z20-4



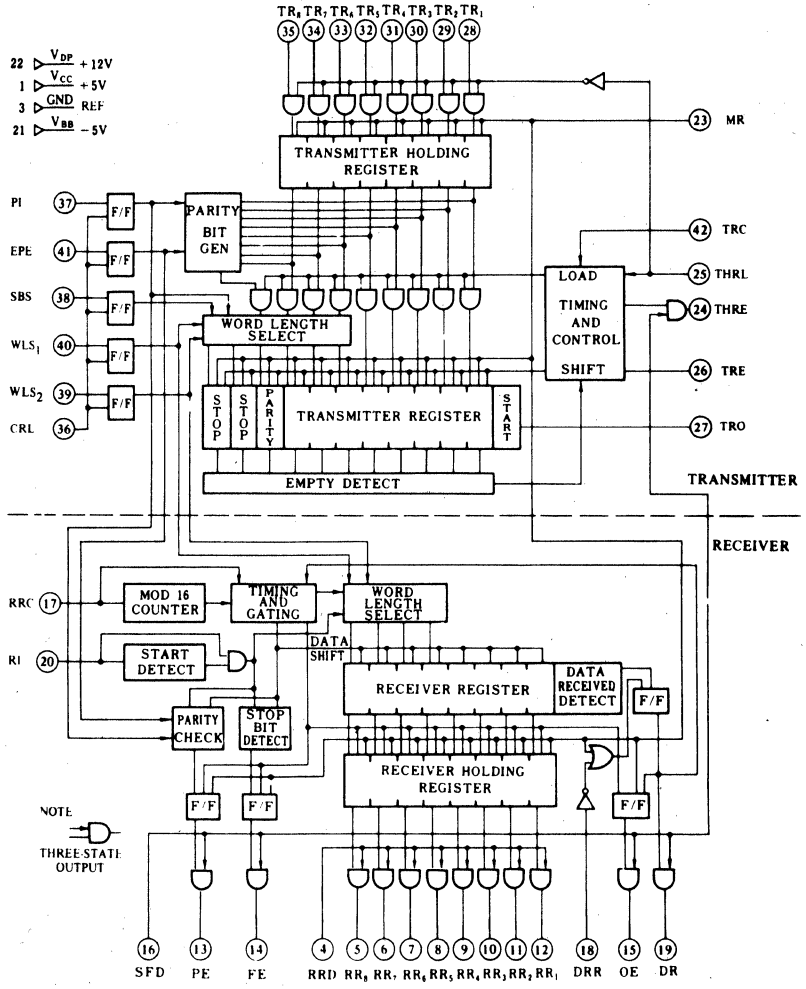
Z20-4a

PIN	Z20-4	W/XTAL	W/EXT CLOCK
2	N/C	DIVIDE CONTROL	DIVIDE CONTROL
17	RRC	XTAL	EXTERNAL CLOCK INPUT
40	TRC	XTAL	GND

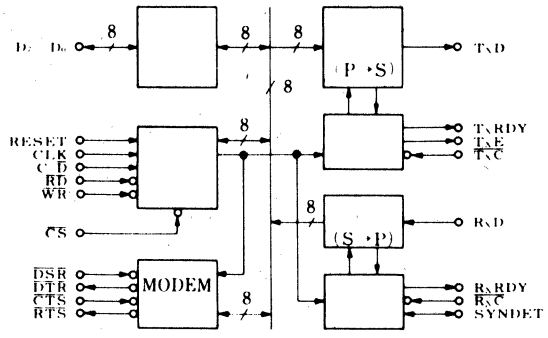


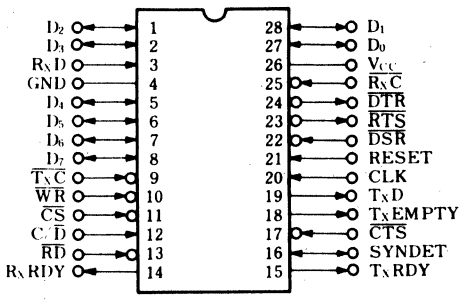
* THESE OUTPUTS ARE THRU STATE FOR Z20-4 OR ALWAYS ACTIVE FOR Z20-4a.

Z20-5

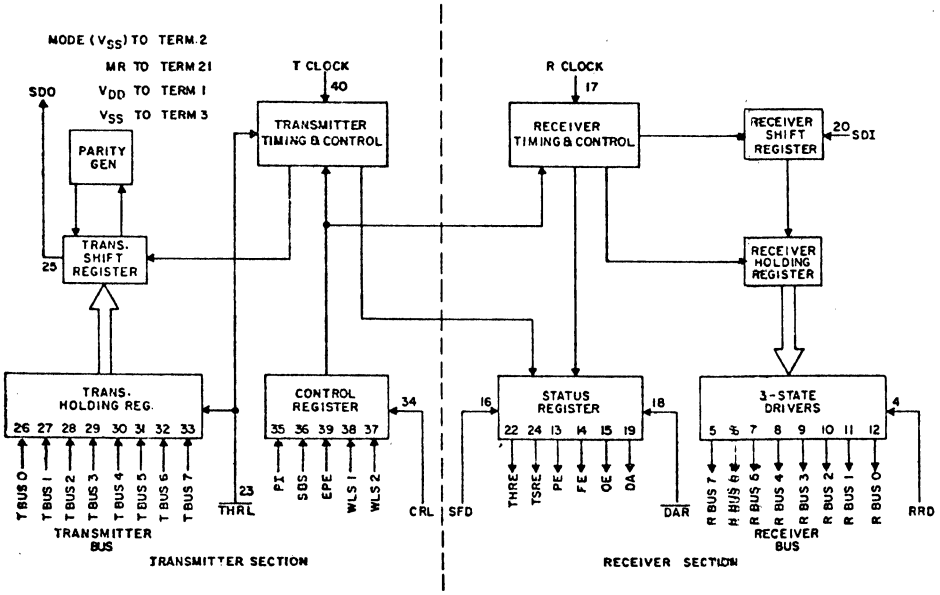

TR8 TR7 TR6 TR5 TR4 TR3 TR2 TR1
35 34 33 32 31 30 29 28
22 VDD +12V
1 VCC +5V
3 GND REF
21 VBB −5V
23 MR
TRANSMITTER HOLDING REGISTER
PI 37
EPE 41
SBS 38
WLS1 40
WLS2 39
CRL 36
F/F
PARITY BIT GEN
WORD LENGTH SELECT
LOAD
TIMING AND CONTROL
SHIFT
42 TRC
25 THRL
24 THRE
26 TRE
27 TRO
STOP
STOP
PARITY
TRANSMITTER REGISTER
START
EMPTY DETECT
TRANSMITTER
RECEIVER
RRC 17
RI 20
MOD 16 COUNTER
TIMING AND GATING
WORD LENGTH SELECT
START DETECT
DATA SHIFT
RECEIVER REGISTER
DATA RECEIVED DETECT
PARITY CHECK
STOP BIT DETECT
RECEIVER HOLDING REGISTER
NOTE
THREE-STATE OUTPUT
16 SFD
13 PE
14 FE
4 RRD
5 RR8
6 RR7
7 RR6
8 RR5
9 RR4
10 RR3
11 RR2
12 RR1
18 DRR
15 OE
19 DR

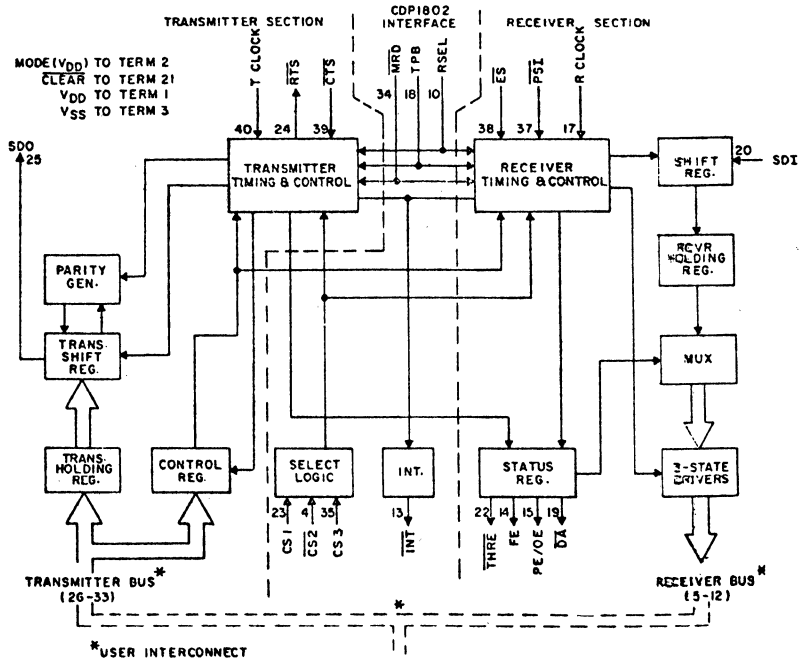
Z20-6


D7 D0
8
(P→S)
TxD
RESET
CLK
C/D
RD
WR
CS
TxRDY
TxE
TxC
(S→P)
RxD
DSR
DTR
CTS
RTS
MODEM
RxRDY
RxC
SYNDET

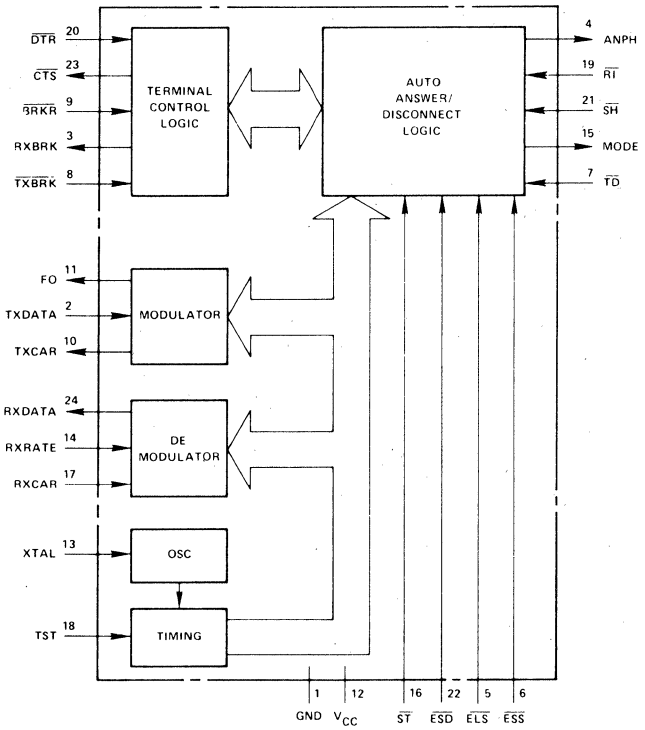

D2 1
D3 2
RxD 3
GND 4
D4 5
D5 6
D6 7
D7 8
TxC 9
WR 10
CS 11
C/D 12
RD 13
RxRDY 14
28 D1
27 D0
26 VCC
25 RxC
24 DTR
23 RTS
22 DSR
21 RESET
20 CLK
19 TxD
18 TxEMPTY
17 CTS
16 SYNDET
15 TxRDY

Z20-7

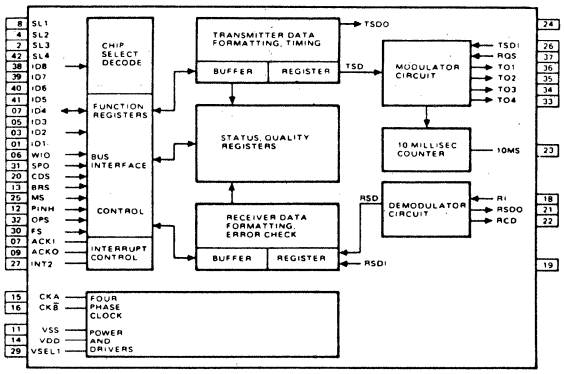

MODE (V_{SS}) TO TERM 2
MR TO TERM 21
V_{DD} TO TERM 1
V_{SS} TO TERM 3
SDO
T CLOCK
40
R CLOCK
17
PARITY GEN
TRANSMITTER TIMING & CONTROL
RECEIVER TIMING & CONTROL
RECEIVER SHIFT REGISTER
20
SDI
TRANS. SHIFT REGISTER
25
RECEIVER HOLDING REGISTER
TRANS. HOLDING REG.
26 27 28 29 30 31 32 33
CONTROL REGISTER
35 36 39 38 37
34
STATUS REGISTER
16
22 24 13 14 15 19
18
3-STATE DRIVERS
4
5 6 7 8 9 10 11 12
T BUS 0
T BUS 1
T BUS 2
T BUS 3
T BUS 4
T BUS 5
T BUS 6
T BUS 7
TRANSMITTER BUS
23
THRL
PI
SOS
EPE
WLS 1
WLS 2
CRL
SFD
THRE
TSRE
PE
FE
OE
DA
DAR
R BUS 7
R BUS 6
R BUS 5
R BUS 4
R BUS 3
R BUS 2
R BUS 1
R BUS 0
RRD
RECEIVER BUS
TRANSMITTER SECTION
RECEIVER SECTION


TRANSMITTER SECTION
CDP1802 INTERFACE
RECEIVER SECTION
MODE (V_{DD}) TO TERM 2
$\overline{CLEAR}$ TO TERM 21
V_{DD} TO TERM 1
V_{SS} TO TERM 3
T CLOCK
$\overline{RTS}$
$\overline{CTS}$
$\overline{MRD}$
TPB
RSEL
ES
$\overline{PSI}$
R CLOCK
40 24 39
34 18 10
38 37 17
SDO
25
TRANSMITTER TIMING & CONTROL
RECEIVER TIMING & CONTROL
SHIFT REG.
20
SDI
PARITY GEN.
RCVR HOLDING REG.
TRANS. SHIFT REG.
MUX
TRANS. HOLDING REG.
CONTROL REG.
SELECT LOGIC
INT.
STATUS REG.
3-STATE DRIVERS
23 4 35
13
22 14 15 19
$\overline{CS1}$
$\overline{CS2}$
CS3
$\overline{INT}$
$\overline{THRE}$
FE
PE/OE
$\overline{DA}$
TRANSMITTER BUS* (26-33)
RECEIVER BUS* (5-12)
*USER INTERCONNECT

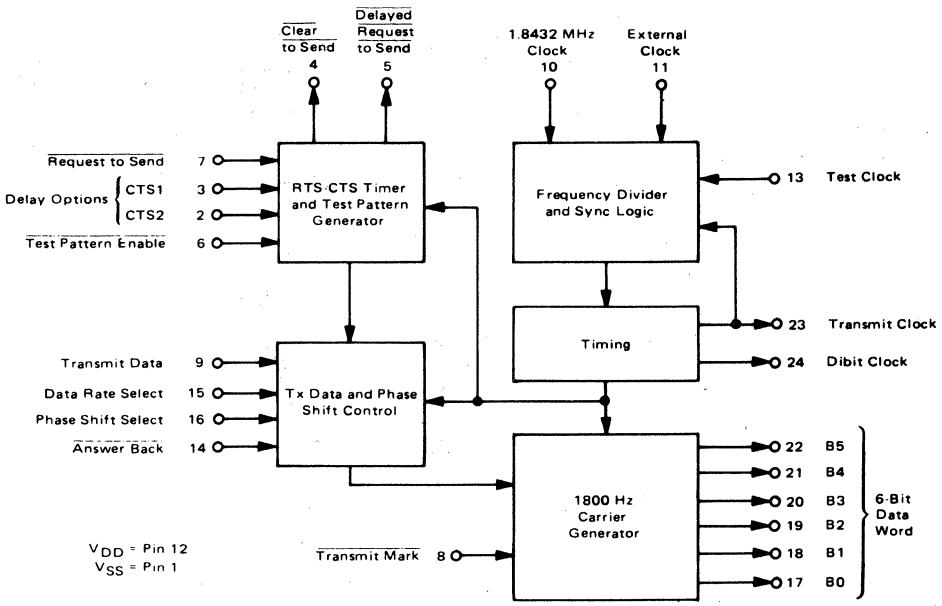
Z20-8



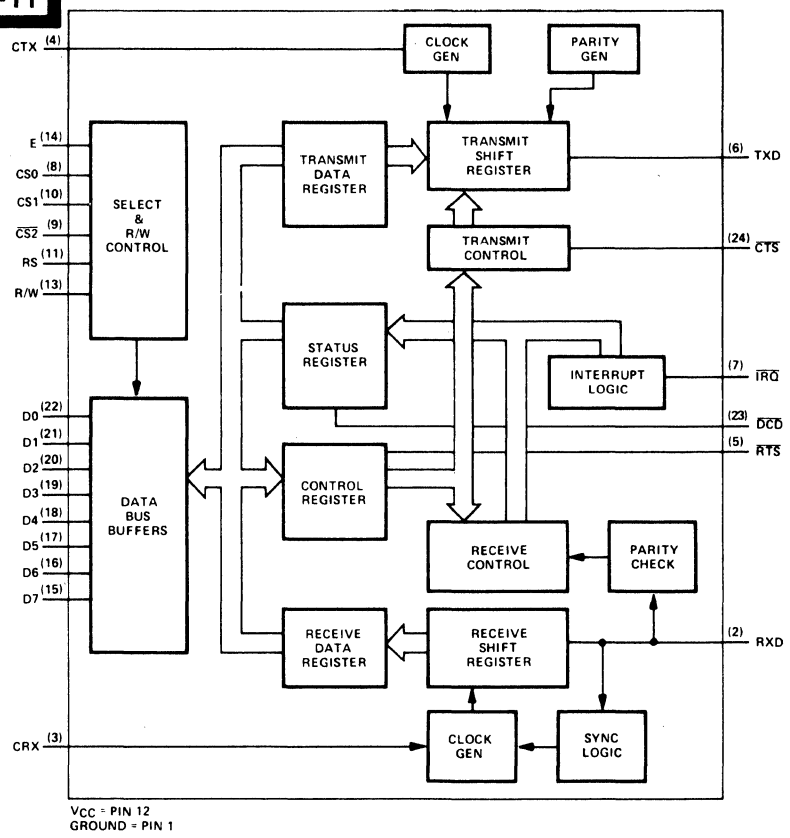
Z20-9



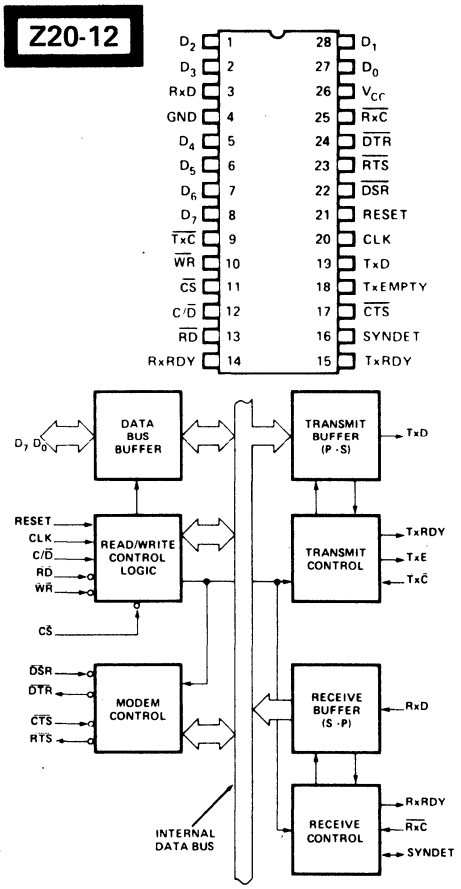
Z20-10



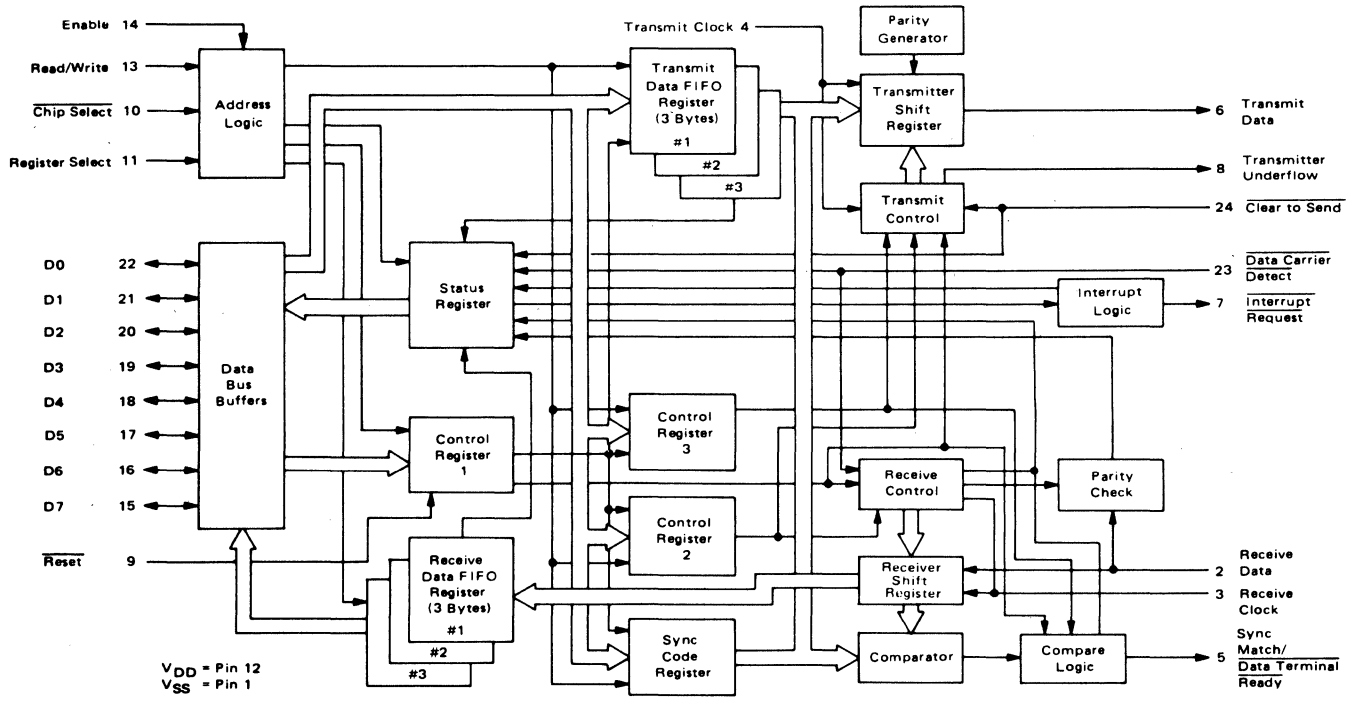
Z20-11



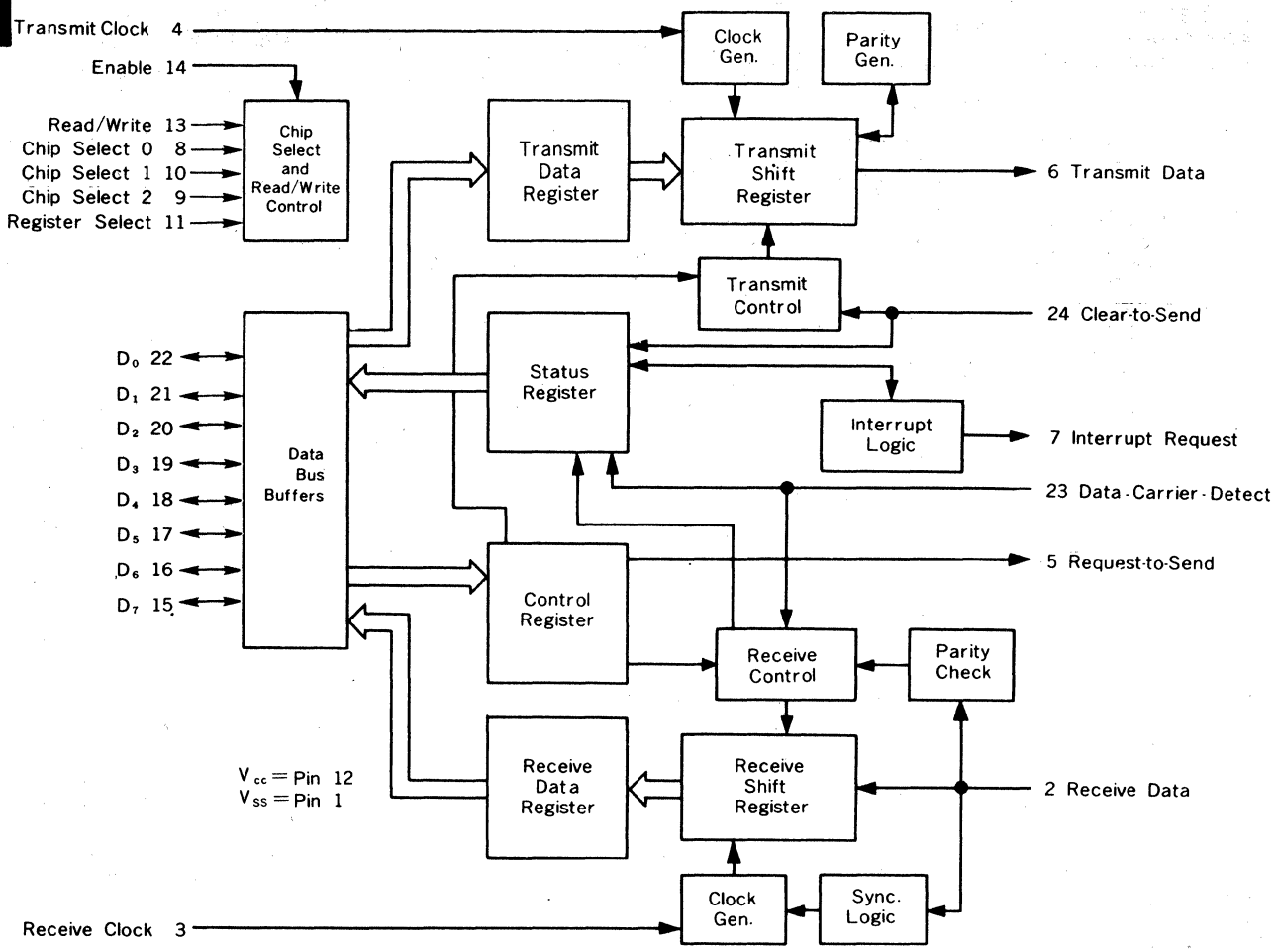
Z20-12



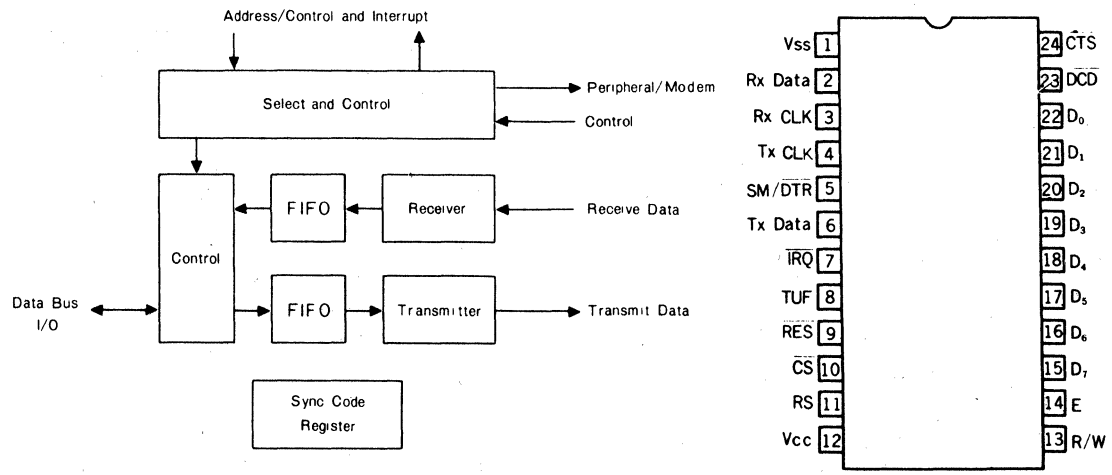
Z20-13



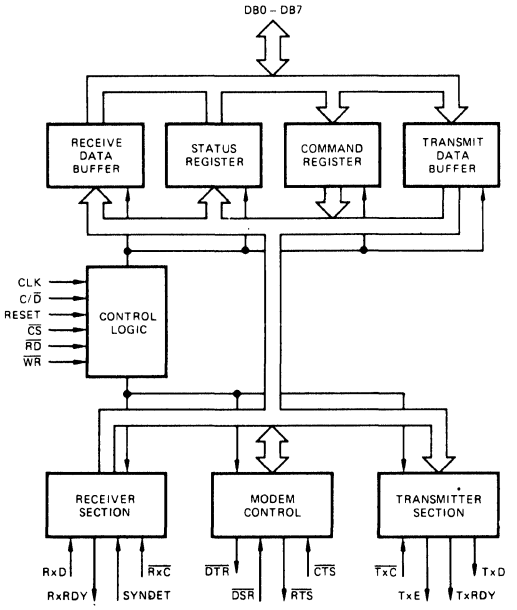
Z20-14


Transmit Clock 4
Enable 14
Read/Write 13
Chip Select 0 8
Chip Select 1 10
Chip Select 2 9
Register Select 11
Chip Select and Read/Write Control
Clock Gen.
Parity Gen.
Transmit Data Register
Transmit Shift Register
6 Transmit Data
Transmit Control
24 Clear-to-Send
Status Register
Interrupt Logic
7 Interrupt Request
23 Data-Carrier-Detect
D0 22
D1 21
D2 20
D3 19
D4 18
D5 17
D6 16
D7 15
Data Bus Buffers
Control Register
5 Request-to-Send
Receive Control
Parity Check
Vcc = Pin 12
Vss = Pin 1
Receive Data Register
Receive Shift Register
2 Receive Data
Clock Gen.
Sync. Logic
Receive Clock 3

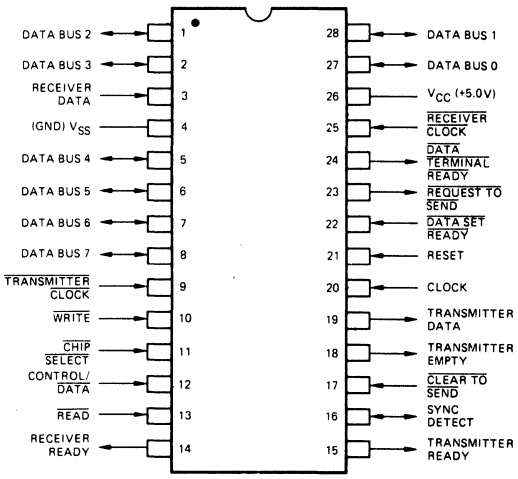
Z20-15


Address/Control and Interrupt
Select and Control
Peripheral/Modem Control
Control
FIFO
Receiver
Receive Data
Data Bus I/O
FIFO
Transmitter
Transmit Data
Sync Code Register
Vss 1
Rx Data 2
Rx CLK 3
Tx CLK 4
SM/DTR 5
Tx Data 6
IRQ 7
TUF 8
RES 9
CS 10
RS 11
Vcc 12
24 CTS
23 DCD
22 D0
21 D1
20 D2
19 D3
18 D4
17 D5
16 D6
15 D7
14 E
13 R/W

Z20-16

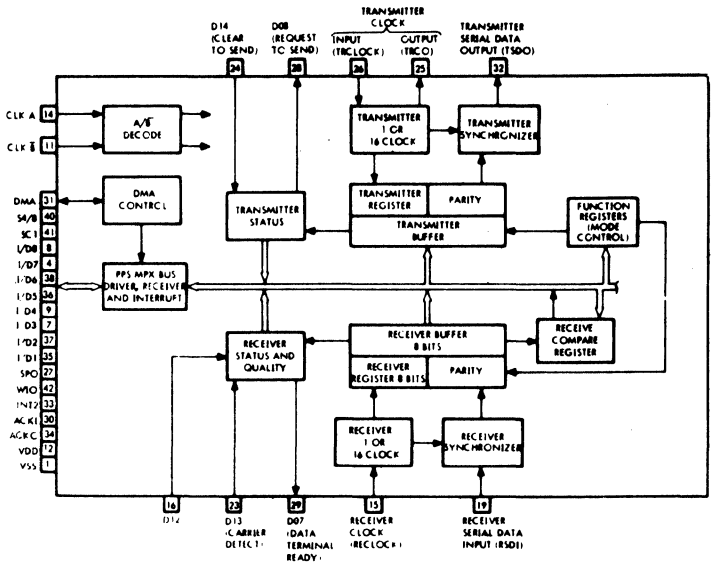


Top View

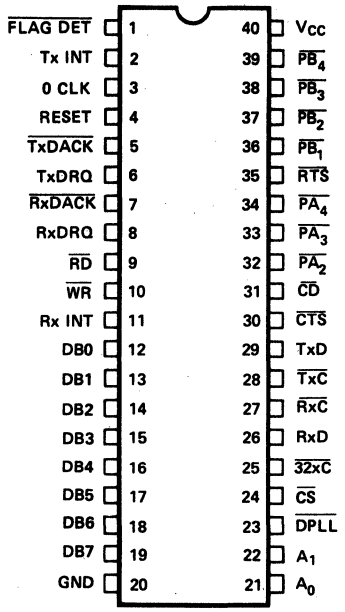


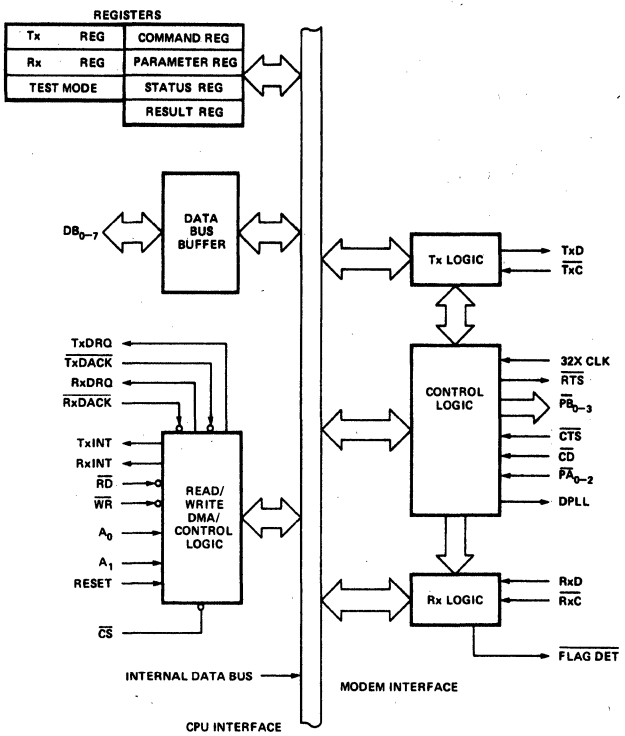
Pin 1 is marked for orientation.

Z20-17

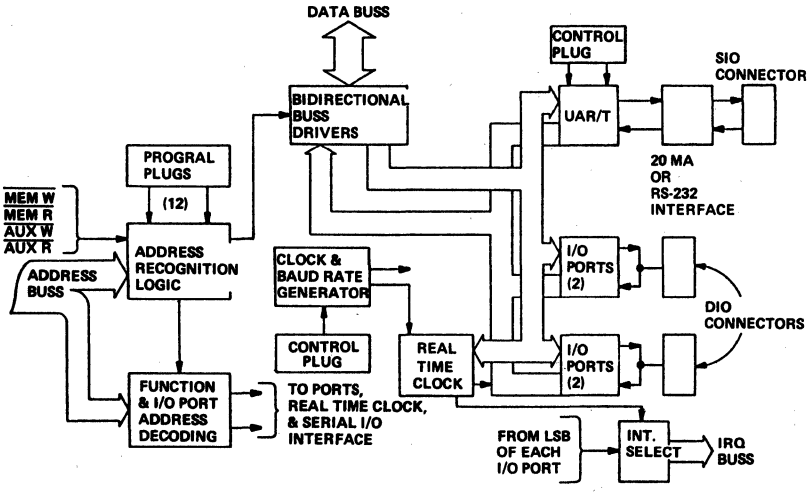


Z20-18





Z20-19



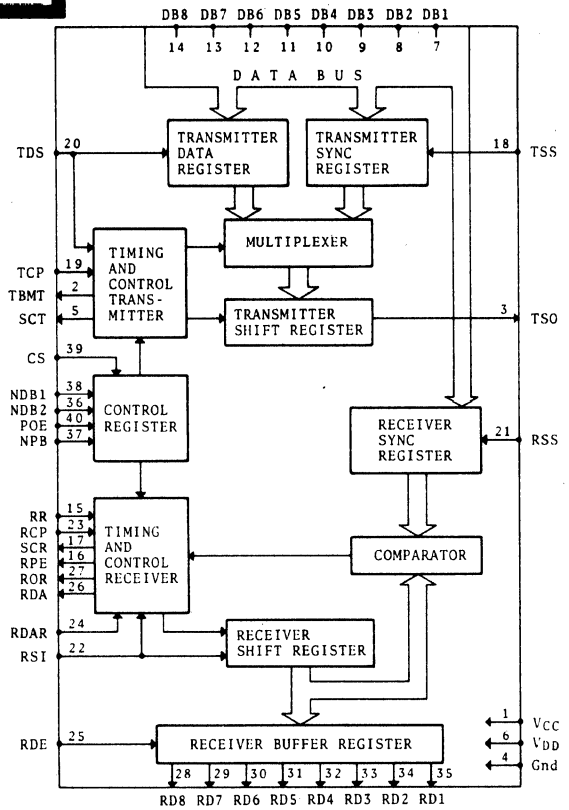
CONNECTOR PIN ASSIGNMENTS

PIN	J1	J2	J3	J4
1	GND	GND	GND	GND
14	GND	GND	GND	GND
2	D7	D7	D7	D7
15	D6	D6	D6	D6
3	D5	D5	D5	D5
16	D4 SECTION A	D4 SECTION A	D4 SECTION A	D4 SECTION A
4	D3 (PORT	D3 (PORT	D3 (PORT	D3 (PORT
17	D2 7)	D2 5)	D2 3)	D2 1)
5	D1	D1	D1	D1
18	D0	D0	D0	D0
6				
19	CS16	CS14	CS12	
7	CS17	CS15	CS13	
20				
8				
21	(MRST +PRST)	MRST +PRST)	(MRST+PRST)	(MRST+PRST)
9	GND	GND	GND	GND
22	GND	GND	GND	GND
10	D7	D7	D7	D7
23	D6	D6	D6	D6
11	D5	D5	D5	D5
24	D4 SECTION B	D4 SECTION B	D4 SECTION B	D4 SECTION B
12	D3 (PORT	D3 (PORT	D3 (PORT	D3 (PORT
25	D2 6)	D2 4)	D2 2)	D2 0)
13	D1	D1	D1	D1
26	D0	D0	D0	D0

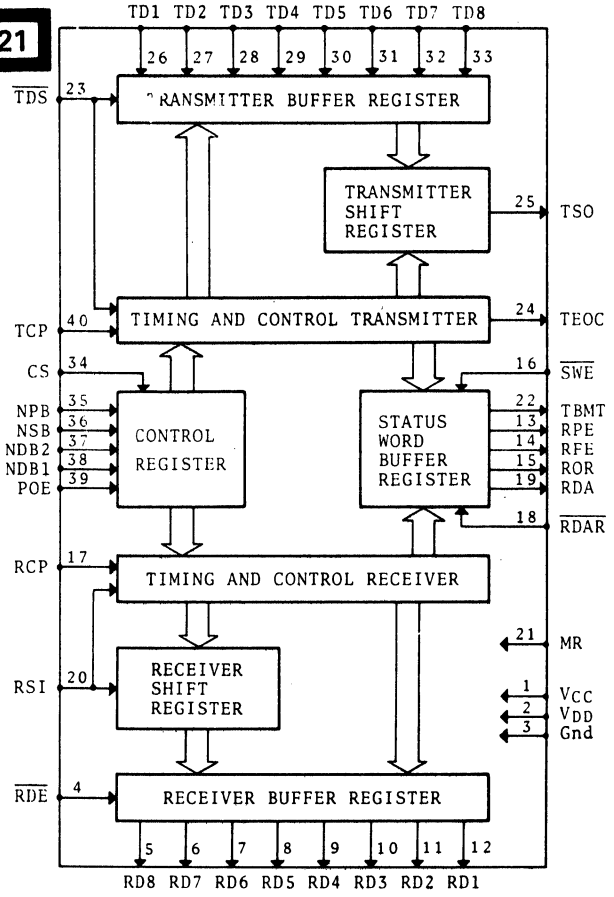
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

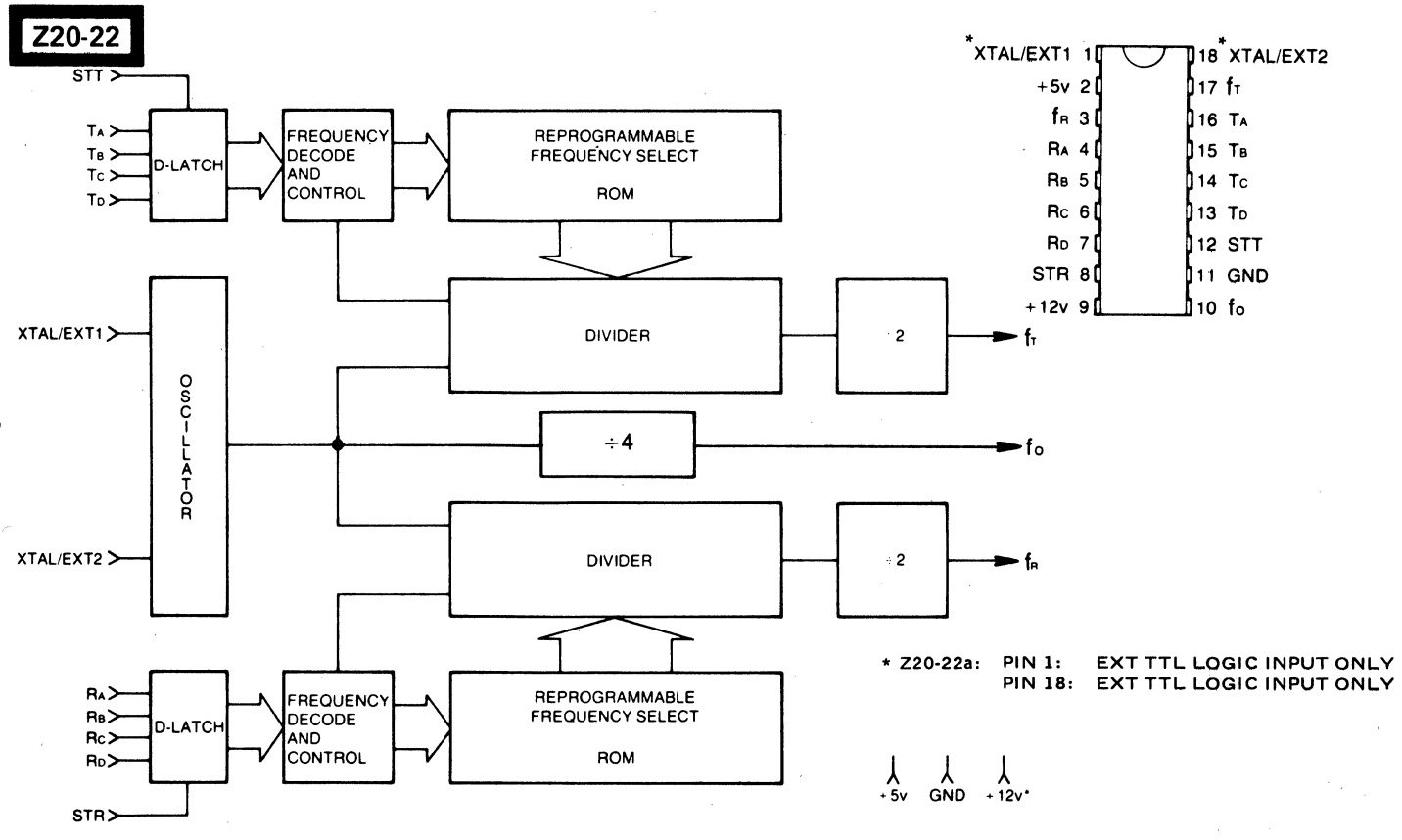
Z20-20



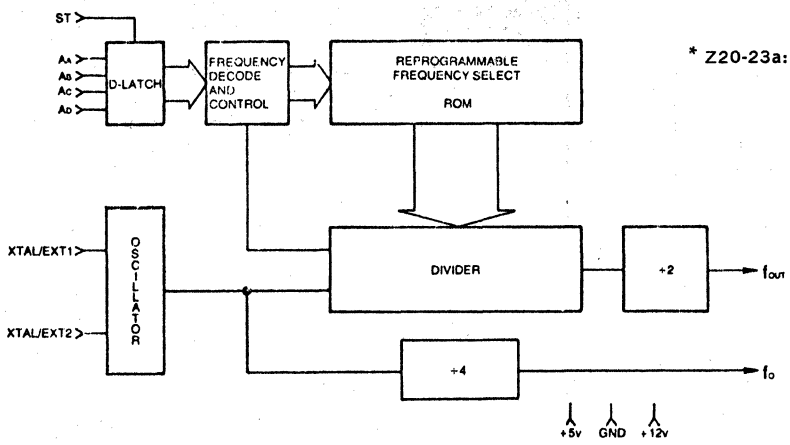
Z20-21



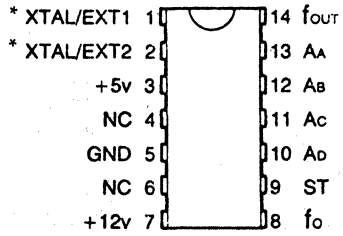
Z20-22



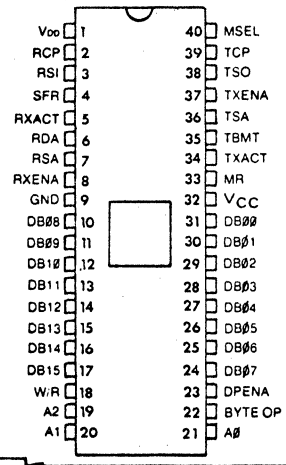
Z20-23

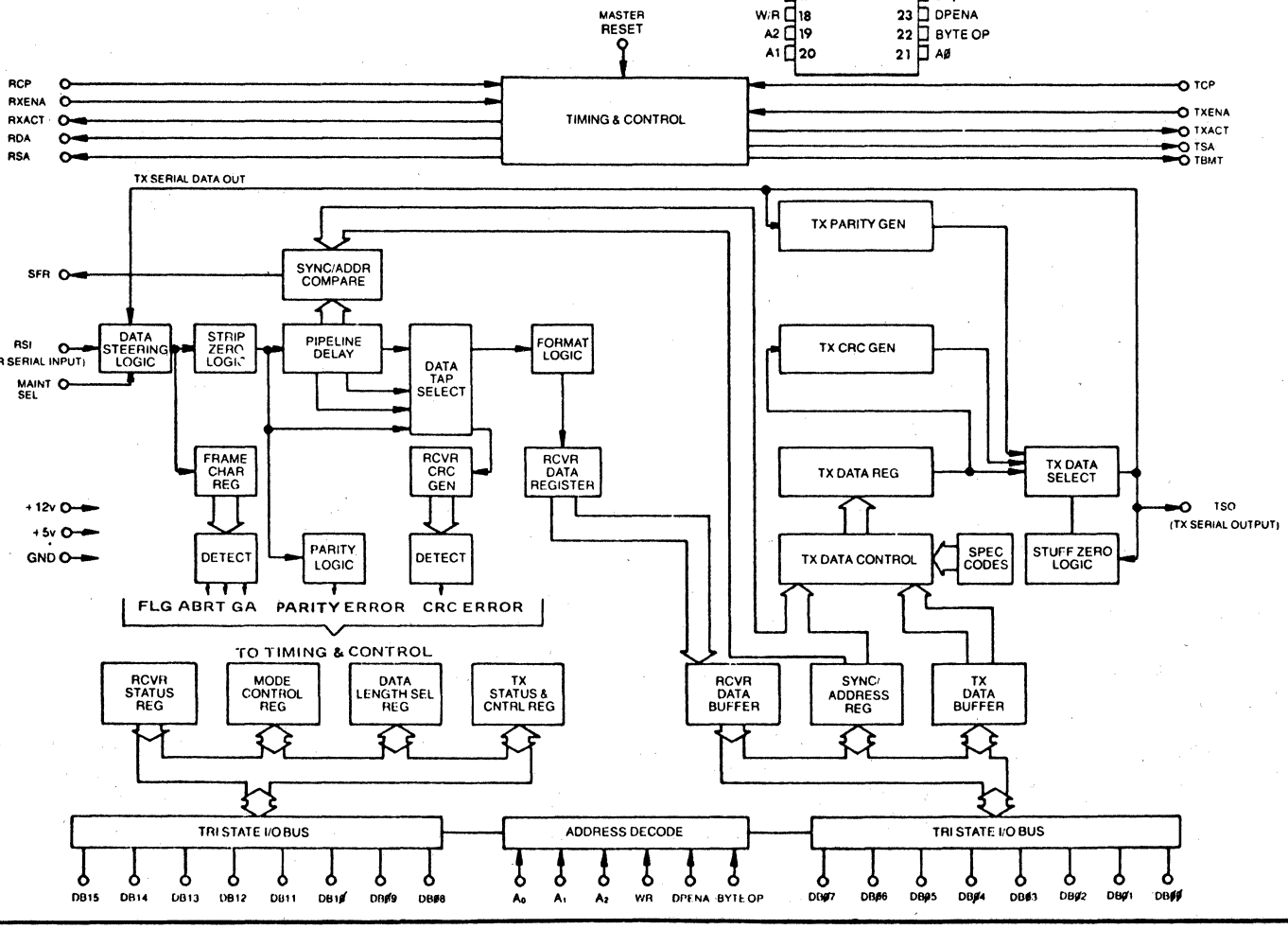


* Z20-23a: PIN 1: EXT TTL LOGIC INPUT ONLY
PIN 2: EXT TTL LOGIC INPUT ONLY

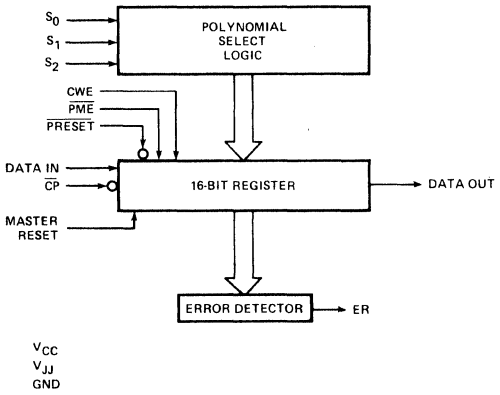


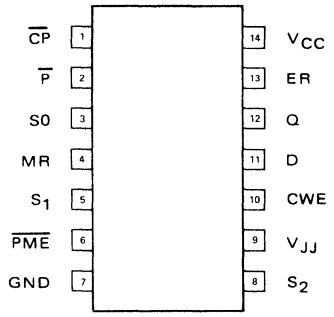
Z20-24



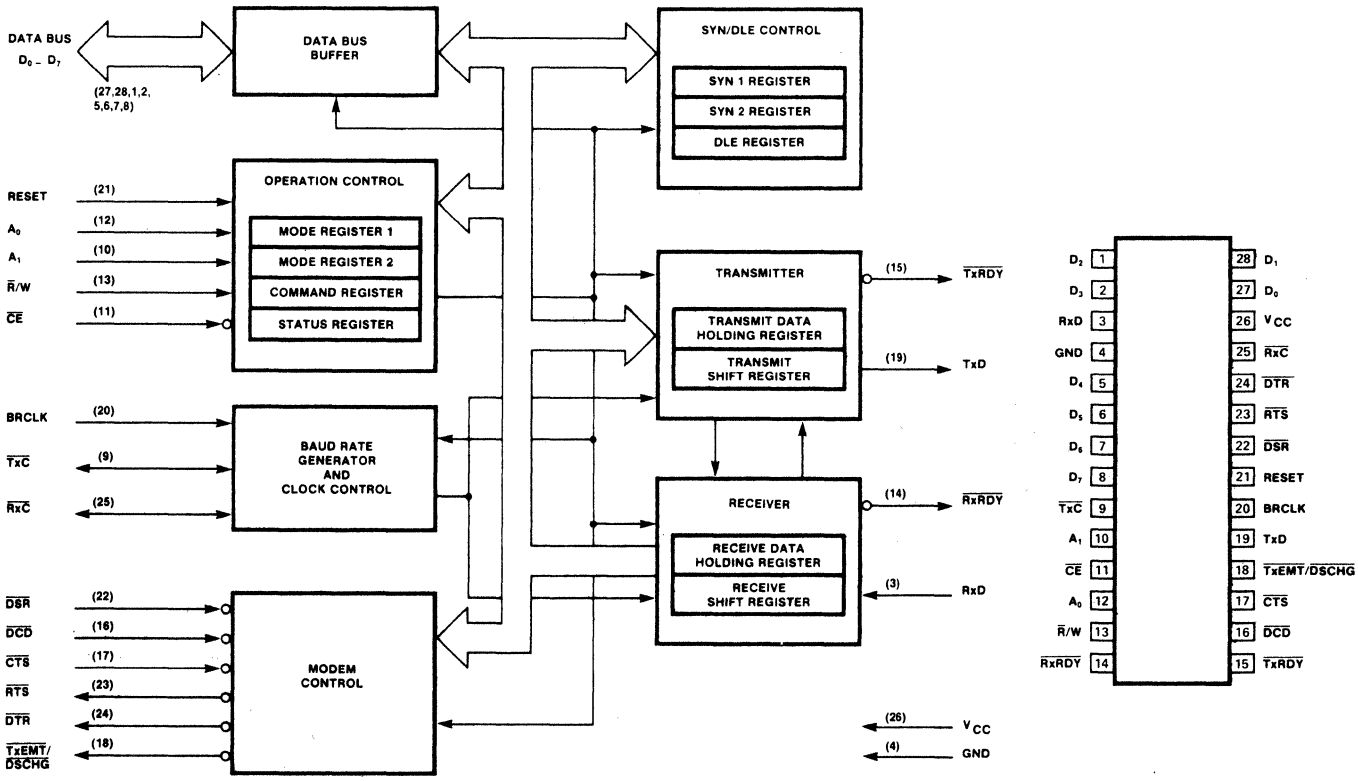


Z20-25

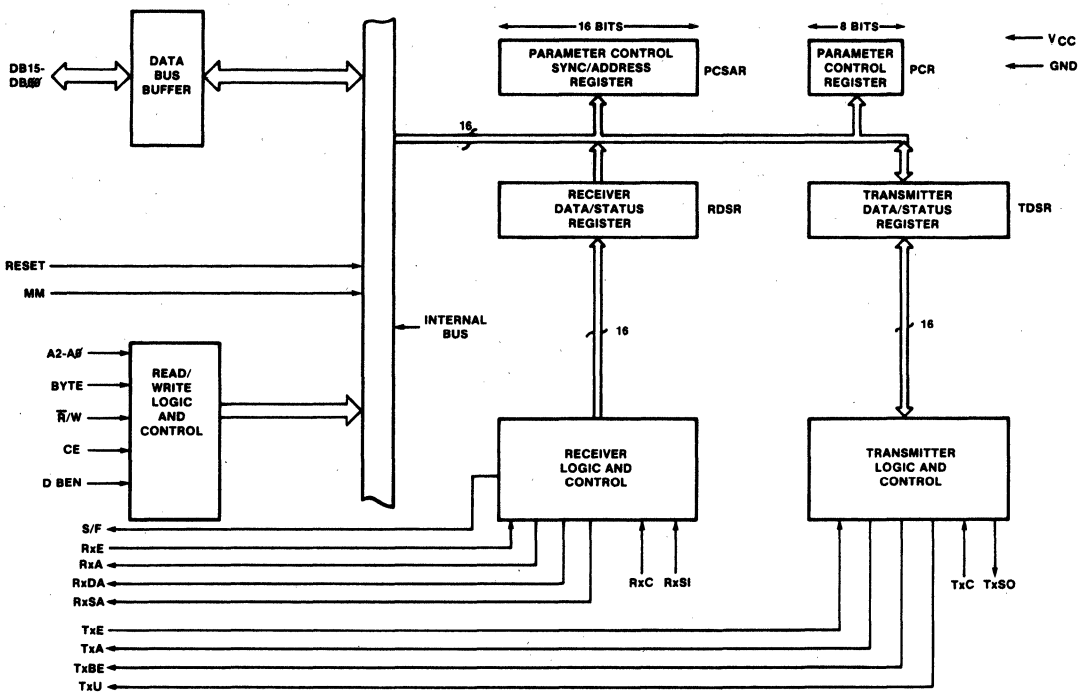

S0
S1
S2
POLYNOMIAL SELECT LOGIC
CWE
PME
PRESET
DATA IN
CP
16-BIT REGISTER
DATA OUT
MASTER RESET
ERROR DETECTOR
ER
VCC
VJJ
GND

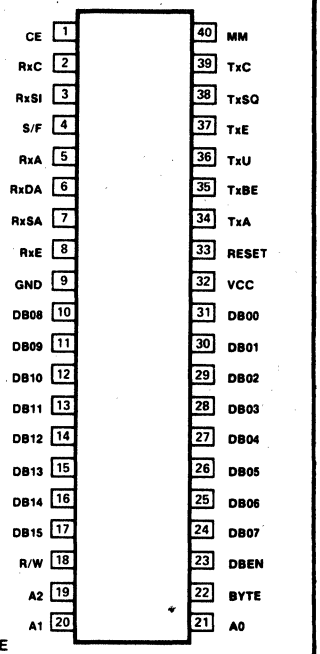

CP 1
P 2
S0 3
MR 4
S1 5
PME 6
GND 7
14 VCC
13 ER
12 Q
11 D
10 CWE
9 VJJ
8 S2

Z20-26


DATA BUS D0 - D7
(27,28,1,2,5,6,7,8)
DATA BUS BUFFER
SYN/DLE CONTROL
SYN 1 REGISTER
SYN 2 REGISTER
DLE REGISTER
OPERATION CONTROL
MODE REGISTER 1
MODE REGISTER 2
COMMAND REGISTER
STATUS REGISTER
RESET (21)
A0 (12)
A1 (10)
R/W (13)
CE (11)
TRANSMITTER
TRANSMIT DATA HOLDING REGISTER
TRANSMIT SHIFT REGISTER
(15) TxRDY
(19) TxD
BRCLK (20)
TxC (9)
RxC (25)
BAUD RATE GENERATOR AND CLOCK CONTROL
RECEIVER
RECEIVE DATA HOLDING REGISTER
RECEIVE SHIFT REGISTER
(14) RxRDY
(3) RxD
DSR (22)
DCD (16)
CTS (17)
RTS (23)
DTR (24)
TxEMT/DSCHG (18)
MODEM CONTROL
(26) VCC
(4) GND
D2 1
D3 2
RxD 3
GND 4
D4 5
D5 6
D6 7
D7 8
TxC 9
A1 10
CE 11
A0 12
R/W 13
RxRDY 14
28 D1
27 D0
26 VCC
25 RxC
24 DTR
23 RTS
22 DSR
21 RESET
20 BRCLK
19 TxD
18 TxEMT/DSCHG
17 CTS
16 DCD
15 TxRDY

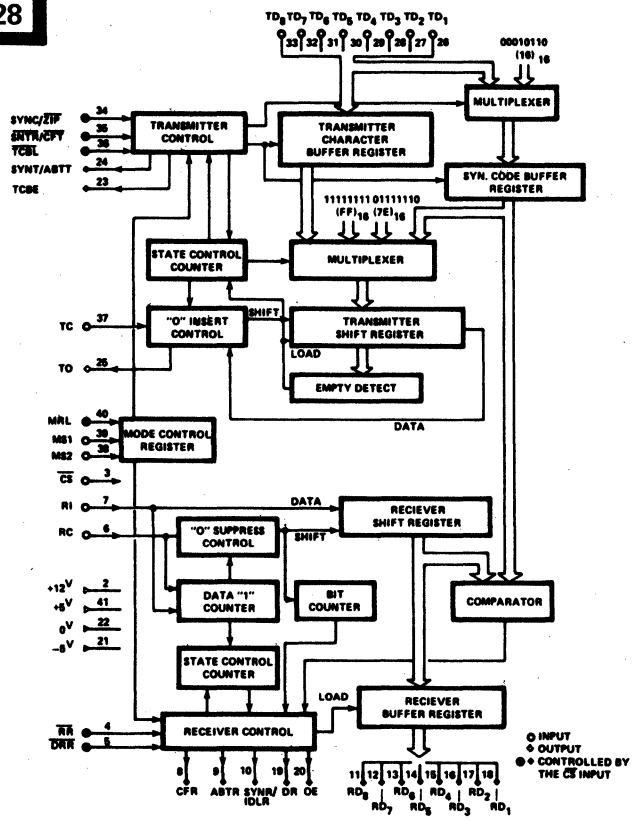
Z20-27

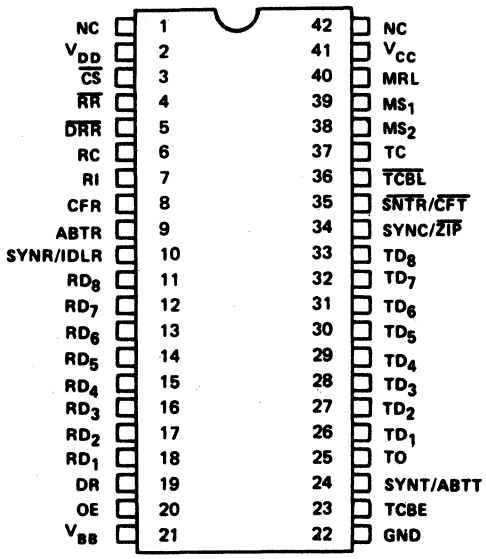




NOTE
00 is least significant bit, highest number (that is, DB15, A2) is most significant bit.

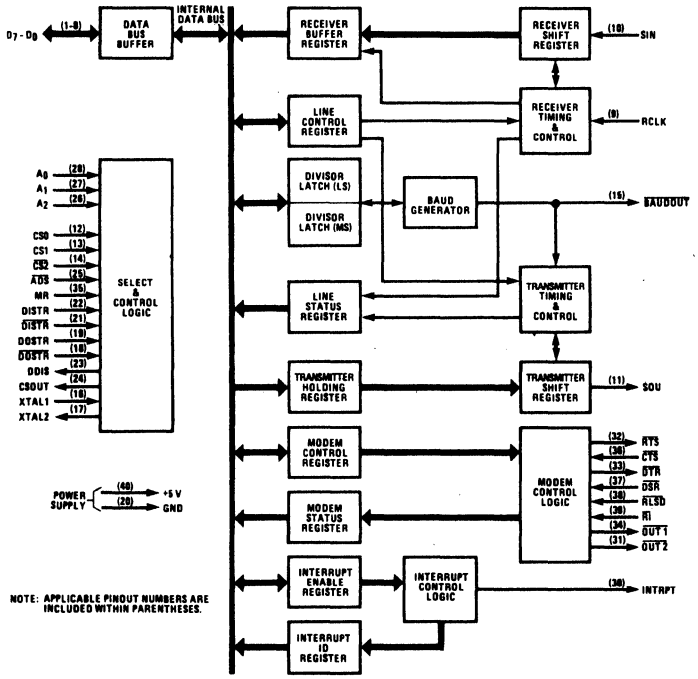
Z20-28



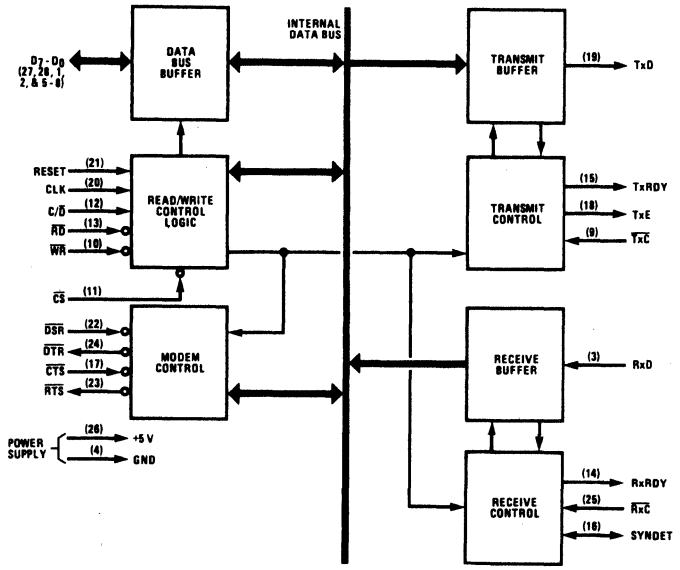


NC: NO CONNECTION

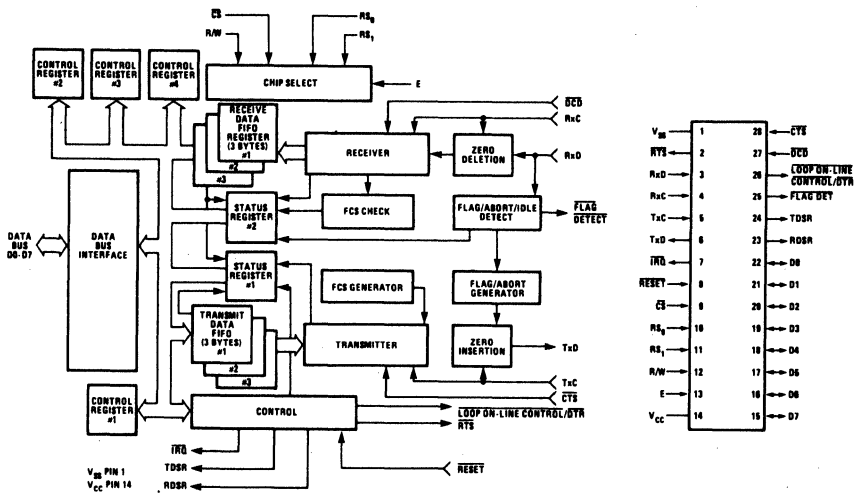
Z20-29



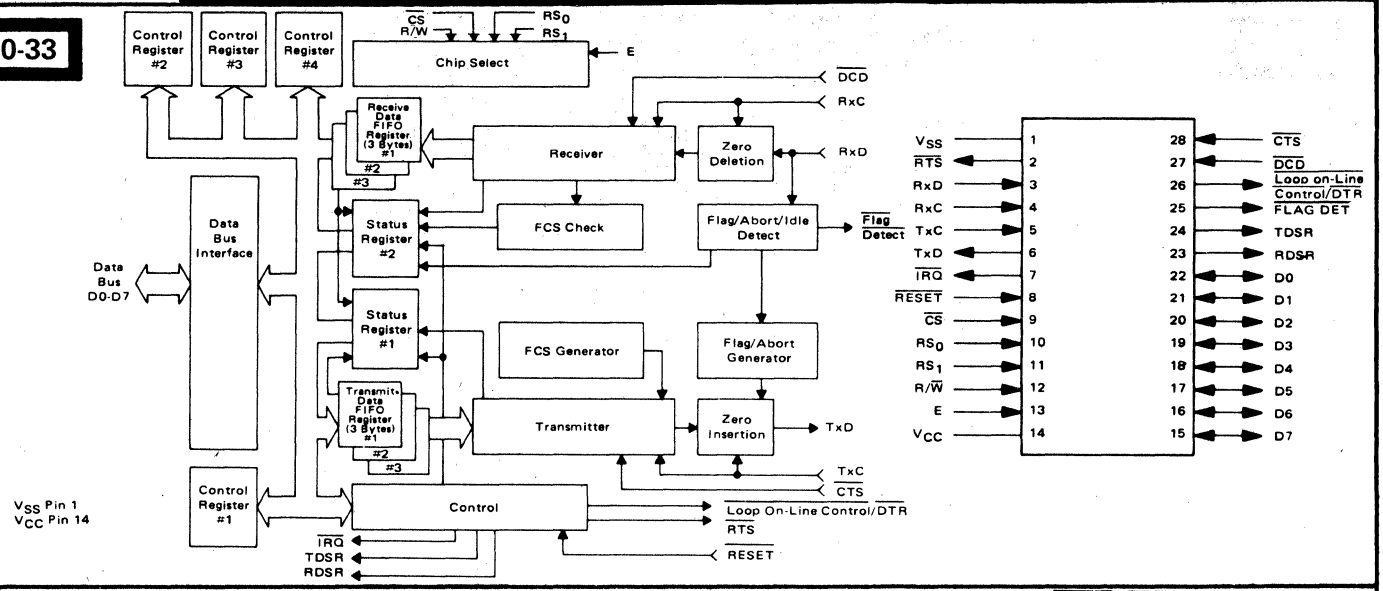
Z20-30



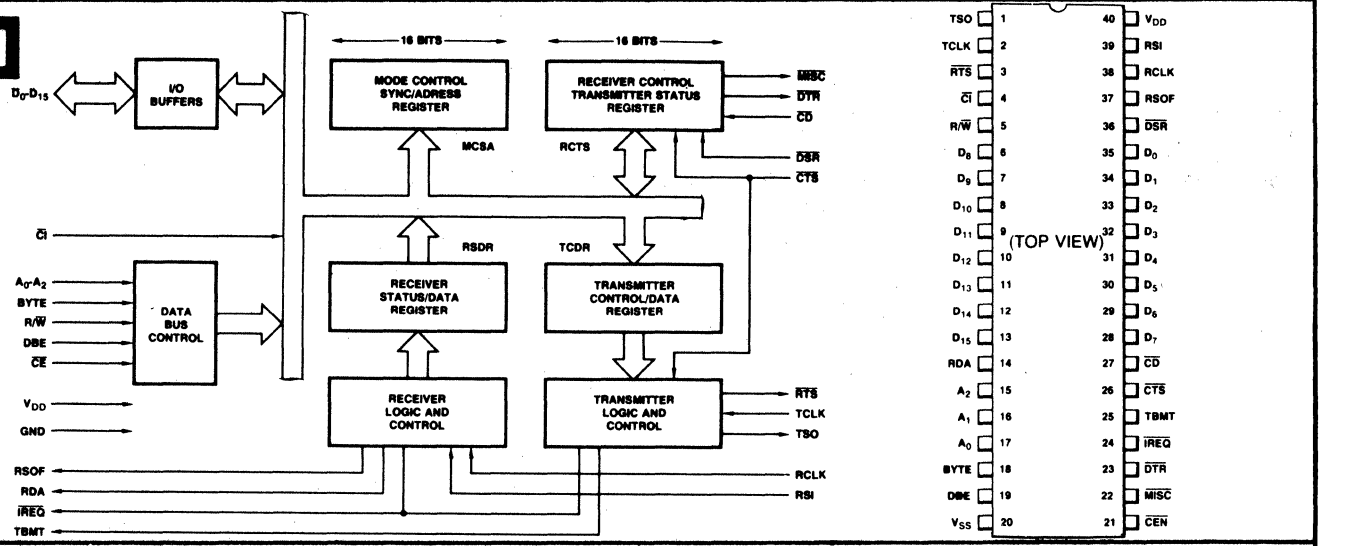
Z20-32



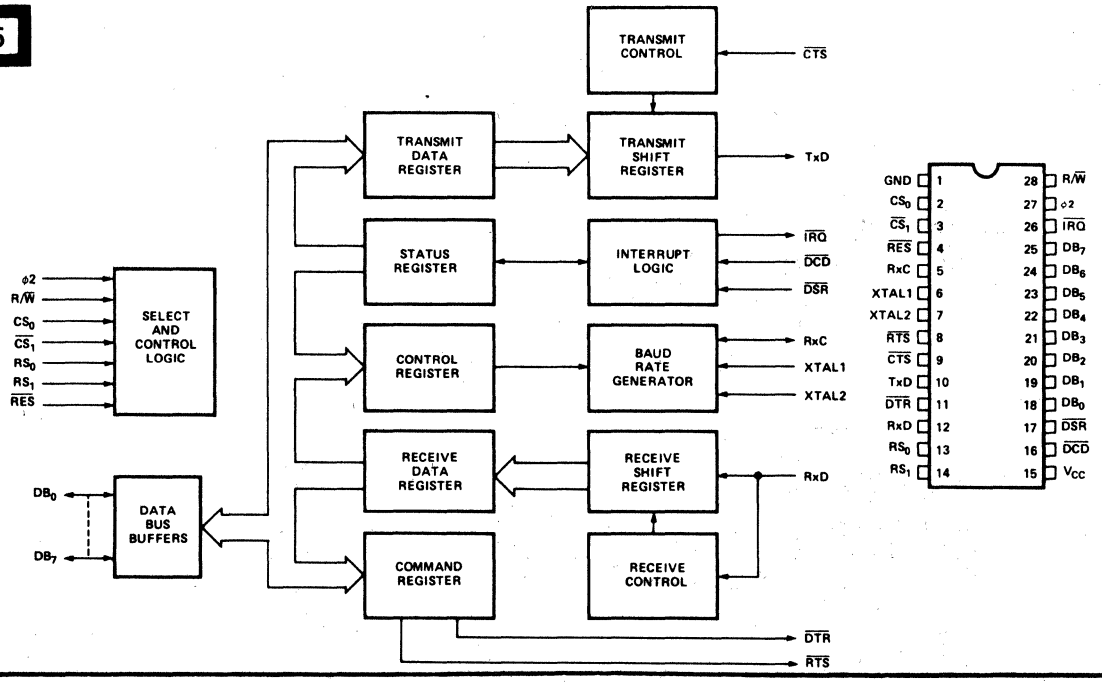
Z20-33



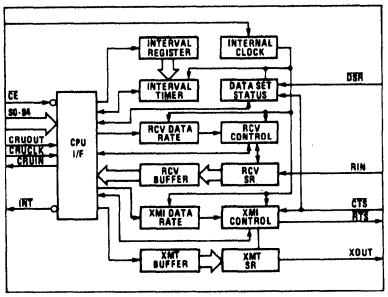
Z20-34

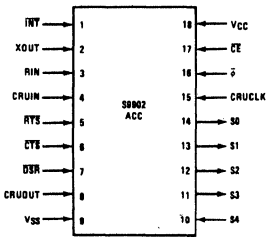


Z20-35

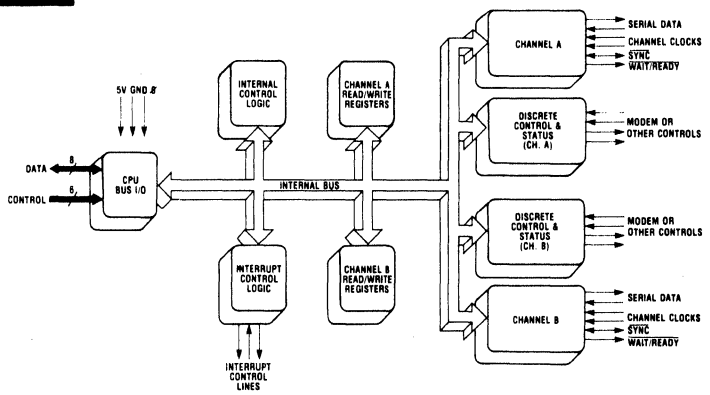


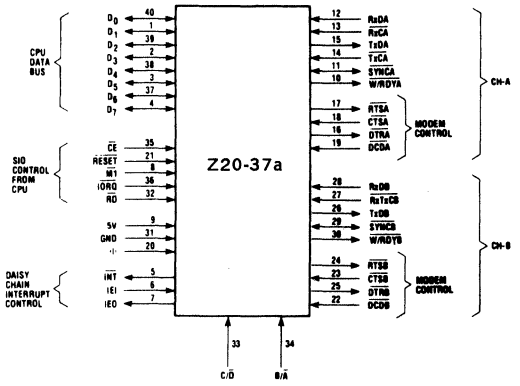
Z20-36

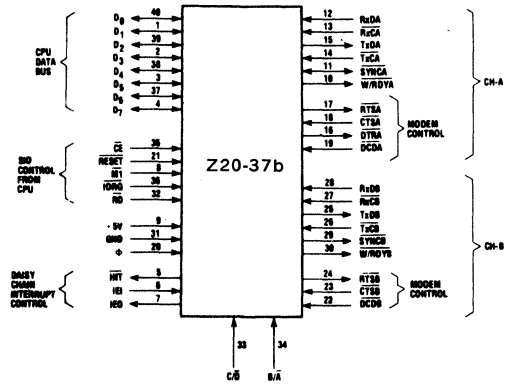


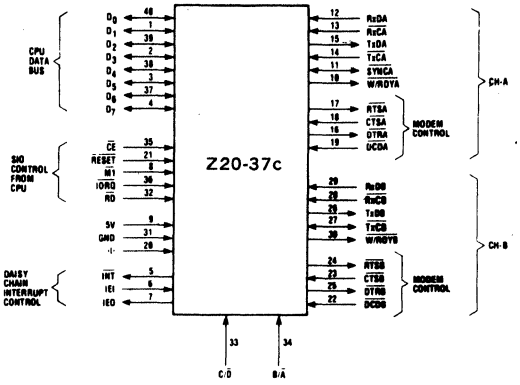


Z20-37

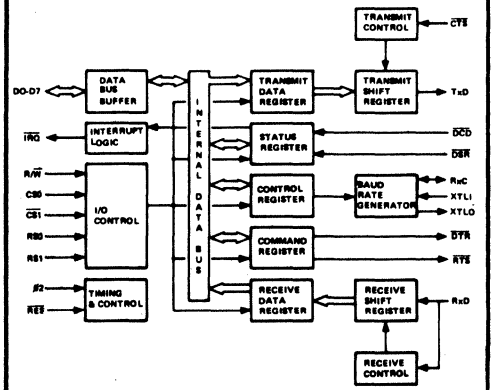


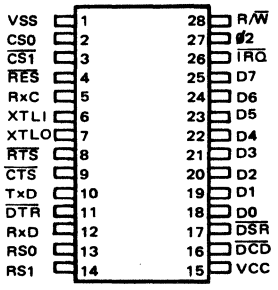




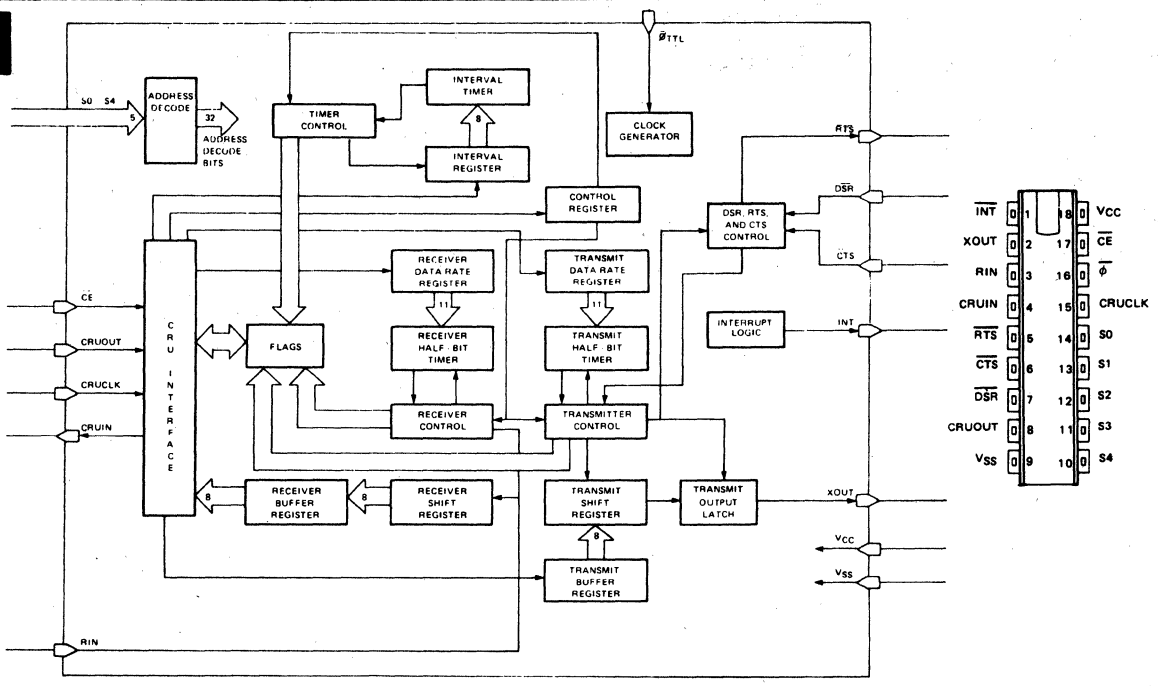


Z20-38

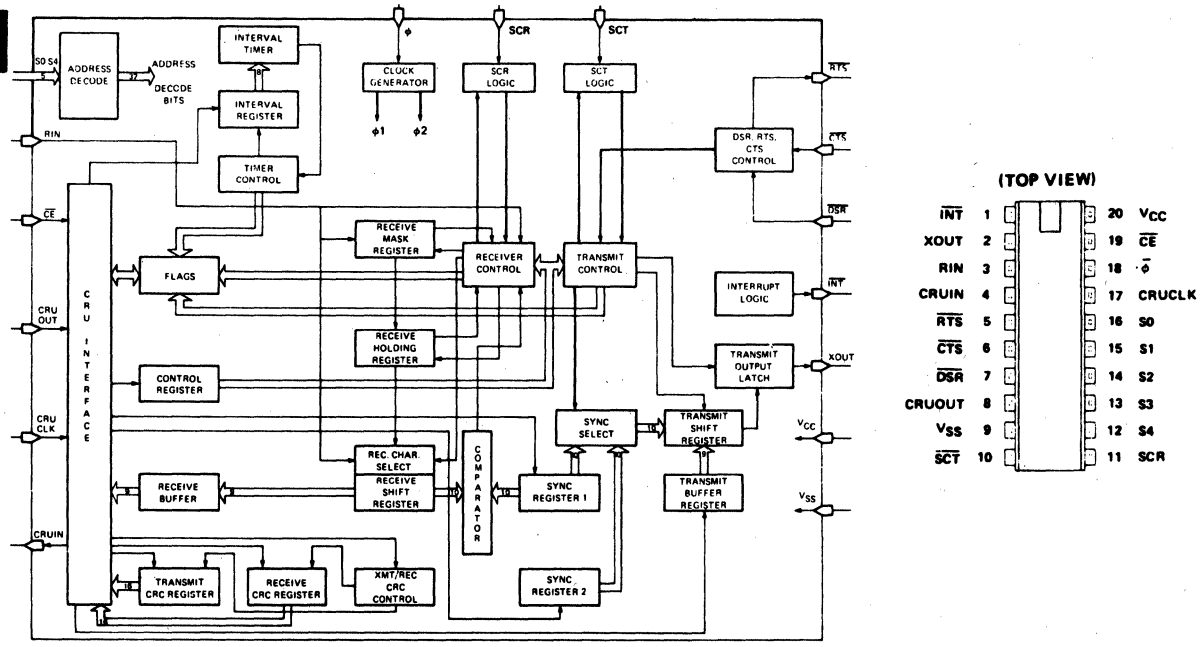




Z20-39

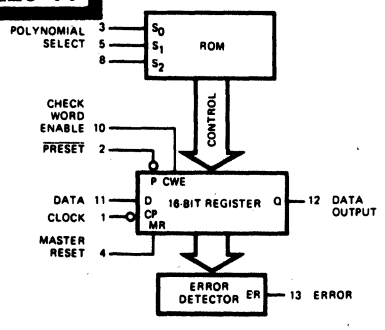


Z20-40



(TOP VIEW)

Z20-41

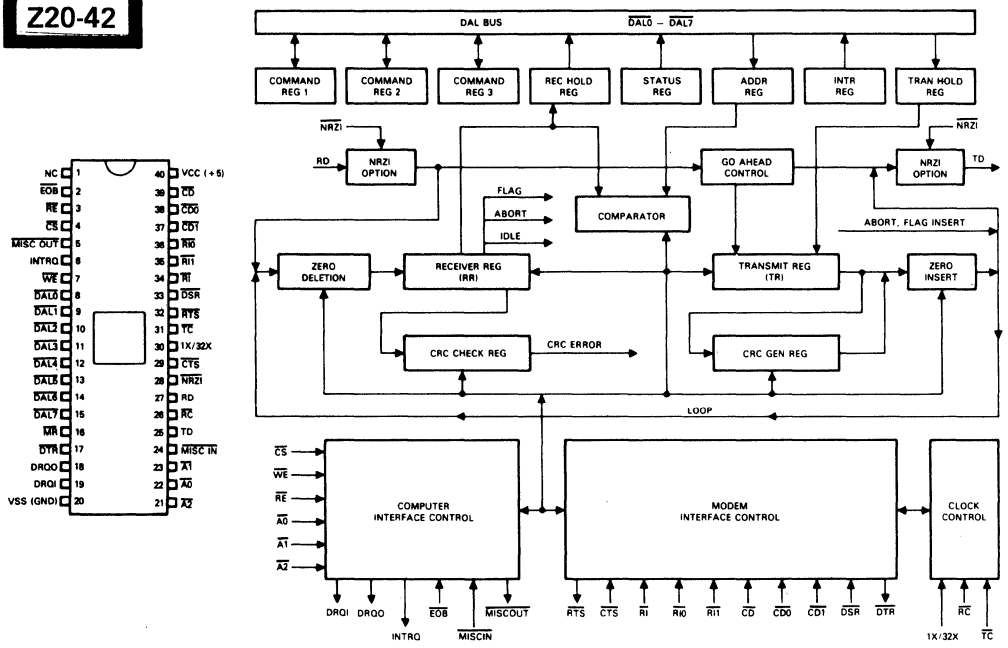


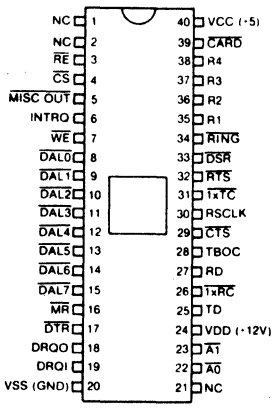
VCC = Pin 14
GND = Pin 7

19. LOGIC/BLOCK DRAWINGS

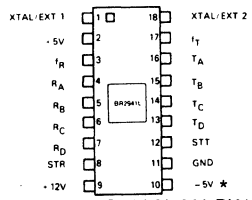
IN DRAWING NUMBER SEQUENCE

Z20-42

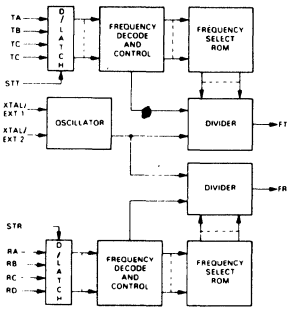




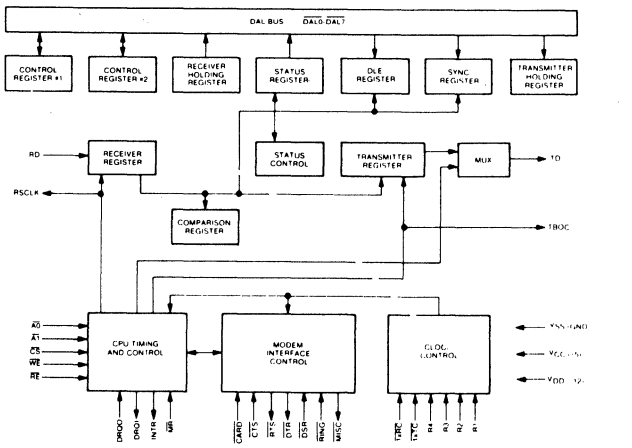
Z20-44



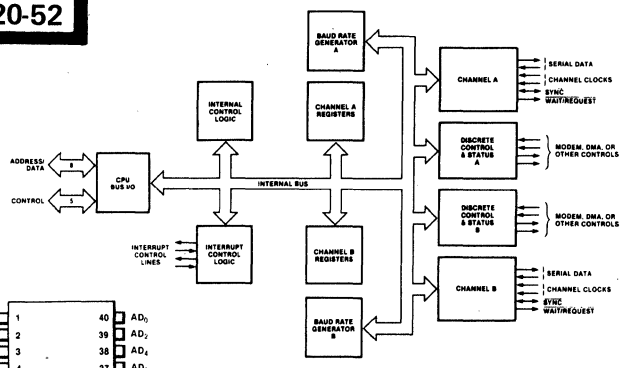
* NO CONNECTION ON PIN 10 FOR Z20-44a

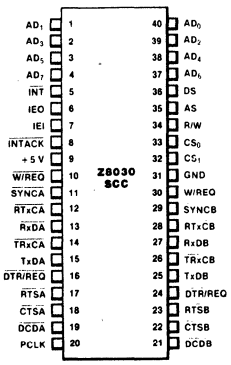


Z20-43



Z20-52





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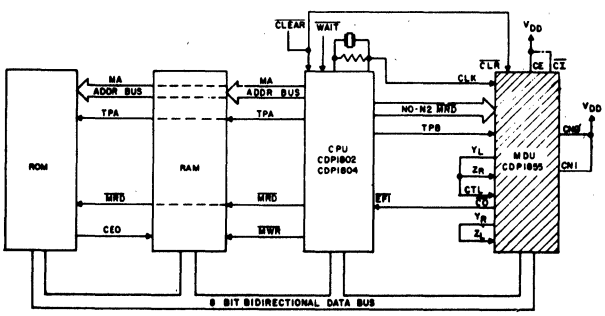

19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

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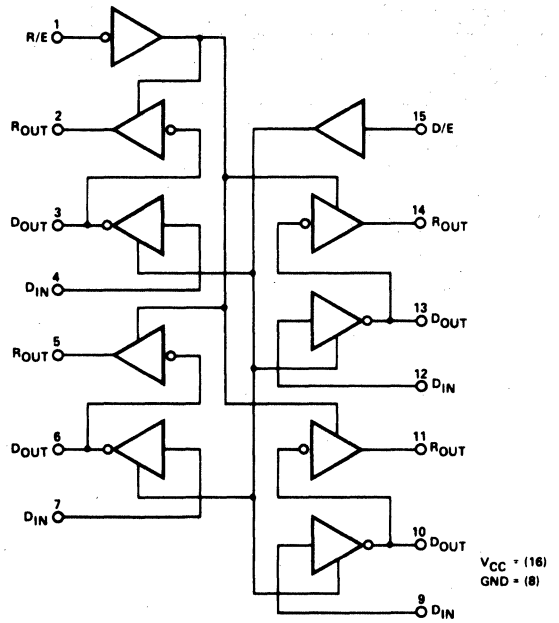

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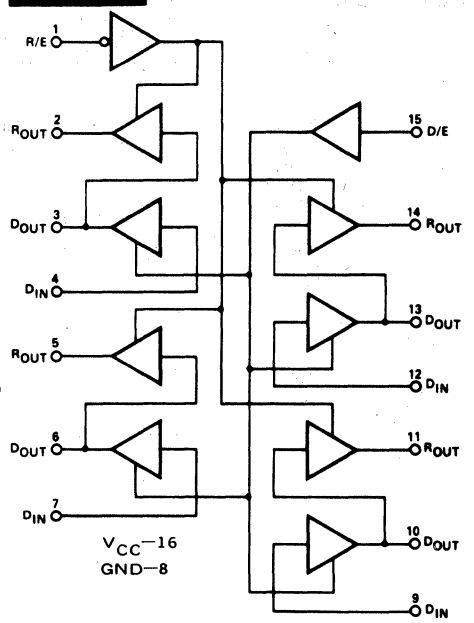

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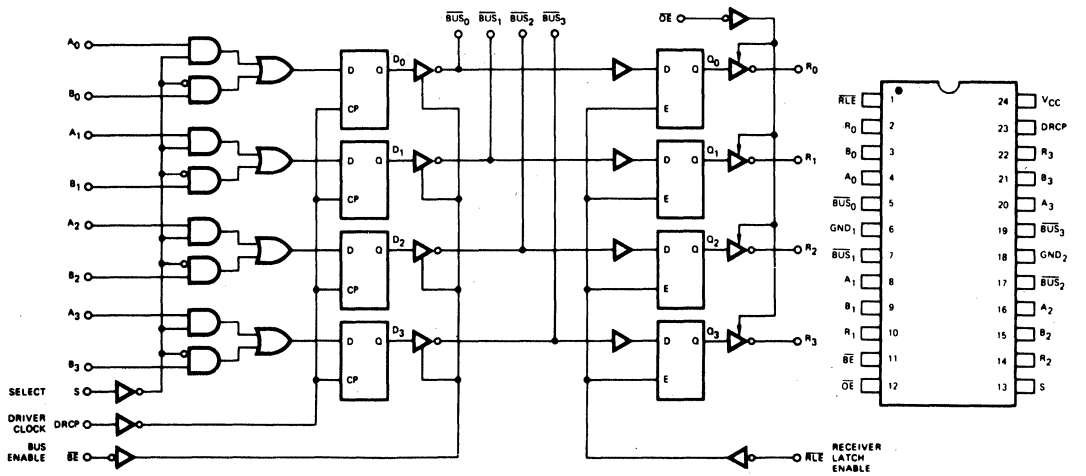

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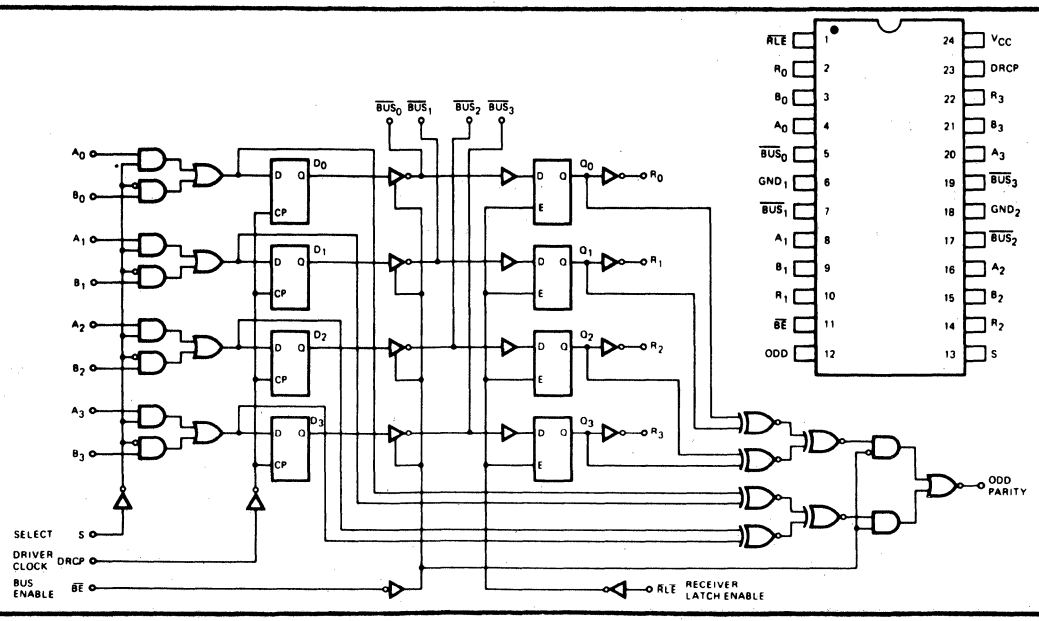

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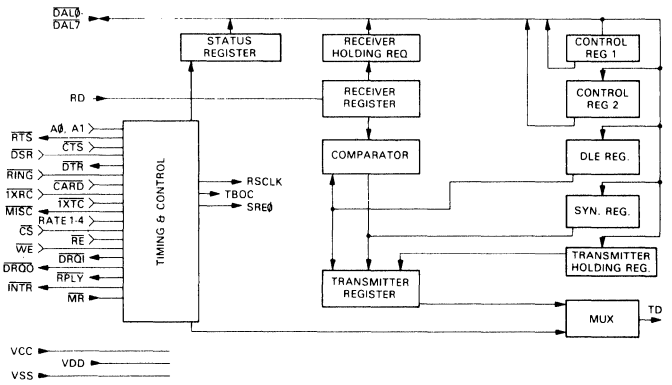

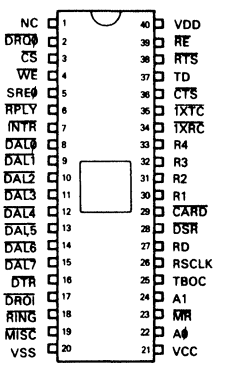

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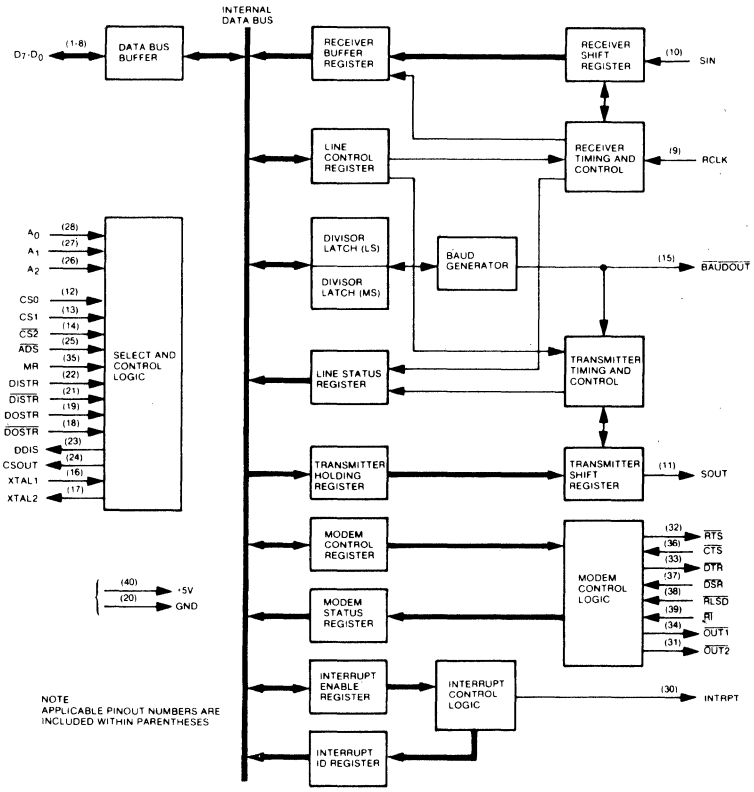

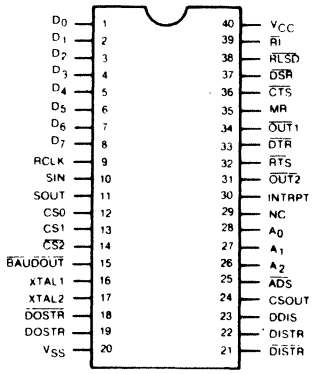

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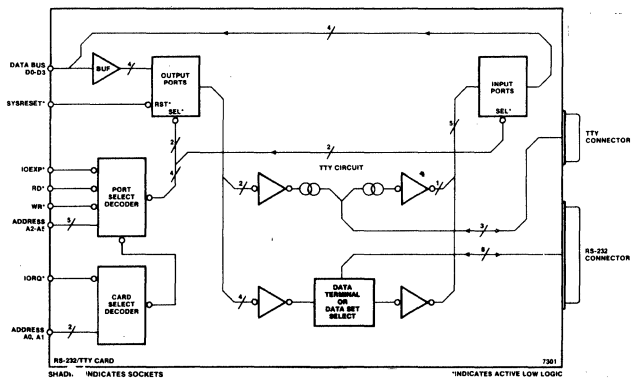

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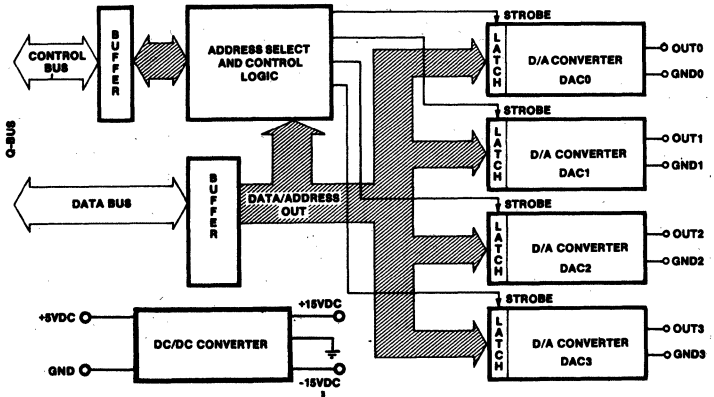

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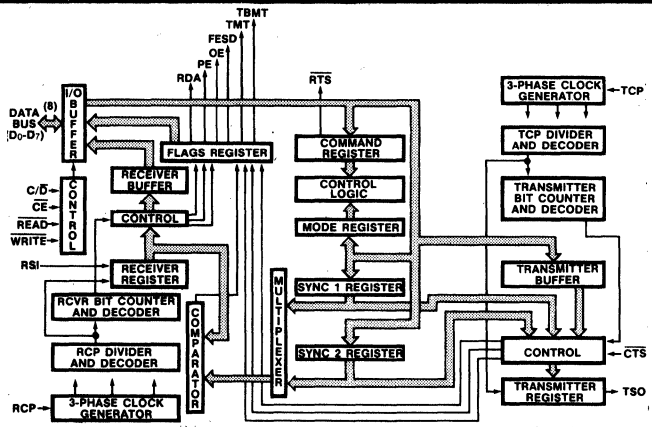

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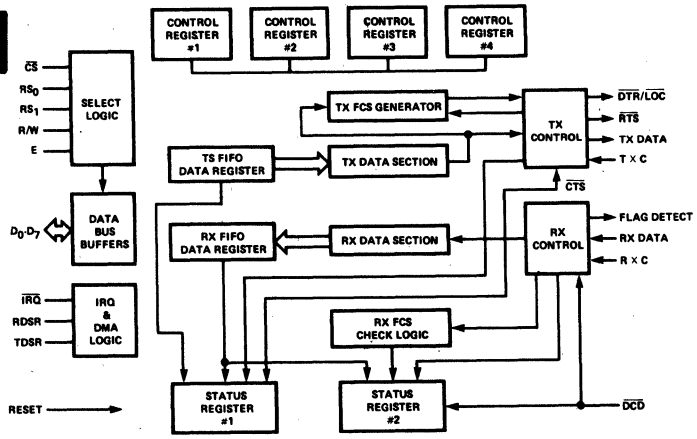

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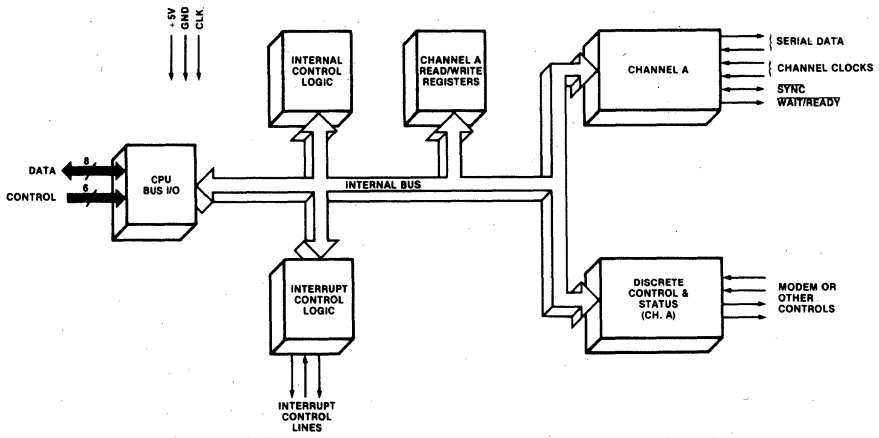

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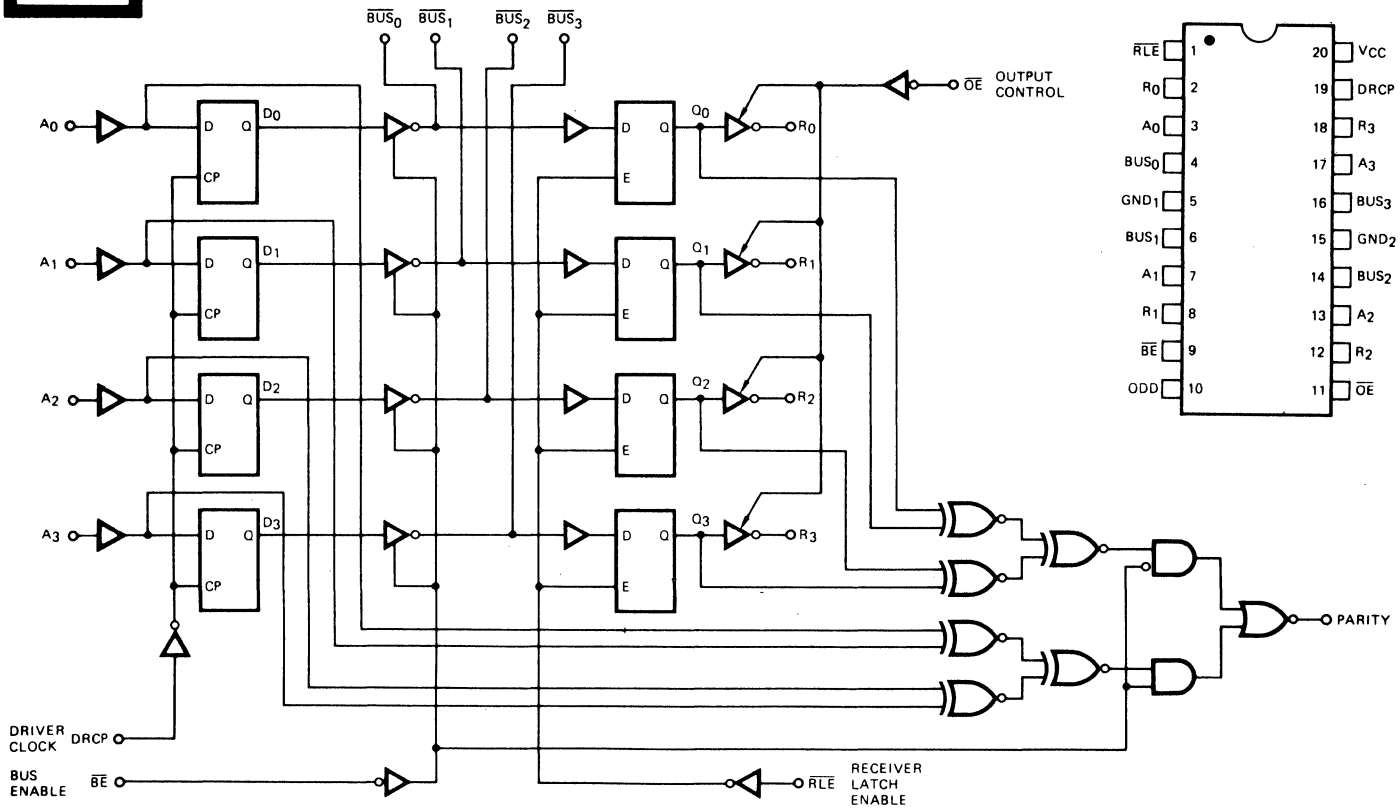

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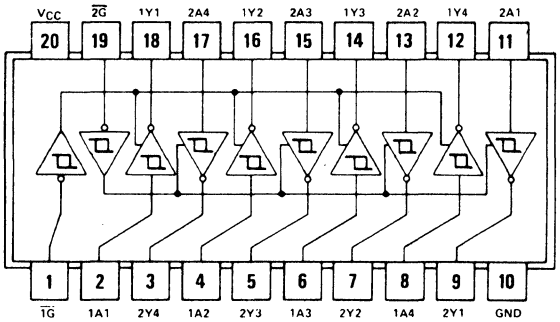

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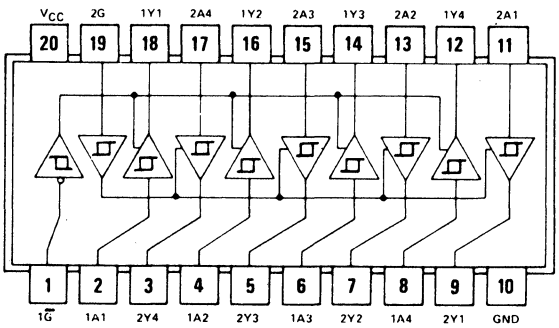

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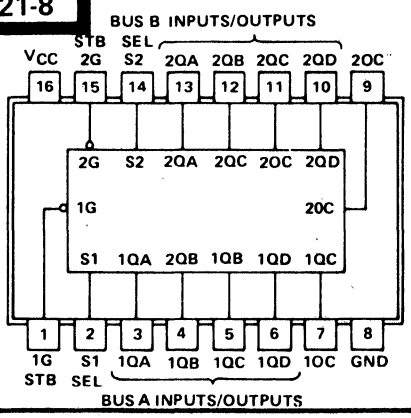

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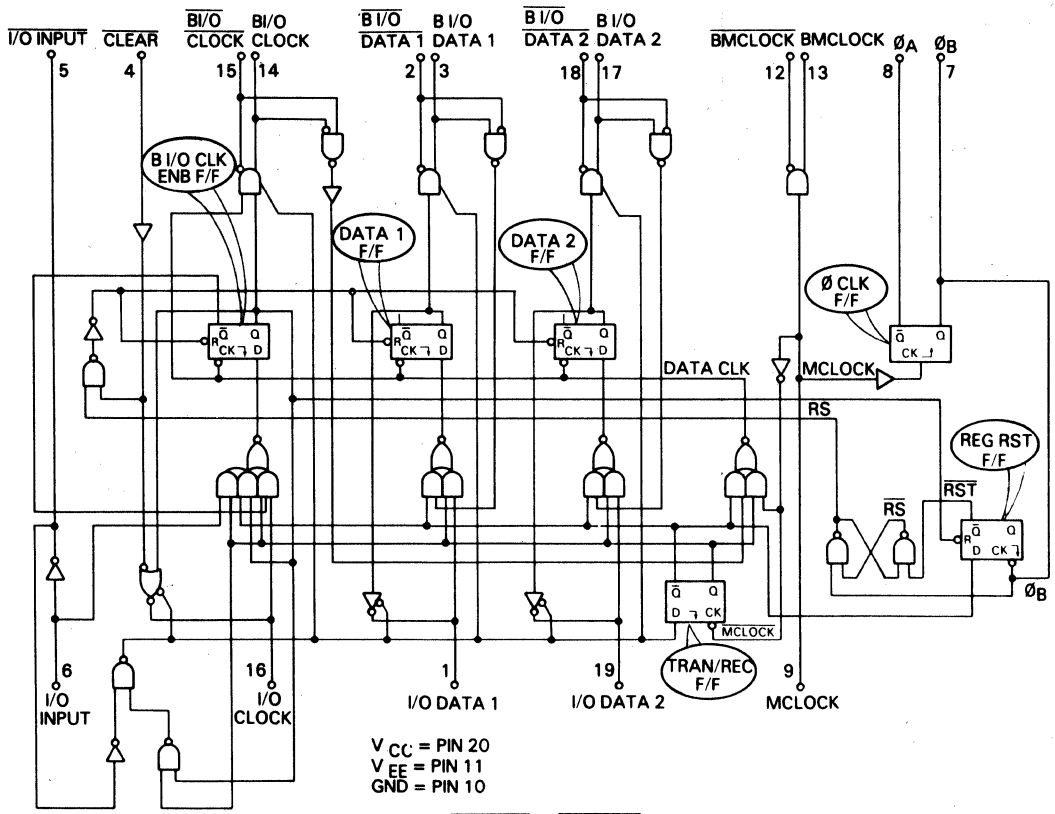

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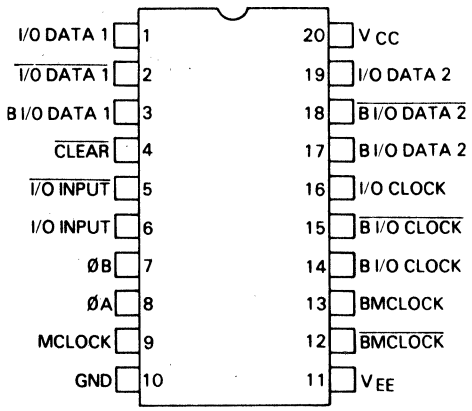
V_{EE} = PIN 11
GND = PIN 10



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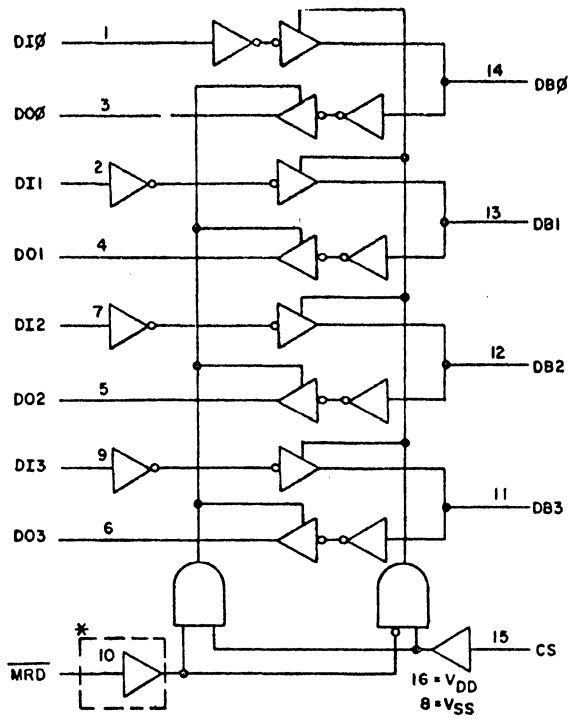

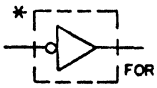

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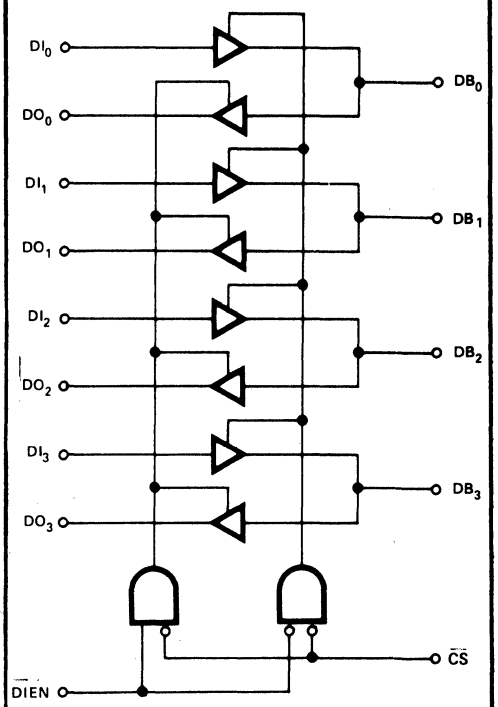

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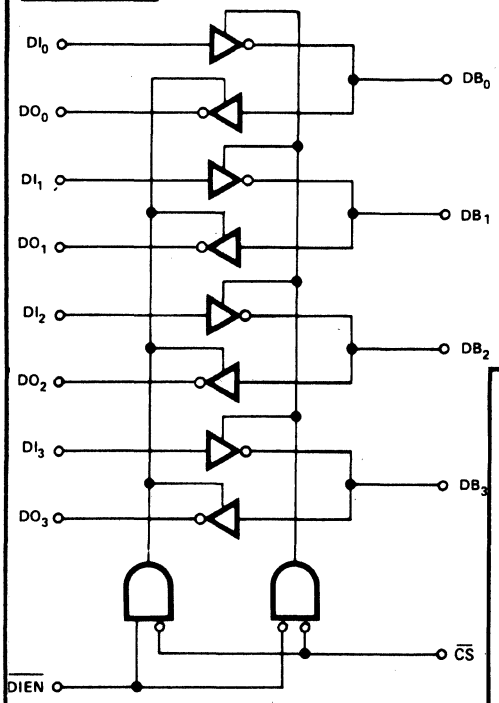

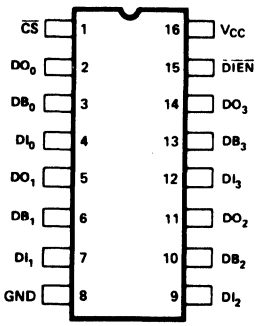

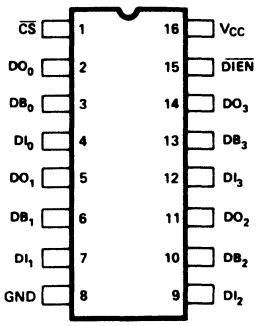

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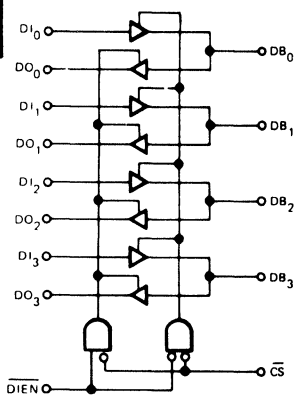

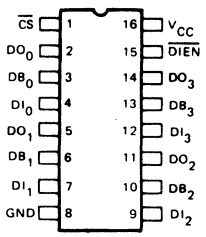

19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

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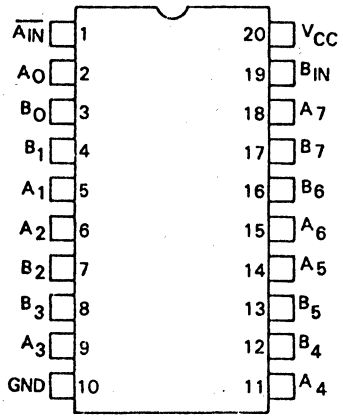
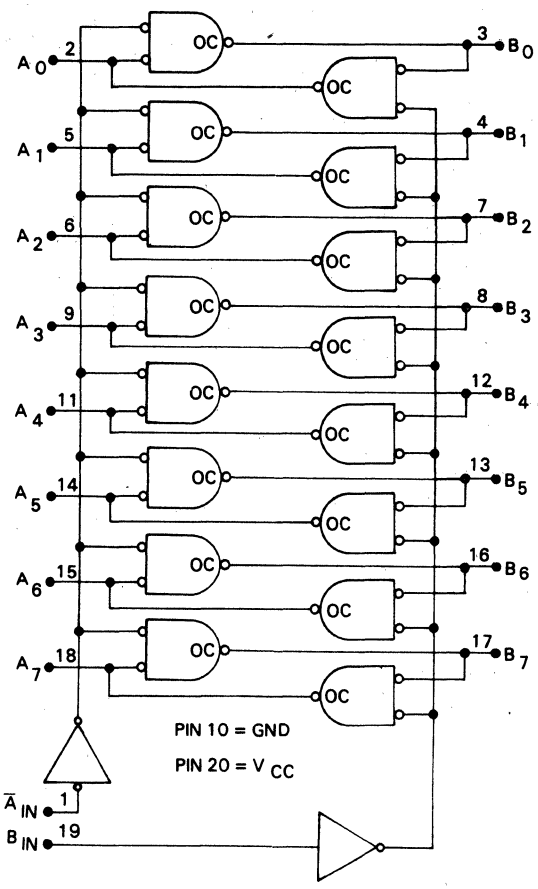
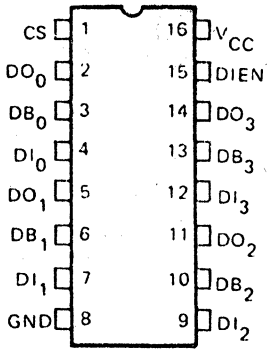
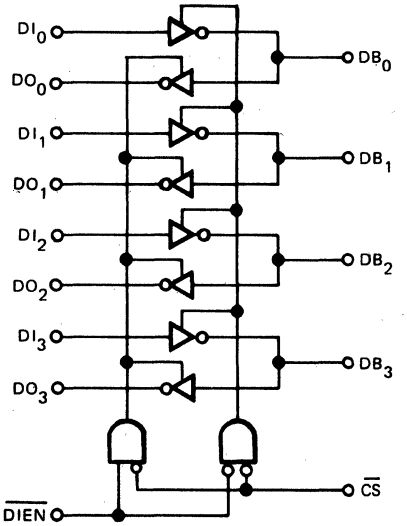


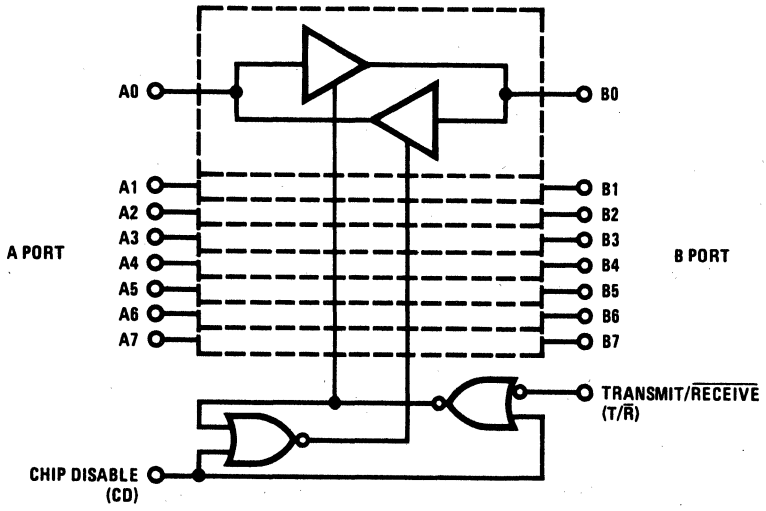


Z21-17

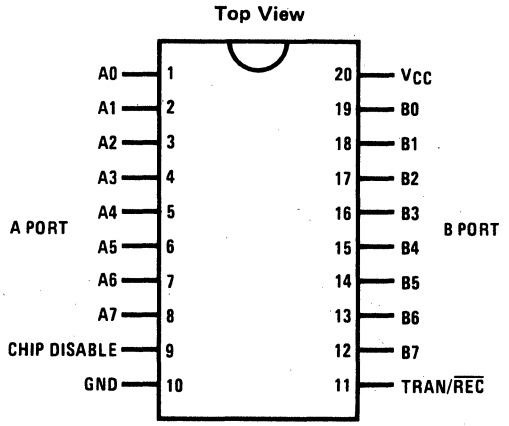




Z21-18



Top View



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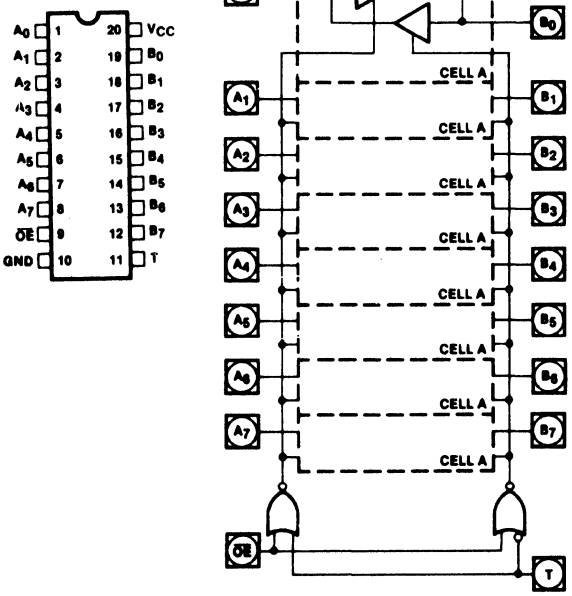

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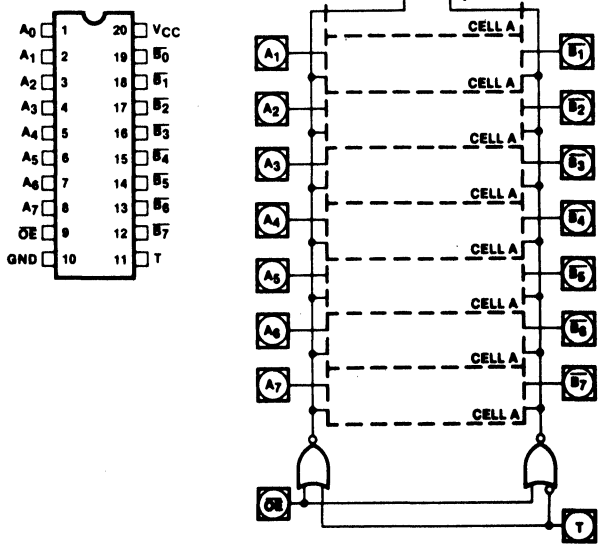

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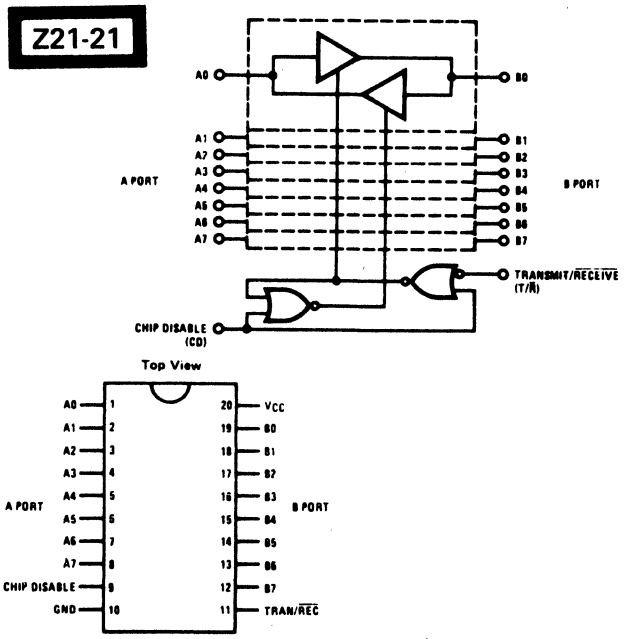

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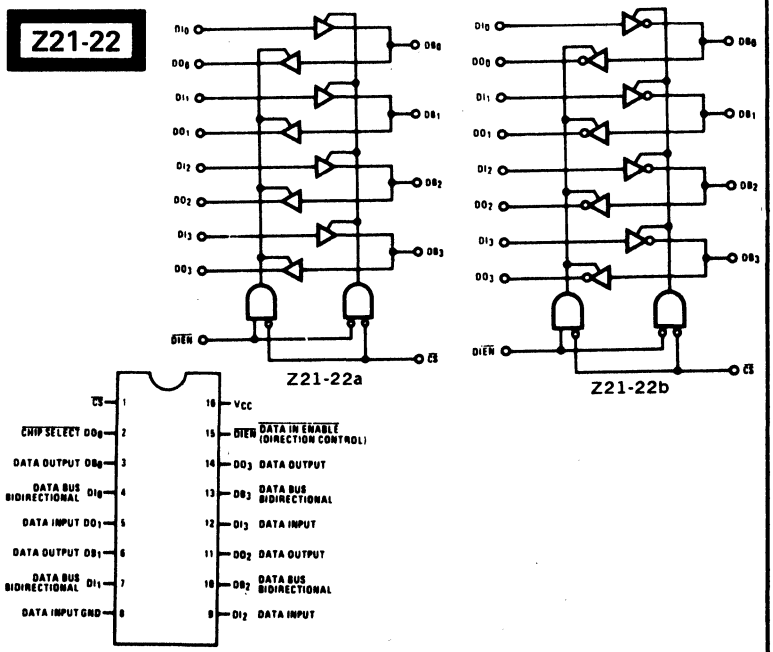

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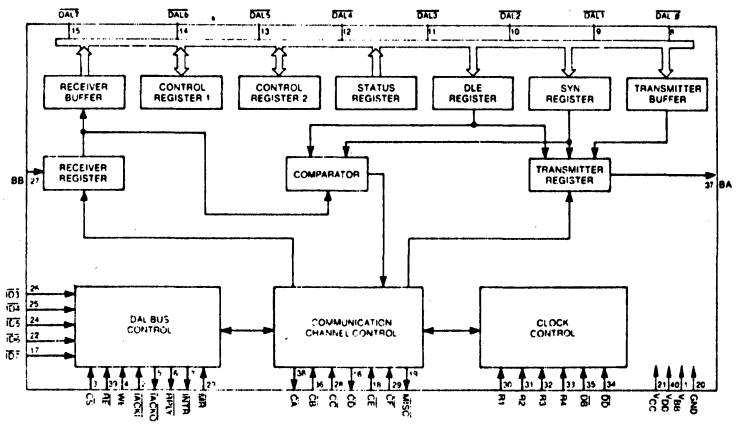

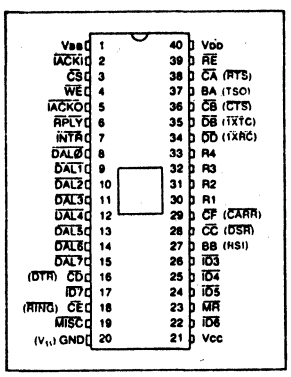

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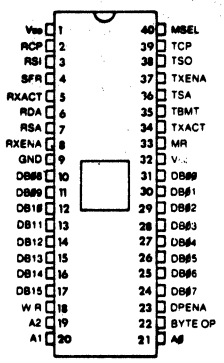

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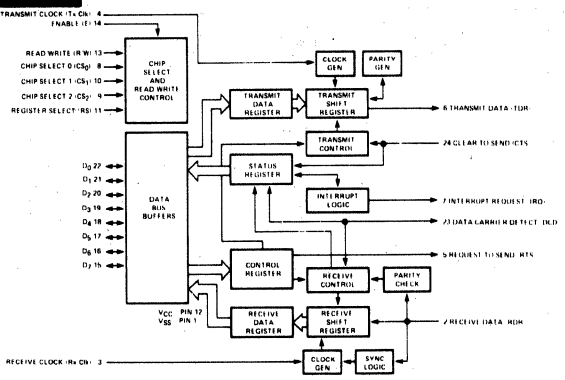
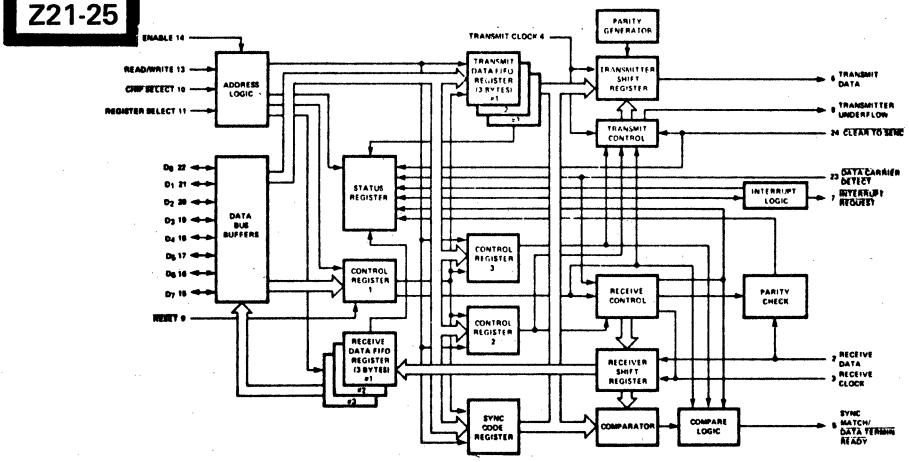
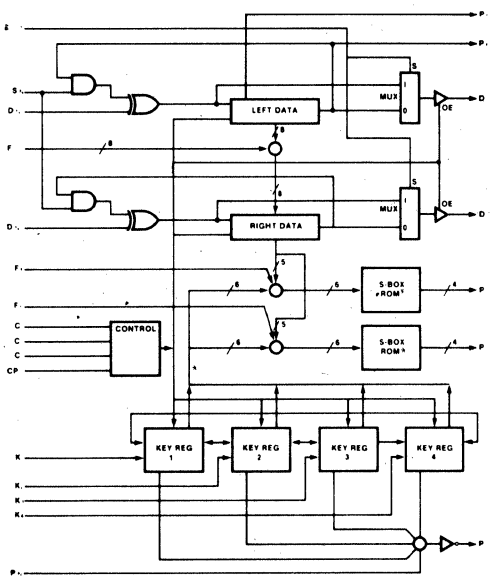


Z21-25



Z22-01



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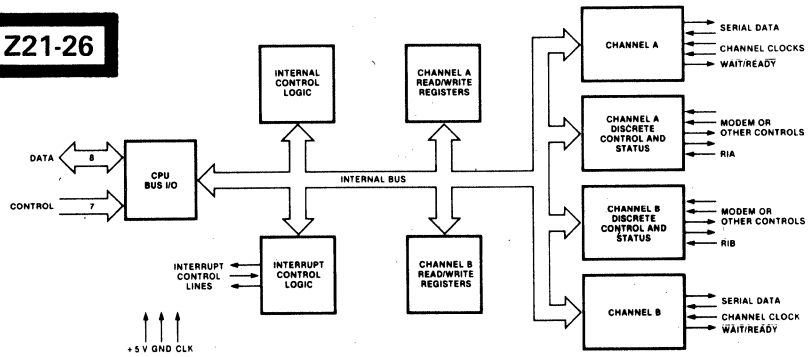
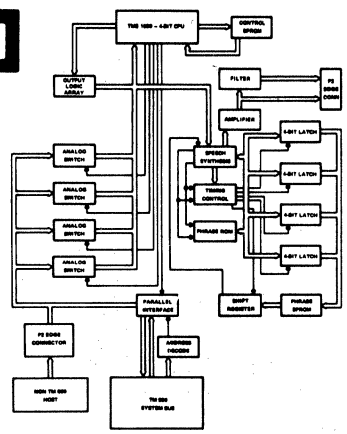
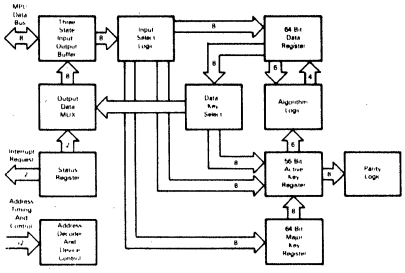


Z22-2



Z22-3



19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

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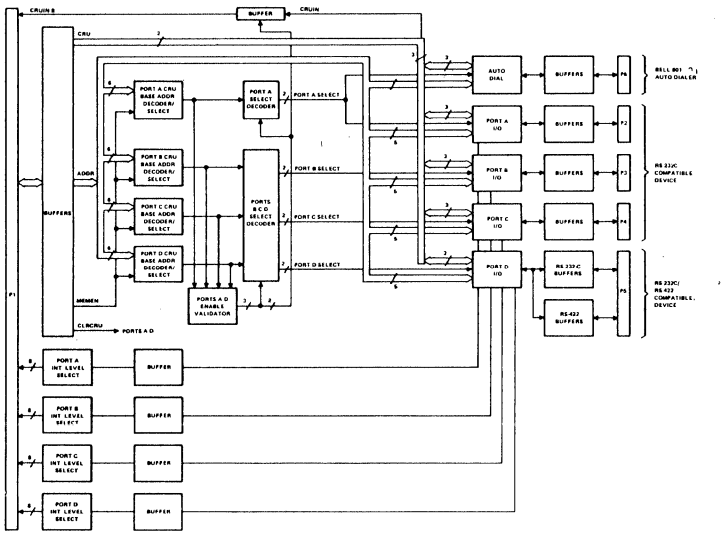
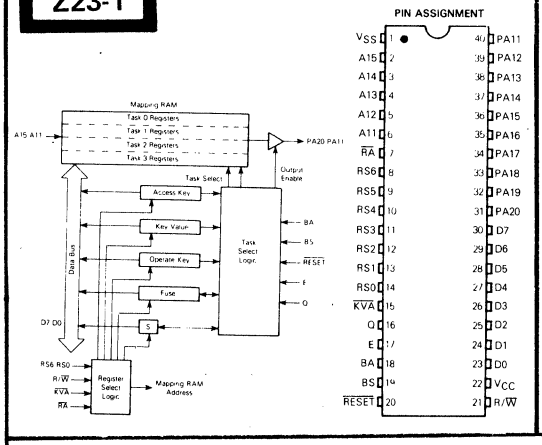
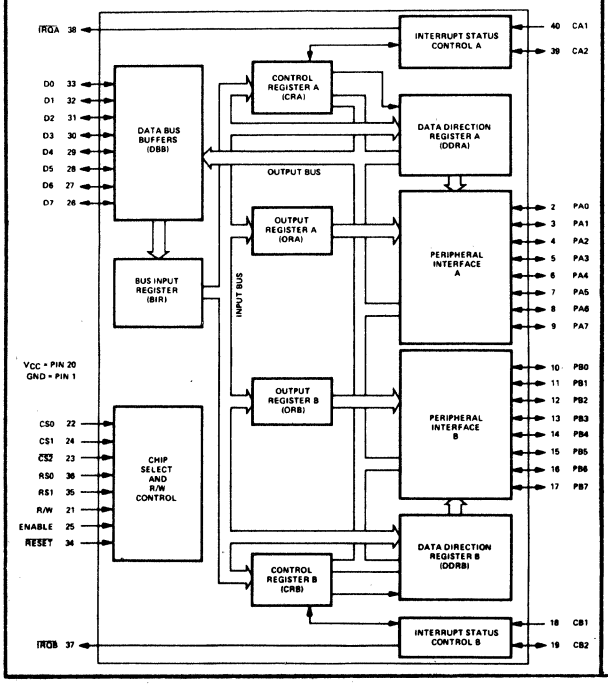


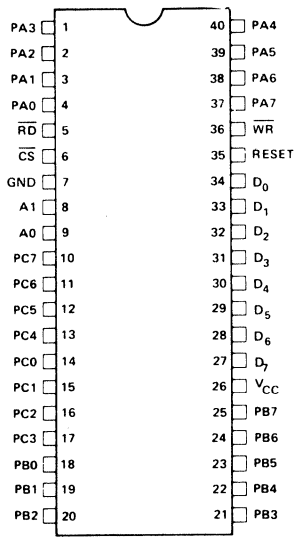
Z23-1

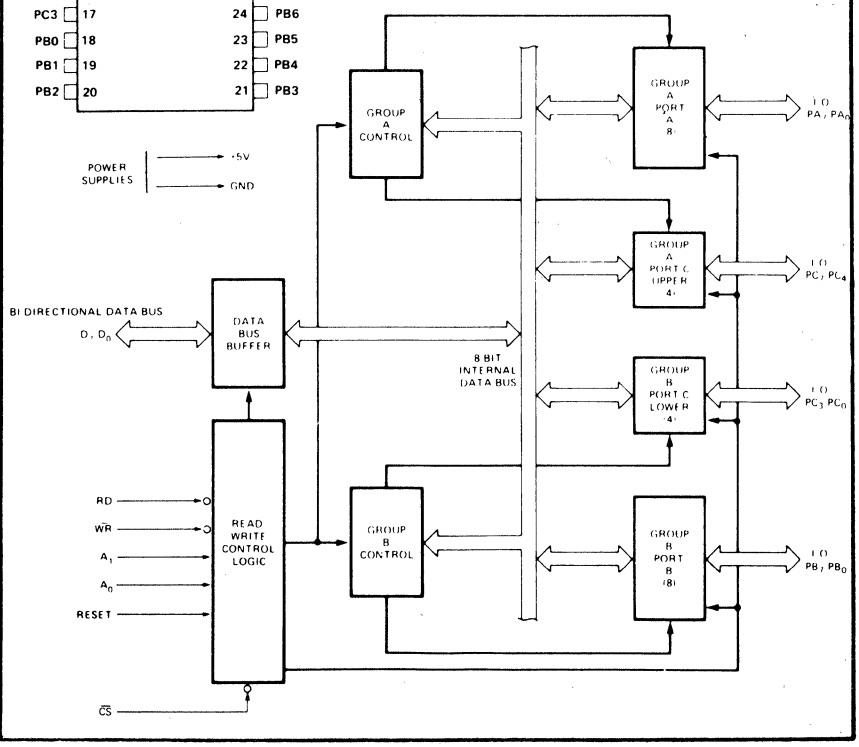


Z30-1

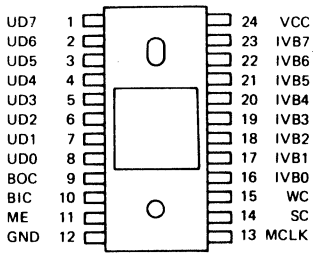


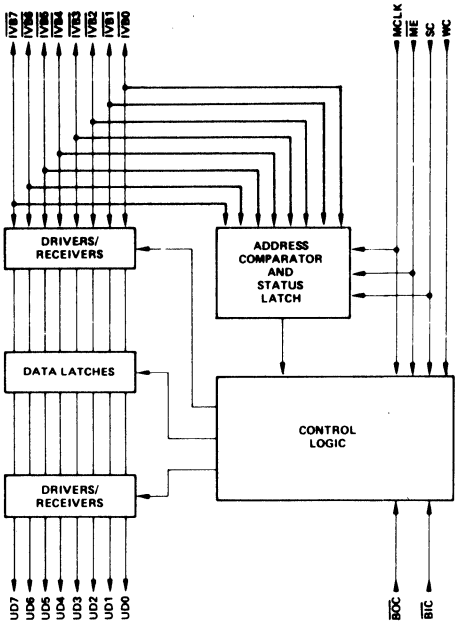
Z30-3



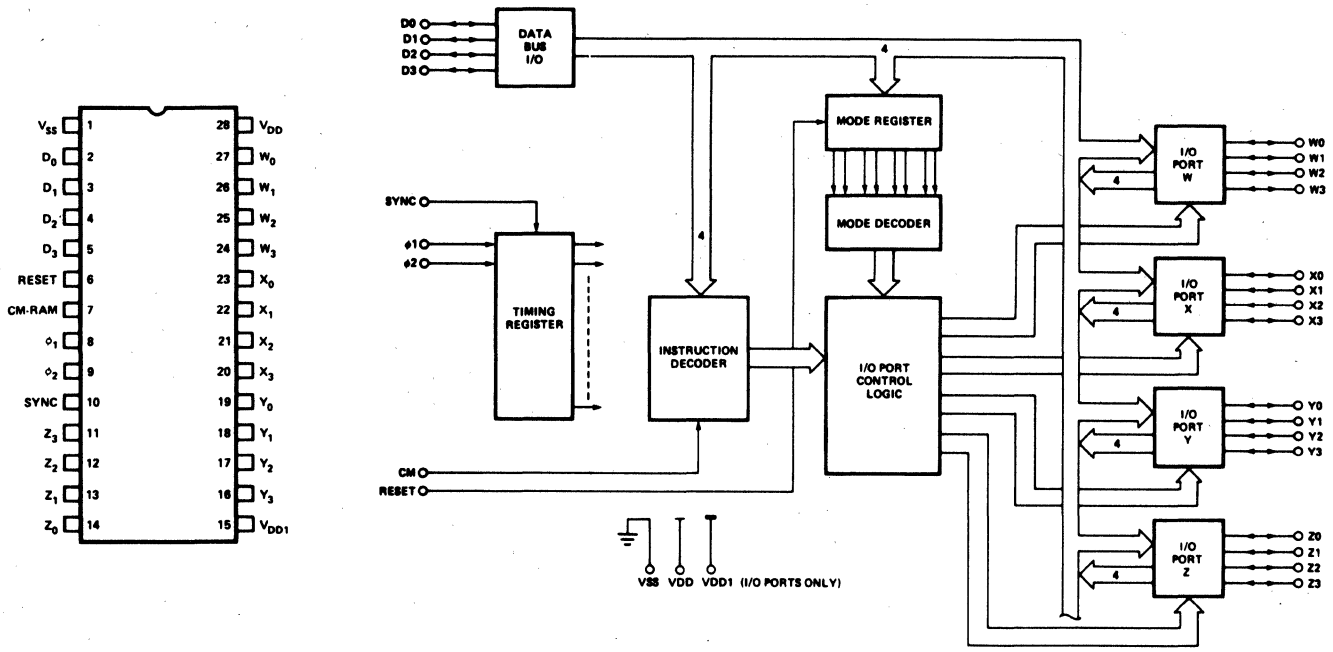


Z30-2

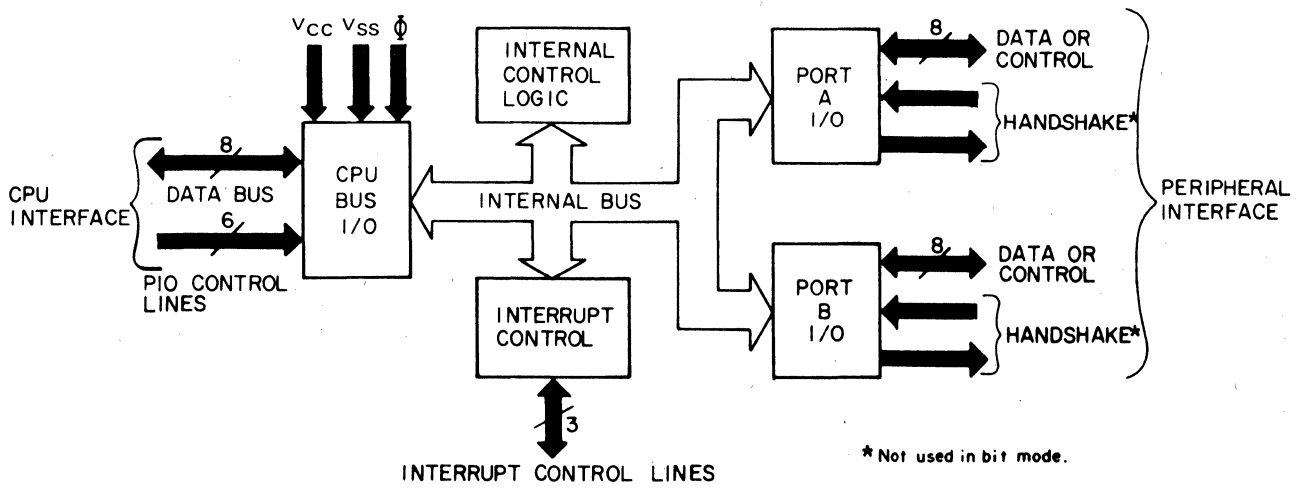




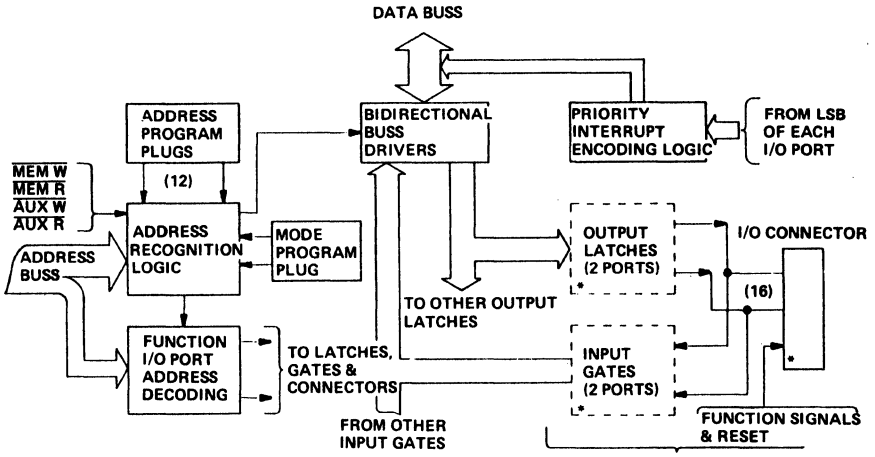
Z30-4


VSS 1
D0 2
D1 3
D2 4
D3 5
RESET 6
CM-RAM 7
Φ1 8
Φ2 9
SYNC 10
Z3 11
Z2 12
Z1 13
Z0 14
28 VDD
27 W0
26 W1
25 W2
24 W3
23 X0
22 X1
21 X2
20 X3
19 Y0
18 Y1
17 Y2
16 Y3
15 VDD1
D0
D1
D2
D3
DATA BUS I/O
4
MODE REGISTER
MODE DECODER
SYNC
Φ1
Φ2
TIMING REGISTER
INSTRUCTION DECODER
I/O PORT CONTROL LOGIC
CM
RESET
I/O PORT W
I/O PORT X
I/O PORT Y
I/O PORT Z
W0
W1
W2
W3
X0
X1
X2
X3
Y0
Y1
Y2
Y3
Z0
Z1
Z2
Z3
VSS VDD VDD1 (I/O PORTS ONLY)

Z30-5


VCC VSS Φ
INTERNAL CONTROL LOGIC
8
DATA OR CONTROL
PORT A I/O
HANDSHAKE*
CPU INTERFACE
8
DATA BUS
6
PIO CONTROL LINES
CPU BUS I/O
INTERNAL BUS
PERIPHERAL INTERFACE
INTERRUPT CONTROL
PORT B I/O
8
DATA OR CONTROL
HANDSHAKE*
3
INTERRUPT CONTROL LINES
* Not used in bit mode.

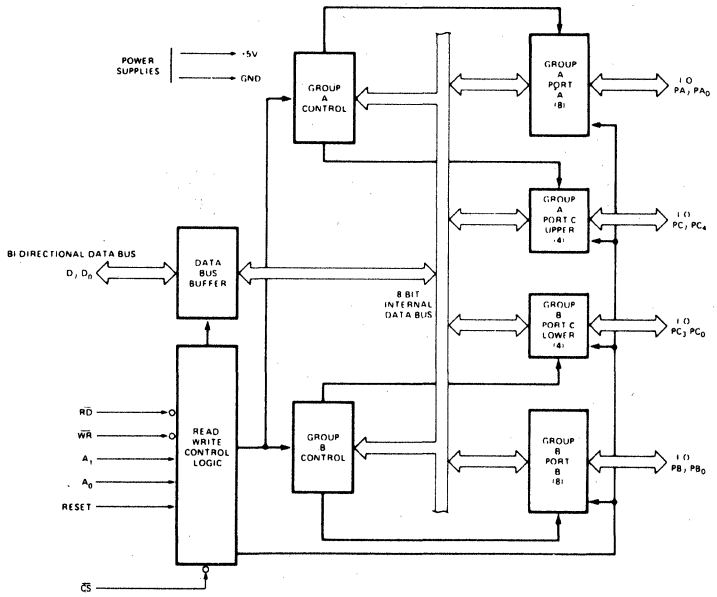
Z30-6

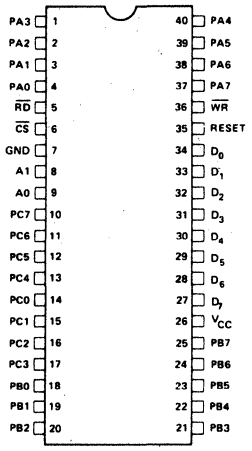


PIN		J1	J2	J3	J4
	1	GND	GND	GND	GND
14		GND	GND	GND	GND
	2	D7	D7	D7	D7
15		D6	D6	D6	D6
	3	D5	D5	D5	D5
16		D4 SECTION	D4 SECTION	D4 SECTION	D4 SECTION
	4	D3 A	D3 A	D3 A	D3 A
17		D2 (PORT	D2 (PORT	D2 (PORT	D2 (PORT
	5	D1 7)	D1 5)	D1 3)	D1 1)
18		D0	D0	D0	D0
	6				
19		$\overline{CS16}$	$\overline{CS14}$	$\overline{CS12}$	
	7	$\overline{CS17}$	$\overline{CS15}$	$\overline{CS13}$	
20					
	8				
21		$\overline{(MRST+PRST)}$	$\overline{MRST+PRST)}$	$\overline{(MRST+PRST)}$	$\overline{(MRST+PRST)}$
	9	GND	GND	GND	GND
22		GND	GND	GND	GND
	10	D7	D7	D7	D7
23		D6	D6	D6	D6
	11	D5	D5	D5	D5
24		D4 SECTION	D4 SECTION	D4 SECTION	D4 SECTION
	12	D3 B	D3 B	D3 B	D3 B
25		D2 (PORT	D2 (PORT	D2 (PORT	D2 (PORT
	13	D1 6)	D1 4)	D1 2)	D1 0)
26		D0	D0	D0	D0

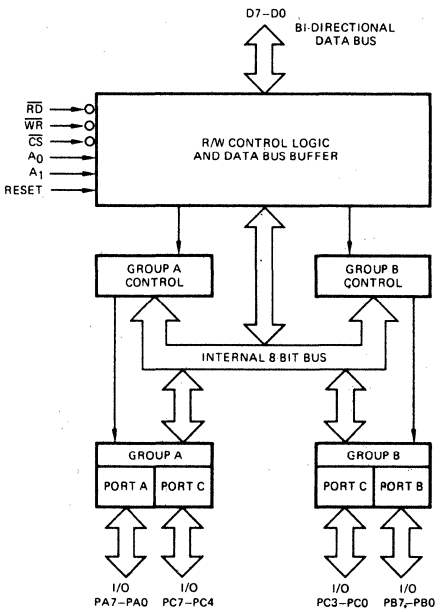
CONNECTOR PIN ASSIGNMENTS

Z30-7

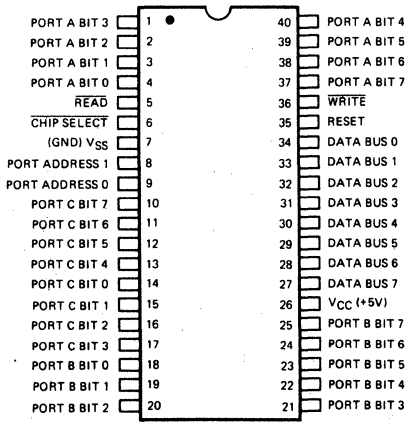




Z30-8

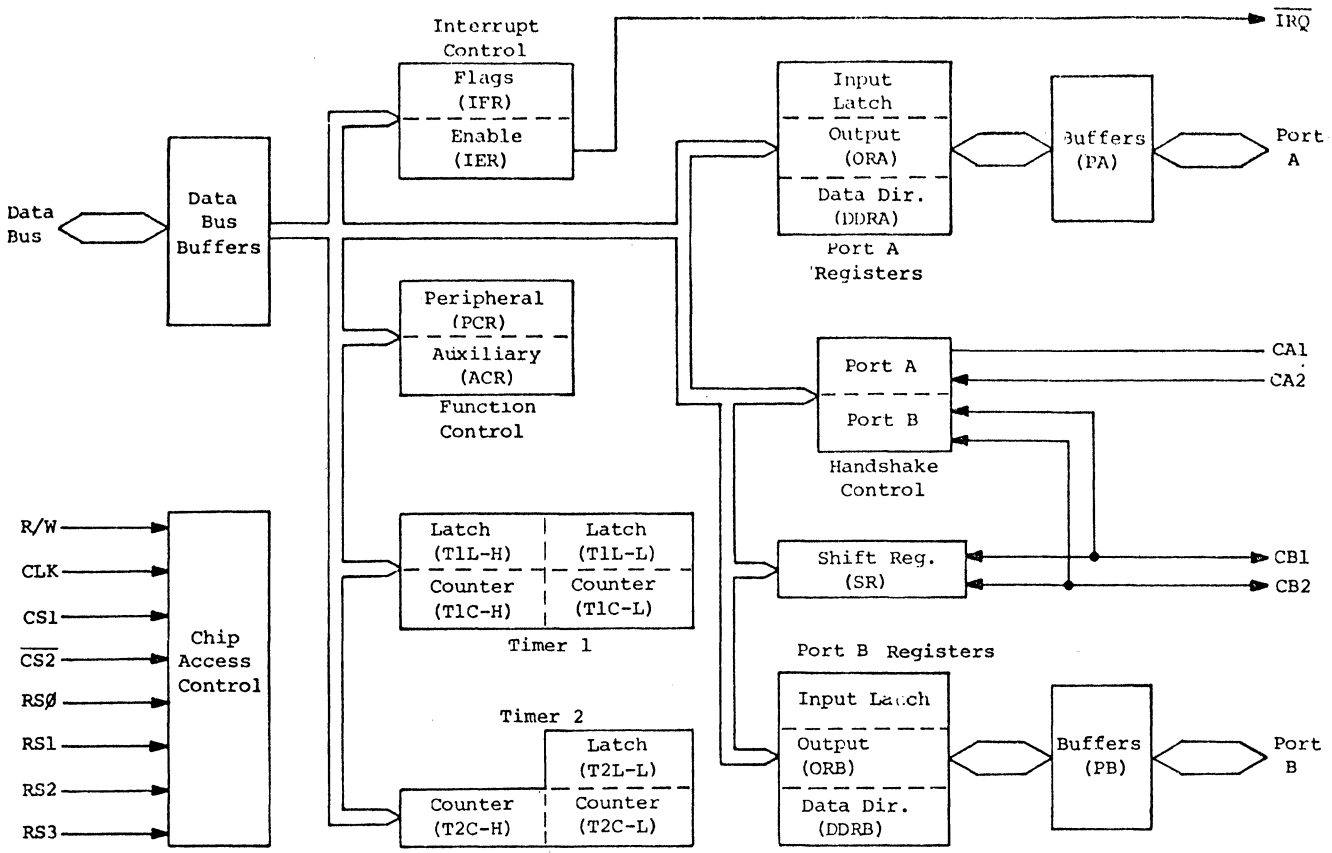


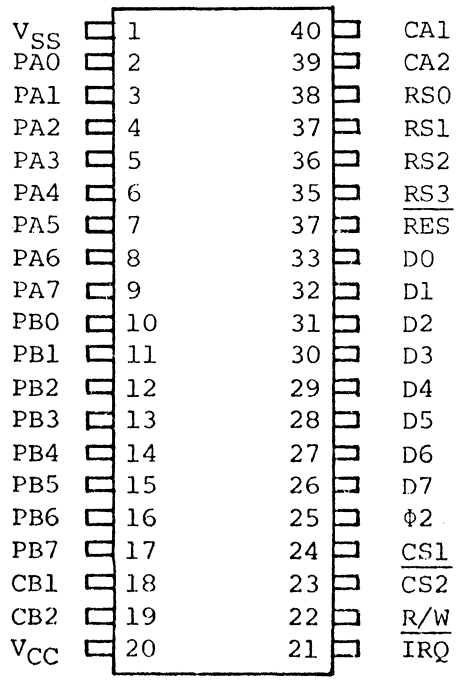
Top View



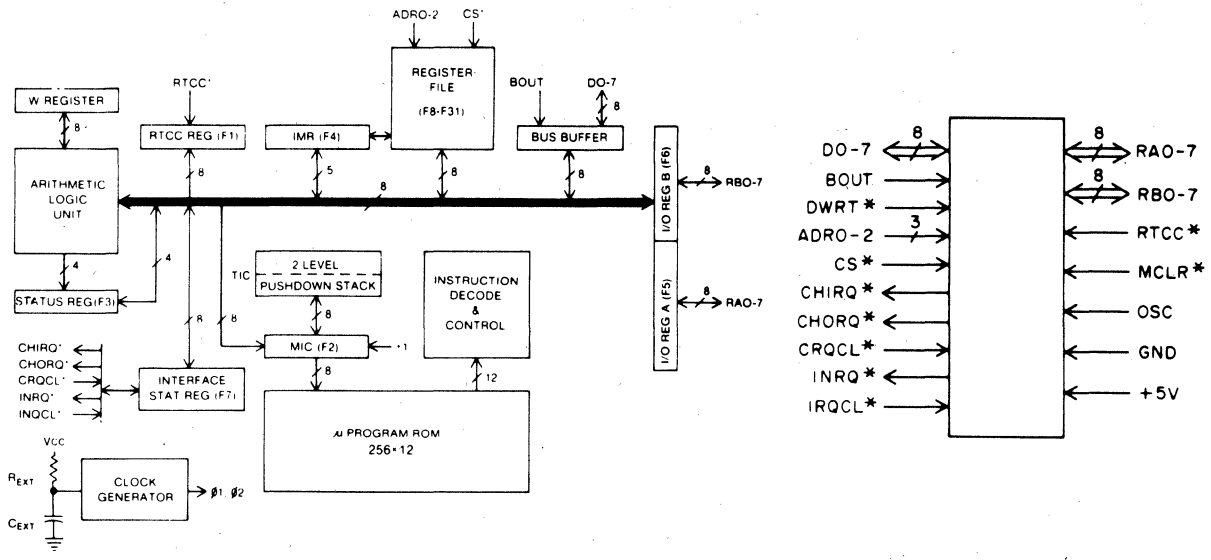
Pin 1 is marked for orientation.

Z30-9

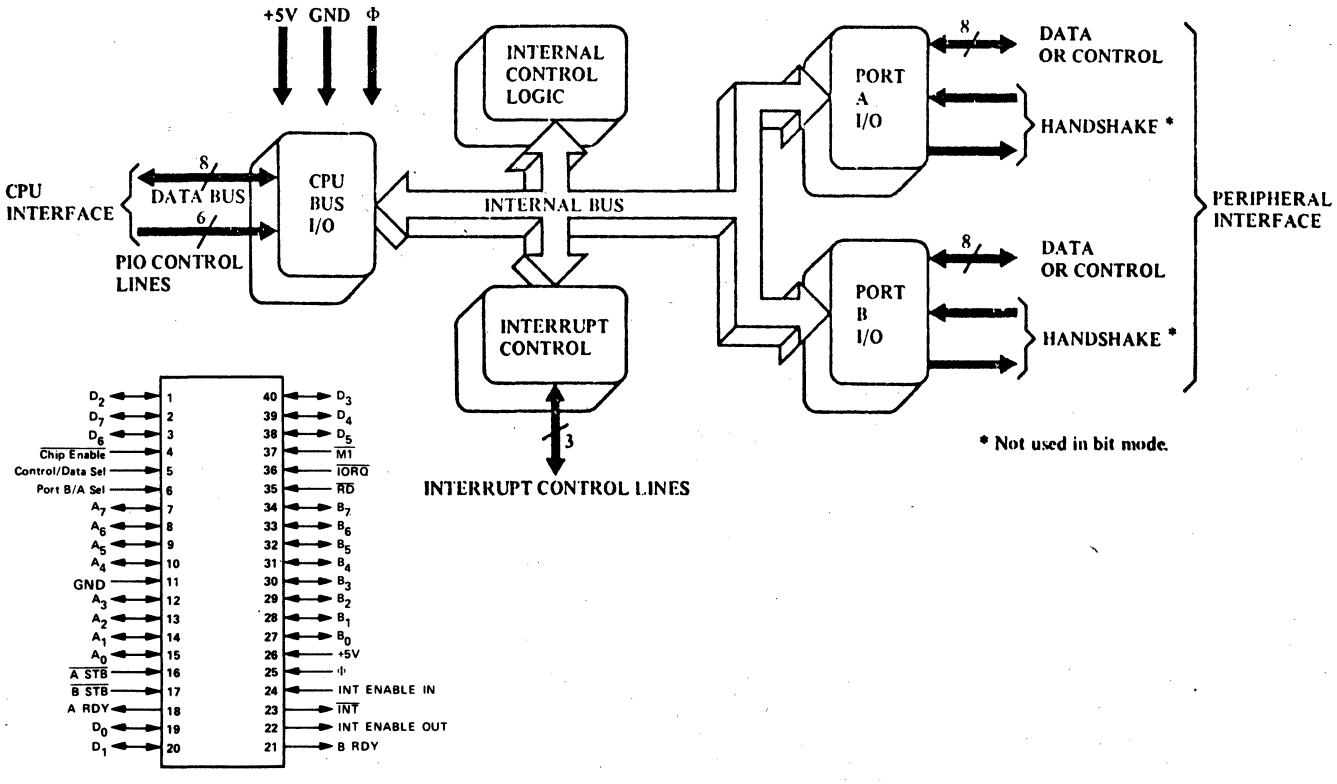

IRQ
Interrupt Control
Flags (IFR)
Enable (IER)
Input Latch
Output (ORA)
Data Dir. (DDRA)
Port A Registers
Buffers (PA)
Port A
Data Bus
Data Bus Buffers
Peripheral (PCR)
Auxiliary (ACR)
Function Control
Port A
Port B
Handshake Control
CA1
CA2
R/W
CLK
CS1
CS2
RSØ
RS1
RS2
RS3
Chip Access Control
Latch (T1L-H)
Latch (T1L-L)
Counter (T1C-H)
Counter (T1C-L)
Timer 1
Timer 2
Latch (T2L-L)
Counter (T2C-H)
Counter (T2C-L)
Shift Reg. (SR)
CB1
CB2
Port B Registers
Input Latch
Output (ORB)
Data Dir. (DDRB)
Buffers (PB)
Port B


V_{SS} 1
PA0 2
PA1 3
PA2 4
PA3 5
PA4 6
PA5 7
PA6 8
PA7 9
PB0 10
PB1 11
PB2 12
PB3 13
PB4 14
PB5 15
PB6 16
PB7 17
CB1 18
CB2 19
V_{CC} 20
40 CA1
39 CA2
38 RS0
37 RS1
36 RS2
35 $\overline{RS3}$
37 $\overline{RES}$
33 D0
32 D1
31 D2
30 D3
29 D4
28 D5
27 D6
26 D7
25 Φ2
24 $\overline{CS1}$
23 $\overline{CS2}$
22 R/$\overline{W}$
21 $\overline{IRQ}$

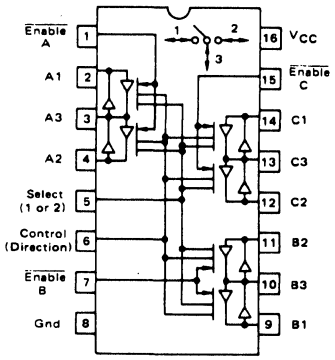
Z30-10


ADRO-2
CS*
REGISTER FILE (F8-F31)
W REGISTER
RTCC*
RTCC REG (F1)
IMR (F4)
BOUT
DO-7
BUS BUFFER
ARITHMETIC LOGIC UNIT
I/O REG B (F6)
RBO-7
I/O REG A (F5)
RAO-7
STATUS REG (F3)
TIC
2 LEVEL PUSHDOWN STACK
INSTRUCTION DECODE & CONTROL
CHIRQ*
CHORQ*
CRQCL*
INRQ*
INQCL*
INTERFACE STAT REG (F7)
MIC (F2)
PROGRAM ROM 256•12
VCC
REXT
CEXT
CLOCK GENERATOR
ø1, ø2
DO-7
BOUT
DWRT*
ADRO-2
CS*
CHIRQ*
CHORQ*
CRQCL*
INRQ*
IRQCL*
RAO-7
RBO-7
RTCC*
MCLR*
OSC
GND
+5V

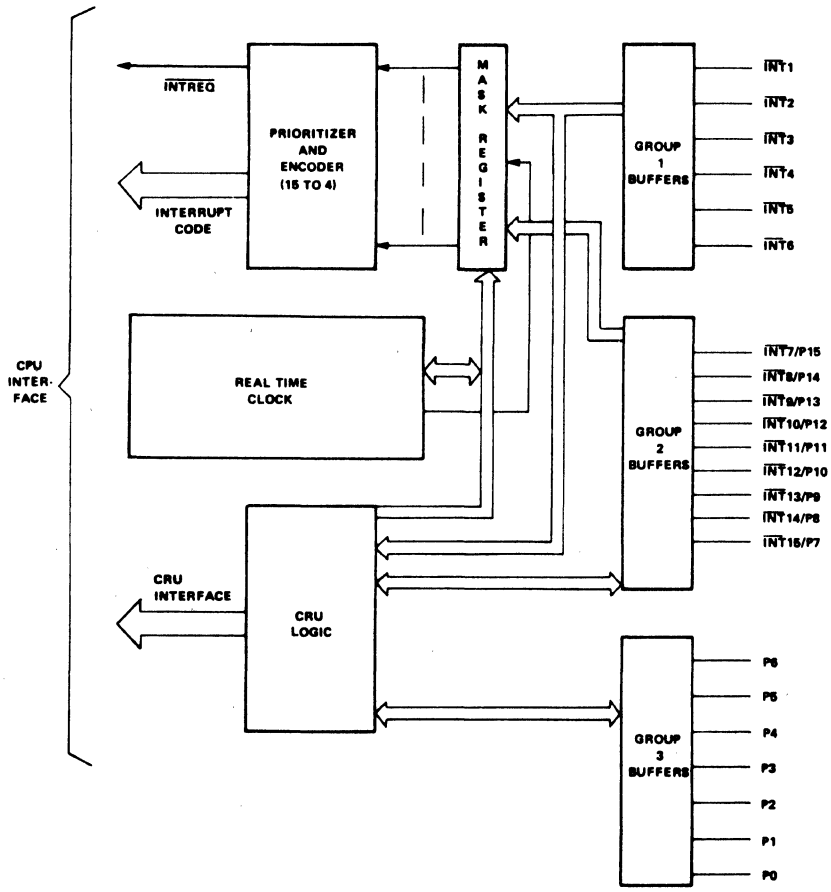
Z30-11

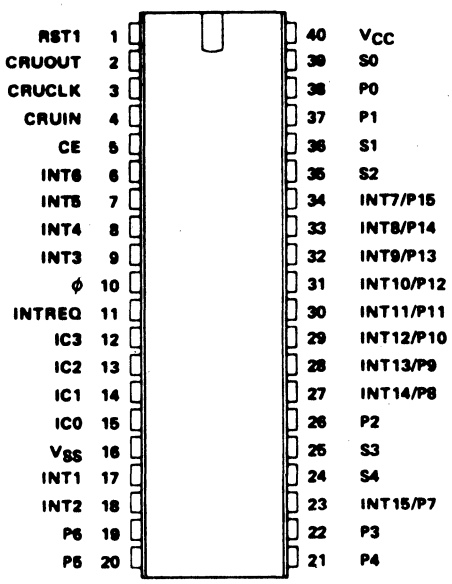

+5V GND Φ
INTERNAL CONTROL LOGIC
CPU INTERFACE
DATA BUS
PIO CONTROL LINES
CPU BUS I/O
INTERNAL BUS
PORT A I/O
DATA OR CONTROL
HANDSHAKE *
PORT B I/O
DATA OR CONTROL
HANDSHAKE *
PERIPHERAL INTERFACE
INTERRUPT CONTROL
INTERRUPT CONTROL LINES
* Not used in bit mode.
D2 1
D7 2
D6 3
Chip Enable 4
Control/Data Sel 5
Port B/A Sel 6
A7 7
A6 8
A5 9
A4 10
GND 11
A3 12
A2 13
A1 14
A0 15
A STB 16
B STB 17
A RDY 18
D0 19
D1 20
40 D3
39 D4
38 D5
37 M1
36 IORQ
35 RD
34 B7
33 B6
32 B5
31 B4
30 B3
29 B2
28 B1
27 B0
26 +5V
25 Φ
24 INT ENABLE IN
23 INT
22 INT ENABLE OUT
21 B RDY

Z30-12

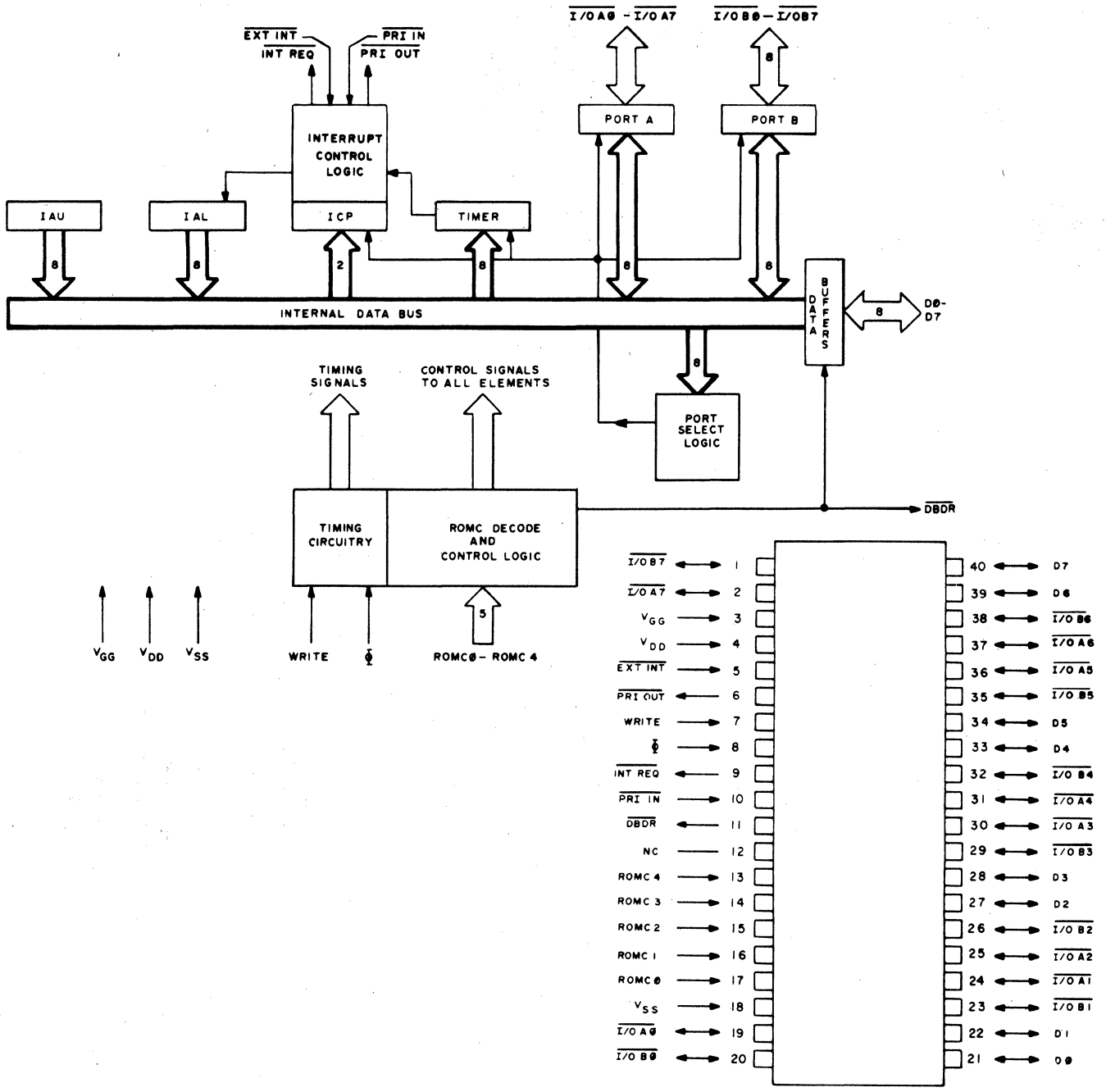

Enable A
A1
A3
A2
Select (1 or 2)
Control (Direction)
Enable B
Gnd
Vcc
Enable C
C1
C3
C2
B2
B3
B1

Z30-13

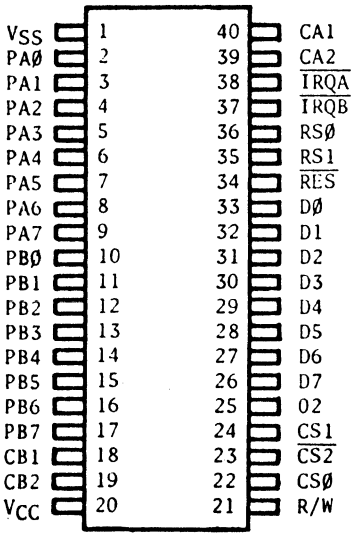

INTREQ
INTERRUPT CODE
PRIORITIZER AND ENCODER (15 TO 4)
MASK REGISTER
GROUP 1 BUFFERS
INT1
INT2
INT3
INT4
INT5
INT6
CPU INTER-FACE
REAL TIME CLOCK
GROUP 2 BUFFERS
INT7/P15
INT8/P14
INT9/P13
INT10/P12
INT11/P11
INT12/P10
INT13/P9
INT14/P8
INT15/P7
CRU INTERFACE
CRU LOGIC
GROUP 3 BUFFERS
P6
P5
P4
P3
P2
P1
P0

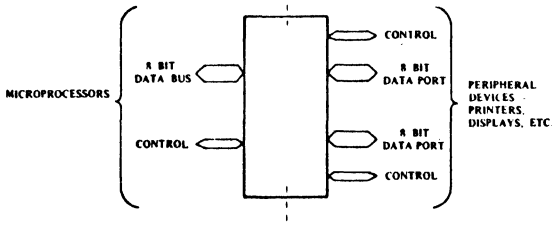

RST1 1
CRUOUT 2
CRUCLK 3
CRUIN 4
CE 5
INT6 6
INT5 7
INT4 8
INT3 9
ϕ 10
INTREQ 11
IC3 12
IC2 13
IC1 14
IC0 15
VSS 16
INT1 17
INT2 18
P6 19
P5 20
40 VCC
39 S0
38 P0
37 P1
36 S1
35 S2
34 INT7/P15
33 INT8/P14
32 INT9/P13
31 INT10/P12
30 INT11/P11
29 INT12/P10
28 INT13/P9
27 INT14/P8
26 P2
25 S3
24 S4
23 INT15/P7
22 P3
21 P4

Z30-14

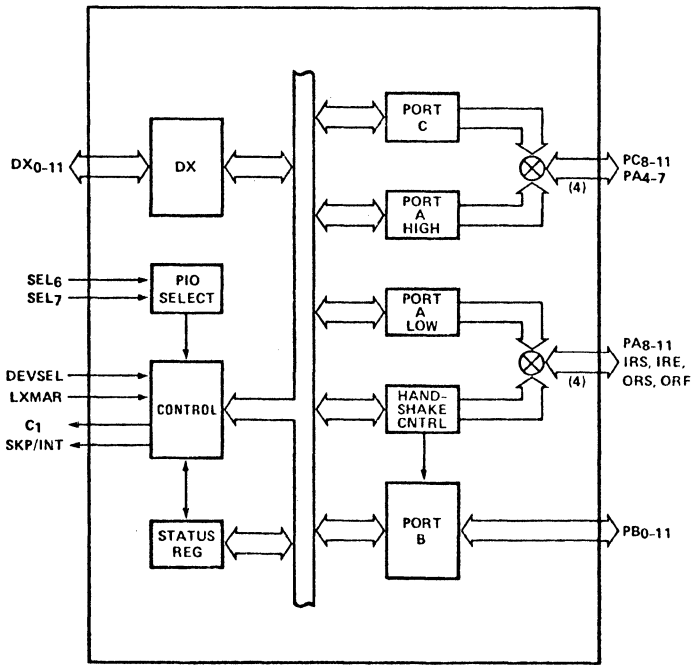

EXT INT
INT REQ
PRI IN
PRI OUT
INTERRUPT CONTROL LOGIC
IAU
IAL
ICP
TIMER
I/O A0 - I/O A7
I/O B0 - I/O B7
PORT A
PORT B
8
2
INTERNAL DATA BUS
DATA BUFFERS
D0-D7
PORT SELECT LOGIC
TIMING SIGNALS
CONTROL SIGNALS TO ALL ELEMENTS
TIMING CIRCUITRY
ROMC DECODE AND CONTROL LOGIC
DBDR
5
VGG
VDD
VSS
WRITE
Φ
ROMC0 - ROMC 4
I/O B7 1
I/O A7 2
VGG 3
VDD 4
EXT INT 5
PRI OUT 6
WRITE 7
Φ 8
INT REQ 9
PRI IN 10
DBDR 11
NC 12
ROMC 4 13
ROMC 3 14
ROMC 2 15
ROMC 1 16
ROMC 0 17
VSS 18
I/O A0 19
I/O B0 20
40 D7
39 D6
38 I/O B6
37 I/O A6
36 I/O A5
35 I/O B5
34 D5
33 D4
32 I/O B4
31 I/O A4
30 I/O A3
29 I/O B3
28 D3
27 D2
26 I/O B2
25 I/O A2
24 I/O A1
23 I/O B1
22 D1
21 D0

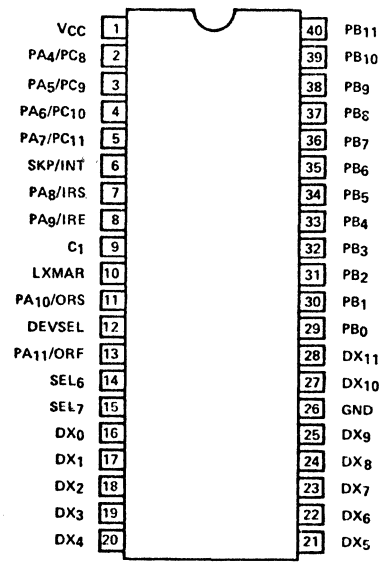
Z30-15


VSS 1 40 CA1
PAØ 2 39 CA2
PA1 3 38 IRQA
PA2 4 37 IRQB
PA3 5 36 RSØ
PA4 6 35 RS1
PA5 7 34 RES
PA6 8 33 DØ
PA7 9 32 D1
PBØ 10 31 D2
PB1 11 30 D3
PB2 12 29 D4
PB3 13 28 D5
PB4 14 27 D6
PB5 15 26 D7
PB6 16 25 02
PB7 17 24 CS1
CB1 18 23 CS2
CB2 19 22 CSØ
VCC 20 21 R/W

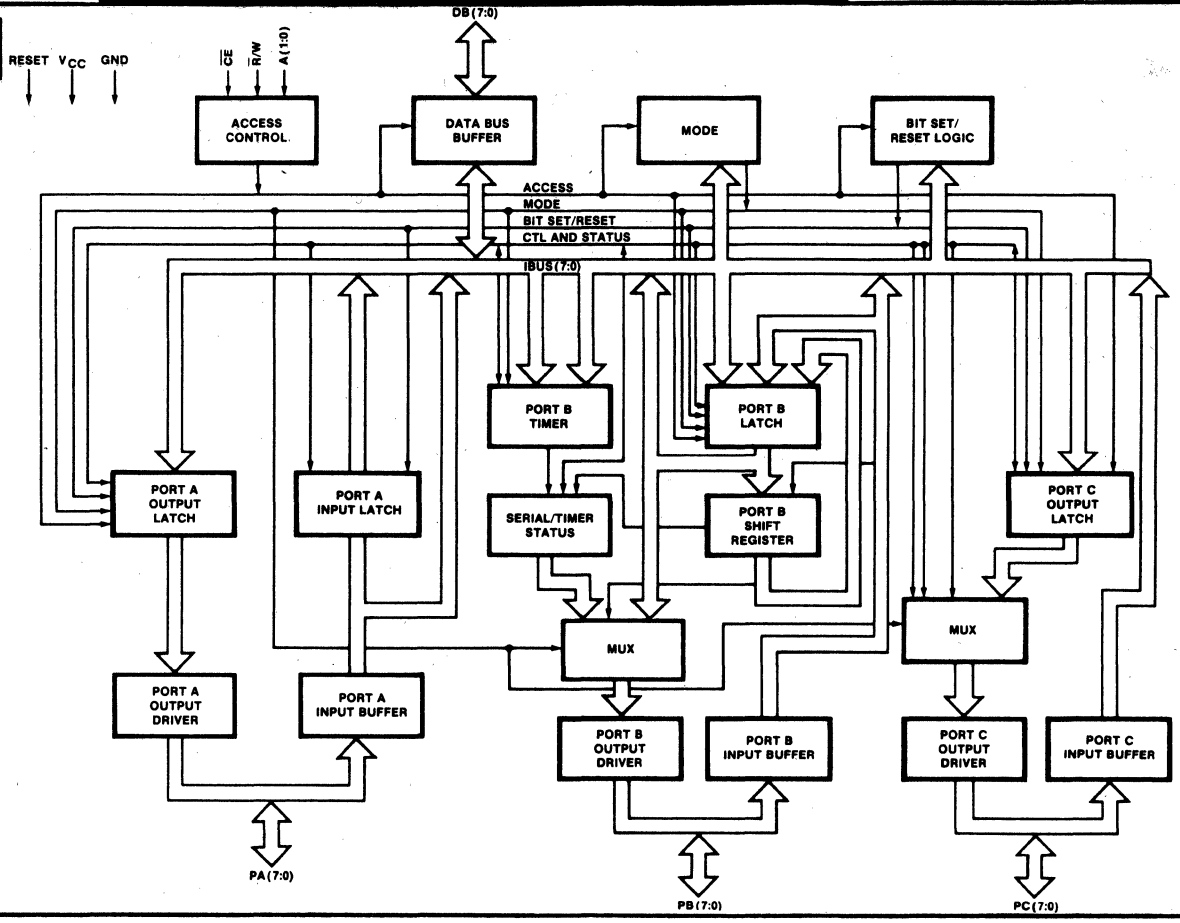

MICROPROCESSORS
8 BIT DATA BUS
CONTROL
CONTROL
8 BIT DATA PORT
8 BIT DATA PORT
CONTROL
PERIPHERAL DEVICES - PRINTERS, DISPLAYS, ETC

Z30-16

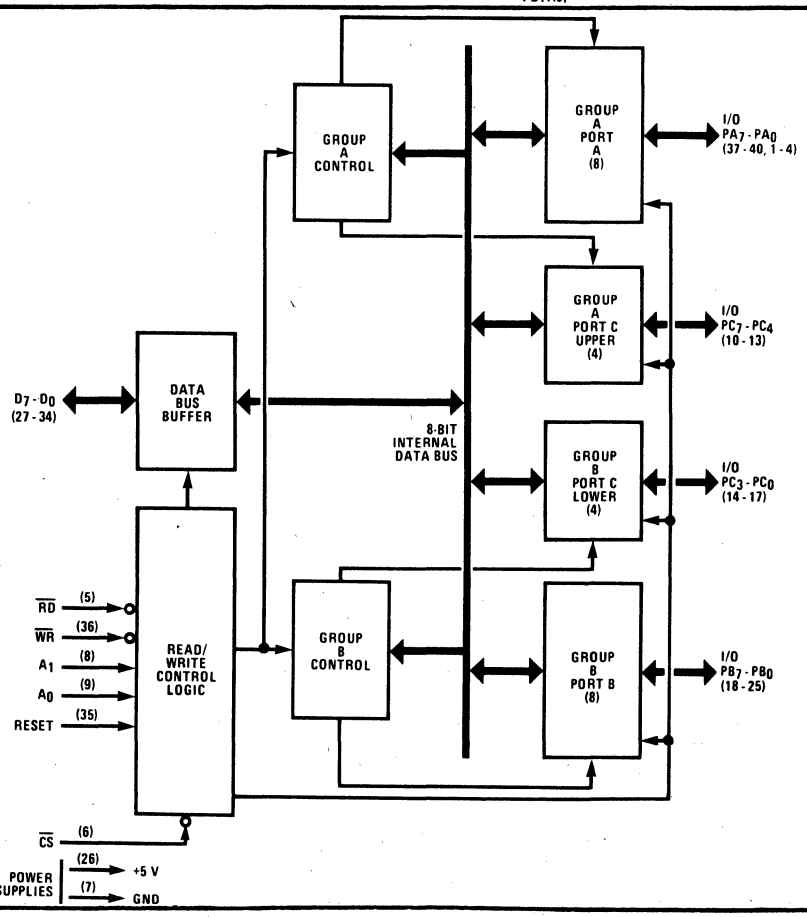

DX0-11
DX
PORT C
PORT A HIGH
PORT A LOW
HAND-SHAKE CNTRL
PORT B
(4)
(4)
PC8-11
PA4-7
PA8-11
IRS, IRE, ORS, ORF
SEL6
SEL7
PIO SELECT
DEVSEL
LXMAR
C1
SKP/INT
CONTROL
STATUS REG
PB0-11


VCC 1 40 PB11
PA4/PC8 2 39 PB10
PA5/PC9 3 38 PB9
PA6/PC10 4 37 PB8
PA7/PC11 5 36 PB7
SKP/INT 6 35 PB6
PA8/IRS 7 34 PB5
PA9/IRE 8 33 PB4
C1 9 32 PB3
LXMAR 10 31 PB2
PA10/ORS 11 30 PB1
DEVSEL 12 29 PB0
PA11/ORF 13 28 DX11
SEL6 14 27 DX10
SEL7 15 26 GND
DX0 16 25 DX9
DX1 17 24 DX8
DX2 18 23 DX7
DX3 19 22 DX6
DX4 20 21 DX5

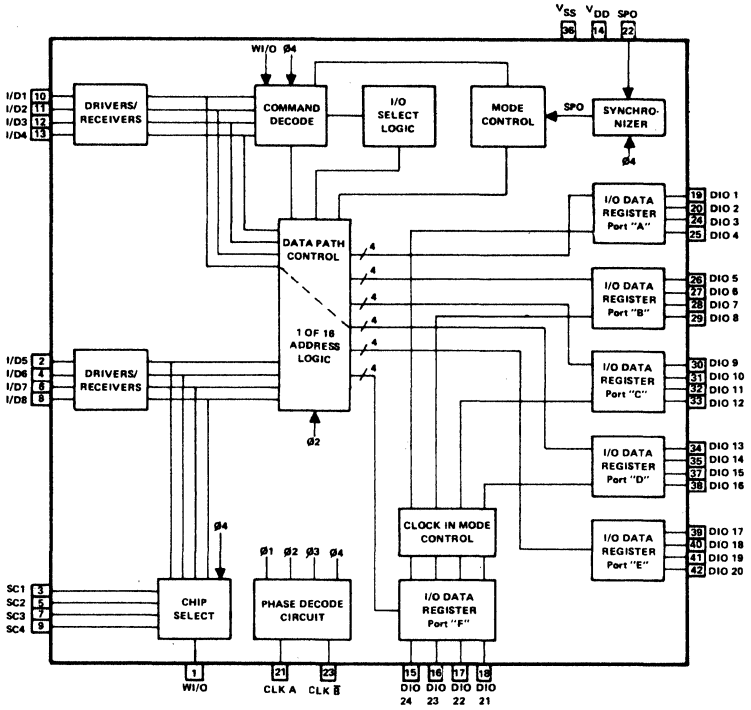
Z30-17

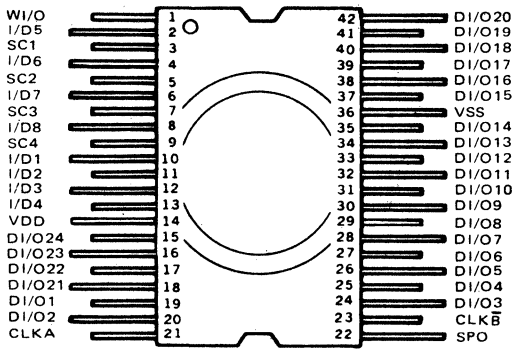

DB(7:0)
RESET
VCC
GND
CE
R/W
A(1:0)
ACCESS CONTROL
DATA BUS BUFFER
MODE
BIT SET/ RESET LOGIC
ACCESS
MODE
BIT SET/RESET
CTL AND STATUS
IBUS(7:0)
PORT B TIMER
PORT B LATCH
PORT A OUTPUT LATCH
PORT A INPUT LATCH
SERIAL/TIMER STATUS
PORT B SHIFT REGISTER
PORT C OUTPUT LATCH
MUX
MUX
PORT A OUTPUT DRIVER
PORT A INPUT BUFFER
PORT B OUTPUT DRIVER
PORT B INPUT BUFFER
PORT C OUTPUT DRIVER
PORT C INPUT BUFFER
PA(7:0)
PB(7:0)
PC(7:0)

Z30-18

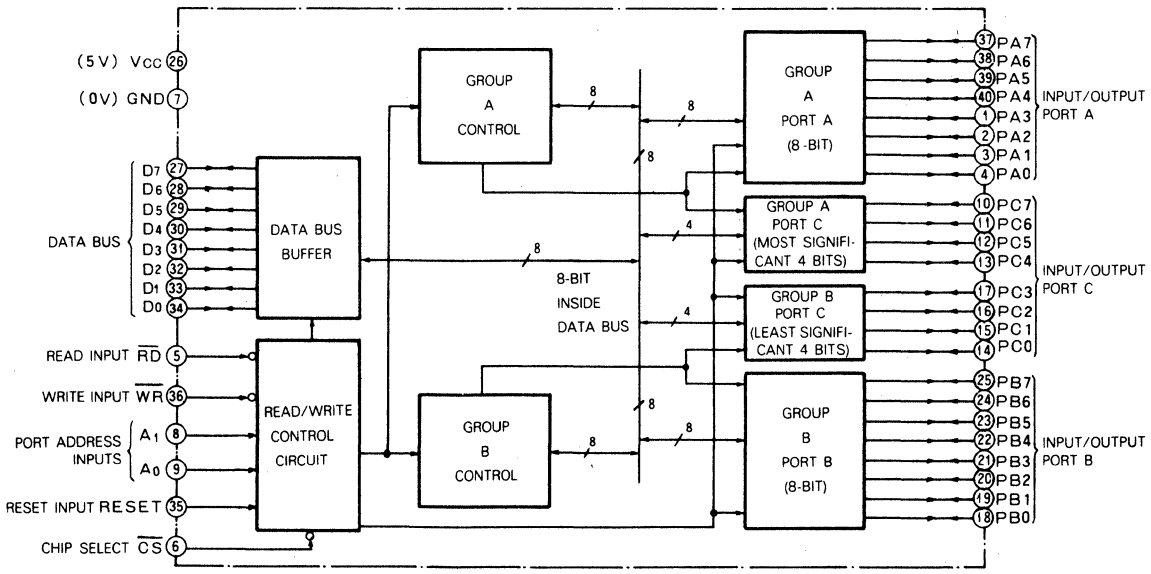

GROUP A CONTROL
GROUP A PORT A (8)
I/O PA7 - PA0 (37 - 40, 1 - 4)
GROUP A PORT C UPPER (4)
I/O PC7 - PC4 (10 - 13)
D7 - D0 (27 - 34)
DATA BUS BUFFER
8-BIT INTERNAL DATA BUS
GROUP B PORT C LOWER (4)
I/O PC3 - PC0 (14 - 17)
RD (5)
WR (36)
A1 (8)
A0 (9)
RESET (35)
READ/ WRITE CONTROL LOGIC
GROUP B CONTROL
GROUP B PORT B (8)
I/O PB7 - PB0 (18 - 25)
CS (6)
POWER SUPPLIES
(26) +5 V
(7) GND

Z30-19

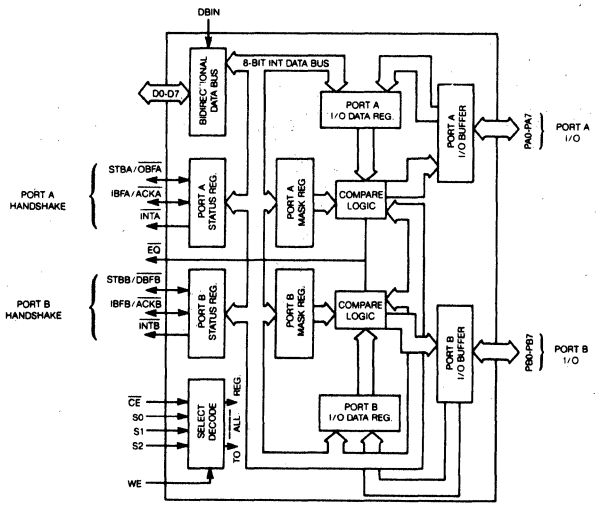

VSS 36
VDD 14
SPO 22
WI/O
Ø4
I/D1 10
I/D2 11
I/D3 12
I/D4 13
DRIVERS/ RECEIVERS
COMMAND DECODE
I/O SELECT LOGIC
MODE CONTROL
SYNCHRO-NIZER
I/O DATA REGISTER Port "A"
I/O DATA REGISTER Port "B"
I/O DATA REGISTER Port "C"
I/O DATA REGISTER Port "D"
I/O DATA REGISTER Port "E"
I/O DATA REGISTER Port "F"
DATA PATH CONTROL
1 OF 16 ADDRESS LOGIC
CLOCK IN MODE CONTROL
CHIP SELECT
PHASE DECODE CIRCUIT
Ø1 Ø2 Ø3 Ø4
SC1 3
SC2 5
SC3 7
SC4 9
I/D5 2
I/D6 4
I/D7 6
I/D8 8
DIO 1 19
DIO 2 20
DIO 3 24
DIO 4 25
DIO 5 26
DIO 6 27
DIO 7 28
DIO 8 29
DIO 9 30
DIO 10 31
DIO 11 32
DIO 12 33
DIO 13 34
DIO 14 35
DIO 15 37
DIO 16 38
DIO 17 39
DIO 18 40
DIO 19 41
DIO 20 42
WI/O 1
CLK A 21
CLK B 22
DIO 24 15
DIO 23 16
DIO 22 17
DIO 21 18


WI/O 1
I/D5 2
SC1 3
I/D6 4
SC2 5
I/D7 6
SC3 7
I/D8 8
SC4 9
I/D1 10
I/D2 11
I/D3 12
I/D4 13
VDD 14
DI/O24 15
DI/O23 16
DI/O22 17
DI/O21 18
DI/O1 19
DI/O2 20
CLKA 21
42 DI/O20
41 DI/O19
40 DI/O18
39 DI/O17
38 DI/O16
37 DI/O15
36 VSS
35 DI/O14
34 DI/O13
33 DI/O12
32 DI/O11
31 DI/O10
30 DI/O9
29 DI/O8
28 DI/O7
27 DI/O6
26 DI/O5
25 DI/O4
24 DI/O3
23 CLKB
22 SPO

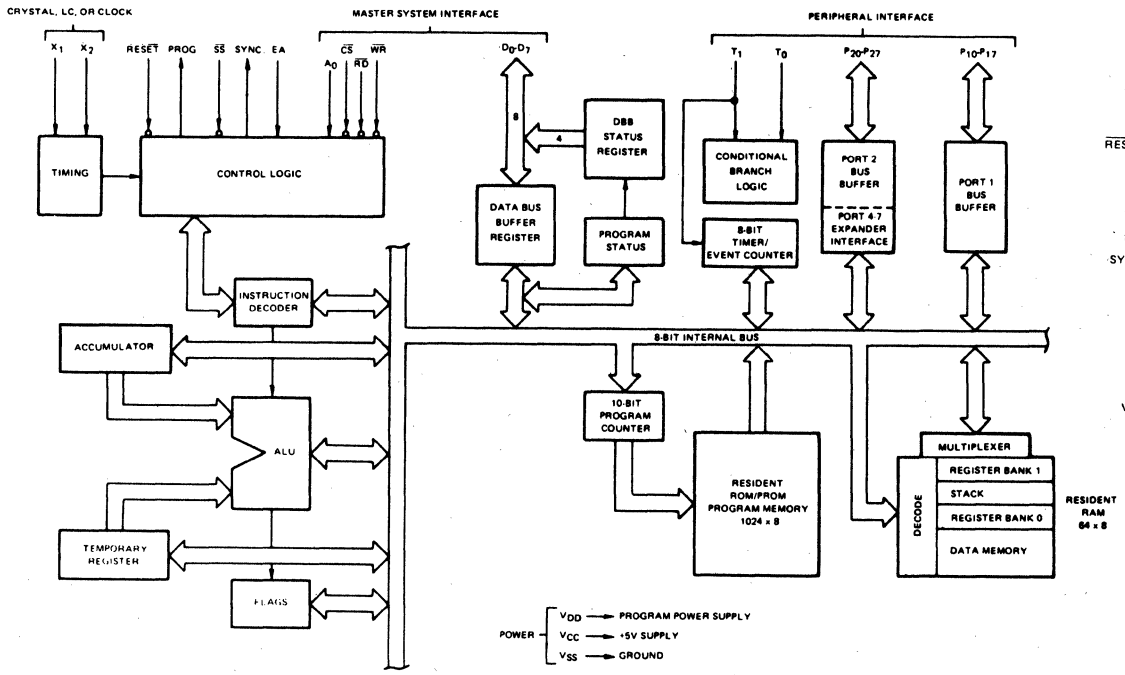
Z30-20


(5V) VCC 26
(0V) GND 7
DATA BUS
D7 27
D6 28
D5 29
D4 30
D3 31
D2 32
D1 33
D0 34
DATA BUS BUFFER
READ INPUT RD 5
WRITE INPUT WR 36
PORT ADDRESS INPUTS
A1 8
A0 9
RESET INPUT RESET 35
CHIP SELECT CS 6
READ/WRITE CONTROL CIRCUIT
GROUP A CONTROL
GROUP B CONTROL
8-BIT INSIDE DATA BUS
GROUP A PORT A (8-BIT)
GROUP A PORT C (MOST SIGNIFI-CANT 4 BITS)
GROUP B PORT C (LEAST SIGNIFI-CANT 4 BITS)
GROUP B PORT B (8-BIT)
37 PA7
38 PA6
39 PA5
40 PA4
1 PA3
2 PA2
3 PA1
4 PA0
INPUT/OUTPUT PORT A
10 PC7
11 PC6
12 PC5
13 PC4
17 PC3
16 PC2
15 PC1
14 PC0
INPUT/OUTPUT PORT C
25 PB7
24 PB6
23 PB5
22 PB4
21 PB3
20 PB2
19 PB1
18 PB0
INPUT/OUTPUT PORT B

Z30-21



Z30-22

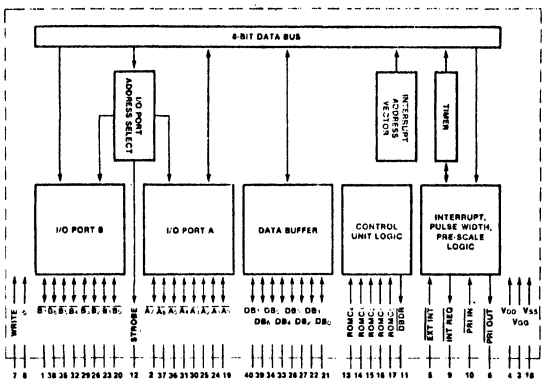


Z30-22a Pin out only applies

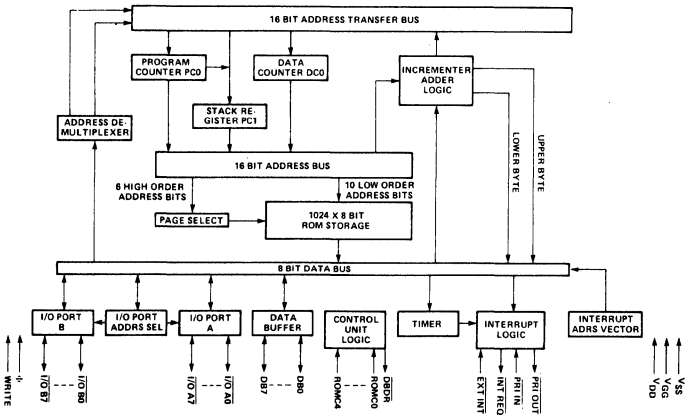
29. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

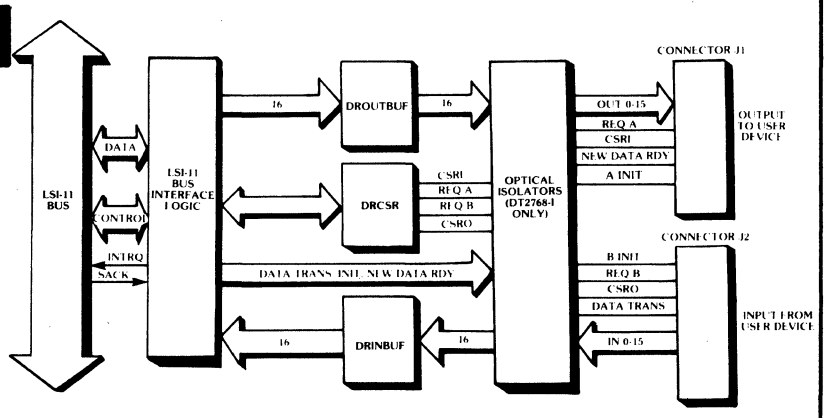
Z30-23



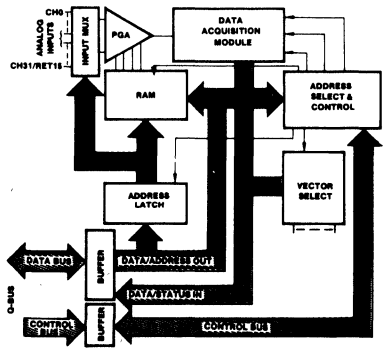
Z30-24



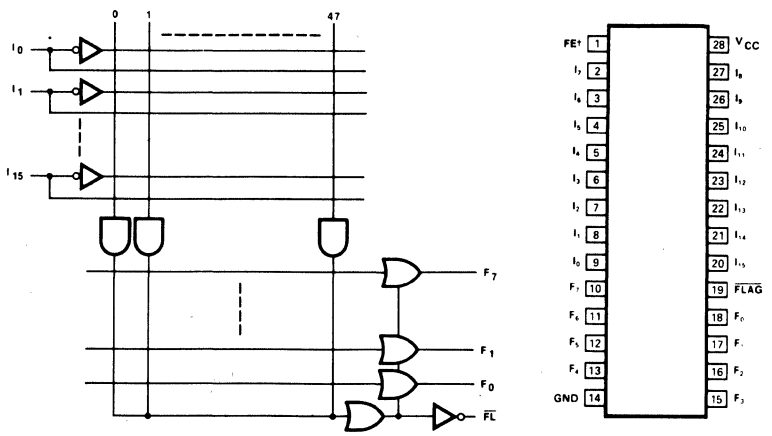
Z30-25



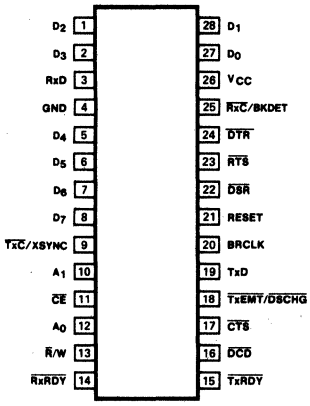
Z30-26

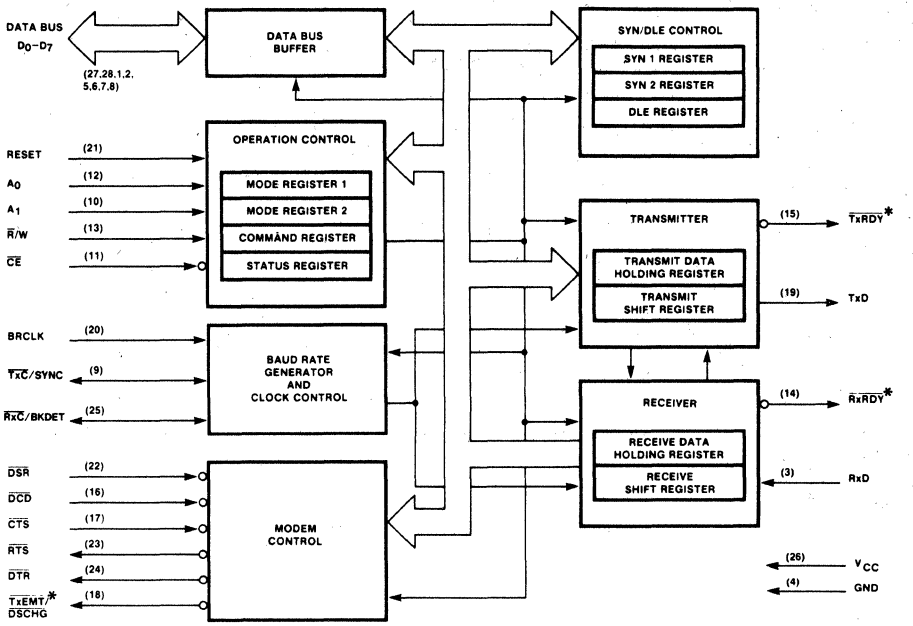


Z30-27

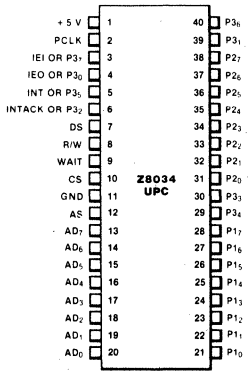


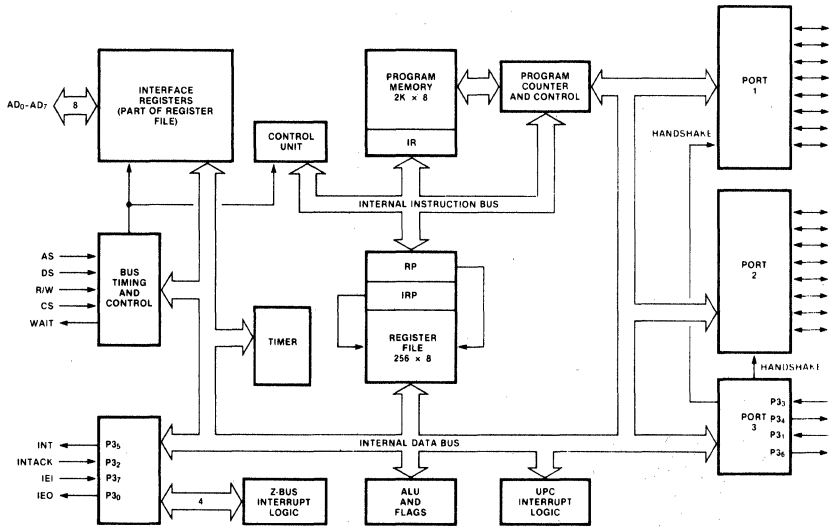
Z30-28



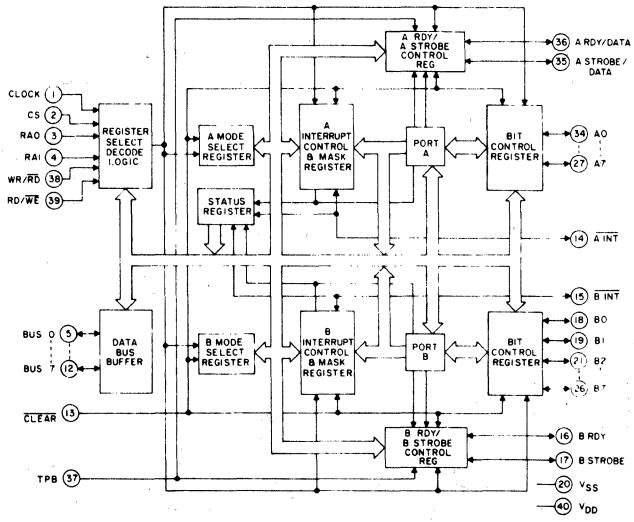


Z30-29





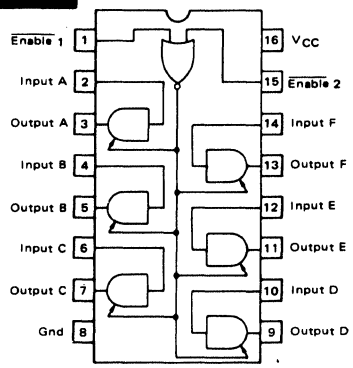
Z30-30



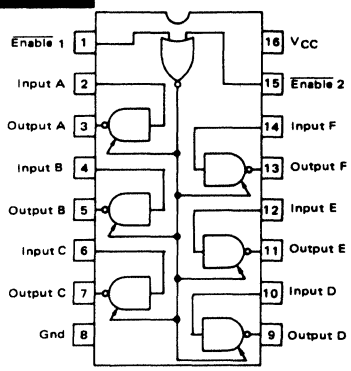
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

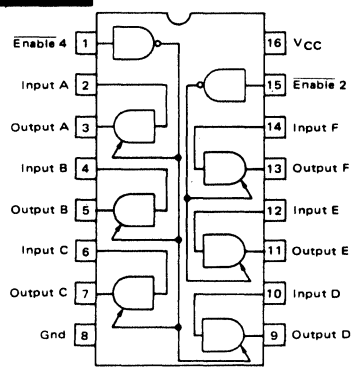
Z31-1



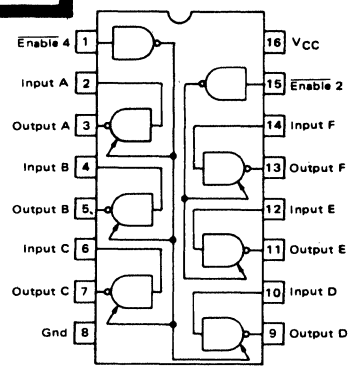
Z31-2



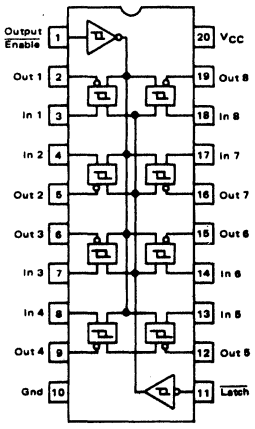
Z31-3



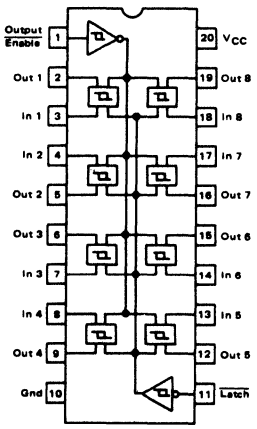
Z31-4



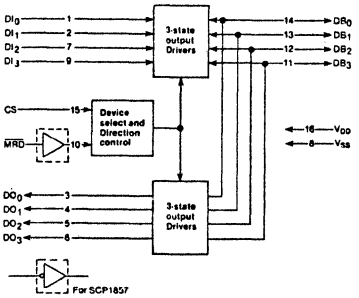
Z31-5



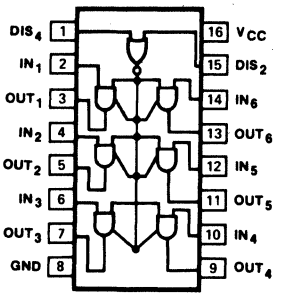
Z31-6



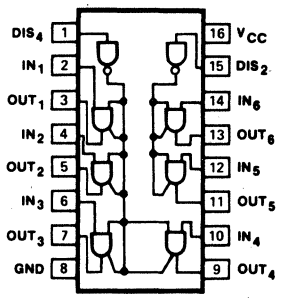
Z31-7



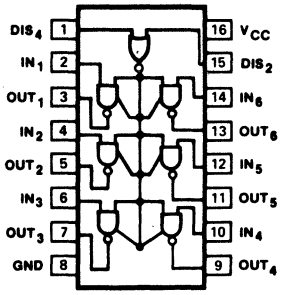
Z31-8



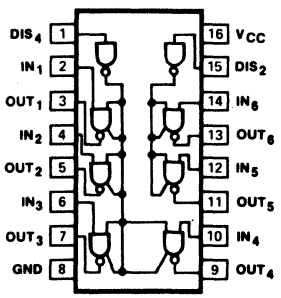
Z31-9



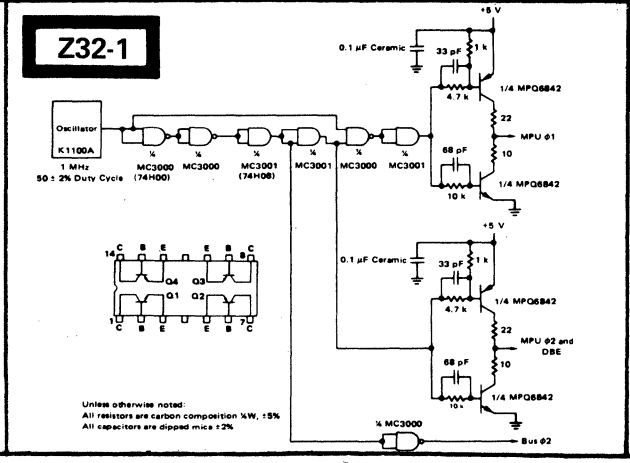
Z31-10



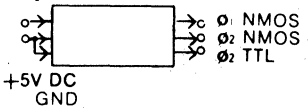
Z31-11



Z32-1



Z32-2

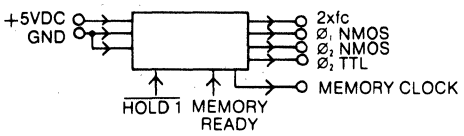


PIN	CONNECTION
1	GND
3	NC
5	ø2 TTL
7	Vcc (+5VDC)
12	ø2 NMOS
13	ø1 NMOS
18	GND
20	NC
22	NC
24	NC

19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

Z32-3



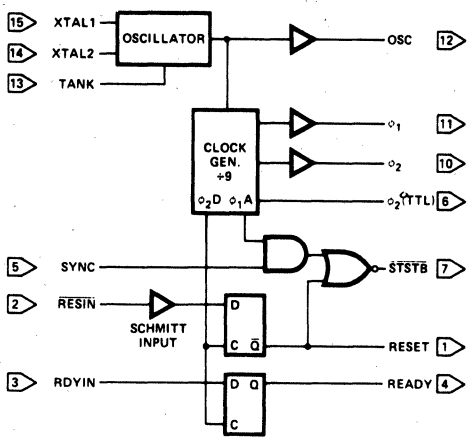
Z32-3

PIN	CONNECTION
1	GND
3	MEMORY CLOCK
5	Ø1 TTL
7	Vcc (+5VDC)
12	Ø2 NMOS
13	Ø1 NMOS
18	GND
20	HOLD 1
22	MEMORY READY
24	2xfc

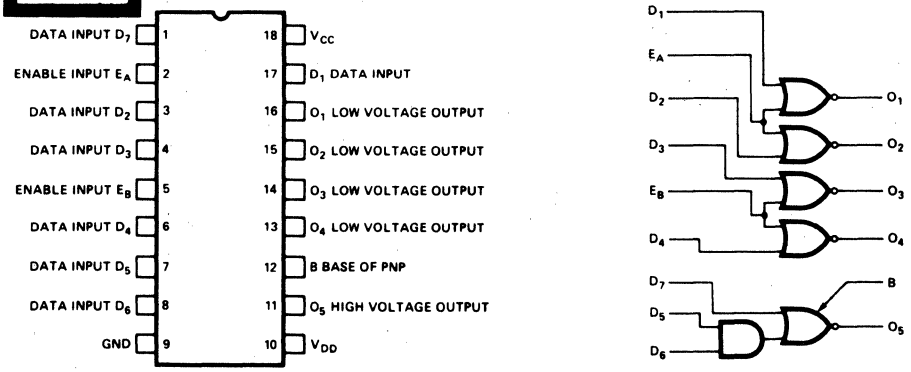
Z32-3a

PIN	CONNECTION
1	GND
3	Ø1 TTL UNGATED
5	Ø2 TTL
7	Vcc (+5VDC)
12	Ø2 NMOS
13	Ø1 NMOS
18	GND
20	HOLD 1
22	HOLD 2
24	2xfc

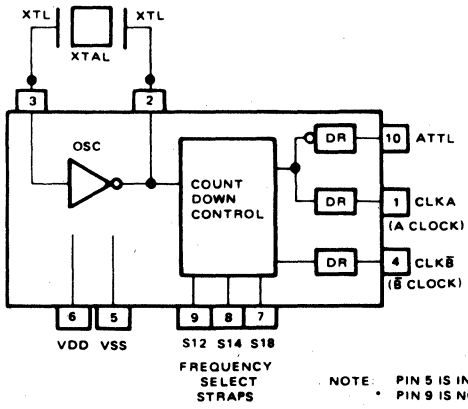
Z32-4



Z32-5

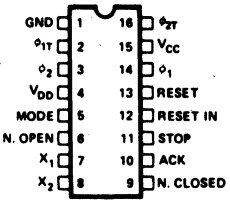


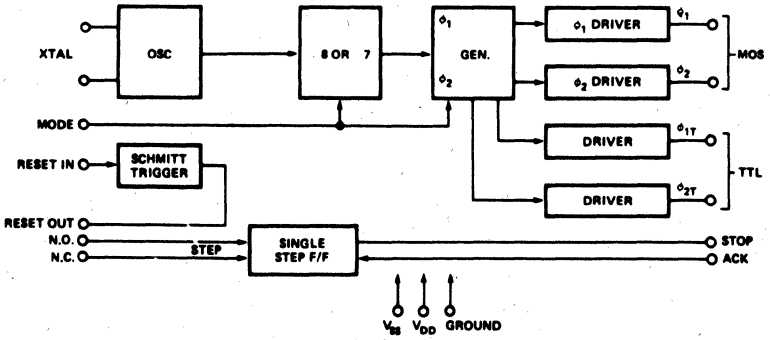
Z32-6



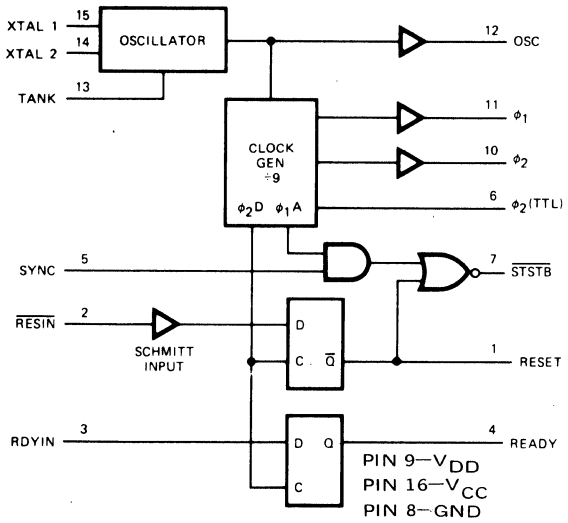
NOTE: PIN 5 IS INTERNALLY TIED TO THE CASE
* PIN 9 IS NOT USED IN PPS-4 APPLICATIONS

Z32-7

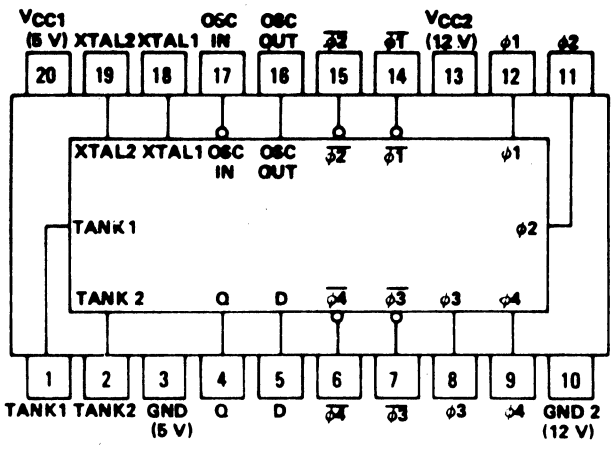




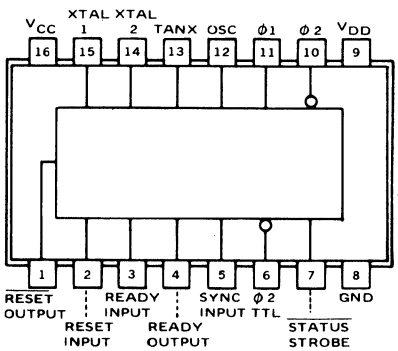
Z32-8



Z32-9



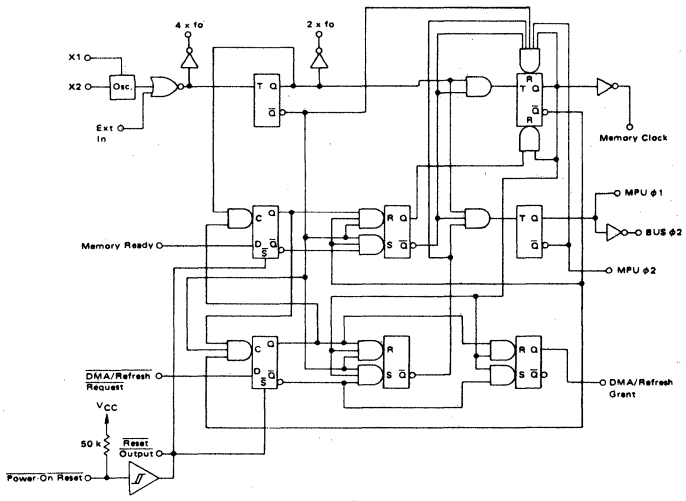
Z32-10

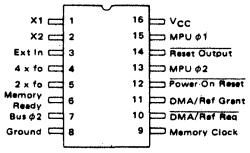


19. LOGIC/BLOCK DRAWINGS

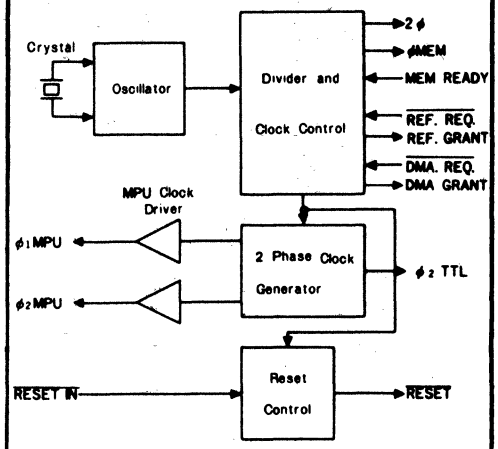
IN DRAWING NUMBER SEQUENCE

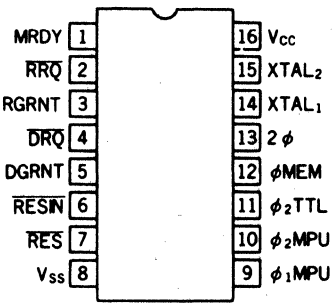
Z32-11





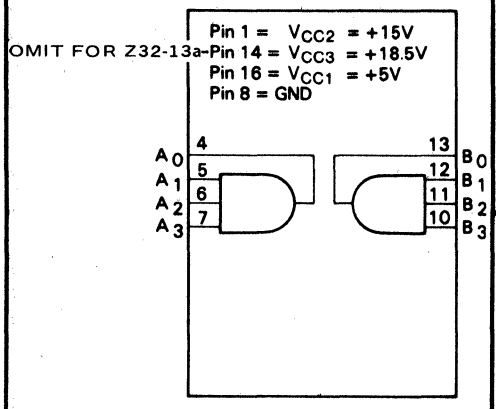
Z32-12



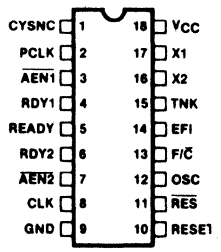


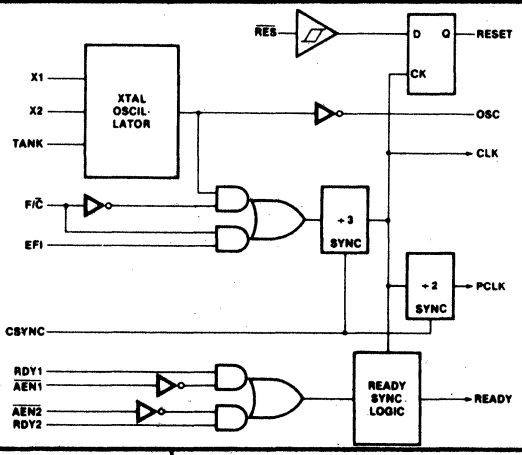
Z32-13

OMIT FOR Z32-13a



Z32-14

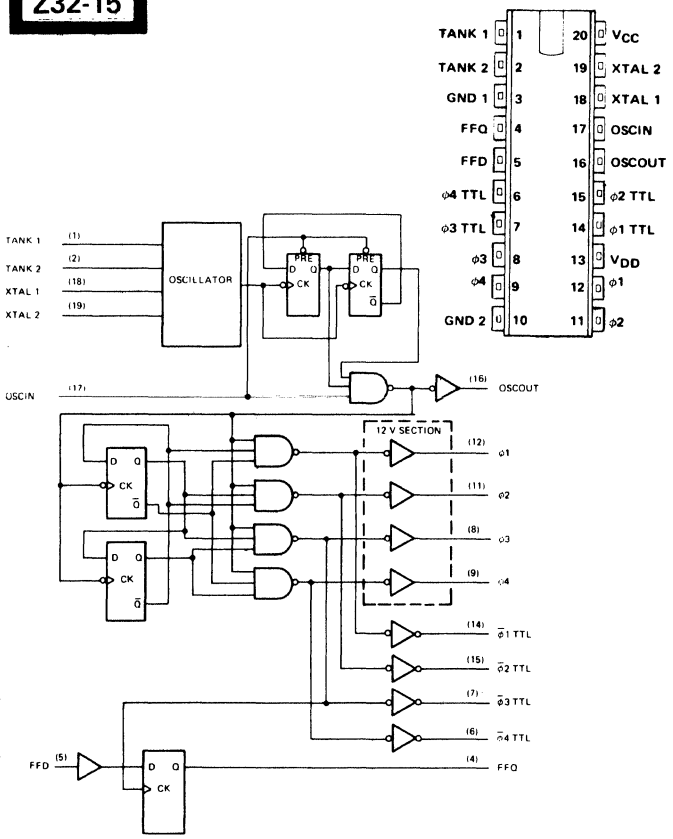




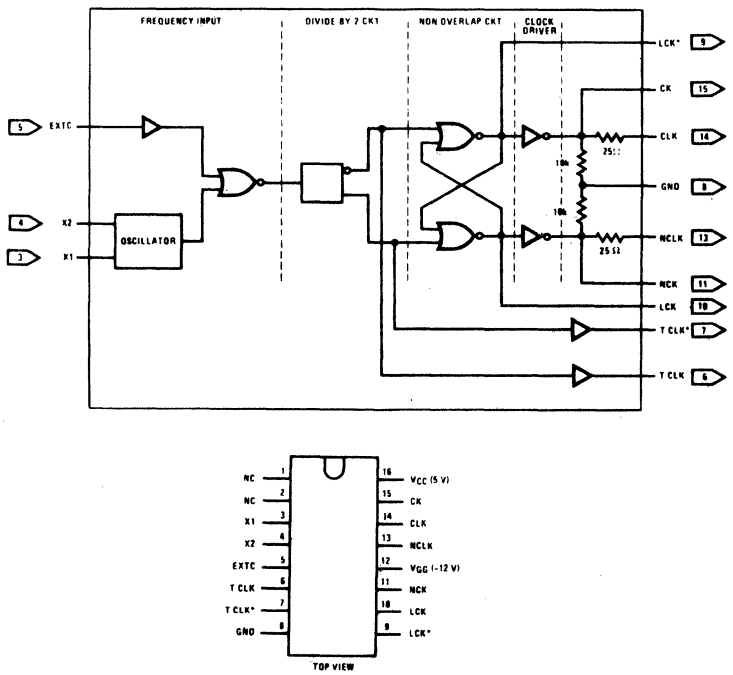
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

Z32-15



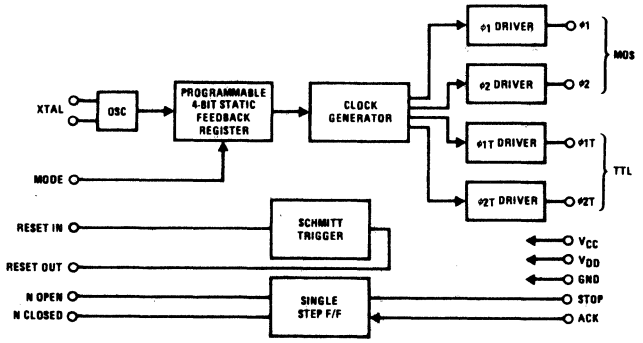
Z32-16

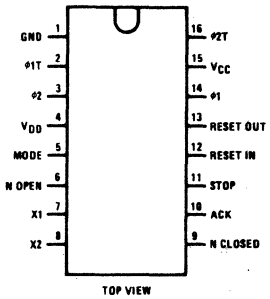


Signal* ≡ N Signal ≡
Low Active Signal

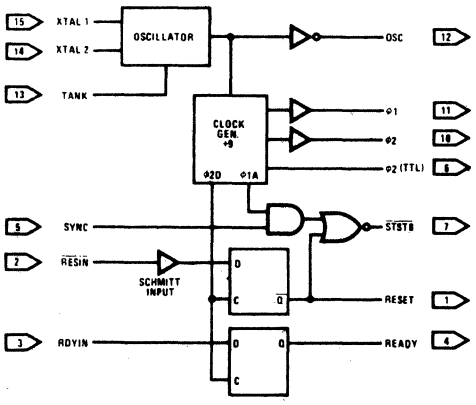
NC = No Connection

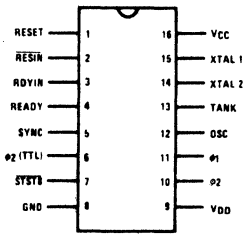
Z32-17



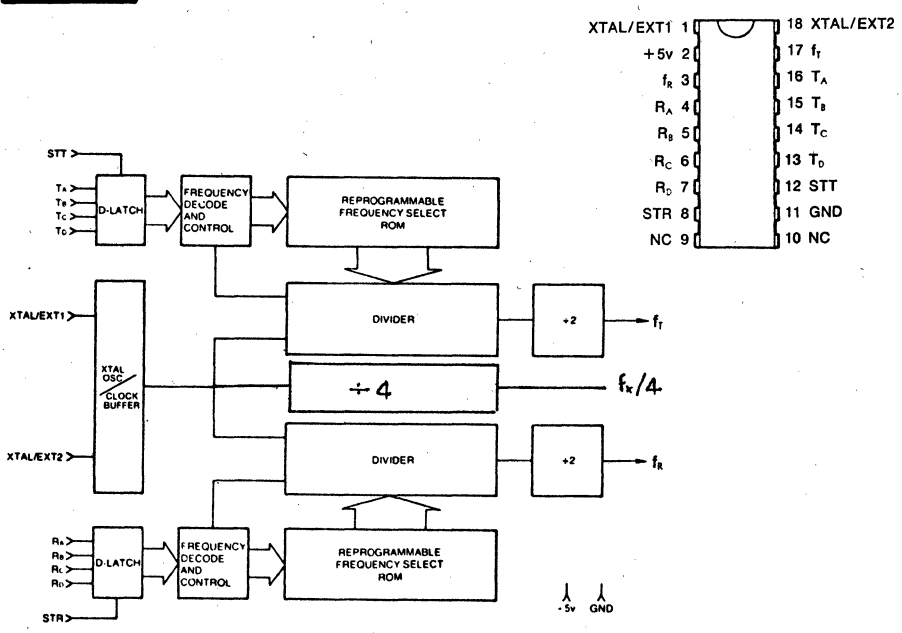


Z32-18

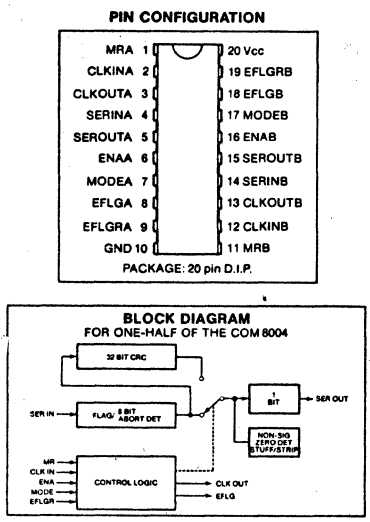




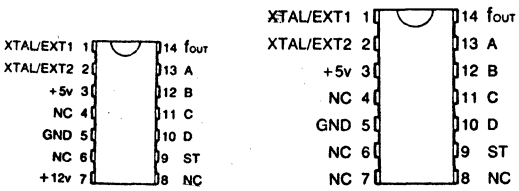
Z32-20

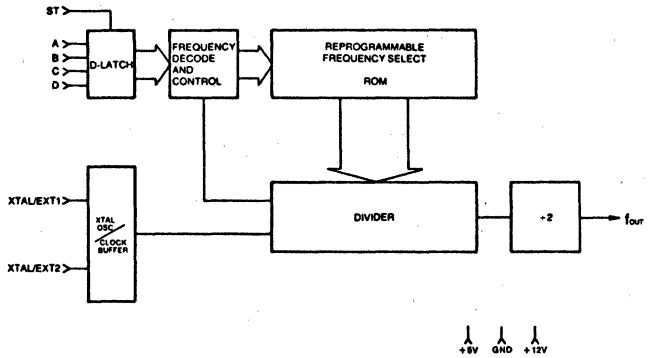


Z32-22

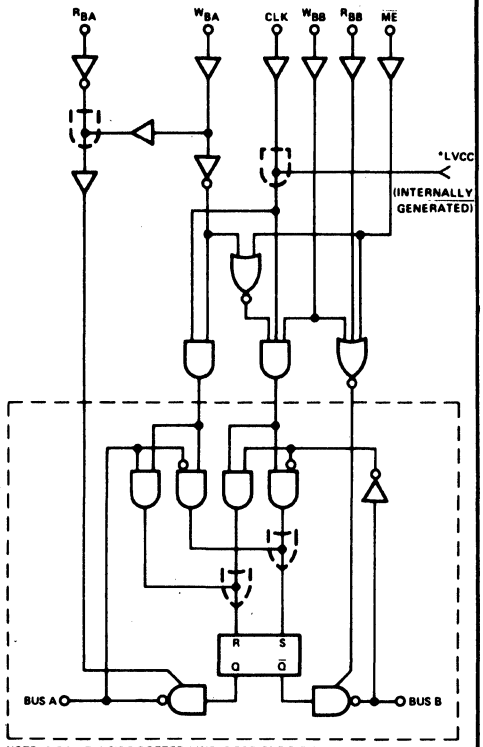


Z32-21

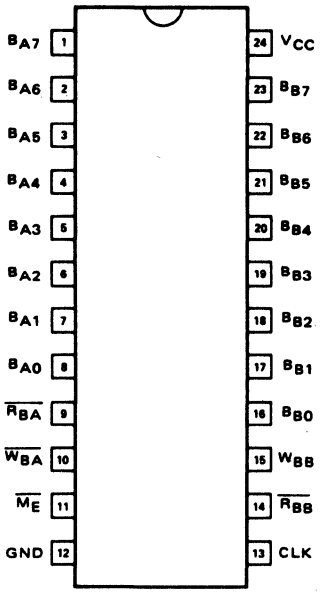




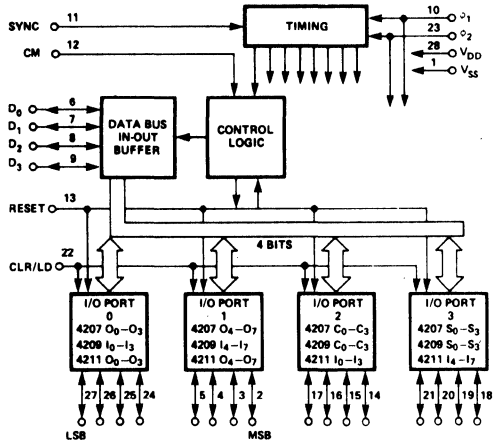
Z33-1

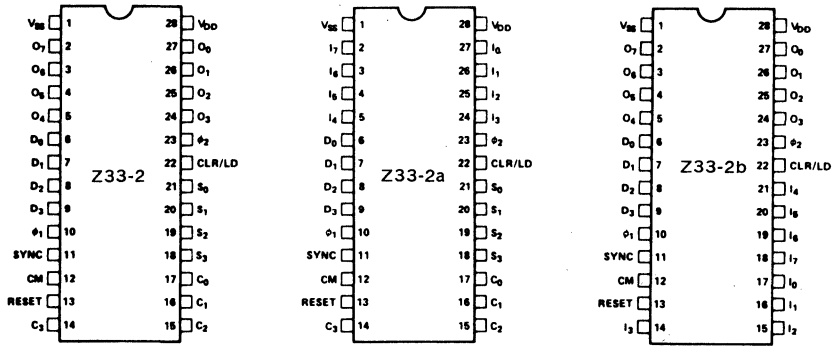


NOTE: CIRCUIT INSIDE DOTTED LINE IS FOR ONE BIT ONLY.
*LOW VOLTAGE CONTROL CIRCUIT

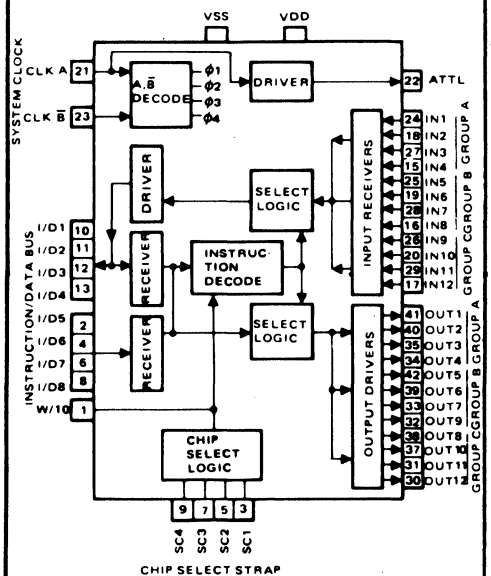


Z33-2

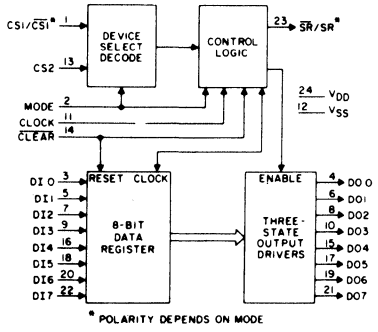




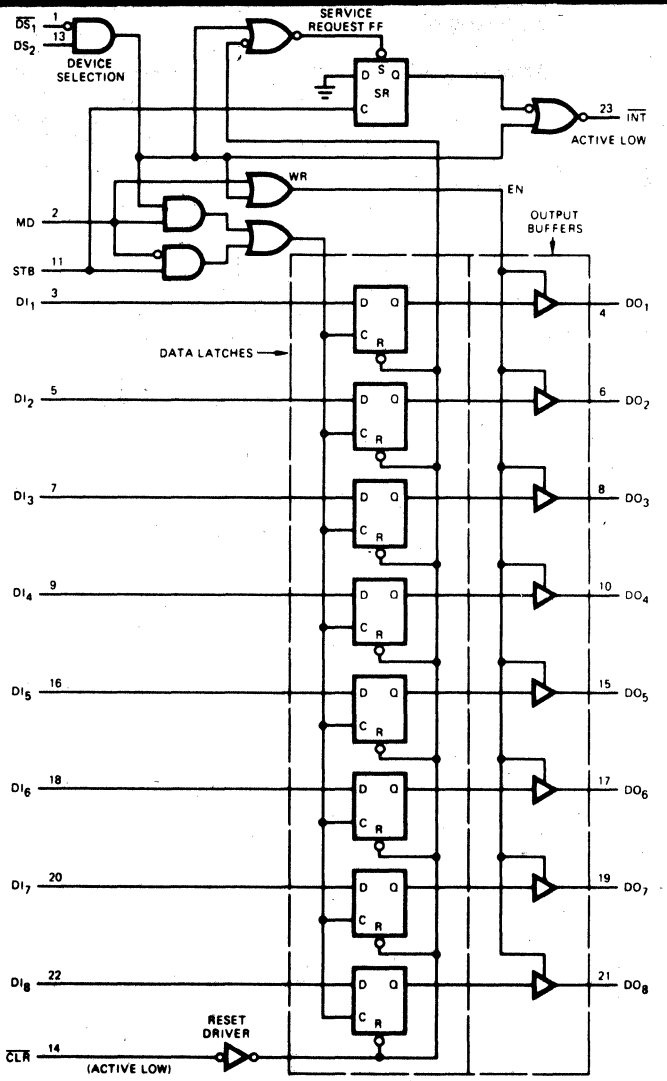
Z33-3



Z33-5

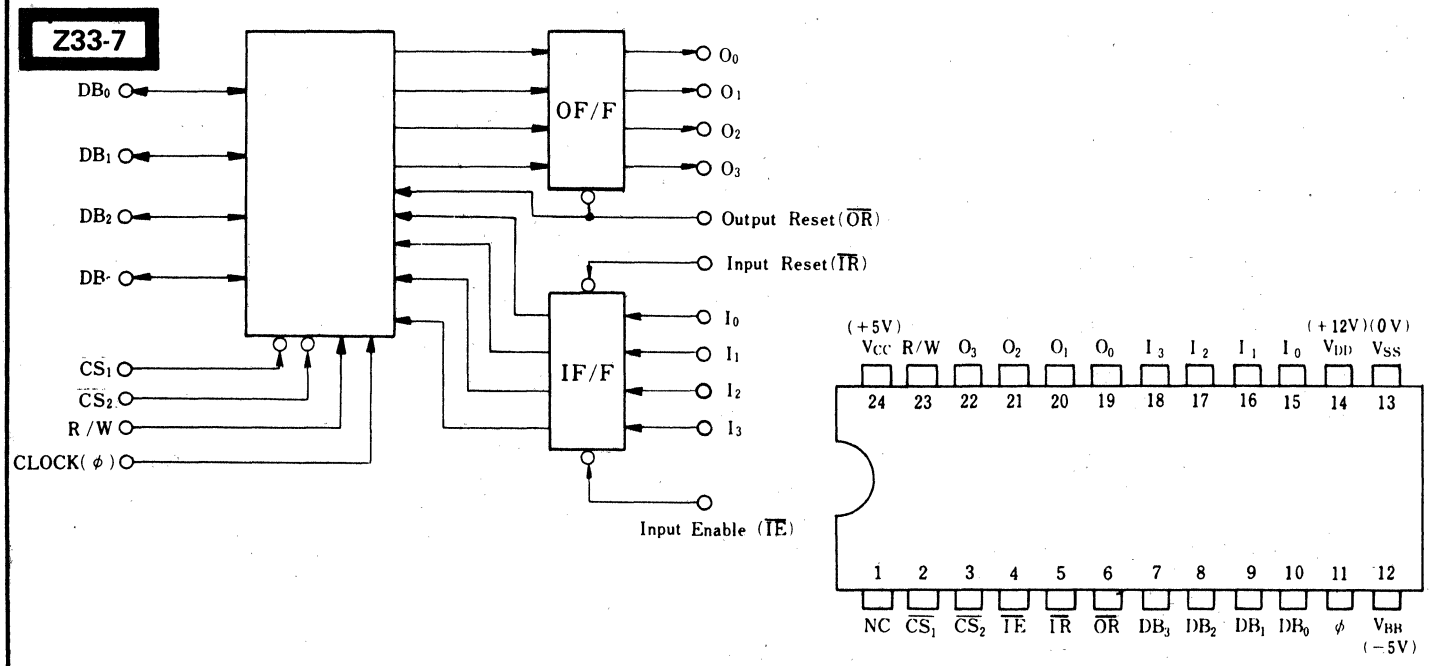


Z33-6

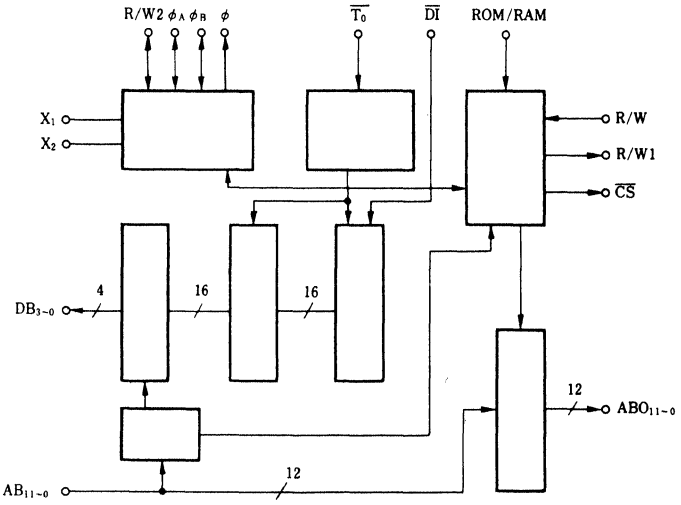


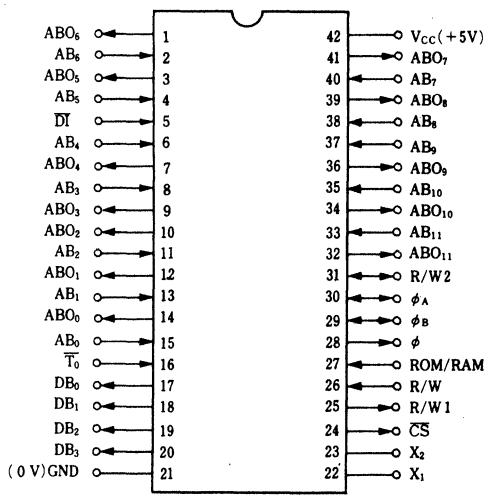
PIN 12—GND
PIN 24—V_{CC}

Z33-7

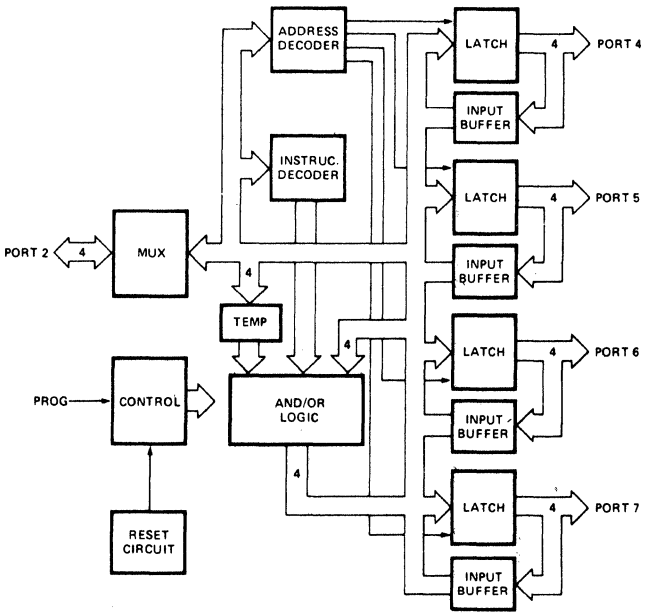


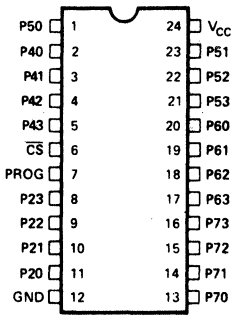
Z33-8


R/W2 ϕ_A ϕ_B ϕ
$\overline{T_0}$
$\overline{DI}$
ROM/RAM
X_1
X_2
R/W
R/W1
$\overline{CS}$
$DB_{3\sim0}$
4
16
16
12
$ABO_{11\sim0}$
$AB_{11\sim0}$
12

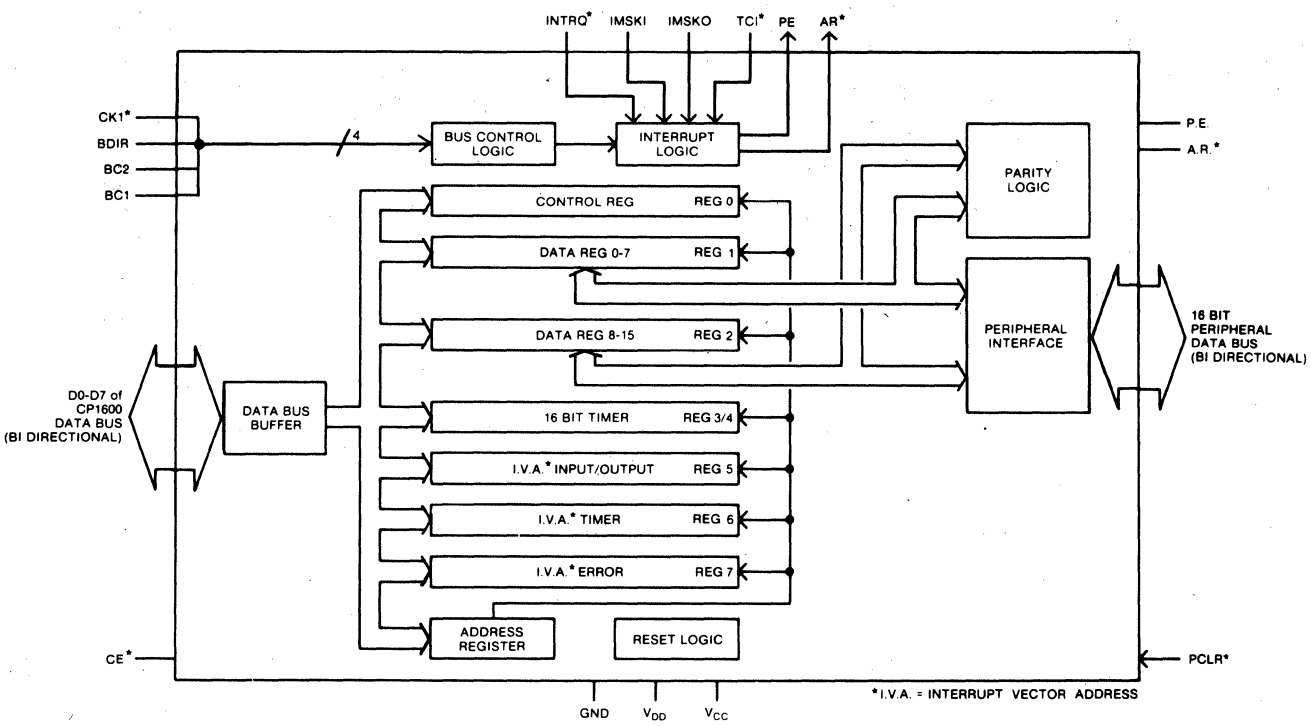

ABO_6 1
AB_6 2
ABO_5 3
AB_5 4
$\overline{DI}$ 5
AB_4 6
ABO_4 7
AB_3 8
ABO_3 9
ABO_2 10
AB_2 11
ABO_1 12
AB_1 13
ABO_0 14
AB_0 15
$\overline{T_0}$ 16
DB_0 17
DB_1 18
DB_2 19
DB_3 20
(0 V)GND 21
42 V_{CC}(+5V)
41 ABO_7
40 AB_7
39 ABO_8
38 AB_8
37 AB_9
36 ABO_9
35 AB_{10}
34 ABO_{10}
33 AB_{11}
32 ABO_{11}
31 R/W2
30 ϕ_A
29 ϕ_B
28 ϕ
27 ROM/RAM
26 R/W
25 R/W1
24 $\overline{CS}$
23 X_2
22 X_1

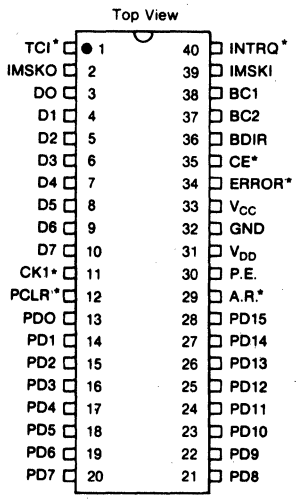
Z33-9


ADDRESS DECODER
INSTRUC. DECODER
MUX
PORT 2
4
TEMP
CONTROL
PROG
AND/OR LOGIC
RESET CIRCUIT
LATCH
INPUT BUFFER
PORT 4
PORT 5
PORT 6
PORT 7


P50 1
P40 2
P41 3
P42 4
P43 5
$\overline{CS}$ 6
PROG 7
P23 8
P22 9
P21 10
P20 11
GND 12
24 V_{CC}
23 P51
22 P52
21 P53
20 P60
19 P61
18 P62
17 P63
16 P73
15 P72
14 P71
13 P70

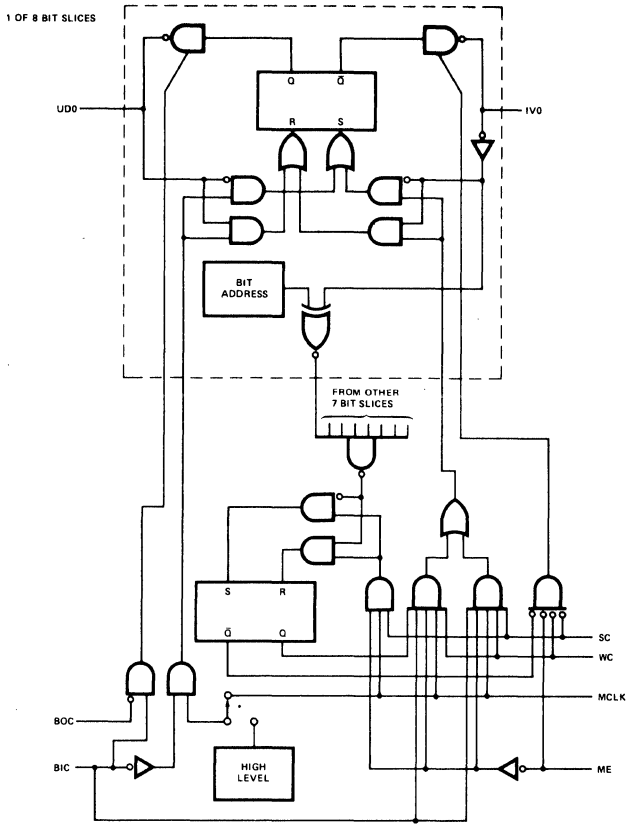
Z33-10

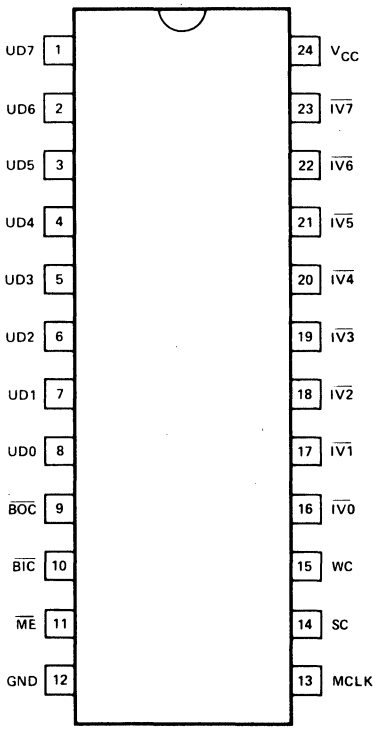




*ACTIVE LOW LEVEL

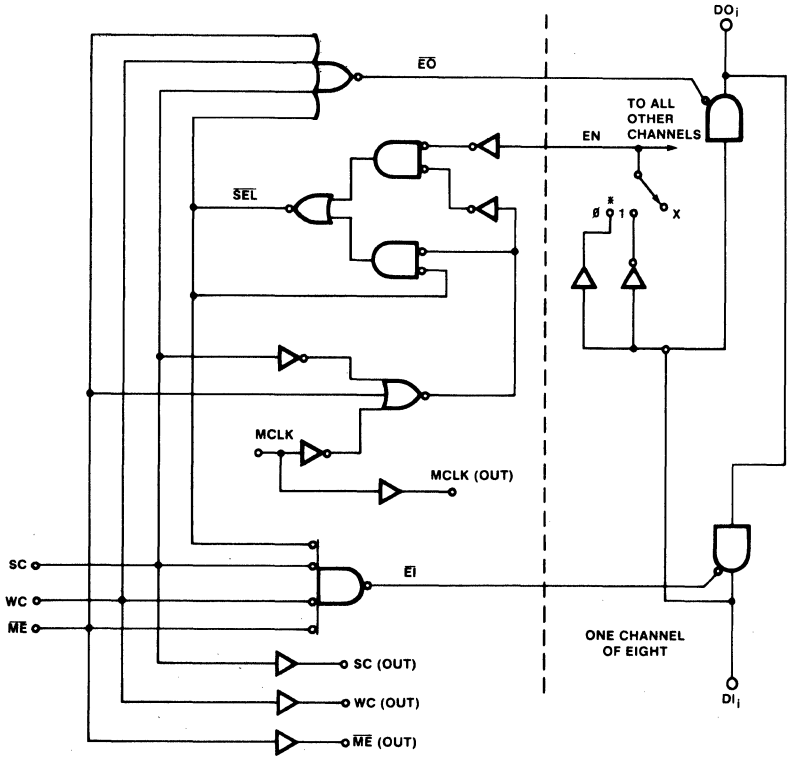
Z33-11

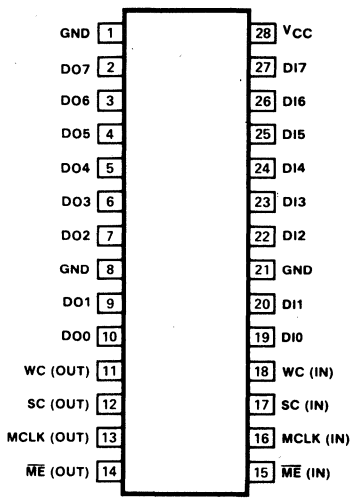




*Switch indicates synchronous/asynchronous user write option. Switch shown for synchronous version.

Z33-12





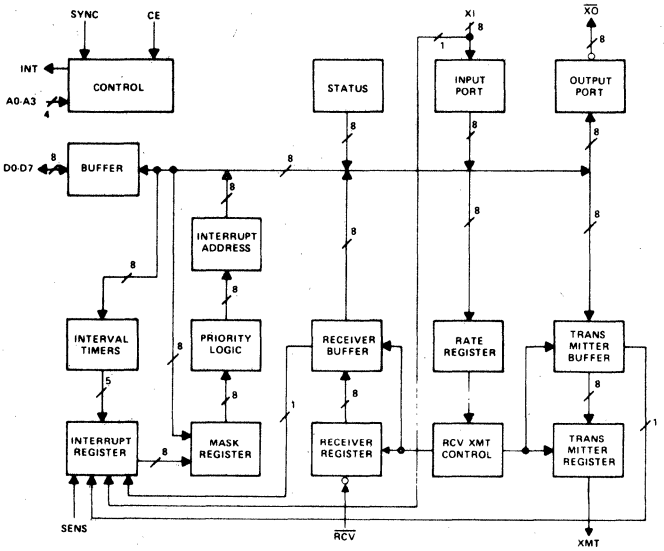
I/O Port Side 8X300 Side

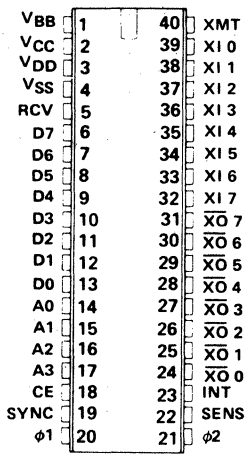
NOTES

*Selection made during manufacture

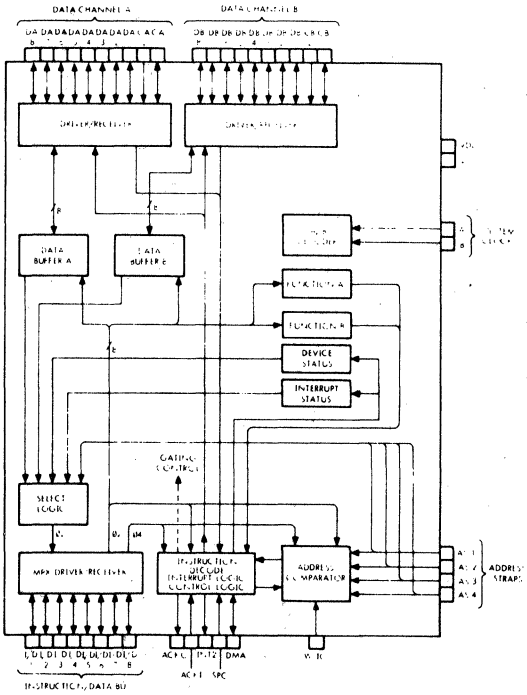
X = Don't care

Z33-13

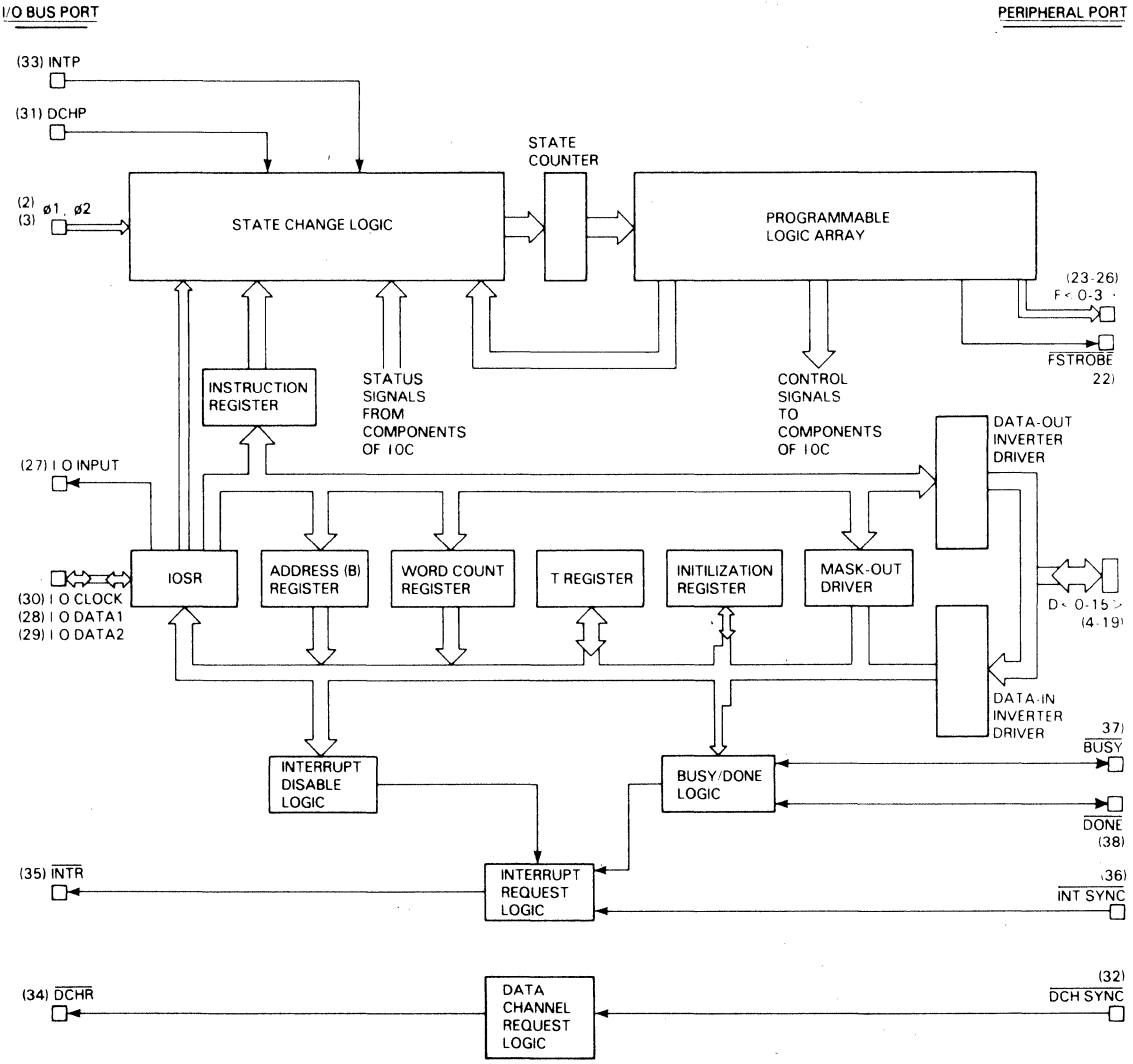

SYNC
CE
INT
A0-A3
CONTROL
STATUS
XI
INPUT PORT
XO
OUTPUT PORT
D0-D7
BUFFER
INTERRUPT ADDRESS
INTERVAL TIMERS
PRIORITY LOGIC
RECEIVER BUFFER
RATE REGISTER
TRANS MITTER BUFFER
INTERRUPT REGISTER
MASK REGISTER
RECEIVER REGISTER
RCV XMT CONTROL
TRANS MITTER REGISTER
SENS
RCV
XMT

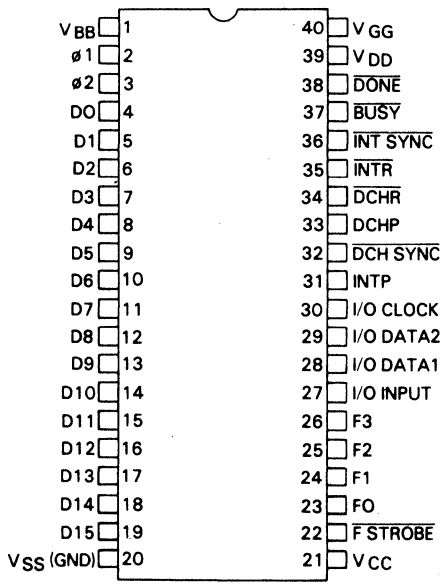

VBB 1
VCC 2
VDD 3
VSS 4
RCV 5
D7 6
D6 7
D5 8
D4 9
D3 10
D2 11
D1 12
D0 13
A0 14
A1 15
A2 16
A3 17
CE 18
SYNC 19
φ1 20
40 XMT
39 XI 0
38 XI 1
37 XI 2
36 XI 3
35 XI 4
34 XI 5
33 XI 6
32 XI 7
31 XO 7
30 XO 6
29 XO 5
28 XO 4
27 XO 3
26 XO 2
25 XO 1
24 XO 0
23 INT
22 SENS
21 φ2

Z33-14


DATA CHANNEL A
DATA CHANNEL B
DATA BUFFER A
DATA BUFFER B
DEVICE STATUS
INTERRUPT STATUS
SELECT LOGIC
ADDRESS COMPARATOR
DMA

Z33-15

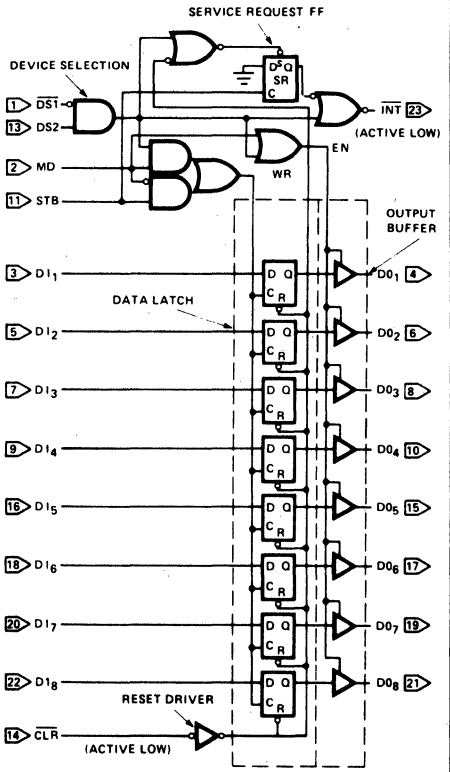

I/O BUS PORT
PERIPHERAL PORT
(33) INTP
(31) DCHP
(2) (3) ø1, ø2
STATE CHANGE LOGIC
STATE COUNTER
PROGRAMMABLE LOGIC ARRAY
(23-26) F<0-3>
FSTROBE (22)
INSTRUCTION REGISTER
STATUS SIGNALS FROM COMPONENTS OF IOC
CONTROL SIGNALS TO COMPONENTS OF IOC
DATA-OUT INVERTER DRIVER
(27) I O INPUT
IOSR
ADDRESS (B) REGISTER
WORD COUNT REGISTER
T REGISTER
INITILIZATION REGISTER
MASK-OUT DRIVER
D<0-15> (4-19)
(30) I O CLOCK
(28) I O DATA1
(29) I O DATA2
DATA-IN INVERTER DRIVER
INTERRUPT DISABLE LOGIC
BUSY/DONE LOGIC
(37) BUSY
DONE (38)
(35) INTR
INTERRUPT REQUEST LOGIC
(36) INT SYNC
(34) DCHR
DATA CHANNEL REQUEST LOGIC
(32) DCH SYNC


VBB 1
ø1 2
ø2 3
DO 4
D1 5
D2 6
D3 7
D4 8
D5 9
D6 10
D7 11
D8 12
D9 13
D10 14
D11 15
D12 16
D13 17
D14 18
D15 19
VSS (GND) 20
40 VGG
39 VDD
38 DONE
37 BUSY
36 INT SYNC
35 INTR
34 DCHR
33 DCHP
32 DCH SYNC
31 INTP
30 I/O CLOCK
29 I/O DATA2
28 I/O DATA1
27 I/O INPUT
26 F3
25 F2
24 F1
23 FO
22 F STROBE
21 VCC

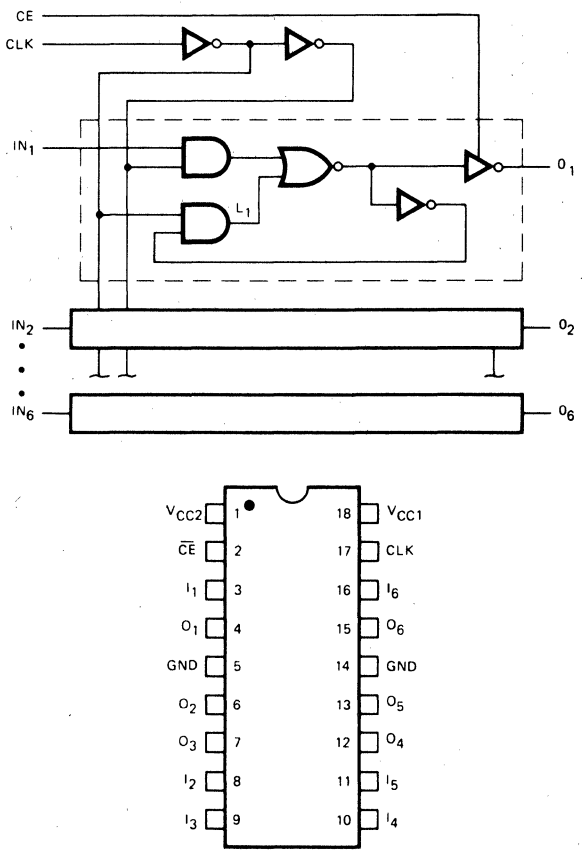
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

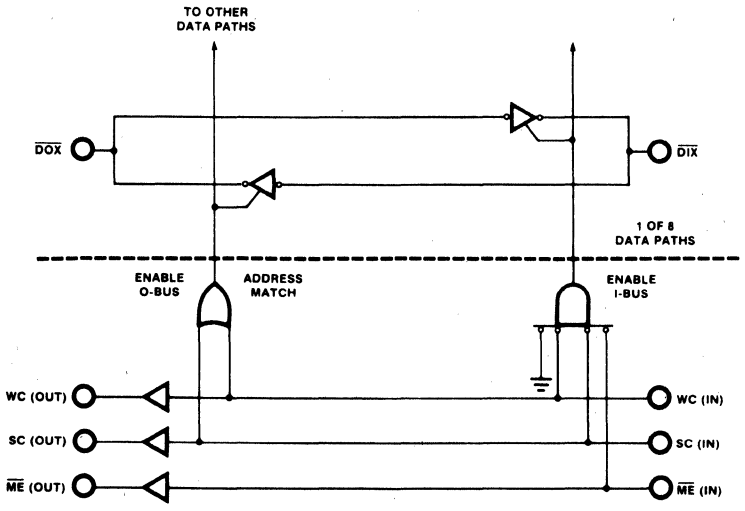
Z33-16

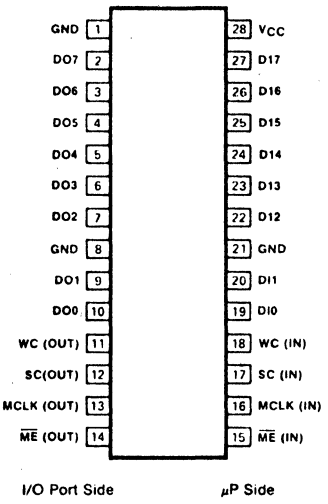


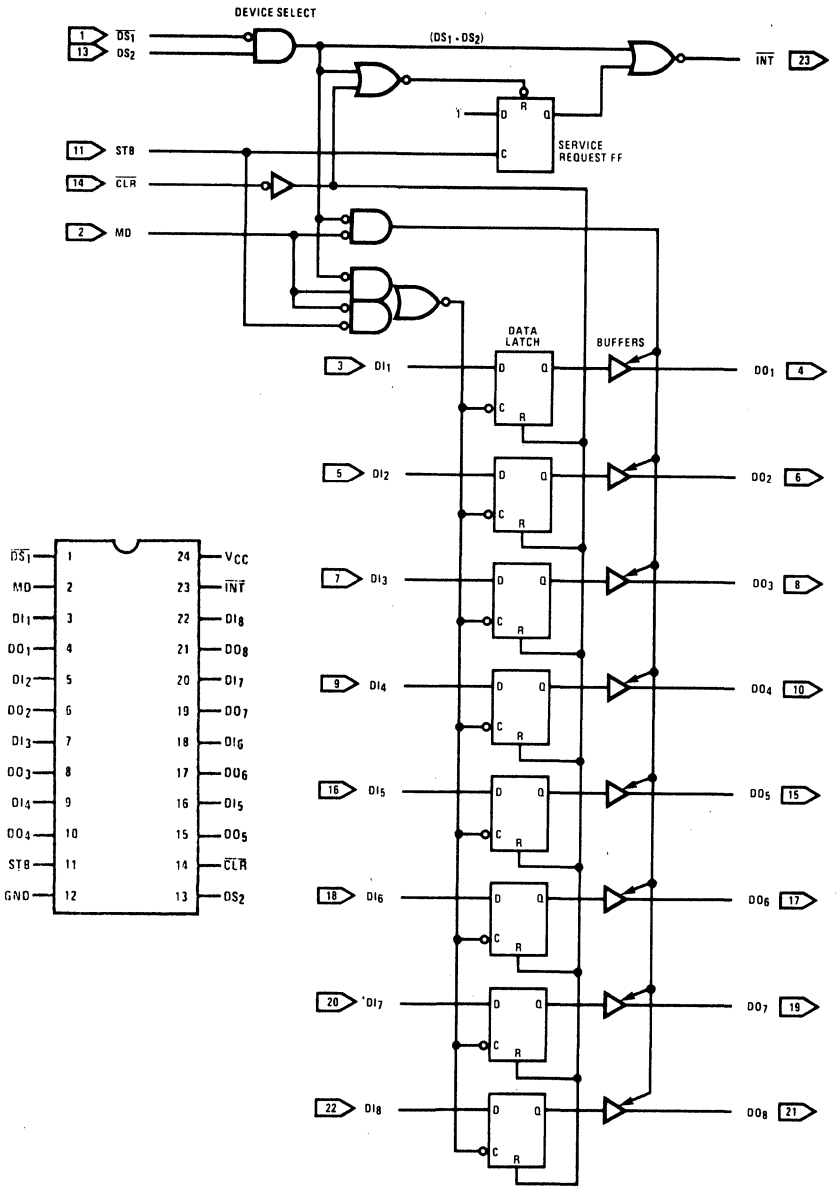
Z33-17



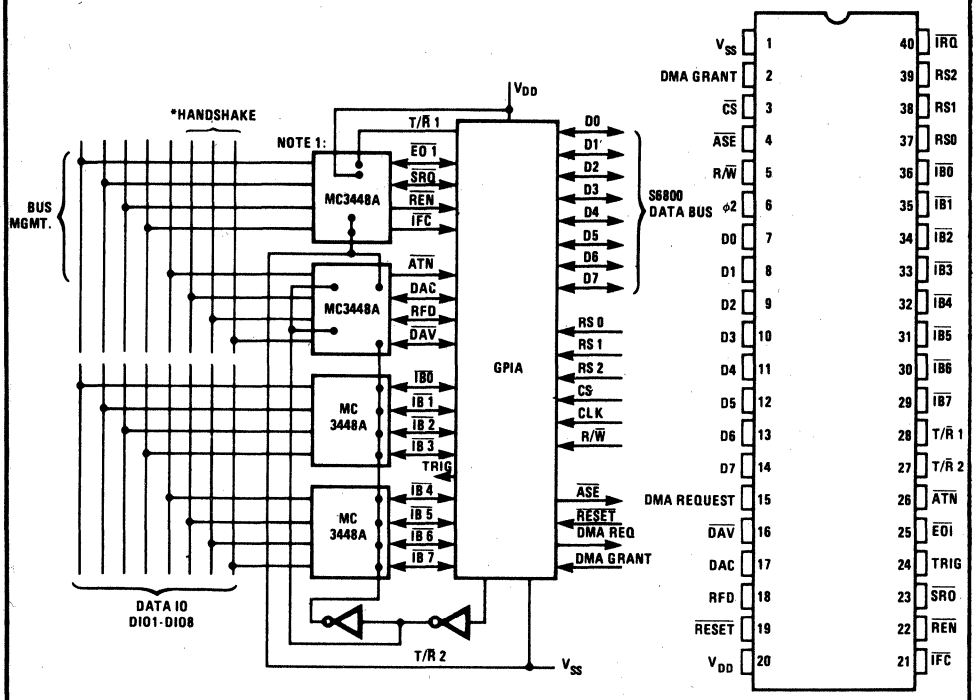
Z33-18



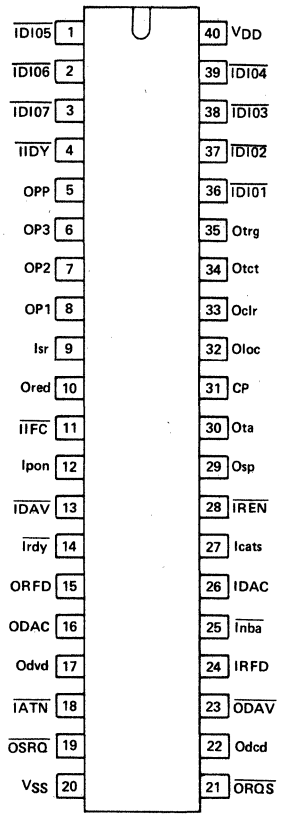



DEVICE SELECT
1 $\overline{DS_1}$
13 DS_2
$(DS_1 \cdot DS_2)$
$\overline{INT}$ 23
SERVICE REQUEST FF
11 STB
14 $\overline{CLR}$
2 MD
DATA LATCH
BUFFERS
3 DI_1
DO_1 4
5 DI_2
DO_2 6
7 DI_3
DO_3 8
9 DI_4
DO_4 10
16 DI_5
DO_5 15
18 DI_6
DO_6 17
20 DI_7
DO_7 19
22 DI_8
DO_8 21
$\overline{DS_1}$ 1
MD 2
DI_1 3
DO_1 4
DI_2 5
DO_2 6
DI_3 7
DO_3 8
DI_4 9
DO_4 10
STB 11
GND 12
24 V_{CC}
23 $\overline{INT}$
22 DI_8
21 DO_8
20 DI_7
19 DO_7
18 DI_6
17 DO_6
16 DI_5
15 DO_5
14 $\overline{CLR}$
13 DS_2

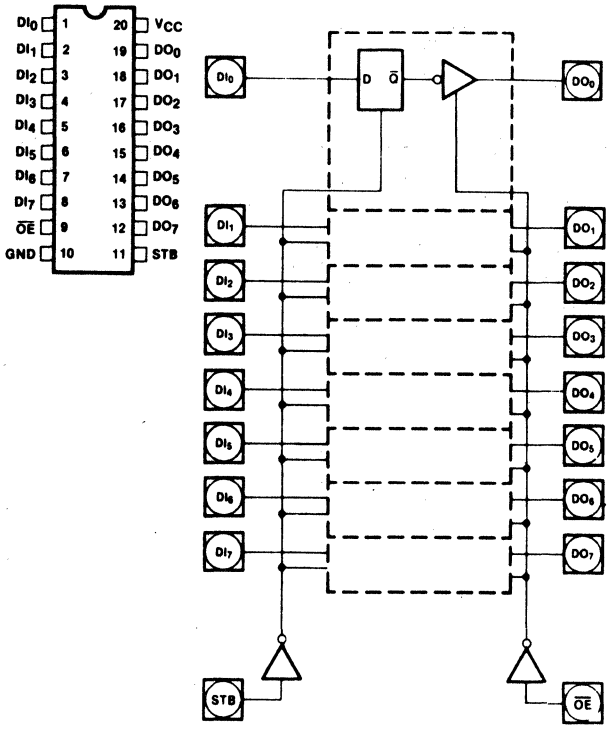
Z33-20



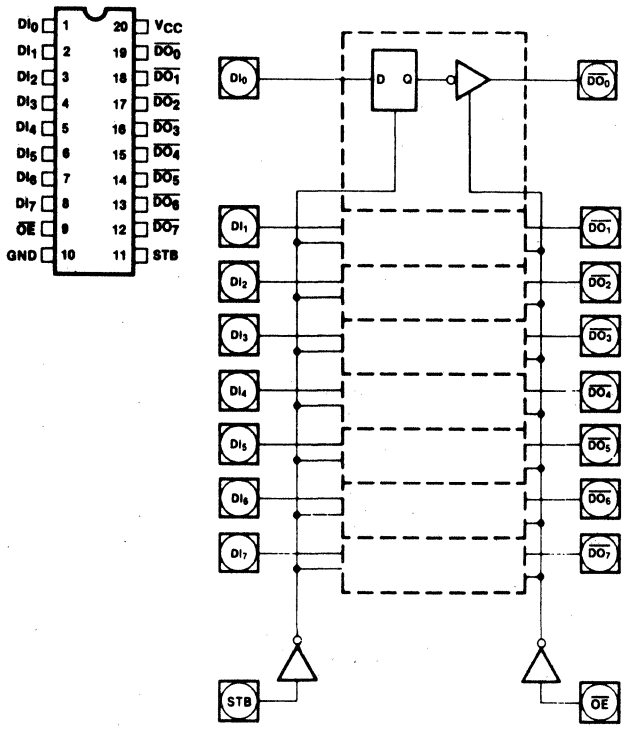
Z33-21



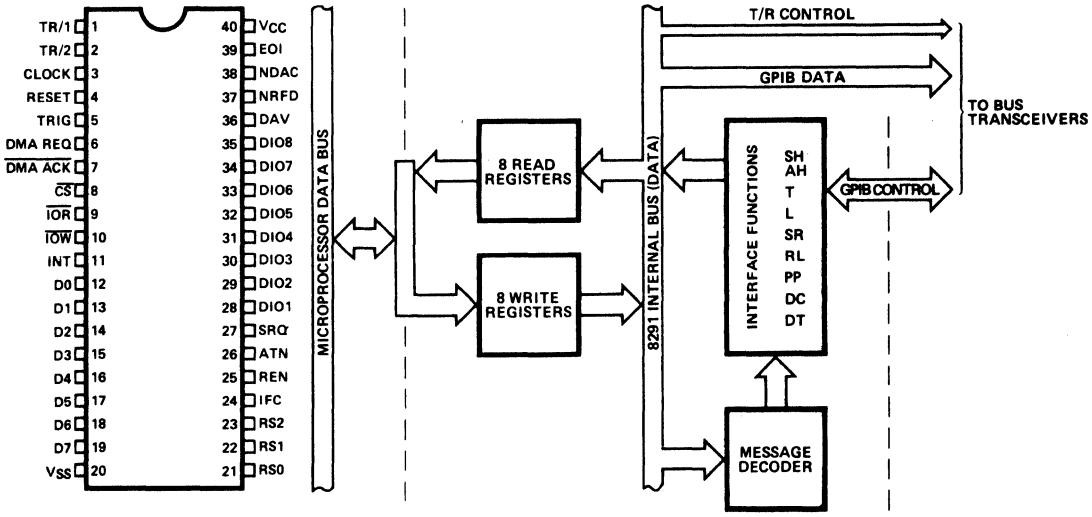
Z33-22



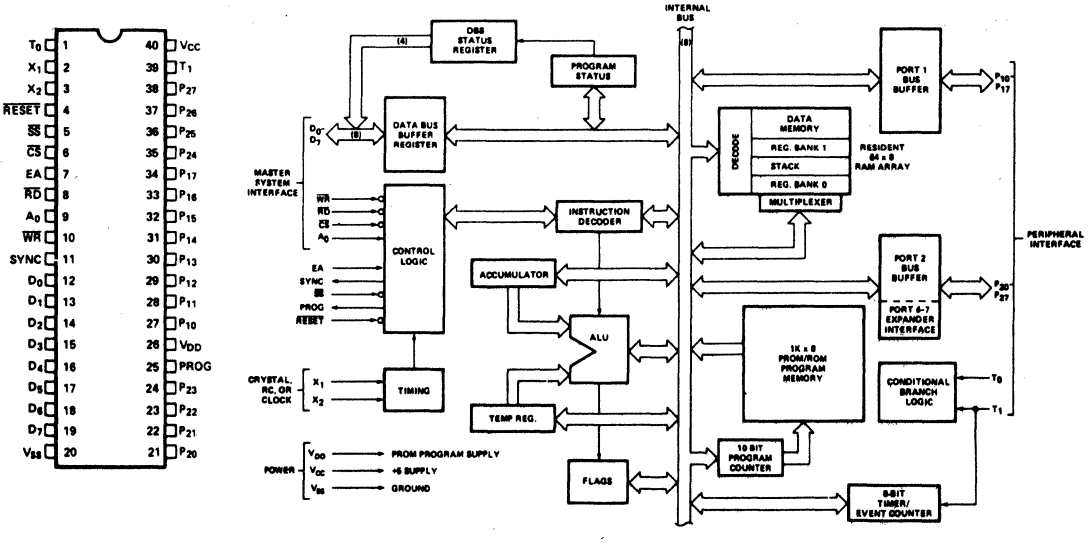
Z33-23



Z33-24


TR/1 1
TR/2 2
CLOCK 3
RESET 4
TRIG 5
DMA REQ 6
DMA ACK 7
CS 8
IOR 9
IOW 10
INT 11
D0 12
D1 13
D2 14
D3 15
D4 16
D5 17
D6 18
D7 19
VSS 20
40 VCC
39 EOI
38 NDAC
37 NRFD
36 DAV
35 DIO8
34 DIO7
33 DIO6
32 DIO5
31 DIO4
30 DIO3
29 DIO2
28 DIO1
27 SRQ
26 ATN
25 REN
24 IFC
23 RS2
22 RS1
21 RS0
MICROPROCESSOR DATA BUS
8 READ REGISTERS
8 WRITE REGISTERS
8291 INTERNAL BUS (DATA)
T/R CONTROL
GPIB DATA
TO BUS TRANSCEIVERS
INTERFACE FUNCTIONS
SH
AH
T
L
SR
RL
PP
DC
DT
GPIB CONTROL
MESSAGE DECODER

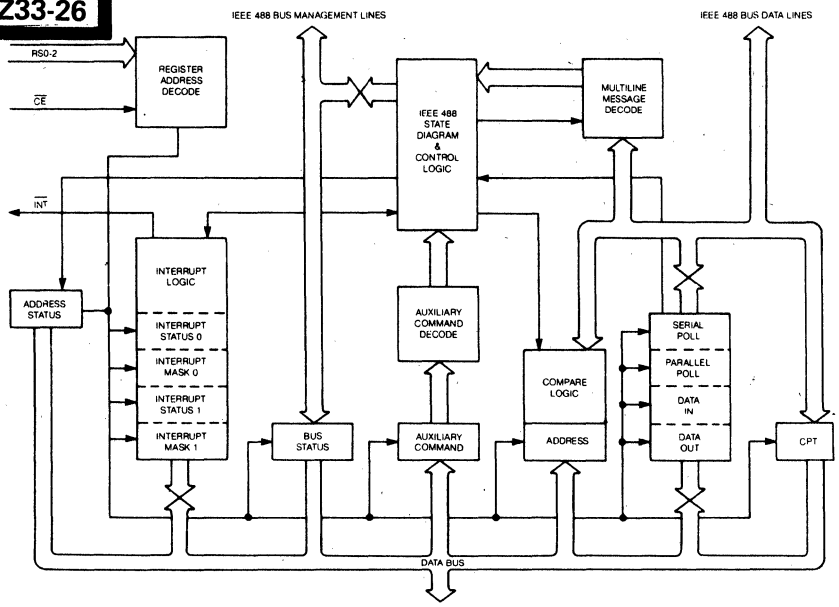
Z33-25


T0 1
X1 2
X2 3
RESET 4
SS 5
CS 6
EA 7
RD 8
A0 9
WR 10
SYNC 11
D0 12
D1 13
D2 14
D3 15
D4 16
D5 17
D6 18
D7 19
VSS 20
40 VCC
39 T1
38 P27
37 P26
36 P25
35 P24
34 P17
33 P16
32 P15
31 P14
30 P13
29 P12
28 P11
27 P10
26 VDD
25 PROG
24 P23
23 P22
21 P21
20 P20
INTERNAL BUS
DBB STATUS REGISTER
PROGRAM STATUS
DATA BUS BUFFER REGISTER
MASTER SYSTEM INTERFACE
CONTROL LOGIC
INSTRUCTION DECODER
ACCUMULATOR
ALU
TEMP REG.
TIMING
CRYSTAL, RC, OR CLOCK
POWER
PROM PROGRAM SUPPLY
+5 SUPPLY
GROUND
FLAGS
DECODE
DATA MEMORY
REG. BANK 1
STACK
REG. BANK 0
MULTIPLEXER
RESIDENT 64 x 8 RAM ARRAY
PORT 1 BUS BUFFER
PORT 2 BUS BUFFER
PORT 6-7 EXPANDER INTERFACE
1K x 8 PROM/ROM PROGRAM MEMORY
CONDITIONAL BRANCH LOGIC
10 BIT PROGRAM COUNTER
8-BIT TIMER/ EVENT COUNTER
PERIPHERAL INTERFACE

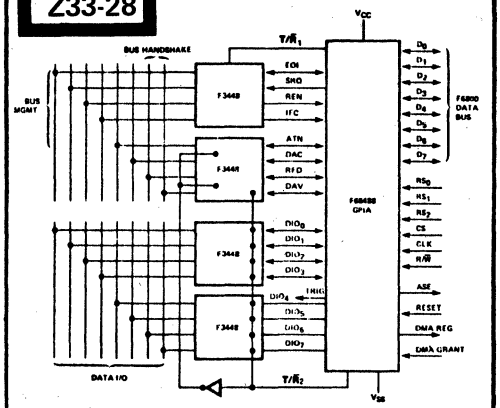
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

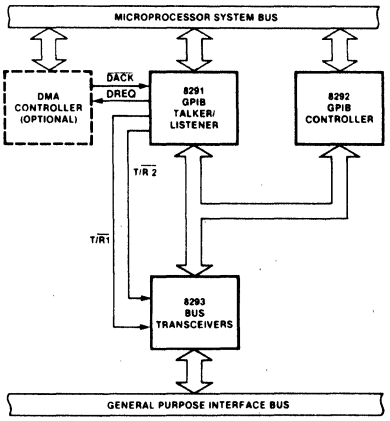
Z33-26



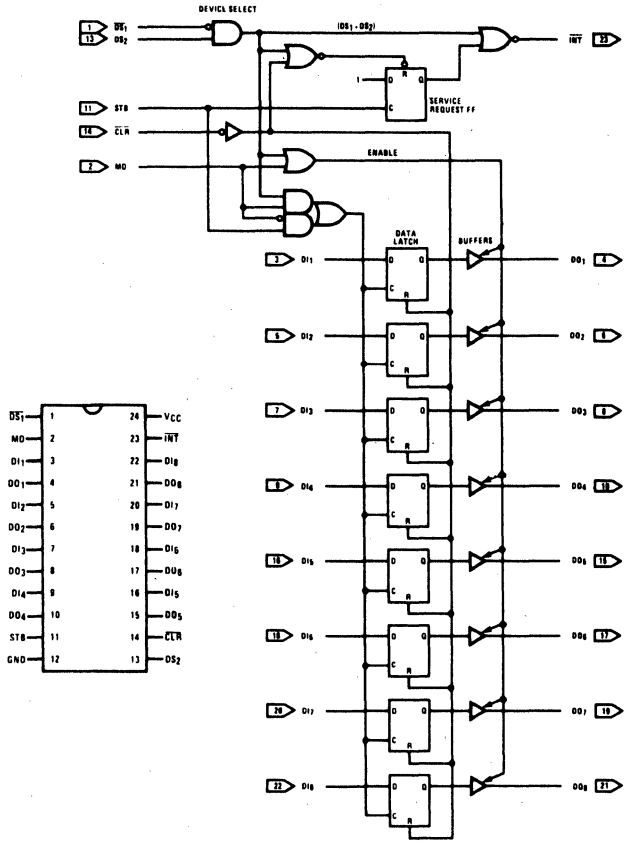
Z33-28

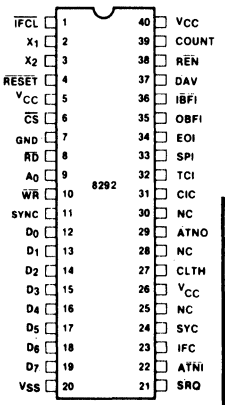


Z33-29

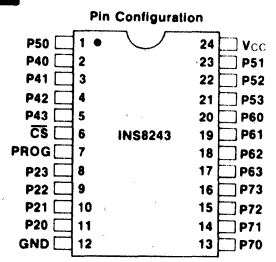


Z33-27

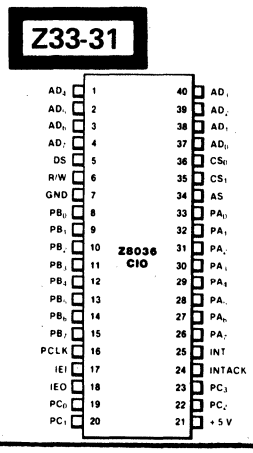


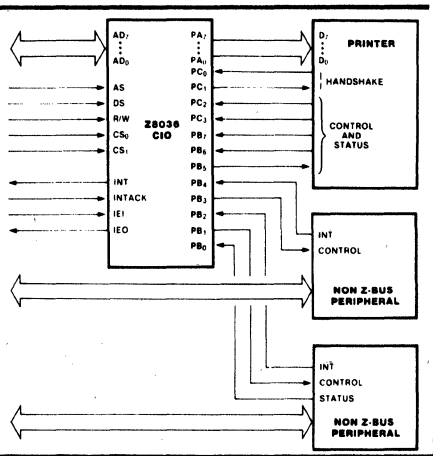


Z33-30



Z33-31

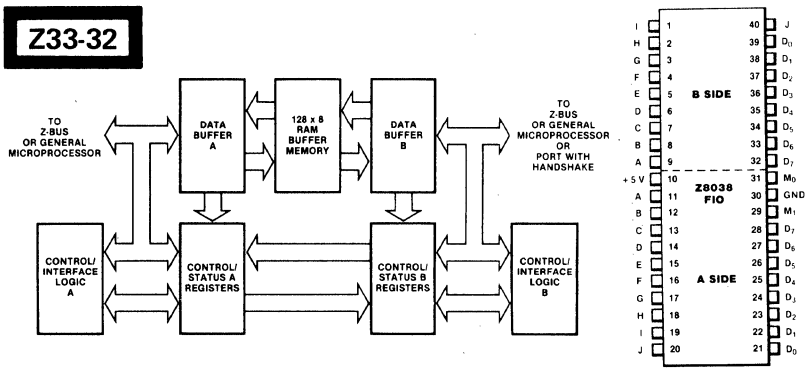




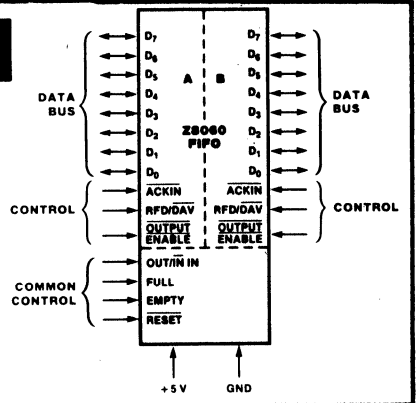
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

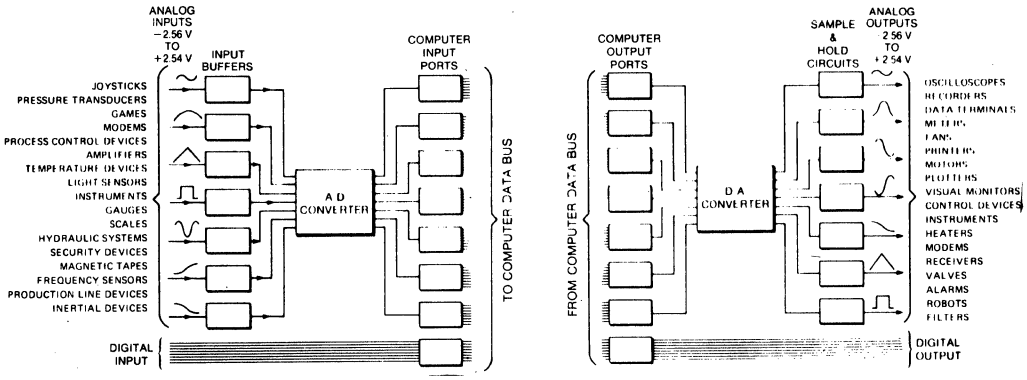
Z33-32



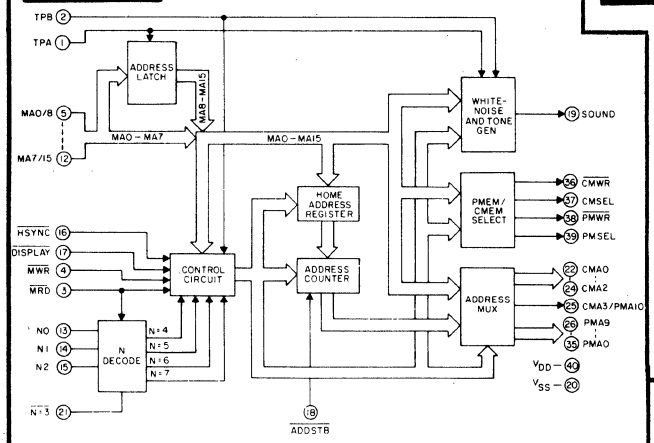
Z33-33



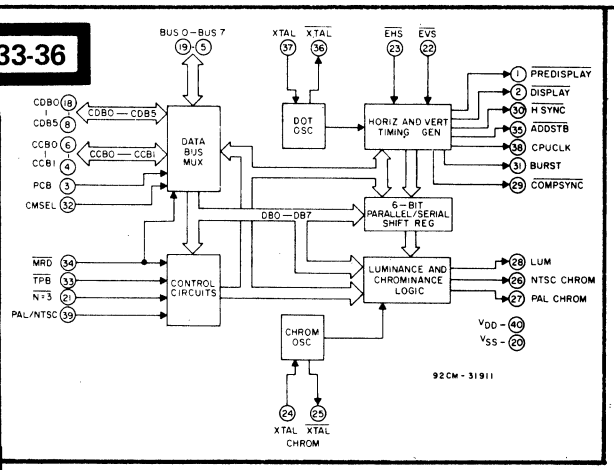
Z33-34

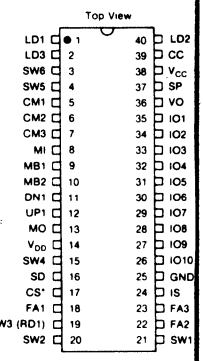


Z33-35

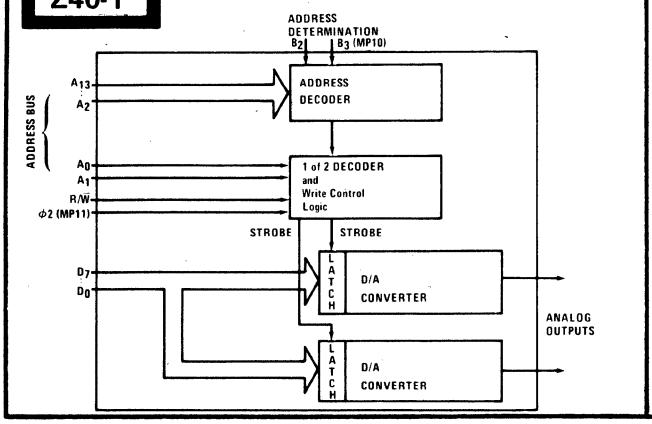


Z33-36

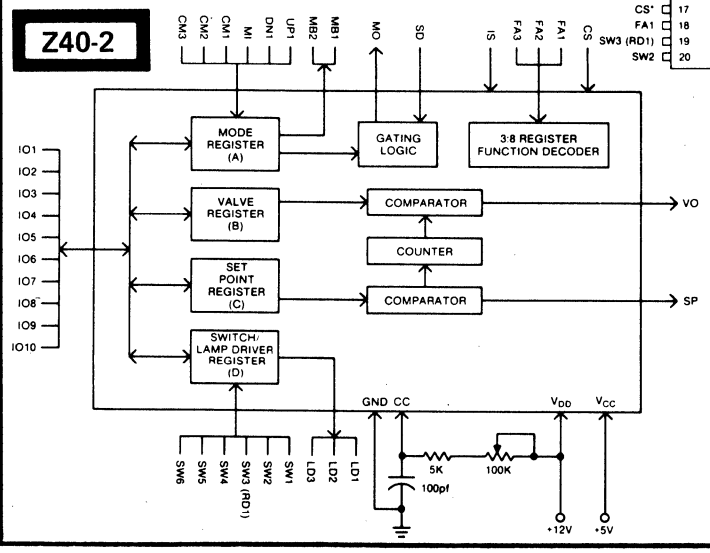




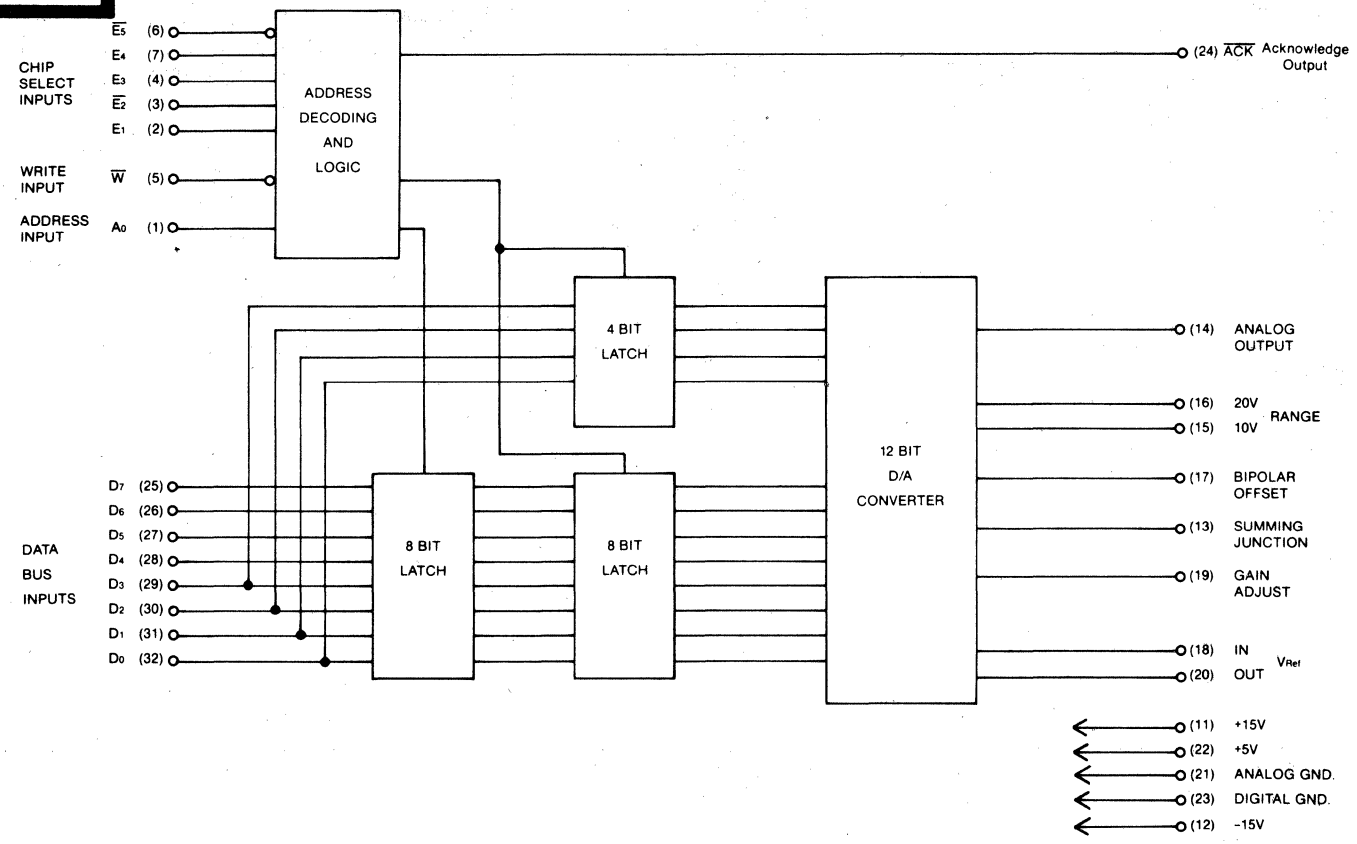
Z40-1



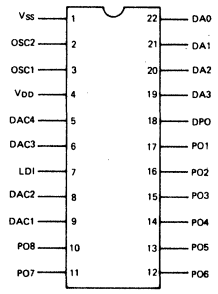
Z40-2

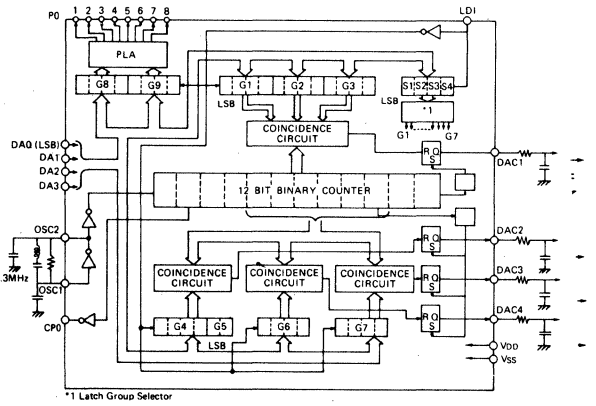


Z40-3

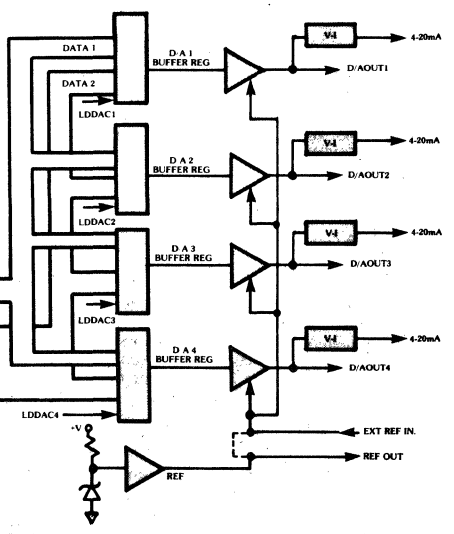


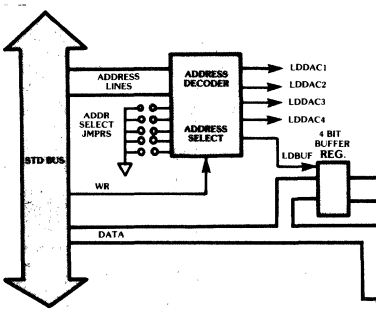
Z40-4



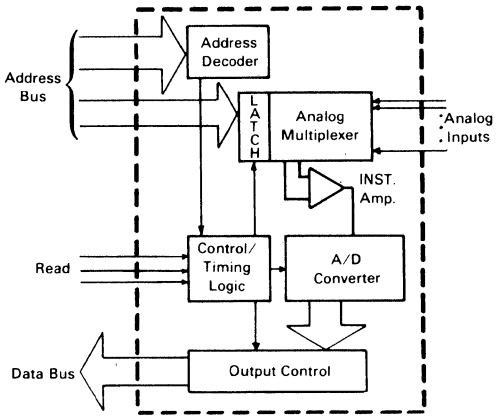


Z40-5

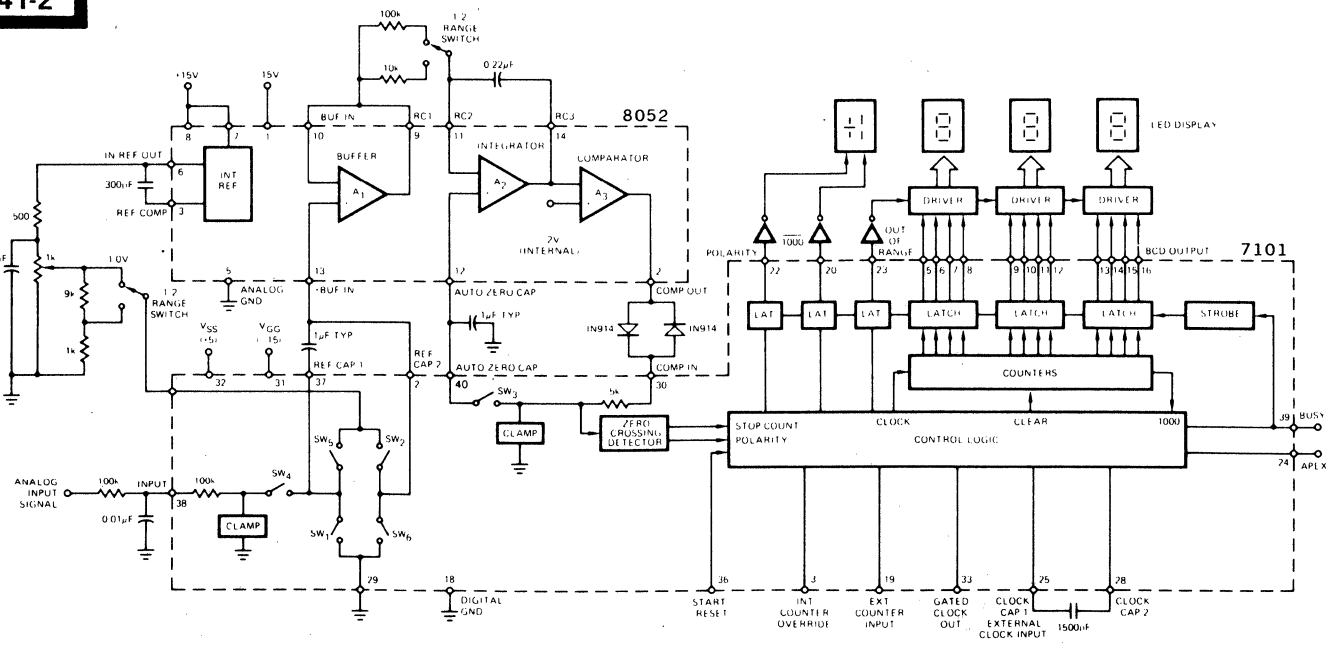




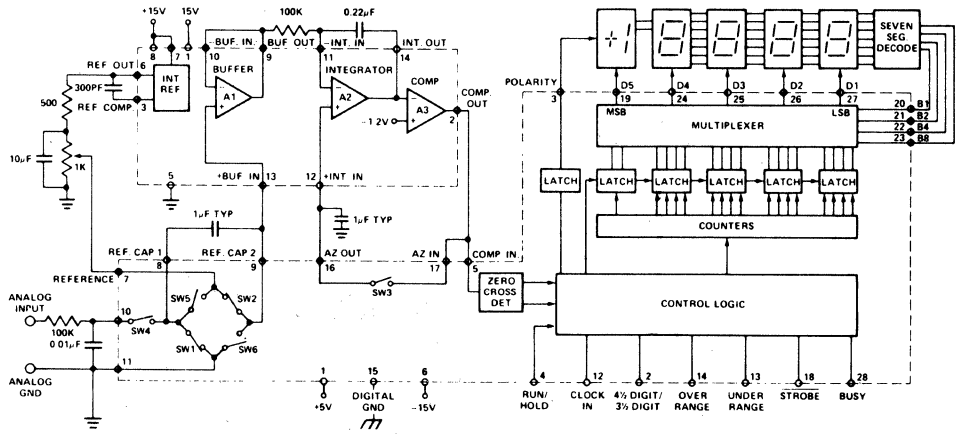
Z41-1



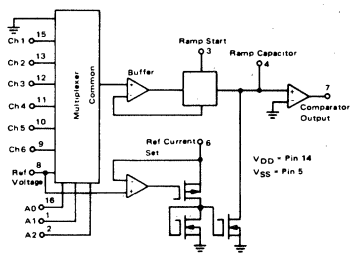
Z41-2



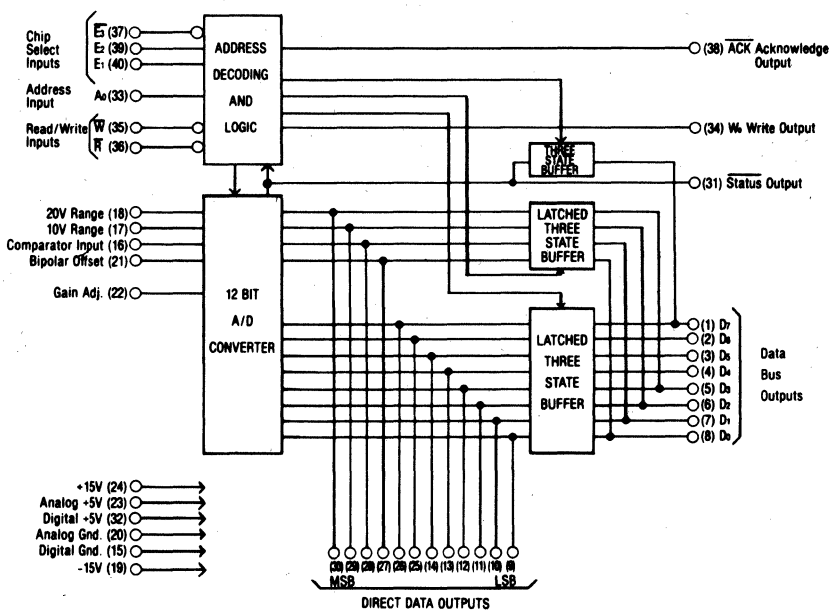
Z41-3



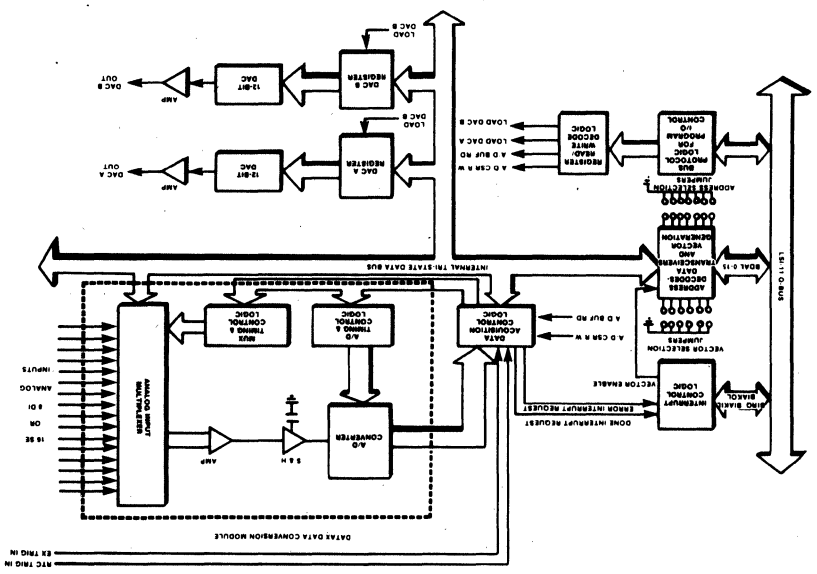
Z41-4



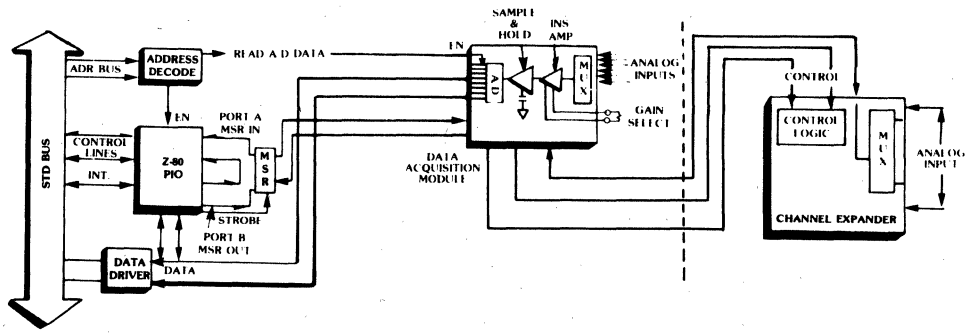
Z41-5



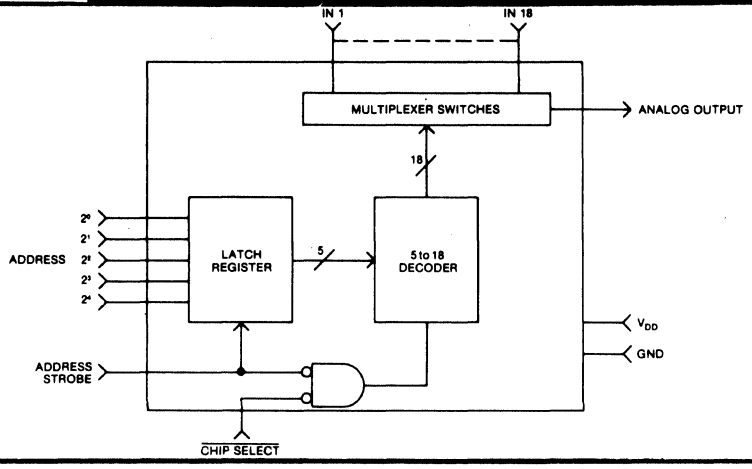
Z41-6

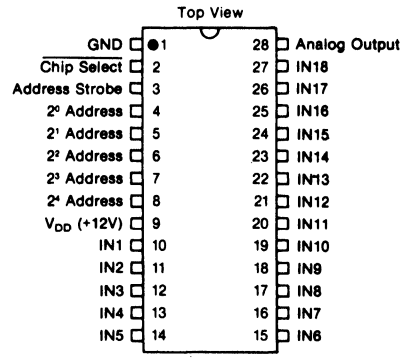


Z41-7

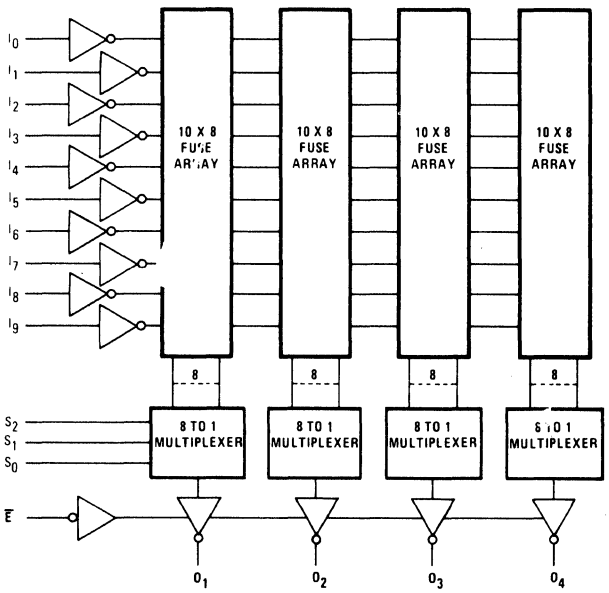


Z43-2

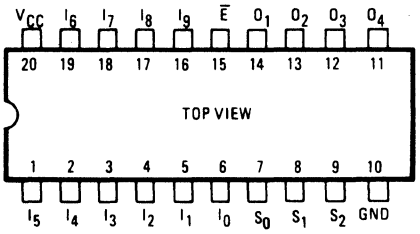




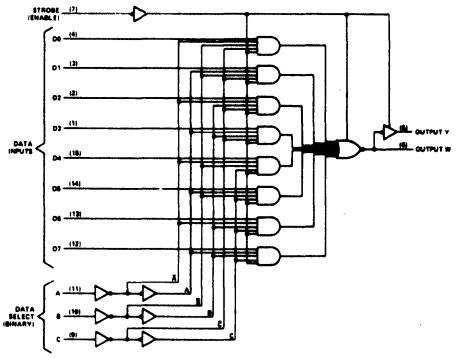
Z43-3

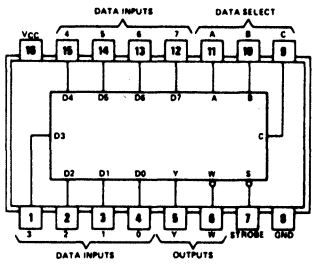


NOTE: PIN 1 IS MARKED FOR ORIENTATION

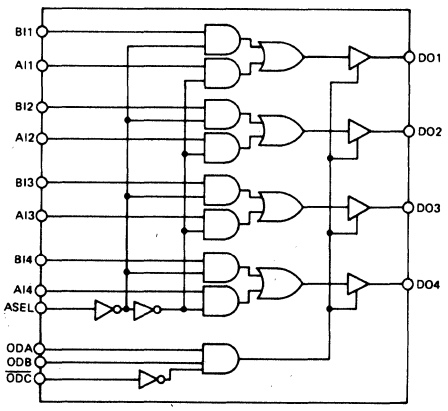


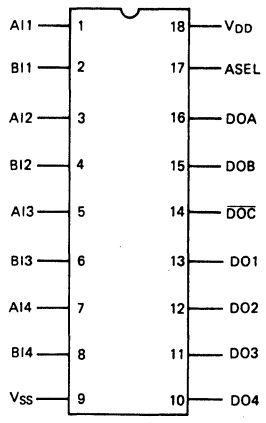
Z43-4



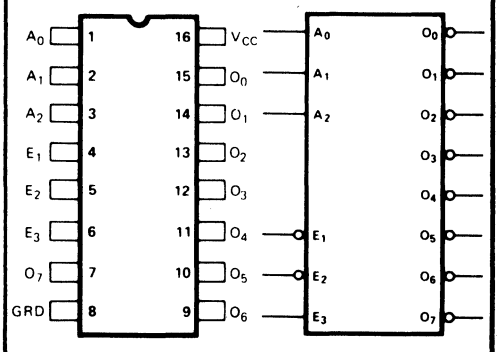


Z43-5

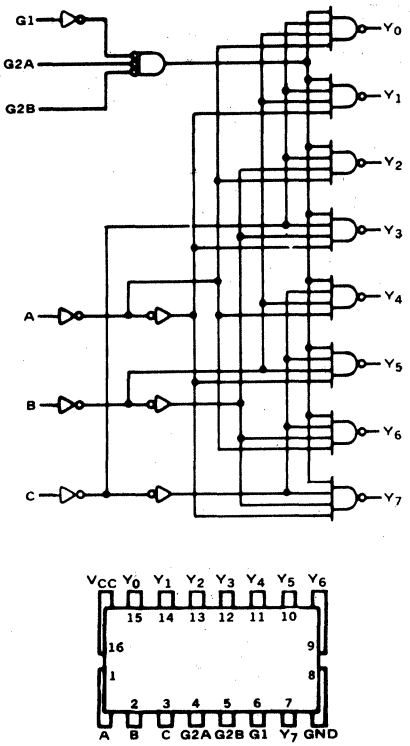




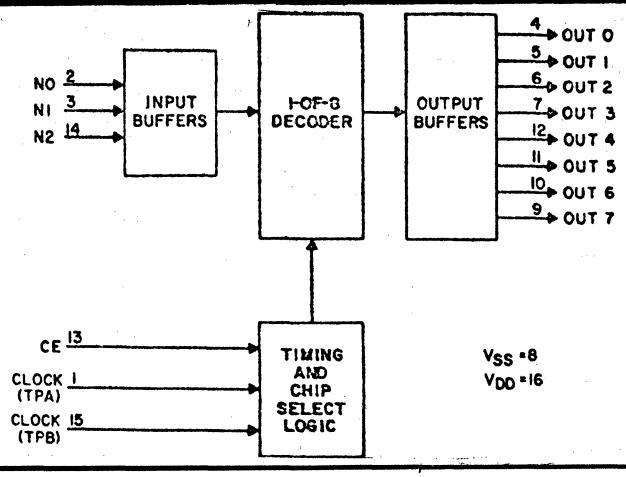
Z44-1



Z44-3



Z44-5



Z45-1

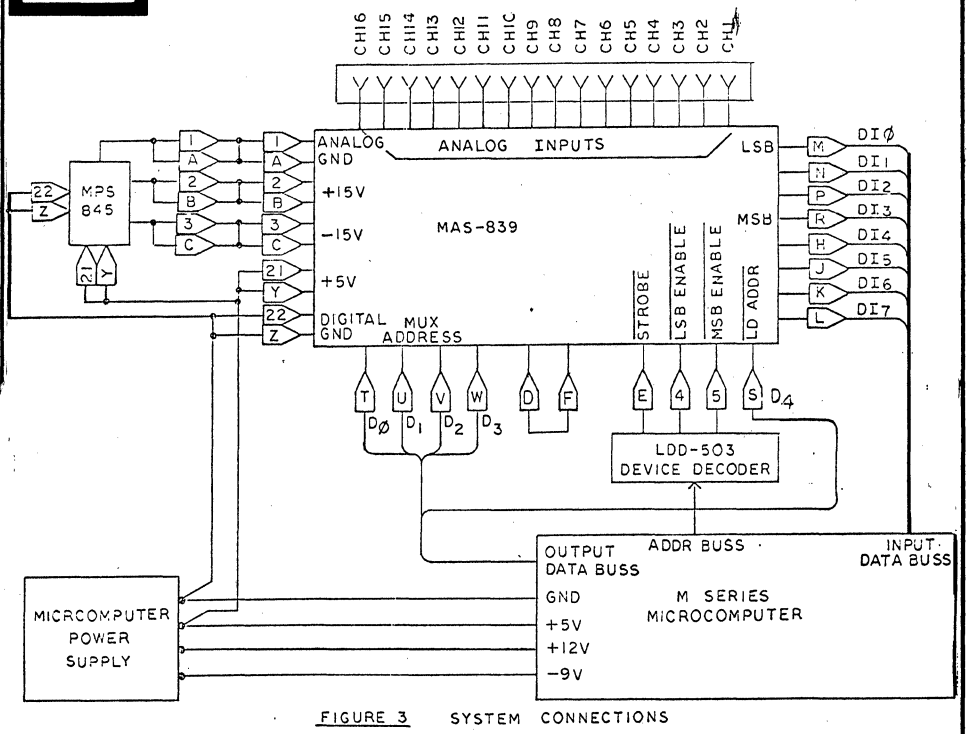
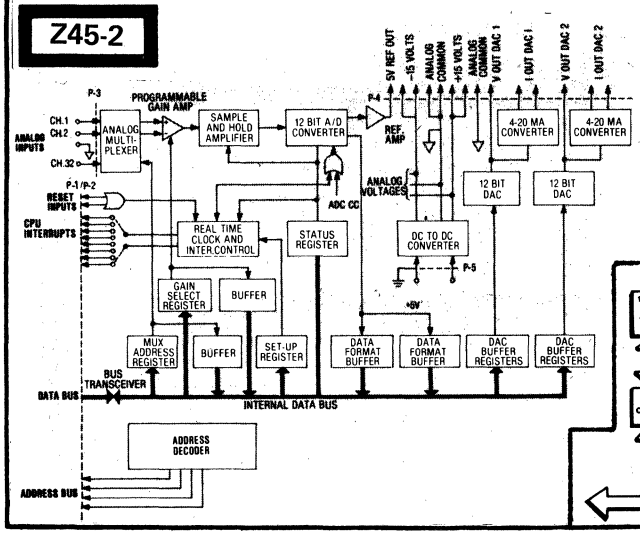
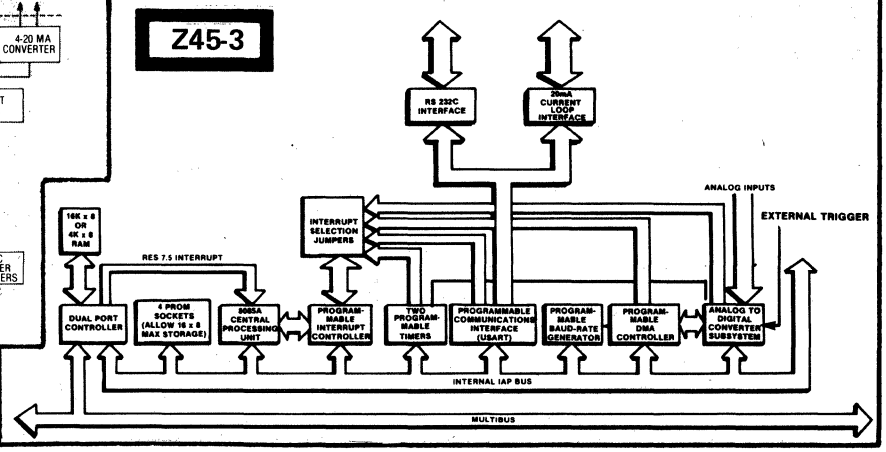


FIGURE 3 SYSTEM CONNECTIONS

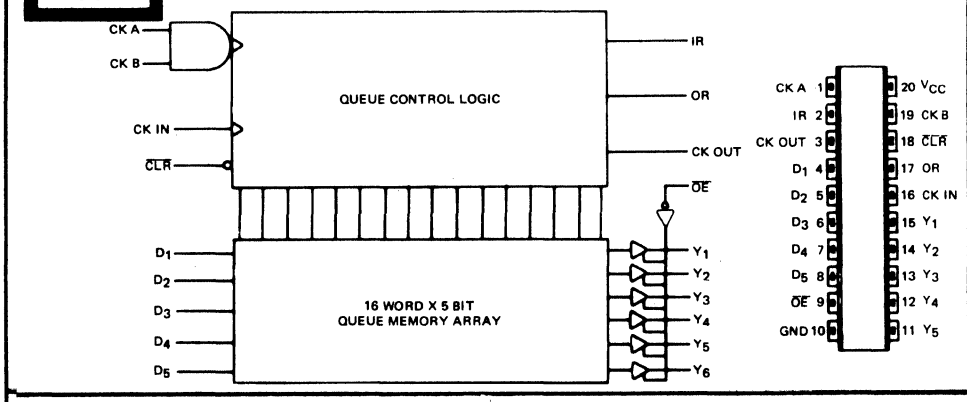
Z45-2



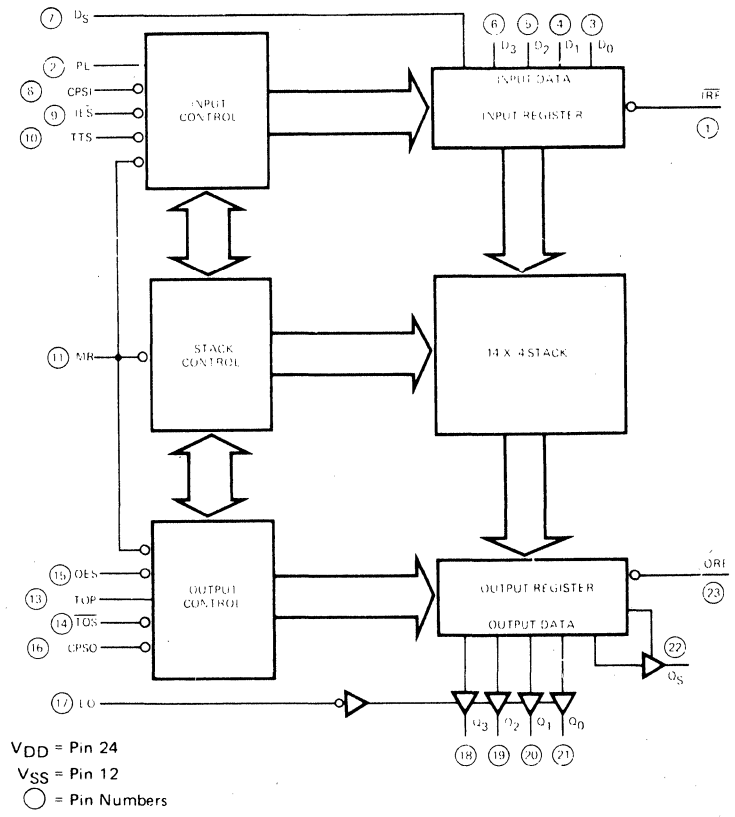
Z45-3



Z55-1

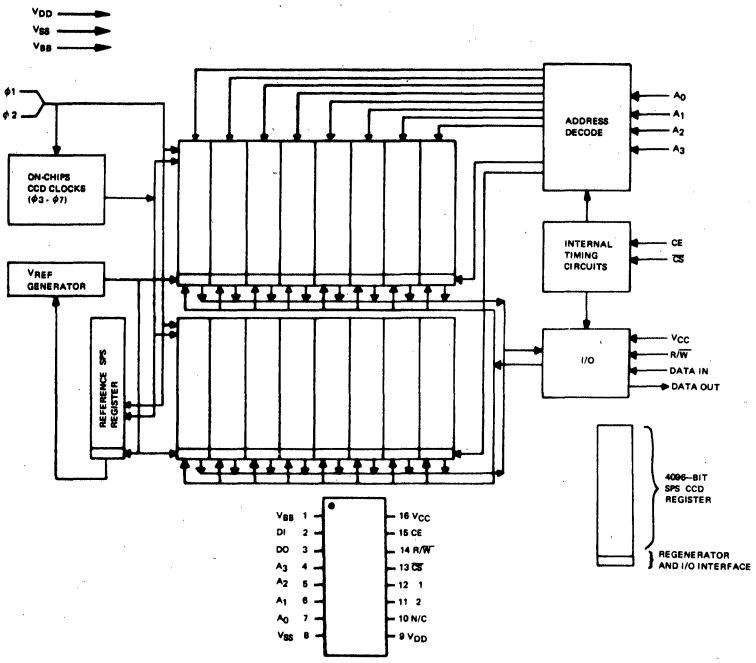


Z55-2

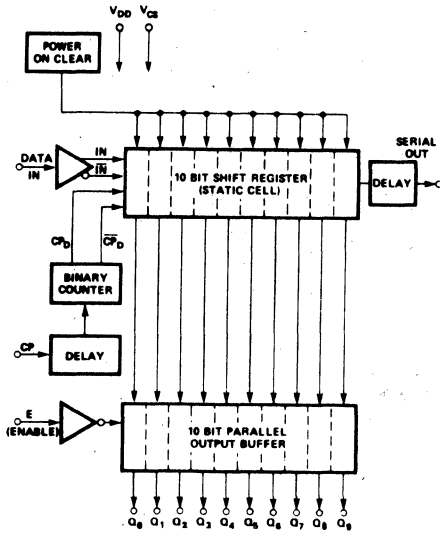


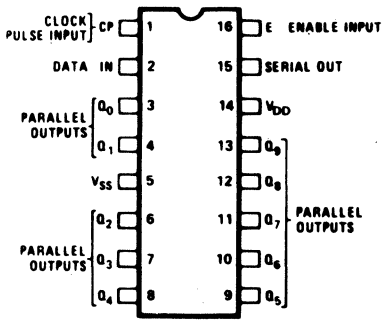
V_{DD} = Pin 24
V_{SS} = Pin 12
◯ = Pin Numbers

Z55-3

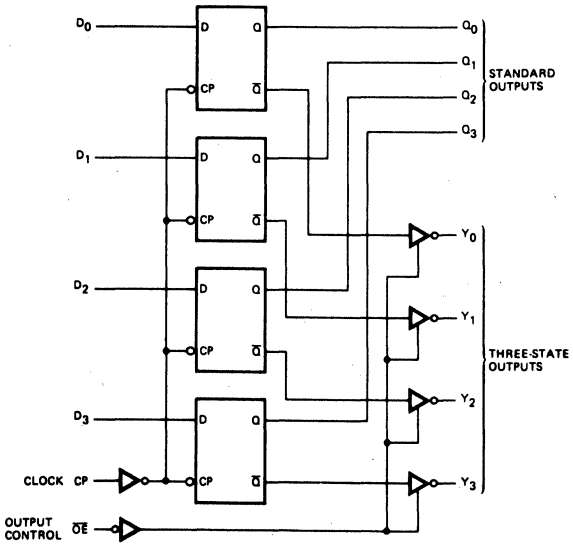


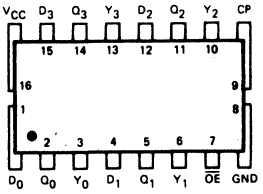
Z55-4



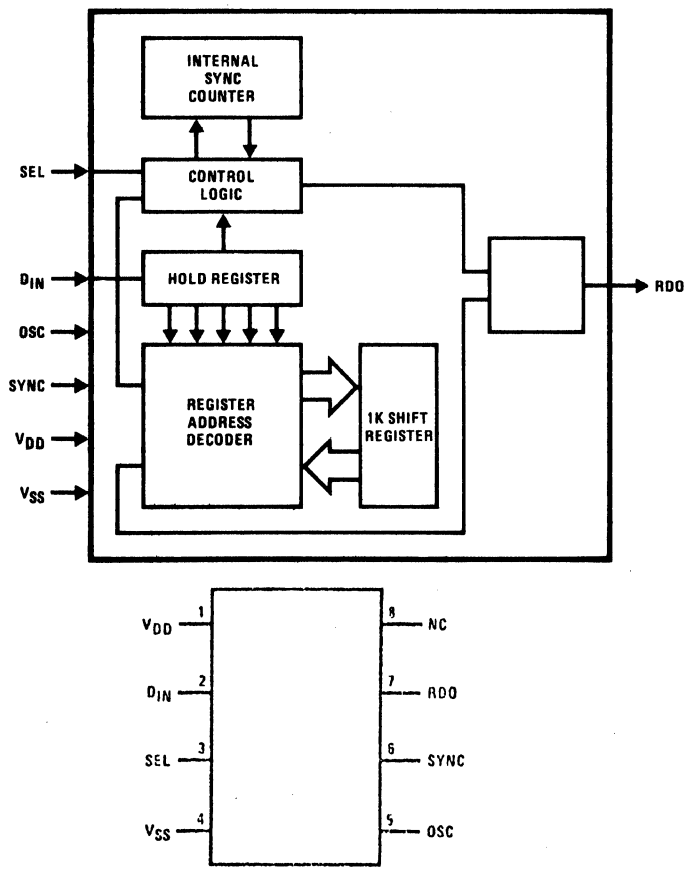


Z55-5

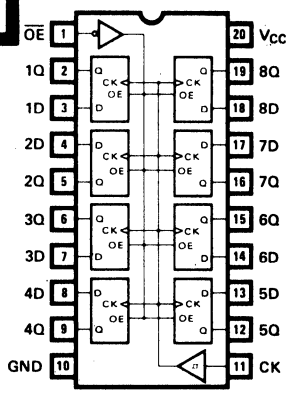




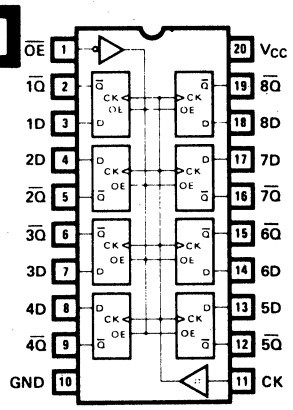
Z55-6



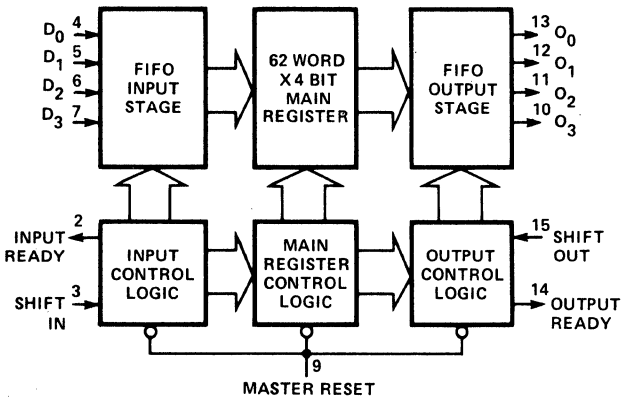
Z55-7



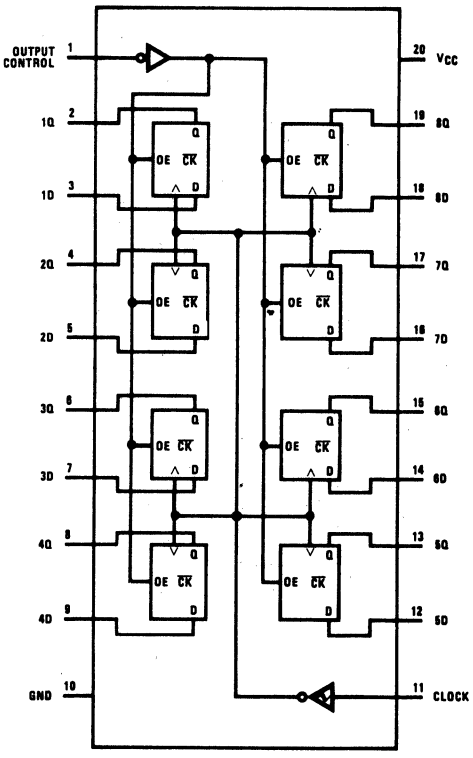
Z55-8



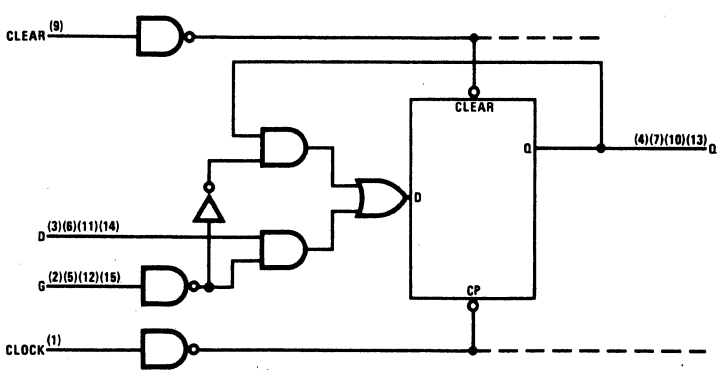
Z55-9



Z55-10



Z55-11

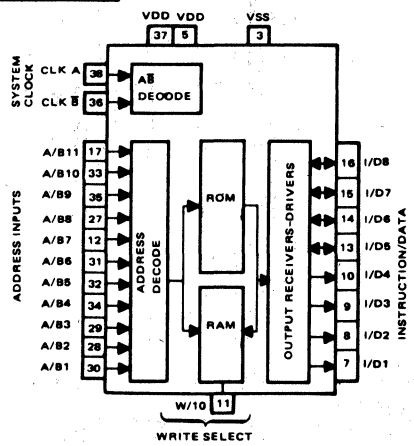


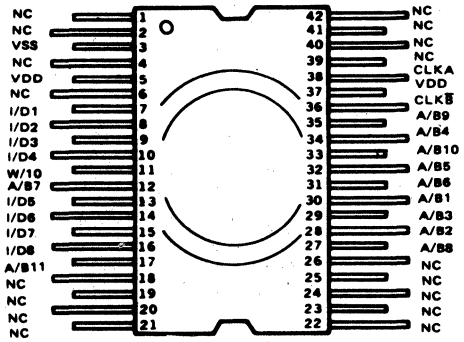
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

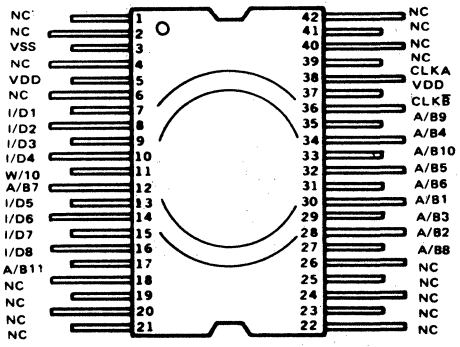
Z55-12

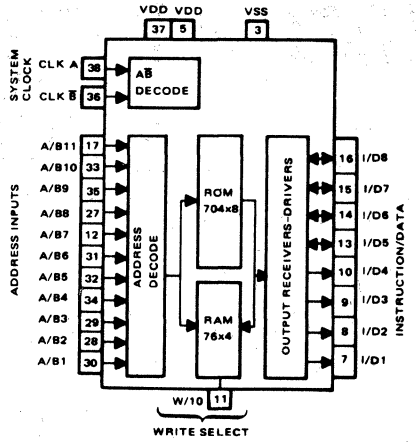
	RAM	ROM
Z55-12	116x4	1024x8
Z55-12a	76x4	704x8



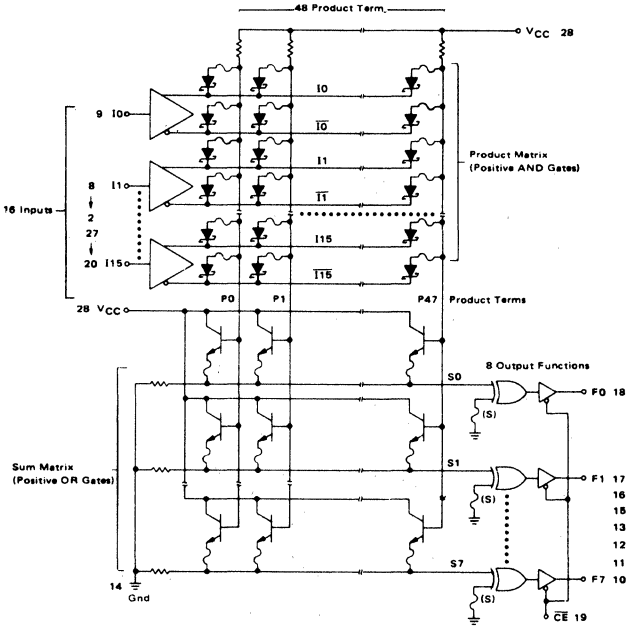


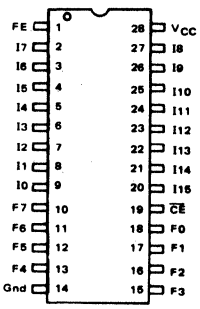
Z55-13



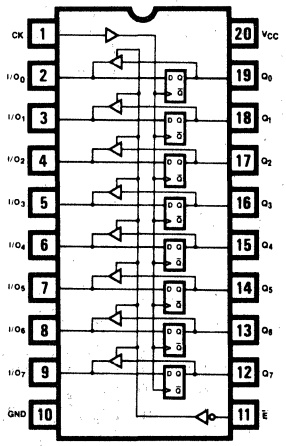


Z55-14

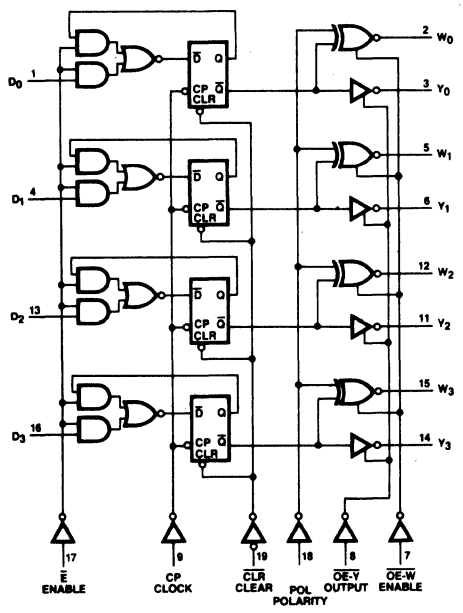




Z55-15

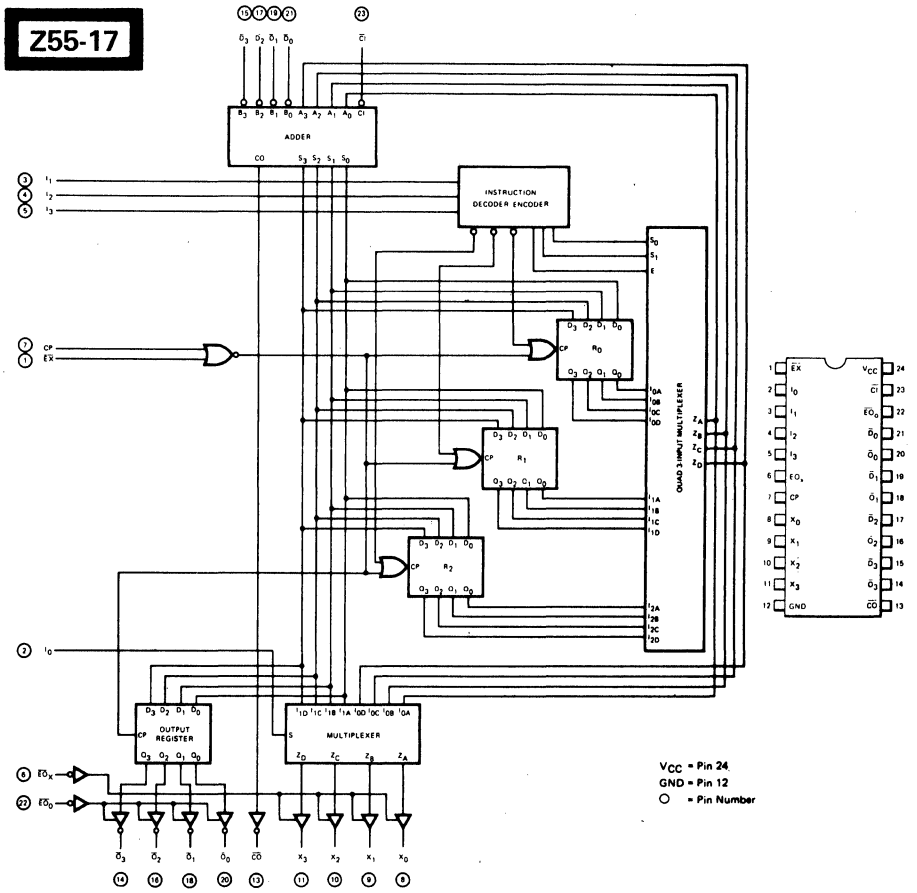


Z55-16



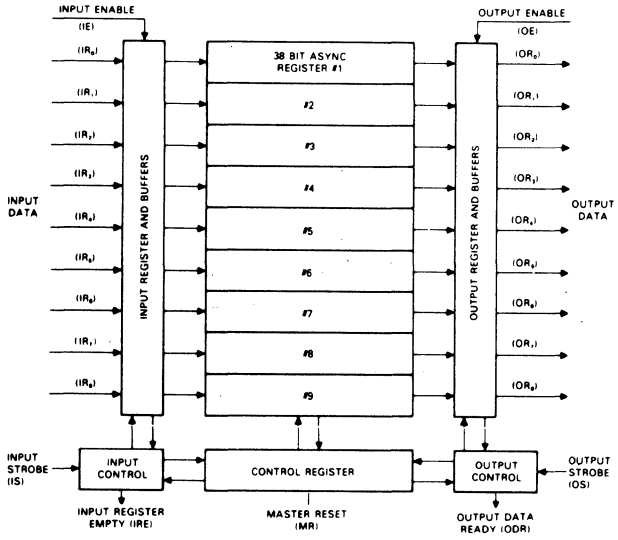
VCC = Pin 20
GND = Pin 10

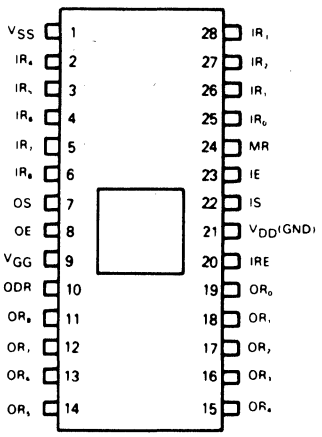
Z55-17



VCC = Pin 24
GND = Pin 12
○ = Pin Number

Z55-18

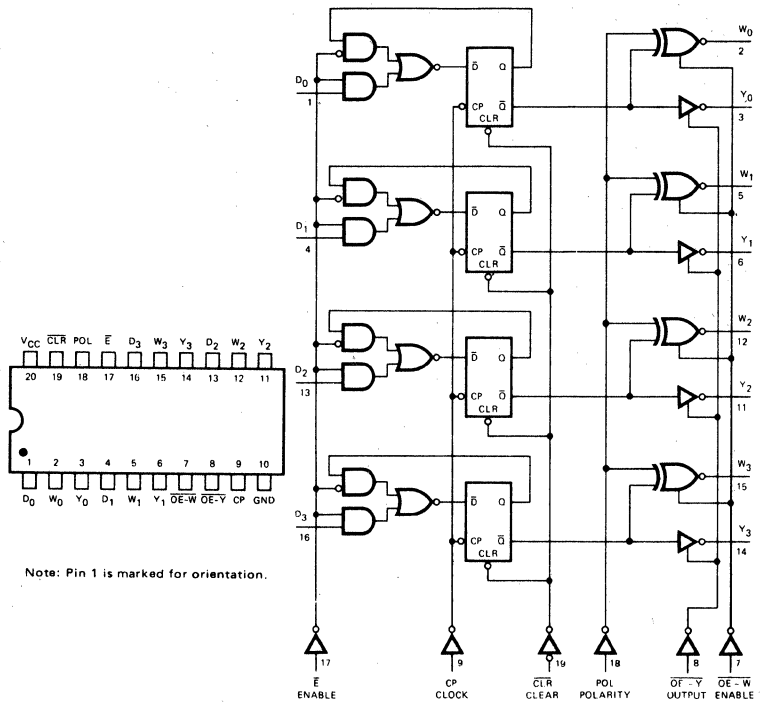




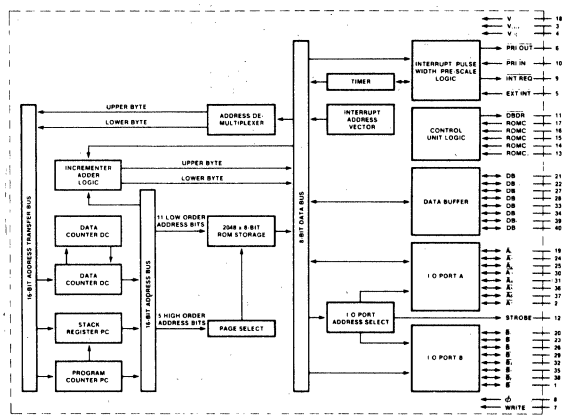
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

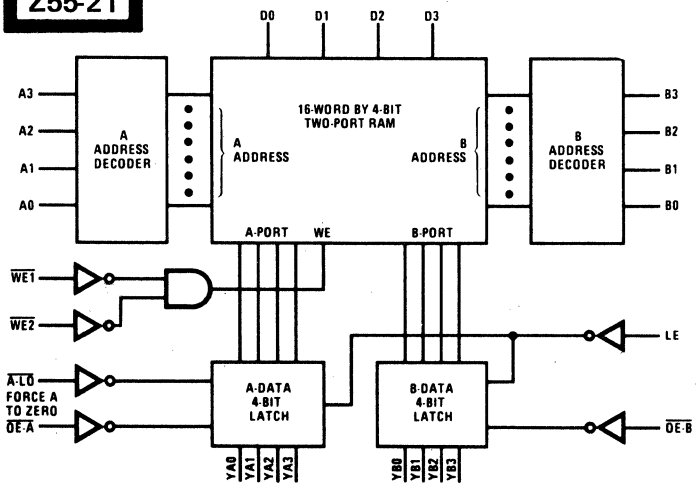
Z55-19



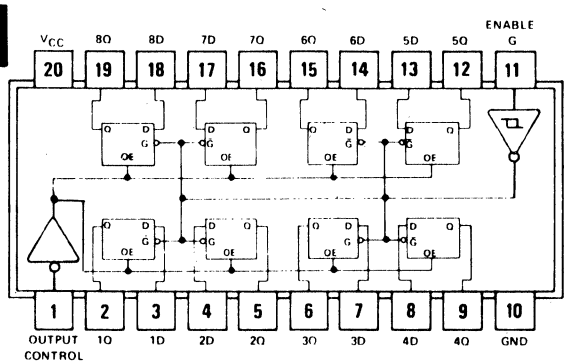
Z55-20



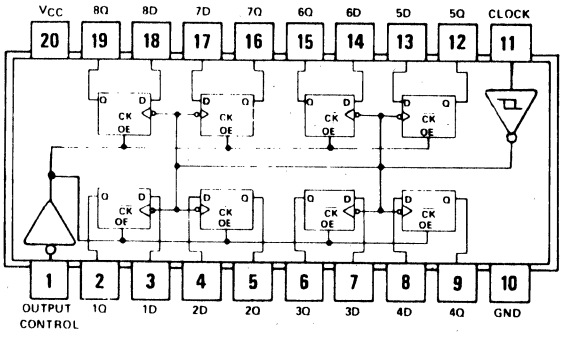
Z55-21



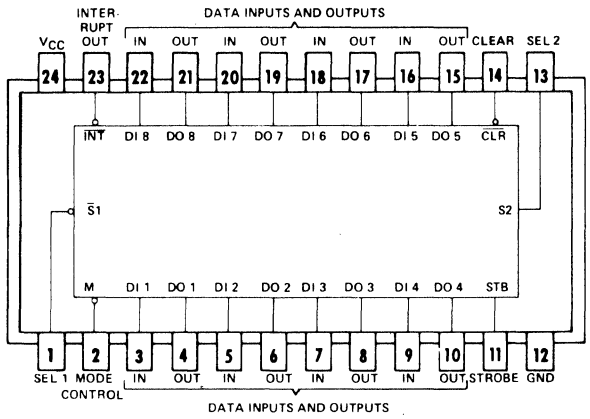
Z56-1



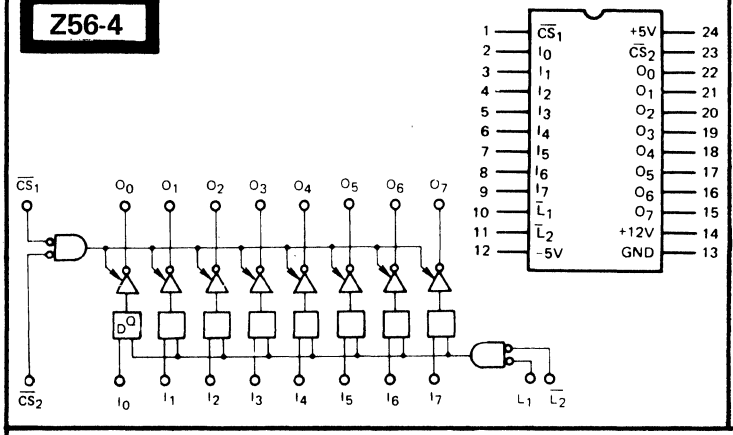
Z56-2



Z56-3

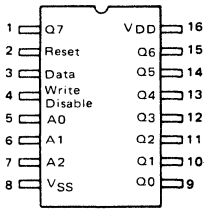


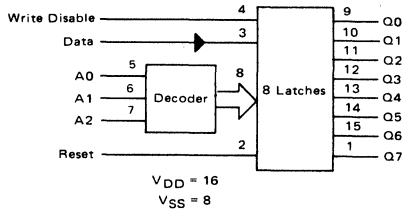
Z56-4



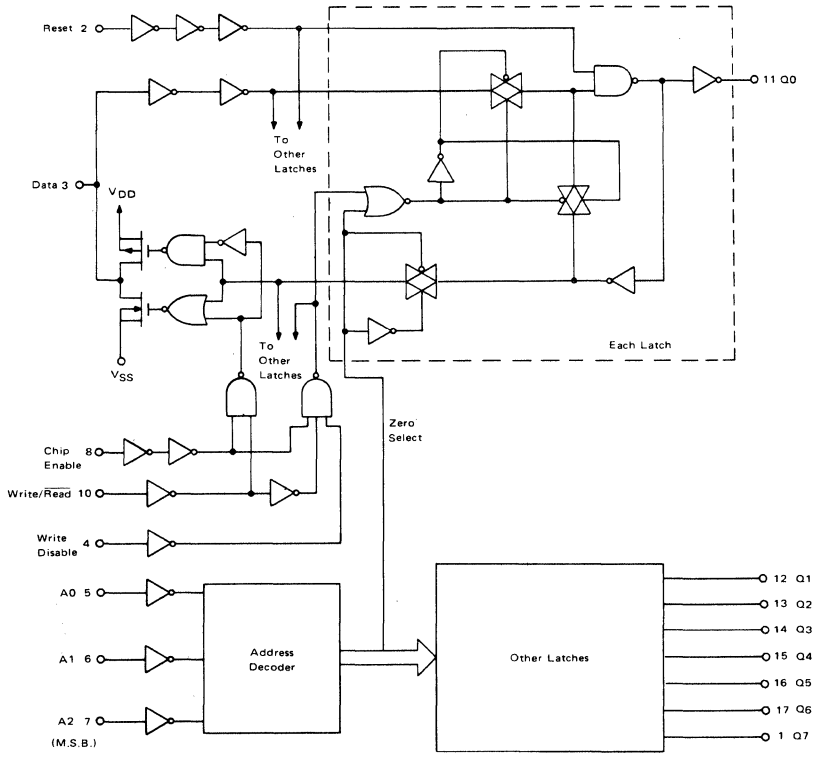
Z56-5

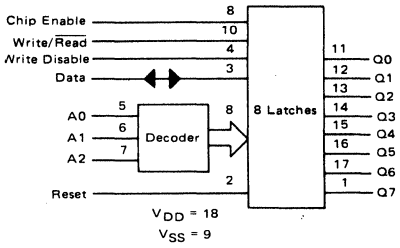
PIN ASSIGNMENT





Z56-6





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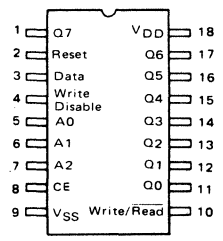
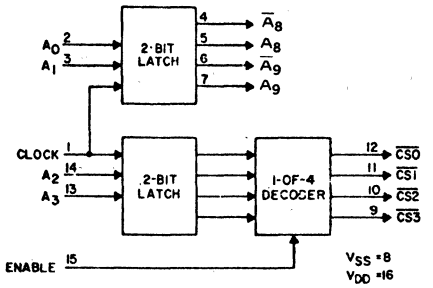


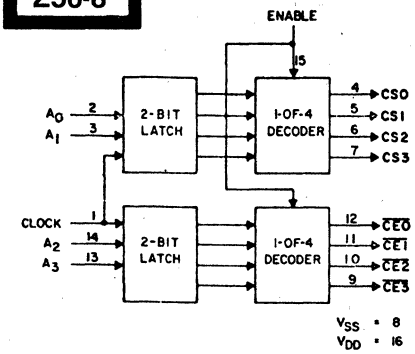
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

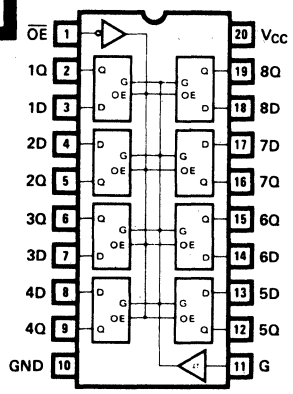
Z56-7



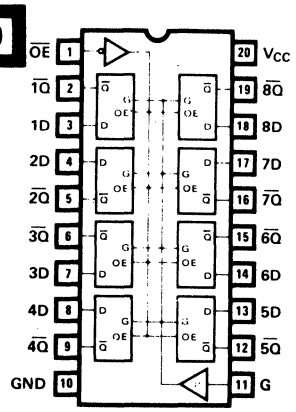
Z56-8



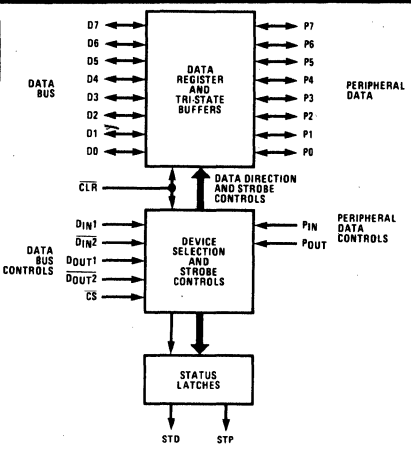
Z56-9

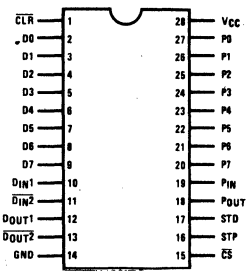


Z56-10

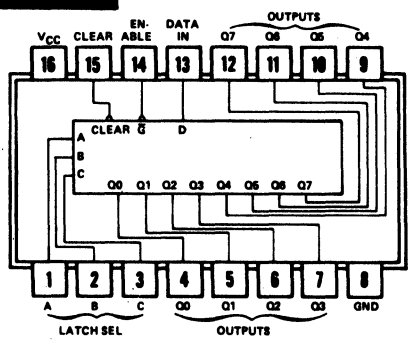


Z56-11

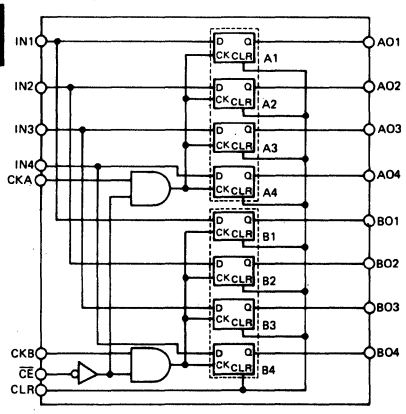


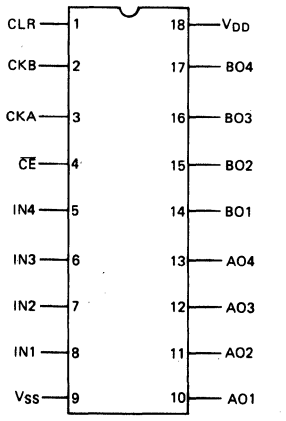


Z56-12

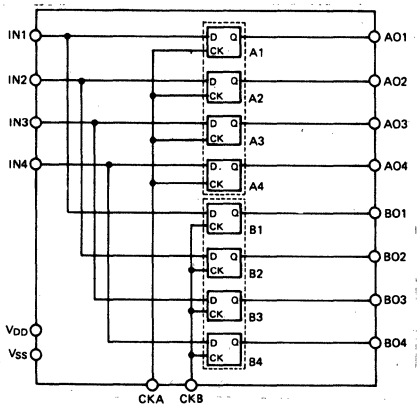


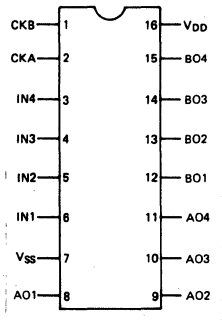
Z56-13



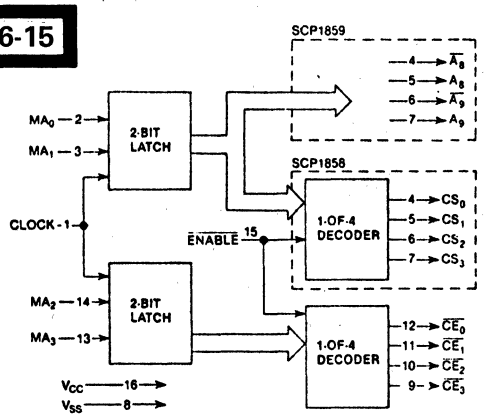


Z56-14

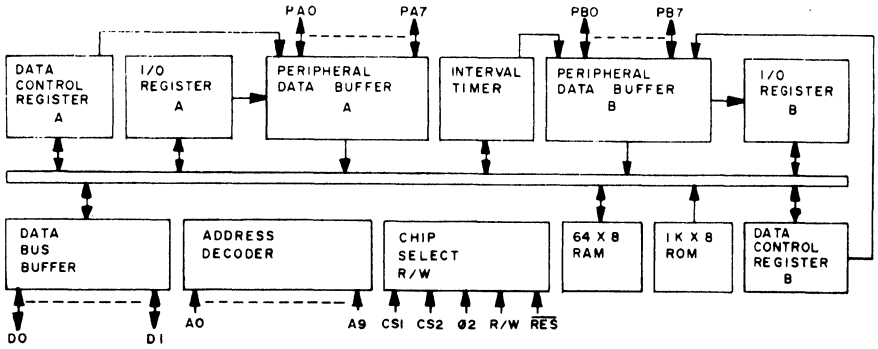


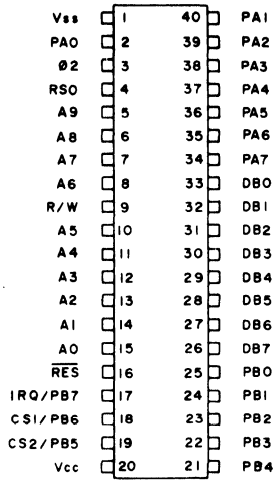


Z56-15

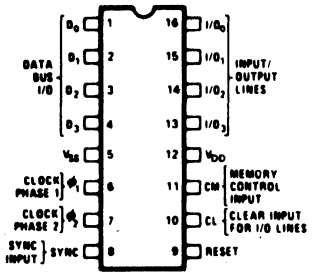


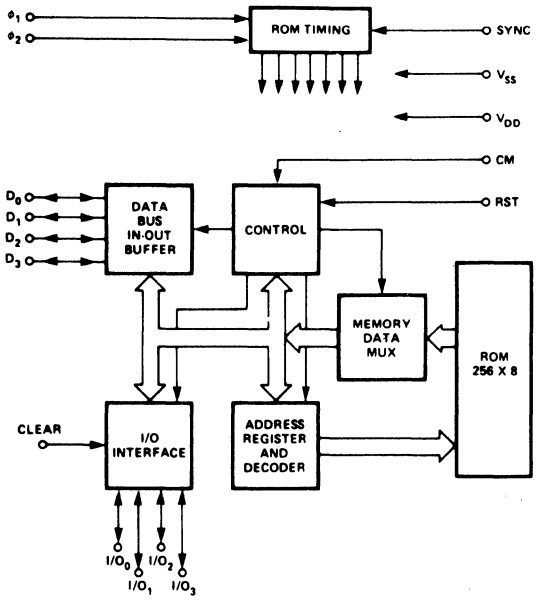
Z57-1



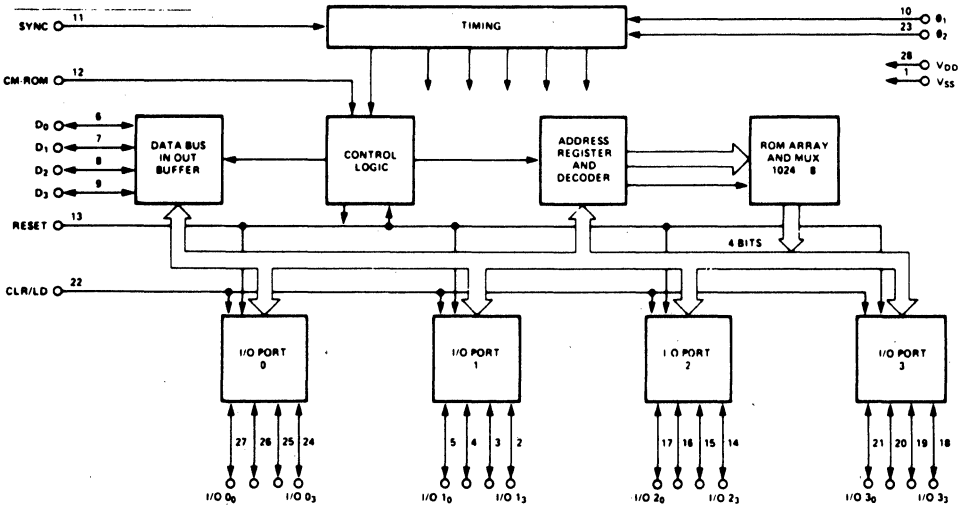


Z57-2

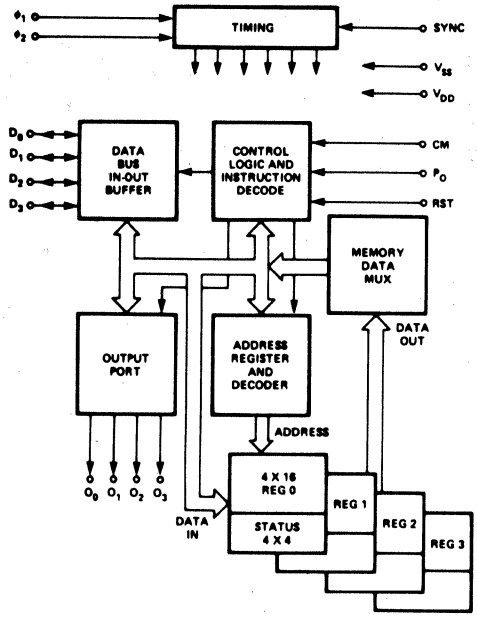


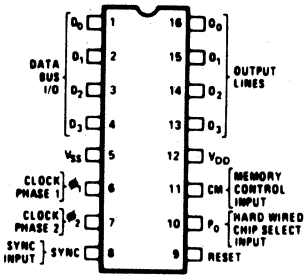


Z57-3

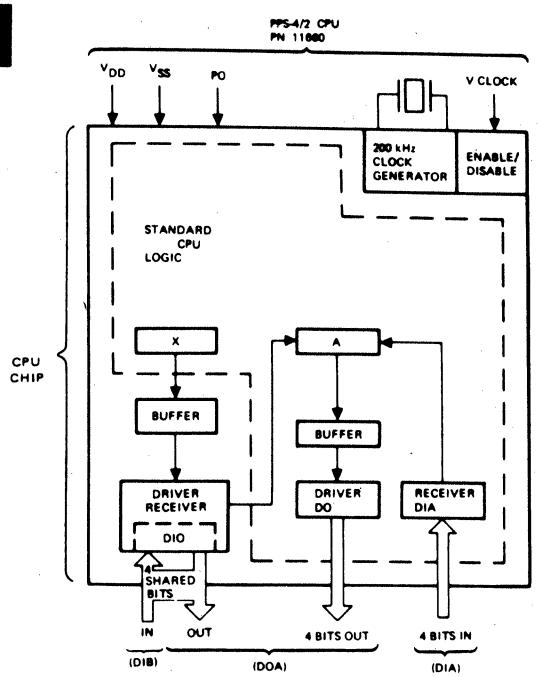


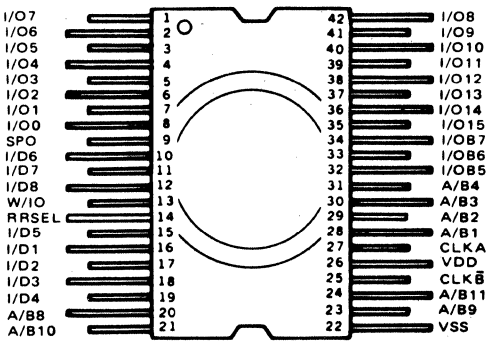
Z57-4



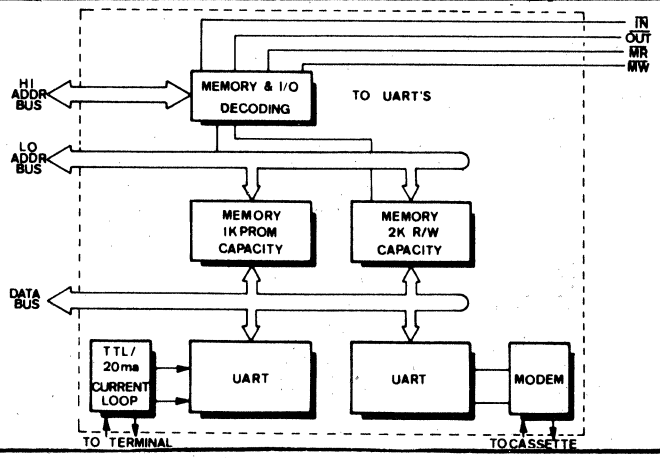


Z57-5

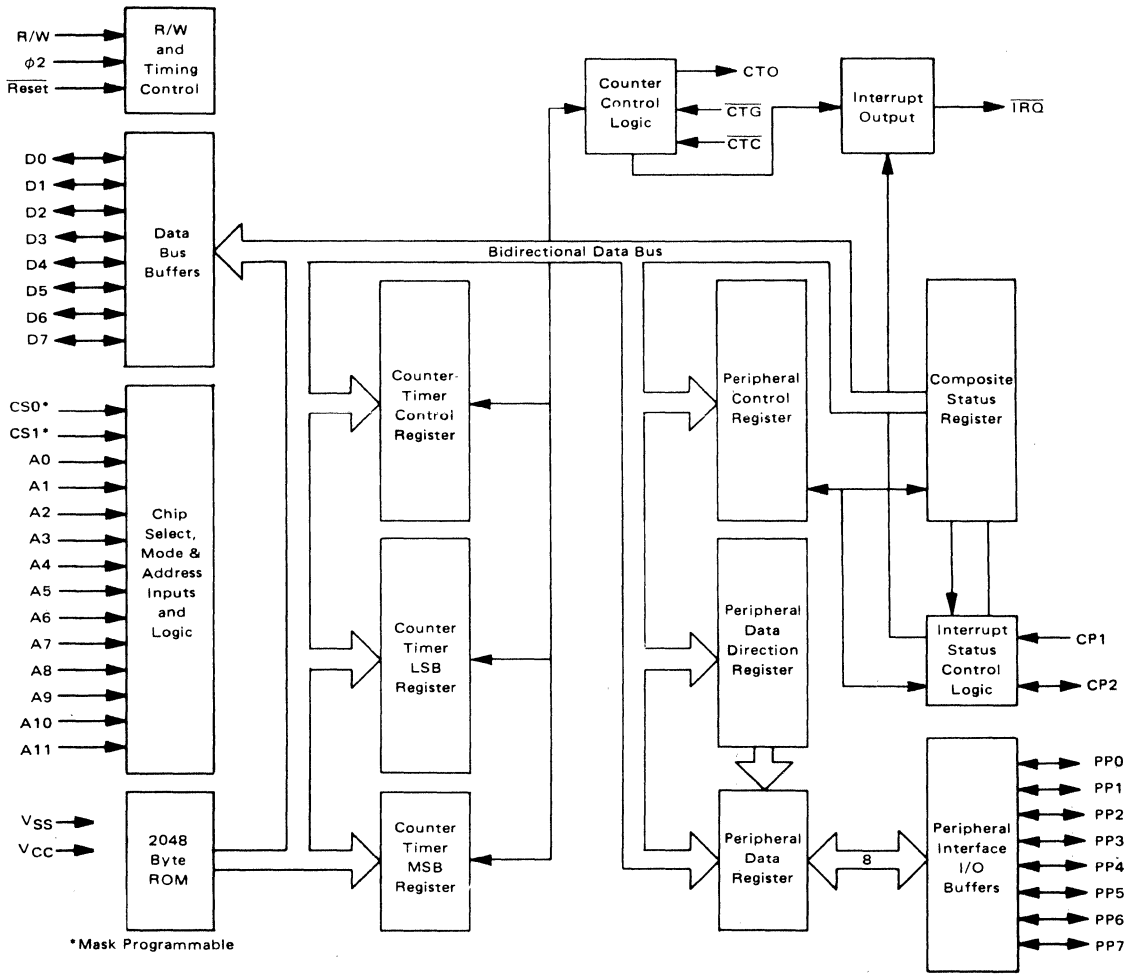


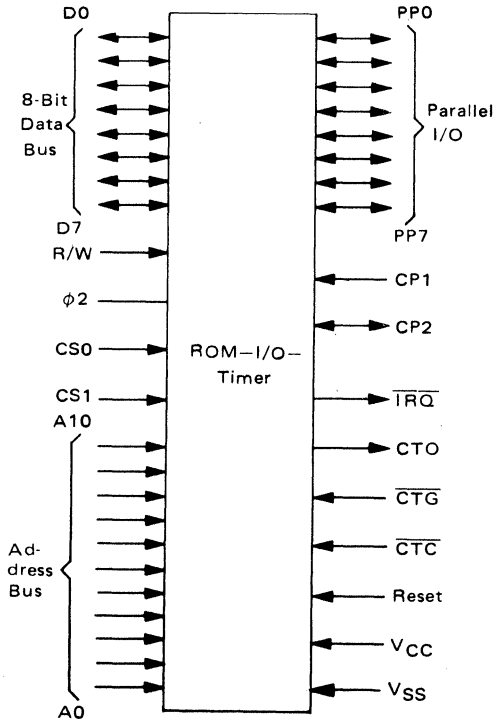


Z57-6

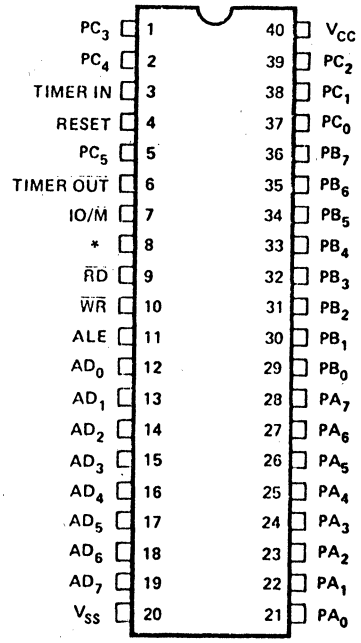


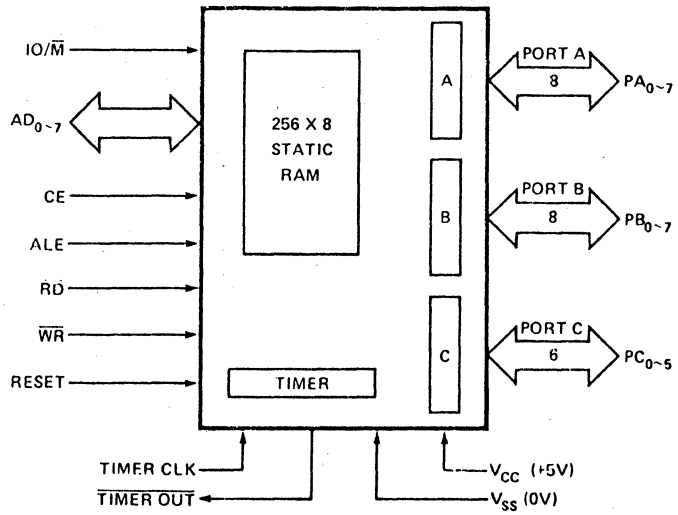
Z57-8


R/W
φ2
Reset
R/W and Timing Control
D0
D1
D2
D3
D4
D5
D6
D7
Data Bus Buffers
CS0*
CS1*
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
Chip Select, Mode & Address Inputs and Logic
VSS
VCC
2048 Byte ROM
*Mask Programmable
Counter Control Logic
CTO
CTG
CTC
Interrupt Output
IRQ
Bidirectional Data Bus
Counter-Timer Control Register
Counter Timer LSB Register
Counter Timer MSB Register
Peripheral Control Register
Peripheral Data Direction Register
Peripheral Data Register
8
Composite Status Register
Interrupt Status Control Logic
CP1
CP2
Peripheral Interface I/O Buffers
PP0
PP1
PP2
PP3
PP4
PP5
PP6
PP7


D0
8-Bit Data Bus
D7
R/W
φ2
CS0
CS1
A10
Address Bus
A0
ROM—I/O—Timer
PP0
Parallel I/O
PP7
CP1
CP2
IRQ
CTO
CTG
CTC
Reset
VCC
VSS

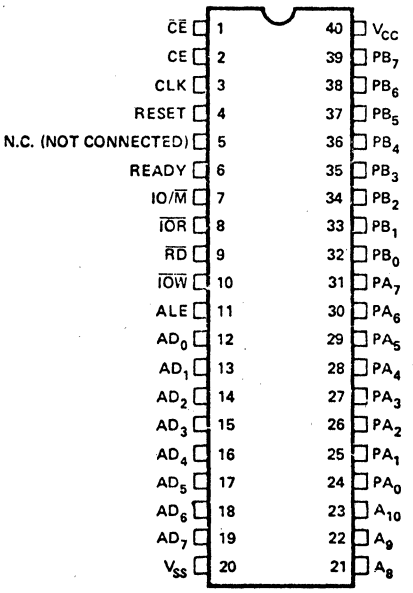
Z57-9

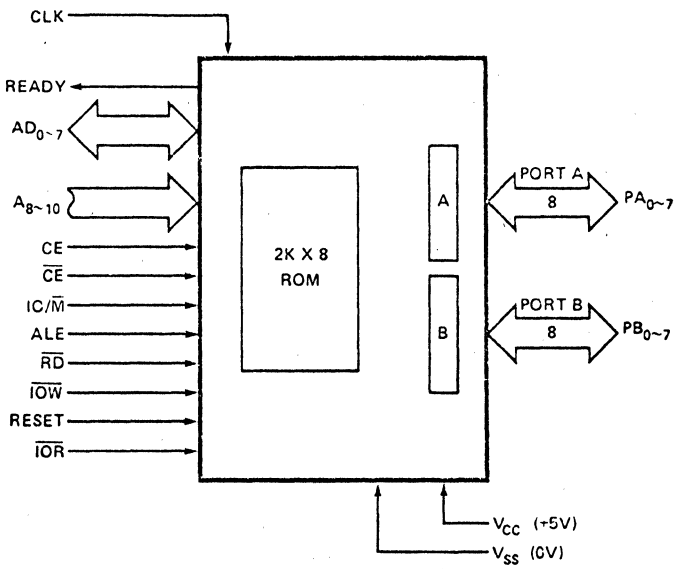




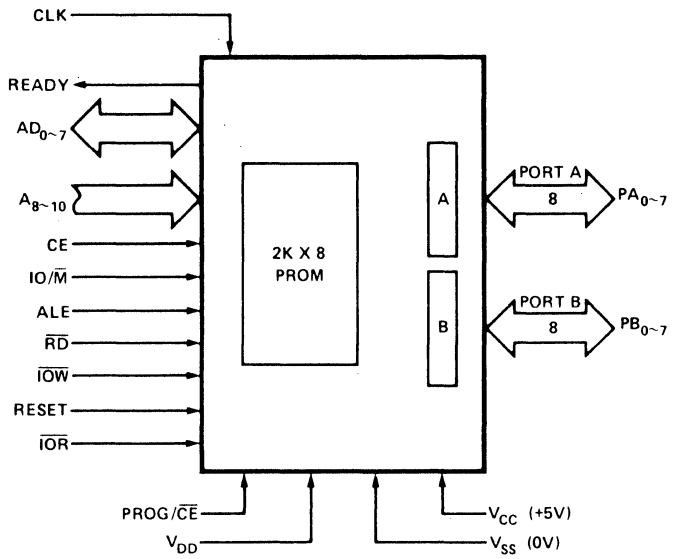
Z57-9: *PIN 8 = CE
Z57-9a: *PIN 8 = $\overline{CE}$

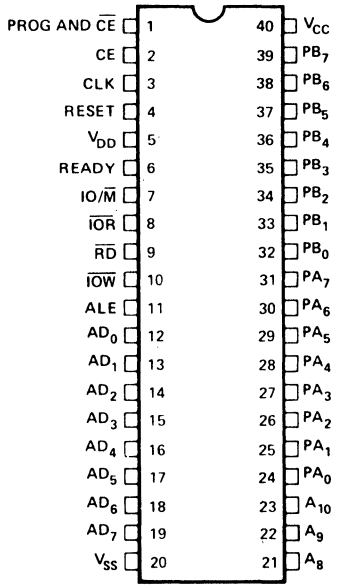
Z57-10



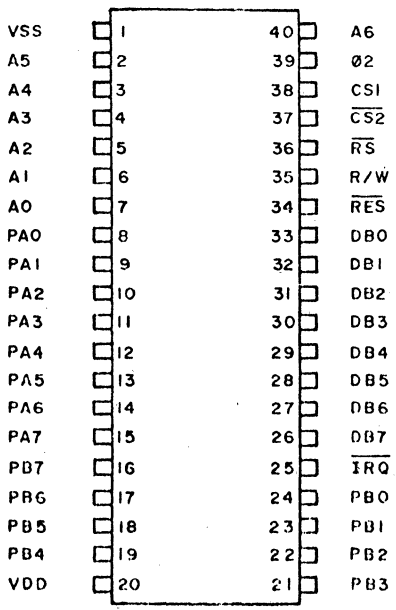


Z57-11

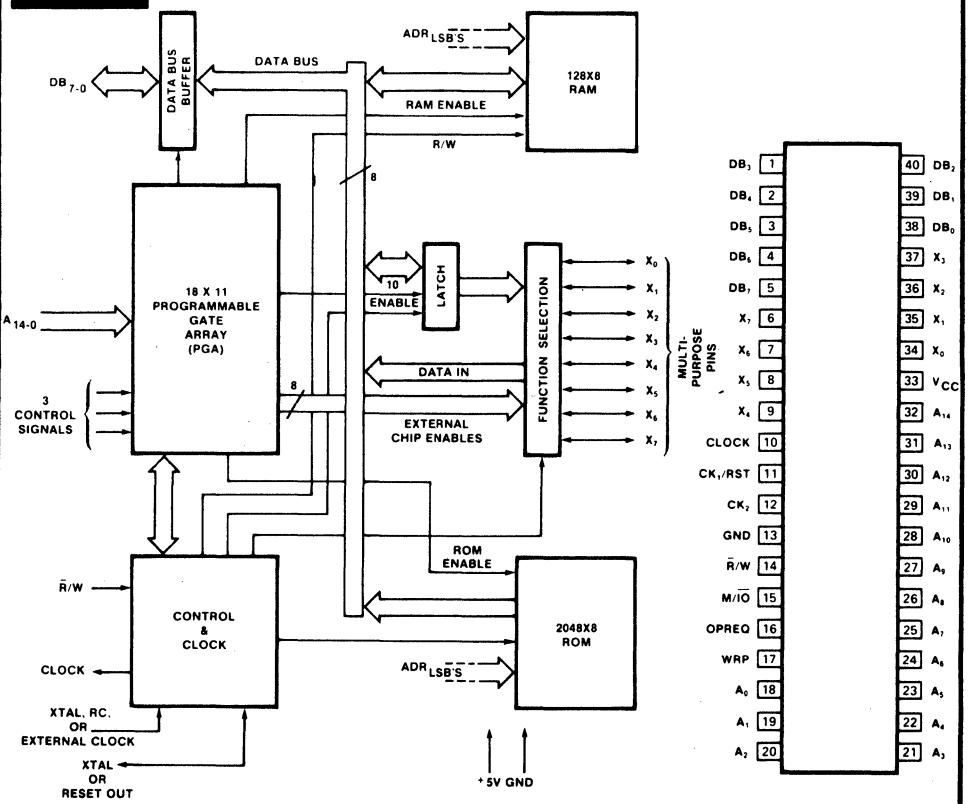




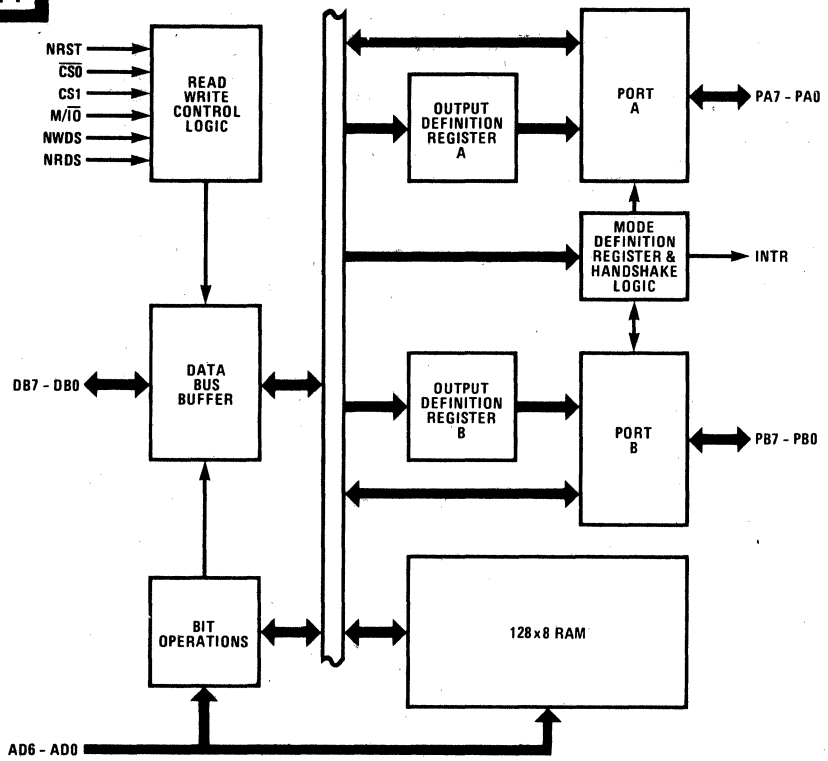
Z57-12

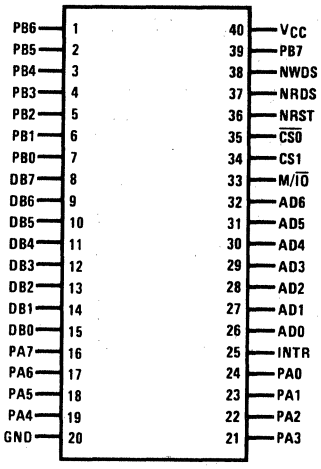


Z57-13

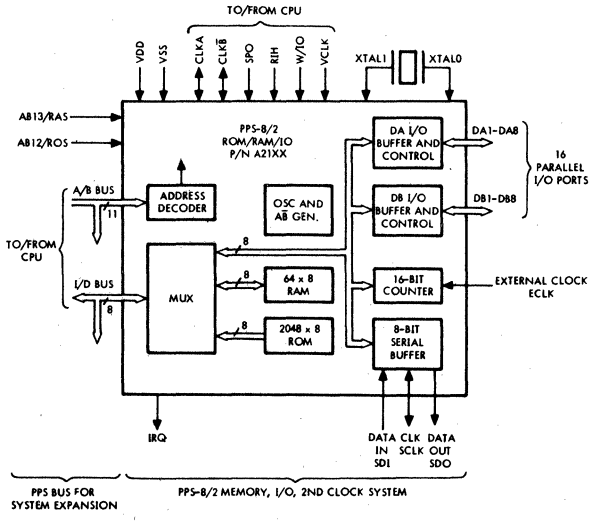


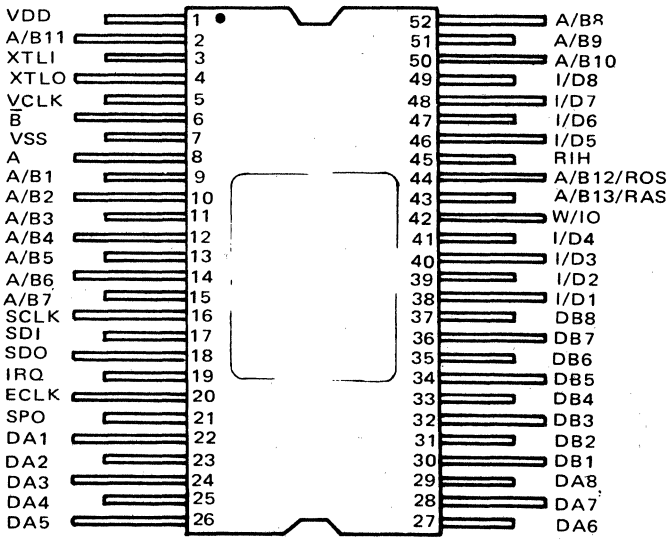
Z57-14


NRST
CS0
CS1
M/IO
NWDS
NRDS
READ WRITE CONTROL LOGIC
OUTPUT DEFINITION REGISTER A
PORT A
PA7 - PA0
MODE DEFINITION REGISTER & HANDSHAKE LOGIC
INTR
DB7 - DB0
DATA BUS BUFFER
OUTPUT DEFINITION REGISTER B
PORT B
PB7 - PB0
BIT OPERATIONS
128x8 RAM
AD6 - AD0

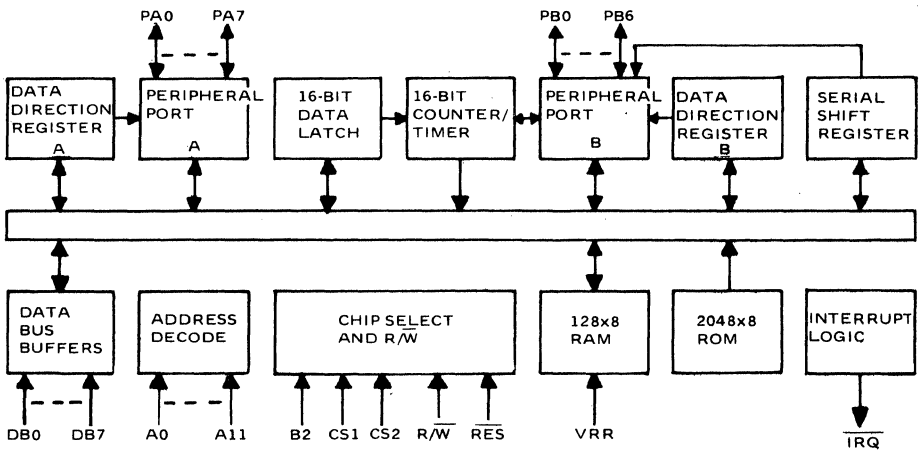

PB6 1
PB5 2
PB4 3
PB3 4
PB2 5
PB1 6
PB0 7
DB7 8
DB6 9
DB5 10
DB4 11
DB3 12
DB2 13
DB1 14
DB0 15
PA7 16
PA6 17
PA5 18
PA4 19
GND 20
40 VCC
39 PB7
38 NWDS
37 NRDS
36 NRST
35 CS0
34 CS1
33 M/IO
32 AD6
31 AD5
30 AD4
29 AD3
28 AD2
27 AD1
26 AD0
25 INTR
24 PA0
23 PA1
22 PA2
21 PA3

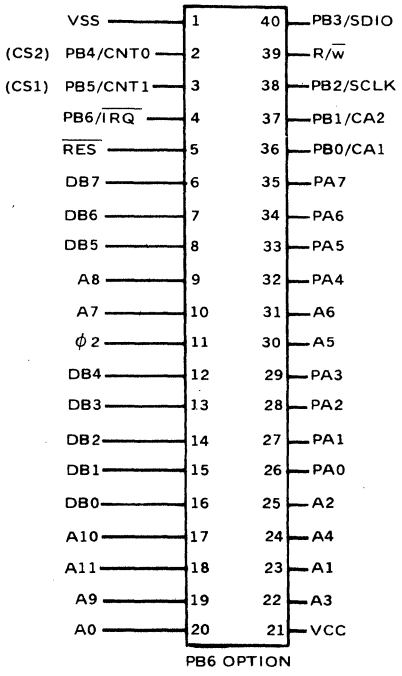
Z57-15


TO/FROM CPU
VDD
VSS
CLKA
CLKB
SPO
RIH
W/IO
VCLK
XTALI
XTALO
AB13/RAS
AB12/ROS
PPS-8/2 ROM/RAM/IO P/N A21XX
DA I/O BUFFER AND CONTROL
DA1-DA8
16 PARALLEL I/O PORTS
A/B BUS
ADDRESS DECODER
OSC AND AB GEN.
DB I/O BUFFER AND CONTROL
DB1-DB8
TO/FROM CPU
I/D BUS
MUX
64 x 8 RAM
2048 x 8 ROM
16-BIT COUNTER
EXTERNAL CLOCK ECLK
8-BIT SERIAL BUFFER
IRQ
DATA IN SDI
CLK SCLK
DATA OUT SDO
PPS BUS FOR SYSTEM EXPANSION
PPS-8/2 MEMORY, I/O, 2ND CLOCK SYSTEM

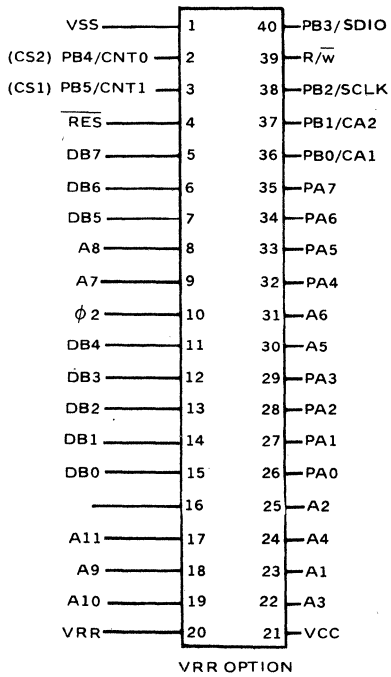

VDD 1
A/B11 2
XTLI 3
XTLO 4
VCLK 5
B 6
VSS 7
A 8
A/B1 9
A/B2 10
A/B3 11
A/B4 12
A/B5 13
A/B6 14
A/B7 15
SCLK 16
SDI 17
SDO 18
IRQ 19
ECLK 20
SPO 21
DA1 22
DA2 23
DA3 24
DA4 25
DA5 26
52 A/B8
51 A/B9
50 A/B10
49 I/D8
48 I/D7
47 I/D6
46 I/D5
45 RIH
44 A/B12/ROS
43 A/B13/RAS
42 W/IO
41 I/D4
40 I/D3
39 I/D2
38 I/D1
37 DB8
36 DB7
35 DB6
34 DB5
33 DB4
32 DB3
31 DB2
30 DB1
29 DA8
28 DA7
27 DA6

Z57-16



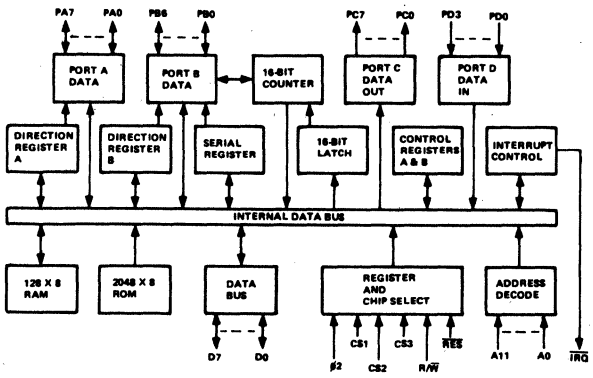


PB6 OPTION

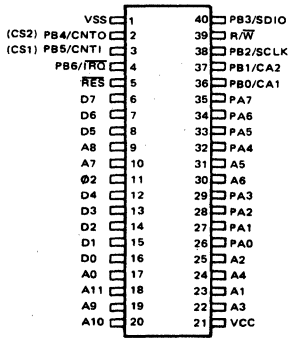


VRR OPTION

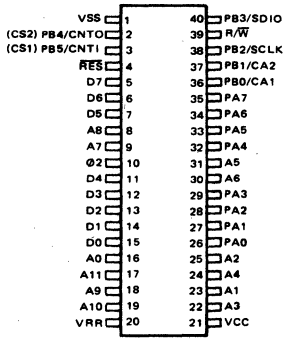
Z57-17



Z57-17

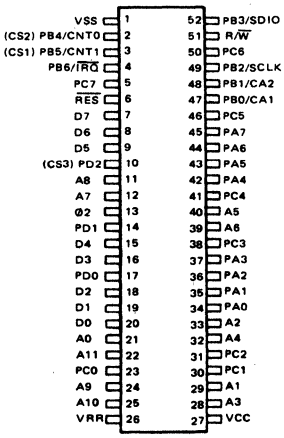


40- Pin Configuration
PB6 Option

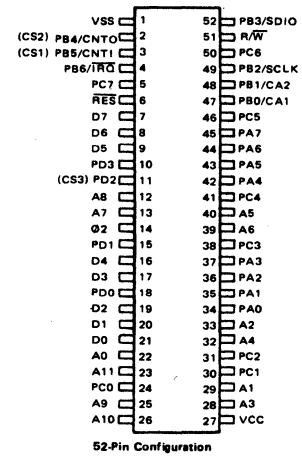


40-Pin Configuration
VRR Option

Z57-17a

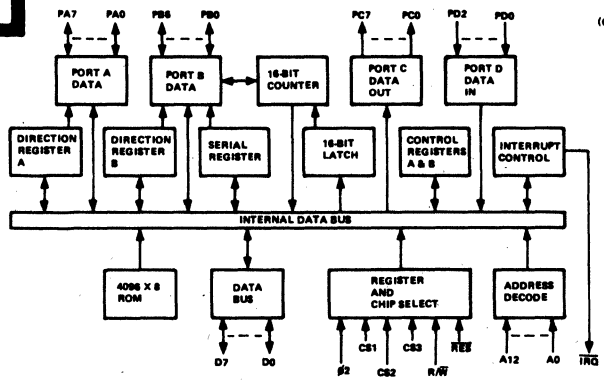


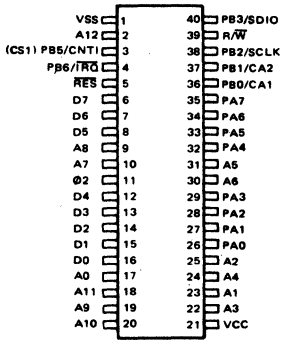
52-Pin Configuration
VRR Option



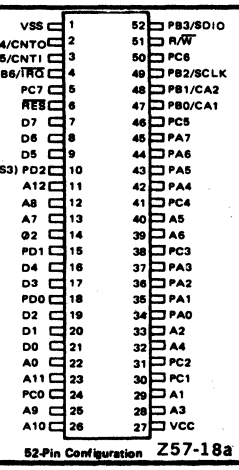
52-Pin Configuration
PD3 Option

Z57-18





40- Pin Configuration
Z57-18

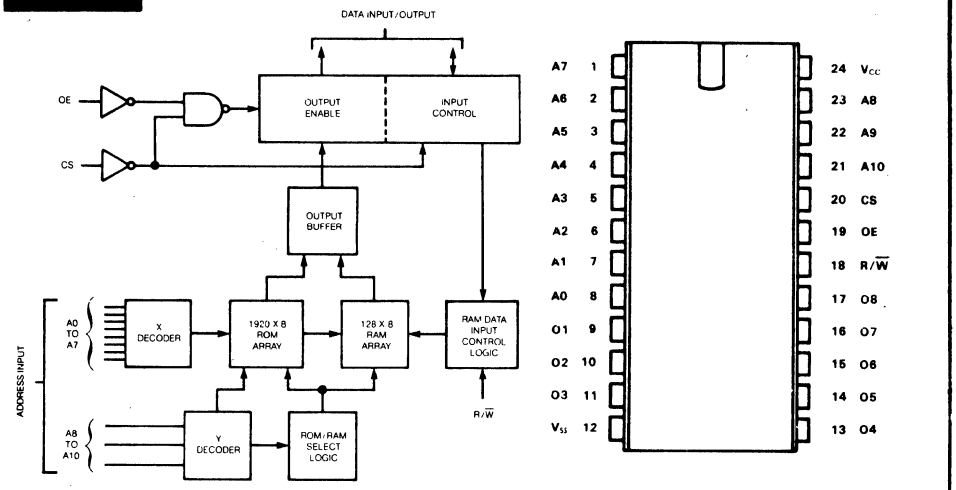


52-Pin Configuration
Z57-18a

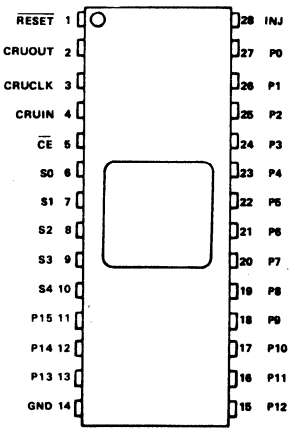
19. LOGIC/BLOCK DRAWINGS

IN DRAWING NUMBER SEQUENCE

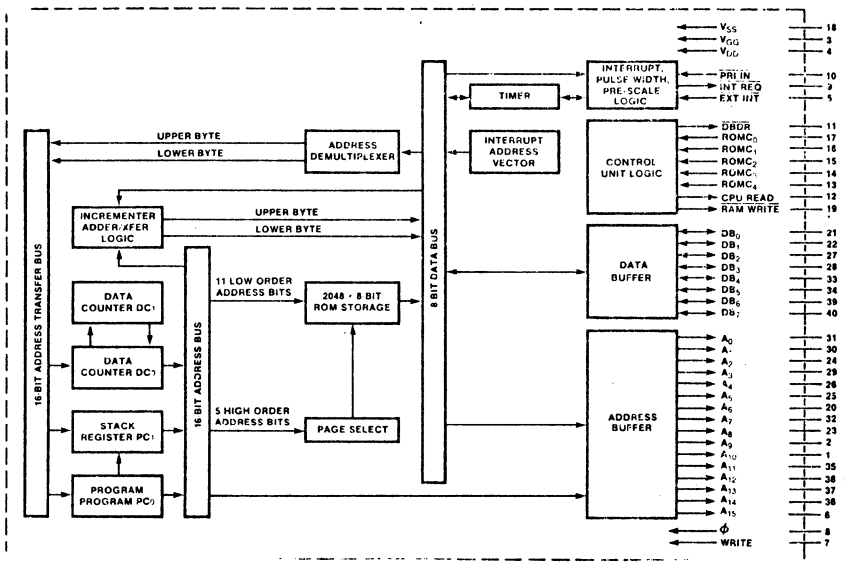
Z57-19



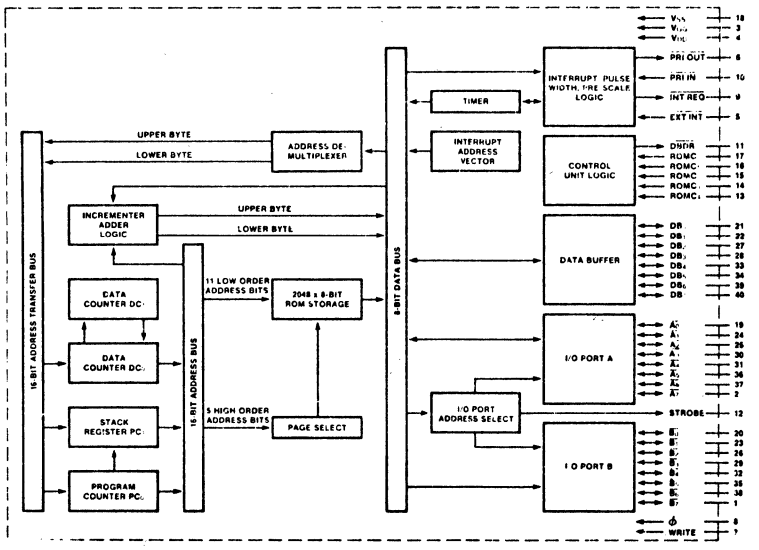
Z57-20



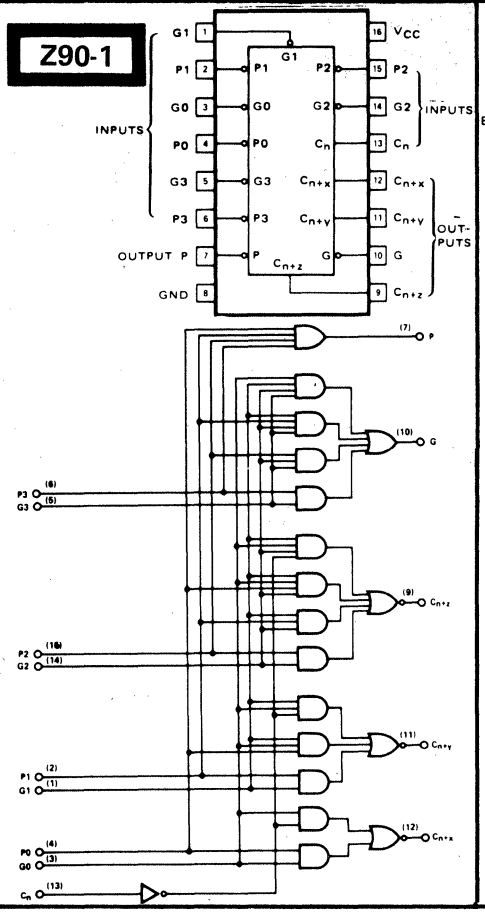
Z57-22



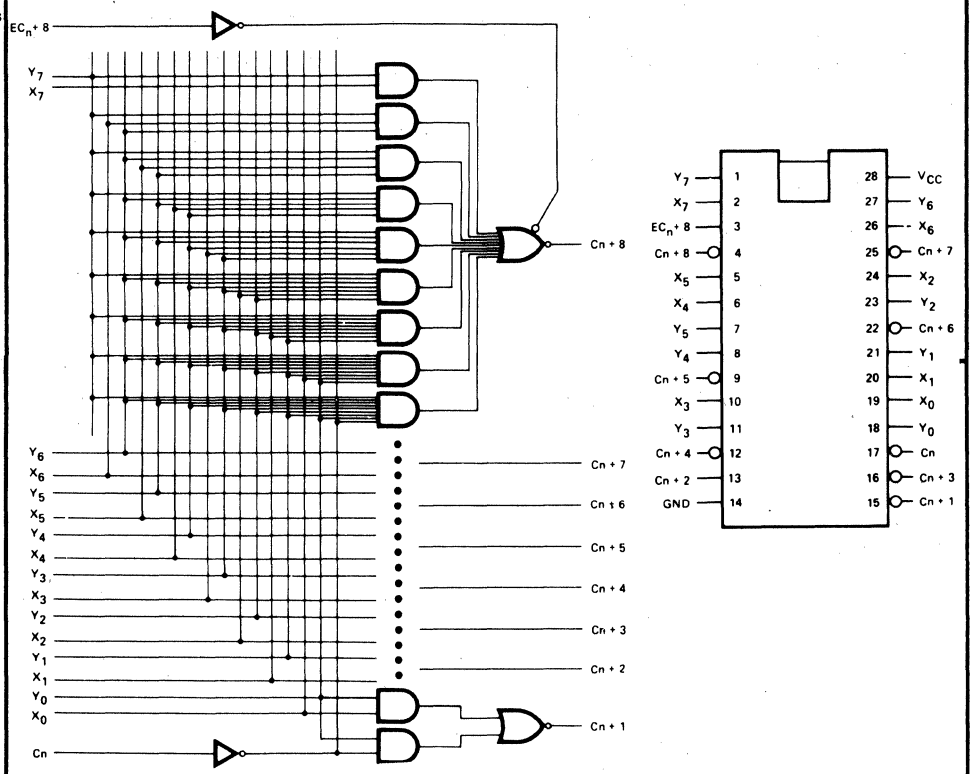
Z57-23



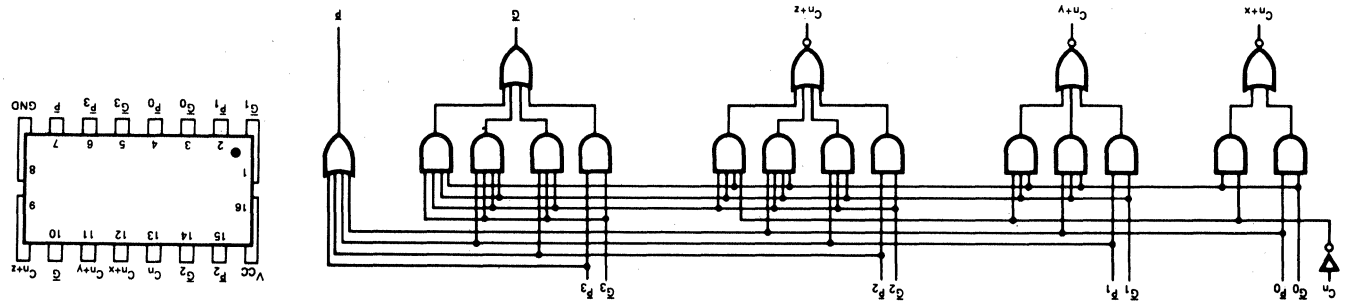
Z90-1



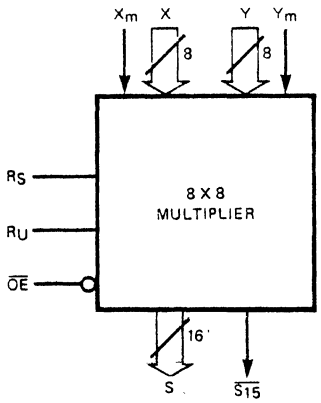
Z90-2

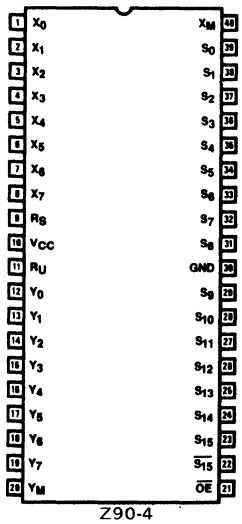


Z90-3

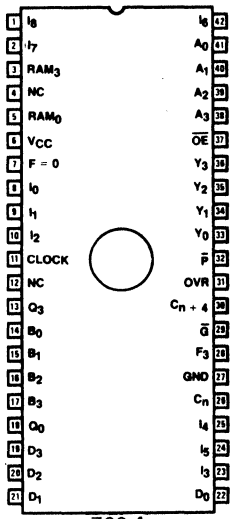


Z90-4



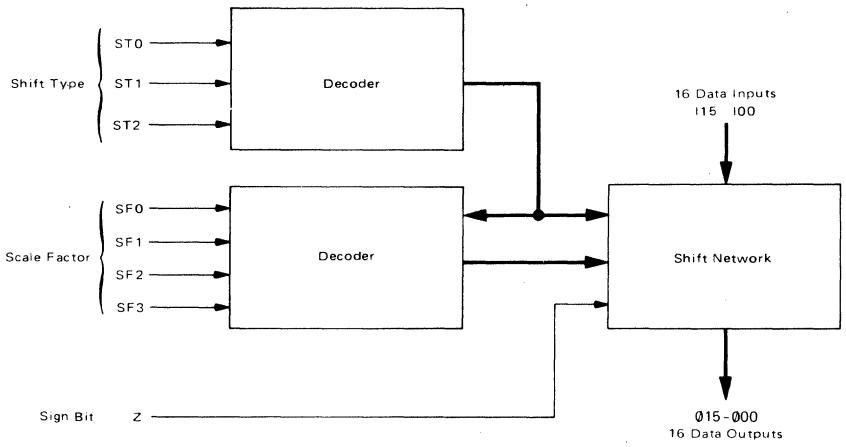


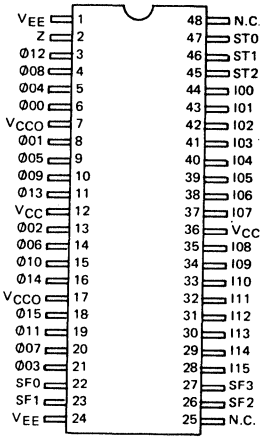
Z90-4



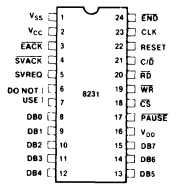
Z90-4a

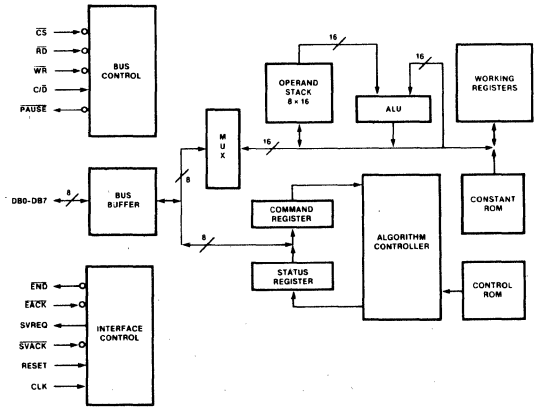
Z90-5



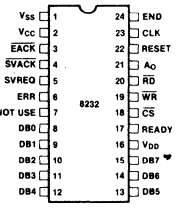


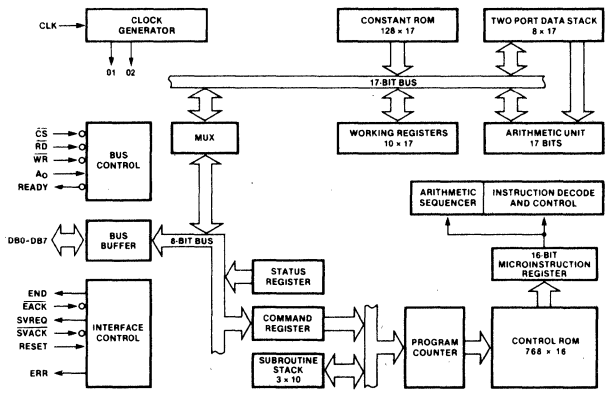
Z90-6



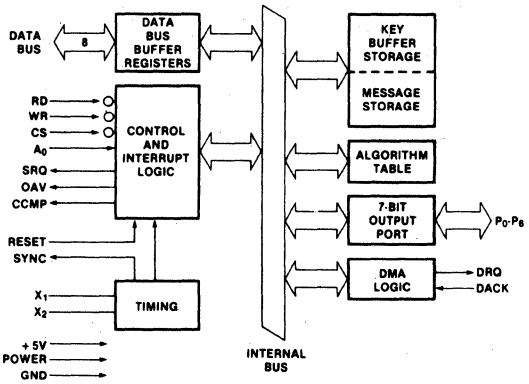


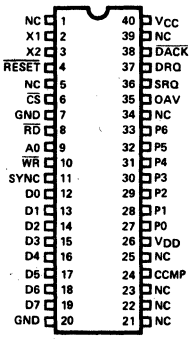
Z90-7



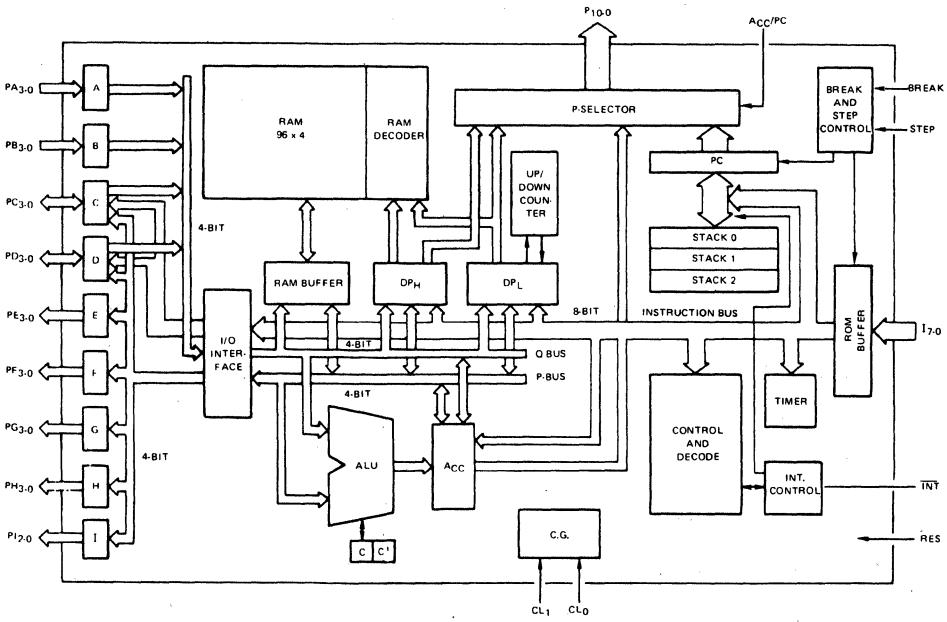


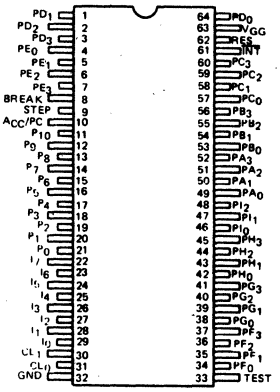
Z92-1



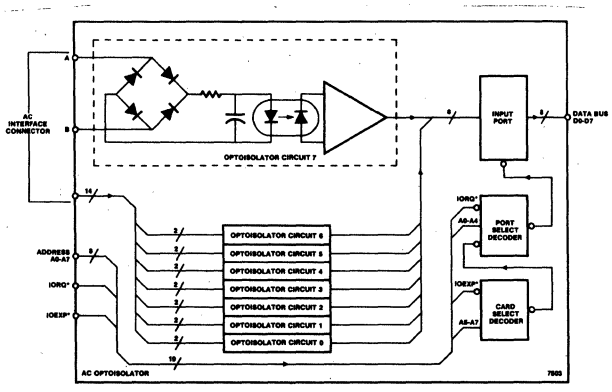


Z92-9

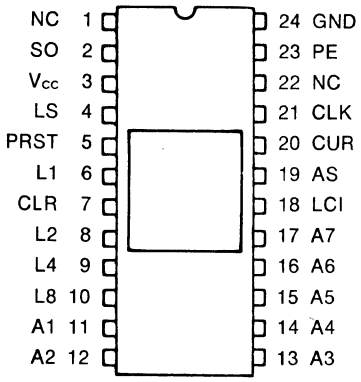


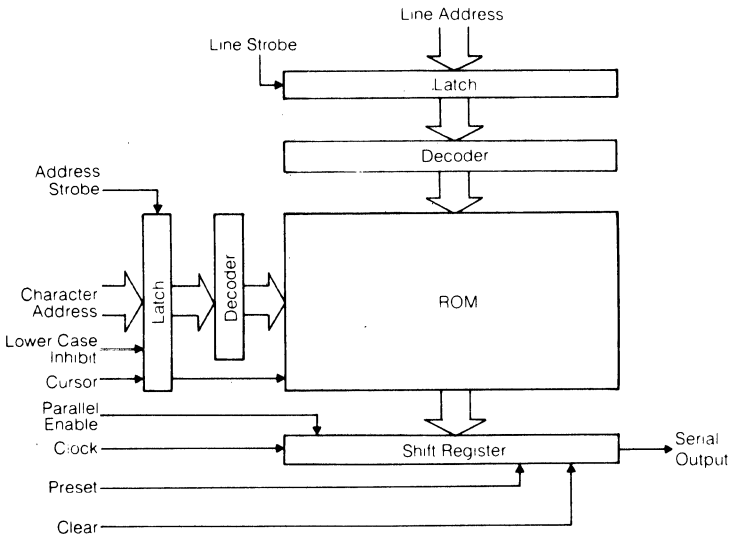


Z92-11

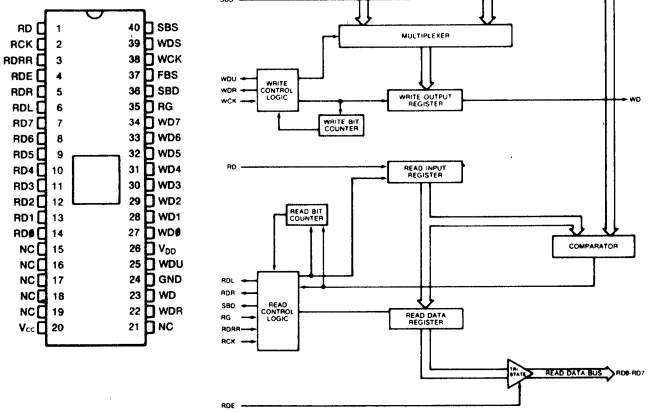


Z92-13

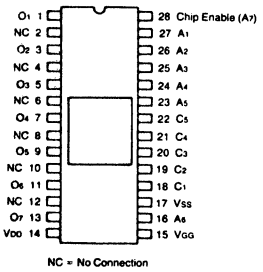




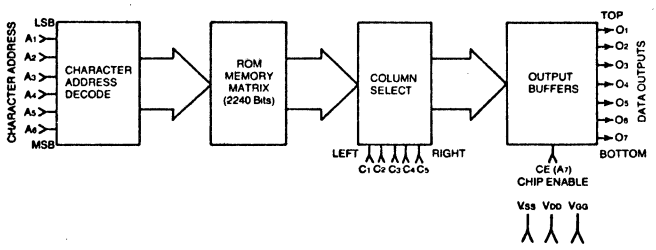
Z92-14



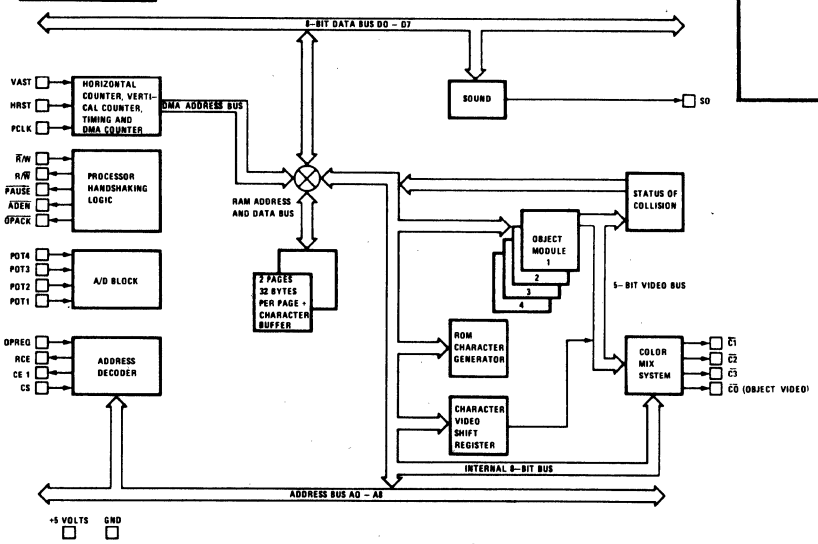
Z92-15



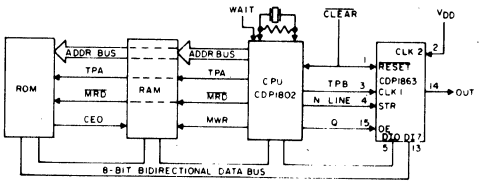
NC = No Connection



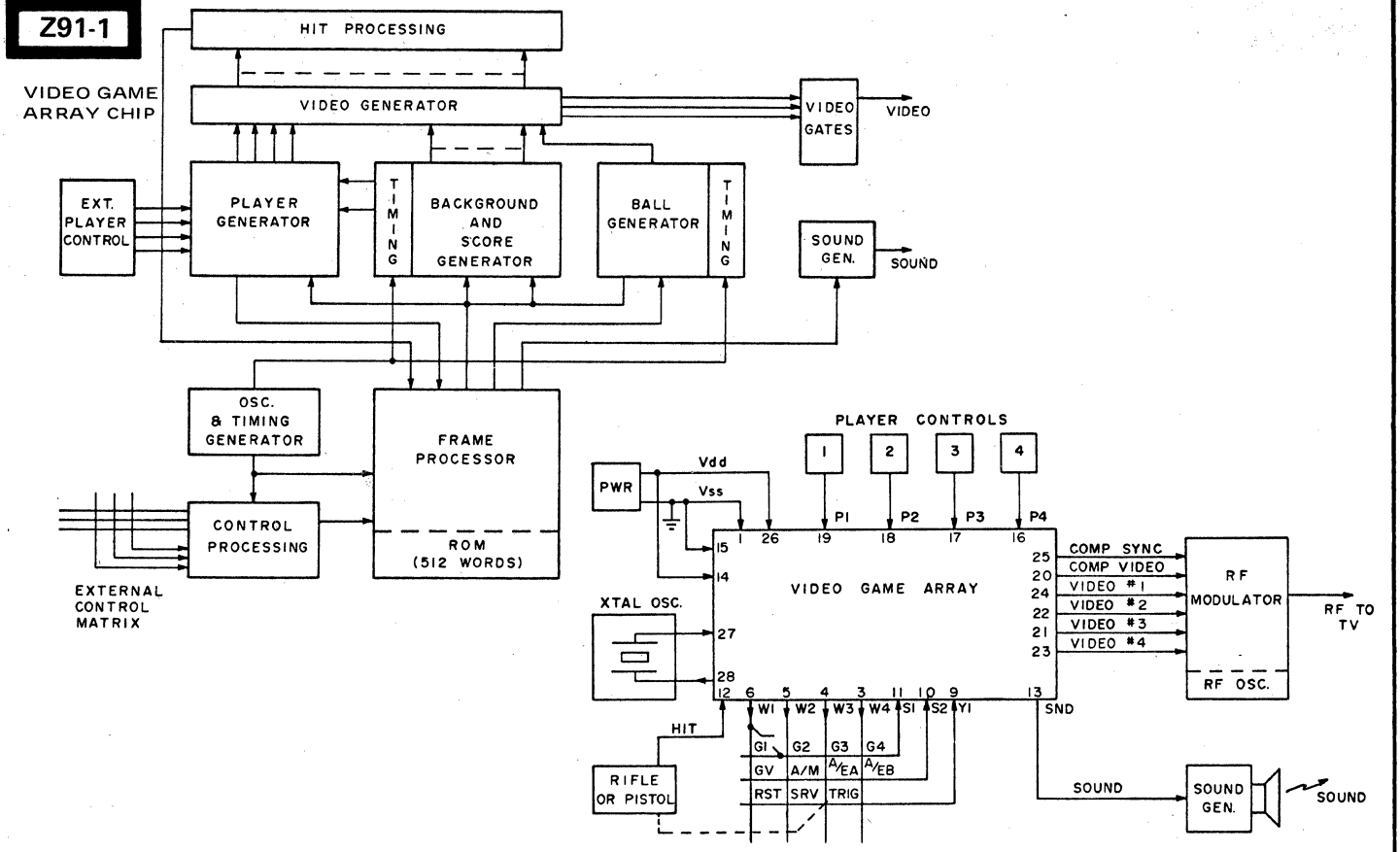
Z92-16



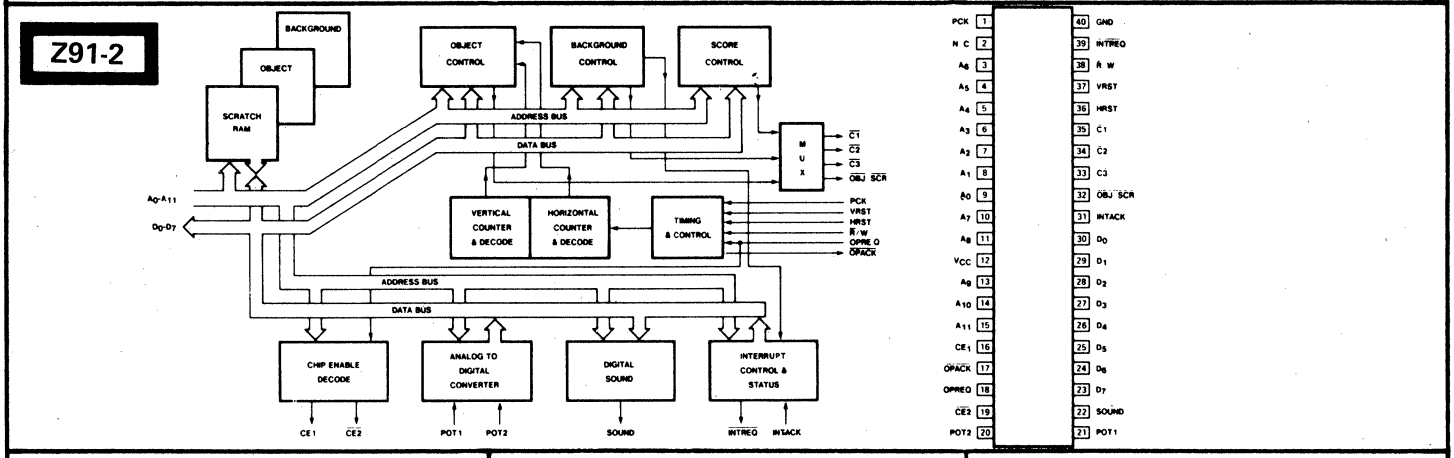
Z92-17



Z91-1


HIT PROCESSING
VIDEO GAME ARRAY CHIP
VIDEO GENERATOR
VIDEO GATES
VIDEO
EXT. PLAYER CONTROL
PLAYER GENERATOR
TIMING
BACKGROUND AND SCORE GENERATOR
BALL GENERATOR
TIMING
SOUND GEN.
SOUND
OSC. & TIMING GENERATOR
FRAME PROCESSOR
CONTROL PROCESSING
ROM (512 WORDS)
EXTERNAL CONTROL MATRIX
PLAYER CONTROLS
PWR
Vdd
Vss
VIDEO GAME ARRAY
XTAL OSC.
COMP SYNC
COMP VIDEO
VIDEO #1
VIDEO #2
VIDEO #3
VIDEO #4
RF MODULATOR
RF OSC.
RF TO TV
HIT
RIFLE OR PISTOL
SND
SOUND
SOUND GEN.
SOUND

Z91-2


BACKGROUND
OBJECT
SCRATCH RAM
OBJECT CONTROL
BACKGROUND CONTROL
SCORE CONTROL
ADDRESS BUS
DATA BUS
MUX
VERTICAL COUNTER & DECODE
HORIZONTAL COUNTER & DECODE
TIMING & CONTROL
CHIP ENABLE DECODE
ANALOG TO DIGITAL CONVERTER
DIGITAL SOUND
INTERRUPT CONTROL & STATUS
GND
INTREQ
VRST
HRST
SOUND
POT1
POT2

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

NOTES: These drawings are referenced in the Microprocessors, Read-Write Memories (RAMS), Read-Only Memories (ROMS), and Interface and Support sections of this D.A.T.A.BOOK in accordance with information supplied by the manufacturers.

These outline drawings are intended as a guide for the user. They should not be used for constructive purposes without first checking with the appropriate manufacturer.

The MO and TO drawings have been reproduced from JEDEC Registration Data Files with the permission of the National Electrical Manufacturer's Association – Electronic Industries Association. JEDEC designations are assigned only to outlines submitted by the JC-11 Committee on Mechanical Standardization. The procedure of assigning and announcing the JEDEC designation constitutes registration.

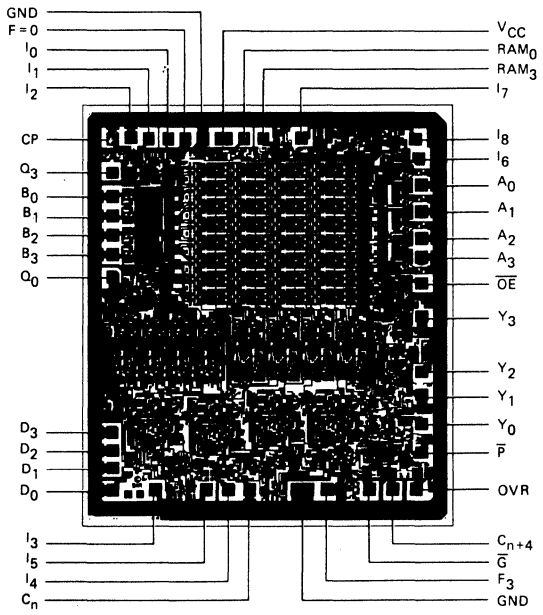
All drawings are in inches except where noted.

OUTLINE DRAWING NO. SIGNIFICANCE

The two-letter prefix associated with these outline drawings describes the basic package style of the device as shown in the table below:

LETTER PREFIX	PACKAGE STYLE
CH	**Chip**
CN	Can
DL	Dual-In-Line
FP	Flat Pack
MD	Modular/Printed Ckt. Bd.
MO	JEDEC Outline

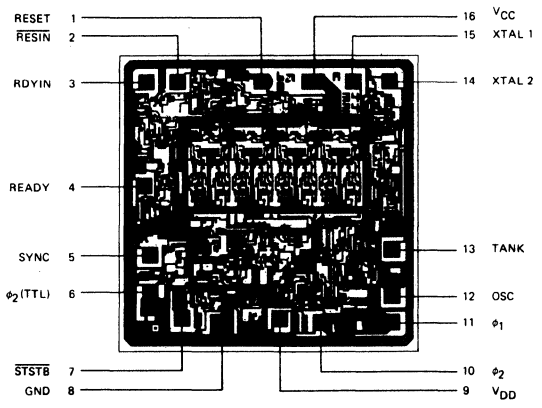
CH1



DIE SIZE 0.132" X 0.149"

CH2

Metallization and Pad Layout



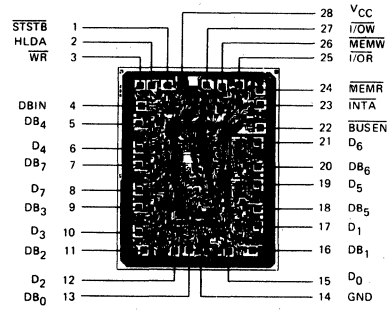
DIE SIZE 0.085" X 0.084"

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

CH3

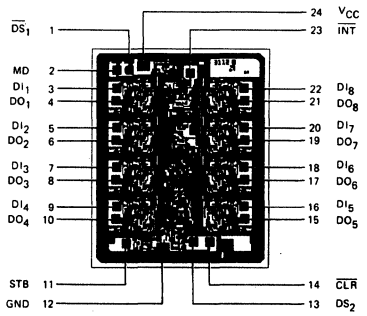
Metallization and Pad Layout



DIE SIZE
0.110" X 0.136"

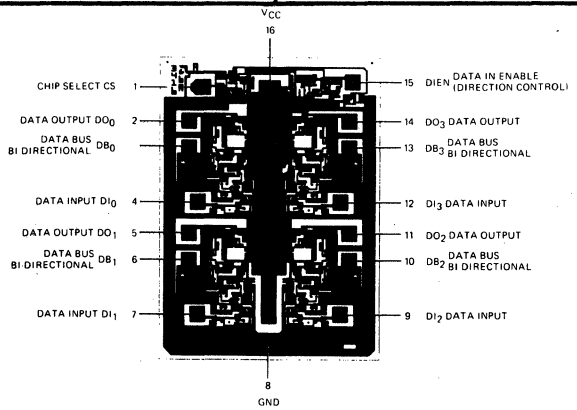
CH4

Metallization and Pad Layout



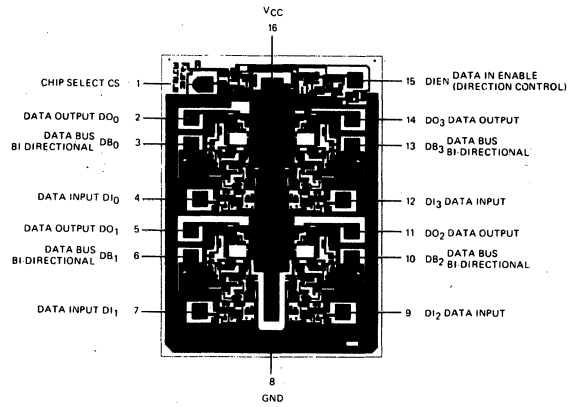
DIE SIZE
0.091" X 0.112"

CH5



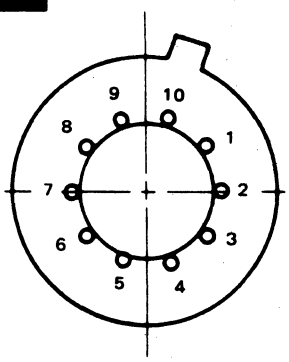
DIE SIZE 0.066" X 0.090"

CH6



DIE SIZE 0.066" X 0.090"

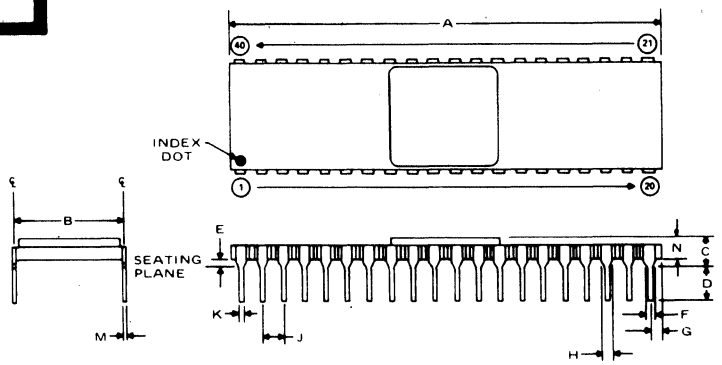
CN1



20. OUTLINE DRAWINGS

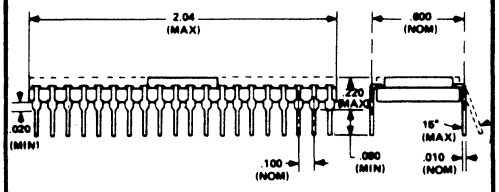
IN DRAWING NUMBER SEQUENCE

DL1

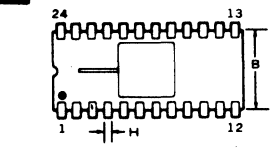


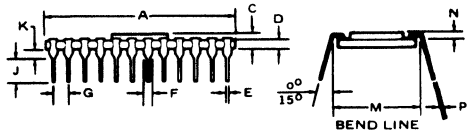
	A	B	C	D	E	F	G	H	J	K	M	N	REMARKS
DL1	2.02 MAX	.590 MAX		.125 MIN	.020 .060		.040 .060	.050	.090 .110	.016 .020	.008 .012	.165 MAX	NOTCH
DL1a	2.02 MAX	.590 .610	.185 MAX	.120 .180	.020 MIN	.032	.030 .070	.040 .060	.100	.015 .021	.010		INDEX DOT
DL1b	1.98 2.03	.580 .610		.125 .150	.030 .070		.030 .065	.045 .060	.090 .110	.015 .021	.008 .012	.080 .120	NO NOTCH OR INDEX DOT
DL1c	1.07 2.03	.585 .615	.230 MAX	.125 MIN	.015 MIN				.090 .110	.014 .022	.007 .013		NOTCH
DL1d	1.98 2.02	.585 .615	.100 .165	.100 .165	.020 .060		.030 .070	.030 .055	.100	.015 .021	.008 .013		NOTCH
DL1e	1.97 2.03	.585 .615	.230 MAX	.125 MIN	.015 MIN				.090 .110	.014 .022	.007 .013		NOTCH
DL1f	1.98 2.02	.580 .620	.095 .155	.125 .175	.025 .050		.030 .070	.050 REF	.100	.017 .023	.008 .012		NOTCH AND INDEX DOT
DL1g	1.97 2.03	.585 .615	.230 MAX	.125 MIN	.015 MIN				.090 .110	.014 .022	.007 .013	.100 TYP	NOTCH
DL1h	1.970 2.030	.565 .595	.230 MAX	.125 MIN	.015 MIN			.040 .070	.090 .110	.014 .022	.007 .013	.120 TYP	NOTCH
DL1j	2.00	.584		.129	.035			.051	.100	.017	.0098	.165	
DL1k	2.10 MAX	.514 .588	.250 MAX	.080 .130	.020 MIN				.090 .100	.015 .023		.230 MAX	
DL1m	1.98 2.02	.560 .600	.130 .160	.160 .180	.030 .060				.090 .110	.015 .023		.100 MAX	
DL1n	2.060 MAX	.590 .610	.200 MAX	.090 MIN	.020 MIN			.040 .065	.100	.015 .020	.008 .012		
DL1p	1.96 2.04	.590 .620	.100 .200	.120 .160	.020 .060			.030 .060	.090 .110	.015 .022	.008 .013		NOTCH
DL1r	2.02 MAX	.590 .610	.185 MAX	.175	.025 MIN		.040 .060	.040 TYP	.100 TYP	.018 TYP	.010 NOM		NOTCH

DL2



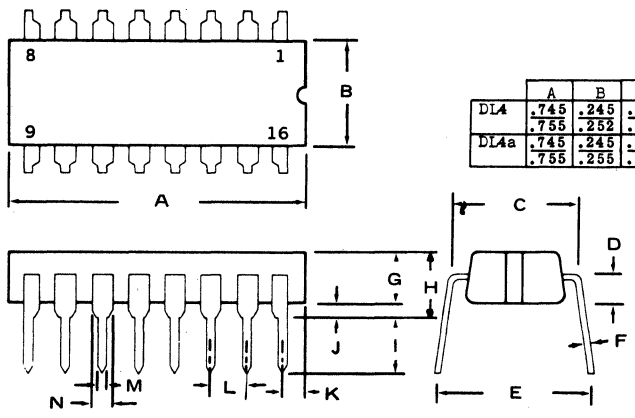
DL3





	A	B	C	D	E	F	G	H	J	K	M	N	P
DL3	1.250 MAX		.200 MAX				.100		.090 MIN	.020 MIN	.600		.010
DL3a	1.175 1.300	.490 .550	.125 MAX	.050 .120	.015 .022	.032	.090 .110	.043 .060	.100 .150	.040	.590 .610	.050 MAX	.008 .012
DL3b	1.100 1.250	.595 .625	.115 MAX		.017 .023		.090 .110		.120 .140	.025 TYP	.490 .580	.040 TYP	.008 .012
DL3c	1.310 MAX	.480 .580	.180 MAX		.015 .020		.100	.040 .065	.090 MIN	.020 MIN	.590 .610		.008 .012

DL4

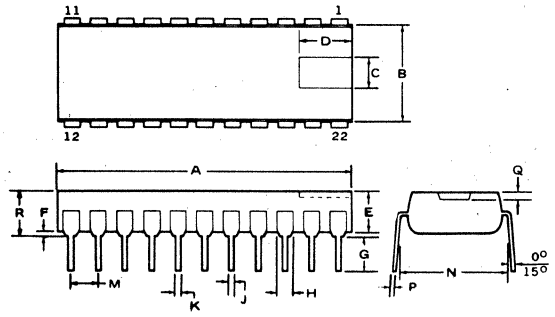


	A	B	C	D	E	F	G	H	I	J	K	L	M	N
DL4	.745 .755	.245 .252	.290 .310	.057 .068	.325 .375	.010 .015	.115 .125		.120 .135	.015 .035	.020 .030	.090 .110	.015 .021	.044 .052
DL4a	.745 .755	.245 .255	.290 .310		.325 .375	.009 .011		.200 MAX	.125 MIN	.020 NOM		.090 .110	.018 .022	

20. OUTLINE DRAWINGS

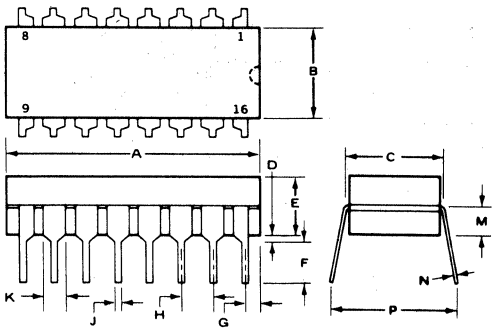
IN DRAWING NUMBER SEQUENCE

DL5



	A	B	C	D	E	F	G	H	J	K	M	N	P	Q	R
DL5	1.130 MAX						.090 MIN				.100	.400			.200 MAX
DL5a	1.090 1.110	.340 .360	.125	.200	.140 .160	.020 MIN.	.100 .150	.060	.032	.016 .023	.100	.400	.010	.025 REF	
DL5b	1.080 1.110	.380 .400			.054 .080	.020 .060	.100 .150	.043 .060		.016 .023	.100	.390 .410	.010		.200 MAX
DL5c	1.120 MAX	.360			.165		.100 MIN		.020		.100	.400	.007 .013		.200 MAX
DL5d	1.102 MAX	.334				.019 MIN	.100 MIN	.055		.015 .023		.400	.007 .013		.204 MAX
DL5e	1.070	.380				.020 MIN	.100 MIN	.052		.015 .022	.090 .110	.400	.008 .015		.220 MAX
DL5f	1.180 1.120	.330 .370			.150 .200	.015 .060	.125 .160	.055 .065	.015 .020		.090 .110	.410 .480	.009 .011	.015 .045	

DL6

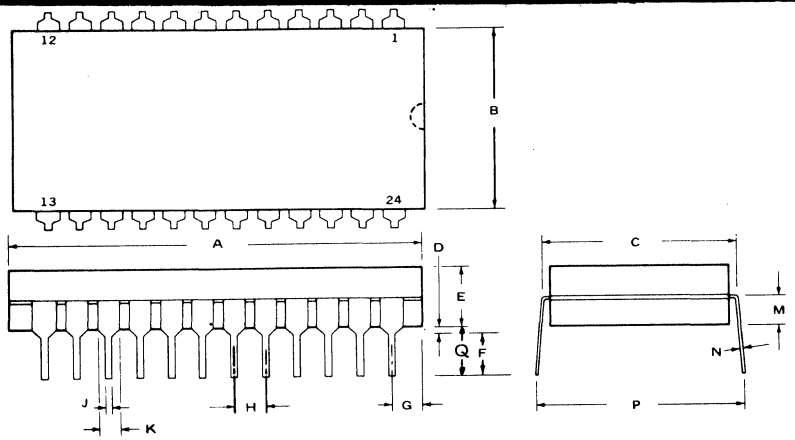


	A	B	C	D	E	F	G	H	J	K	M	N	P	REMARKS
DL6	.755 .785	.280 MAX	.290 .315	.020 .040	.145 .175	.125 .165	.015 .050	.090 .110	.015 .023	.070 MAX	.090	.008 .014	.325 .395	
DL6a	.735 .830	.245 .295	.290 .325	.020 .060	.160 MAX	.100 .150	.010 .065	.090 .110		.045 .070	.055 .160	.008 .012	.290 .410	NOTCH
DL6b	.750 .770	.285 .291	.320	.020	.150 .199	.100 .165	.015 .045	.090 .110	.016 .020	.045 .065		.009 .011	.385 .415	NOTCH
DL6c	.750 .780	.245 .275	.290 .310	.020 .040	.160 .200	.125 .160	.020 .045	.100	.015 .020	.055 .065		.008 .012		NOTCH
DL6d	.755 .785	.245 .300	.290 .310	.020 MIN	.180	.130 MIN	.015 .050	.100	.015 .023			.008 .014		NOTCH
DL6e	.750 .785	.265 .291	.290 .320	.015 .080	.120 .185	.125 MIN	.010 MIN	.090 .110				.009 .011	.380	NOTCH
DL6f	.784 MAX	.250	.300	.019 MIN	.180 MAX	.100		.100	.014 .022	.059		.008 .014		NOTCH
DL6g	.763 MAX	.251	.300	.019 MIN	.160 MAX	.100 MIN		.100	.016 .024	.051		.008 .014		NOTCH
DL6h	.750 .785	.245 .271	.290 .310	.015 MIN	.185 MAX	.125 MIN		.090 .110	.016 .020	.045 .065		.009 .011	.375 NOM	NOTCH
DL6j	.750 .785	.265 .291	.290 .310	.015 MIN	.185 MAX	.125 MIN		.090 .110	.016 .020	.045 .065		.009 .011	.375 NOM	NOTCH
DL6k	.740 .760	.240 .260	.290 .310	.015 NOM	.185 MAX	.100 .150		.090 .110	.016 .020	.045 .065		.009 .011	.375 NOM	NOTCH
DL6l	.750 .785	.245 .280	.290 .320	.020 .050		.125 .160	.015 .060	.100	.015 .020	.035 .065		.008 .012		NOTCH
DL6m	.759	.248	.300	.019 MIN	.181	.100 MIN		.090 .110	.015 .022	.051		.008 .015		NOTCH
DL6n	.753 .767	.241 .249	.307 .317		.148								.350 .380	NOTCH
DL6p	.755 .790	.265 .300	.290 .320	.015 .035	.175 MAX	.125 .165	.070 MAX	.090 .110	.016 .020	.055 .065		.008 .012		
DL6q	.785 MAX	.291 MAX	.290 .320	.020 .070	.180 MAX	.125 MIN	.050 MAX	.090 .110	.016 .020	.055 .065		.008 .012	.360 .410	NOTCH
DL6r	.745 .775	.240 .260		.015 .060	.150 .200	.125 .150	.010 .040	.090 .110	.015 .020	.055 .065		.009 .011	.310 .385	NOTCH
DL6s	.745 .785	.240 .310	.290 .320	.015 .060	.130 .200	.125 .150	.005	.090 .110	.016 .020	.050 .070		.009 .011		NOTCH

20. OUTLINE DRAWINGS

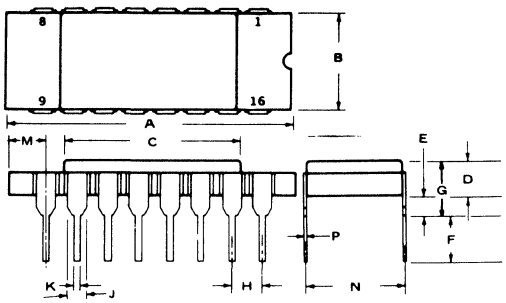
IN DRAWING NUMBER SEQUENCE

DL7



	A	B	C	D	E	F	G	H	J	K	M	N	P	Q	REMARKS
DL7	1.235 1.290	.560 MAX	.590 .610	.020 .055	.150 .200	.120 .140	.060 .100	.090 .110	.015 .023	.076 MAX	.100	.008 .014	.640 .690		
DL7a	1.200 1.300	.550 .650	.550 .650	.020 .050	.170 MAX	.100 .150		.090 .110	.015 .023	.045 .070	.070 .110	.008 .012	.600 .730		NOTCH
DL7b	1.235 1.265	.540 .560	.580 .600	.020 .040		.120 .140	.070 .080	.095 .105	.014 .020	.040 .060		.008 .012			PIN IDENTIFICATION AND CHAMFERED EDGES
DL7c	1.245 1.255	.525 .535	.585 .595	.020 NOM	.220 MAX	.125 MIN		.090 .110	.018 .022			.009 .011	.625 .675		NOTCH
DL7d	1.235 1.290	.510 .540	.590 .620	.020 .060	.260 MAX	.125 MIN		.090 .110	.015 .023			.009 .011	.700 NOM		NOTCH
DL7e	1.225 1.290	.500 .545	.590 .610	.020 MIN	.180 MAX	.125 MIN		.090 .110	.015 .023	.030 .070		.008 .015	.650		DOT
DL7f	1.235 1.290	.515 .560	.590 .610		.150 .200		.060 .100	.100 TYP	.016 .020	.070 MAX			.685 .715	.125 .155	NOTCH
DL7g	1.200 MAX	.380 TYP	.400 TYP	.020 MIN	.140 .190	.115 .135		.090 .110		.045 .065		.009 .011	.500 MAX		NOTCH
DL7h	1.230 1.270	.510 .530	.625 MAX	.015 MIN	.140 .180	.100 MIN		.090 .110	.040 .065	.014 .023		.008 .015	.600 .700		NOTCH
DL7i	1.230 1.290	.515 .575	.600 MON	.025 .063	.125 .210	.100 .200	.040 .100	.090 .110	.027 .037	.045 .065		.009 .011	.750 MAX		
DL7j	1.235 1.290	.560 MAX	.590 .620	.020 .055	.130 .180	.125 .165	.080 .098	.090 .110	.015 .023	.030 .070	.100	.008 .014			NOTCH
DL7k	1.290 MAX	.515 .525	.590 .620	.020 .070	.130 .180	.125 MIN	.060 .100	.090 .110	.016 .020	.050 .060		.008 .012	.660 .710		NOTCH
DL7m	1.240 1.270	.515 .540		.015 .060	.170 .215	.125 .160		.090 .110	.015 .020			.009 .011	.585 .700		NOTCH
DL7n	1.230 1.280	.510 .545	.600 .620	.015 .060	.150 .225	.120 .150		.090 .110	.016 .020			.009 .011			NOTCH

DL8

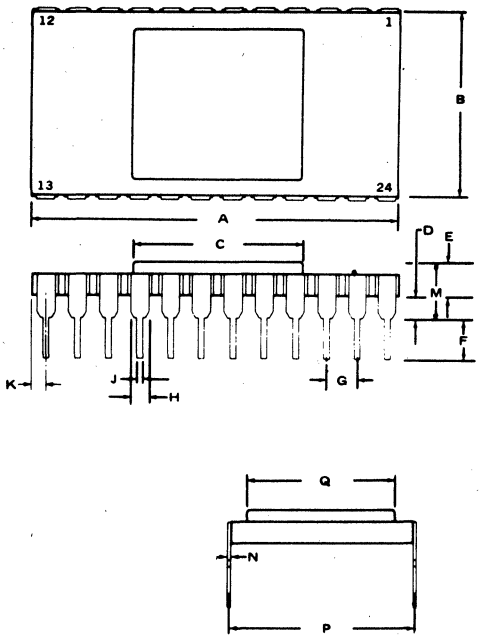


	A	B	C	D	E	F	G	H	J	K	M	N	P	REMARKS
DL8	.740 .830	.280 .310	.420 .470	.080 .120	.030 .060	.125 .150		.090 .110	.045 .060	.015 .021	.020 .065	.290 .320	.008 .012	NOTCH
DL8a	.840 MAX	.299 .310			.020 MIN	.120 .180	.185 MAX	.100	.040 .060	.015 .021	.030 .070	.290 .310	.010	INDEX DOT
DL8b	.808 MAX	.294 MAX			.015 MIN	.130 TYP	.194 MAX	.095 .105				.300 TYP	.008 .012	NOTCH
DL8c	.740 .870	.275 .310			.020 MIN	.125 MIN	.200 MAX	.090 .110	.040 .070	.016 .023		.290 .320	.008 .015	NOTCH AND DOT
DL8d	.740 .810	.280 .300	.370 .475		.020 .050	.130 .200	.160 MAX	.090 .110	.045 .065	.015 .020		.290 .310	.008 .012	NOTCH AND DOT
DL8e	.790 .810	.282 .294		.085 .105	.025 .045	.130		.100	.054	.016 .020		.340	.009 .011	

20. OUTLINE DRAWINGS

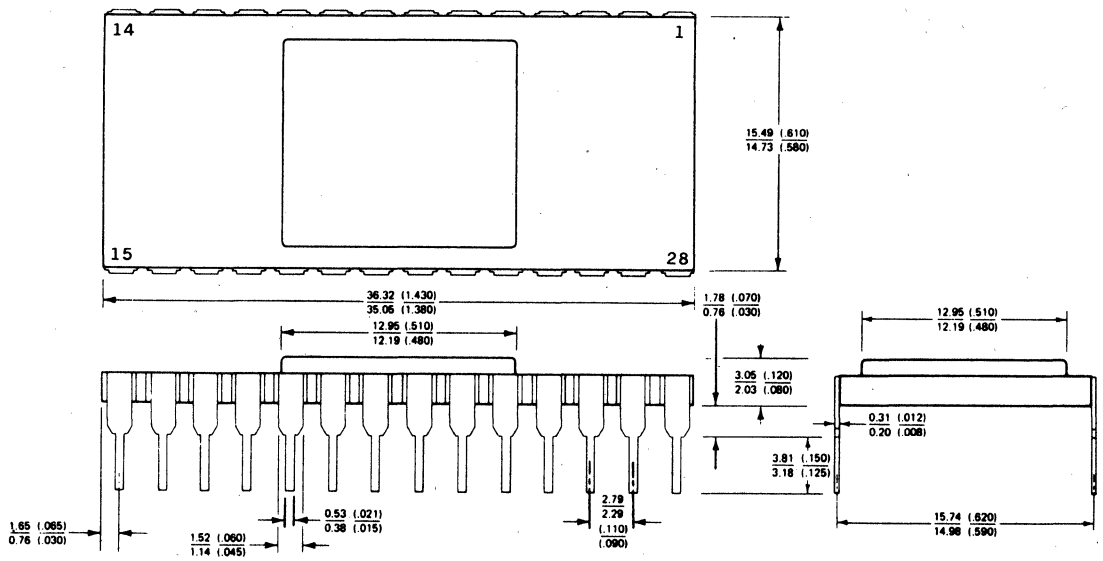
IN DRAWING NUMBER SEQUENCE

DL9



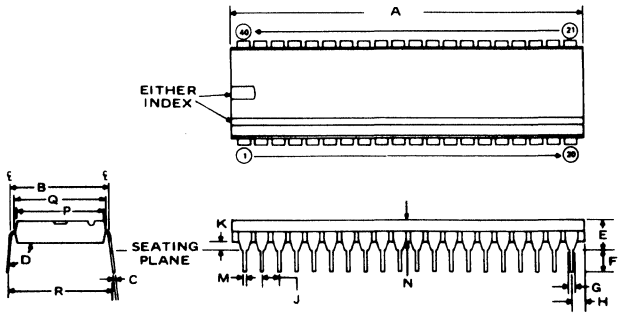
	A	B	C	D	E	F	G	H	J	K	M	N	P	Q	REMARKS
DL9	1.19 1.23	.580 .610	.480 .510	.030 .070	.080 .120	.125 .150	.090 .110	.045 .060	.015 .021	.030 .065		.006 .012	.590 .620	.480 .510	
DL9a	1.29 MAX	.590 .610		.020 MIN		.120 .180	.100	.040 .060	.015 .021	.040 .070	.185 MAX	.010	.590 .610		
DL9b	1.18 1.22	.585 .615		.020 .060		.100 .165	.100	.030 .055	.015 .021	.030 .070	.120 .165	.008 .012	.585 .605		NOTCH
DL9c	1.230 MAX	.580 .620		.030 .060		.125 MIN	.090 .110		.016 .022		.210 MAX	.008 .015	.590 .630		NOTCH AND DOT
DL9d	1.230 MAX	.580 .620		.030 .060		.125 MIN	.090 .110		.016 .022		.200 MAX	.008 .015	.590 .630		NOTCH AND DOT
DL9e	1.290 MAX	.590 MAX		.020 .060		.125 MIN	.090 .110	.050 TYP	.016 .020	.040 .060		.008 .012	.600 TYP		NOTCH
DL9f	1.185 2.015	.568 .588		.050	.090	.120		.040 TYP	.012 .024	.050 TYP	.140	.009 .011	.600 .650		NOTCH AND DOT
DL9g	1.178	.586		.019 MIN		.100 MIN	.090 .110	.050	.015 .022		.200 MAX	.008 .015	.600		NOTCH
DL9h	1.310 MAX	.575 .595		.020 MIN		.090 MIN	.100		.015 .020		.200 MAX	.008 .012	.590 .610		DOT
DL9i	1.230 MAX	.580 .610	.450 .530	.020 .070	.010 .120	.125 .150	.090 .110	.045 .065	.015 .023			.008 .015		.450 .530	

DL10



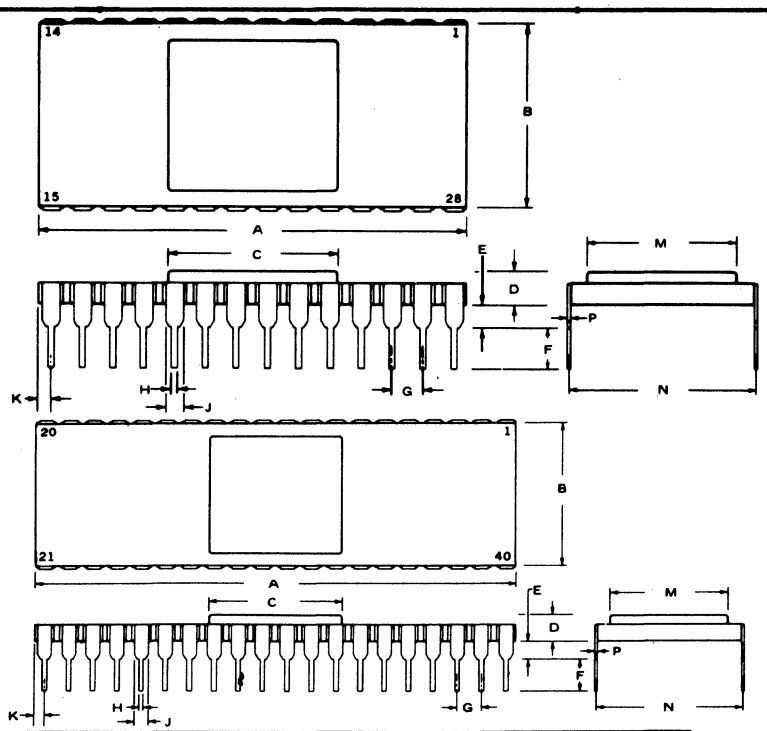
MM(IN)

DL11



	A	B	C	D	E	F	G	H	J	K	M	N	P	Q	R	REMARKS
DL11	2.090 MAX	.590 .610	.008 .014	90 105	.200 MAX	.125 MIN	.033 MIN	.055 .095	.100	.020 MIN	.015 .021	.150 MAX	.500 MAX	.600	.625	EITHER INDEX
DL11a	2.070 MAX	.600	.010		.200 MAX	.120 MIN			.100	.020 MIN	.018	.150 MAX	.500	.600	.625	TAB ONLY
DL11b	2.04	.551	.0098		.155	.129	.051		.100	.025	.018				.600	NOTCH
DL11c	2.028 MAX	.600	.008 .014		.225 MAX	.100 MIN		.014	.096 .104	.019	.015 .023	.206 MAX	.520			NOTCH RAD .059
DL11d	2.040 2.070	.625 MAX	.008 .015		.200 MAX	.100 MIN	.032 TYP		.090 .110	.015 MIN	.014 .023			.530 .550	.600 .700	NOTCH
DL11e	2.030 2.070	.625 MAX	.008 .015		.230 MAX	.100 MIN	.032 TYP		.090 .110	.015 MIN	.014 .023			.510 .530	.600 .700	NOTCH
DL11f	2.070 MAX	.600 .620	.009 .015			.125 MIN		.060 .090	.100	.020 MIN	.015 .021	.125 .135			.610 .650	EITHER INDEX
DL11g	2.080 2.100	.600	.009 .011		.160 .248	.100 .165	.027 .037		.100 TYP	.025 .063	.016 .020	.135 .185	.515 .575		.650 TYP	NOTCH
DL11h	2.035 2.065	.600				.125 MIN	.030 TYP	.075	.100 .101	.065 .075		.145 .155	.535 .545		.645 .675	NOTCH
DL11i	2.050	.600	.010			.115 .130	.018	.075	.090 .110	.020 MIN	.018	.150	.540		.670 REF	NOTCH
DL11j	2.047			90 105	.188	.130			.100	.037	.020	.151		.539	.600	
DL11k	2.060 MAX	.590 .610	.008 .012		.220	.090 MIN			.100	.020 MIN	.015 .020	.200 MAX	.515 .580			NOTCH
DL11m	2.050	.600	.010		.170	.115 .130		.075	.090 .110	.020 MIN	.018			.540	.670	NOTCH
DL11n	2.010 MAX	.600 .620	.009 .015			.125 MIN	.060 .090		.090 .110	.020 MIN	.015 .021	.125 .135	.545 .555		.610 .650	NOTCH

DL12

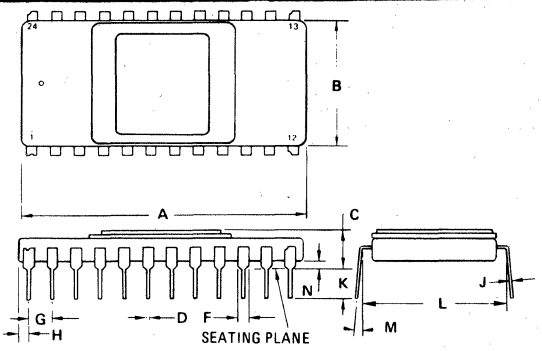


	PIN NO.	A	B	C	D	E	F	G	H	J	K	M	N	P	REMARKS
DL12	28	1.38 1.43	.580 .610	.480 .510	.080 .120	.030 .070	.125 .150	.090 .110	.015 .021	.045 .060	.030 .065	.480 .510	.590 .620	.008 .012	
	40	1.98 2.03	.580 .610	.480 .510	.080 .120	.030 .070	.125 .150	.090 .110	.015 .021	.045 .060	.030 .065	.480 .510	.590 .620	.008 .012	
DL12a	28	1.40 MAX	.514 .588		.210 MAX	.020 MIN	.100 .150	.090 .100	.015 .023				.590 .710		
	40	2.10 MAX	.514 .588		.210 MAX	.020 MIN	.100 .150	.090 .100	.015 .023				.590 .710		
DL12b	28	1.38 1.42			.035 .120	.025 .050	.125 .175	.100	.017 .023		.030 .070		.580 .620	.008 .012	LONGITUDINAL STRIPE
	40	1.98 2.02			.045 .130	.025 .050	.125 .175	.100			.030 .070		.580 .620	.008 .012	LONGITUDINAL STRIPE

20. OUTLINE DRAWINGS

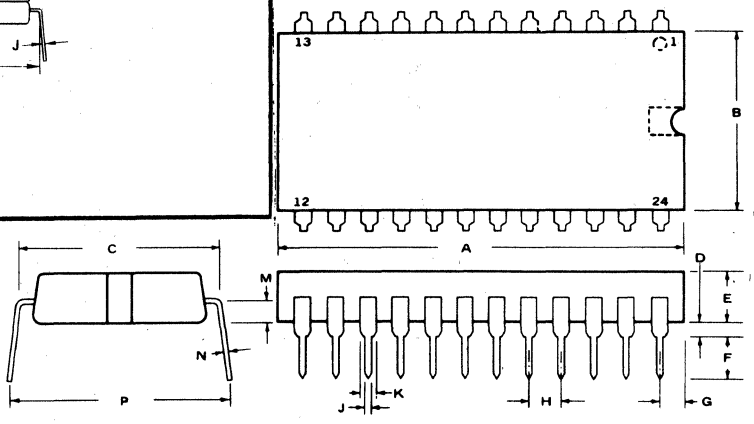
IN DRAWING NUMBER SEQUENCE

DL13



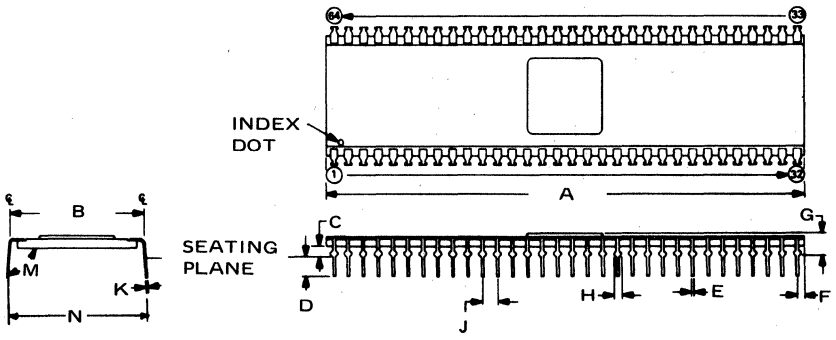
	A	B	C	D	F	G	H	J	K	L	M	N
DL13	1.215 MAX		.220 MAX			.100		.010	.090	.600	15° MAX	.020 MIN
DL13a	1.155 / 1.215	.500 / .560	.120 / .155	.015 / .020	.035 / .055	.100	.035 / .055	.008 / .012	.115 / .145	.585 / .625	15° MAX	.020 / .045

DL14



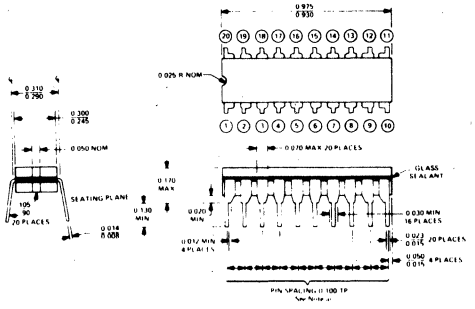
	A	B	C	D	E	F	G	H	J	K	M	N	P	REMARKS
DL14	1.240 / 1.255	.545 / .555	.590 / .610	.020 / .045	.145 / .155	.120 / .135	.065 / .085	.090 / .110	.015 / .021	.044 / .052	.065 / .075	.010 / .015	.625 / .675	NOTCH ONLY
DL14a	1.23 / 1.25	.530 / .550	.590 / .610	.020 MIN	.145 / .165	.100 / .150	.070	.090 / .110	.016 / .023	.060		.008 / .012		SQUARE NOTCH AND INDEX DOT
DL14b	1.310	.550	.590 / .610	.020 MIN	.180 MAX	.125 MIN	.095 MAX	.100	.015 / .021	.033 MIN		.008 / .014		SQUARE NOTCH
DL14c	1.230 / 1.260	.530 / .550	.625 MAX	.015 MIN	.150 / .160	.100 MIN		.090 / .110	.014 / .023	.040 / .065		.008 / .015	.600 / .700	RECT.NOTCH

DL15



	A	B	C	D	E	F	G	H	J	K	M	N	REMARKS
DL15	3.170 / 3.230	.880 / .920	.020 MIN	.125 MIN	.014 / .020	.040 / .080	.185 MAX	.050 TYP	.100 TYP	.010 TYP	90° / 105°		
DL15a	3.201	.800	.020	.118	.017		.185	.050 TYP	.100 TYP		90° / 105°	.900	

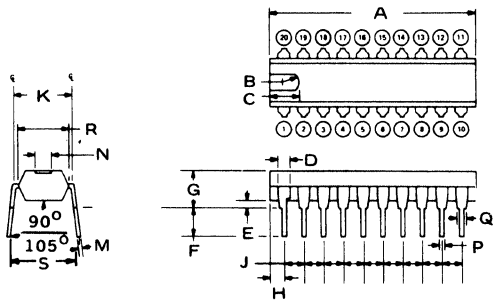
DL16



20. OUTLINE DRAWINGS

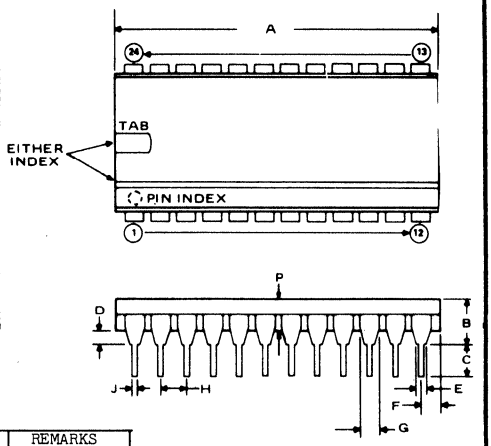
IN DRAWING NUMBER SEQUENCE

DL17

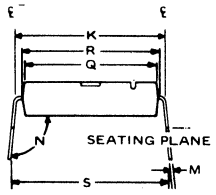


	A	B	C	D	E	F	G	H	J	K	M	N	P	Q	R	S
DL17	1.070 MAX	.093	.160	.070 MAX	.020 MIN	.125 .155	.200 MAX	.075 MAX	.100	.290 .310	.008 .014	.080 NOM	.015 .021	.033 MIN	.240 .260	
DL17a	1.015 1.025					.125 MIN	.200 MAX		.090 .110	.290 .310			.018 .022	.045 .065		.325 .375
DL17b	.942 .958				.030		.175		.100 TYP	.312 .316		.050	.018	.032	.265 .271	.353 .383

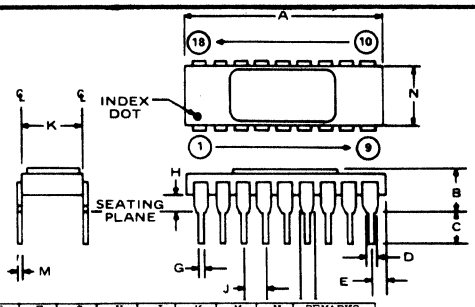
DL18



	A	B	C	D	E	F	G	H	J	K	M	N	P	Q	R	S	REMARKS
DL18	1.290 MAX	.200 MAX	.125 MIN	.020 MIN	.033 MIN	.055 .095	.060	.100	.015 .021	.590 .610	.008 .014	90° 105°					EITHER INDEX
DL18a	1.260 MAX		.115 MIN	.020 MIN	.030	.080 MAX	.060	.100	.018	.600	.009 .011		.200 MAX	.500	.555 MAX	.625	EITHER OR BOTH INDEXES
DL18b	1.30 MAX	.230 MAX	.130 MIN	.020				.100	.020	.600	.008 .014				.520		NOTCH
DL18c	1.32 MAX	.200 MAX	.100 MIN			.110 MAX		.100	.018	.600	.008 .014				.530		NOTCH
DL18d	1.200 MAX		.115 .135	.020 MIN	.027 .037		.045 .065	.090 .110	.016 .020	.400 TYP	.009 .011				.360	.500 MAX	NOTCH
DL18e	1.299 MAX	.225 MAX	.100 MIN	.019 MIN			.059	.100	.015 .023		.008 .013				.519	.600	NOTCH
DL18f	1.31 MAX	.200 MAX	.125 MIN	.020 MIN	.033 MIN	.095 MAX		.100 TYP	.015 .021	.590 .610	.008 .014	90° 105°			.550 TYP		NOTCH
DL18g	1.270 MAX	.170 .180	.125 MIN	.015 MIN		.060 .090		.100	.015 .021	.600 .620	.009 .015				.535 .545	.610 .650	NOTCH

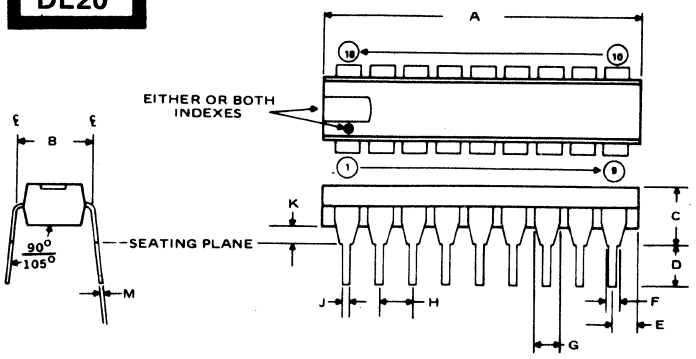


DL19



	A	B	C	D	E	F	G	H	J	K	M	N	REMARKS
DL19	.910 MAX	.185 MAX	.120 .160	.032 NOM	.030 .070	.040 .060	.015 .021	.020 MIN	.100 TYP	.290 .310	.010 NOM		INDEX DOT
DL19a	.900 TYP	.200 MAX	.125 TYP	.032 REF		.043 .060	.016 .023	.040 TYP		.300 TYP	.008 .012	.285 TYP	NOTCH
DL19b	.890 .915	.200 MAX	.100 .150	.032 REF		.043 .060	.016 .023	.020 .060	.090 .110	.290 .310	.008 .012	.275 .295	INDEX DOT AND NOTCH
DL19c	.860 .865	.180 MAX	.130			.060 TYP	.020 TYP	.040 TYP		.235	.010 TYP	.250	INDEX DOT AND NOTCH
DL19d	.880 .920	.160 MAX	.130 .170			.045 .065	.015 .020	.020 .050	.090 .110	.290 .310	.008 .012		NOTCH

DL20

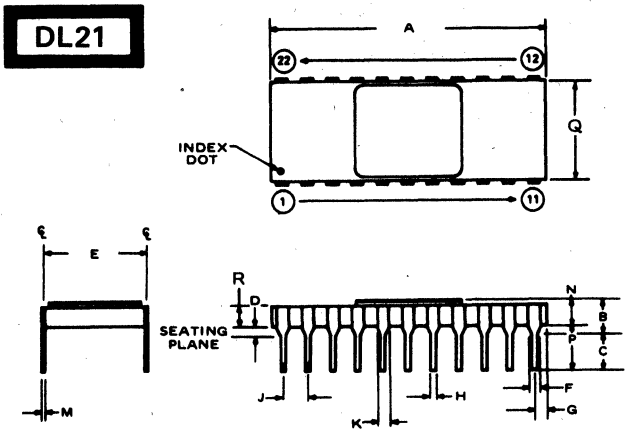


	A	B	C	D	E	F	G	H	J	K	M
DL20	.920 MAX	.290 .310	.200 MAX	.125 MIN	.030 .070	.033 MIN	.060	.100	.015 .021	.020 MIN	.008 .014
DL20a	.905 .925	.290 MIN	.200 MAX	.100 .150	.057 REF	.032 REF	.045 .065	.090 .110	.016 .024	.040 MAX	.009 .012
DL20b	.832 .928	.290 MAX	.190 MAX	.130 MIN		.040 TYP	.060 TYP	.100 TYP	.018 TYP	.030	.008 .012
DL20c	.905 MAX	.300	.179	.100 MIN			.051	.100	.016 .024	.019	.008 .014
DL20d	.880 .920	.300	.165	.125			.060	.100 TYP	.015 .021	.030	.008 .012

20. OUTLINE DRAWINGS

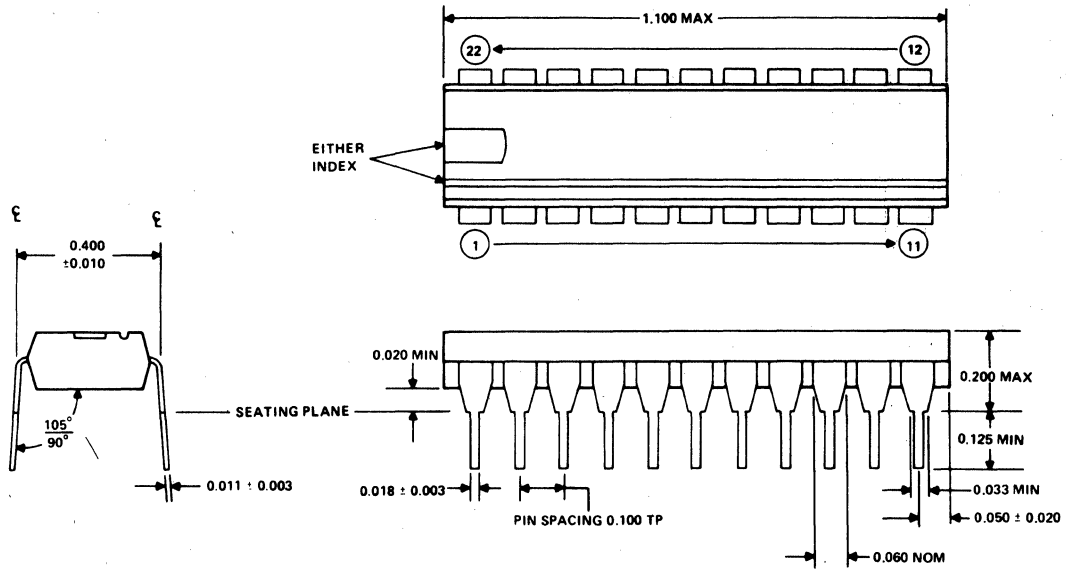
IN DRAWING NUMBER SEQUENCE

DL21

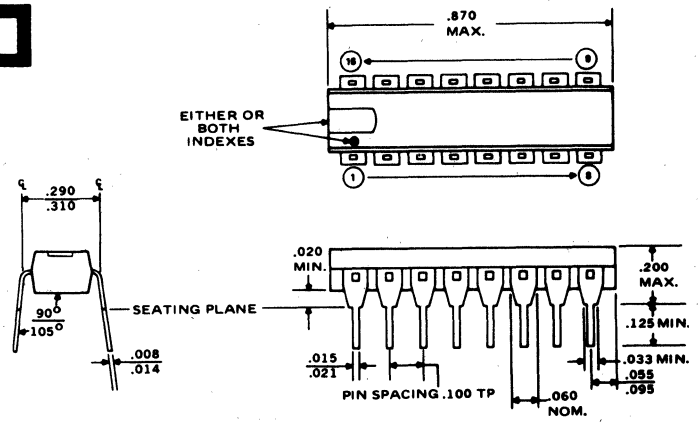


	A	B	C	D	E	F	G	H	J	K	M	N	P	Q	R
DL21	1.100 MAX	.185	.120 .160	.020 MIN	.390 .410	.032 NOM	.030 .070	.015 .021	.100	.040 .060	.010 NOM				
DL21a	1.070 TYP		.155 .160		.400 TYP			.018 TYP	.100		.011 MAX				
DL21b	1.150 TYP		.125 .145	.030 MIN	.390 TYP			.018 TYP	.100		.011 MAX				
DL21c	1.080 1.100	.050	.125	.038	.385					.040 REF	.006 .012				
DL21d	1.135 1.165			.025 .050	.380 .420		.030 .070	.017 .023	.100	.040 REF	.008 .012	.085 .145	.125 .175		
DL21e	1.065 1.100	.085 .145	.125 .175	.025 .050	.380 .420		.030 .070	.017 .023	.100	.040 REF	.008 .012				
DL21f	1.060 1.110	.200 MAX	.100 .150	.020 MIN	.390 .410			.016 .023	.100	.043 .060	.010			.380 .400	.054 .080

DL22



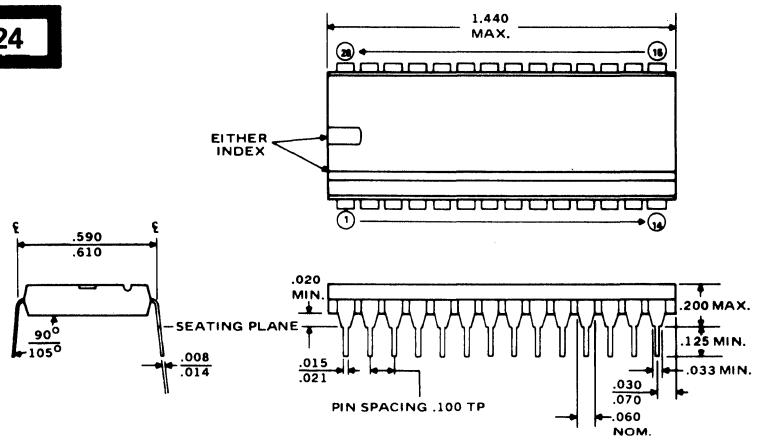
DL23



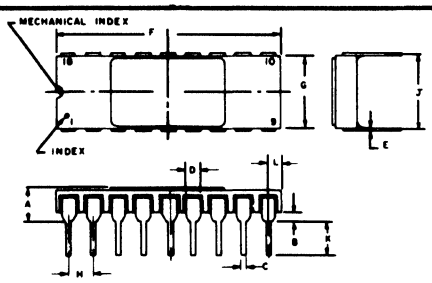
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

DL24

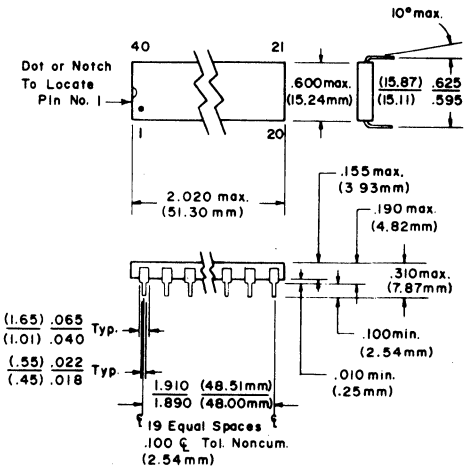


DL25

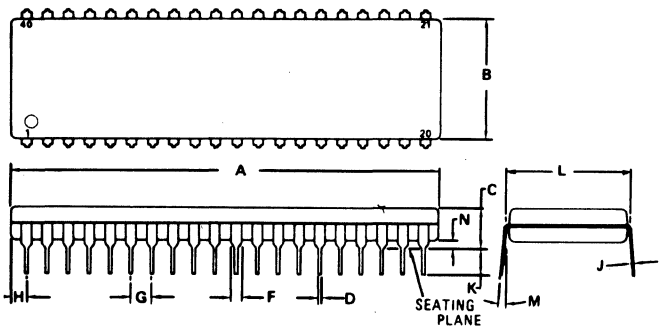


	A	B	C	D	E	F	G	H	J	K	L
DL25	.200 MAX	.020 .045	.015 .021	.054	.008 .012	.890 .915	.280 .300	.100	.300	.125 .150	.035 .065
DL25a	.120 .140	.025 .035	.018 .020	.051 .057	.009 .011	.890 .920		.090 .110	.300 .320	.125 .135	
DL25b	.110 .150	.025 .045	.016 .020	.054 TYP	.010 TYP	.890 .910	.282 .294	.090 .110	.300 .350	.120 .140	
DL25c	.095 .230	.015 .060	.015 .021	.040 .065	.008 .015	.870 .910	.250 .310	.090 .110	.290 .350	.110 .150	

DL26

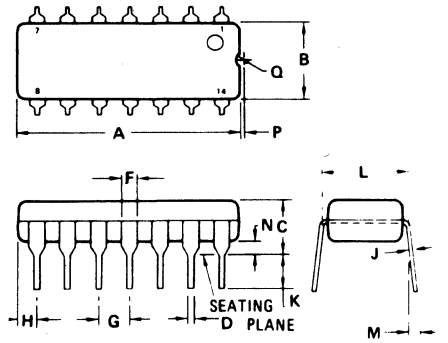


DL27



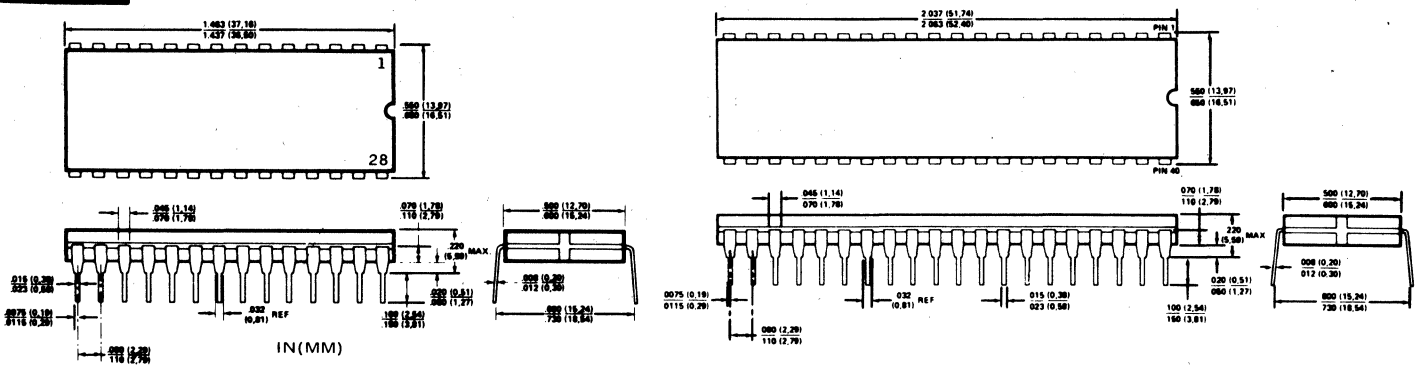
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.68	4.19	0.145	0.165
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

DL28

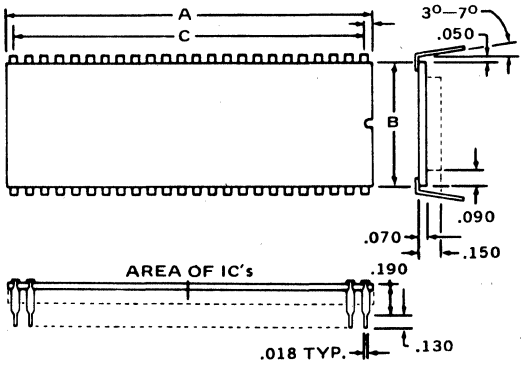


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

DL29

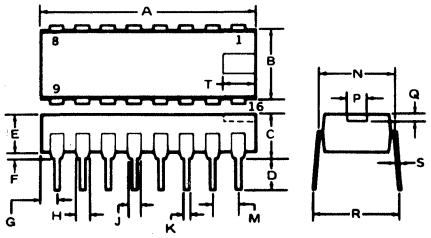


DL32



	A	B	C
DL32	2.40	.800	24 LEADS 100 CENTERS 2.300
DL32a	2.50		25 LEAD 100 CENTERS 2.400

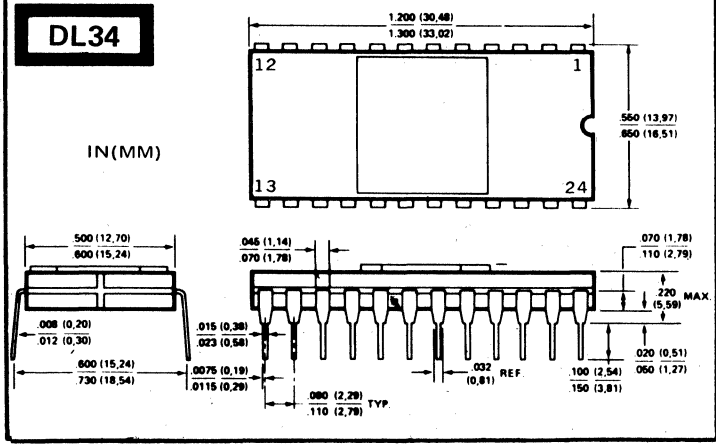
DL33



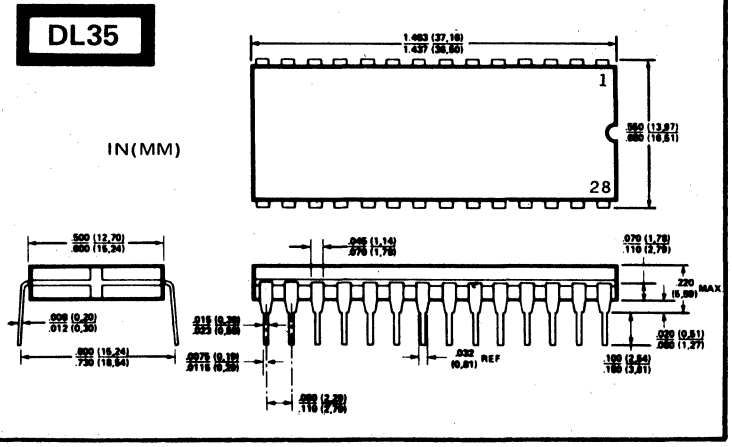
DL33

	A	B	C	D	E	F	G	H	J	K	M	N	P	Q	R	S	T
DL33	.745 .855	.245 .255	.200 MAX	.100 MIN	.125 .155	.020 MIN	.025 .063	.045 .065	.032	.015 .023	.090 .110	.290 .310	.075	.025 REF	.290 .410	.008 .012	.060 .125 REF
DL33a	.870 MAX	.245 .255		.125 MIN	.125 .135	.020 MIN	.060 .090			.015 .021	.100	.300 .320		.030 MAX	.310 .350	.009 .015	
DL33b	.760 .765	.250	.180 MAX	.130		.040 TYP	.020	.060 TYP		.020 TYP		.235			.300	.010	
DL33c	.745 .755	.245 .255	.200 MAX	.125 MIN		.020				.018 .022	.090 .110	.290 .310			.325 .375	.009 .011	
DL33d	.750 .865	.240 .260	.200 MAX	.100 .150		.015 .050		.045 .065		.016 .020	.090 .110	.300 TYP			.375 TYP	.008 .012	
DL33e	.870 MAX	.260 MAX	.200 MAX	.130 TYP		.020 MIN				.200	.095 .105	.300 TYP			.300 TYP		

DL34



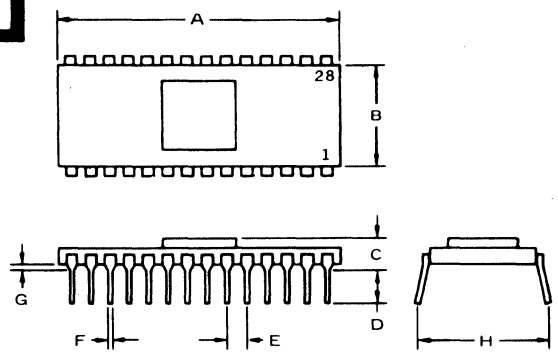
DL35



20. OUTLINE DRAWINGS

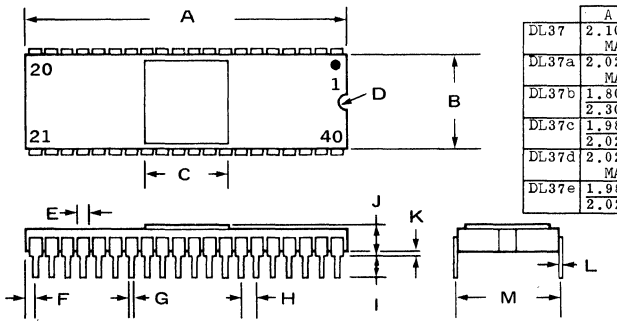
IN DRAWING NUMBER SEQUENCE

DL36



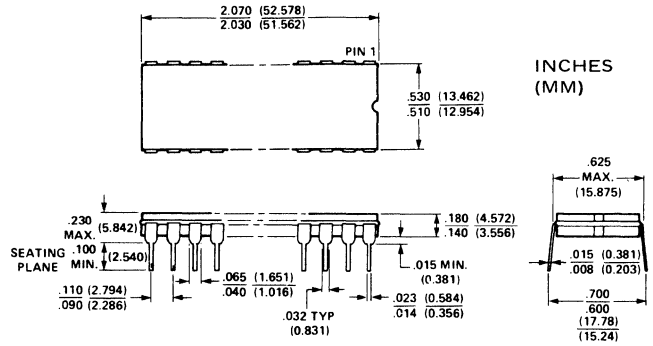
	A	B	C	D	E	F	G	H
DL36	1.40 MAX	.514 .588	.230 MAX	.100 .150	.090 .100	.015 .023	.020 MIN	.590 .710
DL36a	1.425 MAX	.510 .550	.150 MAX	.050 .160	.095 .105	.015 .020	.020 .050	.590 .610
DL36b	1.415 MAX	.590	.165 MAX	.125 MIN	.100 TYP	.017 TYP	.035 MIN	.600 TYP
DL36c	1.42 MAX	.600 MAX	.190 MAX	.100 MIN	.100	.018 .022	.035 MAX	.595 .625
DL36d	1.385 1.415	.568 .588	.140	.120		.016 .020	.050	.600 .650
DL36e	1.386 1.425	.510 .590	.150 MAX	.050 .160	.095 .105	.015 .021	.020 .050	.590 .610
DL36f	1.600	.530	.150	.150	.100	.018 .022	.030	.590 .610
DL36g	1.420 MAX	.598 MAX	.165 MAX	.125 MIN	.090 .110	.015 .023	.020 .060	.600

DL37

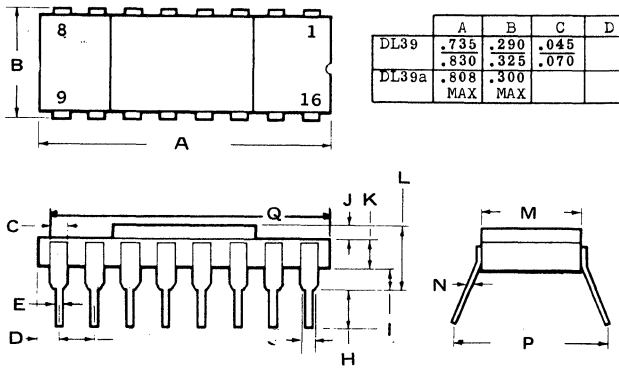


	A	B	C	D	E	F	G	H	I	J	K	L	M	REMARKS
DL37	2.100 MAX	.514 .588					.015 .023	.090 .110	.100 .150	.230 MAX	.020 MIN	.008 .012	.590 .710	NO DOT OR NOTCH
DL37a	2.020 MAX	.590 MAX	.520 SQUARE	.032 RAD	.050 TYP	.040 .060	.016 .020	.090 .110	.125 MIN	.165 MAX	.020 .060	.008 .012	.600 REF	DOT AND NOTCH
DL37b	1.800 2.300	.565 .595			.040 .070		.014 .022	.090 .110	.125 MIN	.230 MAX	.015 MIN	.007 .013	.585 .615	NOTCH ONLY
DL37c	1.980 2.020	.565 .590	.480 .500	.025 RAD	.040 .045	.040 .060	.016 .020	.090 .110	.125 .175	.110 .160	.040 .060	.009 .011	.675 MAX	NOTCH ONLY
DL37d	2.020 MAX	.590 MAX	.520 SQUARE	.032 RAD	.050 TYP	.040 .060	.016 .020	.090 .110	.125 MIN	.230 MAX	.020 .060	.008 .012	.600 REF	NOTCH ONLY
DL37e	1.980 2.020						.016 .020	.100 TYP	.150	.130 .150	.040 .060	.009 .011	.590 .610	NOTCH ONLY

DL38



DL39

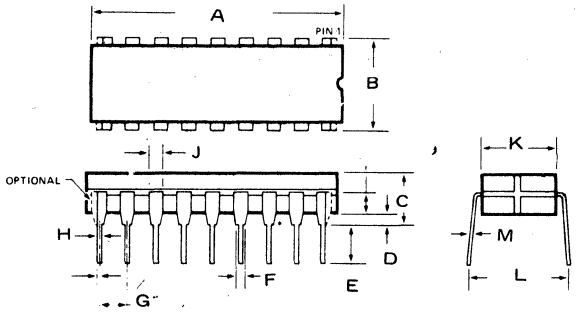


	A	B	C	D	E	F	G	H	I	J	K	L	M	N	P	Q
DL39	.735 .830	.290 .325	.045 .070		.015 .023	.095 .105	.032 REF	.100 .150	.020 .060	.050 MAX	.055 .125	.200 MAX	.245 .295	.002 .010	.290 .410	
DL39a	.808 MAX	.300 MAX				.095 .105		.130 TYP	.015 MIN	.050 MAX		.194 MAX	.294 MAX	.008 .012		.695 .705

20. OUTLINE DRAWINGS

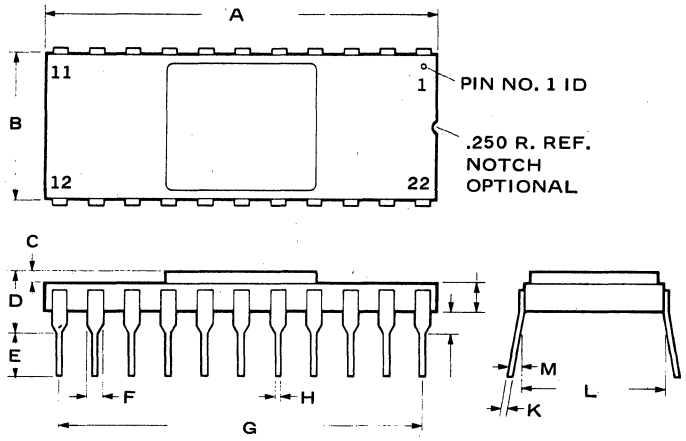
IN DRAWING NUMBER SEQUENCE

DL40



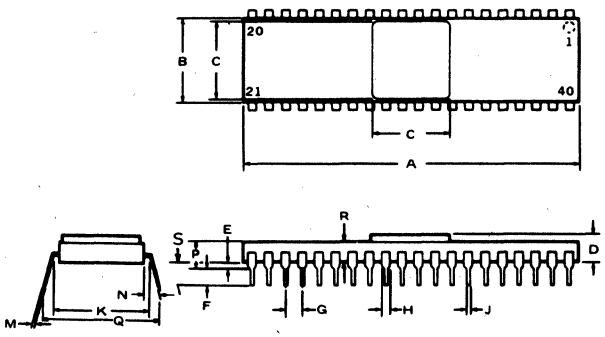
	A	B	C	D	E	F	G	H	J	K	L	M
DL40	.850 .930	.290 .325	.220 MAX	.020 .050	.100 .150	.032 MAX	.090 .110	.016 .023	.045 .070	.240 .295	.290 .410	.008 .012
DL40a	.880 .910	.290 .320	.160 .205	.015 .030	.125 .145		.090 .110	.015 .023	.055 .065	.285 .295	.325 .385	.008 .012
DL40b	.890	.300	.200 MAX	.019 MIN	.100 MIN		.090 .110	.015 .022	.052	.288		.008 .015
DL40c	.915 MAX	.290 .320	.200 MAX	.020 .070	.125 MIN		.090 .110	.015 .021		.290 MAX	.360 .410	.008 .012
DL40d	.870 .910	.310	.175	.020 MIN	.140		.100 TYP	.015 .021	.060	.290		.007 .013

DL41



	A	B	C	D	E	F	G	H	I	J	K	L	M	REMARKS
DL41	1.09 1.11	.380 .400	.010 .040	.200 MAX	.100 .150	.043 .060	.100	.016 .023	.020 .050	.054 .080	.010	.390 .410	0° 20°	PIN#1 ID, NOTCH OPTIONAL
DL41a	1.06 1.11	.380 .400		.200 MAX	.100 .150	.043 .060		.016 .023		.054 .080	.010	.390 .410	N.A.	NOTCH ONLY

DL42

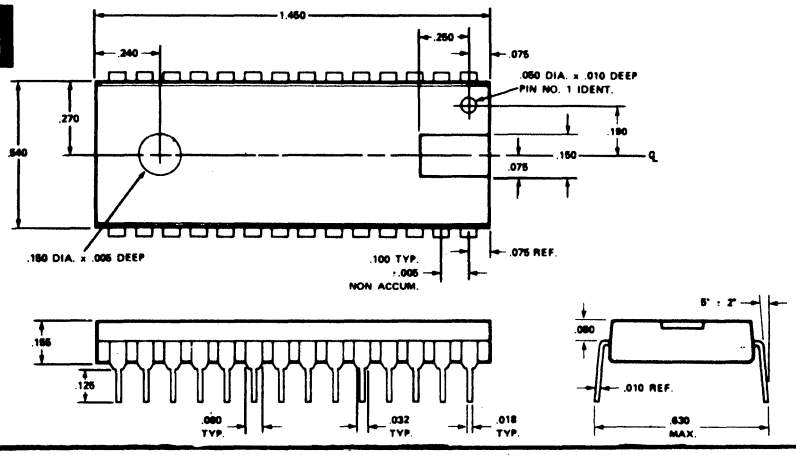


	A	B	C	D	E	F	G	H	J	K	M	N	P	Q	R	S	REMARKS
DL42	1.990 2.020	.500	.470	.190 MAX	.020 MIN	.100 .150	.100	.050	.020	.590 .610	.008 .012	15° MAX					
DL42a	2.015 MAX	.535	.527		.040 MIN	.125 MIN	.100	.045	.017	.600	.008 .011		.190 MAX	.625			INDEX DOT
DL42b	1.97	.500	.460			.188	.100	.030	.015 .019	.600	.009 .012			.600	.070		INDEX TAB ON BOTH SIDES AND INDEX DOT
DL42c	1.975 2.025	.500					.100 TYP	.040 .055	.016 .020	.590 .610	.008 .017		.180 MAX			.140 MIN	INDEX DOT
DL42d	1.980 2.020	.568 .588	.506	.090	.025	.120			.016 .020	.590 .610	.009 .011						NOTCH AND DOT
DL42e	1.975 2.025	.490 .500					.100	.040 .055	.015 .020	.590 .610	.008 .017		.180 MAX			.120 MIN	INDEX TAB ON BOTH SIDES AND INDEX DOT
DL42f	2.040 2.070	.530 .550		.165 .175	.015 MIN	.100 MIN	.090 .110	.040 .065	.014 .023	.625 MAX	.008 .015		.200 MAX	.600 .700			N AND DOT
DL42g	2.060 MAX	.590 .610	.480 .580	.200 MAX	.020 MIN	.090 MIN	.100 TYP		.015 .020		.008 .012		.220				
DL42h	1.950 2.050	.570 .600			.035 .055	.125 .180	.090 .110	.030 .050	.016 .020	.590 .610	.008 .012	15°	.175			.150	
DL42J	2.060	.575		.200	.020	.090	.100	.040	.015	.590	.008	15					INDEX DOT

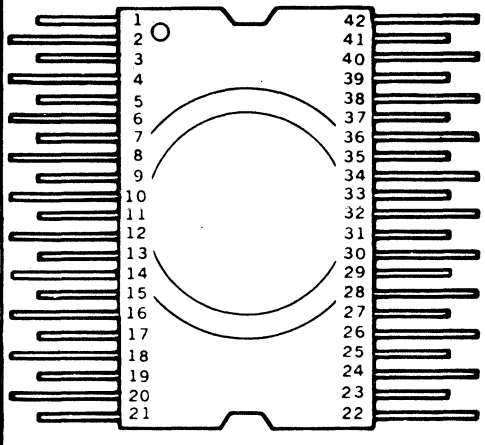
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

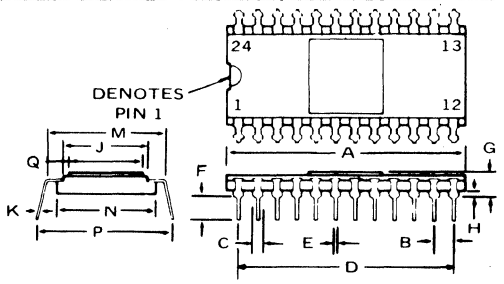
DL43



DL44

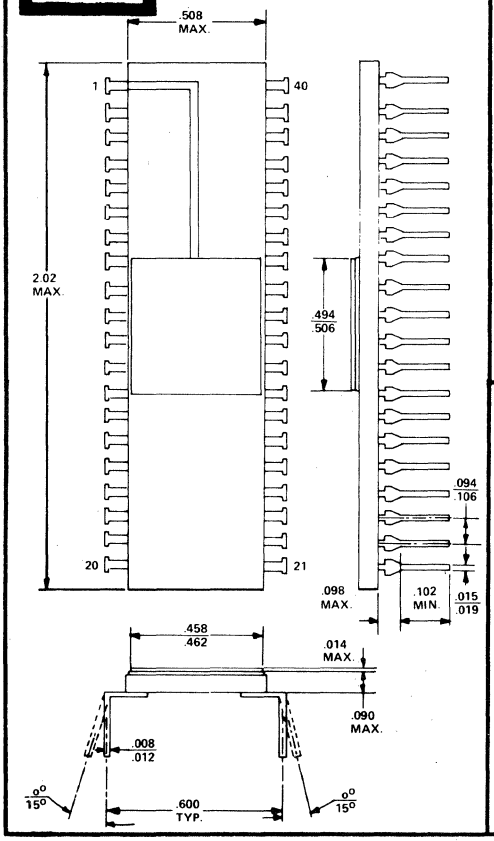


DL45

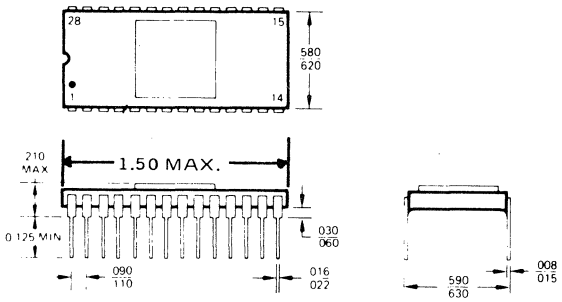


	A	B	C	D	E	F	G	H	J	K	M	N	P	Q
DL45	1.250 MAX	.100 TYP	.050 TYP		.017 TYP	.125 MIN	.145 MAX	.040	.420 TYP	.010 .012	.600 TYP	.500 TYP	.650 TYP	.380 TYP
DL45a	.1280 MAX	.100	.047 MIN	1.10	.020 .024	.126 MIN	.205 MAX	.040 MIN		.008 .016	.600	.550		
DL45b	1.280 MAX	.100	.050	1.10	.020 .024	.126 MIN	.205 MAX	.040		.008 .016	.600	.550		

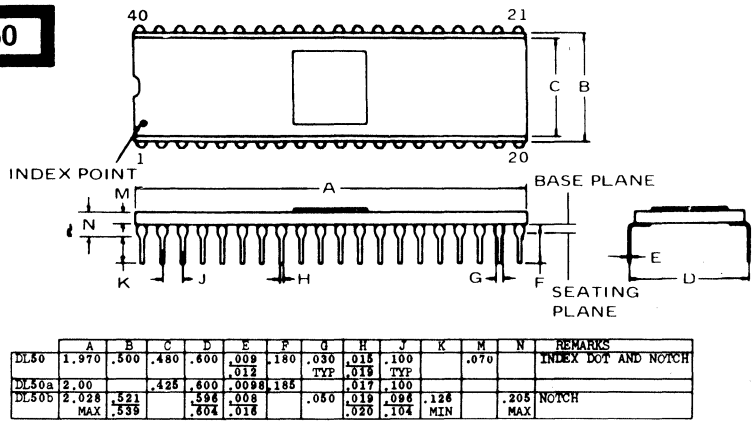
DL48



DL49



DL50

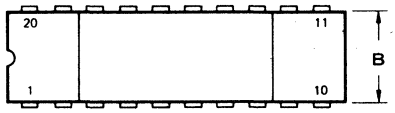


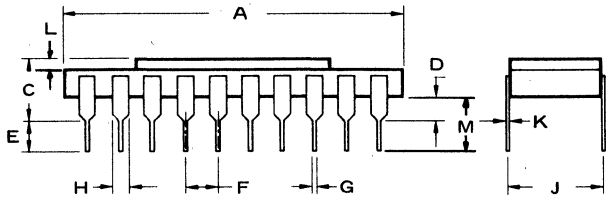
	A	B	C	D	E	F	G	H	J	K	M	N	REMARKS
DL50	1.970	.500	.480	.600	.009 .012	.180	.030 TYP	.015 .019	.100 TYP		.070		INDEX DOT AND NOTCH
DL50a	2.00		.425	.600	.0098	.185		.017	.100				
DL50b	2.028 MAX	.521 .539		.596 .604	.008 .016		.050	.019 .020	.096 .104	.128 MIN		.205 MAX	NOTCH

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

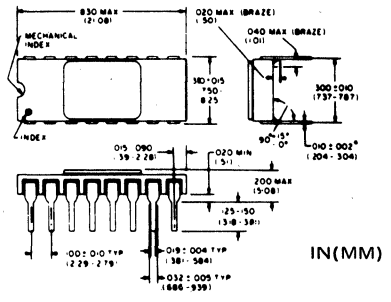
DL51



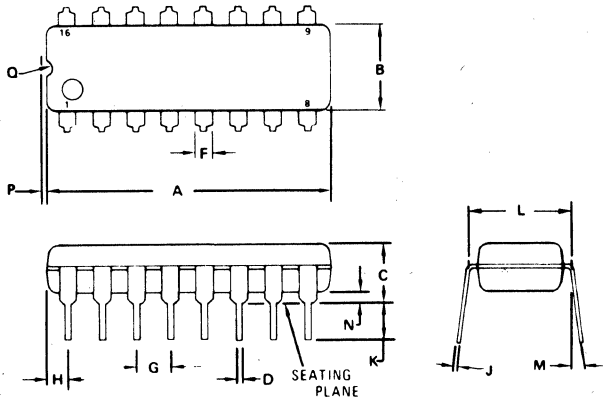


	A	B	C	D	E	F	G	H	J	K	L	M
DL51	.950 1.000	.275 .310	.200 MAX	.020 MIN	.125 MIN	.090 .110	.015 .023	.040 .070	.290 .370	.008 .015		
DL51a	.970 .990	.289				.100 TYP		.050 TYP	.310	.009 .011	.020	.210 .220
DL51b	1.010	.298 MAX	.165 MAX	.020 .060	.125 MIN	.090 .110	.015 .023	.054	.300	.008 .015		

DL52

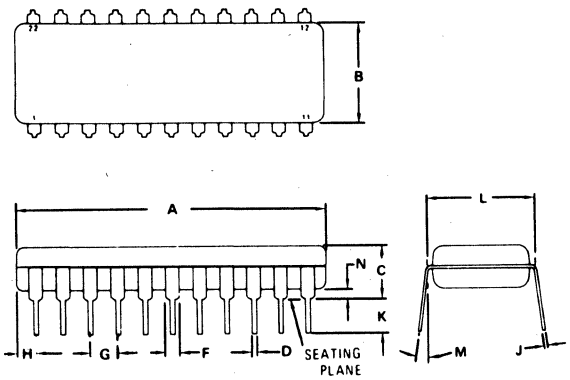


DL53



	A	B	C	D	F	G	H	J	K	L	M	N	P	Q
DL53	.815 .840	.240 .260	.160 .180	.015 .020	.040 .060	.100	.052 .072	.008 .012	.115 .135	.290 .310	10°	.020 .040	.005 .015	.020 .030
DL53a	.750 .780	.245 .275	.160 .200	.015 .020	.055 .065	.100	.020 .045	.008 .012	.125 .160	.290 .310	15°	.020 .040		

DL54

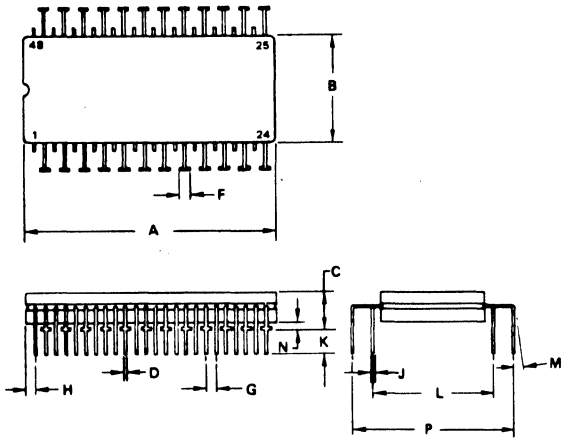


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	28.83	29.59	1.135	1.165
B	8.64	9.14	0.340	0.360
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	9.65	10.16	0.380	0.400
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

20. OUTLINE DRAWINGS

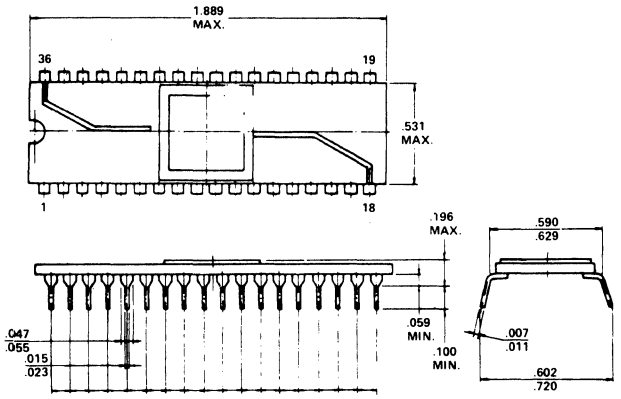
IN DRAWING NUMBER SEQUENCE

DL55

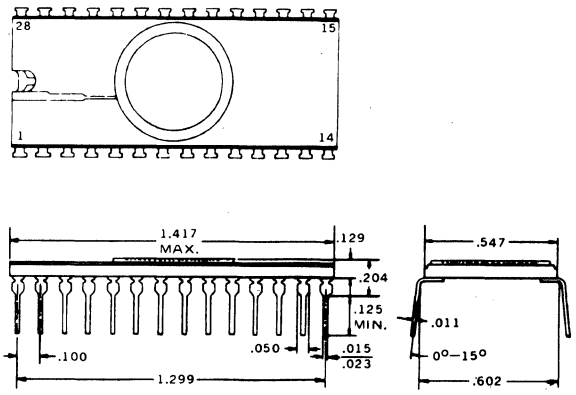


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.57	5.59	0.180	0.220
D	0.36	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	1.27 BSC		0.050 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.54	3.30	0.100	0.130
L	15.24 BSC		0.600 BSC	
M	–	7°	–	7°
N	0.51	1.52	0.020	0.060
P	20.32 BSC		0.800 BSC	

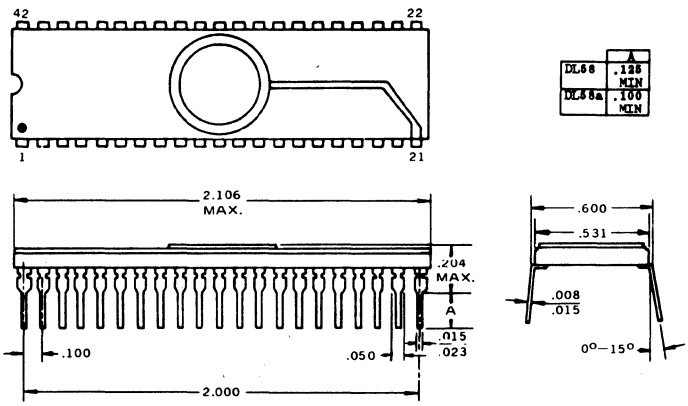
DL56



DL57



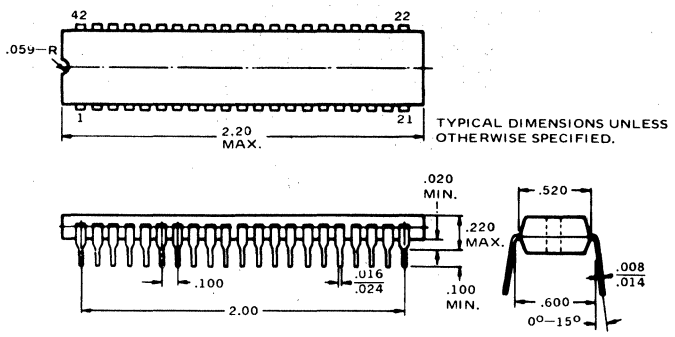
DL58



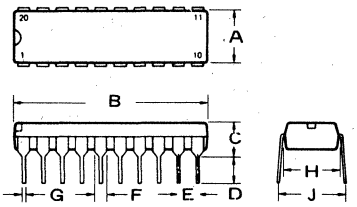
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

DL59

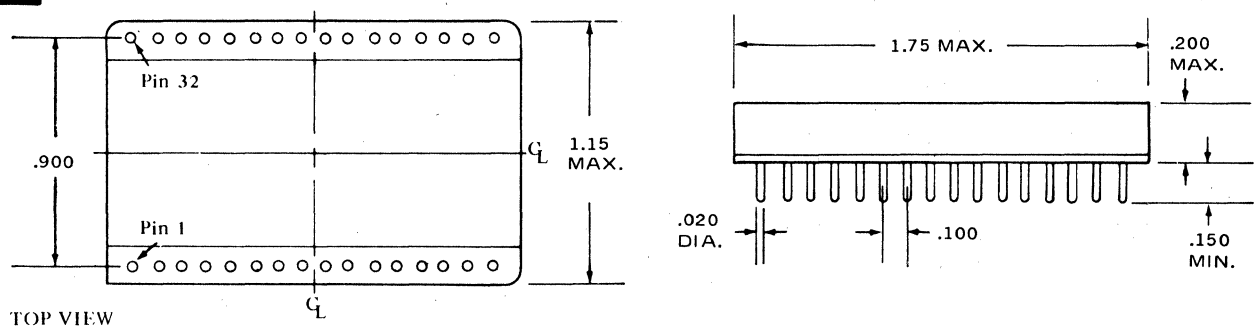


DL60

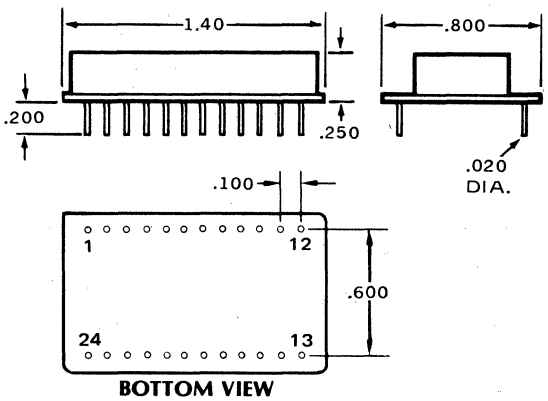


	A	B	C	D	E	F	G	H	J
DL60	.255 .265	1.015 1.025	.200 MAX	.125 MIN	.090 .110	.045 .065	.018 .022	.290 .310	.325 .375
DL60a	.250 .290	1.010 1.050	.150 .200	.125 .150	.090 .110	.055 .065	.015 .020		.310 .385
DL60b	.245 .285	.935 .970	.140 .220	.125 .150	.090 .110	.050 .070	.016 .020		.290 .320

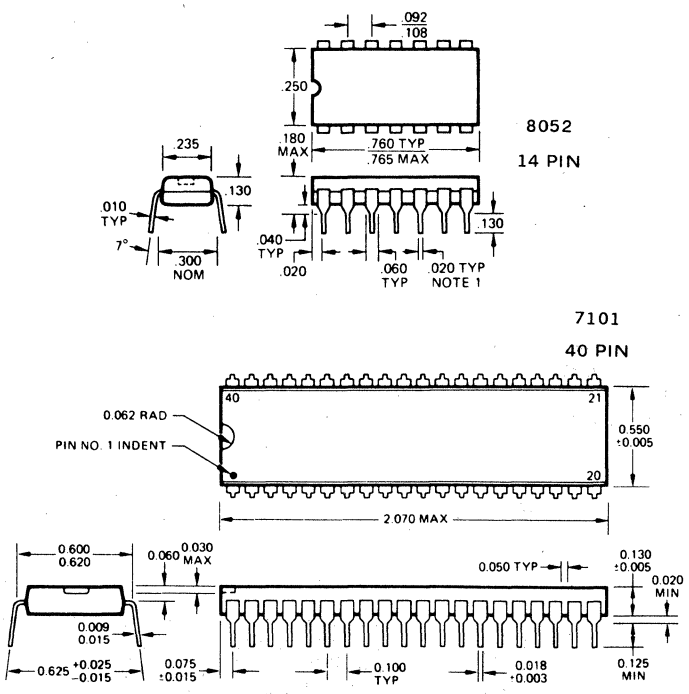
DL61



DL62



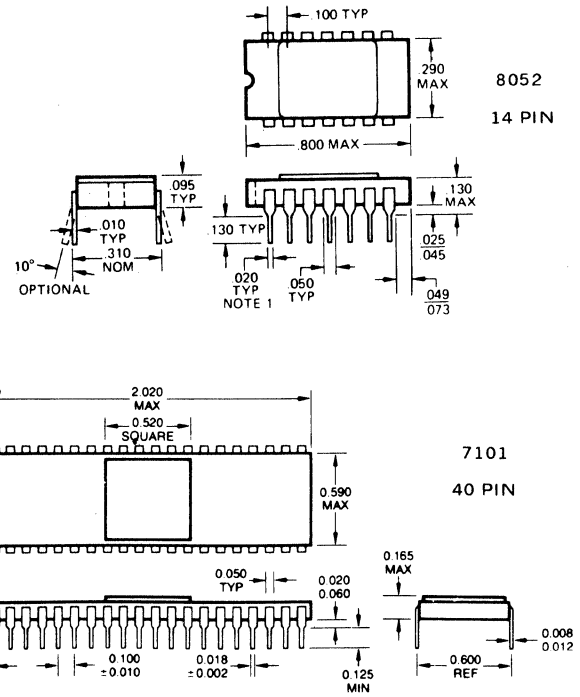
DL63



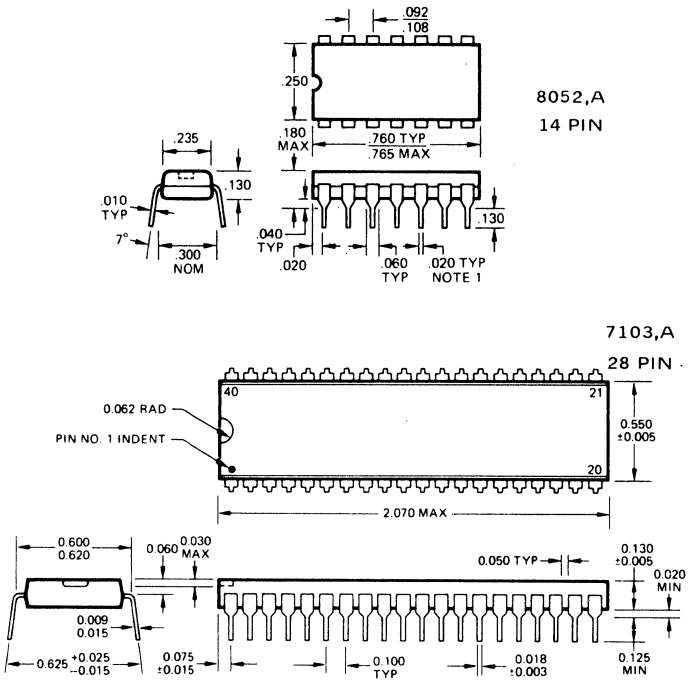
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

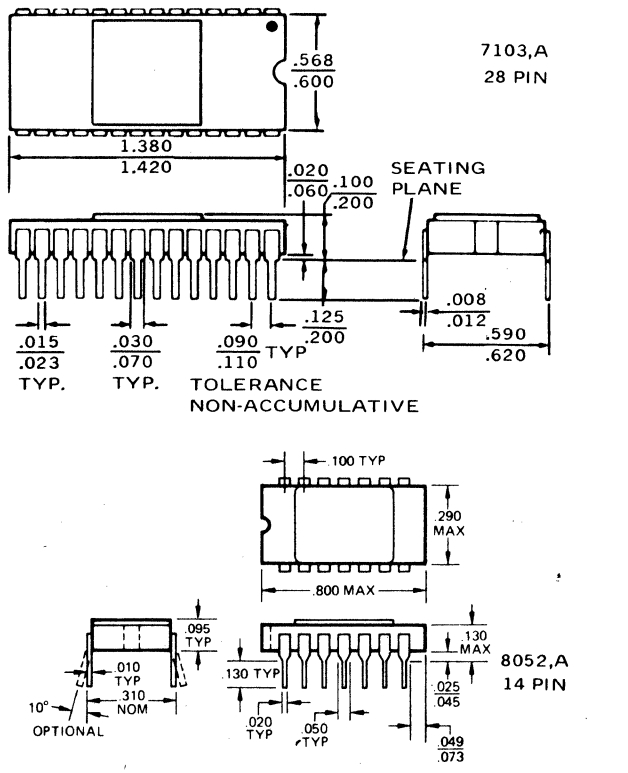
DL64



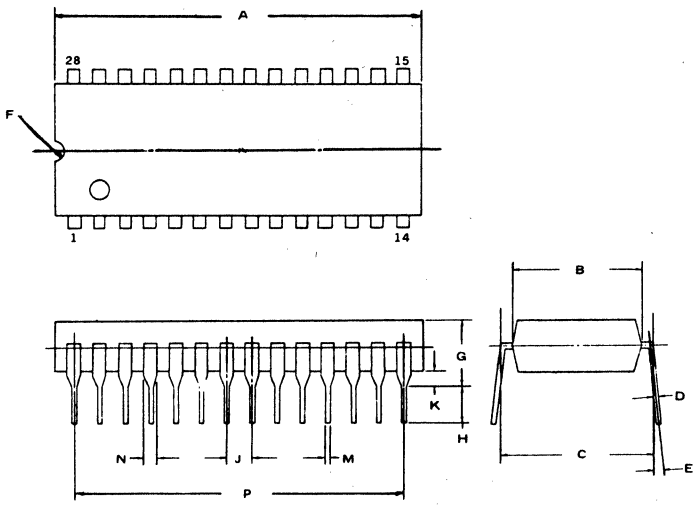
DL65



DL66



DL67

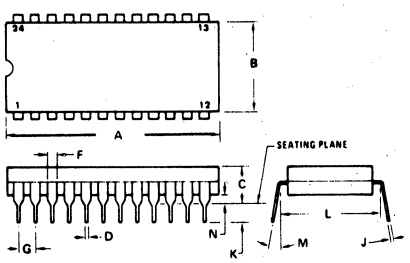


	A	B	C	D	E	F	G	H	J	K	M	N	P
DL67	1.496 MAX	.519	.600	.008 .013	0° 15°	.059	.225 MAX	.100 MIN	.100	.019 MIN	.015 .023	.059	1.300
DL67a	1.468	.515	.600		0° 15°	.059	.200	.106	.100	.070	.019	.053	
DL67b	1.500 MAX	.525 .535	.585 .690	.009 .011			.205 MAX	.125 MIN	.090 .110	.030 .045	.018 .022	.058 .062	.040 .050
DL67c	1.470 MAX	.545 .555	.600 .620	.009 .015		.062	.145 .155	.125 MIN	.100 TYP	.020 MIN	.015 .021		
DL67d	1.386 1.414	.568 .588	.584 .596	.009 .011	0° 10°		.120 .165	.100 .165	.100	.020 .060	.016 .020	.044 .056	
DL67e	1.520	.480 .590	.590 .610	.010	0° 15°		.220 MAX	.090 MIN	.100	.020 MIN	.016 .020		

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

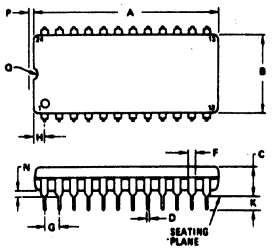
DL68



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.08	0.160	0.200
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	15.37 BSC		0.605 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLE.)

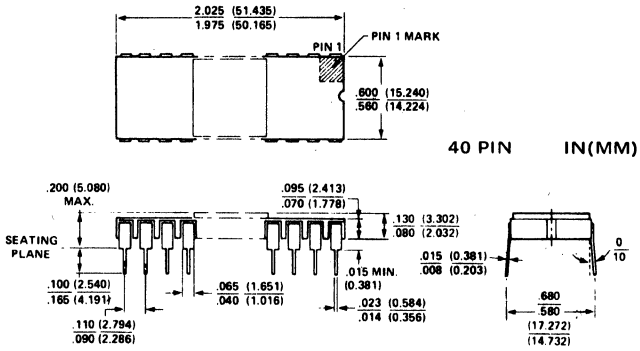
DL69



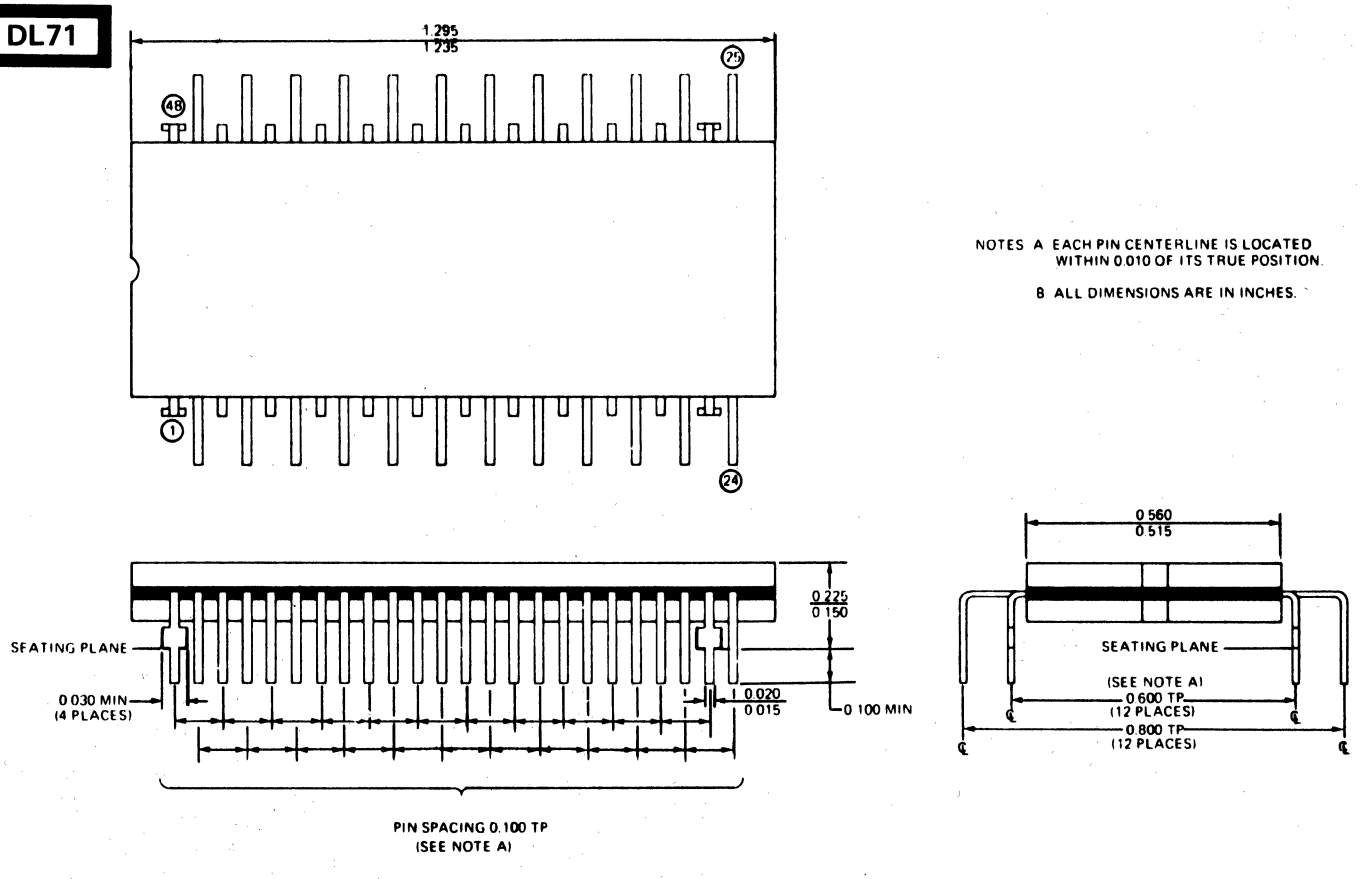
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.88	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.18	0.38	0.007	0.015
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	4.19	4.95	0.165	0.195
Q	3.81	4.19	0.150	0.165

Dimension "L" to lead centerline when formed parallel.

DL70



DL71



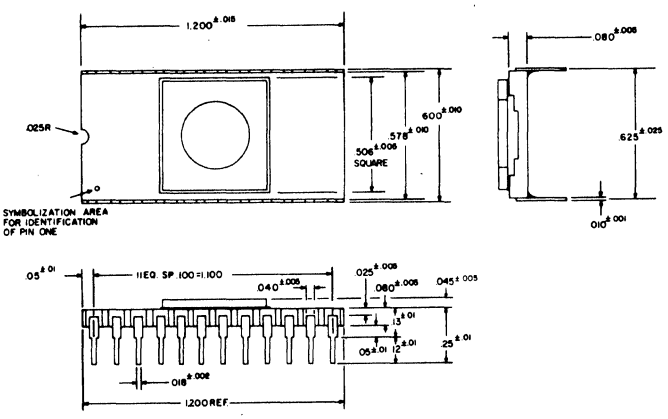
NOTES A EACH PIN CENTERLINE IS LOCATED WITHIN 0.010 OF ITS TRUE POSITION.

B ALL DIMENSIONS ARE IN INCHES.

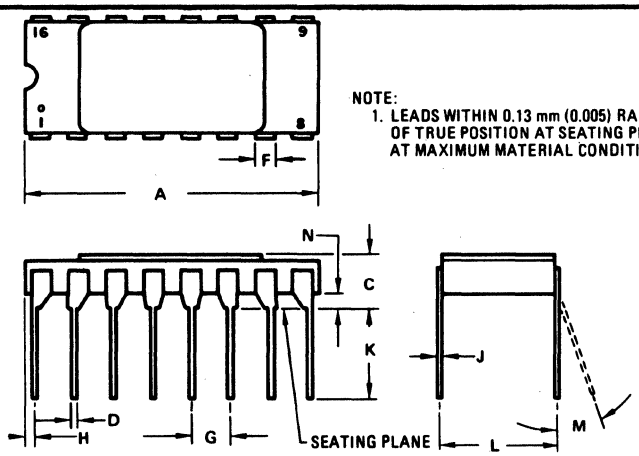
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

DL72



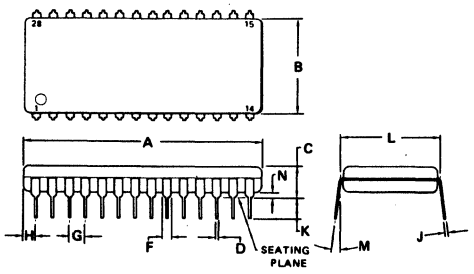
DL73



NOTE:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

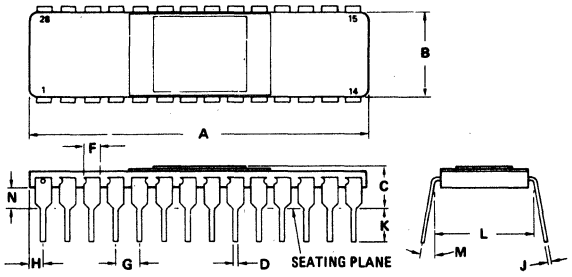
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
C	2.67	3.94	0.105	0.155
D	0.38	0.53	0.015	0.021
F	1.22	1.52	0.048	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.31	0.008	0.012
K	3.05	4.83	0.120	0.190
L	7.62 BSC		0.300 BSC	
M	–	10^0	–	10^0
N	0.64	1.52	0.025	0.060

DL74



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.99	15.49	0.590	0.610
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

DL75



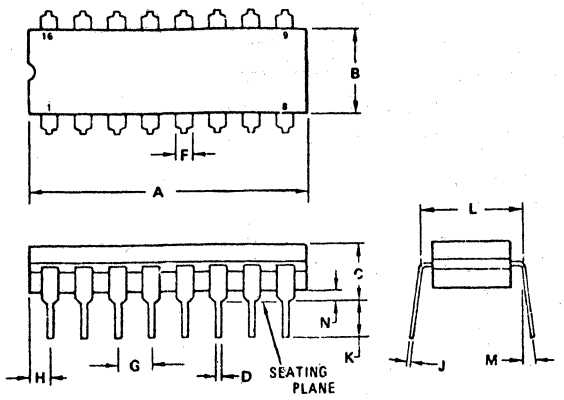
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	34.04	35.56	1.340	1.400
B	13.08	14.22	0.515	0.560
C	3.05	4.19	0.120	0.165
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.28	0.008	0.011
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15^0	–	15^0
N	0.51	1.27	0.020	0.050

NOTES:
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. TO DIM. "A" & "B" AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW PACKAGE BASE).

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

DL76

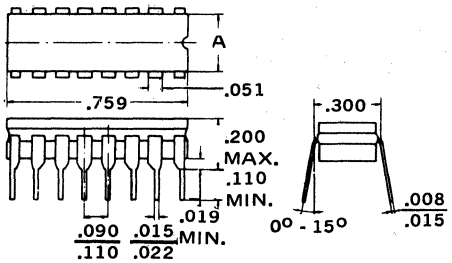


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

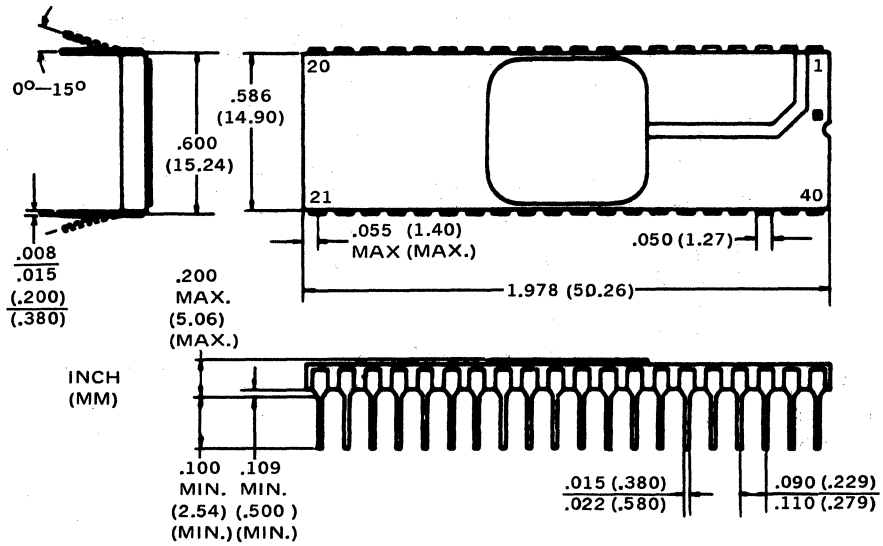
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DL77

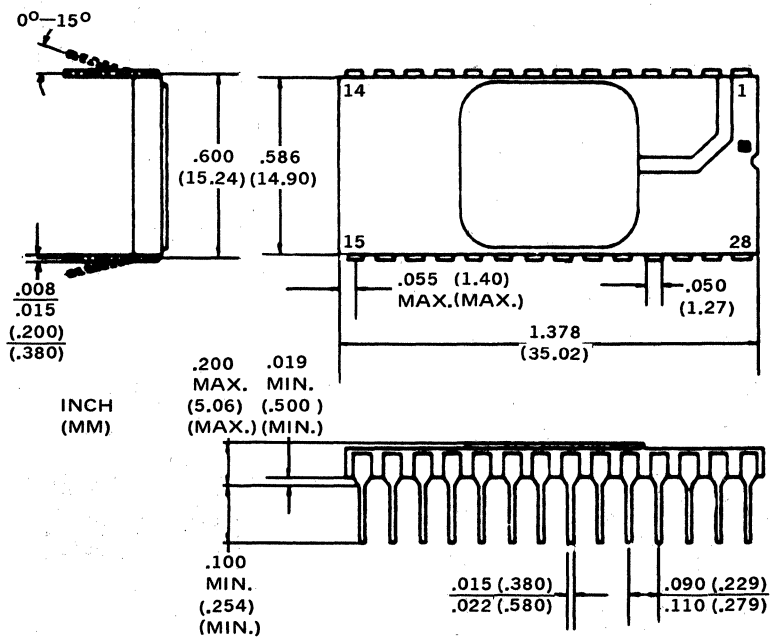
	A
DL77	.248
DL77a	.267



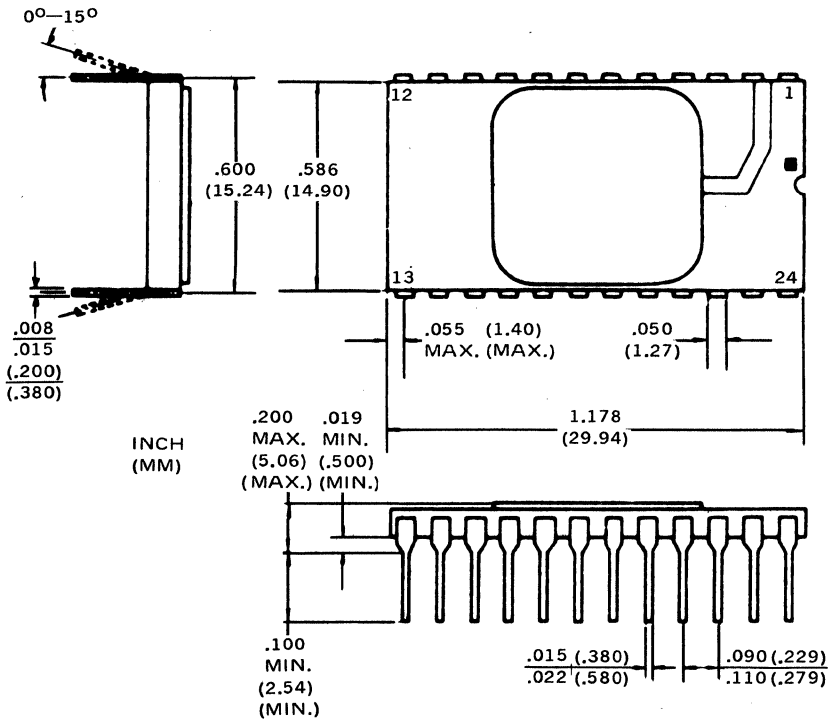
DL79



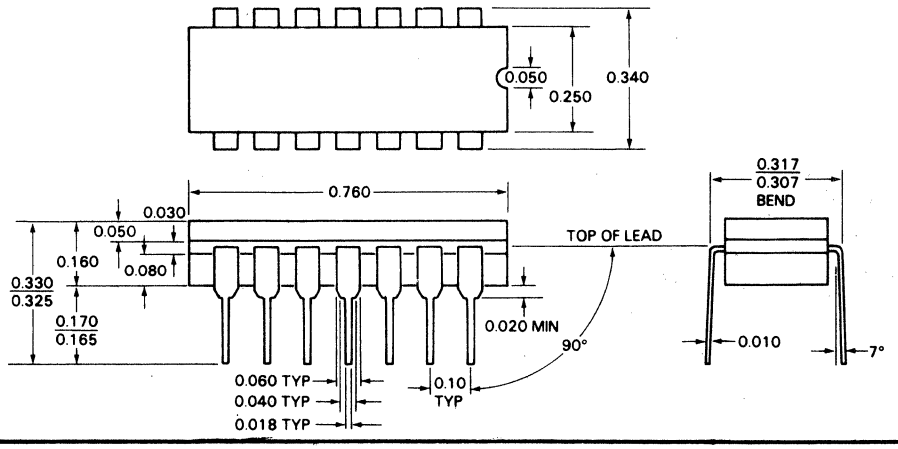
DL80



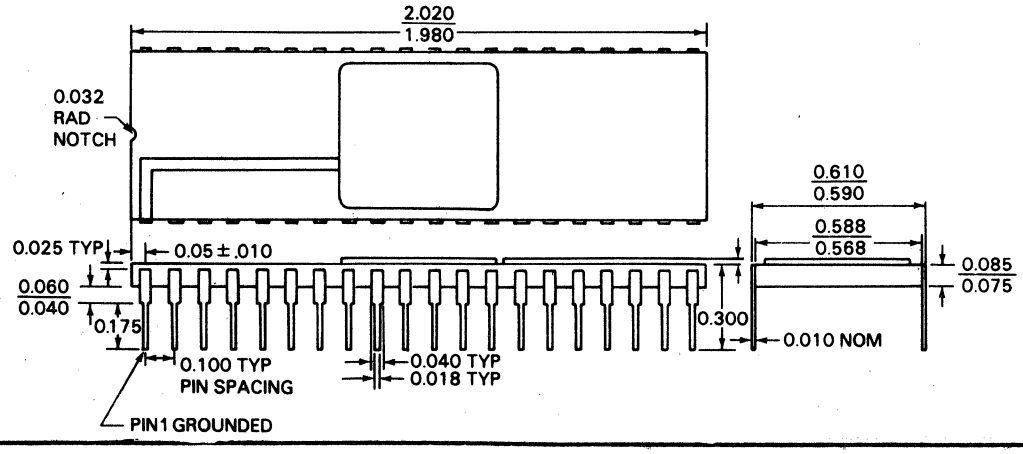
DL81



DL82



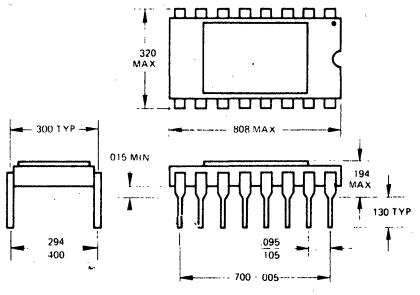
DL83



20. OUTLINE DRAWINGS

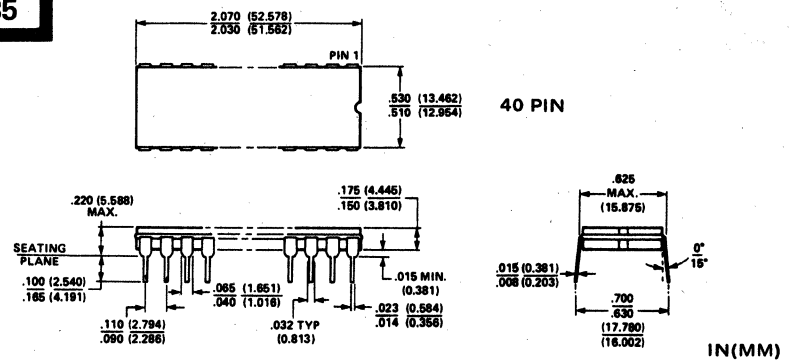
IN DRAWING NUMBER SEQUENCE

DL84



16 LEAD CERAMIC DIP

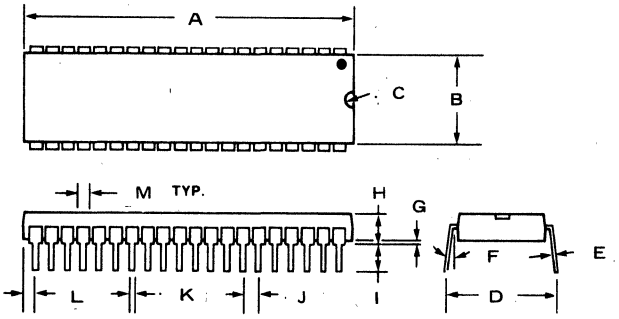
DL85



IN(MM)

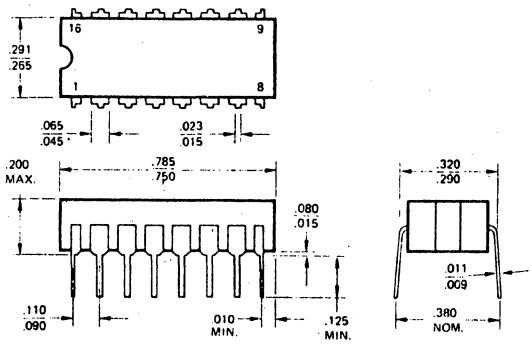
DL86

	A	B	C	D	E	F	G	H	I	J	K	L	M
DL86	2.040	.540	.120	.680 MAX	.011 .013	5°	.025	.160	.160 MIN	.100	.018 .020	.070	.060 .002
DL86a	2.050	.540	.180	.625	.010 .002	90°	.150	.075	.125	.100	.018	.020	.055



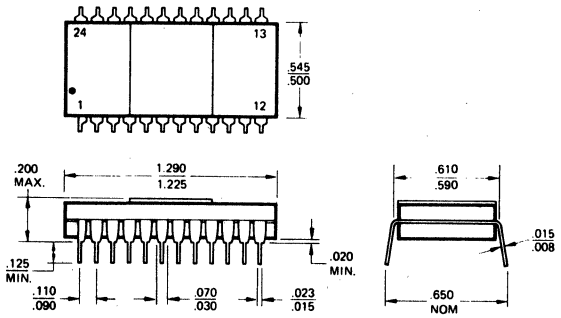
DL87

Hermetic



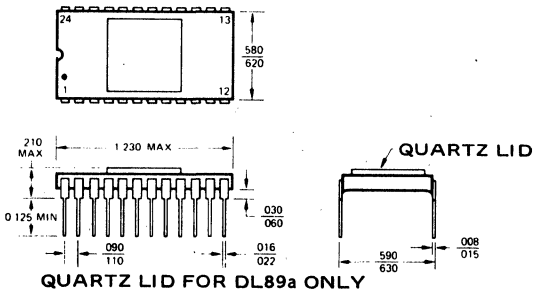
DL88

Hermetic



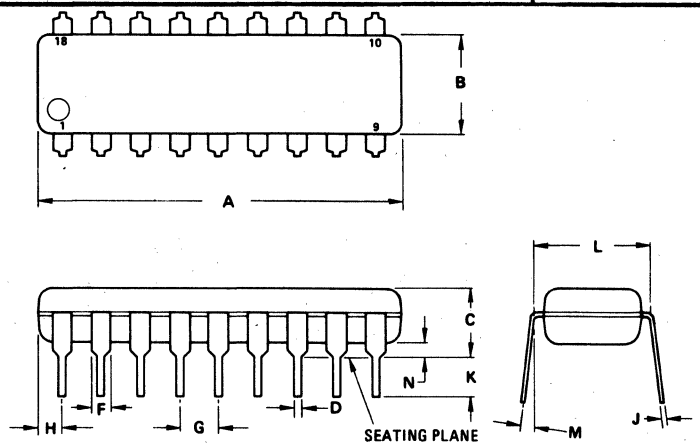
DL89

Quartz Lid



QUARTZ LID FOR DL89a ONLY

DL90

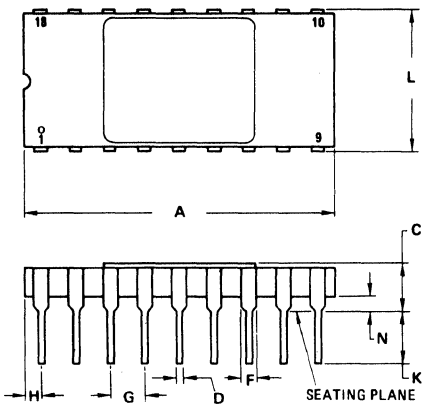


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.60	7.11	0.260	0.280
C	4.06	4.57	0.160	0.180
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.14	1.40	0.045	0.055
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	7.37	7.87	0.290	0.310
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

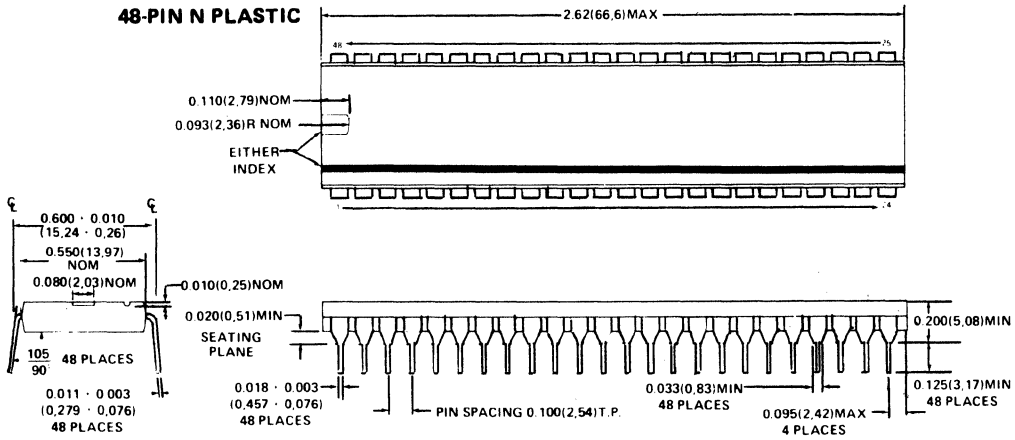
DL91



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.48	23.24	0.885	0.915
C	3.18	4.27	0.125	0.168
D	0.38	0.58	0.015	0.023
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	1.14	1.40	0.045	0.055
J	0.20	0.30	0.008	0.012
K	2.68	4.44	0.105	0.175
L	7.37	8.23	0.290	0.324
M	–	10^0	–	10^0
N	0.64	1.52	0.025	0.060

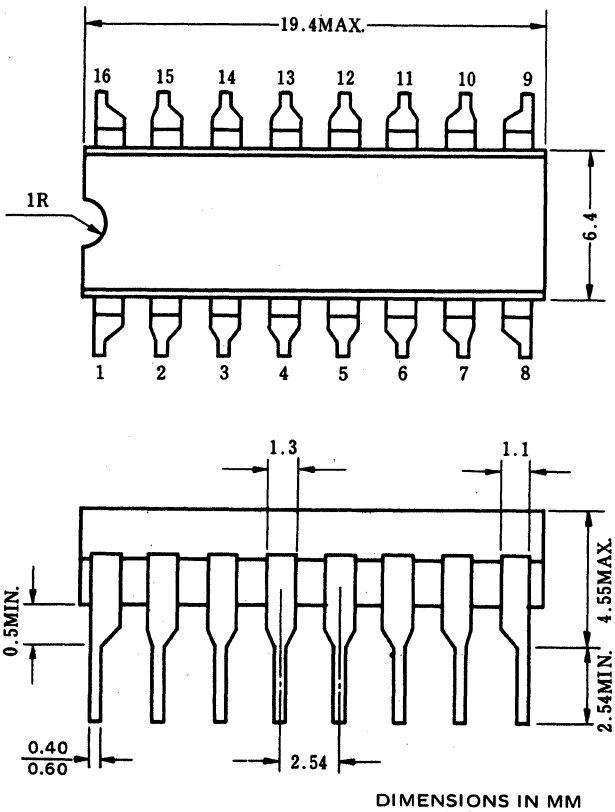
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. NOMINAL DIM FROM CENTER OF LEADS PARALLEL TO DIM "L" IS 7.62 mm (0.300").

DL92



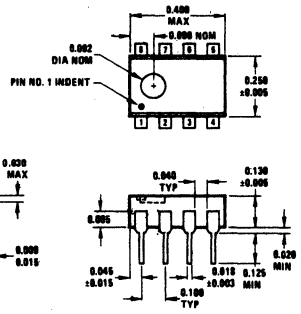
IN(MM)

DL93



DIMENSIONS IN MM

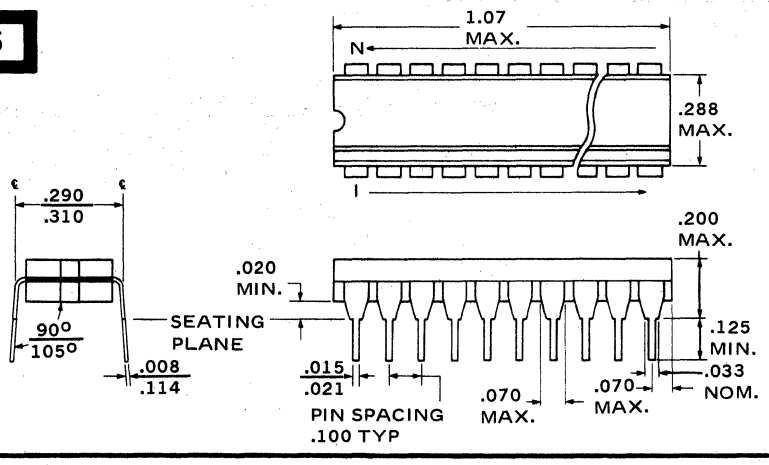
DL94



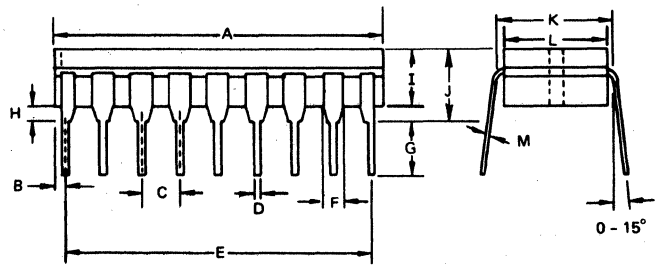
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

DL95

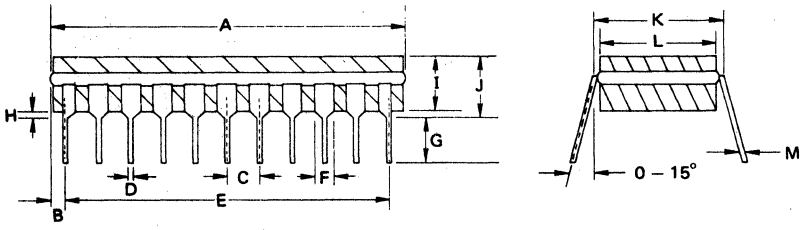


DL96



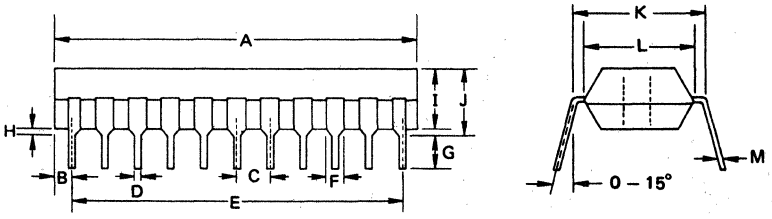
ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.46	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	8.7	0.26
M	0.26	0.01

DL97



ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

DL98

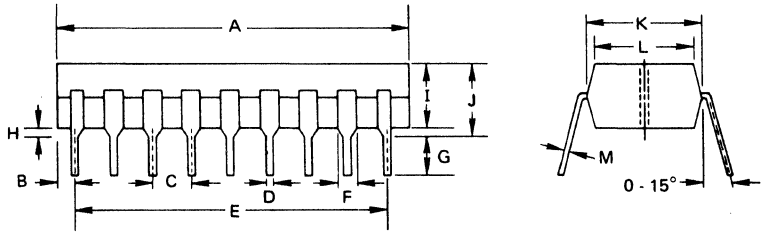


ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

20. OUTLINE DRAWINGS

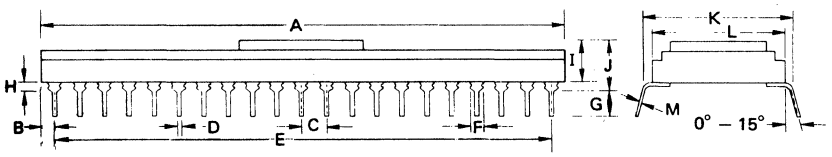
IN DRAWING NUMBER SEQUENCE

DL99



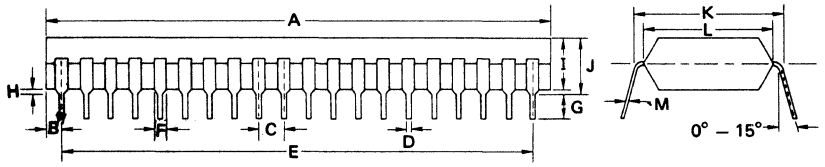
ITEM	MILLIMETERS	INCHES
A	22.5 MAX.	0.89
B	1.09	0.04
C	2.54	0.10
D	0.50 ± 0.10	0.02
E	20.32	0.80
F	1.2 MIN.	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

DL100



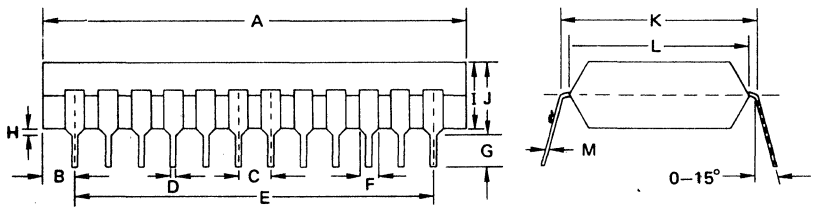
ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

DL101



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.10
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

DL102

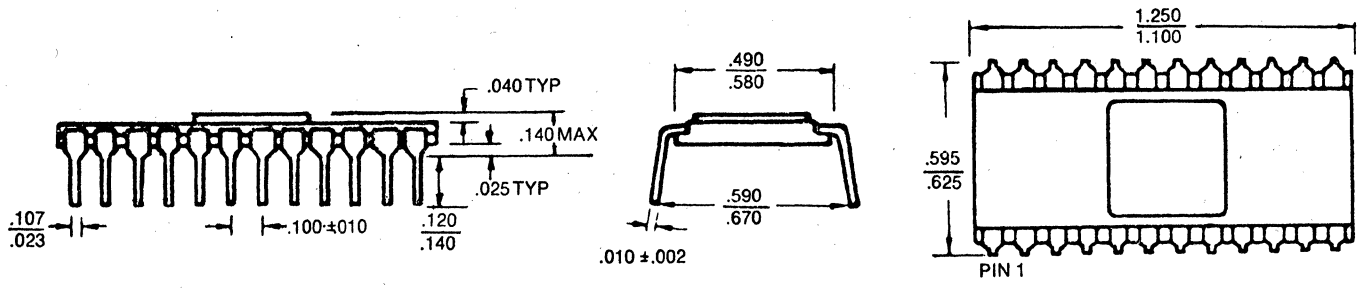


ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

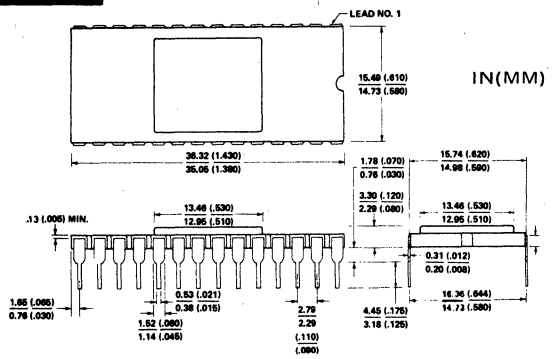
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

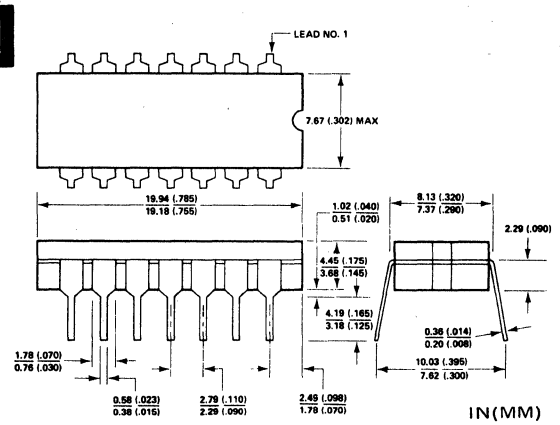
DL104



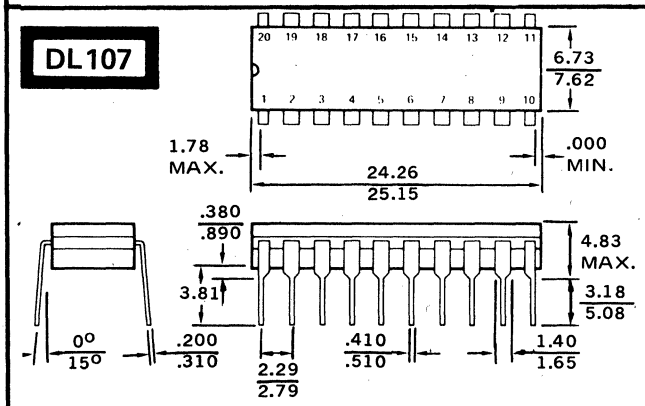
DL105



DL106

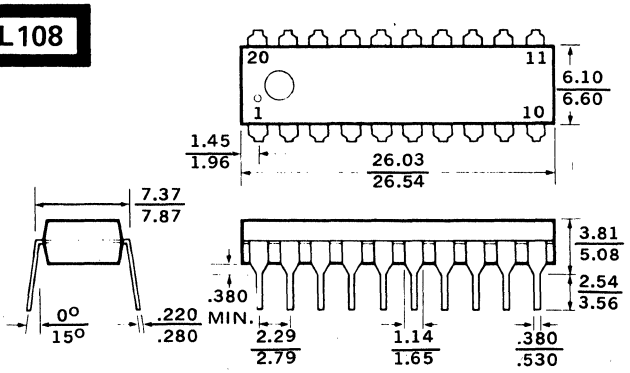


DL107



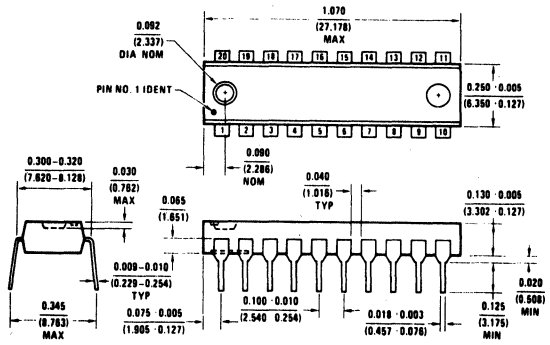
DIMENSIONS IN MM

DL108



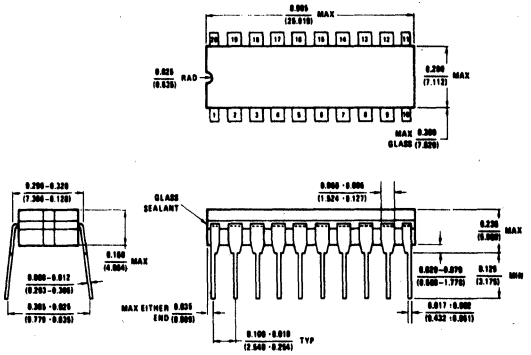
DIMENSIONS IN MM

DL109



IN
(MM)

DL110

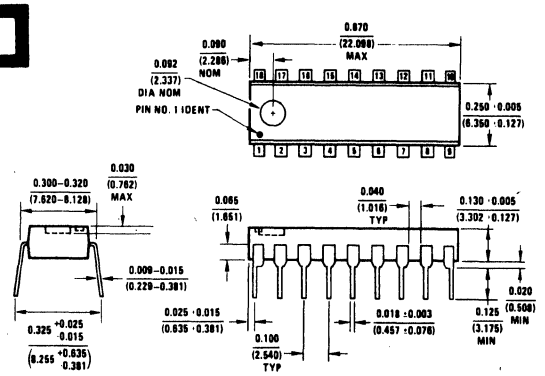


IN
(MM)

20. OUTLINE DRAWINGS

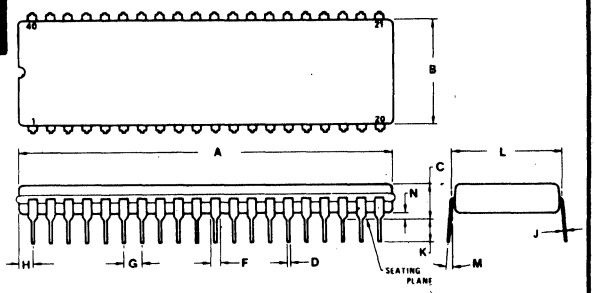
IN DRAWING NUMBER SEQUENCE

DL111



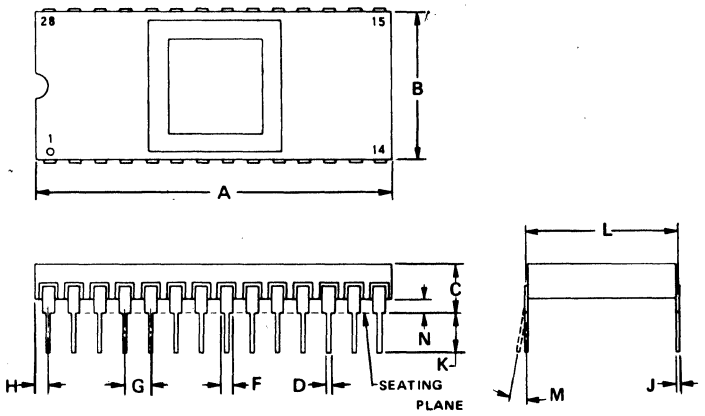
IN
(MM)

DL112



	A	B	C	D	F	G	H	J	K	L	M	N
DL112	2.06	.500	.200	.015	.050	.100	.080	.008	.125	.600	5°	.020
	2.09	.540	.230	.022	.065	BSC	.095	.012	.160	BSC	15°	.050
DL112a	2.05	.530	.150	.015	.055	.090	.040	.009	.125	.585		.015
	2.08	.550	.200	.020	.065	.110	.070	.011	.160	.700		.060
DL112b	2.06	.500	.160	.015	.050	.100		.008	.125	.600	5°	.020
	2.09	.600	.230	.022	.065	BSC		.012	.160	BSC	15°	.050

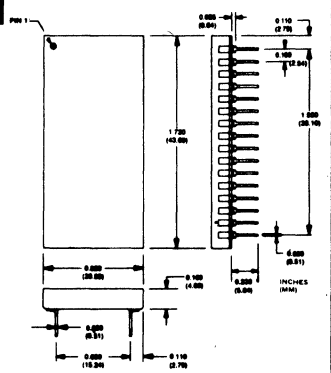
DL113



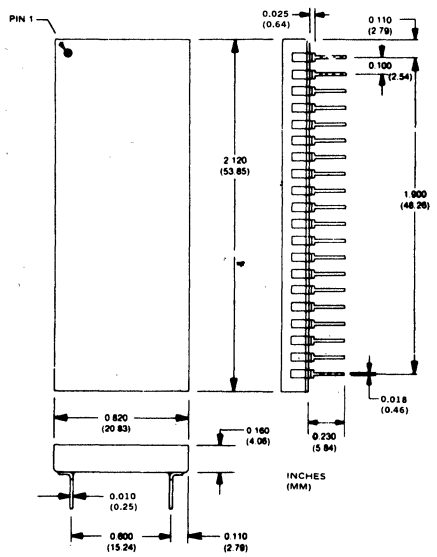
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	52.32	53.09	2.060	2.090
B	12.70	13.72	0.500	0.540
C	5.08	5.84	0.200	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
H	2.03	2.41	0.080	0.095
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	35.20	35.92	1.386	1.414
B	14.43	14.94	0.568	0.588
C	3.05	4.19	0.120	0.165
D	0.41	0.51	0.016	0.020
F	1.12	1.42	0.044	0.056
G	2.54 BSC		0.100 BSC	
H	1.12	1.42	0.044	0.056
J	0.23	0.28	0.009	0.011
K	2.54	4.19	0.100	0.165
L	14.83	15.14	0.584	0.596
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

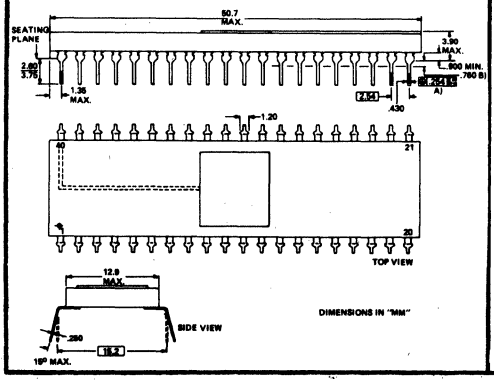
DL114



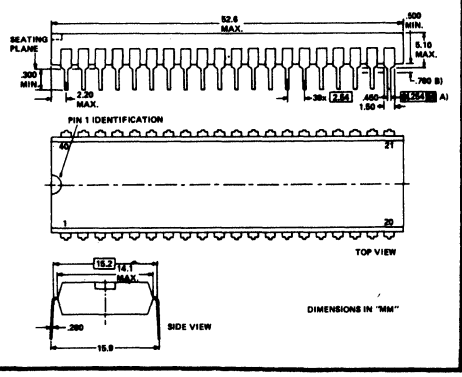
DL115



DL116



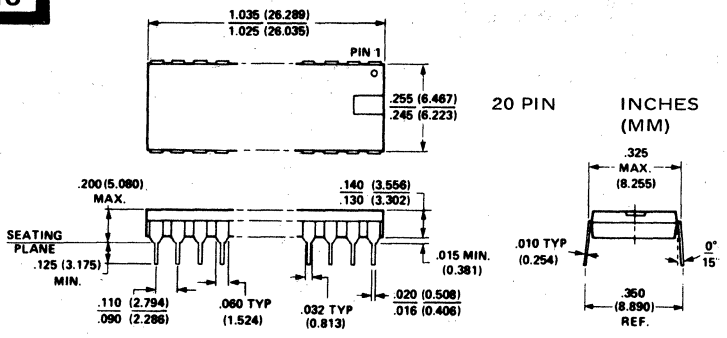
DL117



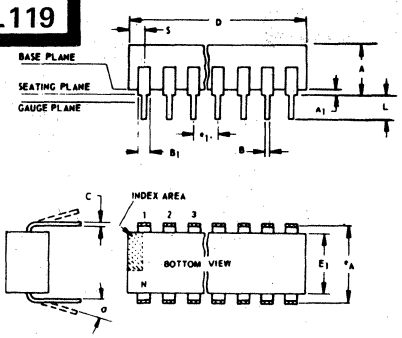
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

DL118



DL119



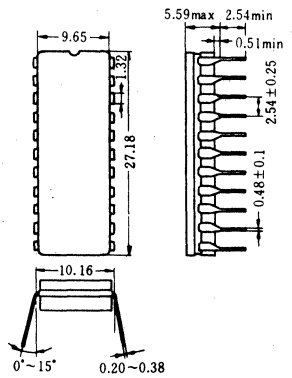
SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.845	0.885		21.47	22.47
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2,3	7.62 TP	
L	0.125	0.150		3.18	3.81
α	0°	15°	4	0°	15°
N	18		5	18	
N_1	0		6	0	
S	0.015	0.060		0.39	1.52

NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

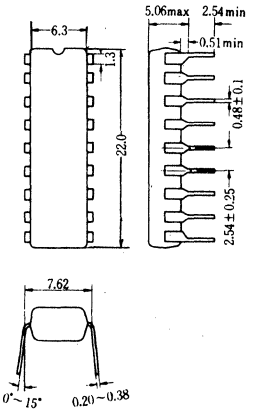
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads

DL120



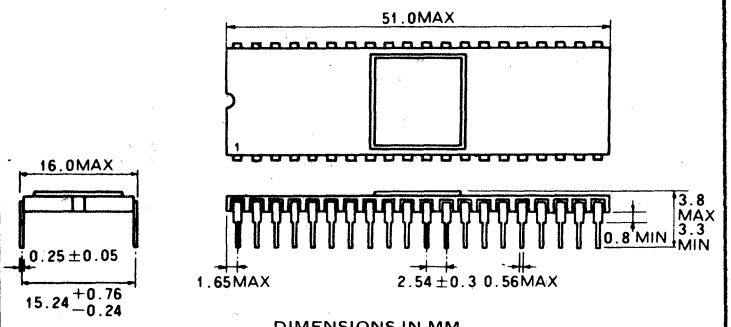
DIMENSIONS IN "MM"

DL121



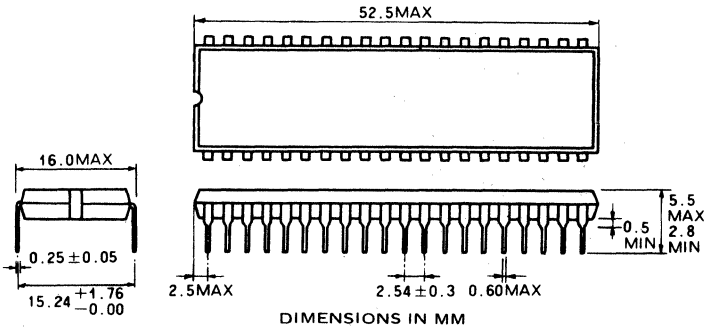
DIMENSIONS IN "MM"

DL122



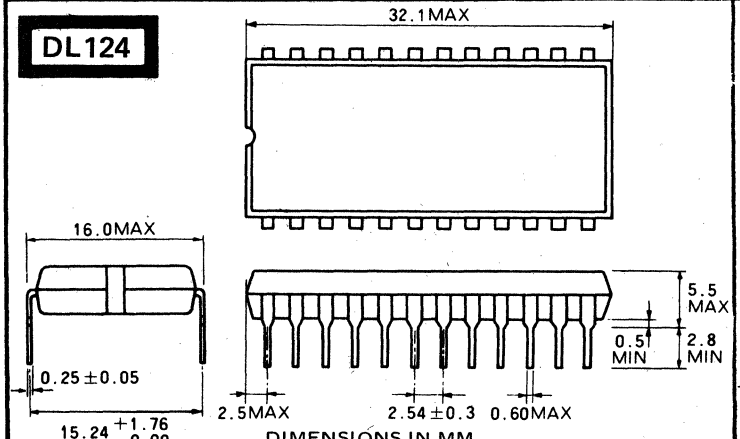
DIMENSIONS IN MM

DL123



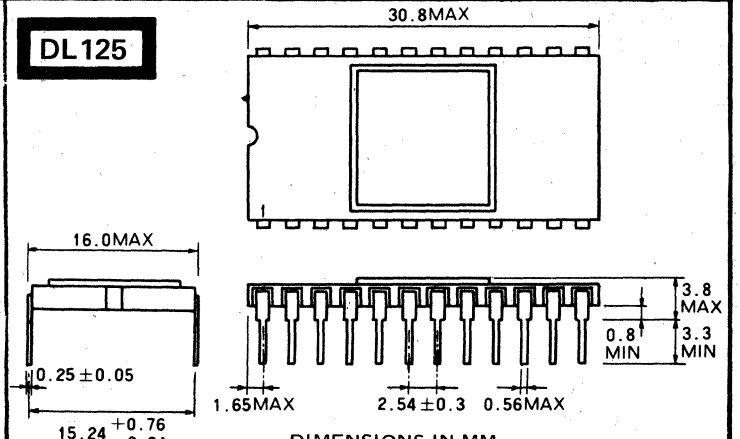
DIMENSIONS IN MM

DL124



DIMENSIONS IN MM

DL125

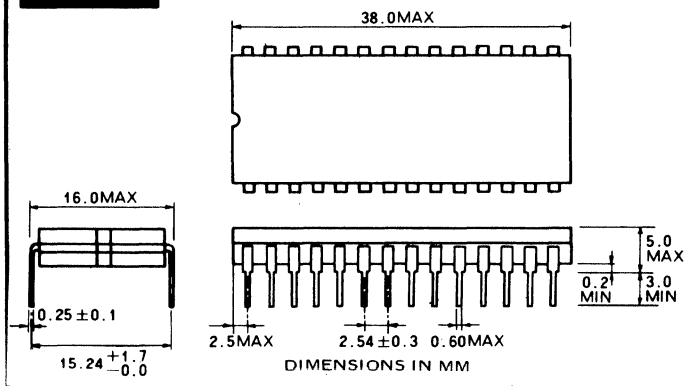


DIMENSIONS IN MM

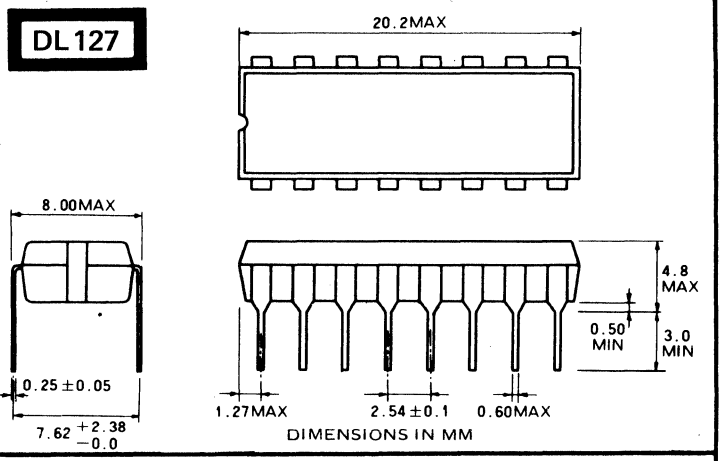
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

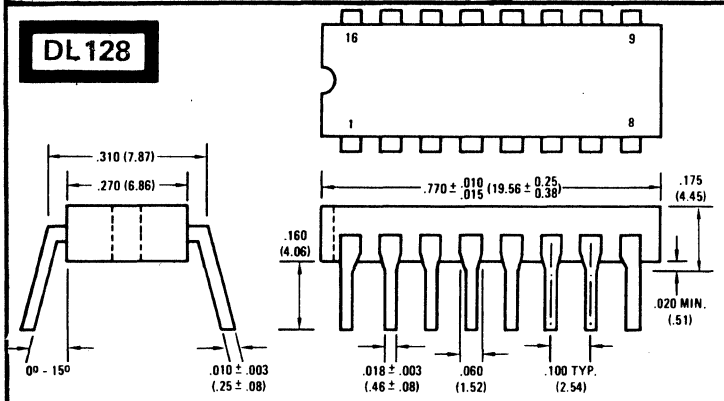
DL126



DL127

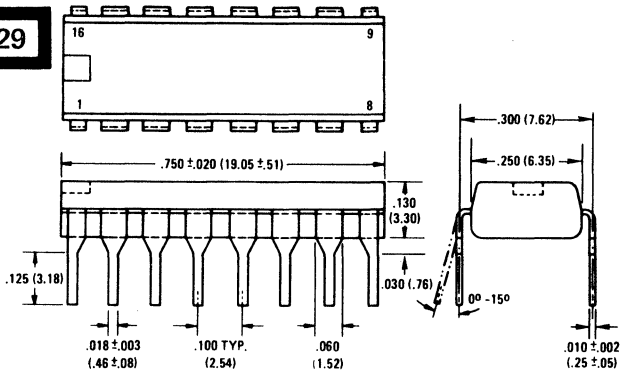


DL128



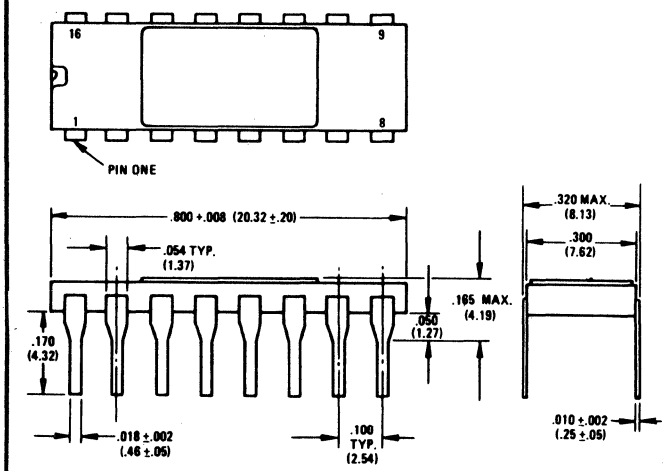
1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

DL129



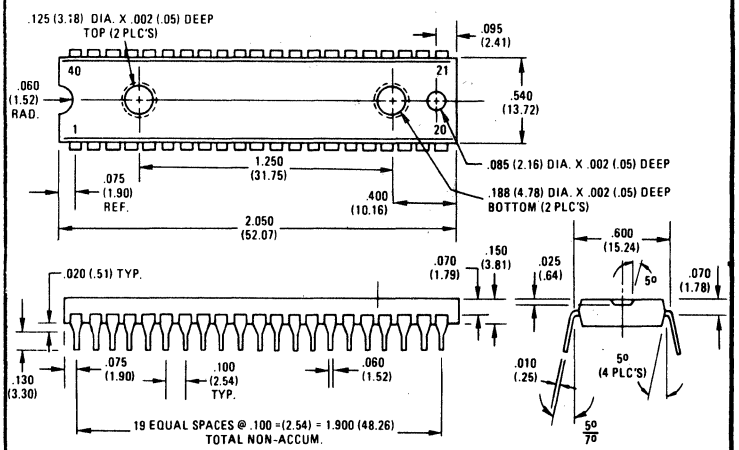
1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

DL130



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

DL131

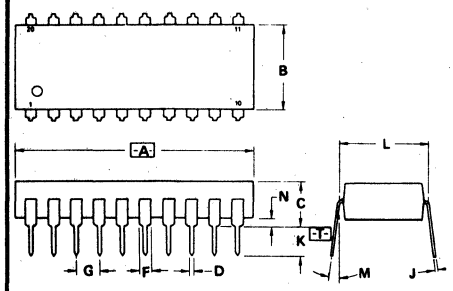


1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

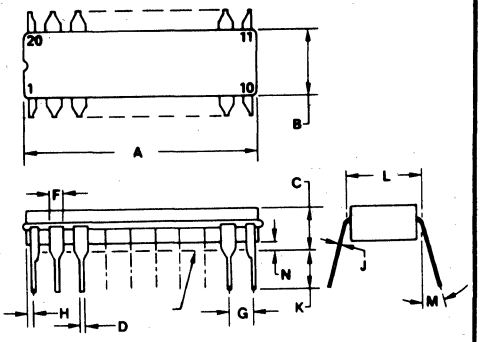
DL132



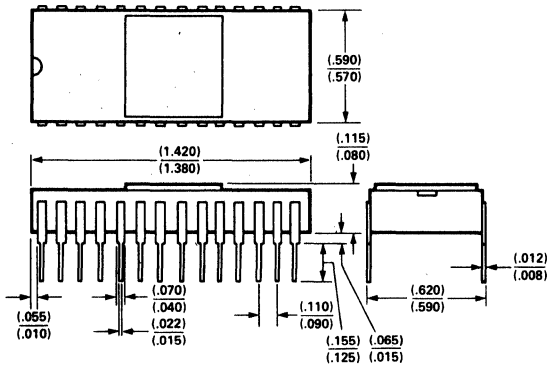
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.19	0.155	0.165
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

DL133

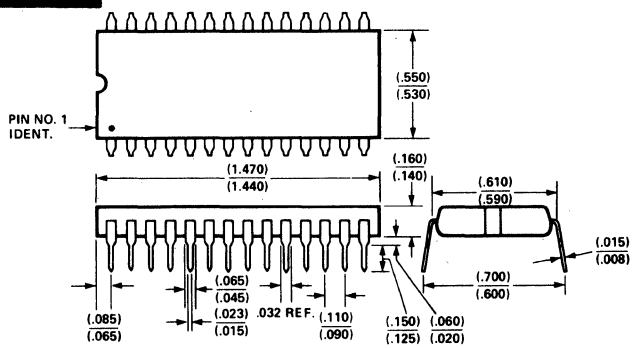
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.38	25.15	0.960	0.990
B	6.86	7.49	0.270	0.295
C	4.32	5.08	0.170	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030



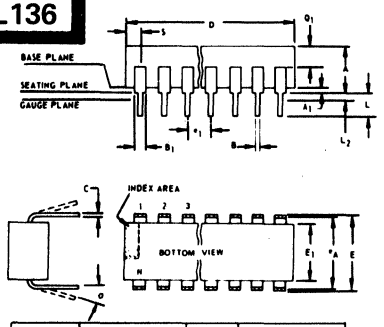
DL134



DL135



DL136

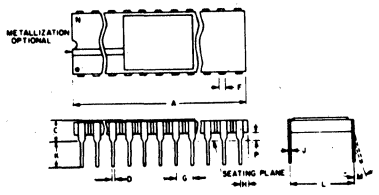


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.015	0.020		0.381	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D		1.120			28.44
E	0.390	0.420		9.91	10.66
E_1	0.345	0.355		8.77	9.01
e_1	0.100 TP		2	2.54 TP	
e_A	0.400 TP		2, 3	10.16 TP	
L	0.125	0.150		3.18	3.81
L_2	0	0.030		0	0.762
α	2°	15°	4	2°	15°
N	22		5	22	
N_1	0		6	0	
Q_1	0.055	0.085		1.40	2.15
S	0.015	0.060		0.381	1.52

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

DL137

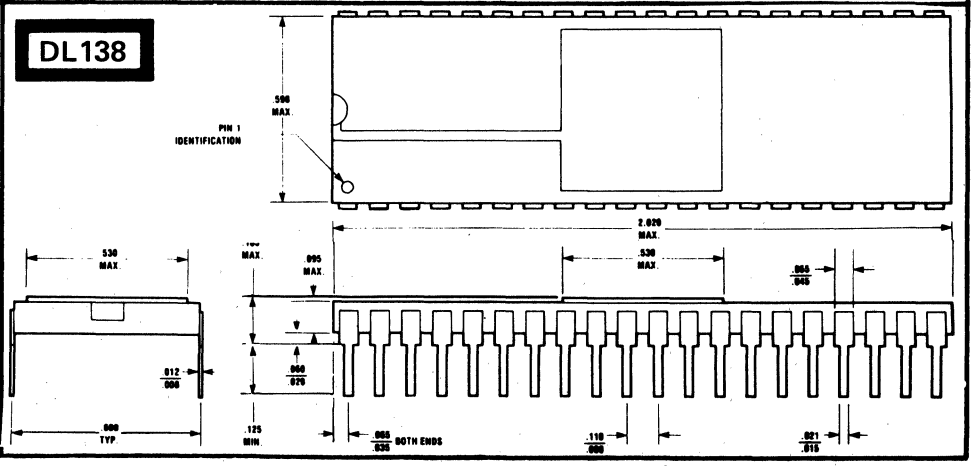


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.180	1.220		29.98	30.98
C	0.085	0.145		2.16	3.68
D	0.015	0.023		0.39	0.56
F	0.040 REF.			1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	–	7		–	7
P	0.025	0.050		0.64	1.27
N	24			24	

NOTES:

1. Leads within 0.005" (0.13 mm) radius of True Position at maximum material condition.
2. Center to center of leads when formed parallel.
3. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

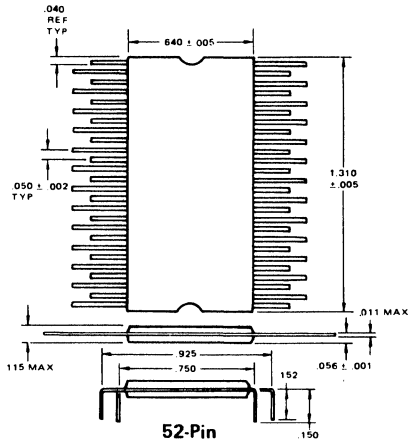
DL138



20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

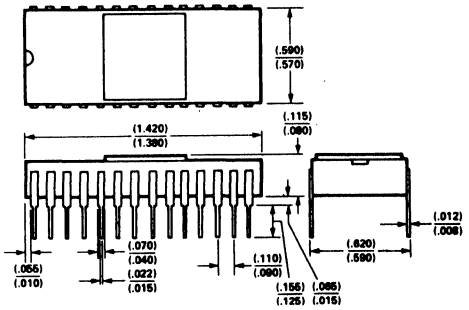
DL139



52-Pin

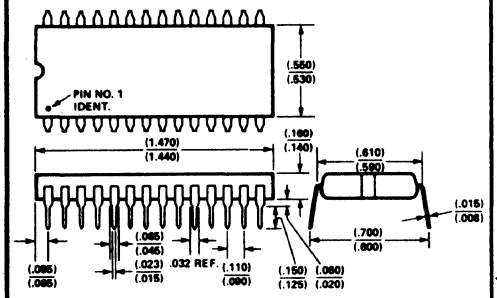
DL140

28 LEAD CERAMIC



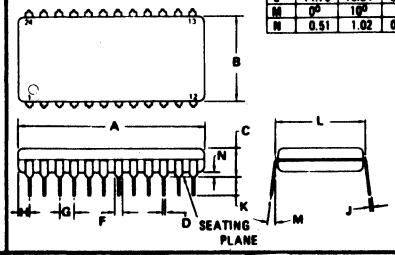
DL141

28 LEAD PLASTIC

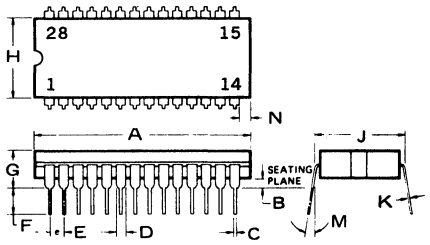


DL142

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.73	15.24	0.580	0.600
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

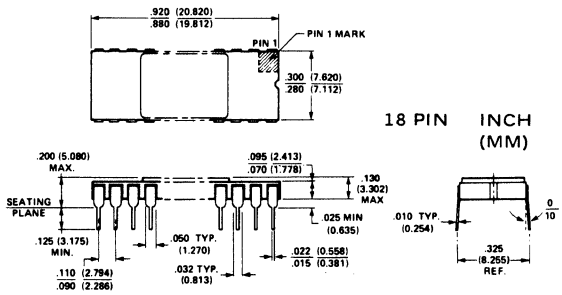


DL143

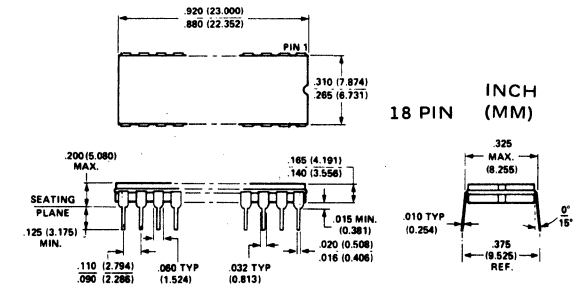


	A	B	C	D	E	F	G	H	J	K	M	N
DL143	1.44	.015	.016	.045	.090	.125	.150	.510	.600	.009	13°	.010
	1.49	.060	.020	.065	.110	.150	.225	.545	.620	.012		
DL143a	1.45	.015	.015	.055	.090	.125	.150	.530	.585	.009		.040
	1.48	.060	.020	.065	.110	.160	.200	.550	.700	.011		.070

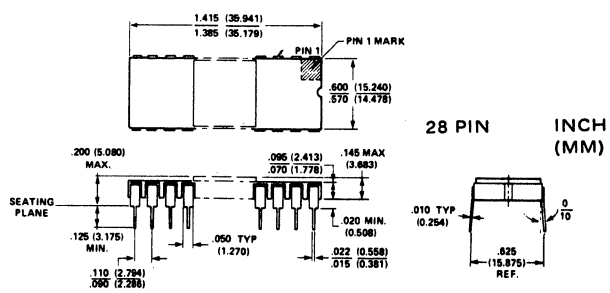
DL144



DL145



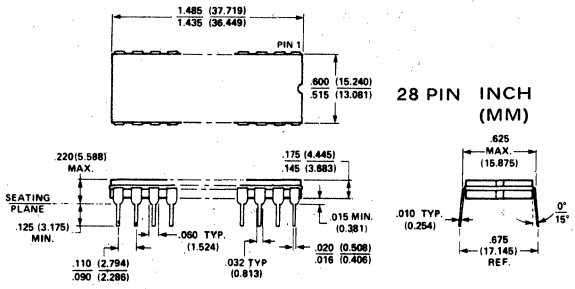
DL146



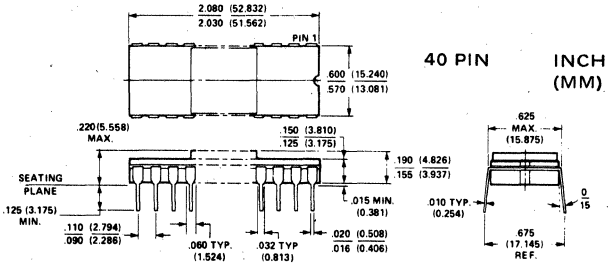
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

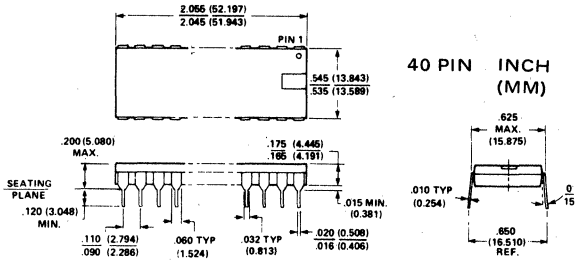
DL147



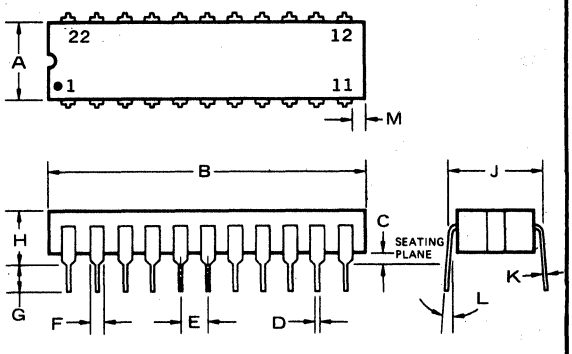
DL148



DL149



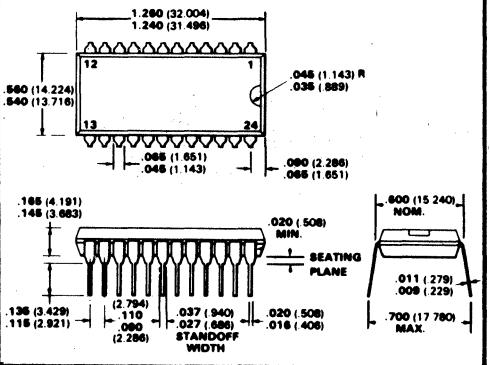
DL150



	A	B	C	D	E	F	G	H	J	K	L	M
DL150	.360	1.045	.015	.016	.090	.045	.125	.140	.390	.009	3°	.005
	.405	1.110	.060	.020	.110	.065	.150	.220	.420	.011	13°	MIN

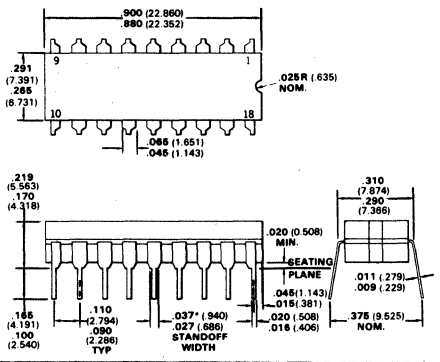
DL151

INCH (MM)



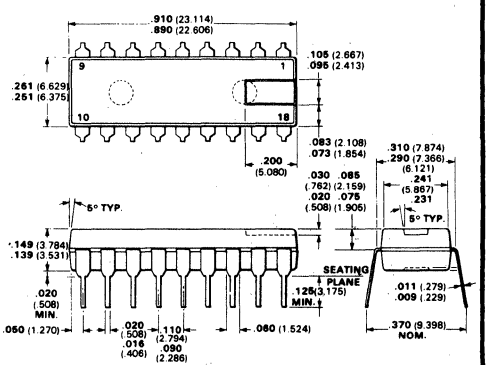
DL152

INCH (MM)



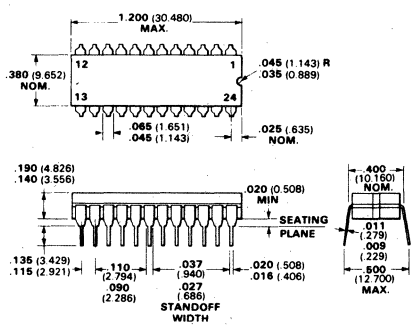
DL153

INCH (MM)



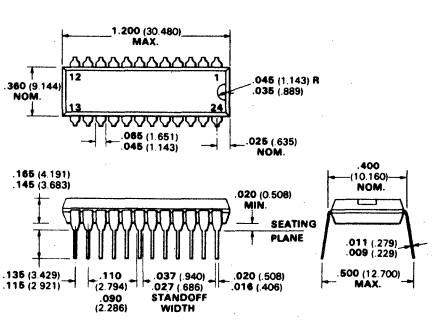
DL154

INCH (MM)



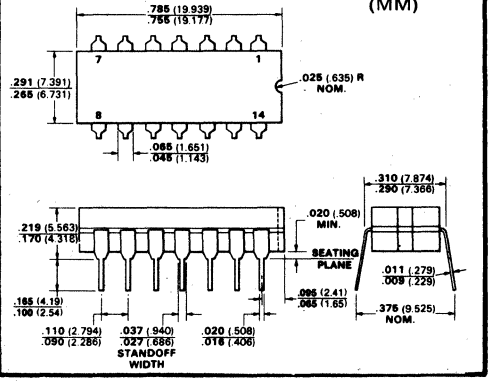
DL155

INCH (MM)



DL156

INCH (MM)

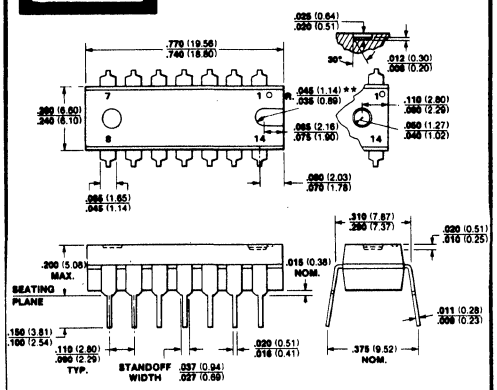


20. OUTLINE DRAWINGS

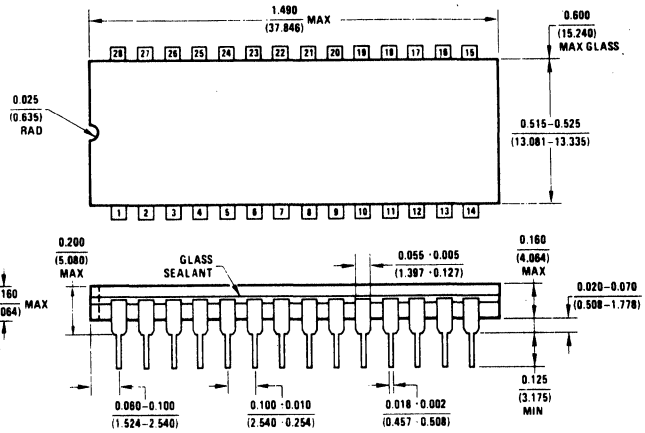
IN DRAWING NUMBER SEQUENCE

DL157

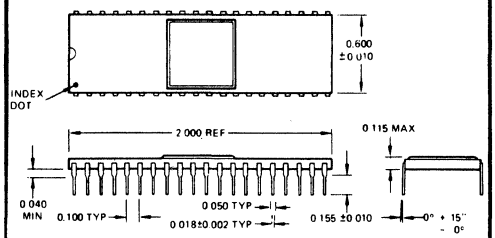
INCH (MM)



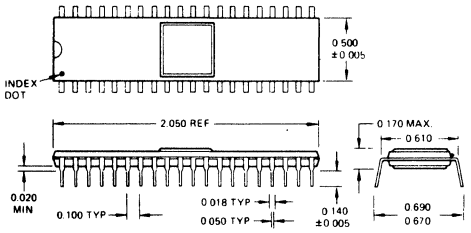
DL159



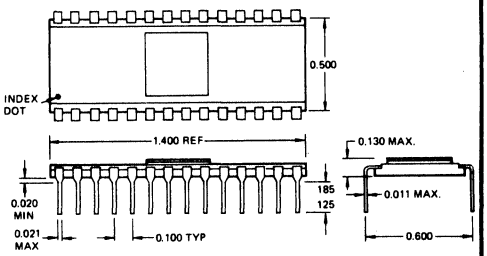
DL160



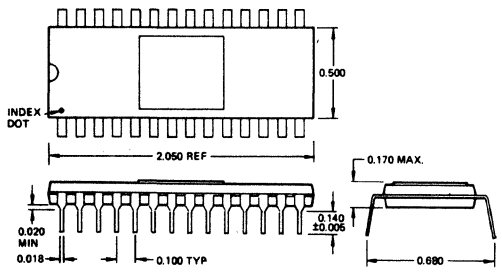
DL161



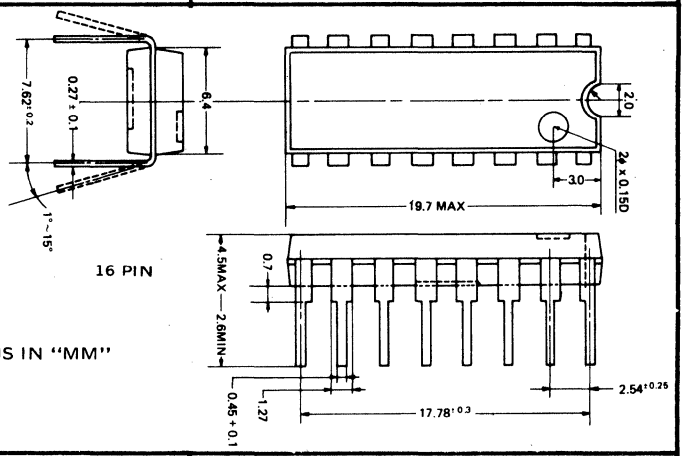
DL162



DL163

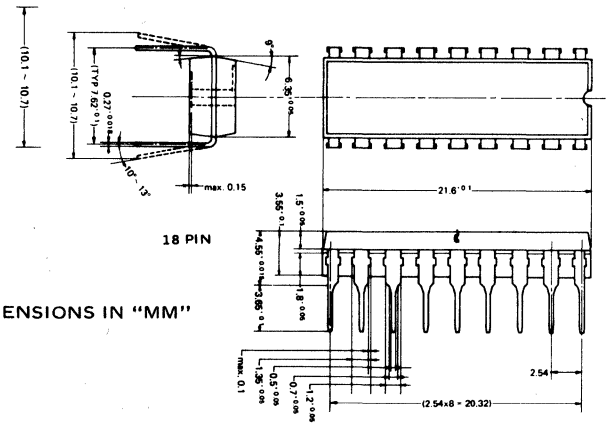


DL164



DIMENSIONS IN "MM"

DL165



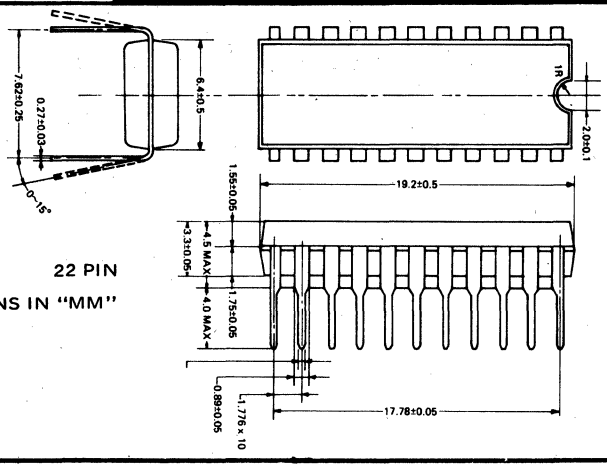
18 PIN

DIMENSIONS IN "MM"

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

DL166

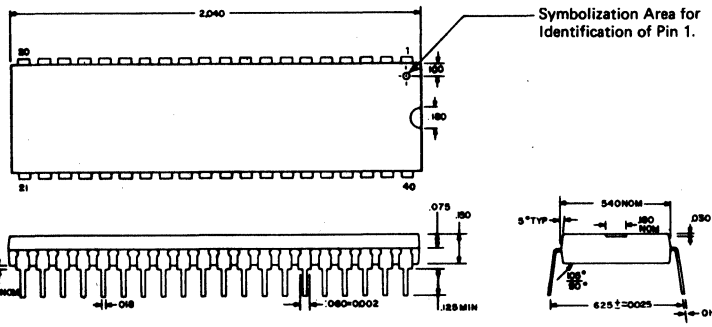


22 PIN

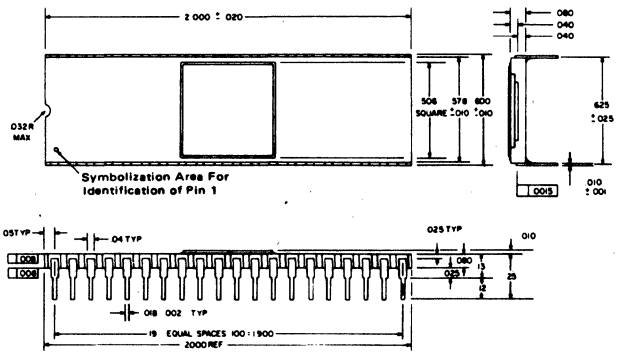
DIMENSIONS IN "MM"

DL167

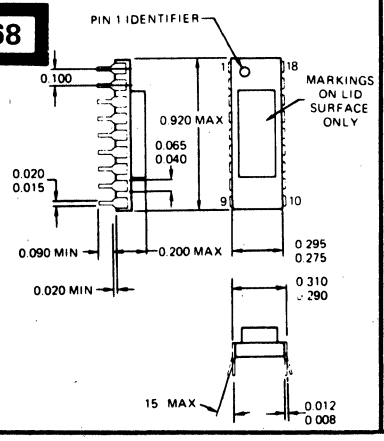
PLASTIC PACKAGE



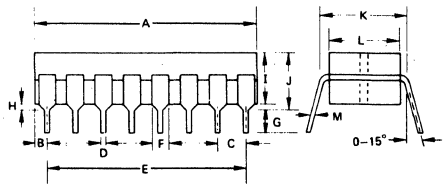
CERAMIC PACKAGE



DL168

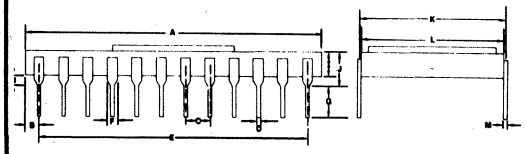


DL169



ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 + 0.10	0.018 + 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

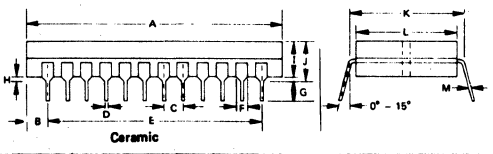
DL170



ITEM	MILLIMETERS	INCHES
A	30.78 Max	1.21 Max
B	1.42	0.06
C	2.54	0.10
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94	1.10
F	1.02	0.04
G	3.2 Min	0.13 Min
H	1.02	0.04
I	3.23	0.13
J	4.25 Max	0.17 Max
K	15.24	0.60
L	14.93	0.59
M	0.25 ± 0.05	0.010 ± 0.002

DL171

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$



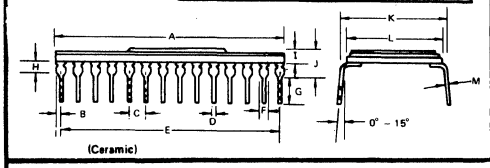
Ceramic

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

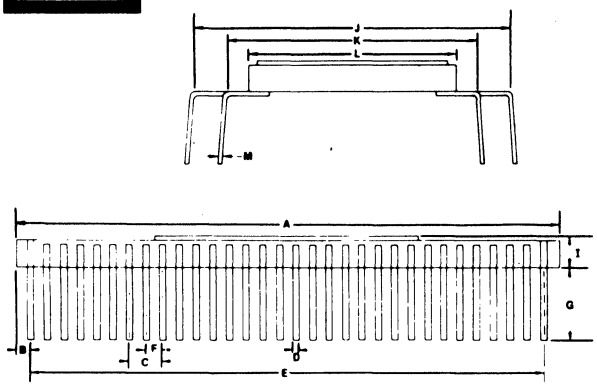
DL172

ITEM	MILLIMETERS	INCHES
A	36.0 MAX	1.41 MAX
B	1.5 MAX	0.059 MAX
C	2.54	0.1
D	0.50 ± 0.1	0.02 ±0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX	0.13 MAX
J	5.2 MAX	0.20 MAX
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004



(Ceramic)

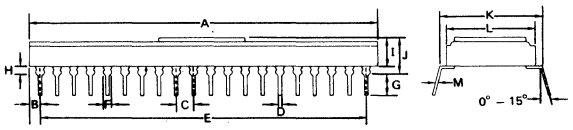
DL173



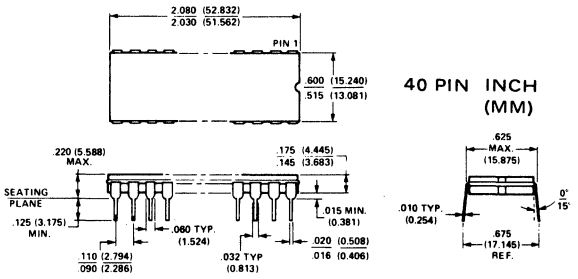
ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002

DL174

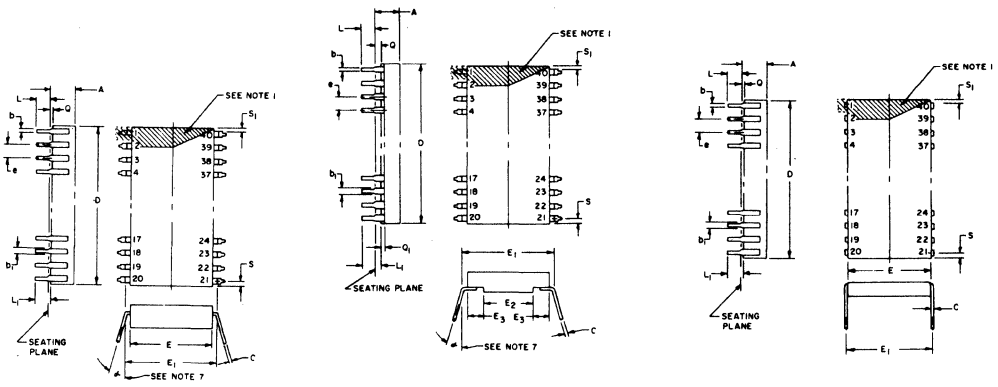
ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.024 MAX
B	1.62	0.064
C	2.54	0.100
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26	1.90
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.5	0.531
M	0.30 ± 0.1	0.012 ± 0.004



DL175



DL176



CONFIGURATION 1 | CONFIGURATION 2 (SEE NOTE 10) | CONFIGURATION 3

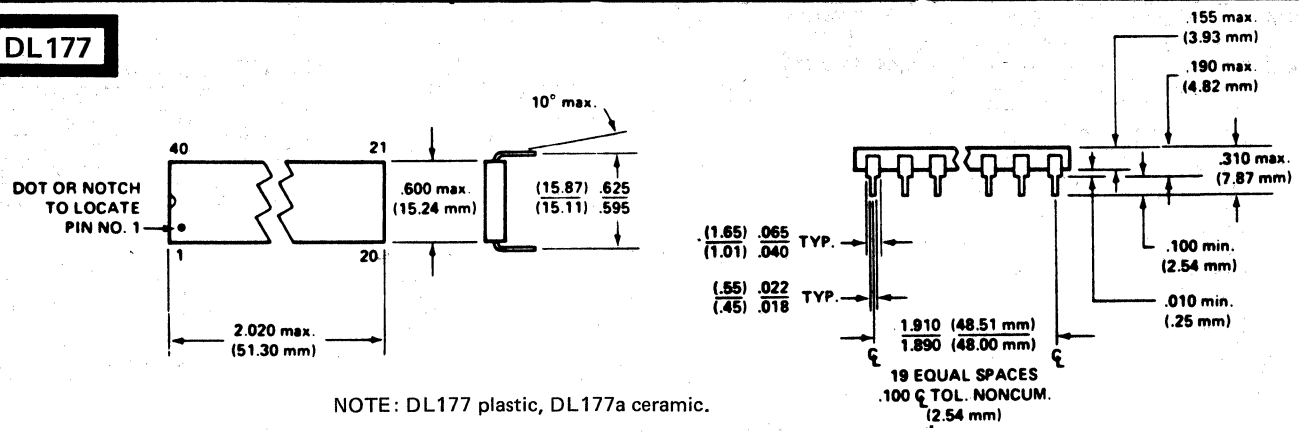
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	---	.225	---	5.72	
b	.014	.023	.36	.58	8
b_1	.030	.070	.76	1.78	2,8
c	.008	.015	.20	.38	8
D	---	2.080	---	52.83	4
E	.510	.615	12.95	15.62	4
E_1	.520	.625	13.21	15.88	7
E_2	.280	---	7.11	---	
E_3	.050	---	1.27	---	
e	.100 BSC		2.54 BSC		5,9
L	.120	.200	3.05	5.08	
L_1	.150	---	3.81	---	
Q	.020	.060	.51	1.52	3
Q_1	.020	---	.51	---	
S	---	.080	---	2.03	6
S_1	.005	---	.13	---	6
S_2	.005	---	.13	---	
α	0°	15°	0°	15°	

NOTES:
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be .020 (.51 mm) for leads number 1, 20, 21 and 40 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact logitudinal position relative to pins 1 and 40.
6. Applies to all four corners (leads number 1, 20, 21 and 40), and 40.5 shall apply.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads (see 40.4 of this appendix).
8. All leads - increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
9. Thirty eight spaces.
10. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

20. OUTLINE DRAWINGS

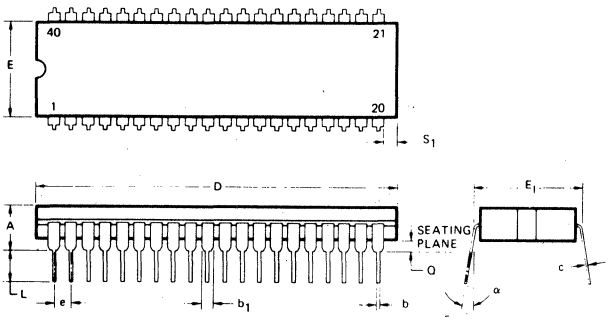
IN DRAWING NUMBER SEQUENCE

DL177



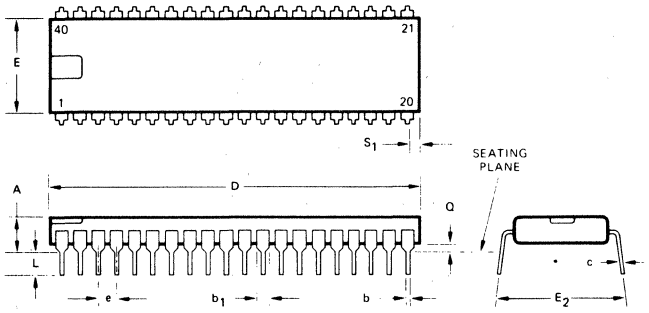
NOTE: DL177 plastic, DL177a ceramic.

DL178



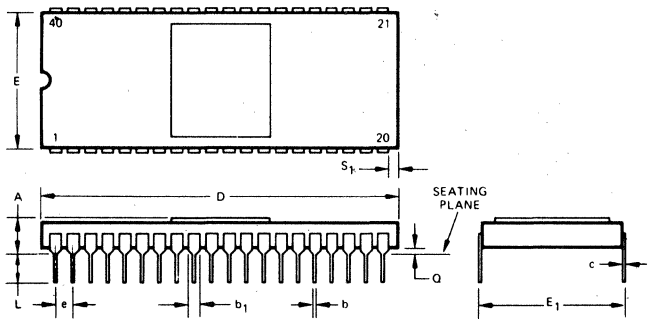
Reference Symbol	Inches	
	Min.	Max.
A	.150	.225
b	.016	.020
b_1	.045	.065
c	.009	.011
D	2.020	2.100
E	.510	.550
E_1	.600	.630
e	.090	.110
L	.120	.150
Q	.015	.060
S_1	.005	

DL179



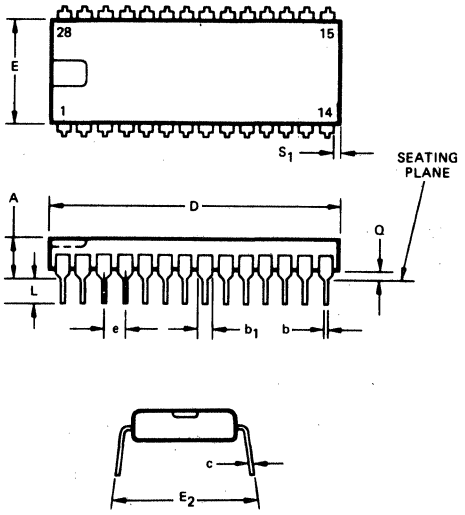
Reference Symbol	Inches	
	Min.	Max.
A	.150	.200
b	.015	.020
b_1	.055	.065
c	.009	.011
D	2.050	2.080
E	.530	.550
E_2	.585	.700
e	.090	.110
L	.015	.060
Q	.015	.060
S_1	.040	.070

DL180



Reference Symbol	Inches	
	Min.	Max.
A	.100	.200
b	.015	.022
b_1	.030	.060
c	.008	.013
D	1.960	2.040
E	.550	.610
E_1	.590	.620
e	.090	.110
L	.120	.160
Q	.020	.060
S_1	.005	

DL181

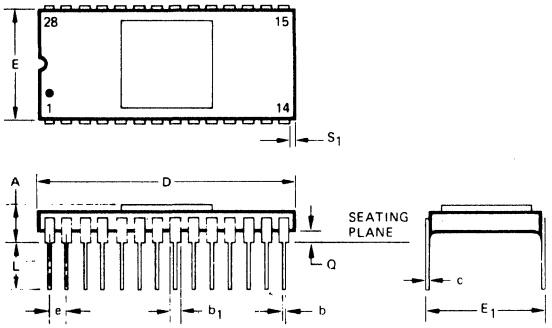


Reference Symbol	Inches	
	Min.	Max.
A	.150	.200
b	.015	.020
b_1	.055	.065
c	.009	.011
D	1.450	1.440
E	.530	.550
E_2	.585	.700
e	.090	.110
L	.125	.160
Q	.015	.060
S_1	.040	.070

20. OUTLINE DRAWINGS

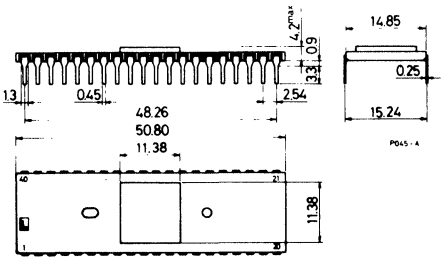
IN DRAWING NUMBER SEQUENCE

DL182

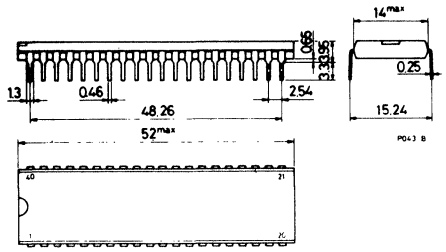


Reference Symbol	Inches	
	Min.	Max.
A	.100	.200
b	.015	.022
b_1	.030	.060
c	.008	.013
D	1.380	1.420
E	.560	.600
E_1	.580	.620
e	.090	.110
L	.120	.160
Q	.020	.060
S_1*	.005	
α	0	0

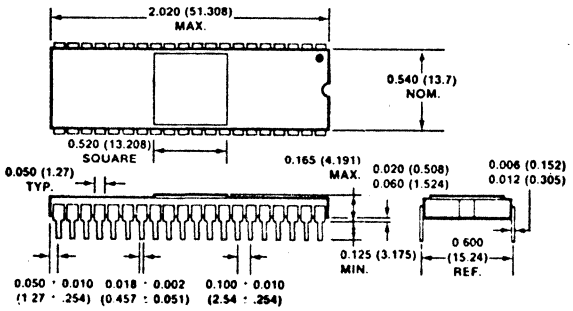
DL183



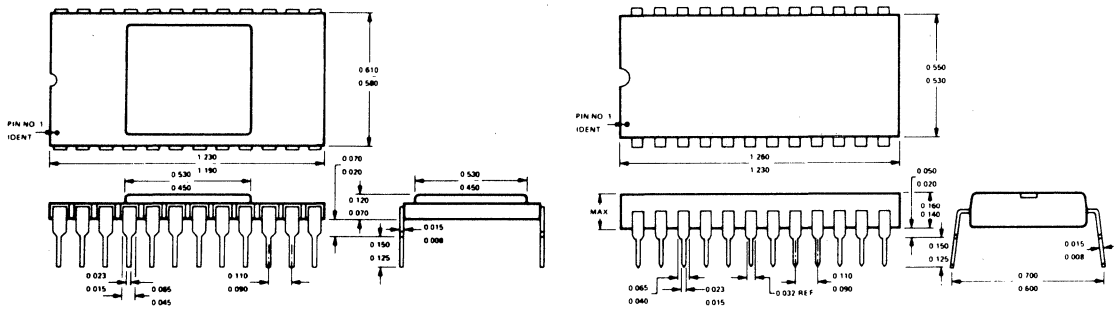
DL184



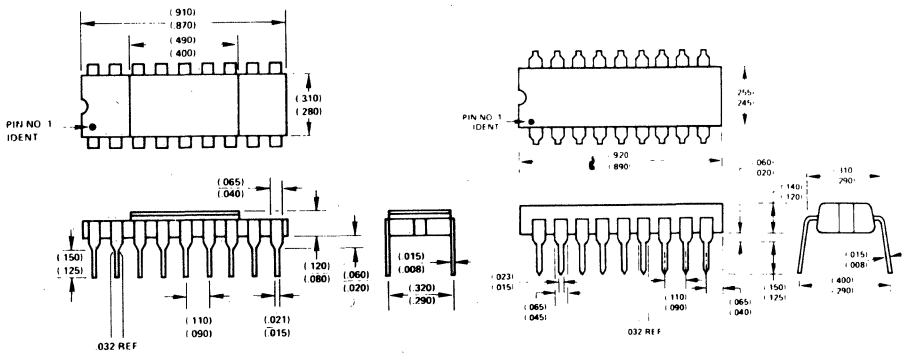
DL185



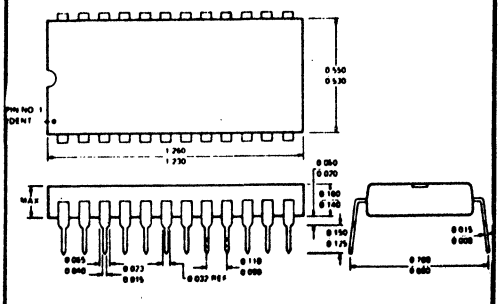
DL186



DL187



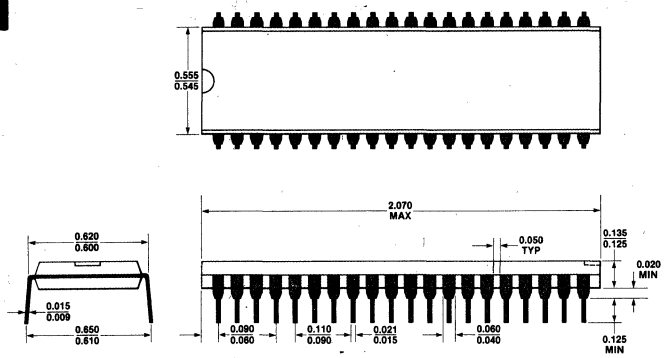
DL188



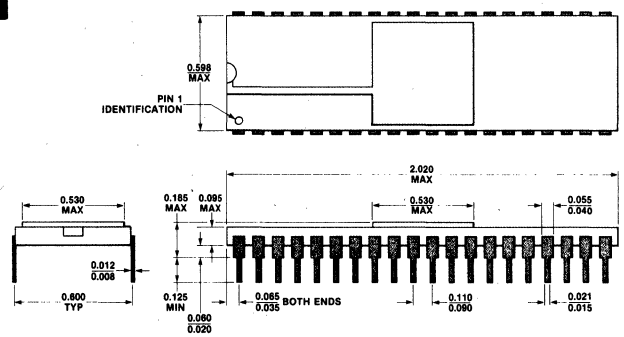
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

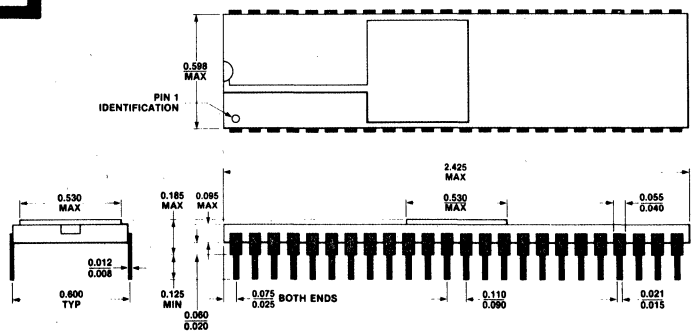
DL189



DL190

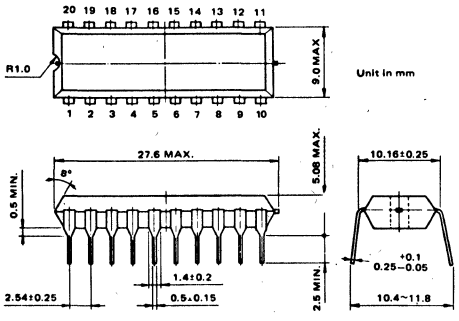


DL191

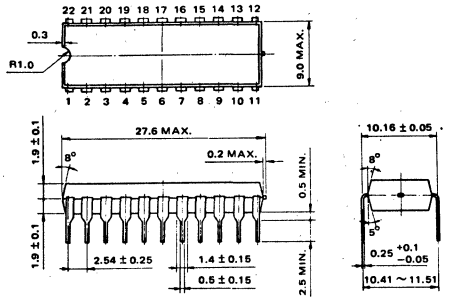


DL192

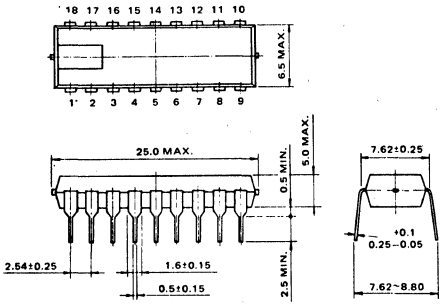
DL193



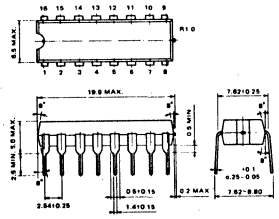
DL194



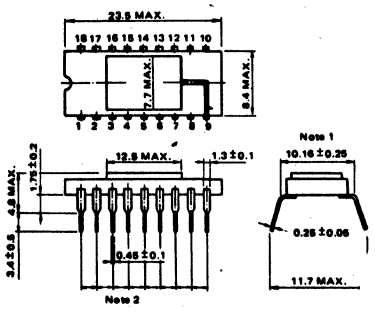
DL195



DL196



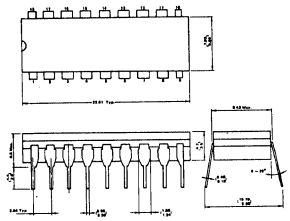
DL197



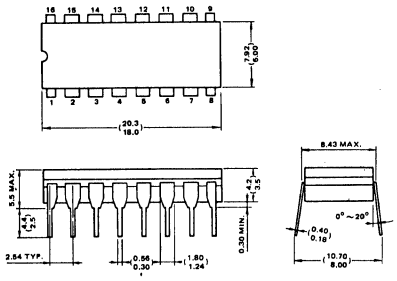
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

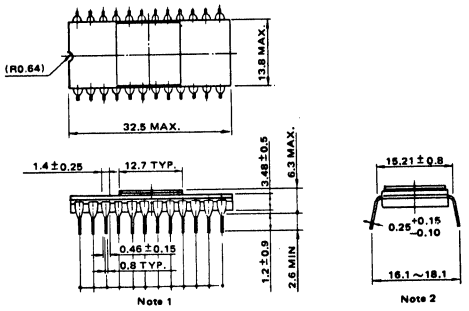
DL198



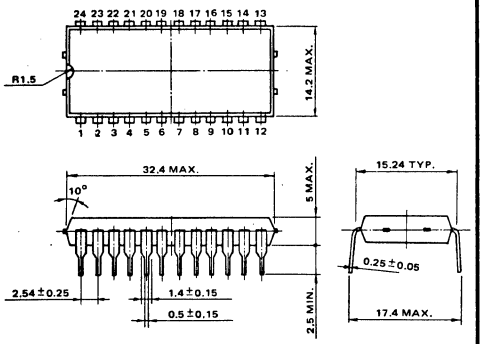
DL199



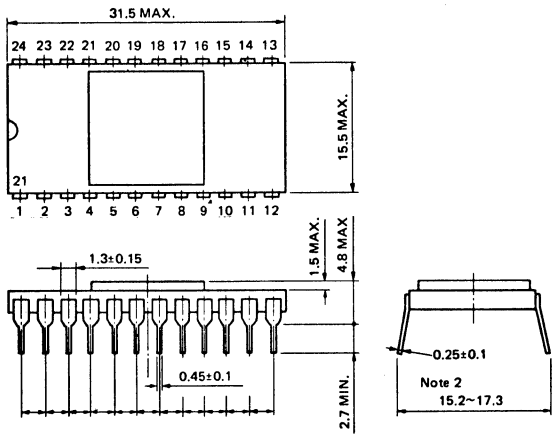
DL200



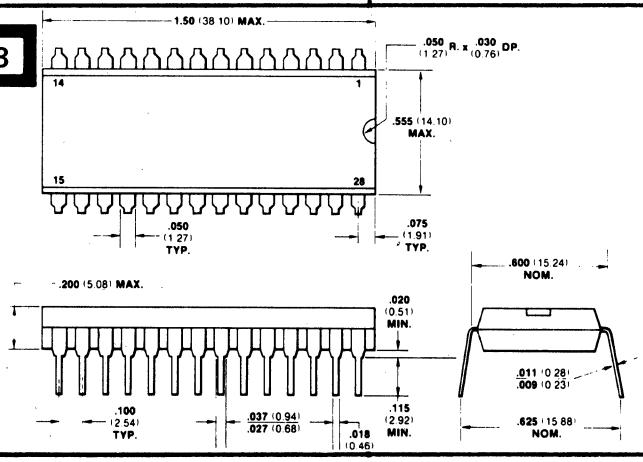
DL201



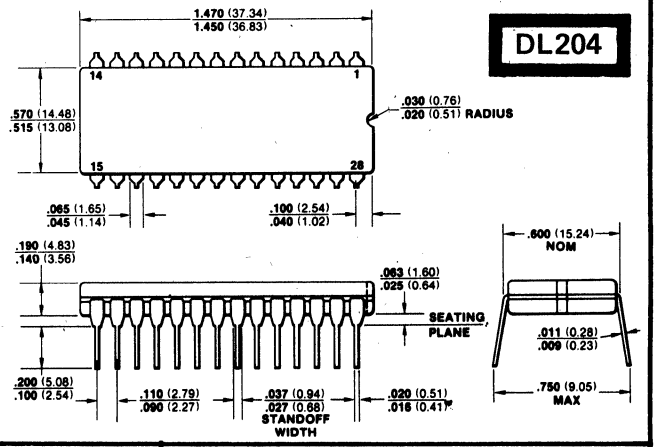
DL202



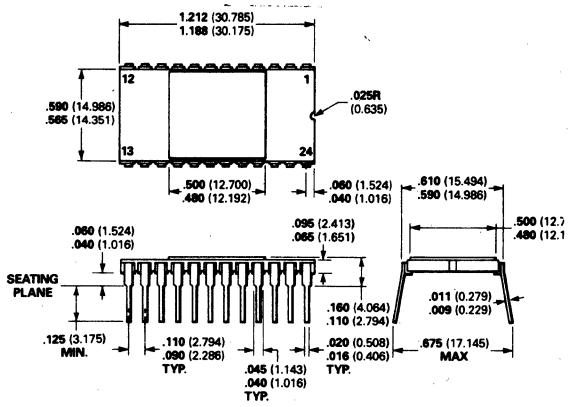
DL203



DL204



DL205

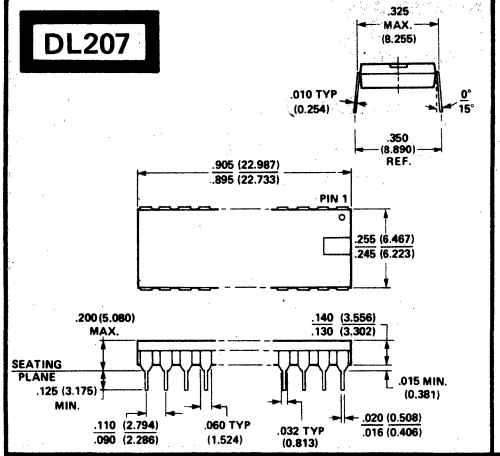


DL206

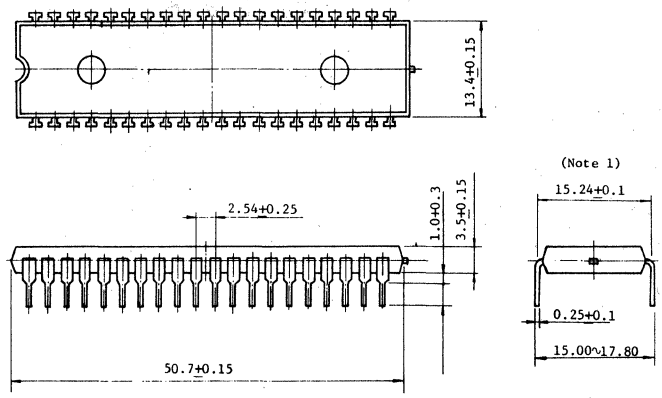
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

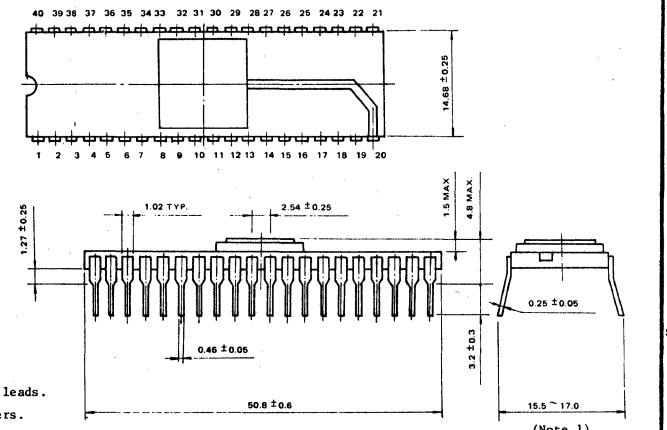
DL207



DL208



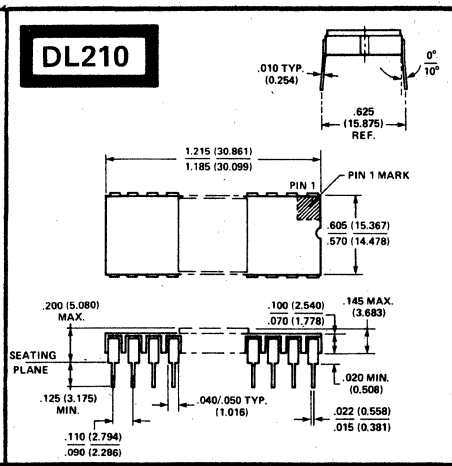
DL209



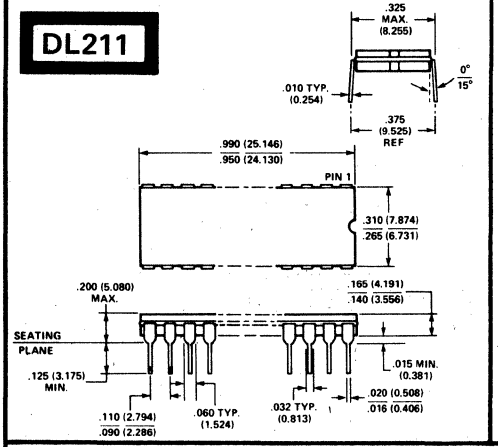
Note 1. This dimension shows spread of leads.

2. All dimensions are in millimeters.

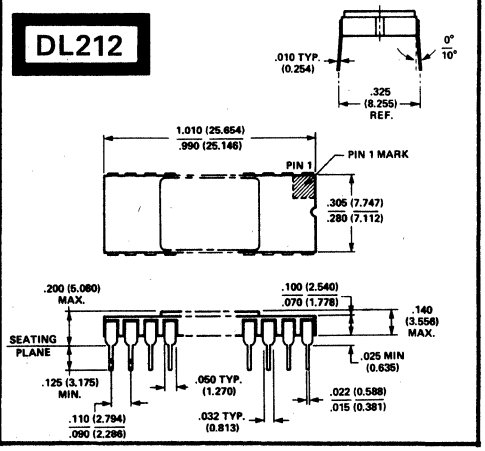
DL210

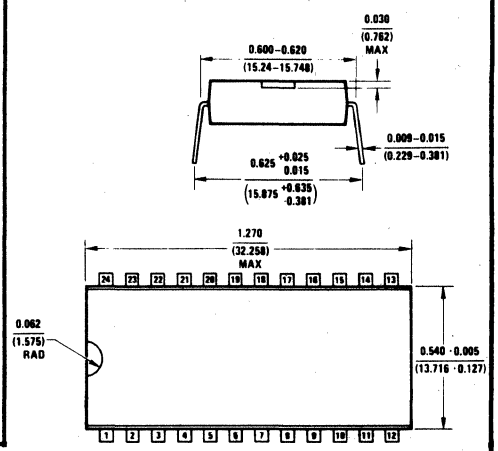


DL211

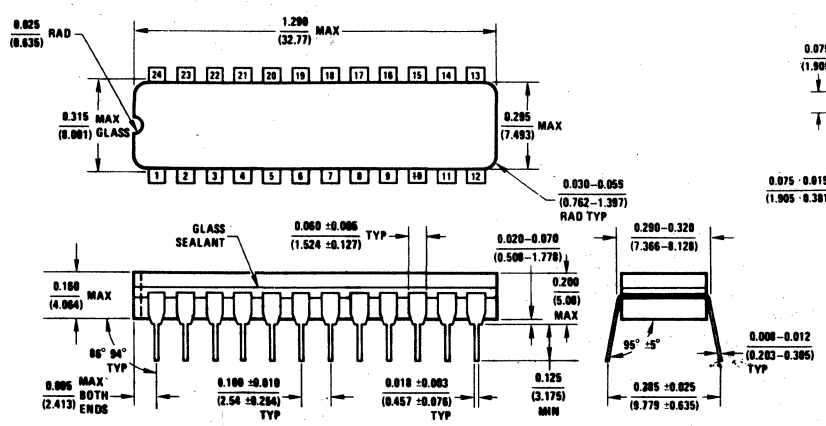


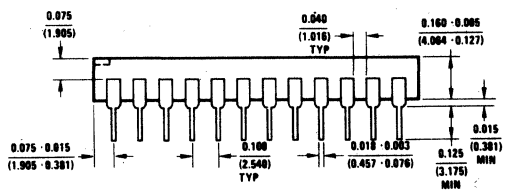
DL212





DL213

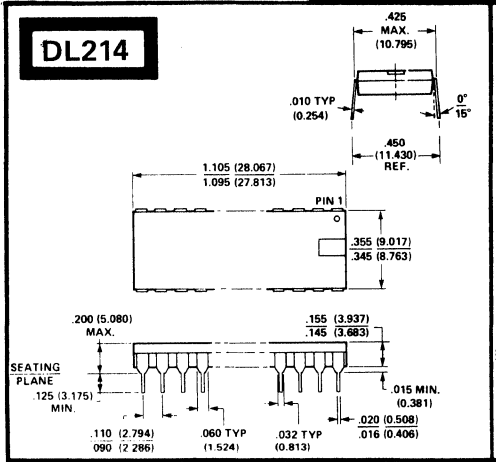




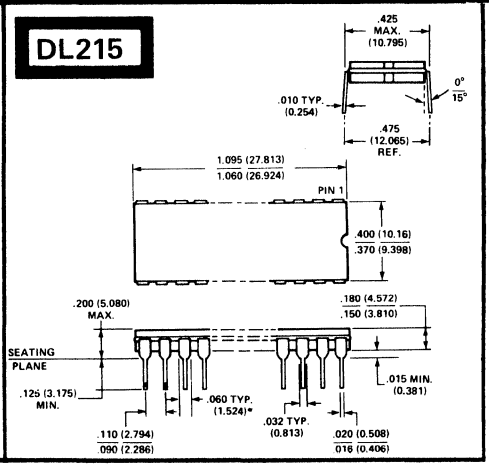
20. OUTLINE DRAWINGS

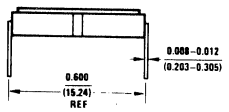
IN DRAWING NUMBER SEQUENCE

DL214

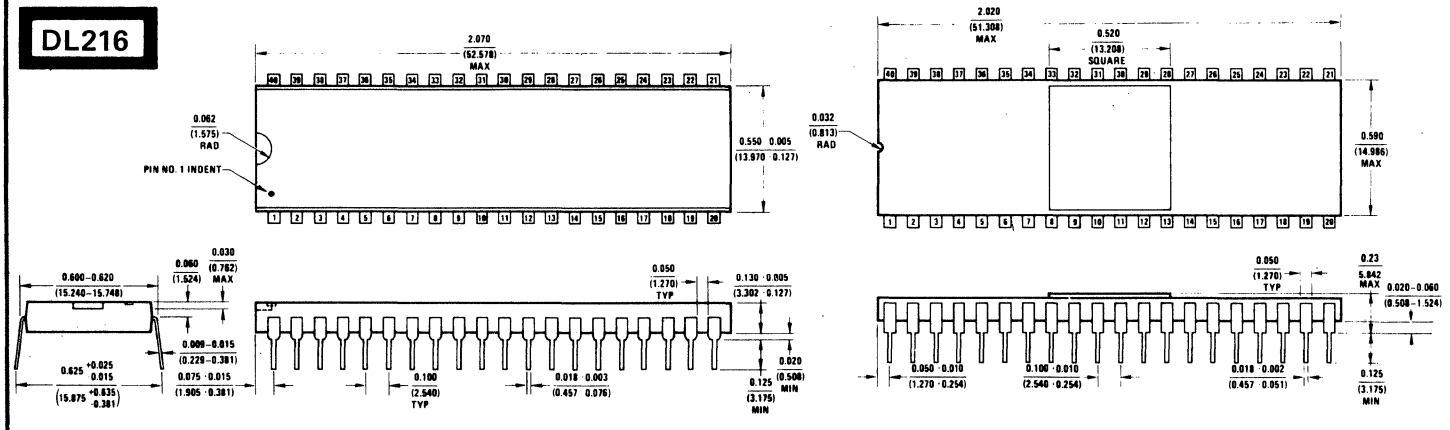


DL215

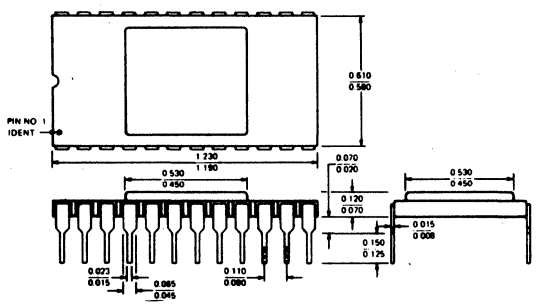




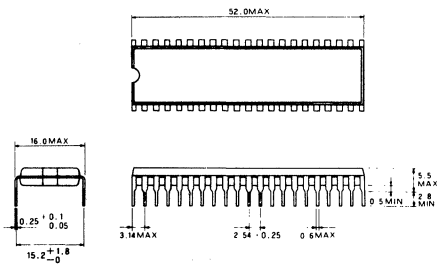
DL216



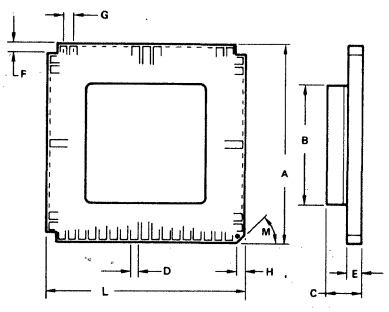
DL217



DL218



DL219



NOTES:
1. DIMENSIONS A AND L ARE DATUMS.
2. POSITIONAL TOLERANCES FOR COVER:

⌖	0.25 (0.010) Ⓜ	A Ⓜ	L Ⓜ

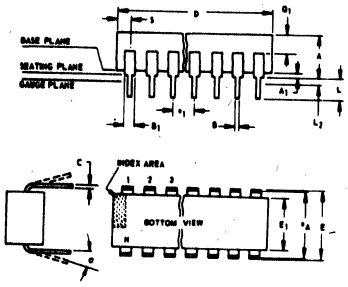
3. DIMENSION D - 68 PLACES
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.00	24.51	0.945	0.965
B	14.22	14.73	0.560	0.580
C	–	4.57	–	0.180
D	0.84	0.99	0.033	0.039
E	1.27	1.78	0.050	0.070
F	1.14	1.40	0.045	0.055
G	1.27 BSC		0.050 BSC	
H	0.89	1.14	0.035	0.045
L	24.00	24.51	0.945	0.965
M	45° NOM		45° NOM	

20. OUTLINE DRAWINGS

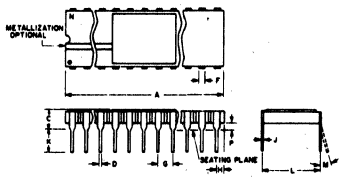
IN DRAWING NUMBER SEQUENCE

DL220



SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	2.000	2.090		50.80	53.09
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	40		5	40	
N_1	0		6	0	
Q_1	0.085	0.095		1.66	2.41
S	0.040	0.100		1.02	2.54

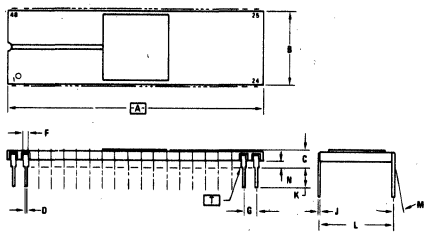
DL221



SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	1.980	2.020		50.30	51.30
C	0.095	0.155		2.43	3.93
D	0.017	0.023		0.43	0.56
F	0.050 REF.			1.27 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	40			40	

DL230

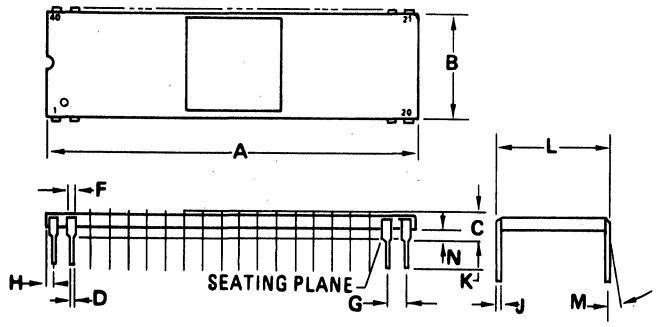
PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

NOTES:
1. DIMENSION [A] IS DATUM.
2. POSTIONAL TOLERANCE FOR LEADS:
   [⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ]
3. [T] IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

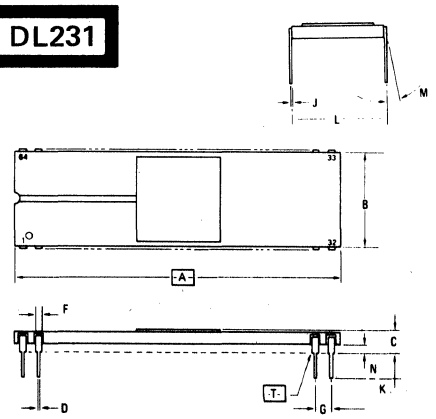
DL228



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.94	15.34	0.588	0.604
C	3.05	4.06	0.120	0.160
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10°		10°
N	1.02	1.52	0.040	0.060

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX MAT'L CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

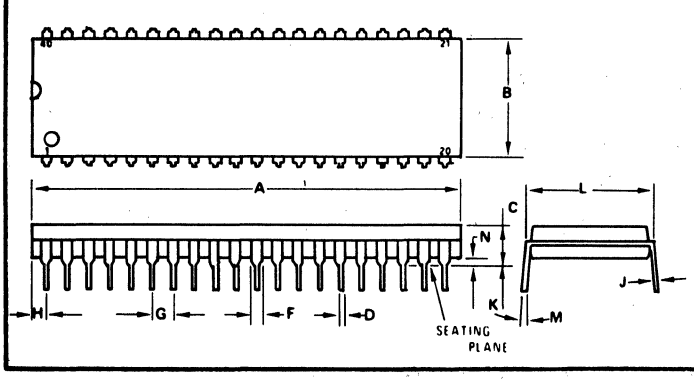
DL231



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	80.52	82.04	3.170	3.230
B	22.25	22.96	0.876	0.904
C	3.05	4.32	0.120	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	22.61	23.11	0.890	0.910
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

NOTES:
1. DIMENSION [A] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   [⌖ 0.25 (0.010) Ⓜ T A Ⓜ]
3. [T] IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DL229



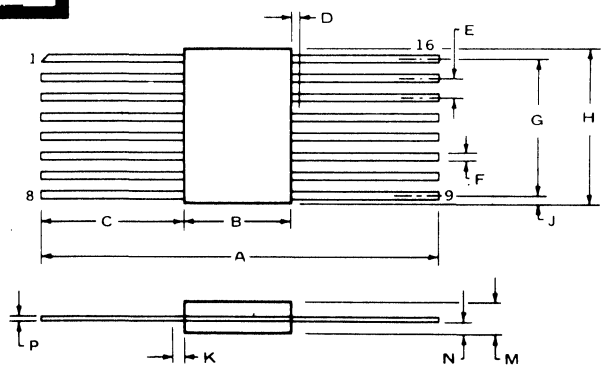
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

20. OUTLINE DRAWINGS

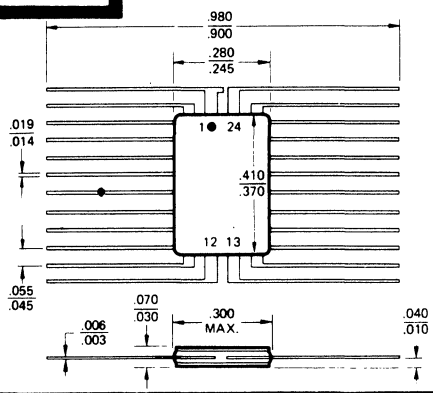
IN DRAWING NUMBER SEQUENCE

FP1

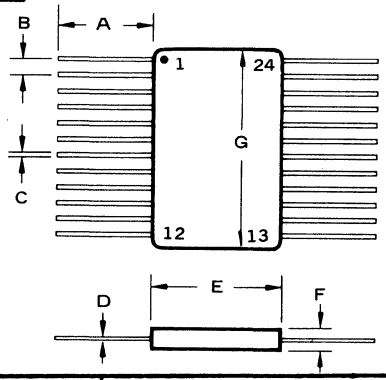


	A	B	C	D	E	F	G	H	J	K	M	N	P
FP1	.940 .960	.245 .275	.330 .370	.020	.045 .055	.015 .019	.340 .360	.370 .395	.010 .025	.030	.060 .080	.020 .040	.004 .006
FP1a	.900 .980	.245 .280	.250 MIN		.045 .055	.015 .019		.370 .390			.050 .070	.010 .040	.003 .007
FP1b	.745 .980	.245 .280	.250 .350		.050 TYP	.015 .019		.370 .410			.060 .085	.038 TYP	.004 .006
FP1c	.845 .990	.248 .290	.310 .350		.045 .055	.015 .020		.373 .400	.000 .027		.045 .080	.015 .040	.003 .007

FP2



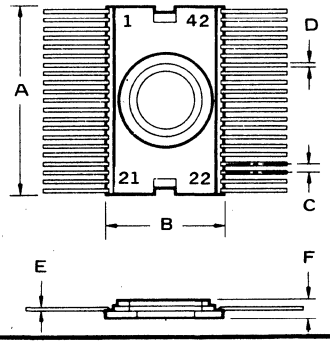
FP3



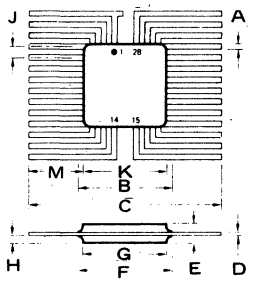
	A	B	C	D	E	F	G
FP3	.250 .350	.050 TYP	.015 .019	.004 .006	.365 .395	.065 .090	.620 MAX
FP3a	.265 .320	.045 .055	.015 .019	.004 .006	.360 .385	.050 .090	.580 .620

FP4

	A	B	C	D	E	F
FP4	1.05 1.07	.634 .646	.045 .055	.018 .022	.007 .010	.071 .091
FP4a	1.03 1.09	.620 .660	.045 .055	.017 .023	.006 .012	.070 .115

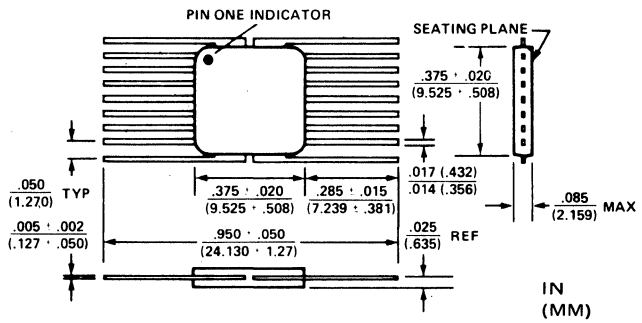


FP5



	A	B	C	D	E	F	G	H	J	K	M
FP5	.016 .018	.400	.865	.004 .005	.045 .065	.400	.375 TYP	.375 TYP	.045 .055		
FP5a	.015 .019	.410	.955	.003 .006	.045 .080	.410	.360 .410	.010 .040	.045 .055	.360 .410	.270 .320

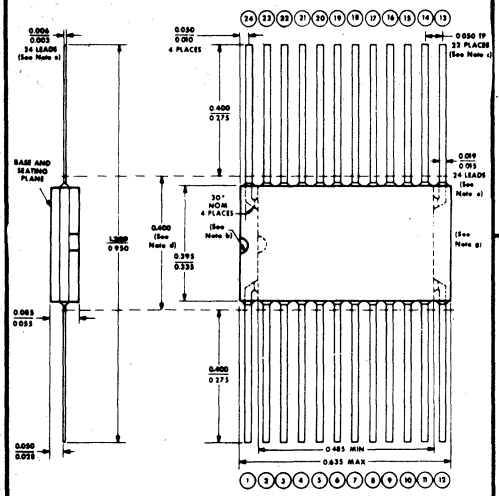
FP6



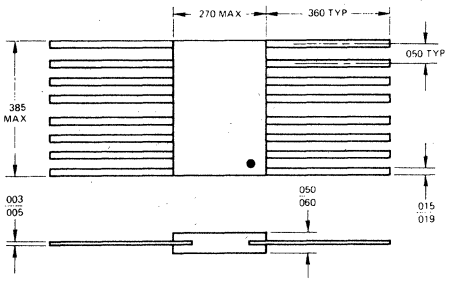
20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

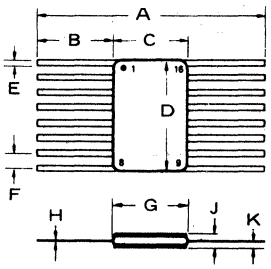
FP7



FP8

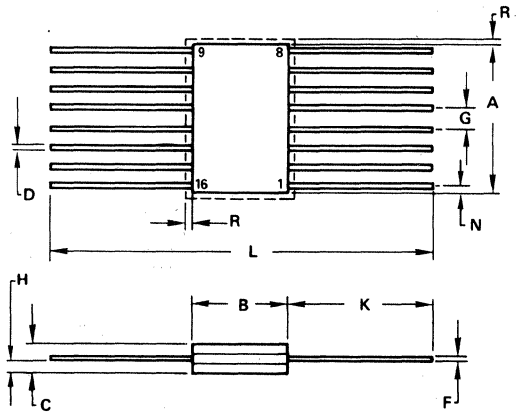


FP9



	A	B	C	D	E	F	G	H	J	K
FP9	.900	.250	.245	.370	.015	.045	.300	.003	.050	.010
	.960	MIN	.280	.390	.019	.055	MAX	.007	.070	.040
FP9a	.930	.270	.355	.355	.017	.050	.355	.004	.085	.025
	.970	.300	.395	.395	.019	TYP	.395	.006	MAX	REF

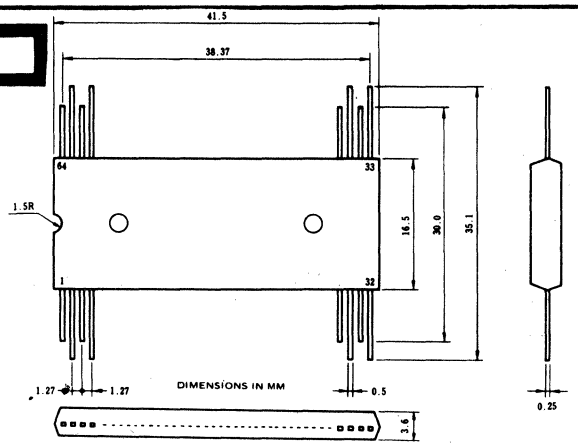
FP10



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	6.60	0.245	0.260
C	1.52	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

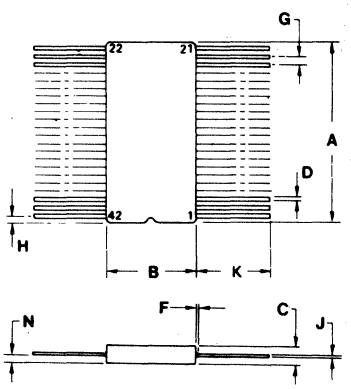
NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

FP11



FP13

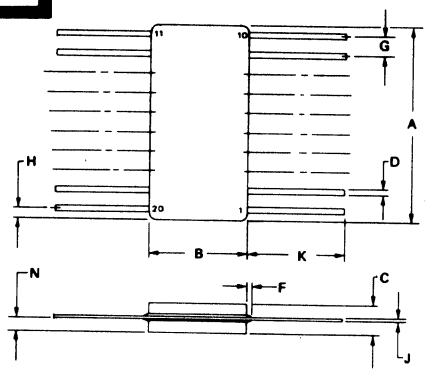
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.92	27.60	1.060	1.090
B	13.72	14.22	0.540	0.560
C	2.41	3.18	0.095	0.125
D	0.43	0.53	0.017	0.023
F	–	0.38	–	0.015
G	1.27 BSC		0.050 BSC	
H	0.89	1.14	0.035	0.045
J	0.20	0.30	0.008	0.012
K	–	11.94	–	0.470
N	–	1.27	–	0.050



20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

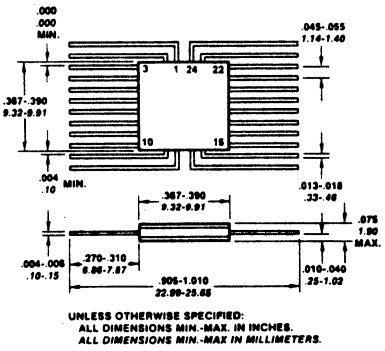
FP14



NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	13.08	–	0.515
B	5.84	6.60	0.230	0.260
C	1.52	2.16	0.060	0.085
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
H	1.14	1.40	0.045	0.055
J	0.08	0.13	0.003	0.005
K	–	9.14	–	0.360
N	–	1.02	–	0.040

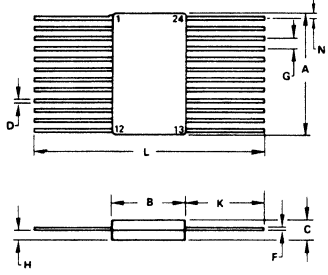
FP15



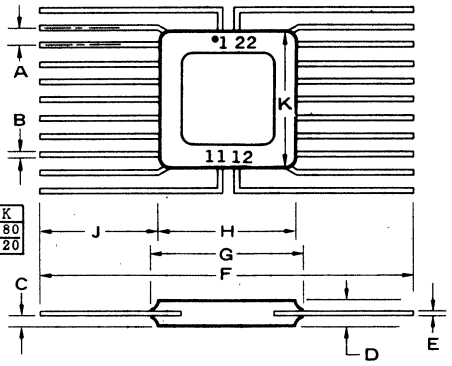
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX IN MILLIMETERS.

FP16

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025



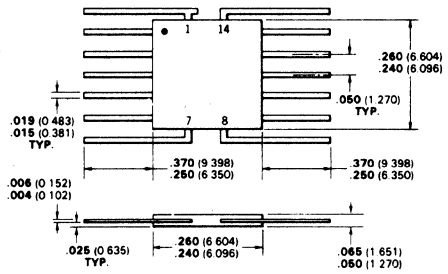
FP18



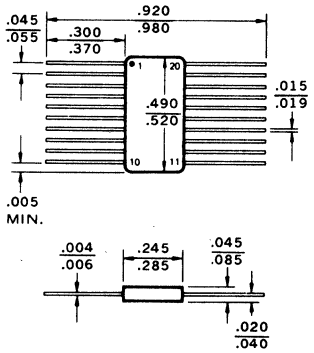
	A	B	C	D	E	F	G	H	J	K
FP18	.045 .055	.015 .019	.010 .040	.045 .090	.003 .006	.920 .980	.440 MAX	.380 .420	.250 .320	.380 .420

FP19

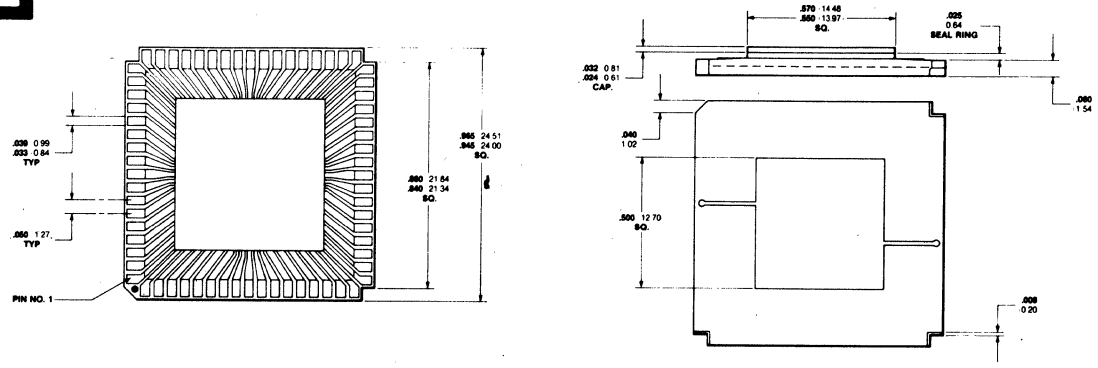
INCH (MM)



FP20



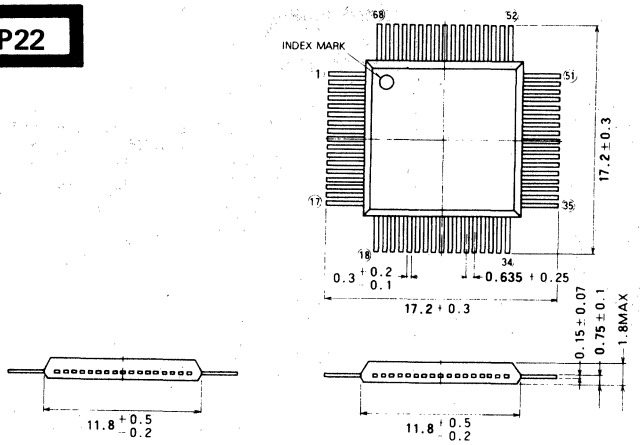
FP21



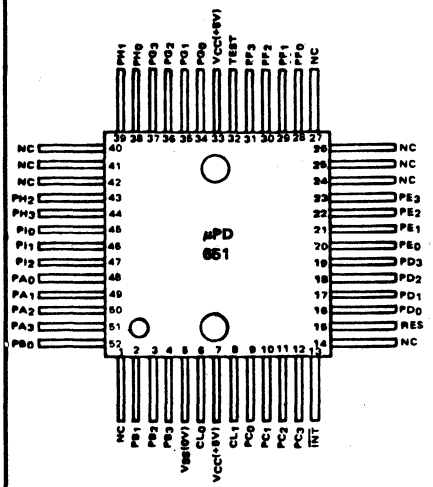
20. OUTLINE DRAWINGS

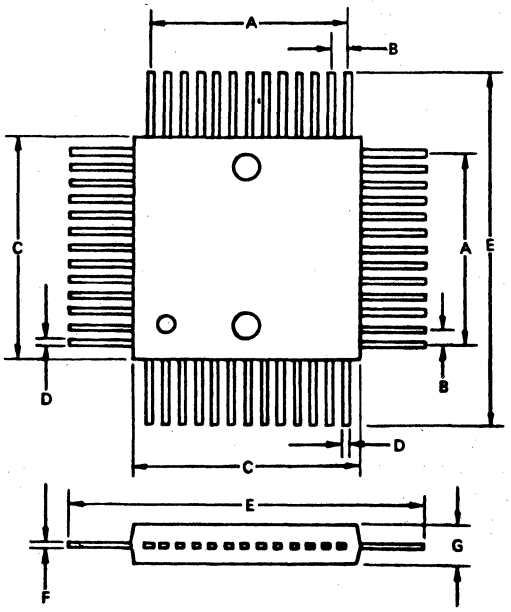
IN DRAWING NUMBER SEQUENCE

FP22



FP23



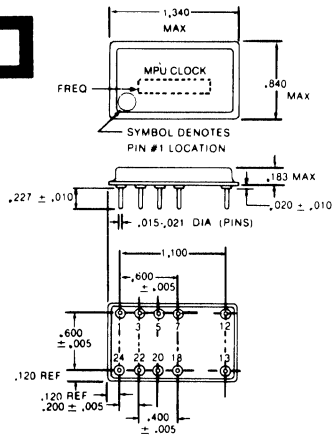


ITEM	MILLIMETERS	INCHES
A	12.0 MAX.	0.47 MAX.
B	1.0 ± 0.1	0.04 ± 0.004
C	14.0	0.55
D	0.4	0.016
E	21.8 ± 0.4	0.86 ± 0.016
F	0.15	0.006
G	2.6	0.1

20. OUTLINE DRAWINGS

IN DRAWING NUMBER SEQUENCE

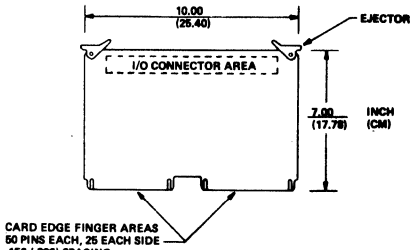
MD1



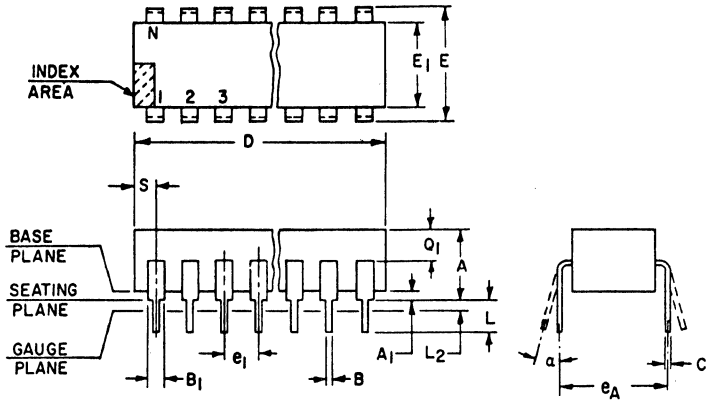
MD2

	DIMENSIONS
MD2	3x4.5
MD2a	2.00x3.00
MD2b	6.30x9.20
MD2c	4.5x4.5
MD2d	4.5x9.25x.062
MD2e	9.13x7.48
MD2f	4.5x8
MD2g	7.48x13.48
MD2h	7.48x10.7
MD2j	2.0x2.0x.2
MD2k	7.0x7.5
MD2m	7.0x8.5
MD2n	4.406x3.28x.610
MD2p	4.5x4.0x.50
MD2q	9.75x5.75
MD2r	4.5x6.5

MD3



MO001

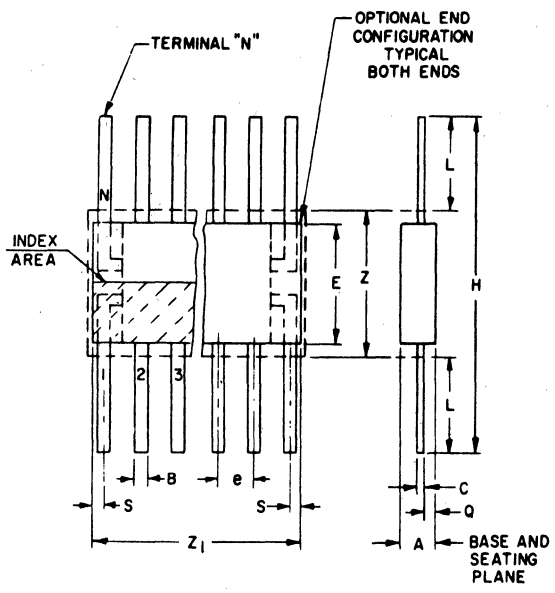


	A	A1	B	B1	C	D	E	E1	e1	eA	L	L2	a	N	N1	Q1	S	NOTES
MO001AA	.200 MAX	.020 MIN	.015 .023	.030 .070	.008 .015	.660 .785	.325 MAX	.220 .260	.100 T.P.	.300 T.P.	.100 MIN	.000 .030	0° 15°	14	0			1,9
NOTES								7	2,3	2,3			4	5	6			
MO001AB	.155 .200	.020 .050	.014 .020	.050 .065	.008 .012	.745 .770	.300 .325	.240 .260	.100 T.P.	.300 T.P.	.125 .150	.000 .030	0° 15°	14	0	.040 .075	.065 .090	1,9
NOTES								7	2,3	2,3			4	5	6			
MO001AC	.155 .200	.020 .050	.014 .020	.035 .065	.008 .012	.745 .785	.300 .325	.240 .260	.100 T.P.	.300 T.P.	.125 .150	.000 .030	0° 15°	16	0	.040 .075	.015 .060	1,9
NOTES								7	2,3	2,3			4	5	6			
MO001AD	.120 .160	.020 .065	.014 .020	.050 .065	.008 .012	.745 .770	.300 .325	.240 .260	.100 T.P.	.300 T.P.	.125 .150	.000 .030	0° 15°	14	0	.050 .085	.065 .090	1,9
NOTES								7	2,3	2,3			4	5	6			
MO001AE	.120 .160	.020 .065	.014 .020	.035 .065	.008 .012	.745 .785	.300 .325	.240 .260	.100 T.P.	.300 T.P.	.125 .150	.000 .030	0° 15°	16	0	.050 .085	.015 .060	1,9
NOTES								7	2,3	2,3			4	5	6			
MO001AF	.165 .210	.015 .045	.015 .020	.045 .070	.009 .011	.750 .795	.295 .325	.245 .300	.100 T.P.	.300 T.P.	.120 .160	.000 .030	2° 15°	14	0	.050 .080	.050 .110	1,9
NOTES								7	2,3	2,3			4	5	6			
MO001AG	.165 .210	.015 .045	.015 .020	.045 .070	.009 .011	.750 .795	.295 .325	.245 .300	.100 T.P.	.300 T.P.	.120 .160	.000 .030	2° 15°	16	0	.050 .080	.010 .060	1,9
NOTES								7	2,3	2,3			4	5	6			

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5-1973.
3. Leads within .127 radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
4. e_1 and e_A applies in zone L_2 when unit installed.
5. α applies to spread leads prior to installation.
6. N is the maximum quantity of lead positions.
7. N_1 is the allowable quantity of missing leads.
8. E_1 does not include mold flash.
9. Outlines on which the seating plane is coincident with the base plane (A_1 = 0) terminal lead stand-offs are not required, and B_1 may equal B along any part of the lead above the seating/base plane.
10. Controlling Dimension: INCH

MO004

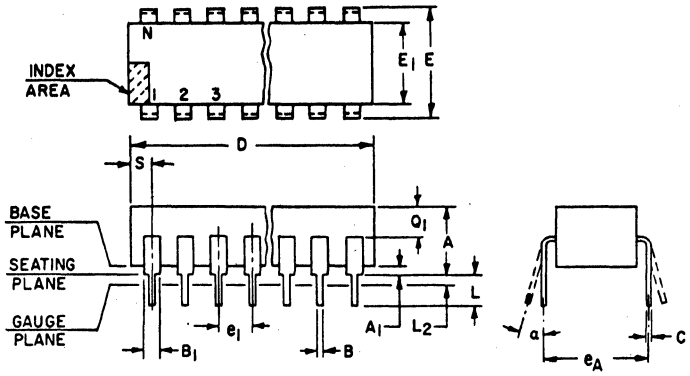


NOTES:

1. Refer to Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within .005 radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.
5. Controlling Dimensions: INCH

	A	B	C	e	E	H	L	N	Q	S	Z	Z_1	NOTES
MO004AA	.008 / .100	.015 / .019	.003 / .006	.050 TP	.200 / .300	.600 / 1.000	.150 / .350	14	.005 / .050	.000 / .025	.300	.350	1,5
NOTES		1	1	2				3		1	4	4	
MO004AB	.008 / .100	.013 / .017	.003 / .006	.050 TP	.200 / .300	.600 / 1.000	.150 / .350	14	.005 / .050	.000 / .025	.300	.350	1,5
NOTES		1	1	2				3		1	4	4	
MO004AC	.008 / .100	.015 / .019	.003 / .006	.050 TP	.200 / .300	.600 / 1.000	.150 / .350	14	.000 / .097	.000 / .025	.300	.350	1,5
NOTES		1	1	2				3		1	4	4	
MO004AD	.008 / .100	.015 / .019	.003 / .006	.050 TP	.200 / .300	.600 / 1.000	.150 / .350	10	.005 / .050	.000 / .050	.300	.300	1,5
NOTES		1	1	2				3		1	4	4	
MO004AE	.008 / .100	.015 / .019	.003 / .006	.050 TP	.200 / .300	.600 / 1.000	.150 / .350	10	.005 / .050	.000 / .025	.300	.250	1,5
NOTES		1	1	2				3		1	4	4	
MO004AF	.008 / .100	.015 / .019	.003 / .006	.050 TP	.200 / .300	.600 / 1.000	.150 / .350	14	.005 / .050	.000 / .050	.300	.400	1,5
NOTES		1	1	2				3		1	4	4	
MO004AG	.008 / .100	.015 / .019	.003 / .006	.050 TP	.200 / .300	.600 / 1.000	.150 / .350	14	.005 / .050	.000 / .025	.300	.400	1,5
NOTES		1	1	2				3		1	4	4	
MO004AH	.008 / .100	.015 / .019	.003 / .006	.050 TP	.200 / .300	.600 / 1.000	.150 / .350	16	.005 / .050	.000 / .050	.300	.450	1,5
NOTES		1	1	2				3		1	4	4	

MO015



	A	A1	B	B1	C	D	E	E1	e1	eA	L	L2	a	N	N1	Q1	S	NOTES
MO015AA	.120 .250	.020 .070	.016 .020	.028 .070	.008 .012	1.200 1.290	.600 .625	.515 .580	.100 TP	.600 TP	.100 .200	.000 .030	0° 15°	24	0	.040 .075	.040 .100	1,2,10
NOTES								8	3,4	3,4			5	6	7			
MO015AB	.120 .250	.020 .070	.016 .020	.028 .070	.008 .012	.700 .840	.600 .625	.515 .580	.100 TP	.600 TP	.100 .200	.000 .030	0° 15°	16	0	.040 .075	.040 .100	1,2,10
NOTES								8	3,4	3,4			5	6	7			
MO015AC	.120 .250	.020 .070	.016 .020	.028 .070	.008 .012	1.800 1.890	.600 .625	.515 .580	.100 TP	.600 TP	.100 .200	.000 .030	0° 15°	36	0	.065 .105	.040 .100	1,2,10
NOTES								8	3,4	3,4			5	6	7			
MO015AD	.100 .200	.000 .070	.015 .020	.015 .055	.008 .012	1.170 1.210	.600 .625	.515 .580	.100 TP	.600 TP	.100 .200	.000 .030	0° 15°	24	0	.020 .080	.025 .050	1,2,10
NOTES	9							8	3,4	3,4			5	6	7			
MO015AE	.100 .200	.000 .070	.015 .020	.015 .055	.008 .012	.770 .810	.600 .625	.515 .580	.100 TP	.600 TP	.100 .200	.000 .030	0° 15°	16	0	.020 .080	.025 .050	1,2,10
NOTES	9							8	3,4	3,4			5	6	7			
MO015AF	.100 .200	.000 .070	.015 .020	.015 .055	.008 .012	1.770 1.810	.600 .625	.515 .580	.100 TP	.600 TP	.100 .200	.000 .030	0° 15°	36	0	.020 .080	.025 .050	1,2,10
NOTES	9							8	3,4	3,4			5	6	7			
MO015AG	.090 .200	.020 .070	.014 .020	.050 .054	.008 .012	1.220 1.290	.600 .625	.520 .550	.100 TP	.600 TP	.125 .150	.000 .030	0° 15°	24	0	.020 .060	.050 .100	1,2,10
NOTES								8	3,4	3,4			5	6	7			
MO015AH	.090 .200	.000 .070	.015 .020	.015 .055	.008 .012	1.380 1.420	.600 .625	.485 .515	.100 TP	.600 TP	.100 .200	.000 .030	0° 15°	28	0	.020 .070	.040 .070	1,2,10
NOTES	9							8	3,4	3,4			5	6	7			
MO015AJ	.100 .200	.000 .070	.015 .020	.015 .055	.008 .012	1.980 2.020	.600 .625	.485 .515	.100 TP	.600 TP	.100 .200	.000 .030	0° 15°	40	0	.020 .070	.040 .070	1,2,10
NOTES	9							8	3,4	3,4			5	6	7			
MO015AK	.145 .175	.030 .050	.015 .020	.040 .050	.008 .015	1.240 1.260	.600 .625	.540 .560	.100 TP	.600 TP	.100 .140	.000 .030	0° 15°	24	0	.045 .075	.065 .085	1,2,10
NOTES								8	3,4	3,4			5	6	7			
MO015AL	.090 .140	.020 .065	.015 .020	.045 .055	.008 .012	1.350 1.430	.600 .625	.480 .520	.100 TP	.600 TP	.100 .180	.000 .030	0° 15°	28	0	.020 .080	.020 .060	1,2,10
NOTES								8	3,4	3,4			5	6	7			
MO015AM	.090 .140	.020 .065	.015 .020	.045 .055	.008 .012	1.950 2.020	.600 .625	.480 .520	.100 TP	.600 TP	.100 .180	.000 .030	0° 15°	40	0	.020 .080	.020 .060	1,2,10
NOTES								8	3,4	3,4			5	6	7			
MO015AN	.090 .150	.020 .065	.015 .020	.045 .055	.008 .012	1.150 1.220	.600 .625	.480 .520	.100 TP	.600 TP	.100 .180	.000 .030	0° 15°	24	0	.020 .080	.020 .060	1,2,10
NOTES								8	3,4	3,4			5	6	7			

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5-1973.
3. Leads within .127 radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
4. e_1 and e_A applies in zone L_2 when unit installed.
5. α applies to spread leads prior to installation.
6. N is the maximum quantity of lead positions.
7. N_1 is the allowable quantity of missing leads.
8. E_1 does not include mold flash.
9. Outlines on which the seating plane is coincident with the base plane (A_1 = 0) terminal lead stand-offs are not required, and B_1 may equal B along any part of the lead above the seating/base plane.
10. Controlling Dimension: INCH

SECTION 21

MICROCOMPUTER D.A.T.A.BOOK

Manufacturers' Sales Offices

These manufacturers have listed their sales offices in this section for your convenience. Please contact the sales office nearest you for any additional information you may need.

(MANUFACTURERS IN ORDER OF D.A.T.A. CODE LETTERS)

AMD – ADVANCED MICRO DEVICES, INC.

	Zip Code	Telephone No.	TWX/Telex
901 Thompson Place, Sunnyvale, California	94086	408-732-2400	910-339-9280 34-6306

FSC – FAIRCHILD CAMERA & INSTRUMENT CORPORATION

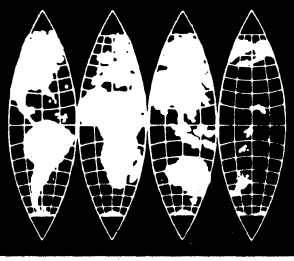
	Zip Code	Telephone No.	TWX/Telex
SEMICONDUCTOR PRODUCTS GROUP 464 Ellis Street, Mountain View, California	94042	415-962-5011	910-379-6435 Cable FAIRSEMCO

ITL – INTEL CORPORATION

	Zip Code	Telephone No.	TWX/Telex
3065 Bowers Avenue, Santa Clara, California	95051	408-987-8080	910-338-0026 34-6372

U. S. SALES OFFICES

CALIFORNIA	Santa Ana	Intel Corporation 2000 East 4th Street No. 105	92701	714-835-9642	910-595-1114



SECTION 21
Manufacturers' Sales Offices

ITL – INTEL CORPORATION

			Zip Code	Telephone No.	TWX/Telex
3065 Bowers Avenue, Santa Clara, California			95051	408-987-8080	910-338-0026
U. S. SALES OFFICES					
ILLINOIS	Rolling Meadows	Intel Corporation 2250 Golf Rd.	60008	312-981-7200	910-651-5881
MASSACHUSETTS	Chelmsford	Intel Corporation 27 Industrial Ave.	01824	617-667-8126	710-343-6333
OHIO	Dayton	Intel Corporation 12675 Research Dr.	45415	513-890-5350	810-450-2528
TEXAS	Dallas	Intel Corporation 2925 LBJ Freeway Suite 175	75234	214-241-9521	910-860-5487
EUROPEAN MARKETING OFFICE					
BELGIUM	Brussels	Intel International Rue du Moulin a Papier 51-Boite 1	B-1160	(02)660 30 10	24814
ORIENT MARKETING OFFICE					
JAPAN	Tokyo	Intel Japan K.K. Flower Hill - Shinmachi E. Building 1-23-9 Shinmachi, Setagaya-ku	154	(03)426-9261	781-28426

ITTG – ITT SEMICONDUCTORS

			Zip Code	Telephone No.	TWX/Telex
INTERMETALL, Post Office Box 840, Freiburg, West Germany			D-7800	761-5171	(07) 72716
JAPAN	Tokyo	ITT Semiconductors Post Office Box 21 Shinjuku-ku	160-91	3478881-5	22858
UNITED KINGDOM	Sidcup (Kent)	ITT Semiconductors H Maidstone Rd.	DA14 5HT	1-300 3333	21836
UNITED STATES	Lawrence (Massachusetts)	ITT Semiconductors 500 Broadway	01841	617-688-1881	710-342-1357
	Dallas (Texas)	ITT Semiconductors 2995 LBJ Freeway Suite 130	75234	214-243-7851	

MATJ — MATSUSHITA-PANASONIC ELECTRIC CORPORATION OF AMERICA

	Zip Code	Telephone No.	TWX/Telex
ELECTRONIC COMPONENTS DIVISION 1 Panasonic Way, Secaucus, New Jersey	07094	201-348-7276	710-992-8920

MMI — MONOLITHIC MEMORIES INC.

	Zip Code	Telephone No.	TWX/Telex
1165 East Arques Avenue, Sunnyvale, California	94086	408-739-3535	910-339-9229

NECJ — NIPPON ELECTRIC COMPANY, LTD.

			Zip Code	Telephone No.	TWX/Telex
33-1, Shiba Gochome, Minato-ku, Tokyo, Japan			108	(03) 454-1111	NECTOK J22686 Cable MICROPHONE Tokyo
GERMANY	Dusseldorf 1	NEC Electronics GmbH Europe (NECD)* Karlstr. 123-127	4000	0211-08141	NECD 8587415
UNITED STATES	Santa Clara (California)	NEC Electron Inc 3120 Central Expressway	95051	408-241-8222	353475 NECAM SNTA

NECM - NEC MICROCOMPUTERS, INC.

	Zip Code	Telephone No.	TWX/Telex
173 Worcester St. Wellesley, Massachusetts	02181	617-237-1910	710 - 383 - 1745 923434

PHIN – PHILIPS GLOEILAMPENFABRIEKEN

			Zip Code	Telephone No.	TWX/Telex
ELCOMA MARKETING COMMUNICATIONS Building BA, Eindhoven, Netherlands				(040) 723142	51121
ARGENTINA	Buenos Aires (Tablada)	Fapesa I.y.C Av. Crovara 2550		652-7438/7478	21243
AUSTRALIA	Lane Cove	Philips Industries Holdings, Ltd. Elcoma Division 67 Mars Road	2066 N.S.W.	427 0888	21503
AUSTRIA	Wien	Österreichische Philips Bauelemente Industrie G.m.b.H. Treisterstrasse 64	A-1101	62 91 11	131802
BELGIUM	Bruxelles	M.B.L.E. 80 Rue des Deux Gares	B-1070	523 00 00	21420
BRAZIL	Sao Paulo, SP	Ibrape Av. Brigadeiro Faria Lima	1735	(011)211-2600	112 4354
CANADA	Scarborough (Ontario)	Philips Electronics Ltd. Electron Devices Division 601 Milner Avenue	M1B 1M8	292-5161	65-25100 65-25103
DENMARK	København NV	Miniwatt A/S Emdrupvej 115A	DK-2400	(01) 69 16 22	15310
FINLAND	Helsinki 10	Oy Philips Ab Elcoma Division Kaivokatu 8	SF-00100	1 72 71	124011
FRANCE	Paris 11	R.T.C. (RTCF)* La Radiotechnique Compelec 130 Avenue Ledru Rollin	F-75540	355-44-99	680495
GERMANY	Hamburg 1	VALVO (VALG)* UB Bauelemente der Philips GmbH Valvo Haus Burchardstrasse 19	D-2	(040)3296-1	2161891
HONG KONG	Kwai Chung, N.T.	Philips Hong Kong Ltd. Elcoma Div. 15/F Philips Industrial Bldg. 24-28 Kung Yip Street	289	12-24 5121	73660

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PHIN — PHILIPS GLOEILAMPENFABRIEKEN (Cont'd)

			Zip Code	Telephone No.	TWX/Telex
ELCOMA MARKETING COMMUNICATIONS Building BA, Eindhoven, Netherlands				(040) 723142	51121
ITALY	Milano	Philips S.p.A. Sezione Elcoma Piazza IV Novembre 3	I-20124	2-6994	3 30262
JAPAN	Tokyo	Nihon Philips Corporation Shuwa Shinagawa Bldg. 26-33 Takanawa, 3-chome Minato-ku	108	(448) 5611	7226388
KOREA	Seoul	Philips Electronics (Korea) Ltd. Philips House-Elcoma Division 260-199 Itaewon-dong Yongsan-ku		794-4202	27291
MEXICO	Mexico 6, D.F.	Electronica S.A. de C.V. Varsovia No. 36		533-11-80	221771227
NETHERLANDS	Eindhoven	Philips Nederland B.V. Afd. Elonco Boschdijk 525	5600 PB	(040) 79 33 33	51238
NEW ZEALAND	Auckland (St. Lukes)	Philips Electrical Industries Ltd. Elcoma Division 2 Wagener Place		867119	2312
NORWAY	Oslo 3	Norsk A/S Philips Electronica Dept. Sørkedalsveien 6		46 3890	11141
SOUTH AFRICA	Johannesburg (New Doornfontein)	EDAC (Pty.) Ltd. 3rd Fl. Rainer House Upper Railway Rd. & Ove St.	2001	614 - 2362/9	95437786
SPAIN	Barcelona 7	Copresa S.A. Balmes 22		301 63 12	54666
SWEDEN	Stockholm 27	A. B. Elcoma Lidingovagen 50	S-11584	08/679780	10776
SWITZERLAND	Zurich	Philips A. G. Elcoma Dept. Allmendstrasse 140-142	CH-8027	01/43 22 11	52392

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PHIN – PHILIPS GLOEILAMPENFABRIEKEN (Cont'd)

			Zip Code	Telephone No.	TWX/Telex
ELCOMA MARKETING COMMUNICATIONS Building BA, Eindhoven, Netherlands				(040)723142	51121
TAIWAN	Taipei	Philips Taiwan Ltd. San Min Bldg., 3rd Floor 57-1 Chung Shan N. Road Section 2		55 13101-5	21570
UNITED KINGDOM	London	Mullard Ltd. Mullard House Torrington Place	WC1E 7HD	01-580-6633	264341
UNITED STATES	California (Sunnyvale)	Signetics Corporation (SIC)* 811 East Arques Avenue	94086	(408)739-7700	910-339-9203

* Manufacturer Code inside ( ) can be found in Section 33, Manufacturers Code Names & Addresses

PRO – PRO-LOG CORPORATION

	Zip Code	Telephone No.	TWX/Telex
2411 Garden Road, Monterey, California	93940	408-372-4593	910-360-7082

SGAI – SGS-ATES COMPONENTI ELETTRONICI S.P.A.

			Zip Code	Telephone No.	TWX/Telex
Via C. Olivetti 2, Agrate Brianza, Italy			20041	039-650341	330131 330141
ENGLAND	Aylesbury Bucks	SGS-ATES (United Kingdom) Ltd. Walton Street		5977	83245
FRANCE	Paris Cedex 13	SGS-ATES France SA Residence "Le Palatino" 17, Avenue de Choisy	75643	584 2730	250938

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SGAI – SGS-ATES COMPONENTI ELETTRONICI S.P.A.

(Cont'd)

			Zip Code	Telephone No.	TWX/Telex
Via C. Olivetti 2, Agrate Brianza, Italy			20041	039-650341	330131 330141
GERMANY	Grafing Bei Munchen	SGS-ATES Deutschland GmbH Haidling 17	8018	08092-691	041-527370
HONG KONG	Kowloon	SGS-ATES Singapore (PTE) Ltd. 1329 Ocean Centre Canton Road		3-662625	63906
ITALY	Milano	SGS-ATES Componenti Elettroici Correggio 1/3	20149	4695651	330141
SINGAPORE	Singapore	SGS-ATES Singapore (PTE) Ltd. Lorong 4 and 6 Toa Payoh	12	531411	21412
SWEDEN	Marsta	SGS-ATES Scandinavia AB Tingvallavagen 9J Box 30	19501	0760/40120	10932
U.S.A.	Massachusetts (Waltham)	SGS-ATES Semicondcutor Corporation 240 Bear Hill Road	02154	617-890-6688	92-3495

SMC – STANDARD MICROSYSTEMS CORPORATION

	Zip Code	Telephone No.
35 Marcus Boulevard, Hauppage, New York	11787	516-273-3100

SSS – SOLID STATE SCIENTIFIC, INC.

	Zip Code	Telephone No.	TWX/Telex
Montgomeryville, Pennsylvania	18936	215-855-8400	510-661-7267

REGIONAL SALES OFFICES

CALIFORNIA	Sherman Oaks	Solid State Scientific, Inc. 15010 Ventura Blvd. Suite 202	91403	213-995-6666	910-495-1746
FLORIDA	Tampa	Solid State Scientific, Inc. 200 S. Hoover Blvd.	33609	813-877-3301	810-876-9120
ILLINOIS	Deerfield	Solid State Scientific, Inc. 108 Wilmot Rd. Suite 206	60015	312-948-8840	910-692-4022
PENNSYLVANIA	Montgomeryville	Solid State Scientific, Inc. Commerce Dr.	18936	215-364-2025	510-667-6864

SYK – SYNERTEK, INC.

	Zip Code	Telephone No.
3001 Stender Way, Santa Clara, California	95051	408-988-5600

TFK
(Product Identifier)

ALGG – AEG-Telefunken

AMI – American Microsystems Inc.

AMD – Advanced Micro Devices Inc.

ANA – Analog Devices Inc.

APL – Apple Computer Inc.

APP – Applied Data Communications

APS – Applied Systems Corp.

BEC – Beckman Instruments Inc.

BUB – Burr-Brown Research Corp.

CAC – Compas Microsystem

CLI – Control Logic Inc.

CRO – Cromemco Inc.

DEC – Digital Components Group

DIG – The Digital Group Inc.

DIV – Diversified Technology

DSI – Computer Div.
Detection Sciences Inc.

DTI – Data Translatoin Inc.

DTL – Datel-Intersil Inc.

DYB – Dynabyte Inc.

DYN – Dynalogic Corp., Ltd.

E/L – E & L Instruments Inc.

ECD – ECD Corporation

EDSI – Educational Data Systems

EMM – EMM/SESCO

(Product Identifier)

EPA — Electronic Products Associates Inc.

Electronic Solutions, Inc.
5780 Chesapeake Ct., San Diego, CA 92123

ESI — Electronic Solutions

etc.

ETL — Electronic Tool Co.

EURF — Euroka Oy

GenRad
futuredata

FCC — Genrad/Futuredata

FOR — Forth Inc.

FAIRCHILD

FSC — Fairchild Camera & Instrument Corp.

GEN — General Automation Inc.

GENERAL INSTRUMENT

GIC — General Instrument Corp.
GICB — General Instrument Corp.

HUGHES
ELECTRON DYNAMICS DIVISION

HAC — Hughes Aircraft Co.

HUGHES

HACC — Hughes Aircraft Co.

HAS — Harris Semiconductor

HEATH Schlumberger

HEA – Heath Company

HEU – Heurikon Corp.

HITACHI

HITJ – Hitachi, Ltd.

HEWLETT PACKARD

HPA – Hewlitt Packard

ICC – Information Control Corp.

IMI – International Microsystems Inc.

INFINITE

INFINITE INCORPORATED ®

INF – Infinite Inc.

INTERSIL

INL – Intersil Inc.

intel®

ITL – Intel Corp.

MR

MAR – Martin Research

MATC – Matrox Electronic Systems

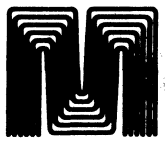
MATJ -- Matsushita Electronics Corp.

MICROTEC

MCT — Microtec

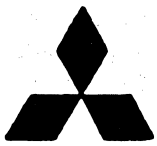
MDB

MDB — MDB Systems, Inc.



MID — Microdata Corp.

MIM — Micro Memory Inc.



MITJ — Mitsubishi Electric Corp.

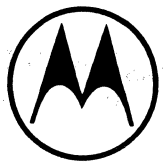
MMI

MMI — Monolithics Memories Inc.

MNC — Micro Networks Corp.

MOSTEK

MOS — Mostek Corp.



MOTA — Motorola Semiconductor Products Inc.

MSCC — Monolithic Systems Corp.

MSS — Millennium Systems Inc.

MOS

MTY — MOS Technology, Inc.

MUL – Multisonics

MULB – Mullard Ltd.

MUP – MUPRO, Inc.

NASB – Nascom Microcomputers Ltd.

NECJ – Nippon Electric Co.

NECM – NEC Micorcomputers Inc.

NSC – National Semiconductor Corp.

OAE – Oliver Advanced Engineering Inc.

OBJ – Cbjective Design Inc.

OHS – Ohio Scientific

PAFJ – Panafacom Ltd.

PAR – Parasitic Engineering

PCM — PC/M, Inc.

PCS — Process Computer Systems Inc.

PHIN — N. V. Philips Gloeilampenfabrieken

PLM — Plessey Peripheral Systems

PRO — Pro-Log Corporation

PRT — Processor Technology Corp.

QUY — Quay Corporation

R2E — R2E-Realisations Etudes Electroniques

RAD — Radio Shack

RCA — RCA Corp.

RCI — RCI/DATA

RKW — Rockwell International Corp.

RTCF – R.T.C. La Radiotechnique-Compelec

RTN – Raytheon Co.

SGAI – SGS-ATES Componenti Elettronici

SIC – Signetics Corporation

SIEG – Siemens Aktiengesellschaft

(Product Identifier)

SMC – SMC Microsystems Corp.

SSM – SSM

SSS – Solid State Scientific Inc.

SYK – Synertek, Inc.

TII – Texas Instruments Inc.

Product Identifier

TLI – TL Industries

TOSHIBA

TOSJ – Toshiba Corp.

TSC – Teledyne Systems Co.

UTEC

UTE -- The Utec Corp.

VALVO

VALG – VALVO GmbH

VECTOR GRAPHIC INC.

VGI – Vector Graphic Inc.

VIRTUAL SYSTEMS

VIR – Virtual Systems Inc.

WESTERN DIGITAL CORPORATION

WDC – Western Digital Corp.

WYLE LABORATORIES COMPUTER PRODUCTS

WLD – Wyle Laboratories/ Computer Products

WINTEK

WTK – Wintek Corp.

ZIA – Zia Tech Corp.

Zilog

ZIL – Zilog Microcomputers

23. MANUFACTURERS' CODES, NAMES & ADDRESSES

FSCM/ NATO No. — D.A.T.A. MFRS.' CODE

MANUFACTURERS IN ORDER OF D.A.T.A. CODE LETTERS

FSCM/NATO No.	D.A.T.A. MFRS.' CODE		
D1597 –	ALGG	* –	AEG-Telefunken, Senenprodukte, Geshoiftsbereich Halbleiter, Postf 1109 Theresieustr 2, D71 Heilbronn West Germany
31471 –	AMI	* –	American Microsystems, Inc., 3800 Homestread Rd., Santa Clara CA 95051
34335 –	**AMD**	* –	**Advanced Micro Devices, Inc., 901 Thompson Pl., Sunnyvale, CA 94086**
	ANA	* –	Analog Devices, Inc., Route 1 Industrial Park, P.O. Box 280, Norwood, MA 02062
	APL	* –	Apple Computer Inc., 20863 Stevens Creek Blvd., B3-C, Cupertino, CA 95014
	APP	* –	Applied Data Communications, 1472 Chambers Rd., Tustin, CA 92680
	APS	* –	Applied Systems Corp., 26401 Harper Ave., St. Clair Shores, MI 48081
	AUC	–	Advanced Micro Computers, 3340 Scott Blvd., Santa Clara, CA 95051
	BEC	* –	Beckman Instruments Inc., 350 No. Hayden Rd., Scottsdale, AZ 85257
	BSO	–	The Boston Systems Office Inc., 469 Moody St., Waltham, MA 02154
13913 –	BUB	* –	Burr-Brown Research Corp., Intl. Airport Industrial Pk., P.O. Box 11400, Tucson, AZ 85734
	CAC	* –	Compas Microsystem (Div. of C.A.C.), 224 SE 16th St., Ames, IO 50010
	CII	–	Chrislin Industries Inc., 31352 Via Colinas, No. 102, Westlake Village, CA 91361
14931 –	CLI	* –	Control Logic, Inc., Nine Tech Circle, Natick, MA 01760
	COM	–	Comptrol, Inc., 9505 Midwest Ave., Cleveland, OH 44125
	CRO	* –	Cromemco Inc., 280 Bernardo Ave., Mountain View, CA 94043
15476 –	DEC	* –	Digital Equipment Corp., Components Group, One Iron Way, Marlborough, MA 01752
34984 –	DGC	–	Data General Corp., Route No. 9, Southboro, MA 01772
	DIG	* –	The Digital Group, Inc., P.O. Box 6528 Denver, CO 80206
	DIV	* –	Diversified Technology, P.O. Box 465, Ridgeland, MA 39157
	DSI	* –	Detection Sciences, Inc., Computer Div., 14050 21st Ave., North, Minneapolis, MN 55441
	DTI	* –	Data Translation, Inc., 4 Strathmore Rd., Natick, MA 01760
	DTL	* –	Datel-Intersil Inc., 11 Cabot Blvd., Mansfield, MA 02048
	DYB	* –	Dynabyte, Inc., 115 Independence Dr., Menlo Park, CA 94025
	DYN	* –	Dynalogic Corp., Ltd., 141 Bentley Ave., Ottawa, Canada K2E 6T7
34312 –	E/L	* –	E & L Instruments, Inc., 61 First St., Derby, CT 06418
55188 –	ECD	* –	ECD Corporation, 196 Broadway, Cambridge, MA 02139
	EDSI	–	Educational Data Systems, 1682 Langley Ave., Irvine, CA 92714
	EFCF	* –★	E.F.C.I.S., B.P. 217 Avenue Des Martyrs, 38019 Grenoble Cedex France
	EMM	* –	EMM/SESCO, 20630 Plummer St., Chatsworth CA 91311
	EPA	* –	Electronic Product Associates, Inc., 1157 Vega St., San Diego, CA 92110
	ESI	* –	Electronic Solutions Inc., 5780 Chesapeake Ct., San Diego, CA 92123
	ETL	* –	Electronic Tool Co., 4736 El Segundo Blvd., Hawthorne, CA 90250

★ **New Manufacturers**

* **See Section 22 for Manufacturers' Logos**

CODE CHANGES THIS EDITION

Manufacturers shown in bold print have sales offices which are included in SECTION 21

23. MANUFACTURERS' CODES, NAMES & ADDRESSES

FSCM/ NATO No. — D.A.T.A. MFRS.' CODE

MANUFACTURERS IN ORDER OF D.A.T.A. CODE LETTERS

FSCM/NATO No.	D.A.T.A. MFRS.' CODE		
	EURF	* —	Euroka Oy, Veneentekijantie 18, 00210 Helsinki 21, Finland
	FCC	* —	Genrad/Futuredata, 6151 W. Century Blvd., Suite 1124, Los Angeles, CA 90045
	FOR	* —	Forth, Inc., 2309 Pacific Coast Hwy, Hermosa Beach, CA 90254
25677 —	**FSC**	* —	**Fairchild Camera & Instrument Corp., Semicon Prods. Group, 464 Ellis St., MS14-1030 Mountain View, CA 94042**
32453 —	GEN	* —	General Automation, 1055 South East St., Anaheim, CA 92805
	GIC	* —	General Instrument Corp., Microelectronics Div., 600 W. John St., Hicksville, NY 11802
	GICB	* —	General Instrument Corp., Regency House, 1-4 Warwick St., London W1, England
73293 —	HAC	* —	Hughes Aircraft Co., 500 Superior Ave., Newport Beach, CA 92663
	HACC	* —	Hughes Aircraft Co., Strategic Systems Div., MS 150/A213, Culver City, CA 90230
34371 —	HAS	* —	Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901
	HEA	* —	Heath Company, Benton Harbor, MI 49022
	HEU	* —	Heurikon Corp., 700 W. Badger Rd., Madison, WI 53713
S4361 —	HITJ	* —	Hitachi, Ltd., Semicon. & IC Div., Nippon Bldg., 6-2, 2-chome, Ohtemachi, Chiyoda-ku, Tokyo 100, Japan
	HPA	* —	Hewlitt Packard, 640 Page Mill Rd., Palo Alto, CA 94304
25055 —	ICC	* —	Information Control Corp., 9610 Bellanca Ave., Los Angeles, CA 90045
	IMI	* —	International Microsystems, Inc., 11554 C Ave., Auburn, CA 95603
	IMS	—	Imsai Manufacturing Corp., 14860 Wicks Blvd., San Leandro, CA 94577
	INF	* —	Infinite, Inc., 1924 Waverly Pl., Melbourne, FL 32901
32293 —	INL	* —	Intersil, Inc., 10710 No. Tantau Ave., Cupertino, CA 95014
34649 —	**ITL**	* —	**Intel Corporation, 3065 Bowers Ave., Santa Clara, CA 95051**
	MAR	* —	Martin Research, 3336 Commerical Ave., Northbrook, IL 60062
	MATC	* —	Matrox Electronic Systems, 5800 Andover Ave., TMR, Montreal, Quebec, H4T 1H4 Canada
01619 —	**MATJ**	* —	**Matsushita Electronics Corp., (Panasonic), 1 Kotari-Yakemachi, Nagaokakyo, Kyoto 167 Japan**
	MCT	* —	Microtec, P.O. Box 60337, Sunnyvale, CA 94088
	MDB	* —	MDB Systems, Inc., 1995 No. Batavia St., Orange, CA 92665
52936 —	MID	* —	Microdata Corporation, 17481 Red Hill Ave., Irvine, CA 92705
	MIM	* —	Micro Memory Inc., 9434 Irondale Ave., Chatsworth, CA 91311
	MIP	—	Micropro International Corp., 1299 Fourth St., San Rafael CA 94901
	MITC	—	Mitel Semiconductor, P.O. Box 13089, Karata, Ottawa, Ontario, Canada
	MITJ	* —	Mitsubishi Electric Corp., Kita-Itami Works, 4-1 Mizuhara, Itami-shi, Hyogo-Ken, Post Code 664 Japan
50364—	**MMI**	* —	**Monolithic Memories, Inc., 1165 E. Orques Ave., Sunnyvale, CA 94068**
	MNC	* —	Micro Networks Corporation, 324 Clark St., Worcester, MA 01606
50088 —	MOS	* —	Mostek Corporation, 1215 W. Crosby Rd., MS 507, Carrollton, TX 75006
04713 —	MOTA	* —	Motorola Semiconductor Products, Inc., 5005 E. McDowell Rd., M360, Phoenix, AZ 85008

★ **New Manufacturers**

* **See Section 22 for Manufacturers' Logos**

Manufacturers shown in bold print have sales offices which are included in SECTION 21

23. MANUFACTURERS' CODES, NAMES & ADDRESSES

FSCM/ NATO No. — D.A.T.A. MFRS.' CODE

MANUFACTURERS IN ORDER OF D.A.T.A. CODE LETTERS

51513 –	MSCC	* –	Monolithic Systems Corp., 14 Inverness Dr., East, Englewood CO 80110
	MSS	* –	Millennium Systems, Inc., 19020 Pruneridge Ave., Cupertino, CA 95014
51284 –	MTY	* –	MOS Technology, Inc., Valley Forge Corporate Ctr., 950 Rittenhouse Rd., Norristown, PA 19401
	MUL	* –	Multisonics, 6444 Sierra Ct., Dublin, CA 94566
K8996 –	MULB	* –	Mullard Limited, Mullard House, Torrington Pl., London WC1E 7HD, England (also under PHIN in Sec. 21)
	MUP	* –	MUPRO, Inc., 424 Oakmead Pkwy, Sunnyvale, CA 94086
	NASB	* –	Nascom Microcomputers Ltd., 92 Broad St., Chesham, Bucks, England
	NECD	–	NEC Electronics (Europe) GmbH, Carlstr, 123-127, 4000 Dusseldorf 1, West Germany (also under NECJ in Sec. 21)
S0543 –	**NECJ**	* –	**Nippon Electric Co., Ltd., 1753 Shimonumabe, Nakahara-ku, Kawasaki City, Japan**
	NECM	* –	**NEC Microcomputers, Inc., 173 Worcester Rd., Wellesley, MA 02181**
	NMS	–	Northwest Microcomputer Systems, 749 River Ave., Eugene, OR 97404
	NOR	–	North Star Computers, Inc., 1440 Fourth Street, Berkeley, CA 94710
27014 –	NSC	* –	National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051
	OAE	* –	Oliver Advanced Engineering Inc., 676 W. Wilson Ave., Glendale, CA 91203
	OBJ	* –	Objective Design, Inc., P.O. Box 20325, Tallahassee, FL 32304
	OHS	* –	Ohio Scientific, Inc., 1333 So. Chillicothe Rd., Aurora, OH 44202
	PAFJ	* –	Panafacom, Ltd., 534 Fukami, Yamato City, Kanagawa 242, Japan
	PAR	* –	Parasitic Engineering, Equinox Div., P.O. Box 6314, Albany, CA 94706
	PAT	–	Patuck Inc., 5073 Russell Ave., Pennsauken, NJ 08109
	PCC	–	PCC Microsystems, 20630 Nordhoff St., Chatsworth, CA 91311
	PCM	* –	PC/M, Inc., 3120 Crow Canyon Rd., San Ramon, CA 94583
	PCS	* –	Process Computer Systems, Inc., 750 No. Maple Rd., Saline, MI 48176
H0002 –	**PHIN**	* –	**N. V. Philips Gloeilampenfabrieken, Product Div., Elcoma, Bldg. BA, Eindhoven, Netherlands**
55154 –	PLM	* –	Plessey Peripheral Systems, 17466 Daimler Ave., Irvine, CA 92714
55051 –	**PRO**	* –	**Pro-Log Corporation, 2411 Garden Rd., Monterey, CA 93940**
	PRT	* –	Processor Technology Corp., 7100 Johnson Industrial Dr., Pleasanton, CA 94566
	QUY	* –	Quay Corporation, P.O. Box 386, Freehold, NJ 07728
	R2E	* –	R2E-Realisations etudes Electroniques, Ave. de Scandinavie, BP 73, 91403 Orsay, France
	RAD	* –	Radio Shack, Div. of Tandy Corp., 1300 One Tandy Center, Fort Worth TX 76102
18714 –	RCA	* –	RCA Corporation, Solid State Div., Route 202, Somerville, NJ 08876
	RCI	* –	RCI/DATA, (Div. of RE-EI Circuits, Inc.), 520 Victor St., Saddle Brook, NJ 07662

★ **New Manufacturers**

* **See Section 22 for Manufacturers' Logos**

Manufacturers shown in bold print have sales offices which are included in SECTION 21

23. MANUFACTURERS' CODES, NAMES & ADDRESSES

FSCM/ NATO No. — D.A.T.A. MFRS.' CODE

MANUFACTURERS IN ORDER OF D.A.T.A. CODE LETTERS

94756 – RKW * – Rockwell International Corp., Microelectronic Dev., POB 3669, Anaheim, CA 92803
RLC – Realistic Controls Corp., 404 W. 35th St., Davenport, IA 52806
RTCF * – R.T.C. La Radiotechnique-Compelec 130, Ave. Ledru-Rollin 75540, Paris Cedex 11, France (Also under PHIN in Sec. 21)
07933 – RTN * – Raytheon Company, Semicon Div., 350 Ellis St., Mountain View, CA 94042
SEC – Standard Engineering Corp., 44800 Industrial Dr., Fremont, CA 94538
A3500 – SGAI * – SGS-ATES Componenti Elettronici SpA., Via C. Olivetti 1, 20041 Agrate Brianza, Milano, Italy
SIA – System Integration Associates, 1510 Russell Rd., Paoli, PA 19301
18324 – SIC * – Signetics Corporation, 811 E. Arques Ave., Sunnyvale, CA 94086 (also under PHIN in Sec. 21)
SIEG * – Siemens Aktiengesellschaft, 8 Munchen 80, Balanstrasse 73, West Germany
SMC * – Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, NY 11787
56341 – SMS – Scientific Micro Systems, Inc., 777 E. Middlefield Rd., Mountain View, CA 94043
SSC – System Service, 3627 Longview Valley Rd., Sherman Oaks, CA 91423
SSM * – SSM Microcomputer Products, 2190 Paragron Dr., San Jose, CA 95131
31019 – **SSS * – Solid State Scientific Inc., Montgomeryville Ind. Center, Montgomeryville, PA 18936**
STP – Southwest Technical Products Corp., 219 W. Rhapsody, San Antonio TX 78216
55576 – **SYK * – Synertek, Inc., P.O. Box 552, 3001 Stender Way, Santa Clara CA 95051**
TAI – Toko America, Inc., 5520 W. Touhey Ave., Skokie, IL 60077
TEKT – Tektronix, Inc., 4455 Sigma Dr., Dallas, TX 75240
THT – Thinker Toys, 1201 10th St., Berkeley, CA 94710
01295 – TII * – Texas Instruments, Inc., Inquiry Answering Service, M/S 308, P.O. Box 225012, Dallas TX 75265
TLI * – TL Industries, Inc., 2573 Tracy Rd., Northwood, OH 43619
S0557 – TOSJ * – Toshiba Corporation, 72 Horikawa-cho, Saiwai-ku, Kawasaki-City, Kanagawa 210, Japan
TSC * – Teledyne Systems Co., 19601 Nordhoff St., Northridge, CA 91324
UTE * – The Utec Corporation, 871 Allwood Rd., Clifton, NJ 07012
D2540 – VALG * – Valvo GmbH, Dept DWE, P.O. Box 993, D2000, Hamburg 1, Germany (also under PHIN in Sec. 21)
VGI * – Vector Graphic Inc., 31364 Via Colinas, Westlake Village, CA 91361
VIR * – Virtual Systems, Inc., 1500 Newell Ave., Suite 406, Walnut Creek, CA 94596
52840 – WDC * – Western Digital Corp., 3128 Red Hill Ave., P.O. Box 2180, Newport Beach CA 92660
07764 – WLD * – Wyle Laboratories/Computer Products, 3200 Magruder Blvd., Hampton VA 23666
WTK * – Wintek Corporation, 1801 South St., Lafayette, IN 47904
XIT – Xitan Inc., P.O. Box 157, 1057 Main St., Hanson, MA 02341
ZIA * – Zia Tech Corporation, 2410 Broad St., San Luis Obispo, CA 95014
ZIL * – Zilog Microcomputers, 10340 Bubb Rd., Cupertino, CA 95014

★ **New Manufacturers**

* **See Section 22 for Manufacturers' Logos**

Manufacturers shown in bold print have sales offices which are included in SECTION 21

SYMBOLS FOLLOWING TYPE NO. & IN TYPE NO. CROSS-INDEX

1, # 2 ..... Used by D.A.T.A. to distinguish systems, devices or components having identical numbers but different capabilities, electrical functions or packages; and software packages or instructions where no numbers are assigned by manufacturers. These numbers include system designations.

SYMBOLS & CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

NOTE: Unless otherwise indicated, all characteristics apply over the entire operating temperature range.

LINE No.

▼– New Type
♦– Revised Specifications
– Non-JEDEC type manufactured outside U.S.A.

MFR. CODE

See Section 23 for Manufacturers' Codes, Names and Addresses.

TECHNOLOGY CODE

3-Letter Code: X X X

TECHNOLOGY
B: Bipolar
M: MOS

TYPE
C: Complementary Symmetry (N+P) — MOS Only
N: N-Channel — MOS Only
P: P-Channel — MOS Only
E: ECL — Bipolar Only
I: I^2L — Bipolar Only
T: TTL — Bipolar Only
X: Not Applicable or Not Specified

PROCESS
D: Schottky Process
G: Silicon Gate
I: Ion-Implanted
N: Silicon Nitride
X: Not Applicable or Not Specified

LOGIC/BLOCK DRAWING PREFIXES
(See Section 19)

A: Read-Write Memories (RAMs-Sec. 11)
B: Read-Only Memories (ROMs-Sec. 12)
Z: Interface & Support (Sec. 13)

OUTLINE DRAWING PREFIXES
(See Section 20)

CH: Chip Package
CN: Can Type
DL: Dual in Line
FP: Flat Pack
MD: Module/Printed Circuit
MO: Standard JEDEC Outline
TO: Standard JEDEC Outline
⍁: Package configuration only shown

2. MICROCOMPUTER SYSTEMS

IN ORDER OF: (1)DATA BITS (2)MANUFACT. CODE & (3)SYSTEM TYPE No.

LINE No.	3 SYSTEM TYPE No.	ORGANIZ-ATION: 1 DATA BITS	ORGANIZ-ATION: ARCHI-TECT-URE	SYS. CONFIGURATION ADDRESSABLE: MEMORY (RAM/ROM) (BYTES)	SYS. CONFIGURATION ADDRESSABLE: I/O DEV @PT WIDTH (D/WDTH)	No. BASIC MICRO INSTR	No. ADDR MODE	INTERR-UPT LEVEL No. & TYPE	INSTRUCT TIME-TYP §CLK CYC *-MIN (s)	No. GEN PUR-POSE REG	STACK LEVEL	SYMBOL: PT-PORT V-VECTORED P-PRIORITY M-MULTIPLE OTHER CAPABILITIES	INSTR SET REF. No.	2 SYSTEM DWG.	MFR. CODE
		4		5	6	7		9	10	12			14	15	•

4 CdF: Card family
ChF: Chip family
CoC: Computer-on-card
SYS: Stand alone microcomputer
μCT: Microcontroller/computer-on-a-chip
*: Available in more than one architecture

5 ▼: Bit capacity No./No. indicates RAM/ROM capacity
*: Internal program ROM is in the form of UV EPROM
ϕ: Paged Memory

• See SYMBOLS AND CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

6 ⍁: I/O Addresses are assigned to unused memory space

7 △: No. of micro instruction, micro codes

9 M: Multiple
P: Priority
V: Vectored
N: Nonmaskable
S: Maskable

10 §: Clock cycle time
*: Minimum
△: Maximum

12 M: Multiple

14 IS: Prefixes instruction set reference number (see Sect. 17)

15 S: Prefixes system drawing number (see Sect. 15)
*: See Sect. 10 (Microprocessors) for Dwg. No. reference

3. SYSTEM COMPONENT INDEX

IN ORDER OF: (1)MFR. CODE (2)SYSTEM TYPE No. (3)COMP. CLASS(4)SUB CLASS &(5)COMP.TYPE No.

LINE No.	5 COMPONENT TYPE No. (NOTE 1)	2 SYSTEM (FAMILY) TYPE No.	3 COMP. CLASS	4 COMP. SUB CLASS	TECHNOLOGY	SYMBOLS: NOTE 1: SOME COMPONENT TYPE NUMBERS LISTED HERE ARE ALSO LISTED IN SECTIONS 10-13. CONSULT CROSS-INDEX FOR PAGE/LINE No. REFERENCE. DESCRIPTION	1 MFR. CODE

4 5 • •

4 COMP: Prepackaged full computing capability
CPU : Central processing unit/microcontroller
CROM: Control and ROM
DEV : Developmental
FPLA : Field Programmable logic array
GAME: Video Game devices (see Type Code Sec. 13)
PROM: Programmable ROM
RAM : Read-write memory
ROM : Read-only memory
uCT : Microcontroller/computer-on-a-chip

INTERFACE & SUPPORT DEVICES (IO)
(see corresponding Type Code in Sec. 13)

CONTROL
IO-01 Program Sequencer/Controller
IO-02 Interrupt System/Controller/Priority Encoder
IO-03 DMA/Memory Interface Controller
IO-04 TTY Interface/Controller
IO-05 Mag. Tape Controller
IO-06 Paper Tape/Card Controller
IO-07 Floppy Disk/Diskette Controller
IO-08 Printer Controller
IO-09 Display Controller/Display
IO-10 Keyboard Encoder/Controller
IO-11 Microcomputer Bus Controller
IO-12 ALU Status/Shift Controller
IO-13 Peripheral Controller

COMMUNICATION
IO-20: Serial Communication/Data Interface Controller
IO-21: Parallel Communication Transceiver
IO-22: Encryption
IO-23: Communication Expander

INTERFACE/DRIVER
IO-30: Parallel Peripheral Interface'(Programmable)
IO-31: Buffer/Driver
IO-32: Clock Generator/Driver
IO-33: General Purpose Interface

CONVERTERS
IO-40: Digital to Analog I/O Converter
IO-41: Analog to Digital I/O Converter
IO-42: Analog to Analog I/O Converter
IO-43: Multiplexer
IO-44: Demultiplexer/Decoder
IO-45: Data Acquisition System

STORAGE
IO-55: Storage/Shift Register/RAM-ROM
IO-56: Latch
IO-57: RAM/ROM/IO

SPECIAL
IO-90: Computational/Arithmetic
IO-92: Special Interface/Support

PERIPHERAL (PE)

STORAGE
PE-01: Floppy Disc Drive/System
PE-02: Rigid/Cartridge Disc Drive/System
PE-04: Mag Tape Drive/System

PRINTERS/DISPLAYS/TERMINALS
PE-10: Printer/Plotter
PE-15: CRT Display
PE-16: LED, etc. Display
PE-20: Terminal/System
PE-21: Terminal-Graphic....CRT
PE-22: Terminal-Graphic....Printer
PE-23: Terminal-Data.....CRT
PE-24: Terminal-Data.....Printer

READERS/PUNCH
PE-40: Card Reader/Punch
PE-42: Tape Reader/Punch

DEVELOPMENT
PE-50: PROM Programmer
PE-51: UV Erasers

SUPPORT
PE-60: Power Supplies
PE-61: Panel/Console/Keyboard
PE-62: Signal Processing

5 CHIP : Single chip device
ChS : Chip set
HYB : Hybrid
MOD : Module/printed circuit board
UNIT : End item equipment (console)
MODS: Module/circuit board set (two or more units)

4.SYSTEM SOFTWARE INDEX

IN ORDER OF: (1)MFR. CODE (2)GENERIC I.D. (3)SYSTEM TYPE No. &(4)SOFTWARE PACKAGE No.

LINE No.	4 SOFTWARE PACKAGE No. ▼-Firmware (SW-D.A.T.A. PREFIX)	2 GENERIC I.D. $-MULTI-SYSTEM APPLICATION	3 SYSTEM TYPE No.	CATEGORY	SOFTWARE LIBRARY NOTE: For Specific Software Compatibility Consult Manufacturer NAME	LANGUAGE	AVAILABILITY/COMPATIBILITY	1 MFR. CODE

2 3 5 •

2 SW: Prefixes software package number

3 MULTI $: Multi System Application

5 SOFTWARE CATEGORY CODES:
ASB : Assembler (Cross-Assemblers, Translators)
BAS : Business Application Software
CMP : Compiler, (Cross-Compiler)
DEB : Debugger
DEV : Development
DIA : Diagonistic
DOS : Disk Operating System
EDT : Editor/Interpreter
LAN : Language Systems
LOA : Loader/Linker/IO (Communications)
MFS : Multifunction Software
MON : Monitor/Executive
OPS : Operating System
SIM : Simulator/Emulator
SSS : Special Support Software (Utility, Formatter, Generator)
SUB : Subroutine Library

5. INSTRUCTION SET INDEX

IN ORDER OF: (1)MANUFACTURER CODE &(2)SYSTEM TYPE No.

LINE No.	2 SYSTEM TYPE No. (IS-D.A.T.A. PREFIX)	No. BASIC INSTR	TOTAL No. INSTRUCTIONS W/VARIATIONS	SYMBOLS: DESCRIPTION	INSTRUCTION SET REFERENCE No.	INSTRUCT FORMAT DWG.	1 MFR. CODE

2 6 7 •

2 IS : Instruction set; prefixes system number

6 IS : Prefixes instruction set reference number (see Sect. 17)

7 F : Prefixes instruction format drawing number (see Sect. 16)

• See SYMBOLS AND CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

SYMBOLS & CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

NOTE: Unless otherwise indicated, all characteristics apply over the entire operating temperature range.

LINE No.

▼ – New Type
♦ – Revised Specifications
– Non-JEDEC type manufactured outside U.S.A.

MFR. CODE

See Section 23 for Manufacturers' Codes, Names and Addresses.

TECHNOLOGY CODE

3-Letter Code: X X X

TECHNOLOGY
B: Bipolar
M: MOS

TYPE
C: Complementary Symmetry (N+P) } MOS Only
N: N-Channel } MOS Only
P: P-Channel } MOS Only
E: ECL } Bipolar Only
I: I^2L } Bipolar Only
T: TTL } Bipolar Only
X: Not Applicable or Not Specified

PROCESS
D: Schottky Process
G: Silicon Gate
I: Ion-Implanted
N: Silicon Nitride
X: Not Applicable or Not Specified

LOGIC/BLOCK DRAWING PREFIXES
(See Section 19)

A Read-Write Memories (RAMs-Sec. 11)
B Read-Only Memories (ROMs-Sec. 12)
Z Interface & Support (Sec. 13)

OUTLINE DRAWING PREFIXES
(See Section 20)

CH: Chip Package
CN: Can Type
DL: Dual in Line
FP: Flat Pack
MD: Module/Printed Circuit
MO: Standard JEDEC Outline
TO: Standard JEDEC Outline
⍁: Package configuration only shown

6. SYSTEM INTERFACE

IN ORDER OF: (1)DATA BITS (2)MFR. CODE (3)SYSTEM TYPE No.

LINE No.	3 SYSTEM TYPE No.	1 DATA BITS	ADDRESSING: TYPE 4	ISOLATED DEVICES @ PORT WIDTH	MEMORY-SPACE DEV @ PT WIDTH	OPERATING MODE: TYPE of OP. 7	No. SERIAL BITS	INTERRUPT: TYPE 9	No LNS	No LEV 11	INITIATION 12	DMA LOC. 13	I/O LINES: ADDR	SENS	CNTL	FLAG	MISC	TRANSFER: INSTR TIME Ffirm (s) 19	OPER. CAPABILITY CODE 20	MAXIMUM BAUD RATE: ASYNC (BPS) 21	SYNC. (BPS) 22	SYSTEM DWG. 23	2 MFR. CODE
								V-vectored Pr-priority P-poll			S-softw,DMA I-interrupt													

4
B : Both isolated & memory space
I : Isolated
M : Memory space

7
P : Parallel
PS : Parallel/serial
S : Serial

9
M : Multiple
P : Polled
Pr : Priority
V : Vectored

11
M : Multiple
U : Unlimited

12
D : DMA
I : Interrupt (hardware)
S : Software

13
CPU : On CPU
EXT : External
N/A : Not available

19
F : Firmware time
§ : Clock cycle time
△ : Max.
* : Min.

20
A : TTL
B : RS232
C : Current loop
D : HINL

21
† : Typical
§ : Words/sec.

22
† : Typical
§ : Words/sec.

23
S : Prefixed system drawing number (see Section 15)

• See SYMBOLS AND CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

SYMBOLS & CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

NOTE: Unless otherwise indicated, all characteristics apply over the entire operating temperature range.

LINE No.

▼– New Type
♦ – Revised Specifications
– Non-JEDEC type manufactured outside U.S.A.

MFR. CODE

See Section 23 for Manufacturers' Codes, Names and Addresses.

TECHNOLOGY CODE

3-Letter Code: X X X

TECHNOLOGY	TYPE		PROCESS	
B: Bipolar	C: Complementary Symmetry (N+P)	MOS Only	D: Schottky Process	
M: MOS	N: N-Channel		G: Silicon Gate	
	P: P-Channel		I: Ion-Implanted	
	E: ECL	Bipolar Only	N: Silicon Nitride	
	I: I^2L		X: Not Applicable or Not Specified	
	T: TTL			
	X: Not Applicable or Not Specified			

LOGIC/BLOCK DRAWING PREFIXES
(See Section 19)

A: Read-Write Memories (RAMs-Sec. 11)
B: Read-Only Memories (ROMs-Sec. 12)
Z: Interface & Support (Sec. 13)

OUTLINE DRAWING PREFIXES
(See Section 20)

CH: Chip Package
CN: Can Type
DL: Dual in Line
FP: Flat Pack
MD: Module/Printed Circuit
MO: Standard JEDEC Outline
TO: Standard JEDEC Outline
⍁: Package configuration only shown

10. MICROPROCESSORS

IN ORDER OF: (1)DATA BITS (2)ARCHITECTURE (3)No. BASIC INSTRUCTIONS & (4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZ. 1 DATA BITS	ORGANIZ. 2 ARCHI-TECTURE	INPUT LOGIC LEVELS TECH NOL.	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RAM/ROM %BIT CONFIG MIXED ▼-bits (BYTES)	MAX. CLOCK FREQ. (Hz)	No Øs	OPER. VOLTAGES V1 (V)	V2 (V)	V3 (V)	MAX. OPER. PWR. DISS. (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	3 No. BASIC INSTR	A D D R	M O D E	DRAWINGS CPU INTERNAL ARCHITECTURE	DRAWINGS OUTLINE	MFR. CODE
		4				7	8	9		11	12	13	14			17			19		•

4
CdS : Card set
Chip : Single chip
ChS : Chip set
MOD : Module/printed circuit board
μCT : Microcontroller/Computer-on-a-chip
▼ : Device operates from injector current source; supply currents in Amps specified in Operating Voltage columns

7
% : Output value (not input) given
§ : Tri-state

• See SYMBOLS AND CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

8
▼ : Bit Capacity
% : RAM/ROM Bit size specified different from data bit size
∅ : On board memory RAM/ROM as indicated
* : Internal ROM is in the form of EPROM

9
Δ : Cycle Time in Seconds
† : Typical

11 12 13 Note: For devices requiring an injector current source, supply current in Amps specified; see Architecture column.

14
⍁: Absolute Max.
† : Typical
♦ : Quiescent power dissipation

17
Δ: No. of micro instruction, micro codes

19
C : Prefixes CPU architecture drawings (see Sect. 18)

INTERPRETER
SYMBOLS & CODES EXPLAINED

11. READ-WRITE MEMORIES (RAMS)

IN ORDER OF: (1)No. WORDS (2)BITS PER WORD (3)WORST CASE R/W CYCLE TIME &(4)TYPE No.

LINE No.	4 TYPE No.	ORGANIZATION 1 No. WORDS	ORGANIZATION 2 BITS PER WORD	MODE	TECHN-OLOGY	3 W/C Min. Rd/Wr CYC.TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED POWER SUPPLY SPAN NEG. (V)	RATED POWER SUPPLY SPAN POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE	MFR. CODE
				5	•	7	8	9	10	11	12			•	•	•

5
- S : Static
- D : Dynamic

7
- $: Access time
- † : Typical
- Δ : Maximum

8
- † : Typical
- ⍁ : Absolute max.
- ♦ : Quiescent power dissipation

9 **10**
- ▼ : Supply current in Amps; device operates from injector current source

11
- † : Typical

12
- † : Typical
- % : Output value (not input) given
- § : Tri-state

12. READ-ONLY MEMORIES (ROMS)

IN ORDER OF: (1)TYPE CODE (2)No. WORDS (3)BITS/WORD (4)ACCESS TIME & (5)TYPE No.

LINE No.	5 TYPE No.	1 TYPE CODE	ORGANIZATION 2 No. WORDS	ORGANIZATION 3 BITS PER WORD	OP. MODE PCM	OP. MODE CODE	TECHNOLOGY	4 MAX. ACCESS TIME (s)	MAX. OPER. PWR. DISS. (W)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYM:*-MIN Δ-MAX S-STATIC D-DYNAMIC DESCRIPT.	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE	MFR. CODE
		3			6		•	8	9	10	11		13				•	•	•

3
- FPLA: Field programmable logic array
- PROM: Programmable ROM
- ROM: Read-only memory
- PSU: Program storage unit

6 2–LETTER CODE: XX

OPERATING MODE
- D: Dynamic
- S: Static

PROGRAM CODE
- C: Mask programmable: custom program
- E: Electrically programmable

7
- Δ : Maximum

8
- $: Read cycle time
- † : Typical

9
- † : Typical
- ⍁ : Absolute max.
- ♦ : Quiescent power dissipation

10 **11**
- ▼ : Supply current in Amps; device operates from injector current source

13
- † : Typical
- % : Output value (not input) given
- § : Tri-state

- • See SYMBOLS AND CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

SYMBOLS & CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

NOTE: Unless otherwise indicated, all characteristics apply over the entire operating temperature range.

OUTLINE DRAWING PREFIXES
(See Section 20)

- CH: Chip Package
- CN: Can Type
- DL: Dual in Line
- FP: Flat Pack
- MD: Module/Printed Circuit
- MO: Standard JEDEC Outline
- TO: Standard JEDEC Outline
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TECHNOLOGY CODE

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- N: N-Channel — MOS Only
- P: P-Channel — MOS Only
- E: ECL — Bipolar Only
- I: I^2L — Bipolar Only
- T: TTL — Bipolar Only
- X: Not Applicable or Not Specified

PROCESS
- D: Schottky Process
- G: Silicon Gate
- I: Ion-Implanted
- N: Silicon Nitride
- X: Not Applicable or Not Specified

LINE No.
- ▼ – New Type
- ♦ – Revised Specifications
- # – Non-JEDEC type manufactured outside U.S.A.

MFR. CODE
See Section 23 for Manufacturers. Codes, Names and Addresses.

LOGIC/BLOCK DRAWING PREFIXES
(See Section 19)
- A: Read-Write Memories (RAMs-Sec. 11)
- B: Read-Only Memories (ROMs-Sec. 12)
- Z: Interface & Support (Sec. 13)

13. INTERFACE AND SUPPORT

IN ORDER OF: (1)TYPE CODE (2)MFR. CODE & (3)TYPE No.

LINE No.	3 TYPE No.	1 TYPE CODE	MAX. No. BITS	INPUT LOGIC LEVELS HIGH (min) (V)	INPUT LOGIC LEVELS LOW (max) (V)	RATED PWR. SUPPLY SPAN NEG. (V)	RATED PWR. SUPPLY SPAN POS. (V)	MAX. OPER. PWR. DISS (W)	OPERATING TEMP. (-)	OPERATING TEMP. (+)	SYMBOLS: §-TRI-STATE *-MIN %-OUTPUT †-TYPICAL ☑-ABS.MAX. DESCRIPTION	DRAWINGS LOGIC/ BLOCK	DRAWINGS OUTLINE	2 MFR. CODE
		3	4	5	6	7	8	9						

3 TYPE CODES
(see corresponding codes in Sec. 3)

CONTROL
- 01: Program Sequencer/Controller
- 02: Interrupt System/Controller/ Priority Encoder
- 03: DMA/Memory Interface Controller
- 04: TTY Interface/Controller
- 05: Mag. Tape Controller
- 06: Paper Tape/Card Controller
- 07: Floppy Disk/Diskette Controller
- 08: Printer Controller
- 09: Display Controller/Display
- 10: Keyboard Encoder/Controller
- 11: Microcomputer Bus Controller
- 12: ALU Status/Shift Controller
- 13: Peripheral Controller

COMMUNICATION
- 20 : Serial Communication/Data Interface Controller
- 21 : Parallel Communication Transceiver
- 22 : Encription/Decription
- 23 : Communication Expander

INTERFACE/DRIVER
- 30 : Parallel Peripheral Interface (Programmable)
- 31 : Buffer/Driver
- 32 : Clock Generator/Driver
- 33 : General Purpose Interface
- 34 : Control Store Sequencer
- 35 : I/O Port

CONVERTERS
- 40 : Digital to Analog I/O/Converter
- 41 : Analog to Digital I/O/Converter
- 42 : Analog to Analog I/O/Converter
- 43 : Multiplerxer
- 44 : Demultiplexer/Decoder
- 45 : Data Acquisition System

STORAGE
- 55 : Storage/Shift Register/RAM-ROM
- 56 : Latch
- 57 : RAM/ROM/IO

SPECIAL
- 90 : Computational/Arithmetic
- 91 : Video Games (see GAME Sec. 3)
- 92 : Special Interface/Support

● See SYMBOLS AND CODES COMMON TO MORE THAN ONE TECHNICAL SECTION

4
- C : No. of Channels
- D : No. devices per package
- F : No. of programmable output frequencies
- G : No. of games
- L : No. output lines
- P : No. output ports
- R : No. Interrupt request levels
- S : Serial transmission
- ∅ : No. clock phases
- △ : Duplex operation receive/transmit

5 † : Typical

6
- † : Typical
- % : Output value (not input)given
- § : Tri-state

7
- ▼ : Supply current in Amps; device operates from injector current source
- ☑ : Absolute max.
- † : Typical
- ♦ : Quiescent power dissipation

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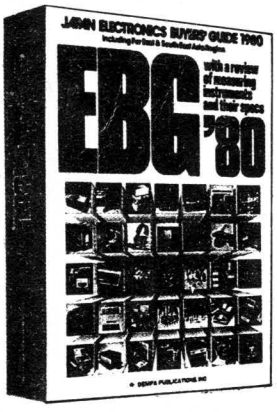

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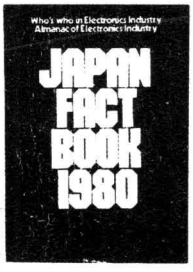

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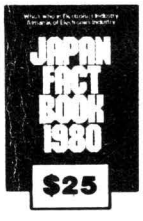

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