CIRRUS LOGIC

ADVANCE PRODUCT BULLETIN

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FEATURES

CL — CD240

Intelligent Multi-Protocol Peripheral (IMP)

Key Features:

- Four full-duplex multi-protocol channels
- Asynchronous, character synchronous and HDLC framing
- 32-bit double-buffered DMA controller for all channels
- Bit rates to 64K baud on transmit and receive
- Independent bit rate generators for transmit and receive
- Digital PLL on each receiver
- NRZ, NRZI and Manchester data encoding supported
- Two independent timers per channel

Asynchronous Operation Features:

- Improved interrupt schemes:
  - — Vectored interrupts to allow direct jump into proper service routines
  - — Good data interrupts™ eliminate need for status checks
- User-programmable and automatic flow control modes:
  - — In-Band (software) via XON, XOFF
  - — Out-of-Band (hardware) via RTS/CTS, DTR/DSR
  - — Line break detection and generation
  - — Special character recognition and transmission

Synchronous Operation Features:

- Programmable sync, frame start/end and idle character
- Optional CRC generation and validation
- Chain/unchain of long frames into multiple buffers

HDLC Features:

- Four 8-bit or two 16-bit frame address matching
- FCS generation and validation
- Header only (small frame) transmission and reception without DMA overhead

Bisync Features:

- ASCII or EBCDIC encoding
- Special character recognition for block separation and CRC processing without host intervention

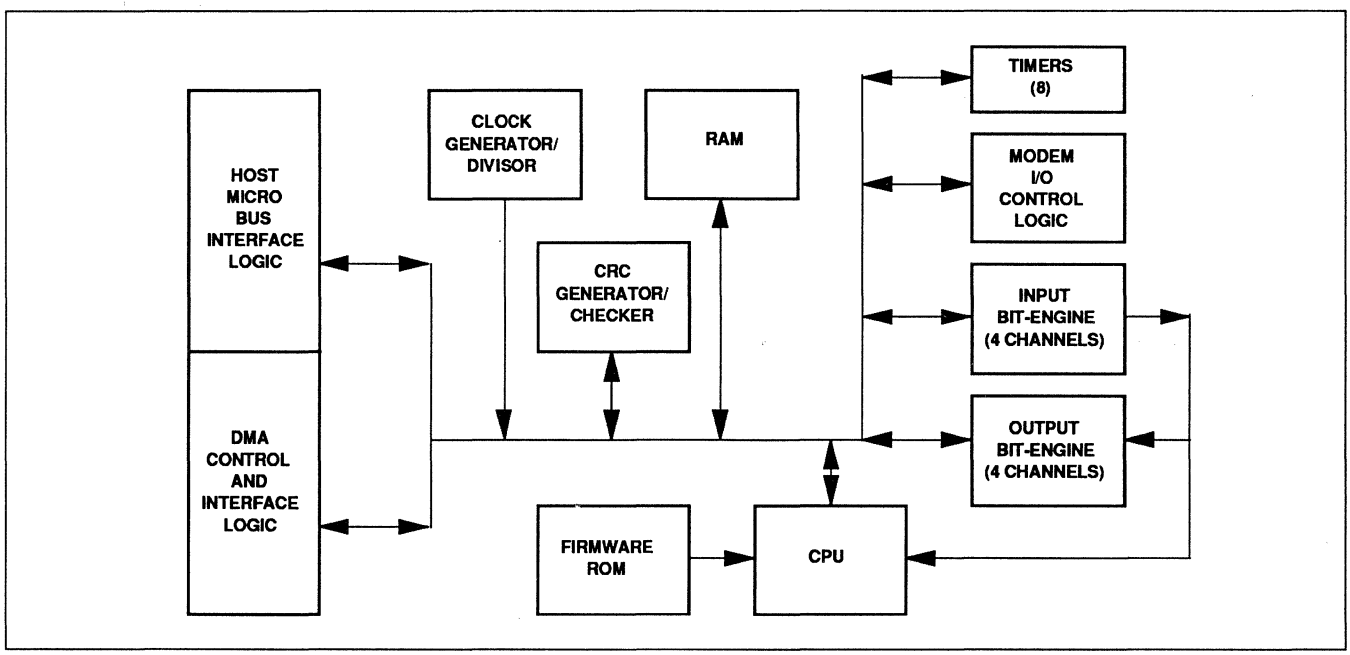

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Figure 1. Functional Block Diagram

FEATURES (Continued)

DMA Controller Features:

- Full 32-bit address and 16-bit data transfers
- Duplicated configuration register set to reduce real-time constraints
- Trickle buffer and block buffer DMA capability on transmit

Other Features:

- Transmit and receive clock rates independently set using a divisor of system clock
- 16 byte receive and transmit FIFOs
- Local and remote maintenance loopback modes
- 5 clock/modem control signals per channel — DTR, CD, DSR, RTS, CTS
- 5- to 8-bit character plus optional parity
- Programmable parity and number of stop bits
- Byte-endian orientation selection pin
- System clock of up to 20 MHz
- Packaged in an 84-pin PLCC
- Advanced low power CMOS process technology

Application Areas:

- ISDN Terminal Equipment
- Data Concentrators/MUX
- Cluster Controllers
- SDLC
- Local Area Networking
- Protocol Converter
- Terminal/Modem
- X.21, X.25 and SS7

OVERVIEW

The CD240 is a sync/async communications controller featuring full on chip DMA for each channel in each direction. Combining the DMA and protocol controllers enables a more efficient Host interface by reducing Host intervention and bus occupancy for both synchronous and asynchronous modes of operation.

The throughput and performance of the CD240 are further improved by the following features:

— optimized firmware sequence for the on-chip protocol handling

— simultaneous usage of more than one buffer area and adding data space to existing buffers during DMA

— on-chip timers keeping track of real time events

— an efficient, fair share mechanism vectored interrupt scheme.

Refer to Figure 1 for the functional block diagram of the CD240.

ADVANTAGES

Unique Features	Benefits
4 multi-protocol serial channels with on-chipDMA	Reduce chip space, increase reliability of the system and cost reduction
On-chip FIFO (16 bytes per direction for each channel)	Greatly reduces real-time response time by the CPU. Cut down overrun/underrun possibilities. Increase DMA efficiency.
On-chip DMA with advanced buffer management schemes (Chain Buffering, Trickle Buffering and Header Segregation)	Efficient utilization of system memory space, reducing CPU overhead of re-programming DMA address locations, byte counts, etc. The buffer management also allows the implementation of Bank Switching or Dual Port memory which increase system performance. The Header Separation eliminates DMA overhead on "small" HDLC frames Rx and Tx.
Two independent timers per channel	Reduce CPU overhead of keeping track of time-out and unnecessary holding of system bus.
Interrupt and DMA handshaking	This allows normal DMA activity to be interspersed with interrupts when special conditions or data errors occur. This is not possible when the DMA and data control functions are separated.

REGISTER SUMMARY (Intel Mode)

Global Registers

Description	Registers	A7	A6	A5	A4	A3	A2	A1	A0	R/W
Global Interrupt Channel Register	GICR	1	0	0	0	0	0	0	0	R/W
Modem End of Interrupt Register	MEOIR	1	0	0	0	0	1	0	1	R/W
Transmit End of Interrupt Register	TEOIR	1	0	0	0	0	1	1	0	R/W
Receive End of Interrupt Register	REOIR	1	0	0	0	0	1	1	1	R/W
Timer Period Register	TPR	1	1	0	1	1	0	0	0	R/W
Priority Interrupt Level Register 1	PILR1	1	1	1	0	0	0	0	1	R/W
Priority Interrupt Level Register 2	PILR2	1	1	1	0	0	0	1	0	R/W
Priority Interrupt Level Register 3	PILR3	1	1	1	0	0	0	1	1	R/W
Channel Access Register	CAR	1	1	1	0	1	1	0	0	R/W
Receive Data Register	RDR	1	1	1	1	1	0	0	0	R
Transmit Data Register	TDR	1	1	1	1	1	0	0	0	W
Global Firmware Revision Code Register	GFRCR	1	0	0	0	0	0	1	0	R
Transmit FIFO Transfer Count	TFTC	1	0	0	0	0	0	1	1	R
Modem Interrupt Status Register	MISR	1	0	0	0	1	0	0	0	R
Transmit Interrupt Status Register	TISR	1	0	0	0	1	0	0	1	R
Receive Interrupt Status Register Low	RISRL	1	0	0	0	1	0	1	0	R
Receive Interrupt Status Register High	RISRH	1	0	0	0	1	0	1	1	R

Channel Registers

Local Interrupt Vector Register	LIVR	0	0	0	0	1	0	1	0	R/W
Channel Command Register	CCR	0	0	0	1	0	0	0	0	R/W
Special Transmit Command Register	STCR	0	0	0	1	0	0	0	1	R/W

REGISTER SUMMARY (Continued)

Description	Registers	A7	A6	A5	A4	A3	A2	A1	A0	R/W
Interrupt Enable Register	IER	0	0	0	1	0	0	1	0	R/W
Channel Option Register 1	COR1	0	0	0	1	0	0	1	1	R/W
Channel Option Register 2	COR2	0	0	0	1	0	1	0	0	R/W
Channel Option Register 3	COR3	0	0	0	1	0	1	0	1	R/W
Channel Option Register 4	COR4	0	0	0	1	0	1	1	0	R/W
Channel Option Register 5	COR5	0	0	0	1	0	1	1	1	R/W
Channel Mode Register	CMR	0	0	0	1	1	0	0	0	R/W
Channel Status Register	CSR	0	0	0	1	1	0	0	1	R
Modem Change Register	MCR	0	0	0	1	1	0	1	1	R/W
Special Character Register 1–4 (Async)	SCHR1–4	0	0	0	1	1	1	X	X	R/W
Receive Frame Address Register 1–4 (Sync)	RFAR1–4									
Special Character Range Low, High (Async)	SCRL, SCRH	0	0	1	0	0	0	0	X	R/W
Transmit Header Address Low, High (Sync)	THAL, THAH									
Transmit Header Control Low	THCL	0	0	1	0	0	0	1	0	R/W
Transmit Header Control High	THCH	0	0	1	0	0	0	1	1	R/W
Receive Header Address Low	RHAL	0	0	1	0	0	1	0	0	R
Receive Header Address High	RHAH	0	0	1	0	0	1	0	1	R
Receive Timeout Period Register Low, High (Async)	RTPRL, H	0	0	1	0	0	1	1	X	R/W
Receive Header Control Low, High (Sync)	RHCL, H	0	0	1	0	0	1	1	X	R
Receive Timer Register Low, High (Async)	RTRL, RTRH	0	0	1	0	1	0	0	X	R
General Timer 1 Low, High (Sync)	GT1L, GT1H	0	0	1	0	1	0	0	X	R/W
Transmit Timer Register (Async)	TTR	0	0	1	0	1	0	1	0	R
General Timer 2 (Sync)	GT2	0	0	1	0	1	0	1	0	R/W
A Receive Buffer Address 0–3	ARBADR0–3	0	1	0	0	0	0	X	X	R/W
B Receive Buffer Address 0–3	BRBADR0–3	0	1	0	0	0	1	X	X	R/W
A Transmit Buffer Address 0–3	ATBADR0–3	0	1	0	1	0	0	X	X	R/W
B Transmit Buffer Address 0–3	BTBADR0–3	0	1	0	1	0	1	X	X	R/W
A Buffer Transmit Byte Count Low	ATBCNTL	0	1	0	1	1	0	0	0	R/W
A Buffer Transmit Byte Count High	ATBCNTH	0	1	0	1	1	0	0	1	R/W
B Buffer Transmit Byte Count Low	BTBCNTL	0	1	0	1	1	0	1	0	R/W
B Buffer Transmit Byte Count High	BTBCNTH	0	1	0	1	1	0	1	1	R/W
A Transmit Buffer Status	ATBSTS	0	1	0	1	1	1	0	0	R/W
B Transmit Buffer Status	BTBSTS	0	1	0	1	1	1	0	1	R/W
Transmit Baud Rate Generator Register	TBPR	1	1	0	0	0	0	0	1	R/W
Transmit Clock Option Register	TCOR	1	1	0	0	0	0	1	0	R/W
Receive Baud Rate Period Register	RBPR	1	1	0	0	1	0	0	1	R/W
Receive Clock Option Register	RCOR	1	1	0	0	1	0	1	0	R/W
CRC Polynomial Select Register	CPSR	1	1	0	1	0	1	0	0	R/W
Modem Signal Value Register — RTS	MSVR-RTS	1	1	0	1	1	1	0	0	R/W
Modem Signal Value Register — DTR	MSVR-DTR	1	1	0	1	1	1	0	1	R/W
Receive FIFO Output Count	RFOC	0	0	1	1	0	0	1	1	R
Receive Current Buffer Address 0–3	RCBADR0–3	0	0	1	1	1	1	X	X	R
A Buffer Receive Byte Count Low	ARBCNTL	0	1	0	0	1	0	0	0	R
A Buffer Receive Byte Count High	ARBCNTH	0	1	0	0	1	0	0	1	R
B Buffer Receive Byte Count Low	BRBCNTL	0	1	0	0	1	0	1	0	R
B Buffer Receive Byte Count High	BRBCNTH	0	1	0	0	1	0	1	1	R
A Receive Buffer Status	ARBSTS	0	1	0	0	1	1	0	0	R
B Receive Buffer Status	BRBSTS	0	1	0	0	1	1	0	1	R

PIN DESCRIPTION

Symbol	NUM	Type	Description
Microprocessor Interface			
V_{cc}	2	I	Power Supply.
GND	4	I	Ground.
$\overline{CS}$	1	I	Chip Select — when low the CD240 registers may be read or written by the Host.
$\overline{AS}$	1	I/O, 3-state	Address Strobe — input when CD240 is the slave. This signal is output when CD240 is the bus master indicating that R/$\overline{W}$, A(0–7) and A(8–31)@ are valid. @ see pin $\overline{ADLD}$ for explanation
$\overline{DS}$	1	I/O, 3-state	Data Strobe — when the CD240 is not a bus master, this is an input used to strobe data into registers during write cycles and enable data onto the bus during read cycles. When the CD240 is a bus master $\overline{DS}$ is an output used to control data transfer to and from system memory.
R/$\overline{W}$	1	I/O, 3-state	Read/$\overline{Write}$ — when the CD240 is not a bus master this pin is an input which determines if a read or write operation is required when the $\overline{CS}$ and $\overline{DS}$ are active. When the CD240 is a bus master R/$\overline{W}$ is an output and indicates a read or write to system memory.
$\overline{DTACK}$	1	I/O, open drain	Data Transfer Acknowledge — when the CD240 is not a bus master this is an output and indicates to the Host when a read or write to the CD240 is complete. When $\overline{BR}$ is driven low by the CD240, $\overline{DTACK}$ is an input which qualifies system bus is no longer in use. When the CD240 is a bus master, $\overline{DTACK}$ is an input which indicates when system memory read and write cycles are complete.
SIZ(0–1)	2	I/O, 3-state	SIZE(0–1) — when not the active bus master these are an inputs which determine the size of the operand being read or written by the Host. When the CD240 is a bus master these are an outputs determining the size of the operand being transferred to or from system memory.
$\overline{IACKIN}$	1	I	Interrupt Acknowledge IN — this input qualified with $\overline{DS}$ and A(0–7), acknowledges CD240 interrupts.
$\overline{IACKOUT}$	1	O	Interrupt Acknowledge OUT — this output is driven low during interrupt acknowledge cycles for which no internal interrupt is valid.
$\overline{IREQ}$(1–3)	3	I/O, open-drain	Interrupt Request (1–3) — these outputs signal that the CD240 has a valid interrupt for modem lead activity [$\overline{IREQ}$(1)], transmit activity [$\overline{IREQ}$(2)], or receive activity [$\overline{IREQ}$(3)].
$\overline{BR}$	1	O, open-drain	Bus Request — this output is used to signal to the Host processor or bus arbiter that bus mastership is required by the CD240.
$\overline{BGIN}$	1	I	Bus Grant IN — this input indicates that the bus is available after the current bus master relinquishes the bus.
$\overline{BGOUT}$	1	O	Bus Grant OUT — this output is asserted when $\overline{BGIN}$ is low and no internal Bus Request has been made. A daisy chain scheme of bus arbitration can be formed by connecting $\overline{BGOUT}$ to $\overline{BGIN}$ of the next device in the chain. If a priority scheme is preferred Bus Requests must be prioritized externally and Bus Grant routed to the $\overline{BGIN}$ of the appropriate device.
$\overline{BGACK}$	1	I/O, open-drain	Bus Grant Acknowledge — as an input this signal is used to determine if another bus master is in control of the bus. As an output it signals to other bus masters that this device is in control of the bus.
$\overline{BERR}$	1	I	Bus Error — if this input becomes active while the CD240 is a bus master the current bus cycle will be terminated, the bus relinquished and an interrupt generated to indicate the error to the Host processor.
A(0–7)	8	I/O, 3-state	Address (0–7) — when the CD240 is not a bus master these pins are inputs, used to determine which registers are being accessed, or which interrupt is being acknowledged. When $\overline{ADLD}$ is low A(0–7) output address bits 8 through 15 for external latching. When the CD240 is a bus master A(0–7) output the least significant byte of the transfer address.

PIN DESCRIPTION (Continued)

Symbol	NUM	Type	Description
Microprocessor Interface (Continued)			
A/D(0–15)	16	I/O, 3-state	Address/Data (0–15) — when the CD240 is not a bus master these pins provide the 16 bit data bus for reading and writing to the CD240 registers. When $\overline{\text{ADLD}}$ is low A/D(0–15) provide the upper address bits A(16–31) for external latching. When the CD240 is a bus master A/D (0–15) provide a data bus for reading and writing to system memory.
$\overline{\text{ADLD}}$	1	O, 3-state	$\overline{\text{Address Load}}$ — is a strobe used to externally latch the upper portion of the system address bus A(8–31). While $\overline{\text{ADLD}}$ is low address bits 16 through 31 are available on A/D(0–15) and address bits 8 through 15 on A(0–7).
$\overline{\text{AEN}}$	1	O, 3-state	$\overline{\text{Address Enable}}$ — this output is used to output enable the external address bus drivers during CD240 DMA cycles.
$\overline{\text{DATDIR}}$	1	O, 3-state	$\overline{\text{Data Direction}}$ — this output is active when either the CD240 is a bus master or the $\overline{\text{CS}}$ pin is low. It is used to control the external data buffers, when low the buffers should be enabled in the CD240 to system bus direction.
$\overline{\text{DATEN}}$	1	O, 3-state	$\overline{\text{Data Enable}}$ — this output is active when either the CD240 is a bus master or the $\overline{\text{CS}}$ and $\overline{\text{AS}}$ pins are low. It is used to enable the external data bus buffers during Host register read/write operations or during DMA operations. For operations on 32 bit buses this signal needs to be gated with A(1) to select the correct half of the data bus.
CLK	1	I	Clock — system clock.
BUSCLK	1	O	Bus Clock — is the system clock divided by 2 which is used internally to control certain bus operations.
$\overline{\text{RESET}}$	1	I	$\overline{\text{Reset}}$ — asynchronously resets the CD240, should be active for a minimum of five clock periods. When $\overline{\text{RESET}}$ is removed the CD240 performs a software initialization of its registers.
TEST	1	I	Test — this must be kept low at all times.
INT/$\overline{\text{MOT}}$	1	I	This pin alters the byte ordering of data during 16-bit transfers to comply with that used in Intel or Motorola processors, it does not alter the bus handshake signals. A different register map is used depending on the state of this pin.
Communications Interface			
$\overline{\text{RTS}}$(0–3)	4	O	$\overline{\text{Request to Send}}$ (0–3).
TXCOUT/$\overline{\text{DTR}}$(0–3)	4	O	Transmit Clock OUT/$\overline{\text{Data Terminal Ready}}$ (0–3) — user selectable via the MSVR-DTR register.
$\overline{\text{CTS}}$ (0–3)	4	I	$\overline{\text{Clear to Send}}$ (0–3).
TXCIN/$\overline{\text{CD}}$(0–3)	4	I	Transmit Clock IN/$\overline{\text{Carrier Detect}}$ (0–3) — when used as transmit clock the state of the pin is still available in the MSVR register.
RXCIN/$\overline{\text{DSR}}$(0–3)	4	I	Receive Clock IN/$\overline{\text{Data Set Ready}}$ (0–3) — when used as receive clock the state of the pin is still available in the MSVR register.
TXD(0–3)	4	O	Transmit Data (0–3) — serial data output for each channel.
RXD(0–3)	4	I	Receive Data (0–3) — serial data input for each channel.

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